Growth and Selective Etch of Phosphorus-Doped Silicon/Silicon–Germanium Multilayers Structures for Vertical Transistors Application

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Abstract

Vertical gate-all-around field-effect transistors (vGAAFETs) are considered as the potential candidates to replace FinFETs for advanced integrated circuit manufacturing technology at/beyond 3-nm technology node. A multilayer (ML) of Si/SiGe/Si is commonly grown and processed to form vertical transistors. In this work, the P-incorporation in Si/SiGe/Si and vertical etching of these MLs followed by selective etching SiGe in lateral direction to form structures for vGAAFET have been studied. Several strategies were proposed for the epitaxy such as hydrogen purging to deplete the access of P atoms on Si surface, and/or inserting a Si or Si0.93Ge0.07 spacers on both sides of P-doped Si layers, and substituting SiH4 by SiH2Cl2 (DCS). Experimental results showed that the segregation and auto-doping could also be relieved by adding 7% Ge to P-doped Si. The structure had good lattice quality and almost had no strain relaxation. The selective etching between P-doped Si (or P-doped Si0.93Ge0.07) and SiGe was also discussed by using wet and dry etching. The performance and selectivity of different etching methods were also compared. This paper provides knowledge of how to deal with the challenges or difficulties of epitaxy and etching of n-type layers in vertical GAAFETs structure.

Keywords: Phosphorus-doped silicon, SiGe, RPCVD, Dopant segregation, Auto-doping, Selective etch

Introduction

As the scaling of complementary metal oxide semiconductor (CMOS) reaches its physical limitation, the short-channel effects significantly weaken the performance of transistors. A solution to these problems is new transistor designs, e.g., GAAFETs (gate-all-around field-effect transistors), which is also considered as the most promising candidate for nanoscale transistors down to 3-nm technology node [1–6]. Lateral and vertical nanowires/nanosheets are main structures according to International Roadmap for Device and Systems (IRDS) 2020 to replace FinFETs [7]. Vertical GAAFETs (or vGAAFETs) have free flexibility design on gate length and have great potential to increase integrated density [4, 8]. There are two main categories to implement vertical nanowire structures: bottom-up and top-down. The bottom-up method introduced metal catalyst, which may bring process compatibility issues [9, 10]. The top-down method is the mainstream in the industry because of its better control of nanowire configuration and its compatibility with FinFET [4, 11–14]. The top-down method to fabricate vertical GAAFETs attracts much attention. Self-alignment gate with accurate gate-length control was a crucial issue.
To achieve better effective gate length control or reduce variation, the gate length could be primarily determined by the thickness of the channel material epitaxially grown on a bottom flat surface, such as Si/SiGe/Si, and SiGe was the channel material [17–20]. Moreover, another critical integration challenge lies in the doping between channel and S/D regions [16, 20, 21], especially with sharp junction control [20]. Compared with the traditional source/drain implantation process, epitaxy process simplifies the fabrication process, reduces surface damage, and achieves uniform doping profile. However, the P-doped Si/SiGe/P-doped Si sandwich structure is difficult to grow epitaxially due to the segregation, auto-doping and out-diffusion phenomena of the most common n-type dopants, phosphorus [22, 23], arsenic [24, 25], and/or antimony [26, 27] at Si/SiGe interface in chemical vapor deposition (CVD) systems. Therefore, the segregated donor atoms gathered at the Si/SiGe interface and the SiGe layer would be doped, which may degrade the transistor performance with high leakage.

One strategy to impede the dopant segregation is to apply very low growth temperature. There are a series of reports to make many efforts to grow n-type doping by molecular beam epitaxy (MBE) [28]; meanwhile, this method has not been applied for CVD. MBE equipment is mostly single-chip design, requiring high vacuum and slow throughput. Moreover, MBE equipment is not compatible with wafer sizes above 8 inches in industry. Therefore, MBE technology is not suitable for industrial mass production applications. However, RPCVD system has strong production capacity and simple equipment structure, which is suitable for IC industry [29]. The first idea for RPCVD growth is to regulate the hydrogen flow in the chamber since the hydrogen is the carrier gas and can affect the kinetics of precursor gases. Li et al. [23] reported that hydrogen changed the bonding structure of host atoms in the surface and reduced the segregation energy by applying low growth temperature in rapid thermal CVD (RTCVD) system. However, the effect of hydrogen has not been explored at Si/SiGe interface in reduced pressure CVD (RPCVD) system. Suvar et al. [30] inserted 30-nm undoped Si spacer layers between P-doped Si and SiGe to lower the P concentration at the interface by a factor of 4 (from $8 \times 10^{19}$ cm$^{-3}$ to $2 \times 10^{19}$ cm$^{-3}$), but the P doping peak cannot be eliminated. Bennett et al. [31] have studied the effect of strain on n-type doping in Si. The solid solubility of doping was increased by introducing tensile strain in Si. Christensen et al. [32] have found no significant dependence of the P diffusivity on the Ge

![Schematic diagram of P-doped Si/SiGe/Si MLs.](image)

Fig. 1  
**a** Schematic diagram of P-doped Si/SiGe/Si MLs.  
**b** P-doping concentration of undoped Si/P-doped Si MLs. 
**c** Ge/Si percentage of Si/P-doped Si MLs. 
**d** No purging and undoped spacer layer were considered.
content in Si$_{1-x}$Ge$_x$ ($0 \leq x \leq 0.22$). And the P diffusion coefficients had little difference between relaxed Si and biaxially compressive-strained SiGe. Zangenberg et al. [33] observed an enhancement of diffusion coefficient by a factor of 2 at 825 °C for relaxed Si$_{0.88}$Ge$_{0.12}$.

In this paper, several methods have been proposed to improve P incorporation in Si in a multilayer of Si/SiGe/Si using RPCVD. In the experiments, different strategies such as hydrogen purge, inserting undoped spacer layers, changing the Si precursor from SiH$_4$ to SiH$_2$Cl$_2$ (DCS), and modulating the strain profile by introducing Si$_{0.93}$Ge$_{0.07}$ sacrificial layer on both sides of SiGe layer have been presented. Furthermore, the selective etch of SiGe was discussed to form thin SiGe layer (intended as channel layer) [6, 34]. The etching characteristics of wet and dry etching tools were also compared. The final structure is intended to be used for vGAAFETs for sub-10-nm technology node in the future.

**Methods**

Si/SiGe/Si multilayers (MLs) were grown on 200-mm Si <100> wafers with RPCVD (ASM Epsilon 2000) equipment. The Si substrates were cleaned with mixture solution of H$_2$SO$_4$ and H$_2$O$_2$, followed by diluted HF to remove native oxide prior to inserting into the load locks of epitaxy chamber. The samples were in situ cleaned by annealing at 1050 °C to remove the native oxide to obtain high-quality surface of Si. The precursors for the Si, Ge, and P were SiH$_4$ (or SiH$_2$Cl$_2$), 10% GeH$_4$ in H$_2$, and 2% PH$_3$ in H$_2$. The growth temperature was 650 °C, while the chamber pressure was kept at 80 Torr during epitaxy. In some experiments, the chamber pressure was reduced to 10 Torr to grow P-doped Si$_{0.93}$Ge$_{0.07}$ layer in the source/drain (S/D) regions. The Ge content in the SiGe channel was kept constant to 0.22. To study the selective etching characteristics, 50 nm nitride/30 nm oxide was deposited as hardmask to protect the nether MLs. Lithography and dry anisotropic vertical etch were performed to form separate cuboid patterns. Selective etch experiments were carried out with wet etch tool of HF (6%):H$_2$O$_2$ (30%):CH$_3$COOH (99.8%) = 1:2:4 and dry etch tool of CF$_4$:O$_2$:He = 4:1:5 [35].

The Si/SiGe/Si MLs were characterized by the techniques of high-resolution (Thermo Scientific Talos F200) transmission electron microscopy (HRTEM), energy-dispersive X-ray spectroscopy (EDX), high-resolution X-ray diffraction (HRXRD), and high-resolution reciprocal lattice map (HRRLM) from Bruker JV Delta-x, scanning...
electron microscopy (SEM) from Hitachi (Japan), and secondary ion mass spectroscopy (SIMS).

Results and Discussion

Epitaxy of P-Doped Si/SiGe/Si MLs

In this study, the incorporation of P in Si and SiGe was initially explored. The ML structures are shown in Fig. 1a. A ML of P-doped Si/undoped Si with increasing PH3 flow was grown, and the layer profiles were examined by SIMS in Fig. 1b. The figure shows P concentration increases and reaches the highest level of $2.6 \times 10^{19} \text{ cm}^{-3}$. Two more samples with profile of ‘P-doped Si/Si$_{0.72}$Ge$_{0.28}$/P-doped Si’ and ‘Si/P-doped Si$_{0.72}$Ge$_{0.28}$/Si’ were designed, and the P-profile is demonstrated in Fig. 1c, d, respectively. In Fig. 1c, a P pile-up is observed at interfaces of P-doped Si/Si$_{0.72}$Ge$_{0.28}$ multilayers. The interfacial P pile-up increases with increasing P concentration from the bottom to the top in the multilayers, and the highest concentration is $1.6 \times 10^{20} \text{ cm}^{-3}$, which is 6 times as much as the concentration in Fig. 1b $(2.6 \times 10^{19} \text{ cm}^{-3})$. In doped Si$_{0.72}$Ge$_{0.28}$ layers (Fig. 1d), P concentrations are remarkably higher, and there are no peaks at the interface. Because of doping, the Ge percentage is slightly increased. This behavior is related to the enhanced adsorption of SiH$_4$ and GeH$_4$ in the presence of PH$_3$. Besides, due to doping, the layer thicknesses are different between Fig. 1c, d, which have the same growth time. It means that P-doping enhances the growth rate of Si$_{0.72}$Ge$_{0.28}$ layers and the absorption of GeH$_4$ while the growth rate of Si is retarded due to P adsorption. These phenomena are consistent with the outcome reported in Refs. [36–38]. From the above, P segregation and auto-doping phenomenon are serious at Si/SiGe interface. The P-doping peak at the Si/SiGe interface makes unintentional doping in the SiGe layer. Since SiGe is intended as the channel layer in the transistors, the inhomogeneous doping profile or high background doping levels would limit device applications [39]. Several methods to eliminate the P peak would be discussed below. For better comparison, all SiGe layers are strained, and the flow ratio of SiH$_4$ (SiH$_2$Cl$_2$) and GeH$_4$ for the SiGe layer was not altered throughout all the experiments.

Impact of Spacer Layers

Undoped Si spacer layers were inserted between the bottom-doped Si layer and undoped SiGe layer to
absorb the excess of P atoms. Figure 2a shows the schematic diagram of the designed structure, and Fig. 2b–d demonstrates the profile results from integrated Si spacers with thickness of (b) 3 nm, (c) 5 nm, and (d) 10 nm. The peaks of P pile-up are reduced, while the Si/Ge percentage and P concentration in Si layers are kept constant as in Fig. 2b–d. The P pile-up level is reduced by 82%, from $4 \times 10^{19}$ cm$^{-3}$ in Fig. 2b to $7 \times 10^{18}$ cm$^{-3}$ in Fig. 2d, when the spacer thickness $X_b$ increased from 3 to 10 nm. Increasing the thickness of undoped Si spacer layers increases the absorption of excessive P atoms. In Fig. 2d, the slope of P-profile at Si$_{0.86}$Ge$_{0.14}$/Si surface is 15.9 nm/dec, while at Si/Si$_{0.86}$Ge$_{0.14}$ interface the slope is 31.3 nm/dec. Meanwhile, too thick Si spacer layer is not an appropriate solution since the sheet resistance increases. Therefore, a trade-off between sheet resistance and uncontrolled of P-profile has to be made for transistors. Figure 2 reveals also the impact of spacer layer between the Si/Si$_{0.86}$Ge$_{0.14}$ layers ($X_b$) was different from the layer between the Si$_{0.86}$Ge$_{0.14}$/Si ($X_i$). In Fig. 2b, c, the spacer thicknesses between the Si$_{0.86}$Ge$_{0.14}$/Si were 3 nm and 5 nm, while in Fig. 2d, no spacer layer was inserted. However, the slope of P-profile at the Si$_{0.86}$Ge$_{0.14}$/Si is the same (about 15.9 nm/dec), although in Fig. 2d the top spacer layer was removed but no influence on the doping profile was observed. From the above results, the P peak was only at the Si/Si$_{0.86}$Ge$_{0.14}$ interface, which was possibly due to the solubility limit; the excess of P atoms may form P–P dimers at surface and be incorporated in the SiGe cap layer. Moreover, there is an auto-doping of P during the SiGe growth after P-doped Si. Therefore, the methods to clear the excess of P atoms or improve the Si solubility have been sought.

**Impact of Hydrogen Purge at the Interface of Si/SiGe/Si MLs**

In this section, Si spacer layer was fixed at 5 nm, and hydrogen purge was introduced to clear the excess of P atoms after the P-doped Si growth. It can be seen from Fig. 3c, d that increasing the hydrogen flow from 20 to 60 sccm and purge time from 2 to 10 min has no obvious effect on the P peak. The doping concentration in Si is $3 \times 10^{19}$ cm$^{-3}$, which is the same as discussed in section

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**Fig. 4** Schematic diagrams of a doping strategy of changing growth chemistry, b experimental structure of Si/SiGe/Si MLs. The SiGe layer was grown with DCS. The purge time was 5 min with flow of 60 sccm after doped Si. The undoped Si spacer layer was 5 nm between bottom-doped Si and undoped SiGe. c Ge/Si profile and P concentration of P-doped Si/Si$_{0.86}$Ge$_{0.14}$/P-doped Si MLs
“Impact of Spacer Layers”. The P peak concentration at the interface is the same with concentration in Si from Fig. 3d. The layer thicknesses are the same under different purge conditions. The P atoms cannot be cleared by hydrogen; this can be explained by the formation of stable P complexes on the surface. By changing parameters such as temperature, pressure, purge time would be helpful [24, 40], but too long purge time is not suitable due to time cost, and high temperature (>950 °C) causes Si-Ge interdiffusion [41].

Impact of Growth Chemistry on P-incorporation
In these experiments, the Si precursor, SiH₄, has been replaced to SiH₂Cl₂ (DCS). In these samples, the growth parameters were the same as before, and the structures contain 5-nm Si spacer layer and the purge time is 5 min with flow of 60 sccm. The idea behind is to investigate whether Cl-based chemistry could clear the excess P atoms by Si surface and reactions of P-Cl, Si-Cl or Ge-Cl could happen [42]. From Fig. 4, the P peak concentration reduces by a factor of 2 (from $2.6 \times 10^{19} \text{cm}^{-3}$ to $1.3 \times 10^{19} \text{cm}^{-3}$), and the P concentrations in Si layers are $2.6 \times 10^{19} \text{cm}^{-3}$. The estimated Ge content is 30%, which is higher than SiGe with SiH₄. The higher Ge content demonstrates that Cl removed preferably the Si atoms at the surface reactions. This result also can be explained by the different relationship of gas flow ratio and Ge concentration with SiH₄ and SiH₂Cl₂ gaseous precursors [32, 43]. Another explanation was that Ge atoms increased hydrogen desorption, then increasing free nucleation sites [44]. The P concentration slope of the Si₀.₇Ge₀.₃/Si interface was 13.2 nm/dec, which was a little sharper than Si₀.₈₆Ge₀.₁₄/Si interface (15.9 nm/dec). The slope of P-profile at the Si/Si₀.₇Ge₀.₃ interface was 20 nm/dec. Therefore, by introducing more HCl or increasing the gas ratio of SiH₂Cl₂ and GeH₄, the segregated P atoms at the doped Si surface can be etched by HCl to form
P-Cl dimers and the P peak concentration at Si/SiGe might be lower [38, 45].

Impact of Ge Content on P-profile
As we discussed before, the incorporation of P in SiGe was remarkably higher than in Si. Therefore, this may raise the idea of adding a few percentages of Ge (7%) in Si spacers (5 nm) could improve the incorporation of P in Si. It is worth mentioning here that our purpose is not to change significantly the character of P-doped Si but impede the segregation of P in Si. In these samples, chamber pressure reduced to 10 Torr during the growth of spacer layers. The doping-dependent growth rate and Ge percentage would be important on this condition. From Fig. 5b, the top and bottom layers were 110 nm Si$_{0.93}$Ge$_{0.07}$ with P concentration of 1 x 10$^{20}$ cm$^{-3}$, the middle layer were 40 nm Si$_{0.78}$Ge$_{0.22}$ with P concentration of 3.5 x 10$^{19}$ cm$^{-3}$. The P concentration slope of P-doped Si$_{0.93}$Ge$_{0.07}$/Si$_{0.78}$Ge$_{0.22}$ was about 33 nm/dec. The slope was not sharp because the Ge percentage difference between the two layers was not large enough. In Fig. 5d, three layers of P-doped Si$_{0.93}$Ge$_{0.07}$/Si$_{0.78}$Ge$_{0.22}$/P-doped Si$_{0.93}$Ge$_{0.07}$ MLs was grown to verify the doping uniformity, and its structure diagram was shown in Fig. 5c. It can be seen, from bottom to top layers, the P concentration was decreasing, which can be explained by the memory effect of P. The residual P atoms in the chamber or diffused P atoms accumulate at the film surface and block free active sites on the surface [38, 39]. Although the P-peak had been eliminated, the segregation between Si$_{0.78}$Ge$_{0.22}$ and Si$_{0.93}$Ge$_{0.07}$ was still serious.

Selective Etching Characteristics of Si/SiGe/Si MLs
When the ML structure is successfully grown (using the above growth strategies), the NWs have formed by vertical etch using SiO$_2$/SiN as hardmask. Afterward, SiGe layer has to be selectively etched to Si in the lateral direction to form the channel layer with a designed width. In these experiments, two types of ML structures have been chosen: P-doped Si/SiGe/P-doped Si (sample-1, in Fig. 2c) and P-doped Si$_{0.93}$Ge$_{0.07}$/Si$_{0.78}$Ge$_{0.22}$/P-doped Si$_{0.93}$Ge$_{0.07}$ (sample-2, in Fig. 5b). These choices are made according to above discussions where the out-diffusion of P has been (partially) suppressed, as well as the perspectives of device application are considered.
The etch in the vertical direction was performed by dry etch, while for lateral etch a selective dry or wet etching was applied. The etching profiles of sample-1 are shown in Fig. 6a, b. And the TEM image and EDS mapping of Fig. 6a has been shown in Fig. 7. In these experiments, the hardmask is oxide/nitride. Figure 6a shows after 11.5 s dry etching of CF$_4$/O$_2$/He. The etch selectivity of Si$_{0.86}$Ge$_{0.14}$ and P-doped Si is 5.8. Figure 6b shows that after 20 min wet etch of HF (6%)/H$_2$O$_2$ (30%)/CH$_3$COOH (99.8%). The wet etch has removed the hardmask (SiO$_2$/SiN), and as a result, Si cap layer was etched ~10 nm as well. As discussed in section "Impact of Spacer Layers", there is a P pile-up at the P-doped Si/Si$_{0.86}$Ge$_{0.14}$ interface. The wet etch is sensitive to the doping level; therefore, the first interface was etched faster. As a result, the front etch interface is not vertical and it is faceted or angled. The average selectivity was less than 4.2. Comparing the two etching methods, dry etch is sensitive to Ge percentage with better selectivity of SiGe, while wet etch is sensitive to dopant concentration. The etchings of sample-2 are also studied in Fig. 6c, d. Similar phenomena were observed in this sample, while the SiGe selective etched depths were deeper (Fig. 6a, c) due to higher Ge percentage. In dry etch, the selectivity of Si$_{0.78}$Ge$_{0.22}$ and P-doped Si$_{0.93}$Ge$_{0.07}$ was 6.3, while in wet etch, the average selectivity was less than 2.5. Therefore, dry etch was a better choice in consideration of etching uniformity and selectivity.

Further analyses were performed to investigate the strain after etch steps in sample-1 and sample-2. Figure 8a–h shows (004) rocking curves (RCs) from these samples as follows: as-grown, after vertical etch, and SiGe lateral etch using wet and dry etching. In RC analysis, the broadening (full-width-half-maximum or FWHM) is an indicator for the defect density, and the position of SiGe peak compared to Si determines the strain amount in the layer. We emphasize here that the peak broadening can be also due to the thin thickness of the layer. Therefore, it will be difficult to distinguish from RC analysis the contribution of defect density, but we can only compare FWHM in some extensions in these analyses. In these RCs, sample-1 (Fig. 8a–d) has a single SiGe layer; meanwhile, sample-2 (Fig. 8e–h) shows two peaks representing 7% and 22% Ge. For As-grown samples, an interference of X-ray beam is observed, which causes thickness layer fringes. The emerging of these fringes shows a high-quality SiGe/Si interface. In RCs, of sample-1 and sample-2, the Ge peak has shifted toward the Si substrate peak indicating strain relaxation. No further shift of Ge peak has been detected after lateral dry etch of SiGe. This is a promising outcome for the transistor performance since the carrier mobility in the channel region is dependent on
the strain. Meanwhile, the strain has been more relaxed for the wet-etched SiGe, and more shift toward the substrate peak has been observed. This shows that the wet etch is not suitable for the lateral SiGe etch, forming the channel layer.

Further X-ray analyses were performed to find out more information about the defect density in the samples in Fig. 9a–h. HRRLMs, which are based on two-dimensional measurements, were performed here as shown in Fig. 9a–h. The indicator for the defect density in HRRLMs is the broadening of SiGe layer along ω-direction (ω is the incident beam angle). The position of Si and SiGe peaks provides the strain components in parallel and perpendicular to the growth direction. In sample-1 and sample-2, the as-grown SiGe layers show minor ω-broadening, and the layer is aligned to the Si showing fully-strained SiGe layers (see Fig. 9a, e). Figure 9b shows the sample after the vertical etch, the SiGe peak has shifted toward the Si substrate in a similar way in RC results in Fig. 8b indicating strain relaxation. But surprisingly, the lateral dry-etched sample (Fig. 9c) shows a clear ω-broadening of SiGe peak along with a shift in the reciprocal space, which is in direction out from the alignment with the Si peak. However, the wet-etched sample (in Fig. 9d) is fully-strain-aligned and has layer intensity lower than the dry-etched one (in Fig. 9c). In this case, it is expected that the generated defects have different origins in these samples since the nature of etch process is different. Sample-2 contains two SiGe layers; the Si₀.₉₃Ge₀.₀₇ peak is survived after etch in both vertical and lateral directions, while Si₀.₇₈Ge₀.₂₂ is disappeared after vertical etch showing full strain relaxation (Fig. 8f–h). The poor process stability of sample-2 could root from P-doping, which promote formation of misfit dislocations.

Conclusions

In this work, the epitaxy of P-doped Si/SiGe/P-doped Si MLs along with etching of these MLs as initial structures for vGAAFET has been investigated. Firstly, the incorporation of P in Si/SiGe/Si MLs was studied. Different strategies for the epitaxy and ML structure have been proposed to eliminate the P-segregated peak at the interface of Si/SiGe heterostructure. From experiments, inserting undoped spacer layer could decrease the P peak. Hydrogen purge to clear the excess P atoms
was not very helpful and stable P-P dimers could not be entirely removed. Substituting SiH₄ with SiH₂Cl₂ as Si precursor to introduce Cl chemistry during the growth decreased the segregated P peak remarkably due to Cl active surface reactions. The impact of Si₀.₉₃Ge₀.₀₇ spacer layers after P-doped Si was also investigated. The results showed that the P peak at the SiGe interface disappeared, while the P incorporation in these layers improved by an order magnitude. In the second part of this study, the vertical etch of Si/SiGe/Si ML was performed to form NWs, and later, in these NWs, the SiGe was selectively wet- or dry-etched. The wet etching was sensitive to dopant concentration; meanwhile, dry etching was sensitive to Ge content. Dry etch was more appropriate for n-type
structures with uniform etching profile and higher selectivity. For P-doped Si/\text{SiGe}_{0.07}/P-doped Si MLs, the selectivity was 5.8 with dry etch and 4.2 for wet etch. The selectivity of P-doped Si/\text{SiGe}_{0.07}/Si/\text{SiGe}_{0.22}/P-doped Si/\text{SiGe}_{0.07} MLs was 6.3 with dry etch and 2.5 with wet etch. The strain in SiGe was mostly preserved in Si/SiGe/Si multilayers and written the articles. HHR and HLZ were the supervisors for the films’ design and characterization, and carried out the epitaxy process of Si/SiGe/Si multilayers and writing the paper. Authors’ Contributions CL and HLL acknowledge project Y71C01X001, and GLW and HHR acknowledge project Grant Nos. 2016YFA0301701, 2019B090909006, 2019B090904015, 2017ZX02315001-002, and 2016112.

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References
1. Guerf Y, Larrieu G (2016) Vertical silicon nanowire field-effect transistors with nanoscale gate-all-around. Nanoscale Res Lett 11:1–7
2. Barraud S, Coquard R, Casse M et al (2012) Performance of omega-shaped-gate silicon nanowire MOSFETs with diameter down to 8 nm. IEEE Electron Device Lett 33:1526–1528
3. Bangsaruntip S, Balakrishnan K, Cheng SL et al (2013) Density scaling with gate-all-around silicon nanowire MOSFETs for the 10 nm node and beyond. IEEE International Electron Devices Meeting (IEDM), New York
4. Veloso A, Altamirano-Sanchez E, Brus S et al (2016) Vertical nanowire FET integration and device aspects. In: Rozeboom F, Narayanan V, Kukush-ima K (eds) Silicon compatible materials, processes, and technologies for advanced integrated circuits and emerging applications. Electrochemical Soc Inc, Pennington, pp 31–42
5. Radamson HH, Zhang YB, He XB et al (2017) The challenges of advanced CMOS process from 2D to 3D. Appl Sci-Basel 7:32
6. Radamson HH, He X, Zhang Q et al (2019) Miniaturization of CMOS. Micromachines, 2019:10
7. International Roadmap for Devices and Systems (IRDS TM) 2017 edn.
8. Song T (2020) Many-tier vertical GAAFET (V-FET) for ultra-miniaturized standard cell designs beyond 5 nm. IEEE Access 8:149984–149998
9. Salem B, Rosaz G, Pauc N, et al. Electrical characterization of horizontal and vertical gate-all-around Si/SiGe nanowires field effect transistors. In: IEEE Silicon Nanoelectronics Workshop, New York. IEEE, 2014.
10. Goldberger J, Hochbaum AI, Fan R et al (2006) Silicon vertically integrated nanogate field effect transistors. Nano Lett 6:973–977
11. Mertens H, Ritzenhailer R, Pena V, et al. Vertically stacked gate-all-around Si nanowire transistors: key process optimizations and ring oscillator demonstration. IEEE International Electronic Devices Meeting. New York: IEEE, 2017.
12. Witters L, Airmira H, Sebaal F et al. (2017) Strained Germanium gate-all-around pMOS device demonstration using selective wire release etch prior to replacement metal gate deposition. IEEE Trans Electronic Devices 64:4587–4593
13. Chu CL, Wu K, Luo GL et al (2018) Stacked Ge-nanosheet GAAFETs fabricated by Ge/Si multilayer epitaxy. IEEE Electron Device Lett 39:1133–1136
14. Huang YS, Lu FL, Tsou YJ et al (2018) Vertically stacked strained 3-GeSn-nanosheet pGAAFETs on Si using GeSn/Gd epitaxial growth and the optimum selective channel release process. IEEE Electron Device Lett 39:1274–1277
15. Radamson HH, Zhu H, Wu Z et al. (2020) State of the art and future perspectives in advanced CMOS technology. Nanomaterials 10:1555
16. Veloso A, Eneman G, Huynh-Bao T, et al. Vertical nanowire and nanosheet FETs: device features, novel schemes for improved process control and enhanced mobility, potential for faster and more energy efficient circuits. In: 2019 IEEE International Electron Devices Meeting (IEDM). IEEE, 2019.
17. Yin X, Zhu H, Wang G et al. (2019) Vertical sandwich gate-all-around field-effect transistors with self-aligned high-k metal gates and small effective-gate-length variation. IEEE Electron Device Lett 41:8–11
18. Veloso A, Huyhn-Bao T, Matagne P et al. (2019) Nanowire and nanosheet FETs for ultra-scaled, high-density logic and memory applications. Solid-State Electron 168:107736
19. Singh N, Buddha haru KD, Manhas SK et al. (2008) SiGe nanowire devices by top-down technology and their applications. IEEE Trans Electronic Devices 55:3107–3118
20. Veloso A, Parascivu V, Vecchio E, et al. Challenges on surface conditioning in 3D device architectures: triple-gate FinFETs, gate-all-around lateral and vertical nanowire FETs. In: Hatton T, Muscat A, Saga K, et al. 15th International Symposium on Semiconductor Cleaning Science and Technology, 2017, 3–20.
21. Veloso A, De Keersgieter A, Matagne P et al. (2017) Advances on doping strategies for triple-gate FinFETs and lateral gate-all-around nanowire FETs and their impact on device performance. Mater Sci Semiconductor Process 2017:62
22. Nutzel JF, Holzmann M, Schittenhelm P et al. (1996) Segregation of n-dopants on SiGe surfaces. Appl Surf Sci. 102/98–101
23. Li YJ, Huang CT, Sturm JC (2012) The effect of hydrogen on the surface segregation of phosphorus in epitaxially grown relaxed Si$_n$Ge$_{1-n}$/Si films by rapid thermal chemical vapor deposition. Appl Phys Lett 101:4
24. Zhang J, Turner SG, Chiam SY et al (2006) Sharp n-type doping profiles in Si/SiGe heterostructures produced by atomic hydrogen etching. Surf Sci 600:2288–2292
25. Ikuta T, Miyamani Y, Fujita S et al (2007) Atmospheric in situ arsenic-doped SiGe selective epitaxial growth for raised-extension N-type metal-oxide-semiconductor field-effect transistor. Jpn J Appl Phys Part 1 Regul Pap Brief Commun Rev Pap 46:1916–1920
26. Yurasov DV, Drozdov MN, Zakharov ND et al (2014) Segregation of Sb in SiGe heterostructures grown by molecular beam epitaxy: Interdependence of growth conditions and structure parameters. J Cryst Growth 396:66–70
27. Portavoce A, Berbezier I, Gas P et al (2004) Sb surface segregation during epitaxial growth of SiGe heterostructures: the effects of Ge composition and biaxial stress. Phys Rev B 69:5
28. Ni W-X, Ekberg J, Joelsson K et al (1995) A silicon molecular beam epitaxy system dedicated to device-oriented material research. J Cryst Growth 157:285–294
29. Wang G (2019) Investigation on SiGe selective epitaxy for source and drain engineering in 22 nm CMOS 409 technology node and beyond. Springer, London
30. Suvar E, Christensen J, Kuznetsov A et al (2003) Influence of doping on thermal stability of Si/Si1-xGe_x/Si heterostructures. Mater Sci Eng B Solid State Mater Adv Technol 102:53–57
31. Bennett NS, Radamson HH, Beer CS et al (2008) Enhanced n-type dopant solubility in tensile-strained Si. Thin Solid Films 517:331–333
32. Christensen J, Kuznetsov AL, Radamson H et al (2001) Phosphorus diffusion in Si1-xGex defect and diffusion forum. Trans Tech Publ 1994–1999:709–716
33. Zangenberg NR, Fage-Pedersen J, Hansen JL et al (2003) Boron and phosphorus diffusion in strained and relaxed Si and SiGe. J Appl Phys 94:3883–3890
34. Teams NLIR. Nanosheet transistor as a replacement of FinFET for future nodes: device ents. VLSI Technology and Circuits, 2020.
35. Li J, Wang W, Li Y et al (2019) Study of selective isotropic etching Si1-xGex in process of nanowire transistors. J Mater Sci Mater Electron 31:134–143
36. Murota M, Sakuraba M, Tillack B (2006) Atomically controlled processing for group IV semiconductors by chemical vapor deposition. Jpn J Appl Phys Part 1 Regul Pap Brief Commun Rev Pap 45:6767–6785
37. Hartmann J, Bogumilowicz Y, Holliger P et al (2003) Reduced pressure chemical vapour deposition of SiGe virtual substrates for high mobility devices. Semicond Sci Technol 19:311
38. Hartmann JM, Clavelier L, Jahan C et al (2004) Selective epitaxial growth of boron- and phosphorus-doped Si and SiGe for raised sources and drains. J Cryst Growth 264:36–47
39. Yang M, Carroll M, Sturm JC et al (2000) Phosphorus doping and sharp profiles in silicon and silicon-germanium epitaxy by rapid thermal chemical vapor deposition. J Electrochem Soc 147:3541–3545
40. Grahn JV, Fosshaug H, Jargellius M et al (2000) A low-complexity 62-GHz (f(T)) SiGe heterojunction bipolar transistor process using differential epitaxy and in situ phosphorus-doped poly-Si emitter at very low thermal budget. Solid-State Electron 44:549–554
41. Zhang QZ, Tu HL, Gu SH et al (2018) Influence of rapid thermal annealing on Ge–Si interdiffusion in epitaxial multilayer Ge0.3Si0.7/Si superlattices with various GeSi thicknesses. ECS J Solid State Sci Technol 7:671–676
42. Sedgwick TO, Agnelo PD, Ngoc DN et al (1991) High phosphorus doping of epitaxial silicon at low-temperature and atmospheric-pressure. Appl Phys Lett 58:1896–1898
43. Suvar E, Radamson HH, Grahn JV (2002) Phosphorus profile control in low-temperature silicon epitaxy by reduced pressure chemical vapor deposition. Mater Sci Eng B Solid State Mater Adv Technol 89:314–318
44. Hartmann J, Loup V, Rolland G et al (2002) SiGe growth kinetics and doping in reduced pressure-chemical vapor deposition. J Cryst Growth 236:10–20
45. Ikuta T, Fujita S, Iwamoto H et al (2008) Characteristics of in-situ phosphorus-doped silicon selective epitaxial growth at atmospheric pressure. J Cryst Growth 310:4507–4510

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