Sneh Saurabh and M. Jagadesh Kumar, "Investigation of the Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field Effect Transistor," *IEEE Trans. on Electron Devices*, Vol. 58, pp. 404-410, February 2011.

Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field Effect Transistor

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Abstract—In this paper, we propose the application of a Dual Material Gate (DMG) in a Tunnel Field Effect Transistor (TFET) to simultaneously optimize the on-current, the off-current and the threshold voltage, and also improve the average subthreshold slope, the nature of the output characteristics and the immunity against the DIBL effects. We demonstrate that if appropriate work-functions are chosen for the gate materials on the source side and the drain side, the tunnel field effect transistor shows a significantly improved performance. We apply the technique of DMG in a Strained Double Gate Tunnel Field Effect Transistor with a high-k gate dielectric to show an overall improvement in the characteristics of the device along with achieving a good on-current and an excellent average subthreshold slope. The results show that the DMG technique can be applied to TFETs with different channel materials, channel lengths, gate-oxide materials, gate-oxide thicknesses and power supply levels to achieve significant gains in the overall device characteristics.

Index Terms—Dual Material Gate, Tunnel Field Effect Transistor, on-current, off-current, threshold voltage, strain.
I. INTRODUCTION

Tunnel Field Effect Transistors (TFETs) exhibit an excellent subthreshold swing and a very low leakage current and hence are being actively investigated for future low power CMOS applications [1-20]. However, TFETs suffer from a low on-current (I\textsubscript{ON}) and therefore, various techniques to improve the I\textsubscript{ON} in a TFET have been suggested [4-14]. The mechanism of current transfer and the saturation in the output characteristics in a TFET is quite different from a conventional MOSFET [16]. As a result, TFETs often exhibit delayed saturation in the output characteristics. This can potentially be detrimental for CMOS applications, and therefore the nature of the output characteristics must be carefully considered while designing TFETs. Also, the dependence of the drain current on the drain voltage in a TFET is different from a conventional MOSFET [16, 18]. Strong DIBL effects is sometimes manifested in a TFET and this can severely limit the utility of the device [18]. Therefore, to employ TFET for low power CMOS applications, it is desirable that in addition to improving the on-current and the subthreshold swing, the overall device characteristics of the TFET be improved. In this paper, we propose the application of a Dual Material Gate (DMG) [21-23] in a Double Gate Tunnel Field Effect Transistor (DGTFET) and demonstrate using 2D device simulations that by engineering the work functions of the dual gates, it is possible to simultaneously optimize the on-current (I\textsubscript{ON}), the off-current (I\textsubscript{OFF}) and the threshold voltage (V\textsubscript{T}), and also improve the average subthreshold slope (SS\textsubscript{AVG}), the nature of the output characteristics and the immunity against DIBL effects.

It has already been demonstrated in the previous works that a conventional DGTFET suffers from an unacceptably low I\textsubscript{ON} [4-10, 20]. The DMG technique alone cannot bring the I\textsubscript{ON} of a DGTFET to that of the MOSFET levels. It has also been shown
that when the channel is composed of a smaller band-gap material, the $I_{ON}$ in a TFET improves dramatically [10-14]. Therefore, we demonstrate the application of the DMG technique in a TFET composed of a small band-gap material so that the $I_{ON}$ is good enough for practical purposes. In ref. [10], the Strained DGTFET (SDGTFET) has been demonstrated to improve the $I_{ON}$ and the subthreshold swing. SDGTFET is structurally same as a DGTFET, except that the silicon body is composed of SiGe free sSOI. The strain in an SDGTFET is controlled by the Ge mole-fraction ($x$) that has been used to fabricate the sSOI [25-27]. Since the introduction of strain decreases the band-gap of the silicon, an SDGTFET shows a remarkably improved device performance [10]. In ref. [5], it has been shown that a high-$k$ gate dielectric improves the coupling between the gates and the tunnel junction resulting in an improved performance of a DGTFET. Therefore, we demonstrate the application of the DMG technique in an SDGTFET with a high-$k$ gate dielectric to not only achieve an improved $I_{ON}$ and $SS_{AVG}$ but also improve the overall performance of the device. It is also demonstrated that, using the additional handle of the DMG, the scalability of the TFET can be extended below 20 nm channel lengths. Finally, considering the potential application of a TFET as a low power device, the suitability of DMG-SDGTFET is studied at $V_{DD} = 0.5$ V [20].

The rest of this paper is organized as follows: Section II describes the structure of a DMG-DGTFET and the simulation model used in this study. Section III presents simulation results for a DMG-DGTFET and demonstrates the advantages of using a DMG. In this section the channel length of the device is taken as 50 nm since the physical phenomenon are easier to appreciate at comparatively larger device dimensions. Section IV demonstrates the improvement in the characteristics of the device due to DMG in an SDGTFET. In this section the channel length is taken to be 25 nm. The analysis of the
DMG-SDGTFET has been done for $V_{DD} = 1.0$ V followed by $V_{DD} = 0.5$ V. Finally, Section V draws important conclusions out of this study.

II. DEVICE STRUCTURE AND SIMULATION MODEL

Fig. 1 shows the cross-sectional view of the proposed DMG-DGTFET in which both the top and the bottom gates are composed of materials with two different work functions. We refer to the gate closer to the source as the tunnel-gate and the one closer to the drain as the auxiliary-gate. The fabrication of a DMG-DGTFET could be done using the techniques reported for fabricating a DMG-FET [21,22]. All the simulations have been carried out using ATLAS version 1.12.1.R [24]. Since the tunneling process is non-local, spatial profile of the energy bands and the band gap narrowing effects are included [24]. We have used non-local tunneling model in this study and validated our simulation model using ref. [5]. We have taken the source and drain doping profiles as abrupt throughout our simulations as in earlier works [4, 5, 10, 12, 15]. The simulation model used in this paper, including the tunneling model and the model for strained silicon, has also been used in ref. [10, 15].

The device parameters used are: source doping = $10^{20}$/cm$^3$, drain doping = $5 \times 10^{18}$/cm$^3$, body doping = $10^{17}$/cm$^3$, silicon body thickness ($t_{si}$) = 10 nm and gate oxide thickness ($t_{ox}$) = 3 nm, channel length ($L$) = 50 nm, tunnel gate length ($L_{tunn}$) = 20 nm and auxiliary gate length ($L_{aux}$) = 30 nm.

III. DUAL MATERIAL GATE DGTFET

First, we analyze the impact of the work-function of the auxiliary-gate ($\Phi_{aux}$) on the $I_{OFF}$ in a DMG-DGTFET. Fig. 2(a) and 2(b) show the change in the band diagram of
the device as $\Phi_{aux}$ is increased, keeping $\Phi_{tunnel}$ fixed at 4.0 eV. In the off-state (Fig. 2(a)), as $\Phi_{aux}$ is increased, the tunneling width increases and the band-overlap decreases on the source side leading to a considerable reduction in the off-state tunneling probability. However, at higher $\Phi_{aux}$ (> 4.4 eV), band overlap begins to appear on the drain side and if the tunneling junction width on the drain side becomes small (as in the case of $\Phi_{aux} = 4.8$ eV), tunneling can occur in the off-state. In the on-state (Fig. 2(b)), the increase in $\Phi_{aux}$ does not change the band diagram significantly. The band overlap begins to decrease when $\Phi_{aux} > 4.4$ eV. Since the reduction in band overlap is over that section of the band-diagram where tunnel-width is already large, the tunneling probability is not affected significantly. Fig. 2(c) shows the change in the transfer characteristics as $\Phi_{aux}$ is increased from 4.0 - 4.8 eV. As expected, the $I_{OFF}$ (calculated at $V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V) reduces by more than 3 orders of magnitude when $\Phi_{aux} \geq 4.4$ eV. However, when $\Phi_{aux} \geq 4.8$ eV, greater tunneling occurs on the drain side increasing $I_{OFF}$ again. The $I_{ON}$ (calculated at $V_{GS} = V_{DS} = 1.0$ V) reduces by not more than 15% when $\Phi_{aux}$ is increased from 4.0 - 4.4 eV.

Next, we analyze the impact of the tunnel-gate work-function ($\Phi_{tunnel}$) on the characteristics of a DMG-DGTFET. Fig. 3(a) and 3(b) show the change in the band diagram of the device as $\Phi_{tunnel}$ is decreased, keeping $\Phi_{aux}$ fixed at 4.4 eV. In the off-state (Fig. 3(a)), there is no band-overlap on the source side, when $\Phi_{tunnel}$ is reduced to 4.0 eV, and hence the $I_{OFF}$ is expected to be quite low. In the on-state (Fig. 3(b)), with the reduction in $\Phi_{tunnel}$, the band-overlap increases and the tunneling width decreases, leading to a significant increase in the tunneling probability on the source side. Fig. 3(c) shows the change in the transfer characteristics of the DMG-DGTFET as $\Phi_{tunnel}$ is decreased from 4.8 - 4.0 eV. As expected, the $I_{ON}$ increases by around 4 orders of magnitude and the
VT (computed as VGS when the drain current reaches 1x10^-7 A/μm) reduces to 0.5 V at Φtunnel= 4.0 eV. The IOFF is below 1 fA/μm for all values of Φtunnel.

The above analysis shows that Φaux and Φtunnel can be adjusted for a better IOFF, ION and VT trade-offs. Since there is a large off-state tunneling when Φtunnel < 4.0 eV (on the source side) or Φaux > 4.8 eV (on the drain side), we have optimized Φaux and Φtunnel within 4.0 - 4.8 eV. Fig. 3(c) shows that when we decrease Φtunnel, the VT reduces and the ION increases. Since in general, DGTFET suffers from a low ION and high VT, it is desirable to adjust the device parameters to obtain a maximum ION and a minimum VT. Therefore, we choose Φtunnel to be the lowest possible value i.e. 4.0 eV. Fig. 2(c) shows that when we increase Φaux, the IOFF decreases. However, making Φaux > 4.4 eV reduces the ION without significantly improving the IOFF. Therefore, 4.4 eV is chosen as the optimal value for Φaux. There are several metal candidates that can be engineered to obtain the desired Φaux (4.4 eV) (e.g.: W, Ta, and Mo) and Φtunnel (4.0 eV) (e.g.: Mo, Ni-Ti and Sc) [28-30]. Next, we find an optimum value of the tunnel gate length (Ltunn), for the given Φaux, Φtunnel and L (50 nm). Fig. 4 shows that the IOFF decreases and the ION remains unchanged as Ltunn is decreased up to 20 nm. However, there is no significant impact on the IOFF below 20 nm. Therefore, we have chosen Ltunn = 20 nm.

The transfer characteristics in Fig. 5 show that the DMG-DGTFET has simultaneously a high ION and a low IOFF which cannot be achieved using an SMG-DGTFET. It may be noted that the ratio ION/IOFF in an SMG-DGTFET can be improved by adjusting Φm as demonstrated in ref. [10]. It is found that, at approximately Φm = 4.2 eV, the best possible value of ION/IOFF (around 3x10^9) is achieved in the given SMG-DGTFET. The ratio of ION/IOFF is in the range of 1x10^10 for a DMG-DGTFET. The improvement in the ratio of ION/IOFF in a DMG-DGTFET is, to some extent, a
consequence of the improvement in the average subthreshold slope ($SS_{AVG}$). The $SS_{AVG}$ is an important parameter for a TFET and is computed as:

$$SS_{AVG} = \frac{(V_T - V_{OFF})}{\log(I_{VT}) - \log(I_{VOFF})}$$

where $V_T$ is the threshold voltage, $V_{OFF}$ is the gate voltage from which the drain current starts to take off (as shown in Fig. 5), $I_{VT}$ is the drain current at $V_{GS} = V_T$ and $I_{VOFF}$ is the drain current of the device at $V_{GS} = V_{OFF}$ (as shown in Fig. 5) [5,31]. The $SS_{AVG}$ improves from 73 mV/decade in an SMG-DGTFET to 58 mV/decade in the DMG-DGTFET. It is worth mentioning that manipulation of the $\Phi_m$ in the SMG-DGTFET just shifts the transfer characteristics parallel to the X-axis and cannot improve the $SS_{AVG}$. However, in a DMG-DGTFET $\Phi_{aux}$ and $\Phi_{tunnel}$ provides an additional handle to manipulate different sections of the transfer characteristics, as shown using energy band-diagrams in Fig. 2 and Fig. 3, and thereby improve the $SS_{AVG}$. Fig. 6 shows the normalized output characteristics with respect to the drain current at $V_{DS} = 1$ V. The saturation voltage ($V_{DSAT}$) is computed as the $V_{DS}$ required to make $I_D$ reach 95% of the $I_D$ at $V_{DS} = 1$ V. For $V_{GS} = 0.7$ V, $V_{DSAT}$ reduces from 0.94 V for an SMG-DGTFET to 0.74 V for a DMG-DGTFET. The saturation voltage in a TFET corresponds to the disappearance of the inversion charge in the channel [16]. The electron concentration along a horizontal cutline close to the gate at different $V_{DS}$ is shown in Fig. 7. Since $\Phi_{aux} > \Phi_m$, the inversion charge density in the channel on the drain side is lower in the DMG-DGTFET compared to the SMG-DGTFET. Therefore, disappearance of the channel charge is facilitated in the DMG-DGTFET and a quicker onset of saturation is observed. It may be noted that a low $\Phi_m$ in a DGFET results in a delayed saturation in the output characteristics. However, increasing $\Phi_m$ would result in an undesirable decrease in $I_{ON}$ and an increase in $V_T$. In a DMG-DGTFET, a low $V_{DSAT}$ and a high $I_{ON}$ is attained
simultaneously by using a high $\Phi_{\text{aux}}$ and a low $\Phi_{\text{tunnel}}$. Hence, the DMG-DGTFET exploits the advantages of both the low and the high work function gate to attain an overall improvement in the device characteristics. Fig. 8(a) and Fig. 8(b) shows the transfer characteristics of the SMG-DGTFET ($\Phi_m = 4.2$ eV) and the DMG-DGTFET respectively. The difference in $V_{GS}$ at a constant drain current for the transfer characteristics of $V_{DS} = 1.0$ V and $V_{DS} = 0.1$ V (as shown in Fig. 8) is a manifestation of DIBL in a DGTFET [18]. The difference in $V_{GS}$ that is marked in Fig. 8 is found to be 0.215 V for the SMG-DGTFET and 0.131 V for the DMG-DGTFET. Therefore, the DMG-DGTFET is more immune against DIBL effects.

IV. DUAL MATERIAL GATE SDGFET

Though the results presented in the previous section show a significant improvement in the characteristics of a DGTFET due to the application of the DMG, the $I_{ON}$ of the DMG-DGTFET is around 10 $\mu$A/µm which is unacceptably low for the CMOS applications [20]. One of the most effective techniques to improve the $I_{ON}$ is to choose a lower band-gap material for the channel [10-14,20]. Therefore, we choose a s-SOI based SDTFET (Ge mole fraction $x = 0.2$) in this section and also make the following modifications to the device that was studied so far: a) HfO$_2$ ($k = 21$) with $t_{ox} = 2$ nm is used as the gate oxide to further boost the $I_{ON}$ [5] b) channel length $L$ is taken as 25 nm so that it is more realistic with the future applications. The detailed description of the impact of strain on the material properties and the simulation parameters of the silicon can be found in ref. [10,15]. It should also be noted that, as in the previous works [5,12,17,18,31], we have not considered the gate leakage through the thin HfO$_2$ gate oxide. Using the methodology outlined above for the DGTFET, the optimum device parameters for the $I_{ON}$, $I_{OFF}$, and $V_T$ trade-offs in a DMG-SDGFET are found to be:
Φ_{tunnel} = 4.3 \text{ eV}, \Phi_{aux} = 4.6 \text{ eV} and L_{tunn} = 12 \text{ nm}. The transfer characteristics obtained for SMG-SDGTFET and the DMG-DGTFET are shown in Fig. 9. The DMG-SDGTFET is able to deliver a high I_{ON} = 351 \mu A/\mu m, I_{OFF} < 1 \text{ fA/\mu m}, the ratio of I_{ON} / I_{OFF} is around 3 \times 10^{12} and V_T = 0.20 \text{ V}. The SS_{AVG} improves from 34 \text{ mV/decade in an SMG-SDGTFET} to 21 \text{ mV/decade in a DMG-SDGTFET}. The V_{DSAT} at V_{GS} = 0.7 \text{ V} reduces from 0.75 \text{ V} in the SMG-DGTFET (Φ_m = 4.3 \text{ eV}) to 0.65 \text{ V} in the DMG-DGTFET. The DIBL (computed as the difference in V_{GS} at I_D = 1 \text{ nA/\mu m for the transfer characteristics of V_{DS} = 0.1 \text{ V and V_{DS} = 1.0 \text{ V}}}) also improves from 86 \text{ mV in an SMG-SDGTFET (Φ_m = 4.6 \text{ eV})} to 43 \text{ mV in a DMG-SDGTFET}. The above results show that an excellent device characteristic is achieved in a DMG-SDGTFET.

Fig. 10 shows the change in V_T with L for an SMG-SDGTFET and a DMG-SDGTFET. For an SMG-SDGTFET there is no change in V_T up to around 20 nm. However, when L < 20 nm, the SMG-SDGTFET does show significant V_T roll-off [10,17]. A DMG-SDGTFET also shows no change in V_T up to 20 nm when the L_{tunn} is fixed to 12 nm. However, for L \leq 20 nm, L_{tunn} can be adjusted (L_{tunn} = 12 \text{ nm for L = 20 nm, } L_{tunn} = 10 \text{ nm for L = 15 nm} \text{ and } L_{tunn} = 7 \text{ nm for L = 10 nm}) to alleviate the problem of V_T roll-off as shown in Fig. 10. Therefore, DMG provides an additional handle to extend the scalability of the TFET. The I_{ON} of both an SMG-SDGTFET and a DMG-SDGTFET is not significantly affected by scaling.

Since Tunnel FETs are being actively investigated as enablers of future logic circuits operating with a V_{DD} < 0.5 \text{ V}, we analyze the suitability of the DMG-SDGTFET at V_{DD} = 0.5 \text{ V} [20]. Since low power applications impose a stricter requirement on the subthreshold swing, we choose an SDGTFET with higher Ge mole fraction (x = 0.5) [10]. The optimal device parameters for DMG-SDGTFET with x=0.5, V_{DD} = 0.5 \text{ V, L =}
25 nm and HfO\textsubscript{2} gate oxide with \(t_{ox} = 2\) nm are: \(\Phi_{\text{tunnel}} = 4.5\) eV, \(\Phi_{\text{aux}} = 4.7\) eV and \(L_{\text{tunn}} = 10\) nm. Fig. 11 shows the comparison of the transfer characteristics of the DMG-SDGTFET with SMG-SDGTFETs at \(V_{DS} = 0.5\) V. The important electrical parameters for the DMG-SDGTFET are: \(I_{ON} = 35\) \(\mu\)A/\(\mu\)m, \(I_{OFF} < 1\) fA/\(\mu\)m, ratio of \(I_{ON} / I_{OFF}\) is around \(3 \times 10^{11}\) and \(V_T = 0.16\) V. The \(SS_{AVG}\) improves from \(28\) mV/decade in the SMG-SDGTFET to \(16\) mV/decade in the DMG-SDGTFET. The \(V_{DSAT}\) at \(V_{GS} = 0.35\) V decreases from \(0.44\) V in the SMG-SDGTFET (\(\Phi_m = 4.5\) eV) to \(0.35\) V in the DMG-SDGTFET. The DIBL (computed as the difference in \(V_{GS}\) at \(I_D = 1\) nA/\(\mu\)m for the transfer characteristics of \(V_{DS} = 0.05\) V and \(V_{DS} = 0.5\) V) also improves from \(100\) mV in the SMG-SDGTFET (\(\Phi_m = 4.6\) eV) to \(62\) mV in the DMG-SDGTFET. The excellent \(SS_{AVG}\) of the DMG-SDGTFET shows that it can be one of the suitable candidates for future low power CMOS applications. However, the \(I_{ON}\) at \(V_{DD} = 0.5\) V may be required to be enhanced further.

V. CONCLUSIONS

In this work, we have studied the implications of the application of a dual material gate in a TFET to simultaneously improve the overall performance of the device. We have demonstrated that the technique of using DMG can be applied in a DGTFET to obtain a good \(I_{ON}, I_{OFF}\) and \(V_T\) tradeoffs along with an improvement in the \(SS_{AVG}\), improve the nature of the output characteristics and increase the immunity against the DIBL effects. We have also shown that DMG provides a technique to exploit the advantages of both a high and a low work-function gate in a TFET and thereby obviate the problems of both these types of gates. The improvement in device characteristics obtained using a DMG in an SDGTFET further demonstrate that the technique of DMG is capable of improving the overall device characteristics in the TFETs that are: a) using smaller band-gap channel
material like sSOI b) based on high-k gate dielectric (HfO<sub>2</sub>) c) having smaller t<sub>ox</sub>=2 nm d) having smaller channel length L=25 nm e) driven by lower V<sub>DD</sub>=0.5 V. It is worth mentioning that using a DMG in a TFET will bring further complexity to the device fabrication. Also, fabricating a DMG at a very small device dimension (channel length less than 100 nm) and extending it to below 10 nm may be challenging. However, since there is an appreciable improvement in the overall device characteristics, the complexity in the device fabrication might be acceptable and further fabrication-driven experiments on DMG at smaller dimensions are worth exploring.

Acknowledgment: This work was supported in part by the NXP (Philips) Chair Professorship awarded to M. Jagadesh Kumar.
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Fig. 1
Fig. 2
Fig. 3
Fig. 4

Fig. 5
Fig. 6
Fig. 7

Electron concentration (cm\(^{-3}\))

- Drain
- Channel
- Source

$V_{DS}$ (V):
- 0.0
- 0.6
- 0.8
- 1.0

Position along X-axis (µm)

(a)

(b)
Fig. 8

(a) Drain Current (A/µm) vs. Gate Voltage (V)

- $V_{DS} = 1.0$ V
- $V_{DS} = 0.1$ V

(b) Drain Current (A/µm) vs. Gate Voltage (V)

- $V_{DS} = 1.0$ V
- $V_{DS} = 0.1$ V

DIBL (SMG)
DIBL (DMG)
Fig. 9

Fig. 10
Fig. 11
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