Evaluating Digital Sine wave Generator Using Analog Metrics

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Abstract—This work aims to relate comparison metrics for both Direct Digital Synthesizers (DDS) and their analog counterparts. The proposed metrics are Total Harmonic Distortion (THD) and maximum absolute error. Error is theoretically formulated into closed forms for known systematic parameters of DDS, sample rate, and bit counts. By the use of Matlab scripting, the system model is simulated for a wide range of parameters sweep.

Keywords—DDS,THD,error,sine,comparison

I. INTRODUCTION

With the rapid growth of digital systems and taking up a major portion of electronics and computer technology, some analog systems are being replaced by their digital counterparts. Analog circuits are being developed for more configurability[1] and the future of Field Programmable Analog Arrays (FPAA) is promising. So in very low power and high speed with limited accuracy applications[2], [3], digital systems substitution should be done with care. Applications with heavy computation load[4] or low output speed with no concern about consuming power are high priority nominees for substitution e.g. controllers[5] and biomedical devices[6].

It is very interesting to have common evaluating merits between digital and analog systems. Two parameters of this kind are Total Harmonic Distortion (THD) and error which is describing the difference between a target or reference signal and produced output in frequency and time domain[7]–[9].

Direct Digital Synthesizers (DDS) usually have a Low Pass Filter (LPF) to suppress very high-frequency components in the produced output signal[10]. There is the same block in analog signal generators to remain most of the signal energy in the desired frequency range. Because of the sameness in this stage between analog and digital synthesizers and added complexity for theoretical analyzing, systems mentioned here have no LPF at their output stages. This leads to more simplification and specialized analytical study. Also, the internal structure of DDS is not mentioned and it is just mentioned as a black computational box with a known Digital-to-Analog Converter (DAC) at the output node.

In the most basic form, the monotonic pure sine wave with fixed amplitude, phase, and frequency is chosen as the target output signal.

Section II will introduce the target signal in a closed formed and try to formulate the output of the DDS in three different conditions. By use of achieved formulas, their distance from the target signal is calculated and theoretically analyzed. In section III simulation results for different value of the system, parameters are presented and their accordance with the theoretical analysis described.

II. METHOD

The ideal expected output signal from DDS and its analog counterpart is a pure sine wave called target expressed in (1) with unity amplitude, real frequency, and zero phase:

\[ f_0(t) = \sin(2\pi f \cdot t) \] (1)

In (1) \( f \) and \( t \) represent the frequency and time in Hertz and Seconds respectively. Error and harmonics distortion of other synthesized signals are calculated in comparison with the amplitude and Fourier analysis of the target function.

A. Quantization (domain discretization) effect

The limited number of amplitude levels in digital-to-analog conversion is usually mentioned as quantization of amplitude. The values between these available levels are transferred to the nearest level. Choosing the nearest available level for a value could be performed at least in 3 different manners with floor, round, or ceiling functions they are formulated in (2), (3), and (4).

\[ f_0,\text{floor}(t, B) = \left\lfloor \sin(2\pi f t) \times 2^{B-1} \right\rfloor / 2^{B-1} \] (2)
\[ f_0,\text{round}(t, B) = \left\lfloor \sin(2\pi f t) \times 2^{B-1} + 0.5 \right\rfloor / 2^{B-1} \] (3)
\[ f_0,\text{ceiling}(t, B) = \left\lceil \sin(2\pi f t) \times 2^{B-1} \right\rceil / 2^{B-1} \] (4)

Where \( B \) is the number of input bits provided by the Digital to analog converter. Consequently, the maximum value of the absolute error is just under (5) which is inversely proportional to the number of bits.

\[ |f_0 - f_0| < \frac{1}{2^{B+1}} \] (5)

Since the total number of available analog amplitude levels in a DAC is \( 2^{\text{No.\,Bits}} \), for sine wave with both positive and negative domain, full-scale range (F.S.R.) is exactly 2 as calculated in (6) but the error in percent is usually intended by a division of peak absolute error by one.

\[ \text{F.S.R.} = \sin \left( \frac{n}{2} \right) - \sin \left( -\frac{n}{2} \right) \] (6)

B. Time discretizing (Sampling) effect

The discretization of the time factor in the digital synthesizer circuit is theoretically modeled (7) by use of floor function and including the effect of the time gap between producing of new values at the output node. The time gap \( \Delta t \) is mentioned to be constant for each output to become ready.

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\[ f_c = \sin \left(2\pi f \times \left| \frac{1}{\Delta t} \times \Delta t \right| \right) \]  

(7)

The function \( f_c \) has modeled a DAC with no loss of precision because of the limited number of available levels in output. With a given time gap, the clock pulse frequency of the digital synthesizer cannot be less than \( f_{CLK} \) \( (8) \).

\[ f_{CLK} = \frac{1}{\Delta t} \]

(8)

The absolute maximum error of the \( f_c \) is difficult to be calculated into a closed-form because it has fractures for every \( \Delta t \). since \( f_c \) is not completely continuous, it is not fully differentiable at all its domain. To find the maximum of its absolute error, a dominant function is used. The only difference between \( f_c \) and \( f_0 \) is their time variable. The most distance between these time variables occurs just before the endpoint of each \( \Delta t \) time gap. Now by use of \( (9) \):

\[ t - \Delta t \leq \left| \frac{1}{\Delta t} \right| \Delta t \leq t \]  

(9)

The farthest distance is less than \( (10) \):

\[ ||f_c - f_0|| < |\sin 2\pi f t - \sin 2\pi f (t - \Delta t)| \leq 2 \]  

(10)

Extremums of inequality \((10)\) happens just before balance points of inequality \( (9) \), \( t=\Delta t \), which led to \((11)\):

\[ ||f_c - f_0|| < |\sin 2\pi f K\Delta t - \sin 2\pi f (K - 1)\Delta t| \]  

(11)

Alternative form of \((11)\) expressed in \((12)\) where \( \omega \) is the constant factor \( 2\pi f K \):  

\[ ||f_c - f_0|| < |\sin(\omega \Delta t) - \sin \left( \omega \Delta t - \frac{\omega}{K} \Delta t \right)| \]  

(12)

\( \Delta t \) in \((12)\) inserts a phase shift while the peak distance between two sine functions is just related to that. The greatest phase shift is calculated in \((13)\) with taking \( K=1 \):

\[ \phi_{max} = 2\pi f \Delta t \]  

(13)

For very large values of time gap when \( 2f, \Delta t=1 \), the phase difference becomes \( 180^\circ \) and absolute error can reach up to 2. This happens when \( \Delta t \) is half the target sine wave period. For small enough values of \( \Delta t \), peak error can be estimated to \((14)\) which is in direct proportion with the time gap:

\[ error_{max} < \sin 2\pi f \Delta t \quad \text{when: } \Delta t \ll \frac{1}{f} \]  

(14)

C. Digitizing effect

A real digital synthesizer has neither an infinite number of output levels nor infinite clock frequency. In other words, a limited number of output levels and the existence of a stop time gap between output changes led to fractures in output on the time and domain axis. Including both discretization effects is necessary for investigating more practical conditions that are formulated in \((15)\).

\[ f_D(t, \Delta t, B) = \frac{\sin(2\pi f \left| \frac{1}{\Delta t} \times \Delta t \right|) \times 2^{B-1}}{2^{B-1}} \]  

(15)

With the same manner for \((5)\) and \((14)\), the maximum error is limited to \((16)\):

\[ |f_D - f_0| \leq \frac{1+2^{B-1}\sin(2\pi f \Delta t)}{2^{B-1}} \]  

(16)

III. SIMULATION RESULTS

A. Domain quantized

In a very fast system with high enough clock pulse speed and a negligible time gap for updating output value, signal specifications can be estimated by just mentioning the quantization effect on domain value. The results of the theoretical analysis for the quantization effect with a different number of bits are plotted in fig. 1 and fig. 2.

Fig. 1. Maximum absolute error in percent for some usual bit counts in logarithmic scale.

Fig. 2. THD in negative decibel scale vs. number of bits.

Both error percent and total harmonic distortion (THD) diminish rapidly in a logarithmic manner by adding each extra single bit. Results for only more usual bit counts are depicted for better obviousness.

B. Time discretized

As the bits number of a digital synthesizer approaches infinity, its domain levels get much closed and lose its negative effects on signal specifications. So the only dominant limitation remained is discontinuity in the time domain. The
effect of this circumstance is investigated and sketched in fig. 3 and fig. 4.

The parameter on the horizontal axis is frequency multiplier which is the ratio of the Sine wave period to the time gap between output updates. Frequency multiplier expresses how many times the digital synthesizer is faster than its target sine wave.

![Fig. 3. Maximum absolute error in a linear scale on the vertical axis vs. a logarithmic range of frequency multiplier](image3)

![Fig. 4. Harmonic distortion is scaled in negative decibel for 30 values of frequency multiplier in each decade.](image4)

As is expected from (14), speeding up the system by making the time gaps smaller, slightly decreases the error and harmonic distortion. Notice that the horizontal axis depicted in the logarithmic scale to include larger speed-up ratios and so on the relation between THD and frequency multiplier is almost linear but for error, results are somewhat better. It is because has a reciprocal ratio of time gap $\Delta t$.

C. Digitized signal

In most real conditions, none of the domain quantization or time discontinuity are negligible and affect the specifications of the output simultaneously. To investigate their effect on the error and harmonic distortion, both parameters are swept and the result for each simulation depicted with colored contours of fig. 5 and fig. 6.

![Fig. 5. The color range of yellow to blue represents the maximum absolute error of one 100 percent to zero.](image5)

![Fig. 6. lighter points show produced signal with more distorted harmonic components energy](image6)

From colored contours of fig. 5 and 6 it is obvious that for fewer bit counts, frequency multiplier is more affective and vice versa.

IV. CONCLUSION

To compare an analog signal generator and its digital counterpart, the common specifications are error and harmonic distortion. This work related these properties to bits number and clock pulse speed of a general direct digital synthesizer. For future works it is recommended to investigate digital synthesizing algorithms and error metrics for a comprehensive comparison. Theoretical analysis of relation between harmonic distortion and the parameters of the digital synthesizer is absent here and needs to be explored.

REFERENCES

[1] S. Nikseresht and S. J. Azhari, “A new current-mode computational analog block free from the body-effect,” Integration, vol. 65, pp. 18–31, Mar. 2019, doi: 10.1016/j.vlsi.2018.10.008.

[2] B. J. Hosticka, “Applications of Mixed Analog/Digital Design,” in ESSCIRC ’92: Eighteenth European Solid-State Circuits conference, Sep. 1992, pp. 27–34, doi: 10.1109/ESSCIRC.1992.5468470.
[3] H. Jafari, Z. Abbasi, and S. J. Azhari, “An Offset-free High linear Low Power High Speed Four-Quadrant MTL Multiplier,” Ital. J. Sci. Eng., vol. 1, no. 3, Nov. 2017, doi: 10.28991/jise-01115.

[4] M. Mollajafari and H. S. Shahhoseini, “An efficient ACO-based algorithm for scheduling tasks onto dynamically reconfigurable hardware using TSP-likened construction graph,” Appl. Intell., vol. 45, no. 3, pp. 695–712, Oct. 2016, doi: 10.1007/s10489-016-0782-2.

[5] S. M. Mohtavipour, H. Jafari, and H. S. Shahhoseini, “A novel design for adaptive cruise control based on extended reference model,” in 2017 IEEE 4th International Conference on Knowledge-Based Engineering and Innovation (KBEI), Dec. 2017, pp. 0822–0827, doi: 10.1109/KBEI.2017.8324910.

[6] H. Jafari, M. B. Heydari, N. Jafari, and H. Mirhosseini, “Design and Fabrication of Novel Digital Transcranial Electrical Stimulator for Medical and Psychiatry Applications,” ArXiv200904411 Cs Eess, Sep. 2020, Accessed: Nov. 07, 2020. [Online]. Available: http://arxiv.org/abs/2009.04411.

[7] B. J. Hosticka, “Performance comparison of analog and digital circuits,” Proc. IEEE, vol. 73, no. 1, pp. 25–29, Jan. 1985, doi: 10.1109/PROC.1985.13107.

[8] B. Razavi, Principles of Data Conversion System Design. IEEE, 1994.

[9] A. Fürtig et al., “Novel metrics for Analog Mixed-Signal coverage,” in 2017 IEEE 20th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS), Apr. 2017, pp. 97–102, doi: 10.1109/DDECS.2017.7934589.

[10] P. Mitra, Recent Trends in Communication Networks. 2020.