Integrated fuzzy-PI controlled current source converter based D-STATCOM

M. Deben Singh¹*, Ram Krishna Mehta¹ and Arvind Kumar Singh¹

Abstract: The distribution static synchronous compensator (D-STATCOM) is a shunt-connected current injection custom power (CP) device that can be used for improving quality and reliability of the power supplied to electric consumers under dynamic conditions of the distribution system. The CP devices such as dynamic voltage restorer and unified power quality conditioner including D-STATCOM are mostly designed and implemented using voltage source converter topology. The performance of D-STATCOM can be improved, if it is realized by using a current source converter topology which can generate a controllable current directly at its output terminals. Although the current source converter (CSC) topology offers many promising advantageous features, not much research publications with CSC-based approach in the field of CP devices has been reported over the last one decade. This paper presents a novel method of realizing a D-STATCOM using CSC topology with an integrated fuzzy-PI controller for not only mitigating voltage sag but also capable of maintaining improved DC-link voltage profile. The model has been simulated in the MATLAB/SIMULINK environment. The simulation results under steady state and dynamic load perturbation provide excellent output characteristics that support the validity of the proposed model.

ABOUT THE AUTHORS

M. Deben Singh received his BTech degree in Electrical Engineering from the North Eastern Regional Institute of Science & Technology (NERIST), Arunachal Pradesh, India, in 1997 and M Tech degree in Electronics Design & Technology from Tezpur University, Assam, in 2001. Mr. Singh is a member of IEEE, USA. His area of research interest is in Power Electronics Applications. He is presently working as an assistant professor in the Department of Electrical Engineering, NERIST.

Ram Krishna Mehta obtained his PhD degree from Jadavpur University, Kolkata in 2008. His research interests are Flight and Power system control. He is presently working as an associate professor in the Department of Electrical Engineering, NERIST.

Arvind Kumar Singh received his PhD degree in 2006 from Tezpur University, Assam, India. His research areas are power system, machines and drives. He is presently working as an associate professor in the Department of Electrical Engineering, NERIST.

PUBLIC INTEREST STATEMENT

This paper presents a novel method of realizing a D-STATCOM using current source converter topology with an integrated fuzzy PI controller for not only mitigating voltage sag but also capable of maintaining improved DC-link voltage profile which is a great challenge where an inductor is used as an energy storage element instead of a pre-charged capacitor as in the case of VSC. The use of CSC topology in the custom power applications which has not been the focus of many researchers for a long time due to various reasons is explored through this paper. The model has been simulated in the MATLAB/SIMULINK. The simulation results under steady state and dynamic load perturbation provide excellent output characteristics that support the validity of the proposed model. This paper will pave the way for initiating the application of CSC topology in other types of custom power devices so as to enhance power quality in the future.
1. Introduction

Modern electric power system networks are highly interconnected and the performances of the most of the loads connected to such systems are very much sensitive to the power quality. The application of power electronics technology in power transmission and distribution system has led to the design and implementation of new engineering systems, viz. flexible AC transmission system (FACTS) devices and custom power (CP) devices, which are capable of solving various types of power quality problems (Acha, Agelidis, Anaya-Lara, & Miller, 2006; Hingorani, 1995; Hingorani, & Gyugyi, 2013). The FACTS devices are aimed at the transmission level, whereas CP devices are meant for use at the distribution level, particularly at the point of connection of the electricity distribution system for the consumers having sensitive loads (Deben & Khumanleima, 2015; Lipi & Deben, 2013). The quality of electrical power which is supplied to the customers can be judged in terms of constant voltage magnitude, i.e. no voltage sags or swell, constant frequency, constant power factor, balanced phases and sinusoidal waveform, i.e. no harmonic content, lack of interruptions and capability to withstand faults and to recover quickly (Deben & Khumanleima, 2015). The voltage source converters (VSC) topology has been using as the basic building block of the new generation of power electronics controllers emerging from FACTS and CP initiatives due to the fact that current source converter (CSC) topology is more complex than a VSC topology in both power and control circuits. The filter capacitors which are connected at the AC side of CSC improve the quality of the output AC current waveforms but increase the overall cost of the converter. These filter capacitors resonate with the AC-side inductances. As a result, some of the harmonic components present in the output current might be amplified, thereby causing high harmonic distortion in the AC-side current (Singh, Mehta, & Singh, 2015). If power switching devices having sufficient reverse voltage withstanding capability such as Gate-Turn-Off Thyristor (GTO) are not used, a diode has to be placed in series with each of the switches in CSC. This almost doubles the conduction losses compared with the case of VSC. The DC-side energy storage element in CSC topology is an inductor, whereas that in VSC topology is a capacitor. The power loss of an inductor is expected to be larger than that of a capacitor because of the need to store energy by circulating current in inductors which are more lossy than capacitive energy storage (Ghosh & Ledwich, 2009). Thus, the efficiency of a CSC is expected to be lower than that of a VSC (Ye, Kazerani, & Quintana, 2005). The advancement made in the field of power semiconductor switching devices recently along with the emergence of new control strategies of CSC topology may overcome the demerits cited above in the near future. The CSC topology is usually more reliable and fault tolerant than a VSC due to the presence of large series inductor which limits the rate of rise of current in the event of a fault (Ghosh & Ledwich, 2009). The presence of the AC-side capacitors provides good sinusoidal voltage and current waveforms at the output terminals when CSC topology is used as the capacitors are the inherent filter for the CSC. The problem of the resonance between the capacitances and inductances on the AC-side can be overcome by careful design of the capacitor-based filter circuit and introduction of sufficient damping using proper control methods (Ye et al., 2005). Furthermore, all the switching problems faced in the early stages of CSC development can be overcome by employing tri-level switching scheme which has become a standard technique in the control of CSC (Wang, 1993). In high-power applications such as FACTS devices, Integrated Gate Commutated Thyristor which has the optimum combination of the characteristics, viz. high ratings, high reverse voltage blocking capability, low snubber requirements, lower gate-drive power requirements than GTO and higher switching speed than GTO, can be used (Steimer et al., 1999). The DC-side losses are expected to be minimized using superconductive materials in the construction of the DC-side reactor (Ye et al., 2005).

In comparison with the VSC topology, the application of CSC topology in distribution static synchronous compensator (D-STATCOM) is expected to achieve many advantages. The direct output of
a CSC is a controllable AC current, whereas that of a VSC is a controllable AC voltage. When operated under sinusoidal pulse width modulation (SPWM) technique (Mohan, Undeland, & Robbins, 1989), the magnitudes of the harmonic components in both converters are directly proportional to the magnitudes of the fundamental components of their direct output quantities. Under the normal operating conditions, the current injected by D-STATCOM is a small percentage of the line current. Hence, when CSC topology is used, the current harmonics are also small. However, when VSC topology is used, for a small injected current, the output voltage of VSC is large and very close to the system voltage. This results in large voltage harmonics, leading to current harmonics that are larger than those generated by CSC, and thus more costly to filter. The other aspect of comparison is the DC-side energy storage requirement. When the D-STATCOM is realized by a CSC, the DC-side current is just larger than the peak value of the required injected current which is a small percentage of the line current. However, when a VSC is used to inject reactive power to the system, the DC-side voltage must be larger than the peak value of the system line-to-line voltage so that the reactive power can be exchanged between the D-STATCOM and the AC distribution system. Hence, the DC energy storage requirement of the CSC topology is expected to be lower than that of the VSC topology when it is used to implement a D-STATCOM system for mitigation of voltage sag (Singh et al., 2015).

The D-STATCOM has plenty of applications in low voltage power distribution systems. It can be used to prevent non-linear loads from polluting the rest of the distribution system. The rapid response of the D-STATCOM makes it possible to provide continuous and dynamic control of the power supply, including voltage and reactive power compensation, mitigation of voltage sag, swell and elimination of harmonics (Acha et al., 2006). A thorough investigation on the feasibility and performance analysis of a CSC-based D-STATCOM for mitigating voltage sag phenomenon which is considered to be one of the well-known unwanted power quality problem resulted from sudden change in load connected to a power distribution system has been fairly reported at (Singh et al., 2015); however, the paper has not discussed about the challenge of maintaining the DC-link voltage profile during the voltage sag compensation period. The magnitude of output voltage of the inverter circuits used in the FACTS and CP devices is directly proportional to the DC-link voltage. Hence, maintenance of this voltage to a fair level is an important and challenging aspect at the time of designing a CSC-based CP device because an inductor is used as energy storage element instead of a pre-charged capacitor as in the case of VSC. By incorporating fuzzy logic controller (FLC) in the control system of the proposed D-STATCOM, an attempt has also been made to maintain the improved DC-link voltage profile during the process of voltage sag mitigation. The simulation results of the proposed model reveal its effectiveness in mitigating voltage sag while maintaining improved DC-link voltage.

2. Power reliability and quality issues

The main concern of electrical energy consumers was the reliability of power supply a few years back. This reliability can be defined as the continuity of electric supply (Ghosh & Ledwich, 2009). Power quality is mainly concerned with deviations of the voltage from its ideal waveform (voltage quality) and deviations of the current from its ideal waveform (current quality). Such deviation is known as “power quality phenomenon” or “power quality disturbance” (Math & Bollen, 2013). Some examples of the power quality problem include impulsive and oscillatory transients, short duration voltage variations (sag or dip, swell and interruption), long duration voltage variation (undervoltage, overvoltage and sustained oscillation), voltage imbalance, waveform distortion (harmonics, notching and DC offset) and voltage flicker. These problems are generally caused by the nature, faults on transmission or distribution system and also by the power consumers. The power transmission lines are exposed to the forces of nature and its loadability limit is usually determined by either stability considerations or by thermal limits. Although the power quality problem is a distribution side problem, transmission lines frequently have an impact on the quality of power supplied. It is however to be noted that while most of the problems associated with transmission systems arise due to the forces of nature or due to the interconnection of power systems, individual customers are responsible for a more substantial fraction of the power quality problems in the distribution side (Ghosh & Ledwich, 2009). The FACTS and the CP devices are the two major power electronics-based initiatives to counter the power quality problems. CP focuses primarily on the reliability and power quality.
However, voltage regulation, voltage balancing and harmonic cancellation may also benefit from this technology (Deben & Khumanleima, 2015).

Amongst the various power quality problems mentioned above, this paper confines itself to the voltage sag only. The voltage sag is a power quality problem phenomenon which falls under the category of short duration voltage variation. Any variation in the supply voltage (rms) for duration not exceeding one minute is called a short duration voltage variation. Usually, such variations are caused by system faults, energization of heavy loads that require large inrush currents and intermittent loose connection in the power wiring. Voltage sag is a fundamental frequency decrease in the supply voltage for a short duration. The duration of voltage sag varies between five cycles to a minute (Ghosh & Ledwich, 2009). The interest in voltage sag is mainly due to the problems they cause on several types of equipment, viz. adjustable speed drives, process control equipment and computers, which are notorious for their sensitivity. Some pieces of equipment trip when the rms voltage drops below 90% for longer than one or two cycles. If this is the process control equipment of a paper mill, one can imagine that the damage due to voltage sags can be enormous. Of course, voltage sag is not as damaging to industry as a (long or short) interruption. But as there are far more voltage sags than interruptions, the total damage due to voltage sags is still larger. Short interruptions and most long interruptions originate in the local distribution network. However, voltage sags at equipment terminals can be due to short circuit faults 100s of kilometres away in the transmission system. Hence, voltage sag is much more of a “global” problem than an interruption. Reducing the number of interruptions typically requires improvements on one feeder and reducing the number of voltage sags requires improvements on several feeders and often even at transmission lines far away (Math & Bollen, 2013). The voltage sag occurring at the power distribution system can be mitigated using VSC-based CP devices such as dynamic voltage restorer (DVR) and D-STATCOM (Deepa & Ranjani, 2015; Singh et al., 2015).

2.1. VSC- and CSC-based D-STATCOM

When STATCOM is used in the low voltage distribution system, it is identified as D-STATCOM. Although both the STATCOM and the D-STATCOM are shunt-connected devices, there is a substantial difference in their operating characteristics. The STATCOM is required to inject a set of three balanced quasi-sinusoidal voltages that are phase displaced by 120°, but the D-STATCOM must be able to inject an unbalanced and harmonically distorted current to eliminate unbalance or distortions in the load current or the supply voltage. Hence, its control is significantly different from that of a STATCOM. In case of VSC-based D-STATCOM, it can be configured using a voltage source inverter circuit interfaced with a coupling transformer and energy storage element, viz. capacitor (Singh et al., 2015). The D-STATCOM used in CP applications uses PWM switching control as opposed to the fundamental frequency switching strategies which are preferably used in FACTS applications. PWM switching is practically used in CP applications as it is at relatively low power level (Acha et al., 2006; Deben & Khumanleima, 2015; Ghosh & Ledwich, 2009). The CSC-based D-STATCOM can be realized by modifying the basic configuration of the VSC-based one. It also consists of a CSC circuit which is interfaced with a coupling transformer and a DC-link reactor/inductor as shown in Figure 1.

3. CSC-based D-STATCOM

The proposed CSC-based D-STATCOM consists a three-leg CSC driven by SPWM, AC-side low pass filters (LPF), coupling transformer and internal control system. The simplified structure of the proposed model is depicted in Figure 2. The working principle and control of CSC for use in D-STATCOM are similar to those of the CSC employed in AC motor drives, but its design strategy is different to some extent. The CSC circuit will be subjected to voltage regulation problem on the AC side when the reactive power is varied from full inductive to full capacitive. This will affect the voltage rating of the switching devices as well as the design of the input LPF circuit (Singh et al., 2015).

As the DC-link circuit consists only inductor and its internal resistance, the electrical time constant will be high and thus affects the design process of this circuit. The design objectives of the CSC for use in D-STATCOM are not only to filter harmonics but also to achieve optimal sizing of the CSC so as
to meet the control range requirements of the D-STATCOM in both the capacitive and inductive operation ranges (Bilgin & Ermis, 2010). The selection of switching device and modulation scheme depends on the application voltage and power ratings (Han, Moon, & Karady, 2000). At distribution-level applications, viz. D-STATCOM, IGBT switches and PWM scheme can be chosen if VSC topology is used. The converter topology for the proposed model being CSC, GTO switches having sufficient reverse voltage withstanding capability are selected. These switches are configured in bridge fashion and fed from a DC-link reactor acting as the energy storage element. The DC-link reactor approximates the DC-link current $I_{dc}$ to a level current waveform in the steady state. The level DC-link current is converted to bidirectional current pulses, alternating at supply frequency in the AC lines of CSC by switching power semiconductor switches in accordance with a pre-specified pattern (Bilgin & Ermis, 2011; Bilgin et al., 2007). In the CSC circuit, the energy storage element is an inductor with its internal resistance. The amount of reactive power to be generated by the CSC can be computed from the relation:

$$Q = \sqrt{3/2}VM_{dc}C\cos \theta$$  

where $V$ = rms value of the fundamental component of converter input line-to-line voltage, $M =$ modulation index, $I_{dc} =$ mean DC-link current and $\theta =$ phase shift (Bilgin & Ermis, 2010). Equation (1) indicates that $Q$ is independent of the DC-link inductance $L_{dc}$. The value of $L_{dc}$ affects the response time of D-STATCOM against the variations of reactive power demand of the load. The time constant of the DC-link circuit $\tau_{dc}$ is $L_{dc}/R_{dc}$. Hence, the value of $L_{dc}$ should be selected as small as possible for allowing rapid rise or decay of mean DC-link current against the rapid changes in $Q$ if the phase shift angle control at fixed modulation index is used for controlling the reactive power. The output of the CSC is filtered by a three-phase LPF comprising of three capacitors connected in shunt manner. These filters ensure to provide good sinusoidal output voltage and current waveforms after separating higher order harmonic components to the coupling transformer. The leakage impedance of the coupling transformer also behaves as a part of the LPF. External series reactors (i.e. $X_t$ in Figure 2) have been used on the low voltage side of the coupling transformer for adjusting the corner frequency of the input filter to an optimum value for the fixed shunt-connected capacitor in implementing the proposed D-STATCOM. The corner frequency should be chosen as small as possible for better performance of the filter circuit. The detailed design strategies of the LPF are available at (Bilgin & Ermis, 2011).

### 3.1. Control system of the model

The control system of the proposed D-STATCOM consists a phase lock loop (PLL), proportional integral (PI) controller, FLC and $dq0$ transformation block, etc. For the sake of convenience in designing the control system, the internal control structure has been divided into two sections, viz.
conventional controller section and FLC section, which will be integrated and converted into a single controller to produce the optimum performance.

3.1.1. Conventional controller section

The task of sensing the voltage sag, calculating the required compensating voltage for the D-STATCOM and generating the reference signals for the SPWM generator to provide switching pulses for the GTO switches used in the CSC are carried out by the internal control system. For generating proper gating signals of the GTO switches used in the CSC, SPWM control scheme is chosen for the proposed model. The SPWM switching strategy has constant switching frequency capability. This constant switching frequency reduces stress levels on the converter switches (Nagesh, Srinivas, & Mahesh, 2012). The control scheme will be able to maintain constant voltage magnitude at the point where a sensitive load is connected under system disturbances. The control system only measures the rms voltage at the point of common coupling (PCC) and no reactive power measurements are carried out. The CSC switching strategy is based on a sinusoidal PWM technique which offers simplicity and good response. As the distribution network operates at a relatively low power, such method offers a more flexible option than the fundamental frequency switching method which is favoured in FACTS applications. The block diagram of the control scheme designed for the proposed model is shown in Figure 3. The commonly used control schemes for the generation of reference source currents in most of the VSC-based DSTATCOM include instantaneous reactive power theory, synchronous reference frame theory (SRFT), unity power factor based, instantaneous symmetrical components based, etc. (Bhim, Jayaprakash, & Kothari, 2008). The control scheme chosen for the proposed D-STATCOM model is based on SRFT. The load currents, $I_{\text{Load}} (i_a, i_b, \text{and } i_c)$, the PCC voltage $V_{\text{PCC}} (v_a, v_b, \text{and } v_c)$ and the reactor DC voltage ($V_{\text{dc}}$) of D-STATCOM are sensed and used as feedback signals. The load currents from the $a$–$b$–$c$ frame are first converted to the $\alpha$–$\beta$–$0$ frame and then to $d$–$q$–$0$ frame using the Park’s transformation relation as:

$$i_d = \frac{2}{3} [i_a \sin \theta + i_b \sin(\theta - 2\pi/3) + i_c \sin(\theta + 2\pi/3)]$$

(2)

$$i_q = \frac{2}{3} [i_a \cos \theta + i_b \cos(\theta - 2\pi/3) + i_c \cos(\theta + 2\pi/3)]$$

(3)

$$i_0 = \frac{1}{3} [i_a + i_b + i_c]$$

(4)

where $\cos \theta$ and $\sin \theta$ are obtained using the three-phase PLL. The PLL receives signal from PCC terminal voltage $V_{\text{PCC}}$ for generation of fundamental unit vectors for conversion of sensed currents to the $d$–$q$–$0$ reference frame. The SRF controller extracts DC quantities by a LPF and removes the harmonics from the reference signal. The distribution feeder terminal voltage $V_{\text{PCC}}$ is regulated by a PI controller after comparing $V_{\text{PCC}}$ with a reference terminal voltage $V_{\text{ref}}$, which produces a $i_q$ signal and adds with $i_q$ generated at equation (3) and acts as a reference component for the current.
controller. The error signal output after comparing DC-link reactor voltage $V_{dc}$ with $V_{dc}(ref.)$ is processed by another PI controller to regulate the DC-link voltage and produces $i_d$ current component. This current is added with the $i_d$ available at equation (1). The reference source current must be in phase with the voltage at the PCC but with no zero-sequence component and it can be obtained using reverse Park’s transformation process (Bhim et al., 2008). The sensed current and reference source currents are compared and a proportional controller is used for amplifying current error in each phase in the current controller (Singh et al., 2015).

3.1.2. FLC section
The conventional PI controllers find applications in industries for a wide range of control processes and provide satisfactory performance once tuned when the process parameters are well known and there is not much variation. However, if operating conditions vary, further tuning may be necessary for good performance. Since most of the control processes are complicated and non-linear, FLC approach seems to be a good choice. The FLC has been widely used in systems with complex structure as it doesn’t require mathematical model of the control system (Resul, Besir, & Fikret, 2011). The design structure of the FLC can be visualized as shown in Figure 4.

There are four main components in a FLC, viz. Fuzzification unit (the Fuzzifier), Inference engine, Rule base and Defuzzifier. The first stage in the fuzzy controller system is to transform the numeric into fuzzy sets. This operation is called fuzzification. From the point of view of fuzzy set theory, the inference engine is the heart of the fuzzy system. It is the inference engine that performs all logical
manipulations in a fuzzy system. A fuzzy system Rule base consists of fuzzy IF–THEN rules and membership functions characterizing the fuzzy sets. The result of the Inference process is an output represented by a fuzzy set, but the output of the fuzzy system should be a numeric value. The transformation of a fuzzy set into a numeric value is called defuzzification. In addition, input and output scaling factors are needed to modify the universe of discourse. Their role is to tune the fuzzy controller to obtain the desired dynamic properties of the process controller closed loop (Jan, 1998).

In the proposed integrated fuzzy PI controller, two numbers of FLC blocks are used for the error signal-d and error signal-q. Each controller has two inputs and one output. One of the input to the FLCs is the derivative of the processed output of the PI controllers and the abc to dq0 transformation blocks used in the model as depicted at Figure 5. In other words, the inputs of FLC are the errors of d- and q-axis currents and derivatives of these errors. An external integrator is used to eliminate the steady-state error in the output of FLC (Resul et al., 2011). The inputs of the FLC have been chosen as the error in DC-link voltage and the change in error in DC-link voltage and these can be represented as:

\[ e(i) = V_{dc\text{ref.}} - V_{dc}(i) \]  
\[ de(i) = e(i) - e(i - 1) \]

where \( e(i) \) is the error and \( de(i) \) is the change in error in the \( i \)th iteration. \( V_{dc\text{ref.}} \) is the reference DC-link voltage of the reactor and \( V_{dc}(i) \) is the DC-link voltage in the \( i \)th iteration. The outputs of the FLC are chosen as the change in \( K_p \) value and the change in \( K_i \) value.

\[ K_p = K_{p\text{ref.}} + \Delta K_p \]  
\[ K_i = K_{i\text{ref.}} + \Delta K_i \]

where \( K_{p\text{ref.}} \) and \( K_{i\text{ref.}} \) are ref is reference proportional and integral gain, respectively. \( \Delta K_p \) and \( \Delta K_i \) are changes in \( K_p \) and \( K_i \) (Harish & Mahesh, 2008). Five triangular membership functions are chosen for the input variables and the output variable, namely: NB, NS, Z, PS and PB, representing negative big, negative small, zero and positive small and positive big, respectively, in the investigation implemented using the membership function editor as depicted at Figure 6(a). A fuzzy inference system file named “dstat.fis” is developed with the triangular membership functions as shown in Figure 6(b) with the help of FIS editor available in the Matlab/Simulink.

Also, the set of 25 fuzzy rules applied while modelling the controller is depicted in Table 1. The basic rule of FLC gives the relationship between the input and output (Deepa & Ranjani, 2015). The Rule base characterizes the control goals and control policy of the domain experts by means of set linguistic control rules. Most of the FLCs are based on various methods. The widely used method in
the FLC design is the Mamdani method proposed by Mamdani and his associates who adopted a min–max compositional rule of inference based on an interpretation of a control rule as a

Figure 6. (a): Membership functions for the FLC of the proposed model and (b): FIS file developed for the FLC of the proposed model.
conjunction of the antecedent and consequent and this method has been used in this work. The rule viewer and the surface viewers of the FLCs used in the model are shown Figures 7 and 8, respectively. The rule viewer is used for determining the approximate reasoning of the results of FLC and the surface viewer is used to observe the pattern of decision-making based on the rules formulated. The basic fuzzy rules are framed using the rule editor available in the MATLAB environment. After compiling the basic rules, the investigation is carried out in accordance with the rule and the surface viewers. With this approach, the output coefficient of the PI controllers is able to tune to the desired levels, thereby achieving the advantages of mitigating voltage sag as well as maintaining the DC-link voltage profile at a better level. Without integrating the FLC in the control system of the CSC-based D-STATCOM, it is not possible to improve the DC-link voltage profile.

Table 1. Rule base for fuzzy PI controller

|   | NB | NS | Z  | PS  | PB  |
|---|----|----|----|-----|-----|
| e |    |    |    |     |     |
| de|    |    |    |     |     |
| NB| NB | NB | NS | NS  | Z   |
| NS| NB | NB | NS | Z   | Z   |
| Z | NS | NS | Z  | PS  | PS  |
| PS| Z  | PS | PS | PB  | PB  |
| PB| Z  | Z  | PS | PB  | PB  |

Figure 7. Rule viewer of the proposed model.
4. Simulation results and discussions

The Simulink model of the proposed integrated fuzzy PI-controlled CSC-based D-STATCOM shown in Figure 9 has been simulated under steady-state (with normal load) and dynamic (sudden change in load) conditions. The various parameter settings of the model for simulation study are listed in Table 2. The practical feeder voltage in Indian three-phase power distribution system lies in the range of 415–400 V which operates at 50 Hz supply frequency. In the proposed model, a lower of 400 V has been chosen as the feeder system voltage taking into account the introduction of CSC topology instead of VSC one in the D-STATCOM which will cause more stress on the switching devices used in the inverter circuit in practical situation.

Firstly, the model has been simulated under normal load conditions without connecting the D-STATCOM and the heavily inductive three-phase series load by opening the three-phase circuit breakers 1 and 2, respectively. Figure 10 shows the voltage and current waveforms under normal load conditions. Figure 10(a) depicts the voltage waveform across the load and (b) shows the current waveform in the load. From this simulation result, it is observed that there is no voltage sag taking place across the load. The magnitude of voltage and current is found to be 360 V and 0.14 A, respectively.

Secondly, the model is simulated under sudden change in load conditions without operating the D-STATCOM. In this case, the D-STATCOM is disconnected by opening the circuit breaker 1 and the second heavily inductive three-phase load is connected by closing the three-phase circuit breaker 2. The circuit breaker 2’s closing transition time is set from 0.4 to 0.6 s. Figure 11(a) and (b) shows the load voltage and current waveforms, respectively. Under this condition, a voltage sag with a magnitude of 340 V which is 20 V less than the non-sag voltage magnitude for a duration from 0.4 to 0.6 s appears across the load as shown in Figure 11(a). Figure 12 shows the voltage and current waveforms at the PCC without operating the D-STATCOM.
Thirdly, the model has been simulated under sudden change in load conditions with operating the D-STATCOM. In order to mitigate the voltage sag taking place due to the sudden change in load, the D-STATCOM is brought to operation by closing the circuit breaker 1 with its transition time setting from 0.4 to 0.6 s. Figure 13(a) and (b) depicts the load voltage and current waveforms. It is observed that the load voltage sag during the period from 0.4 to 0.6 s has been effectively mitigated by the proposed D-STATCOM under this condition. The voltage profile of the load can be improved by connecting the LPF2 through the operation of circuit breaker 3 of the circuit. For reducing the overall cost of the AC-side filter, LPF2 may be eliminated or kept as optional. Under this condition, the performance of the control system of the proposed model in maintaining DC-link reactor voltage profile

| Name of parameters                                      | Value of parameters               |
|---------------------------------------------------------|-----------------------------------|
| Nominal power and frequency of the coupling transformer | 5,000 VA, 50 Hz                   |
| AC-side external reactor, Xr                            | R = 0.01 Ω, L = 1 mH              |
| Feeder impedance                                        | Rf = 0.01 Ω, Lf = 2 mH            |
| Feeder impedance                                        | Vf (PCC) = 400 V(rms), 50 Hz      |
| Feeder reference voltage                                 | Vf (ref.) = 328 V(rms), 50 Hz     |
| DC reference voltage                                     | Vdc (ref.) = 600 V                |
| DC-link reactor of CSC                                   | Ldc = 8,000 mH, Rdc = 0.01 Ω     |
| AC-side LPF1 shunt filter capacitor of CSC              | C = 2.85 mF                       |
| AC-side LPF2 shunt filter capacitor of CSC              | C = 8.5 mF                        |
| Inductive Load1                                         | R = 0.06 Ω, L = 8,000 mH         |
| Inductive Load2                                         | R = 0.06 Ω, L = 98000 mH         |
| PI controller gains for DC-link voltage                  | Kp (dc) = 0.25, Ki (dc) = 0.14    |
| PI controller gains for AC system voltage                | Kp (q) = 0.4, Ki (q) = 0.5        |
| Switching frequency of the CSC                           | fs = 20 kHz                       |
Figure 10. Voltage and current waveforms under normal load conditions.

Figure 11. Voltage and current waveforms under sudden change in load conditions without operating the D-STATCOM.

Figure 12. Voltage and current waveforms under sudden change in load conditions at PCC without operating the D-STATCOM.

Figure 13. Voltage and current waveforms under sudden change in load conditions with the operation of D-STATCOM.
during the voltage sag mitigation process has been examined at the time of simulation. Figure 14 shows the voltage waveform of the DC-link reactor with FLC integration with the conventional PI controller. With this approach, the magnitude of the voltage can be fairly maintained above 20 V (i.e. 22 V) before and after load perturbation. During the load disturbance period, from 0.4 to 0.6 s, the voltage magnitude of the voltage decreases 0 V for a duration of 0.08 s only. This reduction in voltage happens due to the fact that the inductor acts as a current source during the injection period and the voltage under steady-state condition becomes zero.

Lastly, the proposed model has also been simulated without integrating FLC, i.e. with PI controllers alone in order to observe the DC-link voltage profile under load perturbation. The voltage waveform of the DC-link reactor observed under this condition is shown in Figure 15. It is observed that the magnitude of the voltage goes on decreasing from its initial value of 20 V. During the load disturbance period, from 0.4 to 0.6 s, its value drastically reduces to 0 V with a delay of 0.02 s. From this observation, it is learnt that when CSC topology is used in other types of CP devices, such as DVR and unified power quality conditioner, integration of the FLC in the control system will definitely prove to be a good choice for maintaining an improved DC-link voltage profile.

5. Conclusions
In this paper, an integrated fuzzy PI-controlled CSC-based D-STATCOM has been modelled and simulated with the objective of mitigating voltage sag and also to maintain the improved DC-link voltage profile in a power distribution system under sudden change in load condition. The difficulty in maintaining DC-link voltage profile during voltage sag compensation period which is a challenge where inductor is used as the energy storage element instead of a pre-charged capacitor as in the case of VSC is overcome to a great extent with the integration of FLC in the control system of the proposed D-STATCOM. From this work, it is learnt that the voltage sag taking place at the distribution level under load perturbation can be successfully mitigated using a CSC-based D-STATCOM system instead of its VSC-based counterpart. This research paper will pave the way for initiating the application of CSC topology in other types of CP devices so as to enhance power quality in the future.
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Author details
M. Deben Singh1
E-mail: mdsingh2007@gmail.com
ORCID ID: http://orcid.org/0000-0001-9995-977X
Ram Krishna Mehta1
E-mail: rmehta.ee@gmail.com
ORCID ID: http://orcid.org/0000-0001-9995-977X
Arvind Kumar Singh1
E-mail: singharvindk67@gmail.com

1 Department of Electrical Engineering, North Eastern Regional Institute of Science & Technology, Nirjuli, Arunachal Pradesh 791109, India.

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