Type-Directed Compilation for Fault-Tolerant Non-Interference

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Abstract. Environmental noise (e.g. heat, ionized particles, etc.) causes transient faults in hardware, which lead to corruption of stored values. Mission-critical devices require such faults to be mitigated by fault-tolerance – a combination of techniques that aim at preserving the functional behaviour of a system despite the disruptive effects of transient faults. Fault-tolerance typically has a high deployment cost – special hardware might be required to implement it – and provides weak statistical guarantees. It is also based on the assumption that faults are rare. In this paper, we consider scenarios where security, rather than functional correctness, is the main asset to be protected. Our contribution is twofold. Firstly, we develop a theory for expressing confidentiality of data in the presence of transient faults. We show that the natural probabilistic definition of security in the presence of faults can be captured by a possibilistic definition. Furthermore, the possibilistic definition is implied by a known bisimulation-based property, called Strong Security. Secondly, we illustrate the utility of these results for a simple RISC architecture for which only the code memory and program counter are assumed fault-tolerant. We present a type-directed compilation scheme that produces RISC code from a higher-level language for which Strong Security holds – i.e. well-typed programs compile to RISC code which is secure despite transient faults. In contrast with fault-tolerance solutions, our technique assumes relatively little special hardware, gives formal guarantees, and works in the presence of an active attacker who aggressively targets parts of a system and induces faults precisely.

1 Introduction

Transient faults, or soft errors, are alterations of the state in one or more electronic components, e.g., bit flips in a memory module \cite{1}. In some situations, we are willing to accept that a system may fail due to transient faults, for example, that an occasional message may be lost or corrupted. The problem we address in this paper is how to prevent transient faults (which will be referred to as “faults” in the rest of the paper) from compromising the security of the system – for example, by allowing an attacker to access a secret.

It has indeed been shown that bit flips can effectively be used to attack, e.g., the AES encryption algorithm and reveal the cipher key \cite{2}. More recently, it has been shown that faults occurring in the computation of an RSA signature can permit an attacker to extract the private key from an authentication server \cite{3}. Moreover, it is not just the security of crypto systems that is potentially vulnerable. Risks are greatly amplified if
the attacker can influence the code executed by a system that can experience faults: it has been demonstrated that a single fault can cause (with high probability) a malicious but well-typed Java applet to violate the fundamental memory-safety property of the virtual machine [4].

Traditional countermeasures against faults aim to make devices fault-tolerant, i.e. able to preserve their functional behavior despite soft errors. Most fault-tolerance mechanisms are based on redundancy: resources are replicated (either in software or in hardware) so that it is possible to detect, if not repair, anomalies. Typically, such solutions are designed for protection against a very simple fault model, in which a limited number of faults are assumed. Moreover, the formal guarantees of software-based fault-tolerance mechanisms, according to Perry et al. [5], are usually not stated – it is more common that their efficacy is explored statistically. In reasoning about security it is more difficult to give a statistical model of the environment’s behaviour – it might be that the environment is an active adversary with a laser and a stopwatch (cf. [6]) rather than just passive background radiation. Similarly, experimental evidence based on typical deployment of representative programs is not likely to be so useful if an attack, as it often does, requires an atypical deployment of an unusual program.

**Overview of the Paper and Contributions**

In order to be precise about the guarantees that we provide and the assumptions we make, we develop a formal, abstract model of fault-prone systems, attackers who can induce faults based on the observations made of the system’s public output, and the resulting interaction between the two (Section 2.1). From this, we define our central notion of security in the presence of faults, *probabilistic fault-tolerant non-interference* (PNI). A system is secure in the presence of faults if, for any attacker, the probability of a given public output is independent of the secrets held by the system (Section 2.2).

Reasoning directly about fault-tolerant noninterference is difficult because (i) it demands reasoning about probabilities, and (ii) it quantifies over all possible attackers (in a given class).

**Our first contribution** tackles these difficulties with two key theorems. **Theorem 1** (Section 2.3) shows that PNI can be characterised exactly by a simpler *possibilistic* definition of noninterference, defined by assuming that the exact presence and location of faults are observable to the attacker. This removes difficulty (i), the need to reason about probabilities. **Theorem 2** (Section 2.4) then shows that the possibilistic definition is implied by a form of strong bisimulation property, adapting ideas from its use in scheduler independent security of concurrent programs [7]. This theorem eliminates difficulty (ii), enabling PNI to be proved without explicit quantification over all attackers.

**Our second contribution** (Section 3) illustrates the applicability of Theorem 2 in a specific setting: a fault-prone machine modeling a program running on a RISC-like architecture. The aim is to give a sound characterisation of RISC programs which, when placed in the context of the machine, give a system which is secure despite faults. Our approach combines ideas from security type systems for simple imperative programs with a *type-directed compilation* scheme. Roughly speaking, our type-directed compilation of simple imperative programs guarantees that a well-typed program compiles to RISC code which, for this architecture, is secure despite faults. A key assumption for
this result to hold is assuming fault-tolerant code memory and program counter, while
general purpose registers and data memory are susceptible to bit flips.

Our innovative perspective on the problem of guaranteeing security in the presence
of transient faults combines a lot of concepts from other works, coming from both
security and dependability literature. In order to clarify these connections, we discuss
related works in Section 4 whereas in Section 5 we focus on the main limitations of
our results (including those shared with other approaches). We complete the paper in
Section 6 where we briefly summarize the conclusions of our study.

2 A Theory for Probabilistic Fault-Tolerant Non-Interference

We begin (Section 2.1) by setting up a rigorous but abstract semantic model for
systems that can experience transient faults, and for environments inducing these faults.
Then, we establish a model for their interactions and a security definition (Section 2.2)
for the composition of a system with a fault environment as probabilistic fault-tolerant
non-interference (PNI). We continue (Section 2.3) by simplifying the security model
introduced for PNI in two steps. Firstly, we propose a simpler, nondeterministic fault
model for fault-prone systems. This model leads to a more straightforward notion of
security called possibilistic fault-tolerant non-interference (PoNI) which is then shown
to be equivalent to PNI. Finally, we introduce (Section 2.4) the notion of Strong Security
(SS), a bisimulation-based security condition which is proved stronger than PoNI, hence
PNI.

2.1 Probabilistic Fault-Tolerant Non-Interference

We model a fault-prone system as a deterministic labelled transition system. Since we
have to reason about bit flips, we model the state of a system as just a collection of
bits, each of which is identified by a unique location. The locations are partitioned into
a fault tolerant part of the system (e.g. memory with error correcting codes), and a
faulty part. Only the faulty locations are affected by soft errors from the environment.
The labels of the transition system model outputs of the fault-prone system and “clock
ticks” (τ) which mark the discrete passage of time. We assume that some outputs can
be distinguished by an external observer, whereas the others appear as τ.

Definition 1 (Fault-prone System). A fault-prone system Sys is defined as Sys =
\{Loc, Act, \rightarrow \subseteq S \times Act \times S\}, where:

- The set Loc contains all the locations (addresses) of the system. It is partitioned
  into a fault-tolerant subset and a faulty one, namely T and F. Fault-tolerant loc-
  ations are not affected by soft errors, whereas bits stored in the faulty part of the
  hardware can get flipped because of transient faults.
- Act includes system outputs and a distinguished silent action τ marking the pas-
  sage of time. We assume that “public” observations (what an attacker can see)
  are limited to events in LAct ⊆ Act, whereas any other action performed by the
  system is observed as τ.
- The relation \rightarrow formalizes the system behavior. Given the set of all possible states
  for the system, namely S = Loc \rightarrow \{0, 1\}, the relation \rightarrow models how the system

3 A similar but weaker notion of security has been presented in [8].
evolves. We write transitions in the usual infix manner $S \xrightarrow{a} S'$ for $S, S' \in S$. The system is deterministic in the sense that for any $S \in S$ there is at most one state $S'$ and one action $l$ and a transition $S \xrightarrow{l} S'$.

We now introduce a probabilistic fault model, which induces transient faults in $F$. We refer to this model as the environment, or, synonymously as the attacker.

A simple environment can be modeled as an agent that induces bit flips in the faulty locations with some fixed (small) probability. Unfortunately, this representation does not capture many realistic scenarios: for example, some locations in the system may be more error-prone than others, and (due to high densities of transistors) the probability of a location being flipped may be higher if a neighboring bit is flipped. We could therefore consider environments that can induce faults according to a probability distribution over the powerset of faulty locations, where the probability associated with a given set of locations $L$ is the probability that exactly the bits of $L$ are flipped before the next computation step occurs. However, such static model of the environment is not sufficient to model an active attacker. An active attacker may have physical access to the system (e.g., a tamper-proof smart card), and may be able to influence the likelihood of an error occurring at a specific location and time with high precision (see, e.g., [6]). What is more, the attacker may do this in a way that depends on the previous observations, namely the passage of time and the publicly observable actions. We therefore formalize these capabilities of an environment as follows (recall that $\mathcal{P}(A)$ here denotes the powerset of a given set $A$).

**Definition 2 (Fault environment).**

Consider a fault-prone system $\text{Sys} = \{\text{Loc}, \text{Act}, \rightarrow\}$. A fault environment $(\text{Err}, \text{Fault})$ for $\text{Sys}$ consists of:

- a labelled transition system $\text{Err} = (\mathcal{E}, \text{LAct} \cup \{\tau\}, \sim \subseteq \mathcal{E} \times (\text{LAct} \cup \{\tau\}) \times \mathcal{E})$, where $\mathcal{E}$ represents the set of environment’s states;

- a function $\text{Fault} : \mathcal{E} \rightarrow \mathcal{P}(F) \rightarrow [0, 1]$ such that for all states $E \in \mathcal{E}$, we have that $\text{Fault}(E)$ is a probability distribution on sets of locations.

We require that for all states $E \in \mathcal{E}$ and for all actions $a \in \text{LAct} \cup \{\tau\}$ there exists a unique state $E' \in \mathcal{E}$ such that $E \xrightarrow{a} E'$. Intuitively, the state $E \in \mathcal{E}$ determines the probability that a given set of locations (and no others) will experience a fault in the current execution step of the system. At each step, the state of the attacker evolves by the observation of “low” events and the passing of time.

**Example 1.** We illustrate the use of Definition 2 by characterizing the simplest most uniform fault-inducing environment: a bit flip may occur in any location with a fixed probability $\epsilon$. To model this as a fault environment, we need only a trivial transition system involving the single state $\bullet$ ($\mathcal{E} = \{\bullet\}$), whose transitions are $\forall a \in \text{LAct} \cup \{\tau\}. \bullet \xrightarrow{a} \bullet$. As for the Fault function consider a set $L \subseteq F$ where $|L| = k$ and $|F| = n$. Then the probability that flips occur in all locations in $L$ and nowhere else is equal to the probability of faults in every location in $L$, namely $\epsilon^k$, multiplied by the probability of the remaining locations not flipping, namely $(1 - \epsilon)^{n-k}$. Hence

$$\text{Fault}(\bullet)(L) = \epsilon^k(1 - \epsilon)^{n-k}$$

where $k = |L|$ and $n = |F|$. 
We now define, in outline (details are discussed in Appendix A), how fault environments are composed together with fault-prone systems. Some preliminary considerations are needed. We need to model the physical modification performed by the environment on the faulty part of the system. For this, a function \( \text{flip} \) is defined as
\[
\text{flip}(S, L) = S[l \mapsto \neg S[l], l \in L],
\]
which gives the result of flipping the value of every location in \( L \) of state \( S \) (assuming \( L \subseteq F \)). We also need to formalize that an attacker can distinguish only a subset of all possible actions of the system. This is obtained by assuming that there is a function \( \text{low} : \text{Act} \rightarrow \text{LAct} \cup \{\tau\} \) that behaves as the identity for actions in \( \text{LAct} \), and maps any other action to \( \tau \). This provides the public view of the system’s output. Finally, we say that a state \( S \) is stuck if there is no transition from that state.

**Definition 3 (Fault-prone System and Environment).** Consider a fault-prone system \( \text{Sys} = \{\text{Loc}, \text{Act}, \rightarrow\} \), and an environment \( \text{Env} = (\text{Err}, \text{Fault}) \) where \( \text{Err} = \langle \text{E}, \text{LAct} \cup \{\tau\}, \sim_{\tau} \rangle \). The composition of \( \text{Sys} \) and \( \text{Env} \), defined as \( \text{Sys} \times \text{Env} = \langle S \times \text{E}, (\text{Act}, [0, 1]), \rightarrow\rangle \) where \( S \) is the set of all possible states for \( \text{Sys} \), defines a labelled transition system whose states are pairs of the system state and the environment state, and with transitions labelled with an action \( a \) and a probability \( p \), written \( a \rightarrow p \). Transitions depend on the state of the system as follows:

- If the system state \( S \) is not stuck, it undergoes a transient fault according to the \( \text{flip} \) function; then, providing the flipped state is not stuck, the execution takes place, namely
  \[
  \pi = \{L \mid L \in \wp(F) \text{ and } \text{flip}(S, L) \xrightarrow{a} S'\}
  \]

  \[
  p = \Sigma_{L \in \pi} \text{Fault}(E)(L) \xrightarrow{\text{low}(a)} E', E \xrightarrow{\sim_{\tau}} E''
  \]

  Observe that, in general, there might be several subsets of \( L \subseteq F \) such that \( \text{flip}(S, L) \) results in a state that (i) performs the same action \( a \) and (ii) performs a transition to the final state \( S' \). For this reason, the probability associated with the rule corresponds to the sum of all probabilities associated with locations in the set \( \pi \).

- If the system state is stuck, or it is made stuck by a transient fault, it does not perform any action. However, both the environment and the composition of the system state with the environment state evolve as if the system had performed a \( \tau \) action. We enforce these restrictions because an error environment should not be able to distinguish between an active but “silent” and a stuck state. Notice that this way of modeling the composition of systems and environments guarantees that any state of the composition can progress.

This form of transition system is sometimes known as a fully probabilistic labelled transition system, or a labelled markov process.

### 2.2 Defining Security

We can now reason about security of a system operating in an environment: \( \text{Sys} \times \text{Env} \). Firstly, we define the observations that the attacker can perform. Then, we define when sensitive data remains secure despite the attacker observations.
Our attacker sees sequences of actions in $LAct \cup \{\tau\}$, called *traces*, and measures their probability, but does not otherwise have access to the state of the fault-prone system.

We say that the sequence $r = Z \overset{a_0}{\rightarrow} p_0 Z_1 \ldots Z_{n-1} \overset{a_{n-1}}{\rightarrow} p_{n-1} Z_n$ is a *run* of size $n$ of a system state $Z \in \text{Sys} \times \text{Env}$ and has probability $\Pr(r) = \prod_{0 \leq i \leq n-1} p_i$. The set of all $n$-runs of $Z$ are denoted $\text{run}_n(Z)$, and we define the set of all runs for $Z$ as $\text{run}(Z) = \sqcup_n \text{run}_n(Z)$. Consider a run $r = Z \overset{a_0}{\rightarrow} p_0 Z_1 \ldots Z_{n-1} \overset{a_{n-1}}{\rightarrow} p_{n-1} Z_n$ and let trace $\in \text{run}(Z) \rightarrow (LAct \cup \{\tau\})^*$ be a function such that $\text{trace}(r) = \text{low}(a_0) \ldots \text{low}(a_{n-1})$. For any $t \in (LAct \cup \{\tau\})^n$, define $\Pr_Z(t) = \sum_{(r \in \text{run}_n(Z) : \text{trace}(r) = t)} \Pr(r)$. This definition induces a probability distribution over $(LAct \cup \{\tau\})^n$.

**Proposition 1.** For any state $Z \in \text{Sys} \times \text{Env}$ and for any $n \geq 0$ $\sum_{t \in (LAct \cup \{\tau\})^n} \Pr_Z(t) = 1.$

**Proof.** Appendix [9]

We can now define the notion of probabilistic noninterference [9] that characterises security for fault-prone systems. For this purpose, we consider the case when the initial state of a fault-prone system is an encoding of three different components: (i) a “program”, the set of instructions executed by the system, (ii) “public data”, that stores values known by an attacker and (iii) “private data” for confidential information. We formalize this partition by defining three mutually disjoint sets $\text{ProgLoc}$, $\text{LowLoc}$ and $\text{HighLoc}$ (such that $\text{Loc} = \text{ProgLoc} \cup \text{LowLoc} \cup \text{HighLoc}$) and, for a system state $S$, by defining the program component $P$ as $S \mid_{\text{ProgLoc}}$, the public data $L$ as $S \mid_{\text{LowLoc}}$ and $H$ as $S \mid_{\text{HighLoc}}$.

Observe that the way locations are partitioned between program and data is orthogonal to the way they are partitioned between fault-tolerant and faulty components. This is because fault-tolerance is orthogonal to the way security is defined.

Our definition of security, *Probabilistic Fault-Tolerant Non-Interference* (PNI), requires a notion of equivalence to be defined for states that look the same from an attacker’s point of view. Two system states $S$ and $S'$ are low equivalent, written as $S \equiv_L S'$, if $S \mid_{\text{LowLoc}} = S' \mid_{\text{LowLoc}}$. Low equivalence provides us a way for defining when the program component of a state is secure even in the presence of transient faults. Intuitively the definition says that a program component $P$ is secure if the observed probability for any trace is independent of the sensitive data, for all system states where $P$ is the program component.

**Definition 4 (PNI).** Let $\text{Sys}$ be a fault-prone system and let $P$ be a program component of $\text{Sys}$. We say that $P$ is probabilistic fault-tolerant noninterfering, if for any system states $S, S' \in \text{Sys}$ such that $S \mid_{\text{ProgLoc}} = S' \mid_{\text{ProgLoc}} = P$ and $S \equiv_L S'$, it holds that for any state $E$ of any environment $\text{Env}$, for any $n \geq 0$ and for any $t \in (LAct \cup \{\tau\})^n$ we have $\Pr(\langle S, E \rangle(t) = \Pr(\langle S', E \rangle(t)$.

The definition demands that probability of publicly observable traces only depends on values stored in the low locations. Also, it requires that this must hold for any fault-environment.
2.3 Possibilistic Characterisation of Fault-Tolerant Non-Interference

Reasoning directly about fault-tolerant noninterference is difficult because (i) it demands reasoning about probabilities, and (ii) it quantifies over all possible attackers (in a given class). In this section, we address the first of these problems.

A possibilistic model (i.e. not probabilistic) of the interaction between a fault-prone system and the error environment can be obtained by interleaving the transitions of the fault prone system with a nondeterministic flipping of zero or more bits. While this model avoids reasoning about probability distributions as well as injection of faults by an attacker, it is not adequate to directly capture security, as it is well-known that possibilistic noninterference suffers from probabilistic information leaks (see e.g. [9]). In order to capture PNI precisely, we augment this transition system by making the location of the faults observable (details are discussed in Appendix C).

Definition 5 (Augmented Fault-prone System). Given a fault-prone system \( \text{Sys} = \{ \text{Loc}, \text{Act}, \rightarrow \} \) we define the augmented system \( \text{Sys}^+ = \{ \text{Loc}, \wp(F) \times \text{Act}, \rightsquigarrow \} \), where \( \rightsquigarrow \) is defined according to two cases:

- If the system state \( S \) is not stuck, it undergoes a nondeterministic transient fault first; then, providing the flipped state is not stuck, execution takes place, namely
  \[
  \text{flip}(S, L) \xrightarrow{a} S' \quad L \subseteq F
  \]
  \[
  S \xrightarrow{L, a} S'
  \]
  Observe that, compared to the corresponding rule in Definition 3, we have that \( L \) induces a unique transition since it appears in the transition label.

- If the system state is stuck, or it is made stuck by a transient fault, the transition does not modify it. However, the label attached to the transition is \( (L, \tau) \) so that, as in Definition 3 we make a stuck state indistinguishable from a silently diverging one.

The model resembles the composition of fault-prone systems and fault environments presented in Definition 3 including the fact that it hides the termination of a system configuration. However, it introduces two main differences that influence the way security is defined. On one hand, the augmented system is purely nondeterministic, and this supports a simpler definition of security. On the other hand, the augmented system has more expressive labels, that include not only the action performed by the system but also information about flipped locations.

We call the sequence \( r = S \xrightarrow{L_0, a_0} S_1 \xrightarrow{L_1, a_1} \ldots \xrightarrow{L_{n-1}, a_{n-1}} S_n \) a possibilistic run of a system state \( S \in \text{Sys}^+ \), and we say that \( t = L_0, \text{low}(a_0), \ldots, L_{n-1}, \text{low}(a_{n-1}) \) is its corresponding trace. We write \( S \rightsquigarrow t \) when there exists a run \( r \), produced by \( S \), that corresponds to \( t \). With these conventions, security for augmented systems, Possibilistic Fault-Tolerant Non-Interference (PoNI), is defined by using the same notation presented in the previous section for fault-prone systems composed with environments.

Definition 6 (PoNI). We say that a program component \( P \) enjoys possibilistic fault-tolerant non-interference, if for any \( S, S' \in \text{Sys}^+ \) such that \( S' \big|_{\text{ProgLoc}} = S \big|_{\text{ProgLoc}} = P \) and \( S \rightsquigarrow t \), for any trace \( t \), it holds that \( S \rightsquigarrow t \Leftrightarrow S' \rightsquigarrow t \).
The following result says that the definitions of PNI and PoNI coincide.

**Theorem 1.** A program component $P$ enjoys PNI if and only if it enjoys PoNI.

*Proof.* Appendix D

This theorem makes clear that, from an enforcement perspective, security in the presence of transient faults can be achieved by targeting either PNI or PoNI.

### 2.4 Strong Security Implies PNI

We now formalize a different notion of security that guarantees PoNI (and hence PNI) without explicitly modeling the effects of transient faults in a fault-prone system. This notion, called Strong Security, was developed as a way to capture a notion of scheduler independent compositional security for multithreaded programs [7].

Strong security is a bisimulation relation over program components of fault-prone systems. Our goal is to relate strong security to the possibilistic security definition established for augmented systems, and show that indeed it is stronger. Before doing so, we need to make sure that the semantics of fault-prone systems hides termination, as it is the case for augmented systems. In particular, for a fault-prone system $Sys = \{Loc, Act, \rightarrow\}$, we define its termination-transparent version as $Sys^\infty = \{Loc, Act, \rightarrow^\infty\}$ where $\rightarrow^\infty$ coincides with $\rightarrow$ for active states, but has additional transitions $S \xrightarrow{\tau}^\infty S$ whenever $S \not\rightarrow (details are discussed in Appendix C). With this, we define strong security for termination-transparent fault-prone systems as follows.

**Definition 7 (Strong Security (SS)).** Let $Sys$ be a fault-prone system and $Sys^\infty = \{Loc, Act, \rightarrow^\infty\}$ be the corresponding termination-transparent fault-prone system. A symmetric relation $R$ between program components is a strong bisimulation if for any $(P, P') \in R$ we have that for any two states $S, V$ in $S$, if $S|_{ProgLoc} = P$ and $V|_{ProgLoc} = P'$ and $S =_L V$ and $S \xrightarrow{a}^\infty S'$ then $V \xrightarrow{b}^\infty V'$ such that (i) $\text{low}(a) = \text{low}(b)$ and (ii) $S' =_L V'$ and (iii) $(S'|_{ProgLoc}, V'|_{ProgLoc}) \in R$. We say that a program component $P$ is strongly secure if there exists a strong bisimulation $R$ such that $(P, P) \in R$.

Intuitively, a program component $P$ is strongly secure when differences in the private part of the data are neither visible in the computed public data, nor in the transition label. This anticipates the fact that even though an external agent (the error environment, in our scenario) might alter the data component, the program behavior does not reveal anything about secrets.

The next result shows that Strong Security is sufficient to obtain PoNI. Notice, however, that the definition of Strong Security only deals with the modifications that occur in the data part of a fault-prone system. Hence, it only makes sense for the class of systems that host the program component in the fault-tolerant part of the configuration.

**Theorem 2 (Strong security \(\Rightarrow\) PoNI).** Let $P$ be a program component such that $ProgLoc \subseteq T$. If $P$ satisfies SS then $P$ satisfies PoNI.

*Proof.* Appendix F
We conclude this section with a negative result by saying that the reverse implication between SS and PoNI does not hold. Strong security requires that the partition of the state into a program, a low and a high part is preserved (respected) during the whole computation whereas the definition of PNI imposes no special requirement on intermediate states of the computation.

3 A Type System for FTNI

In this section, we present an enforcement mechanism capable of synthesizing strongly secure assembly code. The enforcement is given as a type-directed compilation from a source while-language. All in all, we present a concrete instance of our fault-prone system formalization by defining the RISC architecture (Section 3.1) and propose a technique to enforce strong security over RISC programs (Section 3.2), whose soundness is sketched in Section 3.3. By achieving strong security, we automatically get secure RISC code that is robust against transient faults (recall Theorem 2).

3.1 A Fault-Prone RISC Architecture

The architecture we are interested in has various hardware components to operate over data and instructions.

- Data resides in the memory and in the register bank. We model the memory \( \mathcal{M} \) as a function \( \mathbb{W} \to \mathbb{W} \), where \( \mathbb{W} \) is the set of all constants that can be represented with a machine word. The register bank \( R \) is modeled as a function \( \text{Reg} \to \mathbb{W} \), where \( \text{Reg} \), ranged over by \( r, r' \), is a set of register names.

Figure 1 describes the instruction set of our architecture. We consider that every instruction \( I \) could be optionally labeled by a label in the set \( \text{Lab} \). Instruction load \( r k \) accesses the data memory \( \mathcal{M} \) with the pointer \( k \in \mathbb{W} \) and writes the value pointed by \( k \) into register \( r \in \text{Reg} \). The corresponding store \( k r \) instruction writes the content of \( r \) into the data memory address \( k \). Instruction jmp \( l \) causes the control-flow to transfer to the instruction labeled as \( l \). Instruction \( jz l r \) performs the jump only if the content of register \( r \) is zero. Instruction \( \text{nop} \) performs no computation. The instruction \( \text{mov} k r \) writes the constant \( k \) to \( r \), whereas the instruction \( \text{mov} r r' \) copies the content in \( r' \) to \( r \). The instruction \( \text{op} \) stands for a generic binary operator that combines values in \( r \) and \( r' \) and stores the result in \( r \). Instruction \( \text{out} ch r \) outputs the constant contained in \( r \) into the channel \( ch \), that can be either \( \text{low} \) or \( \text{high} \).

The processor fetches RISC instructions from the code memory \( P \), separated from \( \mathcal{M} \). The code memory is modeled as a list of instructions. We require the code memory to be well-formed, namely not having two instruction bodies labeled in the same way. A dedicated program counter register stores the location in \( P \) hosting the instruction being currently executed. The value of the program counter is ranged over by \( pc \).

As described in Section 2, we partition the architecture into faulty and fault-tolerant components. Both \( R \) and \( \mathcal{M} \) are considered to be faulty: transient faults can strike
any location at any time during the execution. On the other hand, we assume \( P \) and the program counter are implemented in the fault-tolerant part of the architecture. The fact that the code memory is fault-tolerant corresponds to having the machine code in a read-only memory with ECC, a common assumption in dependability domain. The requirement on the program counter is a restriction that turns out to be necessary for proving the soundness of our enforcement mechanism.

We instantiate the RISC architecture as a fault-prone system by defining the semantics of the language as a labelled transition system. A state is defined as a quadruple \( \langle P, pc, R, M \rangle \), for \( pc \in \mathbb{W} \), where the first two elements correspond to the fault-tolerant portion of the hardware. Any action of the system is either an output (\( \text{low}!k \) when the output is performed on the publicly observable channel, \( \text{high}!k \) otherwise) or the silent action \( \tau \). A few examples of transition rules are described in Figure 2 (the full presentation can be found in Appendix F). We write \( P(pc) \) as a shorthand for the instruction at position \( pc \) in \( P \) and \( pc+1 \). We assume that the function \( \text{res}_P \in \text{Lab} \to \mathbb{W} \) returns the position at which label \( l \) occurs in \( P \): \( \text{res}_P(l) = i \) iff \( P(i) = l : B \) for some \( B \).

Once the rule \([\text{Load}]\) is triggered, the register content at \( r \) is updated with the memory content at \( p \) (\( R[r \to M(p)] \)), and the program counter is incremented by one (\( pc^+ \)). Conversely, the rule \([\text{Store}]\) writes the content at register \( r \) in memory location \( p \) (\( M[p \to R(r)] \)). In case of a jump instruction, neither memory nor registers are modified. If the guard is 0, as in rule \([\text{Jz} - \text{S}]\), the execution is restarted at the instruction of the label used as the jump argument \( pc \to \text{res}_P(l) \), otherwise the program counter is just incremented. All previous instructions map to silent actions \( \tau \): channels are written by instruction \([\text{Out}]\) which, on the other hand, leaves both register and memory untouched.

### 3.2 Strong Security Enforcement

We guarantee strong security for some RISC programs via a novel approach based on type-directed compilation. Our strategy targets a simple high-level imperative language, while. For while programs we define a type system that performs two tasks: (i) translation of while programs into RISC programs (ii) enforcement of Strong Security on while programs. The compilation is constructed so that the strong security at the level of while programs is preserved by the compilation.
To facilitate the proof of strong security, the method is factored into a two-step process: a type-directed translation to an intermediate language followed by a simple compilation to RISC. In this section, we limit ourselves to an overview of the method and therefore elide this intermediate step from the presentation.

The grammar of the while language is presented in Figure 3. Both expressions and commands are standard, and assume that the language contains an output command `out`.

\[
C ::= \text{skip} \mid x := E \mid \text{if } E \text{ then } C_1 \text{ else } C_2 \mid \text{out } ch \ E \mid C_1; C_2 \mid \text{while } x \text{ do } C
\]

\[
E ::= k \in \mathbb{W} \mid x \in \text{Var} \mid E_1 \text{ op } E_2
\]

\[
ch ::= \text{low} \mid \text{high}
\]

Fig. 3. while programs syntax

Typing Expressions The general structure of the typing judgement for expressions is presented in Figure 4. The core part of the judgement says that while expression \( E \) (2) can be compiled to secure RISC program \( P \) (3), with security annotation (4). For defining the security annotation, we assume while variables and RISC registers are partitioned into two security levels \( \{L, H\} \) (ordered according to \( \sqsubseteq \), which is the smallest reflexive relation for which \( L \sqsubseteq H \)) according to the function \( \text{level} \in \text{Var} \cup \text{Reg} \rightarrow \{L, H\} \).

The first component \( \lambda \) of a security annotation \( (\lambda, n) \) specifies the security level of the registers that are used to evaluate an expression. The second component \( n \) represents the number of RISC computation steps that are necessary to evaluate \( E \). The reason for tracking this specific information about expressions (and in commands later on) is related to obtain assembly code which avoids timing leaks – the type-directed compilation will use \( n \), for instance, to do padding of code when needed \[10\]. In fact, most of the involved aspects in our type-system arises from avoiding timing leaks in low-level code.

Because the compilation is defined compositionally, some auxiliary information (1) is required: we firstly need to know the label \( l \) which is to be attached to the first instruction of \( P \). Also, we have to consider the set \( A \) of registers which cannot be used in the compilation of \( E \), since they hold intermediate values that will be needed after the computation of \( E \) is complete. Finally, we need to keep track of how variables are mapped to registers. This is done via the register record \( \Phi \), which requires a slightly more elaborate explanation.

Register Records In order to allow for efficiently compiled code, expression compilation builds up a record of associations between while variables and RISC registers in a register record \( \Phi \in \text{Reg} \rightarrow \text{Var} \). If \( \Phi(r) = x \) then it means that the current value of variable \( x \) is present in register \( r \). The register record produced by a compilation is highly nondeterministic, meaning that we do not build any particular register allocation mechanism into the translation.
The rules (in particular the later rules for commands) involve a number of operations on register records which we briefly describe here. We ensure that a register record is always a partial bijection, namely a register is associated to at most one variable and a variable is associated with at most one register. We write $\Phi[r \leftrightarrow x]$ to denote the minimal modification of $\Phi$ which results in a partial bijection mapping $r$ to $x$. Similarly, $\Phi[r \not\rightarrow]$ denotes the removal of any association to $r$ in $\Phi$. The intersection of records $\Phi \cap \Phi'$ is just the subset of the bijections on which $\Phi$ and $\Phi'$ agree. Finally, inclusion between register records, written as $\Phi \subseteq \Phi'$, holds if all associations in $\Phi$ are also found in $\Phi'$.

Beside the compiled expression and its security annotation, each rule returns a modified register record and specifies the actual register where the evaluation of the expression $E$ is found at the end of the execution of $P$ (5).

**Expression Rules**

It will be convenient to extend the set of instructions with the empty instruction $\epsilon_I$. Some sample rules for computing the types of expressions are presented in Figure 5 (the full presentation can be found in Appendix G).

In rule $[K]$ the constant $k$ is compiled to code which write the constant to some register $r$ via the move $k$ $r$ instruction, provided $r$ is not already in use ($r \not\in A$). As a result, any previous association between register $r$ and a variable is lost ($\Phi[r \not\rightarrow]$). The security level of the result is simply the level of the register, and the computation time is one.

In rule $[V - cached]$ the variable to be compiled is already associated to a register, hence no code is produced.

**Typing Commands**

The general structure of a typing rule for commands is presented in Figure 6. Judgements for commands assume a starting label for the code to be produced, and an incoming register record (1). A compilation will result in a new (outgoing) register record, and the label of the next instruction following this block (2) (cf. Figures 8–9 and 10). The security annotation (3) is similar to that for expressions; $w$, the write effect, provides information about the security level of variables, registers, and channels to which the compiled code writes, and $t$ describes its timing behaviour. However, $w$ and $t$ are drawn from domains which include possible uncertainty.

The write effect $w$ is described with a label defined in the set $\{\text{Wr}_H, \text{Wr}_L\}$, with partial ordering $\text{Wr}_H \subseteq \text{Wr}_L$. The value $\text{Wr}_H$ is for programs that never write...
The timing behavior of a command is described by an element of the partial order (and associated operations) defined in Figure 2. We use timing \( t = \text{Trm} n \), for \( n \in \mathbb{N} \), when termination of the code is guaranteed in exactly \( n \) steps (and hence is independent of any secrets); \( t = \text{Trm} L \) is used for programs whose timing characterization does not depend on secret values, but whose exact timing is either unimportant, or difficult to calculate statically. When secrets might directly influence the timing behavior of a program, the label \( \text{Trm} H \) is used.

**Command Rules** We now introduce some of the actual rules for commands. The concatenation of code memories \( P \) and \( P' \) is written \( P + P' \) and is well defined if the resulting program remains well-formed. It will be convenient to extend the set of labels \( \text{Lab} \) with a special empty label \( \epsilon_{\text{lab}} \) such that \( \epsilon_{\text{lab}} : B \) simply denotes \( B \). Also, we consider that the empty instruction \( \epsilon_I \) is such that if \( P = [B, I_1, \ldots, I_n] \) we define \([l : \epsilon_I] + P\) as \([l : B, I_1, I_2, \ldots, I_n]\).

The rule \([:=] \) in Figure 8 requires that the security level of expression \( E \) matches the level of the variable \( x \) (\( \langle \text{level} (x), n \rangle \)). If this is possible, the compilation is completed by storing the value of \( r \) into the pointer corresponding to \( x \) via the instruction \( \text{store} v2p(x) \) \( r \) (assuming there exists an injective function \( v2p \in \text{Var} \rightarrow \mathbb{W} \) which maps variables to memory locations), and the register record is updated by associating \( r \) and \( x \) (\( \Phi' \rightarrow r \leftrightarrow x \)). The resulting security annotation depends on the level of \( x \): when \( \text{level} (x) = H \) the security annotation is \( \langle \text{Wr} H, \text{Trm} n + 1 \rangle \), otherwise it is \( \langle \text{Wr} L, \text{Trm} L \rangle \). Rules for skip and out can be found in Appendix H.

The rule \([\text{if} \ - \ \text{any}] \) in Figure 9 builds the translation of the if statement by joining together several RISC fragments. The basic idea of this rule is that it follows Denning’s classic condition for certifying information flow security: if the conditional involves high data then the branches of the conditional cannot write to anything except high variables. This is obtained by imposing the side condition \( w_i \subseteq \text{write}(\lambda) \), where \( w_i \) is the write-effect of the respective branches, and write is a function mapping the se-
sequence of jump out of the block. The resulting register record of the whole command compilation is the common part of the register records resulting from the respective branches.

conditional expression which computes purely with high data – a so-called write and cannot be allowed to write to low data (register records are passed sequentially from inputs to outputs, and the security types are high conditionals by Smith [12]). The basic strategy is to compute the timing of each high conditional. This is related to timing-sensitive information-flow typing rules for high conditionals. The only way that we can permit a computation to securely write to low variables after independent of the high data (which might depend on high data (write(H) = Wr H), as this would otherwise reveal information about the high data through timing of low events).

Fig. 9. Type rules for if

![Type rules for if](image)

security level of the guard into its corresponding write-effect (such that write(H) = Wr H and write(L) = Wr L). In this rule, in contrast to the [if – H] rule for the conditional, the timing properties of the two branches may be different, so we do not attempt to return an accurate timing. Hence, the use of the operator ⊓ which just records whether the timing depends on only low data, or possibly any data (notice that the security level of the guard is mapped into its corresponding timing label by the function term, such that term(L) = Trm L and term(H) = Trm H). The compilation of the conditional code into RISC is fairly straightforward: compute the expression (P_0) into register r, jump to else-branch (P_2) if r is zero, otherwise fall through to “then” branch (P_1) and then jump out of the block. The resulting register record of the whole command compilation is the common part of the register records resulting from the respective branches.

The rule [if – H] (Figure 9) allows the system to be more permissive. It deals with a conditional expression which computes purely with high data – a so-called high conditional. This rule, when applicable, compiles the high conditional in a way that guarantees that its timing behaviour is independent of the high data. This is important since it is the only way that we can permit a computation to securely write to low variables after a high conditional. This is related to timing-sensitive information-flow typing rules for high conditionals by Smith [12]. The basic strategy is to compute the timing of each branch (n_1 and n_2 respectively) and pad the respective branches in the compiled code with sequences of nop instructions so that they become equally long, where nop^n is a sequence of m consecutive nop instructions when m > 0, and is ε otherwise.

The rule [:] for sequential composition (Figure 10) is largely standard: the label and register records are passed sequentially from inputs to outputs, and the security types are combined in the obvious way. The only twist, the side condition, encodes the key idea in the type system of Smith [12]. If the computation of the first command has timing behaviour which might depend on high data (t_1 = Trm H), then the second command cannot be allowed to write to low data (w_2 = Wr H), as this would otherwise reveal information about the high data through timing of low events.
record on exit. This is because we need a single description of the exit register record
conditions relating the register record at the beginning of the loop, and the register
Firstly, as one would expect in a typing rule for a looping construct, there are technical

$$\Phi \vdash C_1 \leftrightarrow P_1, \langle w_1, t_1 \rangle, l_1, \Phi_1 \quad \Phi_1, l_1 \vdash C_2 \leftrightarrow P_2, \langle w_2, t_2 \rangle, l_2, \Phi_2$$

$$t_1 = \text{Trm } H \Rightarrow w_2 = \text{Wr } H$$

Fig. 10. Type rules for sequential composition (·) and while

The compilation of the while command (Figure 10) is quite involved for two reasons.
Firstly, as one would expect in a typing rule for a looping construct, there are technical
conditions relating the register record at the beginning of the loop, and the register
record on exit. This is because we need a single description of the exit register record
$$\Phi_B$$ which approximates both the register record at the start of the loop body ($$\Phi[r \leftrightarrow x]$$)
and the register record after computing the loop body and putting $$x$$ back into register $$r$$
($$\Phi_E[r \leftrightarrow x]$$). Secondly, for technical reasons relating purely to the proof of correctness
(security), the code is (i) a little less compact that one would expect to write due to an
unnecessarily repeated subexpression, and (ii) contains a redundant instruction store $$x$$
immediately after having loaded $$x$$ into $$r$$. The lack of compactness is due to the fact that
the proof goes via an intermediate language that cannot represent the ideal version of
the code. The redundant instruction establishes a particular invariant that is needed in
the proof: not only is $$x$$ in register $$r$$, but it arrived there as the result of writing $$r$$ into $$x$$. The security concerns are taken care of by ensuring that the security level of the whole
loop is consistent with the levels of the branch variable $$x$$ and the branch register $$r$$,
and that if the timing of the body might depend on high data, then the level of the loop
variable (and hence the whole expression) must be $$H$$.

All the rules introduced in this section are used in Appendix J to compile a simple
while program that computes a hash function.

3.3 Soundness

We open this section by instantiating the definition of strong security for RISC programs,
which requires to view the RISC machine as an instance of a fault-prone system
(Definition 1). For this we consider the set of locations Loc of the RISC fault-prone system
to be the names of the individual bits comprising the registers and memories. So,
for example, a general purpose register $$r$$ corresponds to some set of locations $$r_0, \ldots, r_{31}$$
(for a word-size of 32). With this correspondence, the set of states of the RISC system
are isomorphic to the set of functions Loc $$\rightarrow \{0, 1\}$$. As mentioned earlier, the fault-
prone locations $$F$$ are those which correspond to the general purpose registers and the
data memory.

For the definition of security we must additionally partition the locations into the
program ProgLoc, the low locations LowLoc, and the high locations HighLoc: ProgLoc
comprises the locations of the code and the program counter register, LowLoc the loca-
tions of the low variables and registers, and HighLoc the locations of the high variables and registers.

Since assembly programs are run starting at their first instruction, the following slightly specialised version of strong security is appropriate:

**Definition 8 (Strong Security for RISC programs).** We say that an assembly program $P$ is strongly secure if $(P, 0)$ is strongly secure according to Definition 7 instantiated on the fault-prone system $\mathcal{A} = \{\text{Loc}, \{\text{ch}!k|\text{ch} \in \{\text{low, high}\} \text{ and } k \in \mathbb{W}\} \cup \{\tau\}, \rightarrow\}$.

The type system defined in Section 3.2 guarantees that any type-correct while program is compiled into a strongly secure RISC program. This is formalized as follows.

**Theorem 3 (Strong security enforcement).** Let $C$ be a while program, and suppose $\{\}, \epsilon_{\text{lab}} \vdash C \rightarrow P, \langle w, t \rangle, l, \Phi$. Then $P$ is strongly secure.

**Proof.** See Section I.

According to Theorem 3 we can obtain strongly secure RISC programs from type-correct while programs. Theorem 2 (Section 2.3) states that strong security is a sufficient condition to guarantee PoNI. The two results together express a strategy to translate while programs into RISC programs that enjoy PoNI. We state this formally by instantiating the definition of PoNI for RISC programs.

**Definition 9 (PoNI for RISC programs).** We say that an assembly program $P$ enjoys PoNI if $(P, 0)$ is PoNI according to Definition 6 instantiated on the fault-prone system $\mathcal{A} = \{\text{Loc}, \{\text{ch}!k|\text{ch} \in \{\text{low, high}\} \text{ and } k \in \mathbb{W}\} \cup \{\tau\}, \rightarrow\}$.

**Corollary 1 (PoNI enforcement on RISC programs).** Let $C$ be a while program, and suppose $\{\}, \epsilon_{\text{lab}} \vdash C \rightarrow P, \langle w, t \rangle, l, \Phi$. Then $P$ is PoNI.

**Proof.** Direct application of Theorem 3 and Theorem 2.

## 4 Related Work

### Fault Tolerant Non-Interference

The only previous work of which we are aware that aims to prevent transient faults from violating noninterference is by Del Tedesco et al. [8]. The enforcement approach of that paper is radically different from the approach studied here, and the two approaches are largely complimentary. Here we highlight the differences and tradeoffs:

- Targeting a similar RISC machine, the implementation mechanism of [8] is a combination of software fault isolation [13] and a black-box non-interference technique called secure multi-execution [14]. This can be applied to any program, but only preserves the behaviour of noninterfering memory-safe programs. Verifying that a program is memory-safe would have to be done separately, but could be achieved by compiling correctly from a memory-safe language.

- In [8], fault-tolerance is assumed for the code memory but not in the program counter register. The cost of this is that the method described in that paper can only tolerate up to a statically chosen number of faults, whereas in the present work we can tolerate any number.
The security property enforced by the method described in [8] is a restriction of PoNI to runs with a limited number of faults. However, the work does not justify this definition with respect to the more standard notion of probabilistic noninterference. The limitation in the number of faults, together with our result, shows that the established security property is strictly weaker than PNI.

**Strong Security for Fault Tolerance** This paper is not the first to realise that Sabelfeld and Sands’s strong security [7] implies security in the presence of faults. Mantel and Sabelfeld [15] used strong security in a state-based encoding of channel-based communication. They observed that strong security is not affected by faults occurring in message transmission. Another way to think of this is that strong security of individual threads implies strong security of their composition; a faulty environment is itself a strongly secure thread, simply because it has no ability to read directly from secrets in the state.

**Related Type Systems** The type-directed compilation presented here combines several features which are inspired by existing non-interference type systems for sequential and concurrent programming languages. Our security notion is timing sensitive and has some similarities with Agat’s [10] type-directed source-to-source transformation method that maps a source program into an equivalent target program where timing leaks are eliminated by padding. Similar ideas were shown to apply to a type system for strong security [7]. Our padding mechanism is different from Agat’s, since it is based on counting the number of computation steps in the branches of a high conditional expressions, and our system is more liberal, since it allows e.g. loops with a secret guard. These distinguishing features are both present in Smith’s type system for a concurrent language [12] (see also [16]).

**Non-interference for Low-level Programming Languages** Medel et al. [17] propose a type system for a RISC-like assembly language capable to enforce (termination and time insensitive) non-interference. Enforcing the same security condition, Barthe et al. [18] introduce a stack-based assembly language equipped with a type system. Subsequent work [19] shows a compilation strategy which enforces non-interference across all the intermediate steps until reaching a JVM-like language. Bartuti et al. [20] use a different notion for confidentiality, called $\sigma$-security, which is enforced by abstract interpretation.

**Dependability** The need for a stronger connection between security and dependability has been stated in many works (e.g. [21,22]). Interestingly, it can be observed that many solutions for dependability are based on information-flow security concepts. In [23], well-known concepts from the information-flow literature are introduced as building blocks to achieve dependability goals. In [24], non-interference-like definitions are used to express fault tolerance in terms of program semantics. On the other hand, one could argue that the security domain has been influenced by dependability principles as well. For instance, our enforcement is sound only if fault-tolerant hardware components are deployed for the code memory and the program counter.

**Language-Based Techniques for Fault-tolerance** The style of our work – in terms of the style of formalisation, the use of programming language techniques, and the level of semantic precision in the stated goals – is in the spirit of Perry et al’s fault-tolerant typed
assembly language [5]. Because we need to reason about security and not conventional fault tolerance, our semantic model of faults is necessarily much more involved than theirs, which is purely deterministic.

**Security and Transient Faults** We have not been the first ones to consider the implications of transient faults for security – Bar-El et al. [25] survey a variety of methods that can be used to induce transient faults on circuits that manipulate sensitive data. Xu et al. [26] study the effect of a single bit flip that strikes the opcode of x86 control flow instructions; their work states the non-modifiability of the source code, which is a crucial assumption in our framework. Bao et al. [27] illustrate several transient-fault based attacks on crypto-schemes. Their protection mechanisms either involve some form of replication or a more intensive usage of randomness (to increase the unpredictability of the result). In a similar scenario, Ciet et al. [28] show how the parameters of an elliptic curve crypto-system can be compromised by transient faults, and illustrate how a comparison mechanism is sufficient to prevent the attack from being successful. Canetti et al. [29] discuss security in the presence of transient faults for cryptographic protocol implementations where they focus on how random number generation is used in the code.

Our approach relies on fault-tolerant support for the program counter. While it seems a bit restrictive, there are fault-tolerant solutions for registers (e.g. [30,31]).

**5 Limitations**

The hardware model discussed here is similar to those introduced in [5,8] and, in common with many informal models of faults, has similar shortcomings: faults occurring at lower levels e.g. in combinatorial circuits, are not modelled. It has been argued [32] that these non-memory elements of a processor have much lower sensitivity to faults than state elements, but in our attacker model this does not say so much.

For timing channels discussed in Section 3.2 we make a large simplifying assumption: that the time to compute an instruction is constant. This ignores cache effects, so either implies a greatly simplified architecture, or a need for further refinements to the method to ensure that cache effects are mitigated by preloading or using techniques from [10].

The language we are able to compile is too small to be practical, containing neither functions nor arrays. The type system can perhaps be extended to handle such features, based on our understanding of other security type systems, and with the help of some additional fault-tolerant components (an extra fault-tolerant register should be sufficient to guarantee SS in the presence of dynamic pointers). However, the main challenge was in the non-trivial correctness proof (Appendix I). Clearly, mechanically verifiable proofs will facilitate extending our system to other features as well as verifying our confidence in the formal results.

**6 Conclusion**

We formalize security in presence of transient faults as Probabilistic Fault-Tolerant Non-Interference (PNI). We simplify it by reducing it to possibilistic framework (PoNI), and we show that another well-known security condition, called Strong Security [7], implies it. We explore a concrete instance of our formalism. We consider a simple RISC
architecture, in which the only fault-tolerant components are the program counter and the code memory. We define a type system that maps programs written in a toy while-language to the assembly language executed by our architecture and, at the same time, ensures that the produced code enjoys Strong Security (hence PNI).

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To avoid unintentional printing of the lengthy appendices of this submission, they have been removed from this version. The paper plus appendices can be obtained from arxiv.org.
A Full Definition of Fault-prone Systems with Environments

We formally account the composition of a Fault-prone System together with an error environment as follows.

Definition 10 (Fault-prone System with an Environment). Consider a fault-prone system \( \text{Sys} = \{S, \text{Act}, \rightarrow\} \), and an environment \( \text{Env} = (\text{Err}, \text{Fault}) \) where \( \text{Err} = \langle \mathcal{E}, \mathcal{L} \text{Act} \cup \{\tau\}, \leadsto \rangle \). The composition of \( \text{Sys} \) and \( \text{Env} \), defined as \( \text{Sys} \times \text{Env} = \langle S \times E, \langle \text{Act}, [0, 1] \rangle, \rightarrow \rangle \) where \( S \) is the set of all possible states for \( \text{Sys} \), defines a labelled transition system whose states are pairs of the system state and the environment state, and with transitions labelled with an action \( a \) and a probability \( p \), written \( a \rightarrow_p \). Transitions are determined according to the following rules:

\[
\exists S \xrightarrow{l} S' \quad \pi = \{L \mid L \in \mathcal{g}(F) \text{ and } \text{flip}(L, S) \xrightarrow{a} S'\}
\]

\[
p = \sum_{L \in \pi} \text{Fault}(E)(L) \cdot E'_{\text{low}(a)} \quad \langle S, E \rangle \xrightarrow{a}_p \langle S', E' \rangle
\]

\[
\exists S \xrightarrow{l} S' \quad \text{flip}(L, S) \not\rightarrow \quad p = \text{Fault}(E)(L) \quad E \xrightarrow{\tau} E'
\]

\[
\langle S, E \rangle \xrightarrow{\tau}_p \langle \text{flip}(L, S), E' \rangle
\]

In rule [Step] some locations in the fault-prone component of the system are flipped, then the execution can take place. In general, there might be several subsets of \( L \subseteq F \) such that \( \text{flip}(L, S) \) results in a state that (i) performs the same action \( a \) and (ii) performs a transition to the final state \( S' \). For this reason the probability associated to the rule corresponds to the sum of all probabilities associated to locations in the set \( \pi \).

We assume that a stuck configuration cannot be resumed. In rule [Stuck – 1] a flip on given subset of locations produces a stuck configuration with a certain probability. In rule [Stuck – 2] a stuck configuration remains as such regardless of any possible flip of the faulty component.

B Proof of Proposition 1

In order to prove Proposition 1 we prove an auxiliary result which ensures that our assignment of probability to \( n \)-sized runs is a probability distribution.

Proposition 2. Let \( \text{Sys} \) be a fault-prone system and \( \text{Env} \) an environment. Then \( \forall Z \in \text{Sys} \times \text{Env} \) and \( \forall n \geq 0 \sum_{r \in \text{run}_n(Z)} \text{Pr}(r) = 1 \).

Proof. We prove the statement by induction on \( n \).

Base case
When $n = 0$, the set $\text{run}_0(Z)$ contains only one element, the empty run, and its probability is 1.

**Inductive step**

Consider $n > 0$.

Any run $r \in \text{run}_n(Z)$ can be written as $r = Z \xrightarrow{a_0} p_0 Z_1 \ldots Z_{n-1} \xrightarrow{a_{n-1}} p_{n-1} Z_n = (Z \xrightarrow{a_0} p_0 Z_1 \ldots Z_{n-1}).(Z_{n-1} \xrightarrow{a_{n-1}} p_{n-1} Z_n)$, where $r' = Z \xrightarrow{a_0} p_0 Z_1 \ldots Z_{n-1}$ is a prefix of $r$ in $\text{run}_{n-1}(Z)$ with probability $\Pr(r') = p_{r'}$.

Consider the set $R_{r'} \subseteq \text{run}_n(Z)$ of all $n$-sized runs from $Z$ that has $r'$ as prefix. Since for all subsets in $\wp(F)$ there is a transition rule in $\text{Sys} \times Env$, we have $\sum_{r \in \text{run}_n(Z)} \Pr(r) = 1$. Hence we have that $\sum_{r \in R_{r'}} \Pr(r) = p_{r'}$ and we can conclude that $\sum_{r \in \text{run}_n(Z)} \Pr(r) = \sum_{r' \in \text{run}_{n-1}(Z)} \sum_{r \in R_{r'}} \Pr(r) = \sum_{r' \in \text{run}_{n-1}(Z)} p_{r'} = 1$, where the last result holds by inductive hypothesis.

**Proof (Proof of Proposition 1).** Recall that for any trace $t \in (LAct \cup \{\tau\})^n$, $\Pr_Z(t) = \sum_{r \in \text{run}_n(Z)} \Pr(r)$ where the last equality holds because of Proposition 2.

**C Full definitions of Augmented Fault-prone and Termination Transparent Systems**

An augmented fault-prone system is formally described as follows.

**Definition 11 (Augmented Fault-prone System).** Given a fault-prone system $\text{Sys} = \{\text{Loc}, \text{Act}, \rightarrow\}$ we define the augmented system $\text{Sys}^+ = \{\text{Loc}, \text{Act} \times \wp(F), \rightarrow\}$ by the following rules:

\[
\begin{align*}
\exists S \xrightarrow{L} S' & \quad \text{flip}(S, L) \xrightarrow{a} S' \quad L \subseteq F \\
S & \xrightarrow{L,a} S' \\
\exists S \xrightarrow{L} S' & \quad \text{flip}(S, L) \not\xrightarrow{\tau} \quad L \subseteq F \\
S & \xrightarrow{L,\tau} \text{flip}(S, L) \\
S & \not\xrightarrow{\tau} \quad L \subseteq F \\
S & \xrightarrow{L,\tau} S
\end{align*}
\]

A termination transparent system is formalized as follows.

**Definition 12 (Termination Transparent System).** For a fault-prone system $\text{Sys} = \{\text{Loc}, \text{Act}, \rightarrow\}$ we define its termination-transparent version as $\text{Sys}^* = \{\text{Loc}, \text{Act}, \rightarrow_{\infty}\}$ where $\rightarrow_{\infty}$ is defined with the following rules:

\[
\begin{align*}
S & \xrightarrow{a} S' \quad S \not\xrightarrow{\rightarrow_{\infty}} S' \quad S \not\rightarrow_{\infty} S
\end{align*}
\]

D Proof of Theorem

Before proving the theorem in question, we need to define some auxiliary concepts.

Definition 13 (Enabling set). Let \( Z = \langle S, E \rangle \) and \( Z' = \langle S', E' \rangle \) be a pair of states in \( \text{Sys} \times \text{Env} \) such that \( Z \xrightarrow{a} p Z' \). We say that \( L \) is an enabling set (of locations) for \( Z \xrightarrow{a} p Z' \) in the following cases:

- the transition is derived from rule [Step] and \( L \in \pi \);
- the transition is derived from rule [Stuck – 1] and \( L \) is the argument in \( \text{flip}(S, L) \);
- the transition is derived from rule [Stuck – 2].

Definition 14 (Enabling sequence). Let \( r \) be a run for \( \langle S_0, E_0 \rangle \) in \( \text{Sys} \times \text{Env} \) such that \( \langle S_0, E_0 \rangle \xrightarrow{a_0} p_0 \langle S_1, E_1 \rangle \xrightarrow{a_1} p_1 \ldots \xrightarrow{a_{n-1}} p_{n-1} \langle S_n, E_n \rangle \). The sequence \( L = L_0 \ldots L_{n-1} \) such that \( \forall 0 \leq i \leq n-1 \ L_i \) is an enabling set for \( \langle S_i, E_i \rangle \xrightarrow{a_i} p_i \). \( \langle S_{i+1}, E_{i+1} \rangle \) is called an enabling sequence for \( r \). We define the probability of \( L \) as \( \Pr_r(L) = \Pi_{0 \leq i \leq n-1} \text{Fault}(E_i)(L_i) \). We define the set of all enabling sequences for \( r \) as \( \phi(r) \).

We also need the following intermediate result.

Lemma 1. Let \( r \) be a run for \( Z \) in \( \text{Sys} \times \text{Env} \). Then we have that \( \Pr(\bar{r}) = \Sigma_{L \in \phi(\bar{r})} \Pr_{\bar{Z}}(L) \).

We can now prove Theorem

Proof (Proof of Theorem). Suppose \( P \) enjoys PoNI, we now show it enjoys PNI as well.

Consider a faulty system \( \text{Sys} \), an error environment \( \text{Env} = \langle \text{Err}, \text{Fault} \rangle \) and two states \( Z = \langle S, E \rangle \) and \( Z' = \langle S', E' \rangle \), for \( S, S' \in \text{Sys} \) and \( E \in \text{Err} \). Assume \( S_{\text{ProgLoc}} = S'_{\text{ProgLoc}} = P \) and \( S = L S' \).

We first show that for any \( n \geq 0 \) and for any trace \( t \in (L\text{Act} \cup \{\tau\})^n \), \( \Pr_Z(t) \leq \Pr_{Z'}(t) \), and hence by symmetry that \( \Pr_{Z'}(t) = \Pr_Z(t) \).

We prove the inequality by relating the probability of a trace to the probability determined by the enabling sequences that corresponds to it.

Consider a trace \( t \) such that \( \Pr_{Z'}(t) > 0 \). Let \( p_{Z'}(t) = \{ r \in \text{run}(Z) | \text{trace}(r) = t \} \) be the (nonempty) set of runs from \( Z \) whose trace is \( t \).

We have \( \Pr_{Z'}(t) = \Sigma_{r \in p_{Z'}(t)} \Pr(r) = \Sigma_{r \in p_{Z'}(t)} \Sigma_{L \in \phi(r)} \Pr_{\bar{Z}}(L) \), where the first equality holds by definition and the second one follows from Lemma

We now show that all enabling sequences for \( Z \) are also enabling sequences for \( Z' \). Let \( \kappa_Z = \bigcup_{r \in p_{Z'}(t)} \phi(r) \) be the set of all enabling sequences for \( t \) in \( Z \) and let \( L \) be an enabling sequence for a run \( r \in \text{run}(Z) \). Since \( P \) is PoNI, there must be a run \( r' \) from \( Z' \) such that \( L \) is an enabling sequence for \( r' \), and \( \text{trace}(r') = t \). Hence, for the set \( \kappa_{Z'} = \bigcup_{r \in p_{Z'}(t)} \phi(r') \) we have that \( \kappa_Z \subseteq \kappa_{Z'} \).

Also, observes that for any \( L \in \kappa_Z \), \( \Pr_{Z'}(L) = \Pr_{Z'}(\bar{L}) \), since \( \text{trace}(u) = \text{trace}(u') \).

Then \( \Pr_{Z'}(t) = \Sigma_{L \in \kappa_Z} \Pr_{Z'}(L) \leq \Sigma_{L \in \kappa_Z} \Pr_{Z'}(\bar{L}) = \Pr_{Z'}(t) \).

We continue by showing that PNI implies PoNI by proving the contrapositive. Suppose that \( P \) is not PoNI. Then there must exist two states \( S, S' \) such that \( S_{\text{ProgLoc}} = S'_{\text{ProgLoc}} = P \) and \( S = L S' \), together with a location set \( \lambda \in g(F) \).
a trace \( t = L_0, a_0, \ldots, L_j, a_j \) and \( a, b \in L \) \( \cup \{ \tau \} \) such that \( a \neq b \), \( S \xrightarrow{t, \lambda, a} \) and \( S' \xrightarrow{t, \lambda, b} \).

Define an error environment \( \text{Env} = (\text{Err}, \text{Fault}) \) such that \( \text{Err} = \langle \{L_i | L_i \in t \} \cup \{\lambda\}, L \cup \{\tau\}, \{L_i \rightharpoonup a \mid 0 \leq i \leq j - 1 \text{ and } a \in L \} \cup \{L_j \rightharpoonup \lambda \mid a \in L \} \rangle \) and \( \text{Fault}(\lambda)(\lambda) = \text{Fault}(L)(L) = 1 \). Essentially, \( \text{Env} \) deterministically traverses all flipped locations included in \( t \), and terminates in \( \lambda \), regardless of the actions performed by the fault-prone system.

Consider now the composition of \( \text{Sys} \) with \( \text{Env} \) and let \( Z = \langle S, L_0 \rangle \) and \( Z' = \langle S', L_0 \rangle \). Let \( t' = a_0, \ldots, a_j, a \) be a trace in \( (L \cup \{\tau\})^* \) obtained from \( t \) by (i) stripping flipped locations and (ii) appending the action \( a \) at the end. Then there exists a unique run \( r \in \text{run}(Z) \) such that \( \text{trace}(r) = t' \) and \( \text{Pr}(r) = \text{Pr}(Z)(t') \neq 1 \) \( \neq \text{Pr}(Z')(t') = 0 \). The inequality between \( \text{Pr}(Z)(t') \) and \( \text{Pr}(Z')(t') \) follows from the hypothesis of \( P \) not being PoNI, which implies that there is no \( r' \in \text{run}(Z') \) such that \( \text{trace}(r') = t' \).

### E Proof of Theorem 2

Rather than showing that Strong Security implies PoNI directly, we take an indirect approach.

First we characterize the semantics of a termination-transparent system in terms of “transition traces”, borrowing ideas from [33]. Then we define an ad-hoc security property, called Strong Trace-based Security within this semantic model. We finally show that Strong Security implies Strong Trace-based Security, which in turn implies PoNI.

For improving readability we represent \( S \mid_{\text{LowLoc}; \text{HighLoc}} \) as \( M \), the data component, therefore the state of a fault-prone system is represented as \( (P, M) \). We adopt the concept of low equality between states to data components by saying that \( M =_L M' \) if \( M \mid_{\text{LowLoc}} = M' \mid_{\text{LowLoc}} \).

**Definition 15 (Transition trace semantics).** Let \( \text{Sys} \) be a fault-prone system and let \( \text{Sys}^\infty = \{ \text{Loc}, \text{Act}, \rightarrow \} \) be its termination-transparent version. The \( n \)-step transition-trace semantic of a program component \( P_0 \) is defined as the set \( T_n(P_0) \), such that \( T_n(P_0) = \{(M_0, a_0, M_0'), (M_1, a_1, M_1') \ldots (M_{n-1}, a_{n-1}, M_{n-1}) \mid \forall 0 \leq i \leq n - 1 (P_i, M_i) \rightharpoonup \lambda, (P_{i+1, M_i}') \} \). The transition trace semantics of \( P_0 \) is defined as \( T(P_0) = \cup_n T_n(P_0) \).

In the transition trace model, the semantics of a program component \( P \) is built in sequences of steps. In particular, at any step, the program component is executed on a certain data component, then the data component is modified and the execution is restarted. Observe that the model is very similar to the way a fault-prone system and an error environment interact with each other. This is even more clear when viewing the modification of the data component as the effect of its interaction with the error environment.

We say that two transition traces

\[
\begin{align*}
t & = (M_0, a_0, M_0'), (M_1, a_1, M_1') \ldots (M_{n-1}, a_{n-1}, M_{n-1}) \\
t' & = (N_0, b_0, N_0'), (N_1, b_1, N_1') \ldots (N_{n-1}, b_{n-1}, N_{n-1})
\end{align*}
\]
are input low-equivalent, written \( t =_I t' \), if \( \forall 0 \leq i < n, M_i =_L N_i \), whereas they are output low-equivalent, written \( t =_O t' \) if \( \forall 0 \leq i < n, \text{low}(a_i) = \text{low}(b_i) \) and \( M'_i =_L N'_i \).

**Definition 16 (Strong Trace-based Security (StbS)).** We say that a program component \( P \) is \( n \)-Strong Trace-based Secure if for any two transition traces \( t, t' \in \mathcal{T}_n(P) \), if \( t =_I t' \) then \( t =_O t' \). We say that a program component \( P \) is Strong Trace-based Secure if it is \( n \)-Strong Trace-based Secure for any \( n \in \mathbb{N} \).

We now show how to use the notion of Strong Trace-based Security to bridge the gap between Strong Security and PoNI. We show that Strong Security implies Strong Trace-based Security first.

**Lemma 2 (SS implies StbS).** Let \( P \) be a program component. If \( P \) enjoys SS then \( P \) enjoys StbS.

**Proof.** We define some notation first. We refer to the \( i \)-th triple in a transition trace \( t \) as \( t_i \), and to the program component used to evaluate it as \( P_{t_i} \) (for a trace \( t = (M_0, a_0, M'_0), (M_1, a_1, M'_1), \ldots (M_{n-1}, a_{n-1}, M'_{n-1}) \) we therefore say that the \( i \)-th triple \((M_i, a_i, M'_i)\) is induced by \( (P_{t_i}, M_i) \xrightarrow{\alpha \to \infty} (P_{t_{i+1}}, M'_{i+1}) \).

Consider a program component \( P \) and two \( n \)-transition traces

\[
    t = (M_0, a_0, M'_0), (M_1, a_1, M'_1), \ldots (M_{n-1}, a_{n-1}, M'_{n-1})
\]

and

\[
    t' = (N_0, b_0, N'_0), (N_1, b_1, N'_1), \ldots (N_{n-1}, b_{n-1}, N'_{n-1})
\]

in \( \mathcal{T}_n(P) \).

We want to show that if \( P \) enjoys SS and \( t =_I t' \), then \( t =_O t' \).

Starting from a strong bisimulation \( R \) for \((P, P)\), the idea of the proof is to infer properties of \( t' \) by unwinding \( R \) for \( n \)-steps. We proceed by showing that for all \( 0 \leq i < n \) we have that \((P_{t_i}, P'_{t_i}) \in R \). For \( i = 0 \), \( P_{t_0} = P_{t_0} = P \) and \((P, P) \in R \). If \((P_{t_i}, P'_{t_i}) \in R \), then by definition of \( R \) we have that if \((P_{t_i}, M_i) \xrightarrow{\alpha \to \infty} (P_{t_{i+1}}, M'_{i+1}) \) and \( M_i =_L N_i \), then \((P_{t_i}', N_i) \xrightarrow{\alpha \to \infty} (P_{t_{i+1}}', N'_{i+1}) \) and \((P_{t_{i+1}}', P'_{t_{i+1}}) \in R \). But this is the case for \( t \) and \( t' \), since \( t =_I t' \).

The statement of the lemma is therefore proved by recalling that two program components \( P \) and \( P' \) in a strong bisimulation \( R \) are such that their executions from low equivalent data result in (i) low equivalent data and (ii) low equivalent actions.

We now discuss the relation between Strong Trace-based Security and PoNI. In general it is not true that Strong Trace-based Security is stronger than PoNI. Consider, for example, the class of systems such that \( \text{ProgLoc} \not\subseteq T \). Due to transient faults, a completely innocuous program component can be converted into a harmful one, even when it enjoys Strong Trace-based Security.

Surprisingly, this is not the only constraint that we must impose to the systems of our interest. We must also require that they show a uniform behavior for termination, as shown in the following example.
Example 2. Consider the fault-prone system in Figure 11. For each state $S = \{ b_i \rightarrow \{0, 1\} | i \in \{0, 1, 2\} \}$ we consider $ProgLoc = \{ b_0 \}$, $HighLoc = \{ b_1 \}$ and $LowLoc = \{ b_2 \}$. We also assume that the states where $P$ is 1 are stuck and therefore are omitted.

The system is Strongly Trace-based Secure: all states are either stuck or perform a transition on themselves, therefore low equivalence is preserved. The only difference in the output behavior is observable between $S_0$ and $S_2$: the former is stuck, the latter perform a $\tau$ transition. Nonetheless they result indistinguishable in the termination transparent version of the system. However, the system is not PoNI. In fact, if a bit flip on $b_2$ can transform $S_2$ into $S_3$ so we have $S_0 \stackrel{(b_2), \tau}{\longrightarrow} S_2 \stackrel{(b_2), a}{\longrightarrow}$.

From now onwards we focus our attention on “standard fault-prone” systems. For such systems, we have that the whole program component is fault-tolerant (formally $ProgLoc \subseteq T$) and it is either stuck or active, regardless of the data component.

Definition 17 (Standard fault-prone systems). A fault-prone system is called standard if $ProgLoc \subseteq T$ and, for all $P$, either for any data component $M$ there exists an action $l$ such that $(P, M) \xrightarrow{l}$ or for any data component $M$ the system is stuck, namely $(P, M) \nRightarrow$.

For the class of systems of our interest, Strong Trace-based Security is indeed stronger than PoNI.

Lemma 3 (Strong Trace-based Security implies PoNI). Let $P$ be a program component in a standard fault-prone system $Sys$. If $P$ enjoys StbS then $P$ enjoys PoNI.

Proof. We prove this lemma by showing the contrapositive. Suppose that $P$ is not PoNI. Then there must be two states $S = (P, M_0)$ and $S' = (P, N_0)$ in the augmented version of a fault-prone system $Sys$ such that $M_0 \equiv_L N_0$, and two runs that exit from them whose corresponding traces violate the security condition. Let

$$r = (P, M_0) \xrightarrow{L_0, a_0} (P, M_1) \ldots (P, M_{j-1}) \xrightarrow{L_{j-1}, a_{j-1}} (P, M_j) \xrightarrow{L, a}$$

and

$$r' = (P, N_0) \xrightarrow{L_0, b_0} (P, N_1) \ldots (P, N_{j-1}) \xrightarrow{L_{j-1}, b_{j-1}} (P, N_j) \xrightarrow{L, b}$$
be the runs in question, such that \( \forall 0 \leq i < j \), \( \text{low}(a_i) = \text{low}(b_i) \) but \( \text{low}(a) \neq \text{low}(b) \).

Before continuing, we observe that, in the initial configuration, \( P \) cannot be stuck. Also, it must be that at most one run between \( r \) and \( r' \) contains a sequence of stuck configurations. Both conditions are necessary to have \( \text{low}(a) \neq \text{low}(b) \).

We now show that it is possible to build two transition traces for \( P \) that violate Strong Trace-based Security. Recall that the flip function can be applied only to locations in \( F \), and that we consider systems whose faulty locations are restricted to the data component \( (F \subseteq \text{LowLoc} \cup \text{HighLoc}) \). Hence, when \( S = (P, M) \), we write \( \text{flip}(S, L) \) as \( (P, \text{flip}(M, L)) \), and we focus on the data component \( \text{flip}(M, L) \) when necessary.

We proceed by distinguishing two cases, depending on whether or not a stuck configuration is traversed by \( r \) (equivalently \( r' \)).

**Case 1**: no stuck configurations are traversed in either \( r \) or \( r' \).

Consider the following two transition traces

\[
t = (\text{flip}(M_0, L_0), a_0, M_1), (\text{flip}(M_1, L_1), a_1, M_2) \ldots (\text{flip}(M_j, L), a, M_{j+1})
\]

and

\[
t' = (\text{flip}(N_0, L_0), b_0, N_1), (\text{flip}(N_1, L_1), b_1, N_2) \ldots (\text{flip}(N_j, L), b, N_{j+1})
\]

Since \( r \) does not traverse stuck configurations, all transitions are computed by an application of the rule [Step]. This means that for any transition we have \( (P_i, M_i) \xrightarrow{\begin{array}{c} \text{flip} \\ \text{flip} \end{array}} (P_{i+1}, M_{i+1}) \) if \( (P_i, \text{flip}(M_i, L_i)) \xrightarrow{\begin{array}{c} \text{flip} \\ \text{flip} \end{array}} (P_{i+1}, M_{i+1}) \). Hence \( t \) is in \( T(P) \). By applying a similar argument for \( r' \), we conclude that \( t' \) is in \( T(P) \) as well.

Observe that flip preserves low equivalence between data components (if \( M_i =_L N_i \), then for all set of locations \( L \) it is true that \( \text{flip}(M_i, L) =_L \text{flip}(N_i, L) \)). Considering that \( M_0 =_L N_0 \), there are two possible cases. Either there exists \( k \), such that \( 0 \leq k < j \) and \( (\text{flip}(M_k, L_k), a_k, M_{k+1}) \) and \( (\text{flip}(N_k, L_k), b_k, N_{k+1}) \) and \( M_{k+1} \neq L N_{k+1} \), or \( \forall k \leq k < j \) \( M_k =_L N_k \) and \( \text{low}(a) \neq \text{low}(b) \). In both cases Strong Trace-based Security is violated.

**Case 2**: there is a stuck configuration in \( r \).

We consider the case in which a configuration in \( r \) is stuck. The symmetric case for \( r' \) is similar, and it is omitted.

Since \( S_{\text{sys}} \) is a “standard fault-prone” system, the rule [Stuck – 2] cannot be applied in the first step. Let \( 1 \leq w \leq j \) be the index of the first stuck state \( (P_w, M_w) \) in \( r \). Consider the following transition traces

\[
t = (\text{flip}(M_0, L_0), a_0, M_1), \ldots, (\text{flip}(M_{w-1}, L_{w-1}), a_w, M_w),
\]

\[
(\text{flip}(N_w, L_w), \tau, \text{flip}(N_w, L_w)), \ldots, (\text{flip}(N_j, L), \tau, \text{flip}(N_j, L))
\]

\[
t' = (\text{flip}(N_0, L_0), b_0, N_1), \ldots, (\text{flip}(N_{w-1}, L_{w-1}), b_{w-1}, N_w),
\]

\[
(\text{flip}(N_w, L_w), b_w, N_{w+1}), \ldots, (\text{flip}(N_j, L), b, N_{j+1})
\]

As observed in the previous case, since flip preserves low equivalence of data components, there are the following cases to be considered. Either there exists \( k \) such that \( 0 \leq k < w \) and \( (\text{flip}(M_k, L_k), a_k, M_{k+1}) \) and \( (\text{flip}(N_k, L_k), b_k, N_{k+1}) \) and \( M_{k+1} \neq L \)
Load  
\[ P(pc) = \text{load } \tau p \]  
\[ \langle P, pc, R, M \rangle \xrightarrow{\tau} \langle P, pc^+, R[\tau \mapsto M(p)], M \rangle \]  
\[ P(pc) = \text{store } p \tau \]  
\[ \langle P, pc, R, M \rangle \xrightarrow{\tau} \langle P, pc^+, R, M[p \mapsto R(r)] \rangle \]  
\[ P(pc) = \text{jmp } l \]  
\[ \langle P, pc, R, M \rangle \xrightarrow{\tau} \langle P, pc, R, M \rangle \]  
\[ P(pc) = \text{jz } l \tau \]  
\[ \langle P, pc, R, M \rangle \xrightarrow{\tau} \langle P, pc^+, R, M \rangle \]  
\[ P(pc) = \text{nop } \]  
\[ \langle P, pc, R, M \rangle \xrightarrow{\tau} \langle P, pc^+, R, M \rangle \]  
\[ P(pc) = \text{movek } r n \]  
\[ \langle P, pc, R, M \rangle \xrightarrow{\tau} \langle P, pc^+, R[r \mapsto n], M \rangle \]  
\[ P(pc) = \text{mover } r r' \]  
\[ \langle P, pc, R, M \rangle \xrightarrow{\tau} \langle P, pc^+, R[r \mapsto R(r')], M \rangle \]  
\[ P(pc) = \text{op } r r' \]  
\[ \langle P, pc, R, M \rangle \xrightarrow{\tau} \langle P, pc^+, R[r \mapsto R(r') \text{ op } R(r')], M \rangle \]  
\[ P(pc) = \text{out } ch r \text{ Reg}(r) = n \]  
\[ \langle P, pc, R, M \rangle \xrightarrow{\tau} \langle P, pc^+, R, M \rangle \]  

**Fig. 12.** RISC instructions semantics

\( N_{k+1} \), or there exists \( k \) such that \( w \leq k < j \) and \( \text{flip}(N_k, L_k), \tau, \text{flip}(N_k, L_k) \) and \( \text{flip}(N_k, L_k), b_k, N_{k+1} \) and \( \text{flip}(N_k, L_k) \neq L N_{k+1}, \) or \( \tau \neq \text{low}(b) \). In all cases Strong Trace-based Security is violated.

**Proof (Proof of Theorem 2).** Directly obtained by applying Lemma 2 and Lemma 3.

**F  RISC instructions semantics**

Figure 12 formalizes the semantics of the RISC language.

**G  Typing rule for expressions**

Figure 13 shows all the (abstract) rules for the compilation of while expressions into RISC code.

**H  Typing rule for atomic statements**

All rules for typing atomic statements are presented in Figure 14.
I Proof of Theorem 3

The type system presented in Section 3.2 is an abstraction of the method that we use to enforce Strong Security over RISC programs. In this section we describe such method, together with all the necessary results to prove the Theorem 3.

We begin (Section I.1) by introducing the $i$-while language, an intermediate representation that bridges the translation between while and RISC programs. We also define the type system, whose abstraction is presented in Section 3.2, that translates while programs into $i$-while programs. For a type correct while program, the type system ensures that (i) it is strongly secure (Proposition 3) and (ii) is mapped to a strongly secure $i$-while program (Proposition 6).

In Section I.2 we define a strategy for translating $i$-while programs into RISC programs. The strategy ensures that the target RISC program is semantically equivalent to the source $i$-while program (Proposition 7), hence Strong Security can be inferred for the RISC program via Strong Security enjoyed by the source $i$-while program.

I.1 From while programs to $i$-while programs

The syntax of $i$-while programs is presented in Figure 15.

$i$-while programs are a subclass of while programs that take into account features of the RISC architecture. The first feature is that an $i$-while program distin-
The distinction equips the i-while language with the concept of "register" that is used in the target machine. The second feature is a more restrictive syntax for conditionals and loops, that enables a simpler translation between i-while and RISC programs. Specifically, both while and if commands in i-while syntax require the guard to be a register variable, and require the branches (in the case of if) or the loop body (in the case of while) to be terminated by a skip command.

\[
\begin{align*}
D & ::= \text{skip} \mid x := r \mid r := F \mid D_1; D_2 \mid \text{out} \ ch \ r \\
\text{while } r \ do \{D; \text{skip}\} \mid \text{if } r \ then \{D_1; \text{skip}\} \ else \{D_2; \text{skip}\}
\end{align*}
\]

\[F ::= k \in \mathbb{N} \mid r \in \text{Reg} \mid x \in \text{Var} \mid r_1 \ op \ r_2\]

\[\text{ch} ::= \text{low} \mid \text{high}\]

Fig. 15. i-while programs syntax

This distinction equips the i-while language with the concept of "register" that is used in the target machine. The second feature is a more restrictive syntax for conditionals and loops, that enables a simpler translation between i-while and RISC programs. Specifically, both while and if commands in i-while syntax require the guard to be a register variable, and require the branches (in the case of if) or the loop body (in the case of while) to be terminated by a skip command.

\[
\begin{align*}
\Phi, A \vdash^{\text{Reg}}_\text{Var} k & \leftrightarrow \{r := k\}, (\text{level}(r), 1), r, \Phi[r \not\in]
\end{align*}
\]

\[
\begin{align*}
x & \in \text{Var} \quad r \in \text{Reg} \quad [r \leftrightarrow x] \in \Phi
\end{align*}
\]

\[
\begin{align*}
\Phi, A \vdash^{\text{Reg}}_\text{Var} x & \leftrightarrow \{\ast\}, (\text{level}(r), 0), r, \Phi
\end{align*}
\]

\[
\begin{align*}
x & \in \text{Var} \quad r, r' \in \text{Reg}
\end{align*}
\]

\[
\begin{align*}
\Phi, A \vdash^{\text{Reg}}_\text{Var} & \{D_1\}, (\lambda, n_1), r, \Phi_1
\end{align*}
\]

\[
\begin{align*}
\Phi, A \vdash^{\text{Reg}}_\text{Var} & \{D_2\}, (\lambda, n_2), r', \Phi_2
\end{align*}
\]

\[
\begin{align*}
\Phi, A \vdash^{\text{Reg}}_\text{Var} & \{D_1; D_2; r := r op r'\}, (\lambda, n_1 + n_2 + 1), r, \Phi_2[r \not\in]
\end{align*}
\]

Fig. 16. Type system for while expressions

In Figures 16, 17 and 18 the type system that performs both the translation of a while program \(C\) into an i-while program \(D\) and the security analysis on \(C\) is described. We now discuss these aspects in detail.

\[
\begin{align*}
\Phi \vdash^{\text{Reg}}_\text{Var} \text{skip} & \leftrightarrow \{\text{skip}\}, (\text{Wr} \ H, \text{Trm} \ (1, 1)), \Phi
\end{align*}
\]

\[
\begin{align*}
x & \in \text{Var} \quad r \in \text{Reg} \quad \Phi, \{\} \vdash^{\text{Reg}}_\text{Var} E \leftrightarrow \{D\}, (\text{level}(x), n), r, \Phi'
\end{align*}
\]

\[
\begin{align*}
\Phi \vdash^{\text{Reg}}_\text{Var} x := E & \leftrightarrow \{D; x := r\}, \text{level}(x) = H?\langle \text{Wr} \ H, \text{Trm} \ (1, n + 1) \rangle : \langle \text{Wr} \ L, \text{Trm} \ L \rangle, \Phi'[r \not\in]
\end{align*}
\]

\[
\begin{align*}
r & \in \text{Reg} \quad \Phi, \{\} \vdash^{\text{Reg}}_\text{Var} E \leftrightarrow \{D\}, (\text{level}(\text{ch}), n), r, \Phi'
\end{align*}
\]

\[
\begin{align*}
\Phi \vdash^{\text{Reg}}_\text{Var} \text{out} \ ch \ E & \leftrightarrow \{D; \text{out} \ ch \ r\}, \text{level}(\text{ch}) = H?\langle \text{Wr} \ H, \text{Trm} \ (1, n + 1) \rangle : \langle \text{Wr} \ L, \text{Trm} \ L \rangle, \Phi'
\end{align*}
\]

Fig. 17. Type system for atomic while statements
\[
\begin{aligned}
\Phi \vdash_{\text{Reg}} \varnothing &\rightarrow \{ D \}, (w_1, t_1), \Phi_1 \\
\Phi_1 \vdash_{\text{Reg}} \varnothing &\rightarrow \{ D' \}, (w_2, t_2), \Phi_2 \\
\Phi \vdash_{\text{Var}} C &\rightarrow \{ D; D' \}, (w_1 \cup w_2, t_1 \cup t_2), \Phi_2
\end{aligned}
\]

\[t_1 = \text{Trm} \Rightarrow w_2 = \text{Wr} \]

\[
\begin{aligned}
\Phi \vdash_{\text{Reg}} C; C' &\rightarrow \{ D; D' \}, (w_1 \cup w_2, t_1 \cup t_2), \Phi_2
\end{aligned}
\]

\[
\begin{aligned}
r \in \text{Reg} \\
\Phi_1 \vdash_{\text{Reg}} C_1 &\rightarrow \{ D_1 \}, (w_1, t_1), \Phi_2 \\
\Phi_1 \vdash_{\text{Reg}} C_2 &\rightarrow \{ D_2 \}, (w_2, t_2), \Phi_3 \\
D'_1 = D_1; \text{skip} &
\text{write}(\lambda) \sqsubseteq w_1,  \\
\Phi_F = \Phi_2 \cap \Phi_3
\end{aligned}
\]

\[
\begin{aligned}
\Phi \vdash_{\text{Var}} C &\rightarrow \{ D_0 \}, (d_0); \\
\Phi &\rightarrow \{ \text{term}(\lambda) \sqsubseteq \lambda \}
\end{aligned}
\]

\[
\begin{aligned}
r \in \text{Reg} \\
\Phi_1 \vdash_{\text{Reg}} E &\rightarrow \{ D_1 \}, (H, \text{Trm} (m, n)), \Phi_2 \\
\Phi_1 \vdash_{\text{Reg}} C_1 &\rightarrow \{ D_2 \}, (\text{Trm} (m, n)), \Phi_3 \\
D'_1 = D_1; \text{skip} &\rightarrow \{ \text{wr} \}
\Phi_F = \Phi_2 \cap \Phi_3
\end{aligned}
\]

\[
\begin{aligned}
\Phi \vdash_{\text{Var}} C &\rightarrow \{ D_0 \}, (d_0); \\
\Phi &\rightarrow \{ \text{term}(\lambda) \sqsubseteq \lambda \}
\end{aligned}
\]

\[
\begin{aligned}
\lambda = \text{level}(x) = \text{level}(r) \\
\Phi' = \Phi[r \rightarrow x] \\
\Phi_B \vdash \Phi' \\
\Phi_B \vdash \Phi_E[r \rightarrow x]
\end{aligned}
\]

\[
\begin{aligned}
\lambda = \text{level}(x) = \text{level}(r) \\
\Phi \vdash_{\text{Reg}} \text{while } x \rightarrow C &\rightarrow \{ D_0 \}, \text{while } r \rightarrow \{ D; D_0; \text{skip} \}; \\
\Phi_B &\rightarrow \{ \text{term}(\lambda) \sqsubseteq \lambda \}
\end{aligned}
\]

\[
\begin{aligned}
\Phi &\rightarrow \{ \text{term}(\lambda) \sqsubseteq \lambda \}
\end{aligned}
\]

**Fig. 18.** Type system for non-atomic **while** statements

**Type System: Translation** The type system described in Figures 16, 17 and 18 converts a **while** program into an i-**while** program.

In general, observe that none of the rules involve labels, since these are no longer part of the target language. However, the rules still require that a register record is carried along the compilation. We assume, similarly to what has been done in Section 3.2, that there is a register record function \( \Phi \in \text{Reg} \rightarrow (\{ R, W \} \times \text{Var}) \) which not only associates variables to registers, but also records the modality (read/write) in which the association was created. Notice that in this context \( \text{Reg} \) are just variables and have not direct hardware interpretation. Finally, observe that the rules are parametrized in the set of pure and register variables (\( \text{Var} \) and \( \text{Reg} \)). Implementing our translation strategy does not require this parametrization, since the set of registers that are used in the RISC machine is known beforehand. However it turns out to be a useful tool for implementing our proof strategy: first we show that a type-correct **while** program \( C \) is strongly secure, then we show that the correspondent i-**while** program \( D \) is strongly secure.
by retyping it under a different set of register variables, that are solely used for stating
the security property of D (all the details are formalized in Proposition 6).

The rules in Figure 16 that formalize the compilation of expressions, are very similar
to the rules in Figure 13 beside the fact that operations over registers and memory
locations are replaced by assignments between pure and register variables. In order to
represent a compilation that produces no code (see rule \([V \rightarrow \text{cached}]\)) we explicitly
extend the syntax of i-while programs (i.e. while programs) with • the empty state-
ment, that represents the i-while correspondent of the \(\epsilon_I\) statement used for RISC
programs. However, since • has no semantic meaning, we assume that the composi-
tion operator ; strips the occurrences of • when composing commands together. This
is formalized by defining structural equivalence to be the least congruence relation \(\equiv\)
between programs such that •.C \equiv C: •.C = C.

Commands translation, implemented by the rules in Figures 17 and 18 are also similar
to the rules in Figures 14,9 and 10 hence we only focus on the main differences.

The compilation of if E then Ci else Ce performed by the [if − any] rule produces
the code \(D_g\) for E first, that corresponds to evaluating E in register variable r. Then, subprograms \(D_t\) and \(D_c\) are obtained from \(C_t\) and \(C_c\) respectively. In order
to comply with the i-while syntax, a skip instruction is appended to both \(D_t\) and \(D_c\), obtaining respectively programs \(D_t'\) and \(D_c'\) that are used in the rule output
\(D_g\); if \(r\) then \(D_t'\) else \(D_c'\). In the rule [if − H] we follow a padding strategy which is
similar to the one used for RISC programs: we say skip\(^n\) is a sequence of \(n\) skip com-
mands when \(n > 0\), whereas it is • for \(n \leq 0\). In the compilation of a while x do C
command, we deploy the fragment of code \(D_0\) to establish the invariant property on the
register record. Moreover, we append skip to \(D: D_0\) in order to make the code compliant
with i-while syntax.

Type System: Security analysis In order to reason about security of while programs,
we distinguish between public and secret data. In particular, as we did in Section 3.2
we assume that variables are labeled in a way that does not change during the execution
and it is determined by the function level \(\in \text{Reg} \cup \text{Var} \rightarrow \{L,H\}\).

The security information calculated by the type system is essentially the same one
presented for the type system in Section 3.2 A type-correct while expression is decor-
ad with a label \((\lambda, n)\), which indicate the security level of the register variables that
are used to evaluate E and the number of i-while steps that are required to evaluate
E, exactly as in Figure 13 A type-correct while program is associated to a label \((w,t)\)
describing its write effect (label w) and timing behavior (label t). Write labels are taken
from the two-element set \(\{\text{Wr}H, \text{Wr}L\}\), with partial ordering \(\text{Wr}H \sqsubseteq \text{Wr}L\), and have the same semantics introduced in Section 3.2. The timing label t is an element from the
partial order \(\mathcal{L}_t\) which is described in Figure 19 (notice that, for improving readability,
the order relation is just sketched). Compared to the partial order presented in Figure
7 we define a refined annotation for programs that are certainly terminating in a finite
number of steps. In particular we label such programs with values Trm \((m,n)\), which
specifies that (i) the source while program terminates in m steps and (ii) the compiled
i-while program terminates in \(n\) steps, no matter which values the variables

---

\(^4\) A congruence relation, in this context, is an equivalence relation on commands that is closed
under the syntactic constructors of the language.
are set to. As for rules parametrization, this feature is a tool for our proof strategy. In fact, the type system has to track timing behavior of both the original program and its compiled version because it might happen that the timing behavior is modified in the recompilation of a compiled program.

\[
\begin{array}{c}
\text{Trm } H \\
\text{Trm } L
\end{array}
\]

\[
\text{Trm } (m, 0) \quad \text{Trm } (m, 1) \quad \cdots \quad \text{Trm } (m, n) \quad \cdots
\]

\[
\text{Trm } (1, 0) \quad \text{Trm } (1, 1) \quad \cdots \quad \text{Trm } (1, n) \quad \cdots
\]

\[
\text{Trm } (0, 0) \quad \text{Trm } (0, 1) \quad \cdots \quad \text{Trm } (0, n) \quad \cdots
\]

\[
t_1 \sqcup t_2 =
\begin{cases}
\text{Trm } L \text{ if } \forall i \in \{1, 2\} t_i \subseteq \text{Trm } L \\
\text{Trm } H \text{ otherwise}
\end{cases}
\]

\[
t_1 \uplus t_2 =
\begin{cases}
\text{Trm } (m_1 + m_2, n_1 + n_2) \text{ if } \forall i \in \{1, 2\} t_i = \text{Trm } (m_i, n_i) \\
t_1 \sqcup t_2 \text{ otherwise}
\end{cases}
\]

![Fig. 19. Termination partial order](image)

We now explain how security annotations are computed by the type system in Figures 17 and 18.

The skip commands takes exactly one step to be completed in both its original and its compiled version. Moreover, it does not modify the value of any of the variables used in the program. For this reason, [skip] rule assigns \(\langle \text{Wr } H, \text{Trm } (1, 1) \rangle\) as security annotation for skip.

The security annotation for an assignment command \(x := E\) depends on the security level of the variable \(x\). If level(\(x\)) = H, we require that all instructions used to evaluate the expression perform write actions solely on H variables. This, in turn, requires that \(E\) has an associated type \(\langle H, n \rangle\), which not only specifies the information about written variables, but also states that \(E\) has been compiled into \(n\) i-while instructions. Hence, for level(\(x\)) = H, rule \([:=]\) assigns \(\langle \text{Wr } H, \text{Trm } (1, n + 1) \rangle\) to \(x := E\), since a single instruction is mapped to \(n + 1\) i-while instructions (\(n\) instructions correspond to \(E\), the last instruction \(x := r\) counts for one). If level(\(x\)) = L, then we require that written variables are at security level L\(^5\), beside making sure that no content from H variables is used. In this case the final type for \(x := E\) is \(\langle \text{Wr } L, \text{Trm } L \rangle\).

The rule \([\text{out}]\) follows a similar argument, with the role of \(x\) taken by the channel \(ch\).

The rule \([\vdash]\) requires that whenever a component \(C_1\) has a timing behavior described by Trm \(H\), the following component \(C_2\) induces a \(\text{Wr } H\) write effects, in order to avoid timing channel leaks. The annotation computed by rule \([\vdash]\) considers the least upper

\(^5\) In fact security could be established in a more liberal setting, however this strictness simplifies arguments in proofs.
bound of the writing effects of $C_1$ and $C_2$, and uses an extended least upper bound operator $\sqcup$ (cf. Figure 19).

The rule $[\text{if} - \text{any}]$ prevents implicit flows from happening in the program by applying the same strategy presented for the type system in Figure 9. In particular, the security label $\lambda$ of an expression is translated into a write effect by the function $\text{write}$ (cf. Section 3.2), and write effects of both branches are expected to be lower than $\text{write}(\lambda)$. The resulting security annotation for the if $E$ then $C_1$ else $C_e$ command is computed in terms of the least upper bound of the security annotations for $E$, $C_1$ and $C_e$. In particular, the write effect $\text{write}(\lambda) \sqcup w_1 \sqcup w_2$ corresponds to the least upper bound of all write effects, whereas the time behavior $\text{term}(\lambda) \sqcup t_1 \sqcup t_2$ is determined from the timing behavior of branches, together with the corresponding time behavior of the guard, according to the function term (where term is defined in Section 3.2). Notice that the exact label for termination would be $\text{Trm}(0, n_g) \sqcup \text{term}(\lambda) \sqcup (t_1 \sqcup \text{Trm}(0, 1)) \sqcup (t_2 \sqcup \text{Trm}(0, 1))$, because of the code $D_g$ that is executed at the loop entrance and the skip commands that are appended at the end of $D_1$ and $D_e$. However, we can omit this information because term always returns a label in $\{\text{Trm} L, \text{Trm} H\}$, hence the exact number of steps for $D_g$ and skip is irrelevant.

When it is known that the if statement involves only write actions on $H$ variables, the timing behavior can be computed more accurately, as for the type system in Figure 9. In particular, as shown by rule $[\text{if} - \text{H}]$, if $C_1$ and $C_e$ are associated to a security type $\langle \text{Wr} H, \text{Trm}(m, n_t) \rangle$ and $\langle \text{Wr} H, \text{Trm}(m, n_e) \rangle$, the resulting annotation for the statement becomes $\langle \text{Wr} H, \text{Trm}(m + 1, \max(n_t, n_e) + n_g + 2) \rangle$. The first timing value, namely $m + 1$, adds one expression evaluation step to the timing behavior of the branches, which is required to have the same value. The second timing value, namely $\max(n_t, n_e) + n_g + 2$ considers the expression compilation (factor $n_g$), the final skip command and the register evaluation (they count for the factor 2), together with the biggest factor between $n_t$ and $n_e$ for branches. Notice that alignment of branches is performed by applying the usual padding strategy.

As for the type system in Figure 10 the rule $[\text{while}]$ prevents implicit flow from happening by enforcing several constraints. Indirect information flows involving the loop guard are prevented by requiring the write effect of the loop to be lower than the write effect of the guard. The timing channel induced by the loop body is prevented by requiring the write effect of the body to be $\text{Wr} H$ if its timing behavior depends on secrets.

**Type System: Results** In order to formalize the properties of the type system we proceed with specifying the semantics of the while language. Since we are targeting the notion of Strong Security, we instantiate the abstract machine for the while language as a fault-prone system.

Observe that we formulate the semantic definition generally enough to be suitable for $i$-while programs as well. Since $i$-while programs are a subclass of while programs, the only difference to be considered is the set of variables on which programs are defined in the two languages. We therefore define the rules in Figure 20 to be parametric on $\mathcal{V}$, the set of variables, such that $\mathcal{V} = \mathcal{V}_L$ for while programs and $\mathcal{V} = \mathcal{V}_L \cup \mathcal{V}_R$ for $i$-while programs.
We define the memory as an element $M$ from the set $\{ Var \cup Reg \to N \}$ of mappings between variables and values in $N$. The semantics for the while language as a fault-prone system is described by the LTS $S_w = \{ \langle C, M \rangle, \to, \{ \text{ch!n}| \text{ch} \in \{ \text{low, high} \} \text{ and } n \in N \} \cup \{ \tau \} \}$ where $C$ is the fault-tolerant part of configurations, $M$ is the fault-prone part and $\to$ is obtained by rules in Figure 20. Notice that rules for sequential composition are expressed using evaluation contexts, defined as $R ::= [-] | R; C$. The rule $[c - 2]$ requires a particular attention: since we need a fine control over the number of execution steps, rule $[c - 2]$ simultaneously executes statements that terminates in one step (like skip, :=, out) and stripes off the terminating command \* they are reduced to. In this way, the number of reductions performed by a while program according to while semantics are easily mapped to the number of steps performed by the corresponding RISC program in the RISC semantics.

We want to show that any type-correct while program is SS. First we instantiate the definition of Strong Security for while programs.

**Definition 18 (Strong Security for while programs).** We say that a while program $C$ is strongly secure if it is strongly secure according to Definition 7 instantiated for the fault-prone system $S_w$.

The first property of the type system presented in Figures 16, 17 and 18 is that any type-correct program is strongly secure. We formalize this result as follows.
Proposition 3 (Type System Enforces Strong Security). Let \( C \) be a while program. If there exists \( \Phi \) such that \( \Phi \vdash_{Var}^C \{ D \}, \langle w, t \rangle, \Phi' \), then \( C \) is strongly secure.

Proving this statement requires few auxiliary results. The first one, formalized in Lemma \( \mathcal{L} \), illustrates a property of the type system which we refer to as “upward closure”: if a command is type-correct with respect to a register record \( \Phi \), it also results type-correct with respect to any other register record \( \Phi' \) that is bigger than \( \Phi \). Also, the output register record corresponding to \( \Phi' \) results bigger than the one corresponding to \( \Phi \).

In order to prove Lemma \( \mathcal{L} \), two auxiliary results are required. The first one formalizes some properties of the operations over register records.

Lemma 4. Let \( \Phi \) and \( \Phi' \) two register records such that \( \Phi' \supseteq \Phi \). Then:

- \( \Phi'[r \not\in \Phi] \supseteq \Phi[r \not\in \Phi] \);
- \( \Phi'[r \not\leftrightarrow x] \supseteq \Phi[r \not\leftrightarrow x] \).

Proof. The first statement follows directly by the fact that inclusion is preserved by set difference. Proving the second statement is slightly more challenging, since the update operation requires the bijection property of register records to be preserved. In particular, implementing \( \Phi[r \not\leftrightarrow x] \) requires that (i) any existing association \( [r' \leftrightarrow x] \) is removed, and (ii) the new association \( [r' \not\leftrightarrow x] \) is added to the register record. The statement is proved by distinguishing the following cases:

- Assume \( x \) is not associated in \( \Phi \). This implies that there is no \( r' \in \text{Reg} \) such that \( [r' \leftrightarrow x] \in \Phi \). We distinguish four cases:
  - \( x \) is not associated in \( \Phi' \). Then \( \Phi'[r \not\leftrightarrow x] \supseteq \Phi[r \not\leftrightarrow x] \) is true because \( \Phi'[r \not\leftrightarrow x] \subsetneq \Phi'[r \not\leftrightarrow x] \) since \( \Phi'[r \not\leftrightarrow x] \supseteq \Phi[r \not\leftrightarrow x] \).
  - There exists \( r' \neq r \) such that \( [r' \leftrightarrow x] \in \Phi' \). Then \( \Phi'[r \not\leftrightarrow x] \supseteq \Phi[r \not\leftrightarrow x] \) because \( r' \) is unassociated in \( \Phi \).
  - \( [r' \not\leftrightarrow x] \in \Phi' \) but \( \mu' \neq \mu \). Then \( \Phi'[r \not\leftrightarrow x] \supseteq \Phi[r \not\leftrightarrow x] \) because \( \Phi'[r \not\leftrightarrow x] \supseteq \Phi[r \not\leftrightarrow x] \).
  - Assume \( x \) is associated in \( \Phi \), hence there exists \( r' \in \text{Reg} \) such that \( [r' \not\leftrightarrow x] \in \Phi \).

Since \( \Phi' \supseteq \Phi \), \( [r' \not\leftrightarrow x] \in \Phi' \). We distinguish three cases:

- \( r' \neq r \). Then \( \Phi'[r \not\leftrightarrow x] \supseteq \Phi[r \not\leftrightarrow x] \) since (i) \( \Phi'[r \not\leftrightarrow x] \subsetneq \Phi'[r \not\leftrightarrow x] \) and (ii) \( r' \) results unassociated in both \( \Phi'[r \not\leftrightarrow x] \) and \( \Phi[r \not\leftrightarrow x] \).
- \( r' = r \) but \( \mu' \neq \mu \). Then \( \Phi'[r \not\leftrightarrow x] \supseteq \Phi[r \not\leftrightarrow x] \) holds because \( \Phi'[r \not\leftrightarrow x] \supseteq \Phi[r \not\leftrightarrow x] \).
- Assume \( x \) is associated in \( \Phi \), hence there exists \( r' \in \text{Reg} \) such that \( [r' \not\leftrightarrow x] \in \Phi \).
Lemma 4. If \( r' = r \) and \( \mu' = \mu \). Then \( \Phi'[r \xrightarrow{r'} x] = \Phi' \supseteq \Phi = \Phi[r \xrightarrow{r'} x] \).

The second result that supports the proof of Lemma 4 formalizes the notion of “upward closure” for expressions.

**Lemma 5 (Register Record Upward Closure for Expressions).** Let \( E \) be a while expression. If there exists \( \Phi \) such that \( \Phi, A \models_{\text{Reg \ Var}} E \rightarrow \{ D \}, \langle \lambda, n \rangle, r, \Phi_\alpha \) then \( \forall \Phi' \supseteq \Phi \Phi', A \models_{\text{Reg \ Var}} E \rightarrow \{ D \}, \langle \lambda, n \rangle, r, \Phi_\beta \) such that \( \Phi_\beta \supseteq \Phi_\alpha \).

**Proof.** We prove the proposition by induction on the structure of \( E \) and by cases on the last rule applied in the type derivation.

**Base case**

Case \( E = k \). We know that there exists \( \Phi \) such that \( \Phi, A \models_{\text{Reg \ Var}} k \rightarrow \{ r := k \}, \langle \text{level}(r), 1 \rangle, r, \Phi'[r \not\rightarrow] \) and consider \( \Phi' \supseteq \Phi \). Then \( \Phi', A \models_{\text{Reg \ Var}} k \rightarrow \{ r := k \}, \langle \text{level}(r), 1 \rangle, r, \Phi'[r \not\rightarrow] \) and \( \Phi_\beta = \Phi'[r \not\rightarrow] \supseteq \Phi[r \not\rightarrow] = \Phi_\alpha \) by Lemma 4.

Case \( E = x \). Assume that the rule \([V - \text{cached}]\) is used. Then there exists \( \Phi \) such that \( \Phi, A \models_{\text{Reg \ Var}} x \rightarrow \{ r := x \}, \langle \text{level}(r), 1 \rangle, r, \Phi[r \not\rightarrow x] \) and \( \Phi_\beta = \Phi[r \not\rightarrow x] \supseteq \Phi[r \not\rightarrow x] = \Phi_\alpha \) by Lemma 4.

**Inductive step**

Case \( E = E_1 \op E_2 \). We know that there exists \( \Phi \) such that \( \Phi, A \models_{\text{Reg \ Var}} E_1 \op E_2 \rightarrow \{ D_1; D_2; r := r \op r' \}, \langle \lambda, n_1 + n_2 + 1 \rangle, r, \Phi_2[r \not\rightarrow] \), under the assumption that \( \Phi, A \models_{\text{Reg \ Var}} E_1 \rightarrow \{ D_1 \}, \langle \lambda, n_1 \rangle, r, \Phi_1 \) and \( \Phi_1, A \cup \{ r \} \models_{\text{Reg \ Var}} E_2 \rightarrow \{ D_2 \}, \langle \lambda, n_2 \rangle, r', \Phi_2 \). Consider \( \Phi' \supseteq \Phi \). By applying the inductive hypothesis on \( E_1 \) we obtain \( \Phi', A \models_{\text{Reg \ Var}} E_1 \rightarrow \{ D_1 \}, \langle \lambda, n_1 \rangle, r, \Phi'_1 \) such that \( \Phi'_1 \supseteq \Phi_1 \). By applying the inductive hypothesis on \( E_2 \) we obtain \( \Phi'_1, A \cup \{ r \} \models_{\text{Reg \ Var}} E_2 \rightarrow \{ D_2 \}, \langle \lambda, n_2 \rangle, r', \Phi'_2 \) such that \( \Phi'_2 \supseteq \Phi_2 \). Hence \( \Phi', A \models_{\text{Reg \ Var}} E_1 \op E_2 \rightarrow \{ D_1; D_2; r := r \op r' \}, \langle \lambda, n_1 + n_2 + 1 \rangle, r, \Phi'_2[r \not\rightarrow] \) and \( \Phi_\beta = \Phi'_2[r \not\rightarrow] \supseteq \Phi_2[r \not\rightarrow] = \Phi_\alpha \) by Lemma 4.

We continue with the formalization (and the proof) of “upward closure” for commands.

**Lemma 6 (Register Record Upward Closure for Commands).** Let \( C \) be a while program. If there exists \( \Phi \) such that \( \Phi \models_{\text{Reg \ Var}} C \rightarrow \{ D \}, \langle w, t \rangle, \Phi_\alpha \) then \( \forall \Phi' \supseteq \Phi \Phi' \models_{\text{Reg \ Var}} C \rightarrow \{ D \}, \langle w, t \rangle, \Phi_\beta \) such that \( \Phi_\beta \supseteq \Phi_\alpha \).

**Proof.** We prove the proposition by induction on the structure of \( C \) and by cases on the last rule applied in the type derivation.
Base case

Case $C = \text{skip}$. We know that $\Phi \vdash_{\text{Reg}} \text{skip} \leftrightarrow \{\text{skip}\}$, $⟨\text{Wr}, \text{Trm} (1, 1)⟩$, $Φ$. Consider $Φ' \equiv Φ$. Then $Φ' \vdash_{\text{Var}} \text{skip} \leftrightarrow \{\text{skip}\}$, $⟨\text{Wr}, \text{Trm} (1, 1)⟩$, $Φ'$ and $Φ_β = Φ' \equiv Φ = Φ_α$ by hypothesis.

Case $C = x := E$. We know that $\Phi \vdash_{\text{Reg}} x := E \leftrightarrow \{D; x := r\}$, $\text{level}(x) = H?⟨\text{Wr}, \text{Trm} (1, n + 1)⟩$, $⟨\text{Wr} L, \text{Trm} L⟩$, $Φ_e[r \leftarrow x]$, under the assumption that $Φ, \{\} \vdash_{\text{Reg}} E \leftrightarrow \{D\}, \text{level}(x), n, r, Φ_c$. Consider $Φ' \equiv Φ$. By applying Lemma 5 we obtain that $Φ', \{\} \vdash_{\text{Reg}} E \leftrightarrow \{D\}, \text{level}(x), n, r, Φ'_c$, such that $Φ'_e \equiv Φ_e$ and $Φ' \vdash_{\text{Reg}} x := E \leftrightarrow \{D; x := r\}$, $\text{level}(x) = H?⟨\text{Wr}, \text{Trm} (1, n + 1)⟩$: $⟨\text{Wr} L, \text{Trm} L⟩$, $Φ'_e[r \leftarrow x]$ and $Φ_β = Φ'_e \equiv Φ_e = Φ_α$ by Lemma 4.

Inductive step

Case $C = \text{out ch E}$. The derivation $Φ \vdash_{\text{Reg}} \text{out ch E} \leftrightarrow \{D; \text{out ch r}\}$, $\text{level}(\text{ch}) = H?⟨\text{Wr}, \text{Trm} (1, n + 1)⟩$: $⟨\text{Wr} L, \text{Trm} L⟩$, $Φ_e$ holds, under the assumption that $Φ, \{\} \vdash_{\text{Reg}} E \leftrightarrow \{D\}, \text{level}(\text{ch}), n, r, Φ_c$. Consider $Φ' \equiv Φ$. By applying Lemma 5 we obtain that $Φ', \{\} \vdash_{\text{Reg}} E \leftrightarrow \{D\}, \text{level}(\text{ch}), n, r, Φ'_c$ such that $Φ'_e \equiv Φ_e$. Hence $Φ' \vdash_{\text{Reg}} \text{out ch E} \leftrightarrow \{D; \text{out ch r}\}$, $\text{level}(\text{ch}) = H?⟨\text{Wr}, \text{Trm} (1, n + 1)⟩$: $⟨\text{Wr} L, \text{Trm} L⟩$, $Φ'_e$ and $Φ_β = Φ'_e \equiv Φ_e = Φ_α$.

Assume the rule $[\text{if } \text{any}]$ is used. By hypothesis, we have that the derivation $Φ \vdash_{\text{Reg}} \text{if } \text{any}$ if $E$ then $C_t$ else $C_c$ if $E$ then $C_t$ else $C_c$. By applying the inductive hypothesis on $C_t$ we obtain $Φ' \vdash_{\text{Var}} C_t \leftrightarrow \{D_t\}$, $⟨\text{wr} (\text{any}) ∪ w_1 ∪ w_2, \text{term}(\text{any}) \cup t_1 ∪ t_2⟩$, $Φ_2 \cap Φ_3$ holds, for $D_t' = D_t$; skip and $D_c' = D_c$; skip, providing that $Φ, \{\} \vdash_{\text{Reg}} C_t \leftrightarrow \{D_t\}, ⟨\text{wr} (\text{any}) ∪ w_1 ∪ w_2, \text{term}(\text{any}) \cup t_1 ∪ t_2⟩$, $Φ_2 \cap Φ_3$ such that $Φ'_t \equiv Φ_t$. Hence we conclude that $Φ' \vdash_{\text{Reg}} \text{if } \text{any} : E$ then $C_t$ else $C_c$ if $E$ then $C_t$ else $C_c$. By applying Lemma 5 on $E$ we obtain $Φ', \{\} \vdash_{\text{Reg}} \text{if } \text{any} : E \leftrightarrow \{D_g\}, ⟨\text{wr} (\text{any}) ∪ w_1 ∪ w_2, \text{term}(\text{any}) \cup t_1 ∪ t_2⟩$, $Φ_2 \cap Φ_3$ such that $Φ'_t \equiv Φ_t$. By applying the inductive hypothesis on $C_c$ we obtain $Φ' \vdash_{\text{Var}} C_c \leftrightarrow \{D_c\}$, $⟨\text{wr} (\text{any}) ∪ w_1 ∪ w_2, \text{term}(\text{any}) \cup t_1 ∪ t_2⟩$, $Φ'_2 \cap Φ'_3$ such that $Φ'_c \equiv Φ_c$.
φ' \equiv \phi_3$. Hence we can conclude that the derivation $\phi' \vdash^{\text{Reg}}_{\text{Var}} E$ if $E$ then $C_t$ else $C_e \rightarrow \{D_0;\ \text{if} \ r \ \text{then} \ D'_r \ \text{else} \ D'_e\}$, $(\text{Wr} \ H, \ \text{Trm} \ (m + 1, n_q + \max(n_i, n_e) + 2))$, $\phi_2 \cap \phi_3'$ holds and $\phi_0 = \phi_2 \cap \phi_3' \supseteq \phi_0 \cap \phi_3 = \phi_0$.

Case $C = \text{while} \ x \ \text{do} \ C'$. By considering the rule definition we know that $\phi \vdash^{\text{Reg}}_{\text{Var}} \text{while} \ x \ \text{do} \ C \rightarrow \{D_0; \ \text{while} \ r \ \text{do} \ \{D; \ D_0; \ \text{skip}\}\} \ \langle \text{write}(\lambda) \sqcup w, \ \text{term}(\lambda) \sqcup t \rangle \ \phi_B$ for $D_0 = r := x; \ x := r, \ \phi_\star = \phi[r \rightarrow x], \ \phi_B \sqsubseteq \phi_\star$ and $\phi_B \sqsubseteq \phi_E[r \rightarrow x]$, providing that $\phi_B \vdash^{\text{Reg}}_{\text{Var}} C \rightarrow \{D\}, \langle w, t \rangle \phi_E$. Consider $\phi' \equiv \phi$. By Lemma 4 we know that $\phi'[r \rightarrow w] \equiv \phi[r \rightarrow w]$, hence the same $\phi_B$ used for $\phi$ can be used for $\phi'$ to conclude that $\phi' \vdash^{\text{Reg}}_{\text{Var}} \text{while} \ x \ \text{do} \ C \rightarrow \{D_0; \ \text{while} \ r \ \text{do} \ \{D; \ D_0; \ \text{skip}\}\} \ \langle \text{write}(\lambda) \sqcup w, \ \text{term}(\lambda) \sqcup t \rangle \ \phi_B$ and $\phi_\beta = \phi_B \sqsubseteq \phi_B = \phi_\alpha$.

Case $C = C_1; C_2$. We know that $\phi \vdash^{\text{Reg}}_{\text{Var}} C_1; C_2 \rightarrow \{D_1; D_2\}, \langle w_1 \sqcup w_2, t_1 \sqcup t_2 \rangle \ \phi_\star$, providing that $\phi \vdash^{\text{Reg}}_{\text{Var}} C_1 \rightarrow \{D_1\}, \langle w_1, t_1 \rangle \ \phi_1$ as well as $\phi_1 \vdash^{\text{Reg}}_{\text{Var}} C_2 \rightarrow \{D_2\}, \langle w_2, t_2 \rangle \ \phi_2$ hold. Consider $\phi' \equiv \phi$. By applying the inductive hypothesis on $C_1$ we obtain $\phi' \vdash^{\text{Reg}}_{\text{Var}} C_1 \rightarrow \{D_1\}, \langle w_1, t_1 \rangle \ \phi'_1$ such that $\phi'_1 \equiv \phi_1$. By applying the inductive hypothesis on $C_2$ we obtain $\phi'_1 \vdash^{\text{Reg}}_{\text{Var}} C_2 \rightarrow \{D_2\}, \langle w_2, t_2 \rangle \ \phi'_2$ such that $\phi'_2 \equiv \phi_2$. Hence $\phi' \vdash^{\text{Reg}}_{\text{Var}} C_1; C_2 \rightarrow \{D_1; D_2\}, \langle w_1 \sqcup w_2, t_1 \sqcup t_2 \rangle \ \phi'_2$ and $\phi_\beta = \phi'_2 \equiv \phi_2 = \phi_\alpha$.

The second result that supports the proof of Proposition 3 is subject reduction. In order to characterize subject reduction we have to reason about the connection between the operational semantics and the type system. For this purpose it is convenient to generalize the syntax to include $\bullet$ (the terminated program) as a possible sub term of any sequential composition term. We extend the type system to include the following typing rule for $\bullet$:

$$
\frac{}{\phi \vdash^{\text{Reg}}_{\text{Var}} \bullet \rightarrow \{\bullet\}, \langle \text{Wr} \ H, \ \text{Trm} \ (0, 0) \rangle \phi}
$$

We choose this particular typing value since $\bullet$ represents the final configuration, which does not perform any reduction step.

**Lemma 7 (Extended typing is compatible with structural equivalence).** For any while-e program $C$, if $\phi \vdash^{\text{Reg}}_{\text{Var}} C \rightarrow \{E\}, \langle w, t \rangle \phi'$ and $C \equiv C'$, then $\phi \vdash^{\text{Reg}}_{\text{Var}} C' \rightarrow \{D'\}, \langle w, t \rangle \phi'$ such that $D \equiv D'$.

**Proof.** Induction on derivation, which follows easily from the fact that the typing of $\bullet, C, C; \bullet$ and $C$ are all equivalent.

This compatibility property allows us to implicitly view a typing derivation as applying to structural equivalence classes of terms (much in the same way that one reasons informally about alpha equivalence in languages with variable binding). When reasoning about induction on the size of a derivation, we will view the size of a derivation to be the size of the $[T]$-rule free derivation i.e. the smallest derivation of the given typing.
Lemma 8 (Reduction Context Typing). For any while command $C$ and reduction context $R[\cdot]$, there exists $\Phi$ such that $\Phi \vdash_{\text{Reg}} R[\cdot] \leftrightarrow \{\ldots \}, \langle w, t \rangle, \Phi'$ if and only if there exist $\Phi$ and pairs $t_1, t_2$ and $w_1, w_2$ such that $\Phi \vdash_{\text{Var}} R[\cdot] \leftrightarrow \{\ldots \}, \langle w_1, t_1 \rangle, \Phi_1$ and $\Phi_1 \vdash_{\text{Var}} R[\cdot] \leftrightarrow \{\ldots \}, \langle w_2, t_2 \rangle, \Phi'$ and $t_1 = \text{Trm} \ H \Rightarrow w_2 = \text{Wr} \ H$ for $w = w_1 \sqcup w_2$ and $t = t_1 \sqcup t_2$.

Proof. We prove the lemma by induction on the structure of $R$.

**Base Case**
Assume $R = \emptyset$. Then $R[\cdot] = C$.

$(\Rightarrow)$ Assume $\Phi \vdash_{\text{Reg}} R[\cdot] \leftrightarrow \{\ldots \}, \langle w, t \rangle, \Phi'$. Since $R[\cdot] = C$ then $\Phi \vdash_{\text{Reg}} C \leftrightarrow \{\ldots \}, \langle w, t \rangle, \Phi'$ hence $t_1 = t$ and $w_1 = w$. Also, $R[\cdot] = \emptyset$, and we know that $\forall \Phi \vdash_{\text{Reg}} \emptyset \leftrightarrow \{\ldots \}, \langle \text{Wr} \ H, \text{Trm} \ (0, 0) \rangle, \Phi'$, hence $t_2 = \text{Trm} \ (0, 0)$ and $w_2 = \text{Wr} \ H$.

Notice that $w = w_1 = w_2$ and $t = t_1 = t_1 \sqcup t_2$.

$(\Leftarrow)$ Assuming $\Phi \vdash_{\text{Reg}} C \leftrightarrow \{\ldots \}, \langle w, t \rangle, \Phi'$ the following type derivation is correct

$$
\Phi \vdash_{\text{Var}} C \leftrightarrow \{\ldots \}, \langle w, t \rangle, \Phi' \\
\Phi \vdash_{\text{Reg}} C; \emptyset \leftrightarrow \{\ldots \}, \langle w, t \rangle, \Phi'
$$

and $C; \emptyset \equiv C = R[\cdot]$.

**Inductive Step**
Assume $R[\cdot] = R_1[\cdot]; C_1$. Then there exists a command $C'$ such that $R[\cdot] = R_1[\cdot]; C_1$.

$(\Rightarrow)$ Assume $\Phi \vdash_{\text{Reg}} R[\cdot] \leftrightarrow \{\ldots \}, \langle w, t \rangle, \Phi'$ Then the following type derivation must exist:

$$
\Phi \vdash_{\text{Reg}} R_1[C'] \leftrightarrow \{\ldots \}, \langle w_{\alpha}, t_{\alpha} \rangle, \Phi_{\alpha} \\
\Phi_{\alpha} \vdash_{\text{Var}} C_1 \leftrightarrow \{\ldots \}, \langle w_{\beta}, t_{\beta} \rangle, \Phi_{\beta} \\
\quad w = w_{\alpha} \sqcup w_{\beta} \\
\quad t = t_{\alpha} \sqcup t_{\beta} \\
\Phi \vdash_{\text{Reg}} R_1[C']; C_1 \leftrightarrow \{\ldots \}, \langle w, t \rangle, \Phi'
$$

such that $t_{\alpha} = \text{Trm} \ H \Rightarrow w_{\beta} = \text{Wr} \ H$. We now focus on $R_1[C']$. By applying the inductive hypothesis we know that there exist $w_{\alpha}$, $w_{\beta}$, $t_{\alpha}$, $t_{\beta}$ and $r_{\alpha}$ such that $\Phi \vdash_{\text{Reg}} C' \leftrightarrow \{\ldots \}, \langle w_{\alpha}, t_{\alpha} \rangle, \Phi_1$ and $\Phi_1 \vdash_{\text{Var}} R_1[\cdot] \leftrightarrow \{\ldots \}, \langle w_{\beta}, t_{\beta} \rangle, \Phi_1$ and $w_{\alpha} = w_{\alpha} \sqcup w_{\beta}$ and $t_{\alpha} = t_{\alpha} \sqcup t_{\beta}$. Hence, the following type derivation

$$
\Phi_1 \vdash_{\text{Reg}} R_1[\cdot] \leftrightarrow \{\ldots \}, \langle w_{\beta}, t_{\beta} \rangle, \Phi_1 \\
\Phi_{\alpha} \vdash_{\text{Reg}} C_1 \leftrightarrow \{\ldots \}, \langle w_{\beta}, t_{\beta} \rangle, \Phi_{\beta} \\
\quad \Phi_1 \vdash_{\text{Reg}} R_1[C']; C_1 \leftrightarrow \{\ldots \}, \langle w_{\beta} \sqcup w_{\beta}, t_{\beta} \sqcup t_{\beta} \rangle, \Phi'
$$

is correct. In particular, if $t_{\beta} = \text{Trm} \ H$, then $t_{\alpha} = \text{Trm} \ H$, hence $w_{\beta} = \text{Wr} \ H$ for hypothesis.

$(\Leftarrow)$ Assume that $\Phi \vdash_{\text{Reg}} C' \leftrightarrow \{\ldots \}, \langle w_{\alpha}, t_{\alpha} \rangle, \Phi_1$ together with $\Phi_1 \vdash_{\text{Reg}} R_1[\cdot]; C_1 \leftrightarrow \{\ldots \}, \langle w_{\beta}, t_{\beta} \rangle, \Phi'$ such that $t_{\alpha} = \text{Trm} \ H \Rightarrow w_{\beta} = \text{Wr} \ H$. Then the following type
derivation

\[
\Phi \vdash_{\text{Var}}^{\text{Reg}} C' \leftarrow \{ \ldots \}, \langle w_\alpha, t_\alpha \rangle, \Phi_1 \\
\Phi_1 \vdash_{\text{Var}}^{\text{Reg}} R_1[\bullet]; C_1 \leftarrow \{ \ldots \}, \langle w_c, t_c \rangle, \Phi' \\
\Phi \vdash_{\text{Var}}^{\text{Reg}} R_1[C']; C_1 \leftarrow \{ \ldots \}, \langle w_\alpha \sqcup w_c, t_\alpha \sqcup t_c \rangle, \Phi'
\]

is correct.

We can now present all the details related to subject reduction.

**Proposition 4 (Subject Reduction).** Let \( C \) be a while program. If there exists \( \Phi \) such that \( \Phi \vdash_{\text{Var}}^{\text{Reg}} C \leftarrow \{ D \}, \langle w_\alpha, t_\alpha \rangle, \Phi_\alpha \) and there exists \( M \) such that \( \langle C', M' \rangle \rightarrow (C', M') \), then there exists \( \Phi' \) such that \( \Phi' \vdash_{\text{Var}}^{\text{Reg}} C' \leftarrow \{ D' \}, \langle w_\beta, t_\beta \rangle, \Phi_\beta \) and:

- \( w_\beta \sqsubseteq w_\alpha \) and \( t_\beta \sqsubseteq t_\alpha \);
- \( \Phi_\beta \sqsubseteq \Phi_\alpha \).

**Proof.** We prove the proposition by induction on the structure of \( C \) and by cases on the last rule applied in the type derivation. In the proof we omit the explicit representation of the code production since it is not relevant in this context.

**Base case**

In this case \( C \in \{ \text{skip}, x := E, \text{out} \; \text{ch} \; E \} \). For any such \( C \) we have that \( \forall M \langle C, M \rangle \rightarrow (\bullet, M') \) for suitable \( l \) and \( M' \). Since \( \forall \Phi \Phi \vdash_{\text{Var}}^{\text{Reg}} \bullet \leftarrow \{ \bullet \}, \langle \text{Wr} \; H, \text{Trm} \; (0, 0) \rangle \), \( \Phi \) the statement trivially holds.

**Inductive step**

Case \( C = \text{if} \; E \) then \( C_1 \) else \( C_2 \). An if statement can be typed according to two rules, \([\text{if} - \text{any}]\) and \([\text{if} - \text{H}]\).

Assume the rule \([\text{if} - \text{any}]\) is used. Then \( \Phi \vdash_{\text{Var}}^{\text{Reg}} \beta \) if \( E \) then \( C_1 \) else \( C_2 \) \( \leftarrow \{ \ldots \}, \langle \text{write}(\lambda) \sqcup w_1 \sqcup w_2, \text{term}(\lambda) \sqcup t_1 \sqcup t_2 \rangle, \Phi_F \) holds under the assumption that \( \Phi,\{ \} \vdash_{\text{Var}}^{\text{Reg}} E \leftarrow \{ \ldots \}, \langle \lambda, n_\beta \rangle, r, \Phi_1 \) and \( \Phi_1 \vdash_{\text{Reg}}^{\text{Var}} C_1 \leftarrow \{ \ldots \}, \langle w_1, t_1 \rangle, \Phi_2 \) and \( \Phi_1 \vdash_{\text{Reg}}^{\text{Var}} C_2 \leftarrow \{ \ldots \}, \langle w_2, t_2 \rangle, \Phi_3 \), such that \( \Phi_F = \Phi_2 \sqcap \Phi_3 \). Assume that \( M \) is such that \( \langle \text{if} \; E \; \text{then} \; C_1 \; \text{else} \; C_2, M \rangle \rightarrow (C_1, M) \). The statement is true for \( \Phi' = \Phi_1 \) since \( w_\beta = \frac{1}{2} \text{write}(\lambda) \sqcup w_1 \sqcup w_2 = w_\alpha \) and \( t_\beta = \frac{1}{2} \text{term}(\lambda) \sqcup t_1 \sqcup t_2 = t_\alpha \). Thus \( \Phi' \sqsubseteq \Phi_\alpha \). The case for \( M \) such that \( \langle \text{if} \; E \; \text{then} \; C_1 \; \text{else} \; C_2, M \rangle \rightarrow (C_1, M) \) is analogous, hence it is omitted.

Consider the case in which the rule \([\text{if} - \text{H}]\) is used instead. Then we know \( \Phi \vdash_{\text{Var}}^{\text{Reg}} \beta \) if \( E \) then \( C_1 \) else \( C_2 \) \( \leftarrow \{ \ldots \}, \langle \text{Wr} \; H, \text{Trm} \; (m + 1, n_\beta + \text{max}(n_4, n_\epsilon) + 2) \rangle, \Phi_F \) under the assumption that \( \Phi,\{ \} \vdash_{\text{Var}}^{\text{Reg}} E \leftarrow \{ \ldots \}, \langle H, n_\beta \rangle, r, \Phi_1 \) and \( \Phi_1 \vdash_{\text{Var}}^{\text{Reg}} C_1 \leftarrow \{ \ldots \}, \langle \text{Wr} \; H, \text{Trm} \; (m, n_\beta) \rangle, \Phi_2 \) and \( \Phi_1 \vdash_{\text{Reg}}^{\text{Var}} C_2 \leftarrow \{ \ldots \}, \langle \text{Wr} \; H, \text{Trm} \; (m, n_\epsilon) \rangle, \Phi_3 \), such that \( \Phi_F = \Phi_2 \sqcap \Phi_3 \). Assume that \( M \) is such that \( \langle \text{if} \; E \; \text{then} \; C_1 \; \text{else} \; C_2, M \rangle \rightarrow (C_1, M) \). The statement is true for \( \Phi' = \Phi_1 \) since \( w_\beta = \text{Wr} \; H \sqsubseteq \text{Wr} \; H = w_\alpha \) and \( t_\beta = \text{Trm} \; (m, n_\beta) \sqsubseteq \text{Trm} \; (m + 1, n_\beta + \text{max}(n_4, n_\epsilon) + 2) = t_\alpha \). Thus \( \Phi' \sqsubseteq \Phi_\alpha \). The case for \( M \) such that \( \langle \text{if} \; E \; \text{then} \; C_1 \; \text{else} \; C_2, M \rangle \rightarrow (C_1, M) \) is analogous, hence it is omitted.

Case \( C = \text{while} \; x \; \text{do} \; C' \). Then we know that \( \Phi \vdash_{\text{Reg}}^{\text{Var}} \text{while} \; x \; \text{do} \; C' \leftarrow \{ \ldots \}, \langle \text{write}(\lambda) \sqcup w, \text{term}(\lambda) \sqcup t \rangle, \Phi_B \). This is true under the assumption that, for
\[ \Phi_2 = \Phi[E[r \rightarrow W]], \] there exists \( \Phi_B \) such that \( \Phi_B \models \Phi_2 \) and \( \Phi_B \models \Phi_E[r \rightarrow W] \) for which \( \Phi_B \vdash \text{Reg}_{\text{Var}} C' \hookrightarrow \{ \ldots \}, (w, t), \Phi_E \). It is required that \( \lambda = \text{level}(x) = \text{level}(r) \) and write(\( \lambda \)) \( \models w \) and \( t = \text{Trm} H \Rightarrow \text{write}(\lambda) = \text{Wr} H \). Assume that \( M \) is such that \( \langle \text{while } x \text{ do } C', M \rangle \vdash \langle C' \rangle \) while \( x \) do \( C' \), and consider the following type derivation

\[
\begin{align*}
\Phi_B \vdash \text{Reg}_{\text{Var}} C' \hookrightarrow \{ \ldots \}, (w, t), \Phi_E \\
\Phi_B \models \Phi_E[r \rightarrow W] \\
\text{write}(\lambda) \models w \\
t = \text{Trm} H \Rightarrow \text{write}(\lambda) = \text{Wr} H \\
\Delta
\end{align*}
\]

for \( \Delta = \Phi_E \vdash \text{Reg}_{\text{Var}} \) while \( x \) do \( C' \hookrightarrow \{ \ldots \}, (w, t), \Phi_B \).

Notice that the proposition is true for \( \Phi' = \Phi_B \) since \( \beta \models \text{write}(\lambda) \models w \) and \( t_\beta = t \uplus (\text{term}(\lambda) \uplus t) = \text{term}(\lambda) \uplus t \uplus \text{term}(\lambda) \uplus t = t_\alpha \) and \( \Phi_\alpha = \Phi_B \models \Phi_B = \Phi_\alpha \). The case for \( M \) such that \( \langle \text{while } x \text{ do } C', M \rangle \vdash \langle \bullet, M \rangle \) is trivial, hence it is omitted.

Case \( C = C_1; C_2 \). Then we know that \( \Phi \vdash \text{Reg}_{\text{Var}} C_1; C_2 \hookrightarrow \{ \ldots \}, (w_1 \sqcup w_2, t_1 \uplus t_2), \Phi_3 \) under the assumption that \( \Phi \vdash \text{Reg}_{\text{Var}} C_1 \hookrightarrow \{ \ldots \}, (w_1, t_1), \Phi_1 \) and \( \Phi \vdash \text{Reg}_{\text{Var}} C_2 \hookrightarrow \{ \ldots \}, (w_2, t_2), \Phi_2 \) and \( t_1 = \text{Trm} H \Rightarrow w_2 = \text{Wr} H \). We now consider the reduction of \( C \) by distinguishing two cases.

Assume the rule \( \lfloor e = 1 \rfloor \) is applied. Hence there exists \( C_3 \) such that \( C = R[C_3] \) and \( \langle R[C'_3], M \rangle \xrightarrow{\text{Trm}} \langle R[C'_3], M' \rangle \), given that \( \langle C_3, M \rangle \xrightarrow{\text{Trm}} \langle C'_3, M' \rangle \) and \( C'_3 \neq \bullet \). By hypothesis of type-correctness and Lemma 8 this type derivation for \( C \) must exist

\[
\begin{align*}
\Phi \vdash \text{Reg}_{\text{Var}} C_3 \hookrightarrow \{ \ldots \}, (w_3, t_3), \Phi_3 \\
\Phi_3 \vdash \text{Reg}_{\text{Var}} R[\bullet] \hookrightarrow \{ \ldots \}, (w_c, t_c), \Phi_2 \\
t_3 = \text{Trm} H \Rightarrow w_c = \text{Wr} H \\
\Phi \vdash \text{Reg}_{\text{Var}} R[C'_3] \hookrightarrow \{ \ldots \}, (w_3 \sqcup w_c, t_3 \uplus t_c), \Phi_2
\end{align*}
\]

Notice that it must also be that \( w_3 \sqcup w_c = w_1 \sqcup w_2 \) and \( t_3 \uplus t_c = t_1 \uplus t_2 \). By applying the inductive hypothesis on \( C_3 \), there must exist a \( \Phi' \) such that \( \Phi' \vdash \text{Reg}_{\text{Var}} C_3' \hookrightarrow \{ \ldots \}, \Phi'_3; \langle w'_3, t'_3 \rangle \) such that \( w'_3 \sqcup w_3 \) and \( t'_3 \sqcup t_3 \) and \( \Phi'_3 \models \Phi_3 \). Consider this type derivation for \( R[C'_3] \)

\[
\begin{align*}
\Phi'_3 \vdash \text{Reg}_{\text{Var}} R[\bullet] \hookrightarrow \{ \ldots \}, (w_c, t_c), \Phi_2 \\
(t_i \Phi'_3 \vdash \text{Reg}_{\text{Var}} R[\bullet] \hookrightarrow \{ \ldots \}, (w_c, t_c), \Phi_2) \\
t'_3 = \text{Trm} H \Rightarrow w_c = \text{Wr} H \\
\Phi' \vdash \text{Reg}_{\text{Var}} R[C'_3] \hookrightarrow \{ \ldots \}, (w'_3 \sqcup w_c, t'_3 \uplus t_c), \Phi'_2
\end{align*}
\]

where \( i \) stays for \( \Phi' \vdash \text{Reg}_{\text{Var}} C_3' \hookrightarrow \{ \ldots \}, \langle w'_3, t'_3 \rangle, \Phi'_3 \) and holds by hypothesis, and \( ii \) is an application of Lemma 8 We have that \( w_\beta = w'_3 \sqcup w_c \sqcup w_3 \sqcup w_c = w_1 \sqcup w_2 = w_\alpha \).
and $t_\beta = t'_3 \uplus t_c \sqsubseteq t_3 \uplus t_c = t_1 \uplus t_2 = t_\alpha$ and $\Phi_\beta = \Phi'_2 \sqsupseteq \Phi_2 = \Phi_\alpha$ because of Lemma 6.

Assume the rule $[c - 2]$ is applied instead. Hence $\exists C_3, C_4$ such that $C = R[C_3; C_4]$ and $R[C_3; C_4], M \xrightarrow{1} R[C_4], M'$, given that $C_3, M \xrightarrow{1} \langle \ast, M' \rangle$. By hypothesis of type-correctness, this type derivation for $C$ must exist

$$\Phi \vdash_{\text{Reg}}^R C_3 \iff \{ \ldots, \langle w_3, t_3 \rangle, \Phi_3 \vdash_{\text{Var}}^R C_4 \iff \{ \ldots, \langle w_c, t_c \rangle, \Phi_2 \}

\begin{align*}
\vdash_{\text{Reg}}^{\ast} R[C_3; C_4] & \iff \{ \ldots, \langle w_3 \sqcup w_c, t_3 \uplus t_c \rangle, \Phi_2 \}
\end{align*}

$$

Notice that it must also be that $w_3 \sqcup w_c = w_1 \sqcup w_2$ and $t_3 \uplus t_c = t_1 \uplus t_2$. By having $\Phi' = \Phi_3$ we immediately have that $\Phi_3 \vdash_{\text{Reg}}^R C_4 \iff \{ \ldots, \langle w_c, t_c \rangle, \Phi_2 \}$ and $w_3 = w_c \sqsubseteq w_3 \sqcup w_c = w_1 \sqcup w_2 = w_\alpha$ and $t_\beta = t_c \sqsubseteq t_3 \uplus t_c = t_1 \uplus t_2 = t_\alpha$ and $\Phi_\beta = \Phi'_2 \sqsupseteq \Phi_2 = \Phi_\alpha$.

Before illustrating the details of the proof for Proposition 3 we continue with some other auxiliary results that formalize features of commands that are associated to a write effect $\text{Wr} H$. The first result states that a $\text{Wr} H$ command does not produce low-distinguishable actions and does not alter the low part of the memory.

**Lemma 9 (Low transparency of $\langle \text{Wr} H, t \rangle$ commands).** Let $C$ be a while $\ell$ command such that $C \neq \ast$ and there exists $\Phi$ such that $\Phi \vdash_{\text{Reg}}^R C \iff \{ \ldots, \langle \text{ Wr} H, t \rangle, \Phi_\alpha \}$. Then for any $M$ we have $\langle C, M \rangle \xrightarrow{3} \langle C', M' \rangle$ such that $\text{low}(l) = \tau$ and $M = \ast, M'$.

**Proof.** We prove the proposition by induction on the structure of $C$ and by cases on the last rule applied in the type derivation. In the proof we omit the explicit representation of the code production since it is not relevant in this context. Recall that $\forall \Phi \Phi \vdash_{\text{Reg}}^R \ast \iff \{ \ast, \langle \text{Wr} H, \text{Trm} \langle 0, 0 \rangle \rangle, \Phi \}$.

**Base case**

Case $C = \text{skip}$. We know that $\Phi \vdash_{\text{Reg}}^R \text{skip} \iff \{ \ldots, \langle \text{Wr} H, \text{Trm} \langle 1, 1 \rangle \rangle, \Phi \}$ and, for any memory $M$, $(\text{skip}, M) \xrightarrow{3} \langle \ast, M \rangle$.

Case $C = x : = E$. Assume that $\Phi \vdash_{\text{Reg}}^R x : = E \iff \{ \ldots, \langle \text{Wr} H, \text{Trm} \langle 1, n + 1 \rangle \rangle, \Phi' \}$. Then $\text{level}(x) = H$ and we know that, for any memory $M$, $\langle x : = E, M \rangle \xrightarrow{3} \langle \ast, M[x \sqcup E] \rangle$ such that $M[x \sqcup E] = L, M$.

Case $C = \text{out} \ ch \ E$. Assume that $\Phi \vdash_{\text{Reg}}^R \text{out} \ ch \ E \iff \{ \ldots, \langle \text{Wr} H, \text{Trm} \langle 1, n + 1 \rangle \rangle, \Phi' \}$. Then $\text{level}((ch) = H$ and we know that, for any memory $M$, it is true that $\langle \text{out} \ ch \ E, M \rangle \xrightarrow{3} \langle \ast, M \rangle$ such that $\text{low}(ch[E](M)) = \tau$.

**Inductive step**

Case $C = \text{if} \ E \text{ then } C_t \text{ else } C_e$. Regardless of the typing derivation, for any memory $M$ there are two cases that are possible: either $(\text{if} \ E \text{ then } C_t \text{ else } C_e, M) \xrightarrow{3} \langle C_t, M \rangle$ or $(\text{if} \ E \text{ then } C_t \text{ else } C_e, M) \xrightarrow{3} \langle C_e, M \rangle$. Hence, regardless of $M$, the transition produces a silent action and does not alter the memory, therefore the property trivially holds.

Case $C = \text{while} \ x \ do \ C'$. Regardless of the typing derivation, for any memory $M$ there are two cases that are possible: either we have that $\langle \text{while} \ x \ do \ C', M \rangle \xrightarrow{3} \langle \ast, M \rangle$ or $\langle \text{while} \ x \ do \ C', M \rangle \xrightarrow{3} \langle C', \text{while} \ x \ do \ C', M \rangle$. Hence, regardless of $M$,
the transition produces a silent action and does not alter the memory, and the property trivially holds.

Case $C = C_1; C_2$. We proceed by cases according to the semantic rule used to reduce the first element of the pair.

Assume $M$ is considered such that rule $[c - 1]$ is applied. Hence there exists $C_3 \in \{\text{if } E \text{ then } C_1 \text{ else } C_2, \text{ while } x \text{ do } C'\}$ such that $C_1; C_2 = R[C_3]$ and $\langle R[C_3], M \rangle \rightarrow \langle R[C_3'], M' \rangle$, given that $C_3 \neq \bullet$.

As it has been observed previously, regardless of their type derivation, none of the commands produce a visible action and alter the memory, hence the property trivially holds. Assume $M$ is considered such that rule $[c - 2]$ is applied instead. Hence there exist two commands $C_3$ and $C_4$ such that $C_1; C_2 = R[C_3; C_4]$ and $\langle R[C_3; C_4], M \rangle \rightarrow \langle R[C_3'], M' \rangle$, given that $\langle C_3, M \rangle \rightarrow (\bullet, M')$. We distinguish two cases. Assume $C_3$ in $\langle \text{skip}, x := E, \text{ out } ch E \rangle$. If $\Phi \vdash_{\text{Var}} C_1; C_2 \rightarrow \{\ldots\}, \langle \text{Wr } H, t \rangle, \Phi_\alpha$ then, by Lemma 8 a type derivation

\[
\begin{align*}
\Phi \vdash_{\text{Var}} C_3 \rightarrow \{\ldots\}, \langle \text{Wr } H, \text{Trm } (1, n_a) \rangle, \Phi_1 \\
\Phi_1 \vdash_{\text{Var}} R[\bullet; C_4] \rightarrow \{\ldots\}, \langle \text{Wr } H, t' \rangle, \Phi_\alpha
\end{align*}
\]

must exist such that $t = \text{Trm } (1, n_a)\circ t'$. By applying the inductive hypothesis on $C_3$ we know that for all $M$ we have $\langle C_3, M \rangle \rightarrow (\bullet, M')$ such that $\text{low}(l) = \tau$ and $M = L, M'$, hence the property holds. Assume $C_3 = \text{while } x \text{ do } C'$. As observed previously, the command neither produces a visible action nor alter the memory. Therefore the property trivially holds.

The second result investigates the features of $\text{Wr } H$ commands further.

**Lemma 10 (Progress properties of $\langle \text{Wr } H, t \rangle$ commands).** Let $C$ be a $\text{while } e \text{ command for which there exists } \Phi$ such that $\Phi \vdash_{\text{Reg}} C \rightarrow \{\ldots\}$, $\langle \text{Wr } H, \text{Trm } (m, n) \rangle, \Phi_\alpha$. Then for any memory $M$ such that $\langle C, M \rangle \rightarrow (\bullet, M')$ there exists $\Phi$ such that $\Phi' \vdash_{\text{Var}} C' \rightarrow \{\ldots\}, \langle \text{Wr } H, \text{Trm } (m - 1, n') \rangle, \Phi_\beta$ and $\Phi_\beta \models \Phi_\alpha$.

**Proof.** We prove the proposition by induction on the structure of $C$ and by cases on the last rule applied in the type derivation. In the proof we omit the explicit representation of the code production since it is not relevant in this context. Recall that $\forall \Phi \Phi' \vdash_{\text{Var}}\bullet \rightarrow \{\bullet\}, \langle \text{Wr } H, \text{Trm } (0, 0) \rangle, \Phi$, and observe that there is no type derivation that can associate $\langle \text{Wr } H, \text{Trm } (m, n) \rangle$ while $x$ do $C$.

**Base case**

Case $C = \text{skip}$. We know that $\Phi \vdash_{\text{Reg}} \text{skip} \rightarrow \{\ldots\}, \langle \text{Wr } H, \text{Trm } (1, 1) \rangle, \Phi$ and that, for any memory $M$, $\langle \text{skip}, M \rangle \rightarrow (\bullet, M)$.

Case $C = x := E$. Assume that $\Phi \vdash_{\text{Reg}} x := E \rightarrow \{\ldots\}, \langle \text{Wr } H, \text{Trm } (1, n + 1) \rangle, \Phi'$. Then we know that, for any memory $M$, it is true that $\langle x := E, M \rangle \rightarrow (\bullet, M[x\{E\}(M)])$.

Case $C = \text{out } ch E$. Assume that $\Phi \vdash_{\text{Var}} \text{out } ch E \rightarrow \{\ldots\}, \langle \text{Wr } H, \text{Trm } (1, n + 1) \rangle, \Phi'$. Then we know that, for any memory $M$, $\langle \text{out } ch E, M \rangle \rightarrow (\bullet, M)$.
Case $C = C_1; C_2$. Assume $\Phi \vdash_{reg} R[C_3] \iff \Phi_1 \vdash_{reg} R[C_3] \iff \Phi_1$. Then it must be
Assume $\Phi \vdash_{reg} \langle \varphi \rangle$ if $E$ then $C_t$ else $C_e \iff \{ \ldots \}$, $\langle Wr \ H, \ Trm \ (m + 1, n_g + max(n_t, n_e) + 2) \rangle$, $\Phi_2$ \therefore $\Phi_3$. Hence, regardless of which branch is triggered by the reduction step, the property holds.

Case $C = C_1; C_2$. Assume $\Phi \vdash_{reg} C_1; C_2 \iff \{ \ldots \}$, $\langle Wr \ H, \ Trm \ (m, n) \rangle$, $\Phi_0$. We proceed by cases according to the semantic rule used to reduce the first element of the pair.

Assume $M$ is considered such that rule $[e - 1]$ is applied. Hence there exists $C_3 = \{ \ldots \}$, $\langle Wr \ H, \ Trm \ (m, n) \rangle$. Then it must be $\Phi_1$, $\{ \} \vdash_{reg} \langle \varphi \rangle$, $\Phi_1$ together with the derivation $\Phi_1 \vdash_{reg} C_t \iff \{ \ldots \}$, $\langle Wr \ H, \ Trm \ (m, n) \rangle$, $\Phi_2$ and $\Phi_1 \vdash_{reg} C_e \iff \{ \ldots \}$, $\langle Wr \ H, \ Trm \ (m, n) \rangle$, $\Phi_3$. Hence, regardless of which branch is triggered by the reduction step, the property holds.

Inductive step

Assume $M$ is considered such that rule $[e - 2]$ is applied instead. Hence there exist two commands $C_3 \in \{ \text{skip, } x := E, \text{out } ch \ E \}$ and $C_4$ such that $C_1; C_2 = R[C_3; C_4]$ and $\langle R[C_3; C_4], M \rangle \vdash \langle \varphi \rangle \iff \langle \varphi \rangle$. By the hypothesis about the type of $C$ and Lemma 8, a type derivation

$$
\Phi \vdash_{reg} \langle \varphi \rangle 
$$

is a valid type derivation and $\Phi_0 \iff \Phi_0$. by Lemma $8$ and Lemma $6$.

Assume $M$ is considered such that rule $[e - 2]$ is applied. Hence there exist two commands $C_3 \in \{ \text{skip, } x := E, \text{out } ch \ E \}$ and $C_4$ such that $C_1; C_2 = R[C_3; C_4]$ and $\langle R[C_3; C_4], M \rangle \vdash \langle \varphi \rangle \iff \langle \varphi \rangle$. By the hypothesis about the type of $C$ and Lemma 8, a type derivation

$$
\Phi \vdash_{reg} \langle \varphi \rangle 
$$

hence $\Phi_1 \vdash_{reg} R[C_4] \iff \{ \ldots \}$, $\langle Wr \ H, \ Trm \ (m, n) \rangle$, $\Phi_0$ is a derivation proving the property.

Proof (of Proposition 3).

Let us consider the relation $R$ between while programs defined as follows:
Moreover, \(\mathcal{E}, \mathcal{M}\) of the security levels of written registers, which in turns represent the upper bound of variables from that necessary (Part 2).

We start by showing that pairs in \(\mathcal{E}, \mathcal{M}\) perform transitions that correspond to low equivalent actions and preserve low equality of memories. Also, we show that transitions are performed towards pairs of commands that are either in \(\mathcal{A}, \mathcal{X}\) or \(H^2\). We proceed by cases on \(C\).

Case (skip, skip). We know that \(\forall M =_L N \langle \text{skip}, M \rangle \xrightarrow{\tau} \langle \bullet, M \rangle\) if and only if \(\langle \text{skip}, N \rangle \xrightarrow{\tau} \langle \bullet, N \rangle\). Moreover, \(\langle \bullet, \bullet \rangle \in H^2\).

Case \((x := E, x := E)\). Assume that \(\text{level}(x) = H\). Then \(\forall M =_L N \langle x := E, M \rangle \xrightarrow{\tau} \langle \bullet, M[x\{[E](M)]\} \rangle\) if and only if \(\langle x := E, N \rangle \xrightarrow{\tau} \langle \bullet, N[x\{[E](N)]\} \rangle\). Moreover \(M[x\{[E](M)\}] =_L N[x\{[E](N)\}]\) since \(\text{level}(x) = H\).

Assume that \(\text{level}(x) = L\). Then we know that the derivation \(\Phi \vdash^\text{Reg}_\text{Var} x := E \rightarrow \{\ldots, \langle \text{Wr} L, \text{Trm} L, \Phi'[W x] \rangle\}\) holds under the assumption that \(\Phi, \{\} \vdash^\text{Reg}_\text{Var} E \rightarrow \{\ldots, \langle \text{L}, \text{n} \rangle, r, \Phi'\}\). Since the security level of an expression represents the upper bound of the security levels of written registers, which in turns represent the upper bound of the security levels of read variables, the type derivation ensures that \(E\) does not involve variables from \(H\). Hence \(\forall M =_L N \{E\} = \{E\}(N) = k\). We therefore conclude that \(\langle x := E, M \rangle \xrightarrow{\tau} \langle \bullet, M[x\{k\}] \rangle\) if and only if \(\langle x := E, N \rangle \xrightarrow{\tau} \langle \bullet, N[x\{k\}] \rangle\). Moreover \(M[x\{k\}] =_L N[x\{k\}]\).

Case (out \(ch E\), out \(ch E\)). Assume that \(\text{level}(ch) = H\). In this case \(\forall M =_L N\) it must be that \(\langle \text{out} ch E, M \rangle \xrightarrow{\text{ch}[E](M)} \langle \bullet, M \rangle\) if and only if \(\langle \text{out} ch E, N \rangle \xrightarrow{\text{ch}[E](N)} \langle \bullet, N \rangle\). Moreover low \(\text{level}(\text{ch}[E](M)) = \text{low}(\text{ch}[E](M))\) = \(\tau\) since \(\text{level}(ch) = H\).

Assume that \(\text{level}(ch) = L\). Then we know that the derivation \(\Phi \vdash^\text{Reg}_\text{Var} \text{out} ch E \rightarrow \{\ldots, \langle \text{Wr} L, \text{Trm} L, \Phi' \rangle\}\) holds provided that \(\Phi, \{\} \vdash^\text{Reg}_\text{Var} E \rightarrow \{\ldots, \langle \text{L}, \text{n} \rangle, r, \Phi'\}\).
Since the security level of an expression represents the upper bound of the security levels of written registers, which in turns represent the upper bound of the security levels of read variables, the type derivation ensures that \( E \) does not involve variables from \( H \). Hence \( \forall M = L N \ [E](M) = [E](N) = k \). We therefore conclude that \( \langle \text{out ch } E, M \rangle \stackrel{\text{chk}}{\rightarrow} \langle \bullet, M \rangle \) if and only if \( \langle \text{out ch } E, N \rangle \stackrel{\text{chk}}{\rightarrow} \langle \bullet, N \rangle \).

Case (if \( E \) then \( C_t \) else \( C_e \), if \( E \) then \( C_t \) else \( C_e \)). Regardless of the typing derivation used for including the pair in \( A \), for any memory \( M \) two cases are possible: either (if \( E \) then \( C_t \) else \( C_e \), \( M \) \( \leadsto \) \( \langle C_t, M \rangle \)) or (if \( E \) then \( C_t \) else \( C_e \), \( M \) \( \leadsto \) \( \langle C_e, M \rangle \)). Hence, regardless of \( M \), the transition produces a silent action and does not alter the memory. This reduces checking the strong bisimulation condition to checking that the pairs of reduced commands are in \( R \). This aspect is ensured by a careful analysis of the type derivation used to include the pair in \( A \).

An if statement can be typed according to two rules, [if — any] and [if — H].

Assume the rule [if — any] is used. Then we know that the derivation \( \Phi \vdash^{\text{Reg}}_{\text{Var}} C_t \) if \( E \) then \( \langle \ldots \rangle \), \( \langle \text{term}(\lambda) \sqcup t_1 \sqcup t_2, \text{write}(\lambda) \sqcup w_1 \sqcup w_2 \rangle \), \( \Phi_E \) holds under the assumption that \( \Phi_t \models^{\text{Reg}}_{\text{Var}} E \models \langle \ldots \rangle \), \( \langle \lambda, n_g, r, \Phi_1 \rangle \) and \( \Phi_1 \vdash^{\text{Reg}}_{\text{Var}} C_t \models \langle \ldots \rangle \), \( \langle w_1, t_1 \rangle \), \( \Phi_2 \) and \( \Phi_1 \vdash^{\text{Reg}}_{\text{Var}} C_e \models \langle \ldots \rangle \), \( \langle w_2, t_2 \rangle \). Assume that \( \lambda = H \). Then \( \text{write}(\lambda) = H \) and \( w_1 = w_2 = H \). Hence, all possible pairs of reduced terms, namely \( (C_t, C_t), (C_t, C_e), (C_e, C_t) \) and \( (C_e, C_e) \) are in \( H^2 \). Assume that \( \lambda = L \). Since the security level of an expression represents the upper bound of the security levels of written registers, which in turns represent the upper bound of the security levels of read variables, the type derivation ensures that \( E \) does not involve variables from \( H \). Then \( \forall M = L N \) (if \( E \) then \( C_t \) else \( C_e \), \( M \) \( \leadsto \) \( \langle C_*, M \rangle \)) if and only if (if \( E \) then \( C_t \) else \( C_e \), \( M \) \( \leadsto \) \( \langle C_*, N \rangle \)), for \( C_* \in \{ C_t, C_e \} \). Moreover, \( (C_*, C_*) \in A \) follows directly by Proposition 6.

Assume the rule [if — H] is used instead. Then we know that it must be \( \Phi \vdash^{\text{Reg}}_{\text{Var}} C_t \) if \( E \) then \( \langle \ldots \rangle \), \( \langle \text{write}(H), \text{Trm}(m + 1, n_g + \text{max}(n_1, n_2) + 2) \rangle \), \( \Phi_E \) under the assumption that \( \Phi_t \models^{\text{Reg}}_{\text{Var}} C_t \models \langle \ldots \rangle \), \( \langle \text{write}(H), \text{Trm}(m, n_t) \rangle \), \( \Phi_2 \) and \( \Phi_1 \vdash^{\text{Reg}}_{\text{Var}} C_e \models \langle \ldots \rangle \), \( \langle \text{write}(H), \text{Trm}(m, n_e) \rangle \). Hence, as it was concluded in the previous subcase, all possible pairs of reduced terms, namely \( (C_t, C_t), (C_t, C_e), (C_e, C_t) \) and \( (C_e, C_e) \) are in \( H^2 \).

Case (while \( x \) do \( C \), while \( x \) do \( C \)). Regardless of the typing derivation used for including the pair in \( A \), for any memory \( M \) two cases are possible: either it is true that \( \langle \text{while } x \text{ do } C, M \rangle \leadsto \langle \bullet, M \rangle \) or \( \langle \text{while } x \text{ do } C, M \rangle \leadsto \langle C; \text{while } x \text{ do } C, M \rangle \). Hence, regardless of \( M \), the transition produces a silent action and does not alter the memory. This reduces checking the strong bisimulation condition to checking that the pairs of reduced commands are in \( R \). This aspect is ensured by a careful analysis of the type derivation used to include the pair in \( A \). We know that \( \Phi \vdash^{\text{Var}} \text{while } x \text{ do } C \leadsto \ldots \), \( \langle \text{write}(\lambda) \sqcup w, \text{term}(\lambda) \sqcup t \rangle \), \( \Phi_B \) providing that \( \Phi_B \vdash^{\text{Reg}}_{\text{Var}} C \models \langle \ldots \rangle \), \( \langle w, t \rangle \), \( \Phi_E \) and \( \text{write}(\lambda) \sqcup w \) and \( t = \text{Trm} \Rightarrow \text{write}(\lambda) = \text{Trm} \) for \( \lambda = \text{level}(x) = \text{level}(r) \). Assume that \( \lambda = H \). Then \( \text{write}(\lambda) = w = \text{Trm} \), hence all possible pairs of reduced terms, namely \( (C, C), (C, \bullet), (\bullet, C) \) and \( (\bullet, \bullet) \) are in \( H^2 \). Assume that \( \lambda = L \). Then \( \forall M = L N \) (while \( x \) do \( C, M \) \( \leadsto \) \( \langle C_*, M \rangle \)) if and only if (while \( x \) do \( C, N \) \( \leadsto \) \( \langle C_*, N \rangle \)), for \( C_* \in \{ C; \text{while } x \text{ do } C, \bullet \} \). Moreover we can conclude that the pair
Case \((C_1; C_2, C_1; C_2)\). We proceed by cases according to the semantic rule used to reduce the first element of the pair.

Assume \(M\) is considered such that rule \([e - 1]\) is applied. Hence there exists \(C_3 \in \{\text{if } E \text{ then } C_t \text{ else } C_e, \text{while } x \text{ do } C\}\) such that \(C_1; C_2 = R[C_3]\) and \(\langle R[C_3], M \rangle \rightarrow \langle R[C'_3], M' \rangle\), given that \(C_3 \neq \bullet\).

Let us consider \(C_3 = \text{if } E \text{ then } C_t \text{ else } C_e\). As it has been observed previously, for any memory \(M\) two cases are possible: either we have that \(\langle \text{if } E \text{ then } C_t \text{ else } C_e, M \rangle \rightarrow \langle C_t, M \rangle\) or \(\langle \text{if } E \text{ then } C_t \text{ else } C_e, M \rangle \rightarrow \langle C_e, M \rangle\). Hence, regardless of \(M\), the transition produces a silent action and does not alter the memory. We only need to ensure that the pair of reduced commands remains in \(R\).

Assume the rule \(\text{[if − any]}\) was used for typing \(C_3\). Then we know \(\Phi \vdash_{\text{Reg} \ Var} C_3 \rightarrow \{\ldots\}\), \(\langle \text{write}(\lambda) \sqcup w_1 \sqcup w_2, \text{term}(\lambda) \sqcup t_1 \sqcup t_2 \rangle\). \(\Phi_F\) under the assumption that \(\Phi, \{\} \vdash_{\text{Reg} \ Var} E \rightarrow \{\ldots\}, \langle \lambda, n_g \rangle, r, \Phi_1 \text{ and } \Phi_1 \vdash_{\text{Var}} C \rightarrow \{\ldots\}, \langle w_1, t_1 \rangle, \Phi_2\) and \(\Phi_1 \vdash_{\text{Var}} C \rightarrow \{\ldots\}, \langle w_2, t_2 \rangle, \Phi_3\) and write(\(\lambda\)) \(\sqcup w_1\), such that \(\Phi_F = \Phi_2 \cap \Phi_3\).

Assume that \(\lambda = H\). Then write(\(\lambda\)) = \(H\) and \(w_1 = w_2 = H\), hence \(\Phi \vdash_{\text{Reg} \ Var} C_3 \rightarrow \{\ldots\}, \langle \text{Wr} H, \text{Trm} H \rangle, \Phi_F\). Since \(R[C_3]\) is typable, \(\Phi[\star]\) must be typable (Lemma \(\Box\)) and it must have type \(\langle \text{Wr} H, t \rangle\) for an appropriate \(t\). Hence, \(R[C_t]\) must have type \(\langle \text{Wr} H, t'\rangle\) and \(R[C_e]\) must have type \(\langle \text{Wr} H, t''\rangle\) (Proposition \(\Box\)). Therefore all possible pairs of reduced terms, namely \((R[C_t], R[C_t]), (R[C_t], R[C_e]), (R[C_e], R[C_t])\) and \((R[C_e], R[C_e])\) are in \(H^2\). Assume that \(\lambda = L\). Since the security level of an expression represents the upper bound of the security levels of written registers, which in turns represent the upper bound of the security levels of read variables, the type derivation ensures that \(E\) does not involve variables from \(H\). Then for all memories \(N\) such that \(M = L\), \(N\) (if \(E\) then \(C_t\) else \(C_e, M\) \(\rightarrow\) \(C_s, N\)) implies (if \(E\) then \(C_t\) else \(C_e, N\) \(\rightarrow\) \(C_s, N\)), for \(C_s \in \{C_t, C_e\}\). Moreover, by Proposition \(\Box\) \(R[C_s]\) is typable, hence pairs \((R[C_s], R[C_s])\) are in \(A\).

Assume the rule \(\text{[if − H]}\) is used instead. Then we know that the derivation \(\Phi \vdash_{\text{Reg} \ Var} C_3 \rightarrow \{\ldots\}, \langle \text{Wr} H, \text{Trm} (m + 1, n_g + \max(n_t, n_e) + 2) \rangle, \Phi_2 \cap \Phi_3\) holds under the assumption that \(\Phi, \{\} \vdash_{\text{Reg} \ Var} E \rightarrow \{\ldots\}, \langle H, n_g \rangle, r, \Phi_1 \text{ and } \Phi_1 \vdash_{\text{Var}} C_t \rightarrow \{\ldots\}, \langle \text{Wr} H, \text{Trm} (m, n_k), \Phi_2\) and \(\Phi_1 \vdash_{\text{Var}} C_e \rightarrow \{\ldots\}, \langle \text{Wr} H, \text{Trm} (m, n_e), \Phi_3\).

Since \(R[C_3]\) is typable, \(\Phi[\star]\) must be typable in \(\Phi_2 \cap \Phi_3\) (Lemma \(\Box\)). Also, since \(\Phi_1 \sqsubseteq \Phi_2 \cap \Phi_3\), for \(i \in \{2, 3\}\), \(\Phi[\star]\) must be also typable in \(\Phi_2\) and \(\Phi_3\) (Lemma \(\Box\)). Hence all possible pairs of reduced terms, namely \((R[C_t], R[C_t]), (R[C_t], R[C_e]), (R[C_e], R[C_t])\) and \((R[C_e], R[C_e])\) are in \(X^2\).

Let us consider \(C_3 = \text{while } x \text{ do } C\). Since \(C_1; C_2\) is typable, both \(C_3\) and \(R[\bullet]\) must be typable (Lemma \(\Box\)). We know that \(\Phi \vdash_{\text{Reg} \ Var} C_3 \rightarrow \{\ldots\}, \langle \text{write}(\lambda) \sqcup w, \text{term}(\lambda) \sqcup t \rangle, \Phi_B\) for \(\lambda = \text{level}(x) = \text{level}(r)\), providing that \(\Phi_B \vdash_{\text{Reg} \ Var} C \rightarrow \{\ldots\}, \langle w, t \rangle, \Phi_E\) and write(\(\lambda\)) \(\sqcup w\) and \(t = \text{Trm} H \Rightarrow \text{write}(\lambda) = \text{Wr} H\). Assume that \(\lambda = H\). Then write(\(\lambda\)) = \(H\) and \(w = H\), hence \(\Phi \vdash_{\text{Reg} \ Var} C_3 \rightarrow \{\ldots\}, \langle \text{Wr} H, \text{Trm} H \rangle, \Phi_B\) and \(R[\bullet]\) must have type \(\langle \text{Wr} H, t \rangle\) for an appropriate \(t\). Since we know, for the assumption on \(M\), that \(\langle R[C_3], M \rangle \rightarrow \langle R[C; C_3], M \rangle\) it must be, by Proposition \(\Box\) that
also \( R[C; C_3] \) has type \( \langle \text{Wr } H, t' \rangle \), for a suitable \( t' \). Hence, for all memories \( N \) such that \( M = L, N \), either \( \langle R[C_3], N \rangle \vdash (R[C; C_3], N) \) and \( \langle R[C; C_3], R[C; C_3] \rangle \) is in \( H^2 \), or \( \langle R[C_3], N \rangle \vdash (\bullet, N) \) and therefore \( \langle R[C; C_3], R[\bullet] \rangle \) is in \( H^2 \). Assume that \( \lambda = L \). Then for all memories \( N \) such that \( M = L, N \langle R[C_3], N \rangle \vdash (R[C; C_3], N) \). By Proposition\(^4\) \( R[C; C_3] \) is typable, hence the pair \( \langle R[C; C_3], R[C; C_3] \rangle \) is in \( A \).

Assume the rule \([c - 2]\) is applied instead. Hence there exist two commands \( C_3 \) and \( C_4 \) such that \( C_1; C_2 \equiv R[C_3; C_4] \) and \( \langle R[C_3; C_4], M \rangle \xrightarrow{\text{L}} \langle R[C_4], M' \rangle \), given that \( \langle C_3, M \rangle \xrightarrow{\text{L}} (\bullet, M') \). We distinguish two cases. Assume \( C_3 \) is typable. Since \( C_1; C_2 \) is typable, both \( C_3 \) and \( R[C_4] \) must be typable (Lemma\(^3\)). We know that \( \Phi \vdash_{\text{Var}} C_3 \equiv \{ \ldots \} \), \( \langle \text{write}(\lambda) \sqcup w, \text{term}(\lambda) \sqcup t \rangle \), \( \Phi_B \)

for \( \lambda = \text{level}(x) = \text{level}(r) \), providing that \( \Phi_B \vdash_{\text{Var}} C \equiv \{ \ldots \}, \langle w, t \rangle, \Phi_E \) and \( \text{write}(\lambda) \sqcup w \) and \( t = \text{Trm} H \Rightarrow \text{write}(\lambda) = \text{Wr } H \). Assume that \( \lambda = H \). Then write(\lambda) = H and \( w = H \), hence \( \Phi \vdash_{\text{Var}} C_3 \equiv \{ \ldots \} \), \( \langle \text{Wr } H, \text{Trm } H \rangle \), \( \Phi_B \) and \( \Phi_B \vdash_{\text{Var}} C \equiv \{ \ldots \}, \langle \text{Wr } H, t \rangle, \Phi_E \). Since \( R[C_4] \) is typable (Proposition\(^4\)), \( R[\bullet] \) must have type \( \langle \text{Wr } H, t \rangle \) for an appropriate \( t \). This implies that also \( R[C_3; C_4] \) has type \( \langle \text{Wr } H, \text{Trm } H \rangle \). Hence, for all memories \( N \) such that \( M = L, N \), either \( \langle R[C_3; C_4], N \rangle \xrightarrow{\text{L}} \langle R[C; C_3; C_4], N \rangle \) and \( \langle R[C_4], R[C; C_3; C_4] \rangle \) is in \( H^2 \), or we have that \( \langle R[C_3; C_4], N \rangle \xrightarrow{\text{L}} \langle R[C_3; C_4], N \rangle \) and \( \langle R[C_4], R[C_3; C_4] \rangle \) is in \( H^2 \). Assume that \( \lambda = L \).

Then for all memories \( N \) such that \( M = L, N \langle R[C_3; C_4], N \rangle \xrightarrow{\text{L}} \langle R[C_3; C_4], N \rangle \). By Proposition\(^4\) \( R[C_4] \) is typable, hence the pair \( \langle R[C_3; C_4], R[C_3; C_4] \rangle \) is in \( A \).

**Part 2.**

Let \( C \in H \) such that \( C \neq \bullet \). Lemma\(^9\) ensures that, for any memory \( M, C \) does not produce an action different than \( \tau \) or alter the low part of \( M \). Proposition\(^4\) ensures that the reduced command remains in \( H \). Also, recall that \( \langle \bullet, M \rangle \xrightarrow{\text{L}} \langle \bullet, M \rangle \). This suffices to show that, according to the termination transparent semantics of \texttt{while}, all pairs in \( H^2 \) perform transitions that correspond to low equivalent actions, in which low equality of memories is preserved and such that reduced pairs of commands are still in \( H^2 \).

**Part 3.**

We complete the proof by showing that pairs in \( X \) perform transitions that correspond to low equivalent actions and preserve low equality of memories. Also, we show that transitions are performed towards pairs of commands that are either in \( X \) or in \( A \). Let \( \langle R[C_1], R[C_2] \rangle \in X \). By definition there must exist \( \Phi_1 \) and \( \Phi_2 \) such that the following derivation are correct:

\[
\Phi_1 \vdash_{\text{Var}} C_1 \Leftarrow \{ \ldots \}, \langle \text{Wr } H, \text{Trm } (m, n_1) \rangle, \Phi'_1 \\
\Phi_2 \vdash_{\text{Var}} C_2 \Leftarrow \{ \ldots \}, \langle \text{Wr } H, \text{Trm } (m, n_2) \rangle, \Phi'_2 \\
\Phi'_1 \sqcap \Phi'_2 \vdash_{\text{Var}} R[\bullet] \Leftarrow \{ \ldots \}, \langle w, t \rangle, \Phi_3
\]
Consider $M = L N$ such that $(C_1, M) \xrightarrow{L} (C'_1, M')$ and $(C_2, N) \xrightarrow{L} (C'_2, N')$. Lemma 2 ensures that $\text{low}(l_1) = \text{low}(l_2) = r$ and $M' = L N'$. If $m = 1$ then both $C'_1$ and $C'_2$ are $\ast$ and $\Phi'_1 \sqcap \Phi'_2 \vdash_{\text{Reg}} R[\ast] \rightarrow \{\ldots, \langle w, t \rangle \}$, $\Phi_3$ ensures that $(R[\ast], R[\ast]) \in R$. If $m > 1$ then Lemma 10 ensures that there exists $\Phi_\alpha$ and $\Phi_\beta$ for which the following derivations are correct

$$\Phi_\alpha \vdash_{\text{Reg}} C'_1 \rightarrow \{\ldots, \langle W H, \text{Trm} (m - 1, n'_1) \rangle, \Phi'_\alpha \}
\Phi_\beta \vdash_{\text{Reg}} C'_2 \rightarrow \{\ldots, \langle W H, \text{Trm} (m - 1, n'_2) \rangle, \Phi'_\beta \}$$

for $\Phi'_\alpha \Vdash \Phi'_1$ and $\Phi'_\beta \Vdash \Phi'_2$. Hence it is true that $(R[C'_1], R[C'_2]) \in X$ because $\Phi_\alpha \vdash_{\text{Reg}} R[C'_1] \rightarrow \{\ldots, \langle w_\alpha, t_\alpha \rangle, \Phi'_\alpha \}$ (Lemmas 8 and 9), $\Phi_\beta \vdash_{\text{Reg}} R[C'_2] \rightarrow \{\ldots, \langle w_\beta, t_\beta \rangle, \Phi'_\beta \}$ (Lemmas 8 and 9) and $\Phi'_\alpha \sqcap \Phi'_\beta \vdash_{\text{Reg}} R[\ast] \rightarrow \{\ldots, \langle w_c, t_c \rangle, \Phi_c \}$ (Lemma 6).

We have shown that a type-correct while program is strongly secure. We now have to show that the type system in Figures 17 and 18 translates a secure while program into a secure $\text{i}-\text{while}$ program. Since $\text{i}-\text{while}$ programs form a subclass of while programs, this can be shown by retyping a translated program and showing it is indeed type-correct.

In order to state this result formally, we consider that now programs have variables in the set $\text{Var}' = \text{Var} \cup \text{Reg}$. Moreover, from the set of register variables $\text{Reg} = \{r_1, \ldots, r_n\}$ we define a new set of register variables, $\text{Reg}' = \{s_1, \ldots, s_n\} \cup \{s'_1, \ldots, s'_n\}$, such that for a (former) register variable $r_i$ there are a corresponding register variable $\text{corr}(r_i) = s_i$ and a corresponding shadow variable $\text{shw}(r_i) = s'_i$. We assume that $\text{level}(r_i) = \text{level}(s_i) = \text{level}(s'_i)$.

In order to show that the code $D$ obtained from the compilation of a while program $C$ is retypable, we proceed via a stronger property. In particular we show that the recompilation of $D$ (i) maps two related input register records into two related output register records and (ii) computes a security annotation which is equivalent (up-to slowdown) to the one corresponding to $D$. We formalize the first aspect as follows.

**Definition 19 (Register Correspondence).** Let $\Phi$ and $\Phi'$ be two record registers defined over $\text{Reg}$ and $\text{Reg}'$ respectively. We say that they are corresponding, written as $\Phi \Rightarrow \Phi'$, if:

- $[r_i \xrightarrow{W} x] \in \Phi \Rightarrow [s_i \xrightarrow{W} x] \in \Phi'$
- $[r_i \xleftarrow{W} x] \in \Phi \Rightarrow [s_i \xrightarrow{W} r] \in \Phi'$

Notice that for any register variable $r_i$ associated in $\Phi$ we explicitly require the corresponding register variable $s_i$ (not the shadow register variable $s'_i$) to be associated in $\Phi'$.

In order to state and prove the result about recompilation of compiled programs, we begin by stating an auxiliary result that formalize the type correctness of the code corresponding to the evaluation of a while expression.

**Proposition 5 (Retyping of expressions).** Let $E$ be a while expression such that there exists $\Phi$ for which $\Phi, A \vdash_{\text{Reg}} E \rightarrow \{D\}, \langle \lambda, n \rangle, r, \Phi_\alpha$ holds. Then for all $\Phi'$ such
that \( \Phi \overset{\sim}{\rightarrow} \Phi' \) we have that there exists a derivation \( \Phi' \vdash_{\mathit{Var}'} D \twoheadrightarrow \{D'\}, \langle w, t \rangle, \Phi'_\alpha \) such that \( \Phi'_\alpha \overset{\sim}{\rightarrow} \Phi'_\alpha \) and:

- if \( \lambda = H \) or \( n = 0 \), then \( w = \mathit{Wr} H \) and \( t = \langle n, p \rangle \);
- if \( \lambda = L \) and \( n > 0 \), then \( w = \mathit{Wr} L \) and \( t = \mathit{Trm} L \).

Proof. We prove the proposition by induction on the structure of \( E \) and by cases on the last rule applied in the type derivation.

**Base case**

Case \( E = k \). Assume the following derivation exists

\[
\begin{align*}
\Phi, A \vdash_{\mathit{Reg}} & \quad k \rightarrow \{r := k\}, \langle H, 1 \rangle, r, \Phi[r \not\rightarrow] \\
\phi \in \mathit{Reg} & \quad \phi \notin A \quad \text{level}(r) = H
\end{align*}
\]

and consider \( \Phi' \), such that \( \Phi \overset{\sim}{\rightarrow} \Phi' \), together with \( s = \mathit{corr}(r) \). Then the following derivation exists.

\[
\begin{align*}
\Phi' \vdash_{\mathit{Reg}'} & \quad k \rightarrow \{s := k\}, \langle H, 1 \rangle, s, \Phi'[s \not\rightarrow] \\
\phi' \in \mathit{Reg}' & \quad \phi' \notin A \quad \text{level}(s) = H
\end{align*}
\]

We have that \( \Phi[r \not\rightarrow] \overset{\sim}{\rightarrow} \Phi'[s \rightarrow r] \) because:

- for any \( r' \neq r \), if \( [r' \rightarrow x] \in \Phi[r \not\rightarrow] \) then \( [s' \rightarrow x] \in \Phi'[s \rightarrow r] \) because \( s' \neq \mathit{corr}(r) \);
- for any \( r' \neq r \), if \( [r' \rightarrow x] \in \Phi[r \not\rightarrow] \) then \( [s' \rightarrow r'] \in \Phi'[s \rightarrow r] \) because \( s' \neq \mathit{corr}(r) \);
- \( r \) is unassociated in \( \Phi[r \not\rightarrow] \).

Assume the following derivation exists

\[
\begin{align*}
\Phi, A \vdash_{\mathit{Reg}} & \quad k \rightarrow \{r := k\}, \langle L, 1 \rangle, r, \Phi[r \not\rightarrow] \\
\phi \in \mathit{Reg} & \quad \phi \notin A \quad \text{level}(r) = L
\end{align*}
\]

instead and consider \( \Phi' \), such that \( \Phi \overset{\sim}{\rightarrow} \Phi' \), together with \( s = \mathit{corr}(r) \). Then the following derivation exists

\[
\begin{align*}
\Phi' \vdash_{\mathit{Reg}'} & \quad k \rightarrow \{s := k\}, \langle L, 1 \rangle, s, \Phi'[s \not\rightarrow] \\
\phi' \in \mathit{Reg}' & \quad \phi' \notin A \quad \text{level}(s) = L
\end{align*}
\]

We have that \( \Phi[r \not\rightarrow] \overset{\sim}{\rightarrow} \Phi'[s \rightarrow r] \) because:

- for any \( r' \neq r \), if \( [r' \rightarrow x] \in \Phi[r \not\rightarrow] \) then \( [s' \rightarrow x] \in \Phi'[s \rightarrow r] \) because \( s' \neq \mathit{corr}(r) \);
– for any \( r' \neq r \), if \( [r' \xrightarrow{R} x] \in \Phi[r \not\in] \) then \( [s' \xrightarrow{W} r'] \in \Phi'[s \xrightarrow{W} r] \) because \( s' \neq \text{corr}(r) \);
– \( r \) is unassociated in \( \Phi[r \not\in] \).

Case \( E = x \). Assume the following derivation exists

\[
\begin{align*}
x &\in \text{Var} \\
r &\in \text{Reg} \\
[r \leftrightarrow x] &\in \Phi
\end{align*}
\]

and consider \( \Phi' \) such that \( \Phi \equiv \Phi' \). Then the following derivation exists

\[
\Phi' \vdash \text{Reg}'_\text{Var}, r \mapsto \{\bullet\}, (\text{Wr } H, \text{Trm } (0, 0)), \Phi'
\]

Assume the following derivation exists instead

\[
\begin{align*}
x &\in \text{Var} \\
r &\in \text{Reg} \\
r &\not\in A \\
\text{level}(r) &\equiv \text{level}(x)
\end{align*}
\]

\[
\Phi, A \parallel \text{Reg}'_\text{Var} x \mapsto \{r := x\}, (H, 1), r, \Phi[r \xrightarrow{R} x]
\]

Then for \( \Phi' \), such that \( \Phi \equiv \Phi' \) and \( s = \text{corr}(r) \) the following derivation exists

\[
\begin{align*}
s &\in \text{Reg}' \\
\text{level}(s) &\equiv H
\end{align*}
\]

\[
\Phi', \{\} \parallel \text{Reg}'_\text{Var} x \mapsto \{s := x\}, (H, 1), s, \Phi'[s \xrightarrow{R} x]
\]

\[
\Phi' \vdash \text{Reg}'_\text{Var}, r := x \mapsto \{s := x; r := s\}, (\text{Wr } H, \text{Trm } (1, 2)), \Phi'[s \xrightarrow{W} r]
\]

We have that \( \Phi[r \xrightarrow{R} x] \equiv \Phi'[s \xrightarrow{W} r] \):

– for any \( r' \neq r \) and \( y \neq x \), if \( [r' \xrightarrow{W} y] \in \Phi[r \xrightarrow{R} x] \) then \( [s' \xrightarrow{W} y] \in \Phi'[s \xrightarrow{W} r] \) because \( s' \neq \text{corr}(r) \);

– for any \( r' \neq r \) and \( y \neq x \), if \( [r' \xrightarrow{R} y] \in \Phi[r \xrightarrow{R} x] \) then \( [s' \xrightarrow{W} r'] \in \Phi'[s \xrightarrow{W} r] \) because \( s' \neq \text{corr}(r) \);

– \( [r \xrightarrow{R} x] \in \Phi[r \xrightarrow{R} x] \) and \( [s \xrightarrow{W} r] \in \Phi'[s \xrightarrow{W} r] \).

If

\[
\begin{align*}
x &\in \text{Var} \\
r &\in \text{Reg} \\
r &\not\in A \\
\text{level}(r) &\equiv \text{level}(x)
\end{align*}
\]

\[
\Phi, A \parallel \text{Reg}'_\text{Var} x \mapsto \{r := x\}, (L, 1), r, \Phi[r \xrightarrow{R} x]
\]

then for \( s = \text{corr}(r) \) and \( \Phi' \) such that \( \Phi \equiv \Phi' \) the following derivation exists

\[
\begin{align*}
s &\in \text{Reg}' \\
\text{level}(s) &\equiv L
\end{align*}
\]

\[
\Phi', \{\} \parallel \text{Reg}'_\text{Var} x \mapsto \{s := x\}, (L, 1), s, \Phi'[s \xrightarrow{R} x]
\]

\[
\Phi' \vdash \text{Reg}'_\text{Var}, r := x \mapsto \{s := x; r := s\}, (\text{Wr } L, \text{Trm } L), \Phi'[s \xrightarrow{W} r]
\]

We have that \( \Phi[r \xrightarrow{R} x] \equiv \Phi'[s \xrightarrow{W} r] \):
– for any \( r' \neq r \) and \( y \neq x \), if \( [r' \xrightarrow{W} y] \in \Phi[r \xrightarrow{R} x] \) then \( [s' \xrightarrow{W} y] \in \Phi'[s \xrightarrow{W} r] \) because \( s' \neq \text{corr}(r) \);

– for any \( r' \neq r \) and \( y \neq x \), if \( [r' \xleftarrow{R} y] \in \Phi[r \xrightarrow{R} x] \) then \( [s' \xrightarrow{W} r'] \in \Phi'[s \xrightarrow{W} r] \) because \( s' \neq \text{corr}(r) \);

– \( [r \xrightarrow{R} x] \in \Phi[r \xrightarrow{R} x] \) and \( [s \xrightarrow{W} r] \in \Phi'[s \xrightarrow{W} r] \).

### Inductive Step

Case \( E = E_1 \circ E_2 \).

Consider that the following derivation exists

\[
\begin{align*}
\Phi, A \parallel^\text{Reg} E_1 \& \Phi_1, A \cup \{r\} \parallel^\text{Reg} E_2 \& \Phi_2 \\
H = \text{level}(r) = \text{level}(r_a)
\end{align*}
\]

and consider \( \Phi' \) such that \( \Phi \equiv \Phi' \). Then the following derivations exist by inductive hypothesis

\[
\begin{align*}
\Phi', A \parallel^\text{Reg} E_1 \& \Phi_1', A \cup \{r\} \parallel^\text{Reg} E_2 \& \Phi_2'
\end{align*}
\]

such that \( \Phi_2 \equiv \Phi_2' \). In order for completing the case, we have to show that \( \Phi_2' \parallel^\text{Var'} E_2 \)

\[
\begin{align*}
E_2 \parallel^\text{Reg'} r := r \circ r_a \rightarrow \{D', \langle H, \text{Trm}(1, p) \rangle, \Phi_3 \}
\end{align*}
\]

such that \( \Phi_2[\] \equiv \Phi_3 \). We distinguish four cases.

Case 1: there exist \( [r \xrightarrow{R} x], [r_a \xrightarrow{R} y] \in \Phi_2 \). Since \( \Phi_2 \equiv \Phi_2' \), then we know \( [s \xrightarrow{W} r], [s_a \xrightarrow{W} r_a] \in \Phi_2' \) and the following type derivation exists

\[
\begin{align*}
\Phi_2', \} \parallel^\text{Reg'} r \circ r_a \rightarrow \{s := s \circ s_a; r := s \}, \langle W, H, \text{Trm}(1, 2) \rangle, \Phi_2'[s \xrightarrow{W} r]
\end{align*}
\]

We have that \( \Phi_2[\] \equiv \Phi_2'[s \xrightarrow{W} r] \):

– for any \( r'' \neq r \), if \( [r'' \xrightarrow{W} z] \in \Phi_2[r \xrightarrow{W} z] \) then \( [s'' \xrightarrow{W} z] \in \Phi_2'[s \xrightarrow{W} r] \) because \( s'' \neq \text{corr}(r) \);

– for any \( r'' \neq r \), if \( [r'' \xrightarrow{R} z] \in \Phi_2[r \xrightarrow{R} z] \) then \( [s'' \xrightarrow{W} r'] \in \Phi_2'[s \xrightarrow{W} r] \) because \( s'' \neq \text{corr}(r) \);

– \( r \) is unassociated in \( \Phi_2[r \xrightarrow{W}] \).

Case 2: there exists \( [r \xleftarrow{R} x] \in \Phi_2 \) but there is not \( [r_a \xrightarrow{R} y] \in \Phi_2 \). We therefore distinguish two further subcases.
Case 2a: \( r_a \) is unassociated in \( \Phi_2 \). Since \( \Phi_2 \models \Phi_2' \) we know \([s \xrightarrow{W} r] \in \Phi_2'\) and the following type derivation for \( s_a = \text{corr}(r_a) \) exists

\[
\Phi_2', \{s\} \vdash_{\text{Reg'}} r_a \leftarrow \{s_a := r_a\};\quad \langle H, 1\rangle, s, \Phi_2'[s_a \xleftarrow{R} r_a] \quad \text{level}(s) = H
\]

We have that \( \Phi_2[r \not\models \chi] \equiv \Phi_2'[s \xrightarrow{W} r][s_a \xleftarrow{R} r_a] \):

- for any \( r'' \) such that \( r'' \neq r \) and \( r'' \neq r_a \), if \([r'' W z] \in \Phi_2[r \not\models \chi]\) then \([s'' W z] \in \Phi_2'[s \xrightarrow{W} r][s_a \xleftarrow{R} r_a]\) because \( s'' \neq \text{corr}(r) \) and \( s'' \neq \text{corr}(r_a) \);
- for any \( r'' \) such that \( r'' \neq r \) and \( r'' \neq r_a \), if \([r'' R z] \in \Phi_2[r \not\models \chi]\) then \([s'' W r''] \in \Phi_2'[s \xrightarrow{W} r][s_a \xleftarrow{R} r_a]\) because \( s'' \neq \text{corr}(r) \) and \( s'' \neq \text{corr}(r_a) \);
- \( r \) and \( r_a \) are unassociated in \( \Phi_2[r \not\models \chi] \).

Case 2b: there exists \([r_a \xrightarrow{W} y] \in \Phi_2 \). Since \( \Phi_2 \models \Phi_2' \) we know \([s \xrightarrow{W} r] \in \Phi_2'\) and \([s_a \xrightarrow{W} y] \in \Phi_2'\) and the following type derivation exists for \( s'_a = \text{shw}(r_a) \)

\[
\Phi_2', \{s\} \vdash_{\text{Reg'}} r_a \leftarrow \{s_a := r_a\};\quad \langle H, 1\rangle, s', \Phi_2'[s_a \xleftarrow{R} r_a] \quad \text{level}(s) = H
\]

We have that \( \Phi_2[r \not\models \chi] \equiv \Phi_2'[s \xrightarrow{W} r][s'_a \xleftarrow{R} r_a] \):

- for any \( r'' \) such that \( r'' \neq r \) and \( r'' \neq r_a \), if \([r'' W z] \in \Phi_2[r \not\models \chi]\) then \([s'' W z] \in \Phi_2'[s \xrightarrow{W} r][s'_a \xleftarrow{R} r_a]\) because \( s'' \neq \text{corr}(r) \) and \( s'' \neq \text{corr}(r_a) \);
- for any \( r'' \) such that \( r'' \neq r \) and \( r'' \neq r_a \), if \([r'' R z] \in \Phi_2[r \not\models \chi]\) then \([s'' W r''] \in \Phi_2'[s \xrightarrow{W} r][s'_a \xleftarrow{R} r_a]\) because \( s'' \neq \text{corr}(r) \) and \( s'' \neq \text{corr}(r_a) \);
- \( [r_a \xrightarrow{W} y] \in \Phi_2[r \not\models \chi] \) and \([s_a \xrightarrow{W} y] \in \Phi_2'[s \xrightarrow{R} r][s'_a \xleftarrow{R} r_a]\) because \( s'_a = \text{shw}(r_a) \);
- \( r \) is unassociated in \( \Phi_2[r \not\models \chi] \).

Case 3: there exists \([r_a \xrightarrow{R} x] \in \Phi_2 \) but there is not \([r \xrightarrow{R} x] \in \Phi_2 \). We therefore distinguish two further subcases.
Case 3a: \( r \) is unassociated in \( \Phi_2 \). Since \( \Phi_2 \models \Phi_2' \) we know \( [s_a \xrightarrow{W} r_a] \in \Phi_2' \) and the following type derivation for \( s = \text{corr}(r) \) exists:

\[
\begin{align*}
    s, s_a & \in \text{Reg}' \quad \text{level}(s) = H \\
\Phi_2', \{ \} \vdash_{\text{Var}', r} s : \{ s := r \}, (H, 1), s, \Phi_2'[s \leftarrow r] \\
\Phi_2', \{ \} \vdash_{\text{Var}', r \ op \ r_a} \{ s := r; s := s \ op s_a \}, (H, 2), s, \Phi_2'[s \not\rightarrow r]
\end{align*}
\]

We have that \( \Phi_2[\not\rightarrow s] \models \Phi_2'[s \xrightarrow{W} r] \):

- for any \( r'' \) such that \( r'' \neq r \), if \( [r'' \xrightarrow{R} z] \in \Phi_2[\not\rightarrow s] \) then \( [s'' \xrightarrow{W} z] \in \Phi_2'[s \xrightarrow{W} r] \) because \( s'' \not\rightarrow \text{corr}(r) \);
- for any \( r'' \) such that \( r'' \neq r \), if \( [r'' \xrightarrow{R} z] \in \Phi_2[\not\rightarrow s] \) then \( [s'' \xrightarrow{W} r''] \in \Phi_2'[s \xrightarrow{W} r] \) because \( s'' \not\rightarrow \text{corr}(r) \);
- \( r \) is unassociated in \( \Phi_2[\not\rightarrow s] \).

Case 3b: there exists \( [r \xrightarrow{W} x] \in \Phi_2 \). Since \( \Phi_2 \models \Phi_2' \) we know \( [s_a \xrightarrow{W} r_a] \in \Phi_2' \) and \( [s \xrightarrow{W} x] \in \Phi_2 \) so the following type derivation exists for \( s' = \text{shw}(r) \):

\[
\begin{align*}
    s', s_a & \in \text{Reg}' \quad \text{level}(s') = H \\
\Phi_2', \{ \} \vdash_{\text{Var}', r} s' : \{ s' := r \}, (H, 1), s', \Phi_2'[s' \leftarrow r] \\
\Phi_2', \{ \} \vdash_{\text{Var}', r \ op \ r_a} \{ s' := r; s' := s' \ op s_a \}, (H, 2), s', \Phi_2'[s' \not\rightarrow r]
\end{align*}
\]

We have that \( \Phi_2[\not\rightarrow s] \models \Phi_2'[s' \xrightarrow{W} r] \):

- for any \( r'' \) such that \( r'' \neq r \), if \( [r'' \xrightarrow{W} z] \in \Phi_2[\not\rightarrow s] \) then \( [s'' \xrightarrow{W} z] \in \Phi_2'[s' \xrightarrow{W} r] \) because \( s'' \not\rightarrow \text{shw}(r) \);
- for any \( r'' \) such that \( r'' \neq r \), if \( [r'' \xrightarrow{R} z] \in \Phi_2[\not\rightarrow s] \) then \( [s'' \xrightarrow{W} r''] \in \Phi_2'[s' \xrightarrow{W} r] \) because \( s'' \not\rightarrow \text{shw}(r) \);
- \( r \) is unassociated in \( \Phi_2[\not\rightarrow s] \).

Case 4: neither \( [r_a \xrightarrow{R} x] \) nor \( [r_a \xrightarrow{R} y] \) are in \( \Phi_2 \). This case is provable by considering the combined cases 2 and 3.
Consider that the following derivation exists instead

\[
\Phi, A \vdash_{\text{Var}} E_1 \rightsquigarrow \{ D_1 \}, \langle L, n_1 \rangle, r, \Phi_1
\]

\[
\Phi_1, A \cup \{ r \} \vdash_{\text{Var}} E_2 \rightsquigarrow \{ D_2 \}, \langle L, n_2 \rangle, r_a, \Phi_2
\]

\[
L = \text{level}(r) = \text{level}(r_a)
\]

\[
\Phi, A \vdash_{\text{Var}} E_1 \text{ op } E_2 \rightsquigarrow \begin{cases}
D_1; \\
D_2; \\
r := r \text{ op } r_a
\end{cases}, \langle L, n_1 + n_2 + 1 \rangle, r, \Phi_2[r \not\rightarrow]
\]

and consider \( \Phi' \) such that \( \Phi \vdash_{\text{Var}}^{\text{corr}} \Phi' \). Then the following derivations exist by inductive hypothesis

\[
\Phi' \vdash_{\text{Var}'} D_1 \rightsquigarrow \{ D'_1 \}, \langle w_1, t_1 \rangle, \Phi'_1
\]

\[
\Phi'_1 \vdash_{\text{Var}'} D_2 \rightsquigarrow \{ D'_2 \}, \langle w_2, t_2 \rangle, \Phi'_2
\]

such that:

- if \( n_i > 0 \) then \( w_i = \text{Wr} L \) and \( t_i = \text{Trm} L \);
- if \( n_i = 0 \) then \( w_i = \text{Wr} H \) and \( t_i = \text{Trm} (0, 0) \);
- \( \Phi_2 \equiv \Phi'_2 \).

In order for completing the case, we have to show that \( \Phi'_2 \vdash_{\text{Var}'} D := r \text{ op } r_a \rightsquigarrow \{ D' \}, \langle \text{Wr} L, \text{Trm} L \rangle, \Phi_3 \) such that \( \Phi_2[r \not\rightarrow] \equiv \Phi_3 \). In fact, recall that for all \( w \) it holds that \( w \cup \text{Wr} L = \text{Wr} L \) and for any \( t \subseteq \text{Trm} L \) it holds that \( t \cup \text{Trm} L = \text{Trm} L \). We distinguish four cases.

Case 1: there exist \([ r \overset{R}{\rightarrow} x ], [ r_a \overset{R}{\rightarrow} y ] \) \( \in \Phi_2 \). Since \( \Phi_2 \equiv \Phi'_2 \), then we know \([ s \overset{W}{\rightarrow} r ], [ s_a \overset{W}{\rightarrow} r_a ] \) \( \in \Phi'_2 \) and the following type derivation exists

\[
\begin{array}{c}
\Phi'_2, \{ \} \vdash_{\text{Var}'} D := r \text{ op } r_a \rightsquigarrow \langle s := s \text{ op } s_a \rangle, \langle L, 1 \rangle, s, \Phi'_2[s \not\rightarrow]\n\\
\Phi'_2 \vdash_{\text{Var}'} D := r \text{ op } r_a \rightsquigarrow \{ s := s \text{ op } s_a, r := s \}, \langle \text{Wr} L, \text{Trm} L \rangle, \Phi'_2[s \overset{W}{\rightarrow} r]
\end{array}
\]

We have that \( \Phi_2[r \not\rightarrow] \equiv \Phi'_2[s \overset{W}{\rightarrow} r] \):

- for any \( r'' \neq r \), if \([ r'' \overset{W}{\rightarrow} z ] \) \( \in \Phi_2[r \not\rightarrow] \) then \([ s'' \overset{W}{\rightarrow} z ] \) \( \in \Phi'_2[s \overset{W}{\rightarrow} r] \) because \( s'' \neq \text{corr}(r) \);
- for any \( r'' \neq r \), if \([ r'' \overset{R}{\rightarrow} z ] \) \( \in \Phi_2[r \not\rightarrow] \) then \([ s'' \overset{W}{\rightarrow} r'' ] \) \( \in \Phi'_2[s \overset{W}{\rightarrow} r] \) because \( s'' \neq \text{corr}(r) \);
- \( r \) is unassociated in \( \Phi_2[r \not\rightarrow] \).

Case 2: there exists \([ r \overset{R}{\rightarrow} x ] \) \( \in \Phi_2 \) but there is not \([ r_a \overset{R}{\rightarrow} y ] \) \( \in \Phi_2 \). We therefore distinguish two further subcases.
Case 2a: $r_a$ is unassociated in $\Phi_2$. Since $\Phi_2 \equiv \Phi'_2$ we know $[s \overset{W}{\rightarrow} r] \in \Phi'_2$ and the following type derivation for $s_a = \text{corr}(r_a)$ exists

$$
\begin{align*}
&\forall s, s_a \in \text{Reg}' \quad \text{level}(s) = L \\
&\Phi'_2, \{s\} \vdash_{\text{Reg}'} \text{Var}, r_a \Rightarrow \{s_a := r_a\}, \{L, 1\}, s_a, \Phi'_2[s_a \overset{R}{\leftarrow} r_a]
\end{align*}
$$

We have that $\Phi_2[r \not\rightarrow] \equiv \Phi'_2[s \overset{W}{ightarrow} r][s_a \overset{R}{\leftarrow} r_a]$:

- for any $r''$ such that $r'' \neq r$ and $r'' \neq r_a$, if $[r'' \overset{W'}{\rightarrow} z] \in \Phi_2[r \not\rightarrow]$ then $[s' \overset{W'}{\rightarrow} z] \in \Phi'_2[s \overset{W}{\rightarrow} r][s_a \overset{R}{\leftarrow} r_a]$ because $s'' \neq \text{corr}(r)$ and $s'' \neq \text{corr}(r_a)$;

- for any $r''$ such that $r'' \neq r$ and $r'' \neq r_a$, if $[r'' \overset{R}{\leftarrow} z] \in \Phi_2[r \not\rightarrow]$ then $[s' \overset{W}{\rightarrow} r'''] \in \Phi'_2[s \overset{W}{\rightarrow} r][s_a \overset{R}{\leftarrow} r_a]$ because $s'' \neq \text{corr}(r)$ and $s'' \neq \text{corr}(r_a)$;

- $r$ and $r_a$ are unassociated in $\Phi_2[r \not\rightarrow]$.

Case 2b: there exists $[r_a \overset{W}{\rightarrow} y] \in \Phi_2$. Since $\Phi_2 \equiv \Phi'_2$ we know $[s \overset{W}{\rightarrow} r] \in \Phi'_2$ and $[s_a \overset{W}{\rightarrow} y] \in \Phi'_2$ and the following type derivation exists for $s'_a = \text{shw}(r_a)$

$$
\begin{align*}
&\forall s, s'_a \in \text{Reg}' \quad \text{level}(s) = L \\
&\Phi'_2, \{s\} \vdash_{\text{Reg}'} \text{Var}, r_a \Rightarrow \{s'_a := r_a\}, \{L, 1\}, s'_a, \Phi'_2[s'_a \overset{R}{\leftarrow} r_a]
\end{align*}
$$

We have that $\Phi_2[r \not\rightarrow] \equiv \Phi'_2[s \overset{W}{\rightarrow} r][s'_a \overset{R}{\leftarrow} r_a]$:

- for any $r''$ such that $r'' \neq r$ and $r'' \neq r_a$, if $[r'' \overset{W'}{\rightarrow} z] \in \Phi_2[r \not\rightarrow]$ then $[s' \overset{W'}{\rightarrow} z] \in \Phi'_2[s \overset{W}{\rightarrow} r][s_a \overset{R}{\leftarrow} r_a]$ because $s'' \neq \text{corr}(r)$ and $s'' \neq \text{shw}(r_a)$;

- for any $r''$ such that $r'' \neq r$ and $r'' \neq r_a$, if $[r'' \overset{R}{\leftarrow} z] \in \Phi_2[r \not\rightarrow]$ then $[s' \overset{W}{\rightarrow} r'''] \in \Phi'_2[s \overset{W}{\rightarrow} r][s_a \overset{R}{\leftarrow} r_a]$ because $s'' \neq \text{corr}(r)$ and $s'' \neq \text{shw}(r_a)$;

- $[r_a \overset{W}{\rightarrow} y] \in \Phi_2[r \not\rightarrow]$ and $[s_a \overset{W}{\rightarrow} y] \in \Phi'_2[s \overset{W}{\rightarrow} r][s'_a \overset{R}{\leftarrow} r_a]$ because $s'_a = \text{shw}(r_a)$;

- $r$ is unassociated in $\Phi_2[r \not\rightarrow]$.

Case 3: there exists $[r_a \overset{R}{\leftarrow} x] \in \Phi_2$ but there is not $[r \overset{L}{\rightarrow} x] \in \Phi_2$. We therefore distinguish two further subcases.
Case 3a: $r$ is unassociated in $\Phi_2$. Since $\Phi_2 \equiv \Phi'_2$ we know $[s_a \xrightarrow{W} r_a] \in \Phi'_2$ and the following type derivation for $s = \text{corr}(r)$ exists

\[
\begin{align*}
\Phi'_2, \{\} & \vdash \text{reg}'_{\text{var}}, r \mapsto \{s := r, \langle L, 1 \rangle, s, \Phi'_2[s \xrightarrow{R} r] \} \\
\Phi'_2, \{\} & \vdash \text{reg}'_{\text{var}}, r \mapsto \{s := r; s := s \text{ op } s_a, \langle L, 2 \rangle, s, \Phi'_2[s \not\xrightarrow{W} r] \} \\
\end{align*}
\]

We have that $\Phi_2[r \not\xrightarrow{W}] \equiv \Phi'_2[s \xrightarrow{W} r]$:

- for any $r''$ such that $r'' \neq r$, if $[r'' \xrightarrow{W} z] \in \Phi_2[r \not\xrightarrow{W}]$ then $[s'' \xrightarrow{W} z] \in \Phi'_2[s \xrightarrow{W} r]$ because $s'' \neq \text{corr}(r)$;
- for any $r''$ such that $r'' \neq r$, if $[r'' \xrightarrow{R} z] \in \Phi_2[r \not\xrightarrow{W}]$ then $[s'' \xrightarrow{W} r'' \in \Phi'_2[s \xrightarrow{W} r]$ because $s'' \neq \text{corr}(r)$;
- $r$ is unassociated in $\Phi_2[r \not\xrightarrow{W}]$.

Case 3b: there exists $[r \xrightarrow{W} x] \in \Phi_2$. Since $\Phi_2 \equiv \Phi'_2$ we know $[s_a \xrightarrow{W} r_a] \in \Phi'_2$ and $[s \xrightarrow{W} x] \in \Phi'_2$ so the following type derivation exists for $s' = \text{shw}(r)$

\[
\begin{align*}
\Phi'_2, \{\} & \vdash \text{reg}'_{\text{var}}, r \mapsto \{s' := r, \langle L, 1 \rangle, s', \Phi'_2[s' \xrightarrow{R} r] \} \\
\Phi'_2, \{\} & \vdash \text{reg}'_{\text{var}}, r \mapsto \{s' := r; s' := s' \text{ op } s_a, \langle L, 2 \rangle, s', \Phi'_2[s' \not\xrightarrow{W} r] \} \\
\end{align*}
\]

We have that $\Phi_2[r \not\xrightarrow{W}] \equiv \Phi'_2[s' \xrightarrow{W} r]$:

- for any $r''$ such that $r'' \neq r$, if $[r'' \xrightarrow{W} z] \in \Phi_2[r \not\xrightarrow{W}]$ then $[s'' \xrightarrow{W} z] \in \Phi'_2[s' \xrightarrow{W} r]$ because $s'' \neq \text{shw}(r)$;
- for any $r''$ such that $r'' \neq r$, if $[r'' \xrightarrow{R} z] \in \Phi_2[r \not\xrightarrow{W}]$ then $[s'' \xrightarrow{W} r' \in \Phi'_2[s' \xrightarrow{W} r]$ because $s'' \neq \text{shw}(r)$;
- $r$ is unassociated in $\Phi_2[r \not\xrightarrow{W}]$.

Case 4: neither $[r \xrightarrow{R} x]$ nor $[r_a \xrightarrow{R} y]$ are in $\Phi_2$. This case is provable by considering the combined cases 2 and 3.

We can now present the details for the recompilation of $\text{i-while}$ programs. In order to relate the type annotations produced in the two compilations, we consider a relation $\gg \subseteq \mathcal{L}_t \times \mathcal{L}_t$ such that $\text{Trm } H \gg \text{Trm } H$, $\text{Trm } L \gg \text{Trm } L$ and $\text{Trm } (m, n) \gg \text{Trm } (n, p)$. 
**Proposition 6 (Type prediction).** Let $C$ be a while program. If $\Phi \vdash_{Var} C \rightarrow \{D\}, \langle w, t \rangle, \Phi'$, then for any $\Phi_1$ such that $\Phi \equiv \Phi_1$ there exists a derivation $\Phi_1 \vdash_{Var'} D \rightarrow D', \langle w, t' \rangle, \Phi'_1$ such that $t \gg t'$ and $\Phi' \equiv \Phi'_1$.

**Proof.** We prove the proposition by induction on the structure of $C$ and by cases on the last rule applied in the type derivation.

**Base case**
Case $C =$ skip. Assume

$$\Phi \vdash_{Var} \text{skip} \rightarrow \{\text{skip}\}, \langle \text{Wr } H, \text{Trm } (1, 1) \rangle, \Phi$$

and let $\Phi_1$ be a register record such that $\Phi \equiv \Phi_1$. Then the following derivation holds

$$\Phi_1 \vdash_{Var} \text{skip} \rightarrow \{\text{skip}\}, \langle \text{Wr } H, \text{Trm } (1, 1) \rangle, \Phi_1$$

Case $C = x := E$. Assume

$$x \in \text{Var} \quad r \in \text{Reg} \quad \text{level}(r) = H \quad \Phi, \{\} \vdash_{Var} E \rightarrow \{D\}, \langle H, n \rangle, r, \Phi'$$

and let $\Phi_1$ be a register record such that $\Phi \equiv \Phi_1$. By applying Proposition 6 on $E$ we have that $\Phi_1 \vdash_{Var} D \rightarrow \{D'\}, \langle \text{Wt } H, \text{Trm } (n, p) \rangle, \Phi'_1$ such that $\Phi' \equiv \Phi'_1$. We now distinguish two cases.

Case 1: there exists $[r \not\rightarrow z] \in \Phi'$. Then since $\Phi' \equiv \Phi'_1$ there exists $[s \rightarrow W r] \in \Phi'_1$ and the following derivation is correct

$$\Phi_1 \vdash_{Var} D \rightarrow \{D'\}, \langle \text{Wt } H, \text{Trm } (n, p) \rangle, \Phi'_1$$

$$\Phi'_1 \vdash_{Var} x := r \rightarrow \{x := s\}, \langle \text{Wt } H, \text{Trm } (1, 1) \rangle, \Phi'_1[s \rightarrow W x]$$

$$\Phi_1 \vdash_{Var} D; x := r \rightarrow \{D'; x := s\}, \langle \text{Wt } H, \text{Trm } (n + 1, p + 1) \rangle, \Phi'_1[s \rightarrow W x]$$

and $\Phi'[r \rightarrow W x] \equiv \Phi'_1[s \rightarrow W x]$.

Case 2: There is not $[r \not\rightarrow z] \in \Phi'$. We distinguish two further cases.

Case 2a: $r$ is unassociated in $\Phi'$. Then

$$\Phi_1 \vdash_{Var} D \rightarrow \{D'\}, \langle \text{Wt } H, \text{Trm } (n, p) \rangle, \Phi'_1$$

$$\Phi'_1 \vdash_{Var} D; x := r \rightarrow \left\{ \begin{array}{l} D' \\ s := r \\ x := s \end{array} \right\}, \langle \text{Wt } H, \text{Trm } (n + 1, p + 2) \rangle, \Phi'_1[s \rightarrow W x]$$

where

$$s \in \text{Reg} \quad s = \text{corr}(r) \quad s = \text{corr}(r)$$

$$\Phi'_1\{\} \vdash_{Var} r \rightarrow \{s := r\}, \langle 1, \text{Wr } H \rangle, \Phi'_1[s \rightarrow W r]$$

$$(ii) = \Phi'_1 \vdash_{Var} D; x := r \rightarrow \{s := r; x := s\}, \langle \text{Wt } H, \text{Trm } (1, 2) \rangle, \Phi'_1[s \rightarrow W x]$$
and \( \Phi'[r \xrightarrow{w} x] \equiv \Phi'[s \xrightarrow{w} x] \).

Case 2b: \( r \xrightarrow{z} 2 \in \Phi' \). Then since \( \Phi' \equiv \Phi' \) there exists \( s \xrightarrow{z} 2 \in \Phi' \). Then the following derivation is correct

\[
\Phi_1 \vdash_{\text{Var}'} \ D \xrightarrow{d} \{D', \langle \text{Wr } H, \text{Trm } (n, p) \rangle \} ; \Phi'_i
\]

\[
\Phi_1 \vdash_{\text{Var}'} \ D; x := r \leftrightarrow \left\{ \begin{array}{l}
D'; \\
s := r; \\
x := s
\end{array} \right\} \langle \text{Wr } H, \text{Trm } (n + 1, p + 2) \rangle , \Phi'_1 \left[ s \xrightarrow{w} x \right]
\]

where

\[
\begin{align*}
& s \in \text{Reg}' \\
& s = \text{corr}(r) \\
& \Phi'_1 \{ \} \models_{\text{Var}'} r \leftrightarrow \{ s := r \} , \langle 1, \text{Wr } H \rangle , s ; \Phi'_1 \left[ s \xrightarrow{R} r \right]
\end{align*}
\]

\( \Phi_1 \vdash_{\text{Var}'} x := r \leftrightarrow \{ s := r ; x := s \} , \langle \text{Wr } H, \text{Trm } (1, 2) \rangle , \Phi'_1 \left[ s \xrightarrow{w} x \right] \)

and \( \Phi'[r \xrightarrow{w} x] \equiv \Phi'[s \xrightarrow{w} x] \).

Assume

\[
\begin{array}{c}
x \in \text{Var} \\
r \in \text{Reg} \\
\text{level}(r) = L \\
\Phi, \{ \} \models_{\text{Reg}} E \leftrightarrow \{ D \} , \langle L, n \rangle , r , \Phi'
\end{array}
\]

instead, and let \( \Phi_1 \) be a register record such that \( \Phi \equiv \Phi_1 \). By applying Proposition 5 on \( E \) we have that \( \Phi_1 \vdash_{\text{Var}'} D \xrightarrow{d} \{ D' \} , \langle w, t \rangle , \Phi'_1 \) such that:

- if \( n > 0 \) then \( w = \text{Wr } L \) and \( t = \text{Trm } L \);
- if \( n = 0 \) then \( w = \text{Wr } H \) and \( t = \text{Trm } (0, 0) \);
- \( \Phi_2 \equiv \Phi'_2 \).

We now distinguish two cases.

Case 1: there exists \( [r \xrightarrow{R} z] \in \Phi' \). Then since \( \Phi' \equiv \Phi' \) there exists \( s \xrightarrow{z} 2 \in \Phi' \) and the following derivation is correct

\[
\begin{align*}
& \Phi_1 \vdash_{\text{Var}'} D \xrightarrow{d} \{ D' \} , \langle w, t \rangle , \Phi'_1 \\
& \Phi'_1 \vdash_{\text{Var}'} x := r \leftrightarrow \{ x := s \} , \langle \text{Wr } L, \text{Trm } L \rangle , \Phi'_1 \left[ s \xrightarrow{w} x \right]
\end{align*}
\]

and \( \Phi'[r \xrightarrow{w} x] \equiv \Phi'_1 \left[ s \xrightarrow{w} x \right] \).

Case 2: There is not \( [r \xrightarrow{R} z] \in \Phi' \). We distinguish two further cases.

Case 2a: \( r \) is unassociated in \( \Phi' \). Then

\[
\Phi_1 \vdash_{\text{Var}'} D \xrightarrow{d} \{ D' \} , \langle w, t \rangle , \Phi'_1
\]

\[
\Phi_1 \vdash_{\text{Var}'} D; x := r \leftrightarrow \{ D'; s := r ; x := s \} , \langle \text{Wr } L, \text{Trm } L \rangle , \Phi'_1 \left[ s \xrightarrow{w} x \right]
\]
where

\[
(i) = \begin{cases}
\Phi'_{i, \{ \}} \vdash_{\text{Reg}'} r \leftarrow \{ s := r \}, 1, L, s, \Phi'_{i, [s \leftarrow r]}
\end{cases}
\]

and \( \Phi'[r \xrightarrow{W} x] \subseteq \Phi'_1[s \xrightarrow{W} x] \).

Case 2b: \( [r \xrightarrow{W} z] \in \Phi' \). Then since \( \Phi' \supseteq \Phi'_1 \), there exists \( [s \xrightarrow{W} z] \in \Phi'_1 \). Then the following derivation is correct

\[
\Phi_1 \vdash_{\text{Reg}'} D \rightsquigarrow \{ D' \}, \langle w, t \rangle, \Phi'_1
\]

where

\[
(ii) = \begin{cases}
\Phi'_{i, \{ \}} \vdash_{\text{Reg}'} r \leftarrow \{ s := r \}, 1, L, s, \Phi'_{i, [s \leftarrow r]}
\end{cases}
\]

and \( \Phi'[r \xrightarrow{W} x] \subseteq \Phi'_1[s \xrightarrow{W} x] \).

Case 2: There is not \( [r \xrightarrow{R} z] \in \Phi' \). We distinguish two further cases.

Case 2a: \( r \) is unassociated in \( \Phi' \). Then

\[
\Phi_1 \vdash_{\text{Var}'} D \rightsquigarrow \{ D', \langle r, L \rangle, \Phi' \}, \Phi_1
\]

where

\[
\Phi'_{i, \{ \}} \vdash_{\text{Reg}'} x := r \leftarrow \{ s := r; x := s \}, \langle W, L, \text{Trm} L \rangle, \Phi'_1[s \xrightarrow{W} x]
\]

and \( \Phi'[r \xrightarrow{W} x] \subseteq \Phi'_1[s \xrightarrow{W} x] \).

Then since \( \Phi' \supseteq \Phi'_1 \), there exists \( [s \xrightarrow{W} z] \in \Phi'_1 \). Then the following derivation is correct

\[
\Phi_1 \vdash_{\text{Reg}'} D \rightsquigarrow \{ D' \}, \langle w, t \rangle, \Phi'_1
\]

where

\[
(i) = \begin{cases}
\Phi'_{i, \{ \}} \vdash_{\text{Reg}'} r \leftarrow \{ s := r \}, 1, L, s, \Phi'_{i, [s \leftarrow r]}
\end{cases}
\]

and \( \Phi'[r \xrightarrow{W} x] \subseteq \Phi'_1[s \xrightarrow{W} x] \).

Case C = out \( \text{ch} \) \( E \). Assume

\[
\Phi \vdash_{\text{Reg}'} \text{out} \text{ch} E \rightsquigarrow \{ D; \text{out} \text{ch} r \}, \langle W, H, \text{Trm} \{ 1, n + 1 \} \rangle, \Phi'
\]

and let \( \Phi_1 \) be a register record such that \( \Phi' \supseteq \Phi_1 \). By applying Proposition 5 on \( E \) we have that \( \Phi_1 \vdash_{\text{Reg}'} D \rightarrow \{ D' \}, \langle W, H, \text{Trm} \{ n, p \} \rangle, \Phi'_1 \) such that \( \Phi' \supseteq \Phi'_1 \). We now distinguish two cases.

Case 1: there exists \( [r \xrightarrow{R} z] \in \Phi' \). Then since \( \Phi' \supseteq \Phi'_1 \), there exists \( [s \xrightarrow{W} z] \in \Phi'_1 \) and the following derivation is correct

\[
\Phi_1 \vdash_{\text{Reg}'} D \rightarrow \{ D' \}, \langle W, H, \text{Trm} \{ n, p \} \rangle, \Phi'_1
\]

\[
\Phi'_{i, \{ \}} \vdash_{\text{Reg}'} x := r \leftarrow \{ s := r; x := s \}, \langle W, H, \text{Trm} \{ 1, 1 \} \rangle, \Phi'_1
\]

\[
\Phi_1 \vdash_{\text{Reg}'} D; \text{out} \text{ch} r \rightarrow \{ D'; \text{out} \text{ch} s \}, \langle W, H, \text{Trm} \{ n + 1, p + 1 \} \rangle, \Phi'_1
\]

Case 2: There is not \( [r \xrightarrow{R} z] \in \Phi' \). We distinguish two further cases.

Case 2a: \( r \) is unassociated in \( \Phi' \). Then

\[
\Phi_1 \vdash_{\text{Reg}'} D \rightarrow \{ D' \}, \langle W, H, \text{Trm} \{ n, p \} \rangle, \Phi'_1
\]

where

\[
(i) = \begin{cases}
\Phi'_{i, \{ \}} \vdash_{\text{Reg}'} r \leftarrow \{ s := r \}, 1, L, s, \Phi'_{i, [s \leftarrow r]}
\end{cases}
\]

and \( \Phi'[r \xrightarrow{W} x] \subseteq \Phi'_1[s \xrightarrow{W} x] \).
where 

\[(ii) = \begin{align*}
\Phi_1, \{ \} \vdash_{\text{Reg}}^r \varphi, r & \mapsto \{ s := r \}, \langle 1, \text{Wr} H \rangle, s, \Phi'[s \xrightarrow{R} r] \\
\Phi_1' \vdash_{\text{Var}}^r \text{out ch } r & \mapsto \{ s := r; \text{out ch } s \}, \langle \text{Wr} H, \text{Trm} (1, 2) \rangle, \Phi'[s \xrightarrow{R} r]
\end{align*}\]

and \(\Phi' \equiv \Phi'_1[s \xrightarrow{R} r]\) because \(r\) is unassociated in \(\Phi'\).

Case 2b: \([r \xrightarrow{W} z] \in \Phi'\). Then since \(\Phi' \equiv \Phi'_1\) there exists \([s \xrightarrow{W} z] \in \Phi'_1\). Consider 
\(s' = \text{shw}(r)\), then the following derivation is correct 

\[
\Phi_1 \vdash_{\text{Reg}}^r D \rightarrow \{ D' \}, \langle \text{Wr} H, \text{Trm} (n, p) \rangle, \Phi'_1
\]

\[(ii) \]

\[
\Phi_1 \vdash_{\text{Var}}^r D; x := r \rightarrow \left\{ \begin{array}{l}
D' \\
s' := r; \\
\text{out ch } s'
\end{array} \right\}, \langle \text{Wr} H, \text{Trm} (n + 1, p + 2) \rangle, \Phi'_1[s' \xrightarrow{R} r]
\]

where 

\[(ii) = \begin{align*}
\Phi_1, \{ \} \vdash_{\text{Reg}}^r \varphi, r & \mapsto \{ s' := r \}, \langle 1, \text{Wr} H \rangle, s', \Phi'[s' \xrightarrow{R} r] \\
\Phi_1' \vdash_{\text{Var}}^r x := r & \mapsto \{ s' := r; \text{out ch } s' \}, \langle \text{Wr} H, \text{Trm} (1, 2) \rangle, \Phi'_1[s' \xrightarrow{R} r]
\end{align*}\]

and \(\Phi' \equiv \Phi'_1[s' \xrightarrow{R} r]\).

Assume 

\[
\Phi, \{ \} \vdash_{\text{Reg}}^r E \rightarrow \{ D \}, \langle L, n \rangle, r, \Phi'
\]

instead, and let \(\Phi_1\) be a register record such that \(\Phi \rightarrow \Phi_1\). By applying Proposition on \(E\) we have that \(\Phi_1 \vdash_{\text{Reg}}^r D \rightarrow \{ D' \}, \langle w, t \rangle, \Phi'_1\) such that:

- if \(n > 0\) then \(w = \text{Wr} L\) and \(t = \text{Trm} L\);
- if \(n = 0\) then \(w = \text{Wr} H\) and \(t = \text{Trm} (0, 0)\);
- \(\Phi_2 \equiv \Phi'_2\).

We now distinguish two cases.

Case 1: there exists \([r \xrightarrow{R} z] \in \Phi'\). Then since \(\Phi' \equiv \Phi'_1\) there exists \([s \xrightarrow{W} r] \in \Phi'_1\) and the following derivation is correct 

\[
\Phi_1 \vdash_{\text{Reg}}^r D \rightarrow \{ D' \}, \langle w, t \rangle, \Phi'_1
\]

\[
\Phi_1' \vdash_{\text{Var}}^r \text{out ch } r & \mapsto \{ \text{out ch } s \}, \langle \text{Wr} L, \text{Trm} L \rangle, \Phi'_1
\]

\[
\Phi_1 \vdash_{\text{Reg}}^r D; \text{out ch } r \rightarrow \{ D'; \text{out ch } s \}, \langle \text{Wr} L, \text{Trm} L \rangle, \Phi'_1
\]

and \(\Phi' \equiv \Phi'_1\).

Case 2: There is not \([r \xrightarrow{R} z] \in \Phi'\). We distinguish two further cases.
Case 2a: \(r\) is unassociated in \(\Phi'\). Then

\[
\Phi_1 \vdash_{\text{Reg}'} D \hookrightarrow \{D'\}, (w, t), \Phi'_1
\]

\[
\Phi_1 \vdash_{\text{Var}} D; \text{out } x \in \{D'; s := r; \text{out } x \in s\}, (\text{Wr } L, \text{Trm } L), \Phi'_1[s \mapsto r]
\]

where

\[
(ii) = \begin{align*}
\Phi'_{1}, \{\} & \vdash_{\text{Reg}'} r \in \{s := r\}, (1, L), s, \Phi'_1[s \mapsto r] \\
\Phi'_{1} & \vdash_{\text{Var}} \text{out } ch \ r \in \{s := r; \text{out } ch \ s\}, (\text{Wr } L, \text{Trm } L), \Phi'_1[s \mapsto r]
\end{align*}
\]

and \(\Phi' \equiv \Phi'_1[s \mapsto r]\) because \(r\) is unassociated in \(\Phi'\).

Case 2b: \(\{r \xrightarrow{W} z\} \in \Phi'\). Then since \(\Phi' \equiv \Phi'_1\) there exists \([s \xrightarrow{W} z] \in \Phi'_1\). Consider \(s' = \text{shw}(r)\), then the following derivation is correct

\[
\Phi_1 \vdash_{\text{Reg}'} D \hookrightarrow \{D'\}, (w, t), \Phi'_1
\]

\[
\Phi_1 \vdash_{\text{Var}} D; \text{out } r \in \{D'; s' := r; \text{out } ch \ s'\}, (\text{Wr } L, \text{Trm } L), \Phi'_1[s' \mapsto r]
\]

where

\[
(ii) = \begin{align*}
\Phi'_{1}, \{\} & \vdash_{\text{Reg}'} r \in \{s' := r\}, (1, L), s', \Phi'_1[s' \mapsto r] \\
\Phi'_{1} & \vdash_{\text{Var}} \text{out } ch \ r \in \{s' := r; \text{out } ch \ s'\}, (\text{Wr } L, \text{Trm } L), \Phi'_1[s' \mapsto r]
\end{align*}
\]

and \(\Phi' \equiv \Phi'_1[s' \mapsto r]\).

\[\text{Inductive Step}\]

Case \(C = C_1; C_2\). Assume

\[
\Phi \vdash_{\text{Reg}} C_1 \hookrightarrow \{D_1\}, (w_1, t_1), \Phi_\alpha
\]

\[
\Phi_\alpha \vdash_{\text{Var}} C_2 \hookrightarrow \{D_2\}, (w_2, t_2), \Phi_\beta
\]

and let \(\Phi_1\) be a register record such that \(\Phi_1 \equiv \Phi_1\). Then the following type derivation exists

\[
\Phi_1 \vdash_{\text{Reg}'} D_1 \hookrightarrow \{D'_1\}, (w_1, t_1'), \Phi'_1
\]

\[
\Phi'_\alpha \vdash_{\text{Reg}} D_2 \hookrightarrow \{D'_2\}, (w_2, t_2'), \Phi'_\beta
\]

and \(\Phi_\beta \equiv \Phi'_\beta\) by applying the inductive hypothesis on derivations for \(D_1\) and \(D_2\).
Case $C = \text{if } E \text{ then } C_t \text{ else } C_c$. Assume 

\[
\Phi \vdash \text{Reg} \quad \Phi, \{\} \vdash_{\text{Reg}} E \rightarrow \{D_g\}, \langle H, n_g \rangle, r, \Phi_\alpha \\
\Phi_\alpha \vdash_{\text{Var}} C_t \rightarrow \{D_t\}, \langle W H, t_1 \rangle, \Phi_\beta \\
\Phi_\beta \vdash_{\text{Reg}} C_c \rightarrow \{D_c\}, \langle W H, t_2 \rangle, \Phi_\gamma
\]

\[
\Phi \vdash_{\text{Var}} \text{if } E \text{ then } C_t \text{ else } C_c \rightarrow \begin{cases} 
D_g; \\
n \in \text{Reg} \\
\text{if } r \text{ then } D_t; \text{skip} \\
\text{else } D_c; \text{skip}
\end{cases} , \langle W H, \text{Trm} H \rangle, \Phi_\beta \cap \Phi_\gamma
\]

and let $\Phi_1$ be a register record such that $\Phi \equiv \Phi_1$. By applying the Proposition S on $E$ we have that $\Phi_1 \vdash_{\text{Var}'} D_g \rightarrow \{D'_g\}, \langle W H, \text{Trm} (n_g, p_g) \rangle, \Phi'_\alpha$ such that $\Phi_\alpha \equiv \Phi'_\alpha$. We distinguish two cases.

Case 1: there exists $[r \stackrel{R}{\rightarrow} z] \in \Phi_\alpha$. Then since $\Phi_\alpha \equiv \Phi'_\alpha$ there exists $[s \stackrel{W}{\rightarrow} r] \in \Phi'_\alpha$ and the following derivation is correct

\[
\Phi_1 \vdash_{\text{Reg}'} D_g \rightarrow \{D'_g\}, \langle W H, \text{Trm} (n_g, p_g) \rangle, \Phi'_\alpha \\
\Phi'_\alpha \vdash_{\text{Var}'} D_t \rightarrow \{R_t\}, \langle W H, t_1' \rangle, \Phi'_\beta \\
\Phi'_\alpha \vdash_{\text{Var}'} D_c \rightarrow \{R_c\}, \langle W H, t_2' \rangle, \Phi'_\gamma \\
R'_t = R_t; \text{skip}; \text{skip} \\
R'_c = R_c; \text{skip}; \text{skip}
\]

\[
\Phi' \vdash_{\text{Reg}'} \begin{cases} 
D_g; \\
n \in \text{Reg} \\
\text{if } s \text{ then } D_t; \text{skip} \\
\text{else } D_c; \text{skip}
\end{cases} \rightarrow \begin{cases} 
D'_g; \\
n \in \text{Reg} \\
\text{if } s \text{ then } R'_t \\
\text{else } R'_c
\end{cases} , \langle W H, \text{Trm} H \rangle, \Phi'_\beta \cap \Phi'_\gamma
\]

and $\Phi_\beta \cap \Phi_\gamma \equiv \Phi'_\beta \cap \Phi'_\gamma$ because the correspondence between records is preserved by record intersection.

Case 2: There is not $[r \stackrel{R}{\rightarrow} z] \in \Phi_\alpha$. We distinguish two further cases.

Case 2a: $r$ is unassociated in $\Phi_\alpha$. Then the following derivation is correct

\[
\Phi_1 \vdash_{\text{Reg}'} D_g \rightarrow \{D'_g\}, \langle W H, \text{Trm} (n_g, p_g) \rangle, \Phi'_\alpha \\
\Phi'_\alpha \vdash_{\text{Var}'} D_t \rightarrow \{R_t\}, \langle W H, t_1' \rangle, \Phi'_\beta \\
\Phi'_\alpha \vdash_{\text{Var}'} D_c \rightarrow \{R_c\}, \langle W H, t_2' \rangle, \Phi'_\gamma \\
R'_t = R_t; \text{skip}; \text{skip} \\
R'_c = R_c; \text{skip}; \text{skip}
\]

\[
\Phi' \vdash_{\text{Reg}'} \begin{cases} 
D_g; \\
n \in \text{Reg} \\
\text{if } r \text{ then } D_t; \text{skip} \\
\text{else } D_c; \text{skip}
\end{cases} \rightarrow \begin{cases} 
D'_g; \\
n \in \text{Reg} \\
\text{if } s \text{ then } R'_t \\
\text{else } R'_c
\end{cases} , \langle W H, \text{Trm} H \rangle, \Phi'_\beta \cap \Phi'_\gamma
\]
In particular notice that $\Phi_\alpha \equiv \Phi'_\alpha[s \xleftarrow{R} r]$, since $r$ is unassociated in $\Phi_\alpha$ and $\Phi_\beta \sqcap \Phi_\gamma \equiv \Phi'_\beta \sqcap \Phi'_\gamma$ because the correspondence between records is preserved by record intersection.

Case 2b: $[r \xrightarrow{W} z] \in \Phi_\alpha$. Then the following derivation is correct

$$
\begin{align*}
\Phi_1 & \vdash \text{Reg}'_{\text{Var}}, D_g \mapsto \{D'_g\}, \langle \text{Wr} \ H, \text{Trm} \ (n_g, p_g) \rangle, \Phi'_\alpha \\
& \text{if } s' \in \text{Reg}' \\
& \quad \text{then } D_e; \text{skip} \\
& \quad \text{else } D_c; \text{skip} \\
& \quad \mapsto \quad \begin{cases} \\
& D'_g; \\
& \text{if } s' \\
& \quad \text{then } R'_e; \\
& \quad \text{else } R'_e \\
& \langle \text{Wr} \ H, \text{Trm} \ H \rangle, \Phi'_\beta \sqcap \Phi'_\gamma
\end{cases}
\end{align*}
$$

In particular notice that $\Phi_\alpha \equiv \Phi'_\alpha[s' \xleftarrow{R} r]$, since $\Phi_\alpha \equiv \Phi'_\alpha$ and $[r \xrightarrow{W} z] \in \Phi_\alpha$ implies $[s \xrightarrow{W} z] \in \Phi'_\alpha[s' \xleftarrow{R} r]$ and $\Phi_\beta \sqcap \Phi_\gamma \equiv \Phi'_\beta \sqcap \Phi'_\gamma$ because the correspondence between records is preserved by record intersection.

Assume

$$
\begin{align*}
\Phi_\alpha \vdash \text{Reg}'_{\text{Var}}, C_t \leftarrow \{D_t\}, \langle w_1, t_1 \rangle, \Phi_\beta & \quad \Phi_\alpha \vdash \text{Reg}'_{\text{Var}}, C_e \leftarrow \{D_e\}, \langle w_2, t_2 \rangle, \Phi_\gamma
\end{align*}
$$

and let $\Phi_1$ be a register record such that $\Phi_1 \equiv \Phi_1$. By applying the Proposition 5 on $E$ we have that $\Phi_1 \vdash \text{Reg}'_{\text{Var}}, D_g \mapsto \{D'_g\}, \langle w, t \rangle, \Phi'_\alpha$ such that:

- if $n > 0$ then $w = \text{Wr} \ L$ and $t = \text{Trm} \ L$;
- if $n = 0$ then $w = \text{Wr} \ H$ and $t = \text{Trm} \ (0, 0)$;
- $\Phi_\alpha \equiv \Phi'_\alpha$.

We distinguish two cases.

Case 1: there exists $[r \xleftarrow{R} z] \in \Phi_\alpha$. Then since $\Phi_\alpha \equiv \Phi'_\alpha$ there exists $[s \xrightarrow{W} r] \in \Phi'_\alpha$ and
the following derivation is correct
\[
\Phi_1 \vdash_{\text{Reg}'} D_g \mapsto \{D'_g\}, (w, t), \Phi'_\alpha
\]
s \in \text{Reg}'
\Phi'_\alpha \vdash_{\text{Var}'} D_t \mapsto \{R_t\}, (w_1, t'_1), \Phi'_\beta
\]
\[s = \text{corr}(r)\]
\Phi'_\alpha \vdash_{\text{Var}'} D_e \mapsto \{R_e\}, (w_2, t'_2), \Phi'_\gamma
\]
\[R'_t = R_t; \text{skip}; \text{skip}\]
\]
\[R'_e = R_e; \text{skip}; \text{skip}\]

and \(\Phi_\beta \cap \Phi_\gamma \models \Phi'_\beta \cap \Phi'_\gamma\) because the correspondence between records is preserved by record intersection.

Case 2: There is not \(|r \xrightarrow{R} z| \in \Phi_\alpha\). We distinguish two further cases.

Case 2a: \(r\) is unassociated in \(\Phi_\alpha\). Then the following derivation is correct
\[
\Phi_1 \vdash_{\text{Reg}'} D_g \mapsto \{D'_g\}, (w, t), \Phi'_\alpha
\]
s \in \text{Reg}'
\Phi'_\alpha \vdash_{\text{Var}'} D_t \mapsto \{R_t\}, (w_1, t'_1), \Phi'_\beta
\]
\[s = \text{corr}(r)\]
\Phi'_\alpha \vdash_{\text{Var}'} D_e \mapsto \{R_e\}, (w_2, t'_2), \Phi'_\gamma
\]
\[R'_t = R_t; \text{skip}; \text{skip}\]
\]
\[R'_e = R_e; \text{skip}; \text{skip}\]

In particular notice that \(\Phi_\alpha \models \Phi'_\alpha \models \Phi'_\alpha[s \xrightarrow{R} r]\), since \(r\) is unassociated in \(\Phi_\alpha\) and \(\Phi_\beta \cap \Phi_\gamma \models \Phi'_\beta \cap \Phi'_\gamma\) because the correspondence between records is preserved by record intersection.

Case 2b: \(|r \xrightarrow{W} z| \in \Phi_\alpha\). Then the following derivation is correct
\[
\Phi_1 \vdash_{\text{Reg}'} D_g \mapsto \{D'_g\}, (w, t), \Phi'_\alpha
\]
s' \in \text{Reg}'
\Phi'_\alpha \vdash_{\text{Var}'} D_t \mapsto \{R_t\}, (w_1, t'_1), \Phi'_\beta
\]
\[s' = \text{slice}(r)\]
\Phi'_\alpha \vdash_{\text{Var}'} D_e \mapsto \{R_e\}, (w_2, t'_2), \Phi'_\gamma
\]
\[R'_t = R_t; \text{skip}; \text{skip}\]
\]
\[R'_e = R_e; \text{skip}; \text{skip}\]

In particular notice that \(\Phi_\alpha \models \Phi'_\alpha \models \Phi'_\alpha[s' \xrightarrow{R} r]\), since \(r\) is unassociated in \(\Phi_\alpha\) and \(\Phi_\beta \cap \Phi_\gamma \models \Phi'_\beta \cap \Phi'_\gamma\) because the correspondence between records is preserved by record intersection.
In particular notice that $\Phi_\alpha \equiv \Phi'_\alpha [s' \xrightarrow{R} r]$, since $\Phi_\alpha \equiv \Phi'_\alpha$ and $[r \xrightarrow{W} z] \in \Phi_\alpha$ implies $[s \xrightarrow{W} z] \in \Phi'_\alpha [s' \xrightarrow{R} r]$ and $\Phi_\beta \cap \Phi_\gamma \equiv \Phi'_\beta \cap \Phi'_\gamma$ because the correspondence between records is preserved by record intersection.

Assume

$$
\begin{align*}
& r \in \text{Reg} \\
& \Phi \vdash \text{Var} E \rightarrow \{D_g\}, \langle H, n_g \rangle, r, \Phi_\alpha \\
& \Phi_\alpha \vdash \text{Var} C_t \rightarrow \{D_t\}, \langle \text{Wr} H, \text{Trm} (m, n_t) \rangle, \Phi_\beta \\
& \Phi_\alpha \vdash \text{Var} C_e \rightarrow \{D_e\}, \langle \text{Wr} H, \text{Trm} (m, n_e) \rangle, \Phi_\gamma \\
& D'_t = D_t; \text{skip}^{n_e-n_t}; \text{skip} \\
& D'_e = D_e; \text{skip}^{n_e-n_c}; \text{skip} \\
& n = \max(n_t, n_e)
\end{align*}
$$

for $\tau = \text{Trm} (m+1, n_g+n+2)$ and let $\Phi_1$ be a register record such that $\Phi \equiv \Phi_1$. By applying the Proposition 5 on $E$ we have that $\Phi_1 \vdash \text{Var} D_g \rightarrow \{D'_g\}, \langle \text{Wr} H, \text{Trm} (n_g, p_g) \rangle, \Phi'_\alpha$ such that $\Phi_\alpha \equiv \Phi'_\alpha$. We distinguish two cases.

Case 1: there exists $[r \xrightarrow{R} z] \in \Phi_\alpha$. Then since $\Phi_\alpha \equiv \Phi'_\alpha$ there exists $[s \xrightarrow{W} r] \in \Phi'_\alpha$ and the following derivation is correct

$$
\begin{align*}
& \Phi_1 \vdash \text{Var} D_g \rightarrow \{D'_g\}, \langle \text{Wr} H, \text{Trm} (n_g, p_g) \rangle, \Phi'_\alpha \\
& s = \text{corr}(r) \\
& \Phi'_\alpha \vdash \text{Var} D_t \rightarrow \{R_t\}, \langle \text{Wr} H, \text{Trm} (n+1, p_t) \rangle, \Phi'_\beta \\
& \Phi'_\alpha \vdash \text{Var} D_e \rightarrow \{R_e\}, \langle \text{Wr} H, \text{Trm} (n+1, p_e) \rangle, \Phi'_\gamma \\
& R'_t = R_t; \text{skip}^{p_e-p_t}; \text{skip} \\
& R'_e = R_e; \text{skip}^{p_e-p_c}; \text{skip} \\
& p = \max(p_t, p_e)
\end{align*}
$$

Notice that $\tau' = \text{Trm} (n_g, p_g) \cup \text{Trm} (n+2, p+2) = \text{Trm} (n_g + n + 2, p_g + p + 2)$ and $\Phi_\beta \cap \Phi_\alpha \equiv \Phi'_\beta \cap \Phi'_\alpha$ because the correspondence between records is preserved by record intersection.

Case 2: There is not $[r \xrightarrow{R} z] \in \Phi_\alpha$. We distinguish two further cases.
Case 2a: $r$ is unassociated in $\Phi_\alpha$. Then the following derivation is correct

$$
\Phi_1 \vdash_{\text{Reg}'_{\text{Var}'}} D_g \Rightarrow \{D'_g\}, \langle \text{Wr } H, \text{Trm } (n_g, p_g) \rangle, \Phi'_\alpha
$$

$$
s \in \text{Reg}'_{\text{Var}'}, D_a = s := r
$$

$$
\Phi'_\alpha[s \overset{R}{\leftarrow} r] \vdash_{\text{Reg}'_{\text{Var}'}} D_t \Rightarrow \{R_t\}, \langle \text{Wr } H, \text{Trm } (n + 1, p_t) \rangle, \Phi'_\beta
$$

$$
\Phi'_\alpha[s \overset{R}{\leftarrow} r] \vdash_{\text{Reg}'_{\text{Var}'}} D_e \Rightarrow \{R_e\}, \langle \text{Wr } H, \text{Trm } (n + 1, p_e) \rangle, \Phi'_\gamma
$$

$$
R'_t = R_t; \text{skip}^{p_t \leftarrow p_t}; \text{skip}
$$

$$
R'_e = R_e; \text{skip}^{p_e \leftarrow p_e}; \text{skip}
$$

$$
p = \max(p_t, p_e)
$$

for $r' = \text{Trm } (n_g, p_g) \uplus \text{Trm } (n + 2, 1 + p + 2)$. In particular notice that $\text{Trm } (n_g, p_g) \uplus \text{Trm } (n + 2, 1 + p + 2) = \text{Trm } (n_g + n + 2, 1 + p_g + p + 2)$ and $\Phi_\alpha \equiv \Phi'_\alpha[s \overset{R}{\leftarrow} r]$, since $r$ is unassociated in $\Phi_\alpha$ and $\Phi_\beta \sqcap \Phi_\gamma \equiv \Phi'_\beta \sqcap \Phi'_\gamma$ because the correspondence between records is preserved by record intersection.

Case 2b: $[r \overset{W}{\rightarrow} z] \in \Phi_\alpha$. Then the following derivation is correct

$$
\Phi_1 \vdash_{\text{Reg}'_{\text{Var}'}} D_g \Rightarrow \{D'_g\}, \langle \text{Wr } H, \text{Trm } (n_g, p_g) \rangle, \Phi'_\alpha
$$

$$
s' \in \text{Reg}'_{\text{Var}'}, D_a = s' := r
$$

$$
\Phi'_\alpha[s' \overset{R}{\leftarrow} r] \vdash_{\text{Reg}'_{\text{Var}'}} D_t \Rightarrow \{R_t\}, \langle \text{Wr } H, \text{Trm } (n + 1, p_t) \rangle, \Phi'_\beta
$$

$$
\Phi'_\alpha[s' \overset{R}{\leftarrow} r] \vdash_{\text{Reg}'_{\text{Var}'}} D_e \Rightarrow \{R_e\}, \langle \text{Wr } H, \text{Trm } (n + 1, p_e) \rangle, \Phi'_\gamma
$$

$$
R'_t = R_t; \text{skip}^{p_t \leftarrow p_t}; \text{skip}
$$

$$
R'_e = R_e; \text{skip}^{p_e \leftarrow p_e}; \text{skip}
$$

$$
p = \max(p_t, p_e)
$$

for $r' = \text{Trm } (n_g, p_g) \uplus \text{Trm } (n + 2, 1 + p + 2)$. In particular notice that $\text{Trm } (n_g, p_g) \uplus \text{Trm } (n + 2, 1 + p + 2) = \text{Trm } (n_g + n + 2, 1 + p_g + p + 2)$ and $\Phi_\alpha \equiv \Phi'_\alpha[s' \overset{R}{\leftarrow} r]$, since $\Phi_\alpha \equiv \Phi'_\alpha$ and $[r \overset{W}{\rightarrow} z] \in \Phi_\alpha$ implies $[s \overset{W}{\rightarrow} z] \in \Phi'_\alpha[s' \overset{R}{\leftarrow} r]$ and $\Phi_\beta \sqcap \Phi_\gamma \equiv \Phi'_\beta \sqcap \Phi'_\gamma$ because the correspondence between records is preserved by record intersection.
Case $C = \text{while } x \text{ do } C_1$. Assume $H = \text{level}(x) = \text{level}(r)$ and

\[
x \in \text{Var} \quad r \in \text{Reg} \\
A = r := x; x := r; \\
\Phi_a = \Phi[r \xrightarrow{W} x] \\
\Phi_B \sqsubseteq \Phi_a \\
\Phi_B \sqsubseteq \Phi_E[r \xrightarrow{W} x] \\
\Phi_B \upharpoonright_{\text{Reg}} C \leftarrow \{D\}, \langle W_r H, t \rangle, \Phi_E
\]

and let $\Phi_1$ be a register record such that $\Phi \xrightarrow{\rightarrow} \Phi_1$. We now have to show that

\[
\Phi_1 \upharpoonright_{\text{Reg}} \text{ while } x \text{ do } C \leftarrow \left\{ \begin{array}{l}
A; \\
\text{while } r \text{ do } \{D; A; \text{skip}\}
\end{array} \right\}, \langle W_r H, \text{Trm } H \rangle, \Phi_B
\]

and $\Phi_B \xrightarrow{\rightarrow} \Phi'_B$. We begin by constructing the derivation for $A$ as follows

\[
(i) \quad (ii)
\]

\[
\Phi_1 \upharpoonright_{\text{Reg}} r := x; x := r; \leftarrow \left\{ \begin{array}{l}
\{s := x; \} \\
\{r := s; \} \\
x := s;
\end{array} \right\}, \langle W_r H, \text{Trm } (2, 3) \rangle, \Phi_1[s \xrightarrow{W} x]
\]

where

\[
(i) \quad (ii)
\]

\[
\Phi_1 \upharpoonright_{\text{Reg}} r := x \leftarrow \left\{ \begin{array}{l}
s := x; \\
r := s;
\end{array} \right\}, \langle W_r H, \text{Trm } (1, 2) \rangle, \Phi_1[s \xrightarrow{W} r]
\]

\[
\Phi_1[s \xrightarrow{W} r] \upharpoonright_{\text{Reg}} x := r \leftarrow \left\{ x := s; \right\}, \langle W_r H, \text{Trm } (1, 1) \rangle, \Phi_1[s \xrightarrow{W} x]
\]

Notice that $\Phi[r \xrightarrow{W} x] \xrightarrow{\rightarrow} \Phi_1[s \xrightarrow{W} x]$. We now need to show that

\[
\Phi_1[s \xrightarrow{W} x] \upharpoonright_{\text{Reg}} \text{ while } r \text{ do } \{D; A; \text{skip}\} \leftarrow \left\{ \ldots \right\}, \langle W_r H, \text{Trm } H \rangle, \Phi'_B
\]
Consider the following derivation

\[ r \in \text{Var}' \quad s' \in \text{Reg}' \quad s' = \text{shw}(r) \quad A' = s' := r; r := s'; \]
\[ \Phi'_1 = \Phi_1[s \xrightarrow{w} x][s' \xrightarrow{w} r] \quad \Phi'_B \subseteq \Phi'_1 \quad \Phi'_B \subseteq \Phi'_E[s \xrightarrow{w} x][s' \xrightarrow{w} r] \]

(iii) \[ \Phi_1[s \xrightarrow{w} x] \vdash_{\text{Var}'} \]
\[ \text{while } r \text{ do } \{
\begin{array}{l}
D;
\end{array}
\] \[ \begin{array}{l}
s := x;
\end{array} \]
\[ \begin{array}{l}
x := r;
\end{array} \]
\[ \begin{array}{l}
\text{skip; }
\end{array} \]
\[ \quad \equiv \quad \begin{array}{l}
A';
\end{array} \]
\[ \begin{array}{l}
\text{while } s' \text{ do } \{
D';
\end{array} \]
\[ \begin{array}{l}
s := x;
\end{array} \]
\[ \begin{array}{l}
r := s;
\end{array} \]
\[ \begin{array}{l}
x := s;
\end{array} \]
\[ \begin{array}{l}
\text{skip; }
\end{array} \]
\[ , \langle \text{Wr } H, \text{Trm } H \rangle, \Phi'_B \]
\[ \text{\}
\]

Notice that \( \Phi[r \xrightarrow{w} x] \equiv \Phi_1[s \xrightarrow{w} x][s' \xrightarrow{w} r] \equiv \Phi'_1 \), since \( r \) is already in correspondence with \( s \). Consider the smallest \( \Phi'_B \subseteq \Phi'_1 \) such that \( \Phi_B \equiv \Phi'_B \) (the domain of \( \Phi'_B \) is \( \text{corr}(\text{dom}(\Phi_B)) \)). Then the following derivation

(iii) = (iv) (v) (vi) \[
\Phi'_B \vdash_{\text{Reg}'} \]
\[ \begin{array}{l}
D;
\end{array} \]
\[ \begin{array}{l}
s := x;
\end{array} \]
\[ \begin{array}{l}
x := r;
\end{array} \]
\[ \begin{array}{l}
\text{skip; }
\end{array} \]
\[ \quad \equiv \quad \begin{array}{l}
D';
\end{array} \]
\[ \begin{array}{l}
s := x;
\end{array} \]
\[ \begin{array}{l}
r := s;
\end{array} \]
\[ \begin{array}{l}
x := s;
\end{array} \]
\[ \begin{array}{l}
\text{skip; }
\end{array} \]
\[ , \langle \text{Wr } H, \text{Trm } (2, 3) \cup \text{Trm } (1, 1) \rangle, \Phi'_E \]

holds for

(iv) \( \Phi'_B \vdash_{\text{Reg}'} D \equiv \{ D' \}, \langle \text{Wr } H, t' \rangle, \Phi'_E \)

(v) \( \Phi'_E \vdash_{\text{Reg}'} \begin{array}{l}
r := x;
\end{array} \]
\[ \begin{array}{l}
x := r;
\end{array} \]
\[ \begin{array}{l}
\text{skip; }
\end{array} \]
\[ \quad \equiv \quad \begin{array}{l}
s := x;
\end{array} \]
\[ \begin{array}{l}
r := s;
\end{array} \]
\[ \begin{array}{l}
x := s;
\end{array} \]
\[ , \langle \text{Wr } H, \text{Trm } (1, 3) \rangle, \Phi'_E[s \xrightarrow{w} x] \]

(vi) \( \Phi'_E[s \xrightarrow{w} x] \vdash_{\text{Reg}'} \text{skip } \equiv \{ \text{skip} \}, \langle \text{Wr } H, \text{Trm } (1, 1) \rangle, \Phi'_E[s \xrightarrow{w} x] \]

In particular:

- the type derivation (iv) follows from the inductive hypothesis on \( D \), which also guarantees that \( \Phi_E \equiv \Phi'_E \);
- type derivation (v) is identical, up to environment renaming, to the same derivation calculated previously. It also holds that \( \Phi_E[s \xrightarrow{w} x] \equiv \Phi'_E[s \xrightarrow{w} x] \), since \( \Phi_E \equiv \Phi'_E \);
- type derivation (vi) is straightforward.
The case is concluded by observing that $\Phi_B \equiv \Phi'_B$ and $\Phi_B \sqsubseteq \Phi_E[s \xrightarrow{w} x]$ and $\Phi_E[s \xrightarrow{w} x]$ implies that $\Phi'_B \sqsubseteq \Phi'_E[s \xrightarrow{w} x][s' \xrightarrow{w} r]$.

Assume $L = \text{level}(x) = \text{level}(r)$ and

$$x \in \text{Var} \quad r \in \text{Reg}$$
$$A = r := x; x := r;$$
$$\Phi_\alpha = \Phi[r \xrightarrow{w} x]$$
$$\Phi_B \sqsubseteq \Phi_\alpha$$
$$\Phi_B \sqsubseteq \Phi'_E[r \xrightarrow{w} x]$$
$$\Phi_B \vdash_{\text{Reg}} C \rightarrow \{D\}, (w, t), \Phi_E$$

instead. Notice that for $\text{level}(x) = \text{level}(r) = L$ we have that $t$ must be $t \sqsubset \text{Trm} H$, hence $\text{term}(\lambda) \vdash t = \text{Trm} L$. Let $\Phi_1$ be a register record such that $\Phi \equiv \Phi_1$. We now have to show that

$$\Phi_1 \vdash_{\text{Reg}} \begin{cases} A; \\ \text{while } r \text{ do } \{D; A; \text{skip}\} \end{cases} \rightarrow \{\ldots\}; \langle \text{Wr} L, \text{Trm} L \rangle, \Phi_B$$

and $\Phi_B \equiv \Phi'_B$. We begin by constructing the derivation for $A$ as follows

\[
\begin{array}{l}
(i) \quad \Phi_1 \vdash_{\text{Reg}} \begin{cases} A; \\ \text{while } r \text{ do } \{D; A; \text{skip}\} \end{cases} \rightarrow \{\ldots\}; \langle \text{Wr} L, \text{Trm} L \rangle, \Phi_1[s \xrightarrow{w} x] \\
(ii) \quad \Phi_1 \vdash_{\text{Reg}} \begin{cases} x := x; \\ r := s; \\ x := s; \end{cases} \rightarrow \{\text{Wr} L, \text{Trm} L, \Phi_1[s \xrightarrow{w} x]\}
\end{array}
\]

where

$$s \in \text{Reg}'$$
$$s = \text{corr}(r)$$

\[
\begin{array}{l}
(i) = \quad \Phi_1, \{\} \vdash_{\text{Reg}} x \rightarrow \{s := x, \langle L, 1, s, \Phi_1[s \xrightarrow{R} x]\\}, \langle \text{Wr} L, \text{Trm} L \rangle, \Phi_1[s \xrightarrow{w} x] \\
(ii) = \quad \Phi_1[s \xrightarrow{w} r], \{\} \vdash_{\text{Reg}} x := r \rightarrow \{x := s, \langle \text{Wr} L, \text{Trm} L \rangle, \Phi_1[s \xrightarrow{w} x]\}
\end{array}
\]

Notice that $\Phi[r \xrightarrow{w} x] \equiv \Phi_1[s \xrightarrow{w} x]$. We now need to show that

$$\Phi_1[s \xrightarrow{w} x] \vdash_{\text{Reg}} \begin{cases} A; \\ \text{while } r \text{ do } \{D; A; \text{skip}\} \rightarrow \{\ldots\}; \langle \text{Wr} L, \text{Trm} L \rangle, \Phi'_B$$
Consider the following derivation

\[
\begin{align*}
A' &= s' := r; r := s'; \\
\Phi'_E &\sqsubseteq \Phi'_E[x \mapsto x][s' \mapsto r]
\end{align*}
\]

Notice that \(\Phi_E[R \mapsto x] \equiv \Phi_E[R \mapsto x][s' \mapsto r] = \Phi'_E\), since \(r\) is already in correspondence with \(s\). Consider the smallest \(\Phi'_E \sqsubseteq \Phi'_E\) such that \(\Phi'_E \equiv \Phi'_E\) (the domain of \(\Phi'_E\) is \(corr(dom(\Phi_B))\)). Then the following derivation

\[
(iii) =
\begin{align*}
\begin{array}{c}
\Phi'_E \vdash \text{Var}^r \\
\{ \begin{array}{l}
D; \\
\text{skip;}
\end{array} \} \mapsto \{ \begin{array}{l}
D'; \\
\text{skip;}
\end{array} \}
\end{array}
\end{align*}
\]

holds for

\[
(iiv) = \Phi'_E \vdash \text{Var}^r \\
D \mapsto \{D'; \} \mapsto \{w \sqcup \text{Wr} \sqcup \text{Wr} H \sqcup \text{L, \ Trm (1, 1)}, \Phi'_E[s \mapsto x]\}
\]

\[
(v) = \Phi'_E \vdash \text{Var}^r \\
\{ \begin{array}{l}
r := x; \\
x := r;
\end{array} \} \mapsto \{ \begin{array}{l}
s := x; \\
r := s; \\
x := s;
\end{array} \}, \langle \text{Wr} H, \text{Trm (1, 1)} \rangle, \Phi'_E[s \mapsto x]
\]

\[
(vi) = \Phi'_E[s \mapsto x] \vdash \text{Var}^r \mapsto \{\text{skip;}, \langle \text{Wr} H, \text{Trm (1, 1)} \rangle, \Phi'_E[s \mapsto x]\}
\]

In particular:

- the type derivation \((iv)\) follows from the inductive hypothesis on \(D\), which also guarantees that \(\Phi_E \equiv \Phi'_E\);
- type derivation \((v)\) is identical, up to environment renaming, to the same derivation calculated previously. It also holds that \(\Phi_E[s \mapsto x] \equiv \Phi'_E[s \mapsto x]\), since \(\Phi_E \equiv \Phi'_E\);
- type derivation \((vi)\) is straightforward.
The case is concluded by observing that $\Phi_B \supseteq \Phi'_B$ and $\Phi_B \subseteq \Phi_E[s \rightarrow x]$ and $\Phi_E[s \rightarrow x] \supseteq \Phi'_E[s \rightarrow x]$ implies that $\Phi'_B \subseteq \Phi'_E[s \rightarrow x][s' \rightarrow r]$. Also, $w \cup \text{Wr } L \cup \text{Wr } H = \text{Wr } L$ and $t' \cup \text{Trm } L \cup \text{Trm } (1, 1) = \text{Trm } L$ (since $t \gg t'$ and $t \sqsubset \text{Trm } H$ implies that $t' \sqsubset \text{Trm } H$).

Proposition 6 states that the an i-while program obtained from a type-correct while program is also type-correct, and from Preposition 3 we have that any type-correct program is strongly secure. We therefore conclude that the type system in Figures 17 and 18 compiles a while program $C$ into an i-while program $D$ which enjoys Strong Security. Notice that the definition of Strong Security for i-while programs is obtained by considering the semantics of i-while programs as a LTS $\mathcal{S}_{i-w} = \{(\{D, M\}, \rightarrow, \{ch!n|ch \in \{\text{low}, \text{high}\} \text{ and } n \in \mathbb{N}\} \cup \{\tau\})\}$, where $\rightarrow$ is defined by rules in Figure 20 for $\mathcal{V} = \text{Var} \cup \text{Reg}$.

### 1.2 From i-while programs to RISC programs

We now introduce the compilation function that translate i-while programs into RISC programs. The syntax for RISC programs is defined in Figure 1. The translation $\alpha$ between i-while and RISC instructions is defined in Figure 21.

![Fig. 21. Translation between i-while and RISC programs](image-url)
Besides the input i-while code and the output RISC program, the function $\alpha$ requires a label as input and produces a label as output. The role of these labels is clarified in the explanation of if and while instructions compilation.

All cases skip, $x := r, r := F$ and out $\text{ch} r$ correspond to a straightforward mapping between i-while instructions and RISC instructions. The input label is used to label the produced instruction, and the empty label $\epsilon_{\text{lab}}$ is given as output. The first instruction in the compilation of the if statement is $l : \text{jz} \ br \ r$, that corresponds to the register variable evaluation in the i-while language. Branches $D_1$ and $D_2$ are translated into RISC programs $P_1$ and $P_2$ respectively. In particular, $P_2$ requires the label $\text{br}$ to be used as argument for $\alpha$ in order to move the control flow from $l : \text{jz} \ br \ r$ to $P_2$ in case the content of $r$ is 0. The trailing skip statements are converted into a $l_1 : \text{jmp} \ ex$ and a $l_2 : \text{nop}$ respectively, to guarantee that the first instruction to be executed after any of the two branches is the one labeled with $\text{ex}$, if any. The compilation of the while instruction produces a conditional jump on $r$ as the first instruction, similarly to the if case. The compilation of the loop body follows, and the skip statement is replaced by the $l' : \text{jmp} \ l$ instruction, that moves back the control to the register evaluation when the execution of the loop body is completed.

The relation between an i-while program $D$ and its corresponding RISC program $\alpha(D)$ is stated in terms of the RISC semantics. Recall from Section 3.1 that the semantic of RISC programs is defined in terms of a labelled transition system $S_\alpha = \{((P, k, R, M)), \{\text{ch} k | \text{ch} \in \{\text{low}, \text{high}\} \cup \{\tau\}, \rightarrow\}$ where the first two elements of the state $P$ and $k \in \mathbb{W}$ are the fault-tolerant component $T$, the elements $R$ and $M$ are the faulty part $F$ and transitions are defined in Figure 12.

In general, a RISC program behaves exactly as the corresponding i-while program. However, this does not hold for i-while programs that manipulate constants outside $\mathbb{W}$. We therefore postulate the existence of a technique for approximating the resource footprint for the source i-while program statically (cf. the approach to transparency in [8]) and, from now onwards, we focus only on i-while programs that have a resource footprint compatible with the capabilities of the RISC machine.

Before proceeding further, we need some notational conventions. We say an i-while memory $M$ is equivalent to the RISC storage $(R, M)$, written as $M = (R, M)$ if $M|_{\text{Reg}} = R$ and $M|_{\var} = \nu_2 p \circ M$.

**Definition 20 (Strong Coupling).** A relation $R$ between i-while programs and $(P, k)$ pairs, where $P$ is a RISC program and $k \in \mathbb{W}$ is an exact bisimulation if for any $(D, (P, n)) \in R$, $\forall M \models (R, M), (D, M) \xrightarrow{\tau} (D', M')$ if and only if $(P, n, R, M) \xrightarrow{\tau} (P, n', R', M')$ such that $M' = (R', M')$ and $(D', (P, n')) \in R$. We say that an i-while program $D$ is strongly coupled with a RISC program $P$, written as $D \approx P$, if there exists an exact bisimulation $R$ such that $(D, (P, 0)) \in R$.

We can now characterize the existing relation between an i-while program $D$ and its translated version $P$ in terms of strong coupling.

**Proposition 7 (Strong coupling between i-while and RISC programs).** Let $D$ be an i-while program and $P$ be the first component of $\alpha(D, \epsilon_{\text{lab}})$. Then $D \approx P$. 
The result in this section can be combined with the ones in Section I.1 to show that we can translate a type-correct while program into a strongly secure RISC program. In particular, let $C$ be a while program such that $\{\} \vdash_{Var} C \rightarrow \{D\}, \langle t, w \rangle, \Phi'$ and let $\alpha(D, \epsilon_{lab}) = (P, l)$. Then $P$ is strongly secure.

### J Example of a Compilation

In this section we show an example of a simple hash calculation that we can implement within our language. Informally, the hashing algorithm works as follows:

- define two public integers $i$ and $j$ such that $1 < j \ll i$
- pick a public message $m$ in the interval $[0, 2^i - 1]$, while the public hash $h$ will be in $[0, 2^j - 1]$
- define a public value $p$, the smallest prime such that $p > 2^j$
- pick two secret values $q$ and $r$ such that $1 \leq q \leq p - 1, 0 \leq r \leq p - 1$
- calculate the hash as $h_{q,r}(m) = [(q \cdot m + r) \mod p] \mod 2^i$

In the while language a possible implementation of the hash program proceeds as follows:

```plaintext
limit := 1;
while $i$ do {limit := limit * 2; $i := i - 1$;}
source := $q \cdot m$;
source := source + $r$;
guard := source - $p$;
while guard > 0 do {guard := guard - $p$; source := source - $p$;}
guard := source - limit;
while guard > 0 do do{guard := guard - limit; source := source - limit;}
```

---

6 Notice that this statement is not completely accurate. The inaccuracy arises from the fact that $guard > 0$ is not a valid expression in the language. This is not a big issue, since RISC can be smoothly extended by including a jlez instruction without breaking any of the results.
This correspond to the following RISC code

\[
\text{movek } r_{\text{lim}} 1 \\
\text{store } \text{limit } r_{\text{lim}} \\
\text{load } r_i i \\
\text{store } i r_i \\
\text{loop1 : jz exit\_loop1 } r_i \\
\text{movek } r_2 2 \\
\text{mul } r_{\text{lim}} r_2 \\
\text{store } \text{limit } r_{\text{lim}} \\
\text{movek } r_1 1 \\
\text{sub } r_i r_1 \\
\text{store } i r_i \\
\text{load } r_i i \\
\text{store } i r_i \\
\text{jmp } \text{loop1} \\
\text{exit\_loop1 : load } r_g q \\
\text{load } r_m m \\
\text{mul } r_g r_m \\
\text{store } \text{source } r_g \\
\text{load } r_r r \\
\text{add } r_g r_r \\
\text{store } \text{source } r_g \\
\text{load } r_p p \\
\text{sub } r_g r_p \\
\text{store } \text{guard } r_g \\
\text{load } r_g \text{guard} \\
\text{store } \text{guard } r_g \\
\text{jmp } \text{loop2} \\
\text{loop2 : jlez exit\_loop2 } r_g \\
\text{sub } r_g r_p \\
\text{store } \text{guard } r_g \\
\text{load } r_s \text{source} \\
\text{sub } r_s r_p \\
\text{store } \text{source } r_s \\
\text{load } r_g \text{guard} \\
\text{store } \text{guard } r_g \\
\text{jmp } \text{loop2} \\
\text{exit\_loop2 : load } r_{\text{lim}} \text{ limit} \\
\text{load } r_g \text{ source} \\
\text{sub } r_g r_{\text{lim}} \\
\text{store } \text{guard } r_g \\
\text{load } r_g \text{guard} \\
\text{store } \text{guard } r_g \\
\text{jmp } \text{loop3} \\
\text{loop3 : jlez exit\_loop3 } r_g \\
\text{sub } r_g r_{\text{lim}} \\
\%
\]
The security levels of resources involved in this example are assigned as follows:

- level $L$ variables: $\text{limit}, i, m, p$;
- level $H$ variables: $q, \text{source}, \text{guard}, r$;
- level $L$ registers: $r_{\text{lim}}, r_i, r_2, r_1$;
- level $H$ registers: $r_g, r_m, r_p, r_s, r_{\text{hl}}$, $r_r$. 
