Improved Gradual Resistive Switching Range and 1000× On/Off Ratio in HfO$_x$ RRAM Achieved with a Ge$_2$Sb$_2$Te$_5$ Thermal Barrier

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ABSTRACT: Gradual switching between multiple resistance levels is desirable for analog in-memory computing using resistive random-access memory (RRAM). However, the filamentary switching of HfO$_x$-based conventional RRAM often yields only two stable memory states instead of gradual switching between multiple resistance states. Here, we demonstrate that a thermal barrier of Ge$_2$Sb$_2$Te$_5$ (GST) between HfO$_x$ and the bottom electrode (TiN) enables wider and weaker filaments, by promoting heat spreading laterally inside the HfO$_x$. Scanning thermal microscopy suggests that HfO$_x$+GST devices have a wider heating region than control devices with only HfO$_x$, indicating the formation of a wider filament. Such wider filaments can have multiple stable conduction paths, resulting in a memory device with more gradual and linear switching. The thermally-enhanced HfO$_x$+GST devices also have higher on/off ratio ($>10^3$) than control devices ($<10^2$), and a median set voltage lower by approximately 1 V (~35%), with a corresponding reduction of the switching power. Our HfO$_x$+GST RRAM shows 2× gradual switching range using fast (~ns) identical pulse trains with amplitude less than 2 V.

Abundant-data computing requires significant data movement to and from off-chip memory, resulting in a “memory-wall bottleneck,” where speed and energy efficiency are dominated by the data movement. In order to solve this memory-wall bottleneck, fine grained access between memory and logic is required for which two types of solutions exist: (i) integrating multi-bit digital memory on-chip with high capacity and (ii) in-memory computing, a type of neuromorphic computing where some part of the computation is done inside the memory, reducing data movement between computing and memory. In-memory computing requires storage of analog values, which requires resistive memories to switch gradually between different resistive states.

Among possible candidates for in-memory computing, resistive random-access memory (RRAM) is one of the emerging non-volatile memory technologies that is highly scalable, back-end-of-line (BEOL) compatible, and capable of low energy switching. Filamentary RRAM is a metal/oxide/metal device that operates by forming single or multiple filaments composed of oxygen vacancies created by a soft breakdown in the oxide due to the applied electric field. One of the challenges for filamentary RRAM to switch gradually across a large range of conductance values is the abrupt set process. The filament formation and the subsequent set and reset cycles are due to O$^2-$ion
movement to and from the filament to the top electrode (TE), which serves as the oxygen reservoir. In HfOx RRAM, the O$^{2-}$ ion movement is mostly driven by the electric field (E-field), due to its relatively low hopping activation energy (0.7 eV). The E-field driven ion movement causes a soft oxide breakdown which initiates rapid positive feedback of current and local self-heating, making the set process abrupt.

However, it has been demonstrated that O$^{2-}$ diffusion is thermally controlled, where both the lateral temperature gradient away from the filament and the high temperature of the filament increase the lateral diffusion of O$^{2-}$. Padovani et al. demonstrated by kinetic Monte-Carlo modeling that high temperature formation causes a wider filament. Trap-assisted tunneling transport between the oxygen vacancies in a wider filament result in multiple stable conduction paths through the filament resulting in a gradual and linear change in resistances. High temperature operation of the RRAM device as performed by Jiang et al. requires a separate micro-thermal stage that is not scalable in practice. Also, this approach cannot directly probe temperature gradients at nanoscale resolution due to fabrication constraints. In addition, probing the surrounding oxide may not be sufficient to get a complete thermal picture of the filament, since majority of the heat is dissipated through the electrodes. Note that the filament typically ruptures and reforms at the top electrode interface. Adding a thermal barrier material with low thermal conductivity and good electrical conductivity between the switching oxide and the bottom electrode (BE) could raise the temperature in the switching layer without reducing the E-field within the filament, thereby increasing lateral diffusion of O$^{2-}$ ions to form a wider filament.

Wu et al. reported thermal enhancement using a conductive TaOx layer between HfOx and the BE, where the gradual switching range from the high to low resistance state (HRS to LRS) is 3× and the switching is highly non-linear. However, no experimental visualization of the wider filament caused by the TaOx thermal barrier has been reported. Compared to the thermal conductivity of HfOx (~0.5 to 1.0 Wm$^{-1}$K$^{-1}$), the TaOx thermal conductivity is not low (~10 Wm$^{-1}$K$^{-1}$). Therefore, the origin of gradual resistive switching from TaOx insertion could be due to the addition of thermal interfaces: electrode/TaOx and TaOx/HfOx, and the low oxygen vacancy mobility of TaOx compared to HfOx that could also result in effective width modulation of the conductive filament.
In this work, we report experimental visualization of a conductive filament and correlate its morphology with the switching characteristics including on/off ratio, set voltage, and gradual switching behavior. Our experiments suggest that the filament is wider in HfO$_x$ RRAM with a Ge$_2$Sb$_2$Te$_5$ (GST) thermal barrier placed between HfO$_x$ and the BE. We choose GST here because such chalcogenide glasses have lower thermal conductivity (~0.45 Wm$^{-1}$K$^{-1}$ in the fcc phase)$^{14}$ and higher electrical conductivity than transition metal oxides (like HfO$_x$, TaO$_x$). We have observed that for similar input power, the HfO$_x$+GST devices also show 1.5-2× higher temperature difference at the filament hot spot with respect to the ambient. This reduces the set voltage and results in a linear and gradual resistive switching due to thermal enhancement in this RRAM device.

Our RRAM is fabricated in series with an NMOS Si transistor to form a 1-transistor 1-resistor (1T1R) test structure. Figures 1(a,b) show a schematic of the RRAM cross-section and the fabrication flow, respectively, and Fig. 1(c) shows the top-side optical image of the completed 1T1R. The transistor has gate length $L = 5$ µm and width $W = 5$ µm. After the transistor is fabricated, the drain contact is extended to form the BE (50 nm Pt) of the
RRAM, followed by a layer of sputtered GST (12 nm) on the BE. The GST region is 5 μm × 5 μm patterned using a lift-off process to fully cover the BE (1 μm × 1 μm) sidewalls. A very thin capping layer of Hf (1 nm) is sputtered in situ to prevent the oxidation of the GST, and the thin Hf film oxidizes to HfOₓ on vacuum break. The HfOₓ (5 nm) switching layer is then immediately deposited by atomic layer deposition (Cambridge Nanotech Savannah S200) at 200 °C, using TDMA-Hf as Hf precursor and water as the oxygen source. Finally, the 500 nm × 500 nm TE is sputtered and patterned as TiN (30 nm) capped by Pt (10 nm) to make a crossbar structure. Due to the processing temperature of HfOₓ, the as-deposited amorphous GST crystallizes into the cubic (fcc) phase. In Fig. 1(d) we observe that after switching, the Raman spectra show a slightly asymmetric peak at ~100 cm⁻¹ which indicates some mixed phase other than fcc.¹⁶

The devices undergo RRAM forming with a linear bipolar DC current-voltage (I-V) sweep up to 6 V while keeping the BE at 0 V. During the forming process the compliance current is controlled by the transistor gate voltage. The I_D vs. V_GS and the I_D vs. V_DS characteristics of the NMOS transistor are shown in Figs. 1(e,f) respectively. We measure the apparent changes in the width of the filamentary region with multiple steady-state voltage biases using scanning thermal microscopy (SThM),¹⁶ a scanning probe technique which enables temperature measurement of the RRAM top surface with sub-100 nm spatial resolution.¹⁵,¹⁶

Figure 2(a) shows the SThM tip voltage (V_{STM}, proportional to the surface temperature rise) across the top surface, for devices with only HfOₓ and those with HfOₓ+GST, at several bias conditions. These devices were formed and cycled 5 times to the LRS before measurement. During measurement, a low magnitude, steady-state bias is applied so that the filament conducts a current small enough to not disturb it, but large enough to induce some Joule self-heating which is detected by the SThM on the top surface. Figures 2(a) (i and ii) show the SThM tip voltage map for zero current flowing through the filament. This figure establishes the baseline measurement that represents the topography of the device surface. At a smaller current level, driving 20-30 μW power through the filament, we start to observe the increase in V_{STM} [Figs. 2(a) (iii) and (iv)] indicating Joule heating. When the power reaches 55-70 μW [Figs. 2(a) (v) and (vi)], a hot spot is seen having the highest V_{STM}. This represents the possible location of the filament. Figure 2(b) shows the estimated ΔT at the top of the device, after calibration of V_{STM} from known temperatures.¹⁶ (This temperature corresponds to the highest V_{STM} point in the 2D map.)
We observe that the HfO$_x$+GST device has higher peak hot spot temperature rise ($\Delta T$, which is proportional to $V_{SThM}$), indicating better heat trapping due to the lower thermal conductivity of the GST thermal barrier. The temperature rise at the top surface for the same electrical power is as much as twice in our RRAM device with GST, compared to control devices without, at similar applied electrical power. Figure 2(c) shows the line profile of $\Delta T$ as a function of the $x$-axis [in Fig. 2(a)] through the hot spot. The broader hot spot in HfO$_x$+GST RRAM is due to the higher thermal resistance of the HfO$_x$+GST stack that results in a higher temperature rise for the same applied power compared to the GST-only device [Fig. 2(b)]. This suggests that GST with its lower thermal conductivity acts as a thermal barrier which prevents heat loss from the switching layer (HfO$_x$) to the BE. As a result, the HfO$_x$+GST device has higher temperature forming, causing a wider filament. In the HfO$_x$-only device, forming the filament is dominated mostly by the E-field that results in a narrower, more compact filament formation.

One important consequence of a wider filament is the transport mechanism in both set and reset is dominated by trap-assisted tunneling (TAT) between oxygen vacancies spaced farther apart than in a single strong filament [Figs. 3(a) and 3(b)]. TAT is highly sensitive to the average tunneling distance and hence to the microscopic
configuration of the filament after each cycle. Figure 4(a) shows the comparison of LRS and HRS distributions for both HfO$_x$-only and HfO$_x$+GST devices for 50 switching cycles. TAT dominated transport in the wider filament in HfO$_x$+GST device show a broader resistance distribution (more prominent in HRS) and a higher on/off ratio. Note that the on/off ratio increases with the compliance current for HfO$_x$+GST device whereas, it remains very similar for HfO$_x$-only device. The energy barrier for electrons to hop from one trap state to another depends on the E-field. Therefore, switching in conventional HfO$_x$-only RRAM is determined by E-field dependent direct tunneling during set and by Joule heating during reset, where the Joule heating enhances oxygen transport. On the other hand, our RRAM with the GST thermal barrier switches by a combination of tunneling transport mechanisms during both set and reset. This is due to the higher temperature forming that causes increased defect density in the oxide surrounding the filament. Heat trapping also helps move oxygen ions relatively easily during set in response to the applied E-field. In other words, higher temperatures make the oxygen ion more responsive to E-field.

Despite the insertion of a relatively thicker GST layer with respect to HfO$_x$, the set voltage ($V_{\text{set}}$) does not increase because the HfO$_x$ is more resistive than the GST when the device is in HRS. A majority of the $V_{\text{set}}$ voltage drop is across the oxide rather than the GST, because GST is more electrically conductive. In fact, Fig. 4(b) shows that the $V_{\text{set}}$ of the HfO$_x$+GST device is lower than that of the HfO$_x$ device (the distribution is over 50 cycles of switching) for same reset voltage ($V_{\text{rst}}$). This also suggests that adding GST makes it easier to form a filament by heat trapping inside the HfO$_x$, in agreement with the findings of Jiang et al. that forming voltage is lowered at higher temperatures. The reduction in $V_{\text{set}}$ is more significant for higher compliance current ($I_{\text{cc}} = 100$ µA), which indicates that more heating in the filament increases the mobility of the O$^{2-}$ ions, requiring less E-field for set.
We demonstrate gradual switching in HfO$_x$+GST RRAM by applying a pulse train with the same amplitude and width, and measuring the resistance after each pulse. The conductance as a function of the number of pulses is shown in Fig. 4(c). Both potentiation (low to high conductance) and depression (high to low conductance) show gradual and linear switching with a $\sim\!2\times$ dynamic range. For potentiation (depression), the write pulse amplitude and width are $+1.8$ V ($-1.77$ V) and 100 ns (70 ns), respectively. In both cycles, a 1 ns rise/fall time is used. The gradual switching response is linear with respect to the number of pulses applied. This demonstrates that heat trapping in HfO$_x$ due to the GST thermal barrier layer causes gradual set/reset.

In conclusion, we have demonstrated experimental observation of filament formation in RRAM, and observed that inserting a GST thermal barrier causes a wider filament to form in the HfO$_x$. Such thermally-enhanced RRAMs show higher on/off ratio and linear gradual resistive switching. Gradual resistance switching is promoted by the formation of wider instead of narrow filaments (in control devices without a GST barrier, where the oxygen vacancies are more compact). Such change in the filament morphology can increase the contribution of trap-assisted tunneling, which reduces the bistable nature of filamentary switching. Lateral heat spreading inside the HfO$_x$
switching material also improves the mobility of O$_2^-$ ions, resulting in a decrease of the set voltage, which can potentially improve the energy-efficiency of switching. Such thermally-enhanced RRAMs can be a potential candidate as synaptic devices for in-memory computing.

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AUTHOR DECLARATIONS

Conflict of Interest: The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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