High-Throughput and Memory-Efficient Parallel Viterbi Decoder for Convolutional Codes on GPU

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Abstract—This paper describes a parallel implementation of Viterbi decoding algorithm. Viterbi decoder is widely used in many state-of-the-art wireless systems. The proposed solution optimizes both throughput and memory usage by applying optimizations such as unified kernel implementation and parallel traceback. Experimental evaluations show that the proposed solution achieves higher throughput compared to previous GPU-accelerated solutions.

Index Terms—Convolutional codes, Viterbi decoder, Software-defined radio (SDR), Parallel processing, GPU, CUDA

I. INTRODUCTION

C HANNEL coding is a technique that is widely employed in transmission of data over an unreliable or noisy communication channel. The transmitter encodes the original message by adding redundancy. This enables the receiver to recover the original data by decoding the received noisy data. Convolutional coding is a channel coding method which has been widely used in industrial protocols, for instance, in DVB-T, DVB-S, GPRS, GSM, LTE, 3G, CDMA, WiFi and WiMAX. Different decoding algorithms exist for convolutional codes, among which the Viterbi decoding algorithm is the optimal and the most widely-used method.

The Viterbi decoder operates in either hard-decision mode or soft-decision mode. In the hard-decision mode, every bit in the input of the decoder is represented by either a zero or one. In the soft-decision mode, however, every input bit is a log likelihood ratio (LLR) that is formed based on the probability that the received bit is zero or one. In this mode, the Viterbi decoder takes advantage of the additional information in order to decrease the bit error rate (BER) by about 2.3 dB. A lower BER means a better recovery of the original signal. This comes at the cost of higher computational requirement, which in turn, lowers the overall decoding throughput.

Many FPGA-based methods have been proposed for acceleration of the Viterbi decoding algorithm. While such methods achieve very high throughput, they do not provide the flexibility required for software defined radio (SDR) and cognitive radio (CR) applications.

This paper proposes a novel parallel algorithm for implementation of the Viterbi decoding algorithm in the soft-decision mode on GPU hardware. Flexibility is a key factor in software defined radio (SDR) and GPU provides a platform for flexible software-based implementations at high throughput.

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Fig. 1: a) Convolutional encoder \((\beta, 1, k)\) with \(k = 7, \beta = 2\), and generator polynomials 1111001 and 1011011. b) Branch \(ij\) from state \(i\) to \(j\) in the encoder FSM.

The proposed solution is mainly focused on optimizing the memory requirement. This aspect has not been explored in previous works but has a very large impact in boosting the throughput. The proposed algorithm reaches a very high decoding rate compared to previous solutions.

II. PRELIMINARIES

This section presents a brief overview of convolutional encoding, Viterbi decoding algorithm, and the concept of soft-decision inputs. In addition, a brief overview of CUDA API for parallel programming on GPU hardware is presented.

A. Convolutional Encoder

Fig. 1(a) shows an example convolutional encoder. The encoder receives a series of \(n\) bits and produces a series of \(2^k-1\) encoded bits which will be transmitted over the communication channel. \(\beta \geq 2\) encoded bits are generated for every input bit. Code rate \(r\) is defined as the inverse of \(\beta\). At time (stage) \(t\), each one of the \(\beta\) output bits is computed based on the current input bit, i.e., \(i_t\), and the previous \(k - 1\) input bits as

\[
(g_{k-1}.i_t) \oplus \cdots \oplus (g_0.i_{t-k+1})
\]  

where, \(k\) is called the constraint length, \(\oplus\) is the xor operator, and \(g\) is a \(k\)-bit value called the generator polynomial. There are \(\beta\) generator polynomials, one for every output bit. In the example shown in Fig. 1(a), \(k = 7\) and \(\beta = 2\). The two generator polynomials are 1111001 and 1011011, whose octal representations are 171 and 133, respectively.

The encoder can be viewed as a finite state machine (FSM) with \(2^{k-1}\) states. The previous \(k - 1\) input bits, i.e., \((i_{t-1}, i_{t-2}, \ldots i_{t-k+1})\), form the current state. Assume the
FSM is in state $i \in [0, 2^{k-1} - 1]$. Depending on $i_{\text{in}}$, i.e., the current input bit which is either zero or one, the FSM takes a branch $ij$ from state $i$ to state $j$. Hence, a series of input bits causes the FSM to take a series of branches, which is called a path.  

The encoder FSM can be formed solely based on $k, \beta$, and the generator polynomials. Every branch $ij$ in the FSM is associated with a single-bit branch input $\alpha_{\text{in}}^{ij}$ and a $\beta$-bit branch output $\alpha_{\text{out}}^{ij}$. See Fig. 1(b). The output of the encoder is $\alpha_{\text{out}}^{ij}$ provided that the FSM goes from state $i$ to $j$. This transition happens if the input bit is equal to $\alpha_{\text{in}}^{ij}$.

**B. Viterbi Decoding Algorithm**

The encoded bits are transmitted over the channel. When they arrive at the receiver, some of the bits are corrupted. The received bits are decoded in order to recover the original data. The Viterbi decoding algorithm is the optimal and the most widely-used method for decoding convolutional codes [1].

Given the received series of bits, the decoding algorithm recovers the original data by finding the most probable path swept by the encoder FSM. This is done by investigating the likelihood of many different paths. Since the number of possible paths grow exponentially, the Viterbi decoding algorithm employs a dynamic programming approach to efficiently find the most probable path as the following [1].

First, for branch $ij$ from state $i$ to state $j$ at stage $t \in [0, n)$, branch metric $\delta_{ij}^t$ is computed as

$$\delta_{ij}^t = \sum_{b=0}^{\beta-1} (-1)^{\alpha_{\text{out}}^{ij}[b]} \times \text{llr}_t[b]$$ (2)

where, $\alpha_{\text{out}}^{ij}[b]$ and $\text{llr}_t[b]$ denote bit $b$ of $\alpha_{\text{out}}^{ij}$ and $\text{llr}_t$, respectively. $b \in [0, \beta]$. The term $\text{llr}_t$ denotes the received bit at decoder input at time $t$. Basically, $\delta_{ij}^t$ indicates the amount of similarity between the received data and the output of branch $ij$. Next, for state $j$ at stage $t$, path metric $\sigma_{j}^t$ is computed as

$$\sigma_{j}^t = \max_{i \in \text{prev}(j)} (\sigma_{i}^{t-1} + \delta_{ij}^t)$$ (3)

where, $i$ iterates over the previous states of state $j$ in the FSM. Note that every state has two previous states, i.e., two input branches. The above equation is known as ACS (add, compare and select) operation. Basically, $\sigma_{j}^t$ is formed by accumulating a series of branch metrics which eventually end at state $j$ at stage $t$ and also, have the highest possibility. In other words, $\sigma_{j}^t$ indicates the likelihood of the most probable path which ends at state $j$ till stage $t$.

While computing $\sigma_{j}^t$, the selected previous state $\pi_{j}^t$ which maximized $\sigma_{j}^t$ needs to be saved as well. It basically indicates one stage of the survivor path which ends at state $j$ at stage $t$.

$$\pi_{j}^t = \arg \max_{i \in \text{prev}(j)} (\sigma_{i}^{t-1} + \delta_{ij}^t)$$ (4)

The above calculations constitute the forward procedure in the Viterbi decoding algorithm. See Alg. 1. The outer loop iterates through all stages $t \in [0, n)$ and the inner loop iterates through all states $j \in [0, 2^{k-1})$.

Once the forward procedure is complete, the backward procedure is performed as the following. First, the most probable survivor path at the last stage, i.e., $t = n - 1$, is selected as the winner, and that specific path is traced back to the first stage, i.e., $t = 0$. At every stage during the traceback, the decoder output (which is ideally equal to the original data) is formed based on $\alpha_{\text{in}}^{ij}$. The two operations are called traceback and decoding. See Alg. 2

**C. Hard-decision vs. Soft-decision**

The input to the Viterbi decoding algorithm can be represented in either hard-decision mode or soft-decision mode. In **hard-decision** mode, every bit is simply represented by either zero or one. In **soft-decision** mode, however, every bit in the input of the decoder is a log likelihood ratio (LLR) that is formed by the receiver circuit based on the probability that the received bit is zero or one. A larger positive LLR means a larger probability of zero, and a larger negative LLR means a larger probability of one. Basically, in addition to

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**Algorithm 1** The first step, i.e., the forward procedure, in the Viterbi decoding method.

**input:** $\text{llr}_t[b]$ (b) 
**output:** $\pi_{2^{k-1}}$ 
1: Initialize $\pi_{2^{k-1}}$ to zero 
2: for $t = 0$ to $n - 1$ do 
3: for $j = 0$ to $2^{k-1} - 1$ do 
4: Set $i'$ and $i''$ equal to the two previous states of $j$ 
5: Compute $\delta_{ij}^t$ and $\delta_{i}^{t-1}$ according to (2) 
6: $\sigma' = \pi_t[j, t-1] + \delta_{ij}^t$ 
7: $\sigma'' = \pi_t[j'', t-1] + \delta_{i}^{t-1}$ 
8: if $\sigma' > \sigma''$ then 
9: $\pi_t[j, t] = \sigma'$ 
10: else 
11: $\pi_t[j, t] = \sigma''$
12: end if
13: end for 
14: end for 
15: end for 
16: end for

**Algorithm 2** The second step, i.e., the backward procedure, in the Viterbi decoding method.

**input:** $\pi_{2^{k-1}}$ 
**output:** $\text{Out}$ 
1: $j^* = \arg \max_{j \in [0, 2^{k-1}]} \sigma[j, n - 1]$ 
2: for $t = n - 1$ to 0 do 
3: $i = \pi_t[j^*, t]$ 
4: $\text{Out}[t] = \alpha_{\text{in}}^{ij}$ 
5: $j^* = i$ 
6: end for
the indication of the value of the input bit, the truth of this indication is provided as well.

The Viterbi decoder can take advantage of this additional information in order to better recover the original data. Bit error rate (BER) is lower in the soft-decision mode by about 2.3 dB. This comes at the cost of higher computational requirement.

D. CUDA Parallel Programming API

CUDA is a parallel programming API for Nvidia GPUs. GPU is a massively parallel processor with hundreds to thousands of cores. CUDA follows a hierarchical programming model. At the top level, computationally intensive functions are specified by the programmer as CUDA kernels. A kernel is specified as a sequential function for a single thread. The kernel is then launched for parallel execution on the GPU by specifying the number of concurrent threads.

Threads are grouped into blocks. A kernel consists of a number of blocks, and every block consists of a number of threads. In order to identify blocks within a kernel, and also, threads within a block, a set of indices are used in the CUDA API, for instance, blockIdx.x as the block index in dimension x within a kernel, and threadIdx.x as the thread index in dimension x within a block.

III. Previous GPU-Accelerated Viterbi Decoder Methods

The Viterbi decoder algorithm is inherently a sequential procedure and the amount of available parallelism is minimal. In specific, calculating the branch metrics is the only step which can be fully parallelized, and path metric calculations can only be partially parallelized using at most \(2^{k-1}\) threads, e.g., \(2^7-1 = 64\) threads, where each thread sequentially iterates over \(n\) stages. This approach was proposed in [2], [3]. See Fig. 2(a).

In order to better utilize the parallel computing capabilities of GPU and increase the throughput, the decoder output can be estimated by dividing the \(n\) stages into many small frames (tiles) of \(f\) stages each [4]–[7]. Every frame is processed in parallel with other frames, and decodes \(f\) out of \(n\) output bits. This tiling scheme increases the amount of available parallelism by a factor of \(n/f\). However, BER is degraded because not all previous history is available in a frame. In order to reduce BER degradation, consecutive frames should have small overlaps in order to carry enough history for correct decoding [4]–[7]. As shown in Fig. 2(b), every frame has an overlap of length \(v\) with its neighbor frames, that is composed of left overlap \(v_1\) and right overlap \(v_2\). Hence, to generate \(f\) decoded bits as the output, a frame needs to process \(f + v\) stages of the original Viterbi decoding algorithm.

In the forward procedure, the resulting survivor paths need to be stored in GPU global memory for later use in the backward procedure [4]–[7]. The amount of GPU global memory required to store the survivor paths is in the order of

\[
O\left(2^{k-1} \times n \times \left(1 + \frac{v}{f}\right)\right)
\]

(5)

because there are \(n/f\) frames, and every frame requires \(O(2^{k-1} \times (v + f))\) space from GPU global memory. The parallel algorithms proposed in [8], [9] improved the throughput by judiciously combining the execution of multiple frames in order to coalesce the memory accesses of the survivor paths in global memory. The coalesced memory accesses result in higher throughput.

In [10], in addition to the tiling scheme and coalescing accesses of survivor paths, branch metrics are efficiently computed according to specific repetitive patterns which help to share computations. In addition, data transfers between CPU and GPU are optimized, in specific, by employing multiple CUDA streams.

IV. Proposed Parallel Algorithm

This section presents our proposed parallel algorithm for execution of the Viterbi decoding algorithm on GPU based on CUDA framework.
A. Unified Kernel

As discussed above, the best previous parallel algorithms coalesce access to survivor paths in GPU global memory in order to minimize the associated latency and increase the throughput [3]–[10]. We propose to take a radically different approach, which I) highly reduces this memory access latency, and II) exposes a higher degree of parallelism.

In specific, we propose to parallelize the backward procedure (i.e., trace-back and decode) which enables us to efficiently combine both the forward procedure (i.e., branch metric, path metric and survivor path computations) and the backward procedure into a single unified parallel kernel. This unified kernel, in turn, allows the survivor paths to be stored in GPU shared memory, and therefore, global memory access is no longer required for storing and retrieving this intermediate data. As a result, the associated access latency to GPU global memory for survivor paths is removed completely and throughput is increased. In CUDA programming API, every block has access to a small, on-chip and low-latency memory, called shared memory. The shared memory of a block is accessible to all threads within that block, but not to any thread from other blocks.

It is very important to note that once the execution of a parallel kernel is completed, its shared memory data is no longer available, for instance, to subsequent kernels. Therefore, survivor paths cannot be stored in shared memory in any of the previous solutions, because the forward and backward procedures are performed in separate kernels [2]–[10].

The reason previous solutions had to employ separate kernels is that the forward and backward procedures in the Viterbi decoding algorithm have very different degrees of parallelism. In particular, in the forward procedure, branch metric computations are fully parallelizable, and the degree of parallelism available for computing the path metrics is $2^k$. At the other hand, the backward procedure is completely serial. See the first row in Table I. Even after applying the tiling scheme, the amount of parallelism made available in the backward procedure is minimal. In specific, it is equal to the number of frames, because the backward procedure is still performed sequentially in every frame [4]–[10]. In the proposed solution, however, the backward procedure is parallelized. See the last row in Table I.

A parallelized methods for the backward procedure are presented in Sections IV-D. However, before discussing the parallelized backward procedure, the proposed ideas in optimizing branch metric and path metric computations are discussed in Sections IV-B and IV-C.

B. Branch Metrics

In our proposed unified-kernel approach, every frame is processed in parallel to other frames, and decodes $f$ out of $n$ output bits. Every frame involves $f + v$ stages, and every stage has $2^k$ states. In the simplest form, every block processes one frame using $2^k - 1$ threads. Hence, $2^k \times (f + v)$ branch metrics need to be computed in every block. As shown in

|Algorithm 3| The forward and backward procedures in a unified parallel kernel.|
|---|---|
|input:| $llr[\beta][n]$|
|output:| $Out[n]$|
|# of blocks:| $\frac{2^k}{f}$|
|# of threads / block:| $2^k - 1$|
|1:| __shared \( \delta[2^k - 1][f + v][2] \)|
|2:| __shared \( \sigma[2^k - 1][f + v] \)|
|3:| __shared \( \pi[2^k - 1][f + v] \)|
|4:| for \( t = 0 \) to \( f + v - 1 \) do|
|5:| \( j = threadIdx.x \)|
|6:| Set \( i' \) and \( i'' \) equal to the two previous states of \( j \)|
|7:| Compute \( \delta[j][t][0] = \delta[i'] \) and \( \delta[j][t][1] = \delta[i''] \)|
|8:| \( \sigma' = \sigma[i'][t - 1] + \delta[j][t][0] \)
|9:| \( \sigma'' = \sigma[i''][t - 1] + \delta[j][t][1] \)|
|10:| __syncthreads( )|
|11:| if \( \sigma' > \sigma'' \) then|
|12:| \( \sigma[j][t] = \sigma' \)
|13:| \( \pi[j][t] = i' \)
|14:| else|
|15:| \( \sigma[j][t] = \sigma'' \)
|16:| \( \pi[j][t] = i'' \)
|17:| end if|
|18:| end for|
|19:| \( j^* = \arg \max_{j \in [0,2^k-1]} \sigma[j][n-1] \)
|20:| for \( t = f + v - 1 \) to \( 0 \) do|
|21:| \( i = \pi[j^*][t] \)
|22:| \( out[t] = \alpha_{in}^{j^*} \)
|23:| \( j^* = i \)
|24:| end for|

Fig. 4(a), storing all such values in shared memory requires a two-dimensional matrix of size

$$2^k \times (f + v),$$

which is not an efficient use of shared memory. GPU has a hardware scheduler that automatically assigns multiple blocks to every streaming multi-processor (SM). Since the amount of shared memory in every SM is limited, the smaller the shared-memory usage of every block, the larger the number of blocks that are assigned to every SM, and hence, the higher the achieved throughput. We employ the following strategies in order to reduce the amount of shared memory usage in every block.

On-the-fly Computation: During the computation of the path metrics, branch metrics can be computed on-the-fly. In other words, equations (2) and (3) can be evaluated at the same time. This approach does not require storing any of the branch metrics in shared memory.

Repetitive Patterns: The above approach leads to many redundant computations. This is because branch metrics follow specific repetitive patterns [10]. See (2). In every stage $t$, $llr_t$ is constant. Hence, since $\alpha_{out}^\beta$ has $\beta$ bits, there are only $2^\beta$
unique branch metric values in every stage \[10\]. Therefore, a more optimized approach is to first compute
\[2^\beta \times (f + v)\] (7)
unique branch metrics and store them in shared memory, then compute the path metrics.

**Standard Convolutional Codes:** We can cut the above shared-memory requirement for branch metrics to half. Since \(\alpha_{ij}^{out} = 2^\beta - \alpha_{ij}^{out}\), we have
\[
\sum_{b=0}^{\beta-1} (-1)^{\alpha_{ij}^{out}[b]} \times llr_t[b] = -\sum_{b=0}^{\beta-1} (-1)^{\alpha_{ij}^{out}[b]} \times llr_t[b]
\] (8)
which means half of the branch metric values are complements of the other half. As a result, a matrix of size
\[2^{\beta - 1} \times (f + v)\]
(9)
is sufficient to store the branch metrics.

**Wrap-Efficient Sub-folding:** In above approaches, branch metrics for whole the stages are evaluated at first and then path metrics calculation are performed. These two loops that have \(f + v\) iterations can be folded and performed in \(S\) iterations if both of them are in an outer loop of size \(f + v/S\). An important point is that \(S\) should be selected wisely to avoid violating considerations about wrap efficiency.

**C. Path metrics**

Similar to the branch metrics, \(2^{k-1} \times (f + v)\) path metrics need to be computed in every block, and storing all such values in shared memory is not efficient. As shown in (3), path metrics \(\sigma\) are computed iteratively. In other words, to compute path metrics in stage \(t\), it is enough to have access to path metrics only from the previous stage. Hence, with proper thread synchronizations from stage \(t-1\) to stage \(t\), an array of size \(2^{k-1}\) is sufficient to store the path metrics in shared memory.

**D. Parallel Traceback Algorithm**

The traceback step is intrinsically serial and should be done by one thread. However, it leads to a decrease in GPU utilization as other threads are idle. So a parallel traceback algorithm should be provided to solve this problem. In order to parallelize the traceback step, two different algorithms are provided in this article.

In the first parallel traceback, the non-overlapping part of the frame should be divided into some subframes that every subframe is decoded by one thread in parallel. However, in the Viterbi algorithm, at the point that traceback starts to some stages later, decoded bits are not reliable and mustn’t be stored. After some stages, the survivor path that is traced back converges to its correct states and decoded bits become reliable and can be stored. That is the reason that the main frame should overlap its right-handed neighbor and the decoded bits of the overlapping part are not stored and is only used for the convergence of the survivor path. The same approach should be taken in the parallel traceback. Each subframe should overlap its right-handed neighbor as depicted in Fig. 5 and the decoded bits of the overlapping part is not stored. The length of the overlapping part depends on the coding parameters. Thus, it can be the same as the main frame like Fig. 5.

Another problem to be solved is that the starting state of the traceback is the state that its final path metric is the maximum. So in this parallel traceback algorithm, the final path metrics of all subframes that are the path metrics of the stages of subframes right boundaries are needed. However, when the traceback step is going to start, only the path metrics of the final stage is available. To handle this problem, the starting...
point can be random. As a result, the convergence will take longer. So the overlapping length $v_2$ should be increased. Another approach is that, instead of storing all path metrics of intermediate stages, only the state with maximum path metric can be obtained and stored. Thus, a reasonable amount of memory is used and convergence is not postponed.

E. De-puncturing

In the primary form of the convolutional encoder, the rate of the coding can be only $1/a$ where $a$ is a natural number greater than $2$. Puncturing is the elimination of some bits from the output of the encoder to produce codes with a wider variety of rates. This elimination should be done using a standard pattern. The standard pattern is like a mask with a fixed size that drops some bits and is replicated on the data. As the number of the output bits decreases after puncturing, the rate of the encoder increases. Since some information is removed, BER increases after puncturing. In the receiver, eliminated bits is replaced with zeros to make them neutral to metrics. It is called depuncturing. Then the Viterbi algorithm is applied like before.

In the implementation on GPU, a depuncturing step should be added at the beginning of the algorithm before branch metric calculation. In order to parallelize the step, each thread can depuncture some bits independently. Additionally, another array should be allocated to store depunctured data. As explained before, it is better to store this intermediate data in the shared memory.

In order to avoid the divergence of the blocks, all frames should start at the beginning of a pattern mask both in their overlapping and non-overlapping part. It means that $f$, $v_1$ and $v_2$ should be a multiple of the size of the pattern mask.

F. Memory Management

The important parameter of memory efficiency in GPU is coalesced access. In the branch metric calculation step, the $BM$ array is divided into some subarrays and each subarray is calculated by one independent thread as depicted in Fig. 6. In such an approach, distant elements are accessed at a time as the graph in Fig. 7 illustrates. Thus, it is better that all threads fill $T$ successive columns of the array where $T$ is the number of the threads. Then all threads calculate the next $T$ columns as depicted in Fig. 7. As a result, threads’ access is coalesced. This approach can be employed also in the filling of the depunctured frame array.

Another modification that can lead to coalesced access is handling more than one frame in each block. Even though GPU analyses the kernel to decide how many blocks can be assigned to each SM, handling it in the kernel can be effective. when some frames are running on one SM under the decision of GPU, the amount of shared memory block needed is allocated after each other. As all blocks are running the same algorithm, their shared memory blocks are accessed in the same part simultaneously. As a result, the arrays that are accessed simultaneously by different GPU blocks of the same SM are distant as much as the size of the shared memory. However, when several frames are handled in a block, their shared memory block can be interleaved, meaning arrays size is considered for all frames and the arrays are consecutive not whole the shared memory. Therefore, memory cells accessed at the same time will closer to each other.

Another aspect of memory optimization is the size of the shared memory used. In this algorithm, according to the report of Visual Profiler, shared memory is the bottleneck and reduction of the size of the used shared memory can be helpful. An approach used to do so is reusing shared memory. There
are three steps in this algorithm and each step has some arrays stored in shared memory. However, each of these intermediate arrays is used in a limited number of steps and their life time is not whole the kernel life time. Therefore, if there are two arrays needed in two distinct life time, both arrays can be stored in the same place. It is important to keep in mind that if their types are different, the pointer alignment should be satisfied for the larger type. As a result, the size of the used shared memory will be reduced and GPU utilization will enhance. In this implementation, $SP$ and depunctured frame are two arrays that can use the same memory. boundary states of the second parallel traceback algorithm and $PM$ can also be stored in the same place.

V. EXPERIMENTAL EVALUATION

A. Setup

The hardware platform is a server with an Intel Xeon CPU operating at 2.5 GHz. We experiment with Tesla V100 GPU. We employ Ubuntu OS 18.04 and CUDA version 10.2.

We experiment with a widely-used standard convolutional code, namely, $(2, 1, 7)$, i.e., code rate $1/2$ and constraint length 7, with generator polynomials 171 and 133. This configuration is shown in Fig. 1. In addition, we also consider the puncturing rates of $2/3$ and $3/4$.

B. BER Performance

In order to verify the implementation, the system shown in Fig. 8 is employed. At the first step, a vector of uniformly distributed bits is generated and, at step 2, passed to convolutional encoder. This part is the simulated transmitter. Then, at step 3, encoded bits are transmitted in an AWGN channel with a specific $E_b/N_0$. Assuming that the BPSK modulation is used, the channel simulation is done by adding a vector of normally distributed values with standard deviation of $2^{-(k_b/N_0)/20}$. Having generated a noisy coded vector, at step 4, the simulated receiver can decode the signal and produce an output vector. At last, comparing the decoder output with the bits generated at the first step, Bit Error Rate (BER) will be obtained. It should be also noted that the BER value is reliable if enough data is generated and tested in the verification system. As a rule of thumb, if a vector of size $n$ is generated in the first step, only the BER value more than $100/n$ will be valid.

The process shown in Fig. 8 can produce the BER for a specific $E_b/N_0$. Complete verification is done by drawing the BER curve over a range of $E_b/N_0$ values and comparing it with the theoretical one that can be generated by MATLAB BER tool which is invoked by “bertool” command. Implementation parameters can be tuned this way.

In Fig. 9, the effect of $v_2$ on BER for $v_2 = 20$ and $f = 256$ that for $v_2 = 20$, theoretical performance is achieved and no considerable improvement can be gained by $v_2 > 20$. A metric can be defined to show the code performance for every set of parameters. What concerns is the distance between practical and theoretical curve. Therefore, the metric should represent this distance. The distance in the dimension of $E_b/N_0$ is reasonable since it shows that in order to achieve a specific BER, how much clearer the signal should be than it should be in theory. Table. III shows this metric for a wider range of $f$ and $v_2$ than Fig. 9.

TABLE II: The effect of $f$ and $v_2$ on BER

| $v_2$ | 32  | 64  | 128 | 256 | 512 |
|-------|-----|-----|-----|-----|-----|
| 10    | 0.72| 0.48| 0.31| 0.18| 0.12|
| 20    | 0.15| 0.090| 0.044| 0.040| 0.039|
| 30    | 0.030| 0.016| 0.0069| 0.022| 0.033|
| 40    | 0.0040| 0.00097| 0.0032| 0.025| 0.034|

In parallel traceback, there is another parameter which is the non-overlapping size of subframes. Fig. 10 shows the effect of both $v_2$ and $f_0$ on BER in parallel traceback algorithm. It can be seen that for $v_2 = 45$ and $f_0 = 32$, the decoder is reliable. It can also be observed that $v_2$ is still more important than the other parameters.

In Table. III the metric discussed above is also used to show the effect of $v_2$ and $f_0$ on BER.
TABLE III: The effect of $v_2$ and $f_0$ on BER in parallel traceback algorithm

| $v_2$ | $f_0$ | 8  | 16  | 24  | 32  | 40  | 48  | 56 |
|-------|-------|----|-----|-----|-----|-----|-----|-----|
| 25    |       | 2.90 | 2.41 | 2.15 | 1.94 | 1.77 | 1.72 | 1.54 |
| 30    |       | 1.57 | 1.28 | 1.09 | 0.97 | 0.85 | 0.81 | 0.70 |
| 35    |       | 0.87 | 0.66 | 0.53 | 0.44 | 0.39 | 0.33 | 0.29 |
| 40    |       | 0.43 | 0.31 | 0.22 | 0.18 | 0.15 | 0.12 | 0.10 |
| 45    |       | 0.18 | 0.11 | 0.08 | 0.06 | 0.05 | 0.03 | 0.03 |

In parallel traceback algorithm, a challenge was explained regarding final path metrics of each subframe. Two discussed solutions were starting traceback from a random state and storing states with maximum path metric. Fig. 11 shows that the first solution adversely affect BER and the cost of memory for storing the states pays off.

Fig. 11: The effect of traceback starting stated BER for $v_1 = 20$, $v_2 = 20$ and $f = 256$

C. Throughput

Table. IV shows the throughput of the regular decoder over the same range of $f$ and $v_2$ as Table. III Likewise,

| $v_2$ | $f$ | 32 | 64 | 128 | 256 | 512 |
|-------|-----|----|----|-----|-----|-----|
| 10    | 4.28 | 5.11 | 6.64 | 6.15 | 4.97 |
| 20    | 3.79 | 4.79 | 6.36 | 6.05 | 4.86 |
| 30    | 3.10 | 4.25 | 5.74 | 5.77 | 4.80 |
| 40    | 2.82 | 3.93 | 5.50 | 5.62 | 4.77 |

TABLE IV: Decoder throughput (Gb/s)

Table. V that shows the throughput in parallel traceback algorithm is associated with Table. III In order to demonstrate the improvement made by parallel traceback algorithm, cells of throughput should be compared. However, since parallel traceback increase BER, the cells that their associated cells in BER tables are close should be picked.

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