ABSTRACT This article demonstrates a digitally friendly time-based analog-to-digital converter (ADC) exploiting Dickson charge-pump (CP) as part of a voltage-to-time conversion (VTC) implemented in 28-nm CMOS. In the proposed technique, the Dickson CP generates a ramp signal that is compared with the input voltage to generate a pulse of commensurable widths, which is then fed to a D-type flip-flop (DFF)-based time-to-digital converter (TDC). The TDC is composed of CMOS DFFs and digital circuits for digital conversion without any use of analog-intensive circuits, e.g., amplifiers or current sources. Thanks to the robustness of Dickson CP characteristics, the digital outputs of the proposed ADC can be corrected through a low-complexity deterministic digital mapping with improvements of 1.5-bit in peak effective number of bits (ENOB) and 9 dB in peak signal-to-noise-and-distortion ratio (SNDR) verified over three measured sample prototypes.

INDEX TERMS Analog-to-digital converter (ADC), time-based ADC, Dickson charge pump (CP), time quantization, voltage-to-time converter (VTC), ADC calibration, distortion correction.

I. INTRODUCTION

DESPITE the continual CMOS scaling in favor of higher speed and integration of digital circuitry, the reduction of transistor dimensions results in lowering of available voltage headroom, thus unavoidably causing deterioration of analog circuitry, such as ADCs. As gate length shrinks, shorter gate delay and therefore finer time resolution can be achieved in nanoscale CMOS. Instead of directly quantizing voltage/current information, ADC architectures which utilize time/frequency information could offer better solutions [1].

The time-domain approach can be exploited by means of a voltage-controlled oscillator (VCO) [2]. A VCO in such an ADC generates a clock whose frequency is proportional to the analog input voltage. The clock’s phase is then sampled and differentiated such that the ADC’s digital output is ideally proportional to the analog input. Unfortunately, the nonlinearity of the VCO’s voltage-to-frequency conversion, which originates from the active devices, will directly affect the ADC’s nonlinearity, thus requiring extensive calibration due to PVT variations [3].

An alternative time-domain ADC implementation is an intermediate conversion of the input analog voltage into time information using a voltage-to-time converter (VTC) prior to digitization using a time-to-digital converter (TDC) [4]–[8]. Most of the proposed topologies are, however, hardly amenable to a low supply voltage operation, given their analog-intensive implementation, i.e., operational transconductance amplifiers (OTAs) and current sources [4]. In [8], the compact nature of the inverter-based VTC presents a potential for high-speed time-based ADCs. In [9]–[13],
“hybrid” converters that make use of time-domain quantizers show promising performance but using analog intensive circuits brings limitations at finer CMOS nodes. In [13], a highly linear current source is required for a time-residue amplification. In order to increase the resolution in time-domain ADCs, a time amplifier is employed in [14]. However, complex calibration to correct the time amplifier’s nonlinearity is necessary. Although [15], [16] demonstrated power-efficient time-domain data conversions using a linear current source for the time amplification without an expensive residue amplifier, there were restrictions in performance to either low bandwidth [15] or limited resolution [16]. In our previous work [17], we use a Dickson charge pump (CP) as a VTC but the system still needs a multitude of VTCs to overcome the non-linearity of the generated ramp signal. Event-based ADC in [18] can reduce the system sampling rate and power consumption but still requires analog comparators of high performance.

In this work, we propose a new architecture of a time-based ADC in which a sampled input voltage uses a reference ramp, generated by means of a Dickson CP, to produce a PWM signal whose width is inversely proportional to it. Thus realized voltage-to-time conversion (VTC) can be free from any highly linear current sources. The input-modulated pulse-width signal is fed into simple latches and digital logic for digital conversion. Due to the precise characteristics of Dickson CP, the digital outputs can be compensated through a deterministic digital mapping. At a nominal 1 V supply, the proposed ADC achieves a sample rate of 0.6 MS/s, while consuming 209 μW, in a highly digital implementation. The digital distortion correction is identical for all the measured samples and improves ENOB from 4.21 to 5.7 bits. Likewise, SNDR improves by up to 9 dB.

This article is organized as follows. Section II presents the proposed VTC exploiting Dickson charge pump and the distortion correction technique for linearizing its characteristics. Section III presents detailed implementation of the proposed ADC. Section IV describes measurement results.

II. DICKSON CHARGE-PUMP-BASED VOLTAGE-TO-TIME CONVERSION

In this section, we first study a working principle of the Dickson CP as a ramp reference signal generator for the proposed ADC. Then, top-level modeling and SPICE/MATLAB simulations of the effects of Dickson CP non-idealities are presented.

A. WORKING PRINCIPLE OF DICKSON CHARGE-PUMP

Dickson CP has been widely used in power management applications, in which a DC supply voltage, $V_{DD}$, is multiplied by a factor of $N$ that is equal to the number of cascaded stages. Due to the charge-transfer operation of a Dickson multiplier, the steady-state output voltage $V_S$ is a linear function of $V_{DD}$, and its time behavior can be well approximated by an RC exponential transient, increasing asymptotically towards $V_S$ and with a time constant which depends on the CLK frequency ($f_{CLK}$), number of stages $N$ and by the value of internal capacitance $C$. Thus, Dickson CP can operate as a voltage-slope generator which can be employed as a key building block in a VTC. Since it is composed of switches and capacitors, the proposed technique is suitable for highly scaled CMOS processes.

Figs. 1(a) and (b) show the schematic of Dickson charge-pump based on four cascaded stages and their corresponding signals, respectively. Each stage is composed of an NMOS switch in parallel to a diode-connected NMOS and a capacitor, $C_i$. During the initial exponential transient, charge is transferred along the chain towards the output $V_{ramp}$. The voltages between each stage across the inter-staged capacitors ($V_1$ to $V_4$) are gradually charged as CLK signal of $V_{DD}$ is toggling at the bottom plates of inter-stage capacitors until their voltages reach their respective steady-state values of $V_{DD} - V_{on}$, $V_{DD} - 2V_{on}$, $V_{DD} + V_{on}$, and $V_{DD} - 3V_{on}$, and $V_{DD} + 2V_{on}$, respectively. $V_{on}$ is the voltage drop caused by the on-resistance of switches, and $V_{DD}$ is the voltage shift caused by the CP input. Based on simulations of this 8-stage Dickson CP, $V_S$, which

![FIGURE 1. Dickson charge-pump: (a) schematic diagram ($N = 4$ for the sake of illustration), (b) corresponding waveforms, (c) equivalent model of (a), and (d) output voltage $V_{ramp}$ vs. time.](image-url)
is the steady-state output voltage of the Dickson CP, is estimated to be 5 V. $V_4$ transfers the generated voltage to $V_{\text{ramp}}$ output through the last-stage switch. The overall waveform of $V_{\text{ramp}}$ shown in Fig. 1(d) behaves as a charging ramp starting from 0 to $V_S$ exceeding the supply voltage $V_D$. Thanks to the proposed technique, it can be observed that the effective region from 0 to $V_D$ (shown in Fig. 1(d)) can exhibit better linearity as, for example, when using only a simple capacitor-resistor network that charges from zero to $V_D$.

**B. PROPOSED EQUIVALENT MODEL**

As presented in the simplified model of the proposed system in Fig. 2(a), $V_{\text{ramp}}$ generated by means of the Dickson CP is used as a reference to compare with samples $V_{\text{in}}$ of the input voltage $V_{\text{in}}(t)$. The output of comparator captures the timestamp $t_{\text{in}}$ when $V_{\text{ramp}}$ intersects with $V_{\text{in}}$ and it is further converted to digital domain by means of a TDC. Figure 2(b) shows the equivalent model of the ADC, consisting of a linear ADC that converts $V_{\text{in}}(t)$ to its equivalent normalized digital code $d_{\text{uncal}}$, i.e., $V_{\text{in}} \rightarrow 0 \ldots d_{\text{max}}$. By adding the non-linearity of the Dickson CP ramp signal, which is due to the exponential charge transfer characteristic of the Dickson CP, the equivalent model generates the final output digital code, $d_{\text{cal}}$. In the second part of the model, the deterministic distortion correction look-up table (LUT), implemented off-chip, is used to compensate the non-linearity derived from the exponential charge characteristic of the Dickson CP.

Based on the derived model of the Dickson CP shown in Fig. 1(c), the generated ramp can be written as:

$$V_{\text{ramp}}(t) = V_S \left(1 - e^{-\frac{t}{\tau}}\right)$$

(1)

$V_S$ is the steady-state equivalent voltage of the Dickson CP and $\tau$ represents the equivalent time-constant. Fig. 2(c) shows the generated CP ramp that maps the input signal $V_{\text{in}}$ to its equivalent timestamp $t_{\text{in}}$. With an assumption that all the interface blocks, i.e., S&H and TDC, are ideal and the only source of non-linearity is the Dickson CP, $t_{\text{in}}$ can be mapped as the un-calibrated digital code, i.e., $d_{\text{uncal}}$ in Fig. 2(b).

$$V_{\text{in}} = V_S \left(1 - e^{-\frac{t}{\tau}}\right)$$

(2)

Due to the exponential/logarithmic mapping transfer function of $V_{\text{in}}$ to $t_{\text{in}}$ and then eventually to $d_{\text{uncal}}$, the latter has a logarithmic format:

$$d_{\text{uncal}} = K_{\text{tDC}} \cdot t \cdot \ln \left(\frac{V_S}{V_S - d_{\text{lin}}}\right)$$

(3)

Equation (3) derives from (2) by inserting $d_{\text{uncal}}$ into $t_{\text{in}}$ with a time-to-digital converter (TDC) gain [LSB/sec], $K_{\text{tDC}}$. It makes an assumption that the only source of non-linearity in the proposed model is from the Dickson CP. As a result, $t_{\text{in}}$ can be mapped into the normalized output digital code. Therefore, the linearized CP ramp signal can be derived from (3) as:

$$d_{\text{cal}} = V_S \left(1 - e^{-\frac{d_{\text{uncal}}}{\tau_{\text{lin}}}}\right)$$

(4)

where $d_{\text{cal}}$ represents the final output code after the aforementioned distortion correction method. Following this approach, the correction LUT can be derived from the inverse of known characteristics of the Dickson CP, and implemented fully in the digital domain. If the nonlinear characteristic of Dickson CP can correctly match the proposed digital mapping, the normalized output code will be fully calibrated and so the output code will be linearized as follows:

$$d_{\text{cal}}(d_{\text{uncal}}) = d_{\text{lin}}$$

(5)

as a result of inserting (3) into (4).

Figure 3(a) shows simulation results of the normalized output signal of the Dickson CP vs. time. The CP of Fig. 1(a) is designed in 28 nm CMOS with $N = 8$ stages. It runs at $f_{\text{CLK}}$ of 400 MHz. Capacitors $C_{\text{out}}$ and $C$ are 2 pF and 30 fF, respectively. The critical node in terms of noise is the input of the VTC which has a smaller capacitor (i.e., $C$). By choosing 30 fF, the equivalent $KT/C$ noise will be $<400 \mu$Vrms.
which is sufficient for the required design specifications. Comparison of the results from theoretical modelling (with reference to (2), (3) and (5)) vs. simulated results of the derived reversed function of the CP voltage ramp shown in (4) and the calibrated ramp derived in (5) are also shown in Fig. 3(a). It can be observed that the simulation results for the implemented Dickson CP are in compliance with the derived model. The inverse and calibrated characteristics of the proposed technique are extracted from the previously derived (3) and (4).

The ramp generated by the CP is used as a reference to a comparator for pulse-width modulated output as it is compared to the sampled input voltage. To compensate for the CP non-linearity effects, the generated ramp signal \( V_{ramp} \) and its corresponding inverse function are combined to generate the calibrated ramp signal, which can be accurately pre-determined. Based on (4), a deterministic LUT is constructed to represent \( d_{cal} \) and nonlinear digital output codes can be corrected as shown in Fig. 3(b).

III. PROPOSED ARCHITECTURE

A. HARDWARE ARCHITECTURE

Fig. 4 illustrates a detailed diagram of the Dickson CP-based voltage-to-time converter (VTC) used in the proposed time-domain ADC. The CP is composed of \( N = 8 \) stages. This helps improving the linearity of \( V_{ramp} \) as higher \( N \) results in increased \( V_S \), as illustrated in Fig. 1. Furthermore, smaller \( C_{out} \) results in weaker filtering of the generated ramp. This can affect the ADC performance by increasing the ripple on the Dickson CP output due to its high-frequency clocking. A faster CP clock, \( CLK_{VTC} \), results in lower \( t_{vdd} \), allowing to use a faster ADC sampling clock, \( CLK_{REF} \), but also leads to higher power consumption while requiring more sensitive TDC due to the steeper slope of the generated ramp.

The \( CLK_{REF} \) and \( CLK_{VTC} \) signals terminate on the D-flip-flop (DFF) to generate a synchronized clock, \( CLK_{S_nq} \), which enables PWM and eventually resets all the Dickson CP capacitors when the generated ramp signal reaches \( V_{DD} \)

The CP is clocked at 400 MHz by \( CLK_{VTC} \). As it is toggling, output voltage \( V_{ramp} \) keeps increasing. The time at which \( V_{ramp} \) crosses the sampled input signal, i.e., \( V_{IN,S} \) will trigger the PWM pulse. At a later instance when the ramp signal \( V_{ramp} \) crosses over \( V_{DD} \), the output of the following latch comparator, in turn, triggers the reset of the Dickson CPs by shorting to ground their \( V_{1-S} \) internal nodes (shown in Fig. 1), until the next \( CLK_{S_nq} \) rising edge in order to avoid further increase in the \( V_{ramp} \) which can damage the devices. \( S\&HSIG \) feeds the AND gate to generate the falling edge of the PWM’s signal and is also being used as a controlling signal for the active-low S&H circuit in the proposed ADC. The falling edge of the PWM signal is being controlled not by the sampled input analog signal \( V_{IN,S} \) but by the discharging signal of the Dickson CP (i.e., \( S\&HSIG \)), in order to avoid intermodulation with the input analog signal which can increase the noise. Fig. 4(b) shows more details of the timing behavior of the controlling signal of the proposed ADC.

The detailed diagram of the proposed top-level architecture is shown in Fig. 5. It is composed of the core ADC operating at \( V_{DD} = 1 \) V, an LVDS receiver for the Dickson CP clock \( (CLK_{VTC}) \), output voltage level shifters for transmitting the output code \( D < 8:1 > \) to the off-chip data acquisition and off-chip digital mapping which linearizes the un-calibrated output code, as discussed in Section II. The core circuit is composed of the Dickson CP as VTC, sample and hold circuit (S&H), clock generator block, and TDC.

Fig. 6 reveals the schematic of the TDC which comprises an asynchronous 8-bit counter. It starts counting at the rising edge of PWM until the next rising edge of \( CLK_{S_nq} \). The generated quantized digital output \( D < 8:1 > \) bus will be sent to the level shifter at the falling edge of \( S\&HSIG \), while the counter still keeps counting, which helps relaxing the timing constraint between the counter resetting and data transferring phases, as shown at the bottom of Fig. 6.

B. DESIGN PROCESS

As shown in Fig. 1(c), increasing the number of stages, \( N \), can result in a higher steady-state voltage \( V_S \). From Fig. 1(d), higher \( V_S \) leads to a more linear ramp within the effective region spanning from the ground to the nominal supply voltage \( V_{DD} \). This leads to a more accurate voltage-to-time
conversion and ultimately to a more faithful PWM. To prove the concept described above, the time-domain equation of the generated ramp signal is derived as follows. From (1), assuming $V_{on}$ is negligible, as well as the peak-to-peak voltage of the clock buffers is equal to $V_{DD}$, $V_{ramp}$ can be derived as:

$$V_{ramp}(t) = (N + 1)V_{DD} \left(1 - e^{-\frac{t}{RSC_{out}}}\right)$$ (6)

Assuming, $V_{ramp}(t)$ reaches $V_{DD}$ at time $t = t_{vdd}$, as shown in Fig. 1(d), (6) can be re-written as:

$$R_S \cdot C_{out} = \frac{t_{vdd}}{\ln\left(1 + \frac{1}{N}\right)}$$ (7)

For a fair comparison of the $V_{ramp}$ linearity, we adjust $C_{out}$ such that $V_{DD}$ is reached at the same $t_{vdd}$ across all different cases of $N$. The deviation $V_{err}(t)$ of the generated ramp from the ideal linear ramp can be calculated as:

$$V_{err}(t) = (N + 1)V_{DD} \left(1 - e^{-\frac{t}{RSC_{out}}}\right) - V_{DD} \cdot \frac{t}{t_{vdd}}$$ (8)

The instantaneous voltage error during $t = 0 \ldots t_{vdd}$ can be re-written by substituting (7) into (8):

$$V_{err}(t) = (N + 1) \cdot V_{DD} \cdot \left(1 - \left(\frac{N + 1}{N}\right)^{-\frac{t}{t_{vdd}}}\right) - V_{DD} \cdot \frac{t}{t_{vdd}}$$ (9)

It can be observed that by adjusting $C_{out}$ for the ramp to hit $V_{DD}$ at $t_{vdd}$, the case of utilizing a larger number of stages (e.g., $N = 8$) will result in better linearity than when $N$ is lower (e.g., $N = 4$). This is illustrated in Fig. 7, which compares the ideal ramp with the ramps generated with $N = 4$ and 8 based on SPICE simulations in this TSMC 28nm LP CMOS technology.

By utilizing a higher frequency $f_{CLK}$ of clock $CLK_{VTC}$ to quickly reach the desired voltage level at the output of the Dickson CP, as described in Fig. 1(c), a faster sampling rate can be achieved. However, the higher sampling rate entails higher charging current with wider switching transistors as to reduce the on-resistance. Unfortunately, the larger transistors also increase the parasitic capacitance, ultimately resulting in larger voltage losses in the switches [19]. Additionally, the high-frequency clocking driving the capacitors in the Dickson CP (i.e., $C$ in Fig. 1) may generate ripples at the output due to the AC coupling from the clock generator to the Dickson CP output capacitor (i.e., $C_{out}$), deteriorating the linearity of the generated ramp signal. To avoid these issues, an appropriate ratio between the frequencies of $CLK_{VTC}$ and $CLK_{REF}$ should be carefully defined to achieve the targeted ADC resolution ($N_{ADC}$) within the corresponding input range ($V_{range}$).

Fig. 8 illustrates how the quantization effects at the output ramp of the Dickson CP can be lowered by increasing $f_{VTC}$. The quantization step is a function of a time step at the pumping stages which is inversely proportional to $f_{VTC}$. Assuming the same slope of the generated ramps, the quantization steps can be finer with increased $f_{VTC}$. To achieve this goal, the ratio of $f_{VTC}$ over $f_{REF}$ must be much higher than the total number of voltage steps within the range of the ADC convergence time. Unfortunately, this will lead to a difficult tradeoff with the efficiency of the CP switches.
and can contribute to unnecessary high power consumption. A condition to minimize the quantization effects caused by the high frequency clock can be written as:

\[ \frac{f_{\text{VTC}}}{f_{\text{REF}}} \gg \left( \frac{V_{\text{DD}}}{V_{\text{range}}} \times 2^{N_{\text{ADC}}} \right) \]  

(10)

By plugging in into (10) the design numbers \( f_{\text{VTC}} = 400 \text{ MHz}, f_{\text{REF}} = 0.6 \text{ MHz}, V_{\text{DD}} = 1 \text{ V} \) and \( V_{\text{range}} = 0.3 \text{ V} \), assuming that the analog input voltage range is one-third of \( V_{\text{DD}} \), we obtain (11) that meets the design specifications.

\[ \frac{400 \text{ MHz}}{0.6 \text{ MHz}} \gg \left( \frac{1 \text{ V}}{0.3 \text{ V}} \times 2^6 \right) \]  

(11)

On the other hand, the TDC comprises the DFF counter which counts the number of CLK VTC edges within the period of pulse generated (i.e., PWM) by the prior-stage Dickson CP VTC. As a result, the frequency of CLK VTC should be chosen such that the TDC gain matches with the maximum range of PWM. To meet the required specification, it can be written as:

\[ \frac{V_{\text{range}}}{V_{\text{DD}}} \times \frac{f_{\text{VTC}}}{f_{\text{REF}}} < 2^{N_{\text{TDC}}} \]  

(12)

In this design, it can be shown that the condition can be met as:

\[ \frac{0.3 \text{ V}}{1 \text{ V}} \times \frac{400 \text{ MHz}}{0.6 \text{ MHz}} < 2^8 \]  

(13)

It can be concluded that the given specifications meet the system design requirements for the resolution of the TDC (i.e., \( N_{\text{TDC}} \)).

Regarding the noise requirements, there are two separate parts to consider, i.e., \( kT/C \) noise of the capacitors in the Dickson CP at 1) the output capacitance \( C_{\text{out}} \), and 2) the pumping capacitors in the intermediate stages (i.e., \( C \)), see Fig. 1. The sum of these two noise contributions must satisfy the SNR requirements of the system. Assuming \( C_{\text{out}} = 2 \text{ pF} \) and \( C = 30 \text{ fF} \), the thermal noise budget for each section can be calculated as \( 45 \mu \text{V}_{\text{rms}} \) and \( 370 \mu \text{V}_{\text{rms}} \), respectively, which is much smaller than the target specification, i.e., \( 4.6 \text{ mV} \text{ LSB} \) \( (N_{\text{ADC}} = 6, \) and \( V_{\text{range}} = 300 \text{ mV} \)). Note that the noise of the charge pump circuit is limited by the output capacitor, i.e., \( C_{\text{out}} \), as described in [20]. A similar conclusion was obtained in [21] for a re-programmable switched-capacitor filter with a complex network of capacitors.

As far as the jitter requirement is concerned, Fig. 9 plots the conceptual diagram of the generated ramp from the Dickson CP VTC in the interval of \( t = 0 \ldots t_{\text{vdd}} \). It can be observed that the timing error or jitter \( (\Delta t_{\text{error}}) \) of the high frequency clock CLK VTC can be translated into voltage noise. Assuming a linear characteristics of the generated ramp, the slope can be written as \( V_{\text{DD}}/t_{\text{vdd}} \). To avoid the jitter affecting the targeted ADC resolution \( (N_{\text{ADC}}) \), the equivalent voltage error should be less than \( 1 \text{ LSB} \). For \( N_{\text{ADC}} = 6 \), the condition can be written as:

\[ \Delta t_{\text{err}} < V_{\text{LSB}} \times \frac{t_{\text{vdd}}}{V_{\text{DD}}} \]  

(14)

By inserting the targeted performance into (14), it can be ascertained that the timing error of CLK VTC should be less than 7.9 ns.

Fig. 10 shows the 500-run Monte Carlo circuit-level simulation of the comparator’s timing offset. The standard deviation (STD) of the timing offset reads 19 ns. Since it is constant and independent of the input, the comparator delay will merely add a constant timing offset equally for all the generated PWMs. Hence, the system linearity will not be affected.

IV. MEASUREMENT RESULTS

The microphotograph of the proposed ADC is shown in Fig. 11. It is fabricated in TSMC LP 28nm CMOS and occupies 0.04 mm². The total consumed power at the maximum conversion rate of 0.6 MS/s is 209 \( \mu \text{W} \), including input buffers and output voltage-level-shifters. The consumed power is broken down as: 25% for the clock buffer, 60% for the VTC, including the comparators and the Dickson CP, and 15% for the TDC and the level-shifter.
FIGURE 11. Die microphotograph.

FIGURE 12. DNL/INL measurement results: (a) before distortion correction, and (b) after distortion correction.

FIGURE 13. Dynamic characterization measurement result for $f_{in} = 23$ kHz, (a) before distortion correction, (b) after distortion correction.

The static linearity characterized at the 1 V nominal supply, 0.6 MS/s sampling rate and using a 3 kHz input sine-wave is shown in Fig. 12, demonstrating a differential (DNL) and integral nonlinearity (INL), respectively, equal to $+1.3/-0.45$ LSB, and $+1.5/-1.3$ LSB, after the correction. The dynamic linearity characterization of the converter is presented in Figs. 13 and 14, before and after the distortion correction, respectively. Two input frequency cases are applied: low-frequency (23 kHz) input sine-wave and a near-Nyquist 0.293 MHz at the maximum conversion rate of 0.6 MS/s. Note that matching of coefficients in the LUT could partially cancel out the second harmonic, but for the higher harmonics the task would be much more challenging due to the mismatch between LUT and process variation in the fabricated chip.

Fig. 15 shows the measured SFDR, SNR and SNDR across the sine-wave input frequency. The SNDR characterization over three different IC chips at 0.6 MS/s sampling frequency is shown in Fig. 16. Less than 15% performance variation can be observed, which indicates the robustness of our approach. Fig. 15 shows almost 15 dB improvement in the SFDR after the distortion correction, which is due to the suppression of the second harmonic of the output power spectrum, as shown in Figs. 13 and 14.
TABLE 1. Comparison table of state-of-the-art time-domain ADCs.

| Architecture   | Lin, JSSC'15 | Wang, TCAS'09 | Danesh, JSSC'13 | Shen, TCAS'11 | Chen, VLSI'16 | Straayer, VLSI'07 | Song, JSSC'00 | Wang, JSSC'09 | This Work         |
|----------------|--------------|---------------|-----------------|--------------|--------------|-----------------|--------------|--------------|------------------|
| Technology     | Pipeline     | ZCBC Time Domain | Time-interleaved | CP Pipeline | Two-stepTD | CT Delta-Sigma | Current Interpolate | Pipelined | Dickson-CP Time Domain |
| Sampling Rate (MHz) | 90 | 180 | 130 | 190 | 130 | 350 | 350 | 28 |
| SNDR (dB)      | 37.88        | 44.2          | 49.95           | 37.1         | 59.1        | 55              | 27           | 70.2         | 36.11            |
| ENOB           | 6            | 7.04          | 8.0             | 5.8          | 9.5         | 8.8             | 4.2          | 11.4         | 5.7              |
| FoM (pJ/Hz)    | 0.23         | 1.76          | 0.40            | 0.25         | 1.16        | 2.13            | 10.9         | 4.4          | 6.70             |
| Power (mW)     | 2.43         | 4.64          | 25.3            | 1.39         | 2.9         | 38.0            | 10           | 231          | 0.21             |
| Area (mm²)     | 0.25         | 0.84          | 0.55            | 0.04         | 0.07        | 0.19            | 4.8          | 7.5           | 0.04             |

FIGURE 16. SNDR variation for three different samples vs. input frequency: (a) before distortion correction, (b) after distortion correction.

The generated LUT, based on the proposed model and equation, was kept identical for all the three measured samples. It shows almost an identical performance improvement for all the three samples. Table 1 summarizes the ADC performance after the correction and compares it with state-of-the-art time-domain (TD) ADCs. The ADC achieves more than 1.5-bit and 9-dB improvement in ENOB and SNDR, respectively, thanks to the proposed affordable and digital friendly distortion correction technique to linearize the predictable non-linearity of the designed passive Dickson-CP-based VTC. Without any use of analog-intensive circuits for the VTC ramp generation, the proposed ADC can achieve good SNDR among state-of-the-art TD ADCs under a lower power consumption.

V. CONCLUSION

This article presents a time-based ADC employing a Dickson charge-pump (CP) for the purpose of ramp generation in a voltage-to-time conversion (VTC). The proposed ADC makes use of a well-behaved transient behavior of the Dickson CP to generate a ramp signal as a VTC and transmitting the modulated signal to a TDC for quantization. Using the Dickson CP as a VTC can potentially relieve various types of ADCs from using intensive analog circuits, such as current sources or OTAs, which can be rather challenging in advanced CMOS nodes. The proposed distortion correction technique generates look-up table values without any need for individual fine-tuning.

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