Design of Low-Power Low-noise CMOS ECG Amplifier for Smart Wearable Device

Yuze Yang
Department of Electronic Engineering, Xidian University, Xian, PR China.
Email: yuzeyangeecs@163.com

Abstract. The artificial intelligence health care devices have focused on the portability and accuracy and the most trending area of wearable biomedical application has become the electrocardiogram (ECG) recording device. The ECG signals have the characteristic of low amplitude, prone to be influenced by Power Line Interference (PLI), so it is essential to achieve high gain and high common-mode rejection ratio (CMRR), while the input-referred noise and power consumption need to be low to realize the cardiac screening system on chip (SoC). In this paper, a low-noise low-power analog front end (AFE) amplifier which based on Driven-Right-Leg circuit (DRL) has been proposed. It was implemented in CMOS 180 nm with bias current and supply voltage of 12µ A and 0.7V, respectively. The simulation results showed that this front-end circuit can achieve a low input referred noise of 4.11µ V/Hz and high common mode rejection ratio of 135dB. It also gave voltage gain of 41.8 dB with the bandwidth from 0.1Hz to 100Hz and the total power consumption was 4.32µ W. Compared with recently relevant whole circuit design, we believe that it is suitable to be used in smart wearable device.

Keywords: Low-power, Low noise, ECG, CMOS Amplifier, Smart Wearable Device

1. Introduction
As the recent advancement in artificial intelligence is touching the new heights, nowadays smart wearable devices have become more accurate, portable and more comfort to use with various features. To reduce the risk of fatality caused by cardiovascular disease, continuous monitoring of the ECG signal is highly desired in public community. ECG measurement setup consists of measuring the ECG signal from the human body by two electrodes, an AFE amplifier that amplifies the ECG signal, analog to digital converter (ADC) for digitizing the analog ECG signal, and a display device to monitor the patient’s heart regularly[1]. A typical three-electrode measurement is performed with the reference electrode connected at the right leg of the subject. The other two electrodes are at the subject’s chest and connected to the differential input nodes of the proposed amplifier. The block diagram of typical ECG monitoring system design is shown in Figure 1.

Nemievosky et al. [2] demonstrated the input referred noise and power spectral density model in saturation and subthreshold regions. They proposed an optimization method to reduce the noise by changing the aspect ratio. Yang and Hollema [3] illuminated dual stages, single ended input stage and differential second stage, and focused on supply noise cancellation which could achieve better NEF. Jie Zhang [4] presented a current-reused OTA which employed inverter-based differential pairs in the first stage to improve the power-to-noise efficiency, and class-AB output stage to enhance the $g_m/I$ efficiency. Study of these related works reveals the significance of low-noise and low-power preamplifier design with optimized device geometry to make a complete cardiac screening SoC that is
suitable to be used with the wearable devices and internet of things (IoT). Therefore, as a fundamental part, the design of low voltage, low-power analog circuits has become more important. [5]

Figure 1. Block diagram of ECG monitoring system

As the amplitude of ECG signal, varying from the microvolt to the millivolt range, is small, the signals need to be amplified properly in order to be better interpreted. Typical bio potential amplifiers have high input impedance and the output impedance of the amplifier should be low to cancel out any external load with minimal distortion. AFE is one of the key building blocks in the biopotential recording system [6–9]. As the heart signal is a low frequency signal ranging from 0.1Hz to 100Hz, flicker noise is prominent at low frequency in the circuit output. Unstable input offsets due to impedance between electrodes and skin cause the amplifier to be saturated easily. These noise and offset influence the preciseness of wearable monitoring system [10–12]. So the key specifications for a future realization of a SoC ECG monitoring system include low input-referred noise to detect the weak input signal down to μV level, minimum power consumption to increase the lifetime of the battery powered device [13].

This paper proposed a front-end ECG amplifier by using a standard 180nm CMOS technology with power supply of 0.7V. A pair of electrodes sense the differential ECG signal which was mixed with PLI from left arm and right arm. The signal amplifier was a modified two-stage three Instrumentation Amplifier (IA) design, which had high CMRR and low noise, while the DRL was introduced as Common-Mode (CM) interference suppression. The cut-off frequency was set up by pseudo-resistor and capacitor network in the 2nd stage of the signal amplifier and by the Miller capacitor in the OTA. The remaining part of the paper is organized as follows. Section 2 introduces the structure of main circuit components. The measurement results and the overall discussion are presented in Section 3. Section 4 concludes the whole paper.

2. Circuit Design

2.1 Instrumentation Amplifier Design

An instrumentation amplifier is constructed from three amplifiers, which is the main stage in an instrumentation system. The standard Instrumentation amplifier circuit is shown in Figure 2. As small voltages usually received from the probes need to be amplified significantly for being precisely detected, the following reasons elaborate the usage of instrumentation amplifier: High CMRR, High input impedance, High gain, High common-mode extraction.

The gain of the standard instrumentation amplifier circuit is given by

\[ V_{\text{out}} = V_{\text{in}} = \frac{A_v}{2} \left( V_{R2} - V_{\text{CM}} \right) \]

For \( R_2 = R_1 = R \) and \( R_1 = R_2 \),

\[ A_v = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{2}{1} \times \frac{R_2}{R_1} \]

(1)
IA is used to amplify low level signals and achieve higher differential gain. High input resistance and high CMRR is desirable for which unbalanced matching resistors are used [14]. This paper describes a new technique of designing a low-noise high gain CMOS instrumentation amplifier for ECG measurement. It modified the resistor network and introduced the capacitor network to perform better in the OTA. The capacitive feedback amplifier is a popular topology in biomedical recordings, which utilizes capacitors to set the mid-band gain to reject DC offset from the skin-electrode. The schematic design of proposed AFE is shown in Figure 3.

The function of the 1st stage is to provide enough differential gain to minimize the noise. The gain of the first stage is set by the resistor network. The second stage of the AFE consists of an OTA amplifier and capacitive feedback network with pseudo-resistor which occupies small area but can realize resistance larger than $10^{12} \Omega$ [4]. The function of the 2nd stage amplifier is to convert differential signal to single-ended signal and provide sufficient voltage swing. The mid-band gain of the second stage is set by the capacitor network. The lower cut-off frequency of the system, $f_L$, is given by $1/(2\pi R_p C_j)$, where $R_p$ is the 2nd stage MOS-BJT pseudo-resistor and $C_j$ is the feedback capacitor. The higher cut-off frequency $f_H$, equals to $\frac{g_{m,n1}}{2\pi AC_c}$, given by the transconductance of the first stage $g_{m,n1}$ and the Miller compensation capacitor $C_c$.

2.2 Main OTA Amplifier
Compared with the single-stage OTA architecture, the two-stage one is more commonly used in biomedical applications for its better linearity, and larger open-loop gain. At the input stage, inverter-based
input pairs are exploited to double the transconductance under the same bias current. Several considerations are counted into the amplifier design in order to eliminate the noise such as the transistor’s threshold biasing and circuit approach to get highest common mode rejection ratio (CMRR).

Subthreshold biasing of the transistors can reduce the transistor noise and the power consumption as the minimum operating voltage can be achieved. In fact, it is getting more attention in biomedical amplifier research in recent times due to the ability to design ultra-low power sensors and amplifiers for low frequency applications.

Sub-threshold equation for transconductance in sub-threshold region is shown in equation (2)

\[ g'_m = \frac{1}{NV_T} I_D \]

It shows that the transconductance of the transistor is linearly proportional to the biasing current ID rather than proportional to square root ID. Thus, lower current can be used to achieve the same amount of transconductance and gain of the amplifier leading to low power design.

\[ I_D = I_{DO} \left( \frac{W}{L} \right) e^{[V_{gs}-V_T (-\frac{L}{nKT})]} \]

\[ I_D = \frac{1}{2} K \frac{W}{L} (V_{gs} - V_T)^2 \]

As in equation (3), it shows the drain current of the transistor in subthreshold operation where \( I_{DO} \) is the current when \( V = V_T \). The current is directly proportional to the aspect ratio of the transistor, as similar to the transistor operation in saturation region, shown in Equation (4).

![Proposed Operational Transconductance Amplifier](image)

Figure 4. Proposed Operational Transconductance Amplifier

The overall structure of the main amplifier proposed in this paper is shown in Figure 4. The transistors sizing ratio especially near to the power supply are large to eliminate the flicker noise ad increase the CMRR as much as possible. Larger input transistors size ratio is also contributing to a higher gain due to the transconductance \( g'_m \) is directly contributing to the gain of the amplifier. For extracting good quality of ECG signal, high CMRR is required. This main amplifier has differential gain 37 dB. It generates a dc offset, for which electrode offset cancellation circuit is used. Two inverter-based pairs with large W/L ratio of 1000\( \mu \)/10\( \mu \) and 12\( \mu \)/2\( \mu \) working in the subthreshold region are used for transconductance boosting with current reuse and flicker noise suppression in the signal bandwidth. The upper cut-off frequency of the system is determined by the first stage OTA. Design performance optimization was done by repeatedly changing the value of Miller capacitor and the biasing current until
the performance specification was met.

2.3 Driven-Right-Leg Circuit

DRL is a well-established method for CM interference suppression. The DRL loop gain must be within the stable range, otherwise sufficient phase margin cannot be guaranteed and lead to potential oscillation. By shifting the DRL feedback point to the AFE amplifier output, the AFE amplifier is reused to provide the DRL loop gain and the loop dominant pole is pushed toward lower frequency to improve loop stability. In the DRL circuit configuration shown in the Figure 5, the two biasing resistors get the common-mode voltage. After inverting amplifying, the voltage which is opposite to the previous polarity feedbacks to right leg.

\[
U_0 = \frac{V_{i1} + V_{i2}}{2} - \frac{R_1 - R_2}{2(R_1 - R_2)} (V_{i1} - V_{i2})
\]

When \(R_1 = R_2\), \(U_0 = V_{cm} = \frac{V_{i1} + V_{i2}}{2}\). It is the common-mode interference. In DRL circuit, the value of \(R_0\) and the design of CMFB influence the performance of suppressing the PLI. \(R_0\) is significant to protect the body from leakage circuit through the right leg which must be lower than 0.1mA. When the CMFB is fixed, the lower the value of \(R_0\) is, the faster the common-mode signal attenuate. This means lower \(R_0\) is essential to cancel out the influence, but it will lead larger current into the right leg. After adding the designed DRL circuit, the whole design of the circuit is shown in the Figure 6.

![Figure 5. Driven-Right-Leg (DRL) circuit configuration](image)

![Figure 6. The whole circuit configuration](image)
3. Analysis of Circuit

3.1 Simulation Result
The circuit was designed in 0.18µm CMOS. It drew 12µA current from 0.7V supply. Although, at the input, the ECG signal was mixed with Power Line Interference which leads to distortion. After further processing by the DRL circuit, 60Hz PLI was effectively suppressed and the original ECG signal is possible to be recovered. Figure 7(a) shows the simulated transient response of the proposed ECG signal amplifier, there is few distortion in the ECG waveform. Figure 7(b) shows the simulated transient response without DRL circuit.

Figure 8(a) shows the periodic AC response of the proposed ECG signal amplifier, it had the characteristic of band pass filter. The dc gain of the amplifier equals 0 dB while the mid-band gain is 41.8dB. The low cut-off frequency and high cut-off frequency are 0.1 and 100Hz, respectively. The mid-band gain of the CMFB shown in Figure 8(b) is set to 0dB to avoid oscillation.

The simulated output noise power spectral density of the proposed amplifier is shown in Figure 9. Integrated from 0.1Hz to 100Hz, we obtained an input referred noise of 4.11µV/Hz.

Considering the noise efficiency factor $\text{NEF}$, it could be found that

$$\text{NEF} = \frac{2I_{\text{total}}}{V_{\text{INR}}} \sqrt{\frac{2 \pi U_T}{4kT \cdot BW}} = 21.99$$

(a) without DRL  (b) with DRL

(a) the proposed ECG signal amplifier (b) CMFB
Figure 9. The spectral density of output noise power

3.2 Comparison

Table 1 summarizes the main performance parameters of our preamplifier compared to state-of-the-art circuit design. Over the last years remarkable work has been done in this field. The proposed design achieved the best overall performance in power consumption and INR compared to previous work.[1, 14, 16-18]

|                | 2013[16] | 2016[17] | 2016[1] | 2018[18] | 2019[14] | This work |
|----------------|----------|----------|---------|----------|----------|-----------|
| Tech.[μm]      | 0.8      | 0.18     | 0.18    | 0.5      | 0.18     | 0.18      |
| VDD[V]         | 0.8      | 1        | 1       | 3.3      | 1.8      | 0.7       |
| Gain[dB]       | 40       | 56       | 40      | 32       | 65.88    | 41.8      |
| CMRR[dB]       | -        | -        | 3       | 88       | 136.05   | 132.2     |
| INR[μV/Hz]     | 36       | 60       | -       | 1.94     | -        | 4.11      |
| Power[μW]      | 30       | 3.25     | 86.3    | 28.05    | 1367     | 4.32      |

4. Conclusion

The electrocardiogram is an essential biomedical measurement in public community and an important clinical diagnostic tool. To measure ECG signal successfully amidst the PLI and other noise, it requires subtle design. This paper describes a low-power low-voltage amplifier design in 180nm CMOS process using DRL circuit to reduce the PLI. The amplifier achieves gain of 41.2 dB, CMRR of 135 dB, and input referred noise of 4.11μV/Hz. The lower cut-off frequency of the system is determined by 2nd stage pseudo-resistor and capacitor network at 0.1Hz, while the upper cut-off frequency of the system is determined by the Miller capacitor in the OTA at 100Hz. This amplifier design could achieve lower power consumption of 4.32μW which presents a better performance and is suitable to be implemented into a smart wearable device. However, compared with other state-of-the-art designs, the NEF of this design is still too high. In the future design, a better-adjusted OTA and circuit topology are needed to decrease the noise and lower the total power consumption.

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