TECHNICAL NOTE

The pitfalls of planar spin-glass benchmarks: raising the bar for quantum annealers (again)

Salvatore Mandrà1,2,7, Helmut G Katzgraber3,4,5 and Creighton Thomas6

1 Quantum Artificial Intelligence Lab., NASA Ames Research Center, Moffett Field, CA 94035, United States of America
2 Stinger and Ghaffarian Technologies, 7701 Greenbelt Road, Suite 400 Greenbelt, MD 20770, United States of America
3 Department of Physics and Astronomy, Texas A&M University, College Station, Texas 77843-4242, United States of America
4 1QB Information Technologies (1QBit), Vancouver, British Columbia, Canada V6B 4W4
5 Santa Fe Institute, 1399 Hyde Park Road, Santa Fe, New Mexico 87501 United States of America
6 Google Inc., 111 8th Avenue New York, NY 10011, United States of America
7 Author to whom any correspondence should be addressed. E-mail: salvatore.mandra@nasa.gov, hgk@tamu.edu and creightonthomas@gmail.com

Keywords: quantum annealing, spin glasses, P versus NP, exact algorithms, benchmarking

Abstract

In an effort to overcome the limitations of random spin-glass benchmarks for quantum annealers, focus has shifted to carefully crafted gadget-based problems whose logical structure typically has a planar topology. Recent experiments on these gadget problems using a commercially available quantum annealer have demonstrated an impressive performance over a selection of commonly used classical optimisation heuristics. Here, we show that efficient classical optimisation techniques, such as minimum-weight-perfect matching, can solve these gadget problems exactly and in polynomial time. We present approaches on how to mitigate this shortcoming of commonly used benchmark problems based on planar logical topologies.

1. Introduction

The quest for quantum speedup using analogue quantum annealing machines with a transverse field remains elusive. There have been multiple attempts [1–5] to demonstrate that the D-Wave Systems Inc. quantum annealer can outperform classical optimisation methods. Unfortunately, it has been relatively straightforward for classical optimisation algorithms to stay ahead in this race [6]. Either the random spin-glass benchmark problems were too easy on the quasi-planar topology of the D-Wave quantum annealer [1, 3, 7], or the logical structure of carefully crafted problems designed to give the annealer an advantage have a trivial structure [5].

The notable advances made by D-Wave Systems Inc. in the development of medium-scale quantum annealing has inspired multiple corporations (e.g., Microsoft, Google and IBM) to further invest in quantum computing technologies in addition to large-scale government-funded projects. The D-Wave 2000Q device is a special-purpose quantum optimisation machine specialised in minimising quadratic unconstrained binary cost functions by means of quenching quantum fluctuations induced by a transverse field. The generic cost function to be minimised is given by

\[ \mathcal{H}_P = \sum_{i=1}^{n} J_{ij} \sigma_i \sigma_j + \sum_{i=1}^{n} h_i \sigma_i, \]

where the \( n \) variables \( \sigma_i \in \{ \pm 1 \} \) are Boolean and the couplings \( J_{ij} \in \mathbb{R} \) and biases \( h_i \in \mathbb{R} \) are the parameters that define the problem to be minimised. In the case of the D-Wave chip, these variables are arranged in the so-called Chimera topology [8]. Real-world applications then require the embedding of the problems onto this topology, thus typically resulting in an embedding overhead that results in logical problems with less sites than the native topology of the chip. As such, it is desirable to find classes of problems for benchmarking that ideally use the complete set of variables on the chip, while not being a trivial optimisation problem [1].
There have been multiple approaches to harden the benchmark problems to be solved on different generations of the D-Wave device, ranging from post-selection methods based on statistical-physics metrics \cite{Denchev2} to the engineering of problems based on the classical algorithmic complexity of the Hamze--de Freitas--Selby \cite{Hamze, Selby} algorithm \cite{HamzeSelby2012}. Although these approaches generated harder problems for different generations of the D-Wave devices and there were some suggestions that there is some level of ‘quantumness’ in the device \cite{Selby}, only studies tailored to explicitly demonstrate quantumness, as well as attempt to determine (quantum) speedup \cite{Brighton, King} pushed the field forward noticeably. Both the studies of Denchev et al \cite{Denchev2} and King et al \cite{King} focused on the generation of logical problems designed to elucidate the value of quantum fluctuations, as well as to ‘fool’ archetypal classical optimisation algorithms (e.g., simulated annealing \cite{Lucas2011}, the classical pendant to quantum annealing \cite{Lucas2017, Lucas2018}) to become stuck in the carefully designed energy landscape of the problems. In \cite{King} it was subsequently shown that the use of state-of-the-art optimisation techniques beyond simulated annealing for the benchmarks designed in \cite{Denchev2} resulted in time-to-solutions scaling considerably better than the D-Wave device, as well as simulated quantum annealing. In this work we demonstrate that if the logical problems to be optimised on the D-Wave device have a planar structure, a quantum annealer would have to scale polynomially in the number of (logical) variables (i.e., be exponentially faster) to compete with the current classical state-of-the-art for frustrated problems on planar topologies, such as the minimum-weight perfect-matching (MWPM) exact algorithm \cite{Lucas2017-5, Lucas2018-5}. We emphasise that both the benchmark instances designed by Denchev et al \cite{Denchev2} and King et al \cite{King} suffer from the same problem. Namely, they can both be solved in polynomial time. Although one could, in principle, compare the quantum annealer against fast heuristics such as the Hamze--de Freitas--Selby \cite{Hamze, Selby} algorithm \cite{HamzeSelby2012} or parallel tempering Monte Carlo with isoenergetic cluster moves \cite{Lucas2011-5}, if claims of speedups over many orders of magnitude against classical algorithms are made, then the true state-of-the-art for planar topologies should be included in the study.

Although one might argue that exploiting the logical structure of the problem could be seen as ‘cheating’, combining MWPM techniques with simple cluster-finding and/or decimation techniques that are also polynomial in the size of the input would still scale exponentially faster than the D-Wave device. However, there would be no more guarantee for an exact result and the cluster-detecting MWPM algorithm could, at best, be seen as a heuristic that scales polynomial in the size of the input.

The paper is structured as follows. In section 2 we describe the crafted benchmark problem designed by D-Wave Systems Inc. \cite{King} and in section 3 we describe the classical algorithms and methods we used in our analysis of these problems. Results are summarised in section 4, followed by a discussion that also includes different strategies to design problems on quantum annealing machines that might have potential for quantum speedup and cannot be solved with polynomial algorithms for planar technologies.

2. D-Wave’s crafted problems

Given its hardware limitations, not all possible couplings $J_{ij}$ between two arbitrary qubits $i$ and $j$ can be set in the D-Wave quantum annealer. Indeed, only those couplings belonging to the native Chimera topology can be independently tuned within the range $[-1, +1]$, while the remaining are set to zero. The Chimera topology \cite{Fleming} is composed of $k \times k$ unit cells, each containing a $K_{4,4}$ fully connected bipartite graph of eight qubits. The unit cells are coupled together so that only adjacent unit cells share couplings. Despite the somewhat restrictive structure of the lattice, it can be shown that, in principle, any topology can be embedded, albeit at the cost of using multiple physical variables to define a logical variable.

In \cite{King}, the latest incarnation of the quantum annealer, namely the D-Wave 2000Q with over 2000 quantum bits, is tested using a set of carefully crafted optimisation problems also referred to as the ‘frustrated cluster loop’ (FCL) problems. One of the main characteristics which makes the FCL problems appealing for benchmarking is that many classical heuristics struggle with minimising the value of the cost function, even though the optimal configuration can be deduced by exploiting the actual structure of the problem \cite{Selby, King}.

Although the FCL problems can, in principle, be directly generated for the Chimera topology \cite{Selby}, the D-Wave Systems Inc. group has chosen a slightly different strategy, divided into two steps, which assists in elucidating the effects of the landscape ruggedness:

1. All couplings inside a $K_{4,4}$ unit cell are set to be ferromagnetic, i.e., $J_{ij} = -1, \forall i, j \in K_{4,4}$. Because the unit cells are fully connected, all the ‘physical’ qubits within a single cell are forced to behave as a single ‘logical’ qubit. This process generates a two-dimensional lattice with open boundary conditions of these logical variables.

2. The FCL instances are then generated on the logical topology with a varying level of ruggedness of the energy landscape and parameters $\alpha$ (clause-to-variable ratio) and $\rho$ (precision), as defined in \cite{Selby-2017}. Note that for the ruggedness $R$ we expect $R \gg \rho$. 


3. Methods

In this section, we briefly outline the algorithms used, as well as the definition of time to solution used in the benchmarks. Reference [19] provides the necessary details for the isoenergetic cluster move (ICM) heuristic.

3.1. Minimum-weight perfect-matching algorithm

The MWPM algorithm is an exact classical algorithm designed to find optimal configurations for planar two-dimensional spin-glass-like optimisation problems without biases (i.e., $h_i = 0, \forall i \in n$). The algorithm is polynomial in the size of the input $n$. The MWPM algorithm consists of three steps:

1. The planar spin-glass problem is mapped onto a minimum-weight perfect-matching problem.
2. The minimum-weight-perfect-matching problem is solved exactly using the deterministic Blossom algorithm [21] that scales polynomially in the size of the input.
3. The perfect-matching solution is then translated to the optimal configuration for the spin-glass problem.

3.2. Definition of time to solution

Heuristic methods, such as simulated annealing, simulated quantum annealing, the D-Wave 2000Q quantum annealer or isoenergetic cluster moves, can only determine the optimum of the cost function up to a probability $p$. If the optimisation procedure requires a certain time $T$, given that the optimum is only obtained with a probability $p$, it is necessary to define a time-to-solution (TTS). A simple (yet naive) possibility consists of making the observation that, on average, one needs to repeat the computation $\approx 1/p$ times in order to observe one optimal result. Therefore, for a computational time $T$, a possible definition of the TTS is

$$TTS_1 = \frac{T}{p}. \quad (2)$$

A commonly used and more accurate definition of the TTS that incorporates the cost of having uncertainty in the heuristic results is given as follows: let $k$ be the number of (unknown) iterations required to have a probability of success of at least 99%, i.e., $s = 0.99$. The probability that all $k$ attempts fail to find the correct answer is $P_{\text{wrong}} = (1 - p)^k$. Because an overall probability of success $s$ is needed, it is required that $P_{\text{wrong}} < s$. Therefore, $k$ must be at least $k > \log(1 - s) / \log(1 - p)$. Assuming that each attempt require $T$ times, the TTS can be defined as

$$TTS_2 = T \frac{\log(0.01)}{\log(1 - p)}. \quad (3)$$

Note that $TTS_2 < TTS_1$ at fixed $p$ and $T$. However, in general, $TTS_2$ is preferred, because it gives a lower bound to the overall probability. Reference [14] used the definition shown in equation (2). Using the raw data from [13], we have converted their results into the more commonly used TTS shown in equation (3).

4. Results

Figure 1 summarises our results where we compare the performance of the D-Wave 2000Q quantum annealer with both ICM and MWPM. The simulations were performed on a single core of an Intel(R) Xeon(R) CPU (E5-1650v2 with 3.50 GHz clock speed). While both the D-Wave 2000Q quantum annealer and ICM scale exponentially, MWPM scales polynomially with the size of the input. To show this in more detail, we generated artificial problems on perfect Chimera lattices of up to $256 \times 256$ logical variables. Although for small systems the D-Wave 2000Q chip is remarkably fast, only by doubling the largest number of logical variables on the chip results in MWPM outperforming the quantum annealer by approximately three orders of magnitude. One has
to remember, however, that the D-Wave 2000Q quantum annealer is a special-purpose machine designed to
minimise binary problems, whereas classical CMOS technologies require other processes to run, such as the
operating system, kernel and other concurrent processes.

Figure 1. Scaling of the TTS in μs as a function of logical variables in a log-log scale (left) or linear–log scale (right). Data for the D-Wave 2000Q (DW2000Q) quantum annealer for both definitions of the TTS are compared to MWPM and ICM. Because the maximal logical problem size is limited on the D-Wave 2000Q to 16 × 16 variables, we have generated artificial full Chimera lattices with no broken qubits of up to 256 × 256 K4,4 unit cells. Note that MWPM scales linearly in a log-log scale, whereas the D-Wave 2000Q scales exponentially. In all panels, data points represent the 50% of the TTS, while error bars represent the 5%–95% of the distribution. Although the D-Wave 2000Q is relatively fast for a small number of logical qubits n, MWPM quickly outperforms the quantum device by several orders of magnitude for the larger lattice sizes. Raw D-Wave 2000Q data taken from [13].

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5. Discussion

Although the D-Wave chip shows remarkable promise, in this work we show that benchmarks which encodes the logical problem on a planar topology is bound to fail in reaching the crown of quantum speedup. The quantum annealer would have to perform exponentially faster, in order to outperform the exact polynomial algorithm.

So how can we eventually prove the value of quantum annealing topologies? First and foremost, encode the problems in nonplanar logical topologies to ensure that no exact polynomial algorithms can be used. One possible approach we call ‘anticlusters’ (see figure 2) is to contract the links between the $K_{4,4}$ cells to become logical variables. This would result in a nontrivial nonplanar topology where each logical variable has 10 neighbours, except for the logical variables on the edges of the lattice which only have five neighbours. For a Chimera lattice with $c \times c$ $K_{4,4}$ cells (i.e., $8c^2$ physical qubits), the corresponding anticluster lattice would have $4c(c+1)$ logical qubits arranged on a square-lattice-like structure of linear dimensions $c \times c$. The large connectivity of the anticluster lattice, as well as the large number of logical variables allows for the generation of nontrivial benchmarking problems. For example, overlaying this topology that resembles the offspring of a farm fence with a square lattice with frustrated cluster loops or post-selected spin-glass problems, should generate hard benchmarks for classical algorithms.

A second alternative to demonstrate the capabilities of the D-Wave 2000Q is to use the machine as a physical simulator to study nontrivial quantum physics Hamiltonians [22]. Because these are very hard to simulate already for small numbers of variables, the D-Wave 2000Q might be able to outperform classical simulation techniques in the near future.

Acknowledgements

We thank the D-Wave team, in particular J King, for sharing their problem instances and raw data, as well as comments on the manuscript. We are also indebted to Richard Harris at D-Wave for sharing potentially groundbreaking, yet hopefully soon-to-be-published results. We thank H Munoz-Bauza for rendering the anticluster problems. HGK would like to thank Zheng Zhu for sharing his implementation of the ICM heuristic, as well as F Hamze and G Rosenberg for multiple discussions. HGK also thanks Franziskaner Naturtrüb for inspiration. HGK acknowledges support from the NSF (grant No. DMR-1151387). SM acknowledges Eleanor G Rieffel for the useful discussions and the careful reading of the manuscript. This research is based upon work supported in part by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA), via MIT Lincoln Laboratory Air Force contract No. FA8721-05-C-0002. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of ODNI, IARPA or the US Government. The US Government is authorised to reproduce and distribute reprints for governmental purpose notwithstanding any copyright annotation thereon.
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