Mining CryptoNight-Haven on the Varium C1100 Blockchain Accelerator Card*

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Abstract—Cryptocurrency mining is an energy-intensive process that presents a prime candidate for hardware acceleration. This work-in-progress presents the first coprocessor design for the ASIC-resistant CryptoNight-Haven Proof of Work (PoW) algorithm. We construct our hardware accelerator as a Xilinx Run Time (XRT) RTL kernel targeting the Xilinx Varium C1100 Blockchain Accelerator Card. The design employs deeply pipelined computation and High Bandwidth Memory (HBM) for the underlying scratchpad data. We aim to compare our accelerator to existing CPU and GPU miners to show increased throughput and energy efficiency of its hash computations.

Index Terms—FPGA Acceleration, Cryptocurrency, FPGA miner, Hardware miner, Cryptonight Haven

I. INTRODUCTION

Cryptocurrencies have become an increasingly popular medium for decentralized transactions in recent years. The computation of a cryptographic Proof of Work (PoW) is the foundational concept of decentralized consensus. It is computed by so-called miners, which are rewarded with a fraction of cryptocurrency for their effort. Currently, PoW computations are built by iterating a cryptographic hash function until the output has a dedicated form. This energy-intensive process presents a prime candidate for hardware acceleration.

Several cryptocurrencies adopt so-called ASIC-resistant PoW algorithms. These types of PoW aim to deter dedicated hardware miners in favor of CPU- and GPU-based miners, which are more generally available to the public, thereby sustaining the distributed ledger idea. The Haven Protocol [1] is one of the projects with such a goal. For its PoW, Haven leverages on a custom ASIC-resistant hash function named as CryptoNight-Haven.

In this project, we challenge the ASIC-resistance claims of CryptoNight-Haven, by implementing the PoW as an RTL kernel on FPGA. We target the Xilinx Varium C1100 Blockchain Accelerator Card [2]. The card employs Xilinx’ recent Ultrascale+ architecture, Xilinx Run Time (XRT) integration over a high-speed PCIe Gen 4 bus connection, and 8 GB of High Bandwidth Memory (HBM). Xilinx demonstrated that the Varium C1100 accelerates transaction validation in Hyperledger Fabric [3] over an Intel Xeon Silver 4114 CPU with a factor of 14×.

Our CryptoNight-Haven accelerator aims at a full hardware-based computation of the hash rather than software-assisted. It employs a pipelined datapath with multi-hash computation in a single kernel, and targets multiple kernel instantiations on a single FPGA with nonce-based HBM partitioning. We verified the computation modules under simulation; however, its memory interface demands improvements for random access rather than the simulator’s straightforward memory models.

Our CryptoNight-Haven miner RTL, testbench, and host-code (a software patch to XMRig [4] with XRT integration) are publicly available at: https://github.com/KULeuven-COSIC/CryptoNightHaven-FPGA-miner.

II. ALGORITHM

The Cryptonight-Haven algorithm is a variant of Cryptonight [5]. It chains together multiple well-known cryptographic primitives: AES, Keccak, Blake, etc. Collectively, these primitives are used to initialize a large scratchpad data buffer, on which semi-random operations are performed.

Figure 1 shows an overview of the computation flow. First, the input passes through a Keccak module, extracting the state. The explode module takes the first 32 bytes of the state and expands them to 10 AES round keys. These keys are used to perform AES rounds on the remaining bytes (divided into 8 blocks of 128-bits) of the Keccak state. After 10 rounds, the AES output is written to the memory buffer. Next, the blocks are XOR'ed with each other, and they again undergo 10 rounds

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of AES with the same keys as before. This process is repeated until 4 MB of data has been generated.

The Shuffle step performs a semi-random operation; either AES, a division, or a multiplication followed by addition. Corresponding input and output data yield intensive memory accesses to irregular addresses.

The Implode operation is similar to Explode. Bytes 32-63 of the state are used to generate AES round keys. Bytes are read from the start of the memory buffer and XOR’ed with state bytes 64-191. Subsequently, these bytes are put through 10 AES rounds – one round per key – and the next bytes in the memory buffer are read. After reading the entire 4 MB scratchpad buffer twice, the 10 AES rounds are repeated 16 additional times without reading from the memory buffer.

Finally, the new state passes through a Keccak permutation to generate the final state. Depending on the 2 LSBs of this state, it is subsequently hashed using either of the Blake, Skein, JH or Groestl schemes, resulting in the final 256-bit output.

III. IMPLEMENTATION

Our single accelerator kernel employs a datapath with a module hierarchy similar to Figure 1. The hash computations in the first and last steps of the computation stages contribute a negligible overhead. The Explode step consists of a simple implementation that generates 4 MB of data with simple binary operations and stores it into HBM memory. It heavily benefits from AXI burst transfers with multiple outstanding transactions. The Implode step has double the latency of Explode for accessing the memory twice. For the underlying computations, both the Explode and Implode modules employ 10 AES cores.

In contrast, Shuffle’s computation is demanding due to the multitude of iterations and underlying memory accesses. Additionally, data dependencies between consecutive accesses prevent optimizations, e.g. burst transfers. The memory size prevents using on-chip memory – BRAM or URAM – that allows single-cycle data access. Irregular addresses are another obstacle that prevents caching parts of the memory on-chip. Hence, minimizing data transfer overheads is the most advantageous strategy.

The memory accesses of Shuffle form one of the foundations for CryptoNight-Haven’s ASIC-resistance claims. Implementing these computations on an ASIC requires significant chip resources to be reserved for implementing memory, leaving a limited amount of silicon for the computation. In contrast, the Varium C1100 natively has 8 GB of HBM available, and our accelerator heavily benefits from it. Moreover, the partitioning of HBM into a number of Pseudo Channels (PCs) allows us to instantiate each Shuffle unit with a dedicated memory port, resulting in a scalable design.

We pipelined Shuffle for simultaneous computation of up to 128 hashes to boost the computation performance. That requires an identical increase in memory consumption – easily accommodated by the 8 GB HBM – where individual nonces for each hash computation partition memory regions. In line with this pipelining, we split the computation into various stages that communicate over AXI-Stream interfaces connected with FIFOs. Our pipelining approach allows the time-critical Shuffle module to be clocked at 500 MHz while the other modules remain at 200 MHz.

IV. FUTURE WORK

In its current state, our design computes hashes correctly within the Vivado simulation environment. That employs a simplified view of memory, which restricts the memory model to AXI accessed BRAM. However, when instantiated as an XRT kernel on the Varium C1100, the hash computations are inconsistent with simulation. We have enhanced the design with a set of AXI-lite accessible status registers that collect additional performance and debug information on the hardware execution. The further roadmap we envision is as follows:

1) Enhancing our Vivado simulation with random AXI access latencies and AXI protocol checkers.
2) Progressing with XRT kernel construction, by replacing the BRAM with HBM under Vitis hw_emu based XRT executions.
3) Extending Shuffle’s memory accesses with Xilinx’ Random Access Master Attachment (RAMA) IP.

After these steps enable the correct computation of the CryptoNight-Haven PoW, we have already taken the first steps to integrate the accelerator into XMrig [4] using XRT APIs. The accelerator should be compared thoroughly to existing CPU and GPU-based miners for Cryptonight-Haven, hopefully showing increased throughput and/or energy efficiency. Finally, we also aim to compare to related work: FPGA-based miners were proposed for the ASIC-resistant PoW Lyra2REv2 [6], [7], Scrypt [8], and X16R [9].

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