Special-Purpose Quantum Processor Design

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Abstract

Full connectivity of qubits is necessary for most quantum algorithms, which is difficult to directly implement on Noisy Intermediate-Scale Quantum processors. However, inserting swap gate to enable the two-qubit gates between uncoupled qubits significantly decreases the computation result fidelity. To this end, we propose a Special-Purpose Quantum Processor Design method that can design suitable structures for different quantum algorithms. Our method extends the processor structure from two-dimensional lattice graph to general planar graph and arranges the physical couplers according to the two-qubit gate distribution between the logical qubits of the quantum algorithm and the physical constraints. Experimental results show that our design methodology, compared with other methods, could reduce the number of extra swap gates per two-qubit gate by at least 104.2\% on average. Also, our method’s advantage over other methods becomes more obvious as the depth and qubit number increase. The result reveals that our method is competitive in improving computation result fidelity and it has the potential to demonstrate quantum advantage under current technical conditions.

INTRODUCTION

In recent years, quantum computing has progressed to a “Noisy Intermediate-Scale Quantum (NISQ) era” in which quantum processors have dozens to hundreds of noisy qubits.\textsuperscript{[1-3]} NISQ processors have short coherence time and quantum operations with nonzero error rates.\textsuperscript{[4]} Besides, only a subset of physical qubit pairs are coupled for two-qubit gates, i.e., the Physical Coupling Graphs (PCG) of NISQ processors are not complete. Here, the vertexes of the PCG are physical qubits and the edges are physical couplers. Quantum algorithms are represented by a quantum circuit model. In general, quantum circuits allow two-qubit gates to act on any qubit without restriction. Therefore, a transformation process that insert extra swap gates before two-qubit gates between uncoupled physical qubits to move the qubits to coupled qubits is required. Because swap gate consists of imperfect gates supported by NISQ processors, this process will significantly decrease the computation result fidelity.\textsuperscript{[5]}

To improve the fidelity, two solutions are proposed, one is finding the optimized transformation process on the fixed PCG to reduce extra swap gates.\textsuperscript{[6-23]} The other is designing the PCG according to a weighted Circuit Coupling Graph (CCG) of the quantum circuit. Here the vertex of CCG is logical qubit and the edge weight is the number of successive two-qubit gate blocks.\textsuperscript{[24]} Since the designed PCG is more suitable for the given CCG, the transformation process adds less swap gates than on fixed PCG. The commonly used PCGs are two-dimensional(2d) lattice graphs because they can be used in Quantum Error Correction (QEC)\textsuperscript{[25-28]} and fabricating these structures on superconducting system is technically practicable\textsuperscript{[30-31]}. In\textsuperscript{[24]}, the authors proposed a method that designs the PCG based on 2d lattice graph.

However, under current technology, NISQ processor has too few qubits to perform fault-tolerant universal quantum algorithms\textsuperscript{[22]}. Therefore, making quantum processor into lattice graphs is not necessary in the NISQ era. As the general CCG is not a lattice graph, we can extend PCG from lattice graph to general planar graph. Actually, in\textsuperscript{[1-3]}, we know that manufacturing the general planar PCG is also feasible.

In this paper, we propose a Special-Purpose Quantum Processor Design (SPQPD) method. The method extends PCG from lattice-graph to general planar graph. We first get the CCG of the circuit, and then arrange the physical couplers according to the CCG under physical constraints. Finally, we get a manufacturable PCG. When using realistic algorithms\textsuperscript{[45]} as circuit benchmarks, we find that compared with other methods, our method, on average, reduces the extra swap gate number by at least 104.2\%. To further verify the effectiveness of SPQPD, we use a series of random circuits as benchmarks and carry out the control variable experiments. When fixing qubit number, the number of extra gates in our method decreases as depth increases while other methods either increase or have no obvious trend; when fixing algorithm depth, the growth rate of extra gates to the qubit number is reduced at least by 37.1\%. The results reveal that the PCG designed by SPQPD outperforms its competitors. Hence, it has great potential to demonstrate the quantum advantage in the NISQ era.

If quantum processor has enough qubit resources for QEC, i.e., transformation won’t reduce the fidelity of the computation results, SPQPD method can still play an important role because it can reduce the number of swap gates, the depth of the circuits, and the time of quantum algorithm execution effectively.

RESULTS

Technical Constraints of Manufacturable PCG

There are some technical constraints to NISQ processor’s PCG structure.

\textbf{Maximum degree} The essence of the two-qubit gate is to entangle the control and target qubits\textsuperscript{[34-37]}. In superconducting system, the physical coupler that create entanglement
will interfere the working frequency of the qubit [22,33,38,41]. Thus fabricating entangled structure is non-trivial. There is a fully entangled structure [12] and the largest number of entangled qubits so far is 10. But its drawback is that the entanglement cannot be closed, which will create difficulties in the control of larger-scale quantum processor. Therefore, the current architecture still tends to establish entanglement between two qubits. Limited by the state of the art, the number of couplers on one qubit can’t be too large, i.e., there is a maximum degree of vertex in PCG. In this paper, the maximum degree is set to be 6 because the largest degree of 2d lattices [44] and the achievable highest degree of structures in [24] are 6.

**Planarization** Fabricating the 2d superconducting quantum processor is a mature technology [20,31]. Thus all qubits and couplers are placed on one layer and the couplers cannot cross each other in space. In the future, when multi-layer processor is available, some qubits or couplers can be placed on another layer. In this situation, for the couplers on the same layer, circuit transformation is still of great essential [15,16] and SPQPD can play a significant role. For this reason, a legitimate PCG should have a way of embedding to 2d plane without edge-interaction except at vertexes, i.e., the PCG should be a planar graph.

**Profiling the Coupling Information**

To design the quantum processor, we should profile information about the quantum circuit. The number of two-qubit gates between vertexes pair is the key information to bridge the quantum circuit and processor, because there are a large number of two-qubit gates in a circuit while NISQ processor has extremely limited coupler resources. Designing a quantum processor according to the number of two-qubit gates is expected to dramatically reduce the number of extra gates. For this reason, two-qubit gates information should be profiled.

Fig. 1 are three examples of profiling the coupling information of a quantum circuit. These examples indicate the existence of different CCG patterns. Fig. 1(a) is an example of the phase estimation algorithm. Most of the weight is concentrated between q4 and other vertexes. Fig. 1(b) is an example of Grover’s search algorithm. The matrix elements are concentrated on the off-diagonal, thus the corresponding CCG forms a chain-like structure. Fig. 1(c) is an example of the Quantum Fourier Transformation (QFT) algorithm. All edges are equally weighted.

Fig. 1 illustrates that the quantum processors can be customized for different circuits. E.g., the q4 in fig. 1(a) need more coupler resources, PCG of fig. 1(b) should be designed as a chain structure and the coupler resources in fig. 1(c) should be arranged more uniformly.

**Pruning**

The second step is pruning the edges. After profiling, we get a CCG. Since the CCG often violates the constraints, fabricating quantum processor with the original CCG’s structure is intractable. Pruning some edges will reduce the degree, eliminate the intersections and make the CCG meet the constraints. To answer the question that which edges need to be pruned, we present the following facts.

First, if the edge is pruned, the two-qubit gates between the corresponding vertexes cannot execute directly, and swap gates are required. Second, since the weight is the number of two-qubit gates, pruning the edges with smaller weight can reduce the number of extra swap gates. Third, the vertex connected to more edges with larger weight should have more coupler resources. Finally, the pruned graph must be planarizable.

Hence in this section, our goal is to modify the CCG into a planar graph with only a few important vertexes with high degree. It is sparser than the original CCG, more flexible and maybe more similar to the original CCG than the PCG with lattice-graph structures. And a PCG that meets the constraints and is as similar to the original CCG as possible can be designed in the further step.

**Ranking Vertexes**

Here, we rank the vertexes according to their importance. The key idea of our method is giving more coupler resources to the more important vertex. Because the connection information (detail discussions are in the “METHODS” section) such as degree and weight of the connected edges of each vertex are different, it is natural to infer that the importance of vertexes is different. We define a metric of vertex importance in the “METHODS” section. Under the metric, if the edges connected to the less important vertex were pruned, fewer swap gates will be inserted in the transformation process.

Fig. 2 is an example design process from original CCG to the final legitimate PCG. This CCG is generated from a circuit provided by [35]. The sum of the edge weight connected to q6 is greater than that of other’s, so it is an important vertex that needs more coupler resources. After the ranking subroutine, the ranking result is q6, q7, q5, q3, q0, q4, q2, q1.

**Pruning Based on the Media Vertexes**

Now we should complete the pruning process according to the ranking result. Based on the ideas proposed above, we shouldn’t change the vertexes with high rankings, but prune the edges of the vertexes with lower rankings.

The original CCG fig. 2(a) violates the constraint of planarization, thus the pruning subroutine is needed. The ranking result shows that the most important and the second impor-
A media structure is a black box that behaves like the media vertex. Therefore, media structure should contain sufficient free connections for the non-media vertexes connected by the media vertex, i.e., \( k \leq Dn - e \), where \( D \) is the maximum degree, \( k \) is the number of non-media vertexes connected by original media vertex are \( q_0 \) and \( q_7 \). Fig. 2(c) is the pruning result of the media vertex number \( N = 1 \), where \( q_0 \) is chosen as media vertex. Fig. 2(d) is the result of \( N = 2 \), where \( q_0 \) and \( q_7 \) are both chosen as media vertexes. These media vertexes are not only the most important, but also serve as the path to execute the two-qubit gate between non-adjacent vertexes. After choosing the media vertexes, the edge that connect \( q_i, q_j \) is pruned if \( \{q_i, q_j\} \cap media\_vertex\_set = \emptyset \), where \( media\_vertex\_set \) is the set of media vertexes. The pruned edges are stored in a \textit{recover_set} that is useful in the “Recovering” section. The question of how many media vertexes should be selected is discussed in the “METHODS” section.

**Handling the High Degree Vertex**

**Splitting the High Degree Vertex**

The third step is handling the vertexes whose degree violate the maximum degree constraint. After pruning, although we have eliminated the intersections in the CCG and pruned some edges that violate degree constraint, the degrees of the media vertexes in the graph may still violate the constraint of the maximum degree. For this reason, the third step of SPQPD is adding ancilla vertexes and changing the media vertex into a structure with multiple vertexes. The logical qubit contained by the media vertex \( v \) now corresponds to one vertex \( v_i \) in media structure at a time. We connect a part of edges of media vertex to the ancilla vertexes to reduce the excessive degree. Fig. 3(a) and fig. 3(b) are two examples of reducing degree by adding ancilla qubits.

This step is defined as splitting media vertex. The media structure must satisfy the following four conditions. First, the media structure should be a connected graph. Therefore, for a media structure with \( n \) vertexes, the number of edges \( e \) of the media structure should satisfy \( e \geq n - 1 \). Second, as in fig. 3(a), from the external perspective of the media structure, media structure is a black box that behaves like the media vertex. Therefore, media structure should contain sufficient free connections for the non-media vertexes connected by the media vertex, i.e., \( k \leq Dn - e \), where \( D \) is the maximum degree, \( k \) is the number of non-media vertexes connected by original media vertex. Third, the graph of media structure should meet the technical constraints for manufacturable PCGs. Forth, the number of vertexes \( n \) should be as few as possible because increasing the number of ancilla qubits will increase the difficulty of processor manufacturing. The subroutine which can search for media structures based on these conditions will be discussed in the “METHODS” section.

**Allocating the Non-Media Vertexes**

After replacing the media vertex by media structure, we need to reconnect the non-media vertexes to the vertexes in the media structure. This step is called weight allocation and the allocation way is not unique. We should find an optimized allocation way to minimize the extra swap gates because of the following reasons.

First, because only one vertex \( v_i \) in the media structure contains the logical qubit of the original media vertex \( v \) at a time, swap gates are required if \( v_i \) doesn’t directly connected to the non-media vertex \( q_j \) when two-qubit gate \( g \) between \( q_i, v \) need to be executed immediately. To describe this, we define a matrix \( S \) whose element is the sum of the number of the two-qubit gate blocks in two subcircuits only about vertexes \( q_m, v \) and \( q_i, v \).
Second, the non-media vertex are now connected by media vertex, swap gates are required when two-qubit gate between non-media vertices \( q_m, q_i \) need to be executed. The farther they are on the graph, the more swap gates are required. The adjacency matrix \( M \) can be used to describe this.

To describe how close \( q_m, q_i \) should be allocated on the media structure, we define an interaction matrix \( I \) whose element is \( I_{ij} = a^{M_{ij} = 1} (1-a) S_{ij} \), where \( a \) is the combination coefficient.

Another matrix required is \( C \) whose element is the shortest length between vertexes in media structure. Our goal is to find an allocation map \( alloc \) to let the score

\[
F = \sum_{i, j, alloc[i]=\text{alloc}[j]} C_{ij} I_{\text{alloc}[i]=\text{alloc}[j]},
\]

\[alloc : V \rightarrow 2^{\{q \in \text{neighbor of } v\}}\]

get the minimum value, where \( alloc \) is a map that allocates the neighbor of media vertex \( v \) to the vertexes in the media structure. \( V \) is the set of vertexes in media structure and \( v \) is the original media vertex.

In fig. 3c), \( N = 1 \), the most important vertex is \( q_6 \). Thus after the pruning subroutine, \( q_6 \) is selected as media vertex. \( q_6 \) violates the degree constraint and need to be replaced by a media structure. First, we try the media structure with two vertexes \( q_6, q_8 \) which meets the condition \( 1 = e \leq D_n - k = 6 \times 2 - 7 = 5 \). Then, the non-media vertexes are allocated according to the matrix \( I \). In fig. 3c), the elements in columns 3, 5, 7, 0 and 4 of \( I \) is relatively larger than columns 1 and 2, thus allocating the former 5 vertexes to the same vertex \( q_6 \) will let the summation terms in eq. (4) with larger \( I_{\text{alloc}[i]=\text{alloc}[j]} \) become zero and reduce the value of \( F \). After \( q_6 \) reaching the degree constraint \( D_{q_6} = 6 \), \( q_1 \) and \( q_2 \) have to be allocated to \( q_6 \), because they have less interaction with the former vertexes, the impact that their allocation is far away from the former important vertexes is smaller. Thus, the result is eq. (3), eq. (4) and fig. 2f).

\[ alloc[q_6] = \{ q_5, q_0, q_3, q_7, q_4 \}, \]

\[ alloc[q_8] = \{ q_1, q_2 \}, \]

where \( q_6, q_8 \) are vertexes in media structure and the others are the non-media vertexes needed to be allocated.

The media vertexes with more than two vertexes have multiple non-isomorphic topological structures. In this case, we should repeat the process above and find the structure with the smallest score \( F \).

**Recovering**

The fourth step recovering is to reconnect some pruned edges to the CCG. In fig. 2f), vertexes except for \( q_6 \) are far from the maximum degree, this means that some edges in the recovery set can be recovered to the CCG. Based on the idea that changing the subgraph with smaller weight and degree has less impact, the edge with larger degree has higher recovery priority.

**Fig. 4g)** is the final CCG of the routine. The structure of this CCG meets the constraints mentioned above, so it is also a legitimate PCG structure that can be implemented by the superconducting system.

**Comparing the Number of Extra Swap Gates Using 158 Benchmarks**

Finally, we use a series of circuits as benchmarks to test SPQPD method and compare it with other lattice-graph struc-
tures. 158 circuits are used for the experiment [48]. Triangular lattice structure, the 2d planar lattice structure that with the largest degree 6 [44], structures designed by the method in [23] and cross square lattice structure based on the same foundation as the Li’s structure are used as representatives of lattice-graph structures.

We define the metric as the number of extra swap gates per input two-qubit gate $g_{ap} = \frac{g_{ori}}{g_{ori} + g_{add}}$, where $g_{ori}$ is the number of extra swap gates and $g_{ori}$ is the number of original two-qubit gate.

Fig. 4(a)-(d) are the histograms of $g_{ap}$ for four kinds of structures. The results show that on average, the SPQPD method has the best performance and its average $g_{ap} = 0.072$. It is improved by 104.2% compared with the second-best structure, the triangular lattice structure. In fig. 4(a), a majority part of $g_{ap}$ belongs to the smallest interval, which means that the SPQPD method can design the most suitable processor for a quantum algorithm.

Using Random Circuits

To further verify the effectiveness of SPQPD method, we evaluate its performance to circuits with different qubit numbers and depth. Random circuits within the desired qubit number and depth range are generated for such evaluation.

Since NISQ processor has dozens to hundreds of qubits, we set the range of qubit numbers to be [30, 300]. The order of the coherence time is in [10, 200]μs and the gate execution time satisfies $t_{gate} > 10$ns. Based on the data and the noise model in [32], if we choose $T = 100$μs, $t_{gate} = 20$ns, for a circuit with depth $d = 2000$, after rough calculation, the fidelity of computation result is less than 70%. At this depth, the fidelity is very low, thus the circuit depth won’t exceed a few thousand and we set the range of depth to be [50, 2000].

Fig. 5(a)-(b) shows the process of information profiling. In fig. 5(a), we sample 100 random circuit outputs. Error bars are obtained by computing the credible intervals for the data set of circuits with the same size. These intervals are computed with normal distribution, with a credible level of 95%. This ensures that the mean value is inside the credible interval with a probability of at least 95%.

In fig. 5(a), if we consider the mean value $(g_{ap})_d$ of every data bar of circuits with depth $d$, the structures designed by the SPQPD method has the smallest $(g_{ap})_d$. To find out the trend of $(g_{ap})_d$ as depth increases, we use the Mann-Kendall trend test [50]. After computation, the statistics $Z$, for SPQPD, triangle structure, Li’s structure, and cross square structure are $-3.92$, $-0.12$, $0.59$, and $2.81$. Therefore, at the significance level $α = 0.05$, the SPQPD method has a decreasing trend, cross square structure increasing and the other two have no obvious trend. This result reveals that the SPQPD method has good scalability for depth.

In fig. 5(b), the $g_{ap}$ increases as the qubit number increases. Using linear regression, the slope of the SPQPD method is the smallest one 0.0105. The growth rate of SPQPD method is improved by 37.1% compared with the second-best method, Li’s method.

In summary, all results show that the SPQPD method can design the most suitable planar quantum processor for quantum algorithm. It is an effective way to reduce the number of extra gates and improve the computation fidelity. As the scale of the algorithm expands, the structure designed by the SPQPD method’s advantage becomes more obvious over other structures.

DISCUSSION

To improve the quantum computation fidelity, instead of following the old paths of optimizing the transformation process or designing quantum processor with lattice-graph structures, we come up with an idea that designing the quantum processor with general planar graph structures according to the quantum algorithm. In particular, we formalize our SPQPD method with four steps: profiling two-qubit gate information, pruning edges of unimportant vertexes, handling the high degree vertexes, and recovering the edges with large weights. The numerical experiments show that SPQPD method is a competitive alternative approach to improve the computation fidelity when executing quantum algorithms on NISQ processor. Therefore, the SPQPD method has great potential to demonstrate the quantum advantage in the NISQ era.

In conclusion, this work explores a step in mitigating the quantum software-hardware gap and provides a new idea for the development of special-purpose quantum processor. With the development of technology, SPQPD method might be used in the design of larger NISQ processor and multi-layer processor. Even after fault-tolerant quantum computation is realized, the SPQPD method will still have practical significance. PCG designed for certain CCG can reduce the number of swap gates and the circuit depth and therefore result in decreasing the execution time of quantum algorithms.

METHODS

Profiling Subroutine

We ignore all single-qubit gates, initialization, and measurement operations, and combine the two-qubit gates which act on the same two qubits successively. The reason for combining is that if the current map allows the first gate to be executed directly, then there is no need for more swap gates for the successive two-qubit gates. Therefore, in the circuit transformation process, they can be seen as a whole block. After counting the number of two-qubit gate blocks, we get the adjacency matrix $M$ and the corresponding CCG.

Fig. 6 shows the process of information profiling. In fig. 6(a), after ignoring the one-qubit gates and measurement operations, we find that the two CNOT gates between $q_0$ and $q_1$ can be combined as one two-qubit block. The other CNOTs are two-qubit blocks themselves. Fig. 6(b) is the adjacency matrix of the circuit, whose element with index $m, l$ represents the number of two-qubit gate blocks between $q_m$ and $q_l$. Fig. 6(c) is the corresponding CCG of fig. 6(b). The relative width of the edges represents the relative size of the weight.

Vertex Ranking Subroutine

At first, we need to define some concepts about the connection information of the vertexes.

**Definition 1** The total weight of vertex $q_m$, $W_m = \sum_{l}M_{ml}$, representing the sum of total two-qubit block number of a vertex.

**Definition 2** Weight dispersion of vertex $q_m$, $\sigma_m$, representing the deviation of the number of two-qubit blocks the vertex executes with each of its neighbors.

Based on the definitions and the discussion above, we choose the following three indicators to evaluate the importance of vertexes.

**Vertex degree** $D_m$, the larger the degree of the vertex is, the more important the vertex is.

**Total weight**, according to def. 1, the larger the total weight, the more frequently this vertex executes two-qubit gates with its neighbors, and thus more important the vertex is.
Weight dispersion, the smaller the weight dispersion, the more important this vertex is. The reason why we introduce this indicator will be discussed in the Recovering Subroutine.

Vertexes are sorted by these three indicators in lexicographic order.

Pruning Subroutine

The first step is choosing the top $N$ most important vertexes as media vertexes. The second step is pruning the edges on the graph that don’t connect to the media vertexes. The third step is storing those pruned edges to a recover_set.

Media Structures Searching Subroutine

We search for all candidate media structures that are not isomorphism with each other with $n$ vertexes and delete those violate the constraints. $n$ is searched from small to large within this range $[2, \infty]$. If legitimate media structures are found with $n$ vertexes, the searching process stops immediately. Because the greater the number of ancilla qubits, the more difficult it is to manufacture the quantum processor. All of these media structures with $n$ vertexes will be stored and be used as candidate media structures in the following “Weight Allocation Subroutine” subsection.

Weight Allocation Subroutine

First, we compute the element of interaction matrix $I_{ml} = aM_{ml} + (1 - a)S_{ml}$. We give an example fig. 7(a) of the computation of $S_{ml}$ between $q_m$ and $q_l$. When only $q_m$, $q_l$ and $v$ are of interest, we ignore the operations between other vertexes (the red ones), and combine the successive blocks together. At last, we get the sum of the number of the two-qubit blocks in the subcircuits of $q_m$, $v$ and $q_l$ which is $S_{ml} = 2 + 1 = 3$.

Then for every media structure, we compute the element of matrix $C$, whose elements are the shortest length between $v_i$, $v_j$ in the media structure.

If no non-media vertex has been allocated on the media structure, we comcompute the indicator,

$$E_m = \sum_l I_{ml},$$

and choose the largest $m$ as the index of the first non-media vertex to allocate. And the location is the vertex with the largest degree under the degree constraint.

Else if there are non-media vertexes have been allocated, we compute another indicator

$$E_m = \sum_{l \in \text{non-media vertexes have been allocated}} I_{ml},$$

and choose the largest $m$ as the index of next non-media vertex to allocate.

To find the best location for the non-media vertex $q_m$, we compute

$$s_i = \sum_{j, alloc[j]} C_{ij}I_{alloc[j],m},$$

for every $v_i$ and the $v_i$ with the smallest $s_i$ will be connected to the $q_m$, $alloc[i] \rightarrow alloc[i] \cup q_m$. If the degree of $v_i$ break the maximum degree constraint, we repeat the procedure that excluding $v_i$ and choose the $v_j$ with the second smallest $s_j$ until the constraint is met.

Compute the score according to eq. (1) and choose the media structure with the smallest $F$.

Recovering Subroutine

We sort the recover_set from large to small by weight. Then we try to add the edges to the CCG in the order of recover_set. If the CCG doesn’t violate any constraint after edge addition, then updates the CCG, otherwise, delete the edge we add.

The reason that why the vertex with smaller weight dispersion is more important is as follows. As in fig. 8 in both cases, the vertexes in the middle have the same total weight, while the fig. 8(a) has a smaller weight dispersion. As a result, the weight dispersion of edges that are not connected to the media vertex is smaller. For instance, more weight is concentrated on the one edge weight 7 in fig. 8(a). While in fig. 8(b), the largest weight of edges is only 4, and we can only recover total weight 8 by recovering two edges. Consequently, in fig. 8(a), more weight can be recovered by recovering fewer edges.

Determining the Number of Media Vertexes

We should decide how many high ranking vertexes should be chosen as media vertexes because different circuits have very distinct patterns. E.g., fig. 1(c), is very different from fig. 1(a).
It is reasonable to choose just one media vertex for fig. 1(a) since almost all weights are concentrated on the edges connected to one vertex. While in fig. 1(b,c), the weight distribution is uniform. Choosing one media vertex will lose a lot of weight. Therefore, we try $N$ from 1 to the number of CCG vertexes and compute the score $S = \sum_{m=1}^{N} \sum_{q=l}^{d_{ml}} M_{ml}$, where $d_{ml}$ is the shortest distance between $q_{ml}$, $q_{l}$ on the PCG. The smallest score $S$ corresponds to the best choice of the number of media vertexes.

**Experiment setup**

**Benchmarks** 158 quantum programs are collected from IBM’s qiskit. These benchmarks cover several important fields and have various sizes for a versatility test of the proposed SPQPD method.

**Hardware Model for Comparison** We use cross-square structure, triangular lattice structure and the structures in [24] as representatives of lattice-graph structures and compare them with the SPQPD structure.

**Circuit Transformation Method** The PCG produced by SPQPD is different from the original CCG. Thus, optimized transformation process are still required. To illustrate the improvement of our method, for all the structures, we use the same Sabre transformation method provided by IBM qiskit.

**Simulation Tools**

The simulation and compilation of quantum algorithms are completed by an open-source software development kit (SDK) IBM qiskit.

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