Implementation of LDN to MLI and RSC-MLI configurations with a simple carrier-based modulation

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Abstract. The design of multilevel inverters (MLI) and reduced switch count (RSC) MLIs majorly depend on the requirements of desired output voltage levels, number of dc sources switching devices, and their ratings. With regard to these requirements ‘Level Doubling Network (LDN)’ configuration is introduced. LDN has the ability to double the output voltage levels of any MLI or RSC-MLI, preserving inverter modularity. However, the implementation of LDN to MLI or RSC-MLI is not unified and varies with switching operations. Thus, this work presents the implementation of LDN to popular MLI and RSC-MLI configurations and further presents a brief comparison on the switch count, number of levels, and harmonic performance for both LDN and non-LDN cases. Further, a generalized carrier-based PWM scheme is presented to implement the LDN for any MLI and RSC-MLI configurations irrespective of voltage levels, dc-voltage ratios, and topological configuration. The performance of the inverter and the proposed modulation scheme are validated on MATLAB/Simulink environment.

Keywords. Level doubling network, multilevel inverter, H-bridge, PWM, RSC-MLI

1. Introduction
Day after day, the world's population is growing more and more so that the need for electricity is rising. To meet the demand for bulk loads, power generation should be increased, which is difficult to accomplish only from non-renewable sources of energy. The demand for renewable energy sources is therefore strong. This further created complexity issues and increased the significance of grid integrated systems dominated [1-4]. Thus, the significance of inverter which can survive for high and medium power conditions became crucial. Most often an inverter designed for high/medium power grid-connected systems is supposed to meet few key objectives for providing grid-connected service. The first objective is inverter must produce a proper sinusoidal voltage at the load end. The second objective is the load current of the inverter must have a low total harmonic distortion (THD)[3-11]. However, the ability of multilevel inverters (MLIs) to improve harmonic performance and sustain
high and medium power conditions with matured medium power electronic devices enhanced their prominence in grid-connected systems for high voltage, high-power applications [7, 12-15]. In addition, its ability to operate with low input dc requirement turned MLIs viable for low-medium voltage PV based standalone and grid-connected systems. Further reduction in \( \frac{dv}{dt} \), common-mode voltage, and filter requirements are the added advantages of MLIs [1-12,13]. Though MLIs are able to produce any number of levels in output voltage, however, their increase in output voltage levels increased the switch count and imposes enormous limitations on inverter size and complexity for high levels. Hence, the demand to simplify the circuit configuration of MLIs for higher levels enhanced the prominence of reduced switch count (RSC) MLIs. Though numerous topological configurations of RSC-MLI are reported in the literature, only a few of them possess practical feasibility. Among the RSC-MLIs reported, the concept of level doubling network (LDN) turned highly popular.

This paper presents a nine-level RSC-MLI configuration and investigates its harmonic performance for different switching frequencies. To resolve the problems associated with the nine-level inverter and, increase the number of levels without effecting device ratings a seventeen-level RSC-MLI with LDN network is proposed and implemented. Further, the comparative performance of LDN and non-LDN configurations is presented for the same maximum output voltage and system ratings.

2. System description

2.1. Reduced switch count multilevel inverter topology

The per-phase structure of considered RSC-MLI for nine-level is shown in figure 1. As seen in figure 1, the considered RSC-MLI posses a separate level and polarity generator. All switched indexed with ‘S’ corresponds to level-generator and, all the switches indexed with ‘H’ corresponds to polarity generator. Level-generator produces a uni-polar stair-case voltage waveform comprising all the desired magnitude levels in output voltage. Further, polarity generator converter the uni-polar output obtained form level generator to bi-polar. The switching operation of this nine-level RSC-MLI to produce the required nine-level output voltage is depicted in table 1. It is to be noted that switching devices in polarity generators are rated for total dc-link voltage i.e, 4Vdc and, operate at modulating frequency. Thus refereeing to the operating frequency, these devices can be termed as fundamental frequency switching devices. On the other hand devices in the level generator are rated for Vdc and operate at a carrier frequency. Further to minimize system cost and increase efficiency, the device ratings of level and polarity generator must be properly selected according to the rated power of the inverter circuit.
Figure 1. Per-phase structure of nine-level RSC-MLI.

Table 1. Switching paths of nine-level RSC-MLI to produce nine-level phase voltage.

| Level  | S1 | S2 | 0  | S4 | S5 | S6 | S7 | S8 | H1 | H2 | H3 | H4 |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|
| -4Vdc  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 0  |
| -3Vdc  | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 0  |
| -2Vdc  | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 0  |
| -Vdc   | 0  | 1  | 1  | 1  | 0  | 1  | 0  | 0  | 0  | 1  | 0  | 0  |
| 0      | 0  | 1  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| Vdc    | 0  | 1  | 1  | 1  | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 1  |
| 2Vdc   | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 1  | 1  | 0  | 1  | 1  |
| 3Vdc   | 0  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 1  | 1  |
| 4Vdc   | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 1  |

2.2. RSC-MLI operation

The load voltage of the Reduced switch count (RSC) Multi-level Inverter shown in figure 1 has nine levels ranging from \( \pm 4 \) Vdc, with a step size of Vdc. It is to be noted that this work incorporates the popular Phase opposition disposition with reduced carrier arrangement to realize the PWM [2].

To synthesize this desired voltage levels, the complete switching operation is divided into five different modes. These modes are classified referring to the instantaneous magnitude of modulating signal with respect to the carrier limits. All the considered modes of operation with respect to the instantaneous magnitude of reference (modulating) signal (Vref) and the peak value of the carrier signal (Vc) are given in Table 2. Pulse width modulation strategy based on Phase opposition disposition (POD) modulation involving only one reference signal and four carrier signals is proposed.
and a comprehensive PWM strategy is outlined. For \( V_{\text{ref}} > 0 \) the switch pair H1-H2 are turned ON and, further H3, H4 triggered for \( V_{\text{ref}} < 0 \). Thus, the H-bridge acts as a polarity generator by turning on and off once with respect to the modulating signal frequency. The voltage at the blocking state of the switch is 4Vdc. The generation of the PWM signal for level generator switches can be explained for mode 1 and follows for the remaining modes as shown in Table 2.

| Working Mode | Reference voltage | ON state Switches | Output – voltage |
|--------------|------------------|------------------|-----------------|
| Mode 1       | \( V_{\text{ref}} \geq V_c \) | S2, S3, S4, S6   | 4Vdc or -4Vdc   |
| Mode 2       | \( V_{\text{ref}} \geq 2V_c \) | S2, S3, S6, S8   | 3Vdc or -3Vdc   |
| Mode 3       | \( V_{\text{ref}} \geq 3V_c \) | S2, S6, S7      | 2Vdc or -2Vdc   |
| Mode 4       | \( V_{\text{ref}} \geq 4V_c \) | S1, S6          | Vdc or -Vdc     |
| Mode 5       | \( V_{\text{ref}} < V_c \) | S2, S3, S4, S5   | 0               |

Table 2. Shows operating according output for one working mode to the voltage cycle.

3. LDN derived topology

The LDN definition in [8] has shown that the number of level scans is almost double with the number of dc source, where a LDN shown in figure 3, is a single-phase H-bridge configuration [9,11] with two control semiconductor switches. The half-bridge subsidizes two extra voltage stages, this added voltage has only ac and harmonic component with regard to the main component of the load voltage. The half-bridge network fixed dc-bus voltage is exactly fifty percent of the consistent cascaded bridge source voltage. Power balancing occurs in one cycle, i.e generated power in the quasi cycle will be compensated in the remaining half interval. During the initial time or any transient period, LDN voltage should be maintained at half of the main inverter voltage to get symmetricity in output, results in less THD as marked in table 3.

| Working Mode | Reference voltage | ON state Switches | Output – voltage |
|--------------|------------------|------------------|-----------------|
| Mode 1       | \( V_{\text{ref}} \geq V_c \) | S2, S3, S4, S6   | 4Vdc or -4Vdc   |
| Mode 2       | \( V_{\text{ref}} \geq 2V_c \) | S2, S3, S6, S8   | 3Vdc or -3Vdc   |
| Mode 3       | \( V_{\text{ref}} \geq 3V_c \) | S2, S6, S7      | 2Vdc or -2Vdc   |
| Mode 4       | \( V_{\text{ref}} \geq 4V_c \) | S1, S6          | Vdc or -Vdc     |
| Mode 5       | \( V_{\text{ref}} < V_c \) | S2, S3, S4, S5   | 0               |

Table 3. Five level inverter(one H-bridge with single LDN).

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4. Proposed seventeen level inverter (RSC-MLI+LDN)

4.1. Operation
In the proposed topology as shown in figure 4, LDN inverter is connected in series to 9-level RSC-MLI inverter to generate a seventeen-level output. The 9-level reduced switch count inverter has 12 switches (S1 to S8 and H1 to H4), compared to traditional cascaded H bridge 9-level inverters [10] where 16 switches are essential. Double-level network forms with a single DC voltage source and two semiconductor power (S9, S10) units. If \(V_{dc}\) is known to be the dc-bus voltage of the RSC-MLI, then \(V_{dc}/2\) will be the dc-bus voltage of the corresponding LDN. The versatility of the LDN to have other voltage levels and the ability of the capacitors to sustain an open-loop voltage

The topology is shown in Figure 5 and can produce an output voltage of nine LDN-free levels (±4\(V_{dc}\), ±3\(V_{dc}\) ±2\(V_{dc}\), ±1\(V_{dc}\), 0\(V_{dc}\)) and seventeen levels: zero, eight positive voltage level, and 8 negative voltage level with LDN at unit modulation index.

| Switch | During positive voltage level | During negative voltage level | Both positive and negative voltage levels | Zero voltage |
|--------|-------------------------------|-------------------------------|------------------------------------------|--------------|
| S1     | 8 \(V_{dc}\)                  | 7 \(V_{dc}\)                  | 2 \(V_{dc}\) to 6 \(V_{dc}\)             | ON           |
| S2     | 7 \(V_{dc}\)                  | \(V_{dc}\)                    | 2 \(V_{dc}\) to 4 \(V_{dc}\)             | ON           |
| S3     | 5 \(V_{dc}\)                  | \(V_{dc}\)                    | 2 \(V_{dc}\)                              | ON           |
| S4     | 3 \(V_{dc}\)                  | \(V_{dc}\)                    |                                          | ON           |
| S5     | \(V_{dc}\)                    |                                |                                          |              |
| S6     |                                | 2 \(V_{dc}\) to 8 \(V_{dc}\)  |                                          |              |
| S7     | 5 \(V_{dc}\)                  | 7 \(V_{dc}\)                  | 6 \(V_{dc}\)                              |              |
| S8     | 3 \(V_{dc}\)                  | 5 \(V_{dc}\)                  | 4 \(V_{dc}\)                              |              |
| S9     |                                |                               | Odd levels (1, 3, 5, 7)                   |              |
Table 5. Output voltage and switching states (RSC-MLI with LDN).

| Level | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | H1 | H2 | H3 | H4 | S9 | S10 |
|-------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|-----|
| -8 Vdc| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 1  | 1  |
| -7 Vdc| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1  | 0  | 0  | 1  | 0  | 1  |
| -6 Vdc| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0  | 0  | 1  | 0  | 0  | 1  |
| -5 Vdc| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1  | 0  | 1  | 0  | 1  | 0  |
| -4 Vdc| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0  | 0  | 1  | 0  | 0  | 0  |
| -3 Vdc| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1  | 0  | 0  | 0  | 0  | 1  |
| -2 Vdc| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0  | 0  | 0  | 0  | 1  | 0  |
| -1 Vdc| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0  | 1  | 0  | 0  | 1  | 0  |
| 0 Vdc | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0  | 1  | 0  | 0  | 0  | 1  |
| 1 Vdc | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 1  | 1  | 0  | 1  | 1  |
| 2 Vdc | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1  | 1  | 1  | 1  | 1  | 1  |
| 3 Vdc | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1  | 1  | 1  | 1  | 1  | 1  |
| 4 Vdc | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1  | 0  | 1  | 1  | 1  | 1  |
| 5 Vdc | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0  | 1  | 1  | 1  | 1  | 1  |
| 6 Vdc | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1  | 1  | 1  | 0  | 1  | 1  |
| 7 Vdc | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1  | 1  | 1  | 0  | 1  | 1  |
| 8 Vdc | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1  | 1  | 0  | 1  | 0  | 1  |

A Multi-Level Inverter with all available modulation techniques, phase-shifted PWM (PSPWM), and level-shifted PWM (LSPWM) are easy to implement because they are carrier-based pwm method is used[5,6].The reduced carrier PWM [8] is the other common PWM that involves unipolar modulating and level-shifting carrier signals. This technique includes N-level inverter, (N-1)/2 carrier signals, and these carrier signals are produced...
by positive and negative voltage levels. The proposed 17-level inverter requires eight carrier signals from Cr1 to Cr8 as shown in figure 5, the required pulses are produced as shown in figure 8.

These pulses (P1 to P8) are created by comparing the reference to their carriers as shown in figure 5, and by user-defined logical expressions as shown in Table5 for the necessary switching pulses to control the inverter. The inverter of individual voltage signals depends on P1 to P8 and C1 to C8 signals, for example, the condition for generating first pulse P1 is Vref > Cr1, follows Table6 for the remaining seven pulses. By applying the Pn pulse > carrier over the Cn interval, the desired non-overlapped switching pulse occurs.

| P signal | condition |
|----------|-----------|
| P1 generates | Vref > Cr1 |
| P2 generates | Vref > Cr2 |
| P3 generates | Vref > Cr3 |
| P4 generates | Vref > Cr4 |
| P5 generates | Vref > Cr5 |
| P6 generates | Vref > Cr6 |
| P7 generates | Vref > Cr7 |
To generate sequential pulses (c1 to c8) depending on the voltage level, they are generated by the use of the XOR combination of A0 and A1 as shown in figure 6. In Table 7 C1 pulse is high when A0 and A1 are provided as an additional condition for A0 signals. During the interval when A0 and A1 are additional signals, C1 generates a high-level pulse during the remaining period, which generates a low-level pulse.

For Nth pulse $C_N = A_{N-1} \otimes A_N$ follows table-7 for pulses from C1 to C8.

### Table 7. Condition for the carrier signal.

| Carrier pulse | condition |
|---------------|-----------|
| C1            | A0A1      |
| C2            | A1A2      |
| C3            | A2A3      |
| C4            | A3A4      |
| C5            | A4A5      |
| C6            | A5A6      |
| C7            | A6A7      |
| C8            | A7A8      |

P8 generates $V_{ref} > Cr8$. pulses from A0 to A8 are generated according to the condition given in table 8, for example, to generate A0 the required condition is $|V_{ref}| > 0$ similarly, remaining pulses are generated according to the condition.

### Table 8 A0 to A8 signal condition.
### Table 8: A0 to A8 signal and Condition

| A0 to A8 signal | Condition |
|-----------------|-----------|
| A0              | $|V_{ref}| > 0$ |
| A1              | $|V_{ref}| > 1$ |
| A2              | $|V_{ref}| > 2$ |
| A3              | $|V_{ref}| > 3$ |
| A4              | $|V_{ref}| > 4$ |
| A5              | $|V_{ref}| > 5$ |
| A6              | $|V_{ref}| > 6$ |
| A7              | $|V_{ref}| > 7$ |
| A8              | $|V_{ref}| > 8$ |

#### Figure 8
pulses A0 to A3.

#### 5. Simulation results and discussion

The proposed seventeen-level inverter and its control structure are built in a simulation for which the simulation parameters are given in Table 8 using MATLAB / SIMULINK and tested to verify the operating principle [16-25]. The simulation results with and without LDN are shown in Figure 9, 10, and THD analysis for different input of LDN voltage is displayed in Figure 11, 12, 13. The electrical specifications of the projected inverter are summarized in Table 8. From the simulation result
Comparison between 9L RSMLI and proposed topology (RSC-MLI with LDN configuration) is developed and explained in table 9.

Table 8. Electrical specifications of the proposed inverter.

| Parameter                        | Value          |
|----------------------------------|----------------|
| Dc link voltage for RSMLI        | 50V            |
| Dc link voltage for LDN          | 25V            |
| Switching frequency              | 5000HZ         |
| Modulation index (ma)            | 1              |
| Output RMS voltage               | 141.3v         |
| Load resistance                  | 100ohm         |
| Load current                     | 1.413amp       |
| THD                              | 8.13           |
| The maximum output voltage level | 200V           |

Table 9. Comparison between 9L RSMLI and proposed topology.

| Parameters                          | RSMLI | RSMLI&LDN configuration |
|-------------------------------------|-------|-------------------------|
| No of output voltage Level          | 9     | 17                      |
| Number of switches                  | 12    | 14                      |
| Number of Carrier signals           | 4     | 4                       |
| Number of dc sources                | 4     | 5                       |
| THD                                 | 13.67 | 8.13                    |
| The maximum output voltage level    | 40    | 40                      |
| RMS output voltage                  | 142.8 V | 141.4 V                |

Figure 9. Nine level RSC-MLI with dc-link voltage 25V.
Figure 10. Seventeen level output of proposed RSCMLI+LDN.

Figure 11. FFT analysis for LDN voltage < half of the bridge voltage.

Figure 12. FFT analysis for LDN voltage is half of the bridge voltage.
6. Conclusion
A new multi-level inverter topology with RSC-MLI with LDN is proposed in this paper, a generalized PWM technique is implemented in MATLAB/Simulink software that can be used for any MLI configuration extension with LDN. The proposed MLI has the following advantages—self-regulating function, a simple logic expression for switching operation, and can apply for higher rates with less computational problems, resulting in a reduction in line-voltage harmonics to improve THD efficiency. The proposed reduced carrier PWM system serves as a feasible solution to resolve the demerits of traditional multicarrier, reduced carrier, and multi-reference PWM schemes.

7. References
[1] Grandi G, Rossi C, Ostojic D and Casadei D 2009 A new multilevel conversion structure for grid-connected PV applications IEEE Transactions on Industrial Electronics 56(11)4416-4426
[2] Nabae A, Takahashi I and Akagi, H 1981 A new neutral-point-clamped PWM inverter IEEE Transactions on industry applications 5518-523
[3] Rajababu D, Sudhakar AVV and Sathyavani B 2019 Development of technology for high-power industry converters Int. J.Innov. Technol. Explor. Eng. 8(10)3130-3132
[4] Chinthamalla R, Karampuri R, Jain S, Sanjeevikumar P and Blaabjerg F 2018 Dual solar photovoltaic fed three-phase open-end winding induction motor drive for water pumping system application Electric Power Components and Systems 46(16-17) 1896-1911
[5] Karampuri R, Jain S and Somasekhar V T 2018 Common-mode current elimination PWM strategy along with current ripple reduction for open-winding five-phase induction motor drive IEEE Transactions on Power Electronics 34(7) 6659-6668
[6] Arulmurugan R and Chandramouli A 2019 Modeling of PV powered seven-level inverter for power quality improvement Smart Innov. Syst. Technol. 105113-121
[7] Sun H D, Cha H, Kim H G, Chun T W and Nho E C 2012 Multi-level inverter capable of power factor control with DC link switches Applied Power Electronics Conference and Exposition 1639-1643
[8] Vemuganti H P, Sreenivasarao D and Kumar G S 2017 Improved pulse-width modulation scheme for T-type multilevel inverter IET Power electronics 10(8) 968-976
[9] Sanjeevan AR, Kaarthik RS, Gopakumar K 2016 Reduced common mode voltage operation of a new seven-level hybrid multilevel inverter topology with a single DC voltage source IET Power Electron 9(3) 519-528
[10] Babaei E, Laali Sand Alilu S 2014 Cascaded multilevel inverter with series connection of novel H-bridge basic units IEEE Trans. Ind. Electron. 61(12) 6664-6671
[11] Hinago Y and Koizumi H 2009 A single-phase multilevel inverter using switched series/parallel dc voltage sources IEEE transactions on industrial electronics 57(8) 2643-2650
[12] Kassakian J G 1982 A new current mode sine wave inverter IEEE Transactions on Industry Applications 3 273-278
[13] Mudi J, Shiva C K, Vedik B and Mukherjee V 2020 Frequency stabilization of solar thermal-photovoltaic hybrid renewable power generation using energy storage devices Iranian Journal of Science and Technology, Transactions of Electrical Engineering 1-21https://doi.org/10.1007/s40998-020-00374-w
[14] Arulmurugan R 2018 Photovoltaic powered transformerless hybrid converter with active filter for harmonic and reactive power compensation ECTI Transactions on Electrical Engineering, Electronics, and Communications 16(2) 44-51
[15] Vedik B, Shiva C K and Harish P 2020 Reverse harmonic load flow analysis using an evolutionary technique SN Appl. Sci. 2, 1584 https://doi.org/10.1007/s42452-020-03408-4
[16] Vedik B, Ritesh K, Deshmukh R and Shiva C K 2020 Renewable energy based load frequency stabilization of interconnected power systems using quasi-oppositional dragonfly algorithm J Control AutomElectr Syst. https://doi.org/10.1007/s40313-020-00643-3
[17] Vedik B, Naveen P and Shiva C K 2020 A novel disruption based symbiotic organisms search to solve economic dispatch Evol. Intel. https://doi.org/10.1007/s12065-020-00506-5
[18] Kumar R, Sahu B, Shiva C K and Rajender B 2020 A control topology for frequency regulation capability in a grid integrated PV system Archives of Electrical Engineering 69(2)389–401
[19] Basetti V, Chandel A K and Subramanyam K B 2018 Power system static state estimation using JADE-adaptive differential evolution technique Soft Computing 22(21) 7157-76https://doi.org/10.1007/s00500-017-2715-3
[20] Shiva C K, Vedik B and Kumar R 2019 Integration of distributed power sources to hydro-hydro power system subjected to load frequency stabilization International Journal of Engineering and Advanced Technology 8(2) 128-32
[21] Pasha SN, Harshavadhan A, Ramesh D and Md S Shabana 2019 Variation analysis of artificial intelligence machine learning and advantages of deep architectures International Journal of Advanced Science and Technology 28(17) 488-495
[22] Swathi N, Padmaja Ch and Navya Jyothi G 2020 Audio assistive for blind people to identify the cloth patterns and colors Journal of Critical Reviews 7(17) 154-158 10.31838/jcr.07.17.23
[23] Prakash TC, Mamatha M and Samala S 2020 An IoT based under weather monitoring system Journal of Critical Reviews 7(17) 148-153 10.31838/jcr.07.17.22
[24] Kumar CN and Satyanarayana N 2015 Hybrid loss recovery technique for multipath load balancing in MANETs 2nd International Conference on Electronics and Communication Systems ICECS 2015 1294-1301 10.1109/ECS.2015.7124793
[25] Sekhar VM Rao, KVG Rao NS and Chand MG 2016 Comparing the capacity NCC and fidelity of various quantization intervals on DWT Advances in Intelligent Systems and Computing 413 45-55 10.1007/978-981-10-0419-3_6