A Four-Phase High Voltage Conversion Ratio Bidirectional DC-DC Converter for Battery Applications

Li-Kun Xue, Ping Wang, Yi-Feng Wang *, Tai-Zhou Bei and Hai-Yun Yan

School of Electrical Engineering and Automation, Tianjin University, Tianjin 300072, China; E-Mails: xuelikun@tju.edu.cn (L.-K.X.); pwang@tju.edu.cn (P.W.); 396913440@163.com (T.-Z.B.); zhangyanyj@126.com (H.-Y.Y.)

* Author to whom correspondence should be addressed; E-Mail: wayif@tju.edu.cn; Tel.: +86-185-2206-2559; Fax: +86-22-2740-1479.

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Abstract: This study presents a four-phase interleaved high voltage conversion ratio bidirectional DC-DC converter circuit based on coupled inductors and switched capacitors, which can eliminate the defects of conventional high voltage conversion ratio bidirectional DC-DC converters in terms of high-voltage/current stress, less efficiency and low-power limitation. Parallel channels are used to reduce current stress at the low-voltage side and series connected switched capacitors are used to enlarge voltage conversion ratio, reduce voltage stress and achieve auto current sharing. This paper proposes the operation principle, feature analysis and optimization design considerations. On this basis the objectives of high voltage conversion ratio, low voltage/current stress, high power density, high efficiency and high-power applications can be achieved. Some experimental results based on a 500 W prototype converter (24 V to 48 V at low-voltage side, 400 V at high-voltage side) are given to verify the theoretical analysis and the effectiveness of the proposed converter.

Keywords: battery; bidirectional DC-DC converter; high conversion ratio; interleaved; switched capacitor; coupled inductor
1. Introduction

Recently, the development of distributed renewable energy generation systems has become a foremost topic to save the fossil fuel consumption and protect the natural environment [1–3]. Energy storage elements (ESEs) are adopted to smooth and stabilize the output power and improve the dynamic response of the system. The bidirectional DC-DC converter (BDC) links the ESEs to the DC voltage bus. Unfortunately, the DC bus voltage could be as high as 800 V when the system includes three phase PWM inverters for high-power applications [3,4]. As the most developed and widely used energy storage devices [5,6], the battery energy storage system typically includes numerous low-voltage battery cells. Although a storage battery series string can provide high enough voltage, slight mismatches or temperature differences will cause a charge imbalance when the series string is charged as a unit [7]. Batteries arranged in parallel strings can enhance the power redundancy and alleviate the problems caused by storage battery series strings [8,9]. However, the output voltage still remains low (24 V–48 V) in this parallel connected configuration, thus an efficient BDC with high voltage conversion ratio (HVCR) is required [9].

Dual-active-bridge isolated bidirectional DC-DC converters (DAB-IBDCs) based on high frequency transformers are the most common topologies for conventional HVCR BDCs [10–12]. HVCR can be achieved by adjusting the transformer turns ratio. However, those topologies have some drawbacks such as: High voltage spike on the main switch devices, low efficiency due to the leakage-inductor, and only suitable for low-power applications. As shown in Figure 1, some isolated and bidirectional soft switching techniques are generally applied to improve conversion efficiency [13–15], such as LLC or CLLC resonant converter, full-bridge phase-shift converter and so on [16–18]. Unfortunately, those resonant topologies will increase circuit complexity, and usually need complex-structured transformers [19].

Many applications of HVCR BDCs do not require isolation [20], and non-isolated BDCs (NIBDCs) with HVCR have attracted much attention in order to simplify structure design, lower the cost and improve conversion efficiency.

To avoid the huge current spike, as shown in Figure 2, a category of SC-based resonant converters are proposed [21,22]. By adding a small series resonant inductor, the di/dt slew rate is efficiently suppressed, and high voltage ratio and zero-current switching (ZCS) can be achieved, but these topologies are only suitable for low-power applications due to the excessive input ripple current and too many components.
On the other hand, as shown in Figure 3, CI-BDCs are widely used in order to achieve HVCR with fewer components and reduce voltage stress at the same time [23,24]. Leakage inductance energy can alleviate the reverse-recovery problem of the rectifier diode. Furthermore, active clamp circuit or the passive counterpart is necessary to alleviate the turn-off voltage spike and achieve zero voltage switching (ZVS) even zero current switching (ZCS) of the switches [24,25]. In these converters, the voltage ratio can be easily extended by increasing the winding-ratio of the coupled-inductors. However, the current ripple at low voltage side (LVS) is also largely increased, which constrain their high-power applications.

To minimize the current ripple at LVS and extend power conversion ability, SC-BDCs and CI-BDCs based on interleaved structures are presented [26–29]. [19] and [26] present a multiphase quasi-resonant (QR) ZCS SC-BDC structure, and in [27], another ZCS SC-BDC topology is studied, these topologies extend the voltage conversion ratio (VCR) by adding an increased number of SCs and switches with a series connected resonant inductor to obtain voltage conversion ratios from the 2-ratio or 1/2 ratio to n-ratio or 1/n ratio, and enlarge the power conversion ability by adding interleaved cells, but there are too many switches and other power devices, system efficiency becomes low, converter structure becomes too complex and the controller will be overburdened. As shown in Figure 4, to reduce the number of the power devices, a ZVS BDC topology is proposed in [28]. However, the VCR of the ZVS BDC is still less than six, and phase-shift control goes against the topology extension.
Based on the above analysis, the NIBDC with HVCR and high efficiency that can be applied to high-power level has rarely been proposed. A novel 4-phase interleaved NIBDC with SCs and CIs is proposed in this work. The proposed BDC is optimized to further improve converter efficiency and power density, reduce device voltage and current stress, and increase VCR. Eight MOSFETs, two CIs, three SCs and no diode are used to achieve 4 times VCR \((4/(1-D))\) or \(D/4\), where \(D\) is the turn-on duty cycle of switch) compared to conventional Buck/Boost BDC. The key point about the proposed converter is how to reduce the current stress on LVS, voltage stress for all switches, and achieve high efficiency when the circuit operates under HVCR. A 4-phase parallel structure easily facilitates current stress and current ripple reduction. Moreover, auto current sharing (ACS) of parallel 4 channels can be obtained by the effect of SCs. Furthermore, CIs are used to guarantee very low current ripple when the inductance is small, thus fewer winding turns reduce the size, cost and power losses of the CIs. This paper is organized as follows: the operation principles and feature analyses are described in Sections 2 and 3 respectively. Section 4 presents the circuit features and the design considerations, and Section 5 presents the experimental results for a 24 V–48 V LVS, 400 V high voltage side (HVS) and 500 W power output with 200 kHz switching frequency to validate the effectiveness of the proposed topology. Finally, conclusions are given in Section 6.

2. Coupling Mode Selection

Figure 5 shows the two different coupling patterns of the coupled inductor, and also their equivalent decoupling models [30]. As shown in Figure 5a, the direct coupling inductor with initial inductance \(L_1, L_2\) can be modeled as one positive mutual inductance \(M\) at the common node, and two separate leakage inductors with inductance \(L_1 - M\) and \(L_2 - M\), where \(M = kL\). Correspondingly, the inverse coupling counterpart can be modeled as one negative mutual inductance \(-M\) at the common node, and two separate leakage inductors with inductance \(L_1 + M\) and \(L_2 + M\) as shown in Figure 5b. The voltages \(v_{L1}, v_{L2}\) across \(L_1, L_2\) now equal the summation of the voltage across mutual inductance and the leakage inductance.
In order to investigate how the CIs influence the channel inductor ripple and the dynamic processing, typical operation waveforms of two-phase interleaved continuous current mode (CCM) Boost (TPICB) are shown in Figure 6.

Figure 6a displays the current waveforms in inverse coupling mode, the dotted line represents the current waveforms of $i_{L1}$, $i_{L2}$ without coupling. Compared with the uncoupled counterpart, the current rising slope of $i_{L2}$ in phase $b$-$c$ is slower, due to the effect of the CI. At interval $T_1$ and $T_3$, the rising slope of the coupled inductors is greater. However, in TPICB circuits, the overlap time that the corresponding switches both on is short, so the total effect of the CI is to reduce the inductor current ripple. Moreover, in transient response phase, when output power increases, the ON time of switches will be increased and $T_1$, $T_3$ last longer, which will lead to fast dynamic response. This is another advantage by choosing the inverse coupling mode. Correspondingly, the current waveforms with direct coupling condition are shown in Figure 6b. The channel inductor ripple will be enlarged. Although above conclusions are obtained when $D > 0.5$, the same conclusion can be obtained when $D < 0.5$:  

**Figure 5.** Two different coupling patterns (a) Direct coupling; (b) Inverse coupling.

**Figure 6.** Current curves when duty cycle is larger than 0.5 (a) Inverse coupling, (b) Direct coupling.
\[
\begin{align*}
\begin{cases}
 v_{L1} = v_{L1-M} + v_M \\
v_{L2} = v_{L2-M} + v_M
\end{cases}
\quad \text{and} \quad
\begin{cases}
 v_{L1} = v_{L1-M} + v_{-M} \\
v_{L2} = v_{L2-M} + v_{-M}
\end{cases}
\end{align*}
\]

(1)

For quantitative analysis, taking inverse coupling for example, some expressions will be given [30].

During phase \(T_1\), MOSFETs of channel 1 and 2 are turned on, voltages across \(L_1, L_2\) are \(v_{L1} = v_{L2} = V_L\), therefore, the equivalent inductances for channel 1 and channel 2 are obtained:

\[
\begin{align*}
V_L &= (L_i + M) \cdot \frac{di_{i1}}{dt} - M \cdot (i_{i1} + i_{i2})/dt \\
V_L &= (L_i + M) \cdot \frac{di_{i2}}{dt} - M \cdot (i_{i1} + i_{i2})/dt
\end{align*}
\]

(2)

\[
L_{T-EQ1A} = L - M
\]

(3)

\[
L_{T-EQ2A} = L - M
\]

(4)

During \(T_2\) period, MOSFET of channel 1 is turned off, and MOSFET of channel 2 is turned on. Voltages across \(L_1, L_2\) are \(v_{L1} = V_L - V_H, v_{L2} = V_L\). Therefore, the equivalent inductance for channel 1 and channel 2 are calculated as:

\[
L_{T-EQ1B} = \frac{L^2 - M^2}{L - 1} \cdot \frac{1}{D} M
\]

(5)

\[
L_{T-EQ2B} = \frac{L^2 - M^2}{L - D} \cdot \frac{1}{D} M
\]

(6)

During \(T_3\) period, MOSFETs of channel 1 and 2 are turned on. It’s the same as in time interval \(T_1\).

During \(T_4\) period, MOSFET of channel 1 is turned on, and MOSFET of channel 2 is turned off. It’s symmetry of the situation during \(T_2\):

\[
L_{T-EQ1D} = \frac{L^2 - M^2}{L - D} \cdot \frac{1}{D} M
\]

(7)

\[
L_{T-EQ2D} = \frac{L^2 - M^2}{L - 1} \cdot \frac{1}{D} M
\]

(8)

Based on above analyses, to decrease the current ripple of low voltage input side, accelerate the auto current sharing process of switch capacitors, inverse coupling mode is selected in this paper.

3. Proposed Topologies and Operation Principles

3.1. Proposed Topologies

Figure 7 shows the proposed HVCR BDC circuit after inductor decoupling. There are four parallel inductors at \(V_i\) side, to reduce inductance and mitigate channel ripple current effectively, phases 1 and 2, as well as phases 3 and 4, share an inverse coupled inductor with a turn ratio of \(N_p:N_s = 1:1\). The coupling coefficient is denoted by \(k \ (0 < k < 1)\). In addition, there are three SCs connected in series in the circuit, SCs named \(C_1, C_2\) and \(C_3\) are used in the circuit to realize HVCR, furthermore, with attendance of the SCs, the channel inductors can achieve auto current sharing (ACS) feature.
The PWM drive signal of the proposed circuit is very simple. Phases 1 and 3, as well as phases 2 and 4, share the same gate PWM signal. When the circuit works in Boost stage, energy flows from $V_L$ to $V_H$; the duty cycle $D_{up}$ of gate drive signals for $S_1$, $S_2$, $S_3$ and $S_4$ should be larger than 0.5 in order to eliminate circulating current during the turn-off of all ground-connected MOSFETs; and $Q_1$, $Q_2$, $Q_3$ and $Q_4$ are working in synchronous rectification (SR) mode during this time. Correspondingly, when the circuit works in Buck stage, energy flows from $V_H$ to $V_L$; the duty cycle $D_{down}$ of PWM for $Q_1$, $Q_2$, $Q_3$ and $Q_4$ should be less than 0.5; and $S_1$, $S_2$, $S_3$ and $S_4$ are working in SR mode during this period.

**Figure 7.** Schematic of the proposed four-phase HVCR BDC.

During the following theoretical analyses and calculation process, the component parameters are regarded as identical, and the following three conditions are assumed:

1. All switches are treated as ideal.
2. $L_1 = L_2 = L_3 = L_4 = L$ and $C_1 = C_2 = C_3 = C$.
3. Capacitors $C_1$, $C_2$ and $C_3$ are large enough that $V_{C1}$, $V_{C2}$ and $V_{C3}$ are considered to be constant in a switching period.
4. The coupling coefficient $k$ and the mutual inductance $M$ of the CIs are equal, $k = M/L$, and the turn ratio of the CIs is equal to 1.

### 3.2. CCM Boost Stage

Figure 8 shows the major operating waveforms of the proposed HVCR BDC in CCM Boost stage. Figure 9 shows the equivalent circuits. In this mode, LVS energy flows from $V_L$ to $V_H$. Switches $S_1$, $S_2$, $S_3$ and $S_4$ are operating in active switching with duty cycles of $D_{up}$ and switches $Q_1$, $Q_2$, $Q_3$ and $Q_4$ are operated in SR mode, as shown in Figure 8. The operation of the CCM Boost stage can be divided into four intervals.
Figure 8. Operating waveforms for the CCM Boost stage.

Figure 9. Equivalent circuits in CCM Boost stage (a) interval 1; (b) interval 2; (c) interval 3; (d) interval 4.

Interval 1 \([t_0 \sim t_1]\): Power switches \(S_1, S_3\) are on, and \(S_2, S_4\) turn off. Inductor \(L_1\) are charged by \(V_L\), and inductor current \(i_{L1}\) goes up linearly. Inductor \(L_2\) is series-connected with \(C_1\) to charge capacitor \(C_2\), with inductor current \(i_{L2}\) going down linearly. Inductor \(L_3\) is charged by \(V_L\), and inductor current \(i_{L3}\) goes
up linearly. Inductors $L_4$ and $C_3$ are series-connected to charge capacitor $C_H$ and the load, and inductor current $i_{L4}$ goes down linearly. The voltage equations across inductors are obtained:

\[
\begin{align*}
V_L &= L_1 \cdot di_{L1}/dt - M \cdot di_{L2}/dt \\
V_L + V_{C1} - V_{C2} &= L_2 \cdot di_{L2}/dt - M \cdot di_{L1}/dt \\
V_L &= L_3 \cdot di_{L3}/dt - M \cdot di_{L4}/dt \\
V_L + V_{C3} - V_H &= L_4 \cdot di_{L4}/dt - M \cdot di_{L3}/dt
\end{align*}
\] (9)

\[
\begin{align*}
\frac{di_{L1}}{dt} &= LV_L + M(V_L + V_{C1} - V_{C2}) \\
\frac{di_{L3}}{dt} &= LV_L + M(V_L + V_{C3} - V_H)
\end{align*}
\] (10)

**Interval 2 [$t_1 \sim t_2$]:** Power switches $S_1$, $S_2$, $S_3$ and $S_4$ are turned on, and the corresponding SR switches $Q_1$, $Q_2$, $Q_3$ and $Q_4$ are turned off. Inductors $L_1$, $L_2$, $L_3$ and $L_4$ are charged by $V_L$. Inductor currents $i_{L1}$, $i_{L2}$, $i_{L3}$ and $i_{L4}$ go up linearly. The load absorbs energy from $C_H$. The voltage relationship of each inductor can be written as follows:

\[
\begin{align*}
V_L &= L_1 \cdot di_{L1}/dt - M \cdot di_{L2}/dt \\
V_L &= L_2 \cdot di_{L2}/dt - M \cdot di_{L1}/dt \\
V_L &= L_3 \cdot di_{L3}/dt - M \cdot di_{L4}/dt \\
V_L &= L_4 \cdot di_{L4}/dt - M \cdot di_{L3}/dt \\
\frac{di_{L1}}{dt} &= \frac{di_{L3}}{dt} = \frac{V_L}{L - M}
\end{align*}
\] (11)

**Interval 3 [$t_2 \sim t_3$]:** Switches $S_1$, $S_3$ and $Q_2$, $Q_4$ are turned off, switches $S_2$, $S_4$ and $Q_1$, $Q_1$ are turned on. Inductor $L_2$ release energy to $C_1$ through $Q_1$, with inductor current $i_{L1}$ going down linearly. Inductor $L_3$ is charged through $V_L$, $S_2$ path, and inductor current $i_{L2}$ goes up in a linear way. Similarly, series-connected $L_3$, $V_L$, and $C_2$ charge energy to $C_3$ through $Q_3$. Current $i_{L3}$ goes down in a linear way. Inductors $L_4$ are linearly charged by $V_L$. The load is charged by $C_H$. The voltage equations across inductors $L_1$, $L_2$, $L_3$ and $L_4$ are listed as following:

\[
\begin{align*}
V_L - V_{C1} &= L_1 \cdot di_{L1}/dt - M \cdot di_{L2}/dt \\
V_L &= L_2 \cdot di_{L2}/dt - M \cdot di_{L1}/dt \\
V_L + V_{C2} - V_{C3} &= L_3 \cdot di_{L3}/dt - M \cdot di_{L4}/dt \\
V_L &= L_4 \cdot di_{L4}/dt - M \cdot di_{L3}/dt \\
\frac{di_{L1}}{dt} &= \frac{(V_L - V_{C1})L + MV_L}{L^2 - M^2} \\
\frac{di_{L3}}{dt} &= \frac{(V_L + V_{C2} - V_{C3})L + MV_L}{L^2 - M^2}
\end{align*}
\] (13)

**Interval 4 [$t_3 \sim t_4$]:** As the state of mode 2, $S_1$, $S_2$, $S_3$ and $S_4$ are all turned on, and $Q_1$, $Q_2$, $Q_3$ and $Q_4$ are switched off. Inductors $L_1$, $L_2$, $L_3$ and $L_4$ are all linearly charged by $V_L$. 


3.3. CCM Buck Stage

Figures 10 and 11 show the key waveforms and equivalent circuits in the CCM Buck stage, respectively.

![Operating waveforms for the CCM Buck stage.](image)

**Figure 10.** Operating waveforms for the CCM Buck stage.

![Equivalent circuits in CCM Buck stage.](image)

**Figure 11.** Equivalent circuits in CCM Buck stage (a) interval 1; (b) interval 2; (c) interval 3; (d) interval 4.
In this mode, HVS energy flows from $V_H$ to $V_L$. Switches $Q_1$, $Q_2$, $Q_3$ and $Q_4$ are operating in active switching with duty cycles of $D_{down}$ and switches $S_1$, $S_2$, $S_3$ and $S_4$ are conducting in SR mode, as shown in Figure 10. The operation of the CCM Buck stage can be divided into four intervals.

**Interval 1 [$t_0 \sim t_1$]:** The switches $Q_2$, $Q_4$ and $S_1$, $S_3$ are turned on, while switches $Q_1$, $Q_3$ and $S_2$, $S_4$ are turned off. The inductor $L_4$ and capacitor $C_3$ are linearly charged by $V_H$ through $Q_4$, $C_3$, $L_4$ and $V_L$. Inductor current $i_{L4}$ goes up linearly. The series-connected $L_2$ and $C_1$ are charged by $C_2$, with linearly increasing inductor current $i_{L2}$. Inductors $L_3$, $L_1$ linearly discharge energy to $V_L$ through $S_3$ and $S_1$ respectively. The voltage equations across each inductor are written as follows:

$$
\begin{align*}
-V_L &= L_4 \cdot \frac{di_{L4}}{dt} - M \cdot \frac{di_{L2}}{dt} \\
V_{C2} - V_L - V_{C1} &= L_2 \cdot \frac{di_{L2}}{dt} - M \cdot \frac{di_{L1}}{dt} \\
-V_L &= L_3 \cdot \frac{di_{L3}}{dt} - M \cdot \frac{di_{L4}}{dt} \\
V_H - V_L - V_{C3} &= L_4 \cdot \frac{di_{L4}}{dt} - M \cdot \frac{di_{L3}}{dt}
\end{align*}
$$

(15)

**Interval 2 [$t_1 \sim t_2$]:** The power switches $Q_1$, $Q_2$, $Q_3$ and $Q_4$ are turned off, and $S_1$, $S_2$, $S_3$ and $S_4$ are turned on to reduce conductive losses. In this time period, the inductors $L_1$, $L_2$, $L_3$ and $L_4$ release energy to $V_L$ through $S_3$ and $S_1$ respectively. The voltage of SCs stay the same, with no current flowing ($i_{C1} = i_{C2} = i_{C3} = 0$). Therefore, the following relationships are derived:

$$
\begin{align*}
-V_L &= L_1 \cdot \frac{di_{L1}}{dt} - M \cdot \frac{di_{L2}}{dt} \\
-V_L &= L_2 \cdot \frac{di_{L2}}{dt} - M \cdot \frac{di_{L1}}{dt} \\
-V_L &= L_3 \cdot \frac{di_{L3}}{dt} - M \cdot \frac{di_{L4}}{dt} \\
-V_L &= L_4 \cdot \frac{di_{L4}}{dt} - M \cdot \frac{di_{L3}}{dt}
\end{align*}
$$

(16)

**Interval 3 [$t_2 \sim t_3$]:** The power switches $Q_1$, $Q_3$ and $S_2$, $S_4$ are turned on, while $Q_2$, $Q_4$ and $S_1$, $S_3$ are turned off. Inductor $L_1$ is linearly charged by $C_1$ with linearly increasing current $i_{L1}$. Inductor $L_2$ releases energy to $V_L$ with linearly decreasing $i_{L2}$. Similarly, inductor $L_3$ and capacitor $C_2$ are charged by $C_3$ through $Q_3$. Inductor current $i_{L3}$ goes up linearly. At the same time, inductor $L_4$ discharges energy to $V_L$ through switch $S_4$. Inductor current $i_{L4}$ goes up linearly. The $V_L$ is charged by the summation of inductor currents $i_{L1}$, $i_{L2}$, $i_{L3}$, $i_{L4}$. The voltage equations across each inductor are written as follows:

$$
\begin{align*}
V_{C1} - V_L &= L_1 \cdot \frac{di_{L1}}{dt} - M \cdot \frac{di_{L2}}{dt} \\
-V_L &= L_2 \cdot \frac{di_{L2}}{dt} - M \cdot \frac{di_{L1}}{dt} \\
V_{C2} - V_L - V_{C1} &= L_3 \cdot \frac{di_{L3}}{dt} - M \cdot \frac{di_{L4}}{dt} \\
-V_L &= L_4 \cdot \frac{di_{L4}}{dt} - M \cdot \frac{di_{L3}}{dt}
\end{align*}
$$

(17)

**Interval 4 [$t_3 \sim t_4$]:** It’s the same as Interval 2. The power switches $Q_1$, $Q_2$, $Q_3$ and $Q_4$ are turned off, and $S_1$, $S_2$, $S_3$ and $S_4$ are turned on to reduce conductive losses. In this time period, the inductors all release energy to $V_L$ through the corresponding current paths as shown in Figure 11d. Meanwhile, the voltage of switched-capacitors remain unchanged, $i_{C1} = i_{C2} = i_{C3} = 0$. 
3.4. Discontinuous Current Mode (DCM) Boost Stage

Figure 12 shows the major operating waveforms of the proposed HVCR BDC in DCM Boost stage. In this mode, relative faint energy flows from \( V_L \) to \( V_H \). Switches \( S_1, S_2, S_3 \) and \( S_4 \) are conducting in active switching with duty cycles of \( D_{up} \) and switches \( Q_1, Q_2, Q_3 \) and \( Q_4 \) are operating in SR mode, as shown in Figure 12. The operation of the DCM Boost stage can be divided into six intervals.

**Interval 1 \([t_0 \sim t_1]\):** The same as interval 1 in CCM Boost mode: \( S_1, S_3 \) are on, and \( S_2, S_4 \) turn off. Inductor \( L_1 \) is charged by \( V_L \), and inductor current \( i_{L1} \) goes up linearly. Inductor \( L_2 \) is series-connected with \( C_1 \) to charge capacitor \( C_2 \), and inductor current \( i_{L2} \) goes down linearly. Inductor \( L_3 \) is charged by \( V_L \), and inductor current \( i_{L3} \) goes up linearly. Inductor \( L_4 \) and \( C_3 \) are series-connected to charge capacitor \( C_H \) and the load, and inductor current \( i_{L4} \) goes down linearly.

**Interval 2 \([t_1 \sim t_2]\):** The state of \( S_1 \) and \( S_3 \) are unchanged, but \( Q_2 \) and \( Q_4 \) are turned off. \( L_1, L_3 \) are charged by \( V_L \), with \( i_{L1}, i_{L3} \) increasing linearly. Unlike interval 1, the current of \( C_2 \) is zero, the output parasitic capacitors of \( S_2 \) and \( S_4 \) are resonant with channel inductors respectively. \( i_{L2}, i_{L4} \) will increase firstly and then decrease positively, and their peak values are related with the value of output parasitic capacitances. When \( i_{L2} \) and \( i_{L4} \) reach zero, ZVS turn-on of \( S_2 \) and \( S_4 \) can be achieved at this time, and if \( S_2 \) and \( S_4 \) still not be turned on, \( i_{L2} \) and \( i_{L4} \) will begin the oscillation of positive phase.

**Interval 3 \([t_2 \sim t_3]\):** The same as interval 2 in CCM Boost mode, power switches \( S_1, S_2, S_3 \) and \( S_4 \) are turned on, and \( Q_1, Q_2, Q_3 \) and \( Q_4 \) are turned off. Inductors \( L_1, L_2, L_3 \) and \( L_4 \) are charged by \( V_L \). Inductor currents \( i_{L1}, i_{L2}, i_{L3} \) and \( i_{L4} \) go up linearly. The load absorbs energy from \( C_H \).

**Interval 4 \([t_3 \sim t_4]\):** The same as interval 3 in CCM Boost mode, switches \( S_1, S_3 \) and \( Q_2, Q_4 \) are turned off, while switches \( S_2, S_4 \) and \( Q_1, Q_3 \) are turned on. Inductor \( L_1 \) releases energy to \( C_1 \) through \( Q_1 \), and inductor current \( i_{L1} \) goes down linearly. Inductor \( L_2 \) is charged through \( V_L, S_2 \) path, and inductor current \( i_{L2} \) goes up in a linear way. Similarly, series-connected \( L_3, V_L \) and \( C_2 \) charge energy to \( C_3 \) through \( Q_3 \). Current \( i_{L3} \) goes down in a linear way. Inductor \( L_4 \) is linearly charged by \( V_L \). The load is charged by \( C_H \).
Interval 5 \([t_4 \sim t_5]\): This interval is the continuation of interval 4. Switches \(S_1, S_3\) and \(Q_2, Q_4\) are turned off, switches \(S_2, S_4\) are turned on when \(i_{L2}\) and \(i_{L4}\) decrease to zero. During this interval, \(i_{L2}, i_{L4}\) increase linearly. Similar to interval 2, the current of \(C_1\) and \(C_3\) is zero, and the output parasitic capacitors of \(S_1\) and \(S_3\) are resonant with channel inductors respectively. \(i_{L1}, i_{L3}\) will increase firstly and then decrease positively, and their peak values are related to the value of output parasitic capacitances of selected MOSFETs. When \(i_{L1}\) and \(i_{L3}\) reach zero, ZVS turn-on of \(S_1\) and \(S_3\) can be achieved at this time, and if \(S_1\) and \(S_3\) still not be turned on, \(i_{L1}\) and \(i_{L3}\) will begin the oscillation of positive phase.

Interval 6 \([t_5 \sim t_6]\): As the state of interval 3, \(S_1, S_2, S_3\) and \(S_4\) are all turned on, and \(Q_1, Q_2, Q_3\) and \(Q_4\) are switched off. Inductors \(L_1, L_2, L_3\) and \(L_4\) are all linearly charged by \(V_I\).

Based on the above analyses, it can be seen that, channel inductor will resonant with the output parasitic capacitor of the corresponding MOSFET in DCM mode, which will lead to negative oscillation of the inductor current other than constant zero. Moreover, the negative oscillation peak is determined by the value of output parasitic capacitor for the selected MOSFET. In this paper, silicon carbide (SiC) MOSFETs are selected due to their very tiny output parasitic capacitor. Furthermore, ZVS turn-on of the relevant MOSFET can be achieved in turning on the switch during the negative oscillation of the inductor current, which will improve the circuit light-load efficiency further.

4. Feature Analysis and Design Considerations

4.1. Voltage Gain and Duty Ratio

By adopting energy conservation method for \(L_1\), the following express can be obtained:

\[
\Delta E = L_1 \cdot i_{L1}^2(t_4) / 2 - L_1 \cdot i_{L1}^2(t_0) / 2 = 0
\]

(18)

This indicates the total inductor current increment is zero in a switching period, as in Equation (19), with the time periods of each mode listed in Equation (20):

\[
\begin{align*}
\int_{t_{MODE1}}^t di_{L1} + 2\int_{t_{MODE2}}^t di_{L1} + \int_{t_{MODE3}}^t di_{L1} &= 0 \\
\int_{t_{MODE1}}^t di_{L3} + 2\int_{t_{MODE2}}^t di_{L3} + \int_{t_{MODE3}}^t di_{L3} &= 0
\end{align*}
\]

(19)

\[
\begin{align*}
T_{MODE1} &= T_{MODE3} = (1 - D_{up})T_s \\
T_{MODE2} &= T_{MODE4} = (D_{up} - 1/2)T_s
\end{align*}
\]

(20)

where \(t_{MODE1}, t_{MODE2}, t_{MODE3}\) and \(t_{MODE4}\) are the duration time of each corresponding mode.

Substitute Equations (10), (12) and (14) in (19), following equations are therefore deduced:

\[
\begin{align*}
L \cdot [V_L - (1 - D_{up})V_{C1}] + M \cdot [V_L + (1 - D_{up})(V_{C1} - V_{C2})] &= 0 \\
L \cdot [V_L + (1 - D_{up})(V_{C2} - V_{C3})] + M \cdot [V_L + (1 - D_{up})(V_{C3} - V_{H})] &= 0
\end{align*}
\]

(21)

Due to the effect of voltage doubling cells based on SCs, \(V_H = 4V_{C3}/3 = 4V_{C2}/2 = 4V_{C1}/1\). Then solving Equation (21), we get:
\[
\begin{align*}
V_L - (1 - D_{up})V_{C1} &= 0 \\
V_L + (1 - D_{up})(V_{C1} - V_{C2}) &= 0 \\
V_L + (1 - D_{up})(V_{C2} - V_{C3}) &= 0 \\
V_L + (1 - D_{up})(V_{C3} - V_H) &= 0
\end{align*}
\]  
(22)

In consequence, voltage gain for the proposed 4-phase BDC topology in CCM Boost stage can be obtained:

\[
M_H = \frac{V_H}{V_L} = \frac{4}{(1 - D_{up})}
\]  
(23)

Similarly, the voltage gain in CCM Buck stage is deduced as:

\[
M_L = \frac{V_L}{V_H} = \frac{D_{down}}{4}
\]  
(24)

The relationship between the voltage ratio and duty ratio of the proposed 4-phase BDC is sketched in Figure 13.

**Figure 13.** Duty cycles *versus* voltage gain (a) CCM Boost operation; (b) CCM Buck operation.

1. The voltage ratio of the proposed BDC is extended significantly, with duty cycle $D$ varies from 0.5 to 0.9 ($D_{up}$) or 0.1 to 0.5 ($D_{down}$), the voltage ratio can achieve 8 - 40 in CCM Boost operation, and 0.025 - 0.125 in CCM Buck operation.

2. Within the whole working scope, the voltage gain varies evenly when the duty cycle is changing, which is conductive to the design of the closed-loop digital controller.

### 4.2. Auto Current Sharing

As mentioned above, due to the effects of the series SCs between the four channels, the ACS mechanism of the proposed BDCs is different from traditional parallel circuits. In theory, for static current sharing, even with different inductor values, the proposed BDCs can achieve ACS, if the same duty cycle of each channel MOSFET is fulfilled. Based on Figure 8 and above analysis, a case study of CCM Boost stage will be given. The current expressions for SCs can be obtained as:
\begin{align}
\begin{cases}
 i_{C1} = (1 - S_1 \cdot S_3) \cdot i_{L1} - (1 - S_2 \cdot S_4) \cdot i_{L2} \\
 i_{C2} = (1 - S_2 \cdot S_4) \cdot i_{L2} - (1 - S_1 \cdot S_3) \cdot i_{L3} \\
 i_{C3} = (1 - S_1 \cdot S_3) \cdot i_{L3} - (1 - S_2 \cdot S_4) \cdot i_{L4}
\end{cases}
\end{align}
\tag{25}

where $S_1$, $S_2$, $S_3$ and $S_4$ = “0” or “1” are the switching state of the corresponding power switches. The Ampere-second balance equation can be expressed as follows:
\begin{align}
\begin{cases}
 -I_{L2}(t_1 - t_0) + I_{L1}(t_3 - t_2) = 0 \\
 I_{L2}(t_1 - t_0) - I_{L3}(t_3 - t_2) = 0 \\
 -I_{L4}(t_1 - t_0) + I_{L3}(t_3 - t_2) = 0
\end{cases}
\end{align}
\tag{26}

where $I_{L1}$, $I_{L2}$, $I_{L3}$ and $I_{L4}$ represent the mean value of corresponding inductor current during time interval $[t_2, t_3]$ or $[t_0, t_1]$. The time-period of $t_3 - t_2$ equals to $t_1 - t_0$ when $S_1$, $S_2$, $S_3$ and $S_4$ with the same duty cycle $D_{up}$, and therefore $I_{L2} = I_{L1}$ is obtained. In the same way, $I_{L2} = I_{L3}$, $I_{L3} = I_{L4}$ are derived. Based on above analysis, ACS among each inductor can be achieved if the switches $S_1$, $S_2$, $S_3$ and $S_4$ share the same turn-on duty cycle.

Capability of ACS is a significant advantage for the proposed 4-phase BDC, which can simplify the design of CIs and the digital controller. Unfortunately, the regulation process of ACS leads to current pulsation, and even instability of the whole system. To solve this negative effect, a sufficiently small inductance value and a relatively large SC value should be selected based on the above optimization methods. A small inductance is used to shorten the ACS process, and a large SC is used to minimize the voltage fluctuation between SC and input/output capacitors. Besides, a careful designed digital control loop is used to guarantee the stability of the proposed BDC, as shown in Figure 14. With the control loop compensation, low-frequency gain is enlarged, several resonant peaks caused by SCs are weakened, and the cut off frequency of the current loop is decreased to 35.8 kHz and the system is stable with good phase margin (PM) and gain margin (GM).

\begin{figure}
\centering
\includegraphics[width=\textwidth]{Bode_diagram.png}
\caption{Bode diagram with and without the loop compensation.}
\end{figure}
4.3. Design Considerations

4.3.1. Optimal Design of the CIs

In this section, the following analyses are mainly aim to optimize the coupling coefficient of the CIs to minimize inductor current ripple on the premise that the inductance and inductor volume are small enough. Under uncoupled mode, assumes that the inductor ripple current of the design target is less than 1 A, and its value can be calculated by the following expressions in Boost mode:

\[ L = \frac{D_{up} \cdot V_i}{\Delta i_L \cdot f_s} \]  

(27)

where \( \Delta i_L = 1 \) A is the expected inductor current ripple, and \( V_C3 \) is the average voltage of \( C3 \). And finally the minimum inductance under uncoupled mode \( L_{min} = 125 \mu H \) is calculated.

As mentioned above, small inductance can accelerate the ACS process, increase system stability. What’s more, smaller inductance can reduce the volume of coupled-inductors as well as increase power density. Thus, without considering the inductor current ripple, winding losses and phase cross-over frequency, smaller inductance should be adopted. However, considering smaller inductors will lead to larger ripple current and inductor losses, CIs are used to reduce the current ripple further, on the premise that with the same initial inductance \( L_{min} \). Take CCM Boost stage for example, Figure 8 shows that the inductor ripple current equals to the current decrement of \( L_1 \) during time interval \([t_2-t_3]\), which is proportional to the equivalent inductance \( L_{EQ1} \) within the same period:

\[ \frac{di_{L1}}{dt} = \frac{L(V_L - V_{C1}) + MV_i}{L^2 - M^2} \]  

(28)

where \( V_{C1} = 4V_L/(1 - D_{up}) \), and \( M = kL \). Then:

\[ \frac{di_{L1}}{dt} = \frac{V_L(1 - \frac{1}{1-D_{up}} + k)}{(1 - k^2)L} \]  

(29)

\[
\begin{align*}
\frac{\partial}{\partial D} \left( \frac{di_{L1}}{dt} \right) &= \frac{D_{up} - 1 - V_L}{(1 - D_{up})^2 (1 - k^2)L} \\
\frac{\partial}{\partial k} \left( \frac{di_{L1}}{dt} \right) &= \frac{V_L(1 - k^2)L + 2V_L(1 - \frac{1}{1-D_{up}} + k)kL}{(1 - k^2)^2 L^2} \\
\frac{\partial}{\partial L} \left( \frac{di_{L1}}{dt} \right) &= \frac{(1 - k^2)L - V_L(1 - \frac{1}{1-D_{up}} + k)(1 - k^2)}{(1 - k^2)^2 L^2}
\end{align*}
\]

(30)

Equation (30) describes the relationship between \( L_{EQ1} \), \( D_{up} \), \( k \) and \( L_1 \). When Equation (30) equals to zero, the relevant maximum equivalent inductance will be obtained. Thus, with the same inductance and different coupling coefficients, the ripple current can be minimized if the equivalent inductance \( L_{EQ1} \) reaches a maximum:
In the same way, the optimal $k$ value corresponding to the global maximum $L_{EQ2}$ in CCM Buck stage can be obtained:

$$k = \left( 1 - D_{down} - \sqrt{1 - 2D_{down}} \right) / (D_{down})$$

Based on the expression Equations (30)–(32), Figure 15 can be obtained, and we can see that:

1. With a smaller initial channel inductance, a more tiny variation of the equivalent inductance with changing $D_{up}/D_{down}$ will be obtained, which indicates a smaller input ripple current in the range of any load condition;
2. The maximum equivalent inductance is related to duty cycle $D_{up}$ or $D_{down}$, for example, if rated $D_{up}$ equals to 0.64 or $D_{down}$ equals to 0.36, then the optimized coupling coefficient is $k = 0.3$. It is obviously that the optimized $k$ value in CCM Boost operation and CCM Buck operation is equal, when rated $V_L$ and $V_H$ are given.

![Figure 15. Equivalent inductance curves versus $k$ and $D$](image)

According to the above two conclusions and the $L_{min}$ under uncoupled mode, finally, $L = 120 \, \mu H$ and $k = 0.3$ can be selected, where $k = 0.3$ is the optimum solution of the coupling coefficient under rated load condition.

### 4.3.2. Optimal Design of SCs

According to the assumed conditions in Section 3.1, to facilitate the circuit analyses and calculations, voltage ripple across SCs has been ignored. However, quantitative analysis of the ripple voltage across SCs is necessary to guarantee the feasibility of the assumed conditions. It is generally known that the voltage ripple across switched-capacitors $C_1$, $C_2$ and $C_3$ can be expressed as:

$$\Delta U_C = \frac{I_C(1-D_{up})}{f_s \cdot C}$$

where $I_C$ is the mean value of the SCs current $i_C$ during a switching period $T_s$: 

$$k = \left( D_{up} - \sqrt{2D_{up} - 1} \right) / (1 - D_{up})$$
Assume that the voltage ripple of each SC is lower than 0.5 V, according to above expression, 

$$C_{\text{min}} = 21 \mu F$$

can be calculated. Considering the ripple voltage caused by ESR, parasitic inductance and thermal effect of capacitors in applications, 40 µF/500 V metalized-polyester film capacitors are selected. Because of its excellent characteristics like the high frequency performance, low ESR, low dielectric dissipation factor and high \(\frac{di}{dt}\) or \(\frac{du}{dt}\) capabilities. Its ESR is only about 5 m Ohm, and RMS current is about 19 A at 10 kHz, which is exactly suitable for the proposed high-frequency and large-current switching capacitor application.

### 4.3.3. Selection of Power MOSFETs

According to operation analysis in Sections 3.2 and 3.3, the voltage stress of the power switches \(S_1 - S_4\) and \(Q_4\) is \(V_H/4\), while for \(Q_1, Q_2\) and \(Q_3\), the voltage stress is \(V_H/2\) in either CCM Boost or CCM Buck stage. Furthermore, when the circuit works in discontinuous current mode (DCM), all switches \(S_1 - S_4\) and \(Q_1 - Q_4\) will suffer \(V_H/2\) voltage stress. In all of the normal states, the voltage stress of power switches only relate to the value of \(V_H\), no matter with duty cycle, value of \(V_L\) or load variations. From Figure 8 we can see that the voltage gain in Boost/Buck stage is 4 times of the conventional Boost/Buck converter, while the voltage stress is only one half.

The maximum current through \(S_2, S_3\) and \(S_4\) occurs at their turn off instant, superimposed by two inductor currents, which is calculated as:

$$i_s = \frac{2P_o}{V_H(1 - D_{up})} + \frac{V_L(D_{up} - 0.5)}{L_{EQ2D} \cdot f_s}$$

(35)

where \(L_{EQ2D}\) represents the equivalent inductance of channel 2 in Mode 4, which can be easily obtained with the method given in Section 2. Similarly, the maximum currents through \(Q_1, Q_2, Q_3\) and \(Q_4\) occur at their turn on instant, given as:

$$i_Q = \frac{P_o}{V_H(1 - D_{up})} + \frac{(V_H/4 - V_L)(1 - D_{up})}{2L_{EQ2A} \cdot f_s}$$

(36)

where \(L_{EQ2A}\) represents the equivalent inductance of channel 2 in Mode 1. In addition, the above expression is also suitable for switch \(S_1\), because when \(S_1\) turns off, the current \(i_{L1}\) all transfer from \(S_1\) to \(Q_1\). It indicates the current stress for \(S_1\) is smaller compared to \(S_2, S_3\) and \(S_4\), owing to only one inductor current \(i_{L1}\) flowing through.

According to Equations (35), (36) and the analysis above, the maximum current through \(S_1 - S_4\) and \(Q_1 - Q_4\) and the maximum voltage stress can be obtained easily. Moreover, in order to minimize the parasitic output capacitance and decrease the negative resonant current peak in DCM mode, increase the operating frequency as well as the power density and guarantee the conversion efficiency, SiC Power MOSFETs have been selected.
4.4. Losses Distribution

4.4.1. Conduction Losses on MOSFETs

For MOSFET $S_1$, the average current during its ON state is mean inductor current $I_{L1}$, so the conduction losses of $S_1$ can be calculated based on the Joule principle as follows:

$$P_{CM-S1} = I_{L1}^2 R_{ds-on} D_{up}$$  \hspace{1cm} (37)

where $R_{ds-on}$ is the MOSFET conduction resistor, and $D_{up}$ is the conduction time of $S_1$ in one switching period. In a similar way, the heat losses of $Q_1$ is obtained as:

$$P_{CM-Q1} = I_{L1}^2 R_{ds-on} (1 - D_{up})$$  \hspace{1cm} (38)

where $(1 - D_{up})$ is the conduction time of $Q_1$ in one switching period. Furthermore, it can obtained that: $I_{L1} = I_{L2} = I_{L3} = I_{L4} = I_{L4}$, with precondition: $D_1 = D_2 = D_3 = D_4 = D_{up}$. Thus the above expression is also suitable for $Q_2$, $Q_1$ and $Q_4$.

In reference to switches $S_2$, $S_3$ and $S_4$, the current flowing through is larger than $S_1$ due to two inductor currents superimposed. For switch $S_2$, the heat losses result from average inductor current $I_{L1}$ and $I_{L2}$ according to analyses in Section 3.2. In Mode 2, $S_2$ and $S_1$ are ON (duration of time: $(D_{up} - 0.5)T_s$), the current through $S_2$ is just $i_{L2}$ according to steady state waveforms shown in Figure 8, thus the average current in Mode 2 is calculated as:

$$I_{S2-M2} = I_{L2} + \frac{V_L - V_{CL}}{2L_{EQ2A}} (1 - D_{up})T_s + \frac{V_L (D_{up} - 0.5)T_s}{2L_{EQ2B}}$$  \hspace{1cm} (39)

where $L_{EQ2A}$ and $L_{EQ2B}$ are the equivalent inductance for channel 2 in Mode 2 and Mode 4 respectively. In Mode 3, $S_2$ ON and $S_1$ OFF (Duration of time: $(1 - D_{up})T_s$), the current through $S_2$ is the sum of $i_{L1}$ and $i_{L2}$. That is:

$$I_{S2-M3} = I_{L1} + I_{L2} = \frac{I_L}{2}$$  \hspace{1cm} (40)

In Mode 4, $S_2$ ON, $S_1$ OFF (Duration of time: $(D_{up} - 0.5)T_s$), the current $i_{L1}$ is removed from $S_2$. Therefore, the average current through $S_2$ in Mode 4 is calculated based on waveforms in Figure 8:

$$I_{S2-M4} = I_{L2} - \frac{V_L - V_{CL}}{2L_{EQ2A}} (1 - D_{up})T_s - \frac{V_L (D_{up} - 0.5)T_s}{2L_{EQ2B}}$$  \hspace{1cm} (41)

Combine Equations (40)–(42), and the total conduction losses of $S_2$ is expressed as:

$$P_{CM-S2} = I_{S2-M2}^2 R_{ds-on} (D_{up} - 0.5) + I_{S2-M3}^2 R_{ds-on} (1 - D_{up}) + I_{S2-M4}^2 R_{ds-on} (D_{up} - 0.5)$$  \hspace{1cm} (42)

Due to the circuit symmetry, the conduction losses of $S_3$, $S_4$ are equal to Equation (42).

4.4.2. Switching Losses of MOSFETs

The switching losses are composed of turn-on, turn-off losses and the free-wheel diode (FWD) losses. PWD losses is ignored considering that the mechanism of SR mode. According to reference [31–33], the calculation expression of turn-on and turn-off losses are obtained as:
\[
\begin{align*}
\frac{P_{\text{SW-ON}}}{2} &= \Delta U_{\text{on}} \cdot i_{\text{on}} \cdot T_{\text{sw-on}} \cdot f_s \\
\frac{P_{\text{SW-OFF}}}{2} &= \Delta U_{\text{off}} \cdot i_{\text{off}} \cdot T_{\text{sw-off}} \cdot f_s 
\end{align*}
\]  

where \( \Delta U_{\text{off}} \) represents the voltage level altering value before/after turn-off transient, and for each MOSFET, \( \Delta U_{\text{off}} = 100 \) V is always right. \( T_{\text{sw-off}} \) is the turn-off crossing time. \( \Delta U_{\text{on}} \) is also about 100 V for each switch, which is obtained from Figure 8. And \( T_{\text{sw-on}} \) is the turn-on overlap time.

In a same switching point, the instantaneous current value of \( S_1, S_2, S_3 \) and \( S_4 \) at turn-off moment \( i_{\text{off-S}} \) is equal to the instantaneous current value of \( Q_1, Q_2, Q_3 \) and \( Q_4 \) at turn-on moment \( i_{\text{on-Q}} \), and then:

\[
i_{\text{off-S}} = i_{\text{on-Q}} = I_L(1 - D_{up}) \frac{(V_{C1} - V_L)(1 - D_{up})}{2L_{EQ1C}f_s}
\]

In a similar way:

\[
i_{\text{on-S}} = i_{\text{off-Q}} = I_L(1 - D_{up}) \frac{(V_{C1} - V_L)(1 - D_{up})}{2L_{EQ1C}f_s}
\]

Based on Equations (43)–(45), the switching losses of all MOSFETs can be obtained.

4.4.3. Capacitor ESR Losses

The power losses on capacitors is proportional to ripple current and total dissipation resistor ESR. And the equation for switching capacitor \( C_1 \) is given as:

\[
P_{SC1} = \Delta i_{L1}^2 R_{C-ESR}^2 (1 - D_{up})
\]

In reference to SCs \( C_1, C_2, C_3 \), the ripple current is just the inductor current ripple \( \Delta i_L \). While for filter capacitors, the ripple current refer to input/output current ripple.

4.4.4. ESR Losses of CIs

The heat consumption on each inductor is proportional to its average current and the parasitic resistor. That is:

\[
P_{L-ESR} = I_L^2 R_{L-ESR}
\]

4.4.5. Magnetic Losses of CIs

The magnetic losses of coupled inductors can be calculated as [34]:

\[
P_{L-CORE} = p_w \cdot W_{Fe}
\]

where \( W_{Fe} \) is the total weight of the selected core, and \( p_w \) is the losses on unit weight, the unit is: mW/g, and the \( p_w \) can be found out from datasheet.
5. Experimental Results

The experiments are performed under voltage and current closed-loop conditions. The output/input voltage acquisition is simply achieved by voltage-splitter resistances, and the inductor current acquisition utilizes a LAH 25-NP current transducer. According to the analysis in Section 4.2, the average inductor currents are identical to each other \( I_{L1} = I_{L2} = I_{L3} = I_{L4} \), assuming that \( D_1 = D_2 = D_3 = D_4 = D_{up} \). Based on this fact, channel current transducers can be reduced to just one. The experimental results of channel current comparison shown in the following figures are just the results with the effect of ACS fulfilled by SCs, there is no other additional current-sharing controller. This would dramatically reduce circuit complexity, cost and controller design.

As illustrated in Figure 16, a 500 W prototype converter is built in the laboratory. It can be seen that each of the CIs is constituted with two separated leakage inductors and a strong coupling \( (k = 0.95) \) transformer, which is used to reduce the difficulty of CIs construction \( (k = 0.3) \). Moreover, with limited selectable types, \( S_1 \) to \( S_4 \) as well as \( Q_1 \) to \( Q_4 \) are the same type of SiC MOSFET: C2M0080120D. In addition, isolated driver circuit based on pulse transformer is used as the driver circuit of those MOSFETs. \( S_1 \) and \( Q_1 \) (the same as \( S_2 \) and \( Q_2 \), or \( S_3 \) and \( Q_3 \), or \( S_4 \) and \( Q_4 \)) share a drive circuit, and complementary symmetrical PWM driving signals will be supplied to \( S_1 \) and \( Q_1 \) (the same as \( S_2 \) and \( Q_2 \), or \( S_3 \) and \( Q_3 \), or \( S_4 \) and \( Q_4 \)) respectively. In this way only four identical drive circuits are needed, which can effectively reduce the complexity of the driving circuits.

![Figure 16. Picture of the laboratory setup.](image)

Based on above analyses and optimization methods, the optimized parameters are shown in Table 1.

| Parameters and components | Values (units) |
|---------------------------|----------------|
| Rated power \( P_n \)     | 500 W          |
| Low side input DC voltage \( V_L \) | 24–48 V       |
| High side input DC voltage \( V_H \) | 400 V         |
| Operating frequency \( f_s \) | 200 kHz        |
| Power MOSFETs             | C2M0080120D    |
| Switched capacitors \( (C_1, C_2, C_3) \) | 40 \( \mu \)F |
| Input/Output Capacitors \( (C_L, C_h) \) | 80 \( \mu \)F |
| ESR \( (C_1, C_2, C_3, C_L, C_h) \) | 5 m Ohm        |
Table 1. Cont.

| Parameters and components          | Values (units) |
|-----------------------------------|----------------|
| Inductance of channel 1 ($L_1$)   | 122 $\mu$H     |
| Inductance of channel 2 ($L_2$)   | 128 $\mu$H     |
| Inductance of channel 3 ($L_3$)   | 124 $\mu$H     |
| Inductance of channel 4 ($L_4$)   | 126 $\mu$H     |
| Coupling coefficient ($k$)         | 0.3            |
| Weight of magnetic core           | 25.2 g         |
| Core loss per unit weight         | 20 mW/g        |
| Length of magnetic path           | 8.95 cm        |
| Number of turns                   | 48             |
| ESR ($L_1, L_2, L_3, L_4$)        | 30 m Ohm       |

Figures 17a,c,d show the input and output voltages, channel 1 inductor current, and drain-source voltage of $Q_1$ in CCM Boost mode under different input voltages (24 V to 48 V). It can be seen that inductor current ripples are less than 1 A in the entire input voltage range, and voltage stress across $Q_1$ is about 200 V. When $V_L$ side voltage varies from 24 V to 48 V, output voltage $V_H$ fluctuates between 395 V and 405 V. As shown in Figure 17c, when $V_L = 23.2$ V, each channel average inductor current is about 5.5 A, and peak value is about 6 A. Figure 17b shows channel 1 and channel 2 inductor current waveforms, drain-source and gate-source voltages of $S_1$ in rated CCM Boost mode. Combine this figure with the inductances given in Table 1, it can be seen that when inductance deviation among $L_1, L_2, L_3$ and $L_4$ are less than ±5%, the coefficient of ACS executed by SCs will be greater than 0.95 (Just the effect of ACS fulfilled by SCs, without extra current-sharing control). Furthermore, voltage stress across $S_1$ is about 100 V.

![Figure 17a](image1.png)  ![Figure 17b](image2.png)  ![Figure 17c](image3.png)  ![Figure 17d](image4.png)

**Figure 17.** Experimental waveforms under CCM Boost mode (a) and (b) 36 V to 400 V; (c) 24 V to 400 V; (d) 48 V to 400 V.
Figure 18 displays the experimental results obtained in CCM Buck stage under 400 V (or 300 V) input and 36 V output. Figure 18a gives the input and output voltages, channel 1 inductor current, and drain-source voltage of $Q_1$. It can be seen that inductor current ripples remain less than 1 A when the output voltage $V_L = 36$ V. Voltage stress across $Q_1$ is still approximately 200 V. Figure 18b shows the channel 1 and channel 2 inductor currents, input and output voltages, it can be seen that the coefficient of ACS is still larger than 0.95.

![Figure 18. Experimental waveforms under CCM Buck stage (a) 400 V to 36 V (b) 300 V to 36 V.](image)

Figure 19 shows the experimental waveforms of the input and output voltages, channel 1 inductor current, and drain-source voltage of $Q_1$ under light-load conditions. Figure 19a is the waveforms of Boost mode with 15.7 W output power, and Figure 19b shows the waveforms of Buck mode with 13 W output power. Therefore, the proposed BDC can achieve quasi-critical inductor currents even under tiny load conditions. Moreover, as shown in Figure 19, ZVS turn-on for each switch is achieved under light-load conditions, which is beneficial to the light-load efficiency optimization.

![Figure 19. Experimental results in light-load condition (a) 36 V input and 400 V/10 k Ohm output; (b) 400 V input and 36 V/100 Ohm output.](image)

Figure 20 gives the dynamic response of the proposed BDC against load variation. Figure 20a shows the input and output voltages, channel 1 and channel 2 current waveforms with 34.6 V input and 394 V output. During this time period, load resistance is changed between 10 k Ohm and 320 Ohm. It can be seen that output voltage variation is less than 15 V. Figure 20b shows the input and output voltages, channel 1 and channel 2 current waveforms when input is 300 V and output 36.5 V. At this time, load resistance is changed between 100 Ohm and 2.5 Ohm. It can be seen that output voltage variation is less than 10 V. Therefore, fast and stabilized dynamic responses are achieved.

![Figure 20. Dynamic response of the proposed BDC against load variation.](image)
Figure 20. Dynamic response of the proposed BDC against load variation (a) load resistance variation between 10 k Ohm and 320 Ohm; (b) load resistance variation between 100 Ohm and 2.5 Ohm.

The measured efficiency of the proposed BDC is depicted in Figure 21a, and the test result is based on YOKOGAWA WT3000 data, with a basic power accuracy of ±0.02% of reading, DC and 0.1 Hz–1 MHz measurement bandwidths. When the output power is 500 W, the efficiency under CCM Boost stage and CCM Buck stage are about 96.1% and 94.8% respectively. Benefit from the margin of the selected devices and heat sink, during the experiment, the maximum output power of the proposed converter has been raised to 1 kW, the efficiency under 1 kW Boost stage and 1 kW Buck stage are about 95.8% and 94.5% respectively. Moreover, due to the achievement of the ZVS and SR features under light-load conditions, the fluctuation of the system efficiency curve is relatively small.

In order to clarify the actual efficiency further, the dissipated power has been calculated and shown in Figure 21b, based on equations in Section 4.4 and parameters in Table 1. From Figure 21b we can see that the total power losses is 19 W, accounting for 3.8% in rated condition. This matches the measured efficiency (96.1% at 500 W Boost stage) well. Also, the heat losses induced by parasitic ESR of inductors is about 1.4 W with magnetic counterpart 2.9 W. The capacitor ESR caused extremely low energy losses. However, the power dissipated in MOSFETs is relatively high, with switching losses and conduction losses 7.4 W and 7 W, respectively.

Figure 21. (a) Measured efficiency. (b) Calculated losses breakdown.
6. Conclusions

This paper proposed a 4-phase interleaved HVCR BDC topology with SCs and CIs, which can prominently reduce the current/voltage stress of the power devices, and only needs a simple PWM control method. With an optimized design of the coupled inductors and switched capacitors, it can further reduce the inductance and inductor volume, lower the channel ripple current, and improve the dynamic performance of ACS. A 500 W prototype converter is built in the laboratory for experimental verification of the proposed topology. The maximum voltage stress of each MOSFET is about VH/2. Under different working conditions, inductor current ripples remain less than 1 A and the coefficient of ACS is greater than 0.95. The prototype converter efficiency achieves 96.1% in CCM Boost stage and 94.8% in CCM Buck stage at rated load.

Furthermore, the proposed circuit can be extended into n-mode/1/n-mode (n is a positive even number: 2, 4 … n) HVCR BDC shown in Figure 22. Higher VCR and lower current/voltage stress characteristics can be obtained by extending structure, and the relationship between VH and VL can be derived by:

\[
\begin{align*}
M_{nH} &= \frac{V_H}{V_L} = \frac{n}{n}(1-D_{up}) \\
M_{nL} &= \frac{V_L}{V_H} = D_{down}/n
\end{align*}
\]

Figure 22. Extensible circuits based on the proposed topology.

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Author Contributions

Li-Kun Xue, Ping Wang and Yi-Feng Wang designed the main parts of the study, including the circuit model, topology innovation and prototype development. Tai-Zhou Bei helped in the DSP controller procedures. Hai-Yun Yan was also responsible for writing the paper.
Conflicts of Interest

The authors declare no conflict of interest.

Reference

1. Long, B.; Jeong, T.W.; Lee, J.D.; Jung, Y.C.; Chong, K.T. Energy management of a hybrid AC-DC micro-grid based on a battery testing system. *Energies* 2015, 8, 1181–1194.

2. Chang, C.-H.; Wu, F.-Y.; Chen, Y.-M. Modularized bidirectional grid-connected inverter with constant-frequency asynchronous sigma-delta modulation. *IEEE Trans. Ind. Electron.* 2012, 11, 4088–4100.

3. Dong, D.; Cvetkovic, I.; Boroyevich, D.; Zhang, W.; Wang, R.; Mattavelli, P. Grid-interface bidirectional converter for residential DC distribution systems—Part one: High-density two-stage topology. *IEEE Trans. Power Electron.* 2013, 4, 1655–1666.

4. Rawn, B.G.; Lehn, P.W.; Maggiore, M. Control methodology to mitigate the grid impact of wind turbines. *IEEE Trans. Energy Convers.* 2007, 2, 431–438.

5. Carpinelli, G.; Celli, G.; Mocci, S.; Mottola, F.; Pilo, F.; Proto, D. Optimal integration of distributed energy storage devices in smart grids. *IEEE Trans. Smart Grid* 2013, 2, 985–995.

6. Wang, X.Y.; Vilathgamuwa, D.M.; Choi, S.S. Determination of battery storage capacity in energy buffer for wind farm. *IEEE Trans. Energy Convers.* 2008, 3, 868–878.

7. Wei, L.; Joos, G. Comparison of energy storage system technologies and configurations in a wind farm. In Proceedings of the IEEE Power Electronics Specialists Conference, Orlando, FL, USA, 17–21 June 2007; pp. 1280–1285.

8. Giess, H. The operation of VRLA lead acid batteries in parallel strings of dissimilar capacity or can we now sin? In Proceedings of the 21st International Telecommunication Energy Conference, Copenhagen, Denmark, 6–9 June 1999.

9. Sathyan, S.; Suryawanshi, H.M.; Ballal, M.S.; Shitole, A.B. Soft switching DC-DC converter for distributed energy sources with high step up voltage capability, *IEEE Trans. Ind. Electron.* 2015, 99, 1.

10. Zhao, B.; Song, Q.; Liu, W.H.; Sun, Y.D. Overview of dual-active-bridge isolated bidirectional DC-DC converter for high-frequency-link power-conversion system. *IEEE Trans. Power Electron.* 2014, 8, 4091–4106.

11. Zhao, B.; Song, Q.; Liu, W.H.; Sun, Y.D. Dead-time effect of the high-frequency isolated bidirectional full-bridge DC-DC converter: Comprehensive theoretical analysis and experimental verification. *IEEE Trans. Power Electron.* 2014, 4, 1667–1680.

12. Wang, K.; Lin, C.Y.; Zhu, L.; Qu, D.; Lee, F.C.; Lai, J.S. Bidirectional dc to dc converters for fuel cell systems. In Proceedings of the Power Electronics Transportation, Dearborn, MI, USA, 22–23 October 1998; pp. 47–51.

13. Jung, J.-H.; Kim, H.-S.; Ryu, M.-H.; Baek, J.-W. Design methodology of bidirectional CLLC resonant converter for high-frequency isolation of DC distribution systems. *IEEE Trans. Power Electron.* 2013, 4, 1741–1755.
14. Jung, J.-H.; Kim, H.-S.; Kim, J.-H.; Ryu, M.-H.; Baek, J.-W. High efficiency bidirectional LLC resonant converter for 380 V DC power distribution system using digital control scheme. In Proceedings of the 27th Annual IEEE Applied Power Electronics Conference and Exposition, 5–9 February 2012; pp. 532–538.

15. Wang, Z.; Li, H. A soft switching three-phase current-fed bidirectional DC-DC converter with high efficiency over a wide input voltage range. *IEEE Trans. Power Electron*. 2012, 2, 669–684.

16. Sedaghati, F.; Hossein Hosseini, S.; Sabahi, M.; Gharehpetian, G.B. Analysis and implementation of a modular isolated zero-voltage switching bidirectional dc-dc converter. *IET Power Electron.* 2013, 8, 2035–2049.

17. Li, W.H.; Xu, C.; Yu, H.B.; Gu, Y.J.; He, X.N. Analysis, design and implementation of isolated bidirectional converter with winding-cross-coupled inductors for high step-up and high step-down conversion system. *IET Power Electron.* 2013, 1, 67–77.

18. Lin, B.-R.; Huang, C.-L.; Lee, Y.-E. Asymmetrical pulse-width modulation bidirectional DC-DC converter. *IET Power Electron.* 2008, 3, 336–347.

19. Ko, Y.-P.; Lee, Y.-S.; Liu, L.-J. Design of high efficiency multi-phase QR ZCS switched-capacitor bidirectional power converters. In Proceedings of the 8th International Conference on Power Electronics and ECCE Asia, Jeju, Korea, 30 May–3 June 2011; pp. 860–867.

20. Zhao, Q.; Lee, F.C. High-efficiency, high step-up DC-DC converters. *IEEE Trans. Power Electron.* 2003, 1, 65–73.

21. Law, K.K.; Cheng, K.W.E.; Yeung, Y.P.B. Design and analysis of switched-capacitor-based step-up resonant converters. *IEEE Trans. Circuits Syst.* 2005, 5, 943–948.

22. Lee, Y.-S.; Chiu, Y.-Y. Zero-current-switching switched-capacitor bidirectional DC-DC converter. *IEEE Proc. Electric Power Appl.* 2005, 6, 1525–1530.

23. Hsieh, Y.-P.; Chen, J.-F.; Yang, L.-S.; Wu, C.-Y.; Liu, W.-S. High-conversion-ratio bidirectional DC-DC converter with coupled inductor. *IEEE Trans. Ind. Electron.* 2014, 1, 210–222.

24. Duan, R.-Y.; Lee, J.-D. High-efficiency bidirectional DC-DC converter with coupled inductor. *IET Power Electron.* 2012, 1, 115–123.

25. Wai, R.-J.; Duan, R.-Y.; Jheng, K.-H. High-efficiency bidirectional dc-dc converter with high-voltage gain. *IET Power Electron.* 2012, 2, 173–184.

26. Lee, Y.-S.; Ko, Y.-P.; Cheng, M.-W.; Liu, L.-J. Multiphase zero-current switching bidirectional converters and battery energy storage application. *IEEE Trans. Power Electron.* 2013, 8, 3806–3815.

27. Lee, Y.-S.; Chiu, Y.-Y.; Cheng, M.-W. Inverting ZCS switched-capacitor bi-directional converter. In Proceedings of the 37th Power Electronics Specialists Conference, Jeju, Korea, 18–22 June 2006; pp. 1–6.

28. Kwon, M.; Choi, W. High gain soft-switching bidirectional DC-DC converter for eco-friendly vehicles. *IEEE Trans. Power Electron.* 2014, 4, 1659–1666.

29. Xue, L.K.; Wang, P.; Wang, Y.F.; Li, W. High step-up DC-DC converter with switched capacitors and interleaved inductors. In Proceedings of the 2014 International Electronics and Application Conference and Exposition, Shanghai, 5–8 November 2014; pp. 26–29.

30. Wong, P.L.; Wu, Q.Q.; Xu, P.; Yang, B.; Lee, F.C. Investigating coupling inductors in the interleaving QSW VRM. In Proceedings of the 15th 2000 Annual IEEE Applied Power Electronics Conference and Exposition, New Orleans, LA, USA, 6–10 February 2000; pp. 973–978.
31. Pressman, A.I.; Billings, K.; Morey, T. *Switching Power Supply Design*, 3rd ed.; McGraw-Hill Education: New York, NY, USA, 2009.

32. Havanur, S. Quasi-clamped inductive Switching behaviour of power Mosfets. In Proceedings of the IEEE Power Electronics Specialists Conference, Rhodes, Greece, 15–19 June 2008; pp. 4349–4354.

33. Ren, Y.C.; Xu, M.; Zhou, J.H.; Lee, F.C. Analytical loss model of power MOSFET. *IEEE Trans. Power Electron.*, **2006**, *21*, 310–319.

34. McLyman, W.T. *Transformer and Inductor Design Handbook*, 3rd ed.; Marcel Dekker, Inc.: New York, NY, USA, 2004.

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