Lack of correlation between C-V hysteresis and capacitance frequency dispersion in accumulation of metal gate/high-k/n-InGaAs metal-oxide-semiconductor stacks

S. M. Pazos, F. L. Aguirre, K. Tang, P. McIntyre, and F. Palumbo

Citation: Journal of Applied Physics 124, 224102 (2018); doi: 10.1063/1.5031025
View online: https://doi.org/10.1063/1.5031025
View Table of Contents: http://aip.scitation.org/toc/jap/124/22
Published by the American Institute of Physics
Lack of correlation between C-V hysteresis and capacitance frequency dispersion in accumulation of metal gate/high-k/n-InGaAs metal-oxide-semiconductor stacks

S. M. Pazos,¹,² F. L. Aguirre,¹,² K. Tang,³ P. McIntyre,³ and F. Palumbo¹,²,a)

¹Unidad de Investigación y Desarrollo de las Ingenierías, Facultad Regional Buenos Aires, Universidad Tecnológica Nacional (UIDI FRBA-UTN), Medrano 951, C1179AAC Buenos Aires, Argentina
²Consejo Nacional de Investigaciones Científicas y Técnicas, Godoy Cruz 2290, C14250QB Buenos Aires, Argentina
³Department of Materials Science and Engineering, Stanford University, Stanford, California 94305, USA

(Received 27 March 2018; accepted 24 November 2018; published online 12 December 2018)

The correlation between capacitance-voltage hysteresis and accumulation capacitance frequency dispersion of metal gate/high-k/n-InGaAs metal-oxide-semiconductor stacks is experimentally assessed. Samples fabricated employing forming gas annealing (FGA) or substrate air exposure to obtain different densities of defects were thoroughly characterized and the results were compared with previous literature on the topic. Results indicate a lack of correlation between capacitance-voltage hysteresis and accumulation capacitance dispersion with frequency, suggesting that defects with remarkably different kinetics are involved in each phenomenon. This is assessed through the dependence of the capacitance-voltage hysteresis with DC bias and stress time, observing that permanent interface defect depassivation under bias has no effect on the hysteresis width after stress. Overall, capacitance-voltage hysteresis probes slow trapping mechanisms throughout the oxide and the bandgap, which are consistent with the negative charge trapping characteristic of the current-time curves for FGA samples at constant voltage stress. Instead, accumulation capacitance frequency dispersion probes defects with short trapping/detrapping characteristic times that can be linked to the stress induced leakage current of air exposed samples under constant DC stress. Experimental results indicate that each effect must be assessed separately due to the large difference in the kinetics of the probed defects. Published by AIP Publishing. https://doi.org/10.1063/1.5031025

I. INTRODUCTION

Among III–V compound semiconductors, InGaAs emerged as an attractive alternative to silicon for future complementary metal oxide semiconductor (CMOS) technologies due to its high electron mobility, but it has shown poor interface quality when paired with high-k dielectrics. In this regard, oxide defects, such as interface traps ($D_{it}$) due to dangling bonds and border traps (BTs) ascribed to oxygen vacancies, located away from the interface, have a strong impact on the electrical characteristics of MOS stacks. The spotlight was recently set on the accumulation capacitance ($C_{acc}$) dispersion with frequency. The reduction of the measured capacitance in accumulation at high frequencies can be linked to BTs through distributed bulk-oxide trap models based on a spatial distribution of defects located in the vicinity of the high-k/III–V interface. In addition, oxide defects are also accounted for the hysteresis observed on C-V sweeps in trace back mode, and special attention has been drawn toward the energy and spatial distribution of such defects.

Surface treatments such as sulfur passivation, nitridation, As$_2$O$_5$ capping and decapping, hydrogen, oxygen, and forming gas anneals (FGA) have shown diverse levels of success in the passivation of $D_{it}$ and BTs, resulting in different values for the capacitance dispersion with frequency. Dependences on fabrication process have been also observed on the widths of the loops during C-V hysteresis sweeps. Although both C-V hysteresis and $C_{acc}$ dispersion with frequency have been attributed to BTs, a clear correlation has not yet been found between them. Recently, Lin et al. provided an insight into this relationship based on their respective dependence on the FGA temperature: the optimal temperature for FGA (450 °C) is linked to the lower BT density ($N_{bt}$) estimated by means of a distributed BT model and correlated to the most pronounced reduction of $N_{bt}$ extracted from C-V hysteresis. However, no clear trends were observed in Al$_2$O$_3$-based stacks for the variation of C-V hysteresis with FGA temperature. It is also worth mentioning that BT estimation by means of this method is performed in Ref. assuming a 1 nm probing depth into the oxide with homogeneous spatial trap distribution.

On the other hand, in previous work by Tang et al., it is possible to observe hydrogen isotope effects and defect depassivation on forming gas (FG) annealed Pd/Al$_2$O$_3$/n-InGaAs MOS stacks, highlighting that although FGA treatment reduces the initial $D_{it}$ and $N_{bt}$, it also causes significant hysteretic behavior, indicating that C-V hysteresis is not directly correlated with the initial $D_{it}$ and $N_{bt}$. Contrarily, a study of the FGA impact on the electrical characteristics of sulfur passivated Pt/Au/Al$_2$O$_3$/InGaAs(110)
MOS capacitors by Fu et al. showed a strong reduction of hysteresis in both p-type and n-type substrate capacitors, in addition to marginally reduced $D_a$ and $N_{it}$. Additionally, independent results by Do et al. have shown that oxygen segregation can form unstable interfacial layers at the metal gate (MG)/high-$k$ interface depending on the MG material and the high-$k$/III–V interface preparation. This effect can be responsible for the presence of mobile ions that have an impact on the electrostatics of the device under study, producing different hysteresis widths for certain metal gate materials and annealing atmospheres.

These strong disconnections between different reported results and the complexity of the trapping kinetics and of both interfaces present in the MG/high-$k$/InGaAs system make it difficult to relate two indicators of defects that have been used to characterize border traps, as are the capacitance frequency dispersion in accumulation and C-V hysteresis. In this work, 4 sets of the same Pd/Al$_2$O$_3$/n-InGaAs MOS stacks were intentionally fabricated to display different levels of $D_a$ and $N_{it}$. These samples showed evidence of the lack of correlation between C-V hysteresis and frequency dispersion, displaying strongly different trapping/detrapping kinetics involved during the AC and DC characterization. The use of constant voltage stress (CVS) helps one to separate frequency dispersion from C-V hysteresis in order to improve the understanding of this lack of correlation through the strong time and DC bias dependence of C-V hysteresis in annealed samples.

II. EXPERIMENTAL

The fabrication process of the samples employed in this study is sketched in Fig. 1. Epitaxial n-type $In_{0.53}Ga_{0.47}As$ (100) substrates doped with Si (1 x $10^{17}$ cm$^{-3}$) [epilayers deposited on lattice-matched n-InP (100) wafers] were coated with 200 nm of amorphous As$_2$ capping during the post-growth cooling in the InGaAs molecular beam epitaxy chamber. The As$_2$ capping protects the InGaAs surface from oxidation and contamination during air exposure before the substrates are loaded into the Atomic Layer Deposition (ALD) chamber, where 10 nm of Al$_2$O$_3$ was deposited using 100 cycles of alternating trimethylaluminum (TMA) and H$_2$O pulses at a substrate temperature of 270°C after a decapping procedure. Samples with intentionally modified trap densities were prepared by first exposing the InGaAs substrate surface to room temperature lab air in the light for 5 days after As$_2$ decapping, and then reloading them into the ALD chamber for the same cycle count of Al$_2$O$_3$ ALD. After Al$_2$O$_3$ deposition, 40 nm thick circular (50–125 μm radius) Pd top electrodes and 100 nm thick Al back contacts were deposited by thermal evaporation. A subset of the Pd/Al$_2$O$_3$/InGaAs MOS capacitor samples prepared with both types of decapping conditions were treated with forming gas (5%H$_2$/95%N$_2$) anneal for 30 min at 400°C. On the other hand, a subset of As$_2$ decapped samples were treated with an O$_2$ anneal and a subset of air exposed samples were not annealed anyhow. As used in similar stacks in the past annealing in O$_2$ atmosphere annihilates oxygen vacancies that exist in the high-$k$ material, and it was chosen in this work as a trade-off between $D_a$, BT passivation, and C-V hysteresis between no FGA and FGA samples with As$_2$ decap. This resulted in a total of four types of samples with different magnitudes for C-V hysteresis and $C_{acc}$ frequency dispersion. The fabrication procedure has been thoroughly tuned throughout the years, and further details about the process have been widely reported in our previous papers. Along this work and for clarity purposes, reference samples that underwent As$_2$ decapping and FGA are identified by the code FGA-#, while those annealed in O$_2$ are assigned the code O2A-##. Samples that were intentionally air-exposed are identified with the code AE: the set of samples that underwent FGA is identified as AE-FGA-#3 and those that were not annealed are assigned the identifier AE-#4.

AC C-V measurements were performed at room temperature and at the dark, using an Agilent E4980A LCR meter and a triaxial probe station. Multi-frequency C-V (MFCV) experiments were conducted from an AC frequency of 200 Hz up to 1.1 MHz. Accumulation capacitance dispersion with frequency is extracted at a given gate voltage as to maintain a constant electric field across the oxide in all samples, through the expression $100 \times \left( C_{acc,200Hz} - C_{acc,f} \right) / C_{acc,200Hz}$, where $C_{acc,200Hz}$ is the accumulation capacitance at the lowest frequency and $C_{acc,f}$ is the accumulation capacitance at each frequency step $f$.

Successive two-way voltage stress sweeps (C-V dynamic stress) and constant voltage stress (CVS) sweeps with increasing stress times were performed to study the hysteresis cycle of the samples when stressed in the accumulation
regime. C-V hysteresis width ($V_{\text{Hys}}$) observed in such measurements was extracted at the flatband voltage capacitance value ($C_{\text{FB}}$) obtained from the first sweep toward accumulation (using the inflection point technique) and interpolating the voltage values at $C_{\text{FB}}$ in the following sweeps. $V_{\text{Hys}}$ is then extracted as the voltage difference $V_{C_{\text{FB}} \text{bwd}} - V_{C_{\text{FB}} \text{fwd}}$, where the terms represent the voltages at $C_{\text{FB}}$ in the forward and backward sweeps, respectively.

I-V and I-t measurements were carried out using a Keithley 2636 Source Measure Unit (SMU). I-V measurements were performed until the breakdown of the sample when biased toward positive voltages. I-t measurements were performed at constant voltage stress with a mean time resolution fixed at 20 ms.

### III. CHARACTERIZATION RESULTS

#### A. Multi-frequency capacitance-voltage measurements

Figure 2 shows the typical MFCV curves for all sets of samples. Vertical dashed lines in the plot indicate the flatband voltage calculated using the inflection point technique. The MFCV characteristics of the samples are largely consistent with the previous work by Tang et al. and those reported in the literature. Significant frequency dispersion can be observed from inversion into accumulation. Dispersion in such regions can be explained by the interface traps inside the bandgap and the response of border traps, respectively. Horizontal dashed lines indicate the expected nominal oxide capacitance ($C_{\text{ox}}$) considering 10 nm Al$_2$O$_3$ with $k=7$. The lower experimental values observed toward accumulation can be attributed to the reduced density of states in the $\Gamma$ valleys of the conduction band in InGaAs.

Compared to the samples fabricated using the standard in situ As$_2$ decapping procedure (samples FGA-#1 and O2A-#2), the intentionally air-exposed samples (sets AE+FGA-#3 and AE-#4) clearly demonstrate both a larger dispersive capacitance feature in inversion and larger weak inversion hump, ascribed to higher $D_{\text{it}}$ across the bandgap. This can be observed qualitatively comparing Figs. 2(a) and 2(b) with 2(c) and 2(d). This indicates a degradation of the interface quality due to the pre-ALD air exposure of the InGaAs surface, which causes surface contamination and formation of a defective interfacial InGaAs native oxide layer observed in XPS measurements in previous work. It is noteworthy that the presence of such a layer does not severely impact the effective oxide capacitance due to a thermally-activated conduction effect that results in the inter-layer acting more like a semiconductor than as an insulator.

In terms of $C_{\text{acc}}$ dispersion with frequency, samples AE-#4 show the most pronounced dispersive behavior at first glance. But to clearly compare between sets of samples, Fig. 3 shows the relative dispersion of the capacitance in accumulation as a function of the AC probing frequency, with a reference capacitance value obtained from the C-V sweep at 200 Hz and at an applied voltage of 1.35 V referred to $V_{\text{FB}}$ (absolute applied voltages $V_G$ between 2 V and 2.7 V depending on the sample). These biasing conditions are set so that similar regions of the bandgap are being probed for each sample: simulations considering non-parabolic band effects on ideal Al$_2$O$_3$/InGaAs MOS structures render a surface potential variation of roughly 110 mV per volt increase of the applied gate voltage $V_G$. Under these conditions, the energy region being probed during the extraction of the accumulation capacitance dispersion with frequency is located around 0.15 eV into the conduction band. Although differences in the trap density and capacitance equivalent thickness ($C_{\text{ET}}$) among sets of samples can introduce slight

![FIG. 2. 200 Hz to 1.1 MHz C-V curves for the four sets of samples: As$_2$ decap + FGA (FGA-#1) (a), As$_2$ decap + O$_2$ anneal (O2A-#2) (b), air exposed + FGA (AE+FGA-#3) (c), and air exposed without annealing (AE-#4) (d).](image)

![FIG. 3. Frequency dispersion of the capacitance in accumulation vs. probing frequency. Filled markers represent samples that underwent FGA, while unfilled markers correspond to an O$_2$ or no anneal whatsoever.](image)
variations on the actual position of the Fermi level, the very weak dependence of the extracted dispersion with the accumulation voltage in our samples (clearly observed on the MFCV curves when compared to other reported results in the literature\textsuperscript{12,17} and quantified for our samples to be <2% relative variation per 500 mV increase in maximum $V_G$) does not alter the interpretation of our results.

It should be pointed out that there is no general agreement on the voltage toward accumulation at which dispersion should be measured, but in order to compare different material stacks by probing the same energy regions, an equal electric field should be established in all samples to characterize dispersion. Therefore, the applied voltage should be calculated as\textsuperscript{15} $V_G = V_{FB} + E_{ox} \times CET$, where $CET$ is the capacitance equivalent thickness, $E_{ox}$ the equivalent electric field across the oxide, and $V_{FB}$ the flatband voltage of the samples. For our particular set of samples, an estimation of $CET$ through the expression $CET = \varepsilon_{{SiO}_2} \times A / C_{acc}$ (with $\varepsilon_{{SiO}_2}$ the permittivity of SiO$_2$, $A$ the device area, and $C_{acc}$ the capacitance measured in accumulation) yields values for $CET$ of 6.78 nm, 7.33 nm, 7.13 nm, and 7.04 nm for sets of samples FGA-#1, O2A-#2, AE-FGA-#3, and AE-#4, respectively. Although there is a spread between sets (particularly for O2A-#2), considering the hyperbolic dependence of dispersion with $CET$,\textsuperscript{15} for values larger than 4 nm, the error induced in the extraction of frequency dispersion is negligible if the measurements are performed at constant $V_G - V_{FB}$ instead of constant $E_{ox}$.

In Fig. 3, it is possible to observe that all samples follow the same trend but two groups can be identified: those with FGA treatment (FGA-#1 and AE+FGA-#3) show a smaller absolute value of dispersion than those without it (O2A-#2 and AE-#4). Additionally, air exposed samples are more sensitive to FGA effects, showing the stronger reduction on the magnitude of the frequency dispersion: 3.79% per decade for AE-#4 versus 2.43% per decade for AE+FGA-#3 (around 1.5 times smaller) compared to 3.74% per decade for O2A-#2 versus 2.71% per decade for FGA-#1 (around 1.3 times smaller).

From MFCV curves, it was possible to address in a general manner the effects of the fabrication procedure on the relative quality of the samples. FGA provides an effective improvement of both high-\textit{k}/III–V interface quality (reduced dispersive behavior toward inversion and smaller weak inversion humps) and BT response (reduced $C_{acc}$ frequency dispersion) when probed in the AC domain.

### B. C-V hysteresis measurements under dynamic stress

To further compare charge trapping for these sets of samples, it is important to assess the dependence of charge trapping effects on band bending. Vais \textit{et al.} reported in Refs. 18 and 19 the interpretation of the hysteresis width as a function of oxide trap energy distribution throughout the bandgap of the semiconductor. In this regard, while frequency dispersion in accumulation is an indicator of charge exchange from the semiconductor with available states (i.e., BTs) within energies closely around the Fermi level, C-V hysteresis is an indicator of the trapping characteristics throughout a large section of the bandgap,\textsuperscript{15} where the total trapped charge ($Q_{trapped}$) in the two-way C-V measurement relates to the hysteresis width through the expression $Q_{trapped} = V_{hys} \times C_{ox} / q$, where $C_{ox}$ is the oxide capacitance and $q$ is the electron charge. Due to this different interpretation, it is important to assess the trapping behavior of our samples in terms of the C-V hysteresis.

Two-way C-V sweeps (in back trace mode) were performed stressing the sample dynamically into accumulation. For each complete loop, the final voltage in accumulation, $V_{stress}$, was increased by 0.25 V from the previous one, while the initial voltage of the sweep in inversion, $V_{start}$, was held constant throughout a total of 16 cycles (i.e., 4 V total increase in $V_{stress}$). The probing frequency was fixed at 500 kHz to minimize the contribution of $D_{it}$ and the impact of serial inductance of the cables. Minimum delay between sweeps is fixed by the instrument at ~100 ms. The resulting measurements can be observed in Fig. 4 for all sets of samples. It should be pointed out that, given the influence of the initial and final voltages of the sweep on the C-V hysteresis,\textsuperscript{18,19} $V_{start}$ and the initial $V_{stress}$ were chosen for each sample such that the applied stress is equal among samples at each corner of the sweep, i.e., the same voltage referred to $V_{FB}$. At this point, it is worth to mention that $V_{FB}$ displacement during stress sweeps can have further impact on the effective stress field between sweeps. However, this shift is considerably small compared to the absolute values of stress.

![FIG. 4. C-V dynamic stress sweeps toward accumulation at f = 500 kHz for the four sets of samples: As$_2$ decap + FGA (FGA-#1) (a), As$_2$ decap + O$_2$ anneal (O2A-#2) (b), air exposed + FGA (AE+FGA-#3) (c), and air exposed without annealing (AE-#4) (d).](image-url)
FIG. 5. C-V hysteresis loop width $dV_{hys}$ vs. relative stress voltage $V_{stress} - V_{FB}$. The inset shows the same data in terms of $Q_{trapped}$ vs. equivalent oxide field $E_{ox}$, filled markers represent samples that underwent FGA, while unfilled markers correspond to an O2 anneal or no anneal whatsoever.

FIG. 6. Typical I-V Characteristics for the 4 sets of samples.
In Fig. 7, numbered dashed arrows are guides to the eye for the effects of annealing on different samples. Arrows 1 and 2 show the effects of FG and O2 anneals on As2 decapped samples, while arrow 3 shows the impact of FGA on air exposed samples. FGA clearly results in a reduction in $C_{acc}$ frequency dispersion accompanied by an increase in hysteresis for our sets of samples. Although Lin et al. showed a reduction of both indicators for certain temperatures of the FGA process (see triangle markers on a gray scale with dashed arrows number 4 indicating rising FGA temperature in Fig. 7), no clear trend can be found between them on individual, differently processed sets of samples, raising questions regarding the physical origin of each characteristic. In fact, a steep rise in hysteresis suggests that the net amount of traps involved per unit increase in band bending is larger throughout the bandgap. Ergo, one would expect a higher frequency dispersion accompanying larger C-V hysteresis. This is clearly not the case for most of the samples that can be found in the literature. Results by Fu et al. (see diamond markers and dashed arrow number 5 between them in Fig. 7) showed a strong decrease in C-V hysteresis after FGA, with a slight reduction of frequency dispersion, adding up to the difficulty of tracing a clear correlation between these two quality indicators. It should be pointed out that these samples are fabricated on (110) InGaAs substrates, where the nucleation and growth of Al2O3 can produce different distribution of defects throughout the oxide and the bandgap.

This discussion highlights the impact of FGA on the C-V hysteresis of the sample, although there is a strong lack of correlation between widely accepted $N_{bt}$ indicators. In this framework, while frequency dispersion probes only those defects located around the Fermi level, dynamic stress sweeps in hysteresis measurements reveal the full defect profile throughout the bandgap.

In Fig. 7, numbered dashed arrows are guides to the eye for the effects of annealing on different samples. Arrows 1 and 2 show the effects of FG and O2 anneals on As2 decapped samples, while arrow 3 shows the impact of FGA on air exposed samples. FGA clearly results in a reduction in $C_{acc}$ frequency dispersion accompanied by an increase in hysteresis for our sets of samples. Although Lin et al. showed a reduction of both indicators for certain temperatures of the FGA process (see triangle markers on a gray scale with dashed arrows number 4 indicating rising FGA temperature in Fig. 7), no clear trend can be found between them on individual, differently processed sets of samples, raising questions regarding the physical origin of each characteristic. In fact, a steep rise in hysteresis suggests that the net amount of traps involved per unit increase in band bending is larger throughout the bandgap. Ergo, one would expect a higher frequency dispersion accompanying larger C-V hysteresis. This is clearly not the case for most of the samples that can be found in the literature. Results by Fu et al. (see diamond markers and dashed arrow number 5 between them in Fig. 7) showed a strong decrease in C-V hysteresis after FGA, with a slight reduction of frequency dispersion, adding up to the difficulty of tracing a clear correlation between these two quality indicators. It should be pointed out that these samples are fabricated on (110) InGaAs substrates, where the nucleation and growth of Al2O3 can produce different distribution of defects throughout the oxide and the bandgap.

This discussion highlights the impact of FGA on the C-V hysteresis of the sample, although there is a strong lack of correlation between widely accepted $N_{bt}$ indicators. In this framework, while frequency dispersion probes only those defects located around the Fermi level, dynamic stress sweeps in hysteresis measurements reveal the full defect profile throughout the bandgap.
show the resulting C-V plots for these experiments. Stress voltage, referred to as $V_{FB_{\text{st}}} $, was set to 3.4 V, and successive C-V loops were measured with stress times of 5, 10, 30, 60, 300, and 1000 s at the fixed stress voltage. Large quiescent times (>10 s) with no applied voltage elapsed between sweeps to minimize the contribution of previous stress cycles, taking advantage of the relatively fast recovery of trapped charge in these type of stacks, with exponential or cycles, taking advantage of the relatively fast recovery of times ($\tau_{1}$ = 10 s) with no applied voltage elapsed between sweep (forward curve displaces to higher voltages). Meanwhile, air exposed, non-FG annealed samples show very slight variations, in both $V_{FB}$ and $V_{Hys}$, with each stress cycle.

These results are observed more clearly in Figs. 8(c) (set FGA-#1) and 8(d) (set AE-#4), by plotting the hysteresis loop width and the $V_{FB}$ (both calculated with the same criteria as in dynamic stress experiments) as a function of the stress time of each consecutive cycle. Calculated values confirm the trends observed in the C-V plots: samples from set FGA-#1 show an increase on the hysteresis of ~250 mV and on the $V_{FB}$ of ~130 mV, while those from set AE-#4 show very small increase in the hysteresis of ~35 mV and decrease in the flatband voltage of ~30 mV. This clearly shows that the charge trapping effects that lead to C-V hysteresis are strongly time and DC bias dependent and, in our samples, FGA treatment increases the C-V hysteresis while reducing the frequency dispersion. This strong dependence with stress time evidences different kinetics for the charge trapping mechanisms. Moreover, the speed of the voltage sweep, the quiescent time between sweeps, and the stress time in the corners of the sweep must be carefully defined and accounted for when characterizing C-V hysteresis loops, as the obtained results can be greatly affected by a change on these conditions, especially when extracting $N_{0}$ values.

The unfilled markers show an extra measurement of the $V_{Hys}$ and $V_{FB}$ performed with the minimum stress time in accumulation after all stress cycles had been performed. This way, permanent (long term) effects after stress can be separated from recoverable variations after quiescent time without applied bias. Interestingly, while samples from set AE-#4 show negligible alterations after the experiment ($V_{FB}$ decreases around 20 mV, $V_{Hys}$ does not increase), those from set FGA-#1 indicate an increase in $V_{FB}$ of ~130 mV, up to a very similar value as the one measured during the final stress sweep. On the other hand, and taking into account this increase in $V_{FB}$, the measured hysteresis does not change after a clear degradation has occurred. This allows one to separate stress related damage from C-V hysteresis charge trapping. It should be noted that this is not an artifact of measurement uncertainty, because as our measurements are performed without disconnecting the device, the only source of uncertainty is one of the instruments, hence the error bars are well within the size of the plotted markers.

It might be argued that the effects of $V_{FB}$ displacement during the stress experiment would reduce the effective applied voltage ($V_{G} - V_{FB}$) between stress runs, mainly for FGA-#1 samples. This reduction is roughly ~4% for the final stress run [see maximum $V_{FB}$ shift in Fig. 8(c)] and the impact on the starting sweep voltage ($V_{FB} - V_{start}$) is negligible considering that hysteresis effects toward negative voltages are considerably weaker in these stacks (results not shown), as also shown in other works. However, to evaluate the impact of such $V_{FB}$ increase, sweeps with stress times of 1000, 300, and 60 s were performed on individual, fresh FGA-#1 samples. Hysteresis was measured considering the $V_{FB}$ extracted for the fresh condition of each sample (which was 0.65 V for all measured samples). Measurement results are included in Fig. 8(c) as half-filled markers, showing higher hysteresis values than for the stress results extracted from a single sample. This difference between hysteresis values can be attributed to the flatband increment experienced by the stressed samples, highlighting the fact that the overall impact of previous cumulative stress does not alter the interpretation of hysteresis results. Moreover, samples stressed from the fresh condition showed similar $V_{FB}$ deviations (~130 mV) and $V_{Hys}$ for the post-stress hysteresis sweep measured from the resulting $V_{FB}$ (results not superimposed for the sake of clarity). It is worth mentioning that although it is clear that the time acceleration factor, e.g., for a power law fit of the $V_{hys}$ data, is larger for fresh samples in Fig. 8(c) (half-filled markers), the trend and the interpretation of the results remain the same. However, when not accounted for, the non-recoverable $V_{FB}$ increase can result in an overestimation of the extracted trapped charge from the C-V hysteresis cycle width.

On our experimental conditions, all the defects involved in the charge buildup that results in hysteretic behavior are quickly, fully recovered when the sample is not under stress, which indicates that the defects involved have short emission times compared to the time between sweeps. On the other hand, $V_{FB}$ increase is an indicator of the permanent (non-recoverable without applied bias) degradation of the sample. This degradation is also noted in the inset of Figs. 8(a) and 8(b), where the normalized $G_{p}/A_{\text{dev}}$ peak, with $A$ being the device area, $G_{p}$ the parallel conductance, and $\omega$ the angular frequency of the AC signal, shows an increase in magnitude, a displacement to higher voltages in FG annealed samples, and only small variations in air exposed ones. This alteration can be linked to an increase of $D_{it}$ after stress. To verify this, post-stress MPCV curves were obtained for the samples under study in order to extract an estimation of $D_{it}$.

Figure 9(a) shows pre- and post-stress $D_{it}$ calculations for both sets of samples under study, obtained by the Castagné-Vapaille (high frequency/low frequency) method. It should be pointed out that although this method at room temperature may underestimate the value of $D_{it}$ for III–V semiconductors at energies close to the band edges, it is widely accepted in the literature to quantitatively compare the $D_{it}$ around mid-gap between differently fabricated samples. While no modifications can be observed for sample AE-#4, sample FGA-#1 shows a clear increase in $D_{it}$ around the mid-gap (i.e., depletion). This effect has been observed in similar samples and can be attributed to hydrogen depassivation effects under applied field. Ergo, the CVS resulted in the formation of interface defects around...
the mid-gap of the semiconductor, and $V_{FB}$ variations can be attributed to these states. It should be pointed out that these defects do not influence the capacitance frequency dispersion in accumulation nor the Fermi level movement toward the inversion region (obtained from $G_p$ maps, results not shown). Additionally, they do not affect the C-V hysteresis characteristics of the MOS stack when stressed at constant voltage in accumulation, as shown by the unfilled and half-filled markers in Figs. 8(c) and 8(d). This can be observed as the unfilled markers, which represent the hysteresis measurements after all stress cycles, show great coincidence with the hysteresis measured after the first stress cycle. Moreover, the $C_{acc}$ frequency dispersion shows negligible variations after the stress cycles as can be observed in Fig. 9(b), which indicates that there were no considerable alterations to the overall $N_h$ after the experiments, in accordance to previously reported results.\(^{20}\) Although interface defect hydrogen deactivation is supported by an increase in $D_{it}$ and $V_{FB}$ after stress as shown in previous works,\(^{21,34}\) it cannot be held accountable for the hysteretic behavior in FGA samples, as our results clearly indicate that hysteresis is not affected by permanent degradation after CVS.

It arises from these measurements that, although C-V hysteresis and $C_{acc}$ dispersion with frequency are ascribed to the same type of defects,\(^{12,17,18,21,33}\) there is a strong lack of correlation between these two indicators showing that C-V hysteresis involves trapping mechanisms with considerably different kinetics. $C_{acc}$ dispersion with frequency can be interpreted as an AC indicator of carrier-trap interaction around the Fermi level (with emission and capture times shorter than the period of the AC signal) and, despite the strong movement of the Fermi level into the conduction band in InGaAs-channel devices biased into accumulation,\(^{7}\) it is most often reported for a single $E_{acc}$. C-V hysteresis, on the other hand, holds a strong dependence on the DC state of the sample (probes defects located all the way up to the Fermi level) and on the stress time under applied bias (involved defects with large capture times). Although the exact location of the traps into the oxide cannot be accurately determined, defects with high activation energies for capture and relaxation may not contribute to dispersion but can be involved in C-V hysteresis when the stress time or bias is increased.\(^{36}\)

This trapping behavior has also been largely observed in CVS current versus time (I-t) characteristics of high-k dielectrics in both metal-insulator-semiconductor (MIS)\(^{49}\) and also in metal-insulator-metal (MIM)\(^{50}\) structures. The observed effect is a progressive current reduction that is usually modeled through Curie-von Schweidler law\(^{21}\) and ascribed to electron trapping.\(^{49}\) This phenomenon is observed in Fig. 10 that shows the current transients under CVS for fresh samples of sets FGA-#1 and AE-#4. Voltage stress was fixed at 5 V referred to the $V_{FB}$ of each sample in order to obtain currents high enough to be above the leakage of the setup but low enough to prevent the fast degradation of the oxides and second order effects such as hot carriers. Samples were stressed during 1000 s without showing evidence of breakdown. Both samples show very similar currents under this condition, between 25 pA (0.3 $\mu$A/cm$^2$) and 30 pA (0.4 $\mu$A/cm$^2$). The highlight of this figure is the clear difference on the charge trapping dynamics between the two sets of samples: FG annealed samples show a negative slope in the current transient, while air exposed samples experience a current increase from the very beginning of the CVS experiment, ergo showing that the trapping dynamics and the overall distribution of the electric field in the stack under stress conditions is considerably different between these sets of samples.

Interestingly, in Ref. 49, the electron trapping leading to current decay with time was linked to border traps in samples with similar I-t characteristics to those of FGA-#1 samples. This interpretation cannot explain the observed behavior in our sets of samples. Those samples with a large dispersion (i.e., large BT density, AE-#4) do not show trapping behavior but a typical stress induced leakage current (SILC) behavior.\(^{52}\) This can be attributed to a high density of neutral electron traps in the oxide that act as “stepping stones” for trap assisted tunneling, which is consistent with large BT density. On the other hand, before showing any signs of SILC increase (for the stress times used in this work), FGA-#1 samples show a slow activation of defects (electron trapping) that reconfigures the band bending in the structure,\(^{53}\) leading to a strong instability that is recoverable in relatively short times. This can be linked to a large density of bulk oxide traps created during FGA, where the MG/high-k interface may play a role too.\(^{35,54}\)
For the purposes of this work, these measurements highlight the strong difference in the trapping dynamics of differently processed samples. It is shown that BT density estimated by means of frequency dispersion cannot explain the trapping effects observed on the I-t characteristics of the samples. On the other hand, oxide traps involved in C-V hysteresis are consistent with I-t characteristics inducing instabilities that are both DC stress and time dependent, where not only the high-k/InGaAs interface plays a role but also the MG/high-k side must be taken into account, along with the full kinetics of the defect centers involved. The lack of correlation between frequency dispersion and C-V hysteresis/I-t characteristics points out that these indicators must be individually accounted for and not generalized as two effects with the same origin, solely linked to near high-k/III–V interface effects, i.e., border traps. Although revealing the full nature of the defects involved is challenging, further study of the full kinetics of trapping/detrapping processes in these stacks is worthy in order to fully explain the impact of the fabrication process on their final electrical characteristics, in the pursuit of highly reliable III–V electronics.

VI. SUMMARY AND CONCLUSIONS

In this paper, the oxide defect indicators of MOS structures were measured and compared between differently fabricated sets of samples, mainly studying the effects of FGA on the electrical characteristics. Accumulation capacitance dispersion with frequency and C-V hysteresis were compared between samples with and without interfacial native oxide layers (As2 decapped and air exposed samples, respectively) and after different annealing conditions (forming gas, oxygen, or no annealing). The results clearly show a strong disconnection between these two indicators among the evaluated samples, where FGA increases the hysteresis and reduces the dispersion for all cases. Additionally, the effects of CVS on \( D_{\text{it}} \), C-V hysteresis, \( V_{\text{FB}} \), and frequency dispersion were addressed. Results showed that C-V hysteresis loop width is strongly dependent on the stress time in accumulation for FGA samples, thus suggesting that the trapping phenomena involved are both voltage- and time dependent and that trapped charge is quickly recovered when no bias is applied. Meanwhile, dispersion is constant throughout and after stress measurements for both FGA and non-FGA samples. Moreover, defect depassivation at the interface cannot explain the hysteretic behavior of FGA samples, as shown by the fact that permanent (non-recoverable in short-term) degradation after constant voltage stress has no effect on the C-V hysteresis width, adding evidence toward the interpretation of C-V hysteresis involving a set of defects with slower kinetics than those responsible for accumulation capacitance frequency dispersion. This is further supported by current-time characteristics at constant applied voltage, which show clear signs of negative charge trapping in FGA samples.

In a general manner, while accumulation capacitance frequency dispersion is an AC dependent figure of quality, hysteresis is the result of a DC driven phenomenon, so they must be carefully separated as they involve different defect kinetics across the MG/high-k/III–V stacks and not generalized as two \( N_{\text{it}} \) estimators. Moreover, experimental conditions for C-V hysteresis measurements must be carefully defined as sweep speed, corner voltages, and stress times directly affect the extracted loop width, which can lead to considerable differences when used to extract \( N_{\text{it}} \). Further investigation considering the full kinetics of the defects involved in each phenomenon would be worthy in the pursuit of an optimal trade-off between reliability and device performance.

ACKNOWLEDGMENTS

This work was funded by the following Argentinean institutions: MINCyT under contracts PICT2013/1210 and PICT2016/0579, CONICET under project PIP-11220130100077CO and UTN.BA under projects EIUTIBA4395TC3, CCUTIBA4764TC, and MATUNBA4936. The authors also acknowledge support from Semiconductor Research Corporation through the Non-Classical CMOS Research Center (Task ID 1437.008), the Stanford Initiative in Nanoscale Materials and Processes (INMP), and the US-Israel Binational Science Foundation. Fabrication of the samples used in this study was performed at the Stanford Nano Shared Facilities (SNSF).

1J. A. del Alamo, Nature 479, 317 (2011).
2R. Englet-Herbert, Y. Hwang, and S. Stemmer, J. Appl. Phys. 108, 124101 (2010).
3G. Brammertz, A. Alian, D.-H.-C. Lin, M. Meuris, M. Caymax, and W.-E. Wang, IEEE Trans. Electron Devices 58, 3890 (2011).
4K. Cherkaoui, E. O’Connor, S. Monaghan, R. D. Long, V. Dijan, A. O’Mahony, R. Nagle, M. E. Pemble, and P. K. Hurley, ECS Trans. 28, 181 (2010).
5J. Franco, A. Alian, B. Kaczer, D. Lin, T. Ivanov, A. Pourghaderi, K. Martens, Y. Mols, D. Zhou, N. Waldron, S. Sionccke, T. Kauerauf, N. Collaert, A. Thean, M. Heyns, and G. Groeseneken, in 2014 IEEE International Reliability Physics Symposium (IEEE, 2014), pp. 6A.2.1–6A.2.6.
6J. Robertson and R. M. Wallace, Mater. Sci. Eng. R: Rep. 88, 1 (2015).
7J. Robertson, Appl. Phys. Lett. 94, 152104 (2009).
8J. R. Weber, A. Janotti, and C. G. Van de Walle, J. Appl. Phys. 109, 033715 (2011).
9E. Simoen, D. H.-C. Lin, A. Alian, G. Brammertz, C. Merckling, J. Miard, and C. Claey, IEEE Trans. Device Mater. Reliab. 13, 444 (2013).
10I. Krylov, D. Ritter, and M. Eizenberg, J. Appl. Phys. 118, 084502 (2015).
11S. Stemmer, V. Cherbottanna, and S. Rajan, Appl. Phys. Lett. 100, 233510 (2012).
12C. Dou, D. Lin, A. Vais, T. Ivanov, H.-P. Chen, K. Martens, K. Kakushina, H. Iwai, Y. Taur, A. Thean, and G. Groeseneken, Microelectron. Reliab. 54, 746 (2014).
13R. V. Galatage, D. M. Zhermokletov, H. Dong, B. Brennan, C. L. Hinkle, R. M. Wallace, and E. M. Vogel, J. Appl. Phys. 116, 014504 (2014).
14I. Krylov, D. Ritter, and M. Eizenberg, J. Appl. Phys. 117, 174501 (2015).
15A. Vais, J. Franco, K. Martens, D. Lin, S. Sionccke, V. Putcha, L. Nyns, J. Maes, Q. Xie, M. Givens, F. Tang, X. Jiang, A. Mocuta, N. Collaert, A. Thean, and K. De Meyer, IEEE Electron Device Lett. 38, 318 (2017).
16Y. Yuan, B. Yu, J. Aln, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, and Y. Taur, IEEE Trans. Electron Devices 59, 2100 (2012).
17A. Vais, H.-C. Lin, C. Dou, K. Martens, T. Ivanov, Q. Xie, F. Tang, M. Givens, J. Maes, N. Collaert, J.-P. Raskin, K. DeMeyer, and A. Thean, Appl. Phys. Lett. 107, 053504 (2015).
18A. Vais, J. Franco, H.-C. Lin, N. Collaert, A. Mocuta, K. De Meyer, and A. Thean, Appl. Phys. Lett. 107, 223504 (2015).
19A. Vais, J. Franco, D. Lin, V. Putcha, S. Sionccke, A. Mocuta, N. Collaert, A. Thean, K. De Meyer, J. Appl. Phys. 121, 144504 (2017).
20F. Palumbo, S. Pazos, F. Aguirre, R. Winter, I. Krylov, and M. Eizenberg, Solid-State Electron. 132, 12 (2017).
21 K. Tang, F. R. M. Palumbo, L. Zhang, R. Droopad, and P. C. McIntyre, ACS Appl. Mater. Interfaces 9, 7819–7825 (2017).

22 J. Q. Lin, S. J. Lee, H. J. Oh, G. Q. Lo, D. L. Kwong, and D. Z. Chi, IEEE Electron Device Lett. 29, 977 (2008).

23 Y.-C. Fu, U. Peralagu, D. A. J. Millar, J. Lin, I. Povey, X. Li, S. Monaghan, R. Droopad, P. K. Hurley, and I. G. Thayne, Appl. Phys. Lett. 110, 142905 (2017).

24 T. Hoshii, S. Lee, R. Suzuki, N. Taoka, M. Yokoyama, H. Yamada, M. Hata, T. Yasuda, M. Takenaka, and S. Takagi, J. Appl. Phys. 112, 073702 (2012).

25 K. Tang, A. C. Meng, R. Droopad, and P. C. McIntyre, ACS Appl. Mater. Interfaces 8, 30601 (2016).

26 J. Ahn, T. Kent, E. Chagarov, K. Tang, A. C. Kummel, and P. C. McIntyre, Appl. Phys. Lett. 103, 071602 (2013).

27 J. Ahn, B. Shin, and P. C. McIntyre, ECS Trans. 45, 183 (2012).

28 E. J. Kim, E. Chagarov, J. Cagnon, Y. Yuan, A. C. Kummel, P. M. Asbeck, S. Stemmer, K. C. Saraswat, and P. C. McIntyre, J. Appl. Phys. 106, 124508 (2009).

29 E. J. Kim, L. Wang, P. M. Asbeck, K. C. Saraswat, and P. C. McIntyre, Appl. Phys. Lett. 96, 012906 (2010).

30 H.-S. Kang, M. Siva Pratap Reddy, D.-S. Kim, K.-W. Kim, J.-B. Ha, Y. S. Lee, H.-C. Choi, and J.-H. Lee, J. Phys. D Appl. Phys. 46, 155101 (2013).

31 F. Kersten, A. Schmid, S. Bordihn, J. W. Müller, and J. Heitmann, Energy Proc. 38, 843 (2013).

32 V. Djara, K. Cherkaoui, M. Schmidt, S. Monaghan, E. O’Connor, I. M. Povey, D. O’Connell, M. E. Pembble, and P. K. Hurley, IEEE Trans. Electron Devices 59, 1084 (2012).

33 J. Lin, S. Monaghan, K. Cherkaoui, I. M. Povey, B. Sheehan, and P. K. Hurley, J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. 31, 030604 (2013).

34 K. Martens, C. O. Chai, G. Brummertz, B. De Jaeger, D. Kuzum, M. Meuris, M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, IEEE Trans. Electron Devices 55, 547 (2008).

35 R. Winter, J. Ahn, P. C. McIntyre, and M. Eizenberg, J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. 31, 030604 (2013).

36 H. B. Do, Q. H. Luc, M. T. H. Ha, S. H. Huynh, T. A. Nguyen, Y. C. Lin, and E. Y. Chang, AIP Adv. 7, 085208 (2017).

37 S. Kar, High Permittivity Gate Dielectric Materials (Springer, Berlin, Heidelberg, 2013).

38 B. Shin, J. B. Clemens, M. A. Kelly, A. C. Kummel, and P. C. McIntyre, Appl. Phys. Lett. 96, 252907 (2010).

39 R. Winter, J. Ahn, P. C. McIntyre, and M. Eizenberg, J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct. 31, 030604 (2013).

40 K. Martens, C. O. Chai, G. Brummertz, B. De Jaeger, D. Kuzum, M. Meuris, M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, IEEE Trans. Electron Devices 55, 547 (2008).

41 R. Engel-Herbert, Y. Hwang, and S. Stemmer, Appl. Phys. Lett. 97, 062905 (2010).

42 R. M. Wallace, P. C. McIntyre, J. Kim, and Y. Nishi, MRS Bull. 34, 493 (2009).

43 A. Vais, K. Martens, D. Lin, N. Collaert, A. Mocuta, K. DeMeyer, and A. Thean, Microelectron. Eng. 147, 227 (2015).

44 J. Lin, S. Monaghan, K. Cherkaoui, I. M. Povey, E. O’Connor, B. Sheehan, and P. K. Hurley, in 2014 IEEE International Integrated Reliability Workshop Final Report (IIRW) (IEEE, 2014), pp. 36–40.

45 F. L. Aguirre, S. M. Pazos, F. Palumbo, I. Krylov, and M. Eizenber, in 32nd Symposium on Microelectronics Technology and Devices (SBMicro) (IEEE, Fortaleza, Brasil, 2017).

46 V. Djara, M. Sousa, N. Dordevic, L. Czomomaz, V. Deshpande, C. Marchiori, E. Uccelli, D. Caimi, C. Rossel, and J. Fompeyrine, Microelectron. Eng. 147, 231 (2015).

47 F. Palumbo and M. Eizenberg, J. Appl. Phys. 115, 014106 (2014).

48 Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices (Cambridge University Press, 2009), p. 656.

49 S. Yoshida, D. Lin, A. Vais, A. Alian, J. Franco, S. El Kazzi, Y. Mols, Y. Miyamani, M. Nakazawa, N. Collaert, H. Watanabe, and A. Thean, Appl. Phys. Lett. 109, 172101 (2016).