Physics Based Modelling of Short-Channel Nanowire MOSFET

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Abstract. A modelling framework for short channel nanowire (NW) MOSFETs that covers a wide range of operating conditions is presented. The device electrostatics in the subthreshold regime is dominated by the inter-electrode capacitive coupling, which, in the case of double gate (DG) devices, is analyzed in terms of conformal mapping techniques. Previously, we have shown that these results can also be successfully applied to the NW MOSFET, by performing an appropriate mapping to compensate for the difference in gate control between the two devices. Near and above threshold, the influence of the electronic charge is taken into account in a precise, self-consistent manner by combining suitable model expressions with Poisson’s equation. The models are verified by comparison with numerical device simulations.

1. Introduction
The nanowire (NW) MOSFET is considered a strong contender for replacing classical MOSFETs in next generation CMOS technology. This device has a cylindrical gate electrode giving the device a superior gate control of the conducting channel. This helps to reduce debilitating short-channel effects, such as drain induced barrier lowering (DIBL) and excessive sub-threshold swing.

A modelling framework for short-channel NW MOSFETs that covers a wide range of operating conditions has been developed. Near and above threshold, the influence of the electronic charge on the electrostatics is taken into account in a precise, self-consistent manner by combining suitable model expressions with the 3D Poisson’s equation in the device body. For finite drain voltages, the self-consistency also extends to a calculation of the quasi-Fermi potential and the drain current. In strong inversion, where the electronic charge dominates the device electrostatics, the device behaviour approaches that of long-channel devices.

The NW device considered has gate length $L=25$ nm, silicon substrate radius $r_{si}=6$ nm, insulator thickness $t_{ox}=1.6$ nm and insulator relative dielectric constant $\varepsilon_{ox}=7$. The doping density of the $p$-type silicon body is $1 \times 10^{15}$ cm$^{-3}$. As gate material, we selected a midgap metal with the work function 4.53 eV (corresponding to that of molybdenum). Idealized Schottky contacts with work function of 4.17 eV (corresponding to that of $n^+$ silicon) are assumed for the source and drain. This ensures equipotential surfaces on all the device contacts. Note the device dimensions considered are such that a classical treatment of the electron distribution is warranted. For simplicity, we also assume a drift-diffusion transport mechanism with a constant mobility.
2. Sub-threshold
In devices with nanoscale gate length, the device electrostatics in the sub-threshold regime is dominated by capacitive coupling between the gate, source and drain electrodes. Previously, we have shown that in the double-gate (DG) MOSFET structure, the two-dimensional (2D) potential distribution within the device body can be analytically determined by conformal mapping techniques based on Laplace’s equation. Although the NW MOSFET is a 3D structure, we have further shown that the DG MOSFET results can be successfully applied to the central, longitudinal cross-sections of the NW structure as well, by performing an appropriate device scaling to compensate for the difference in gate control between the two devices [1-3]. This mapping is described in terms of the characteristic longitudinal field penetration lengths from source and drain of the DG and NW MOSFET geometries.

Figure 1 illustrates the improved gate control obtained by the cylindrical gate all around structure of the NW compared to the DG. Under identical biasing conditions, we observe a considerably flatter potential distribution in the centre of the NW device compared to the DG. The device electrostatics and the drain current calculated from this NW model show excellent agreement with numerical simulations in the sub-threshold regime [2-3].

![Figure 1. Modelled potential distribution in DG (left) and NW device (right) in the sub-threshold regime ($V_{GS}=V_{DS}=0$).](image)

3. Near and above threshold
Near and above threshold, the carrier contribution to the body potential cannot be neglected. In this case, Poisson’s equation is divided into two superimposed parts, the first of which is the 2D inter-electrode capacitive coupling found by the mapping technique as described above. The second part accounts for the electrostatic effects associated with the charge carriers which must be derived in a self-consistent manner in agreement with Poisson’s equation.

Within the present framework, the modelling of the NW proceeds by first establishing the potential distributions along the radial gate-to-gate (G-G) and the axial drain-to-source (D-S) symmetry lines. First, it is required to initialize the quasi-Fermi potential distribution from D-S. We have used a set of two linear trial functions with a value at the device centre equal to, $V_{F%S}=0.4V_{DS}$.

Figure 2 illustrates above-threshold potential profiles along the G-G symmetry line for different biasing when an optimized quasi-Fermi level has been established. At low drain voltages, $V_{DS}=0.1V$, the 1D solution gives excellent correspondence with numerical simulations. When $V_{DS}$ is increased to 0.5V, we observe a small deviation (< 5mV) in the centre potential. However, the deviation decreases towards the Si-SiO$_2$ interface, which is the region with the highest density of mobile charge and most significant when it comes to calculating the current.
Figure 2. Potential profile along the radial gate-to-gate symmetry line for $V_{DS}=0.1V$ (left) and $V_{DS}=0.5V$ (right). Lines are modelled results and symbols are numerical simulations (Silvaco Atlas).

The potential along the D-S symmetry line is modelled by two exponential trial functions for the source and drain side respectively. Close to the drain and source electrodes, we apply the 1D Poisson’s equation to estimate the D-S potential a small distance, $\delta_{D,S}$, from the drain and source electrodes. Hence, the parameters of the D-S trial functions are determined from the boundary conditions at the device centre (potential, $\phi_c$, and an estimate of its first derivative) and the potential and its derivative at $\delta_{D,S}$. The left plot in figure 3 compares the potential profiles along the D-S axis obtained with the model and with numerical simulations.

The potential along the Si-SiO$_2$-interface is modelled by a set of trial functions. The interface potential terminates at the idealized drain and source Schottky contact corners, with values equal to the respective electrode potentials and with an electric field that approaches infinity. The potential profile close to these corners is modelled by a square-root function. The central part of the interface potential is modelled by a parabola whose parameters are determined by the level of $V_{DS}$ and values estimated by the long channel limit. The right plot in figure 3 illustrates the interface potential for different drain biasing obtained after a few iterations which also involve the calculation of the drain current and the quasi-Fermi potential distribution (see below).

In the above procedure, a number of radial G-G cutlines are also calculated. By numerical integration along the G-G cutlines, we can estimate the inversion charge density as a function of $x$. The inversion charge is used to find estimates the drift diffusion current and the quasi-Fermi potential distribution in each iteration [1]. Normally, only two to three iterations are needed for a satisfactory accuracy.

To the left in figure 3, the modelled quasi-Fermi potential is compared with numerical simulations. The drift diffusion current is plotted in figure 4.

4. Conclusion
We have developed a precise, compact modelling framework for calculating the electrostatics as well as the drain currents in nanoscale nanowire MOSFETs. The modelling is based on conformal mapping techniques and a self-consistent analysis of the energy barrier topography, that include the effects of both the inter-electrode capacitive coupling and the presence of inversion electrons. Short-channel effects, including DIBL, are inherently contained in this analysis, and no adjustable parameters are used. The modelling framework covers the full range of bias voltages from subthreshold to strong inversion. Assuming a drift-diffusion transport mechanism, the drain current calculated from the present models and from numerical simulations (Silvaco Atlas) show excellent agreement.
Figure 3. Comparison of modelled and simulated (Silvaco Atlas) D-S potential profiles. The left plot illustrates the potential and quasi-Fermi level along the axial symmetry line. The right plot shows the potential profile along the Si-SiO₂ interface.

Figure 4. Comparison of modelled and simulated (Silvaco Atlas) drift-diffusion current.

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