Ku-band compact Wilkinson power divider based on multi-tap inductor technique in 65-nm CMOS

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Abstract: This paper presents a Ku-band compact Wilkinson power divider (WPD). The proposed WPD is realized by a multi-tap inductor with shunt capacitors to achieve low insertion loss, broadband isolation while minimizing chip area. Occupying only 188 × 116 μm², the proposed WPD achieves a measured insertion loss of less than 1 dB from 1 to 16 GHz. From 11 to 16 GHz, the measured isolation is better than 20 dB with input and output return losses higher than 16 and 21 dB, respectively.

Keywords: Wilkinson power divider, CMOS, phased array transceiver, millimeter wave

Classification: Integrated circuits

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1 Introduction

Wilkinson power divider (WPD) is widely used for signal dividing and combining in microwave and millimeter-wave circuits and systems [1, 2, 3, 4, 5, 6, 7]. It features high isolation and low insertion loss [8], which makes it essential in phased-array transceivers [3, 4, 5, 6, 7]. Traditional Ku-band WPDs, however, occupy relatively large area due to the long quarter-wavelength transmission lines (T-lines). Various techniques have been proposed to reduce the circuit area. For example, the defected ground structure (DGS) is proposed in

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[9] and the modified T-type impedance transformers (MTITs) are used in [10]. The π-section LC topology is used in [11] to realize a core chip size of 120 × 290 μm², but its operating frequency is limited by the cut-off frequency of LC ladder. While WPD using symmetric inductors with embedded capacitors technique [12] demonstrates broadband operation from 5.2 to 19.5 GHz, its isolation is relatively low. In addition, periodic synthesized T-lines [13] and complementary conducting strip (CCS) T-lines [14] are used to realize miniaturized WPDs. The former is still not as compact as lumped counterparts, and the latter suffers from relatively high insertion loss.

This letter presents a compact WPD in 65-nm CMOS. Multi-tap inductor technique is employed to reduce chip area while broadening bandwidth. From 11 to 16 GHz, the WPD achieves an isolation better than 20 dB with the insertion loss of less than 1 dB.

2 Design considerations

The conventional WPD is realized by quarter-wavelength T-lines. To reduce chip area, the T-line is implemented by n-section LC ladders (see Fig. 1). The cut-off frequency (ωₘ) is expressed as

\[ ωₘ = \frac{2}{√LC} \]  \hspace{1cm} (1)

where L and C are the unit inductance and capacitance of each section. Note that the values of L and C are inversely proportional to the number of sections (n). Therefore, to realize broadband operation, the number of LC sections should be sufficiently large.

Fig. 2 and Fig. 3 compare the chip area and performance of Ku-band WPDs designed by T-lines and LC networks. Fig. 2(a) shows a coplanar waveguide (CPW) based WPD, consuming a rather large physical dimension of 2244 × 74 μm². To ease the system layout floor-planning, folded CPW based WPD shown in Fig. 2(b) is preferred, but it still occupies large area. To reduce the chip area, 1-, 2- and 4-section LC networks (see Fig. 2(c) to (e)) are considered. According to the electromagnetic (EM) simulation results shown in Fig. 3, T-line based WPDs have relatively high insertion loss. As expected, the bandwidth of the LC-network based WPD increases with n. However, a larger n indicates that more inductors are needed, resulting in an increased dimension. Therefore, there is a trade-off between size and performance. In this work, the multi-tap inductor technique provides an effective solution.

![Fig. 1. Transmission line and its lumped element equivalent.](image-url)
3 Multi-tap inductor based Wilkinson power divider

Fig. 4 shows the proposed multi-tap inductor based WPD. The design of the power divider is described in the following subsections.

Fig. 4. The proposed WPD (a) layout (b) equivalent schematic.
3.1 Multi-tap inductor
The multi-tap inductor is realized with symmetric square shape (see Fig.4 (a)).
The inductor is implemented with top metal. The metal line width of 4 μm and
line spacing of 3 μm are chosen for self-resonate frequency consideration. It is
clear that the inductance of the inductor is determined by the inductance of its
metal lines and their mutual inductance between each other. The metal line
length determines the self-inductance. The mutual inductance, however, is
affected by both metal line length and the current carried by the metal line. Thus,
small adjustment of tap positions will make a relatively big change of the
inductance values. Moreover, the parasitics of interconnects between capacitors
and taps would degrade the signal. Based on these observations, the positions of
the taps 2’, 3’, and 4’ are co-optimized with the design of the inductor. For
simplicity, 1’ and 5’ are used to identify the start and end of the inductor. As the
multi-tap inductor is a 5-port network. The effective inductance \( L_i \) of each
sub-section is equal to the self-inductance plus the sum of the mutual inductances,
given by

\[
L_i = L_{s_{i'}j'} + \sum_{j=1,j\neq i}^{4} M_{ij}
\]

\( L_{s_{i'}j'} \) stands for the self-inductance of the sub-section between port \( i' \) and \( j' \) of the
multi-tap inductor. It can be calculated from the input impedance \( Z_{in} \) at port \( i' \)
with port \( j' \) grounded. From Thevenin’s theorem, \( Z_{in} \) can be expressed with Z
parameters as

\[
Z_{in} = Z(i', i') - \frac{Z(j', i')Z(i', j')}{Z(j', j') + Z_L},
\]

in which load impedance \( Z_L = 0 \) because port \( j' \) is grounded. Thus,

\[
L_{s_{i'}j'} = \frac{\text{Im} \left( Z(i', i') - \frac{Z(j', i')Z(i', j')}{Z(j', j')} \right)}{2\pi f}.
\]

\[
M_{ij} = \frac{(L_{s_{i'}k'} - L_{s_{i'}j'} - L_{s_{j'}k'})}{2}.
\]

\( M_{ij} \) is the mutual inductance between \( i^{th} \) and \( j^{th} \) sub-section inductors. Using (4)
and (5), the exact values of \( L_{s_{i'}j'} \) and \( M_{ij} \) can be extracted from the results of EM
simulations.

![Fig. 5. Inductance value of the multi-tap inductor, self-inductance values of
sub-section inductors and the mutual inductance values between sub-sections.](image-url)
Fig. 5 plots the total inductance value of the inductor \( L_T \), the sum of the four effective inductances \( L_{\text{sum}} \), the self-inductance values of sub-sections \( L_{12}, L_{23}, L_{34} \) and \( L_{45} \) and the mutual inductance values between sub-sections \( M_{12}, M_{13}, M_{23}, M_{14}, M_{24} \) and \( M_{34} \). As can be seen, at 13 GHz, \( L_{12} = 156 \) pH, \( L_{23} = 154 \) pH, \( L_{34} = 158 \) pH, \( L_{45} = 160 \) pH, \( M_{12} = 45 \) pH, \( M_{13} = 47 \) pH, \( M_{23} = 94 \) pH, \( M_{14} = 97 \) pH, \( M_{24} = 50 \) pH and \( M_{34} = 48 \) pH. According to (2), effective inductance \( L_1 = 345 \) pH, \( L_2 = 343 \) pH, \( L_3 = 347 \) pH and \( L_4 = 355 \) pH. Adding these four values yields 1.39 nH, agreeing with \( L_{\text{sum}} = L_T \). In Fig. 5, it can be seen that \( L_{\text{sum}} \) and \( L_T \) fall on the top of each other.

3.2 Design of the Wilkinson power divider

Fig. 4(a) shows the proposed compact WPD based on multi-tap inductor. It consists of two multi-tap inductors with six shunt capacitors, which is equivalent to 4-section LC ladders (see Fig. 4(b)). They are lumped equivalents of quarter wavelength transmission line of the WPD. The effective inductances \( L_1, L_2, L_3, L_4 \) and \( L_5 \) of about 340 pH satisfies the theoretically calculated value at the center frequency of 13 GHz. Consequently, by employing multi-tap inductor technique, 4-section LC networks are realized in a compact area (i.e., \( 188 \times 116 \) \( \mu \text{m}^2 \)) compared with 4-section cascaded LC structure (i.e., \( 134 \times 348 \) \( \mu \text{m}^2 \)). The values of shunt capacitors (i.e., \( C_1, C_2 \) and \( C_3 \)) are co-optimized with the inductors to satisfy the impedance transformation expression of LC network across broad bandwidth in Fig. 4(b)

\[
(((((2Z_o + sL_1)|| \frac{1}{sC_1}) + sL_2)|| \frac{1}{sC_2}) + sL_3)|| \frac{1}{sC_3}) + sL_4 = Z_o. \tag{6}
\]

And set to 83 fF to further improve the bandwidth. The isolation resistor is tuned to 105 \( \Omega \). The WPD is connected to probe pads through CPW T-lines. The pad capacitance of 20 fF is taken into account for impedance transformation to 50 \( \Omega \).

Thanks to the multi-tap inductor technique, the proposed WPD achieves an insertion loss and isolation of better than 1 dB and 20 dB from 11.5 to 17 GHz, as shown in Fig. 3. It outperforms the 4-section LC WPD while consuming less than half of the chip area. Its design methodology is summarized in the following three steps:

Step 1  Design an inductor of inductance \( L_{\text{total}} = 4L \). The value of \( L \) and \( C \) are calculated using the well-known expressions of \( T_D = \sqrt{L/C} \) and \( Z_o = \sqrt{L/C} \).

Step 2  Choose the inductor metal line center as tap position 3. The other two taps are selected from the sub-section inductance calculation. Consider the capacitors connection carefully because the inductor shape may need some modification.

Step 3  If necessary, co-optimize the capacitance values of capacitors according to the predicted inductance values. They should satisfy (6) to ensure impedance transformation and matching.
4 Measurement results

Fig. 6 shows the die micrograph of the WPD. Fabricated in 65-nm CMOS, the core area is $188 \times 116 \ \mu m^2$. The prototype WPD was measured on a high-frequency probe station.

![Die microphotograph of the multi-tap inductor based WPD.](image)

Fig. 6. Die microphotograph of the multi-tap inductor based WPD.

Fig. 7 shows the measurement results of the multi-tap inductor based WPD. The insertion loss shown in Fig. 7(a) is less than 1 dB from 11 to 16 GHz. The isolation and return losses are better than 20 dB and 16 dB respectively (see Fig. 7(b)). The measured results are in good agreement with simulations. From 6 to 22 GHz, the WPD achieves the isolation, insertion loss and return losses better than 10 dB, 1.8 dB and 11 dB respectively.

![Measurement results of the multi-tap inductor based WPD (a) $S_{23}/S_{31}$ (b) $S_{23}/S_{11}/S_{22}/S_{33}$.](image)

Fig. 7. Measurement results of the multi-tap inductor based WPD (a) $S_{23}/S_{31}$ (b) $S_{23}/S_{11}/S_{22}/S_{33}$. 
Table I. Performance comparison of integrated WPDs.

| Ref. | Technology   | Frequency (GHz) | Insertion Loss (dB) | Isolation (dB) | Return Loss (dB) | Core Area (mm²) | Relative |
|------|--------------|-----------------|---------------------|---------------|-----------------|----------------|----------|
| [11] | 0.13 μm CMOS | 22–26           | <1.4                | >14.8         | >8.9            | 0.035          | 2.2E-4λo² |
| [12] | 0.13 μm SiGe | 5.2–19.5        | <1                  | >10           | >10             | 0.109          | 2E-4λo²  |
| [15] | 0.5 μm GaAs  | 1.87–3.5        | <1.17               | >15           | >15             | 1.258          | 8.7E-5λo² |
| [16] | 0.35 μm SiGe | 8–14            | 1.4                 | >10           | >12             | 0.12           | 1.3E-4λo² |
| [17] | 65 nm CMOS   | 35.67           | <0.8                | >10           | >13             | 0.0055         | 2.2E-4λo² |
| This work | 65 nm CMOS | 11–16           | <1                  | >20           | >16             | 0.022          | 4.4E-5λo² |
|       |              | 6–22            | <1.8                | >10           | >11             |                |          |

Table I shows the performance comparison of the proposed work with prior-arts in SiGe, CMOS and GaAs technologies. The WPD proposed in this letter achieves broadband performance in a relatively small area, competing well with other works.

5 Conclusion

This letter proposes a compact and low-loss Ku-band WPD. The multi-tap inductor technique is used to achieve broadband isolation while minimizing the chip area. The WPD is fabricated in 65-nm CMOS technology and occupies a core area of 188 × 116 μm². It achieves isolation better than 10 dB from 6 to 22 GHz. From 11 to 16 GHz, the WPD provides an isolation higher than 20 dB with the insertion loss less than 1 dB.

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