Comparing binary and ternary adders and multipliers

Daniel Etiemble
Computer Science Laboratory (LRI)
Paris Sud University
Orsay, France
de@lri.fr

Abstract—While many papers have proposed implementations of ternary adders and ternary multipliers, no comparisons have generally been done with the corresponding binary ones. We compare the implementations of binary and ternary adders and multipliers with the same computing capability according to the basic blocks that are 1-bit and 1-trit adders and 1-bit and 1-trit multipliers. Then we compare the complexity of these basic blocks by using the same CNTFET technology to evaluate the overall complexity of N-bit adders and M-trit adders on one side, and NxN bit multipliers and MxM trits multipliers with M = N/IR (IR = log(3)/log(2) is the information ratio). While ternary adders and multipliers have less input and output connections and use less basic building blocks, the complexity of the ternary building blocks is too high and the ternary adders and multipliers cannot compete with the binary ones.

I. INTRODUCTION

Many papers have been published on the design and performance of ternary circuits at different levels: inverters, basic gates, arithmetic circuits, flip-flops and SRAMs, etc. Some of these papers will be quoted in this text. However, these papers generally do not compare the ternary circuits with the corresponding binary ones. Having presenting such a comparison in 1988 [1], we want to do it again more than 30 years later to determine if ternary circuits can compete with the binary ones. As ternary wires carry more information, N bits are approximately equivalent to M trits according to the relation M = N/IR where IR = log(3)/log(2) = 1.585 is the information ratio per wire. Table I presents the correspondence for some values of N. Due to rounding, N/M ranges from 1.5 to 1.6 in Table I.

Table I: Number of ternary and binary wires

| Number of bits | 8  | 16  | 32  | 64  |
|---------------|----|-----|-----|-----|
| Number of trits | 5  | 11  | 21  | 41  |

We restrict the comparison to the arithmetic circuits, which are typical implementations of combinational logic. We compare ternary and binary circuits having approximately the same computing capability. For adders or multipliers, it means comparing N-bit circuits with M-trit circuits according to the information ratio per wire. The table presents the correspondence for some values of N. Due to rounding, N/M ranges from 1.5 to 1.6 in Table I.

We restrict the comparison to the arithmetic circuits, which are typical implementations of combinational logic. We compare ternary and binary circuits having approximately the same computing capability. For adders or multipliers, it means comparing N-bit circuits with M-trit circuits according to the information ratio per wire. The table presents the correspondence for some values of N. Due to rounding, N/M ranges from 1.5 to 1.6 in Table I.

II. ADDERS

A. Carry-Propagate Adders (CPAs)

1) The carry propagate approach: The most straightforward implementation of N-bit or M-trit adders is the carry propagate scheme, also called “Ripple-Carry Adder”. It is presented in Figure I for a 4-digit adder. For the binary version, Ai, Bi and Ci are binary values. For the ternary version, Ai and Bi are ternary values, while Ci are binary values. In the literature, ternary adders are sometimes presented with ternary carries. We consider them as ternary compressors that could be used in Wallace trees for multiplication. For ternary additions, the carries are always binary.

2) 8-bit CPA versus 5-trit CPA: An 8-bit CPA uses eight 1-bit full adder while a 5-trit CPA uses five 1-trit full adder. The comparison is straightforward: a 5-trit multiplier will be more efficient if the 1-trit adder complexity is no more than x8/5 the 1-bit adder. The result is the same for any M-trit adder compared to a N-bit adder for which M ≈ N/1.585. Obviously, there are different other techniques to implement...
fast adders. Considering all the possible versions is out of the scope of this paper. We just consider two other schemes which purpose is to speed-up the carry propagation.

B. Carry Look-ahead Adders (CLAs)

Figure 2 presents a 4-bit carry look-ahead adder. This adder has the same number of full adders than the CPA. The binary equations of the carry computation part are well-known:

\[ G_i = A_i \cdot B_i \]
\[ P_i = A_i \oplus B_i \]
\[ C_1 = G_0 + P_0 \cdot C_0 \]
\[ C_2 = G_1 + G_0 \cdot P_1 + P_0 \cdot P_1 \cdot C_0 \]
\[ C_3 = G_2 + G_1 \cdot P_2 + G_0 \cdot P_1 \cdot P_2 + P_0 \cdot P_1 \cdot P_2 \cdot C_0 \]
\[ C_4 = G_3 + G_2 \cdot P_3 + G_1 \cdot P_2 \cdot P_3 + G_0 \cdot P_1 \cdot P_2 \cdot P_3 + P_0 \cdot P_1 \cdot P_2 \cdot P_3 \cdot C_0 \]

For the ternary implementation, \( G_i \) and \( P_i \) are binary functions of ternary inputs. The computation of \( C_1, C_2, C_3 \) and \( C_4 \) uses binary circuits.

- For stage \( i \), a carry is generated when \( (A_i = 2 \text{ and } B_i = 1) \) or \( (A_i = 1 \text{ and } B_i = 2) \).
- For stage \( i \), a carry is propagated when \( (A_i = 0 \text{ and } B_i = 2) \) or \( (A_i = 1 \text{ and } B_i = 1) \) or \( (A_i = 2 \text{ and } B_i = 0) \).

Just as CPAs, an 8-bit CLA uses eight 1-bit full adders while a 5-trit CLA uses five 1-trit full adders. As the binary carry look-ahead computation complexity increases with the carry index, an 8-bit CLA is generally implemented as a cascade of two 4-bit CLAs. The carry computation part is thus two times the carry computation of a 4-bit CLA. The computation of the carry look-ahead part of a 5-trit CLA can be implemented as a block of 5-trit, with \( G_i \) and \( P_i \) (\( 0 < i < 5 \)) and 5 equations computing \( C_1 \) to \( C_5 \). Comparing the two approaches means

- Comparing eight 1-bit full adders with five 1-trit full adders
- Comparing two blocks of 4-bit look-ahead computation with one block of 5-trit look-ahead computation

The comparison is exactly the same for 16-bit, 32-bit or 64-bit adders and the corresponding ternary adders.

C. Carry Skip Adders (CSA)

Figure 3 presents a 4-bit binary skip adder. As the CPA, it has four 1-bit full adders. The carry “skip” scheme uses the \( P_i \) propagate function of the CLA, a And gate to compute \( P_0 \cdot P_1 \cdot P_2 \cdot P_3 \) and a two-input multiplexer. For the “skip” part, the only difference between the binary and the ternary version is the computation of the propagate functions, which have been defined for the CLA.

Just as CPAs, an 8-bit CSA uses eight 1-bit full adders while a 5-trit CSA uses five 1-trit full adders. As for the CLA approach, the 8-bit “skip” part is decomposed into two blocks of 4-bit “skip” parts while the 5-trit CSA has only one block of 5-trit “skip” part. Comparing the two approaches means

- Comparing eight 1-bit full adders with five 1-trit full adders
- Comparing two blocks of 4-bit “skip” computation with one block of 5-trit “skip” computation. A binary block computation uses four \( P_i \) functions, one 4-input And gate and one multiplexer. A ternary block computation uses five \( P_i \) functions (binary functions of ternary inputs), one binary And gate and one binary multiplexer.

D. Adder comparisons

CPAs, CLAs and CSA have the same N/M ratio of 1-bit adders and 1-trit adders. This ratio is close to \( IR = 1.585 \). For CLAs and CSAs, the circuits to speed-up computation slightly modifies the overall comparison. More details will be given in Section 5.

III. MULTIPLIERS

A. Comparing a 8*8 binary multiplier with a 5*5 ternary one

1) 8*8 binary multiplier: Typical binary multipliers can be decomposed in two parts: the first one generates the partial products and the second part reduces the partial products into
two sums to be added by a final fast adder. Figure 4 shows the process for an 8*8 bit multiplier.

- The first part generates 8 partial products of 8 bits, i.e. 64 bits that are the products of $A_i \times B_j$ for $0 \leq i < 8$ and $0 \leq j < 8$. The binary product $A_i \times B_j$ is implemented by a And gate.

- The reduction of the partials products can use different schemes. The typical one is the Wallace tree, for which 3 lines of partial products are reduced to two lines by using 3-input 2-output full adders (and half adders). For 8*8 bit multipliers, there are several steps of parallel additions of lines of partial products: 8 to 6, 6 to 4, 4 to 3, and finally 3 to 2. At that point, a fast adder is used to add the two final lines. Dadda reduction tree is another one. Other reduction operators can be used, such as 4-2 compressors, 7-3 compressors, etc. With the 3-2 reduction scheme, there are 35 FAs and 18 HAs. Considering the final addition, the total is 44 FAs and 19 HAs.

2) 5*5 ternary multipliers: Ternary multipliers use 3 different values (0, 1 and 2). A ternary wire carries more information than a binary one. The information ratio is $IR = \log(3)/\log (2) = 1.585$. An $M \times M$ ternary multiplier would be equivalent to a $N \times N$ binary multiplier with $M = N/1.858$. For $N = 8$, $M = 5.04$. A 5x5 trit multiplier has slightly less computing capability than an 8*8 bit multiplier. Figure 5 shows the process for a 5*5 trit multiplier.

- The ternary product $A_i \times B_j$ generates one trit (product) and one binary carry according to Table II. The first part generates 5 partial products of 5 trits and 5 partial products of 5 bits for $A_i \times B_j$ for $0 \leq i < 5$ and $0 \leq j < 5$. 10 lines of partial products should be reduced.

- A Wallace tree can be used to reduce the 10 partial products down to two final lines to be summed by a fast ternary adder. As shown in Figure 5, the reduction process alternates between a set of 2 ternary lines and 1 binary line and a set of 1 ternary line and 2 binary lines. The reduction tree is thus based on usual ternary full adders (quoted as T-FA) and ternary half adders (quoted as T-HA). There is one specific case when two successive lines are binary lines. In that case, T-HAs can be used for a 2 to 1 reduction that only provides one ternary line. The different steps are thus 10 to 7, 7 to 5, 5 to 3 and 3 to 2 for a total of 29 T-FAs and 12 T-HAs. Considering the final addition, the total is 34 T-FAs and 12 T-HAs.

3) Comparing $N \times N$ bit multipliers with $M \times M$ trit multipliers for $N = 8, 12, 16$: The comparison includes

- The number of 1-bit multipliers and 1-trit multipliers
- The number of binary full and half adders (B-FA and B-HA) and ternary full and half adders (T-FA and T-HA) for the reduction trees
- The final fast adder can use techniques such as carry-look adder adders, carry skip adders, etc. To keep the comparison simple, we consider using the carry propagate adder (CPA) which simply cascades B-FAs or T-FAs. While more sophisticated techniques speed-up the propagation
The ternary Wallace tree operates on a smaller number of trits (N/IR), but two times more partial product lines because the 1-trit multiplier generate a product term and a carry. It results than there are only slightly more equivalent 1-bit adders than 1-trit adders. The ratio ranges from 1.13 to 1.36 for the cases that we considered. The complexity of the ternary full adder versus the binary full adder should not be more than a value that is less than IR.

### IV. Complexity comparisons

Comparing ternary and binary circuits is not easy. The main reason is that there have been a huge number of binary circuits designed, fabricated and used since the first days of integrated circuits, while very few ternary circuits have been fabricated and used. In the last period, while FinFET technologies have been implemented with 14 nm, 10 nm and even 7 nm technological nodes, only proposals of ternary or multivalued circuits can be found, generally based on simulations. To be able to make significant comparisons, we must define a common technology for both types of circuits and define some complexity measures.

#### A. A technology: CNTFET

A carbon nanotube field-effect transistor (CNTFET) refers to a field-effect transistor that uses a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET. The MOSFET-like CNTFETs having p and n types look the most promising ones. This technology has advantages and drawbacks:

- CNTFET have variable threshold voltages (according to the inverse function of the diameter). Among advantages, high electron mobility, high current density, high transconductance can be quoted.
- Lifetime issues, reliability issues, difficulties in mass production and production costs are quoted as disadvantages.

We use this technology for several reasons:

- It is one of the few proposed ones to overcome the limitations of the FinFET technologies after the end of Moore’s law.
- Its variable threshold voltages make easier the implementation of the different thresholds that are needed for ternary and multi-valued circuits.
- The MOSFET-like CNTFETs have the same circuit styles as the CMOS technologies, which means that the comparison results are not limited to that technology.
- A large number of CNTFET ternary or m-valued circuits have been proposed in the recent last years. They facilitate the comparison with the corresponding binary circuits. We will use these proposals for the comparisons.

#### B. Complexity figures

Hardware complexity is difficult to define as many parameters can be considered:

- Number of transistors
- Number of interconnections
- Chip area

### TABLE III

**Comparison for 8*8 bit and 5*5 trit multipliers**

| Ai*Bi   | Binary | Ternary | Binary/F ternary |
|---------|--------|---------|------------------|
| 64      | 25     |         | 2.56             |
| Reduction FA | 35      | 29      |                  |
| Reduction HA | 18      | 12      |                  |
| Final Add FA | 9       | 5       |                  |
| Final Add HA | 1       | 0       |                  |
| Total FA   | 44      | 34      |                  |
| Total HA   | 19      | 12      |                  |
| Total equivalent FA | 53.5   | 40      | 1.34             |

### TABLE IV

**Comparison for 12*12 bit and 8*8 trit multipliers**

| Ai*Bi   | Binary | Ternary | Binary/F ternary |
|---------|--------|---------|------------------|
| 144     | 64     |         | 2.25             |
| Reduction FA | 102     | 102     |                  |
| Reduction HA | 34      | 18      |                  |
| Final Add FA | 18      | 10      |                  |
| Final Add HA | 0       | 0       |                  |
| Total FA   | 120     | 112     |                  |
| Total HA   | 34      | 18      |                  |
| Total equivalent FA | 137     | 121     | 1.13             |

Using the same methodology, Table IV compares a 12 × 12 bit multiplier and a 8 × 8 trit one. Table V compares a 16 × 16 bit multiplier and a 10 × 10 trit one.

### TABLE V

**Comparison for 16*16 bit and 10*10 trit multipliers**

| Ai*Bi   | Binary | Ternary | Binary/F ternary |
|---------|--------|---------|------------------|
| 256     | 100    |         | 2.56             |
| Reduction FA | 200     | 153     |                  |
| Reduction HA | 54      | 38      |                  |
| Final Add FA | 24      | 13      |                  |
| Final Add HA | 1       | 1       |                  |
| Total FA   | 224     | 166     |                  |
| Total HA   | 55      | 39      |                  |
| Total equivalent FA | 251.5   | 185.5   | 1.36             |
- Power dissipation
- Propagation delays
- Etc.

Obviously, the most significant information is speed, chip area and power dissipation of fabricated chips in a given technology. However, comparing ternary and binary circuits according to chip area and power dissipation is quite impossible as there are very few or no integrated ternary circuits available for comparisons. Comparisons must be done with a simple criterion that is available from the circuit electrical scheme. We use the number of transistors. Although the transistor count is only an estimation, it gives significant insights. In fact, when using the same technology to implement the same operator, it is very doubtful that:

- More transistors lead to less interconnects as these transistors are interconnected
- More transistors lead to less chip area.
- More transistors lead to less power dissipation

Finding counter-examples look very challenging! When the difference in transistor counts is limited to a few %, no conclusion can be derived. However, if the transistor count for ternary circuits is x2, x3 or more than for the equivalent binary circuits when the information ratio \( IR = \frac{\log(3)}{\log(2)} = 1.585 \), it only means that the ternary circuits have more interconnects, more chip area, more power dissipation than the corresponding binary ones.

V. COMPLEXITY OF TERNARY AND BINARY ADDERS

A. Complexity of 1-bit and 1-trit adders

For 1-bit, various designs have been proposed using binary CMOS circuitry, which can be considered to implement CNTFET binary 1-bit adders [3]. The transistor counts range from 28T for the conventional CMOS design down to 8T for a scheme using 3T Xor gates. Typical implementations with transmission gates use 14T or 16T. All circuits are not equivalent: while conventional CMOS design has maximal noise margins, circuits using transmission gates, or directly connecting inputs either to drain or source of transistors can have reduced noise margins. There is not a similar comparison of the different ternary 1-trit adders. Our reference is the CNTFET ternary half-adder proposed in 2017 [4] that will be completed to implement a ternary full adder. As any multivalued circuits, the ternary half adder uses the general scheme presented in Figure 6. The decoder (a, b) and encoder (c) circuits are presented in Figure 7. The sum binary part and the carry generation part are respectively presented in Figure 8 and Figure 9. The transistor count for the ternary half adder is 66T.

While the half adder compute Sum10, Sum20 and Cm0 with an implicit input carry equal to 0, similar circuitry can be used to compute Sum11, Sum21 and Cm1 when the input carry is 1. Two multiplexers controlled by the input carry are used to compute the final Sum1, Sum2 and Cm to drive the final encoder and carry circuit. We do not show all the details of computation. The final count for the full adder is 124T. Table 6 summarizes the number of transistors for the ternary adder and different binary adders. There are from \( x4.4 \) to \( x15.5 \) more

![Fig. 6. General scheme of m-valued circuits.](image)

![Fig. 7. Decoder and encoder circuits.](image)

![Fig. 8. Sum binary parts.](image)

![Fig. 9. Carry generation.](image)
transistors for the ternary adder versus the different binary adders.

Two papers should also be mentioned, which allow a comparison between the binary and the ternary implementations of a carbne nanotube full adder [5] [6]. They both use the threshold logic approach with a linear combination of capacitive inputs. The advantage is the reduction of the number of devices needed to combine the inputs. The drawback is a drastic reduction of the noise margins when coherent noises are simultaneously present on the different inputs. If NM is the noise margin for one input, the noise margin for N-input is NM/N. The binary FA is presented in Figure 10. Considering that the capacitors are implemented with transistors as in Figure 11, it has 11 T. The ternary FA is presented in Figure 11: it has 27T. The ratio is $\frac{27}{11} = 2.45$, which is greater than the information ratio $IR = 1.585$.

B. Complexity of carry circuitry

1) Ripple carry adders: As previously mentioned, a M-trit multiplier will be more efficient than a N-bit multiplier with $M \approx \frac{N}{1.585}$ iff the 1-trit adder complexity is no more than x1.585 the complexity of the 1-bit adder. As shown in Table 6, this is never the case when comparing the best implementations for binary and ternary adders.

2) Carry-Look Ahead Adders: We now compare the carry circuitry for 5-trit and 8-bit CLAs. The equations have been given in 2.2. Binary Gi and Pi functions are implemented respectively by Nand + Inverter and Nor + inverter. Both function uses 6T. Binary C1 is implemented as $C1 = \overline{G0}\overline{P0}\overline{C0}$, i.e. one inverter and two 2-input Nand gates for a total of 10T. C2, C3, C4 are implemented by two levels of Nand gates. The transistor count for a 4-bit carry computation is given in Table VII. The transistor count for a 5-trit carry computation is given in Table VIII.

It turns out that the carry computations are more costly for a 5-trit CLA than for an 8-bit CLA. The difference comes from the cost of computing Gi and Pi ternary functions versus the binary ones.

3) Carry-Skip Adders: For an 8-bit CSA, the binary carry computation is composed of two 4-bit skip computations. For 4-bit, it means P0 to P3 functions, a 4-input And gate and a multiplexer. For a 5-trit CSA, the carry computation uses P0 to P4 functions, a 5-input And gate and a multiplexer. The transistor counts are given in Table IX. Again, the ternary approach is more costly due to the Pi computation costs.

4) Conclusion for adders: The transistor count for 1-trit adders is greater than for 1-bit adder and cannot compensate the reduced number of adders. Similarly, the carry computations are more costly for CLAs and CSAs. For CPAs, CSAs and CSAs, the M-trit adders cannot compete with the N-bit adders with $M = \frac{N}{1.585}$.

### TABLE VI

| Transistor count | 3-FA | Nand-2 FA | Xor-2 FA | 8T-FA |
|------------------|------|----------|----------|-------|
| Ratio 3/2        | 124  | 28       | 14 to 16 | 8     |
|                  | 7.7 to 8.8 |        |          | 15.5 |

### TABLE VII

| Function | Gi | Pi | C1 | C2 | C3 | C4 | 4-bit | 8-bit |
|----------|----|----|----|----|----|----|-------|-------|
| Transistor count | 24 | 24 | 10 | 18 | 28 | 40 | 144   | 288   |

### TABLE VIII

| Function | Gi | Pi | C1 | C2 | C3 | C4 | C5 | 5-trit |
|----------|----|----|----|----|----|----|----|--------|
| Transistor count | 80 | 90 | 10 | 18 | 28 | 40 | 54 | 310    |

### TABLE IX

| Function | Pi | Nand+inverter | Mux | 4-bit CS | 8-bit 5-trit CS |
|----------|----|---------------|-----|----------|-----------------|
| Binary   | 24 | 10            | 14  | 48       | 96              |
| Ternary  | 90 | 12            | 14  | 48       | 116             |
VI. COMPLEXITY OF BINARY AND TERNARY MULTIPLIERS

Ternary and binary multipliers are decomposed in two parts:
- 1-trit and 1-bit multipliers
- 1-trit and 1-bit full adders and half-adders that are used in the reduction tree.

A. Complexity of 1-bit and 1-trit multipliers

1-bit multiplier is implemented with a And gate, which means 6T (Nand + Inverter). 1-trit multiplier is far more complicated as it generates a product and a carry according to Table II.

Using the same approach as for the ternary adder, the equations are:

\[ S_2 = A_1 \cdot B_1 \cdot B_0 + B_1 \cdot A_1 \cdot A_0 \]  
\[ S_1 = A_1 \cdot B_1 + B_1 \cdot B_0 \cdot A_1 \cdot A_0 \]  
\[ C_m = A_1 \cdot B_1 \]

The number of transistors for the 1-trit multiplier is 4 (decoder) + 12 (Sum2) + 12 (Sum1) + 6 (Product encoder) + 4 (cout encoder) = 38 T, i.e. 38/6 = 6.3. While a 5-trit multiplier uses 25 1-trit multiplier (950 T), a 8-bit multiplier uses 64 And gates for a total of 384 T. The ternary/binary ration is x2.47. There are less 1-trit multipliers than 1-bit ones. However, it cannot compensate their larger complexity compared to the binary ones.

B. Complexity of the reduction tree

We consider the reduction trees for 5-trit multipliers and 8-bit multipliers. The ternary Wallace tree (Figure 5) has 34 T-FAs and 14 T-HAs and the binary Wallace tree (Figure 3) has 35 B-FAs and 18 B-HAs. For a quick comparison, we can assume that a HA transistor count is half the FA transistor count. Then there are approximately 41 T-FAs and 44 B-FAs. Obviously, this small difference is not able to compensate the advantage of binary FAs compared to ternary FAs that were shown in 2.4. The issue for ternary multipliers is the carry generated by the 1-trit multiplier, which doubles the number of partial products to reduce by the Wallace tree.

C. Overall complexity

Both the set of elementary multipliers and the Wallace tree needs more transistors for the ternary approach versus the binary ones. M-trit multipliers cannot compete with N-bit ones with \( M = N/1.585 \).

VII. CONCLUDING REMARKS

We have compared ternary and binary adders and multipliers processing the same amount of information. First, we compared the number of elementary cells such as 1-bit/1-trit full adders, 1-bit/1trit multipliers. This comparison remains valid for any implementation of these cells. Then we consider the hardware complexity using the transistor count for the typical implementation of these cells with CNTFET technology. It turns out that both ternary adders and multipliers cannot compete with the binary ones. If M-trit adders or multipliers have less input and output connections than the corresponding N-bit adders or multipliers, the larger number of transistors means that the ternary arithmetic operators have more connections when considering the internal ones. More transistors mean more connections, more chip area, more propagation delays and more power dissipation for the ternary operators versus the binary ones when using the same technology.

REFERENCES

[1] D. Etiemble, M. Israel, “Comparison of Binary and Multivalued ICs according to VLSI Criteria”; in Computer, Vol. 21, Issue 4, April 1988, pp 28-42.
[2] W. J. Townsendl, E. E. Swartzlander Jr. and J. A. Abraham, “A comparison of Dadda and Wallace multiplier delays”, Proc. SPIE 5205, Advanced Signal Processing Algorithms, Architectures, and Implementations XIII, (24 December 2003); https://doi.org/10.1117/12.507012
[3] R. Anitha, “Comparative study on transistor based full adder designs”, World Scientific News, WSN 53(3) (2016) 404-416, EISSN 2392-2192
[4] S.K. Sahoo, G.Akhilesh, R. Sahoo and M. Mugkilar, “High Performance Ternary Adder using CNTFET”, IEEE Transactions on Nanotechnology, Vol 16, No 3, January 2017
[5] K. Navi, A. Momeni, F. Shariﬁ and P. Keshavarzian, “Two novel high speed carbon nanotube Full-Adder cells”, in IEICE Electronics Express, Vol. 6, No 19, 1395-1401, 2009
[6] R. Faghih Mirzaee and K. Navi, “Optimized Adder Cells for Ternary Ripple-Carry Addition” in IEICE Trans. INF SYST, Vol.E97-D, No 9, September 2014.