Formalizing Traceability and Derivability in Software Product Lines

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Abstract—In the literature, the definition of product in a Software Product Line (SPL) is based upon the notion of consistency of the constraints, imposed by variability and traceability relations on the elements of the SPL. In this paper, we contend that consistency does not model the natural semantics of the implementability relation between problem and solution spaces correctly. Therefore, we define when a feature can be derived from a set of components. Using this, we define a product of the SPL by a (specification, architecture) pair, where all the features in the specification are derived from the components in the architecture. This notion of derivability is formulated in a simple yet expressive, abstract model of a productline with traceability relation. We then define a set of SPL analysis problems and show that these problems can be encoded as Quantified Boolean Formulas. Then, QSAT solvers like QUBE can be used to solve the analysis problems. We illustrate the methodology on a small fragment of a realistic productline.

Keywords—Software Product Line; Sanity analysis; Formal methods; QSAT

I. INTRODUCTION

Software Product Line (SPL) is a development framework to jointly design a family of closely related software products in an efficient and cost-effective manner. Every SPL is built upon a collection of features and components. Each individual product is specified by a subset of features. Each product in the family is specified by a set of features drawn from a collection common to the family, and is implemented by an architecture comprising a set of reusable components selected from a collection of basic assets which are developed once for the entire family.

There are two key orthogonal aspects of an SPL, namely, variability and traceability. While variability introduces different choices (termed variation points) within the artifacts in system development, such as specifications, architectures and components, traceability relates the variation points together across the artifacts. Since variability introduces complex constraints among the variation points, managing variability in large industrial SPLs is quite complex and has given rise to a number of analysis problems. These have been the focus of SPL research in the recent years. A comprehensive survey of these analysis problems and their solutions can be found in Benavides et al. [1].

On the other hand, we observe that traceability and its implications have not been studied in much depth in the literature. In the following, we mention the few works addressing traceability as a primary aspect. It is defined in [2] as one of the four important characteristics of a variability model, namely, consistency, visualization, scalability and traceability. A variability management model that focuses on the traceability aspect between the notion of problem and solution spaces is presented in [3]. Anquetil et al. [4] formalize the traceability relations across problem and solution space and also across domain and product engineering. In [5], the notion of product maps is defined which is a matrix giving the relation between features and products. Consistency analysis of product maps is presented in [6]. Zhu et al. [7] define a traceability relation from requirement to feature and also from feature to architecture with consistency analysis. [8] presents a consistency verification method between feature model and architecture model. Metzger et al. [9] differentiate SPL variability and product variability and then present a framework based on OVM by Pohl et al. [10] to perform checks for consistency, liveness, commonness, realizability (completeness), and flexibility (soundness).

One of the central concepts of the SPL analyses in the above-mentioned works is that of a product. It is defined through the notion of consistency between a collection of features and components and the constraints imposed by variability and traceability. In this report, we contend that consistency does not model the natural semantics of the implementability relation between problem and solution spaces correctly. It allows components and features to coexist without any conflict, but it also allows cases where the features may not be derivable from the components. Hence, the SPLs can be shown to allow products where the components are not related to the features in a more intuitive notion of traceability. Therefore, we define when a feature can be derived from a set of components. Using this, we define a product of the SPL by a (specification, architecture) pair, where all the features in the specification are derived from the components in the architecture. This definition of products is tighter than the existing "consistency" based definitions.
An introduction to the report is a simple yet expressive, abstract model of a product line where we formally define the derivability notion through the traceability relation. We then define a set of SPL analysis problems. Some of these problems are already addressed in earlier works but are redefined in the light of the new concepts. The others are new and arose because of the separation of problem and solution space linked through traceability. We show that these problems, in general, can be encoded as Quantified Boolean Formulas (QBF) and QSAT solvers \[11\] can be used to solve the problems. We illustrate the methodology on a small fragment of a realistic product line.

The summary of our contributions in this report are the following:

1) A new definition for SPL products based on a notion of derivability of feature specifications from component architectures. The traceability relation plays the central role in this definition.

2) A simple, abstract semantic model of SPL with traceability. The model abstracts out the details from the existing descriptions of SPL in the literature and allows us to define the core concepts in a formal and concise manner.

3) A set of analysis problems in the SPL, some of which are known but cast anew in the light of the new definitions, and others that are novel.

4) A solution method for the analysis problems which is based on QBF encoding and QSAT solving. This is necessitated by the nature of some of the analysis problems and is in contrast to the SAT based solving methods generally employed for the extant SPL analyses.

Outline of The Report: In the following section, we introduce a case study of Entry Control Product Line (ECPL) from the automotive domain. This is used as a running example throughout the rest of the report. The formal model of an SPL with traceability is described in Section III. It introduces the central notion of derivability and the analyses we would like to carry out in SPL. In Section IV, we show how the analysis problems can be encoded in QBF. The results of the analyses using QSAT on the ECPL case study is presented in Section V. Finally, we conclude in Section VII with a summary of the report and some future directions. The proof of the main result relating the analysis problems and QBF formulae is given in the appendix.

II. THE ENTRY CONTROL PRODUCT LINE (ECPL)

We introduce a fragment of a typical Entry Control Product Line (ECPL) used in the automotive industry. It will be used to illustrate the concepts throughout the report and as a case study in Section IV. The entry control system comprises all the features involved in the controlling of door locking/unlocking in a car. In this study, we focus on the following subset:

- Manual lock: controls the locking/unlocking through manual lever presses
- Power lock: controls the locking/unlocking according to key button press, courtesy switch press and sill button press.
- Door lock: controls automatic locking of doors when the vehicle starts.
- Door relock: controls automatic relocking of doors in case of pick up/drop and drive.

The ECPL feature diagram: Figure 1 presents the feature diagram of the ECPL (a la Czarnecki \[12\]). The dark gray boxes are features of the ECPL. The light gray boxes are parameters modeled as features. The Power lock feature is mandatory. Manual lock is optional. When it is present, the Power lock feature is excluded. The Door lock feature is optional and can be triggered either when gear is shifted out of park or when car speed reaches a predefined value. The Door relock feature is optional. The car should have either a manual or an automatic transmission. Manual transmission disallows the “park options” of Door lock since there is no park gear in a manual gearbox.

The ECPL architectural diagram: Figure 2 represents the platform of ECPL using a notation called Modal Architectural Model (abbreviated as MAM). It is a simplified form of EASEL by \[13\] and yet preserves the essential notion of variability central to the product line. The platform is composed of three components: Door lock manager, Power lock, and Auto lock. The first is mandatory but the two others are optional (denoted by dotted boxes). The system has seven “in” ports (dark squares) and three “out” ports (light squares). The interconnections between external and internal ports connect ports of the same type but internal interconnection connect complementary ports (“out” port to “in” port). The signals “Transmission in Park” and “Speed” are alternatives. Similarly “Automatic” and “Manual” inform the system on the type of transmission.

Auto lock component requires two global input signals while Power lock component requires five. They provide lock/unlock command signals to Door lock manager. The command provided by Power lock component depends upon manual action, and the command provided by Auto lock component is according to the requirements of the
features Door lock and Door relock.

The Door lock manager component arbitrates the lock/unlock command signals from Auto lock and Power lock and forwards them to the global outputs depending upon a calibration (1/Unlock all doors, 2/Unlock Driver door, 3/Lock all doors).

The traceability relations of the ECPL: To avoid confusion between the homonymous features and components (Automatic, Manual, and Speed), we, in the sequel, prefix the labels with $f_-$ or $c_-$ respectively. Table I presents the required components to implement each feature.

| Feature              | Component                  |
|----------------------|----------------------------|
| Power lock           | Door lock manager & Power lock |
| Door lock            | Auto lock                  |
| Door relock          | Auto lock                  |
| $f_-$Automatic       | $c_-$Automatic             |
| $f_-$Manual          | $c_-$Manual                |
| Shift out of Park    | Gear in Park               |
| $f_-$Speed           | $c_-$Speed                 |

Table I

Each feature requires component(s)

Table II presents the features provided by the architectural elements.

| Component/Interconnection | Feature              |
|---------------------------|----------------------|
| Door lock manager & Power lock | Power lock |
| $c_-$Automatic            | $f_-$Automatic       |
| $c_-$Manual               | $f_-$Manual          |
| Auto lock                 | Door lock & Door relock |
| Gear in park              | Shift out of park    |
| $c_-$Speed                | $f_-$Speed           |

Table II

The architectural elements provide some features

III. MODEL OF SPL: TRACEABILITY AND IMPLEMENTATION

In this section, we propose a model of the software productline making the traceability relation explicit and define an implementation relation between architectures and specifications based on traceability.

A. Modeling Decisions

In [9], the traceability relation is given as a set of arbitrary propositional constraints over the components and features. In the current report, we impose a fairly natural structure on the traceability relation, consisting of a provides and a requires function for each feature. This is inspired by the points of view of the suppliers and integrators (OEMs). Suppliers usually would package one or more features in a component, which is captured by the provides relation. On the other hand, integrators start with a set of features which requires a set of components for implementation.

Importantly, the implementations are related to the specifications only when they can be derived using the traceability relation. Consider a simple SPL consisting of a feature $f$ and a component $c$, but without any traceability relation between $f$ and $c$. According to analyses such as in [9], since $\{f, c\}$ is consistent (in a propositional logic), it is considered as a product. Clearly, it is not natural. On the other hand, if $f$ was provided by $c$, then $\{f, c\}$ would be a natural product.

Another novel point in our model is the notion of approximate implementation (Covers). In the literature, the definition of implementation is usually exact: we need the components that provide exactly the same set of features in a specification. However, since many components are pre-built by the suppliers, there may not be a choice suitable for an exact implementation. For example, if the OEM wants a feature of ABS (Anti-lock Braking) and the supplier has packaged both ABS and TC(Traction Control) in one component, the OEM has to choose this component which covers (but does not exactly implement) the specification of ABS.

B. Formal Model

Let $\mathcal{F}$ be a set of features. A subset of $\mathcal{F}$ is called a specification. The scope of an SPL is a collection of specifications: $\overline{\mathcal{F}} \subseteq \varphi(\mathcal{F})$. The specifications are implemented using a set of (reusable) components $\mathcal{C}$. Each subset of $\mathcal{C}$ is called an architecture. An SPL platform consists of a set of architectures: $\overline{\mathcal{C}} \subseteq \varphi(\mathcal{C})$.

A traceability relation $\mathcal{T}$ connects the features and components: $\mathcal{T}$ is specified as a pair $(\text{prov}, \text{req})$ where $\text{prov}$ and $\text{req}$ are maps $\mathcal{F} \to \varphi(\varphi(\mathcal{C}))$. Through the traceability relation we capture the sufficient $(\text{prov}(\cdot))$ and necessary $(\text{req}(\cdot))$ conditions to implement a feature. When $\text{prov}(f) = \{C_1, C_2\}$, we interpret it as the fact that the set of components $C_1$ (also, $C_2$) provides the implementation of the feature $f$. On the other hand, when $\text{req}(f) = \{D_1, D_2\}$, we interpret as the fact that the implementation of the feature $f$ requires the set of components $D_1$ or the set of components $D_2$.

Definition 1. An SPL $\Psi$ is defined as a triple $(\mathcal{F}, \overline{\mathcal{C}}, \mathcal{T})$, where $\mathcal{F}$ is the scope, $\overline{\mathcal{C}}$ is the platform and $\mathcal{T}$ is the traceability relation.

The representation of specification and platform is semantic in nature. Syntactic representation of these may use FODA diagrams, MaMs, or a variety of notations in the literature. In general, one can have implicit representations through constraints on the features and components; we will adopt this view in the following sections.
In the ECPL case study, $\mathcal{F}$ contains the nine features of Figure 1 and the ECPL scope $\overline{\mathcal{F}}$ contains eight specifications. For illustration, we choose the following specifications: $\text{spec}_1 = \{\text{Power lock, } f_{\text{Automatic}}\}$ and $\text{spec}_2 = \{\text{Power lock, } f_{\text{Automatic}}, \text{Door lock, Shift out of park, Door relock}\}$. The top-most feature Entry control is in every specification and is not mentioned explicitly.

In ECPL, $\mathcal{C}$ contains the three components of Figure 2 and the twelve interconnections which are also modeled as components. Note that the mandatory interconnections are in every architecture and are not mentioned explicitly. The ECPL platform $\mathcal{C}$ contains nine architectures which can be extracted from the ECPL platform. Again, for illustration, we select two architectures $\text{arch}_1 = \{\text{Door lock manager}\}$ or $\text{arch}_2 = \{\text{Door lock manager, Power lock, } c_{\text{Automatic}}, \text{Auto lock, Transmission in park}\}$.

The traceability relation in ECPL is given through the Tables $\text{I}(\text{req}(.))$ and $\text{II}(\text{prov}(.))$. For example, the Auto lock component provides the features Door lock and Door relock. Each of these features requires only Auto lock component.

The main concept of implementability in $\Psi$ is defined as follows: a feature is implemented by an architecture (set of components in $\mathcal{C}$) if the architecture provides the feature and simultaneously fulfills the mandatory requirements of the feature.

**Definition 2** (Implements). Given an SPL $\Psi = (\mathcal{F}, \mathcal{C}, \mathcal{T})$, $\text{implements}_\Psi(C, f)$ if $\exists C_1 \in \text{prov}(f), C_2 \in \text{req}(f), C_2 \subseteq C_1 \subseteq C$.

The set of features implemented by an architecture $C$ is defined as $\text{Provided}_\Psi(C) = \{f | \text{implements}_\Psi(C, f)\}$.

In ECPL, $\text{implements}_\Psi(\text{spec}_2, \text{Power lock})$ holds but $\text{implements}_\Psi(\text{spec}_1, \text{Power lock})$ does not hold. Moreover, if one considers prov as given in Table II without the last line, $\text{implements}_\Psi(\text{arch}, f_{\text{Speed}})$ never holds for any architecture $\text{arch}$ because $\text{prov}(f_{\text{Speed}}) = \emptyset$ even if $\text{req}(f_{\text{Speed}}) = \{(c_{\text{Speed}})\}$.

With the basic definitions above, we can now define when an architecture exactly implements a specification.

**Definition 3** (Realization). Given $C \in \mathcal{C}$ and $F \in \mathcal{F}$, $\text{Realizes}(C, F)$ if $F = \text{Provided}_\Psi(C)$.

Due to the required equality, we have the following easy result.

**Proposition 4.** An architecture realizes at most one specification in an SPL.

The realizes definition in the above imposes a strictness on the implementations. Thus, in the ECPL example, the architecture $\text{arch}_2$ realizes the specification $\text{spec}_2$, but it does not realize $\text{spec}_1$ even though it provides the implementation of all the features of $\text{spec}_1$. In many cases, this may be a practical definition. Hence, we relax the definition of realization in the following.

**Definition 5** (Covers). Given $C \in \mathcal{C}$ and $F \in \mathcal{F}$, $C$ covers $F$ if $\text{Provided}_\Psi(C) \subseteq F \subseteq \text{Provided}_\Psi(C)$.

The additional condition $(\text{Provided}_\Psi(C) \subseteq F)$ is added to ensure that the chosen $C$ provides the implementation of a specification in the scope. In ECPL, $\mathcal{C}_2$ covers $\mathcal{F}_1$ but $\mathcal{C}_1$ does not cover (or even realize) anything.

Given $F, F' \in \mathcal{F}$, let $F \subseteq F'$. Then, $F'$ is called the extension of $F$. The following simple proposition establishes a connection between the relations realizes and covers.

**Proposition 6.** Given $C \in \mathcal{C}$ and $F \in \mathcal{F}$ and $C$ covers $F$. Then, there is an extension $F'$ of $F$ in $\mathcal{F}$ such that $\text{Realizes}(C, F')$. Hence, if there is no extension of $F$ in $\mathcal{F}$, then $\text{Realizes}(C, F)$.

In the ECPL case study, $\text{arch}_2$ covers $\text{spec}_1$, $\text{spec}_2$ extends $\text{spec}_1$, and $\text{arch}_2$ realizes $\text{spec}_2$.

The set of products of the SPL are now defined as the specifications and the architectures implementing them through the traceability relation.

**Definition 7** (SPL Products). Given an SPL $\Psi = (\mathcal{F}, \mathcal{C}, \mathcal{T})$, the products of the SPL denoted as $\text{Prod}(\Psi) \equiv \{(F, C) | C \in \mathcal{C}, F \in \mathcal{F}, C \subseteq \mathcal{C}\}$.

In the ECPL, out of 8 specifications and 9 architectures, there are 11 products. Even if the architecture $\text{arch}_3 = \{\text{Door lock manager, Power lock, } c_{\text{Manual}}, \text{Auto lock, Transmission in park}\}$ “covers” the specification $\{\text{Power lock, } f_{\text{Manual}}\}$, this pair is not a product because $\text{Provided}_\Psi(\text{arch}_3)$ is not in the scope $\mathcal{F}$.

This is because $\text{arch}_3$ provides features $f_{\text{Manual}}$ and $\text{Shift out of park}$ which should be exclusive.

**C. SPL Level Properties**

Given an SPL $(\mathcal{F}, \mathcal{C}, \mathcal{T})$, we define two important relationships between the scope (specification space) and platform (architecture, or implementation, space).

1) Completeness: An SPL $(\mathcal{F}, \mathcal{C}, \mathcal{T})$ is complete if $\forall F \in \mathcal{F}, \exists C \in \mathcal{C}, \text{Covers}(C, F)$.

The completeness property of the SPL determines if the platform for the SPL is adequate to provide implementation for all the specifications in its scope.
The ECPL is complete. For illustration’s sake, let us omit
the last entry in Table I. Then, none of the specifications
which include the feature \( f \_Speed \) is realizable because \( f \_Speed \) cannot be derived from any component.

2) Soundness: An SPL \((\mathcal{F}, \mathcal{C}, \mathcal{T})\) is sound if for all \( C \in \mathcal{C} \cdot \exists F \in \mathcal{F} \cdot \text{Covers}(C, F)\).

The soundness property relates to the non-redundancy
of the platform in an SPL. If the architectures (sets of components) are generated using certain rules or constraints,
soundness stipulates that only those architectures which pro-
vide an implementation of some specification are generated.

The ECPL is not sound because, for example, the arch-
itecture \( arch_1 \) does not realay any specification (feature
set). This is the case with all the architecture where \( Power\_lock \) is absent. Now, let us assume that the com-
ponent \( Power\_lock \) is mandatory. The ECPL is still not
sound because of \( arch_3 \) only. If \( arch_3 \) is omitted from the
platform, the remaining ECPL become sound.

3) Existentially Explicit: Given an SPL, and a specifica-
tion \( F \in \mathcal{F} \), it is called an existentially explicit specification in
the SPL if there exists a \( C \in \mathcal{C} \cdot \text{Realizes}(C, F) \).

In ECPL, \( spec_1 \) and \( spec_2 \) are existentially explicit. However, another specification \( spec_3 = \{\text{Power\_lock, f\_Automatic, Door\_lock, Shift\_out\_of\_park}\} \) is not, be-
cause none of the architecture realizes a specification with
\( Door\_lock \) and without \( Door\_lock\).

4) Universally Explicit: Given an SPL, and a specifica-
tion \( F \in \mathcal{F} \), it is called a universally explicit specification in
the SPL if (i) there exists a \( C \in \mathcal{C} \cdot \text{Realizes}(C, F) \) and
(ii) for all \( C \in \mathcal{C} \cdot \text{Covers}(C, F) \Rightarrow \text{Realizes}(C, F) \).

In ECPL, \( spec_2 \) is universally explicit. \( spec_1 \) is exist-
tentially explicit but not universally explicit because it is
covered but not realized by the \( arch_2 \).

It follows from Proposition 3 that

**Proposition 8.** If \( F \in \mathcal{F} \) is covered by some architecture
but is not extendable, then it is universally explicit. If \( F \)
is universally explicit, then none of its extensions has a
covering architecture.

In the ECPL, \( spec_2 \) is covered and cannot be extended; so
it is universally explicit. On the contrary, if a specification
has an extension which is covered, the same also covers the
extended specification.

5) Unique Implementation: A given specification may
be implemented by multiple architectures. This may be a
desirable criterion of the platform from the perspective of
optimization among various choices. Thus the specifications
which are implemented by single architectures are to be
identified. \( F \in \mathcal{F} \) has a unique implementation if \( \exists C \in \mathcal{C} \cdot \text{Covers}(C, F) \land \forall C' \in \mathcal{C} \cdot \text{Covers}(C', F) \Rightarrow C = C' \).

In ECPL, each specifications including \( Door\_lock\) has a
unique implementation. On contrary, \( spec_1 \) has more than
one implementation.

6) Common, live and dead elements: Identification of
common, live and dead elements in an SPL is one of the
basic analyses identified in the SPL community. We redefine
these concepts in terms of the our notion of products.

1) An element \( e \) is common if \( \forall (F, C) \in \text{Prod}(\Psi) \cdot e \in F \cup C \).

2) An element \( e \) is live if \( \exists (F, C) \in \text{Prod}(\Psi) \cdot e \in F \cup C \).

3) An element \( e \) is dead if \( \forall (F, C) \in \text{Prod}(\Psi) \cdot e \notin F \cup C \).

In ECPL, the feature \( Manual\_lock \) is dead. All the other
features are live. The component \( Door\_lock\) manager is com-
mon.

7) Superfluous Component: A component is superfluous
if the platform without the component suffices to provide
the same set of specifications.

Let \( P \subseteq \text{Prod}(\Psi) \), \( \text{spec}(P) = \{F|(F, C) \in P\} \). Let \( \text{Prod}_{\neg e}(\Psi) = \{(F, C)|(F, C) \in \text{Prod}(\Psi) \land (e \notin C)\} \). \( e \) is
Superfluous if \( \text{spec}(\text{Prod}(\Psi)) = \text{spec}(\text{Prod}_{\neg e}(\Psi)) \).

Superfussiness is relative to a given platform. If in an
SPL \( \Psi \), \( \text{prov}(f) = \{\{a\}, \{b\}\}, \mathcal{F} = \{\{\}\} \) and \( \mathcal{C} = \{\{a\}, \{b\}\} \), then both \( a \) and \( b \) are superfluous w.r.t. \( \Psi \),
whereas if either \( \{a\} \) or \( \{b\} \) is removed from the platform,
the remaining \( \{b\} \) or \( \{a\} \) is not superfluous anymore (w.r.t.
the reduced SPL).

**Lemma 9.** Let \( c \in C \) be Superflus for \( \Psi \). Then, for every
\( C \in \mathcal{C} \cdot C \Rightarrow (\exists C' \in \mathcal{C} \cdot c \notin C' \land \text{Provided\_by}(C) = \text{Provided\_by}(C')) \).

8) Redundant Component: A component is redundant if
it is not contributing to any feature in any architecture in
the platform. \( c \in C \) is redundant if for every \( C \in \mathcal{C} \cdot c \in C \Rightarrow (\exists C' \in \mathcal{C} \cdot c \notin C' \land \text{Provided\_by}(C) = \text{Provided\_by}(C')) \).

Note that redundancy is a stronger version of superflu-
ousness; a redundant component is superfluous whereas
a superfluous element many not be redundant.

In ECPL, no component is neither superfluous nor re-
dundant. Let us assume that we have a component called
\( Door\_Relock\_Alt \) such that \( \{Door\_Relock\_Alt, Auto\_lock\} \) provides the feature \( Door\_Relock\). This component would be redundant because \( Auto\_lock\) already provides the feature
\( Door\_Relock\).

It is expected that an SPL can be optimized by omitting
the redundant components without affecting the set of prod-
ucts.

**Lemma 10.** Let \( c \in C \) be redundant. Construct a SPL
\( \Psi' = (\mathcal{F}, \mathcal{T}', \mathcal{C}) \) where, \( \mathcal{T}' \) be a traceability relation with
\( \text{req}'(f) = \text{req}(f) \setminus \{C|c \in C\} \) and \( \text{prov}'(f) = \text{prov}(f) \setminus \{C|c \in C\} \). Then, \( \text{Prod}(\Psi) = \text{Prod}(\Psi') \).

9) Critical Component: Given an \( f \in \mathcal{F} \), a compo-
nent \( c \) is critical for \( f \) if for all \( C \in \mathcal{C} \cdot (c \notin C \Rightarrow \lnot\text{implements}_\Psi(C, f)) \).
In ECPL, all the components are critical. Let us assume a component $\text{Auto lock}_\text{Alt}$ which is an alternative to $\text{Auto lock}$ and also provides the feature $\text{Door lock}$. In such case neither $\text{Auto lock}$ or $\text{Auto lock}_\text{Alt}$ are critical for the feature $\text{Door lock}$ but $\text{Auto lock}$ remains critical for the feature $\text{Auto relock}$.

10) Emerging Features: When a specification is not realizable, but is covered by one or more architectures, the emerging features $\text{Emerging}(F) \equiv \{(C, \text{Provided by}(C \setminus F)) \mid \text{Covers}(C, F)\}$. $\text{Emerging}(F)$ gives the covering architectures and the emerging features corresponding to the architecture.

In ECPL, while considering the only architecture that covers $\langle \text{Power lock, Manual, Door lock, f\_speed} \rangle$, $\text{Door relock}$ will emerge.

D. Canonical Traceability Relation

A given traceability relation can be reduced to a canonical form without affecting the set of features implementable in the SPL. We define the canonical form in the following.

**Definition 11.** $T$ is non-redundant if for every feature $f$, 
1) $C_i, C_j \in \text{prov}(f), i \neq j$ implies $C_i \not\subseteq C_j$, and
2) $C_i, C_j \in \text{req}(f), i \neq j$ implies $C_i \not\subseteq C_j$.

Intuitively, if a smaller set of components implements a feature, a larger set also will. On the other hand, if a larger set of components is required to implement a feature, a smaller set is required automatically. Given a traceability relation, one can check if it is non-redundant and convert it to a non-redundant relation by removing the larger (resp. smaller) sets in $\text{prov}(f)$ (resp. $\text{req}(f)$).

**Definition 12.** $T$ is internally consistent if $\forall f \in \mathcal{F}, \forall C \subseteq \mathcal{C}, (C \in \text{prov}(f) \Rightarrow (\exists C' \in \text{req}(f) \cdot C' \subseteq C))$.

Intuitively, internal consistency of a traceability relation states that each set of components in $\text{prov}(f)$ can indeed satisfy the mandatory requirements (coming from $\text{req}(f)$) of $f$.

Given a traceability relation, we can reduce it to a canonical form by the following operations for the $\text{prov}()$ and $\text{req}()$ of each feature $f$.

**Claim 13.** For a given SPL $\Psi = (\mathcal{F}, \mathcal{C}, T)$, the above procedure results in a canonical traceability relation $T'$ such that for all $C \subseteq \mathcal{C}$, $\text{implcements}_{\Psi'}(C, f)$ implements$_{\Psi'}(C, f)$.

**Proof:** The canonization algorithm stops when no rules are applicable. Then the conditions of the rules ensure that the resulting traceability relation is canonical.

In order to prove the preservation of implementability, it is easy to show that each rule preserves implementability.

**Theorem 14.** If $\Psi$ is an SPL with a canonical traceability relation, implements$_{\Psi'}(C, f)$ if $\exists C_1 \in \text{prov}(f) \cdot C_1 \subseteq C$.

**Algorithm 1** Canonization of Traceability Relation

1: if $\text{prov}(f) = \emptyset$ or $\text{prov}(f)$ is undefined then
2: $\text{prov}(f) \leftarrow \bot$; $\text{req}(f) \leftarrow \bot$
3: end if
4: if $C_i, C_j \in \text{prov}(f), i \neq j, C_i \subseteq C_j$ then
5: $\text{prov}(f) \leftarrow \text{prov}(f) \setminus \{C_i\}$
6: end if
7: if $C_i, C_j \in \text{req}(f), i \neq j, C_i \subseteq C_j$ then
8: $\text{req}(f) \leftarrow \text{req}(f) \setminus \{C_i\}$
9: end if
10: if $C \in \text{prov}(f)$, but $\forall C_i \in \text{req}(f), C_i \not\subseteq C$ then
11: $\text{prov}(f) \leftarrow \text{prov}(f) \setminus \{C\}$
12: end if

| Short-Hand | Feature               |
|------------|-----------------------|
| $F_1$      | Manual Lock           |
| $F_2$      | Power Lock            |
| $F_3$      | Door Lock             |
| $F_4$      | Door Relock           |
| $F_5$      | $F\_\text{automatic}$ |
| $F_6$      | $F\_\text{manual}$   |
| $F_7$      | $F\_\text{speed}$    |
| $F_8$      | Shift out of Park     |

Table III

**FEATURES IN ECPL.**

Proof: In a canonical traceability relation, due to internal consistency, for every $C' \in \text{prov}(f), \exists C'' \in \text{req}(f) \cdot C'' \subseteq C'$. Hence the result.

Since one can always canonize the traceability relation of an SPL, henceforth we will assume that the SPL under scope is canonical. Thereby, the definition of implementation will henceforth be as given in [14].

IV. ANALYSIS OF THE ECPL

In this section, we analyze some properties of the ECPL example using QuBE.

In ECPL, there are total 8 Features and 13 Components. The features are listed in Table III and the components are given in Table IV.

A specification is a subset of Features $\mathcal{F}$. The scope of an SPL is a collection of specifications: $\mathcal{F} \subseteq \wp(\mathcal{F})$. In our example, scope of ECPL is $\mathcal{F} = \{S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8\}$. All the specifications are represented in tabular form as shown in Table V. A specification corresponds to a column and the 1’s in the column select the features in the specification.

1) $S_1 = \{\text{Power Lock, F\_automatic}\}$
2) $S_2 = \{\text{Power Lock, F\_manual}\}$
3) $S_3 = \{\text{Power Lock, F\_automatic, Door Lock, F\_speed}\}$
4) $S_4 = \{\text{Power Lock, F\_manual, Door Lock, F\_speed}\}$
An architecture is a subset of components $C$. An SPL platform consists of a set of architectures: $\mathcal{C} \subseteq \wp(C)$. In ECPL, the platform is $\mathcal{C} = \{ A_1, A_2, A_3, A_4, A_5, A_6, A_7, A_8, A_9 \}$. The architectures are represented in Table VI.

1) $A_1 = \{ \text{Door Lock Manager, Unlock Driver Door, Unlock all doors, Lock all doors} \}$
2) $A_2 = \{ \text{Door Lock Manager, Unlock Driver Door, Unlock all doors, Lock all doors, Auto Lock, C\_speed} \}$
3) $A_3 = \{ \text{Door Lock Manager, Unlock Driver Door, Unlock all doors, Lock all doors, Auto Lock, C\_speed} \}$
4) $A_4 = \{ \text{Door Lock Manager, Unlock Driver Door, Unlock all doors, Lock all doors, Power Lock, Courtesy switch, Key signal, Sill door signal, C\_automatic} \}$
5) $A_5 = \{ \text{Door Lock Manager, Unlock Driver Door, Unlock all doors, Lock all doors, Power Lock, Courtesy switch, Key signal, Sill door signal, C\_manual} \}$
6) $A_6 = \{ \text{Door Lock Manager, Unlock Driver Door, Unlock all doors, Lock all doors, Auto Lock, C\_speed, Power Lock, Courtesy switch, Key signal, Sill door signal, C\_automatic} \}$
7) $A_7 = \{ \text{Door Lock Manager, Unlock Driver Door, Unlock all doors, Lock all doors, Auto Lock, C\_speed, Power Lock, Courtesy switch, Key signal, Sill door signal, C\_manual} \}$
8) $A_8 = \{ \text{Door Lock Manager, Unlock Driver Door, Unlock all doors, Lock all doors, Auto Lock, C\_speed, Power Lock, Courtesy switch, Key signal, Sill door signal, C\_manual} \}$
9) $A_9 = \{ \text{Door Lock Manager, Unlock Driver Door, Unlock all doors, Lock all doors, Auto Lock, Gear in park, Power Lock, Courtesy switch, Key signal, Sill door signal, C\_manual} \}$

The traceability relations (provides and requires) are as in Tables I and II. We reproduce the tables here for ease of reference.

![Table IV](image-url)

**Components in ECPL.**

| Short-Hand | Component                      |
|------------|--------------------------------|
| $C_1$      | Door Lock Manager             |
| $C_2$      | Unlock Driver Door            |
| $C_3$      | Unlock all doors              |
| $C_4$      | Lock all doors                |
| $C_5$      | Auto Lock                     |
| $C_6$      | Power Lock                    |
| $C_7$      | Courtesy switch               |
| $C_8$      | Key signal                    |
| $C_9$      | Sill door signal              |
| $C_{10}$   | C\_automatic                  |
| $C_{11}$   | C\_manual                     |
| $C_{12}$   | Gear in park                  |
| $C_{13}$   | C\_speed                      |

5) $S_5 = \{ \text{Power Lock, F\_automatic, Door Lock, Shift out of Park} \}$
6) $S_6 = \{ \text{Power Lock, F\_automatic, Door Lock, F\_speed, Door relock} \}$
7) $S_7 = \{ \text{Power Lock, F\_manual, Door Lock, F\_speed, Door relock} \}$
8) $S_8 = \{ \text{Power Lock, F\_automatic, Door Lock, Shift out of Park, Door relock} \}$

![Table V](image-url)

**Specifications in tabular form.**

| Specifications | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | $S_8$ |
|----------------|------|------|------|------|------|------|------|------|
| $F_1$          |      |      |      |      |      |      |      |
| $F_2$          | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| $F_3$          | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| $F_4$          | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| $F_5$          | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| $F_6$          | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| $F_7$          | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| $F_8$          | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |

![Table VI](image-url)

**Architectures in tabular form.**

| Architectures | $A_1$ | $A_2$ | $A_3$ | $A_4$ | $A_5$ | $A_6$ | $A_7$ | $A_8$ | $A_9$ |
|---------------|------|------|------|------|------|------|------|------|------|
| $C_1$         | 1    |      |      |      |      |      |      |      |      |
| $C_2$         |      | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| $C_3$         | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| $C_4$         | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| $C_5$         | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| $C_6$         | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| $C_7$         |      | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| $C_8$         |      |      | 1    | 1    | 1    | 1    | 1    | 1    | 1    |
| $C_9$         |      |      |      | 1    | 1    | 1    | 1    | 1    | 1    |
| $C_{10}$      |      |      |      | 1    | 1    | 1    | 1    | 1    | 1    |
| $C_{11}$      |      |      |      |      | 1    | 1    | 1    | 1    | 1    |
| $C_{12}$      |      |      |      |      |      | 1    | 1    | 1    | 1    |
| $C_{13}$      |      |      |      |      |      |      | 1    | 1    | 1    |

![Table VII](image-url)

**Requires relation in ECPL.**

| Feature | Component                      |
|---------|--------------------------------|
| Power lock | Door lock manager& Power lock |
| Door lock | Auto lock                     |
| Door relock | C\_automatic              |
| F\_automatic | C\_manual                |
| F\_speed | Gear in Park                  |
| Shift out of Park | C\_speed                |
### Table VIII
PROVIDES RELATION IN ECPL

| Component/Interconnection       | Feature                |
|--------------------------------|------------------------|
| Door lock manager & Power lock | Power lock             |
| C_{automatic}                  | F_{automatic}          |
| C_{manual}                     | F_{manual}             |
| Auto lock                      | Door lock & Door relock|
| Gear in park                   | Shift out of park      |
| C_{speed}                      | F_{speed}              |

### Table IX
FEATURE IMPLEMENTATION IN GIVEN SPL.

| Architectures | A_1 | A_2 | A_3 | A_4 | A_5 | A_6 | A_7 | A_8 | A_9 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| F_1           | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| F_2           |     |     |     |     |     |     |     |     |     |
| F_3           |     |     |     |     |     |     |     |     |     |
| F_4           |     |     |     |     |     |     |     |     |     |
| F_5           |     |     |     |     |     |     |     |     |     |
| F_6           |     |     |     |     |     |     |     |     |     |
| F_7           |     |     |     |     |     |     |     |     |     |
| F_8           |     |     |     |     |     |     |     |     |     |

### Table X
SPECIFICATIONS AND THE REALIZING ARCHITECTURES.

| Architectures | A_1 | A_2 | A_3 | A_4 | A_5 | A_6 | A_7 | A_8 | A_9 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| S_1           | 1   |     |     |     |     |     |     |     |     |
| S_2           | 1   |     |     |     |     |     |     |     |     |
| S_3           |     | 1   |     |     |     |     |     |     |     |
| S_4           |     | 1   |     |     |     |     |     |     |     |
| S_5           |     |     |     |     |     |     |     | 1   |     |
| S_6           |     |     |     |     |     |     |     |     | 1   |
| S_7           |     |     |     |     |     |     |     |     |     |
| S_8           |     |     |     |     |     |     |     |     |     |

### Table XI
SPECIFICATIONS AND THEIR COVERING ARCHITECTURES.

Solution: Let P_1 = prov(Power Lock). From Table I, P_1 = prov(Power Lock) = \{Door Lock Manager, Power Lock\}. Let R_1 = req(Power Lock). From Table I, R_1 = req(Power Lock) = \{Door Lock Manager, Power Lock\}. Since R_1 ⊆ P_1 ⊆ A_4, implements(A_4, Power Lock) holds. On other hand, R_1 ⊆ P_1 ⊆ A_1, hence implements(A_1, Power Lock) does not hold.

For each feature, we can find the architectures which implement it. The results are listed in Table IX the 1’s in the column corresponding to an architecture gives us the features implemented.

Realization: Given A ∈ C and S ∈ F, Realizes(A, S) if S = Provided by(A).

Example: In ECPL, check if Realizes(A_4, S_1) holds.

Solution: The specification S_1 has the features \{Power Lock, F_{automatic}\}. From Table IX Provided by(A_4) = \{Power Lock, F_{automatic}\}. Since Provided by(A_4) = S_1, Realizes(A_4, S_1) holds. On the other hand, Provided by(A_5) = \{Power Lock, F_{manual}\} ≠ S_1, hence Realizes(A_5, S_1) does not hold.

The Table X shows all the specifications and it’s corresponding realized architectures.

Covers: Given A ∈ C and S ∈ F, A covers S if Provided by(A) ∈ F ∧ S ⊆ Provided by(A).

Example: In ECPL, check Covers(A_6, S_1) Hold?

Solution: The specification S_1 has \{Power Lock, F_{automatic}\} features. From Table IX Provided by(A_6) = \{Power Lock, Door Lock, Door Relock, F_{automatic}\}. Since Provided by(A_6) ∈ F and S_1 ⊆ Provided by(A_6), hence Covers(A_6, S_1) hold. On the other hand, Provided by(A_5) = \{Power Lock, F_{manual}\} ∈ F but S_1 ⊈ Provided by(A_5), hence Covers(A_5, S_1) does not hold.

Similarly, for all other specifications we can find the architectures which cover the specifications. The Table XI has all the specifications and their covering architectures.

### A. SPL Level Properties of ECPL

Completeness: In ECPL, from Table XI one can observe that every specification in scope F is covered by some architecture in platform C. Hence, ECPL is complete.

Soundness: From Table XI one can observe that the architectures S_1, S_2 and S_3 do not cover any specification in scope F. Hence, ECPL is not sound.

Existentially Explicit: It is observed from Table X that the architectures S_1, S_2, S_6, S_7 and S_8 are realized by the architectures A_4, A_5, A_6, A_7 and A_8 respectively. Hence these specifications are existentially explicit. From the same table, one can observe that the specifications S_3, S_4 and S_5 are not realized by any architecture in the given platform.

Universally Explicit: In ECPL, from Table X and XI it is observed that the specifications S_6, S_7 and S_8 are realized by the architectures A_6, A_7 and A_8 respectively, and these are the only architectures which cover the respective specifications. Hence, these specifications are universally explicit. As we have already seen from Table X the architectures S_3, S_4 and S_5 are not realized at all. The remaining architectures S_1 and S_2 are realized by A_4 and A_5 respectively, but S_1 is also strictly covered (covered but not realized) by architectures A_6 and A_7 and S_2 is strictly covered by A_7. Hence, the specifications S_1, S_2, S_3, S_4 and S_5 are not universally explicit.
**Unique Implementation:** In an SPL, a given specification is said to be uniquely implemented if it is covered by exactly one architecture. In ECPL, from Table XI it is found that the specifications $S_3$, $S_4$, $S_5$, $S_6$, $S_7$ and $S_8$ are covered by exactly one architecture ($A_6$, $A_7$, $A_8$, $A_6$, $A_7$, $A_8$ respectively). Hence, these specifications have unique implementation. On the other hand, the specifications $S_1$ and $S_2$ have multiple implementations.

**Products:** In ECPL, from Table XI we get $Prod(\Psi) = \{\langle S_1, A_4 \rangle, \langle S_1, A_6 \rangle, \langle S_1, A_8 \rangle, \langle S_2, A_5 \rangle, \langle S_2, A_7 \rangle, \langle S_3, A_6 \rangle, \langle S_4, A_7 \rangle, \langle S_5, A_8 \rangle, \langle S_6, A_6 \rangle, \langle S_7, A_7 \rangle, \langle S_8, A_8 \rangle\}$.

**Common, live and dead elements:** From the set of products and referring to the tables and XI we find the common elements of ECPL are \{Power Lock$^1$, Door Lock Manager, Unlock Driver Door, Unlock all doors, Lock all doors, Power Lock$^2$, Courtesy switch, Key signal, Sill door signal\}. Power Lock$^1$ is the feature and Power Lock$^2$ is the component.

The live elements for $Prod(\Psi)$ are \{Power Lock$^1$, Door Lock, Door Relock, F\_automatic, F\_manual, F\_speed, Shift out of Park, Door Lock Manager, Unlock Driver Door, Unlock all doors, Lock all doors, Power Lock$^2$, Courtesy switch, Key signal, Sill door signal\}. The only dead element is Manual Lock.

**Superfluous Component:** There are no superfluous components in ECPL. For example, consider the element AutoLock. The specification $S_1$ is covered by architectures $A_4$, $A_6$, and $A_8$. If architectures $A_4$, $A_6$ and $A_8$ are removed, then $S_1$ is still in the product (being implemented by $A_4$). However, $A_6$ is the only architecture covering $S_3$. Hence, when $A_6$ is removed, $\langle S_3, A_6 \rangle$ is removed from the list of products. This implies that AutoLock is not superfluous.

**Redundant Component:** A component is redundant if it is not contributing to any feature in any architecture in the platform. In ECPL, there are not any redundant component. Let us assume we have a component called Door Relock$_{Alt}$ such that $\{\text{Door Relock}_{Alt}, \text{Auto Lock}\}$ provides the feature Door Relock. This component would be redundant because AutoLock already provide the feature Door Relock.

**Critical Component:** In ECPL, all the components are critical. Let us remove the component C\_automatic from architecture $A_4$. Then, $\text{implements}_{[A_4, F\_\text{automatic}]}$ will not hold. Hence, we can say that the component C\_automatic is critical for feature F\_automatic.

**Emerging Features:** In ECPL, the specification $S_4$ is not realized by any architecture but it is covered by $A_7$. So the set of emerging features is $\text{Provided by}(A_7) - S_4 = \{\text{Door relock}\}$.

| Properties and Formulae | Test 1 | Test 2 | Test 3 | Average Time(ms) |
|-------------------------|-------|-------|-------|------------------|
| Implements              | 3     | 2     | 2     | 2.33             |
| realizes                | 2     | 2     | 2     | 2                |
| covers                  | 3     | 2     | 2     | 2.33             |
| complete                | 3     | 2     | 2     | 2.33             |
| sound                   | 4     | 3     | 3     | 3.33             |
| existentially explicit  | 3     | 2     | 3     | 2.61             |
| critical                | 3     | 3     | 3     | 3                |
| extended features       | 2     | 2     | 2     | 2                |

**Table XII**

**TIME COMPLEXITY FOR PROPERTIES AND FORMULAE**

**B. Performance**

We have recorded the time required to check the satisfiability of the formulae for some analysis problems using QuBE (Refer Table XII). Each formula has been run three times and the average time is calculated. The performance of QuBE seems quite good for small SPLs the size of ECPL.

**V. ANALYSIS BETWEEN THE SPECIFICATION AND THE IMPLEMENTATION PERSPECTIVES**

In the literature, different analysis problems in SPL are usually encoded as propositional satisfiability problems and SAT solvers such as Yices, Bddsolve etc. are used to solve the problems. However, looking at the definition of implements and the subsequent problems, we observe that there is quantification over the features and components which can be encoded as propositions. In fact, we show in the following that it is possible to transform the analysis problems of the previous section into QBF formula such that the questions have an affirmative answer iff the corresponding QBF formulae hold.

1) Let $C = \{c_1, \ldots , c_n\}$ be the set of all components and let $F = \{f_1, \ldots , f_m\}$ be the set of all features. A subset of $F$ is a specification, while a subset of $C$ is called an architecture. A platform is a set of architectures $\mathcal{P} \subseteq \mathcal{P}(C)$. A scope is a set of specifications $\mathcal{F} \subseteq \mathcal{P}(F)$.

2) Given an architecture $C = \{c_1, \ldots , c_k\}$, let $\text{Prop}(C)$ be the tuple of propositions $\text{Prop}(C)(i) = \begin{cases} c_i & \text{if } c_i \in C \\ \neg c_i & \text{if } c_i \notin C \end{cases}$

Thus, $\text{Prop}(C)$ is an n-tuple made up of 0’s and 1’s. The tuple $\text{Prop}(F)$ for a specification $F$ can be defined similarly.

3) Let $f$ be a feature. Let $\text{prov}(f) = \{S_1, S_2, \ldots , S_k\}$. Each $S_j$ is a set of components that provides $f$. Then we define $\text{formula}_\text{prov}(f)$ as $\bigvee_{j} \bigwedge_{c \in S_j} c_i$. $\text{formula}_\text{prov}(f)$ is satisfiable whenever there is some set $S_j$ of components that provide feature $f$. If the set $\text{prov}(f)$ is undefined(empty), then $\text{formula}_\text{prov}(f)$ is FALSE, since there are no components that provide feature $f$. 


4) Let \( f \) be a feature. Let \( \text{req}(f) = \{S_1, S_2, \ldots, S_k\} \).
\( f \) requires at least one set \( S_j \) of components for its implementation. Then, we define \( \text{formula\_req}(f) = \bigvee_j \bigwedge_{c_i \in S_j} c_i \). \text{formula\_req}(f) is satisfiable iff \( \text{req}(f) \) has at least one set (say \( S_j \)) of its required components. If \( \text{req}(f) \) is empty or undefined, then \( \text{formula\_req}(f) \) is TRUE, since there are no requirements for \( f \).

5) Let \( f \) be a feature and let \( \text{prov}(f) = \{S_1, S_2, \ldots, S_k\} \).
Given a tuple of component parameters \( (c'_1, \ldots, c'_n) \) where each \( c'_i \) is 0 or 1, and a feature \( f \), we define the formula \( f\_\text{implements}(c'_1, \ldots, c'_n, f) \) as

\[
\forall c_1 \ldots c_n \left( \bigwedge_{i=1}^n (c'_i \Rightarrow c_i) \right) \Rightarrow \text{formula\_prov}(f)
\]

Whenever the truth values of \( c_i \) agree with those of the variables of some \( S_j \) in \( \text{prov}(f) \), or correspond to a superset of some \( S_j \) in \( \text{prov}(f) \), the formula \( \text{formula\_prov}(f) \) will hold.

6) Let \( F = \{f_1, f_2, \ldots, f_l\} \) be a specification. For each \( f_i \), let \( \text{prov}(f_i) = \{S_1, \ldots, S_k\} \) be defined. Consider a tuple of component parameters \( (c'_1, \ldots, c'_n) \) and a tuple of feature parameters \( (f'_1, \ldots, f'_m) \).
Here again, each \( c'_i, f'_i \) is a zero or a 1. Define \( f\_\text{covers}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_m) \) as

\[
\bigwedge_{i=1}^m (f'_i \Rightarrow f\_\text{implements}(c'_1, \ldots, c'_n, f_i))
\]

Define \( f\_\text{realizes}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_m) \) as

\[
\bigwedge_{i=1}^m (f'_i \Leftarrow f\_\text{implements}(c'_1, \ldots, c'_n, f_i))
\]

7) Let \( \Psi = (\mathcal{F}, \overline{c}, \mathcal{T}) \) be an SPL. Let \( \overline{c} = \{S_1, \ldots, S_k\} \).
Given a tuple of component parameters \( (c'_1, \ldots, c'_n) \) where each \( c'_i \) is 0 or 1, the predicate \( C_f(c'_1, \ldots, c'_n) \) is defined as

\[
\bigvee_j \bigwedge_{c_i \in \text{Prop}(S_j)} c'_i
\]

Then \( C_f(c'_1, \ldots, c'_n) \) is satisfied iff \( \{c'_k \mid c'_k = 1\} = S_k \) for some \( S_k \in \overline{c} \). \( C_f(f'_1, \ldots, f'_m) \) is defined similarly.

**Lemma 1.** (Internal Consistency of Traceability) Consider a canonical SPL. Let \( TCF \), the trace consistency formula be defined as \( \forall c_1 \ldots c_n \\\\bigwedge_{f \in \mathcal{F}} (f\_\text{prov}(f) \Rightarrow f\_\text{req}(f)) \). Then, \( \mathcal{T} \) is internally consistent iff \( TCF \) is true.

**Lemma 2.** (Implements) Given a canonical SPL, a set of components \( C \), and a feature \( f \), \( f\_\text{implements}(C, f) \) iff \( f\_\text{implements}(c'_1, \ldots, c'_n, f) \) where \( \text{Prop}(C) = (c'_1, \ldots, c'_n) \).

**Lemma 3.** (Realizes, Covers) Given a set of components \( C \) and a set of features \( F \), let \( \text{Prop}(C) = (c'_1, \ldots, c'_n) \) and \( \text{Prop}(F) = (f'_1, \ldots, f'_m) \). Then the following statements hold:

1) \( C \) covers \( F \) iff \( f\_\text{covers}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_m) \)
2) \( C \) realizes \( F \) iff \( f\_\text{realizes}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_m) \)

**Lemma 4.** (Completeness, Soundness) Given an SPL, the SPL is complete iff

\[
\forall f'_1 \ldots f'_m [C_f(f'_1, \ldots, f'_m) \Rightarrow \exists c'_1 \ldots c'_n [C_1(c'_1, \ldots, c'_n) \land f\_\text{covers}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_m)]
\]

Given an SPL, the SPL is sound iff

\[
\forall c'_1 \ldots c'_n [C_1(c'_1, \ldots, c'_n)] \Rightarrow \exists f'_1 \ldots f'_j [C_f(f'_1, \ldots, f'_j) \land f\_\text{covers}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_j)]
\]

**Lemma 5.** (Existentially Explicit Features) Given a set of features \( F \), let \( \text{Prop}(F) = (f'_1, \ldots, f'_m) \).
Then \( F \) is existentially explicit iff \( \exists c'_1 \ldots c'_n [C_1(c'_1, \ldots, c'_n) \land f\_\text{realizes}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_m)] \).

**Lemma 6.** (Universally Explicit Features) Given a set of features \( F \), let \( \text{Prop}(F) = (f'_1, \ldots, f'_m) \).
Then \( F \) is universally explicit iff \( \exists c'_1 \ldots c'_n [C_1(c'_1, \ldots, c'_n) \land f\_\text{realizes}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_m)] \)

**Lemma 7.** (Unique Implementation) Given a set of features \( F \), let \( \text{Prop}(F) = (f'_1, \ldots, f'_m) \).
Then \( F \) has a unique implementation iff \( \exists c'_1 \ldots c'_n [C_1(c'_1, \ldots, c'_n) \land f\_\text{realizes}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_m)] \land \forall d'_1 \ldots d'_n [\exists c'_1 \ldots c'_n [C_1(c'_1, \ldots, c'_n) \land f\_\text{realizes}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_m) \Rightarrow (\bigwedge_{i=1}^n (d'_i \Leftrightarrow c'_i))] \}

**Lemma 8.** (Common, live and dead elements)

1) A component \( c \) is common iff
\[
\forall c'_1 \ldots c'_n [C_f(f'_1, \ldots, f'_m) \land f\_\text{covers}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_m)] \Rightarrow c \}
\]
holds.

2) A component \( c \) is live iff
\[
\exists c'_1 \ldots c'_n [C_f(f'_1, \ldots, f'_m) \land f\_\text{covers}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_m) \land c] \}
\]

3) A component \( c \) is dead iff
\[
\forall c'_1 \ldots c'_n [C_f(f'_1, \ldots, f'_m) \land f\_\text{covers}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_m)] \Rightarrow \neg c \}
\]
holds.

**Lemma 9.** (Superfluous) A component \( c_i \) is superfluous iff \( \forall c'_1 \ldots c'_n [f'_1 \ldots f'_m] [c'_i \land C_f(f'_1, \ldots, f'_m) \land f\_\text{covers}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_m)] \Rightarrow \exists d'_1 \ldots d'_n [\neg d'_i \land C_1(d'_1, \ldots, d'_n) \land f\_\text{covers}(d'_1, \ldots, d'_n, f'_1, \ldots, f'_m)] \}

**Lemma 10.** (Redundant) A component \( c_i \) is redundant iff \( \forall c'_1 \ldots c'_n [f'_1 \ldots f'_m] [c'_i \land C_f(f'_1, \ldots, f'_m) \land f\_\text{covers}(c'_1, \ldots, c'_n, f'_1, \ldots, f'_m)] \Rightarrow \)
Lemma 11. (Critical) A component c is critical for $f_j$ if $\forall c_1, \ldots, c_n \{(C_f(c_1, \ldots, c_n) \land f_{\text{covers}}(d_1', \ldots, d_n', f_1', \ldots, f_m'))\}.$

Lemma 12. (Extends) Let $F$ and $F'$ be subsets of features. Let $\text{Prop}(F) = \{f_1, \ldots, f_m\}$ and $\text{Prop}(F') = \{f_1', \ldots, f_m'\}$. Then $F'$ extends $F$ if $\bigwedge_{i=1}^{m} (f_i \Rightarrow f_i')$ is true. $F'$ is extendable if $\exists f_1', \ldots, f_m' [\bigwedge_{i=1}^{m} f_i' \Rightarrow f_i].$

Theorem 15. Given an SPL $\Psi$, each of the properties listed in Table XIII holds good iff the corresponding formulae evaluate to true.

Proof: The detailed proof is given in the full version of the paper.

VI. IMPLEMENTATION

In this section, we give some details of the implementation of the theory developed, using off-the-shelf QSAT solvers. We also illustrate the encoding of the analysis problems in QBF and their solutions through a small example.

A. QBF and QDIMACS format

Quantified Boolean Formulae (QBF) are generalized form of propositional formulae with quantification (existential and universal) over the propositional symbols. The boolean satisfiability problem for propositional formulae is then naturally extended to QBF satisfiability problem (QSAT).

Most QBF solvers follow QDimacs, a standard input and output file format. QDimacs Format is built on top of the DIMACS standard for SAT Solver. A QDimacs file representing a QBF has three parts: Preamble, Prefix and Matrix. The notations use a unique indexing of all the propositional variables occurring in the QBF.

1) Preamble: The Preamble contains different types of information about the file, namely,

a) Comments: Each comment line should start with lower case character 'c'. There can be multiple comment lines in the File.

Format: c COMMENT_STRING

Example:
c qdimacs file for completeness.

c cnf 2 2

b) Problem Line: There is only one problem line in each QDimacs File. The problem line starts with the lower case character 'p' followed by the string 'cnf', which denotes that the given formula is in conjunctive normal form (CNF). The 'cnf' string is followed by variables count and clauses count.

Format: p cnf VAR_COUNT CLA_COUNT

Example:
p cnf 4 2

2) Prefix: The Prefix lines are used to represent the quantifiers in the Formula. Each Prefix line starts with a lower case character 'a' or 'e'; 'a' represents universal quantifier and 'e' represents existential quantifier. Quantifiers are followed by the indices of variables. Each prefix line ends with '0'.

Example:
a 1 2 0
e 3 4 0

3) Matrix: Each line in matrix represents a clause and should end with '0'. Each propositional variable in clause is represented by it's corresponding unique index. The complement of a variable is represented by negation of the index.

Example:
1 3 0
2 -4 0

As an example, the QDimacs format for the formula $\forall X \exists Y ((X \lor \neg Y) \land (\neg X \lor Y))$ is as follows. The first line is a comment line. The second one is the problem line which mentions that there are two variables and two clauses. The third line represents the universal quantification of $X$ and the fourth line represents the existential quantification of $Y$.

The fifth line represents the first clause $(X \lor \neg Y)$ and the sixth line represents the second clause $(\neg X \lor Y)$.

c Illustration
c cnf 2 2
a 1 0
e 2 0
1 -2 0
-1 2 0

QuBE is a solver for Quantified Boolean Formulas (QBFs). It accepts QBFs in QDimacs format and returns TRUE if the formula is satisfiable, and FALSE otherwise. We have developed a tool called CNF2QDIMAC converter. The tool converts QBFs in CNF to QDimacs format which can be given as input to QuBE. Conversion of arbitrary QBFs to CNF is done using some online tools.

B. An Illustrative Example

Consider the following SPL $\Psi = (\mathcal{C}, \mathcal{F}, T)$ with $\mathcal{C} = \{\{c_1, c_2\}, \{c_3, c_4\}\}$ and $\mathcal{F} = \{\{f_1, f_2\}, \{f_3\}\}$. Thus, there are 4 components and 3 features. Further, let the traceability relation $T$ be given as follows:

- $\text{prov}(f_1) = \{\{c_1, c_2\}, \{c_3\}\}$, $\text{req}(f_1) = \{\{c_1\}, \{c_3\}\}$
- $\text{prov}(f_2) = \{\{c_2\}\}$, $\text{req}(f_1) = \{\{c_2\}\}$
- $\text{prov}(f_3) = \{\{c_1, c_4\}\}$, $\text{req}(f_3) = \{\{c_4\}\}$

Let us answer the following questions using the logic formulation with the help of the QuBE tool.
1) Does $C = \{c_1, c_2\}$ implement $f_3$? Clearly, the answer is YES. In the logic formalism, $f\_implements(1, 1, 0, 0, f_1)$ is defined as
$
\forall c_1, c_2, c_4 \{((1 \Rightarrow c_1) \land (1 \Rightarrow c_2) \land (0 \Rightarrow c_3) \land (0 \Rightarrow c_4)) \Rightarrow f\_prov(f_1)\}$
where $f\_prov(f_1) = (c_1 \land c_2) \lor c_3$. The formula when simplified is
$
\forall c_1, c_2, c_4 \{(c_1 \land c_2) \lor (c_1 \land c_3) \land (c_4)\} \Rightarrow c_4.
$
It is easy to see that the formula evaluates to true. Hence QuBE returns an affirmative answer.

Now consider $C = \{c_3\}$. Does $C$ implement $f_3$? Clearly, the answer is NO. In the logic formalism, $f\_implements(0, 0, 1, 0, f_3)$ is defined as
$
\forall c_1, c_2, c_4 \{((0 \Rightarrow c_1) \land (0 \Rightarrow c_2) \land (1 \Rightarrow c_3) \land (0 \Rightarrow c_4)) \Rightarrow f\_prov(f_3)\}$
where $f\_prov(f_3) = (c_1 \land c_4)$. The simplified formula is
$
\forall c_1, c_2, c_4 \{(c_1 \land c_4) \lor (c_1) \land (c_2) \land (c_3)\} \Rightarrow c_4.
$
The assignment $c_3 = 1, c_1 = 0$ evaluates the quantifier-free formula to false. Hence QuBE returns a negative answer.

2) Consider $C = \{c_1, c_2\}$. Does $C$ realize $\{f_1, f_2\}$? Clearly, the answer is YES. In the logic formalism, $f\_realizes(1, 1, 0, 0, 1, 1)$ is defined as
$
[1 \iff f\_implements(1, 1, 0, 0, f_1)] \land [1 \iff f\_implements(1, 1, 0, 0, f_2)] \land [0 \iff f\_implements(1, 1, 0, 0, f_3)]
$
Now, $f\_implements(1, 1, 0, 0, f_1)$ is defined as
$
\forall c_1, c_2, c_4 \{((1 \Rightarrow c_1) \land (1 \Rightarrow c_2) \land (0 \Rightarrow c_3) \land (0 \Rightarrow c_4)) \Rightarrow f\_prov(f_1)\}$
where $f\_prov(f_1) = (c_1 \land c_2) \lor c_3$. Clearly, $f\_implements(1, 1, 0, 0, f_1)$ holds. Thus, we have
$
[1 \iff f\_implements(1, 1, 0, 0, f_1)] \land [1 \iff f\_implements(1, 1, 0, 0, f_2)].
$
As seen above, clearly, $[1 \iff f\_implements(1, 1, 0, 0, f_1)]$ holds. However, we have $f\_implements(1, 1, 0, 0, f_2)$ is true since $prov(f_2) = \{c_2\}$. Then, we do not have
$
[0 \iff f\_implements(1, 1, 0, 0, f_3)]
$
3) Is the given SPL complete? That is, for every $F \in \mathcal{F}$, does there exist some $C \in \mathcal{C}$ such that $ Covers(C, F) $? Clearly, the answer is NO since there is no $C \in \mathcal{C}$ covering $\{f_3\} \in \mathcal{F}$. The formula for this is
$
\forall f_1, f_2 \subseteq \mathcal{F} \{C\_F(f_1, f_2, f_3) \iff \exists c_1, c_2, c_4 \{C_1(c_1, c_4, c_2) \land f\_covers(c_1, c_2, c_4, f_1, f_2)\}\}
$
This expands
C_{F}(1, 1, 1) \Rightarrow \exists c_1', c_2', c_3', c_4'[C_f(c_1', \ldots, c_4') \wedge f_{covers}(c_1', \ldots, c_4', 1, 1, 1)]

C_{F}(1, 1, 0) \Rightarrow \exists c_1', c_2', c_3', c_4'[C_f(c_1', \ldots, c_4') \wedge f_{covers}(c_1', \ldots, c_4', 1, 1, 0)]

C_{F}(1, 0, 1) \Rightarrow \exists c_1', c_2', c_3', c_4'[C_f(c_1', \ldots, c_4') \wedge f_{covers}(c_1', \ldots, c_4', 0, 1, 1)]

C_{F}(0, 1, 1) \Rightarrow \exists c_1', c_2', c_3', c_4'[C_f(c_1', \ldots, c_4') \wedge f_{covers}(c_1', \ldots, c_4', 0, 1, 0)]

C_{F}(0, 0, 1) \Rightarrow \exists c_1', c_2', c_3', c_4'[C_f(c_1', \ldots, c_4') \wedge f_{covers}(c_1', \ldots, c_4', 0, 0, 1)]

C_{F}(0, 1, 0) \Rightarrow \exists c_1', c_2', c_3', c_4'[C_f(c_1', \ldots, c_4') \wedge f_{covers}(c_1', \ldots, c_4', 0, 1, 1)]

C_{F}(0, 0, 0) \Rightarrow \exists c_1', c_2', c_3', c_4'[C_f(c_1', \ldots, c_4') \wedge f_{covers}(c_1', \ldots, c_4', 0, 0, 0)]

Among these, \(C_{F}(1, 1, 0)\), \(C_{F}(0, 0, 1)\) evaluate to true. The rest evaluate to false - hence the formula involving them holds.

Now, consider \(C_{F}(1, 1, 0)\). Then we must check whether \(\exists c_1', c_2', c_3', c_4'[C_f(c_1', \ldots, c_4') \wedge f_{covers}(c_1', \ldots, c_4', 1, 1, 0)]\) holds. The tuple \((1, 1, 0, 0)\) as well as \((0, 0, 1, 1)\) satisfy \(C_f(c_1', c_2', c_3', c_4')\). Hence, these are the only two tuples that we need to examine for \((c_1', c_2', c_3', c_4')\). Consider \((1, 1, 0, 0)\). Then \(C_f(1, 1, 0, 0) \wedge f_{covers}(1, 1, 0, 0, 1, 0)\) evaluates to true \(\Rightarrow [1 \Rightarrow f_{implements}(1, 1, 0, 0, f_1)] \wedge [1 \Rightarrow f_{implements}(1, 1, 0, 0, f_2)]\), \([0 \Rightarrow f_{implements}(1, 1, 0, 0, f_3)]\). Clearly, this is true, as \(\{c_1, c_2\}\) covers \(\{f_1, f_2\}\).

Now consider \(C_{F}(0, 0, 1)\). Then we must check \(\exists c_1', c_2', c_3', c_4'[C_f(c_1', \ldots, c_4') \wedge f_{covers}(c_1', \ldots, c_4', 0, 0, 1)]\) holds. Again, consider the two possibilities for \(C_f(c_1', c_2', c_3', c_4')\).

Look at \(C_{F}(1, 1, 0, 0)\) first. Then we have to check if \(f_{covers}(1, 1, 0, 0, 0, 1)\) is true. This is \(0 \Rightarrow f_{implements}(1, 1, 0, 0, f_1)\) \(\wedge [0 \Rightarrow f_{implements}(1, 1, 0, 0, f_2)] \wedge [1 \Rightarrow f_{implements}(1, 1, 0, 0, f_3)]\). Clearly, \(f_{implements}(1, 1, 0, 0, f_3)\) does not hold since \(\text{pro}(f_3) = \{c_1, c_4\}\) and \(c_4\) can be assigned \(0\) in this formula. Now consider the second assignment \((0, 0, 1, 1)\). Then again, \(C_f(0, 0, 1, 1)\) holds. Now check if \(f_{covers}(0, 0, 1, 1, 0, 0, 1)\) holds. That is, \(0 \Rightarrow f_{implements}(0, 0, 1, 1, f_1)\) \(\wedge [0 \Rightarrow f_{implements}(0, 0, 1, 1, f_2)] \wedge [1 \Rightarrow f_{implements}(0, 0, 1, 1, f_3)]\). Since \(\text{pro}(f_3) = \{c_1, c_4\}\), \(f_{implements}(0, 0, 1, 1, f_3)\) is false. Thus, this does not hold good as well.

Therefore, for \(\{f_3\}\) (equivalently, \(C_{F}(0, 0, 1)\)), there is no \(C_f(c_1', c_2', c_3', c_4')\) which realizes \(\{f_3\}\). Hence, QuBE returns false. Then, we can conclude that the SPL is not complete.

VII. RESULTS OF ANALYSES ON THE ECPL CASE-STUDY

In this section, we analyze some properties of the ECPL example using QUBE. The platform \(\mathcal{C}\) contains the following architectures:

1) \(C_1 = \{\text{Door Lock Manager, Unlock Driver Door, Unlock all doors, Lock all doors}\}\)

2) \(C_2 = \{\text{Door lock manager, Unlock driver door, Unlock all doors, Lock all doors, AutoLock, Speed}\}\)

3) \(C_3 = \{\text{Door lock manager, Unlock driver door, Unlock all doors, Lock all doors, AutoLock, Gear in park}\}\)

4) \(C_4 = \{\text{Door lock manager, Unlock driver door, Unlock all doors, Lock all doors, Power Lock, Courtesy switch, Key signal, silldoor signal, Automatic}\}\)

5) \(C_5 = \{\text{Door lock manager, Unlock driver door, Unlock all doors, Lock all doors, Power Lock, Courtesy switch, Key signal, silldoor signal, Manual}\}\)

6) \(C_6 = \{\text{Door lock manager, Unlock driver door, Unlock all doors, Lock all doors, AutoLock, Speed, Power Lock, Courtesy switch, Key signal, silldoor signal, Automatic}\}\)

7) \(C_7 = \{\text{Door lock manager, Unlock driver door, Unlock all doors, Lock all doors, AutoLock, Gear in park, Power Lock, Courtesy switch, Key signal, silldoor signal, Automatic}\}\)

8) \(C_8 = \{\text{Door lock manager, Unlock driver door, Unlock all doors, Lock all doors, AutoLock, Gear in park, Power Lock, Courtesy switch, Key signal, silldoor signal, Manual}\}\)

9) \(C_9 = \{\text{Door lock manager, Unlock driver door, Unlock all doors, Lock all doors, AutoLock, Gear in park, Power Lock, Courtesy switch, Key signal, silldoor signal, Automatic}\}\)

Consider the following specifications in the scope \(\mathcal{F}\).

1) \(F_1 = \{\text{Power Lock, f automatic}\}\)

2) \(F_2 = \{\text{Power Lock, f automatic, Door Lock, Shift out of Park, Door relock}\}\)

1) Does \(C_1\) realize \(F_1\)? The formula to check is \([1 \Leftrightarrow f_{implements}(1, 1, 1, 1, 0, 0, 0, 0, 0, 0, \text{Power Lock})] \wedge [1 \Leftrightarrow f_{implements}(1, 1, 1, 1, 0, 0, 0, 0, 0, 0, \text{f automatic})] \wedge \ldots \wedge [0 \Leftrightarrow f_{implements}(1, 1, 1, 1, 0, 0, 0, 0, 0, 0, \text{Door relock})]\)

Let \(c_1 = \text{Door Lock Manager, c}_2 = \text{Unlock Driver Door, c}_3 = \text{Unlock all doors, c}_4 = \text{Lock all doors, c}_5 = \text{Power Lock}\). This is defined as \(\forall c_1, \ldots, c_5 ([(1 \Rightarrow c_1] \wedge [1 \Rightarrow c_2] \wedge [1 \Rightarrow c_3] \wedge [1 \Rightarrow c_4] \wedge [0 \Rightarrow c_5] \wedge [0 \Rightarrow c_6]) \Rightarrow (c_1 \wedge c_5)\). Clearly, this does not hold (for \(c_5 = 0\), the formula does not hold).
Hence, QUBE returns false.

2) Is ECPL sound? If so, then for every \( C_i \in \mathcal{C} \), we can find a specification \( F_i \) such that \( \text{Covers}(C_i, F_i) \). The formulae for this is

\[
\forall c_1 \ldots c_n[C_f(c_1, \ldots, c_n)] \Rightarrow \\
\exists f_1 \ldots f_m[C_f(f_1, \ldots, f_m) \land \\
f_{\text{covers}}(c_1, \ldots, c_n, f_1, \ldots, f_m)]
\]

Consider the tuple \((1, 1, 1, 0, \ldots, 0)\) where the first four entries are 1, and the rest are zero. This corresponds to \( C_1 \). Clearly, \( C_1 \) does not realize any \( f \). Let us look at \( f_{\text{covers}}(1, 1, 1, 0, \ldots, 0, f_1, \ldots, f_m) \). It is easy to see that \( f_{\text{impl}}(1, 1, 1, 0, \ldots, 0, f) \) does not hold good for any \( f \) since \( C_1 \) does not provide any features alone, and \( c_i, i > 0 \) do not provide any features. Thus, the formula does not hold good, and QUBE returns false. Hence, the ECPL is not sound.

3) Is \( F_i \) universally explicit? If so, then any \( C_i \in \mathcal{C} \) which covers \( F_i \) must realize \( F_i \); moreover, there must be at least one \( C \in \mathcal{C} \) which covers it. The formula for this is

\[
\exists c_1' \ldots c_n'[C_f(c_1', \ldots, c_n')] \land \\
f_{\text{realizes}}(c_1', \ldots, c_n', f_1', \ldots, f_m') \land \\
\forall c_1' \ldots c_n'[(C_f(c_1', \ldots, c_n') \land \\
f_{\text{covers}}(c_1', \ldots, c_n', f_1', \ldots, f_m')) \Rightarrow \\
f_{\text{realizes}}(c_1', \ldots, c_n', f_1', \ldots, f_m')]
\]

Let us denote \( C_1 = \text{Door Lock Manager}, C_2 = \text{AutoLock}, C_3 = \text{Power Lock}, C_4 = \text{Gear in Park} \) and \( C_5 = \text{Automatic}, C_6 = \text{Unlock driver door}, C_7 = \text{Unlock all doors}, C_8 = \text{Lock all doors}, C_9 = \text{Courtesy switch}, C_{10} = \text{Key signal}, C_{11} = \text{sill door signal}, C_{12} = \text{Speed and } C_{13} = \text{Manual} \). Similarly, let \( f_1 = \text{Power Lock} \) and \( f_2 = f_{\text{Automatic}} \). Consider the component tuple \((1, 0, 1, 0, 1, 1, 1, 1, 1, 1, 1, 0, 0)\). Then we have \( C_f(1, 0, 1, 0, 1, 1, 1, 1, 1, 1, 1, 0, 0) \). \( C_4 \) corresponds to this set and \( f_{\text{realizes}}(1, 0, 1, 0, 1, 1, 1, 1, 1, 1, 0, 0, 1, 1, 0, \ldots, 0) \). Let us consider the component tuple \((1, 1, 1, 1, 1, 1, 1, 0, 0)\). Clearly, \( C_f(1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 0, 0) \) does not hold good. Hence, \( C_4 \) does not realize \( F_1 \).

Hence, this conjunct does not hold good. Hence, \( f_{\text{realizes}}(1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 0, 0, 1, 1, 0, \ldots, 0) \) does not hold.

Hence, QUBE returns false. Thus, for the component tuple \((1, 0, 1, 0, 1, 1, 1, 1, 1, 1, 0, 0)\) which realizes \( F_1 \), there exists a component tuple which covers, but does not realize \( F_1 \). Hence, \( F_1 \) is not universally explicit.

VIII. Conclusion

In this report, we have given a new definition for products in a Software Product Line, based on the notion of derivability of feature specifications from component architectures. The traceability relation between features and components plays a central role in this definition. We show that our definition is different from the consistency based definition of SPL products and captures the implementation relation in a more natural way. In the light of this, we define a set of analysis problems for the SPLs. We show that these problems can be formulated as Quantified Boolean Formulae and can be solved using QSAT tools such as QUBE.

We have demonstrated the feasibility of our approach through a small fragment of an industrial SPL. The scalability of the above approach for complete SPLs is yet to be studied. Since QSAT problem is PSPACE-complete, generic QSAT solvers may not scale well. However, one observes that the formulas for the analyses have very specific structure which can be exploited for efficient QSAT solving.

The proposed semantic model of the SPL treats specifications and architectures as sets of features and components respectively. When richer structure is imposed on these elements, it will affect the definition of traceability relation. Then the implementation relation has to be refined to handle the resulting complexity.

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