High-Performance InGaAs HEMTs on Si Substrates for RF Applications

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Abstract: In this paper, we have fabricated InGaAs high-electron-mobility transistors (HEMTs) on Si substrates. The InAlAs/InGaAs heterostructures were initially grown on InP substrates by molecular beam epitaxy (MBE), and the adhesive wafer bonding technique was employed to bond the InP substrates to Si substrates, thereby forming high-quality InGaAs channel on Si. The 120 nm gate length device shows a maximum drain current ($I_{D,\text{max}}$) of 569 mA/mm, and the maximum extrinsic transconductance ($g_{m,\text{max}}$) of 1112 mS/mm. The current gain cutoff frequency ($f_T$) is as high as 273 GHz and the maximum oscillation frequency ($f_{MAX}$) reaches 290 GHz. To the best of our knowledge, the $g_{m,\text{max}}$ and the $f_T$ of our device are the highest ever reported in InGaAs channel HEMTs on Si substrates at given gate length above 100 nm.

Keywords: InGaAs HEMTs; Si substrates; wafer bonding; maximum extrinsic transconductance ($g_{m,\text{max}}$); current gain cutoff frequency ($f_T$)

1. Introduction

The advancement of Si CMOS technology has brought revolutionary changes to microelectronics. Although Si has proven to be very suitable for digital processing and logic applications, it is not omnipotent. Limited by the inherent physical characteristics of the material, Si is inferior to some other materials such as III–V compound semiconductors in high-frequency applications.

InGaAs displays outstanding carrier transport properties including high electron effective mobility and high sheet carrier density, compared with Si-based materials. InGaAs channel high-electron-mobility transistors (HEMTs) have been used in millimeter-wave and even terahertz monolithic integrated circuits [1–4]. They play key roles in radio-astronomy and deep-space communication. InGaAs channel HEMTs are typically manufactured on either InP or GaAs substrates in commercial production. However, ideally InGaAs channel HEMTs should be integrated on Si substrates to utilize the infrastructure and technology established by Si CMOS to improve monolithic integration and reduce costs. There have been many attempts to integrate the InGaAs channel material on Si substrates. X. Zhou et al. [5] used MOCVD heteroepitaxy technology to grow InGaAs channel material on Si substrate, but required buffer layer thickness greater than 2 µm to reduce dislocation density, which was difficult to be compatible with Si CMOS process. N. Waldron et al. [6] developed the aspect-ratio-trapping technique for heterogeneous integration, but the consistency and defects of the materials are difficult to manage. Recently, wafer bonding technology has been widely used to realize the integration of InGaAs channel material on Si substrates [7–10]. Compared with the aforementioned technology, wafer bonding...
can more easily form a high-quality InGaAs channel layer. Heterogeneous integration of InGaAs channel logic transistors on Si substrates has been reported in many published literature [11–14]. However, InGaAs channel RF devices on Si substrates have received little attention.

In this letter, we have developed InGaAs HEMTs on Si substrates for RF applications. The transfer of III–V heterostructures from InP substrates to Si substrates was realized through adhesive wafer bonding technology. Moreover, DC and RF characteristics of the fabricated 120 nm gate length HEMTs were reported. The fabricated HEMTs show high maximum extrinsic transconductance ($g_{m,\text{max}}$) and current gain cutoff frequency ($f_T$) attributable to a 70% indium content in the channel and a dielectric-assisted T-gate process that strictly suppresses series resistance.

2. Experiment

InGaAs HEMTs structures layers on Si substrates were manufactured using adhesive wafer bonding technique, as illustrated in Figure 1. The inverted HEMTs structures were grown using molecular beam epitaxy (MBE) on Semi-Insulating (SI) InP substrates with a 5 nm InP buffer layer and etching stopper layers (composed of 100 nm In$_{0.53}$Ga$_{0.47}$As and 10 nm InP) between active layers and SI InP substrates. From the InP substrates side to the top, the inverted HEMT structures composed of a 40 nm Si-doped composite InGaAs cap layer, a 4 nm InP etching stopper layer, an 8 nm In$_{0.53}$Al$_{0.47}$As Schottky barrier layer, Si delta doping layer with $5 \times 10^{12}$ cm$^{-2}$ doping concentration, a 3 nm In$_{0.52}$Al$_{0.48}$As spacer layer, a 10 nm In$_{0.7}$Ga$_{0.3}$As channel layer, and a 200 nm In$_{0.52}$Al$_{0.48}$As buffer. To prevent interface degradation, a 30 nm SiO$_2$ film was deposited by using plasma-enhanced chemical vapor deposition (PECVD). After cleaning, both the InP substrate and Si substrate were coated with an adhesion promoter layer (AP 3000, Dow Chemical) and a benzocyclobutene (BCB) layer (3022-46, Dow Chemical (Midland, MI, USA)). After 15 min of pre-curing, the formal wafer bonding was performed in a nitrogen environment. Finally, the InP substrate and the etching stopper layers were etched with hydrochloric acid and phosphorus acid/hydrogen peroxide mixed solution, and the InGaAs HEMTs structures layers were completed on the Si substrate. Figure 2 shows a 10 µm × 10 µm atomic force microscopy (AFM) scan of the n-InGaAs cap layer after back etching. The root mean square (RMS) roughness of the cap layer is 0.236 nm, which is much lower than that grown by MOCVD [15,16].

![Figure 1. Process flow for the InGaAs HEMTs structures layers on Si substrates fabrication by using adhesive wafer bonding technique.](image-url)
The device structure of InGaAs HEMTs on Si substrates and the band diagram of the heterojunction are shown in Figure 3. In the device fabrication, mesa isolation was achieved using phosphorus acid/hydrogen peroxide mixed solution and hydrochloric acid/phosphorus acid mixed solution by wet chemical etching. Optical lithography was used to define S/D ohmic contacts, which were made of Ti/Pt/Au metal. Afterward, as a hard mask for gate recess, around 5 nm SiO$_2$ was formed on the surface using PECVD. The T-shaped gating process consisted of gate e-beam lithography, SiO$_2$ etching, recess, and metallization. E-beam lithography was used to define the gate pattern, which was then transferred to the SiO$_2$ layer via reactive ion etching (RIE). The gate recess was formed by wet chemical etching with a mixture of phosphoric acid/hydrogen peroxide solution. By strictly controlling the width of the gate recess to achieve the lowest possible series resistance. The Ti/Pt/Au T-shaped gate metal was e-beam evaporated and lifted off, with the gate area defined as $2 \times (0.12 \times 50)$ µm$^2$. Finally, as surface passivation in the active region, a 20 nm Si$_3$N$_4$ layer was formed through PECVD. The cross-sectional focused ion beam (FIB) image of the T-gate region of the fabricated HEMTs on Si substrates is shown in Figure 4. The gate length can be determined as 120 nm.
3. Result and Discussion

The DC performance of devices is carried out at room temperature through the HP4142 semiconductor parameter analyzer. Figure 5 shows the $I_D$–$V_D$ output characteristics for a 120 nm gate length InGaAs HEMTs on Si substrates at room temperature with a gate bias from $-1$ V to 0 V in the step of 0.1 V. The device demonstrates superior pinch-off characteristics. The maximum drain current ($I_{D,\text{max}}$) is 569 mA/mm at $V_G = 0$ V and $V_D = 0.8$ V.

Figure 6 shows the transfer characteristic of InGaAs HEMTs on Si substrates. Benefit from an indium content of 70% in the channel, the maximum extrinsic transconductance of 1112 mS/mm was achieved at $V_G = -0.4$ V and $V_D = 0.8$ V. The threshold voltage of InGaAs HEMTs is about $-0.63$ V. The subthreshold-swing ($S$) and drain induced barrier lowering (DIBL) were 150 mV/dec and 100 mV/V, respectively.
Figure 6. Transfer characteristics of the InGaAs HEMTs on Si substrates.

Although the manufactured devices exhibit sufficiently small gate leakage currents, impact ionization cannot be ignored at high $V_D$. Impact ionization has been shown to have a negative impact on the RF and noise characteristics of HEMTs [17]. Future experiments can suppress impact ionization by using compound channels [18].

Figure 7. Gate current leakage characteristic of the InGaAs HEMTs on Si substrates.

The RF performance of devices is carried out at room temperature through the Agilent E8363B PNA vector network analyzer from 0.1 GHz to 40 GHz. On-wafer S-parameters of the InGaAs HEMTs on Si substrates were measured and extracted. Before measurement, the devices were de-embedded by using on-wafer open and short pad structures to exclude the parasitic effect. The values of current gain ($H_{21}$), maximum available gain and maxi-
mum stable gain (MAG/MSG), Mason’s unilateral gain (U), and stability factor (k) were calculated using the following Equations (1)–(6), and were plotted in Figure 8.

\[ H_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}, \]  
\[ \text{MAG} = \left| \frac{S_{21}}{S_{12}} \right| (k - \sqrt{k^2 - 1}) \quad k > 1, |\Delta| < 1 \]  
\[ \text{MSG} = \left| \frac{S_{21}}{S_{12}} \right| k < 1, |\Delta| < 1, \]  
\[ U = \frac{|(S_{21}/S_{12}) - 1|^2}{2k|S_{21}/S_{12}| - 2\text{Re}[S_{21}/S_{12}]}' \]  
\[ k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2 \cdot |S_{12}S_{21}|}, \]  
\[ \Delta = S_{11}S_{22} - S_{12}S_{21}, \]  

Figure 8. RF characteristics of the HEMTs at \( V_G = -0.4 \) V and \( V_D = 0.8 \) V.

In addition, the small-signal model of HEMTs fabricated on Si substrates was made at the \( g_{m,max} \) point of \( V_G = -0.4 \) V and \( V_D = 0.8 \) V. The device modeling parameters are tweaked until the S-parameters match closely with the measured parameters, as shown in Figure 8. Since the limitation of test frequency, \( f_T \) and maximum oscillation frequency (\( f_{MAX} \)), were obtained by extrapolating the simulated curve of \( H_{21} \) and MAG/MSG. The extrapolated \( f_T \) and \( f_{MAX} \) were 273 and 290 GHz, respectively. The \( f_T \) and \( f_{MAX} \) are expressed by Equations (7) and (8).

\[ f_T = \frac{g_{mi}}{2\pi \left( C_{gs} + C_{gd} \right) \left[ 1 + g_{ds}(R_s + R_d) \right] + C_{gd} \cdot g_{mi}(R_s + R_d)}, \]  
\[ f_{MAX} = \frac{f_{T,int}}{\sqrt{4g_{ds}(R_g + R_s + R_d) + \frac{2C_{gd}}{C_{gs}} \left( \frac{C_{gd}}{C_{gs}} + g_{mi}(R_i + R_d) \right)}}, \]  

where \( g_{mi} \) is the intrinsic transconductance, \( C_{gs} \) and \( C_{gd} \) are the parasitic capacitances from gate to source and gate to drain, respectively; \( g_{ds} \) is conductance between drain and source;
$R_s$, $R_d$ and $R_g$ are the parasitic resistances of source, drain and gate, respectively. $R_i$ is the intrinsic resistance in the channel region. $f_{T,int}$ represents the cut-off frequency of the intrinsic part of HEMTs without parasitic resistance and capacitance. From Equations (7) and (8) we can know that $C_{gs}$, $C_{gd}$, $R_s$ and $R_d$ are the key parasitic parameters that affect $f_T$ and $f_{MAX}$ [19]. Especially, $R_s$ and $R_d$ have a great impact on $f_T$. In our device manufacturing process, $R_s$ and $R_d$ were effectively restricted by controlling the etching of the gate recesses, thus improving $f_T$. The extraction of parameters through the small-signal model further confirms our viewpoint. Table 1 summarizes the small-signal modeling parameters of InGaAs HEMTs on Si substrates at the $g_{m,max}$ point of $V_G = -0.4$ V and $V_D = 0.8$ V.

**Table 1.** The parameters of the small-signal equivalent circuit of devices.

| $C_{gs}$ (fF) | $C_{gd}$ (fF) | $C_{ds}$ (fF) | $g_{ds}$ (mS) | $R_s$ (Ω) | $R_d$ (Ω) | $R_g$ (Ω) | $R_i$ (Ω) | $g_{m}$ (mS) | $\text{Tau}$ (fs) |
|--------------|--------------|---------------|-------------|-----------|-----------|-----------|-----------|-------------|---------------|
| 62.1         | 9.5          | 11.5          | 10          | 1.6       | 4.5       | 3         | 7.5       | 116         | 400           |

The performance of our fabricated device and other reported InGaAs channel transistors on Si substrates are summarized in Table 2. Our 120 nm gate length device exhibits $g_{m,max} = 1112$ mS/mm and $f_T = 273$ GHz, which are the highest values reported in the InGaAs channel transistors on Si substrates at given $L_G$ above 100 nm as far as we know.

**Table 2.** Comparison with published InGaAs channel transistors on Si substrates.

| Reference | $L_G$ (nm) | Channel | $I_{D,max}$ (mA/mm) | $g_{m,max}$ (mS/mm) | $f_T$ (GHz) | $f_{MAX}$ (GHz) |
|-----------|------------|---------|---------------------|--------------------|-------------|-----------------|
| [7]       | 125        | InGaAs/InAs/InGaAs       | 650                | 500                | 227         | 187             |
| [15]      | 150        | InGaAs/InGaAs          | 160                | -                  | 60          | -               |
| [20]      | 400        | InGaAs/InGaAs         | 150                | 155                | 5.5         | 13              |
| [21]      | 120        | InGaAs/InGaAs        | 450                | 770                | 185         | 290             |
| This work | 120        | InGaAs/InGaAs        | 569                | 1112               | 273         | 290             |

4. Conclusions

We have demonstrated InGaAs HEMTs on Si substrates for RF applications. The 120 nm gate length device exhibits good DC and RF performances featuring $g_{m,max} = 1112$ mS/mm and $f_T = 273$ GHz, which are the highest values reported in InGaAs channel transistors on Si substrates above $L_G = 100$ nm. These results show the potential for InGaAs HEMTs in future high-frequency applications on Si substrates.

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