Shape optimization of superconducting transmon qubits for low surface dielectric loss

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Abstract
Surface dielectric loss from superconducting transmon qubits is believed to be one of the dominant sources of decoherence. Reducing surface dielectric loss is crucial for achieving a high quality factor and a long relaxation time ($T_1$), which can be engineered by carefully changing the geometry of a transmon. In this paper, we present a shape-optimization approach to reduce surface dielectric loss in a transmon qubit. The capacitor pads and junction wires of transmons are shaped as spline curves and optimized through the finite-element method and a global optimization algorithm. We find that the participation ratio of capacitor pads and junction wires can be reduced by 15%–18% and 22%–26% compared to previous designs, while the overall footprint and anharmonicity are maintained at acceptable values. As a result, the two-level system-limited quality factor and the corresponding $T_1$ were increased by 21.6%.

Keywords: shape optimization, superconducting qubits, surface dielectric loss, transmon

1. Introduction

With the dramatic improvement of the coherence time of superconducting quantum computers [1] over the past decades, superconducting quantum circuits have become a promising platform for quantum information processing. Among the various types of superconducting qubits, the transmon qubit [2] is one of the most popular structures, and is a charge qubit featuring an exponential decrease in charge noise caused by a shunting Josephson junction (JJ). To realize practical quantum computers, long relaxation times ($T_1$) and dephasing times ($T_2$) are required. Various loss mechanisms, such as Purcell loss [2], quasiparticles [3] and radiation [4], have been identified and it is widely acknowledged that two-level system (TLS) defects are limiting factors of quality factors and $T_1$ [5–9]. TLS defects are known to be coupled to qubit systems via an oscillating electric field [10] and can be calculated from the electric field profile and the geometry of transmons [11–16].

One of the common approaches for reducing TLS loss is to change material properties or fabrication methods [13, 17–19]. The geometry dependence of TLS loss has also been studied [9, 14, 20, 21] and a potential trade-off between footprint and quality factor [19] is commonly observed in those studies. However, to the best of our knowledge, TLS loss reduction in transmons that is solely based on the shape optimization approach with free-form shaping has not been vastly studied yet.

Shape and topology optimization [22] has been studied profoundly in mechanical engineering [23–25], antenna optimization [26–33] and other electromagnetic (EM) systems [22, 34]. In particular, it has been shown that the impedance matching [31], bandwidth [27, 29, 30] and current density of a planar antenna [28] can be improved through shape optimization. The optimization techniques used in those studies include adjoint-based sensitivity analysis [28, 31, 35], genetic

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algorithms [33, 36], particle swarm optimization [29, 30] and artificial neural networks [37].

In this paper, we present a shape optimization-based approach to reduce the surface dielectric loss of a transmon. Inspired by shape optimization techniques used for planar antennas, we look for an optimized geometry that features a low participation ratio within a limited footprint size. Similar to the spline-based antenna [27, 29, 30, 33], we used a spline curve to express the geometry of the capacitor pads and junction wires. We then utilized a global optimization tool to find the optimized geometry. In section 2, a fundamental scheme for participation ratio calculation and optimization is introduced. The effect of the complex surface impedance of superconducting layers is also discussed to justify our simulation settings. In section 3, the results of our optimization, including the convergence, optimized geometry and extracted key parameters, are presented. Finally, we conclude by discussing the increase of the TLS-limited quality factor and the corresponding $T_1$ using actual parameter values.

2. Surface participation calculation and optimization method

2.1. Surface participation ratio calculation

It has been acknowledged that parasitic TLS defects contained in dielectric layers function as dominant loss sources [5, 6, 38] in low-temperature superconducting circuits. TLS-related effects have been studied numerically [11, 12] and experimentally [10]. Thin dielectric layers are formed at MS (metal–substrate), MA (metal–air) and SA (substrate–air) interfaces as depicted in figures 1(a) and (b), and TLS defects contained in those layers are of our main interest. Typically, TLS loss has been studied with the participation ratio model [11–16], where the TLS-limited quality factor $Q_{\text{TLS}}$ can be expressed as

$$Q_{\text{TLS}}^{-1} = \sum_i p_i \tan \delta_i,$$

where $p_i$ and $\tan \delta_i$ denote the geometry-dependent participation ratio and loss tangent of dielectric layer $i$ ($i = \text{MS}, \text{MA}, \text{SA}$). The participation ratio $p_i$ of each dielectric layer can be numerically calculated as [11, 16]

$$p_i = \frac{t_i \varepsilon_i}{2W} \int dS |E_i|^2,$$

where $W, t_i, \varepsilon_i$ denote the total stored energy, thickness and dielectric constant of $i$th dielectric layer. In (2), an uniform electric field within the dielectric layers is assumed, which is valid when these layers are thin compared to the overall transmon geometry feature size. However, calculating (2) directly from the full EM simulation is challenging due to the diverging electric field on the metal edge [11, 39–41].

For capacitor pads, this issue can be addressed analytically with conformal mapping [16, 40] or through numerical approximations [11, 12, 17]. We adopted the method introduced in [12], where we first divided the capacitor pad into two regions—‘interior’ and ‘perimeter’—then divided the perimeter region into ‘accurate’ and ‘diverging’ regions, as illustrated in figure 1(b). The participation ratio of the interior and accurate regions can now be calculated numerically with full EM simulations, and the participation of the diverging region is calculated from the local scaling of the electric field near the metal edge [12]. The participation ratio of the junction wire illustrated in figure 1(c) was calculated from a separate simulation that only includes the junction wire and the nearby pad region. Then, we adopt the flat coax approximation [16], which can effectively approximate the $x$-dependence of an electric field. The electric energy stored in the upper junction wire can be calculated within the flat coax approximation as [16]

$$U = t \varepsilon \int_{\text{upper}} E(y)^2 r(y) \left\{ \ln \left( \frac{4r(y)}{t} \right) + 5 \right\} dy,$$

where $E(y)$ and $r(y)$ denote the electric field and half-width of the junction wire at the centerline ($x = 0$ in figure 1(c)) point with distance $y$ from the JJ. $t$ and $\varepsilon$ denote the thickness and dielectric constant of the dielectric layer, and $5$ in the integrand is a corner correction factor. Therefore, we can calculate the participation ratio from the EM simulation.

2.2. Optimization method

Shape or topology optimization techniques can be roughly categorized into gradient-based and derivative-free optimization methods [43]. Gradient-based methods require sensitivity analysis to express the gradient of the objective function, which is commonly done by using the adjoint variable method [22, 26]. However, due to numerical reasons, we adopted the DIRECT algorithm [44–47] instead, which is a global optimization method capable of finding the optimum region in design space within a few iterations [45, 47]. During each iteration with $N$ total design variables, the $N$-dimensional design space is divided into hyperrectangles and then the objective function is evaluated at the center of each hyperrectangle. Among these hyperrectangles, a set of ‘potentially optimal’ samples [44] is selected and refined at the following iterations. A detailed description of this algorithm is provided in [45]. The DIRECT optimization scheme usually terminates when the maximum number of function evaluations (NFEs) is reached [44–46] or the reduction of the objective function value becomes marginal [47].

In the capacitor pad geometry optimization, the length of the junction wire and the coordinates of the spline curve control points described in figure 2(a) are optimized in a way that the $p_{\text{MS}}$ of the interior region can be minimized. Typically, the relation between the participation ratio of the interior region and the perimeter region shows a linear proportion for the double pad geometry in figure 3. Each data point in figure 3 represents the participation ratio of a double pad geometry generated from a parametric sweep of capacitor pad dimension. Thus, the participation ratio of the perimeter region can also be minimized through the optimization of the interior region participation for this particular class of floating transmons. We used the Ansys HFSS eigenmode solver and the
Figure 1. Illustration of TLS layers in a planar transmon and a junction wire. (a) Schematic of a floating transmon. Two grey-colored capacitor pads are connected by a junction wire represented in brown color. (b) Schematic of TLS layers. The blue, red and black regions represent the MA, MS and SA interface dielectric layer. Dielectric layers are divided into ‘interior’ and ‘perimeter’ regions with a boundary at a distance $x_0 = 1 \mu m$ from the metal edge. The perimeter region is further divided into ‘accurate’ and ‘diverging’ regions with a boundary at a distance $0.5x_0 = 0.5 \mu m$ from the metal edge. (c) Illustration of the junction wire. The red box in the middle represents the JJ, the brown color represents the junction wire connecting the capacitor pad and the JJ, and $r(y)$ denotes the half-width of the junction wire at distance $y$.

Figure 2. Spline-based geometry of the capacitor pad and the flowchart of the optimization process. (a) For given control point coordinates $(P_0 - P_4)$, the capacitor pad geometry is constructed using B spline [42]. Points $P_1', P_2'$ and $P_3'$ are symmetric to $P_1, P_2$ and $P_3$, and the distance between the ground plane and the capacitor pad is fixed. (b) From the given footprint limit and wire length constraint, the range of control point coordinates is determined and the DIRECT optimizer finds an optimal geometry that minimizes the participation ratio. After each iteration, the optimizer checks if the maximum number of function evaluations or dynamic criteria is met. As a result, the geometry of the spline-shaped capacitor pad is optimized and the corresponding participation ratio $p_i$ and TLS-limited quality factor $Q_{TLS}$ are obtained.
We used a quadratic penalty function \[ \alpha \] and the value used in \[ \beta \] as

\[ \alpha, \beta \approx -0.1 \]

which is valid for the transmon regime \( E_g/E_C \gg 1 \) [2]. Junction energy \( E_g/h \) was assumed to be 16.35 GHz, which comes from \( L_1 = 10 \) nH assumption and the Ambegaokar–Baratoff relation [49, 50]. \( E_C \) was calculated from the eigenmode solution using (7), then fed into the penalty function (6). Spline-based geometry was also used for junction wire geometry, where the objective function \( p_{\text{MS}} \) was calculated from the electric field along the centerline \( E(y) \). During the optimization, \( E(y) \) was calculated using electrostatic simulation; then, \( \text{DIRECT} \) optimization was again used to find a junction wire shape that minimized the participation ratio. Detailed parameter settings and termination criteria are identical to capacitor pad optimization.

2.3. Parameter settings and in-depth analysis

In the optimization, we set \( \varepsilon_f = 10 \), \( h_i = 3 \) nm for dielectric interface layers, which is a simplified setting commonly used in related studies [11, 12, 16]. For further analysis, we first calculated the TLS-limited quality factor and the corresponding \( T_1 \) value using the actual material parameters measured in the literature [13]. We compared them with existing double pad capacitor designs [14, 17, 18] and concentric transmons [51]. Furthermore, we investigated the effect of a superconductor’s surface impedance to validate the perfect conductor boundary condition. We confirmed that the participation ratio and resonant frequency changes were less than 0.1% at 20 mK when the surface impedance of a typical superconducting film is taken into account [38, 52, 53]. Thus, we safely applied a perfect conductor boundary condition for superconducting films.

3. Results and discussion

Optimization of both capacitor pads and junction wires converged with a maximum footprint 800 \( \mu \text{m} \times 800 \mu \text{m} \). Figure 4 shows the evolution of the participation ratio in the capacitor pad geometry optimization. In figure 4, the y-axis shows the interior \( p_{\text{MS}} \) value of the current best sample point. In the early steps of the optimization (inset a, b of figure 4), \( E_C/h \) exceeds the upper bound of 350 MHz. After a few iterations, the optimizer approaches the design space region where the \( E_C \) constraint is satisfied and, eventually, the objective function value converges and termination conditions are satisfied.

The resulting capacitor pad and junction wire geometries are shown in figures 5(a) and (b), respectively. The optimized capacitor geometry in figure 5(a) can be seen as a typical double pad capacitor being smoothly tapered near the junction wire. Similar to the tapered wire suggested in [16], the optimized junction wire geometry in figure 5(b) shows a tapered wire with an optimal taper slope \( S = 0.4 \), with a narrow neck in the middle bringing an additional reduction of participation.

Key parameters of the optimized capacitor pad, junction wire and some reference geometries were extracted from EM simulations and summarized in table 1. In order to compare our design with the existing ones, we extracted the participation ratios of traditional transmon designs called double pad capacitors [17] and a concentric transmon [51]. Table 1 shows...
Figure 4. Convergence plot of capacitor pad optimization. Insets (a)–(d) show how the capacitor pad shape of the potentially optimal sample points evolves through the optimization. The Y-axis shows the evolution of the capacitor pad interior $p_{MS}$ value of the current best sample point.

Figure 5. Capacitor pad and junction wire geometry generated by DIRECT optimization. (a) Optimized capacitor pad geometry. The distance between the capacitor pad and the ground plane is fixed to 100 $\mu$m and the resulting overall footprint is $763 \times 751 \mu$m. (b) Optimized junction wire geometry with wire length of 81 $\mu$m and junction width of 1 $\mu$m. Red box represents the JJ.

Table 1. Key parameters of the optimized capacitor pad, junction wire and existing structures.

|                  | Optimized pad | Double pad [17] | Concentric [51] |
|------------------|---------------|-----------------|-----------------|
| $p_{MS}$ [ppm]   | 81.5          | 97.5            | 106.5           |
| $p_{SA}$ [ppm]   | 70.7          | 82.7            | 88.1            |
| $p_{MA}$ [ppm]   | 6.09          | 7.46            | 8.44            |

|                  | Optimized wire | Straight      | Linear taper   |
|------------------|----------------|---------------|----------------|
| $p_{MS}$ [ppm]   | 16.8           | 22.8          | 17.8           |
| $p_{MA}$ [ppm]   | 0.17           | 0.23          | 0.18           |

$\varepsilon_i = 10, t_i = 3$ nm for all dielectric layers
that the total MS, MA and SA participation ratios were reduced approximately by 15% – 18% compared to the double pad capacitor geometry. The lower part of table 1 displays the participation ratio of junction wires, which in turn indicates that the optimized wire has a participation ratio that is approximately 22% – 26% smaller than the straight wire, with the optimized wire showing a slightly smaller value than the linear taper.

Based on the parameters in table 1, TLS-limited quality factor $Q_{\text{TLS}}$ and corresponding TLS-limited relaxation time $T_1 (= Q_{\text{TLS}}/\omega_0)$ were calculated. We assumed superconducting niobium layers in a silicon substrate device [54], using the material parameters reported in [54] (tan $\delta_{\text{MS}} = 1.3 \times 10^{-3}$, tan $\delta_{\text{SA}} = 2.1 \times 10^{-3}$, tan $\delta_{\text{MA}} = 4.7 \times 10^{-2}$) with dielectric constant $\varepsilon_{\text{MS}} = 11.7$, $\varepsilon_{\text{sub}} = 11.7$, $\varepsilon_{\text{SA}} = 4.2$, $\varepsilon_{\text{MA}} = 33$ and dielectric layer thickness $t_{\text{MS}} = 2 \text{ nm}$, $t_{\text{SA}} = 5 \text{ nm}$, $t_{\text{MA}} = 5 \text{ nm}$. The TLS-limited quality factor and $T_1$ of a transmon with a double pad capacitor and a straight wire were calculated as $2.24 \times 10^6$ and 71.1 $\mu$s for qubit frequency $f_0 = 5 \text{ GHz}$. On the other hand, the $Q_{\text{TLS}}$ and $T_1$ of a transmon with an optimized capacitor pad and junction wire were $2.72 \times 10^6$ and 86.5 $\mu$s. Hence, both the TLS-limited quality factor and relaxation time were improved by 21.6% through shape optimization.

4. Conclusion

We present a shape optimization-based approach to improve the $T_1$ of superconducting transmon qubits. A common approach for reducing surface dielectric loss is to change the material or fabrication method, but we adopted geometry optimization techniques that have been used in other EM systems. The results indicate that surface dielectric loss can be reduced by optimizing the geometry. Further research of geometry optimization-based approaches is required to design a qubit structure with a smaller footprint and sufficient $T_1$. Moreover, combining the geometry optimization-based approach with the recently described tantalum transmons [17, 18] will further improve the state-of-the-art transmons. In addition, studying other loss mechanisms including quasiparticle loss [55] will widen our understanding of the optimized geometry. Our transmon design can also be applied to realize practical quantum computers since the longer $T_1$ reduces the coherence-limited quantum gate error [56].

Data availability statement

The data cannot be made publicly available upon publication because they are owned by a third party and the terms of use prevent public distribution. The data that support the findings of this study are available upon reasonable request from the authors.

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Conflict of interest

The authors declare no conflicts of interest.

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