Investigation of Ferroelectric Grain Sizes and Orientations in Pt/Ca$_x$Sr$_{1-x}$Bi$_2$Ta$_2$O$_9$/Hf–Al–O/Si High Performance Ferroelectric-Gate Field-Effect-Transistors

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Abstract: Electron backscatter diffraction (EBSD) was applied to investigate the grain size and orientation of polycrystalline Ca$_x$Sr$_{1-x}$Bi$_2$Ta$_2$O$_9$ (C$_x$S$_{1-x}$BT) films in ferroelectric-gate field-effect transistors (FeFETs). The C$_x$S$_{1-x}$BT FeFETs with $x = 0, 0.1, 0.2, 0.5,$ and $1$ were characterized by the EBSD inverse pole figure map. The maps of $x = 0, 0.1,$ and $0.2$ showed more uniform and smaller grains with more inclusion of the $a$-axis component along the film normal than the maps of $x = 0.5$ and $1$. Since spontaneous polarization of C$_x$S$_{1-x}$BT is expected to exist along the $a$-axis, inclusion of the film normal $a$-axis component is necessary to obtain polarization versus electric field ($P$–$E$) hysteresis curves of the C$_x$S$_{1-x}$BT when the $E$ is applied across the film. Since memory windows of FeFETs originate from $P$–$E$ hysteresis curves, the EBSD results were consistent with the electrical performance of the FeFETs, where the FeFETs with $x = 0, 0.1,$ and $0.2$ had wider memory windows than those with $x = 0.5$ and $1$. The influence of annealing temperature for C$_{0.1}$S$_{0.9}$BT poly-crystallization was also investigated using the EBSD method.

Keywords: EBSD; FeFET; ferroelectric; grain; orientation

1. Introduction

As a memory device, the ferroelectric-gate field-effect transistor (FeFET) has attracted much interest [1–7]. It has many features, such as non-volatile memory function, voltage driven write operation, nondestructive read operation, and possible compact 4F$^2$ cell size (F: feature size) [1,3]. FeFETs can be applied not only to NAND flash memories intended for large scale storage [8–11], but also to embedded flash memories with logic devices for portable and other IOT (internet of things) devices with low power dissipation and low voltage operation [12–14]. The FeFET in this paper is a type of metal-ferroelectric-insulator-semiconductor (MFIS). The FeFET is shown schematically in Figure 1. MFIS FeFETs with long retention and high endurance were realized for the first time using Pt/SrBi$_2$Ta$_2$O$_9$(SBT)/Hf–Al–O(HAO)/Si gate stacks, where the HAO is (HfO$_2$)$_y$(Al$_2$O$_3$)$_{1-y}$, often with $y = 0.75$ [15–17]. One-month-long retention was demonstrated by a self-aligned gate FeFET with Pt/SBT/HAO/Si [18]. In 2013, calcium doped SBT, Ca$_x$Sr$_{1-x}$Bi$_2$Ta$_2$O$_9$ or C$_x$S$_{1-x}$BT, was introduced as a ferroelectric material in MFIS FeFETs that attained larger memory windows of the FeFETs than the conventional SBT [19]. After the FeFETs with C$_x$S$_{1-x}$BT were developed, 3.3 V-write-voltage FeFETs [14] and 100-nm metal-gate FeFETs [20] were demonstrated. Write performances of FeFETs were precisely investigated by applying pulse voltages [21]. Memory-cell properties for new ferroelectric NOR flash memories were examined [22].
Ferroelectricity of materials strongly depends on the crystallinity, which has been conventionally characterized by X-ray diffraction (XRD) [23,24]. Recently, the electron backscatter diffraction (EBSD) method was developed into an important technique for metallography [25] and was also used to characterize the ferroelectric materials [26,27]. In this study, the EBSD is applied for the first time in order to discuss the relevance of the nonvolatile-memory-cell performances of the FeFETs with the ferroelectric crystallinity of the $C_{x}S_{1-x}BT$ hidden inside the MFIS gate stacks. The EBSD method exhibits a two-dimensional map of the $C_{x}S_{1-x}BT$ grains, whose size and crystal orientation can be understood visually. The minimum size detectable by the EBSD is as small as 10 nm, which can be observed in situ by the field-emission-type scanning electron microscope (FESEM) [25]. The spatial resolution of the EBSD is much higher than that of XRD. With downsizing of ferroelectric devices [20,28], micro area analysis of the ferroelectric layers would be very helpful to understand the quality and achieve better device performance. In this work, the EBSD characterizations of $C_{x}S_{1-x}BT$ layers in the FeFETs were performed after the manufacturing processes were completed and the electrical properties were identified. In the processes, the whole MFIS stacks were annealed for the $C_{x}S_{1-x}BT$ crystallization with the Pt electrodes formed on the $C_{x}S_{1-x}BT$ by photo-lithography and ion-beam etching [19]. Therefore, grain size and orientation of the polycrystalline $C_{x}S_{1-x}BT$ underneath the gate-electrode Pt could not be directly observed. How to remove the Pt layer was an important technique in this work.

Figure 1. (a) Drain current ($I_d$) vs. gate voltage ($V_g$) curves, modified from [19]; (b) Polarization ($P$) as a function of gate voltage of $C_{x}S_{1-x}BT$ ferroelectric-gate field-effect transistors (FeFETs) with $x = 0, 0.1, 0.2, 0.5$, and 1. $C_{x}S_{1-x}BT$ crystallization annealing were performed in O$_2$ ambient for 30 min at 813 °C for $x = 0$ and at 800 °C for the others. (c) Schematic drawing with voltage terminals for the metal-ferroelectric-insulator-semiconductor (MFIS) type FeFET.
2. Experimental

2.1. Fabrication of FeFETs and Electrical Characterization

_P-type_ Si substrates, with _n^+_ source and drain regions formed in advance, were used to fabricate _n_-channel MFIS FeFETs with Pt/_{C_xS_{1-x}BT}/(HAO)/Si gate stacks [19]. The thicknesses of HAO, C_xS_{1-x}BT, and Pt were 7 nm, 200 nm, and 200 nm, respectively. HAO and C_xS_{1-x}BT were deposited by pulse laser deposition. Pt was deposited by electron-beam evaporation. Further details of the fabrication process were reported elsewhere [19]. The metal gate length (L) was 10 µm, and the gate width (W) was 200 µm [19]. Here, two groups of FeFETs were investigated by EBSD. In the first group, _x_ was varied. Namely, C_{x}S_{1-x}BT FeFETs with _x_ = 0 (SBT), _x_ = 0.1, _x_ = 0.2, _x_ = 0.5, and _x_ = 1 (CaBi_{2}Ta_{2}O_{9}, CBT), were characterized. The SBT FeFET was annealed at 813 °C. The other C_{x}S_{1-x}BT FeFETs were annealed at 800 °C. In the second group, _x_ was fixed at _x_ = 0.1 and the C_{0.1}S_{0.9}BT FeFETs were annealed at nine different temperatures in O_2 ambient, which were 748, 755, 763, 775, 788, 800, 813, 823, and 833 °C. All the temperatures were set-temperatures, which were about 10 °C higher than the real sample temperatures according to a temperature sensor. The sensor was an _R_-type thermocouple buried in a 20 mm^2 diced Si wafer. Drain current versus gate voltage (I_d–V_g) curves were measured using an Agilent 4156C transistor analyzer. Memory window (MW) was defined as the difference of the threshold voltages when I_d/W = 10^-8 A/µm on the I_d–V_g hysteresis loops [19]. Polarization (P) versus gate voltage (P–V_g) hysteresis curves were obtained using the virtual ground mode of the Radiant RT6000S ferroelectric test system.

2.2. EBSD Sample Preparation

High quality Pt/_{C_xS_{1-x}BT}/HAO/Si FeFETs were manufactured successfully with good reproducibility [19]. For crystallizing the C_{x}S_{1-x}BT, the whole MFIS stacks were annealed. Due to the coverage by the Pt gate metal, the ferroelectric C_{x}S_{1-x}BT film was hidden in the MFIS stacks. To observe the C_{x}S_{1-x}BT by EBSD, therefore, the Pt layer was removed using polishing cloths with 0.25 µm-size fine diamond pastes of SCAN-DIA. After the polishing, the samples were ultrasonically cleaned in acetone and in deionized water. Although the polishing made linear scratches to some extent on the surface of the C_{x}S_{1-x}BT layer, such scratches had no influence on crystal-orientation characterization by EBSD.

2.3. EBSD Scanning

An EBSD system (EDAX-TSL, AMETEK, Inc., Berwyn, PA, USA) was installed in the FESEM (JSM-7001F, JEOL Ltd., Tokyo, Japan). During EBSD scanning, the samples were kept 70° tilted from the horizontal position in order to optimize the fraction of electrons scattered and the contrast in the diffraction pattern. When the electron beam hit the sample surface region, some of the scattered electrons agreed with the Bragg’s law and were diffracted from lattice planes. The diffraction patterns in the space, which are well known as Kikuchi bands, were captured by a phosphor screen equipped inside the FESEM. The Kikuchi band of every sample point was collected by the EBSD software and outputted into EBSD maps after Miller indexing. The crystal structure of C_{x}S_{1-x}BT is orthorhombic (A21am) [29]. However, since the EBSD software could hardly identify the very small difference of a and b, we assumed it to be a pseudo-tetragonal structure (I4/mmm), with a = b = 0.5523 nm and c = 2.5026 nm, to index the Kikuchi patterns [27], where a, b, and c were the lattice parameters of the crystal unit cell. During the scanning in this work, the FESEM accelerating voltage, work distance, and magnification were set to 15 kV, 25 mm, and 20,000, respectively. The scanning area and step were 4.4 × 6.6 µm^2 and 15 nm, respectively. The EBSD is a good method to know the relationship between electrical properties and crystal orientations of ferroelectric materials [27].
3. Results and Discussion

3.1. Electrical Properties of C\textsubscript{x}S\textsubscript{1–x}BT FeFETs with Varying x

The electrical properties of Pt/C\textsubscript{x}S\textsubscript{1–x}BT/HAO/Si FeFETs with $x = 0$, 0.1, 0.2, 0.5, and 1 were reported in our former work [19]. $I_d-V_g$ curves are shown in Figure 1a, with $V_g$ scanning from $-4$ V to $6$ V, and then back to $-4$ V. During the scanning, the drain voltage ($V_d$) was set to 0.1 V. The source voltage ($V_s$) and substrate voltage ($V_{sub}$) were kept to zero. Drawing directions of the $I_d-V_g$ hysteresis loops were counter-clockwise in the cases of $x = 0, 0.1, 0.2$, and 0.5 V, indicating that the origins of the loops were ferroelectric. MWs of the C\textsubscript{x}S\textsubscript{1–x}BT FeFETs were 0.75 V ($x = 0$, namely, SBT), 0.89 V ($x = 0.1$), 0.84 V ($x = 0.2$), and 0.43 V ($x = 0.5$). In the case of CBT ($x = 1$), the MW was almost zero, but, more exactly, the loop direction was clockwise, indicating that the CBT was not ferroelectric and that the CBT FeFET showed weak charge-injection behavior in the $I_d-V_g$ measurement.

The polarization, $P$, of the C\textsubscript{x}S\textsubscript{1–x}BT FeFETs was also measured as a function of $V_g$, as shown in Figure 1b. During the $P-V_g$ measurements, $V_d$, $V_s$, and $V_{sub}$ were set to 0 V. Note that the $V_g$ was applied across all the stacked layers, which included C\textsubscript{x}S\textsubscript{1–x}BT, HAO, and the interfacial layer between HAO and Si, and the surface potential of the silicon. While $V_g$ changed between $-4$ V and $6$ V, half the peak-to-peak amplitudes of polarization ($P_{hppa}$) [21,30], were 2.56 $\mu$C/cm$^2$ ($x = 0$), 2.22 $\mu$C/cm$^2$ ($x = 0.1$), 2.12 $\mu$C/cm$^2$ ($x = 0.2$), 1.46 $\mu$C/cm$^2$ ($x = 0.5$), and 0.93 $\mu$C/cm$^2$ ($x = 1$). The MWs on $P-V_g$ curves, i.e., the voltage differences when $P = 0$, were 0.72 V ($x = 0$), 1.18 V ($x = 0.1$), 0.86 V ($x = 0.2$), 0.56 V ($x = 0.5$), and 0.1 V ($x = 1$). Drawing directions of the $P-V_g$ hysteresis loops for all cases were counter-clockwise. As a non-volatile memory FeFET cell, a large coercive field of the C\textsubscript{x}S\textsubscript{1–x}BT is preferred rather than a spontaneous or remnant polarization if an appropriate $P_{hppa}$ (typically 2.5 $\mu$C/cm$^2$) is attained [30].

3.2. EBSD Characterization Results for C\textsubscript{x}S\textsubscript{1–x}BT FeFETs with Varying x

The EBSD scanning results are shown in Figures 2 and 3. Figure 2a–e are inverse pole figure maps, where every point of the C\textsubscript{x}S\textsubscript{1–x}BT was shaded with a color guided by the color code unit triangle according to its orientation (Figure 2f). In the map (Figure 2), the different colors represent the different orientations. The red color point designated as (001) means that the c-axis of the grain is parallel to the film normal. The green color point designated as (100) means that the a-axis of the grain is parallel to the film normal. When the points with the same crystal orientation are accumulated together and make an area of one color, this is a grain of C\textsubscript{x}S\textsubscript{1–x}BT observed by EBSD. A neutron diffraction showed that SBT and CBT have spontaneous polarization along the c-axis [31]. Electrical measurements of polarization versus electric field ($P-E$) curves of epitaxial SBT thin films supported the a-axis directed spontaneous polarization [32,33]. Hence the direction of spontaneous polarization of C\textsubscript{x}S\textsubscript{1–x}BT can be regarded as the a-axis, and the more green color in the EBSD map (Figure 2f) can be attributed to larger polarization. Figure 3 indicates the unit triangles of inverse pole figures, in which one black point represents one unique orientation of the C\textsubscript{x}S\textsubscript{1–x}BT.

The crystal orientation data of grains can also be characterized by the angle $\psi$ (Figure 4a) between the film normal and the grain c-axis. Here the EBSD distribution density was integrated over with respect to the other Euler angles. Orientation distributions as a function of $\psi$ for C\textsubscript{x}S\textsubscript{1–x}BT FeFETs with $x = 0, 0.1, 0.2$, and 0.5 are shown in Figure 4b–e, respectively. The crystal orientations in the SBT ($x = 0$), C\textsubscript{0.1}S\textsubscript{0.9}BT ($x = 0.1$), and C\textsubscript{0.2}S\textsubscript{0.8}BT ($x = 0.2$) are broadly distributed in the range of $0^\circ < \psi \leq 90^\circ$. On the other hand, the distribution of C\textsubscript{0.5}S\textsubscript{0.5}BT ($x = 0.5$) shows a large distribution below $20^\circ$, representing the near-c-axis oriented crystallization. Average values of the grain diameters (Figure 2a–d) and crystal orientation angles (Figure 4b–e) of the C\textsubscript{x}S\textsubscript{1–x}BT with $x = 0, 0.1, 0.2$, and 0.5 were statistically calculated with the standard deviations as shown in Figure 5a,b.
0.2, 0.5, and 1. CxS1–xBT crystallization annealing were performed in O2 ambient for 30 min at 813 °C for x = 0 and at 800 °C for the others. (c) Schematic drawing with voltage terminals for the metal–ferroelectric–insulator–semiconductor (MFIS) type FeFET. The polarization, P, of the CxS1–xBT FeFETs was also measured as a function of Vg, as shown in Figure 1b. During the P–Vg measurement, Vd, Vs, and Vsub were set to 0 V. Note that the Vg was applied across all the stacked layers, which included CxS1–xBT, HAO, and the interfacial layer between HAO and Si, and the surface potential of the silicon. While Vg changed between −4 V and 6 V, half the peak-to-peak amplitude of polarization (P_hppa) [21,30], were 2.56 μC/cm$^2$ (x = 0), 2.22 μC/cm$^2$ (x = 0.1), 2.12 μC/cm$^2$ (x = 0.2), 1.46 μC/cm$^2$ (x = 0.5), and 0.93 μC/cm$^2$ (x = 1). The MWS on P–Vg curves, i.e., the voltage differences when P = 0, were 0.72 V (x = 0), 1.18 V (x = 0.1), 0.86 V (x = 0.2), 0.56 V (x = 0.5), and 0.1 V (x = 1). Drawing directions of the P–Vg hysteresis loops for all cases were counterclockwise. As a non-volatile memory FeFET cell, a large coercive field of the CxS1–xBT is preferred rather than a spontaneous or remnant polarization if an appropriate P_hppa (typically 2.5 μC/cm$^2$) is attained [30].

Figure 2. Electron backscatter diffraction (EBSD) inverse pole figure map of C$_x$S$_{1-x}$BT layer in the FeFET stacks with (a) x = 0; (b) x = 0.1; (c) x = 0.2; (d) x = 0.5; and (e) x = 1; (f) Color coded unit triangle.
In the map (Figure 2), the different colors represent the near distribution of C with the standard deviations as shown in Figure 5. In each Figure of (a–e), integration of number fraction as a function of ψ makes 1.0.

Figure 3. EBSD inverse pole figure unit triangle of $C_{x}S_{1-x}BT$ layer in the FeFET stacks, with (a) $x = 0$; (b) $x = 0.1$; (c) $x = 0.2$; (d) $x = 0.5$; and (e) $x = 1$.

Figure 4. (a) Definition of angle $\psi$, and EDSD analyses of crystal orientation distribution represented as a function of $\psi$ of the $C_{x}S_{1-x}BT$ layers in the FeFETs with (b) $x = 0$; (c) $x = 0.1$; (d) $x = 0.2$; and (e) $x = 0.5$. In each Figure of (b–e), integration of number fraction as a function of $\psi$ makes 1.0.
According to the EDX maps for the Bi and Ta (Figure 6d,e), the noisy multi-color-dot area outside the future will provide a sure solution. The second explanation is that grains in the areas were crystalized with random orientations, but they were exhibited lower Bi and higher Ta intensity peaks than the spot inside j, while both spots had exactly overlapped Ca peaks. A magnified SEM image at the position i in Figure 6a indicated that the spot outside j and k, which was in the multi-color-dot area in Figure 2e, consisted of tiny grains as small as 20 nm (Figure 6g). By these experimental results, there are possible two explanations for the multi-color-dot areas. The first explanation is that grains in the areas were crystalized with random orientations, but they were as small as the resolution limit of EBSD. Hence Kikuchi bands could not be observed. The second one is that grains were not well crystalized yet. From the latter view point, a possible phase was Bi-substituted CaTa₂O₆ on the multi-color-dot area, whose crystallization temperature was much higher than the present annealing temperature of about 800 °C [34,35]. Further investigation in the future will provide a sure solution.
The XRD spectra of the C$_x$BT with $x = 0.1$ and 0.2 have narrow and strong non-$c$-axis peaks of (115) and (200). They do not have the $c$-axis oriented (008) peak. On the other hand, C$_{0.5}$S$_{0.5}$BT shows the (008) $c$-axis peak as well as the (115) peak but does not have the (200) peak. The XRD measurements of the $c$-axis orientation more in the C$_{0.5}$S$_{0.5}$BT than in the C$_x$S$_{1-x}$BT with $x = 0, 0.1,$ and 0.2 are in good agreement with the EBSD characterization, which showed the C$_{0.5}$S$_{0.5}$BT orientated near the $c$-axis direction (Figure 4e). The XRD of the CBT seemed insufficiently crystallized because the (115) peak got weaker and broader than those of SBT and C$_x$S$_{1-x}$BT of $x = 0.1$ and 0.2, and the (008) and (200) peaks did not appear. The insufficient crystallization of the CBT was supported by EBSD observation of a major area occupied by multi-color dots (Figure 2e).

Figure 6. (a) Gray-colored energy dispersive X-ray spectroscopy (EDX) map of the integrated counts. The grains $j$ and $k$ are the same grains appearing in Figure 2e. The EDX element mapping of (b) O; (c) Ca; (d) Bi; and (e) Ta. Each color bar at the top right in (b–e) represents a scale of intensity counts of the element. The color for the zero intensity would be black; (f) EDX spectra both on the area $j$ and on the multi-color-dot area, where the counts are normalized to the O peak; (g) SEM image at the spot $i$ shown in (a).

3.4. X-ray Diffraction for C$_x$S$_{1-x}$BT

The XRD spectra of C$_x$S$_{1-x}$BT are shown in the Figure 7. Samples of Pt/CSBT/HAO/Si with non-patterned Si were used [19]. The SBT and C$_x$S$_{1-x}$BT with $x = 0.1$ and 0.2 have narrow and strong non-$c$-axis peaks of (115) and (200). They do not have the $c$-axis oriented (008) peak. Further investigation in the future will provide a sure solution.
Figure 7. X-ray diffraction (XRD) profiles of C$_x$S$_{1-x}$BT with (a) $x = 0$; (b) $x = 0.1$; (c) $x = 0.2$ (d) $x = 0.5$; and (e) $x = 1$. The intensities were normalized to the Si (400) peak intensity. Modified from [19].

3.5. Comparison of Electrical Properties with Results of EBSD and Other Characterizations

In the EBSD maps of Figure 2a–c, many grains with rather uniform size and non-c-axis orientation were recognized on SBT, C$_{0.1}$S$_{0.9}$BT, and C$_{0.2}$S$_{0.8}$BT layers. As a function of the angle $\psi$ between the film normal and the grain c-axis (Figure 4a), the crystal orientations of the SBT, C$_{0.1}$S$_{0.9}$BT, and C$_{0.2}$S$_{0.8}$BT layer were broadly distributed in the wide range of $0^\circ < \psi \leq 90^\circ$ as shown in Figure 4b–d. In fact, the average values of the $\psi$ were about 50$^\circ$ regarding the C$_x$S$_{1-x}$BT with $x = 0$, 0.1, and 0.2 (Figure 5b). The XRD profiles of the C$_x$S$_{1-x}$BT with $x = 0$, 0.1, and 0.2 in Figure 7, which have the (200) and (115) peaks without the (008) peak, are consistent with the wide range $\psi$ distributions of the crystal orientations observed by the EBSD. Since spontaneous polarization of C$_x$S$_{1-x}$BT is expected to exist along the a-axis, inclusion of the film-normal a-axis component is required to obtain polarization versus electric field ($P$–$E$) hysteresis curves of the C$_x$S$_{1-x}$BT, where the $E$ is applied across the C$_x$S$_{1-x}$BT film. Regarding the C$_x$S$_{1-x}$BT with $x = 0$, 0.1, and 0.2, the wide range $\psi$ distributions observed by EBSD (Figure 4b–d) agreed with the large MWs of the C$_x$S$_{1-x}$BT FeFETs (Figure 1a) due to the inclusion of the a-axis components in the C$_x$S$_{1-x}$BT film-normal directions, which were also supported by Figure 7.

In the case of the C$_{0.5}$S$_{0.5}$BT FeFET, the EBSD map (Figure 2d) showed many grains painted in nearly red colors, which indicated c-axis-preferred crystal orientations. Figure 4e also indicated the c-axis-preferred crystal orientations of the C$_{0.5}$S$_{0.5}$BT by the large number of fractions below 20$^\circ$. As shown in Figure 5b, the average value of $\psi$ was 37$^\circ$, which was about 13$^\circ$ lower than those of C$_x$S$_{1-x}$BT with $x = 0$, 0.1, and 0.2. In the XRD profile of the C$_{0.5}$S$_{0.5}$BT in Figure 7, the inclusion of c-axis crystal orientation was confirmed by the (008) peak. Figure 7 indicated that the C$_{0.5}$S$_{0.5}$BT had the (115) peak but had no (200) peak corresponding to the a-axis orientation. The c-axis-preferred crystal orientations are expected to show very small ferroelectric-polarization switching by imposing bipolar $V_g$ pulses. Actually, the C$_{0.5}$S$_{0.5}$BT FeFET had smaller MW than the C$_x$S$_{1-x}$BT with $x = 0$, 0.1, and 0.2 (Figure 1a). The increase of a noisy multi-color-dot area of the C$_{0.5}$S$_{0.5}$BT (Figure 2d) can be another reason for the small MW of the C$_{0.5}$S$_{0.5}$BT FeFET because it would be non-ferroelectric in the area. In the C$_{0.5}$S$_{0.5}$BT FeFET, therefore, the ferroelectric behavior was weakened, resulting in the memory window 0.43 V being much narrower than those for the FeFET of $x = 0$, 0.1, and 0.2 (Figure 1a).

In the CBT FeFET case, more than half of the EBSD map was occupied by the multi-color-dot areas (Figure 2e). This suggests insufficient crystallization of such areas, in which no ferroelectricity is expected. The XRD profile in Figure 7 showed only a weak and broad peak at the (115) position, which also indicated the insufficient crystallization of the CBT. The non-ferroelectric $I_d$–$V_g$ and $P$–$V_g$ curves of the CBT FeFET in Figure 1a can be understood by the EBSD and XRD investigations.

3.6. EBSD Characterization for C$_{0.1}$S$_{0.9}$BT with Various Annealing Temperatures

The EBSD characterization was also performed to investigate the influence of annealing temperature ($T_a$) on the C$_{0.1}$S$_{0.9}$BT crystallization. Figure 8 shows the EBSD map of C$_{0.1}$S$_{0.9}$BT in the FeFET annealed
at $T_a = 748, 755, 763, 775, 788, 800, 813, 823,$ and $833 \, ^\circ C$. For $T_a = 748 \, ^\circ C$, several grains were found, but noisy multi-color-dot areas covered most parts of the scanning area. For $T_a = 755 \, ^\circ C$, although the multi-color-dot areas still occupied more than half the map, grain size and number were increased in comparison with those for $T_a = 748 \, ^\circ C$. In the case of $T_a \geq 763 \, ^\circ C$, grains with certain crystal orientations covered the most scanning area. In the temperature range from $T_a = 775 \, ^\circ C$ to $833 \, ^\circ C$ (Figure 8c–i), the grains had uniform sizes and random crystal orientations. Multi-color-dot areas were located only on the grain boundaries in Figure 8c–i, without significant differences among the figures.

Figure 8. EBSD map of $C_{0.1}S_{0.9}$BT FeFETs with different annealing temperature, (a) $748 \, ^\circ C$, (b) $755 \, ^\circ C$, (c) $763 \, ^\circ C$, (d) $775 \, ^\circ C$, (e) $788 \, ^\circ C$, (f) $800 \, ^\circ C$, (g) $813 \, ^\circ C$, (h) $823 \, ^\circ C$, and (i) $833 \, ^\circ C$. Color coded unit triangle is the same as Figure 2f.
The inverse polar figures (Figure 9a–i) showed a similar tendency without significant differences from Figure 8a–i. The memory windows of these FeFETs that were reported [19] are shown in the Figure 10 as a function of \( T_a \). The MW of the \( C_{0.1}S_{0.9}BT \) FeFET with \( T_a = 748 \) °C was 0 V. The MW with \( T_a = 755 \) °C was 0.43 V. With further increases of \( T_a \) from 763 °C to 813 °C, the MW became as large as 0.8 V–0.9 V. More exactly, at \( T_a = 788 \) °C and 800 °C the MWs exhibited the maximum. After exceeding the maximum region, the MWs were gradually decreased. MW = 0.68 V was obtained at \( T_a = 833 \) °C.

![Figure 9](image)

**Figure 9.** EBSD inverse pole figure of \( C_xS_{1-x}BT \) FeFETs with different annealing temperature. (a) 748 °C, (b) 755 °C, (c) 763 °C, (d) 775 °C, (e) 788 °C, (f) 800 °C, (g) 813 °C, (h) 823 °C, and (i) 833 °C.

![Figure 10](image)

**Figure 10.** Memory windows vs. annealing temperature curve of \( C_xS_{1-x}BT \) (\( x = 0.1 \) ) FeFETs. Modified from [19].

The increasing MW with increasing \( T_a \) from 748 °C to 763 °C can be explained by the increase of the size and frequency of grains and by the decrease of the noisy multi-color-dot areas. Crystallinity may be improved with further increases of \( T_a \). The FeFETS showed the maximum MW in the \( T_a \) range from 788 °C to 800 °C. The decreases of MWs at \( T_a > 800 \) °C may be caused by the increase of a SiO\(_2\)-like interfacial layer (IL) grown between the I layer and the S surface in the MFIS of the FeFETs. As shown in [14,16,17,19], during the annealing for the \( C_xS_{1-x}BT \) crystallization, the IL is grown to normally a few nano-meters-thick. The IL may get thick as the \( T_a \) increases from 800 °C to 833 °C.
In the MFIS, three capacitances of $F$, $I$, and $IL$ and a capacitance of $S$ (appearing when the depletion layer is formed) are connected in series and share the $V_x$. The voltage across the $C_{S1-x}BT$ is reduced when the IL becomes thick because the voltage across the IL is increased. With the voltage decrease across the $C_{S1-x}BT$, the MW may become narrow as $T_a$ is increased from $800 \, ^\circ\text{C}$ to $833 \, ^\circ\text{C}$.

4. Conclusions

The EBSD method was used to characterize the $\text{Ca}_{x}\text{Sr}_{1-x}\text{Bi}_2\text{Ti}_2\text{O}_9$ layer inside the FeFET stacks. The distributions of grain size and orientation of $C_{S1-x}BT$ with $x = 0$ (SBT), $0.1$, $0.2$, $0.5$, and $1$ (CBT) were presented in the inverse polar figure maps and the unit triangles of EBSD. The grain size and crystal orientation distributions depended on the content $x$ of $C_{S1-x}BT$. There were more uniform and smaller grains with random orientation in SBT, $C_{0.1}\text{S}_{0.9}BT$, and $C_{0.2}\text{S}_{0.8}BT$. In $C_{0.5}\text{S}_{0.5}BT$, grains got larger and the major grains were orientated near the $c$-axis direction. Since spontaneous polarization exists along the $a$-axis, these EBSD results explain well the reason that the memory windows of SBT, $C_{0.1}\text{S}_{0.9}BT$, and $C_{0.2}\text{S}_{0.8}BT$ FeFETs were much wider than that of the $C_{0.5}\text{S}_{0.5}BT$ FeFET. EBSD investigation also revealed the existence of noisy multi-color-dot areas on which no Kikuchi-bands appeared, indicating that the areas were non-ferroelectric. EBSD characterizations of the $C_{0.1}\text{S}_{0.9}BT$ FeFETs with various annealing temperatures from $T_a = 748$ to $833 \, ^\circ\text{C}$ were performed. As the $T_a$ was raised from $748 \, ^\circ\text{C}$ toward $763 \, ^\circ\text{C}$, grain size and number increased, and the noisy multi-color-dot areas decreased. When $T_a$ was increased from $763 \, ^\circ\text{C}$ to $833 \, ^\circ\text{C}$, the EBSD maps showed the $C_{0.1}\text{S}_{0.9}BT$ mostly composed of grains with rather uniform sizes and random crystal orientations. Good consistency among the EBSD investigations of the $C_{S1-x}BT$ and memory window widths of the $C_{S1-x}BT$ FeFETs could be discussed.

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