**Design of ECG Front End Amplifier Based on CMOS OTA**

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**Abstract.** The low-noise and low-power amplifier, an important part of ECG recordings, remains a vital challenge in the biomedical instrumentation amplifier field. This paper describes a method of using the capacitive feedback structure and the MOS-bipolar pseudo-resistor to reject the DC offset and amplify signals down to the milli-hertz range. This study used the noise efficiency factor (NEF) to quantify the tradeoff between power and noise. Fabricated in a 180 nm CMOS process, the amplifier consumes 1.44 µW, and achieves the input referred noise of 3.89 µV rms. The calculated NEF is 18.07, while the corresponding common-mode rejection ratio (CMRR) is 87.72 dB. The device achieves low-noise, low-power and appropriate CMRR, which provides a reference for the design of biomedical instrumentation amplifier.

1. **Introduction**

Real-time monitoring of human health characteristics has been playing an important role in the medical field in recent decades, setting higher requirements for convenience and efficiency of health monitors. These health characteristics are usually extracted from the body physiological signals, like electroencephalogram (EEG) [1], electrocardiogram (ECG) [2] and electromyography (EMG) [3], among which the ECG is the most commonly used one due to the accessibility [4]. With the launch of more and more smart watches and sports bracelets such as IWatch, a large number of wearable devices have been widely used, which also makes the use of wearable biomedical devices become a normal in the near future [5, 6].

ECG is a technique for recording the electrical activity of the heart from the surface of the body and it also has several forms of waves [7]. In order to record and reflect the electrical activities of different parts of the heart, electrodes are placed in different parts of the human body [8]. The basic logic sequence of Wearable ECG sensing technology is as follows. Firstly, the weak physiological electric signal is detected and amplified by the ECG amplifier circuit. Secondly, the analog signal is converted into digital signal for subsequent processing by using the corresponding data acquisition card [9].

The amplifier is a very important part in the field of ECG which has been studied by some researchers. Recent theoretical developments have revealed that the use of multiple-input operational transimpedance amplifiers (OTAs) can reduce the number of OTAs for realizing the fifth-order low-pass filter architecture, which can make the structure become very beneficial by reducing the number of active devices and power consumption [10]. Besides, another common strategy used to monitor human
body is to use a three-stage ECG amplifier composed of LNA, TBPF, and VGA [11]. Nonetheless, this increasing complexity in circuit design tends to increase the energy consumption.

This work aims to develop an overarching framework to design a convenient Wearable ECG sensor device based on a classical amplifier structure model, which can measure the ECG signal and display the physical condition in time, in order to make it easier to monitor the body and manage living habits [12]. Different from the literature mentioned above, in this design, the principle of low-pass filter in the circuit of OTA is the only needed, and the high pass filter that meets the requirements can be realized by using the internal capacitance of OTA. The thesis here has made significant contributions to the field of biomedicine and electrical engineering.

2. Methods
In our research, a low-noise and low-power capacitive feedback amplifier based on an OTA for ECG recordings is used. The system used a feedback framework, which is mainly composed of the following parts: capacitive feedback amplifier, human body circuit (HBC), and OTA.

2.1. Capacitive feedback amplifier
The capacitive feedback amplifier is a common type of amplifier in biomedical recordings [13], which uses capacitors to reject the DC offset from the three skin electrodes and to set the mid-range gain. As shown in Figure 1, the mid-band gain of the device is \( A_M \), which is fixed by the relation between the input capacitor \( C_1 \) and the feedback capacitor \( C_2 \) leading to \( A_M = \frac{C_1}{C_2} \). And the bandwidth of the device is \( f_0 \), where \( g_m \) is the transconductance of the OTA. As shown in Figure 1 and Figure 2, transistors \( M_a - M_h \) are eight MOS-bipolar devices work as “pseudo-resistors” to provide larger resistance values. When \( V_{GS} \) is negative, they act as diode-connected PMOS devices. When \( V_{GS} \) is positive, the parasitic source-well-drain pnp bipolar transistor is enabled, and it operates as a diode-connected bipolar device. The added resistance \( r_{inc} \) is very high when small voltages across this device. The four MOS-bipolar devices are connected in series to decrease the distortion of the large output signal. The low-frequency cutoff of the amplifier is \( f_L \) which is found by \( \frac{1}{2\pi r_{inc} C_2} \). Although having a long time constant, large changes in the input result in large voltages through the MOS-bipolar element, thereby decreasing its incremental resistance while providing fast settling times [12].
2.2. OTA, HBC and NEF
The OTA architecture as shown in Figure. 3 has a lot of advantages such as high open-loop gain, only one capacitor is required for frequency compensation, large input range of common-mode input, high CMRR and low transistor count. The details of this kind of OTA architecture have been extensively described in previous works, with wide usage in bio-medical applications [14], switched-capacitor applications [15], operational transconductance amplifier-capacitor filters [16], fourth-order bandpass filters and relaxation oscillators [17, 18].

HBC is the necessary part in this work to identify the performance of the amplifier, consisting of voltage source, current source, capacitors, resistors, and electrode model (see Figure. 4(b)). As shown in Figure. 4(a), we use a 2 kΩ resistor in series with a parallel-combination of a 1 MΩ resistor and a 50 nF capacitor to set the electrode model which could simulate the impedance of real electrodes. The voltage source is used to simulate the voltage generated when the heart is beating. Resistors are on behalf of the resistance value of left arm, right arm and right leg. The noise when the heart is beating is simulated by current source and capacitors.

Since we are addicted in reducing noise with the tight power budget, the weigh among power, noise,
and BW should be considered. The NEF determines the weigh.

\[
\text{NEF} = V_{\text{in, rms}} \sqrt{\frac{2I_{\text{tot}}}{\pi U_T 4kT \cdot BW}}
\]  

(1)

Where \(V_{\text{in, rms}}\) is the voltage of the total equivalent input noise voltage, \(I_{\text{tot}}\) is the current total supply of the amplifier total supply current, \(U_T\) is the thermal voltage and its value is \(\frac{KT}{q}\), and the value of the amplifier bandwidth is BW. The NEF of an amplifier that utilizing a single bipolar transistor (with no \(\frac{1}{f}\) noise) is one; The value of NEF of all practical circuits is larger than one \cite{19}.

Figure 3. The inside structure of the OTA.

Figure 4. The inside structure of the HBC: (a) electrode model; (b) HBC circuit.

3. Results

In this research, the output of ECG signal amplifier based on CMOS OTA was simulated on LTspice.
The most important component that used in this research was CMOS 180 nm. 180 nm refers to the length of the gate, that is, the length of the conductive channel. The smaller the length is, the faster the electron migration rate is and the better the CMOS performance is. It is the basic part of OTA and pseudo resistance described below. The circuit is mainly composed of HBC, CMOS OTA and the pseudo resistor. When building the circuit diagram, HBC, electrode model and OTA were indispensable parts of the research. Their existence made the results more real, reliable and accurate. There are many capacitors with specific parameters in these modules, whose parameters are very important to the output signal, such as frequency range, CMRR.

Table 1 lists the data comparison between this design and previous similar studies. The total current of the circuit is at a relatively low level-1.44 μA, which is lower than other designs. ECG front-end amplifier is only composed of one-stage structure, so the power consumption is also lower than them. The front-end amplifier has higher CMRR and lower output noise, which means that when our design is integrated with wearable equipment, the design can more resist the interference of external signals, at the same time, it will not cause greater interference to other signals.

As shown in Figure. 5, the final bandwidth of this design is ~ 100 mHz to ~100 Hz, which is in line with the frequency range of ECG signal. The decibel value corresponding to the two dotted lines is 35.46 dB. Figure. 5 also presents the intermediate frequency gain of this design, and the gain measured at ~ 7 Hz is 38.43 dB, which means that the amplifier has strong amplification ability for weak signal. In the part of output noise, due to the relatively small number of capacitors and CMOS transistors in the circuit, we get a lower output noise, as shown in Figure. 6 (a). CMRR can also not be ignored when evaluating whether a circuit has its use value. This is schematically shown in Figure. 6 (b) that CMRR is 87.72 dB at 60 Hz, which means the amplifier can effectively resist interference.

| Table 1: The parameter comparison between this design and the previous similar design [20]. |
|---------------------|--------|--------|--------|--------|
|                      | [2]2017| [4]2015| [10]2012| [11]2018|
| \( I_{tot}[\mu A] \) | 15     | 10.08  | 8.5    | 1.44   |
| \( V_{DD}[V] \)     | 1.2    | 1.455  | 49.2   | 4.9    |
| \( Power[\mu W] \)  | 18     | 5.04   | 28.05  | 32     |
| \( Gain[\text{dB}] \) | 52     | 4.3    | 3.2    | 1.94   |
| \( IRN[\mu V_{rms}] \) \* | 4.2   | 0.86   | 3.2    | 3.89   |
| \( CMRR \)          | 65     | 0.5    | 88     | 1.44   |
| \( Output noise \)  | ——     | ——     | ——     | 220.75 |
| \( \mu V/Hz^{1/2} \) | ——     | ——     | ——     | ——     |
| \( Employed Capacitance \) \* | ——     | ——     | ——     | 466.16p|
| \( F \)             | ——     | ——     | ——     | ——     |
| \( Block Included \) | Pre-amp| Pre-amp| Pre-amp| Pre-amp|

\*IRN: Total integrated input-referred noise.
Figure. 5. The bandwidth of the design ranges from \( \sim 100 \text{ mHz} \) to \( \sim 100 \text{ Hz} \), which is close to the frequency range of ECG signal (Dotted lines). Furthermore, differential gain of the design is around 38.43 dB, measured at 7.82 Hz (Chain-dotted line).

4. Discussion

The CMOS OTA in this design is a two stage Millar compensated OTA. In its internal schematic diagram, the bias current is 10 nA, and the MOS transistors in it all have appropriate width of the conductive channel, which can better ensure the accuracy of data. Besides, the internal capacitor value is related to the bandwidth, so doing more precise calculations to get it is necessary. After that, in this two-stage structure, it includes the application of differential pairs and current mirror. The current mirror is a transistor biased in the active region, which is used as the active load of the amplifier to accurately process the mirror current.

As seen in the last chapter, the CMOS OTA is used to complete the design. However, classic 3-op-amp is the initial choice which is easier to grasp the starting point. In the later research, we find that the
CMOS OTA could better fit ECG signal specifications. Furthermore, the number of transistors and the stage of the structure are less than classic op-amp and even some previous studies, the structure is more concise and advanced, and the resulting output noise is also smaller, which is consistent with the trend of low power consumption required by today's wearable sensor technology.

In addition to the OTA structure, the use of pseudo resistors is also a certain need. Different from the feedback loop of the general op-amp, which uses a simple resistor as the feedback impedance, four MOS-bipolar pseudo resistors are used as the impedance in the feedback structure of this circuit. The structure consists of four PMOS transistors in cascade. The current flowing through them is 180 nA and the width of conductive channel is the same. On this basis, there is a larger input resistance, smaller DC bias voltage and smaller noise, which will interfere with the output signal. Furthermore, the circuit will have a greater voltage gain.

In the hypothesis section before the experiment, we hope our circuit had very low power consumption. The experimental results fully confirm our hypothesis. Compared with the previous research, for our OTA structure is simpler, the power consumption of our circuit is less than 80 μW which is obtained in another design.

Although there is no condition to carry out real human experiments, in the simulation process, HBC is used in the research to simulate the real human situation, which is close to the reality to the greatest extent. Clearly, the reason for using HBC is not just to approach the real situation, it also plays a role of energy supply in this circuit diagram. If HBC is not used, this experiment would only stay in the simplest simulation stage, which is not necessarily feasible.

It can be seen from the above that this front-end amplifier circuit has lower power consumption and suitable CMRR, but at the same time, the electrode offset voltage (EOV) and chip size are not considered in the design, which will directly become the key point of whether it can be used in daily life. In the following further research, discussing and designing on EOV and chip volume will be more important, and we will also address the design of material object of circuits.

5. Conclusion

We designed a Wearable ECG sensor in order to measure the ECG signal and display the body condition in real time, so as to monitor the body and manage the living habits conveniently. By simulating the output of the designed ECG amplifier based on CMOS OTA on Allspice platform, the results show that the circuit bandwidth is about 100 Hz, which is in line with the frequency range of ECG signal. The capacitance used is ~ 466.46 pF, which means low output noise. In addition, the circuit has low power consumption of 1.44 μW, suitable CMRR and good installation adaptability. To sum up, we found that this design can achieve the original goal, that is, a front-end amplifier with low power consumption and appropriate CMRR, which can fit the design of Wearable ECG sensor. Therefore, people in the medical field and electrical engineering field may be interested in this paper. The work involved in this paper can contribute to the ECG detection and display in the medical field, provide design ideas for the research personnel of wearable devices, and provide inspiration and reference for electrical engineers in the design of similar sensors.

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