Silicon carbide (SiC) is a suitable material for power device applications, owing to its superior physical properties, such as wide bandgap, high critical electric field, and high thermal conductivity. A unique advantage of SiC over other compound semiconductors is that it can be thermally oxidized to give high-quality silicon dioxide (SiO₂). Thus, SiC metal-oxide-semiconductor field effect transistors (MOSFETs) have attracted much attention for low-loss and fast power switches. SiC MOSFETs have, however, suffered from the low channel mobility due to the high interface state density (Dₓ) at a SiC/SiO₂ system.

Although the physical origin of the interface states remains uncertain, several methods were found to passivate the defect levels. For instance, post-oxidation annealing in nitric oxide (NO) or nitrous oxide (N₂O) (interface nitridation) or in a gas mixture of phosphoric chloride (POCl₃), oxygen (O₂), and nitrogen (N₂) (POCl₃ annealing) is effective in reducing the Dₓ near the conduction band edge (E_c) of SiC. However, since these methods rely on the incorporation of foreign atoms [nitrogen (N) or phosphorus (P)], generation of extrinsic defects at the interface and in the oxide have been pointed out as a problem. By interface nitridation, generation of very fast interface states and oxide hole traps was indicated, and for POCl₃ annealing, generation of electron and hole traps in the oxide was suggested.

It is more desirable if high-quality interface can be obtained without introducing foreign atoms into the interface and oxide. In recent years, ultrahigh-temperature oxidation (~1400 °C–1600 °C), thin (~15 nm) oxidation with rapid cooling (>600 °C min⁻¹), and post-oxidation argon (Ar) annealing have been reported to be effective in reducing the interface states, without introduction of foreign atoms. In this study, we demonstrate that the Dₓ reduction by the post-oxidation Ar annealing is not the effect of “pure” thermal annealing but the effect of unintentional very-low-oxygen-partial-pressure (pO₂) annealing.

Samples employed in this study were n-type SiC (0001) MOS capacitors (donor concentration (N_D) ~10¹⁶ cm⁻³). Oxides were formed by dry oxidation at 1300 °C for 30 min followed by annealing in either pure Ar or Ar containing very small amount of oxygen (O₂) (0.001%–0.1%; low-pO₂) at 1300 °C–1500 °C for 1 min. In the case of pure-Ar annealing, Ar was purified so that the concentration of contained oxygen was below 100 ppt. For low-pO₂ annealing, the partial pressure of oxygen was strictly controlled by supplying a gas directly from a gas cylinder containing the mixture gas of Ar and O₂. The low-pO₂ annealing was performed at 1 atm in an induction heating furnace with a fast cooling rate (>600 °C min⁻¹), in order to minimize the additional oxidation during the cooling phase. The furnace was evacuated down to 10⁻² Pa by a turbo molecular pump prior to the gas introduction so as to purge residual gas species in the furnace. The oxide thicknesses were about 51–58 nm and the gate electrodes were aluminum (Al) (diameter: 0.5–1 mm). All of the measurements were conducted at room temperature.

Figure 1 shows the current density-electric field (J–E) characteristics of the prepared MOS capacitors. Here, the oxide electric field, Eox, was estimated by Eox = Vthox/Vox, where V and Vox are the applied voltage and the oxide thickness, respectively. We see that the as-oxidized and low-pO₂-annealed samples exhibit typical J–E characteristics with Fowler–Nordheim tunneling current at a sufficiently high oxide field (>7 MV cm⁻¹). In contrast, a high leakage current is observed even at a very low field (<0.2 MV cm⁻¹) in the case of pure-Ar-annealed sample.

In order to clarify the origin of the leakage current, secondary ion mass spectrometry (SIMS) measurements were performed. Figure 2 depicts the depth profiles of carbon concentration in the SiC/SiO₂ samples acquired by SIMS. After annealing in pure Ar, a high concentration of carbon atoms (>10²⁰ cm⁻³) is detected in the oxide, as reported in Ref. 6. Note that such a pure Ar ambient cannot be realized simply by introducing Ar immediately after the oxidation process, since residual oxygen remains in the oxidation furnace. In our case, we excluded the effect of oxygen by performing the Ar annealing in a leak-tight resistive heating furnace which is different from the oxidation furnace. In the case of low-pO₂-annealed sample, the carbon concentration in the oxide is close to the detection limit (~10¹⁰ cm⁻³). Thus, carbon atoms are ejected from the interface during the annealing, and they remain in the oxide in the case of pure Ar annealing, which leads to the severe degradation of oxide dielectric property (Fig. 1). In the case of low-pO₂ annealing, slight oxygen (0.001%–0.1%) removes the ejected carbon atoms by oxidizing them into gas species such as CO or CO₂, leading to the suppression of the leakage current (Fig. 1).

Figures 3(a) and 3(b) show the capacitance–voltage (C–V) characteristics of the MOS capacitors; annealed in the temperature range of 1300 °C–1500 °C in (a) O₂ (0.001%) and in (b) O₂ (0.1%). Both the frequency dispersion and C–V stretch-out are reduced by the low-pO₂ annealing, which is

---

**Reduction of interface state density in SiC (0001) MOS structures by low-oxygen-partial-pressure annealing**

Takuma Kobayashi, Keita Tachiki, Koji Ito, and Tsunenobu Kimoto

Department of Electronic Science and Engineering, Kyoto University, Nishikyo, Kyoto 615-8510, Japan

E-mail: kobayashi@semicon.kuee.kyoto-u.ac.jp

Received January 16, 2019; revised January 27, 2019; accepted January 30, 2019; published online February 14, 2019

We report that annealing in low-oxygen-partial-pressure (low-pO₂) ambient is effective in reducing the interface state density (Dₓ) at a SiC (0001)/SiO₂ interface near the conduction band edge (E_c) of SiC. The Dₓ value at E_c ~ 0.2 eV estimated by a high (1 MHz)-low method is 6.2 × 10¹² eV⁻¹ cm⁻² in as-oxidized sample, which is reduced to 2.4 × 10¹² eV⁻¹ cm⁻² by subsequent annealing in O₂ (0.001%) at 1500 °C, without interface nitridation. Although annealing in pure Ar induces leakage current in the oxide, low-pO₂ annealing does not degrade the oxide dielectric property (breakdown field ~10.4 MV cm⁻¹).

© 2019 The Japan Society of Applied Physics
indicative of reduction in $D_{\text{IT}}$ near $E_C$. The effective fixed charge densities estimated from the flat-band voltage shift were $2.4 \times 10^{12}$ cm$^{-2}$ (negative) and $1.2 \times 10^{12}$ cm$^{-2}$ (positive) in the as-oxidized sample and the sample annealed in O$_2$ (0.001%) at 1500 °C, respectively.

Energy distributions of $D_{\text{IT}}$ extracted by a high (1 MHz)-low method$^{24}$ are compared in Fig. 4. In the case of annealing in O$_2$ (0.001%), the $D_{\text{IT}}$ is effectively reduced by increasing the temperature, and takes its minimum values (e.g. $2.4 \times 10^{12}$ eV$^{-1}$ cm$^{-2}$ at $E_C - 0.2$ eV) after annealing at 1500 °C. For O$_2$ (0.1%) annealing, in contrast, the $D_{\text{IT}}$ at $E_C - 0.2$ eV increases from $4.9 \times 10^{12}$ to $6.3 \times 10^{12}$ eV$^{-1}$ cm$^{-2}$ by increasing the temperature from 1300 °C to 1500 °C. The oxide thicknesses of the as-oxidized and low-$p_{\text{O}_2}$-annealed samples determined by spectroscopic ellipsometry are summarized in Fig. 5. We see that the oxide thickness hardly changes (<1 nm) with the annealing in O$_2$ (0.001%), whereas, the thickness increases by about 6 nm with annealing in O$_2$ (0.1%) at 1500 °C. Such results indicate that the $D_{\text{IT}}$ is determined by the balance of the removal and creation of the interface defects during the low-$p_{\text{O}_2}$ annealing, and that it is important to avoid excessive oxidation of SiC during the low-$p_{\text{O}_2}$ annealing to suppress additional defect generation. Note that, in SiC MOS systems, it is known that the incorporation of impurities, such as boron (B),$^{25}$ P,$^{15,16}$ and sodium (Na),$^{26,27}$ in a high concentration of about $10^{20}$–$10^{21}$ cm$^{-3}$ leads to remarkable reduction of $D_{\text{IT}}$. From SIMS measurements, we confirmed that the concentration of B, P, and Na atoms near the SiC/SiO$_2$ interface is at least below $2 \times 10^{16}$ cm$^{-3}$ after the low-$p_{\text{O}_2}$

Fig. 1. (Color online) Current density–electric field ($J$–$E$) characteristics of as-oxidized, pure-Ar-annealed, and low-$p_{\text{O}_2}$-annealed SiC MOS structures.
annealing, indicating that the observed $D_{IT}$ reduction by the low-$p_{O2}$ annealing (Fig. 4) is not due to the impurity contamination.

We indicate that a high density of positive fixed charge (1.2 x 10^{17} \text{cm}^{-2}) resides in the sample annealed in O$_2$ (0.001\%) at 1500 °C. It should be noted that, it is difficult to estimate the real positive fixed charge density simply from the flat-band voltage shift in the case of as-oxidized sample, since electrons trapped at the acceptor-like interface states act as “effective” negative charge and compensates the positive charge. Thus, the positive charge may even reside in the as-oxidized sample and may become apparent by the low-$p_{O2}$ annealing owing to the reduction of acceptor-like interface states (Fig. 4).

Here we discuss the possible atomic configurations of the major interface defects in SiC/SiO$_2$ systems. It has widely been believed that the carbon byproducts at (or near) the interface are the origin of interface states in SiC MOS structures, since carbon is one of the host atoms of SiC. We confirmed that a high concentration of carbon atoms is ejected from the interface by the pure Ar annealing (Fig. 2), which also suggests that the interface defects are related to carbon species. A result of density-functional calculations indicates that, among the various forms of carbon atoms that are frequently observed at a SiC/SiO$_2$ interface during molecular dynamics simulations, ethylene-like structure (SiO$_2$ > C = C > SiO$_2$) creates defect levels near the $E_C$ of SiC. Si$_2$O$_2$ > C = C > Si$_2$O$_2$ defect and Si$_3$O$_3$ > C = O defect are also possible candidates, since they also create defect levels near the $E_C$. It is also suggested that oxygen helps the dissociation of interface carbon defects by reducing the energy of the structure after the dissociation by terminating the Si dangling bonds at the interface. Thus, the low-$p_{O2}$ annealing may reduce the $D_{IT}$ near $E_C$ (Fig. 4) by dissociating the carbon defects while preventing the additional generation of carbon defects caused by excessive oxidation of SiC.

In conclusion, we found that low-$p_{O2}$ annealing is effective in reducing the $D_{IT}$ at a SiC (0001)/SiO$_2$ interface without introduction of foreign atoms. For annealing in O$_2$ (0.001\%), the $D_{IT}$ decreased by increasing the temperature up to 1500 °C, whereas, for O$_2$ (0.1\%) annealing, the $D_{IT}$ increased by increasing the temperature from 1300 °C to 1500 °C. The oxide thickness hardly changed (<1 nm) with the annealing in O$_2$ (0.001\%), whereas the thickness increased by about 6 nm with annealing in O$_2$ (0.1\%) at 1500 °C. Thus, during the low-$p_{O2}$ annealing, it is of importance to remove the interface defects by oxidizing them, while preventing the excessive oxidation of SiC to minimize additional defect creation. In the case of pure Ar annealing, carbon atoms are ejected from the interface, and they remain in the oxide, which leads to the severe degradation of oxide dielectric property. In low-$p_{O2}$ annealing, however, slight oxygen (0.001\%–0.1\%) removes these carbon atoms by oxidizing them into gas species such as CO or CO$_2$, leading to the suppression of the leakage current.

Acknowledgments This work was supported in part by the JSPS KAKENHI (Grant Number 15030483), the Super Cluster Program, and Open Innovation Platform with Enterprises, Research Institute and Academia (OPERA) Program from the Japan Science and Technology Agency.