Design Exploration and Security Assessment of PUF-on-PUF Implementations

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Abstract—We design, implement, and assess the security of several variations of the PUF-on-PUF (POP) architecture. We perform extensive experiments with deep neural networks (DNNs), showing results that endorse its resilience to learning attacks when using APUFs with 6, or more, stages in the first layer. Compositions using APUFs with 2, and 4 stages are shown vulnerable to DNN attacks. We reflect on such results, extending previous techniques of influential bit analysis to assess stage bias in APUF instances. Our data shows that compositions not always preserve security properties of PUFs, the size of PUFs used plays a crucial role. We implemented a testchip in 65 nm CMOS to obtain accurate measurements of uniformity, uniqueness, and response stability for our POP implementations. Measurement results show that minimum bit error rate is obtained when using APUFs with 8 stages in the first layer, while fewer APUF stages lead to a large spread of bit error rate across different chips.

Index Terms—arbiter PUF, composite, learning attacks, DNN

I. INTRODUCTION

Strong physical unclonable functions (PUFs) offer a solution for the counterfeiting problem of integrated circuits (ICs). They harvest device specific characteristics to generate a digital fingerprint used to authenticate an IC. It is infeasible to manufacture two identical PUFs. Different PUF instances will always produce distinct fingerprints. Strong PUF authentications are performed with a challenge-response protocol [4]. The mapping from challenges to responses is unique for each PUF. This is unlike traditional authentication methods, where two ICs can be programmed to produce the same proof of identity.

However, researchers have shown that learning attacks are able to predict responses after seeing a limited number of challenge-response pairs (CRPs) [15]. A well known countermeasure for learning attacks is to surround the PUF with keyed cryptographic operations such as SHA or AES [3]. Although effective in increasing security, such solutions have large area cost, which restricts the range of applications that can benefit from strong PUFs. Constructing low-cost strong PUFs capable of withstand learning attacks is an unsolved problem, and an active field of research.

In this paper, we study the effect of composite architectures in the learning resilience and response stability of PUFs. In particular, we designed and implemented a testchip in 65 nm CMOS with several variations of the PUF-on-PUF (POP) architecture, introduced by Wu et al [26]. POP uses a two layers construction, shown in Fig. [1] where responses from first layer serve as input to the second layer. Our implementation also adds new features to POP, including support for multiple first round evaluations, and temporal majority voting (TMV) for noise removal. We use APUFs as basic building block. Our testchip includes different implementations of the first layer using APUF of 2, 4, 6, 8, 12, and 24 stages.

To assess the security of our POP implementations, we performed extensive learning attacks varying number of rounds and size (number of stages in first layer APUFs). We show that attacks using deep neural networks (DNNs) fail to predict responses when the first layer uses APUFs of 6, 8, 12, and 24 stages. We also found counter-intuitive results for learning resilience. POP implementations using 2, and 4 stage APUFs in the first layer are vulnerable to DNN attacks. Moreover, increasing the number of rounds brought no improvements against DNN attacks, in fact, it made small sized POP implementations more vulnerable. We reflect on such results, extending previous techniques of influential bit analysis to assess stage bias in APUF instances [2]. To shed light on why depth increase is ineffective to thwart learning attacks, we show that the hamming-distance of first layer responses decreases as the number of rounds increases. Therefore, small APUFs in the first layer limit the challenge space of the second layer APUF, showing that compositions not always preserve security properties of PUFs — the size of PUFs used plays a crucial role.

Other contributions of our work include extensive measurements from our testchip, including uniformity, uniqueness, and bit error rate for different implementation sizes. We show that there is an optimal number of stages to improve APUF...
Composite constructions require larger CRP datasets, and longer training time, but still, security against DNN attacks remain an unsolved problem [5], [19], [23], [25], [26]. The work by Wu et al [26] highlights the vulnerabilities of prior composite PUFs against cryptanalysis attacks [17], and introduces a new architecture which is resistant against such attacks, denoted as PUF-on-PUF (POP). In this work, we explore the design space of POP, implementing a testchip in 65 nm CMOS process, and performing an extensive security assessment on various POP implementations.

III. Notation

An arbiter PUF (APUF) with an n-bit challenge is denoted as an APUF size n, or n-APUF. An n-APUF-POP refers to a POP implementation where all APUFs in first layer have n stages. Vectors are written in bold text, and are indexed from zero, for example, \( \mathbf{c} = (c_0, c_1, \ldots, c_{n-1}) \). The hamming weight and hamming distance functions are denoted as \( \text{HW}(\cdot) \), and \( \text{HD}(\cdot) \), respectively. The narrow, and wide temperature sets refer to \{0 °C, 20 °C, 60 °C\}, and \{-30 °C, 0 °C, 20 °C, 60 °C, 80 °C\}.

IV. Background

The essential difference between strong PUFs and conventional authentication methods is the lack of blank samples. Two authentic ICs using PUFs will never produce the same digital fingerprint, regardless of their programmed memory content. The challenge response protocol used to authenticate PUFs still requires the programming of a chip identifier, which is used to fetch the corresponding CRP database enrolled for that PUF instance. Authentication is performed by inquiring the PUF with a subset of the challenges in the database. To avoid replay attacks, challenges are never used more than once. If the number of correct responses exceeds an application defined threshold, the IC is deemed authentic.

A. Performance Metrics

The quality assessment of strong PUFs uses metrics that evaluate uniformity, uniqueness, and stability of responses.

1) Uniformity: estimates the ratio of zeros and ones in PUF responses. It is also known as “normalized hamming weight”. Ideal uniformity is 0.5, which indicates, on average, equal number of zeros and ones.

2) Uniqueness: estimates the distance between responses from multiple instances. It is also known as “normalized hamming distance”. Ideal uniqueness is 0.5, which indicates that, for the same set of challenges, on average, half responses will differ.

3) Bit error rate (BER): estimates reproducibility of responses under several environmental conditions. Bit error rate (BER) reports a ratio of bits (responses) that differ from their enrolled value. BER ideal value is 0%, which indicates no incorrect responses during measurement. Other literature may use the term reliability, which simply denotes (100% - BER).
B. Authenticating with Non-ideal Bit Error Rate

For an IC to be deemed authentic, the number of correct responses must exceed a response threshold, otherwise the authentication fails. Response threshold is a system defined parameter which is set according to PUF response stability. If the threshold is expressed as a percentage of correct responses needed to authenticate, we can argue that it must be less than (100% - BER), otherwise the PUF is unlikely to successfully authenticate due to noisy responses.

As discussed in [21], Fig. 4 simulates PUFs with different BER. Threshold was set 5% below (100% - BER). For example, when simulating an authentication using 200 CRPs, with a PUF that has 10% BER, 170 correct responses are required to authenticate. As shown in Fig. 4, the probability of authentication failure falls exponentially with the number of CRPs used to authenticate. For example, for a 1% failure rate, a PUF with 10% BER will require 200 CRPs, while if the PUF BER is increased to 20% or 30%, the required CRPs to achieve the same failure rate will increase to 350, and 400, respectively.

V. THE PUF-ON-PUF ARCHITECTURE

The PUF-on-PUF (POP) architecture was proposed by Wu et al. [26]. It utilizes composition as an alternative to increase strong PUF resilience to learning attacks. Our implementation of POP is shown in Fig. 1. It uses a two layers construction, where responses from the first layer serve as input to the second layer. Our implementation adds support for multiple first round evaluations as a low-cost alternative to increasing the number of layers. In other words, first layer responses can be reused as input challenge for additional evaluation rounds, prior to the final second layer evaluation.

Our implementation of POP uses APUFs as building block, for its simplicity, stability, and well understood security characteristics. The input challenge has 64 bits, and the number of APUF instances in the first layer matches the number of challenge bits. The first layer can be implemented with APUFs of any size, while the second layer APUF must match the number of stages with the number of APUF instances in the previous layer. In this paper, we restrict ourselves to first layer implementations where all APUFs have the same size.

Each APUF instance uses temporal majority voting (TMV) to filter out noise, as shown in Fig. 2. TMV performs a predetermined number of repeated evaluations, returning the most frequent response. It is important to notice that TMV is not applied to the overall composition, but to each individual APUF instance.

As described by Wu et al, careful wiring of challenge bits in the first layer is required to avoid cryptanalysis attacks [26]. The wiring pattern must apply each challenge bit in more than a single PUF instance. The POP wiring for a first layer implementation using 4-APUF is shown in Fig. 3. Each 4-APUF, is connected to the input challenge at offset i. If the sum of offset and APUF size is greater than 63, the challenge bits simply wrap around. When performing evaluations with multiple rounds, the challenge register is re-loaded with responses from APUFs in the first layer. Responses of each APUF are used as challenge bit i for first layer re-evaluation. Similarly, second layer evaluations are performed by wiring responses of each APUF, in the first layer to the stage i of the second layer APUF.

VI. TESTCHIP DESIGN

High-level models offer a convenient alternative to test the security of new PUF architectures. The delay of each APUF stage follows a well understood normal distribution. When noise is not considered, PUF responses from high-level models tend to be indistinguishable from responses obtained from silicon. This allows designers to perform an early assessment of uniformity, uniqueness, and resilience to learning attacks. However, response stability is a key performance metric which can not be accurately estimated without silicon implementation. For this reason, we designed and implemented a testchip in 65 nm CMOS technology. Our testchip is used to evaluate the response uniformity, uniqueness, and bit error rate of our POP implementations.

We use APUF as building block. Our APUF instances are designed with tri-state inverters and NAND-based arbiter, as shown in Fig. 5. Layout of APUFs is custom-made to ensure identical routing of delay paths. The layout of an APUF with 2 stages is shown in Fig. 6. We designed APUFs with 2, 4, 6, 8, 12, 24, and 64 stages. Area information for each APUF is shown in Table 4. Height and width dimensions are
listed in $\mu m$, while area is provided in $\mu m^2$, and normalized by the NAND2 area. Our APUF cells have the same height as logic gates from the commercial standard-cell library, which allows automatic placement and routing by EDA tools. This methodology significantly reduces design effort, without losing the performance of a custom approach.

Die photo and layout are shown in Fig. 7. Die photo and layout view of implemented design. TMV logic is oversized since it uses larger counters than necessary.

Die photo and layout are shown in Fig. 7. The cells highlighted in yellow implement a JTAG interface and test logic. APUF instances used in the first layer are highlighted in blue, they account for 64 instances of each APUF cell size, including 2, 4, 6, 8, 12, and 24 stages. In total, 384 APUFs are instantiated to construct 6 different first layer implementations. The PUF with 64 stages, used in the second layer, is highlighted in red. Cells highlighted in green implement the round control logic and TMV counters. The TMV logic is largely oversized for exploratory reasons, using a total of 65 counters, each with 24-bits. Results reported in section VII show that more than 15 TMV evaluations bring diminishing returns in response stability. Therefore, the size of TMV counters may be significantly reduced. Further area optimization is possible if the first layer PUFs do not evaluate simultaneously, allowing operation with fewer TMV counters. This impacts throughput, but significantly reduces the TMV hardware size.

In summary, each testchip includes 6 different first layer implementations. Each implementation uses a different APUF size, including 2, 4, 6, 8, 12, and 24 stages. The first layer does not mix APUFs of different sizes. There is a single 64-APUF instance, therefore, the testchip includes only one second layer implementation.

VII. MEASUREMENT RESULTS

We measured a total of 10 dies to accurately assess uniformity, uniqueness, and response stability. Each die contains 6 different first layer implementations, and a single 64-APUF which implements the second layer. We performed enrollment at 20 $^\circ$C. To calculate bit error rate, CRPs are evaluated 100 times at the narrow and wide temperature sets, which denote $\{0^\circ C, 20^\circ C, 60^\circ C\}$, and $\{-30^\circ C, 0^\circ C, 20^\circ C, 60^\circ C, 80^\circ C\}$, respectively. Temporal majority voting (TMV) is used in all evaluations. TMV with a single (one) repeated evaluation is equivalent to an ordinary evaluation without temporal majority voting. Boxplots show the distribution of mean values for different chips — they include 10 different mean values of the respective performance metric, one from each tested chip.

Bit error rate measures the stability of PUF responses. Fig. 8(a), and (b) plot bit error rate for POP implementations with various APUF sizes in the first layer, for the narrow and wide temperature sets, respectively. A single first layer evaluation was performed (one round). A total of 15 repeated evaluations were used for TMV. The median BER for 24-APUF-POP is 19.2%, and 22.1% in the narrow, and wide temperature sets, respectively. Minimum bit-error rate is found with 8-APUF-POP, where we measured median BER of 17.1%, and 19.7%
for the narrow, and wide temperature sets. Small APUFs, with
2, 4, and 6 stages, showed a steep increase in the spread of bit error rate across different chips. This is likely related to stage bias, which is discussed in section VIII-C.

Temporal majority voting (TMV) performs multiple evaluations of a PUF instance to remove noise from responses. We assessed the impact of TMV in POP response stability. Results plotted in Fig. 9 show bit error rate for different TMV settings. In (a), the median BER for 8-APUF-POP in the narrow temperature set, is 23.5%, 18.5%, 17.1%, and 16.5%, for 1, 7, 15, and 31 repeated TMV evaluations. Increasing the number of repeated evaluations quickly reaches diminishing returns. A similar trend was observed for other sizes of POP, in both temperature sets. Therefore, 15 TMV offers a reasonable compromise between throughput and bit error rate for composite evaluations.

Our POP implementations adds support to multiple first layer evaluation rounds. We assessed the response stability for 1, 2, 3, and 4 evaluation rounds, using 1 k CRPs. Results are shown in Fig. 10 (a), (b), (c), and (d) for 2, 4, 8, and 24 stages in first layer APUFs, respectively. All implementations showed median BER near 20% for single round evaluations. Larger APUFs in the first layer lead to lower response stability when using additional rounds, as expected. Similarly to Fig. 8 small APUFs in the first layer show a wide spread of BER measurement across multiple chips. Therefore, median BER for 2-APUF-POP, and 4-APUF-POP, may be a misleading performance metric, if not accompanied by the corresponding standard deviation.

We also measured uniformity and uniqueness of POP instances in our testchip. The former, captures the balance of zeros and ones in the final response, while the later, measures the normalized hamming distance of different instances. Measured uniformity and uniqueness for various rounds are plotted in Fig. 11 for 2-APUF-POP in (a, c), and 8-APUF-POP in (b, d). Both uniformity, and uniqueness showed a small variation in performance values across different sizes of POP. The median uniformity for 2-APUF-POP, and 8-APUF-POP, with one evaluation round, is 0.55, and 0.52, respectively. The corresponding median uniqueness is 0.50 for both 2-APUF-POP and 8-APUF-POP. Other POP implementations with different sizes presented similar results.

In section VIII-D we show that small APUFs in the first layer lead to poor hamming distance in the intermediate responses. Such result is not noticeable when evaluating the final output of POP, but it is likely the cause of security vulnerabilities studied in the next section.

VIII. SECURITY ASSESSMENT

The primary motivation for composite strong PUFs is to increase security against learning attacks. We start this section
discussing the applicability of logistic regression, cryptanalysis, and reliability attacks to POP. Next we describe how deep neural networks (DNNs) are used to model strong PUFs. We assess the learning resilience of our POP implementations against DNNs using up to 10 M CRPs. Next, we discuss influential bits, and hamming distance of intermediate responses, showing that compositions do not necessarily preserve the security properties of PUFs — the size of composing PUFs plays a crucial role.

A. Learning Attack Results

1) Logistic regression and cryptanalysis: logistic regression (LR), and cryptanalysis attacks are described in [15] and [17]. LR uses gradient descent to find coefficients of a linear model that minimizes the prediction error. Modeling POP with LR is non-trivial, since careful mathematical manipulation is required for an adequate linear fitting [26]. The cryptanalysis attack exploits the mapping of challenge bits to different APUFs in the first layer. It was shown in [26], that such attacks are ineffective against POP due to the wiring scheme used in the first layer — every challenge bit is fed to more than a single first layer PUF.

2) Reliability based attacks: reliability based attacks were initially introduced in [1]. The key insight is that CRPs with small delay difference are more susceptible to noise. Authors demonstrated the attack against XOR-APUFs using response stability as side-channel information. The POP architecture, however, uses a construction where noisy CRPs in the first layer affect the final output with different probabilities. Such characteristic is described in detail in section VIII-B. Hence, analogously the the formal proof provided for the interpose PUF in [13], reliability-based attacks are unlikely to obtain better prediction accuracy than other learning attacks that do not exploit response stability information.

3) Deep neural networks: deep neural networks (DNNs) are emerging as an efficient attack technique capable of learning complex PUF structures. DNNs do not require a mathematical model of the PUF being modelled. We use a 12-layer DNN architecture proposed in [5] for our DNN attacks. The input and output layers have 64, and 2 units, respectively. Hidden layers have 2000 units. Our attack experiments use CRPs from a high-level model to avoid noise as confounding factor for prediction accuracy. Table II summarizes DNN attack results using 10 M CRPs. The Implementation column specifies POP parameters used, for example, the 2-APUF-POP uses 64 instances of 2-APUF in the first layer. All our POP implementations use a 64-APUF instance in the second layer. The Rounds column refers to the number of first layer evaluations used, prior to the second layer evaluation. The BER column reports the median worst bit error rate among the temperature points of \{0 °C, 20 °C, 60 °C\}. The Area column reports the silicon area (normalized by the NAND2 area) for all APUF instances, excluding control, and TMV logic. The Accuracy column reports the accuracy obtained after 72 h of training using a Quadro P4000 GPU.

Results reported in Table II show that the DNN model achieved accuracy of 81.8% for 2-APUF-POP using 1 round. This implementation has median BER of 20.0%, and uses an area of 1.2 k ND2. Increasing the size of APUFs in the first layer to 4, 6, 8, 12, and 24 stages reduces prediction accuracy to 74.7%, 48.0%, 51.5%, 49.6%, and 54.4%, respectively. Therefore, our results suggest that increasing the size of APUFs in the first layer strengthens the POP composition, at an area and response stability cost.

We explored multiple first layer evaluation rounds as a cost-effective approach for strengthening POP against learning attacks. Table II reports bit error rate and prediction accuracy result for 2-APUF-POP and 24-APUF-POP, using 1, 2, 4, and 8 rounds. Response stability falls as more evaluation rounds are used. We measured median BER of 17.7% and 31.7% for 2-APUF-POP and 24-APUF-POP when using 2 evaluation rounds, respectively. Prediction accuracy for 24-APUF-POP did not shown significant change when varying number of rounds, however, prediction accuracy for 2-APUF-POP increased when more rounds are used. This result was unexpected, and counter-intuitive. We carefully reflect on possible explanations for such outcomes in the next sections.

B. Probability of Output Change

The DNN prediction accuracy when using small APUFs in the first layer, reported in section VIII-A deserves additional investigation. In this section, we use the concept of strict avalanche criterion (SAC) to look into the differences between APUFs of various sizes.

As defined in [24], if a cryptographic function is to satisfy the strict avalanche criterion (SAC), then, each output bit should change with a probability of one half, whenever a single input bit is complemented. In [11], this concept was extended to strong PUFs, where authors measure the probability of output response change given a single bit change in the input challenge. Furthermore, it was demonstrated that the probability of output change for the APUF, depends on the distance between toggled bit and the arbiter.
bins applied to stages near the arbiter are more likely to cause a change in the response. This result is reproduced in Fig. 12 (a). Using simulation, we estimate the probability of output change for 64-APUF when evaluating a random challenge, before, and after it is XORed with a mismatch pattern. When HW(e) = 1, a single challenge bit will toggle between evaluations. In the plots of Fig. 12 the position of the toggled bit is shifted towards the arbiter, and is denoted as mismatch pattern shift. When the pattern shift is zero, probability of output change is 5.5%, but as the toggled bit nears the arbiter, probability of output change increases, reaching 90.5% at the last APUF stage. This result can be intuitively explained by the wire permutation present in every stage of the APUF, and the cumulative nature of the delay path.

We also estimate the probability of output change when two consecutive challenge bits are toggled. This is plotted in Fig. 12 (a) as HW(e) = 2, showing that, for 64-APUF, the probability of output change remains nearly constant, at 8%. This result represents a more realistic view on the SAC criterion for APUFs, where minimal input change requires toggling two adjacent stages, instead of a single one. The same technique was applied to APUF of various sizes in Fig. 12 (b). The estimated probability of output change for APUFs with 24, 12, 8, 6, 4, and 2 was 13.2%, 19%, 23.6%, 26.5%, 33.5%, and 50.5%, respectively. The increase in probability of output change for smaller sizes of APUFs gives an important insight to understand the results found in section VIII-A the influence of individual stages on the output increases, as APUF size decreases.

C. Influential Bits and Stage Bias

Influential bits were previously studied in [2], [20], [27]. Authors showed how distinct challenge bits have different influence on the output of a bistable ring PUF (BR-PUF). Based on the value of a few influential challenge bits, it is possible to predict responses with high accuracy [2]. To avoid confusion with previous work nomenclature, we denote the influence of each challenge bit as stage bias. This section performs an assessment of stage bias in APUFs of various sizes, leading to conclusions that help explain learning attack results obtained in section VIII-A.

Algorithm 1 Stage bias assessment for an APUF instance.

1: let NC be the number of challenges
2: let CW be the challenge width in bits
3: let y and n be zero initialized matrices of size (2, CW)
4: for i = 0 to NC − 1 do
5:   c = RandomizeChallenge()
6:   r = EvaluateResponse(c)
7:     p = 0
8:   for j = 0 to CW − 1 do
9:     p = p ⊕ c[j]
10: for j = 0 to CW − 1 do
11:     t = c[j]
12:     p = p ⊕ t
13:     y[t, j] += (r ⊕ p)
14:     n[t, j] += 1
15: end for
16: end for
17: end for
18: y = y/n

Fig. 12. Simulated probability of output change when evaluating a random challenge, before, and after it is XORed with a mismatch pattern. Results in (a) for 64-APUF, and in (b) for smaller APUF sizes. The HW(e)=2 only includes mismatch patterns where nonzero bits are adjacent.

To the best of our knowledge, no previous literature reports the measurement of stage bias in APUFs. In [2], authors used an algorithm described in [14] to assess stage bias of BR-PUFs, however, the algorithm is only suitable for monotone Boolean functions. Therefore, we introduce Algorithm 1 for measuring stage bias in APUFs. The main idea is to evaluate a set of randomized challenges, keeping track of responses statistics per stage, and per challenge bit value. The key insight of Algorithm 1 is on line 14. When summing the response, r, for challenge bit value t, at stage j, the response is conditionally inverted (XORed) with p, where p is a parity bit (reduced XOR operation) over the challenge bits from position j + 1, onwards. If the number of twisted stages after position j is odd, the value of p will be 1, which then inverts the response r. The final stage bias is stored in the matrix y, indexed by challenge bit value, and by stage position. Notice that the division operation in line 18 is element-wise.

Using CRPs from our testchip, we calculated stage bias for different APUF sizes. The results are shown in Fig. 13. A distinction was made for stage bias when ci is zero (first row), and one (second row), since challenge bits select between two pairs of inverters in each stage, and each pair exerts different influence on the response. The plots (a, e), (b, f), (c, g), and (d, h), refer to APUFs with 2, 4, 8, and 24 stages, respectively. The results refer to a single APUF instance of each size (not the overall POP composition).

Results plotted in Fig. 13 express the probability of response
Stage bias

Fig. 13. Stage bias calculated using CRPs from our testchip. The first row shows biases when $c_i = 0$, while the second row shows biases when $c_i = 1$. The plots (a, c), (b, f), (c, g), and (d, h), refer to APUFs with 2, 4, 8, and 24 stages, respectively. We used 100 k CRPs to calculate stage bias for the 24-APUF, while APUFs of 2, 4, and 8 stages were enumerated (all CRPs were collected).

$r$ being equal to $(1 \oplus p_i(c))$, given challenge bit $c_i$ is zero, or one. The term $p_i(c)$ is denoted as parity. It will have a value of one when the challenge imposes an odd number of wire twists between the stage under analysis $i$, and the arbiter. Parity is calculated as

$$p_i(c) = \bigoplus_{j=i+1}^{n-1} c_j.$$  

For example, based on data from Fig. 13 (f) for the 4-APUF, the probability of $r = 1$, given $c_3 = 1$, is 0.38, or equivalently, probability of $r = 0$, given $c_3 = 1$, is 0.62. In this case, the parity calculated by Eq. 1 is zero, since there are no stages that could twist the wires between position 3 and the arbiter. As an alternative example, the stage bias reported in Fig. 13 (c) for the 8-APUF shows that, the probability of $r = (1 \oplus p_i(c))$, given $c_4 = 0$, is 0.76. Therefore, all challenges which have $c_4 = 0$, and an even number of ones in $(c_5, c_6, c_7)$, have 0.76 probability of evaluating to 1. Moreover, challenges that have $c_4 = 0$, but an odd number of ones in $(c_5, c_6, c_7)$, have a 0.76 probability of evaluating to 0.

Large stage bias deviations from 0.5 are undesirable, since they grant certain challenge bits an unfair influence over the response. It was also shown that large stage bias can be exploited by attackers [2]. To understand how stage bias varies across APUFs of different sizes, we simulated 100 APUF instances using 3 k CRPs, and plotted the stage bias distribution in Fig. 14. The stage bias mean is 0.5 for all APUF sizes, but the standard deviation for 24, 8, 4, and 2-APUF are 0.12, 0.20, 0.29, and 0.40, respectively. Therefore, we may conclude what is also apparent in the measurements presented in Fig. 13 fewer APUF stages increase the likelihood of large stage bias deviations.

D. Hamming Distance of Intermediate Responses

Previous section assessed the effects of smaller APUFs on stage bias, showing that reducing the size of APUFs creates challenge bits that hold large influence over the final response. Such result motivates an investigation of the hamming distance between responses produced by the first layer of the POP architecture, over multiple rounds (same challenge), and across multiple challenges. Although mathematically similar, we avoid using the term uniqueness for such experiment, since it is not applied to the final POP response.

The normalized hamming distance (HD) measures the distance between two numbers, divided by their length. The normalized HD is herein denoted as distance, for short. For
example, if the distance between two numbers is 0.5, it implies that half the bits of their binary representation differ. Fig. [15](a) plots the average distance between responses produced from the POP first layer, across multiple rounds, for the same challenge, for various APUF sizes. For instance, the data denoted as \((1,2)\)-round reports the average distance between responses produced from first to the second evaluation round. While implementations with 24-APUF show nearly ideal distance of 0.5 across all evaluation rounds, reducing the size of APUFs gradually degrades the distance between responses. In implementations with 2-APUF, the average distance between responses from first to the second round is 0.36, which implies that 64% of response bits from the first evaluation remained unchanged after the second evaluation. As the number of rounds increases, average distance for 2-APUF continues to fall, reaching 0.24 for responses between fourth, and fifth rounds.

We also examine the average distance of first layer responses, across multiple challenges, after 1, 2, 4, and 8 evaluation rounds. Results are plotted in Fig. [15](b). Implementations using 24-APUF show nearly ideal distance of 0.5 across multiple challenges, but reducing the size of APUFs, gradually degrades the distance between responses — this time, across multiple challenges. For example, 2-APUF implementations show average distance of 0.36, 0.30, 0.25, and 0.22 when evaluated with 1, 2, 4, and 8 rounds. Moreover, the data suggests that even with a single evaluation round, small APUFs fail to produce responses with distance near 0.5. Another perspective to such result, is to consider that small APUFs limit the challenge space of the second layer APUF, seriously impacting to the learning resilience of the overall composition.

The poor hamming distance performance of smaller APUFs, likely caused by larger stage bias, is a plausible cause for the learning results observed in section VIII-A. The results in Fig. [15] suggest a strong performance drop for 2 and 4 stages APUFs, which agrees with our attack results, where DNNs failed to obtain generalized knowledge for 6-APUF-POP implementations and above (see section VIII-A). It is also important to notice that our results do not assess the benefits of multiple round evaluations for larger APUFs in the first layer. In terms of prediction accuracy, those implementations were already resilient to DNN attacks with a single round. Our analysis shows, however, that there is no apparent reduction in challenge space when multiple evaluations rounds are used with first layer implementation of 12, and 24 stages.

### IX. Conclusion

We explored the design space of the POP architecture using APUFs of various sizes. We performed extensive DNN attacks to assess the security of POP. Our results endorse POP resilience to learning attacks when using APUFs with 6, or more, stages in the first layer. Compositions using APUFs with 2, and 4 stages are shown vulnerable to DNN attacks. Moreover, POP implementations with 2 stage APUFs in the first layer show a trend of higher prediction accuracy as the number of evaluation rounds increases. To study such result, we extended previous techniques of influential bits to assess stage bias in APUF instances. Our data suggests that small APUFs in the first layer limit the challenge space of the second layer APUF, showing that compositions not always preserve security properties of PUFs. Measurements from our testchip show that minimum bit error rate is obtained when using APUFs with 8 stages, while fewer APUF stages lead to a large spread of bit error rate across different chips.

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