III–V nanowire MOSFETs with novel self-limiting Λ-ridge spacers for RF applications

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Abstract

We present a semi self-aligned processing scheme for III–V nanowire transistors with novel semiconductor spacers in the shape of Λ-ridges, utilising the effect of slow growth rate on 111B facets. The addition of spacers relaxes the constraint on the perfect alignment of gate to contact areas to enable low overlap capacitances. The spacers give a field-plate effect that also helps reduce off-state and output conductance while increasing breakdown voltage. Microwave compatible devices with \( L_g = 32 \) nm showing \( f_T = 75 \) GHz and \( f_{\text{max}} = 100 \) GHz are realized with the process, demonstrating matched performance to spacer-less devices but with relaxed scaling requirements.

Keywords: nanowire, metal–oxide–semiconductor field-effect transistor, radio-frequency, spacers, InGaAs, InP

(Some figures may appear in colour only in the online journal)

1. Introduction

III–V materials such as InGaAs has been widely used in HEMTs for mmWave applications due to its high electron mobility [1–3]. In recent years, high-performance digital MOSFETs made of III–V materials have also been reported and are candidates for replacing Si in order to maintain a high on-current while reducing the supply voltage [4–8]. Another way of improving the performance of CMOS devices is to use nanowires or nanosheets due to the improved electrostatic control gained by surrounding the channel with gates from multiple sides, allowing more aggressive gate length scaling [9, 10]. III–V nanowire MOSFETs and FinFETs have also been studied for RF applications [11, 12] and is an interesting candidate for future mixed applications where analogue and digital function is placed close to each other, for instance in system on Chip (SoC) used in 5G telecommunication and above. One limiting factor for RF MOSFETs is the parasitic capacitance between the highly doped contact regions and the gate contact which increases compared to HEMT devices due to the high-k oxide. Lowering the parasitic capacitances is especially important for nanowire MOSFETs since there is space in between the nanowires that contribute with a parasitic capacitance but not with current or transconductance [13]. This makes the requirement on alignment accuracy very high since any gate overlap on contact regions results in increased parasitic capacitances.

In this paper we propose a novel semi self-aligned InGaAs nanowire MOSFET with self-limited growth of InP ridges with triangular cross-section (Λ-ridges) acting as spacers for use in RF applications. The introduction of InP spacers can reduce the effect of gate-drain and gate-source overlap on transistor performance, while keeping the increase in access resistance small due to the introduction of modulation-doped Si layer in the Λ-ridges [14]. The process also allows...
Figure 1. Schematic illustrations of the RF nanowire MOSFET device with InP Λ-ridge spacers. (a) HSQ exposure and MOCVD growth of InGaAs nanowires. (b) Dummy gate and spacer exposure followed by growth of modulation doped InP self-limiting Λ-ridge bound by 111B facets. (c) Device after stripping of the HSQ resist. (d) Second HSQ dummy gate exposure and contact regrowth. (e) Resist stripping and high-k deposition. (f) T-gate and source drain evaporation.

for low access resistance due to a lack of wide bandgap heterojunction between the ohmic contact and nanowire channel.

2. Device fabrication

The processing starts with e-beam exposure and development of hydrogen silsesquioxane (HSQ) resist to form a SiO-like template for the selective area metalorganic chemical vapor deposition (MOCVD) growth of 7 nm thick and 30 nm wide In$_{0.85}$Ga$_{0.15}$As nanowires on a semi-insulating (100) InP:Fe substrates, figure 1(a). The HSQ lines sets the width and pitch of the nanowires while the growth time sets the thickness. The lines are aligned in the [100] direction, forming nanowires bound by 110 side walls with 45° inclination relative to the (100) top facet. Next, a second HSQ exposure is performed to create a 40 nm dummy gate and 80 nm wide spacer openings aligned in the [011] direction, which will later set the gate length of the device. This is followed by growth of the InP self-limiting Λ-ridges with a layer sequence of 4 nm i-InP, 4 nm Si-modulation doped layer ($N_D = 5 \times 10^{19}$ cm$^{-3}$) and 60 nm thick i-InP. Due to the 45° rotation of the dummy gate compared to the nanowires, the InP ridges are defined by slow growing 111B facets with 54.7° inclination relative to the (100) top facet, as seen in figure 1(b) [15]. Most of the atoms impinging on the 111B facets either migrate to the top (100) facet or reevaporate. As the growth proceeds the (100) becomes smaller due to the minimal growth rate on the 111B facets. In the limit the (100) facet disappears, leading to a ridge with height determined by the width of the base. The width of the Λ-ridges continues to expand by growth on the 111B facets at a near negligible growth rate, which means that for all practical purposes the process can be viewed as being self-limited. Importantly, the gate length and spacer length is set by the separation and width of the Λ-ridges simultaneously and independently of each other, making the spacer placement self-aligned. After a second HSQ dummy gate has been exposed to avoid growth in the channel region, 20 nm thick Sn-doped In$_{0.63}$Ga$_{0.37}$As contact regions ($N_D = 5 \times 10^{19}$ cm$^{-3}$) are grown, figure 1(d). This second dummy gate must be same width or wider than the initial dummy gate, but not wider than the dummy-gate plus the two spacer regions for the scheme to work. InGaAs is known to have negligible growth rate on 111B facets in MOCVD, however, we cannot exclude some minor InGaAs growth due to roughening of the facets by the processing done between growth runs [15, 16].

To finalize the transistor, mesa-isolation, ALD high-k oxide (7 cycles Al$_2$O$_3$ and 37 cycles HfO$_2$) figure 1(e), and TiPdAu T-gate and source drain metals are evaporated, figure 1(f). Figure 2 shows a top-view SEM image of a device after InP ridge growth (figure 2(a)) and a tilted cross-sectional SEM image after the device is completed. In a similar process, we have also fabricated reference spacerless devices without InP ridges. The gate contact will here have a 10 nm overlap against the source and drain n+ regions.

The reason for using the InP Λ-ridge spacers are two-fold. First, separating the n+ contact region and the gate could potentially reduce the parasitic gate-drain and gate-source capacitance. Secondly, the inclusion of a field-plate region in the drain-side has been shown to increase the breakdown voltage and reduce the output conductance of MOSFET devices, due to the reduced maximum electric field at the drain side, minimizing band-to-band tunnelling and short-channel effects. However, including the InP underneath the n+ contact regions as in [14] adds a series resistance in the access regions, which the novel Λ-ridge layout avoids.

The second consideration comes to self-alignment. In a spacer-less layout, the gate should ideally be placed perfectly...
Figure 2. (a) False coloured SEM image of a nanowire device after growth of 80 nm wide InP Λ-ridge spacers, separated by 40 nm, corresponding to figure 1(c). (b) Tilted cross-sectional SEM image of the same device after high-k and gate deposition, corresponding to figure 1(f).

between the two n+ contact regions without any overlap. By using the Λ-ridges, the requirement on perfect alignment can be relaxed and the gate can on purpose be designed wider than the opening between the spacers and overlap the side walls without a significant loss in overlap capacitance. The limitations of this design is that the second HSQ dummy gate must be aligned to the first one. However, due to that the spacers have 111B sidewalls, with very limited growth rate, as long as the edges of the second dummy gate is inside the two Λ-ridges, the n+ contacts will start to grow at the (100) surface on top and between the nanowires outside the channel region. This allows for a misalignment equal to approximately the half of the spacer width, easily accomplished with high-resolution lithography techniques.

3. Results and discussion

We have successfully fabricated nanowire MOSFETs with Λ-ridge InP spacers utilising very limited growth on 111B facets. In figure 3(a) output and figure 3(b) transfer characteristics of a 32 nm gate length device with 80 nm InP spacers are shown with peak transconductance of 300 µS µm −1, consisting of two fingers with 100 nanowires in parallel per finger, giving a total gated nanowire circumference of 7 µm and a total device width of 14 µm. Due to the use of the InP spacers, the device exhibits excellent pinch off at high drain bias up to V_{DS} = 1 V and low gate bias. This is an improvement from our earlier work where the output conductance was considerable already at V_{DS} = 0.75 V for the same gate length [17]. The transistor has a minimum off-current at 100 nA µm −1, with a subthreshold slope of 400 mV/decade, which is a slight reduction compared to a spacer-less reference device with gate length of 52 nm at 500 mV/decade. The output conductance of the two devices at 1 V V_{DS} and 1 V gate overdrive is 200 µS µm −1 even though the gate length is shorter for the device with spacer, indicating the positive effect of the InP spacer. In order to evaluate the high frequency performance of the device, we have measured the transistor RF-gains from 100 MHz up to 67 GHz. Off-chip LRRM calibration and pad deembedding on open/short structures have been performed. In figure 4(a) the RF gain of the transistor with V_{DS} = 1 V and V_{GS} = 1 V is shown. Linear fitting with −20 db/decade gives f_T = 70 GHz and f_{max} = 100 GHz. The measured y-parameters we have fitted a small signal model seen in figure 4(b). The device current and unilateral gain show a roll-off of 20 db/decade and the frequency dispersion in transconductance is less than 10%, indicating that the high-k oxide has a minor effect on the high-frequency device performance.

To be able to extract the parasitic capacitances of the device, we have measured the RF as a function of V_{GS}. For negative biases below V_T, the obtained capacitances are mainly due
to the parasitic capacitance, since at this points the channel is depleted of carriers. The equivalent of the small-signal model is shown in figure 5 for the analysed device in figures 3 and 4 as well as a reference spacer less device with gate length of 52 nm. The spacerless device has been optimised for small gate overlap, with approximately 10 nm gate overlap on each side of gate towards the n+ contact regions, this in comparison with the Λ-ridge device, where the overlap is approximately 40 nm per side. Both devices show similar transconductance around 300 µS µm⁻¹ even though the InP Λ-ridge spacers ads a 80 nm access region, thus the addition of modulation doped InP spacers does not add significantly to the access resistance. At higher gate overdrive, the spacer-less device performs slightly better, possibly due to source-starvation in the Λ-ridge device. Source starvation can limit the transconductance at high gate overdrive due to a lack of carriers in the source-access region [18]. We obtain a parasitic gate capacitance from $V_{GS} - V_T = -0.55$ V of $C_P \approx 5.0$ fF for the ridge device, and $C_P = 5.5$ fF for the spacer less device. Even though the device with the Λ-ridge has a gate overlap which is substantially larger, both $C_{GS}$ and $C_{GD}$ is very comparable to the spacerless device with minimal overlap, up until high-gate overdrive where the charging in the InP spacers starts to play a significant role. To compare and verify the proposed device architecture, we have modelled the parasitic capacitance between the gate and the n+ InGaAs, InGaAs channel and the InP Λ-ridge spacers using a 2D electrostatic model in COMSOL multiphysics. A similar device width of $W = 14$ µm as the fabricated devices is used in the model. The quantum capacitances of the channel quantum well and n+ source regions are taken into account in the model as a distributed capacitance. In the model, we have compared the gate overlap capacitance for 80 nm Λ-ridge InP spacers and for a spacerless layout with varying contact thickness, for both 80 nm InP Λ-ridge spacers and for a spacerless layout with varying contact thickness, for both 80 nm InP spacer and for a spacerless layout. Figure 6 shows the RF behavior for $V_{DS} = 0.2, 0.6$ and 1 V of a device with 80 nm InP Λ-ridge spacers (gate overlap 40 nm) and a spacerless device where the spacerless device has been optimized for small gate overlap on the source and drain regions. (a) RF transconductance, (b) current gain, (c) gate-source capacitance and (d) gate-drain capacitance as extracted from small-signal model.

4. Conclusion

We have successfully fabricated InGaAs nanowire MOSFETS with a processing scheme utilizing the faceting of MOCVD grown InGaAs and InP to include Λ-ridge spacers in a semi

self-aligned process. We have shown that utilizing this scheme, the gate can overlap the spacer regions without a significant loss in overlap capacitance, compared to a non-self-aligned spacerless approach, which considerably relaxes the alignment requirements in the gate definition. The scheme also opens up possibilities to vary the gate length and spacer length independently over the wafer and it is even possible to fabricate asymmetric spacers with larger gate-drain separations for improved $f_{\text{max}}$. The self-limiting Λ-ridge scheme is not limited to nanowires and can also be implemented for planar MOSFETS.
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