Charge Buildup and Leakage Current in Gold/Parylene-C/Pentacene Capacitor under Constant-Voltage Stress

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Abstract
Degradation of metal-insulator-semiconductor (MIS) capacitors of gold/Parylene-C/Pentacene under constant voltage stress (CVS) was investigated to explore the electrical stability and reliability of Parylene C as a gate dielectric in flexible electronics. A stress voltage of fixed magnitude as high as 20 V, both negative and positive in polarity, was applied to each MIS capacitor at room temperature for a fixed duration as long as 10 s. The CVS effects on the capacitance-voltage curve-shift, the time-dependent leakage current and the time-dependent dielectric breakdown were measured and analyzed. CVS is observed to induce charge in Parylene-C and its interfaces with gold and Pentacene. The net induced charge is positive and negative for, respectively, negative and positive gate bias polarity during CVS. The magnitude of the charge accumulated following positive gate CVS is significantly higher than that following negative gate bias CVS in the range of 4 to 25 nC cm$^{-2}$. In contrast, the leakage current during the negative gate stress is three orders of magnitude higher than that during the positive gate stress for the same bias stress magnitude. The charge buildup and leakage current are due to the trapping of electrons and holes near the Parylene-C/Pentacene interface as well as in the Parylene-C layer. Before the application of the CVS, a dielectric breakdown occurs at an electric field of 1.62 MV cm$^{-1}$. After the application of the CVS, the breakdown voltage decreases and the density of the trapped charges increases as the stress voltage increases in magnitude, with the polarity of the trapped charges opposite to that of the stress voltage. The magnitude and direction of the capacitance-voltage curve-shift depend on the trapping and recombination of electrons and holes in the Parylene-C layer and in the proximity of the Parylene-C/Pentacene interface during CVS.

1. Introduction

The stability of flexible devices is a major reliability concern. To enhance environmental stability, passivation/encapsulating layers are used. Another critical reliability concern is device stability against electrical stress. Flexible devices often operate under continuous voltage biases which can affect performance dramatically [1, 2]. The general reason for bias instability is charge trapping [2]; electrode, insulator and semiconductor interfaces easily trap charges, resulting in device-parameter shifts and degraded performances. Therefore, processes that take place at bimaterial interfaces must be characterized and controlled.

Parylene C is commonly used as a dielectric material for electronic applications [1, 3–9]. Pinhole-free films of this polymer function well as protection layers [10] to minimize device degradation caused by exposure to air and moisture. In recent years, this polymer has been used for flexible substrates due to its desirable mechanical properties (yield strength of 55.1 MPa and static Young’s modulus of 2.76 GPa) and the ease of deposition in both micrometer- and nanometer-thickness regimes [11]. In addition, we have recently shown that Parylene-C columnar...
microfibrous thin films are viable candidates for use as interlayer dielectrics [3–5].

Moreover, Parylene-C thin films exhibit superior electrical insulation characteristics, high breakdown strength (∼2.5 MV cm⁻¹, according to the manufacturer’s specification) and low dielectric loss [11], not only as passivation layers but also as gate dielectrics for organic field-effect transistors (OFETs) [12–14]. In fact, there is a limited number of materials that can be simultaneously used as a substrate, gate dielectric and encapsulation layer simultaneously while exhibiting a high-performance level comparable to materials dedicated to a specific application [1, 2].

Parylene-C films have been extensively studied [1, 12–20] as gate dielectrics in OFETs. However, very little is known about the electrical stability and reliability of Parylene C and its interfaces with the active layers in these devices. Current-voltage measurements are commonly made to study the electrical degradation of OFETs under constant-voltage stress (CVS) [20]. However, capacitance-voltage measurements are more sensitive than current-voltage measurements for investigating interface characteristics [21]. As exemplified in table 1, researchers previously used either current-voltage measurements or capacitance-voltage measurements, but not both, to study the electrical degradation under CVS. For more comprehensive understanding, we investigated the electrical stability and reliability of Parylene C as a gate dielectric using both capacitance-voltage measurements and current-voltage measurements.

We undertook a systematic analysis of gold/Parylene-C/Pentacene metal–insulator–semiconductor (MIS) capacitors. In this paper, the effects of CVS, the capacitance-voltage curve-shift and time-dependent dielectric-breakdown (TDDB) are experimentally analyzed. Needless to add, the gold/Parylene-C/Pentacene system is the heart of the OFET.

2. Experimental Procedures

The fabrication process of an Au/Parylene-C/Pentacene capacitor incorporating bulk Parylene C as an insulator is shown schematically in figure 1. P-type silicon (p-Si) substrates were ultrasonically cleaned in an ultrasonic cleaner (2200 Branson, Emerson, St. Louis, MO, USA) using, successively, acetone, DI water, isopropyl alcohol and DI water for 10 min each. Subsequently, the cleaned substrates were etched for 20 min using a 1:4 mixture of hydrofluoric acid and DI water.

A 150-nm-thick layer of silicon dioxide (SiO₂) was then deposited atop the p-Si substrate using a PECVD tool (P-5000, Applied Materials, Santa Clara, CA, USA). Thereafter, a 50-nm-thick adhesion layer of chromium (Cr) was deposited using a sputter tool (Desktop Pro®, Denton Vacuum, Moorestown, NJ, USA). Next, a 150-nm-thick gold (Au) layer was sputtered on top of the Cr layer using the same tool.

Pentacene was purified in gradient-temperature sublimation system (MK-5024-S, Lindberg Electric, Watertown, WI, USA) and then loaded in a tubular chamber. A thermal gradient was maintained along that chamber maintained at about 10⁻⁵ Torr pressure. The material was sublimated at 300 °C and re-condensed down the tube at 165 °C in order to drive out impurities. A 150-nm-thick layer of purified Pentacene was then deposited atop the Au layer via vacuum thermal evaporation (Amod, Angstrom Engineering, Kitchener, ON, Canada) at a rate of 0.2 nm s⁻¹. During that process, the Au/Cr/SiO₂/p-Si structure was fixed to a rotating chuck and maintained at 0 °C in a chamber with a base pressure of 10⁻⁷ Torr.

A 200-nm-thick insulating layer of Parylene C was deposited on top of the Pentacene layer using a physicochemical vapor deposition technique. An aluminum-foil boat loaded with 0.2 g of commercial Parylene-C dimer (980 130-C-01LBE, Specialty Coatings and Systems, Indianapolis, IN, USA) was placed inside the vaporizer of a Parylene Labcoater (PDS2010, Specialty Coatings and Systems, Indianapolis, IN, USA). Parylene-C dimer was first vaporized at 175 °C and then pyrolyzed into a reactive-monomer vapor at 690 °C. The reactive-monomer vapor was diffused onto the Pentacene/Au/Cr/SiO₂/p-Si structure attached to a rotating platform in a vacuum chamber maintained at 28 mTorr pressure.

Finally, a 150-nm-thick circular disk of Au was sputtered on top of the Parylene-C insulating layer using a shadow mask to form the gate of an Au/Parylene-C/Pentacene capacitor above the Au/Cr/SiO₂/p-Si bottom structure. The area of the circular disk was set as 7.1 × 10⁻² cm².

Capacitance-Voltage (C-V) measurements were carried out using a Precision LCR Meter (HP 4284, Hewlett-Packard, Palo Alto, CA, USA), while the parallel mode of ‘C-D’ option was selected. These measurements were made at 100 kHz frequency and room temperature with an applied gate voltage V₆ ∈ [−2.2] V and an oscillating voltage signal Vₛₖ = 24 mV.

Using a Semiconductor Parameter Analyzer (HP 4155 C, Hewlett-Packard, Palo Alto, CA, USA), we measured the time-dependent leakage current Iₜₚₑₓ as a function of time t while a stress voltage Vₜₚₑₓ ∈ {±10, ±15, ±20} V was being applied at room temperature. A fresh Au/Parylene-C/Pentacene/Au/Cr/SiO₂/p-Si structure was used for every value of Vₜₚₑₓ.
Table 1. Parylene C as a gate dielectric in different flexible multilayer structures.

| Structure | Active layer | Thickness | C-V Curve-shift | I-V Breakdown voltage | reference |
|-----------|--------------|-----------|-----------------|------------------------|-----------|
| MIM       | –            | 115 nm    | –               | 1.3 MV cm\(^{-1}\)     | [25]      |
| MIM       | –            | 210 nm    | –               | 2.2 MV cm\(^{-1}\)     | [9]       |
| OFET/MIM  | Pentacene    | 200 nm    | –               | 2 MV cm\(^{-1}\)       | [12]      |
| MIS       | p-Si         | 100 nm    | 0.1 V           | –                      | [13]      |
| MIS       | Pentacene    | 200 nm    | 3 V             | –                      | [24]      |
| OTFT      | Pentacene    | 170 nm    | –               | 2.7 MV cm\(^{-1}\)     | [15]      |
| OTFT      | Pentacene    | 500 nm    | 3.2 V           | –                      | [20]      |

Figure 1. Fabrication process of an Au/Parylene-C/Pentacene capacitor incorporating bulk Parylene C as an insulator.

3. Results

3.1. Capacitance-voltage characterization before application of constant-voltage stress

The measured C-V characteristics of an Au/Parylene-C/Pentacene capacitor at 100 kHz are shown in figure 2. As this sample was not subjected to CVS, it served as our control sample. Its C-V characteristics were measured in small voltage sweeps from ±2 V to ±2 V. The capacitance shows an apparent transition from accumulation to depletion. Also, a negligible hysteresis is observed, as the C-V curve-shift ∆V of 150 mV is very small [22, 23].

An MIS capacitor is generally modeled as two capacitors in series: the insulator capacitance \(C_i\) and the semiconductor-depletion-layer capacitance \(C_s\) [21, 22, 24]; hence, the capacitance

\[
C = \frac{C_i C_s}{C_i + C_s}. \tag{1}
\]

For \(V_g > 0\), the measured capacitance reaches a constant value equivalent to \(C\) given by equation (1). In contrast, for \(V_g < 0\), the capacitance saturates to a value close to

\[
C_i = \frac{\varepsilon_o \kappa A}{d}, \tag{2}
\]

where \(\varepsilon_o = 8.854 \times 10^{-14} \text{ F cm}^{-1}\) is the permittivity of vacuum. The Parylene-C layer is of thickness \(d = 200 \text{ nm}\) and the top-electrode area \(A = 7.1 \times 10^{-2} \text{ cm}^2\).

3.2. MIS capacitor characterization under constant-voltage stress

3.2.1. Capacitance-voltage characterization after application of constant-voltage stress

Figure 3 shows the C-V curves measured at 100 kHz in Au/Parylene-C/Pentacene capacitors after the room-temperature application of (a) \(V_{\text{stress}} \in \{-10, -15, -20\} \text{ V}\) and (b) \(V_{\text{stress}} \in \{10, 15, 20\} \text{ V}\) for duration \(t_{\text{stress}} = 10 \text{ s}\). After the 10-s application of \(V_{\text{stress}} \geq 0\), a C-V curve-shift \(\Delta V \geq 0\) is observed for all three values of \(|V_{\text{stress}}|\), which suggests a positive (resp. negative) charge buildup in the insulator of
the MIS capacitor during the application of positive (resp. negative) CVS. For the same $|V_{\text{stress}}|$ and $t_{\text{stress}}$, $|\Delta V|$ is higher for $V_{\text{stress}} > 0$ than for $V_{\text{stress}} < 0$. Parenthetically, the C-V curves in figure 3 were all taken for voltage sweeps between $-4$ V and $+4$ V, but are plotted in different voltage ranges to bring out the voltage shift after the application of CVS.

3.2.2. Time-dependent leakage current under constant-voltage stress
The time-dependent leakage current $I_{\text{stress}}$ was measured as a function of $t \in [1, 11]$ s during the application of CVS on MIS capacitors for $V_{\text{stress}} \in \{-10, -15, -20\}$ V. The data presented in figure 4 show that $I_{\text{stress}}$ is larger for larger $|V_{\text{stress}}|$. For the same $|V_{\text{stress}}|$, $I_{\text{stress}}$ is lower by three orders of magnitude for $V_{\text{stress}} > 0$ than for $V_{\text{stress}} < 0$. Irrespective of the polarity of $V_{\text{stress}}$, $I_{\text{stress}}$ decays as $t$ increases.

3.2.3. Time-dependent dielectric-breakdown characterization after application of constant-voltage stress
The TDDB characteristics of the Au/Parylene-C/Pentacene capacitors were obtained by recording the current-voltage (I-V) response before and after the 10-s application of $V_{\text{stress}} > 0$. Before CVS, the I-V curve in figure 5(a) shows a dielectric breakdown occurs at an electric field of 1.62 MV cm$^{-1}$. This value is comparable to the values of the breakdown electric field $E_{\text{bd}}$ in the range 1.9 to 2.2 MV cm$^{-1}$ reported for 200-nm-thick Parylene-C layers in MIM structures [9, 25], but for a much smaller gate electrode area of about $3 \times 10^{-4}$ cm$^2$.

In figure 5(b), measured values of the breakdown field $E_{\text{bd}}$ and the time-to-breakdown $t_{\text{bd}}$ are plotted as functions of $V_{\text{stress}} \in \{5, 10, 15, 20\}$ V. Time-to-breakdown $t_{\text{bd}}$ is the time it takes for the Parylene C to breakdown under the application of each $V_{\text{stress}}$.

As expected, both $E_{\text{bd}}$ and $t_{\text{bd}}$ decrease as $V_{\text{stress}} > 0$ increases. The value of $E_{\text{bd}}$ decreases from 1.62 MV cm$^{-1}$ for the control sample (i.e. $V_{\text{stress}} = 0$) to
1.04 MV cm⁻¹ for the sample stressed with \( V_{\text{stress}} = 20 \) V. Furthermore, \( \Delta t_{\text{bd}} \) decreases from 1005 s for the control sample to 104 s for the sample stressed with \( V_{\text{stress}} = 20 \) V.

Also, figure 4(b) shows the measured time-dependent leakage current \( I_{\text{stress}} \) in a Au/Parylene-C/Pentacene capacitor at room temperature as a function of time \( t \in [1,11] \) s during CVS application. However, in figure 5(a), leakage current was measured as a function of gate voltage \( V_g \) before CVS application. The leakage current in figure 4(b) is about 200 \( \mu A \) at \( V_{\text{stress}} = 20 \) V and \( t = 11 \) s, while the \( I_{\text{stress}} \) in figure 5(a) is about 266 \( \mu A \) at \( V_g = 19.75 \) V. The value of the leakage current in figure 4(b) is higher because the MIS capacitor is under CVS. Therefore, the leakage current is expected to decay as the stress time increases until a steady-state value that equals to the leakage current in figure 5(a) [5].

4. Discussion

The C-V characteristics of organic-based MIS capacitors are limited by contact injection [21, 26-29]. The C-V curve obtained in figure 2 can be explained in terms of charge accumulation arising from injection and contained within the semiconductor layer.

For \( V_g > 0 \), a thin accumulated layer of injected holes occurs at the Au/Pentacene interface, while the Parylene-C/Pentacene interface is depleted and devoid of any significant free charge carriers. As a result, a depletion layer is created inside the Pentacene. Hence, the capacitance is given by \( C \) in equation (1). For \( V_g < 0 \), an accumulation of holes occurs near the interface of Pentacene/Parylene-C. As \( V_g \) further increases to more negative values, \( C \) increases and \( C \) approaches \( C_i \) given by equation (2).

The C-V curve shifts observed in figure 3 are attributed to charge buildup \( \Delta Q_i \) in Parylene C [30, 31]. Charges of three different provenances are associated with \( \Delta Q_i \) [30, 31]; i.e.

\[
\Delta Q_i = Q_{in} + Q_b + Q_t. \tag{3}
\]

Here, \( Q_{in} \) is the charge density of mobile positive charges located in the bulk of the insulator and arising from ionic impurities such as Na⁺. The effect of these charges can be seen as a hysteresis in the C-V curve when sweeping \( V_g \) in a negative-positive-negative loop. Also, \( Q_b \) is the charge density of charges trapped in the bulk insulator. It can be either negative or positive, depending on whether holes or electrons are trapped. \( Q_t \) is the charge density of charges trapped in the semiconductor/insulator interface. It can also be either negative or positive. Because these charges are trapped at the interface, \( Q_t \) has the largest effect on \( \Delta V \).

As can be deduced from figure 2, \( Q_{in} \) is negligibly small because a very small hysteresis (\( \Delta V = 150 \) mV) is detected as the gate voltage is swept from \(-2 \) V to \(+2 \) V to \(-2 \) V. Hence, \( Q_{in} \) plays no role in the charge buildup observed in Parylene C after the application of CVS so that

\[
\Delta Q_t = Q_b + Q_t. \tag{4}
\]

Let us now attempt a quantitative analysis of \( \Delta Q_t \) and its dependence on \( V_{\text{stress}} \) and \( I_{\text{stress}} \). Accordingly [32],

\[
\Delta Q_t = \frac{-\Delta V C_i}{A}. \tag{5}
\]

Table 2 provides the values of \( \Delta Q_i \) for \( V_{\text{stress}} \in \{ \pm 10, \pm 15, \pm 20 \} \) V. Clearly, the charge buildup is positive for \( V_{\text{stress}} < 0 \) but negative for \( V_{\text{stress}} > 0 \). Furthermore, for fixed \( |V_{\text{stress}}| \), the charge buildup is more than twice in magnitude for \( V_{\text{stress}} > 0 \) than for \( V_{\text{stress}} < 0 \).

During the time that \( V_{\text{stress}} < 0 \), electrons are injected from the gate and holes are injected from the layer of accumulated holes near the Parylene-C/Pentacene interface. Electrons and holes transiting the Parylene-C layer can be trapped at defect sites and give rise to charge buildup. It is apparent from table 2 that hole trapping dominates and the net charge buildup is positive for \( V_{\text{stress}} < 0 \).

In contrast and during the time that \( V_{\text{stress}} > 0 \), holes are only injected from the gate into Parylene-C. The resulting hole-leakage current is observed to be much smaller than \( I_{\text{stress}} \) shown in figure 4(a). This is because a significant portion of the applied \( V_{\text{stress}} \) is
Table 2. C–V curve-shift $\Delta V$ of and the charge buildup $\Delta Q_t$ in a Au/Parylene-C/Pentacene MIS capacitor subjected to $V_{\text{stress}} \in \{ \pm 10, \pm 15, \pm 20 \} \text{V}$ for $t_{\text{stress}} = 10 \text{s}$.

| $V_{\text{stress}}(\text{V})$ | $\Delta V(\text{V})$ | $\Delta Q_t(\text{C cm}^{-2})$ |
|-----------------------------|---------------------|-------------------------------|
| $-10$                       | $-0.35$             | $+4.10 \times 10^{-9}$         |
| $-15$                       | $-0.56$             | $+6.50 \times 10^{-9}$         |
| $-20$                       | $-0.89$             | $+1.04 \times 10^{-8}$         |
| $+10$                       | $+0.76$             | $-8.90 \times 10^{-9}$         |
| $+15$                       | $+1.37$             | $-1.60 \times 10^{-8}$         |
| $+20$                       | $+2.10$             | $-2.45 \times 10^{-8}$         |

dropped across the depleted (i.e. devoid of charge carriers) layer near the Pentacene/Parylene C interface; much less hole transport takes place across Pentacene for $V_{\text{stress}} > 0$. However, the charge-buildup sign is negative, which may indicate that the observed charge buildup is not entirely due to the trapping of charge carriers (electrons and holes) but could also be caused by defect generation. Presumably, these generated defects are electrons traps that are populated during the application of $V_{\text{stress}}$.

The I–V curve in figure 5(a) shows a dielectric breakdown occurs at an electric field of $1.62 \text{ MV cm}^{-1}$. This breakdown may indicate the formation of a defect-related conduction path [33, 34]. In other words, a higher applied voltage could induce defects that eventually form different conducting paths from the gate to the semiconductor in the Au/Parylene-C/Pentacene structure.

As shown in figure 5(b), the decrease in $E_{\text{bd}}$ suggests that more/longer conductive paths are formed with increasing $V_{\text{stress}} > 0$. Conductive paths result from defect-generation processes and, hence, more defects are presumably generated as $V_{\text{stress}}$ further increases to higher values. This deduction is in agreement with earlier inference from table 2 that defect generation dominates over charge trapping during $V_{\text{stress}} > 0$.

5. Concluding Remarks

A systematic analysis of the reliability of Au/Parylene-C/Pentacene MIS capacitors under constant-voltage stress was performed, with focus on the effects of CVS on the stability of Pentacene as a gate dielectric. 200-nm-thick Parylene-C thin films were utilized as gate-dielectric layers of Au/Parylene-C/Pentacene MIS capacitors. Measurements and analysis of the C–V curve-shift, the time-dependent leakage current and the time-dependent dielectric breakdown were performed before and after application of CVS. Positive and negative stress voltages of the same magnitude were applied for 10-s duration.

Therefore, our main conclusions are as follows:

- The C–V characteristic can be explained in term of accumulation charges within the semiconductor layer.
- This accumulation charge is due to contact injection.
- Inside the insulating layer, the charge buildup resulting from the accumulation of trapped charges affects the stability of the MIS capacitor by shifting its C–V curve.
- The shift of the C–V curve is attributed to the trapping and recombination of electrons and holes inside Pentacene and its interface with Pentacene.
- The dielectric-breakdown mechanism is defect dominated.

Overall, the buildup of trapped charges in the Parylene-C layer and near the Parylene-C/Pentacene interface plays a major role in the degradation of Au/Parylene-C/Pentacene capacitors. Our analysis in this paper provides a first-level understanding of the charge buildup in Au/Parylene-C/Pentacene capacitors and, perhaps, will serve as the basis of future studies on the defect-generation process and the trapping of charge carriers within the insulator layer in OFETs.

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