GaAs- $A_3B_5$ heterostructures for high-speed power diodes manufacturing

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Abstract. Physical basis of using the controlled defect formation in InGaAs heteroepitaxial layers to vary the carrier lifetime is considered. It is shown that the lifetime of nonequilibrium carriers in the base layers of a diode can be controllably varied from several to hundreds of nanoseconds. The results obtained in a study of (i) structural defects and their rearrangement related to the lattice mismatch between the heteroepitaxial InGaAs layer and the GaAs substrate and (ii) influence exerted by these defects on the carrier lifetime and on the voltage blocked by diode structures are reported. Dynamic switching characteristics of high-speed power heteroepitaxial diodes at different temperatures are presented.

1. Introduction

One of the main tendencies in the development of modern power electronics and pulse technology consists in raising the conversion efficiency of electrical signals and reducing the mass and size of technical devices used in electricity converters. Further advances in this field primarily require that high-frequency fast power semiconductor devices with improved set of static and dynamic characteristics should be used in converter devices. As applied to the class of bipolar diodes, this requires that devices with short switching times should be developed, with the minimum possible forward voltage drops in the conducting state, low leakage current under reverse biases, and extremely high working temperatures of the diode crystal preserved. It is nearly impossible to simultaneously satisfy all these requirements because of the opposite correlation of the static and dynamic characteristics of a diode on parameters of its semiconductor structure. Use of GaAs-$A_3B_5$ heterostructures instead of the conventional Si-based devices opens up new opportunities for development of fast power diodes and improvement of the whole set of their frequency and static characteristics [1, 2].

One of the most important dynamic characteristics of high-power pulse bipolar diodes, which limit frequency parameters, is the reverse recovery time $t_{rr}$ (the time in which the blocking properties of a p-n junction are restored after the diode is switched from the conducting to blocking state). When a diode is switched off, two phases in which the reverse resistance is restored are distinguished: the stage of a high reverse conductivity in which the p-n junction remains forward-biased despite the change of the polarity of the applied external voltage and the stage of recovery of the high reverse
resistance in which a space-charge layer is formed near the p-n junction and, while extending, this layer blocks the voltage applied to the diode. The switch-off parameters of a diode can be controlled by varying the conditions of minority carrier accumulation and resorption and, in the first place, by changing the values and distribution profile of minority carrier lifetimes in the lightly doped base layers of the high voltage diode. In the present work, the main results on investigation and elaboration of methods for decreasing the values of charge carrier lifetime by means of application of a technique for generation of additional intrinsic structural defects arising in crystals during epitaxial growth of mismatched heterostructures are presented.

2. Sample fabrication
We fabricated the structures of high-voltage gradual p-i-n junctions by liquid-phase epitaxy (LPE) technique the fundamentals of which had been developed at the Ioffe Physical-Technical Institute [3]. This technique is simple in implementation, economically efficient, and, in our opinion, is the only presently possible method for obtaining high-voltage GaAs p-n junctions capable of blocking voltages on the order of 1000 V and more [4]. Epitaxial layers of GaAs and In$_x$Ga$_{1-x}$As solid solutions with InAs content $x$ of up to 6% were grown on p$^+$-GaAs (111) and (100) substrates doped with zinc to $(2-10) \cdot 10^{18} \text{ cm}^{-3}$. The growth equipment used in the study made it possible to growth epitaxial layers on 2- and 3-inch GaAs substrates. The epitaxial growth of lightly doped gradual p-n junction layers was carried out from a confined Ga-As or In-Ga-As melt in the hydrogen atmosphere in quartz boat from 900ºC to room temperature. Heavily doped (with Te or Sn) n$^+$-GaAs emitter layers of the diode structures were grown in piston graphite cassette.

![Typical free carrier distribution across the thickness of GaAs or InGaAs high voltage p$^0$-i$^0$n$^0$ layers grown on p$^+$-GaAs substrates with a later-grown n$^+$-GaAs emitter.](image)

The content of electrically active defects in epitaxial layers grown by this method is controlled by the content of residual (background) impurities in the melt and growth system, temperature and duration of a preliminary annealing of the melt, and flow rate and humidity of hydrogen, as well as by the growth velocity of the epitaxial film under programmed cooling of the system. In this mode of LPE growth of p-i-n structures, it is possible to obtain thick lightly doped i-type layers of GaAs or InGaAs with a free carrier concentration of $\sim 10^{13} \text{ cm}^{-3}$, which makes it possible to reach $U_b$ of up to 2000 V. Typical free carrier distribution across the thickness of diode structures with GaAs or InGaAs base layers are shown in figure 1.

The relative amounts of the components of the In-Ga-As liquid phase used to obtain In$_x$Ga$_{1-x}$As layers of required composition was found by calculations in terms of the quasi-regular approximation model, with consideration for the elastic stresses appearing because of the lattice mismatch between the layer and substrate for elastically strained layers [1,5,6] and with elastic stresses disregarded for layers in which these stresses are partly relaxed (under relatively large lattice mismatch in heterostructure). It has been found previously [7] that, when layers for which the combination of the
lattice mismatch and thicknesses is such that elastic stresses are partly relaxed and mismatch dislocations are thereby formed (see below), the composition of the solid solution of a layer tends to be the closest to that in equilibrium. This was confirmed by X-ray microanalysis on a Camebax installation for In\textsubscript{x}Ga\textsubscript{1-x}As layers in which elastic stresses are partly relaxed via formation of a network of linear mismatch dislocations revealed by X-ray topography [7].

Diode chip samples had a form of «mesa» with round base which was obtained by chemical etching of active layers up to substrate around contact pads. The double-layer lithography with lift-off photoresists (LOR) was used to form thick (up to 2-3 μm) contact pads during single vacuum evaporation process [8, 9]. The Cr-Ni-Au or Cr-Ni-Au contact systems was used to make ohmic contacts to p⁺-GaAs substrate, and AuGe-Ni-Au, AuGe-Ni-Ag, or Ti-Ge-Pt-Au [10] – to n⁺-GaAs emitter layers.

3. Study of the crystalline structure of In\textsubscript{x}Ga\textsubscript{1-x}As heteroepitaxial layers. Relationship between the layer crystalline structure and the device characteristics of diodes

The real crystalline structure of lightly doped layers in In\textsubscript{x}Ga\textsubscript{1-x}As-GaAs heterostructures was studied with Cu K\textsubscript{α} radiation and 422, 533, and 331 asymmetric reflections in the back reflection X-ray diffraction topography at different information layer depths. This procedure for studying the crystalline structure of the layers was described in detail in [11].

Figure 2. Topograms of the homostructure GaAs (a) and heterostructures In\textsubscript{x}Ga\textsubscript{1-x}As-GaAs (b-d) with equal thicknesses (50-65μm) and different x of the base layers: x = 0 (a); x ~ 2% (b); x ~ 3.5% (c); x ~ 5% (d). Bragg method, CuK\textsubscript{α}-radiation; reflection: 422 (a); 422 (b); 511 (c); 331 (d).

Figure 2 shows how the crystalline structure of a heteroepitaxial layer changes with increasing lattice mismatch (increasing x) at the same base layer thicknesses. After the critical elastic strain relaxation thicknesses of In\textsubscript{x}Ga\textsubscript{1-x}As layers were reached, there appeared networks of mismatch dislocations (figure 2, b), with the type of these networks determined by the solid solution concentration x, layer thicknesses, and crystallographic orientation of wafers. In [7], the range of compositions x at which a network of linear mismatch dislocations is characteristically formed in In\textsubscript{x}Ga\textsubscript{1-x}As (111) layers with thicknesses of 50 to 65 μm was experimentally found to be x = 1.5-3.3 mol %. At these thicknesses and compositions of the In\textsubscript{x}Ga\textsubscript{1-x}As solid solutions, a quasi-uniform network of linear mismatch dislocations is formed in the epitaxial layers (figure 2, b).

With x increasing at the same thickness of epitaxial layers, the average density of mismatch dislocations in the layers became higher and the shape of cells of the dislocation network for In\textsubscript{x}Ga\textsubscript{1-x}As (111) layers changed from triangular to rounded (figure 2, c), being transformed at x ≈ 4 mol % to a cellular dislocation structure with dense cell boundaries (figure 2, d). In this case, the dislocation density at dislocation cell boundaries increased to about 10\textsuperscript{6} cm\textsuperscript{-2} and more.

In a study of samples with high isovalent doping levels (x > 4 mol %), optical methods also revealed characteristic growth figures on the surface of the epitaxial layers. As a rule, these figures combine several dislocation cells at once. These growth figures are also well identified in X-ray topographs in reflections with a small X-ray beam incidence angle (331 in comparison with 422 or 533). Their presence is indicative of the high content of structural defects in the In\textsubscript{x}Ga\textsubscript{1-x}As epitaxial layer.
The process in which the dislocation of heteroepitaxial layers changes with increasing $x$ is accompanied by a substantial decrease in the lifetime of nonequilibrium carriers near the p-n junction from hundreds to several nanoseconds (figure 3) and also by a gradual decrease in voltages blocked by diodes (figure 4), and at $x > 3.5$ mol $\%$, by a sharp fall of these voltages. We attribute the sharp decrease in $U_b$ for diode heterostructures with higher content of InAs (figure 4, $x > 3.5$ mol $\%$) to a fundamental change of the dislocation structure of In$_x$Ga$_{1-x}$As layers, i.e., to a major transition from a uniform network of rectilinear dislocations with symmetry in the (111) plane to a "cellular" dislocation structure with very high dislocation density at boundaries of cellular networks and formation of growth figures on the surface of an epitaxial layer. This conclusion about the effect of dense dislocation walls on the decrease in the blocking capacity of p-n junctions is well correlated, both qualitatively and quantitatively, with the results of a study of dislocations in silicon epitaxial structures of power devices [12].

The forward voltage drops $U_f$ for InGaAs-GaAs diodes with nanosecond times $\tau_{\text{eff}}$ and $U_b < 600$ V had values of $U_f$ not exceeding 2 V at a working current density $j_f = 150$ A/cm$^2$. At increased current densities, the forward voltage drop $U_f$ on diodes of this kind has quite acceptable values $U_f < 3.0$ V at $j_f = 1000$ A/cm$^2$. It should be noted that this combination of small values of $U_f$ and a nanosecond switching-off time of a diode cannot be reached in silicon-based devices. The electrical capacitance $C$ of GaAs diodes weakly depends on voltage and has a value on the order of $C_0 \approx (1-2) \times 10^3$ pF/cm$^2$ under zero bias and $C_{300V} \approx (2-4) \times 10^2$ pF/cm$^2$ under a reverse bias $U_r = 300$ V.

![Figure 3](image1.png)
![Figure 4](image2.png)

**Figure 3.** Effective nonequilibrium charge carrier lifetime $\tau_{\text{eff}}$ in In$_x$Ga$_{1-x}$As layers grown on GaAs substrates depending on $x$.

**Figure 4.** Maximum blocking voltages $U_b$ of In$_x$Ga$_{1-x}$As-GaAs heterostructures of thickness up to 65$\mu$m depending on $x$.

![Figure 5](image3.png)

**Figure 5.** Waveforms of 4A current turn-off switching for InGaAs-GaAs heterojunction diode (blue curve 1) and GaAs homojunction diode (green curve 2). Vertical scanning – 1A/div and horizontal one – 10 ns/div; $T = 25$ °C.
Figure 5 shows for comparison oscillograms of the switching-off dynamics of diodes with different base layers: heteroepitaxial InGaAs base layer (curve 1 in figure 5; $t_{rr} \sim 16$ ns) and homoepitaxial GaAs base layers (curve 2 in figure 5; $t_{rr} \sim 60$ ns). Comparative tests of device structures of this kind demonstrated that the heterostructure growth technology with controlled defect formation makes it possible to fabricate diodes having the lowest amount of accumulated charge, shortest switching-off time, and minimum switch-on and switch-off losses among Si and GaAs bipolar diodes.

![Figure 5](image)

**Figure 6.** Waveforms of 1A current turn-off switching for InGaAs-GaAs heterojunction diode under different temperature measurements: under 25 °C (a) and 175 °C (b). Vertical scanning – 0.25A/div and horizontal one – 5 ns/div.

As regards the whole set of their dynamic characteristics, InGaAs-GaAs diodes are nearly not inferior to SiC Schottky diodes, especially at high current densities [7]. InGaAs-GaAs diodes are actually capable of operating at frequencies on the order of several megahertz at crystal temperatures $T$ of up to 250°C (provided that the diode chip surface is passivated and protected by, e.g., insulators; without protection of the lateral surface of a chip, power GaAs diodes are properly functioning up to 190-200°C). As the temperature of the crystal of heteroepitaxial diodes increases from room temperature to 175°C, the time and charge of reverse recovery of InGaAs-GaAs diodes grow by a factor of ~1.5 (see figure 6), whereas when Si bipolar diodes are heated to 175°C, the recovery times commonly become more than three times longer.

4. **Summary**
The principal result of the study is that the carrier lifetime in base layers of power InGaAs-GaAs diodes can be controlled in the range from several to hundreds of nanoseconds by using the method of intrinsic defect formation in growth of mismatched heteroepitaxial base layers. This growth technique can be successfully used in fabrication of high-voltage high-temperature power diodes with working voltages of 300-800 V and reverse recovery times on the order of 10 ns and shorter at an acceptable loss in the conducting state.

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5. **References**

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