Research on thick copper CMP based on multilayer wiring of radio frequency microsystem

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Abstract. To cope with the special requirements of RF microsystem for ultra-thick wiring layer and large-size line width of microwave signal, based on the damascene process in CMOS manufacturing, the dishing phenomenon and causes of thick copper CMP dishing were discussed. Through using the radio frequency module wiring layout, dishing generated by different line width in copper CMP was studied and compared. The influence of the thickness of electroplated copper on dishing is discussed, and a method to reduce dishing is proposed. In addition, in order to reduce the dishing generated by the Ta-CMP process, the removal rates of Ta, Cu and SiO₂ were tested, and a polishing selection ratio close to 1:1:1 were obtained. Dishing was reduced to 1000 Å. Finally, a three-layer thick copper wiring consisting of a thick dielectric film deposition and etching, thick copper plating and CMP was successfully developed with a total thickness of 10μm.

1. Introduction
The chemical mechanical polishing (CMP) process is one of the most effective global planarization technique [1-2], and CMP is one of the key technology for IC manufacturing. The CMP process also plays a vital role in RF microsystem, 3D stacking, wafer level packaging, TSV interconnect, integrated passive device, multilayer interconnect, and sacrificial layer technology.

Copper CMP is one of the key processes in the damascene process [3-5], because the surface morphology after dielectric deposition, etching and metallization is very poor. The large height fluctuation not only affects the second dielectric deposition, but also seriously affects the integrity of the graphic after lithography. Therefore, global planarization is achieved by copper CMP, which places the metal at a relative level to the surface of the dielectric. During the copper CMP process, both dishing and erosion occurs, which can seriously affect the dielectric deposition and metallization. The copper dishing is influenced by many factors, such as the thickness of the metal layer, the duty cycle and the line width. Many researches on reducing dishing had been proposed [6-7]. But in RF microsystem applications, it is not only necessary to meet the requirements of ultra-thick metal layers for microwave signals, but also to meet the requirements of line width for different signal lines. Therefore, thick metal multilayer wiring based on RF microsystems puts higher requirements on copper CMP.

This study is based on the damascene process in CMOS manufacturing, focusing on the process of thick copper CMP dishing in thick copper wiring process, and discuss the main reasons for dishing. In addition, for the different requirements of the thickness and width of the microwave signal line in the
RF micro-system, the copper CMP dishing of different line width pattern and plating thickness were discussed. Then a practical method to reduce dishing was proposed. Finally, a three-layer thick copper wiring consisting of a thick dielectric film deposition and etching, thick copper plating and CMP was developed.

2. Theories and Methods

2.1. Damascene process
The dual damascene process is the basis of the three-dimensional integrated wiring process. While forming the planar interconnect, the functions of connecting device or interconnect under the dielectric layer to the surface of the dielectric layer can be realized. Therefore, the copper interconnect is currently using dual damascene process, as shown in Figure 1. A thin layer of silicon carbide is deposited by PECVD as a diffusion barrier and an etch stop layer. Then a certain thickness of silicon dioxide is deposited on the silicon carbide. Etching the vertical micro-via which will be used to connect the multilayer metal interconnection after photolithography, the etching depth of micro-via cannot bigger than the thickness of silicon dioxide layer. Then the trench of planar interconnect is formed by photolithography. The trench of the planar interconnect and the micro-via is realized by etching simultaneously. All the dielectric layers at the micro via position are removed. The diffusion barrier layer, the adhesion layer and the copper seed layer are sputtered by PVD, and then the electroplated copper layer. Finally the copper layer on the oxide surface is removed by CMP, which can realize a planar interconnection of the lateral wiring connecting and a vertical interconnection of the inter-layer metal.

2.2. CMP process
The basic principle schematic of CMP is shown in Figure 2. Under the high-speed rotation of the polishing head and the polishing pad, the polishing liquid and the material to be polished undergo a series of complicated chemical reactions to produce an easily removable substance, which is removed by the abrasive in slurry. Then the newly exposed surface of the polishing material continues to react and be removed. Finally the globe planarization is achieved. Currently, CMP is widely used for planarization of various materials, including polymers, metals, dielectrics, and ceramics, for its excellent performance. The application of CMP can be divided into metal CMP and non-metal CMP, the most representative are silicon dioxide CMP and copper CMP, which represent almost all CMP process principles and methods.
The CMP process involves very complex chemical and mechanical effects. The mathematical theory model is continuously improved on the basis of the Preston model and has not yet been fully understood. The copper CMP process is divided into three steps: 1) polishing copper with high speed for eliminating the steps rapidly; 2) polishing copper with low speed and low pressure until copper is completely removed, for reduction the dishing; 3) barrier Ta is completely removed through specific slurry and process parameters for reduce Dishing. Due to the different physical and chemical properties of different materials, the polishing rates of different materials are also inconsistent. The copper removal rate is too fast, but the barrier layer material and the dielectric layer material are removed very slowly, which is likely to cause local over-polishing. Over polishing will bring in serious dishing and erosion problems, as shown in Figure 3. In addition, the generation of the dishing is also related many factors, such as the deformation of the polishing pad, the type of the polishing liquid, the over-polishing time, the polishing pressure, the relative velocity between the polishing pad and the wafer, the distribution of the polishing particles on the polishing pad, the oxidation in the polishing liquid, the concentration of the material, the pattern density, the copper line width and the plating process of the copper. In this study, we used fixed polishing liquid, polishing pad and disk. Therefore, the method of reducing the dishing is started from the selection ratio of CMP of different materials, the line width of the pattern, and the thickness of the pattern.

![Figure 2. Fundamental schematic of CMP.](image1)

![Figure 3. Dishing and Erosion.](image2)

3. Experiment and Results

3.1. Experiment condition

All of the CMP experiments were complemented by AMAT Mirra Mesa. The equipment has three polishing platens. Platen1 and platen2 are for Cu polishing, platen3 is for barrier metal and oxide polishing. In order to achieve controllable non-uniformity, 5 zone polishing head is used. And we use IC1000 pad, 3M 165A disk, and commercialization slurry. We use the optical microscope and scanning electronic microscope (SEM) to characterize the copper surface topography after CMP. Platen1 and Platen2 used the same commercial polishing slurry, and the proportion of the slurry was the same. So, the polishing rate and polishing non-uniformity of copper CMP were adjusted by the down force, the platen rotation rate, the head rotation rate and the flow rate.

Polishing pressure is a very important parameter in the chemical mechanical polishing process, which directly determines the polishing rate and polishing effect. Down force mainly determines the polishing rate and the non-uniformity of CMP. The removal rate varies with down force under different slurry flow rate as shown in Figure 4. When rotation rate of the platen and head is fixed, experiments of copper CMP have shown that the removal rate increases as increasing the down force, but an increase in the removal rate causes scratches and bigger dishing. The removal rate increases as increasing the flow rate of the slurry, but the removal rate does not increase if the flow rate increases to a certain extent, because the chemical reaction is already saturated. It can be seen from the figure
that the removal rate can be maximized and the polishing effect is best when the flow rate is 200 ml/min.

Figure 4. Removal Rate versus down force.

3.2. The effect of line width on dishing

In order to meet the special requirements of the RF microsystem for the high power and microwave performance of the interconnect, the three-layer wiring has a line width ranging from 2μm to 600μm and a line spacing ranging from 2μm to 500μm, which includes strip, circle and square structure, as shown in Figure 5. Therefore, further process optimization is performed for the influence of the line width on dishing.

Copper CMP experiments with a large number of different line widths show that the generation of dishing is the result of the combination of down force and line width, as shown in Figure 6. Dishing increases as increasing of the line width. When the line width increases to more than 300um, the effect of the increase in line width on dishing is relatively reduced. In addition, dishing increases significantly as increasing of down force. We selected several down force to CMP. When the down force is less than 3Psi, the dishing is greatly reduced. Because the removal rate is very low when the down force is too small, the dishing decreasing by reduction the down force is not obvious. Therefore, if the line width cannot be changed, lowering down force is the best way to reduce dishing. We can use low down force on platen2 for much more less dishing.

Figure 5. Pattern of three-layer inter-connection.

Figure 6. Dishing versus Line Width.
3.3. The effect of plating thickness on dishing

In the RF microsystem, in order to reduce the loss of microwave signal transmission, the thickness of the metal layer is generally greater than 2μm, or even more than 10μm. Thick metal means that there are deeper steps after plating, which places higher demands on copper CMP, as shown in step D in Figure 7. As the process progresses during the copper CMP process, the step of the plating trench will gradually become smaller until the step is removed completely. The thickness of the electroplated Cu affects the effect of the grooving, which in turn affects the CMP process. For a 2μm wiring thickness, the effect of plating thickness on dishing is shown in Figure 8. The patterns with line widths of 2μm, 10μm, 50μm, and 100μm were selected. It can be seen that when the thickness of the electroplated Cu is 2 to 3 times the thickness of the copper wiring, the reduction of dishing is the largest and the value of dishing is the smallest.

![Figure 7. Step of Plating.](image)

![Figure 8. Dishing versus plating thickness.](image)

3.4. Removal rate of Ta-CMP

In order to minimize the influence of dishing increase due to different removal rates of Cu, Ta and SiO2, the removal rate of three materials was studied on Platen3. After optimization of the process parameters, the polishing selection ratio of the three materials is close to 1. As shown in Figure 9, the removal rates of Cu, Ta, and SiO2 on the 8-inch silicon wafer are all close to 500 Å/min, and the Ta removal rate has a good non-uniformity, NU < 2%. Through the optimization of process parameters, dishing can be reduced to less than 1000Å.

![Figure 9. Removal Rate on platen 3.](image)

3.5. Three-layer wiring
Through the optimization of the above CMP process parameters, the three-layer interconnect wiring process is completed based on the module layout of the T/R module. Figure 10 is the profile of the three-layer interconnection. The process includes three layers of wiring of Metal1, Via2, Metal2, Via3, and Metal3. It was completed by 3 times of dielectric deposition, metallization, and CMP, and the final thickness of the wiring was 10μm. The thickness of Metal1, Via2, and Metal2 is 2μm, the thickness of Metal3 is 3μm, and the thickness of Via3 is 1μm. The SEM image of the three-layer wiring is shown in Figure 11. Because of the variation of deposition of and measurement, the thickness is very close to the design value. The thickness of Metal1 is 1.99μm, the thickness of Via2 is 2.00μm, the thickness of Metal2 and Via3 is 3.00μm, and the thickness of Metal3 is 3.00μm.

**Figure 10.** Profile of the three-layer interconnection.

**Figure 11.** SEM image of the three-layer interconnection.

Through the further optimized CMP process parameters and plating conditions, the three-layer wiring is completed. All the lines are complete in structure, the lines are clear, the surface of the Cu line has no defects, and the electrical performance can meet design requirements. After measurement, the Cu line dishing is less than 1000 Å. The SEM image of the cross section is shown in Figure 12. It can be seen that the three-layer structure is complete and the micro-via has no fracture.

**Figure 12.** SEM image of three-layer interconnection profile.

4. Conclusion
In this paper, we analyze the dishing problems in thick copper CMP process. By optimizing the process parameters, setting the low down force, selecting 2 to 3 times the thickness of the electroplated copper, the dishing effect of the large-size line width and the thick copper CMP can be greatly reduced. And through the optimized copper CMP process, a three-layer wiring structure based on the RF module is realized.

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