Gate capacitance of back-gated nanowire field-effect transistors

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Gate capacitances of back-gated nanowire field-effect transistors (NW-FETs) are calculated by means of finite element methods and the results are compared with analytical results of the “metallic cylinder on an infinite metal plate model”. Completely embedded and non-embedded NW-FETs are considered. It is shown that the use of the analytical expressions also for non-embedded NW-FETs gives carrier mobilities that are nearly two times too small. Furthermore, the electric field amplification of non-embedded NW-FETs and the influence of the cross-section shape of the nanowires are discussed.

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Semiconducting nanowires (NWs) with diameters from several nanometers up to around 100nm are currently being investigated for their potential towards realization of electronic devices with significantly enhanced performance like enhanced carrier mobility. While much effort is spent on growth and structural characterization, obviously reliable and accurate electrical characterization is equally important. For electronic applications the charge carrier mobility \( \mu \) is a crucial property. The mobility can be determined from the linear part of the transconductance \( g = dI_{sd}/dU_{gs} \) measured in a field-effect transistor device \( \mu = gL^2/(CU_{sd}) \), with \( L \) being the channel length, \( C \) the gate capacitance, \( U_{sd} \) the source-drain, and \( U_{gs} \) the gate-source voltage.

In the case of NWs usually back-gated nanowire field-effect transistors (NW-FETs) are fabricated: \( 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 \) a highly doped Si-substrate and thermally grown SiO\(_2\) function as the back-gate and the gate dielectric, respectively. Then NWs are transferred on the SiO\(_2\) followed by the deposition of the source and drain electrodes. Such a transistor has the advantage that it can be processed relatively easily. However, in practical devices other geometries like the wrap-around NW-FET will be preferred. A cross-sectional view along the NW axis with equipotential lines due to the gate voltage is shown in Fig. 1(a).

![Cross section geometry of back-gated NW-FETs](image)

**FIG. 1:** Cross section geometry of back-gated NW-FETs of non-embedded NWs (a) and embedded NWs (b) with \( t/R = 6 \). The lines are on equally separated constant potentials obtained by FEM calculations.

To calculate the gate capacitance, usually the “metallic cylinder on an infinite metal plate model” \( 1 \) is used. \( 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 \) The cross section geometry and the equipotential lines of this model are depicted in Fig. 1(b). To use this model, the charge density in the nanowire is assumed to be so high that the semiconducting NW can be treated as metallic. It was shown \( 16 \) that this approximation yields reasonable results for GaN NWs with doping concentrations above \( 10^{17} \text{cm}^{-3} \). Additionally, it is assumed that the NW is much longer than the dielectric layer thickness so that the fringing capacitance at the source and drain contact can be neglected and that there are no movable charges or defects in the dielectric layer or at the NW surface. The model further assumes that the NWs are completely embedded in the dielectric and posses a circular cross section. The latter assumptions are reexamined in detail in this paper.

The model yields an analytical equation for the gate capacitance per unit length

\[
\frac{C}{L} = \frac{2\pi \epsilon_0 \epsilon_r}{\cosh^{-1}\left(\frac{1}{R} \right)}. \tag{1}
\]

with \( \epsilon_r \) being the dielectric constant of the embedding dielectric, \( t \) the distance between the metal plate and the center of the cylinder, and \( R \) the radius of the cylinder [see Fig. 1(b)]. For \( x = t/R \gg 1 \), the approximation \( \cosh^{-1}(x) = \ln(x + \sqrt{x^2 - 1}) \approx \ln(2x) \) can be used. Equation (1) then reads

\[
\frac{C}{L} = \frac{2\pi \epsilon_0 \epsilon_r}{\ln(2R)}. \tag{2}
\]

In Fig. 2 the results of Eqs. (1) and (2) are shown. Here SiO\(_2\) is considered as the gate dielectric with \( \epsilon_r = 3.9 \). The relative error by using Eq. (2) is less than 1% for \( t/R \gg 6 \). Because most NW-FETs have \( t/R \) ratios above six, this approximation yields usually good accuracy. Equation (1) and Eq. (2) are used to estimate the gate capacitance also in the case of back-gated NW-FETs in which the NW is lying on top of the gate dielectric [Fig. 1(a)]. Because of the missing dielectric material around the NW, it is expected that both analytical equations give only an upper limit for the gate capacitance. To examine this in detail, I have carried out finite element method (FEM) studies of the gate capacitance.

The FEM results are shown in Fig. 2. For the embedded NWs the numerical results agree very well with the
analytical ones using Eq. (1). For small \( t/R \) values the deviation due to the approximation in (2) can be seen. For the non-embedded NWs, the capacitances are nearly two times lower than the analytical results for embedded NWs. Thus if Eqs. (1) or (2) are used to determine the gate capacitance also in the case of non-embedded NW-FETs, the carrier mobilities are underestimated by a factor of almost two. This discrepancy is very important when the carrier mobilities in NWs are compared with bulk values. Furthermore, this implies that the gate coupling of non-embedded NW-FETs can be nearly doubled by packing the NWs completely in SiO\(_2\). This has also a positive effect on the electric field distribution as will be discussed later.

In literature the weaker gate coupling in case of non-embedded NW-FETs is taken into account by an empirical effective dielectric constant for SiO\(_2\) of \( \epsilon_{r,\text{eff}} = 2.5 \) \( [13, 14] \) or \( \epsilon_{r,\text{eff}} = 1.95 \) \( [15, 16] \) in combination with Eq. (2). In Fig. 2 a fit of the numerical data using an effective dielectric constant is shown. The fit is carried out for \( 6 < t/R < 100 \) and results in \( \epsilon_{r,\text{eff}} = 2.20 \) with a relative deviation of less than 3\% in this \( t/R \) range. The reason why the use of an effective dielectric constant works well, is the relatively small difference between the dielectric constants of SiO\(_2\) and vacuum. This ensures that the \( t/R \) dependence of the gate capacitance is not changed much and only the gate coupling is reduced.

For comparison, gate capacitances for the high-\( k \) dielectric HfO\(_2\) (\( \epsilon_r = 25 \)) are calculated (Fig. 3). The fit of the calculated capacitances in the range \( 6 < t/R < 100 \) results in an effective dielectric constant of \( \epsilon_{r,\text{eff}} = 8.5 \). But clearly this fit does not describe the gate capacitances well. The reason is that the electric field is changed drastically compared to the embedded case due to the high dielectric constant. For high-\( k \) dielectrics, the radius of the NW becomes less important for the gate capacitance since the electric field gets more and more confined to the gate dielectric. This results in a weaker \( t/R \) dependence compared with SiO\(_2\).

A further point of interest is that much higher electric fields are reached when the NW is not embedded in the gate dielectric. The highest electric fields are near the contact between the NW and the gate dielectric. Assuming \( t = 120\text{nm} \) and \( R = 20\text{nm} \) as in Fig. 1, the electric field strength of SiO\(_2\) (10^5 V/cm) is reached locally at \( U_{gs} = 40\text{V} \) for the embedded NW, but already at \( U_{gs} = 6\text{V} \) for the non-embedded NW. For comparison, a 100nm thick SiO\(_2\) plate capacitor withstands roughly 100V. This is an important issue, especially if the gate hysteresis is and the durability are considered.

To obtain a high on-current in the NW-FET, a homogeneously induced charge density on the NW surface is important. The optimum case is obtained with a wrap-around NW-FET. In Fig. 4 the induced charge densities are shown for \( U_{gs} = 6\text{V} \). The charge density of the non-embedded NW-FET possess the same trend as the embedded one only at a lower level due to the weaker gate coupling. But at the contact point, the non-embedded NW shows an even stronger peak than the embedded NW because of the high electric fields. Importantly, the maximum amount of charges that can be induced in the embedded NW-FET is around 12 times higher than in non-embedded one for the above geometry. This is due to the higher gate capacitance and due to the higher maximum gate voltage. This voltage is scalable, if the \( t/R \) ratio is kept constant.

In addition, in various instances, the distance between the center of the NW and the back gate \( t \) has moreover been approximated by the thickness of the gate dielectric \( h = t - R \). In Fig. 2 the analytical values of Eqs. (1) and (2) while using this approximation
FIG. 4: FEM calculations of the induced charge density in elementary charges per cm$^2$ on the NW surface for non-embedded (solid line) and embedded (dashed line) NW-FETs with $R = 20$nm, $t = 120$nm, and $U_{gs} = 6$V.

are shown by “t-h approx”. For $t/R > 10$, the error is negligible but it becomes large for smaller values. This can result in values for the gate capacitance that are off by more than a factor of three.

Usually NWs grow with a non-cylindrical cross section. The actual shape rather depends on the crystal structure and the growth direction. For zinc-blende NWs grown in the $[111]$ direction, a hexagonal cross section is found while NWs grown in the $[001]$ direction have a square-like cross section. Furthermore, NWs grown in the $[112]$ direction with a triangular cross section have been observed. In Fig. 5 the calculated gate capacitances for NWs with these cross sections are shown. To make the results comparable, I define an effective radius $R^*$ as the radius of a circle with the same area as the hexagon, the square, or the triangle. The fits are carried out for $6 < t/R^* < 100$ and result in an effective dielectric constant of $\epsilon_{r,\text{eff}} = 2.25$ for the hexagonal, $\epsilon_{r,\text{eff}} = 2.45$ for the square-like, and $\epsilon_{r,\text{eff}} = 2.65$ for the triangular cross section. The higher effective dielectric constants are due to the larger contact area between these NWs and the gate dielectric compared to the line contact for NWs with circular cross section. This effect increases for smaller $t/R^*$ ratios. Because of the sharp corners, the electric field amplification is an important issue for these cross sections.

In conclusion, FEM calculations of the gate capacitance of back-gated NW-FETs using SiO$_2$ are discussed. Compared with the analytical model of completely embedded NWs, the capacitances of non-embedded NWs are nearly two times smaller. This can be accounted for by an effective dielectric constant of 2.20 within the analytical model of embedded NWs. However, for high-$k$ materials as HfO$_2$ this is not possible and the analytical solution cannot be applied. Due to the electric field amplification of non-embedded NWs, the dielectric strength of SiO$_2$ is reached locally at much lower gate voltages than for the planar geometry. Thus the gate control of the charge density inside the NW is drastically improved by embedding the NW. Furthermore, non-embedded NWs with non-circular cross sections have been considered.

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[1] S. Ramo, J.R. Whinnery, and Th. van Duizer, *Fields and waves in communication electronics* (Wiley, New York, 1993), Chap. 7.
[2] P.M. Morse and H. Feshbach, *Methods of theoretical physics*, (McGraw-Hill, New York, 1953), Chap. 10.
[3] S. De Franceschi, J. A. van Dam, E.P.A.M. Bakkers, L. F. Feiner, L. Gurevich, and L. P. Kouwenhoven, Appl. Phys. Lett. 83, 344 (2003).
[4] S.J. Tans, M.H. Devoret, H. Dai, A. Thess, R.E. Smalley, L.J. Geerlings, and C. Dekker, Nature 386, 474 (1997).
[5] M.T. Björk, C. Thelander, A.E. Hansen, L.E. Jensen, M.W. Larsson, L.R. Wallenberg, and L. Samuelson, Nano Lett. 4, 1621 (2004).
[6] W. Lu, J. Xiang, B.P. Timko, Y. Wu, and C.M. Lieber, PNAS 102, 10046 (2005).
[7] D. Wang, Q. Wang, A. Javey, R. Tu, H. Dai, H. Kim, P.C. McIntyre, T. Krishnamohan, and K.C. Saraswat, Appl. Phys. Lett. 83, 2432 (2003).
Finite element method calculations are performed using COMSOL Multiphysics v3.2. The capacitance is calculated via an integration of the electric field energy density $W_e (C = 2W_e/U_{gs})$ as well as via an integration of the induced charge density $Q$ on both electrodes ($C = Q/U_{gs}$).