Sherman: A Write-Optimized Distributed B⁺Tree Index on Disaggregated Memory

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Abstract

Memory disaggregation architecture physically separates CPU and memory into independent components, which are connected via high-speed RDMA networks, greatly improving resource utilization of databases. However, such an architecture poses unique challenges to data indexing due to limited RDMA semantics and near-zero computation power at memory-side. Existing indexes supporting disaggregated memory either suffer from low write performance, or require hardware modification.

This paper presents SHERMAN, a write-optimized distributed B⁺Tree index on disaggregated memory that delivers high performance with commodity RDMA NICs. SHERMAN combines RDMA hardware features and RDMA-friendly software techniques to boost index write performance from three angles. First, to reduce round trips, SHERMAN coalesces dependent RDMA commands by leveraging in-order delivery property of RDMA. Second, to accelerate concurrent accesses, SHERMAN introduces a hierarchical lock that exploits on-chip memory of RDMA NICs. Finally, to mitigate write amplification, SHERMAN tailors the data structure layout of B⁺Tree with a two-level version mechanism. Our evaluation shows that, SHERMAN is one order of magnitude faster in terms of both throughput and 99th percentile latency on typical write-intensive workloads, compared with state-of-the-art designs.

CCS Concepts

• Information systems → Data structures; • Software and its engineering → Distributed memory.

Keywords

disaggregated memory; index; RDMA

1 Introduction

The popularity of in-memory databases (e.g., SAP HANA [5]) and in-memory computing (e.g., Spark [74]) catalyzes ever-increasing demands for memory in modern datacenters. However, datacenters today suffer from low memory utilization (< 65%) [29, 45, 55, 61], which results from imbalanced memory usages across a sea of servers. In response, academia and industry are working towards a new hardware architecture called memory disaggregation, where CPU and memory are physically separated into two network-attached components – compute servers and memory servers [16, 23, 30, 36, 38, 39, 42, 49, 55, 56, 65, 71, 78, 79]. With memory disaggregation, CPU and memory can scale independently and different applications share a global disaggregated memory pool efficiently.

Since almost all CPUs are assembled on compute servers under the memory disaggregation architecture, memory servers have near-zero computation power, which highlights the challenge that how compute servers access disaggregated memory residing on memory servers. Fortunately, RDMA (Remote Direct Memory Access), a fast network technique, allows compute servers to directly access disaggregated memory unmediated by memory servers’ computation power with a single-digit-microsecond level latency, becoming an essential building block of memory disaggregation architecture [16, 23, 55, 79].

In this paper, we explore how to design a high-performance tree index, a key pillar of database systems, on disaggregated memory. We first revisit existing RDMA-based tree indexes and examine their applicability on disaggregated memory. Several RDMA-based tree indexes rely on remote procedure calls (RPCs) to handle write operations [47, 54]; they are ill-suited for disaggregated memory due to near-zero computation power of memory servers. For tree indexes that can be deployed on disaggregated memory, they also have some critical limitations: ① Some indexes using RDMA one-sided verbs for all index operation [81] (we call it one-sided approach); they can deliver high performance for read operations, but suffer from low throughput and high latency in terms of write operations, especially in high-contention scenarios (< 0.4 Mops with ~20ms tail latency, §3.1). ② Other indexes bake write operations into SmartNICs or customized hardware [6], which brings high TCO (total cost of ownership) and cannot be deployed in datacenters in a large scale immediately.

Our goal is designing a tree index on disaggregated memory that can deliver high performance for both read and write operations with commodity RDMA NICs. To this end, we further analyze what makes one-sided approach inefficient in write operations, and find
out three major causes. First, due to limited semantics of one-sided RDMA verbs, modifying an index node (e.g., tree node in B∗Tree) always requires multiple round trips (i.e., lock, read, write, and unlock), inducing high latency and further making conflicting requests more likely to be blocked. Second, the locks used for resolving write-write conflicts are slow and experience performance collapse under high-contention scenarios. This is because ① at the hardware level, NICs adopt expensive concurrency control to ensure atomicity between RDMA atomic commands, where each command needs two PCIe transactions. ② at the software level, such locks always trigger unnecessary retries, which consumes RDMA IOPS, and do not provide fairness, which leads to high tail latency. Third, the layout of index data structure incurs severe write amplification. Due to coarse-grained consistency check mechanisms (e.g., using checksum to protect a whole tree node), a small piece of modification will result in large-sized write-back across the network.

Motivated by the above analysis, we propose SHERMAN, a write-optimized distributed B∗Tree index on disaggregated memory. The key idea of SHERMAN is combining RDMA hardware features and RDMA-friendly software techniques to reduce round trips, accelerate lock operations, and mitigate write amplification. SHERMAN spreads B∗Tree nodes across a set of memory servers, and compute servers perform all index operations via RDMA one-sided verbs purely. SHERMAN uses a classic approach for concurrency control: lock-free search with versions to resolve read-write conflicts and exclusive locks to resolve write-write conflicts [44, 81].

To reduce round trips, SHERMAN introduces a command combination technique. Based on the observation that RDMA NICs already provide in-order delivery property, this technique allows client threads to issue dependent RDMA commands (e.g., write-back and lock release) simultaneously, letting NICs at memory servers reflect them into disaggregated memory in order.

To accelerate lock operations, we design a hierarchical on-chip lock (HOCL) for SHERMAN. HOCL is structured into two parts: global lock tables on memory servers, and local lock tables on compute servers. Global lock tables and local lock tables coordinate conflicting lock requests between compute servers and within a compute server, respectively. Global lock tables are stored in the on-chip memory of RDMA NICs, thus eliminating PCIe transactions of memory servers and further delivering extremely high throughput for RDMA atomic commands (~110 Mops). Within a compute server, before trying to acquire a global lock on memory servers, a thread must acquire the associated local lock, so as to avoid a large amount of unnecessary remote retries. Moreover, by adopting wait queues, local lock tables improve fairness between conflicting lock requests. Based on local lock tables, a thread can handle its acquired lock over to another thread directly, reducing at least one round trip for acquiring global locks.

To mitigate write amplification, SHERMAN tailors the leaf node layout of B∗Tree. First, entries in leaf node are unsorted, so as to eschew shift operations upon insertion/deletion. Second, to support lock-free search while avoiding write amplification, we introduce a two-level version mechanism. In addition to using a pair of node-level versions to detect the inconsistency of the whole leaf node, we embed a pair of entry-level versions into each entry, which ensures entry-level integrity. For insertion/deletion operations without split/merging events, only entry-sized data is written back, thus saving network bandwidth and making the most of the extremely high IOPS of small RDMA messages.

To demonstrate the efficacy of SHERMAN, we evaluate SHERMAN using a set of benchmarks. Under write-intensive workloads, SHERMAN achieves much better performance than FG [81], a state-of-the-art distributed B∗Tree supporting disaggregated memory. Specifically, in common skewed workloads, SHERMAN delivers one order of magnitude performance improvement in terms of both throughput and 99th percentile latency. Meanwhile, a SHERMAN tree can be accessed concurrently by more than 500 client threads, while providing peak throughput stably. For read-intensive workloads (i.e., 95% read operations), SHERMAN exhibits slightly higher throughput with 25% lower 99th percentile latency.

**Contributions.** The main contributions of this paper are:

- An analysis of existing tree indexes on disaggregated memory, demonstrating that the inefficiency of write operations in the one-sided approach stems from excessive round trips, slow synchronization primitives and write amplification (§3).
- The design and implementation of SHERMAN, a write-optimized B∗Tree index on disaggregated memory, which boosts write performance by combining RDMA hardware features and RDMA-friendly software techniques (§4).
- A set of evaluations that demonstrate the high performance of SHERMAN under different workloads (§5).

## 2 Background

In this section, we provide the background on memory disaggregation (§2.1) and RDMA network (§2.2) briefly.

### 2.1 Memory Disaggregation

Traditional datacenters pack CPU and memory into the same hardware units (i.e., monolithic servers), leading to low memory utilization (~ 65%) [29, 55, 61] and further increasing the TCO (total cost of ownership) of datacenters. To attack this problem, academia and industry are exploring a new hardware architecture called memory disaggregation [23, 42, 51, 55, 79], which is shown in Figure 1. In such an architecture, CPU and memory are physically separated into two different hardware units: compute servers (CSs) and memory servers (MSs). CSs own a mass of CPU cores (10s - 100s), but
MSs host high-volume memory (100s - 1000s GB) with near-zero computation power. CPUs in CSs can directly access the disaggregated memory in MSs via high-speed RDMA networks (§2.2). With memory disaggregation, CPU and memory can scale independently and applications can pack resources in a more flexible manner, boosting resource utilization significantly.

To reduce remote accesses from CSs to MSs, CSs are always equipped with a small piece of memory as the local cache (1 - 10 GB). Moreover, MSs own a small set of wimpy CPU cores (1 - 2) to support lightweight management tasks, such as network connection management and disaggregated memory allocation.

2.2 RDMA Network

RDMA network is the key enabler of memory disaggregation architecture. RDMA is increasingly popular in modern datacenters due to high bandwidth (e.g., 100Gbps) and low latency (2-μs) [21, 28]. RDMA provides two types of verbs, namely two-sided verbs and one-sided verbs, to applications. Two-sided verbs – RDMA_SEND and RDMA_RECV— are the same as traditional Linux socket interface: the sender generates messages via RDMA_SEND, and the receiver pre-posts RDMA_RECV commands as well as processes incoming messages. One-sided verbs, i.e., RDMA_WRITE, RDMA_READ and RDMA_ATOMIC (RDMA_FAA and RDMA_CAS), operate directly on remote memory without involving the CPUs of receivers. The direct-access feature of one-sided verbs makes memory servers with near-zero computation power possible.

RDMA hosts communicate via queue pairs (QPs). A QP consists of a send queue and a receive queue, and a completion queue (CQ) is associated with the QP. A sender performs an RDMA command by posting the request to the send queue. On completion, the sender’s NIC writes a completion entry into the CQ, and the sender can know it by polling the CQ. RDMA supports three transport types: reliable connected (RC), unreliable connected (UC), and unreliable datagram (UD). SHERMAN uses RC, since it supports all one-sided verbs and is reliable; yet, RC requires one-to-one connections between QPs (i.e., a QP can only communicate with one QP).

Sparked by high performance and new one-sided verbs of RDMA, there is an active line of research in RDMA-based indexing [6, 21, 47, 54, 81]. In this paper, we focus on distributed B*Tree index on disaggregated memory due to its elasticity and support for range query, but our ideas can be applied to other kinds of indexes.

3 Motivation

Designing a high-performance distributed tree index on disaggregated memory poses unique challenges. In this section, we first revisit two existing approaches — using one-sided verbs purely and extending RDMA interfaces — and reveal their respective issues (§3.1). Then, we analyze why using one-sided verbs is slow, which motivizes the design of SHERMAN (§3.2).

3.1 Existing Approaches

With near-zero computation power at MS-side, we cannot delegate index operations to CPUs of MSs via remote procedure calls (RPCs), which is the main difference between memory disaggregation and traditional architectures. Existing work enables efficient lookup operations via lock-free search and caching mechanisms [21, 47, 67, 81], leading to a single RDMA_READ in the ideal situation (i.e., cache hit). However, write operations are in a quandary due to their complex semantics; specifically, there are two avenues to design write operations, each of which has its own issues.

3.1.1 Using One-sided Verbs Purely. FG [81], a distributed RDMA-based B*Tree, is the only one tree index that completely leverages one-sided verbs to perform index write operations (so it can be deployed on disaggregated memory). Specifically, FG uses a B-link tree structure [40] and distributes tree nodes across different servers. For write operations, it adopts a lock-based approach, where tree node modification is protected by RDMA-based spinning locks; the locks leverage RDMA_CAS for lock acquisition and RDMA_FAA for lock release. For read operation, FG follows a lock-free search scheme, where threads fetch tree nodes via RDMA_READ without holding locks and then check the consistency using checksum. FG does not adopt any caching mechanism.

We conduct an experiment to evaluate FG’s performance. Since FG is not open-source, we implement it from scratch; we also cache internal tree nodes to reduce remote accesses. Table 1 shows the result, and we make two observations. First, in read-intensive workload (95% lookup and 5% insert/update), FG can achieve high throughput (> 30Mops) and low 99th percentile latency (< 16μs). Second, in write-intensive workload (50% lookup and 50% insert/update), FG delivers 18Mops with 19μs tail latency under the uniform setting; yet, its performance collapses in case of skew setting, where the key popularity follows a Zipfian distribution (i.e., Zipfian distribution) [8, 20, 31], where a small number of hot items receive frequent accesses. (iii) More and more applications exhibit write-intensive workloads, such as graph computation [26], parameter servers [41], and data warehousing systems [64]. The inefficiency of write operations comes from excessive round trips, slow synchronization primitives, and write amplification, which we will elaborate in §3.2.

3.1.2 Extending RDMA Interfaces. Another approach to designing indexes on disaggregated memory is extending RDMA interfaces. This approach offloads index write operations into memory servers’ NICs via SmartNICs or other customized hardware [6, 14, 22, 37, 43, 53, 59]. For example, by exploiting interface extensions (i.e., indirect addressing and notification), researchers propose HT-Tree (without

| Throughput (Mops) | uniform | skew |
|-------------------|---------|------|
| 50th              | 31.8    | 32.9 |
| 90th              | 4.7     | 6.4  |
| 99th              | 19.5    | 21.2 |
| Latency (μs)      |         |      |
| 50th              | 4.7     | 9.5  |
| 90th              | 6.2     | 14.3 |
| 99th              | 15.3    | 19   |

Table 1: Index performance in one-sided approach (100 Gbps ConnectX-5 NICs, 8 MSs, 8 CSs with 176 client threads, 8/8-byte key/value, 1 billion key space). The performance collapses under write-intensive and skew setting.
improvements) [6], a hybrid index combining the hash table and tree. Yet, compared with commodity RDMA NICs, SmartNICs come at the price of higher TCO (total cost of ownership) and lower performance. More specifically, SmartNICs have much higher market price (~5×) than that of commodity RDMA NICs at present [62]. As for performance, at 100Gbps network environment, StRoM [59], the state-of-the-art RDMA extensions using FPGA, has 2× higher RDMA_READ/RDMA_WRITE round-trip latency (4μs) against commodity RDMA NICs (~2μs).

Table 2 shows a comparison of RDMA-based distributed tree indexes. Among them, Cell [47] and FaRM-Tree [54] use RPCs for write operations, so they cannot be deployed on disaggregated memory. FG [81] suffers from low write performance and HT-Tree [6] needs hardware modification. Sherman aims to achieve high performance (for both read and write operations) with commodity RDMA NICs on disaggregated memory.

|                  | Cell [47] | FaRM-Tree [54] | FG [81] | HT-Tree [6] | Sherman |
|------------------|-----------|----------------|---------|-------------|---------|
| **Read Performance** | Medium    | High           | Medium  | High        | High    |
| **Write Performance** | Medium    | High           | Low     | High        | High    |
| **No Hardware Modification** | ✓         | ✓              | ✓       | ✓           | ✓       |
| **Support Disaggregated Memory** | ✓         | ✓              | ✓       | ✓           | ✓       |

Table 2: A comparison of RDMA-based distributed tree indexes. All indexes use one-sided verbs for read operations. HT-Tree is a hybrid index combining the hash table and tree, and the remaining four are B²Tree structure. Cell executes write operations via RPCs; it only caches tree nodes near the root (at least four node levels above the leaf node level), so all read/write operations need four round trips at least. FaRM-Tree implements write operations by exploiting transactions, which in turn uses RPCs; it caches all internal tree nodes. FG leverages one-sided verbs to realize write operations, and does not use any caching mechanism. HT-Tree is a conceptual design without implementation, which relies on hardware extensions.

3.2 Why One-sided Approach is Slow?

Using analysis and experiments, we show the inefficiency of write operations using one-sided verbs stems from excessive round trips, slow synchronization primitives, and write amplification.

3.2.1 Excessive Round Trips. The most obvious cause of slow write operations is excessive round trips. For example, when modifying a tree node (not consider node split/merging), a client thread needs 4 round-trips: ➀acquiring associated exclusive lock, ➁reading the tree node, ➂writing back the modified tree node ➃and finally releasing the lock. Excessive round trips negatively impact write performance in two aspects. First, the latency of a single write operation is proportional to the number of round trips. Second, more round trips lead to the longer critical path, so conflicting write operations (i.e., requests targeting at the same tree nodes) are more likely to be blocked, degrading the concurrency performance.

3.2.2 Slow Synchronization Primitives. RDMA-based locks used in these indexes cannot provide usage synchronization under a variety of workloads. We conduct an experiment to present performance issues of such locks. In the experiment, 154 threads across 7 CSs acquire/release 10240 locks residing in an MS; we choose the RDMA verbs used by FG [81], where RDMA_CAS for lock acquisition and RDMA_FAA for release. The access pattern follows Zipfian distribution and we vary Zipfian parameter to control the contention degree (0 is uniform setting, and 0.99 is the most common real-world scenario). Figure 2 shows the result. The system experiences performance collapse in terms of throughput and latency under high-contention settings. We attribute the performance collapse to the following three reasons.

**Expensive in-NIC concurrency control.** To guarantee correct atomicity semantic between RDMA_ATOMIC commands targeting the same addresses, RDMA NICs adopt an internal locking scheme [34]. More specifically, a NIC maintains a certain number of buckets (e.g., 4096), and puts RDMA_ATOMIC commands having the same certain bits in their destination addresses (e.g., 12 LSBs) into the same bucket. Commands in the same bucket are considered conflicting. An RDMA_ATOMIC can not be executed until the previous conflicting commands are finished. Unfortunately, a single RDMA_ATOMIC needs two PCIe transactions: ➀reading data from CPU memory into the NIC and ➁writing back after modification (➋can be omitted in case of failed RDMA_CAS). These PCIe transactions stretch the queuing time of conflicting RDMA_ATOMIC commands and thus degrade concurrency performance of RDMA_ATOMIC commands, especially in high-contention workloads.

**Unnecessary retries.** When failing to acquire a lock, the client thread retries. Different from locks designed for shared memory with coherent cache, such retries in the RDMA environment require remote network accesses, squandering limited throughput of NICs in both senders and receivers. Retries can be eliminated via notification mechanisms, where a client thread is notified when the lock it wants to acquire has been released. Yet, notification needs remote CPU involvement, which is impractical on disaggregated memory, or specialized hardware like programmable switches [73].

**Lacking Fairness.** Existing locks in RDMA-based indexes do not take into account fairness between conflicting lock acquisition, thus starving some client requests and further inducing high tail latency.
3.2 Write Amplification. RDMA prefers small IO size, but indexes using one-sided verbs fail to exploit this feature. Figure 3 shows the throughput of outbound/inbound RDMA_WRITE under varied IO sizes\(^4\). When IO size is less than or equal to 128 bytes, the throughput is more than 50Mops; however, when IO size reaches 256 bytes, NICs’s hardware bandwidth restricts throughput; our result is consistent with previous studies \([68]\). Yet, existing RDMA-based indexes always trigger large-sized RDMA_WRITE, suffering from write amplification. This issue stems from two causes. 

**Sorted layout.** A B\(^+\)Tree keeps entries in each tree node sorted, to support traversal in internal nodes and binary search in leaf nodes. To ensure this property, when an entry is inserted/deleted to/from a node, all the entries on the right side of the insertion/deletion position need to be shifted. The shift operations cause extra data to be written via RDMA_WRITE. 

**Coarse-grained consistency check.** In order to read tree nodes in a lock-free way and detect incomplete data due to ongoing writes, two main consistency check mechanisms are proposed. In the first mechanism (Figure 4(a)), each node includes a checksum covering the whole node area (except the checksum itself) \([46, 81]\); the checksum is re-calculated when modifying the corresponding node, and is verified when reading the node. The other mechanism, namely version-based consistency check (Figure 4(b)), stores a version number at the start and end of each node \([47]\); when modifying a node via RDMA_WRITE, the corresponding two version are incremented; a node’s content obtained via RDMA_READ is consistent only when the two versions are the same\(^5\). Since the granularity of the above two mechanisms is tree node, any modification to part of the node area requires to write back the whole node (include the metadata, e.g., checksum and version), leading to severe write amplification.

4 Design

Motivated by our observations about root causes of inefficient write operations (§3.2), we design SHERMAN, a write-optimized distributed B\(^+\)Tree index on disaggregated memory. In this section, we begin by presenting our design principles (§4.1), proceed to give an overview of SHERMAN (§4.2), and then describe our key techniques (§4.3–§4.5). Finally, we conduct a discussion (§4.6).

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\(^4\)Outbound/inbound throughput: the throughput of sending/receiving RDMA_WRITE commands from a NIC.

\(^5\)Like Cell \([47]\), we observe that the NIC reads data in increasing address order, so we omit per-cache line version mechanisms used by FaRM \([21]\).
4.2.2 Concurrency Control. SHERMAN adopts lock-based write operations and lock-free read operations.

Write-write conflicts. SHERMAN uses node-grained exclusive locks to resolve write-write conflicts: before modifying a tree node, the client thread must acquire the associated exclusive lock. These exclusive locks are hierarchical: local lock tables at CS-side and global lock tables in on-chip memory of MS’s NICs (§4.3). Such a hierarchical structure avoids PCIe transactions at MS-side, reduces remote retries, and improves fairness.

Read-write conflicts. SHERMAN supports lock-free search, which leverages RDMA_READ to fetch data residing in MSs without holding any lock. Moreover, SHERMAN uses versions to detect inconsistent data caused by concurrent writes. However, different from traditional mechanisms that use node-level versions, SHERMAN proposes a two-level version mechanism, which combines entry-level and node-level versions, to mitigate write amplification (§4.4).

4.2.3 Cache Mechanism. To reduce remote accesses in the tree traversal, SHERMAN adopts a cache mechanism. Each CS maintains an index cache, which only makes two types of internal nodes’ copies: a nodes above the leaf nodes (level 1 in Figure 5), and b the highest two levels of node (including root). A client thread firstly searches type a cache. On hit, it fetches the targeted leaf node directly from MSs; otherwise, it searches type b cache and then traverses to leaf nodes via remote accesses. The type b is always cached; the type a is structured as a lock-free skip-list, and applies power-of-two-choices [48] for eviction: selecting two cached nodes randomly and evicting the one least recently used. The index cache never induces data inconsistency issues for two reasons. First, internal nodes in B+Tree only contain location information, and the real data stored in leaf nodes are always accessed by RDMA commands. Second, in every node, we store a lower bound and upper bound for the set of keys that can appear in it (i.e., fence keys [27]), and we also store the level of the node (leaf nodes are level 0). When fetching a node from MSs, we check whether fence keys and node level are legal; if not, we invalidate the cache entry steering us to the wrong node and retry.

4.2.4 Memory Management. In each MS, we reserve a dedicated memory thread to manage disaggregated memory. The memory

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Figure 5: SHERMAN’s architecture and interactions.

Figure 6: Pseudo-code of hierarchical on-chip lock (HOCL). combine_list is used to collect commands of RDMA_WRITE that can be issued together (§4.5).
and improve fairness. Moreover, locks can be handed over between client threads within the same CSs, thus saving at least one round trip. Figure 6 shows the pseudo-code of HOCL.

**On-chip lock table.** Current RDMA verbs support device memory programming [1]. Specifically, an RDMA NIC can expose a piece of its on-chip memory to the upper applications, which can be allocated and read/written by RDMA commands. The on-chip memory eliminates PCIe transaction at receiver-side, thus providing extremely high throughput (~110 Mops RDMA_CAS). SHERMAN separates locks from tree nodes, and stores locks into on-chip memory at MS-side; each tree node is in the same MS as the lock protecting it. These locks in each MS are structured as an array, namely global lock table (GLT). When locking a tree node, the client thread first hashes the address of the tree node into a position number in the corresponding GLT (line 5 in Figure 6), and then issues an RDMA_CAS command to the lock, which tries to change it from 0 to the 16-bit CS identifier atomically (line 18). For lock release, the client thread clears the lock via an RDMA_WRITE (line 31 and 34).

An important consideration of GLT is the on-chip memory size. In the NIC we use (i.e., ConnectX-5), 256KB on-chip memory is available. To accommodate more locks, we make the granularity of RDMA_CAS finer (16 bits rather than 64 bits), by applying an infrequently used RDMA verb called masked compare and swap [2], which allows us to select a portion of 64-bit for RDMA_CAS operations. Thus, an MS can maintain 131,072 locks in its GLT, enabling extremely high concurrency, particularly considering that we only lock at most one tree node at a time for a single write operation [52]. To the best of our knowledge, SHERMAN is the first RDMA-based system that leverages on-chip memory of commodity RDMA NICs. A concurrent work leverages NIC’s on-chip memory to accelerate Ethernet network functions [30].

**Hierarchical structure.** SHERMAN maintains a local lock table (LLT) in each CS, to coordinate conflicting lock requests within the same CSs. The LLT stores a local lock for each lock of all GLTs. When a thread needs to lock a tree node, it first acquires the associated local lock in LLT (lines 6, 7, 13), and then acquires the associated lock in GLT; thus, conflicting lock requests from the same CSs are queued on the LLT at CS-side, avoiding unnecessary remote retries and thus saving RDMA IOPS. Moreover, each local lock in LLT is associated with a wait queue. A thread that cannot acquire a local lock in LLT pushes itself into the corresponding queue; the thread can learn if its turn has arrived by checking whether it is at the head of the queue (lines 8-14). The queue provides first-come-first-served fairness among threads within the same CSs. For lock release, the thread first releases the lock in GLT and then the local lock in LLT. Of note, an LLT consumes small local memory space of each CS; in our implementation, each local lock is 8-byte, so an LLT uses n MB space, where n is the number of MSs (i.e., n = 8 * 131072 bytes).

**Handover mechanism.** The hierarchical structure of HOCL enables a handover mechanism: handing over a lock from one client thread to another. When releasing a lock, if a thread finds out the lock’s wait queue is not empty, it will hand the lock over to the one at the head of the wait queue (lines 24-26). To avoid starving threads at other CSs, we limit the maximum number of consecutive handovers to 4. The thread that is handed over a lock no longer needs remote accesses for acquiring the lock, thus saving at least one round trip (lines 15-16).

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**Figure 7:** Pseudo-code of SHERMAN’s insertion procedure. To simplify exposition, we omit the details on 1) traversing the tree in case of index cache miss and 2) following sibling pointers in case of concurrent node split/merging.

```plaintext
1 NODE_SIZE # size of a tree node
2 ENTRY_SIZE # size of an entry
3
4 def Sherman_insert(key, value):
5     leaf_addr = index_cache.find(key) # search index cache
6         # lock the targeted leaf node
7     node = RDMA_READ(leaf_addr, NODE_SIZE) # RDMA_READ(remote_addr, size);
8     combine_list = () # RDMA_WRITE task list: (buffer, addr, size)
9
10 if leaf_addr.ms_id == sibling_addr.ms_id:
11     # if a node is locked by the same CS:
12     entry = node.entry
13     idx = entry.k.value
14     # check at the beginning of insertion
15     if entry.k.value == key:
16         # update/insert
17         combine_list.push((node, leaf_addr.offset(entry)), ENTRY_SIZE))
18     else:
19         # split
20         sibling = malloc(NODE_SIZE) # local buffer
21         sibling_addr = remote_alloc(NODE_SIZE) # allocate memory at MSs
22         node.sort().move_half_entries_to(sibling) # sort and move
23         link(node, sibling) # link sibling and list: ... node => sibling ...
24         update_feches(node, sibling)
25         # node-level node modification
26         node.add(key, value)
27         node.front_node_ver++
28         node.rear_node_ver++
29         # collect a combined command for write-back of the sibling node
30         combine_list.push((sibling, sibling_addr, NODE_SIZE))
31
32 if leaf_addr.ms_id == sibling_addr.ms_id:
33     # collect a combined command for write-back of the sibling node
34     combine_list.push((node, leaf_addr.offset(entry)), ENTRY_SIZE))
35     else:
36         RDMA_WRITE(sibling, sibling_addr, NODE_SIZE)
37         # collect a combined command for write-back of the leaf node
38         combine_list.push((node, leaf_addr, NODE_SIZE))
39     RDMA_UNLOCK(leaf_addr, combine_list) # unlock the targeted leaf node
40     if sibling != None: # update internal nodes
41         insert_internal(sibling.entry[0].k, sibling_addr)
```

4.4 Two-Level Version

To address the write amplification issue, SHERMAN incorporates a two-level version mechanism. First, SHERMAN uses unsorted leaf nodes so that shift operations upon insertion/deletion can be avoided. Unsorted leaf nodes complicate write operations in two aspects, as shown in Figure 7: (i) When looking up a key, the client thread needs to traverse the entire targeted leaf node (line 11). (ii) Before splitting a leaf node, the client thread must sort the entries in it (line 21). Given the microsecond-level network latency, the added overhead is slight. Although previous work on persistent memory data structures leverages unsorted nodes to reduce persistence overhead [19, 70], we are the first one that uses it to alleviate write amplification of indexes on disaggregated memory.

Second, SHERMAN introduces entry-level versions to enable fine-grained consistency check, as shown in Figure 8. Specifically, in leaf nodes, each entry is surrounded by a pair of 4-bit entry-level versions (i.e., FEV and REV). In case of insertion without splitting, the associated entry-level versions are incremented and only the modified entry (includes FEV and REV) is written back via RDMA_WRITE (lines 13-17 in Figure 7), thus evading write amplification. Also, a
Figure 8: The format of internal nodes and leaf nodes in SHERMAN. FNV/RNV is 4-bit front/rear node version; FEV/REV is 4-bit front/rear entry version. The entries in leaf nodes are unsorted. Entry-level versions are updated in case of insertion/deletion without split/merging. Node-level versions are updated in case of node split/merging.

Figure 9: Pseudo-code of SHERMAN’s lookup procedure. RDMA command only after receiving the acknowledgement of the preceding one [81]. Yet, we observe that RDMA already provides a strong ordering property at the hardware level: in a reliable connected (RC) queue pair, RDMA_WRITE commands are transmitted in the order that they are posted, and the NIC at receiver-side executes these commands in order [7, 77]. By leveraging this ordering property, SHERMAN combines multiple RDMA_WRITE commands in a write operation, so as to reduce round trips.

There are two cases that SHERMAN combines multiple RDMA_WRITE commands. First, since a tree node and its associated lock co-locate at the same MS, the write-back of tree node and lock release can be combined through aQP (lines 17, 35 in Figure 7 and line 31 in Figure 6), as opposed to issuing an unlock request after receiving acknowledgement of write-back; thus, one round trip is saved and the critical path shortens. Second, when a node (we call it A here) splits, we check whether the newly allocated sibling node belongs to the same MS as A; if so, three RDMA_WRITE commands can be combined together: ➀ write-back of the sibling node, ➁ write-back of A and ➂ release of A’s lock (line 31 in Figure 7).

Client threads issue these combined commands to the targeted MS by posting a linked list of them in one call (line 34 in Figure 6); such a combination not only saves round trips, but also reduces CPU usages and PCIe transactions. In addition, we only mark the last one in the list as signaled (i.e., generate a completion entry to the corresponding CQ), so NIC-initiated DMAs for writing completion entries can be reduced [34].

4.6 Discussion

Generality of RDMA features used by SHERMAN. SHERMAN leverages two RDMA hardware features: in-order property and on-chip memory. The in-order property is defined in RDMA specification [7]. The on-chip memory is supported in Mellanox’s ConnectX-5 NICs (announced in 2016) and above [1]. Note that ConnectX-5 NICs and above are already widely used in datacenters; for example, Alibaba uses ConnectX-5 NICs to build a performant production-level cloud storage system [25].

Generality of SHERMAN’s techniques. SHERMAN’s techniques can be applied to other kinds of indexes. Specifically, any lock-based indexes (e.g., bucket hash table) can use HOCL and command combination to improve concurrency performance and reduce round trips. If an index follows lock-free search scheme, the two-level version mechanism is a good choice to mitigate write amplification.

```python
1 def Sherman_lookup(key):
2     leaf_addr = index_cache.find(key)
3     retry:
4     node = RDMA_READ(leaf_addr, sizeof(node))
5     # node-level check
6     if node.front_node_ver != node.rear_node_ver:
7         goto retry
8     if e fron_entry_ver != e.rear_entry_ver:
9         # entry-level check
10     if e.front_entry_ver != e.rear_entry_ver:
11         goto retry
12     return e.v
13     return None
```
5 Evaluation

In this section, we evaluate SHERMAN to answer following questions:
- How does SHERMAN perform under different workloads, and how do the different techniques employed in SHERMAN contribute to overall performance (§5.2 and §5.3)?
- How scalable is SHERMAN when varying client threads (§5.4)?
- How SHERMAN's techniques impact internal metrics, e.g., the number of round trips and write amplification (§5.5)?
- How do parameters of SHERMAN, e.g., key size and cache index size, impact performance (§5.6)?
- How does HOCL perform (§5.7)?

5.1 Setup

5.1.1 Hardware Platform. Since memory disaggregation hardware is unavailable, we use a cluster of commodity, off-the-shelf servers to emulate MSs and CSs by limiting their usages of CPUs and memory [55]. Our cluster consists of 8 servers, each of which is equipped with 128GB DRAM, two 2.2GHz Intel Xeon E5-2650 v4 CPUs (24 cores in total), and one 100Gbps Mellanox ConnectX-5 NIC, installed with CentOS 7.7.1908 (Linux kernel version is 3.10.0). All these servers are connected with a Mellanox MSB7790-ES2F switch. For Mellanox ConnectX-5 NICs, the versions of driver and firmware are ofed 4.7-3.29.0 and 16.26.4012, respectively. Due to the limited size of our cluster, we emulate each server as one MS and one CS. Each MS owns 64GB DRAM and 2 CPU cores, and each CS owns 1GB DRAM and 22 CPU cores.

5.1.2 Compared Systems. FG [81] is the only distributed B+Tree that supports disaggregated memory. Since FG is not open-source, we implement it from scratch. For fair comparison, we add necessary optimizations to it: (i) index cache for reducing remote accesses, (ii) using RDMA_WRITE to release lock rather than expensive atomic verb RDMA_FAA. In order to distinguish our modified version of FG from the original one, we call it FG+ in the evaluation. The performance of FG+ is higher than that reported in FG paper [81].

5.1.3 Workloads. We explore different aspects of the systems by using YCSB workloads [20]. We use five types of read-write ratio, as shown in Table 3. Note that insert operations include updating existing keys (about 2/3 of all insert operations).

There are two types of key popularity: uniform and skewed. In uniform workloads, all keys have the same probability of being accessed. Skewed workloads follow a Zipfian access distribution

![Figure 10: Contributions of techniques to performance (skewed workloads, skewness=0.99).](image)

| Workload     | Insert | Lookup | Range Query |
|--------------|--------|--------|-------------|
| write-only   | 100%   | 50%    | 100%        |
| write-intensive | 50%   | 95%    | 50%         |
| read-intensive | 5%    | 100%   | 50%         |
| range-only   | 50%    |        |             |
| range-write  |        |        |             |

Table 3: Workloads.

(Zipfian parameter, i.e., skewness, is 0.99 by default), which is common in production environments [18, 20].

Unless otherwise stated, all the experiments are conducted with 8 MSs and 8 CSs. Each CS owns 500MB index cache, and launches 22 client threads (176 in total in our cluster). For each experiment, we bulkload the tree with 1 billion entries (8-byte key, 8-byte value) 80% full, then perform specified workloads. The size of a tree node (i.e., internal node and leaf node) is 1KB. All plots in this section present the average of 3 or more runs.

5.2 Overall Performance

To analyze SHERMAN’s performance, we break down the performance gap between FG+ and SHERMAN through applying each technique one by one. Figure 10 and Figure 11 show the results under skewed and uniform workloads, respectively.

In these two figures, +Combine stands for command combination technique. +On-Chip and +Hierarchical are two design parts of HOCL: leveraging on-chip memory of NICs to store locks, and hierarchical structure with handover mechanism, respectively. +2-Level Ver represents two-level version mechanism, and shows the final performance of SHERMAN.

5.2.1 Skewed Workloads. We make following observations from Figure 10. First, in both write-only and write-intensive workloads, SHERMAN has much higher throughput and lower latency against FG+. Specifically, in write-only workloads, SHERMAN achieves 24.7× higher throughput with 1.2× lower median latency (50p latency) and 35.8× lower 99th percentile latency (99p latency). In write-intensive workloads, SHERMAN achieves 23.6× higher throughput with 1.4×/ 30.2× lower 50p/99p latency.

Second, all techniques contribute to the high write efficiency of SHERMAN. Here we analyze each technique in terms of write-intensive workloads (write-only workloads have the same conclusions): ① Command combination improves the throughput by 3.37× and reduces the 50p/99p latency by 1.14×/3.18×, since it
which comes from the following three reasons. First, by acquiring local locks before remote ones, unnecessary RDMA_CAS retransmits from the same CSs are avoidable, mitigating the consumption of RDMA NICs’ limited IOPS. Second, the local locks in each CS guarantee first-come-first-served fairness by maintaining wait queues, thus lowering tail latency. Third, the handover mechanism saves one round trip opportunistically. Two-level version mechanism does not bring considerable throughput improvement (only 3%), since the major bottleneck is concurrent conflicts rather than RDMA IOPS at this time; the 50p latency is reduced by 400ns (from 7.3μs to 6.9μs), since smaller RDMA WRITE IO size has shorter PCIe DMA time at both CS-side and MS-side.

Third, in read-intensive workloads (Figure 10(c)), SHERMAN does not present considerable performance improvement, as expected, since all techniques we propose aim to boost performance of write operations. Yet, there are still two points worth noting here: 1) By saving round trips for 5% insert operations, command combination reduces 99p latency from 15.3μs to 12.9μs. 2) SHERMAN increases the 50p latency by 100ns (2%), we contribute it to unsorted leaf node layout, which causes traversal of the entire leaf node even for non-existing keys.

5.2.2 Uniform Workloads. As shown in Figure 11, compared with FG+, SHERMAN delivers 1.24× and 1.15× higher throughput in write-only and write-intensive workloads, respectively. These improvements mainly come from command combination and two-level version. Command combination saves round trips, so each client thread can execute more insert operations per second; two-level version reduces IO size of RDMA_WRITE from node size to entry size, thus giving full play to the RDMA’s characteristics of extremely high small IO rate. HOCL is designed for high-contention scenarios (i.e., skewed workloads), so it does not increase throughput in uniform workloads. As for latency, SHERMAN reduces 50p/99p latency by 1.24×/2.01× and 1.19×/1.27× in write-only and write-intensive workloads, respectively, which mainly is contributed to command combination and HOCL: command combination saves round trips, and HOCL saves PCIe transaction time in MS-side as well as improves the fairness of locks.

5.3 Range Query Performance

In this experiment, we evaluate the performance of range query by using range-only and range-write workloads. The targeted range follows the skewed access pattern. Figure 12(a) shows the performance of range-only workloads, from which we make two observations. First, when the range size equals 100, FG+ outperforms SHERMAN by 2%. This is because the unsorted leaf layout in SHERMAN leads to unnecessary scans when targeted leaf nodes are partially occupied. Second, as range size grows (i.e., 1000), the throughput of SHERMAN and FG+ drops and is almost the same, since network bandwidth becomes the bottleneck.

Figure 12(b) shows the throughput of range query, under range-write workloads. Half of the client threads issue insert operations, and the other half issue range query operations. SHERMAN outperforms FG+ by up to 1.82×. This is because SHERMAN’s write operations save a considerable quantity of network resources for range query operations. Specifically, HOCL significantly decreases the number of RDMA messages via lock handover and the hierarchical structure; two-level version mechanism reduces the RDMA_WRITE IO size from node level to entry level.
we bind multiple coroutines to every core of CSs; coroutines are useful work. We use write-intensive workloads. Figure 13 shows after initiating RDMA commands, allowing other coroutines to do useful work. We use write-intensive workloads. Figure 13 shows the results under uniform and skewed scenarios. We make the following observations.

First, in uniform workloads, both SHERMAN and FG+ can scale well. In case of 528 client threads, SHERMAN achieves 44 Mops, 1.14× the throughput of FG+. The improvement mainly comes from two-level version mechanism: by writing back leaf nodes in a smaller granularity, more RDMA bandwidth are saved for RDMA_READ commands and lock operations.

Second, in skewed workloads, a higher contention degree (i.e., larger skewness value) leads to lower peak throughput. Specifically, SHERMAN achieves 21 Mops peak throughput in case of 0.9 skewness, which is 1.44× higher than that of FG+; and 9 Mops in case of 0.99 skewness, which is 1.4× higher than that of FG+. This is because the more serious the contention, the more likely concurrent write operations to be blocked, degrading the peak throughput.

Third, in skewed workloads, SHERMAN can provide sustainable throughput when more client threads are added; yet, FG+ experiences performance collapse. We attribute the SHERMAN’s stable performance to a combination of all techniques we propose, as stated in §5.2.1.

5.5 In-Depth Analysis

In order to unveil detailed information of SHERMAN, we collect statistics for various internal metrics, including the number of read retries, the number of round trips, and write size, to perform an in-depth analysis. We choose write-intensive workloads with a skewed access pattern (skewness=0.99).

5.5.1 Retry Counts

Figure 14(a) shows retry counts of lookup operations. We make two observations. First, for FG+ and SHERMAN, 99.98% of lookup operations do not requires retries. This is because PCIe links already guarantee a certain level of atomicity: a PCIe read transaction is strictly ordered after prior PCIe write transactions [33]. Such a guarantee circumvents most interleaving accesses between read and write operations. Second, FG+ experiences a few multiple times (e.g., 9) of read retries. This is because FG+ does not adopt SHERMAN’s two-level mechanism, causing larger RDMA IO size with longer DMA times at MS-side and thus increasing the likelihood that lookup operations fetch inconsistent tree nodes.

5.5.2 The Number of Round Trips

Figure 14(b) reports the cumulative distribution of write operations’ round trips. We make three observations. First, 94% of write operations need 4 round trips in

Figure 13: Scalability of SHERMAN (write-intensive workloads).

Figure 14: In-depth analysis using internal metrics (write-intensive workloads, skewness=0.99).
FG+, while 93.6\% need 3 round trips in SHERMAN. The reason is that SHERMAN uses command combination technique to coalesce write-back and lock release. Second, 3.6\% of write operations in SHERMAN only need 2 round trips, since HOCL’s handover mechanism saves one round trip opportunistically. Third, for FG+, the 99th percentile of round trips is 453, which explains why its tail latency is so high (§5.2.1). In contrast, SHERMAN leverages HOCL to avoid massive lock retries and offer fairness; thus, its 99th percentile of round trips is 11, ensuring low tail latency.

5.5.3 Write Size. Figure 14(c) shows the write size of write operations. Since we use skewed workloads which have strong access locality, only about 0.4\% of write operations trigger node splits, inducing large than 1KB writes. As shown in the figure, for write operations without node splits, SHERMAN only needs to write back 17 bytes (i.e., 16-byte key-value pair along with two 4-bit versions) by using two-level version mechanism, rather than writing back the whole tree node, thus eliminating write amplification.

5.6 Sensitivity Analysis

5.6.1 Key Size. Here we study how key size affects SHERMAN’s performance. Since SHERMAN embeds keys in tree nodes, in this experiment we fix the number of entries in a leaf node to 32 by changing the size of leaf nodes. We bulkload the tree with 200 million entries 80\% full and then perform write-intensive workloads. Figure 15(a) shows the throughput under uniform workloads. We make two observations. First, as the key size grows, the performance of both SHERMAN and FG+ drops. This is because every index operation needs to fetch the whole leaf node via RDMA_READ, and thus larger node size (caused by larger key size) consumes more network bandwidth for each index operation. Second, as the key size grows from 16B to 1KB, the performance advantage of SHERMAN over FG+ increases from 1.17× to 1.47×, since two-level version in SHERMAN can save more bandwidth for larger tree nodes.

Figure 15(b) presents the throughput under skewed workloads. Since FG+ suffers from low throughput in high-contention scenarios, the increasing key size does not affect its throughput. When the key size is 1KB, SHERMAN still outperforms FG+ by 1.4×.

5.6.2 Index Cache Size. In order to study how the index cache size affects the performance of SHERMAN, we conduct an experiment with uniform and write-intensive workloads. Figure 15(c) shows the result. As the cache index capacity grows, both SHERMAN’s performance and cache hit ratio increase. For large dataset (i.e., 1 billion entries in our evaluation), a 400MB index cache can bring a cache hit rate close to 98\%, which demonstrates the efficiency of our index cache design.

5.7 HOCL Performance

In this experiment, we evaluate the performance of HOCL. We launch 176 threads across 8 CSs to acquire/release 10240 locks stored in an MS. These operations follow a skewed access pattern with 0.99 skewness. Figure 16 shows the result. Putting locks into on-chip memory improves the throughput by 2.89× and reduces the 50p/99p latency by 3.01×/2.88×, since on-chip memory eliminates PCIe transactions for RDMA_CAS commands at MS-side, making processing units in NICs more efficient and shortening queuing time of conflicting commands. By introducing local lock tables at CS-side and further forming a hierarchical structure, we gain 3.85×, 5.39×, and 3.65× improvement in throughput, 50p latency, and 99p latency, respectively. This is because a thread can issue RDMA_CAS to acquire a remote lock only when no thread at the same CS holds this lock, avoiding a large amount of failed RDMA_CAS retries and further saving RDMA IOPS. Wait queues provide first-come-first-served fairness within a CS; as a result, the 99p latency is reduced from 414μs to 372μs. Handover mechanism further improve the throughput by 2.34× and reduces the 99p latency by 3.19×, since by handing over locks from a thread to another thread locally, remote locking via RDMA_CAS commands can be avoided, accelerating lock acquisition.
6 Related Work

To our knowledge, SHERMAN is the first tree index on disaggregated memory that can deliver high performance for both read and write operations with commodity RDMA NICs. We discuss two aspects of related work: RDMA-based databases and memory disaggregation.

6.1 RDMA-based Databases

Fast RDMA network spurs researchers to build new distributed databases. FaRM [21, 54] provides general distributed transactions by using RDMA for messaging and direct-access to remote memory. DrTM [69] leverages the strong consistency between RDMA and HTM (hardware transaction memory) to transform a distributed transaction into a local one. FaSST [35] argues that two-sided unreliable verbs have higher scalability than one-sided verbs; thus, FaSST proposes a fast RPC framework using two-sided unreliable RDMA and builds an OCC-based distributed transaction engine on it. Chiller [76] proposes a contention-centric partitioning scheme to improve throughput of RDMA-based transactions. Aurora [32] redesigns phases of transaction execution with RDMA to reduce aborts. Other databases exploit RDMA to support distributed join operations [10, 11]. These above systems can use SHERMAN to index data, or employ HOCL to boost their concurrency performance.

Other distributed database systems assume a NAM (network-attached memory) architecture that logically decouples compute and memory servers and uses RDMA for communication [12, 75, 81]. Specifically, NAM-DB [75] designs a scalable global counter technique to support snapshot isolation efficiently. Compared with NAM architecture, memory disaggregation assumed by SHERMAN is more radical: it decouples compute and memory physically, contributing to an ideal independent scaling of compute and memory. Furthermore, memory disaggregation poses more challenges to database design: near-zero computation power at memory-side and small local memory at compute-side.

Active-Memory [77] leverages RDMA to replicate data in a failure atomic way. It uses ordering property of RDMA to combine undo logging and in-place update in a single network round trip. Inspired by Active-Memory, SHERMAN combines RDMA commands within an index write operation to reduce round trips.

DFI [60] abstracts low-level RDMA verbs and provides a set of flexible interfaces (e.g., multicast, global sequencers) to support data-intensive applications such as OLAP. It will be interesting if DFI exposes on-chip memory of RDMA NICs to applications, to accelerate some interfaces such as global sequencers.

RDMA also accelerates indexing in distributed databases. As discussed in §3, most RDMA-based indexes do not support disaggregated memory. FG [81] is the first RDMA-based tree index that can be deployed on disaggregated memory, since it uses one-sided verbs for all index operations. RACE [82] is an extendible hashing index on disaggregated memory that supports lock-free accesses and remote resizing. SHERMAN rethink how to combine RDMA hardware features and RDMA-friendly software designs to improve tree indexes’ performance on disaggregated memory.

Finally, some researchers design general distributed shared memory (DSM) with RDMA [15, 57, 58, 66], to support database components such as transaction engine. Specifically, GAM [15] provides a unified global memory abstraction and maintains coherence between cache copies via a directory-based protocol. Concordia [66] leverages programmable switches to mitigate cache coherence overhead. Hotpot [57] and TH-DPMS [58] support data durability by using persistent memory. Index cache in SHERMAN exploits the structure of B+Tree to invalidate stale cached entries lazily without any coherence protocols.

6.2 Memory Disaggregation

Memory disaggregation is not a new idea: Lim et al. [42] proposed it more than a decade ago, to attack the problem of a growing imbalance in compute-to-memory-capacity ratio. Recently, memory disaggregation regains attention for two reasons. First, large-scale companies report the low memory utilization in datacenters [29, 55, 61]. Second, high-speed RDMA network makes performance of remote accesses close to that of local accesses. Gao et al. [24] find that, under a memory disaggregation architecture, 40-100Gbps network bandwidth and 3-5µs network latency can maintain application-level performance.

Many recent academic efforts have been devoted to making memory disaggregation practical. LegoOS [55] designs a distributed operating system to manage disaggregated resources. pBPM [62] explores how to deploy disaggregated persistent memory (PM) in an efficient manner. Rao et al. [51] demonstrate that, for Spark SQL, memory disaggregation is promising with currently available network hardware. Zhang et al. [79] evaluate two production DBMSs, PostgreSQL and MonetDB, on disaggregated memory using TPC-H benchmark; they find that in several scenarios, memory disaggregation can boost performance of databases. LegoBase [80] and PolarDB Serverless [17] co-design database and memory disaggregation, achieving faster failure recovery speed than traditional architectures. SHERMAN focuses on building a fast B+Tree index on disaggregated memory.

Industry is proposing memory disaggregation hardware. HPE’s “The Machine” [3, 36] connects a set of SoCs to a shared memory pool via photonic network. IBM’s ThymesisFlow [49] leverages OpenCAPI [4] to enable CPUs directly access remote disaggregated memory without software involvement. VMware uses cache coherence mechanisms to track applications’ memory accesses, reducing data amplification of disaggregated memory [16].

7 Conclusion

We proposed and evaluated SHERMAN, an RDMA-based B+Tree index on disaggregated memory. SHERMAN introduces a set of techniques to boost write performance and outperforms existing solutions. We believe SHERMAN demonstrates that combining RDMA hardware features and RDMA-friendly software designs can enable a high-performance index on disaggregated memory. SHERMAN is open-source at: https://github.com/thustorage/Sherman.

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