Exploiting the DRAM Microarchitecture to Increase Memory-Level Parallelism

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This paper summarizes the idea of Subarray-Level Parallelism (SALP) in DRAM, which was published in ISCA 2012 [66], and examines the work's significance and future potential. Modern DRAMs have multiple banks to serve multiple memory requests in parallel. However, when two requests go to the same bank, they have to be served serially, exacerbating the high latency of off-chip memory. Adding more banks to the system to mitigate this problem incurs high system cost. Our goal in this work is to achieve the benefits of increasing the number of banks with a low-cost approach. To this end, we propose three new mechanisms, SALP-1, SALP-2, and MASA (Multitude of Activated Subarrays), to reduce the serialization of different requests that go to the same bank. The key observation exploited by our mechanisms is that a modern DRAM bank is implemented as a collection of subarrays that operate largely independently while sharing few global peripheral structures.

Our three proposed mechanisms mitigate the negative impact of bank serialization by overlapping different components of the bank access latencies of multiple requests that go to different subarrays within the same bank. SALP-1 requires no changes to the existing DRAM structure, and needs to only reinterpret some of the existing DRAM timing parameters. SALP-2 and MASA require only modest changes (≤0.15% area overhead) to the DRAM peripheral structures, which are much less design constrained than the DRAM core. Our evaluations show that SALP-1, SALP-2 and MASA significantly improve performance for both single-core systems (7%/13%/17%) and multi-core systems (15%/16%/20%), averaged across a wide range of workloads. We also demonstrate that our mechanisms can be combined with application-aware memory request scheduling in multicore systems to further improve performance and fairness.

Our proposed technique has enabled significant research in the use of subarrays for various purposes (e.g., [15, 16, 21, 37, 76, 78, 84, 87, 125, 129, 130, 135, 156, 159]). SALP has also been described and evaluated by a recent work by Samsung and Intel [54] as a promising mechanism to tolerate long write latencies that are a result of aggressive DRAM technology scaling.

1. **Introduction**

To be able to serve multiple memory requests in parallel, modern DRAM chips employ multiple banks that can be accessed independently, providing bank level parallelism. Unfortunately, if two memory requests go to the same bank, they have to be served one after another. This is called a bank conflict. In the worst case, bank conflicts may delay a memory request by hundreds or even thousands of nanoseconds [16, 37, 66, 129]. In particular, bank conflicts cause three specific problems that degrade the access latency, bandwidth utilization, and energy efficiency of the main memory subsystem:

1. **Serialization.** Bank conflicts serialize requests that could potentially have been served in parallel. Such serialization exacerbates the already large latency of a memory access, and may cause processor cores to stall for much longer.

2. **Write Recovery.** A request scheduled after a write request to the same bank experiences an extra delay called the write recovery penalty, which is an additional time required to safely store new data in the cells. This write recovery latency further aggravates the impact of serialization.

3. **Row Buffer Thrashing.** Each bank has a row buffer that caches the last accessed row. A request that hits in the row buffer is much cheaper in terms of both latency and energy than a request that misses in the row buffer. However, bank conflicts between requests that access different rows lead to costly row buffer misses.

A naive solution to bank conflicts is to increase the number of banks. Unfortunately, as we discuss in Section 1 of our ISCA 2012 paper [66], simply adding more banks to the memory subsystem comes at significantly high costs or reduced performance regardless of the way it is done: more banks per chip, more ranks per channel, or more channels [17].

The goal in our ISCA 2012 paper [66] is to mitigate such detrimental effects of bank conflicts in a cost-effective manner. Toward that end, we make two key observations that lead to our proposed solutions.

**Observation 1.** A modern DRAM bank is not implemented as a monolithic component equipped with only a single row buffer. Implementing a DRAM bank in such a way requires very long internal wires (called bitlines) to connect the row buffer to all the rows in the bank, which can significantly increase the access latency. Instead, as Figure 1 shows, a bank consists of multiple subarrays, each with its own local row buffer. Subarrays within a bank share two important global structures: i) a global row address decoder, and ii) a global row buffer.
Observation 2. The latency of a bank access predominantly consists of three major components: i) loading a row into the local row buffer (activation), ii) accessing the data from the local row buffer (read or write), and iii) clearing the local row buffer (precharging) [14, 37, 38, 66, 76, 77, 78]. In existing DRAM banks, all three operations must be completed for one request before serving another request to a different row, even if the two rows reside in different subarrays. However, this does not need to be the case for two reasons. First, activation and precharging are mostly local to each subarray, which enables the opportunity to overlap these operations when they are to different subarrays. Second, if we reduce the sharing of the global structures among subarrays, we can parallelize the concurrent activation of different subarrays. Doing so would allow us to exploit the existence of multiple local row buffers across the subarrays, enabling more than just a single row to be cached for each bank and thereby increasing the row buffer hit rate.

2. Subarray-Level Parallelism

Subarray-Oblivious Baseline. Let us consider the baseline example shown in Figure 2 which presents a timeline of four memory requests being served at the same bank in a subarray-oblivious manner. This example highlights the three key problems that we discussed in Section 1. First, requests are completely serialized, even though they are to different subarrays. Second, although the write-recovery penalty is local to a subarray, it delays a subsequent request to a different subarray. Third, a request to one subarray unnecessarily evicts (i.e., precharges) the other subarray’s local row buffer, which must be reloaded (i.e., activated) when a future request accesses the evicted row. In this section, we describe how SALP-1, SALP-2 and MASA can take an advantage of the DRAM bank organization to enable parallel DRAM operations in a cost-effective manner.

2.1. SALP-1: Subarray-Level-Parallelism-1

We observe that precharging and activation are mostly local to a subarray. Based on this observation, we propose SALP-1, which overlaps the precharging of one subarray with the activation of another subarray. In contrast, existing systems always serialize precharging and activation to the same bank, conservatively provisioning for when they are to the same subarray. SALP-1 requires no modifications to existing DRAM structure. It only requires reinterpretation of an existing timing constraint (tRP) and, potentially, the addition of a new timing constraint (which we describe in Section 5.1 of our ISCA 2012 paper [66]). Figure 3 (top) shows the timeline of the same four requests from Figure 2 when we use SALP-1 instead of our Baseline. As the timeline shows, overlapping the precharge operation reduces the overall time needed to complete the four requests.

2.2. SALP-2: Subarray-Level-Parallelism-2

While SALP-1 pipelines the precharging and activation of different subarrays, the relative ordering between the two commands is still preserved. This is because existing DRAM banks do not allow two subarrays to be activated at the same time. As a result, the write-recovery latency of an activated subarray delays not only a PRECHARGE to itself, but also a subsequent ACTIVATE to another subarray. Based on the observation that the write-recovery latency is also local to a subarray, we propose SALP-2. SALP-2 issues the ACTIVATE to another subarray before the PRECHARGE to the currently-activated subarray. As a result, SALP-2 can overlap the write recovery of the currently-activated subarray with the activation of another subarray, further reducing the service time compared to SALP-1 (as shown in the middle timeline of Figure 3).

However, as highlighted in the figure, SALP-2 requires two subarrays to remain activated at the same time. This is not possible in existing DRAM banks as the global row-address latch, which determines the wordline in the bank that is raised, is shared by all of the subarrays. Section 5.2 of our ISCA 2012 paper [66] discusses how to enable SALP-2 by eliminating this sharing. The key idea is to push the global address latch to each subarray, thereby creating local address latches, one per subarray.

2.3. MASA: Multitude of Activated Subarrays

Although SALP-2 allows two subarrays within a bank to be activated, it requires the controller to precharge one of them before issuing a column command (e.g., READ) to the bank. This is because when a bank receives a column command, all activated subarrays in the bank will connect their local row buffers to the global bitlines. If more than one subarray is activated, this will result in a short circuit. As a result, SALP-2 cannot allow multiple subarrays to concurrently remain activated and serve column commands.

To solve this, we propose MASA, whose key idea is to allow multiple subarrays to be activated at the same time, while allowing the memory controller to designate exactly one of the activated subarrays to drive the global bitlines during the next column command. MASA has two advantages over SALP-2. First, MASA overlaps the activation of different subarrays within a bank. Just before issuing a column command to any of the activated subarrays, the memory controller designates one particular subarray whose row buffer should
Figure 2: Timeline of four requests to two different rows in the same bank. Adapted from [66].

Figure 3: Timeline of four requests to two different rows in the same bank but different subarrays, using our mechanisms to exploit subarray-level parallelism. Adapted from [66].

serve the column command. Second, MASA eliminates extra ACTIVATEs to the same row, thereby mitigating row buffer thrashing. This is because the local row buffers of multiple subarrays can remain activated at the same time without experiencing collisions on the global bitlines. As a result, MASA further improves performance compared to SALP-2, as shown in the bottom timeline of Figure 3.

MASA: Overhead. To designate one of the multiple activated subarrays, the controller needs a new command, SA_SEL (subarray-select). In addition to the changes required by SALP-2, MASA requires a single-bit latch per subarray to denote whether a subarray is designated or not. According to our detailed circuit-level analysis, MASA increases the DRAM die-size by only 0.15\% (due to extra latches) and the static power consumption by only ~1\% (each additional activated subarray consumes 0.56 mW). Also, the memory controller needs less than 256 bytes to track the status of subarrays across all DRAM banks. We discuss a detailed implementation of MASA, along with its overhead, in Section 5.3 of our ISCA 2012 paper [66].

3. Experimental Methodology

We evaluate our three mechanisms for subarray-level parallelism using Ramulator [62, 124], an open-source cycle-accurate DRAM simulator that we developed which accurately models DRAM subarrays. We use Ramulator as part of a cycle-level in-house x86 multi-core simulator, whose frontend is based on Pin [85]. We calculate DRAM dynamic energy consumption by associating an energy cost with each DRAM command, derived using Micron’s DDR3 DRAM tool [93], Rambus’ DRAM power model [123], and previously published data [150].

We evaluate SALP-1, SALP-2, and MASA on a wide variety of workloads [39, 41, 89, 146] and system configurations [45, 46, 134, 143]. The results shown in Section 4 are based on the conservative assumption that a DRAM bank exposes only 8 subarrays to be exploited by our subarray-level parallelism mechanisms, whereas in practice the number of subarrays in current DRAM banks is typically much higher (~64). Section 9.2 of our ISCA 2012 paper [66] shows that the performance improvement of our three mechanisms over a subarray-oblivious baseline increases with a greater number of subarrays.

For our full methodology, we refer the reader to Section 8 of our ISCA 2012 paper [66].

4. Evaluation

Figure 4 shows the performance improvement of SALP-1, SALP-2, and MASA on a system with 8 subarrays-per-bank over a subarray-oblivious baseline. The figure also shows the performance improvement of an “Ideal” scheme which is the subarray-oblivious baseline with 8 times as many banks (this represents a system where all subarrays are fully independent). The benchmarks are sorted along the x-axis by increasing memory intensity. We make two observations from the figure. First, SALP-1, SALP-2, and MASA consis-
tently perform better than the baseline for all benchmarks. On average, they improve the average performance by 6.6%, 13.4%, and 16.7%, respectively. Second, MASA captures most of the benefits of "Ideal," which improves performance by 19.6% compared to baseline.

The difference in performance improvement across benchmarks can be explained by a combination of three factors related to the benchmarks’ individual memory access behavior. First, subarray-level parallelism in general is most beneficial for memory-intensive benchmarks that frequently access memory (e.g., the benchmarks located towards the right of Figure 4). By increasing the memory throughput for such applications, subarray-level parallelism significantly alleviates their memory bottleneck. The average memory intensity of the applications that gain >5% performance with SALP-1 is 18.4 MPKI (last-level cache misses per kilo-instruction), compared to 1.14 MPKI for the other applications.

Second, the advantage of SALP-2 is large for applications that are write-intensive (i.e., those with the most write misses per kilo-instruction, or WMPKI). For such applications, SALP-2 can overlap the long write-recovery latency with the activation of a subsequent access. In Figure 4, the three applications that improve more than 38% with SALP-2 are among both the most memory-intensive (>25 MPKI) and the most write-intensive (>15 WMPKI).

Third, MASA is beneficial for applications that experience frequent bank conflicts. For such applications, MASA parallelizes accesses to different subarrays by concurrently activating multiple subarrays (ACTIVATE) and allowing the application to switch between the activated subarrays at low cost (SA_SEL). Therefore, the subarray-level parallelism offered by MASA can be gauged by the SA_SEL-to-ACTIVATE ratio. For the nine applications that benefit more than 30% from MASA, on average, one SA_SEL was issued for every two ACTIVATEs, compared to one-in-seventeen for all other applications. For a few benchmarks, MASA performs slightly worse than SALP-2. This is because the baseline scheduling algorithm used with MASA tries to overlap as many ACTIVATEs as possible, and in the process inadvertently delays the column command of the most critical request. This delay to the most critical request slightly degrades performance for these benchmarks.

5. Related Work
To our knowledge, our ISCA 2012 paper [66] is the first to exploit the existence of subarrays within a DRAM bank and enable their parallel operation in a cost-effective manner. We propose three schemes that exploit the existence of subarrays within DRAM banks to mitigate the negative effects of bank conflicts. Related works propose increasing the performance and energy-efficiency of DRAM through approaches such as DRAM module reorganization, changes to DRAM chip design, and memory controller optimizations. We briefly discuss these works here.

**DRAM Module Reorganization.** Several prior works partition a DRAM rank and the DRAM data bus into multiple rank subsets, each of which can be operated independently. While these techniques increase parallelism, they reduce the width of the data bus of each rank subset, leading to longer latencies to transfer a 64 byte cache line. Furthermore, having many rank subsets requires a correspondingly large number of DRAM chips to compose a DRAM rank, an assumption that does not hold in mobile DRAM systems where a rank may consist of as few as two chips [95]. Unlike these works, our mechanisms increase memory-level parallelism without increasing memory latency or the number of DRAM chips.

**Changes to DRAM Design.** Cached DRAM organizations, which have been widely proposed, augment DRAM chips with an additional SRAM cache that can store recently accessed data in order to reduce memory access latency. However, these proposals increase the chip area and design complexity of DRAM designs. Furthermore, cached DRAM provides parallelism only when accesses hit in the SRAM cache, while serializing cache misses that access the same DRAM bank. Our schemes parallelize DRAM bank accesses while incurring significantly lower area and logic complexity.

Fujitsu’s FCRAM [126] and Micron’s RLDRAM [57] propose to implement shorter local bitlines (i.e., fewer cells per bitline) that are quickly drivable due to their lower capacitance in order to reduce DRAM latency. However, this significantly increases the DRAM die size (30-40% for FCRAM, 40-80% for RLDRAM) because the large area of sense-amplifiers
is amortized over a smaller number of cells. Hybrid memory systems can reduce the die size overhead by using a small amount of FCRAM [126] or RLDDRAM [57] in conjunction with conventional DRAM and managing which subset of the data resides in FCRAM/RLDRAM at any given time to lower the latency of memory accesses.

A patent by Qimonda [113] proposes the high-level notion of separately addressable sub-banks, but lacks concrete mechanisms for exploiting the independence between sub-banks. Yamauchi et al. propose the Hierarchical Multi-Bank (HMB) [154], which parallelizes accesses to different subarrays in a fine-grained manner. However, this scheme adds complex logic to all subarrays.

Udipi et al. [147] propose two techniques (SBA and SSA) to lower DRAM power. In SBA, global wordlines are segmented and controlled separately so that tiles in the horizontal direction are not activated in lockstep, but selectively. However, this increases DRAM chip area by 12-100% [147]. SSA combines SBA with chip-granularity rank-subsetting to achieve even higher energy savings. Both SBA and SSA increase DRAM latency, more significantly so for SSA (due to rank-subsetting).

When transitioning from a write request to serving a read request, and vice versa [18, 73, 137], a DRAM chip experiences bubbles in the data bus, called the bus-turnaround penalty (tWR and tRTW). During the bus turnaround penalty, Chatterjee et al. [18] propose to internally “prefetch” data for subsequent read requests into extra registers that are added to the DRAM chip.

Other works propose new DRAM designs that are capable of reducing memory latency of conventional DRAM [3, 14, 16, 19, 36, 40, 44, 56, 62, 75, 76, 78, 79, 86, 94, 112, 113, 126, 133, 135, 151, 164] as well as non-volatile memory [68, 69, 70, 71, 90, 91, 121, 122, 155]. Previous works on bulk data transfer [13, 16, 33, 34, 47, 51, 53, 84, 127, 129, 158, 163] and in-memory computation [1, 2, 5, 9, 11, 12, 23, 26, 27, 28, 29, 30, 32, 35, 42, 43, 55, 60, 67, 88, 114, 116, 117, 119, 128, 130, 131, 132, 136, 144, 157] can be used to improve DRAM bandwidth utilization and lower the number of costly data movements between CPU cores and DRAM. All these works can benefit from SALP as the underlying memory substrate.

**Memory Controller Optimizations.** To reduce bank conflicts and increase row buffer locality, Zhang et al. [160] propose to randomize the bank address of memory requests by XOR hashing. Sudan et al. [142] propose to improve row buffer locality by placing frequently-referenced data from different rows together in the same row buffer. Both proposals can be combined with our mechanisms to further improve parallelism and row buffer locality.

Prior works propose memory scheduling algorithms for CPUs (e.g., [24, 31, 48, 58, 64, 65, 72, 73, 74, 82, 96, 97, 98, 99, 106, 107, 111, 137, 138, 139, 140, 141, 153, 162]), GPUs (e.g., [7, 8, 20, 50, 52]), and other systems (e.g., [148, 149, 162]) that prioritize certain favorable requests in the memory controller to improve system performance and/or fairness. Subarrays expose more parallelism to the memory controller, increasing the controller’s flexibility to schedule requests. Our subarray-level parallelism mechanisms can be combined with many of these schedulers to provide increased performance benefits. Enabling higher benefit from SALP by designing SALP-aware memory scheduling algorithms is a promising open research topic.

### 6. Significance and Long-Term Impact

We believe SALP will have long-term impact because: i) it tackles a critical problem, bank conflicts and memory parallelism, whose importance will increase in the future; and ii) the memory substrate it provides can further be leveraged to enable other novel optimizations in the memory subsystem. In fact, as Section 6.2 shows, there has been a significant amount of work that built upon our ISCA 2012 paper in the past six years.

#### 6.1. Trends and Opportunities in Favor of SALP

**Worsening Bank Conflicts.** Future many-core systems with large numbers of cores and accelerators (e.g., bandwidth-hungry GPUs) will exert increasingly larger amount of pressure on the memory subsystem. On the other hand, naively adding more DRAM banks is difficult without incurring high costs, high energy or reduced performance. Therefore, as
more and more memory requests contend to access a limited number of banks, bank conflicts will occur with increasing likelihood and severity. SALP is a cost-effective mechanism to alleviate the bank conflict problem by exploiting the existing subarrays in DRAM at low cost.

**Challenges in DRAM Scaling.** DRAM process scaling is becoming more difficult due to increased manufacturing complexity/cost and reduced cell reliability. As a result, it is critical to examine alternative ways of improving memory performance while still maintaining low cost. SALP is a new cost-effective DRAM design whose advantages are mostly orthogonal to the advantages of DRAM process scaling. Therefore, SALP can further improve the performance and the energy-efficiency of future DRAM. In fact, a recent industry proposal to enhance the DDR standard incorporates one of our SALP mechanisms. This work by Samsung and Intel quantitatively shows that SALP is an effective mechanism to tolerate increasing write latencies in DRAM, corroborating the results in our ISCA 2012 paper on SALP-2.

**A Building Block for New Optimizations.** SALP enables new DRAM optimizations that were not possible before. We discuss three potential examples. First, exploiting subarray-level parallelism can potentially mitigate DRAM unavailability during refresh by parallelizing refreshes in one subarray with accesses to another subarray within the same bank. Work by Chang et al., which builds on our ISCA 2012 paper, shows that such parallelization can eliminate most of the performance overhead of refresh. Second, subarrays provide an additional degree of freedom in mapping the physical address space onto different levels of the DRAM hierarchy (channels, ranks, banks, subarrays, rows, columns). Thus, they enable more flexibility in performance and energy optimization via data mapping. Third, DRAM can be divided among different applications (to provide quality-of-service) at the finer-grained partitions of subarrays that are less vulnerable to capacity and bandwidth fragmentation. As we discuss, some research has explored these approaches (also see Section 6.2). We expect even more future research will tap into these and other opportunities that can use our proposed SALP substrate as a building block for other optimizations.

**Widely Applicable Substrate.** SALP is a general-purpose substrate that is also applicable to embedded DRAM (eDRAM) and 3D die-stacked DRAM (3D-DRAM), both of which consist of subarrays. For example, eDRAM is known to be vulnerable to the write-recovery penalty, since it is typically used as the last-level cache and thus exposed to higher amounts of write traffic. SALP can increase the availability of eDRAM by hiding the write-recovery penalty. In addition, SALP may be applied to future emerging memory technologies as long as their banks are organized hierarchically, similar to how a DRAM bank consists of subarrays.

**New Research Opportunities.** SALP creates new opportunities for exploiting and enhancing the parallelism and the locality of the memory subsystem.

- **Enhancing Memory-Level Parallelism.** To tolerate the long latency of DRAM, computer architects often design mechanisms that perform multiple memory requests in a concurrent manner. Such efforts may become ineffective when requests access the same DRAM bank and, as a consequence, are not actually served in parallel. SALP, on the other hand, parallelizes requests to different subarrays within the same bank. In this regard, we believe SALP not only enhances previous approaches to memory-level parallelism, but also creates opportunities for developing new techniques that preserve memory-level parallelism in a subarray-aware manner.

- **Enhancing Memory Locality.** Memory access patterns that exhibit high locality benefit greatly from a DRAM bank’s row buffer where the last accessed row is cached (4–8kB). While a DRAM bank has multiple row buffers across multiple subarrays, an existing DRAM system exposes only one row buffer at a time in a bank and, as a result, is prone to row buffer thrashing. In contrast, SALP allows a DRAM bank to utilize multiple row buffers concurrently. This enables the opportunity for new techniques that can take advantage of the multiple row buffers, whether they be for streaming/strided accesses (demand or prefetch), vector processing, or GPUs.

**6.2. Works Building on SALP**

The introduction of the notion of subarrays and their microarchitecture has enabled the use of the subarrays in many works. These include RowClone, TL-DRAM, DSARP, DIVA-DRAM, LISA, ChargeCache, Multiple Clone Row DRAM, and other works on improving DRAM locality of the memory subsystem.

**7. Conclusion**

Our ISCA 2012 paper introduces three new mechanisms that exploit the existence of subarrays within a DRAM bank to mitigate the performance impact of bank conflicts. Our mechanisms are built on the key observation that subarrays within a DRAM bank operate largely independently and have their own row buffers. Hence, the latencies of accesses to different subarrays within the same bank can potentially be overlapped to a large degree. Our three mechanisms take
advantage of this fact and progressively increase the independence of operation of subarrays by making small modifications to the DRAM chip. Our most sophisticated scheme, MASA, enables i) multiple subarrays to be accessed in parallel, and ii) multiple row buffers to remain activated at the same time in different subarrays, thereby improving both memory-level parallelism and row buffer locality. We show that our schemes significantly improve system performance on both single-core and multi-core systems on a variety of workloads while incurring little (<0.15%) or no area overhead in the DRAM chip. Our techniques can also improve memory energy efficiency.

We conclude that exploiting subarray-level parallelism in a DRAM bank can be a promising and cost-effective method for overcoming the negative effects of DRAM bank conflicts, without paying the large cost of increasing the number of banks in the DRAM system. Significant recent work has built upon our ISCA 2012 paper, and we expect many other new works can exploit the new substrate we have enabled to achieve even bigger goals and higher benefits.

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