Conversion of Logic Gates in Netlists for Rapid Single Flux Quantum Circuits Utilizing Confluence of Pulses

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Abstract: A conversion method of a netlist consisting of conventional logic gates for superconducting rapid single flux quantum (RSFQ) circuit realization is proposed. The method detects OR gates which can be replaced with confluence buffers (CBs) which converge their input pulses into their outputs. The detection problem of replaceable OR gates is treated as a SAT problem. By replacing OR gates with CBs, wiring for clocking those OR gates are eliminated and the number of active devices known as Josephson junctions is reduced.

Keywords: rapid single flux quantum circuits, logic circuits, pulse logic

1. Introduction

Superconducting logic devices have been studied for high-speed and low-power information processing [1]. Recently, conventional CMOS circuits are suffering from difficulties in improving performance, and superconducting rapid single flux quantum (RSFQ) circuit technology [2] is attracting attention [3]. RSFQ circuits work at high frequency up to 100 GHz [4], and simple microprocessors have been demonstrated [5].

In RSFQ circuits, voltage pulses are used to represent logic values, i.e., pulse logic is used, and each basic logic gate works with a clock signal. RSFQ circuits have been designed mainly by hand because of incompatibility with conventional CMOS circuits and tight timing constraints. Recently, automation of layout design has been studied [6], [7], [8]. Because generation of logic circuits exploiting pulse logic has not been studied enough, netlists composed of basic logic gates are considered as the design entry in those studies and advantages of pulse logic are not exploited. In this paper, we propose a conversion method of netlists for realizing compact RSFQ circuits exploiting pulse logic.

Converging pulses with a special gate named confluence buffer (CB) is a useful technique in RSFQ circuit design. In logic design of experienced circuit designers, CBs are used extensively to realize a circuit in compact area. Especially, if an OR gate never receive plural “1”, it can be replaced with a CB. A CB is smaller than an OR gate. Wiring for clock distribution and the depth of circuits can be reduced. Wiring in RSFQ circuits occupies large area because it is realized by a transmission line composed of active devices known as Josephson junctions (JJs) or by a passive transmission line with a driver and a receiver. Although utilizing CBs instead of OR gates is effective, CBs are not generated directly by existing logic synthesis tools.

In this paper, we show a conversion method of a netlist consisting of conventional logic gates for RSFQ circuit realization. The method replaces OR gates with CBs by examining possibility of replacement for each OR gate in the given netlist. We convert the examination of an OR gate as a SAT problem. We show experimental results, and show many OR gates can be replaced with CBs.

2. RSFQ Circuits

In RSFQ circuits, voltage pulses are used to represent logic values, and transmitted on signal lines. Each basic logic gate has a clock input and works synchronized with clock pulses. As an example, the symbol of RSFQ OR gate is shown in Fig. 1(a). The value of the gate input is evaluated with clock pulses as shown in the figure. When a pulse arrives at a gate input during an interval between adjacent clock pulses, the input value corresponding to the interval is evaluated as “1”. If no pulse arrives during the interval, the input value is evaluated as “0”. It is prohibited to feed plural pulses into a data input of a basic logic gate during the interval. The output of a gate is synchronized with the clock pulse.

Other than basic logic gates such as AND, OR, and XOR gates, CBs are used to converge pulses as shown in Fig. 1(b). A CB has two data inputs and one output. Pulses arrive at inputs of a CB are converged at its output.

As an example, we show a design of a full adder. Figure 2(b) is the design derived directly from the design in Fig. 2(a) consisting of conventional logic gates. Each RSFQ logic gate works as if it has a flip-flop, and a circuit is designed to be pipelined at each gate. In the figure, DFFs are inserted to maintain pipeline stages, and large dots in the crosspoints of lines represent splitters which distribute pulses and are composed of JJs.
3. Conversion of Netlists by Replacing OR Gates Considering Confluence of Pulses

We can obtain compact RSFQ logic circuits by utilizing CBs. When plural inputs of an OR gate never receive pulses simultaneously for any circuit input, we can use a CB in place of an OR gate. For example, both inputs of OR gate $g_4$ in Fig. 2(a) never be “1” simultaneously. Thus, we can replace the OR gate in Fig. 2(b) with a CB as shown in Fig. 2(c). Depth of the circuit in Fig. 2(c) is reduced. The number of DFFs and wiring for clock distribution including splitters are reduced from Fig. 2(b). In the cell library for AIST ADP2 process [9], a 2-input CB cell is realized with 7 JJs while a 2-input OR cell is realized with 12 JJs. Therefore, this conversion reduces the number of JJs.

The conversion method which we propose examines each OR gate separately whether it can be replaced with a CB. To examine an OR gate, we insert an AND gate whose inputs are the same as the OR gate, and we inspect whether the AND gate can output “1”. If the AND gate never outputs “1” for any circuit input, the OR gate can be replaced with a CB. In this paper, we treat the examination as the OR gate, and we insert an AND gate whose inputs are the same as the OR gate, and we inspect whether the AND gate can output “1”. If the AND gate never outputs “1” for any circuit input, we can use a CB in place of an OR gate.

As an example, we examine gate $g_4$ in Fig. 2. AND gate $g_5$ is inserted for the examination as shown in Fig. 2(a’). A CNF formula can be prepared as follows:

$$(i_1 + i_2 + \overline{n_0}) \cdot (i_1 + \overline{i_2} + n_0) \cdot (i_1 + i_2 + n_0) \cdot (i_1 + \overline{i_2} + \overline{n_0}) \cdot (i_1 + \overline{i_2} + n_1) \cdot (i_1 + n_1) \cdot (i_2 + n_1) \cdot (\overline{i_0} + n_0 + n_3) \cdot (i_0 + n_3) \cdot (n_0 + n_3) \cdot (n_1 + n_3 + n_5) \cdot (n_1 + n_5) \cdot (n_3 + n_5) \cdot n_5.$$  

Lines 1-4 of the formula describe relations of inputs and outputs of gates $g_0$, $g_1$, $g_3$, and $g_5$ on the paths from the circuit inputs to the output of the appended AND gate. Lines 1, 2, 3, and 4 correspond to gates $g_0$, $g_1$, $g_3$, and $g_5$, respectively. The last line constrains the output of the AND gate as “1”. Once the above formula is fed to SAT solver, it turns out to be unsatisfiable. Thus the OR gate can be replaced with a CB in RSFQ circuit realization.

4. Experimental Results

We have evaluated the method using netlists synthesized from Verilog-HDL descriptions. We have prepared netlists consisting of AND, OR, XOR, and NOT gates by employing Synopsys Design Compiler. For each OR gate, we examined whether it can be replaced with a CB by the proposed method. We used minisat [11] as the SAT solver and used a computer with Ryzen 7 2700X processor. We show the results in Table 1. The 32-bit adder and the 32-bit ALU were described with arithmetic operators of Verilog-HDL. The ALU was described to carry out one of functions such as addition, multiplication, and bit-wise logic operations. The address decoder is a part of IWLS 2005 benchmark suite.

The last column of the table represents total runtime of the SAT solver. The examinations for OR gates were carried out in short time. The second, third, and fifth columns represent the number of gates, the number of OR gates in the source netlists, and the number of OR gates after the replacement by the method. The results demonstrate up to 25% of gates can be replaced with CBs, and depth from circuit inputs to circuit outputs was reduced in two circuits. By the method, it will be possible to realize logic circuits in smaller area than realizing logic circuits from synthesized results directly.

5. Concluding Remarks

We have proposed a conversion method of a netlist consisting of conventional logic gates for RSFQ circuit realization considering confluence of pulses. By examining each OR gate in a netlist, we detect OR gates which can be replaced with CBs.
In this paper, we treat the examination as a SAT problem. Another observation is that the problem can be viewed as a test generation problem for stuck-at-0 fault at the output of the appended AND gate as described above. To investigate various techniques in automatic test pattern generation for the problem is the future work.

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