Front-end-Electronics for the SiPM-readout gaseous TPC for neutrinoless double beta decay search

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Abstract

We have developed a dedicated front-end-electronics board for a high-pressure xenon gas time projection chamber for a neutrinoless double-beta decay search. The ionization signal is readout by detecting electroluminescence photons with SiPM’s. The board readout the signal from 56 SiPM’s through the DC-coupling and record the waveforms at 5 MS/s with a wide dynamic range up to 7,000 photo/200 ns. The SiPM bias voltages are provided by the board and can be adjusted for each SiPM. In order to calibrate and monitor the SiPM gain, additional auxiliary ADC measures 1 photon-equivalent dark current. The obtained performance satisfies the requirement for a neutrinoless double-beta decay search.

1 Introduction

Neutrinoless double beta decay (0νββ) is a phenomenon in which two beta-decays simultaneously happen inside a nucleus without emitting neutrinos. It happens only in the case neutrino has Majorana-type mass for some nuclei. Hence, the observation of 0νββ would be a direct proof of the Majorana nature of neutrinos, but so far it has not been observed and only lower limits on the life have been obtained. The KamLAND-Zen experiment reported the lower limit on the half life of 0νββ as $T_{1/2}^{0ν} > 1.67 \times 10^{26}$ yr at 90% C.L. [1]. The most relevant feature of 0νββ is monochromaticity of the energy sum of the two emitted β-rays. The track topology has also characteristic feature: two beta-rays are emitted from a nucleus. Therefore, in order to conduct the sensitive search for 0νββ with good signal and background separation, detectors having high energy resolution and track topology identification has been desired.

We are developing a high-pressure $^{136}$Xe gaseous TPC (time projection chamber) detector, AXEL. Thanks to the pixelized readout utilizing the electroluminescence process, called as ELCC (Electroluminescence Light Collection Cell) [2], the AXEL detector has good energy resolution and tracking capability. The schematic view of AXEL is shown in Fig. 1. Ionization electrons generated by β-rays are drifted to ELCC and generate electroluminescence (EL) photons by a few kV/cm/bar electric field applied in each cell. As the EL process is a linear process [3], ionization electrons can be converted to the photons with small fluctuation. EL photons are detected...
by a SiPM (Hamamatsu MPPC, SS13370) in each cell. Event track topologies can be reconstructed from the hit pattern and the hit timing of ELCC. The target energy resolution is $\Delta E = 0.5\%$ (FWHM) at the Q-value (2,458 keV) of $^{136}$Xe.

Currently, we are constructing a 180-L size prototype detector to demonstrate the performance at Q-value and to establish the technique to construct larger-size detectors. The number of channels of this detector is 1,512. To operate and readout the waveform of more than 1,500 SiPM’s, we have developed a dedicated front-end electronics board, AxFEB (AXEL front-end electronics board). In this paper, we present the design and performance of the AxFEB.

2 Design of AxFEB

2.1 Requirements to the AxFEB

To evaluate the requirement, $0\nu\beta\beta$ events were simulated by Geant4 and Garfield++ with responses of ionization electron drift, EL process, and MPPC. Fig. 2 shows a distribution of signal time width for each channel obtained by the simulation. The required record length is 150 µs. The sampling rate required to reconstruct the energy with sufficient resolution was estimated to be 2 MS/s. However, it turned out that 5 MS/s is necessary to correct the non-linearity of the MPPC. Typical electron drift velocity in xenon gas is ~ 0.1 cm/µs. So 5 MHz corresponds to 0.2 mm in z position sampling, which is smaller than the longitudinal diffusion. Fig. 3 shows distribution of photon rate for each channel, that is, number of photons detected by the MPPC in each 1 µs. The photon rate reaches 35,000 photons/µs, but most of the time, the photon rate is less than 2,000 photons/µs. With detailed simulation, it was found that required dynamic range is 4 – 7,000 photons/200 ns at 5 MHz sampling to obtain the target energy resolution.

The gain of SiPM is given as following,

$$ g \equiv \frac{Q_{1 \text{p.e.}}}{q_e} = \frac{C(V_{\text{bias}} - V_{\text{break}})}{q_e} = C \cdot \frac{V_{\text{over}}}{q_e}, $$(1)

where, $Q_{1 \text{p.e.}}$ is the charge of the 1 photon-equivalent (p.e.) signal, $q_e$ - elementary charge, $C$ capacitance of MPPC, $V_{\text{bias}}$ applied voltage to the MPPC, and $V_{\text{break}}$ voltage at which APDs (Avalanche Photo Diode) in an MPPC starts causing Geiger discharge. The $V_{\text{over}}$ is called overvoltage, and the MPPC gain is proportional to it. The overvoltage is very small compared to the breakdown voltage, e.g., a typical breakdown voltage of SS13370 is $\approx 55 – 60$ V while $V_{\text{over}} = 3 – 4$ V. Besides, the breakdown voltage varies for each MPPC. Therefore, the front-end board is required to control the bias voltage precisely for each MPPC to get uniform gain for all MPPC’s.

The gain calibration and stability monitoring are done by measuring 1 p.e. signal by dark current. Since the time constant of the 1 p.e. signal is as short as several tens of nanoseconds, it cannot be measured with the 5 MS/s ADC. Therefore another type of ADC with 40 MS/s sampling is added for MPPC calibration. The typical gain of MPPC S13370 is $2.6 \times 10^6$, so 1 p.e. signal corresponds to 0.96 pC. To match the 40 MS/S, 2 V pp, 12 bit ADC whose 1 count corresponds to 0.2 pC, the signal is amplified by 165 times in the analog section before being sent to the ADC for calibration.

In summary, the requirements for the front-end electronics circuit are as follows,

- Dynamic range: 4 – 7,000 photons/200 ns
- Record length: 150 µs
- One p.e. signal measurement for calibration
- Independent bias voltage supply to each MPPC with tens of mV resolution
2.2 Overview of the AxFEB

Fig. 4 depicts the block diagram of AxFEB. One board readout the waveform signal from 56 MPPC’s. The board operates at DC 5 V.

Fine adjustments of bias voltage for each MPPC is realized by using two types of DAC’s: one for common high voltage supply and is connected to the cathode side of MPPC, and the other for fine adjustment for each MPPC and is connected to the anode side of MPPC. Special configuration is adopted for analog signal processing to avoid the AC-coupling readout and is described in Sec. 2.3.

There are two types of ADCs in AxFEB – ADCL and ADCH. ADCL is used for $0\nu\beta\beta$ detection, and ADCH is used for calibration of MPPC by measuring dark current. Since calibration only needs to be done intermittently, one ADCL reads out every 7 channels switched by a multiplexer.

The board calculate the sum of 56 channels ADC values and send it to a general trigger module. The trigger module issues a trigger to each AxFEB according to the sum signal from AxFEBs. Each AxFEB has an IP address and can communicate via the Ethernet with PC’s. The overall control, data processing and communication with other modules and PC’s are managed by a FPGA on the board.

2.3 Analog section

Fig. 5 shows the diagram of the analog section of AxFEB. The analog section has three main roles:

1. Amplify the signal to match the dynamic range of the ADC
2. Shaping the signal to match the ADC sampling rate
3. Apply the bias voltage to each MPPC.

The first-order filter (integration circuit) indicated in Fig. 5 shapes the waveform with
the 17 ns time constant and also amplifies the signal by 5 times. The second-order filter (Sallenkey filter) in Fig. 3 shapes the waveform to the ~400 ns time constant for ADCL. The total gain of the circuit for ADCL is 5. The signal to ADCH is further amplified by 16.5 times by the inverting amplifier circuit in Fig. 5 and two times by a differential amplifier placed in before ADCH. The total gain of the circuit for ADCH is 165. The ADC used for ADCL is LTC2325CUKG-12#PBF which has 2 Vpp and 12 bit dynamic range. The ADC used for ADCH is AD9637BCPZ-40 which has 2 Vpp and 12 bit dynamic range.

The bias voltage is applied by using two types of DAC's. High voltage (∼60 V) is generated by a DAC (LTC2630CSO6-LZ8) and applied to the cathode of all MPPC's, separated by low-pass filters. Then, a DAC (LTC2636CSO6-LZ8) is individually connected to the anode of each MPPC to finely adjust the bias voltage. This scheme has been used for many readout board for SiPM. Since both electrodes are applied to finite voltage, the AC-coupling readout, as shown in Fig. 6 is often used. However, it is not adequate for our usage. The maximum time width of 0νββ signal is 150 µs, and the required time constant of the low-pass filter is 30 ms to suppress the deformation of the signal waveform. Then, the acceptable event rate becomes very low. To realize the DC-coupling readout, we adopted the configuration shown in Fig. 7. The bias voltage is adjusted by the \( V_{\text{ADJ}} \) via a virtual short of the operational amplifier. Then, an offset corresponding to \( V_{\text{ADJ}} \) appears on the output of the operational amplifier. This offset is canceled by connecting the \( V_{\text{ADJ}} \) to the second-stage amplifier via register \( R_p \). When \( R_u/R_{u}' = R_p/R_{p}' \) is satisfied, the offset of the output of the first stage operational amplifier is canceled. An OFFSET DAC to the second operational amplifier controls the baseline dynamically.

### 2.4 Digital section

The ADC chip for ADCL is LTC2325CUKG-12#PBF, whose dynamic range is 2 Vpp and sampling rate is 5 MS/S. By taking account of the gain of the analog section (×5), the maximum signal height of ADCL is about 400 mV. If the gain of MPPC is 2.6 × 10^6, the acceptable number of photons is 4,000 photons/200 µs.

The ADC chip for ADCH is AD9637BCPZ-40. The dynamic range is 2 Vpp, and the sampling rate is 40 MS/s. One ADCH exists for every seven channels, switched by a multiplexer. The maximum signal height of ADCH is about 12 mV.

The AxFeB has a FPGA, Xilinx, and XC7A200T-1FBG484C. It controls DACs (HV supply, bias voltage fine adjustment, offset adjustment) and multiplexer by SPI protocol and ADCs. The ADC values are continuously written to the FIFO (ring buffer) created on the FPGA every clock. When a trigger is issued, data writing is switched to another buffer, and the data in a previous buffer is sent to the PC using SiTCP [6]. The maximum data size for event for one board is about 2 Mbit. To keep a certain margin, we chose the 200T series, which has 13 Mbit memory. The FPGA calculates the sum of 56 channels ADC counts, averages over three samples, and sends it to a general trigger module. The trigger module calculates the total sum of the data sent from AxFeB's and issues a trigger based on the sum value.

AxFeB can be driven by either internal or external clocks. When using several boards at the same time, clocks are supplied from the trigger module. The communication between AxFeB and the trigger module is conducted by LVDS (160 MHz). The ADC sum of 56 channels is converted to a pseudo analog signal by DAC (1 MS/s), the output from a LEMO connector, and can be checked by an oscilloscope.

Data transportation and slow control between AxFeB and PC are performed via Ethernet. Acquired data is transported by TCP protocol, and AxFeB is slow controlled by UDP protocol. In order to perform this communication, we use SiTCP as a technology to connect FPGA and Ethernet. The IP address of AxFeB can be set with an 8 bit DIP switch on the board.
Figure 5: Circuit diagram of the analog part of one channel of the AXELBOAED
Figure 6: Diagram of AC coupling readout

Figure 7: Diagram of the AxFEB DC coupling readout, which corresponds to the operational amplifiers of Fig. 5c, first stage operational amplifiers of Fig. 5d and Fig. 5e).

Figure 8: Photograph of AxFEB

3 Performance Evaluation

3.1 Performances of ADCL

The linearity of ADCL was checked by inputting constant voltage to AxFEB with 1 mV step. Fig. 9 shows the measured ADC value with respect to the input voltage for a certain channel. It was fitted with a quadratic function. The second-order term is about $10^{-5}$ of the first-order term. The non-linearity of ADCL is sufficiently small. We also calculate the gain of the analog section of ADCL for 56 channels. The gain of the analog section was also measured and confirmed that the value is as designed, $\times \sim 5$.

Fig. 10 shows an example of the waveform of one channel obtained by AxFEB. The 180-L size prototype detector is irradiated with a $^{22}$Na source.

3.2 Performance of ADCH

Fig. 11 shows an example waveform acquired by ADCH. The pulses were integrated and the distribution were obtained as shown in Fig. 12. Dark current pulses corresponding to 1 p.e. and 2 p.e. are clearly separated.

Fig. 13 shows the measured MPPC gain as
Figure 11: Example waveform taken by ADCH. Dark current pulses corresponding to 1 p.e. and 2 p.e. are clearly seen.

Figure 12: Dark current pulse integral distribution obtained by ADCH. Peaks corresponding to 1 p.e., 2 p.e., and 3 p.e. are clearly separated. Those between peaks are caused by after pulses of MPPC.

Figure 13: Measured MPPC gain as a function of the bias voltage. The blue points represent the gain when the common bias voltage (BIAS) is changed from 54.9 V to 55.3 V, while $V_{\text{ADJ}}$ is fixed to zero. The green points represent the gain when the $V_{\text{ADJ}}$ is changed with fixing the common bias voltage to 55.3 V. From the result, it was confirmed that the gain can be controlled by the applied voltage expressed by $V_{\text{BIAS}} - V_{\text{ADJ}}$.

The gain of MPPC changes by about 2.5% with 0.1 V bias voltage change. Since the voltage of the DAC can be adjusted in 0.01 V steps, the gain of each MPPC can be adjusted by about 0.25%.

Fig. 14 shows a result of the fine adjustment of the bias voltage for 56-channels of MPPC’s. The gains of individual MPPC’s, were different when only common bias voltage was applied; on the other hand, gains are aligned after fine adjustment was conducted.

4 Summary

We are developing a high-pressure xenon gaseous TPC for searching for neutrinoless double-beta decay. The ionization signal is readout by detecting electroluminescence photons with SiPM’s. A large number of channels have to be readout at 5 MS/s with a wide dynamic range. Currently, we are constructing a 180-L size prototype detector to demonstrate the detector performance at the Q-value and to establish the techniques for larger-size detector. The number of SiPM’s for this detector is 1,512 channels. To operate and readout such many SiPM’s, we have developed a front-end electronics board as AxFEB. The bias voltage to SiPM’s can be adjusted for individual channels. The signal is readout with the DC coupling by canceling the offset caused by bias ad-
justment. To calibrate and monitor the gain of SiPM’s, the board has an additional high gain ADC to measure the dark current. We evaluated the performance of AxFEB and confirmed that it satisfies the requirement.

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