Design of a low-power 12.5Gb/s 1:10 demultiplexer in 0.18μm CMOS*

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Abstract. A low-power 12.5Gb/s 1:10 Demultiplexer (DEMUX) without inductors is designed in 0.18μm CMOS (Complementary metal oxide semiconductor) process. The 1:10 DEMUX includes a high-speed 1:2 DEMUX, two serial low-speed 1:5 DEMUX, a 5 frequency divider and so on. The latch of the high-speed 1:2 DEMUX adopts the CML (Current Mode Logic) structure. The rest of the triggers all use E-TSPC (Extended True Single Phase Clock) structure. In the design of the 5 frequency divider, the logic gate circuit is embedded in flip-flop to improve the work frequency. The post simulated result shows that when the data rate of the input pseudorandom is 12.5Gb/s and the clock frequency is 6.25GHz at a supply voltage of 1.8V, this 1:10 DEMUX can work well and the eye diagram of output data is clear. The output swing is 400mV on an external 50 Ohm load and the total power dissipation is 200mW. The die size is 0.64×0.57mm².

1. Introduction

With the rapid growing demand of information flow need, the conventional parallel interface technique has blocked the improvement of data transmission rate. SerDes, a serial communication technology that was mainly used in optical fiber communication in the past, is slowly replacing parallel communication technology because of high speed, strong anti-interference ability and low cost. It has become the mainstream technology for high-speed I/O interfaces today [1]. For a long time, in SerDes receivers, the design and implementation of the DEMUX which is used to convert single high-speed data stream to multiple low-speed data streams have been an important research direction, and many papers have reported these [1]-[3]. However, through analysis, it is not difficult to find that the operating rate of DEMUX using the 0.18μm CMOS process rarely exceeds 10Gb/s, because the characteristic frequency $f_T$ of this process is only 49GHz. And in past published high-speed DEMUX designs, current mode logic (CML) or improved CML structure were used mostly, which caused a large chip area and high power consumption[4]-[6]. In this paper, the combination of CML and E-TSPC can reduce power consumption and chip area.

DEMUX has three basic structures: string type, parallel type, and tree type. The string structure is simple, but the working rate is low and the power consumption is high. The parallel structure has a high working rate and low power consumption, but it requires a multi-phase clock. Especially for high-order DEMUX systems, the clock circuit is too complex. The tree structure can design the high-speed and low-speed sections separately, so as to obtain the best trade-off between low power consumption and high speed, but it only realizes $2^n$ DEMUX. The 12.5Gb/s 1:10 DEMUX in this
paper does not use the tree structure because it is not \(2^n\), but uses a combination of tree and string structures.

2. STRUCTURE OF DEMUX

2.1 The structure of 1:10 DEMUX
The block diagram of the 1:10 DEMUX is shown as Figure 1. It consists of a clock channel and a data channel which include a high-speed 1:2 DEMUX, two low-speed 1:5 DEMUX, and some buffers. In the input, the high-speed 1:2 DEMUX demultiplexes 12.5Gb/s data to two 6.25Gb/s data. Then the two 6.25Gb/s data are sent to two low-speed 1:5 DEMUXs and 10 1.25Gb/s data are obtained at the output. The input 6.25 GHz clock is sent to these DEMUXs and a 5 frequency divider by which the 1.25GHz clock is obtained. In addition, because 1:2 DEMUX in this design uses CML latches, the input data, the input clock, and the 1:2 DEMUX output data are all differential CML-level signals. The subsequent 1:5 DEMUX and the 5 frequency divider are all designed with E-TSPC which need the single CMOS input signal. Therefore, double to single and level conversion circuits are added after the data channel and clock channel. To ensure the clock and the data correspondence, data and clock input buffers are essential. The output buffers are used to drive the external 50 Ohm for measurement. Other Buffers are utilized to obtain sufficient capability of driving DEMUXs and frequency divider.

2.2 The structure of 1:5 DEMUX
The structure of 1:5 string DEMUX is shown in Figure 2, which is composed of nine D flip-flops. However, there is a serious flaw in this structure: the heavy load of the clock circuit limits the speed of the clock circuit. To reduce this effect, the E-TSPC trigger which is triggered by a single clock is adopted because there is no clock skew phenomenon. Besides, at the same working speed the power consumption of E-TSPC trigger is lower than that of CML triggers.

![Figure 1. Block diagram of the 1:10 DEMUX](image1)

![Figure 2. Block diagram of the 1:5 DEMUX](image2)
2.3 The structure of 5 frequency divider
The structure of 5 frequency divider is shown in Figure 3. This design uses a digital frequency divider composed of D flip-flop, which has the advantages of simple structure, no need for inductance, relatively low power consumption, and a relatively large frequency division range [7]. The D flip-flops use the E-TSPC structure. And the two inputs and-non-gates can be integrated with E-TSPC, which can simplify the circuit, reduce the loop delay and increase the working speed [8].

![Figure 3. Block diagram of the 5 frequency divider](image)

3. Latch Circuit

3.1 CML
Figure 4 shows the circuit schematic of the CML latch which can achieve a high operation rate, although it consumes more power for the continuous tail current. The CML structure is composed of a sampling pair M1-M2, a latching pair M3-M4, a pair of loads R1-R2, two nMOS switches M5-M6 and a tail current source M7. The input signals D/ Dn and CK/ CKn are both differential signals. The working principle is: When CK is high, M5 is on while M6 is off and M1-M2 is used to sense the input in the sampling mode. When CK is low, M6 is on while M5 is off and the cross-coupled pair M3-M4 is configured as a positive feedback to latch the output in the latching mode. Therefore, the logical expression is shown in equation (1).

\[ Q^{n+1} = D \cdot CK + Q^n \cdot CKn \]  

(1)

The transmission delay of the CML can be shown as the equation (2).

\[ T_{delay} \propto \frac{C_L V_p}{I_{ss}} \]  

(2)

Where \( C_L \) is the total output load capacitor, \( V_p \) is the output single amplitude and \( I_{ss} \) is the tail current. At the same time, we can find that the power consumption of this latch is constant at \( V_{dd} I_{ss} \).

The advantages of CML logic are as follows [1] [9]: 1) The differential structure has high stability. 2) The electromagnetic field of the differential line is concentrated between the lines, which has little impact on the outside circuit. 3) CML logic also has a strong driving capabilities and is compatible with various high-speed circuit interfaces.

The disadvantages of CML logic are: 1) Because a pair of complementary clocks is needed in the circuit, there is a problem of clock skew. 2) CML logic circuit has a complicated structure and needs a large number of transistors, which causes a large chip area and high power consumption. 3) The stack structure of the circuit needs to provide a high power supply voltage.
3.2 E-TSPC

Figure 5 shows the circuit schematic of the E-TSPC which relies on node capacitance to store data, so it is a dynamic trigger [10]. The working principle is: When D=1, CK=1, M1 is on and M2 is off, which causes A=0. Then M3-M4 are on and the size of M3-M4 are set so that B=0. After that, M5-M6 are off which cause Q to maintain the original state. At this time, if CK changes from 1 to 0, M1 is off which make A remain 0 and B=1. Then M5-M6 are on and the size of M5-M6 are set to make \( \bar{Q} = 0 \), that is \( Q = 1 \). When D=0, CK=1, M1-M2 is on and the size of M1-M2 are set to make A=1, which cause B=0. Then M5-M6 are off so Q maintains the original state. At this time, if CK changes from 1 to 0, M1 is off which make A=1. Then M3-M4 are off, so B remains 0. After, M5 is off and M6 is on, which can get \( \bar{Q} = 1 \), that is \( Q = 0 \). When CK=0, if D changes from 1 to 0, A jumps from 0 to 1. Then M4-M5 are off and Q remains in the original state. Those show that this latch is triggered by a falling edge.

Compared with CML, E-TSPC has a simple structure and a small number of transistors, so chip area and power consumption can be reduced. Moreover, only a single clock is needed, and there is no problem of clock skew, which is good for speed increasing. However, this latch has a problem which can be seen in the previous working principle. When D=1, CK=1, A=0, and D changes from 1 to 0, M1-M2 are on at the same time. The circuit passes through M2 charge to A and through M1 discharge, so the electricity at A cannot be full instantaneously. There is a delay that will produce burrs. In order to reduce burrs, the size of M2 can be appropriately increased and the charging rate can be increased. Similarly, M3-M4, and M5-M6 also have the same problem, so the size of M3 and M5 can appropriately be increased, which increase the discharge rate.

4. Design of double to single and level conversion circuits

The circuit schematic of double to single and level conversion circuits is shown in Figure 6, which can convert a differential CML signal to a single CMOS signal. The first stage is a buffer circuit. Its gain
does not need to be too high, because the transition region with a larger slope is more disadvantageous when the process angle changes. The second stage is a differential amplifier circuit with a current mirror as the load. The mirrored current source converts the double-terminal input into a single-terminal output to achieve a double to single function. The P-channel tube in cascade with the first-stage N-channel tube has a level shifting function. The C point voltage is properly designed to Vdd/2. Finally, the cascading CMOS inverter is used to amplify and shape the signal, and improve the driving ability of the latter circuit.

**Figure 6.** Circuit schematic of the double to single and level conversion

5. SIMULATION RESULT

The proposed 1:10 DEMUX was designed and fabricated in TSMC 0.18μm CMOS technology. Figure 7 shows the layout of the circuit. The die size is 0.64mm×0.57mm and is determined by the bonding pad.

**Figure 7.** 1:10 DEMUX layout

In post simulation, the input signals are a 12.5Gb/s non-return-to-zero (NRZ) 2\(^{31}\)-1 pseudo-random binary sequence (PRBS) and a 6.25GHz sinusoidal clock. The ten 1.25 GB/s output eye diagrams, simulated by Cadence software, are shown in Figure 8. The eye opening is 400mVpp with external 50 Ohm load and the chip total power dissipation is 200mW. Figure 9 shows the output 1.25GHz clock waveform of the 5 frequency divider, which is outputted in the eye diagram mode of infinite superposition. When one data pattern (1111000001,1001000111,1000110101,1000011110) at 12.5Gb/s and 6.25GHz difference clock signals are input to 1:10 DEMUX, the corresponding output should be ten patterns at 1.25Gb/s (q1:1111,q2:1000,q3:1000, q4: 1100, q5:0010, q6:0011,q7:0001, q8:0111, q9:0101, q10:1110), which are shown in Figure 10. So the logic function of DEMUX is proved to be correct.
6. Conclusion
This paper designs and implements a 12.5Gb/s low-power 1:10 DEMUX in 0.18μm CMOS technology. The proposed circuit adopts the combination of tree and string structures, and selects CML and E-TSPC latch. All of those ways help in the realization of high speed, low power, and small area. The test results show when the supply voltage is 1.8V, DEMUX’s operating rate can be up to 12.5Gb/s. The whole system works well and the output eye diagrams are clear. The chip area (including the pads) is 0.64×0.57mm² and the total power consumption is 200mW. This paper will provide a good foundation for the subsequent 12.5 Gb/s SerDes receiver.

![Figure 8. Ten output eye-diagrams at 12.5Gb/s input](image)

![Figure 9. Waveform of output 1.25GHz clock](image)
Figure 10. Input and ten output waveforms at 12.5Gb/s input

7. References
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