Review

Status of Aluminum Oxide Gate Dielectric Technology for Insulated-Gate GaN-Based Devices

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Abstract: Insulated-gate GaN-based transistors can fulfill the emerging demands for the future generation of highly efficient electronics for high-frequency, high-power and high-temperature applications. However, in contrast to Si-based devices, the introduction of an insulator on (Al)GaN is complicated by the absence of a high-quality native oxide for GaN. Trap states located at the insulator/(Al)GaN interface and within the dielectric can strongly affect the device performance. In particular, although AlGaN/GaN metal–insulator–semiconductor high electron mobility transistors (MIS-HEMTs) provide superior properties in terms of gate leakage currents compared to Schottky-gate HEMTs, the presence of an additional dielectric can induce threshold voltage instabilities. Similarly, the presence of trap states can be detrimental for the operational stability and reliability of other architectures of GaN devices employing a dielectric layer, such as hybrid MIS-FETs, trench MIS-FETs and vertical FinFETs. In this regard, the minimization of trap states is of critical importance to the advent of different insulated-gate GaN-based devices. Among the various dielectrics, aluminum oxide (Al2O3) is very attractive as a gate dielectric due to its large bandgap and band offsets to (Al)GaN, relatively high dielectric constant, high breakdown electric field as well as thermal and chemical stability against (Al)GaN. Additionally, although significant amounts of trap states are still present in the bulk Al2O3 and at the Al2O3/(Al)GaN interface, the current technological progress in the atomic layer deposition (ALD) process has already enabled the deposition of promising high-quality, uniform and conformal Al2O3 films to gate structures in GaN transistors. In this context, this paper first reviews the current status of gate dielectric technology using Al2O3 for GaN-based devices, focusing on the recent progress in engineering high-quality ALD-Al2O3/(Al)GaN interfaces and on the performance of Al2O3-gated GaN-based MIS-HEMTs for power switching applications. Afterwards, novel emerging concepts using the Al2O3-based gate dielectric technology are introduced. Finally, the recent status of nitride-based materials emerging as other gate dielectrics is briefly reviewed.

Keywords: GaN; gate dielectric; aluminum oxide; interface; traps; instability

1. Introduction

Owing to the large bandgap of 3.43 eV, resulting in a high electric breakdown field of 3.3 MV/cm and in a low intrinsic carrier concentration, and to the large saturation velocity of $2.5 \times 10^7$ cm/s, GaN is one of the most promising semiconductors for the future energy-efficient generation of high-power, high-frequency and high-temperature electronics [1–4]. Besides the unique intrinsic material properties, one of the most attractive properties of GaN is the possibility to exploit the polar nature of GaN-based materials to form AlGaN/GaN heterostructures featuring a two-dimensional electron gas (2DEG) at the heterointerface with a high carrier density of over $1 \times 10^{13}$ cm$^{-2}$ and high mobility values exceeding 2000 cm$^2$ V$^{-1}$ s$^{-1}$ [5,6]. AlGaN/GaN heterostructures enable the fabrication of high electron mobility transistors (HEMTs) which can significantly outperform the
traditional Si power devices in terms of breakdown strength, on-resistance and switching speed, achieving higher power density and higher energy efficiency [7,8].

Nowadays, GaN-on-Si HEMTs qualified for 200 V and 650 V high voltage power switching applications with operating frequency capabilities in the MHz range are commercially available and on the way towards 1.2 kV applications using engineered substrates [1,9,10]. For targeting higher voltage capabilities up to 1.7–1.8 kV, current aperture vertical electron transistors (CAVETs) adopting AlGaN/GaN heterojunctions have also recently attracted significant attention [11–13], where the high conductivity of the 2DEG channel is combined with the better field distribution of the vertical device geometry, and hence with the capability of vertical architectures of achieving an even higher breakdown voltage without enlarging the device area, in contrast to lateral transistors. In addition, GaN-based HEMTs with downscaled gate lengths to the sub-100 nm regime have also been demonstrated to achieve maximum current gain cutoff frequencies over 200 GHz, which are well suited for radio frequency (RF) high power amplifiers for 5G and beyond applications [14–18].

Despite the potentiality of AlGaN/GaN HEMTs, one of the most serious problems degrading the device performance and reliability is represented by the exceedingly high leakage currents through the Schottky-gate contact, especially under forward gate bias, which limits the gate voltage swing and the maximum on-state current of the device, resulting in reduced power efficiency and weak device failure protection [19]. In particular, a small gate swing is a strong limiting factor for power switching applications due to faulty gate voltage overshoots often occurring in circuits, which can eventually lead to early device failures. Moreover, since GaN-based HEMTs are naturally normally on (or depletion-mode) transistors with a negative threshold voltage \( V_{th} \), normally off (or enhancement-mode) HEMTs with a positive \( V_{th} \) are highly preferred to guarantee safe operation and for the reduced power consumption in power switching devices [20,21]. However, since normally off devices require a large positive gate voltage to be turned on, the problem of gate leakage currents becomes even more critical in normally off HEMTs. Similarly, in RF applications, power amplifiers using Schottky-gate HEMTs can suffer from reduced gain and efficiency caused by large gate inputs, which can drive the devices into deep forward bias regimes [22].

The employment of a metal–insulator–semiconductor (MIS) gate is an efficient way to suppress the gate leakage currents of AlGaN/GaN HEMTs, enabling reduced power consumption, a larger gate bias swing and a better immunity to gate breakdown [23–25]. However, in contrast to Si-based devices, the introduction of an insulator in AlGaN/GaN metal–insulator–semiconductor high electron mobility transistors (MIS-HEMTs) is complicated by the absence of a high-quality native oxide for (Al)GaN. Trap states located at the dielectric/(Al)GaN interface or within the dielectric can lead to dynamic charge/discharge processes, which are especially critical in the case of wide bandgap GaN-based materials where the traps can be deeply located in the bandgap and can cause severe operational instability due to their slow detrapping behavior [26–29]. The instability of the threshold voltage in AlGaN/GaN MIS-HEMTs is one of the major challenges [30–33]. In particular, a serious \( V_{th} \) shift induced by the “spill-over” of electrons from the 2DEG channel towards the dielectric/(Al)GaN interface in forward gate bias conditions has often been reported [34–37]. Another problem is the degradation of the current linearity in the transfer characteristics of AlGaN/GaN MIS-HEMTs, which can be responsible for gain loss and the degradation of large signal linearity in power amplifiers [38].

Besides insulated-gate GaN-based transistors adopting AlGaN/GaN heterostructures, other emerging GaN-based devices in the form of MIS-FETs use a gate dielectric layer on a GaN channel, such as lateral hybrid GaN MIS-FETs [39], vertical GaN trench MIS-FETs [40] and vertical FinFETs [41]. Figure 1 schematically summarizes the main configurations of lateral and vertical GaN-based transistors employing a gate dielectric layer. A Schottky-gate HEMT is reported for comparison in Figure 1a. Hybrid GaN MIS-FETs obtained by a fully recessed AlGaN barrier layer are especially attractive for normally off operation
and large gate voltage operation [42], while GaN trench MIS-FETs have drawn attention among other vertical transistor concepts since they are inherently normally off with a $V_{th} > 3$ V and do not need the regrowth of the AlGaN/GaN channels [43,44]. Similar to MIS-HEMTs, instabilities over the gate dielectric affecting the device performance can arise in GaN devices with MIS-FET configurations due to the trap states at the dielectric/GaN interface influencing the $V_{th}$ and reducing the current drive capability or/and bulk or border traps within the dielectric itself, which might mostly affect the long-term reliability performance of the device [43,45]. Moreover, differently from the MIS-HEMTs, where the 2DEG formed at the AlGaN/GaN interface benefits from the spatial separation from the dielectric/AlGaN interface, minimizing the interface scattering processes [46], interface traps in GaN MIS-FET configurations are located in the proximity of the electron channel and are more prone to act as impurity scattering centers, additionally affecting the carrier mobility [47]. This is particularly challenging for transistor concepts including a recess of the AlGaN barrier layer, as in the case of trench MIS-FETs and vertical FinFETs, since the etching process can critically affect the properties of the dielectric/GaN interface [48].

Therefore, regardless of the transistor concept and design, trap states need to be minimized to ensure the safe operation and long-term lifetime of the insulated-gate GaN-based transistors. In particular, a gate dielectric technology aiming to improve the dielectric/(Al)GaN interface and dielectric bulk quality is essential to enhance the performance of the device. In general, various insulator materials have been employed, with SiO$_2$, SiN and Al$_2$O$_3$ as the most commonly used dielectrics [7,29,49,50]. The same dielectric layer deposited both underneath the gate as well as between the gate and the ohmic contacts of the source and drain usually functions both as the gate dielectric and the passivation layer [51]. The latter has been indeed reported to mitigate the effects of drain current collapse and leakage currents at the (Al)GaN surface due to the passivation of trap states at the surface [52–54]. However, even though excellent device characteristics have been obtained, trap states in MIS gate structures still remain one of the biggest challenges for insulated-gate GaN-based transistors, and the practical implementation of these devices has been hindered by the concerns over the gate dielectric stability and reliability [1].

In this paper, the current status of the gate dielectric technology employing Al$_2$O$_3$ for insulated-gate GaN-based transistors is reviewed. First, the relevant aspects taken into account for selecting a suitable gate dielectric for GaN-based transistors are highlighted and the influence of this additional layer on the device parameters and performance is discussed. Afterwards, the state of the art of Al$_2$O$_3$ as a gate dielectric is presented with a particular
attention to the recent progress in engineering high-quality Al$_2$O$_3$/(Al)GaN interfaces and to the performance of Al$_2$O$_3$-gated GaN-based MIS-HEMTs for power switching applications. Novel emerging concepts using the Al$_2$O$_3$-based gate dielectric technology are also introduced. Finally, the recent status of nitride-based materials emerging as other gate dielectrics is briefly reviewed.

### 2. Gate Dielectrics on (Al)GaN

The design of a MIS gate structure for insulated-gate GaN-based transistors requires consideration of the properties of the bandgap, the band offset to (Al)GaN, the permittivity and the chemical stability of the insulators [7,29,49–51]. For a sufficient suppression of the gate leakage currents, even at forward gate bias operation, a large bandgap material as well as large band offsets to (Al)GaN are necessary, in particular for power switching devices. On the other hand, a high value of permittivity is favorable to obtain high transconductance [55]. In particular, in the case of MIS-HEMTs, since the introduction of a dielectric leads to a reduction of the gate-to-channel capacitance with respect to Schottky-gate HEMTs, a high permittivity dielectric reduces the capacitive contribution of the gate dielectric, enabling it to obtain a stronger coupling between the gate and the 2DEG channel, and hence to maintain a high transconductance, which is especially important for RF devices. At the same time, in normally on MIS-HEMTs, high-permittivity materials can minimize the shift of the threshold voltage towards negative values when compared to Schottky-gate HEMTs, which is beneficial to reduce the static power consumption and to improve the energy efficiency of the device [7].

Various insulator materials have already been considered as gate dielectrics in insulated-gate GaN-based transistors. Figure 2 reports the relationship between the bandgap and permittivity for the relevant insulators and nitride compounds. Figure 3a shows the band offsets of the insulators on the GaN as calculated by Robertson and Falabretti, who first predicted the band alignment of the GaN and the insulators based on the calculation of the charge neutrality levels (ECNL) [56]. The band offsets of the dielectrics on Al$_{0.3}$Ga$_{0.7}$N, recently determined by Reddy et al. using the same method, are illustrated in Figure 3b [57]. Note that, as shown from the comparison of Figure 3a,b, the different values of the energy bandgap of the same insulators are used in the calculations performed by Robertson and Falabretti [56] and by Reddy et al. [57].

![Figure 2. Energy bandgap versus permittivity for major insulators and GaN compounds. Data taken from [7,29,49–51].](image-url)
SiO$_2$ is an attractive insulator due to its large bandgap, large band offset to (Al)GaN and chemical stability. In fact, after Khan and coworkers first applied SiO$_2$ to AlGaN/GaN MIS-HEMTs to control the gate leakage currents and improve the gate voltage swing capability [24], further high-performance MIS-HEMTs using SiO$_2$ have been demonstrated [58,59]. Nevertheless, the relatively low dielectric constant of SiO$_2$ represents a disadvantage compared to other dielectrics. From this perspective, various high-permittivity dielectrics such as HfO$_2$, ZrO$_2$, Ta$_2$O$_5$, L$_2$O$_3$, CeO$_2$, TiO$_2$, etc., have been applied to the MIS gate structures of GaN HEMTs [60–72]. Although higher $g_m$ values have been achieved in some cases, most of these insulators have reported to be relatively susceptible to leakage problems due to the relatively small band offsets with respect to (Al)Ga$_2$O$_3$ [49,68,73,74]. Similar observations of high gate leakage currents were reported for MIS gate structures employing dielectrics such as SiN$_x$ and Ga$_2$O$_3$ due to the small conduction band offsets [51,75–77]. Ga$_2$O$_3$ would be appealing as a native oxide grown by thermal or chemical processes. However, in addition to the small band offset to GaN, Ga$_2$O$_3$ grown by thermal oxidation at low temperatures has a slow growth rate, while surface damage can be caused at higher growth temperatures [51]. Moreover, the growth of Ga$_2$O$_3$ is even more difficult on AlGaN since Al is more easily oxidized than Ga. Differently, SiN$_x$ deposited by in situ metal organic chemical vapor deposition (MOCVD) or by low-pressure chemical vapor deposition (LPCVD) has emerged as a promising candidate as a gate dielectric as well as a passivation layer [42,78]. Similarly, AlN has also been reported in a few studies to be suitable as a gate insulator and passivation layer, especially due to its small lattice mismatch to (Al)GaN [51,79–81]. Other attempts have also used dielectrics like NiO, MgO and Sc$_2$O$_3$ [82–87], stacked dielectric layers like SiN$_x$/SiO$_2$, SiN$_x$/Al$_2$O$_3$ and HfO$_2$/Al$_2$O$_3$ [88–90] or engineered alloys such as SiON, HfSiO$_x$ and LaLuO$_3$ in order to tune the dielectric constant and band gap of the insulators [90–93]. A comprehensive overview and comparison of the various insulators which have been considered as gate dielectrics for insulated-gate GaN-based devices is given in [7,29,49–51].
Among the insulators, Al₂O₃ remains one of the most attractive insulators as a gate dielectric because of its large bandgap and conduction band offset to (Al)GaN, relatively high permittivity (~9) as well as high breakdown field (~10 MV/cm) and thermal and chemical stability against (Al)GaN [75,94,95]. Additionally, the considerable technological progress in the atomic layer deposition (ALD) process enables the deposition of high-quality Al₂O₃ films to the gate structures in GaN transistors. In the next section, the status of the gate dielectric technology using Al₂O₃ for GaN-based devices is reviewed.

3. Al₂O₃ for Insulated-Gate GaN Devices

Table 1 reports the physical parameters of the energy bandgap (E₀), conduction band offset (ΔE_c) and valence band offset (ΔE_v) obtained experimentally from amorphous Al₂O₃ films deposited on GaN and AlGaN by various deposition methods. Note that the bandgap of the amorphous Al₂O₃ ranges between 6.7 eV and 7.6 eV depending on the method of the oxide film growth, and it is lower than the value for the crystalline bulk α-Al₂O₃ (8.8 eV–9 eV) considered in the theoretical calculations (Figure 3). In fact, it is well known that the E₀ of Al₂O₃ compounds strongly depends on its crystallographic phase [96,97]. Momida et al. investigated the structure of amorphous Al₂O₃ by first-principles calculations, concluding that the reduction of the bandgap of amorphous Al₂O₃ compared to crystalline Al₂O₃ could be related to the changes in the density of the Al₂O₃ compounds and the average coordination number of Al atoms [98]. Toyoda et al. showed that annealing at temperatures of 800 °C led to phase transformations of the Al₂O₃ films from amorphous to crystalline, which correlated to a significant increase in the energy bandgap and the modification of the conduction band discontinuity [99]. Afnan’ev et al. pointed out that for Al₂O₃ films treated at temperatures above 800 °C, the widening of the Al₂O₃ bandgap with the phase transformation from amorphous to crystalline mostly occurred at the valence band side [96,97]. Differently, Yang et al. revealed that the annealing processes at a lower temperature of 650 °C can affect the band bending of GaN but has almost no effect on the Al₂O₃/GaN band offset [100]. The decrease of the bandgap of amorphous Al₂O₃ has also been associated with defect-induced states located in the bandgap [101]. This could explain the large discrepancy between the theoretical (Figure 3) and experimental (Table 1) values of ΔE_v. In fact, since in the case of Al₂O₃ the valence band maximum states are associated with the O 2p states, and the conduction band minimum states are associated with the Al 3s, 3p states [102], the rehybridization between Al 3s, 3p and O 2p modifies the charge transfer between Al and O and consequently decreases the bandgap, thus increasing the valence band maximum [51]. In contrast to ΔE_v, the experimental values of ΔE_c obtained for the Al₂O₃/(Al)GaN system are consistent with the theoretical predictions and make Al₂O₃ a suitable dielectric for insulated-gate GaN-based transistors.

In addition to the physical properties of the bandgap of Al₂O₃ and the band offsets in the Al₂O₃/(Al)GaN system, high-quality dielectric layers in terms of defects and bulk traps and an Al₂O₃/(Al)GaN interface with a low interface trap density are required to deliver a high performance and highly efficient MIS gate structure, as discussed above. It is important to mention that these properties strongly depend on the deposition technique and temperature, the crystalline structure of the film and the surface and annealing treatments [51]. Among the techniques explored for the deposition of Al₂O₃ films, such as sputtering [103], the oxidation of a thin Al layer [53] and MOCVD [104–106], the ALD technique is widely used. The main advantages of the ALD method are the low deposition temperature (<350 °C), the excellent film thickness control as well as the high uniformity and conformality, which have enabled the deposition of high-quality Al₂O₃ films and Al₂O₃/(Al)GaN interfaces compared to other methods. Nevertheless, despite substantial progress in the ALD technology, large amounts of defects in the as-deposited Al₂O₃ bulk material and interface traps at the Al₂O₃/(Al)GaN interface are still present and still hinder the success of the insulated-gate GaN devices [1].
The exact nature of the fixed charges in the bulk of the as-deposited Al2O3 is still under debate, with native O2

| Structure  | Deposition Method | Measurement Method | E_c (eV) | ΔE_c (eV) | ΔE_V (eV) | Ref.           |
|------------|------------------|--------------------|---------|-----------|-----------|----------------|
| Al2O3/GaN  | ALD              | C–V                | -       | -         | 1.2       | [107]         |
| Al2O3/GaN  | ALD              | XPS and F–N plot   | 6.7     | 2.2       | -         | [108]         |
| Al2O3/GaN  | ALD              | XPS                | 6.6     | 2.0       | 1.2       | [109]         |
| Al2O3/GaN  | ALD              | IPE and C–V        | -       | 2.2       | -         | [110]         |
| Al2O3/GaN  | PEALD            | XPS and UPS        | 6.7     | 2.1       | 1.2       | [111]         |
| Al2O3/GaN  | PEALD            | XPS and UPS        | -       | 1.3       | 1.8       | [100]         |
| Al2O3/GaN  | CVD              | XPS and XAS        | 7.6     | 2.7       | 1.5       | [99]          |
| Al2O3/Al0.3Ga0.7N | MBD + ECR plasma oxidation | XPS | 7.0 | 2.1 | 0.8 | [53,75] |
| Al2O3/Al0.25Ga0.75N | ALD | XPS | 6.9 | 1.8 | 1.2 | [112] |
| Al2O3/Al0.25Ga0.75N | ALD | XPS | 6.7 | 1.8 | 0.9 | [26] |

3.1. Al2O3/(Al)GaN Structures

The presence of defects acting as traps or fixed charge centers within the Al2O3 films and at the Al2O3/(Al)GaN interface is of critical importance because of their potential to affect the threshold voltage and the gate leakage currents of the MIS gate structures [51], eventually deteriorating the operational stability and the reliability of the insulated-gate GaN-based devices.

For ALD-Al2O3/(Al)GaN structures, a positive fixed charge arising from donor-type interface states and/or defect levels in the bulk Al2O3 was often reported [112–115]. In this regard, Esposto et al. [107] and Son et al. [116] pointed out that fixed charges at the Al2O3/GaN interface shifted the flat-band voltage (VFB) in the C–V curves of Al2O3/GaN capacitors. A shift of the VFB towards the negative bias direction in Al2O3/GaN structures was observed by Kaneki et al. [115]. Similar shifts in the C–V characteristics attributed to interface states acting as fixed charges were reported for Al2O3/AlGaN/GaN structures by Mizue et al. [26] and Yatabe et al. [73]. Nishiguchi et al. [38] reproduced the observed negative shift in the C–V curve of Al2O3/AlGaN structures, assuming an effective fixed positive charge of +1.2 × 10^{13} \text{cm}^{-2} in the Al2O3 layer or at the Al2O3/AlGaN interface.

In line with this, annealing treatments have been reported to affect the VFB and Vth of Al2O3/(Al)GaN structures as a result of a change in the defect levels in Al2O3 films [117,118]. For example, Hashizume et al. [114] reported a VFB recovery of Al2O3/GaN structures after a post metallization annealing (PMA) in N2 at 200–400 °C, possibly attributed to the reduction of the donor-type interface states and/or the defect levels in the bulk. Similarly, Hung et al. [119] obtained a VFB recovery by PMA in H2/N2 forming gas at 400–550 °C. Zhou et al. [120] showed a permanent positive shift of the Vth in ALD-Al2O3-gated MIS-HEMTs after a postdeposition annealing (PDA) at 600 °C in N2, which was also suggested to be caused by a reduction of the deep-level bulk or interface traps. For similar reasons, a recovery of the Vth of MIS-HEMTs towards positive bias values was reported by Nishiguchi et al. [38] when using a reverse-bias anneal at 300 °C in air, and by Nakazawa et al. [121] with an anneal process at 750 °C in O2 atmosphere.

The exact nature of the fixed charges in the bulk of the as-deposited Al2O3 or in the vicinity of the Al2O3/(Al)GaN interfaces is still under debate, with native O2.
in the oxide layer or dangling bonds at the interface being the major candidates. Choi et al. [122] investigated the impact of native point defects in Al₂O₃ by first-principle calculations, revealing that oxygen vacancies introduce charge-state transition levels near the GaN conduction band edge, which can act as border traps close to the Al₂O₃/n-GaN interface or as source of leakage current through the dielectric. However, other defects such as aluminum vacancies and interstitials have been identified to act as fixed-charge centers [122]. Weber et al. [123] also suggested that aluminum vacancy and oxygen interstitial defects introduce negatively charged centers while the aluminum interstitials act as positively charged centers, affecting carrier scattering in the channel and the threshold voltage of the device. Moreover, Liu et al. [124] studied the energy levels of the oxygen vacancy in Al₂O₃. Shin et al. [125] and Kim et al. [126] identified oxygen and Al dangling bonds as the origin of the fixed charges in ALD-Al₂O₃. Huang et al. [127] suggested that these defective dangling bonds, which are also associated to fixed positive charges and acceptor-like border traps, can be suppressed by the substitution of H₂O as an oxygen source with O₃ for the ALD deposition of Al₂O₃. Other groups have also demonstrated the influence of using different ALD precursors and different deposition temperatures on oxide charges, as well as the interface traps of Al₂O₃ films [128–132].

Defect states inside Al₂O₃ can affect the leakage current of the MIS gate structures through trap-assisted tunneling mechanisms. For Al₂O₃-gated MIS-HEMTs under forward bias, Liu et al. [133] and Yoshitsugu et al. [131] showed that trap-assisted tunneling (TAT) and Poole–Frenkel emissions (PFE) are dominant at medium electric fields and temperatures above 0 °C, whereas Fowler–Nordheim tunneling (FNT) dominates at high electrical fields and temperatures below 0 °C. In addition, Yoshitsugu et al. [131] estimated a TAT-related trap energy of about 1.0 eV below the conduction band minimum of Al₂O₃. Wu et al. [134] instead suggested that TAT is the dominant transport mechanism in high oxide fields, with trap energies of ~1.1–1.2 eV, while PFE was responsible for medium oxide field gate current transport. Recently, Heuken et al. [135] also suggested that the time-dependent dielectric breakdown (TDDB) of ALD-Al₂O₃ films occurs with the presence of an initial defect density in the film and is then related to the formation of a percolation path by randomly generated defects in the oxide under stress bias. The time to breakdown was found to be thermally activated, with an activation energy of 1.25 eV, similar to the reported values of the activation energy of TAT in Al₂O₃ at a high oxide field [131,134].

While defect states and bulk traps acting as fixed charges mostly affect the absolute value of the threshold voltage, the charging and discharging of bulk traps, especially border traps near the Al₂O₃/(Al)GaN interface, and interface traps deeply located in the bandgap of the (Al)GaN at the Al₂O₃/(Al)GaN interface can induce significant dynamic instabilities of the threshold voltage and of the drain current during device operation due to their slow detrapping behavior. A schematic illustration of the band diagram of Al₂O₃/GaN and Al₂O₃/AlGaN/GaN structures, including border and interface traps, is shown in Figure 4.

Figure 4. Schematic band diagram of the (a) Al₂O₃/GaN structure and (b) Al₂O₃/AlGaN/GaN heterostructure at equilibrium, showing border traps near the Al₂O₃/(Al)GaN interface and interface traps at the Al₂O₃/(Al)GaN interface. E_C and E_V are the conduction and valence bands of (a) GaN and (b) AlGaN, respectively. E_F denotes the Fermi energy.
For these reasons, many groups have focused their efforts on the characterization and minimization of trap states at the dielectric/(Al)GaN interface of the MIS gate structures. Figure 5 illustrates a summary of the interface trap density ($D_{it}$) distributions reported in the literature for Al$_2$O$_3$/(Al)GaN structures. Note that the best results reported in each reference have been illustrated in Figure 5. The Terman method [136] and conductance method [137] are often used to estimate the interface trap state densities of Al$_2$O$_3$/GaN structures. Differently, since for Al$_2$O$_3$/AlGaN/GaN structures the evaluation of interface trap states is more challenging due to the presence of a double interface (Al$_2$O$_3$/AlGaN and AlGaN/GaN) complicating the potential distribution over the structure, more advanced techniques such as conductance dispersion techniques [138–140] and frequency and/or temperature-dependent capacitance voltage measurements [26,73,141] are employed. More detailed overviews on the characterization of the electronic states at the insulator/(Al)GaN interfaces of GaN-based MIS-HEMTs with respect to their applicability and potential limitations are given by Ramanan et al. [142] and Yatabe et al. [49].

![Figure 5](image-url)

**Figure 5.** Interface density distributions (column) extracted from literature for (I) Al$_2$O$_3$/GaN, (II) Al$_2$O$_3$/GaN/Al$_x$Ga$_{1-x}$N/GaN and (III) Al$_2$O$_3$/Al$_x$Ga$_{1-x}$N/GaN structures. The corresponding reference is indicated at the bottom of the graph for each column. The conduction band minimum $E_C$ of GaN and AlGaN is set at 0 eV as reference. The valence band maximum $E_V$ of GaN and AlGaN, accordingly to the bandgap values of 3.4 eV and 3.9 eV, respectively, are also illustrated as dashed lines.

The results reported in Figure 5 highlight the presence of high-density interface trap states, especially at energies close to the conduction and valence band edges of (Al)GaN. For Al$_2$O$_3$/GaN interfaces, minimum values of the interface state densities in the range of $10^{10}$–$10^{11}$ cm$^{-2}$ eV$^{-1}$ have been reported [114,115,143–146]. In comparison, Al$_2$O$_3$/AlGaN interfaces have shown minimum values of interface state densities that are about one order of magnitude higher [26,27,38,73,145,147–150]. Mizue et al. [26] suggested that this difference can be due to oxygen incorporation into AlGaN or to a higher density of defects in the AlGaN layer. Note also that some groups investigated Al$_2$O$_3$/GaN/AlGaN/GaN structures where a thin GaN layer (~1–3 nm) was present on top of the AlGaN layer, possibly affecting the distribution of the interface trap states [105,150–153]. A very thin GaN cap layer is indeed often included in the AlGaN/GaN epitaxial material, as it also helps to protect the AlGaN surface and to reduce leakage currents. Gregušová et al. [150] obtained an interface trap state density that was two to three times lower for the Al$_2$O$_3$-gated AlGaN/GaN structures with a GaN cap compared to ones without a GaN cap. On the contrary, Šapajna et al. [106] reported almost the same C–V characteristics and interface trap state distributions for Al$_2$O$_3$/(GaN)/AlGaN/GaN structures with and without a GaN cap.
cap layer. For ALD-Al₂O₃/AlGaN/GaN structures, Mizue et al. [26] estimated the trap states density distribution at the ALD-Al₂O₃/AlGaN interface for the first time, showing that trap states with densities higher than $1 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$ exist at the Al₂O₃/AlGaN interface. To evaluate the near-midgap electronic states at room temperature (RT), a photoassisted C–V method using photon energies less than the AlGaN bandgap was developed [26,73]. For states close to the valence band of (Al)GaN, Matys et al. [154,155] developed a method based on the measurement and simulations of the photo-capacitance of MIS gate heterostructures. Combining this method with the photoassisted capacitance–voltage technique, the interface state density in the entire band gap at the Al₂O₃/AlGaN interface was determined, revealing the presence of a large amount of trap states with $D_{it}$ values higher than $1 \times 10^{13} \text{cm}^{-2} \text{eV}^{-1}$ also near the valence band edge [148].

When using Al₂O₃ films on (Al)GaN, particular attention has to be given to the temperature processes applied after the dielectric deposition. Hori et al. [108] showed that the annealing process at 800 °C for the ohmic contact formation applied after the ALD-Al₂O₃ deposition created a large number of microcrystalline regions in the Al₂O₃ layer, causing a pronounced increase of the leakage current of the Al₂O₃/n-GaN structures. To prevent this effect, an “ohmic-first” approach with a SiN protection layer was applied, which maintained the amorphous phase in the atomic configuration of Al₂O₃, leading to a sufficient suppression of the leakage current. In addition, protecting the surface with a SiN layer during annealing resulted in the low interface trap densities of less than $1 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$ extracted from the C–V characteristics of the Al₂O₃/GaN structures. 

Other processing steps for the fabrication of GaN devices are also critical and can affect the interface quality and the electrical properties of the Al₂O₃/(Al)GaN structures. To achieve normally off operation, recessed gates are often employed in MIS-HEMTs or hybrid MIS-FETs. For this reason, the influence of inductively coupled plasma (ICP) etching on the interface properties of Al₂O₃/(Al)GaN structures has also been investigated. Yatabe et al. [73] estimated the state density distribution at the Al₂O₃/AlGaN interface of MIS structures subjected to ICP dry etching of the AlGaN surface, using for the first time the combination of the photoassisted C–V method and the modeling of the C–V curves [26,156]. Trap state densities higher than $2 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$ were obtained at the Al₂O₃/AlGaN interface of the ICP-etched structures [73]. Without the ICP etching of AlGaN, a near-midgap $D_{it}$ of about $1 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$ or less was obtained. Similarly, Kim et al. [144] also investigated the effects of a Cl₂-based ICP etching on the interface properties of Al₂O₃/GaN structures. From the X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM) analyses, it was shown that the ICP etching caused a disorder of the chemical bonds at the GaN surface. This resulted in high-density trap states with a density larger than $1 \times 10^{13} \text{cm}^{-2} \text{eV}^{-1}$ near the conduction band edge of the GaN at the Al₂O₃/GaN interface, which was suggested to include defects related to nitrogen vacancy ($V_N$) levels. A decrease of the interface state density was obtained by applying a PDA process in N₂ at 400 °C, which partially recovered the $V_N$-related levels, thus increasing the chemical bond order at the GaN surface. Yatabe et al. [149] also reported that the ICP etching of the AlGaN surface introduced a monolayer-level crystalline roughness, the disorder of the chemical bonds and various types of defect complexes including $V_N$, resulting in high trap state densities of up to $8 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$ at the Al₂O₃/AlGaN interface. Fang et al. [157] also reported that Cl₂-based ICP etching enhanced the deep centers at the GaN surface originating from $V_N$ and other defect complexes.

Other studies have demonstrated the importance of PDA and PMA treatments to minimize the interface trap states at the Al₂O₃/(Al)GaN interface. From the TEM investigations, Hashizume et al. [114] revealed that PMA in N₂ at 300–400 °C led to a uniform distribution of the lattice constant near the interface of the ALD-Al₂O₃/GaN MIS structures, which resulted in excellent C–V characteristics almost without frequency dispersion and a reduced $D_{it}$ ranging from 1 to $4 \times 10^{10} \text{cm}^{-2} \text{eV}^{-1}$ at energies near the conduction band edge. Similar values of $D_{it}$ at the Al₂O₃/GaN interface after PMA in N₂ at 400 °C were also very recently obtained by Ando et al. [158]. Ando et al. [147] also demonstrated that a PMA
in N₂ at 300 °C led to a similar reduction of the electronic states at the ALD-Al₂O₃/AlGaN interface. Kaneki et al. [115] pointed out that annealing under reverse bias at 300 °C in air for 3 h is also beneficial to decrease the interface state density of ALD-Al₂O₃/GaN structures, and it is more effective than PDA in N₂ at 400–700 °C, probably due to a relaxation of the dangling bonds and/or the point defects at the GaN surface. Moreover, almost no shift of the V₃ FB with respect to the expected value was observed in the C–V curves due to the reduction of the donor-type interface states and/or defect levels in the bulk Al₂O₃. Similar effects of the reverse-bias annealing were obtained by Nishiguchi et al. [38] for ALD-Al₂O₃/AlGaN structures. Winzer et al. [143] reported that PDA in O₂ or forming gas (H₂/N₂) at 500 °C were more efficient for decreasing the traps at the Al₂O₃/GaN interface than PDA in N₂ at the same temperature. A very low interface trap density of less than 5 × 10¹¹ cm⁻² eV⁻¹ was achieved for Al₂O₃/GaN structures treated by forming gas PDA at 500 °C. However, it was also reported that forming gas PDA resulted in a detrimental increase of the leakage currents of the Al₂O₃ films. Similar results were reported by Long et al. [159], where the effect of trap passivation during the forming gas anneal was correlated to the incorporation of hydrogen at the interface.

Similar to annealing processes, surface treatments are also effective in reducing interface trap states at the Al₂O₃/(Al)GaN interface. Hori et al. [27,145] demonstrated that an N₂O-radical treatment can decrease interface states both at the Al₂O₃/GaN and Al₂O₃/AlGaN interfaces. For Al₂O₃/AlGaN structures, the interface state density was estimated to be 1 × 10¹² cm⁻² eV⁻¹ or less around the midgap and 8 × 10¹² cm⁻² eV⁻¹ near the conduction band edge [27]. Calzolaro et al. [151] recently reported a significant reduction of frequency dispersion of the C–V characteristics of Al₂O₃/GaN/AlGaN/GaN structures after a remote O₂ plasma-based surface treatment prior to the ALD-Al₂O₃ deposition combined with a PMA in N₂ at 350 °C. The Dₜ was estimated to be reduced to a value in the order of 2 × 10¹² cm⁻² eV⁻¹ near the conduction band edge.

Trapping mechanisms at the Al₂O₃/(Al)GaN interface are especially critical for AlGaN/GaN MIS-HEMTs under forward gate bias, where electrons can spill over from the 2DEG channel towards the dielectric by overcoming the AlGaN barrier and become trapped at the Al₂O₃/(Al)GaN interface [34–37]. Similarly, charge trapping in high-density electronic states at the interface has been reported to lead to a significant screening of the gate electric field and the consequent loss of control of the surface potential of the barrier layer, causing the degradation of the current linearity and the saturation of the current at forward bias in AlGaN/GaN MIS-HEMTs [38]. In this regard, the next section focuses on reviewing the recent progress on the performance of Al₂O₃-gated MIS-HEMTs.

3.2. Al₂O₃-Gated MIS-HEMTs

Among the issues facing the MIS gate toward the improvement of the performance of AlGaN/GaN MIS-HEMTs, the dynamic V th instability caused by the trapping mechanisms involving the gate dielectric is the one major concern [1]. The instability of the V th has been reported under various bias conditions [31,32,34,78,160,161]. In particular, the large V th shift induced by forward gate bias stress due to electron trapping at the dielectric/(Al)GaN interface is one of the most serious problems for the operational stability and reliability of the device [34–37]. For this reason, many groups have focused their efforts on studying the origin of the V th instability and various fabrication processing strategies to overcome this issue.

For Al₂O₃-gated MIS-HEMTs, Lu et al. [32] reported that a larger V th shift towards the forward bias direction was induced by increasing the gate positive bias stress in the pulsed current-voltage (I-V) measurements. Similar results were obtained by other groups [28,31,35,151,160,162,163]. Bisi et al. [160] pointed out that the large positive shift of the V th can also promote the current collapse of MIS-HEMTs. Regarding the origin of the V th instability, Šapajna et al. [105] discussed the effect of interface states and bulk traps on the V th shift in Al₂O₃-gated MIS-HEMTs. Wu et al. [153] and Zhu et al. [33] pointed out that the V th shift during a positive gate bias stress was highly correlated to the trap states
at the dielectric/(Al)GaN interface but also to the border traps near the interface. Fixed charges within the dielectric are also involved in the \( V_{th} \) shift mechanism [107,116].

A reduction of the interface and/or border traps by means of annealing and surface treatments can lead to an improvement of the dynamic \( V_{th} \) instability of MIS-HEMTs. In addition, as mentioned before, the current linearity and the saturation of current at forward bias of MIS-HEMTs can be also affected by a change in the density of the electronic states at the dielectric/(Al)GaN interface [38]. Hori et al. [27] reported that the reduction of the interface states obtained by applying an \( \text{N}_2\text{O} \)-radical treatment on the AlGaN surface prior to the ALD-\( \text{Al}_2\text{O}_3 \) deposition led to a higher maximum drain current of the MIS-HEMTs at the positive gate bias and a suppressed \( V_{th} \) instability under the negative gate bias stress even at 150 °C. Nishiguchi et al. [38] showed that the improvement of the \( \text{Al}_2\text{O}_3 \)/AlGaN interface by the reverse-bias anneal at 300 °C in air for 3 h of \( \text{Al}_2\text{O}_3 \)-gated MIS-HEMTs gave a better gate control of the current even at forward gate bias, effectively enhancing the current linearity, subthreshold behavior and the maximum drain current of the device. Moreover, reduced gate leakage currents and more stable \( V_{th} \) under forward bias stress and at higher temperatures were obtained. Similarly, Ando et al. [147] recently reported on the improved gate controllability and current linearity of MIS-HEMTs with the \( \text{Al}_2\text{O}_3 \) gate dielectric as a result of a reduction of the electronic states at the \( \text{Al}_2\text{O}_3 \)/AlGaN interface after PMA in \( \text{N}_2 \) at 300 °C. A subthreshold slope of 68 mV dec\(^{-1}\) and excellent \( V_{th} \) and operation stability up to 150 °C were also achieved, as shown in Figure 6. Note that in this case Ando et al. [147] pointed out that the improvement of the device performance also benefited from using epitaxial GaN layers grown on free-standing GaN substrates from hydride vapor phase epitaxy (HVPE) with a low dislocation density. Very recently, Calzolaro et al. [151] reported that the reduction of interface trap states by a remote \( \text{O}_2 \) plasma-based surface treatment before the ALD-\( \text{Al}_2\text{O}_3 \) deposition combined with a PMA in \( \text{N}_2 \) at 350 °C resulted in a better \( V_{th} \) stability in pulsed I-V measurements. It is worth mentioning that, despite the benefits of the PMA treatments, specific attention has to be paid to the employment of higher PMA temperatures, as it can affect the gate leakage currents of the devices using ALD-grown \( \text{Al}_2\text{O}_3 \) films [119,164]. Therefore, a trade-off must be considered when using the PMA treatment between the quality of the \( \text{Al}_2\text{O}_3 \)/(Al)GaN interface and the gate leakage currents in a certain voltage range of operation.

Figure 6. Transfer characteristics of \( \text{Al}_2\text{O}_3 \)-gated AlGaN/GaN MIS-HEMTs fabricated on free-standing HVPE GaN substrates and subjected to PMA at 300 °C in \( \text{N}_2 \) atmosphere, reported by Ando et al. [147]. In (a,b), the transfer characteristics of MIS-HEMTs with and without PMA are compared in a semi-log scale and as a function of the gate overdrive voltage, respectively. Transfer curves in (c,d) were obtained after applying an initial gate voltage stress up to 10 V and by increasing the temperature up to 150 °C, respectively.
As in the case of the surface and annealing treatments, various strategies in the fabrication process of the devices can also be adopted to influence the trap states at the interface and, therefore, suppress the $V_{th}$ instability. Szabó et al. [31] reported that for MIS-HEMTs where the deposition of the Al$_2$O$_3$ gate dielectric was performed before the ohmic contacts formation and at annealing temperature of 650 °C resulted in an improvement of the $V_{th}$ stability compared to devices where the Al$_2$O$_3$ was deposited after the ohmic contacts formation was obtained with a high temperature anneal of 850 °C. It was suggested that this result was a consequence of a better Al$_2$O$_3$/AlGaN interface quality. Nakazawa et al. [165] applied an interesting approach based on the selective area regrowth of AlGaN to reduce the impact on the ALD-Al$_2$O$_3$/AlGaN interface of the dry etching process used for the fabrication of normally off AlGaN/GaN MIS-HEMTs with recessed gate structures. With this approach, they reported a reduced $V_{th}$ instability compared to Al$_2$O$_3$-gated MIS-HEMTs with dry-etched recessed gates.

Trapping mechanisms related to the gate dielectric can lead to the failure of the device. For this reason, reliability tests of the gate dielectric are also essential to bring the MIS-HEMT devices to industrial maturity. In this regard, Meneghesso et al. [30] performed an extensive analysis of trapping mechanisms and the reliability issues of AlGaN/GaN MIS-HEMTs using different insulators. They reported a significant correlation between the dynamic $V_{th}$ shift and gate leakage currents under forward gate bias stress and suggested that trapping effects were determined by the electrons trapped in the gate insulator or at the AlGaN/insulator interface. Wu et al. [166] investigated the positive bias temperature instability (PBII) in hybrid GaN MIS-FETs. Since the defect distribution inside the ALD-Al$_2$O$_3$ was found to be centered at about 1.15 eV away from the conduction band of the GaN with a narrow spread in energy, the ALD-Al$_2$O$_3$ gate dielectric was suggested to be very promising to improve the PBII reliability. Meneghesso et al. [30] also measured the TDDB characteristics of MIS-HEMTs with Al$_2$O$_3$ as gate dielectrics. Since the time-to-failure of devices indicated a Weibull distribution with slopes larger than 1.0, they demonstrated high robustness for ALD-Al$_2$O$_3$. Similarly, a Weibull distribution with a slope of 2.87 was extracted from the TDDB measurements of the Al$_2$O$_3$-gated MIS structures by Wu et al. [134]. Huang et al. [127] also achieved good TDDB behavior and a high breakdown electric field of 8.5 MV cm$^{-1}$ in recessed-gate MIS-HEMTs with a gate dielectric stack consisting of 13 nm of ALD-Al$_2$O$_3$ deposited using O$_3$ as an oxygen source and grown on top of 2 nm of ALD-Al$_2$O$_3$ deposited using a H$_2$O oxygen source. For the ALD-Al$_2$O$_3$ films on the GaN, Kachi et al. [167] reported a TDDB lifetime at RT and 150 °C of more than 20 years at an electric field of 3 MV cm$^{-1}$. Kikuta et al. [168] obtained a time-to-breakdown for the ALD-Al$_2$O$_3$ on a dry-etched GaN of more than 40,000 years at 3 MV cm$^{-1}$ and RT. In contrast, a time-to-breakdown of only $10^2$–$10^3$ s was obtained at 250 °C, which was suggested to be caused by large TAT leakage currents.

As mentioned before, the dielectric layer employed in MIS-HEMTs can be used both as a gate dielectric and a passivation layer to reduce current collapse. Hashizume et al. [53, 75] first demonstrated the use of an Al$_2$O$_3$ layer as a gate dielectric and a passivation scheme to control the current collapse in AlGaN/GaN HEMTs. Moreover, comparing the effects of surface passivation on MIS-HEMTs and Schottky-gate HEMTs, Tajima and Hashizume [169] showed a more pronounced reduction of the current collapse in Al$_2$O$_3$-gated MIS-HEMTs in contrast to Schottky-gated HEMTs, with Al$_2$O$_3$ serving only as a surface passivation. The suppression of the current collapse with a passivation layer, arising from negative surface charges, injected from gate edges to surface states was generally attributed to a reduction of electronic states at the AlGaN surface and of the peak field near the gate edge. Park et al. [94] reported for the first time on the use of Al$_2$O$_3$ deposited by ALD as a gate dielectric and passivation layer for AlGaN/GaN MIS-HEMTs. Park et al. [94] and Ye et al. [23] reported on the excellent electrical characteristics of AlGaN/GaN MIS-HEMTs using ALD-Al$_2$O$_3$ as a gate dielectric and passivation layer. Despite the improvements obtained by Al$_2$O$_3$-based passivation schemes for MIS-HEMT devices, further work is still required to limit and...
fully understand the current collapse phenomena in GaN transistors [1]. A more detailed overview about surface passivation for GaN-based transistors can be found in [29,49–51].

3.3. Modified Al$_2$O$_3$ Gate Dielectrics

Besides the use of pure Al$_2$O$_3$ films, other approaches involving the use of Al$_2$O$_3$-based bilayer gate stack dielectrics, interface engineering techniques or Al$_2$O$_3$-based compound materials have been investigated to combine the properties of Al$_2$O$_3$ with the favorable properties of other dielectric materials.

Kambayashi et al. [170] applied a SiO$_2$/Al$_2$O$_3$ gate stack (layers indicated from top to bottom) in hybrid GaN MIS-FETs, thus demonstrating a high-performance device with a channel mobility of 192 cm$^2$/Vs. Using a SiO$_2$/Al$_2$O$_3$ gate stack, Guo and del Alamo [171,172] studied the origin of PBTI and negative bias temperature instability (NBTI) in hybrid GaN MIS-FETs. It was shown that for a composite SiO$_2$/Al$_2$O$_3$ gate oxide, the resulting $V_{th}$ shifts are due to electron trapping or detrapping in pre-existing oxide traps and the generation of oxide traps near the oxide/GaN interface. Van Hove et al. [173] applied an ALD-Al$_2$O$_3$/in situ MOCVD-Si$_3$N$_4$ gate bilayer stack in AlGaN/GaN MIS-HEMTs to achieve excellent electrical device characteristics with lower gate leakage currents, more stable threshold voltages and reduced current collapse when compared to Al$_2$O$_3$-gated MIS-HEMTs. Capriotti et al. [174] investigated the fixed interface charges between the AlGaN and the Al$_2$O$_3$/in situ Si$_3$N$_4$ gate stack of AlGaN/GaN MIS-HEMTs. Colon and Shi [90] fabricated AlGaN/GaN MIS-HEMTs with low gate leakage currents using an ALD-HfO$_2$/Al$_2$O$_3$ bilayer stack as well as an ALD-HfAlO$_x$ ternary compound as gate dielectrics to achieve a higher dielectric constant than Al$_2$O$_3$ and a higher conduction band offset, thermal stability and crystallization temperature than HfO$_2$. However, both the HfO$_2$/Al$_2$O$_3$ and HfAlO$_x$-gated MIS-HEMTs still showed low transconductance, high interface state density and pronounced current collapse. The energy band alignment of MOCVD-HfAlO to GaN was investigated by Liu et al. [175,176], reporting a conduction band offset of 2.2 eV and minimum values of interface trap density in the range of 1–3 x 10$^{11}$ cm$^{-2}$ eV$^{-1}$ at the HfAlO/GaN interface. Hatano et al. [177] demonstrated reduced gate leakage and the improved operation and thermal stability of AlGaN/GaN MIS-HEMTs using a ZrO$_2$/Al$_2$O$_3$ gate stack dielectric.

Other approaches based on the use of Al$_2$O$_3$-based composite materials have also been reported. Partida-Manzanera et al. [178] investigated the potential of a ternary phase of Ta$_2$O$_5$ and Al$_2$O$_3$ as gate dielectrics to achieve higher permittivity than Al$_2$O$_3$, and hence enhance the transconductance of AlGaN/GaN MIS-HEMTs. Although a higher transconductance and reduced gate leakage current were achieved, the C–V curves did not feature the characteristic step at the forward bias in the spill-over regime, indicating a high density of trap states at the dielectric/AlGaN interface. Kikuta et al. [179] applied Al$_2$O$_3$/SiO$_2$ nanolaminate films deposited by ALD on GaN to obtain a gate dielectric material with a larger conduction band offset to GaN and a higher crystallization temperature than pure Al$_2$O$_3$ films in order to reduce gate leakage currents. The composition of Al and Si in the oxide and the resulting oxide properties of the permittivity, breakdown field and leakage currents could be controlled and tuned by the numbers of ALD cycles. Compared to pure Al$_2$O$_3$ films, a higher breakdown field and better reliability were obtained for the SiO$_2$ composition, from 0.21 to 0.69. Similarly, Mitrovic et al. [180] suggested that Al$_2$O$_3$/TiO$_2$ nanolaminates can also be favorable as gate dielectrics, and they very recently investigated the band alignment to the GaN and the permittivity of the Al$_2$O$_3$ layers doped with Ti, corresponding to Ti$_x$Al$_{1-x}$O$_y$. Although the permittivity of Ti$_x$Al$_{1-x}$O$_y$ increased significantly with the increasing Ti content, a small conduction band offset for all compositions was obtained. However, Le et al. [181,182] reported excellent characteristics with good insulating properties for MIS-HEMTs using AlTiO deposited by ALD as a gate dielectric.

Current research has also focused on the “doping” by fluorine ions (F$^-$) of Al$_2$O$_3$ gate dielectric films in order to control the threshold voltage of MIS-HEMTs towards normally off operation [183,184]. The latter can be obtained by implanting F$^-$ ions into the AlGaN
barrier prior to the dielectric ALD. After the ALD-Al₂O₃ deposition, the incorporated F⁻ ions can act as a source of negative fixed charges, compensating the intrinsic positive charges in the dielectric and shifting the V_{th} of the device in positive bias direction. It is worth mentioning that a previous physical approach based on the fluorine incorporation via plasma etching under the gate to shift the device threshold voltage was demonstrated by Cai et al. [185]. Using an ALD-Al₂O₃ gate dielectric combined with a fluorine-based plasma treatment, Chu et al. [186] demonstrated normally off Al₂O₃-gated MIS-HEMTs with a breakdown voltage of 1200 V.

An interesting process was used by Liu et al. [79] and Yang et al. [187], who improved the performance and the V_{th} stability of the Al₂O₃-gated hybrid MIS-FETs by inserting a monocrystalline AlN interfacial layer via plasma-enhanced atomic layer deposition (PEALD) at the Al₂O₃/GaN interface to block oxygen from the GaN surface and prevent the formation of oxygen-related interface traps. Al₂O₃/AlN/GaN structures showed a small frequency dispersion in the C–V curves and a D_i in the range of 10^{11}–10^{12} cm⁻² eV⁻¹, determined using the conventional conductance method. Similarly, Yang et al. [188] and Chen et al. [189] used an in situ low-damage plasma treatment based on NH₃ and N₂ prior to the ALD-Al₂O₃ deposition to effectively remove the native oxide while forming an ultrathin monocrystal-like nitridation interlayer (NIL) at the Al₂O₃/GaN interface. The N₂ plasma treatment was also demonstrated to compensate for the V_{th}-related defects at the surface. After a PDA was carried out at 500 °C in O₂ ambient, the Al₂O₃/NIL-gated MIS structures showed a lower interface trap density in the range of 1–6 × 10¹² cm⁻² eV⁻¹, resulting in AlGaN/GaN MIS-HEMTs with improved performance [189].

Finally, a very promising approach proposed by Asahara et al. [190] consists in using a sputtered AlION film as a gate dielectric, obtained by introducing nitrogen into Al₂O₃. An atomically abrupt high quality AlION/AlGaN interface with extremely low D_i values ranging from 1.2 to 1.4 × 10¹¹ cm⁻² eV⁻¹ and improved bulk properties were achieved, resulting in excellent C–V characteristics with negligible frequency dispersions and a markedly suppressed gate leakage current. Similar results were obtained by Wang et al. [191], who deposited AlION films by inserting thin AlN alternating layers into Al₂O₃. As shown in Figure 7, Ueda et al. [192] very recently applied AlION films deposited by ALD combined to a PDA in O₂ for shifting the V_{th} so to realize the normally off operation in the recessed-gate AlGaN/GaN MIS-HEMTs, with a negligible hysteresis in the transfer characteristics, a reduced off-state leakage current, a breakdown voltage of 730 V, an on-state resistance of 270 mΩ for a 10 A drain current rating and impressive switching performance, indicating the great potential of AlION as gate dielectric technology.

Figure 7. Transfer and output characteristics of recessed-gate AlGaN/GaN MIS-HEMTs using AlION as gate dielectric and subjected to PDA in O₂ atmosphere, reported by Ueda et al. [192]. The positive shift of V_{th} obtained by O₂ annealing for the AlION-gated transistor is shown in (a), while (b) reports the transfer curves without hysteresis obtained after applying a maximum gate voltage up to 10 V. The output characteristics of AlION-gated MIS-HEMTs in the on-state and off-state are shown in (c,d), respectively.
4. Nitride-Based Dielectrics

Despite the potentiality of $\text{Al}_2\text{O}_3$ and $\text{Al}_2\text{O}_3$-based dielectric materials, other insulators have emerged as suitable candidates for insulated-gate GaN-based transistors [1,29]. Among them, nitride-based dielectrics are of particular interest compared to oxide-based insulators because of the suppression of the Ga-O bonds that tend to induce interface traps [187].

$\text{SiN}_x$ deposited by in situ MOCVD or LPCVD has been widely demonstrated to be very promising both as a gate dielectric and a surface passivation [29,49]. In particular, in situ $\text{SiN}_x$ enables the dielectric deposition without exposing the (Al)GaN surface to air, which prevents the oxidation of the surface and passivates the surface states, possibly reducing the interface traps. Ogawa et al. [193] demonstrated that the in situ process of $\text{SiN}_x$ can realize an oxide free $\text{SiN}_x$/AlGaN interface. Takizawa et al. [194] reported high-resolution TEM analysis revealing abrupt interfaces between $\text{SiN}_x$ and AlGaN. Jiang et al. [78] systematically investigated MIS structures and MIS-HEMTs using in situ MOCVD-$\text{SiN}_x$ as a gate dielectric. A $D_{it}$ in the range of $2\times10^{12}$ cm$^{-2}$ eV$^{-1}$ was obtained, which resulted in a stable $V_{th}$ under gate bias and thermal stress. Derluyn et al. [195] reported that the reduction of surface states with in situ $\text{SiN}_x$ passivation of HEMT structures led to higher 2DEG density and lower current collapse. Moens et al. [196] even reported on MIS-HEMTs for 650 V applications with excellent interface quality and dielectric reliability using MOCVD-grown in situ $\text{SiN}_x$, which demonstrated a maximum gate voltage of $\sim$3.1 V at 10 years for a 100 ppm failure rate. LPCVD-$\text{SiN}_x$ has the advantages of a large conduction band offset to GaN ($\sim$2.3 eV), a relatively high dielectric constant (~7) and a low defects density enabled by the high deposition temperature. Moreover, compared to plasma-enhanced chemical vapor deposition (PECVD)-$\text{SiN}_x$, LPCVD-$\text{SiN}_x$ is free of plasma-induced damage and exhibits low oxygen contamination. In this regard, Hua et al. [197] reported on the superior properties of LPCVD-$\text{SiN}_x$ in terms of the leakage currents, breakdown field and TDBB lifetime. Similar investigations were performed by Jauss et al. [198], who predicted a 20-year 100 ppm lifetime at 130 °C for a gate voltage of 10.1 V. However, the high deposition temperature of more than 700 °C for LPCVD-$\text{SiN}_x$ can instead degrade the GaN surface in recessed-gate structures employed for normally off operations [48]. To overcome this issue, Hua et al. [48] successfully employed an interface protection technique consisting of a $\text{SiN}_x$ interlayer deposited by PECVD prior to the high-temperature deposition process of LPCVD-$\text{SiN}_x$. With this approach, normally off hybrid MIS-FETs using high-quality LPCVD-$\text{SiN}_x$ with a gate breakdown voltage of 21 V, a maximum gate bias of 11 V at failure rate of 63.2% for a 10-year lifetime, a stable $V_{th}$ and a small current collapse were demonstrated. A similar approach has been also applied by Jiang et al. [78], who instead used in situ $\text{SiN}_x$ in conjunction with PECVD $\text{SiN}_x$ as a passivation scheme to effectively suppress the current collapse in MIS-HEMTs. Finally, it is worth mentioning that for normally off hybrid MIS-FETs, Hue et al. [42] recently developed another promising technique to protect the etched-GaN surface during the LPCVD-$\text{SiN}_x$ high temperature deposition. This is based on an oxygen-plasma treatment followed by in situ annealing prior to the LPCVD to form a sharp and stable crystalline oxidation interlayer (COIL) protecting the surface. LPCVD-$\text{SiN}_x$-gated hybrid MIS-FETs with a COIL revealed a stable $V_{th}$ and a highly reliable gate dielectric.

$\text{AlN}$ is another promising nitride-based material which is attractive as a gate dielectric for insulated-gate GaN-based transistors due to its large bandgap, resulting in a high breakdown field, high permittivity and small mismatch to GaN, which might reduce the trap states at the AlN/(Al)GaN interface. $\text{AlN}$ is mainly grown by MOCVD or PEALD techniques [199]. Hashizume et al. [200] were the first to report the low values of $D_{it}$ in the range of $1\times10^{11}$ cm$^{-2}$ eV$^{-1}$ at the MOCVD-$\text{AlN}$/GaN interface. Huang et al. [81] revealed an atomically sharp interface between the PEALD-$\text{AlN}$ and AlGaN. They also demonstrated that polarization charges in the monocrystal-like $\text{AlN}$ used as a passivation layer can effectively compensate the interface traps at the AlN/(Al)GaN interface, significantly reducing current collapse and the on-resistance degradation in ALD-$\text{AlN}$-passivated
AlGaN/GaN HEMTs. Polarization charges in monocrystalline thin AlN layers have also been reported to affect the $V_{th}$ of hybrid MIS-FETs [79]. The high thermal conductivity of AlN has been also shown to be beneficial to suppress the self-heating of AlN-passivated HEMTs, thus improving the device performance [80]. AlN as passivation layer has also been demonstrated to improve the breakdown voltage of AlGaN/GaN HEMTs compared to SiN-passivated devices [201]. Very recently, Hwang et al. [202] reported a sharp interface between the GaN and PEALD-AlN. With the PEALD-AlN used as interfacial layer, they also successfully suppressed the surface oxidation of the GaN, which resulted in the improved C–V characteristics of AlN/GaN structures. AlGaN/GaN MIS-HEMTs and MIS structures using AlN deposited by a novel technique called low-temperature epitaxy (LTE) have been also recently investigated [199,203,204].

5. Summary

In this paper, we have summarized the most relevant challenges and recent progress on the development of a gate dielectric technology for insulated-gate GaN-based devices for high-frequency and high-power applications. Specifically, we first pointed out the important physical properties of the insulators which need to be considered for designing a MIS gate structure which delivers improved energy efficiency and reliable device performance. Afterwards, we highlighted that, regardless of the GaN transistor concept and the design, one of the major challenges arising from the insertion of a dielectric on (Al)GaN is represented by the trap states located at the dielectric/(Al)GaN interface or within the bulk dielectric. These trap states strongly affect the performance and the reliability of the device and need to be minimized to ensure high energy efficiency, safe operation and the long-term lifetime of the insulated-gate GaN-based transistors.

Among the various dielectrics, we focused our attention on Al$_2$O$_3$, which is one of the most promising dielectric materials due to its large bandgap and conduction band offset to (Al)GaN, its relatively high dielectric constant, its high breakdown electric field and its thermal and chemical stability against (Al)GaN. In particular, we pointed out that despite the technological progress in the ALD process, enabling the fabrication of high-quality Al$_2$O$_3$ films and of Al$_2$O$_3$-gated devices with improved and reliable performance, a large amount of defects and trap states at the Al$_2$O$_3$/(Al)GaN interface is still present and still degrades the device performance. In this regard, the main results obtained in the literature of the interface state density distribution at the Al$_2$O$_3$/(Al)GaN interface are presented and discussed in detail, and the recent progress in the performance of the Al$_2$O$_3$-gated MIS-HEMTs are reviewed.

Finally, novel Al$_2$O$_3$-based dielectric or compound materials and interface engineering approaches involving the use of Al$_2$O$_3$, which have been exploited to improve the quality and electrical performance of Al$_2$O$_3$-gate MIS structures, have been presented. Among them, AlON, or the use of nitride-based interface control layers have been demonstrated to be the most promising techniques. In addition to that, nitride-based dielectric materials have also been briefly presented as promising candidates, especially driven by their potential to function both as a gate dielectric as well as a passivation layer.

The insights of this paper help to understand the current status and the recent progress of the Al$_2$O$_3$ gate dielectric technology for insulated-gate GaN-based transistors. It also highlights that the current state of the art has made great advancements, but still requires remarkable progress in terms of gate dielectric, gate stack engineering and interface control technology. Focused efforts are still needed in order to ensure a low interface and bulk trap density, thus enabling a robust reliability under stringent and dynamic electrical stresses. Further advances in the gate dielectric technologies are necessary to overcome these obstacles and to pave the way for the massive advent of insulated-gate GaN-based technologies in the electronic market.

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References
1. Amano, H.; Baines, Y.; Beam, E.; Borga, M.; Bouchet, T.; Chalker, P.R.; Charles, M.; Chen, K.J.; Chowdhury, N.; Chu, R. The 2018 GaN Power Electronics Roadmap. J. Phys. D Appl. Phys. 2018, 51, 163001. [CrossRef]
2. Hassan, A.; Savaria, Y.; Sawan, M. GaN Integration Technology, an Ideal Candidate for High-Temperature Applications: A Review. IEEE Access 2016, 8, 78790–78802. [CrossRef]
3. Okumura, H. Present Status and Future Prospect of Widegap Semiconductor High-Power Devices. Jpn. J. Appl. Phys. 2006, 45, 7565. [CrossRef]
4. Ambacher, O.; Dimitrov, R.; Stutzmann, M.; Foutz, B.E.; Murphy, M.J.; Smart, J.A.; Shealy, J.R.; Weimann, N.G.; Chu, K.; Chumbes, M.; et al. Role of Spontaneous and Piezoelectric Polarization Induced Effects in Group-III Nitride Based Heterostructures and Devices. Phys. Status Solidi B 1999, 216, 381–389. [CrossRef]
5. Ambacher, O.; Smart, J.; Shealy, J.R.; Weimann, N.G.; Chu, K.; Murphy, M.; Schaff, W.J.; Eastman, L.F.; Dimitrov, R.; Wittmer, L. Two-Dimensional Electron Gases Induced by Spontaneous and Piezoelectric Polarization Charges in N-and Ga-Face AlGaN/GaN Heterostructures. J. Appl. Phys. 1999, 85, 3222–3233. [CrossRef]
6. Ambacher, O.; Foutz, B.; Smart, J.; Shealy, J.R.; Weimann, N.G.; Chu, K.; Murphy, M.; Sierakowski, A.J.; Schaff, W.J.; Eastman, L.F.; et al. Two Dimensional Electron Gases Induced by Spontaneous and Piezoelectric Polarization in Undoped and Doped AlGaN/GaN Heterostructures. J. Appl. Phys. 2000, 87, 334–344. [CrossRef]
7. Roccaforte, F.; Fiorenza, P.; Greco, G.; Nigro, R.L.; Giannazzo, F.; Patti, A.; Saggio, M. Challenges for Energy Efficient Wide Band Gap Semiconductor Power Devices. Phys. Status Solidi A 2014, 211, 2063–2071. [CrossRef]
8. Flack, T.J.; Pushpakaran, B.N.; Bayne, S.B. GaN Technology for Power Electronic Applications: A Review. J. Electron. Mater. 2016, 45, 2673–2682. [CrossRef]
9. Trescases, O.; Murray, S.K.; Jiang, W.L.; Zaman, M.S. GaN Power ICs: Reviewing Strengths, Gaps, and Future Directions. In Proceedings of the 2020 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 12–18 December 2020; pp. 27.4.1–27.4.4. [CrossRef]
10. Hsu, L.-H.; Lai, Y.-Y.; Tu, P.-T.; Langpoklakpam, C.; Chang, Y.-T.; Huang, Y.-W.; Lee, W.-C.; Tzou, A.-J.; Cheng, Y.-J.; Lin, C.-H.; et al. Development of GaN HEMTs Fabricated on Silicon, Silicon-on-Insulator, and Engineered Substrates and the Heterogeneous Integration. Micromachines 2021, 12, 1159. [CrossRef]
11. Chowdhury, S.; Swenson, B.L.; Mishra, U.K. Enhancement and Depletion Mode AlGaN/GaN CAVET with Mg-Ion-Implanted GaN as Current Blocking Layer. IEEE Electron Device Lett. 2009, 29, 543–545. [CrossRef]
12. Yeluri, R.; Lu, J.; Hurni, C.A.; Browne, D.A.; Chowdhury, S.; Keller, S.; Speck, J.S.; Mishra, U.K. Design, Fabrication, and Performance Analysis of GaN Vertical Electron Transistors with a Buried p/n Junction. Appl. Phys. Lett. 2015, 106, 183502. [CrossRef]
13. Ji, D.; Agarwal, A.; Li, H.; Li, W.; Keller, S.; Chowdhury, S. 880 V/2.7 mΩ·cm² MIS Gate Trench CAVET on Bulk GaN Substrates. IEEE Electron Device Lett. 2018, 39, 863–865. [CrossRef]
14. Tang, Y.; Shinohara, K.; Regan, D.; Corrion, A.; Brown, D.; Wong, J.; Schmitz, A.; Fung, H.; Kim, S.; Micovic, M. Ultrahigh-Speed GaN High-Electron-Mobility Transistors with $f_t/f_{max}$ of 454/444 GHz. IEEE Electron Device Lett. 2015, 36, 549–551. [CrossRef]
15. Shinohara, K.; Regan, D.C.; Tang, Y.; Corrion, A.L.; Brown, D.E.; Wong, J.C.; Robinson, J.F.; Fung, H.H.; Schmitz, A.; Oh, T.C.; et al. Scaling of GaN HEMTs and Schottky Diodes for Submillimeter-Wave MMIC Applications. IEEE Trans. Electron Devices 2013, 60, 2982–2996. [CrossRef]
16. Lv, Y.; Song, X.; Guo, H.; Fang, Y.; Feng, Z. High-Frequency AlGaN/GaN HFETs with $f_t/f_{max}$ of 149/263 GHz for D-Band PA Applications. Electron. Lett. 2016, 52, 1340–1342. [CrossRef]
17. Lee, D.S.; Laboutin, O.; Cao, Y.; Johnson, W.; Beam, E.; Kettersson, A.; Schuette, M.; Saunier, P.; Palacios, T. Impact of Al2O3 Passivation Thickness in Highly Scaled GaN HEMTs. IEEE Electron Device Lett. 2012, 33, 976–978. [CrossRef]
18. Chung, J.W.; Kim, T.-W.; Palacios, T. Advanced Gate Technologies for State-of-the-Art $f_t$ in AlGaN/GaN HEMTs. In Proceedings of the 2010 International Electron Devices Meeting, San Francisco, CA, USA, 6–8 December 2010; pp. 30–32. [CrossRef]
19. Hashizume, T.; Kotani, J.; Hasegawa, H. Leakage Mechanism in GaN and AlGaN Schottky Interfaces. Appl. Phys. Lett. 2004, 84, 4884–4886. [CrossRef]
20. Greco, G.; Iucolano, F.; Roccaforte, F. Review of Technology for Normally-off HEMTs with p-GaN Gate. Mater. Sci. Semicond. Process. 2018, 78, 96–106. [CrossRef]
21. Lidow, A.; De Rooij, M.; Strydom, J.; Reusch, D.; Glaser, J. GaN Transistors for Efficient Power Conversion; John Wiley & Sons: Hoboken, NJ, USA, 2019.
22. Kanamura, M.; Kikkawa, T.; Iwai, T.; Imanishi, K.; Kubo, T.; Joshi, K. An over 100 W n-GaN/n-AlGaN/GaN MIS-HETP Power Amplifier for Wireless Base Station Applications. In Proceedings of the IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest, Washington, DC, USA, 5 December 2005; pp. 572–575. [CrossRef]

23. Ye, P.D.; Yang, B.; Ng, K.K.; Bude, J.; Wilk, G.D.; Halder, S.; Hwang, J.C.M. GaN Metal-Oxide-Semiconductor High-Electron-Mobility-Transistor with Atomic Layer Deposited Al2O3 as Gate Dielectric. Appl. Phys. Lett. 2005, 86, 063501. [CrossRef]

24. Khan, M.A.; Hu, X.; Sumin, G.; Lunev, A.; Yang, J.; Gaska, R.; Shur, M.S. AlGaN/GaN Metal Oxide Semiconductor Heterostructure Field Effect Transistor. IEEE Electron Device Lett. 2000, 21, 63–65. [CrossRef]

25. Chen, K.J.; Yang, S.; Liu, S.; Liu, C.; Hua, M. Toward Reliable MIS-and MOS-Gate Structures for GaN Lateral Power Devices. Phys. Status Solidi A 2016, 213, 861–867. [CrossRef]

26. Mizue, C.; Hori, Y.; Miczek, M.; Hashizume, T. Capacitance–Voltage Characteristics of Al2O3/AlGaN/GaN Structures and State Density Distribution at Al2O3/AlGaN Interface. Jpn. J. Appl. Phys. 2011, 50, 021001. [CrossRef]

27. Hori, Y.; Yatabe, Z.; Hashizume, T. Characterization of Interface States in Al2O3/AlGaN/GaN Structures for Improved Performance of High-Electron-Mobility Transistors. J. Appl. Phys. 2013, 114, 244503. [CrossRef]

28. Lu, X.; Yu, K.; Jiang, H.; Zhang, A.; Lau, K.M. Study of Interface Traps in AlGaN/GaN MISHETMs Using LPCVD SiNx as Gate Dielectric. IEEE Trans. Electron Devices 2017, 64, 824–831. [CrossRef]

29. Hashizume, T.; Nishiguchi, K.; Kaneki, S.; Kuzmik, J.; Yatabe, Z. State of the Art on Gate Insulation and Surface Passivation for GaN-Based Power HEMTs. Mater. Sci. Semicond. Process. 2018, 88, 75–85. [CrossRef]

30. Meneghesso, G.; Meneghini, M.; Bisi, D.; Rossetto, I.; Cester, A.; Mishra, U.K.; Zanoni, E. Trapping Phenomena in AlGaN/GaN HEMTs: A Study Based on Pulsed and Transient Measurements. Semicond. Sci. Technol. 2013, 28, 074021. [CrossRef]

31. Szabó, N.; Wachowiak, A.; Winzer, A.; Ocker, J.; Gärtner, J.; Hentschel, R.; Schmid, A.; Mikolajick, T. High-k/GaN Interface Engineering toward AlGaN/GaN MIS-HETM with Improved Vth Stability. J. Vac. Sci. Technol. B 2017, 35, 01A102. [CrossRef]

32. Ho, Y.; Yang, S.; Jiang, Q.; Tang, Z.; Li, B.; Chen, K.J. Characterization of Vt-Instability in Enhancement-Mode Al2O3-AlGaN/GaN MIS-HEMTs. Phys. Status Solidi C 2013, 10, 1397–1400. [CrossRef]

33. Zhu, J.; Hou, B.; Chen, L.; Zhu, Q.; Yang, L.; Zhou, X.; Zhang, P.; Ma, X.; Hao, Y. Threshold Voltage Shift and Interface/Border Trapping Mechanism in Al2O3/AlGaN/GaN MOS-HEMTs. In Proceedings of the 2018 IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, USA, 11–15 March 2018; p. P-WB. [CrossRef]

34. Winzer, A.; Schuster, M.; Hentschel, R.; Ocker, J.; Merkel, U.; Jahn, A.; Wachowiak, A.; Mikolajick, T. Analysis of Threshold Voltage Instability in AlGaN/GaN MIS-HEMTs by Forward Gate Voltage Stress Pulses. Phys. Status Solidi A 2016, 213, 1246–1251. [CrossRef]

35. Huang, S.; Yang, S.; Roberts, J.; Chen, K.J. Threshold Voltage Instability in Al2O3/AlGaN/GaN Metal-Insulator–Semiconductor High-Electron-Mobility Transistors. Jpn. J. Appl. Phys. 2011, 50, 110202. [CrossRef]

36. Lagger, P.; Ostermaier, C.; Pobegen, G.; Pogany, D. Towards Understanding the Origin of Threshold Voltage Instability of AlGaN/GaN MIS-HEMTs. In Proceedings of the 2012 International Electron Devices Meeting, San Francisco, CA, USA, 10–13 December 2012; pp. 13.1.1–13.1.4. [CrossRef]

37. Lagger, P.; Steinschifter, P.; Reiner, M.; Stadtmüller, M.; Denifl, G.; Naumann, A.; Müller, J.; Wilde, L.; Sundqvist, J.; Pogany, D.; et al. Role of the Dielectric for the Charging Dynamics of the Dielectric/Barrier Interface in AlGaN/GaN Based Metal-Insulator-Semiconductor Structures under Forward Gate Bias Stress. Appl. Phys. Lett. 2014, 105, 033512. [CrossRef]

38. Nishiguchi, K.; Kaneki, S.; Ozaki, S.; Hashizume, T. Current Linearity and Operation Stability in Al2O3-Gate AlGaN/GaN MOS High Electron Mobility Transistors. Jpn. J. Appl. Phys. 2017, 56, 101001. [CrossRef]

39. Huang, W.; Khan, T.; Chow, T.P. Enhancement-Mode n-Channel GaN MOSFETs on p and n-GaN/Sapphire Substrates. In Proceedings of the 2006 IEEE International Symposium on Power Semiconductor Devices and IC’s, Naples, Italy, 4–8 June 2006; pp. 1–4. [CrossRef]

40. Oka, T.; Ueno, Y.; Ina, T.; Hasegawa, K. Vertical GaN-Based Trench Metal Oxide Semiconductor Field-Effect Transistors on a Free-Standing GaN Substrate with Blocking Voltage of 1.6 kV. Appl. Phys. Express 2014, 7, 021002. [CrossRef]

41. Sun, M.; Zhang, Y.; Gao, X.; Palacios, T. High-Performance GaN Vertical Fin Power Transistors on Bulk GaN Substrates. IEEE Electron Device Lett. 2017, 38, 509–512. [CrossRef]

42. Hua, M.; Wei, J.; Tang, G.; Zhang, Z.; Qian, Q.; Cai, X.; Wang, N.; Chen, K.J. Normally-off LPCVD-SiNₓ/AlGaN MIS-FET with Crystalline Oxidation Interlayer. IEEE Electron Device Lett. 2017, 38, 929–932. [CrossRef]

43. Mukherjee, K.; De Santi, C.; Borga, M.; Geens, K.; You, S.; Bakeroott, B.; Decoutere, S.; Diehle, P.; Hübner, S.; Allmann, F.; et al. Challenges and Perspectives for Vertical GaN-on-Si Trench MOS Reliability: From Leakage Current Analysis to Gate Stack Optimization. Materials 2021, 14, 2316. [CrossRef][PubMed]

44. Hentschel, R.; Wachowiak, A.; Großer, A.; Kotzea, S.; Debald, A.; Kalisch, H.; Vescan, A.; Jahn, A.; Schmutl, S.; Mikolajick, T. Extraction of the Active Acceptor Concentration in (Pseudo-) Vertical GaN MOSFETs Using the Body-Bias Effect. Microelectron. J. 2019, 91, 42–45. [CrossRef]

45. Mukherjee, K.; De Santi, C.; Borga, M.; You, S.; Geens, K.; Bakeroott, B.; Decoutere, S.; Meneghesso, G.; Zanoni, E.; Meneghini, M. Use of Bilayer Gate Insulator in GaN-on-Si Vertical Trench MOSFETs: Impact on Performance and Reliability. Materials 2020, 13, 4740. [CrossRef]

46. Pérez-Tomás, A.; Placidi, M.; Baron, N.; Chenot, S.; Cordier, Y.; Moreno, J.C.; Constant, A.; Godignon, P.; Millán, J. GaN Transistor Characteristics at Elevated Temperatures. J. Appl. Phys. 2009, 106, 074519. [CrossRef]
47. Pérez-Tomás, A.; Placidi, M.; Perpiñá, X.; Constant, A.; Godignon, P.; Jordà, X.; Brosselard, P.; Millán, J. GaN Metal-Oxide-Semiconductor Field-Effect Transistor Inversion Channel Mobility Modeling. *J. Appl. Phys.* 2009, 105, 114510. [CrossRef]

48. Hua, M.; Zhang, Z.; Wei, J.; Lei, J.; Tang, G.; Fu, K.; Cai, Y.; Zhang, B.; Chen, K.J. Integration of LPCVD-SiN$_x$ Gate Dielectric with Recessed-Gate E-Mode GaN MIS-FETs: Toward High Performance, High Stability and Long TDDB Lifetime. In Proceedings of the 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2016; pp. 10–14. [CrossRef]

49. Yatabe, Z.; Asubar, J.T.; Hashizume, T. Insulated Gate and Surface Passivation Structures for GaN-Based Power Transistors. *J. Phys. D Appl. Phys.* 2016, 49, 395001. [CrossRef]

50. Roccaforte, F.; Fiorenza, P.; Greco, G.; Vivona, M.; Nigro, R.L.; Giannazzo, F.; Patti, A.; Saggio, M. Recent Advances on Dielectrics Technology for SiC and GaN Power Devices. *Appl. Surf. Sci.* 2014, 301, 9–18. [CrossRef]

51. Eller, B.S.; Yang, J.; Nemanich, R.J. Electronic Surface and Dielectric Interface States on GaN and AlGaN. *J. Vac. Sci. Technol. A* 2013, 31, 050807. [CrossRef]

52. Vetury, R.; Zhang, N.Q.; Keller, S.; Mishra, U.K. The Impact of Surface States on the DC and RF Characteristics of AlGaN/GaN HFETs. *IEEE Trans. Electron Devices* 2001, 48, 560–566. [CrossRef]

53. Hashizume, T.; Ootomo, S.; Hasegawa, H. Suppression of Current Collapse in Insulated Gate AlGaN/GaN Heterostructure Field-Effect Transistors Using Ultrathin Al$_2$O$_3$ Dielectric. *Appl. Phys. Lett.* 2003, 83, 2952–2954. [CrossRef]

54. Green, B.M.; Li, Y.; Ng, K.K. *Dielectric of High K Gate Oxides on III-V Semiconductors.* John Wiley & Sons: Hoboken, NJ, USA, 2021.

55. Sze, S.M.; Li, Y.; Ng, K.K. *Physics of Semiconductor Devices;* McGraw-Hill: New York, NY, USA, 1998.

56. Robertson, J.; Falabretti, B. Band Offsets of High K Gate Oxides on III-V Semiconductors. *Appl. Surf. Sci.* 2006, 252, 7230–7234. [CrossRef]

57. Anderson, T.J.; Wheeler, V.D.; Shahin, D.I.; Tadjer, M.J.; Koehler, A.D.; Hobart, K.D.; Christou, A.; Kub, F.J.; Eddy, C.R., Jr. Enhancement Mode AlGaN/GaN MOS-HEMTs. *IEEE Trans. Electron Devices* 2001, 48, 533–534. [CrossRef]

58. Kambayashi, H.; Satoh, Y.; Ootomo, S.; Kokawa, T.; Nomura, T.; Kato, S.; Chow, T.P.; Over 100 A Operation Normally-off AlGaN/GaN HEMTs. *IEEE Electron Device Lett.* 2000, 21, 268–270. [CrossRef]

59. Zee, S.M.; Li, Y.; Ng, K.K. *Physics of Semiconductor Devices;* John Wiley & Sons: Hoboken, NJ, USA, 2021.

60. Liu, C.; Chor, E.F.; Tan, L.S. Investigations of HfO$_2$/AlGaN/GaN Metal-Oxide-Semiconductor High Electron Mobility Transistors. *Appl. Phys. Lett.* 2006, 88, 173504. [CrossRef]

61. Liu, C.; Chor, E.F.; Tan, L.S. Enhanced Device Performance of AlGaN/GaN HEMTs Using HfO$_2$ High-k Dielectric for Surface Passivation and Gate Oxide. *Semicond. Sci. Technol.* 2007, 22, 522. [CrossRef]

62. Shi, J.; Eastman, L.F.; Xin, X.; Pophristic, M. High Performance AlGaN/GaN Power Switch with HfO$_2$ Insulation. *Appl. Phys. Lett.* 2005, 86, 98–100. [CrossRef]

63. Ye, G.; Wang, H.; Arulkumaran, S.; Ng, G.I.; Hofstetter, R.; Li, Y.; Anand, M.J.; Ang, K.S.; Maung, Y.K.T.; Foo, S.C. Atomic Layer Deposition of ZrO$_2$ as Gate Dielectrics for AlGaN/GaN Metal-Insulator-Semiconductor High Electron Mobility Transistors on Silicon. *Appl. Phys. Lett.* 2013, 103, 142109. [CrossRef]

64. Anderson, T.J.; Wheeler, V.D.; Shahin, D.I.; Tadjer, M.J.; Koehler, A.D.; Hobart, K.D.; Christou, A.; Kub, F.J.; Eddy, C.R., Jr. Enhancement Mode AlGaN/GaN MOS-HEMTs. *IEEE Electron Device Lett.* 2000, 21, 268–270. [CrossRef]

65. Anderson, T.J.; Wheeler, V.D.; Shahin, D.I.; Tadjer, M.J.; Koehler, A.D.; Hobart, K.D.; Christou, A.; Kub, F.J.; Eddy, C.R., Jr. Enhancement Mode AlGaN/GaN MOS-HEMTs. *IEEE Electron Device Lett.* 2000, 21, 268–270. [CrossRef]

66. Kikkawa, T.; Makiyama, K.; Ohki, T.; Kanamura, M.; Imanishi, K.; Hara, N.; Yoshin, K. High Performance and High Reliability AlGaN/GaN HEMTs. *Phys. Status Solidi A* 2009, 206, 1135–1144. [CrossRef]

67. Deen, D.A.; Storm, D.F.; Bass, R.; Meyer, D.J.; Katzer, D.S.; Binari, S.C.; Lacis, J.W.; Gouguets, T. Atomic Layer Deposited Ta$_2$O$_5$ Gate Insulation for Enhancing Breakdown Voltage of AlN/GaN High Electron Mobility Transistors. *Appl. Phys. Lett.* 2011, 98, 023506. [CrossRef]

68. Fiorenza, P.; Greco, G.; Fisichella, G.; Roccaforte, F.; Malandrino, G.; Lo Nigro, R. High Permittivity Cerium Oxide Thin Films on AlGaN/GaN Heterostructures. *Appl. Phys. Lett.* 2013, 103, 112905. [CrossRef]

69. Chiu, Y.S.; Liao, J.T.; Lin, Y.C.; Liu, S.C.; Lin, T.M.; Iwai, H.; Kakushina, K.; Chang, E.Y. High-Permittivity Cerium Oxide Prepared by Molecular Beam Deposition as Gate Dielectric and as Passivation Layer Applied to AlGaN/GaN Power High Electron Mobility Transistor Devices. *Jpn. J. Appl. Phys.* 2016, 55, 051001. [CrossRef]

70. Su, C.-H.; Shih, W.-C.; Lin, Y.-C.; Su, H.-T.; Su, H.-H.; Huang, Y.-X.; Lin, T.-W.; Wu, C.-H.; Wu, W.-H.; Maa, J.-S.; et al. Improved Linearity and Reliability in GaN Metal–Oxide–Semiconductor High-Electron-Mobility Transistors Using Nanolaminate La$_2$O$_3$/SiO$_2$ Gate Dielectric. *Jpn. J. Appl. Phys.* 2016, 55, 04EG04. [CrossRef]

71. Hansen, P.J.; Vaithyanathan, V.; Wu, Y.; Mates, T.; Heikman, S.; Mishra, U.K.; York, R.A.; Schlom, D.G.; Speck, J.S. Rutilite Films Grown by Molecular Beam Epitaxy on GaN and AlGaN/GaN *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct. Process. Meas. Phenom.* 2005, 23, 499–506. [CrossRef]

72. Rawat, A.; Meek, M.; Kumar Surana, V.; Bhardwaj, N.; Pendem, V.; Garigapati, N.S.; Yadav, Y.; Ganguly, S.; Saha, D. Thermally Grown TiO$_2$ and Al$_2$O$_3$ for GaN-Based MOS-HEMTs. *IEEE Trans. Electron Devices* 2018, 65, 3725–3731. [CrossRef]
99. Toyoda, S.; Shinohara, T.; Kumiugashira, H.; Oshina, M.; Kato, Y. Significant Increase in Conductance Band Discontinuity due to Solid Phase Epitaxy of Al$_2$O$_3$ Gate Insulator Films on GaN Semiconductor. *Appl. Phys. Lett.* **2012**, *101*, 231607. [CrossRef]
100. Yang, J.; Eller, B.S.; Zhu, C.; England, C.; Nemanich, R.J. Comparative Band Alignment of Plasma-Enhanced Atomic Layer Deposited High-k Dielectrics on Gallium Nitride. *J. Appl. Phys.* **2012**, *112*, 053710. [CrossRef]
101. Costina, I.; Franchy, R. Band Gap of Amorphous and Well-Ordered Al$_2$O$_3$ on Ni$_3$Al(100). *Appl. Phys. Lett.* **2001**, *78*, 4139–4141. [CrossRef]
102. French, R.H. Electronic Band Structure of Al$_2$O$_3$, with Comparison to AlON and AlN. *J. Am. Ceram. Soc.* **1990**, *73*, 477–489. [CrossRef]
103. Maeda, N.; Wang, C.; Enoki, T.; Makimoto, T.; Tarawa, T. High Drain Current Density and Reduced Gate Leakage Current in Channel-Doped AlGaN/GaN Heterostructure Field-Effect Transistors with Al$_2$O$_3$/Si$_3$N$_4$ Gate Insulator. *Appl. Phys. Lett.* **2005**, *87*, 073504. [CrossRef]
104. Gregušová, D.; Stoklas, R.; Čičo, K.; Heidelberger, G.; Marso, M.; Novák, J.; Kordoš, P. Characterization of AlGaN/GaN MOSFETs with Al$_2$O$_3$ as Gate Oxide. *Phys. Status Solidi C* **2007**, *4*, 2720–2723. [CrossRef]
105. Štapajna, M.; Jurkovič, M.; Válik, L.; Haščík, Š.; Gregušová, D.; Brunner, F.; Cho, E.-M.; Kuzmík, J. Bulk and Interface Trapping in the Gate Dielectric of GaN Based Metal-Oxide-Semiconductor High-Electron-Mobility Transistors. *Appl. Phys. Lett.* **2013**, *102*, 243509. [CrossRef]
106. Gregušová, D.; Stoklas, R.; Čičo, K.; Heidelberger, G.; Marso, M.; Novák, J.; Kordoš, P. Characterization of AlGaN/GaN MOSFETs with Al$_2$O$_3$ as Gate Oxide. *Phys. Status Solidi C* **2007**, *4*, 2720–2723. [CrossRef]
107. Esposto, M.; Krishnamoorthy, S.; Nath, D.N.; Bajaj, S.; Hung, T.-H.; Rajan, S. Electrical Properties of Atomic Layer Deposited Aluminum Oxide on Gallium Nitride. *Appl. Phys. Lett.* **2011**, *99*, 133503. [CrossRef]
108. Hori, Y.; Mizue, C.; Hashizume, T. Process Conditions for Improvement of Electrical Properties of Al$_2$O$_3$/n-GaN Structures Prepared by Atomic Layer Deposition. *Jpn. J. Appl. Phys.* **2010**, *49*, 080201. [CrossRef]
109. Suri, R. Investigation of MOS Interfaces with Atomic-Layer-Deposited High-k Gate Dielectrics on III-V Semiconductors. Ph.D. Thesis, North Carolina State University, Raleigh, NC, USA, 2010.
110. Zhang, Z.; Jackson, C.M.; Arehart, A.R.; McSkimming, B.; Speck, J.S.; Ringel, S.A. Direct Determination of Energy Band Alignments of Ni/Al$_2$O$_3$/GaN Based Metal Structures Using Internal Photoemission Spectroscopy. *J. Electron. Mater.* **2014**, *43*, 828–832. [CrossRef]
111. Yang, J.; Eller, B.S.; Nemanich, R.J. Surface Band Bending and Band Alignment of Plasma Enhanced Atomic Layer Deposited Dielectrics on Ga- and N-face Gallium Nitride. *J. Appl. Phys.* **2014**, *116*, 123702. [CrossRef]
112. Qin, X.; Cheng, L.; McDonnell, S.; Azcatl, A.; Zhu, H.; Kim, J.; Wallace, R.M. A Comparative Study of Atomic Layer Deposition of Al$_2$O$_3$ and HfO$_2$ on AlGaN/GaN. *J. Mater. Sci. Mater. Electron.* **2015**, *26*, 4638–4643. [CrossRef]
113. Winiar, A.; Szabó, N.; Ocker, J.; Hentschel, R.; Schuster, M.; Schubert, F.; Gärtner, J.; Wachowiak, A.; Mikolajick, T. Detailed Analysis of Oxide Related Charges and Metal-Oxide Barriers in Terrace Etched Al$_2$O$_3$ and HfO$_2$ on AlGaN/GaN Heterostructure Capacitors. *J. Appl. Phys.* **2015**, *118*, 124106. [CrossRef]
114. Hashizume, T.; Kaneki, S.; Oyobiki, T.; Ando, Y.; Sasaki, S.; Nishiguchi, K. Effects of Postmetallization Annealing on Interface Properties of Al$_2$O$_3$/GaN Structures. *Appl. Phys. Express* **2018**, *11*, 124102. [CrossRef]
115. Kaneki, S.; Ohira, J.; Toiya, Y.; Yabe, T.; Asohar, J.T.; Hashizume, T. Highly-Stable and Low-State-Density Al$_2$O$_3$/GaN Interfaces Using Epitaxial n-GaN Layers Grown on Free-Standing GaN Substrates. *Appl. Phys. Lett.* **2016**, *109*, 162104. [CrossRef]
116. Son, J.; Chobpattana, V.; McSkimming, B.M.; Steemer, S. Fixed Charge in High-k/GaN Metal-Oxide-Semiconductor Capacitor Structures. *Appl. Phys. Lett.* **2012**, *101*, 102905. [CrossRef]
117. Uedono, A.; Nabatame, T.; Egger, W.; Koschine, T.; Hugenschmidt, C.; Dickmann, M.; Sumiya, M.; Ishibashi, S. Vacancy-Type Defects in Al$_2$O$_3$/GaN Structure Probed by Monoenergetic Positron Beams. *J. Appl. Phys.* **2018**, *123*, 155302. [CrossRef]
118. Kubo, T.; Miyoshi, M.; Egawa, T. Post-Deposition Annealing Effects on the Insulator/Semiconductor Interfaces of Al$_2$O$_3$/GaN Structures on Si Substrates. *Semicond. Sci. Technol.* **2017**, *32*, 065012. [CrossRef]
119. Hung, T.-H.; Krishnamoorthy, S.; Esposto, M.; Neelim Nath, D.; Sung Park, P.; Rajan, S. Interface Charge Engineering at Atomic Layer Deposited Dielectric/III-Nitride Interfaces. *Appl. Phys. Lett.* **2013**, *102*, 072105. [CrossRef]
120. Zhou, H.; Ng, G.I.; Liu, Z.H.; Arul Kumaran, S. Improved Device Performance by Post-Oxide Annealing in Atomic-Layer-Deposited Al$_2$O$_3$/GaInN Metal–Insulator–Semiconductor High Electron Mobility Transistor on Si. *Appl. Phys. Express* **2011**, *4*, 104102. [CrossRef]
121. Nakazawa, S.; Shih, H.-A.; Tsurumi, N.; Anda, Y.; Hatsuda, T.; Ueda, T.; Kimoto, T.; Hashizume, T. Effects of Post-Deposition Annealing in O$_2$ on Threshold Voltage of Al$_2$O$_3$/GaN/MOS Heterojunction Field-Effect Transistors. *Jpn. J. Appl. Phys.* **2019**, *58*, 030902. [CrossRef]
122. Choi, M.; Lyons, J.L.; Janotti, A.; Van de Walle, C.G. Impact of Native Defects in High-k Dielectric Oxides on GaN/Oxide Metal–Oxide–Semiconductor Devices. *Phys. Status Solidi B* **2013**, *250*, 787–791. [CrossRef]
123. Weber, J.R.; Janotti, A.; Van de Walle, C.G. Native Defects in Al$_2$O$_3$ and their Impact on III-V/Al$_2$O$_3$ Metal-Oxide-Semiconductor-Based Devices. *J. Appl. Phys.* **2011**, *109*, 033715. [CrossRef]
124. Liu, D.; Clark, S.J.; Robertson, J. Oxygen Vacancy Levels and Electron Transport in Al$_2$O$_3$. *Appl. Phys. Lett.* **2010**, *96*, 032905. [CrossRef]
125. Shin, B.; Weber, J.R.; Long, R.D.; Hurley, P.K.; Van de Walle, C.G.; McIntyre, P.C. Origin and Passivation of Fixed Charge in Atomic Layer Deposited Aluminum Oxide Gate Insulators on Chemically Treated InGaAs Substrates. Appl. Phys. Lett. 2010, 96, 152908. [CrossRef]

126. Kim, J.B.; Kwon, D.R.; Chakrabarti, K.; Lee, C.; Oh, K.Y.; Lee, J.H. Improvement in Al2O3 Dielectric Behavior by Using Ozone as an Oxidant for the Atomic Layer Deposition Technique. J. Appl. Phys. 2002, 92, 6739–6742. [CrossRef]

127. Huang, S.; Liu, X.; Wei, K.; Liu, G.; Wang, X.; Sun, B.; Yang, X.; Shen, B.; Liu, C.; Liu, S.; et al. O2-Sourced Atomic Layer Deposition of High Quality Al2O3 Gate Dielectric for Normally-off GaN Metal-Insulator-Semiconductor High-Electron-Mobility Transistors. Appl. Phys. Lett. 2015, 106, 033507. [CrossRef]

128. ˇTapajna, M.; Václav, L.; Gucmann, F.; Gregušová, D.; Fröhlich, K.; Hašček, Š.; Dobročka, E.; Tóth, L.; Pécz, B.; Kuzmík, J. Low-Temperature Atomic Layer Deposition-Grown Al2O3 Gate Dielectric for GaN/AlGaN/GaN MOS HEMTs: Impact of Deposition Conditions on Interface State Density. J. Vac. Sci. Technol. B Nanotechnol. Microelectron. Mater. Process. Meas. Phenom. 2017, 35, 01A107. [CrossRef]

129. Uenuma, M.; Takahashi, K.; Sonohara, S.; Tominaga, Y.; Fujimoto, Y.; Ishikawa, Y.; Uraoka, Y. Influence of Carbon Impurities and Oxygen Vacancies in Al2O3 Film on Al2O3/GaN MOS Capacitor Characteristics. AIP Adv. 2018, 8, 105103. [CrossRef]

130. Qin, X.; Wallace, R.M. In Situ Plasma Enhanced Atomic Layer Deposition Half Cycle Study of Al2O3 on AlGaN/GaN High Electron Mobility Transistors. Appl. Phys. Lett. 2015, 107, 081608. [CrossRef]

131. Yoshisugu, K.; Horita, M.; Ishikawa, Y.; Uraoka, Y. Characterizations of Al2O3 Dielectric Deposited on n-GaN by Plasma-Assisted Atomic Layer Deposition. Status Solidi C 2010, 7, 1426–1429. [CrossRef]

132. Ozaki, S.; Ohki, T.; Kanamura, M.; Imada, T.; Nakamura, N.; Okamoto, N.; Miyajima, T.; Kikkawa, T. Effect of Oxidant Source on Threshold Voltage Shift of AlGaN/GaN MIS-HEMTs Using ALD-Al2O3 Gate Insulator Films. In Proceedings of the CS MANTECH 2012 Conference, USA, 23-26 April 2012.

133. Liu, Z.H.; Ng, G.I.; Arulkumaran, S.; Maung, Y.K.T.; Zhou, H. Temperature-Dependent Forward Gate Current Transport in Atomic-Layer-Deposited Al2O3/AlGaN/GaN Metal-Insulator-Semiconductor High Electron Mobility Transistor. Appl. Phys. Lett. 2011, 98, 01A107. [CrossRef]

134. Wu, J.; Lu, X.; Ye, S.; Park, J.; Streit, D. Electrical Characterization and Reliability Analysis of Al2O3/AlGaN/GaN MOS MISH Structure. In Proceedings of the 2014 IEEE International Reliability Physics Symposium, Waikoloa, HI, USA, 1–5 June 2014; p. CD-6. [CrossRef]

135. Heuken, L.; Ottaviani, A.; Fahle, D.; Zweipfennig, T.; Lükens, G.; Kalisch, H.; Vescan, A.; Heuken, M.; Burghart, J.N. Limitations for Reliable Operation at Elevated Temperatures of Al2O3/AlGaN/GaN Metal–Insulator–Semiconductor High-Electron-Mobility Transistors Grown by Metal–Organic Chemical Vapor Deposition on Silicon Substrate. Phys. Status Solidi A 2020, 217, 1900697. [CrossRef]

136. Terman, L.M. An Investigation of Surface States at a Silicon/Silicon Oxide Interface Employing Metal-Oxide-Silicon Diodes. Solid-State Electron. 1962, 5, 285–299. [CrossRef]

137. Nicollian, E.H.; Goetzberger, A. The Si-Sio Interface–Electrical Properties as Determined by the Metal-Insulator-Silicon Conduction Technique. Bell Syst. Tech. J. 1967, 46, 1033–1055. [CrossRef]

138. Shih, H.-A.; Kudo, M.; Suzuki, T. Analysis of AlN/AlGaN/GaN Metal-Insulator-Semiconductor Structure by Using Capacitance-Frequency-Temperature Mapping. Appl. Phys. Lett. 2012, 101, 043501. [CrossRef]

139. Freedmans, J.J.; Kubo, T.; Egawa, T. Trap Characterization of In-Situ Metal-Organic Chemical Vapor Deposition Grown AlN/AlGaN/GaN Metal-Insulator-Semiconductor Heterostructures by Frequency Dependent Conductance Technique. Appl. Phys. Lett. 2011, 99, 033504. [CrossRef]

140. Stoklas, R.; Gregušová, D.; Nováček, J.; Vescan, A.; Kordos, P. Investigation of Trapping Effects in AlGaN/GaN/Si Field-Effect Transistors by Frequency Dependent Capacitance and Conductance Analysis. Appl. Phys. Lett. 2008, 93, 124103. [CrossRef]

141. Yang, S.; Tang, Z.; Wong, K.-Y.; Lin, Y.-S.; Lu, Y.; Huang, S.; Chen, K.J. Mapping of Interface Traps in High-Performance Al2O3/AlGaN/GaN MIS-Heterostructures Using Frequency- and Temperature-Dependent C-V Techniques. In Proceedings of the 2013 IEEE International Electron Devices Meeting, Washington, DC, USA, 9–11 December 2013; pp. 6.3.1–6.3.4. [CrossRef]

142. Ramanan, N.; Lee, B.; Misra, V. Comparison of Methods for Accurate Characterization of Interface Traps in GaN MOS-HFET Devices. IEEE Trans. Electron Devices 2015, 62, 546–553. [CrossRef]

143. Winzer, A.; Szabó, N.; Wachowiak, A.; Jordan, P.M.; Heitmann, J.; Mikolajick, T. Impact of Postdeposition Annealing upon Film Properties of Atomic Layer-Deposition-Grown Al2O3 on GaN. J. Vac. Sci. Technol. B 2015, 33, 01A106. [CrossRef]

144. Kim, S.; Hori, Y.; Ma, W.-C.; Kikuta, D.; Narita, T.; Iuchi, H.; Uesugi, T.; Kachi, T.; Hashizume, T. Interface Properties of Al2O3/n-GaN Structures with Inductively Coupled Plasma Etching of GaN Surfaces. Jpn. J. Appl. Phys. 2012, 51, 060201. [CrossRef]

145. Hori, Y.; Mizue, C.; Hashizume, T. Interface State Characterization of ALD-Al2O3/GaN and ALD-Al2O3/AlGaN/GaN Structures. Phys. Status Solidi C 2012, 9, 1356–1360. [CrossRef]

146. Ooyama, K.; Kato, H.; Miczek, M.; Hashizume, T. Temperature-Dependent Interface-State Response in an Al2O3/n-GaN Structure. Jpn. J. Appl. Phys. 2008, 47, 5426. [CrossRef]

147. Ando, Y.; Kaneki, S.; Hashizume, T. Improved Operation Stability of Al2O3/AlGaN/GaN MOS High-Electron-Mobility Transistors Grown on GaN Substrates. Appl. Phys. Express 2019, 12, 024002. [CrossRef]
172. Guo, A.; del Alamo, J.A. Negative-Bias Temperature Instability of GaN MOSFETs. In Proceedings of the 2016 IEEE International Reliability Physics Symposium (IRPS), Pasadena, CA, USA, 17–21 April 2016; pp. 4A-1–4A-1-6. [CrossRef]

173. Van Hove, M.; Kang, X.; Stoffels, S.; Wellekens, D.; Ronchi, N.; Venegas, R.; Geens, K.; Decoutere, S. Fabrication and Performance of Au-Free AlGaN/GaN-on-Silicon Power Devices With Al2O3 and Si3N4/Al2O3 Gate Dielectrics. IEEE Trans. Electron Devices 2013, 60, 3071–3078. [CrossRef]

174. Capriotti, M.; Alexewicz, A.; Fleury, C.; Gavagnin, M.; Bethge, O.; Visalli, D.; Derluyn, J.; Wanzenböck, H.D.; Bertagnolli, E.; Pogany, D.; et al. Fixed Interface Charges between AlGaN Barrier and Gate Stack Composed of in Situ Grown SiN and Al2O3 in AlGaN/AlGaN High Electron Mobility Transistors with Normally off Capability. Appl. Phys. Lett. 2014, 104, 113502. [CrossRef]

175. Liu, X.; Liu, Z.; Pannirselvam, S.; Pan, J.; Liu, W.; Jia, F.; Lu, Y.; Liu, C.; Yu, W.; He, J.; et al. Band Alignment of HfAlO/GaN (0001) Determined by X-Ray Photoelectron Spectroscopy: Effect of in Situ SiH4 Passivation. J. Alloys Compd. 2015, 636, 191–195. [CrossRef]

176. Liu, X.; Chin, H.-C.; Tan, L.S.; Yeo, Y.-C. High-Permittivity Dielectric Stack on Gallium Nitride Formed by Silane Surface Passivation and Metal–Organic Chemical Vapor Deposition. IEEE Electron Device Lett. 2009, 31, 8–10. [CrossRef]

177. Hatano, M.; Taniguchi, Y.; Kodama, S.; Tokuda, H.; Kuzuhara, M. Reduced Gate Leakage and High Thermal Stability of AlGaN/GaN MIS-HETs Using ZrO2/Al2O3 Gate Dielectric Stack. Appl. Phys. Express 2014, 7, 044101. [CrossRef]

178. Partida-Manzanera, T.; Zaidi, Z.H.; Roberts, J.W.; Dolmanan, S.B.; Lee, K.B.; Houston, P.A.; Chalker, P.R.; Tripathy, S.; Potter, R.J. Control of Atomic Layer Deposited Al2O3 and Ta2O5.12Al2O3.G85 Gate Dielectrics on the Characteristics of GaN-Capped AlGaN/GaN Metal-Oxide-Semiconductor High Electron Mobility Transistors. J. Appl. Phys. 2019, 126, 034102. [CrossRef]

179. Mitrovic, I.Z.; Das, P.; Jones, L.; Gibbon, J.; Dhanak, V.R.; Mahapatra, R.; Manzanera, T.P.; Roberts, J.W.; Potter, R.J.; Chalker, P.R.; et al. Band Line-up of High-k Oxides on GaN. ECS Trans. 2020, 97, 67. [CrossRef]

180. Le, S.P.; Nguyen, T.Q.; Shih, H.-A.; Suzuki, T. Low-Frequency Noise in AlTiO/AlGaN/GaN Metal-Insulator-Semiconductor Heterojunction Field-Effect Transistors. J. Appl. Phys. 2016, 119, 204503. [CrossRef]

181. Le, S.P.; Nguyen, D.D.; Suzuki, T. Insulator-Semiconductor Interface Fixed Charges in AlGaN/GaN Metal-Insulator-Semiconductor-Deoevices with Al2O3 or AlTiO Gate Dielectrics. J. Appl. Phys. 2018, 123, 034504. [CrossRef]

182. Roberts, J.W.; Chalker, P.R.; Lee, K.B.; Houston, P.A.; Cho, S.J.; Thayne, I.G.; Guiney, I.; Wallis, D.; Humphreys, C.J. Control of Threshold Voltage in E-Mode and D-Mode GaN-on-Si Metal-Insulator-Semiconductor Heterostructure Field Effect Transistors by in-Situ Fluorine Doping of Atomic Layer Deposition Al2O3 Gate Dielectrics. Appl. Phys. Lett. 2016, 108, 072901. [CrossRef]

183. Zhang, Y.; Sun, M.; Joglekar, S.J.; Fujishima, T.; Palacios, T. Threshold Voltage Control by Gate Oxide Thickness in Fluorinated GaN Metal-Oxide-Semiconductor High-Electron-Mobility Transistors. Appl. Phys. Lett. 2013, 103, 033524. [CrossRef]

184. Cai, Y.; Zhou, Y.; Chen, K.J.; Lau, K.M. High-Performance Enhancement-Mode AlGaN/GaN HEMTs Using Fluoride-Based Plasma Treatment. IEEE Electron Device Lett. 2005, 26, 435–437. [CrossRef]

185. Chu, R.; Corrion, A.; Chen, M.; Li, R.; Wong, D.; Zehnder, D.; Hughes, B.; Boutros, K. 1200-V Normally off GaN-on-Si Field-Effect Transistors with Low Dynamic on-Resistance. IEEE Electron Device Lett. 2011, 32, 632–634. [CrossRef]

186. Yang, S.; Liu, S.; Liu, C.; Hua, M.; Chen, K.J. Gate Stack Engineering for GaN Lateral Power Transistors. Semicond. Sci. Technol. 2015, 31, 024001. [CrossRef]

187. Yang, S.; Wang, N.; Zhang, W.; Lin, Y.; Liu, C.; Lu, Y.; Huang, S.; Chen, K.J. High-Quality Interface in Al2O3/SiN/GaN/AlGaN/AlGaN MIS Structures With In Situ Pre-Gate Plasma Nitridation. IEEE Electron Device Lett. 2013, 34, 1497–1499. [CrossRef]

188. Chen, K.J.; Yang, S.; Tang, Z.; Huang, S.; Lu, Y.; Jiang, Q.; Liu, C.; Li, B. Surface Nitridation for Improved Dielectric III-Nitride Interfaces in GaN MIS-HEMTs. Phys. Status Solidi A 2015, 212, 1059–1065. [CrossRef]

189. Asahara, R.; Nozaki, M.; Yamada, T.; Ito, J.; Nakazawa, S.; Ishida, M.; Ueda, T.; Yoshigoe, A.; Hosoi, T.; Shimura, T.; et al. Effect of Nitrogen Incorporation into Al-Based Gate Insulators in AlON/AlGaN/GaN Metal–Oxide–Semiconductor Structures. Appl. Phys. Express 2016, 9, 101002. [CrossRef]

190. Wang, Q.; Cheng, X.; Zheng, L.; Shen, L.; Li, J.; Zhang, D.; Qian, R.; Yu, Y. Interface Engineering of an AlNO/AlGaN/GaN MIS Diode Induced by PEALD Alternate Insertion of AlN in Al2O3. RSC Adv. 2017, 7, 11745–11751. [CrossRef]

191. Ueda, T. GaN Power Devices: Current Status and Future Challenges. Jpn. J. Appl. Phys. 2019, 58, SC0804. [CrossRef]

192. Ogawa, E.; Hashizume, T.; Nakazawa, S.; Ueda, T.; Tanaka, T. Chemical and Potential Bending Characteristics of Si3N4/GaN Interfaces Prepared by in Situ Metal-Organic Chemical Vapor Deposition. Jpn. J. Appl. Phys. 2007, 46, L590. [CrossRef]

193. Takizawa, T.; Nakazawa, S.; Ueda, T. Crystalline SiN4 Ultrathin Films Grown on AlGaN/GaN Using in Situ Metalorganic Chemical Vapor Deposition. J. Electron. Mater. 2008, 37, 628–634. [CrossRef]

194. Derluyn, J.; Boeykens, S.; Cheng, K.; Vandersmissen, R.; Das, J.; Ruythooren, W.; Degroote, S.; Leys, M.R.; Germain, M.; Borghs, G. Improvement of AlGaN/GaN High Electron Mobility Transistor Structures by in Situ Deposition of a Si3N4 Surface Layer. J. Appl. Phys. 2005, 98, 054501. [CrossRef]

195. Moens, P.; Liu, C.; Banerjee, A.; Vanmeerebeek, P.; Coppins, P.; Zi, H.; Constant, A.; Li, Z.; De Vleeschouwer, H.; Roig-Guitart, J.; et al. An Industrial Process for 650V Rated GaN-on-Si Power Devices Using in-Situ SiN as a Gate Dielectric. In Proceedings of the 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC’s (ISPSD), Waikoloa, HI, USA, 15–19 June 2014; pp. 374–377. [CrossRef]
197. Hua, M.; Liu, C.; Yang, S.; Liu, S.; Fu, K.; Dong, Z.; Cai, Y.; Zhang, B.; Chen, K.J. Characterization of Leakage and Reliability of SiN$_x$ Gate Dielectric by Low-Pressure Chemical Vapor Deposition for GaN-Based MIS-HEMTs. *IEEE Trans. Electron Devices* 2015, 62, 3215–3222. [CrossRef]

198. Jauss, S.A.; Hallaceli, K.; Mansfeld, S.; Schwaiger, S.; Daves, W.; Ambacher, O. Reliability Analysis of LPCVD SiN Gate Dielectric for AlGaN/GaN MIS-HEMTs. *IEEE Trans. Electron Devices* 2017, 64, 2298–2305. [CrossRef]

199. Whiteside, M.; Arulkumaran, S.; Dikme, Y.; Sandupatla, A.; Ng, G.I. Demonstration of AlGaN/GaN MISHEMT on Si with Low-Temperature Epitaxy Grown AlN Dielectric Gate. *Electronics* 2020, 9, 1858. [CrossRef]

200. Hashizume, T.; Alekseev, E.; Pavlidis, D.; Boutros, K.S.; Redwing, J. Capacitance-Voltage Characterization of AlN/GaN Metal–Insulator–Semiconductor Structures Grown on Sapphire Substrate by Metalorganic Chemical Vapor Deposition. *J. Appl. Phys.* 2000, 88, 1983–1986. [CrossRef]

201. Uemoto, Y.; Shibata, D.; Yanagihara, M.; Ishida, H.; Matsuo, H.; Nagai, S.; Batta, N.; Li, M.; Ueda, T.; Tanaka, T.; et al. 8300V Blocking Voltage AlGaN/GaN Power HFET with Thick Poly-AlN Passivation. In Proceedings of the 2007 IEEE International Electron Devices Meeting, Washington, DC, USA, 10–12 December 2007; pp. 861–864. [CrossRef]

202. Hwang, I.-H.; Kang, M.-J.; Cha, H.-Y.; Seo, K.-S. Crystalline AlN Interfacial Layer on GaN Using Plasma-Enhanced Atomic Layer Deposition. *Crystals* 2021, 11, 405. [CrossRef]

203. Whiteside, M.; Ng, G.I.; Arulkumaran, S.; Ranjan, K.; Dikme, Y. Low Temperature Epitaxy Grown AlN Metal-Insulator-Semiconductor Diodes on AlGaN/GaN HEMT Structure. In Proceedings of the 2019 Electron Devices Technology and Manufacturing Conference (EDTM), Singapore, 12–15 March 2019; pp. 103–105. [CrossRef]

204. Whiteside, M.; Arulkumaran, S.; Dikme, Y.; Sandupatla, A.; Ng, G.I. Improved Interface State Density by Low Temperature Epitaxy Grown AlN for AlGaN/GaN Metal-Insulator-Semiconductor Diodes. *Mater. Sci. Eng. B* 2020, 262, 114707. [CrossRef]