Contamination-Assisted Rather Than Metal Catalyst-Free Bottom-Up Growth of Silicon Nanowires

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1. Introduction

Starting from the 60’s,[1] metal-catalyzed vapor–liquid–solid (VLS) growth was vastly explored and emerged as the key strategy for SiNW bottom-up synthesis. Nanoscale devices based on such bottom-up grown silicon nanowires (SiNWs) were extensively researched over the past two decades and remain of interest for a variety of applications ranging from CMOS electronics and nanoscale sensing to photonics and quantum computing.[2–5] However, there are still several issues that need to be addressed in order to realize the full potential of bottom-up material synthesis and, to compete with conventional top-down SiNW etching protocols. SiNW device fabrication employing a top-down approach enables planar SiNW devices in high quality, quantity, and density by using established microtechnologies.[6] Complex transistor arrangements for highly integrated circuits and also unique architectures, e.g., reconfigurable field-effect transistors, can be effectively manufactured in this manner.[7] Despite these benefits, adequate substrate materials, e.g., silicon-on-insulator substrates, and strategies to limit the impact of etching procedures, e.g., on the charge carrier mobility, are required.[6] A bottom-up SiNW growth strategy enables in contrary to synthesize SiNWs with nanoscale diameters and several micrometers in length without the need for sophisticated lithography tools operating in the deep-ultraviolet and even extreme-ultraviolet spectral range. Nanowires can be furthermore grown on and also transferred to various substrate materials. However, capable single-nanowire assembly strategies must be still developed to arrange billions of nanowires in a reproducible manner in future.[8] A key aspect of a VLS process for bottom-up growth is the nanoscale metal catalyst used, which must allow pure Si phase precipitation from the metal-silicon alloy in question. Various metals such as Au, Pt, Al, Fe, and many more were already successfully applied in this regard for SiNW synthesis.[9–12] The noble metal Au is still by far the preferred catalyst material here, as it enables SiNW growth at relatively low temperatures, such as 380 °C.[13] As well as SiNWs kinking, epitaxial growth, and certain morphology control.[14,15] Contrary to the widespread expectation that bottom-up synthesized SiNWs are pure, i.e., free of any metal impurities in this case, the catalyst material can actually be incorporated into the
Figure 1. a,b) SEM images of SiNWs synthesized at 520 and 680 °C, respectively. Prior to growth, both substrates were boiled in ultrapure water for one hour. c) Representative SiNW growth on a KOH-activated substrate. The substrate was pretreated in aqueous 30 wt% KOH for 120 s followed by the SiNW synthesis at 680 °C for one hour.

Growing nanowire in a very small amount and to the detriment of the material. Generally, metallic contamination in semiconductors and especially in silicon is a well-known cause of semiconductor device failure. Metal impurities readily induce so-called trap energy states within the band gap of the semiconductor, which not only degrade the electronic and optical properties of SiNWs, but are also known to be key aspects for the reproducibility of the electronic properties of SiNWs.\[9,16,17\] It is therefore critical to keep contamination under control to reduce its impact on the overall charge carrier transport, optical properties, and reproducibility of SiNWs. Therefore, metal-free bottom-up synthesis of SiNWs is intriguing and appears as an inevitable step to avoid the risk of metal contamination and thus create, for instance, CMOS compatibility.\[18\]

To date, there are surprisingly only few reports addressing metal-free SiNW bottom-up synthesis. Generally, three principle mechanisms were discussed so far for metal-free SiNW growth, namely, oxygen-assisted growth (OAG),\[19,20\] carbothermal growth,\[21,22\] and sulfur-assisted growth.\[23,24\] Among these methods, OAG is the most viable candidate for the synthesis of pure SiNWs in a gas-phase reactor system and at relatively low temperatures. Within OAG, SiNW growth is assumed to be triggered by SiO<sub>2</sub> clusters and reactive open bonds at the substrate surface.\[19\] Kim et al.\[25\] recently demonstrated gas-phase SiNW OAG at temperatures as low as 520 °C using hydrogen-terminated silicon substrates activated only in heated ultrapure water prior to growth. In their studies, they demonstrated dense SiNW assemblies, indications of epitaxial growth, and SiNW doping. Although this method is overall promising, there are still many persisting research challenges regarding fundamental aspects of this kind of SiNWs synthesis such as reproducibility and epitaxial yield that we will cover in the following discussion. Aside from a pure demonstration of the growth, there is hardly any knowledge that covers the SiNW nucleation process or the role of unintentional metal contaminations. To elucidate these aspects further is the aim of this paper.

Starting from the substrate water boiling experiments for SiNW synthesis,\[25\] SiNW growth was mainly realized at 680 °C using a SiH<sub>4</sub>-based gas-phase reaction and further substrate pretreatments. In contrast to water-only pretreatment, KOH surface etching yielded SiNWs with high reproducibility and high density. Even controlled localized SiNW growth on the substrate was possible and epitaxial growth seems feasible. We also systematically investigated the effects of key growth parameters such as the crystal orientation of the silicon substrate, pretreatment time, and KOH concentration to determine the overall growth characteristics. To extend the knowledge of the inherent growth mechanisms, the initial stages of SiNW formation were also investigated. However, contrary to the original expectation of metal catalyst-free growth, our studies suggest that SiNW growth is primarily triggered by, e.g., iron impurities, which may be present as contamination on the etched surface.

The electrical properties of these so-called contamination-assisted grown SiNWs were studied by means of transmission line measurements (TLM) and common nanowire transistor characterization,\[26–28\] and revealed a convincing performance in comparison to the common gold-catalyzed SiNWs. This aspect strongly supports further exploration of such SiNW synthesis strategies and SiNW implementation in devices.

2. Result and Discussion

2.1. SiNWs Synthesis and Structural Characterization

The starting point of our investigations are the promising experiments on metal-free bottom-up SiNW synthesis by simple pretreatment of a silicon substrate in boiling water.\[25\] As shown in Figure 1a, SiNWs can be reproducibly grown by such an approach also in our gas-phase reactor using a gaseous SiH<sub>4</sub> atmosphere and a temperature of 520 °C but at a working pressure of 100 mbar. Nevertheless, the total SiNW density was rather low and SiNWs grew inhomogeneously on the substrate. Figure 1b depicts an area with one of the highest SiNW densities achieved within our experiments. This was triggered in our studies by increasing the growth temperature to 680 °C, which was also used in the following to further study an intended metal catalyst-free growth. However, despite the temperature increase, the inhomogeneities in SiNW growth density at the substrate surface persisted. Based on the current view of the OAG mechanism, the surface oxide concentration or rather the silicon-oxide state should directly affect the SiNW growth. Therefore, instead of using substrate water boiling, an aqueous KOH solution (30 wt%, 120 s) was used as a surface pretreatment to remove the native oxide and simultaneously provide a more homogeneous OH surface termination. An OH surface termination should also produce a more homogeneous OH surface termination. An OH surface termination should also produce a more homogeneous OH surface termination.
approach, KOH pretreatment of the growth substrate resulted in a dramatic increase in SiNW density under the same growth conditions as before (here 680 °C) as shown in Figure 1c.

Moreover, SiNW growth could be localized and confined to desired positions on the growth substrate by selectively treating predefined areas on the growth substrate with KOH by means of microtechnological lithographic techniques (Figure S1, Supporting Information).

To further elucidate the acting growth mechanisms and the morphology of the synthesized SiNWs, SiNWs were examined by high-resolution transmission electron microscopy (HRTEM) and scanning transmission electron microscopy (STEM) including spatially resolved energy dispersive X-ray spectroscopy (EDX) for elemental analysis as for instance shown in Figure 2 for KOH-pretreatment and in Figure S2 (Supporting Information) for water boiling experiments. Figure 2a illustrates a HRTEM image of a representative SiNW, which has been synthesized on a KOH-etched surface. Thermal decomposition of gaseous SiH₄ at the SiNW surface during nanowire elongation at a process temperature of 680 °C, yields a pronounced overcoating of the SiNW and hence, a distinct SiNW tapering.

The length of the grown SiNWs ranged from 6 to 25 μm with a mean value of (13 ± 4) μm. The diameter changed from (449 ± 120) nm at the base to (10.7 ± 0.2) nm at the tip due to tapering (length and diameter histograms of SiNW are shown in Figure S3 in the Supporting Information). Selected area electron diffraction patterns (SAED) showed additionally a pattern that is characteristic for single-crystalline silicon as shown in Figure 2b. This fact is well aligned with the results from HRTEM images that show clearly a crystalline lattice structure with a lattice plane distance of about 0.32 nm as indicated in Figure 2c. The measured lattice plane distance fits well to an expected growth of SiNWs in the [111] direction. SiNWs are furthermore wrapped by an ≈ 2 nm thick amorphous native silicon-oxide shell. Hence, metal catalyst-free SiNWs appear comparable to conventional metal-catalyzed SiNWs in terms of the preferred crystallographic nanowire growth direction, the single crystallinity of the SiNWs and the fact that SiNWs are decorated at their tip with a metallic catalyst particle. Nonetheless, the nanowire morphology differs with respect to severe tapering of the metal catalyst-free SiNWs.

However, HRTEM inspection of the tip section of the metal catalyst-free grown SiNWs reveals an unexpected feature in this regard. As shown in Figure 2d, a crystalline nanoparticle with a lattice plane distance of about 0.19 nm is embedded at the tip of SiNWs despite the fact that no catalyst particle was intentionally introduced into the growth process. Based on the OAG mechanism, one may assume first that the nanoparticle is just silicon-oxide. However, the crystalline nature, as well as the lower brightness (material contrast) in comparison to the SiNW stem, do not support this assumption. Energy dispersive X-ray spectroscopy (EDX) was used to evaluate the elemental composition in the tip region comparatively to the SiNW stem. The elemental mappings here first of all clearly show the presence of silicon and oxygen. Silicon is obviously the key element for SiNWs, as expected, and oxygen is presented along the entire SiNW including the tip region in a homogeneous concentration, which should be due to the native silicon-oxide coverage of the SiNWs. Nevertheless, a significant concentration of iron was also detected in the SiNW tip region (Figure 2e–h; Figures S4 and S5, Supporting Information). Iron, which is a well-known catalyst for SiNWs, was not actively introduced into the process.
which puts metallic impurities in focus as the cause. SiNWs that
grew on substrates pretreated with boiling water only and that
were investigated in the same manner interestingly also exhibited
metallic nanoparticles at their tip region. In these cases
despite the use of the same synthesis quartz tube, not iron,
but Au and Ag nanoparticles, which are also established cata-
lyst materials for the bottom-up SiNW growth, were detected.
This rules our synthesis tube as a major source. Nevertheless,
these findings emphasize the need to discuss contamination
issues in the context of an intended metal catalyst-free SiNW
synthesis. Iron and other metal impurities are known and
mostly critical impurities in CMOS electronics. In general,
the utilized silicon wafers are produced according to the con-
tventional Czochralski (Cz) or float-zone crystal growth (here
Cz wafers are used), which guarantees in principle ultrahigh
purity single-crystalline silicon. Critical contamination is
therefore mainly due to metal contamination originating from
the chemicals, tools or equipment used. Such sources comprise
polishing and packaging of the wafers as well as conventional
postcleaning procedures. Wafer dipping in a hydrofluoric
acid solution, as it is the case for the water boiling experiments,
appears to increase the risk of noble metal contamination such
as Au, Ag, and Cu. This might explain observed Ag and Au
catalyzed SiNWs in case of the water boiled samples. Common
heavy metal contamination comprising the observed iron impu-
rity can be introduced also from chemicals (wet etchants and
water), but also from the CVD reactor system itself (quartz
tube, heating, gas delivery systems, and stainless steel compo-
nents) and from handling tools such as beakers and metal
tweezers. Accordingly, it should be noted that our chemical
consumables, and here specifically KOH, may contain heavy
metals in a range of ppm according to the KOH specification
sheet. Therefore, the question arises whether a contamination-
free or a metal catalyst-free SiNW synthesis is possible at all.

To elucidate this question further, the initial growth stages of
a SiNW growth after KOH pretreatment were examined again
by high-resolution (S)TEM. For these experiments, SiNWs
were synthesized directly on silicon TEM membranes. This
allowed direct TEM inspection after SiNW growth without
further preparation steps. The membranes were placed in the
growth chamber immediately after pretreatment in KOH solu-
tion (30 wt%). SiNWs were thereby grown at 680 °C for only
five minutes. The limited SiNW growth time here allowed SEM
and TEM evaluation of the first steps of the synthesis process,
as shown in Figure 3a.b. The observed highly tapered SiNW
seeds exhibited a hexagonal cross-section that was maintained
during further growth in length of the SiNWs (Figure 3c,d).
Some SiNWs also maintained their pristine facets during fur-
ther length growth, whereas other SiNWs exhibited a signifi-
cant roughening of the surface. This roughening of the surface
should be primarily attributable to thermal overcoating.
The origin of this distinct difference must be still clarified.

Although pristine facets of the initial seeds indicate already
clearly a single-crystalline nature of these seeds, high-resolution
TEM was employed for further inspection (Figure 3e) and con-
firmed this assumption. The lattice plane distance with about
0.32 nm is equal to the value measured previously for SiNWs
(cf. Figure 2c) and indicates again a [111] growth direction of the
prospective SiNW. The single-crystal nature of the seeds also supports future
efforts for epitaxial growth, which is beyond set goals in this
study. However, an epitaxial relationship may well be suspected
for some of our SiNWs observed on the basis of SEM investiga-
tions. TEM inspection of the seed tip region revealed notably
again a crystalline nanoparticle with a displayed lattice plane dis-
tance of 0.19 nm, which is identical with the previous observation
of an iron-based particle (cf. Figure 2d). Iron thus appears here
to be a trigger or an unintended catalyst material for the growth
of SiNWs, which is also correspondingly present at the earliest
stages of growth. A real metal catalyst-free synthesis can thus not
be confirmed. Nevertheless, the method is still intriguing as it
appears still CMOS compatible based on the utilized cleaning
procedures and chemicals. However, for further use of contam-
ination-assisted SiNW synthesis, SiNW growth must be technol-
ogically controllable, e.g., by KOH substrate pretreatment.

2.2. Contamination-Assisted SiNW Growth with KOH
Substrate Pretreatment

To study and enable control of the SiNW synthesis by a KOH
pretreatment, three critical parameters, namely, concentration
of the KOH solution and hence indirectly of the iron contami-
nation, crystal orientation of the used silicon growth substrate
as well as the overall etching time (10 and 120 s) were consid-
ered (Figure 4 and 5). As evidently shown in Figure 4a–c, SiNWs
cannot be grown without any pretreatment, which exemplifies
that regardless of the silicon wafer orientation neither the sil-
icon substrate wafers itself nor the SiNW-CVD tool creates suf-
ficient metal contamination to trigger a SiNW growth at 680 °C
in a SiH4 atmosphere. On the contrary, already 10 s of KOH
pretreatment suffice to trigger a SiNW growth. The SiNW den-
sity increased by increasing the etching time to 120 s, which
directly indicates KOH as the cause of SiNW growth. Further-
more, a distinct dependence on the silicon crystal orientation
was observed, which appears to correlate qualitatively in an
inverse manner with the respective KOH etching rates. Hence,
the highest SiNW density is achieved for a silicon (111)
surface (Figure S6, Supporting Information).

The origin of this effect is still unclear, but several aspects can
be discussed. The degree of adsorption of metal impurities on a
silicon surface can be correlated with three main conditions: sil-
icon surface roughness, surface energy, and purity of the etchant
solution. Among the different silicon crystal orientations, despite
the lower etch rate of a silicon crystal with (111) orientation,
etched substrates may possess naturally a higher surface rough-
ness that can potentially facilitate absorption of metal impurities
during the etching process. Accordingly, iron impurities in the
etching solution, e.g., in the form of cations, are to be con-
sidered as the main source of adsorbed metallic impurities.

To investigate adsorbed iron contamination on the etched
surface, the substrate was characterized by X-ray photoemission
spectroscopy (XPS) before and after etching. XPS revealed that
iron (Fe2p spectrum) is only detectable on an etched-surface,
which confirms the assumption that KOH is the main reason
for iron contamination and thus for SiNW growth by means of
iron catalyst according to VLS mechanism (Figure S7, Sup-
porting Information). Future experiments should also consider
Figure 3. a,b) Hexagonally shaped, crystalline seeds that occur on the substrate surface after 5 min of SiNW growth. c) Single crystalline growth of seeds under formation of a SiNW. Epitaxial growth can be assumed for individual SiNWs. d) SiNW surface roughing during growth due to thermal overcoating. The reason for the observed overcoating inhomogeneity is not clear so far. e) HRTEM image of a SiNW seed. The left image demonstrates that the seed is single-crystalline with lattice plane distance of 0.32 nm, which is equal to the SiNWs. The tip region exhibits a crystalline nanoparticle with a lattice plane distance of about 0.19 nm, which appears identical to the nanoparticle that is present in the SiNW. The insets show the calculated fast FFT images.

Figure 4. SEM images of grown SiNWs on silicon substrates with different crystal orientation: (100), (110), and (111). The growth substrates were etched in 30 wt% KOH solution at 70 °C. SiNW growth a–c) without pretreatment, d–f) etched for 10 s, and g–i) etched for 120 s.
highly sensitive analysis methods such as time-of-flight secondary ion mass spectroscopy and vapor phase decomposition total reflection X-ray fluorescence spectroscopy to further study adsorbed contaminations.

To further explain the relationship between the adsorbed metal contamination from a KOH pretreatment and the catalytic VLS growth of SiNWs, the etched substrate was rinsed with a standard RCA (Radio Corporation of America) standard clean 2 (SC-2) cleaning procedure after KOH treatment but before growth. RCA cleaning is well-known as a robust and established cleaning technique to remove organic and metal impurities from wafer surfaces in semiconductor industry. Accordingly, the SiNW density of the RCA (SC-2) purified samples was significantly reduced, but a sufficient concentration of iron still remained on the substrate surface to trigger SiNW growth (Figure S8, Supporting Information). Aside from the aforementioned parameters, the KOH concentration (1, 15, 30 wt%) was also varied and the SiNW growth was carried out on KOH etched (111)-oriented silicon substrates. Figure 5 shows that the density of the grown SiNWs correlates with the concentration of the KOH solution, which means that the SiNW density increases by increasing the KOH concentration. This again supports the assumption that iron is introduced into the process mainly by the KOH used, despite an expected maximum iron concentration in the starting solution in the range of 5 ppm.

2.3. Electrical Characterization

Silicon nanowires were frequently discussed to be employed as transducers in nanoscale electronic devices as mentioned before. The electrical properties are therefore a crucial aspect to be also evaluated. The evaluation of the electrical transport properties was done via TLM (Figure S9, Supporting Information) to be able to consider a potential impact of the contact resistance. The measurements, as shown in Figure 6, were done by using SiNWs grown as per our iron-based contamination-assisted growth and by using conventional Au-catalyzed VLS growth for comparison purposes. The results clearly show that without any dopant addition, an overall comparable resistivity is achieved for both types of synthesis protocols despite different synthesis temperatures and the occurrence of SiNW tapering. Furthermore, p- and n-type doping is possible as well for both protocols. However, the elevated temperature must be considered with respect to the incorporation of dopants into the growing SiNW and should be enhanced by the elevated growth temperature, here true for contamination-assisted growth. Therefore, dopant control for contamination-assisted SiNW growth seems to be more challenging so far, which explains the observed low sensitivity of the resistivity when the dopant gas flow is increased. Control of dopant incorporation into the silicon lattice, as well as simultaneous control of the degree of tapering, could potentially be possible through appropriate process adjustments, such as increasing the addition of hydrogen to dilute the dopant gases, as well as for more efficient sidewall passivation.

In addition to TLM studies, contamination-assisted SiNWs were directly implemented in a field-effect-transistor...
configuration. The drain current \( I_D \) versus drain-source voltage \( V_{DS} \) plots in dependence on the applied back-gate voltage \( V_{BG} \) using a range from \(-30 \) to \(30 \) V is shown in Figure 7a. The drain current evidently increases at a set drain-source voltage with the decreasing \( V_{BG} \), which represents a common p-type channel characteristics, which can be governed by surface and bulk states as well as the SiNW morphology. To support this, Figure 7b demonstrates the dependence of the drain current on the back-gate voltage for a constant drain-source voltage of 2 V. The transconductance of the SiNW was measured in the linear part of the \( I_D-V_{BG} \) curve and was determined as \(-3.7 \times 10^{-8} \) A V\(^{-1}\), which is higher than the value determined for our conventional gold-catalyzed SiNWs with about \(-1 \times 10^{-8} \) A V\(^{-1}\) (Figure S10, Supporting Information).

The origin of this effect has not yet been clarified and requires further appropriate investigations. The absolute drain current difference is mainly due to the difference diameter or cross-sectional area as the contribution of contact resistance is expected to be less than 10% of the absolute resistance based on the aforementioned TLM measurements. Nevertheless, the results show that SiNWs synthesized by contamination-assisted growth generally appear to be quite suitable for the numerous application scenarios discussed, albeit taking into account their significant taper.

3. Conclusion

In summary, we discussed the metal-catalyst-free growth of SiNWs and showed that metallic impurities can trigger an unintended metal-catalytic SiNW growth. The contamination-assisted growth mechanism is therefore introduced and it can certainly be used for the synthesis of single-crystalline SiNWs, assuming a significantly reduced risk of metal poisoning as required for CMOS technology. In particular, pretreatment of the substrate surface with a diluted KOH solution yielded unintentional iron impurities absorbed on the etched substrate, which served as a precursor to a metal catalytic VLS-based synthesis of SiNWs at 680 °C and using SiH\(_4\) gas. Compared to the conventional VLS mechanism, the existence of a catalyst nanoparticle, in this case of iron, on the nanowire tip was detected already at the early growth stages of the SiNW growth.

HRTEM images further show that the SiNWs grow, as expected for a VLS-based growth, as single-crystals and preferentially in a [111] direction. Also, we studied systematically the effect of various growth parameters (crystallographic substrate orientation, KOH etching time, and concentration) on the SiNW synthesis. In addition, electrical characterization of the SiNWs demonstrated a convincing electrical performance compared to conventional Au-catalyzed SiNWs. The results obtained in this study reveal, on the one hand, that real metal-catalyst-free growth is still debatable even by using high-purity chemicals, but on the other hand that contamination-assisted SiNW growth may still offer an intriguing alternative to minimize the risk of metal poisoning of SiNWs.

4. Experimental Section

**Sample Preparation:** Single-crystalline silicon wafers with (100), (110), and (111) orientations were used as a growth substrate (n-doped Cz-Si wafers, resistance of 1 to 10 Ω cm, purchased from Microchemicals GmbH, Germany). After the wafer was cut into smaller pieces, a standard cleaning procedure was applied to all samples that consists of three steps: (1) substrate rinse in N-ethyl-2-pyrrolidone (NEP) for 5 min with ultrasonic support, (2) sample immersion in acetone and isopropanol for 3 min each, (3) sample drying with nitrogen gas. For SiNW growth based on water boiling, samples were treated first for 7 s with an hydrofluoric acid (2%) prior to the sample boiling in ultrapure (deionized) water. For the contamination-assisted growth experiments using potassium hydroxide (KOH) etching, the native silicon oxide was first removed by applying hydrofluoric acid (2%) for 1 min. The samples were subsequently etched in (30 wt%) KOH solution (BioXtra, ≥85% KOH basis, SIGMA-ALDRICH) at 70 °C for 10 and 120 s. To localize the etched area within some experiments, a photoresist layer (SU-8 2015, MicroChem, Westborough, USA) was deposited as a polymeric protective layer and patterned by laser lithography (µPG 101, Heidelberg Instruments, Germany). For specific experiments, KOH etched substrates were combined with a RCA SC-2 cleaning procedure. Sample were immersed for the RCA SC-2 cleaning in standard cleaning solution \((6:1:1 \text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{HCL})\) for 15 min, while heated at 70 °C, to desorb metallic contaminations. For back gate measurements, drain and source metal contacts were positioned on the SiNW at 2 μm separation distance (gate length). Metal contacts were made from a thin film stack consisting of 10 nm Ti, 100 nm Au, and 700 nm Al as top layer, respectively. The back-gate contact was a 50 nm Al thin film that was deposited on the backside of the chip.

Figure 7. Characterization of SiNWs synthesized by contamination-assisted growth and assembled in a back-gate field-effect transistors configuration.

- a) Current–voltage \( I_D-V_{DS} \) characteristic in dependence on the applied back-gate potential \( V_{BG} \). \( V_{BG} \) was varied between 30 to \(-30 \) V in steps of 10 V.
- b) Drain current dependence in \( I_D \) on the back-gate potential and gate leakage current \( I_L \) in [nA] at \( V_{DS} = 2 \) V.
Synthesis of SiNWs: All synthesis experiments were carried out in the same in-house-built quartz tube gas phase reactor (based on a Carbolite EST12/60/450 furnace) using a purified quartz tube chamber. Before every growth process, the growth chamber was heated to 850 °C and rinsed with a flow of Ar for 30 min. To avoid cross-contamination, contamination-assisted growth experiments were realized using an own quartz tube and sample boat. SiNW growth on samples treated by water boiling was realized at 520 and 680 °C (working pressure 100 mbar) and for KOH-based contamination-assisted growth at 680 °C using a also constant working pressure of 100 mbar. Monosilane (SiH₄ 2% in He) at a flux of 30 sccm was used as a precursor and hydrogen (H₂) was admixed with a flow of 260 sccm. Doped SiNWs were achieved by admixture of 5 and 10 sccm diborane (B₂H₆ 100 ppm in helium) for p-type doping and 2 and 4 sccm monophosphine (PH₃ 200 ppm in helium) for n-type doping. Gold-catalyzed SiNWs were synthesized based on the VLS-method by using colloidal gold nanoparticles (100 nm diameter, with prior poly-L-lysine surface activation for 1 min) at 485 °C for 40 min. The working pressure was 100 mbar, while SiH₄ and H₂ were introduced with a flow of 70 and 10 sccm, respectively. Identical dopant flow rates were utilized to grow p- and n-doped SiNWs.

Characterization: The SiNW morphology was characterized by scanning electron microscopy (SEM, Leo Zeiss, 1550), aberration corrected HRTEM (FEI Titan 80–300, 80 kV operation voltage) was used to examine the crystal structure and the elemental composition of the SiNWs. Scanning TEM including local EDX mappings to determine the elemental composition of the SiNWs was carried out at 200 kV using a Temaflosher Talos 200x equipped with a high sensitivity 4-quadrant detector SuperX EDX system. A Keithley parameter analyzer (4200 SCS, Keithley Instruments Inc., Cleveland, OH) was used for the electrical characterisation.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest
The authors declare no conflict of interest.

Data Availability Statement
Research data are not shared.

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