SiC-Based Active Quasi-Z-Source Inverter with Improved PWM Control Strategy

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Abstract: In this paper, an improved PWM scheme is proposed for an active quasi-Z source inverter (AqZSI). Compared to the quasi-Z-source inverter (qZSI), the AqZSI with improved PWM strategy can operate in a wide range of input voltage with a higher efficiency. Furthermore, the AqZSI can operate with a higher modulation index, a lower inductor current stress, and a reduced shoot-through current. A procedure flowchart is presented for the optimal selection of the shoot-through duty cycle, the switching ratio of the additional switch, and the modulation index for AqZSI. Moreover, some comparative results between the AqZSI, qZSI and conventional two-stage inverter with a boost DC-DC converter are shown in detail. Finally, 1.2-kVA SiC-based three-phase inverter prototypes are built to verify the agreement between theory and measurement.

1. Introduction

The renewable energy sources such as photovoltaics (PVs), wind power, and fuel cell stacks are found to be attractive solutions in global efforts of making power generation environmentally friendly. Micro-grids and small scale distribution systems, comprised of distributed power, energy sources, energy conversion devices, energy storage devices, local loads, and protection devices play an essential role in distributed power generation. For interfacing renewable energy sources to distributed power grid, power inverters play an important role [1]. Voltage source inverters (VSIs) are the most established DC-AC power converter in any electric power system. However, VSIs can only handle a buck conversion where the DC bus input voltage is always higher than that of the output AC voltage. In order to improve the boost capability of the traditional VSI, the two-stage boost converter based VSI (BC-VSI) [2]-[3] is implemented by adding a boost DC-DC converter between the energy source and the conventional H-bridge inverter. In the BC-VSI, the short-circuiting of the DC-link bus in the inverter stage is prevented, and a dead-time must be inserted into the switching pulses of each phase leg switches owing to the limited switching transition times of the switches. Some compensating techniques are proposed in [4]-[5] to evaluate the dead-time effect and as a consequence the complexity of the VSI control system is increased.

Recently, to overcome the aforementioned limitations in two-stage BC-VSI power conversion systems, studies on single-stage power conversion have been conducted intensely. Z-source and quasi Z-source inverters (ZSI/qZSIs) presented in [6]-[9] belong to a family of first types of such single-stage power conversion systems. They can be used for power conversion from the low voltage sources to any desired AC voltage without the shoot-through (ST) problem theoretically. In practice, however, the voltage gain of ZSI/qZSIs is limited by the parasitic elements of the topology. Some comparisons between single-stage qZSIs and conventional two-stage inverters are given in [10]-[13]. In [10], a comparison between BC-VSI and ZSI for fuel-cell vehicles is presented.

![Fig. 1. Three-phase circuits. (a) qZSI, (b) AqZSI](image)

In this comparison, it is shown that in cases where power switches with high switching loss are used for high power applications, ZSI is very competitive with great reliability and higher efficiency when the boost ratio is lower than 2. In the same way, qZSI is compared with BC-VSI in the low voltage gain region of (1 – 2) and at a switching frequency of 10 kHz as addressed in [11]. qZSI is shown to have a lower THD and higher efficiency than that of the BC-VSI. According to comparison results in [11], the switching frequency of the active switch in boost stage is five times the switching frequency of the H-bridge inverter. Furthermore, a wide band-gap device based BC-VSI and qZSI are discussed in [12]-[13]. The three-phase three-level VSI and qZSI expressed in [12] are tested under identical conditions with a low voltage gain of 1.33 and a switching frequency of 50 kHz. The size of passive components and loss contribution are presented, and it is shown that the qZSI does not have obvious advantages in comparison to BC-VSI under these circumstances. In [13], a SiC-based 6-kW/100-kHz qZSI and BC-VSI prototypes are investigated and comparisons are
made on power losses, input current, and output quality. According to findings of this study, qZSI shows superior THD up to 40\(^\text{th}\) harmonic but BC-VSI has a better power density.

By considering the number of active switches in the Z-network, the impedance source inverters can be divided into two main types: passive in [14]-[17] and active in [18]-[23]. The passive qZSIs depicted in Fig. 1(a) show a good performance in low boost voltage applications. When high boost voltages are required, a large ST duty cycle needs to be applied to qZSI. Consequently, qZSI has a high conduction loss because it carries a high ST current that is equal to twice the input current [17]. In order to overcome the limitations of qZSI, a large number of high boost impedance source inverter topologies have been developed by adding active and passive components to the impedance source network. In these structures, the use of a large number of components in the Z-source network may not be appropriate for high power applications because of the increase in power losses and low efficiency.

A family of quasi-switched boost inverters (qSBIs) is proposed in [24] with reduced number of passive components. As introduced in [25], qSBI can be used to replace qZSI when the voltage gain of 2 to 3 is required. Some modified PWM methods for qSBI are introduced to enhance the performance of qSBI. For instance, a new family of \(n\)-pulse PWM scheme is proposed in [26] by combining ST mode and turning-on state of the active switch. The \(n\)-pulse PWM scheme can improve the modulation index, reduce the input current ripple, and decrease component stresses. However, this PWM technique is more complex, and it increases switching loss of the additional switch in the impedance source network. To achieve the same outcomes, another PWM scheme is proposed for qSBI in [27]. This PWM method shows some advantages; specifically, it can reduce the switching loss of the additional switch. But the ST time interval and turning-on time of the additional switch are interdependent and not selected optimally.

The qSBIs can operate with low ST duty cycles in the modified PWM methods [26][27]. However, qSBIs have a significant performance deterioration in buck mode of operation when the additional switch is turned off and the inverter operates without ST state. To avoid the unwanted operating states of qSBI at low ST duty cycle, one of the diodes in the switched-boost network needs to be replaced by an active switch as presented in [28]. This is not a good solution because two additional switches need to be used in the Z-network and the switches of each phase leg require a dead time.

In order to overcome limitations in qZSI and qSBI, an active qZSI (AqZSI) topology in Fig. 1(b) is proposed in [21]. By adding one more switch and a diode to the Z-source network, AqZSI topology with 3-pulse PWM method is shown to exhibit high voltage gain, low voltage stress on components, and low input current ripple than qZSI [21]. However, the overall performance of AqZSI and comprehensive comparison between AqZSI, qZSI, and BC-VSI are not presented in [21]. This paper presents and evaluates the performance of the single-stage three-phase AqZSI with improved PWM scheme for a wide range of input voltages. In the improved PWM technique, the ST duty cycle and the turning-on state of \(S_0\) are independently controlled with a simple PWM generation. By combining the variables of the modulation index, the ST duty cycle, and the duty cycle of the active switch, AqZSI can provide a wider input voltage operating range with higher efficiency. To study and verify the advantage of AqZSI with improved PWM scheme, a comprehensive comparison between the BC-VSI, qZSI, AqZSI with PWM scheme in [21] and AqZSI with improved PWM scheme is presented. 1.2-kVA SiC-based three-phase inverter prototypes are built to evaluate the analysis.

In the next section, the operational considerations of new PWM strategy for AqZSI are introduced. Section 3 discusses the control parameter selection for optimization. The power loss calculation is presented in Section 4. Section 5 compares AqZSI with improved PWM scheme and the BC-VSI, qZSI, and AqZSI with PWM scheme in [21]. Then, the experimental results are described in Section 6. Finally, the conclusions are given in Section 7.

2. Analysis of The Three-Phase AqZSI

2.1. Improved PWM Control Strategy

In this section, the improved PWM scheme is applied for the three-phase AqZSI. Fig. 2 shows the improved PWM method based on the maximum constant boost method with third harmonic injection for the three-phase AqZSI, where the control signal of the additional switch \(S_0\) and the ST signal are generated independently. In Fig. 2, \(D, D_0, T\) represent ST duty cycle, duty cycle of \(S_0\) switch, and switching period, respectively. Three-phase reference voltages \(v_a, v_b,\) and \(v_c\) are
compared with the triangle waveform \( v_{tri} \) to produce the control signal of H-bridge switches. The ST state with the interval time of \( DT \) is created by comparing the reference signal \( V_{ref} \) and the triangle waveform \( v_{tri} \). On the other hand, the switch \( S_0 \) can be turned on during the non-shoot-through (NST) states of the H-bridge circuit with the time interval of \( D_B\cdot T \). A constant voltage \( V_0 \) is compared with \( v_{tri} \) which has twice the frequency of \( v_{tri} \) to produce the PWM for the switch \( S_0 \). The operating states of AqZSI are ST state, NST state 1, and NST state 2 which are comprehensively explained below.

### 2.2. Operating Principles

#### ST state

[Fig. 3(a), during \( DT \):] Fig. 3(a) depicts the equivalent circuit of AqZSI in the ST state. Here, only the three-phase H-bridge switches are turned on simultaneously, while \( S_0 \) is switched off. The diode \( D_1 \) is reverse-biased, while the diode \( D_2 \) is forward-biased. In this mode, the inductors \( L_1 \) and \( L_2 \) store energy, while the capacitors \( C_1 \) and \( C_2 \) are discharged. The following formulas can be written:

\[
\begin{align*}
 v_{i1} &= V_i + V_{C2} \\
 v_{i2} &= V_{C1} \\
 V_{PS} &= 0
\end{align*}
\]  
\[
\begin{align*}
 i_{C1} &= -I_{L2} \\
 i_{C2} &= -I_{L1}.
\end{align*}
\]

#### NST state 1

[Fig. 3(b), during \((1 - D - D_B)\cdot T\):] In the NST state 1, \( S_0 \) is switched off, while the H-bridge circuit is not short-circuited. Two diodes, \( D_1 \) and \( D_2 \) are forward-biased. The inductors \( L_1 \) and \( L_2 \) store energy while the capacitors \( C_1 \) and \( C_2 \) are charged. We have:

\[
\begin{align*}
 v_{i1} &= V_i - V_{C3} \\
 v_{i2} &= -V_{C2} \\
 V_{PS} &= V_{C1} + V_{C2}
\end{align*}
\]  
\[
\begin{align*}
 i_{C1} &= I_{L1} - I_{PN} \\
 i_{C2} &= I_{L2} - I_{PN}.
\end{align*}
\]

#### NST state 2

[Fig. 3(c), during \(D_B\cdot T\):] \( S_0 \) is turned on, while the H-bridge circuit is not short-circuited. The diode \( D_1 \) is forward-biased while the diode \( D_2 \) is reverse-biased. The inductor \( L_1 \) and the capacitor \( C_2 \) are charged while the inductor \( L_2 \) and the capacitor \( C_1 \) are discharged. The following equations can be written:

\[
\begin{align*}
 v_{i1} &= V_i \\
 v_{i2} &= -V_{C2} \\
 V_{PS} &= V_{C1} + V_{C2}
\end{align*}
\]  
\[
\begin{align*}
 i_{C1} &= -I_{PN} \\
 i_{C2} &= I_{L2} - I_{PN}.
\end{align*}
\]

where \( I_{PN} \) is the average DC-link current in NST states.

### 2.3. Boost Factor and Voltage Gain

In the steady state, the average voltage across the inductors \( (L_1 \) and \( L_2 \)) and the average current through the capacitors \( (C_1 \) and \( C_2 \)) over one switching period are zero. Applying the volt-second balance principle to the inductors and the charge-second balance principle to the capacitors, from (1) to (3), we can obtain the following voltages for capacitors \( C_1 \) and \( C_2 \):

\[
\begin{align*}
 V_{C1} &= \frac{1 - D}{L_1} \cdot V_i \\
 V_{C2} &= \frac{D}{L_2} \cdot V_i
\end{align*}
\]

The peak DC-link voltage in the NST states is

\[
V_{PS} = V_{C1} + V_{C2} = \frac{1}{1 - D_B - 2D + D_B D} V_i.
\]

The boost factor of AqZSI is rewritten as

\[
B = \frac{V_{PS}}{V_i} = \frac{1}{1 - D_B - 2D + D_B D}.
\]

The peak AC output phase voltage is given by

\[
V_o = M \cdot \frac{V_{PS}}{2} = M \cdot \frac{B \cdot V_i}{2},
\]

where \( M \) is the modulation index and is limited to

\[
M \leq 2(1 - D) / \sqrt{3}.
\]

In one switching period, the average value of the capacitor current is zero. By using the equations (1)-(3), the average current through \( L_1 \) and \( L_2 \) can be calculated as follows.

\[
\begin{align*}
 I_{i1} &= \frac{1 - D}{L_1} \cdot V_{PS} \\
 I_{i2} &= \frac{1 - D}{L_2} \cdot V_{PS}
\end{align*}
\]

where \( I_{PS} \) is defined as the average DC-bus current and is equal to

\[
I_{PS} = \frac{\sqrt{3} M \cdot V_{PS}}{2R_i},
\]

where \( R_i \) is the simplified equivalent DC load of the inverter’s AC side circuit and is calculated based on the resistive load \( R \) as (11).

\[
R_i = \frac{8}{3M^2} \frac{1 - D}{R}.
\]

### 2.4. Analytical Study with Parasitic Components in NST State

The boost factor of AqZSI can be determined by the selection of \( D \) and \( D_B \) as shown in (6). In addition, \( M \) will be calculated at the maximum value of \( 2(1 - D) / \sqrt{3} \). To find the optimal values of \( D \) and \( D_B \), the constrained optimization theory explained in Section 3 will be used. In this optimal solution, the value of \( D_B \) must be limited and AqZSI is operated in NST to improve the performance. Hence, the analytical equivalent circuit with parasitic components in NST state is discussed in this subsection. The DC circuit analysis of AqZSI is conducted with the following assumptions: 1) the inverter is operated in continuous conduction mode; 2) the parasitic resistance of the inductors and the equivalent series resistance (ESR) of the capacitors are defined as \( r_L \) and \( r_C \), respectively; 3) the resistance of all switches is \( r_S \); 4) the resistance of all diodes is \( r_D \); 5) the switching frequency is greater than the frequency of the AC output voltage, and 6) the ST state is disabled \( (D = 0) \). The equivalent circuits of AqZSI without ST state are shown in Fig. 4.

#### Mode 1

[Fig. 4(a), during \((1 - D)\cdot T\):] The following equations can be obtained.

\[
\begin{align*}
 v_{i1} &= V_i - V_{C1} - r_C \cdot I_{i1} - I_{PS} - r_S \cdot I_{i2} - r_C \cdot I_{i3} \\
 v_{i2} &= -V_{C2} - r_L \cdot I_{i2} + r_C \cdot I_{i1} + I_{PS} + r_S \cdot I_{i3} - I_{PS} \\
 v_{i3} &= -r_L \cdot I_{i3} + V_{C1} + r_C \cdot I_{i1} - I_{PS} + r_S \cdot I_{i2} - I_{PS} + r_C \cdot I_{i1} - I_{PS} \\
 V_{PS} &= V_{C1} + V_{C2} + r_C \cdot I_{i1} - I_{PS} + r_L \cdot I_{i2} + I_{PS} + r_C \cdot I_{i3} - I_{PS}
\end{align*}
\]

where

\[
B = \frac{V_{PS}}{V_i} = \frac{1}{1 - D_B - 2D + D_B D}.
\]
The inductor current

\[
\begin{align*}
V_{r_1} &= V_c - r_c + V_{r_0} - r_0 \quad I_{L1} - r_L + I_{L2} - I_{PN} \\
V_{r_2} &= -V_c - r_c + I_{L1} - r_0 \quad I_{L1} - r_0 - I_{L2} - I_{PN} - r_L I_{L2} \\
V_{r_3} &= -r_L + V_{r_2} + V_{r_1} + r_c \quad I_{L2} - I_{PN} + r_0 \quad I_{L1} + I_{L2} - I_{PN} + r_L I_{PN} \\
I_{PS} &= \left(1 - D\right) V_{PS} - I_{PS} = 3V_c - I_o.
\end{align*}
\]

Substituting \( D = 0 \) into (9), the inductor current of \( L_1 \) and \( L_2 \) in this case can be written as

\[
\begin{align*}
I_{L1} &= \frac{1}{1 - D_0} I_{PS} \\
I_{L2} &= I_{PS}.
\end{align*}
\]

Supposing no losses in the H-bridge inverter, the output power is equal to the power transferred through DC-link in the NST states. The output power is defined as

\[
p_o = \left(1 - D\right) V_{PS} - I_{PS} = 3V_c - I_o.
\]

In steady state, the average inductor voltage across \( L_1 \) and \( L_2 \) over one switching period is zero. From (12) to (14), we have

\[
\begin{align*}
1 - D_0 \quad V_i - 1 - D_0 \quad V_c + D_0 - D_0 & - D_0 - D_0 - r_0 \quad 2 - D_0 \quad 2 - D_0 \quad I_{PS} = 0 \\
I_{PS} &= \frac{V_c}{4/3 R + r_L}.
\end{align*}
\]

Using (13)-(15), the capacitor voltage \( V_c \) and voltage boost factor \( B \) can be derived as follows

\[
\begin{align*}
V_c &= \frac{4/3 R + r_L}{4/3 R + 1 - D_0} V_i \\
B &= \frac{4/3 R - 1 - D_0}{4/3 R - 1 - D_0} V_i.
\end{align*}
\]

The boost factor \( B \) of AqZSI versus the duty cycle \( D_0 \) at \( D = 0 \) is shown in Fig. 5. Note that line (1) in Fig. 5 shows the ideal case with \( r_S = r_L = r_C = r_0 = 0 \), whereas lines (2) and (3) indicate the parasitic case with the resistive load \( R = 35 \Omega \) (full-load) and \( R = 70 \Omega \) (50% full-load), respectively. The value of parasitic resistance is defined as in the experimental verification as follow: \( r_S = 0.8 r_L = r_C = 1.5 r_0 = 78 \, m\Omega \). The boost factor with non-ideal components in lines (2) and (3) reaches its peak and then goes down as the duty cycle \( D_0 \) is increased to 1. From the plot structure of Fig. 5, it can be seen that the boost factor value of the full-load case is lower than that of the ideal and 50% full-load cases. In this case, we chose the maximum value of \( D_0 \) based on the full-load operating condition. We can see AqZSI has a near-ideal region with a good performance, has a shallow slope in \( B-D_0 \) characteristics and easy to control when \( D_0 \) is from 0 to 0.55. There are obvious differences between ideal and non-ideal line (2)-(3) when \( D_0 \) is higher than 0.6. Thus, the maximum value of \( D_0 \) is selected as 0.55.

3. Design Guideline Optimal Control Parameter Selection

The values of \( M, D \), and \( D_0 \) are directly related to the voltage gain. Alternatively, the value of \( D \) is associated with the duration of ST state in the H-bridge, voltage and current stresses of power components, and the system power losses of AqZSI. In order to improve the value of \( M \) and to reduce the power losses, \( D \) will be kept as small as possible. Fig. 6 shows the flowchart of the optimal control parameter calculation. As shown in Fig. 6, the input values of the process are the input voltage, \( V_i \) and the peak value of ac output voltage, \( V_o \). The calculation value of gain voltage, \( G_{ref} \) is defined as \( 2V_i/V_o \). The initial values of \( M, D \), and \( D_0 \) are set to 1.15, 0, and 0, respectively. In this flowchart, \( j \) is the step change which is a very small value. The selection process in the flowchart has two cases as follows

Case (i): \( G_{ref} < 1.15 \). As shown in the right branch of Fig. 6, the inverter operates in buck mode with the voltage gain lower than 1x1.15 similar to a conventional VSI. In this case, \( D \) and \( D_0 \) are set to zero. If \( M \) happens to be higher than \( G_{ref} \), \( M \) will be decreased by step values of \( j \) so that \( M \) is kept lower or equal to \( G_{ref} \). The loop is completed with \( D = D_0 = 0 \) and \( G_{real} = M \). Case (ii): \( G_{ref} \geq 1.15 \). The inverter is set to operate in boost mode, and \( D_0 \) is increased with step values of \( j \). In this mode \( D_0 \) is limited to its maximum value \( D_{0,\text{max}} \). If \( D_0 \leq D_{0,\text{max}} \), \( G_{real} \) is just dependent on \( M \) and \( D_0 \), and equal to \( M(1 - D_0) \). Otherwise, \( D_0 \) is kept to \( D_{0,\text{max}} \), and the value of \( D \) will be increased by step values of \( j \). In this case, the inverter is operating with the ST state, and the real voltage gain \( G_{real} \) is \( M \left(1 - D_{0,\text{max}} - 2D + DD_{0,\text{max}}\right) \). It is noted that because of the small value of step change \( j \) chosen, \( G_{ref} \) is approximated to \( G_{real} \).

In summary, the voltage gain of AqZSI can be rewritten as

\[
G = \begin{cases} 
M & 0 \leq D_0 \leq D_{0,\text{max}} \\
\frac{M}{1 - D_{0,\text{max}} - 2D + DD_{0,\text{max}}} & D > 0, \text{ with ST state.}
\end{cases}
\]
the conduction loss of switch \( S_0 \) and H-bridge switches, and is determined as
\[
P_{\text{con}} = P_{\text{con,3n}} + P_{\text{con,H}}
\]
\[
= R_{D_{\text{Son}}} I_{L1}^2 D_0 + 6 \cdot R_{D_{\text{Son}}} \left( \frac{I_{L1} + I_{L2}}{3} \right)^2 \cdot D
+ \frac{3}{\pi} \int_{0}^{\pi} \left[ (I_{L1} + I_{L2})^2 \cdot 0.5 \right] \left( 1 - \sqrt{3} M \right) \cdot d\omega
\]

where \( R_{D_{\text{Son}}} \), \( u_{D0} \), and \( R_{D\text{b}} \) are the on state drain-source resistance, the ON-state zero-current voltage and the ON-state resistance of the body diodes, of SiC MOSFETs respectively.

The switching loss encompasses the switching loss in switch \( S_0 \) and H-bridge switches, and is defined as
\[
P_{\text{sw}} = P_{\text{sw,3n}} + P_{\text{sw,H}}
\]
\[
= V_{C1} \cdot I_{L1} \cdot 2 f_s \cdot \left( \frac{I_{in} + I_{off}}{2} \right) + \frac{3}{\pi} \int_{0}^{\pi} \left[ I_{L1}^2 \cdot \left( 1 - \sqrt{3} M \right) \right] \cdot d\omega
+ 6 \cdot V_{Pn} \left( \frac{I_{L1} + I_{L2}}{3} \right) \cdot f_s \cdot \left( \frac{I_{in} + I_{off}}{2} \right) + 3 \cdot Q_{on} \cdot V_{Pn} \cdot f_s,
\]

where \( f_s \), \( I_{in} \), \( I_{off} \), and \( Q_{on} \) are the switching frequency of H-bridge, the turn-on and turn-off delay times of SiC MOSFET switch, and the reverse recovery charge of the body diode, respectively.

### 4.2. Power loss in diodes

The power loss in the diodes comprises of the conduction loss and reverse recovery loss, and is calculated as
\[
P_d = P_{cd} + P_{rd}
\]
\[
= \left[ u_{di} \cdot (I_{L1} + I_{L2}) + R_{di} \cdot (I_{L1} + I_{L2}) \right] \left( 1 - \frac{\sqrt{3}}{2} M - D \right)
+ \frac{1}{\pi} \left[ \left( u_{di} \cdot (I_{L1} + I_{L2} - I_c) + R_{di} \cdot (I_{L1} + I_{L2} - I_c) \right) \right] \left( \frac{\sqrt{3}}{2} M \cdot d\omega \right)
+ \left( u_{di} \cdot I_{L1} + u_{di} \cdot I_{L2} \right) \left( 1 - D_{0} \right) + Q_{on} \cdot V_{Pn} \cdot f_{ls} + Q_{on} \cdot V_{C1} \cdot 2 f_s,
\]

where \( u_{di}, u_{do}, R_{di}, R_{do}, Q_{on} \) and \( Q_{on} \) are the ON-state zero-current voltage and the ON-state resistance, reverse recovery charge of the diodes \( D_1 \) and \( D_2 \), respectively.

### 4.3. Power loss in capacitors

The power loss in \( C_1 \) and \( C_2 \) capacitors is expressed as
\[
P_c = r_{c1} \cdot I_{c1,\text{rms}}^2 + r_{c2} \cdot I_{c2,\text{rms}}^2
\]

where \( r_{c1} \) and \( r_{c2} \) are the equivalent series resistance (ESR) of capacitors \( C_1 \) and \( C_2 \), respectively. \( I_{c1,\text{rms}} \) and \( I_{c2,\text{rms}} \) are the RMS capacitor currents and are calculated as
\[
I_{c1,\text{rms}} = \left\{ \begin{align*}
& I_{L1}^2 D + \frac{1}{\pi} \int_{0}^{\pi} I_{L1}^2 \cdot D \cdot d\omega + \frac{1}{\pi} \int_{0}^{\pi} \left( I_{L1} - I_c \right)^2 \left( \frac{\sqrt{3}}{2} M - D \right) \cdot d\omega
\end{align*} \right\}
\]
\[
I_{c2,\text{rms}} = \left\{ \begin{align*}
& I_{L2}^2 D + \frac{1}{\pi} \int_{0}^{\pi} I_{L2}^2 \cdot D \cdot d\omega + \frac{1}{\pi} \int_{0}^{\pi} \left( I_{L2} - I_c \right)^2 \left( \frac{\sqrt{3}}{2} M - D \right) \cdot d\omega
\end{align*} \right\}
\]

Based on the analysis in Section 2.4 with parasitic components of the AqZSI, the maximum value of \( D_0 \) is selected as 0.55. From (18), the voltage gain curve consists of two parts. The relationships between \( G \) and \( M \), duty cycles \( D_0 \) and \( D \) are shown in Fig. 7 where \( D_{0,\text{max}} = 0.55 \). Fig. 7(a) shows the variation of voltage gain versus \( M \) in buck mode. Fig. 7(b) shows the voltage gain versus \( M \) when \( D = 0 \). The value of \( D_0 \) is changed from 0 to \( D_{0,\text{max}} \) when the voltage gain is increased from 1.15 to 2.56. Fig. 7(c) shows the voltage gain versus \( D \) when \( D_0 = 0.55 \). In Fig. 7(c), the voltage gain is varied in the range of [2.56, +∞) when \( D \) is increased from 0 to 0.31.

### 4. Power loss calculation of AqZSI

#### 4.1. Power loss in switches

Power loss in switches are predominantly conduction loss and switching loss. The conduction loss of the AqZSI is
4.4. Power loss in inductors

The power loss in the inductors comprises of the core loss and the copper loss.

\[
P_L = P_{core} + 2P_{cu} = r_L \cdot I_{1_{rms}}^2 + r_L \cdot I_{2_{rms}}^2 + 2 \cdot 0.33 \cdot B^{1.98} \cdot f^{1.64} \cdot A_{i} \cdot L_{i},
\]

where \( I_{1_{rms}} \) and \( I_{2_{rms}} \) are the RMS inductor current through inductors \( L_1 \) and \( L_2 \), respectively.

The detailed power loss comparison is presented in the next section.

5. Comparison Criteria for AqZSI, qZSI, and BC-VSI

A comprehensive comparison between AqZSI and the other high voltage gain impedance source inverters was presented in [21]. In this section, a comparison between the proposed PWM scheme and the conventional PWM scheme in [21] for AqZSI, qZSI and BC-VSI is presented. Table 1 shows the key equations of AqZSI with improved PWM scheme, AqZSI with PWM scheme in [21], and qZSI.

5.1. Input Current Ripple and Boost Factor

The input current ripple of the BC-VSI is given as

\[
\Delta I_i = \frac{D_1 \cdot V_i}{L_i \cdot 2f_i}
\]

where \( f_i \) is the switching frequency.

In the qZSI, the stored energy of \( L_1 \) and \( L_2 \) inductors in the ST state is largest. Thus, the peak to peak current ripples of the inductors \( L_1 \) and \( L_2 \) are determined as

\[
\Delta I_i = \Delta I_{1i} = \frac{D \cdot 1 - D}{1 - 2D} \frac{V_i}{L_i \cdot 2f_i}
\]

where \( f_i \) is the switching frequency.

Table 1. Comparison between AqZSI with proposed PWM scheme, AqZSI with PWM scheme in [21] and qZSI

| Parameter | AqZSI | AqZSI with PWM in [21] | qZSI |
|-----------|-------|------------------------|------|
| Boost Factor | \( \frac{1}{1-2D} \) | \( \frac{1}{1-D} \) | \( \frac{1}{1-D} \) |
| \( V_{in/V_i} \) | DB | \( (1-D)B \) | B |
| \( V_{in/V_i} \) | DB | \( (1-D)B \) | B |
| \( V_{in/V_i} \) | DB | \( (1-D)B \) | B |
| \( I_{1s}/I_{2s} \) | \( (1-D)B \) | \( (1-D)B \) | \( (1-D)B \) |
| \( I_{1s}/I_{2s} \) | \( (1-D)B \) | \( (1-D)B \) | \( (1-D)B \) |
| \( I_{1s}/I_{2s} \) | \( (1-D)B \) | \( (1-D)B \) | \( (1-D)B \) |

Input current ripple \( \frac{D}{L_b} - \frac{D}{L_b} \)

4.5. Parameters Used for Loss Calculation

| Parameters | Values |
|------------|--------|
| \( L_{i1}(r_{11}) \) and \( L_{i2}(r_{22}) \) | 0.12 \( \Omega \) |
| Core for inductors | CM777125 (142 nH/n²) |
| ESR of \( C_1 \) (r_{11}) | 250 \( \mu \)Ω for BC-VSI |
| ESR of \( C_2 \) (r_{22}) | 220 \( \mu \)Ω for qZSI and AqZSI |
| ESR of \( C_3 \) (r_{22}) | 120 \( \mu \)Ω for qZSI |
| SiC MOSFETs SFT3060AL | 650V, 39A, \( R_{DS} = 78 \Omega \) |
| SiC diodes IDH166G65C6 | 650V, 16A, \( V_T = 1.35 \) V |

Fig. 8. The key waveforms of AqZSI when \( D_{\text{max}} = 0.55 \). (a) \( D < 0.215 \) and (b) \( D > 0.215 \).
By solving (27), the peak-to-peak value of the current ripple for \( L_1 \) is calculated as

\[
\Delta I_{L_1} = \begin{cases} 
\frac{D_k V_i}{L_1 (2 f_s)} - \frac{D_k \leq 0.55, \text{ without ST state}}{L_1 (2 f_s)}, & D_k \leq 0.55, \text{ without ST state} \\
0.55 V_i \left( \frac{D_k - \frac{1}{2}}{1 - D_k} \right) - \frac{D_k \leq 0.215, \text{ with ST state}}{L_1 (2 f_s)}, & D_k \leq 0.215, \text{ with ST state} \\
D_k V_i + \frac{V_c}{L_1 (2 f_s)} - \frac{D_k \geq 0.215, \text{ with ST state}}{L_1 (2 f_s)}, & D_k \geq 0.215, \text{ with ST state}. 
\end{cases}
\]  

(28)

Thus, the current ripple of \( L_1 \) is determined as follows

\[
r_{L_1} = \begin{cases} 
\frac{D_k \leq 0.55, \text{ without ST state}}{1 - D_k \frac{1}{2 f_s}}, & D_k \leq 0.55, \text{ without ST state} \\
0.55 \frac{0.45 - 1.45D - R_f}{1 - D_k \frac{1}{2 f_s}} - \frac{D_k \leq 0.215, \text{ with ST state}}{L_1 (2 f_s)}, & D_k \leq 0.215, \text{ with ST state} \\
0.45D \frac{0.45 - 1.45D - R_f}{1 - D_k \frac{1}{2 f_s}} - \frac{D_k \geq 0.215, \text{ with ST state}}{L_1 (2 f_s)}, & D_k \geq 0.215, \text{ with ST state}. 
\end{cases}
\]  

(29)

The slope of inductor \( L_2 \) current is the same and equal to \(-Vc/I2\) for both ST state and NST states as presented in Fig. 3. The peak-to-peak inductor \( L_2 \) current ripple is determined as

\[
\Delta I_{L_2} = \frac{V_{c1} D T}{L_2 2 f_s}. 
\]  

(30)

Substituting the expression of \( Vc1 \) and \( Vc2 \) into (30), the peak-to-peak inductor \( L_2 \) current ripple can be rewritten as

\[
\Delta I_{L_2} = \frac{D 1 - D \frac{1}{2 f_s}}{0.45 - 1.45D \frac{1}{2 f_s}}. 
\]  

(31)

The inductor \( L_2 \) current ripple can be derived as follows

\[
r_{L_2} = \frac{D \frac{0.45 - 1.45D \frac{1}{2 f_s}}{0.45 - 1.45D \frac{1}{2 f_s}} - \frac{D \leq 0.55, \text{ without ST state}}{0.45 - 1.45D \frac{1}{2 f_s}}}{0.45 - 1.45D \frac{1}{2 f_s}}. 
\]  

(32)

The critical inductions of \( L_1 \) and \( L_2 \) are verified under the following conditions

\[
I_{L_1} = \frac{\Delta I_{L_1}}{2}, \quad I_{L_2} = \frac{\Delta I_{L_2}}{2}. 
\]  

(33)

Substituting (9), (10), and (28) into (33), the critical inductions of \( L_1 \) and \( L_2 \) are determined as

\[
L_{1, \text{cmin}} = \frac{\frac{D_k 1 - D_k (2 f_s)}{4 f_s} - \frac{D_k \leq 0.55, \text{ without ST state}}{4 f_s}}, \quad D_k \leq 0.55, \text{ without ST state} \\
0.55 \frac{0.45 - 1.45D \frac{1}{2 f_s}}{4 f_s} - \frac{D_k \leq 0.215, \text{ with ST state}}{4 f_s}, \quad D_k \leq 0.215, \text{ with ST state} \\
0.45D \frac{0.45 - 1.45D \frac{1}{2 f_s}}{4 f_s} - \frac{D_k \geq 0.215, \text{ with ST state}}{4 f_s}, \quad D_k \geq 0.215, \text{ with ST state}. 
\]  

(34)

\[
L_{2, \text{cmin}} = \frac{\frac{D (0.45 - 1.45D) \frac{1}{2 f_s}}{0.9 (1 - D) - 2 f_s}}{D_k \leq 0.55, \text{ without ST state}}, \quad D_k \leq 0.55, \text{ without ST state} \\
0.55 \frac{0.45 - 1.45D \frac{1}{2 f_s}}{1 - D}, \quad D_k \leq 0.215, \text{ with ST state} \\
0.45D \frac{0.45 - 1.45D \frac{1}{2 f_s}}{1 - D}, \quad D_k \geq 0.215, \text{ with ST state}. 
\]  

(35)

Fig. 9(a) shows the relationship between the input current ripple versus the voltage gain and the boost factor versus shoot-through duty cycle of the inverters when \( D_{0, \text{max}} = 0.55 \). The inductor current ripple of AqZSI with improved PWM scheme is equal to that of BC-VSI when \( G \leq 2.56 \). The inductor current ripple of AqZSI with improved PWM scheme is lower than that of BC-VSI when \( G \) is varied in \([5.99, 7.47]\). As shown in the right side of Fig. 9(a), the boost factor of AqZSI with improved PWM scheme is highest.

We have the boundary condition of the capacitor \( C_1 \) voltage ripple as

\[
\Delta V_{C1, \text{_HPP}} = \Delta V_{C1, \text{.innerHeight}}. 
\]  

(36)

Thus, the selected capacitance of \( C_1 \) is calculated as

\[
C_1 = \begin{cases} 
\frac{D_k \leq 0.55, \text{ without ST state}}{0.45 - 1.45D \frac{1}{2 f_s}}, & D_k \leq 0.55, \text{ without ST state} \\
D_k \leq 0.215, \text{ with ST state} \\
\frac{0.45D \frac{1}{2 f_s}}{1 - D}, & D_k \geq 0.215, \text{ with ST state}. 
\end{cases}
\]  

(37)

The capacitance of \( C_2 \) can be written as

\[
C_2 = \frac{1 - D^2}{0.45 - 1.45D \frac{1}{2 f_s}}. 
\]  

(38)
5.2. Voltage and Current Stress

The voltage stress $V_s$ on the H-bridge inverter of BC-VSI is calculated as

$$\frac{V_s}{V_i} = \frac{G}{M_{GSI}}$$  \hspace{1cm} (39)

The voltage stress on the H-bridge inverter of qZSI is calculated

$$\frac{V_s}{V_i} = \frac{\sqrt{3}G}{2} - 1$$  \hspace{1cm} (40)

The voltage stress on the H-bridge inverter of AqZSI is determined as

$$\frac{V_s}{V_i} = \begin{cases} \frac{G}{M} & G \leq \frac{M}{1 - D_{0_{\text{max}}}} \\ \frac{2 - D_{0_{\text{max}}}}{2} \sqrt{3}G - 1 & G > \frac{M}{1 - D_{0_{\text{max}}}} \end{cases}$$  \hspace{1cm} (41)

The ST current and the input current of qZSI and AqZSI are calculated as

$$I_{\text{st,qZSI}} = 2I_{\text{in}}$$  and  $$I_{\text{st,AqZSI}} = 2 - D_{0} I_{\text{in}}$$  \hspace{1cm} (42)

As shown in (42), the ST current of the AqZSI with improved PWM scheme is lower than the qZSI when $D_0 > 0$.

Based on (39)-(41) and Table 1, the voltage and current stress comparison between the BC-VSI, qZSI, AqZSI with improved PWM scheme is shown in Fig. 9(b)-(c). The voltage stress of H-bridge inverter switches in BC-VSI and AqZSI with improved PWM is identical when the voltage gain is lower than $M/(1 - D_{0_{\text{max}}})$. In contrast, the voltage stress of AqZSI with improved PWM is higher than that of the BC-VSI when the voltage gain is over $M/(1 - D_{0_{\text{max}}})$.

AqZSI with improved PWM scheme has a lower voltage stress on H-bridge inverter switches when compared to the qZSI and AqZSI [21]. However, voltage stresses of capacitor $C_1$ and switch $S_0$ of aforementioned inverters are identical but the capacitor $C_2$ voltage of AqZSI with improved PWM scheme is lower than that of the qZSI and AqZSI [21]. Because inductor $L_1$ is directly connected to the DC source, the inductor $L_1$ current stress of the aforementioned inverters is the same. The current stress of inductor $L_2$ and ST current stress of AqZSI with improved PWM scheme are lowest because the ST duty cycle of AqZSI with improved PWM scheme is minimized under optimal control conditions.

5.3. Power Loss

In this section, the power loss of the AqZSI with improved PWM scheme will be compared to BC-VSI, qZSI and AqZSI [21]. The power loss calculation is based on that presented in Section 4. Table 2 shows the circuit parameters of the inverters used in the power loss calculation. The SiC semiconductor devices were used to match the experiment. Fig. 10 shows the loss distribution in the inverters at 1037 W output power and the voltage gains of 1.05, 1.5 and 3.19. At a low voltage gain of 1.05 in buck mode, AqZSI with improved PWM method is the same as that in [21]. The diode loss of AqZSI is dominant owing to the full conduction of the additional $D_2$ diode. This leads to high conduction loss in AqZSI. At a voltage gain of 1.5 in boost mode, the switch loss of qZSI is highest because the ST state is used in qZSI. In the same way, the power loss of AqZSI [21] is higher than that of AqZSI with improved PWM scheme. This is because the ST state is not applied to AqZSI with improved PWM scheme, while it is used in the PWM scheme in [21]. At the high voltage gain of 3.19, the loss contribution of AqZSI is lower than that of qZSI, AqZSI [21]. This is because the minimal use of ST duty cycle by AqZSI compared to large ST duty cycle used in qZSI, AqZSI [21]. In all three aforementioned cases considered, the loss in BC-VSI is lower than that of qZSI, AqZSI [21], AqZSI with improved PWM scheme.

5.4. Dead-Time Effect and Output Quality

The BC-VSI is able to operate at the maximum modulation index of 1x1.15. However, it has a ST problem. In order to avoid the short circuit in the BC-VSI, the dead-time between the upper and lower switches is needed. This leads to a reduction in the output voltage quality of BC-VSI as compared to the other single-stage Z-source inverters.

For the single-stage conversion, qZSI and AqZSI can work in the ST state, and hence, it does not need any dead-time and compensation circuits. When compared to qZSI, AqZSI uses a higher modulation index to generate the same voltage gain. Thus, a better output quality can be found in the AqZSI.
### Table 3 Experimental circuit parameters

| Parameters | BC-VSI | qZSI | AqZSI with improved PWM scheme |
|------------|--------|------|-------------------------------|
| DC voltage range | 100 V – 350 V | | |
| Power rating | 1.2 kVA | | |
| Output phase voltage | 110 Vrms/50 Hz | | |
| Switching frequency | | 30 kHz | |
| Switching frequency of $S_p$ | 60 kHz | NA | 60 kHz |
| Minimum modulation index | 0.913x1.15 | 0.6x1.15 | 0.913x1.15 |
| Duty cycle $D$ | NA | 0 – 0.4 | 0 – 0.09 |
| $D_0$ | 0 – 0.66 | NA | 0 – 0.55 |

**Fig. 11. A photo of the experimental setup.**

### 6. Experiment Results

To perform a comprehensive comparison, 1.2-kVA SiC-based inverter prototypes are built according to the following specifications. In the power circuit, the inverter feeds to a star-connected resistive load through an $L$-$C$ filter with the values of 1 mH and 10 μF. The input DC voltage range is from 100 V to 350 V. The output phase voltage is 110 Vrms/50 Hz. The switching frequency of H-bridge inverter is 30 kHz. Parameters of BC-VSI, qZSI, and AqZSI are shown in Table 3. Furthermore, all switches of BC-VSI, qZSI, and AqZSI are SiC power MOSFETs SCT3060AL (650 V, 39 A, $R_{DS(on)} = 78$ mΩ).

For qZSI, the selected Z-source network parameters are $L_1 = L_2 = 1$ mH, $C_1 = 220$ μF/400 V and $C_2 = 220$ μF/200 V. The SiC Schottky diodes of IDH16G65C6 are used for $D_1$. In AqZSI, one more SiC MOSFET SCT3060AL and one more SiC Schottky diodes of IDH16G65C6 are added to Z-source network of qZSI. Moreover, the capacitor $C_2$ in AqZSI is changed to 220 μF/100 V. This is because the value of $D$ in AqZSI is decreased by following the flowchart for the modulation index optimization as presented in Section 3. According to (4), the capacitor $C_2$ voltage stress of AqZSI is reduced when $D$ is reduced. Note that the inductance and capacitance selections of AqZSI are considered when AqZSI is operated in the voltage gain of 3.19 and the full-load of 1037 W. To limit the current ripples of $L_1$ and $L_2$ to 10 %, the inductance values of $L_1$ and $L_2$ are selected 1 mH. Also, to limit the voltage ripple of capacitor $C_1$ and $C_2$ to 1%, the capacitances $C_1$ and $C_2$ are selected as 220 μF. In order to ensure AqZSI operates in continuous conduction mode, from (34) and (35), the minimum output power of 145 W is tested.

To confirm the efficiency improvement of AqZSI, the prototype of three-phase BC-VSI is constructed. In the construction of the boost stage of BC-VSI, schottky IDH16G65C6, and a 470 μF/400 V capacitor are used. The dead-time between the two switches on each phase leg is set to 0.4 μs. The values of input and output power of three topologies are obtained from the YOKOGAWA WT230 and HIOKI PW3360 power meter measurements, respectively. In the AqZSI, the values of $M$, $D$, and $D_0$ are selected by following the flowchart calculation in Section 3. In BC-VSI, the modulation index $M$ is fixed at its maximum value of 1x1.15. On the other hand, qZSI control parameters are selected by using $M = 1.15(1 - D)$. Fig. 11 shows a photo of the assembled prototypes and experimental setup.

### 6.1. Experimental waveforms of AqZSI with improved PWM scheme and qZSI

Fig. 12 shows the experimental results of qZSI and AqZSI when $V_i = 100$ V, $V_o = 110$ Vrms, $D = 0.09$, $M = 1.15x0.913$, $R = 40$ Ω, and $R = 88$ Ω. As shown in Fig. 12(a), the peak-to-peak input voltage of AqZSI is 1 A lower than that of qZSI of 1.96 A. In the same way, the peak-to-peak inductor $L_2$ current ripple of AqZSI is 0.5 A is also lower than that of qZSI. In this case, the dc-link voltage of AqZSI is higher than that of qZSI so that the voltage stress of switches on H-bridge circuit of AqZSI can be reduced. Figs. 12(c) show the experimental waveforms of the output voltage current and its harmonics. The measured THD of the output phase current for qZSI and AqZSI are 2.4% and 2.2%, respectively. Compared to qZSI, AqZSI achieves a larger modulation index. Therefore, the output voltage quality of the AqZSI can be improved. In order to verify the AqZSI with improved PWM method, the values of the voltage gain, boost factor, DC-link voltage, capacitors voltage, inductors current and inductors current ripple were measured when the power load changed from 145 W to 1037 W. As shown in Fig. 13, it can be seen that the measured values are slightly changed when the power load is increased.

Fig. 5 also shows the experimental boost factor versus the duty cycle $D_0$ to confirm the near ideal region operation of the converter from the analysis in Section 2.4. The values of the boost factor in experiment are measured at $V_i = 100$ V and full-load of 1037 W when the duty cycle $D_0$ changes from 0 to 0.75. It can be seen from Fig. 5 that the value of parasitic case is matched with experiment case.

Fig. 14 shows the experimental results of the AqZSI with improved PWM scheme when the input voltage is 350 V ($G = 0.91$) and 250 V ($G = 1.27$). In the buck mode with $G = 0.91$, the peak DC-link voltage is equal to the capacitor $C_1$ voltage of 350 V while the switch $S_0$ is always turned off. The value of capacitor $C_1$ voltage is about zero, the measured THD of the output phase current is 2.4% as shown in Fig. 14(a). In this case, the inverter operates with turning switch $S_0$ off and without ST state at a modulation index of 0.91. In Fig. 14(b), the inverter operates at a low boost voltage with $G = 1.27$, maximum modulation index of 1.15 and without ST state. Switch $S_0$ is turned on with $D_0 = 0.1$. It can be seen that the peak DC-link voltage is also equal to the capacitor $C_1$ voltage of 276 V. The measured THD of the output phase voltage.
Fig. 12. Experimental waveforms for qZSI (left side) and AqZSI (right side) with output power of 900 W when $G = 3.19$. From top to bottom: (a) inductor $L_1$ and $L_2$ current, capacitor $C_1$ voltage, DC-link voltage (left side); inductor $L_1$ and $L_2$ current, switch $S_0$ voltage, DC-link voltage (right side); (b) inductor $L_1$ and $L_2$ current, capacitor $C_1$ and $C_2$ voltage; (c) output current and it’s FFT.

Fig. 13. Experimental results of AqZSI with different load values.

Fig. 14. Experimental waveforms of AqZSI with improved PWM scheme at (a) $G = 0.91$, (b) $G = 1.27$. From top to bottom: (a) inductors $L_1$ current, DC-link voltage, capacitor $C_2$ voltage, and output phase current; (b) inductor $L_1$ current, switch $S_0$ voltage, DC-link voltage, and output phase current.
current is 2.3%, while the measured peak-to-peak inductor $L_1$ current is 0.4 A, which is consistent with the calculated value from (28).

6.2. Efficiency Comparison

Figs. 15-16 compare the measured efficiency of BC-VSI, qZSI and AqZSI with improved PWM scheme when the output power is varied from 145 W to 1037 W. The voltage gain in the experiment are $G = 0.91$, $G = 1.05$; $G = 1.27$; $G = 1.5$; $G = 2.167$; and $G = 3.19$. In Figs. 15(a) and 15(b), the ST state in qZSI and AqZSI with improved PWM scheme is not applied, while the additional $S_0$ switch in BC-VSI and AqZSI with improved PWM scheme is turned off. The efficiency of AqZSI with improved PWM scheme is slightly lower than that of BC-VSI and qZSI. This is because AqZSI uses more components than BC-VSI and qZSI. When the voltage gain is increased, the efficiency of BC-VSI is highest. In Fig. 15(c), the efficiency of AqZSI is slightly higher than qZSI when $G = 1.27$. However, the efficiency of AqZSI is always higher than that of qZSI when the voltage gain is higher than 1.27, as shown in Figs. 16(a)-16(c). According to the compared efficiency results, AqZSI with the improved PWM algorithm has a lower ST time and a lower voltage stress of H-bridge switches for the same voltage gain condition. Consequently, AqZSI has a much lower conduction loss in the H-bridge switches and diodes in boost mode when compared with qZSI. Moreover, a large ST duty cycle should be used in qZSI for high voltage gain requirement. This leads to increase in the conduction loss of the H-bridge circuit in qZSI. Therefore, qZSI is not suitable for high voltage gains.

7. Conclusion

An improved PWM control scheme for AqZSI was presented in this paper. Moreover, the optimal operation control of $M$, $D$, and $D_0$ for AqZSI was derived to improve the efficiency and the modulation index. The comparative results between the three-phase BC-VSI, qZSI, and AqZSI under the optimal control condition showed that in boost voltage mode AqZSI with improved PWM scheme performs with a higher efficiency than qZSI but slightly lower than BC-VSI. However, the inductor current ripple of AqZSI with improved PWM scheme is lower than that of BC-VSI and qZSI when $G$ is in the range of (2.56, 9.13) for BC-VSI and full range of $G$ for qZSI. Moreover, AqZSI with proposed PWM scheme improves the modulation index and does not need the dead-time. Compared to conventional PWM scheme in [21] for AqZSI, the improved PWM scheme has higher modulation, lower voltage stress on capacitor $C_2$, diode $D_1$, and H-bridge switches, lower current stress of inductor $L_2$ and shoot-through current stresses lead to reduce the inverter’s size and power losses. The experimental results were presented to confirm the correctness of the analysis. It should be considered that AqZSI with improved PWM scheme can be used to replace qZSI for renewable energy system applications when a wide range of input voltage is required.

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9. References

[1] Abu-Rub, H., Malinowski, M., Al-Haddad, K.: ‘Power electronics for renewable energy systems, transportation and industrial applications’, John Wiley & Sons, Hoboken, NJ, 2014.
[2] Xue, Y., Chang, L., Kjaer, S. B., Bordonau, J., Shimizu, T.: ‘Topologies of single-phase inverters for small distributed power generators: An overview.’ IEEE Trans. Power Electron., 2004, 19, (5), pp.1305–1314
Enhanced impedance source networks for electric applications. Comparison of traditional inverters and Z source topology, three phase quasi-boost inverters with switched Z source inverter to minimize current ripple and voltage stress. IEEE Trans. Ind. Appl., 2006, 42, (3), pp. 770–778

Anderson, J., Peng, F. Z.: ‘A class of quasi-Z-source inverters’. Proc. IEEE IAS’08, 2008, pp. 1 – 7

Siwakoti, Y. P., Peng, F. Z., Blaabjerg, F., Loh, P. C., Town, G. E.: ‘Impedance source networks for electric power conversion part I: a topological review’, IEEE Trans. Power Electron., 2015, 30, (2), pp. 699-716

Shen, M., Joseph, A., Peng, F. Z., Tolbert, L. M., Adams, D. J.: ‘Constant boost control of the Z-source inverter to minimize current ripple and voltage stress’, IEEE Trans. Ind. Appl., 2006, 42, (3), pp. 770–778

Blaabjerg, F., Blaabjerg, F., Loh, P. C., Town, G. E.: ‘Impedance source networks for electric power conversion part I: a topological review’, IEEE Trans. Power Electron., 2015, 30, (2), pp. 699-716

Shen, M., Joseph, A., Peng, F. Z., Adams, D. J.: ‘Comparison of traditional inverters and Z-source inverter for fuel cell vehicles’, IEEE Trans. Power Electron., 2007, 22, (4), pp. 1453-1463

Ayad, A., Kennel, R.: ‘A comparison of quasi-Z-source inverters and conventional two-stage inverters for PV applications’, EPE journal, 2017, 27, (2), pp. 43-59

Panfilov, D., Husev, O., Blaabjerg, Zakis, F., Khandakji, K.: ‘Comparison of three-phase three-level voltage source inverter with intermediate dc–dc boost converter and quasi-Z-source inverter’, IET Power Electron., 2016, vol. 9, no. 6, pp. 1238–1248

Wolski, K., Zdanowski, M., Rabkowski, J.: ‘SiC-based three-phase quasi-Z-source inverter versus the two-stage topology - a comparison’, Proc. 2018 Int. Power Electron. Conf., May 2018, pp. 470–474

Jagan, V., Kotturu, J., Das, S.: ‘Enhanced-boost quasi-Z-source inverters with two switched impedance network’, IEEE Trans. Ind. Electron., 2017, 64, (9), pp. 6885–6897

Nguyen, M. K. et al.: ‘Switched-inductor quasi-Z-source inverter’, IEEE Trans. Power Electron., 2011, 26, (11), pp. 3183-3191

Fathi, H., Madadi, H.: ‘Enhanced-boost Z-source inverters with switched Z-impedance’, IEEE Trans. Ind. Electron., 2016, 63, (2), pp. 691–703

Sun, D., Ge, B., Yan, X., Bi, D., Zhang, H., Liu, Y., Rub, H. A., Brahim, L. B., Peng, F. Z.: ‘Modeling, impedance design, and efficiency analysis of quasi-Z source module in cascaded multilevel photovoltaic power system’, IEEE Trans. Ind. Electron., 2014, 61, (11), pp. 6108-6117

Nguyen, M. K., Le, T. V., Park, S. J., Lim, Y. C., Yoo, J. Y.: ‘A class of high boost inverters based on switched-inductor structure’, IET Power Electron., 2015, 8, (5), pp. 750–759

Nguyen, M. K., Duong, T. D., Lim, Y. C., Kim, Y. G.: ‘Switched-capacitor quasi-switched boost inverters’, IEEE Trans. Ind. Electron., 2018, 65, (6), pp. 5105-5113

Gu, Y. W., Chen, Y. F., Zhang, B.: ‘Enhanced-boost quasi-Z-source inverter with an active switched Z-network’, IEEE Trans. Ind. Electron., 2018, 65, (10), pp. 8372-8381

Nguyen, M. K., Duong, T. D., Lim, Y. C., Choi, J. H.: ‘High Voltage Gain Quasi-Switched Boost Inverters with Low Input Current Ripple’, IEEE Trans. Ind. Informat., 2018, pp. 1–1 (early access). DOI: 10.1109/TII.2018.2806933

Zhu, X., Zhang, B., Qiu, D.: ‘Enhanced boost quasi-Z-source inverters with active switched-inductor boost network’, IET Power Electron., 2018, vol. 11, no. 11, pp. 1774–1787

Nozadian, M. H. B., Babaei, E., Hosseini, S. H., Asl, E. S., “Steady state analysis and design considerations of high voltage gain switched Z source inverter with continuous input current,” IEEE Trans. Ind. Electron., 2017, 64, (3), pp. 5342–5350

Nguyen, M. K., Le, T. V., Park, S. J., Lim, Y. C.: ‘A class of quasi-switched boost inverters’, IEEE Trans. Ind. Electron., 2015, 62, (3), pp. 1526-1536

Nguyen, M. K., Lim, Y. C., Park S. J.: ‘A comparison between single-phase quasi-Z-source and quasi-switched boost inverters’, IEEE Trans. Ind. Electron., 2015, 62, (10), pp. 6336 – 6344

Nguyen, M. K., Tran, T. T., Lim, Y. C., ‘A family of PWM control strategies for single-phase quasi-switched-boost inverter’, IEEE Trans. Power Electron., 2019, 34, (2), pp. 1458-1469

Nguyen, M. K., Choi, Y. O.: ‘PWM control scheme for quasi-switched-boost inverter to improve modulation index’, IEEE Trans. Power Electron., 2018, 33, (5), pp. 4037-4044

Nguyen, M. K., Choi, Y. O.: ‘Maximum boost control method for single-phase quasi-switched-boost and quasi-Z-source inverters’, Energies, 2017, 10, (4): 553