Fabrication of Nanocrystalline Silicon Thin Films Utilized for Optoelectronic Devices Prepared by Thermal Vacuum Evaporation

Magdy S. Abo Ghazala, Hosam A. Othman, Lobna M. Sharaf El-Deen, Mohamed A. Nawwar,* and Abd El-hady B. Kashyout*

Cite This: ACS Omega 2020, 5, 27633−27644

ABSTRACT: Metal-induced crystallization of amorphous silicon is a promising technique for developing high-quality and cheap optoelectronic devices. Many attempts tried to enhance the crystal growth of polycrystalline silicon via aluminum-induced crystallization at different annealing times and temperatures. In this research, thin films of aluminum/silicon (Al/Si) and aluminum/silicon/tin (Al/Si/Sn) layers were fabricated using the thermal evaporation technique with a designed wire tungsten boat. MIC of a:Si was detected at annealing temperature of 500 °C using X-ray diffraction, Raman spectroscopy, and field emission scanning electron microscopy. The crystallinity of the films is enhanced by increasing the annealing time. In the three-layer thin films, MIC occurs because of the existence of both Al and Sn metals forming highly oriented (111) silicon. Nanocrystalline silicon with dimensions ranged from 5 to 300 nm is produced depending on the structure and time duration. Low surface reflection and the variation of the optical energy gap were detected using UV−vis spectroscopy. Higher conductivities of Al/Si/Sn films than Al/Si films were observed because of the presence of both metals. Highly rectifying ideal diode manufactured from Al/Si/Sn on the FTO layer annealed for 24 h indicates that this device has a great opportunity for the optoelectronic device applications.

INTRODUCTION

In the recent decades, polycrystalline silicon devices have attained great attention because it is used for the applications of thin-film solar cells and MOSFET transistors.1−3 MIC of amorphous silicon is a promising method for polycrystalline silicon fabrication at low temperatures. This gives the ability to utilize commercial substrates for thin-film deposition.4 Knappe et al. studied the MIC process for several metals. They found that there are about seven metals that lowered the crystallization temperature. They are Ni, Pt, Pd, Cu, Au, Al, and Ag.5 Al is a cheap and low crystallization temperature metal. Al behaves as a shallow acceptor instead of a contaminant.6 The challenge in the MIC process is to get large grains of poly-silicon at a suitable temperature to the commercial substrates. Nast et al. obtained continuous polycrystalline silicon thin films on low temperature glass substrates. Silicon grain sizes of larger than 10 μm were detected at temperature of 475 °C and annealing times around 1 h.7 Schneider et al. showed that the crystal growth depends on the aluminum oxide membrane between Al and Si layers.8 Matsumura et al. reported that the grain size of grown Si films increases with increasing time of exposure of the Al layer in the open air to form an aluminum oxide membrane. This is due to the suppression of the nucleation during the growth by increasing the thickness of Al2O3 membrane.9 McMahon et al. demonstrated the growth of a (111) oriented crystalline silicon thin film at 725 °C on a glass substrate.10 Maity et al. studied the Al-induced crystallization of amorphous (a)-Si by thermal annealing and rapid heavy ion irradiation. They observed

Received: August 30, 2020
Accepted: September 30, 2020
Published: October 16, 2020

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metal-induced crystallization at 200 °C with the aid of 100 MeV Ni\(^{7+}\) ion irradiance. Neimash et al. investigated the application of laser radiation to provide the tin-induced crystallization in amorphous silicon. They used Raman spectroscopy to measure the size and concentration of formed nanocrystals for the fabrication of nanocrystalline silicon films with a given energy gap width. Mohiddon et al. employed X-ray diffraction (XRD) to detect the crystallinity of Si in the as-deposited layers of Sn and Si thin films annealed at 300–500 °C. They found the appearance of Si(111) peak of the diamond cubic structure with disappearing of Sn peak. The crystallite size of Si increased from 5 up to 18 nm. The layers of metals and silicon were deposited using many techniques such as chemical vapor deposition and electron beam deposition. Ion implantation was employed to produce nanocrystalline silicon.

In this work, we demonstrate the growth of poly-silicon for Al/a-Si and Al/a-Si/Sn thin films via MIC of a:Si using Al and Sn metals. The layers are prepared by thermal vacuum evaporation using a simple homemade designed tungsten boat that can withstand high electrical current to evaporate silicon instead of magnetron sputtering or electron beam techniques. Later mentioned techniques have high cost targets; the impurities that result from unconfined electrons and reactive ions that hit out of the target and other problems had been overcome using the thermal vacuum evaporation technique via this novel designed boat. The growth of Si crystallites depends on the annealing time. The produced thin films are highly oriented Si(111). The effects of the Sn top layer on reducing the surface relectance of different Si thin films, on the variation of the optical energy gap with annealing time and on the conductivity of the films are investigated. Fabrication of an ideal high rectifying diode which is constructed from Al/Si/Sn deposited on the FTO layer annealed at 500 °C for 24 h is demonstrated with \(I-V\) curve under dark and calculations of the series and shunt resistances, ideality factor, and reverse saturation current.

**RESULTS AND DISCUSSION**

**XRD and Raman Analyses.** To investigate the formation of poly-silicon prepared by MIC, XRD was carried out for both two-layer Al/Si and three-layer Al/Si/Sn thin films. Figure 2 shows XRD patterns of Al/Si thin films annealed at 500 °C for different times. It is observed that as-deposited Al/Si thin film does not exhibit any peaks and confirms the amorphous behavior of silicon and aluminum. After annealing the thin film for 4 and 8 h at 500 °C, two peaks are clearly distinguished. One of them at \(2\theta \approx 28.45°\) corresponds to the preferred orientation of Si(111) plane according to JCPDS card no. (01-079-0613) and another one at about \(2\theta \approx 38.5°\) corresponds to Al(111) plane according to JCPDS card no. (04-0787). The height of the Si(111) peak increases with increasing the annealing time. A more intense Si(111) peak is detected for the Al/Si thin film annealed for 8 h than the other one annealed for 4 h by a value of 28%.

Figure 3 shows XRD patterns of Al/Si/Sn thin films annealed at 500 °C for different times. The as-deposited Al/Si/Sn thin film does not exhibit any peak of Si, Al, or Sn and confirms the amorphous behavior of the prepared materials. After annealing the film for 4, 8, 12, and 24 h at 500 °C, a high diffraction peak appears at \(2\theta \approx 28.6°\) corresponds to the preferred orientation of Si(111) plane according to JCPDS card no. (01-079-0613). There is no other peak appears for Al as in the two-layer thin films of Figure 2. In the three-layer thin films, the metal-induced crystallization occurs because of the existence of both Al and Sn metals. Si atoms diffuse in both two layers of metals forming the highly oriented (111) silicon.
structure. It is observed that the height of Si(111) peak increases with increasing the annealing time with a percentage of 37, 87, and 124% for annealing times 8, 12, and 24 h, respectively, respect to the 4 h annealing time. The shifting in the position of Si(111) peak increases with increasing the annealing time from $2\theta = 28.51^\circ$ to $2\theta = 28.68^\circ$, respectively, as the time increased from 4 to 24 h. In the film annealed for 24 h, the height of the peak for Si(111) plane is of the value of 224 counts that is much higher than the other thin films such as the Al/Si/Sn thin film annealed for 4 h with the height of the peak for Si(111) of the value 121 counts. This may be explained that as the film reaches to semi full crystallization of amorphous silicon, its XRD intensity increases significantly. The following Tables 1 and 2 summarize the lattice parameters of the formed polycrystalline silicon of Al/Si and Al/Si/Sn thin films annealed at different times.

### Table 1. Lattice Parameters of the Formed Polycrystalline Silicon and Al of Al/Si Thin Films Annealed at Different Times

| sample     | hkl  | $2\theta$ (degrees) | d-spacing (Å) | lattice const (Å) |
|------------|------|---------------------|---------------|------------------|
| Al/Si 4h   | Si(111) | 28.45              | 3.134         | 5.428            |
| Al(111)    |      | 38.43              | 2.34          | 4.053            |
| Al/Si 8h   | Si(111) | 28.46              | 3.133         | 5.427            |
| Al(111)    |      | 38.54              | 2.33          | 4.041            |

### Table 2. Lattice Parameters of the Formed Polycrystalline Silicon of Al/Si/Sn Thin Films Annealed at Different Times

| sample     | hkl  | $2\theta$ (degrees) | d-spacing (Å) | lattice const (Å) |
|------------|------|---------------------|---------------|------------------|
| Al/Si/Sn 4h| Si(111) | 28.51              | 3.127         | 5.416            |
| Al/Si/Sn 8h| Si(111) | 28.56              | 3.12          | 5.404            |
| Al/Si/Sn 12h| Si(111) | 28.67              | 3.11          | 5.387            |
| Al/Si/Sn 24h| Si(111) | 28.68              | 3.11          | 5.387            |

of the formed polycrystalline silicon of Al/Si and Al/Si/Sn thin films. The values of the lattice constants of the silicon decreased significantly for Al/Si/Sn from 5.416 to 5.387 Å as the annealing time increased from 4 to 24 h. This may be attributed to the addition of Sn layers which increase the pressure in the structure of the film and reduces the interatomic distance because the lattice constant of Sn = 0.649 nm that is larger than the lattice constant of Si = 0.543 nm.20–23

Raman spectroscopy was also employed to validate the presence of nanocrystalline silicon. Figure 4 shows that there is a narrow band at $\approx$15 cm$^{-1}$ for Al/Si/Sn films annealed for 4 and 12 h, which is corresponding to polysilicon and the intensity of the band increases with the increasing of the annealing time. It is an indicator of the increase of the crystallinity.24 This band shifts toward the higher wavenumbers with increasing the annealing time as the size of Si crystallites increases.12

A wide band around 110 cm$^{-1}$ was observed which is due to the overlapping of Sn metal, SiO$_2$ bands. The bands that are at 80, 95, and 160 cm$^{-1}$ correspond to the Sn metal25 and at 120 cm$^{-1}$ corresponds to the SiO$_2$ mode.26 The intensity of Sn metal peak reduces because of the entrance of Sn substitutionally with silicon in the polysilicon lattice. The Sn peaks also shifts toward the higher wavenumbers with the annealing time.27

### Field Emission Scanning Electron Microscopy. Both aSi, Al/Si and Al/Si/Sn annealed thin films were coated with a gold metal thin film to study their morphology and layers exchange. Figure 5a shows the field emission scanning electron microscopy (FESEM) micrograph of an amorphous silicon thin film with evidence of no crystallites as shown. In Figure 5b, FESEM micrograph shows that there is some clusters of crystallites corresponds to polycrystalline silicon that formed after annealing of Al/Si thin films for 4 h because of the layers exchange in the aluminum-induced crystallization of amorphous silicon layer via the eutectic reaction.5,7,22 These crystallites accumulate and form island-like shape.26,29 These islands increase with increasing the annealing time as shown for Al/Si thin films annealed for 4 and 8 h as shown in Figure 5b, and then these islands continuously attached to each other. This may enhance the electron mobility of the formed poly-Si.30

For both Al/Si and Al/Si/Sn thin films, FESEM micrographs show more bright islands with the increasing of the annealing time. But for Al/Si/Sn thin films more brightness islands are appeared because of more accumulation effect as a result of the addition of Sn top layer as shown in Figure 6, so the films of the Sn top layer have rougher surface than other thin films without Sn deposition. This rough surface texturing may cause light trapping and reduce the surface reflectance.31–33 FESEM micrograph of Al/Si/Sn annealed for 24 h shows the appearance of the film seems as a semi full crystalline.34 So, for Al/Si/Sn thin films, the metal induced crystallization is occurred by aluminum and tin layers exchange with the amorphous silicon layer from both the top and bottom of the films. For the thin films annealed for 4, 8, 12, 24 h, FESEM micrographs (Figure 6a–d) show that these islands increased in area with the increasing of the annealing time. This leads to accumulations of the Si island-like shape.
grain boundaries are reduced because of the increasing of the nanocrystallites for polycrystalline silicon and this may be occurred as a result of the layer exchange between aluminum and silicon during the metal induced crystallization of amorphous silicon by aluminum.4,35,36

**Transmission Electron Microscopy.** Figure 7a,b shows transmission electron microscopy (TEM) micrographs of Al/Si thin films annealed at 500 °C for 4 and 8 h. Spherical shapes of the nanocrystallites for polycrystalline silicon are observed as a result of the layer exchange between aluminum and silicon during the metal-induced crystallization of amorphous silicon by aluminum.4,35,36 These nanocrystallites of average size 5 nm accumulated and forming islands of the polycrystalline silicon as shown also in Figure 5b. It is observed that island sizes of the sample annealed for 4 h is small (about 50–80 nm) causing large grain boundaries as shown in the inset of Figure 7a. On the other hand, in the sample annealed for 8 h, the size of islands is larger (about 200–300 nm) as shown in Figure 7b and consequently smaller grain boundaries exist. This is caused by higher crystal growth in the sample annealed for 8 h than the other annealed for 4 h.37,38 Selected area electron diffraction (SAED) shown in the insets of Figure 7a,b indicate the bright spots (crystallites) on the diffraction rings for the polycrystalline silicon and aluminum. For Al/Si/Sn samples, Figure 8a−d shows TEM micrographs of Al/Si/Sn nanocrystals annealed at 500 °C for 4, 8, 12, and 24 h. The accumulation of the crystallites is very small for the thin films annealed for 4 h. This accumulation increases in the films annealed for 8 h. In the sample annealed for 12 h, the accumulated crystallites forming island shapes increase as the annealing time duration increased and these islands shapes began to attach continuously to each other. At the Al/Si/Sn thin film annealed for 24
h, the islands reach to quasi full continuity. The SAED patterns of the total grain area in the inset of Figure 8a−d show a strong spot ring, suggesting that the poly-Si grains has a (111) preferred orientation accompanied by many weak spot rings accounting for the existence of other planes such as (220) and (311) of the polycrystalline silicon.

The possible formation mechanism is shown in Figure 1 as explained from the FESEM and TEM images in Figures 5−8. At longer annealing time of 8 h for Al/a-Si and 24 h for Al/a-Si/Sn, the MIC process is completed as the XRD shows high intensity Si(111) plane. It is associated with Al(111) in the case of a-Si/Al and disappeared in the case of Al/a-Si/Sn. a-Si nanoparticles diffused in the Al and Sn metals at 500 °C annealing temperature in two stages. The first stage is that the deconvolution of a:Si and diffusion in Al to form poly:Si surrounded by aluminum. The second stage is that the diffusion of a:Si into the Sn layer forming polysilicon and at higher annealing times the Sn incorporated substitutionally in the polysilicon\(^2,3,34,39,40\) reducing the lattice constants as confirmed by XRD analyses.

**Optical Properties.** The optical properties of the polysilicon thin films are studied using UV−vis spectroscopy.
Figure 9a,b shows the variation of the reflectance spectra with different annealed Al/Si and Al/Si/Sn thin films deposited on glass substrates. The reflectance blue edge shifted for the thin films as the annealing time increased as well as it decreased with increasing the annealing time. The produced nanocrystalline Si with a top Sn layer have lower reflectance than their values for Al/Si thin films. The reflectance decreases significantly for the higher annealing time sample as shown in Figure 9b. The lower reflectance was confirmed by SEM. Because FESEM micrographs show that the samples with higher annealing time with the Sn top layer have brighter and higher island-like shapes of crystallites that make the surface of the samples is rougher as in the Al/Si/Sn sample annealed for 24 h. The rougher surface scatters the light and reduces the surface reflectance of the samples to the percentage of 10% to reach 0% at about 500 nm of wavelength.\(^2\) Samples that annealed for only 4 h show high reflection than the others annealed for longer annealing time. This is because the short annealing time can not give the chance to aluminum to segregates into the polysilicon rather than the higher annealing times during which the diffusion of aluminum saturates and the transparency of the longer annealed films increases than the shorter annealing time samples or the as-deposited samples as seen in the photographs of the films in Figure 1.\(^4\)

The absorption coefficient was calculated from reflectance and transmittance data using the equation\(^4\)

\[
\alpha = \frac{1}{d} \ln\left(\frac{1 - T}{R}\right)
\]

where \(d\) is the film thickness, \(T\) is the sample transmittance and \(R\) is the sample reflectance. For both crystalline and amorphous semiconductors, the dependence of absorption coefficient \(\alpha\) upon the photon energy takes the formula\(^4\)

\[
\alpha h \nu = A(h \nu - E_g)^n
\]

where \(A\) is a constant, \(E_g\) the optical energy gap in eV, \((h \nu)\) is the energy of photons in eV, and \(n\) is an exponent parameter depending on the nature of optical transition. The usual method for the determination of the optical energy gap, \(E_g\) is the plotting a graph of \((\alpha h \nu)^{1/n}\) versus \((h \nu)\).\(^4\)

Crystalline silicon is considered an indirect transition material.\(^4\) However, it can transfer to direct transition if the thickness of the film is lower than 3.2 nm, the transition undergoes directly because of the quantum confinement as Lin et al. reported.\(^4\) Or it can transfer to a direct transition by incorporation of Sn interstitially in polysilicon lattice as we discussed below. So the optical transition of the polysilicon induced by layer exchange with aluminum in Al/Si annealed films undergoes indirectly.\(^4\,46\) Figure 10 shows Tauc’s plot of Al/Si films. The following Table 3 shows the values of optical energy gap of the prepared samples. The optical energy gap increases as the annealing time increases from 4 to 8 h. For Al/Si/Sn samples, they have direct optical transition as seen in Figure 11. This is due to the incorporation of Sn content as Kurosawa et al. reported.\(^4\) The optical energy gap decreases as the annealing time increases from 4 to 24 h except the sample that annealed for 8 h. The optical energy gap is 2.65 eV corresponding to the Al/Si/Sn annealed for 4 h and increased to 3.02 eV corresponding to the Al/Si/Sn film that annealed for 8 h. Then, the optical energy gap significantly decreases to 2.32 and 2.2 eV corresponding to Al/Si/Sn film annealed for 12 and 24 h, respectively. Mohiddon et al.\(^13\) reported that the optical energy gap is decreased from 3.2 to 2.9 eV for Sn/Si sample annealed for 1 h at temperatures 300, 400, and 500 °C. The lattice constant of Sn = 0.649 nm, i.e. larger than the lattice constant of Si = 0.543 nm. So, the addition of Sn in the thin film and increasing the annealing time increases the pressure in the structure of the film and consequently reduces the interatomic distance. As a sequence, the energy gap decreases.\(^20\,23\) Because the lattice constant of polysilicon for Al/Si samples annealed for 4 h is 5.428 Å, but after the addition of the Sn top layer the lattice constant is equal 5.416 Å corresponds to the Al/Si/Sn film annealed for 4 h. The lattice constant decreased to 5.387 Å for the Al/Si/Sn film annealed for 24 h as seen in Tables 1 and 2.

**Fourier Transform Infrared.** As we discussed above that the optical energy gap decreases as the annealing time increases except the sample that annealed for 8 h. So, Fourier
Transform infrared (FTIR) was employed to investigate the bonding between Si and O that is responsible for the widening of the energy gap.

Figure 12 shows FTIR transmittance of the Al/Si/Sn thin films annealed at 500 °C for 4 and 8 h. It is observed that there are absorption peaks at \( \approx 429 \), \( \approx 768 \), and \( \approx 917 \) cm\(^{-1} \) which correspond to Si–O, Si–O–Si, and Al–O vibrational modes, respectively.\(^{48,49} \) When the annealing time increases, the absorption peaks intensities at \( \approx 429 \) and \( \approx 768 \) cm\(^{-1} \) which correspond to Si–O and Si–O–Si increase. This implies that there is larger number of Si–O bonds in Al/Si/Sn films annealed for 8 h than the other one annealed for 4 h. This large bonding between Si and O increases the energy gap of the film as shown in UV–vis–NIR spectroscopy measurements. Because the energy gap of silicon oxide is larger many times than the pure silicon semiconductor.\(^{50} \)

**DC Conductivity.** A two-probe method was used to investigate the dependence of the electrical conductivity of the prepared thin films on temperature under vacuum \( 8 \times 10^{-3} \) mbar. Two surface electrodes of aluminum were evaporated on the surface of the films. Figure 13a–c shows the DC electrical conductivity versus the temperature in K of amorphous silicon, Al/Si thin films annealed for 4 and 8 h. It is seen that the conductivity of the Al/Si thin films annealed for 4 h and Al/Si thin films annealed for 8 h is higher than the amorphous one. This is because Al prefers to segregate at the grain boundaries. When the concentration of Al is high at the grain boundaries, these insulating boundaries become electrically active and the resistivity of the film decreases.\(^{6} \) Figure 14a–d shows the DC electrical conductivity versus the temperature in K of the Al/Si/Sn thin films annealed for 4, 8, 12, 24 h. It is seen that the conductivity of the Al/Si/Sn thin films annealed for 4, 8, 12, and 24 h is higher than the amorphous one. This is because Al and Sn metals segregate at the insulating grain boundaries.\(^{38} \) When the concentration of Al and Sn top metal is high at the grain boundaries, these insulating boundaries become electrically active and the resistivity of the film decreases.\(^{38} \) It was observed that increasing the annealing time of the samples the electrical conductivity decreases from 40 \( \Omega^{-1} \) m\(^{-1} \) corresponds to Al/Si/Sn annealed for 4 h to 0.4 \( \Omega^{-1} \) m\(^{-1} \) corresponds to Al/Si/Sn annealed for 24 h. The reasons are that: (1) the increasing the bonding between Si atoms and the oxygen atoms in the

| sample          | Al/Si 4h | Al/Si 8h | Al/Si/Sn 4h | Al/Si/Sn 8h | Al/Si/Sn 12h | Al/Si/Sn 24h |
|-----------------|---------|---------|------------|------------|-------------|-------------|
| energy gap (eV) | 2.1     | 2.97    | 2.65       | 3.02       | 2.32        | 2.2         |

**Figure 11.** Tauc plot of the Al/Si/Sn thin films annealed for 4, 8, 12, 24 h on a glass substrate.

**Figure 12.** FTIR spectra of the Al/Si/Sn thin films annealed at 500 °C for 4 and 8 h.

Table 3. Optical Energy Gap Values for Different Annealed Al/Si and Al/Si/Sn Thin Films on A Glass Substrate
membrane of the aluminum oxide as discussed above in FTIR analysis. The second reason is that (2) the annealing time assists the diffusion and solubility of tin. The excess addition of tin changes the electrical conduction from the thermally activation of the charges from the valence band to conduction band into the hopping between the localized states within the energy gap.\textsuperscript{51} The figure shows that the electrical conductivity of the Al/Si/Sn thin films with the tin top layer as a function of the temperature is higher than the electrical conductivity of the Al/Si thin films contain Al metal only. This is due to that high concentrations of metals make the insulating grain boundaries that block the electrons and reduce their mobility more electrically active.\textsuperscript{52}

Figures 15 and 16 show $\ln(\sigma)$ versus $1000/T$ (K)$^{-1}$ plot for a:Si, the annealed Al/Si and the annealed Al/Si/Sn thin films. The values of the activation energy of the films can be calculated from Arrhenius equation. The following Table 4 shows the values of the activation energy of the prepared thin films. It is observed that the amorphous silicon sample has higher activation energy. Silicon is a pure intrinsic semiconductor film. It has higher ionization energy than metals. It is equal 8.15 eV.\textsuperscript{53} Al/Si and Al/Si/Sn thin films which contain one or two layers of metals have lower activation energy than the amorphous silicon thin films. These metals act as dopants during layer exchanging via metal-induced crystallization of the amorphous silicon and introduce shallow energy levels inside the energy gap of the polycrystalline silicon that reduce the activation energy.\textsuperscript{6} From the values of the activation energy, it is seen that when the annealing time increases the activation energy decreases for both Al/Si and Al/Si/Sn thin films except the Al/Si/Sn thin film annealed for 24 h. According to UV–vis–NIR measurements, the calculated Urbach energy of this film is higher than the other films with lower annealing time. Because the annealing time assists the diffusion and solubility of tin. The excess addition of tin changes the electrical
conduction from the thermally activation of the charge carriers from the valence band to conduction band into the hopping between the localized states within the energy gap.51

**FTO/c-Si/Al Device Structuring and Properties.** Aluminum acts as a dopant in the aluminum-induced crystallization of amorphous silicon forming p-type silicon.7 Al/Si/Sn layers were deposited on the FTO/glass substrate and annealed at 500 °C for 24 h forming p–n junction structure as the FTO behaves as a transparent conducting n-layer and Si doped with Al as the p-layer. The diode parameters, that is, series resistance $R_s$, shunt resistance $R_{sh}$, saturation current $I_o$, and the diode quality factor $n$ were investigated via $I–V$ diode characteristics under dark condition using the Shockley equation54

$$I_D = I_o \left[ \exp \left( \frac{q(V + IR_s)}{nkT} \right) \right] + \frac{V - IR_s}{R_{sh}}$$

where, $q$ is the elementary charge, $I_o$ is the reverse saturation current, $k$ is Boltzmann constant, $V$ is voltage across the diode, $n$ is the diode quality factor, $R_s$ is the series resistance, and $T$ is the temperature in kelvin and the $I–V$ measurements were carried out at room temperature using a computer-controlled potentiostat (Metrohm Autolab, model: 87070) under a scan rate of 10 mV/s within the range between $-1$ and $+1$ V.

Figure 17 shows the measured $I–V$ characteristics under dark conditions of the formed device as structured in the inset of the figure. It is observed that there is not detected high reverse current, which is normally caused by the structural defects;54–56 therefore this device structure acts as an ideal diode. We deduced the value of the ideality factor of the diode ($n$) from plotting $\ln(I)$ versus $V$ as seen in Figure 18.

The low value of the series resistance, the high value of the shunt resistance, and the ideality factor that is very close to one indicate that the diode has an ideal behavior and well-manufactured (Table 5). It is a good indicator for promising applications in rectification and solar cells.57,58 The conduction mechanism is divided into three regions (1, 2, 3). In region (1) for the lower voltages, the ideality factor $n \approx 1$ where the total diode current would be based only on the diffusion process. No recombination processes happened inside the space-charge region of the junction. It causes the minimization of reverse current loss and increasing in the rectification ratio $I_1/I_2$ to a very high ratio that is equal 25,803 that makes this fabrication process a promising device in many rectification applications.47 However, in the region (2) with higher voltages, $n = 109.2$, which caused by the recombination of electrons in holes because of the presence of aluminum impurity located interstitially in the crystal lattice of silicon and the tunneling motion of charge carriers due to electron cloud screening in the aluminum accumulations. Electrons may be dropped into the trap from the conduction band and recombine with holes that are presented by aluminum dopant in the c-Si as proofed by XRD and energy dispersive X-ray (EDX) analyses.59,60 In region (3), in the reverse bias $n = 6.83$. In this region, the rectifying behavior appears. Because of the current value is very small in order of $10^{-9} \text{A}$ due to the recombination of electrons in holes because of the presence of aluminum impurity atoms located interstitially in the crystal lattice of silicon.61

**CONCLUSIONS**

Metal-induced crystallization of thermally vacuum evaporated amorphous silicon via aluminum and tin metals were successfully synthesized and studied. The crystallinity of the evaporated thin films is greatly increased with increasing annealing time duration. For both Al/Si and Al/Si/Sn thin films, the Si(111) plane is revealed after the increasing of the annealing time for several hours at 500 °C. Thin films with Sn layers show lower surface reflectance to 10% than the other samples fabricated without the Sn layer on the surface. The addition of the Sn layer lowers the energy gap to 2.2 eV because it increases the pressure in the structure of the film and reduces the interatomic distance. The activation energy decreases for both Al/Si and Al/Si/Sn thin films as the
Table 5. Shows the Calculated Series Resistance $R_s$, Shunt Resistance $R_{sh}$, Saturation Current $I_{sat}$, Threshold Voltage $V_{th}$, and the Ideality Factor $n$ of the Formed Diode

| $R_s$ (Ω) | $R_{sh}$ (Ω) | $V_{th}$ (V) | $I_{sat}$ (A) | $n$ |
|-----------|--------------|-------------|---------------|-----|
| 0.955     | 3.2 $\times$ 10^7 | 0.37        | 1.026 $\times$ 10^{-3} | region (1) |
|           |              |             | 2.74 $\times$ 10^{-3} | region (2) |
|           |              |             | 5.07 $\times$ 10^{-9} | region (3) |
|           |              |             | 1.056          | region (1) |
|           |              |             | 109.2          | region (2) |
|           |              |             | 6.83           | region (3) |

annaling time increases except the Al/Si/Sn thin film annealed for 24 h. Because Sn changes the electrical conduction from the thermally activation of the charge carriers from the valence band to conduction band into the hopping between the localized states within the energy gap. High rectifying diode with the rectification ratio of the value of 25,803 and ideality factor of the value of 1.056 constructed from Al/Si/Sn deposited on the FTO layer annealed at 500 °C for 24 h can be a promising device in many rectification applications.

**EXPERIMENTAL SECTION**

Polycrystalline silicon thin film was deposited on commercial glass substrates. Glass substrates were first washed by hot water and soap, and cleaned by ultrasonic washer, then dried at 150 °C and wiped with acetone. Layers of aluminum and silicon thin films were evaporated by thermal vacuum evaporation using a tungsten triple wire boat at vacuum 2 × 10^{-3} mbar using the Edwards E306A coating unit for the films of amorphous Al/Si, as shown in Figure 1. The thickness of the layers was measured using a quartz crystal thickness monitor (MAXTEK INC. TM-100). Thin films of aluminum, silicon, and tin are also coevaporated by the thermal evaporator under the same conditions for Al and Si layers and then the Sn layer of thickness 30 nm was evaporated at a current value of 12 A. The aluminum layer exposure for 1 h in open air before the evaporation of the other layers so that the Al$_2$O$_3$ membrane is formed. The films are then annealed under vacuum 2 × 10^{-3} mbar at 500 °C for 4 and 8 h for Al/Si thin films and 4, 8, 12, and 24 h for Al/Si/Sn thin films. The resulting polycrystalline thin films were characterized using the X-ray diffractor (SHIMADZU 6100 LabX), Raman spectrometer (SENTERRA BRUKER) with laser wavelength (514 nm), field emission scanning electron microscope (QUANTA FEG 250), EDX spectroscopy analysis, and transmission electron microscope (JEOL 1230). The optical properties of the prepared thin films were investigated using the UV–vis–NIR spectrometer (JASCO V-570). Infrared spectra transmittance was carried out using (BRUKER VERTEX 80). The I–V measurements were carried out at room temperature using a computer-controlled potentiostat (Metrohm Autolab, model: 87070) under a scan rate of 10 mV/s within the range between −1 and +1 V.

**AUTHOR INFORMATION**

**Corresponding Authors**

Mohamed A. Nawwar — Physics Department, Faculty of Science, Menoufia University, Shebin El-Kom, Menoufia 32511, Egypt; orcid.org/0000-0002-2837-8115; Email: mohamed.nawwar@science.menoufa.edu.eg

Abd El-hady B. Kashyout — Electronic Materials Department, Advanced Technology and New Materials Research Institute, City of Scientific Research and Technological Applications (SRTA-City), New Borg El-Arab City, Alexandria 21934, Egypt; Email: akashyout@srtacity.scil.edu.

**Authors**

Magdy S. Abo Ghazala — Physics Department, Faculty of Science, Menoufia University, Shebin El-Kom, Menoufia 32511, Egypt

Hosam A. Othman — Physics Department, Faculty of Science, Menoufia University, Shebin El-Kom, Menoufia 32511, Egypt

Lobna M. Sharaf El-Deen — Physics Department, Faculty of Science, Menoufia University, Shebin El-Kom, Menoufia 32511, Egypt

Complete contact information is available at: https://pubs.acs.org/10.1021/acsomega.0c04206

**Notes**

The authors declare no competing financial interest.

**ACKNOWLEDGMENTS**

The authors gratefully acknowledge Physics Department, Faculty of Science, Menoufia University as it introduced many facilities in the preparation of the samples of this work and Electronic Materials Department, Advanced Technology and New Materials Research Institute, City of Scientific Research and Technological Applications (SRTA-City), Egypt-Japan University for Science and Technology, New Borg El-Arab City, Alexandria, and the National Research Centre, Dokki, Giza, Egypt as they introduce many facilities in the investigations and measurements techniques of the work.

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