Conduction Mechanism Analysis of Abrupt- and Gradual-Switching InGaZnO Memristors

Woo Sik Choi¹, Min Suk Song², Hyungjin Kim²,∗ and Dae Hwan Kim¹,∗

¹ School of Electrical Engineering, Kookmin University, Seoul 02707, Korea
² Department of Electronic Engineering, Inha University, Incheon 22212, Korea
∗ Correspondence: hkim@inha.ac.kr (H.K.); drlife@kookmin.ac.kr (D.H.K.)

Abstract: In this work, two types of InGaZnO (IGZO) memristors were fabricated to confirm the conduction mechanism and degradation characteristics of memristors with different electrode materials. The IGZO memristor exhibits abrupt switching characteristics with the Pd electrode owing to the formation and destruction of conductive filaments but shows gradual switching characteristics with the p-type Si electrode according to the amount of generated oxygen vacancy. The electrical characteristics and conduction mechanisms of the device are analyzed using an energy band diagram and experimentally verified with random telegraph noise characteristics confirming the trap effects on the device conduction.

Keywords: memristor; InGaZnO; gradual and abrupt switching; conduction mechanism; oxygen vacancy; random telegraph noise

1. Introduction

Recently, a neuromorphic system has been widely studied to supplement the computing efficiency of a von Neumann structure [1–5]. Unlike conventional computing architectures, it can process data efficiently thanks to a parallel structure, and quickly maximize energy efficiency and operation speed, increasing the feasibility of in-memory computing in which computations can be conducted inside memory devices. Nonvolatile memories, such as memristors, flash memories, and ferroelectric memories, are being studied as synapses to store weight values for vector-matrix multiplications [6–15]. Especially a memristor is one of the most potential candidates because of its fast switching speed, low operation voltage, and simple structure having two terminals, which leads to a cross-point array structure with superior advantages of a high-density parallel-connected structure [16–25].

Memristor devices can be divided into abrupt and gradual types based on their switching characteristics. An abrupt-switching memristor switches with the formation and collapse of a conductive filament (CF) constructed by oxygen vacancy (V_O) and has binary conductance states [26–29]. Although abrupt-switching memristors have fast switching and good retention characteristics, they have limitations in terms of expressing the floating-point weight values of artificial neural networks and significant disadvantages in terms of endurance and device variation owing to the nonuniformly formed and ruptured CF [30,31]. In contrast, gradual-type devices are switched according to the amount of V_O generated near the interface between the electrode or switching layer, resulting in multiconductance states; they tend to have the disadvantages of poor retention characteristics and relatively slow switching speeds because of the interface-type conducting path [32–40].

In this study, we fabricated two types of devices with different electrode materials (Pd/InGaZnO(IGZO)/Pd and Pd/IGZO/SiO2/p-type Si), and their electrical characteristics are analyzed. IGZO is widely used as a channel material for display devices thanks to high mobility and uniformity and has a great advantage in cointegration with CMOS circuitry through a low-temperature process [41–46]. Depending on the bottom electrode,
the abrupt and gradual switching characteristics are analyzed through an energy band diagram, and conduction mechanisms are verified by replotted current (I)–voltage (V) characteristics. In addition, the random telegraph noise (RTN) signals of both devices are analyzed to verify the presence or absence of the CF in each device.

2. Materials and Methods

The two types of IGZO memristors are fabricated having an active area of $10 \times 10 \text{µm}^2$ with the different electrodes, respectively, as shown in Figure 1a,b. Sample #1 (S1) has a Pd bottom electrode (BE), and sample #2 (S2) has p-type Si BE and an additional SiO$_2$ layer. The bottom electrode (BE) was deposited using an e-beam evaporator for both samples. For the S1, 40 nm of Pd was deposited as the BE, and 40 nm of p$^+$-silicon was deposited as the BE for the S2. Then, 60 nm of the IGZO layer was deposited with Ar/O$_2$ flow using radio frequency (RF) sputtering (150 W). The IGZO layer was deposited with a ratio of In:Ga:Zn = 1:1:1.

For the top electrode (TE), 40 nm of Pd was deposited on both devices using an e-beam evaporator. The electrical characteristics in this work were measured using a semiconductor parameter analyzer (Keithley 4200-SCS). Figure 1c shows the electrical switching characteristics of S1 and S2 with a feature size of 10 µm. (e,f) Cumulative probability plot for both HRS and LRS of S1 and S2 measured at 0.1 V.

For the top electrode (TE), 40 nm of Pd was deposited on both devices using an e-beam evaporator. The electrical characteristics in this work were measured using a semiconductor parameter analyzer (Keithley 4200-SCS). Figure 1c shows the electrical switching characteristics of the S1. The device was formed by a positive voltage sweep of up to 8 V, and 10 mA of compliance current was applied to prevent device overshoot during the forming process. A positive voltage sweep to 6 V was performed for a set operation, whereas a reset operation was performed through a negative voltage sweep to $-2.5 \text{V}$. It is clearly observed that abrupt digital switching occurs during the set and reset processes in the S1 because of the formation and destruction of the CF. In contrast, the forming of the
S2 was conducted with a negative voltage sweep to \(-20\) V, as shown in Figure 1d. A positive sweep to 6 V and a negative sweep to \(-4\) V were performed for the set and reset operations, respectively. Unlike the S1, the S2 has gradual switching characteristics, which means the device state can be gradually in the set and reset operations because of the \(V_O\) generation. Figure 1d,f summarize the cumulative probability of 100 devices for both samples with regard to the high resistive state (HRS) and low resistive state (LRS). It is confirmed that the S1 has a wider state distribution than the S2 because the S1 state changes abruptly by the randomly formed and ruptured CF. These switching behaviors cause a difference in the endurance characteristics of the two samples, as shown in Figure 2. Because the abrupt switching characteristics of the S1 can cause enough stress to the switching layer, the S1 fails to switch after 150 switching cycles between LRS and HRS; however, the S2 can switch over 500 cycles thanks to the gradual switching characteristics.

Figure 2. Endurance switching characteristics of (a) S1 and (b) S2 read at 0.1 V.

3. Results

The \(I–V\) characteristics of both samples are replotted to investigate the conduction mechanism of each sample, as shown in Figure 3. A total of three devices are verified for the analysis of the conduction mechanism. It is verified that the HRS of the S1 is conducted by the Poole–Frenkel emission since the device current has a relation of \(\ln \left(\frac{I_{\text{RRAM}}}{V}\right) \propto \sqrt{V}\), which means that the Schottky barrier (SB) between the IGZO and BE is high enough to suppress thermionic emission from the BE. In addition, the dominant conduction at the LRS of the S1 is confirmed as ohmic conduction, which means that the strong CF is formed during the set operation, and electrons can easily move to the conduction band. In contrast, the dominant conduction mechanism of the S2 is analyzed as thermionic emission regardless of the device state since the \(I–V\) characteristics can be expressed as \(\ln(I_{\text{RRAM}}) \propto \sqrt{V}\) despite the bias polarity. This implies that the device state of the S2 can be controlled by the SB height (\(\phi_B\)) modulation, and the conductance level is modulated in analog grade accordingly.

To analyze the switching mechanisms of both samples more thoroughly, the flat band diagram and energy band diagram at equilibrium, including work function, electron affinity, and bandgap of the S1 and S2, are illustrated in Figure 4a,b, respectively [47,48]. It is expected that the Schottky barrier near the BE of the S1 is 0.8 eV and can become small similar to the ohmic junction, after the forming process. On the other hand, the SiO\(_2\) layer inherently formed during the deposition step is placed between the IGZO and BE layers and forms a higher SB than the S1, resulting in a lower-level operation current. It is expected that the device state of the S2 can be controlled by the electron trapping at the interface states between the IGZO and SiO\(_2\) layers, leading to the gradual switching characteristics.
Figure 3. Replotted $I-V$ switching characteristics of a total of 3 devices. (a,b) log($I$/V)–sqrt($V$) plots of S1 and (c,d) log($I$)–sqrt($V$) plots of S2 under positive and negative bias conditions.

Figure 4. Flat band diagram and energy band diagram in the equilibrium of (a) S1 (Pd/IGZO/Pd) and (b) S2 (Pd/IGZO/SiO$_2$/p-type Si).
To confirm the switching mechanism of S2, the $\phi_B$ with respect to the TE voltage is extracted, as shown in Figure 5a, using the following equation:

$$\ln \left( \frac{I_{\text{RAM}}}{V_{TE}} \right) = \phi_B \frac{q}{kT}$$

where $T$ is the absolute temperature, $q$ is the amount of charge, and $k$ is the Planck constant.

It is verified that the $\phi_B$ is gradually modulated from 0.38 eV to 0.11 eV (0.27 eV of $\phi_B$ difference) as the voltage is increased, and accordingly, the device state becomes more conductive by thermionic emission. The $\phi_B$ is also extracted from the Arrhenius plot of $\ln \left( \frac{I_{\text{RAM}}}{T^2} \right)$ for both states (LRS and HRS), as shown in Figure 5b, which also confirms that the $\phi_B$ difference is 0.24 eV, and two states can be programmed according to the $\phi_B$ modulation. Figure 5c illustrates the change in the $\phi_B$ with respect to the applied voltage and movement of electrons using an energy band diagram. The $\phi_B$ modulation can be explained by the electric field-induced oxygen ion migration, depending on the bias conditions [49,50]. At a low voltage, electrons cannot move easily because of the SB between the SiO$_2$ layer and p-type Si BE. However, as the voltage is increased, oxygen vacancies at the interface of SiO$_2$-Si are placed higher than the Fermi level, and they are ionized into VO$_{2+}$ and electrons. The electric field generated by VO$_{2+}$ ions reduces the $\phi_B$, which allows electrons to cross the SB (set process). On the other hand, when a negative voltage is applied, the energy state of the oxygen vacancies is lower than that of the Fermi level, and the ionized VO$_{2+}$ becomes neutralized VO. Therefore, the lowered $\phi_B$ by ionized VO$_{2+}$ is restored to its original height, and it becomes difficult for electrons to cross the SB (reset process).

Figure 5. (a) $\phi_B$ of S2 according to the applied voltage. (b) Arrhenius plot of $I/T^2$ for S2 to extract $\phi_B$. (c) Energy band diagrams of S2 during the set and reset operation.
The schematic diagram summarizing the conduction mechanism of each device is illustrated in Figure 6. Figure 6a shows the switching operations of the S1. First, when a positive voltage is applied to the TE, oxygen ions drift toward the TE, and a conductive filament composed of $V_O^{2+}$ is formed. In contrast, when the negative bias is applied to the TE, oxygen ions move back toward the bottom electrode, and the CF is ruptured by the recombination of $V_O^{2+}$ and oxygen ions, resulting in increased resistance. Once the forming process is conducted, the CF can be easily formed at a lower voltage than the forming process because of the residual filament. Figure 6b shows the switching operations of the S2. As a strong negative voltage is applied to the TE, $V_O^{2+}$ are generated near the interface between the IGZO and SiO$_2$ layers because the oxygen ions drift to the BE. This is because the SiO$_2$ layer is more resistant than the IGZO layer, so most of the electrical field is applied across the SiO$_2$ layer. Due to the drift of oxygen ions, soft breakdown occurs first in the IGZO layer with low resistance, which leads to the formation of conductive filaments in the IGZO layer [51]. As a result of the oxygen ions drift, the SiO$_2$ layer is thickened from 1.2 nm to 2.1 nm after the forming process, as shown in the transmission electron microscopy (TEM) images. The ionized $V_O^{2+}$ lowers the $\phi_B$ and electrons can move easily through thermionic emission, resulting in a decrease in resistance. After the forming process, $V_O^{2+}$ can become $V_O$ by the electron occupancy depending on the bias condition, resulting in the $\phi_B$ modulation discussed above.

Lastly, the RTN signals of both devices were measured to analyze the electron trapping effects depending on the conduction mechanism. RTN is a type of intrinsic random noise, and it refers to a phenomenon in which device current randomly fluctuates by trapping or de-trapping of electrons [52,53]. In general, the RTN signals can be obtained when the CF is ruptured, and the device conduction is dominated by trap-assisted transport, but rarely occurs when the CF is formed since the CF can be hardly affected by electron trapping. The transient characteristics of the device current for the S1 and S2 were measured for 2 s (sample frequency = 10 kHz) under 0.1 V of the TE voltage, as shown in Figure 7a and b, respectively, which confirms that the RTN signals only occur in the HRS of the S1. This implies that the HRS of the S1 is conducted by trap-assisted transport, such as the Pool–Frenkel effect, which is in line with what has been discussed above. In contrast, the noise signals observed in the S2, regardless of the state, are believed to be thermal or 1/f noise.
noise rather than RTN signals [54] since its conduction mechanism is thermionic emission for both states, meaning that the S2 is hardly disturbed by intrinsic random noise during the read operation.

4. Conclusions

In this study, the conduction mechanisms of abrupt and gradual switching characteristics of IGZO memristors were analyzed. Because of the different BE material, the switching operation of the S1 was obtained by the formation and rupture of the CF, resulting in the abrupt switching, whereas that of the S2 was obtained by the $\phi_B$ modulation, resulting in the abrupt switching behaviors. The RTN measurement also confirmed that the S2 was affected by the electron trapping in the HRS because the trap-assisted transport of the S2 was not affected by the electron trapping caused by thermionic emission conduction. We believe that the interface-type switching in the S2 without the trapping effect can be preferred in a neuromorphic system where the memristor device represents floating-point weight values thanks to both gradual switching characteristics and robustness to the intrinsic random noise source.

Author Contributions: Methodology, W.S.C. and M.S.S.; formal analysis, W.S.C.; data curation, M.S.S.; writing—original draft preparation, W.S.C. and M.S.S.; writing—review and editing, H.K. and D.H.K.; funding acquisition, H.K., D.H.K., W.S.C. and M.S.S. All authors contributed equally to this work. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the National Research Foundation of Korea (NRF) grant funded by the Korean Government (MSIT) (No. 2016R1A5A1012966, 30%, No. 2020R1A2B5B01001979, 25%, and No. 2022M3I7A1085471, 25%), partly by the Institute of Information and Communications

Figure 7. I-t characteristics of (a) S1 and (b) S2 under 0.1 V for both HRS and LRS.
Technology Planning and Evaluation (IITP) grant funded by the Korea government (MSIT) (No. 2021-0-01764, 20%), and in part by the Brain Korea 21 Four Program.

Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Hochstetter, J.; Zhu, R.; loeffler, A.; Diaz-Alvarez, A.; Nakayama, T.; Kuncic, Z. Avalanches and edge-of-chaos learning in neuromorphic nanowire networks. Nat. Commun. 2021, 12, 4008. [CrossRef] [PubMed]

2. Kim, T.-H.; Kim, S.; Hong, K.; Park, J.; Hwang, Y.; Park, B.-G.; Kim, H. Multilevel switching memristor by compliance current adjustment for off-chip training of neuromorphic system. Chaos Solitons Fractals 2021, 153, 115877. [CrossRef]

3. Choi, M.; Lee, M.; Lee, B.; Lee, Y.T. Multigate opto-neuromorphic process system based on commercial optoelectric devices. Curr. Appl. Phys. 2020, 10, 1125–1129. [CrossRef]

4. Hsu, C.-L.; Saleem, A.; Singh, A.; Kumar, D.; Tseng, T.-Y. Enhanced linearity in CBRAM synapse by post oxide deposition annealing for neuromorphic computing applications. IEEE Trans. Electron Devices 2021, 68, 5578–5584. [CrossRef]

5. Lee, G.S.; Jeong, J.S.; Yang, M.; Song, J.D.; Lee, Y.T.; Ju, H. Non-volatile memory behavior of interfacial InOx layer in InAs nano-wire field-effect transistor for neuromorphic application. Appl. Surf. Sci. 2021, 541, 148483. [CrossRef]

6. Seo, Y.-T.; Kwon, D.; Noh, Y.; Lee, S.; Park, M.-K.; Woo, S.Y.; Park, B.-G.; Lee, J.-H. 3-D AND-type flash memory architecture with high-k gate dielectric for high-density synaptic devices. IEEE Trans. Electron Devices 2021, 68, 3801–3806. [CrossRef]

7. Kim, S.K.; Geum, D.-M.; Lim, H.-R.; Han, J.; Kim, H.; Jeong, Y.; Kim, S.-H. Photo-responsible synapse using Ge synaptic transistors and GaAs photodetectors. IEEE Electron Device Lett. 2020, 41, 605–608. [CrossRef]

8. Hwang, S.; Yu, J.; Lee, G.H.; Song, M.S.; Chang, J.; Min, K.K.; Jang, T.; Lee, J.-H.; Park, B.-G.; Kim, H. Capacitor-based synaptic devices for hardware spiking neural networks. IEEE Electron Device Lett. 2022, 43, 549–552. [CrossRef]

9. Shen, J.-X.; Li, H.; Wang, W.-H.; Wang, S.-G.; Sun, Y. Artificial synaptic device and neural network based on the FeGa/PN-PT/FeGa memtransistor. Appl. Phys. Lett. 2021, 119, 192902. [CrossRef]

10. Nguyen, M.-C.; Lee, K.; Kim, S.; Youn, S.; Hwang, Y.; Kim, H.; Choi, R.; Kwon, D. Incremental drain-voltage-ramping training method for ferroelectric field-effect transistor synaptic devices. IEEE Electron Device Lett. 2021, 43, 17–20. [CrossRef]

11. Xu, Y.; Liu, W.; Huang, Y.; Jin, C.; Zhou, B.; Sun, J.; Yang, J. Recent advances in flexible organic synaptic transistors. Adv. Electron. Mater. 2021, 7, 2100336. [CrossRef]

12. Li, S.; Lyu, H.; Li, J.; He, Y.; Gao, X.; Wan, Q.; Shi, Y.; Pan, L. Multiterminal ionic synaptic transistor with artificial blink reflex function. IEEE Electron Device Lett. 2021, 42, 351–354. [CrossRef]

13. Shao, L.; Zhao, Y.; Liu, Y. Organic synaptic transistors: The evolutionary path from memory cells to the application of artificial neural networks. Adv. Funct. Mater. 2021, 31, 2101951. [CrossRef]

14. Cho, S.W.; Kwon, S.M.; Kim, Y.-H.; Park, S.K. Recent progress in transistor-based optoelectronic synapses: From neuromorphic computing to artificial sensory system. Adv. Intell. Syst. 2021, 3, 2000162. [CrossRef]

15. Park, S.; Jang, J.T.; Hwang, Y.; Lee, H.; Choi, W.S.; Kang, D.; Kim, C.; Kim, H.; Kim, D.H. Effect of the gate dielectric layer of flexible InGaZnO synaptic thin-film transistors on learning behavior. ACS Appl. Electron. Mater. 2021, 3, 3972–3979. [CrossRef]

16. Kim, H.; Mahmoudi, M.; Nili, H.; Strukov, D.B. 4K-memristor analog-grade passive crossbar circuit. Nat. Commun. 2021, 12, 5198. [CrossRef]

17. Li, Y.; Ang, K.-W. Hardware implementation of neuromorphic computing using large-scale memristor crossbar arrays. Adv. Intell. Syst. 2021, 3, 2000137. [CrossRef]

18. Feng, Y.; Huang, P.; Zhao, Y.; Shan, Y.; Zhang, Y.; Zhou, Z.; Liu, L.; Liu, X.; Kang, J. Improvement of state stability in multi-level resistive random-access memory (RRAM) array for neuromorphic computing. IEEE Electron Device Lett. 2021, 42, 1168–1171. [CrossRef]

19. Milo, V.; Glukhov, A.; Perez, E.; Zambelli, C.; Lepri, N.; Mahadevaiah, M.K.; Quesada, E.P.-B.; Olivo, P.; Wenger, C.; Ielmini, D. Accurate program/verify schemes of resistive switching memory (RRAM) for in-memory neural network circuits. IEEE Trans. Electron Devices 2021, 68, 3832–3837. [CrossRef]

20. Li, H.; Wang, S.; Zhang, X.; Wang, W.; Yang, R.; Sun, Z.; Feng, W.; Lin, P.; Wang, Z.; Sun, L.; et al. Memristive crossbar arrays for storage and computing applications. Adv. Intell. Syst. 2021, 3, 2100017. [CrossRef]

21. Kim, T.-H.; Kim, S.; Hong, K.; Park, J.; Youn, S.; Lee, J.-H.; Park, B.-G.; Kim, H. Effect of program error in memristive neural network with weight quantization. IEEE Trans. Electron Devices 2022, 69, 3151–3157. [CrossRef]

22. Sahu, D.P.; Jetty, P.; Jammalamadaka, S.N. Graphene oxide based synaptic memristor device for neuromorphic computing. Nanotechnology 2021, 32, 155701. [CrossRef] [PubMed]

23. Nikam, H.; Satyam, S.; Sahay, S. Long short-term memory implementation exploiting passive RRAM crossbar array. IEEE Trans. Electron Devices 2022, 69, 1743–1751. [CrossRef] [PubMed]

24. Sakellaropoulos, D.; Bousoulas, P.; Papakonstantinopoulos, C.; Kitsios, S.; Tsoukalas, D. Impact of active electrode on the synaptic properties of SiO2-based forming-free conductive bridge memory. IEEE Trans. Electron Devices 2021, 68, 1598–1603. [CrossRef]
25. Bousoulas, P.; Sakellaropoulos, D.; Tsoukalas, D. Tuning the analog synaptic properties of forming free SiO2 memristors by material engineering. *Appl. Phys. Lett.* 2021, 118, 143502. [CrossRef]

26. Lv, J.; Wang, S.; Li, F.; Liang, Q.; Yang, M.; Ma, X.; Wang, H.; Hao, Y. A physically transient self-rectifying and analogue switching memristor synapse. *IEEE Electron Device Lett.* 2021, 42, 1599–1602. [CrossRef]

27. Giacomin, E.; Greenberg-Toledo, T.; Kvatinsky, S.; Gaillardon, P.-E. A robust digital RRAM-based convolutional block for low-power image processing and learning applications. *IEEE Circuits Syst. I Regul. Pap.* 2018, 66, 643–654. [CrossRef]

28. Chuang, K.-C.; Chu, C.-Y.; Zhang, H.-X.; Luo, J.-D.; Li, W.-S.; Li, Y.-S.; Cheng, H.-C. Impact of the stacking order of HfO2 and AlOx dielectric films on RRAM switching mechanisms to behave digital resistive switching and synaptic characteristics. *IEEE J. Electron Devices Soc.* 2019, 7, 589–595. [CrossRef]

29. Lin, C.-Y.; Wu, C.-Y.; Wu, C.-Y.; Lee, T.-C.; Yang, F.-L.; Hu, C.; Tseng, T.-Y. Effect of top electrode material on resistive switching properties of ZrO2 film memory devices. *IEEE Electron Device Lett.* 2007, 28, 366–368. [CrossRef]

30. Chen, B.; Kang, J.F.; Gao, B.; Deng, Y.X.; Liu, L.F.; Liu, X.Y.; Fang, Z.; Yu, H.Y.; Wang, X.P.; Lo, G.Q. Endurance degradation in metal oxide-based resistive memory induced by oxygen ion loss effect. *IEEE Electron Device Lett.* 2013, 34, 1292–1294. [CrossRef]

31. Chen, B.; Lu, Y.; Gao, F.; Yu, Z.; Zhang, F.; Huang, P.; Chen, Y.; Liu, L.; Liu, X.; Kang, J. Physical mechanisms of endurance degradation in TMO-RRAM. In Proceedings of the 2011 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 5–7 December 2011; pp. 12.13.11–12.13.14.

32. Choi, W.S.; Jang, J.T.; Kim, D.; Yang, T.J.; Kim, C.; Kim, H.; Kim, D.H. Influence of Al2O3 layer on InGaZnO memristor crossbar array for neuromorphic applications. *Chaos Solitons Fractals* 2012, 50, 111813. [CrossRef]

33. Yang, J.; Cho, H.; Ryu, H.; Ismail, M.; Mahata, C.; Kim, S. Tunable synaptic characteristics of a Ti/TiO2/Si memory device for reservoir computing. *Appl. Mater. Interfaces* 2021, 13, 33244–33252. [CrossRef] [PubMed]

34. Li, X.; Wu, H.; Gao, B.; Wu, W.; Wu, D.; Deng, N.; Cai, J.; Qian, H. Electrode-induced digital-to-analog resistive switching in TaOx-based RRAM devices. *Nanotechnology* 2016, 27, 305201. [CrossRef] [PubMed]

35. Song, W.; Wang, W.; Lee, H.K.; Li, M.; Zhuo, Y.Y.-Q.; Chen, Z.; Chui, K.J.; Liu, J.-C.; Wang, T.-T.; Zhu, Y. Analog switching characteristics in Ti/W/Al2O3/TaOx/Ta RRAM devices. *Appl. Phys. Lett.* 2019, 115, 135301. [CrossRef]

36. Cho, S.; Jung, J.; Kim, S.; Pak, J.J. Conduction mechanism and synaptic behaviour of interfacial switching AlOx-based RRAM. *Semicond. Sci. Technol.* 2020, 35, 085006. [CrossRef]

37. Moon, K.; Fumarola, A.; Sidler, S.; Jang, J.; Narayanan, P.; Shelby, R.M.; Burr, G.W.; Hwang, H. Bidirectional non- filamentary RRAM as an analog neuromorphic synapse, Part I: Al/Mo/Pr2O3/MnO2 material improvements and device measurements. *IEEE Electron Devices Soc.* 2017, 6, 146–155. [CrossRef]

38. Woo, J.; Yu, S. Resistive memory-based analog synapse: The pursuit for linear and symmetric weight update. *IEEE Nanotechnol. Mag.* 2018, 12, 36–44. [CrossRef]

39. Chai, Z.; Freitas, P.; Zhang, W.; Hatem, F.; Zhang, J.F.; Marsland, J.; Govoreanu, B.; Goux, L.; Kar, G.S. Impact of RTN on pattern recognition accuracy of RRAM-based synaptic neural network. *IEEE Electron Device Lett.* 2018, 39, 1652–1655. [CrossRef]

40. Ma, J.; Chai, Z.; Zhang, W.D.; Zhang, J.F.; Ji, Z.; Benbakhti, B.; Govoreanu, B.; Simoen, E.; Goux, L.; Belmonte, A. Investigation of pre-existing and generated defects in non-filamentary a-Si/TiO2 RRAM devices. *IEEE Access* 2020, 8, 192304–192311. [CrossRef]

41. Lee, Y.; Jo, H.; Kim, K.; Yoo, H.; Bae, H.; Lee, D.R.; Oh, H. IGZO synaptic thin-film transistors with embedded AlOx charge-trapping layers. *Appl. Phys. Express* 2022, 15, 061005. [CrossRef]

42. Abbas, H.; Ali, A.; Jung, J.; Hu, Q.; Park, M.R.; Lee, H.H.; Yoon, T.-S.; Kang, C.J. Reversible transition of volatile to non-volatile resistive switching and compliance current-dependent multistate switching in IGZO/MnO RRAM devices. *Appl. Phys. Lett.* 2019, 114, 093503. [CrossRef]

43. Zhu, L.; He, Y.; Chen, C.; Zhu, Y.; Shi, Y.; Wan, Q. Synergistic modulation of synaptic plasticity in IGZO-based photoelectric neuromorphic TFIs. *IEEE Trans. Electron Devices* 2020, 67, 1659–1663. [CrossRef]

44. Jang, J.T.; Ahn, G.; Choi, S.-J.; Kim, D.M.; Kim, H.; Kim, D.H. Digital and analog switching characteristics of InGaZnO memristor depending on top electrode material for neuromorphic system. *IEEE Access* 2020, 8, 192304–192311. [CrossRef]

45. Margaryan, D.; Doroshkevich, L.; Furuta, M.; Murakami, M.; Tseng, T.Y.; Kato, M. High performance hydrogenated In–Ga–Zn–O flexible Schottky diodes. *Appl. Mater. Interfaces* 2022, 12, 47739–47746. [CrossRef]

46. Feigerle, C.S.; Corderman, R.R.; Bobashev, S.V.; Lineberger, W.C. Binding energies and structure of transition metal negative ions. *J. Chem. Phys.* 1981, 74, 1580–1598. [CrossRef]

47. Kim, D.; Lee, H.J.; Yang, T.J.; Choi, W.S.; Kim, C.; Choi, S.-J.; Bae, J.H.; Kim, D.M.; Kim, S.; Kim, D.H. Effect of post-annealing on barrier modulations in Pd/IGZO/SiO2/p+–Si memristors. *Nanomaterials* 2022, 12, 3582. [CrossRef]

48. Hu, R.; Li, X.; Tang, J.; Li, Y.; Zheng, X.; Gao, B.; Qian, H.; Wu, H. Investigation of resistive switching mechanisms in Ti/TiOx/Pd-based RRAM devices. *Adv. Electron. Mater.* 2022, 8, 2100827. [CrossRef]

49. Choi, W.S.; Kim, D.; Yang, T.J.; Choe, I.; Kim, C.; Kim, H.; Kim, D.H. Electrode-dependent electrical switching characteristics of InGaZnO memristor. *Chaos Solitons Fractals* 2022, 158, 112106. [CrossRef]
52. Puglisi, F.M.; Larcher, L.; Padovani, A.; Pavan, P. A complete statistical investigation of RTN in HfO$_2$-based RRAM in high resistive state. *IEEE Trans. Electron Devices* **2015**, *62*, 2606–2613. [CrossRef]

53. Park, J.; Kim, T.-H.; Kim, S.; Lee, G.H.; Nili, H.; Kim, H. Conduction mechanism effect on physical unclonable function using Al$_2$O$_3$/TiO$_x$ memristors. *Chaos Solitons Fractals* **2021**, *152*, 111388. [CrossRef]

54. Barone, C.; Pagano, S. What Can Electric noise spectroscopy tell us on the physics of perovskites? *Coatings* **2021**, *11*, 96. [CrossRef]