Modeling the temperature distribution of multi-chip integrated circuits combining Wire-Bond and Flip-Chip technologies

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Abstract. On the basis of finite-element computer modeling, the temperature distribution of a multi-chip integrated circuit was calculated in System on Package configuration, combining Wire-Bond and Flip-Chip technologies. Technical recommendations are suggested for choosing a compound, taking into account the continuous layer of the compound separating the active elements and the heat sink.

1. Introduction
One of the most important factors affecting the reliability of equipment during prolonged and constant operation is to ensure its thermal conditions [1]. The problem of heat removal from the most heat-loaded elements is especially relevant in modern semiconductor and hybrid integrated circuits [2], where a reduction in topological dimensions and improved characteristics of microcircuit dies can be leveled due to non-optimal solutions for the formation of contacts, the placement of elements in the case [3, 4], as well as the choice of compound at the stage of encapsulation the IC [5].

Currently, one of the main systems of the electronic component base is System on Package (SiP) [6]. When developing SiP, the main focus is not on increasing the number of transistors used, but on the number of different functions that can be integrated in one device in the most reliable and cheap way. SiP dies are placed on one level (2D integration) or one above the other (3D integration), complemented with passive or other necessary components. Thus, integrated modules are formed in one case, which ensure the full functioning of the final electronic device.

An additional aspect in the development of SiP is that for chips with a large number of contacts, such as processors, Flip-Chip mounting technology is used, while others, such as memory, continue to use direct mounting on a substrate using Wire-Bond technology. In such hybrid SiP [7], the processor is mounted upside down on the board with the active side down (Flip-Chip), fixed on it with ball contacts, after which the remaining voids between the board and the microcircuit are filled with glue (underfill). It is advisable to place flash memory dies on the substrate with the active side up (direct die placement), and place the contacts behind the die and connect the die and substrate pads by Wire-Bond welding [8].

During the operation of such a hybrid system in the case, individual active modules are heated differently, especially in the case of a large number of contacts, because, despite their overall small area, the thermal conductivity is maximum compared to other materials (silicon and textolite). This
raises the problem of the optimal placement of dies on the board, and also requires solving the problem of choosing a compound and its filling, which is most often used as epoxy molding mixtures [9, 10]. If there are no high-precision circuits in the developed block, the electric strength of the compound fades into the background. The most important parameters for the task are low coefficient of specific expansion, low shrinkage during polymerization (so as not to damage the tracks when filling the board) and a high coefficient of thermal conductivity.

In this paper, technical recommendations based on the finite-element computer simulation of the temperature distribution of the integrated circuit are suggested for choosing a compound and its filling, taking into account the hybrid 2D technology for packaging the microcircuit: Flip-Chip and Wire-Bond, and using a powerful heat-generating element (processor).

2. Materials and Methods

Figure 1 shows the developed three-dimensional model of the IC device layout, consisting of elements of a heat generation source - a processor (CPU), two DDR3L memory dies (Die 1, 2), NAND flash memory (Die 3), and two NOR flash dies (Die 4, 5) placed on a printed circuit board. The processor, which has 3,000 ball pins, is mounted on Flip-Chip technology, all memory dies are connected by means of wire welding using Wire-Bond technology. To improve heat transfer with the environment and lower the temperature of the dies, a copper radiator with a surface area of 64 cm² mounted on the surface of the compound is used. For the calculation, the developed project of the SiP microcircuit on a substrate having 16 conductive layers separated by a dielectric is used.

As can be seen from figure 1, the processor, as the most dimensional heat-dissipation element, stands above the memory dies, and therefore has a smaller thickness of the compound layer above these dies. This imposes certain restrictions, both on the process of filling the compound and on the heat removal in the mode of operation of the IC from heat-loaded elements. The fact is that the pouring of the hot compound mixture always starts on one side of the IC and goes evenly to the opposite side, completely covering the entire chip. According to the technological regulations, grinding (thinning) of the compound after its hardening is not provided, due to the non-technological nature of this operation and the undesirable loss of the overall mechanical strength and encapsulation of the microcircuit. Thus, some layer of compound h (figure 1b), should always remain above the processor affecting the heat sink in view of its low thermal conductivity (compared with the silicon substrate of the processor and copper radiator), the thickness of which can be varied by the height of the molds for filling mold compound.
Table 1. Parameters of materials and IC heat-dissipation elements.

| Dies       | Mounting technology | Material | Heat dissipation power (W) | Die size (mm)         |
|------------|---------------------|----------|----------------------------|-----------------------|
| CPU        | Flip-Chip           | Silicon  | 7.0000                     | 12.600x8.000x0.800    |
| Die 1, 2   | Wire-Bond           | Silicon  | 0.3500                     | 7.800x9.200x0.200     |
| Die 3      | Wire-Bond           | Silicon  | 0.0132                     | 2.925x3.025x0.200     |
| Die 4, 5   | Wire-Bond           | Silicon  | 0.0825                     | 7.300x9.750x0.200     |

Modeling based on the heat equation and the conditions for matching heat fluxes at the boundaries of the regions was performed by the finite-element method in the Cadence Sigrity software package. Table 1 details the materials used for their thermal properties, as well as the characteristics of the heat-dissipation elements. The required parameters of the problem were the maximum temperatures in the processor and memory dies, depending on the thermal conductivity of the compound and the thickness of its layer above the processor.

3. Results and discussion.

As a result of simulation, it was found that the processor, as the most powerful heat-generating element, has the highest temperature, as might be expected, in any calculations (see table 1). The initial condition for the problem under consideration was the presence of a processor with large heat dissipation, with a power of 7 W (table 1).

Figure 2a shows how the temperature of the processor and other dies of the chip assembly changes with an increase in the thermal conductivity coefficient, thus, it is possible to select the thermal conductivity value sufficient for the considered structure to effectively reduce the temperature of the processor. At the same time, it is worth noting that the temperature of the processor depends on the thickness of the compound separating it from the radiator, the higher the thickness of the compound layer, the stronger the temperatures depend on its thermal conductivity. For the minimum temperature of the processor, the best option would be the absence of a compound layer (h = 0), but it should be excluded for the above technological reasons. Figure 2b shows graphs of the rate of change of the temperature of the processor depending on the thermal conductivity of the compound and the dependence of this temperature on the thickness of the compound layer above the processor.

On the one hand, figure 2b does not show a significant change in the temperature of the processor at various thicknesses of the compound, however, in more detailed consideration, it can be stated that the maximum temperature of the processor shows a significant decrease for thicknesses less than 300 μm. Thus, there exists an optimal range of compound parameters (thermal conductivity coefficient and its layer thickness above the processor), which determines the required die temperature regime in SiP.
The choice of compound is also determined by the filling technology and its price. Exceeding the compound layer over the processor of more than 500 μm is impractical because of its additional consumption, which means the cost per IC with excessive strength of the protective layer. A compound with a high coefficient of thermal conductivity has an increased cost, since for its synthesis it is necessary to use additives from heat-conducting materials [9]. In addition, a more thermally conductive compound transfers heat more efficiently when filling (in the form of a hot mixture) IC, that is, it hardens faster, which can also create certain problems in this process.

In our view, the best option for choosing a compound is the one in which the maximum processor temperature does not reach 85°C (for using ICs in nonventilated environment). In this case, the compound can have a thermal conductivity coefficient in the range 0.4–0.7 W/(m·K), for example, a widespread compound with $\lambda \sim 0.6$ W/(m·K), with the protection of a relatively thin layer above the processor of the order of 100–200 μm. In the field of these parameters (figure 2b), the temperature change from thermal conductivity drops sharply, which gives additional advantages in the variability of the compound parameters when it is selected.

4. Conclusion
In this work, the temperature distribution of a multi-chip integrated circuit was calculated using the Cadence Sigrity software package. The integrated circuit consisted of a processor, DDR3L memory dies, NAND and NOR flash dies, each of these elements being a heat source. The processor was mounted using Flip-Chip technology, and all the memory dies were connected using Wire-Bond technology. To improve heat transfer with the environment, a copper radiator was installed on the microcircuit. During the simulation, the thickness of the compound layer $h$ in the range 50–1000 μm and the thermal conductivity coefficient of the compound $\lambda$ in the range 0.1–1 W/(m·K) were changed. It was found that, taking into account the technological limitations of the production of an integrated circuit, there is an optimal combination of the values of these parameters. With a compound thickness $h$ in the range 100–200 μm and a thermal conductivity coefficient $\lambda$ in the range 0.4–0.7 W/(m·K), the maximum temperature of the processor (the most heat-generating element of the integrated circuit) did not exceed 85°C. In conclusion, it should be noted that the presented results can be useful for the technical regulation of the process of filling the compound not only of this IC, but also for other microcircuits created by the technology of 2D packaging the System in Case.
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