Test Platform of LTE-U Communication System Based on FPGA

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Abstract. In order to solve the problem that the LTE communication system cannot be easily deployed, we design a test platform of LTE-U communication system based on FPGA. The test platform includes mobile terminals, base stations and base station networking system. It supports 5G unauthorized frequency band, WIFI and 100M network. A single base station can support up to 8 terminals with a distance of 1 km. It uses an omnidirectional antenna to communicate with the terminal and uses a gigabit ring network between base stations. In the process of mobile communication, we use RSSI (received signal strength indication) and bit error rate as the evaluation criteria and test the 32 terminals covered by the chain network and 4 base stations. The test platform can complete the LTE-U test well.

1. Introduction
LTE (long term evolution) communication system has the characteristics of wide coverage (300 ~ 500m), high uplink and downlink rate, etc. In some applications, LTE can even replace WIFI (wireless fidelity). However, the biggest problem of LTE is that it must use the authorized frequency band [1]. Considering that spectrum resources are extremely scarce, which is one of the strategic management projects of a country, it is not affordable by some individual organizations. Therefore, how to use the same language protocol and obtain commercial value in the civil field has become the research topic of many scholars and enterprises. As a result, LTE-U (long term evolution in unlicensed spectrum) communication technology based on unauthorized channels was first formally proposed in 2013. In 2014, Verizon, together with Alcatel lucent, Ericsson, Qualcomm and Samsung, established the LTE-U forum to jointly develop technical documents that relate to R12 (release 12) protocol based on 3GPP (3rd generation partnership project). In 2015, Ericsson and Qualcomm jointly demonstrated LTE-U technology. The two sides aggregate a 20MHz licensed frequency band unit and a 20MHz band unit on 5GHz unauthorized frequency, and achieve a 300Mbps download peak on the airport. Therefore, if the mature LTE-U communication system can be deployed in ISM (industrial, scientific, medical) and other unauthorized frequency bands, it will bring great value. Therefore, in order to solve the problem that the LTE communication system cannot be simply deployed, considering that LTE can be better used in unlicensed frequency bands, we design and implement a test platform of LTE-U communication system based on FPGA (field programmable gate array), and successfully realize the design and deployment of LTE-U communication system. It has the characteristics of simple system, simple deployment and repeated experiment optimization.
The rest of the paper is organized as follows. In Section 1, we describe the system structure and hardware design. The system’s FPGA design includes overall design, time slot controller, modulator and demodulator is presented in Section 2. The system instruction design is presented in Section 3. The system physical test is presented in Section 4. Finally, we conclude the paper and describe the future work in Section 5.

2. System Structure and Hardware Design
As shown in figure 1, the system is mainly composed of base station, mobile terminal, data center and optical fiber ring network. A wireless access device sets every 1 km along with the optical fiber. The base station connects with the data center through a 1.25 GHz synchronous ring network formed by optical fiber. Each base station conducts broadband communication with multiple mobile terminals at the same time. The mobile terminal switches between the coverage areas of the base station equipment during the mobile process. The communication between the mobile terminal and base station adopts 5.8 GHz frequency band. The uplink (from terminal to the base station) rate and downlink (from base station to terminal) rate adopt asymmetric mode. The uplink rate is low and the downlink rate is high, and the uplink and downlink rate ratio can be configured. The maximum number of terminals that a base station can access at the same time is \(N\), where \(N\) can be configured as 32, 64, 128, etc. The communication rate with each terminal can be automatically adjusted according to the number of terminals connected at the same time.

![Figure 1. System structure.](image)

2.1. Design Scheme of Mobile Terminal and Base Station Multiplexing
As shown in figure 2, the base station adopts single-mode and dual fiber, and uses Intel FPGA to realize forwarding, filtering, coding and baseband processing of network packets [1]. Then it uses AD9364 to achieve zero intermediate modulation and uses an omnidirectional antenna to send signal. At the same time, it uses the antenna of another port to receive the terminal’s signal that is processed by AD9364 and sent back to FPGA for receiving and demodulation. Finally, it sends the signal to the network port and back to the data center. For the mobile terminal, the only difference is that the SFP port is not enabled. Of course, the actual application scenario is also required. If the terminal needs to upload some third-party data sources, the optical port and WIFI can access other data. The hardware
design can realize TDD (time division duplex) and FDD (frequency division duplex) deployment. It uses the 5.8 GHz unauthorized frequency band for communication. The base station has three antennas, two of which are RX (receive) and TX (transmit), and the third antenna is GPS (global positioning system) antenna, which is used for timing synchronization of multiple base stations to ensure that the communication windows will not conflict. The mobile terminal has an optional WIFI antenna, but due to the conflict between WIFI and LTE on the same frequency band [2,3], the WIFI frequency band is temporarily selected on 2.4 GHz.

2.2. Design Scheme of Ring Network Topology
As shown in figure 3, the base station supports ring network access with dual optical fiber ports. The maximum access number to the base station is 255. The IP (internet protocol) address of the base station is the IP address of the CPU. In the design of multi-base station networking, it is necessary to pay attention to different frequency networking. As shown in figure 3 and figure 4, the available frequencies are 4.9 GHz ~ 5.9 GHz. The 1GHz frequency band is divided into eight bands. Each frequency band occupies 125MHz bandwidth, and each frequency band contains 8 channels with 51 MHz bandwidth. For a base station, when the frequency band of the using frequency point is selected, it has eight channels to avoid frequency interference from other signals.

3. FPGA Design of the System
The hardware design of the system mainly includes mobile terminal and base station. In fact, in order to save design cost and reuse platform, unified hardware platform and uniform code design are adopted for data receiving and sending algorithms.

Figure 3. Structure of terminal and base station.  Figure 4. Different frequency networking.

3.1. Overall Design
As shown in figure 5, the register table mainly communicates with the CPU (central processing unit). CPU controls some modes triggering and state reading. Because the scheduling information of each slot is inconsistent, such as the number of UE (user equipment) and the RE (resource element) used, the most important is the real-time dynamic configuration which can be realized through this interface. The event processing module mainly collects some information during FPGA operation, especially when HARQ (hybrid automatic repeat request), ACK (acknowledge character) and other information are collected, the event should report to upper software. MAC (media access control) is to send and receive packets from the network. The time slot controller is responsible for base station synchronization to ensure start sending and receiving data at the same time. Adjusting demodulator is
the most complex part in the FPGA implementation. It mainly realizes IFFT (inverse fast fourier transform) / FTT (fast fourier transform) transform, constellation mapping, filtering, etc.

3.2. Design of Time Slot Controller
As shown in figure 6, CPU manages sending data area at the beginning of the system. CPU uses DMA (direct memory access) to import user data from IP switching module (or WIFI module) into the cache (double data rate, DDR), and then hands over management rights to the hardware. After receiving management right, the hardware will code and interleave the data from cache according to command, then code the data by LDPC (low density parity check code) [4], and finally write into corresponding sending data area (first in first out, FIFO) as required. At the same time, CPU writes the instruction of how to process data in sending data area into a dynamic configuration register. Then it sends the data to a digital modulator according to configuration instruction. When completing data reading in the data area, the CPU hands the management right of the data area over to CPU. At the same time, an interrupt request will be sent to CPU to start DMA to fill data in the sending data area.

Figure 7. Design of receiving slot control.

The data flow of the receiver is shown in figure 7. First, CPU is responsible for writing the instruction of how to receive data into receiving command area. The receiving slot controller reads the command and receives the data from the demodulator according to the corresponding instruction. Then LDPC decodes and deinterleaves the data [5,6]. Next it RS (reed-solomon) decodes, and detects CRC (cyclical redundancy check) error, then writes the processed data into DDR cache. When a certain amount of data is stored in the receiving data area, the receiving slot controller will send an interrupt request to the CPU so that the CPU can set DMA to read the data. At the same time, the system uses the GPS signal to control the synchronization of multi-base stations. As shown in figure 8, all base stations start sending PN (pseudo-noise) heads at 0ms.

3.3. Modulator Design

The basic structure of the digital modulator is shown in figure 9. QPSK (quaternary Phase Shift Keying), 16QAM (16 quadrature amplitude modulation), 64QAM (64 quadrature amplitude modulation) modulation are applied to the input data with constellation mapping module. Bandwidth control module is that whether inserts pilot subcarrier according to the setting of effective subcarrier number register in sending instruction. Differential coding module uses a differential encoder of differential OFDM (orthogonal frequency division multiplexing) system to be more suitable for
mobile communication scenarios in a simple model. IFFT module realizes inverse fast Fourier transform, and directly uses Intel IP to convert frequency domain signal to the time domain to form OFDM symbol. Cyclic prefix insertion module copies the number of sampling points with a size of 32 / 64 in the back of the OFDM symbol according to the size of the register configuration window. PN insertion module is a synchronization head’s generation circuit of mobile terminal and base station that can generate multiple synchronization heads by configuration. Gain control module can adjust gain according to the feedback of the transmitting signal.

3.4. Demodulator Design

The basic structure of the digital demodulator is shown in figure 10. Gain control module adjusts the received signal to a specific amplitude. PN correlator module starts to search synchronization header after receiving a command. The circuit can provide time offset information of the system and send clock information to AD9364 as a new reference clock to receive data. Cyclic prefix removal module constructs the fixed length of FFT transform according to timing protocol, and deletes CP (cyclic prefix) header, then eliminates the multipath effect. FFT module is a fast Fourier transform. It converts OFDM signal from time domain to frequency domain. The differential decoder module is a decoder of differential OFDM system. The pilot phase difference module calculates the phase difference between the second pilot signal received and the pilot signal in the local cache, and submit the operation results to the post-processing module. Post processing module extracts and corrects frequency offset information according to the phase difference of the data before and after the decision. Constellation mapping module adjusts the last data by constellation mapping and eliminates pilot subcarriers inserted at the transmitter [7].

4. System Instruction Design

As shown in figure 11, the system instruction is

| TIME(32)          | RS(4) | CRC(1) | PN(2) | CAR(10) | OFDM_NUM(10) | QAM(2) | Reserve(3) |
|-------------------|-------|--------|-------|---------|--------------|--------|------------|
| OFDM_SIZE(2)      | CP(2) | Reserve(28) |

Figure 11. Format of send/ receive command.

Where, the definitions of symbols are as follows in table 1.
Table 1. Detailed description of instruction type.

| Category  | Bit width | Description                                                                 |
|-----------|-----------|-----------------------------------------------------------------------------|
| TIME      | 32        | It is the counter value of the processing clock. The lower 21 bits are intra-frame counters, and the upper 9 bits is frame counters. |
| RS        | 4         | Word group number of RS code                                                 |
| CRC       | 1         | Whether the receiving end needs CRC check                                    |
| PN        | 2         | 4 kinds of PN head                                                          |
| CAR       | 10        | Number of effective subcarriers in OFDM                                      |
| OFDM_NUM  | 10        | Number of OFDM symbols                                                      |
| QAM       | 2         | QPSK/16QAM/64QAM modulation indication                                       |
| OFDM_SIZE | 2         | 128/256/512/1024 FFT points                                                 |
| CP        | 2         | Window size of cyclic prefix                                                 |

5. System Physical Test

5.1. System Test Environment

As shown in figure 12, in the test environment above, the first line of equipment includes 1 base station with a weak signal, PN synchronization head and pilot and 2 interference base stations with a single tone signal. The second line includes 1 test base station and 2 test terminals. The third line includes 2 computers.

5.2. Test Base Station Registration

As shown in figure 13, there are 2 interference sources and weak base station signals. In this case, after base station power on, it performs frequency scanning automatically to obtain the following spectrum.

As shown in figure 14, through automatic scanning and registration of the base station, the base station is successfully allocated to the 5.81 GHz frequency band in the experiment environment. It occupies 50M bandwidth, and successfully avoids 3 preset interference sources.
5.3. Test Terminal Registration
As shown in figure 15, in the case of keeping the above environment unchanged, we reduce the signal strength of 2 interference sources, and turn on the terminal. As shown in figure 16, in this case, terminal 1 successfully selects the frequency point of 5.811G, registers successfully, and the network Ping packet is normal. As shown in figure 16, in this case, terminal 1 successfully selects the frequency point of 5.811 GHz, registers successfully, and the network Ping packet is normal. As shown in figure 17, after terminal 2 successfully registers, the upstream channel is divided equally.

Figure 16. Time domain diagram of terminal 1.

Figure 17. Time domain diagram of terminal 2.

6. Conclusion
We design a test platform of LTE-U communication system based on FPGA for the current LTE-U system’s inability to be easily deployed, and successfully realized automatic backoff registration of 5GHz unauthorized band base station, registration of terminal, network communication between the base station and terminal in the laboratory environment. The design of this test platform has certain research and application value. Because FPGA is reprogrammable, we will continue to study how to implement a 3GPP physical layer protocol on FPGA.

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