ReGraph: Scaling Graph Processing on HBM-enabled FPGAs with Heterogeneous Pipelines

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Abstract—The use of FPGAs for efficient graph processing has attracted significant interest. Recent memory subsystem upgrades including the introduction of HBM in FPGAs promise to further alleviate memory bottlenecks. However, modern multi-channel HBM requires much more processing pipelines to fully utilize its bandwidth potential. Existing designs do not scale well, resulting in underutilization of the HBM facilities even when all other resources are fully consumed.

In this paper, we re-examine the graph processing workloads and find much diversity in processing. We also found that the diverse workloads can be easily classified into two types, namely dense and sparse partitions. This motivates us to propose a resource-efficient heterogeneous pipeline architecture. Our heterogeneous architecture comprises of two types of pipelines: Little pipelines to process dense partitions with good locality and Big pipelines to process sparse partitions with extremely poor locality. Unlike traditional monolithic pipeline designs, the heterogeneous pipelines are tailored for more specific memory access patterns, and hence are more lightweight, allowing the architecture to scale up more effectively with limited resources.

Furthermore, we develop an automated open-source framework, called ReGraph¹, which automates the entire development process. ReGraph outperforms state-of-the-art FPGA accelerators by up to 5.9× in terms of performance and 12× in terms of resource efficiency.

I. INTRODUCTION

Graphs are de facto data structures to represent the relationships between entities in many application domains such as social networks, genomics, and machine learning [13], [24]. As a result, efficient graph processing is becoming increasingly important, especially as the amount of graph data grows [35]. Allowing efficient customization on the hardware logic to computation/memory access patterns, FPGA usually delivers better memory efficiency and energy efficiency than CPUs/GPUs [1], [3], [4], [9], [29], [36], [50]–[52]. Furthermore, high-level synthesis (HLS) that translates kernels written in high-level languages to low-level RTL modules alleviates the poor programmability issue of FPGAs, providing high usability to efficient graph processing systems [4], [14], [28].

While graph processing is data access intensive, recent High Bandwidth Memory (HBM) enabled-FPGAs bring tremendous performance potentials. Graph processing explores the irregular structure of a graph rather than performing large numbers of computations, resulting in poor data locality and high communication to computation ratio [25], [53]. Memory bandwidth is therefore the major bottleneck to the system performance. Recent FPGAs have started integrating HBM to meet the demand for the ever-increasing memory bandwidth of data center applications [6], [19]. For example, Alveo U280 [46] equipped with 32 HBM channels can deliver up to 460 GB/s of peak memory bandwidth, which is a sixfold increase over the latest FPGA platform with four DRAM channels (Alveo U250 [45]). The largely increased bandwidth from more memory channels offers to satiate much more graph processing pipelines [4], [51], hence boosting performance.

It turns out that the effective utilization of HBM requires significant logic resources. Table I presents the estimated resource utilization of existing designs on U280 [46], the largest HBM-enabled FPGA on the market, where we obtain the resource usage from corresponding papers and proportionally project them with the number of utilized memory channels. All designs greatly exceed the resource capacity even when only 8 of the 32 memory channels are used. This underutilization of the HBM implies that performance can be scaled further if we find a way to use the logic resources more efficiently.

The key contribution of our work is in finding the opportunity to be more resource-efficient by taking into account the diversity of workloads in graph processing. While graph partitioning is a widely employed technique for improving memory efficiency and extracting data-level parallelism [1], [3], [4], [9], [29], [36], [50]–[52], partitions are inevitably unbalanced due to the irregular graph structure [21], [34], [40]. As a result, different partitions can have quite different requirements. For example, in a pull-based execution model, every vertex reads vertex properties from its neighbors. A partition containing more vertices with high in-degrees tends to have more memory accesses to the vertex property array, hence a better data locality. Previous research used monolithic pipelines that employ elaborate techniques to provide high performance for a wide variety of graph partitions [1], [4], [51]. However, this can lead to over-provisioned pipeline

¹ReGraph is open-sourced at https://anonymous.4open.science/r/ReGraph/.

table I: Estimation of resource utilization of existing designs with increasing the number of memory channels (#CH).

| Existing Designs | Resource Type | 1 CH (14 GB/s) | 4 CH (58 GB/s) | 8 CH (115 GB/s) | 16 CH (230 GB/s) | 32 CH (460 GB/s) |
|------------------|---------------|----------------|----------------|----------------|-----------------|-----------------|
| HiGraph [51]     | LUT           | +16.9%         | +68.1%         | +36.2%         | +272.4%         | +544.8%         |
| FabGraph [36]    | LUT           | +25.5%         | +102.1%        | +204.2%        | +408.5%         | +817.0%         |
| ISCA'21 [4]      | LUT           | +18.6%         | +74.2%         | +148.4%        | +296.8%         | +593.6%         |
| ThunderGP [4]    | CLB           | +21.3%         | +85.3%         | +170.6%        | +341.2%         | +682.4%         |

*Numbers are obtained from corresponding papers and normalized to U280 while others are proportionally scaled with the number of memory channels.
*Note the maximal LUT usage in practice is less than 80%.
designs and underutilization of hardware resources. Partitions with poor locality require a different memory access technique that is not necessary for partitions with good locality. This leads to the key idea of our proposal: heterogeneous pipelines.

While heterogeneity has been widely adopted in multi-core architectures [20], [26], [41], realizing heterogeneous pipelines to accelerate graph processing on FPGA is nontrivial. First, due to the irregularity of graphs, there exists significant workload diversity within graph processing, which in turn leads to a large design space of pipeline types. Second, the pipelines must be efficiently tailored to the challenging irregular memory access patterns of graph processing while being resource-efficient. Third, the computational pattern of graph processing is data-dependent, which makes scheduling tasks for the heterogeneous pipelines even more challenging. In this paper, we tackle the above-mentioned challenges and propose a heterogeneous pipeline architecture for graph processing that efficiently adapts to workload diversity.

In particular, we make the following contributions.

- We classify graph partitions to dense and sparse partitions by grouping vertices based on their degrees; The dense partitions have high-degree vertices, with good locality, and the sparse partitions have low-degree vertices, with low locality. Then, on the basis of the workload characteristics, we customize two types of pipelines: Little and Big pipelines.

- We propose a model-guided task scheduling method that maps partitions to suitable pipeline types based on the proposed performance model, determines the most efficient pipeline combination, and balances the workloads of pipelines.

- To ease the entire process, we develop an open-sourced end-to-end framework – ReGraph, which generates efficient deployable graph accelerators with user-defined functions and schedules graphs in a push-button manner.

The comprehensive evaluation shows ReGraph delivers $1.6 \times -5.9 \times$ performance speedup and $12 \times$ resource efficiency improvement over state-of-the-arts. ReGraph is $1.5 \times -9.7 \times$ faster than the state-of-the-art CPU solution and $2.5 \times -9.2 \times$ more energy efficient than GPUs.

II. Maximizing Performance Per Resource with Heterogeneous Pipelines

By efficiently adapting to the diversity of applications, heterogeneous multi-core architectures (HMAs) deliver greater throughput for a given silicon area [20], [26], [41]. While HMA has been effective for multi-core architecture, we need to revisit the challenges and opportunities of heterogeneous design for graph processing on FPGAs. In this section, we study the workload diversity in graph processing and explore lightweight heterogeneous pipelines with maximized performance per resource. In particular, we characterize the diversity of workloads in graph processing, classify the workloads into two different categories, and specialize two types of pipelines to these workload characteristics for higher resource efficiency.

A. Workload Classification: Dense vs. Sparse

Graphs can be processed in a vertex-centric or edge-centric manner, with the latter being the more popular of the two [1], [3], [4], [9], [36], [50]–[52]. In edge-centric processing, edges are accessed sequentially with high memory efficiency. To access vertices efficiently, the vertices of large graphs are usually partitioned to fit into the limited on-chip RAMs to avoid random memory accesses. Most state-of-the-art designs [1], [4] opted to buffer destination vertices and employ customized memory access techniques to access source vertices from the global memory, as buffering both results in a large amount of redundant data transfers. Figure 1 illustrates the graph partitioning method of ThunderGP [4]. The input is a directed graph in standard coordinate list (COO) format with the row indices (source vertices) in ascending order [4], [51]. Suppose a graph has $V$ vertices ($V=6$ in the example) and the size of vertex set of a partition is $U$ ($U=3$ in the example). $[V/U]$ partitions will be generated with the vertex set of the $i^{th}$ partition ranging from $(i-1) \times U$ to $i \times U$. Partitions also maintain edge lists that contain all edges whose destination vertices belong to the vertex set. In this paper, we adopt this graph partitioning method.

Graph partitions are naturally imbalanced because most graphs are naturally irregular [2], [21], [40]. Power-law graphs usually have a few high degree vertices (hot vertices) that are involved in lots of connections [12], [25]. Therefore, the distribution of these vertices influences the workloads of partitions significantly. Figure 2 shows workload characteristics of graph partitions from four representative datasets (see Table III). Note that the y-axis of the figure is on a logarithmic scale. For each partition, we profile the percentage of edges and the percentage of source vertices accessed. The figure suggests large workload diversity in the graph partitions.

Although graph workloads are diverse, we note that they can be easily divided into two categories, namely one with high-degree vertices and the other with low-degree vertices. This can be achieved using the lightweight degree-based grouping (DBG) [12] technique, which is widely used to balance partitions and improve cache efficiency [1], [5], [12]. The colored markers in Figure 2 depict partition workload characteristics with the partitions sorted in the descending order of in-degree after applying DBG. Partitions without any edges are not included. We see that we can categorize them into two major kinds of partitions: 1) dense partitions are partitions that have a large number of edges and access a
large portion of source vertices. It happened to be the first few partitions as they contain all high degree vertices. For example, the first partition of HD covers up to 72% of edges and accesses 80% of source vertices; 2) sparse partitions are partitions that have a few edges and only access a small portion of source vertices. The remaining partitions are sparse as they only have low degree vertices. For instance, the majority of G23 partitions have only fewer than 1% of edges and access less than 10% of source vertices. The exact classification of the partitions is determined during the task scheduling stage according to the performance models of two types of pipelines (see Section IV).

B. Rationales for Heterogeneous Pipeline Customization

We aim at addressing the scalability issue of HBM-enabled FPGAs. The ability to easily classify the diverse workloads motivates us to propose two types of heterogeneous pipelines - one for dense and the other for sparse partitions.

Big pipelines are designed to handle sparse partitions. Firstly, due to the extremely poor data locality of sparse partitions, memory access techniques such as caching, prefetching [4] and the cache miss optimized memory system [1] do not work efficiently. Therefore, Big pipelines opt to tolerate the latency of inevitable memory requests instead of equipping with resource-intensive memory access techniques. Secondly, because sparse partitions have a few edges but are of a large number, partition switching overhead introduced by emptying the pipeline and enqueuing tasks are non-negligible compared to its short execution time [4]. This severely diminishes speedup from multiple pipelines. To mitigate the overhead, we adopt the data routing technique [3], [4] to let Big pipelines process multiple partitions per execution.

Little pipelines are designed to process dense partitions. On the one hand, benefiting from good spatial locality from a large amount of source vertex accesses, Little pipelines read source vertices in a burst manner without concerning redundant memory accesses argued in existing works [1], [4]. Therefore, without using resource-intensive memory access techniques [1], [4], Little pipelines only adopt a lightweight ping-pong buffer to overlap the source vertex access and edge process. On the other hand, since the number of dense partitions is small, and they have a long execution time, the overhead of partition switching is negligible. Therefore, we do not adopt the data routing technique to Little pipelines.

As our pipelines are designed for heterogeneous workloads, they omit underutilized hardware logic in existing pipelines and therefore provide higher performance with more efficient resource utilization. This enables us to scale the graph processing system on HBM-enabled platforms by instantiating more high-performance pipeline instances.

III. SYSTEM ARCHITECTURE

To support various graph algorithms, our system adopts the popular Gather-Apply-Scatter (GAS) model, which contains three stages for each iteration: the Scatter, the Gather, and the Apply [1], [3], [4], [9], [29], [36], [50]–[52]. In this section, we present the proposed heterogeneous pipeline architecture for resource-efficient graph processing.

A. Architecture Overview

Figure 3a shows the overview of the proposed architecture. It is composed of a Little pipeline cluster with $M$ Little pipelines, a Big pipeline cluster with $N$ Big pipelines, the Little and Big mergers, the Apply and the Writer modules.

Little and Big pipelines connect to disjoint memory channels and perform the Scatter and the Gather stages for dense partitions and sparse partitions, respectively. Both of them manipulate $N_{spe}$ Scatter PEs and $N_{gpe}$ Gather PEs to process multiple edges per cycle and consume the full bandwidth of a memory channel. Figure 4 shows the data layout in a HBM channel and a running example. The input is a set of edges composed of source vertex ID, destination vertex ID and weights (optional). The Scatter stage calculates update values for destination vertices by processing the source vertex properties (retrieved from the global memory by dereferencing source vertex ID). The Gather stage accumulates update values for destination vertices whose temporary properties are buffered in local buffers and writes out the accumulated values after all edges of the current task are processed. The Big and Little mergers combine the intermediate results in buffers of the Big and Little pipelines, respectively.

The Apply module receives accumulated temporary results from the Big and Little pipeline clusters simultaneously, as shown in Figure 3c. Together with vertex properties from HBM channels, it calculates new vertex properties with multiple PEs. The new vertex properties are transferred to the Writer on a first-come-first-serve basis. The Writer finally writes new vertex properties to all memory channels for the next iteration. All accesses to the global memory are in granularity of a block (with 512-bit) for high memory efficiency.
**B. Big Pipeline Architecture**

Figure 3d depicts the architecture of the Big pipeline, which is composed of the Burst read module, the Vertex Loader, the Data Router, $N_{spe}$ Scatter PEs, and $N_{gpe}$ Gather PEs. Figure 4 shows a running example of PageRank on the pipeline. The Burst read module sequentially reads multiple edges and duplicates source vertices for the Vertex Loader. The Vertex Loader retrieves source vertex properties for Scatter PEs by tolerating memory access latency. The Data Router dynamically dispatches update tuples generated by Scatter PEs to Gather PEs that buffer the corresponding destination vertices. This allows Gather PEs to process and buffer distinct vertices; therefore, $N_{gpe}$ Gather PEs can handle $N_{gpe}$ partitions per execution (while Little pipelines only handle one), minimizing the number of partition switches. We adopt a multi-stage butterfly network in the Data Router for high resource efficiency [3], [6]. Next, we introduce details of the Vertex Loader.

Figure 5 shows the architecture and data flow of the Vertex Loader, assuming the Big pipeline processes four edges per cycle. The input is a set of source vertex IDs (four in the example) extracted from a set of edges. The output is a set of source vertex properties that Scatter PEs are requesting. As the IDs are in ascending order with the standard COO graph formats, we only cache the last request of the previous vertex ID set (assumed as one in Figure 5). The logic is split into two small pipelines: the Request sending pipeline that minimizes the number of issued memory requests to the global memory, and the Response processing pipeline that dispatches fetched source vertex properties to Scatter PEs in parallel. This allows execute/access decoupling as memory requests can be issued before processing.

As shown in the Figure 5, the data flow of the Vertex Loader is as follows. In Step ①, the Decoder module calculates block indices in the global memory and the offsets of vertices in the blocks in parallel. For example, if the vertex property is 32-bit in the memory, the indices equal to $\lfloor src \cdot 32/512 \rfloor$ and offsets equal to $src \cdot 32 \mod 512$. In Step ②, the Request sending pipeline compares indices with the last requested index (one in this example) and marks it as zero if matched, otherwise outputs the index. In Step ③, the memory Request generator extracts valid memory requests (non-zeros). As indices are
monotonically increased, it ascertains the positions of valid requests by counting the number of leading zeros. In the example, the index set has two zeros; thus, the Request generator reads the requests from the offset of two to the end. As a return, it saves two cycles compared to enumerating all indices. In Step 4, the Property reader fetches a vertex property block (512-bit as well) for each block index from the global memory, and writes it to the corresponding stream in a blocking manner based on its offset in the current index set. In the example, two property data blocks are written to the third stream and the fourth stream, respectively, as their offsets are three and four.

The Response processing pipeline responses source vertex properties for \(N_{\text{spe}}\) Scatter PEs in one cycle. In Step 5, it compares the block indices with the last request in parallel and reuses the last requested property block if they are matched, otherwise reads from the stream. In the example, it only reads the third and fourth streams as the first two indices are matched. In Step 6, the pipeline decodes out the vertex properties based on their offsets in the corresponding property blocks and sends them to Scatter PEs in parallel. Lastly, the last request index and its property block are updated with the last index of the current set and its properties, respectively.

C. Little Pipeline Architecture

Figure 3a shows the architecture of the Little pipeline, which contains the Burst read module, the Ping-Pong Buffer, the Merger, \(N_{\text{spe}}\) Scatter PEs, and \(N_{\text{spe}}\) Gather PEs. Figure 4 shows a running example of PageRank on the pipeline. The Burst read unit sequentially reads edges. The Ping-Pong Buffer accesses source vertex properties for Scatter PEs in a burst manner. Without dynamic data routing, the update tuples generated by Scatter PEs are statically dispatched to Gather PEs. As different Gather PEs process update tuples with the same destination vertices, they buffer the same destination vertices, as shown in Figure 4. As a consequence, the Merger accumulates their intermediate results once all edges of a partition are processed. Instead, Big pipelines do not require merger as PEs process distinctive vertices. Next, we introduce the detailed HLS-based design of it.

Ping-pong Buffer allows the pipeline to read vertex properties from one buffer and meanwhile fetch vertex properties from the global memory to the other buffer, hence improving effective memory bandwidth. Figure 6 shows the proposed Ping-Pong Buffer architecture. Same with the Vertex Loader in Big pipelines, inputs are source vertex IDs, and outputs are vertex properties. We allocate both ping and pong buffers for each Scatter PE for parallel processing. To enable 512-bit data access to a buffer, we cascade multiple BRAMs to construct a 512-bit memory port, e.g., eight BRAMs for Xilinx devices (72 bit \(\times 8\)), as shown in the bottom right of Figure 6. The logic for filling and reading buffers are realized in one loop with an initiation interval (II) [44] of one. The buffer write index and the buffer read index are used for synchronization, and they are initialized as zeros. The read index is calculated by dividing the vertex ID by the buffer size. The write index is determined by the read index as the buffers are written before read. Switching between two buffers is determined by the last bits of the write and read indices.

Buffer filling is executed only when the write index is behind the read index or not ahead by one (to avoid override of the other buffer). The Burst reader is responsible for writing successive data blocks to buffers and accessing the global memory in a burst manner. In each cycle, it requests one data block to buffers. Once the buffers (e.g., ping buffers) are full, it increases the buffer write index by one. This will switch buffering filling to other buffers in the next execution (e.g., pong buffers). On the other hand, the pipeline reads vertex property blocks for Scatter PEs when the read index is behind the write index, indicating that the properties are loaded into the buffers. Multiple property blocks can be returned per cycle with duplicated buffers. The Byte selector outputs the vertex properties based on block offsets in corresponding vertex property blocks. As vertex property access addresses are monolithic increased, the architecture also adopts a jump access mechanism that forces the write index to be the read index (not shown in the figure). This avoids redundant memory accesses when the Little pipeline processes only a portion of the partition.

IV. Graph-Aware Task Scheduling

While the effectiveness of heterogeneous architectures heavily depends on task scheduling, an accurate performance model that estimates the execution time of partitions on both types of pipelines is required for effective partition-to-pipeline mapping (i.e., identifying whether a given partition is dense or sparse) and workload balancing. In this section, we first introduce the performance model of two types of pipelines and then the model-guided task scheduling method.

A. Performance Modeling of Big-Little Pipelines

Unlike regular applications that have deterministic memory access and computation latency [7], irregular graph structure
makes performance modeling challenging. A simple regression model based on the numbers of edge and vertex is unable to model the processing performance accurately [4], because the bottleneck of the pipeline alternates between edge access and vertex access during execution. Instead, we propose a cycle-level performance model that accurately estimates the execution time of Big and Little pipelines of an application on graph partitions by enumerating edges. As performance estimation has only lightweight computation and is integrated to the graph partitioning phase to reduce edge enumeration overhead, it introduces little extra preprocessing overhead.

The estimated execution cycles $C_p$ of two types of pipelines on a partition $p$ is shown in Equation (1):

$$C_p = \sum_{i=0}^{E_p} \max(C_{acs,v}^i, C_{acs,e}^i, C_{proc}^i) + C_{store} + C_{const}$$  

where $i$ enumerates $E_p$ edges of a partition (happening with graph partitioning), $C_{acs,v}^i$ denotes cycles to access the source vertex of the edge, $C_{acs,e}^i$ denotes cycles of reading the edge, $C_{proc}^i$ represents cycles to process the data, $C_{store}^i$ denotes cycles to write out buffered destination vertices and $C_{const}$ is the constant overhead.

As edges are sequentially accessed, given the data size the memory channel can access in one cycle (i.e., the size of the data block), $S_{mem}$, and the size of an edge, $S_e$, $C_{acs,v}$ can be calculated as a constant value, $\frac{S_e}{S_{mem}}$. For $C_{const}$, we measure the execution time of dummy partitions with a few edges to estimate the constant overhead of partition switching.

Let $S_{ram}$ denote the data width of the port of the buffers in $N_{gpe}$ Gather PEs and let $S_{buf}$ denote the size of the buffer. $C_{store}$ is calculated by Equation (2). The buffers of Gather PEs in Little pipelines are merged; hence, the data size to write out is $N_{gpe}$ times smaller than that of the Big pipeline.

$$C_{store} = \begin{cases} \max\left(\frac{S_{buf}}{S_{ram}}, \frac{S_{buf} \cdot N_{gpe}}{S_{mem}}\right), & \text{if Big pipeline} \\
\max\left(\frac{S_{buf}}{S_{ram}}, \frac{S_{buf}}{S_{mem}}\right), & \text{if Little pipeline} 
\end{cases}$$  

Meanwhile, $C_{proc}$ is determined by numbers of Scatter PEs ($N_{spe}$). Gather PEs ($N_{gpe}$) and their IIs ($I_{spe}$ and $I_{gpe}$), as shown in Equation (3). The II indicates the number of cycles the PE could process one input and is determined by the compiler once the logic of PE is set.

$$\frac{1}{C_{proc}} = \max\left(\frac{N_{spe}}{I_{spe}}, \frac{N_{gpe}}{I_{gpe}}\right)$$  

Lastly, we model $C_{acs,v}^i$ based on the architecture of the Vertex Loader and Ping-Pong Buffer in Big and Little pipelines, respectively. As the Vertex Loader directly accesses the memory for different requests without caching and prefetching, we benchmark the memory access latency with varying access distance (stride) on the test FPGAs [18]. The benchmark results show that the $C_{acs,v}^i$ of the Big pipeline can be modeled by a linear function with respect to access distance, as shown in Equation (4), where $a$ and $b$ denote the coefficients, $S_{vprop}$ denote the size of the vertex property and $vid$ the source vertex ID of the edge. In addition, it has an upper bound and a lower bound, as there exists the worst-case and best-case memory access latency. For the Little pipeline, the Ping-Pong Buffer sequentially reads the vertices; hence, the $C_{acs,v}^i$ of the Little pipeline can be modeled by the access distance and the data size the memory channel can read per cycle, $S_{mem}$, as shown in Equation (4).

$$C_{acs,v} = \begin{cases} a \cdot (vid^i - vid^{i-1}) \cdot S_{vprop} + b, & \text{if Big pipeline} \\
(vid^i - vid^{i-1}) \cdot S_{mem}, & \text{if Little pipeline} 
\end{cases}$$  

Combining Equations (1)–(4), we can estimate the execution cycles of Big and Little pipelines for a given partition.

### B. Model-Guided Task Scheduling

Our task scheduling method includes inter- and intra-cluster task schedulings which are based on the estimated execution time of partitions (obtained by the performance model during the graph partitioning phase) to fully utilize the heterogeneous pipeline architecture for a graph. Firstly, the inter-cluster task scheduling method schedules partitions to the suitable type of pipelines and selects the most efficient pipeline combination to minimize the worst execution time of two clusters. Secondly, the intra-cluster task scheduling method cuts partitions to sub-partitions with equal execution times to utilize multiple pipelines within clusters. The task scheduling process runs offline and only once to generate a static scheduling plan for a graph on an application.

**Inter-cluster task scheduling.** Figure 7a shows two steps of inter-cluster task scheduling. Firstly, given a graph with total of $N_p$ partitions, it ascertains the number of dense partitions, $X$, and the number of sparse partitions, $Y$, to minimize the overall execution time of partitions on Big and Little pipeline clusters, $\sum_{p=0}^{N_p} T_{p,\text{Little}} + \sum_{p=0}^{N_p} T_{p,\text{Big}}$. In particular, a partition is marked as a sparse partition if the estimated execution time on the Big pipeline is shorter than that on the Little pipeline, otherwise marked as a dense partition. In Figure 7, $P_1$ and $P_2$ are marked as dense partitions.

Secondly, it determines the numbers of two types of pipelines to balance the execution time of the Big and Little pipeline clusters. Assume the total number of pipelines is $N_{pip}$ (bounded by the numbers of memory channels and memory ports of the platform), it sets $M + N = N_{pip}$ and tunes $M$ and $N$ to minimize the difference between execution times of two
clusters, \( \frac{\sum_{p=0}^{x} T_{\text{finish}}}{M} - \frac{\sum_{p=0}^{y} T_{\text{big}}}{N} \). Figure 7a illustrates the example with a total of five pipelines. Three Little pipelines are allocated to process two dense partitions, whereas two Big pipelines are built for the execution of four sparse partitions.

**Intra-cluster task scheduling.** In our design, pipelines within clusters process a partition cooperatively. This requires a partition divided to sub-partitions for multiple pipelines. While previous works [1], [4] cut the edges or vertices of partitions evenly, the irregularity of partitions results in unbalanced execution time of pipelines. Instead, we cut partitions to sub-partitions with similar execution times via the proposed performance model. Figure 7b shows the example to cut four sparse partitions for two Big pipelines and two dense partitions for three Little pipelines. As the Big pipeline buffers \( N_{\text{gpe}} \) times as many vertices as the Little pipeline, we merge every \( N_{\text{gpe}} \) sparse partitions into large sparse partitions before the performance estimation. To calculate the boundaries of sub-partitions by scanning once, we estimate execution time at granularity of a window that contains a certain number of edges during graph partitioning and then divide these windows into \( M \) or \( N \) clusters with similar overall execution times.

**V. ReGraph: An Automated Framework**

**A. ReGraph Framework Overview**

Figure 8 shows the overview of the ReGraph workflow. To obtain a customized accelerator design for a graph application, developers only need to write user-defined functions (UDFs) of three stages of the GAS model with the provided programming interface (Step ①). ReGraph then takes the UDFs, accelerator templates and platform specific optimizations to generate a set of synthesizable codes for accelerators with all possible pipeline combinations (Step ②). The synthesizable codes are compiled to bitstreams using the Xilinx Vitis tool-chain.

After that, users assign the graph for acceleration (Step ③). ReGraph groups vertices based on their in-degrees and partitions the graph. Then, the task scheduler with the built-in model-guided task scheduling method selects the accelerator with the most efficient pipeline combination and generates the scheduling plan (Step ④). Lastly, ReGraph deploys the selected accelerator and runs on the target FPGA (Step ⑤).

**B. Programming Interface**

```c
// logic for the Apply phase */
8 inline prop_t accApply(prop_t tProp, prop_t oProp, prop_t outDeg)
9 return ((kDampFixPoint * tProp) >> 7) * (1 << 16) /
10 (outDeg) >> 16;
```

Users can implement different graph accelerators by only writing three high-level functions: accScatter(), accGather() and accApply(). We demonstrate users’ efforts using PageRank as an example in List 1. In lines 2–5, the accScatter() returns the source vertex property, which means the vertex pushes its property (an averaged score) to its neighbours. In lines 5–6, the accGather() accumulates the property for destination vertices by adding the buffered property and incoming values. In lines 8–9, the accApply() calculates the new property of each vertex by dividing weighted accumulated score by its out-degree. For invoking the graph accelerator, ReGraph leverages the OpenCL APIs (enabled by Xilinx Vitis [44]) and provides several encapsulated APIs, e.g., initAccelerator() for initializing hardware context in one function.

**C. Platform-Specific Optimizations**

ReGraph adopts various platform-specific optimizations to provide great performance on Xilinx HBM-enabled devices.

**Memory port management.** Current HBM-enabled FPGA platforms support limited memory ports, e.g., 32 ports on U280, which largely constrains the number of pipelines instantiated on the platform. As a read port and a write port in one kernel can be bundled [44], we propose HBM port wrappers to bundle the write port in the Apply module and the read port for reading vertex properties. Wrappers receive memory requests, access the global memory, and send the responses to corresponding modules. This optimization reduces memory ports per pipeline from three to two.

**SLR crossing-aware optimizations.** Modern FPGAs have multiple super logic regions (SLRs) to enlarge resource capacity; however, the costly inter-SLR communication may result in low implementation frequency [14], [15]. Beyond applying the existing timing optimizations [1], [14], we implement the Big merger and the Little merger by a merge-tree with many small free running kernels [44] and merge the data within the SLR as much as possible before sending it to other SLRs.

**Utilizing URAMs.** We utilize URAMs for vertex buffering in Gather PEs, using a 64-bit data access granularity. We also solve the read after write hazard by utilizing a set of shift registers to obtain an II of one for Gather PEs.
D. Accelerator Generation

ReGraph generates a set of accelerators that have different numbers of Big and Little pipelines with the following steps. Firstly, it tunes the numbers of Scatter and Gather PEs to fully utilize the memory bandwidth of a memory channel. Secondly, ReGraph calculates the total number of pipelines that can be instantiated on the platform, $N_{pip}$. While resources allow $N_{pip}$ to be the number of memory channels, $N_{ch}$, the number of memory ports, $N_{port}$, constrains it, as each pipeline occupies two memory ports. Assume the number of reserved memory ports for the Apply module is $N_{res}$. ReGraph sets $N_{pip}$ as $\min(N_{ch}, \frac{N_{port}}{2} - N_{res})$. Thirdly, ReGraph enumerates the numbers of Big and Little pipelines, by varying $M$ from 0 to $N_{pip}$ and varying $N$ from $N_{pip}$ to 0 to generate $N_{pip}$ sets of configurations. Finally, with these configurations, ReGraph spreads the kernels even to SLRs according to a preset kernel-to-SLR mapping table and connects kernels with AXI streams or memory channels. We have developed a python-based code generation program that automatically generates the connectivity of the kernels for synthesizable codes.

TABLE II: Two HBM-enabled platforms used in experiments.

| Platform   | #LUTs | #URAMs | #SLRs | Bandwidth | #CH | #Port | TDP |
|------------|-------|--------|-------|-----------|-----|-------|-----|
| Alveo U280 (U280) | 1,304K | 960    | 3     | 460 GB/s  | 32  | 32    | 225 W |
| Alveo U50 (U50)   | 872K   | 640    | 2     | 316 GB/s  | 32  | 28    | 70 W  |

TABLE III: The graph datasets.

| Graphs       | $|V|$ | $|E|$ | $|D|$ | Type   | Categories |
|--------------|-----|-----|-----|-------|-----------|
| rmat-19-32 (R19) [22] | 524.3K | 16.8M | 32   | Directed | Synthetic |
| rmat-21-32 (R21) [22] | 2.1M  | 67.1M | 32   | Directed | Synthetic |
| rmat-24-16 (R24) [22] | 16.8M | 266.4M | 16  | Directed | Synthetic |
| graph500-scale23 (G23) [33] | 4.6M | 258.5M | 56 | Directed | Synthetic |
| web-google (GG) [33] | 916.4K | 5.1M | 6  | Directed | Web |
| amazon-2008 (AM) [33] | 735.3K | 5.2M | 7  | Directed | Social |
| web-hetong (HD) [33] | 2.0M | 14.9M | 7  | Directed | Web |
| web-baidu-baie (BB) [33] | 2.1M | 17.8M | 8  | Directed | Web |
| wiki-topics (TC) [23] | 1.8M | 28.5M | 16 | Directed | Web |
| pokec-relationships (PK) [23] | 1.6M | 30.6M | 19 | Directed | Social |
| soc-flickr-friend (FU) [33] | 1.7M | 15.6M | 9  | Undirected | Social |
| wikipedia-20070206 (WP) [10] | 3.6M | 45.0M | 13 | Directed | Web |
| liveJournal (LJ) [23] | 4.8M | 68.9M | 14 | Undirected | Social |
| ca-hollywood-2009 (HW) [33] | 1.1M | 56.3M | 53 | Undirected | Collabo |
| dbpedia-link (DB) [33] | 18.3M | 172.2M | 9  | Directed | Social |
| orkut (OR) [33] | 3.1M | 117.2M | 38 | Undirected | Social |

VI. EVALUATION

We first assess the efficiency of Big and Little pipelines and their performance models. We then evaluate the benefits of heterogeneity and resource utilization, followed by the demonstration of system scalability and the assessment of the cost of preprocessing. Finally, we compare ReGraph to state-of-the-art FPGA solutions and CPU/GPU solutions.

A. Experimental Setup

Hardware platform. Table II shows two HBM-enabled FPGAs used in our evaluation. U50 is a low-profile card with fewer resources and a lower thermal design power (TDP). It supports only 28 memory ports, resulting in a lower peak memory bandwidth. We host U280 and U50 on servers with Xeon Gold 6246R CPU and Xeon W-2155 CPU, respectively. Xilinx Vitis 2020.2 is used for development for both platforms.

Applications and datasets. We consider three graph processing applications as benchmarks: PageRank (PR), Breadth-First Search (BFS), and Closeness Centrality (CC). Table III shows the details of the used graph datasets, including synthetic [22] graphs and real-world large-scale graphs.

Implementation details. The prototype of ReGraph consists of 2,787 lines of HLS code for code templates, 2,063 lines of C++ code for graph preprocessing, scheduling and accelerator deployment and 423 lines of Python code for automated accelerator code generation.

Parameter details. The size of the Ping-Pong Buffer is 32KB. The depths of streams that cross SLRs are set to 16 for better timing. For all applications, the numbers of Scatter PEs and Gather PEs (with II of one) of a pipeline are set to eight. While the resources of the two platforms allow us to instantiate one pipeline per memory channel, the memory port limitation constrains the number of pipelines to 14 on U280 and 12 on U50. Each Gather PE buffers 65,536 destination vertices on U280 and 32,768 on U50. All raw graph data are 32-bit in our experiments. Same with ThunderGP [4] and GraphLily [17], ReGraph uses fixed-point data type for PR.

Baselines. ThunderGP [4] and Asiatici et al. [1] are two state-of-the-art graph processing frameworks using multiple SLRs and memory channels on DRAM-FPGA platforms. GraphLily [17] is a graph linear algebra overlay on HBM-equipped FPGAs that expresses different graph algorithms with two built-in primitives.

B. Efficiency of Big-Little Pipelines and Their Models

We first evaluate the performance of two types of pipelines on different partitions together with the proposed performance model. Figure 9 presents the measured and estimated execution time of PR of a single Big/Little pipeline on partitions of four graphs (profiled in Figure 2). We report execution time per eight partitions, as the Big pipeline processes eight partitions per execution, benefiting from data routing. As shown in Figure 9, the Little pipeline executes faster than the Big pipeline when the partition is dense (the first few partitions) while the Big pipeline performs better when the partition is sparse (the rest of partitions). This is attributed to the architectures of Big and Little pipelines. At the same time, the estimated performance is very close to the measured performance. The average error ratio (defined as the difference between estimated and measured execution time dividing measured execution time) of the Big pipeline’s model is only 4% and that of the Little pipeline’s model is 6%.

C. Benefits of Heterogeneity

Figure 10 shows PR implementations with different pipeline combinations, where we vary the numbers of Little and Big pipelines. The numbers of dense and sparse partitions are determined by the framework. Implementations with only Big pipelines (0L14B) or only Little pipelines (14L0B) are referred as homogeneous pipeline architectures.

There are several highlights. First, the best performance implementations are always with mixed pipeline types rather
throughput (GTEPS)

R19 R21 R24 G23 GG AM HD BB TC PK FU WP LJ HW DB OR

System selected implementation

Dense <---                                     --->Sparse
G23
LP est.
BP est.
LP meas.
BP meas.

Fig. 11: Resource utilization and frequency of PR implementations with all pipeline combinations on U280.

Fig. 12: Performance of PR with varying the number of pipelines on U280.

TABLE IV: Preprocessing time with one CPU (Xeon Gold 6248R) thread in millisecond.

| Graphs | R19 | R21 | R24 | G23 | GG | AM | HD | BB | TC | PK | FU | WP | LJ | HW | DB | OR |
|--------|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|----|----|
| Vertex Grouping (DBG) | 3.4 | 14.2 | 111.2 | 29.9 | 9.6 | 7.3 | 12.6 | 18.8 | 13.9 | 14.9 | 10.8 | 28.9 | 34.3 | 7.3 | 131.0 | 30.9 |
| Partitioning & Scheduling | 168.9 | 719.6 | 4054.1 | 2943.3 | 66.1 | 57.0 | 171.1 | 229.4 | 357.1 | 318.9 | 436.5 | 508.9 | 996.3 | 1290.4 | 2842.9 | 2977.1 |

than a single type, which demonstrate the benefits of heterogeneity. Moreover, the configuration on the numbers of Little and Big pipelines varies across different graphs, which demonstrates both Little and Big pipelines contribute to the overall performance. Second, the performance of our system selected implementations is close (around 92% on average) to that of the best implementations. Third, synthetic graphs (R19, R21, R24 and G23) have better performance and require more Little pipelines than real-world graphs, because they are relatively regular and have larger portion of edges located in dense partitions.

D. Resource Utilization

Figure 11 presents resource utilization and frequency of PR with different pipeline combinations on U280. We observe similar resource utilization for other applications. We omit the presentation of URAM utilization as it decides the partition size and is constantly 96% for all implementations. Overall, the highest performant implementations such as 7L7B only utilize around 30% of LUTs and less than 50% of BRAMs. This indicates that resource is no longer the bottleneck in ReGraph, benefiting from heterogeneous pipelines customization. In addition, with more Little pipelines (hence fewer Big pipelines), LUT and register consumption decrease but BRAM consumption increases. This is because Little pipelines cost more BRAMs with the Ping-Pong Buffer module, whereas Big pipelines cost more LUTs and registers in the Vertex Loader and Data Router modules. Lastly, the frequency is always above 210MHz, benefiting from our crossing SLR optimizations and the efficient resource utilization.

E. Scalability Exploration

Figure 12 shows the performance of PR with varying the number of pipelines on U280.
256MB capacity, when the number of HBM channels is small, some graphs are out of memory (marked as ‘OoM’). The trends in Figure 12 indicate ReGraph scales well on synthetic graphs or real-world graphs with high average degrees. However, super irregular and small graphs are unable to gain linear speedup, which is also observed in previous studies [1], [4]. This is because the constant overhead from partition switching overwhelms the speedup of multiple pipelines when partitions are super sparse.

F. Preprocessing Cost

Table IV shows the preprocessing time of PR on the target CPU with one thread. Overall, the preprocessing overhead is small and comparable to existing works [1], [4] as they have the same complexity: \( O(E) \) for graph partitioning and \( O(V) \) for DBG, where \( E \) stands for the number of edges of a graph and \( V \) indicates the number of vertices.

G. Comparison with State-of-the-arts

We compare ReGraph on U280 and U50 against ThunderGP [4], Asiatici et al. [1] and GraphLily [17].

**Performance.** Table V shows the performance comparison between ReGraph and three state-of-the-art works. For a more compelling comparison, we ported the open-sourced code of ThunderGP [47] to U280. It is worth noting that the ported ThunderGP (U280) is 1.3× faster than original design [4]. For the other two works, we obtain performance numbers from their papers. In short, ReGraph delivers significant speedups to all state-of-the-arts. Specifically, ReGraph outperforms Asiatici et al. [1] by up to 5.5×–5.9×, GraphLily [17] by 2.1×–3.7× and ThunderGP (U280) by 1.6×–4.4×. Even on U50, a budget platform with only three-quarters of the peak memory bandwidth of U280, ReGraph outperforms GraphLily [17] by up to 3.3× and ThunderGP (U280) by up to 3.7×.

**Resource efficiency.** Figure 13 shows the proposed resource-centric roofline model and resource efficiency comparison with recent designs. Processing frameworks on CPU and GPU, respectively. Table VI shows the configurations of the 48-core CPU platform where we run the latest available Ligra framework [37] and two different GPU platforms where we run the Gunrock framework [30]. We measure the CPU power using CPU Energy Meter [27], GPU power using nvidia-smi and FPGA power using xbutil [44]. The energy efficiency improvement is calculated as the ratio of ReGraph’s GTEPS/Watt to the comparison target’s GTEPS/Watt.

Figure 14 shows the comparison between ReGraph and Ligra on a latest server-level CPU. For PR, ReGraph delivers 1.6×–7.1× runtime speedup and up to 10×–38× improvement in energy efficiency. For BFS, ReGraph outperforms Ligra by 1.5×–9.7× in terms of performance and 9.5×–58× improvement in energy efficiency. The significant performance and energy efficiency improvements demonstrate the efficacy of customizing accelerators for graph processing.

Figure 15 shows the comparison with Gunrock on Tesla P100 and A100 GPUs. For PR, both GPUs perform better than ReGraph in terms of throughput, benefiting from much higher memory bandwidth. However, ReGraph delivers TABLE V: ReGraph on the U280 and U50 compared to state-of-the-art FPGA-based designs.

| Apps | SOTA Works (Platform) | Graph Datasets | Throughput (MTEPS) | Our Speedup (U280) | Power (GTEPS/Watt) |
|------|-----------------------|----------------|-------------------|--------------------|-------------------|
|      | Asiatici et al. [1] (UltraScale+) | DB | 920 | 4.2× | 5.9× |
|      |                  | R24 | 1,800 | 4.1× | 5.5× |
| PR   | GraphLily [17] (U280) | R21 | 4,653 | 2.8× | 3.3× |
|      |                  | HW | 7,471 | 2.9× | 2.1× |
|      |                  | PK | 2,933 | 2.3× | 2.8× |
|      |                  | OR | 5,940 | 1.7× | 2.1× |
|      | ThunderGP [4] (U280) | R21 | 5,920 | 2.1× | 2.6× |
|      |                  | HW | 6,147 | 2.4× | 2.5× |
|      |                  | PK | 3,832 | 1.8× | 2.1× |
|      |                  | OR | 5,661 | 2.1× | 2.2× |
|      |                  | HD | 1,760 | 4.0× | 4.4× |
| BFS  | GraphLily [17] (U280) | PK | 1,965 | 3.3× | 3.7× |
|      |                  | OR | 4,937 | 2.3× | 2.5× |
|      |                  | HW | 6,863 | 2.1× | 2.2× |
|      | ThunderGP [4] (U280) | R21 | 6,978 | 1.9× | 2.0× |
|      |                  | HW | 7,743 | 1.9× | 1.9× |
|      |                  | PK | 4,105 | 1.6× | 1.8× |
|      |                  | OR | 7,629 | 1.5× | 1.6× |
|      |                  | HD | 1,868 | 3.3× | 3.7× |
| CC   | ThunderGP [4] (U280) | R21 | 6,182 | 2.1× | 2.8× |
|      |                  | HW | 6,076 | 2.5× | 3.1× |
|      |                  | PK | 3,790 | 1.7× | 2.0× |
|      |                  | OR | 5,872 | 2.0× | 2.5× |
|      |                  | HD | 1,737 | 3.7× | 4.4× |
TABLE VI: CPU, GPU and FPGA platform specifications. Power is measured during execution.

| Platform            | Bandwidth | Power | Process | Release date |
|---------------------|-----------|-------|---------|--------------|
| Alveo U280 (FPGA)   | 460 GB/s  | 35 W  | 16-nm   | Q4 2018      |
| Xilinx Ultrascale   | 122 GB/s  | 208 W | 14-nm   | Q1 2020      |
| Tesla P100 (GPU)    | 732 GB/s  | 176 W | 16-nm   | Q2 2016      |
| Tesla A100 (GPU)    | 2.039 GB/s| 187 W | 7-nm    | Q2 2020      |

2.4× (geomean) energy efficiency improvement over P100. For BFS, ReGraph delivers better performance than P100 and significantly improved energy efficiency: 2.5×–9.2× improvement (7× in geomean). Meanwhile, A100 delivers the best performance with its impressive memory bandwidth and advanced manufacturing process. Still, ReGraph demonstrates an up to 3.5× (geomean) energy efficiency improvement over A100. In summary, ReGraph delivers better energy efficiency than GPUs that have the same or even more advanced manufacturing process.

VIII. CONCLUSION AND DISCUSSION

HBM-enabled FPGAs have massive memory bandwidth. However, the bottleneck in processing graphs has moved to other resources, making it difficult to fully utilize the bandwidth. In this paper, we propose the use of heterogeneous pipeline architectures to alleviate this issue. We first identify two kinds of major workloads within graph processing and showed that the processing of dense vs sparse graph partitions can be optimized in different ways. This gives rise to two customized pipeline types, designed to be resource-efficient for their specific workloads. We also propose an effective task scheduling method that determines pipeline combinations and schedules the graph partitions accordingly. Our framework, ReGraph, further eases the entire development process, delivering up to 5.9× performance speedup and 12× resource efficiency improvement compared to the state-of-the-art.

In our work, we found architectural features that will improve graph processing on future HBM-enabled FPGAs. Firstly, logic resources should be increased in general to match the memory level parallelism provided by HBM so that the system is more balanced. Secondly, current HBM restricts graph sizes to smaller than 8 GB. As a future work, we plan to introduce SSDs as storage while using HBM as buffers to process billion-scale graphs. Thirdly, an increased number of flexible memory ports are needed to improve the utilization of the HBM. ReGraph’s performance can be scaled even further once these features are available.

VII. RELATED WORK

In the early stage, ForeGraph [9] explores graph processing with multiple FPGA boards. Later, FabGraph [36] enables two-level vertex buffering technique to ForeGraph and improves performance by 2×. Their technique in high-level is overlapping vertex access and edge process, which is similar to our ping-pong buffering design in the Little pipeline. However, they only conduct simulation-based experiments, while we implement them efficiently with HLS. Zhou et al. proposed a series of FPGA-based graph processing works [49]–[52]. HitGraph [51] executes the scatter and the gather stages in a bulk synchronous parallel (BSP) manner. Instead, ReGraph pipelined the Scatter, Gather and Apply stages, hence reducing memory accesses to the global memory. Oguntebi et al. presented an open-source modular hardware library, GraphOps [31]. Chen et al. proposed an OpenCL-based graph processing framework on FPGAs [3]. ThunderGP [4] fully utilizes the memory bandwidth of the DRAM-FPGA platform. Asiatici et al. [1] proposed to use cache miss optimized memory system for efficient graph processing. However, these solutions suffer from high resource cost, which essentially prevents them from scaling on HBM platforms. Although GraphLily [17] explored the graph processing on HBM, they failed to customize accelerators as their main technique is to reuse bitstreams of basic modules (e.g., SpMV/SpMSpV). ReGraph outperforms all the above works significantly in both performance and resource efficiency. To the best of our knowledge, we are the first to propose heterogeneous pipeline architectures for graph processing accelerators.

There also exists ASIC-based graph accelerators that demonstrate superior performance under the simulation environment. For example, Graphicionado [16] achieves 4.5 GTEPS for PageRank via effective graph partitioning and vertex buffering to an on-chip memory. GraphDynS [48] achieves more than 85 GTEPS with HBM (512GB/s) through a hardware/software co-designed approach. Ozdal et al. [32] presented an architecture template based on asynchronous execution model to exploit memory-level parallelism, which delivers 3× speedup over CPU. However, these solutions adopt homogeneous pipeline designs and do not consider resource capacity constraint. Rather than having monolithic pipelines, our heterogeneous pipeline designs are lightweight and tailored to diverse workloads of graph processing, delivering significantly improved resource efficiency.
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