Input referred low-frequency noise analysis for single-layer graphene FETs

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Abstract—The bias-dependence of input referred low-frequency noise (LFN), $S_{\text{VG}}$, is a crucial figure of merit (FoM) since it can provide advantageous information regarding the selection of the operating point of analog/RF circuits. It can be defined as [1]:

$$S_{\text{VG}} = \frac{S_{\text{ID}}}{g_m}$$  \hspace{1cm} (1)

where $S_{\text{ID}}$ is the output or drain current LFN and $g_m$ is the transconductance of the device. Equation (1) has been proven to be valid in all regions of operation [2]. LFN model proposed in [2] is based on carrier number fluctuation ($\Delta N$) effect which is generated by trapping/detrapping mechanism of active traps near the gate oxide of the device [3] and assumes a $(g_m/I_D)^2$ bias-dependence of normalized output noise divided by squared drain current ($S_{\text{ID}}/I_D^2$) where $I_D$ is the drain current of the transistor. Such approximation which is valid under the consideration of a uniform channel at low drain voltage $V_{\text{DS}}$ region, results in a constant $S_{\text{VG}}$ vs. gate voltage $V_{\text{GS}}$ (or $I_D$) because of (1), as shown in the following expression:

$$S_{\text{VG}} = \frac{S_{\text{ID}}}{g_m} = \frac{S_{\text{ID}}^2}{I_D} \frac{I_D}{g_m} = \frac{S_{\text{VFB}}}{I_D} \frac{I_D}{g_m} = S_{\text{VFB}}$$  \hspace{1cm} (2)

where $S_{\text{VFB}}$ is the flat-band voltage spectral density related to trapped charge density [2] and is a constant.

Two more mechanisms generate LFN to semiconductor devices: mobility fluctuation ($\Delta \mu$) effect due to fluctuations of the bulk mobility which is described by the empirical Hooge formula [4] and contact resistance contribution ($\Delta R$) [5]. Recent experimental findings from MOSFETs prove that the approximation of a constant $S_{\text{VG}}$ does not hold [5], [6]. An increasing trend of $S_{\text{VG}}$ is reported towards deeper weak inversion due to $\Delta \mu$ mechanism as well as a similar increase towards stronger inversion due to $\Delta N$ and $\Delta R$ effects which result in a minimum in moderate inversion. This can be a reliable indicator for circuit designers to select the specific regime to bias the circuits. As mentioned before, the simplified $(g_m/I_D)^2$ $\Delta N$ approach provides a constant $S_{\text{VG}}$, but the aforementioned increase due to $\Delta N$ effect in higher current regime of MOSFETs is attributed to Coulomb Scattering (CS) effect [2]. The same occurs for more complete $\Delta N$ models [5, §6.3.1], where the vast percentage of this increase is still induced by CS effect.

Nowadays, new material candidates are explored to replace silicon for integrated circuits (ICs) due to the limitations on gate length scaling in CMOS devices. Among them, graphene has been proven to be an ideal contestant for RF applications due to its remarkable characteristics [7]. Graphene transistors (GFETs) have already been fabricated and used in circuits at research labs [8] but for large scale integration production, LFN and more specifically $S_{\text{VG}}$ should be thoroughly investigated and this is the main goal of the present study. LFN is up-converted to phase noise and consequently, deteriorates the performance of analog/RF circuits such as oscillators [9] or terahertz detectors [10]. Several GFET LFN characterization and modeling studies have been reported [11]-[15] where simple $S_{\text{ID}}/I_D^2$ models [11], [12] based on $\Delta N$ $(g_m/I_D)^2$ approximation [2] have been proposed, whereas a complete physics-based compact model including all the LFN generators ($\Delta N$, $\Delta \mu$, $\Delta R$) was developed by our group [14], [15] based on a chemical-potential IV model [16]. Our model is proven to be valid in all regions of operation as it includes the effect of non-homogeneous channel on LFN as well as the contribution of Velocity Saturation (VS) effect at high electric field regime. To our knowledge, no study has been reported yet regarding the behavior of $S_{\text{VG}}$ in GFETs. A constant $S_{\text{input}}$ is defined in [11] which is equivalent to $S_{\text{VFB}}$ mentioned before, but any possible bias-dependence of $S_{\text{VG}}$ has not been explored so far. In this work, we give insight into the performance of $S_{\text{VG}}$ in GFETs at different operating conditions by validating our model with experimental data from three fabricated short-channel GFETs [17].

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Fig. 1. Transconductance $g_m$ (upper plots) and input noise $S_{VGS}^* f = S_{ID}^* f / g_m^2$, referred to 1 Hz, (bottom plots) vs. gate voltage $V_{GS}$ with markers representing the measurements and lines the model for short-channel GFETs with $W=12 \, \mu m$ and $L=100 \, nm$ (a, d), $L=200 \, nm$ (b, e) and $L=300 \, nm$ (c, f), respectively for all available drain voltage $V_{DS}$ values.

II. DEVICES AND MEASUREMENTS

$I_D$ and LFN measurements were conducted at three short-channel single-layer (SL) GFETs with width $W=12 \, \mu m$ and gate length $L=300 \, nm$ (A300), $L=200 \, nm$ (A200) and $L=100 \, nm$ (A100), respectively [14], [17]. The data were obtained after sweeping $V_{GS}$ from strong p-type to strong n-type region including charge neutrality point (CNP) for a wide range of $V_{DS}$ values, covering from low to high electric field regime. In the present work, p-type region is exclusively shown as maximum $g_m$ is reported there [14] while asymmetries are recorded in IV data between p- and n-type region [14] due to different electron and hole mobilities or due to effects caused by parasitic junctions at graphene metal contacts (For more details on the device fabrication process and schematics as well as the measurement setup, see [14], [17]). Regarding LFN, $S_{ID}$ was measured from 1.5 Hz to 2.5 KHz, averaged from 10-40 Hz in order to calculate its value at 1 Hz and then $S_{VGS}$ data were estimated through (1) where $g_m$ is extracted as the first derivative of $I_D$ w.r.t. $V_{GS}$.

In order to calculate the simulated $S_{VGS}$ through the $S_{ID}$ model [14], [15], the value of the modeled $g_m$ is needed in order to apply (1). Thus, it is crucial to have a precise fitting between measured and simulated $g_m$ and this is achieved successfully as it is illustrated in Fig. 1a (A100), 1b (A200) and 1c (A300), respectively where $g_m$ is plotted vs. $V_{GS}$ at all available $V_{DS}$ values. One parameter set is used for the IV simulations which can be found elsewhere [14].

III. RESULTS – DISCUSSION

A complete bias-dependent analysis of experimental $S_{VGS}$ data at $f=1$ Hz is presented in this section while the model is validated successfully at every operation regime. Measured $S_{VGS}$ presents a minimum versus $V_{GS}$ for every device under test (DUT) at each individual $V_{DS}$ from low to high electric field resulting in a parabolic shape and the model precisely captures this trend (cf. Fig. 1d-1f). (extracted LFN model parameters can be found elsewhere [14].) It is also evident that the magnitude of this minimum $S_{VGS}$ has a slight $V_{DS}$ dependence while the whole $S_{VGS}$ shifts slightly to higher $V_{GS}$.
as $V_{DS}$ increases which can be justified by the corresponding increment of $V_{GSM}$ [14]-[16]. In general, $S_{VG}$ is nearly independent of $V_{DS}$ towards p-type region below the $V_{GS}$ value where its minimum is recorded ($V_{GS,minVSG}$), and the model captures this trend. Looking thoroughly to the $V_{GS-minVSG}$, one could notice that it is located in the same point where maximum $|g_m|$ is achieved ($V_{GS-maxGM}$=$V_{GS-minVSG}$) for all DUTs and this can be explained by (1) where $g_m$ is in the denominator. The latter is shown in Fig. 2a vs. $V_{GS}$ for the A100 GFET both low $V_{DS}$=60 mV and high $V_{DS}$=0.3 V. $S_{VG}$ is shown in the left y-axis while $|g_m|$ in the right. Up to now, $S_{D/I0^2}$ was shown to be maximum at the same preceding point where the peak of the well-known $\Delta N$ effect related M-shape is also reported [11]-[15] and this is confirmed by our simulations in Fig. 2b (left subplot: $V_{DS}$=60 mV, right subplot: $V_{DS}$=0.3 V, $S_{VG}$-S$_{D/I0^2}$; left y axis) vs. $V_{GS}$ where $\Delta N$, $\Delta \mu$, $\Delta R$ effects are also presented. The latter indicates that $V_{GS-opt}$ ensures minimum $S_{VG}$ appropriate for biasing circuits in terms of LFN performance despite the maximum $S_{D/I0^2}$ recorded there.

In Fig. 3 both measured and modeled $S_{VG}$ are presented vs. $V_{GS}$ (Fig.3a) and $V_{DS}$ (Fig.3b) for the A100 DUT whereas a long-channel model after de-activating VS effect [14],[15] is also depicted with dashed lines. Both low and high $V_{DS}$=60 mV, 0.3 V cases are drawn in Fig. 3a and a decrease of the total model (similarly to $S_{D/I0^2}$ [14],[15]) is observed at high $V_{DS}$ which is accurately confirmed by the experimental data. This reduction is associated with VS effect which has been successfully incorporated in our model [14],[15]. Oppositely, the long-channel model overestimates noise in the high $V_{DS}$ case while it coincides with the total model at low $V_{DS}$ where VS effect is insignificant. Regarding Fig. 3b, $S_{VG}$ is illustrated for two $V_{GS}$ values; near ($V_{GS}$=1 V) and away ($V_{GS}$=0.6 V) CNP. At higher $V_{DS}$, the complete model predicts successfully experimental $S_{VG}$ while the long-channel one overestimates it and the latter is more evident near CNP ($V_{GS}$=1 V). No strong deviations are observed to $S_{VG}$ with respect to $V_{DS}$ away from CNP confirming its independence of $V_{DS}$ while near CNP there is a steep decrease of $S_{VG}$ from $V_{DS}$=30 mV to 60 mV while it slightly changes for the rest of higher $V_{DS}$ values. This decrease is attributed to $V_{GS}$=1 V being higher than $V_{GS-opt}$ at $V_{DS}$=30 mV and thus $S_{VG}$ has already started to increase in contrary with the rest of $V_{DS}$ cases which exhibit higher $V_{CNP}$ and consequently higher $V_{GS-opt}$ (cf. Fig. 1d).

In order to investigate deeper the contribution of each of $\Delta N$, $\Delta \mu$ and $\Delta R$ mechanisms to $S_{VG}$, an explicit analysis is demonstrated in Fig. 4 where $S_{VG}$ is sketched vs. $I_D$ for low (cf. Fig. 4a-4c) and high (cd. Fig. 4d-4f) $V_{DS}$ for all the available GFETs. Apart from the measurements and the total model, each individual contribution is shown with dashed and dotted lines for every case. It is evident that $\Delta N$ effect increases $S_{VG}$ with $I_D$ away from CNP towards p-type region below $V_{GS-opt}$ for both low and high $V_{DS}$. It is worth mentioning that this increase is recorded without the impact of CS effect as in MOSFETs since the LFN model fits the data without the contribution of the aforementioned mechanism. Near CNP above $V_{GS-opt}$, $\Delta N$ contribution decreases as $I_D$ is lessened for low $V_{DS}$ which is reasonable as $S_{D/I0^2}$ is quite imperceptible there (deep minimum of M-shape, cf. Fig. 2b [14],[15]). In the contrary, at high $V_{DS}$, $\Delta N$ has a sizeable effect on $S_{VG}$ near CNP and adds to its increase with $I_D$ noticed there as the non-homogeneous channel results in an increase of the minimum of $S_{D/I0^2}$ M-shape, cf. Fig. 2b [14],[15] which apparently affects $S_{VG}$ also. $\Delta N$ contribution continues to grow with $I_D$, at stronger p-type region both at low and high electric fields where with the simultaneous effect of $\Delta R$ effect, a further and steeper boost
is caused to $S_{VG}$ especially at high $V_{DS}$ region; $\Delta R$ is trivial near CNP. Regarding $\Delta \mu$ effect, it is mainly responsible for the increase of $S_{VG}$ with $1/I_D$ near CNP above $V_{GS-opt}$. $\Delta \mu$ main contribution to $S_{VG}/I_D^2$ has been shown to be near CNP [14], [15] (cf. Fig. 2b), and this is confirmed regarding $S_{VG}$ in the present study. $\Delta \mu$ effect is also noticed to increase with $I_D$ towards stronger p-type region below $V_{GS-opt}$ at both high and low $V_{DS}$ and thus, can moderately contribute to $S_{VG}$ even away CNP. The above theoretical observations are successfully verified on experimental data from all the DUTs (cf. Fig. 4.)

IV. CONCLUSIONS

Input referred LFN is for the first time analyzed thoroughly for SL GFETs in this brief. The assumption of a constant $S_{VG}$ versus $V_{GS}$ is experimentally proven to be incorrect in GFETs, similarly to CMOS. Instead, a parabolic-like behavior is demonstrated around an optimum $V_{GS-opt}$ point where $|g_{m}|$ is maximized. The coexistence of maximum $|g_{m}|$ and minimum input LFN can certainly induce an attractiveness from the circuit design aspect regarding the specific point. We successfully validated our recently proposed LFN model with the above experimental findings where $\Delta \mu$ mechanism is proven to mainly increase $S_{VG}/I_D^2$ is reduced near CNP above $V_{GS-opt}$ whereas below this, $\Delta N$ leads to an $S_{VG}$ increment towards stronger p-type region which becomes even steeper with the concurrent contribution of $\Delta R$ effect far away from CNP.

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