Wideband Signal Analyzer Based on Time-Interleaved ADCs with Digital Calibration

A S Fateeva\textsuperscript{1,2}, G V Nikonova\textsuperscript{1} and I E Kashchenko\textsuperscript{2}
\textsuperscript{1}Omsk State Technical University, 11 Mira ave., Omsk, 644050, Russia
\textsuperscript{2}JSC Omsk Research and Development Institute of Instrument Making, Omsk, Russia

Abstract. This paper presents a novel architecture of wideband signal analyzer based on time-interleaved ADCs. Architecture of signal analyzer include improved method of digital calibration of ADC channels operating in the time-interleaved mode of input signals. This method is based on the least squares method. The advantage of the proposed method is high speed and high accuracy of ADC channels tuning in comparison with the majority of existing methods, which are based on the least squares method. The results of simulation modeling of the proposed method, including spectral analysis of the output signal before and after calibration, are presented. The comparison of the proposed method with existing methods is performed.

1. Introduction
Modern wideband signal analyzers can analyze the signal bandwidth up to several tens of gigahertz. Various methods are used to extend the analysis band, including parallel switching of the ADC in time-interleaved mode. Parallel switching on of several ADCS allows expanding the bandwidth of the signal analyzer's receiving path using the time-interleaved method [1]. The use of multiplexing signals with time interleave allows to achieve high performance of receiving paths-up to 20 GSMP / sec.

However, in practical implementation, this method has significant disadvantages associated with the spread of parameters of real ADC, uncontrolled time delays of paths, aperture error of ADC, etc. [2]. Ultimately, this can affect the quality of signal reception, namely the signal-to-noise ratio and distortion (SINAD). To compensate for most of these shortcomings, various methods of calibration of ADC channels are used [3]. Recently, digital methods for calibrating the reference voltage offset, gain, and time delay between channels have become widely used [4]. However, existing digital calibration methods require a calibration procedure in a special mode when the actual signal is not received. At the same time, the time required to complete calibration reduces the performance of the digital signal processing device. In some cases, the performance of a digital signal processing device is a key indicator of the entire communication system. Therefore, speeding up the ADC channel calibration procedure is one of the priorities in the development of broadband signal analyzers.

2. Theory
2.1. Signal Multiplexing with time-interleaved ADCs
Block diagram of multiplexing signal with time-interleaved ADCs shown in figure 1 [2].
In this block diagram, the input analog signal is simultaneously fed to the input of 4 ADCs (ADC1 ... 4). ADCs clock-port is connected to a clock synthesizer in such a way that the initial phases of the clock signals are shifted by 90° in turn. This allows you to synchronize the multiplexing of time-interleaved signals and restore the digital signal using a digital multiplexer with a sampling rate four times higher than the ADC sample rate. In this way, the bandwidth extension for the digital signal processing device is achieved. It is obvious that the quality of the received signal depends on the identity of the parallel ADC channels [2]. The difference in ADC channel parameters leads to a decrease in the signal-to-noise ratio and the appearance of distortion (SINAD).

2.2. LMS-algorithm for Adjusting the Gain and Reference Voltage Offset

Offset of the ADC reference voltage is often associated with propagation in the parameters of the built-in operational amplifiers and comparators. In addition, the offset of the ADC reference voltage can occur due to the asymmetry of the ADC conversion stages and is associated with errors in the production of chips at the fabric.

The difference in the gain of several ADCS is due to parasitic capacitances and inductances of operational amplifiers, as well as differences in the parameters of input analog capacitors.

To find the offset of the reference voltage, we select the reference voltage of one of the ADCS. Then the averaged RMS deviation of the digital signal from the parallel ADC output relative to the reference ADC will determine the offset of the reference voltage [5]. The difference in the gain of parallel ADCS can be found in the same way, except that instead of rejecting the digital signal, the value of this signal module at the output of each ADC is required.

Using an iterative algorithm based on the least squares method (LMS), you can find and compensate for the offset of the reference voltage, and the difference in the gain of parallel ADCS. To do this, select one of the parallel ADCS as the reference (for example, the first ADC). Then an iterative algorithm based on the least squares method for determining the offset voltage of parallel connected ADCS will look like this:

\[ a_i(n) = a_i(n-1) + \mu(\bar{x}(n-1) - x_i(n-1)) \]  \hspace{1cm} (1)

where \( x_i(n) \) to the digital output of the reference (first) ADC; \( x(n) \) - digital output to one of ADC; \( \mu \) is the adaptation step; \( a_i \) is the reference bias voltage of one of the parallel ADCs relative to the reference ADC.
In turn, the algorithm for finding the gain in the ADC with parallel connection can be represented by the following expression:

\[ k_i(n) = k_i(n-1) + \mu_k (x(n-1) - x_1(n-1)) \]  

(2)

where \( x_1(n) \) is the digital output from the reference (first) ADC; \( x_i(n) \) is the digital output from one of the ADCs; \( \mu \) is the adaptation step; \( k_i \) is the parameter that defines the difference of the gains of one of the parallel ADCs relative to the reference ADC. The parameter \( k_i \) is represented by the following expression:

\[ k_i = \frac{g_1}{g_i} \]  

(3)

where \( g_1 \) is the gain of the reference (first) ADC; \( g_i \) the gain of one of the parallel ADC.

The values of \( a_i \) and \( k_i \) obtained using expressions (1) and (2) should be “averaged” to increase the accuracy and speed of calibration. For averaging, all methods based on the accumulation of a large amount of data and methods based on exponential averaging are used [6]. Using custom averaging methods requires large computational resources. Exponential averaging does not require large computational resources, however, it involves the use of two averaging parameters (forward and reverse search). In addition, the use of the division operation is required to find the inverse gain.

3. Research

3.1. Euler numerical integration method for averaging data

An alternative method of "averaging" the coefficients obtained using expressions (1) and (2) is a method based on the numerical method of Euler integration. The basis of integration is the classical Euler formula:

\[ y(t + \Delta t) = y(t) + \Delta t \cdot f(x(t), y(t), t) + \varepsilon \]  

(4)

where \( y(t) \) is the current state; \( \Delta t \) increment; \( f(x(t), y(t), t) \) is an increasing speed. Based on formula (3), one can obtain an expression for integration in a discrete form. Depending on what input data will be taken into account when calculating the result, the Euler method can be direct or inverse [7]. It is more convenient to use the direct method to implement the averaging function. The direct Euler method is described by the following expression:

\[ y(n) = y(n-1) + P[t(n) - t(n-1)] \cdot x(n-1) \]  

(5)

where \( y(n) \) is the current value of the function; \( P \) gain (determines the gain for the increment), \( x(n) \) - input. To "average" the offset of the reference voltage of one of the parallel ADCs relative to the reference ADC \( (a_i) \), you can write the following expression:

\[ A_i(n+1) = A_i(n) + P[t(n) - t(n-1)] \cdot A_i(n-1) \]  

(6)

where \( A_i(n) = (a_i(n) - a_i(n-1)) \). In practice, the implementation of the “averaging” algorithm based on expression (5) will require three adders and two factors. A distinctive feature will be that to change the increment step (averaging speed) one coefficient \( P \) is used, which greatly simplifies the adjustment of the parameters of the ADC calibration system. In a same way, we can describe the function of “averaging” the gain of parallel-connected ADCs:

\[ K_i(n+1) = K_i(n) + P[t(n) - t(n-1)] \cdot K_i(n-1) \]  

(7)

where \( K_i(n) = (k_i(n) - k_i(n-1)) \). It should be noted that the use of large values of the coefficient \( P \) leads to an increase in the error \( \varepsilon \) and, accordingly, the accuracy of the calibration of the ADC as a whole.

3.2. Simulation of the proposed method for regulating the offset of the reference voltage and gain

To study and analyze the effectiveness of the proposed method for regulating the offset of the reference voltage and gain, a specialized simulation model was developed. This model includes four parallel-connected 12-bit ADCs, a clock synthesizer, a digital multiplexer, a reference oscillator, and a gain and bias voltage control unit. The block diagram of the model is shown in figure 2.
Figure 2. Block diagram of time time-interleaved ADCs with the unit of correction of reference voltage and gain

In this block diagram, the gain and bias voltage control unit implements digital signal processing algorithms in accordance with formulas (1) - (3) and (5), (6). The first ADC was chosen as the reference ADC. The source data for the simulation are presented in Table 1.

Table 1. The source data for simulate

| #ADC | 1   | 2   | 3   | 4   |
|------|-----|-----|-----|-----|
| Difference of reference voltage | 0   | 0.005 | -0.005 | 0.001 |
| Difference of gain            | 1   | 1.005 | 0.995  | 1.01  |
| Sampling frequency (MHz)      | 125 | 125  | 125  | 125  |
| Resolution (bits)             | 12  | 12   | 12   | 12   |

Figure 3 shows the signal spectrum at the output of the first ADC with the sine signal of 10 MHz.
Figure 3. Sine wave at the output of the first ADC (Fin=10 MHz).

The spectral characteristics of the signal at the output of the first ADC: 1) signal to noise ratio (SNR): 62.0 dB, 2) parasite-free dynamic range (SFDR): 71.7 dB, 3) Total Harmonic Distortion (THD): -71.2 dB. In Figure 4 we present the analysis of the signal at the output of the digital multiplexer was carried out without a correction block for.

Figure 4. The spectrum of the signal at the output of a digital multiplexer with a sinusoidal signal of 10 MHz (without calibration).

As seen in Figure 4, parasitic components are present in the signal spectrum. Spectral characteristics of the digital multiplexer output signal (without calibration):
1) Signal-to-noise ratio (SNR): 53.7 dB.
2) Spurious-free dynamic range (SFDR): 56.3 dB.
3) Total harmonic distortion (THD): -68.3 dB.
The signal analysis at the output of the digital multiplexer was performed with pre-calibration of the gain and offset voltage of all ADCs. The parameters of the correction block were selected as follows:

1) The adaptation step for correcting the reference voltage offset is equal to $\mu = 0.1$.
2) The adaptation step for the gain correction is equal to $\mu_k = 0.1$.
3) The coefficient for "averaging" the offset of the reference voltage is $P_a = 40000$.
4) The coefficient for "averaging" the win is $P_k = 40000$.

Figure 5 shows the signal spectrum at the output of a digital multiplexer with calibrated ADCs.

![Figure 5](image_url)

**Figure 5.** The spectrum of the signal at the output of a digital multiplexer with a 10 MHz sine wave (with calibration).

As can be seen from the graph shown in Figure 5, the level of spurious components in the spectrum of the output signal has decreased significantly. Spectral characteristics of the signal at the output of the digital multiplexer with the included correction unit:

1) Signal to noise ratio (SNR): 61.3 dB.
2) Spurious-free dynamic range (SFDR): 68.9 dB.
3) Total Harmonic Distortion (THD): -68.2 dB.

In conclusion, we performed a simulation of the input path of the signal analyzer using wideband signals.

Figure 6 shows the signal spectrum at the digital output of the signal analyzer model when exposed to a multi position signal with a 20 MHz bandwidth. In this case, the carrier frequency ($F_c=190 \text{ MHz}$) is located behind the frequency range of the ADC.
Figure 6. The spectrum of the wideband multi position signal with a 20 MHz bandwidth signal at the digital output of a signal analyzer (with calibration).

As can be seen from figure 6, there are no discrete and side components in the signal spectrum. In the next step, the signal analyzer input was affected by a signal with a bandwidth of 210 MHz. Figure 7 shows the signal spectrum at the digital output of the signal analyzer when exposed to a signal with a bandwidth of 210 MHz.

Figure 7. The spectrum of the wideband multi position signal with a 210 MHz bandwidth signal at the digital output of a signal analyzer (with calibration).
As can be seen from figure 7, the amplitude-frequency response of the signal analyzer is linear over the entire frequency range.

4. Results of simulating

Table 2 shows the spectral characteristics of the signal (SNR, SFDR, THD) at the output of the simulation model with calibrated ADCs. Correction block parameters: $\mu = 0.1; \mu K = 0.1; P_A = 40,000; P_K = 40,000$.

| Frequency, MHz | SNR, dB | SFDR, dB | THD, dB |
|---------------|--------|---------|--------|
| 10            | 61.3   | 68.9    | -68.2  |
| 50            | 59.2   | 66.7    | -51.4  |
| 150           | 55.7   | 66.3    | -48.9  |
| 200           | 53.6   | 66.2    | -47.7  |

Based on the data presented in Table 2, it can be concluded that the use of the proposed calibration method for correcting the reference voltage bias and gain can significantly improve the spectral characteristics of the signal when using the multiplexing method with a time division of signals. It is worth noting that the proposed calibration method does not depend on the frequency and has the same efficiency in the entire input signal band. The main factor affecting the quality of ADC calibration is the choice of parameters for the correction unit. The smaller the adaptation step ($\mu$) and the greater the gain $P$, the more accurately the ADCs are calibrated, but the calibration time is significantly increased.

5. Conclusion

Calibration method proposed in this article for the time-interleaved ADCs in wideband signal analyzer allows to significantly increase the dynamic characteristics of output signal. Using the numerical Euler integration method for the "averaging" procedure can significantly reduce processing requirements. During the analysis of the simulation results, it was found that the proposed calibration method does not depend on the frequency and is equally effective in the entire input signal band. In addition, the proposed method does not distort the transfer characteristic of the signal analyzer. The use of this method may be limited by the choice of parameters for the correction unit, since the calibration speed and calibration accuracy are mutually exclusive.

6. References

[1] W. C. Black and D. A. Hodges Dec. 1980 Time-interleaved converter arrays IEEE J. Solid-State Circuits, vol. 15, no. 12, pp 1022–1029
[2] A. Fateeva, G. Nikonova April 2019 Digital Receiving Devices with Time-Division Multiplexing for Bandwidth Extension In Proceedings of Ural Symposium on Biomedical Engineering, Radioelectronics and Information Technology (USBEREDIT 2019)
[3] B. T. Reyes, L. Tealdi, G. Paulina et al. February 2014 A 6-bit 2GS/s CMOS time-interleaved ADC for analysis of mixed-signal calibration techniques In Proceedings of the IEEE 5th Latin American Symposium on Circuits and Systems (LASCAS '14), pp 1–4
[4] H. Jin and E. K. F. Lee Jul. 2000 A digital-background calibration technique for minimizing timing-error effects in time-interleaved ADCs IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 47, no. 7, pp 603–613
[5] J. Eklund and F. Gustafsson May 2000 Digital offset compensation of timeinterleaved ADC using random chopper sampling In IEEE Symp. Circuits Syst., pp 447–450
[6] Y. Yin, J. Li, and H. Chen December 2014. A digital background calibration algorithm of time-interleaved ADC In Proceedings of the International Conference on Anti-counterfeiting, Security, and Identification (ASID’14), pp. 1–4 (Macao,China)
[7] Butcher, John C. Numerical Methods for Ordinary Differential Equations. New York: John Wiley & Sons. ISBN 978-0-471-96758-3.
Acknowledgments
The reported study was funded by RFBR, project number 19-38-90162