High Pressure Deuterium Passivation of Charge Trapping Layer for Nonvolatile Memory Applications

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Abstract: In this study, the deuterium passivation effect of silicon nitride (Si$_3$N$_4$) on data retention characteristics is investigated in a Metal-Nitride-Oxide-Silicon (MNOS) memory device. To focus on trap passivation in Si$_3$N$_4$ as a charge trapping layer, deuterium (D$_2$) high pressure annealing (HPA) was applied after Si$_3$N$_4$ deposition. Flat band voltage shifts ($\Delta V_{FB}$) in data retention mode were compared by CV measurement after D$_2$ HPA, which shows that the memory window decreases but charge loss in retention mode after program is suppressed. Trap energy distribution based on thermal activated retention model is extracted to compare the trap density of Si$_3$N$_4$. D$_2$ HPA reduces the amount of trap densities in the band gap range of 1.06–1.18 eV. SIMS profiles are used to analyze the D$_2$ profile in Si$_3$N$_4$. The results show that deuterium diffuses into the Si$_3$N$_4$ and exists up to the Si$_3$N$_4$–SiO$_2$ interface region during post-annealing process, which seems to lower the trap density and improve the memory reliability.

Keywords: deuterium high pressure anneal; flash memory; silicon nitride; retention

1. Introduction

Although research on ReRAM, MRAM, PCM etc. is being actively conducted for next-generation nonvolatile memories [1,2], the demands for Silicon-Oxide-Nitride-Silicon (SONOS) flash memory are still dominant. SONOS memory can obtain large capacity easily and have a simple circuit structure. Due to these advantages, the memory has been continuously developed since its invention, improving its storage capacity and reliability [3]. In SONOS, to optimize the silicon nitride (Si$_3$N$_4$) film which is used as charge trapping layer (CTL) of the device is very important for the performance enhancement. Substantial research has been carried out to improve the Si$_3$N$_4$ by varying Si/N ratio during deposition, post-annealing condition, or imbedding nano particles [4–8].

Several works on deuterium (D$_2$) passivation of Si$_3$N$_4$ with high pressure annealing (HPA) has been also reported. In the conventional CMOS transistors, D$_2$ HPA has been used for the hot carrier reliability [9–11]. HPA is known to enhance the deuterium incorporation at the Si/SiO$_2$ interface, and the deuterium-passivated silicon materials and interfaces are more electrically stable and reliable. In the case of the memory device, Tanaka’s group at Toshiba Corporation has reported that the MONOS devices with the memory window increment and improve reliability by applying D$_2$ treatment in 2002 [12]. With variations in the pressure of D$_2$, they show that D$_2$ annealing can be used to terminate the traps. In 2004–2005, S.M. Choi’s group checked the high temperature (900 °C) D$_2$ annealing effect on the memory device [13,14], and it showed excellent program/erase endurance and a significantly reduced charge loss rate. They focused on D$_2$ annealing to passivate the interface traps between the tunneling oxide and Si substrate. The decreased interface trap was confirmed by the quasi-static capacitance measurement. In 2016, L. Breuill’s group investigated D$_2$ effect on poly-Si channel with trap passivation at the interface between the ONO layer and the poly-Si channel and in the bulk poly-Si [15]. The D$_2$ high pressure...
annealing has been conducted at the last step of the fabrication process. The results show drive current ($I_{\text{ON}}$), subthreshold swing ($SS$) improvement after $D_2$ annealing, which points to a reduction of the defects at the channel and Si-SiO$_2$ interface. Threshold voltage ($V_{\text{TH}}$) is also reduced due to the passivation of negative fixed charges in the ONO stack. However, in this study, retention characteristics seem not to be affected. In 2020, J.M. Yu’s group at Korea Advanced Institute of Science and Technology investigated the high-pressure $D_2$ annealing effects on Gate-All-Around SONOS memory [16]. Maximum transconductance ($g_{\text{m,max}}$), $SS$, and $I_{\text{ON}}$ were extracted, which were improved after $D_2$ annealing. The low-frequency noise (LFN) measurement was used to extract the oxide trap density ($D_{\text{OT}}$) and it was found that the tunneling oxide-channel interface trap decreases by the trap passivation effect of deuterium annealing.

In this study, $D_2$ high pressure annealing (HPA) at low temperature is suggested to suppress the shallow trap formation of Si$_3$N$_4$. Unlike previous research where $D_2$ annealing is applied after the metallization and the analyses are concentrated on the oxide-channel interface traps, the suggested process is applied before the metal deposition and the passivation effect of the traps in silicon nitride is focused on.

During Si$_3$N$_4$ deposition, stoichiometric Si$_3$N$_4$ is formed and nonstoichiometric bonding would be created. In nonstoichiometric bonding, there may be silicon vacancies and nitrogen vacancies, and some studies found out that the Si-O-N bond caused by oxygen diffusion to nitrogen vacancy makes shallow traps [17,18]. The oxygen ions can migrate from the tunneling oxide. The suggested $D_2$ passivation is intended to cure the nitrogen vacancies and suppress the trap generation (similar to the oxygen complex bond). If the deuterium ion occupies the vacancy site, Si-O-N bond cannot be formed even though the oxygen ion migrates. Compared with H$_2$ passivation, $D_2$ passivation can cure defects more stably because deuterium forms stronger bond than hydrogen [19]. Via passivate shallow traps with $D_2$, the memory window can be decreased, but the retention characteristic is expected to improve.

The fabricated devices are programed and then flat band voltage ($V_{\text{FB}}$) is extracted in retention mode at a high temperature via CV measurement. Based on the experimental results, trap energy distribution of Si$_3$N$_4$ is extracted based on the thermal activated retention model. To find out $D_2$ profile and bonding formation in Si$_3$N$_4$, secondary ion mass spectroscopy (SIMS) and Fourier transform infrared spectroscopy (FT-IR) are analyzed. FT-IR spectroscopy is often used to see atomic bonding in materials [20,21] where each atomic bonding absorbs specific wavelength of light. Furthermore, the greatest benefit of FT-IR is its high sensitivity in order to inspect light atoms such as hydrogen and deuterium.

2. Experiments

A metal-nitride-oxide-silicon structure capacitor was fabricated and Figure 1 shows the process flows. Contrary to the SONOS structure, the blocking oxide is skipped to remove the process effect by blocking oxide deposition, which is also preferable for the direct correlation of electrical characteristics with SIMS profile whose sample is nitride/oxide/Si substrate. With p-type silicon substrate, SiO$_2$ for tunneling oxide was grown to 7 nm via dry oxidation. Then, the Si$_3$N$_4$ for CTL was deposited via plasma enhanced chemical vapor deposition (PECVD) with a thickness of 15 nm. Next, $D_2$ high pressure annealing was performed on some samples. $D_2$ 6%/N$_2$ 94% forming gas was used and high-pressure annealing condition was 450 °C, 10 atm. Afterward, post-annealing was done in 600 °C in N$_2$ ambient. Ti 100 nm was deposited via RF sputter for use as a top and bottom gate. Table 1 shows the experimental conditions. The as-deposited sample functions as a reference, and the $D_2$ HPA sample and $D_2$ HPA + post-anneal sample are for testing the temperature effect in $D_2$ treatment. For the electrical analysis, CV was measured using a Hewlett Packard 4284A precision LCR meter. Programming was completed via same program voltage using Hewlett Packard 41501A pulse generator. The thermal activated retention model is used to extract the trap energy distribution of Si$_3$N$_4$ based on the measurement. Physical analyses were also used to support the experiment results. $D_2$ is well
known for possessing a heavier ion than H$_2$, but they both are still very light ions compared with other atoms. Thus, there are not many methods to detect D$_2$ in the silicon nitride layer. In this study, SIMS and FT-IR were used to find out D$_2$ profile and bonding formation in the silicon nitride after the annealing process.

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**Figure 1.** (a) Fabrication process and (b) the cross view of the capacitor-type device with metal nitride oxide silicon (MNOS) structure.

![Fabrication process and capacitor-type device with metal nitride oxide silicon (MNOS) structure.](image)

**Table 1.** Experimental conditions of the post treatment on the silicon nitride, which is performed before the metal deposition.

| As-Deposited | D$_2$ HPA | D$_2$ HPA + Post Anneal |
|--------------|-----------|------------------------|
| D$_2$, 450 °C, 10 atm | × | O | O |
| N$_2$, 600 °C | × | × | O |

3. Results and Discussion

3.1. Electrical Analysis

3.1.1. Memory Window

Figure 2a shows the I-V measurement results of the fabricated devices and shows similar breakdown properties of NO stack independent of annealing conditions. Figure 2b is the CV measurement results at the initial and program state. The maximum capacitance is determined by the nitride/oxide thickness and the values are observed to be similar in all samples, which indicates that the NO thickness is not changed by the annealing condition. The programming pulse width was 0.1 s, and the magnitude was 20 V for one pulse time. Sweep mode with long integration time was used in 1 MHz frequency. Compared with the reference, the device with D$_2$ HPA shows a decreased memory window and this effect was accelerated in one experiment with additional post-annealing. This seems to be the result of trap curing in Si$_3$N$_4$ bulk and interface [22].

3.1.2. Retention Characteristics

Retention properties are measured at various temperatures. The flat band voltage ($V_{FB}$) decrement was measured with CV measurement in retention mode after programming. The retention characteristic was quantified with the percentage of $V_{FB}$ decrease by $V_{FB}$ | program-initial. As shown in Figure 3a, compared with the reference (which shows a 27.53% $V_{FB}$ decrement), the device subjected to D$_2$ HPA exhibits slight improvement, with a 21.37% decrement. Then, additional post-anneal activity makes a significant difference in $V_{FB}$ decrease during retention mode. Figure 3b is a comparison result of charge loss amount at various temperatures, which shows that D$_2$ passivation effects become clearer at higher temperatures. The extracted values are summarized in Table 2.
was calculated by the amount of $V_{FB}$ shift after retention time divided by the memory window. Here, as-dep is a reference device, and $D_2$ HPA is $D_2$ high pressure annealed device at 450 °C and $D_2$ HPA + Post-anneal is $D_2$ high pressure annealed device with post-anneal at 600 °C.

Figure 3. CV measurement results in data retention mode at 30 min after programming. (a) CV shift at 100 °C retention mode; (b) extraction results of charge loss amount (percent) in retention mode at various temperature. Here, charge loss was calculated by the amount of $V_{FB}$ shift after retention time divided by the memory window.

| Temperature | As-dep | $D_2$ HPA | $D_2$ HPA + Post-anneal |
|-------------|--------|-----------|-------------------------|
| 85 °C       | 19.43  | 16.75     | 10.30                   |
| 100 °C      | 27.53  | 21.37     | 10.52                   |
| 125 °C      | 35.65  | 27.65     | 9.84                    |

3.1.3. Trap Energy Level Distribution

Trap energy level of CTL can be extracted by measuring the charge loss through the tunneling oxide. In this experiment, it is assumed that most of the shallow traps are located at or near the interface between $Si_3N_4$ and $SiO_2$ tunneling oxide and the amount of charge
loss through the metal gate can be ignored. To extract the trap density in Si₃N₄, thermal activated retention model is used like follows [23].

\[
\frac{\partial \Delta V_{TH}}{\partial \log(t)} = -2.3k_BTX_N \left( \frac{X_N}{2\varepsilon_N} + \frac{X_{OX}}{\varepsilon_{OX}} \right) g(E_{TA}) 
\]

(1)

\[
E_{TA} = k_BT \ln \left( \frac{A}{T} \right)
\]

(2)

\[
A = 2\sigma_n \left[ \frac{3k_B}{m^*} \left( \frac{2\pi m^* k_B}{\hbar^2} \right)^{3/2} \right]
\]

(3)

Equation (1) shows the charge decay model in relation to \( V_{TH} \) shift according to time at specific temperature. \( E_{TA} \) is the energy level expressed like Equation (2). In Equation (3), \( \sigma_n \) is the capture cross-section and \( m^* \) is the effective mass of electron in the silicon nitride.

Measurements were conducted at 85 °C.

Figure 4a shows the extracted energy distribution of trap in each process condition based on the experimental results of charge loss according to the retention time as shown in Figure 4b. The results show that D₂ passivation reduces the amount of trap densities in the band gap range of 1.06 eV~1.18 eV, and this suppression seems to be reinforced with post-annealing. This result explains the program window reduction in D₂ HPA, as mentioned before.

![Figure 4](image)

Figure 4. (a) Trap energy level distribution is Si₃N₄ according to the post treatment. (b) Measurement results of charge loss according to the retention time at 85 °C. The extraction is based on thermal activated retention model.

3.2. Physical Analysis

3.2.1. Secondary Ion Mass Spectroscopy

SIMS can be used to find out the D₂ profile in Si₃N₄ [24,25]. The selected elements Si, O, N, D, and depth profiles were obtained with a commercial SIMS instrument (CAMECA IMS 7f). The primary ions were 6 keV Cs⁺ at 10 nA and raster into a 250 μm × 250 μm with a detected area of 63 μm in diameter. Figure 5 shows the SIMS profile results for as-deposited silicon nitride and D₂ passivated Si₃N₄, including the post-anneal process. As-deposited Si₃N₄ has a negligible quantity of deuterium, but in the sample treated with D₂ high pressure annealing, it can be seen that deuterium exists from the surface side. Furthermore, with additional post-annealing, it was confirmed that deuterium diffuses into the Si₃N₄ and exists up to the Si₃N₄-SiO₂ tunneling oxide interface region. It is possible that deuterium can be dissociated during the post-annealing period, but the SIMS results indicate that deuterium affects silicon nitride property during N₂ 600 °C anneal. That is, even if some injected deuterium could dissociate and diffuse out to air at 600 °C, some could diffuse...
into the layer and form bondage with Si and N atoms. Furthermore, previous research had conducted D\textsubscript{2} high pressure annealing even at 900 °C [12]. This result supports our theory as why V\textsubscript{FB} in the initial state is shifted to the left and the memory window decreases.

3.2. Physical Analysis

3.2.1. Secondary Ion Mass Spectroscopy

SIMS can be used to find out the D\textsubscript{2} profile in Si\textsubscript{3}N\textsubscript{4} [24,25]. The selected elements Si, O, N, D, and depth profiles were obtained with a commercial SIMS instrument (CAMECA IMS 7f). The primary ions were 6 keV Cs\textsuperscript{+} at 10 nA and raster into a 250 μm × 250 μm with a detected area of 63 μm in diameter. Figure 5 shows the SIMS profile results for as-deposited silicon nitride and D\textsubscript{2} passivated Si\textsubscript{3}N\textsubscript{4}, including the post-anneal process. As-deposited Si\textsubscript{3}N\textsubscript{4} has a negligible quantity of deuterium, but in the sample treated with D\textsubscript{2} high pressure annealing, it can be seen that deuterium exists from the surface side. Furthermore, with additional post-annealing, it was confirmed that deuterium diffuses into the Si\textsubscript{3}N\textsubscript{4} and exists up to the Si\textsubscript{3}N\textsubscript{4}-SiO\textsubscript{2} tunneling oxide interface region. It is possible that deuterium can be dissociated during the post-annealing period, but the SIMS results indicate that deuterium affects silicon nitride property during N\textsubscript{2} 600 °C anneal. That is, even if some injected deuterium could dissociate and diffuse out to air at 600 °C, some could diffuse into the layer and form bondage with Si and N atoms. Furthermore, previous research had conducted D\textsubscript{2} high pressure annealing even at 900 °C [12]. This result supports our theory as why V\textsubscript{FB} in the initial state is shifted to the left and the memory window decreases.

(a)

(b)

(c)

Figure 5. SIMS profile of N, O, Si, D in (a) as-deposited silicon nitride; (b) D\textsubscript{2} high pressure annealed silicon nitride; (c) D\textsubscript{2} high pressure anneal with post-annealing silicon nitride.

3.2.2. Fourier Transform InfraRed Spectroscopy

To analyze the change in atomic bonding in Si\textsubscript{3}N\textsubscript{4}, it is needed to detect the deuterium bonding. In FT-IR, each bonding absorbs specific wavelength of Infrared light and the results don’t affect each other. The analysis can be employed for detecting and determining bond densities of light atoms such as H\textsubscript{2} or D\textsubscript{2}. In 2008, G. Scardera investigated high temperature annealing effect on silicon-rich silicon nitride films using FT-IR spectroscopy [20]. Si-H bonding is detected by FT-IR measurement, allowing for investigation of changes in bonding ratio after annealing process. In 1995, Z. Lu’s group also used FT-IR spectroscopy to check the RTA effect on a-Si:N:H(D) films, where Si-H and Si-N-H bonds are detected and Si-D and Si-N-D peaks are also detected [21].

In this experiment, FT-IR spectroscopy is applied to find out the D\textsubscript{2} passivation effect on silicon nitride bonding structure. Figure 6 shows the results of FT-IR spectroscopy on Si\textsubscript{3}N\textsubscript{4} with D\textsubscript{2} passivation. A Thermo-Nicolet 5700 FT-IR spectrometer was used. With reference to previous studies, the range of the SiN-D peak is around 2400 cm\textsuperscript{-1}. As shown in Figure 6, the sample with D\textsubscript{2} HPA with 600 °C annealing shows slightly increased absorbance in the rage of 2375 cm\textsuperscript{-1}. Considering the difficulty of detecting the light atoms (such as H\textsubscript{2} or D\textsubscript{2}), more precise physical method should be studied.
4. Conclusions

In this study, the effects of D2 HPA on Si3N4 are investigated in MNOS-type flash memory device. To focus on silicon nitride’s trap control, D2 passivation is conducted directly on Si3N4 films before metal deposition. The results show the memory window decreased after D2 passivation, but the charge loss in retention mode after the program is suppressed, which becomes clearer as temperature increases. The D2 passivation effect seems to be reinforced with post-annealing. Trap energy distribution based on the thermal activated retention model is also extracted to compare the trap density. The results show that D2 passivation reduces the amount of trap densities in the band gap range of 1.06 eV–1.18 eV. SIMS and FT-IR spectroscopy are also applied to find out the deuterium profile and bond structure in Si3N4. SIMS results show that deuterium diffuses into the Si3N4 and exists up to the Si3N4-SiO2 tunneling oxide interface region, which demonstrates the possibility of the deuterium passivation of shallow traps near Si3N4 and SiO2 interface.

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References
1. Qin, S.; Jiang, Z.; Li, H.; Fujii, S.; Lee, D.; Wong, S.S.; Wong, H.S.P. Next-generation ultrahigh-density 3D vertical resistive switching memory (VRSM)-Part I: Accurate and Computationally Efficient Modeling. IEEE Trans. Electron Devices 2019, 66, 5139–5146. [CrossRef]
2. Endoh, T.; Honjo, H.; Nishioka, K.; Ikeda, S. Progresses in STT-MRAM and SOT-MRAM for Next Generation MRAM. In Proceedings of the 2020 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 16–19 June 2020.
3. Ishimaru, K. Challenges of flash memory for next decade. In Proceedings of the 2021 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 23 January 2021.
4. Chen, T.S.; Wu, K.H.; Chung, H.; Kao, C.H. Performance improvement of SONOS memory by bandgap engineering of charge-trapping layer. IEEE Electron Device Lett. 2004, 25, 205–207. [CrossRef]
5. Wang, S.Y.; Lue, H.T.; Lai, E.K.; Yang, L.W.; Yang, T.; Chen, K.C.; Gong, J.; Hsieh, K.Y.; Liu, R.; Lu, C.Y. Reliability and processing effects of bandgap engineered SONOS (BESONOS) flash memory. In Proceedings of the 2007 IEEE International Reliability Physics Symposium Proceedings 45th Annual, Phoenix, AZ, USA, 1–19 April 2007.
6. Kim, H.D.; An, H.M.; Kim, K.C.; Seo, Y.J.; Kim, T.G. Influence of post-annealing on the electrical properties of metal/oxide/silicon nitride/oxide/silicon capacitors for flash memories. *Semicond. Sci. Technol.* 2008, 23, 075046. [CrossRef]

7. Lim, J.G.; Yang, S.D.; Yun, H.J.; Jung, J.K.; Park, J.H.; Lim, C.; Cho, G.S.; Park, S.G.; Huh, C.; Lee, H.D.; et al. High performance SONOS flash memory with in-situ silicon nanocrystals embedded in silicon nitride charge trapping layer. *Solid-State Electron.* 2018, 140, 134–138. [CrossRef]

8. Furnemont, A.; Zahid, M.B.; Degraeve, R.; Breuil, L.; Cacciato, A.; Rothschild, A.; Olsen, C.; Ganguly, U.; Van Houdt, J. Nitride engineering for improved erase performance and retention of TANOS NAND Flash memory. In Proceedings of the 2008 Joint Non-Volatile Semiconductor Memory Workshop and International Conference on Memory Technology and Design, Opio, France, 18–22 May 2008.

9. Chasin, A.; Franco, J.; Bury, E.; Ritzenhaler, R.; Litta, E.; Spessot, A.; Horiguchi, N.; Linten, D.; Kaczer, B. Relevance of fin dimensions and high-pressure anneals on hot-carrier degradation. In Proceedings of the 2020 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 28 April–30 May 2020.

10. Park, J.Y.; Yoo, T.J.; Yu, J.M.; Lee, B.H.; Choi, Y.K. Impact of Post-Metal Annealing WITH Deuterium or Nitrogen for Curing a Gate Dielectric Using Joule Heat Driven by Punch-Through Current. *IEEE Electron Device Lett.* 2020, 42, 276–279. [CrossRef]

11. Lee, J.; Cheng, K.; Chen, Z.; Hess, K.; Lyding, J.W.; Kim, Y.K.; Lee, H.S.; Kim, Y.W.; Suh, K.P. Application of high pressure deuterium annealing for improving the hot carrier reliability of CMOS transistors. *IEEE Electron Device Lett.* 2000, 21, 221–223.

12. Tanaka, M.; Saida, S.; Mitani, Y.; Mizushima, I.; Tsunashima, Y. Highly reliable MONOS Devices with optimized silicon nitride film having deuterium terminated charge traps. In Proceedings of the Digest International Electron Devices Meeting, San Francisco, CA, USA, 8–11 December 2002.

13. Choi, S.; Baek, S.; Jang, M.; Jeon, S.; Kim, J.; Kim, C.; Hwang, H. Effects of High-Pressure Deuterium annealing on nonvolatile memory device with silicon nanocrystals embedded in silicon nitride. *J. Electrochem. Soc.* 2005, 152, G345. [CrossRef]

14. Choe, S.; Jang, M.; Park, H.; Hwang, H.; Jang, J.; Kim, C. High-pressure deuterium annealing for improving the reliability characteristics of silicon-oxide-nitride-oxide-silicon nonvolatile memory devices. *Appl. Phys. Lett.* 2004, 85, 6415–6417. [CrossRef]

15. Breuil, L.; Lisoni, J.G.; Delhougne, R.; Tan, C.L.; Van Houdt, J.; Furnemont, A. Improvement of poly-Si channel vertical charge trapping NAND devices characteristics by high pressure D$_2$/H$_2$ annealing. In Proceedings of the 2016 IEEE 8th International Memory Workshop (IMW), Paris, France, 15–18 May 2016.

16. Yu, J.M.; Park, J.Y.; Yoo, T.J.; Han, J.K.; Yun, D.H.; Lee, G.B.; Hur, J.; Lee, B.H.; Kim, S.Y.; Lee, B.H.; et al. Quantitative analysis of high-pressure Deuterium annealing effects on vertically stacked Gate-All-Around SONOS memory. *IEEE Trans. Electron. Devices* 2020, 67, 3903–3907. [CrossRef]

17. Schmidt, J.; Schuurmans, F.M.; Sinke, W.C.; Glunz, S.W.; Aberle, A.G. Observation of multiple defect states at silicon-silicon nitride interfaces fabricated by low-frequency plasma enhanced chemical vapor deposition. *Appl. Phys. Lett.* 1997, 71, 252–254. [CrossRef]

18. Perera, R.; Ikeda, A.; Hattori, R.; Kuroki, Y. Effects of post annealing on removal of defect states in silicon oxynitride films grown by oxidation of silicon substrates nitride in inductively couple nitrogen plasma. *Thin Solid Films.* 2003, 423, 212–217. [CrossRef]

19. Hess, K.; Kizilyali, I.C.; Lyding, J.W. Giant Isotope Effect in Hot Electron Degradation of Metal Oxide Silicon Devices. *IEEE Trans. Electron Devices* 1998, 45, 406–416. [CrossRef]

20. Scardera, G.; Puzzer, T.; Conibeer, G.; Green, M.A. Fourier transform infrared spectroscopy of annealed silicon-rich silicon nitride thin films. *J. Appl. Phys.* 2008, 104, 104310. [CrossRef]

21. Lu, Z.; Santos-Filho, P.; Stevens, G.; Williams, M.J.; Lucovsky, G. Fourier transform infrared study of rapid thermal annealing of aSi$_x$N$_{1-x}$H(D) films prepared by remote plasma enhanced chemical vapor deposition. *J. Vac. Sci. Technol. A Vac. Surf. Film.* 1995, 13, 607–613. [CrossRef]

22. Sandhya, C.; Ganguly, U.; Singh, K.K.; Singh, P.K.; Olsen, C.; Seutter, S.M.; Hung, R.; Conti, G.; Ahmed, K.; Krishna, N.; et al. Nitride Engineering and the effect of interfaces on charge trap flash performance and reliability. In Proceedings of the 2008 IEEE International Reliability Physics Symposium, Phoenix, AZ, USA, 27 April–1 May 2008.

23. Yang, Y.L.; White, M.H. Charge retention of scaled SONOS nonvolatile memory devices at elevated temperatures. *Solid-State Electron.* 2000, 44, 949–958. [CrossRef]

24. Chang, M.; Hasan, M.; Jung, S.; Park, H.; Jo, M.; Choi, H.; Hwang, H. Impact of high-pressure deuterium oxide annealing on the blocking efficiency and interface quality of metal-alumina-nitride-oxide-silicon-type flash memory devices. *Appl. Phys. Lett.* 2007, 91, 192111. [CrossRef]

25. Carlson, D.E.; Magee, C.W. A SIMS analysis of deuterium diffusion in hydrogenated amorphous silicon. *Appl. Phys. Lett.* 1978, 33, 81–83. [CrossRef]