Performance Analysis of 5:2 compressor with 58 transistors

Kothakonda Durga Bhavani¹, R Sireesha², Kongala Raju¹, Ganesh Kumar M⁴, Ratala Koteswara Naik³, Sanam Nagedram⁶
¹,⁶Koneru Lakshmaiah Education Foundation (KLEF), Vaddeswaram, A.P
³GPREC, Kurnool, A.P
²,⁴ SVREC, Nandyal, A.P
⁵Loyola institute of engineering and technology, A.P
durga.ece@kluniversity.in

Abstract: In the present generation of VLSI domain, designing a circuit with less power, area, and delay has become challenge for every designer. In this article we have design and implemented a design for 5:2 compressor which is the vital component in CMOS multiplier circuits. The proposed compressor circuit design requires less transistor count i.e. 58 transistors. The Simulation results of proposed 5:2 compressor has substantially expanded the performance of power delay in contrast to earlier designs.

Keywords: Compressor, Full adder, Multiplexer(MUX)

1 Introduction
Increased usage of electronic devices demand VLSI design with improved power delay characteristics which leads to design of fast and efficient systems. In processors multiplication is a very regular and critical operation. The speed is a part which shows how hastily the processors can function [2]. Basically, the multiplication process consists of three stages[3-9]. The second stage furnish more power, area and also delay in giant multipliers, so enhancing in this domain is deemed essential[6-8].

Compressors are used that the number of operands is reduced while performing addition operation with the partial products, while doing the multiplication operation. So, the stage which is used to reduce partial products can be efficaciously applied with the trees of compressor circuit. The basic building blocks of compressor tree are 4:2 and 5:2 compressors. By designing efficient compressor, hence the multiplier performance will increase. Earlier designers have designed many different compressors like 3:2, 4:2, 4:3, 5:2, 5:3, 6:3, 7:3 etc [5, 6, 9, 10]. Several publications have proposed the various designs for a 5by2 compressor with exclusive construction and overall design performance trade-offs [3-13]. In this paper we are presenting a CMOS 5by2 compressor using a smaller number of transistors and also the performance has been analysed with different parameters.

2 COMPRESSORS
The compressor consists of a one-bit adder circuit, in which more than 3 inputs and a smaller number of outputs.

The 5 by 2 compressor adds five primary inputs in addition with two carry inputs Cin1 and Cin2 totally it receives 7 inputs. For the first 5:2 compressor the carry inputs can be taken as zero otherwise these carry inputs can be decided by the previous stage carry outputs[1-7]. The output of compressor is Sum, Carry and two carry outputs which can be taken as the carry and used as inputs for the next stage 5:2 compressor. In the diagram S indicates sum and C indicates carry.

![Figure 1](image1.png)

**Figure 1** Circuit diagram for the 5:2 Compressor

The function of 5 by 2 compressor is expressed by:

\[ A1 + A2 + A3 + A4 + A5 + Cin1 + Cin2 = S + 2 \times (Cu1 + Cu2 + Carry) \]  \( \text{(1)} \)

![Figure 2](image2.png)

**Figure 2.** Circuit diagram of 5-2 compressor with full adders

compressor which use the cascade connection of three full adders [2-10]. Generally, a full adder consists of three inputs (A, B, Cin) and generate two outputs (Sum\text{\textsubscript{FA}}, Carry\text{\textsubscript{FA}}), which can be expressed by using the following Boolean functions.

\[ \text{Sum} = A \text{xor} B \text{xor} C_in \]  \( \text{(2)} \)
\[
\text{Carry}_{FA} = (A \oplus B) \cdot C_{in} + (A \oplus B)^{'} \cdot A \quad (3)
\]

Similarly, by applying “(2)” and “(3)” to the conventional implementation of 5:2 compressor as shown in Fig. 2, the following Boolean expressions can be analyzed.

\[
\begin{align*}
C_{u1} &= (A_1 \oplus A_2) \cdot A_3 + (A_1 \oplus A_2)^{'} \cdot A_1 \\
C_{u2} &= (A_1 \oplus A_2 \oplus A_3 \oplus A_4) \cdot C_{in1} + (A_1 \oplus A_2 \oplus A_3 \oplus A_4)^{'} \cdot A_4 \cdot A_5 \cdot C_{in2} \cdot C_{in3} \cdot A_5 \\
S &= A_1 \oplus A_2 \oplus A_3 \oplus A_4 \oplus A_5 \oplus C_{in1} \oplus C_{in2} \cdot A_5 \\
C &= (A_1 \oplus A_2 \oplus A_3 \oplus A_4 \oplus A_5 \oplus C_{in1}) \cdot C_{in2} + (A_1 \oplus A_2 \oplus A_3 \oplus A_4 \oplus A_5 \oplus C_{in1})^{'} \cdot A_5 \cdot C_{in2} \cdot C_{in3} \cdot A_5
\end{align*}
\]

The above implementation is not very efficient, because it has six gate delays in critical path to generates sum and carry outputs. It requires more transistors for implementation and requires more area, power consumption. In many architectural designs have been proposed, using different logics [1-9].

3 PROPOSED CIRCUIT

A circuit design of the proposed 5 by 2 compressors is shown in below figure 3. The design consists of xor gates and multiplexer blocks. There are six 2 input XOR gates and 3 multiplexer blocks with 2 inputs and 1 output. Fig.3 shows generalized schematics of XOR and MUX blocks. This compressor circuit is characterized by [6]-[8], similar to the conventional one.

![Fig.3 proposed 5:2 compressor](image-url)
The circuit which adds three inputs and gives output as sum and carry is designed by using two XOR gates and a 2 by 1 MUX. These all the cells are arranged to get a smaller critical path with four gate delays to get final sum and carry outputs, where existing design requires six gate delays.

4 Experimental Results

The simulation is performed by using Tanner EDA at 250nm technology. The transistor level implementation is entered in S-Edit which is schematic entry tool in Tanner EDA. After schematic entry the simulation is done in T-SPICE which is used to measure the consumption of power and delay. After running the schematic in T-SPICE the waveform will be viewed in W-Edit in Tanner EDA which is the waveform viewer.

The transistors used in the implementation has equal length i.e for PMOS $L_p=0.25\mu m$ and for NMOS $L_n=0.25\mu m$. And transistor width also equally sized i.e for PMOS $W_p=2.50\mu m$ and for NMOS $W_n=2.50\mu m$. We include some inverters for the simplicity of circuit. In previous methods [4,9] they used only pass transistors which increased the transistor count greater than original method.
Fig. 4a Simulation Results

Fig. 4b Simulation Results-Inputs
5 COMPARISON

The Table below shows the comparison between different types of compressor circuits with respect to number of transistors, power, delay and power delay product depends on technology. Power is calculated by adding all the average powers and divided with number of sources. Total delay is given directly. Power delay product is calculated by multiplying power and delay. The power is given in terms of nanowatts(nW), delay in terms of picoseconds(ps) and PDP is in terms of attojoules(aJ). The proposed method giving good results compared to previous methods. The proposed method has less transistor count, better power, delay and PDP compared to other designs.

| 5:2 compressor | Technology (nm) | Transistors | Power (nW) | Delay (ps) | PDP (aJ) |
|----------------|-----------------|-------------|------------|------------|----------|
| Proposed       | 250             | 58          | 3239       | 455        | 1318     |
| [1]2001        | 350             | 76          | 5510       | 624        | 3438     |
| [2]2004        | 180             | 76          | 3987       | 352        | 1403     |
| [3]2014        | 90              | 78          | 4519       | 518        | 2341     |
| [4]2018        | 90              | 82          | 5045       | 329        | 1660     |
| [5]2007        | 180             | 90          | 6184       | 515        | 3185     |
| [6]2013        | 180             | 94          | 3375       | 450        | 1519     |

Table 1. Comparison Table

6 CONCLUSION
In this paper, we presented a new plan for 5:2 compressor using transmission gate full swing outputs with 58 transistor which is the lowest transistor count compared to previously designed circuits. According to the simulation results, it attains acceptable power delay results and contrast to earlier designs. It has very good performance in all simulated conditions. The new design of 5:2 compressor can be used as competent adder circuit for the fast multiplication.

REFERENCES

[1] ‘Low-power 4-2 and 5-2 compressors’ by Prasad, K., and Parhi, K.K.
[2] Ultralow-voltage low-power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits by Chang, C.H., Gu, J., and Zhang, M.
[3] ‘Low-power and high-performance 5:2 compressors’ by Najafi, A., Najafi, A., and Mirzakhani, A.
[4] ‘High-speed energy-efficient 5:2 compressor’ by Najafi, A., Timarchi, S., and Najafi, A.
[5] ‘Novel architectures for high-speed and low-power 3-2, 4-2 and 5-2 compressors’ by Veeramachaneni, S., Krishna, K.M., Avinash.
[6] ‘CMOS implementation of a new high speed, glitch-free 5-2 compressor for fast arithmetic operations’ by Tohidi, M., Mousazadeh, M., Akbari, S.
[7] Murali Krishna B., Madhumati G.L., Khan H., "FPGA based pseudo random sequence generator using XOR/XNOR for communication cryptography and VLSI testing applications", International Journal of Innovative Technology and Exploring Engineering, Vol No:8, Issue No:4, 2019, pp: 485-494.
[8] Naga Lakshmi Prasanna K., Murali Krishna B., Sadiya Shireen S.K., Poorna Chander Reddy A., "FPGA based convolutional encoder for GSM-900 architecture", International Journal of Innovative Technology and Exploring Engineering, Vol No:8, Issue No:4, 2019, pp: 642-650.
[9] SarathChandraK. HariKishore.,"Physical design implementation of high performance CMOS dynamic latch comparator",2018,Journal of Engineering and Applied Sciences ,Vol: 13 ,Issue: 11 ,pp: 4099-4103
[10] KumarM.S., TulasiS.K., SrinivasuluN., BandiV.L., KishoreK.H.," Bit wise and delay of vedic multiplier “, 2018, International Journal of Engineering and Technology(UAE), Vol: 7, Issue: 27, pp: 651 - 654.
[11] Siva Kumar M., Syed Shameen S., Raghu Sai M.N.V., Nikhil D., Kartheek P., Hari Kishore K., “Efficient and low latency turbo encoder design using Verilog-Hdl “, 2018, International Journal of Engineering and Technology(UAE),Vol: 7, Issue:27, pp: 609-612
[12] Kumar M.S., Tulasi S.K., Srinivasulu N., Yedla G.S.K.N., Raghuvir E., Kishore K.H.,” Improvement of the efficiency of booth multiplier “, 2018, International Journal of Engineering and Technology(UAE), Vol: 7, Issue:34, pp: 316-322
[13] Murali A., Hari Kishore K., “Integrated and effective in-system debugging approach in FPGA circuits “, 2018, Journal of Advanced Research in Dynamical and Control Systems, Vol: 10, Issue: 7, pp: 1818-1826.
[14] LagadapatiN., KarriM.,VaddineniT.,SubhaniM.,HariKishoreK.,” A VLSI implementation of elevator control based on finite state machine using Verilog HDL “, 2018, Smart Innovation,Systems and Technologies ,Vol: 78 ,pp: 75-83