Energy Efficient VLSI Design on FPGA using Capacitance Scaling Technique

Gasim Alandjani*, Altaf H. Bouk¹, Tanesh Kumar², S. H. A. Musavi² and Manoj Kumar³

¹Department of Information and Computer Technology, Yanbu University College (YUC), Yanbu, Saudi Arabia; alandjanig@rcyci.edu.sa, bouka@rcyci.edu.sa
²Faculty of Engineering, Sciences and Technology, Indus University, Karachi, Pakistan; tanesh.kumar@indus.edu.pk, dean@indus.edu.pk
³Department of Computer Science, Muhammad Ali Jinnah University, Karachi, Pakistan; m_kumar@jinnah.edu

Abstract

In medical sciences and particular in cardiology related area, ECG machine is considered a basic equipment to get the fundamental knowledge about proper functioning of heart. In this work the aim is to make energy efficient ECG machine design on FPGA using capacitance scaling technique while the device is operating under various WLAN specific frequencies. Concept of internet of things is used in this work by adding additional 128-bit IPv6 address in the input of ECG machine that will use to control the device via internet. Kintex-7 is used from the FPGA family for this task. It is analyzed that 89.15%, 89.75% and 89.81% power reduction can be achieved under device operating frequencies 0.9 GHz, 2.4 GHz and 3.6 GHz respectively when the capacitance is taken 500 pF in place of 5000 pF.

Keywords: Capacitance Scaling, ECG Machine, FPGA, Internet of Things (IoT), Total Power

1. Introduction

Internet of Things (IoT) is a new trend of modern era comprising of all computing aspects including smart, powerful and low power or efficient computing. It makes devices interact with each other from remote areas, generally utilizes Wireless Sensor Networks (WSN) technologies for wearable handheld devices to extract appropriate information for analysis and processing, features real time monitoring. IoT covers wide range of domains like bio-medical, aerospace aviation, agriculture, education, manufacturing and so on and its rate is upstaging day by day. Much recent technological advancement has put positive impact in the area of healthcare. Now devices are aiming to be more powerful gradually, sensor technology has been emerged and serving as a salient component in different fields comprises medical science, various acquisitions were already proposed to design an eco friendly (i.e., environment friendly) Electrocardiograph (ECG) health monitoring system for self and remote diagnostics, which will monitor an individual’s heartbeat regularity and potential on runtime. Devices like ECG monitoring shirt and wearable are available easily in the marketplace, operated via android, iOs and windows phone devices and its information is kept on cloud. ECG interprets the heart’s electrical functioning into tracings on a paper, where dips and spikes in the line tracings are called waves. An ECG system records the potential and clocking of electrical signals as they have been passed through the heart, brawn the heart rhythm and rate respectively. Certain cardiac disorders cannot be evaluated by ECG, diagnosing those disorders, angiography and echocardiography is done on subjects according to the need. ECG is considered as a representative indication of cardiac physiology, bit useful in diagnosing cardiovascular disorders. Arrhythmia detection and its classification is a vital necessity in clinical cardiology, peculiarly when executed in real time. In order to design an ECG monitoring system efficiently, health care professionals and computer technologists are fronting up with challenges like scalability, real time data collection, accurate measurements, less energy efficiency,
noise and availability of data for both patients and doctors etc. Various analysis have addressed the integration of mobile and cloud computing to examine the ECG data for testing. Arise some challenges of traditional computing and service models and addresses related issues. Several designs are also implemented on HDL Verilog Language and FPGA Field Programmable Gate Arrays, relatively are of low cost, step-up the productivity tends to spotlight the flaws of ECG on a wireless transmission system embedded on a FPGA chip. Recently IoT based analysis is examined in various FPGA devices to design diverse devices for various applications. As the number of IoT devices are increasing rapidly, results the need to build a smart world of devices with less human influence. General idea of IoT is to assign an IP address to a relative device to be pinged out from remote distance, widely used for real time data collection. In this work we are also implementing our ECG machine design on FPGA and making it IoT enable. In this work ECG machine is operated under following frequency standard of WLAN (Wireless Local Area Network). Power is measured in milli Watt.

Table 1. List of WLAN channels

| Channels | Operating Frequency (MHz) |
|----------|--------------------------|
| ah       | 900                      |
| b/g/n    | 2,400                    |
| y        | 3,600                    |
| a/h/j/n/ac | 4,900                |
| p        | 5,900                    |

Reliability of target design ECG machine can be tested through this process. By this we can connect the target device through WLAN frequency channels and perform communication through these channels.

2. Literature Review

The work in1 highlights remote ECG health monitoring systems that acquire data from heterogeneous sort of biomedical sensors, transmits to gateway via appropriate channel. Transmission itself experiences inefficient power intake and network traffic issues. Proposed a low complex rule system grounded on health care systems acquisitions and smart data transmission architecture, Used 3 Lead Data Acquisition architecture for accumulation of data and IEEE 802.15.4 standard to transmit data on server, Implemented on Spartan-3E FPGA Power Consumption and network consequences been resolved by adapting event based transmission instead of continuous transmission, resulting it to be a positive perspective for IOT systems. The work in2 describes the significance of Signal Processing in bio-medical engineering and elaborate it's advancements for amendment monitoring of patients through ECG systems, utilized digital filters for noise reduction intent, followed by a comparison between FIR and IIR filters to reduce the artifacts, concludes with some advantages of FIR over IIR. The work in3 highlights the contiguous growth of computing to reduce noise and other artifacts from ECG signals, using nondecimated Wavelet Transform UWT, Projects some algorithms having more appropriate and reproducible results on wavelet domain over other conventional algorithms in a user friendly Graphical User Interface (GUI). Multiple heterogeneous approaches are given in4 in order to withdraw Baseline noise from ECG signals. Several filtering methods are analyzed to drill down the Baseline Wandering generally characterized as non-adapting and adapting filtering, observed aspects and outcomes and recommended wavelet adaptive filtering approach for baseline reduction. Long-term health monitoring and harmful consequences detection using developed wearable sensor devices advancing Wireless Sensor Networks (WSN) in health care applications is discussed in5, have ability for real time analysis and decision making, He proposed that ECG is a fundamental parameter approach assessing a human’s health status, demanding broad analysis, asserting full coveted functionality. Flash based Field Programmable Gate Array (FPGA) is utilized for smart and power efficient biological signal processing and to develop a conciliatory and inconspicuous device to extract appropriate data. FPGA have some advantages over microcontrollers is the parallel execution for power minimization using slow system clock, proposed a design of two-channel ECG system to get continuous data analysis. Actel’s Flash FPGA, ProASIC3 transformed into power effective IGLOO’s FPGA, incorporates a 12 BIT ADC, oscillator and flash storage for device configuration. In the work in6 author highlight the technology trend of Artificial Neural Networks (ANN) and presented a FPGA stationed ECG signal classified in to parallel genetic algorithm and block based neural network system appropriate for hardware implementation to get portability and ECG signals for long extent monitoring. Proposed architecture for Black Based neural Networks (BBNN) and EC-CGA and concluded with a comparison and deliver some advantages of BBNN over EC-CGA, practiced often when Wavelet Transform is occupied to
accumulate features, represents a proof concept design for ECG smart monitoring systems. Various IO standard have been used in order to design low power VLSI design on different FPGAs.

### 3. Capacitance Scaling for ECG machine

ECG machine can give more efficiency with the variation of capacitance and it is directly proportional to the power. For the particular reason, capacitance scaling technique is used in this work. Four different types of capacitance are taken into the account that includes 5000 pF, 500 pF, 50 pF and 5 pF.

![Top level schematic of ECG machine.](image1)

Figure 1. Top level schematic of ECG machine.

Figure 1 shows top level schematic of ECG machine which contains 128-bit IPv6 address by which we can control the target device through internet. Other inputs include clock, Left Foot (LL) and Right Arm (RA). The output contains LEADII.

### 3.1 Power Consumption using Capacitance Scaling at 0.9GHz

IO power imposes a great impact on overall power of the target device. By scaling down the capacitance of target design from 5000 pF to 5 pF, IO power is reduced up to 98.72% and Quiescent power is reduced up to 30.76% under the frequency 0.9 GHz as shown in Table 2 and Figure 2.

![Power consumption using capacitance scaling at 0.9 GHz.](image2)

**Table 2.** Power consumption using capacitance scaling at 0.9GHz

| Frequency (GHz) | 5000 pF | 500 pF | 50 pF | 5 pF |
|----------------|---------|--------|-------|------|
| IO Power       | 7,195   | 737    | 91    | 26   |
| Quiescent Power| 65      | 47     | 45    | 45   |
| Overall Power  | 7,265   | 788    | 141   | 76   |

### 3.2 Power Consumption using Capacitance Scaling at 2.4GHz

Quiescent power is also known as static power and its consumptions are one of the major issues in energy efficient VLSI design for reconfigurable devices like FPGA. In this case when the WLAN frequency is taken as 2.4 GHz, the reduction in Quiescent power become 91.72% with shifting of capacitance from 5000 pF to 5 pF.

![Power consumption using capacitance scaling at 2.4 GHz.](image3)

**Table 3.** Power consumption using capacitance scaling at 2.4GHz

| Frequency (GHz) | 5000 pF | 500 pF | 50 pF | 5 pF |
|----------------|---------|--------|-------|------|
| IO Power       | 38,980  | 3,988  | 489   | 139  |
| Quiescent Power| 570     | 55     | 46    | 46   |
| Overall Power  | 39,562  | 4,055  | 547   | 197  |

### 3.3 Power Consumption using Capacitance Scaling at 3.6GHz

By replacing capacitance of target device from 5000 pF to 500 pF, IO power of is reduced up to 89.76% and Quiescent power is reduced up to 93.85% under the
WLAN frequency 3.6 GHz as shown in Table 4 and Figure 4.

**Table 4.** Power consumption using capacitance scaling at 3.6 GHz

|            | 3.6 GHz | 5000 pF | 500 pF | 50 pF | 5 pF |
|------------|---------|---------|--------|-------|------|
| IO Power   | 58,471  | 5,983   | 737    | 209   |      |
| Quiescent Power | 993   | 61      | 47     | 46    |      |
| Overall Power | 59,482 | 6,061   | 798    | 272   |      |

Figure 4. Power consumption using capacitance scaling at 3.6 GHz.

### 3.4 Power consumption using capacitance scaling at 4.9GHz

In Table 5 and Figure 5, when the ECG machine is operating on a frequency of 4.9 GHz and capacitance is taken as 50 pF in place of 500 pF, there is 87.73% reduction in IO power and 31.88% reduction in Quiescent power.

**Table 5.** Power consumption using capacitance scaling at 4.9GHz

|            | 4.9 GHz | 5000 pF | 500 pF | 50 pF | 5 pF |
|------------|---------|---------|--------|-------|------|
| IO Power   | 79,585  | 8,143   | 999    | 284   |      |
| Quiescent Power | 993   | 69      | 47     | 46    |      |
| Overall Power | 80,602 | 8,236   | 1,070  | 354   |      |

Figure 5. Power consumption using capacitance scaling at 4.9 GHz.

### 3.5 Power consumption using capacitance scaling at 5.9 GHz

IO power can be saved up to 71.54% and Quiescent power can be saved up to 4.16% when the capacitance is 5 pF in place of 50 pF and the device is operating at WLAN frequency 5.9 GHz as shown in Table 6 and Figure 6.

**Table 6.** Power consumption using capacitance scaling at 5.9 GHz

|            | 5.9 GHz | 5000 pF | 500 pF | 50 pF | 5 pF |
|------------|---------|---------|--------|-------|------|
| IO Power   | 95,827  | 9,805   | 1,202  | 342   |      |
| Quiescent Power | 993   | 76      | 48     | 46    |      |
| Overall Power | 96,849 | 9,910   | 1,279  | 417   |      |

Figure 6. Power consumption using capacitance scaling at 5.9 GHz.

### 3.6 Comparison of power reduction at different WLAN frequencies

The Table 7 shows the comparison of total power reduction of ECG machine operating at different WLAN frequencies with different capacitances. It is observed that by replacing device capacitance from 5000 pF to 500 pF, total power is reduced by 89.15%, 89.75%, 89.81%, 89.78% and 89.76% for the device operating WLAN frequencies 0.9 GHz, 2.4 GHz, 3.6 GHz, 4.9 GHz and 5.9 GHz respectively.

**Table 7.** Comparison of power reduction at different WLAN frequencies

|            | 0.9 GHz | 2.4 GHz | 3.6 GHz | 4.9 GHz | 5.9 GHz |
|------------|---------|---------|---------|---------|---------|
| 5000 pF    | 7,265   | 39,562  | 59,482  | 80,602  | 96,849  |
| 500 pF     | 788     | 4,055   | 6,061   | 8,236   | 9,910   |
| 50 pF      | 141     | 547     | 798     | 1,070   | 1,279   |
| 5 pF       | 76      | 197     | 272     | 354     | 417     |
4. Conclusion

ECG machine is one of the basic equipment used in the field of cardiology. Kintex-7 FPGA device is used in this work and it is implemented using Xilinx simulator. ECG machine is operated at different WLAN frequencies and under different capacitance. It is observed that by the variation of capacitance from upper values to lower, total power of the device is also reduced and power optimization can be achieved. Total power can be saved up to 89.15%, 89.75% and 89.81% for frequencies 0.9 GHz, 2.4 GHz and 3.6 GHz respectively by replacing capacitance 500 pF from 5000 pF.

5. Future Scope

In Future this ECG machine can be implemented using different other families of FPGA like Airtex-7 or Virtex-7. Moreover IO standards are also can be used in further to make this design more power efficient.

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