LEASH: Enhancing Micro-architectural Attack Detection with a Reactive Process Scheduler

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Abstract
Micro-architectural attacks use information leaked through shared resources to break hardware-enforced isolation. These attacks have been used to steal private information ranging from cryptographic keys to privileged Operating System (OS) data in devices ranging from mobile phones to cloud servers. Most existing software countermeasures either have unacceptable overheads or considerable false positives. Further, they are designed for specific attacks and cannot readily adapt to new variants.

In this paper, we propose a framework called LEASH, which works from the OS scheduler to stymie micro-architectural attacks with minimal overheads, negligible impact of false positives, and capable of handling a wide range of attacks. LEASH works by starving maliciously behaving threads at runtime, providing insufficient time and resources to carry out an attack. The CPU allocation for a falsely flagged thread found to be benign is boosted to minimize overheads. To demonstrate the framework, we modify Linux’s Completely Fair Scheduler with LEASH and evaluate it with seven micro-architectural attacks ranging from Meltdown and Rowhammer to a TLB covert channel. The runtime overheads are evaluated with a range of real-world applications and found to be less than 1% on average.

1. Introduction
For several years, computer systems designers have relied on traditional hardware mechanisms such as protection rings, segmentation, page tables, and enclaves, to isolate software entities executing in a CPU. These isolation mechanisms have been considerably weakened by a potent class of side-channel attacks known as micro-architectural attacks. A micro-architectural attack makes use of shared hardware resources to leak information across isolation boundaries. They have been used in a variety of applications, from creating covert channels [32], retrieving secret keys of ciphers [13, 58], reading Operating System data [38, 43], fingerprinting websites [65], logging keystrokes [64], reverse engineering Deep Learning algorithms [30], and breaking Address Space Layout Randomization [11, 27]. The last couple of years have seen these attack vectors applied on a range of devices from mobile phones [42] to third-party cloud platforms [64]. They have been used to leak secrets stored in Trusted Execution Environments like SGX [15] and Trustzone [77] and attack remote computers using webpages that host malicious Javascript [55] or Web-assembly [25].
tection is typically done using performance monitoring registers in the CPU called Hardware Performance Counters (HPCs) [8, 10, 16, 18, 50, 78]. On detection, the malicious-behaving thread is terminated or rescheduled to a different CPU. A severe limitation of current detection schemes is the false positives due to which benign processes are falsely flagged malicious. Contemporary works [8, 18, 50, 52, 78] attempt to reduce false positives by deploying complex Machine Learning models. While this increases overheads, the impact of the false positive rate is still unacceptably high. This limitation is exacerbated by the fact that a micro-architectural attack occurs rarely compared to the number of benign programs executing. Thus, these detection techniques more often impact benign program execution than mitigate an attack.

In this paper, we present a micro-architectural attack detection countermeasure called LEASH that has all the advantages of detection countermeasures with almost no impact of false positives. LEASH makes use of the observation that a spy thread in a micro-architectural attack needs to contend with the victim for a shared resource. The success of the attack depends on the extent to which the spy can force this contention. If the spy gets insufficient time to execute on the CPU, then the information leakage is reduced, stymieing the attack.

Figure (1a) provides an analogy.

The LEASH framework works from the Operating System (OS) scheduler. At every context switch, it uses the HPCs to quantify the malicious behavior of each thread in the system using a metric called threat index. It then allocates CPU resources for the thread based on its threat index. A high value of threat index indicates that the process gets less CPU time. For instance, in Figure (1b) thread $t_1$ has a threat index that continuously increases. The time slice it obtains for execution correspondingly reduces. If the thread were indeed a micro-architectural attack, the lesser CPU time would clamp the amount of information that is leaked from the victim, thus stymieing the attack.

A significant advantage of LEASH is in its handling of false detection. Suppose a benign thread temporarily exhibits malicious behavior, its CPU quota falls temporarily, and over time it regains its full CPU quota. Thread $t_2$ in Figure (1b) demonstrates this recovery after the 4-th epoch. This is unlike contemporary works [8, 18, 50, 52, 78], where a false detection has adverse irreversible effects. With LEASH, the false detection would only result in a small overhead. With the wide range of benchmarks we evaluated, the performance overheads were found to be less than 1% on average.

The important contributions of this paper are as follows:

- LEASH is a system scheduler based countermeasure for micro-architectural attacks that has low overheads and negligible impact of false positives. It can support a variety of micro-architectural attacks and can easily adapt to new variants. The framework is highly versatile and can be tuned to detect multiple different attacks simultaneously. It is designed to provide quick response, while still having features for sophisticated add-ons that can detect complex scenarios.
- We modify Linux’s Completely Fair Scheduler (CFS) with LEASH and evaluate its effectiveness with seven micro-architectural attacks including Prime+Probe on the L1 Data [56], L1 Instruction [6], and LLC caches [74]; L1 and TLB Evict+Time attacks [26, 56], Rowhammer [3, 37], Meltdown [1, 43]. The entire framework just adds around 20 lines of C code in the Linux kernel to provide micro-architectural security for the entire system.
- We have evaluated LEASH with multiple benchmark suites including the SPEC-2017 [17], SPEC-2006 [66], SPECViewperf-13 [4] and STREAM [48] and found an average performance overhead of 1%.

The rest of the paper is organized as follows. Section 2 presents the necessary background on micro-architectural attacks, Hardware Performance Counters, and Linux scheduler. In Section 3, we discuss the related works in micro-architectural attack mitigation. Section 4 sums the key idea in the LEASH framework. In Sections 5 and 6 we discuss the implementation details and present the evaluation and results, respectively. Section 7 discusses the caveats and limitations of LEASH. Section 8 concludes the paper.

2. Background

2.1. Micro-architectural attacks

A micro-architectural side-channel attack leverages leakage from shared micro-architectural resources in a system to glean sensitive information from a process. We illustrate a micro-architectural attack that uses a shared L1-data cache to create a covert channel between a sender and a receiver process. Apriori, the sender and receiver agree upon two cache sets for communicating 0 and 1 respectively. The receiver first performs memory operations that fill both cache sets. This is known as the prime phase. Depending on the message bit, the sender performs a memory operation to evict the receiver’s data from the corresponding cache set. In the probe phase, the receiver performs the memory operations again and times the accesses. Based on the access time, the receiver can infer the transmitted bit since the memory access to the evicted cache set would take longer owing to the cache miss.

Later in the paper, we use this covert channel as a running example to explain LEASH and show how the transmission-rate between sender and receiver can be reduced by throttling the receiver’s CPU time. Further, we apply LEASH to other micro-architectural attacks, including Meltdown [1, 43], Rowhammer [3, 37], L1 data cache attacks on AES [56], L1 instruction cache attacks on RSA [6], a TLB covert channel [26] and a prime-and-probe LLC covert channel [74].

2.2. Hardware Performance Counters

Most modern processors have a Performance Monitoring Unit on-chip to monitor micro-architectural events of running applications. Each logical core has a dedicated set of 4 to 8...
configurable registers that can count the number of times a particular event occurs in a given duration. These registers are called Hardware Performance Counters (HPCs) and can be used to monitor a wide range of events like CPU-cycles, cache accesses, context-switches, and page faults. The number of such events that can be monitored simultaneously is limited by the number of HPCs available in the hardware.

Patterns present in the time series traces of performance counter events have been shown to characterize the behavior of a thread’s execution. This has been leveraged in several applications such as detecting anomalous behavior in programs [40, 67, 72], side-channel attacks [10, 18, 50, 78] and malware analysis [12, 21, 67]. LEASH, similarly uses HPCs to compute a threat index for a thread. Threads which depict a micro-architectural attack like behavior are given a high threat index and are throttled by reducing their CPU time.

2.3. Process Scheduling

LEASH modifies the OS scheduling algorithm to consider the threat index of a thread for CPU resource allocation. While we can incorporate LEASH in most scheduling algorithms, in this paper, we demonstrate LEASH with the Completely Fair Scheduler (CFS); the default scheduler present in the Linux kernel since Version 2.6 [41].

The CFS algorithm tries to achieve the ideal multitasking environment where threads with equal priorities receive the same share of processor time, called timeslice. The timeslice allocated to a thread $t$, denoted $\Delta_{ts}$, is a fraction of a predefined value called targeted latency ($\Delta_{tl}$). When multiple threads compete for CPU time, the scheduler allocate timeslices in proportion to a metric called weight of the thread as follows

$$
\Delta_{ts} = \Delta_{tl} \times \frac{w}{\sum_{\text{threads}} w} = \Delta_{tl} \times s, \tag{1}
$$

where $w$ is the weight of the thread $t$, $\sum_{\text{threads}} w$ is the sum of weights of all the threads sharing the CPU, and $s$ is the relative weight of thread $t$. On thread creation, its weight takes a default value ($w_{\text{def}}$) which lies in the middle of 40 discrete levels, ranging from $w_{\text{MIN}}$ to $w_{\text{MAX}}$. The ratio of weights at two consecutive levels $\gamma$, ($0 < \gamma < 1$) is determined by the OS scheduler at design time. The relationship between these weight levels can be given as $w_{\text{MIN}} = \gamma^{19} w_{\text{def}} = \gamma^{39} w_{\text{MAX}}$. The weight also gives a notion of thread priorities. A higher weight value for thread implies a larger timeslice and a higher frequency of getting scheduled for execution.

3. Related work

There is a pressing need to develop lightweight, portable solutions for micro-architectural attacks. Most preventive countermeasures that have low overheads require hardware modifications [22, 35, 39, 44, 54, 57, 60, 61, 68, 71, 73] and cannot be incorporated in existing systems. To achieve portability, there have been a few attempts to tackle micro-architectural attacks from the Operating System, such as flushing shared resources [19, 32] and soft isolation of Virtual Machines sharing the same hardware [69]. Nomani and Szefer in [53] incorporate a neural-network within the OS scheduler, to detect tasks requiring the same functional units and scheduling them on different cores to minimize contention. Such solutions are likely to have scalability issues as the workloads increase.

Most contemporary detection-based solutions use HPCs and Machine Learning (ML) models [8, 18, 50, 51, 52]. Among the several shortcomings [20] of these works, the most serious limitation is with the false positives which adversely affect benign program execution. Contemporary works use complex techniques like KNNs, decision trees, neural networks and ensemble methods to reduce false positives which can still have unacceptable impacts. Furthermore, the complex techniques used have considerable overheads and could reduce the prediction rate leading to fast attacks completing undetected. Unlike these works, LEASH reacts to a flagged program by throttling its CPU-share, thus preventing the attack from completing. Contemporary works, on the other hand, would either migrate the program to another CPU or terminate it. The advantage we achieve with the feedback loop of LEASH is that falsely flagged threads can recover and regain their CPU-share with only slight increase in execution time. Further, due to the reactive control loop, very simple detection mechanisms are sufficient.

4. The LEASH Framework

Micro-architectural attacks depend considerably on CPU resources. If the attack programs are starved of the CPU, the success drops considerably. Consider, for example, the L1-cache timing covert channel discussed in Section 2.1. Figure 2 shows that starving the receiver thread not only reduces the communication bandwidth considerably but also increases the transmission errors. The reduced bandwidth and the increased error is due to smaller CPU-time shares, which prevents the receiver from performing a sufficient number of timing measurements.

Along with being highly CPU-bound, micro-architectural attacks are procedural and repetitive by design, which gives them a distinct execution behavior. For example, the receiver in the cache covert channel continuously executes a small set of instructions in a loop performing extensive memory
Equation 1. If the thread stops exhibiting the anomalous behavior, its threat index and the mean of its HPCBs logged would widen the scope of the attacks that can be detected. Section 5 discusses this further.

**Algorithm 1:** Detector component in LEASH for thread $t$ at the beginning of the $i$-th epoch.

1. **Initial State:** At $i = 0$, $T_i = 0$ and $flag = 0$. Global:
   - Event count threshold: $\tau$, default weight: $w_{\text{DEF}}$.
   - Input: Thread $t = \{w_{t-1}, T_{t-1}, \text{HPCBuf}\}$.

2. **Result:** Threat index for $i$-th epoch: $T_i$, flag $flag$.

3. \begin{algorithm}
   \begin{algorithmic}
   \State $\mu = \text{mean}(\text{HPC Buf})$
   \If {$flag = 1$}
   \State $T_i = T_{i-1} + S(t)$ // threat index update
   \EndIf
   \If {$w_{t-1} = w_{\text{DEF}}$}
   \State $flag = 0$ // Thread $t$ is unflagged
   \State $T_i = 0$
   \EndIf
   \If {$flag = 0$ and $\mu \geq \tau$}
   \State $flag = 1$ // Thread $t$ is flagged
   \EndIf
   \State return $(T_i, flag)$
   \end{algorithmic}
\end{algorithm}

LEASH flags threads which begin to behave maliciously (Line 11 in Algorithm 1). This happens when the mean $\mu$ of an unflagged thread first violates the threshold. For every subsequent epoch for this thread, where $\mu$ exceeds the threshold, its threat index is modified as per the output of the Supervisor function $S()$ as described in Equation 5 (Line 6). LEASH allows a flagged thread to recover if it stops behaving maliciously. The recovery starts when $\mu$ for the flagged thread first falls below the threshold. The thread’s threat index is then reduced in subsequent epochs until the threat reattains the default weight, which restores its CPU share. When this happens, the thread is unflagged and its threat index is reset (Lines 8 and 9).

Figure 4 shows two threads, a L1 Data Cache Covert Channel and a benign program bzip2 from the SPEC-2006 benchmark suite. While both threads, with counter values greater than the threshold get flagged by LEASH, the benign thread bzip2 recovers its fair share of CPU resources (in the 14th epoch) when its counter values go below the threshold. The CPU share for the covert channel is never restored as its counter values always remains over the threshold. Thus the...
covert channel is never unflagged. Its threat index saturates when the minimum weight is reached.

**Actuator.** For each thread in the $i$-th epoch, the Actuator receives the threat index ($T_i$) from the Detector and modifies the thread’s weight $v_i$ and in turn, the relative weight $s_i$ (Equation 1) for the thread. The relative weight for the thread at the beginning of the $i$-epoch is given as

$$s_i = A(s_{i-1}, T_i) = s_{i-1} - \gamma(s_{i-1}) \times T_i,$$  \hspace{1cm} (3)

where is $\gamma$, ($0 < \gamma < 1$) is a constant fixed by the OS scheduler which determines the amount of fall in the weight with every increase in the threat index. In our evaluation platform, $\gamma = 0.1$ which means that, for every rise in threat index values, the weight drops by 10% until it reaches $v_{\text{THR}}$. Similarly, when a thread is recovering, the threat index value is negative and hence every fall in threat index value increases its weight by 10% until its weight is restored. The adaptable design of LEASH efficiently brings down the cost of a false penalization. Once a benign thread, which is erroneously flagged, is unflagged, it regains its CPU share and executes without any additional overheads.

**Supervisor.** LEASH’s Detector identifies threads that are penalized and rewarded. Ideally, this decision should be based on careful analysis of the HPCBuf data so that malicious threads are quickly identified and penalized while benign threads are not affected. However, supporting sophisticated analysis in the Detector is difficult because it executes in a context switch and therefore affects the performance of the entire system. Thus, as seen in Algorithm 1, the Detector is kept very simple and comprises of about 6 instructions that are executed at every epoch ($N$ context switches).

To support complex analysis on the performance counter data, LEASH uses a Supervisor that does not need to execute in the context switch. The Supervisor provides threat specific control value ($v_i$) that represents the amount by which the thread index $T_i$ of a flagged thread is degraded or upgraded in the $i$-th epoch. The output of the $S(t)$ for a thread $t$ is given by

$$v_i = S(v_{i-1}, T_{i-1}, T_{i-2}, T_{i-3}, \ldots) .$$  \hspace{1cm} (4)

A general framework for the Supervisor function for thread $t$ involves a penalty function $P(t)$ and reward function $R(t)$, as given in Equation (5). Such a design allows the Supervisor to be implemented with different policies

$$S(t) = \begin{cases} P(t), & \mu > \tau \text{ (t is malicious)} \\ R(t), & t \text{ is flagged and } \mu \leq \tau \text{ (recovering)} \\ 0, & \text{thread t is unflagged} \end{cases}$$  \hspace{1cm} (5)

where $\mu$ is the mean of HPCBuf and $\tau$ is the threshold. Configurable Supervisor policies allow LEASH to handle new attack vectors. Section 5.3 provides more details about the Supervisor.

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**Algorithm 2: Context Switching in LEASH**

**Input:** Task prev getting preempted from runqueue rq

1. Begin
2. if threads in rq = 1 and flag = 1 then
   2.1. Wake up dummy thread
3. if prev.start then
4.   prev.end ← read event count
5.   prev.HPCBuf[prev.cs_count] ← (prev.end – prev.start)
6.   increment prev.cs_count
7. if prev.cs_count == N then
8.   Detector(prev) // Algorithm 1
9.   Reset HPCBuf, prev.cs_count
10. CFS context switching steps
11. next.start ← read event count
12. Return rq

13. End

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5. Implementation

This section provides the implementation details of LEASH and some of its primary design choices.

5.1. Sensing Program Behavior

Most modern processors have 4 to 8 Hardware Performance Counters (HPCs) per logical core that can be configured to count one of several micro-architectural events such as cache misses, branch events, or loads and stores to various levels of memory. To enhance readability, we label 40 selected events as $e_1, e_2, \ldots, e_{40}$ in the paper. We describe these events and associated masks defined by the micro-architecture in detail in the Appendix.

5.2. Enhancing the CFS Scheduler for LEASH

In the Linux kernel’s CFS implementation, the context switch is implemented in a function called context_switch$^\dagger$. The function switches context from a thread called prev to a thread called next as shown in Algorithm 2. To support LEASH, the context_switch function is modified to perform three additional operations; (a) it schedules a dummy thread if needed; (b) it logs the performance counter data in the scheduled out thread’s task structure; and (c) it executes the detector when the HPCBuf gets full. We describe each of these operations.

**Dummy Thread.** As described in Equation (1), the targeted latency $\Delta t_1$ is shared among the threads in the Run Queue (rq), proportional to their weights. However, when there is only one thread in the Run Queue, the timeslice it receives is

$^\dagger$This function is defined in kernel/sched/core.c in the kernel source.
5.3. Supervisor Policy

The Supervisor in LEASH manages the control values, as shown in Equation (5). Algorithm 1 shows how these values affect the threat index and, in turn, the weight of a flagged thread. The key components of the Supervisor are the penalty ($P(t)$) and reward ($R(t)$) functions that respectively provide the rate of degradation and recovery for a flagged thread.

The penalty and reward functions are pluggable. The simplest form is a static policy, where the outputs of the functions are constants. Such a policy is agnostic to the thread execution history. In contrast, an adaptive policy uses the thread execution history. An example of such policy is $P(t) = P(t) + 1$ and $R(t) = R(t) + 1$ which increments the penalty values every flagged epoch and the reward value every recovering epoch. Figure 6, shows the difference between the two policies for a fragment of the benign bzip2 execution, where the thread briefly crossed the threshold for seven epochs. With the static policy, the threat index is increased with the same rate, independent of the previous epochs. Similarly, when the counter drops below the threshold, the threat index decreases with the same rate until the thread is unflagged. With the adaptive policy, the output of $P(t)$ and hence the rate of increase of threat index (Algorithm 1), is incremented in every flagged epoch. Similarly, when the counter drops below the threshold, the threat index is reduced much more quickly. As seen in Figure 6, recovery for this benign thread takes 2 epochs less compared to the static policy.

6. Evaluation and Results

Every micro-architectural attack is characterized by two aspects. The first is the micro-architectural component that leaks information, for example, shared resources like the L1 data [13, 56] and instruction [6] caches, the Last Level Cache (LLC) [45, 75, 74], Translation Lookaside Buffer (TLB) [26], DRAM [37], and Branch Prediction Units (BPU) [23, 14]. The second is the attack strategy used to extract information from the leaking resources. Several strategies such as Prime+Probe [5, 6, 45], Evict+Time [36, 33], Flush+Reload [75], and time-driven attacks [13, 23] have been proposed for this purpose. We evaluate LEASH with seven different micro-architectural attacks chosen to get a wide coverage of leaking components and attack strategies.

Table 1 provides the details of attacks evaluated with some example events to detect them. Further in this section we discuss the deployment of LEASH on a system and present the evaluation results for various attacks. We then present the overheads on various workloads including the SPEC-2006 [66], SPEC-2017 [17], SPECviewperf-13 [4] and STREAM [48] benchmark suites.

The evaluation is done on an Intel Core i7-3770 processor, which deploys Intel’s Ivy Bridge micro-architecture. The processor has four physical cores, each with two hyperthreads. We patch the Linux kernel, version 4.19.2, with LEASH and boot Ubuntu 16.04 Operating System. We configure LEASH...
Table 1: Micro-architectural attacks evaluated; their leaking component; and the attack strategy used. For our evaluation we have used $e_2$, $e_{11}$, $e_{12}$, and $e_{39}$.

| Attack                          | Leaking Component | Strategy            | Example Event(s) to detect the attack                                                                 |
|---------------------------------|-------------------|---------------------|--------------------------------------------------------------------------------------------------------|
| L1-D cache Covert Channel [56]  | L1-D cache        | Prime+Probe         | $e_{12}$: cycles for which the instruction decode queue is empty, or $e_{26}$: writebacks from L1D to L2 cache lines in modified coherency state. |
| L1-D cache attack on AES [56]   | L1-D cache        | Evict+Time          | $e_{12}$, or $e_{26}$: L2 store read for ownership (RFO) requests from the thread.                     |
| L1-I cache attack on RSA [5, 6] | L1-I cache        | Prime+Probe         | $e_{39}$: the number of prefetcher requests that miss the L2 cache, or $e_{13}$: the number of instruction cache misses. |
| LLC Covert Channel [74]         | LLC               | Prime+Probe         | $e_{39}$, or $e_{37}$: the cache lines for references to the LLC                                        |
| Meltdown [1, 43]                | Memory            | Flush+Reload        | $e_2$: the mispredicted branch instructions at retirement, or $e_{15}$: direct and indirect near call instructions |
| Rowhammer [3, 37]               | DRAM              | Hammer access       | $e_2$, or $e_{17}$: the dirty L2 cache lines evicted by demand.                                       |
| TLB Covert Channel [26]         | TLB               | Evict+Time          | $e_{11}$: the misses in all TLB levels                                                                  |

![Figure 7: A heatmap of the Detectability Score of 40 selected events for each of the attacks in Table 1. Identically annotated events for multiple attacks can be used to detect all those attacks, such as event $e_2$ for Rowhammer and Meltdown.](image)

![Figure 8: The effects of LEASH on different attacks.](image)

with an adaptive Supervisor policy with $P(t) = P(t) + 1$ and $R(t) = R(t) + 1$ (Section 5.3) for the evaluation.

### 6.1. Deploying LEASH

Prior to the deployment of LEASH on a system, the designer models the threat in terms of a set of attack vectors. Events need to be chosen to detect all attack vectors in the set. While typical microprocessors have a large number of countable events, they have a limited number of configurable Hardware Performance Counter (HPC) registers. Our evaluation platform for instance, has 208 events and four configurable HPC registers [34]. The designer thus has to choose at most four events that can best distinguish the set of attacks from benign programs. In the subsequent sections, we present techniques to choose such events and the evaluation results.

**Selecting HPCs.** As a representative for benign programs, we use all programs of a CPU benchmark suite that we assume cover a variety of benign program behavior. For each micro-architectural attack, we analyze all supported events and rank them based on distinguishability from the benign set using Principal Component Analysis [24]. Figure 7 summarises the distinguishability score for the 7 attack vectors in Table 1 using SPEC-2006 CPU benchmark suite as the set of benign programs [66] for the best 40 events of the 208 supported on our platform. Since there are only 4 HPC registers available, we configure at most 4 events that can best distinguish the 7
attacks. From Figure 7, we notice that events $e_9$, $e_{11}$, $e_{12}$, and $e_{39}$ satisfy this requirement. Event $e_9$ covers attacks Meltdown and Rowhammer event $e_{11}$ covers attacks L1-I Cache attack and TLB Covert Channel, event $e_{12}$ covers attacks L1-D Cover Channel and L1-D attack on AES while the event $e_{39}$ can cover the attacks LLC Covert Channel and Rowhammer. Many other such event combinations are also possible.

Detecting Attacks. LEASH is able to throttle all the attacks in Table 1. Figure 8 describes the impact of LEASH on these attacks. For example, the guessing entropy [47] for 1 byte of an T-table based AES key [2], using the L1-D Evict+Time attack increases from 10 to 131 (Figure 8a). The error in guessing 1-bit of an RSA key used in a square-and-multiply implementation [49] increases to 50% (Figure 8b). In both cases, the attacks are as good as an attacker that randomly guesses the key. The covert channels at LLC [74] and TLB [26] see a drastic fall in the number of bits communicated after getting throttled by LEASH (Figure 8c and 8f). The Rowhammer [3] attack, which induces a bit-flip in a DRAM row every 29 iterations (on average) is unable to cause a single bit-flip even after a day of execution (Figure 8d). Further, the Meltdown [1] attack that dumps contents of the kernel memory, is throttled by LEASH to become ineffective (Figure 8e).

LEASH with Attack Variants. While configuring LEASH, events are chosen by profiling a specific realization of an attack. However, with the same configuration LEASH can detect different variants of the attacks as well. For example, the covert channel described in Section 2.1, can have multiple variants by tweaking the communication protocol. For example, we design a Variant 1, which transmits redundant bits for reliability while a Variant 2, which uses multiple sets to transmit two bits at a time. LEASH can detect these variants of the covert channel as seen in Figure 9. Without LEASH, the bandwidth is 0.43 bits/second for the base variant, 1.76 bits/second for Variant 1 and to 0.087 bits/second for Variant 2. With LEASH, all three covert channels are stymied and almost no bit gets transmitted correctly.

6.2. Performance Overheads

We evaluated LEASH with several benchmark suites including SPEC-2006 [66], SPEC-2017 [17], SPECViewperf-13 [4] and STREAM [48]. SPEC-2006 and SPEC-2017 are CPU benchmark suites with different integer and floating-point programs like Machine Learning algorithms. SPECViewperf-13 is a collection of graphics-oriented benchmarks programs, while STREAM is designed to perform memory-intensive tasks. The overheard seen in Figure 10 is due to (1) the few additional instructions in each context switch (Figure 5) and (2) benign threads being falsely flagged. In contrast to contemporary detection counter-measures [8, 10, 16, 18, 50, 78], all falsely flagged programs recover and are not adversely affected. The only case where over 25% overheads occurs is blender_r, a 3D rendering program, which is falsely flagged in 30% of its epochs due to the prolonged malicious looking behavior. Out of the programs evaluated, over 45% were flagged at least once. However, run-time overheads on average across all benchmarks remain low at 1%. Another reason for the low overheads is that LEASH executes during a context switch in the kernel. Unlike [10, 16, 18, 50, 78], it does not require a background task that needs scheduling and is independent of the system load.

7. Caveats and Limitations

- Time-Driven Attacks. Unlike the attacks discussed in Section 6, in a time-driven attack, the attacker uses the victim’s execution time [14, 62, 63]. LEASH cannot detect such attacks because of the absence of a spy thread to flag.
- High-resolution Attacks. If a high-resolution attack like [9] works in less time than an epoch, LEASH would not be able to stop it unless the epoch is shortened. However, this can increase the overheads (Figure 5).
- Undetectable Attacks. While the attacks evaluated were identifiable by HPCs, there may be attacks that evade them. LEASH would not be able to thwart such attacks.
- Complex adversarial attacks on LEASH. While the Supervisor component in LEASH can be designed to detect multiple adversarial attacks, there may be complex strategies such as using distributed colluding threads [29]. The Supervisor would need to be enhanced to handle such distributed attacks.
- Detecting a large number of attacks. As the attack vectors to detect increase, the number of events to be counted may exceed the HPCs available in the hardware, requiring multiplexing. This may increase context switch times and reduce the precision of the results.
8. Conclusions

Detection based countermeasures for micro-architectural attacks are promising as they can adapt easily to a wide range of attacks. However, a major shortcoming is the unacceptably high false positive rate. Contemporary research attempts to address this limitation on by deploying sophisticated analysis techniques. While this has found to only marginally improve false positives, the overheads and latencies are affected considerably due to complex techniques used. Unlike these approaches, the reactive design of LEASH facilitates lightweight analysis which allows falsely flagged threads to recover quickly with minimum overheads of less than 1% while still accurately detecting attacks. To the best of our knowledge, LEASH is the first reactive countermeasure for micro-architectural attacks in the Operating System scheduler and is therefore, invariant to system load. Additionally, it just adds around 15 instructions per context switch which has a negligible impact on context switch latencies. It thus opens avenues to security aware OS scheduler designs.

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