μ-cuDNN: Accelerating Deep Learning Frameworks with Micro-Batching

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Abstract—NVIDIA cuDNN is a low-level library that provides GPU kernels frequently used in deep learning. Specifically, cuDNN implements several equivalent convolution algorithms, whose performance and memory footprint may vary considerably, depending on the layer dimensions. When an algorithm is automatically selected by cuDNN, the decision is performed on a per-layer basis, and thus it often resorts to slower algorithms that fit the workspace size constraints. We present μ-cuDNN, a transparent wrapper library for cuDNN, which divides layers’ mini-batch computation into several micro-batches. Based on Dynamic Programming and Integer Linear Programming, μ-cuDNN enables faster algorithms by decreasing the workspace requirements. At the same time, μ-cuDNN keeps the computational semantics unchanged, so that it decouples statistical efficiency from the hardware efficiency safely. We demonstrate the effectiveness of μ-cuDNN over two frameworks, Caffe and TensorFlow, achieving speedups of 1.63x for AlexNet and 1.21x for ResNet-18 on P100-SXM2 GPU. These results indicate that using micro-batches can seamlessly increase the performance of deep learning, while maintaining the same memory footprint.

I. INTRODUCTION

Prevalent Deep Neural Networks (DNNs) are becoming increasingly deeper and are trained with large batch sizes. Specifically, state-of-the-art DNNs contain hundreds of layers [1], [2], and utilize batch sizes in the order of thousands [3], [4], [5].

Large batches are also favored by distributed data-parallel deep learning frameworks, because they improve utilization of accelerators, as well as hiding the communication of parameter gradients in the computation efficiently. Consequently, the batch size per accelerator (e.g., GPU) should be large to achieve better scaling. Since the memory usage of a DNN is nearly proportional to the layer size and the batch size, the accelerator memory tends to be used at full capacity in most real-world cases.

This “limited memory scenario” is also exhibited in cuDNN [6], a deep learning kernel library for NVIDIA GPUs. cuDNN provides a variety of computational primitives for deep neural networks, and is widely used in deep learning frameworks, such as Caffe [7] and others [8], [9], [10]. cuDNN provides up to eight different algorithms to perform convolutions, each of which requires different temporary storage (workspace) schemes. To guide users to determine the best algorithm for a given maximum workspace size, cuDNN provides a function cudnnGetConvolutionAlgorithm (* is one of convolution types, Forward, BackwardData and BackwardFilter), that benchmarks all the algorithms and chooses the best algorithm, either with respect to computation time or memory usage. However, if the workspace size requested by a fast algorithm is one byte larger than provided, cuDNN will resort to a slower algorithm that requires less workspace. In fact, the performance impact can be 4.51x in the 2nd convolutional layer of AlexNet, as shown in Fig. 1.

In this paper, we propose μ-cuDNN, a transparent wrapper for cuDNN that attempts to mitigate the aforementioned inefficiency. In order to utilize fast convolution algorithms with limited size of workspace, μ-cuDNN automatically divides layer mini-batch computation into several micro-batches and perform multiple convolutions sequentially. μ-cuDNN decouples the statistical efficiency (speed of accuracy/loss improvement with fixed amount of parameter updates) from the hardware efficiency (speed of computations with fixed amount of parameter updates), improving only the latter. Using micro-batches, μ-cuDNN improves the utilization of the accelerators without incurring any reduction in training accuracy.

The contributions of this paper are as follows:

- We present a method to automatically divide mini-batch training into several “micro-batches”, so that faster algorithms are utilized with tight workspace constraints.
- We propose two different workspace allocation policies, which enable optimization of multiple convolutional layers with inter-dependencies.
- We evaluate μ-cuDNN over two different deep learning frameworks, Caffe and TensorFlow, showing that it can mitigate the inefficiency of cuDNN even with state-of-the-art Convolutional Neural Networks (CNNs), such as AlexNet and ResNet.

II. THE ANATOMY OF CONVOLUTIONAL NEURAL NETWORKS

Convolution operations in Convolutional Neural Networks (CNNs) apply multiple filters to a batch of channels of two-dimensional data (Algorithm 1, Fig. 2). In particular, input and output tensors are represented as four-dimensional tensors with dimensions \((N, C, H, W)\), where \(N\) is the mini-batch size, \(C\) is the number of channels, and \(H\) and \(W\) represent...
Fig. 1: Execution time of cuDNN 7.0.1 forward convolution of single-column AlexNet [11] with different workspace sizes. The “Best” case always chooses the fastest algorithm regardless of workspace size, while in the “−1 byte” case the maximum workspace size is limited to 1 byte less than the best algorithm.

Algorithm 1 Pseudo-code of two-dimensional convolution.

```
for(n = 0; n < N; n++) // Mini-batch loop
  for(k = 0; k < K; k++) // Output channel loop
    for(h = 0; h < H; h++) // Height loop
      for(w = 0; w < W; w++) // Width loop
        for(c = 0; c < C; c++) // Input channel loop
          for(v = 0; v < V; v++) // Kernel width loop
            for(u = 0; u < U; u++) // Kernel height loop
              Y[n, k, h, w] += W[k, c, v, u] × X[n, c, h + v, w + u];
```

Fig. 2: Two-dimensional convolution. Each element of Y is set to be a sum of element-wise products between partial C × V × U area of X and one filter from W.

image height and width, respectively. Similarly, the filter tensor is represented as four-dimensional (K, C, V, U) tensor, where K is the number of output channels and V, U represent kernel height and width.

The two-dimensional convolution is composed of seven-nested loops (Algorithm 1). The innermost three loops compute the actual convolution, where one element of the input tensor X is multiplied and accumulated to one element of the output tensor Y. The remaining loops iterate over all elements of Y. The key observation is that in order to solve the problem described in Section I, there is no dependency inside the mini-batch loop between different iterations. This is intuitive because in training or inference we compute parameter gradients or outputs with respect to different data samples, so this is equivalent to computing N different CNNs concurrently. This observation motivates us to apply loop tiling to the mini-batch loop, so that we can reduce the resident workspace size.

The only exception to the inter-sample independency is the computation of parameter gradients;

\[
\frac{\partial L}{\partial W} = \frac{1}{N} \sum_{n=1}^{N} \frac{\partial L_n}{\partial Y_n} \ast X_n,
\]

where L and L_n is the loss function with respect to a mini-batch and a sample n respectively, and * is the convolution operation [12]. The semantics of this computation is, however, not violated by the loop splitting, only if each of the iterations is performed sequentially.

In cuDNN, there are three operations related to the two-dimensional convolution; Forward for forward computation (Fig. 2), BackwardData for computing neuron errors in back-propagation, BackwardFilter for computing parameter gradients in back-propagation.

Although Forward and BackwardData can directly be divided into several micro-batches, BackwardFilter cannot, since there are output dependencies on the accumulated parameter gradients tensor dW. However, we can still divide the loops by running BackwardFilter multiple times while accumulating the results, i.e., output scale = 1 in cuDNN. Therefore, loop splitting can be achieved by repeating cuDNN kernels one or more times for any convolution-related operation, regardless of the underlying method.
III. \(\mu\)-cuDNN

\(\mu\)-cuDNN is a transparent C++ wrapper library for cuDNN, which can easily be integrated into most deep learning frameworks [7], [13], [8], [10]. The key concept of \(\mu\)-cuDNN is that it automatically divides a mini-batch to several batches (referred to as “micro-batches” in this paper) and optimizes their sizes, to utilize faster convolution algorithms (Fig. 3).

A. \(\mu\)-cuDNN Methodology

\(\mu\)-cuDNN library employs one of two workspace utilization policies to optimize micro-batches for convolution kernels (Fig. 4):

- **Workspace Reuse (WR):** WR allocates one workspace per layer, sharing the space between the internal micro-batches. In this scheme, each layer is assumed to use the workspace exclusively, hence the total size of the workspaces is in proportion to the number of convolutional layers.

- **Workspace Division (WD):** WD allocates one workspace per network, and assigns different segments to each convolutional layer. WD enables small groups of convolution operations, as in the Inception module [14], to run concurrently with larger workspaces. In WD, the actual workspace is managed by \(\mu\)-cuDNN rather than the deep learning framework. This is because conventional frameworks allocate each workspace separately, lacking a global view of the entire network’s workspace requirements.

WR and WD both rely on the parameters of one or more convolution kernel(s), the mini-batch size, and the maximum workspace size. The output of \(\mu\)-cuDNN is a division of the mini-batch, and “micro-configurations”; a pair of a convolution algorithm and micro-batch size for each convolution micro-batch. In this paper, we define “configuration” of a segmented convolution kernel as “a list of micro-configurations”. For example, if a kernel with a mini-batch size of 256 is equally divided into four micro-batches and each of them uses algorithm \(X\), the configuration is represented as \(\{(X, 64), (X, 64), (X, 64), (X, 64)\}\). Also we define concatenation of two lists as +, such as \(\{a, b\} + \{c, d\} = \{a, b, c, d\}\) and \(\{a\} + \emptyset = \{a\}\).

B. WR Algorithm

The goal of the WR policy is to optimize \(T(B)\), the total execution time with mini-batch size of \(B\) using Dynamic Programming (DP), given by:

\[
T(b) = \min \left\{ T_\mu(b), \min_{b' = 1, 2, \ldots, B-1} T(b') + T(b - b') \right\},
\]

where \(T_\mu(b)\) is the fastest execution time of one convolution kernel with a micro-batch size of \(b\), within the workspace constraint. If the first row of the definition of \(T(B)\) is smaller than the second row, \(\mu\)-cuDNN does not have to divide the batch. Otherwise, it is beneficial to divide the batch into two or more parts, applying the process recursively (Fig. 5).

The key point of WR is that the optimal micro-configuration size is deterministic and independent from other kernels. This is because in this case, we assume that multiple kernels do not run simultaneously.

The algorithm of WR is three-fold, where the mini-batch size is \(B\), and user-given maximum workspace size is \(M\):

1) For \(b = 1, 2, \ldots, B\), WR benchmarks all available convolution algorithms of micro-batch size of \(b\) with maximum workspace size of \(M\), using cuDNN. We define the fastest micro-configuration as \(c_\mu(b) = (a, b)\) (where \(a\) is the fastest algorithm) and its execution time as \(T_\mu(b)\).

2) For \(b = 1, 2, \ldots, B\), WR computes \(T(b)\), the fastest execution time for micro-batch size of \(b\), and \(c(b)\), the corresponding configuration, as follows (where \(T(0) = 0, c(0) = \emptyset\)). \(T(b)\) and \(c(b)\) are memorized and reused for further iterations.

\[
\hat{b}_\mu \leftarrow \arg\min_{b = 1, 2, \ldots, b} \{ T_\mu(b_\mu) + T(b - b_\mu) \}
\]

\[
T(b) \leftarrow T_\mu(b_\mu) + T(b - b_\mu)
\]

\[
c(b) \leftarrow \{ c_\mu(b_\mu) \} + c(b - b_\mu)
\]

3) Outputs the optimal configuration \(c(B)\).
C. WD Algorithm

In the WD scheme, configurations for multiple convolution kernels are optimized, while at the same time the total workspace size should be less than the total workspace limit that users specify. Therefore, WD is a more complex problem than WR, since the configuration of each convolution kernel is no longer independent from others, due to the total workspace size constraint.

To solve this problem, we formulate a 0-1 Integer Linear Programming (ILP)-based optimization algorithm (Fig. 6). Given the set of kernels $K$ and sets of available configurations $C_k$ of kernel $k$, WD is solved by minimizing Equation 1:

$$
\text{min.} \quad T = \sum_{k \in K} \sum_{c \in C_k} T_k(c) x_{k,c} \tag{1}
$$

subject to:

$$
\sum_{k \in K} \sum_{c \in C_k} M_k(c) x_{k,c} \leq M \tag{2}
$$

$$
\sum_{c \in C_k} x_{k,c} = 1 \quad (\forall k \in K) \tag{3}
$$

$$
\sum_{k \in K} \sum_{c \in C_k} T_k(c) x_{k,c} \leq M \tag{4}
$$

where $M_k(c)$ and $T_k(c)$ are the workspace size and execution time of kernel $k$ with configuration $c$, respectively. Equation 2 limits the total workspace size to the user-specified size $M$. cuDNN uses configuration $c$ on kernel $k$ if and only if $x_{k,c} = 1$, and exactly one of them is selected for each kernel $k$, according to the constraint in Equation 3.

1) Desirable Configuration Selection: The challenging problem of the above ILP-based algorithm is that if all possible configurations are evaluated (i.e., all combinations of the number of micro-batch and algorithms), the search-space is in the order of $|K||A|^B$ (where $A$ is set of algorithms and $B$ is the mini-batch size) configurations in total, which makes the problem impractically large.

Here we compute a Pareto front to remove undesirable configurations from all possible configurations, without returning any sub-optimal solutions. The resulting Pareto front $C_k$ is then input to the ILP (Equation 1-4) to solve the entire problem.

First, we modify the DP algorithm from WR (Section III-B) to output a set of configurations, rather than the fastest configuration, as follows:

$$
C(b) = D \left( \bigcup_{b_1=1,2,\ldots,b} \bigcup_{c \in C_b} \bigcup_{b \in (0-b_1)} \{c_b \} + c \right),
$$

where $C_b(c)$ is a set of available micro-configurations of micro-batch size of $b$, and $D$ is a pruning function described below. Note that this outputs $c(B)$ of the WR algorithm as one of its elements; $c(b) \in C(b)$ and $c(b) \in C_b(b)$ for any $b$.

Second, we define the “desirable configuration set” $D(C) \subset C$ as a Pareto front in the two-dimensional (execution time $\times$ workspace size) space (Fig. 7):

$$
D(C) = \{c \in C | \forall c' \in C \ [T(c) < T(c') \lor M(c) < M(c')]\}
$$

where $T(c)$ and $M(c)$ is execution time and required workspace size of a configuration set $c$. This definition implies that any $c \in D(C)$ is the fastest configuration among any of the elements of $D(C)$ using a workspace size of $M(c)$ or less. Conversely, if an element $c \in C$ is not in $D(C)$, there is an element that is faster than $c$ and requires less workspace, hence there is no reason to choose $c$, namely “undesirable”.

The pruning drastically reduces the number of variables of Equation 1, and enables solving the ILP for state-of-the-art deep CNNs in practical time. For instance, the maximum number of desirable configurations of AlexNet’s layers we examined in Section IV-D was 68, which is much smaller than the exponential order. Fig. 8 illustrates a Pareto front of one convolutional layer of AlexNet.

The validity of the pruning algorithm that the optimal solution of the ILP does not include any undesirable configurations is proved as follows:
and Equation 2 as

\[
\sum_{k \in K} \sum_{c \in C_k} M_k(c)g(x_{k,c}) = \sum_{k \in K} \sum_{c \in C_k} M_k(c)g(x_{k,c}) + M_a(v)g(x_{a,v}) \\
\leq \sum_{k \in K} \sum_{c \in C_k} M_k(c)f(x_{k,c}) + M_a(u)f(x_{a,u}) \\
\leq \sum_{k \in K} \sum_{c \in C_k} M_k(c)f(x_{k,c}) \leq M.
\]

Similarly, by replacing \(M_k\) as \(T_k\) in the inequality above, the objective value of \(g\) is proved to be lower than \(f\), hence \(g\) is a better solution of the ILP. Therefore it contradicts the supposition that \(f\) is the optimal solution.

\[\Box\]

\[ D. \ \mu\text{-}cuDNN \ Implementation\]

To enable \(\mu\)-cuDNN, the only modification that needs to be performed to the code is to replace the cuDNN handle type `cudnnHandle_t` with `UcudnnHandle_t`. The \(\mu\)-cuDNN handle object is an opaque type that wraps the original type, such that users can call any cuDNN function. When a convolution operation or benchmarking function is called with the \(\mu\)-cuDNN handle object, the \(\mu\)-cuDNN library internally computes the optimal configurations, and returns a virtual algorithm ID and zero required workspace size. This mechanism enables users to call \(\mu\)-cuDNN with minimal modification to the original code. For example, the number of lines to be modified to introduce \(\mu\)-cuDNN to Caffe (v1.0) is approximately three.

The implementation of \(\mu\)-cuDNN is based on overloading a subset of cuDNN functions, where the memory of the \(\mu\)-cuDNN handle type is structured to behave to act as the cuDNN internal handle for the other calls. We define a cast operator from the \(\mu\)-cuDNN handle object to cuDNN (\(\mu\)-cuDNN delegates most of the functions to cuDNN, but overrides functions related to the convolutional layers).

The optimization algorithm in \(\mu\)-cuDNN is based on the methodology described in Section III-A. In practice, \(\mu\)-cuDNN provides a “batch size policy”, which determines what micro-batch sizes are benchmarked at the step 1 of the WR algorithm, as follows:

- all uses all batch sizes \(b \in \{1, 2, 3, \cdots, B\}\). Although this always finds the optimal solution, it takes \(O(B)\) time for the benchmark.
- powerOfTwo uses only power-of-two batch sizes \(b \in \{2^0, 2^1, 2^2, \cdots, B\}\). This saves a considerable amount of time since it only costs \(O(\log B)\) time for the benchmark.
- undivided uses only the original mini-batch size \(b \in \{B\}\). In WR, this option always selects the same configuration as cuDNN, hence this option is only useful to evaluate the overhead of \(\mu\)-cuDNN.

These policies can be specified via an environment variable or through a special library function in \(\mu\)-cuDNN. Furthermore,
\(\mu\)-cuDNN supports parallel micro-configuration evaluation via an environment variable, in which the aforementioned micro-batches are distributed to different GPUs on the same computing node and tested concurrently. This function assumes that the node contains multiple homogeneous GPUs.

\(\mu\)-cuDNN caches the optimized configurations and the benchmark results into memory and optional file-based database respectively, to skip unnecessary recomputations. This is especially beneficial for networks that replicate convolutional layers of the same size, such as ResNet [2]. In addition, the file-based caching enables offline benchmarking, as well as sharing the results among a homogeneous GPU cluster via network file system.

E. Implementation of WD Optimization

To perform WD optimization, \(\mu\)-cuDNN must know the number of convolutional layers and corresponding layer parameters in advance, i.e., before running any kernel. In the current cuDNN API, however, the parameters are passed one layer at a time, and thus there is no way to obtain all the parameters collectively from deep learning frameworks.

To overcome this issue, we assume that the deep learning framework calls `cudnnGetConvolution*Algorithm` one time for each layer prior to the computation of the entire network (e.g., training, inference). This is the most straightforward use of the cuDNN interface, as memory (including workspace) is usually allocated before initiating computations. Due to the specific implementation of Caffe, we add a \(\mu\)-cuDNN library call after network initialization, which ignores subsequent cudnnGetConvolution*Algorithm calls.

When cudnnGetConvolution*Algorithm is called, \(\mu\)-cuDNN pushes the kernel parameters to an internal list, and returns a dummy result. Note that the returned results satisfy the semantics given by the cuDNN interface, so the framework will not raise errors and will not allocate its own workspaces.

When cudnnConvolution* is called for the first time, \(\mu\)-cuDNN executes the optimization algorithm (namely, WD). We use the GNU Linear Programming Kit (GLPK) [15] as the ILP solver.

### Table I: Evaluation Environment Specification.

|              | TSUBAME-KFC/DL | TSUBAME 3 | DGX-1 |
|--------------|----------------|-----------|-------|
| CPU (Intel Xeon) | E5-2620 x 2    | E5-2680 v4 x 2  | E5-2698 v4 x 2  |
| GPU (NVIDIA Tesla) | K80 x 4       | P100-SXM2 x 4   | V100-SXM2 x 8   |
|               | - 8.73 SP TFlop/s | - 10.6 SP TFlop/s | - 15.7 SP TFlop/s |
|               | - 24 GIB DDR5  | - 16 GIB HBM2  | - 16 GIB HBM2  |
|               | (480 GB/s BW) | (732 GB/s BW)  | (900 GB/s BW)  |
| OS            | CentOS 7.3.1611 | SUSE Linux Enterprise Server 12 SP2 | Ubuntu 16.04.3 |

**CUDA**

- 8.0.61
- 8.0.44
- 9.0

**cuDNN**

- 6.0
- 6.0
- 7.0.5

**GLPK**

- 4.63
- 4.63
- N/A

**Caffe**

- 1.0
- 1.0
- N/A

**TensorFlow**

- N/A
- 1.4.1
- N/A

IV. Performance Evaluation

We evaluate the performance of \(\mu\)-cuDNN for three different GPU architectures: NVIDIA Tesla K80 [17], P100-SXM2 [18] and V100-SXM2 [19] on the TSUBAME-KFC/DL, TSUBAME 3, and DGX-1 supercomputers, respectively. The specifications of these supercomputers are listed in Table I.

Throughout the evaluation, we use single-precision floating point format and store tensors in the NCHW storage order. We use three different deep learning frameworks for evaluations: Caffe [7], its NVIDIA branch (NVCaffe) [16], and TensorFlow [8]. Both support recent versions of cuDNN (6 or 7). We use a built-in benchmarking command (Caffe’s “time” command) or an official benchmarking script (from TensorFlow models repository [20]) to measure the execution time of forward and backward passes, and show the sum of forward and backward passes together. In the following sections, unless explicitly mentioned, each forward-backward passes are measured 50 times on Caffe and 100 times on TensorFlow.

For neural networks, we use AlexNet[1], ResNet[2], and DenseNet[21]. For evaluations on Caffe, we use the AlexNet model defined in Caffe, ResNet-18, and ResNet-50 from NVCaffe. We modify data prefetching size from 4 to 16 for AlexNet and ResNet-18 for TSUBAME 3. For evaluations on TensorFlow, we use the definitions in an official benchmarking repository [22].

As for workspace limit, unless explicitly mentioned, we use 8 MiB and 64 MiB for each layer, which are the default workspace size limits of Caffe and Caffe2 [13] respectively. In addition, we use 512 MiB of workspace per layer to investigate the case where sufficiently large workspace is provided. To shorten the benchmarking time, we use several GPUs on the same node with the parallel evaluation function of \(\mu\)-cuDNN, mentioned in Section III-D.

A. Convolution Kernel Optimization Using WR

Fig. 9 shows the execution time of forward convolution (cudnnConvolutionForward) of the “conv2” layer in AlexNet on P100-SXM2. With workspace size of 64 MiB,
the GEMM (GEneral Matrix-Matrix multiply)-based algorithm is the one chosen by cuDNN, requiring only 4.3 KiB for workspace if the mini-batch is not divided. On the other hand, FFT-based convolution [12] is more efficient, although it requires excessive amount of workspace (213 MiB) to store the images and filters in the frequency domain, \( \mu \text{-cuDNN} \) with powerOfTwo option successfully utilizes the use of FFT within the workspace size constraints, using 48.9 MiB over micro-batches of size 32.

The all option also enables \( \mu \text{-cuDNN} \) to use Winograd convolution [23], an algorithm that is especially efficient for small convolution kernels, achieving 2.33x speedup over undivided in total.

B. CNN Optimization Using WR

We evaluate WR-based optimization on two different deep learning frameworks: Caffe and TensorFlow.

1) Caffe: Fig. 10 shows timing breakdowns of Caffe on AlexNet with three different GPUs. Additionally, we only highlight convolutional layers since the others (e.g., pooling) are out of the scope of this paper.

One important observation from Fig. 10 is that the performance improvement of \( \mu \text{-cuDNN} \) over cuDNN (which is equivalent to undivided) is significant when the moderate amount of workspace is set by users. For instance, if the workspace size per kernel is 64 MiB, \( \mu \text{-cuDNN} \) with the all option achieves 1.81x speedup with respect to the entire iteration, and 2.10x with respect to convolutions alone, than undivided on K80. This is because \( \mu \text{-cuDNN} \) successfully enables cuDNN to use faster algorithms, as in the example from Section IV-A. In addition, a similar speedup is achieved on P100-SXM2 (1.40x for the entire iteration, and 1.63x for convolutions alone), and on V100-SXM2 (1.47x for the entire iteration, and 1.63x for convolutions alone).

In the case where workspace size is limited to 8 MiB, \( \mu \text{-cuDNN} \) cannot attain any performance improvement, because even if the mini-batch is finely divided, the specified workspace is too small to utilize. Indeed, on P100-SXM2, only one kernel of all option seems to increase the utilization of the workspace over undivided.

On the other hand, when the workspace size limit is too large (512 MiB) on K80 and P100-SXM2 GPUs, performance difference between cuDNN and \( \mu \text{-cuDNN} \) is negligible. This is because there is no benefit from dividing the mini-batch, as all algorithms fit into the workspace constraints. However, this workspace limit consumes a considerable amount of workspace memory: While the undivided option consumes 2.87 GiB in total, all with 64 MiB limit only consumes 0.70 GiB, although with 4% overhead caused by the choice of micro-batch algorithms.

From the viewpoint of the time to optimization, including kernel benchmarking and solving DP, powerOfTwo considerably outperforms all. In particular, with 64 MiB workspace on P100-SXM2, all takes 34.16 s, whereas powerOfTwo takes 3.82 s. This result and Fig. 10 imply that powerOfTwo is a reasonable choice to test the computation efficiency of new CNNs quickly. Generally, the overhead of \( \mu \text{-cuDNN} \) is negligible with respect to the entire training time, in which the forward and backward passes are repeated hundreds of thousands of times.

2) TensorFlow: Fig. 11 presents timing breakdowns of AlexNet and ResNet-50, DenseNet-40 on P100-SXM2.

We set the (input width, output width) as (224,1000) for AlexNet and ResNet-50, or (32,10) for DenseNet-40, which are used for training ILSVRC2012 classification dataset [24] or the CIFAR dataset [25], respectively. We also set \( k \) of DenseNet-40, the number of feature maps of each convolutional layer, to 40 to obtain better computational efficiency.

Since TensorFlow 1.4.1 does not provide any workspace limits to \( \mu \text{-cuDNN} \) via cuDNN’s benchmarking functions before actual convolutions, we manually provide workspace limits of 8, 64, and 512 MiB to \( \mu \text{-cuDNN} \). \( \mu \text{-cuDNN} \) with a workspace limit of 64 MiB achieves 1.24x speedup for
ResNet-50 and 1.06x for ResNet-50. These results prove that \( \mu \)-cuDNN has good performance portability between different deep learning frameworks that depend on cuDNN.

C. Memory Consumption Using WR

Fig. 12 shows the per-layer memory usage of AlexNet and ResNet-18 on P100-SXM2. In Fig. 12, we set a per-layer workspace limit of 512 MiB for cuDNN, and 64 MiB for \( \mu \)-cuDNN, where the slowdown due to the decrease of memory limit is negligible (1.17x). These figures clearly show that \( \mu \)-cuDNN can cut down per-layer memory consumption by up to 3.43x and 2.73x on AlexNet and ResNet-18 respectively.

D. CNN Optimization Using WD

Fig. 13 shows the benchmark results of using the WD algorithm. The adjoined bars have the same workspace limit in total: For example, since AlexNet has five convolutional layers and each layer has three kernels (Forward, BackwardData, BackwardFilter), we place the result with 120 MiB WD only show the memory usage of unique convolutional layers (CONV\(_n\)) and fully-connected layers (fc or fc\(_n\)) in one forward propagation. We use a mini-batch of 256 for AlexNet and 128 for ResNet-18 respectively. We set a per-layer workspace limit of 512 MiB for cuDNN, and 64 MiB for \( \mu \)-cuDNN. Each bar segment of “WS (\( \mu \)-cuDNN)” represents the maximum workspace size of the layer.

Fig. 11: Benchmark results of different CNNs on P100-SXM2 with different workspace sizes (8, 64, 512 MiB), using TensorFlow framework. We use a mini-batch size of 256 for AlexNet and DenseNet, and 64 for ResNet-50.
Fig. 13: Benchmark results of AlexNet and ResNet-50 on P100-SXM2 with different workspace sizes and policies (WR and WD). We use a mini-batch size of 256 for AlexNet and 32 for ResNet-50. Note that the adjoined bars have the same workspace limit in total.

Fig. 14: Assigned workspace division of AlexNet on P100-SXM2. “F”, “BF”, “BD” represent kernel types (Forward, BackwardFilter, BackwardData respectively). We use a mini-batch size of 256 for AlexNet. We set a workspace limit of 8 MiB for WR, and a total workspace limit of 120 MiB for WD.

(WR, undivided). In contrast, μ-cuDNN doesn’t allocate workspace of over 3 MiB for “conv4” and “conv5”, although μ-cuDNN lists some faster and desirable configurations than the baseline. For instance, the fastest configuration of conv5 (forward), which uses FFT-based convolution with two micro-batches, is 1.29x faster than baseline, although this configuration uses 109 MiB of workspace. This observation implies that the WD does not unnecessarily allocate workspace for a specific layer but chooses the best combination, as defined by the ILP.

V. RELATED WORK

Li et. al [26] propose a heuristic to automatically tune each tensor memory layout to utilize either GEMM-based or FFT-based convolution efficiently. The proposed heuristic is, however, based on the authors’ performance observation using conventional convolutional layers and specific GPU architecture, and thus there is no guarantee that the algorithm always provides the best memory alignment for any deep neural network and GPU architecture. On the other hand, since μ-cuDNN uses the techniques of dynamic programming and integer linear programming, it is mathematically guaranteed that μ-cuDNN provides the best performance that the library can produce, provided that each convolution is independent from the others.

Rhu et al. [27] propose a memory management technique that offloads neuron activations, parameters, and errors from the GPU memory to the CPU memory during forward/backward-propagation, so that larger models can be trained with the same memory constraint. However, as Fig. 12 shows, even in such memory-efficient implementation or similar memory management techniques [28] μ-cuDNN is expected to save the peak memory usage of each layer.
Zlateski et al. [29] propose ZNNi, an FFT-based convolution algorithm, and mention micro-batching technique to reduce the temporal memory usage by FFT. μ-cuDNN, however, generalizes the schema so that micro-batching can be applied to any convolution algorithm, obtaining the best computational performance for the given layer configurations, as well as maintains high portability between different existing deep learning frameworks.

VI. CONCLUSION

In this paper, we proposed μ-cuDNN, a wrapper library for cuDNN, which divides the mini-batch to utilize high-performance convolution algorithms with limited amount of memory for workspace. We have shown that μ-cuDNN works well even with recent CNNs, which are composed of many convolutional layers, and can easily be integrated into existing deep learning frameworks.

The performance of μ-cuDNN demonstrated in our work suggests that other layer types can be optimized as well, if they can be decomposed and computed by different algorithms. This is because μ-cuDNN does not use any special properties of the convolution operator, apart from gradient accumulation.

In addition, the result of WD optimization (Fig. 14) provides us with the insight that allocating the same workspace memory for each convolutional layer is not necessarily effective, and dynamic, adaptive assignment performs better. This observation should be beneficial for advanced deep learning frameworks that dynamically manage GPU memory to store tensors such as neuron data, weights and their gradients, for further memory optimization.

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REFERENCES

[1] A. Krizhevsky, I. Sutskever, and H. Geoffrey E., “ImageNet Classification with Deep Convolutional Neural Networks,” Advances in Neural Information Processing Systems 25 (NIPS 2012), Dec 2012.
[2] K. He, X. Zhang, S. Ren, and J. Sun, “Deep Residual Learning for Image Recognition,” in Proceedings of the IEEE Computer Society Conference on Computer Vision and Pattern Recognition (CVP 2016), Jun 2016, pp. 770–778.
[3] P. Goyal, P. Dollár, R. B. Girshick, P. Noordhuis, L. Wesolowski, A. Kyrola, A. Tulloch, Y. Jia, K. He, and P. Dollar, “Accurate, Large Minibatch SGD: Training ImageNet in 1 Hour,” CoRR, vol. abs/1706.02677, Jun 2017, https://arxiv.org/abs/1706.02677.
[4] T. Akiba, S. Suzuki, and K. Fukuda, “Extremely Large Minibatch SGD: Training ResNet-50 on ImageNet in 15 Minutes,” CoRR, vol. abs/1711.04325, Nov 2017, https://arxiv.org/abs/1711.04325.
[5] S. L. Smith, P.-J. Kindermans, and V. Q. Le, “Don’t Decay the Learning Rate, Increase the Batch Size,” CoRR, vol. abs/1711.04049, Nov 2017, https://arxiv.org/abs/1711.04049.
[6] NVIDIA. NVIDIA cuDNN. [https://developer.nvidia.com/cudnn]. Accessed on 2017-11-23.
[7] Y. Jia, E. Shelhamer, J. Donahue, S. Karayev, J. Long, R. Girshick, S. Guadarrama, and T. Darrell, “Caffe: Convolutional Architecture for Fast Feature Embedding,” arXiv preprint arXiv:1408.5093, 2014.
[8] M. Abadi, A. Agarwal, P. Barham, E. Brevdo, Z. Chen, C. Citro, G. S. Corrado, A. Davis, J. Dean, M. Devin, S. Ghemawat, I. Goodfellow, A. Harp, G. Irving, M. Isard, Y. Jia, R. Jozefowicz, L. Kaiser, M. Kudlur, J. Levenberg, D. Mané, R. Monga, S. Moore, D. Murray, C. Olah, M. Schuster, J. Shlens, B. Steiner, I. Sutskever, K. Talwar, P. Tucker, V. Vanhoucke, V. Vasudevan, F. Viégas, O. Vinyals, P. Warden, M. Wattenberg, M. Wicke, Y. Yu, and X. Zheng, “TensorFlow: Large-scale machine learning on heterogeneous systems,” https://www.tensorflow.org/, Nov 2015.
[9] Theano Development Team, “Theano: A Python framework for fast computation of mathematical expressions,” arXiv e-prints, vol. abs/1605.02688, May 2016, http://arxiv.org/abs/1605.02688.
[10] S. Tokui, K. Oono, S. Hido, and J. Clayton, “Chainer: A Next-Generation Open Source Framework for Deep Learning,” in Proceedings of Workshop on Machine Learning Systems (LearningSys) in The Twenty-Ninth Annual Conference on Neural Information Processing Systems (NIPS 2015), Dec 2015.
[11] A. Krizhevsky, “One weird trick for parallelizing convolutional neural networks,” arXiv preprint, vol. abs/1404.5. Apr 2014, http://arxiv.org/abs/1404.5997.
[12] M. Mathieu, M. Henaff, and Y. LeCun, “Fast training of convolutional networks through FFTs,” in International Conference on Learning Representations (ICLR 2014), Apr 2014.
[13] Facebook. Caffe2. [https://caffe2.ai/]. Accessed on 2017-11-23.
[14] G. Szegedy, W. Liu, Y. Jia, P. Sermanet, S. Reed, D. Anguelov, D. Erhan, V. Vanhoucke, and A. Rabinovich, “Going deeper with convolutions,” in Proceedings of the IEEE Computer Society Conference on Computer Vision and Pattern Recognition (CVPR 2015), vol. 07-12-June, Jun 2015.
[15] A. Mahkorni. GLPK (GNU Linear Programming Kit). [https://www.gnu.org/software/glpk/]. Accessed on 2017-11-23.
[16] NVIDIA. NVIDIA Caffe. [https://github.com/NVIDIA/caffe]. Accessed on 2017-11-23.
[17] ——. Tesla K80 HPC and Machine Learning Accelerator. [http://www.nvidia.com/object/tesla-k80.html]. NVIDIA. Accessed on 2017-11-23.
[18] ——. Tesla P100 Most Advanced Data Center Accelerator. [http://www.nvidia.com/object/tesla-p100.html]. Accessed on 2017-11-23.
[19] ——. NVIDIA Tesla V100. [https://www.nvidia.com/en-us/data-center/tesla-v100/]. Accessed on 2018-3-1.
[20] The TensorFlow Authors. tensorflow/models. [https://github.com/tensorflow/models]. Accessed on 2018-3-1.
[21] G. Huang, Z. Liu, L. van der Maaten, and K. Q. Weinberger, “Densely connected convolutional networks,” in Proceedings of the IEEE Computer Society Conference on Computer Vision and Pattern Recognition (CVPR 2017), Jul 2017.
[22] The TensorFlow Authors. tensorflow/benchmarks. [https://github.com/tensorflow/benchmarks]. Accessed on 2018-3-1.
[23] A. Lavin and S. Gray, “Fast Algorithms for Convolutional Neural Networks,” in Proceedings of the IEEE Computer Society Conference on Computer Vision and Pattern Recognition (CVPR 2016), Jun 2016, pp. 4013–4021.
[24] O. Russakovsky, J. Deng, H. Su, J. Krause, S. Satheesh, S. Ma, Z. Huang, A. Karpathy, A. Khosla, M. Bernstein, A. C. Berg, and L. Fei-Fei, “ImageNet Large Scale Visual Recognition Challenge,” International Journal of Computer Vision, no. 3, pp. 211–252, 2015.
[25] A. Krizhevsky, “Learning Multiple Layers of Features from Tiny Images,” [https://www.cs.toronto.edu/~kriz/learning-features-2009-TR.pdf]. Tech. Rep., Apr 2009.
[26] C. Li, Y. Yang, M. Feng, S. Chakradhar, and H. Zhou, “Optimizing Memory Efficiency for Deep Convolutional Neural Networks on GPUs,” in Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis (SC ’16). Piscataway, NJ, USA: IEEE Press, Nov 2016, pp. 54:1-54:12.
[27] M. Rhu, N. Gimelshein, J. Clemons, A. Zulfiqar, and S. W. Keckler, “vDNN: Virtualized deep neural networks for scalable, memory-efficient neural network design,” in 2016 49th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO 2016), Oct 2016.
[28] K. Shirahata, Y. Tomita, and A. Ike, “Memory reduction method for deep neural network training,” in Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis (SC ’16). Piscataway, NJ, USA: IEEE Press, Nov 2016, pp. 54:1-54:12.
[29] A. Zlateski, K. Lee, and H. S. Seung, “ZNII: Maximizing the Inference Throughput of 3D Convolutional Networks on CPUs and GPUs,” in
