Evaluation and Improvement of a Transformerless High-Efficiency DC–DC Converter for Renewable Energy Applications Employing a Fuzzy Logic Controller

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Abstract: This article discusses a transformer-free, high-efficiency DC–DC converter besides renewable energy applications. The traditional buck–boost, classic Zeta, Sepic, and Cuk converter does have the benefits of a simple design, low cost, as well as the capacity to execute voltage step-up and step-down. Conversely, because of the detrimental consequences of the parasitic constraints of the device, the voltage conversion gain of the traditional DC–DC converter is much more restricted, and the efficiency is also significantly smaller, whereas this proposed converter does have a higher voltage gain and efficiency because it is used in a single power switch, resulting in reduced switching losses and voltage stress. The said converter’s design is very simple, which simplifies the operation control and reduces switching and conduction losses, leading to an efficiency of 97.4%. This converter seems to have the same capabilities as the Zeta converter, including continuous desired output current and desired buck–boost operation. Such an article offers the operation principle and steady evaluation, as well as a comparison with other existing high step-up configurations. The proposed converter employs a fuzzy logic controller, which improves the voltage level as well as reduces the time taken to set the voltage output of a conventional PI and ANN controller, especially in comparison to the FLC controller. For deployment, experimental result and MATLAB/Simulink have been used, and the modeling results indicate that the proposed controller performance has improved. The proposed approach delivers better performance with an output power of 248 W and an efficiency of 97.4%, which is comparatively better than the other converters.

Keywords: High voltage gain; Transformerless; Zeta converter; Voltage stress; Buck–boost; Fuzzy logic controller

List of symbols

| Symbol | Description |
|--------|-------------|
| $S$    | Semiconductor switch |
| $T_S$  | Time period ($1/f_{\text{switch}}$) in S |
| $V_d, V_i, V_S, V_o$ | Input & output DC voltage (V) |
| $D$    | Duty ratio (%) |
| $V_{C1}, V_{C2}, V_{C3}$ | Capacitor voltage (V) |
| $V_{D1}, V_{D2}$ | Diodes voltages (V) |
| $I_{L1}, I_{L2}, I_{L3}$ | Inductors currents (A) |
| $I_{C1}, I_{C2}, I_{C3}$ | Capacitor currents (A) |
| $M_{\text{CCM}}$ | Voltage transfer gain of CCM mode |
| CCM    | Mode of continuous conduction |
| DCM    | Mode of discontinuous conduction |
| $M_{\text{DCM}}$ | Voltage gain (in DCM mode) |
| $\tau_b$ | Time constant of a boundary normalized inductor (s) |
| $D_m$  | Duty cycle (DCM mode) |
| BCM    | Boundary conduction mode |
| $K_p$  | Proportional gain |
| $M_P$  | Maximum overshoot |
| $T_s$  | Setting time |
| $r_{DS}$ | Switch on-state resistances (ohm) |
| $R_{F1}$ and $R_{F2}$ | $D_1$ and $D_2$ diode forward resistance (ohm) |
| $V_{F1}$ and $V_{F2}$ | Diode $D_1$ and $D_2$ threshold voltages (V) |
| $R_{L1}, R_{L2} \& R_{L3}$ | The equivalent $L_1$ $L_2$ & $L_3$ inductor resistance (ohm) |
| $r_{C1}, r_{C2}, r_{C3}$ | The equivalent $C_1$, $C_2$, $C_3$, $C_0$ capacitor resistance (ohm) |
| $P_{\text{DS}}$ | The switch’s condition is loss |

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1. Introduction

The two most important energy sources seem to be fuel cells as well as photovoltaic. The voltage levels of these sources, even so, have become too small and uncertain, differing with weather patterns including solar irradiation and temperature. As a result, photovoltaic as well as fuel cell applications require high voltage gain converters [1, 2]. The inherent voltage levels of such renewable energy sources were also considerably lower and uncertain. As a result, a high boost-up converter requires maintaining and boosting the low voltage renewable input energy of the source to convert higher voltage into delivering the grid is illustrated in Fig. 1. The conventional boost converter has been commonly used due to its low hardware complexity, compact configuration, and relatively cheap. Even so, this voltage gain is insufficient. While the output voltage of a standard boost converter may theoretically reach infinite as the duty ratio reaches one, the actual voltage gain is constrained by parasitic elements and gradually decreases as the duty ratio reaches one. Most of all, the main switch must limit a rising output voltage, necessitating the use of the main switch with a rising on-resistance, which tends to increase the conduction loss. Furthermore, the diode of a conventional boost converter must also obstruct the large output voltage, creating a severe major issue with reverse recovery current as well as conduction loss [3–6].

These several improvements besides DC/DC converters are compared to provide higher voltage conversion ratios. Switched-capacitor converters are such an approach to increase the voltage gain in this case. Analyzed, the authors developed a few design guidelines helpful for achieving various switched capacitor converters. Therefore, many modular multilevel inverters depending on a switched capacitor cell theory have been described, with a soft-switched scheme that is used to reduce electromagnetic interference and switching losses. The switched capacitor methodology, on the other hand, causes the switch to suffer from serious current transient and large conduction losses. Besides that, numerous switched capacitor cells have been necessary to accomplish the incredibly large step-up conversion, increasing the circuit complexity [7–9].

Combined inductor-based converters are also another option for implementing high boost-up gain, so the combined inductor’s turn ratio could be used as further control independence to strengthen the voltage gain. Even so, when using single-phase single-stage coupled inductor-based converters, the current ripple of the input has been substantially higher. That may reduce the useful life of the insight electrolytic capacitor. However, this combined inductor converter would have had some issues with leakage inductance as well as pulsating input current [10–12]. In [13], high voltage converters have been introduced in transformerless buck–boost converters. That although the converters should not use coupling inductors. The converter’s switches and diodes had too much difficulty and stress. Thus, the converter’s losses are considerable. A high step-up converter without transformers has been addressed in [14], one main switch and capacitor technology would be used for such converters. This converter’s main objective is to improve the voltage gain, and the easiest way is to cascade the boost converter. In such a converter, only one disadvantage is that increased the switching voltage stress of the converter.

The transformerless high voltage converters were also introduced in [15], the converter has low voltage stress. The losses and high efficiency can thus be lowered. Transformerless cell-based converters were also displayed in [16], and the converter has certain benefits, including greater voltage gain, lower power diodes, and switches stresses, minimal ripples, and greater efficiency. The alternating transformer conversion method has been described in [17]. Clamps, both active and passive, are frequently utilized in those other converter topologies to lessen the burden on the switch voltage. Additional active clamping and passive clamping circuit designs were also conversely embraced to decrease the spike voltages around the active switches. A Zeta dc to dc converter of the active clamp has been displayed in [18] for zero voltage switching (ZVS). To minimize the transition, the Flyback and Zeta converters in the presented converter use the same active switches in conveys. Banaei and Bonab [19] proposes a transformerless buck–boost converter, and the converter’s voltage gain is three times that of a traditional buck–boost converter.

A buck–boost converter, incorporating KY as well as a buck converter, was introduced in [20] transformerless, to lower the power switches number to two. However, all

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| Symbol | Description |
|--------|-------------|
| $P_{Sw}$ | Switching loss of the presented converter |
| $P_{Loss}$ | Total loss of the switch |
| $P_{Loss}$ | Presented converter total loss |
| $\eta$ | Efficiency (%) |
| $\Delta V_{CI}$ | Capacitor voltage ripples (V) |
| $\tau_L$ | The normalized time constant of an inductor (s) |
| FLC | Fuzzy logic controller |
| ANN | Artificial neural network |
| $e, \, de, \, du$ | Error, change in error, control output |
| $R \, Load$ | Resistive load |
| $K_i$ | Integral gain |
| $\epsilon_{ss}$ | Steady-state error |
| $T_p$ | Peak time |
buck–boost converters achieve a high voltage gain of two. Besides, high step converters are constructed using a KY converter. The biggest limitation of the KY converter is that there have been sudden charges of some condensers in some working modes. As a consequence, current stresses have also worsened on diodes, switches, and condensers. There are some problems with implementing this major issue. In [21], this same output voltage ripple decrease has been achieved by using two Zeta DC/DC converters. However, the control operation of the Zeta converter is highly complex. A high-step converter was indeed addressed at [22] with the connected inductor. Such a converter has one primary switch as well as the stress has been lowered through the main switch. However, the voltage stress of the converter's three diodes would be high. The leakage power could be reused in this converter.

A high-step converter was also described in [23]. These same comprehensive study boost converters, as well as the voltage-double module, have been used for one such converter as well as the conversion has two main switches. High DC–DC converters are provided in [24], and the version was released. Two main switches and highly stressful diodes and switching are used for this converter. The buck–boost converters were indeed described in [25, 26] transformerless. Three switches are located on this converter. The switch’s voltage stress is equal to the converter’s output voltage in this converter. The switching and conduction losses of the converter are extremely significant. A DC–DC converter was incorporated in [27] with a transformerless buck–boost converter. There is a higher voltage gain from this converter than from the buck–boost, cuk, spice, and Zeta converters, and only one active switch is used. The converter has three inducers and displays a pulse current of the input or output. The switch and converter diode are stressful. The converter’s losses are thus high.

In [28–30], a non-coupled DC–DC inductor was introduced using two switches. In [28, 29], there was a passive switched capacitor and an active DC–DC inductor.

In spite of having many benefits, the voltage transfer gain ratio of these converters is not optimal. The serious issue of diode reverse recovery is one of the major limitations of these converters. In addition, these converters have delivered high conduction losses because of large duty ratios. A SEPIC transformer with a continuous input current was also addressed in [30], which is a transformerless high stage. Compared with construction, such converters benefit from the decreased number of objects and low-voltage pressure throughout the switches. Even so, the control complexity is increased by using two switches in the configuration.

It is suggested in this paper that a unique transformerless buck–boost converter be developed on the basis of the Zeta converter. The gain of the voltage converter is greater than that of the traditional buck–boost converter, as well as that of the Zeta, Cuk, and Sepic converters. The suggested converter topology is easy, and as a result, the converter function control is also easy. There is only one primary switch on this converter. Due to the fact that the primary switches and diode stress levels are lower than the output’s voltage, the switching loss becomes minimal, and increased efficiency also this converter. Buck–boost converters are utilized in a variety of applications, including led drivers, fuel cells, and electronic components in automobiles. An explanation analysis of the modes is provided, and experimental data are presented to verify that the converter is operating properly.

This paper is discussed as: In Sect. 2, we detailed the presented converter buck and boost functions, the operation modes of Mode I, Mode II, and Mode III, the steady-state condition of the CCM and DCM modes, voltage gain, inductor voltage and current values, BCM, efficiency, voltage stress, and calculated inductors and capacitors.
values. In Sect. 3, we detailed the design of the FLC and membership functions. In Sect. 4, we discussed the proposed converter experimental and simulation results of both boost and buck modes, and these converter results, such as efficiency and voltage gain, compared with another converter. The conventional PI controller is compared with this proposed converter. In Sect. 5, the proposed converter concluding remarks of the article.

2. The Proposed Converter

The topology of the converter’s circuit is depicted in Fig. 2 (topology). The converter is made up of a single primary (S) switch and also includes two (D₁, D₂) diodes, three (L₁, L₂, L₃) inductors, four (C₁, C₂, C₃, C₀) capacitors, and a single (R) load.

The following criteria were taken into consideration in order to simplify the analysis of the new buck–boost converter.

a. As a result, the voltages of the capacitors may be considered constant since all capacitors are of sufficient size.

b. Semiconductor components, such as diodes and switches, are the best choice for this.

The suggested converter works in both continuous and discontinuous conduction modes. The CCM has two modes. Following is a detailed examination of the CCM converter.

2.1. Mode of Continuous Conduction (CCM)

Mode 1 [t₀, t₁], the primary (S) Switch is ON and the diodes D₁ and D₂ are OFF throughout this time period. Figure 3(i) shows the current flow direction. A magnetized inductor is L₁ followed by L₂ and L₃. Capacitors C₂ and C₃ are charged, while C₁ is discharged. As a result, the appropriate formulas are as follows:

\[ V_{L1} = V_i \]  
\[ V_{L2} = V_i + V_{C1} - V_{C2} - V_{C3} \]  
\[ V_{L3} = V_{C1} + V_i - V_o \]  

Mode 2 [t₁, t₂], as illustrated in Fig. 3(ii), the current flow direction is presented. Switch S is switched OFF throughout this period. The D₁ and D₂ diodes are switched on. The L₁, L₂, and L₃ inductors are demagnetized. The inductor L₁ charges the capacitor C₁. The C₂ and C₃ capacitors discharge. Inductor voltages are derived as follows:

\[ V_{L1} = V_{C2} - V_{C1} \]  
\[ V_{L2} = -V_{C2} = -V_{C3} \]  
\[ V_{L3} = V_{C3} - V_o \]  

2.2. The Proposed Converter’s Steady-State Analysis

2.2.1. Gain in Voltage

In the case of L₁ and L₂, we can use the volt-sec balancing concept and use Eqs. (1), (2), (4), and (5), we obtain

\[
\frac{1}{T_s} \left( \int_{0}^{T_s} V_i \, dt + \int_{0}^{T_s} (V_{C2} - V_{C1}) \, dt \right) = 0
\]  
\[
\frac{1}{T_s} \left( \int_{0}^{T_s} (V_i + V_{C1} - V_{C2} - V_{C3}) \, dt + \int_{0}^{T_s} (-V_{C2}) \, dt \right) = 0
\]  

The voltage of C₁, C₂, and C₃ (V_{C1}, V_{C2}, and V_{C3}) may be obtained by using (5), (7) and (8) as follows:

\[ V_{C1} = \frac{2DV_i}{1-D} \]
Using volt seconds balance $L_3$ and (9) and (10), get the voltages transfer gain ($M_{CCM}$):

$$M_{CCM} = \frac{V_o}{V_i} = \frac{2D}{1 - D}$$

As shown in (12), the suggested converter’s voltages gain is double that of the Zeta converter. As a result, the converter’s voltage gain is greater than the Zeta converter’s. Figure 4 illustrates some of the suggested converter’s main waveforms in CCM.

As illustrated in Fig. 5, the suggested converter, Zeta and traditional buck–boost converter show the gain of the voltage. As can be observed, the suggested converter has a greater voltages transfer gain than the other converters.

### 2.2.2. Current Calculation

The average currents of the inductor $I_{L2}$, $I_{L3}$ of respective inductors $L_2$ and $L_3$ and the average currents move to the across capacitors $C_2$, $C_3$ ($I_{C2,on}$, $I_{C3,on}$) during the switch ON period time in mode 1, and the following expressions are obtained,

$$I_{L3} = \frac{(2D)V_i}{R(1 - D)}$$

$$I_{C1,on} = \left( I_{L2} + \frac{(2D)V_i}{R(1 - D)} \right)$$

Then, the mean current $I_{C1,off}$ of capacitor $C_1$ in mode 2, the following expressions are obtained,

$$I_{C1,off} = (I_{L2} - I_{C2,off} - I_{C3,off} - I_{L3})$$

Here, $I_{C2,off}$ is the mean current of $C_2$ and $I_{C3,off}$ is the mean current of $C_3$ in mode 2 on the principle of ampere sec balance on $C_1$, $C_2$, $C_3$; the expression framed is,

$$\frac{1}{T_s} \left( \int_0^{D_T} I_{C1,2,3,off} \, dt + \int_{D_T}^T I_{C1,2,3,off} \, dt \right) = 0$$

By applying the expressions (12), (13), (14), (15) in expression (16), the mean current $I_{C2, on}$ $I_{C3, one}$ of capacitors $C_2$, $C_3$, and the current $I_{L2}$ of the inductor $L_2$ are framed as below,
\[ I_{L2} = I_{C2,\text{on}} = I_{C3,\text{on}} = \frac{(2D)V_i}{R(1 - D)} \] (17)

Concerning the above-said expression (17), the mean current \( I_{C1,\text{on}} \) of the corresponding capacitor \( C_1 \) is framed as below,

\[ I_{C1,\text{on}} = \frac{(-4D)V_i}{R(1 - D)} \] (18)

About the expression (18) and Fig. 3(ii), \( I_L \), which is the mean current of the inductor \( L_1 \), is framed as,

\[ I_{L1} = I_{C1,\text{off}} = \frac{(4D^2)V_i}{R(1 - D)^2} \] (19)

Regarding Fig. 3(i), (ii) \( I_s \) which is the stress of the current across the switch (S), and \( I_{D1}, I_{D2} \) that is the current stress across \( D_1, D_2 \) diodes are framed as below,

\[ I_s = I_{L1} - I_{C1,\text{on}} = \frac{(4D)V_i}{R(1 - D)^2} \] (20)

\[ I_{D1} = I_{L2} - I_{C2,\text{off}} = \frac{V_i(2D)}{R(1 - D)^2} \] (21)

\[ I_{D2} = I_{L2} - I_{C3,\text{off}} = \frac{V_i(2D)}{R(1 - D)^2} \] (22)

Figure 6 depicts the presented converter’s, and [19] converter’s switch current stress curves. As shown, the suggested converter’s current stress is less than that of the converter in [19], implying that the given converter’s conduction loss will be minimal.

2.3. Mode of Discontinue Conduction (DCM)

DCM consists of three modes. DCM’s mode 1 is identical to CCM’s Mode 1. In Mode 2, the diodes’ currents decrease. In Mode 3, the diode current decreases to zero. The diodes are switched off in this mode. The circuit equivalent is illustrated in Fig. 7. The voltage across inductors \( L_1, L_2, \) and \( L_3 \) is zero in this condition.

About Fig. 3(ii), the summation of the mean of the diode currents can be achieved with the following expression.

\[ I_{D1} + I_{D2} = I_{L1} + I_{L2} + I_{L3} \] (23)

The mean diode currents represented as \( (I_{D1,\text{av}}, I_{D2,\text{av}}) \) of \( D_1, D_2 \) can be found by

\[ I_{D1,\text{av}} = I_{D2,\text{av}} = \frac{V_o}{R} \] (24)

The total of the average diode \( D_1 \) and \( D_2 \) during one switching time may be calculated as follows, according to Fig. 8: The duty cycle is represented as \( D_{m2} \) in Mode 2 in DCM. The summation of \( L_1, L_2, \) and \( L_3 \) gives the peak value represented as \( I_{D,\text{PK}} \)

![Fig. 6 Duty ratio versus switching current stress of the converter’s](image)

\[ I_{D,\text{PK}} = I_{L1,\text{PK}} + I_{L2,\text{PK}} = \frac{V_oDT_s}{L_e} \] (25)

where

\[ \frac{1}{L_e} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} \] (26)

By applying an inductor volt-sec balancing \( L_1, L_2, \) and \( L_3 \) duty ratio to Mode 2 in DCM \( (D_{m2}) \), the following expressions are obtained:

\[ D_{m2} = \frac{2DV_i}{V_o} \] (27)

The voltage gain \( (M_{DCM}) \) in discontinuous mode can be obtained using (23)–(27) and does \( M_{DCM} \) is provided as

\[ M_{DCM} = \frac{D}{\sqrt{\tau_L}} \] (28)

\( (\tau_L) \), which is the time constant for the normalized inductor, is obtained as

\[ \tau_L = \frac{2L_e}{RT_s} \] (29)

2.4. Analysis of Boundary Condition Mode (BCM)

The gain of the voltage in CCM and DCM becomes uniform during the working of the presented converter in BCM. The time constant \( (\tau_b) \) can be obtained using Eqs. (11) and (28), and it is represented as

\[ \tau_b = \frac{(1 - D)^2}{4} \] (30)

\( (\tau_b) \), which is the time constant curve for the boundary normalized inductor indicated in Fig. 9. The presented converter operates in continuous conduction mode when \( \tau_b \) is less compared to \( \tau_L \). Figure 10 illustrates the proposed and ZETA converters’ boundary normalized inductor time constant curves.
2.5. Analysis of Efficiency

The presented converter plays a significant role in enhancing the overall performance of the system. The efficiency of this converter is highly maximum, which is validly expounded in the subsequent part. As the switching losses are minimized by this converter, it delivers optimal output power with less duty cycle, which in turn improvises the efficiency of the converter. The parasitic resistances listed below can be used to evaluate the efficiency of the converter under consideration. $P_{DS}$, $P_{SW}$, $P_{Switch}$, $P_{D1,2}$, $P_{Cl,2,3,0}$, $P_{l1,2,3}$, $P_{loss}$. The capacitor’s inductor’s voltage ripples are not considered.

$(P_{DS})$, which is the switch $(S)$ condition loss, is given by,
\[ P_{DS} = r_{DS} I_{rms}^2 = r_{DS} \frac{4D}{(1-D)^2} I_o^2 \]  

\[ (P_{SW}), \text{ which is the switch losses of the presented converter’s, is given by,} \]

\[ P_{SW} = f_s C_s V_i^2 = f_s C_s \left( \frac{V_i}{1-D} \right)^2 \]  

\[ (P_{\text{Switch}}), \text{ which is the switch (S) the total loss is given by,} \]

\[ P_{\text{Switch}} = P_{DS} + \frac{P_{SW}}{2} \]  

\[ (P_{D1,2}), \text{ which is the loss of the diode } D_1 \text{ and Diode } D_2, \text{ is provided as} \]

\[ PD_{1,2} = R_{F1,2} \frac{1}{1-D} I_o^2 + V_{F1,2} I_o \]  

\[ (P_{C1,2,3,0}), \text{ the capacitor loss of } C_1, C_2, C_3, C_0 \text{ is obtained by,} \]

\[ P_{C1,2,3,0} = r_{C1} \frac{4DP_o}{(1-D)R} + r_{C2,3} \frac{DP_o}{(1-D)R} \]

\[ + r_{Co} \frac{(1-D)^2 R P_o}{48 L_2 f_s^2} \]  

\[ (P_{L1,2,3}), \text{ the inductor loss of } (L_1, L_2, L_3) \text{ is presented as,} \]

\[ PL_{1,2,3} = R_{L1} \left( \frac{2D}{1-D} \right) \frac{P_o}{R} + R_{L2,3} \frac{P_o}{R} \]  

The presented converter’s total loss \( (P_{\text{loss}}) \) is obtained as,

\[ P_{\text{Loss}} = P_{\text{Switch}} + \sum_{i=1}^{2} (P_{RF})_{Du} + \sum_{i=1}^{2} (P_{VF})_{Du} \]

\[ + \sum_{i=1}^{3} P_{RCa} + P_{RCa} + P_{RL1} + P_{RL2} + P_{RL3} \]  

\[ \eta, \text{ which is the proposed converter of efficiency given by} \]

\[ \eta = \frac{P_o}{P_o + P_{\text{Loss}}} = \frac{1}{1 + \frac{P_{\text{Loss}}}{P_o}} \]  

2.6. Analysis of Voltage Stress

The most important criterion in the circuit is the stress of the voltage. Here, the switch \( (S) \) and diodes, the stress of the voltage is calculated as given below,

\[ V_s = V_i \left( \frac{1}{1-D} \right) \]  

\[ V_{D1} = V_{D2} = \frac{V_i}{1-D} \]  

According to (39) and (40), the diodes’ and switch’s voltage stresses are well below the output voltage. The suggested converter’s normalized voltage stress is compared to the ZETA converter in Fig. 11. Because the ZETA converter’s normalized voltage stress is greater than that of the presented converter, it is possible to choose a switch with a low conduction loss.

2.7. Capacitors Across the Voltage Ripple Calculation

A voltage ripple is formed by \( C_1 (\Delta V_{C1}, \Delta V_{C1,\text{ESR}}) \) from the current that is in equivalent series resistance (ESR) which is shown in Fig. 12. Another voltage ripple \( (\Delta V_{C1,\text{cap}}) \) is formed by \( C_1 \) due to the discharging and charging mode of the capacitor. The capacitors \( C_2, C_3 \) of voltage and current waveform are shown in Fig. 13.
Thus, the capacitor $C_1$ voltage ripple can be framed as given below,

$$\Delta V_{C1} = \Delta V_{C1,ESR} + \Delta V_{C1,\text{cap}}$$  \hspace{1cm} (41)

$\Delta V_{C1,ESR}$ is given by,

Fig. 14 FLC simplified diagram

Fig. 15 Membership functions, a e, b de, c du

Fig. 16 Control surface of the FLC
where

\[
\text{ESR}_{C1} = \frac{\tan \delta_{C1}}{2\pi f_s} \tag{43}
\]

Capacitor \( C_1 \)'s dissipation factor \( \tan \delta_{C1} \).

\[
\Delta V_{C1,\text{cap}} = \frac{I_{C1,\text{on}} DT_s}{C_1} = \frac{2DT_s V_o}{RC_1} \tag{44}
\]

Likewise, \( \Delta V_{C2,3} \) which is a capacitor \( C_2 \) and \( C_3 \) voltage ripple is given by,

\[
\Delta V_{C2,3} = \Delta V_{C2,3,\text{ESR}} + \Delta V_{C2,3,\text{cap}} = \frac{ESR_{C2,3}(2D)V_i}{(1 - D)^2 R} + \frac{DT_s V_o}{RC_{2,3}} \tag{45}
\]

2.8. Inductors and Capacitors Design

In CCM, the theoretical \( L_1, L_2, L_3 \) inductors derived values as follows:

\[
L_1 \geq \frac{V_o (1 - D)^2}{8Df_i f_s} \geq \frac{90(1 - 0.53)^2}{8 \times 0.53 \times 2.8 \times 40 \times 10^3} = 42 \mu\text{F} \tag{46}
\]

\[
L_2,3 \geq \frac{V_o (1 - D)}{4Df_i f_s} \geq \frac{90(1 - 0.53)}{4 \times 2.8 \times 40 \times 10^3} = 94 \mu\text{F} \tag{47}
\]

In CCM, the theoretical \( C_1, C_2, C_3, C_o \) capacitors derived values as follows:

\[
C_1 \geq \frac{2DT_s V_o}{R A V_{C1}} \geq \frac{2DV_o}{R \times 0.01 \times V_o \times f_s} \geq \frac{32 \times 0.01 \times 90 \times 40 \times 10^3}{2 \times 0.53 \times 90} = 83 \mu\text{F} \tag{48}
\]

\[
C_{2,3} \geq \frac{DT_s V_o}{R A V_{C2,3}} \geq \frac{DV_o}{R \times 0.01 \times V_o \times f_s} \geq \frac{32 \times 0.01 \times 90 \times 40 \times 10^3}{0.53 \times 90} = 41 \mu\text{F} \tag{49}
\]

\[
C_o \geq \frac{V_o (1 - D)}{16L_2 f_s^2 A V_{C_o}} \geq \frac{100(1 - 0.53)}{16 \times 0.001 \times (40 \times 10^3)^2 \times 1} = 1.8 \mu\text{F} \tag{50}
\]
3. The Fuzzy Logic Controller (FLC) Algorithm

FLC is a technique that is utilized in nonlinear systems. It derives the ideas of various experts and uses mathematical principles to resolve various complex issues with much simpler calculations. FLC completely depends upon linguistic control variables. FLC is similar to human thinking, and thus, it reduces the gap between mathematical calculation and human thinking. FLC has three steps. The first step is fuzzification, followed by fuzzy inference and finally by defuzzification.

In the case of the PI controller, there are no orderly schematic procedures for the design of an FLC. However, the common schematic diagram of the FLC is shown in Fig. 14. By comparing the actual values with their reference values at every interval, the change in error (Δe) and
error ($e$) is obtained for all loops which are provided as input for FLC to achieve the control output ($u$) [31]. By altering the duty cycle, the voltage of the output of a transformerless high-efficiency DC to DC converter is controlled. When compared with output voltage values with reference voltage values, this time is obtained by the error value. Here, the voltage of reference is given as $r(k)$, and the obtained voltage of the output is given as $y(k)$. From the following Eq. (51), the error voltage can be calculated.

$$e(k) = r(k) - y(k)$$  \hspace{1cm} (51)

From the below equation, the change in the error voltage can be calculated

$$\Delta e(k) = e(k) - e(k - 1)$$  \hspace{1cm} (52)

In the first step, when $e(k)$ is positive (‘+’) and $\Delta e(k)$ is considered negative ‘−’, the error becomes ‘+’ and lowers down to zero. To reduce the error, $\Delta u$ is made positive. The error becomes negative and goes on decreasing when the $(k)$ is ‘−’ and $\Delta e(k)$ is made ‘+’. $\Delta u$ is applied to stop the error from further decreasing from negative. [32]

3.1. The Internal Structure of the Fuzzy Controller

Here, Mamdani-type fuzzy inference has been applied. The simulation circuit of the entire FLC is given in Fig. 15. The two inputs ($e, de$) and output ($du$) are provided in the FLC as illustrated in Fig. 15a–c.
Using the five membership function tables, the inputs ($e$, $de$) are framed as values of fuzzy. Trapezoidal and triangle methods of membership function are applied here because of their efficiency and simplicity in implementation. Below are the abbreviations of the membership functions.

1. NB $\leftrightarrow$ Negative Big
2. NL $\leftrightarrow$ Negative Low
3. Z $\leftrightarrow$ Zero
4. PL $\leftrightarrow$ Positive Low
5. PB $\leftrightarrow$ Positive Big

For the provided inputs, the membership functions that are designed are illustrated in Fig. 16a, and Fig. 16b as PWM oscillations are suppressed by the trapezoidal function Z, it is used here and the output is shown in Fig. 16c.

Upon experience, the rules are framed for the fuzzy system. The rules are represented in symmetric matrix skew form in Table 1. It has twenty-five rules derived from twenty-five input combinations.

Some of the fuzzy rules are explained below.

When $de$ and $e$ are PB, then $du$ is PB,
When $de$ is PL and $e$ is PB, then $du$ is PB,
When $de$ is NB and $e$ is PB, then $du$ is Z.
When $de$ is NB and $e$ is PL, then $du$ is NL.
When $de$ is NB and $e$ is Z, then $du$ is NL.

One more rule is added to improve the transient response. The rule is given below.

When $e$ is PB, then $du$ is PB.
4. Simulation and Experimental Results

The gate pulses to the active power switch $S$ are generated by a PWM generator using MATLAB/Simulink 19 with a switching 40 kHz frequency of as shown in Fig. 17.

The simulation results show that the oscillation in the steady state at the highest power point is minimal resulting in less energy loss and higher system efficiency, and this section discussed the evaluation and performance of the FLC controller-based transformerless high-efficiency dc to dc converter. The proposed converter results of the simulation are given in both step-up (boost) and step-down (buck) modes, and a comparison between the PI, ANN controllers and the proposed FLC-based controllers is shown in the following sections. Table 2 lists the components utilized in the proposed converter.

4.1. The Output of the Boost Mode

Figures 18 and 19 illustrate the waveforms of the voltages at the input and output, as well as of the input and output power, as well as of the input and output current, inductor currents, capacitor voltages, diode voltages, current and power switch voltages, in this case, the boost mode.

When triggering the switch at 40 kHz frequency with an input 36 V voltage, the outputs voltage is obtained as 89 V, as it is shown in Fig. 18(i). The output current of 2.8 A with the output power of 248 W is shown in Fig. 18(ii), and the input current of 7.06 A with the input power of 254.4 W is shown in Fig. 18(iii).

The switch is in ON time in the CCM mode, the energy is stored in the inductors $L_1$, $L_2$, $L_3$ by the input source, and while the switch is in the OFF position, the inductors discharge it. The inductor currents produced are 6.3 A, 2.4 A, 2.4 A for inductors $I_{L_1}$, $I_{L_2}$, and $I_{L_3}$, respectively, which are shown in Fig. 19 (i). The corresponding inductor waveforms of period time of 0–0.5 s and this inductor current from the zoomed viewpoint period time 0.3–0.3008 s are also shown in Fig. 19(i).

The voltage and current waveform of diodes $D_1$ and $D_2$ are similar and these respective diode voltages $V_{d_1}$, $V_{d_2}$ are 78 V and diode currents $I_{d_1}$, $I_{d_2}$ are 6.5 A are shown in Fig. 19(ii), and this diode voltage and current of zoomed viewpoint waveforms also shown in Fig. 19(ii).

The various waveforms of capacitor $C_1$, $C_o$ and $C_2$, $C_3$ are similar, and these respective capacitors voltages $V_{c_1}$ = $V_{c_o}$ = 90 V and $V_{c_2}$ = $V_{c_3}$ = 44 V are shown in Fig. 19(iii). And this capacitor voltage of zoomed viewpoint is also shown in Fig. 19(iii). The voltages waveforms across the switch voltages $V_S$ are 78 V, and this zoomed viewpoint is also shown in Fig. 19(iv).

![Fig. 22 Experimental converter setup and prototype](image-url)
Fig. 23 Experiments performed in boost mode (in CCM). Time: 50 us/div) (i) output voltage (20 V/div), (ii) output current (1 A/div) (iii) inductor $L_1$ current (1 A/div) (iv) inductor $L_2$ current (1 A/div) (v) inductor $L_3$ current (1 A/div) (vi) diode voltage $D_1, D_2$, voltage across the switch $V_s$ (10 V/div)
Fig. 24 Experimental results in buck mode (time: 50 us/div). (i) Output voltage (5 V/div), (ii) output current (500 mA/div) (iii) inductor $L_1$ current (500 mA/div) (iv) inductor $L_2$ current (500 mA/div) (v) inductor $L_3$ current (500 mA/div)
4.2. Waveforms of Buck Mode

In the buck mode, the output current and output voltage obtained are 0.54 A and 17.3 V, respectively, which is shown in Fig. 20(i). The three inductor currents $I_{L1}$, $I_{L2}$, $I_{L3}$ obtained are 1.3 A, 0.6 A, 0.6 A, respectively, and the respective waveforms are shown in Fig. 20(ii), and this inductor’s current zoomed view also is shown in Fig. 20(ii). The two diodes current and voltage waveform of $D_1$ and $D_2$ are similar and their respective voltages $V_{d1}$ and $V_{d2}$ are found to be 17 V and currents $I_{d1}$ and $I_{d2}$ are 1.3 A as shown in Fig. 20(iii), and these diodes zoomed viewpoint of the waveform is shown in Fig. 20(iii).

In consideration with the aforementioned outcomes, it is validated that the proposed converter delivers optimum output with high accuracy, less switching stress and minimum ripples.

4.3. Comparison of the Conventional PI Controller, ANN and Proposed FLC in CCM Mode

The proposed converter-based FLC controller’s performance is compared with the performance of the conventional PI controllers and artificial neural network (ANN) [33]. The output voltage waveform is illustrated in Fig. 21.

The various parameters of time specifications for the output voltage waveform of the proposed FLC, ANN controller and PI controllers are compared in Table 3. Table 3 analyzed the overshoot of maximum output voltage, the time settling point of output voltage, the output voltage of steady-state error, and peak value, the above-mentioned parameter values of the suggested FLC controller have better performance when compared with the ANN and PI controller is shown in Table 3.

4.4. Experimental Results

Experimental data are included to validate the converter’s performance. The step-up and step-down modes of operation are supported by the presented buck–boost converter. The converter’s prototype is depicted in Fig. 22. The converter shown here has been subjected to CCM performance.

As shown in Fig. 22, a prototype of 240 W is modeled for analyzing proposed converter, and the specifications of this prototype are listed out in Table 2. For generating the gating pulses of converter switches with applicable duty ratio, the DSPIC30F2010 microcontroller is employed in this study. The fuzzy rule bases are programmed in this controller through embedded C. The converter delivers steady-state output irrespective of the load variations. Thus, it delivers high efficiency of 97.4%.

The experimental prototype is modeled for 60 V, and the outcome of the proposed converter in boost mode is displayed in Fig. 23(i), (ii). Figure 24(iii)–(v) displays the waveforms of the currents flowing through the inductors $L_1$, $L_2$, and $L_3$, correspondingly. As the hardware prototype is designed for 60 V, the inductor current values of experimental results are slightly varied from the simulation outcomes. As per (12), (17), and (19), the averaged currents through $L_1$, $L_2$, and $L_3$ inductors are 6.3, 2.4, and 2.4 A, correspondingly. The voltage waveform of diode $D_2$ is identical to that of diode $D_1$. Figure 23(vi) shows the voltage across diode $D_1$ and $D_2$. Figure 23(vi) shows the voltage across the switch $V_s$ as 20 V.

Inductors $L_1$, $L_2$, and $L_3$ have a voltage of 60 V in mode 1 and 12 V in mode 2. The step-down mode output voltage is depicted in Fig. 24(i), (ii). 12 V is the output voltage and 0.8 A output current.

Figure 24(iii)–(v) depicts the waveforms of the $L_1$, $L_2$, and $L_3$ inductors current in the buck mode of the converter. As per (12), (17), and (19), the averaged currents through $L_1$, $L_2$, and $L_3$ inductors are 1.3, 0.6, as well as 0.6 A, correspondingly. However, the hardware output waveforms of inductor current are slightly varied from the simulation outputs because the prototype is modeled for 60 V.

4.5. Efficiency Comparison of Presented Converter and other Converters in CCM Mode

The proposed converter is much efficient with an output power of 248 W shown in Fig. 18(ii), and this converter input power 254.4 W is shown in Fig. 18(iii), so both (input and output) powers are calculated and achieved by the highest efficiency of 97.4%. It is observed from the output waveforms that the presented converter has high efficiency, which is comparatively better than the other.
converters. The comparative analysis of the proposed converter with other converters is remarkably portrayed in Fig. 25. It is demonstrated that the presented converter has a significantly greater efficiency when compared to the Zeta converters and other converters in [19] and [28].

When operating in boost mode, Fig. 26(i) shows the step-up mode, efficiency vs output power, and Fig. 26(ii) shows the efficiency versus load currents in boost mode at a duty ratio of 0.53. Figure 26(iii) plots the efficiency gains from 0.35 to 0.7 with \( I_0 = 2.7 \) A versus duty ratio. Moreover, the experimental maximum efficiency is 97.1%.

In Table 5, a comparison of efficiency, voltage gain, and stress of the voltage the count of the total components used are done between the proposed converter and other converters. The presented converter has a greater voltage gain of 16 dB and greater efficiency of 97.4%, which are comparatively higher than other conventional converters. Though the number of components used in the proposed converter is slightly more when compared to other converters, it delivers maximum efficiency with less complexity, which is regarded as one of the advantageous impact of this proposed approach. In addition, the switching stress of the proposed converter is lesser than the other conventional converters.

5. Conclusion

This article describes a transformerless DC–DC converter for high-efficiency applications requiring large voltage
Table 5 A comparative analysis of the proposed converter to a range of different converters

| S. No | Converter [24] | Converter (14) [25] | ZETA converter [21] | Traditional buck-boost converter | KY converter [28] | Converter (28) [24] | Proposed converter |
|-------|---------------|---------------------|---------------------|----------------------------------|-------------------|---------------------|-------------------|
| Switches used | 2 | 2 | 3 | 1 | 1 | 2 | 1 | 1 |
| Diodes used | 4 | 2 | 3 | 1 | 1 | 3 | 2 |
| Capacitors used | 4 | 3 | 1 | 2 | 1 | 4 | 4 |
| Inductors used | 4 | 3 | 2 | 2 | 1 | 3 | 3 |
| Total component count | 14 | 10 | 10 | 6 | 4 | 10 | 12 | 10 |
| Voltage stress of the switch (V<sub>i</sub>/V<sub>in</sub>) | $V_i$ | $S_1 = \frac{1}{1-D}$ | $S_2 = \frac{1 - \frac{V_o}{V_i}}{D}$ | $\frac{V_{i+V}}{V_i}$ | $\frac{1}{1-D}$ | $\frac{V_o}{V_i}$ | $\frac{V_{i+2V_i}}{V_i}$ |
| Voltage gain | $\frac{V_o}{V_i}$ | $\frac{D}{(1-D)^2}$ | $\frac{D}{(1-D)^2}$ | $\frac{D}{(1-D)^2}$ | $\frac{D}{(1-D)^2}$ | $\frac{D}{(1-D)^2}$ | $\frac{D}{(1-D)^2}$ |
| Efficiency (%) | 94.5 | 92.5 | 96.2 | 90 | 85 | 95 | 96 |

step-down and step-up ratios. Some of the attributes could be summarized in the following points. With a moderate duty cycle, a high step-up and step-down voltage conversion ratio has been enforced. High efficiency owing to the use of reduced MOSFETs throughout the consolidated single-stage and the use of low-voltage high-performance power switches, making it an accurate frequency operation. The non-pulsating current and decreased current ripple are the results of the alternative research. Experimental result and MATLAB/Simulink tools have been used for verification as well as evaluation. The article examines the envisaged converter’s steady-state operational activities. To illustrate the effectiveness of the suggested configuration, modeling of 36–89 V 248 W converters has been designed and developed, and it accomplished a peak efficiency. A comparative analysis is done between the proposed converter and other conventional converter in terms of efficiency, switching stress and switching loss. The proposed converter provides optimal outcome with high voltage gain of 14.02 and maximum efficiency of 97.4%. This same parametric study was verified by simulated and experimental results. In the experimental analysis, the proposed converter delivers maximum efficiency of 97.1%, which is comparatively better than other traditional converters. The proposed converter employs an FLC controller strategy, and this FLC is analogized with conventional PI and ANN controllers. The FLC has a 0% overshoot with an output voltage of 89 V. In addition, it delivers quick settling time of 0.01 s with less steady-state error of 0.01 V. However, the PI controller has a 23% overshoot, 88.5 V output voltage, 0.5 V steady-state error and 0.062 s as settling time, whereas the ANN has 3.6% overshoot, 88.9 V output voltage, 0.1 V steady-state error and 0.03 s as settling time. Thus, the proposed FLC produces better performance than other controllers in terms of efficiency, output voltage, steady-state error and settling time. Existing converter technologies have an output power of 205 W, whereas the proposed converter has an output power of 248 W. Thus, the cumulative performance of the proposed approach is magnificently higher than the other approaches.

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