Research and Implementation on Wideband Receiver of LTE-Advanced Air-Interface Monitoring Analyzer

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Abstract. In this paper, the significance of LTE-Advanced (LTE-A) air-interface monitoring analyzer for LTE-A network construction and optimization are analyzed, and the physical architecture and logical architecture design of the device from the system level are introduced. In order to realize the RF signal acquisition and baseband processing of 4x4 MIMO carrier unit, a wideband receiver design scheme based on AD9361 is proposed, the scheme adopts zero-IF architecture, which has the characteristics of miniaturization, configurability, low power consumption and wideband. Then, the composition of the receiver is introduced in detail, and a digital baseband Multi-Chip Synchronization (MCS) scheme is presented. Finally, the RF receiving performance and MCS function were verified by building a test platform.

1. Introduction
With the full commercial use of LTE-A network and the explosive growth of the number of users, operators have provided users with a more superior network environment and higher speed of information services, but the resulting network quality problems are gradually increasing, the maintenance and optimization of the network put forward higher requirements. In order to improve the user's network experience, operators urgently need to use scientific testing methods to optimize LTE-A network. Since all data related to wireless resources need to be acquired from the air-interface of LTE-A network, the air-interface monitoring is performed, it has become the key to accurately locating network problems[1]. In recent years, LTE-A air-interface monitoring analyzer has become a research hotspot in the field of communication network optimization. The analyzer can perform real-time monitoring and analysis on the air-interface, which provides powerful technical support for the optimization of LTE-A network. Therefore, the research and implementation of LTE-A air-interface monitoring analyzer is of great significance for the maintenance and optimization of LTE-A network.

Figure 1. Air-Interface Monitoring Technology Principle.
The LTE-A air-interface monitoring analyzer is an instrument that acquires and resolves LTE-A air-interface signals. As shown in Figure 1, during the communication process between the eNodeB and the UE, the analyzer simultaneously receives the signals transmitted by the eNodeB and the UE, completes the acquisition of the signals, and performs parsing based on the standardized air-interface protocol, thus exhibiting signal quality and detailed communication process [2]. The monitoring analyzer is neither subordinate to the eNodeB nor to the UE, it is tested from the perspective of a third party tester. This makes the monitoring results objective and neutral, and can truly assess the possible irregularities in the actual network.

2. System Architecture Design

The system architecture of LTE-A air-interface monitoring analyzer is mainly divided into two aspects: physical structure and logical structure.

2.1. The physical architecture of the analyzer

As shown in Figure 2, according to the physical architecture, the LTE-A air-interface monitoring analyzer is composed of a Receive Antenna Matrix Chassis, 10 Radio Frequency Baseband Boards (RFBB), a Layer Two Processing Board (L2B), a System Clock Board (SYSCLKB), a PXI Controller Board and a Chassis Backplane.

![Analyzer Structure Diagram](image)

**Figure 2. Analyzer Structure Diagram**

The following describes the functions of each part:

**Receive Antenna Matrix Chassis**: Completes 4x4 MIMO reception, each antenna is passed through a splitter and divided into 10 outputs, which are respectively connected to the RF input terminals of 10 RF baseband boards;

**RFBB**: Completes RF and baseband processing of a 4x4 MIMO carrier unit, including four RF channel acquisitions of the same frequency, baseband demodulation, channel decoding, and recovery of baseband data; Transmits the baseband data to L2B directly by DMA mode through PCIE bus; Completes the storage of the 4 channels of IQ data; Receives the commands from the PXI controller;
Completes the modification and inquiry of the channel, mode and configuration parameters; Receives the clock information of the system clock board, and completes the clock synchronization.

**L2B**: Receives data from the RFBB, Completes protocol decoding of MAC, RLC and PDCP; Writes the processed data to the PXI controller memory through DMA; Receives instructions from the PXI controller to complete configuration parameters modification and query.

**PXI Controller Board**: It is a computer board with CPU, memory, hard drive and various peripherals. It integrates a PCIE SWITCH and is connected to the backplane. It receives data from the L2B, completes the decoding synthesis of the RRC and NAS layers; completes the protocol analysis of the IP and application user planes; implements the user interface, supports parameter configuration, query, and real-time data display.

**SYSCLKB**: Provides 0.1ppm 10MHz clock source for each daughter board of the device; Supports external 10MHz clock input and 10MHz clock output; Receives the clock of the external GPS receiver and synchronizes to the device clock; Provides clock synchronization for the RFBB signal; Extends a 100/1000 Base-X fiber interface through PCIE.

**Chassis Backplane**: Multiple PCIE SWITCHs are integrated on the backplane, and these SWITCHs on the backplane are connected to each other through SWITCH in the PXI controller board. The RFBB, the L2B, and the SYSCLKB are connected to the backplane PCIE SWITCH through the socket, thereby implementing PCIE interconnection communication between the boards.

![PCIE data flow direction](image)

**Figure 3.** PCIE data flow direction

As shown in Figure 3, the data flow direction of each board is shown, and 10 RFBBs use peer-to-peer (P2P) to simultaneously write data to the L2B. The peak rate of a single RF baseband board is 200 Mbps; The L2B uses DMA mode to write data to the PXI controller at a peak rate of 2 Gbps; There is also a small amount of control query information interaction between the PXI controller and other sub-boards.

### 2.2. The logical architecture of the analyzer

As shown in Figure 4, according to the logical architecture, LTE-A monitoring analyzer consists of Layer 1 (L1) processing, Layer 2 (L2) processing, master drive interface, Layer 3 (L3) and business processing, scheduling control, user interface, clock management. Each part is introduced below.

1. **The L1 processing** module is located on the RFBB to perform the LTE-A physical layer analysis of a single carrier in a single direction.
2. **The L2 processing** module is located on the L2B, and completes protocol analysis of the PDCP layer, the MAC layer, and the RLC layer, and includes carrier aggregation reception.
3. **The master drive interface** module is located on the PXI controller board, and provides an interface for the upper layer to access the L1 processing module and the L2 processing module.
4. **The L3 and business processing** module are located on the PXI controller board, complete the decoding synthesis of the RRC layer and the NAS layer, and complete the protocol resolution of the IP and application layer user planes.
(5) The **scheduling control** module is located on the PXI controller board, the configuration and query of the L1 processing module, the L2 processing module, and the clock management module are completed according to the configuration of the user interface. The parsed information is fed back to the L1 processing module and the L2 processing module in time. In the scan state, based on the feedback of L1, a judgment, a selection, and then a configuration schedule are performed.

(6) The **user interface** module is located on the PXI controller board, which completes the control interface of user operation and displays the parsed data.

(7) The **clock management** module is located on the SYSCLKB to complete the clock switching and status query.

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**Figure 4.** The logical architecture of the analyzer.

3. **Wideband RF Receiver**

During the communication between UE and eNodeB, the RF receiver board simultaneously receives both uplink and downlink signaling and data from the air-interface, completes the acquisition of signaling and data, and then converts it into a digital baseband signal that can be used by the baseband board. The baseband board performs baseband demodulation, channel decoding, and then recovers the baseband data. In order to meet the requirements of wideband, software configuration, miniaturization and low cost of LTE-A monitoring analyzer RF receiver, this paper designs a wideband receiver based on AD9361 and presents a MCS scheme.

3.1. **Introduction of AD9361**

The AD9361 is a highly integrated RF agile transceiver based on zero-IF architecture. It combines a RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers and provides a configurable digital interface to a processor. The AD9361 operates in the 70MHz to 6.0GHz range, covering all TD-LTE and FDD-LTE bands specified by the 3GPP. It integrates two receivers and two transmitters with a direct conversion architecture, the two receivers have very good linearity and noise figure, and independent automatic gain control (AGC), dc offset correction, quadrature correction and digital filtering. Each receiver contains two high dynamic range 12-bit analog-to-digital converters that digitize the received analog signals[3].

3.2. **Wideband RF Receiver Board Based on AD9361**

The RF baseband board is divided into two parts: the RF board and the baseband board. The two are connected by the high-speed connector of SAMTEC[4]. As shown in Figure 5, the RF
baseband board is based on AD9361 and ZYNQ. The AD9361 chip receives the RF signal and the ZYNQ chip processes the baseband signal.

The radio frequency board has three parts:

1. RF receiving module: mainly composed of Low Noise Amplifier (LNA), Digital Attenuator (DATT), filter and two AD9361 chips. Two AD9361 chips complete the acquisition of RF signals and down-conversion processing of four channels, as shown in Figure 6.

2. Power module: converts the 3.3V and 12V power supplies to the required voltage to provide power supply for the RF board.

3. Clock BUFFER: converts the 60 MHz (LVDS) clock from the baseband board to the RF board into two CMOS clocks, which are sent to two AD9361 chips as external reference clocks.

3.3. Digital Baseband Multi-Chip Synchronization

This board is a 4x4 MIMO RF front-end. Two AD9361 chips complete the acquisition of four RF channels. When multiple AD9361 chips are used for MIMO, multi-chip synchronization operations are required[5]. Since the RF board is connected to the baseband board through the SAMTEC high-speed connector, the AD9361 chip transmits the output I/Q quadrature baseband component to the baseband board for demodulation processing through the connector. Each AD9361 chip generates
a digital signal DATA and a synchronous clock CLK_OUT. Although the synchronous clock CLK_OUT achieves the clock homology, since the passing network link may not be equal in length, there will be a certain error in its phase, so the digital signal sampling of the two AD9361s is not synchronized. The AD9361 provides a trigger interface SYNC_IN for simultaneous sampling of digital signals, which can be used to realize multi-chip synchronization. At this point, a synchronous trigger signal SYNC of the FPGA is used to calibrate the phase error. The reference clock of the FPGA and the reference clock of the two AD9361s are from the same reference clock source. When the rising edge of SYNC comes, the AD9361_0_CLK_OUT and AD9361_1_CLK_OUT will be aligned after the same delay time on the rising edge of SYNC, and the multi-chip synchronization is completed. As shown in Figure 7.

\[ \Delta \varphi \]

**Figure 7. Multi-Chip Synchronization**

4. **Testing and Verification**

Aiming at the LTE-A air-interface monitoring analyzer proposed in this scheme, a test and verification platform is built. The analyzer and the algorithm of multi-chip synchronization technology is tested and verified. The test and verification platform is shown in Figure 8.

**Figure 8. Test and verification platform**

Connect the device according to Figure 8, reset the base station emulator CMW500, set the Operating Band to Band3, the Downlink Channel to 1575, the Frequency to 1842.5MHz, the Cell Bandwidth to 10MHz, and the power to -30dBm. The analyzer is triggered for analysis. The result show that the analyzer can acquire and analyze the downlink bandwidth, PCI, MIB, SIB1 of the corresponding cell. The results are shown in Figure 9.
5. Conclusion
Firstly, this paper explains the significance of LTE-A air-interface monitoring analyzer for LTE-A network construction, maintenance and optimization, and then introduces its system architecture and logic architecture in detail. In order to complete the air-interface signaling and data acquisition of four RF channels, a design scheme of wideband RF receiver board based on AD9361 is proposed, and a digital baseband multi-chip synchronization method for MIMO with multiple AD9361 chips is presented. Finally, the RF receiving performance and multi-chip synchronization method of LTE-A Air-port monitoring analyzer are tested and verified. The test results show that the design of RF card of LTE-A Air-port monitoring analyzer is reasonable.

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References
[1] P.K.Fu, Z.Z.Zhang, “Z.He.System, Design of LTE-Advanced Air-Interface Monitoring Instrument”[J]. Video Engineering, 2015, 39(15):46-50.
[2] W.B.Xu, Z.Z.Zhang, Z.He , “Design and Implementation of PDCP Protocol in LTE-A Air Interface Monitoring Instrumentation”[J].Video Engineering, 2015,39(17):64-68.
[3] Analog Devices,Inc.RF Agile Transceiver AD9361 Data Sheet [EB/OL] https://www.analog.com/media/en/technicaldocumentation/data-sheets/AD9361.pdf,2013.
[4] T.Shi, W.Guo, L.Yang, et al. “Remote wideband data acquiring system based on ZC706 and AD9361”[C]. Wireless Symposium. IEEE, 2015:1-4.
[5] Analog Devices, Inc.AD9361 Reference Manual UG-570 [EB/OL].www.analog.com, 2014.