A CMOS Active Rectifier with Time Domain Technique to Enhance PCE

Shao-Ku Kao

Abstract: This paper presents a CMOS active rectifier with a time-domain technique to enhance power efficiency. A delay compensation circuit was designed using a time-domain technique. It converts the delay buffer’s delay time to a voltage value. The voltage is able to control on/off time in the comparator for variable input voltage. This circuit is designed in 0.18 m CMOS process. The input voltage range is from 2 V to 3.8 V with the output voltage from 1.8 V to 3.6 V. The efficiency can be maintained at more than 83% when the load is from 100 Ω to 1300 Ω for 3.3 V input voltage. The maximum efficiency is 90.3% at output power to be 109 mW for 3.3 V input voltage.

Keywords: wireless power transfer; delay compensation; phase error detector; current compensation; PCE

1. Introduction

In recent years, various wireless technologies have played an important role in our day-to-day life, especially in wireless power transfer (WPT) systems. They provide power without using a physical cable and are easier to use. They are reliable, efficient, fast, low in maintenance cost and can be used at short range or long range. To address the frequency of wireless power transfer, an analysis has reported that the transfer efficiency increases with higher frequency [1]. However, the energy attenuation increases over about 20 MHz due to the energy absorption of the human tissue. A frequency from 1 MHz to 13.56 MHz is recommended. Thus, the inductive link power transfer is suitable for this high frequency at 13.56 MHz. The volume and area of the LC resonance decreases with higher transfer frequency, which contributes to the shrink the volume and area for wireless power-implantable medical devices (IMDs). WPT is widely used in IMDs such as pacemakers [1], neural recording implants [2], cochlear [3] and retinal prostheses [4]. For these implants, a long-term reliable battery is an important issue in IMDs. In addition, IoT nodes can also be powered by WPT [5]. Therefore, WPT is a suitable solution for recharging a battery to sustain the power supply without surgeries for battery replacements. In IMD applications, the power supply range varies from 10 mW to 100 mW according to the types of implants. The WPT system is shown in Figure 1. On the receiver side, the received AC voltage ($V_{AC1}$ and $V_{AC2}$) is first converted to a DC voltage $V_{DC}$ by the active rectifier [6–13]. The power conversion efficiency of the active rectifier plays an important role in the wireless power transmission system. The wireless power transmission system is applied in implantable medical products and many portable electrical devices. In addition, the wireless power transmission system replaced the traditional way to charge implantable medical devices.
Improving the power conversion efficiency (PCE) of wireless power transmission systems over a wide input voltage range is an important issue. The active rectifier with control pulse ($V_{GN1}$ and $V_{GN2}$) is shown in Figure 2a. The active diode ($M_{N1}$, $M_{N2}$) adapted on the active rectifier is due to the constant voltage drop of a Schottky diode, which is typically between 0.14 V–0.45V. This device is favored for low-power systems, but for integrated circuits, these require costly fabrication processing and are highly dependent on temperature. The differential fully cross-coupled rectifier has the reverse characteristic of the rectifying devices because the rectifying cross-coupled transistor is still a bidirectional device. The active rectifier always operates at near-optimum conditions with buffer delay elimination to significantly enhance the PCE if the $V_{GN1}$ and $V_{GN2}$ signals drive $M_{N1}$ and $M_{N2}$ in the incorrect time. The on-and-off propagation delay time of the comparator and buffer causes the power transistor ($M_{N1}$ and $M_{N2}$) to turn on and off at incorrect times which will reduce the PCE. For example, in Figure 2b, during the ON propagation delay, this leads to a decrease in the charge time of the rectifier. For the OFF propagation delay, it induces reverse leakage current on the power MOS, as shown in Figure 2b. Figure 2b shows the simulation result of the reverse current. It is crucial to solve the on/off propagation delay problem, even when the delay time varies by input amplitude.

Until now, many kinds of techniques for delay compensation have been proposed [6–18]. In this work [9], both input signal $V_{AC}$ and ground voltage (VSS) are fed to the error amplifier (EA) for comparison. The error voltage controls the injected current to the push–pull comparator use to compensate the delay. As the feedback loop is stable, it can generate a stable voltage to set the offset current. In Reference [9], the $V_{AC}$ is larger/smaller than VSS, which indicates the NMOS turn off to late/early, and Voffset-off is decreased/increased to allow offset current to turn off NMOS earlier/later. In Reference [10], the feedback-type operational transconductance amplifier (OTA) is replaced with the error amplifier. In this work, it is implemented with a control logic circuit to control the timing of the comparison. The value of $V_{AC}$ is a sample and is passed to the OTA and compared with VSS. The output voltage ($V_{ea\_off}$) of OTA adjusts the offset current of the comparator. After several cycles, $V_{ea\_off}$ is adjusted to the steady-state value. For both EA and OTA, it is very slow, and it costs many input cycles to calibrate the correct voltage. In Reference [11], the power stage contains two cross-coupled PMOSs and two power NMOSs (MNA and MNB) controlled by adaptive-delay time control (ADTC) by sensing the input AC signal. The ADTC generates the delayed pulses for power NMOS by tracking the optimal on/off time. The optimal on/off time of the power switches is generated by two current-controlled delay lines (CCDLs) in the ADTC. Therefore, the rising edge and falling control signal of the power NMOS are generated by the delay-line method rather than using the continuous-time comparator. In Reference [13], the control pulse of the power transistor is generated from the digital circuit. The digital circuit is able to control the on/off delay compensated in the active rectifier. The compensation current’s on-current and off-current are injected into the comparators, when they are needed, to reduce the buffer’s delays. A single-comparator architecture and auto-calibration mechanism are implemented in Reference [14]. The falling edge of the gate driving signal should be located at the zero-crossing point of the comparator’s input to prevent reverse current. The auto-calibration mechanism circuit senses the time error in
which the output of the comparator is away from the zero-crossing point. In Reference [15], a two-step coarse- and fine-tuning circuit is implemented for shifting the voltage level of the comparator’s input signal. The coarse/fine-tuning block generates digital control signals to adjust the current mirror arrays according to the detection signals. The offset current of the current mirror array could be tuned up or tuned down for a wide delay compensation range. The propagation delay of comparators and buffers is relative to the rail-to-rail supply voltage. In Reference [16], the lower supply rail is provided by the double-pass regulator that shifts the lower supply level from zero voltage to 1.4 V. With this technique, lowering the rail-to-rail supply voltage can improve the delay time of the comparator and buffers. The 3.3 V transistor devices in the comparators and buffers are replaced with 1.8 V devices that can reduce gate capacitance and ON resistance of the transistor. In Reference [17], the dual-loop adaptive delay compensation circuitry for fine control and coarse control is used to adjust the offset of comparator. The initial is set with fine control to provide a smaller level offset current. For fine control, the inputs of the rectifier are sampled and fed to the error amplifier, which generates a DC offset voltage. The offset voltage is proportional to the delay time of the buffer and comparator. The coarse control compares the error voltage with high and low threshold levels for small and large compensation scenarios, respectively.

![Figure 2. (a) Active rectifier without delay calibration circuit, (b) reverse current problem.](image)

In this paper, a time-domain technique for compensated delay of the buffer in an active rectifier is proposed to enhance the PCE. The contributions from this paper are highlighted below:

- The proposed circuit is well-suited for a wide range of input voltage and loading resistors.
• A phase error detector is proposed to detect the phase difference induced by the buffers. The phase difference is converted to voltage and adaptively tracks the on/off delay time in the rectifier with variable input voltage.
• This technique can effectively overcome the problem of varied delay time by the buffer in different input voltages.
• The advantages of our circuits are with high resolution for accuracy-compensated phase difference between input and output buffer. It can generate the desired pulse to turn on/off the power MOS.

The rest of the paper is constructed as follows. The proposed active rectifier circuit is discussed in Section 2. The measurement results are illustrated in Section 3. Section 4 gives the conclusion.

2. Proposed Circuit

As shown in Figure 3, $V_{AC1}$ and $V_{AC2}$ are the input of rectifiers from the receiver coupling inductor $V_{AC}$. Following the change of $V_{AC1}$ and $V_{AC2}$, the four power MOS ($M_{N1}, M_{N2}, M_{P1}$ and $M_{P2}$) are controlled. When voltage $V_{AC1}$ is larger than voltage $V_{AC2}$, the comparator $Cmp2$ will generate a high signal to turn on $M_{N2}$, and the current passes through $M_{P1}$ to charge the output capacitance $C_L$. During another half cycle, voltage $V_{AC2}$ is larger than $V_{AC1}$, the $M_{N2}$ and $M_{P1}$ will turn off and the $M_{N1}$ and $M_{P2}$ will turn on to continue charging the rectifier output. However, as the comparators’ output passes through the buffer to turn on the power NMOS transistors ($M_{N1}, M_{N2}$), the buffer will generate a delay time to turn on/off $M_{N1}$ and $M_{N2}$. The turn-on delay time to the charge output is less than is required. The turn-off delay time leads to a reverse current problem. These delay problems may waste the power of the rectifier.

Figure 3. Active rectifier with phase error detector.

2.1. Phase Error Detector

A phase error detector is proposed to detect and compensate the on/off delay time. As shown in Figure 4, the proposed phase error detector consists of logic gates, capacitors and transistors. The phase error detector is able to detect the phase difference between $V_{C1}/V_{C2}$ and $V_{GN1}/V_{GN2}$. The phase error is converted into voltage $V_{on}$ and $V_{off}$. The operation of the phase detection is described as follows. The proposed circuit detects the phase difference between the $V_{C1}$ and $V_{GN1}$ or $V_{C2}$ and $V_{GN2}$. The signal $S_{sample\_on}$ is generated by the adjacent rising edge between $V_{C1}$ and $V_{GN1}$. The adjacent falling edge between $V_{C1}$ and $V_{GN1}$ is the generated signal, $S_{sample\_off}$. These phase differences are converted by the transistors ($M_{1A}, M_{2A}, M_{3A}, M_{1B}, M_{2B}, M_{3B}$) and generate two voltages $V_{on}$ and $V_{off}$ respectively. The voltages of the $V_{on}$ and $V_{off}$ depend on pulse width of signal, $S_{sample\_on}$ and $S_{sample\_off}$. The control signals $S_{sample\_on}, S_{sample\_off}, S_{shareA}, S_{resetA}, S_{shareB}$ and $S_{resetB}$ are
generated with logic gates as shown in Figure 4. The timing diagram of the phase error detector is shown in Figure 5. Figure 5 only presents the timing diagram to adjust the on-delay-time of the power MOS. The operation of the generated $V_{on}$ is divided into three steps. The first step, the signal $S_{sample\_on}$, turns on the $M_1$ and charges the capacitor, $C_1$, for the rising edge difference between input and output of the buffer. In the second step, the charging sharing between two capacitors, $C_1$ and $C_2$, the voltage $V_{on}$ is charged up. It is controlled by the signal $S_{shareA}$. In the third step, the voltage of $V_{sample\_A}$ is discharged by the signal $S_{resetA}$ to a zero voltage. These steps repeat themselves and generate a stable voltage $V_{on}$. The off-delay-time is the same operation procedure, but the input signal is the $S_{sample\_off}$.

![Figure 4. Phase error detector.](image1)

![Figure 5. Timing diagram of phase error detector.](image2)

### 2.2. Comparator Circuit

Figure 6a shows the comparator with current compensation transistors. The comparator is implemented with transistors M1–M8. The current compensation circuit is composed of transistors M9–M12. The two clock phases, $C_{k\_on}$ and $C_{k\_off}$, turn on transistors M10 and
M12 for injection of the current into the comparator. The \( C_{\text{on}} \) turns on M10 when the \( V_{\text{AC1}} \) starts to decrease to 0 V, until \( V_{\text{AC1}} \) is lower than 0 V. After \( C_{\text{on}} \) is turned off, \( C_{\text{off}} \) is turned on M12 until \( V_{\text{AC1}} \) becomes a high voltage. The pulse signals \( C_{\text{on}} \) and \( C_{\text{off}} \) adjust the offset voltage of the comparator. The simulated operation process of the comparator is shown in Figure 6b with a 0.18 µm CMOS process. Figure 6a shows that the simulation waveform of the proposed phase error detector generates two stable voltages, \( V_{\text{on}} \) and \( V_{\text{off}} \). These voltages give the comparators with adaptive offset the voltage to solve the delay due to the buffer. In Figure 6b, the edge of \( V_{\text{GN1}} \) is turned on earlier in each cycle, and the reverse current \( I_{\text{AC1}} \) gradually decreases.

![Comparator circuit](image_url)

**Figure 6.** (a) Comparator circuit, (b) simulation result of \( V_{\text{on}} \) and \( V_{\text{off}} \).

### 2.3. PCE Analysis and Considerations

The power conversion efficiency (PCE) is one of the important parameters in the full-wave rectifier. A simplified equivalent circuit model of an active full-wave rectifier is shown in Figure 7. The AC power supply, \( V_{\text{AC}} \), represents the AC power from the secondary LC-resonant coil. The switches represent the power NMOS transistors (\( M_{\text{N1}}, M_{\text{N2}} \)). The capacitors, \( C_{\text{g,p}} \), represent the equivalent capacitance on the power PMOS transistors. The resistors, \( R_{S} \), represent the turn-on resistance of both p-type and n-type power transistors. The output load, \( R_{L} \) and \( C_{L} \), represents the output resistance and output capacitance load, respectively. To estimate the PCE, the charge and discharge equation is given by Equations (1) and (2).

\[
Q_{\text{ch}} = C_{L} \times \Delta V = (I_{\text{RS}} - I_{\text{RL}}) \times 2 \times D \times TS \quad (1)
\]

\[
Q_{\text{dis}} = C_{L} \times \Delta V = I_{\text{RL}} \times (1 - 2D) \times TS \quad (2)
\]
where $D$ is the duty cycle, and $T_S$ is the period of the resonant frequency.

\[ \text{Figure 7. Equivalent circuit model of an active full-wave rectifier.} \]

The proposed rectifier comprises symmetrical circuits, the charge and discharge are equal and the current flows from $R_S$ and $R_L$ can be described as follows.

\[ \begin{align*}
Q_{\text{ch}} &= Q_{\text{dis}} \\
IRS &= \frac{1}{2D} I_{RL} = \frac{1}{2D} \frac{V_{DC}}{RL}
\end{align*} \]  
(3)

By calculating the current equation, the power dissipation on the proposed rectifier can be estimated as follows (Equation (4)):

\[ P_{\text{CE}} = \frac{P_{\text{Load}}}{P_{\text{Load}} + 2 \times (P_{\text{on}}, p + P_{\text{on}}, n + P_{\text{swp,cg}} + P_{\text{comp}})} \]  
(4)

In Equation (4), the $P_{\text{Load}}$ represents the output power on the $R_L$ and $C_L$, and the $P_{\text{Load}}$ is calculated according to Equation (5):

\[ P_{\text{Load}} = \frac{V_{DC}^2}{RL} \]  
(5)

Because of the full-wave structure, the switching and turn power dissipation would happen twice in a period once switching and turn power dissipation are doubled. The $P_{\text{on},p}$ and $P_{\text{on},n}$ represent the turn-on power NMOS transistors ($M_{N1}, M_{N2}$) and power PMOS transistors ($M_{P1}, M_{P2}$), respectively, and the summation of $P_{\text{on},p}$ and $P_{\text{on},n}$ can also be considered as the power consumption on the $R_S$ shown in Figure 7. The power consumption of the turn-on resistance can be calculated as

\[ \begin{align*}
P_{\text{on}, p} &= IRS^2 \times D \times Ron, p \\
&= \left( \frac{1}{2D} \frac{V_{DC}}{RL} \right)^2 \times D \times Ron, p \\
&= \left( \frac{1}{4D} \frac{V_{DC}}{RL} \right)^2 \times Ron, p
\end{align*} \]  
(6)

\[ \begin{align*}
P_{\text{on}, n} &= \left( \frac{V_{DC}}{RL} \right)^2 \times Ron, n
\end{align*} \]  
(7)

where $I_{RS}$ can be substituted by Equation (3). In Equations (6) and (7), the $R_{on,p}$ and $R_{on,n}$ represent the linear resistance of the power transistors. This resistance can be described as Equation (8).

\[ Ron = \frac{1}{\mu Cox \frac{W}{L} (V_{GS} - V_{TH})} \]  
(8)

The switching power $P_{\text{swp,cg}}$ includes the buffer and the comparator in the proposed rectifier. The switching power $P_{\text{swp,cg}}$ has a switching frequency $f_s$ and creates a path for current to charge or discharge the capacitance on the power transistors $C_{g,p}$. The switching
power can be described by Equation (9). The power consumption of the comparator is eliminated.

\[ P_{swp, cg} = C_g, p \times V_{DC}^2 \times f_s \]  

(9)

Figure 8 shows the power consumption pie chart of the post-simulation result. This result is simulated under the output load, 300 Ω, and the input VDC is 3.3 V, which is the highest PCE situation. This simulation includes the parasitic capacitance in the layout, so the power consumption of the inverter is closer to the real chip. The 0.18 μm process includes 1.8 V/3.3 V dual-voltage devices. The proposed circuit is realized with only 3.3 V NMOS/PMOS devices. The breakdown voltage of 3.3 V and 0.18 μm CMOS technology is around 4 V. Therefore, the transistor works at less than 4 V to prevent damage to the transistor. The simulation result of the voltage conversion ratio (VCR) and PCE under the different process corner TT, FF and SS, is shown in Figures 9 and 10. The simulated VCR with the input voltage that ranges from 2 V to 3.6 V with \( R_{Load} = 300 \Omega \), as shown in Figure 9. This result verifies that the VCR of the proposed rectifier has the worst VCR, 88.7%, for SS corner. Figure 10 shows the simulated result of PCE of proposed rectifier versus output load \( R_{Load} \) under different process corners TT, FF and SS, when the AC input peak-peak amplitude is fixed at 3.6 V. The simulated PCE result has a slight drop of around 1% to 6%, especially in heavy loads for the SS corner. The simulation of the variation with the process and temperature is included in Table 1. This result shows that the proposed active rectifier has a very stable PCE with 3.9% of variation and VCR with 2% of variation under different processes and temperatures.

![Figure 8. Pie chart of power consumption.](image-url)
Figure 9. Voltage conversion ratio (VCR) versus different input voltage.

Figure 10. Power conversion efficiency (PCE) versus different output load.

Table 1. Power conversion efficiency (PCE) and voltage conversion ratio (VCR) versus process and temperature.

| Simulation Result | Corner | Temperature (°C) | PCE (%) | VCR (%) |
|-------------------|--------|------------------|---------|---------|
| TT                | 27     | 92.5%            | 92.5%   |
| SS                | 100    | 88.7%            | 90.6%   |
| FF                | 0      | 92.6%            | 92.6%   |

3. Measurement Results

The proposed rectifier is fabricated in 0.18 μm CMOS process with standard I/O devices. The microphotograph with its floorplan is shown in Figure 11. The core area of the chip is 0.24 mm². The outputs of the active rectifier included in the external resistor and capacitor are 300 Ω and 2 nF, respectively. The measurement setup is shown in Figure 12. The experimental setup includes a current waveform analyzer Keysight CX3324A, CX1101A current probe and N2862B passive probe (Keysight Technologies, Santa Rosa, CA, USA). In this measurement, the distance between primary coil $L_1$ and secondary coil $L_2$ would influence the magnetic resonant amplitude. Therefore, we put it as close as possible for maximum amplitude to be received by the inductor $L_2$. The proposed IC die is attached directly to PCB and bonded out with 5–6 mm aluminum wire. The ringing of the measured signal is due to the bond wire and the onboard capacitance in the PCB. The AC input voltage amplitude ranges from 2 V to 3.8 V, and the resonant frequency is fixed at 13.56 MHz.
Figure 13a shows the measured waveform of the active rectifier without a phase error detector. Figure 13a shows very serious ringing for the AC input waveforms, and the ringing inside the chip is expected to be even more serious. Figure 13b shows the measured waveform of the active rectifier without the phase error detector. Figure 13b shows less ringing for the AC input waveform and demonstrates the effectiveness and accuracy of the proposed technique. Figure 14 shows the measured PCEs with load resistor that range from 100 Ω to 1300 Ω when the input voltage is 3.3 V. As shown in Figure 14, the minimum load resistance is 50 Ω with 2 nF of the external capacitor. The optimized PCE is allocated at 300 Ω load, and its output power is 109 mW. Figure 15 shows the performance of the rectifier in various input voltages. The measured VCR with the output voltage ranging from 2 V to 3.8 V are higher than 90.3% when $R_{\text{Load}} = 300 \, \Omega$ and 90% when $R_{\text{Load}} = 600 \, \Omega$, respectively. The measured result of the output current with output load resistance ranging from 100 Ω to 1300 Ω is shown in Figure 16. The proposed rectifier generates current from 2.6 mA up to 55.4 mA with 3.3 V input voltage. Table 2 compares the performance of the proposed work with state-of-the-art active rectifiers. The proposed rectifier achieves high PCE and VCE over a wide loading range from 100 Ω to 1.3 kΩ. A peak PCE of 90.3% and maximum output power of 109 mW are achieved at 3.3V input voltage. The proposed circuit is well-suited for a wide range of input voltage and loading resistors. The phase error detector works well to remove the phase difference due to the buffer itself.
Figure 13. Measured waveforms of the proposed rectifier (a) without phase error detector and (b) with phase error detector.

Figure 14. Measured PCE under different load resistors.
Figure 15. Measured VCR under different input voltage.

Figure 16. Output current versus different output loads.

Table 2. Comparison with prior works.

| Parameters       | [18] TCASII’12 | [9] JSSC’16 | [11] JSSC’19 | This Work |
|------------------|----------------|-------------|--------------|-----------|
| Technology (µm)  | 0.18           | 0.18        | 0.18         | 0.18      |
| Frequency (MHz)  | 13.56          | 13.56       | 13.56        | 13.56     |
| Input Amp.(V)    | 0.9–2          | 1.3–2.5     | 1.0–2.5      | 1.8–3.6   |
| Output Amp.(V)   | 0.45–1.78      | 1.24–2.44   | 0.928–2.37   | 1.62–3.35 |
| Pout (Max. mW)   | 3.2            | 248.1       | 34.1         | 109       |
| VCR (%)          | 82–89 (R_{\text{Load}} = 1 \, \Omega) | 91.7–95.2 (R_{\text{Load}} = 100 \, \Omega) | 92.8–97.5 (R_{\text{Load}} = 510 \, \Omega) | 89–90.3 (R_{\text{Load}} = 200 \, \Omega) |
| PCE (%)          | 60–81.9 (R_{\text{Load}} = 1 \, \Omega) | 91.3–94.6 (R_{\text{Load}} = 100 \, \Omega–500 \, \Omega) | 82.6–94.1 (R_{\text{Load}} = 510 \, \Omega–2 \, k\Omega) | 83–90.3 (R_{\text{Load}} = 100 \, \Omega–1.3 \, k\Omega) |

4. Conclusions

In this paper, an active rectifier with a phase error detector is presented to compensate the phase difference due to the buffer in the rectifier. The rectifier has a high power efficiency over a wide input range from 2 V to 3.8 V. A peak PCE of 90.3% and maximum output power of 109 mW are achieved at 3.3 V input voltage.
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**References**

1. Campi, T.; Cruciani, S.; Palandrani, F.; De Santis, V.; Hirata, A.; Feliziani, M. Wireless Power Transfer Charging System for AIMDs and Pacemakers. *IEEE Trans. Microw. Theory Tech.* 2016, 64, 633–642. [CrossRef]

2. Akin, T.; Najafi, K.; Bradley, R.M. A wireless implantable multichannel digital neural recording system for a micromachined sieve electrode. *IEEE J. Solid State Circuits* 1998, 33, 109–118. [CrossRef]

3. Bhatti, P.T.; Wise, K.D. A 32-Site 4-Channel High-Density Electrode Array for a Cochlear Prosthesis. *IEEE J. Solid State Circuits* 2006, 41, 2965–2973. [CrossRef]

4. Rothermel, A.; Liu, L.; Pour Aryan, N.; Fischer, M.; Wensschmann, J.; Kibbel, S.; Harscher, A. A CMOS Chip with Active Pixel Array and Specific Test Features for Subretinal Implantation. *IEEE J. Solid State Circuits* 2008, 44, 290–300. [CrossRef]

5. Cheng, L.; Ki, W.; Lu, Y.; Yao, Y.; Ki, W.-H. An Implantable Ultrasonically Powered System for Optogalvanic Stimulation with Power-Efficient Active Rectifier and Charge-Reuse Capability. *IEEE Tran. Biomed. Circuits Syst.* 2019, 13, 1362–1371. [CrossRef]

6. Rashidi, A.; Laursen, K.; Hosseini, S.; Huynh, H.; Moradi, F. A CMOS Rectifier with a Cross-Coupled Latched Comparator for Wireless Power Transfer in Biomedical Applications. *IEEE Trans. Circuits Syst. II Express Briefs* 2012, 59, 409–413. [CrossRef]