Algorithm engineering for a quantum annealing platform

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Recent advances bring within reach the viability of solving combinatorial problems using a quantum annealing algorithm implemented on a purpose-built platform that exploits quantum properties. However, the question of how to tune the algorithm for most effective use in this framework is not well understood. In this paper we describe some operational parameters that drive performance, discuss approaches for mitigating sources of error, and present experimental results from a D-Wave Two quantum annealing processor.

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1 Introduction

In the last three decades researchers in algorithm engineering have identified many strategies for bridging the gap between abstract algorithm and concrete implementation to yield practical performance improvements; see [21] or [24] for an overview. In this paper we apply this conceptual framework in a novel context, to improve performance of a quantum annealing algorithm implemented on a purpose-built platform. Quantum annealing (QA) is a heuristic method for solving combinatorial optimization problems, similar to simulated annealing. The platform is a D-Wave Two system, which exploits quantum properties to solve instances of the NP-hard Ising Minimization Problem (IMP).

Several research groups have reported on experimental work to understand performance of D-Wave systems; see for example [5], [6], [14], [23], [27], and [30]. Building on this experience we describe an emerging performance model that helps to distinguish the algorithm from its realization on a physical platform. Using this model we present a collection of strategies for improving computation times in practice. Our discussion exposes similarities as well as differences in algorithm engineering approaches to quantum versus classical computation.

The remainder of this section presents a quick overview of the quantum annealing algorithm and its realization in D-Wave hardware. Section 2 surveys the main factors that drive performance. Section 3 presents our strategies together with experimental results to study their efficacy. Section 4 presents a few concluding remarks.

The native problem An input instance to the Ising Minimization Problem (IMP) is described by a Hamiltonian \((h, J)\) containing a vector of local fields \(h \in \mathbb{R}^n\) and a matrix of couplings \(J \in \mathbb{R}^{n \times n}\) (usually upper-triangular). We may consider weights \(h_v\) and nonzero \(J_{uv}\) to be assigned to vertices and edges of a graph \(G = (V, E)\). The problem is to find an assignment of spin values \(s \in \{-1, 1\}^n\) (i.e. a spin configuration or spin state) that minimizes the function

\[
E(s) = E(h, J, s) := \sum_{v \in V(G)} h_v s_v + \sum_{uv \in E(G)} J_{uv} s_u s_v.
\]

This problem has origins in statistical physics, where \(E(s)\) defines the energy of a given spin state \(s\). A ground state has minimum energy. A non-ground state is called an excited state; a first excited state has the lowest energy among exited states. Notice how the signs of \((h, J)\) affect this function: a term with \(J_{uv} < 0\), called a ferromagnetic coupling, is minimized when \(s_u = s_v\); an antiferromagnetic coupling term with \(J_{uv} > 0\) is minimized when \(s_u \neq s_v\). The problem is NP-hard when \(G\) is nonplanar [15].

Quantum annealing While a classical bit takes discrete values 0 or 1, a quantum bit (qubit) is capable of superposition, which means that is simultaneously in both states; thus a register of \(N\) qubits can represent all \(2^N\) possible states simultaneously. When a qubit is read, its superposition state “collapses” probabilistically to a classical state, which we interpret as a spin \(-1\) or \(+1\).

Qubits act as particles in a quantum-mechanical system that evolves under forces described by a time-dependent Hamiltonian \(H(t)\). For a given Hamiltonian they naturally seek their ground state just as water seeks the lowest point in a landscape. Since superposition is represented not by a single state but by a probability mass, we can think of it as moving through hills in a porous landscape – this is sometimes called tunneling. A quantum annealing algorithm exploits this property to perform an analog computation defined by the following components.

\[\text{D-Wave, D-Wave Two, and Vesuvius are trademarks of D-Wave Systems Inc.}\]
Table 1: Operating parameters for the processor used in our tests.

| name | qubits | couplers | temperature |  \( t_p \) |  \( t_f \) |  \( t_s \) |
|------|--------|----------|------------|----------|----------|----------|
| V7   | 481    | 1306     | 14mK       | 30ms     | 20\( \mu \)s | 116\( \mu \)s |

(C1) The initial Hamiltonian  \( H_I \) puts each qubit into superposition whereby spins are independent and equiprobable.

(C2) The problem Hamiltonian  \( H_P = (h, J) \) matches the objective function (1) so that a ground state corresponds to an optimal solution to the problem.

(C3) The path functions  \( A(r), B(r) \) define a transition from  \( H_I \) to  \( H_P \), where  \( A(r) : 1 \to 0 \) and  \( B(r) : 0 \to 1 \) as  \( r : 0 \to 1 \). Parameter  \( r \) controls the rate of change  \( r = r(t) \) (possibly speeding up or slowing down) as time  \( t \) moves from start  \( t_0 = 0 \) to finish  \( t_f \).

The entire algorithm is defined by the time-dependent Hamiltonian:

\[
H(t) = A(r)H_I + B(r)H_P.
\]  

A QA algorithm can be simulated classically using many random states to model superposition: (C3) is analogous to a simulated annealing schedule, except it modifies the problem landscape rather than a traversal probability; (C1) corresponds to choosing random initial states in a flat landscape; and (C2) to the target solution. See [10], [17] or [20]. QA belongs to the adiabatic model of quantum computation (AQC), which is a polynomially-equivalent [2, 13] alternative to the more familiar quantum gate model. QA algorithms typically use problem Hamiltonians from a subclass of those in the full AQC model; thus QA computation is likely not universal, although the question is open (see [22]).

2 Hardware platform and cost models

A D-Wave Two (DW2) platform contains a quantum annealing chip that physically realizes the algorithm in Equation (2). Qubits and the couplers connecting them are made of microscopic superconducting loops of niobium, which exhibit quantum properties at the processor’s operating temperature, typically below 20mK. See [7] for an overview.

The annealing process is managed by a framework of analog control devices that relay signals between a conventional CPU and the qubits and couplers onboard the chip, in stages as follows.

1. Programming. The weights  \( (h, J) \) are loaded onto the chip. Elapsed time =  \( t_p \).
2. Annealing. The algorithm in (2) is carried out. Time =  \( t_f \).
3. Sampling. Qubit states are measured, yielding a solution  \( s \). Time =  \( t_s \).
4. Resampling. Steps 2 and 3 are repeated to obtain some number  \( k \) of sampled solutions.

Total computation time is therefore equal to

\[
T = t_p + k(t_f + t_s).
\]  

Component times vary from machine to machine; the system used in our tests has operating parameters shown in Table 1. Note that total time is dominated by what are essentially I/O costs; successive processor models have generally shown reductions in these times and this trend is expected to continue. Anneal time  \( t_f \) can be set by the programmer; the minimum setting 20\( \mu \)s is dictated by the system’s ability to shape  \( A(r) \) and  \( B(r) \).
2.1 Analysis

In algorithm engineering we can identify different levels of instantiation in a spectrum that includes the pencil-and-paper algorithm, an implementation in a high-level language, and a sequence of machine instructions. The definition of time performance (dominant cost vs. CPU time) and the set of strategies for reducing it (asymptotics vs. low-level coding) depend on the level being considered. This framework applies to quantum as well as classical computation. This subsection describes instantiation layers and cost models for the quantum annealing algorithm realized on D-Wave platforms.

Asymptotics of closed-system AQC  
Abstract AQC algorithms have been developed for many computational problems; see [22] for examples. For a given algorithm (a generalization of (2)) and input of size $n$, let $\gamma = \gamma(n)$ denote the minimum spectral gap, the smallest difference between the energies of the ground state and the first excited state at any time $t : 0 \rightarrow t_f$. Under certain assumed conditions, if $t_f$ is above a threshold in $\Theta(poly(n)/\gamma^2)$, then the computation will almost surely finish in ground state. Setting $t_f$ below the threshold increases the probability that a nonoptimal solution is returned. Typically $\gamma$ is difficult to compute and bounds are known only for simple scenarios; some algorithm design strategies have been identified for “growing the gap” to reduce asymptotic computation times. See [12], [13], [16], [22], or [25] for more.

Quantum computation in the real world  
Asymptotic analysis assumes that the algorithm runs in a closed system in perfect isolation from external sources of energy (thermal, electrical, magnetic, etc). It is a matter of natural law, however, that any physically-realized quantum computer runs in an open system and suffers interference from the environmental “energy bath.” Environmental interference may reduce the probability of finishing in ground state – in particular the theoretical annealing time threshold depends on both $\gamma^2$ and the ambient temperature $T$, implying that colder is faster. In practice, there is evidence that the thermal bath can increase the probability of success substantially [11].

We use the terms AQC and QA to distinguish algorithms running in closed vs. open systems. Some (exponential) bounds on convergence times of classical QA algorithms are known [17, 28]; these bounds are better than those of simulated annealing in some cases.

Realization on D-Wave platforms  
In addition to the above nonideality, DW2 architecture imposes some restrictions on inputs:

1. The connection topology defines a hardware graph $G = (V,E)$, a subgraph of a $C_8$ Chimera graph [7] containing 512 qubits. An IMP instance defined on a general graph $G_0$ must be minor-embedded onto $G$. This requires $O(n^2)$ expansion in problem size [9] in the worst case; in practice we use a heuristic approach described in [8]. See Appendix A for more about Chimera graphs and minor-embeddings.

2. The elements of $h$ and $J$ must be in the real range $[-1,1]$. This can be achieved by scaling general $h$ and $J$ by a positive constant factor $\alpha$.

3. The weights $(h,J)$, specified as floats, are transmitted imperfectly by the analog control circuitry. As a result, they experience perturbations of various sorts, systematic (biased), random, persistent, and transient. The perturbations are collectively referred to as intrinsic.

This is in contrast to the meme that Hamiltonian misspecification is due to calibration errors (cf. [29]). Calibration errors, which are systematic and relatively fixed, represent only a small component of ICE.
control error (ICE). Because of ICE, the problem Hamiltonian solved by the chip may be slightly different from the problem Hamiltonian specified by the programmer.

Putting all this together, total computation time in Equation (3) depends on the probability \( \pi \) of observing a successful outcome (a ground state) in a single sample. In theory, \( \pi \) depends on a threshold value for \( t_f \), which is typically unknown in open-system computing. Because of Hamiltonian misspecification we may prefer \( \pi < 1 \) in order to sample solutions near the (wrong) ground state; if \( \pi \) is too small, \( k \) can be increased to improve the overall success probability. Just as in classical computing, there is a trade-off between time and solution quality, although very little is known about the nature of that trade-off.

In what follows, we calculate the empirical success probability \( \pi \) for a given input as the proportion of successful samples drawn among \( k \) samples from the hardware, using various definitions of success in order to examine the relationship between computation time and solution quality. We calculate the expected number of samples required to observe a successful outcome with probability at least 0.99 (ST99): this is \( k_{99} = \log(1 - 0.99) / \log(1 - \pi) \). Computation time is found by combining \( k_{99} \) with component times as in (3).

### 2.1.1 ICE: The error model

Our simplified model of ICE, which will be described more fully in a forthcoming paper, assumes that the problem Hamiltonian \((h, J)\) is perturbed by an error Hamiltonian \((\tilde{h}, \tilde{J})\), where \( \tilde{h}_u \) and \( \tilde{J}_{uv} \) are independent Gaussians having mean 0 and standard deviations \( \sigma_h \) and \( \sigma_J \), which vary by chip (and generally decrease with new models). For V7 (see Table 1) we have \( \sigma_h \approx .050 \) and \( \sigma_J \approx .035 \). These errors are relative to the nominal scale of \([-1, +1]\), which means that if \( h \) and \( J \) are scaled by \( \alpha \in (0, 1) \), relative errors are amplified by a factor of \( 1/\alpha \).

For a given spin configuration \( s \) this shifts the effective energy from \( E(s) \) by a Gaussian error \( \tilde{E}(s) \) with mean 0 and standard deviation \( \sigma_E = (N\sigma_h^2 + M\sigma_J^2)^{1/2} \) where \( N \) and \( M \) are the number of active qubits and couplers in the hardware graph. On a full size V7 problem \((N = 481)\) we have \( \sigma_E = 1.67 \). By the three-sigma rule, \(|\tilde{E}(s)| < 1.67 |E(s)| < 5.01 \) for about 68 and 99.5 percent of spin configurations, respectively. Although \( \sigma_E \) scales as \( \Theta(\sqrt{n}) \), the typical value of \( \max_s |\tilde{E}(s)| \) scales linearly in \( n \), and is near 14 at full size.

ICE imposes a practical limit on the precision of (scaled) weights that can be specified in successful computations. For example, if \( h_u, J_{uv} \in [-1, +1] \), then two solutions \( s \) and \( s' \) with \( E(s) < E(s') \) satisfy \( E(s) \leq E(s') - 2 \), so it is relatively unlikely that \( E(s) + \tilde{E}(s) > E(s') + \tilde{E}(s') \). The difficulty occurs when energy levels differ by smaller amounts, which can happen when integer weights are scaled by \( \alpha < 1 \).

Figure 1 illustrates this effect using RAN3 instances (described in the next section) solved at full scale \((\alpha = 1/3)\) and half-scale \((\alpha = 1/6)\). The left panel shows how reducing the problem scale increases ST99 roughly tenfold in the median case for largest problems when searching for an optimal solution. The right panel shows ST99 when the success condition is to find a solution within \( \sigma_E \) of ground state. In both scales, computation times shrink by more than two orders of magnitude in nearly all percentiles. This suggests that reductions in ICE on future chip models are likely to boost hardware performance significantly. Analyzing performance with respect to the \( \sigma_E \) error bound allows us to look beyond the effect of Hamiltonian misspecification, which is detrimental to hardware success rates and may mask evidence of quantum speedup.

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\[ \text{This holds for most sources of ICE, with the notable exception of background susceptibility, denoted } \chi, \text{ which is reduced by a factor of } 1/\alpha - \text{ see [31]. Background susceptibility is an instance-dependent, non-transient error that, in a more sophisticated error model, might be separated from Gaussian error.} \]
3 Algorithm Engineering on D-Wave Two Platforms

In this section we consider strategies for mitigating ICE-related nonideality and small spectral gaps with the goal of increasing success probabilities and lowering computation times.

D-Wave systems realize a specific QA algorithm in the sense that the components $H_I, A(r), B(r)$ and $r(t)$ are set in firmware (see [7] for details). Here we focus on parameters that can be controlled by the programmer, namely $(h, J), t_f$, and $k$. We also consider classical methods for pre-processing and error correction. We evaluate these strategies on the following instance classes, described more fully in Appendix [13]

- Random native instances (RANR). For each $(u, v) \in G$, $J_{uv}$ is assigned a random nonzero integer in $\{-R \ldots + R\}$. We set $h_u = 0$.

- Frustrated loop instances (FLR) [14]. These are constraint satisfaction problems whose entries of $J$ lie in $\{-R, \ldots, R\}$. They are combinatorially more interesting than RANR instances but do not require minor-embedding.

- Random cubic MAX-CUT instances (3MC). These are MAX-CUT problems on random cubic graphs, which must be minor-embedded onto the V7 hardware graph.

- Random not-all-equal 3-SAT instances (NAE). These are randomly generated problems near the SAT/UNSAT phase transition, filtered subject to having a unique solution (up to symmetry), and then minor-embedded onto the V7 hardware graph.

All experiments described here take random instances generated at sizes of up to 481 qubits; the specifics of instances are given in Appendix A. Unless otherwise specified, $k_{99}$ is calculated from 1000 samples in 10 gauge transformations (next section), totaling 10,000 samples. Optimal solutions are verified using an independent software solver. In rare cases a sample will not contain

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4 Katzgraber et al. [18] have shown that these instances are not suitable for investigating quantum speedup because the solution landscape has many global minima and no nonzero-temperature phase transition. Consequently heuristic search algorithms act almost as random samplers, and there is no evolution of tall, thin barriers that would allow an open-system quantum annealer to exhibit an advantage through tunneling. However, this class is suitable for looking at non-quantum effects such as ICE, as we do here.
an optimal solution, giving an empirical success probability of 0 and ST99 = ∞. To simplify data analysis we look at ST99 for the 95th and lower percentiles of each input set; missing percentile points in some graphs correspond to observations of π = 0.

3.1 Gauge transformations

Given instance $H = (h, J)$, one can construct a modified instance $H' = (h', J')$ by flipping the sign of some subdimension of the search space, as follows: take a vector $\vec{g} \in \{-1, 1\}^n$, set $h'_u = h_u g_u$ for each $u$, and set $J'_{uv} = J_{uv} g_u g_v$ for each coupler $uv$. When solving $H$ in hardware, we can divide the $k$ samples among $p$ instances $H_1, H_2, \ldots, H_p$, where $H_i$ is constructed from $H$ by a random gauge transformation $\vec{g}^{(i)}$; we then apply the (idempotent) transformation to the hardware output to obtain a solution for $H$. Doing this mitigates the effects of some sources of ICE. Gauge transformations are also described in [6] and [29].

Figure 2 shows the effect of applying $p = 10$ gauge transformations on RAN1 instances (left) and NAE instances (right). In both cases, gauge transformations help more on the most difficult problems (higher percentiles). This is unsurprising, as difficult problems are typically more sensitive to perturbation by ICE. Note that every $H_i$ is a new instance which requires a programming step; the current dominance of $t_p$ over $t_f + t_s$ means that it is rarely cost-effective to draw fewer than 1000 samples per gauge transformation. However, this technique may yield more significant performance improvements in applications other than optimization, such as fair sampling of the solution space, which is highly sensitive to Hamiltonian misspecification.

3.2 Optimal anneal times

Previous work [6, 29] has reported on experiments to find optimal settings of $t_f$ for RANR instances, concluding that for problem sizes $N \leq 512$ the lowest possible $t_f = 20\mu s$ is longer than optimal. More recent work has found instances whose optimal anneal time on a DW2 processor is greater than $20\mu s$ [19]. Those studies consider anneal time in isolation, so that the optimal time $t_f$ minimizes $k_{99} t_f$. However, under the cost model in (3), the optimal $t_k$ minimizes $k_{99} (t_k + t_s)$ so that a smaller increase in $\pi$ is sufficient to reduce total runtime in practice. Also, by analogy to observations about simulated annealing in [30], we might expect that longer anneal times are optimal for problem

Figure 2: Effect of gauge transformations on RAN1 (left) and NAE (right) instances. Times marked in blue take 10,000 samples with no gauge transformation; times in red take 1000 samples at each of $p = 10$ gauge transformations. Percentile lines are shown for 100 and 50 inputs at each problem size, respectively.
Figure 3: Changing anneal times for RAN1 (top) and FL2 (bottom) instances at largest problem size. Box plots show percentiles 5, 25, 50, 75, and 95, plus outliers, in 200 instances.

classes that are combinatorially interesting but relatively insensitive to misspecification (compared to RANR instances for large $R$).

Figure 3 shows the result of varying the anneal time from 20µs to 160µs for 200 RAN1 problems and 200 FL2 problems at a 481-qubit scale drawing 100,000 samples over 100 gauge transformations: despite the noisy data, small reductions in ST99 can be seen at all quantiles. (Improvements from increased anneal time are less apparent for more error-sensitive classes such as NAE.) These limited results – together with very preliminary data on a prototype chip with $> 900$ qubits – suggest that we can expect anneal times to be more important to performance and to grow above 20µs on next-generation chips with up to 1152 qubits.

3.3 Methods for minor-embedded problems

Suppose we have a Hamiltonian $(h_0, J_0)$ for a general (non-Chimera-structured) IMP instance defined on a graph $G_0$ of $n_0$ vertices; this graph must be minor-embedded in the hardware graph $G = (V, E)$ for solution. In current D-Wave architectures we have $G \subseteq C_k$ where $C_k$ is a Chimera graph on $8k^2$ vertices. Each $C_k$ contains $K_{4k}$ as a minor (actually requiring only $4k(k+1)$ qubits [30]), but in practice we can find more compact embeddings using a heuristic algorithm such as described in [9]. (See Appendix A.)

**Optimizing chain strength** An embedding contains, for each vertex $v_i$ of $(h_0, J_0)$, a set $V_i$ of vertices assigned to a connected subgraph of $G$. We call each $V_i$ (and a spanning subgraph induced
Figure 4: Performance on 50 NAE instances at each problem size using minimal ($\kappa_0$) and elevated ($\kappa_0 + 1$) chain strength for each instance.

by $V_i$ in $G$) a chain. By assigning a strong ferromagnetic coupling (a large-magnitude value $-\kappa$ for $\kappa > 0$) between qubits in the same chain we can ensure that in low-energy states of $(h, J)$, all qubits in $V_i$ will take the same spin value, for each $i$. Thus the hardware output is likely to yield feasible solutions when mapped back to $v_i$ in $(h_0, J_0)$.

Too-small $\kappa$ produces broken chains (i.e. chains whose spins do not unanimously agree) in hardware output; that is, the solution in the code space cannot be mapped back to the (unembedded) solution space (see [32]). On the other hand, large $\kappa$ decreases the problem scaling factor $\alpha$, which effectively boosts ICE, as in Figure 1. Therefore the choice of $\kappa$ has a significant effect on hardware success rates.

For NAE3SAT it appears that the hardware performs best when $\kappa$ is minimized subject to the constraint that no ground state contains a broken chain; results on fully-connected spin glasses appear to agree [30]. This value of $\kappa$, denoted $\kappa_0$, is instance dependent, and can be approximated empirically by gradually increasing $\kappa$ from zero until the lowest energy found corresponds to a state with no broken chains. Figure 4 shows the effect of varying chain strength in NAE instances, with $\kappa \in \{\kappa_0, \kappa_0 + 1\}$. For these instances $\kappa_0$ ranges between 1.5 and 6 on instances of 10 to 40 logical variables, embedded on 18 to 379 physical qubits. At largest problem sizes, increasing $\kappa_0$ by 1 can more than double median computation times. The right panel shows a difference of two orders of magnitude on some instances and an interesting bimodal property that awaits further analysis.

Chain shimming One can think of the Hamiltonian $(h, J)$ in an embedded problem as a combination of two Hamiltonians, one encoding the original problem and one encoding the chain constraints. Thus we have $(h, J) = (h, J_p + J_c)$ since the chain Hamiltonian contains no local fields. Due to ICE, $J_c$ introduces a set of effective small local fields called $h$-biases. Although ICE will be mitigated in future hardware generations, this issue can be addressed immediately using a simple technique called chain shimming.

Chain shimming starts by sending the Hamiltonian $(0, J_c)$ to the hardware and measuring the bias on each chain: that is, since $(0, J_c)$ has no local fields and no connections between chains, the hardware should return unbroken chains having spins $+1$ and $-1$ with equal probability. If the distribution is biased, we place a compensating $h$-bias on each qubit of each askew chain. A few iterations of this process to refine $h$-biases can sometimes improve time performance. This technique can be most efficiently applied when the structure of $G_0$ (and therefore the chain Hamiltonian) is constant over many instances, e.g. for the fully-connected graphs described in [30].
Figure 5 shows ST99 for 210 3MC instances on V7 with and without shimming. The data provides some evidence of a slight but systematic improvement in performance as problems become larger and more difficult. This improvement is not seen for NAE instances, likely due to the higher chain strength required for NAE instances and the subsequent ICE sensitivity (3MC instances use $\kappa = 2$, which is always sufficient).

3.4 Classical Error Correction via Postprocessing

An obvious remedy for some types of errors described in 2.1.1 is to apply error correction techniques. Pudenz et al. [26, 27] present quantum error-correcting codes for D-Wave architectures; and Young et al. [32] describe quantum stabilizer codes. These techniques boost hardware performance immensely at the cost of many ancillary and redundant qubits, and consequently a reduction in the size of problems that can be solved on a fixed-size chip. An alternative strategy discussed here is to apply cheap classical postprocessing operations to the solutions returned by hardware.

**Majority vote** In embedded problems it is possible for the hardware to return solutions with broken chains. Rather than discarding such samples, we may instead set the spin of each qubit in a chain according to a *majority vote* of qubits in the same chain (breaking ties randomly). This is computationally inexpensive and improves hardware success probabilities. Several more sophisticated methods may be considered for repairing broken chains, such as increasing chain strength until votes are unanimous or converting unanimous chains into local fields to reduce the problem: further study is needed.

**Greedy descent** Another simple postprocessing technique is to walk each hardware solution down to a local minimum by repeatedly flipping random bits to strictly reduce solution cost. We call this approach *greedy descent*. In a minor-embedded problem, this can be applied to the solution to the unembedded or the embedded problem, or both. More generally, one can apply as a postprocessing step any classical heuristic that takes an initial state from the hardware and refines it, e.g. simulated annealing, tabu search, or parallel tempering.

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Footnote: We recognize that there is conceptually a fine line between using a DW2 system as a preprocessor and using classical heuristic as an error-correcting postprocessor. Work is underway to explore these ideas.
Figure 6: Error correction by postprocessing on 50 NAE problems on each problem size.

Figure 6 shows the effect of postprocessing on NAE instances. In these tests $\kappa$ is set to $\kappa_0 + 1$, runs at higher $\kappa$ will derive less benefit from majority vote, and more from greedy descent.

4 Conclusions

We have presented several algorithm engineering techniques that aim to improve the performance of D-Wave quantum annealing processors. These include strategies for modifying anneal times, changing the problem Hamiltonian (gauge transformations, chain shimming), improving chains in embedded problems, and exploiting simple postprocessing ideas. Many more ideas along these lines can be identified, and it remains to be seen what performance gains can be achieved by applying combinations of techniques. Beyond these individual strategies, perhaps a more important contribution has been the presentation of a conceptual framework for distinguishing performance of the quantum algorithm from its realization in technologically immature but rapidly-developing hardware.

The question arises as to how some of these techniques might affect the performance of classical software solvers. Techniques that focus on mitigating Hamiltonian misspecification (e.g. chain shimming and gauge transformation) are largely irrelevant to classical heuristic approaches to solving IMP, since digital computers do not experience these types of errors. Other techniques such as postprocessing and longer anneal times can be successfully transferred to some algorithmic approaches – such as heuristic search – but not necessarily to others – such as dynamic programming based approaches.

Both the quantum annealing paradigm and its implementation on quantum hardware are very new concepts, and the current performance model is primitive and incomplete. This paper represents a small step towards better understanding of performance in this novel computing paradigm.

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References

[1] D. Achlioptas, A. Chtcherba, G. Istrate, and C. Moore. The phase transition in 1-in-k SAT and NAE 3-SAT. In *Proceedings of the Twelfth Annual ACM-SIAM Symposium on Discrete Algorithms*, pages 721–722. Society for Industrial and Applied Mathematics, 2001.

[2] D. Aharonov, W. van Dam, J. Kempe, Z. Landau, S. Lloyd, and O. Regev. Adiabatic quantum computation is equivalent to standard quantum computation. *SIAM Journal on Computing*, 37(1):166–194, 2007.

[3] T. Albash, S. Boixo, D.A. Lidar, and P. Zanardi. Quantum adiabatic Markovian master equations. *New Journal of Physics*, 14(12):123016, 2012.

[4] P. Berman and M. Karpinski. On some tighter inapproximability results. In *Proceedings of the 26th International Colloquium on Automata, Languages and Programming*, pages 200–209. Springer-Verlag, 1999.

[5] Z. Bian, F. Chudak, R. Israel, B. Lackey, W.G. Macready, and A. Roy. Discrete optimization using quantum annealing on sparse Ising models. *Frontiers in Physics*, 2:56, 2014.

[6] S. Boixo, T.F. Rønnow, S.V. Isakov, Z. Wang, D. Wecker, D.A. Lidar, J.M. Martinis, and M. Troyer. Evidence for quantum annealing with more than one hundred qubits. *Nature Physics*, 10(3):218–224, 2014.

[7] P. Bunyk, E. Hoskinson, M. Johnson, E. Tolkacheva, F. Altomare, A. Berkley, R. Harris, J. Hilton, T. Lanting, A. Przybysz, et al. Architectural considerations in the design of a superconducting quantum annealing processor. *IEEE Transactions on Applied Superconductivity*, 2014.

[8] J. Cai, W.G. Macready, and A. Roy. A practical heuristic for finding graph minors. *arXiv preprint arXiv:1406.2741*, 2014.

[9] V. Choi. Minor-embedding in adiabatic quantum computation: I. The parameter setting problem. *Quantum Information Processing*, 7(5):193–209, 2008.

[10] A. Das and B.K. Chakrabarti. *Quantum annealing and related optimization methods*, volume 679 of *Lecture Notes in Physics*. Springer, 2005.

[11] N.G. Dickson et al. Thermally assisted quantum annealing of a 16-qubit problem. *Nature Communications*, 4(May):1903, January 2013.

[12] E. Farhi. Different strategies for optimization using the quantum adiabatic algorithm. Presented at AQC 2014, [www.isi.edu/events/aqc2014/](http://www.isi.edu/events/aqc2014/), 2014.

[13] E. Farhi, J. Goldstone, S. Gutmann, J. Lapan, A. Lundgren, and D. Preda. A quantum adiabatic evolution algorithm applied to random instances of an NP-complete problem. *Science*, 292(5516):472–475, 2001.

[14] I. Hen. Performance of D-Wave Two on problems with planted solutions. Presented at AQC 2014, [www.isi.edu/events/aqc2014/](http://www.isi.edu/events/aqc2014/), 2014.
[15] S. Istrail. Statistical mechanics, three-dimensionality and NP-completeness: I. Universality of intracatability for the partition function of the Ising model across non-planar surfaces. In Proceedings of the thirty-second annual ACM symposium on Theory of computing, pages 87–96. ACM, 2000.

[16] S.P. Jordan, E. Farhi, and P.W. Shor. Error-correcting codes for adiabatic quantum computation. Physical Review A, 74(5):052322, 2006.

[17] T. Kadowaki and H. Nishimori. Quantum annealing in the transverse Ising model. Physical Review E, 58(5):5355, 1998.

[18] H.G. Katzgraber, F. Hamze, and R.S. Andrist. Glassy Chimeras could be blind to quantum speedup: Designing better benchmarks for quantum annealing machines. Physical Review X, 4(2):021008, 2014.

[19] D.A. Lidar. Personal communication. 2014.

[20] R. Martoñák, G.E. Santoro, and E. Tosatti. Quantum annealing by the path-integral Monte Carlo method: The two-dimensional random Ising model. Physical Review B, 66(9):094203, 2002.

[21] C.C. McGeoch. A guide to experimental algorithmics. Cambridge University Press, 2012.

[22] C.C. McGeoch. Adiabatic quantum computation and quantum annealing: Theory and practice. Synthesis Lectures on Quantum Computing, 5(2):1–93, 2014.

[23] C.C. McGeoch and C. Wang. Experimental evaluation of an adiabatic quantum system for combinatorial optimization. In Proceedings of the ACM International Conference on Computing Frontiers, page 23. ACM, 2013.

[24] M. Müller-Hannemann and S. Schirra. Algorithm engineering: bridging the gap between algorithm theory and practice, volume 5971. Springer, 2010.

[25] H. Nishimori, J. Tsuda, and S. Knysh. Comparative study of the performance of quantum annealing and simulated annealing. arXiv preprint arXiv:1409.6386, 2014.

[26] K.L. Pudenz, T. Albash, and D.A. Lidar. Error-corrected quantum annealing with hundreds of qubits. Nature Communications, 5, 2014.

[27] K.L. Pudenz, T. Albash, and D.A. Lidar. Quantum annealing correction for random Ising problems. arXiv preprint arXiv:1408.4382, 2014.

[28] J. Roland and N.J. Cerf. Quantum search by local adiabatic evolution. Physical Review A, 65(4):042308, 2002.

[29] T.F. Rønnow, Z. Wang, J. Job, S. Boixo, S.V. Isakov, D. Wecker, J.M. Martinis, D.A. Lidar, and M. Troyer. Defining and detecting quantum speedup. Science, 345(6195):420–424, 2014.

[30] D. Venturelli, S. Mandrà, S. Knysh, B. O’Gorman, R. Biswas, and V. Smelyanskiy. Quantum optimization of fully-connected spin glasses. arXiv preprint arXiv:1406.7553, 2014.

[31] W. Vinci, T. Albash, A. Mishra, P.A. Warburton, and D.A. Lidar. Distinguishing classical and quantum models for the D-Wave device. arXiv preprint arXiv:1403.4228, 2014.

[32] K.C. Young, R. Blume-Kohout, and D.A. Lidar. Adiabatic quantum optimization with the wrong Hamiltonian. Physical Review A, 88(6):062314, 2013.
A Chimera structure and the hardware graph

A Chimera graph $C_k$ consists of a $k \times k$ grid of cells. In current D-Wave configurations each cell is a complete bipartite graph $K_{4,4}$. Vertices in a row are matched to corresponding vertices in neighboring cells above and below, and vertices in a column are matched to corresponding vertices in neighboring cells to the left and right. See Figures 7 and 8. $C_k$ contains $8k^2$ vertices of degree 6 (internal vertices), and 5 (sides), totalling $24k^2 - 16k$ edges. The hardware graph of V7 is a subgraph of $C_8$, a result of fabrication imperfections and high calibration throughput. The working graph varies from chip to chip.

Minor-embeddings  A minor of a given graph $G = (V, E)$ is any graph that can be constructed from $G$ by application of some number of the following operations, in any order:

1. Remove an edge.

2. Remove a vertex and incident edges.

3. Contract an edge, combining its incident vertices.

If graph $G'$ is a minor of graph $G$, it is straightforward to reduce IMP on $G'$ to IMP on $G$: for each edge $(uv)$ of $G$ that is contracted in the graph minor construction, assign to $J_{uv}$ a strong ferromagnetic (negative) coupling. If $J_{uv}$ is sufficiently large, $u$ and $v$ will take the same spin in any low-energy configuration. As discussed in the paper, sufficient bounds on $J_{uv}$ are highly dependent on the structure of the individual minor chosen.

Choi [9] shows that a complete graph of $n = 4k$ vertices can be minor-embedded in the upper diagonal of a $C_k$, using $4k(k + 1)$ vertices. The problem complexity of deciding the minor-embeddability of an arbitrary graph into a Chimera graph is open.

B Instance classes

We present a brief overview of instance classes used in this work.

B.1 Random instances (RANR)

For given hardware graph $H = (V, E)$, for each $(u, v) \in E$ generate a weight uniformly at random from the integer range $[-R \ldots + R]$ (omitting 0).

Katzgraber et al [18] have shown that these instances are fairly easy for simulated annealing based solvers, for two reasons. First, a random instance typically has a large number of global
minima, which can be found using many random restarts. Second, during most of the anneal time
the solution landscape has gentle slopes and no high barriers: thus the correct neighborhood of a
global optimum is found early in the anneal process.

B.2 Frustrated loop instances

We present a construction of Hen [14] for an Ising Hamiltonian \( (h, J) \) over a hardware graph \( G \)
in which \( \uparrow \uparrow \ldots \uparrow \) is a ground state. Let \( R \), our precision limit, be a positive integer, let \( n \) be the
number of vertices in \( G \), and let \( r \) be a constraint-to-qubit ratio. We construct a Hamiltonian
consisting of a conjunction of \( [rn] \) frustrated loops (where \( [rn] \) denotes the round-off of \( rn \)) as
follows.

First let \( c_1 \) be a cycle chosen at random in some way. Here we do this by performing a random
walk in \( G \) starting at a random vertex, and taking the first cycle we find. To ensure that the cycles
spread across \( G \) sufficiently, we reject a cycle if it is contained entirely in a Chimera \( K_{4,4} \) unit cell, and
repeat the construction. Let \( n_1 \) be the number of vertices in \( c_1 \); note that due to the structure
of \( G \), \( n_1 \) is even and at least 6. We construct a Hamiltonian \( (0, J^{(1)}) \) by setting every edge of \( c_1 \) to
\(-1\) except one chosen uniformly at random, which we set to 1. It is now straightforward to check
that \( (0, J^{(1)}) \) has \( 2n_1 \) ground states, and ground state energy \(-n-2\).

We repeat this construction for further cycles \( c_2, \ldots, c_rn \), with the following wrinkle: if after
choosing \( k \) cycles, an edge \( uv \) of \( G \) has
\[
\sum_{i=1}^{k} J_{uv}^{(i)} = R,
\]
we forbid the edge \( uv \) from appearing in cycles \( c_{k+1}, \ldots, c_{rn} \).

The final Hamiltonian of the problem is \( (h, J) = (0, \sum_{i=1}^{[rn]} J^{(i)}) \). Note that the specified ground state \( \uparrow \uparrow \ldots \uparrow \) can be “hidden” by applying a gauge transformation to the Hamiltonian.

The instances we use in this paper have ratio \( r = 0.2 \), which roughly corresponds to an empirically observed phase transition [14], and precision limit \( R = 2 \), which is the minimum possible value that allows a rich set of instances.

### B.3 Random cubic MAX-CUT instances

MAX-CUT on cubic graphs is a well-known NP-hard problem [4] that has a very simple Ising formulation. Maximum cardinality cuts on a graph \( G \) correspond to ground states of the Ising problem \( (0, J) \) where \( J_{uv} = 1 \) for all \( uv \in E(G) \), and \( J_{uv} = 0 \) elsewhere. It is straightforward to confirm that in the cubic case, when embedding a MAX-CUT Hamiltonian, chain strength \( \kappa = 2 \) is always sufficient to guarantee chain fidelity in the ground state. Indeed, any \( \kappa > 1 \) is sufficient.

### B.4 NAE3SAT instances

As in FLR instances described above, we construct NAE instances as the conjunction of \([rn]\) constraints. In this case we use \( r = 2.1 \), which corresponds roughly to the phase transition for Not-all-equal 3-SAT [1]. Further, the instances must be minor-embedded, as they do not naturally fit into the Chimera hardware graph.

We generate a random NAE3SAT instance by choosing \([rn]\) clauses at random. Each clause consists of 3 unique randomly selected variables, each of which is negated independently with probability \( \frac{1}{2} \). The Hamiltonian for a clause \( (q_1 x_1, q_2 x_2, q_3 x_3) \), where \( q_i = -1 \) if \( x_i \) is negated in the clause and \( q_i = 1 \) otherwise, has \( h = 0 \), and all entries of \( J \) zero except \( J^{(i)}_{x_i, x_j} = q_i q_j \) for \( 1 \leq i < j \leq 3 \). As with frustrated loops, our final Hamiltonian \( (h, J) \) has \( h = 0 \) and \( J = \sum_{i=1}^{[rn]} J^{(i)} \).

For sufficiently large \( n \), the adjacency graph of the nonzero entries of \( J \) is sparse, with average degree \( 6r \), and the nonzero entries of \( J \) are overwhelmingly in \( \{-1, 1\} \). These random instances are converted to Chimera-structured problems via the heuristic minor-embedding algorithm described in [3]. The question of how performance varies from one embedding of an instance to another requires further study outside the scope of this paper. To separate this issue from the algorithm engineering approaches we study here, we take five embeddings of each instance. When we want to compare the performance under several parameter settings, we choose the “best” embedding to study. That is, we choose the embedding for each instance that maximizes the geometric mean of \( \pi \) under the parameter settings we compare.

Our choice of \( \kappa_0 \) for each embedded instance was (over)estimated by solving each problem for chain strength in \( 1, 1.5, 2, \ldots \) until a ground state without broken chains was found.