Design and Characteristics of CMOS Inverter based on Multisim and Cadence

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Abstract. Known as complementary symmetrical metal oxide semiconductor (cos-mos), complementary metal oxide semiconductor is a metal oxide semiconductor field effect transistor (MOSFET) manufacturing process, which uses complementary and symmetrical pairs of p-type and n-type MOSFETs to realize logic functions. CMOS technology is used to build integrated circuit (IC) chips, including microprocessors, microcontrollers, memory chips (including CMOS BIOS) and other digital logic circuits. CMOS technology is also used in analog circuits, such as image sensors (CMOS sensors), data converters, RF circuits (RF CMOS), and highly integrated transceivers for various types of communications. Based on multisim14.0 and cadence, the characteristics and performance of CMOS inverter are studied by simulation.

1. Introduction

Multisim is a windows-based simulation tool launched by National Instruments (NI) Co., Ltd. It is suitable for board-level analog/digital circuit board design [3] and includes graphical input of circuit schematics, circuit hardware description language input. It has a large simulation analysis capabilities. With Multisim, engineers can interactively build circuit schematics and simulate the circuit. Multisim refines the complex content of SPICE simulation, so that engineers can quickly capture, simulate and analyze new designs without knowing in-depth SPICE technology, which also makes it more suitable for electronics education. PCB design engineers and electronics educators can complete a complete integrated design process from theory to schematic capture and simulation to prototype design and testing through Multisim and virtual instrument technology.

Cadence is a large, professional EDA (Electronic Design Automation) software, which can realize almost all the contents of electronic design, layout design, experimental simulation, etc. Software with similar functions include mentor graphics, Synopsys and so on. But compared with other EDA software cadence, cadence has more powerful functions in circuit simulation, circuit diagram design, layout design and wiring. In addition, cadence also shares data with many semiconductor companies and establishes a process library for simulation, which is convenient for users to carry out simulation. The process used in this paper is smic18mm.

The static complementary CMOS combinational logic gate is actually formed by expanding the static CMOS inverter into a logic gate with multiple inputs, so the inverter is discussed here first. The inverter is used in digital integrated circuits to invert the phase of the input signal by 180 degrees, that
is, the gate circuit that performs the inversion operation. At this time, the MOS tube is working in the on-off state. But when the MOS tube works in the transition zone, it can play an amplifying role and can be used in audio amplifiers or clock oscillators. The circuit structure is composed of a PMOS tube and an NMOS tube. Here, the pull-down network and the pull-up network are composed of a single MOS tube to form a static complementary circuit [5].

Noise margin is a measure of design margins to ensure circuits functioning properly within specified conditions [9]. When an inverter is transitioning from a logic high to a logic low, there is an indistinct region in which we cannot consider the voltage either low or high. It is at this precise moment that we consider it to be our noise margin. the CMOS inverter has good logic buffer characteristics, in that, its noise margins in both low and high states are large. Noise margin happened when a inverter connect to another inverter, there could be a noise, which means that the Vout could be higher or lower, and if the VOH is lower than VIH, the signal will not be treated as a logic high. What we do is we need some margin that to make sure that we have enough space for the noise margin. Since The VOH in CMOS inverter is close to the supply voltage, and the minimum of the voltage is also close to zero. The CMOS inverter has the great noise margin. To ensure that transistors switch properly under specified noisy conditions, circuits must be designed with specified noise margins. Figure 1 illustrates the noise margin and the terms [9].

Noise margin high : \( NMH = VOH - VIH \)
Noise margin low : \( NML = VIL - VOL \)

Figure 1. Noise margin and terms [9]

This paper aims to study the properties and characteristics of COMS inverter through two different platforms: Multisim and cadence, so as to provide more reference for other inverter research later.

2. The design of inverter base on Multisim

2.1. Structure of CMOS inverter
Static complementary CMOS gate-level circuits are the most widely used type of logic gates. Because of its good stability, good performance and low power consumption, it is widely used in the design of integrated circuits. The static complementary CMOS gate-level circuit is a combination of a pull-up network (PUN) and a pull-down network (PDN), and its structure is shown in the Figure 2 in the static complementary CMOS gate circuit design, a pull-down network is generally first designed according to the logic solution calculation formula to be implemented, and then a pull-up network is made according to the logic structure of the pull-down network. The specific implementation is to exchange the serial-parallel mode of the MOS transistors in the pull-down network and the N/P attributes of the MOS transistors to obtain a new network that is the pull-up network. In terms of operation, for NMOS tubes, series connection means to do the method operation, parallel means do the addition operation, and vice versa [5].
2.2. The design principle of inverter based on Multisim

What the NOT gate realizes is that the logic function is out = -in, which means that the input signal is reversed, so it is also called an inverter. The gate level diagram is as in Figure 3.

![Figure 2](image2.png)

**Figure 2. Two-input complementary logic gate structure**

![Figure 3](image3.png)

**Figure 3. The gate level diagram [2]**

The corresponding CMOS structure is as follows in Figure 4: it is composed of a PMOS and NMOS, PMOS is pulled up and connected to VDD; NMOS is pulled down and connected to GND.

![Figure 4](image4.png)

**Figure 4. Corresponding CMOS structure [2]**

When the input is 0 (low level), the output is 1 (high level), that is, the output is connected to the power supply VDD; when the input is 1 (high level), the output is 0 (low level), that is, the output must be connected to GND (ground). Therefore, the equivalent circuit of the above NOT gate CMOS circuit is as follows:

![Figure 5](image5.png)

**Figure 5. NOT gate CMOS circuit [2]**
As in Figure 5, when the input is 0, switch k1 is closed and k2 is opened, that is, the output is connected to VDD, and the output is 1. When in is 1, the switch k1 is opened and k2 is closed, that is, the output is connected to GND, and the output is 0.

PMOS is equivalent to a switch, as follows in Figure 6, when the G terminal is low, the D terminal and the S terminal are connected.

![PMOS Diagram](image)

Figure 6. PMOS [2]

NMOS is equivalent to a switch, as follows in Figure 7, when the G terminal is high, the D terminal and the S terminal are connected.

![NMOS Diagram](image)

Figure 7. NMOS [2]

![Inverter Diagram](image)

Figure 8. Inverter

![Simulation Results](image)

Figure 9. Simulation results
Through the simulation of the circuit in Figure 8, during the test time, the input waveform (Figure 9) is ultimately opposite to the output waveform displayed on the oscilloscope. When the input is high, the output is exactly low, and the error is within the allowable range.

3. Transient characteristics of CMOS inverter based on Multisim

The transient characteristics of the inverter can be expressed by the rise time and fall time of the inverter. The rise time $t_r$ is the time required to make the output level of the inverter from 0.1vdd to 0.9vdd, and the fall time $t_f$ is defined as the time required for the output level to fall from 0.9vdd to 0.1vdd. Set the input high level inverter to 1.8V and the input low level to 0V [4].

Similarly, the output high level and low level are 1.8V and 0V respectively. It can also be found that the potential of input and output is just the opposite, which satisfies $V_{out} = \overline{V_{in}}$. According to the design requirements, select the appropriate aspect ratio, so that the inverter input flip level is exactly half of the supply voltage, $V_{it} = 0.5V_{DD}$. Through transient simulation, the rise time and fall time of inverter are obtained. It can be found from Figure 10 that the threshold voltage $V_{it}$ is approximately equal to 0.9V, and it is not difficult to find that the rise time is about 1US and the fall time is about 0.7us.

When NMOS transistors transmit at high level, threshold loss occurs, while PMOS transistors transmit at low level, threshold loss occurs. As a result, the CMOS process combines two different MOS transistors. Moreover, when the output is high or low, only one MOS transistor in the CMOS inverter is on. Theoretically, there is no current between the power supply and the ground, and there is no static power consumption. The power consumption of the CMOS inverter is very low, which is also the biggest advantage of the CMOS inverter circuit [1].

![Figure 10. DC voltage transmission characteristic curve of CMOS inverter](image)

4. Design principle of inverter based on Cadence

The not gate (inverter) has an input and an output. The input is in and the output is out. When the input is high level, the output is low level, when the input is low level, the output is high level. Output $OUT = \overline{IN}$.

Table 1. Not gate (inverter) truth table

| IN | OUT |
|----|----|
| 0  | 1  |
| 1  | 0  |

Inverter used in digital integrated circuits can reverse the phase of the input signal by 180 degrees, which is the gate circuit for reverse operation. At this time, the MOS transistor works in the on-off state. But when the MOS transistor works in the transition region, it can play the role of amplification, and can be used in audio amplification or clock oscillator [6].

The inverter circuit is composed of a NMOS transistor (N transistor) and a PMOS transistor (P transistor). The source of P transistor is connected with high level $V_{DD}$, and the source of N transistor...
is connected with low level $V_{SS}$. Input in controls the conduction and cutoff of P transistor and N transistor. When the input in level is low, the P transistor is on, the N transistor is off, and the output out level is high; When the input in level is high, the N transistor is on, the P transistor is off, and the output out level is low. In this way, the logic operation of the inverter (not gate) can be achieved. The inverter (not gate) circuit and transient simulation results are shown in the Figure 11, Figure 12 and Figure 13.
5. Transient characteristics of CMOS inverter based on Cadence

The transient characteristics of the inverter can be expressed by the rise time and fall time of the inverter. The rise time $t_r$ is the time required to make the output level of the inverter from 0.1vdd to 0.9vdd, and the fall time $t_f$ is defined as the time required for the output level to fall from 0.9vdd to 0.1vdd. Set the input high level of Figure 11 inverter to 1.8V and the input low level to 0V [8].

Similarly, the output high level and low level are 1.8V and 0V respectively. It can also be found that the potential of input and output is just the opposite, which satisfies $V_{out} = \overline{V_{in}}$. According to the design requirements, select the appropriate aspect ratio, so that the inverter input flip level is exactly half of the supply voltage, $V_{it} = 0.5V_{DD}$. Through transient simulation, the rise time and fall time of inverter are obtained. It can be found from Figure 14 that the threshold voltage $V_{it}$ is approximately equal to 0.9V, and it is not difficult to find that the rise time is about 1US and the fall time is about 0.7us.

When NMOS transistors transmit at high level, threshold loss occurs, while PMOS transistors transmit at low level, threshold loss occurs. As a result, the CMOS process combines two different MOS transistors. Moreover, when the output is high or low, only one MOS transistor in the CMOS inverter is
on. Theoretically, there is no current between the power supply and the ground, and there is no static power consumption. The power consumption of the CMOS inverter is very low, which is also the biggest advantage of the CMOS inverter circuit [7].

6. Conclusion
In this paper, the classic static CMOS logic gate circuit of the inverter is simulated by Multisim and cadence simulation software, and the correct simulation results are obtained. The rise time and fall time of the inverter and the relationship between the input and output level and the power supply voltage are verified. On this basis, the NAND gate is optimized and simulated by using pseudo NMOS structure.

The structure has the following excellent characteristics: (1) the number of quality tubes is reduced by nearly half and the power consumption is greatly reduced. (2) The load terminal is connected with smaller loads, which increases the effective utilization area of the layout. (3) The processing difficulty is small and the processing cost is reduced (4) The CMOS noise immunity is high.

Because CMOS inverter is one of the basic units of static CMOS logic circuit and an important part of integrated circuit design, it is very important to verify its working principle and switching characteristics.

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