Digital pulse-width modulator with spread-spectrum emission reduction

T. Karaca, M. Auer

1. Introduction

Pulse-width modulators (PWM) are one of the core blocks of many power-electronic circuits. PWMs are used to encode an amplitude signal into a rectangular signal with varying pulse-width. They are needed especially in switched-mode power circuits, such as DC-DC converters, servo-motor drivers and power-amplifiers. In these applications, the active power components are operated as switches in order to achieve a high power efficiency and PWMs are needed to control these switches. Using PWM control, some state-of-the-art circuits achieve power-efficiency figures in excess of 95% [1].

Despite their high power efficiency, switched-mode circuits using PWM have a major drawback. These circuits are prone to create electromagnetic emission. These emission can interfere with the functional integrity of other circuits inside the same device or violate legal emission limits as specified by EN or FCC regulations. The conventional way to deal with these emission is to apply filtering and shielding measures [2]. However, adding such additional components to a device is often not applicable due to cost or space requirements. Therefore several techniques have been developed to reduce the creation of emission already inside the switched mode circuit.

Slew-rate control methods [3, 4] are frequently used to reduce electromagnetic emission. The principle idea is to control the speed of voltage transitions at the power switches, thereby reducing high frequency noise. A drawback of these methods is their negative impact on power efficiency. Still, these methods are used in many applications [3–5] to counter high-frequency emission above 30 MHz. Therefore several techniques have been developed to reduce the creation of emission already inside the switched mode circuit.

Slew-rate control methods [3, 4] are frequently used to reduce electromagnetic emission. The principle idea is to control the speed of voltage transitions at the power switches, thereby reducing high frequency noise. A drawback of these methods is their negative impact on power efficiency. Still, these methods are used in many applications [3–5] to counter high-frequency emission above 30 MHz.
The paper is organized as follows: Sect. 2 introduces the basic principles of PWMs and SSM, Sect. 3 presents the proposed digital PWM, describing the implementation in detail, Sect. 4 shows the application of the proposed PWM. An FPGA based prototype of a Class-D audio amplifier is presented and measurement results are given. Finally Sect. 5 summarizes the works.

2. Pulse width modulators and spread-spectrum modulation

Figure 1 shows the main building blocks and Fig. 2 the operation principle of a typical PWM. The PWM is used to encode an amplitude signal into a rectangular signal with varying pulse-width. The average of the resulting rectangular signal ideally represents the input amplitude signal. The created signal has only two levels and can be directly used to control a power-switch. As switches ideally do not dissipate power, a PWM in combination with a switch can be used to build a very power efficient voltage conversion system. Even for non-ideal switches the losses can be kept low and highly efficient systems are possible.

The PWM typically consists of two main building blocks, a reference signal generator and a comparator. The reference signal generator creates a sawtooth or triangle waveform. Triangle waveforms are preferred in many applications, as the resulting PWM signal shows lower unwanted harmonics [14]. The fundamental frequency of this reference signal is at least twice the input signal bandwidth. In many practical applications fundamental frequencies of 0.1 MHz to 1 MHz are used. The comparator detects the intersection points of the input signal with the reference signal, thereby creating a pulse width modulated rectangular output signal.

The output signal $y(t)$ of the PWM with triangular reference signal can be mathematically described as [14]:

$$y(t) = x(t) + \sum_{k=1}^{\infty} \frac{2(-1)^k}{k\pi} \left[ \sin \left( 2\pi kf_\text{R} t + k\pi \frac{x(t) + 1}{2} \right) - \sin \left( 2\pi kf_\text{R} t - k\pi \frac{x(t) + 1}{2} \right) \right]$$

with the fundamental frequency $f_\text{R}$ of the triangle waveform, and input signal $x(t)$. In typical applications, $f_\text{R}$ is at least an order of magnitude higher than the highest frequency in $x(t)$. Thus the resulting signal $y(t)$ can be divided into a low frequency and a high frequency part. The low frequency part of $y(t)$ perfectly encodes $x(t)$, without adding any distortion or unwanted signal components. This feature is used in many power amplifiers processing band-limited input signals. The high frequency part of $y(t)$ consists of harmonics of the reference signal, each being phase modulated by the input signal. This high frequency content is unwanted in most applications and is a root cause of the created emissions. The energy of this unwanted signal content is concentrated around ($\pm f_\text{R}$) and can propagate to other electronic circuits via various coupling mechanisms and thereby create interference.

Spread-spectrum modulation (SSM) [6] is a well known technique to reduce interference created by clocked electronic circuits. These circuits, such as synchronous digital electronics often create emission at their clock frequency and multiples of it. A reduction of the created emission amplitudes can be achieved by using a variable frequency clock instead of a fixed frequency one. For instance in digital communication [15] the frequency of the digital clock is modulated with a certain pattern. This causes the emission to no longer being concentrated at fixed frequencies, but being spread over a larger frequency band, resulting in a signal that has a smaller overall amplitude. Figure 3 illustrates the resulting emission spectra.

This idea has been applied to various analog PWM [7–10]. The implementation is as follows: Instead of using a reference generator that creates a triangle signal with a fixed frequency $f_\text{R}$, a variable frequency reference generator is used which has an output frequency confined to $f_\text{R} \pm \Delta f$. The variable frequency reference generator can be implemented having either a pseudo-random frequency pattern, or a periodic frequency pattern. Our previous works [16] have revealed that periodic frequency modulation generally leads to better emission reduction for the same frequency deviation $\Delta f$. In such periodic SSM implementations, the reference triangle signal is frequency modulated by $\pm \Delta f$ using a periodic modulation signal of frequency $f_\text{m}$. The result is, that the energy of $y(t)$'s unwanted signal

![Fig. 1. Simplified block diagram of a PWM driving a power-switch](image1)

![Fig. 2. Operation principle of the PWM: waveforms at the different nodes](image2)

![Fig. 3. Frequency domain representation of a clocked circuit's emission, with and without SSM](image3)
content is no longer concentrated around \(k f_0\), but is distributed over a larger bandwidth. This bandwidth can be roughly estimated for \(k = 1\) using Carson’s rule as: 
\[ 2 \left( \Delta f + f_m \right) . \]

However, quantifying the achieved emission reduction is not straightforward. Sometimes simply the spectrum of the created emission is measured. The obtained results heavily depend on the used measurement instrument, in particular on its effective frequency resolution. Various quantification setups can be found in the literature [7, 9–11] and in datasheets [17] of devices using SSM. This makes comparison of different SSM implementations very difficult if not impossible. We believe, that an EMI-Test-Receiver as specified in CISPR16-1-1 should be used to quantify the emission reduction of an SSM method. These instruments have standardized measurement characteristics and are used in legal emission measurements according to EN/FCC regulations. Thus the use of a CISPR-16 conformal EMI-Test-Receiver leads to fair and comparable results of emission reduction larger than 6 dB, the frequency deviation \(\Delta f\) should be chosen according to the simulated signal.

For comparability, it was decided, that the PWM should have \(N_S = 128\) on average. Thus the SSM-PWM is implemented using an 8-bit up-down counter with configurable upper and lower bounds. It counts up, until it reaches the set upper bound, then starts counting down until it reaches the set lower bound and vice versa. To implement a triangular modulation profile, the upper and lower bounds have to be increased stepwise and then accordingly decreased. This is achieved with two additional up-down counters to determine the bounds. One of these additional counters is updated whenever the main counter reaches its set upper bound, the other at the set lower bound. Each of the additional counters has \(N_{SSM}\) steps. Thus, the upper bound of the PWM counter can be altered by \(N_{SSM} + 1\) and the lower bound can by altered by the same amount. Therefore, the main counter has \(N_S = 128 \pm N_{SSM}\) steps. As the upper and lower bound is modified at every cycle, \(N_S\) changes by two every PWM cycle.

Finally, \(N_{SSM}\) was selected to be 14, leading to a triangular modulated PWM with \(f = 390 \pm 43\) kHz and \(f_m = 44\) kHz. Figure 4 shows the VHDL simulation of the implemented reference signal with SSM. In the end a third additional up-down counter was added, to track the current number of PWM steps, as this value was needed for error-correction. In the implementation, all the additional counters are clock-gated, as they are incremented infrequently. The implementation consumes 120 µW and needs 8100 µm² of silicon area.
3.1 Multiplier based error correction
The digital input signal $x[m]$ of a non-SSM PWM with $N_{SSM}$ counter steps is mapped to a duty-cycle ($DC$) of

$$DC = \frac{x[m]}{N_{SSM}} \quad \text{with } x[m] \in [0; N_{SSM}]$$

Altering the number of counter steps to $N_{SSM}$ leads to an erroneous duty-cycle $DC = \frac{x[m]}{N_{SSM}}$, which can be corrected by multiplying the input value $x[m]$ with a correction factor $N_{SSM}/N_{SSM}$.

Thus, one way to correct for the introduced error is to multiply the input value $x[m]$ with the current number of steps in the counter then divide the result with the average number of steps. In this case, this number is $128 (2^7)$ and the division can easily be implemented with a right shift operation. The current number of steps is provided by the SSM-PWM, and can be represented by an 8-bit unsigned number, the input signal is a 8-bit 2’s complement number. The multiplier and shift operation is added as asynchronous combinational block in front of the SSM-PWM and provides an 8-bit 2’s complement number to the SSM-PWM. The multiplier, implemented using a non-booth algorithm, consumes 7 µW and needs 3400 µm² of silicon area.

3.2 Look-up table based error correction
For comparison, it was evaluated, whether a look-up table (LUT) replacing the multiplier could reduce area and power consumption. The error-correction needs to consider $2 \times N_{SSM} + 1 = 29$ possible mappings of all the input values. With 8-bit input values and 8-bit output values, the LUT needs 7.25 kB. For a first estimate, no data reduction was considered. Again, the LUT will be placed as asynchronous combinational block in front of the SSM-PWM. The LUT is implemented as ROM, consumes 40 µW and needs 38000 µm² of silicon area. As can be seen, significant data reduction would be needed, to achieve a better performance, than the multiplier. Consequently, for this work the error correction using a multiplier was chosen. Table 1 summarizes all the estimated implementation parameters.

### Table 1. Area and power consumption of the digital blocks. Implemented in 180 nm CMOS width 1.8 V supply and clock frequency $f_c = 100$ MHz. Input signal: 8-bit PCM sampled at $f_c/128$

| Block                        | Area [µm²] | Power [µW] |
|------------------------------|------------|------------|
| Reference PWM                | 2300       | 90         |
| SSM-PWM                      | 8100       | 120        |
| Error correction, multiplier | 3400       | 7          |
| Error correction, LUT        | 38000      | 40         |

4. A digitally-controlled Class-D audio amplifier
Before going to silicon, a rapid-prototype was developed. In this way the feasibility of the proposed SSM-PWM could be easily evaluated and the actual emission reduction could be measured. The prototype is a PWM based Class-D audio amplifier. These kind of amplifiers have become very popular for driving loudspeakers in a very power efficient way. Figure 5 shows a simple block diagram of the amplifier. The PWM block converts the input signal into a pulse-width modulated signal. It outputs two differential PWM-signals, which drive a switching power-stage. The amplified signal is directly applied to an electrodynamic loudspeaker. The loudspeaker has an intrinsic low-pass behavior, such that only the low-frequency content of the output PWM-signal contributes to the generated sound.

The prototype is built using an FPGA to implement the digital blocks. Figure 6 shows a picture of the prototype. The power stage is build of discrete MOS-transistors controlled by off-the-shelf integrated drivers. The power stage is supplied with 5 V and can drive up to 1.5 W into a 8 Ω loudspeaker. Additionally, a small mixed signal control loop was added around the PWM and power-stage to improve the audio performance. The control-loop mainly suppresses errors induced by the power switches and performs quantization-
noise shaping to achieve a higher dynamic range in the audible bandwidth. As before, the FPGA was clocked at 100 MHz. The described reference PWM and the proposed SSM-PWM are ported to the FPGA. In contrast to the PWM implementations above, a second digital comparator was added to generate the second output signal.

This prototype was used to evaluate the emission reduction when using the proposed PWM with SSM. For the evaluation, the 150 Ω direct-coupling measurement setup according to IEC 61967 was used. Figure 7 shows the setup. This measurement setup is actually intended to measure the emission of integrated circuits. Yet, as this setup allows comparable and repeatable results it was considered very suitable for this task. Using a matching network, the common-mode voltage on the speaker lines is probed. This common-mode voltage is considered one of the root-causes of interference. The signal is measured with a CISPR-16 conformal EMI-Test-Receiver in CISPR-Band B (0.15 MHz to 30 MHz). The peak detector is used with a dwell-time of 10 ms. The amplifier was loaded with a loudspeaker dummy consisting of 8 Ω and 44 µH in series. The measurements were carried out with a 1 kHz input signal, creating 1 W at the load.

Figure 8 shows the emission spectra for the reference PWM and the SSM-PWM. The emission spreading effect is clearly visible. An emission reduction of 5 dB at the fundamental PWM harmonic and 9.5 dB at the third harmonic is achieved.

Next, the performance of the error-correction circuitry is evaluated. For this reason, the total harmonic distortion and noise ratio (THD+N) was measured using an audio analyzer. In this measurement, a high quality sinusoidal signal is applied to the Class-D audio amplifier. The amplifier’s output spectrum is measured in the audible range (20 Hz to 20 kHz). Then the power of the amplified sinusoidal signal $P_{VD, N}$ is compared to the power of all the additional signals $P_{VD, N}$ present at the output. $P_{VD, N}$ typically consists of harmonic distortion components created by the amplifier’s non-linearity and noise components added by the amplifier. THD+N is calculated as:

$$THD + N = \frac{P_{VD, N}}{P_{VD, N}} \text{ typically notated in } % \quad (3)$$

For this measurement, the amplifier was again loaded with the loudspeaker dummy and the input signal amplitude was swept. In this way, also the clipping behavior of the amplifier can be evaluated. Figure 9 shows the result for the reference PWM and the SSM-PWM with and without error-correction. The THD+N is plotted versus the power at the dummy load. The implemented error-correction circuitry significantly improves the audio performance. Still there is a small penalty of about 0.006% in THD+N compared to the reference PWM. Without error correction, the amplifier starts clipping very early. Thanks to the error-correction the linear output range is completely restored.

5. Conclusion

In this work, we presented a spread-spectrum implementation for digital PWM which is compatible with highly linear voltage converters. The area and power overhead of the presented emission reduction method was shown for a fully integrated implementation. Finally the proposed implementation was tested on an FPGA prototype, showing impressive emission reduction of up to 10 dB, with only minor impact on the signal conversion performance. Although higher reduction is possible using more elaborate methods, this technique clearly stands out owing to its lightweight implementation with low overhead and low power consumption. For comprehensive emission reduction, the proposed digital SSM implementation can be easily combined with a slew-rate controlled power-stage (such as [4] or [5]). In this way, emission created by the low order harmonics of the PWM’s reference signal are reduced by SSM. The high-order harmonics are countered by slew-rate control.

Acknowledgements

Open access funding provided by Graz University of Technology.
Digital pulse-width modulator with spread-spectrum emission reduction

**Authors**

**Timuçin Karaca**

Received the master degree in electrical engineering (Dipl.-Ing.) from Graz University of Technology, Austria, in 2014. In his master thesis he worked with NXP Semiconductors on the design of ultra-low power voltage regulators for Systems-on-Chip. Currently, Timuçin Karaca is working towards his Ph.D. degree at the Institute of Electronics, Graz University of Technology. His research interests involve analog circuit design, switched power circuits and electromagnetic compatibility.

**Mario Auer**

Is assistant professor at the Institute of Electronics, Graz University of Technology, Austria. He is working in the field of microelectronics, integrated analog circuit design and electromagnetic compatibility. His research interests are the design of highly efficient analog circuits and the design of robust analog building blocks.

**References**

1. Jiang, X., Song, J., Cheung, D., Wang, M., Arunachalam, S. K. (2014): Integrated class-d audio amplifier with 95% efficiency and 105 dB SNR. IEEE J. Solid-State Circuits, 49, 2387–2396.
2. Ditt, N. (2009): Electromagnetic compatibility engineering. New York: Wiley
3. Deutschmann, B., Ostermann, T. (2003): CMOS output drivers with reduced ground bounce and electromagnetic emission. In Proceedings of the 29th European solid-state circuits conference (ESSCIRC), Portugal, September (pp. 537–540).
4. Subotkaya, V., Bodano, E., Deutschmann, D. (2017): Adaptive current source driver for high-frequency boost converter. In Proceedings of the 11th international workshop on the electromagnetic compatibility of integrated circuits, St. Petersburg, Russia, July (pp. 85–90).
5. Karaca, T., Auer, M. (2017): A class-D output bridge with dynamic dead-time, small delay and reduced EMI. In 2017 IEEE international symposium on circuits and systems (ISCAS), Baltimore, USA, May (pp. 1–4).
6. Hardin, K., Fessler, J., Bush, D. (1994): Spread spectrum clock generation for the reduction of radiated emissions. In IEEE international symposium on electromagnetic compatibility, Chicago, USA, August (pp. 227–231).
7. Tanaka, T., Ninomiya, T., Harada, K. (1989): Random-switching control in DC-to-DC converters. In 20th annual IEEE power electronics specialists conference, Milwaukee, USA, Juny (pp. 500–507).
8. Edwards, C., Easson, C., Kihuri, M., Doy, A. (2005): Efficient minimum pulse spread spectrum modulation for filterless class D amplifiers. US Patent 6847257.
9. Boudjenda, N., Melit, M., Nekhoul, B., El khamlichi Drissi, K., Kernsso, K. (2008): Spread spectrum in DC-DC full bridge voltage converter by a dual randomized PWM scheme. In IEEE international symposium on electromagnetic compatibility (EMC Europe) 2008, Hamburg, Germany, September.
10. Ming, X., Chen, Z., Zhou, Z., Zhang, B. (2009): An advanced spread spectrum architecture to improve EMI emissions in class D amplifier. In International conference on communications, circuits and systems (ICCCAS), Milpitas, USA, July (pp. 661–665).
11. Tse, K., Chung, H., Hui, S., So, H. (2000): A comparative investigation on the use of random modulation schemes for DC/DC converters. IEEE Trans. Ind. Electron., 47, 253–263.
12. Trescases, O., Wei, G., Prodic, A., Ng, W. T. (2007): An EMI reduction technique for digitally controlled SMPS. IEEE Trans. Power Electron., 22, 1560–1565.
13. Dousoky, G. M., Broyama, M., Ninomiya, T. (2011): FPGA-based spread-spectrum schemes for conducted-noise mitigation in DC-DC power converters: design, implementation, and experimental investigation. IEEE Trans. Ind. Electron., 58, 429–435.
14. Song, Z., Sarwate, D. (2003): The frequency spectrum of pulse width modulated signals. Signal Process., 83(10), 2227–2236.
15. HP, Intel, Microsoft, NEC, ST/NXP Wireless and TI (2008): Universal Serial Bus 3.0 Specification.
16. Karaca, T., Auer, M. (2016): Characterization of EMI-reducing spread-spectrum techniques for class-D audio amplifiers. In Asia-Pacific international symposium on electromagnetic compatibility (APEMC), Shenzhen, PRC, May (pp. 791–793).
17. Maxim Integrated (2008): MAX9768: 10W mono class D speaker amplifier with volume control (Rev. 2).
18. Gonzalez, D., Balcells, J., Santolaria, A., Bunetel, J. C. L., Gago, J., Magnon, D., Brebaut, S. (2007): Conducted EMI reduction in power converters by means of periodic switching frequency modulation. IEEE Trans. Power Electron., 22, 2271–2281.
19. Shepherd, J., Rolland, E., Abouda, K., Meurier, P. (2009): Getting the most out of frequency spreading. Freescale Semiconductor.
20. Deutschmann, B. (2013): Spread spectrum clocking for emission reduction of charge pump applications. In 9th intl. workshop on electromagnetic compatibility of integrated circuits (EMC Compo), December (pp. 123–128).