Dynamic Behaviors and Training Effects in TiN/Ti/HfO$_x$/TiN Nanolayered Memristors with Controllable Quantized Conductance States: Implications for Quantum and Neuromorphic Computing Devices

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Abstract

Controllable quantized conductance states of TiN/Ti/HfO$_x$/TiN memristors are realized with great precision through a pulse-mode reset procedure, assisted with analytical differentiation of the condition of the set procedure, which involves critical monitoring of the measured bias voltage. An intriguing training effect that leads to faster switching of the states is also observed during the operation. Detailed analyses on the low- and high-resistance states under different compliance currents reveal a complete picture of the structural evolution and dynamic behaviors of the conductive
filament in the HfO$_x$ layer. This study provides a closer inspection on the quantum-level manipulation of nanoscale atomic configurations in the memristors, which helps to develop essential knowledge about the design and fabrication of the future memristor-based quantum devices and neuromorphic computing devices.

Keywords: HfO$_2$, filament, resistive random-access memory (RRAM), memristor, oxygen vacancy, resistive switching, conductance quantization, training effect

1 Introduction

Memristors with high scalability, low power consumption, and multilevel switching is one of the promising candidates for artificial synapses in neuromorphic computing to replace the conventional von-Neumann architecture.$^{1-3}$ Linear conductance of a memristor in a wide voltage range is pursued for the purpose of implementing vector-matrix multiplication in conductance programming for memristor arrays.$^{4-6}$ Nonlinear memristor dynamics due to intrinsic conduction mechanisms$^{7-9}$ are therefore one of the key challenges to build memristor-based dot-product engines.

In the mean time, quantized conduction in memristor-based devices is being introduced to this field for its great potential for high-density data storage through multilevel switching, and for analog synaptic weight update in effective training of the artificial neural networks.$^{10,11}$ While implementations of quantum neuromorphic computing platforms with quantum memristors are being proposed,$^{12,13}$ realization of these architectures remains difficult because conductance quantization of the memristors suffers significant instability in terms of endurance and tuning accuracy, which includes large half-widths in the histogram of the quantized conductance.$^{14,15}$ The occurrence of conductance quantization seems unstable and random even when an optimal condition is used in the measurement.$^{16-18}$ The mechanism that guarantees conductance quantization in a memristor remains a mystery. The detailed atomic dynamics of the conductive filaments in the memristors is not yet fully
explored and therefore demands more research.

In this letter, we have made in-depth investigations on conductance characteristics of bipolar TiN/Ti/HfO$_x$/TiN valence-change memristors (VCMs), aiming to look into the instability issue of the quantized conductance. The dynamics of the set procedure is observed to be decisive for the quantization performance in the reset procedure. Detailed analyses on the low-resistance state (LRS) have also been conducted to explicitly explore the electrical characteristics associated with the nanoscale atomic structure of the conductive filament in the HfO$_x$ layer. With better understanding of the atomic dynamic behaviors of the conductive filament, we are able to perform a precise control of the quantized conductance states of the memristors.

2 Device Fabrication and Measurement Methods

Fig. 1 shows the device layout of the TiN/Ti/HfO$_x$/TiN memristor. A 300-nm SiO$_2$ layer was grown via wet oxidation on a lightly doped p-type Si(100) substrate. The SiO$_2$ layer serves as an insulating layer between the Si substrate and the bottom electrodes, which were formed by depositing TiN (50 nm)/Ti (50 nm) using radio-frequency (rf) sputtering. After that, a 10-nm switching layer of HfO$_2$ was formed with atomic layer deposition, followed by a deposition of TiN (40 nm)/Ti (10 nm) layer as top electrodes. Lithography and inductively-coupled-plasma (ICP) etching were then used to define the active cell area. Then, a low-temperature oxide (LTO) SiO$_2$ layer was deposited, followed by lithography and ICP etching to create via-hole structures in LTO. Finally, AlCu/TaN contacts for the electrodes were formed via lithography and rf sputtering. The electrical characteristics are measured at room temperature using Keithley 2400 and Agilent B1500A. The bias voltages are applied to the top electrodes as the bottom electrodes are grounded during electrical measurements.
3 Results and Discussion

3.1 Measurements with the DC Voltage Sweep Mode

Electrical measurements are performed on several devices with the same structure as described in Section 2, and the results are found to be similar and reproducible. The data presented in this paper are measured from a device with a cell area of 0.36 µm². The forming procedure before the electrical measurements for each device is described in detail in Supporting Information Section S1. Two representative current-vs.-voltage (I–V) curves in the dc voltage sweep mode of the memristor operation are shown in Fig. 2, one with signatures of conductance quantization in the reset procedure and one without. A compliance current (I_c) is applied during each set procedure to prevent permanent breakdown. The
Figure 2: Currents in a log scale as functions of voltage with the compliance current for the set procedure $I_c = 135 \, \mu\text{A}$ (blue curve) and $60 \, \mu\text{A}$ (red curve), respectively. A stepwise feature is observed during the reset of the curve with $I_c = 60 \, \mu\text{A}$, and its blown-up view in a linear scale is shown in the inset. The stepwise feature is absent from the curve with $I_c = 135 \, \mu\text{A}$.

$I-V$ curve with $I_c = 135 \, \mu\text{A}$ (blue curve) shows the standard electrical characteristics with a steep drop in $I$ at $-0.85 \, \text{V}$ in the reset procedure after the current reaches a maximum, whereas the one with $I_c = 60 \, \mu\text{A}$ (red curve) exhibits a series of descending steps (boxed with dashed lines) starting at a smaller bias voltage of $-0.38 \, \text{V}$. The steps correspond to the quantized conductance of a conducting channel in the switching layer, which reveals the nanoscale atomic-level reaction of a conductive filament consisting of oxygen vacancies in the switching layer.$^{14,19-22}$ During the reset procedure as the current is slowly switched from LRS to the high-resistance state (HRS), the quantum point contact of the filament that touches the negatively-charged top Ti electrode thins further and further because the oxygen vacancies of the filament are gradually removed under the voltage stress through recombination of the oxygen vacancies of the filament and oxygen ions from the Ti layer.$^{21}$
Figure 3: Representative examples of conductance quantization during the reset procedure with $I_c = 60 \, \mu A$. Conductance plateaus occur at half-integer multiples of $2e^2/h$.

After the last oxygen vacancy in contact is removed, breaking the circuit established by the filament, a Schottky barrier is created in the conduction.\textsuperscript{23}

The corresponding conductance of the quantum point contact in the reset procedure of the $I_c = 60 \, \mu A$ curve in Fig. 2 is calculated and expressed in terms of the conductance quantum $G_0 = 2e^2/h$ in Fig. 3(a), along with other examples of conductance quantization of the device shown in Figs. 3(b)–3(d). In each set-and-reset cycle, the voltage is swept at a rate of $\Delta V = \pm 10 \, \text{mV}$ per 0.5 second for each data point, except for the reset procedure from $-0.35 \, \text{V}$ to $-1 \, \text{V}$, during which the sweep rate is decreased to $\Delta V = -2 \, \text{mV}$ per 0.5 second to gently process the switching of the quantized conductance states. The resistance in series with the atomic point contact must be taken into consideration to precisely extract the quantized conductance of the point contact.\textsuperscript{19,24} It can be seen that the conductance plateaus occur at some of the half-integer multiples of $G_0$. Fig. 4 summarizes the numbers of counts of respective values of the conductance plateaus collected from 330 $I-V$ curves using various $I_c$ (listed in Table 1). The histogram clearly demonstrates the tendency of the device to yield quantized conductance. The appearance of half-integer multiples of $G_0$ instead of merely integer multiples is not universal in atomic point contacts. It is suggested
to be caused by the chemical potential difference between the two carrier reservoirs across the filament,\textsuperscript{25} rearrangement of the atomic contact configuration,\textsuperscript{26} or possible weak magnetism from oxygen vacancies that may lift spin degeneracy.\textsuperscript{14}

The compliance current $I_c$ for the set procedure plays an important role in search of the quantized conductance states of a memristor. The set procedures have been performed with different $I_c$ from 165 to 40 µA, with 30 set-and-reset cycles completed for each $I_c$. The statistics of the results from a memristor with a cell area of 0.36 µm$^2$ are listed in Table 1. (Statistics from other devices with different cell areas show the similar behaviors; see Supporting Information Section S3. Temperature dependence of the electrical characteristics is also studied, as shown in Supporting Information Section S4.) All the curves that exhibit conductance quantization in the reset procedure (see the row “w/ Quant.”) belong to the \textit{fair-set} group (definition in the next paragraph). The chance of observing conductance quantization in the reset procedure stays zero for $I_c = 165$ µA to 105 µA, and then gradually increases to 50% as $I_c$ is gradually decreased to 70 µA, and then reaches the maximum 67% when $I_c = 60$ µA. The percentage then decreases to 33% as $I_c$ is decreased further to 40
Table 1: Numbers of counts of various set conditions using different $I_c$. (a) Good sets. Bottom row: good sets with SCLC in LRS. (b) Fair sets. Bottom row: fair sets with quantized conductance in the reset procedure. Notice that the fair-set category is the only category in which current quantization in the reset procedure can be observed. (c) Poor sets. (d) Set failures.

| $I_c$ (µA) | 165 | 150 | 135 | 120 | 105 | 90  | 80  | 70  | 60  | 50 | 40 |
|-----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|----|
| a) Good set | 30  | 30  | 30  | 30  | 30  | 23  | 20  | 11  | 5   | 4  | 0  |
| w/ SCLC   | 19  | 18  | 20  | 17  | 20  | 11  | 7   | 4   | 3   | 0  | 0  |
| b) Fair set | 0   | 0   | 0   | 0   | 0   | 7   | 10  | 18  | 21  | 15 | 17 |
| w/ Quant. | 0   | 0   | 0   | 0   | 0   | 6   | 10  | 15  | 20  | 12 | 10 |
| c) Poor set | 0   | 0   | 0   | 0   | 0   | 1   | 4   | 8   | 10  |    |    |
| d) Set failure | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 3   | 3  | 3  |

µA. This is an $I_c$ so small that a good set (definition in the next paragraph) can barely be acquired. With the highest yield of conductance quantization, $I_c = 60$ µA is considered to be the optimal condition for later operation of the memristor for controlling the quantized conductance states.

The electrical characteristics of the set-and-reset cycles can be generally classified into five categories, as illustrated in Fig. 5 with representative examples. (More examples are presented in Supporting Information Section S2.) The blue dashed curves are plotted against the programmed bias voltage provided by the voltage source, whereas the red solid curves are plotted against the measured bias voltage ($V_m$). The only discrepancy between them lies in the set procedure when the resulting current abruptly jumps high to hit $I_c$. The five categories are as follows:

1. **Good set with space-charge-limited current (SCLC)** (Figs. 5(a) and 5(b)): The conduction in LRS after the set procedure is ohmic with a resistance of 2.0–4.0 kΩ (mostly around 3 kΩ), followed by a significant slope increase (boxed with dashed lines) at a negative voltage ($-0.48$ V in the representative example), known as the SCLC feature. The current then gradually increases to a maximum before it drops abruptly into HRS in a reset procedure (at $-0.85$ V in Fig. 5(a) and $-0.61$ V in Fig. 5(b)). A good set procedure is featured with an $I–V_m$ curve hitting $I_c$ at only one
point for a stay, indicating a very stable $V_m$.

2. **Good set without SCLC** (Fig. 5(c)): This has similar features with the previous category, except that it tends to undergo the reset process at smaller voltages ($\sim 0.18 \text{ V smaller on average}$), and the SCLC signature is missing. (At the spot in the dashed box, it seems almost entering the SCLC regime especially when compared with Fig. 5(b), but the filament fails to hold for it. More discussion about the SCLC is presented in the following contexts and in Supporting Information Section S2.1.) Tiny fluctuations are observed at larger negative bias voltages in LRS, before the reset procedure takes place (at $-0.59 \text{ V in this example}$).

3. **Fair set** (Fig. 5(d)): The conduction in LRS after the set is ohmic with a resistance of 4.8–7.5 kΩ (mostly around 6 kΩ), which is about twice larger than those in the good-set cases. Tiny fluctuations are usually observed at larger bias voltages in the ohmic state. The reset procedure starts at an even smaller bias voltage ($-0.38 \text{ V in this example}$), but with a progressive phase that is prolonged to a more negative bias voltage. A fair set procedure is featured with an $I-V_m$ trace frequently wiggling left and right along the horizontal compliance line. This is the *only* category in which current quantization in the reset procedure can be observed. Notice that $I_c = 60 \mu\text{A}$ in both Figs. 5(c) and 5(d). In very few cases where quantization is absent (not presented in Fig. 5), the reset process exhibits chaotic noise-like fluctuations similar to those found in Fig. 5(e).

4. **Poor set** (Fig. 5(e)): The conduction in LRS is no longer ohmic, but follows the Schottky-emission equation, with resistance considerably higher than that in the fair-set cases. A poor-set procedure is also featured with an $I-V_m$ trace wiggling along the compliance ceiling, and even occasionally falling off and rising back to the ceiling before entering LRS.

5. **Set failure** (Fig. 5(f)): The $I-V$ curve cannot enter LRS after the set procedure.
Figure 5: The electrical characteristics of the set-and-reset cycles can be classified into five categories: (a)(b) good set with SCLC, (c) good set without SCLC, (d) fair set, (e) poor set, and (f) set failure. The blue dashed curves are plotted against the programmed bias voltage provided by the voltage source, whereas the red solid curves are plotted against the measured bias voltage.
The Schottky-emission equation is shown as follows:

\[ I = aA^*T^2 \exp \left[ \frac{- (\phi_B - \sqrt{q^3V/4\pi\epsilon d_s})}{kT} \right], \]

where \( a \) is the effective cross section of the filament, \( A^* \) is the effective Richardson constant, \( q \) is the carrier charge, \( T \) is the temperature, \( \phi_B \) is the energy barrier height, \( d_s \) is the effective switching thickness, and \( \epsilon \) is the permittivity, which is \( \sim 25\epsilon_0 \) for HfO\(_2\). A fit to the LRS curve in Fig. 5(e) yields \( \phi_B = 0.36 \) eV and \( d_s = 2.4 \) nm, which reveals the characteristics of the device structure with the filament grown between the bottom TiN electrode and the positively-biased top Ti electrode to a point where it is only a tiny gap (~2.4 nm) away from completion of the connection. The value of \( \phi_B \) is about half of that of our previous similar HfO\(_x\) memristors,\(^{23}\) which may imply a larger amount of impurities or defects in the switching layer.

Shown in the inset of Fig. 5(a) is a log-scale blown-up view of the spot where the \( I-V \) slope changes due to SCLC, which is known to be mostly detected in memristors with \( \phi_B \lesssim 0.3 \) eV.\(^{27}\) The \( I-V \) characteristic is ohmic until \( V \) is swept to a more negative value of \(-0.48 \) V, where the device enters the trap-filling regime\(^{28-30}\) with the slope in the log scale prominently increased to \( > 2 \), until the \( I-V \) characteristic changes again to follow the Mott–Gurney law of SCLC\(^{31}\) starting at \( V = -0.52 \) V:

\[ I = \frac{9}{8} a\epsilon \mu \frac{V^2}{d_s^3}, \]

where \( \mu \) is the electron mobility, which is \( \sim 200 \) cm\(^2\)/Vs in HfO\(_2\).\(^{32,33}\) The \( V^2 \) law of SCLC only holds for a limited range of bias voltage. After \( V \) is swept to \(-0.64 \) V, the characteristic becomes \( I \propto V^x \) with \( 1 < x < 2 \), until the reset procedure starts. This may be interpreted with a negative field dependence of the mobility of the space charges due to positional and energetic disorder in the material.\(^{34,35}\) At lower electric fields, the most energetically favorable paths for percolative hopping transport will proceed via randomly oriented jumps.
However, with increasing electric field, charge carriers are forced to make less energetically favorable jumps in the direction of the field, leading to a reduced mobility.

It is generally believed that a larger $I_c$ leads to a more compact structure of the oxygen vacancies\textsuperscript{36} or a larger diameter\textsuperscript{37} of the conductive filament. Therefore, a large $I_c$ in our experiment such as 135 $\mu$A results in an $I$–$V$ curve with standard characteristics of a fairly strong filament, as shown in Fig. 5(a). For $I_c = 60$ $\mu$A, however, manifolds of set conditions and electrical characteristics of the cycles can be observed (see Table 1), despite it being the set $I_c$ with the highest yield of conductance quantization in the reset procedure. Figs. 5(c) and 5(d) both have $I_c = 60$ $\mu$A, and the key difference between them is the stability of $V_m$ in the set procedure. One may forecast conductance quantization in the later reset procedure only when a “wiggling”, unsteady $V_m$ is detected in the set procedure.

Some previous works have tried to determine the size of the conductive filaments in Ti/HfO$_2$/TiN memristors either through TEM material analyses\textsuperscript{38} or through theoretical simulations.\textsuperscript{21,39} From the electrical characteristics and the TEM images or simulation results provided in these works, a filament in the 10-nm thick HfO$_2$ layer of our device with a resistance of around 3 k$\Omega$ to 6 k$\Omega$ may be roughly estimated to be only $\lesssim$ 3 nm in diameter. This explains why it has been extremely difficult to observe a filament in cross-sectional TEM images of our devices. Electrical stresses on a narrow filament structure that lead to conductance evolution in the order of $G_0$, on the other hand, have also been studied in several simulation works.\textsuperscript{14,20,40,41} However, a precise prediction of the quantized conductance value as a function of the atomic evolution of the filament structure is not available yet, nor is there a concise conclusion on the numerical values of the stress voltage to optimize the chance of observing conductance quantization. More experimental and theoretical research are necessary to unveil the detailed mechanism of the conductance quantization, and our work presents a step forward toward understanding the filament evolution.

Although multiple growths of filaments or branches composed of oxygen vacancies are possible in the device, the conduction is believed to be contributed by a single dominant
filament because there is only one LRS in each $I-V$ cycle (i.e., multiple filaments would have been resulted from multiple set procedures in sequence in an $I-V$ cycle, exhibiting state switching between multiple LRSs). Once a filament is established, the current flows mostly through the connected filament, and further filament growth will be suppressed owing to reduced electric field.\textsuperscript{42} It has been found from the TEM images of SiO$_2$-based planar devices that, in the LRS, there exists only one completed filament accompanied with a few incomplete ones.\textsuperscript{43}

A good set without SCLC (Fig. 5(c)) may be regarded as an intermediate state between the state with SCLC (Figs. 5(a) and 5(b)) and the state with conductance quantization (Fig. 5(d)) in the sense of the resultant filament strength. For a filament robust enough to stand a higher negative voltage, the device can enter the SCLC-dominating regime until an abrupt drop of the current occurs upon the reset procedure when the filament is ruptured under a much higher voltage. A filament that exhibits a progressive reset, on the other hand, features a relatively unstable figure showing unsteady $V_m$ in the set procedure, possibly with the oxygen vacancies at the tip of the filament moving around among multiple metastable states to establish or dismiss an ohmic contact. This instability is revisited in the reset procedure starting around $V = -0.4$ V in a more distinct fashion, i.e., the conductance quantization, which again reveals nanoscale atomic-level movements. As $I_c$ is lowered to 40 $\mu$A, with examples shown in Figs. 5(e) and 5(f), 43% of the $I-V$ curves exhibit Schottky emissions or set failures. From the facts above, $I_c = 60$ $\mu$A is the critical compliance current in our experiment that is just large enough to build an ohmic filament, and yet simultaneously small enough to allow atomic-level behaviors to be unveiled in the memristor operation. Our experiment is the first of its kind to classify the different signatures of $I-V_m$ (the measured voltage) for a better understanding of the atomic-level dynamics in a memristor.

Electrochemical metallization memristors may behave differently from VCMs in the reset procedure in accordance with the filament resistance. For example, Celano et al.\textsuperscript{44} have found from Cu/Al$_2$O$_3$/TiN memristors that Cu filaments with larger diameters and lower LRS
resistance tend to exhibit progressive resets, whereas Cu filaments with smaller diameters and higher LRS resistance are inclined to undergo abrupt ruptures, which is opposite to our findings on the HfO$_x$-based devices. The different behaviors can be interpreted with the filament growth and dissolution dynamic scenario being governed by the ion or vacancy mobility and diffusivity, and the redox rate.\textsuperscript{45,46} The activation energies for diffusion of oxygen vacancies in HfO$_2$ ($\sim$0.7 eV for a mobile charged (2+) oxygen vacancy\textsuperscript{22} and $\sim$3 eV for a neutral one\textsuperscript{47}) are much higher than those of Cu ions in amorphous Al$_2$O$_3$ ($\sim$0.3 eV for mobile ones\textsuperscript{48} and $\sim$0.9 eV for less mobile ones\textsuperscript{49}). As a very narrow oxygen-deficient filament undergoes a reset procedure with extremely limited current and thus limited Joule power, the oxygen vacancies, which have significantly low diffusivity, may leave the filament one by one slowly and discretely, allowing us to observe the step-wise conductance. The tendency to exhibit progressive resets at lower $I_c$ and consequently with higher LRS resistance is typical of memristors based on the VCM mechanism.\textsuperscript{50,51}

It is not clear yet why set-and-reset cycles with the same $I_c$ (60 $\mu$A) can lead to different set conditions for the same memristor. Possible overshooting of the current is considered at the compliance point as the memristor is quickly switched from HRS to LRS. The $I$–$V$ curves of our device exhibit a fairly linear relation in LRS, as shown in Figs. 5(c) and 5(d). This ohmic behavior indicates that possible parasitic capacitance, and hence current overshotting, are quite limited in our device.\textsuperscript{52} However, because the conductance characteristics of the memristor are markedly affected by the dynamic behaviors in the nanoscale, possible small overshooting of the current even to a minimal extent may matter. Since it is difficult to directly detect the probable variations of this minimal overshooting, monitoring $V_{in}$ becomes the only practical and effective method to determine the set condition right away. The cause of the different resultant set conditions under the same $I_c$ may also involve the instant internal state of the memristor in the atomic scale being affected dynamically by the second-order state variables (the temperature decay for example) present in the structure.\textsuperscript{53} With these nanoscale uncertainties in the system, it seems that the most easily observable signal
that reveals the multiple metastable states of a point contact in the filament, and thus the potential to yield quantized conductance states in the reset procedure, is the wiggling $V_m$ at the set procedure. Monitoring $V_m$ therefore becomes the critical method to track the qualities of the device fabrication and measurements.

3.2 Measurements with the Pulse-Mode Reset Procedure

Distinguishing *fair sets* from the others allows us to achieve a high success rate of control of the conductance quantization of the memristor using a pulse-mode reset procedure. A typical example is demonstrated in Fig. 6(a). The reset process is preceded by a set procedure using $I_c = 60 \, \mu A$ that exhibits a fair-set condition (i.e., with wiggling $V_m$) as depicted in Fig. 5(d). Voltage pulses with fixed width of 0.1 second and fixed value of $-0.35 \, V$ are used to control the atom-by-atom evolution. The pulse width and amplitude are chosen from amongst multiple tests to achieve the optimal result, that is, to stimulate switching to the next conductance state with a minimal average number of pulses. The pulse value $-0.35 \, V$, which is very close to the onset voltage of the reset process observed in dc voltage sweeps with a fair set (Fig. 5(d)), is speculated to be a favorable value for our device to activate recombination between oxygen ions and vacancies through oxygen migration by providing a proper electric field and a local temperature enhancement due to Joule heating.\textsuperscript{21,54} After each pulse, the current is read at $-0.01 \, V$ for 5 seconds, from which the conductance of the point contact is computed and then presented in units of $G_0$. It can be seen that the conductance decreases stepwise from $9G_0$ to $0.5G_0$ in steps of $0.5G_0$ with great precision, with an average standard deviation of only $\sim 0.014G_0$ for the quantized plateaus. The width of each conductance plateau falls within 20 seconds, which corresponds to 1 to 4 voltage stimuli before stepping down to the next plateau.

Fig. 6(b) presents another example of the pulse-mode measurement of the same memristor after a fair set using the same $I_c$ (60 \, $\mu A$). This set of data is from a cycle taken after three successive cycles with fair sets using $I_c = 60 \, \mu A$. (The quantized conductance data of all
Figure 6: (a)(b) Two representative examples of controllable quantized conductance states at integer multiples of $0.5G_0$ using a pulse-mode reset procedure after a fair set with $I_c = 60 \mu A$. (a) is taken right after changing $I_c$ from 70 $\mu A$ to 60 $\mu A$. (b) is taken after three successive cycles with fair sets. (c) Average total number of exceptional steps, which is the sum of spontaneous steps with $|\Delta G| \leq G_0$ and stimulated steps with $|\Delta G| = G_0$, as a function of the order of successive fair-set cycles. Also displayed are the fastest and the slowest training sequences from the data.

In this 4th cycle, not every step in the reset procedure is $0.5G_0$ in height and stimulated by a voltage pulse. A few exceptions are found between $6G_0$ and $2G_0$, where some of the conductance drops have magnitudes of $1G_0$, and some occur spontaneously without a pulsed voltage stimulus. This leads to a faster switching from a high-conductance state to the lowest one. The occurrence probability of these exceptions roughly increases with the number of repetitions of the measurements under the same $I_c$ (60 $\mu A$), implying a possible training effect. This training effect can be removed by applying a higher $I_c$ (70 $\mu A$ for example) to the set procedure before returning to the original $I_c$ to regain well-controlled state switchings.
in steps of $0.5G_0$ without exceptions. The training effect may be seen from the statistics shown in Fig. 6(c), where the average number of exceptions (i.e., the number of spontaneous steps with $|\Delta G| = 0.5G_0$ or $G_0$, plus the number of stimulated steps with $|\Delta G| = G_0$) is plotted against the order of successive fair-set cycles, collected from 10 sequences in which no steps larger than $G_0$ are involved. (In other words, a very minor group of sequences interrupted by a reset procedure with steps larger than $G_0$ are not included in Fig. 6(c) for simplicity.) For example, the total number of this kind of exceptional steps is 4 for Fig. 6(b).

Also displayed in Fig. 6(c) are the fastest (dashed line) and the slowest (solid line) training sequences from the data. It is rare for the fair set to appear continuously for more than 5 cycles, except for a “slow learner” like the solid trace in Fig. 6(c), which has 7 successive fair sets. Some may hope for an ideal memristor with controllable quantized conduction that always generates a conductance decrease of $0.5G_0$ in response to each voltage stimulus, but no realization of such a memristor has been reported up to date. It is possible that the conductance is governed not only by the external stimuli but also by its instant internal state, known as the property of a second-order memristor. In fact, memristors with this kind of instability on intermediate conductance states are being proposed as candidate neuromorphic computing devices that can naturally emulate the temporal behaviors, including sequence learning, of biological synapses.\textsuperscript{55,56} More research is necessary to accommodate or even take advantage of the second-order behaviors of the memristors for constructing practical neuromorphic computing architectures.

Set conditions other than fair sets generally do not yield controllable quantized conductance states in the pulse-mode reset procedure. For example, most of the time a reset process preceded by a good set requires a larger stimulating voltage, but only to lead to an abrupt conductance drop that brings the device directly to HRS. In very few cases, a reset process preceded by a good set that enters LRS at a relatively small $V_m$ (similar to that in Fig. 5(c)) can exhibit a few quantized conductance plateaus, but is far away from accessing a complete set of integer multiples of $0.5G_0$. Therefore, to efficiently repeat the operation of
the quantum-level manipulation, a pulse-mode reset procedure is executed only when a fair set is detected. The ability of the nanoscale atomic structure of a filament to switch among multiple metastable states upon the set process, as implied by the wiggling $V_m$ during a fair set (Fig. 5(d)), may be a necessary feature for a memristor to permit excellent realization and modulability of the quantized conductance states. Future device fabrications and characterizations are encouraged to incorporate $V_m$ measurements to analyze the set condition. Memristors that guarantee fair sets under certain $I_c$’s should be favorable.

For comparison, Xue et al.\textsuperscript{57} have found from a Pt/HfO$_x$/ITO memristor that switching of the quantized conductance states needs to be stimulated by extremely long (20-second) pulses, and becomes even more insensitive to voltage stimuli at lower conductance, which they attributed to the lower current and thus a lower power available for modulating the filament. In contrast to their findings, our devices are more efficient in that they are sensitive to short voltage stimuli throughout the whole reset procedure. This indicates the high modulability of a very narrow filament even with a very low current, which points to the criticality of the current density and the local temperature enhancement based on heat transfer around the constriction (i.e., the narrowest point) of the filament during the reset procedure.\textsuperscript{21,54} On the other hand, there are other previous studies on conductance quantization of memristors that also demonstrate state switching upon short pulsed voltage stimuli, but with much lower precision of the quantized conductance values.\textsuperscript{14} As analytical differentiation of the $I$–$V_m$ characteristics (Fig. 5) is employed in our experiment during device selection and measurements, the precision and signal-to-noise ratios of the quantized conductance are significantly improved in our experiment compared to previous reports, and thereby brings the study of memristors closer to practical application in neuromorphic computing.
4 Conclusions

In summary, we report on controllable quantized conductance states of TiN/Ti/HfO$_x$/TiN memristors in a pulse-mode reset procedure with significantly improved precision. The high controllability and precision are realized through analytical diagnoses of the set conditions of the fabricated devices. The $I-V_m$ characteristics of the set procedure can be classified into good, fair, and poor conditions, and only those with fair sets (i.e., with a “wiggling”, unstable measured voltage $V_m$ at the compliance current) can permit quantized conductance states in the reset procedure. Controlled conductance decrease from $9G_0$ to $0.5G_0$ in steps of $0.5G_0$ is successfully observed in pulse-mode reset procedures that are preceded by a fair set with an optimal compliance current (60 $\mu$A). A training effect that leads to a faster state switching is found in the operation, which is regarded as a candidate mechanism for temporal sequence learning. Our experiment is the first of its kind to point out the importance of monitoring the measured bias voltage to track the qualities of the device fabrication and measurements for the research of conductance quantization of memristors. Our study unveils a full spectrum of the dynamic behaviors under different set conditions to provide an overview of the mechanisms of the conductive filament, from a strong ohmic structure with space-charge-limited current (SCLC), to that without SCLC, then to a relatively unstable configuration that supports quantized conduction as well as ohmic conduction, and then to a nano-gapped channel with Schottky emission. This allows a better understanding of the dynamics of the nanoscale atomic-level structures in the memristors, which should promote the progress of future design and fabrication of the memristors for neuromorphic computing and quantum information processing algorithm.

Associated Content

Supporting Information available: more examples for each set category; information pertaining to the forming procedure, SCLC statistics, and operation using a pulse-mode set
procedure; measurements of devices with different cell areas; temperature-dependent measurements down to 4.2 K; data of a complete training sequence.

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**References**

(1) Chua, L. Memristor-The missing circuit element. *IEEE Trans. Circuit Theory* **1971**, *18*, 507–519.

(2) Yang, J. J.; Strukov, D. B.; Stewart, D. R. Memristive devices for computing. *Nat. Nanotechnol.* **2013**, *8*, 13–24.

(3) Milo, V.; Malavena, G.; Monzio Compagno, C.; Ielmini, D. Memristive and CMOS Devices for Neuromorphic Computing. *Materials (Basel)*. **2020**, *13*, 166.

(4) Li, B.; Gu, P.; Shan, Y.; Wang, Y.; Chen, Y.; Yang, H. RRAM-Based Analog Approximate Computing. *IEEE Trans. Comput. Des. Integr. Circuits Syst.* **2015**, *34*, 1905–1917.

(5) Merced-Grafals, E. J.; Dávila, N.; Ge, N.; Williams, R. S.; Strachan, J. P. Repeatable, accurate, and high speed multi-level programming of memristor 1T1R arrays for power efficient analog computing applications. *Nanotechnology* **2016**, *27*, 365202.

(6) Sun, Z.; Ambrosi, E.; Bricalli, A.; Ielmini, D. Logic Computing with Stateful Neural Networks of Resistive Switches. *Adv. Mater.* **2018**, *30*, 1802554.
(7) Pickett, M. D.; Strukov, D. B.; Borghetti, J. L.; Yang, J. J.; Snider, G. S.; Stewart, D. R.; Williams, R. S. Switching dynamics in titanium dioxide memristive devices. *J. Appl. Phys.* **2009**, *106*, 074508.

(8) Menzel, S.; Waters, M.; Marchewka, A.; Böttger, U.; Dittmann, R.; Waser, R. Origin of the Ultra-nonlinear Switching Kinetics in Oxide-Based Resistive Switches. *Adv. Funct. Mater.* **2011**, *21*, 4487–4492.

(9) Strachan, J. P.; Torrezan, A. C.; Miao, F.; Pickett, M. D.; Yang, J. J.; Yi, W.; Medeiros-Ribeiro, G.; Williams, R. S. State Dynamics and Modeling of Tantalum Oxide Memristors. *IEEE Trans. Electron Devices* **2013**, *60*, 2194–2202.

(10) Lim, S.; Sung, C.; Kim, H.; Kim, T.; Song, J.; Kim, J.-J.; Hwang, H. Improved Synapse Device With MLC and Conductance Linearity Using Quantized Conduction for Neuromorphic Systems. *IEEE Electron Device Lett.* **2018**, *39*, 312–315.

(11) Chen, Q.; Han, T.; Tang, M.; Zhang, Z.; Zheng, X.; Liu, G. Improving the Recognition Accuracy of Memristive Neural Networks via Homogenized Analog Type Conductance Quantization. *Micromachines* **2020**, *11*, 427.

(12) Marković, D.; Grollier, J. Quantum neuromorphic computing. *Appl. Phys. Lett.* **2020**, *117*, 150501.

(13) Pfeiffer, P.; Egusquiza, I. L.; Di Ventra, M.; Sanz, M.; Solano, E. Quantum memristors. *Sci. Rep.* **2016**, *6*, 29507.

(14) Li, Y.; Long, S.; Liu, Y.; Hu, C.; Teng, J.; Liu, Q.; Lv, H.; Suñé, J.; Liu, M. Conductance Quantization in Resistive Random Access Memory. *Nanoscale Res. Lett.* **2015**, *10*, 420.

(15) Xue, W.; Gao, S.; Shang, J.; Yi, X.; Liu, G.; Li, R. Recent Advances of Quantum Conductance in Memristors. *Adv. Electron. Mater.* **2019**, *5*, 1800854.
(16) Ohno, T.; Hasegawa, T.; Tsuruoka, T.; Terabe, K.; Gimzewski, J. K.; Aono, M. Short-term plasticity and long-term potentiation mimicked in single inorganic synapses. Nat. Mater. 2011, 10, 591–595.

(17) Yi, W.; Savel’ev, S. E.; Medeiros-Ribeiro, G.; Miao, F.; Zhang, M.-X.; Yang, J. J.; Bratkovsky, A. M.; Williams, R. S. Quantized conductance coincides with state instability and excess noise in tantalum oxide memristors. Nat. Commun. 2016, 7, 11142.

(18) Xie, Z.; Gao, S.; Ye, X.; Yang, H.; Gong, G.; Lu, Y.; Ye, J.; Liu, G.; Li, R.-W. Magnetism modulation and conductance quantization in a gadolinium oxide memristor. Phys. Chem. Chem. Phys. 2020, 22, 26322–26329.

(19) Lv, H.; Xu, X.; Sun, P.; Liu, H.; Luo, Q.; Liu, Q.; Banerjee, W.; Sun, H.; Long, S.; Li, L.; Liu, M. Atomic View of Filament Growth in Electrochemical Memristive Elements. Sci. Rep. 2015, 5, 13311.

(20) Long, S.; Lian, X.; Cagli, C.; Cartoixà, X.; Rurali, R.; Miranda, E.; Jiménez, D.; Perniola, L.; Liu, M.; Suñé, J. Quantum-size effects in hafnium-oxide resistive switching. Appl. Phys. Lett. 2013, 102, 183505.

(21) Dirkmann, S.; Kaiser, J.; Wenger, C.; Mussenbrock, T. Filament Growth and Resistive Switching in Hafnium Oxide Memristive Devices. ACS Appl. Mater. Interfaces 2018, 10, 14857–14868.

(22) Capron, N.; Broqvist, P.; Pasquarello, A. Migration of oxygen vacancy in HfO$_2$ and across the HfO$_2$/SiO$_2$ interface: A first-principles investigation. Appl. Phys. Lett. 2007, 91, 192905.

(23) Syu, Y.-E.; Chang, T.-C.; Lou, J.-H.; Tsai, T.-M.; Chang, K.-C.; Tsai, M.-J.; Wang, Y.-L.; Liu, M.; Sze, S. M. Atomic-level quantized reaction of HfO$_2$ memristor. Appl. Phys. Lett. 2013, 102, 172903.
(24) Tappertzhofen, S.; Linn, E.; Menzel, S.; Kenyon, A. J.; Waser, R.; Valov, I. Modeling of Quantized Conductance Effects in Electrochemical Metallization Cells. *IEEE Trans. Nanotechnol.* 2015, 14, 505–512.

(25) Mehonic, A.; Vrajitoarea, A.; Cueff, S.; Hudziak, S.; Howe, H.; Labbé, C.; Rizk, R.; Pepper, M.; Kenyon, A. J. Quantum Conductance in Silicon Oxide Resistive Memory Devices. *Sci. Rep.* 2013, 3, 2708.

(26) Krishnan, K.; Muruganathan, M.; Tsuruoka, T.; Mizuta, H.; Aono, M. Highly Reproducible and Regulated Conductance Quantization in a Polymer-Based Atomic Switch. *Adv. Funct. Mater.* 2017, 27, 1605104.

(27) Malliaras, G. G.; Scott, J. C. Numerical simulations of the electrical characteristics and the efficiencies of single-layer organic light emitting diodes. *J. Appl. Phys.* 1999, 85, 7426–7432.

(28) Kao, K. C.; Hwang, W. *Electrical Transport in Solids*; Pergamon: New York, 1981.

(29) Lampert, M. A.; Mark, P. *Current Injection in Solids*; Academic: New York, 1970.

(30) Mark, P.; Helfrich, W. Space-Charge-Limited Currents in Organic Crystals. *J. Appl. Phys.* 1962, 33, 205–215.

(31) Mott, N. F.; Gurney, R. W. *Electronic Processes in Ionic Crystals*; Oxford University Press, 1940.

(32) Negara, M. A.; Cherkaoui, K.; Hurley, P. K.; Young, C. D.; Majhi, P.; Tsai, W.; Bauza, D.; Ghibaudo, G. Analysis of electron mobility in HfO$_2$/TiN gate metal-oxide-semiconductor field effect transistors: The influence of HfO2 thickness, temperature, and oxide charge. *J. Appl. Phys.* 2009, 105, 024510.

(33) Özben, E. D. *Carrier mobility in advanced channel materials using alternative gate dielectrics*; Forschungszentrum Jülich, 2010.
(34) Bässler, H. Charge Transport in Disordered Organic Photoconductors a Monte Carlo Simulation Study. *Phys. status solidi* 1993, 175, 15–56.

(35) Bhattarai, G.; Caruso, A. N.; Paquette, M. M. Steady-state space-charge-limited current analysis of mobility with negative electric field dependence. *J. Appl. Phys.* 2018, 124, 045701.

(36) Zahoor, F.; Azni Zulkifli, T. Z.; Khanday, F. A. Resistive Random Access Memory (RRAM): an Overview of Materials, Switching Mechanism, Performance, Multilevel Cell (mlc) Storage, Modeling, and Applications. *Nanoscale Res. Lett.* 2020, 15, 90.

(37) Yu, S. Resistive Random Access Memory (RRAM). *Synth. Lect. Emerg. Eng. Technol.* 2016, 2, 1–79.

(38) Privitera, S.; Bersuker, G.; Butcher, B.; Kalantarian, A.; Lombardo, S.; Bongiorno, C.; Geer, R.; Gilmer, D.; Kirsch, P. Microscopy study of the conductive filament in HfO2 resistive switching memory devices. *Microelectron. Eng.* 2013, 109, 75–78.

(39) Nardi, F.; Larentis, S.; Balatti, S.; Gilmer, D. C.; Ielmini, D. Resistive Switching by Voltage-Driven Ion Migration in Bipolar RRAM—Part I: Experimental Study. *IEEE Trans. Electron Devices* 2012, 59, 2461–2467.

(40) Li, Y.; Zhang, M.; Long, S.; Teng, J.; Liu, Q.; Lv, H.; Miranda, E.; Suné, J.; Liu, M. Investigation on the Conductive Filament Growth Dynamics in Resistive Switching Memory via a Universal Monte Carlo Simulator. *Sci. Rep.* 2017, 7, 11204.

(41) Zhong, X.; Rungger, I.; Zapol, P.; Heinonen, O. Oxygen-modulated quantum conductance for ultrathin HfO2-based memristive switching devices. *Phys. Rev. B* 2016, 94, 165160.

(42) Kwon, D.-H.; Kim, K. M.; Jang, J. H.; Jeon, J. M.; Lee, M. H.; Kim, G. H.; Li, X.-S.;
Park, G.-S.; Lee, B.; Han, S.; Kim, M.; Hwang, C. S. Atomic structure of conducting nanofilaments in TiO2 resistive switching memory. *Nat. Nanotechnol.* 2010, 5, 148–153.

(43) Yang, Y.; Gao, P.; Gaba, S.; Chang, T.; Pan, X.; Lu, W. Observation of conducting filament growth in nanoscale resistive memories. *Nat. Commun.* 2012, 3, 732.

(44) Celano, U.; Goux, L.; Belmonte, A.; Opsomer, K.; Degraeve, R.; Detavernier, C.; Jurczak, M.; Vandervorst, W. Understanding the Dual Nature of the Filament Dissolution in Conductive Bridging Devices. *J. Phys. Chem. Lett.* 2015, 6, 1919–1924.

(45) Yang, Y.; Lu, W. Nanoscale resistive switching devices: mechanisms and modeling. *Nanoscale* 2013, 5, 10076.

(46) Ielmini, D. Resistive switching memories based on metal oxides: mechanisms, reliability and scaling. *Semicond. Sci. Technol.* 2016, 31, 063002.

(47) Duncan, D.; Magyari-Kope, B.; Nishi, Y. Filament-Induced Anisotropic Oxygen Vacancy Diffusion and Charge Trapping Effects in Hafnium Oxide RRAM. *IEEE Electron Device Lett.* 2016, 37, 400–403.

(48) Pandey, S. C. Atomistic mechanisms of ReRAM cell operation and reliability. *Mater. Res. Express* 2018, 5, 014005.

(49) Sankaran, K.; Goux, L.; Clima, S.; Mees, M.; Kittl, J. A.; Jurczak, M.; Altimême, L.; Rignanese, G.-M.; Pourtois, G. Modeling of Copper Diffusion in Amorphous Aluminum Oxide in CBRAM Memory Stack. *ECS Trans.* 2012, 45, 317–330.

(50) Wouters, D. J.; Menzel, S.; Rupp, J. A. J.; Hennen, T.; Waser, R. On the universality of the I – V switching characteristics in non-volatile and volatile resistive switching oxides. *Faraday Discuss.* 2019, 213, 183–196.

(51) Volos, C.; Pham, V.-T. *Mem-elements for Neuromorphic Circuits with Artificial Intelligence Applications*; Academic Press, 2021; p. 392.
(52) Ambrogio, S.; Milo, V.; Wang, Z.; Balatti, S.; Ielmini, D. Analytical Modeling of Current Overshoot in Oxide-Based Resistive Switching Memory (RRAM). *IEEE Electron Device Lett.* 2016, 37, 1268–1271.

(53) Kim, S.; Du, C.; Sheridan, P.; Ma, W.; Choi, S.; Lu, W. D. Experimental Demonstration of a Second-Order Memristor and Its Ability to Biorealistically Implement Synaptic Plasticity. *Nano Lett.* 2015, 15, 2203–2211.

(54) Roldán, J. B.; González-Cordero, G.; Picos, R.; Miranda, E.; Palumbo, F.; Jiménez-Molinos, F.; Moreno, E.; Maldonado, D.; Baldomá, S. B.; Moner Al Chawa, M.; de Benito, C.; Stavrinides, S. G.; Suñé, J.; Chua, L. O. On the Thermal Models for Resistive Random Access Memory Circuit Simulation. *Nanomaterials* 2021, 11, 1261.

(55) Mikheev, V.; Chouprik, A.; Lebedinskii, Y.; Zarubin, S.; Matveyev, Y.; Kondratyuk, E.; Kozodaev, M. G.; Markeev, A. M.; Zenkevich, A.; Negrov, D. Ferroelectric Second-Order Memristor. *ACS Appl. Mater. Interfaces* 2019, 11, 32108–32114.

(56) Marrone, F.; Zoppo, G.; Corinto, F.; Gilli, M. Second Order Memristor Models for Neuromorphic Computing. 2019 IEEE 62nd Int. Midwest Symp. Circuits Syst. 2019; pp 315–318.

(57) Xue, W.; Li, Y.; Liu, G.; Wang, Z.; Xiao, W.; Jiang, K.; Zhong, Z.; Gao, S.; Ding, J.; Miao, X.; Xu, X.; Li, R. Controllable and Stable Quantized Conductance States in a Pt/HfO$_x$/ITO Memristor. *Adv. Electron. Mater.* 2020, 6, 1901055.
Supporting Information:

Dynamic Behaviors and Training Effects in TiN/Ti/HfO$_x$/TiN Nanolayered Memristors with Controllable Quantized Conductance States: Implications for Quantum and Neuromorphic Computing Devices

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All the $I$–$V$ figures in the Supporting Information show the device current plotted against the measured bias voltage ($V_m$).

S1 The Forming Procedure

The forming procedure for all the devices are performed in the dc voltage sweep mode with a compliance current $I_c$ ranging from 10 to 100 µA. The bias voltage for the forming procedure...
is programmed to be swept from 0 to 3.5 V and then back to 0 V at a rate of $\Delta V = \pm 2 \text{ mV}$ per 0.5 second for each data point. $I_c$ starts from 10 µA, and will be increased by 10 µA each time up to 100 µA only if the forming procedure is not successful under the present smaller $I_c$. Devices that cannot undergo a successful forming procedure with an $I_c \leq 100$ µA are considered defective.

Representative examples of a successful forming procedure are shown in Fig. S1. Most
devices can undergo a successful forming process with $I_c = 10 \, \mu A$, followed by a Schottky-emission-like LRS, and then a tremendous increase of the conductance starting around $-0.3$ V. The current keeps enhancing enormously and becomes comparable with that from the category “good set with SCLC” around $-0.7$ V. Under a higher negative voltage, the $I-V$ curve starts to experience some violent oscillations before it enters HRS in a reset procedure.

The tremendous increase in the conductance under negative voltage is also examined in the log scale, as plotted in Figs. S1(c) and S1(d) for Figs. S1(a) and S1(b), respectively. It can be seen that the $I-V$ curve shows a Schottky-emission behavior (both with $\phi_B \approx 0.36$ eV and $d_s \approx 1.9$ nm) at lower voltages, then a tremendous increase in $I$ with significant oscillations, and then an $I-V$ relation close to the $V^2$ law of SCLC under higher voltages. The oscillating but overall increasing current in the middle regime is suspected to be attributed to trap filling. It is presumed that a local trap-rich conducting region is formed in the HfO$_2$ layer after the forming process, and the new-born filament which initially exhibited a Schottky-emission behavior can be unsteady and susceptible when handling the trap-mediated SCLC for the first time, thereby leading to apparent oscillations.

The non-ohmic $I-V$ in the LRS right after the forming process does not indicate a device of poorer quality. In fact, in a study on HfO$_2$-based memristors by Milo et al., the memristor with the best quality (i.e., with the highest process yield, lowest device-to-device variability, lowest set and reset voltages, largest resistance ratio, and best endurance) happens to be an Al-doped HfO$_2$ device with a curved, non-ohmic $I-V$ in the LRS after the forming process. In our device, the SCLC-dominating high conduction through the newly-formed filament under higher negative voltages before the 1st reset has probably invoked some modulation of the filament configuration (which may have led to the oscillations in the trap-filling regime) into a stronger one, and thereby the filament remains after rupture help the growth of an ohmic filament in the following set procedures.

Regarding the 1st reset procedure after forming, there may be step-like features in those violent oscillations during the reset, but the noise levels of possible conductance plateaus
among them are greater than \( G_0 \), and thus their corresponding values in conductance quanta are unreliable. Attempts on observing conductance quantization using a pulsed-voltage mode during the 1st reset procedure were also not successful.

**S2 The Set Procedure**

This section provides more examples for each set category, and discussion on the space-charge limited current (SCLC). All the data are from the same device as depicted in the paper (cell area = 0.36 \( \mu \text{m}^2 \)).

**S2.1 Good Set**

![Figure S2: Representative I–V curves of good sets with SCLC.](image)

Fig. S2 shows more examples of the category “good set with SCLC”, and Fig. S3 for “good set without SCLC”. Fig. S4, on the other hand, provides the distributions of the reset voltages and the SCLC onset voltages in the good-set group, and the probability of observing the SCLC feature in an I–V curve when the I–V curve exhibits the respective reset voltage. It can be seen that both the resets and the SCLC onsets occur most often at voltages between −0.6 and −0.7 V, and in this reset-voltage interval the probability of not
Figure S3: Representative $I-V$ curves of good sets without SCLC.

Figure S4: Distributions of the reset voltages and the SCLC onset voltages, and the probability of observing or not observing the SCLC feature in an $I-V$ curve with the respective reset voltage.
observing SCLC also reaches a local maximum. This may imply that some of the resets are triggered by SCLC, especially for the filaments with less stable atomic configurations. As the SCLC-dominating regime kicks in between $-0.6$ and $-0.7$ V in most cases, it may trigger a reset process, which leads to a tendency for the filament to break at a voltage between $-0.6$ and $-0.7$ V, being unable to exhibit the SCLC feature in the $I-V$ curve. This results in a local maximum of the “Prob. w/o SCLC” line in Fig. S4. It is speculated that the trap-filling events or the abrupt involvement of SCLC in the conduction can affect filaments with less stable atomic configurations. More research is needed to fully understand the mechanism.

### S2.2 Fair Set

![Representative $I-V$ curves of fair sets. (a)–(e): $I_c = 60 \mu$A. (f) $I_c = 90 \mu$A (same data as Fig. 3c). (g) $I_c = 50 \mu$A (same data as Fig. 3b). (g) $I_c = 40 \mu$A.](image)

Figure S5 shows more examples of the fair-set category with various $I_c$. It can be seen from Table 1 that the set $I_c$ that can yield conductance quantization in the reset procedure falls...
between 40 and 90 µA. The current at which a reset process starts for all the measurements with conductance quantization also stays between 40 and 90 µA, making the $I-V$ curves exhibit a more symmetric image on the set and reset sides than the good-set curves.

### S2.3 Poor Set

Fig. S6 shows more examples of the poor-set category.

![Figure S6: Representative I–V curves of poor sets.](image)

### S3 Measurements of Devices with Different Cell Areas

We have fabricated dozens of devices of the same structure with the same or different cell areas, and all of them show similar behaviors in the measurements, in particular the tendency to exhibit fair sets at lower $I_c$, and the high yield rate of conductance quantization during the reset procedure when a fair set is detected. Tables S1 and S2 are two representative examples of the statistics of the electrical characteristics of devices with a cell area of 0.60 µm$^2$ and of 0.96 µm$^2$, respectively. The measurement for each device (including the device presented in the paper with the statistics summarized in Table 1) starts from the lowest $I_c$ (= 40 or 30 µA) to the highest (= 165 µA) with 15 cycles for each $I_c$, followed by another 15 cycles repeated for each $I_c$ starting from the highest $I_c$ this time to the lowest. The statistics
from the second 15 cycles have always looked very similar to the first 15, which is consistent with the hypothesis that the average diameter of the filament grown depends mostly on $I_c$. Therefore, we simply display the total statistics from the 30 cycles for each $I_c$ in the tables.

Although the optimal $I_c$ for conductance quantization may show a little device-to-device variability, the $I$–$V$ characteristics do not seem to have apparent dependence on the cell area.

Table S1: Statistics from a device with a cell area of 0.60 $\mu$m$^2$.

| $I_c$ (µA) | 165 | 150 | 135 | 120 | 105 | 90 | 80 | 70 | 60 | 50 | 40 | 30 |
|------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|
| a) Good set  | 30  | 30  | 30  | 30  | 30  | 24 | 24 | 15 | 7  | 5  | 4  | 1  |
| w/ SCLC     | 22  | 18  | 17  | 20  | 10  | 11 | 5  | 2  | 2  | 0  | 0  | 0  |
| b) Fair set  | 0   | 0   | 0   | 0   | 6   | 6  | 6  | 22 | 22 | 20 | 14 |
| w/ Quant.   | 0   | 0   | 0   | 0   | 5   | 5  | 5  | 17 | 19 | 18 | 8  |
| c) Poor set  | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 1  | 3  | 6  | 14 |
| d) Set failure | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 1  | 1  |

Table S2: Statistics from a device with a cell area of 0.96 $\mu$m$^2$.

| $I_c$ (µA) | 165 | 150 | 135 | 120 | 105 | 90 | 80 | 70 | 60 | 50 | 40 |
|------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|
| a) Good set  | 30  | 30  | 30  | 30  | 29  | 22 | 20 | 11 | 6  | 4  | 0  |
| w/ SCLC     | 20  | 20  | 21  | 17  | 17  | 15 | 8  | 3  | 3  | 1  | 0  |
| b) Fair set  | 0   | 0   | 0   | 0   | 1   | 8  | 9  | 18 | 20 | 17 | 16 |
| w/ Quant.   | 0   | 0   | 0   | 0   | 0   | 6  | 7  | 15 | 19 | 14 | 12 |
| c) Poor set  | 0   | 0   | 0   | 0   | 0   | 0  | 1  | 1  | 4  | 8  | 12 |
| d) Set failure | 0   | 0   | 0   | 0   | 0   | 0  | 0  | 0  | 1  | 4  | 4  |

S4 Temperature-Dependent Measurements

The resistance of the ohmic LRS of a filament always exhibits a decreasing trend when the ambient temperature decreases. This is a typical electronic transport behavior for a metal, in which phonon scattering is dominant. The temperature dependence of metallic resistance can be approximated as $R(T) = R_0[1 + \alpha(T - T_0)]$, where $R_0$ is the resistance at temperature $T_0$, and $\alpha$ is the temperature coefficient of resistance. An example of the LRS resistance as a function of the ambient temperature is shown in Fig. S7, which is measured from a filament
Figure S7: LRS resistance as a function of temperature. The black line shows the linear fit to the curve.

that has been set at a temperature of 4.2 K at $I_c = 135 \, \mu A$ with a good set. The resistance is read using a very small current of 10 nA with a lock-in technique to avoid excessive Joule heating at low temperature. By choosing $T_0$ as 300 K, $\alpha$ is further calculated to be $4.2 \times 10^{-4}$ K$^{-1}$. The temperature dependence of the filament resistance is small, as also found in other studies on conductive filaments in HfO$_2$-based devices.$^3$

The temperature dependence of the characteristics of the set-and-reset cycles is also studied. An example of the $I$–$V$ curve at 4.2 K with a fair set and quantized conductance during the reset procedure is displayed in Fig. S8. The electrical characteristics at different temperatures from 4.2 K to 360 K look similar to those at room temperature, but statistics from these measurements show that the average reset voltage in each set category increases slightly in magnitude as temperature decreases, and becomes 0.4–0.7 V larger in magnitude at 4.2 K than that at room temperature. The statistics of the set categories at 4.2 K, on the other hand, are listed in Table S3. It can be seen that the probability of observing fair sets with quantized conductance is substantially increased especially for larger $I_c$’s, and the optimal $I_c$ to observe conductance quantization is increased from 60 $\mu A$ at room temperature to 80 $\mu A$ at 4.2 K.

The temperature dependence of the device characteristics can be interpreted with the following mechanisms. First, the mobility of oxygen vacancies is dependent on temperature.$^4$
Figure S8: (a) An $I$–$V$ example at 4.2 K, with its quantized conductance during the reset procedure expressed in terms of $G_0 (= 2e^2/h)$ in Fig. (b). The set $I_c$ is 80 µA. This plot features a wiggling set $V_m$, and an ohmic LRS with a resistance of 6.1 kΩ. It falls into the “fair set” category.

Table S3: Statistics about the set-and-reset cycles of the device (cell area = 0.36 µm$^2$, same device as that presented in the paper) at 4.2 K.

| $I_c$ (µA) | 165 | 150 | 135 | 120 | 105 | 90  | 80  | 70  | 60  | 50  | 40  |
|------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| a) Good set | 15  | 13  | 13  | 14  | 12  | 10  | 5   | 3   | 0   | 0   | 0   |
| w/ SCLC    | 9   | 8   | 7   | 7   | 5   | 5   | 2   | 0   | 0   | 0   | 0   |
| b) Fair set | 15  | 17  | 17  | 16  | 18  | 19  | 24  | 20  | 17  | 12  | 5   |
| w/ Quant. | 13  | 14  | 15  | 16  | 16  | 19  | 23  | 18  | 16  | 10  | 3   |
| c) Poor set | 0   | 0   | 0   | 0   | 0   | 1   | 1   | 6   | 10  | 12  | 17  |
| d) Set failure | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | 3   | 6   | 8   |

Lower mobilities at lower temperatures may explain the shift of the optimal $I_c$ from 60 µA to 80 µA, as the filament growth and dissolution dynamics is highly dependent on the ion or vacancy mobility.\(^5\) According to our experimental results, it is also speculated that a lower mobility and diffusivity at lower temperature is favorable for development of multiple metastable states of a filament, leading to the increased probability of observing fair sets (i.e., wiggling $V_m$) especially for larger $I_c$’s. The second key mechanism is that Joule heating can be better dispersed at lower temperatures,\(^6\) especially at a temperature as low as 4.2 K. This, together with the lower mobility of oxygen vacancies, may explain the higher reset voltage and the higher yield of progressive resets (instead of abrupt ruptures) with quantized conductance at 4.2 K than at room temperature. A very low ambient temperature is therefore
Figure S9: A representative example at 4.2 K of controllable quantized conductance states at integer multiples of $0.5G_0$ using a pulse-mode reset procedure after a fair set with $I_c = 80$ μA.

The device is also operated with the pulse-mode reset procedure at 4.2 K, with a representative result shown in Fig. S9, which looks very similar to the result at room temperature (Fig. 6(a)). To limit the number of voltage stimuli within 4 for each conductance plateau, voltage pulses with fixed width of 0.1 second and fixed value of $-0.41$ V are found optimal and thereby used at 4.2 K. It has a larger magnitude than the voltage stimuli used at room temperature (i.e., $-0.35$ V). This is consistent with the higher reset voltages observed at lower temperature in dc voltage sweep mode. The signal-to-noise ratio shows very little dependence on temperature. The average standard deviation is $\sim 0.012G_0$ for the quantized conductance plateaus at 4.2 K, which is close to that at room temperature. This confirms the picture of local heating by recurrent pulsed voltage stimuli as the main source of noise during a reset procedure, as the filament is being ruptured atomically under Joule heating that results in a much higher local temperature than room temperature.

S5 The Training Sequence

The complete sequence of the training effect shown in Figs. 6a and 6b is displayed in Fig. S10.
Figure S10: A complete sequence of the training effect using the pulse-mode reset procedure.
S6  Operation Using a Pulse-Mode Set Procedure

HfO$_2$-based devices can also undergo a set procedure using a pulsed-voltage mode to form an ohmic conductive filament.\textsuperscript{9–14} Although being capable of yielding progressive conductance decrease in the reset procedure, memristors with high-$\kappa$ insulating layers like HfO$_2$ tend to undergo an abrupt set (under voltage stresses in either a dc sweep mode or a pulse mode) owing to the local field enhancement factor.\textsuperscript{15,16} Therefore, it is not easy to find quantized conductance in the set procedure. Some have reported observation of conductance quantization in the set procedure, but the number of quantization plateaus is limited to only one during each set procedure, and the set process is still abrupt in nature.\textsuperscript{17} We can successfully perform a set procedure on our device either with a dc sweep mode or with a pulse mode (the voltage required for a successful set is usually $\sim$0.5 V higher in a 0.1-sec pulse mode than in a dc sweep mode), but we have not observed any conductance quantization in the set procedure. For our devices that are in a condition with potential to yield quantized conductance during the reset process, the set procedure would exhibit a wiggling $V_m$ (which implies multiple metastable states) instead of conductance plateaus, as stated in the paper.

We have also tried to find quantized conductance on the reset side after a pulse-mode set procedure, but the success rate is very low ($\lesssim$15% using optimal $I_c$). Most showed an abrupt reset, and a few showed a gradual reset but with noise-like fluctuations that do not correspond to (half-)integer multiples of $G_0$ (i.e., similar to the reset behavior in the poor-set category). We suspect that a short but $\sim$0.5 V-higher voltage stress applied during a pulse-mode set procedure is not a favorable condition for developing multiple metastable states of the atomic configuration of a filament, which is known to be a requirement for yielding quantized conductance in the reset procedure for our devices.
References

(1) Voronkovskii, V. A.; Aliev, V. S.; Gerasimova, A. K.; Islamov, D. R. Conduction mechanisms of TaN/HfO$_x$/Ni memristors. Mater. Res. Express 2019, 6, 076411.

(2) Milo, V.; Zambelli, C.; Olivo, P.; Pérez, E.; K. Mahadevaiah, M.; G. Ossorio, O.; Wenger, C.; Ielmini, D. Multilevel HfO$_2$-based RRAM devices for low-power neuromorphic networks. APL Mater. 2019, 7, 081120.

(3) Walczyk, C.; Walczyk, D.; Schroeder, T.; Beretaud, T.; Sowinska, M.; Lukosius, M.; Fraschke, M.; Wolansky, D.; Tillack, B.; Miranda, E.; Wenger, C. Impact of Temperature on the Resistive Switching Behavior of Embedded HfO$_2$-Based RRAM Devices. IEEE Trans. Electron Devices 2011, 58, 3124–3131.

(4) Singh, J.; Raj, B. Temperature dependent analytical modeling and simulations of nanoscale memristor. Eng. Sci. Technol. an Int. J. 2018, 21, 862–868.

(5) Yang, Y.; Lu, W. Nanoscale resistive switching devices: mechanisms and modeling. Nanoscale 2013, 5, 10076.

(6) Zhang, X.; Xu, L.; Zhang, H.; Liu, J.; Tan, D.; Chen, L.; Ma, Z.; Li, W. Effect of Joule Heating on Resistive Switching Characteristic in AlOx Cells Made by Thermal Oxidation Formation. Nanoscale Res. Lett. 2020, 15, 11.

(7) Yi, W.; Savel’ev, S. E.; Medeiros-Ribeiro, G.; Miao, F.; Zhang, M.-X.; Yang, J. J.; Bratkovsky, A. M.; Williams, R. S. Quantized conductance coincides with state instability and excess noise in tantalum oxide memristors. Nat. Commun. 2016, 7, 11142.

(8) Dirkmann, S.; Kaiser, J.; Wenger, C.; Musseenbrock, T. Filament Growth and Resistive Switching in Hafnium Oxide Memristive Devices. ACS Appl. Mater. Interfaces 2018, 10, 14857–14868.
(9) Wang, G.; Long, S.; Yu, Z.; Zhang, M.; Li, Y.; Xu, D.; Lv, H.; Liu, Q.; Yan, X.; Wang, M.; Xu, X.; Liu, H.; Yang, B.; Liu, M. Impact of program/erase operation on the performances of oxide-based resistive switching memory. *Nanoscale Res. Lett.* 2015, 10, 39.

(10) Yuan, F.-Y.; Deng, N.; Shih, C.-C.; Tseng, Y.-T.; Chang, T.-C.; Chang, K.-C.; Wang, M.-H.; Chen, W.-C.; Zheng, H.-X.; Wu, H.; Qian, H.; Sze, S. M. Conduction Mechanism and Improved Endurance in HfO\textsubscript{2}-Based RRAM with Nitridation Treatment. *Nanoscale Res. Lett.* 2017, 12, 574.

(11) Lin, C.-Y.; Chen, P.-H.; Chang, T.-C.; Chang, K.-C.; Zhang, S.-D.; Tsai, T.-M.; Pan, C.-H.; Chen, M.-C.; Su, Y.-T.; Tseng, Y.-T.; Chang, Y.-F.; Chen, Y.-C.; Huang, H.-C.; Sze, S. M. Attaining resistive switching characteristics and selector properties by varying forming polarities in a single HfO\textsubscript{2}-based RRAM device with a vanadium electrode. *Nanoscale* 2017, 9, 8586–8590.

(12) Mahata, C.; Kang, M.; Kim, S. Multi-Level Analog Resistive Switching Characteristics in Tri-Layer HfO\textsubscript{2}/Al2O\textsubscript{3}/HfO\textsubscript{2} Based Memristor on ITO Electrode. *Nanomaterials* 2020, 10, 2069.

(13) Tang, L.; Maruyama, H.; Han, T.; Nino, J. C.; Chen, Y.; Zhang, D. Resistive switching in atomic layer deposited HfO\textsubscript{2}/ZrO\textsubscript{2} nanolayer stacks. *Appl. Surf. Sci.* 2020, 515, 146015.

(14) Zazpe, R.; Ungureanu, M.; Golmar, F.; Stoliar, P.; Llopis, R.; Casanova, F.; Pickup, D. F.; Rogero, C.; Hueso, L. E. Resistive switching dependence on atomic layer deposition parameters in HfO\textsubscript{2}-based memory devices. *J. Mater. Chem. C* 2014, 2, 3204–3211.

(15) Panda, D.; Sahu, P. P.; Tseng, T. Y. A Collective Study on Modeling and Simulation of Resistive Random Access Memory. *Nanoscale Res. Lett.* 2018, 13, 8.
(16) McPherson, J.; Kim, J.-Y.; Shanware, A.; Mogul, H. Thermochemical description of
dielectric breakdown in high dielectric constant materials. Appl. Phys. Lett. 2003, 82,
2121–2123.

(17) Ulhas, S. S. Defect Engineering in HfO$_2$/TiN based Resistive Random Access Memory
(RRAM) Devices by Reactive Molecular Beam Epitaxy. Doctoral dissertation, Techni-
cal University of Darmstadt, Darmstadt, Germany, 2018.