SDC-based Resource Constrained Scheduling for Quantum Control Architectures

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ABSTRACT
Instruction scheduling is a key transformation in backend compilers that take an untimed description of an algorithm and assigns time slots to the algorithm’s instructions so that they can be executed as efficiently as possible while taking into account the target processor limitations, such as the amount of computational units available. For example, for a superconducting quantum processor these restrictions include the amount of analogue instruments available to play the waveforms to drive the qubit rotations or on-chip connectivity between qubits. Current small-scale quantum processors contain only a few qubits; therefore, it is feasible to drive qubits individually albeit not scalable. Consequently, for NISQ and beyond NISQ devices, it is expected that classical instrument sharing to be designed in the future quantum control architectures where several qubits are connected to an instrument and multiplexing is used to activate only the qubits performing the same quantum operation at a time. Existing quantum scheduling algorithms either rely on ILP formulations, which do not scale well, or use heuristic based algorithms such as list scheduling which are not versatile enough to deal with quantum requirements such as scheduling with exact relative timing constraints between instructions, situation that might occur when decomposing complex instructions into native ones and requiring to keep a fixed timing between the primitive ones to guarantee correctness. In this paper, we propose a novel resource constrained scheduling algorithm that is based on the SDC formulation, which is the state-of-the-art algorithm used in the reconfigurable computing. We evaluate it against a list scheduler and describe the benefits of the proposed approach. We find that the SDC-based scheduling is not only able to find better schedules, with an improvement of 10% on average, but it is also more versatile being able to model the complex relative timing constraints required for quantum circuit resource constrained scheduling.

1. INTRODUCTION
Quantum technology promises to boost the computing capabilities available today by orders of magnitude, which will revolutionize key application domains and give birth to new ones that will drive the human evolution for decades to come. However, because of the novelty of the computing approach that completely differs from any existing classical computing technology, we require a holistic research and development agenda in which everything from the lowest physical level, the qubit, to the highest application level needs to be (re)invented. A key component in the quantum full stack is the (backend) compiler. The main objective of a compiler is to efficiently translate a quantum high-level algorithm into an optimal quantum circuit that can be executed correctly on a quantum chip. For example, quantum circuits, which are composed of a series of quantum operations called gates, require scheduling to ensure all the gates of the quantum algorithm and their dependencies are satisfied while making sure that the resource limitations of the target quantum chip are taken into consideration. Moreover, in the context of quantum compilation, where short decoherence times are an additional burden, the availability of a performant scheduling algorithm can be the difference between a correctly executing quantum algorithm and a completely useless circuit.

At the same time, the number of qubits available in current quantum processors is low (at the moment of publication the largest device is IBM Eagle with 127 qubits), which implies that qubits can be driven individually and independently of other qubits because in these early quantum computing chips the quantum control electronics are not shared. Nevertheless, this simplistic approach is not realistic for scalable quantum computing systems starting with several hundreds to thousands of qubits, such as the IBM System Two quantum architecture, that will require multiplexing qubit control wires. Consequently, developing resource constrained scheduling algorithms is key to the success of these future architectures. However, existing approaches for current quantum computing deal with the scheduling problem in a trivial manner by mostly ignoring architectural limitations and resort to scheduling the quantum algorithm in an as soon as possible (ASAP) style, where only the program dependencies are taken into consideration.

One of the few compiler frameworks for quantum computation that addresses the limitations mentioned above is OpenQL, which includes a backend list scheduling compiler pass for the Surface-17 superconducting quantum processor. However, the problem with using list scheduling in a quantum compiler backed is that it is not versatile enough to model quantum gate decomposition and satisfy the relative timings finer quantum operations should obey with respect to one another after decomposition, e.g., performing a flux operation while at the same time parking other qubits, or ensuring fixed timing that might be required for feedback control or error detection and correction. The alternative to use a fully specified integer linear programming (ILP) formulation would solve the above ver-
satellite problem, albeit not being scalable. Consequently, a scheduling algorithm that provides a balanced trade-off between versatility and scalability was proposed. This scheduling algorithm is based on a system of difference constraints (SDC) [8] formulation stemming from ILP and is the state-of-the-art in high-level synthesis compilers [9] used in classical reconfigurable computing. However, SDC scheduling with resource constraints in a quantum context is not optimal due to the way quantum resources are shared, i.e., one quantum instrument can perform multiple quantum gates of the same type at once similar to classical vector processing units.

In this paper, we propose a novel quantum resource constraint scheduling algorithm based on SDC (QSDC) to generate efficient quantum schedules when quantum resources are shared. Concretely, the novelties of this paper are:

- We develop a novel resource constraint scheduling algorithm based on the SDC formulation and integrate it into the OpenQL compiler framework.
- We provide a comprehensive analysis of the advantages of our proposed algorithm when compared with the current list scheduling algorithm available in OpenQL.

The paper is organized as follows. First, section 2 presents the necessary background, including SDC preliminaries and related works. Then, in section 3 we present the QSDC algorithm. Section 4 describes the experimental results. Finally, section 5 summarizes the paper and highlights future work.

2. BACKGROUND

In this section, we introduce first the underlying concepts of quantum computation, then we present the instruction scheduling problem based on the system of difference constraints formulation, and finally, we review the scheduling state-of-the-art for quantum compilers.

2.1 Quantum Computing and Resources

Quantum computing requires a radically novel approach to the developing of processors and compilers, the hardware and software building blocks of any computing system. The main reason for the requirement of new processor design techniques and novel compiler algorithms is due to the switch to implementing quantum mechanics operations rather than the classical approach of performing Boolean logic arithmetic. While processing units enabling Boolean logic operations can be implemented fully in the digital domain by mature EDA techniques using large-scale integrated circuits, quantum mechanics requires the integration of analogue instruments that drive the basic quantum computational unit, the qubit, by generating waveforms to instruct which quantum gate has to be performed on a qubit. Table 1 summarizes the differences between the classical and quantum basic computational concepts and processor micro-architecture functional units.

Table 1: Comparison of Classical vs. Quantum Computing

| Compute Concept      | Classical | Quantum                      |
|----------------------|-----------|-----------------------------|
| Basic Compute Element| bit       | qubit                       |
| Logic Type           | arith/boolean | quantum mechanics            |
| Logic Operations     | +, -, *, &, | X, H, CNOT                  |
| Micro Architecture   | only digital | digital & analogue          |
| enabled by an        | CU+ALU    | CU+AWG                      |

The major difference stems from the requirement to implement quantum mechanics that requires driving analogue devices, e.g., an Arbitrary Waveform Generator (AWG) to play different waveforms corresponding to particular quantum gates (e.g., an X gate, as opposed to an arithmetic operation performed by an Arithmetic-Logic Unig (ALU) in a classical processor) controlled by general-purpose Control Units (CUs) that keep track of which quantum gates have to be performed at a given time step according to the quantum algorithm. Consequently, due to the digital-analog domain crossing required in the design of a quantum processor micro-architectures, the sharing of AWGs is key to the success of developing scalable quantum computing systems. For example, Figure 1 shows the Surface-17 "schematic of the targeted realization of Surface-17 in a planar cQED architecture with vertical I/O. Every transmon (represented by a circle) has dedicated flux control line, microwave-drive line, and readout resonator. Dedicated bus resonators mediate interactions between nearest-neighbor data and ancilla qubits. Readout resonators are simultaneously interrogated using frequency-division multiplexing in diagonally-running feedlines [6]. In the current S-17 configuration, qubits colored the same are connected to the same microwave-drive line and controlled by the same AWG instrument. For example, qubits 8, 9, and 10 are driven by a single AWG.

In this work, we use this target processor with the instrument connections depicted in Figure 1. However, the work can be easily retargeted by modifying the instrument sec-
tion in the OpenQL’s platform configuration file, as shown in Listing 1. `qwgs` section describe the connections for the single-qubit rotation gates (instructions of ‘mw’ type) that are controlled by AWGs. Each qwg controls a private set of qubits, enumerated in the `connection_map`. A qwg can control multiple qubits at the same time, but only when they perform the same gate and started at the same time. There are ‘count’ qwgs. For each qwg it is described which set of qubits it controls as configured for the S17 quantum device. Additionally, single-qubit measurements (instructions of ‘readout’ type) are controlled by measurement units. Each one controls a private set of qubits. A measurement unit can control multiple qubits at the same time, but only when they start at the same time. There are ‘count’ measurement units and for each measurement unit it is described which set of qubits it controls. Sections concerning the available instructions and chip topology information related to the connectivity of the device is left out for space reason.

Listing 1: Excerpt of the Platform Configuration File used by the OpenQL Compiler. Instrument Counts and Connectivity Correspond to the S-17 Shown in Figure 1.

```
"resources":
{
"qubits":
{
"count": 17
},
"qwgs":
{
"count": 3,
"connection_map":
{
"0": [2, 3, 4, 14, 15, 16],
"1": [8, 9, 10],
"2": [1, 5, 6, 7, 11, 12, 13, 17]
}
},
"meas_units":
{
"count": 3,
"connection_map":
{
"0": [14, 17],
"1": [2, 5, 6, 8, 9, 11, 12, 15, 16],
"2": [1, 3, 4, 7, 10, 13]
}
}, ...
```

OpenQL [4] is quantum compiler framework developed by Qutech, depicted graphically in Figure 2. It is a modular and retargetable framework as it allows to easily add new compiler passes as well as generate code for different quantum devices and technologies by simply describing the chip architecture in a new platform configuration file [5], illustrated above. OpenQL currently supports ASAP and ALAP scheduling, and resource constrained list scheduling. Furthermore, quantum programs can be written either in C++ or using the python API. It can generate both simulatable CQASM code [10] for QX simulator [11] and quantum micro-code (CC-micro) for Qutech’s Central Controller [12].

2.2 SDC Preliminaries

Instruction scheduling is a central problem in compilers. Informally, the instruction scheduling problem can be formulated as finding the best (i.e., usually the one that runs the fastest) sequence of instructions that minimize the execution time of an algorithm given different constraints, such as the available resources existent in Instruction scheduling is a central problem in compilers. Informally, the instruction scheduling problem can be formulated as finding the best (i.e., usually the one that runs the fastest) sequence of instructions that minimize the execution time of an algorithm given different constraints, such as the available resources existent in the target processor. Formally, the scheduling problem can be defined as an assignment of execution slots to each instruction (i.e., the time when the instruction is active) so that all program and platform dependencies are taken into account. For example, using integer linear programming (ILP) the following constraint has to be imposed on the scheduling variables defined for each instruction so that a valid schedule is produced:

\[
\sum_{j=1}^{m} x_{ij} = 1
\]

where it is assumed an \( m \) clock-cycle schedule for each of the \( i \) instructions in the program. According to [13], equation (1) is called an appearance constraint and is needed to ensure one instruction will only be executed in exactly one cycle.

Several other constraints have to be formulated in a similar manner as in (1) to solve the scheduling problem. Although using this formal specification using a mathematical approach is optimal, giving the best Quality-of-Results (QoR), due to the difficulty of solving it for large problems (i.e., the scheduling problem under resource constraints is known to be NP-hard), alternative scheduling algorithms have been proposed that are based on heuristics. One well-known algorithm is list scheduling [14], which uses a ready list of instructions and sorts them in increasing order of some predefined priority to select the next node to be scheduled. By using this ready list of instructions, the algorithm reduces the search space that in turn increases the scalability of the algorithm with the risk of obtaining a local minima solution; therefore, degrading the QoR of the obtained schedule. Figure 3 highlights this trade-off between QoR and scalability.
As a compromise between the two orthogonal features, i.e., runtime vs. QoR, a more versatile scheduling heuristic has been proposed in [8] based on a system of integer difference constraints (SDC). This heuristic is rooted in ILP, however, due to the intelligent way of encoding the scheduling variables and instruction constraints, which are defined as a linear system of inequalities where the underlying matrix is totally unimodular, the scheduling formulation can be solved using a linear programming relaxation that generates optimal integer solutions in polynomial time. Therefore, SDC can find better schedules than list scheduling while being faster than the fully specified ILP problem. Furthermore, contrary to list scheduling, in the SDC formulation we can easily specify relative timing constraints, which are very important in quantum computing because it is often necessary to guarantee an exact latency distance between two operations that would avoid for example the situation where the qubits will decohere. Using the terminology in [8], equations (2) and (3) highlight the inequalities needed to specify an exact timing constraint between two operations $a$ and $b$:

$$sv_{beg}(a) - sv_{beg}(b) \leq -l_{ab} \quad (2)$$

$$sv_{beg}(b) - sv_{beg}(a) \leq l_{ab} \quad (3)$$

where $sv_{beg}$ is the first cycle scheduling variable associated with an instruction and $l_{ab}$ is the number of clock cycles between $a$ and $b$. It is worth noting that several other constraints can be specified using the SDC formalism, all of which can be found in [8].

2.3 Related Works

Several quantum compilation frameworks have been developed over the last decade and in this part we will highlight some of them focusing on the available scheduling algorithm and target platform supported as a differentiating factor from this work. One of the first compilers developed was the ScaffCC [15] compiler for the Scaffold programming language. Developed initially by the Princeton University, in collaboration with IBM T.J. Watson and University of Santa Barbara, the compiler was built using the LLVM compiler infrastructure [16] and offered several advanced compiler transformations, such as the RKQC, the reversible logic circuitry toolkit for quantum computation, and the Longest-Path-First-Schedule (LPFS) scheduling compiler pass. Furthermore, another important characteristic of ScaffCC is that it is able to generate OpenQASM v2.0 [17] and cQASM v1.0 [19] quantum assembly languages. However, ScaffCC can be considered only a front-end compiler because it does not support a target quantum processor, rather it defers this compilation process to a backend-compiler, available for example in IBM’s QisKit runtime [], that knows the resource limitation of that particular quantum device. Consequently, the LPFS scheduler in ScaffCC is just a variant of an As-Soon-As-Possible (ASAP) scheduler that does not consider any resource constraints.

Qiskit [18] is another compilation framework developed by IBM. The software development kit is written in python for fast prototyping and uses a list scheduler for the different backends it supports. However, due to the limited amount of qubits available in the early quantum devices, i.e., up to 127 qubits available in the IBM Eagle that was based on the System One architecture, there was no multiplexing of the control wires of each qubits. Consequently, there was no need for advanced scheduling algorithms that optimize the circuit under resource sharing incurred by control wire stemming from multiplexing control wires as required for developing scalable quantum control architectures starting with IBM System Two quantum architecture [3]. Therefore, developing resource constrained scheduling algorithm is key to the success of these future architectures.

Other compilers, such as Qcor [19] and tket [20], are suffering the same drawbacks as the compilers described above, namely they are focusing on front-end compilation tasks and defer backend target compilation to quantum device providers and their backend runtime software, e.g., via IBM Quantum Experience. The main limitation of this approach is, as previously mentioned, that due to current small size of existing quantum devices the scheduling algorithms used were mostly based on basic ASAP style of scheduling. Contrary to this state-of-the-art in quantum circuit scheduling, we focus on the resource constraint scheduling problem for future quantum processors, such as those based on IBM’s System Two architecture, that will include sharing of quantum control electronics. We integrate our proposed QSDC scheduling algorithm into OpenQL compiler framework and target the Surface-17 chip that has a scalable architecture by sharing its control electronics as described in section 2.1.

3. QSDC SCHEDULING ALGORITHM

In this section, we will describe the QSDC scheduling algorithm at the hand of a simple example shown in Algorithm 1. The quantum circuit is written using OpenQL’s python API and is composed of four gates $X,Y,X,$ and $Z$ that operate on three qubits $2,3,$ and $4$. Recall that according to the S-17 instrument connections the qubits involved are driven by the same AWG with id 0 (see Figure 1 and Listing 1).

Algorithm 1 Running Example Quantum Circuit

```python
k.gate("x", [2])
k.gate("y", [3])
k.gate("x", [4])
k.gate("z", [2])
...
```

To compile any (quantum) program, a compiler will first cre-
ate a control and data dependency graph (CDFG) out of the program instructions that fulfill the dependencies of the program code, e.g., the abstract operations X and Z should happen exactly in the order they appear in the code. Please note that we call these operations abstract because at this point the compiler does not know that the quantum gates X and Z operating on qubit 2 are commutative. The (C)DFG for our example is shown in Figure 4(a). Alongside we show the SDC formulation when the chosen scheduling option is As-Soon-As-Possible (ASAP) without considering any resource constraints. When we schedule in this way, we see that a state transition graph (STG) is created in which all the independent operations are scheduled in parallel in the first state. That is, the first cycle 0 is assigned to the scheduling variables (s1, s2, and s3) belonging to the v1 to v4 graph nodes, while cycle 1 is assigned to s4 of the Z2's v4 node.

Before we continue with the formulation for the resource constrained scheduling problem, we recall that the scheduling problem with resource constraints is known to be an NP-hard problem. Therefore, to solve large problems, we rely on heuristics such as list scheduling or SDC, which also cannot model exactly the resource constraints. Consequently, the heuristic in SDC is to use a sorting algorithm to create a linear order of the CDFG nodes and then to use this order to add constraints based on the resources types and counts. In the best mode of operation known for SDC, as explained in [6], this includes sorting the nodes in ascending order using an As-Late-As-Possible (ALAP) primary key with the ASAP key as a tiebreaker when a couple of nodes have the same ALAP cycle. However, this is not optimal for quantum computing as illustrated in Figure 4(b). Using the X2, Y3, X4, Z2 linear order created by the aforementioned sorting heuristic and considering that an AWG can perform multiple operations in parallel only if they are the same type, a resource constraint between Y3 and X4 has to be imposed such that X4 starts at least 1 cycle after Y3 finishes because they both require the same AWG-0. Similarly, two other resource constraints have to be added between <v1 and v2> and <v3 and v4>, leading to a sub-optimal schedule in which all 4 nodes execute individually on the AWG requiring 4 cycles to run the whole quantum circuit.

However, if we consider that an AWG can control multiple qubits at the same time when they perform the same gate started at the same time, we observe that the X2 and X4 quantum gates could have been scheduled in parallel because stacking is possible in a quantum context. This observation led us to introduce a new heuristic that we call QSDC, which can be combined with the default resource constraint linear order sorting heuristic to generate a more optimized STG that takes into consideration the quantum resource features. QSDC enables stacking of quantum operations on the same quantum resource whenever possible, as shown in Figure 4(c).

Algorithm 2 Main Resource Constrained QSDC

Function: addResourceConstraints
Input: CDFGNodes[], PlatformResources[], QSDC
Goal: Assign rc_cycles to the CDFGNodes
Prerequisites: [asap][alap]_cycles are valid
Output: StateTransitionGraph[]
STG where rc_cycles are assigned to CDFGNodes

```plaintext
1: for resourceType : PlatformResources do
2: for resourceInstance : resourceType do
3:     qubitConnections[] = getConnectedQubitsOf(resourceInstance)
4:     reinstr = clear()
5:     for qubit : qubitConnections do
6:         for gateOP : CDFGNodes do
7:             if isQubitNeeded(gateOP, qubit) then
8:                 reinstr.push_back(gateOP)
9:                 break
10:         end if
11:     end for
12: end for
13: end for
14: if (reinstr.size() > 1) then
15:     addResourceConstraintsInstrument(16: reinstr, getInstrStacking(resourceInstance, QSDC))
17: end if
18: end for
```

The full QSDC RC scheduling algorithm is given in Algorithms 2 and 3. In the first algorithm, the overall main loop is shown to iterate through the resource types (e.g., AWG or readout units) of the platform and for each type it selects each instance (e.g., 0, 1, or 2 for an AWG type), shown...
We integrated these algorithms in the OpenQL compiler as a new scheduling pass. To solve the linear problem relaxation we used the lpsolve software package for solving linear, integer and mixed programs [21].

4. EXPERIMENTAL RESULTS

In this section, we evaluate the QSDC algorithm by compiling ten circuits from [22] for the superconducting processor Surface-17 that shares several control electronics among the 17 qubits for different types of quantum operations, limitations described in section [2.1] and highlighted in Figure [1] This sharing is translated into the resource constraints described in the platform configuration file used by the OpenQL compiler (see Listing [1]). We implemented the QSDC compiler into the release version 0.8.1 of OpenQL and compare it against the default existing resource constrained list scheduling algorithm. Furthermore, because the list scheduling pass was recently updated in OpenQL version 0.10.5, the latest version at the time of writing, we compare against as well. Please note that several bug fixes were done from version 0.8.1 to 0.10.5, which increased the overall latency of the compiled benchmarks. We compiled and run the benchmarks in an Ubuntu 20.04.5 LTS installation running on an eight-core eight-thread Intel(R) Core(TM) i7-9700 processor @ 3.00 GHz with 16 GB of memory.

4.1 Benchmarks

The ten benchmarks randomly selected from [22] are described in Table [2] which lists the initial number of qubits, gates, and CNOTs as specified in the original, not scheduled, circuit. To compile and schedule these circuits so that they can correctly execute on the S-17 quantum processor, the following compiler passes are selected, executed in the listed order: Clifford gate optimizer, Qmap, Clifford gate optimizer, and RCsched, which was configured both as a list scheduling and qdc for the experiments. For the Qmap pass the minextendrc option was set, while the platform configuration file did not include the gate_decomposition section. It is important to realize that each of these passes modify the original specification to optimize it as well as to solve connectivity limitations (i.e., by Qmap), which introduce additional gates to move the qubits into adjacent positions before the actual CNOTs gates can be executed. For example, the Qmap compiler pass increases the number of quantum operations and therefore the latency of the circuit. The QSDC as well as the resource constraint scheduler are invoked after the qmap has generated a topologically correct circuit.

| Benchmark     | Qubits | Gates | CNOTs | Latency |
|---------------|--------|-------|-------|---------|
| 4gt12_v1_89   | 6      | 228   | 100   | 448     |
| 4gt4_v0_72    | 6      | 258   | 113   | 478     |
| alu_bdd_288   | 7      | 84    | 38    | 169     |
| alu_v0_27     | 5      | 36    | 17    | 72      |
| clip_206      | 14     | 33827 | 14772 | 61786   |
| mini_alu_167  | 5      | 288   | 126   | 564     |
| mini_alu_305  | 10     | 173   | 77    | 242     |
| sqrt2_260     | 12     | 3009  | 1314  | 5740    |
| sym10_262     | 12     | 64283 | 28084 | 122564  |
| z4_268        | 11     | 3073  | 1343  | 5688    |
4.2 QSDC Evaluation

The compiler version used to obtain the results are 0.8.1 and 0.10.5 from the OpenQL github repository [23]. The results are shown in Table 3, where we can observe an increase in both number of qubits and gates used. The Latency column list the circuit execution time in cycles considering the real gate duration that are specified in the platform configuration file (20 ns per cycle). Finally, the two speed-up columns describe the speedup obtain of the QSDC algorithm against the default list scheduler when we compare to both the OpenQL versions tested.

Please note that the goal of the evaluation is focused on the sdc formulation in comparison with list scheduling. We did not intend to compare the efficiency of different implementations of list scheduling against other, since this is tightly connected to the platform and the resources. For example, in Scaffc there is a LPFS scheduler that deal with resources; however, this is not modeling a chip, rather a fictional one where all qubits are driven individually.

Table 3: Experimental Evaluation Results

| Benchmark   | Version | Qubits | Gates | CNOTs | Latency | Speedup |
|-------------|---------|--------|-------|-------|---------|---------|
| 4gt12_v1_89 | 0.10.5  | 9      | 311   | 152   | 1.361   | 1       |
| Qsdc-0.8.1  | 0.10.5  | 10     | 308   | 148   | 0.307   | 1       |
| 4gt4_w0_72  | 0.10.5  | 9      | 327   | 152   | 1.688   | 1       |
| Qsdc-0.8.1  | 0.10.5  | 10     | 340   | 159   | 1.012   | 1       |
| aluypad_288 | 0.10.5  | 9      | 115   | 69    | 0.853   | 1       |
| Qsdc-0.8.1  | 0.10.5  | 10     | 116   | 68    | 1.041   | 1       |
| alu0_v27    | 0.10.5  | 9      | 54    | 34    | 0.984   | 1       |
| Qsdc-0.8.1  | 0.10.5  | 10     | 55    | 34    | 1.147   | 1       |
| clip_206    | 0.10.5  | 15     | 45265 | 26210 | 169513  | 1       |
| Qsdc-0.8.1  | 0.10.5  | 16     | 45368 | 26341 | 110965  | 1.041   |
| min_4alu_167| 0.10.5  | 9      | 368   | 266   | 1284    | 1       |
| Qsdc-0.8.1  | 0.10.5  | 10     | 371   | 269   | 1202    | 1       |
| min_4alu_305| 0.10.5  | 10     | 234   | 138   | 790     | 1       |
| Qsdc-0.8.1  | 0.10.5  | 10     | 236   | 140   | 467     | 1       |
| sptk_260    | 0.10.5  | 10     | 243   | 147   | 486     | 0.961   |
| Qsdc-0.8.1  | 0.10.5  | 10     | 4599  | 2452  | 10299   | 1       |
| sym10_262   | 0.10.5  | 10     | 4699  | 2452  | 10711   | 1.011   |
| Qsdc-0.8.1  | 0.10.5  | 10     | 4699  | 2452  | 10711   | 1.011   |
| z4_268      | 0.10.5  | 10     | 4699  | 2452  | 10711   | 1.011   |

5. CONCLUSIONS AND FUTURE WORK

In this paper, we proposed a novel resource constrained scheduling algorithm that is based on the SDC formulation, which is the state-of-the-art algorithm used in the reconfigurable computing. Concretely, we have proposed a new selection heuristic to select the operation nodes in a quantum efficient way to account for the quantum context where quantum gates can be stacked on the same instrument when they are the same type. Furthermore, we have validated our work by integrating the QSDC algorithm into the OpenQL compiler framework and evaluated it using ten quantum algorithms. The experimental results showed the benefits of QSDC against the default OpenQL list scheduling, where an average of 10% speedup was observed. In future work, we will analyze and demonstrate the benefits of controlling relative timing constraints between quantum operations. However, before that can be showed, support for integrating flexible conditions between quantum gates have to be added to the data-dependecy graph in OpenQL.

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