Note on (active-)QRAM-style data access as a quantum circuit

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Abstract
We observe how an active (i.e., requiring $2^n$ parallel control operations) QRAM-like effect
\[
\sum_{y=0}^{N-1} |y\rangle \langle y| \otimes U^{\text{result, memory}}_y
\]
can be realized, as a quantum circuit of depth $O(n + \sqrt{m})$ (where $m$ is the size of the result register) plus the maximum over all $z$ of the circuit depths of controlled-$U^z$ operations.

Keywords: Gate-based quantum computing, quantum circuits, QRAM.

1 Introduction

All data processing, classical or quantum, requires that input data be made available in the computer. On a quantum computer, one way to make data available is through Quantum Random Access Memory (QRAM). QRAM is an abstract concept defined through the following interaction: If $y$ is a nonnegative $n$-bit integer representing the address of a memory location, $|\mu_y\rangle = \sum_{s \in \{0, 1\}^n} \alpha_s |s\rangle$ is a pure $m$-qubit quantum state “stored” at that “memory location”, and $r \in \{0, 1\}^m$ is a target $m$-bit string, then QRAM access has the following effect:

\[
|y\rangle|r\rangle|\mu_y\rangle \xrightarrow{\text{QRAM access}} |y\rangle \sum_{s \in \{0, 1\}^m} \alpha_s |s \oplus r\rangle |s\rangle,
\]

where $\oplus$ is the bit-wise XOR between bit-strings. This can be concisely written as

\[
\sum_{y=0}^{N-1} |y\rangle \langle y| \otimes CNOT^{\oplus m}_{\text{mem, result}}.
\]

QRAM is an implicit assumption that quantum algorithms such as the quantum linear system solver, HHL [4], and quantum machine learning algorithms derived from it make on the quantum computer on which they run. A physical realization of QRAM with $O(n^2)$ access time has been proposed [3, 2]; it is, however, unclear whether it is possible to build a so-called “passive” QRAM [1], i.e., one which doesn’t require $2^n$ parallel (classical) operations.

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controlling the quantum hardware. Using active QRAM will not give exponential speedup of, say, HHL over classical algorithms using $2^n$ processors.

This paper deals with a realization of (an obvious generalization of) active QRAM as a quantum circuit. Given, for each $z \in \{0, \ldots, 2^n - 1\}$, a “memory register” $\text{mem}_z$ of $k_z$ qubits and a unitary operation $U^z$ acting on two registers, a result register of $m$ qubits and the said “memory register”, we realize the unitary operation defined through

$$|y\rangle|\text{result}\rangle|\text{mem}_y\rangle \mapsto |y\rangle U^y(|\text{result}\rangle|\text{mem}_y\rangle),$$

(1)

whenever $y \in \{0, \ldots, 2^n - 1\}$ and $|\text{result}\rangle$ is in a computational basis state. This can be written concisely as an operation on the Hilbert space $H_{\text{address}}^{(n)} \otimes H_{\text{result}}^{(m)} \otimes \bigotimes_{z=0}^{N-1} H_{\text{mem}_z}^{(k_z)}$ (the superscripts give the number of qubits):

$$\sum_{y=0}^{N-1} |y\rangle\langle y| \otimes U^y$$

(2)

where it is understood, by abuse of notation, that $U^y$ acts on $H_{\text{result}} \otimes H_{\text{mem}_y}$, i.e., it is tensored with identities on $H_{\text{mem}_z}$, $z \neq y$.

The point of this note is the observation that at the expense of (a) $2^n$ parallel quantum operations being performed, and (b) $O(m2^n)$ ancillary qubits, (2) can be realized in with a quantum circuit of depth $n + \sqrt{m}$ plus the maximum (over all $z$) circuit depth of a controlled-$U^z$.

Taking $k_z = m$ for all $z$, and $U^z$ an $m$-fold tensor-product of CNOTs gives QRAM. Given a function $f : \{0, 1\}^n \rightarrow \{0, 1\}^m$, setting, $k_z = 0$ for all $z$, and

$$U^z := \bigotimes_{i=0}^{m} X^{f(z)_i}$$

(where $X$ stands for the Pauli $X$ operator and exponents are taken as usual) realizes the unitary $U_f$ with $U_f(|y\rangle|r\rangle) = |y\rangle|f(y) \oplus r\rangle$.

Hence, it can be said that (2) gives access to data which is partly “hard-coded” into the quantum circuit, and partly “stored” in qubits on the quantum processor. Another example are, e.g., controlled rotations $e^{-i\pi \mu X}$, where $\mu$ is an $m$-bit fixed point fraction stored in $m$ qubits (possibly in superposition).

Our proposed quantum circuit follows the structure of [3], i.e., it is arranged in a binary tree in such a way that operations on nodes with the same distance from the root can be run in parallel.

2 Description of the quantum circuit

Some notation

Let $N := 2^n$. We freely switch between interpreting nonnegative integers in $\{0, \ldots, N - 1\}$ as bit-strings of length $n$; as usual, bit-strings have the higher-significant bits to the left.

The empty bit-string is denoted by $\varepsilon$.

Overview

Suppose implementations (quantum circuits or “black boxes”) of the controlled unitaries

$$|0\rangle\langle 0| \otimes \text{Id} + |1\rangle\langle 1| \otimes U^z$$

(3)
for $z \in \{0, 1\}^n$ are given. Each $U^z$ acts on two quantum registers: a result register $\text{res}_z$ of size $m$, and a “memory” register $\text{mem}_z$ of size $k_z$; we allow $k_z = 0$. All these registers $\text{res}_z$, $\text{mem}_z$, $z \in \{0, 1\}^n$ are assumed disjoint.

As in [3], the whole process is organized in a binary tree. The nodes of the tree are labeled by bit-strings $x = x_{\ell-1} \cdots x_0$ of up to $n$ bits; we denote by $|x|$ length of the bit-string ($\ell$ in the case of $x = x_{\ell-1} \cdots x_0$). The root of the tree has the label $\varepsilon$, which is the empty bit-string; if $x$ labels a node and $|x| < n$, then $x0$ and $x1$ are the labels of the two (left and right) children of $x$; the leaves of the tree are the bit-strings of length $n$.

2.1 Down–Run–Up

As in [3], the quantum circuit operates in two phases: The “Down” phase, which propagates the address information from the root of the tree to the leaves; and the “Up” phase, which propagates the result of running $U^z$ back to the root. Between the two, we have a “Run” phase, which runs the controlled unitaries (3).

Uncomputation is needed in general, i.e., the complete quantum circuit will be: Down–Run–Up–do-stuff–(Down–Run–Up)$^\dagger$.

2.1.1 The “Down” phase

For each non-root node $x$ in the tree (i.e., each bit-string $x$ with $1 \leq |x| \leq n$), we use an ancilla qubit $\text{life}_x$. If the address register $\text{address}$ is in a computational basis state $|z\rangle$, then the “Down” phase will set $\text{life}_x$ to state $|1\rangle$, iff the node $x$ is on the path from the root to the leaf with label $z$.

For each non-leaf node $x$ in the tree (i.e., each bit-string $x$ with $1 \leq |x| < n$), we use an ancilla register $\text{adr}_x$ with $n - |x|$ qubits. If the address register $\text{address}$ is in a computational basis state $|z\rangle$ with $z = z_{n-1} \cdots z_0$, then the “Down” phase will set $\text{adr}_x$ to the state $|z_{n-|x|-1} \cdots z_0\rangle$, i.e., $\text{adr}_x$ is a copy of the $n - |x|$ least significant bits of the address register.

We also need to “hand down” the contents of the result register $\text{res}$. For that, for each non-root, non-leaf tree node $x$, we use an ancilla register $\text{res}_x$, of size $m$. This is in addition to the register $\text{res}_z$, for each leaf $z$, on which the $U^z$ operate, which we also consider as ancilla registers. Further, we denote $\text{res}_\varepsilon := \text{result}$.

The “Down” phase proceeds as follows. First of all, all ancilla qubits (including $\text{res}_z$, for $z$ of length $n$) are prepared in state $|0\rangle$, except for $\text{life}_\varepsilon$, which is prepared in state $|1\rangle$. 3
For each $k = 0, 2, 3, \ldots, n-1$ (sequentially) do the following:

1.) For each node with label $x$ of length $k$ in parallel:
   for each $j = 0, \ldots, n-k-1$ in parallel:
   Apply the following CNOT gate: Controlled on $adr_x[j]$ flip $adr_x[0][j]$

2.) For each node with label $x$ of length $k$ in parallel:
   for each $j = 0, \ldots, n-k-1$ in parallel:
   Apply the following CNOT gate: Controlled on $adr_x[j]$ flip $adr_x[1][j]$

3.) For each node with label $x$ of length $k$ in parallel:
   Apply the following Toffoli gate:
   Controlled on $adr_x[n-k-1]$ and on $life_x$, flip $life_x[0]$.

4.) For each node with label $x$ of length $k$ in parallel:
   Sandwiched between two applications of the Pauli-X gate on $adr_x[n-k-1]$, apply the following Toffoli gate:
   Controlled on $adr_x[n-k-1]$ and on $life_x$, flip $life_x[1]$.

5.) For each node with label $x$ of length $k$ in parallel:
   for each $i = 1, \ldots, m$ sequentially:
   Apply the following two Fredkin gates in parallel:
   Controlled on $life_x[0]$, swap $res_x[i]$ and $res_x[0][i]$; and
   Controlled on $life_x[1]$, swap $res_x[i]$ and $res_x[1][i]$.

This has the effect that the address bits required to determine the lifeness of each node is “handed down” in the tree to the leaves, which allows, on each level $k$ of the tree, to run in parallel the operations for all nodes on that level.

At the end of the “Down” phase, $life_z, z \in \{0,1\}^n$, indicates whether the execution of $U^z$ is requested.

2.1.2 Resource analysis

The $life$-qubits alone already require $2N$ qubits. A short calculation shows that the number of $adr$-qubits is

$$\sum_{k=0}^{n-1} (n-k-1)2^k = (1 + o(1)) N$$

The number of $res$-qubits is, of course, $(1 - o(1))2mN$. In total, the number of ancilla qubits is $(1 + o(1))(2m + 3)N$.

Owing to the parallelism, the circuit depth is $O(n + m)$. The circuit width (maximum number of parallel operations) is $2mn$.

Remark 1. At the expense of $\sqrt{m}$ additional ancilla qubits, the circuit depth can be reduced to $O(\sqrt{m} + n)$. Indeed, replace the sequential loop in step 5.) by the following. In every step $i = 1, \ldots, \sqrt{m}$, do this in parallel: (a) make a CNOT-copy of the control-ancilla, and (b) perform $s - 1$ controlled operations controlled on the copies of the ancilla qubit created in the earlier steps. Finally, uncompute the ancillas.

2.1.3 The “Run” phase

After the completion of the “Down” phase, we execute the controlled unitaries (3).

For each $z \in \{0,1\}^n$ in parallel:

```
life_z
```

```
res_z
```

```
mem_z
```

```
U^z
```

```
r^m
```

```
k^z
```
Recall that \( k_z \) can be zero.

### 2.1.4 The “Up” phase

The “Up” phase moves the result from the leaves up to the root. As a unitary operator, it is, the adjoint operation of the “Down” phase. We repeat it here for clarity.

For each \( k = n - 1, n - 2, \ldots, 0 \) (sequentially) do the following:

1.) For each node with label \( x \) of length \( k \) in parallel:
   for each \( i = 1, \ldots, m \) in parallel:
   Apply the following two Fredkin gates in parallel:
   Controlled on \( \text{life}_x0 \), swap \( \text{res}_x[i] \) and \( \text{res}_x0[i] \); and
   Controlled on \( \text{life}_x1 \), swap \( \text{res}_x[i] \) and \( \text{res}_x1[i] \).

2.) For each node with label \( x \) of length \( k \) in parallel:
   Sandwitched between two applications of the Pauli-X gate on \( \text{adr}_x[n - k - 1] \),
   apply the following Toffoli gate:
   Controlled on \( \text{adr}_x[n - k - 1] \) and on \( \text{life}_x \), flip \( \text{life}_x1 \).

3.) For each node with label \( x \) of length \( k \) in parallel:
   Apply the following Toffoli gate:
   Controlled on \( \text{adr}_x[n - k - 1] \) and on \( \text{life}_x \), flip \( \text{life}_x0 \).

4.) For each node with label \( x \) of length \( k \) in parallel:
   for each \( j = 0, \ldots, n - k - 1 \) in parallel:
   Apply the following CNOT gate: Controlled on \( \text{adr}_x[j] \) flip \( \text{adr}_x1[j] \)

5.) For each node with label \( x \) of length \( k \) in parallel:
   for each \( j = 0, \ldots, n - k - 1 \) in parallel:
   Apply the following CNOT gate: Controlled on \( \text{adr}_x[j] \) flip \( \text{adr}_x0[j] \)

### 2.2 The effect

It should be apparent from the construction that the circuit does what it is supposed to do:

**Proposition 2.** If the address register is in a computational basis state \(| address \rangle = | y \rangle\), for \( y \in \{0, 1\}^n \), then the unitary transformation has the following effect:

\[
| address \rangle | \text{result}, \text{mem} \rangle | 0 \rangle \cdots | 0 \rangle \xrightarrow{\text{ancillas}} | address \rangle (U^y \otimes \mathbf{1})(| \text{result}, \text{mem} \rangle | 0 \rangle \cdots | 0 \rangle ) ,
\]

where the effect of \((U^y \otimes \mathbf{1})\) is \( U^y \) on \text{result} and \text{mem}_y \text{ registers}, and identity on all \text{mem}_z \text{ with } z \neq y.

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