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Development of a Depleted Monolithic CMOS Sensor in a 150 nm CMOS Technology for the ATLAS Inner Tracker Upgrade

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Abstract: The recent R & D focus on CMOS sensors with charge collection in a depleted zone has opened new perspectives for CMOS sensors as fast and radiation hard pixel devices. These sensors, labelled as depleted CMOS sensors (DMAPS), have already shown promising performance as feasible candidates for the ATLAS Inner Tracker (ITk) upgrade, possibly replacing the current passive sensors. A further step to exploit the potential of DMAPS is to investigate the suitability of equipping the outer layers of the ATLAS ITk upgrade with fully monolithic CMOS sensors. This paper presents the development of a depleted monolithic CMOS pixel sensor designed in the LFoundry 150 nm CMOS technology, with the focus on design details and simulation results.

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1 Introduction

Standard CMOS pixel sensors, integrating the sensing volume and the readout electronics on the same substrate, have proven to be high precision tracking and vertexing devices in high energy particle physics experiments, thanks to their fine granularity and low material. In addition, the use of commercial technologies makes them very suitable for covering large area in trackers due to their relative low cost. However, existing CMOS detectors in operation [1], or under construction [2], still rely in part or even substantially on diffusion for charge collection, which in turn leads to limited speed and radiation hardness, and therefore are not suitable for the extreme rate and radiation environment found in ATLAS. A recent trend of exploiting the high-voltage/high-resistivity add-ons of CMOS technologies to increase the depletion of the sensing volume has enabled fast charge collection by drift in CMOS sensors [3–5]. This relatively new sensor family, labeled as depleted CMOS pixels or depleted monolithic active pixel sensors (DMAPS), is currently under study, targeting high performance and cost efficient CMOS detectors for the ATLAS Inner Tracker (ITk) upgrade in the High-Luminosity LHC (HL-LHC) era. Depleted CMOS pixels, that have survived the radiation levels approaching the harshest requirements of the ITk upgrade, have already been reported [6, 7].

So far, the reported depleted CMOS pixels are either passive sensors or active ones with only first stage(s) of front-end (FE) electronics integrated in the pixel. The data readout and processing rely on a readout chip, bump bonded or capacitively coupled via glue bonds to the sensor [8]. These sensors are attractive alternatives for the sensing layers of hybrid detectors, enabling the cost reduction and introducing added features, such as sub-pixel address encoding, in the diode array [6]. A more ambitious step to explore the potential of depleted CMOS pixels is to develop a
fully monolithic sensor with a fast readout architecture. Such a monolithic sensor may be suitable for
the outer layers of the ATLAS ITk upgrade, where the performance requirements are less stringent
in comparison to the inner layers while the cost consideration becomes important.

This work presents a depleted monolithic CMOS pixel sensor design in the LFoundry 150 nm
CMOS technology, namely LF-Monopix01. In section 2, a short overview of R & D on depleted
CMOS pixels in the LFoundry technology is given. Then, the design challenges of a monolithic
sensor are addressed in section 3. In section 4, the design details of LF-Monopix01 are described,
followed by the simulation results in section 5. The conclusions are given in section 6.

2 Overview of R & D on depleted CMOS pixels in the LFoundry 150 nm technology

2.1 Implementation concept

Figure 1. Schematic cross-section of a depleted CMOS pixel in the LFoundry 150 nm CMOS technology.
The charges created in the p-substrate are collected by a n-type collection electrode. Various capacitance
contributions to the sensing node are indicated by respective symbols. It is noted that the schematic is not in
scale and shows only the relative implantation depth of different wells. In reality, the dimensions of the well
structures in depth are negligible as compared to the sensing volume (p-substrate).

A simplified schematic cross-section of a typical depleted CMOS pixel cell developed in the
LFoundry 150 nm CMOS technology is shown in figure 1. The charges created in the sensing vol-
ume (p-substrate) are collected by the charge collection node formed by the n-type well structures
with different implantation depth, so that the in-pixel electronics is isolated from the p-substrate and
completely hosted inside the charge collection node. The PSUB layer is used to isolate the n-well
(NW), hosting the PMOS transistors, from the charge collection node, thus allowing for full CMOS
capability in the pixel. The depletion of the sensing volume is increased with the resistivity of
p-substrate and the reverse bias voltage. Therefore, a high resistivity (≈ 2 kΩ·cm) substrate is used.
The maximum bias voltage relies on the sensor geometry and guard ring design, and a value higher
than 100 V is generally expected. Wafer thinning and backside implantation are possible after the
CMOS processing, thus a fully depleted thin sensor, e.g. less than 100 µm, biased via backside can
be achieved, yielding a strong electric field and uniform charge collection inside the sensor.

2.2 Demonstrated capabilities

The capabilities of depleted CMOS pixels implemented in the LFoundry 150 nm technology were
verified by the measurement of a previous prototype [5, 9]. A depletion depth over 160 µm can
be achieved with a reverse bias voltage of 110 V, confirming the high resistivity of the substrate.
In-beam timing measurements show that the fraction of in-time (< 25 ns) hits is only 91% even with a high threshold over one third of the most probable signal value. This means the time walk of readout should be further improved. The chip sample after 50 Mrad of total ionizing dose (TID) can operate with affordable noise degradation. And a depletion depth over 50 \( \mu \text{m} \) was observed with chip sample irradiated up to \( 1 \times 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2} \) of neutron fluence. These results indicate that depleted CMOS pixels developed in the LFoundry 150 nm technology may satisfy the requirements of the outer layers of the ATLAS ITk upgrade, provided that the FE electronics is further optimized in terms of speed and digital readout. This has greatly encouraged the design of a monolithic sensor in the same technology.

3 Design challenges of depleted monolithic CMOS pixels

The main consequence of implementing the sensor concept described in section 2.1 is a non-negligible increase in the detector capacitance, which in turn degrades the noise performance and the speed of the FE electronics. The contributions of capacitance to the sensing node can be seen in figure 1. Apart from the backplane capacitance \( C_{\text{sub}} \) and inter-pixel capacitance \( C_{n} \), which also exist in a standard n-in-p planar sensor, depleted CMOS pixels have another major contribution from the capacitance \( C_{\text{pw}} \) between the collection well and the p-well hosted inside. Because the p-well sits in close vicinity to the collection well, the contribution of \( C_{\text{pw}} \) is not negligible. Its capacitance value depends strongly on the area of electronics hosted inside the charge collection node. As revealed by TCAD simulation, \( C_{\text{pw}} \) tends to become dominant for a monolithic sensor where complex in-pixel electronics is required. In the case of LF-Monopix01, the contribution from \( C_{\text{pw}} \) ranges from 200 fF to 300 fF. For comparison, a passive CMOS pixel, which has no electronics inside the collection node, has only a total capacitance of \( \sim 100 \text{ fF} \), assuming the same pixel pitch and fill factor.

Therefore, the monolithic design calls for FE electronics optimized for the large input capacitance up to 400 fF. Additionally, since the electronic substrate is directly coupled to the sensing node via \( C_{\text{pw}} \), a large \( C_{\text{pw}} \) may introduce serious cross-talk. Thus, low noise digital logic is mandatory for the in-pixel circuitry, and the pixel layout must be carefully designed to ensure good protection for the p-wells in the charge collection node against the noise injection from the digital circuitry.

4 Design of LF-Monopix01

The LF-Monopix01 is a fast readout monolithic CMOS sensor, and it employs the column drain architecture as used in [10, 11]. The following sections present the design details.

4.1 Pixel

The pixel size of LF-Monopix01 is \( 50 \times 250 \ \mu \text{m}^2 \). The block diagram as well as the layout of a typical pixel in LF-Monopix01 are depicted in figure 2.
Figure 2. (a) Block diagram and (b) layout of a pixel with integrated readout logic. The pixel pitch is $50 \times 250 \, \mu m^2$ and the shaded area in the layout represents the area of the charge collection node, where all the in-pixel electronics is hosted. (c) The timing diagram for the readout logic.

Two short pulses are generated, respectively, at the leading edge (LE) and trailing edge (TE) of the discriminator output. These two pulses strobe the 8-bit timing information into two RAM cells. The TE pulse also sets the HIT flag register, which inserts a Token that can propagate to the column end through a chain of OR logic. The output Token is received by a readout controller (not shown in figure 2(a)), which sends back the Freeze signal to the column. The Freeze signal makes sure that new hits will not disturb the readout process, while these later hits can still be recorded by a first latch. The readout controller then generates the Read signal, which is selected by a priority network so that only the topmost hit pixel has its internal ReadInt signal enabled. The ReadInt signal allows the hit information (8-bit LE timestamp, 8-bit TE timestamp and 8-bit pixel address) from the in-pixel memories to be driven to the column data bus for readout. Since the ReadInt signal also clears the hit flag register, the priority network ripples down to find the next hit pixel, if any, once the Read signal goes back to zero. This readout cycle continues by sending repetitively the Read pulse until this frozen column is “drained out”.

Preamplifier. There are two preamplifier designs in LF-Monopix01, and their schematics are given in figure 3(a). Both preamplifiers use the single-ended folded cascode topology, and their transistor parameters were optimized to cope with the expected large detector capacitance ($\sim 400 fF$) in LF-Monopix01. The major difference between the two amplifiers is that one uses an NMOS transistor as the input device, whereas the other uses two complementary input transistors to increase the transconductance for a given bias current, and thus is expected to have better speed and noise.
performance [12]. However, the bias of the CMOS input preamplifier relies on separate analog power (VDDAPRE in figure 3(a)) provided by a regulator at the periphery, and the sensitivity of the circuit performance to this power line needs to be verified in a large scale sensor.

**Discriminator.** There are also two discriminator designs in LF-Monopix01 (see figure 3(b)). The discriminator V1 has a typical two-stage open loop structure and it has been implemented in previous LF Foundry prototypes. The discriminator V2 is a self-biased differential amplifier, followed by a CMOS inverter as the output stage. The latter exploits the complementary character of CMOS input devices for high gain and fast operation [13]. Thus, the pixel with discriminator V2 is expected to have less time walk.

**Cross-talk minimization.** As mentioned in section 3, significant cross-talk may be introduced from the electronic layer to the sensing node via $C_{pw}$, mimicking signals. Therefore, the digital readout logic employs a full custom design to minimize the area, and accordingly the capacitance value of $C_{pw}$. In addition, the switching noise of some critical digital blocks was minimized. For instance, a current steering logic [14] is used for token propagation. Moreover, the readout of the memory cells adopts a source follower as the output stage, so that high current injection into the substrate of in-pixel electronics is avoided during the readout. In this prototype, another readout concept was implemented by moving the readout logic to the column end, forming a matrix of logic units. In this case, the drawbacks of complex in-pixel circuits are eliminated. However, the insensitive area is increased, and one-to-one connection from the sensor pixel to the corresponding logic unit is needed, which will complicate the layout design when scaling up the pixel array.

### 4.2 Chip architecture

The size of the LF-Monopix01 prototype is $\sim 10 \times 10$ mm$^2$. The chip layout is shown in figure 4. The bottom part of the prototype includes the circuits that are used for chip bias, configuration and monitoring. The main body contains an array of $129 \times 36$ pixels. In order to perform comparative studies, there are in total nine pixel designs, each of them occupying four pixel columns. Seven designs are pixels with in-pixel readout logic. They differ from each other by different circuit block designs (i.e. preamplifier and discriminator) and layout implementations. The other two designs are binary pixels with the readout logic located at the column end. These pixels have the same preamplifier and discriminator design, but different output stages are used to drive the
binary information to the column bus. On the top side, each pixel column interfaces with its own End-of-Column (EoC) circuitry. The EoC circuitry includes 24 sense amplifiers to receive and temporally store the 24-bit data from the column bus, a gray counter running at 40 MHz to provide the timing information to the column, and the EoC logic which performs the column level readout priority scan and data transmission. The data from the EoC circuitry is serialized on-chip and sent out by a LVDS driver with a bit rate of 160 Mbps. For design simplicity, the readout controller will be implemented off-chip by an FPGA.

5 Simulation results

The functionality and performance of LF-Monopix01 have been extensively simulated, and some selected results are presented in this section.

Gain and noise. Figure 5 shows the simulated gain and noise of the preamplifier, as a function of detector capacitance. The input signal charge is 4000 e\(^{-}\). The bias current is \(\sim 17.5 \mu A\) for the NMOS preamplifier. Thanks to the complementary input transistors, the CMOS preamplifier is expected to have better performance than the NMOS counterpart under the same bias current, and therefore has a lower design current of \(\sim 15 \mu A\). The estimated total detector capacitance, including \(C_{pw}\) in figure 1, is \(\sim 400 \text{ fF}\) for pixels with readout logic, and is \(\sim 300 \text{ fF}\) for binary pixels. As can be seen from figure 5, the CMOS amplifier has better performance, yielding a gain value above 19 \(\mu V/e^-\) and a noise value of \(\sim 125 e^-\) with 400 fF detector capacitance. It is noted that the gain for both amplifiers is linear up to 20 ke\(^{-}\), covering the expected signal range. The agreement between simulation and measurement of a previous prototype [5, 9] indicates a good prediction of real circuit performance by the simulation results shown above.

Time walk. Figure 6 shows the simulated waveforms of the discriminator output (“HIT”) and the LE pulse, with the input charge ranging from 1500 e\(^{-}\) to 80 ke\(^{-}\). The simulated pixel uses the NMOS preamplifier with the detector capacitance of 400 fF, and followed by the discriminator
Figure 5. Simulated (a) gain and (b) noise for the NMOS (dashed line) and CMOS (solid line) preamplifiers, as a function of detector capacitance. The estimated total detector capacitance is $\sim 400$ fF for the pixel with readout logic, and is $\sim 300$ fF for the binary pixel. The bias current is $\sim 17.5$ µA for the NMOS preamplifier, and is $\sim 15$ µA for the CMOS preamplifier.

V2. The threshold of the discriminator is adjusted to be 1500 e$^-$, meaning that only signal charge beyond this value will fire the discriminator and generate the LE pulse. The resulting LE pulse indicates the arrival of the hit. The simulated time walk in the worst case is $\sim 23$ ns, which is the time difference between the two LE pulses that are generated from the “small” signal (1500 e$^-$) and a very large signal (80 ke$^-$) respectively. Similar simulation was performed with pixel using discriminator V1, and the time walk has a larger value of $\sim 34$ ns.

Figure 6. Time walk simulation for a pixel with NMOS preamplifier and discriminator V2.

Column simulation. The biasing and power/ground lines are distributed column-wise in the layout of the pixel array. Thus, post-layout simulation of an entire pixel column was performed, in order to study the parasitic effects. The simulated column is composed of pixels with integrated readout logic. Figure 7(a) shows the response of the preamplifier in the hit pixel, together with the responses of two neighboring pixels. As can be seen from the zoomed-in view around the baseline level (see figure 7(b)), the perturbation in the two neighboring pixels, caused by the hit pixel, is only $\sim 240$ µV in peak-to-peak value. This is equivalent to a charge injection less than 15 e$^-$. Moreover, the digital activities in the pixel have negligible influence on the analog part during the hit readout.
Figure 7. (a) Simulated preamplifier outputs of the hit pixel (black) and two neighboring pixels (blue) in the column. (b) the zoomed-in view around the baseline.

Full chip simulation. The full chip including the extracted parasitics was simulated with a FastSpice tool to verify the chip functionality. The readout controller was realized by the Verilog-A model. The simulated waveforms, resulting from the signal injection into an arbitrary pixel, are shown in figure 8. The firing of the pixel can be observed on a common monitoring line (HIT_Monitor). TokenChip, Freeze and Read are the interfacing signals between the chip and the readout controller as described in section 4.1. DataOut is the serialized data, including the hit timing and address.

Figure 8. Post layout chip simulation.

6 Conclusions

Depleted CMOS pixels have shown their potential for the ATLAS ITk upgrade. One possible use case would be equipping the outer layers of the ITk upgrade with fast readout monolithic CMOS sensors. In this work, a depleted monolithic CMOS pixel sensor, named LF-Monopix01, was designed in the LFoundry 150 nm CMOS technology. The prototype is capable of fast readout by using a column drain architecture. The chip is foreseen to have similar radiation tolerance as a previous prototype, which has showed affordable performance loss after irradiation up to the levels expected for the outer layers of the ITk upgrade. As compared to previous prototypes, the FE electronics in LF-Monopix01 was optimized for a better timing performance, and a time walk
value of \(\sim 23\) ns was achieved in simulation. Negligible cross-talk was seen when simulating one extracted pixel column with SPICE-level accuracy. The functionality of the full chip, containing over two million transistors, was verified by post-layout simulation using a FastSpice tool. The design was submitted in August 2016, and the delivery on silicon is expected in Q1 of 2017.

References

[1] L. Greiner et al., *Experience from the construction and operation of the STAR PXL detector*, 2015 *JINST* **10** C04014.

[2] M. Mager, *ALPIDE, the Monolithic Active Pixel Sensor for the ALICE ITS upgrade*, *Nucl. Instrum. Meth. Phys. Res. A* **824** (2016) 434.

[3] I. Peric, *Active pixel sensors in high-voltage CMOS technologies for ATLAS*, 2012 *JINST* **7** C08002.

[4] T. Obermann et al., *Characterization of a Depleted Monolithic Active Pixel Sensor (DMAPS) prototype*, 2015 *JINST* **10** C03049.

[5] T. Hirono et al., *CMOS pixel sensors on high resistive substrate for high-rate, high-radiation environments*, *Nucl. Instrum. Meth. Phys. Res. A* **831** (2016) 94.

[6] J. Liu et al., *HV/HR-CMOS sensors for the ATLAS upgrade-concepts and test chip results*, 2015 *JINST* **10** C03033.

[7] B. Ristic, *Measurements on HV-CMOS active sensors after irradiation to HL-LHC fluences*, 2015 *JINST* **10** C04007.

[8] I. Peric, *Hybrid Pixel Particle-Detector Without Bump Interconnection*, *IEEE T. Nucl. Sci.* **56** (2009) 519.

[9] P. Rymaszewski et al., *Prototype Active Silicon Sensor in 150 nm HR-CMOS technology for ATLAS Inner Detector Upgrade*, 2016 *JINST* **11** C02045.

[10] E. Mandelli et al., *Digital column readout architecture for the ATLAS pixel 0.25 \(\mu\)m front end IC*, *IEEE T. Nucl. Sci.* **49** (2002) 1774.

[11] I. Peric et al., *The FEI3 readout chip for the ATLAS pixel detector*, *Nucl. Instrum. Meth. Phys. Res. A* **565** (2006) 178.

[12] Y. Degerli et al., *Pixel Architectures in HV/HR CMOS Process for ATLAS Inner Detector Upgrade*, in proceedings of *Topical Workshop on Electronics for Particle Physics*, Karlsruhe, Germany, 26–30 September 2016.

[13] M. Bazes, *Two novel fully complementary self-biased CMOS differential amplifiers*, *IEEE J. Solid-State Circuits* **26** (1991) 165.

[14] H-T. Ng and D.J. Allstot, *CMOS current steering logic for low-voltage mixed-signal integrated circuits*, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **5** (1997) 301.