Effect of interfacial conductivity on electrical characteristics of negative capacitance field effect transistors

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Abstract

In this article, an interfacial conductivity model for the surface potential and the drain current was proposed based on the metal-interface-ferroelectric-insulator-semiconductor (MIFIS) structure negative capacitance field effect transistor (NC-FET). The simulating results illustrate that the electrical conductivity (σ) of the interface layer between the electrode and ferroelectric thin film caused by lattice misfit plays an important role in the process of voltage amplifying and steep switching for the NC-FET. It is indicated that new device design rules should take into account this scenario.

With the development of Moore’s law, the feature size of semiconductor devices has been continuously reduced, which has increased the power density of integrated circuits and the operating temperature of chips while the reliability and performance have been greatly reduced [1]. Reducing the subthreshold swing of the transistor is an effective way to reduce the voltage and power consumption of the integrated circuit. As early as 2008, Salahuddin and Datta [2] proposed to use ferroelectric thin film to replace the insulating material in the traditional MOS transistor to form an MFS structure, and such transistor with a negative capacitance can decrease the subthreshold swing (SS) below the physical limitation (60 mV/dec), thus a device with low power consumption can be realized. The subthreshold swing is numerically equal to the gate-source voltage required to increase the subthreshold current by an order of magnitude. The smaller the value of the subthreshold swing is the stronger control of the gate-source voltage imposes on the subthreshold current in the channel [3]. Equation (1) is the expression of subthreshold swing.

\[ SS = \ln 10 \times \left( \frac{kT}{q} \right) \times (1 + \frac{C_s}{C_{ox}}) \]  

At room temperature, the value of \((kT/q)\ln10\) term is about 60 mV/decade, so how to make SS smaller than 60 mV/decade depends on the value of \((1 + C_s/C_{ox})\) term, where \(C_s\) is the capacitance of semiconductor silicon, while \(C_{ox}\) is the insulator capacitance. Since the theory of negative capacitance was proposed, many researchers have conducted a large number of theoretical and experimental studies [4–12]. In these studies, Hoffmann et al [7] proposed that defects, charge trapping, and electric field-induced structural changes need, in particular, to be investigated in greater detail in the NC-FET devices. Previous studies [13, 14] showed that the conductivity of the interface layer between the ferroelectric layer and the electrode caused by the failure of the lattice matching can be used as an intermediate parameter to link the lattice mismatch. Based on this idea, in this article, we propose a theoretical model to describe the influence of intermediate variable electrical conductivity on the electrical characteristics of the NC-FET, focusing on the voltage amplification factor and the subthreshold characteristics. It is expected that this study can provide some useful guidelines for the design of low power dissipation of the NC-FETs.

First, the electric displacement \(D\) formula in the MIFIS structure (as shown in figure 1(a)) can be given as follows
Where \( \varepsilon_0 \) is the vacuum permittivity, \( \varepsilon_i \) is the dielectric constant, \( E_i \) is the electric field, and \( P_i \) is the polarization. The subscripts \( f \) and \( i \) represent the ferroelectric layer and the interface layer between the electrode and the ferroelectric layer, respectively. Figure 1(b) is the equivalent capacitance divider of the MIFIS structure. 

The \( C_i' \) is the capacitance of the interfacial layer between the metal electrode and the ferroelectric. \( C_f \) stands for the capacitance of the ferroelectric layer. \( C_i \) is the capacitance of the insulator layer between the ferroelectric and the semiconductor. \( C_s \) stands for the semiconductor capacitance. Given the current continuity between the ferroelectric layer and the interface layer, the total current density satisfies the following equation

\[
J = \sigma_i E_i + \sigma_f E_f = \sigma_i E_i + D_f'
\]

Where \( J \) is the current density, \( \sigma_i \) and \( \sigma_f \) represent the conductivity of the interface layer and the ferroelectric layer, respectively. \( D \) represents \( \partial D/\partial t \). To avoid complicated calculations caused by time \( t \), an external triangular electric field is employed, and the value of \( \partial E/\partial t \) takes +1 or −1 when the electric field is increasing or decreasing [13]. According to the Landau-Khalatnikov (LK) theory, for a nonlinear ferroelectric capacitor, the relationship between the Gibb’s free energy \( U \) and ferroelectric polarization \( P \) can be expressed as [15–17]

\[
\rho(dP/dt) + \nabla U = 0
\]  

(4)

Where

\[ U = \alpha P^2 + \beta P^4 + \gamma P^6 - E_f \cdot P \]  

(5)

\( E_f \) is the electric field across the ferroelectric layer, and \( \alpha, \beta, \) and \( \gamma \) are called Landau parameters. For simplicity, the steady-state polarization was considered and \( dP/dt = 0 \) was assumed in equation (4). Combining equations (4) and (5), one can get the ferroelectric electric field.

\[
E_f = 2\alpha P + 4\beta P^3 + 6\gamma P^5
\]  

(6)

Equation (6) can be further expressed as.

\[
V_f = 2\alpha t_f P + 4\beta t_f P^3 + 6\gamma t_f P^5
\]  

(7)

According to the previous derivation reported by Salahuddin [2], equation (7) can be rewritted as

\[
V_f = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5
\]  

(8)

In equation (8), \( Q \) is the charge density of the combination of layers for the series capacitor. In this work, we assume Y-HfO\(_2\) as the ferroelectric material [18, 19], which is characterized by the Landau parameters \( \alpha = -1.23 \times 10^9 \text{ m F}^{-1}, \beta = 3.28 \times 10^{10} \text{ m}^2\text{ F}^{-1}\text{ C}^{-2}, \) and \( \gamma = 0 \) (as shown in figure 2). Ignoring the interface trap and space charge, the gate voltage applied to the MIFIS structure can be described as.
Where, $V_{\text{int}} = Q_{\text{int}}/(\varepsilon_0\varepsilon_{\text{int}})$, $V_{\text{ins}} = Q_{\text{ins}}/(\varepsilon_0\varepsilon_{\text{ins}})$ are the voltage drops of the interface.

Layer and the insulator layer, respectively. $\varphi_i$ stands for the silicon surface potential. $t_\text{fi}$, $t_\text{int}$ and $t_\text{ins}$ are the thickness of the ferroelectric layer, the interface layer, and the insulator layer, respectively. According to Sze’s model [20], $Q$ can be described as the function of $\varphi_i$.

$$Q(\varphi_i) = -\text{sign}(\varphi_i) \times \sqrt{2|\varepsilon_s|/(\lambda L_\text{D})}$$

$$\times (n_i^2/N_a^2 \cdot (e^{-\lambda \varphi_i} + \lambda \varphi_i - 1) + (e^{\lambda \varphi_i} - \lambda \varphi_i - 1))^{1/2}$$

IN equation (10), $L_\text{D} = (\varepsilon/qN_a\lambda)^{1/2}$ is the Debye length, $N_a$ the majority carrier concentration, and $n_i$ the intrinsic carrier concentration. $\lambda$ can be calculated by $\lambda = q/kT$, where $k$ is the Boltzmann constant, $T$ is the absolute temperature, and $q$ is the electric charge. According to Pao and Sah’s model [21], the current from source to drain in MIFIS-FET can be expressed as.

$$I = \frac{q\mu W}{L} \int_0^{V_{\text{DS}}} \int_{\phi_s}^{\phi_g} \frac{n_i^2}{N_a^2} e^{-\lambda(\phi_g - V)} N_\xi(\phi_s/V) d\phi_s d\phi_g$$

WHERE $\phi_\text{b} = (kT/q)\ln(N_a/n_i)$, while the electric field $\xi(\varphi_s, V)$ can be expressed as [21]

$$\xi(\varphi_s, V) = \sqrt{2N_a kT/\varepsilon_s}$$

$$\times (e^{\lambda \varphi_s} - \lambda \varphi_s - 1) + (n_i^2/N_a^2) e^{\lambda V} (e^{-\lambda \varphi_s} + \lambda \varphi_s e^{-\lambda V} - 1))^{1/2}$$

From the equations (2)–(12), one can get the curves of $V_{\text{gs}} - \varphi_i$ and $V_{\text{gs}} - I_{\text{DS}}$ of the MIFIS structure field effect transistor.

In the process of simulation, we assumed four different ferroelectric layer thicknesses $t_f = 4, 6, 8, 10$ nm, the thickness ratio is $\upsilon = t_{\text{int}}/t_f = 0.1$. The most obvious amplification effect of silicon surface potential can be observed at $t_f = 8$ nm when the interfacial conductivity is $0.035 \times 10^{-11} \, \Omega^{-1} \, \text{m}^{-1}$, which is shown in figure 3(a). As a general rule, big value of $t_f$ gives rise to hysteretic phenomenon. When $t_f$ reduces, the hysteresis disappears, and the voltage amplification effect can be obtained. The result is consistent with the previous results reported by Salahuddin [2] and Jiménez [22]. For better understanding the surface potential amplification effect, the voltage amplification factor defined as $G = \partial \varphi_s/\partial V$ which is present in figure 3(b). The maximal value of $G$ (bigger than 10) for the case of $t_f = 8$ nm appears when the gate voltage is about 0.52 V. For small values of $t_f$, the voltage amplification capability vanishes.

In order to prove the voltage amplification effect can be used as a way of obtaining steep subthreshold slope, we calculated the drain-source current versus the gate voltage ($I_{\text{DS}} - V_{\text{gs}}$) characteristic in figure 4. Where, the interfacial conductivity is assumed to be $0.035 \times 10^{-11} \, \Omega^{-1} \, \text{m}^{-1}$. Four different $I_{\text{DS}} - V_{\text{gs}}$ curves corresponding the ferroelectric film thickness of 2 nm, 4 nm, 6 nm, and 8 nm for the NC-FET were shown. From figure 4, one can see that the best subthreshold characteristic is the case of 8 nm, which means the maximal $G$ in the MIFIS structure automatically translates into $SS < 60 \text{ mVdec}^{-1}$ in the transfer characteristic. It is indicated that tuning $t_f$ properly is a key part of the NC-FET device design.

In actual devices, due to the mutual diffusion of atoms between the electrode material and the ferroelectric thin film, an interface layer will inevitably be formed under the action of heat and electricity, and the electron transport ability of this interface layer can be attributed to the electrical conductivity ($\sigma$). For the purpose of
investigating the effect of $\sigma$ on the electrical characteristic of the NC-FET, we firstly calculated the changes of silicon surface potential with the gate voltage under different values of interface electrical conductivity, which is present in figure 5(a). Where, $t_f = 8$ nm, and the value of $\sigma$ changes from $0.015 \times 10^{-11} \Omega^{-1} \text{m}^{-1}$ to $0.055 \times 10^{-11} \Omega^{-1} \text{m}^{-1}$. Interestingly, small-$\sigma$ values result in hysteretic behavior. When $\sigma$ increases, hysteresis disappears, and $G \approx 1$ can be obtained, the biggest value of $G$ appears at $\sigma = 0.035 \times 10^{-11} \Omega^{-1} \text{m}^{-1}$, which is shown in figure 5(b). Actually, this phenomenon can be understood like this. According to figures 3(b) and 5(b), for $t_f = 8$ nm, the biggest $G$ appears at $\sigma = 0.035 \times 10^{-11} \Omega^{-1} \text{m}^{-1}$. Smaller values of the interfacial conductivity mean that the behavior of the interfacial layer is closer to the ferroelectric layer, indicating the effective thickness of the ferroelectric is increased, so small values of $\sigma$ result in hysteretic behavior. While, bigger
values of the interfacial conductivity indicate the behavior of the interfacial layer is more different from the ferroelectric layer, which means there is a reduction of effective thickness of ferroelectric layer, thus bigger values of $\sigma$ enable the voltage amplification effect to vanish, which is similar to the thickness effect as shown in figure 3. It is worth noting that the effect of $\sigma$ is more obvious than that of $t_f$. The result illustrated that there is an optimal $\sigma$ which enables the voltage amplification factor to be maximal when $t_f = 8$ nm, which may provide useful guidelines for designing the NC-FETs as logic devices.

Figure 6 shows the effect of interface electrical conductivity on the transfer characteristics of the NC-FET, and three $I_D-V_g$ curves with typical electric conductivity values of $\sigma = 0.035 \times 10^{-11}$, $0.045 \times 10^{-11}$ and $0.055 \times 10^{-11}$ $\Omega^{-1} \text{m}^{-1}$ were computed. Where, the thickness of Y-HfO$_2$ ferroelectric thin film was assumed to be $t_f = 8$ nm. From figure 6, for the case of $\sigma = 0.035 \times 10^{-11}$ $\Omega^{-1} \text{m}^{-1}$, one can clearly see that the subthreshold slope is the steepest one, corresponding the biggest $G$ in figure 5(b).

That is to say, for a certain $t_f$, there is an optimal $\sigma$ enabling the voltage amplification factor to be the biggest and the subthreshold swing to be the smallest. For better to see the changes of SS with the gate voltage, we plotted the SS-$V_g$ curve in figure 7. Where, $t_f = 8$ nm, and $\sigma = 0.035 \times 10^{-11}$ $\Omega^{-1} \text{m}^{-1}$. It can be seen that the smallest value of SS is 27 mV dec$^{-1}$ when the gate voltage is about 0.5 V. This property can provide reference for the design and performance improvement of the NC-FETs.

In summary, an surface potential and drain current model considering the interface layer with an electric conductivity between the ferroelectric thin film and electrode was proposed in the MIFIS structure based on the Landau-Khalatnikov (LK) theory, Poisson equation, and current continuity equation. The influences of the conductivity on the $V_g-\phi_s$ characteristics, $G-V_g$ characteristics, and $I_D-V_g$ characteristics of the negative capacitance FET were simulated. The results showed that there is a best value of the electric conductivity for obtaining the maximal voltage amplification factor and the steepest subthreshold slope in the NC-FET, and the interface conductivity has a considerable influence on the electrical properties of the NC-FET. It was suggested that more attention should be paid to the arts and crafts of the NC-FET devices. Further work based on the TCAD simulation should be carried out [23, 24].

Figure 5. (a) The relationship between the silicon surface potential and gate voltage, and (b) the relationship between the voltage amplification coefficient $G$ and gate voltage with different conductivity of interface.
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Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.
Conflict of interest

The authors declared that they have no conflicts of interest to this work.

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