High-performance programmable grounded resistor and its applications

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ABSTRACT
Programmable resistor and analog computational circuits are essential for many applications such as analog signal processing units, automatic gain control, neural, fuzzy and instrumentation systems. A high-performance programmable grounded resistor (PGR) using complementary metal oxide semiconductor (CMOS) technology is proposed in this paper. A highly linear CMOS resistor with equivalent resistance ranging from 9.4 to 1.5 kΩ is obtained by cancelling the non-linear term present in the current equation of an MOSFET working in the linear region. The proposed resistor operates on both positive as well as negative input voltage. The inherited features of PGR are simplicity, extensive control voltage range, wider bandwidth and low-power dissipation. Additionally, analog computational units such as multiplier, squarer and divider are also discussed as applications of the PGR. All circuits are implemented and simulated using TSMC 0.13 μm CMOS technology in SPICE.

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Introduction
Resistor is one of the basic elements of analog signal processing applications [1,2]. Programmable resistors with accurate resistance value are imperative to on-chip-based systems and specific applications where variable resistance value is required. Unfortunately, the use of resistors has reduced in the field of integrated circuits due to the non-availability of accurate and programmable resistors. Many configurations have been proposed to implement programmable resistors using different techniques. Several resistors have been realized [3–12] using complementary metal oxide semiconductor (CMOS) technology and can be programmed externally. Few resistors are implemented using current conveyors, operational transconductance amplifier (OTA) arrays and the floating-gate metal oxide semiconductor transistor (FGMOS) technique. The drawbacks of these proposed resistors are short range of programmability, large silicon area and high power dissipation. Various applications of CMOS resistors are current to voltage converters, current mode dividers [12–14], multipliers [13,15–17,19–21], filters [22–24] and automated measurement systems [25]. These analog computational blocks which are implemented using these reported resistors lack high performance.

A simple CMOS-based programmable grounded resistor (PGR) is proposed in this paper which is operating on minimal power of only 34.1 μW. The other salient characteristics of the presented block are high linearity, wider bandwidth, less silicon area and ability to operate on both positive and negative input voltage values which proves it to be the most appropriate for various signal processing applications. Three simple and programmable analog computational blocks based on PGR, namely analog amplitude modulator (using multiplier), squarer and voltage divider have been suggested. These proposed circuits are most appropriate for analog systems where accuracy and programmability are crucial.

The paper is organized as follows: the second section presents proposed PGR. Second-order effects are considered in the third section. An amplitude modulator and squarer are presented in the fourth section in addition to voltage mode divider. The fifth section validates the theoretical results from simulation outcomes to confirm the effectiveness of proposed circuits. Lastly, the paper is concluded in the sixth section.

Proposed PGR

The proposed PGR and its symbol are shown in Figures 1 and 2. It consists of two N-type metal oxide semiconductor (NMOS) transistors M1 and M2, operating in linear region. V_in and I_in are the input voltage and current, respectively and V_c is the control voltage to tune the resistance of the circuit.

According to the square law relation, the drain current of M1 operating in the triode region is given by Equation (1).

\[ I_1 = k_1 \left( (V_c - V_{in1}) V_{in} - \frac{V_{in}^2}{2} \right). \]
This drain current is valid for the condition given in Equation (2) where $k_1$ is the transconductance parameter of $M_1$.

$$|V_{in}| = V_{DS1} < (V_{GS1} - V_{tn1}).$$ (2)

The value of $V_c$ should be selected greater than the threshold voltage $V_{tn1}$ for proper operation of circuit. The gate voltage applied to transistor $M_2$ is $V_{in} + V_c$ and the corresponding drain current is

$$I_2 = k_2 \left( (V_{in} + V_c - V_{tn2})V_{in} - \frac{V_{in}^2}{2} \right).$$ (3)

According to Figure 2, the input current $I_{in}$ is summation of $I_1$ and $I_2$

$$I_{in} = I_1 + I_2.$$ (4)

Since the drain to source voltages of both transistors are equal and it is fair enough to assume that threshold voltages are the same, $V_{in1} = V_{in2} = V_{in}$ in addition to the same transconductance parameters; $k_1 = k_2 = k$, the current expression is rewritten as

$$I_{in} = 2k((V_c - V_{in})V_{in}).$$ (5)

Hence, input resistance can be given as

$$R_{eq} = \frac{V_{in}}{I_{in}} = \frac{1}{2k(V_c - V_{in})}.$$ (6)

It can be seen that the non-linear term of Equation (1) is cancelled by current $I_2$, entailing the proposed circuit to behave as a linear resistor.

Bias voltage $V_{in} + V_c$ is generated by the summation circuit consisting of transistors $M_3$, $M_4$, $M_5$ and $M_6$ as shown in Figure 3. NMOS transistors $M_3$ and $M_4$ are working in the saturation region, whereas P-type metal oxide semiconductor (PMOS) $M_5$ and $M_6$ are biased to act as a current mirror. The drain currents of $I_3$ and $I_4$ are equal with assumption that transconductance parameters and threshold voltages of PMOS and NMOS transistors are equal respectively. Thus, gate to source voltages of $M_3$ and $M_4$ are also same and can be given as

$$V_{in} - V_{ss} - V_{t4} = V_x - V_{t3},$$ (7)

where $V_{ss} = -V_c$ and $V_{t3} = V_{t4}$ for the desired operation. Thus,

$$V_0 = V_{in} + V_c.$$ (8)

Second-order effects

It is necessary to consider second-order effects on the proposed circuits to analyse non-idealities [26].

Mobility degradation

The carrier’s mobility decreases under high electric field circumstances and is given by the expression:

$$\mu = \frac{\mu_0}{1 - \theta(V_{GS} - V_{tn})}. \tag{9}$$

The equivalent resistance equation will be modified by factor $m$ and is expressed by

$$R_{eq} = \frac{1}{mk^*2(V_c - V_{in})}. \tag{10}$$

$k$ is $\mu_0C_0W/L$ and $m$ is $1/1 - \theta(V_{in} - V_{tn})$ and the value mobility degradation parameter of $\theta$ ranges from 0.001 to 0.1 V$^{-1}$. The errors due to extremely small value of degradation parameter $\theta$ are insignificant. Thus, the output function will be slightly affected, except the voltage mode divider circuit which is independent of this factor.

Temperature variation

The relationship between the mobility of carriers and the temperature is given below:

$$\mu(T) = \mu(T_c)\left(\frac{T}{T_c}\right)^\gamma. \tag{11}$$
It is known that the temperature variation affects the transconductance parameter $\beta$. Mobility is calculated at $T_c$ to analyse the temperature variation where $T$ is the absolute temperature (300 K). The value of constant parameter $\gamma$ ranges from 1.5 to 2. The mobility decreases by maximum 6.3% ($\gamma = 2$) and minimum by 4.7% for $\gamma = 1.5$.

The interconnect resistance of MOSFET also gets affected by temperature variations and is expressed as below:

$$ R_i = R_0(1 + \alpha(T_i - T_0)), $$  \hspace{1cm} (12)

where $R_i$ is a resistance at temperature $T_i$ and the value of $\alpha$ is an empirical temperature coefficient of resistance with value 0.004 for copper wire and 0.0043 for aluminium wire. $R_0$ and $T_0$ are reference resistance and temperature, respectively. Suppose $R_0$ is 30 kΩ at 20°C, the value of $R_i$ at 30°C is 30.129 kΩ for copper and 30.129 kΩ for aluminium after using Equation (12) and results in an increase of 4% and 4.3%, respectively. It can be seen that the variations in interconnect resistance and mobility due to temperature will almost nullify each other. Thus, proposed circuits are less prone to error due to temperature variations.

### Mismatch effect

The mismatches in threshold voltages of transistors in the PGR circuit can add a DC offset to expression of equivalent resistance which can be nullified by offset applied externally. Second, the inequality of transconductance parameters can also cause deviation from the desired result. Assume that the $k_t$ is transconductance parameter of $M_1$ and $k_t + \Delta k_t$ of $M_2$ of PGR. The current expression given in Equation (4) can be rewritten as follows:

$$ I_{in} = I_1 + I_2 + \Delta I_2, $$  \hspace{1cm} (13)

$$ \Delta I_2 = \Delta k_1 \left( (V_{in} + V_c - V_{in2}) V_{in} - \frac{V_{in}^2}{2} \right). $$  \hspace{1cm} (14)

The value of $\Delta k_1$ is much smaller to affect the expression given in Equation (14) by a considerable amount. Moreover, a DC offset current added to circuit can nullify this mismatch.

### Applications

#### Proposed analog multiplier and squarer

An analog voltage multiplier can be implemented using two proposed PGRs as depicted in Figure 4. The gate voltages of $V_{G1a}$ and $V_{G2a}$ are $V_c + V_2$, and $V_1 + V_c$ and input voltages for $V_{G1b}$ and $V_{G2b}$ are $V_c$ and $V_c - V_1$, respectively. This analog multiplier can be utilized to realize amplitude modulating function.

**Figure 4. Configuration of analog multiplier.**

After simplification using Equations (1)–(6), the currents $I_a$ and $I_b$ are as follows:

$$ I_a = V_1 V_2 + 2(V_c - V_{in}) V_1, $$  \hspace{1cm} (15)

$$ I_b = 2((V_c - V_{in}) V_1). $$  \hspace{1cm} (16)

Thus, $I_{out}$ is found to be $I_a + I_b$ and is given by

$$ I_{out} = k(V_1 V_2). $$  \hspace{1cm} (17)

Hence, the above expression results in the multiplication of two input voltages with the assumption of matched transistors. Thus, it can be used to realize analog amplitude modulator.

For squarer, if $V_1 = V_2 = V_{in}$ is chosen then the configuration shown in Figure 4 will function as an amplitude squarer with expression given below.

$$ I_{out} = kV_{in}^2. $$  \hspace{1cm} (18)

Bias voltages $V_1 + V_c$, $V_2 + V_c$ and $-V_1 + V_c$ are generated using the bias circuit shown in Figure 3.

#### Proposed analog voltage divider

A new voltage mode divider is shown in Figure 5 and implemented using two PGRs and one NMOS transistor $M_3$ operating in the saturation region. Using Equations (1)–(6), the current $I_1$ can be given as

$$ I_1 = 2(V_c V_1) = I_{out}. $$  \hspace{1cm} (19)

The expression for $I_{out}$ is

$$ I_{out} = 2(V_2 V_{out}). $$  \hspace{1cm} (20)

The output voltage $V_{out}$ can be obtained from Equations (19) and (20) and expressed as

$$ V_{out} = V_c \left( \frac{V_1}{V_2} \right). $$  \hspace{1cm} (21)

Thus, the function of voltage division is achieved which can be programmed by control voltage $V_c$.

Bias voltages $V_c + V_{th}$ and $V_2 + V_{th}$ are obtained from the circuit mentioned in Figure 3 with $V_{as} = -V_{th}$. $V_c + V_1$ and $V_{out} + V_2$ are achieved using the bias circuit shown in Figure 3 again when the source of the $M_3$ of Figure 3 is connected to $V_{th}$ instead of ground.
Simulation results and comparisons

All the circuits proposed in this paper are validated through simulations using T-Spice in 0.13 μm TSMC BSIM3, CMOS technology with level 49. The aspect ratios of all transistors are chosen to be 1:1. $V_{dd}$ and $V_{ss}$ vary as the value of $V_c$ varies from 0.5 to 1.5. Figure 6 shows $I$–$V$ characteristics where the input current is applied to the circuit and corresponding voltage $V_{in}$ is measured for different values of control voltage $V_c$. The respective values of $R_{eq}$ are shown in Table 1. It can be seen that it is validating the analytical analysis that it functions as a linear resistor programmable by $V_c$ with equivalent values of resistance, $R_{eq}$ ranging from 9.46 kΩ to 1.5 kΩ. The effect of temperature on $R_{eq}$ is analysed and shown in Figure 7. $R_{eq}$ varies from 9.8 kΩ to 9.6 kΩ for temperature ranging from 50°C to −50°C leading to minor deviations.

In Figure 8, distortion analysis of PGR is measured for different values of sinusoidal input current of magnitude up to 50 μA at a frequency of 1 MHz. Maximum total harmonic distortion (THD) measured is 2.7% at $I_{in} = 50$ μA. The power dissipation observed for the circuit shown in Figure 2 is 946 nW which is remarkably low. The total power dissipation of PGR including bias circuit for $V_{in} + V_c$ is 34.1 μW at $V_c = 1$ V, which is again low. The frequency response of PGR for $R_{eq} = 9.4$ KΩ at $V_c = 0.5$ V is shown in Figure 9 with constant magnitude of equivalent resistance up to 130 MHz. The transient analysis and fast Fourier transform characteristics of the proposed PGR is given in Figure 10 for current input signal of magnitude 45 μA at

**Table 1.** $R_{eq}$ for different values of $V_c$.

| $V_c$ (V) | 0.5 | 0.6 | 0.7 | 0.8 | 1.0 | 1.25 | 1.5 | 2.5 |
|-----------|-----|-----|-----|-----|-----|------|-----|-----|
| $R_{eq}$ (kΩ) | 9.41 | 5.52 | 4.17 | 3.68 | 2.76 | 2.22 | 1.87 | 1.5 |

Figure 5. Proposed voltage divider.

Figure 6. DC characteristics of PGR for different values of $V_c$.

Figure 7. Variation in $V_{in}$ with respect to temperature.

Figure 8. THD analysis of PGR at $V_c = 1$.

Figure 9. Frequency response of PGR.

Figure 10. THD analysis of PGR at $V_c = 1$.
frequency of 1 MHz. The value of $R_{eq}$ is set to approximately 2 kΩ to get both the responses.

The output of the summation circuit is also shown in Figure 11 to verify the implementation given in Figure 2. Figure 11 depicts the linear increase in the output, $V_{in} + V_c$ when $V_{in}$ is varying and $V_c$ is constant at a value of 1 V.

Table 2 compares the proposed PGR with existing resistors available in the literature. The presented CMOS resistor is linear due to cancellation of non-linear terms of drain equations of both NMOS transistors. It works on positive as well as negative values of the input voltage $V_{in}$ ($V_{in} > 0$ and $V_{in} < 0$), whereas many reported resistor realizations operate only for positive values of $V_{in}$. It is evident that the proposed PGR achieved wider bandwidth of 130 MHz and provides broad range of programmability using control voltage $V_c$ varying from 0.5 to 2.5 V. It also dissipates less power up to 34.1 μW when compared to the reported circuits. THD observed is 2.7% which also low. Thus, the proposed PGR is most suitable for high-performance analog applications demanding low-power dissipation, tunability, linearity and less silicon area.

The operation of the analog amplitude modulator using the proposed voltage multiplier is analysed with input waveforms of $V_1(t) = 100 \text{mV} \sin(2\pi \times 10^5)$ and $V_2(t) = 200 \text{mV} \sin(2\pi \times 10^6)$ shown in Figure 12. The aspect ratio chosen for all transistors is 6.5 μm/0.13 μm. The modulated output waveform is depicted in Figure 13 for given input signal. For squarer function, Figure 14 depicts $V_1 = V_2 = 100 \text{mV} \sin(2\pi \times 10^6)$ and the output waveform is given in Figure 15 justifying the analytical analysis. The bandwidth measured is 79.9 MHz with a linear range of input voltage from +0.6 V to −0.6 V. The DC simulation results of the proposed voltage divider are shown in Figure 16 when $V_1$ is varied from 0 to 800 mV for different values of $V_2$ ranging from 0.6 to 1 V. The aspect ratio of all transistors chosen for the voltage mode divider circuit is 1:1 except $M_3$ which is 10:1. The bandwidth of the voltage divider is found to be 89 MHz and depicted in Figure 17.
Table 2. Comparison of proposed PGR with reported literature.

| Parameters                  | [3] | [4] | [5] | [6] | [7] | [8] | [9] | [26] | Proposed work |
|-----------------------------|-----|-----|-----|-----|-----|-----|-----|------|--------------|
| No. of transistors          | 5   | 9   | 2   | 2-MOS 3-FGMOS | 1, 3-R, 1-CCII | 3   | 22, 2-R | 2-MOS | 6            |
| No. of biasing voltage/currents | 1   | 2   | 2   | 1   | 1   | 1   | 3   | 0    | 0            |
| Technology (μm)             | –   | –   | –   | 0.25 | –   | 0.25 | 0.35 | 2    | 0.13         |
| Supply voltages (V)         | ±5  | ±5  | ±5  | ±0.75 | ±2.5 | ±1.25 | ±1.65 | ±5   | ±5          |
| Resistance range (kΩ)       | –   | 200 to 60 | 4 to 2 | –   | < 2.63 | 15 to 5 | 1.1 to 5.7 | –    | –           |
| Power dissipation (μW)      | –   | –   | –   | 254 | –   | 440 | 2600 | –    | 34.1         |
| Bandwidth (MHz)             | –   | –   | –   | –   | –   | > 100 | 100 | –    | 130          |
| Control voltage range (V)   | 2.4 to 3.3 | 0.10 to 0.75 | 0.65 to 2.5 | 0.0, 10, 01 | 8 to 15 | 0.50 to 2.5 | –    | –           |
| THD (%)                     | –   | –   | 2.5 | –   | –   | –   | 0.02 | 2.7  |              |

Figure 12. Input signals $V_1$ and $V_2$ for four-quadrant multiplier.

Figure 13. Output waveform of four-quadrant multiplier.

Figure 14. Input waveforms of squarer.

Figure 15. Output waveforms of squarer.

Figure 16. Variation in $V_{out}$ with respect to $V_2$.

Figure 17. Frequency response of voltage divider.
Conclusion

This paper proposed a new high-performance PGR and its applications in analog arithmetic circuits such as analog amplitude modulator, squarer and voltage mode divider. The power dissipation of PGR measured is 34.1 μW which is quite low. Wider bandwidth and broad programmability range are achieved. All circuits exhibit simplicity while validating the claimed theoretical results from simulation results. These blocks are believed to be beneficial for low-power analog applications such as analog fuzzy hardware, artificial neural networks and automated measurement systems.

Disclosure statement

No potential conflict of interest was reported by the authors.

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