Comparative Study of Switched Capacitor Converter Topologies for Wearable Devices

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Abstract. As wearable devices with low input voltages have drawn much attention from academic and industrial fields, the use of switched capacitor converters (SCC) also increases. This is because the wearable devices are required to utilize small size power converters and SCCs have no bulky circuit components such as magnetic components. Many kinds of SCCs have been suggested but they are based on three fundamental SCC topologies that are Dickson, series-parallel and Fibonacci topologies. In this study, three topologies are theoretically analyzed and simulated. With the results from them, a comparison is conducted to provide future circuit designers with a standard to choose a proper SCC topology for wearable devices.

1. Introduction

As semiconductor and Internet of Things technologies are advanced, wearable devices using low input voltages such as energy harvesting technologies have drawn a lot of attention from academic and industrial fields [1-3]. These devices are usually manufactured into small sizes. This requires them to use compact power converters. Among many kinds of power converters, switched capacitor converters (SCC) can be designed into a smaller size than inductor-based converters. This is because SCCs do not have inductors or transformers, which lead to reduce their sizes and to free from EMC (Electro-Magnetic Compatibility) or EMI (Electro-Magnetic Interference) problems. Until now, many SCCs have been suggested but they are based on fundamental topologies such as Dickson [4-7], series-parallel [8-10] and Fibonacci types [11-13].

In this paper, those three fundamental topologies are analyzed and compared by using a slow and fast switching limit impedance model, and simulations [14, 15]. This comparison can provide future circuit designers with a standard to select a proper SCC topology.

The remainders of this paper are organized as follows. In section II, circuit configurations of the fundamental SCC topologies are described. Section III carries out a theoretical analysis of the topologies. In section IV, those SCC topologies are simulated and compared. Section V concludes this study.

2. Circuit configuration

2.1. Dickson topology

The Dickson topology consists of \( n \)-1 (\( n \) is an integer) flying capacitors (\( C_n \)-1) and \( 3n-1 \) switches (S1 and S2) in Fig. 1, where \( V_{in} \) and \( V_{out} \) indicate the input and output voltages, and \( C_{out} \) are the output

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capacitor. This topology can generate $n$ times boosted output voltage. The Dickson topology is operated by turning on and off the switches, complementarily. With this operation, the Dickson topology has two equivalent circuits as shown in Fig. 2. In Fig. 2, $R_{on}$ are the on-resisters of switches, $\Delta q_{T1, Vin or out}$ and $\Delta q_{T2, Vin or out}$ are the charge amounts of the input and output at state-1 and 2, respectively. Additionally, the parameters in Fig. 1 and 2 are utilized in the other topologies for the same meaning of each of them. In state-1, flying capacitor C1 is charged up to the input voltage. The charged C1 and the input source charge flying capacitor C2 up to 2 times the input voltage in state-2. Generalizing this charging way to $C_n$, the output voltage of the Dickson voltage is yield as $nV_{in}$.

Figure 1. Dickson topology

Figure 2. Equivalent circuits of Dickson topology at state-1 and 2

Figure 3. Series-parallel topology
Figure 4. Equivalent circuits of series-parallel topology at state-1 and 2

Figure 5. Fibonacci topology

Figure 6. Equivalent circuits of Fibonacci topology at state-1 and 2
2.2. Series-parallel topology
The series-parallel topology consists of n flying capacitors and one output capacitor (Cn and Cout) and 3n-1 switches (S1 and S2) in Fig. 3. The switching rule of the series-parallel topology is the same as the Dickson topology. However, the flying capacitors are charged differently as shown in Fig. 4. In state-1, all of the flying capacitors are connected in parallel and charged up to the input voltage. In state-2, the charged flying capacitors are connected in series and charge the output capacitor up to n times the input voltage for nVin as the output voltage.

2.3. Fibonacci topology
The Fibonacci topology consists of n flying capacitors, one output capacitor and 3n+1 switches as shown in Fig. 5. This topology is operated by 2 modes of charging capacitors. In the first mode, the boosting ratio is Fibonacci numbers. The first mode is operated by turning on and off switches, complimentarily like the Dickson topology. In the first mode, n-2-th and n-1-th capacitors connected in series charge n-th capacitor. Therefore, the boosting ratio of n-th capacitor can be n-th Fibonacci number, where n is over 3. Fig. 6 shows the equivalent circuits for the first mode. The remainders of boosting ratios are generated in the second mode, where the number of equivalent states is 3 and all of the charged flying capacitors are connected in series. Taking 7 times boosting ratio for example, where the Fibonacci topology has 3 flying capacitors, the boosting ratio can be produced by using flying capacitors charged up to 1, 1, 2 and 3 times the input voltage. In state-3, the input source and the flying capacitors are connected in series and can boost the output voltage up to 7 times the input voltage.

3. Theoretical analysis
The three topologies are analyzed by using slow and fast switching limit output impedance model [14, 15]. Using this model, the frequency characteristic and power consumption caused by capacitors and switches can be examined. The analysis is conducted based on the equivalent circuits with assumptions as followed. The duty ratios between state-1 and 2 are fixed 50% (1/3 for Fibonacci topology in the second mode). The capacitance of flying and output capacitors are the same.

In state 1 of the Dickson topology, the relation of charge amounts of the input voltage and capacitors can be expressed by using Kirchhoff’s current law (KCL) as (1) and (2).

\[ \Delta q_{T1, Vin} = \Delta q_{T1}^1 - \Delta q_{T1}^2 - \Delta q_{T1}^3 - \cdots - \Delta q_{T1}^{n-2} \]  
\[ \Delta q_{T1}^{n-2} = -\Delta q_{T1}^{n-1} \]  

where \( \Delta q_{T1}^k \) is the charge amount of k-th capacitor during state-1 and \( T1 \) means state-1.

In state-2, the charge amounts are yielded as (3) and (4), using the same method for state-1.

\[ \Delta q_{T2, Vin} = \Delta q_{T2}^1 + \Delta q_{T2}^2 + \Delta q_{T2}^3 + \cdots - \Delta q_{T2}^{n-1} \]  
\[ \Delta q_{T2}^{n-3} = -\Delta q_{T2}^{n-2} \]  

where \( \Delta q_{T2}^k \) is the charge amount of k-th capacitor during state-2 and \( T2 \) means state-2.

From (1) to (4), the charge multiplier vectors, \( a1 \) and \( a2 \), for state-1 and 2 can be derived as (5) and (6) [14, 15].

\[ a1 = \begin{bmatrix} 1 & -1 & \cdots & -1 \end{bmatrix}^T \]  
\[ a2 = \begin{bmatrix} 1 & -1 & \cdots & 1 \end{bmatrix}^T \]  

Using (5) and (6), slow and fast switching limit output impedance can be calculated as (7) and (8).
\[ R_{SSL} = \frac{n^2}{Cf_{sw}} \]  
(7)

\[ R_{FSL} = 2(n^2 + 3n - 2) \]  
(8)

where \( R_{SSL} \) and \( R_{FSL} \) are the slow and fast switching limit output impedances, respectively, \( C_f \) is the capacitance of flying capacitors and \( f_{sw} \) is the switching frequency of one operation cycle.

The total output impedance, \( R_{out} \), is approximated by using (7) and (8) as (9).

\[ R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \]  
(9)

Using a similar analysis method above, the total output impedances of the other two topologies can be derived.

4. Simulation and comparison

4.1. Simulation

Simulations are conducted with the simulation condition as shown in Tab. 1 by using the SPICE tool (LTspice). The boosting ratios are selected from 2 to 10 with consideration of the fact that the voltage levels of the power sources for wearable devices are very low [1-3]. The power efficiencies of three topologies are described in Fig. 7.

4.2. Comparison

From Fig 7, the power efficiencies of the Dickson topology are the highest among the three topologies over all the boosting ratios. The power efficiencies of Fibonacci topology are higher than those of the series-parallel under the boosting ratios of 9. Fig. 8 shows the total output impedances of three topologies at different boosting ratios. The curves of the total output impedances are inversely proportional to those of the power efficiencies in Fig. 7, which confirms the validity of the theoretical analysis.

| Table 1. Simulation Condition |
|-------------------------------|
| Parameters                  | Values                           |
| On-resistor \((R_{on})\)     | 0.1 Ω                            |
| Load resistor \((R_L)\)      | 1 kΩ                             |
| Operation frequency \((f)\)  | 1 MHz                            |
| Capacitance \((C_f \text{ and } C_{out})\) | 10 μF |
| Duty ratio \((D)\)           | 1/3 for Fibonacci topology in the second mode and 50% for the others |
| Input voltage \((V_{in})\)   | 10 V                             |
Fig. 7 shows the influences of the operation frequency on the slow switching limit output impedances for three topologies. As the frequency increases, the impedance is reaching 0. However,
when the topologies are operated under 0.1 kHz, the series-parallel topology is impacted the most among three topologies.

Fig. 10 describes the total number of circuit components (capacitors and switches) of three topologies. Among them, the smallest circuit size is the Fibonacci topology.

![Figure 10. The number of circuit components](image)

### 4.3. Standard to choose topology

Three results of the comparison can provide a standard to choose a proper SCC topology. For instance, if a wearable device requires a high power efficiency topology and its circuit size is not an issue, Dickson topology can be a solution. When the design issues are relatively high power efficiency and small size, the Fibonacci topology can be a solution.

In the case that the selected circuit topology is applied to a target system of a wearable device, the total output impedances based on (9) shown as in Fig. 8 can be utilized to check the input impedance of the applied system.

### 5. Conclusion

In this paper, the Dickson, series-parallel and Fibonacci topologies have been theoretically analyzed, simulated and compared. From the comparison, it is confirmed that the topology of the highest power efficiency is the Dickson topology, the topology with the smallest size is the Fibonacci topology, and the operation in the low frequency under 0.1 kHz has negative impacts on the series-parallel topology. These results can provide future circuit designers with a standard to select a proper SCC topology for wearable devices.

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