The Doping of Si p-Field-Effect Transistor Devices by Gallium Focused Ion Beam Implantation Enabling Flexible Fabrication Routes at Moderate Temperatures

Felix Winkler,* Carsten Strobel, Christian Wenzel, and Johann W. Bartha

A maskless approach of forming p-doped regions in Si wafers using the Ga source of a standard focused ion beam (FIB) system and the moderate activation temperatures of 400–700 °C is demonstrated in this work. This simple and flexible route is accessible to many research labs and is successfully used to fabricate Si-based diodes and field-effect transistors (FETs). For the diodes, tunneling is found to be the forward current transport mechanism. The fabricated p-FET structures show excellent switching behavior with a high $I_{D,ON}/I_{D,OFF}$ current ratio of $5 \times 10^6$.

1. Introduction

Gallium is used as a p-type dopant of silicon for various applications, including long-wavelength IR silicon detectors in the atmospheric window between 8 and 14 μm [11] and in photovoltaics as a substitution for boron substrate doping to extend the minority carrier lifetime and to reduce degradation [2, 3]. Already in the 1980s, Ga implantation with an acceleration energy of $E = 275$ keV [4] and for focused ion beam (FIB) implantation with $E = 50$ keV [5] together with moderate activation and annealing temperatures of 400–700 °C have been demonstrated. While the previous studies [4, 5] analyzed doping profiles, sheet resistances, and a structural analysis of the Si crystal, a performance test in real devices has not been conducted. While the FIB technique is increasingly used for micro- and nano-analysis, ion microscopy, and the repair of interconnects, [6] its application for direct doping in semiconductor device manufacturing is strongly limited by the low throughput. [7] However, maskless doping is of interest for experimental devices and research or academic institutions where an FIB tool is available as imaging equipment and lamella preparation. It brings superior design flexibility, allows structures in the 100 nm range, and eliminates photomask purchasing costs. In this regard, bipolar transistors [8], junction gate field-effect transistors (JFETs) [9], in-plane gate transistors [10], and also metal-oxide-semiconductor field-effect transistors (MOSFETs) [11] have already been realized using a Ga FIB tool. However, electrical data of the MOSFETs have not been shown by Wanzenboeck et al. [11] and the same applies to an insight into a possible integration flow for the fabrication of the p-field-effect transistor (FET). Our work closes this gap and additionally expands the presented output and transfer characteristics by simulations in LTspice. We use FIB implantations of gallium for the fabrication of diodes and an active device in the form of a p-FET. An additional investigation of diodes allows to compare our process to previous studies [12, 13].

While the FIB-based implant is fully capable of defining doped regions with lateral dimensions down to the 100 nm range, this exceeds the limits of the i-line contact lithography system used to define the metal contacts of source, drain, and gate of the FET. Therefore, we realized doped areas with dimensions in the micrometer range. A possible application is the realization of a p-through-silicon via FET (TSVFET) with a hole diameter of several tens of micrometers that was only published as an n-FET before. [14] Through silicon vias are often introduced in the presence of the metallization, [15] allowing only low thermal budgets for its fabrication. The moderate activation temperature of implanted gallium in silicon enables the fabrication of active device inside these holes.

2. Gallium-Doped Silicon Diodes

2.1. Preliminary Considerations

An FEI Expida 1285 FIB system has been used, allowing acceleration voltages between 3 and 30 kV. Simulations using the SRIM [16] software revealed a projected range $R_p$ of 29.6 nm and a longitudinal straggling $\Delta R_p$ of 9.3 nm for the highest possible ion energy of 30 kV. The implantation of Ga using very high ion fluences leads to the formation of a very shallow continuous amorphous Si layer. This critical fluence was found to be $8\times10^{13}$ ions cm$^{-2}$ for 50 keV Ga implantations. [5]. To form a
continuous amorphous Si layer using a lower implantation energy of 30 keV, the fluence must be larger and was, therefore, chosen in the range of $10^{10}$ ions cm$^{-2}$. This allowed low activation temperatures in the range of 400–600 °C by regrowing the Si crystal from the amorphous layer and incorporating the Ga via solid phase epitaxy.\[4,17\] This temperature is rather low compared with vacancy-mediated self-diffusion, which usually requires above 750 °C.\[18\]

Grove reported an activation energy of $E_A = 3.31$ eV and a pre-exponential factor of $D_0 = 8.21 \times 10^{-5}$ m$^2$ s$^{-1}$ for the diffusion of Ga in Si.\[19\] For Ga diffusion in SiO$_2$, an activation energy of $E_A = 4.17$ eV and $D_0 = 1.04 \times 10^5$ m$^2$ s$^{-1}$ could be calculated from the previous studies.\[20,21\] This allows the determination of the diffusion length $L_D$ of gallium in Si and SiO$_2$ during the activation anneal, that is required after implantation, by the following equations

$$L_D = \sqrt{2Dt} \tag{1}$$

$$D = D_0 \times \exp\left(-\frac{E_A}{kT}\right) \tag{2}$$

where $t$ is the diffusion time, $D$ is the diffusion coefficient, $k$ is the Boltzmann constant, and $T$ is the diffusion temperature.

### 2.2. Diode Fabrication

The diodes were fabricated on phosphorous n-doped Si (100) substrates ($1 \times 10^{15}$ ions cm$^{-2}$) with a thickness of 525 μm. The fabrication steps are shown in Figure 1. The implantation was performed with an acceleration voltage of 30 kV with no tilt angle, and the fluence varied between 1 and $8 \times 10^{16}$ cm$^{-2}$, while using a low ion current (5900–8250 pA) to limit the Si layer removal to <10 nm. Due to this superimposed sputter effect of the surface, the concentration maximum shifts to deeper regions. The roughness was below 5 nm, as obtained by measurements using a Veeco Dektak 8 profiler. The so-called “TV Mode” of the FEI Expida 1285 was used, whereby an optimal resolution was achieved using a beam diameter of 10 nm for implantation of a rectangular area in multiple scans.

A maximum activation temperature in the range of 400–700 °C was applied for 15 min in N$_2$ atmosphere in a conventional furnace. As shown in Table 1, the change of the implantation profile is negligible at these temperatures (e.g., diffusion length of 1.1 nm in Si at 700 °C). Table 1 summarizes the calculated diffusion lengths of Ga in Si and SiO$_2$, indicating the fast diffusion in SiO$_2$. The real values are expected to be slightly higher, because the samples additionally experienced the upward and downward ramps of the furnace ($T_{\text{max}}$ was reached after 30 min, cool down within 30 min to $T < 100$ °C).

### 2.3. Diode Characterization

#### 2.3.1. Current–Voltage Characteristics

$I$–$V$ measurements were conducted and showed typical diode behavior for all samples (Figure 2a) except for samples 6 and 7 where a large series resistance dominates the forward current

| Sample | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|--------|---|---|---|---|---|---|---|
| $T_{\text{max}}$ [°C] | 400 | 450 | 500 | 550 | 600 | 650 | 700 |
| $t$ [min] | 15 | 15 | 15 | 15 | 15 | 15 | 15 |
| $L_D$ (Si) [m] | 2.9E-11 | 2.9E-11 | 2.9E-11 | 2.9E-11 | 2.9E-11 | 2.9E-11 | 2.9E-11 |
| $L_D$ (SiO$_2$) [m] | 6.4E-12 | 6.4E-12 | 6.4E-12 | 6.4E-12 | 6.4E-12 | 6.4E-12 | 6.4E-12 |

**Table 1.** Annealing conditions for the diode samples and the calculated diffusion lengths $L_D$ of Ga in Si and SiO$_2$ for these parameters.

![Figure 1. Fabrication of the Ga-doped Si diodes.](image-url)
of the diodes. The high leakage currents of samples 6 and 7 occur due to a so-called “reverse” annealing effect, namely, a decrease in the electrical activity of the implanted ions when a critical annealing temperature is exceeded. As Figure 2b shows, the highest on-current density ($J_{\text{on}}$ at 1 V) was obtained for the activation temperature of 400 °C, and it is also accompanied by the largest on/off current ratio of all diodes. The higher the activation temperature, the more Ga will escape from the silicon, and the lower is the resulting surface dopant concentration. This is detrimental to the contact resistance of the metal–semiconductor interface. The effective resistance of this Schottky barrier is, among other things, determined by the doping concentration at the interface. The expected result of an increasing contact resistance is a reduction of the output current density $J_{\text{on}}$ of the diode, which is exactly what our experimental observations in Figure 2b show for the annealing temperatures of 650 and 700 °C. The sample that was annealed at 500 °C should be viewed with caution, because the activation energy of the saturation current density differs strongly from the other samples, as shown in the following.

2.3.2. Temperature Dependence

$I–V–T$ measurements have also been performed to gain insights into the current transport mechanism dominating the $p–n$ junction. In general, the forward current density of a $p–n$ junction can be expressed as

$$J(V, T) = J_0(T) \left( \exp\left(\frac{qV}{n k T}\right) - 1 \right)$$

with

$$J_0(T) \propto \exp\left(-\frac{E_a}{k T}\right)$$

and

$$A = \frac{q}{n k T}$$

where $J_0$ is the saturation current density, $A$ is the temperature-dependent coefficient, $n$ is the diode ideality factor, and $k$ is Boltzmann’s constant. Typical current transport mechanisms that have been proposed are diffusion, recombination, thermionic emission, and tunneling (see Table 2). By comparing the measured activation energies $E_a$ of $J_0(T)$, $n$ as well as $A(T)$ with the model prediction (see Table 2) conclusions about the conduction mechanisms in the devices can be drawn.

**Figure 2.** a) $J–V$ curves and b) on/off current comparison and on-current density $J_{\text{on}}$ at 1 V for different activation temperatures.

**Table 2.** Current transport mechanisms of $p–n$ diodes with saturation current density $J_0(T)$, temperature-dependent exponential term $A(T)$, and diode ideality factor $n$.

| Conduction mechanism | $J_0(T)$ | $A(T)$ | $n$ |
|----------------------|----------|--------|-----|
| Diffusion            | $J_0 \propto \exp(-q E_a/k T)$ | $A = q/k T$ | 1   |
| Recombination        | $J_0 \propto \exp(-q E_a/2k T)$ | $A = q/k T$ | ≤ 2 |
| Tunneling            | $J_0 \propto \exp(-q E_a/k T)$ | $A = \text{const.}$ | $n \neq \text{const.}$ |
| Thermionic           | $J_0 \propto T^n \exp(-q \Phi a/k T)$ | $A = q/k T$ | 1   |

**Figure 3a** shows the exponential term $A$ as a function of $1000/T$ for selected devices, which were annealed at different temperatures (400–700 °C). As it is shown, the exponential term $A$ is almost independent of the measurement temperature (1000/°C). This demonstrates that the temperature-independent conduction mechanism of tunneling dominates the devices— independent of the dopant activation and annealing temperature. This is in contrast to the study of Mogul and Steckl, where diffusion and generation currents were identified for $p–n$ diodes based on Ga implantation of lightly doped $n$-Si substrates. However, the annealing conditions and Ga fluence in the present study were different compared with Mogul et al., which might also lead to different electrical transport across the $p–n$ junction. The saturation current density $J_0$ as a function of $1000/T$ is shown in Figure 3b. Here, $J_0$ is extracted from a fit of the exponential part of the $J–V$ curves between about 0.1 and 0.4 V. The exponential relationship between $J_0$ and $1000/T$ is matching most with multistep tunneling capture emission (MTCE) as the tunneling model, comparing it with data from the previous study. The extracted activation energies $E_a$ in Figure 3b span a range of 0.56–0.71 eV, except for the sample annealed at 500 °C, that exhibits a much lower value of 0.17 eV, which we believe is an outlier. The relatively high activation energies for the majority of the samples indicate that the electron capture rate is larger than the hole emission rate.
3. Gallium-Doped Silicon FETs

3.1. p-FET Fabrication

Si wafers (100) with phosphorous n-doping \((1 \times 10^{15} \text{ ions cm}^{-3})\) and a thickness of 525 μm were used as a substrate. A SiO\(_2\) layer of 1000 nm thickness was thermally grown at 1000 °C in H\(_2\)O atmosphere to serve as field oxide (FOX). Alternatively, a plasma-enhanced chemical vapor deposition (PE-CVD) process as the one described in the following could be used in the case of a restricted thermal budget. The source and drain areas were patterned using a first lithography mask. Wet etching was done with buffered hydrofluoric acid (BHF). Subsequently, gallium was implanted, utilizing an FEI Expida 1285 FIB system. The resist was left on top of the oxide to protect it from the ion bombardment. A rectangular area, overlapping source and drain, was scanned by the ion beam, as shown in Figure 4a. The implantation fluence was varied between 1.3 and 2.3.

![Diagram](image)

**Figure 4.** Integration flow of the Ga-doped p-FET device.
and the ion current was again kept very low at 600 pA, leading to a very thin Si layer removal of about 10 nm and a Si surface roughness of <5 nm. An acceleration voltage of 30 kV was used, and there was no tilt angle between the wafer surface normal and the ion beam. The resist was subsequently removed, and 500 nm of SiO$_2$ was deposited via the PE-CVD process using silane and nitrous oxide at 340 °C, as shown in Figure 4b. This cover layer should primarily prevent a contamination of the silicon originating from the furnace tube during thermal activation and annealing performed in N$_2$ for 15 min at 600 °C. Subsequently, the CVD oxide was removed with BHF. During that treatment, the underlying thermally grown SiO$_2$ layer serving as FOX was thinned down from originally 1000 to 890 nm.

With a second mask, the active area was defined (patterning of the FOX) by removing the remaining silicon dioxide in the channel area between source and drain and in a small section around them (Figure 4c).

The gate dielectric was made of a stack of SiO$_2$ and Al$_2$O$_3$. The oxide was grown at 700 °C for 60 min, resulting in a layer of 8 nm thickness. As shown by preliminary experiments, Ga tends to agglomerate under very high temperatures; therefore, it had to be kept moderate for the gate oxidation.

This higher thermal budget is expected to negatively affect the performance of the source/drain junctions and contact resistances (compare with Figure 2a, diode reverse current density is several orders of magnitude higher for 650/700 °C anneal than lower temperatures). However, the corresponding MOSFETs show an excellent switching behavior. To safely prevent a degradation at this point, an even thinner chemically grown interface oxide (SC1 or piranha treatment) could be an alternative. As mentioned in Section 2, gallium diffuses fast in SiO$_2$ (segregation coefficient $m > 1$), and a diffusion length of 4.4 nm is expected for annealing at 700 °C for 60 min. Thus, most of the Ga diffusing into the SiO$_2$ also escapes into the furnace atmosphere, and the surface concentration in the silicon is reduced. A layer of 30 nm Al$_2$O$_3$ was deposited on top of the SiO$_2$ by thermal atomic layer deposition (ALD) at 300 °C with tri-methyl aluminum (TMA) and H$_2$O as the precursors.[24] As shown in Figure 4d, a third mask was used to structure contact holes, which was again done by wet etching with BHF.

A stack of titanium (20 nm, as Si diffusion barrier to prevent spiking[25]) and aluminum (300 nm) was deposited by e-beam evaporation and structured by a fourth mask as the gate metal as well as the source and drain contact metal. Wet etching was done by an etchant containing phosphoric acid (for Al) and 0.5% HF (for Ti). The backside of the wafer was metallized by Al (500 nm) to ensure a good body contact. The fabrication was concluded by a forming gas anneal at 400 °C for 45 min (5% H$_2$ in N$_2$ at atmospheric pressure) to reduce the contact resistivity and to passivate oxide and interface defects. The transistor structure is shown in Figure 4e.

The gate lengths of the transistors ranged from 10 to 25 μm. The top view microscope image of a transistor with a gate length of 15 μm is shown in Figure 5.

### 3.2. p-FET Characterization

The p-FETs were electrically characterized with a Keithley 4200 Semiconductor Characterization System. Output curves $I_D(V_D)$ and transfer curves $I_D(V_G)$ were measured in direct current mode. The results for transistors with a gate length of 15 μm are shown in Figure 6a,b. Output curves with a very stable saturation could be measured, and a very high $I_{D,ON}/I_{D,OFF}$ ratio was found at 5 × 10$^6$ ($V_D = -6$ V and $V_{G,ON} = -4$ V/$V_{G,OFF} = 0$ V), representing an excellent switching behavior. The threshold voltage was −0.61 V, and a maximum field-effect mobility of 480 cm$^2$ V$^{-1}$ s$^{-1}$ was calculated from the transfer curve using a gate capacitance per unit area of 1.53 × 10$^{-1}$ As V$^{-1}$ m$^{-2}$. The sub-threshold swing was found to be 73 mV dec$^{-1}$, which is a typical value for silicon MOSFETs.

### 3.3. Simulation in LTspice

Simulations of the p-FET were done in LTspice.[26] The following parameters were defined for the model.

![Figure 5](image-url)  
**Figure 5.** Top view microscope photograph of the transistor with 15 μm gate length.

![Figure 6](image-url)  
**Figure 6.** a) Output curves and b) transfer curve and calculated field-effect mobility for the p-FET with a channel length of $L = 15$ μm and a channel width of $W = 29$ μm.
Table 3. Simulation in LTspice.

|                | $I_{D, sat}$ (V$_G$ = 0 V) | $I_{D, sat}$ (V$_G$ = -2 V) | $I_{D, sat}$ (V$_G$ = -4 V) |
|----------------|---------------------------|---------------------------|---------------------------|
| **Measurement**| $1.9 \times 10^{-11}$ A   | $2.9 \times 10^{-5}$ A    | $9.5 \times 10^{-5}$ A    |
| **Simulation** | $1.2 \times 10^{-11}$ A   | $3.0 \times 10^{-5}$ A    | $9.3 \times 10^{-5}$ A    |

PMOS(LEVEL = 3  $L = 15\mu m$  $W = 29\mu m$  VTO = $-0.61$

TOX = 22.6 n TPG = 0  $U0 = 480$  $RS = 24k$  $RD = 13k$)

The simulated saturation currents are in good agreement with the measurements, as shown in Table 3. To achieve this good fit, the source and drain resistances (RS and RD) had to be set to very high values of 24 and 13 kΩ, respectively. Under the assumption of single crystal Si, an average doping concentration in the range of $3 \times 10^{17} - 7 \times 10^{17}$ cm$^{-3}$ was calculated for the estimated junction depth of 39 nm ($\approx R_p + \Delta R_p$), a source/drain width of 29 μm, and also, a contact hole distance of 29 μm from the transistor channel. The activated carrier concentration of gallium is expected to exceed these moderate values, because the S/D resistance is negatively affected by the grain boundaries and crystal defects resulting from incomplete annealing after implantation.\[5\]

4. Conclusion

We report the maskless doping using a standard FIB instrument for Ga implantation into silicon. The capabilities of this approach were assessed in Si diodes and p-FETs as demonstrator devices. The activation of the implanted dopants could be done at moderate temperatures between 400 and 700°C. This makes gallium an interesting alternative dopant for low thermal budgets. Independent of the annealing temperature, the mechanism of tunneling is dominating for the manufactured diodes as the forward current transport mechanism. An integration flow for the transistors is shown that yields devices with a very low off-current below $10^{-11}$ A and a very high $I_{D, ON}/I_{D, OFF}$ ratio of 5 × 10$^6$ for $V_G = -4$ V. While we used micrometer-sized "lab-scale" devices in this work due to limitations of our metal lithography process, we believe that the process can be transferred to more advanced scaling nodes enabling design flexibility and low activation temperatures. A lateral scattering of 7.2 nm was obtained for an ion energy of 30 keV from SRIM simulations for the impinging Ga ions—a radius of 3.6 nm surrounding the point of impact. With a minimal beam diameter of about 10 nm, the lateral dopant distribution could be kept at a minimum of <15 nm. As the minimal point-to-point distance is in the range of several 10 nm (typical for transmission electron microscope lamella preparation), a minimal source/drain spacing (representing the channel length of the FET) in the same range is expected.

Acknowledgements

The authors thank Tony Schenk from the Luxembourg Institute of Science and Technology (LIST) for fruitful discussions and valuable comments that improved the manuscript. Open access funding enabled and organized by Projekt DEAL.

Conflicts of Interest

The authors declare no conflict of interest.

Keywords

field-effect transistors, focused ion beam implantation, maskless gallium doping

Received: August 10, 2020
Revised: October 28, 2020
Published online: December 2, 2020

[1] J. Guldberg, *Neutron-Transmutation-Doped Silicon*, Springer, New York, NY, 2013, p. 437.
[2] S. W. Glunz, S. Rein, J. Knobloch, W. Wettling, T. Abe, *Prog. Photovolt: Res. Appl.* 1999, 7, 463.
[3] G. Eranna, *Crystal Growth and Evaluation of Silicon for VLSI and ULSI*, CRC Press, Boca Raton, FL, 2014.
[4] B. M. Arora, J. M. Castillo, M. B. Kurup, R. P. Sharma, *Radiation Effects* 1982, 63, 47.
[5] M. Tamura, S. Shukuri, M. Momiwa, M. Default, *Appl. Phys. A* 1986, 39, 183.
[6] J. Gierak, *Nanofabrication 2014*, 1, 35.
[7] M. I. J. Beale, C. Broughton, V. G. I. Deshmukh, *Microelectron. Eng.* 2016, 4, 233.
[8] C. M. Lin, A. J. Steckl, T. P. Chow, *J. Vac. Sci. Technol. B* 1988, 6, 977.
[9] J. De Marco and J. Melngailis, *Solid-St. Electron.* 2004, 48, 1833.
[10] C. Crell, K. Wiczek, H.-U. Schreiber, A. D. Wieck, *Appl. Phys. Lett.* 1996, 68, 2538.
[11] H. D. Wanzenboeck, C. Ostermaier, A. Gruen, B. Eichinger, M. Karner, E. Bertagnolli, *Nucl. Instr. Meth. B* 2006, 242, 257.
[12] H. C. Mogul, A. J. Steckl, *IEEE Elec. Dev. Lett.* 1993, 14, 123.
[13] H. C. Mogul, A. J. Steckl, E. Ganin, *IEEE Trans. Elec. Dev.* 1993, 40, 1823.
[14] F. Winkler, S. Killge, D. Fischer, K. Richter, A. Hiess, J. W. Bartha, *IEEE Elec. Dev. Lett.* 2018, 39, 1493.
[15] ITRS, *International Technology Roadmap for Semiconductors Interconnect – 2009 Edition*, https://www.semiconductors.org/wp-content/uploads/2018/09/Interconnect.pdf (accessed: August 2020).
[16] J. F. Ziegler, *SRIM – The Stopping and Range of Ions in Matter*, http://www.srim.org (accessed: August 2020).
[17] J. S. Williams, R. G. Elliman, W. L. Seidel, *Phys. Rev. Lett.* 1985, 55, 1482.
[18] T. Sudkamp, B. Hartnutt, *Phys. Rev. B* 2016, 94, 125208.
[19] A. S. Grove, *Physics And Technology Of Semiconductor Devices*, Wiley, New York, NY 1967.
[20] A. S. Grove, O. Leistiko Jr, C. T. Sah, *J. Phys. Chem. Solids* 1964, 25, 985.
[21] A. H. van Ommen, *J. Appl. Phys.* 1985, 57, 1872.
[22] H. Matsuura, T. Okuno, H. Okushi, K. Tanaka, *J. Appl. Phys.* 1984, 55, 1012.
[23] Y. J. Song, M. R. Park, E. Guliants, W. A. Anderson, *Sol. Energy Mater. Sol. Cells* 2000, 64, 225.
[24] M. Knaut, M. Junige, V. Neumann, H. Wojcik, T. Henke, C. Hossbach, A. Hiess, M. Albert, J. W. Bartha, *Microelectron. Eng.* 2013, 107, 80.
[25] G. Bose, *IC Fabrication Technology*, McGraw-Hill Education, New Delhi 2013.
[26] M. Engelhardt, *LTspice Manual, 2011*, http://www.ieca-inc.com/images/LTSPICE_Manual.pdf (accessed: August 2020).