DESIGN AND IMPLEMENTATION OF 64 BIT IIR FILTERS USING VEDIC MULTIPLIERS

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Abstract

Digital signal processing operation utilizing Vedic mathematics which performs the signal handling operation like convolution, circular convolution, cross correlation, auto-correlation and filter design. Digital signal processing (DSP) operations are vital part of engineering and medical field. Outlining of DSP operations have numerous methodologies. This configuration procedure gives the analysis of signals to enhance the accuracy of the mathematical calculations. It encourages the time sharing for all signals to process mathematical operations all the while. Vedic mathematics is the ancient math which has a unique method of mental calculation with the assistance of basic rules and standards based on sutras. The utilization of multiplier with higher speed is of most extreme significance to any DSP. Convolution is the fundamental idea of designing Infinite Impulse Response (IIR) filter. IIR filter is likewise called convolution filter. Our project has demonstrated the efficiency of Urdhava-Tiryagbhyam method for multiplication which conveys a distinction in the real procedure of multiplication itself. The configuration of IIR filters utilizing Urdhava-tiryagbhyam sutra. This calculation is performed in Xilinx 13.4 ISE and implemented on vertex-5 FPGA (XC5VLX50T+1136).

Keywords: DSP; IIR Filters; Urdhva tiryagbham; vedic mathematics; FPGA(vertex-5).

1. Introduction

High speed multiplier is a standout amongst the most critical parts in outlining Digital Signal Processors (DSPs). Digital Signal Processing (DSP) operations, for example, convolution, correlation, Fast Fourier Transforms (FFTs)
and so forth make utilization of multipliers. Computational speed and execution time are the two elements that choose the productivity of augmentation calculation. In this DSP, filtering (sifting) is a typical term that is connected to different kinds of applications. Advanced feature oblige computerized filters to decrease noise because of coding and transmission through a noisy channel. As a rule, any operation performed to concentrate needed data from a digital signal is known as filtering. Information put away in memory contains loads of data both desirable and non-desirable. Desirable data is particular data at a particular frequency and non-desirable data is the commotion (noise) introduce in the signal. Digital filter performs scientific operations on a discrete time signal, sampled to diminish or upgrade certain parts of the information or signal. Advanced digital filters performs scientific operation on an inspected, discrete timed sign to accomplish the wanted highlights with the assistance of an exceptionally planned digital signal processor (DSP) chip or a processor utilized as a part of a universally useful PC.

2. Vedic Mathematics

"Vedic" is a Sanskrit word got from "Veda" that implies the gathering of all information. Veda is a blessing from old sages of India. From the antiquated times Vedas were gone from past era to next era orally instead of composed. Vedic mathematics is basically in light of 16 Sutras (or axioms) managing different sectors of arithmetic like arithmetic, trigonometry, geometry, algebra and so on.

3. Urdhava – Tiryagbyam

Urdhava Tiryagbhyam word is taken from Sanskrit, which indicates vertically and crosswise meaning in English. This method is general duplication equation appropriate to all instances of duplication. This is taking into account a novel idea through which every single incomplete item are created simultaneously. Indicated beneath figure 1 P3P2P1P0 & Q3Q2Q1Q0 shows parallel-duplication utilizing this strategy. The strategy can be summed up for N x N bit augmentation. This type sort of multiplier is free of the clock recurrence of the processor in light of the fact that the halfway items furthermore, their aggregates are ascertained in parallel.

Figure 1. Urdhava-Tiryagbhyam method of two bits number multiplication.

The net favorable position is that it lessens the requirement of microchips to work at progressively high clock frequencies. According to the working recurrence of processor builds the quantity of exchanging cases likewise increments. This outcomes in more power utilization furthermore dispersal as warmth that results in higher gadget working temperatures. Second point of interest of Urdhva Tiryagbhyam multiplier is adaptability. The preparing force can undoubtedly be expanded by expanding information and yield information transport widths from it has a consistent figure. Because of its standard design, it can be effortlessly design in a silicon chip furthermore devours ideal zone. As the quantity of info bits build, entryway delay and territory increment gradually
when contrasted with different multipliers. Along these lines Urdhava Tiryagbhyam multiplier is space, time, & power productive.

Fig.2. Design of Q63 format multiplier.

Fig.2 shows architecture of multiplier. Consider a 64 bit Q63 multiplier; the result is a Q63 bit number that is 64 bits in length. Initially, if most significant bit of input is 1 then it indicates negative number. Therefore 2’s complements of these numbers are taken before performing operation of multiplication. Therefore most significant bit indicates sign it is excluded in this place while multiplying.

A Q63 format multiplier includes four 32x32 Urdhava tiryagbyam multipliers and resulting outcome is of 64 bits long in length. Then the 128 bit product is taken left shifted by 1 bit to delete redundant sign bit and only higher 64 bits of this product result are taken as final result of this multiplier. XOR logic is considered based on the input sign bits to calculate the sign of the result of this product. In case result is ‘1’ then it processes the operation of 64 bits final result to its 2’s complement format to make it as negative product.

4. IIR Filters

IIR filters are digital filters with vast motivation reaction. Dissimilar to FIR filters, they have the feedback and is called recursive digital filters.

Fig.3. Block diagram of FIR and IIR Filter.

The IIR filters have vastly improved frequency reaction than FIR filters of the same request (order). Dissimilar to FIR filters, their stage trademark (phase characteristics) is not direct which can bring about an issue to the frameworks which need stage linearity. For this reason, it is not desirable over utilization IIR filters in digital signal processing when the phase is of the substance. FIR filters can have straight phase trademark that is certainly not normal of IIR filters. When it is important to have straight phase trademark, FIR filters are the main accessible arrangement. In different situations when straight phase trademark is redundant, for example, FIR filters, speech signal processing is bad arrangement. IIR filters ought to be utilized. The subsequent filter request is significantly
lower for the same frequency reaction. The IIR filter transfer function is a proportion of two polynomials of complex variable $z^{-1}$.

The numerator characterizes area of zeros, though the denominator characterizes area of poles of the subsequent IIR filter transfer function.

**Types of IIR Filter**

a) Butterworth filters.

b) Chebyshev filters.

c) Inverse Chebyshev filters.

d) Elliptic filters.

5. Implementation results

**Butterworth filter**

![Simulation result of Butterworth filter](image_url)
Fig. 5. RTL schematics of Butterworth filter.

Fig. 6. Hardware implementation result of butterworth filter

Chebyshev 1 Filter

Fig. 7. Simulation result of chebyshev 1 filter
Fig. 8. RTL schematic of Chebyshev 1 filter.

Fig. 9. Simulation result of Chebyshev 2 filter.

Fig. 10. RTL schematic of Chebyshev 2 filter.

Chebyshev 2 Filter
**Elliptical filter**

![Fig.12. Simulation result of elliptical filter.](image)

![Fig.13. RTL schematic of elliptical filter.](image)

Table no.1 comparison between MATLAB (16-bit and 32-bit) and XILINX (64-bit)

| S. No. | IIR Window | Vedic method implemented in MATLAB (16-bit) | Conventional method implemented in MATLAB (32-bit) | Vedic method implemented in XILINX ISE (32-bit) | Vedic method implemented in XILINX ISE (64-bit) |
|--------|------------|---------------------------------------------|---------------------------------------------------|-----------------------------------------------|-----------------------------------------------|
| 1      | Butterworth | 0.53ms                                      | 4.01ms                                            | 1.55ms                                        | 23.239ns                                      |
| 2      | Chebyshev 1 | 0.60ms                                      | 4.45ms                                            | 1.15ms                                        | 23.221ns                                      |
| 3      | Chebyshev 2 | 0.67ms                                      | 3.99ms                                            | 1.01ms                                        | 22.809ns                                      |
| 4      | Elliptical  | 0.65ms                                      | 3.74ms                                            | 1.07ms                                        | 23.432ns                                      |

Note: The values represent the time taken for the respective filters to execute.
6. Conclusion

The proposed structure of IIR filters utilizing Urdhava Tiryagbhyam sutra of Vedic mathematics. This proposed design is performed in XILINX 13.4 ISE version and implemented on vertex-5 FPGA. The sutras of Vedic mathematics are much more effective than customary mathematics. The Urdhava Tiryagbhyam sutra is faster than the customary method of multiplication. Thus, IIR filter based on Vedic sutra taking less average processing time as compared to conventional methods.

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