SANQ: A Simulation Framework for Architecting Noisy Intermediate-Scale Quantum Computing System

Gushu Li, Yufei Ding, and Yuan Xie
University of California, Santa Barbara, CA, 93106, USA
{gushuli,yufeiding,yuanxie}@ucsb.edu

Abstract—To bridge the gap between limited hardware access and the huge demand for experiments for Noisy Intermediate-Scale Quantum (NISQ) computing system study, a simulator which can capture the modeling of both the quantum processor and its classical control system to realize early-stage evaluation and design space exploration, is naturally invoked but still missing. This paper presents SANQ, a Simulation framework for Architecting NISQ computing system. SANQ consists of two components, 1) an optimized noisy quantum computing (QC) simulator with flexible error modeling accelerated by eliminating redundant computation, and 2) an architectural simulation infrastructure to construct behavior models for evaluating the control systems. SANQ is validated with existing NISQ quantum processor and control systems to ensure simulation accuracy. It can capture the variance on the QC device and simulate the processor and control systems. Several potential applications are proposed to show that SANQ could benefit the future design of NISQ compiler, architecture, etc.

I. INTRODUCTION

Quantum Computing (QC) has attracted great interest from both academia and industry during the last decades due to its strong potential in accelerating various important applications, e.g., integer factorization [1], database search [2], molecule simulation [3]. The second quantum revolution, transition from quantum theory to quantum engineering [4], is leading us towards Noisy Intermediate-Scale Quantum (NISQ) era [5], when QC devices have fewer than 1000 qubits and are not large enough to support Quantum Error Correction (QEC). To make good use of such NISQ devices which suffer from limited qubit lifetime and imperfect operations, more attention is given to NISQ system design and optimization in recent years, ranging across NISQ compiler [6–8], quantum control hardware architecture [9–11], NISQ device [12–15], etc.

Ideally, all these innovations should be evaluated on realistic NISQ hardware. However, NISQ devices require extreme execution environment and most of them still remain in physics laboratories. Existing QC cloud services, e.g., IBM Quantum Experience [16], Rigetti’s QPU [17], only provide limited access which can not satisfy the ever-increasing demand for experiments for evaluating new NISQ system designs. These restrictions are blocking more researchers from getting into this area.

Simulation can be a potential solution to this problem as NISQ system innovations can be proposed and evaluated without accessing realistic hardware. Since a complete NISQ system consists of two major components, the quantum processor and its classical control system, a simulator for NISQ systems needs to meet the following requirements:

1) Simulating a Noisy Quantum Processor. Quantum processors in NISQ era suffer from various noise effects. A simulator needs to be able to model the noises on realistic NISQ devices. The simulated output fidelity can help guide future NISQ system design.

2) Simulating a Classical Control System. The design of a control system can significantly affect the overall NISQ system performance, e.g., execution time. Such effects also influence the performance of the quantum processor. For example, longer execution time may exceed the qubit lifetime, which limits the size of a QC program that can be executed.

Unfortunately, such a simulator that can satisfy these requirements is still missing. Traditional architectural simulators, e.g., GEMS [18], GPGPU-Sim [19], are designed for classical digital computing without the ability to simulate QC. Existing QC simulators [20–32], no matter with or without noise effect considered, do not take the classical control system into consideration, lacking comprehensive modeling of a NISQ computing system.

In this paper, we propose a simulation framework, namely SANQ, for NISQ computing system design and evaluation. SANQ consists of one noisy QC simulator for the quantum processor, and one architectural simulation infrastructure to construct behavior models for the classical control system, leading to a comprehensive evaluation of NISQ systems and preparing for future design innovations. The noisy QC simulator in SANQ can adopt realistic error models and is accelerated by optimized Monte Carlo simulation. The architectural simulation infrastructure is specially designed for control system design. Users can construct a behavior model for a classical control system with provided common hardware modules or with customized newly designed hardware components. SANQ currently focuses on the execution fidelity and timing simulation, which are both critical in NISQ system evaluation, while it is extensible to accommodate more simulation, e.g., power, reliability.

To illustrate the design of SANQ, this paper demonstrates examples of how to adopt the noise model of a quantum processor and how to construct a control system based on the programming model and quantum processor interface requirement. SANQ is validated against real NISQ systems. Several
potential applications of SANQ are proposed with examples to show that SANQ can help with compiler and control system architectural design by providing early-stage evaluation and execution status analysis. The main contributions of this paper can be summarized as follows:

- We, for the first time, present a full system simulation infrastructure for comprehensive NISQ system modeling and early-stage evaluation.
- A noisy QC simulator is introduced with the ability to adopt the error model from realistic quantum processors. The proposed optimization can accelerate the error injection noisy simulation by $7 \times$ on average without affecting the final results, compared with the brute-force simulation strategy on industrial simulator under selected benchmarks.
- We propose a simulation infrastructure for control system design. A mini control system is constructed by adopting realistic control hardware design. Several key hardware modules are provided, and they can also be reconfigured or customized by users.
- The entire simulation framework has been validated against realistic NISQ systems, including one superconducting quantum processor from IBM and two control systems from both IBM and Delft UT. The noisy simulator can capture the variance on the QC device and the control system simulator can simulate the timing behavior precisely ($< 1\%$ and $10\%$ error for Delft and IBM’s control systems, respectively).
- We propose three applications of SANQ. 1) full system performance evaluation, 2) design space exploration, and 3) finding new optimization opportunities, to show that SANQ could benefit compiler optimization, control system design, etc. For example, our simulation suggests that increasing the number of Digital-to-Analog channels in the control system could provide at most $15\%$ execution time reduction.

The rest of this paper is organized as follows. We first introduce some background information about QC in Section II and then provide an overview of SANQ in Section III. The noisy QC simulator and its optimization are detailed in Section IV. An example of constructing a mini control system in our simulation infrastructure is given in Section V. We evaluate the QC simulation optimization and validate SANQ in Section VI. Several potential applications of SANQ are proposed in Section VII. Some limitations and future works are given in Section VIII. Related works are discussed in Section IX, and we finally conclude this paper in Section X.

II. BACKGROUND

In this section, we will present a brief review of relevant background knowledge to help understand the NISQ computing system. We first introduce the fundamentals in QC, followed by an overview of NISQ systems.

A. QC Basics

**Qubit.** Classical computing uses bits as the basic information unit with two deterministic states, ‘0’ and ‘1’, while QC employs qubits with basis states denoted as $|0\rangle$ and $|1\rangle$. The state of one qubit can be the linear combination of the two basis states, represented by $|\Psi\rangle = \alpha|0\rangle + \beta|1\rangle$, where $\alpha, \beta \in \mathbb{C}$ and $|\alpha|^2 + |\beta|^2 = 1$. Two or more qubits can be in a superposition of more basis states. For example, a two-qubit system can be in the state $|\Psi\rangle = \alpha_{00}|00\rangle + \alpha_{01}|01\rangle + \alpha_{10}|10\rangle + \alpha_{11}|11\rangle$ and represented by a four-dimensional complex vector $(\alpha_{00}, \alpha_{01}, \alpha_{10}, \alpha_{11})$. In general, a $2^N$-dimensional vector is required to describe the state of a system with $N$ qubits.

**Quantum Operation.** The state of a QC system can be manipulated by quantum operations. The first type is quantum gates, which are unitary operators applied on one or more qubits to change the state vector. The second type of operation is measurement operation, which will collapse the superposition state to the basis states with different probabilities based on the amplitudes in the state vector.

**Quantum Circuit and Computation.** Quantum circuit is a diagram to represent a quantum program in the well-adopted quantum circuit model [13]. Figure 2 shows an example of a quantum circuit and its computation. On the left is the quantum circuit which contains two qubits and two H gates (in the two squares). The initial state is $S_0 = |00\rangle$ and its state vector $(1, 0, 0, 0)$ is shown on the right. To compute the state $S_1$, the two $H$ gates are applied on $S_0$ and the result is $S_1 = \frac{1}{2} |00\rangle + \frac{1}{2} |01\rangle + \frac{1}{2} |10\rangle + \frac{1}{2} |11\rangle$. This process can be considered as a matrix-vector multiplication since the quantum system is linear and quantum gates are linear transformations. The applied matrix is determined by the Kronecker product of the applied quantum gates.

\[
S_0 = \begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix}, \quad S_1 = \frac{1}{2} |00\rangle + \frac{1}{2} |01\rangle + \frac{1}{2} |10\rangle + \frac{1}{2} |11\rangle
\]

B. NISQ System

Figure 1 shows a schematic NISQ computing system. On the left is a host machine, a classical computer which will interact
with users and control the QC system. Users provide QC programs and the QC compilers will convert these programs to the basic instructions which can be executed by the control system. The control system will further convert the instructions to control signals and send them to the quantum processor to implement different operations.

Quantum Processor. The quantum processor is the core of the NISQ computing system, which can be implemented by different underlying technologies, e.g., superconducting quantum circuit [34], ion trap [35], quantum dots [36]. The state of the qubits on the quantum processor is changed by external physical operations, e.g., micro-frequency electronic signals [37], lasers [38]. For the lack of QEC, the qubits are also affected by various noise effects [33]. Unlike classical processors which work on digital signals, quantum processors are manipulated by analog signals.

Classical Control System. A classical control system lies between the host machine and the quantum processor [39]. It converts post-compilation instructions into control pulse signals to control the quantum processor. The measurement results in analog form are also received from the quantum processor and converted to a digital form. Such a classical control system provides a digital interface for the quantum processor and makes the NISQ system a co-processor of the host machine.

III. Simulator Overview

In this section, we will provide an overview of SANQ, a simulation framework that contains a noisy QC simulator and a classical control system simulation infrastructure to cover the entire NISQ computing system. Both components are validated against realistic NISQ systems from IBM and Delft UT to guarantee the effectiveness of the simulation outcome. The workflow of SANQ is illustrated in Figure 3.

Input. The input required by SANQ has three components, a post-compilation QC program, an error model, and a control system design. The instructions in the post-compilation QC program must be executable on the simulated hardware, which means all the quantum operations have been decomposed into hardware supported operations via compilation. The rest two components are about the simulated NISQ system. An error model should be provided to describe error operator, error position, and error probability on the simulated noisy quantum processor. Users can define customized error model via the provided interface. More accurate error model can come from the vendor or be characterized by physical experiments. The hardware design of the control system is about the model of each hardware module in the simulated control system. Users need to specify the output of each module under all possible input and how these modules are connected. By default, SANQ is pre-configured to be the baseline system model in the rest of this paper. The input used in this paper for the baseline error model and control system design is provided for user reference.

Simulation. With the required input information, the two simulation components in SANQ can provide comprehensive modeling of an entire NISQ system. The noisy QC simulator uses the error information to construct an error model and generate error injection traces for the follow-up Monte Carlo (MC) simulation. The generated error injection traces will first be analyzed and reordered to eliminate redundant computation. Then SANQ will perform functional QC simulation for all the error injection traces and average the results, to obtain an output distribution and evaluate the fidelity. On the other hand, the control system simulation infrastructure in SANQ will use the provided hardware design to generate a behavior model for the simulated control system. Traditional architectural simulation is then performed to model how the control system will execute each instruction of the input QC program and control the quantum processor. Important information like the total execution time for a quantum program and the control hardware resource utilization rate can be simulated to evaluate the overall system performance.

Output. The output from SANQ will demonstrate key execution information of the simulated NISQ system. The noisy QC simulator will provide the final output distribution in the MC simulation. By comparing this result with error-free execution, SANQ can evaluate the fidelity for one QC program execution on the simulated quantum processor. The control system simulation will then provide detailed timing information for one execution. More information like the occupation for each hardware component can also be collected to help locate the bottleneck in the simulated control system.

This section provides an overview of SANQ. In the next two sections, we will introduce the two simulation components in detail with examples of how SANQ could simulate an existing NISQ system. In Section IV, we illustrate how to configure the error model based on IBM’s public quantum processor information and how to accelerate the noisy QC simulation by eliminating redundant computations. In Section V, we will construct a mini control system in SANQ based on real control systems.

IV. Noisy Simulation & Optimization

In this section, we will illustrate how users can define an error model based on error information of a realistic device, followed by the optimization in our noisy simulator. Quantum processors in the NISQ era are affected by noise effects. A noisy QC simulator is designed and employed to capture the behavior of noisy quantum processors in SANQ. In general, simulation QC on a classical machine is a hard problem. Our noisy simulator can scale up to 20 qubits, which is the
A. Error Model Construction

We use the error information from IBM’s Yorktown 5-qubit superconducting quantum chip to construct an error model for the noisy QC simulation [16]. Figure 4 shows the error rate data of IBM Yorktown chip. Note that this information will change over time and we only sampled the results from one characterization. On the left is the qubit coupling graph. Each vertex represents a qubit and each edge in the graph means that a two-qubit Control-NOT (CX) gate can be applied between the two connected qubits. The error rates for a CX gate applied on all edges are labeled. On the right is a table showing the error rate of single-qubit gates and measurement operations for each qubit. We will use this error rate data to construct an error model with error operator, error position, and error probability.

1) Error Operator: Error operators are some special operators that will be randomly injected in the quantum circuit in order to model the noise effect in the QC program execution on noisy quantum hardware. By default, SANQ provides the basic Pauli error operators. The three Pauli matrices, \(X\), \(Y\), and \(Z\) (given in Equation 1), are basic error operators that can describe three types of errors, a bit flip error \((X)\), a phase flip error \((Z)\), and an error in which both a bit flip and a phase flip occur \((Y)\).

\[
X = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, Y = \begin{bmatrix} 0 & -i \\ i & 0 \end{bmatrix}, Z = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}
\]

(1)

Alternatively, SANQ also supports customized error operators. Users can either define their customized set of error operators as a linear combination of these three operators, or directly specify their matrix representation.

The error information data from IBM do not specify the error operators. As a result, we apply these three default Pauli matrices as the basic error operators.

2) Error Position: Error positions are the places where an error could possibly be injected in the simulated quantum circuit. Errors can be injected after a gate or measurement if triggered by operations. Some other errors like decaying from high-energy state \(|1\rangle\) to low-energy state \(|0\rangle\) or interacting with the environment can happen without an operation. Such an error could appear at any place across the quantum circuit.

The error information from IBM is all about operation errors. So that the constructed error model will only inject error operators after quantum gates or measurement operation.

3) Error Probability: After the error operators and positions are determined, we still need to know the probability for each error position with each error operator. Each time when we meet an error position during the simulation, we will randomly inject one error operator based on the error probability for each operator at this position. IBM data have specified the error probability at each error position. For example, an error will be injected after a single-qubit gate with a probability of 1.37 \(\times\) \(10^{-3}\) if this gate is applied on \(Q_0\).

The error model construction has almost finished while a few more assumptions are still required. First, the error probability is determined for each error occurrence but the error operator is not specified. For this question, we assume the error comes from a depolarization error channel, an important type of noise which converts a qubit to a completely mixed state with a small probability [33]. This error channel is widely used to model gate errors [26], [32] and suggested by IBM [32]. On the left of Figure 5 is the probability distribution of each error operator under depolarization channel. An error operator \(E\) can be one of \(X\), \(Y\), and \(Z\) with the same probability \(p\). Or it will become an identity operator \(I\) with the probability \(1 - 3p\), which means no error is injected in this position.

B. Noisy QC Simulator Optimization

The proposed noisy QC simulator is optimized to exploit the computation redundancy among different error injection executions in the noisy QC simulation. In this section, we will start from a motivating example to show the redundancy...
in the MC simulation. Then we will show how to manage the executions to reduce the computation amount.

1) A Motivating Example: Figure 6 shows a motivating example to demonstrate the computation redundancy. There are totally four error injection executions in this example, represented by four quantum circuits. The first one in (a) is the original error-free execution. \( S_1 \) and \( S_2 \) are two intermediate states during the error-free execution. The other three in (b) (labeled with 1, 2, and 3) are error injected executions. Each of them has one error operator occurred, represented by gate \( E_{1,2,3} \). To run the noisy QC simulation, all these four quantum circuits will be simulated and then averaged to obtain a distribution of the final output. We can find that all the four quantum circuits are exactly the same before reaching \( S_1 \) state. The state vector of \( S_1 \) is the same for all four execution since no errors are injected before \( S_1 \). As a result, the computation from the initial state to \( S_1 \) can be shared by all four executions. The state vector at \( S_1 \) only needs to be calculated and stored in one execution. The rest three executions can start from the stored \( S_1 \) state instead of starting from the beginning. Such redundancy exists at multiple locations across the error injection MC executions. For example, the state vector at \( S_2 \) can also be shared by the error-free execution and the first two error injected executions 1,2.

The motivating example above has shown computation redundancy among MC executions. We can store some state vectors when we first reach such states and the results will be reused in the following executions. However, the maximal number of state vectors we can store is limited since one state vector has \( 2^n \) amplitudes (\( n \) is the number of qubits). Although several techniques have been proposed to store the state vector in a compressed form [23], [24], the memory requirement will still grow exponentially as the number of qubits increases. To allow circuits with more intermediate states to be simulated efficiently, we introduce an execution reorder technique to reduce the number of concurrently maintained state vectors without loss of the benefit from the computation redundancy elimination.

2) Execution Reorder: Different execution order can significantly affect the number of states that need to be stored. For the example in Figure 6 (b), 1,2,3 is an inefficient MC execution order. When running 1, both the states \( S_1 \) and \( S_2 \) need to be stored so that 2 can start from \( S_2 \) and 3 can start from \( S_1 \). An optimized execution order for this example can be 3,2,1. When executing 3, we only need to store state \( S_1 \). The execution of 2 can directly start from the stored \( S_1 \) and then \( S_1 \) can be dropped since it is no longer used in the follow-up executions. During the execution of 2, \( S_2 \) will be stored and finally used when executing 3. Consequently, only one state vector needs to be stored during the entire simulation process. An optimized execution order reduced 50% of memory requirement (from two state vectors to one state vector) compared with a straight-forward order in this example.

In our noisy QC simulator, we first generate the MC execution traces without actually running the simulation. The simulated quantum circuit is divided into layers, in which any two quantum operations are not applied on the same qubit. Error operators will only be injected at the end of each layer (shown in Figure 5). One execution trace will record the location and operator of each injected error. These traces will be ordered by the location of the first injected error. The traces with the first error injected in the first layer (e.g., 3 in Figure 6) will appear at the beginning of the execution order, followed by those traces with the first error injected in the second layer (e.g., 2 in Figure 6), and so on.

After the ordering procedure above, we begin our simulation by executing the first layer of the circuit with no error injected and store the state as \( S_1 \). This part of computation can be shared by all MC traces. Then we will execute all the traces with errors first injected in the first layer. If two or more error traces share the same first error (injected on the same qubit with the same error operator), these traces will be grouped. The simulation for these traces can be optimized recurrently if we consider \( S_1 \) as the initial state and let the remaining circuit after the first layer be the simulated circuit. After finishing the traces with first error in the first layer, we can execute one more layer without error and store the new state as \( S_2 \). Now \( S_1 \) can be dropped as no executions remaining will rely on it. Additional memory space is only required when recurrent reordering happens because these traces with shared first error operator need the state vector after the shared error to help eliminate the computation redundancy among them. The maximal number of state vectors we need to store is the recursion depth, which is small because the probability for two independent randomly generated traces to have \( m \) shared error operators decreases exponentially as \( m \) increases.

The proposed noisy QC simulator will divide the input circuit into layers based on the error model and apply the optimized MC simulation. The final result is not changed since the simulated error-injected circuits are not changed and we just reuse computation across the MC simulation trials.

V. CONTROL SYSTEM DESIGN

Compared with conventional experiment instruments, integrated control system for QC is becoming more and more popular due to the demand for supporting larger scale QC systems [10]. To build an architectural simulator for the QC control system, we investigated existing control systems
A. Assumptions

Although programming and compilation should be done on the host machine and are not simulated in SANQ, some assumptions need to be made for them before we can continue to construct the architecture of a classical control system. For the quantum processor, our assumption is only about the interface with the control system and does not affect the error models in the noisy simulation.

1) Programming Model and Compiler: This mini control system accepts OpenQASM [43], the interface language of IBM’s QC cloud service designed for small depth quantum circuits, as the ISA. OpenQASM is selected due to its rich benchmark resource and compiler support. Quantum programs can be developed in high-level languages like Scaffold [49], Quipper [50], or Q# [51], and then compiled to flattened OpenQASM format instructions. However, some OpenQASM instructions are not executable so that we add some constraints for the program used in our mini control system. There are only 5 types of instructions from OpenQASM remaining after compilation (the first 5 types in Figure 7). In addition, we add one ‘Wait’ instruction, which is critical in realistic control systems [10] [47], to enable more flexible timing control. Our control system will support this 6 types of instructions. For simplicity, the conditional instruction in the original OpenQASM standard is slightly modified and we only support one instruction in the branch based on one bit comparison result. The quantum operations in the post-compilation instructions are in the Quantum ISA (QISA) of the target quantum processor, which means the control signals for these operations are prepared and available. A conditional instruction in OpenQASM is also included and will be managed inside the control system. All the hardware constraints, e.g. the limited physical two-qubit gate availability, have been addressed during compilation optimization and the generated quantum program is completely hardware compatible. All the post-compilation instructions have been pre-uploaded to an instruction memory in the control system. There is no communication between the host machine and the control system during the quantum program execution.

2) Quantum Processor: The quantum processor is assumed to be based on superconducting quantum circuit technolo-

designs [10], [39], [41]–[47]. The default control system model provided in SANQ, the mini control system, is constructed through abstracting the key components in real control systems.

In the rest of this section, we start from discussing the assumptions on the programming model, compiler, and quantum processor, because they will affect the interface of the control system. Then we will introduce the hardware design and the behavior model of the mini control system. This part and the noisy simulator in the last section make SANQ a full NISQ system simulator. Different from the full state QC simulator, this architectural control system simulator does not have a scalability issue. If users do not need to simulate the output distribution, this part also can be used individually and simulate the control of a large-scale QC system.

B. Hardware Design

With the assumptions above, users can specify the hardware design of the control system. For each hardware module, users need to determine what internal states the hardware module should maintain, and the output under all possible inputs. Moreover, users need to specify how the input and output ports of the hardware modules are connected in the hardware design.

As an example, a mini control system consisting of a control unit, a Digital-to-Analog (DA) interface, and an Analog-to-Digital (AD) interface, is shown in Figure 8. The hardware modules in the control unit are introduced as follows:

- **Instruction Memory.** This memory stores all the instructions. Since there is no existing binary encoding standard for OpenQASM [53], we assume that each instruction consumes 32 bits (encoding shown in Figure 7). The input for this module is a memory address from Program Counter and the output is the instruction on that address which will be sent to a Decoder.
- **Program Counter.** The Program Counter (PC) records the address of the next instruction. It will automatically increase after one instruction is issued by the scheduler. It can also accept new address under conditional instructions.
- **Measurement Register.** The measurement register stores the measurement results from the measurement unit. The comparator can read the measurement register.
- **Decoder & Comparator.** The decoder will decode those instructions in binary form fetched from the instruction memory. If it is a conditional instruction, the decoder will ask the comparator to read the measurement registers, do the comparison to determine the address of the next instruction. If an instruction needs to be applied on the quantum processor, the decoder will send the operation information to the scheduler.
- **Scheduler.** The scheduler will decide which signal channel(s) will be used to apply an operation and send the operation to the instructions queue(s) of the signal channel(s). The operation dispatch policy is to find the signal channel(s) that can finish all the jobs in the queue(s) at the earliest time. The instructions are dispatched in order.
**Interface Design.** The Mini Control System adopted the interface design from Quantum Control Box (QCB) [10], which is briefly introduced as follows. For the DA interface, we employ three DA signal channels, the minimum requirement to implement two-qubit gates. Each channel has an instruction queue as a temporary buffer for the instructions. The waveform is implemented by a Pulse Look-Up-Table (LUT), which can directly fetch stored pulse data, and we assume that all the pulse waveform data are already in the LUT. A Digital-Analog-Converter (DAC) follows the Pulse LUT to generate analog signals. For the AD interface, one AD channel will receive an analog signal from the quantum processor and convert it to digital form by an Analog-Digital-Converter (ADC). The Measurement Unit will perform a weighted integration over the signal and then compare the results with a threshold value to determine whether the measurement result is 0 or 1. All the channels in the AD/DA interface can connect to different qubits via switches.

**C. Behavior Model Generation**

After the hardware design is specified, SANQ will generate a behavior model for the simulated control system. A behavior model is about how the hardware will execute the given instructions. In our mini control system example, only 5 types of basic instructions in OpenQASM standard [48] and the additional ‘Wait’ instruction in Figure 7 will appear after being compiled and flattened. The execution for these 6 types of instructions in the mini control system is listed here.

1) \( U(\theta, \phi, \lambda) \). \( U(\theta, \phi, \lambda) \) is a parameterized single-qubit gate. The decoder will send the instruction information to the scheduler and the scheduler will select one signal channel and put the instruction in the instruction queue. When this instruction is popped out, its control pulse will be fetched from the Pulse LUT, converted to an analog signal through DAC, and sent to the target qubit.

2) \( CX \). \( CX \) is Control-NOT, the only supported two-qubit gate. Different from single-qubit gates, the scheduler needs to select three signal channels to complete this operation.

3) \( Measure \). Measure is the measurement operation. The scheduler needs to choose one DA channel to send a special pulse and one AD channel will receive a feedback pulse. The Measurement Unit will determine the output and write the result to the Measurement Register.

4) \( Reset \). Reset is a single-qubit operation that reset the qubit to \( |0\rangle \) state. In this mini control system, Reset is implemented by passive reset, which waits for \( 5 \times T_1 \) coherence time to let the qubit decay to \( |0\rangle \) state.

5) \( If \). This is a conditional instruction. The decoder will ask the comparator to read the measurement register, do the comparison to determine the address of the next instruction. If the condition is not satisfied, the next instruction will be ignored.

6) \( Wait \). The control system will wait for a specific number of cycles before executing the next instruction.

**D. Architectural Simulation**

After the behavior model is established, SANQ will simulate the control system by executing the provided post-compilation instructions. The post-compilation instructions are put into the **Instruction Memory** first and PC is set to be the address of the first instruction. Then, the configured NISQ control system will be simulated.

Besides simulating the execution time, SANQ can also actively collect and record the states of all the hardware modules, e.g., the number of instructions in each instruction queue, the number of instructions executed, etc. These statistical data can help locate the bottleneck in the system design. An example will be given in Section VII.

**VI. Evaluation**

In this section, we first evaluate the speed-up and memory consumption of the optimized noisy simulation. Then we validate our simulator against real NISQ computing systems.

**A. Evaluating the Optimization in Noisy Simulation**

To evaluate the proposed optimization in the noisy simulation, we implemented a full state QC simulator with Python 3.4. The numerical noisy QC simulator is developed with Numpy 1.15. All the experiments are executed on a server with Intel Xeon E5-2680 CPU. The operating system is CentOS 7.5 with kernel version 3.10.

1) **Experiment Configuration: Baseline.** The baseline noise simulation strategy is from Rigetti’s QVM [40], which repeats error injection simulation many times to generate an output distribution.

**Metric.** In order to perform a fair evaluation of our noisy simulator optimization, the metrics in this section are chosen to be independent of implementation and platform. For the computation time, we use the number of basic operations (matrix-vector multiplication) in full state QC simulation to indicate the computation amount. For the memory consumption, we use the number of Maintained State Vectors (MSVs) during the noisy simulation since the memory space for the state vectors, which will grow exponentially as the number qubits increases, dominates the memory consumption.

**Benchmarks.** Table II shows the 12 quantum programs used in this experiment. They are collected from IBM OpenQASM benchmarks and prior work [8]. These benchmarks include Bernstein-Vazirani algorithm (bv) [54], Quantum Fourier Transform (qft) [33], Quantum Volume (qv) [55], Grover algorithm [2], Randomized Benchmarking (rb) [56], Modular...
Multiplication \((7x1\mod 15)\) [32], and W-state [57]. The four columns on the right in Table I show the number of qubits and instructions in the post-compilation programs for each benchmark. The selected programs have 5 or fewer qubits to be simulated on the IBM 5-qubit chip model (illustrated by Figure 4) and do not contain \textit{Reset} instructions. The measurement instructions only appear at the end of each program so that there are no conditional instructions. All the benchmarks only have \(U(\theta, \phi, \lambda), CX,\) and \textit{Measure} instructions after compilation.

### Table I: Benchmark Characteristics

| Name   | Qubit # | U # | CX # | Measure # |
|--------|---------|-----|------|-----------|
| rb     | 2       | 9   | 2    | 2         |
| grover | 3       | 87  | 25   | 3         |
| wstate | 3       | 21  | 9    | 3         |
| 7x1mod15 | 4       | 17  | 9    | 4         |
| bv4    | 4       | 8   | 3    | 3         |
| bv5    | 5       | 10  | 4    | 4         |
| qft4   | 4       | 42  | 15   | 4         |
| qf5    | 5       | 83  | 26   | 5         |
| qv_n5d2 | 5       | 44  | 12   | 5         |
| qv_n5d3 | 5       | 74  | 21   | 5         |
| qv_n5d4 | 5       | 100 | 30   | 5         |
| qv_n5d5 | 5       | 130 | 36   | 5         |

**Compiler.** Quantum algorithms are usually developed for ideal device model while the allowed two-qubit gates are restricted by the available physical-qubit connections on the hardware model (shown in Figure 4). Prior works have discussed how to overcome this problem by qubit allocation and remapping during compiler optimization [5], [8]. In this paper, We choose the Enfield project [58], which provides a dynamic programming based optimal qubit mapping in terms of gate count on IBM’s 5-qubit devices [8], as the compiler to generate hardware compatible quantum programs.

**Experiment Method.** We run different numbers of trials (from 1024 to 8192) of the selected 12 benchmarks. The errors are injected based on the error model in Section IV. Then we will compare the computation amount between the baseline and our optimized noisy simulation. The effect on memory consumption of our reordering scheme is studied by comparing the number of MSVs with or without reordering the executions.

2) Results: Our optimization modifies the simulation process to reduce runtime but does not affect the final output. Figure 9 shows the computation saving for all benchmarks and different numbers of trials. The proposed optimization can save about 85% of computation on average. In the worst case when the benchmark is large (‘qv_n5d5’), the computation amount saving still achieves 57% with 8192 trials. We can also find that the more trials we execute, the more computation we will save because more overlapped computation can be identified.

Figure 10 shows the memory saving in experiments with 1024 trials and this result does not significantly change when the number of trials increases from 1024 to 8192. The number of MSVs is 3 for the smallest benchmark ‘rb’ and only 6 in the largest benchmarks ‘qft5’ and ‘qv_n5d5’. As discussed in Section IV the number of MSVs will grow slowly since the probability for two trials to share the same \(m\) injected errors decays exponentially with \(m\). As a result, the memory saving ratio will increase as the benchmark size increases. For the small benchmark ‘bv4’, about 43% memory is saved. While for the largest benchmark ‘qv_n5d5’, our execution reordering technique can save about 92% memory for MSVs.

**B. Simulator Validation.** In this section, both components in SANQ are validated against realistic systems. Due to the noise in the state-of-the-art NISQ systems, the output distribution of some benchmarks used in the last section will be hidden in noise and those benchmarks cannot be directly applied during validation experiments. In the validation experiments, we carefully select validation methods, which will be explained later in this section, based on the capability of real QC systems.

1) Noisy QC Simulator Validation: We validate the noisy simulator against IBM’s Yorktown 5-qubit chip (shown in Figure 4) and the error model is constructed in Section IV-A

**Validation Methodology.** Different from testing a classical digital device, a quantum processor has its unique benchmarking methodology. In experimental physics, Randomized Benchmarking (RB) [56] is applied to each individual physical qubit and each connected physical qubit pairs. Such benchmarking method is widely accepted [59], [60] and the error data in Figure 4 is also from RB experiments run by IBM. Since our noisy simulator is targeting realistic devices, the validation experiments are designed based on the device calibration methodology. We select the two-qubit Bell State program consisting of single-qubit gates, two-qubit gates, and measurement. We test it on all connected physical qubit pairs. The experiment was repeated in 1024 trials and the output distributions are compared.

**Results.** Figure 11 shows the final output distributions of realistic execution results from IBM’s real chip in blue, and the simulation results are shown in orange. The expected error-free output distribution in this experiment is \((0.5, 0, 0, 0.5)\), but the noise effect will make the output distribution slightly different. For example, the output distribution for this experiment on \((Q_1, Q_2)\) qubit pair is about...
The simulation result for \((Q_1, Q_2)\) qubit pair is about \((0.42, 0.06, 0.07, 0.43)\), which is much close to the realistic execution compared with the error-free result. Among all the six experiments, the \((Q_0, Q_1)\) qubit pair has about 30% lower error rate compared with other qubit pairs. The single-qubit error rate and measurement error rate on these two qubits are not significantly worse than others. So the output of the experiment on \((Q_0, Q_2)\) on both the realistic quantum processor and our simulator show a distribution closer to the expected output compared with experiments on other qubit pairs. Our simulator is able to capture the variation among different qubit connections by adopting the error rate information of a realistic quantum processor.

2) Control System Simulator Validation: Validation Against Delft UT’s Control System. To validate our simulator against QCB [10]. The clock frequency is set to be 200 MHz. Other key parameters are shown in Table I. The latency of single-qubit gates, two-qubit gates, and measurement operations are assumed to be 20\(ns\), 40\(ns\), and 300\(ns\), respectively.

To validate our simulator against QCB, we run the AllXY program[4] the original testing experiment for QCB [10]. The AllXY test program has 21 iterations and in each iteration, two single-qubit gates are applied to one qubit followed by a measurement operation. Figure 12 shows the code for one iteration (U1 and U2 represent different single-qubit gates in different iterations) and the execution time on QCB and SANQ. Our simulator could simulate the timing behavior of QCB with very low error (<1%) and the small error becomes negligible as the number of iterations increases.

Valiation Against IBM’s Control System. IBM’s experimental control system model is different from the baseline. The latency for single-qubit and two-qubit gates are 50\(ns\) and 300\(ns\), respectively, with 2 DA channels and 2 AD channels. The test program is Active Reset as shown in Figure 13 on the left. We first send measurement pulse to a qubit and then wait for 60 cycles for cavity emptying (required by IBM’s device). If the measurement result is \(|1⟩\), we apply a bit flip operation. This procedure is repeated for 3 times to guarantee a high reset fidelity. The execution time of IBM’s real control system and the simulation results are in Figure 13 on the right. The simulated execution time is close to that of IBM’s real system. There exists a constant error (about 130\(ns\)) which comes from the warm-up phase of the control system because such procedure before issuing the first instruction is not yet simulated in SANQ. In summary, the average error ratio is 10% and such error can be mitigated if we take the communication between the host machine and the control system into consideration, which will be addressed in our future work.

Generality. Our simulation capability is not limited to QCB. We compared the control system design for the superconducting quantum circuit from major vendors, including IBM [47], Google [45], Rigetti [46], and Delft UT [10]. The control system architectures of them are similar, which suggests that our default design is representative. This architecture is also proved to be scalable and stable because Google is using a similar one [45], [61] to control its 72-qubit chip by adding more hardware resources without changing the overall architecture.

For details about AllXY program, please refer the QCB paper [10].

### Table II: Baseline Control System Model

|                        | Single-qubit Gate | Two-qubit Gate |
|------------------------|-------------------|----------------|
| Channel                | 1                 | 3              |
| DA Channel #           | 3                 |                |
| AD Channel #           | 1                 |                |
| Measurement            | Latency 300\(ns\), 1 AD Channel and 1 DA Channel |

VII. Future Applications

In this section, we propose three future applications of SANQ that are not available on existing QC simulators. First, SANQ can perform a comprehensive system performance evaluation by simulating both the quantum processor and the control system. Second, SANQ can perform design space exploration for the control system to guide future control hardware architecture design. Third, by monitoring the utilization of the hardware components, SANQ can help locate new optimization opportunities to improve NISQ system design.
The rest of this section will provide three examples to illustrate the applications of SANQ in detail.

**Baseline Configuration.** The baseline quantum processor model in this section is from the IBM 5-qubit Chip [16] and generated in Section [V]. The control system model is the QCB validated in Section [VI] with key parameters shown in Table [I]. The baseline compiler remains the same with Section [VI] and the benchmarks used are in Table [I].

### A. System Performance Evaluation

We demonstrate the ability to perform a comprehensive system performance evaluation by comparing two different QC compiler optimization approaches on the qubit mapping problem. One is the dynamic programming approach (DYN) in Enfield, the baseline compiler [8]. The other one is a heuristic approach for efficient qubit mapping (EFF) [6].

**Experiment Design.** We compile the 12 benchmarks with the two compilers mentioned above. Then we simulate the execution fidelity and time, from the noise QC simulator and the architectural control system simulator, respectively. Since some benchmarks are large and the correct output will be hidden by the noise on IBM’s 5-qubit device [60], the term ‘execution fidelity’ used in this section is the ratio of error-free trial count over total trial count. Both the quantum processor model and control system model used in compilation and simulation are the baseline models.

**Results.** Figure 14 shows that the execution fidelity and time (with and without measurement operations included) of EFF normalized to the results of DYN. For two small benchmarks ‘rb’ and ‘wstate’, EFF and DYN generate the same code and the simulation results are the same for them. In general, DYN is well optimized for CX gates and the execution fidelity is about 35% better than that of EFF on average. However, EFF also considered parallelism optimization. For the ‘qv’ benchmarks, the execution time is shorter for EFF even when the execution fidelity is still worse than EFF. For the ‘bv4’ and ‘bv5’ benchmarks, they are small and the dominant factor in execution time is the CX gates so that EFF is much worse than DYN. The original evaluation in the EFF and DYN papers [6], [8] was based on the coarse-grained gate count and circuit depth metric in the generated program. SANQ generates consistent results to verify the optimality of DYN and the parallelism optimization in EFF. Moreover, SANQ could perform fine-grained fidelity and execution time evaluation, preparing for deeper compiler optimization.

![Fig. 14: Normalized Simulation Result of EFF](image)

### B. Design Space Exploration

By simulating the classical control system, SANQ is able to perform design space exploration to help guide the control system design. This example focuses on the number of DA channels, which places an upper bound on the instruction parallelism. For a quantum processor, instructions applied on different qubits can be executed in parallel theoretically. However, the number of DA channels to send the control pulses is limited in a realistic control system. The baseline employs three DA channels (the same with QCB configuration [10]), which can support at most three simultaneous single-qubit operations or one two-qubit operation. In this study, we investigate how the number of DA channels can affect the overall performance of a NISQ computing system.

**Experiment Design.** We vary the number of DA channels from three to eleven and simulate the execution time. All other configurations remain the same. In the end, we assume that there are infinite DA channels to remove this constraint. This will show the ultimate limit if we continue to increase the number of DA channels.

**Results.** Figure 15 shows the execution time with various numbers of DA channels. The results shown in the upper half include the measurement instructions. All the benchmarks can benefit from more DA channels, except ‘rb’, which only has two qubits and is not constrained by the number of DA channels. Larger size benchmarks can save more execution time than small size benchmarks. When there are eleven DA channels, most benchmarks have been close to the upper bound with infinite DA channels, which is about 15% on average since the execution is also limited by other effects, such as instruction dependencies.

Our simulation shows that the execution time of measurement instructions is the major limitation in this case study. For all the experiments, the number of AD channels is always one which means that all the measurement instructions must be executed sequentially. Moreover, the size of the selected benchmarks is small but the latency of measurement instruction is much longer than other operations in our quantum processor model (300ns vs. 20 ~ 40ns). Fortunately, all the measurement operations are at the end of each benchmark and we can calculate the execution time before the measurement. The execution comparison without the measurement instructions is provided in the lower half of Figure[15] and the average execution time-saving limit can achieve about 36%.

### C. Finding New Optimization Opportunity

The third example will show that SANQ can suggest new optimization opportunities in NISQ system design by analyzing the execution status and locating the bottlenecks. For this example, we monitor the utilization rate of the DA channels in the system performance evaluation experiments (in Section [VII-A]). Figure 16 shows one bottleneck found in our experiments. On the left are the first five instructions in ‘bv4’ benchmark. In this case, SANQ finds that from 0ns to 20ns, the number of instructions that is being executed is three and the DA channel utilization rate is 100%. But starting from 20ns to 60ns, only one instruction is being executed and the utilization rate is just 33.3%. The reason for this situation is discovered after looking into the execution details (shown in the middle of Figure [16]). From 0ns to 20ns, the first three
instructions are executed in parallel. The fourth instruction cannot be executed due to the DA channel constraint. But from 20\textit{ns} to 60\textit{ns}, only two instructions are executed because all the following instructions involve \textit{q}_3 and cannot be executed before the fifth instruction. As a result, the utilization rate of DA channels is only 33\% from 20\textit{ns} to 60\textit{ns}.

For example, all errors are generated independently in our Monte Carlo simulation while error correlation actually exists and is being studied by physicists \cite{62, 63}. Deeper understanding of the mechanisms on the target QC platform will lead to more precise noise models.

**Advanced Quantum Control Architecture.** The baseline control system is implemented with OpenQASM \cite{48}, a widely used intermediate representation for NISQ computing process. This interface language is designed for small depth quantum circuit experiments on IBM’s QC cloud service and lacks several important features for a control system ISA, e.g., efficient encoding, flexibility for quantum optimal control \cite{64, 65}. For further research, SANQ will adopt more advanced quantum control architectures, such as eQASM \cite{11}.

**Cooperating with Host Machine.** SANQ assumes that all the post-compilation instructions have been transferred to the control unit and does not include the communication between the host machine and the QC subsystem. The assumption brings error in the simulation as discussed in Section VI-B2. In the future, SANQ can be integrated as a sub-module into an existing computer system simulator, e.g., GEM5 \cite{18}, to include the modeling of the host machine and its cooperation with QC subsystem.

**IX. RELATED WORK**

**QC Simulator Optimization.** Previous optimizations for QC simulators can be summarized into two categories. Some simulators increase the simulation capability from algorithm-level \cite{20–25, 66}. These works exploited sparsity or redundancy inside a single QC simulation process while the proposed optimization leverages the redundancy among multiple MC simulation executions. The other type of optimizations is from computer system level, including vector instructions \cite{26, 27}, specialized linear algebra library \cite{28}, multi-thread \cite{26, 27, 29}, distributed system \cite{27–29}, GPU \cite{30, 31}. Our acceleration is from algorithm-level and is compatible with these system-level approaches.

**Noisy QC Simulator.** Several existing QC simulators have supported error modeling and noisy simulation, e.g., IBM QISKit \cite{32}, QX \cite{26}, Rigetti QVM \cite{17}, ‘quantumsim’ \cite{30, 67}. These simulators above can be used to model a realistic quantum processor while none of them is capable of evaluating an entire QC sub-system since the effect of classical control components is not considered.

**Classical Control System Design.** The electronic interface for quantum processors has been studied for small size
cases [39, 41–44]. Fu et al. proposed QuMA, a microarchi-
tecture, with accurate timing control, fast feedback control, etc. for a superconducting quantum processor [10]. Dijk et al. proposed SPINE, a toolset with a circuit simulator, for co-simulation of the electrical circuit and a spin-qubit-based quantum processor [68]. To the best of our knowledge, this work proposes the first architectural level simulation framework for early-stage evaluation of an entire NISQ system.

X. Conclusion

This paper presents SANQ, a simulation framework for architecting NISQ computing systems. SANQ consists of two components, an optimized noisy QC simulator and an architectural simulation infrastructure for the classical control system. The noisy QC simulator is equipped with flexible error modeling and optimized by computation redundancy elimination. The architectural simulation infrastructure can construct behaviour models and evaluate control systems design decisions. The usage of SANQ is illustrated by adopting realistic error model and published control system design. Three examples are given to show that SANQ could benefit NISQ system design through comprehensive system evaluation and execution status analysis. In conclusion, this paper proposes the first NISQ system simulator, allowing more researchers to participate in QC research and perform the early-stage evaluations for future innovations.

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