Reversible Gate Mapping into QCA Explicit Cells Packed with Single Layer

N Pathak¹, N K Misra²*, B K Bhoi³, S Kumar⁴

¹,⁴Department of Computer Science and Engineering, Maharishi University of Information Technology, Lucknow, Uttar Pradesh 226013, India
²*Department of Electronics and Communication Engineering, Bharat Institute of Engineering and Technology, Hyderabad, Telangana, India
³Department of Electronics and Telecommunication, Veer Surendra Sai University of Technology, Burla 768018, India

Email Id: ²neeraj.mishra3@gmail.com

Abstract. MOS based circuits and computing devices are facing challenge related to energy dissipation, short channel effect and device density. The state of the art technology is driven towards Quantum cellular automata (QCA) computing with an emphasis on a high-speed and smaller area. QCA is a new computing technology that is made of quantum cell restraining two electrons and two dots. In this paper, a novel design of Fredkin, Toffoli, and Feynman gate layout is designed using the molecular QCA concept. Presented cell layout of newly circuit validity is verified by QCADesigner software. Further, a large number of articles are reviewed and comparison results are presented to show the optimal results such as cell count, majority gate count, bounded box area, and clock utilize. In this work, QCA and reversible logic combined together and the proposed designs have less bounded box area and delay, which is an essential part of the next-generation computing.

Keywords: Reversible Logic, QCA nanocomputing, Molecular QCA, Low power design

1. Introduction

According to Moore’s law, the chip design industry has evolved spectacularly. Eventually, the chip size has been minimized to nanoscale and the processing speed has been increased immensely [1]. Now for the engineers, it is the trade-off between power dissipation and increased processing speed. To minimize the power dissipation different technologies are available like charge based recovery [2]. By going beyond conventional method energy dissipation can be minimized. For this reversible logic can be used as a solution. Rolf Landauer [3] manifested for a one-bit of digital logic signal during data erasing KTln2 joules of energy is dissipated. During computation in irreversible logic, some information are being erased so as to avoid its reversible logic circuits are used. Bennet demonstrated by using reversible logic circuit zero power dissipation can be possible [4]. A logic binary gates are known as reversible if its equal input and output in numbers an input to output mapping is Bijective [5]. Because of this property, no information loss occurs in the reversible circuit. The reversible circuit must have minimum garbage output [6]. In this article study and designs of high speed reversible gates
layout in QCA has been introduced. Results and discussion show a higher level of performance for the new layout in QCA are better than CMOS at high speed computing applications.

The major features of the proposed work are as follows:

- The reversible gate architecture is designed using Boolean expression and truth table which can be further used for designing QCA layouts.
- The parameter analysis of reversible gate is done by the QCA Designer tool.
- The proposed circuit is designed with QCA technology using QCADesigner 2.0.3 version software with efficient clocking schemes.
- Simulations are generated for proposed design to check its design, implementation and functionality.
- The area and delay are calculated using QCADesigner software.

The rest of the article as follows: section 2 describes Terminology, section 3 shows proposed work, section 4 reviews comparison and section 5 concludes the paper.

2. Terminology

QCA cell serves as an integral component in the process of QCA circuit designing [7]. Its structure is equivalent to a square box. Four corners of which contain four quantum dots. The location of electrons determines the two basic binary states possessed by the cells which are logic 0 and logic 1. There is no charge transport mechanism between the QCA cells, unlike CMOS. QCA comprises coulombic processes only [8]. The state of the nearby QCA cells during previous clock cycle determines the instantaneous state of a cell at a specified time [9]. Clocks numbers are the four clock zones present in QCA. The colour green is used to indicate clock zone 0, which is termed as the switch state [10]. The colour magenta is used to indicate clock zone 1, which is termed as the hold state. The colour blue is used to indicate clock zone 2, which is termed as the release state.

2.1 Basic QCA Elements

The working principle of QCA cell is based on Coulombs law. Due to Coulomb force, two electrons interact with each other called as kink energy with the four quantum dots of a QCA cell using the help of the clock signal through the junction of tunnels. The two electrons are occupied in such a way that they are diagonal to each other due to interaction between two electrons [11]. The way the electrons are placed give the polarization of the cell. The polarization of a QCA cell can only be done in two ways. The polarization of QCA cell are -1 and +1. There are four preferred clocking schemes or zones with four different clock signals which help with the information flow and switching of QCA cells [12]. They are discussed as Clocking Zone 0, zone 1, zone 2, zone 3. In each clocking zone, there are four clock phases as Switch, Hold, Release and Relax. The four clock are each in 90 degree phase difference with each other, which is shown in Fig. 1. One of four clock signal use for reference while other clocks are delays namely

1. Reference clock (0 phase)
2. Delay 1 clock (phase)
3. Delay 2 clocks (phase)
4. Delay 3 clocks (phase)

When a cell holds no binary information, the cell is electro-statically switched from a void or null state, clocking is achieved depending on its phase [13]. In switch phase, cell state is influenced by its neighboring cells. In lock phase, cell state is not influenced by its neighboring cells, it’s independent [14]. At the time of transfer of information cells in each clock zone pass through all the four phases present in that particular clock zone. After passing all four phases information transfer takes place.
Fig. 1. Clocking Zones of QCA

**Switch Phase**
- During the switch phase, the junction barrier rise QCA cells are polarized respective to its polarization of the driver cell.
- Computation actually takes place in the switch clock phase

**Hold Phase**
- During the hold phase, the junction barriers are raised to its highest value.
- QCA cell is now input to the next stage in the hold phase

**Release Phase**
- During the release phase, the junction barriers are down or getting low.
- QCA cell is non-polarized and remain in the neutral state.

**Relax Phase**
- During the relax phase, the cell will return to its first reference clock phase.
- QCA cells can be again polarized in relaxed phase.

Fig. 2. QCA architectures based on quantum cell (a) Polarization (b) Majority gate (c) NOT (d) Wire

If we use all four clock signals in a circuit, then there will be a delay in the output of the circuit. So complex circuits have high delay. Assignment of clock schemes or zones is vital part during evaluation of QCA circuit and its simulation [17]. So, research of novel advanced clocking scheme is required during the implementation of QCA circuit layouts [18]. By arranging a different number of
QCA cells, different types of QCA devices can be designed such as polarization in QCA, QCA majority gate, QCA inverter, QCA wire, which is shown in Fig. 2a, 2b, 2c, 2d respectively. The data flow from one cell to another cell in a QCA wire. The array of QCA cells will act as a wire. If QCA cells are located adjacent to each other, the electron position is transferred from one cell to another adjacent cell. Due to this the state of all adjacent cells will all be same state because of coulomb interaction.

3. Proposed Work

3.1 Reversible Feynman gate.

In Feynman gate, if the first input is reset when the second output is same as input and if the first input is reset then second input is flipped at the output. It is also known as controlled not. Schematic of Feynman gate is drawn in Fig. 3. Cell layout and simulation results of Feynman gate are presented in Fig. 4 (a & b), respectively.

![Feynman Gate Schematic](image)

**Fig. 3. Schematic of Feynman gate**

![Feynman Gate Simulation Results](image)

**Fig. 4. Feynman Gate (a) Cell Layout (b) Results**
3.2 Reversible Fredkin gate
In Fredkin gate first output is same as the input. If the first input is set, then it swaps other inputs at the output. It is also known as a controlled permutation gate. In Fig. 5, shows a block diagram of Fredkin gate. Cell layout and simulation results of Fredking gate are presented in Fig. 6a and 6b respectively.

![Fig. 5. Schematic of Fredkin gate](image)

![Fig. 6. Fredkin Gate Cell Layout and Results](image)
3.3 Reversible Toffoli gate. In Toffoli gate, if the first two bits are set, then it flips the third input at the output. It is considered as a universal reversible logic gate and it is also known as a controlled-controlled-not gate. In Fig. 7, shows a block diagram of Toffoli gate. Cell layout and simulation results of Toffoli gate are presented in Fig. 8a and 8b respectively.

![Fig. 7. Schematic of Toffoli Gate](image)

![Fig. 8. Toffoli Gate (a) Cell Layout (b) Results](image)
4. Comparison

The QCA integrating circuits are designed using basic logic gates like majority gates, inverters, and minority gates. These are important components, while designing any circuit in QCA technology. The design of architecture of computer system and processor system face problems regarding storage devices optimizing. For complex systems, efficient circuits with novel clock schemes need to be introduced to QCA technology designing. The designing of reversible gates in QCA technology is done in this article. The performance of proposed reversible gates based on QCA technology is evaluated and simulated using QCAdesigner version 2.03 software and verified its functionality. Compared to prior works, the performance of the proposed reversible gate in QCA technology is improved in terms of cell, cycle and bounded area. The Table 1 shows the efficient utilization of the number of QCA cells by the proposed reversible Feynman, Toffoli, Fredkin gates than the previous best designs in the paper [15], [16], [19]. The novelty should be present in the architecture of basic reversible gates layout, because designing cells architecture using QCA technology is less complex, and high speed and low power during implementation. So, an effective circuit should be designed using basic components like inverter, majority gates with new techniques, which can make our circuit layout yield low power consumption even with high speeds. Designing in QCA technology requires advanced clocking and efficient circuit layout which can be tricky. The proposed basic reversible gates have advanced clocking, while designing circuits and use less number of QCA cells while keeping power low. The proposed basic reversible gate architecture in QCA technology should also be more efficient compared to existing designs. Then basic reversible gates designed using QCA techniques are compared to conclude which reversible gate architecture cell designed with QCA technology is more efficient.

Table. 1 Comparison results based on the QCA figure of merits

|                  | Reference | Feynman | Toffoli | Fredkin |
|------------------|-----------|---------|---------|---------|
| **Cells**        | [15]      | 53      | 57      | 97      |
|                  | [16]      | 89      | 128     | *NS     |
|                  | [19]      | 32      | 45      | 73      |
|                  | Proposed work | 17      | 25      | 67      |
| **Cycles**       | [15]      | 0.75    | 0.75    | *NS     |
|                  | [16]      | 1       | 1       | *NS     |
|                  | [19]      | 0.75    | 0.75    | 0.75    |
|                  | Proposed work | 0.5     | 0.5     | 0.75    |
| **Bounded-area** | [15]      | 15*10   | 17*9    | 16*16   |
|                  | [16]      | 17*15   | 31*16   | *NS     |
|                  | [19]      | 9*8     | 11*10   | 17*9    |
|                  | Proposed work | 6*6     | 10*6    | 18*8    |

*NS significance- not specified

5. Conclusion

The QCA technology is one of the popular Nanotechnology, which uses quantum gates for designing instead of transistors, which makes it a transistor less technology. Its attractive features like low density, low power consumption, high computation speed and high scaling over CMOS technology make it a future trend technology, which can used for designing electronic devices in the dimensions of nano-scale. The important concern during designing a basic reversible gates is to design an efficient circuit layout with advanced clocking schemes as its first concern for designing any circuit layout in
the QCA technology. The basic reversible gates, which is of single layer architecture is proposed in this article. The proposed gate is designed and implement using QCA technology. The proposed three gates use 46.87%, 44.44% and 8.95% less number of QCA cells than the previous best design respectively. The proposed designs in this paper lesser rectangular layout of the gates than those earlier papers. Only one XOR gate used in Feynman gate while there is no usage of any majority gate. One from each of the XOR and majority gate are used in Toffoli gate and one majority gate and three XOR gates are used in Fredkin gate.

References

[1] Misra, N. K., Sen, B., Wairya, S., & Bhoi, B. (2017). Testable novel parity-preserving reversible gate and low-cost quantum decoder design in 1D molecular-QCA. Journal of Circuits, Systems and Computers, 26(9), 1750145.
[2] Misra, N. K., Wairya, S., & Singh, V. K. (2014). Preternatural low-power reversible decoder design in 90 nm technology node. International Journal of Scientific & Engineering Research, 5(6), 969-978.
[3] Landauer, R. (2000). Irreversibility and heat generation in the computing process. IBM Journal of Research and Development, 44(1/2), 261.
[4] Bennett, C. H. (1973). Logical reversibility of computation. IBM journal of Research and Development, 17(6), 525-532.
[5] Misra, N. K., Wairya, S., & Singh, V. K. (2014, May). An inventive design of 4* 4 bit reversible NS gate. IEEE International Conference on Recent Advances and Innovations in Engineering (ICRAIE-2014), 1-6.
[6] Bhoi, B. K., Misra, N. K., & Pradhan, M. (2018). Novel robust design for reversible code converters and binary incremenetr with quantum-dot cellular automata. In Intelligent Computing and Information and Communication (pp. 195-205). Springer, Singapore.
[7] Lent, C. S., & Tougaw, P. D. (1993). Lines of interacting quantum-dot cells: A binary wire. Journal of Applied Physics, 74(10), 6227-6233.
[8] Misra, N. K., Wairya, S., & Singh, V. K. (2015). Frame of Reversible BCD Adder and Carry Skip BCD Adder and Optimization Using New Reversible Logic Gates for Quantum-Dot Cellular Automata. Australian Journal of Basic and Applied Sciences, 9(31), 286-298.
[9] Bhoi, B., Misra, N. K., & Pradhan, M. (2017). Design and evaluation of an efficient parity-preserving reversible QCA gate with online testability. Cogent Engineering, 4(1), 1416888.
[10] Misra, N. K., Wairya, S., & Sen, B. (2018). Design of conservative, reversible sequential logic for cost efficient emerging nano circuits with enhanced testability. Ain Shams Engineering Journal, 9(4), 2027-2037.
[11] Fredkin, E., & Toffoli, T. (2002). Conservative logic In: Collision-based computing, pp. 47-81.
[12] Dueck, G. W., & Maslov, D. (2003, March). Reversible function synthesis with minimum garbage outputs. In 6th International Symposium on Representations and Methodology of Future Computing Technologies (pp. 154-161).
[13] Bahar, A. N., Habib, M. A., & Biswas, N. K. (2013). A novel presentation of toffoli gate in quantum-dot cellular automata (QCA). International Journal of Computer Applications, 82(10).
[14] Islam, M. S., & Bahar, A. N. A Review on Reversible Logic Gates and it’s QCA Implementation. International Journal of Computer Applications, 975, 8887.
[15] Mohammadi, Z., & Mohammadi, M. (2014). Implementing a one-bit reversible full adder using quantum-dot cellular automata. Quantum information processing, 13(9), 2127-2147.
[16] Garg, U., & Jain, R. (2016). Design and performance analysis of reversible RSG gate using QCA. Int J Comput Appl, 139(12), 37-41.
[17] Walus, K., Dysart, T. J., Jullien, G. A., & Budiman, R. A. (2004). QCADesigner: A rapid design and simulation tool for quantum-dot cellular automata. IEEE transactions on nanotechnology, 3(1), 26-31.
[18] Srivastava, S., Asthana, A., Bhanja, S., & Sarkar, S. (2011, May). QCAPro—an error-power estimation tool for QCA circuit design. In 2011 IEEE international symposium of circuits and systems (ISCAS) (pp. 2377-2380). IEEE.
[19] Singh, G., Sarin, R. K., & Raj, B. (2017). Design and analysis of area efficient QCA based reversible logic gates. Microprocessors and Microsystems, 52, 59-68.