Continuous-Time Analog Filters for Audio Edge Intelligence: Review and Analysis on Design Techniques

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Abstract—Silicon cochlea designs capture the functionality of the biological cochlea. Their use has been explored for cochlea prostheses and more recently in edge audio devices which are required to support always-on operation. As their stringent power constraints pose several design challenges, IC designers are forced to look for solutions that use low standby power. One promising bio-inspired approach is to combine the continuous-time analog filter channels of the silicon cochlea with a small memory footprint deep neural network that is trained on edge tasks such as keyword spotting, thereby allowing all blocks to be embedded in an IC. This paper reviews the analog filter circuits used as feature extractors for current edge audio devices, starting with the original biquad filter circuits proposed for the silicon cochlea. Our analysis starts from the interpretation of a basic biquad filter as a two-integrator-loop topology and reviews the progression in the design of second-order low-pass and band-pass filters ranging from OTA-based to source-follower-based architectures. We also derive and analyze the small-signal transfer function and discuss performance aspects of these filters. The analysis of these different filter configurations can be applied to other application domains such as biomedical devices which employ a front-end bandpass filter.

Index Terms—Auditory, silicon cochlea, two-integrator-loop, band-pass filter (BPF), continuous-time (CT) filter, flipped voltage follower (FVF), second-order filter, source-follower (SF), super source-follower (SSF).

I. INTRODUCTION

Silicon cochleas capture the functionality of the biological cochlea starting from a set of broadly frequency-selective channels which model the biophysical properties of the basilar membrane [1], [2]. The channel circuits within spiking cochleas implement the frequency-selective filtering properties of the basilar membrane, rectifying properties of the biological inner hair cells, and asynchronous neuronal firing of the ganglion cells [3]–[10]. These biomimetic cochlea circuits have been proposed for biomedical applications, particularly, as a bionic ear processor or for cochlea implants [11]–[13].

The cochlea circuits have been used in other applications such as azimuthal sound source localization [14], [15], speech recognition [16], [17], speaker verification [18], keyword spotting (KWS) [19] pointing to their promise for the area of low-power hearables or Internet of Things (IoT) domain. In the latter domain, there is a strong interest and focus on low-power always-on devices that can perform smart pre-processing of the input before data transmission to the cloud. Typical edge audio tasks performed on these devices include voice activity detection (VAD) and KWS.

Solutions for reported state-of-art edge audio integrated circuits (ICs) come in two forms. The first approach samples the microphone output signal at Nyquist or oversampling frequency and quantized through an analog-to-digital converter (ADC). These data samples are then further processed by a digital signal processing block such as fast Fourier transform (FFT), followed by triangular filtering, and logarithmic compression. The second approach is to replace the synchronous ADC and the subsequent signal processing stages with asynchronous continuous-time (CT) analog filter circuits, inspired by the biological modeling of cochleas [1]. Adopting CT analog filters is regarded as a promising alternative to conventional Nyquist sampling circuits in terms of better power efficiency. This is because the FFT computation circuit is typically the most power-hungry building block of the entire audio feature extractor (FEx) [20]. The analog signal processing potentially has a higher power efficiency [21], [22], and thus it could be useful for tasks implemented on low-power edge audio devices. The CT analog filters on the state-of-art edge audio ICs for VAD [23]–[25] and KWS [26], [27] adopt a set of second-order band-pass filters (BPFs). These circuits were derived from early generations of silicon cochlea designs starting from [1] and a summary of the various voltage-domain/current-domain CT filter designs can be found in [3] and Chapter 3 of [2].

This paper aims to provide a comprehensive analysis of voltage-domain CT analog filters leading to the circuits that have been reported in recent edge audio ICs. It will provide an unified analysis that covers $g_{mC}$ equivalent and small-signal equivalent diagrams, based on a two-integrator-loop biquad topology. To the best of our knowledge, it is the first work to present the operating principle of voltage-domain second-order filters using an unified analysis that includes the operational transconductance amplifier (OTA)-based, cross-coupled source-follower (XSF), super source-follower (SSF), and flipped voltage follower (FVF) biquad filters. Simulation results are also provided to show support for the proposed analysis. This analysis can be applied to other signal domain, e.g., the time-domain filter [26]. It is also useful for the development of new filter circuits and architectures for applications involving temporal signals such as brain computer interface.
The remainder of this paper is organized as follows. Section II introduces the basics of biquad filters and discusses how a second-order BPF can be implemented from the two-integrator-loop topology. Section III presents the notation of a transconductor which is used in the description of the filters. Section IV and Section V present the core analysis of the OTA-based and source-follower (SF)-based filter circuits. Section VI summarizes and discusses the state-of-the-art approaches for the design of edge audio ICs with brief future research prospects. Section VII concludes this paper.

II. REVIEW ON BQUAD FILTER

The second-order filter is also called as a biquadratic filter or a biquad filter. It is because its transfer function is the ratio of two quadratic equations.

a) Biquad LPF: The general transfer function of a second-order LPF is

$$H_{\text{LPF}}(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} = \frac{1}{\omega_0^2 + \frac{s}{Q\omega_0} + 1} \quad (1)$$

where $\omega_0$ is the natural frequency (also the cutoff frequency in LPF or center frequency in BPF) and $Q$ is the quality factor of the filter. We demonstrate how this transfer function can be decomposed into multiple forms that lead to different circuit topologies. We first express Eq. (1) in a similar form to the transfer function of the closed-loop gain of a negative feedback system, i.e., $A_{\text{CL}} = A/(1 + \beta A)$ where $A$ is the feedforward gain, $\beta$ is the feedback gain. By setting $H_{\text{LPF}}(s) = A_{\text{CL}}(s)$, and defining $A(s)$ and $\beta(s)$ as

$$A(s) = \frac{1}{\omega_0^2 + \frac{s}{Q\omega_0} + 1} \quad \beta(s) = 1 \quad (2)$$

we can construct a corresponding block diagram as shown in Fig. 1(a) where $H_{\text{LPF}}(s) = V_{\text{PF}}(s)/V_{\text{IN}}(s)$. This topology can be further decomposed into a cascaded structure forming a Lossy integrator and a Lossless integrator as shown in Fig. 1(b) and is also called a Two-Integrator-Loop topology [28]. The characteristics of both integrator types are shown in Fig. 1(d). We see that the first-order LPF corresponds to the lossy case and an ideal integrator to the lossless case. The lossy integrator can be further decomposed into a lossless integrator associated with a nested feedback path which controls $Q$ of the second-order filter as shown in Fig. 1(c). This two-integrator-loop topology is used in a popular filter implementation called the Tow-Thomas biquad [29].

b) Biquad BPF with Poles at the Same Frequency: Fig. 1(c) also shows how a BPF response is obtained at the output of the lossy integrator within this topology. This is because the lossless integrator is excluded in the feedforward gain of $H_{\text{BPF}}(s)$ compared to $H_{\text{LPF}}(s)$ case, which in turn acts as a differentiation of $H_{\text{LPF}}(s)$ (i.e., $s$). The transfer function of the resulting second-order BPF can be expressed as

$$H_{\text{BPF}}(s) = \frac{\omega_0 s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \quad (3)$$

Note that the same design structure applies for implementing a DC-servo loop within bio-signal amplifiers [30], [31] as the servo loop also include an analog integrator to generate the high-pass frequency response shape, for electrode offset removal.

Fig. 2(a) shows a two-integrator-loop topology that uses a transconductor to realize the transfer function $H_v(s)$ of an allpass second-order filter [32]. In Fig. 2(a), the second integrator is assumed to be lossy, and the input $V_x(s)$ is the differential output of the first integrator. The transfer function $H_v(s)$ is a ratio of the second integrator’s output $V_y(s)$ to the first integrator’s input $V_x(s)$, which is extracted from Fig. 1(a) where $V_x(s)$ corresponds to $V_0(s)$ of the input transistor within the SF-based filters (see Section V-A). Exceptions are type-I SSF and type-I FVF filters, which will be discussed in Sections V-D and V-E. The transfer function $H_v(s)$, which is extracted from $V_x$, the output of lossless integrator, deviates from the ideal BPF ($H_{\text{BPF}}(s)$ in Eq. (3)) response as an equation below.

$$H_v(s) = \frac{\omega_0 \left(s + \frac{\omega_0}{Q}\right)}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \quad (4)$$

Fig. 2(c) shows that $s + \omega_0/Q$ term incurs lossy high-pass response in $H_v(s)$. This lossy response can also be predicted...
by calculating \( H_X(0) \), which gives \( 1/Q \), in contrast to the case where \( H_{\text{LPF}}(0) = 0 \). To achieve an output with an ideal BPF (\( H_{\text{BPF}}(s) \) in Eq. (3)) curve using the lossless-first two-integrator-loop filter, we can use \( V_Y \) (see Fig. 2(a)) where

\[
H_Y(s) = H_X(s) - H_{\text{LPF}}(s) \frac{1}{Q} = H_{\text{BPF}}(s)
\]  

(5)

Another method of getting a BPF output using the lossless-first two-integrator-loop topology is shown in Fig. 2(b). Here, \( V_X \) and \( V_{\text{LPF}} \) are subtracted, outside the feedback loop, to obtain \( V_{\text{BPF}}(s) \) as shown in (5).

c) Biquad BPF with Poles at Different Frequencies: We look next at the case where the filter has two different pole values (set by \( \omega_1, \omega_2 \)) as in Fig. 3 instead of two identical poles (Fig. 2). The transfer functions corresponding to the \( V_{\text{LPF}}, V_X \) nodes and the \( Q \) factor are described below.

\[
H_{\text{LPF}}(s) = \frac{\omega_1 \omega_2}{s^2 + \omega_2 s + \omega_1 \omega_2}
\]

\[
H_X(s) = \frac{\omega_1 (s + \omega_2)}{s^2 + \omega_2 s + \omega_1 \omega_2}
\]

\[
Q = \sqrt{\frac{\omega_1}{\omega_2}}
\]  

(6)

Similarly to (4), \( H_X(s) \) includes \( s + \omega_2 \) term in the numerator and thus it exhibits a lossy behavior at its high-pass shape as shown in Fig. 3(c) where \( H_X(0) = 1 \) and its peak gain is \( \omega_1/\omega_2 = Q^2 \). As in (5), by subtracting \( V_X \) and \( V_{\text{LPF}} \), one gets an ideal band-pass response.

\[
H_Y(s) = H_X(s) - H_{\text{LPF}}(s) = \frac{\omega_1 s}{s^2 + \omega_2 s + \omega_1 \omega_2} = H_{\text{BPF}}(s)
\]  

(7)

The subtraction can be implemented either within the feedback loop (\( V_Y \) in Fig. 3(a)) or out of the loop (\( V_{\text{BPF}} \) in Fig. 3(b)). Note that \( 1/Q \) term is not multiplied with \( H_{\text{LPF}}(s) \) in (7) because \( Q \) is now dependent on \( \omega_1 \) and \( \omega_2 \) while the feedback path within the lossy integrator in Fig. 3 has unity gain.
geometric means (which one can derive by using the inequality of arithmetic and geometric means (x + y ≥ 2√xy). In order to realize a wide Q tunability, a second-order filter based on a two-integrator-loop topology is preferred over a cascaded lossy integrators.

In the following sections, we will analyze the second-order filter circuits by interpreting them either as lossy-first or as lossless-first two-integrator-loop topologies. In addition, we will only deal with the small-signal models excluding large-signal behaviors of the filter.

### III. Notation Declaration

Throughout this paper, transconductors ($g_m$) will be depicted using a 4-port drawing as shown in Fig. 5(a) [32], instead of the conventional 3-port drawing style that uses a single output port (rightside of Fig. 5(b)). This is particularly needed to analyze the source-follower-based filters, in which a single transistor acts as a transconductor and multiple transconductors are placed in a single bias current branch. We will discuss this type of filters in Section V. Fig. 5(b) shows an example of a $g_m$C lossy integrator implementation. The block diagram of this circuit can be described either with voltage-mode (Fig. 5(c)) subtraction or current-mode (Fig. 5(d)) subtraction. We will use both representations interchangeably throughout this paper.

#### IV. OTA-Based Filters

**A. Second-Order LPF**

Fig. 6 shows the OTA-based second-order LPF adopted in the early silicon cochlea designs [1], [5], [33], [34]. The circuit consists of 3 OTAs and 2 capacitors leading to a $g_m$C topology. Note that the diode-connected source degeneration technique was used in the OTAs of the feed-forward path ($g_{m1}; g_{m2}$), to extend the linear input range of the filter [5] but at the expense of voltage headroom. The transfer function of this circuit is described in (8). Here we assumed that the intrinsic gain of transistor is sufficiently large ($g_{m}r_o \gg 1$), where $r_o$ denotes the output impedance of a transistor, such that the load impedance of each transconductors can be approximated as $1/sC$. This assumption is used throughout our analysis of this paper.

The basic structure of Fig. 6 is equivalent to the cascaded lossy integrators (or first-order LPFs) in Fig. 4. However, the added positive feedback $g_{m3}$ makes a significant difference to the transfer function in (9) because it cancels out the negative feedback within the first lossy integrator when $g_{m1} = g_{m3}$. It can be seen from the transfer function that $-g_{m3}/C_1$ cancels out $g_{m1}/C_1$ when $g_{m1} = g_{m3}$ thereby the overall topology reduces to the lossless-first two-integrator-loop structure (see Fig. 3(a)). In other words, the positive feedback converts a lossy integrator into a lossless one. This in turn leads to complex poles in its transfer function and its maximum Q value is no longer limited to 0.5 in contrast to the case of cascaded lossy integrators (Fig. 4 and (9)). The transfer function, $\omega_0$, and Q factor of the OTA-based LPF when $g_{m1} = g_{m3}$ are given below.

$$H_{OTA-LPF}(s) = \frac{g_{m1}g_{m2}}{s^2 + s \left( \frac{g_{m1}}{C_1} - \frac{g_{m3}}{C_1} + \frac{g_{m2}}{C_2} \right) + \frac{g_{m1}g_{m2}}{C_1C_2}}$$

$$\omega_0 = \frac{\sqrt{g_{m1}g_{m2}}}{C_1C_2} \quad Q = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2} - \frac{g_{m3}}{C_1} + \frac{g_{m2}}{C_2}} \quad (8)$$

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$$H_{OTA-LPF}(s) = \frac{g_{m1}g_{m2}}{s^2 + s \left( \frac{g_{m1}}{C_1} - \frac{g_{m3}}{C_1} + \frac{g_{m2}}{C_2} \right) + \frac{g_{m1}g_{m2}}{C_1C_2}}$$

$$\omega_0 = \frac{\sqrt{g_{m1}g_{m2}}}{C_1C_2} \quad Q = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2} - \frac{g_{m3}}{C_1} + \frac{g_{m2}}{C_2}} \quad (8)$$

With this parameter setting, the positive feedback path is removed and thus the feedback stability is easier to be ensured.
Fig. 7. OTA-based second-order BPF [35] with (a) $g_mC$ equivalent circuit and (b) small-signal diagram.

$$H_{OTA-BPF}(s) = \frac{s g_{m1}}{s^2 + s \left( \frac{g_{m1}}{C_1} - \frac{g_{m3}}{C_2} + \frac{g_{m2}}{C_1} \right) + \frac{g_{m1}g_{m2}}{C_1C_2} + g_{m1}g_{m2}}$$

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}$$

$$Q = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2} + \frac{g_{m1}g_{m2}}{C_1C_2}}$$

(10)

In the original paper [1] that proposed the LPF in Fig. 6 for the cochlea channel, the following choices were made: $C = C_1 = C_2$ and $g_{m1} = g_{m2}$ leading to the following equations for the transfer function, $Q$, and $\omega_0$.

$$H_{OTA-LPF2}(s) = \frac{s^2 + s \left( \frac{g_{m1}}{C_1} - \frac{g_{m3}}{C_1} + \frac{g_{m2}}{C_2} \right) + \frac{g_{m1}g_{m2}}{C_1C_2}}$$

$$\omega_0 = \frac{g_{m1}}{C}$$

$$Q = \frac{1}{2 \left( 1 - \frac{g_{m3}}{2g_{m1}} \right)}$$

(12)

Compared to (11), this approach obtains $\omega_0$ and $Q$ with simpler forms. In addition, it offers better $\omega_0$ matching since $\omega_0$ is determined by only two core parameters, $g_{m}$ and $C$. However, the positive feedback path is not removed and thus design parameters must be chosen carefully to ensure stability.

B. Second-Order BPF

Fig. 7 shows the implementation of an OTA-based BPF [35]. In addition to the original LPF in Fig. 6, a differential buffer takes the difference of the $V_X$ and $V_{LPF}$. The buffer structure is equivalent to an open-loop first-order $g_mC$ LPF (see Chapter 19 in [36]) or a lossy integrator, however its cutoff frequency is set by a parasitic capacitance $C_{par}$. Note that the buffer is an open-loop design because the used transconductances for the feedforward ($g_{m4}$) and feedback ($g_{m5}$) paths are different. This architecture follows the lossless-first two-integrator-loop topology with an external subtractor as discussed in Fig. 3(b). The transfer function of this OTA-based BPF is given in (10) which can be derived using a nodal analysis as below where $H_{LPF}(s)$ is given in (8).

$$H_{OTA-BPF}(s) = H_{X}(s) = H_{Lpf}(s) \frac{1 + s C_2}{g_{m4} + s C_{par}} \approx 1$$

$$H_{OTA-BPF}(s) = (H_{X}(s) - H_{Lpf}(s)) H_{Buf}(s) = s \frac{C_2}{g_{m2}} H_{Lpf}(s)$$

(13)

Here, the approximation for $H_{Buf}(s)$ is valid when the parasitic pole $g_{m5}/C_{par}$ within the buffer stage is far higher than $\omega_0$ of the BPF and satisfying $g_{m4} = g_{m5}$. This means that the buffer stage is assumed to have a sufficiently wide bandwidth. Note that $\omega_0$ and $Q$ in (10) are the same as in (8) because the polynomial equation on the denominator does not change. Adopting the principle of this OTA-based BPF structure, further improved versions of the BPF [6], [9] that output a current-domain signal (excluding $g_{m5}$ in Fig. 7) were implemented in a cascaded filter array. In [16], the fabricated filter circuit [6] was used as an audio FEx whose output was fed into a field-programmable gate array (FPGA)-based recurrent neural network (RNN) classifier for speech recognition task using the TIDIGITS dataset.

A simpler form of the BPF as shown in Fig. 8 uses the OTA as a core building block [23]. This circuit adopts a capacitively-coupled instrumentation amplifier (CCIA) [37] associated with a buffer-based DC-servo loop. Its transfer
function can be derived as in (14) using a nodal analysis below.

\[
H_{\text{CCIA-BPF}}(s) = -\frac{g_{m1}}{s^2 + s \frac{g_{m2}}{C_1} + \frac{g_{m1}g_{m2}}{C_1C_2}} \quad \omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad Q = \frac{g_{m1}C_1}{g_{m2}C_2}
\]

(14)

V. SOURCE-FOLLOWER-BASED FILTERS

A. Source-Follower (First-Order LPF)

Fig. 9 shows a transistor-level schematic, \( g_mC \) equivalent circuit, and block diagram of the SF-based first-order LPF. The minus output port (sink) of \( g_m \) transconductor, which is the \( M_1 \) transistor, is tied to AC GND (corresponding to VDD in the schematic) in the \( g_mC \) equivalent circuit. The transfer function of the SF-LPF is given as below, denoting the equivalent transconductance of the circuit as \( G_m = \partial I_\text{IN}/\partial V_\text{IN} \) (see Chapter 3.2.5 in [38]).

\[
H_{\text{SF}}(s) = G_m R_L = \frac{1}{g_{m1} + R_L \left( 1 + \frac{1}{g_{m1}r_{ob1}} \right)} \cdot R_L
\]

\[
= \frac{g_{m1}}{g_{m1} + g_{ds1} + g_{dsb}} \cdot \frac{1}{1 + \frac{sC_1}{g_{m1} + g_{ds1} + g_{dsb}}}
\]

\[
\approx \frac{1}{1 + \frac{sC_1}{g_{m1}}}
\]

(17)

Here, \( r_{ob1} = 1/g_{dsb} \) is the output impedance of transistor \( M_1 \), \( r_{ob} = 1/g_{dsb} \) is the output impedance of tail current source, and \( R_L = (1/sC_1) || r_{ob} = 1/(sC_1 + g_{dsb}) \) is the load impedance seen at the \( V_\text{OUT} \) node. Note that we ignored the body effect of the transistor, i.e., \( g_{mb} = 0 \) and the same assumption will be applied throughout the paper. The approximation in (18) is valid assuming sufficiently large intrinsic gain of the transistor \( g_m/g_m \gg 1 \). Since its cutoff frequency \( \omega_0 = g_{m1}/C_1 \) includes transconductance and capacitance, the SF-LPF is a first-order \( g_mC \) filter or a lossy integrator as discussed in Section II and presented in Fig. 5(b). As shown in Fig. 9(b), the SF implements a local feedback around the source node of the \( M_1 \) transistor. Because the closed-loop gain at DC is given in the first term of (17), we can derive a DC loop gain \( T_0 \) of the local feedback in the SF, using the equation of closed-loop gain in the negative feedback system \( A_{\text{CL}} = A/(1 + \beta A) \) where \( T = \beta A \) and \( \beta = 1 \) are used considering the unity-gain
Fig. 10. (a) Transistor-level schematic, (b) half-circuit representation of the schematic, (c) $g_mC$ equivalent circuit, and (d) small-signal diagram of the cross-coupled source-follower-based LPF.

The above equation shows that the closed-loop gain $A_{CL0}$ approaches 1 as $T_0 \gg 1$. In other words, the linearity performance of a SF-LPF is enhanced with a larger transconductance $g_m$ benefiting from its local feedback. Compared to the conventional open-loop $g_mC$ filters in which the input transistors are usually operated at strong-inversion to suppress harmonic distortions [36], the SF-LPF allows the input transistor to operate in subthreshold. Since the subthreshold region offers a higher $g_m$ within a given power budget, i.e., higher $g_m/I_D$, it leads to both better linearity and lower input-referred noise. Note that the active RC filters also operate with a negative feedback loop thereby offering higher linearity than open-loop $g_mC$ filters, however they have a higher power burden because of the needed amplifiers to drive resistive loads [36]. Overall, the SF filters are more suitable for ultra-low-power audio filter implementation.

B. Cross-Coupled Source-Follower (Second-Order LPF)

Fig. 10 shows a transistor-level full schematic, half-circuit equivalent, $g_mC$ equivalent, and block diagram of the XSF-based second-order LPF [39], [40] while the transfer function and filter parameters are given in (16). Note that we define the polarity of the LPF output in a reversed way due to the cross-coupled structure within the filter circuit. For instance, the signal flow starting from $V_{INP}$ ends at $V_{LPFP}$ through the source-following operations of $M_{1P}$ and $M_{2N}$. If we would like to extract the output from the left-half of the circuit ($V_{LPFN}$) while also keeping the input fixed to the left-half ($V_{INP}$), an ideal inverting buffer is required considering differential structure of the circuit, as shown in the half-circuit schematic Fig. 10(b).

Although not easy to identify, interestingly, the core structure of this filter circuit is the same as the OTA-based LPF in Fig. 6, i.e., it has a lossless-first two-integrator-loop topology with auxiliary positive and negative feedback paths. Assuming $g_m1 = g_m2$ as used in the original paper [39], the transfer function, $\omega_0$, and $Q$ of XSF filter are given below:

This equation becomes quite similar to the transfer function of the OTA-based LPF assuming $g_m1 = g_m2 = g_m3$ in (11).
To provide an intuitive insight into the operation of the XSF circuit, a step-by-step design procedure starting from a basic SF is illustrated in Fig. 11. First, let us consider the case of stacking two SFs in a single branch. The stacking is especially beneficial as it allows a better $g_{m}$ matching and easier cut-off frequency tuning, because the bias current of the two SFs are reused. However, if the two SFs are stacked, the input of the second SF should be connected to the output of the first SF, which in turn, requiring gate and drain ports of input transistor in the second SF to be shorted into a single node. It results in a diode-connection of the input transistor as shown in Fig. 11(b), which incurs a low-impedance load to the first SF output, thereby leading to a failure of proper source-following operation of the first SF. One possible solution to this problem is using a replica SF (Fig. 11(c)). Here, input of the main circuit goes to the input of the replica circuit and we assume that the gate of the $M_2$ transistor in replica circuit is properly biased ($V_B$). Note that the output of the first SF now has a cascode current source which is a high-impedance load. Therefore, the output of the second SF forms a cascaded lossy integrator (the blue line in Fig. 11(c)) as discussed in Fig. 4. Finally, we can exploit this replica circuit as an active building block that operates in a complementary manner to the main circuit, i.e., differential circuit, using a cross-coupling technique. The final schematic of the XSF is drawn as in Fig. 11(d). Note that the added positive feedback path (uppermost $g_{m_2}$ in Fig. 10(d)) cancels lossy property of the first SF within the cascaded lossy integrator and thus the maximum $Q$ value is no longer limited to 0.5, as discussed in Section IV. We can omit the GND connection between the two $C_1$ capacitors and merge them into a single $C_1/2$ capacitor like in Fig. 10(a) because the input signal is in differential-mode and thus a virtual GND forms when $C_1/2$ in Fig. 10(a) is splitted into the two serialized $C_1$.

The transfer function for $V_X$ node is derived as below. As discussed in Fig. 3(a) and (6), $H_X(s)$ exhibits a lossy behavior at its low-frequency band.

$$H_X(s) = \frac{H_{XSF1}(s)}{H_{Lossy}(s)} = H_{XSF1}(s) \left(1 + \frac{sC_2}{g_{m1}}\right)$$

$$= \frac{g_{m1}}{C_1C_2} \left(1 + \frac{sC_2}{g_{m1}}\right)$$

To evaluate the frequency response at $V_X$ and the analysis discussed in Fig. 3 and (6), an AC simulation is conducted with XSF filter circuit using a 65-nm CMOS process. The width and length of all transistors are sized at 1 $\mu$m. The supply voltage is set as 1.2 V. Also, high $V_{TH}$ devices are used since they have higher intrinsic gain than nominal $V_{TH}$ devices. The source and body contacts of the transistors are shorted to negate body effects (a deep N-well layout is required in this case), therefore $g_{m1} = g_{m2}$ and (21) becomes valid. We will use the same simulation setups in Sections V-D and V-E unless otherwise it is specified. We set $C_2/2 = 4C_1/2 = 4$ pF such that $Q = 2$. Fig. 12 shows frequency responses of $H_{LPF}(s)$, $H_X(s)$, and $G_{mx}(s)$ where

$$G_{mx}(s) = \frac{i_{P} - i_{N}}{v_{INP} - v_{INN}}(s)$$

stands for the transconductance of differential current flowing through $M_2$ transistor in Fig. 11(d). As expected, $H_{LPF}(s)$ shows a second-order LPF behavior with a 40dB/dec roll-off while $H_X(s)$ has a band-pass characteristic but having a lossy behavior on its low-frequency band. Since we have designed $Q = 2$, the peak gain is expected as $Q^2 = 4 = 12.04$ dB
Fig. 13. (a) Transistor-level schematic, (b) half-circuit representation of the schematic, (c) \( g_m C \) equivalent circuit, and (d) small-signal diagram of the cross-coupled source-follower-based BPF [41].

\[
H_{XSF-BPF}(s) = \frac{C_{IN}}{s^2 + \frac{g_{m1}}{C_{IN}} + \frac{g_{m1} g_{m2}}{2 C_{IN}^2}}
\]

\[
\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_{IN}^2}}
\]

\[
Q = \sqrt{\frac{g_{m2}}{g_{m1}}}
\]

(22)

According to Fig. 3 which closely matches to 12.33 dB in our simulation result. The plotted \( G_{mX}(s) \) graph shows a BPF response which corresponds to the output of \( g_{m2} \) within the lossy integrator in Fig. 10(d), as also discussed in (7). This is because the \( V_Y \) node in (7) corresponds to the output of the second subtractor in Fig. 10(d). As the extracted DC operating point in our simulation shows \( g_{m2} = 253.2 \text{nS} \), the peak value of frequency response in \( G_{mX}(s) \) is expected as \( 4 \times 253.2 \text{nS} = 1012.8 \text{nS} \) where \( Q = 4 \) is considered according to (6, 7). This estimation also makes a close agreement with 923 nS from our simulation result. The center frequency \( f_0 \) can be estimated using (16) as follow,

\[
f_0 = \frac{\omega_0}{2\pi} = \frac{\sqrt{(253.2 \text{nS})^2}}{2\pi \sqrt{2 \times 1 \text{pF} \times 2 \times 4 \text{pF}}} = 10.07 \text{kHz}
\]

(24)

which also makes an agreement with 9.98 kHz from the simulation result in Fig. 12. The residual estimation errors may come from parasitic capacitance and insufficient \( g_m r_o \) as discussed in (19).

C. Cross-Coupled Source-Follower (Second-Order BPF)

Similarly to Fig. 7 [35], a BPF architecture with an external subtractor applied to a XSF was proposed in [41] as shown in Fig. 13. We use the same XSF circuit from Fig. 10 to describe the operating principle for consistency, despite a folded input stage was used in [41]. The circuit uses a CCIA [37] to subtract \( V_{LPF} \) from \( V_X \). The input ports of the OTA (\( V_Z \)) within a CCIA works as a virtual GND by the negative feedback. Therefore, the virtual GND nodes that also exist in the XSF (see Fig. 11(d)) can be reused. In effect, \( C_{IN} \) capacitors in Fig. 13(a) contribute to the following: (1) filtering capacitors of the XSF; (2) input capacitors of the CCIA. The XSF circuit uses \( C_1 = C_2 = C_{IN} \) to realize \( V_X - V_{LPF} \) equation within the CCIA, otherwise it forms a weighted addition, i.e., \( C_1 V_X - C_2 V_{LPF} \). We assume that the resistance of the pseudo-resistor is sufficiently large such that the associated AC-coupling high-pass cut-off frequency stays far smaller than \( \omega_0 \) in BPF. This allows us to omit pseudo-resistors in a small-signal \( g_m C \) equivalent circuit shown in Fig. 13(c). Based on
the nodal analysis below, we can derive the transfer function of the CCIA $H_{\text{CCIA}}(s)$.

$$
i_Z = [(v_X - v_Z) + (v_{\text{LPPF}} - v_Z)]sC_{\text{IN}}
\approx [v_Z - (v_{\text{LPPF}})]sC_F
\approx -g_{m3}v_Z = -v_{\text{BPF}}sC_L + (v_{\text{LPPF}} - v_Z)sC_F
$$

$$
H_{\text{CCIA}}(s) = \frac{v_{\text{LPPF}}}{v_X - v_{\text{LPPF}}} = \frac{v_{\text{LPPF}}}{1 + s\frac{C_L}{C_F}} \approx \frac{C_{\text{IN}}}{C_F} \quad (25)
$$

where $i_Z$ represents a small-signal current in Fig. 13(c), $C_L$ is a load capacitance of the CCIA. We assume $C_L \gg C_F$ and $s \ll g_{m3}/C_F$ for the first approximation in (25). We can see that the bandwidth of CCIA is reduced by the amount of feedback factor $\beta = C_F/(2C_{\text{IN}} + C_F)$ from the original OTA bandwidth $g_{m3}/C_L$, as also described in [37]. The second approximation used in (25) is valid when the bandwidth of CCIA is sufficiently higher than $\omega_0$ in the BPF. The transfer function of the XSF-based BPF $H_{\text{BPF}}(s)$ is derived in (22) using the equations as below. $H_{\text{LPPF}}(s)$ can be found in (16) but with an additional condition of $C_1 = C_2 = C_{\text{IN}}$.

$$
H_X(s) = \frac{H_{\text{LPPF}}(s)}{H_{\text{Lossy}}(s)} = H_{\text{LPPF}}(s) \left(1 + s\frac{C_{\text{IN}}}{g_{m2}}\right)
$$

$$
H_{\text{BPF}}(s) = (H_X(s) - H_{\text{LPPF}}(s))H_{\text{CCIA}}(s)
\approx s\frac{C_{\text{IN}}}{g_{m2}}H_{\text{LPPF}}(s) \cdot \frac{C_{\text{IN}}}{C_F} \quad (26)
$$

A clear advantage of the SF-based filters over the OTA-based is its minimal number of parasitic poles. As shown in Fig. 10(a), the XSF filter exploits every node with the circuit as a source for pole synthesis while the OTA-based circuit does not. For instance, the mirror pole in the OTA acts as a non-dominant pole thereby necessitating additional power dissipation to uphold the same bandwidth as in the SF filter. A parallel filter array adopting the XSF-based BPF was implemented in [41]; and was used in an environmental sound classification task [43] and a 2-class speech versus noise task [44] with an FPGA environment.

D. Super Source-Follower (Second-Order LPF/BPF)

Fig. 14 shows a schematic, $g_{m}C$ equivalent, and block diagram of the super source-follower (SSF)-based filter circuits. As Fig. 14(a) and (d) show, the SSF filter can be categorized into two different types depending on how the $C_1$ capacitor is connected: (1) $C_1$ bootstraps $V_{\text{BPF}}$ and $V_{\text{LPPF}}$ in type-I; (2) $C_1$ is connected to $V_{\text{BPF}}$ but its other plate is shunted to GND in type-II. In both types, the basic structure follows the lossless-first two-integrator-loop topology as discussed in Fig. 3(a). However, the type-II SSF incorporates a feedforward $g_{m1}$ path. The transfer functions and filter parameters of type-I and type-II SSF filters are summarized in (27, 28). Interestingly, both SSF types can be deployed as a BPF without requiring any external subtractor in contrast to the OTA-based (see Fig. 7) and XSF-based (see Fig. 13) BPFs. For the type-I SSF, this is because $C_1$ bootstraps $V_{\text{LPPF}}$ and $V_{\text{BPF}}$ within the lossless integral operation. In other words, the resulting small-signal voltage difference, i.e., $-g_{m1}(v_{\text{IN}} - v_{\text{LPPF}})sC_1$, is generated on top of the $V_{\text{LPPF}}$ node. In effect, the $V_{\text{BPF}}$ is located after the second subtractor which receives $V_{\text{LPPF}}$ as an operand, thereby $V_{\text{BPF}}$ corresponds to $V_1$ in Fig. 3(a). Note that the small-signal current generated from the $g_{m2}$ transistor does not contribute to the voltage difference over the $C_1$ capacitor since the source and sink ports of the $g_{m1}$ transistor are all tied to both plates of the $C_1$ capacitor. Assuming sufficiently large output impedance $r_o$ of the transistors, the small-signal current generated from the $M_1$ transistor flows entirely into the $C_1$ capacitor, resulting that the generated small-signal current is $\text{trapped}$ within the $M_1$-C1 loop (used in (30)). A similar phenomenon can be found in the noise contribution of cascode devices (see Chapter 7.4.4 in [38]).

A nodal analysis for calculating (27) according to Fig. 14(b) is given as below.

$$
g_{m1}(v_{\text{IN}} - v_{\text{BPF}}) = \frac{1}{sC_1} + v_{\text{BPF}} = v_{\text{LPPF}}
$$

$$
v_{\text{BPF}} = -g_{m2}v_{\text{BPF}} = \frac{1}{sC_2}
$$

For type-II SSF, the key enabler for achieving the BPF response is the $g_{m1}$ feedforward path. As discussed in (6) and Fig. 3(b), $V_{\text{X}}$ within the lossless-first two-integrator-loop topology has a lossy low-frequency behavior. However, the gain path from $v_{\text{IN}}$ to $V_{\text{BPF}}$ for calculating the transfer function $H_{\text{BPF}}(s)$ includes two different paths: (1) direct path $-g_{m1}/sC_1$; (2) loop around path $g_{m1}H_{\text{Lossy}}(s)g_{m1}/sC_1$ where $H_{\text{Lossy}}(s) = 1/(g_{m1} + sC_2)$. Since both paths have different polarities, they cancel out each other so that the lossy term in the numerator of (6), i.e., $\omega_1\omega_2$, is eliminated. A nodal analysis for calculating (28) according to Fig. 14(c) is given as below.

$$
v_{\text{BPF}} = -g_{m1}(v_{\text{IN}} - v_Z) = \frac{1}{sC_1}
$$

$$
v_{\text{Z}} = \left[g_{m1}(v_{\text{IN}} - v_Z) + (-g_{m2}v_{\text{BPF}})\right] \frac{1}{sC_2}
$$

Note that unlike type-I SSF, the remaining node ($V_2$) does not show a second-order LPF response. The transfer function $H_{\text{Z,II}}(s)$ of the type-II SSF is given as below.

$$
H_{\text{Z,II}}(s) = \frac{g_{m1}}{s^2 + \frac{C_1}{C_2} + \frac{g_{m1}g_{m2}}{C_1C_2} + \frac{g_{m1}}{C_1}s + \frac{g_{m2}}{C_2}}
$$

Since the transfer function has 1 pole in the numerator and 2 poles in the denominator, similarly to $H_X(s)$ in (6), it effectively shows a first-order low-pass response.

Our analysis on the type-I and type-II SSF filters are verified with an AC simulation as shown in Fig. 15. We set $I_{B2} = 2 \times I_{B1} = 20$ nA such that the same bias currents are distributed to $M_1/M_2$ transistors. Therefore, the transconduces for both transistors are closely set. $g_{m1} = 252.8$ nS and $g_{m2} = 227.3$ nS. Note that we keep the capacitance ratio as same as the XSF filter simulation shown in Fig. 12, thereby $Q$ can be designed as 2. As predicted in (27, 28), Fig. 15 shows that both type-I and type-II SSF filters when they are probed at $V_{\text{BPF}}$ have BPF responses. Their peak gains are 12.14 dB and 11.28 dB for type-I and type-II cases respectively, and close
to our estimated value of $Q^2 = 4 = 12.04 \text{ dB}$, which is also described in the XSF filter simulation. The simulated peak gain values of the two filters are different because the theoretical $Q$ equations are different as given by (27, 28) considering slightly different $g_m$ values for $M_1/M_2$. A second-order low-pass roll-off is observed with $H_{\text{LPF-I}}(s)$ and a first-order roll-off with $H_{\text{Z-II}}(s)$. The center frequencies of type-I/type-II SSF BPFs can be estimated using (27, 28) as below.

$$f_0 = \frac{\omega_0}{2\pi} = \sqrt{252.8 \text{ nS} \times 227.3 \text{ nS}} = 19.08 \text{ kHz} \quad (34)$$

which makes a close agreement with 19.05 kHz from the simulation result in Fig. 12. The type-II SSF-based BPF was implemented within a channel of a parallel filter bank feature extractor in [24]. Together with an on-chip multilayer perceptron (MLP) classifier, it implemented a VAD.

### E. Flipped Voltage Follower (Second-Order LPF/BPF)

Fig. 16 shows a schematic, $g_mC$ equivalent, and block diagram of the flipped voltage follower (FVF)-based filter circuits [46]. The FVF circuit has been actively used as a core building block in various analog circuits to name, such as LPF [45], low-dropout (LDO) regulator [47]–[49], bio-signal amplifier [50]–[55], and current driver [56], [57]. As of the case in the SSF filters, the FVF filters are also categorized into two types according to the connection methods of $C_1$ capacitor. Interestingly, the $g_mC$ equivalent circuits of the SSF and the FVF are the same except for the input polarity of $g_m$ transconductor (pFET gate in SSF, nFET gate in FVF). Since the inversion characteristic of $g_m$ transconductor still does not change, resultant block diagrams of the SSF and FVF are exactly same regardless of whether they are type-I or type-II. Therefore, the transfer functions of FVF filters described in (35), (36) are also the same as of the SSF filters (27), (28).

Fig. 17 shows an AC simulation result of the type-I and type-II FVF filter circuits. We set $I_B = 10 \text{ nA}$ and the resulting transconductances are $g_m1 = 262.4 \text{ nS}$ and $g_m2 = 262.5 \text{ nS}$. As expected, the transfer curves for $H_{\text{LPF-I}}$, $H_{\text{BPF-I}}$, $H_{\text{BPF-II}}$, and $H_{\text{Z-II}}$ show the same characteristic as we observed in the SSF simulation result (Fig. 15). The peak gains of type-I and type-II BPFs are 11.39 dB and 11.35 dB respectively, where their
12

Fig. 16. (a) Transistor-level schematic, (b) $g_m C$ equivalent, and (c) small-signal diagram of the type-I flipped voltage follower [45] and (d) transistor-level schematic, (e) $g_m C$ equivalent, and (f) small-signal diagram of the type-II flipped voltage follower [25].

\[
H_{FVF-LPF-I}(s) = \frac{g_{m1} g_{m2}}{s^2 + s \frac{g_{m2}}{C_2} + \frac{g_{m1} g_{m2}}{C_1 C_2}} \\
H_{FVF-BPF-I}(s) = \frac{-s \frac{g_{m1}}{C_1}}{s^2 + s \frac{g_{m2}}{C_2} + \frac{g_{m1} g_{m2}}{C_1 C_2}} \\
\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \\
Q = \sqrt{\frac{g_{m2} C_2}{g_{m1} C_1}} \tag{35}
\]

\[
H_{FVF-BPF-II}(s) = \frac{-s \frac{g_{m1}}{C_1}}{s^2 + s \frac{g_{m1}}{C_2} + \frac{g_{m1} g_{m2}}{C_1 C_2}} \\
\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \\
Q = \sqrt{\frac{g_{m2} C_2}{g_{m1} C_1}} \tag{36}
\]

Fig. 17. Simulated frequency responses of FVF filter.

The center frequency is observed as 20.89 kHz. The simulated filter parameters are in close agreement with our estimation using (35) and (36), $Q^2 = 4 = 12.04 \text{ dB}$ and

\[
f_0 = \frac{\omega_0}{2\pi} = \frac{\sqrt{262.4 \text{nS} \times 262.5 \text{nS}}}{2\pi \sqrt{2 \pi^2 \text{pF}^2 \times 4 \text{pF}^2}} = 20.86 \text{kHz} \tag{37}
\]

A significant advantage of the FVF over the SSF is its power efficiency in terms of bandwidth. More specifically, as shown in Fig. 15 and Fig. 17, the FVF consumes 2× less current ($I_B = 10 \text{nA}$) while the SSF consumes $I_B = 20 \text{nA}$ to achieve $\omega_0 = 20 \text{kHz}$ for $C_2 = 4 \times C_1 = 4 \text{pF}$. This is because the tail current $I_{B2}$ in the SSF is divided into two different bias currents, $I_{B1}$ and $I_{B2} - I_{B1}$, for $g_{m1}$ and $g_{m2}$ respectively. On the contrary, the FVF exploits its inherent current reusing nature to save the power. More importantly, the FVF circuit offers better matching over the SSF, not merely because of the single branch biasing, but also of the same transistor type. For example, $M_1$ and $M_2$ transistors are all nFET in the FVF while it is not the case in the SSF. As a result, the FVF circuit is more robust over process variation because it is difficult to match different transistor types especially in regards to the shallow trench isolation (STI) and well proximity effect (WPE) [58].

The type-II FVF-based BPF was implemented as a parallel audio FEx for a VAD IC in [25].

VI. SUMMARY AND OUTLOOK

Table I summarizes the audio feature extractor (FEx) ICs reported for edge artificial intelligence (AI) tasks such as VAD and KWS. To date, both analog and digital FExs have been used in audio edge devices. An analog FEx can be categorized as a CT or discrete-time (DT) filter while a CT filter can be designed using voltage-domain or time-domain circuits. Here, the Time-Domain means the signals are processed using pulse-width modulation (PWM) or pulse-frequency modulation (PFM)-based circuits. Note that it is still a CT signal which is not sampled by a clock running at a known frequency. For instance, a time-to-digital converter (TDC), which is widely used in phase-locked loops (PLLs) [64] and time-of-flight (ToF) [65] sensors, converts an Analog time-domain PWM input signal into a sampled and quantized Digital output.
The CT voltage-domain filter discussed in Section IV-B is combined with a rectifier and a spike generation stage to form a cochlea channel leading to the multi-channel Dynamic Audio Sensor (DAS) silicon cochlea [6]. This design has been used in applications such as sound source localization [15], [66] using the spike timing of the binaural spikes from the DAS. It was also used for multi-modal recognition [18], [67], and keyword spotting using deep neural networks (DNNs) [16], [19]. The latest CT voltage-domain filter circuits show sub-µW ultra-low-power consumption [23]–[25], [27], [41], by mainly exploiting the outstanding power efficiency of SF-based filters operating in subthreshold as discussed in Section V.

However, as shown in Section V-A with Eq. (19), the core strength of the SF-based filter is the intrinsic feedback within the circuit. Unfortunately, the loop gain starts to degrade as technology scales, leading to a higher output non-linearity assuming the transistor size also scales. In addition, the reduced voltage headroom mainly caused by faster $V_{TH}$ scaling than $V_{DD}$, is expected to further complicate the analog filter design forcing IC designers to bring concessions in circuit performances. To this end, an analog FEx that uses the time-domain processing technique is recently reported in [26].

In contrast to the voltage-domain designs, the building blocks of the time-domain processing circuits are based on logic gates and thus it can potentially provide better technology scaling. In addition, it is also expected to be developed towards a fully-synthesizable analog FEx where the layout is automatically generated from the register-transfer level (RTL) hardware description language. Examples of synthesizable analog circuits include all-digital phase-locked loop (ADPLL) [68] and ring-oscillator-based $\Delta \Sigma$ ADC [69].

Although not discussed in this paper, the DT voltage-domain filter circuits are also promising candidates. This is because the center frequency of the BPF is controlled by the frequency of an external clock, rather than $g_m$ of the transconductors, therefore $\omega_0$ can be precisely controlled over process, voltage, and temperature (PVT) variations. A chopper-based mixer with a sequentially varying clock frequency and a subsequent LPF stage was used in [59] where its operational principle is similar to that of lock-in amplifiers, also commonly used in bio-impedance sensors [52], [70]. This architecture achieved a 60 nW ultra-low-power consumption, however, because it sequentially demodulates over the desired frequency band, it cannot perform the filtering operation over its entire frequency range at once. Therefore, this design showed a 512 ms latency until a set of filtered data is collected such that a frequency-selective feature vector to be available. Alternatively, the switched-capacitor (SC) BPFs were developed in [60], [61] with a parallel filter bank approach. As typically considered in $\Delta \Sigma$ [71] and successive approximation register (SAR) [72] ADC designs, the synchronous SC operation comes with $kT/C$ noise-aliasing due to the DT sample-and-hold. This attribute necessitates an anti-aliasing filter and also a buffer stage ahead of the SC filter both of which incur additional power and

| Paper | Filter Type | Process (nm) | Filter Bank | Power | Area (mm$^2$) | Task (# of Classes) | Dataset | Classifier |
|-------|-------------|--------------|-------------|-------|--------------|---------------------|---------|------------|
| TBioCAS 2014 [6] | Analog Voltage (90 nm) | 350 | 2×64×4 Ch 50Hz-50kHz | 14 mW$^A$ | 13.74 | Speech Recognition (12) | TIDIGITS | FFPA RNN |
| JSSC 2016 [41] | Analog Voltage (90 nm) | 180 | 2×64 Ch 8Hz-20kHz | 55 µW | 33.28 | Speech vs Noise (2) | TIMIT MS-SNSD MUSAN | Software MLP |
| JSSC 2016 [23] | Analog Voltage (90 nm) | 90 | 16 Ch 75Hz-5kHz | 6 µW | 2 | VAD (2) | NOIZEUS | On-Chip Decision Tree |
| JSSC 2019 [24] | Analog Voltage (90 nm) | 180 | 16 Ch 100Hz-5kHz | 60 nW | 1.6 | VAD (2) | AuroraDEMAND | On-Chip MLP |
| JSSC 2021 [25] | Analog Time (OSC) | 65 | 16 Ch 100Hz-5kHz | 52 nW | 0.9 | VAD (2) | AuroraDEMAND GSCD | On-Chip MLP (VAD) Software CNN (KWS) |
| JSSC 2021 [27] | Analog Time (OSC) | 65 | 16 Ch 0Hz-1kHz | 109 nW | 0.72 | KWS (5) | HeySnips GSCD | On-Chip MLP |
| JSSC 2022 [26] | Digital (FFT) | 180 | 64 Ch 0Hz-1kHz | 9.3 µW | 1.6 | KWS (12) | GSCD | On-Chip RNN |
| JSSC 2019 [59] | Analog Voltage (Mixer) | 16-48 Ch 75Hz-4kHz | 60 nW | 0.55$^B$ | VAD (2) | LibriSpeech NOISEX-92 | On-Chip MLP |
| TCAS-I 2021 [60] | Analog Voltage (SC) | 130 | 32 Ch 30Hz-8kHz | 800 nW | 0.79 | KWS (12) | GSCD | Software CNN |
| SSC-L 2022 [61] | Analog Voltage (SC) | 65 | 6 Ch 20Hz-4kHz | 150 nW | 0.84 | KWS (3) | GSCD | Simulation MLP |
| TCAS-I 2019 [62] | Digital (FFT) | 28 | 40 Ch 0Hz-8kHz | 9.19 µW$^C$ | 0.08$^C$ | KWS (2) | TIDIGITS | On-Chip CNN |
| VLSI 2019 [20] | Digital (FFT) | 65 | 20 Ch 0Hz-8kHz | 7.33 µW$^C$ | 0.96$^B$ | KWS (12) | GSCD | On-Chip RNN |
| JSSC 2021 [63] | Digital (FFT) | 28 | 10 Ch 0Hz-4kHz | 340 nW | 0.05$^B$ | KWS (2-5) | GSCD | On-Chip CNN |

$A$ This number includes power consumption of the microphone pre-amplifier and test circuits.

B Estimated from chip photograph.

C Estimated from power/area breakdown.
area [72], although they were not actually implemented in [60], [61]. With this DT sample-and-hold environment, capacitance must be increased to reduce the $kT/C$ noise, but this choice comes with a larger capacitor area, a higher switching power of the SC operation, and a higher capacitive driving strength required for the front-end buffer stage which results in higher power consumption. Note that the work in [60] adopted high-density and low-leakage ferroelectric capacitors to realize a low silicon area but it is typically unavailable in standard CMOS process [73]. Also note that cascading approach of a LPF and a high-pass filter (HPF) to build a SC-BPF, adopted in [61], exhibited a limited $Q$ factor ($\leq 0.5$) as discussed in Fig. 4 and Eq. 9.

There are approaches to optimize the FFT-based digital FE\textsuperscript{x} design to reduce the power consumption toward sub-\mu\textit{W}. These designs implemented either a FFT [62], [63] or a discrete Fourier transform (DFT) [20] computation unit and this is typically followed by Mel filtering and logarithmic compression circuits. The work reported in [20] implemented a full signal chain starting from the analog front-end (AFE) consisting of a resistive voltage amplifier and a 10-bit SAR ADC, to the digital back-end with an RNN-based classifier. These blocks consume 16.1\mu\textit{W} power for the KWS whereas the FE\textsuperscript{x} alone consumed 7.33\mu\textit{W} (40\% of total power). The serialized FFT approach reduced FE\textsuperscript{x} power down to only 340\textit{nW} [63], however, it relied on an off-chip 16-bit ADC which incurs additional power and area. Note that the state-of-the-art 16-bit $\Delta\Sigma$ modulator with a 5kHz bandwidth (close to 4kHz used in [63]) already consumes 4.5\mu\textit{W} [74], [75] and this power number did not even account for the decimation filter stage which is an essential building block for the $\Delta\Sigma$ modulators to eliminate high-pass shaped quantization noise. Therefore, it should be noted that the actual power number of the 16-bit ADC will be higher than 4.5\mu\textit{W} in edge audio devices operated in the real world.

Over a range of CT voltage-domain analog filters discussed in this paper, we may conclude that the FVF-based second-order filter is the best option to be adopted for implementing edge audio devices, considering its power-efficiency in terms of bandwidth and design compactness which can potentially lead to better matching property.

The developed design strategies of audio FE\textsuperscript{x} circuits can be applied to other similar application fields such as in-sensor processing biomedical ICs. For instance, the digital finite impulse response (FIR) BPFs implemented in an ultra-low-power electrocardiogram (ECG) processor [76], consumed the largest power of the entire chip. Since this work also required an off-chip 13-bit ADC, an analog FE\textsuperscript{x} can potentially be a better design choice because we can bypass the ADC and perform the frequency-selective filtering operation on the input ECG signal. Another application area of the analog FE\textsuperscript{x} is in electroencephalogram (EEG)-based brain-computer interface. The authors in [77] developed an in-ear sensor IC that uses the auditory steady-state response (ASSR) which is extracted from a raw EEG signal. Because this work implemented an amplifier and ADC only and the subsequent post-processing stages were developed in software, on-chip integration of the entire processing chain from the analog FE\textsuperscript{x} to the DNN classifier will also be an interesting area for the future.

VII. CONCLUSION

This paper introduces an overview of continuous-time analog filters which have been used for audio edge intelligence applications. A unified analysis of second-order voltage-domain filters using the two-integrator-loop interpretation is presented. With a review of several filter architectures ranging from the OTA-based to source-follower-based designs, $g_mC$ equivalents and small-signal diagrams are summarized. The derived transfer functions are also verified with the transistor-level simulations. We provide a summary of the state-of-the-art audio feature extraction circuits that have been used for edge audio tasks. Each type of feature extractor is discussed, including its current challenges and design advantages. This analysis can be also applied to any areas that use front-end analog filters such as brain-computer interface, neuroprosthesis, wearable/hearable sensors, and other biomedical applications.

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