T-count Optimized Quantum Circuits for Bilinear Interpolation

Edgard Muñoz-Coreas, Himanshu Thapliyal
Department of Electrical and Computer Engineering
University of Kentucky, Lexington, KY
Email: hthapliyal@uky.edu

Abstract—Quantum circuits for basic image processing functions such as bilinear interpolation are required to implement image processing algorithms on quantum computers. In this work, we propose quantum circuits for the bilinear interpolation of NEQR encoded images based on Clifford+T gates. Quantum circuits for the scale up operation and scale down operation are illustrated. The proposed quantum circuits are based on quantum Clifford+T gates and are optimized for T-count. Quantum circuits based on Clifford+T gates can be made fault tolerant but the T gate is very costly to implement. As a result, reducing T-count is an important optimization goal. The proposed quantum bilinear interpolation circuits are based on (i) a quantum adder, (ii) a proposed quantum subtractor, and (iii) a quantum multiplication circuit. Further, both designs are compared and shown to be superior to existing work in terms of T-count. The proposed quantum bilinear interpolation circuits for the scale down operation and for the scale up operation each have a 92.52% improvement in terms of T-count compared to the existing work.

I. INTRODUCTION

Quantum computing has promising applications in number theory, encryption, search, scientific computation and image processing. For example quantum algorithms have been proposed for image orientation problems, image pattern recognition and image template matching [1][2]. Quantum image representations and image manipulation are required in the quantum circuit implementations of image processing quantum algorithms. Thus, researchers have proposed quantum image representations such as the Flexible Representation of Quantum Images (FRQI) [3] and the Novel Enhanced Quantum Representation (NEQR) [4]. Further, quantum circuits for image operations such as translation, geometric transformation and bilinear interpolation have also been developed [5][6][7]. If these quantum circuits are based on Clifford+T gates, they can be made fault tolerant with error correcting codes permitting reliable and scalable quantum computation [8][9][10][11][12]. The Clifford+T gate family is illustrated in [8]. The T gate is very costly to implement compared to the Clifford gates making T-count an important optimization goal [9][8][10][11][12].

The design of quantum circuits for operations such as interpolation for NEQR images has been addressed in the literature [5]. The existing bilinear interpolation quantum circuits are based on (i) a quantum subtractor, (ii) a quantum addition circuit, (iii) a quantum multiplication circuit, and (iv) a quantum division circuit. The work in [5] also proposes a color information retrieval scheme based on quantum oracles operating as lookup tables. While an interesting design, the bilinear interpolation circuits in [5] suffers from significant T gate cost because the design is based on quantum arithmetic circuits that have high T-count. Further, the circuits suffer from added overhead due to extra quantum arithmetic operations which can be minimized.

To overcome the limitations of the existing designs, this work presents quantum circuits for bilinear interpolation of NEQR encoded images based on Clifford+T gates. Quantum circuits for the scale up operation and scale down operation are illustrated. The proposed quantum bilinear interpolation circuits are based on: (i) a quantum adder, (ii) a proposed quantum subtractor and (iii) a quantum multiplication circuit. The proposed quantum bilinear interpolation circuits do not require a quantum division circuit. The proposed quantum bilinear interpolation circuits are compared and shown to be superior to the existing work in terms of T-count and number of arithmetic units used. This paper is organized as follows: Section II discusses the Clifford+T gate set and discusses the novel enhanced quantum representation (NEQR). Section III illustrates the quantum adder, proposed quantum subtractor and quantum multiplication circuit used in the proposed bilinear interpolation circuits. In Section IV the design of the proposed quantum bilinear interpolation circuit for the scale down operation is presented and compared to the existing work. Lastly, in Section V the design of the proposed quantum bilinear interpolation circuit for the scale up operation is presented and compared to the existing work.

II. BACKGROUND

A. Quantum Gates

Fault tolerant implementation of quantum circuits is of interest to researchers because physical quantum computers are prone to noise errors [8][9][12]. Recently, researchers have implemented quantum logic gates and circuits with the Clifford+T gate set because they can be made fault tolerant [8][9][10][11][12]. The set of gates that make up the Clifford+T gate family is illustrated in [8]. The bilinear interpolation circuits proposed in this work are composed of the NOT gate, the Feynman (CNOT) gate, the temporary logical- AND gate
and uncomputation gate. The CNOT gate and the NOT gate are in the set of gates that make up the Clifford+T gate family [8]. The temporary logical-AND gate and uncomputation gate must be constructed from Clifford+T gates and are presented in [14]. These gates are based on the designs in [13]. The temporary logical-AND gate is a 3 input, 3 output logic gate and has the mapping \(A, B, A \cdot B \rightarrow A, B, A \cdot B\). The Clifford+T gate implementation of the temporary logical-AND gate is shown in Figure 1a. The input labeled \(A\) in Figure 1a is an ancillae in the state shown in expression (1):

\[
\frac{1}{\sqrt{2}} \left( |0\rangle + e^{\frac{i\pi}{4}} |1\rangle \right)
\]

By using the ancillae set to \(A\), the temporary logical-AND gate designed in [14] can be realized on three qubits instead of four [14].

The uncomputation gate is a 3 input, 3 output logic gate and has the mapping \(A, B, A \cdot B \rightarrow A, B, 0\). The third input qubit can be restored to an ancillae after measurement for use in later computation. The Clifford+T gate implementation of the uncomputation gate is shown in Figure 1b. A Toffoli gate can be realized from the temporary logical-AND gate and uncomputation gate [13]. The Toffoli gate implementation is shown in Figure 2.

Evaluating quantum circuit performance in terms of the number of T gates (T-count) is of interest because the fault tolerant implementation of the T gate is significantly more costly than the fault tolerant implementation costs of the other Clifford+T gates [9] [8] [10] [11] [12]. By using the logical-AND gate and the uncomputation gate to realize quantum arithmetic circuits, our proposed bilinear interpolation circuits reduce the number of T gates used.

B. Novel Enhanced Quantum Representation (NEQR)

An image must be represented as qubits. Researchers have proposed several methods to represent both color and greyscale images on a quantum computer [3] [4]. In this work, we use the Novel Enhanced Quantum Representation (NEQR) presented in [4]. NEQR is a means to represent greyscale images on a quantum computer. For a given image, each pixel is represented with expression (2):

\[
|Y\rangle|X\rangle|C\rangle
\]

Where \(|Y\rangle\) and \(|X\rangle\) are quantum registers that contain the \(x\) and \(y\) coordinates of the image and \(|C\rangle\) contains the greyscale color of the pixel. Quantum registers \(|Y\rangle\) and \(|X\rangle\) are of size \(n\) and the color information quantum register \(|C\rangle\) is of size \(q\) to store the needed color information [4] [5]. NEQR improves the existing encoding scheme FRQI (Flexible Representation of Quantum Images) because the image color information is represented as multiple qubits in the computational basis as opposed to a single qubit in superposition. NEQR benefits from faster image preparation, accurate color measurement and easier implementation of quantum image processing circuits compared to FRQI [4].

III. DESIGN OF QUANTUM CIRCUITS USED IN PROPOSED BILINEAR INTERPOLATION CIRCUITS

The proposed quantum bilinear interpolation circuits are based on: (i) a quantum adder, (ii) a proposed quantum subtractor and (iii) a quantum multiplication circuit. The circuit designs of the quantum adder, quantum subtractor and quantum multiplier are discussed below:

- **Quantum Adder:** We use the quantum ripple carry adder presented in [14] in this work. The quantum adder is based on the ripple carry adder design in [15]. The quantum circuit takes two \(n\) bit inputs \(A\) and \(B\). At the end of computation, the input \(A\) emerges unchanged and the input \(B\) is transformed to the sum \(B + A\). The quantum adder saves \(T\) gates by using the logical-AND gate and the uncomputation gate implementations shown in Section III. The design of the quantum addition circuit is illustrated in [13].

- **Proposed Quantum Subtractor:** We propose a quantum subtraction circuit in this work. The proposed quantum subtraction circuit is shown in Figure 3.
To save $T$ gates, the proposed quantum subtraction circuit is based on the quantum ripple carry adder presented in [14]. To get the ripple carry adder to perform subtraction, we use the design approach presented in [16]. As shown in Figure 3, the input $B$ is complemented before being applied to the quantum ripple carry adder. Thus, the ripple carry adder calculates $B + A$. Afterward, the qubits that originally held $B$ are complemented again. As a result, the quantum subtractor calculates $(B + A)$ at the end of computation. $(B + A)$ is equivalent to $B - A$ [16]. While the example in Figure 3 is sized for 4 qubit operands, the proposed quantum subtraction circuit design can be extended to any operand size.

**Quantum Multiplier:** We use the quantum integer multiplication circuit presented in [17] in this work. The quantum multiplication circuit takes two $n$ bit inputs $a$ and $b$. At the end of computation, the inputs $a$ and $b$ emerges unchanged and the product $b \cdot a$ is generated on ancilla. To save $T$ gates, we use the conditional adder presented in [14] in the multiplication circuit. The quantum conditional adder circuit described in [14] takes two $n$ bit inputs $a$ and $b$ and a 1 bit input control. When the control = 1, the circuit calculates $b + a$ and when control = 0 the circuit performs no computation.

**Design of the Proposed Bilinear Interpolation Circuit for the Scale Down Operation**

The proposed quantum circuit for bilinear interpolation is shown in Figure 4 for the case of a scaling down an image by an integer value $n$. Scaling down an image by an integer value $n$ results in reducing the original $y$ and $x$ positions of each pixel by $2^n$. Inputs to the proposed quantum circuit is the original pixel positions $y$ and $x$ stored in $m$ bit quantum registers $|Y\rangle$, $|X\rangle$, respectively, along with the corresponding original pixel color information $C_{Y,X}$ stored in quantum register $|C_{Y,X}\rangle$. Inputs also include the pixel color information for adjacent pixels at locations $(y+1, x)$, $(y, x+1)$ and $(y+1, x+1)$. The color information for these adjacent pixels are stored in quantum registers $|C_{Y+1,X}\rangle$, $|C_{Y,X+1}\rangle$ and $|C_{Y+1,X+1}\rangle$ respectively. At the end of computation, the circuitry returns the position information for the scaled pixel in quantum registers $|\bar{Y}\rangle$ and $|\bar{X}\rangle$ as well as the corresponding color of the scaled pixel in quantum register $|C_{\bar{Y},\bar{X}}\rangle$.

Our proposed design calculates the position information for the scaled pixel without quantum gates. To reduce an image by a value $n$, the original position value is divided by $2^n$. We accomplish this division by assigning the values at locations $|Y_{m-1}\rangle$ through $|Y_0\rangle$ of quantum register $|Y\rangle$ and locations $|X_{m-1}\rangle$ through $|X_0\rangle$ of quantum register $|X\rangle$ to the output position registers $|\bar{Y}\rangle$ and $|\bar{X}\rangle$, respectively. Thus, we eliminate the need to use a division circuit.

To calculate the color information for the scaled pixel, our proposed quantum circuit must perform the calculation shown in equation 3

$$
\begin{bmatrix}
(2^n - (Y \cdot 2^n - Y)) \cdot (2^n - (X \cdot 2^n - X)) \cdot C_{Y,X} + \\
(2^n - (\bar{Y} \cdot 2^n - Y)) \cdot (2^n - (\bar{X} \cdot 2^n - X)) \cdot C_{Y+1,X} + \\
(2^n - (\bar{Y} \cdot 2^n - Y)) \cdot (2^n - (\bar{X} \cdot 2^n - X)) \cdot C_{Y+1,X+1}
\end{bmatrix} \div 2^n
$$

Where $(\overline{Y} \cdot 2^n - Y)$ corresponds to locations $|Y_{n-1}\rangle$ through $|Y_0\rangle$ of quantum register $|Y\rangle$ and $(\overline{X} \cdot 2^n - X)$ corresponds to locations $|X_{n-1}\rangle$ through $|X_0\rangle$ of quantum register $|X\rangle$.

To perform this computation, the proposed bilinear interpolation circuit requires a quantum multiplication circuit, a quantum addition circuit and a quantum subtraction circuit. Our circuit computes equation 3 by executing the following algorithm:

1. **Step 1:** Copy $(Y \cdot 2^n - Y)$ and $(X \cdot 2^n - X)$ to ancillae with CNOT gates.
2. **Step 2:** Calculate $2^n - (Y \cdot 2^n - Y)$ and $2^n - (X \cdot 2^n - X)$ with quantum subtraction circuits.
3. **Step 3:** Calculate the products $(2^n - (Y \cdot 2^n - Y)) \cdot (2^n - (X \cdot 2^n - X))$, $\bar{Y} \cdot 2^n - Y) \cdot (2^n - (\bar{X} \cdot 2^n - X))$ and $2^n - (\bar{Y} \cdot 2^n - Y) \cdot (\bar{X} \cdot 2^n - X)$ with quantum multiplication circuits.
4. **Step 4:** Calculate the product terms $(2^n - (Y \cdot 2^n - Y)) \cdot (2^n - (X \cdot 2^n - X)) \cdot C_{Y,X}$, $(\bar{Y} \cdot 2^n - Y) \cdot (2^n - (\bar{X} \cdot 2^n - X)) \cdot C_{Y+1,X}$ and $(2^n - (\bar{Y} \cdot 2^n - Y)) \cdot (\bar{X} \cdot 2^n - X) \cdot C_{Y+1,X+1}$ with quantum multiplication circuits.
5. **Step 5:** Complete the calculation of equation 3 with quantum addition circuits.

The values at locations $2 \cdot n - 1$ through 0 of the quantum register with the result of Step 5 are not a part of the new pixel’s color information $|C_{\bar{Y},\bar{X}}\rangle$. By not assigning these locations to the quantum register containing the new pixel’s color information $|C_{\bar{Y},\bar{X}}\rangle$ we eliminate the need to use quantum division circuits. The remaining locations are the new pixel’s color information $|C_{\bar{Y},\bar{X}}\rangle$ and will be assigned to the quantum register containing the new pixel’s color information $|C_{\bar{Y},\bar{X}}\rangle$.  

![Fig. 3: Proposed quantum subtraction circuit for four qubit operands.](image)
The image is scaled down by a value $n$.

**TABLE I: Comparison of the Bilinear Interpolation Circuits for the Scale Down Operation in Terms of Number of Functional Blocks Used**

| Component    | 1   | proposed |
|--------------|-----|----------|
| Adder        | 3   | 3        |
| Subtracter   | 4   | 2        |
| Divider      | 2   | 0*       |
| Multiplier   | 8   | 8        |

* is the design in [5].

A. Cost Analysis of the Proposed Bilinear Interpolation Circuit for the Scale Down Operation

Table I shows the comparison between the proposed quantum circuit for bilinear interpolation and the existing work in terms of total number of arithmetic operations. Through careful layout of functional blocks in our proposed quantum circuit for bilinear interpolation we remove 2 quantum subtraction circuits from our design. By not assigning locations $2 \cdot n - 1$ through 0 of the quantum register containing the result of equation 2 to the quantum register containing the new pixel’s color information $C_{Y,X}$ we eliminate the need to use quantum division circuits.

Comparison of the T-count between the proposed quantum bilinear interpolation circuit for the scale down operation and the existing work in [5] is shown in Table I. The design in [5] has a T-count of order $O(n^2)$. The proposed design’s T-count is of order $O(n^2)$. To calculate the T-count of the existing design in [5], we determined the T-counts for the quantum circuits used in the design. We determined that to calculate equation 3 the design in [5] uses a quantum addition circuit with a T-count of $28 \cdot n - 14$, a quantum subtraction circuit with a T-count of $28 \cdot n - 14$, a quantum multiplication circuit with a T-count of $7 \cdot n^2 + \sum_{i=1}^{\log_2(n)} \frac{n}{2^i} \cdot (14 \cdot (n + i - 2^{i-1}) - 14)$ and a quantum division circuit with a T-count of $\approx 400 \cdot n^2$. We compute the T-count for the proposed work and the existing design by multiplying the T-count for each quantum functional block by the number of times it is used and then sum the result. Table I shows the number of functional blocks used by the design in [5].

Table I shows that the proposed quantum circuit for bilinear interpolation have an improvement ratio of $\approx 92.52\%$ in terms of T-count when performing the scale down operation. Our proposed quantum bilinear interpolation circuits save T gates by (i) using T gate efficient functional blocks and (ii) reducing the number of required functional blocks to calculate the new pixel’s color information (see equation 5). Our proposed designs are based on the quantum arithmetic circuits illustrated in Section III. As a result, our proposed bilinear interpolation quantum circuit is based on a quantum addition circuit with a T-count of $4 \cdot n$, a novel quantum subtraction circuit with a T-count of $4 \cdot n - 4$ and a quantum multiplication circuit with a T-count of $8 \cdot n^2 - 4 \cdot n$.

V. DESIGN OF THE PROPOSED BILINEAR INTERPOLATION CIRCUITS FOR THE SCALE UP OPERATION

The proposed quantum circuit for bilinear interpolation is shown in Figure 5 for the case of a scaling up an image by an integer value $n$. Scaling up an image by an integer value $n$ results in increasing the original $y$ and $x$ positions of each pixel by $2^n$. Inputs to the proposed quantum circuit is the original pixel positions $y$ and $x$ stored in quantum registers $|Y\rangle, |X\rangle$, respectively, along with the corresponding original pixel color information $C_{Y,X}$ stored in quantum register $|C_{Y,X}\rangle$. Inputs also include the pixel color information for adjacent original pixels at locations $(y+1, x), (y, x+1)$ and $(y+1, x+1)$. The color information for these adjacent pixels are stored in quantum registers $|C_{Y+1,X}\rangle, |C_{Y,X+1}\rangle$ and $|C_{Y+1,X+1}\rangle$ respectively. At the end of computation, the circuitry returns the position information for the scaled pixel in quantum registers $|\bar{Y}\rangle$ and $|\bar{X}\rangle$ as well as the corresponding color of the scaled pixel in quantum register $|C_{\bar{Y},\bar{X}}\rangle$.

To scale up an image by a value $n$, the position value is multiplied by $2^n$. By concatenating $n$ ancilla set to 0 to quantum registers $|X\rangle$ and $|Y\rangle$ such that they have the values $X_{m-1} \cdots X_0 0 \cdots 0$ and $Y_{m-1} \cdots Y_0 0 \cdots 0$ we eliminate the need to use a quantum multiplication circuit. These combined registers now contain the position information $\bar{Y}$ and $\bar{X}$, respectively, for the scaled up pixel.

To calculate the color information for the scaled pixel, our proposed quantum circuit must calculate equation 4.
TABLE II: T Gate Comparison of the Bilinear Interpolation Circuits for the Scale Down Operation

| T-count | % impr. w.r.t. 1 |
|---------|-----------------|
| 1       | \(856 \cdot n^2 + 196 \cdot n - 98 + 8\cdot \sum_{i=1}^{(log_2(n))} \frac{n}{2^i} \cdot (14 \cdot (n + i-2^{i-1}) - 14)\) · |
| Proposed | \(64 \cdot n^2 - 12 \cdot n - 8\) | \(\approx 92.52\%\) |

1 is the design in [5]

Table III shows the comparison between the proposed quantum circuit for bilinear interpolation and the existing work in terms of total number of arithmetic operations. Through

**Quantum Circuit for Bilinear Interpolation**

The proposed quantum bilinear interpolation circuit requires a quantum multiplication circuit, a quantum addition circuit, and a quantum subtraction circuit.

Our circuit computes equation (4) by executing an algorithm identical to the proposed scale down circuit. The algorithm our quantum bilinear interpolation circuit for the scale up operation implements is as follows:

1. Step 1: Copy \(\frac{Y}{2^n}\) and \(\frac{X}{2^n}\) to ancillae with CNOT gates.
2. Step 2: Calculate \(2^m - \frac{Y}{2^n}\) and \(2^m - \frac{X}{2^n}\) with quantum subtraction circuits.
3. Step 3: Calculate the products \(\left(2^m - \frac{Y}{2^n}\right) \cdot \left(2^m - \frac{X}{2^n}\right)\), \(\left(\frac{Y}{2^n}\right) \cdot \left(2^m - \frac{X}{2^n}\right)\), \(\left(\frac{X}{2^n}\right) \cdot \left(2^m - \frac{Y}{2^n}\right)\), and \(\left(\frac{Y}{2^n}\right) \cdot \left(\frac{X}{2^n}\right)\) with quantum multiplication circuits.
4. Step 4: Calculate the product terms \(2^m - \frac{Y}{2^n}\) \(\cdot\) \(C_{Y,X}\), \(\left(\frac{Y}{2^n}\right) \cdot \left(2^m - \frac{X}{2^n}\right) \cdot C_{Y,X}\), \(\left(\frac{X}{2^n}\right) \cdot \left(2^m - \frac{Y}{2^n}\right) \cdot C_{Y,X}\), and \(\left(\frac{X}{2^n}\right) \cdot \left(\frac{Y}{2^n}\right) \cdot C_{Y,X}\) with quantum multiplication circuits.
5. Step 5: Complete the calculation of equation (4) with quantum addition circuits.

The values at locations \(2 \cdot m - 1\) through 0 of the quantum register with the result of Step 5 are not a part of the new pixel’s color information \(C_{Y,X}\). By not assigning these locations to the quantum register containing the new pixel’s color information \(C_{Y,X}\), we eliminate the need to use quantum division circuits. The remaining locations are the new pixel’s color information \(C_{Y,X}\) and will be assigned to the quantum register containing the new pixel’s color information \(C_{Y,X}\).

**A. Cost Analysis of the Proposed Bilinear Interpolation Circuit for the Scale Up Operation**

**TABLE III: Comparison of the Bilinear Interpolation Circuits for the Scale Up Operation in Terms of Number of Functional Blocks Used**

| Component     | 1 proposed |
|---------------|------------|
| Adder         | 3          |
| Subtractor    | 4          |
| Divider       | 2          |
| Multiplier    | 8          |

1 is the design in [5]

* Our proposed design does not require a divider.
careful layout of functional blocks in our proposed quantum circuit for bilinear interpolation we remove 2 quantum subtraction circuits from our design. Further, by not assigning locations \(2m - 1\) through 0 of the quantum register containing the new pixel’s color information \(C_{Y,N}\) we eliminate the need to use quantum division circuits.

Comparison of the T-count between the proposed quantum bilinear interpolation circuit for the scale up operation and the existing work in [5] is shown in Table IV. The design in [5] has a T-count of order \(O(n^2)\). The proposed design’s T-count is of order \(O(n^2)\). To calculate the T-count of the existing design in [5], we determined the T-counts for the quantum circuits used in the design. We determined that to calculate equation (3) the design in [5] uses a quantum addition circuit with a T-count of \(28 \cdot n \cdot 14\), a quantum subtraction circuit with a T-count of \(28 \cdot n - 14\), a quantum multiplication circuit with a T-count of \(7 \cdot n^2 + \sum_{i=1}^{\log_2(n)} 14 \cdot (n + i \cdot 2^{-i-1}) - 14\), \(8 \cdot n^2 - 4 \cdot n\) and a quantum division circuit with a T-count of \(\approx 400 \cdot n^2\). We compute the T-count for the proposed work and the existing design by multiplying the T-count for each quantum functional block by the number of times it is used and then sum the result.

Table IV shows that the proposed quantum circuit for bilinear interpolation has an improvement ratio of \(\approx 92.52\%\) in terms of T-count when performing the scale up operation. Our proposed quantum bilinear interpolation circuit reduces T-count by (i) using T-gate efficient functional blocks and (ii) reducing the number of required functional blocks to calculate the new pixel’s color information (see equation 3). Our proposed designs are based on the quantum arithmetic circuits illustrated in Section III. As a result, our proposed bilinear interpolation quantum circuit is based on a quantum addition circuit with a T-count of \(4 \cdot n\), a novel quantum subtraction circuit with a T-count of \(4 \cdot n - 4\) and a quantum multiplication circuit with a T-count of \(8 \cdot n^2 - 4 \cdot n\).

VI. CONCLUSION

In this work, we presented T-count efficient quantum circuits for bilinear interpolation. Proposed quantum circuits for the scale up operation and scale down operation are illustrated. The building blocks used in our proposed quantum bilinear interpolation circuits (quantum adder, proposed quantum subtractor and quantum multiplication circuit) are also shown. The proposed quantum bilinear interpolation circuits are compared and achieve significant T-count savings compared to the existing work. They are also shown to require fewer quantum arithmetic circuits compared to the existing work. We conclude that the proposed quantum bilinear interpolation circuits can be integrated in a larger quantum image processing circuit for NEQR encoded images where T-count is of primary concern.

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| T-count            | % impr. w.r.t. 1 |
|--------------------|------------------|
| 1 \(\approx 856 \cdot n^2 + 196 \cdot n - 98 + 8 \cdot \sum_{i=1}^{\log_2(n)} \frac{14 \cdot (n + i - 2^{-i-1}) - 14}{n^2} - 2^i \) | \(\approx 92.52\%\) |
| Proposed           | \(64 \cdot n^2 - 12 \cdot n - 8\) |