Conductance Degradation in HTS Coated Conductor Solder Joints

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Abstract. Solder joints between YBCO coated conductors and normal metal traces have been analysed as part of an effort to develop a robust HTS lead assembly for a spaceflight mission. Measurements included critical current and current transfer profiles. X-ray micrographs were used to verify proper solder flow and to determine the extent of voiding. SEM of cross-sections with EDS analysis was crucial in understanding the diffusion of the protective silver layer over the YBCO into the solder for different solder processes. The assembly must be stored for an extended period of time prior to final cool-down and operation. Measurements of the joint resistance over the course of months show a significant increase with time. Understanding the interface condition suggests an explanation for the change.

1. Introduction

Spaceflight missions place stringent requirements on the resistance of joints to HTS conductors. The Soft X-ray Spectrometer instrument on JAXA’s Astro-H mission will use a micro-calorimeter operating at 50 mK to measure the energy of each incoming x-ray photon with high resolution. The temperature environment of the microcalorimeter is maintained with a cooling chain consisting of two Stirling coolers, a J-T cooler, a superfluid helium tank, and a three-stage Adiabatic Demagnetization Refrigerator (ADR). To reach its 3-year design lifetime, the total design heat load onto the helium tank is 910 µW [1]. Of this, 10 µW is allocated to the superconducting current leads for the ADR solenoids, each of which draw a peak current of 2 Amps. In an off-nominal (failed Stirling cooler) case, the warm end of the superconducting leads must function at temperatures up to 62 K.

To meet these requirements, a set of High Temperature Superconductor (HTS) lead assemblies were designed, built, tested for flight, and delivered to the project [2]. The assemblies used commercial 2G REBCO coated conductor. To minimize thermal conductance, instead of the standard 2–3 µm sputter-deposited silver outer layer, tapes with a silver-gold alloy were used. The tapes were also cut down to 1 mm width. At the cold (warm) end, transition to NbTi/Cu composite (standard copper) wire were made through solder joints to silver-plated, copper traces on a printed circuit board (PCB). After passing electrical, thermal, and vibration tests, the assemblies were put in storage for nearly a year. Just prior to shipment to Japan for integration into the flight dewar, the assemblies were tested again, and it was discovered that the joint conductance had seriously degraded. The leading hypothesis for the failure was corrosion due to insufficient rinsing of solder flux. A large effort was
mounted to build a new set of assemblies. A significant part of this effort was directed toward understanding the factors influencing solder joint conductance and their degradation over time.

2. Sample Preparation

Samples were prepared using either test boards or spare flight boards. Test boards are large (~ 100 x 150 mm) two-layer PCBs, specifically designed for solder joint testing. They accommodate up to eight ~110 mm sections of HTS tape, with up to 16 joints. The traces are of the same ~ 100 µm thick copper, plated with ~ 0.5 µm immersion silver, as are used in the flight boards. The test boards have wide traces for the high current paths and a nearly continuous bottom layer for heat sinking. A pair of voltage tap traces, connected at either end of each solder joint, allowed the voltage across each joint to be measured. The flight PCBs are 3 layer boards with a nearly continuous central layer thermally linked to plated through holes to provide a thermal path for heat generated in the board. As in the test boards, the flight boards have built-in voltage taps on either end of each solder joint.

The HTS material is the same as used in the flight HTS lead assemblies: 2G REBCO tape with a 50 µm thick Hastelloy substrate, sliced down to 1 mm width. In 2G tapes, local spots of low \( J_c \) limit critical current. Slitting the tape exacerbates this problem, so the \( I_c \) of all lengths of tape was measured and only those with \( I_c > 28 \) Amp used.

Two indium-based solders were used: In3%Ag, and In48%Sn. Both are eutectics. The melting point of In3%Ag is 143 C, and that of In48%Sn in 118 C. While copper-plated 2G conductors are typically soldered with eutectic SnPb, early testing in the project indicated that with these unplated tapes, the silver layer completely dissolves into the tin-rich phase, even with relatively brief exposure to the molten solder. The low soldering temperature of the two indium alloys should slow this reaction. While In48%Sn has a very low melting point, which should also limit damage to the YBCO layer, In3%Ag should have lower solubility of silver, particularly if soldering occurs close to the (eutectic) melting point. In all cases, 50 µm thick solder ribbon was used, cut into preforms 0.5 mm wide and the length of the joint, typically 25mm. Kester RF741 RMA flux was used. In all cases, the HTS tape was oriented so that the side with the superconducting layer was in contact with the solder.

Flight circuit boards are typically soldered using a multi-zone oven. This allows tight control of temperature and temperature rates. The inherently three-dimensional shape of the HTS lead assemblies (see reference [2]) precluded the use of a standard oven, but an oven-based process was developed in attempt to maintain strict control over process parameters. For the test boards, foil heaters mounted directly to bottom applied heat. The flight boards, which were too small to accommodate heaters, were mounted on somewhat larger aluminum plates with heaters. The heavy copper leads that carried current into the boards tended to create cool spots, so a copper clamp with foil heaters was mounted directly on the leads also. To minimize radiative and convective losses, the PCBs were enclosed in foil-lined fiberboard “oven”. A constant pressure was applied to the solder joints with tungsten weights. A stack of thin glass slides, separated by narrow strips of Kapton, minimized the effect of tungsten’s heat capacity. The average pressure on the joints ranged from 8 to 15 kPa. Diode thermometers mounted directly on the boards measured temperature, and PID temperature controllers provided power to the heaters. In this way, temperature could be ramped at a fixed rate, or held at a given value, and the temperature could be logged at a rapid cadence. A heating rate of ~ 35 K/min, within the range recommended by the solder manufacturer, was easily achieved. The enclosure was opened as soon as the joint had reached peak temperature, and forced air used to cool the joints, again at a rate (120 K/min) within the range recommended by the manufacturer.

As will be shown below, following this standard process for the use of indium alloy solders resulted in consumption of the silver layer over the REBCO. A series of samples using a hand-soldering process were produced with In3%Ag (m.p. 143 C). For these, boards were preheated to approximately 20 C below the melting point using a hot air soldering station, and the solder was melted using a temperature-controlled soldering iron 20 C above the melting point. Soldering was done in a single swift stroke to minimize the time above the melting point.
3. Measurements

3.1. Joint Resistance

Joint resistances, and the resistance of the HTS tape between joints, were measured in a closed cycled cryostat down to ~4 K, and also in liquid nitrogen (LN$_2$). For tests in LN$_2$, heavy copper leads were used, and current was supplied by a Cryomagnetics CS-4 current source. Voltages between pairs of taps were read out with Keithley 2000 multimeters. Current was limited to 25 Amps to keep the heat flux from the traces on the boards from exceeding the burnout limit for pool boiling liquid nitrogen. The resistance of each region was determined from the slope of the voltage-current curve. The voltage-current curves of most joints remained linear up to the maximum current (25 Amps).

For measurements in vacuum, resistances were measured using a Linear Research LR-700 AC resistance bridge. The source of the bridge was connected in series through all of the circuits on the board, and the sense lines were connected to all sense lines through a multiplexer. Measurements were made during cool down, and thus the resistance as a function of temperature from 290 K down to 4 K was obtained. For a typical test board, the room temperature values of its 8 joints range from 0.176 to 0.216 $\Omega$. These values drop by approximately a factor of two in cooling to the $T_c$ of the tape, ~92 K. At $T_c$, resistance drops roughly 4 orders of magnitude. Figure 1 shows the low temperature region of the resistance – temperature plot for four of the joints. The resistance behaves like a normal metal, dropping linearly with temperature down to ~30 K, and leveling out at low temperature. Two of the joints undergo a second sharp drop in resistance around 5.3 K, significantly below the reported range for the $T_c$ of In$_{48}\%$Sn (7.1 – 7.5 K); two others show no second transition.

3.2. Joint resistance profile

In an attempt to better understand the variation observed in joint resistances, the resistance profile of joints on two of the test boards was measured. For these measurements, the source of an LR-700 resistance bridge was connected across the circuit, and one sense line was connected to the outer voltage tap, the tap at the end of the tape. The other sense line was connected to a sharp probe. The resistance reading was thus zero when the probe was at the end of the tape, and the polarity of the

![Figure 1](image-url)  

**Figure 1.** Typical resistance – temperature plot for In$_{48}\%$Sn solder joints on a test board. Below the $T_c$ of the HTS tape, the solder resistivity behaves like a standard metal, dropping linearly with temperature, then levelling out. Samples 4A and 5A are near the centerline of the board; samples 3A and 6A were closer to the edges.
sense lines was chosen so that resistance increased as the probe moved toward the opposite end of the joint. The board was positioned in a shallow container filled so that the surface of the liquid nitrogen was approximately 1 cm above the surface of the board. Prior to immersing it in LN$_2$, one millimeter scale lines were marked on the board along, and extending somewhat beyond, the solder region. In this way, the position of the probe could be determined to approximately ± 0.25 mm. As mentioned above, the HTS tape is oriented so that the superconducting layer is on the lower side, facing the solder. In these slit tapes, with no silver on the side walls, current flow from the REBCO-coated face to the upper face must pass through the ceramic transition layers between the superconductor and the substrate, which are inherently insulating. For this reason, the probe was only touched to points on the trace of the board next to the solder joint.

The resistance as a function of the position from the end of the HTS tape, $R[x]$, rises rapidly initially, then levels out and asymptotically approaches the full value of the resistance across the joint, $R_{\text{full}}$, which is the value measured across the voltage taps. Equivalently, the difference $R_{\text{full}} - R[x]$ follows an exponential-like drop to zero with increasing $x$. Figure 2a) shows this difference, scaled by $R_{\text{full}}$, plotted on a semi-log graph versus position. The data roughly follow straight lines. Thus,

$$\frac{R_{\text{full}} - R[x]}{R_{\text{full}}} = 1 - \frac{R[x]}{R_{\text{full}}} \approx e^{-x/\lambda},$$

where $\lambda$ is the current transfer length. The solid lines show the least squares best fit to this equation for all 8 joints. Figure 2b) shows the values of $\lambda$ determined in this way as a function of joint resistance, $R_{\text{full}}$. Note that even the largest value of $\lambda$ is only ~20% of the physical length of the joint. Note also that $\lambda$ and $R_{\text{full}}$ are reasonably well correlated; the solid line shows the least-squares best linear fit. The inverse of the slope gives $dR_{\text{full}}/dx = 6.8 \mu\Omega/mm$. This is of the same order as the trace resistance per length, $dR_{\text{trace}}/dx \sim 8 \mu\Omega/mm$, as determined by probe measurements along the trace outside the joint region.

### 3.3. X-ray imaging

X-ray imaging of solder joints was carried out on most test boards and simulators, as well as all flight solder joints. The flat solder bonds between the trace and the HTS tape are particularly amenable to x-ray imaging. X-ray images reveal variation in solder thickness, areas where it did not flow, and voids.

**Figure 2.** a) Resistance profiles of 8 nominally identical 20 mm joint samples. $R[x]$ is the resistance at position $x$; $R_{\text{full}}$ is the resistance across the entire length of the joint. For each sample, the straight line is the least squares best fit to the function $e^{-x/\lambda}$, where $\lambda$ is the current transfer length. b) Current transfer length as a function of $R_{\text{full}}$ for the various joints. Larger joint resistances are correlated with longer transfer lengths. Note that the transfer lengths are a small fraction of the physical length of the joints.
Figure 3 shows typical images for both oven-soldered and hand soldered joints. The level and type of porosity varied significantly from trace to trace, even on traces soldered simultaneously in the oven, and that thus experienced nearly identical temperature excursions. In general however, traces soldered with an iron had smaller voids, and the voids were often more finely dispersed. We believe this difference arises from higher local pressure when soldering by iron, and from the fact that the application point of this pressure moves down the joint, tending to squeeze out gas formed by the interaction of the flux with the oxides on the surface.

3.4. Imaging and elemental analysis of cross-sections

While x-ray imaging is excellent in revealing voids, it is insensitive to cracks parallel to the surface of the interface. For this reason, cross sections were imaged using an optical microscope and a Scanning Electron Microscope (SEM). Cross-sections were cut from the boards with a diamond saw, mounted in epoxy, and polished. Great care must be used to avoid damaging the sample during polishing.

The SEM included the capability for Energy-Dispersive x-ray Spectroscopy (EDS), which analyzes the spectrum of the x-ray emission stimulated by the electron beam as it scans across the sample. EDS thus produces an image that contains the elemental analysis at every pixel. Figure 4 shows SEM/EDS micrographs for two solder joint cross-sections, one produced by oven soldering, the other by hand soldering. The right-hand images in each row are the electron micrographs. The center and left images show the concentration maps of silver and indium, respectively. The indium and silver images have the same scale, so it is possible to identify areas where the silver layers on both the copper trace and the REBCO have dissolved into the solder and formed an indium-silver intermetallic. In both samples, the indium extends all the way to the copper layer, indicating that the thin, ~0.5 µm, immersion silver layer has been completely consumed, as has the thicker, 2–3 µm silver (actually Ag5%Au) layer on the HTS tape in the oven-soldered sample. This is corroborated by the electron micrographs: areas of indium without high silver concentration are very soft, and trap the grinding media, which show up as dark particles in the image; areas of overlap between indium and silver are hard intermetallics, which do not trap the grit and appear bright. In the hand-soldered sample, the indium does not extend all the way to the superconductor surface, indicating the presence of a thin (0.5–1.0 µm) layer of unreacted silver. That most of the silver layer on the HTS is consumed indicates that the indium-silver reaction proceeds very quickly when the solder is molten. As discussed above, in the hand-solder process the board is preheated to about 20 C below the melting point, so the solder melts quickly as the iron passes over it. Swiping the 2–3 mm wide tip across the 20 mm long joint region requires about 6 seconds, so any point is molten for only approximately a

![Figure 3. X-ray images of In3%Ag solder joints between copper traces (gray region) and 1 mm wide HTS tape (dark region). In general, oven soldered joints showed higher porosity than hand soldered joints.](image-url)

a) Oven soldered sample  

b) Hand soldered sample
second. By contrast, the board remains above the melting point for about a minute in the oven process.

The fact that the silver layer is almost completely consumed in such a rapid soldering process indicates that avoiding complete consumption is difficult. Figure 5 shows a cross section of the final solder test sample. Even though this was done using nominally the same process as the hand-soldered sample shown in figure 4, in this case the indium has diffused to the upper interface, indicating complete reaction. Figure 5 also shows a region with a small (~146 µm long) crack. The separation occurs primarily between the indium-silver intermetallic and the REBCO layer, although in one ~30 µm region, the REBCO has detached from the Hastelloy substrate.

The upper and lower (Hastelloy and copper) interfaces are parallel, indicating the sample has not been distorted in the polishing process. Furthermore, other cross sections from the same sample show a

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**Figure 4.** SEM/EDS analysis of In3%Ag solder joint cross sections. Indium and silver maps are scaled the same. Regions bright in both indium and silver are indium silver intermetallic. Note that indium extends all the way to the lower interface (copper) in both samples, indicating the immersion silver layer is completely consumed. In the hand soldered sample, the indium does not extend all the way to the upper (REBCO) interface, showing that some of the silver layer remains intact.

**Figure 5.** SEM/EDS analysis of the final In3%Ag solder joint test sample, showing a region around a crack. Note that the indium has diffused to the top boundary, indicating complete conversion of the silver layer to In-Ag intermetallic. Note also that the separation occurs primarily between the REBCO and In-Ag layers, although in one region REBCO has detached from the Hastelloy substrate.
region where the solder has flown into a gap. Such cracks were observed in earlier (hand-soldered) samples, and are likely due to the low peel strength between layers in 2G coated superconductors [3].

3.5. Resistance degradation over time
During the first attempt to fabricate the new flight HTS assemblies, inadequate fixturing prevented sufficient pressure from being applied to the cold end board on one of the assemblies during soldering. X-ray images showed uneven solder flow in some joints. Although the assembly met all requirements in cryogenic testing, the unit was rejected and became available for life testing. It was tested five additional times. In each test, the unit was held in vacuum in the “worst case” temperature configuration, with the warm end board controlled at 62 K, and the cold end at 5.7 K. Current was ramped to 5 Amps, and voltage across every joint, and across the HTS tape was recorded. The V-I curves were all linear, and no voltage appeared across the HTS tape outside the joint, within the error of the measurement. The slope of the V-I curves determines the resistance. As in section 3.1, a multiplexed ac resistance bridge also monitored the resistances on cool-down. The resistances determined by the two techniques agreed. Between the first two measurements, the unit was kept in a nitrogen purge box. In subsequent intervals, the unit was stored in vacuum, except between tests 3 and 4, as discussed below.

Figure 6 show the resistance as a function of time above 273 K since fabrication. For all but one of the joints, the resistance increases with a log-time dependence. This suggests a presumably temperature-dependent chemical reaction at the superconductor-solder interface. Storing the unit in a sealed, nitrogen-filled bag in a freezer at -20 C for a month tested this hypothesis. The small interval between points 3 and 4 is the time required to warm up from 273 K, remove the unit from the cryostat, purge and seal it, and transport it to the freezer after test 3, and to reverse the process before test 4. The resistance change between these two tests is zero within the error of the measurement in some cases, and, where it is not, is accounted for by the small interval above 273 K. The resistance of one of the joints in the cold end board did not follow the log time behavior, but instead followed a linear increase with time quite precisely for the first five measurements, as figure 6c shows. In the most recent measurement, the resistance fell below this linear trend.

4. Conclusions
Although we have used the term “joint resistance” throughout this paper, it must be kept in mind that this is a practical term for the total resistance across a lap joint that has a normal conductor on one side. A pointed out in section 3.2, $\frac{dR_{\text{full}}}{d\lambda} \approx \frac{dR_{\text{trace}}}{dx}$, so the joint resistance is primarily the voltage

![Figure 6](image)

Figure 6. Resistances of the different solder joints on an HTS assembly as a function of time stored above 273 K. a) Resistances on the warm end board, measured at 62 K. b) Resistances on the cold end board, measured at 5.7 K. Note that all joints follow a log-time behaviour except one of the cold end joints. c) This joint followed a linear time behaviour for the first ~80 days.
drop in the copper trace, and is controlled by current transfer length, $\lambda$. This length, in turn must be largely controlled by the interface resistance. The interface resistance is determined geometric factors, such as porosity and cracking, and by the intrinsic interface resistivity. We suspect geometric factors, particularly porosity, explain the variance in the data from the simple exponential fit seen in the current transfer plot, figure 2a).

The conductance degradation with time discussed in section 3.5 must almost certainly be due to a slow change in the interface resistivity; it is unlikely a geometric factor, crack growth for instance, would be arrested by storage at -20 C. Ekin, et al. hypothesized [4] and showed [5] that the high oxygen affinity of indium caused the development of an indium oxide layer at the interface of In2%Ag solder applied directly to samples of bulk YBCO. They showed that silver interfaces do not develop oxide layers, and suggested that it be deposited directly on the YBCO, a practice that has become standard. Unfortunately, as shown in section 3.4, indium solder reacts rapidly with the 2–3 µm layer of silver on standard coated 2G superconductors, and can fully consume the silver layer, even if an intentionally rapid solder process is used, leaving a layer of indium-silver intermetallic in contact with the superconductor. For the low soldering temperature used, the intermetallic regions most likely contain both AgIn$_2$ and Ag$_3$In. For In2%Ag soldered directly to bulk YBCO, Ekin measured interface resistivities of up to 5.5 $\Omega$·mm$^2$ at 77 K. For the 20 mm$^2$ joints used in this study, such resistivities would lead to much higher joint resistances than observed. Thus, one might surmise that the tendency to form an oxide layer at the interface with the REBCO is reduced in the intermetallic. However, the low temperature resistance of the oven soldered samples are approximately equal to those of the hand soldered samples. While in the hand soldered cross-sections, some of the silver barrier layer remains intact (figures 4e) and f)), or there is a continuous layer of intermetallic in contact with the superconductor (figures 5b and c)), in the oven-soldered cross-section, the silver-indium reaction not only goes to completion, but the intermetallic lumps migrate to the middle of the joint, leaving indium solder directly in contact with the superconductor (figures 4b and c)). This is ostensibly the same configuration as Ekin’s In2%Ag/YBCO samples, although in his bulk YBCO samples the grains at the interface are randomly aligned, whereas in the coated superconductor the interface is presumably with a-b planes.

Given the complexities in the use of solder, and the possibilities of continuing chemical reactions, when the use of non-copper clad 2G tape is required, a prudent path may be to develop mechanical joints. Ito and Hashizume [6] have demonstrated mechanical lap joints with resistances comparable to those of soldered lap joints.

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