Ramp generator circuit for probe diagnostics using microcontroller for LHCD system

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Abstract. It is well known that in LHCD system, the rf power coupling between antenna and plasma strongly depends on the edge plasma parameter. Thus it is mandatory to monitor edge plasma parameter to establish proper impedance matching condition when LHCD power is launched into the plasma. For SST1 LHCD system, we intend to monitor the edge plasma parameter employing electric probes, connected to the grill antenna sides for the said purpose. In SST1, initially LHCD system would couple rf power to plasmas lasting for small durations. Gradually the power and pulse length would be increased to eventually get 1000 seconds plasma. To monitor the edge plasma parameter, over such a wide spectrum (say few millisecond to seconds) during the above campaign, a flexible measurement scheme is desired which would cater to entire spectrum of operation.

Normally a ramp is utilized to bias the electric probe, which yields various plasma parameters. To cater our requirement, the ramp generator must have facility to change ramp-up rate to meet our pulse length requirement. Further during SST operation, the human access near the machine would not be permitted and ramp circuit might not be accessible for manual settings. Thus remote setting facility to change ramp-up rate is also desired. Keeping these constraints in mind, a ramp circuit has been designed using Analog Device micro-controller ADuC842. The circuit has both manual and remote setting facility. Ramp generator parameters like Ramp-up rate, Trigger mode, number of cycles, etc. can be set from PC through RS-485 serial link. Initially low voltage (0-5V) ramp signal is generated using micro-controller and in-built DAC. This low voltage ramp is then amplified with PA-85 op-amp to get desired probe biasing voltage (-110V to +110V). The ramp period can be change form (1ms to 1000 ms) to cater to different plasma pulse length. Programming for micro-controller is done in structured language-C with the help of “Keil” IDE.

In this paper, a detailed design and results obtained from the above ramp circuit under different settings would be reported and discussed.

1. Introduction
The LHCD system [1] on SST1 tokamak [2] is used mainly for driving and sustaining plasma current non-inductively for steadystate operation. The aim is to launch and couple 1MW of rf power at 3.7GHz to shaped plasma for CW (1000 seconds) operation. The coupling of rf power would be established in a phased manner and power level along with pulse length will be gradually increased with our learning experience. It is well known that optimum edge plasma density is needed for efficient rf power to the plasma. Thus it is mandatory to monitor edge plasma density to establish proper impedance matching condition when LHCD power is launched into the plasma. For SST1 LHCD system, we intend to monitor the edge plasma parameter employing electric probes, connected...
to the sides of the grill antenna. To monitor the edge plasma parameter, over such a wide pulse length (say few millisecond to seconds) during the learning phase, a flexible measurement scheme is desired which would cater to entire pulse durations of operation.

Normally a ramp is used to bias the electric probe for the measurement of various plasma parameters. It is desired to operate the ramp locally as well as remotely since no human access is allowed near the machine when SST1 machine is in operation. Thus the ramp-circuit should have remote access to set different ramp-up rate for different pulse length requirements, trigger mode, number of cycles, etc. To operate the circuit remotely a micro-controller based (Analog Device micro-controller ADuC842) system has been developed. This system is connected to PC using the RS485 configuration. Programming for micro-controller is done in structured language-C with the help of “Keil” IDE. In this paper the detailed design of ramp circuit is presented in section 2. Section 3 presents the results and discussion obtained from the prototype design of the ramp circuit, under different parameter settings followed by conclusions in the last section.

2. Design criteria

The basic idea behind the design of micro-controller based ramp generator is to facilitate the user-friendly measurement of plasma density through remote access and to provide parameter setting facility remotely. The heart of the circuit is Analog Device make ADuC842 micro-controller and is chosen because it has in-circuit re-programmability and has on-chip ADCs and DACs for ease of analog signal handling. A low voltage ramp is thus generated using micro-controller and then amplified with the help of PA-85 op-amp.

![Functional Block diagram of ramp generator](image)

**Figure 1.** Functional Block diagram of ramp generator

The block diagram of the basic circuit operation is shown in figure 1. The user can enter ramp parameters like period of ramp, set trigger mode (i.e. continuous/ External trigger), number of cycles (for external trigger mode), start and end point voltage of ramp (i.e. Vpos & Vneg). These parameters either can be entered by keys or through serial interface. ADuC842 has two on chip DACs. DACs can be configured either employing 8 bit or 12 bit. Here DACs are used in 8 bit configuration for easy and simple operation. The number of counts for DAC0 can be calculated depending upon the inputs Vpos and Vneg. The micro-controller unit calculates number of counts to be varied (DAC0L min) as shown in equation-1.

\[
DAC \ 0L \ min = 256 - \frac{|Vpos| + |Vneg|}{Gain} \times \frac{2^8}{Vref} \tag{1}
\]
Here, DAC0L is low byte of DAC data register, Vpos is maximum voltage of ramp after amplification, Vneg is minimum voltage of ramp after amplification, Gain is PA85 amplifier gain and Vref is reference voltage of DAC. Based on this calculation, DAC0L is ramped down from 0xff to the DAC0Lmin at regular intervals. From the ‘period’ entered by user and number of counts to be varied in DAC, the time interval between the count increments i.e. time/count is calculated. Based on this and the clock frequency of the timer, the delay count to be loaded in timer is calculated using equation-2.

$$\text{Timercount} = 65536 - \frac{\text{Osc. freq} \times \text{Period}}{(256 - \text{DAC0L min}) \times 1000}$$  \hspace{1cm} (2)

Here, Timercount is count to be loaded in timer to generate an interval after which DAC has to be incremented. Osc. Freq is ADuC842 core clock frequency (Hz) and Period is ramp time period entered by user (in ms). This count is reloaded every time the timer overflows. Simultaneously, at each timer-overflow, DAC0L data register is decremented by one. This generates the ramp of desired time period. A new timer delay count is calculated each time the user modifies the ‘period’. This generates ramp of desired peak-to-peak amplitude and period.

An offset voltage is given to the Op-Amp to get desired ramp start and stop voltage. This offset voltage shifts the fixed ramp to the desired ramp voltage values. The offset voltage is generated by another on-chip DAC. Data to be loaded in DAC1 is calculated using equation-3.

$$\text{OffsetCount} = \text{DAC1L} = \frac{\left| \frac{V_{\text{max}}}{\text{Gain}} - \left| \frac{V_{\text{neg}}}{\text{Vref}} \right| \right|_2 \times 2^8}{\text{Vref}}$$  \hspace{1cm} (3)

Here, Vmax is maximum ramp output voltage when DAC0L is 0xff after amplification, Vneg is minimum voltage of ramp after amplification, Gain is PA85 amplifier gain and Vref is reference voltage of DAC. DAC1L generates the desired offset voltage. This voltage is fed to +ve input of op-amp. The –ve input is given by DAC0 which is a ramp voltage in the range between 0-5V. The output of the op-amp is a negative going ramp, starting with the Vneg voltage value, ramping up till Vpos voltage value. If the trigger mode set is continuous, it continuously generates the ramp voltage with the specified time period. In case of external trigger, it generates the ramp voltage for specified number of cycles.

Figure 2. Prototype of ADuC842 board

Figure 3. Prototype of PA85 Amplifier
3. Results and discussions
The prototype of ADuC842 board and the prototype of PA85 Amplifier are shown in figure 2 and figure 3 respectively. Different configuration settings are performed using the prototype ramp circuit. The result obtained from a typical setting is shown in figure 4. The ramp period is set to 11ms, representing the shortest pulse for the measurements. The x-axis scale is 2.5 ms/div and y-axis scale is 50V/div. Figure 5 shows the ramp period set to 1000 ms, representing the longest pulse for measurements. The x-axis scale is 250 ms/div and y-axis scale is 50V/div. The obtained results are in agreement with the set parameters and the prototype conforms to our specifications, which are shown in table 1. All the input parameters are varied and set remotely fulfilling our design criteria.

![](image1)

**Figure 4.** Ramp o/p for period of 11ms

![](image2)

**Figure 5.** Ramp o/p for period of 1000ms

| Parameter                      | Value     |
|--------------------------------|-----------|
| Max Positive Amp, Vpos\(_{\text{max}}\) | +115V     |
| Min Positive Amp, Vpos\(_{\text{min}}\) | +10V      |
| Max Negative Amp, Vneg\(_{\text{max}}\) | -115V     |
| Max Negative Amp, Vneg\(_{\text{min}}\) | -10V      |
| Minimum voltage increment      | 1V        |
| Max ramp period                | 1000ms    |
| Min ramp period                | 11ms      |

4. Conclusions
A prototype ramp generator circuit is developed employing ADuC842 micro-controller and amplifier PA-85 op-amp. The design offer remote operation of the ramp circuit and provides flexible ramp voltage with user defined parameters like pulse length and frequency. The developed system would be used for the measurement of edge plasma parameter for LHCD system on SST1 machine for efficient coupling of rf power to the plasma.

References
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[2] Saxena Y C and SST-1 Team 2000 *Nucl. Fus.* 40 No. 6 1069