Ultra-wideband low noise amplifier employing noise cancelling and simultaneous input and noise matching technique

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Abstract An ultra-wideband (UWB) low-noise amplifier (LNA) exploiting noise cancelling and simultaneous input and noise matching (SINM) technique is presented. The common-gate (CG) input stage with noise cancellation topology is utilized for low-noise figure and wideband input matching. To overcome the noise deterioration induced by the noise-cancelling stages and broaden the input-matching bandwidth, simultaneous input and noise matching technique is employed. The circuit is fabricated in 180-nm CMOS technology. The measurement results show that within 3.1–10.6 GHz UWB applications, S11 is lower than −10 dB, the gain (S21) is 12.4–13.6 dB and the noise figure (NF) is 3.3–4.5 dB. It consumes 12 mA under a 1.8 V supply and occupies an area of 0.56 mm².

Keywords: LNA, CMOS, ultra-wideband

1. Introduction

Recently, ultra-wideband (UWB) technology has become more and more popular because it has the advantages of low power, low cost, fading robustness and flexibility [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12]. Ultra-wideband low-noise amplifiers (LNAs) are crucial components in RF front-ends. The LNA should meet some stringent requirements such as wideband input matching to a 50 Ω antenna, low noise figure, flat gain and good linearity within the wideband range. In recent years, several elegant architectures have been studied to improve the performance of the LNA. The distributed amplifier (DA) is one of the most popular structures for providing flat gain, good impedance matching over a wide range of frequencies [5, 6, 7, 8, 9, 10, 11, 12]. However, the DA demands high-quality transmission lines and consumes a great deal of power. The resistive shunt feedback amplifier can provide wideband input matching [13, 14, 15]. However, in order to obtain low NF, the LNA requires large power. The LNA using noise cancelling technique has been widely used in order to release the trade-off between low NF and wideband input matching [16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27]. However, the traditional noise-cancelling technique is hard to eliminate the noises generated by noise-cancelling stages.

In this paper, an UWB LNA exploiting noise cancelling and simultaneous input and noise matching (SINM) technique is proposed, which can effectively restrain noises of the main transistor and noise cancelling stages and can broaden the input-matching bandwidth.

2. Circuit designs

The noise cancellation technique has been widely used to decouple the input-matching and noise figure. The structure is shown in Fig. 1, the channel thermal noise of M1 flowing through RD1 and RS which is modeled by the current source In,M1, produces two anti-phase noise voltages at nodes X and Y. These two voltages are converted to currents by M2 and M3, respectively [17].

![Fig. 1. Principle of the noise-cancelling technique.](image)

At low frequencies, the noise generated by M1 can be cancelled at the output if \( R_{D1}g_{m2} = R_Sg_{m3} \). Wideband input-matching can be obtained by setting \( 1/g_{m1} \) to 50 Ω. Assuming that the condition for complete noise cancellation and input-matching are satisfied, the noise factor can be derived by considering the noise contribution from two CS-transistors and load resistor as:

\[
F = 1 + \frac{F_{RD} + F_{R} + F_{M}}{R_{D1} + \frac{g_{m2}R_{D1}}{\alpha} + \frac{g_{m3}R_{S}}{\alpha}}
\]

In the case of the noise cancellation amplifier, its input impedance is

\[
R_{in} = R_{D1} + \frac{g_{m2}R_{D1}}{\alpha} + \frac{g_{m3}R_{S}}{\alpha}
\]
The S11 of the amplifier can be derived from Eq. (2):

$$|S_{11}| = \left| \frac{Z_{in} - Z_s}{Z_{in} + Z_s} \right| = \frac{1 - gmR_s - j\omega(C_{gr1} + C_{gr3})R_s}{1 + gmR_s + j\omega(C_{gr1} + C_{gr3})R_s}$$

Since S11 should be less than −10 dB over the band of interest, i.e.,

$$20\log{|S_{11}|} = 20\log{\left| \frac{1 - gmR_s - j\omega(C_{gr1} + C_{gr3})R_s}{1 + gmR_s + j\omega(C_{gr1} + C_{gr3})R_s} \right|} \leq -10\, \text{dB}$$

From Eq. (4), the corresponding input-matching bandwidth $f_{10\,\text{dB}}$ can be derived as

$$f_{10\,\text{dB}} = \frac{gm}{3\pi(C_{gr1} + C_{gr3})}$$

From Eq. (1), we can observe that the increase of $gm_3$ can lower the NF. A large $gm_3$ can be achieved by either increasing the drain current or increasing the ratio of width and length of the transistor. However, large current means more power consumption while a high ratio of width and length introduces larger parasitic capacitance. In addition, since the ratio of $F_{M3}$ to $F_{M5}$ is $F_{M3}/F_{M5} = R_{D3}/R_s > 1$, which indicates that the noise contribution of $M_3$ is larger than $M_5$. In this paper, to reduce the noise contribution of the $M_3$ and broaden the bandwidth, the noise cancelling stage (M3) adopts simultaneous input and noise matching. The proposed LNA is shown in Fig. 2.

![Fig. 2. Complete circuit schematic of the proposed LNA.](image)

The input impedance $Z_{in}$ can be represented as follows:

$$Z_{in} = Z_{in1} \parallel Z_{in2}$$

In which

$$Z_{in1} = \frac{1}{gm_1 + sC_{gr1}}$$

$$Z_{in2} = \frac{1}{gm_2 + sC_{gr2}} + \frac{s}{C_{gr3}} + \omega_T L_4$$

From Eq. (7) and Eq. (8), we can define

$$\omega_0_1 = 0, \quad \omega_0_2 = \frac{1}{\sqrt{(L_3 + L_4)C_{gr3}}}$$

Clearly, if $\omega_0_2$ is not too far away from $\omega_0_1$, then $Z_{in}$ can be expressed as follows at frequency around $\omega_0_1$

$$Z_{in} \approx Z_{in1} = \frac{1}{gm_1 + sC_{gr1}}$$

While at frequency around $\omega_0_2$

$$Z_{in} \approx Z_{in2} = s(L_3 + L_4) + \frac{1}{sC_{gr3}} + \omega_T L_3$$

$S_{11}$ can be expressed as follows at frequency around $\omega_0_1$

$$|S_{11}| = \left| \frac{Z_{in} - Z_s}{Z_{in} + Z_s} \right| = \left| \frac{1 - gm_1R_s - j\omega(C_{gr1} + C_{gr3})R_s}{1 + gm_1R_s + j\omega(C_{gr1} + C_{gr3})R_s} \right|$$

Note that good impedance matching is assumed for simplicity, i.e., $gm_1 \approx 1/R_s$. From Eq. (12), the corresponding lower frequency input-matching bandwidth $f_{10\,\text{dB}-L}$ can be derived as

$$f_{10\,\text{dB}-L} = \frac{gm_1}{3\pi C_{gr1}}$$

At frequency around $\omega_0_2$, $S_{11}$ can be expressed as follows:

$$|S_{11}| = \left| \frac{Z_{in} - Z_s}{Z_{in} + Z_s} \right| = \left| \frac{1 - gm_3R_s - j\omega(C_{gr1} + C_{gr3})R_s}{1 + gm_3R_s + j\omega(C_{gr1} + C_{gr3})R_s} \right|$$

Note that good impedance matching at frequencies around $\omega_0_2$ is also assumed for simplicity, i.e., $\omega_T L_4 \approx R_S$. From Eq. (14), the corresponding upper frequency input-matching bandwidth $f_{10\,\text{dB}-U}$ can be derived as

$$f_{10\,\text{dB}-U} = \frac{R_s}{3\pi(L_3 + L_4)}$$

The overall input-matching bandwidth $f_{10\,\text{dB}}$ of the amplifier can be roughly regarded as the union of $f_{10\,\text{dB}-L}$ and $f_{10\,\text{dB}-U}$ if they overlap.

It is worthy to mention that, different from conventional noise cancellation technology, which presents single notch frequency in the middle band of $S_{11}$ versus frequency characteristics, the proposed LNA can introduce two notch frequencies at the low and high band of $S_{11}$ versus frequency characteristics and achieves wideband input matching.

To evaluate the influence of the SINM topology on input matching, Fig. 3 shows the simulated $S_{11}$ versus frequency characteristics for different values of inductor $L_3 + L_4$. The low frequency ($f_{11low}$) and high frequency ($f_{11high}$) form two notch frequency points of $S_{11}$ response. The impedance matching condition can be extended by these two notch responses. Meanwhile, by modifying the high frequency resonance ($f_{11high}$) bandwidth extension can be further illustrated, as shown in Fig. 3. As can be seen, the higher notch frequency ($f_{11high}$) and $f_{10\,\text{dB}}$ increase with the decrease of $L_3 + L_4$. Meanwhile, the low notch fre-
frequency point \( (f_{\text{f,low}}) \) remains when the inductance of \( L_3 + L_4 \) changes.

3. Experimental results

Based on the proposed circuit topology, the UWB LNA is implemented in a six-metal 0.18-um RF CMOS technology. Fig. 4 shows the die microphotograph. The overall chip area including the RF and DC pads is 0.56 mm\(^2\). The power consumption is 21.6 mW under a 1.8 V supply voltage.

The S-parameters and the noise figure of the LNA are measured with an Agilent E8363B VNA and an Agilent E4440A Spectrum Analyzer, respectively. Fig. 5 shows the measurement results along with the simulation results for the S-parameters versus frequency characteristics of the UWB LNA. As can be seen, flat \( S_{21} \) of 13 ± 0.6 dB was obtained over the 3.1–10.6-GHz band of interest. The LNA achieves \( S_{11} \) smaller than −10 dB and \( S_{22} \) smaller than −15 dB over the 3.1–10.6 GHz band. The NF of the LNA is shown in Fig. 6. The LNA has a minimum NF as 3.3 dB (at 6 GHz) and a maximum NF as 4.5 dB (at 11 GHz), and the average value is 3.9 dB. This optimum selection of the values of \( L_3, L_4 \), the shunt peaking inductor \( L_5 \) and the device size and bias keeps \( S_{21} \) flat while optimizes the NF over the operating bandwidth.

Table I compares the performances of the proposed LNA with the recently reported works. Although the power consumption, noise figure and gain of [8] are approximately equal to this work, in [8] the chip area is 0.88 mm\(^2\) excluding the test pads and a better CMOS technology is used. Compared with all literature lists, the proposed LNA obtains flat and high gain and low noise, and draws 12 mA from a 1.8 V supply voltage. The measurement results of this LNA indicate this topology is suitable for 3.1–10.6 GHz UWB.

|            | [8]     | [28]   | [29]   | [30]   | [30]   | This work |
|------------|---------|--------|--------|--------|--------|-----------|
| Tech CMOS  | 130 nm  | 180 nm | 90 nm  | 180 nm | 180 nm | 180 nm    |
| Freq (GHz) | 3–10    | 3.1–10.6 | 3–10  | 2–12  | 3–12  | 3.1–10.6  |
| \( S_{21} \) (dB) | 14.07 ± 1.69 | 11.25 ± 0.4 | 11.5 ± 1.5 | 10   | 9    | 13 ± 0.6  |
| \( S_{11} \) (dB) | <−10   | <−9.7  | <−9   | <−10  | <−10  | <−10      |
| NF (dB)    | 2.5–3.1 | 4.12–5.16 | 3–7   | 6.2–8 | 5.9–7.4 | 3.3–4.5   |
| Power (mW) | 22     | 22.7   | 7.2   | 380   | 132   | 21.6      |
| Area (mm\(^2\)) | 0.88   | 0.447  | 0.64  | 1.89  | 1.89  | 0.56      |
4. Conclusion

In this brief, an UWB LNA operating in the 3.1–10.6 GHz band has been designed and fabricated using a 0.18-μm CMOS process. In order to improve the noise performance and broaden the input-matching bandwidth of the traditional noise-cancelling configuration, the methodology using simultaneous input and noise matching is adopted. A comparison of measurement results with the recently published UWB LNAs shows that the proposed UWB LNA achieves high and flat $S_21$, wideband input impedance matching and low NF, and is very suitable for UWB system applications.

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