P-type Cu$_2$O Thin Film Transistors for Active Matrix Displays: Physical Modeling and Numerical Simulation

KADIYAM RAJSHEKAR$^1$, AND D KANNADASSAN.$^1$

$^1$School of Electronics Engineering, Vellore Institute of Technology, Vellore 632014, India.

Corresponding author: D Kannadassan (e-mail: dkannadassan@vit.ac.in).

ABSTRACT In this paper, we present the physical modeling and numerical simulations of p-type Cu$_2$O TFT for the design and development of active matrix displays. In Cu$_2$O, the carrier transport is through copper and oxygen vacancies ($V_{Cu}$ and $V_O$) which are prominent defects due to their low formation energies. These defects were modeled with acceptor-like and donor-like Gaussian states. From the simulations, it was observed that the $V_{Cu}$ significantly controls the OFF current and threshold voltage ($V_{th}$), while $V_O$ degrades the ON current. For the analysis of device stability, both positive and negative bias stress (PBS and NBS) on Cu$_2$O TFT was investigated with dielectric/channel interface traps in simulations. Under NBS, a significant negative shift in $V_{th}$ was observed due to hole trapping from channel to dielectrics. On the contrary, during PBS, a small shift in $V_{th}$ was observed with significant degradation in sub-threshold swing (SS) due to the deficiency of free electron and the presence of additional defects generated in Cu$_2$O channel as stress time increase. In addition to this effect of increase in Cu$_2$O channel thickness were studied where a significant amount of shift in $V_{th}$ from -7.1 V to -6.1 V was observed as the thickness increased from 45 nm to 65 nm. Finally, the dynamic performance of Cu$_2$O was evaluated and found to be better for higher channel thickness in terms of holding of the output voltage. From these observations, the p-type Cu$_2$O TFT shall be considered for the stable and efficient pixel circuit of active matrix displays such as AMLCD.

INDEX TERMS Cuprous Oxide (Cu$_2$O), Density of States (DOS), Thin film transistors (TFTs), negative bias stress (NBS), positive bias stress (PBS), and Dynamic response.

I. INTRODUCTION

High resolution flat panel displays such as 8K×4K with high pixel density (7680×4320 pixels) require high refresh rates up to 120 Hz [1]. To achieve this, transient response based thin film transistor (TFT) technology with fast refresh is needed, which can help the pixel capacitor to charge in a short time. There are several reports available on amorphous hydrogenated silicon (a-Si:H) based TFT, where considerable work was done on the transient response. However, they are not efficient at providing high refresh rates due to their low effective-field mobility ($\mu_{FE}$), and high subthreshold swing (SS).

In recent times, oxide semiconductors (OS) have been highly preferred over a-Si:H TFT technology due to their low temperature and good uniformity over large area, which also support flexible displays. Amorphous Indium Gallium Zinc oxide (a-IGZO) TFTs has gained enormous recognition for its high $\mu_{FE}$ (> 10 cm$^2$V$^{-1}$s$^{-1}$), large band gap (~ 3.2 eV), and low SS (~ 0.1 V/dec) [2]. These attractive properties help to reach the required refresh rates for driving high resolution displays. However, it has few limitations, such as high fabrication cost due to the low abundance of indium (~2 ppm by mass of earth’s crust). Also, p-type conduction in a-IGZO is not possible due to its valence band (VB) structure which consists of oxygen 2p orbitals. These orbitals localize the hole carriers, resulting in high effective mass.

Demonstration of complementary metal oxide semiconductor (CMOS) TFTs for large scale displays reported in recent times [3]. Complex pixel circuits can be realized by CMOS-based TFT, which eliminates the need for complex compensation and external driving TFTs [4]. Also, the CMOS-TFT consumes significantly low power for switching between ON and OFF states. As a result, CMOS-TFT produces less heat compared to n-type TFT. In addition to this, it also gives high noise immunity. For successful CMOS-
TFT technology, efficient and fast switching p-type TFTs are required with excellent electrical performance, compatible to n-type TFTs.

Few metal OSs show native p-type characteristics, such as cuprous oxide (Cu$_2$O) and tin monoxide (SnO). Based on the findings by Kawazoe et al., cuprous oxide (Cu$_2$O) was found to be a potential candidate for p-type TFTs [5]. It shows a high Hall mobility of > 100 cm$^2$/V·s [6]. This is due to the hybridization of Cu 3$d$ orbitals and O 2$p$ orbitals, resulting in the dispersion of valence band (VB) states. This weakens the localization of holes, which consequently improves the hole mobility. Since, Cu$_2$O is abundant in nature, its fabrication cost is also low. Several articles were reported on the deposition of Cu$_2$O thin films, which show that it exhibits p-type conduction due to negatively charged Cu vacancies (V$_{Cu}$) and shows a direct band gap of ~ 2 eV [7]. Zou et al., reported the fabrication of Cu$_2$O TFT, where the channel was deposited through pulse laser deposition [9]. It shows a good effective mobility of 2.7 cm$^2$/V·s with high ON/OFF current ratio of 1.5×10$^6$ and low SS of 137 mV/dec. Similarly, Chang et al., achieved a similar TFT performance through defect elimination techniques, such as Sulphur treatment [10]. In view of flexible TFTs, a room temperature (RT) fabrication of Cu$_2$O TFT was demonstrated by Yao et al., where a polyethylene terephthalate (PET) substrate was used [11].

Though, many articles reported the fabrication and characterization of Cu$_2$O TFTs [12], [13], carrier transport through various defects of copper-oxide systems is rarely reported. Jeong et al., studied the carrier transport mechanism of Cu$_2$O through the calculation of the density of VB tail states via bias and temperature dependent drain currents [14]. However, they have not explained the effects of Cu-vacancies ($V_{Cu}$) and O-vacancies ($V_O$) on the performance of TFTs and circuits. Early reports on modeling the carrier transport of amorphous semiconductors account only tail states [15]. Later, Davis et al., added donor/acceptor sub-gap states in the model [16]. The model further expanded to include both donor and acceptor sub-gap and tail states and demonstrated in numerical simulation of TFTs [2], [17]. The modern density of states (DOS) model has flexibility to define the electronic states of defects with respect to valence band maximum (VBM) or conduction band minimum (CBM). Also, the tail and sub-gap states can be described with realistic exponential and Gaussian distributions for accurate simulations.

In this paper, we present the numerical simulation of Cu$_2$O TFTs using density-of states (DOS) model. First, the defects and disorders of the Cu-oxide system are reviewed and DOS model of Cu$_2$O is presented in section II. Numerical simulation of Cu$_2$O TFTs for various thickness and fitting with measured results are presented in section III. Along with DC characteristics, the bias stress test are investigated for various stress times and presented in section III. Finally, in section IV, we have presented the evaluation of the dynamic performance of Cu$_2$O TFT pixel circuit for high resolution displays.

II. DOS MODEL FOR Cu$_2$O

Cu$_2$O has a simple cubic structure with lattice parameter $a$ = 4.2696 Å. Oxygen atoms are organized in a body centered cubic (BCC) sub lattice, where as copper atoms are formed in a face centered cubic (FCC) sub lattice [18] as shown in fig. 1 (a). In general, based on the stoichiometry, copper oxide has two stable phases, i.e. Cu$_2$O and cupric oxides (CuO). Apart from this, it has one more phase called paramelacnite (Cu$_4$O$_3$) which is meta-stable.

Usually, achieving p-type conduction in OS is very difficult due to the localization of the hole carrier by the O 2$p$ orbital. However, in Cu$_2$O, the localization effect is less due to the hybridization between the Cu 3$d$ and O 2$p$ orbitals. Moreover, as shown in fig. 1 (a) defects in Cu$_2$O such as copper vacancies ($V_{Cu}$) generate excess holes, which lead to p-type conduction [19], [20]. It has relatively shallow transition level $e(0/−1)$, positioned just above the VB edge ($E_V + 0.28eV$) [7]. Based on several literature, the concentration of $V_{Cu}$ varies between $10^{16}$-$10^{18}$ cm$^{-3}$ [21], [22].

![Defect Density Profile](image)

**FIGURE 1.** (a) Lattice and defects in Cu$_2$O system (b) Cu and O vacancy defect density profile in Cu$_2$O.
metal vacancies directly affect the density of states of the oxide system, which are mathematically modeled to perform realistic simulations.

The density of states (DOS) model consists of exponentially-decaying band-tail states and deep-gap (Gaussian) states, which are often associated with disorders and defects in oxide semiconductors, respectively. Disorders in OS are related to variation in the bond lengths, bond angles and coordination numbers where as defects are due to cation/anion vacancies or interstitial. These states are of two types i.e., localized acceptor-like and donor-like states. Accordingly, these localized acceptor and donor-like band-tail are present near CB and VB, where as acceptor and donor-like Gaussian states are at lower half and upper half of the forbidden band gap. Now, the total DOS is given by the sum of both exponential decaying band tail states (a donor-like, $G_{TD}(E)$ and acceptor-like, $G_{TA}(E)$) and Gaussian distribution (donor-like, $G_{GD}(E)$ and acceptor-like, $G_{GA}(E)$) of sub-gap states, i.e.

$$G(E) = G_{TA}(E) + G_{TD}(E) + G_{GA}(E) + G_{GD}(E) \quad (1)$$

where

$$G_{TA}(E) = g_{TA}(E) \exp\left(\frac{E - E_G}{E_{TA}}\right)$$

$$G_{TD}(E) = g_{TD}(E) \exp\left(\frac{E - E_V}{E_{TD}}\right)$$

$$G_{GA}(E) = g_{GA}(E) \exp\left[-\frac{(E_G - E)^2}{U_{GA}^2}\right]$$

$$G_{GD}(E) = g_{GD}(E) \exp\left[-\frac{(E - E_{GD})^2}{U_{GD}^2}\right]$$

(2)

Here $E$ is defined as trap energy, $g_{TA}(E)$ (cm$^{-3}$eV$^{-1}$) and $g_{TD}(E)$ (cm$^{-3}$eV$^{-1}$) at $E = E_C$ and $E = E_V$ are band edge densities at CB and VB respectively. There characteristic slopes are given by $U_{TA}$ and $U_{TD}$. Similarly, Gaussian distributions, with peak densities of $g_{GA}(E)$ and $g_{GD}(E)$ for acceptor-like and donor-like traps at trap energies $E = E_G$ and $E = E_{GD}$ respectively. Their slopes are represented by characteristic decay energies $U_{GA}$ and $U_{GD}$.

III. SIMULATION OF P-TYPE Cu$_2$O TFT

A. DC CHARACTERISTICS

The numerical simulation, using TCAD Silvaco [23], was carried out for the staggered bottom gate TFT shown in the Fig. 2 (c) inset. Based on the boundary condition, the simulation tool solves the Poisson, continuity, and charge transport equations which are coupled together. Apart from this, the numerical simulation also considers other models such as Fermi-Dirac model, field-dependent mobility model...

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and defect model etc. These models are applied to the channel layer of the TFT. In addition to this, necessary boundary conditions are also applied to regulate the carrier movement between source and drain contacts along with thermionic and tunneling models.

To validate the physical modeling of Cu$_2$O TFTs, we have considered the experimental work of Nam et al [8]. From the bottom, a p-type (heavily doped) silicon substrate was used as the gate electrode. Thereafter, a 100 nm thick silicon dioxide (SiO$_2$) dielectric was thermally grown on the top of the substrate. Using RF magnetron sputtering, Cu$_2$O thin film of thickness 45 nm was deposited with subsequent annealing for 7 min at 500 °C. For source and drain contacts, nickel (Ni) was deposited using the evaporation method and the latter patterned with a channel length and width of 100 and 1000 μm respectively.

For the simulation and fitting of Cu$_2$O TFT, electronic properties such as hole band mobility ($\mu_p = 47.5$ cm$^2$/V.s) [8], and electron and hole effective mass ($m_C = 0.98m_0$ and $m_V = 0.66m_0$) [24] are considered. Table 1 shows the parameters used for the simulation of Cu$_2$O TFT. Few DOS parameters greatly affect the transfer characteristics of TFTs during simulation, such as $g_{GA}$ and $U_{TD}$. These parameters are taken into account based on the earlier conclusions drawn from our early works [25], [26]. It is believed that cation vacancies with low formation energies are responsible for p-type conduction. This was justified by Raebiger et al., in first principle study of Cu$_2$O. It concludes that p-type conduction originates from copper vacancies ($V_{Cu}$), which are acceptor-like defects and found just above the VBM. Thus, based on the above facts, $V_{Cu}$ was associated to $g_{GA}$.

Fig. 2 (a) illustrates the impact of the change in $g_{GA}$ on the I-V characteristics. There is an increase in the OFF current as $g_{GA}$ increases. This signifies that, more hole carrier transport is taking place between source and drain through the channel which makes the TFT in depletion mode. Apart from the OFF current, $V_{th}$ also shifted towards the positive x-axis. Despite of this, the variation in ON current is minimal. VBM of Cu$_2$O consists of O 2p orbitals. These orbitals are sensitive to direction dependent disorders [27], [28]. Due to this, the characteristic slope of tails state near VB is always larger to direction dependent disorders [27], [28]. Due to this, the variation in ON current is minimal. VBM of Cu$_2$O consists of O 2p orbitals. These orbitals are sensitive to direction dependent disorders [27], [28]. Due to this, the characteristic slope of tails state near VB is always larger than that of CB. To understand this effect we have changed the $U_{TD}$ value as shown in Fig. 2 (b). We can observe that, higher $U_{TD}$ value can degrade the drain current performance. To clarify this anomaly, at the interface (SiO$_2$/Cu$_2$O), band bending due to $U_{TD}$ was examined with the help of a probe. The Fermi energy, $E_F$ relative to the VB edge ($E_F - E_V$) was plotted with respect to $V_{GS}$ for different $U_{TD}$. As shown in Fig. 2 (c), for large values of $U_{TD}$, $E_F$ is moving far away from VBM. This explains the reason for the degradation of drain current. In Cu$_2$O, there are other defects which contribute to the conduction mechanism. These are oxygen vacancies ($V_O$) and copper interstitial (Cu$_i$). However, $V_O$ predominately affects the drain current due to its low formation energy in comparison with Cu$_i$. It is a donor-like defect, since it donates electrons. This is explained by another DOS parameter, $g_{GD}$. Fig. 2 (d) shows that a higher value of $g_{GD}$ can greatly affect the ON current of the TFT. The simulation values used in $g_{GA}$ and $g_{GD}$ are quite comparable with the literature [7]. A detailed overview of Cu$_2$O defects with respect to their formation energy and their associations to DOS parameters, defect density is shown in Fig. 1 (a) and (b) respectively.

The simulation was further applied to Cu$_2$O TFT with a 65 nm channel thickness. Fig. 3 (a) and (b) shows the I-V fitting the measured data [8] and extracted DOS. Lee et al., investigated the a-IGZO TFT for various channel thicknesses such as 30 nm, 50 nm, and 85 nm through DOS [29]. It was observed that, a 30 nm thick channel has less number of carrier concentration as compared to an 85 nm thick channel. This indicates the presence of less number of traps (acceptor-like tail states) in the 85 nm channel than 30 nm thick channel. As a result, there is a decrease in the $V_{th}$ requirement to turn ON the TFT. A similar behavior was observed in Cu$_2$O TFT as the channel thickness increased from 45 nm to 65 nm. As a result, $V_{th}$ has decreased from -7.1 V to -6.1 V. To capture this mechanism, donor-like tail states, $g_{TD}$ were reduced from $1 \times 10^{21}$ to $9 \times 10^{20} \text{cm}^{-3} \text{eV}^{-1}$. Figure 3 (c) shows the overlay of tail states from measured Cu$_2$O TFT (40 nm thick channel) [14] and simulated Cu$_2$O TFT (45 nm and 65 nm thick channel). This significant fit proves that the DOS model for CuZO is realistic and gives physical insight into the defects and disorders present in Cu$_2$O. Key DOS parameters and overall TFT performance are presented in Table 1 and 2 respectively. Recently, few studies on nano crystalline Cu$_2$O show the presence of grain boundary (GB) which largely affect the film resistivity [30]. One shall incorporate the effect of GB in DOS model and field effect mobility model to achieve realistic simulation of TFTs.

### Table 1. Key simulation parameters in DOS model for Cu$_2$O for both 45 nm and 65 nm TFTs.

| Symbols | Units | Cu$_2$O (45 nm) | Cu$_2$O (65 nm) |
|---------|-------|----------------|----------------|
| $N_C$   | cm$^{-3}$ | $2.47 \times 10^{20}$ | $2.47 \times 10^{20}$ |
| $N_V$   | cm$^{-3}$ | $1.11 \times 10^{20}$ | $1.11 \times 10^{20}$ |
| $g_{TA}$ | cm$^{-3}$ eV$^{-1}$ | $2.47 \times 10^{21}$ | $2.47 \times 10^{21}$ |
| $g_{TD}$ | cm$^{-3}$ eV$^{-1}$ | $1 \times 10^{20}$ | $9 \times 10^{20}$ |
| $U_{TA}$ | meV | 30 | 30 |
| $U_{TD}$ | meV | 65 | 70 |
| $E_F$   | eV | 2.7 | 2.75 |
| $\epsilon_F$ | eV | 3 | 2.95 |
| $U_{GA}$ | eV | 0.32 | 0.32 |
| $E_{GD}$ | eV | 1.5 | 1.5 |
| $U_{GD}$ | eV | 2.5 | 2.5 |
| $g_{GD}$ | cm$^{-3}$ eV$^{-1}$ | $4 \times 10^{21}$ | $4 \times 10^{21}$ |
| $g_{GA}$ | cm$^{-3}$ eV$^{-1}$ | $6.3 \times 10^{20}$ | $8 \times 10^{20}$ |
| $\mu_p$ | cm$^2$ V$^{-1}$ s$^{-1}$ | 47.5 | 47.5 |
| $\epsilon$ | cm$^2$ V$^{-1}$ s$^{-1}$ | 4.0 | 4.0 |

### B. Bias-stress-induced Instabilities

Biasing of the gate terminal over a prolonged time period will result change in the electrical performance of TFTs, which
is often referred to bias stress instabilities. Most significantly, the variations in threshold voltage ($V_{th}$) and sub-threshold swing (SS) of transfer characteristics are the common effects. Based on the survey from several literature, it was found that the variation in electrical characteristics of TFTs in the back-panel due to bias stress leads to nonuniform pixel brightness in display technologies, such as AMLCDs, and AMOLEDs [31]–[33]. For instance, a shift of 0.1 V in $V_{th}$ of a TFT in the back-panel of AMOLED display shall reduce about 20% brightness [34]. In this regard, few studies on the characterization of positive and negative bias stress (PBS and NBS) instabilities have been reported in recent times on various oxide semiconductors, such as n-type InGaZnO [32], n-type SnO$_2$ [35], p-type SnO [36] and p-type Cu$_2$O [37].

In this section, similar to the simulation of DC characteristics, we have presented the investigation on the origin of bias stress instability in Cu$_2$O TFT. Recently, Park et al. have examined the bias stress instability in Cu$_2$O TFT experimentally [37]. In both negative bias stress and positive bias stress tests, variation in the transfer characteristics was observed. This is due to two major phenomena; (1) The trapping of hole carriers at the channel/dielectric interface [38], [39], (2) The formation of extra defects states in the subgap states at the channel/dielectric interface [38], [39]. In this regard, the interface trap model is used to describe the time domain emission and capture process of electron/hole from an acceptor/donor trap at the insulator/semiconductor interface, independently reported by F. P. Heiman et al [42] and D. Jelmini et al [43]. In this model, the carrier capture rate defines the recombination rate of the transient current continuity equation, with structural relaxation of hole traps in the insulator. To incorporate this model, a uniform distribution of interface charges at a density of $Q_{it}$, about a depth ($d$) in the insulator from the interface is included. The capture rates are computed using carrier cross-sections of carriers for electrons ($\sigma_{n0}$) and holes ($\sigma_{p0}$) with respect to the quasi-Fermi level is defined as:

$$\sigma_n(d) = \sigma_{n0} \times e^{-k_n d}$$

$$\sigma_p(d) = \sigma_{p0} \times e^{-k_h d}$$

where

$$k_e = \sqrt{\frac{2m_e(E_C - E_{iA})}{\hbar^2}}$$

$$k_h = \sqrt{\frac{2m_h(E_{iD} - E_V)}{\hbar^2}}$$

are the evanescent wave-vectors corresponds to electron and holes. The activation energy levels $E_{iA}$ and $E_{iD}$ are for acceptor-like and donor-like trap respectively, these values are presented in Guellen et al., [44]. Here, $\hbar$ is modified Planks constant and $m_e$, $m_h$ are the effective mass of electrons and holes respectively. It is common approach in TCAD simulators to choose the maximum trap depth $d = 5$ nm [23].

### TABLE 2. Overall Performance of Simulated Cu$_2$O (45 nm and 65 nm) TFTs.

| Parameters | Cu$_2$O (45 nm) | Cu$_2$O (65 nm) |
|------------|----------------|-----------------|
| $V_{th}$ (V) | 7.1            | 6.1             |
| SS (mV/dec) | 1725           | 1914            |
| $\mu_{FE}$ (cm$^2$/V·s) | 0.04           | 0.09            |
| ON/OFF ratio | $1.2 \times 10^4$ | $7 \times 10^3$ |

To compare the results of bias stress simulations, measured NBS and PBS transfer characteristics of Park et al., are taken [37]. Numerical transient simulations of NBS and PBS were performed for Cu$_2$O TFTs for various stress times from 0 to $2 \times 10^4$ s, for the sweep of gate voltage from 10 to -30 V at regular intervals, to meet the experimental results. Fig. 4 (a) and (b) show the simulated NBS and PBS transfer characteristics of Cu$_2$O TFT, respectively, for gate bias for the applied stress time of 0 to $2 \times 10^4$ s, along with the measured results [37]. For NBS at $V_{GS-\text{Stress}} = -25$ V, the $Q_{it}$ is increased to fit the measured results for 0 and $2 \times 10^4$ s, corresponding to before and after stress conditions. The DOS parameters of the channel were not changed. Table-3 lists $Q_{it}$.
for the best fit for both before and after stress conditions. From Fig. 4 (a), it was observed that, as the duration of stress time increases, the transfer characteristics of TFT shift to the negative $V_{GS}$. This shift is computed by change in magnitude of threshold voltage ($|\Delta V_{th}|$), presented in Fig. 4 (c). A close fit was observed between measured and simulated data. The negative $V_{th}$ increases with increasing $Q_{st}$, which explains the transfer of holes from the Cu$_2$O channel to the interface. On the other hand, there is no significant change in SS, which shows that the channel is less influenced by NBS. Similar observations were reported for a-IGZO TFTs [45].

Fig. 4 (b) shows the compatibility of simulated and measured PBS results for $V_{GS-Stress}=25$ V. It was observed that, as the stress time increases, a notable increase in the SS was observed while the maximum shift in $V_{th}$ is less than 3 V. Based on the observation from Park et al., [37], there could be a shortage of free electrons in the Cu$_2$O channel due to PBS. This shows that the DOS of the channel, near the channel/dielectric interface, is disturbed due to electrical stress. In order to model this phenomenon, few DOS parameters need to be tweaked to fit the experimental results. For the shortage of free electrons in channel, that is oxygen vacancies ($V_O$), $g_{GD}$ was parametrically reduced to have a best fit. It was found that a reduction of two orders in $g_{GD}$ results a significant fit. Also, to introduce hole traps near the channel/dielectric interface, acceptor-like Gaussian states ($g_{GA}$) were increased from $6.5 \times 10^{20}$ to $9 \times 10^{20}$ /cm$^3$ eV. These changes in DOS resulted in a good fit between simulated and measured Cu$_2$O TFTs for both with stress (time = 20000 s) and without stress, refer Fig. 4 (b). For various stress times, the $|\Delta V_{th}|$ was extracted from simulation and measured transfer characteristics of Ref. [37], found an excellent fit. Compare to NBS, the PBS shows a small shift of $V_{th}$. This indicates the back-channel was not strongly depleted due to low absorption of O$_2$ during electrical stress and the low carrier concentration at CB of Cu$_2$O. On the other hand, SnO TFT shows a large shift in $V_{th}$ during electrical stress when the back-channel is exposed to air medium [36]. Therefore, Cu$_2$O TFTs show better stress stability compared to p-type SnO TFTs.

**IV. PERFORMANCE OF PIXEL CIRCUIT WITH P-TYPE CU$_2$O TFT**

Ultra-high definition (UHD) display technologies, with resolutions of 4K and 8K pixel densities, require refresh rates of up to 120 Hz to avoid image flickering. This requires pixels to charge within a recommended charge time margin ($t_{cm}$). These issues are often addressed by transient characterization of TFTs. Based on the article reported by Kaneko et al.,
image flickering results from the variation in the feed through voltage ($\Delta V_p$). This $\Delta V_p$ is due to the overlapping of gate-source capacitance ($C_{GS}$) [46]. Lee et al., have studied the details of $\Delta V_p$ and $t_{cm}$ in dynamic response of a-Si:H TFTs [47]. In recent times, Yu et al., reported dynamic studies of IGZO based TFTs for high resolution display requirements [48]. Based on the studies, IGZO TFT was found to be more stable and responsive over a-Si:H TFTs. The reasons for this improvement in IGZO TFT are the high mobility of IGZO ($9.1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) and low SS of $< 130 \text{ mV/dec}$.

Although several reports on dynamic characterization studies are available in $n$-type TFTs, very few reports are available for $p$-type TFTs [26], [49]. Considering the electrical performance and requirements of pixel circuits, in this report, we have presented the characterization of the dynamic response of $p$-type Cu$_2$O TFTs for 45 and 65 nm channel thickness. To study the charging and holding process of the pixel circuit, a mixed-mode simulation of the following pixel circuit was performed. A simple pixel configuration of one Cu$_2$O TFT ($T_1$) and one storage capacitor ($C_{ST}$) is considered for this work, depicted in Fig. 5 (a). Driving control and data signals of pixel circuit is given as follows: In each frame, a fixed DRAIN pulse with a voltage high of $V_{DH}$ is applied at the drain bus to start the charging process. The pulse reaches low DRAIN voltage $V_{DL}$ to reset the frame the pixel. Fig. 5 (b) shows the DRAIN and GATE signals. The charging time margin $t_{cm}$ is calculated by [50],

$$t_{cm} = \frac{1}{FR \times N_{RL}} \quad (7)$$

where the frame rate $FR$ and the number of row-lines $N_{RL}$ are specified by the UHD technology. For full HD and 4K displays, $t_{cm}$ is 16 and 8 $\mu$s respectively [51]. The set/reset period $t_{set}$ is calculated from $t_{cm}$ of the GATE pulse. Often, $t_{set} = 3 \times t_{cm}$ is assumed while the GATE pulse arrives at $1 \times t_{cm}$ just after the rise of the set/reset pulse. Positive and negative edge times ($t_r$ and $t_f$) of GATE pulse shall vary between 1 to 100 ns. The choice of $t_r$ and $t_f$ significantly influences the voltage holding process of storage capacitor. In displays, the delays in GATE and DRAIN lines due to RC parasitic are often affect the requirements of $t_{cm}$ and $t_{set}$. Yet, these effects are not considering to evaluate the performance of Cu$_2$O TFT based pixel circuit.

Simulation of the transient response of a pixel circuit with oxide semiconductor TFTs for various time margins is demonstrated using the mixed-mode platform in the Atlas of TCAD Silvaco. In these simulations, physical models of TFTs such as Fermi-Dirac and defect models, are considered for steady-state analysis, which is initiated with the two-stage Newton method [23]. On the other hand, the positive and negative of GATE and DRAIN pulses ramped on an exponential scale to bypass the convergence issues at the time of numerical simulation. Considering the fact, the $t_r$ and $t_f$ are taken as 10 ns with minimum time-step of 1 ns. In all transient analysis, the GATE pulse amplitude for set and reset is fixed as $V_{GH} = -20 \text{ V}$ and $V_{GL} = 0 \text{ V}$ respectively. During the set and reset of the charging process, the DRAIN pulse is excited with amplitudes of $V_{DH} = -10 \text{ V}$ and $V_{DL} = 0 \text{ V}$. In the pixel circuit, the $C_{ST} = 1 \text{ pF}$ is used to achieve maximum charging delay to evaluate the transient performance of $p$-type Cu$_2$O TFTs.

For the Cu$_2$O TFT, a channel length of 20 $\mu$m, and an S/D overlap length of 5 $\mu$m were chosen. To show the effect of active layer thickness on pixel circuit performance, TFT with 45 nm and 65 nm were simulated, respectively. Dynamic response for full HD displays (10 $\mu$s ) are simulated. Fig. 5 (c) shows the overlayed output voltage at source terminal for 45 and 65 nm TFTs across the storage capacitor. For comparison, W/L ratio, $L_{OVGS}$ was kept the same for both the 45 and 65 nm Cu$_2$O TFT respectively. We can observe that 65 nm TFT overcharged the capacitor voltage as compared with 45 nm. This could be due to more hole carriers present in 65 nm thick channel which is confirmed by increase in the $g_{GA}$. After that, $W$ value of both the TFTs were adjusted to get similar charging and holding performance as shown in fig. 5 (d). From earlier studies [46], the feed through voltage ($\Delta V_p$) is expressed analytically as,

$$\Delta V_p = \frac{C_{GS}}{C_{GS} + C_{ST}} (V_{th} + V_{SH} - V_{GL}) \quad (8)$$

Here, $C_{GS}$ is the overlapping capacitance between gate and source of TFT. From the above equation (6), $\Delta V_p$ is directly and inversely proportional to gate-source overlap length ($L_{OVGS}$) and $C_{ST}$ respectively.

It shows that, $\Delta V_p$ value is high for 45 nm TFT as compared to 65 nm TFT. This is due to the difference in the $V_{th}$ between 45 and 65 nm TFTs. $V_{th}$ for 65 nm TFT was calculated from the simulation and found to be -6.1 V. However, charging capacitor through 45 nm TFT performed marginally quick over 65 nm TFT.

In structural design point of view for TFT, gate to source/drain overlap ($L_{OVGS}$) in an important factor. Figure 6 shows the variation in $L_{OVGS}$ on 65 nm TFT. We can see

| Parameter | NBS | PBS |
|-----------|-----|-----|
| $Q_p$ (cm$^2$) | $1 \times 10^{-14}$ | $6.9 \times 10^{-11}$ |
| $g_{GA}$ (cm$^2$V$^{-1}$) | — | — |
| $g_{GD}$ (cm$^2$V$^{-1}$) | — | — |

TABLE 3. Parameters for NBS and PBS
that as it decreases to 1 \( \mu \text{m} \), \( \Delta V_P \) value got drop since it is proportional to \( L_{OVGS} \). Nevertheless, the TFTs driving capability is reduced, which can be seen in terms of charging. This is due to the fact that, smaller or narrow \( L_{OVGS} \) causes high series resistance at the source/drain contacts due to current crowding effect [52], [53]. Where as larger \( L_{OVGS} \) not good for display operation, since it causes large parasitic capacitance [46]. Finally, an exponential fit of RC time constant (\( \tau \)) for output voltage (\( V_{OUT} \)) within GATE pulse was performed to evaluate the charging characteristics of pixel circuit, expressed as

\[
C_{ST} \frac{dV_{OUT}}{dt} = \frac{\mu_F E C_{ox} W}{L} (V_G - V_{OUT} - V_{th}) (V_D - V_{OUT})
\]

Solving this equation to calculate the required time to charge the \( C_{ST} \) will yield [48],

\[
t_{ch} = \frac{C_{ST} L}{\mu_F E C_{ox} W} \cdot \frac{1}{(V_G - V_{OUT} - V_{th}) (V_D - V_{OUT}) - (V_G - V_{th})(V_D - V_{OUT})} \cdot \frac{1}{V_{G}V_{D}V_{OUT}}
\]

Alternatively, the time constant should be computed by substituting \( V_{OUT} = 0.63V_{DH} \). Similarly, the time constant can also be calculated from transient simulation, by computing the time at 63% of \( V_{DH} \) from \( V_{DL} = 0 \). The theoretical and simulation results are compared in Table 4. It was found that for both the 45 and 65 nm Cu\(_2\)O TFT, the charging time is almost very similar. However, some variation in \( \Delta V_P \) was found. For 65 nm Cu\(_2\)O TFT, \( \Delta V_P \) is low in comparison with 45 nm TFT, which means it will experience less flickering.

V. CONCLUSION

In this article, physical modeling and numerical simulations of the p-type Cu\(_2\)O TFT for the design and development of active matrix displays are presented. To understand the origin of bias stress instabilities, both positive and negative bias stress (PBS and NBS) on Cu\(_2\)O TFT were investigated. From the investigation obtained, the following observations were drawn:

1) Copper and oxygen vacancies (\( V_{Cu} \) and \( V_O \)) are prominent defects due to their low formation energies. They effect the acceptor-like (\( g_{GA} \)) and donor-like (\( g_{GD} \)) of DOS model. While \( V_{Cu} \) significantly affects the OFF current and \( V_{th} \), the \( V_O \) largely degrades the

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**FIGURE 5.** (a) Pixel configuration of one Cu\(_2\)O TFT (\( T_1 \)) and one storage capacitor (\( C_{ST} \)), (b) Input drain and gate pulse Pixel input and output, (c) Output voltage across source terminal for 45 and 65 nm Cu\(_2\)O TFT respectively for same width, \( W = 240 \mu \text{m} \), (d) Output voltage across source terminal for 45 and 65 nm Cu\(_2\)O TFT for \( W = 240 \mu \text{m} \) and 190 \( \mu \text{m} \) respectively.
ON current.

2) Under NBS, the interface charge carrier density, \( Q_{it} \), was responsible for the shift in the \( V_{th} \) since the hole carriers moved from channel to channel/dielectric interface. On the other hand, a small variation in \( V_{th} \) with a significant deterioration in SS was observed under the PBS condition. This is due to the deficiency of free electrons and the presence of additional defects generated in CuO channel as stress time increases.

3) A significant amount of shift in \( V_{th} \) from -7.1 V to 6.1 V was observed as the thickness of CuO channel increased from 45 nm to 65 nm. This is due to the decrease in the donor-like tail states, \( g_{TD} \), since it captures the hole carriers.

4) Dynamic performance of CuO was evaluated and found to be better for higher channel thickness in terms of holding the output voltage. Also, the effect of gate-source overlap length \( L_{OVGS} \) on the output source voltage was studied. It was observed that, smaller or narrower \( L_{OVGS} \) causes high series resistance at the source/drain contacts due to current crowding affect. However, the larger \( L_{OVGS} \) increases the parasitic capacitance, which affects the display performance.

Modeling of TFT through density of states (DOS) is a reliable approach which provides physical insights into the device, such as carrier transport and the behavior of the defects present in the channel. This contributes the necessary recommendations for optimizing the device in terms of its dimensions and channel material, which enhances the overall device efficiency. Finally, from circuit perspective, through DOS, a direct cause-effect relationship between defects and circuit performance can be realized under both DC and transient based electrical characterization. Therefore, it gives the developers a platform to realize complex large scale electronics.

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KADIYAM RAJSHEKAR received M.Tech degree in VLSI Design from Vellore Institute of Technology, Vellore, Tamil Nadu, India in 2011. He is currently pursuing the Ph.D. degree in Electronics Engineering at Vellore Institute of Technology, India. He is also a recipient of Senior Research Fellowship from Council of Scientific and Industrial Research (CSIR), Government of India. His research includes Thin film transistor, semiconductor device modeling.

PROF. DR. D. KANNADASSAN received the Ph.D. degree from School of Electronics Engineering, Vellore Institute of Technology (VIT), Vellore. He is an associate professor with School of Electronics Engineering at VIT. Currently, his research interests are Transparent TFTs and Graphene FETs for future technologies.