Application Ranges of Fault-Tolerant Control for T-Type Three-Level Inverter Under Single/Multi-phase Open-Circuit Faults of Inner Switches

JINPING WANG, (Member, IEEE), WEI ZHANG, WEIDONG JIANG, (Member, IEEE), MINGNA MA, QINGYAN ZHANG, AND XINMEI HUANG
School of Electrical Engineering and Automation, Hefei University of Technology, Hefei 230009, China

Corresponding author: Weidong Jiang (ahjwd@163.com)

This work was supported in part by the Fundamental Research Funds for the Central Universities of China under Grant JZ2019HGTB0074 and Grant PA2019GDPK0080, in part by the Tianchang-Hefei University of Technology (HFUT) Industrial Innovation Lead Key Funds under Grant JZ2019AHDS0002 and Grant JZ2020YDZJ0124, and in part by the 111 Project under Grant BP0719039.

ABSTRACT In recent years, T-type three-level inverter (TLI) has attracted attentions due to its advantages, such as simple structure and higher efficiency. Neutral point voltage (NPV) is very critical for its normal operation, and the necessary conditions of maintaining NPV balance respectively in a switching cycle and in a fundamental cycle are simply reviewed in this paper. With the increment of power switches, the reliability of T-type TLI becomes particularly important. When switch faults occur, fault-tolerant control strategies are usually adopted. However, in existing literatures, it is unknown whether the NPV balance can be still maintained under different fault types. Therefore, the application range of a fault-tolerant control is also unknown. In this paper, based on the necessary conditions of maintaining NPV balance, the application ranges of two representative fault-tolerant control strategies are revealed under different open-circuit (OC) fault types in inner switch. It found that the application ranges are closely related to the modulation index, load power factor (PF) and OC fault type. Finally, the correctness of the theoretical analysis is verified by the experimental results.

INDEX TERMS T-type three-level inverter, neutral-point balance, open-circuit fault, fault-tolerant control.

I. INTRODUCTION
Recently, the rapid development in renewable energy integration requires grid-connected inverters possessing high efficiency, low harmonic as well as small size [1]. And the range of the output ac voltage depends on the requirements of different types of applications. Additionally, the main design targets such as power factor (PF), total harmonic distortion (THD), and efficiency are also determined. Among these targets, efficiency is the most important factor. Three-level inverter (TLI), which exhibits outstanding performances with respect to THD and efficiency, has been used in various wide-power range applications [2]–[6].

Several TLI topologies have been proposed. In the diode neutral-point clamped (NPC) topology, four switches are connected in series. Therefore, the collector-emitter voltage of switches can be reduced by half; however, when the output is connected to the bottom or top of DC-side capacitor, these inner switches must be turned on/off at the same time, which results in large conduction losses [4]. The other is T-type. Compared with the traditional two-level and NPC topology, T-type has the advantages of low switching losses and high cost-efficiency. In addition, in terms of fault-tolerance, T-type has a competitive advantage over other topologies, because the inner switches only affect the switching state [O], and the other two switching states [P and N] are unaffected [1], [7].

For multi-level inverter, the reliability is particularly important because of the increased power switches, which are relatively vulnerable and prone to failure [8, 9]. Switch fault, such as IGBT, can be divided into open-circuit (OC) fault and short-circuit (SC) fault [10]–[13]. Any SC fault is usually catastrophic. It may be caused by high temperature, local...
For OC fault, there are many fault-tolerant control strategies [15]–[20]. However, these strategies proposed for NPC TLI [16] cannot be directly applied to T-type TLI. For T-type TLI, fault-tolerant control strategies were proposed in [17]–[24]. These strategies can be divided into two types. One is realized by adding redundant devices [17]–[19]. However, it is not cost-effective. The other is realized by changing the modulation algorithm [20]–[24], which is highly preferred. The key concern of the latter is to solve the neutral point voltage (NPV) fluctuation, which is critical for three-level operation [22], [23]. At present, the NPV fluctuation of T-type TLI in non-fault condition is mainly focused on, but in fault condition there are few literatures. In [22] and [23], by considering the neutral point (NP) current, proper zero sequence voltage (ZSV) was injected to suppress NPV oscillations for T-type TLI under OC fault. However, the application ranges of the corresponding fault-tolerant control strategies are not fully discussed. Therefore, it is difficult for readers to judge the applicability.

For T-type TLI, while an OC fault occurs in outer switch, fault-tolerant control can be applied to avoid current distortion only under reduced modulation index [23]. Besides, the adjustment of NPV is difficult, since there are no substitute voltage vectors. Therefore, fault-tolerant control based on improving modulation algorithm is very limited to handle OC fault in outer switch. But while OC fault occurs in inner switch, for the worst case, the T-type TLI can be degenerated into two-level inverter. This is the reason why fault-tolerant control is mainly focused on OC fault in inner switch. While OC fault occurs in inner switch, it results in not only output current and voltage distortion, but also NPV unbalance [22], [23].

In [23], two fault-tolerant control strategies were proposed to solve a single-phase inner switch OC fault considering NPV fluctuation. However, the effectiveness under two-phase or three-phase inner switch fault was not discussed. Moreover, in some conditions, it cannot guarantee NPV balance with injectable ZSV, which had been revealed in [25]. For three-phase T-type TLI, there are totally six inner switchers, and many fault types may exist. For a fault-tolerant control strategy, the application ranges should be pointed out under different fault types in which the NPV balance can be well maintained. However, in the existing literatures, it found that there is no report of the relevant studies about that at present.

In this paper, based on the point view of NPV balance, the application ranges of the two representative fault-tolerant control strategies proposed in [23] are revealed under different fault types, which can be used to determine whether the fault-tolerant method is able to deal with the specific fault under certain modulation index and load PF, which is the main contribution of this paper. Then, the applicability can be easily found by readers.

The rest of the paper is organized as follows. Section II reviews T-type TLI, and the necessary conditions of maintaining NPV balance in a switching cycle and in a fundamental cycle are respectively given. In Section III, the two fault-tolerant control strategies are simply reviewed, and a ZSV calculation algorithm is used to minimize NPV fluctuation. In Section IV, the application ranges of the two fault-tolerant control strategies under different fault types are revealed. The corresponding experimental results are given to verify the theoretical analysis in Section V. Finally, Section VI concludes the paper.

II. THE NPV ANALYSIS OF T-TYPE TLI
A. T-TYPE TLI AND ITS NPV CONTROL

The topology of T-type TLI is shown in Fig. 1. Each phase consists of four switches with anti-paralleled diodes, where \( S_{x1} \) and \( S_{x4} \) (\( x = A, B \) or \( C \)) are the outer switches respectively connecting to the positive bus (PB) and the negative bus (NB), and \( S_{x2} \) and \( S_{x3} \) are the inner switches connecting between NP and load. \( C_1 \) and \( C_2 \) are the DC-side capacitors. When the capacitor voltage reaches equilibrium, \( u_{C1} = u_{C2} = u_{dc} \), and the DC-link voltage is \( 2u_{dc} \). Taking NP as the reference point, when \( S_{x1} \) and \( S_{x2} \) are gated on, the output voltage is \( u_{C1} \), remarked as 2 level; when \( S_{x2} \) and \( S_{x3} \) are gated on, the output voltage is 0, remarked as 1 level; when \( S_{x3} \) and \( S_{x4} \) are gated on, the output voltage is \(-u_{C2}\), remarked as 0 level. The phase current flowing from the inverter to the load is defined as the positive direction.

To simplify the analysis, assuming \( u_{C1} = u_{C2} = 1 \), then the three-phase voltages can be expressed as:

\[
\begin{align*}
u_A &= m \sin \omega t \\
u_B &= m \sin(\omega t - 2\pi/3) \\
u_C &= m \sin(\omega t - 4\pi/3)
\end{align*}
\]

where, \( \omega t \in [0, 2\pi] \) is the phase angle of phase A and \( m \in [0, 1.1547] \) is the modulation index. The three-phase
currents can be expressed as:

\[
\begin{align*}
i_A &= I_m \sin(\omega t - \varphi) \\
i_B &= I_m \sin(\omega t - 2\pi/3 - \varphi) \\
i_C &= I_m \sin(\omega t - 4\pi/3 - \varphi)
\end{align*}
\]

(2)

where \(I_m\) is the peak value of the phase current and \(\varphi\) is the load PF angle.

Rearrange three-phase voltages for simplifying analysis:

\[
\begin{align*}
u_{\text{max}} &= \max(u_A, u_B, u_C) \\
u_{\text{min}} &= \min(u_A, u_B, u_C) \\
u_{\text{mid}} &= \text{mid}(u_A, u_B, u_C)
\end{align*}
\]

(3)

And the corresponding phase currents are redefined as \(i_{\text{max}}, i_{\text{min}}, i_{\text{mid}}\).

In order to effectively control NPV or achieve other control objectives, the ZSV \(u_{ZSV}\) is usually injected into modulation voltage. After injecting \(u_{ZSV}\), the modulation voltage \(u'_{x}\) (\(x = \text{max, mid, min}\)) can be expressed as:

\[
u'_{x} = u_{x} + u_{ZSV}
\]

(4)

To avoid over-modulation, the range of \(u_{ZSV}\) is:

\[
u_{ZSV} \in [-1 - u_{\text{min}}, 1 - u_{\text{max}}]
\]

(5)

The notation \(\gamma\) is used to indicate the range of \(u_{ZSV}\). Then, the duty ratio \(d_{x1}\) of 1 level of phase \(x\) can be expressed as:

\[
d_{x1} = 1 - |u'_{x}|
\]

(6)

When 1 level is outputted by one phase, its phase current flows into or out of NP, which causes NPV variation. The NP current \(i_{\text{NPs}}\) introduced by the phase \(x\) in a switching cycle is:

\[
i_{\text{NPs}}(m, I_m, \omega t, \varphi, u_{ZSV}) = i_{x}(1 - |u_{x} + u_{ZSV}|)
\]

(7)

Then, the average NP current \(i_{\text{NP}}\) introduced by the three phases in a switching cycle is:

\[
i_{\text{NP}}(m, I_m, \omega t, \varphi, u_{ZSV}) = i_{\text{NPmax}} + i_{\text{NPmid}} + i_{\text{NPmin}}
\]

(8)

It can be seen from (8) that \(i_{\text{NP}}\) is related to \(m, I_m, \omega t, \varphi\) and \(u_{ZSV}\), where \(m\) and \(\omega t\) are determined by operating point, \(I_m\) and \(\varphi\) are determined by load, and \(u_{ZSV}\) is determined by modulation strategy. The NPV variation \(\Delta u_{\text{NP}}\) caused by the NP current in a switching cycle can be expressed as:

\[
\Delta u_{\text{NP}} = u_{C1} - u_{C2} = \frac{i_{\text{NP}}}{2C} T_s
\]

(9)

where \(C\) is the capacitance of \(C_1\) and \(C_2\), and \(T_s\) is the switching period.

From (9), it can be seen that positive NP current will cause NPV decrease and negative value will cause it increase. To facilitate the analysis, \(i_{\text{NP}}, i_{\text{NP}}^{*}\) and \(\Delta u_{\text{NP}}^{*}\) are used to represent the normalized phase current, NP current and NPV variation in a switching cycle respectively by assuming \(I_m = 1\).

B. THE NECESSARY CONDITION OF MAINTAINING NPV BALANCE IN A SWITCHING CYCLE

In [26], the necessary condition of maintaining NPV balance in a switching cycle is discussed. To achieve that, \(i_{\text{NP}}^{*}\) should equal to zero to make \(\Delta u_{\text{NP}} = 0\) in a switching cycle.

Under a certain condition of \(m, \omega t\) and \(\varphi\), \(i_{\text{NP}}\) can be only adjusted by \(u_{ZSV}\). Assuming \(i_{\text{NPmax}}^{*}\) and \(i_{\text{NPmin}}^{*}\) respectively denote the maximum and minimum NP current in a switching cycle. In \(\gamma\), the relationship between \(i_{\text{NP}}^{*}\) and \(u_{ZSV}\) is linear or piecewise linear. Thus, if \(i_{\text{NPmin}}^{*} \leq 0 \leq i_{\text{NPmax}}^{*}\), there must be at least one \(u_{ZSV}\) satisfying \(i_{\text{NP}}^{*} = 0\); otherwise, NPV balance in a switching cycle is impossible.

C. THE NECESSARY CONDITION OF MAINTAINING NPV BALANCE IN A FUNDAMENTAL CYCLE

Generally, NPV balance in a switching cycle is usually not satisfied. Then, NPV balance in a fundamental cycle is at least required to ensure normal operation.

In a fundamental cycle, the NPV variation \(u_{\text{NPf}}\) can be expressed as:

\[
u_{\text{NPf}} = \frac{\int_0^{2\pi} i_{\text{NP}} d\omega}{\omega \cdot 2C} = \frac{\Delta u_{\text{NPf}}}{2\omega C}
\]

(10)

where \(\Delta u_{\text{NPf}} = \int_0^{2\pi} i_{\text{NP}} d\omega\) is related to \(m, \varphi\) and \(u_{ZSV}\), which represents the NPV variation characteristic in a fundamental cycle.

To effectively control NPV, particularly to avoid gradually increased DC offset, attention should be paid to \(\Delta u_{\text{NPf}}\). If \(i_{\text{NPmin}}^{*}\) or \(i_{\text{NPmax}}^{*}\) is always selected in each switching cycle, two extreme variations in a fundamental cycle are respectively obtained as:

\[
\begin{align*}
u_{\text{NPfmax}}^{*} &= \int_0^{2\pi} i_{\text{NPmax}}^{*}(m, \omega t, \varphi) d\omega \\
u_{\text{NPfmin}}^{*} &= \int_0^{2\pi} i_{\text{NPmin}}^{*}(m, \omega t, \varphi) d\omega
\end{align*}
\]

(11)

To ensure NPV balance in a fundamental cycle, \(\Delta u_{\text{NPf}}^{*} = 0\) should be satisfied, and it is available while \(u_{\text{NPfmax}}^{*}\) and \(u_{\text{NPfmin}}^{*}\) have opposite signs. Otherwise, the gradually increased DC offset on NPV is caused. Therefore, \(u_{\text{NPfmax}}^{*}\) and \(u_{\text{NPfmin}}^{*}\) can be finally used to determine whether the TLI can operate normally from the point view of NPV balance.

III. TWO REPRESENTATIVE FAULT-TOLERANT CONTROL STRATEGIES

When OC fault occurs in an inner switch of one phase, the following two representative fault-tolerant control strategies were proposed in [23]. (1) The fault phase always operates in two-level mode, which is called as 2L/FTC. (2) The fault phase operates in three-level mode in the normal half fundamental cycle, and operates in two-level mode in the fault half fundamental cycle, which is called as 2L + 3L/FTC.

A. 2L/FTC

If OC fault occurs in one inner switch of phase X, it always operates in two-level mode and only 0 and 2 level are outputted. After injecting \(u_{ZSV}\), the modulation voltage is \(u'_{X}\),
and the duty ratio of the corresponding level is:

\[ d_{X2} = \frac{1 + u_X'}{2}, \quad d_{X0} = 1 - d_{X2} \]  

(12)

For normal phase Y, it still operates in three-level mode. After injecting \( u_{ZSV} \), the modulation voltage is \( u_Y' \), and the duty ratio of the corresponding level is:

\[
\begin{align*}
& d_{Y2} = u_Y', \quad d_{Y1} = 1 - d_{Y2}, \quad d_{Y0} = 0 \quad \text{when } u_Y' \geq 0 \\
& d_{Y2} = 0, \quad d_{Y0} = 1 - d_{Y2}, \quad d_{Y0} = -u_Y' \quad \text{when } u_Y' < 0
\end{align*}
\]

(13)

B. 2L+3L/FTC

If OC fault occurs in an inner switch of phase X, it operates in two-level mode in fault half fundamental cycle and operates in three-level mode in normal half fundamental cycle. After injecting \( u_{ZSV} \), the modulation voltage is \( u_X' \), and the duty ratio of the corresponding level is calculated as follows:

\[
\delta X_2 \text{ OC fault:}
\]

\[
\begin{align*}
& i_X > 0 : d_{X2} = \frac{1 + u_X'}{2}, \quad d_{X0} = 1 - d_{X2} \\
& i_X \leq 0 : u_X' > 0 : d_{X2} = u_X', \quad d_{X1} = 1 - d_{X2}, \quad d_{X0} = 0 \\
& u_X' \leq 0 : d_{X0} = -u_X', \quad d_{X1} = 1 - d_{X1}, \quad d_{X2} = 0
\end{align*}
\]

(14a)

\[
\delta X_3 \text{ OC fault:}
\]

\[
\begin{align*}
& i_X < 0 : d_{X2} = \frac{1 + u_X'}{2}, \quad d_{X0} = 1 - d_{X2} \\
& i_X \geq 0 : u_X' > 0 : d_{X2} = u_X', \quad d_{X1} = 1 - d_{X2}, \quad d_{X0} = 0 \\
& u_X' \leq 0 : d_{X0} = -u_X', \quad d_{X1} = 1 - d_{X1}, \quad d_{X2} = 0
\end{align*}
\]

(14b)

For normal phase, the duty ratio of the corresponding level can be referred to (13).

C. THE VARIATION OF NP CURRENT WITH RESPECT TO ZSV

In a switching cycle, the polarity of the modulation voltage may be changed after injecting \( u_{ZSV} \). So, \( i_{NP}^* \) may be not linear with \( u_{ZSV} \).

If the voltage of phase X satisfies with \(-u_X \in \gamma\), the duty ratio of 1 level of this phase will gradually increase while \( u_{ZSV} \) increasing from \(-1-u_{min}\) to \(-u_X\). When \( u_{ZSV} = -u_X \), the duty ratio of 1 level of this phase is 100% and it will gradually decrease while \( u_{ZSV} \) increasing from \(-u_X\) to \(-u_{max}\). Since \( u_{ZSV} = -u_X \) is the demarcation point, the NP current introduced by this phase is different on both sides of this point. There are at most three demarcation points in \( \gamma \). Since the variation of \( i_{NP}^* \) with respect to \( u_{ZSV} \) exhibits a linear relationship in each segment, \( i_{NP}^{*\text{max}} \) and \( i_{NP}^{*\text{min}} \) will be acquired at the boundary points or demarcation points.

It should be noted that while 2L/FTC is adopted under OC fault of \( S_{A2} \) or \( S_{A3} \), the NP current will not be affected by phase A. Thus, \( u_{ZSV} = -u_A \) is not the demarcation point.

However, when 2L+3L/FTC is adopted, \( u_{ZSV} = -u_A \) is the demarcation point in the normal half fundamental cycle and it is not the demarcation point in the fault half fundamental cycle.

Combining with the above analysis, when OC fault occurs in \( S_{A2} \), the classification and criterion of the boundary points and demarcation points are given in Table 1 under 2L/FTC and 2L+3L/FTC. There are four cases. (1) No demarcation point is located in \( \gamma \). (2) Only one demarcation point is located in \( \gamma \). (3) Two demarcation points are located in \( \gamma \). (4) Three demarcation points are all located in \( \gamma \). The four cases are respectively shown in Fig. 2, where \( u_{ZSV1} \), \( u_{ZSV2} \) and \( u_{ZSV3} \) are the demarcation points; \( u_{ZSV4} = -1 - u_{min} \) and \( u_{ZSV5} = 1 - u_{max} \) are the boundary points.

D. THE NPV CONTROL METHOD

For NPV control, not only the NPV variation in a switching cycle should be taken into account, but also the DC offset on NPV should not be produced. The NPV control is achieved by extracting or injecting current from NP. Since the NP current is related to \( u_{ZSV} \), the NPV control method based on ZSV planning proposed in [26] is adopted.

Assuming \( u_{NP,\text{init}} = u_{dc} - i_{C2} \) is the initial offset on NPV in a switching cycle. To maintain NPV balance, the NPV variation \( \Delta u_{NP} \) in this switching cycle should be satisfied as:

\[
\Delta u_{NP} = -u_{NP,\text{init}} \quad (15)
\]

Substituting (15) into (9), the NP current reference value \( i_{NP}^* \) can be obtained:

\[
i_{NP}^* = \frac{-2u_{NP,\text{init}}C}{I_mT_S} \quad (16)
\]

The NPV control method based on ZSV planning is to solve the linear equation according to \( i_{NP}^* \) calculated by (16) and then determine the injected ZSV reference value \( u_{ZSVg}^\text{ref} \) to achieve NPV balance.

Finally, the rule of NPV control method based on ZSV planning is summarized as:

\[
\begin{align*}
\text{if } (i_{NP}^* > i_{NP}^{\text{max}}), & \quad u_{ZSVg}^\text{ref} = u_{ZSV} @ i_{NP}^{\text{max}} \\
\text{if } (i_{NP}^* < i_{NP}^{\text{min}}), & \quad u_{ZSVg}^\text{ref} = u_{ZSV} @ i_{NP}^{\text{min}} \\
\text{if } (i_{NP}^{\text{min}} \leq i_{NP}^* \leq i_{NP}^{\text{max}}), & \quad u_{ZSVg}^\text{ref} = i_{NP}^* - i_{NP}^\text{g} \left( u_{ZSVh} - u_{ZSVg} \right) + u_{ZSVg} \\
& \quad g = 1, 2, 3, 4, \text{ or } 5
\end{align*}
\]

(17)

where \( i_{NP}^\text{g} \) is located in \([i_{NP}^{\text{min}}, i_{NP}^{\text{max}}]\) for the third case, and \( u_{ZSVg} \) and \( u_{ZSVh} \) are the corresponding ZSVs of \( i_{NP}^{\text{g}} \) and \( i_{NP}^{\text{g}} \).

In eq. (17), NPV cannot be adjusted to \( u_{dc} \) within a switching cycle for the former two cases, and it can be achieved for the third case.

IV. APPLICATION RANGES OF FAULT-TOLERANT CONTROL STRATEGIES UNDER DIFFERENT FAULT TYPES

According to Section II, in order to ensure long-term reliable operation of T-type TLI with OC fault of inner switches, the possible control of NPV under different fault types...
TABLE 1. The classification and criterion of the demarcation and boundary points under 2L/FTC and 2L+3L/FTC with OC fault of $S_A2$.

| Condition | $U_{ZSV1}$ | $U_{ZSV2}$ | $U_{ZSV3}$ |
|-----------|------------|------------|------------|
| Case 1 2L/FTC | $-u_{b2} - u_c \notin \gamma$ | — | — |
| 2L+3L/FTC | $-u_{c} - u_{b2} - u_c \notin \gamma$ | $-u_c$ | — |
| Case 2 2L/FTC | $-u_{c} \notin \gamma$ and $-u_{b2} - u_c \notin \gamma$ | $-u_c$ | — |
| 2L+3L/FTC | $-u_{c} \notin \gamma$ and $-u_{b2} - u_c \notin \gamma$ | $-u_c$ | — |
| Case 3 2L/FTC | $-u_{c} \notin \gamma$ and $-u_{b2} - u_c \notin \gamma$ | $\min(-u_{b5}, -u_{c})$, $\max(-u_{b5}, -u_{c})$ | — |
| 2L+3L/FTC | $-u_{c} \notin \gamma$ and $-u_{b2} - u_c \notin \gamma$ and $i_f > 0$ | $\min(-u_{b5}, -u_{c})$, $\max(-u_{b5}, -u_{c})$ | — |
| Case 4 2L/FTC | $-u_{c} \notin \gamma$ and $-u_{b2} - u_c \notin \gamma$ and $i_f < 0$ | $\min(-u_{b5}, -u_{c})$, $\max(-u_{b5}, -u_{c})$ | — |

FIGURE 2. $i_{bP}$ as a function of $U_{ZSV}$ under 2L/FTC and 2L+3L/FTC.

should be revealed for 2L/FTC and 2L+3L/FTC. Based on the analysis given in Section II, the distributions of $i_{bP}^\text{NPmax}$, $i_{bP}^\text{NPmin}$, $\Delta u_{bP}^\text{NPmin}$, and $\Delta u_{bP}^\text{NPmax}$ should be paid attentions. The former and the latter can be used to determine whether the NPV balance is maintained in a switching cycle or in a fundamental cycle, respectively. Especially, the application ranges of a fault-tolerant control strategy are determined by the latter, which should be paid more attentions.

**A. INNER SWITCH WITHOUT OC FAULT**

While $\varphi = 0$ and $\pi/2$, the distributions of $i_{bP}^\text{NPmax}$ and $i_{bP}^\text{NPmin}$ with respect to $m$ and $\omega t$ without OC fault of inner switch can be referred to Fig. 2 in [26]. It found that $i_{bP}^\text{NPmin}$ is satisfied almost in the entire operating regions while $\varphi = 0$, which indicates that the NPV balance can be achieved in a switching cycle. However, while $\varphi = \pi/2$, $i_{bP}^\text{NPmin} < 0 \leq i_{bP}^\text{NPmax}$ is only satisfied at lower modulation index ($m < 0.577$). This is the reason why obvious NPV variation appears under condition of high modulation index and low PF in practice.

Moreover, the distributions of $\Delta u_{bP}^\text{NPmin}$ and $\Delta u_{bP}^\text{NPmax}$ with respect to $m$ and $\varphi$ can be referred to Fig. 4 in [26]. It found that $\Delta u_{bP}^\text{NPmin}$ and $\Delta u_{bP}^\text{NPmax}$ always have opposite signs to ensure NPV balance in a fundamental cycle. The analysis is well consistent with the general cognition of NPV variation for TLI in normal operation, which indirectly indicates that the theoretical analysis is feasible.

In the subsequent analysis, the distributions of $i_{bP}^\text{NPmax}$ and $i_{bP}^\text{NPmin}$ are no longer given because the NPV balance is not necessary in a switching cycle, but it is necessary in a fundamental cycle. So, only $\Delta u_{bP}^\text{NPmin}$ and $\Delta u_{bP}^\text{NPmax}$ are presented to determine the application ranges.
B. THE APPLICATION RANGES OF 2L/FTC

When 2L/FTC is adopted for different $m$ and $\varphi$, the distributions of $\Delta u_{NP, \text{max}}$ and $\Delta u_{NP, \text{min}}$ under OC fault of single-phase inner switches can be referred to Fig. 1(b) in [25]. Under OC fault of two-phase inner switches, the distributions are shown in Fig. 3. It can be seen that $\Delta u_{NP, \text{max}}$ is always higher than zero, and $\Delta u_{NP, \text{min}}$ is always lower than zero. So, the necessary condition of maintaining NPV balance in a fundamental cycle is always satisfied. That makes sense because the NPV can be adjusted by the normal phase.

When OC fault occurs in inner switches of all phases, T-type TLI is completely degraded into two-level inverter under 2L/FTC, and the NPV control ability is thus lost. In this case, the DC offset on NPV cannot be eliminated only by injecting $u_{ZSV}$. Other methods should be used to solve this problem, such as resistance equalization. However, it is noted that the two-level operation is unaffected by NPV.

Therefore, 2L/FTC is always competent for fault-tolerant operation under arbitrary OC fault in inner switch.

C. THE APPLICATION RANGES OF 2L+3L/FTC

When single or multiple phase inner switches OC fault occurs, there are many cases under 2L+3L/FTC, which are divided into five fault types: (1) single-phase inner switch fault ($S_{A3}$); (2) two-phase inner switches fault with the same direction ($S_{A3}$ and $S_{B3}$); (3) two-phase inner switches fault with the opposite direction ($S_{A3}$ and $S_{B2}$); (4) three-phase inner switches fault with two phases in the same direction ($S_{A3}$, $S_{B3}$ and $S_{C2}$); (5) three-phase inner switches fault with the same direction ($S_{A3}$, $S_{B3}$ and $S_{C3}$). Although not all the OC fault types in inner switches are listed, the other types can be obtained by duality. For example, OC fault in $S_{A2}$, $S_{B2}$ and $S_{C3}$ are dual. Thus, only the above five fault types are discussed.
For 2L+3L/FTC, the distributions of $\Delta u_{NPmin}$ and $\Delta u_{NPmax}$ under the first fault type can be referred to Fig. 1(c) in [25], and the distributions are respectively shown in Figs. 4-7 under the latter four fault types. It can be seen that the necessary condition of maintaining NPV balance in a fundamental cycle is always satisfied in the whole regions of $m$ and $\varphi$ only in Fig. 5. For the first fault type, $\Delta u_{NPmin}$ and $\Delta u_{NPmax}$ are both higher than zero around $\varphi = \pi/2$ and $3\pi/2$ with high $m$, which indicates that NPV is not controllable in these regions, and gradually increased DC offset on NPV is caused. There are similar phenomena in Figs. 4 and 6. Especially for Fig. 7, $\Delta u_{NPmin}$ and $\Delta u_{NPmax}$ are always higher than zero in the whole regions, which makes NPV decrease continuously. Thus, in these regions, NPV is out of control, and three-level operation is no longer allowed.

From these figures, it can be seen that 2L+3L/FTC can be adopted unconditionally only under fault type 3, and the application ranges should be taken into account for the other fault types. Especially for the fault condition 5 shown in Fig. 7, 2L+3L/FTC cannot be adopted because that NPV is varied monotonically. In these cases, the inverter will stop working because of unbalance protection. Therefore, in fact, 2L+3L/FTC is not always competent for fault-tolerant operation under arbitrary fault type.

To better reveal the availability of 2L+3L/FTC, the application ranges under the five fault types are presented in Fig. 8. In Fig. 8, $0 < \Delta u^{e}_{NPmin} < \Delta u^{e}_{NPmax}$ is satisfied in the red area, in which NPV is out of control, and $\Delta u^{e}_{NPmin} < 0 < \Delta u^{e}_{NPmax}$ is satisfied in the green area, in which NPV is controllable. From Fig. 8, it found that 2L+3L/FTC can be used in full regions only under fault type 3, in most regions under fault types 1 and 4, and the regions become small under fault type 2. Moreover, under fault type 5, 2L+3L+3L/FTC can no longer be used. The results shown in Fig. 8 can be utilized to easily determine whether 2L+3L/FTC is able to deal with the specific fault types under given conditions of $m$ and $\varphi$.

Finally, the possibility of suppressing the DC offset on NPV under different $m$ and $\varphi$ is given in Table 2 for 2L/FTC and 2L+3L/FTC under different fault types and conditions of $m$ and $\varphi$.

V. EXPERIMENTS

In order to verify the theoretical analysis, the prototype of T-type TLI with key parameters listed in Table 3 was established in the laboratory, which is shown in Fig. 9. The main controller is Freescale’s DSP MC56F84789 and the switching device is SEMiX-205TMLI12E4B. Because the application ranges of the fault-tolerant control strategies are mainly focused on, open-loop control is applied in the experiments.
for fair comparison to avoid the potential effect by the control loop.

In the experiments, the adopted fault diagnosis method can be referred to [24]. After detecting fault type, 2L/FTC or 2L+3L/FTC is applied, and the PWM sequences are generated according to eqs. (12)-(14). Moreover, the injected ZSV is determined by eq. (17).

Figs. 10-17 shows the corresponding experimental results with different fault types respectively under 2L/FTC and 2L+3L/FTC, where $u_{C1}$ and $u_{C2}$ denote the upper and lower capacitor voltage, $u_A$, $u_B$, and $u_{AB}$ represent the voltage of phase A, B and phase A to B, $i_A$, $i_B$ and $i_C$ denote the three phase currents, respectively.

As shown in Fig. 10, with OC fault in $S_{A3}$, gradually increased DC offset on NPV is caused and the phase current is distorted. However, while 2L/FTC is involved, either way, the DC offset emerged in fault stage is always effectively eliminated. It can be also seen that the NPV fluctuation in fault-tolerant operation is obviously larger than that in normal operation, and its fluctuation frequency is mainly varied from three to one times of fundamental frequency.

With OC fault in $S_{A3}$ and $S_{B3}$ as shown in Fig. 11, similar conclusions as that in Fig. 10 can be drawn. As obviously shown in Fig. 11(c), the three phase currents seem unbalanced. In fact, it finally gets into steady state, but a relatively long time is needed. That’s due to the load condition of small resistance and large inductance.

With OC fault in $S_{A3}$, $S_{B3}$ and $S_{C3}$ as shown in Fig. 12, the T-type TLI is completely degraded into two-level inverter under 2L/FTC. Thus, NPV is no more adjustable, and the DC offset on NPV always exists. Although NPV is always unbalanced, the inverter can work normally in two-level operation. However, the NPV unbalance protection may be triggered during the fault diagnosis process.

The experimental results shown in Figs. 10-12 indicate that 2L/FTC is always effective for fault-tolerant operation under arbitrary OC fault in inner switch, which are consistent with the theoretical analysis in Section IV. And the NPV balance

| TABLE 3. Experimental parameters. |
|----------------------------------|
| Parameter                        | Value |
| DC-link voltage                  | 200V  |
| Upper and lower dc-link capacitor| 1300μF |
| Resistive-inductive load for high PF ($Z_{L1}$) | $6\times10^2\Omega$ |
| Resistive-inductive load for low PF ($Z_{L2}$) | $2\times10^3\Omega$ |
| Resistive-inductive load for ZSV ($Z_{L3}$) | $6\times10^2\Omega$ |
| Switching frequency              | 16kHz |
can be ensured as long as not all the phases have OC fault in inner switch.

As shown in Fig. 13 under 2L+3L/FTC, with OC fault in S\textsubscript{A3}, the suppression of emerged DC offset on NPV is related to the load, and it is effective while \( m = 0.9, \varphi = \pi/12 \) and \( m = 0.3, \varphi = 5\pi/12 \), but invalid while \( m = 0.9, \varphi = 5\pi/12 \). Only in Fig. 13(b), the DC offset on NPV can not be eliminated, which increases gradually, and the NPV unbalance protection is finally triggered. Thus, in the case of S\textsubscript{A3} OC fault, 2L+3L/FTC can not be applied under the condition of high modulation index and low PF, but it is competent for the other conditions.

With OC fault in S\textsubscript{A3} and S\textsubscript{B3} under 2L+3L/FTC as shown in Fig. 14, the suppression of emerged DC offset on NPV is mainly related to the load PF, which is a little different from that presented in Fig. 13. In this case, the emerged DC offset on NPV can not be eliminated under low PF (\( \varphi = 5\pi/12 \)) condition, but it is eliminated under high PF (\( \varphi = \pi/12 \)) condition.

With OC fault in S\textsubscript{A3} and S\textsubscript{B2} as shown in Fig. 15, either way, the DC offset on NPV emerged in faulty stage is always effectively suppressed by applying 2L+3L/FTC. That’s because the NP current can be compensated by each other for the two faulty phases. Under this fault type, NPV balance is always ensured, and 2L+3L/FTC can be effectively used in the whole operating regions.

As shown in Fig. 16, with OC fault in S\textsubscript{A3}, S\textsubscript{B3} and S\textsubscript{C2}, very similar conclusions as that of Fig. 13 can be drawn.

With OC fault in S\textsubscript{A3}, S\textsubscript{B3} and S\textsubscript{C3} as shown in Fig. 17, either way, it can be seen that the DC offset on NPV is always gradually increased after applying 2L+3L/FTC. That’s because the NP current can only flow out from NP in this fault type, which makes NPV continuously decrease. In practice, it will finally trigger the NPV unbalance protection.

All the experimental results of Figs. 13-17 are well consistent with the theoretical analysis in Section IV C, and the correctness of Fig. 8 is verified.

From the above experimental results, it also found that 2L/FTC can be applied unconditionally, but the application ranges of 2L+3L/FTC must be considered in terms of fault type and operation condition of \( m \) and \( \varphi \) in practice.

VI. CONCLUSION

For T-type TLI, the necessary conditions of maintaining NPV balance respectively in a switching cycle and in a fundamental cycle are simply reviewed in this paper. Two representative fault-tolerant control strategies are adopted when OC fault
occurs in inner switches, and an NPV control method is used based on planned ZSV injection. According to the necessary conditions, the application ranges of the two fault-tolerant control strategies under different fault types and operation condition of $m$ and $\varphi$ are respectively revealed.

As discussed, for 2L/FTC, regardless of OC fault in inner switches of single or multiple phases, there is no gradually increased DC offset on NPV. But for 2L+3L/FTC, the NPV balance cannot be maintained in some operation conditions. Therefore, when 2L+3L/FTC is adopted, operating conditions must be taken into account under different fault types. If necessary, it can switch to 2L/FTC to extend the fault-tolerant operation range, even though the performance is degraded to some degree.

REFERENCES

[1] J.-S. Lee, U.-M. Choi, and K.-B. Lee, “Comparison of tolerance controls for open-switch fault in a grid-connected T-type rectifier,” IEEE Trans. Power Electron., vol. 30, no. 10, pp. 5810–5820, Oct. 2015.

[2] R. Chen, J. Niu, H. Gui, Z. Zhang, F. Wang, L. M. Tolbert, D. J. Costinett, B. J. Blalock, and B. B. Choi, “Modeling, analysis, and reduction of harmonics in paralleled and interleaved three-level neutral point clamped inverters with space vector modulation,” IEEE Trans. Power Electron., vol. 35, no. 4, pp. 4411–4425, Apr. 2020.

[3] M. Schweizer and J. W. Kolar, “Design and implementation of a highly efficient three-level T-Type converter for low-voltage applications,” IEEE Trans. Power Electron., vol. 28, no. 2, pp. 899–907, Feb. 2013.

[4] L. Zhang, X. Lou, C. Li, F. Wu, Y. Gu, G. Chen, and D. Xu, “Evaluation of different Si/SiC hybrid three-level active NPC inverters for high power density,” IEEE Trans. Power Electron., vol. 35, no. 5, pp. 8824–8836, Aug. 2020.

[5] Q. Zhang, X. Xing, and K. Sun, “Space vector modulation method for simultaneous common mode voltage and circulating current reduction in parallel three-level inverters,” IEEE Trans. Power Electron., vol. 34, no. 4, pp. 3053–3066, Apr. 2019.

[6] S.-M. Kim, I. J. Won, J. Kim, and K.-B. Lee, “DC-link ripple current reduction method for three-level inverters with optimal switching pattern,” IEEE Trans. Ind. Electron., vol. 65, no. 12, pp. 9204–9214, Dec. 2018.

[7] K. Wang, Y. Tang, and C.-J. Zhang, “Open-circuit fault diagnosis and tolerance strategy applied to four-wire T-type converter systems,” IEEE Trans. Power Electron., vol. 34, no. 6, pp. 5764–5778, Jun. 2019.

[8] T. B. Hashfi, S. Mekhilef, S. Ogura, and M. Mubin, “Modular multilevel converter modulation technique with fault-tolerant capability,” in Proc. IEEE 13th Int. Conf. Power Electron. Drive Syst. (PEDS), Toulouse, France, Jul. 2019, pp. 1–6.

[9] T. B. Hashfi, S. Mekhilef, M. Mubin, M. Seyedmahmoudian, B. Horan, and A. Stojcevski, “Adaptive carrier-based PDPWM control for modular multilevel converter with fault-tolerant capability,” IEEE Access, vol. 8, pp. 26739–26748, Feb. 2020.

[10] S. Moshenzi, M. Zarghane, and S. Kaboli, “A series stacked IGBT switch with robustness against short-circuit fault for pulsed power applications,” IEEE Trans. Power Electron., vol. 33, no. 5, pp. 3779–3790, May 2018.

[11] A. Morozumi, K. Yamada, T. Miyasaka, S. Sumi, and Y. Seki, “Reliability of power cycling for IGBT power semiconductor modules,” IEEE Trans. Ind. Appl., vol. 39, no. 3, pp. 665–671, May/Jun. 2003.

[12] R. S. Chokhawala, J. Catt, and L. Kiraly, “A discussion on IGBT short-circuit behavior and fault protection schemes,” IEEE Trans. Ind. Appl., vol. 31, no. 2, pp. 256–263, Mar/Apr. 1995.

[13] K.-H. Chao, L.-Y. Chang, and F.-Q. Xu, “Three-level T-type inverter fault diagnosis and tolerant control using single-phase line voltage,” IEEE Access, vol. 8, pp. 44075–44086, Mar. 2020.

[14] L. Li, S. Shi, B. Wang, G. Wang, W. Wang, and D. Xu, “Fault diagnosis and tolerant control of single IGBT open-circuit failure in modular multilevel converters,” IEEE Trans. Power Electron., vol. 31, no. 4, pp. 3165–3174, Apr. 2016.

[15] U.-M. Choi, J.-S. Lee, F. Blaabjerg, and K.-B. Lee, “Open-circuit fault diagnosis and fault-tolerant control for a grid-connected NPC inverter,” IEEE Trans. Power Electron., vol. 31, no. 10, pp. 7234–7247, Oct. 2016.
WEIDONG JIANG (Member, IEEE) was born in Sichuan, China, in 1976. He received the B.S. and Ph.D. degrees in electrical engineering from the Hefei University of Technology, Hefei, China, in 1999 and 2004, respectively.

Since June 2004, he has been with the School of Electrical Engineering and Automation, Hefei University of Technology, Hefei, China, where he is currently a Professor. His research interests include electrical machines and their control systems, power electronics, and electric drives.

MINGNA MA was born in Henan, China, in 1986. She received the B.S. degree in electrical engineering from Henan Polytechnic University, in 2007, and the Ph.D. degree in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2014.

Since November 2014, she has been with the School of Electrical Engineering and Automation, Hefei University of Technology, Hefei, China, where she is currently an Associate Professor. Her research interests include PM linear motor and linear electromagnetic launch.

QINGYAN ZHANG was born in Jinan, Shandong, China. He received the B.S. degree from the School of Electrical and Information Engineering, Qufu Normal University, Rizhao, China, in 2018. He is currently pursuing the M.S. degree with the Department of Electrical Engineering, Hefei University of Technology, Hefei, China.

His main research interests include power electronics and power converters in renewable energy.

XINMEI HUANG was born in Hefei, Anhui, China. She received the B.S. degree from the Department of Electrical Engineering and Automation, Anhui Polytechnic University, Wuhu, China, in 2018. She is currently pursuing the M.S. degree with the Department of Electrical Engineering, Hefei University of Technology, Hefei, China.

Her main research interests include power electronics and power converters in renewable energy.

***