Interleaved Modulation Scheme With Optimized Phase Shifting for Double-Switch Buck-Boost Converter

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ABSTRACT Owing to low voltage stresses, wide range of input voltage and the same polarity of output voltage and input voltage, double-switch buck-boost converter (DSBBC) is a popular choice to achieve dc/dc conversion in photovoltaic generations (PV), power factor correction (PFC), portable devices and so on. Combined control (CC) makes DSBBC operate efficiently, but large ripples of output voltage are unavoidable during mode transition. With two equal duties, interleaved modulation (IM) makes the inductor ripple current decrease remarkably compared with synchronous modulation (SM) while inductor average current is still high. By introducing duty offset, inductor average current declines and efficiency is enhanced obviously under interleaved modulation with duty cycle offset (IMDO). However, with 180-degree phase-shifted angle, the ripple current is not low enough in some cases. Thus, to make further improvement on ripple current, an interleaved modulation scheme with optimized phase shifting (IMOPS) is proposed for DSBBC in this paper. Current features, optimal phase-shifted angle (OPSA) and operating region under IMOPS are described meticulously. Besides, theoretical and quantitative comparisons of different modulation schemes are presented, including inductor average current, inductor ripple current and ratio of direct power transfer (DPT). Based on a 150W prototype, the feasibility and effectiveness of IMOPS are demonstrated by experimental results.

INDEX TERMS Double-switch buck-boost converter, optimal phase-shifted angle, inductor ripple current, efficiency promotion.

I. INTRODUCTION

Double-switch buck-boost converter (DSBBC) is regarded as a cascaded dc/dc device, where a buck converter lies ahead and a boost converter lies behind. By removing the intermediate capacitor and combining two inductors into one, a DSBBC is achieved, whose topology is drawn in Fig. 1. The converter contains two switches $S_1$, $S_2$, two diodes $D_1$, $D_2$, inductor $L$ and filter capacitor $C$. In addition, $R$ is the load resistor. By adjusting duty cycles, $d_1$ and $d_2$, input voltage $U_i$ can be stepped up or down to output voltage $U_o$, which is decided by

$$U_o/U_i = d_1/(1 - d_2)$$

In contrast with conventional single-switch buck-boost converter, DSBBC has advantages on lower voltage stresses on switches, wider range of input voltage, and the same polarity of output voltage and input voltage [1]. As for other buck-boost converters in non-isolated form, such as Cuk and SEPIC, DSBBC has a simpler circuit structure because of less components, which is beneficial to high power density and high efficiency [1], [2]. On account of these characteristics, DSBBC gains increasing attention in photovoltaic generations (PV) [3]–[5], electric vehicles or plug-in hybrid electric vehicles [6], [7], light-emitting-diode (LED) drivers [8], power factor correction (PFC) [9], [10], power supplies for communication systems [11] and portable devices [12], [13].

At present, research work on DSBBC is mainly focused on fast transient response [11], [12], smooth mode transition [14], [15], novel topologies [16], [17], and modulation
The main drawback of CC is the transition methods or compensation techniques, which is the transition between buck and boost modes needs additional denoting the switching period. Therefore, conduction and switching losses both decrease. Besides, owing to the avoidance of buck-boost mode, inductor average current descends and furthermore conduction loss declines. Based on [19], three possibilities of slope mismatching as well as working states of converter are analyzed in [20]. In addition, a symmetric dual-ramp generation circuit is designed to ease this problem. However, realization of these two approaches is difficult for digital converters.

As for phase-shifted angle optimization, there exist four strategies generally, including combined control (CC), synchronous modulation (SM), interleaved modulation (IM) and IM with duty cycle offset (IMDO). Under CC, the one hand, DSBBC fulfills the function of buck converter when \( S_2 \) is kept off and \( S_1 \) works in PWM style. On the other hand, DSBBC degrades into a boost converter when \( S_1 \) is kept on and \( S_2 \) is driven by PWM signal. However, smooth transition between buck and boost modes needs additional transition methods or compensation techniques, which is the main drawback of CC.

The load power \( P_L \) is divided into two parts, which are \( P_{\text{direct}} \) and \( P_{\text{indirect}} \). \( P_{\text{direct}} \) is directly from input source while \( P_{\text{indirect}} \) is from energy-storage components. If \( S_1 \) is turned on and \( S_2 \) is turned off, then the load is supplied by input source. This case is direct power transfer (DPT), which benefits high efficiency [21]. As Fig. 2 shows, when DSBBC operates under SM, the two switches are turned on and off meanwhile. Here, \( u_{S1}, u_{S2} \) are driving signals of \( S_1, S_2 \) while \( u_L, i_L \) are instant voltage and current of inductor respectively. And \( T_S \) denotes the switching period.

Nevertheless, large volume caused by large energy-storage components goes against power density improvement and efficiency is not high as a result of DPT absence. A two-edge modulation (TEM) scheme is presented in [2], where \( S_1 \) is triggered by trailing edge and \( S_2 \) is triggered by leading edge. In this case, \( S_1 \) is turned on at the beginning of a switching period while \( S_2 \) is turned off in the end of a switching period. Thus, the overlapping interval when switches are both on-state or off-state is narrowed and ripple current decreases somewhat. But the phase-shifted angle \( \phi \) isn’t the optimal choice and varies according to duty cycle. In [21], IM is introduced as Fig. 3 illustrates, where \( d_1 = d_2 \) and phase-shifted angle between two duties is 180°. Due to this technique, inductance is reduced sharply and efficiency is promoted because DPT exists. On account of lower ripple current, IM is also put into use in modified topology [7].

Whereas, high inductor average current is still an existing issue to limit efficiency promotion. An asynchronous control scheme applied in non-inverting buck-boost converter with coupled inductor is proposed in [22]. Under this scheme, two semiconductors work with the synchronous moment of turning on, but asynchronous moment of turning off if \( d_1 \) is not identical to \( d_2 \). This scheme reduces ripple current in comparison with synchronous modulation on the same condition. Practically, inductor average current also descends
and phase-shifted angle is zero in this situation. Furthermore, the concept of duty offset is introduced in [23] and IMDO is put forward thereupon as Fig. 4 depicts. The influence of duty offset on inductor average current is analyzed. What’s more, small-signal model is also derived for realization of dual-loop control. Yet, the ripple current under IMDO is still not low enough in some cases, as phase-shifted angle is fixed at 180 degrees, which may be not always optimal in the whole range of input voltage. In other words, the strategy to reduce ripple current could be further researched. In this paper, interleaved modulation with optimized phase shifting (IMOPS) is proposed for DSBBC based on IMDO. Actually, average current and ripple current of inductor are both low under the proposed modulation scheme, which guarantee high conversion efficiency for various input voltages.

The reminder parts of this paper are organized as follows. In Section II, the impacts of phase-shifted angle on ripple current when duty offset exists are analyzed firstly. Subsequently, the phase-shifted angle and operating region under IMOPS are also described in this section. Comparisons of inductor average current, inductor ripple current and ratio of direct power transfer under different modulation schemes are elaborated in Section III. Experimental verifications and analysis are displayed in Section IV. At last, conclusions are presented in Section V.

II. CURRENT FEATURES OF DSBBC UNDER PROPOSED MODULATION SCHEME

A. DUTY OFFSET

When positive duty offset \( c \) exists, \( d_1 \) is enlarged and \( d_2 \) is narrowed by

\[
d_1 = d + c, \quad d_2 = d - c
\]

where \( d \) is the control signal.

According to [23], evaluation range of \( c \) is

\[
0 < c \leq \min\left(\frac{U_oD_{\text{max}} - U_{i,\text{max}}D_{\text{min}}}{2U_{i,\text{max}}}, \frac{U_{i,\text{min}}D_{\text{max}} - U_oD_{\text{min}}}{2U_o}\right)
\]

(3)

where \( D_{\text{max}} \) and \( D_{\text{min}} \) represent upper and lower bounds of effective duty cycles; \( U_{i,\text{max}} \) and \( U_{i,\text{min}} \) are upper and lower limits of input voltage.

Influenced by unavoidable non-idealities, switching noise and circuit layout in practical operations, \( D_{\text{min}} \) is not zero and \( D_{\text{max}} \) is not one. Virtually, \( D_{\text{min}} \) is the minimum duty cycle to turn on the switch and make it work in PWM style while \( D_{\text{max}} \) is the minimum duty cycle to keep the switch conducting all the time. When \( d_1 \) or \( d_2 \) is less than \( D_{\text{min}} \), it will jump to zero and the corresponding switch keeps off-state. When \( d_1 \) or \( d_2 \) is more than \( D_{\text{max}} \), it will jump to one and the corresponding switch is always on-state. With the help of oscilloscope, values of \( D_{\text{max}} \) and \( D_{\text{min}} \) can be acquired by testing the converter beforehand according to the aforementioned descriptions.

Therefore, duty cycles should follow that

\[
\begin{align*}
D_{\text{min}} &\leq d_1 = d + c \leq D_{\text{max}} \\
D_{\text{min}} &\leq d_2 = d - c \leq D_{\text{max}}
\end{align*}
\]

(4)

As a result, \( d \) has the limitations that

\[
D_{\text{min}} + c \leq d \leq D_{\text{max}} - c
\]

(5)

When DSBBC operates at buck mode, the condition is

\[
d_1 + d_2 < 1 \iff d < 0.5
\]

(6)

As for boost mode, the condition is

\[
d_1 + d_2 > 1 \iff d > 0.5
\]

(7)

Compared to SM and IM, inductor average current is reduced remarkably with the same load, which is evaluated as

\[
I_L = U_o/[(1 - d_2)R]
\]

(8)

Substituting (1) and (2) into (8), it is obtained that

\[
I_L = \frac{(U_o + U_i)U_o}{(1 + 2c)U_oR}
\]

(9)

From Fig. 5, \( I_L \) becomes lower if larger \( c \) is selected, which contributes much to efficiency promotion in practice.
B. SWITCHING STATES

To facilitate the analyzing process, the conditions listed below are considered to be satisfied:

1) all power semiconductors are ideal;
2) filter capacitor $C$ is large enough to ensure output voltage constant in a switching period;
3) DSBBC works at continuous current mode (CCM).

As for DSBBC, there exist four potential switching states in total and relevant current flow paths are outlined in Fig. 6. In a switching period, actual number of switching states depends on the adopted modulation scheme and the values of duty cycles. Each state is described as follows:

*State 1 [$S_1$ ON and $S_2$ OFF]:* As shown in Fig. 6 (a), at this state, $D_1$ is turned off because of closed $S_1$ while $D_2$ is turned on as a result of open $S_2$. Capacitor is charged and load is supplied by power source. If $U_i > U_o$, inductor is charged because of positive terminal voltage. And if $U_i < U_o$, inductor discharges while inductor current drops.

*State 2 [$S_1$ ON and $S_2$ ON]:* With both switches on-state, $D_1$ and $D_2$ are turned off due to inverse voltage, which is drawn in Fig. 6 (b). On the one hand, inductor is charged by input voltage and inductor current increases. On the other hand, load consumes the energy, which is stored in capacitor.

*State 3 [$S_1$ OFF and $S_2$ ON]:* In this situation, $D_1$ is on-state and provides path for inductor freewheeling. Besides, output voltage is maintained by energy-releasing capacitor. The state is displayed in Fig. 6 (c).

*State 4 [$S_1$ OFF and $S_2$ OFF]:* Inductor discharges by the way of two diodes and hence inductor current declines, which is described in Fig. 6 (d). As a consequence, capacitor is charged and load is supplied by $L$.

C. IMPACTS OF PHASE-SHIFTED ANGLE ON RIPPLE CURRENT

If duty offset is zero, the two duty cycles are equal. Based on the above, the phase-shifted angle under SM is zero while that under IM is 180 degrees. With positive duty offset, it is always satisfied that $d_1 > d_2$. To deeply research the influence of phase-shifted angle on inductor ripple current with duty offset, the whole range of $\varphi/360$ is divided into four sections firstly because it affects the switching states and duration time of each state quite a lot. In fact, whether $U_i > U_o$ or $U_i < U_o$, three critical points are common for $\varphi/360$, namely $d_1 - d_2$, $d_1$, and $1 - d_2$. Furthermore, the divided sections are $(0, d_1 - d_2)$, $(d_1 - d_2, d_1)$, $(d_1, 1 - d_2)$, and $(1 - d_2, 1)$ successively when $U_i > U_o$. Accordingly, the sections are $(0, d_1 - d_2)$, $(d_1 - d_2, 1 - d_2)$, $(1 - d_2, d_1)$, and $(d_1, 1)$ when $U_i < U_o$.

Considering buck mode first, where $d_1 + d_2 < 1$, take the section $(0, d_1 - d_2)$ as an example to calculate the inductor ripple current. As Fig. 7 (a) depicts, four intervals constitute a complete switching period. Detailed analysis is presented below, and $\Delta i_{L_n}$ represents the variation of inductor current in each interval.

*Interval 1 [$0 \sim t_1$]:* Converter works at State 1 and the duration time is $(\varphi/360)T_S$. The inductor is in charging process and its current rises up owing to positive terminal voltage. Following volt-second balance rule, it is obtained that

$$U_i - U_o = L\Delta i_{L_1} / [(\varphi/360)T_S]$$

*Interval 2 [$t_1 \sim t_2$]:* DSBBC functions at State 2 and it lasts $d_2T_S$. Thus, variation of inductor current is expressed as

$$U_i = L\Delta i_{L_2} / (d_2T_S)$$

*Interval 3 [$t_2 \sim t_3$]:* Status of all components in this interval is the same as that in Interval 1 while $t_3 - t_2 = (d_1 - d_2 - \varphi/360)T_S$.

Abiding by volt-second balance, it is satisfied that

$$U_i - U_o = L\Delta i_{L_3} / [(d_1 - d_2 - \varphi/360)T_S]$$

*Interval 4 [$t_3 \sim t_4$]:* With circuit operating at State 4, this interval continues for $(1 - d_1)T_S$. To be specific, $\Delta i_{L_4}$ is

![FIGURE 5. Curve of inductor average current versus duty offset.](image)

![FIGURE 6. Current flow paths of DSBBC. (a) $S_1$ ON, $S_2$ OFF, (b) $S_1$ ON, $S_2$ ON, (c) $S_1$ OFF, $S_2$ ON, (d) $S_1$ OFF, $S_2$ OFF.](image)
calculated by

\[-U_o = L\Delta i_{L1}/[(1 - d_1)T_S]\] (13)

Combined with (10), (11), (12) and (13), when \(\varphi/360\) is located in \((0, d_1 - d_2)\), inductor ripple current at buck mode is acquired by

\[\Delta I_L = -\Delta i_{L1} = (1 - d_1)U_o/(Lf_S)\] (14)

where \(f_S\) is the switching frequency.

In a similar way, when \(\varphi/360\) lies in \((d_1 - d_2, 1)\), \((d_1, 1 - d_2)\), or \((1 - d_2, 1)\), the inductor ripple current in those cases could be deduced one by one according to Fig. 7 (b), (c) and (d). The corresponding expressions of \(\Delta I_L\) are summarized in Table 1.

As for boost mode, where \(d_1 + d_2 > 1\), section \((1 - d_2, d_1)\) is taken for instance to derive \(\Delta I_L\). As Fig. 8 (c) displays, a whole period is made up of four intervals.

**Interval 1**[0−t1]: The power circuit operates at State 2 and the sustained time is \((d_2 + \varphi/360 - 1)T_S\). Hence, the increment of inductor current is expressed as

\[U_i = L\Delta i_{L1}/[(d_2 + \varphi/360 - 1)T_S]\] (15)

**Interval 2**[t1−t2]: Converter performs at State 1 and it lasts as long as \((1 - d_2)T_S\). Therefore, the decrement of inductor current is

\[U_i - U_o = L\Delta i_{L2}/[(1 - d_2)T_S]\] (16)

**Interval 3**[t2−t3]: Working state of converter stays the same as that in Interval 1 and this process continues for \((d_1 - \varphi/360)T_S\). Then, \(i_{L3}\) is calculated by

\[U_i = L\Delta i_{L3}/[(d_1 - \varphi/360)T_S]\] (17)

**Interval 4**[t3−t4]: DSBBC is at State 3 and length of the interval is \((1 - d_1)T_S\). Ignoring on-state voltage drops on semiconductors, inductor current keeps constant, which is considered as

\[0 = L\Delta i_{L4}/[(1 - d_1)T_S]\] (18)

Combined with (15), (16), (17) and (18), when \(\varphi/360\) is situated in \((1 - d_2, d_1)\), inductor ripple current at boost mode is attained by

\[\Delta I_L = \Delta i_{L1} + \Delta i_{L3} = (d_1 + d_2 - 1)U_i/(Lf_S)\] (19)

Likewise, when \(\varphi/360\) evaluates in \((0, d_1 - d_2), (d_1 - d_2, 1 - d_2)\) or \((d_1, 1)\), \(\Delta I_L\) could be derived according to Fig. 8 (a), (b) and (d) respectively. The corresponding expressions of \(\Delta I_L\) are listed in Table 2.

**FIGURE 7.** Key waveforms with duty offset when \(U_i > U_o\). (a) \(\varphi/360 < d_1 - d_2\), (b) \(d_1 - d_2 < \varphi/360 < d_1\), (c) \(d_1 < \varphi/360 < 1 - d_2\), (d) \(1 - d_2 < \varphi/360 < 1\).

**FIGURE 8.** Key waveforms with duty offset when \(U_i < U_o\). (a) \(\varphi/360 < d_1 - d_2\), (b) \(d_1 - d_2 < \varphi/360 < 1 - d_2\), (c) \(1 - d_2 < \varphi/360 < d_1\), (d) \(d_1 < \varphi/360 < 1\).
which is evaluated as $\phi$

Actually, the minimum $d_1$ for $(d_1-1)$

For buck mode, the ripple current at boost mode undergoes the same variation process as buck mode. From Fig. 9 (b), inductor ripple current at boost mode is

On the basis of Table 1 and Table 2, curves of $\Delta I_L$ versus $\phi/360$ are plotted in Fig. 9 to make the variation trend clear and definite. From Fig. 9 (a), at buck mode, the ripple current experiences four stages successively when $\phi/360$ ranges from 0 to 1. Particularly, they are remaining unchanged at first, decreasing secondly, remaining unchanged then and increasing finally. Besides, the maximum and minimum values of $\Delta I_L$ are

\[
\begin{align*}
\Delta I_{L,\text{max Bu}} &= (1 - d_1) U_o T_S / L \\
\Delta I_{L,\text{min Bu}} &= (1 - d_1 - d_2) U_o T_S / L \\
\end{align*}
\]

And the minimum $\Delta I_L$ is achieved in section $(d_1, 1 - d_2)$, which is the concern of this paper. In other words, when $\phi/360$ varies between $d_1$ and $1 - d_2$, $\Delta I_L$ is the lowest in the whole range of $\phi/360$ and it keeps constant despite the profile of inductor current. From Fig. 9 (b), inductor ripple current at boost mode undergoes the same variation process as buck mode while the maximum and minimum values of $\Delta I_L$ are

\[
\begin{align*}
\Delta I_{L,\text{max Bo}} &= d_2 U_o T_S / L \\
\Delta I_{L,\text{min Bo}} &= (d_1 + d_2 - 2) U_o T_S / L \\
\end{align*}
\]

Actually, the minimum $\Delta I_L$ is achieved in section $(1 - d_2, d_1)$. According to (20) and (21), $\Delta I_L$ could even reach zero theoretically if $d_1 + d_2 = 1$.

As a matter of convenience, $(d_1, 1 - d_2)$ at buck mode and $(1 - d_2, d_1)$ at boost mode are named as the optimized sections for $\phi/360$. According to (2), length and endpoint locations of $(d_1, 1 - d_2)$ or $(1 - d_2, d_1)$ vary with different $d$. However, $\phi_{\text{mid}}/360$, the midpoint of optimized sections, is unchanged, which is evaluated as

\[
\phi_{\text{OPS}}/360 = \phi_{\text{mid}}/360 = (d_1 + 1 - d_2)/2 = c + 0.5
\]
compare the proposed IMOPS with the scheme to achieve lowest $I_{PEAK}$. Actually, $I_{PEAK}$ could be deduced in a similar way. At buck mode, the lowest $I_{PEAK}$ is achieved when $\varphi/360 = d_1$. As for boost mode, lowest peak current is achieved when $\varphi/360 = 1 - d_2$. However, $I_{PEAK}$ doesn’t decrease obviously because $\Delta I_L$ keeps constant with the same $I_L$ in the optimized section. According to the definition, ratio of DPT is the same under two schemes, which indicates the same efficiency. That’s to say, inductor ripple current and converter efficiency couldn’t be further optimized with the same $L$ even if $I_{PEAK}$ is lowest. What’s more, there are obvious disadvantages to realize the lowest $I_{PEAK}$, which are mentioned in the previous paragraph. By contrast, these issues are avoidable in IMOPS. Based on the above analysis, the proposed IMOPS has more benefits than the scheme to realize the lowest $I_{PEAK}$.

D. DIVISION OF OPERATING REGION

As shown in Fig. 11, to draw a distinction between 180 degrees and OPSA, the whole operating region is divided into four parts according to $d_1$ and $d_2$, including Region A, B, C, and D. The input voltage is stepped down in Region A and B while it is stepped up in Region C and D.

Note that 180-degree phase-shifted angle is equivalent to that $\varphi/360 = 0.5$. At buck mode, when 0.5 lies between $d_1$ and $1 - d_2$, it is satisfied that

$$d_1 < 0.5 < 1 - d_2 \Leftrightarrow d_1 < 0.5, \quad d_2 < 0.5 \quad (23)$$

Combined with (2) and (5), it is obtained that

$$D_{min} + c \leq d < 0.5 - c \quad (24)$$

When 0.5 is outside the optimized section, namely

$$0.5 < d_1 < 1 - d_2 \Leftrightarrow d_2 < 0.5 < d_1 \quad (25)$$

Further, it is acquired that

$$0.5 - c < d < 0.5 \quad (26)$$

Thus, it is summarized that at buck mode, when $d$ meets (24), DSBBC operates in Region A. If so, the same ripple current is shared under IMDO and IMOPS. And when $d$ satisfies (26), DSBBC operates in Region B. In that case, the ripple current under IMOPS is lower than that under IMDO.

At boost mode, when 0.5 is in $(1 - d_2, d_1)$, namely

$$1 - d_2 < 0.5 < d_1 \Leftrightarrow d_1 > 0.5, \quad d_2 > 0.5 \quad (27)$$

Combined with (2) and (5), it is obtained that

$$0.5 + c < d < D_{max} - c \quad (28)$$

When 0.5 is outside $(1 - d_2, d_1)$, that is

$$d_1 > 1 - d_2 > 0.5 \Rightarrow d_2 < 0.5 < d_1 \quad (29)$$

Further, it is acquired that

$$0.5 < d < 0.5 + c \quad (30)$$

Therefore, it is concluded that at boost mode, when $d$ meets (28), DSBBC operates in Region D. If so, the same ripple current is shared under IMDO and IMOPS. When $d$ satisfies (30), DSBBC operates in Region C. In that case, the ripple current under IMOPS is reduced compared to IMDO. Furthermore, with fixed output voltage, a threshold value $U_{th1}$ for input voltage could be calculated with $d$ equal to $0.5 - c$ if converter works at buck mode. In virtue of $U_{th1}$, Region A and B are distinguished. Accordingly, if converter works at boost mode, another threshold value $U_{th2}$ is obtained when $d = 0.5 + c$. With the help of $U_{th2}$, Region C and D are told apart.

III. COMPARISONS OF DIFFERENT MODULATION SCHEMES

A. POWER TRANSFER STYLE

At State 1, DSBBC is in the progress of DPT. Therefore, the ratio of DPT, $P_{direct}/P_L$, is calculated by duration of State 1 occupying $T_S$. The ratio is a quantitative index to indicate efficiency, which considers $I_L$ and $\Delta I_L$ comprehensively. Only with $I_L$ and $\Delta I_L$, efficiency under different modulation schemes could not be distinguished in some cases. But the ratio could give comparative results directly. Thus, the ratio of DPT is necessary to be discussed independently.

In particular, $P_{direct}/P_L$ under IMDO is calculated by

$$P_{direct}/P_L = \begin{cases} 
(1 + 2c)U_o/(U_o + U_i), & d < 0.5, \quad d + c < 0.5 \\
0.5, & d < 0.5, \quad d + c > 0.5 \\
(1 + 2c)U_i/(U_o + U_i), & d > 0.5, \quad d - c < 0.5 \\
(1 + 2c)U_i(U_o + U_i), & d > 0.5, \quad d - c > 0.5 
\end{cases} \quad (31)$$

With IMOPS scheme applied, the ratio is expressed by

$$P_{direct}/P_L = \begin{cases} 
(1 + 2c)U_o/(U_o + U_i), & U_i > U_o \\
(1 + 2c)U_i/(U_o + U_i), & U_i < U_o 
\end{cases} \quad (32)$$

As for IM, the ratio is given by

$$P_{direct}/P_L = \begin{cases} 
U_o/(U_o + U_i), & U_i > U_o \\
U_i/(U_o + U_i), & U_i < U_o 
\end{cases} \quad (33)$$
When converter operates under CC, the ratio is

\[ \frac{P_{direct}}{P_L} = \begin{cases} \frac{U_o}{U_i}, & U_i > U_o \\ \frac{U_i}{U_o}, & U_i < U_o \end{cases} \quad (34) \]

Under SM scheme, the output power is entirely acquired from energy-storage inductor. Thus the ratio is zero.

\[ \frac{P_{direct}}{P_L} = 0 \quad (35) \]

In this section, \( U_i \) ranges from 12V to 60V and \( c \) is set as 0.2. Therefore, \( U_{th1} \) is 54V and \( U_{th2} \) is 16.7V respectively.

In Fig. 12, ratio of DPT is always zero under SM. As for IM, the ratio increases up to 0.5 until \( U_o = U_i \) and afterwards decreases gradually. For CC, the ratio rises up to one in scale while \( U_i < U_o \), and declines in inverse proportion while \( U_i > U_o \). When DSBBC works under IMDO scheme, the ratio increases on condition that \( U_i < 16.7V \), remains unchanged at 0.5 on condition that \( 16.7V < U_i < 54V \), and decreases on condition that \( U_i > 54V \). The ratio under IMOPS is always higher than that under IM. If \( U_i < 16.7V \) or \( U_i > 54V \), the same ratio is shared by IMOPS and IMDO. And in other cases, IMOPS makes the ratio higher. This conclusion indicates less power losses and higher conversion efficiency under IMOPS in contrast with IMDO when \( U_i \) varies from \( U_{th1} \) to \( U_{th2} \).

**B. AVERAGE AND RIPPLE CURRENTS OF INDUCTOR**

Under CC, inductor average and ripple currents in DSBBC can be formulated as

\[ \Delta I_L = \begin{cases} (U_i - U_o)U_o/(L_f S U_i), & \text{buck mode} \\ (U_o - U_i)U_i/(L_f S U_o), & \text{boost mode} \end{cases} \quad (36) \]

\[ I_L = \begin{cases} U_o/R, & \text{buck mode} \\ U_o^2/(U_i R), & \text{boost mode} \end{cases} \quad (37) \]

When converter works under SM, \( I_L \) and \( \Delta I_L \) are

\[ I_L = (U_o + U_i)U_o/(U_i R) \quad (38) \]

\[ \Delta I_L = U_i U_o/M \quad (39) \]

where \( M = (U_i + U_o) L_f S \).

If IM method is applied in DSBBC, \( I_L \) is the same as that under SM. In the meantime, its ripple is expressed by

\[ \Delta I_L = \begin{cases} (U_i - U_o)U_o/M, & U_i > U_o \\ (U_o - U_i)U_i/M, & U_i < U_o \end{cases} \quad (40) \]

With IMDO employed, \( I_L \) is calculated by (9) and \( \Delta I_L \) is

\[ \Delta I_L = \begin{cases} (1 + 2c)(U_i - U_o)U_o/M, & d + c < 0.5, \quad d < 0.5 \\ [(1 + 4c)U_i - U_o]U_o/(2M), & d > 0.5, \quad d < 0.5 \\ (1 + 2c)U_o - U_i U_i/(2M), & d < 0.5, \quad d > 0.5 \end{cases} \quad (41) \]

With regard to the proposed IMOPS, \( I_L \) is exactly as that under IMDO. What’s more, \( \Delta I_L \) is divided into two cases according to \( U_i \) and \( U_o \), which is assigned by

\[ \Delta I_L = \begin{cases} (1 + 2c)(U_i - U_o)U_o/M, & U_i > U_o \\ (1 + 2c)(U_o - U_i)U_i/M, & U_i < U_o \end{cases} \quad (42) \]

In Fig. 13, \( U_o \) is maintained at 30V. When \( U_i \) goes up, \( I_L \) drops under CC (boost) and it keeps constant under CC (buck). What’s more, inductor average current under IMDO and IMOPS declines continuously, which is always lower than that under SM and IM.

In Fig. 14, curves of \( I_L \) versus \( P_L \) under different modulation schemes are plotted when \( U_o \) is fixed at 30V. Input voltage is 60V and 15V in Fig. 14 (a) and (b) respectively. By comparison, \( I_L \) under IMDO and IMOPS is obviously lower than that under SM and IM whether \( U_i < U_o \) or \( U_i > U_o \). In fact, the average current under SM and IM is \((1 + 2c)\) times of that under IMDO and IMOPS, which is deduced from (9) and (38). And \( I_L \) under IMDO and IMOPS is slightly higher than that under CC.

In Fig. 15, curves of \( \Delta I_L \) versus \( U_i \) under different modulation schemes are depicted when \( U_o \) keeps unchanged. With the same \( L \), the inductor ripple current under SM is highest while that under IM is lowest. The \( \Delta I_L \) under IMDO, IMOPS or CC lies between the two limitations respectively. In the case of (25) and (29), \( \Delta I_L \) is reduced under IMOPS compared to IMDO. In else case, \( \Delta I_L \) under IMOPS is the same as that under IMDO. Particularly when \( U_o \) is equal to \( U_i \), the \( \Delta I_L \) under IMOPS, IM or CC could reach zero in theory.

**IV. EXPERIMENTAL VERIFICATIONS AND ANALYSIS**

**A. EXPERIMENTAL SETUP AND PREPARATIONS**

With TMS320F28335 as core chip, a 150W prototype is built to demonstrate the validity of the proposed modulation
scheme. Photograph of the dc/dc converter is shown in Fig. 16 and main parameters are listed in Table 3.

Two MOSFETs constitute a half bridge. One switch works in PWM style while the other is always turned off. And inductor is connected with midpoints of two bridge arms. In addition, a 3kW dc power supply functions as the input source of converter while a variable resistor (5.7 to 40Ω) performs as the load. Current sensor LA50P is used for inductor current sampling while voltage sensor CHV600VD is employed to measure output voltage.

First of all, DSBBC is made to operate as conventional buck converter and boost converter separately. According to the above-mentioned definitions and testing rule, $D_{\text{min}}$ and $D_{\text{max}}$ are found out to be 0.02 and 0.98 respectively. And $c$ is chosen as 0.2 according to (3) subsequently. Note that the lowest input voltage in practice is set at 15V, rather than 12V in Fig. 12 and Fig. 13. Because 12V is the lowest input voltage in ideal conditions that $d_1 = 1$ and on-state voltage drops are ignored. Then, 60V, 45V, 25V and 15V are selected as input voltage one by one, which are corresponding to operating point in Region A, B, C and D with output voltage fixed at 30V.

### B. STEADY TESTS

In the steady tests, switching frequency is fixed at 2kHz. With different input voltage, Fig. 17, Fig. 18, Fig. 19, and Fig. 20 show the inductor ripple currents under five modulation schemes. Waveforms from top to bottom are $S_1$ driving signal $u_{\text{GS}1}$ (20V/div), $S_2$ driving signal $u_{\text{GS}2}$ (20V/div), $i_L$ (1A/div) and $u_L$ (50V/div) respectively with common horizontal scale 250μs/div. And crucial values are summarized in Table 4.

### FIGURE 14. Curves of $i_L$ versus $P_L$ under different modulation schemes. (a) $U_i > U_o$, (b) $U_i < U_o$.

### FIGURE 15. Curves of $\Delta I_L$ versus $U_i$ under different modulation schemes.

According to the experimental waveforms, peak-peak value of $i_L$ under SM is always the highest while that under IM keeps the lowest. When $U_i$ is 60V and 15V, inductor ripple current under IMOPS is equal to that under IMDO while $\Delta I_L$ under IMOPS is obviously reduced compared to IMDO when input voltage is 45V and 25V. In addition, $\Delta I_L$ under CC is always between the highest and lowest ones. These results match well with Fig. 15.

As for inductor average current, CC makes it lowest compared with the other schemes. In fact, $I_L$ under IMOPS is
FIGURE 17. Inductor ripple current when $U_i = 60V$. (a) CC, (b) SM, (c) IM, (d) IMDO, (e) IMOPS.

FIGURE 18. Inductor ripple current when $U_i = 45V$. (a) CC, (b) SM, (c) IM, (d) IMDO, (e) IMOPS.

identical to that under IMDO. And the same case exists between SM and IM. Therefore, taking CC, IM and IMOPS for comparison is enough. With output current $I_o$ fixed at 4.53A, Table 5 presents $I_L$ under CC, IM and IMOPS when input voltage varies from 60V to 15V. It could be analyzed that $I_L$ rises when $U_i$ falls because duty cycles of both switches become larger. On the same condition, inductor average current under IMOPS declines much in comparison with IM thanks to a smaller $d_2$. Besides, IMOPS has increasingly obvious superiority in terms of $I_L$ when $U_i$ decreases. This feature agrees with experimental results in [23].

To confirm the influence of modulation schemes on losses, efficiency curves under CC, SM, IM, IMDO and IMOPS are depicted in Fig. 21 respectively, where load power $P_L$...
 varies from 21W to 156W. It reveals that when input voltage is 60V and 15V, the efficiency under IMDO and IMOPS almost agrees with each other as a result of the same $I_L$ and $\Delta I_L$. And when input voltage is 45V and 25V, the efficiency under IMOPS is further enhanced due to reduced $\Delta I_L$. Thus, the gap of efficiency between CC and IMOPS is narrowed compared with that between CC and IMDO.

In addition, IMOPS makes DSBBC much more efficient than SM and IM in the whole range of input voltage and load power generally. And the advantage on efficiency becomes more prominent with heavier load and lower input voltage. It is because the deviation on inductor average current is much larger in that case, and loss gap is further amplified.
C. TRANSIENT TESTS

In the transient tests, dual-loop control is adopted to achieve mode transition under five modulation schemes. To obtain better transient performance, switching frequency is fixed at 30kHz and it keeps unchanged during the whole process.

Proportional-integral (PI) controllers are utilized for both inner current loop and outer voltage loop. Here, \( k_{pi} \) and \( k_{ii} \) represent proportional and integral parameters of current controller while \( k_{pv} \) and \( k_{iv} \) are proportional and integral parameters of voltage controller respectively.

In practical DSP program, the value of period register is 2500 and time-base counter works in count-up mode. On account of duty offset and effective duty cycles, the maximum of \( d \) is set as 4950 for CC. To realize the effective control, it is 2450 for SM and IM while it is 1950 for IMDO and IMOPS. Under CC, \( k_{pi} \) and \( k_{ii} \) are 200 and 16.7 while \( k_{pv} \) and \( k_{iv} \) are 0.6 and 0.0004. Under SM and IM, \( k_{pi} \) and \( k_{ii} \) are 153 and 3.6 while \( k_{pv} \) and \( k_{iv} \) are 1.5 and 0.003. Under IMDO and IMOPS, \( k_{pi} \) and \( k_{ii} \) are 165 and 6.2 while \( k_{pv} \) and \( k_{iv} \) are 0.85 and 0.015.

Fig. 22 shows the transition from buck to boost mode while Fig. 23 shows the process from boost to buck mode. Waveforms from top to bottom are instantaneous input voltage \( u_i \) (40V/div), instantaneous output voltage \( u_o \) (40V/div), and \( u_{GS1} \) and \( u_{GS2} \) for different control modes.
Under CC, limitations of effective duty cycles cause discontinuity of voltage gain near one. Due to that, obvious ripples of output voltage exist during mode transition. For smooth transition, additional transition strategy or compensation technique is essential to eliminate the negative effects.

In this respect, the other four schemes are advantageous because both switches are working in PWM style and the two duty cycles are always between $D_{\text{min}}$ and $D_{\text{max}}$ when $u_i$ approaches $u_o$. Thus, voltage gain is continuous in the neighborhood of one and adverse effects from discontinuous voltage gain are avoided. As a result, output voltage is almost not influenced during mode transition.

### V. CONCLUSION

Based on IMDO, to further decrease inductor ripple current, interleaved modulation with optimized phase shifting (IMOPS) is presented for DSBBC in this paper. On condition that duty offset exists, impacts of phase-shifted angle on inductor ripple current are deeply researched. Then, optimized section for phase-shifted angle at buck and boost mode is confirmed respectively to achieve the lowest ripple current. To facilitate digital implementation, the optimal phase-shifted angle is set at the midpoint of the above section, rather than 180 degrees, because it is independent of control signal and has consistent form whether at buck or boost mode. Compared with CC, obvious ripples of output voltage are avoided during mode transition because both switches under IMOPS are working in PWM style and voltage gain is continuous near one. Compared with IM, remarkable efficiency promotion is achieved under IMOPS owing to reduced inductor average current, let alone SM. Despite identical inductor average current, lower ripple current and higher efficiency are achieved under IMOPS than those under IMDO if conditions related to control signal are satisfied. On the same conditions, steady and transient tests under five modulation schemes are conducted on a 150W prototype respectively. Experimental results validate the correctness and effectiveness of the proposed IMOPS.

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