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Improved \( I_{\text{on}}/I_{\text{off}} \) Current Ratio and Dynamic Resistance of a p-GaN High-Electron-Mobility Transistor Using an \( \text{Al}_{0.5}\text{GaN} \) Etch-Stop Layer

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Abstract: In this study, we investigated enhance mode \( (E) \)-mode \( \) p-GaN/AlGaN/GaN high-electron-mobility transistors (HEMTs) with an \( \text{Al}_{0.5}\text{GaN} \) etch-stop layer. Compared with an AlN etch-stop layer, the \( \text{Al}_{0.5}\text{GaN} \) etch-stop layer not only reduced lattice defects but engendered improved DC performance in the device; this can be attributed to the lattice match between the layer and substrate. The results revealed that the \( \text{Al}_{0.5}\text{GaN} \) etch-stop layer could reduce dislocation by 37.5% and improve device characteristics. Compared with the device with the AlN etch-stop layer, the p-GaN HEMT with the \( \text{Al}_{0.5}\text{GaN} \) etch-stop layer achieved a higher drain current on/off ratio \((2.47 \times 10^7)\), a lower gate leakage current \((1.55 \times 10^{-5} \text{A/mm})\), and a lower on-state resistance \((21.65 \Omega \cdot \text{mm})\); moreover, its dynamic \( \text{R}_{\text{ON}} \) value was reduced to 1.69 (from 2.26).

Keywords: etch-stop layer; high selectivity ratio; normally off; p-GaN gate HEMT

1. Introduction

In recent years, the wide bandgap (WBG) GaN-based high-electron-mobility transistors (HEMTs) have attracted much attention for high-radio-frequency (RF) and high-power semiconductor device applications owing to their excellent performance of high electric field strength \((3.3 \text{MV/cm})\), high mobility \((>1200 \text{ cm}^2/\text{Vs})\), and favorable thermal conductivity \([1–3]\). To get realistic power supply applications, the normally off behavior of GaN-based HEMTs must be implemented. Thus, several methods have attempted to realize the positive threshold voltage \( (V_{\text{TH}}) \) of AlGaN/GaN HEMTs, such as ultrathin barriers, gate-recessed structures, fluorine treatment, and p-type gates \([4–8]\). However, structures involving p-type gates have drawn increasing attention in industry owing to their low on-state resistance and high threshold voltage. The precision and lower damage etching process is a key factor in device fabrication, and outstanding etching depth control is imperative because the residual p-GaN layer in the out-of-gate area makes the 2DEG channel depleted and leads to a low forward current. Moreover, if the p-GaN layer is overetched in to the AlGaN barrier layer and reduces the AlGaN barrier thickness in this process, the channel carrier density is decreased because of the decrease in spontaneous polarization. In tradition structures, an AlN layer is used as an etch-stop layer; however, high-quality thin AlN has difficulty achieving epitaxy control, and problems related to lattice mismatch can arise \([9,10]\). In this study, we applied an \( \text{Al}_{0.5}\text{GaN} \) etch-stop layer...
between p-GaN and AlGaN barriers and compared its performance with that of an AlN etch-stop layer. The experimental results indicated that the dynamic \( R_{ON} \) was improved and that the leakage current was suppressed. Transmission electron microscopy (TEM) images revealed the etch-stop layer to be smooth and highly selective. Therefore, high-performance normally off p-GaN/AlGaN/GaN HEMTs can be realized using an AlGaN etch-stop layer for high-speed and high-power electronic applications.

2. Device Structure

As illustrated in Figure 1a, we present a new p-GaN/AlGaN/GaN HEMT structure with an Al\(_{0.5}\)GaN etching stop design grown through metal organic chemical vapor deposition (MOCVD) on a 6 in silicon (111) wafer. The epistructure was composed, from bottom to top, of a 4 \( \mu \)m-thick C-doped GaN buffer layer, a 300 nm-thick undoped GaN channel layer, a 12 nm-thick undoped Al\(_{0.17}\)GaN barrier layer, a 2 nm Al\(_{0.5}\)GaN etch-stop layer, and a 75 nm-thick p-type GaN top layer whose active Mg concentration was \( 1 \times 10^{18} \) cm\(^{-3} \).

For device fabrication, we used standard photolithography and lift-off technology, the active region was defined by a photoresist and etched to a depth of 200 nm using BCl\(_3\)/Cl\(_2\)/SF\(_6\) gas plasma by reactive ion etching (RIE). A 5 \( \mu \)m-long p-type GaN gate platform was formed through a mixture of BCl\(_3\)/Cl\(_2\)/SF\(_6\) gas plasma 120 s to remove p-GaN by inductively coupled plasma (ICP). The F radicals from the SF\(_6\) plasma and Al atoms from the Al\(_{0.5}\)GaN barrier layer created a fluorination reaction and formed a thin aluminum fluoride (AlF\(_3\)) etch-stop layer [11]. The resulting etching rate was 0.625 nm/s. Moreover, the Al\(_{0.5}\)GaN layer was etched at an etching rate of <0.016 nm/s, implying a high-selectivity etching process in the p-GaN/Al\(_{0.5}\)GaN layer. Subsequently, the formed AlF\(_3\) can be removed by diluted HF/\( \text{NH}_4\)OH chemical solution [12]. As indicated in Figure 1b the p-GaN removal depth was measured using an atomic force microscope (AFM) and the inset of that figure presents a TEM image after etching (inset).
3. Experimental Results and Discussion

X-ray diffraction (XRD) was used to investigate the dislocation density, and the results are presented in Figure 2. The full width at half-maximum (FWHM) values of the (002) symmetric and (102) asymmetric reflection were used to measure crystal quality. In our device surface measurements, we mainly investigated the crystal quality on the device surface. The FWHM values for the (002) and (102) planes of the AlN and AlGaN etch-stop layer designs were 164/239 and 162/179 arcsec, respectively. In general, the rocking curve scan of a (002) reflection provides information on the degree of tilt with respect to the surface of a device, and the FWHM of this reflection is a qualitative measure of screw dislocation density \( N_{\text{screw}} \) [13,14]. The rocking curve scan of a (102) reflection provides information on the degree of twist with respect to the surface of a device, and the FWHM of this reflection is a measure of edge dislocation density \( N_{\text{edge}} \). The dislocation density can be calculated using XRD-derived FWHM results as follows:

\[
N_{\text{screw}} = \frac{\text{FWHM}_{002}^2}{4.35 \times b_{\text{screw}}^2}, N_{\text{edge}} = \frac{\text{FWHM}_{102}^2}{4.35 \times b_{\text{edge}}^2},
\]

\( N_{\text{total}} = N_{\text{screw}} + N_{\text{edge}} \)  

where \( N_{\text{screw}} \) and \( N_{\text{edge}} \) are the screw and edge dislocation densities, respectively, and \( b \) is Burger’s vector. In this study, these equations were used for calculation, and the results revealed that the total dislocation \( N_{\text{total}} \) values of the Al\(_{0.5}\)GaN etch-stop layer and AlN etch-stop layer were \( 2.23 \times 10^8 / \text{cm}^2 \) and \( 3.57 \times 10^8 / \text{cm}^2 \), respectively. As indicated in Figure 2, the screw dislocation density and edge dislocation density were lower when the Al\(_{0.5}\)GaN etch-stop layer was used than when the AlN etch-stop layer was used.
We observed that threshold voltage \( (kT/q) \) where the AlN and Al\(_{0.5}\)GaN etch-stop layers were 103.5 and 99.2 mV/dec, respectively. The subthreshold swing \( (S_{SS}) \) for the AlN stop layer and Al\(_{0.5}\)GaN stop layer was measured to be 222 nF/cm\(^2\) under a frequency of 1M Hz. Therefore, the interface charge densities \( (D_{it}) \) can be calculated and the \( (D_{it}) \) values of the AlN stop layer and Al\(_{0.5}\)GaN stop layer device were \( 1.02 \times 10^{12} \) and \( 7.64 \times 10^{11} \) cm\(^{-2}\) eV\(^{-1}\), respectively. This indicated the device with the Al\(_{0.5}\)GaN stop layer had better defect density suppression. The Al\(_{0.5}\)GaN stop layer design was determined to be suitable for device switching owing to its favorable \( I_{on}/I_{off} \) ratio and gate drive-control capability. Figure 3b illustrates the \( I_{DS}–V_{DS} \) curves as functions of the gate-to-source voltage \( (V_{GS}) \) bias ranging from 0 to 4 V in steps of 1 V and of the current values of the devices with the AlN and Al\(_{0.5}\)GaN etch-stop layers were 67 and 121 mA/mm, respectively. At a gate bias of 4 V, the maximum output current density \( (I_{D_{max}}) \) for the AlN stop layer and Al\(_{0.5}\)GaN stop layer was 222 nF/cm\(^2\) and 0.23 V, respectively. At a gate bias of 4 V, the maximum output current density \( (I_{D_{max}}) \) for the AlN stop layer and Al\(_{0.5}\)GaN stop layer was 0.37 and 0.23 V, respectively. At a gate bias of 4 V, the maximum output current density \( (I_{D_{max}}) \) for the AlN stop layer and Al\(_{0.5}\)GaN stop layer was 4.31 \( \times 10^{-5} \) and 4.11 \( \times 10^{-6} \) mA/mm, respectively. The device with the Al\(_{0.5}\)GaN etch-stop layer had a superior \( I_{on}/I_{off} \) ratio to the device with the AlN etch-stop layer, which increased from 1.41 \( \times 10^{-5} \) to 2.47 \( \times 10^{-7} \). Moreover, the subthreshold swing (S.S.) values of the devices with the AlN and Al\(_{0.5}\)GaN etch-stop layers were 103.5 and 99.2 mV/dec, respectively. The subthreshold swing (S.S.) is expressed by the analytical equation given below [15]

\[
S.S. = (\ln 10) \left( \frac{kT}{q} \right) \left( 1 + \frac{C_d + C_{it}}{C_{ox}} \right)
\]

(3)

where \( kT/q \) is the thermal voltage, \( C_{ax} \) is the capacitance of the gate dielectric, \( C_d \) the depletion capacitance, \( C_{it} \) is the capacitance of gate and semiconductor interface state, \( D_d \) is interface charge densities, and \( q \) is the electronic charge. The capacitance of the gate dielectric \( (C_{ax}) \) for the AlN stop layer and Al\(_{0.5}\)GaN stop layer was measured to be 222 nF/cm\(^2\) and 184 nF/cm\(^2\) under a frequency of 1M Hz. Therefore, the interface charge densities \( (D_{it}) \) can be calculated and the \( (D_{it}) \) values of the AlN stop layer and Al\(_{0.5}\)GaN stop layer device were \( 1.02 \times 10^{12} \) and \( 7.64 \times 10^{11} \) cm\(^{-2}\) eV\(^{-1}\), respectively. This indicated the device with the Al\(_{0.5}\)GaN stop layer had better defect density suppression. The Al\(_{0.5}\)GaN stop layer design was determined to be suitable for device switching owing to its favorable \( I_{on}/I_{off} \) ratio and gate drive-control capability. Figure 3b illustrates the \( I_{DS}–V_{DS} \) curves as functions of the gate-to-source voltage \( (V_{GS}) \) bias ranging from 0 to 4 V in steps of 1 V and of the...
functions of the gate-to-source voltage \((V_{GS})\) bias ranging from 0 to 4 V in steps of 1 V and of the drain-to-source voltage \((V_{DS})\) sweep ranging from 0 to 10 V. The ON-resistance \((R_{ON})\) could be reduced from 28.03 to 21.65 Ω mm owing to the lower dislocation trap density and the suppressed trap density effect in the channel.

![Graph](image1.png)

**Figure 3.** I–V characteristic comparison of both devices (device dimension: \(L_{GS}/L_{G}/L_{GD}/W_{G} = 2 \mu m/2 \mu m/5 \mu m/100 \mu m\)). (a) Transfer characteristics and (b) output characteristics.

The gate leakage curve presented in Figure 4a was used to investigate the leakage current mechanism. The device with the Al\(_{0.5}\)GaN etch-stop layer exhibited a lower gate leakage current than did the other device. This low gate leakage current not only increased the device breakdown voltage but also improved the gate operator voltage. The off-state breakdown voltage \((V_{BR})\) was measured using an Agilent B1505 analyzer; the \(V_{GS}\) was 1V and the drain leakage current reached 1 mA/mm. As displayed in Figure 4b, the \(V_{BR}\) values of the devices with the AlN and Al\(_{0.5}\)GaN etch-stop layers were 501 and 561 V, respectively. Moreover, Baliga’s figure of merit \((BFOM = V_{BR}^2/R_{DS.on})\) for various power transistors was calculated to evaluate the overall performance of these devices [16,17]. The \(BFOM\) values of the devices with the AlN and Al\(_{0.5}\)GaN etch-stop layers were 44.37 and 83.11 MW/cm\(^2\), respectively.

![Graph](image2.png)

**Figure 4.** (a) Gate leakage characteristics and (b) off-state breakdown voltage measurement of both devices.
The Maury AMCAD pulse IV system was used to further investigate trapping/detrapping phenomena and the dynamic behavior of the devices [18,19]. Furthermore, the $I_{DS}-V_{DS}$ characteristics were also measured from different quiescent bias points at $V_{GS} = 4$ V to investigate the influence of off-state gate bias stress on dynamic $R_{ON}$ and $I_{DS}$, as illustrated in Figure 5. The reference off-state was set to $(V_{GSO}, V_{DSO}) = (0$ V, $0$ V); this setting did not induce any relevant trapping. The device was switched with a 2 μs pulse width and 200 μs period. The quiescent gate bias ($V_{GSO}$) was swept from 0 to $-3$ V. The current collapse in the device with the AlN etch-stop layer was worse than that in the device with the Al$_{0.5}$GaN etch-stop layer, and the high gate lag of the device with the AlN layer under gate voltage stress resulted in a decrease in the $I-V$ slope, indicating that the surface defect trap density of this device was higher than that of the device with the Al$_{0.5}$GaN etch-stop layer. The dynamic $R_{ON}$ ($R_{ON}/R_{ON(0,0)}$) of the device with the Al$_{0.5}$GaN etch-stop layer slightly increased with the gate bias stress from 0 to $-3$ V because of the low electron injection into the surface trap states from the gate electrode [20]. The dynamic $R_{ON}$ ratio increased to 2.26 and the dynamic drain current decreased to 41.4% when the off-state gate bias stress was $-3$ V for the device with the AlN etch-stop layer.

![Image](image_url)

Figure 5. (a) Pulsed $I_{DS}-V_{DS}$ characteristics after quiescent gate bias ($V_{GSO}$) stress and (b) dependence of the $R_{ON}$ collapse ratio and $I_{DS}$ decay versus various quiescent gate voltages of both devices.

4. Conclusions

In this study, a highly selective Al$_{0.5}$GaN etch-stop layer was applied to a p-GaN/AlGaN/GaN HEMT. Compared with the traditional AlN etch-stop layer structure, the Al$_{0.5}$GaN etch-stop layer had a lower dislocation density, according to our XRD results; dynamic $R_{ON}$ and dynamic $I_{DS}$ were significantly lower in the device with the Al$_{0.5}$GaN etch-stop layer. Furthermore, the device with the Al$_{0.5}$GaN etch-stop layer had superior DC characteristics to the other device, including a lower off-state current, lower gate leakage, lower on-resistance, higher on/off ratio, good subthreshold swing, and higher off-state breakdown voltage. A BFOM assessment revealed that applying an Al$_{0.5}$GaN etch-stop layer is a promising method for fabricating high-performance normally off p-GaN HEMTs.

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References

1. Saito, W.; Takada, Y.; Kuraguchi, M.; Tsuda, K.; Ogura, I.; Ohashi, H. High breakdown voltage AlGaN-GaN power-HEMT design and high current density switching behavior. IEEE Trans. Electron Devices 2003, 50, 2528–2531. [CrossRef]

2. Nirmal, D.; Aravizhagan, L.; Fletcher, A.; Ajayan, J.; Prajoo, P. Current collapse modeling in AlGaN/GaN HEMT using small signal equivalent circuit for high power application. Superlattices Microstruct. 2018, 113, 810–820. [CrossRef]

3. Matys, M.; Ishida, T.; Nam, K.P.; Sakurai, H.; Narita, T.; Uesugi, T.; Bockowski, M.; Suda, J.; Kachi, T. Mg-implanted bevel edge termination structure for GaN power device applications. Appl. Phys. Lett. 2021, 118, 093502. [CrossRef]

4. Ohmaki, Y.; Tanimoto, M.; Akamatsu, S.; Mukai, T. Enhancement-Mode AlGaN/AlN/GaN High Electron Mobility Transistor with Low On-State Resistance and High Breakdown Voltage. Jpn. J. Appl. Phys. 2006, 45, L1168–L1170. [CrossRef]

5. Oka, T.; Nozawa, T. AlGaN/GaN Recessed MIS-Gate HFET With High-Threshold-Voltage Normally-Off Operation for Power Electronics Applications. IEEE Electron Device Lett. 2008, 29, 668–670. [CrossRef]

6. Kim, K.W.; Jung, S.D.; Kim, D.S.; Kang, H.S.; Im, K.S.; Oh, J.J.; Ha, J.B.; Shin, J.K.; Lee, J.H. Effects of TMAH treatment on device performance of normally off Al2O3/GaN MOSFET. IEEE Electron. Device Lett. 2011, 32, 1376–1378. [CrossRef]

7. Chen, W.; Wong, K.Y.; Chen, K.J. Monolithic integration of lateral field-effect rectifier with normally-off HEMT for GaN-on-Si switch-mode power supply converters. In Proceedings of the 2008 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2008; pp. 1–4.

8. Cai, Y.; Zhou, Y.; Chen, K.J.; Lau, K.M. High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment. IEEE Electron Device Lett. 2005, 26, 435–437. [CrossRef]

9. Tian, W.; Yan, W.Y.; Dai, J.N.; Li, S.L.; Tian, Y.; Hui, X.; Zhang, J.B.; Fang, Y.Y.; Wu, Z.H.; Chen, C.Q. Effect of growth temperature of an AlN intermediate layer on the growth mode of AlN grown by MOCVD. J. Phys. D Appl. Phys. 2013, 46, 65303. [CrossRef]

10. Demir, I.; Li, H.; Robin, Y.; McClintock, R.; Elagoz, S.; Razeghi, M. Sandwich method to grow high quality AlN by MOCVD. J. Phys. D Appl. Phys. 2018, 51, 085104. [CrossRef]

11. Buttari, D.; Chini, A.; Chakraborthy, A.; McCarthy, L.; Xing, H.; Palacios, T.; Shen, L.; Keller, S.; Mishra, U.K. Selective dry etching of GaN over AlGaN in BC13/SF6 mixtures. Int. J. High Speed Electron. Syst. 2004, 14, 756–761. [CrossRef]

12. Yu, C.J.; Hsu, C.W.; Wu, M.C.; Hsu, W.C.; Chuang, C.Y.; Liu, J.Z. Improved DC and RF Performance of Novel MIS p-GaN-Gated HEMTs by Gate-All-Around Structure. IEEE Electron Device Lett. 2020, 41, 673–676. [CrossRef]

13. Lee, H.-P.; Perozek, J.; Rosario, L.D.; Bayram, C. Investigation of AlGaN/GaN high electron mobility transistor structures on 200-mm silicon (111) substrates employing different buffer layer configurations. Sci. Rep. 2016, 6, 37588. [CrossRef] [PubMed]

14. Booker, I.; Khoshroo, L.R.; Woitok, J.F.; Kaganer, V.; Mauder, C.; Behmenburg, H.; Gruis, J.; Heuken, M.; Kalisch, H.; Jansen, R.H. Dislocation density assessment via X-ray GaN rocking curve scans. Phys. Status Solidi 2010, 7, 1787–1789. [CrossRef]

15. Maity, N.; Thakur, R.; Maity, R.; Thapa, R.; Baishya, S. Analysis of Interface Charge Using Capacitance-Voltage Method for Ultra Thin HfO2 Gate Dielectric Based MOS Devices. Procedia Comput. Sci. 2015, 57, 757–760. [CrossRef]

16. Shen, L.; Muller, S.; Cheng, X.; Zhang, D.; Zheng, L.; Xu, D.; Yu, Y.; Meissner, E.; Erlbacher, T. The GaN trench gate MOSFET with floating islands: High breakdown voltage and improved BFO. Superlattices Microstruct. 2018, 114, 200–206. [CrossRef]

17. Sun, W.; Joh, J.; Krishnan, S.; Pendharkar, S.; Jackson, C.M.; Ringel, S.A.; Arehart, A.R. Investigation of Trap-Induced Threshold Voltage Instability in GaN-on-Si MISHEMTs. IEEE Electron Device Lett. 2019, 66, 890–895. [CrossRef]

18. Liu, C.H.; Chiu, H.C.; Huang, C.R.; Chang, K.J.; Chen, C.T.; Hsueh, K.P. Low Gate Lag Normally-off p-GaN/AlGaN/GaN High Electron Mobility Transistor with Zirconium Gate Metal. Crystals 2020, 10, 25. [CrossRef]

19. Tirado, J.M.; Sanchez-Rojas, J.L.; Izpura, J.I. Trapping Effects in the Transient Response of AlGaN/GaN HEMT Devices. IEEE Trans. Electron Devices 2007, 54, 410–417. [CrossRef]

20. Chiu, H.C.; Chang, Y.S.; Li, B.H.; Wang, H.C.; Kao, H.L.; Chien, F.T.; Hu, C.W.; Xuan, R. High Uniformity Normally-OFF p-GaN Gate HEMT Using Self-Terminated Digital Etching Technique. IEEE Trans. Electron Devices 2018, 65, 4820–4825. [CrossRef]