Modelling and Failure Analysis of SiC MOSFET under the Effects of Parasitic Parameters

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Abstract. Recent years, SiC MOSFET has been gradually utilized in high power devices. However, it has become one of the highest failure rate devices in circuit systems. Its failure relates to the degradation which caused by the hot carrier injection (HCI) effect. Because the parasitic parameters make the oscillations in switching processes more intense, the switching time and voltage overshoot increases, and thus HCI effect exacerbates. So, it is necessary to analyse the influence of parasitic parameters on the failure of SiC MOSFET. In this paper, an improved SiC MOSFET model with all key parasitic parameters is built to set up an accurate test circuit. The parasitic parameters were divided into four parts: body diode, parasitic resistance, parasitic capacitance and parasitic inductance. According to the simulation, it concluded that only the parasitic inductance has a great impact on the HCI effect and the impacts are different according to the different locations of parasitic inductance. The influence of the parasitic inductance on the load circuit and near the source is much greater than other parts. Their increase greatly increases switching time and voltage overshoot, and thus exacerbates HCI effect and accelerates the degradation of SiC MOSFET.

1. Introduction
Recent years, SiC MOSFET has been gradually utilized in high power devices. Compared to Si MOSFET, SiC MOSFET has wider band gap, lower ON-state resistance ($R_{ds(on)}$), higher breakdown voltage and more excellent switching performance [1]. Such advantages enable SiC MOSFET to be an important candidate for high voltage, high switching frequency and high energy density area [2]. But it also has become one of the highest failure rate devices in circuit systems. The failure of SiC MOSFET does not only refer to the failure of the base, but also relate to the degradation of the electrical characteristics which makes the devices' performance worse. Research shows that 81.8% of failures are due to use failures, and 72.7% of them are due to degradation failure caused by electrical stress [3].

High electrical stress is common for SiC MOSFET used in extreme electrical areas. It is related to the voltage overshoot and switching time, which caused by oscillations during the switching processes. And the impacts of parasitic parameters make the oscillations more intense and the electrical stress higher. Excessive electrical stress accelerates the degradation through failure mechanisms such as hot carrier injection (HCI) effect [4]. Therefore, the parasitic parameters affect the failure of SiC MOSFET by changing the electrical stress. For further analysing the influence, an accurate model of SiC MOSFET and a test circuit are necessary to be set up with all key parasitic parameters. Then
according to the simulation results, the effects of parasitic parameters on the failure of SiC MOSFET can be concluded.

2. The hot carrier injection effect
The HCI effect is one of the most important failure mechanisms about SiC MOSFET. And it is also one of the most relative failure mechanisms to electrical stress [5]. It degrades many electrical characteristics of SiC MOSFET, such as threshold voltage ($V_{th}$), saturation current ($I_{ds}$) and linear current.

Under the action of the drain-source voltage ($V_{ds}$), the lateral field strength of the channel region increases significantly, which causes the average kinetic energy of the carriers to increase significantly and the energy to exceed the kinetic energy of the lattice thermal equilibrium state. Such carriers with increased kinetic energy are called hot carriers. Under the modulation of the gate-source voltage ($V_{gs}$), the hot carriers have a chance to move toward the gate, break the Si-H bond at the SiO$_2$ interface to form an interface state, and implant into the oxide layer to generate defects. These interface states and defects lead to degradation of electrical characteristics.

SHAN Wenguang [6] et al. conducted an research on the HCI effect of NMOS under practical application condition. The results show that under the condition of high $V_{ds}$ and low $V_{gs}$, drain-source current ($I_{ds}$) increases with the increase of electrical stress. This is because under such stress condition, a lateral electric field from the drain to the gate is generated near the drain, causing holes to be injected into the gate, and a positively charged defect is formed in the gate oxide layer near the drain. When a reverse voltage is applied to the gate, the $I_{ds}$ cannot be recovered. So, once there is an voltage oscillation, the voltage overshoot increases the electric field strength sharply and aggravate the effect of HCI. According to the test, $V_{ds}$ rose to more than twice the load voltage in the process of turn-off the resistive load. And depending on the type of load, the voltage overshoot can be higher. It undoubtedly exacerbated the HCI effect.

In addition, according to the research of Song Z [7], the HCI effect of NMOS under the worst stress conditions is greatly intensified. The worst-case stress conditions vary depending on the channel length. The device involved in this paper has a long channel length. Therefore, 175 °C, $V_{ds}$-$V_{gs}$ can be considered as the worst stress condition. According to the test, it found that $V_{ds}$ dropped to $V_{gs}$ during the oscillation. And long switching time often leads to a long duration of $V_{ds}$-$V_{gs}$. In addition, while working normally, the device emits a large amount of heat. It increases the temperature and makes the condition worse. So the longer the oscillation time is, the worse the stress condition is. As a result, the HCI effect is exacerbated, and many electrical characteristics of SiC MOSFET are degraded.

Therefore, switching time and voltage overshoot are selected as the dependent variables to determine the severity of the HCI effect. Without considering other failure mechanisms, its severity can directly reflect the speed of degradation.

3. SiC MOSFET model with parasitic parameters
For setting up the test circuit, an accurate SiC MOSFET model needed to be built. A TO-247 package, 900V, 36A Cree SiC MOSFET was utilized. Although Cree provided an official SPICE model, this study was based on Saber and the official SPICE model cannot be used. So a new model needed to be built in Saber. Generally, a SiC MOSFET model is constituted by three parts: ideal switch and internal resistance, internal capacitance, body diode. It is shown in figure 1. Modeling was achieved by establishing parameter equations in Saber Model Architect. There were two main methods for obtaining parameters: Using the tables and curves already given in datasheet to calculate the required parameters through classic MOSFET formulas and measuring the official spice model and actual device to obtain the required parameters.
After completing the SiC MOSFET model, the model’s accuracy needed to be verified. Two same double impulse response circuits were built in Saber and LTspice, as shown in figure 2.

The waveforms of $I_L$ and $V_{ds}$ are shown in figure 3. It can be seen that their switching time and Miller platform height are basically equal. It means that the SiC MOSFET model built in Saber was accurate enough.

The traditional SiC MOSFET model does not consider the parasitic parameters, so it makes the simulation results not in line with reality. Because this study needed to analyse the influence of parasitic parameters, an improved SiC MOSFET model considering the parasitic parameters was built. A PCB was designed to verify the model’s accuracy. Then the parasitic parameters of PCB were extracted by ANSYS Q3D Extractor. The PCB 3D model is shown in figure 4. In order to increase
efficiency, the model needed to be simplified by ignoring the copper far from the three terminals of the SiC MOSFET.

**Figure 4.** The PCB 3D model.

After defining the material and current sources, the PCB model was solved to obtain the parasitic parameters. As the parasitic capacitance and resistance were much less than internal capacitance and source internal resistance, only the parasitic inductance needed to be considered in modeling. The inductance matrix is shown in table 1.

**Table 1.** The inductance matrix.

|      | Load_A | Load_B | Load_C | Load_D | Gate |
|------|--------|--------|--------|--------|------|
| Load_A | 14.36  | -0.29  | -2.82  | -0.46  | -    |
| Load_B | -0.29  | 8.639  | 0.044  | -2.95  | -    |
| Load_C | -2.82  | 0.044  | 5.673  | 0.142  | -    |
| Load_D | -2.95  | 0.37503| 0.142  | 28.29  | -    |
| Gate   | -      | -      | -      | -      | 7.632|

Unit: nH

To simplify calculations, only self-inductance was considered. Then, it was required to estimate the parasitic inductance introduced by the SiC MOSFET package. According to the engineering experience, the parasitic inductance which TO-247 package brought to each terminal was about 30nH. The test circuit with the improved SiC MOSFET model is shown in figure 5.

**Figure 5.** The test circuit with the improved SiC MOSFET model.
The equivalent parasitic inductances of the PCB to the gate, source, and drain of SiC MOSFET are 7.54nH, 20.3nH, and 20.6nH respectively. And the parasitic inductance brought by the package is 30nH at each terminal. \( V_{ds} \) was selected as reference for the switching characteristics. The comparison between the simulation and practice waveform is shown in figure 6. It found that the drain-source voltage waveforms are basically consistent. In other words, the switching characteristics of the improved model are similar to those of actual SiC MOSFET device.

![Figure 6. \( V_{ds} \) turn-off voltage(a) and \( V_{ds} \) turn-on voltage(b) waveforms.](image)

4. Parasitic Parameter’s Effect on Failure
Without considering other failure mechanisms, the severity of the HCI effect can directly reflect the speed of device degradation. Based on previous analysis, the switching time and voltage overshoot during oscillation can affect HCI effect. So for the SiC MOSFET failure analysis under the effect of parasitic parameters, they were mainly considered.

For the definition of switching time, 5% and 95% of stable maximum were used as the judgment criteria. Once the voltage downs to 5%, it is regarded as on. Similarly, once it rises to 95% it is regarded as off. The time between on and off is switching time. The voltage overshoot is the maximum voltage value during the oscillation. The parasitic parameters were divided into four parts: the body diode, parasitic capacitance, parasitic resistance and parasitic inductance.

4.1 Body Diode and Parasitic Resistance
Based on the test circuit, the SiC MOSFET was shorted by a reverse ideal diode. It found that the switching time and voltage overshoot were unchanged. So, whether the body diode is shorted can have negligible effect on HCI effect.

The parasitic resistance extracted from the PCB and SiC MOSFET was equivalent to 10\( \text{m}\Omega \) on each terminal. The source internal resistance was much larger than the parasitic resistance of the gate. The resistance load was also much larger than the parasitic resistance of the drain and source. So, the parasitic resistance also had negligible effect on HCI effect.

4.2 Parasitic Capacitance
According to the datasheet, the parasitic capacitance in SiC MOSFET is divided into three parts: \( C_{iss} \), \( C_{oss} \), \( C_{rss} \). They vary by \( V_{ds} \), but become fixed when \( V_{ds} \) is fixed. In this condition, \( V_{ds} \) was 12V, thus, the values of \( C_{iss} \), \( C_{oss} \), \( C_{rss} \) were 700pF, 470pF, 30pF respectively. The equivalent parasitic capacitance in PCB was about 0.17 pF to each terminal, which was much smaller than the parasitic capacitance in SiC MOSFET. So, the effect of parasitic capacitance in PCB can be ignored. The parasitic capacitance in SiC MOSFET was unchanged, so there was no need to consider its influence on HCI effect.
4.3 Parasitic Inductance

Parasitic inductance was divided into SiC MOSFET package parasitic inductance and PCB parasitic inductance. Based on the test circuit shown in figure 5, the influence of parasitic inductance was further discussed. By changing the value of each inductor, the switching time and voltage overshoot also changed. Different variable combinations were numbered as shown in table 2. Then the results are shown in table 3.

Table 2. Different Variable Combinations.

| No. | $L_1$(nH) | $L_2$(nH) | $L_3$(nH) | $L_4$(nH) | $L_5$(nH) |
|-----|-----------|-----------|-----------|-----------|-----------|
| 1   | 1         | 1         | 1         | 1         | 1         |
| 2   | 30        | 1         | 1         | 1         | 1         |
| 3   | 60        | 1         | 1         | 1         | 1         |
| 4   | 1         | 30        | 1         | 1         | 1         |
| 5   | 1         | 60        | 1         | 1         | 1         |
| 6   | 1         | 1         | 30        | 1         | 1         |
| 7   | 1         | 1         | 60        | 1         | 1         |
| 8   | 1         | 1         | 1         | 30        | 1         |
| 9   | 1         | 1         | 1         | 60        | 1         |
| 10  | 1         | 1         | 1         | 1         | 30        |
| 11  | 1         | 1         | 1         | 1         | 60        |

Table 3. Oscillation on Different Inductance.

| No. | Oscillation Factors(on) | Oscillation Factors(off) |
|-----|--------------------------|--------------------------|
|     | $\text{Switching time}(\text{ns})$ | $\text{overshoot (V)}$ | $\text{Switching time}(\text{ns})$ | $\text{overshoot (V)}$ |
| 1   | 7.424                    | 13.215                   | 28.405                   | 12.000                   |
| 2   | 8.561                    | 12.443                   | 29.105                   | 12.000                   |
| 3   | 9.442                    | 12.297                   | 28.634                   | 12.000                   |
| 4   | 20.677                   | 17.045                   | 44.881                   | 13.572                   |
| 5   | 32.007                   | 17.324                   | 55.014                   | 14.311                   |
| 6   | 6.785                    | 13.464                   | 35.547                   | 16.999                   |
| 7   | 6.551                    | 13.489                   | 79.660                   | 23.405                   |
| 8   | 8.510                    | 12.383                   | 29.393                   | 12.000                   |
| 9   | 9.724                    | 12.223                   | 29.076                   | 12.000                   |
| 10  | 6.785                    | 13.464                   | 35.547                   | 16.999                   |
| 11  | 6.551                    | 13.489                   | 79.660                   | 23.405                   |

It can be seen that the increase of $L_1$ and $L_4$ slightly increased the turn-on time, and slightly reduced the turn-on voltage overshoot. But they had no effect on the turn-off process. The increase of $L_2$ has a great impact on both the turn-on and turn-off processes. It increased the switching time and voltage overshoot. The increase of $L_3$ and $L_5$ greatly increased the turn-off time and turn-off voltage overshoot. However, they had no effect on the turn-on process.

It can be seen that parasitic inductance was the main factor affecting the oscillation. The parasitic inductance in the load circuit and near the source had much greater influence than other parts. Their increase greatly increased switching time and voltage overshoot, thereby exacerbated HCI and
accelerated the degradation of SiC MOSFET. When designing circuit, it is necessary to pay attention to reduce the parasitic inductance of these two parts. It can slow down the degradation of SiC MOSFET and ensure the reliability of the circuit.

Conclusion
In this paper, we concluded that the parasitic parameters affect HCI and the degradation of SiC MOSFET by affecting switching time and voltage overshoot. Considering the accuracy of simulation, we propose a method to establish a SiC MOSFET model with considering parasitic parameters. It found that the body diode and internal parasitic resistance of SiC MOSFET have little effect on HCI effect. The effects of PCB parasitic capacitance and resistance can also be ignored. However, the parasitic inductance of the PCB and package has a great impact on HCI effect and the impacts are different according to the different locations of parasitic inductance. The influence of the parasitic inductance on the load circuit and near the source is much greater than other parts. Their increase greatly increases switching time and voltage overshoot, and thus exacerbates HCI and accelerates the degradation of SiC MOSFET.

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