Accelerating BLAS on Custom Architecture through Algorithm-Architecture Co-design

Farhad Merchant, Tarun Vatwani, Anupam Chattopadhyay, Senior Member, IEEE, Soumyendu Raha, S K Nandy, Senior Member, IEEE, and Ranjani Narayan

Abstract—Basic Linear Algebra Subprograms (BLAS) play key role in high performance and scientific computing applications. Experimentally, yesteryear multicore and General Purpose Graphics Processing Units (GPGPUs) are capable of achieving up to 15 to 57% of the theoretical peak performance at 65W to 240W respectively for compute bound operations like Double/Single Precision General Matrix Multiplication (XGEMM). For bandwidth bound operations like Single/Double precision Matrix-vector Multiplication (XGEMV) the performance is merely 5 to 7% of the theoretical peak performance in multicores and GPGPUs respectively. Achieving performance in BLAS requires moving away from conventional wisdom and evolving towards customized accelerator tailored for BLAS through algorithm-architecture co-design. In this paper, we present acceleration of Level-1 (vector operations), Level-2 (matrix-vector operations), and Level-3 (matrix-matrix operations) BLAS through algorithm architecture co-design on a Coarse-grained Reconfigurable Architecture (CGRA). We choose REDEFINE CGRA as a platform for our experiments since REDEFINE can be adapted to support domain of interest through tailor-made Custom Function Units (CFUs). For efficient sequential realization of BLAS, we present design of a Processing Element (PE) and perform micro-architectural enhancements in the PE to achieve up-to 74% of the theoretical peak performance of PE in DGEMM, 40% in DGEMV and 20% in double precision inner product (DDOT). We attach this PE to REDEFINE CGRA as a CFU and show the scalability of our solution. Finally, we show performance improvement of 3-140x in PE over commercially available Intel micro-architectures, ClearSpeed CSX700, FPGA, and Nvidia GPGPUs.

Index Terms—Parallel computing, dense linear algebra, multiprocessor system-on-chip, instruction level parallelism

1 INTRODUCTION
Several engineering and scientific applications require solution of dense linear systems of equations and linear least square problems where matrix factorizations like LU, QR and Cholesky methods play pivotal role. Traditionally, routines of these factorizations that are part of Linear Algebra Package (LAPACK) are written as a series of Basic Linear Algebra Subprogram (BLAS) calls [1][2]. Pictorial representation of double precision QR factorization routines, DGEQR2 and DGEQRF that are part of LAPACK is shown in the figure[1].

In the pictorial representation of DGEQR2 it can be observed that DGEQR2 is dominated by matrix-vector operations (DGEMV in BLAS) and DGEQRF is dominated by DGEQR2 and matrix-matrix operations (DGEMM in BLAS). Our experiments for DGEQR2 on Intel Core i7 and observation using Intel VTune™ suggests that for matrix of size $10k \times 10k$, 99% of the total time DGEMV executes while double precision inner product (DDOT) executes for hardly 1% of the total time in the operation of DGEQR2. Similarly, DGEQRF is dominated by DGEMM and it runs for 99% of the total time of DGEQRF while DGEQR2 runs for 1% of the time. Similar observations can be made in the routines like XGETRF (double/single precision LU factorization routine) and XPBTRF (double/single precision Cholesky factorization routine). Considering importance of BLAS in LAPACK, it is arguably one of the most interesting research problem to accelerate BLAS.

For acceleration of BLAS, a library based approach is adopted. Based on reference BLAS and LAPACK available on Netlib, Intel Math Kernel Library (MKL), IBM’s Engineering and Scientific Subroutine Library (ESSL), AMD’s AMD Core Math Library (ACML), Nvidia’s CUDA Linear Algebra (CULA) where CULA dense is for Dense Linear Algebra (DLA) and CULA sparse is for Sparse Linear Algebra (SLA), and cuBLAS which is yet another CUDA Basic Linear Algebra Subprograms are developed. There are also several open source packages for multithreads and General Purpose Graphics Processing Units (GPGPUs) based realizations like Parallel Linear Algebra Software for multicore Architectures (PLASMA) and Matrix Algebra on Multicore and GPGPU Architectures (MAGMA) use BLAS as a basic building block.
All these mentioned packages are developed for multicore and GPGPUs for realization of DLA computations in the most efficient way. PLASMA and MAGMA incorporate tiled algorithms that are capable of exploiting memory hierarchy efficiently\textsuperscript{3,4}. Despite all the efforts being directed towards acceleration of DLA computations, the performance attained by yesteryear platforms is as low as 15-17% of the theoretical peak performance in multicore and 55-57% of the theoretical peak performance in GPGPU at $\geq 65$W and $\geq 240$W power consumption respectively. Considering inability of GPGPU and multicore architectures in exploiting parallelism available in BLAS, we recommend algorithm-architecture co-design for BLAS as a solution for efficient realization of DLA. Performance of several recent realizations in detail is discussed in section\textsuperscript{2}.

Recently, Coarse-grained Reconfigurable Architectures (CGRAs) have gained popularity due to their power performance and flexibility\textsuperscript{5,6,7}. Performance advantage in CGRAs is attained by supporting selected number of data-paths out of all possible data-paths and hence they occupy middle ground between Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs)\textsuperscript{8,9,10,11}. CGRAs like REDEFINE have special feature that they can be customized for application domains where several data-paths belonging to a particular domain of interest are realized as a reconfigurable ASIC\textsuperscript{12}. In REDEFINE, several Tiles are connected through a Network-on-Chip (NoC) where Custom Function Units (CFUs) tailored for a particular domain decides performance of overall system for application domain\textsuperscript{12,13}. REDEFINE is shown in figure\textsuperscript{11(k)} along with several Tiles in a simulation environment.

Major contributions in this paper are as follows:

- Firstly, we present evaluation of legacy BLAS on off-the-shelf Intel/AMD processor and Nvidia GPGPUs where Cycles-per-Instruction (CPI) and Gflops/watt (Giga flops per watt) based analysis is discussed. Through detailed experiments it is shown that with the best efforts the performance achieved for BLAS in Intel/AMD and Nvidia GPGPU is between 0.02 to 0.25 Gflops/watt.
- We present Directed Acyclic Graph (DAG) based analysis of representative routines of Level-1, Level-2, and Level-3 BLAS and discuss available parallelism and possible data locality in these routines. We also identify macro operations and realize them on a Reconfigurable Data-path (RDP). Based on our analysis, we arrive at design of a Processing Element (PE).
- Several architectural enhancements are performed in the PE presented in\textsuperscript{13} for improving throughput of BLAS by exploiting parallelism and data locality. These enhancements result in efficient realization of sequential BLAS in the PE. In this exposition, we have extended scope of experiments to accommodate matrix sizes of $80 \times 80$ and $100 \times 100$ to bring more clarity of saturation in the attained performance after each enhancement.
- It is shown that through algorithm-architecture co-design, we are able to break the saturation point with each enhancement and improve the overall performance of the BLAS in PE. With each enhancement, we show that we are able to push the saturation point towards theoretical peak performance of the PE at very high energy efficiency.
- We attach the PE to the Routers in REDEFINE for parallel realization of BLAS and show algorithmic and architecture scalability.

The organization of the paper is as follows: In section\textsuperscript{2} some of the recent Multi-core, GPGPU, and custom realizations of BLAS are discussed. In section\textsuperscript{3} we present legacy BLAS realization on multicore and GPGPU and CPI and energy efficiency analysis of the realization. In section\textsuperscript{4} DAG based analysis of Level-1, Level-2, and Level-3 BLAS is presented and we derive preliminary specifications of a PE. Architectural enhancements in the PE for improvement in throughput in BLAS and parallel realization of BLAS on REDEFINE where we attach PE as a CFU to REDEFINE are presented in section\textsuperscript{5} and the work is summarized in section\textsuperscript{6}.

2 RELATED WORK

Over the years there have been several efficient realization of BLAS due to applicability in high performance scientific application. In this section, we survey several multicore and GPU based, and custom realizations of BLAS. We consider FPGA based realizations as custom realizations.

2.1 Software Packages for Multicore Platforms

The first ever software library LINPACK for performing linear algebra computations was developed in 1970s and early 1980s\textsuperscript{15}. Subsequently, LINPACK that used Level-1 BLAS as a basic building block was superseded by LAPACK that uses Level-3 BLAS as a basic building block\textsuperscript{2}. In the recent years, with arrival of multicore architectures, there have been several advancements in the parallel realization of LAPACK. One such effort is PLASMA, that can perform computations on multicore architecture with the help of dynamic scheduler Queuing and Runtime for Kernels (QUARK). PLASMA creates pipeline model for parallel execution by dynamic scheduling of BLAS kernels on the multicore platform\textsuperscript{16,3}. REDEFINE is shown in figure\textsuperscript{11(k)} along with several Tiles in a simulation environment.

A Formal Linear Algebra Method Environment (FLAME) focuses on issues related to programming of linear algebra programs. The focus of the FLAME project is to automatically generate efficient linear algebra codes for the underlying platform\textsuperscript{17,18}. Under the umbrella of FLAME project, BLAS-like Library Instantiation Software (BLIS) focuses on rapid scheduling of BLAS-like kernels on multicore architectures. Automatically Tuned Linear Algebra Software (ATLAS) is an matured open source package that generates BLAS for the underlying platform\textsuperscript{19,20}. ATLAS relies on legacy BLAS for generation of efficient code for the underlying platform where several parameters are tweaked to suit the underlying platform. OpenBLAS is another open source package that focuses on efficient realization of DLA computations\textsuperscript{21,22}. OpenBLAS relies on GotoBLAS for the performance where GotoBLAS is a set of assembly programs written for DLA computations. A major shortcoming of the packages like LAPACK, PLASMA, BLIS, ATLAS, and OpenBLAS is lack of support from the underlying platform resulting in 15-20% of the theoretical peak performance.

2.2 GPU Based Realizations

GPUs were originally designed for graphics processing are highly suitable for general purpose computing. There have been several packages developed to perform efficient BLAS functionality on GPUs. The most prominent of all of them is MAGMA software.
package [4]. MAGMA relies on MAGMA BLAS for the performance where the performance of MAGMA Dgemm is observed to be 57% of the peak performance of Tesla C2050 GPU with theoretical peak of 512 Gflops for double precision. KAUST BLAS (KBLAS) is one of the most recent and ongoing research project at KAUST. KBLAS internally relies on Cuda BLAS developed by Nvidia for the performance on GPU. BLASX presented in [23] focuses on optimization of Level-3 BLAS in multi-GPU environment. BLASX minimizes the global communication through two level hierarchical tile cache structures and achieves 92.68% of the in-core cuBLAS Dgemm. BLASX also contains better load balancing techniques compared to MAGMA and cuBLAS. Despite elegant scheduling technique and efficient exploitation of memory hierarchy BLASX, the performance achieved by BLASX is limited by cuBLAS Dgemm. In [24], requirement for cache memory is studied in detail for achieving superlinear speed-up for XGEMM. The study presented in [24] has no mention of data type if it is single precision or double precision. All the GPU based realization of BLAS fail to achieve high performance due to lack of support for GEMM primitives.

2.3 Custom Realizations

Customized accelerators are the class of architectures that are tuned for low energy, and unit area at high throughput for domain of interest [25][26]. Cell Broadband Engine (CBE) from International Business Machine (IBM) is a high performance architecture designed based on Power PC core [27]. Due to energy efficiency of CBE, it is viewed as an ideal platform for scientific computing [28]. ClearSpeed’s CSX architecture is back bone of ClearSpeed CSX600 and CSX700 processors. These processors have very high energy efficiency and operate at 12 Watts with theoretical peak of 96 GFlops [29][30][31]. A major shortcoming of ClearSpeed’s CSX and CBE architectures are low Gflops/W and Gflops/mm² [31].

There have been several attempts in viewing Field Programmable Gate Arrays (FPGAs) as high performance computing engines [32][33][34]. Mostly FPGAs are envisioned as a high performance co-processor of a programmable host processor for compute intensive applications [35][36]. A major disadvantage of FPGAs is higher power consumption than an Application Specific Integrated Circuit (ASIC) counterpart of the same logic. FPGAs are also limited by the on-chip logic resulting in scalability issues in high performance computing applications.

To overcome shortcomings of the existing architectures in exploiting parallelisms available in DLA computations, we take a route of algorithm-architecture co-design where we ensure high performance along with energy, area efficiency, and scalability.

3 BLAS REALIZATION ON OFF-THE-SHELF PROCESSORS

GEMM (Level-3 BLAS) and GEMV (Level-2 BLAS) are the most prominent routines in many engineering and scientific computations. These routines also have pedagogical importance due to its simplistic nature and often used to evaluate emerging architectures. In this section, first we discuss GEMM algorithm and then we examine some of the recent realization of GEMM. Based on the analysis of the profiling of the BLAS routines, we arrive at the pitfalls in extracting performance out of GEMM on contemporary multicore and GPU platforms. We further decide to design our own customized platform that is capable of extracting performance in BLAS through efficiently exploiting parallelism in BLAS.

3.1 GEMM and GEMV Algorithms

Algorithm 1 GEMM - General Matrix Multiplication

```plaintext
1: Allocate memories for input and output matrices and initialize input matrices
2: for i = 1 to m do
3:   for j = 1 to n do
4:     for k = 1 to m do
5:       C(i,j) = A(i,k)B(k,j) + C(i,j)
6:     end for
7: end for
```

Algorithm 2 GEMV - Matrix Vector Multiplication

```plaintext
1: Allocate memories for input matrix, input vector and output vector. Initialize input matrix and input vector
2: for j = 1 to n do
3:   for i = 1 to m do
4:     y(i) = A(i,j)x(j) + y(i)
5: end for
```

Pseudo codes for GEMM and GEMV are described in algorithms [1] and [2] respectively. GEMM algorithm has three loops and hence it belongs to Level-3 BLAS while GEMV belongs to Level-2 BLAS. For multiplying two matrices of size $m \times n$, it takes $n^3$ multiplications and $n^3 - n^2$ additions while GEMV takes $n^2$ multiplications and $n^2 - n$ additions. Typically, GEMM and GENV exhibit Instruction Level Parallelism (ILP) and Data Level Parallelism (DLP). GEMM also exhibits mighty data locality and is capable of sustaining $O(n)$ computations to communication ratio. All together, if exploited efficiently and accelerated, GEMM and GENV become an ideal candidate to be used as a basic building block for many high performance scientific applications. Since, GEMM has three nested loops, these loops can be permuted to change the access pattern of input matrices as shown in table [1]

| Loop Order | Inner Loop | Middle Loop | Inner Loop Data Access |
|------------|------------|-------------|------------------------|
| ijk        | dot        | vector × matrix | A by row, B by column |
| jik        | dot        | matrix × vector | A by row, B by column |
| ikj        | saxpy      | row saxpy    | B by row, C by row    |
| jki        | saxpy      | column saxpy | A by column, C by column |
| kji        | saxpy      | row outer product | B by row, C by row |
| kij        | saxpy      | column outer product | A by column, B by column |

In the table [1] saxpy stands for “scalar a multiplied by vector x plus vector y” and gazpy stands for generalized saxpy [37][38]. Further details of GEMM can be found in [37], and [38].

3.2 Performance Evaluation of GEMM and GENV

For contemporary architecture, highly efficient GEMM is realized as a subroutine in BLAS. There exists several vendor specific
realizations of DGEMM. For our experiments, we take DGEMM available in BLAS from The Netlib and for evaluation on GPU we use MAGMA\_DGEMM. We compile DGEMM for different Intel and AMD machines with different compiler options and evaluate the performance of DGEMM for these architectures. We evaluate MAGMA\_DGEMM on Telsa C2050.

Figure 2(a) depicts CPI of DGEMM when executed on Intel Haswell and AMD Bulldozer micro-architectures. For experimental results shown in figure 2(a) we have used BLAS and CBLAS\[ available in The Netlib and hence we have compiled BLAS and CBLAS using publicly available gfortran and gec. It can be observed in figure 2(a) that the CPI in the DGEMM saturates at around 0.85 for Intel’s Haswell and AMD’s Bulldozer. For the matrices that fit in the L1 cache achieve CPI that is lower than that for the matrices that do not fit in the L1 cache. This is due to L1 cache misses observed for larger matrices. While for the matrices that do not fit in the cache memory, attained CPI is slightly higher than the smaller matrices. For Intel Haswell and AMD Bulldozer, the lower bound of the CPI is 0.0625. It can be observed that with DGEMM, which is highly optimized routine of BLAS, CPI achieved is nowhere close to the lower bound of CPI of the architecture. Similar trend is observed when we consider Gflops as a performance metric as shown in figure 2(b).

It can be observed in the figure 2(b) that, for the matrices that fit in the cache memory, the Gflops attained is higher. For the larger matrices that do not fit in the cache memory, Gflops decreases due to cache misses. While these architectures have peak performance of 48 Gflops, attained performance is 10-11% of the peak performance.

One way to improve performance is to use the vendor specific compilers, since vendor specific compilers perform architecture aware optimizations in the programs. In order to further push the performance of DGEMM on Intel Haswell micro-architecture we use Intel C Compiler (icc) for compiling DGEMM routine in BLAS. Performance improvement in CPI and Gflops is shown in figures 2(c) and 2(d) respectively.

It can be observed in the figures 2(c) and 2(d) that the performance improvement in DGEMM is still far from the lower bound of the CPI and peak Gflops.

In the next set of experiments, we add −mavx compiler switch while compiling with icc. Performance improvement due to these switches is shown in the figure 2(e) and figure 2(f).

It can be observed from figures 2(e) and 2(f) that compiler switch −mavx improves performance and finally we are able to achieve 15-17% of the peak IPC (or CPI) and peak Gflops for DGEMM. Percentage of peak performance achieved is 4-5% for DGEMV and 55-57% for DGEMM in Tesla C2050 as depicted in figure 2(g) while percentage of peak performance achieved in Intel and Nvidia machines for DGEMM and DGEMV is ranging from 5% to 57% as shown in the figure 2(h). Considering Gflops watt as a performance parameter, DGEMV and DGEMM in the BLAS achieve performance of 0.14 Gflops/watt and 0.25 Gflops/watt respectively while MAGMA\_DGEMV and MAGMA\_DGEMM achieve performance of 0.03 Gflops/watt to 0.225 Gflops/watt respectively as shown in figure 2(i). One more observation we make from the figure 2(c) and VTune™ that use of −mavx compiler switch along with icc reduces number of instructions by half.

1. CBLAS consists of C wrappers written around BLAS where BLAS is written in Fortran
2. Just to re-emphasize: In case of CPI, lower the better

is because of use of FMA instructions in the generated assembly code. Reduction in the number of instructions leads to increase in CPI measured by VTune™. Though, there is an increase in CPI, performance in terms of Gflops is observed to be improved as shown in the figure 2(f). Hence, CPI measured by VTune™can not be considered as a correct measure for performance. We define terms Cycles-per-Flops (CPF) to be used instead CPI and Flops-per-Cycle (FPC) to be used instead IPC as follows:

\[
CPF = \frac{\text{Total Number of ClockTicks}}{\text{Total Number of Floating Point Operations}}
\]

We define FPC as follows:

\[
FPC = \frac{1}{CPF}
\]

CPF and FPC help us to evaluate performance of the architectures and algorithms more effectively. This is because the granularity of the compute resources considered in CPF and FPC is at the level of floating point operation and not at the level of Fused Multiply-add (FMA).

Across the experiments, we can observe that, significant efforts are needed to improve the performance of DGEMV and DGEMM on contemporary architectures and yet the attained performance is not satisfactory. We address this challenge of extracting performance from DLA computations through algorithm-architecture co-design in the subsequent sections of this paper.

4 Analysis of BLAS and CFU

In this section, we present graph based analysis of several Level-1, Level-2, and Level-3 BLAS. We choose several representative routines in all three levels of BLAS.

4.1 Vector Operations (Level-1 BLAS)

Level-1 BLAS typically has \(O(n)\) operations for a vector size of \(n\) and data movement required is also \(O(n)\). We analyze ddot, ddnrm2, and dakpy operations here. Figure 3 represents inner product of two vectors given by equation 3.

\[
e = x^T y
\]

where \(x = \begin{bmatrix} a_{11} & a_{12} & a_{13} & \ldots & a_{1n} \end{bmatrix} \) and \(y = \begin{bmatrix} b_{11} \\ b_{21} \\ \vdots \\ b_{n1} \end{bmatrix} \). DAG for ddot is shown in figure 3 for \(n = 8\).

The routine ddot has application in matrix-vector and matrix-matrix multiplication.

\(\text{dnrm2}\) is given by equation 4 and DAG for \(\text{dnrm2}\) is shown in figure 3.

\[
k = \sqrt{x^T x} = \sqrt{a_{11}^2 + a_{12}^2 + \ldots + a_{1n}^2}
\]

3. Due to availability of double precision floating point unit, we consider only routines that are with prefix “d”. For example first “d” in ddot represents double precision
Fig. 2: Performance of DGEMV and DGEMM on Different Micro-architectures

Fig. 3: DAGs of `ddot`, `dnrm2`, and `daxpy` for $n = 8$
In the following subsection of the paper, we present design of a PE that can efficiently exploit ILP in the chosen matrix multiplication algorithm.

4.3.1 Matrix Multiplication Algorithms
Over the years there have been several matrix multiplication algorithms proposed in the literature. In this subsection, we review and analyze Strassen’s Matrix Multiplication (SMM), Winograd’s Matrix Multiplication (WMM), and General Matrix Multiplication (GEMM). We consider \( A = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \) and \( B = \begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{bmatrix} \) as input matrices and \( C = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} \) as output matrix where \( A, B, C \) are equal sized block matrices and \( A, B, C \in \mathbb{R}^{2n \times 2n} \).

4.3.2 Strassen’s Matrix Multiplication
SMM algorithm is described in table 2 for \( 2 \times 2 \) block matrix.

Typically, SMM has two steps, 1) decompose step, and 2) merge step. In decompose step, matrix is divided in block matrices and \( M1 \) to \( M7 \) are computed. In merge step, \( C11 \) to \( C22 \) are computed. Directed Acyclic Graphs (DAGs) for SMM are shown in figure 5 for \( n = 1 \). It can be observed in the DAGs of SMM that the computation of \( C11 \) to \( C22 \) depends on computations of \( M1 \) to \( M7 \).

This dependencies in the DAGs of SMM results in higher execution time of SMM. It can also be observed from DAGs of SMM in figure 5 that \( M1 \) to \( M7 \) can potentially be executed in parallel and \( C11 \) to \( C22 \) can also be executed in parallel. One of the way this parallelism can be exploited is through processor pipeline and pipelined arithmetic units. Asymptotic complexity of SMM is \( O(n^{2.81}) \).

4.3.3 Winograd’s Matrix Multiplication
WMM algorithm operates on the same principle as SMM as shown below:

It can be observed from WMM algorithm that it takes 7 block matrix multiplications and 15 matrix additions unlike SMM where the number of block matrix multiplication is same but the number of matrix additions are 18. DAGs for WMM are shown in figure 5 for \( n = 1 \).

WMM has same asymptotic complexity as SMM. In practical scenarios, execution time of WMM is observed to be slightly less than SMM due to fewer additions.

4.3.4 General Matrix Multiplication
GEMM for multiplication of \( A \) and \( B \) can be described by following expressions:

\[
\begin{align*}
C11 &= A_{11}B_{11} + A_{12}B_{21} \\
C12 &= A_{11}B_{12} + A_{12}B_{22} \\
C21 &= A_{21}B_{11} + A_{22}B_{21} \\
C22 &= A_{21}B_{12} + A_{22}B_{22}
\end{align*}
\]

DAGs for a \( 2 \times 2 \) matrix is shown in figure 5. It can be observed from the DAGs of GEMM that it takes 8 multiplications and 4 additions. Asymptotic complexity of GEMM is \( O(n^3) \).

SMM and WMM have lower asymptotic complexities compared to GEMM. A major disadvantage of SMM and WMM is
that they are more suitable for square matrices where size is a power of two. For the matrix sizes where this condition is not met, a complex matrix partitioning scheme is required. Hence, we adopt GEMM over SMM and WMM due to following reasons:

- A complex partitioning scheme required for the matrices in SMM and WMM results in a intricate scheduling scheme for the blocks of input matrices. A way to alleviate these complications is to zero pad the matrices. This zero padding results in few more computations, mostly $O(n^2)$. The zero padding does not reduce the complexity of the implementation since naive zero padding scheme is not efficient
- GEMM has higher pedagogical importance than SMM and WMM. GEMM is highly preferred to evaluate the emerging architectures over SMM and WMM due to its simple structure and ease of implementation

### 4.3.5 Anatomy of General Matrix Multiplication

To discuss available parallelism in GEMM, we take a matrix multiplication of size $4 \times 4$ as an example.

DAGs for $m = n = 4$ for algorithm 1 are shown in figure 6 for computation of elements $c_{11}$ to $c_{44}$. It can be observed in the figure that all the multiplications in the block of the matrix can be computed in parallel. The dependencies are due to accumulation of the multiplied elements of the input matrices.

Potentially, in multiplication of matrix of size $n \times n$, all the $n^3$ multiplications can be computed in parallel. In case of $4 \times 4$ matrix, all 16 elements can be computed in parallel as shown in figure 6. The accumulation process while computing the elements of the resultant matrix enforce the dependencies resulting in pipeline

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**TABLE 2:** Computations in the different Levels of DAGs of SMM at first step of Recursion in $2 \times 2$ Block Matrix Multiplication

| Level 1 | Level 2 | Level 3 | Level 4 |
|---------|---------|---------|---------|
| $T_1 = A_{11} + A_{22}$ | $M_1 = T_1 \times T_2$ | $K_1 = M_1 + M_4$ | $C_{11} = K_1 - K_2$ |
| $T_2 = B_{11} + B_{22}$ | $M_2 = T_2 \times B_{11}$ | $K_2 = M_3 - M_4$ | $C_{22} = K_3 + K_4$ |
| $T_3 = B_{12} - B_{21}$ | $M_3 = A_{11} B_{3}$ | $K_3 = M_1 - M_2$ | |
| $T_4 = B_{21} - B_{11}$ | $M_4 = A_{22} B_{4}$ | $K_4 = M_4 + M_6$ | |
| $T_5 = A_{11} + A_{12}$ | $M_5 = T_5 B_{22}$ | $C_{12} = M_3 + M_5$ | |
| $T_6 = A_{21} - A_{11}$ | $M_6 = T_6 B_{11}$ | $C_{21} = M_2 + M_4$ | |
| $T_7 = B_{11} + B_{12}$ | $M_7 = T_7 B_{12}$ | | |
| $T_8 = A_{12} - A_{22}$ | | | |
| $T_9 = B_{21} + B_{22}$ | | | |

**TABLE 3:** Computations in the different Levels of DAGs of WMM at first step of Recursion in $2 \times 2$ Block Matrix Multiplication

| Level 1 | Level 2 | Level 3 | Level 4 |
|---------|---------|---------|---------|
| $S_1 = A_{11} + A_{22}$ | $S_2 = S_1 - S_1$ | $S_4 = A_{12} - S_2$ | $M_6 = S_4 B_2$ |
| $S_3 = A_{11} - A_{21}$ | $S_6 = B_2 - S_5$ | $S_8 = S_6 - B_2$ | $M_7 = A_{22} S_8$ |
| $S_5 = B_{12} - B_{11}$ | $M_4 = S_3 S_7$ | $M_1 = S_2 S_6$ | $V_1 = M_1 + M_2$ |
| $S_7 = B_{22} - B_{12}$ | $M_5 = S_1 S_5$ | | $C_{12} = V_1 + K_1$ |
| $M_2 = A_{11} B_{11}$ | $C_{11} = M_2 + M_3$ | | |
| $M_3 = A_{12} B_{21}$ | | | |

**Fig. 5:** SMM, WMM, and GEMM for $2 \times 2$ Block Matrix

**Fig. 6:** DAGs in GEMM for $4 \times 4$ Matrix
Algorithm 3 Block General Matrix Multiplication

1: Allocate memories for input and output matrices
2: for $i = 1$ to $m/4$ do
3: \hspace{1em} for $j = 1$ to $n/4$ do
4: \hspace{2em} \hspace{1em} for $k = 1$ to $n/4$ do
5: \hspace{3em} \hspace{2em} \hspace{1em} $C = \text{BLOCK4ADD}(\text{BLOCK4MUL}(A,B),C)$
6: \hspace{2em} \hspace{1em} end for
7: \hspace{1em} end for
8: end for

Algorithm 3 depicts DGEMM with $4 \times 4$ block matrix multiplication (assuming that the matrix dimensions are multiple of 4). In algorithm 3, BLOCK4MUL is multiplication of matrices of size $4 \times 4$, and BLOCK4ADD is addition of matrices of size $4 \times 4$. A pitfall in the unrolling scheme is the exigency of locally available registers. Typically, for $n \times n$ matrix, if fully unrolled, requires $3n^2$ registers. Hence, for a large matrix, it can not be unrolled due to lack of locally available registers, but a small block of the matrix can be unrolled to exploit the fine grained parallelism in the block through processor pipeline and pipelined arithmetic units. In our experiments with PE explained in section 4.4, we have adopted a conservative approach where we have assumed space for $n^2$ intermediate results in the loacal registers and hence we have considered a $4 \times 4$ block matrix with 64 registers of 64-bit wide. In parallel realization of GEMM, different blocks of $4 \times 4$ can be computed in parallel on different PEs. While realizing GEMM on a single PE, we try to exploit parallelism that is available in a block of $4 \times 4$ and in parallel realization on REDEFINE, we try to exploit parallelism across the blocks.

In the next section we present a PE design to skillfully exploit the parallelism that exist in the block of $4 \times 4$ matrix.

### 4.4 Processing Element Design

For initial design of PE, we consider classical sequential architecture model. As a first design, we take a fully pipelined double precision floating point adder, and multiplier arithmetic units as compute resources. Architecture of PE is shown in figure 7.

As shown in the figure, the initial design of PE consists of an Instruction Memory, a Decoder to decode the instructions, a Register File with 64 registers, and pipelined double precision Floating Point Unit (FPU) \[39\][40]. The FPU consists of a multiplier, an adder, a square root, and a divider. For computing matrix multiplication with large matrices, we choose $4 \times 4$ as a block matrix. For the matrices that are not multiple of 4, we partition them in the blocks of $4 \times 4$ as many times as possible and for the residual matrix, we perform unblocked multiplication. Operation of the PE can be described in the following steps:

- **Step 1:** Bring the input matrices to the Register File that by sending Load request to the upper level of the memory
- **Step 2:** Perform matrix multiplication
- **Step 3:** Store back the resultant matrix to the upper level of memory

### 4.5 Simulation Environment and Initial Results

For simulations we connect PE shown in the figure to external/global memory. Initially we use 64 (64 – bit wide) registers, 16KB of instruction memory for our experiments. We model global/external memory delay by placing pipelined delay of 20 stages.

#### 4.5.1 Initial Results

For our experiments, we choose matrix sizes $20 \times 20$, $40 \times 40$, $60 \times 60$, $80 \times 80$, and $100 \times 100$ as a representative matrix sizes for our experiments.

It can be observed in the table 4 that as we increase the matrix size, the CPF decreases and saturates around 1.6 while performance in terms of Gflops/watt is observed to be at 17.3 Gflops/watt at 0.2 GHz. In other words, as we increase the matrix size, the FPC saturates at 62.5% of peak floating point operations per cycle. Here, since, we can potentially compute one multiplication and one addition in parallel, the peak FPC $= 2$.

In this section, we reviewed some of the matrix multiplication techniques. We discussed asymptotic complexity and graph based analysis of three different matrix multiplication algorithms. We justified our choice of GEMM over SMM and WMM algorithms. We presented additional details of GEMM with an example of $4 \times 4$ matrix and proposed an initial design of a PE that achieves CPF of 1.6 and performance of 17.3 Gflops/watt. Intuitively, performance of the PE can be improved methodically by enriching the PE with compute and memory resources.

### 5 Micro-architectural Enhancements in PE and Parallel Realization on REDEFINE

Based on anatomy of the GEMM and design of the PE presented in section 4.4, in this section we dwell on micro-architectural enhancements of the PE. We methodically enhance PE that improves CPF. The PE described in section 4.4 is considered as a Floating Point Sequencer in this section.
5.1 Introducing Local Memory and Load-Store CFU

Major drawbacks of the PE design presented in section 4.4 are no overlap of computations and communication and lack of exploitation of data locality in GEMM. To address these issues, we introduce a Load-Store CFU that operates simultaneously with FPS (depending on availability of data), and facilitates overlap of computation and communication. We also place a Local Memory (LM) of size 256kbits in the Load-Store CFU to exploit data locality in GEMM. Enhanced PE design with FPS and Load-Store CFU is shown in figure 8.

Introduction of an LM in Load-Store CFU inside PE improves the data locality. This improved data locality creates further opportunities for exploitation of higher ILP by increasing compute resources in FPS. Increased compute resources in the FPS demand for improvisation in the data availability in the Register File for computations. In this section we present methodical architectural enhancements in the PE for reduction in latency in execution of GEMM. These enhancements in the PE ensure lower latency in execution of GEMM leading to overlap between computation and communication up-to 90% in GEMM and we are also able to achieve up-to 74% of the peak CPF. To highlight the reduction in the latency due to each architectural enhancement, we consider $20 \times 20$, $40 \times 40$, $60 \times 60$, $80 \times 80$, and $100 \times 100$ matrix sizes as a representative for our experiments. Reduction in the latency due to introduction of Load-Store CFU and LM (refer figure 8) is shown in the table 5.

It can be observed in the table 5 that introduction of LM in the Load-Store CFU improves performance by 2x and as we increase matrix size the performance improves due to improved data locality.

5.2 Special Instructions

In the first enhancement, we try to exploit higher ILP by increasing resources in the FPS that in turn improves performance significantly. This improved performance motivates us to improve data availability in the Register File residing inside FPS. We introduce two types of special instruction: 1) DOT instructions that are executed in FPS on a specialized fully pipelined hardware structure, and 2) Block Data Load and Block Data Store instructions that are executed in the Load-Store CFU.

5.2.1 DOT Instruction

Since we support block size of $4 \times 4$, we introduce a hardware that can perform inner product of a 4-element vector. The hardware structure to compute 4-element vector inner product is shown in figure 9. We further make this hardware structure reconfigurable to support 2-element and 3-element vector inner products to support different matrix sizes. We name this unit as a Reconfigurable Data-path (RDP). Through reconfiguration, RDP can be re-casted to perform macro operations encountered in some of the algorithms in BLAS discussed in the section 4. The RDP is shown in figure 9.

For larger matrices ($> 4 \times 4$) that do not fit in the Register File in FPS for matrix multiplication, we use block size of $4 \times 4$. For the matrices that do not have their size as multiple of 4, we use 2-element, and 3-element inner product configurations of RDP. In this exposition, we restrict our experiment to the matrices with size of multiple of 4 and hence we use 4-element inner product configuration (also termed as DOT4 configuration) of RDP. DOT4 configuration of RDP has a 15-stage deep pipeline. Assuming no pipeline stalls, we can potentially maintain 15 DOT4 instructions in a state of execution. This DOT4 instruction leads to exploitations of higher ILP in a block of $4 \times 4$ in GEMM. Improvement in latency of GEMM due to DOT4 instruction is shown in table 5.

It can be observed from the table 6 that as we increase the matrix size, the benefit due to DOT instruction improves. This is due to improved exploitation of ILP in the FPS.

5.2.2 Block Data Load and Block Data Store Instructions

We further aim to reduce handshaking between LM and GM. This reduction in the handshaking in-turn improves data availability in the Register File. In order to reduce the handshaking between PE and the next level of the Memory, we introduce instructions that can load/store data in a block fashion. Performance improvement due to Block Data Load and Block Data Store is shown in table 7 where we have used $4 \times 4$ as a block size for the transfer.

It can be observed from the table 7 that as we increase matrix size, the benefit due to Block Data Load/Store does not improve. Rather the performance is observed to be saturating. This is because of the constant block size of $4 \times 4$ across all the matrix sizes. Supporting larger block size is not possible due to limited registers availability in the Register File in the FPS. It can also be observed in table 7 that the latency gap between $20 \times 20$ and $40 \times 40$, and $40 \times 40$ and $60 \times 60$ is also decreasing and it is likely to saturate at some point. Further experiments show that the gap saturates at 10% for larger matrix sizes.
TABLE 5: Latencies of $20 \times 20$, $40 \times 40$, $60 \times 60$, $80 \times 80$, and $100 \times 100$ GEMM (with LM and Load-Store CFU (PE-Architectural Enhancement 1 (AE1))

| Matrix Size | $20 \times 20$ | $40 \times 40$ | $60 \times 60$ | $80 \times 80$ | $100 \times 100$ |
|-------------|----------------|----------------|----------------|----------------|-----------------|
| Latency (in clock cycles) without LM | 39000 | 312075 | 1040754 | 2457600 | 4770000 |
| Latency (in clock cycles) with LM | 23000 | 178471 | 595421 | 1410662 | 2730365 |
| Improvement in Latency in terms of percentage | 41% | 42.5% | 42.7% | 42.6% | 42.6% |
| Gflops/watt | 14.37 | 15.53 | 15.77 | 15.81 | 15.98 |

TABLE 6: Latencies of $20 \times 20$, $40 \times 40$, $60 \times 60$, $80 \times 80$, and $100 \times 100$ GEMM (PE with Load-Store CFU, with DOT instruction (PE-Architectural Enhancement 2 (AE2))

| Matrix Size | $20 \times 20$ | $40 \times 40$ | $60 \times 60$ | $80 \times 80$ | $100 \times 100$ |
|-------------|----------------|----------------|----------------|----------------|-----------------|
| Latency (in clock cycles) | 15251 | 113114 | 371699 | 877124 | 1696921 |
| Improvement over table 5 | 33.7% | 36.6% | 37.5% | 37.82% | 37.85% |
| Gflops/watt | 10.52 | 11.49 | 11.85 | 11.93 | 12.06 |

TABLE 7: Latencies of $20 \times 20$, $40 \times 40$, $60 \times 60$, $80 \times 80$, and $100 \times 100$ GEMM (PE with Load-Store CFU, with DOT4, and Block Data Load/Store instructions (PE-Architectural Enhancement 3 (AE3))

| Matrix Size | $20 \times 20$ | $40 \times 40$ | $60 \times 60$ | $80 \times 80$ | $100 \times 100$ |
|-------------|----------------|----------------|----------------|----------------|-----------------|
| Latency (in clock cycles) | 12745 | 97136 | 324997 | 784828 | 1519083 |
| Improvement over table 6 | 16.4% | 14.1% | 12.5% | 10.51% | 10.48% |
| Gflops/watt | 12.59 | 13.38 | 13.56 | 13.33 | 13.47 |

5.3 Bandwidth Increase

Increased resources in the FPS improves performance by almost 2x, and reduced handshaking between LM and the upper level of the memory improves performance by 10%. We still see significant gap between our desired performance and attained performance. The reason for this gap is mainly because of under utilization of the RDP that is configured as DOT4. In order to improve resource utilization of RDP, in this architectural enhancement, we increase bandwidth between FPS and Load-Store CFU to 4 times. We consider increase in the bandwidth to 4 times since the block size supported in FPS is $4 \times 4$. We transfer 256-bit data between FPS and Load-Store CFU in contrast to previous realization where we transferred 64-bit data. The communication between FPS and Load-Store CFU at higher rate ensures better data availability in the Register File of FPS. The performance improvement due to increase in the bandwidth is shown in table 8.

It can be observed in table 8 that as we increase the matrix size the benefits due to increased bandwidth between FPS and Load-Store CFU in the PE improves. This is mainly because of better utilization of RDP (here configured as DOT4).

5.4 Pre-fetching

To improve the utilization of RDP further in the FPS, we restructure the loop in GEMM. We re-write algorithm 1 as algorithm 4

Algorithm 4 General Matrix Multiplication with Pre-fetching

1: Allocate memories for input and output matrices
2: for $i = 1$ to $m$
3: for $j = 1$ to $n$
4: $C[i][j] = A[i][k] \times B[k][j]$
5: for $k = 1$ to $n$
6: $C[i][j] = A[i][k] \times B[k][j] + C[i][j]$
7: end for
8: end for
9: end for

Fig. 10: Pre-fetching Matrix Elements for the Next Iteration

Re-structuring the loops in the algorithm allows us to pre-fetch the matrix block required for the next iteration. This results in better exploitation of FPU pipeline by reduced instruction stalls in FPS as shown in figure 10. The shaded portion in the figure 10 depicts the reduction in the instruction stalls in FPS when there is a pre-fetch of the block of the matrix required in the next iteration for computation. In figure 10, there are two portions, 1) before pre-fetching, and 2) after pre-fetching. Arrows in the figures depict execution of different types of operations such as computations in FPS, loading/storing of data from/to GM (or EM) memory, loading/storing of data from/to GM.

Improvement attained by pre-fetching is shown in table 9. It can be observed in the table 9 that as we increase matrix size the benefits due to pre-fetching increases. This is mainly because of improvement in data availability in the Register File of the FPS.

Collectively, the reduction in execution cycles of GEMM can be seen in the figure 11(a) as we perform different architectural enhancements in the PE. It can be clearly observed that finally we get speed-up of 7x for matrix of size $20 \times 20$, 8.13x for the matrix of size $40 \times 40$, and 8.34x for the matrix of size $60 \times 60$ 11(b).

It can be observed from figure 11(b) that as we perform different architectural enhancements, the ratio of Latency to
(a) Reduction in the Latency in DGEMM (b) Latencies Normalized to Total Computations due to Architecture Enhancements (c) Cycles per Floating Point Operation in DGEMM

(d) Floating Point Operations per Cycle in DGEMM (e) Percentage of Peak FPC in DGEMM with Each Architectural Enhancement (f) Percentage of Peak FPC in DGEMV with Each Architectural Enhancement

(g) Percentage of Peak FPC in DDOT (h) Gflops/watt for DGEMM at 0.2GHz, 0.33GHz, 0.95GHz, and 1.81GHz (i) Gflops/mm² for DGEMM at 0.2GHz, 0.33GHz, 0.95GHz, and 1.81GHz

(j) Performance Comparison of REDEFINE-PE with Other Platforms (k) Simulation Environment where Tile array of 2×2 is used for realizing DGEMM

Fig. 11: Performance of DGEMM
computations reduces. If we denote the ratio of Latency to total computations by $\alpha$ then

$$\alpha = \frac{\text{Latency}}{\text{Total Computations in Terms of DOT4}}$$

(7)

It can be observed in the figure [11(b)] that as we increase matrix size $\alpha$ asymptotically approaches 1. $\alpha = 1$ is a case where there is a complete overlap of computation and communication. Complete overlap of computations and communication is not possible in the real life scenario and hence $\alpha$ can never become 1.

Figure [11(c)] depicts CPF for matrices of size $20 \times 20$, $40 \times 40$, and $60 \times 60$. It can be observed in the figure [11(c)] that as we perform enhancements the CPF tends to decrease and this trend is observed across all the matrices. Figure [11(d)] depicts FPC (where FPC = 1/CPF). It can be observed from figure [11(d)] that, as we perform enhancements in the PE, FPC improves dramatically. Although CPF and FPC are good measure of performance of a PE, they do not convey enough information about how efficiently compute resources are utilized in the PE.

Percentage of peak FPC attained in PE after every enhancement is shown in figure [11(e)]. Figure [11(e)] depicts an interesting trend where the peak FPC reduces drastically and then with further architectural enhancements, improves. As our enhancements suggest, in the first enhancement where we place Load-Store CFU with LM for overlap of computation and communication, the FPC achieved saturates at 54% of the peak FPC.[5] We strongly intend to break this saturation point since 54% of the peak is not a satisfactory performance. In order to break this saturation point we further enhance FPS with compute resources that leads to higher theoretical peak FPC. At this point achieved FPC reduces at AE2 as shown in the figure [11(e)]. This is because of increased compute resources. Our further enhancements help us to improve the resource utilization of the increased resources in FPS and achieve up-to 74% of the peak FPC of the PE.

We presented methodical architectural enhancements to improve the performance of PE. Through architectural customizations, we could break saturation point at 54% and improve performance of PE. In other words, we showed that the performance of the algorithms can be improved by customizations that are specific to the algorithms. Here, we showed this with example of GEMM

6. Here peak FPC = $\frac{1}{\text{CPF}} = 1 = 2$
7. Here peak FPC = $\frac{1}{\text{CPF}} = \frac{1}{2} = 7$. Increase in peak FPC is due to DOT4 instruction

which is a Level-3 BLAS. Finally, 35.7 Gflops/watt in the PE is achieved through careful realization of Level-3 BLAS.

### 5.5 Parallel Realization of Level-3 BLAS

For parallel realization of DGEMM, our two different simulation environments are shown in figure [11(k)]. In figure [11(k)] shaded portion of the Tile array (except the last column) which is $2 \times 2$ Tiles is used for the computations where we realize DGEMM while the last column is used for storing input and output matrices. We use Octave for generating input matrices. Similarly, we use $3 \times 3$ portion of the Tile array for realizing DGEMM.

In our experiments, if output matrix is of size $n \times n$ then we divide the output matrix into blocks of $\frac{n}{2} \times \frac{n}{2}$ where $b \times b$ is the Tile array that we are using. In our experiments $b = 2$ or 3. For example, if output matrix is of size $20 \times 20$, and we are using $2 \times 2$ of the Tile array to compute the DGEMM, we divide output matrices into $10 \times 10$ block matrices. Now, in each Tile that we are using, we compute one of the block of size $10 \times 10$. Similarly, if output matrix is of size $60 \times 60$, and Tile array that is used for computing DGEMM is of size $3 \times 3$ then block of $20 \times 20$ is computed in each of the Tile of REDEFINE.

![Fig. 12: Speed-up in REDEFINE for DGEMM for Different Configurations](image)

Speed-up attained in REDEFINE is is shown in the figure [12] when Tile array of size $2 \times 2$, $3 \times 3$, and $4 \times 4$ are used for the experiments. It can be observed from the figure [12] that when we use Tile array of $2 \times 2$ the speed-up over PE realization approaches 4 as we increase matrix size. When we use Tile array of $3 \times 3$ the speed-up over PE realization approaches 9, and for Tile array of size $4 \times 4$ the speed-up attained approaches 16. For small matrices, communication with the last column of the Tile array is dominant over computations in the Tile. For example, for a matrix
of size $20 \times 20$ and Tile array size of $2 \times 2$, each Tile computes $10 \times 10$ block of the resultant matrix. Ignoring the coefficient of the highest order term, there will be $10^3$ computations over $10^2$ loads/stores. Computation to communication ratio in for $20 \times 20$ matrix will be 10 in each Tile. For matrix a of size $60 \times 60$ where each Tile will compute a block of $20 \times 20$ matrix, computation to communication ratio is 20. One more observation we make here is that, as we increase the matrix size, speed-up in redefine over PE saturates. This is because of the saturation in the parallelism exploited by the PE that is attached in each Tile of redefine.

In this section, we presented results for the PE that we presented in section 4.4. We use the estimation methodology presented in [31], [41], and [26] for fair comparison of the platforms. As shown in the figure [II] it can be observed that the performance of the PE is 40-140x better than Intel Core architectures while 7-139x better than Nvidia GPUs. Compared to Altera FPGA, PE is 10x better in terms of GFlops/watt while compared to ClearSpeed CSX700 it is almost 3x better.

6 Conclusion

While the recent realizations for matrix computations focus on architectural customization for DLA, in this paper we presented a novel way of algorithm-architecture co-design for breaking the performance saturation point in BLAS and presented a systematic analysis of BLAS, and presented a systematic architecture-parallelism co-design for breaking the performance saturation point in BLAS and presented a systematic analysis of BLAS, and de-

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Farhad Merchant Farhad Merchant is a Research Fellow at Hardware and Embedded Systems Lab, School of Computer Science and Engineering, Nanyang Technological University, Singapore. He received his PhD from Computer Aided Design Laboratory, Indian Institute of Science, Bangalore, India. His research interests are algorithm-architecture co-design, computer architecture, reconfigurable computing, development and tuning of high performance software packages.

Tarunvatwani Tarunvatwani is a fresh B.Tech. graduate from Indian Institute of Technology, Jodhpur, India. His research interests are computer architecture, high performance computing, machine learning, performance tuning of different software packages.

SoumyenduRaha Soumyendu Raha obtained his PhD in Scientific Computation from the University of Minnesota in 2000. Currently he is a Professor of the Computational and Data Sciences Department at the Indian Institute of Science in Bangalore, which he joined in 2003, after having worked for IBM for a couple of years. His research interests are in computational mathematics of dynamical systems, both continuous and combinatorial, and in co-development and application of computing systems for implementation of computational mathematics algorithms.

RanjaniNarayan Dr. Ranjani Narayan has over 15 years experience at IIsc and 9 years at Hewlett Packard. She has vast work experience in a variety of fields: computer architecture, operating systems, and special purpose systems. She has also worked in the Technical University of Delft, The Netherlands, and Massachusetts Institute of Technology, Cambridge, USA. During her tenure at HP, she worked on various areas in operating systems and hardware monitoring and diagnostics systems. She has numerous research publications. She is currently Chief Technology Officer at Morphing Machines Pvt. Ltd, Bangalore, India.
S K Nandy  S. K. Nandy is a Professor in the Department of Computational and Data Sciences of the Indian Institute of Science, Bangalore. His research interests are in areas of High Performance Embedded Systems on a Chip, VLSI architectures for Reconfigurable Systems on Chip, and Architectures and Compiling Techniques for Heterogeneous Many Core Systems. Nandy received the B.Sc (Hons.) Physics degree from the Indian Institute of Technology, Kharagpur, India, in 1977. He obtained the BE (Hons.) degree in Electronics and Communication in 1980, MSc.(Engg.) degree in Computer Science and Engineering in 1986, and the Ph.D. degree in Computer Science and Engineering in 1989 from the Indian Institute of Science, Bangalore. He has over 170 publications in International Journals, and Proceedings of International Conferences, and 5 patents.