On the likelihood of multiple bit upsets in logic circuits

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Abstract—Soft errors have a significant impact on the circuit reliability at nanoscale technologies. At the architectural level, soft errors are commonly modeled by a probabilistic bit-flip model. In developing such abstract fault models, an important issue to consider is the likelihood of multiple bit errors caused by particle strikes. This likelihood has been studied to a great extent in memories, but has not been understood to the same extent in logic circuits. In this paper, we attempt to quantify the likelihood that a single transient event can cause multiple bit errors in logic circuits consisting of combinational gates and flip-flops. In particular, we calculate the conditional probability of multiple bit-flips given that a single bit flips as a result of the transient. To calculate this conditional probability, we use a Monte Carlo technique in which samples are generated using detailed post-layout circuit simulations. Our experiments on the ISCAS’85 benchmarks and a few other circuits indicate that, this conditional probability is quite significant and can be as high as 0.31. Thus we conclude that multiple bit-flips must necessarily be considered in order to obtain a realistic architectural fault model for soft errors.

Index Terms—soft error, multiple bit-flips, fault model, logic circuits

I. INTRODUCTION

RELIABILITY of semiconductor devices has become an important area of concern, especially with technology scaling. Circuits are subject to permanent faults, caused due to transistors failing because of phenomena such as hot carrier injection, negative bias temperature stability, oxide breakdown and so on [1]. Circuits can also be subject to transient faults caused due to process variations, signal integrity issues, power supply noise and high-energy particle strikes (neutrons from cosmic rays, alpha particles) [2]. Such errors which do not cause permanent damage to the device are called soft errors and the rate at which they occur is known as the soft error rate (SER).

Soft errors have become a major reliability concern for semiconductor devices in the past few decades. When high energy particles such as alpha particles, protons or neutrons from either cosmic rays or packaging materials strike sensitive regions of a semiconductor device, they generate electron-hole pairs. This process leads to deposition of a certain amount of charge in the device. For example, if the high energy particle strikes a memory cell and if the deposited charge is greater than a certain amount of charge called the critical charge, it can flip the stored bit (0 \rightarrow 1 or 1 \rightarrow 0). Since this error can be reversed by rewriting the correct value and since it is not caused due to permanent physical damage to the device, it is termed “soft error”. A similar process can occur when a particle strikes a sensitive p-n junction in a transistor, creating a transient or a glitch in a combinational logic circuit.

A complete historical review and the experimental results of soft errors and their impact have been presented in [3]. Experiments and field tests conducted on large computer systems at different locations indicate a memory error rate of $1.6 \times 10^{-12}$ upsets/bit-hr and an average of one error per month [5]. Most early studies considered bit-flips in memories. Several studies have also indicated that the SER of a system tends to increase as technology scales [6], [7], [8], which is mainly attributed to the increase in memory density. Also, as the technology scales, a single particle strike can affect more than one memory cell at a time, resulting in multiple bit errors [9], [10].

Single event transients (SETs) in logic circuits were not given as much importance, because such circuits tend to exhibit inherent masking phenomena (described in Section II), which prevent the transients from causing an error at a latching element. Soft errors are generally modeled by a single bit-flip fault model, in which, a single random bit is expected to flip [11], [12], [13]. But, as the technology scales, a single particle strike can affect more than one drain of a transistor, resulting in multiple transients which can propagate to cause multiple bit-flips at the output of a circuit [14]. Further, the masking phenomena seem to reduce as technology scales, and thus, the impact of soft errors on logic circuits is likely to increase, as has been indicated in [15], [16], [17], [18].

In this paper, we address the following question: Suppose that a particle strike affects a drain of a transistor resulting in a single transient in a logic circuit. Given that this transient propagates and flips the content of a single flip-flop, what is the probability that it can flip multiple flip-flop values? This involves the computation of a conditional probability of multiple bit-flips given that at least one bit has flipped. If this conditional probability is significant, then an architectural level fault model for soft errors must incorporate multiple bit failures in order to identify effective error correction schemes. A few studies done in the past, to quantify the multiple bit-flip probability [19], [20], [21] indicate that multiple bit flips are likely. However, the studies use approximate modeling techniques to arrive at these conclusions, and the confidence in their conclusions is doubtful. Our work uses a Monte Carlo scheme in which detailed simulations (using SPICE) of post layout circuit netlists are used to arrive at estimates of this conditional probability. Our results (on the ISCAS’85 bench-
marks and a few other circuits) indicate that, the probability of multiple bit-flips amongst the faulty cases is significant and can be as high as 0.31. Thus, multiple bit-flips must be incorporated in order to obtain a realistic fault model for soft errors.

The rest of this paper is organized as follows. In Section II we review related work on fault models for soft errors and prior work on multiple bit upsets. Section III describes our methodology for calculating the probability of multiple bit flips. Experimental results on ISCAS'85 benchmarks and a few other circuits are presented in Section IV. Section V summarizes and concludes the paper.

II. RELATED WORK

Several experiments on memories have already demonstrated that multiple bit upsets do occur due to a single particle strike [9], [10]. Experiments in [9] conclude that about 7% of the total events are multiple bit upsets (MBU) in memories. Schemes such as bit interleaving along with error correction codes are already in place to handle MBUs in memories. The rate of MBUs is reported to increase with technology scaling, both in memories [9] and in logic circuits [22].

The impact of soft errors on combinational/sequential circuits was not studied in detail in the past, due to the presence of the following three inherent masking phenomena in circuits:

1) Logical masking, in which, the type of logic gate and its input combinations could mask the propagation of the transient.
2) Electrical masking, in which the glitch can get attenuated as it passes through the logic stages.
3) Latching window masking, in which, the glitch might be masked if it does not fall within the setup/hold times of the capturing latch.

However, as the technology scales, the impact of these masking phenomena seems to reduce and hence the SER in logic circuits tends to increase [15], [16], [17], [18]. Several algorithms have been designed to estimate SER of logic circuits in general, without emphasizing on bit correlations or multiple bit upsets. Some of these methodologies build models for glitch generation/propagation and masking [23], [24], [25], employ testing and probability theory [26], [27], employ the method of binary decision diagrams [28] and probability transfer matrices [29], instead of running circuit simulations. Most of these techniques are designed to give fast estimates of the SER at the expense of accuracy. For example, in [30], the authors report an inaccuracy of up to 20% against SPICE simulations. In [25], an SER estimation tool is built, under the assumption that logic paths do not attenuate the glitches to a large extent and report an error of 25% in the results based on their assumption. They conclude that single bit-flips account for over 95% of all the bit-upsets in combinational logic.

There have also been studies that aim to find the probabilities of multiple errors caused due to a single particle strike. These studies are mostly based on the fact that, as technology scales, a single-particle strike can affect more than one drain of a transistor, resulting in multiple transients, which can then propagate to cause multiple bit upsets at the output of a circuit [14], [9], [10]. There are also studies [19], [20] that estimate the multiple bit-flip probability due to a single transient in the circuit and show strong bit correlations. However, their methodology is based on algorithms and approximate models for fault propagation, and the corresponding inaccuracies reduce the confidence in their conclusions. In [21], a fault-injection experiment is conducted on a Verilog model of an embedded microprocessor and they conclude that multiple bit errors occur in more than 30% of the faulty cases. However, their Verilog model does not take into account the phenomenon of electrical masking. This can significantly vary the results of the estimated SER and the rate of multiple bit-flips. In [31], it is assumed that, a gate can possibly affect multiple outputs in its fanout cone, but this assumption is neither verified nor quantified. In [32], a transient fault simulator based on pulse and delay models is built. Their results indicate that multiple bit-flips range from 0.9% to 8.8% of the injected faults and conclude that a single-bit flip model “may not” be adequate. However, they fail to consider the phenomenon of electrical masking and also do not inject faults at the internal nodes of logic gates. In [33], the authors conclude that nearly 17% of faults in combinational logic lead to multiple bit errors. However, their analysis is based on gate level models of the designs with timing delays, which is again an approximate methodology.

In order to increase the confidence in any conclusions about the likelihood of multiple bit flips in logic circuits, it is thus essential that the estimation technique be as accurate as possible. In order to improve the accuracy, we use a Monte Carlo scheme combined with post-layout circuit simulations in SPICE. Since we perform SPICE simulations without making any simplifying assumptions (such as off-path logic values, delay models etc.), all the masking phenomena in logic circuits are taken into account, thereby increasing the confidence in the conclusions of our experiments. There are performance issues, but our results indicate that, with the use of parallel processing, non-trivial circuits can be analyzed in a reasonable amount of time.

III. METHODOLOGY

The overall idea of our experiment is depicted in Fig. I. Suppose that a single particle strike in a logic circuit results in a single glitch or a transient. This can potentially propagate to multiple outputs and cause multiple bits to flip, if it overcomes the three masking phenomena described in Section II. We intend to calculate the following conditional probability of multiple bit-flips:

\[
P(Multiple \ bit \ flips \mid Single \ bit \ flips)\]

as a result of a single transient caused by a particle strike.

Suppose that the total number of cases in which at least one bit flips is \(N\) and of these, the number of cases in which multiple bits have flipped is \(N_m\), then we can estimate the conditional probability, say, \(\theta\) by the estimator

\[
\theta_N = \frac{N_m}{N}
\]

The standard error in this estimate can itself be approximated
\[ \sigma_N = \sqrt{\frac{\theta_N - \theta^2_N}{N - 1}} \]  

so that, with 95\% confidence, the actual value of \( \theta \) lies in the interval \( [\theta_N - 2\sigma_N, \theta_N + 2\sigma_N] \). In our experiments, we continue generating samples until the standard error is reduced to less than 10\% of the value of the estimate. The quantity \( \theta \) is calculated for several test circuits. The overall flow of our methodology is depicted in Fig. 2.

Figure 1. Experimental setup

Figure 2. Experimental Methodology

A reference base is generated by first running an RTL simulation of the test circuit using a representative test-bench. The test circuit is then implemented to layout using synthesis tools, and the post-layout circuit netlist is extracted (with parasitic capacitances). Sample circuit simulation netlists are then generated from the post layout netlist with a glitch injected at a random gate, and at a random point in time. The inputs to the sample circuit simulation netlist are generated by using the corresponding values from the reference base simulation for the clock cycles corresponding to the sample time. The results of the sample circuit simulation are compared with the reference outputs from the reference base RTL simulation to check for bit-flips. Results of several such sample simulations are tabulated to calculate an estimate for \( \theta \).

A. Reference base generation

As shown in Fig. 2, we start with a test circuit which is described in RTL (VHDL or Verilog) together with a reference test-bench. This RTL description is then implemented to layout using synthesis tool (Synopsys Design Compiler [34]) and place-and-route tool (Cadence SoC Encounter [35]). The post layout Verilog netlist is then simulated (with the reference test-bench) using the ModelSim [36] simulator and the circuit inputs, outputs and flip-flop contents are recorded at every clock cycle. These will be used as a reference base for generating the sample circuit simulations, as well as for gathering bit-flip statistics.

B. Glitch injection

When a high energy particle strikes a silicon substrate, the amount of charge that it deposits, depends on the energy of the particle and the node capacitance. The energy of the particle can vary between 10MeV to 100MeV [15]. The deposited charge determines the magnitude of the transient current generated at the node. A particle strike is most widely represented as a current source that is injected at the drain of a transistor [37], [38]. Experiments conducted in [15] indicate that, for a 130nm PMOS transistor, a particle of 10MeV energy can generate a transient current of about 1.8mA. The transient current is mostly modeled as a double exponential pulse [37]:

\[ I(t) = \frac{Q}{\tau_\alpha - \tau_\beta} (e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \]  

where, Q is the deposited charge, \( \tau_\alpha \) and \( \tau_\beta \) are time constants that depend on process parameters.

Based on the data reported in [8], [15], scaled to our 180nm technology, we use the double exponential glitch model shown in Fig. 3. A fixed glitch is used in our experiments, though in reality, the glitch magnitude and decay time depend on the particle energy, location of the particle strike, the node capacitance etc. [15].
fault-injected circuit simulation are measured and recorded. SPICE simulation. In the (i+1)th simulation in this clock cycle are exactly reproduced in the netlist are initialized at the positive edge of the selected clock cycle. The following clock cycle (i-th cycle is just for completeness. This is depicted in Fig. 4.

C. Sample circuit simulation

The post-layout SPICE netlist of the test circuit is the template from which sample simulation decks are generated. To generate a sample simulation deck, we pick a random drain (d) of a transistor in the design at which the glitch will be injected. The probability of a drain being affected by a particle strike is assumed to be proportional to its area. We then select a random clock cycle (t) from the RTL reference base, and introduce the glitch at a random time instant (k) in the selected clock cycle.

Thus, a sample simulation deck is generated using three random numbers, which are generated using uniform sampling from a single seed, so that the results are reproducible. This process is followed till several simulation decks are generated with different (d,t,k) values and are simulated using the Ngspice circuit simulator [39].

The SPICE simulation is run for two and a half clock cycles, of which the first half cycle is for initialization, the following half-cycle is for glitch insertion, the next half-cycle is for monitoring the stabilized flip-flop values and the last half-cycle is just for completeness. This is depicted in Fig. 4.

D. Estimation of multiple bit flip probability

The expected values from the RTL reference simulation are compared with those obtained from the fault-injected SPICE simulation. A table of the resulting difference between the two values is created, in which a '1' indicates that the fault-injection resulted in a bit flip and a '0' indicates that the bit did not flip. The cases which do not have any bit flip are not of interest to us. We calculate an estimate for the conditional probability \( \theta \) and the standard error as indicated in Eq. (1) and Eq. (2) respectively. Our algorithm is said to have converged when the standard error is within 10% of the estimate. The total number of simulations run for each circuit varies, depending on how long it takes for the standard error to become small enough.

IV. Results

Our experiments are run in parallel on a high performance computing facility, utilizing up to a maximum of 200 cores. A maximum of 8 test-circuits with thousands of sample decks for each circuit could be simulated in parallel. The time taken to generate results for the largest circuit was nearly 2 days. The number of cores used for simulations is based on the circuit size, availability of cores and the time taken for each simulation. The glitch injection experiments are performed on the ISCAS’85 benchmark circuits and a few other example circuits. Flip-flops are added to all the inputs and outputs of the combinational logic circuits. The clock frequency for each circuit is set to the maximum operable frequency of the post-layout netlist, which is determined by post-layout timing analysis. The clock frequency ranges from 90MHz to 125MHz across all the circuits, except for the 3:8 decoder, which was simulated at 1GHz.

In Table I we report the estimates for \( \theta \) for all the test-circuits. The reported value is the minimum of the values obtained in the 95% confidence interval. We observe that \( \theta \) ranges from 0.01% up to as high as 31%. Also, the value of \( \theta \) is quite significant in a majority of the circuits. For a particular circuit, the value of \( \theta \) seems to depend on various factors such as the structure of the circuit itself, the presence of balanced paths, logic depth, the kind of logic gates used and the input combinations. This needs further study. However, it is clear that for most circuits, a single bit-flip model is not an adequate fault model for soft errors, if realistic estimates of reliability are to be obtained. Further, these observations are based on detailed post-layout circuit simulations without any simplifying assumptions (other than the glitch injection itself, which is assumed to be uniform across the circuit, and is assumed to affect a single drain). Thus, we have a high degree of confidence in the conclusions.

Although we report results for designs at 180nm technology, we expect that \( \theta \) is likely to increase with technology scaling as indicated in [22]. This is due to the possibility of a single strike affecting multiple nearby gates resulting in multiple transients.
Hence, a multiple bit-flip fault model for soft errors is likely to be necessary at lower technology nodes as well.

V. CONCLUSIONS

In this paper, we have demonstrated that a single bit-flip model is not adequate to model soft-errors in a logic circuit. We use Monte-Carlo sampling with detailed post-layout circuit simulations to estimate the conditional probability that multiple bits flip given that a single bit has flipped. This conditional probability is estimated for a variety of test-circuits, and significant values up to as high as 0.31 (for a multiplier) are observed. A wide variation is seen across the test-circuits, indicating that this probability depends on the structure and logic functionality of the individual circuits. However, the broad conclusion is that, multiple bit-flips must necessarily be considered in order to obtain a realistic fault model for soft errors in logic circuits.

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