Investigate on the Mechanism of HfO$_2$/Si$_{0.7}$Ge$_{0.3}$ Interface Passivation Based on Low-Temperature Ozone Oxidation and Si-Cap Methods

Qide Yao $^{1,2}$*, Xueli Ma $^{2,*}$, Hanxiang Wang $^{1,2}$, Yanrong Wang $^{1,*}$, Guilei Wang $^{2,*}$, Jing Zhang $^1$, Wenkai Liu $^1$, Xiaolei Wang $^2$, Jiang Yan $^1$, Yongliang Li $^{2,*}$ and Wenwu Wang $^2$

$^1$ School of Information Science and Technology, North China University of Technology, Beijing 100144, China; yaoqide@ime.ac.cn (Q.Y.); wanghanxiang@ime.ac.cn (H.W.); zhangji@ncut.edu.cn (J.Z.); liuweik@ncut.edu.cn (W.L.); yanjiang@ncut.edu.cn (J.Y.)

$^2$ Integrated Circuit Advanced Process Center, Institute of Microelectronics, Chinese Academy of Science, Beijing 100029, China; wangguilei@ime.ac.cn (G.W.); wangxiaolei@ime.ac.cn (X.W.); wangwenwu@ime.ac.cn (W.W.)

* Correspondence: maxuqile@ime.ac.cn (X.M.); wangyanrong@ncut.edu.cn (Y.W.); liyongliang@ime.ac.cn (Y.L.)

Abstract: The interface passivation of the HfO$_2$/Si$_{0.7}$Ge$_{0.3}$ stack is systematically investigated based on low-temperature ozone oxidation and Si-cap methods. Compared with the Al$_2$O$_3$/Si$_{0.7}$Ge$_{0.3}$ stack, the dispersive feature and interface state density ($D_{it}$) of the HfO$_2$/Si$_{0.7}$Ge$_{0.3}$ stack MOS (Metal-Oxide-Semiconductor) capacitor under ozone direct oxidation (pre-O sample) increases obviously. This is because the tiny amounts of GeO$_2$ in the formed layer are more likely to diffuse into HfO$_2$ and cause the HfO$_2$/Si$_{0.7}$Ge$_{0.3}$ interface to deteriorate. Moreover, a post-HfO$_2$-deposition (post-O) ozone indirect oxidation is proposed for the HfO$_2$/Si$_{0.7}$Ge$_{0.3}$ stack; it is found that compared with the pre-O sample, the $D_{it}$ of the post-O sample decreases by about 50% due to less GeO$_2$ available in the interface. This is because the amount of oxygen atoms reaching the interface of HfO$_2$/Si$_{0.7}$Ge$_{0.3}$ decreases and the thickness of IL in the post-O sample also decreases. To further reduce the $D_{it}$ of the HfO$_2$/Si$_{0.7}$Ge$_{0.3}$ interface, a Si-cap passivation with the optimal thickness of 1 nm is developed and an excellent HfO$_2$/Si$_{0.7}$Ge$_{0.3}$ interface with $D_{it}$ of 1.53 $\times$ $10^{11}$ eV$^{-1}$cm$^{-2}$@E$-E_c$ = 0.36 eV is attained. After detailed analysis of the chemical structure of the HfO$_2$/IL/Si-cap/Si$_{0.7}$Ge$_{0.3}$ using X-ray photoelectron spectroscopy (XPS), it is confirmed that the excellent HfO$_2$/Si$_{0.7}$Ge$_{0.3}$ interface is realized by preventing the formation of Hf-silicate/Hf-germanate and Si oxide originating from the reaction between HfO$_2$ and Si$_{0.7}$Ge$_{0.3}$ substrate.

Keywords: HfO$_2$/Si$_{0.7}$Ge$_{0.3}$ gate stack; ozone oxidation; Si-cap; interface state density; passivation

1. Introduction

High-mobility channel materials and novel device architectures, such as FinFETs (Fin Field-Effect Transistor) and nanowire FETs, are proposed to address the demand for scaling CMOS (Complementary Metal-Oxide-Semiconductor) technology [1,2]. In contrast to other potential materials, such as germanium (Ge) or III–V materials, silicon germanium (SiGe) is considered the most promising channel material for PMOS due to its tunability of band gaps and high hole mobility [3]. However, one of the main challenges in integrating SiGe into the novel devices is obtaining a high-quality interlayer (IL) between high-k gate oxide and SiGe substrate.

To control the interface quality, many methods have been extensively explored, such as plasma (N$_2$ or NH$_3$) nitridation passivation [4,5], sulfur passivation [6], thermal oxidation [7,8], low-temperature ozone passivation [9–12] and Si-cap passivation [13]. Among them, low-temperature ozone passivation with low thermal budget and Si-cap passivation with excellent properties of interface are considered the most promising passivation methods. For example, the interface state density ($D_{it}$) of 2.2 $\times$ $10^{12}$ eV$^{-1}$cm$^{-2}$
is attained by using a low-temperature ozone oxidation to passivate the interface of Al2O3/Si0.7Ge0.3[11], and the Df of 2 × 10^{11} \text{eV}^{-1}\text{cm}^{-2} for the interface of HfO2/Si0.8/Ge0.2 is realized by using a Si-cap passivation method [14]. However, the technique and mechanism of interface passivation of the HfO2/SiGe via low-temperature ozone oxidation or Si-cap method still needs further investigation.

In this paper, we fabricated HfO2/IL/Si0.7Ge0.3 gate stacks MOS capacitors by utilizing low-temperature ozone oxidation and Si cap passivation methods. We carefully compared their electrical properties, and the chemical structure of HfO2/IL/SiGe gate stacks. It is found that the post-HfO2-deposition (post-O) ozone indirect oxidation is a better choice than a step-by-step procedure (pre-O) method in terms of Df reduction. More importantly, the optimal Si cap method can realize a lower Df of 1.53 × 10^{11} \text{eV}^{-1}\text{cm}^{-2} @ E – E_c = 0.36 \text{eV} by preventing the formation of Hf-silicate/Hf-germanate and Si oxide originating from the reaction between HfO2 and Si0.7Ge0.3 substrate.

2. Materials and Methods

After standard HF-last cleaning, the 30 nm Si0.7Ge0.3 layer was epitaxially grown in a reduced pressure chemical vapor deposition system (ASM E2000 plus, Amsterdam, The Netherlands) on an 8-inch Si substrate. The low-temperature ozone passivation or Si-cap passivation was employed to passivate the interface of HfO2/Si0.7Ge0.3. For low-temperature ozone passivation samples, the ozone oxidation can occur on the Si0.7Ge0.3 surface directly (step-by-step procedure (pre-O)) or post HfO2 deposition (post-O). The ozone oxidation was carried out in 10% O3/O2 mixture ambience with the pressure of 3.1 Torr in an atomic-layer-deposition (ALD) chamber (Beneq TFS 200 system, Espoo, Finland). The temperature of the ozone oxidation was 300 °C. For Si-cap passivation, a Si-cap layer was in situ formed on the epitaxial Si0.7Ge0.3 layer in the same chamber. After the passivation treatment, the W/TiN or W/TiN/HfO2 gate stack was deposited as the gate stack of MOS capacitors. Finally, W/TiN/HfO2/IL/Si0.7Ge0.3 MOS capacitors were annealed in the forming gas (10% H2, 90% N2) at 350 °C for 30 min.

The chemical structures of the HfO2/IL/Si0.7Ge0.3 stacks were studied by X-ray photoelectron spectroscopy (XPS), which was carried out in a Thermo Scientific ESCALAB 250xi (Waltham, MA, USA) system with a photon energy of 1486.7 eV (Al Kα source). The photoelectron emission take-off angle was 90° relative to the sample surface and the pass energy was 15 eV. Moreover, TEM (Transmission Electron Microscope) and EDX (Energy Dispersive X-Ray Spectroscopy) Mapping analysis were performed by using FEI Talos F200X (Hillsboro, MI, USA) to verify the gate stack lattice structure and element content. Multi-frequency capacitance-voltage (C-V) along with conductance-voltage (G-V) measurements were measured using a Keysight 4990 A (Santa Rosa, CA, USA), and leakage-voltage (I-V) was measured using an Agilent B-1500 semiconductor analyzer.

3. Results and Discussion

3.1. Low-Temperature Ozone Oxidation Passivation of HfO2/Si0.7Ge0.3 Interface

In our previous work, the low-temperature ozone oxidation passivation method has been studied in detail based on Al2O3/Si0.7Ge0.3 gate stacks. It was found that oxidation time played an important role to obtain a high-quality interlayer (IL) and should be at least 5 minutes. Otherwise, the unoxidized Ge atoms would be trapped in the IL, causing the IL as well as the relevant electrical properties to deteriorate. Moreover, increasing oxidation time would result in an increase in the ratio of Si^{4+} to Si^{3+} of the oxide interlayer, which can help decrease the Df [15]. Thus, we chose 30 min as the oxidation time, which has proven to be an optimal experimental condition, to passivate the HfO2/Si0.7Ge0.3 interface in this work.

Figure 1a,b depicts the multi-frequency (1 kHz to 1 MHz) C-V characteristics of W/TiN/Al2O3/IL/Si0.7Ge0.3 (Al2O3 sample) and W/TiN/HfO2/IL/Si0.7Ge0.3 (HfO2-pre-O sample) MOS capacitors treated with 30 min ozone direct oxidation, respectively. The flat band voltages (Vfb) are also shown in the figures. The frequency dispersion features
of the C–V curves observed at gate biases smaller than the \( V_{fb} \), are caused by trapping and de-trapping of holes at traps with energies between approximately mid-gap and the Si\(_{0.7}\)Ge\(_{0.3}\) valence band edge, corresponding to the depletion of the Si\(_{0.7}\)Ge\(_{0.3}\) substrate. Comparing Figure 1b with Figure 1a, it is observed that the dispersion feature increases considerably. The energy distributions of the interface state density (\( D_{it} \)) were estimated using the conductance method [16], and given in their respective inset in Figure 1. We can see that both of the \( D_{it} \) of the two samples decreases along with SiGe band gap energy and the maximum \( D_{it} \) values appear near the valence band edge (\( E_v \)). However, the maximum value increases from \( 3.96 \times 10^{12} \text{eV}^{-1}\text{cm}^{-2} \) for the Al\(_2\)O\(_3\) sample to \( 2.67 \times 10^{13} \text{eV}^{-1}\text{cm}^{-2} \) for the HfO\(_2\)-pre-O sample. According to our previous work [17], it is known that for 300 °C/30 min ozone oxidation, about 54% of the Ge atoms of the outermost atomic layer of Si\(_{0.7}\)Ge\(_{0.3}\) can be oxidized in the initial stage of oxidation. No more Ge atoms would take part in the oxidation process as the oxidation time increases. The GeO\(_x\) and SiO\(_x\) thickness of the formed oxide layer are estimated to be 0.15 nm and 0.72 nm, respectively. Compared with Al\(_2\)O\(_3\), GeO\(_x\) is more likely to diffuse into HfO\(_2\) and cause the HfO\(_2\)/SiGe interface to deteriorate [18]. Therefore, the increased \( D_{it} \) of the HfO\(_2\)-pre-O sample can be attributed to tiny amounts of GeO\(_x\) in the formed oxide layer.

![Figure 1](image-url)

**Figure 1.** Multi-frequency C-V characteristics of (a) Al\(_2\)O\(_3\) sample (b) HfO\(_2\)-pre-O sample with 30 min oxidation time (direct). The insets are their respective energy distributions of \( D_{it} \).

Figure 2 depicts the multi-frequency (1 kHz to 1 MHz) C-V characteristics of W/TiN/HfO\(_2\)/IL/Si\(_{0.7}\)Ge\(_{0.3}\) (HfO\(_2\)-post-O sample) MOS capacitor treated with 30 min ozone indirect oxidation, in which the ozone oxidation was carried out after the deposition of HfO\(_2\). The corresponding energy distributions of \( D_{it} \) is also given in the inset. Compared with Figure 1b, an obvious improvement in the frequency dispersion feature is observed, and the \( D_{it} \) value decreases by about 50%. We infer that the improvement may arise from the following two factors. First, due to the barrier effect of the HfO\(_2\) layer on the diffusion of the oxidizer, the amount of oxygen atoms reaching the interface becomes fewer. Because silicon oxidation is more favorable than germanium oxidation in view of thermodynamic considerations [19], germanium atoms are hardly oxidized in this case. Therefore, almost no GeO\(_x\) would diffuse into HfO\(_2\) layer. In addition, the IL thickness of the HfO\(_2\)-post-O sample is smaller than that of the HfO\(_2\)-pre-O sample, which means the amounts of the Ge atoms accumulating at the IL/SiGe interface decrease accordingly. The experimental results prove that the post-O method is a promising technology to realize an HfO\(_2\)/IL/SiGe gate stack with small \( D_{it} \).
The Al$_2$O$_3$ sample, HfO$_2$-pre-O sample and HfO$_2$-post-O sample were compared on capacitance equivalent oxide thickness (CET) at $-1.5$ V bias voltage in accumulation. The CETs of each are 2.28 nm, 1.5 nm and 1.37 nm respectively. Comparing the Al$_2$O$_3$ sample with the HfO$_2$, the CET of the Al$_2$O$_3$ sample is bigger. The HfO$_2$-post-O sample decreased the CET, compared to the HfO$_2$-pre-O sample. This is supposed to be related to the diffusion of GeO$_x$. In general, the diffusion of GeO$_x$ is less in Al$_2$O$_3$ and HfO$_2$-post-O. Using the post-O method can limit the diffusion of GeO$_x$ in HfO$_2$. The diffusion of GeO$_x$ affects not only the CET but also the leakage current.

Figure 3 shows the gate Leakage of the Al$_2$O$_3$ sample, HfO$_2$-pre-O sample and HfO$_2$-post-O sample. Because GeO$_x$ is not easily diffused in Al$_2$O$_3$, the leakage current is minimal for the Al$_2$O$_3$ sample. Comparing with the HfO$_2$-pre-O sample, the leakage current HfO$_2$-post-O sample can be reduced by an order of magnitude.
3.2. Si-Cap Passivation of HfO$_2$/Si$_{0.7}$Ge$_{0.3}$ Interface

To further reduce the $D_{hi}$ of the HfO$_2$/Si$_{0.7}$Ge$_{0.3}$ interface, Si-cap passivation is in situ performed on the Si$_{0.7}$Ge$_{0.3}$ layer with different thicknesses. It is found that if the Si cap thickness is larger than or equal to 2 nm, there is a step observed in its C-V curve because a second channel is formed in the Si cap layer. This can be avoided by further thinning of the Si cap layer to 1 nm. Moreover, multi-frequency C-V curves (1 kHz to 1 MHz) of the W/TiN/HfO$_2$/IL/Si-cap/Si$_{0.7}$Ge$_{0.3}$ MOS capacitor with 1 nm Si-cap are measured and shown in Figure 3. It is worthy to note that the frequency dispersive feature is obviously improved compared with the above ozone passivation. However, the CET of the Si-cap sample from Figure 4 may be inaccurate due to the large gate leakage in the accumulation region. In addition, it can be seen that the carriers are mainly confined in the Si$_{0.7}$Ge$_{0.3}$ layer under this optimal Si-cap thickness due to its large valance band offset. For quantitative analysis, the $D_{hi}$ of $1.53 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ @ E$-E_v = 0.36$ eV is attained by using the conductance method. Meanwhile, HRTEM, Si and Ge element EDX mapping of the W/TiN/HfO$_2$/IL/Si-cap/Si$_{0.7}$Ge$_{0.3}$ MOS capacitor with 1nm Si-cap is also implemented and shown in Figure 5. It is found that there is a ~0.6 nm Si capping on the Si$_{0.7}$Ge$_{0.3}$ with a smooth and high-quality interfacial layer. The reduction of Si cap thickness of 0.4 nm is due to the oxidation of Si cap layer in the process of MOS capacitor fabrication. Therefore, 1-nm Si-cap in situ epitaxial grown is chosen as the optimal Si-cap thickness.

![Figure 4](image_url)

**Figure 4.** Multi-frequency C-V characteristic of W/TiN/HfO$_2$/IL/Si-cap/Si$_{0.7}$Ge$_{0.3}$ MOS capacitor with 1 nm Si-cap.

![Figure 5](image_url)

**Figure 5.** (a) HRTEM, (b) Ge, and (c) Si element EDX mapping of the W/TiN/HfO$_2$/IL/Si-cap/Si$_{0.7}$Ge$_{0.3}$ MOS capacitor with 1 nm Si-cap.
For the purpose of investigating the chemical structure of the HfO$_2$/IL/Si-cap/Si$_{0.7}$Ge$_{0.3}$ gate stack (Si-cap sample), X-ray photoelectron spectroscopy (XPS) technology is implemented. The chemical structure of the HfO$_2$/Si$_{0.7}$Ge$_{0.3}$ gate stack (SiGe sample), in which HfO$_2$ is deposited on Si$_{0.7}$Ge$_{0.3}$ directly, is also analyzed as a control sample. Gaussian-Lorentzian line shapes are used for deconvolution of all the spectra after standard Shirley background subtraction [20]. Figure 6a,b shows the Hf 4f core-level spectra of the Si-cap sample and SiGe sample, respectively. The spectra are both fitted with two component peaks. For the Si-cap sample (shown in Figure 6a), the Hf 4f spectrum consists of a main component at 16.8 eV related to the Hf-O bands in HfO$_2$, and a second component shifted by ~0.9 eV to higher binding energy, which is from the Hf-O-Si and/or Hf-O-Ge bonds. Because the electro-negativities of the Hf second neighbors (i.e., Si and Ge) are similar, it is difficult to distinguish the two contributions of Hf-O-Si and Hf-O-Ge bonds by XPS. It is worth noting that for the SiGe sample (shown in Figure 6b), the areal intensity of Hf-O-Si/Hf-O-Ge is much more than that of Hf-O. This suggests that a large portion of HfO$_2$ would react with SiGe to form Hf-silicate/Hf-germanate during the HfO$_2$ ALD deposition process. In addition, no feature of lower banding energy (14.3 eV–14.8 eV) is detected, indicating that no metallic Hf-Si and/or Hf-Ge are formed in the two samples.

![Figure 6](image_url)

**Figure 6.** The fitted Hf 4f core-level spectra of (a) Si-cap sample and (b) SiGe sample. The blue and red dot lines denote the Hf 4f photoelectron from Hf-O-Si and/or Hf-O-Ge bonds and Hf-O bonds in HfO$_2$, respectively.

Figure 7a,b shows the Si 2p core-level spectra of the Si-cap sample and the SiGe sample, respectively. The spectra are decomposed into four component peaks i.e., Si 2p photoelectron from SiGe (~99.7 eV), SiO$_x$ (~101.2 eV), HfSiO (~102.8 eV), and SiO$_2$ (~103.9 eV). For the Si-cap sample (shown in Figure 7a), the high-binding energy shoulder (101 eV–105 eV) contains few amounts of Si oxide (SiO$_x$ and SiO$_2$) and Hf-silicate (HfSiO). When compared with the Si-cap sample, an obvious increase in the areal intensity of the high-binding energy shoulder (101 eV–105 eV) can be observed for the SiGe sample, and there is no peak corresponding SiO$_x$. Figure 8a,b shows the O 1s core-level spectra of the SiGe sample and Si-cap sample, respectively. The spectra are fitted by the O 1s of SiO$_x$ (~532.8 eV), HfSiO (~532.08 eV) and HfO$_2$ (~531 eV). We can see that the O 1s photoelectron mainly originates from HfO$_2$ for the Si-cap sample, while that of the SiGe sample is mainly from SiO$_x$ and HfSiO. This is consistent with the previous discussions about Hf 4f and Si 2p spectra. All of these results indicate that the interfacial region of the HfO$_2$/SiGe (SiGe sample) is a composite of large amounts of HfSiO (and/or HfGeO) and Si oxide (SiO$_2$). In other words, Si-cap can prevent the formation of Hf-silicate/Hf-germanate and Si oxide originating from the reaction between HfO$_2$ and SiGe substrate, and obtain an excellent HfO$_2$/SiGe interface.
Figure 7. The fitted Si 2p core-level spectra of (a) Si-cap sample (b) SiGe sample. The red, blue, magenta, and green dot lines denote the Si 2p of SiGe, SiOₓ, HfSiO, and SiO₂, respectively.

Figure 8. The fitted O 1s core-level spectra of (a) Si-cap sample (b) SiGe sample. The red, blue, and magenta dot lines denote the O1s photoelectron from HfO₂, HfSiO, and SiOₓ, respectively.

4. Conclusions

In summary, the interface passivation of the HfO₂/Si₀.₇Ge₀.₃ stack is systematically investigated based on low-temperature ozone oxidation and Si-cap methods. Compared with pre-O method, the D₈ of the post-O sample decreases by about 50% due to less GeOₓ available in the IL layer. However, the D₈ of the HfO₂/IL/Si₀.₇Ge₀.₃ gate stack still has room to be further optimized. Finally, an excellent HfO₂/Si₀.₇Ge₀.₃ interface with a D₈ of 1.53 × 10¹¹ eV⁻¹cm⁻² @ E − E₀ = 0.36 eV is attained under the optimal Si cap method by preventing the formation of Hf-silicate/Hf-germanate and Si oxide from the reaction HfO₂ and Si₀.₇Ge₀.₃ substrate.

Author Contributions: Conceptualization, X.M., Y.W. and Y.L.; methodology, Q.Y., X.M., H.W., Y.W., G.W., J.Z., W.L., X.W., J.Y., Y.L. and W.W.; investigation, Q.Y., X.M., Y.W. and Y.L.; data curation, Q.Y., X.M., H.W., Y.W. and Y.L.; writing original draft preparation, Q.Y., X.M., Y.W. and Y.L.; writing review and editing, X.M., Y.W., Y.L. and J.Z.; supervision, J.Y., Y.L. and W.W.; project administration, Y.L. and W.W.; funding acquisition, W.W. All authors have read and agreed to the published version of the manuscript.
**Funding:** This research was funded in part by the Science and Technology Program of Beijing Municipal Science and Technology Commission (Grant no. Z20110004220001), in part by the CAS Pioneer Hundred Talents Program, in part by Beijing Municipal Natural Science Foundation (Grant no. 4202078), in part by National Natural Science Foundation of China (Grant no. 62074160) and in part by Scientific Research Startup Foundation of North China University of Technology.

**Institutional Review Board Statement:** Not applicable.

**Data Availability Statement:** Not applicable.

**Acknowledgments:** We thank the Integrated Circuit Advanced Process Center (ICAC) at the Institute of Microelectronics of the Chinese Academy of Sciences for the devices fabricated on their advanced 200 mm CMOS platform.

**Conflicts of Interest:** The authors declare no conflict of interest.

**References**

1. Mertens, H.; Ritzenthaler, R.; Arimura, H.; Franco, J.; Sebaai, F.; Hikavyy, B.A.; Pawlak, J.; Machkaoutsan, V.; Devriendt, K.; Tsvetanova, D.; et al. Si-cap-free SiGe p-Channel FinFETsand Gate-All-Around Transistors in a Replacement Metal Gate Process: Interface Trap Density Reduction and Performance Improvement by High-Pressure Deuterium Anneal. In Proceedings of the 2015 Symposium on VLSI Technology, Kyoto, Japan, 16–18 June 2015.

2. Hashemi, P.; Balakrishnan, K.; Engelmann, S.U.; Ott, J.A.; Khakifirooz, A.; Baraskar, A.; Hopstaken, M.; Newbury, J.S.; Chan, K.K.; Leobandung, E.; et al. First Demonstration of High-Ge-Content Strained-Si1-xGex(x = 0.5) on Insulator PMOS FinFETs with High Hole Mobility and Aggressively Scaled Fin Dimensions and Gate Lengths for High-Performance Applications. In Proceedings of the 2014 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2014.

3. Hashemi, P.; Ando, T.; Balakrishnan, K.; Bruley, J.; Engelmann, S.; Ott, J.A.; Narayanan, V.; Park, D.-G.; Mo, R.T.; and Leobandung, E. High-Mobility High-Ge-Content Si1-xGexOI PMOS FinFETs with Fin Formed Using 3D Germanium Condensation with Ge Fraction up to x ~0.7, Scaled EOT ~8.5Å and ~10nm Fin Width. In Proceedings of the 2015 Symposium on VLSI Circuits, Kyoto, Japan, 17–19 June 2015.

4. Han, J.; Zhang, R.; Osada, T.; Hata, M.; Takenaka, M.; Takagi, S. Impact of plasma post-nitridation on HfO2/Al2O3/SiGe gate stacks toward EOT scaling. Microelectron. Eng. 2013, 109, 266–269. [CrossRef]

5. Sardashti, K.; Hu, K.-T.; Tang, K.; Madisetti, S.; McIntyre, P.; Oktyabrsky, S.; Siddiqui, S.; Sahu, B.; Yoshida, N.; Kachian, J.; et al. Nitride passivation of the interface between high-k dielectrics and SiGe. Appl. Phys. Lett. 2016, 108, 011604. [CrossRef]

6. Sardashta, K.; Hua, K.T.; Tang, K.; Parka, S.; Kim, H.; Madisetti, S.; Oktyabrsky, S.; Siddiqui, S.; Sahu, B.; Yoshida, N.; et al. Sulfur passivation for the formation of Si-terminated Al2O3/SiGe(0 0 1) interfaces. Appl. Surf. Sci. 2016, 366, 455–463. [CrossRef]

7. Hellberg, P.-E.; Zhang, S.-L.; d’Heurle, F.M.; Petersso, C.S. Oxidation of silicon–germanium alloys. I. An experimental study. J. Appl. Phys. 1997, 82, 5773–5778.

8. Masanori, T.; Tatsuo, O.; Taizoh, S.; Miyao, M. Comprehensive study of low temperature (~<1000 °C) oxidation process in SiGe/SOI structures. Thin Solid Films 2008, 517, 251–253.

9. Song, Y.J.; Mheen, B.; Kang, J.Y.; Lee, Y.S.; Lee, N.E.; Kim, J.H.; Song, J.I.; Shim, K.-H. A low-temperature and high-quality radical-assisted oxidation process utilizing a remote ultraviolet ozone source for high-performance SiGe/Si MOSFETs. Semicond. Sci. Technol. 2004, 19, 792–797. [CrossRef]

10. Ando, T.; Hashemi, P.; Bruley, J.; Rozen, J.; Ogawa, Y.; Koswatta, S.; Chan, K.K.; Cartier, E.A.; Mo, R.; Narayanan, V. High Mobility High-Ge-Content SiGe PMOSFETs Using Al2O3/HfO2 Stacks with In-Situ O3 Treatment. IEEE Electron. Device Lett. 2017, 38, 303–305. [CrossRef]

11. Ma, X.L.; Xi, X.; Zhou, L.X.; Wang, X.L.; Zhang, J.; Zhao, C.; Yin, H.X.; Wang, W.W.; et al. Comprehensive Study and Design of High-k/SiGe Gate Stacks with Interface-Engineering by Ozone Oxidation. ECS J. Solid-State Sci. Technol 2019, 8, N100–N105. [CrossRef]

12. Ma, X.L.; Xiang, J.J.; Zhou, L.X.; Xu, H.; Wang, X.L.; Yang, H.; Li, Y.L.; Yin, H.X.; Wang, W.W. Understanding mechanisms impacting interface states of ozone-treated high-k/SiGe interfaces. Semicond. Sci. Technol. 2020, 35, 055018. [CrossRef]

13. Yeh, W.K.; Chen, Y.T.; Huang, F.S.; Hsu, C.W.; Chen, C.Y.; Fang, Y.K.; Gan, K.J.; Chen, P.Y. The Improvement of High-k/Metal Gate pMOSFET Performance and Reliability Using Optimized Si Cap/SiGe Channel Structure. IEEE Trans. Device Mater. Reliab. 2011, 11, 7–12. [CrossRef]

14. Tsutsui, G.; Durfee, C.; Wang, M.M.; Konar, A.; Wu, H.; Mochizuki, S.; Bao, R.Q.; Bedell, S.; Li, J.T.; Zhou, H.M.; et al. Leakage Aware Si/SiGe CMOS FinFET for Low Power Applications. In Proceedings of the 2008 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 18–22 June 2008.

15. Ma, X.L.; Zhou, L.X.; Xiang, J.J.; Yang, H.; Wang, X.L.; Li, Y.L.; Zhang, J.; Zhao, C.; Yin, H.X.; Wang, W.W.; et al. Identification of a suitable passivation route for high-k/SiGe interface based on ozone oxidation. Appl. Surf. Sci. 2019, 493, 478–484. [CrossRef]
16. Nicollian, E.H.; Brews, J.R. *MOS (Metal Oxide Semiconductor) Physics and Technology*; John Wiley & Sons Inc.: Hoboken, NJ, USA, 1982; p. 176.

17. Ma, X.L.; Wang, X.L.; Zhou, L.X.; Xu, H.; Zhang, Y.Y.; Duan, J.H.; Xiang, J.J.; Yang, H.; Li, J.J.; Li, Y.L.; et al. Experimental study of the ultrathin oxides on SiGe alloy formed by low-temperature ozone oxidation. *Mater. Sci. Semicond. Process.* 2020, 107, 104832. [CrossRef]

18. Gusev, E.P.; Shang, H.; Copel, M.; Gribelyuk, M.; D’Emic, C.; Kozlowski, P.; Zabel, T.; Gusev, E.P.; Shang, H.; Copel, M.; et al. Microstructure and thermal stability of HfO₂ gate dielectric deposited on Ge(100). *Appl. Phys. Lett.* 2004, 85, 2334. [CrossRef]

19. Chang, C.T.; Toriumi, A. Preferential Oxidation of Si in SiGe for Shaping Ge-Rich SiGe Gate Stacks. In Proceedings of the 2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 7–9 December 2015.

20. Shirley, D.A. High-Resolution X-ray Photoemission Spectrum of the Valence Bands of Gold. *Phys. Review B* 1972, 5, 4709. [CrossRef]