1 Abstract

A theoretical memory with limited processing power and internal connectivity at each element is proposed. This memory carries out parallel processing within itself to solve generic array problems. The applicability of this in-memory finest-grain massive SIMD approach is studied in some details. For an array of N items, it reduces the total instruction cycle count of universal operations such as insertion/deletion and match finding to ~ 1, local operations such as filtering and template matching to ~ local operation size, and global operations such as sum, finding global limit and sorting to ~√N instruction cycles. It eliminates most streaming activities for data processing purpose on the system bus. Yet it remains general-purposed, easy to use, pin compatible with conventional memory, and practical for implementation.

Keyword: SIMD processors; Parallel Processors; Memory Structures; Performance evaluation of algorithms and systems;

2 Introduction

In database processing [1], image processing [2], string-based context searching [3], or modeling [4], there are a lot simple parallel operations based on arrays, applying identical and repeated operations to identical and repeated data structures. In the current most common CPU/memory bus-sharing architectures [5][6][7][8], such array problems are solved by serial algorithms, in which data are shuffled frequently between the memory unit and the processing unit for the data processing purpose, to contribute to the bus bottle-neck problem [5][6][7][8]. Many solution based on parallelism [5][6][7][8] has been attempted on this problem.
Concurrent Processing Memory

The increase of bus width or caching ability, and the small-scale usage of SIMD inside CPU in the form of vector processor [5] only levitate the problem to certain degrees [5][6][7].

The current development of parallel processing focuses on two MIMD (multiple instrument multiple data) approaches, namely, the shared memory approach [5][8] and the cluster/grid approach [5][10], whose PEs (processing elements) are either CPUs or computers respectively. These two MIMD approaches have been standardized in software as OpenMP (Open Multi-Processing) [11] and MPI (Message Passing Interface) [12]. As a result, the current focus [13] of parallel processing is the scalability [5][8] of such MIMD systems, and software tools [13][14] to achieve, evaluate and fine-tune parallel programming. Another MIMD approach is to use many in-memory small functional units as PEs [15][16][17][18][19]. While MIMD approaches have achieved impressive results, the mapping of a particular application to the underline connection network [5][8] of PEs remains a general problem [13][20]. One particular issue is that large-scale array problems usually call for massive SIMD execution logically, but such SIMD requirement is not implemented in the most efficient manner by the underline MIMD architecture due to required communication overheads of dispatching, synchronization and data exchanges among relatively small number of PEs [21]. To improve efficiency for solving array problems using MIMD approaches, each PE can have enhanced SIMD capability [22][23], the PEs can be hardwired in a topology targeted at problem to be solved [5][8], each PE can have its cache fine-tuned to handle SIMD execution better [5][8][23], and etc. Manual tuning of software either on coding level or on compiler level is required to take advantage of such hardware specification [24]. But the result performances are usually still much worse than corresponding true massive SIMD executions due to structural difference between the array problems and the underline hardware & software. Another problem of the two prevailing MIMD approaches is that they do not solve the bus bottle-neck problem, because they still store data and instruction at separate location from execution, so that most data transferred on the system
bus are still for processing purpose. The bus bottleneck problem seems to call for in-memory processing [5].

Earliest attempts using massive SIMD (single instrument multiple data) approaches are enhanced version of vector-CPU in special and dedicated systems [25]. Our Human logic tends to formulate serial solutions because both induction and deduction are serial in nature. So SIMD is more likely to be used as special steps of predominantly serial solutions, and it is unlikely to be the foundation of a general-purposed computer system. In-memory SIMD approach using large-to-medium grain size [26][27][28][29] do not seem to have clear advantages over MIMD approach using large number of in-memory small function units, because the former has a reduced processing bandwidth than that of a conceptual SIMD execution of the targeted application [28], while the later is more flexible in usage. As a result, some of such SIMD approaches later evolved into mixed SIMD/MIMD approaches [28][29]. Due to their nontrivial programming need and control overheads, both approaches have compatibility issues with prevailing bus-sharing architectures and operating systems, which may be the reason why both have much less attention than the two prevailing MIMD approaches. So far, the only main-stream usage of pure in-memory massive SIMD is content addressable memory [30], whose success is due to (1) its specificity to a classic and ubiquitous array problem, (2) its distribution of processing power to fine-grain storage units, (3) its compatibility with prevailing bus-sharing architectures & operating systems, and (4) its trivial programming need and minimal control overheads. The design of a smart memory family—the concurrent processing memory [9], or simply CPM—is a theoretical attempt to extend the success of content addressable memory to in-memory massive SIMD architecture in general.

At this moment, silicon integration [32][33] has progressed rapidly in implementing Moore’s law [34], and the silicon industries has entered a new era of billions of transistors per chip [35]. With such a huge transistor budget recently available, it is a hot debate [36][37][38] to establish parallelism whether on instruction level [35], or on thread level [37], or on data level [38].
Among them, data level parallelism is simplest in both programmability and hardware construct [38], while its weakness is its specification for applications. With the advance in intranet speed and grid computing, a specific device such as an ultra-fast SQL engine can now be shared efficiently in a network by multiple tasks, which may create revived interest to use in-memory massive SIMD approach for solving large-scale real-time array problems. In-memory massive SIMD approach may now have a new life in a new era of silicon integration and grid computing.

3 The Concurrent Processing Memory

3.1 Architecture

Built upon the success of content addressable memory, and with silicon integration in mind, the design philosophy of CPM is to distribute limited and specific processing power to the smallest storage unit for its targeted application while maintain its compatibility with a traditional memory. Application specificity further means that the instruction set for each PE is limited to its targeted application(s) only, so that PE programming becomes trivial.

The basic rules for CPM, as shown in Figure 1, are:

**Rule 1.** A CPM is made of identical PEs (processing elements), each of which contains a fixed number of registers.

**Rule 2.** Each PE has at least one addressable register which can read from or write to an exclusive bus exclusively.

**Rule 3.** Each PE contains has a unique element address, but each PE is not aware of its own address, so that each PE exists in an identical environment.

**Rule 4.** Multiple PEs can be activated concurrently if each of their element addresses is: (1) no less than a start address, (2) no more than an end address, and (3) an integer increment starting from the start address.
Rule 5. Multiple activated PEs can read and execute a same instruction concurrently from a concurrent bus which broadcasts to all PEs.

Rule 6. Multiple activated PEs can identify themselves concurrently.

Rule 7. The neighboring PEs are connected so that an PE can read at least one register of each of its neighbors.

Rule 8. There is an extra external command pin to indicate that the address and data bus contains whether (1) address and data or (2) an instruction for the CPM when it is enabled.

As shown in Figure 1, a CPM has a control unit which controls every PE. The control unit has a dedicated line called enable line to enable each PE. It contains a general decoder to implement Rule 4 using those enable lines. In addition, each PE has a dedicated line called match line to the control unit, and positively asserts this line to identify itself for Rule 6. The control unit then uses either a priority encoder to enumerate the identified PEs, or a parallel counter to count the identified PEs. The control unit is in turn controlled by the system bus according to Rule 8.

Rule 1 and Rule 2 specify the functional backward compatibility with a conventional random access memory. Rule 3, Rule 4, Rule 5 and Rule 6 define SIMD concurrency. Rule 7 define connectivity. Rule 8 defines programming methodology.

All array items form a periodical pattern when they are saved continuously in a memory. By setting the carry number for Rule 4 as the memory size of each array item, Rule 4 allows the storing of each array item by a PE or multiple neighboring PEs, and the concurrent and instant operation upon multiple array items within an address range.

The concurrent and the exclusive operations can be independent of each other, so that while some addressable registers of one task is being operated on by concurrent operations, other addressable registers in the same CPM can be simultaneously prepared for other tasks by exclusive operations.
A CPM can be pin-compatible and function-compatible with a conventional random access memory in a bus-sharing environment [6][7]. When it is enabled, an address bit can be dedicated as the command pin of Rule 8. When this pin is false, the CPM behaves exactly like a conventional random access memory; otherwise, the content of the address and data bus is treated as instructions. Thus, a CPM is just a normal device in a bus-sharing system. To cope with large bandwidth disparity between inside and outside a chip [5][6][7], a CPM may have an internal micro-kernel [6][7] to translate instructions, cache instructions and data, make internal macro calls, and presents result using normal synchronization techniques [6]. The micro-kernel may also hide PE instruction set inside the memory, and expose application-oriented instruction set to the user of CPM. If the CPM has a higher execution rate than the system bus, its output also needs to be cached.

Except Rule 4, all of the above rules have mature usages, e.g., Rule 5 is the signature of SIMD approach in general [5], Rule 6 is used extensively in a content addressable memory [30], and Rule 8 is a common technique in programming devices using a bus [6]. Nor the above rules necessarily capture high-performance designs. The PE activation in Rule 4 seems too rigid. The connectivity in Rule 7 is perhaps the most crude and least efficient among existing types of PE connectivity [5][8]. But they may be the most practical ones for massive SIMD architectures specific for large-scale array problems. For an example, if PE activation is done by a dedicated processor, then the number of PE can be activated or deactivated for each instruction cycle is limited by the word width of the processor, thus not suitable for massive number of PEs, even though this approach is much more flexibility in programming and it is widely used in other SIMD and MIMD approaches. Instead, a general decoder implements Rule 4 in ~1 instruction cycles for any number of PEs. The set of rules of CPM capture the essence of a massive in-memory SIMD working in a traditional bus-sharing architecture, with identical PEs, minimal PE control overhead, simplest PE-to-PE relation, uniform PE-to-memory relation, and extreme specificity for its targeted application.
3.2 PE Capability

CPM is actually a family name comprising members in the order of PE complexity: (1) content movable memory, (2) content searchable memory, (3) content comparable memory, and (4) content computable memory. Except content computable memory, each type of CPM targets at a classic and ubiquitous array problem only. It is possible that a bus-sharing system contains multiple types of CPM, such as a content movable memory for memory management, and a content comparable memory as a SQL engine. The CPM of simpler PE construct is also simpler for implementation, and the complexity progress can be used as a roadmap to introduce massive SIMD constructs into a modern bus-sharing system.

As a massive SIMD approach, the silicon budget of each PE needs to be controlled carefully. The construct of each PE is demonstrated on logic design level [39] in this paper.

3.3 General Decoder

The ability to instantly activate PEs according to Rule 4 is crucial for the CPM, which is provided by a general decoder comprising (1) a carry-pattern generator, (2) a parallel shifter, (3) an all-line decoder, and (4) an AND gate array that combines the corresponding bit outputs from the parallel shifter and the all-line decoder.

A carry-pattern generator inputs a carry number (which is the carry number input for the general decoder) and activates all of its bit outputs whose address corresponds to the increments of the carry number. For an example, a 3/8 carry-pattern inputs binary carry number (C[2] ... C[0]), and positively asserts bit outputs (D[7] ... D[0]) in the following manner:

Equation 3-1: \(D[0] = 1;\)

\[
\begin{align*}
D[1] &= !C[2] \ C[1] \ C[0]; \\
D[2] &= !C[2] \ C[1] \ !C[0] + D[1]; \\
D[3] &= !C[2] \ C[1] \ C[0] + D[1]; \\
D[4] &= C[2] \ !C[1] \ !C[0] + D[1] + D[2];
\end{align*}
\]
The above expression can be generalized for arbitrary number of inputs, and transformed into standard product-of-sum format using either K-map or Quine-McCluskey method [6], and the carry pattern generator can be constructed using corresponding two-level gates. The product-of-sum construct is chosen for expansibility, so that the addition of C[N] input bit appended !C[N] product term to all the existing expressions of (C[N-1] ... C[0]).

The outputs of the carry-pattern generator are shifted toward higher address by the amount of the start address to the general decoder, through a parallel shifter, which inputs a shift amount (S[M] ... S[0]), bit inputs (D[N] ... D[0]), and output bit inputs (H[N] ... H[0]) according to the following equation:

\[
\text{Equation 3-2: IF } A=>S: \quad H[A] = D[A - S]; \\
\text{ELSE:} \quad H[A] = 0; 
\]

Since shifting is accumulative, each S[j] bit input just shifts the bit inputs by the amount of \(2^j\) toward higher input number. For an example, a 3/8 parallel shifter is shown in Figure 2, which inputs a shift amount (S[2] S[1] S[0]), bit inputs (D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]), and output bit inputs (H[7] H[6] H[5] H[4] H[3] H[2] H[1] H[0]).

An all-line decoder activates all its bit outputs whose address is less than or equal to its input address, which is the end address to the general decoder in this case. Assuming the bit output is \(F[E, N]\), in which \(E = (E[N-1] ... E[0])\) denotes the address of the bit output and \(N\) denotes the bit width of the address, an all-line-decoder with address bit width of \((N+1)\) can be built from an all-line-decoder with address bit width of \(N\) using the following logic expression of \(F[E, N]\):

\[
\text{Equation 3-3: } F[0, 1] = 1; \\
\quad F[1, 1] = E[0]; 
\]
Concurrent Processing Memory

\[
F[(0E[N-1]...E[0]),N+1] = F[(E[N-1]...E[0]),N] + E[N];
\]
\[
F[(1E[N-1]...E[0]),N+1] = F[(E[N-1]...E[0]),N] * E[N];
\]

The circuit diagram of a 3/8 all-line decoder is shown in Figure 3.

The bit outputs of the parallel shifter are filtered through AND gates by the corresponding bit outputs of the all-line decoder, before becoming the bit outputs of the general decoder, as shown in Figure 4.

If the carry number is a constant of 1 for Rule 4, the general decoder can be simplified. The start address is input into a first all-line decoder whose outputs are negatively assertive, and the end address is input into a second all-line decoder whose outputs are positively assertive. The corresponding outputs from the two all-line decoders are AND-combined, before becoming the bit outputs of the general decoder.

4 Content Movable Memory

4.1 Construct and Basic Functionality

The structure of a content movable PE is shown in Figure 5. Each PE has only one addressable register, which can be read by its left and right neighboring PE. Each PE has an additional temporary register, whose content can be copied to the addressable register. A multiplexer selects the addressable register of either the left or the right neighbor, to copy to the temporary register. The concurrent bus has only two bits, one to select the output of the multiplexer, and the other to select which registers inside each PE to be copied. The content of a neighboring addressable register is first copied to the temporary register, then to the addressable register of the PE. Thus, the temporary register only needs to remember its content for one clock cycle and can be made of DRAM cell [6]. The copy operation is enabled by the enable line from the control unit. With the carry number to be a constant of 1 for Rule 4, the content of all the addressable registers within an address range can be moved concurrently.
in one of the two directions in ~1 instruction cycles. By performing a consecutive right and left content move of all used PEs, the contents of their addressable registers are refreshed locally, concurrently, and instantly. Thus, the addressable register in each PE can also be made of DRAM cells. With 2-gate overhead for each bit, and 4-gate overhead for each PE, a content movable memory has comparable density as a DRAM and comparable speed as a SRAM [6].

Content movable memory does not implement Rule 6 of CPM and each of its PE has no match line.

4.2 Usage

A content movable memory can be used to manage data object within itself. It can inserts, deletes, shrinks, enlarges, or moves data objects without overhead such as extensive copying [6][41], and side-effect such as memory fragmentation [6][41]. It may contain a hardware lookup table to refer each data object by an ID instead of actual address. It allows most efficient use of memory while levitates CPUs and operating systems from a lot of memory management tasks [6][7]. Content movable memory is aimed at replacing both SRAM and DRAM due to its memory management functionality and its overall speed and density.

Programming techniques are tied to memory management. Traditional computer languages require explicitly or implicitly defining the size of an object before using it, so that a compiler can allocate the space for the object in a conventional memory [6][41][42]. The improper size of objects is a major source of errors, such as value overflow [6], value underflow [6] and buffer overrun [6]; while always allocating very large size for safety wastes memory space and computation power. When using a conventional memory, such allocation and dellocation requirement is ubiquitous for all operating systems [41] and programming languages [42], either explicitly or implicitly. Such requirement favors procedural language [42] over functional language [42], because the latter tends to allocate most objects dynamically on heap [42], creating memory fragment problem. When using a content movable memory for programming,
the space allocated for a object can grow and shrink easily according to the need, which brings about the following advantages: (1) a variable will never go out of size, (2) an array is always dynamic, (3) a variable type only concerns the interpretation of the variable, e.g. only one type for integer and only one type for floating-point, and (4) functional language is favored over procedural language, because the former is not tied to implementation details, has better optimization potentials, and is more elegant by pursuing pure algorithm goal [42].

5 Content Searchable Memory

A content searchable memory is similar to a content addressable memory [30], provided that the content searchable memory has smallest grain for searching, and it has local connectivity between neighboring PEs according to Rule 7 of CPM, to remove length limit on the substring to search for, and alignment limit on the content to be searched.

5.1 Construct and Basic Functionality

The PE construct of a content searchable memory is shown in Figure 6. It contains one addressable register and one storage bit register. The concurrent bus sends to every PE:

- A mask, which masks the content of the addressable register of the PE.
- A datum, whose value is compared with the masked data at an equal comparator.
- A comparison code of either $=$ or $\neq$, which is matched against the output of the equal comparator, to become the comparison result bit. Using the datum and mask, more complicated comparison requirement, such as “do not care”, can also be achieved.
- A self code. When it is true, the comparison result bit is saved into the storage bit register. Otherwise, the storage bit register is true only of the comparison result bit is true and the storage bit register from the right neighboring PE is also true.

Assume a string to be searched is loaded in a content searchable memory. To find a substring: (1) The first character of the substring is matched against all addressable registers
with self code to be true. (2) The next character of the substring is matched against all addressable registers with self code to be false. After this step the bit storage of the previous character is reset to false. (3) After the last character of the substring is matched, a true storage bit indicates that it is the last character of the substring to be found.

Because most string consists of either 8-bit or 16-bit characters, and in the most popular 16-bit character set two bytes of each character have different formats [43], the addressable register should have byte size. The carry number is usually a constant of 1 for Rule 4, unless the content to be searched is structured, so as a look-up table.

5.2 Usage

Finding a substring from a large string is an extremely frequent operation which usually needs to be done in very high speed, such as web search. It logically calls for massive SIMD execution if the string to be searched is already in memory. When it is implemented by MIMD approaches, the algorithm is complicated, requiring pre-processing of the string to be searched for high speed applications [3]. In contrast, content searchable memory finds a substring from an original string by concurrently matches each character of the substring, and it only takes \( \sim M \) instruction cycles, in which \( M \) is the length of the substring. Thus, content searchable memory can vastly improve efficiency of string-based content searches.

5.3 Content Change

It is easy to add the PE construct of content movable memory into the PE construct of content searchable memory, to result in a CPM whose content can be searched concurrently and modified easily. Such combination can apply to other types of CPM.

6 Content Comparable Memory

A content comparable memory extends the functionality of a content searchable memory from value matching to value comparing.
6.1 Construct and Basic Functionality

The PE construct of content comparable memory is shown in Figure 7. It is very similar to the PE construct of content searchable memory shown in Figure 6. The concurrent bus sends to every PE:

- A mask, which masks the content of the addressable register of the PE.
- A datum, whose value is compared with the masked data at a value comparator.
- A comparison code of either $=$ or $\neq$ or $<$ or $>$ or $\leq$ or $\geq$, which is matched against the output of the value comparator in a match table, to become the comparison result bit.
- A select code bit, which selects value of either left or right neighboring storage bit register as the selected bit.
- A self code bit, which selects either the selected bit, or the NAND combination of the comparison result bit and the current value of the storage bit register, to input into the bit storage register.
- An update code bit, which is AND combined with the comparison result bit, to update the bit storage register with its input.

Any logic combination between the current values of the bit storage register and the comparison result bit can be constructed using a neighboring storage bit register which is not currently used. A false update code bit enables a condition execution. By transferring the value of storage bit register from one PE to another, and by allowing successive build-up of comparison results among neighboring PEs, a content comparable memory enables comparison using any logic combinations among fields of an array item to common values. For example, it is possible to let neighboring PEs holding one value for a $<$ comparison. For simplicity of discussion, the width of the addressable register is byte, the value to be compared is unsigned, and the neighboring PEs holding one value with significance decreasing from left to right. The comparing algorithm is the following:
Concurrent Processing Memory

1. Set the storage bit register of right-most PEs to true if the addressable register holds a value less than the least significant byte to be compared.

2. In the order of increased significance, (A) Set the storage bit register true if the addressable register holds a value less than the corresponding significant byte to be compared; (B) Save the storage bit register with the value of the storage bit register of the right neighbor if the addressable register holds a value equal the corresponding significant byte to be compared; (C) Reset the storage bit register of right PEs;

3. The leftmost PE of each value holds the result of < comparison.

6.2 Implement SQL

Comparing a field of all array items with one value is another extremely frequent operation which usually needs to be done in very high speed. Perhaps the most important such an application is relational database [1][44], which depends on such comparison to (1) define relations among different tables, and (2) characterize data within tables using a series of such comparison. Using traditional bus sharing architecture, the required instruction cycle for one such comparison equals the total count of array items. To make the speed of such comparison acceptable in real time, a database index [44] pre-sorts a database field. Even with the help of database index, the instruction cycles of such comparison is still ~ M \log(N) in which M is the average item count having the same value and N is the count of unique values in the database index [1]. Database index needs to be updated whenever the underline field changes, so a database index needs to be deleted before the field gets heavy updated, and then recreated afterward [44]. Things become much more difficult when multiple parties can update the database concurrently and the database needs to run continuously [1][44]. In contrast, a content comparable memory compares a field of all array items with one value concurrently in ~1 instruction cycles without any preprocessing. Array traversing usually follows a progressive increment of a field, so a content comparable memory can carry out such traversing effectively.
In worst cases the data within the content searchable memory can still be accessed serially. Thus, a content comparable memory can be used to implement SQL with vastly improved speed.

Rule 4 of CPM requires that each array item to be equal in size, so usually only addresses to a variable size field of large size can be stored in a content comparable memory; however the variable size field can be stored in a content searchable memory if quick content search capability is required.

6.3 Count for Statistics

By matching each section limit one-by-one, the histogram of M sections is constructed in \( \sim M \) instruction cycles, which provides base for statistical characterization of the array.

7 Content Computable Memory

A content computable memory is similar to content addressable processors [26] and associative processors [27] with local neighboring connectivity only. But content computable memory has more overall calculation power due to Rule 4 of CPM, even both SIMD approaches have comparable processing power on PE level. By processes all data related to each array item in each PE, such as all data related to one pixel in imaging processing, or all data related to one cell in modeling, each PE of content computable memory has minimal grain size for the target application.

7.1 Dimension

In a 1-D content computable memory, each PE has two neighbors of immediately higher or lower element addresses. In a 2-D content computable memory, each PE has four neighbors and PEs of a 2-D content computable memory forms a square lattice; the element address is partitioned into X and Y addresses which obeys Rule 4 of CPM independently. Except neighbor count, both types of content computable memory have identical PE construct.
7.2 PE Construct and Basic Functionality

A content computable memory PE with a bit-serial logic is shown in Figure 8. It has:

- Some data register, as 1st, 2nd, and etc data registers in Figure 8.
- A neighboring register, which can be read by its neighboring PEs.
- An operation register, which is involved in each operation.
- A match bit register, a status bit register and a carry bit register, shown as the squares marked by “M”, “S” and “C” respectively in Figure 8.

The concurrent bus sends a datum and an instruction to each PE. The instruction format for is “condition: operation [bit] register[bit]”, in which:

- One operand is the bit of the operation register at the first “[bit]” bit, which is selected by a multiplexer called bit multiplexer in Figure 8.
- The other operand is the bit of the “register” at the second “[bit]” bit, which is selected by a multiplexer called register multiplexer in Figure 8. The “register” could be any of its data registers, its neighboring register, or any of its neighbor's neighboring registers.
- The “[bit]” bit, the “register[bit]” bit, the status bit and the carry bit, together with their respective logic negation, are input into a multiplexer called condition multiplexer in Figure 8, whose bit output V is selected by part of the “condition” code. V is combined with the datum bit D on the concurrent bus, a “compare” code bit C of the “condition” code, and current value of the M bit register according to Equation 7-1, to result in a Boolean value B.

Equation 7-1: \[ B = M + C \ (V \ D + !V \ !D) + !C \ V; \]

- The “operation” decides which registers to write to. The Boolean value B can be saved into the match bit register. If B is true, the match bit register can be saved into (1) the status bit register, (2) the carry bit register, and (3) the “[bit]” bit. If B is true, the “[bit]” bit can be saved into the “register[bit]” bit.
The match bit register, the carry bit register, the logic gates and the condition multiplexer forms a bit-serial ALU, whose output is \( B \). Successive “condition” code forms an arbitrary logic expression of the “[bit]” bit, the “register[bit]” bit, the datum bit of the concurrent bus, and previous values of the match bit register and the carry bit register. The status bit register is intended for general usage, and it can be part of the ALU as well. Using the bit-serial ALU, logic and arithmetic operations based on arbitrary-wide word size, such as comparison, addition, subtraction and multiplication between the operation register and any other register, can be carried out. A content computable memory may contains a micro kernel \([6][7]\) to translate register-level instructions on the system bus into bit-serial instructions for PEs. The ALU output \( B \) also drives the match line of PE.

For simplicity of description of the following concurrent algorithms: (1) the operation registers of all the activated PEs are collectively referred to as the operation layer; (2) the neighboring registers of all the activated PEs are collectively referred to as the neighboring layer; (3) the neighboring layer of the PE whose element address is one less or one more than the activated PE is called the left layer or the right layer respectively; and (4) the neighboring layer of the PE whose \( Y \) element address is one less or one more than the activated PE is called the top layer or the bottom layer respectively. It is assumed that the values to be processed are always initially stored in the neighboring layer.

### 7.3 Local Operations

A special 1D vector of odd-number of items is used to describe the content of the operation layer. The center item describes the content originated from neighboring layer of the PE itself and is indexed as 0. The item left to the center item describes the content originated from the left layer and is indexed as -1. The item right to the center item describes the content originated from the right layer and is indexed as +1. So forth. For an example: (A) (1) denotes the content of the neighboring layer; (B) (1 0 0) denotes the content of the left layer; (C) (1 1 0) denotes the
content of adding the left layer to the neighboring layer. Two successive operations are additive if both of them use the operation layer accumulatively, such as:

Equation 7-2: \((1 1 0) = (1) + (1 0 0)\);

Mathematically, a + operation is defined as:

Equation 7-3: \(C \equiv A + B: C[i] = A[i] + B[i]\);

The + operation satisfies:

Equation 7-4: \(A + B = B + A\);
Equation 7-5: \((A + B) + C = A + (B + C)\);

When operation layer is copied to or exchanged with neighboring layer, the successive operations are no longer additive, such as a 3-point \((1 2 1)\) Gaussian averaging algorithm:

1. Copy neighboring layer to operation layer.
2. Add left layer to operation layer.
3. Copy operation layer to neighboring layer.
4. Add right layer to operation layer. The result is in operation layer.

In the above algorithm, without Step 3, Step 4 is also additive to Step 1 and 2, and the algorithm result is \((1 1 1)\). When the result of a first operation \(A\) undergoes a second operation \(B\), the overall operation \(C\) is expressed mathematically as:

Equation 7-6: \(C \equiv A \# B: C[i] = \sum_j(A[i+j] B[i-j])\);

The \# operation satisfies:

Equation 7-7: \(A \# B = B \# A\);
Equation 7-8: \((A \# B) \# C = A \# (B \# C)\);

The \# and + operations satisfy:

Equation 7-9: \((A + B) \# C = (A \# B) + (A \# C)\);

Thus, the above 3-point \((1 2 1)\) Gaussian averaging algorithm is expressed as:

Equation 7-10: \((1 2 1) = (1 1 0) \# (0 1 1)\);

And a 5-point Gaussian averaging requiring 6 instruction cycles is expressed as:
Concurrent Processing Memory

Equation 7-11:  \((1 2 4 2 1) = (1 1 1) \# (1 1 1) + (1)\);

This concept is extendable to 2D local operations, such as a 9-point Gaussian averaging which requires 8 instruction cycles:

\[
\begin{pmatrix}
1 & 2 & 1 \\
2 & 4 & 2 \\
1 & 2 & 1 \\
\end{pmatrix}
= \begin{pmatrix}
0 \\
0 & 1 \\
1 \\
\end{pmatrix} \# \begin{pmatrix}
0 & 1 & 1 \\
0 & 1 & 1 \\
1 & 1 & 1 \\
\end{pmatrix} \# \begin{pmatrix}
1 \\
1 \\
0 \\
\end{pmatrix}
\]

Equation 7-12:

Generally, a local operation involving M neighbors takes \(\sim M\) instruction cycles.

7.4 Sum

To sum a one-dimensional array of N items, the array is divided into sections, each of which contains M consecutive items. In step 1, all sections are summed concurrently from left to right, in \(\sim M\) instruction cycles. In step 2, the section sums, which are at the right-most items of every sections, are summed together serially in \(\sim N / M\) instruction cycles. This algorithm can be displayed by the algorithm flow diagram in Figure 9, in which a serial operation is represents by a data flow arrow, and concurrent parallel operations are represents by a data flow arrow with two parallel bars on each side. Each data flow arrow shows the data range of the operation, such as on a section of M items within the whole array of N items. Each series of arrows is marked by a step sequence number followed by “:”, an instruction cycle count preceded by “~”, and an operation, such as “1: ~M sum”. The instruction cycle counts from consecutive and independent steps are additive, so that the total instruction cycle count is \(\sim (M + N / M)\), which has a minimum of \(\sim \sqrt{N}\) when \(M \sim \sqrt{N}\).

To sum a two-dimensional array of Nx by Ny items, the array is divided into sections, each of which contains Mx by My consecutive items. In step 1, all rows of all sections are summed concurrently from left to right, in \(\sim Mx\) instruction cycles. In step 2, all the right-most columns of all sections, each item of which contains a row sums for the section, are summed concurrently from bottom to top. Then the top-right-most items of all sections, each of which contains the section sum, are scanned and summed together serially, with the row and the column direction
being the fast and the slow scan direction respectively. Figure 10 is the corresponding algorithm flow diagram, in which step sequence number “4 * 3” means that a complete step 3 is carried out before each instruction cycle of step 4. The total instruction cycle count for such combination of steps is the product of the individual instruction cycle count of each step. The total instruction cycle count for the 2-D sum is \( (Mx + My + Nx/Mx Ny/My) \), which has a minimum of \( \sqrt[3]{Nx Ny} \) when \( Mx \sim My \sim \sqrt[3]{Nx Ny} \).

7.5 Find Global Limit

A procedure similar to sum can be used to find global limit for an array.

7.6 Search for Template

In contrast to a substring search, the result of a template search does not have to match the template exact. The difference between the template and a section of original data is captured by a matching value. The goal of template search is to find a best match or all acceptable matches. Template search is the foundation for image pattern recognition [2].

To search a template of size \( M \), the array is divided into \( N / M \) sections, each of which contains \( M \) consecutive items. The algorithm diagram is shown in Figure 11. In Step 1, the template to be matched is concurrently loaded to all sections in \( \sim M \) instruction cycles. Then the point-to-point absolute difference is calculated concurrently for all points in \( \sim 1 \) instruction cycles, which is omitted from the algorithm flow diagram. In Step 2, the difference in all sections are summed concurrently from right to left in \( \sim M \) instruction cycles, to obtain the difference values of the array to the template at the first positions to the left of all sections. In the first instruction cycle of Step 3, the templates in all sections are shifted right by one item, to calculate the difference at the second positions of all sections, and so forth. Thus the total instruction cycle count is \( \sim (M + M^2) \sim M^2 \).
Similar algorithm can be carried out in searching a 2-D array of size Nx by Ny for a 2-D template of size Mx by My. The algorithm diagram is shown in Figure 12. In step 2*1, the template to be matched is loaded to all sections concurrently. The first instruction cycle of Step 3 sums the point-to-point absolute difference of each row of each section at the left-most column of the section. The first instruction cycle of Step 4 moves the template right by one column. The first complete application of Step 4*3 fills all the columns with the sums of row difference of the corresponding sections. The first instruction cycle of Step 5 results in the matching of the template to the bottom-most row of each section. The first instruction cycle of Step 6 moves the template up by one row. The Step 4*3 is carried out again except that the Step 4 is carried out from right to left this time. The total instruction cycle count is $\sim (Mx My + (Mx^2 + My) My) \sim (Mx^2 My)$.

The instruction cycle count is reduced from $\sim (N M)$ to $\sim M^2$ for 1-D template search, and it is reduced from $\sim (Nx Ny Mx My)$ to $\sim (Mx^2 My)$ for 2-D template search, thus no longer depends on the original image size. It may be small enough now for the template search algorithm to be carried out in real-time for a lot of applications, such as image databases.

7.7 Sort an Array

By asking all elements to identify themselves if their left layer is larger than their neighboring layer, the disorder items, which are the items stored in the neighboring layer that need to be sorted to small-to-large order, can be all found immediately. Thus a sorting algorithm can stop immediately if no further sorting is required. The disorder item count also guides the sorting direction. If initially the disorder item count for small-to-large sorting is more than that of the large-to-small sorting, the array should be sorted into large-to-small order—to sort an array in either order is functionally equivalent. Thus, the worst case for sorting, to sort a nearly sorted array into the other order, can be avoided.

Figure 13 uses topography to describe point defects of sorting disorders.
Concurrent Processing Memory

- **Peak**: It is an insertion of a larger item into an otherwise ordered neighborhood. To restore order, the peak item can be moved to the left of the left-most item to its right which is larger than it, or to the right end of the sequence in ~2 instruction cycles.

- **Valley**: It is an insertion of a smaller item into an otherwise ordered neighborhood. To restore order, the valley item can be moved to the right of the right-most item to its left which is smaller than it, or to the left end of the sequence in ~2 instruction cycles.

- **Fault**: It is an exchange of two already sorted neighboring items. To restore order, the two faulty items can be exchanged in ~1 instruction cycles.

Only ~1 instruction cycles are required to exchange concurrently all even and odd numbered neighboring items once toward small-to-large order. Alternatively repeating exchanging all (1) even and odd and (2) odd and even numbered neighboring items makes a local exchange sorting algorithm, which is good at removing random local disorders. Using the local exchange sorting algorithm, an originally random-ordered array quickly becomes largely sorted with only a few point defects. When M is sufficiently large, after M instruction cycles, the average distance between the remaining point defects is ~ M. However, the local exchange sorting algorithm is inefficient in sorting a nearly sorted array, with peaks and valleys moving to their respective sorting destinations one step at a time.

In contrast, a global moving sorting algorithm removes peaks and valleys in a nearly sorted array and inserts them to proper places. Using content computable memory, the concurrent detection of all of the above point defects in each 4-item neighborhood requires ~4 instruction cycles, the concurrent detection of the destination position of a peak or valley takes ~1 instruction cycles, while each insertion takes ~2 instruction cycles. Thus, the global moving sorting algorithm is very efficient in sorting a nearly sorted array.
To sort an originally random-ordered array, if the local exchange sorting algorithm is first used for \( M \) instruction cycles, then the sorting is finished by the global moving sorting algorithm, the total instruction cycle count is \( \sim (M + N/M) \), which has a minimum of \( \sim \sqrt{N} \) when \( M \sim \sqrt{N} \).

7.8 Thresholding

With its multiple dimensions of data, image processing and modeling generally requires large amount of calculation, which is proportional to the size of data in each dimension.

Using a conventional bus-sharing MIMD computer, the instruction cycle count is linearly proportional to the amount of calculation. Thus, to solve a problem in a realistic time period, thresholding [2] is frequently used to ignore large amount data for the subsequent processing. Thresholding is a major problem [2], because proper thresholding is difficult to achieve, and thresholding in different processing stages may interact with each other.

Using a content computable memory, the instruction cycle count is decoupled from the amount of calculation, and is independent of the size of data in each dimension. Thus, thresholding can be used only in last stage to qualify the result. Also, thresholding itself has been reduced to \( \sim 1 \) instruction cycle operation.

7.9 Line Detection

Due to neighbor-to-neighbor connectivity, 2-D content computable memory can treat line detection problem as a neighbor counting problem. To detect edges line with pixel length \( L \) lying exactly along X direction left to each pixel, the neighbor count algorithm is direct:

1. All pixels concurrently subtract the raw intensity of their bottom layer from that of their top layer, and store the result in the neighboring layer.
2. All pixels concurrently sum the neighboring layers of their \( L \) left neighbors together with their own. The absolute value of the result indicates the possibility of an edge line.
starting from that pixel, while the sign of the result indicates whether the edge is rising or falling along the Y direction.

To detect edge lines with a slope of \(\frac{My}{Mx}\) in which \(Mx\) and \(My\) are two integers, each pixel defines a rectangular area of \(Mx\) by \(My\) pixels denoted as the \((Mx \times My)\) area, and the line which connects the pixel and the furthest corner of the area has the slope of \(\frac{My}{Mx}\). Similar to obtaining the section sums in a sum algorithm, a messenger starts from furthest corner of the area, walks \((Mx + My)\) steps along the line until it reaches the original pixel. In each of its stop, in a predefined fashion, if the pixel is on the left side of the line, its intensity is added to the messenger; otherwise, its intensity is subtracted from the messenger. When reaching the original pixel, the value of the messenger indicated the possibility and the slope direction of the edge line segment which connects the original pixel and the furthest corner of the \((Mx \times My)\) area. Thus, it is called the line segment value of the pixel for the \((Mx \times My)\) area. This accumulating process is carried out concurrently for all the pixels of the image, independent of image sizes. Figure 14 shows the \((4 \times 3)\) area to detection a line with a slope of \((3/4)\) passing the original pixel at 0. The accumulation processing is from pixel 7 to pixel 0 in sequence, with the raw intensity of pixel 1, 3, and 5 to be added to, and those of pixel 2, 4, and 6 to be subtracted from the messenger.

Given an angular resolution requirement, a \(\{(Mx, My)\}\) set can be constructed to detect lines of all slopes on an image. To construct such a set for an angular resolution \(\sim \left(\sqrt{2}/D\right)\), a circle of radius \(D\) is drawn on a square net of pixels, and the vicinity pixels to the circle are the starting pixels for the messengers in the \(\{(Mx, My)\}\) set. Figure 15 shows such a set of lines with \(D\) equals 5. The total instruction count to detect all lines in the set is \(\sim D^2\), independent of the image size. As a result of line detection, each pixel is marked by the best line segment value together with its corresponding \((Mx, My)\) area.
8 Conclusion and Discussion

As an in-memory massive SIMD approach, CPM seems to be able to vastly improve the solutions to typical array problems in the framework of traditional bus-sharing architecture running a prevailing multi-task operating system. Each type of CPM is specified at a particular application in both its hardware construct and software instruction set.

One important issue for the wide acceptance of in-memory massive SIMD architecture is its ability to be shared by multiple tasks. CPM allows task switch by allowing exclusively writing to one set of its addressable registers while concurrently operating on another set of its registers within a same memory. However, while a traditional task is completely captured by its register file [5][6][7][8], a SIMD task has data distributed all over the SIMD device, so that the cost of a traditional task switching for a SIMD task may be too high. How to best incorporate such a SIMD task into a currently prevailing preemptive multitask operating system [5][6] remains a question. Massive amount of data for a pending task needs to be provided to the SIMD device, which may makes the bus bottle-neck problem even worse, thus it may be worthwhile to introduce an additional bus with DMA capability dedicated to a SIMD devices for task switching purposes. On the other hand, as a family member of CPM, the content movable memory may greatly simplify memory management function of current operating systems. Thus, CPM may raise new requirements and new opportunities for the current operating systems.

Another important issue is whether the set of rules for CPM is too restrictive in general, even though content movable memory, content searchable memory and content comparable memory all seem to have worked for their respective targeted application in most efficient manner. For example, super connectivity [5][9] can be introduced to a 1-D content computable memory as shown in Figure 16: (1) In the 1st level, the local connectivity of all PEs forms a periodical pattern; (2) In the 2nd level, a new connection is established in turn between all closest two PEs which have no direct connection; (3) In the 3rd level, same process is repeated on the 2nd level,
so on. Such super connectivity enables a 1-D content computable memory to finish its global operations such as sum and limit finding in $\sim \log(N)$ instead of $\sim \sqrt{N}$ instruction cycles. However, such super connectivity breaks Rule 1, Rule 3 and Rule 7 of CPM, and it brings additional hardware & software costs, e.g., according to Figure 16, the instruction set of each PE depending on its element address, though on each level of super connectivity SIMD is still preserved. Whether such cost is justified for a massive SIMD approach needs further studies.

As a theoretical discussion focusing on the applicability of an in-memory massive SIMD approach, this paper has left out all implementation technical questions, such as (1) how to broadcast a same instruction to a massive number of PEs on a same chip at decent speed, (2) how to deal with grounding problem when a massive number of PEs change states concurrently, (3) how to chain a same type CPM together to achieve higher capacity like chaining real memories, and (4) what is the expected clock rate and number of PEs using today’s technology. Although these questions are vital for CPM, and they are probably very challenging questions in term of currently available technologies, they can be solved only if there is a need to solve them—further studies are need for the worth and practicability of CPM.

Simply physics may give a rough estimation for the above questions. For an example, assume that all PEs of a CPM are laid out on a square lattice, and a dedicated routing layer is used for each bit of the concurrent bus. Such a routing layer has a speed limit due to its capacitance and resistance. Denote the overall size and the thickness of the copper layer for routing as L and T respectively. Denote the thickness of silicon dioxide which insulates the copper layer as D. The time delay of the routing layer is given by Equation 8-1:

Equation 8-1: \[ (4 \times 8.8 \times 10^{-12} \frac{L^2}{D}) (17 \times 10^{-9} /T) = 0.6 \times 10^{-18} \frac{L^2}{D/T}; \]

Equation 8-1 shows that for massive SIMD the vertical dimension of the routing layer should be as large as possible. Let $D = 25$ nm, and $T = 10$ nm. Assume that the CPM needs to run at 1 GHz, which means an overall delay less than $0.5 \times 10^{-9}$ sec. Thus $L$ should be no more than 0.5 mm. For content movable memory, a rough layout using 20-nm technology requires about 0.25
\( \mu m^2 \) per 32-bit PE. A total silicon area about 15x15 mm\(^2\) is required to make a 4G-byte content moveable memory, which is within the practical size of current semiconductor devices [39]. If the content memory needs to update its content at 1GHz, each time the routing layer can broadcast to no more than \(10^3 \times 10^3\) PEs, which corresponds to 4M-byte memory. However, if a content movable memory can cache input requests, it may delay the memory management requests to the next update cycle for RDAM cells, so that the routing layer can be larger running at a slower speed. For example, if output cache depth is 4, and system bus is at 400MHz, then each routing layer can run at 100MHz with a size of 1.5x1.5 mm\(^2\). Within a same chip, due to SIMD simplicity, the CPM only needs simple caching logic for input & output, and simple synchronization logic between each synchronized PE arrays, both of which should not occupy significant amount of silicon area. Thus, at least content moveable memory seems practical using today’s best technologies.

As an independent research, the author of this paper feels indebted to the encouragements and valuable discussions with Dr. Nick Tredennick from Gilder Technology Report, Prof. Pao-Kuang Kuo from Wayne State University, Prof. Sangjin Hong and Prof. Tzi-cker Chiueh from SUNY at Stony Brook, and the organizers of PDPTA 2003, Prof. Hamid R. Arabnia from University of Georgia in particular.

9 Reference

[1] R. Ramakrishnan and J. Gehrke, Database Management Systems (Mc Graw Hill, 2002)
[2] E. R. Davies, Machine Vision: Theory, Algorithms, Practicalities (Academic Press, 1990)
[3] String searching algorithm, http://en.wikipedia.org/wiki/String_searching_algorithm
[4] B. Szabó, B. A. Szabó, I. Babuska, Finite Element Analysis (Wiley and Sons, 1991)
[5] T. J. Fountain, Parallel Computing: Principle and Practice (Cambridge, 1994)
[6] John P Hayes, Computer Architecture (McGraw-Hill, 1988)
Concurrent Processing Memory

[7] John L. Hennessy, David A. Patterson, Computer Organization & Design (Morgan Kaufmann 1998)

[8] D. E. Culler, J. P. Singh, A. Gupta, Parallel Computer Architecture : a Hardware / Software Approach (Morgan Kaufmann 1999)

[9] C. P. Wang, and Z. Wang, A Smart Memory Design. In: Parallel and Distributive Processing, Technology, and Application, June, 2003.

[10] Frederic Magoules, Fundamentals of Grid Computing: Theory, Algorithms and Technologies (Chapman and Hall/CRC Numerical Analy and Scient Comp. Series)

[11] The OpenMP API specification for parallel programming, http://openmp.org/wp/

[12] The Message Passing Interface standard, http://www.mcs.anl.gov/research/projects/mpi/

[13] M. A. Heroux, P. Raghaven, H. D. Simon, Parallel Processing for Scientific Computing (Siam 2006)

[14] J. Labarta, and J. Gemenez, pages 9-31, Performance Analysis: from Art to Science, Parallel Processing for Scientific Computing (Siam 2006)

[15] M. Hall, P. Kogge, J. Koller, P. Diniz, J. Chame, J. Draper, J. LaCoss, J. Granacki, J. Brockman, A. Srivastava, W. Athas, V. Freeh, J. Shin, and J. Park. Mapping Irregular Applications to DIVA, a PIM-Based Data-Intensive Architecture. In: Supercomputing, November 1999.

[16] Basilio B. Fraguela Jose Renaus Paul Feautrierz David Paduay Josep Torrellas. Programming the FlexRAM Parallel Intelligent Memory System, PPoPP 2003.

[17] K. Mai, T. Paaske, N. Jayasena, R. Ho, W. Dally, M. Horowitz. Smart Memories: A Modular Reconfigurable Architecture. In: ISCA, June 2000.

[18] The Berkeley Intelligent RAM (IRAM) Project, Univ. of California, Berkeley, at http://iram.cs.berkeley.edu.
[19] David L. Tennenhouse, Jonathan M. Smith, W. David Sincoskie, David J. Wetherall, and Gary J. Minden. A Survey of Active Network Research. IEEE Communications Magazine, Vol. 35, No. 1, pp80-86. January 1997.

[20] Mark Oskin, Lucian-Vlad Lita, Frederic T. Chong, Justin Hensley and Diana Keen. Algorithmic Complexity with Page-Based Intelligent Memory. Parallel Processing Letters Vol 10. No 1 (2000) pages 99-109.

[21] L. Oliker, R. Biswas, R. V. Wijngaart, D. Bailey, A. Snavely, Performance Evaluation of Modeling of Ultra-Scale Systems, pages 77-93, Parallel Processing for Scientific Computing (Siam 2006)

[22] Streaming SIMD Extensions, [http://en.wikipedia.org/wiki/Streaming_SIMD_Extensions](http://en.wikipedia.org/wiki/Streaming_SIMD_Extensions)

[23] G. Almasi, S. Chatterjee, A. Gara, J. Gunnels, M. Gupta, A. Henning, J. E. Moreira and B. Walkup, Achieving high performance on the blue gene supercomputer, pages 59-75, Parallel Processing for Scientific Computing (Siam 2006)

[24] J. D. Teresco, J. E. Flaherty, S. B. Badenz, J. Faikx, S. Lacour, M. Parashark, V. E. Taylor and C. A. Varelay, Approaches to architecture-aware parallel scientific computing, pages 35-51, Parallel Processing for Scientific Computing (Siam 2006)

[25] R. J. Offen, VISL Image Processing (McGraw-Hill, 1986)

[26] Caxton Foster, Content Addressable Parallel Processors (Van Nostrand Reinhold, 1976)

[27] A. Krikelis (Editor), C. C. Weems (Editor), Associative Processing and Processors (IEEE Computer Society Press, 1997)

[28] K. K. Rangan, N. B. Abu-Ghazaleh, P. A. Wilsey, A Distributed Multiple-SIMD Intelligent Memory, Proceedings of the 2001 International Conference on Parallel Processing (2001), Page 507-516

[29] R.A. Walker, J. Potter, Y. Wang, M. Wu, Implementing Associative Processing: Rethinking Earlier Architectural Decisions, Proceedings 15th International Parallel and Distributed Processing Symposium (2001), Page 2092-2100,
Concurrent Processing Memory

[30] L. Chivin and R. Duckworth, Content-addressable and associative memory: Alternatives to the ubiquitous RAM. IEEE Computer Magazine, p51-64, July 1989.

[31] Wafer-scale integration, http://en.wikipedia.org/wiki/Wafer-scale_integration

[32] 3D integrated circuit, http://en.wikipedia.org/wiki/Three-dimensional_integrated_circuit.

[33] System-on-a-chip, http://en.wikipedia.org/wiki/System-on-a-chip.

[34] G. E. Moore, Cramming more components onto integrated circuits, Electronics, Volume 38, Number 8, April 19, 1965.

[35] Y. Patt, S. Padel, M. Evers, D. Friendly, and J. Shark. One Billion Transistors, One Uniprocessor, One Chip, IEEE Computer, 30 (1997), 51-57.

[36] D. Burger and J. Goodman, Billion-Transistor Architecture, There and Back Again, IEEE Computer, 37 (2004), 22-28.

[37] L. Hammond, B. Hubbert, M. Siu, M. Prabhu, M. Chen, and K. Olukotun, The Stanford Hydra CMP, IEEE Micro 20 (2000) 71-84

[38] M.I. Soliman, A.F. Al-Junaid, Pages 103-121, System-C implementation and performance evaluation of a decoupled general-purpose matrix processor, Parallel Processing Letters, Vol 20-2 (2010, June)

[39] J. Rabaey, Digital Integrated Circuits (Prentice Hall 1999)

[40] P. Horowitz and H. Winfield, Art of Electronics (Cambridge Univ Press, 1995)

[41] A. Silberschatz and P. B. Galvin, Operating System Concepts (Wiley & Son, 2001)

[42] H. L. Dershem, M. J. Jipping, Programming Languages: Structures and Models (Wadsworth Publishing 1990)

[43] Unicode, http://en.wikipedia.org/wiki/Unicode.

[44] R. K. Stephens and R. R. Plew, Teach Yourself SQL in 21 Days (Sams Publishing 2002)
Concurrent Processing Memory

10 Figures

Figure 1: Concurrent Processing Memory Architecture

Figure 2: 3/8 Parallel Shifter
Concurrent Processing Memory

Figure 3: 3/8 All-line Decoder

Figure 4: Element Activation Logic

Figure 5: PE Construct of a Content Movable Memory.
Figure 6: PE Construct of a Content Searchable Memory.

Figure 7: PE Construct of a Content Comparable Memory.
Figure 8: PE Construct of a Content computable memory.

Figure 9: Algorithm Flow Diagram for 1-D Sum

Figure 10: Algorithm Flow Diagram for 2-D Sum
Concurrent Processing Memory

1: \(\sim M\) load
2: \(\sim M\) sum
3 * 2: \(\sim M\) right move

Figure 11: Algorithm Flow Diagram for 1-D Template Matching

Figure 12: Algorithm Flow Diagram for 2-D Template Matching

Figure 13: Point Defects in a Otherwise Sorted Neighborhood
Concurrent Processing Memory

Figure 14: 2-D Line Detection Using Messenger

Figure 15: A Set of Lines of Pixel Spans about 5 In Real Distance.

Figure 16: A 1-D Content Comparable Memory with Super Connections.