X-ray speed reading: enabling fast, low noise readout for next-generation CCDs

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ABSTRACT

Current, state-of-the-art CCDs are close to being able to deliver all key performance figures for future strategic X-ray missions except for the required frame rates. Our Stanford group is seeking to close this technology gap through a multi-pronged approach of microelectronics, signal processing and novel detector devices, developed in collaboration with the Massachusetts Institute of Technology (MIT) and MIT Lincoln Laboratory (MIT-LL). Here we report results from our (integrated) readout electronics development, digital signal processing and novel SiSeRO (Single electron Sensitive Read Out) device characterization.

Keywords: readout electronics, CCD, ASIC, ROIC, integrated circuit, X-ray, Lynx, HDXI

1. INTRODUCTION

Future strategic X-ray astronomy missions like AXIS propose a combination of large collecting area mirrors with large, fast, wide-field imagers. High frame rates will be essential to minimize the impact of pile-up for point sources and to mitigate the impact of the particle background on studies of faint, diffuse gas. At the same time, low noise and excellent soft X-ray energy response must also be maintained to meet the key science goals. State-of-the-art CCDs are close to being able to deliver all key performance figures for such missions except for the required frame rates. Fast frame rates for large detectors result in very high effective pixel rates. Our group at Stanford is addressing this technology gap through a multi-pronged approach, in collaboration with the Massachusetts Institute of Technology (MIT) and MIT Lincoln Laboratory (MIT-LL). To achieve higher frame rates, we are working to increase both the readout speed of individual outputs and the number of outputs per CCD that can operate in parallel. Figure 1 shows a possible CCD module concept suitable for the AXIS focal plane. Speed increases on individual outputs stem from CCD output stage optimization, reduction of parasitic output loading through the use of an dedicated ASIC, and the use of digital signal processing on the video waveform. The readout ASIC also allows us to operate multiple outputs in parallel with a small footprint and modest power consumption. We are also investigating a novel detector technology manufactured at MIT-LL, the Single electron Sensitive Read Out (hereafter SiSeRO) that, while not quite yet capable of single electron noise performance, offers a promising pathway to very low noise, high speed X-ray detectors.

2. CCD OUTPUTS AND VIDEO SIGNAL

The output of a CCD is usually implemented with a floating diffusion, which collects the charge signal, connected to the gate of a source follower biased with a current source. While the gate is not driven by a low impedance, as for a normal source follower, but rather by a high impedance floating capacitor plate, any charge moved...
| Parameter                        | demonstrated lab capability | target capability |
|---------------------------------|-----------------------------|-------------------|
| CCD size [pixels]               | 1440                        | 1440              |
| pixel size [µm]                 | 24                          | 24                |
| total FOV of 4 modules [armin⁻¹]| 25.1                        | 25.1              |
| CCD outputs                     |                             |                   |
| IA to DS clock rate [MHz]       | 1                           | 2                 |
| serial pixels per output        |                             |                   |
| pixel rate per output [MPix/s]  | 160                         | 90                |
| FS transfer time [µs]           | 1.4                         | 0.7               |
| readout time [µs]               | 140                         | 37                |
| frame rate [fps]                | 7                           | 26                |
| out of time ratio               | 1.0%                        | 1.9%              |
| photon rate per sec and pixel   | 2.4                         | 8.7               |

(a) Concept of a CCD module
Figure 1: One possible implementation for a AXIS focal plane would be to tile four sub modules each consisting of a frame-transfer CCD with 1440 x 1440 pixels of 24 µm size into a detector with a total of 8 Mega-pixels, where each pixel corresponds to 0.5°. Image to frame store transfer could be achieved in roughly 1 ms, with read out of the frame store occurring while the subsequent image is gathered. To achieve a desired frame rate of more than 20 fps, the CCD would use 16 outputs distributed across the 34 mm of the detector edge, each of them read out with a pixel rate of at least 4 MHz.

(b) specifications and estimated performance

(a) CCD output stage schematic
Figure 2: Left - CCD output stage schematic consisting of a floating diffusion, a JFET first stage followed by a NMOS second stage and a discrete transistor third stage. Right - A typical CCD video waveform seen at the source of the output stage transistor. The output exhibits usually a large DC offset from the bias points of the output stage. During the readout operation the waveform goes through the stages of reset, baseline settling, charge transfer and signal settling for every pixel that is read out onto this node will change the output voltage at the source. In order to achieve a large conversion gain from charge to voltage, the node capacitance needs to be minimized, which demands a small transistor with minimal gate capacitance and therefore limited transconductance. To improve the drive strength (and speed) of such an output, further source follower stages utilizing larger transistors are often used. To establish a bias point for the floating capacitor plate and therefore the source of the transistor, the node is periodically reset to a fixed potential - this potential is commonly called the Reset-Drain voltage, supplied via a reset transistor (switch).
Figure 2a shows such an output for a MIT Lincoln Laboratory CCD with a p-JFET first stage and a NMOS second stage. The first stage is biased with a CCD on-chip current source, while the second stage requires an off-chip current source. During operation, charge is shifted through the CCD registers and will end on the floating diffusion and modulate the transistor gate. The whole process is depicted in Figure 2b and consists of the following steps, with the resulting waveform at the output commonly called the CCD video signal:

- **Reset** - the reset pre-charges the floating diffusion, and the gate of the first stage, to a predefined potential. The reset clock on the gate of the reset transistor often generates considerable reset feed-through on the video waveform.
- **Baseline settling** - after the reset, the output will settle to a baseline voltage level that corresponds to the empty charge state.
- **Charge transfer** – clocking transfers the charge from the serial register of the CCD to the floating diffusion and, therefore, the gate of the first stage. This clocking often generates a disturbance on the video waveform due to parasitic capacitive coupling.
- **Signal settling** - after the signal charge is transferred and acts on the transistor gate, the output will settle to a signal level. The change from the baseline to the signal level is directly proportional to the amount of charge transferred. If the charge packet consists of electrons, the resulting signal level is at a lower potential than the baseline level.

The signal amplitude and, therefore, the size of the charge packet transferred is extracted from the waveform by taking the difference between the signal and baseline, more recently performed by digital signal processing of the sampled waveform. The described voltage readout with source follower output stage is a common implementation, but not the only option. Another option is drain current readout, as pioneered by the Athena Wide Field Imager\(^2\) and its readout chip VERITAS.\(^3\) In the MIT Lincoln Laboratory SiSeRo (Single-electron Sensitive Readout) implementation, the floating diffusion and the JFET are replaced with a PMOS transistor that includes a region under the transistor (in the bulk of the silicon) that serves as the back gate. The CCD channel can clock the charge signal into the region under the PMOS and also move it out again. Any charge transferred in the area under the PMOS modulates the transistor channel changing the current flow. To optimize charge transfer in and out of the transistor area, fixed voltages at the transistor terminals are preferred. At this fixed voltage a small current biases the transistor and the signal is determined by measuring the change in current.

### 3. INCREASING THE READOUT SPEED FOR PJFET OUTPUTS

The output stage as outlined above has multiple nodes that limit the speed due to their inherent RC time constants. The first limitation is the pJFET driving the second stage NMOSFET. In the CCID85 there is roughly a five fold difference in Gm between the two transistors, slightly higher than the usual factor of three that is commonly used. (It is to be noted that these are also two different types of transistors and such the optimum scaling is different.) We estimate this limitation to be around 8 MHz in bandwidth. The next limitation is the second stage driving the off-chip stage. From DC characterization we estimate the \(g_m\) of the NMOS to be around 250 \(\mu S\) (depending on the exact bias condition). For the following measurements, we have been using our TinyBox CCD\(^4\) test system that utilizes an STA Archon Controller with digital correlated double sampling but also a raw mode to export complete video waveforms for offline processing.

#### 3.1 Improved discrete electronics

In order to minimize the load capacitance and not add further voltage follower stages that exhibit gains below unity and small but not negligible noise components, we decided to replace the external JFET with an active amplification stage with small input capacitance. We selected the ADA4817 OPAMP for its wide bandwidth (1 GHz), small input capacitance (1.3 pF) and low input noise (4 nV/√Hz). The complete circuit is shown in figure 3 and delivers an effective bandwidth of 50MHz (including compensation) at a gain of 5, with a total input referred noise of around 15 nV/√Hz.

While the input noise of the alternative JFET can be lower, one has to consider that a source follower stage has less then unity gain, requiring an additional gain stage in any case. In conclusion, the amplification stage
Figure 3: Schematic of the preamplifier circuit to read out the CCD analog output. It uses a single-ended operational amplifier (ADA4817) in a non-inverting configuration as the first stage, which is followed by a fully differential ADC driver (AD8138).

performs as good as the solution with an external JFET but with smaller input capacitance, such that in a practical implementation the load capacitance will be limited by the packaging and PCB parasitic capacitance. We performed an extensive characterisation campaign with a MIT Lincoln CCID85 in,\textsuperscript{5} where we also optimized for high speed readout up to 4 MPix/sec, double that previously obtained. Figure 4 is a summary for the achieved results. As we increase the pixel rate, the video waveform gets squeezed and the baseline and signal region are barely recognizable. Further, the reset pulse begins to dominate the readout time, a problem we plan to improve with a faster reset clock driver in the next generation of the readout PCB. Due to the squeezed waveform, the available number of samples that can be used for digital CDS reduces from 18 to 7 as the speed doubles from 2 to 4 MPix/sec, resulting in a noise increase of roughly a factor of $\sqrt{2}$, in line with the expectations. The CCID85 used here has a conversion gain of $28 (\mu V/e^{-})$ while the newer CCID93 delivers up to $60 (\mu V/e^{-})$ and has demonstrated noise performance as low as $2.6 e_{RMS}$ for 2 Mpix/sec.\textsuperscript{6}

![Figure 3: Schematic of the preamplifier circuit to read out the CCD analog output. It uses a single-ended operational amplifier (ADA4817) in a non-inverting configuration as the first stage, which is followed by a fully differential ADC driver (AD8138).](image)

Figure 4: Results from CCID85 characterisation at readout speeds of 2, 3 and 4 MPIX/sec. At high speeds the reset pulse dominates the readout time, resulting in the number of samples that can be used for signal processing dropping from 18 to 7, while the speed doubles from 2 to 4 MPix/sec. The readout noise increases by the expected factor of approximately $\sqrt{2}$ as the speed doubles.

| Readout speed (MHz) | 2    | 3    | 4    |
|---------------------|------|------|------|
| Num. of samples in CDS | 18   | 10   | 7    |
| Read noise ($e_{RMS}$) | 5.3  | 6.1  | 7.6  |
| Board noise ($e_{RMS}$) | 1.7  | 2.0  | 3.2  |
| System gain (ADU/e) | 0.84 | 0.83 | 0.81 |
| Conversion gain (µV/e) | 28   | 27.8 | 26.8 |
| FWHM (eV) @ 5.9 keV | 133  | 139  | 148  |

3.2 MIT CCD Readout ASIC MCRC

Further improvements to the discrete readout electronics pose a number of challenges. Firstly, discrete electronics require considerable board space and power consumption. This is especially problematic when, in order to increase the frame-rate further, many parallel operating outputs are required. In addition, it is not obvious how the load capacitance to the detector output could be further reduced when packaging and PCB parasitics dominate the load capacitance. An integrated microelectronics solution can remedy all of these problems:
Figure 5: Left - Photograph of the MCRC V1.0 chip. The eight groups of pads at the top are the analog inputs to the eight channels. The bottom row is composed of differential outputs pads and power supply pads, respectively. Pads on the right side belong to the digital communication interface, while the left side pads are part of the biasing and debugging circuits. The analog core is compact and located in the center of the chip. Right - Overview schematic of the MCRC analog channel. Each of the analog channels consists of an input stage, which is user selectable between the voltage input and the current input. The input section of the chip is followed by a pre-amplifier and a fully differential buffer driver.

- The footprint is small enabling the ASIC to sit close to the detector output.
- The proximity of the unpackaged die allows the chip to be wire-bonded directly to the detector outputs, significantly reducing the load capacitance.
- Custom ASIC solutions usually have a much smaller power consumption than generic commercial components.

These potential advantages lead our group to developed the MIT CCD Readout Chip (MCRC) V1.0. Figure 5a shows the manufactured chip and its functional blocks outlined on the photograph. The ASIC includes 8 readout analog channels operating in parallel, a digital SPI interface to program the ASIC settings and control the internal switch logic, four bias DACs to set the various internal circuitry operating points. Each of the analog channels consists of an input stage, which offers the user the ability to select between the voltage and the current inputs, respectively. In addition, both inputs feature CCD bias current sources. The input stage is followed by a pre-amplifier and a fully differential buffer driver. The chip can handle up to 12 V of input DC voltage at its voltage input. Figure 5b shows an overview schematic of a single analog readout channel. The manufactured chip has been verified and characterised for its functionality and performance. Details of this characterisation can be found in.

Compared to a discrete solution, the MCRC V1.0 benefits from:

- A small input capacitance of only 1.5 pF total.
- A bandwidth of 50 MHz over the full chain.
- Low power consumption of only 35 mW per Channel. Roughly an order of magnitude less than the discrete implementation.
- A measured input noise voltage spectral density of 6.5 nV/√Hz. Further outperforming the discrete implementation.

The next stage of development is to test a multi-output CCD with the MCRC V1.0 ASIC. We have constructed a dedicated test module for the large 2 megapixel CCID89 sensor from MIT Lincoln Laboratory that features eight outputs. Figure 6 shows a photograph of the module. The MCRC V1.0 ASIC can be mounted on the board mid-way along the bottom edge of the sensor, replacing the eight-channel discrete electronics (highlighted...
Figure 6: Photography of a CCID89 X-ray CCD mounted in a test circuit board. The large 2 megapixel sensor features eight output ports. The orange boxes show the 8-channel discrete readout electronics, while the MCRC V1.0 ASIC can be mounted on the board mid-way along the bottom edge of the sensor. The replacement of the discrete electronics with the MCRC V1.0 ASIC will result in a substantial reduction in foot print and an order of magnitude power reduction.

in orange), enabling a substantial reduction in board space. Initial measurements with the discrete electronics have already started and measurements with the ASIC will commence in the fall of this year. This module should provide frame rates of around 5 fps with the discrete electronics and 18 fps with the MCRC V1.0 ASIC.

4. DIGITAL SIGNAL PROCESSING

Our readout concept offers the capability to examine the video waveform and perform digital signal processing, beyond the classical per pixel processing required to construct X-ray events and an image.

4.1 Digital signal processing on CCD with JFET output

In order to optimize the digital CDS filtering of the 2 to 4 MPIX/sec measurements presented in section 3.1, we saved a number of raw video waveforms for offline processing. The first thing we examined was the overall variation of the waveforms from pixel to pixel, as most of this variation will be suppressed by the CDS filtering used for X-ray images. Figure 7a shows a waveform ensemble from 50 pixels, read out at a rate of 2 MPix/sec, which line up closely on top of each other. Figure 7b shows the residuals of the same data after the subtraction of the average waveform: The spread during the reset pulse (at around 50-100 ns) is small (around 3.5 ADU rms) while after the reset the output node settles at different levels (18 ADU rms), dominated by the KTC noise of the reset process. Due to the limited bandwidth of the output stage, the transient behavior between reset and baseline level is visible. The next question posed is how close the baseline measurement can be positioned towards the reset pulse. For this investigation, every single one of the 50 waveforms was offset corrected, such that the level at the baseline portion of the waveform is set to the average level. This process is equivalent to analog clamping. Then the rms variation for the waveform sample points across all the 50 waveforms was calculated. This will reflect the actual readout procedure, where the signal is measured relative to the baseline. Figure 7c shows the resulting plot. The variation around the baseline portion is low, stays relatively constant between baseline and signal, but rises sharply as it approaches the reset pulse.
4.2 Digital signal processing with SiSeRO outputs

Previously, we have demonstrated proof of principle measurements of novel SiSeRo devices fabricated by MIT Lincoln Laboratory. In our ongoing characterisation efforts, we have used the same waveform analysis techniques outlined above to study the overall variation and reset behavior of these devices. As SiSeRO devices clear charge from the back gate region by simply transferring out, like any other charge transfer in a charge coupled device, this process should not exhibit KTC noise. Figure 8a shows an ensemble of 50 video waveforms from 50 different pixels (as above for the JFET in 7a). Figure 8b plots the sample point variation of the waveforms after they have been referenced to the average value at the baseline. The plot shows two successive pixels to illustrate the evolution across pixels. Variation is low at the baseline level where the video waveform is clamped and increases left and right from this point. The charge clear pulse has no effect on the sample variation and no KTC noise bump is visible.

Figure 8: Left - Video waveform ensemble of 50 pixels with the SiSeRo output. The large pulse at the beginning is from the clear pulse, while the small bump around 90 ns is from the charge transfer into the back gate of the SiSeRO. The slight variation between the 50 waveforms can be seen. Right - Root-mean-square variation of the sample points across the 50 waveforms after each waveform has been clamped at the baseline level. Two successive waveforms are shown to illustrate the evolution across pixels. Variation is low at the baseline level where the video waveform is clamped and increases left and right from this point. The charge clear pulse has no effect on the sample variation and no KTC noise bump is visible.

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the signal measurement can use not only the baseline level before the signal but also the baseline level after the signal, or both. This technique of using both baseline levels increases the effective integration time for the digital CDS baseline and reduces the noise without a decrease in pixel rate: in our measurement, we achieved \(6.2 \, e_{\text{RMS}}\) noise for a classical digital CDS at 625 kPix/sec rate, while the noise improved to \(5.0 \, e_{\text{RMS}}\) by using the baseline before and after the signal (at the same 625 kPix/sec rate). Figure 9 shows the resulting X-ray spectrum from a Fe55 source. Based on this (almost) perfect transfer of the signal charge into and out of the back gate of the transistor we investigated repetitive non destructive readout (RNDR) techniques which can further improve the noise performance (at the expense of increased readout time): With nine repetitive readout cycles we achieve an noise as low as \(2 \, e_{\text{RMS}}\). Details and further results can be found in.\(^{11}\) Once this technique is refined and reaches sub-electron noise levels, it could be of considerable advantage for the (in-situ) calibration of X-ray detectors.\(^{12}\)

Figure 9: The X-ray spectrum of a \(^{55}\)Fe radioactive source for single-pixel (grade 0) events measured at 625kPix/sec. As the SiSeRo device is KTC noise free, the measurement uses the baseline regions before and after the signal to estimate the baseline for improved noise performance (5 \(e_{\text{RMS}}\)).

5. CONCLUSION

Substantial progress has been made by our Stanford and MIT team to increase the frame rate of state-of-the-art X-ray CCD technology. We follow a two-pronged approach, working to increase both the readout speed of individual outputs and the number of outputs per CCD. We have demonstrated operation of MIT-LL CCID85 JFET output stages at 4 MPIX/sec per channel using discrete electronics, maintaining a spectral resolution of better than 150 eV FWHM for the 5.9 keV line. Improved output stages exhibit twice the conversion gain of the CCID85 and correspondingly improved noise performance: \(2.6 \, e_{\text{RMS}}\) at 2.0 MPix/sec.\(^{6}\) To support multi-output CCDs, we have developed a dedicated readout ASIC, the MCRC V1 ASIC, which has 8 readout channels capable of operating at high speeds with modest power consumption. Full functionality of the MCRC V1 ASIC has been demonstrated,\(^{8}\) and tests of the paired 8-channel MIT-LL CCID89 + MCRC V1 ASIC are scheduled for this fall.\(^{9}\) In addition, we are investigating a novel detector technology manufactured at MIT Lincoln Laboratory, the Single electron Sensitive Read Out (SiSeRO) that, while not yet (quite) capable of single electron noise performance, offers a promising pathway to very low noise, high speed X-ray detectors. We have demonstrated that this output stage is KTC noise free and capable of repetitive nondestructive readout (RNDR).\(^{11}\)
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