Phase polynomials synthesis algorithms for NISQ architectures and beyond

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Abstract

We present a framework for the synthesis of phase polynomials that addresses both cases of full connectivity and partial connectivity for NISQ architectures. In most cases, our algorithms generate circuits with lower CNOT count and CNOT depth than the state of the art or have a significantly smaller running time for similar performances. We also provide methods that can be applied to our algorithms in order to trade an increase in the CNOT count for a decrease in execution time, thereby filling the gap between our algorithms and faster ones.

1 Introduction

Quantum circuits optimization is essential to foster the practicability and efficiency of quantum computation. In particular, to cope with the much-needed compactness of quantum circuits, the synthesis of reversible circuits is being studied thoroughly. Because the $T$ gate has a high fault-tolerant implementation cost [1], much work has been put into the minimization of the $T$-count [2–9] and the $T$-depth [10–13]. In contrast, the CNOT gate has a low implementation cost as it is part of the Clifford group [14]. Nonetheless, the usage of metrics based on the $T$ gate have limitations, it turns out that the number of CNOT gates in a circuit is a metric that should not be overlooked as it can have a significant impact on the implementation cost of a circuit [15].

On top of that, quantum computers in the Noisy Intermediate Scale Quantum (NISQ) era [16] have architectural constraints. Concretely, the qubits within these computers are not connected in an all-to-all manner. It implies that logical gates having an arity of 2, such as CNOT gates, can only be applied between certain pairs of qubits. Thus, making a circuit compliant with a given architecture inevitably causes an increase in the CNOT count [17].

A common way of dealing with architectural constraints is to insert SWAP gates to route logical qubits [18–21]. An alternative is to perform architecture-aware synthesis [22], a method which often produces circuits with a much lower CNOT count while satisfying the architectural constraints. This approach is typically applied on subsets of circuits that can be represented by high-level constructs such as linear reversible functions. These circuits can then be put together to form a complete architecture compliant quantum circuit [23,24]. An important building block in this compilation scheme is the synthesis of circuits composed exclusively of CNOT and $R_Z$ gates. These circuits can be represented by a high-level construct called phase polynomials. In this work we tackle the phase polynomials synthesis problem and propose efficient algorithms for both cases of restricted and complete connectivity.
State of the art. In [25], a SAT-based algorithm that optimally solves the phase polynomials synthesis problem is proposed. Although this method offers good results regarding the CNOT count, it has an exponential complexity since the SAT problem is NP-complete and is therefore only practical for the synthesis of small phase polynomials. An efficient heuristic algorithm for phase polynomials synthesis is provided by Amy et al. in [26]. This algorithm, named Gray-Synth, is inspired by Gray code [27] and is considered as the current state of the art. There exists numerous other algorithms for phase polynomials synthesis. Some of them don’t have CNOT minimization as primary objective, as it is the case of the $T_{\text{par}}$ algorithm [11] that aims to parallelize the phase gates of a phase polynomial. This is also the case, with a lower degree, in [28] where automated methods for the optimization of large quantum circuit are given. As their algorithm scales similarly to the Gray-Synth algorithm and is purposely designed for specific circuits, we will prefer to compare our algorithm with the Gray-Synth algorithm.

Regarding the complexity of the problem, the results presented in [29] lead us to think that it is intractable. The same authors of the Gray-Synth algorithm corroborate this idea by proving the NP-completeness of the problem in some restricted cases [26].

Qubit routing could be used to make the Gray-Synth algorithm compliant with constrained architectures. This idea was developed and greatly refined by Nash et al. [30], and a modified version of their algorithm has been implemented in the Staq toolkit [31]. An altered version of this algorithm was also recently incorporated by Gheorghiu et al. in a slice-and-build algorithm that optimizes a given quantum circuit while taking into account the connectivity constraints imposed by the physical hardware architecture [24]. In a recent work and with a similar goal, a framework composed of greedy architecture-aware synthesis routines for the compilation of quantum circuits was presented in [23].

A phase polynomial is partially composed of a set of parities which can be stored in a parity table. As explained in [26], a circuit in which each parity occurs at least once is called a parity network and can be easily modified in order to implement the corresponding phase polynomials. In all parity network synthesis algorithms the parities are synthesized in an established order, we refer to this order as the parity ordering. In the Gray-Synth algorithm [26] this ordering is inspired by Gray code. Most of the parity network synthesis algorithms for arbitrary connectivity follow this idea and are based on the Gray-Synth algorithm. Yet, while the parity ordering defined by the Gray-Synth algorithm is efficient for all-to-all connectivity, it may be unfitted for arbitrary connectivity. Indeed, most Gray-Synth based algorithms for arbitrary connectivity are not taking the architecture into account when establishing the parity ordering [24, 30, 31]. In other words, the choice of the next parity to synthesize is solely based on the parity table, without taking into account the underlying graph of the architecture. An algorithm proposed by Arianne Meijer-van de Griend and Ross Duncan [32] aims to solve this shortcoming by recursively considering only non-cutting vertices of the underlying graph. However this algorithm is still based on the parity ordering of the Gray-Synth algorithm which is foremostly designed for all-to-all connectivity.

Our approach. In this paper we present an efficient alternative to the Gray code inspired parity ordering that yields better results in both cases of all-to-all connectivity and constrained architectures. In our approach, the parity ordering is defined by a two steps iterative process. The first step consists in choosing a parity and the second one corresponds to the synthesis of the chosen parity, we iterate until all parities have been synthesized. Here the parity choice is not bound to a parity ordering uniquely defined upon the parity table as it is the case for Gray code inspired methods, but can also take into account an arbitrary connectivity. In fact, we will see that this method can be easily adapted to constrained architectures by relying on the commonly used notion of Steiner tree. This extension to constrained architectures induces an important time cost,
nevertheless we will present some techniques to significantly reduce the running time of our algorithm while preserving an important CNOT count reduction when compared to the state of the art.

**Outline.** This paper is organized as follows. Section 2 introduces the circuit-polynomial correspondence for quantum circuits over the \{CNOT, R_z\} gate set. In Section 3 we present our heuristic algorithm for the synthesis of phase polynomials in the case of full connectivity. In Section 4 we extend our algorithm for partial connectivity and we give methods to lower the complexity of our approach. Benchmarks are given at the end of Sections 3 and 4.

**2 Phase polynomials synthesis**

Let \( C \) be a quantum circuit operating over \( n \) qubits and composed of CNOT and \( R_z \) gates. Such circuit can be best described by exploiting the circuit-polynomial correspondence \[33, 34\], which associates a phase polynomial and a linear reversible function to \( C \). The action of \( C \) on a basis state has the form

\[
|\mathbf{x}\rangle \mapsto e^{2\pi i p(\mathbf{x})} |g(\mathbf{x})\rangle
\]

where \( g : \mathbb{F}_2^n \rightarrow \mathbb{F}_2^n \) is a linear reversible function and

\[
p(\mathbf{x}) = \sum_{i=1}^{2^n} \theta_i f_i(\mathbf{x})
\]

is a linear combination of linear Boolean functions \( f_i : \mathbb{F}_2^n \rightarrow \mathbb{F}_2 \). Any linear Boolean function \( f_i \) can be written as

\[
f_i(\mathbf{x}) = \mathbf{y}^i \cdot \mathbf{x} = y_1^ix_1 \oplus y_2^ix_2 \oplus \ldots y_n^ix_n
\]

where \( \mathbf{y}^i \in \mathbb{F}_2^n \) and \( \oplus \) stands for the XOR operation. The function \( p(\mathbf{x}) \) is the phase polynomial associated with \( C \), and we will refer to the Boolean vectors \( \mathbf{y}^i \) as the parities of the phase polynomial \( p(\mathbf{x}) \). For instance, the circuit represented Figure 1 performs the mapping

\[
|x_1, x_2, x_3, x_4\rangle \mapsto e^{i p(x_1, x_2, x_3, x_4)} |x_1 \oplus x_2 \oplus x_3, x_1 \oplus x_3 \oplus x_4, x_3, x_4\rangle
\]

where \( p(x_1, x_2, x_3, x_4) = \theta_1(x_1 \oplus x_2) + \theta_2(x_1 \oplus x_2 \oplus x_3) + \theta_3(x_1 \oplus x_3 \oplus x_4) \). The parities of a phase polynomial can be described by a matrix where each line represents a qubit and each column represents a parity having an associated angle not equal to 0, we call this matrix the parity table of the phase polynomial and we denote it \( P \). In our example, the parity table of the phase polynomial is

\[
P = \begin{pmatrix}
1 & 1 & 1 \\
1 & 1 & 0 \\
0 & 1 & 1 \\
0 & 0 & 1
\end{pmatrix}.
\]

Performing the synthesis of the phase polynomial \( p(\mathbf{x}) \) and the linear reversible function \( g(\mathbf{x}) \) amounts to constructing a circuit equivalent to \( C \). The synthesis of linear reversible functions is a well studied problem as there exists asymptotically optimal methods \[35\], as well as efficient heuristic algorithms in both cases of partial and full connectivity \[36, 37\]. For that reason we will put aside the problem of synthesizing the linear reversible function \( g(\mathbf{x}) \), and we will focus on the phase polynomials synthesis problem.

**Parity networks.** Following Amy et al. \[26\], we tackle the phase polynomials synthesis problem via the parity network formalism.
Definition 1 (Parity network). A parity network for a parity table $P$ is a CNOT circuit in which each parity $y \in P$ appears at least once.

The $R_z$ gate only modifies the phase and doesn’t affect the logical value of the qubit. Therefore, a parity network can be easily modified by exclusively inserting $R_z$ gates to implement any phase polynomial associated with the parity table $P$. It implies that the phase polynomials synthesis problem can be reduced to the parity network synthesis problem. For the remaining of this paper we will consider the parity network synthesis problem and ignore the rotation gates in order to focus on the core of the problem.

Recall that a CNOT gate performs the mapping $|x_i⟩|x_j⟩ \rightarrow |x_i⟩|x_i \oplus x_j⟩$. When applying a CNOT $x_i,x_j$ gate where $x_i$ is the control qubit and $x_j$ is the target qubit, the parity table can be expressed in the new basis by performing the row addition $P_i = P_i \oplus P_j$. It follows that a parity $y \in P$ is being carried out by a qubit if it satisfies $\sum_{i=1}^{n} y_i = 1$.

3 Parity network synthesis for all-to-all connectivity

3.1 An efficient heuristic algorithm

In this section we formalize a heuristic algorithm for phase polynomials synthesis in all-to-all connectivity. Our algorithm is presented in pseudo-code in Algorithm 1 and an example is provided in Figure 2. The term CNOT $x_i,x_j$ refers to a CNOT gate with control $i$ and target $j$ and we define the function $h$ as the Hamming weight of a binary vector or binary matrix, i.e. $h(y) = \sum_{i=1}^{n} y_i$ where $y \in \mathbb{F}_2^n$ and $h(P) = \sum_{y \in P} h(y)$ where $P$ is a parity table. Let $S$ be a sequence of row additions, we denote by $y^S$ (resp. $P^S$) the state of $y$ (resp. $P$) after applying the sequence of additions in $S$ onto $y$ (resp. $P$). Our algorithm follows a two steps iterative process:

1. Choose a parity $y \in P$.

2. Perform the synthesis of $y$. Remove $y$ from $P$ and go to step 1.

Step 1. To know which parity $y \in P$ it would be judicious to choose in step 1 of our algorithm we first reflect on the minimum CNOT cost induced by the synthesis of $y$. Let $S_y$ be the set of minimum length sequences of additions such that for all $S \in S_y$ we have $h(y^S) = 1$. In other words, $S_y$ contains all minimum length sequences of additions that effectively synthesize $y$. Note that one addition can reduce the value of $h(y)$ by at most 1. That being so, it is clear that the length of all $S \in S_y$ is equal to $h(y) - 1$, implying a minimum CNOT cost of $h(y) - 1$ for the synthesis of $y$. Based on this fact it is rather intuitive to choose the parity $y$ for which $h(y)$ is minimum for the step 1 of our algorithm.
Step 2. We are left with the second step of the algorithm that raises the following question: which sequence \( S \in S_y \) of additions should we choose to perform the synthesis of \( y \)? A natural choice would be to select the sequence \( S \in S_y \) that minimizes the value \( h(P^S) \). However we are faced with a challenge as the size of \( S_y \) is exponential with respect to \( h(y) \). In fact, we will see that the size of \( S_y \) is greater than the number of spanning arborescences in a complete directed graph composed of \( h(y) \) vertices. We define this graph as follows.

**Definition 2** (Parity graph). Let \( P \) be a parity table and \( y \) be a parity of \( P \), the parity graph associated with \( y \) is the complete directed graph \( G_y = (V, A) \) where \( V = \{ i \mid y_i = 1 \} \) and where each arc \((i, j) \in A\) going from \( i \) to \( j \) is weighted by \( w_{i,j} = h(P_i \oplus P_j) - h(P_j) \).

Let \( X \) be a spanning arborescence of \( G_y \), note that \( X \) is composed of \( h(y) - 1 \) arcs. For each arc \( (i, j) \in X \) going from \( i \) to \( j \) we associate the addition \( P_j = P_j \oplus P_i \). Now consider a successors-first traversal of \( X \) as defined below.

**Definition 3** (Successors-first traversal). A traversal of an arborescence \( X \) is a successors-first traversal if and only if for every vertex \( i \) in \( X \) the successors of \( i \) in \( X \) are visited before \( i \).

For example, the traversal resulting from a depth-first search postordering is a successors-first traversal. We can construct a sequence \( S \) of additions by following the order of this traversal: if \( j \) is the currently visited vertex then we append to \( S \) the addition associated with the unique arc \((i, j) \in X \) going from \( i \) to \( j \). The length of \( S \) is equal to \( h(y) - 1 \) and \( h(S^S) = 1 \), thus \( S \in S_y \) and we say that \( X \) is the spanning arborescence associated with \( S \). A different successors-first traversal would give us a different sequence of additions for the same spanning arborescence \( X \), and for every sequence \( S \in S_y \) there is a corresponding spanning arborescence in \( G_y \). Hence there is a surjection between \( S_y \) and the set of spanning arborescences in \( G_y \), in particular we have \( |S_y| \geq |\{ X \mid X \text{ is a spanning arborescence of } G_y \}| = n^{n-1} \) where \( n = h(y) \). As a result we have to choose \( S \in S_y \) among an exponential number of possibilities.

To cope with this problem we can first notice that if two sequences \( S_i, S_j \) are associated with the same arborescence, then they are equivalent in the sense that \( P^{S_i} = P^{S_j} \). As our only metric is the number of CNOT we don’t make any distinction between these equivalent sequences, and we can equivalently refer to \( S \in S_y \) or its associated spanning arborescence in \( G_y \). Recall that each arc \((i, j) \in A\) going from \( i \) to \( j \) is weighted by \( w_{i,j} = h(P_i \oplus P_j) - h(P_j) \), then we have

\[
h(P^S) = h(P) + \sum_{(i,j) \in X} h(P_i \oplus P_j) - h(P_j) = h(P) + \sum_{(i,j) \in X} w_{i,j}
\]

where \( S \in S_y \) and \( X \) is the spanning arborescence associated with \( S \) in \( G_y \). In consequence, minimizing \( h(P^S) \) amounts to minimizing \( \sum_{(i,j) \in X} w_{i,j} \), which is optimally satisfied when \( X \) is the minimum weight spanning arborescence of \( G_y \). The minimum weight spanning arborescence problem is a well-known problem, an algorithm proposed by Robert Endre Tarjan \[38\] solves it with a complexity of \( \mathcal{O}(|V|^2) \) for complete graphs where \( |V| \) is the number of vertices.

**Correctness and complexity.** Let \( P \) be a parity table of size \( n \times m \). Our algorithm terminates when \( P \) is empty and a parity \( y \in P \) is removed from \( P \) at each iteration. Therefore our algorithm performs \( m \) iterations and finishes. The algorithm starts with an empty circuit \( C \) and at each iteration \( C \) is extended to synthesize a parity \( y \in P \) not yet occurring in \( C \). Hence the constructed circuit \( C \) is a parity network for \( P \) and our algorithm is correct.

Choosing the parity in the step 1 of our algorithm has a cost of \( \mathcal{O}(mn) \). For the step 2, constructing the graph \( G_y \) has a complexity of \( \mathcal{O}(mn^2) \), whereas computing its minimum weight
spanning arborescence and performing the for loop over the depth-first search both have a smaller complexity of $O(n^2)$ and $O(mn)$ respectively. Both steps are performed $m$ times so the overall complexity of our algorithm is $O(m^2n^2)$.

**Algorithm 1: Parity network synthesis**

**Input:** Parity table $P$

**Output:** Circuit synthesizing a parity network associated with $P$

1. $C \leftarrow$ new empty circuit
2. while $P$ non-empty do
3. \hspace{1em} $y \leftarrow \min \argmin \{h(y) \mid y \in P\}$
4. \hspace{1em} $P \leftarrow P \setminus y$
5. \hspace{1em} $G_y \leftarrow (\{i \mid y_i = 1\}, \{(i, j, h(P_i \oplus P_j) - h(P_j)) \mid y_i = 1, y_j = 1, i \neq j\})$
6. \hspace{1em} $X \leftarrow$ MinimumWeightSpanningArborescence($G_y$)
7. \hspace{1em} for $i \in$ DepthFirstSearchPostordering($X$) do
8. \hspace{2em} $j \leftarrow$ direct predecessor of $i$ in $X$
9. \hspace{2em} $C \leftarrow C :: CNOT_{i,j}$
10. \hspace{2em} $P_i \leftarrow P_i \oplus P_j$
11. \hspace{1em} end
12. end
13. return $C$

![Figure 2: Example for 1 iteration of Algorithm 1. The chosen parity $y$ is represented in bold.](image-url)

(a) Parity table and graph $G_y$. The minimum weight spanning arborescence of $G_y$ is represented by bold arcs.

(b) State of the parity table after the synthesis of $y$, the additions performed are $P_5 = P_5 \oplus P_2$ and $P_2 = P_2 \oplus P_3$. And circuit corresponding to the synthesis of $y$ with respect to the minimum weight spanning arborescence of $G_y$. 

Figure 2: Example for 1 iteration of Algorithm 1. The chosen parity $y$ is represented in bold.
Further optimizations. The parity $y$ selected in the step 1 of our algorithm satisfies $y = \text{argmin}\{h(y) \mid y \in P\}$. Yet it often arises that multiple parities satisfy this property. A second selection criteria is needed in order to choose among these parities. After experimenting with different methods, we found that what gives the best results is to simply choose the parity representing the smallest integer. This way the parities will be ordered according to their most significant bit as it is done in [29], and the parities will be processed in an order analogous to the Gray code. As a result and in the same manner as the Gray-Synth algorithm, our algorithm is optimal when the given parity table contains all possible parities.

As previously mentioned, if two sequences $S_i, S_j$ are associated with the same spanning arborescence $X$, then they are equivalent in the sense that $P^{S_i} = P^{S_j}$. Nonetheless, the circuits produced by $S_i$ and $S_j$ can have different depths. Thus, by choosing wisely among these equivalent sequences we could enhance the depth performances of our algorithm without affecting the CNOT count of the outputed circuit. This opportunity is interesting as depth is often considered as a second metric in CNOT circuits synthesis. Despite that, we decided not to implement such optimization as finding the depth-optimal traversal of $X$ induces a computational overhead. As a side note, we want to mention that one could also prioritize depth minimization over CNOT count minimization by finding the sequence of additions $S$ that minimizes $h(P^S)$ among all the sequences in $S_y$ with a corresponding CNOT circuit of depth $\lceil \log_2 h(y) \rceil$.

3.2 Benchmarks

For a parity table $P$ of size $n \times m$ we call density the value $100 \times \frac{m}{2^n - 1}$, which is the percentage representation of the ratio between the number of parities in $P$ and the number of possible parities for $n$ qubits. To evaluate the performances of our algorithm we generate random parity tables for 7, 10, 13 and 16 qubits with a density varying from 1% to 100%. We compare our results to the state of the art, namely the Gray-Synth algorithm [26] and the Lazy-Synth framework [23]. Throughout this paper, we have always set the Lazy-Synth depth parameter to 3 for its recursive search. Our algorithm as well as the Gray-Synth algorithm have been implemented in Python whereas the Lazy-Synth algorithm has been implemented in C++. The standard deviation $\sigma$ is not represented in our benchmarks as it is particularly low ($\sigma < 10^{-2}$).

We first discuss the CNOT count and depth performances of our algorithm in comparison to the Gray-Synth algorithm as presented in Figure 3. As expected, both algorithms are optimal for full density parity tables. That being said, our algorithm has a better CNOT depth than the Gray-Synth algorithm for all other densities and it also has a better CNOT count for all parity tables with a density between 1% and 95%. Moreover, we observe that the percentage of CNOT gained over the Gray-Synth algorithm increases as the number of qubits gets larger. It is therefore reasonable to project that our algorithm outperforms the Gray-Synth algorithm for all phase polynomials acting on larger number of qubits and whose parity table has a density between 1% and 95%.

As it can be seen in Figure 4 for 10 and 13 qubits the Lazy-Synth algorithm is solving the parity network synthesis problem with less CNOT than our algorithm for parity tables having a density under 50%. However, this performance gap never exceeds 6% and comes with a tremendous time cost. The runtimes for the 3 algorithms are shown in Table 1 we weren't able to execute the Lazy-Synth algorithm for 16 qubits due to its important computational time. As expected by the complexity analysis, our algorithm is slower than the Gray-Synth algorithm but still has a decent enough running time to be applied on large parity tables. We provide methods to further reduce the running time of our algorithm while preserving good performances in Section 4.3. Also, the
complexity of our algorithm is majored by the creation of the graph $G_y$, yet this task can be easily parallelized to significantly reduce the computational time of the algorithm.

We also performed benchmarks on much lower densities in order to test our algorithm on a higher number of qubits, the results are depicted in Figure 5. We can see that our algorithm still offers a significant CNOT reduction when compared to the Gray-Synth algorithm for higher number of qubits. Interestingly, the CNOT count ratio is increasing when the number of qubits increases while the CNOT depth ratio does the opposite. The computational times for this setting are shown in Table 2. In a similar way as in Table 1, we can see that the computational time of our algorithm grows faster than the computational time of the Gray-Synth algorithm as the size of the parity table increases.

Overall, with regards to the CNOT metrics, our algorithm offers much better results than the Gray-Synth algorithm and its performances are similar to the Lazy-Synth algorithm but with a viable execution time for large phase polynomials, thus achieving an efficient performance over time ratio.

Figure 3: CNOT count and depth of the circuits generated by our algorithm divided by the CNOT count and depth of the circuits outputed by the Gray-Synth algorithm. Each point is averaged over 1000, 100, 10 and 10 randomly generated parity tables for 7, 10, 13 and 16 qubits respectively.

Figure 4: CNOT count and depth of the circuits generated by our algorithm divided by the CNOT count and depth of the circuits outputed by the Lazy-Synth algorithm. Each point is averaged over 1000, 100, 10 and 10 randomly generated parity tables for 7, 10, 13 and 16 qubits respectively.
Table 1: Average computational time in seconds of the Gray-Synth algorithm, the proposed algorithm and the Lazy-Synth algorithm.

| Density | 7 qubits | 10 qubits | 13 qubits | 16 qubits |
|---------|----------|-----------|-----------|-----------|
|         | Gray-Synth | Proposed | Lazy-Synth |          | Gray-Synth | Proposed | Lazy-Synth |          | Gray-Synth | Proposed | Lazy-Synth |
| 1%      | 0.006     | 0.011     | 0.045     |          | 0.058     | 0.094     | 0.798     |          | 0.583     | 0.839     |          |
| 20%     | 0.007     | 0.018     | 0.056     |          | 0.079     | 0.156     | 1.393     |          | 0.775     | 1.606     | 94.539    |          | 8.909     | 37.710    |
| 40%     | 0.011     | 0.032     | 0.113     |          | 0.111     | 0.303     | 4.283     |          | 1.167     | 3.708     | 329.136   |          | 19.042    | 119.998   |
| 60%     | 0.015     | 0.048     | 0.185     |          | 0.146     | 0.447     | 8.729     |          | 1.622     | 6.541     | 688.243   |          | 30.944    | 253.264   |
| 80%     | 0.017     | 0.063     | 0.279     |          | 0.176     | 0.591     | 14.985    |          | 2.030     | 10.121    | 1195.277  |          | 43.895    | 431.766   |
| 100%    | 0.020     | 0.078     | 0.380     |          | 0.201     | 0.751     | 22.193    |          | 2.402     | 14.143    | 1748.428  |          | 56.923    | 652.193   |

Figure 5: CNOT count and depth of the circuits generated by our algorithm divided by the CNOT count and depth of the circuits outputed by the Gray-Synth algorithm. The number of parities ranges from 1% of $n^2$ to $n^2$ where $n$ is the number of qubits. Each point is averaged over 100 randomly generated parity tables.

Table 2: Average computational time in seconds of the Gray-Synth algorithm and the proposed algorithm for $n^2$ parities where $n$ is the number of qubits.

| Algorithm | 20 qubits | 30 qubits | 40 qubits | 50 qubits | 60 qubits |
|-----------|-----------|-----------|-----------|-----------|-----------|
| Gray-Synth | 0.749     | 3.696     | 13.406    | 30.7      | 71.3      |
| Proposed  | 0.815     | 4.924     | 22.598    | 81.2      | 243       |

4 Parity network synthesis for partial connectivity

Many synthesis algorithms are first designed for all-to-all connectivity before being adapted to the case of partial connectivity. We follow the same process in this work and now demonstrate how our algorithm can be extended to perform architecture-aware synthesis.

4.1 Extending the heuristic function

As we have seen in Section 3.1 in the case of all-to-all connectivity the cost function $C : F_2^n \rightarrow \mathbb{N}$ that gives the minimum CNOT cost for the synthesis of a parity $y$ is equal to $h(y) - 1$. This is utterly incorrect in the case of partial connectivity as the function $h$ doesn’t even take into account the connectivity graph of the architecture. Hence, to extend our algorithm for constrained
architectures we first need to determine the value of our heuristic function \( C \) for the case of partial connectivity. For this purpose we will rely on Steiner trees, which are commonly used when it comes to designing architecture-aware synthesis algorithms \([22, 24, 30, 31]\).

**Steiner trees.** Given a graph \( G = (V,E) \) and a set of vertices \( S \subseteq V \), the Steiner tree problem consists of finding the minimum tree \( T = (V_T, E_T) \), called Steiner tree, such that \( T \) is a subgraph of \( G \) and \( S \subseteq V_T \). The vertices in \( S \) are called terminals and the vertices in \( V_T \setminus S \) are called Steiner nodes. To perform the synthesis of a parity \( y \), a Steiner tree is required since we must interconnect the vertices in \( S = \{i \mid y_i = 1\} \). Once the Steiner tree \( T \) is computed, two steps must be carried out:

1. Fill-in all Steiner nodes such that for all \( u \in V_T \) we have \( y_u = 1 \).
2. Perform the sequence of additions associated with a successors-first traversal of any spanning arborescence of \( T \).

An example of this process is given Figure 6 and the pseudo-code to perform the fill-in step is provided in Algorithm 2. We use the notation \( G[X] \) to refer to the induced subgraph of \( G \) formed by the subset of vertices \( X \). For the second step it is exactly the same procedure as the for loop in Algorithm 1 for an arbitrary spanning arborescence of \( T \). The fill-in step requires \( |V_T \setminus S| \) additions and the second step takes \( |V_T| - 1 \) additions, hence the total CNOT cost for the synthesis of \( y \) is \( C(y) = |V_T \setminus S| + |V_T| - 1 = 2|V_T| - |S| - 1 \). Solving optimally the Steiner tree problem would minimize \( C(y) \), unfortunately finding the minimal Steiner tree is NP-hard \([40]\). We will therefore rely on an approximation algorithm proposed by Takashashi et al. \([41]\) that has an approximation ratio of \( 2 - 2/|S| \). The algorithm is presented in pseudo-code in Algorithm 3; it starts by adding an arbitrary vertex of \( S \) to the Steiner tree \( T \) and then constructs \( T \) by iteratively adding the shortest path between \( T \) and one vertex of \( S \) not yet in \( T \). Its runtime is \( O(|S||V|^2) \), although it can be lowered to \( O(|V|^2) \) if all the shortest paths are provided.

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**Algorithm 2: Arbitrary fill-in**

1. procedure FillIn\( (T, S) \)
2. \( C \leftarrow \) new empty circuit
3. \( F \leftarrow T[V_T \setminus S] \)
4. while \( F \) non-empty do
5. \hspace{1em} \( u \leftarrow \) a leaf of \( F \)
6. \hspace{1em} \( v \leftarrow \) any vertex in \( S \cap T.\text{neighbors}(u) \)
7. \hspace{1em} \( C \leftarrow C :: \text{CNOT}_{u,v} \)
8. \hspace{1em} \( S \leftarrow S \cup \{u\} \)
9. \hspace{1em} \( F \leftarrow F[V_F \setminus \{u\}] \)
10. end
11. return \( C \)
Algorithm 3: Steiner tree

1 procedure SteinerTree(S, paths)
2     u ← any vertex in S
3     S ← S \ {u}
4     T ← Graph({u}, Ø)
5     while S non-empty do
6         u,v ← argmin_{u,v} |paths_{u,v}|, u ∈ T, v ∈ S
7         T ← T ∪ paths_{u,v}
8         S ← S \ {v}
9     end
10    return T

Figure 6: Synthesis example for the parity \( x_1 \oplus x_6 \oplus x_8 \oplus x_{10} \) on a grid architecture. The gray nodes are the terminals and the Steiner tree is represented by bold edges. The chosen root for the spanning arborescence is the vertex 1.

4.2 Architecture-aware algorithm

In this section we present an architecture-aware version of Algorithm 1 by relying on the heuristic function \( C \) defined in Section 4.1. The pseudo-code of the algorithm is provided in Algorithm 4. We reuse some notations of Section 3.1: \( P \) is a parity table, \( y \) is a parity of \( P \) and \( G_y \) is the parity graph associated with \( y \). We define \( P^X \) as being the state of the parity table \( P \) after performing the sequence of additions associated with any successors-first traversal of the arborescence \( X \). We denote by \( T_y \) the Steiner tree of \( y \) where the terminals are the vertices in the set \( S = \{ i \mid y_i = 1 \} \).

We consider again the two steps process described in Section 3.1 and modify it to take into account the architecture’s connectivity. Namely, we choose the parity \( y \) that minimizes \( C(y) \) and we perform the synthesis of \( y \) in an architecture-aware manner such as described in Section 4.1. In most cases, the number of minimum size fill-in of \( T_y \) is exponential with respect to the number of terminals. As we want our algorithm to be scalable we get over this step by doing an arbitrary fill-in as presented in Algorithm 2. Then, we must perform the sequence of additions associated with a successors-first traversal of any spanning arborescence \( X \) of \( T_y \). Our heuristic function \( C \) isn’t merely based on the Hamming weight anymore, it implies that we cannot rely again on the minimum weight spanning arborescence to choose among the spanning arborescences of \( T_y \) as we have done in Section 3.1. However, since \( T_y \) is a tree it only has \( |V_{T_y}| \) different spanning
arborescences (a tree can have exactly one spanning arborescence rooted at each of its vertices),
we can compute all the possibilities to choose the one that gives the best results and still have a
polynomial time algorithm.
Let \( c^X = \text{sort} \{ C(y) \mid y \in P^X \} \) be the cost vector sorted in ascending order with respect to
a spanning arborescence \( X \) of \( T_y \). As we don’t rely on the minimum weight spanning arbores-
cence anymore, we are not compelled to choose the spanning arborescence \( X \) of \( T_y \) that minimizes
\( \sum_{y \in P^X} C(y) \). Our experiments have shown that choosing the spanning arborescence \( X \) of \( T_y \) such
that \( c^X_1 \) is minimal leads to better results. If several arborescences satisfy this property then we
choose among them by taking the spanning arborescence \( X \) such that \( c^X_2 \) is minimal. We repeat
the process for \( c^X_i \) where \( i \in [3, \ldots, m] \) until we only have one spanning arborescence left or until
the end of the cost vectors is reached. The chosen spanning arborescence \( X \) of \( T_y \) then satisfies
\[
X = \arg\min \{ c^X \mid X \text{ is a spanning arborescence of } T_y \}
= \arg\min \{ \text{sort} \{ C(y) \mid y \in P^X \} \mid X \text{ is a spanning arborescence of } T_y \}.
\]

Algorithm 4: Architecture-aware parity network synthesis

**Input:** A parity table \( P \) and a connectivity graph \( G \)

**Output:** Circuit synthesizing a parity network associated with \( P \) and compliant with the
architectural constraints described by \( G \)

1. \( C \leftarrow \text{new empty circuit} \)
2. \( \text{paths} \leftarrow \text{ShortestPaths}(G) \)
3. while \( P \) non-empty do
   4. \( y \leftarrow \arg\min \{ C(y) \mid y \in P \} \)
   5. \( P \leftarrow P \setminus y \)
   6. \( S \leftarrow \{ i \mid y_i = 1 \} \)
   7. \( T \leftarrow \text{SteinerTree}(S, \text{paths}) \)
   8. for \( \text{CNOT}_{i,j} \in \text{FillIn}(T, S) \) do
      9. \( P_i \leftarrow P_i \oplus P_j \)
     10. \( C \leftarrow C :: \text{CNOT}_{i,j} \)
   end
   12. \( X \leftarrow \arg\min \{ \text{sort} \{ C(y) \mid y \in P^X \} \mid X \text{ is a spanning arborescence of } T \} \)
   13. for \( i \in \text{DepthFirstSearchPostordering}(X) \) do
      14. \( j \leftarrow \text{direct predecessor of } i \text{ in } X \)
     15. \( C \leftarrow C :: \text{CNOT}_{i,j} \)
     16. \( P_i \leftarrow P_i \oplus P_j \)
   end
17 end
18 return \( C \)

**Complexity analysis.** Let \( n \) be the number of qubits and \( m \) the number of parities. Algorithm 3
compute the Steiner tree of a parity with a complexity of \(O(n^2)\). The complexity of Algorithm 4
is majored by the task of finding the optimal spanning arborescence \( X \), which takes \( O(mn^3) \) oper-
ations as it requires to compute \( O(mn) \) Steiner trees. The algorithm performs \( m \) iterations so the
overall complexity is \(O(m^2n^3)\). Some methods to further reduce the complexity of our algorithm
are described in Section 4.3.
Further optimizations. We refer to the implementation cost of a Steiner tree $T_y$ as the value $C(y)$. In most cases, in order to find the spanning arborescence $X$ satisfying $X = \operatorname{argmin}\{\text{sort}\{C(y) \mid y \in P^X\}\}$, we don’t actually need to know all the values of the vector $c^X$. Our experiments show that the CNOT performances of our algorithm doesn’t change when we only consider the $K = 10$ first values of $c^X$. Indeed, it is rather rare to have 2 arborescences $X_1$, $X_2$ such that $c^X_1 = c^X_2 \forall i \in [1, \ldots, K = 10]$. Also, when it happens, then choosing $X_1$ or $X_2$ doesn’t make a significant difference in the algorithm performances. Consequently, to determine the values $c^X_i \forall i \in [1, \ldots, K]$ for an arborescence $X$, we only have to compute the $K$ Steiner trees of $\{T_y \mid y \in P^X\}$ having a minimum implementation cost $C(y)$.

In order to find the $K$ minimum cost Steiner trees we propose an algorithm that simultaneously constructs all the Steiner trees and stops when the $K$ minimum cost Steiner trees are found. In this algorithm, only $K$ Steiner trees will be completely computed and all the others will be partially constructed, thus saving a considerable amount of time. The pseudo-code of the algorithm is given in Algorithm 5. It takes as input the shortest paths of the graph, an integer $K$ and a set $S$ of sets $S_1, \ldots, S_m$ of terminals from which we want to find the $K$ minimum cost Steiner trees.

**Algorithm 5: $K$ minimum cost Steiner trees**

1. **procedure** MinimumCostSteinerTrees($S$, $paths$, $K$)
2. \hspace{1em} $R \leftarrow$ new empty list
3. \hspace{1em} $L \leftarrow$ new list of empty stacks
4. \hspace{1em} $cost \leftarrow 0$
5. \hspace{1em} for $i \in \{1, \ldots, |S|\}$ do
6. \hspace{2em} $u \leftarrow$ any vertex in $S_i$
7. \hspace{2em} $S_i \leftarrow S_i \setminus \{u\}$
8. \hspace{2em} $T_i \leftarrow \text{Graph}(\{u\}, \emptyset)$
9. \hspace{2em} $L_0$.push($i$)
10. end
11. while $L$ non-empty do
12. \hspace{1em} $Q \leftarrow L$.popleft
13. \hspace{2em} while $Q$ non-empty do
14. \hspace{3em} $i \leftarrow Q$.pop
15. \hspace{3em} if $S_i$ is empty then
16. \hspace{4em} $R \leftarrow R :: (cost, T_i)$
17. \hspace{4em} if $|R| = K$ then
18. \hspace{5em} return $R$
19. \hspace{4em} end
20. \hspace{3em} end
21. \hspace{3em} $u, v \leftarrow \operatorname{argmin}_{u,v}\{|paths_{u,v}| \mid u \in T_i, v \in S_i\}$
22. \hspace{3em} $T_i \leftarrow T_i \cup paths_{u,v}$
23. \hspace{3em} $S_i \leftarrow S_i \setminus \{v\}$
24. \hspace{3em} $j \leftarrow 1 + 2 \times (|paths_{u,v}| - 2)$
25. \hspace{3em} $L_j$.push($i$)
26. \hspace{2em} end
27. \hspace{2em} $cost \leftarrow cost + 1$
28. end
29. return $R$
4.3 Lowering the complexity

In this section we describe some methods that can be applied to our algorithms in order to reduce their complexity and achieve the best trade-off possible between performances and running time constraints. We demonstrate these methods in the case of constrained architectures, although they can also be applied in the same way on Algorithm 4 for all-to-all connectivity.

**Greedy method.** For this method we consider a greedier version of Algorithm 4 by choosing an arbitrary spanning arborescence instead of the one satisfying $X = \text{argmin}\{\text{sort}\{C(y) \mid y \in P_X\}\}$. The algorithm then simply consists in choosing the parity $y$ minimizing $C(y)$, performing the synthesis of $y$ optimally and reiterating until all parities have been synthesized. The complexity of this algorithm is $O(m^2 n^2)$.

**Sliding window.** Another way of lowering the complexity of our algorithm is to only consider the parities that are in the range of a sliding window of size $\alpha$ that runs over the parity table. At each iteration of our algorithm the parity which has just been synthesized is removed from the window and another parity not yet considered is added to the window. With this method the complexity of our algorithm is lowered to $O(\alpha m n^3)$. By combining the greedy and sliding window methods, the complexity of the algorithm is further lowered to $O(\alpha m n^2)$.

4.4 Benchmarks

We compare our algorithms with the algorithm proposed by Meijer-van de Griend et al. [32], the phase polynomials synthesis algorithm implemented in Staq [31] and the Lazy-Synth algorithm [23]. Beside Algorithm 4, we benchmark 3 modified versions of it stemming from Section 4.3 with a sliding window of size 50, with the greedy method and with both the greedy method and a sliding window of size 50. All algorithms have been implemented in Python except for the Lazy-Synth algorithm which has been implemented in C++. The standard deviation $\sigma$ is not represented in our benchmarks as it is particularly low ($\sigma < 10^{-2}$).

Figure 7a compares the algorithms on a $3 \times 3$ grid with a density ranging from 1% to 100%. In this setting, our algorithm and the Lazy-Synth algorithm both offer the best CNOT performances, our algorithm being faster. In Figure 7b for the Melbourne architecture, the Lazy-Synth algorithm provides the best performances with regards to the CNOT metrics but has an important running time. All the variants of Algorithm 4 have a better CNOT count and CNOT depth than the algorithms proposed by Meijer-van de Griend et al. and Staq. Moreover, the greedy version with a sliding window of size 50 has a similar running time. We tested the algorithms on various architectures and didn’t notice any significant changes.

We also did benchmarks for a constant number of parities with an increasing number of qubits, the results are shown in Figure 8. We didn’t run the sliding window variants for this benchmark because their usefulness is limited by the small constant number of parities. We can notice that the algorithm proposed by Meijer-van de Griend et al. has a smaller CNOT depth than the other algorithms when the number of qubits is greater than 36, however it also has the worst CNOT count. Algorithm 4 and the Lazy-Synth algorithm are producing again the smallest circuits. Nevertheless, as it can be seen in Table 2, they both have a rapidly growing computational time. The greedy method seems to offer the best compromise. Indeed, it produces circuits with significantly better CNOT count than the algorithms proposed by Meijer-van de Griend et al. and Staq, and has a much more tolerable running time than Algorithm 4 and the Lazy-Synth algorithm.
Figure 7: Scaling of the circuit size, circuit depth and computational time on a $3 \times 3$ grid architecture and the 14 qubits IBM’s Melbourne architecture. Each point is averaged over 1000 randomly generated parity tables.
Figure 8: Scaling of the circuit size and circuit depth on square grids for 100 parities. Each point is averaged over 100 randomly generated parity tables.

Table 3: Average computational time in seconds on square grids for 100 parities.

| Algorithm                | Grid size |
|--------------------------|-----------|
|                          | 3 × 3     | 4 × 4     | 5 × 5     | 6 × 6     | 7 × 7     | 8 × 8     | 9 × 9     | 10 × 10   |
| Proposed                 | 0.303     | 1.439     | 5.763     | 18.650    | 50.745    | 137.250   | 339.595   | 768.073   |
| Greedy                   | 0.088     | 0.209     | 0.498     | 1.070     | 2.095     | 4.270     | 8.254     | 15.098    |
| Staq                     | 0.038     | 0.078     | 0.157     | 0.268     | 0.421     | 0.648     | 0.990     | 1.616     |
| Meijer-van de Griend et al. | 0.066 | 0.217     | 0.517     | 0.941     | 1.577     | 2.584     | 3.960     | 5.977     |
| Lazy-Synth               | 0.560     | 5.524     | 80.920    | 523.639   | 2381.802  | -         | -         | -         |

5 Conclusion

We presented heuristic algorithms for the synthesis of circuits over the \{CNOT, R_Z\} gate set. We covered both cases of full connectivity and partial connectivity for NISQ architectures. When compared to the state of the art, the benchmarks have shown that our algorithms are producing circuits of smaller or comparable size. State of the art algorithms yielding analogous CNOT count and CNOT depth performances are outperformed when it comes to the execution time.

Our framework could be further expanded by adding depth and width to our algorithms, which would result in an even smaller CNOT count at the cost of a runtime increase. This methods was utilized in the Lazy-Synth framework, instead of going in the same direction we presented methods to lower the complexity of our algorithms while preserving as much performances as possible, with the aim of providing a more comprehensive toolkit for the synthesis of phase polynomials.

Finally, the modularity of our approach makes it easily adaptable for the synthesis of other circuits such as sequences of Pauli rotations, a generalization of phase polynomials. This is not the case for the Gray-Synth algorithm and all its architecture-aware derivatives. Indeed, the Gray-Synth algorithm relies on the fact that the row \(j\) of the parity table isn’t affected when applying the gate \(CNOT_{i,j}\). This invariant isn’t true when considering sequences of Pauli rotations. Therefore the Gray-Synth algorithm needs to be coupled with phase polynomials extraction routines in order to compile a generic circuit.
Acknowledgments

This work was supported in part by the French National Research Agency (ANR) under the research project SoftQPRO ANR-17-CE25-0009-02, and by the DGE of the French Ministry of Industry under the research project PIAGDN/QuantEx P163746-484124.

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