Skydive: A Spiking Neural Network Accelerator Exploiting Spatio-Temporal Workload Balance

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Abstract—Spiking Neural Networks (SNNs) are developed as a promising alternative to Artificial Neural networks (ANNs) due to their more realistic brain-inspired computing models. SNNs have sparse neuron firing over time, i.e., spatio-temporal sparsity; thus, they are useful to enable energy-efficient hardware inference. However, exploiting spatio-temporal sparsity of SNNs in hardware leads to unpredictable and unbalanced workloads, degrading the energy efficiency. In this work, we propose an FPGA-based convolutional SNN accelerator called Skydive that exploits spatio-temporal workload balance. We propose the Approximate Proportional Relation Construction (APRC) method that can predict the relative workload channel-wisely and a Channel-Balanced Workload Schedule (CBWS) method to increase the hardware workload balance ratio to over 90%. Skydive was implemented on a Xilinx XC7Z045 FPGA and verified on image segmentation and MNIST classification tasks. Results show improved throughput by 1.4× and 1.2× for the two tasks. Skydive achieved 22.6 KFPS throughput, and 42.4 μJ/Image prediction energy on the classification task with 98.5% accuracy.

Index Terms—workload balance, spiking neural network, FPGA.

I. INTRODUCTION

OVER the past decade, the revolution of Deep Neural Networks (DNNs) has led to an impressive performance on various challenging tasks. However, such continuous-valued networks usually have tremendous parameters, leading to a large memory footprint and power budget when deployed on resource-constrained platforms. To deal with this problem, many researchers designed DNN compression methods and efficient hardware architectures [1]. Another promising approach is to use Spiking Neural Networks (SNNs). Compared to non-spiking DNNs, SNNs mimic the spiking behavior of biological neurons, thus have the potential to achieve better performance with lower complexity. The energy efficiency primarily benefits from: (1) the sparsity brought by discrete spikes; (2) replacing multiply-accumulate (MAC) operations by addition due to binary spike connections. However, modern silicon implementations of SNNs have lagged behind those of DNNs, mainly featuring lower throughputs [2]. Since SNNs run over multiple timesteps, the sparsity exists spatially across neurons and temporally over timesteps, i.e., spatio-temporal sparsity. However, exploiting spatio-temporal sparsity in hardware usually leads to an unpredictable and dynamic workload, affecting the hardware efficiency of running SNNs.

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Research on improving SNN efficiency can be categorized into three categories. The first category is to deploy SNNs on commercial architectures. However, CPUs lack enough parallelism to achieve decent throughput. GPUs have high efficiency when running tasks with highly parallel computation and memory access, but low efficiency when facing irregular computational flow and data access which is ubiquitous in SNNs. The second approach is to design domain-specific hardware, including large-scale systems (e.g. Loihi [3], TrueNorth [4]) and low-power accelerators [5]–[10]. Our work also falls into this category. The third category is to explore emerging devices that are easier adaptable to the event-driven properties of SNNs [11], [12].

This paper proposes an SNN accelerator, Skydive, that achieves high throughput by exploiting the spatio-temporal workload balance. The main contributions are:

• We proposed an Approximate Proportional Relation Construction (APRC) method to predict the relative workload channel-wisely offline by modifying the network structure without any accuracy loss.

• Based on the workload prediction, our Channel-Balanced Workload Schedule (CBWS) method can be easily applied to exploit spatio-temporal workload balance.

• The proposed accelerator Skydive is implemented on a Xilinx XC7Z045 FPGA and verified by image segmentation and classification tasks. Results show that Skydive achieved 98.5% classification accuracy and 22.6 K FPS throughput on the MNIST dataset.

II. MOTIVATION

As shown in Fig. 1 SNNs are organized in cascaded layers and are executed over timesteps with inputs encoded in spike trains. A spike generated by a neuron triggers the update of the membrane potential of each fan-out neuron. The membrane potential $V^l_i(t)$ integrates the input current $z$ at each time step:

$$V^l_i(t) = V^l_i(t-1) + z_i^l(t) - V_{th} \Theta_i^l(t)$$

Fig. 1. SNN topology and spiking neural dynamics
where $\Theta^l_i(t)$ is a spike, $V_{th}$ is the voltage threshold, and $z^l_i(t)$ is the input of neuron $i$ in layer $l$, which is given as:

$$z^l_i(t) = \sum_{j=1}^{M^l-1} W_{ij}^l \Theta^{l-1}_j(t) + b^l_i,$$

(2)

where $W_{ij}^l$ is the synaptic weight. A spike $\Theta^l_i$ is generated when $V^l_i(t)$ exceeds the threshold $V_{th}$ as

$$\Theta^l_i(t) = U(V^l_i(t) - V_{th} \Theta^l_i(t-1)),$$

(3)

where $U(x)$ denotes a unit step function. The spikes propagate through the network until reaching the output.

SNNs have intrinsically event-driven workloads since the update of membrane potentials is triggered by spikes. Fig. 2(a) shows that the spikerate varies, ranging substantially from 2% to 18% across the layers. The average spikerate is less than 8%, indicating a high level of spatio-temporal sparsity. Thus, arithmetic operations can be saved if connections without a spike are skipped. Moreover, the spikerate differs across timesteps, indicating that the proportion of active neurons varies over time. The dynamic active connections between neurons introduce an irregular computation flow and unpredictable memory access patterns, leading to an unbalanced workload. Fig. 2(b) and 2(c) showcase the unbalanced workload with respect to channels. They present the spike summation and distribution over 50 timesteps of 16 channels in a representative spiking layer, from which we find the significant imbalance by several orders of magnitude. Next, we present how Skydiver balances the workload to achieve higher hardware efficiency.

III. ARCHITECTURE DESIGN AND DATA PROCESSING

To exploit spatio-temporal workload balance, we first create an approximately proportional relationship between channel spikerates and filter magnitudes to predict the relative channel workload. Then, a channel-balanced workload schedule method is applied on Skydiver, which can alleviate the imbalance without overheads.

A. Skydiver: Architecture

The top-level architecture of the proposed Skydiver accelerator is depicted in Fig. 3. Skydiver is composed of a controller, memory blocks, and processing elements. The memory module contains a neuron state memory, a membrane potential (VMEM) Memory, and weight memory. A Xilinx Direct Memory Access (DMA) IP block controlled by the host is used to manage the I/O communications between the accelerator and the host. Input spike trains are streamed from DDR to the accelerator and buffered in the neuron state memory. The spike scheduler is used to detect the neurons that fire and generate the memory address of the corresponding weights, of which the details can be found in our previous work [7].

The processing elements comprise several filter-based Spiking Processing Elements (SPE) clusters. Each SPE cluster is connected to a corresponding weight bank and contains multiple channel-based SPEs, the finest grain of workload balance. The controller manages the overall execution, which updates the state of the accelerator and decodes the information fetched from the host.

B. Approximate Proportional Relation Construction (APRC) between Channel Spikerates and Filter Magnitude

Fig. 4(a) outlines how the output feature maps are formed by filters and input feature maps in a convolutional layer. The core operation is a 3-dimensional sliding window convolution of a $R \times R \times C$ element filter over a $H \times H \times C$ element input channels. Multiple ($M$) filters can be applied to the same input feature maps to generate $M$ output channels, each output channel is associated with a filter.

According to Eq.(1)-Eq.(3), the larger the filter magnitude (i.e., the summation of all the elements within a filter) is, the higher membrane potential the neuron has accumulated. However, shown in Fig. 4(b), the exact proportionality could
Kernel-based SPE cluster M
  Kernel-based SPE cluster 1
…
Channel-based SPE 1
…
Channel-based SPE N
  Output channel 1
  …
  Output channel M

Fig. 5. Structure of the filter-based spiking processing unit.

the channel spikerates and filter magnitudes approximately proportional.

For better illustration, we take an example (Fig. 4(c)) to explain how the proportional relation between channel spikerates and filter magnitude are constructed based on modified convolutions. Assume two 3 x 3 filters with different magnitudes (2.7 and 0.9; the ratio is 3) and an 8 x 8 input neuron state map padded by zeros. After convolutions, two output channels are generated. The summations of the updated membrane potential across the two output channels are 16.2 and 5.4, respectively, showing the same ratio as that of filter magnitudes. A spike is generated once the membrane potential exceeds the pre-defined threshold. 6 and 2 spikes are generated in the two output channels, respectively. It shows that the filter magnitudes have a proportional relationship with output channel spikerates.

C. Channel-Balanced Workload Schedule (CBWS) mechanism

SPE clusters are provided with different filters, and each cluster can calculate the membrane potential of a specific output channel independently. As shown in Fig. 5, a cluster consists of several channel-based SPEs and adder trees. Each channel-based SPE receives a subset of kernels within a filter and produces partial sums of membrane potentials. Within a channel-based SPE, the workload is further partitioned into four streams, which calculate equal rows of elements in the output. Each adder tree collects the partial sums from the corresponding stream of all channel-based SPEs.

Since the sparsity of input channels are quite different, the SPE which computes channels with the most zero inputs first completes the task, whereas the SPE computing channels with the most nonzero inputs become the bottleneck of hardware throughput. To deal with this unbalanced event-driven workloads, the Channel-Balanced Workload Schedule (CBWS) method (seen in Algorithm 1) is proposed, in which the input channels will be partitioned into N groups with almost equal workloads and processed by N SPEs. First, build a list containing filter magnitudes; Second, resort the list piecewisely by making each two adjacent data fields have opposite orders; Third, split the list into N sublists, and initialize them with roughly equal element summations by gathering the elements with the same index in each data field together; Finally, fine-tune the elements in each sublist.
Algorithm 1 Channel-balanced workload schedule mechanism

Require:

\( W, \) the parameters in the network; \( K, \) the number of filters in a certain layer; \( M, \) the number of SPE clusters; \( N, \) the number of SPEs in a cluster.

Ensure:

Balanced task allocation;
1. Sum up the parameters of each kernel, \( s = \sum W. \)
2. Build a list \( C \) containing all the \( s, \) and sort the elements in descending order.
3. // Build a new list \( C_{new} \) by resorting list \( C \) piecewisely.

4: for \( i = 0; i \leq K/N - 1; i++ \) do
  5:    if \( \text{mod}(i, 2) \) then
  6:      \( C_{new}.\text{append}(C[Ni:Ni+N-1]). \)
  7:    else
  8:      \( C_{new}.\text{append}(\text{sort}(C[Ni:Ni+N-1],'\text{descend}'). \)
  9:   end if
10: end for
11: // Split the list \( C \) into \( N \) sublists, and initialize them with roughly equal summations.
12: for \( i = 0; i \leq K/N - 1; i++ \) do
13:   for \( j = 0; j \leq N - 1; j++ \) do
14:     Add the element \( C_{new}[Ni+j] \) to sublist \( L_j; \)
15:   end for
16: end for
17: // Finetune the elements in sublists within \( T \) iterations.
18: for \( t = 0; t \leq T; t++ \) do
19:   \( \text{sum}_j = \sum L_j. \)
20:   \( \text{diff}(t) = \text{max}(\text{sum}_j) - \text{min}(\text{sum}_j). \)
21:   Obtain the sublist \( L_{\max} \) with \( \text{max}(\text{sum}_j) \), and the sublist \( L_{\min} \) with \( \text{min}(\text{sum}_j). \)
22:   if \( \text{diff}(t)/2 > \\text{min}(L_{\max}) \) then
23:     move the element \( \text{min}(L_{\max}) \) from \( L_{\max} \) to \( L_{\min}. \)
24:     Update \( L_i. \)
25:   else
26:     BreakTimeLoop()
27:   end if
28: end for

IV. EXPERIMENTAL RESULTS

Skydiver was evaluated on an image classification task and a segmentation task. As for the classification model, we adopt a spiking network with a 28x28-16c-32c-8c-10 structure on the MNIST dataset. As for the spiking segmentation model, we use the structure with 160x80x3-32c-32c-32C3-16C3-1C3-160x80xI from MLND-Capstone project which has 189.5K parameters.

The proposed APRC strategy is supposed to construct an approximate proportional relation between the number of spikes in an output channel and the corresponding filter magnitude. Fig. 6(a) shows a relatively irregular relation between the number of spikes and filter magnitude when APRC was not applied. Fig. 6(b) shows that APRC constructed an approximately proportional relation in the convolutional SNN layers of the classification network. Unbalanced workloads between SPEs lead to deteriorated actual throughput. Thus, the most important feature of Skydiver is the ability to efficiently handle the dynamic workload of SNNs, which is quantified by the balance ratio defined in [15]. Fig. 7 shows the balance ratio across layers of the segmentation network. It was observed that the performance of the CBWS mechanism is directly affected by the existence of the APRC strategy. When CBWS has applied alone, this design only achieved a 54.37% balance ratio. After combining with the APRC mechanism, the ratio was improved to 95.69%. Besides, without the proposed CBWS and APRC strategies, the accelerator achieved a 69.19%

1https://github.com/mvirgo/MLND-Capstone/
ratio, which proves the importance of APRC in predicting workloads in advance. The balance ratio is improved for the classification network from 79.63% to 94.14% using both APRC and CBWS. The higher balance ratios result in 1.4× and 1.2× actual throughput increase in the segmentation and classification tasks, respectively.

The proposed Skydiver accelerator is synthesized and implemented on an XC7Z045 FPGA at 200 MHz. The host manages the input and output data transfer of the programmable logic. The resource utilization of the programmable logic, which reflects the physical area of Skydiver, is shown in Table II. Table I presents the results of this work and prior state-of-the-art SNN processors. Skydiver achieved 110 FPS throughput and 0.91 mJ/image prediction energy when processing the segmentation network, and 22.6K FPS throughput, 42.4 μJ/image prediction energy when processing the classification network. Compared to prior SNN processors, Skydiver achieved competitive prediction throughput. Prior DNN accelerators such as Spartan [16] groups filters by density to schedule the workloads, however it can not solve the workload imbalance caused by dynamic neuron sparsity in SNNs.

V. CONCLUSION

In this work, we introduced an energy-efficient convolutional SNN accelerator called Skydiver. We showed that a significant workload imbalance exists in the channels of the feature maps. To exploit spatio-temporal workload balance, the APRC method was proposed to predict the relative workload channel-wisely. Based on the prediction, the workload balancing method CBWS was proposed to improve the hardware efficiency and throughput gain. Skydiver was evaluated on an XC7Z045 FPGA, and the results show that it can achieve competitive energy efficiency and throughput.

TABLE I

| Platform | Network | Task | Freq. (MHz) | on-chip Power (W) | Predition Energy (mJ/frame) | Throughput (FPS) | Efficiency (GSOp/s/W) |
|----------|---------|------|-------------|------------------|-----------------------------|-----------------|---------------------|
| VC707    | MLP     | image classif. | 100        | 1.6              | 5.04                        | 0               | 4.04                |
| XCZU9EG  | MLP/CNN | image classif. | 125        | 1.5              | 2.34/33.84                  | 22              | 0.91                |
| XC7XV690T | MLP     | image classif. | 0.7        | 0.7              | 0.77                        | 0.91            | 1.04                |
| Zynq ZCU102 | CNN   | image classif. | 700        | 4.6              | 30                          | 9.12/seg.       | 0.11/seg./22.6/16.8 |
| XC7Z045  | CNN/CNN | image classif./video seg. | 200       | 19.3             | 9.12@seg.0.04/classif.       |                 |                     |

1 Classification network with 784-500-500-10 and 28x28-32C3-P2-32C3-P2-256-10 for MNIST.
2 Classification network with 784-512-384-10 for MNIST.
3 Classification network with 28x28-64C5-2S-64C5-2S-128F-10 for MNIST.

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