Accelerator Codesign as Non-Linear Optimization

Nirmal Prajapati, Sanjay Rajopadhye Hristo Djidjiev, Nandkishore Santhi Tobias Grosser Rumen Andonov
Colorado State University Los Alamos National Laboratory ETH IRISA
Fort Collins, CO Los Alamos, NM, USA Zurich University of Rennes

Abstract—We propose an optimization approach for determining both hardware and software parameters for the efficient implementation of a (family of) applications called dense stencil computations on programmable GPGPUs. We first introduce a simple, analytical model for the silicon area usage of accelerator architectures and a workload characterization of stencil computations. We combine this characterization with a parametric execution time model and formulate a mathematical optimization problem. That problem seeks to maximize a common objective function of all the hardware and software parameters. The solution to this problem therefore "solves" the codesign problem: simultaneously choosing software/hardware parameters to optimize total performance.

We validate this approach by proposing architectural variants of the NVIDIA Maxwell GTX-980 (respectively, Titan X) specifically tuned to a predetermined workload of four common 2D stencils (Heat, Jacobi, Laplacian, and Gradient) and two 3D ones (Heat and Laplacian). Our model predicts that performance would potentially improve by 28% (respectively, 33%) with simple tweaks to the hardware parameters such as adapting coarse and fine-grained parallelism by changing the number of streaming multiprocessors and the number of compute cores each contains. We propose a set of Pareto-optimal design points to exploit the trade-off between performance and silicon area and show that by additionally eliminating GPU caches, we can get a further 2-fold improvement.

I. INTRODUCTION

Software-hardware codesign is one of the proposed enabling technologies for exascale computing and beyond [31]. Currently, hardware and software design are done largely separately. Hardware manufacturers design and produce a high-performance computing (HPC) system with great computing potential and deliver it to customers, who then try to adapt their application codes to run on the new system. But because of a typically occurring mismatch between hardware and software structure and parameters, such codes are often only able to run at a small fraction of the total performance the new hardware can reach. Hence, optimizing both the hardware and software parameters simultaneously during hardware design is considered as a promising way to achieve better hardware usage efficiency and thereby enabling leadership-class HPC availability at a more manageable cost and energy efficiency.

The design of HPC systems and supercomputers is by no means the only scenario where such optimization problems occur. The execution platforms of typical consumer devices like smart phones and tablets consist of very heterogeneous Multi-Processor Systems-on-Chip (MPSoCs) and the design challenges for them are similar.

Despite the appeal of an approach to simultaneously optimize for software and hardware, its implementation represents a formidable challenge because of the huge search space. Previous approaches [7], [9], [22], pick a hardware model \( \mathcal{H} \) from the hardware design space, a software model \( S \) from the software design space, map \( S \) onto \( \mathcal{H} \), estimate the performance of the mapping, and iterate until a desirable quality is achieved. But not only each of the software and hardware design spaces can be huge, each iteration takes a long time since finding a good mapping of \( S \) onto \( \mathcal{H} \) and estimating the performance of the resulting implementation are themselves challenging computational problems.

In this paper, we propose a new approach for the software-hardware codesign problem that avoids these pitfalls by considerably shrinking the design space and making its exploration possible by formulating the optimization problem in a way that allows the use of existing powerful optimization solvers. We apply the methodology to programmable accelerators: Graphics Processing Units (GPUs), and for stencil codes. The key elements of our approach are to exploit multiple forms of domain-specificity. Our main contributions are:

- We propose a new approach (see Section II) to software-hardware codesign that it is computationally feasible and provides interesting insights.
- We develop a simple, analytical model for the silicon area (Section III) of programmable accelerator architectures, and calibrate it using the NVIDIA Maxwell class GPUs.
- We combine this area model with a workload characterization of stencil codes, and our previously proposed execution time model [27] to formulate a mathematical optimization problem that maximizes a common objective function of the hardware and software parameters (see Section IV).
- Our analysis (Section V) provides interesting insights. We produce a set of Pareto optimal designs that represent the optimal combination of hardware and compiler parameters. They allow for up to 33% improvement in performance as measured in GFLOPs/sec.

II. APPROACH

The key element of our approach is exploiting domain specificity. We do this in three ways. First, we tackle a specific (family of) computations that are nevertheless very important in many embedded systems. This class of computations, called dense stencils, includes the compute intensive parts of many image processing kernels, simulation of physical systems relevant to realistic visualization, as well as the solution of partial differential equations (PDEs) that arise in many cyber-physical systems such as automobile control and avionics.
second, we target GPU-like vector-parallel programmable accelerators. Such components are now becoming de-facto standard in most embedded platforms and MPSoCs since they provide lightweight parallelism and energy/power efficiency. We further argue that they will become ubiquitous for the following reasons. Any device on the market today that has a screen (essentially, any device, period) has to render images. GPUs are natural platforms for this processing (for speed and efficiency). So all systems will have an accelerator, by default. If the system now needs any additional dense stencil computations, the natural target for performing it in the most speed/power/energy efficient manner is on the accelerator.

The third element of domain specificity is that we exploit a formalism called the polyhedral model as the tool to map dense stencil computations to GPU accelerators. Developed over the past thirty years \cite{4, 5, 7, 8, 9}, it has matured into a powerful technology, now incorporated into gcc, llvm and in commercial compilers [Rstream, IBM]. Tools targeting GPUs are also available \cite{16, 2}. We recently showed \cite{27} that these elements of the domain specificity can be combined to develop a simple analytical model for the execution time of tiled stencil codes on GPUs, and that this model can be used to solve for optimal tile size selection.

Thus, we formulate the domain specific optimization problem as: simultaneously optimize compilation and hardware/architectural parameters for compiling stencil computations to GPU-like vector-parallel accelerators.

To explain our overall approach, first recall how tile size selection is formulated as an optimization problem \cite{27}. A given class of programs, with some problem parameters, $\vec{p} \in \mathcal{P}$ (e.g., size of the iteration space, number of array variables) is compiled to an accelerator with some hardware parameters $\vec{h} \in \mathcal{H}$ (e.g., number of cores, number of vector units, cache size, etc.) The compiler itself may use some well defined optimization strategies (e.g., tiling, skewing, parallelization, etc.), and may have some software parameters, notably tile sizes ($\vec{s}$).

We develop an analytical function, $\mathcal{T}(\vec{p}, \vec{h}, \vec{s})$ that predicts the execution time of the target program as a function of these parameters. The values of the parameters must satisfy a set of feasibility constraints (e.g., tile sizes must be such that the data footprint of a tile must fit in the available scratchpad memory) denoted by $\mathcal{F}(\vec{s}, \vec{h}, \vec{s})$. Then, optimal tile size selection is simply solving the following problem:

\begin{equation}
\begin{aligned}
\text{minimize} & \quad \mathcal{T}(\vec{p}, \vec{h}, \vec{s}) \\
\text{subject to:} & \quad \vec{s} \in \mathcal{F}(\vec{p}, \vec{h}, \vec{s})
\end{aligned}
\end{equation}

Here, the unknown variables are $\vec{s}$. The hardware and program parameters are considered as constants—compiling a different program and/or compiling to a different target machine entails solving a new optimization problem. Extending this to codesign requires the following steps.

- **Workload characterization** We first pick a set $\mathcal{W}$ of representative program instances. For each one, we use profiling to pick the probability/frequency with which it occurs in the workload. Each program may be executed with a range of program parameters, and we also have a frequency with which these appear in the workload. So, $\overrightarrow{\rho}_{i,j}$ are the program parameters of the $i$-th instance of the $j$-th benchmark, and the set $\{\overrightarrow{\rho}_{i,j} | i \in \text{Instances}, j \in \text{Benchmark}\}$ is $\mathcal{P}$, the range of program parameters.

- **Codesign Optimization** Now we formulate a simple extension of \cite{27}. Instead of leaving the hardware parameters as constants, we allow them to be unknown variables of the optimization problem, which now becomes

\begin{equation}
\begin{aligned}
\text{minimize} & \quad \mathcal{T}(\vec{p}, \vec{h}, \vec{s}) \\
\text{subject to:} & \quad \vec{s} \in \mathcal{F}(\vec{p}, \vec{h}, \vec{s}), \quad \vec{h} \in \mathcal{H}(\vec{h})
\end{aligned}
\end{equation}

- **Area Model** Since $\vec{h}$ is now an unknown, we must formulate its feasible space, $\mathcal{H}(\vec{h})$ precisely. For this, we develop an analytical model of the area of the accelerator. We assume that we are given an area budget within which the accelerator must fit, and solve the optimization problems over the resulting feasible space.

This seems (deceptively) simple, but the devil is in the detail. The resulting optimization problem has many hundreds of variables, and has non-convex constraints and objective functions, making it computationally intractable. The details of how we solve it are explained in Section IV.

### III. Area Model

We now develop an analytic model for the total silicon area of a GPU accelerator. We faced some difficulties in deriving an acceptable analytical model, as silicon data had to be reverse engineered from extremely limited public domain resources. As a general observation, within each GPU family, there is little diversity in the parameter configurations. For the Maxwell family of GPUs, the GTX980 and Titan X chips were chosen as two sufficiently distinct points to calibrate our analytical models. The calibration itself was performed by evaluating die photomicrographs, publicly available information about the nVidia GTX-980 (Maxwell series) GPU, and other generally accepted memory architecture models. The model validation was done by comparing the predictions with known data on the Maxwell series Titan X GPU. We found the model prediction to be accurate to within, 2%, though this number is not significant.\footnote{Although a many configurations of any family of GPUs are spaced out, they come from binning only a small number of distinct dies. We ended up calibrating our model on one die and validating it on only another one.}

#### A. Analytical Model for GPU Area

The area model is a function of the main parameters that we want to select optimally in the codesign problem: the number of SMs, $n_{\text{SM}}$, the number of vector units or cores in each SM, $n_{\text{V}}$, and the respective sizes of the register file and shared memory size of the SM, $R_{\text{SM}}$, and $M_{\text{SM}}$. Table \ref{table:1} shows a summary of the various parameters used in developing the area model.
TABLE I: Area model parameters. The top two groups are elementary parameters, and the third one is composite (some function of the elementary parameters). Of the elementary ones, the second one are treated as variables in our optimization formulation.

| Name         | Description                                                                 |
|--------------|------------------------------------------------------------------------------|
| \( \alpha_{SFU} \) | overhead area per kB of register-memory per vector-unit                     |
| \( \alpha_{M} \) | overhead area per kB of shared-memory per SM                                |
| \( \alpha_{L1} \) | L1 cache overhead area per SM-pair                                           |
| \( \alpha_{L2} \) | L2 cache overhead area                                                       |
| \( \alpha_{oh} \) | common overhead area (I/O, global routing etc) per SM                       |
| \( \beta_{FPU} \) | area per register-file-bank per kB per vector-unit                          |
| \( \beta_{I} \) | area per shared-memory-bank per kB per SM                                    |
| \( \beta_{L1} \) | L1 cache area per kB per SM-pair                                             |
| \( \beta_{L2} \) | L2 cache area per kB per vector-unit                                         |
| \( \beta_{VU} \) | core-logic area within a vector-unit                                        |
| \( n_{SM} \) | total number of SM on the GPU chip                                          |
| \( n_{V} \) | number of vector-units per SM                                               |
| \( \beta_{FU} \) | kB of register files per vector-unit                                        |
| \( M_{SM} \) | kB of shared memory per SM                                                  |
| \( L1_{SMpair} \) | kB of L1 cache per SM-pair                                                  |
| \( L2_{SM} \) | kB of L2 cache                                                              |
| \( A_{tot} \) | total GPU chip die area                                                     |
| \( A_{SM} \) | total shared-memory die area                                                |
| \( A_{cache} \) | total cache die area                                                        |
| \( A_{oh} \) | total on-chip overhead die area                                             |
| \( A_{LDU} \) | total load-store unit die area                                              |
| \( A_{FPU} \) | total special-function unit die area                                        |
| \( A_{FDU} \) | total fetch-decode unit die area                                            |
| \( A_{cache} \) | total instruction-cache die area                                            |
| \( A_{LDUperSM} \) | load-store unit die area per SM                                             |
| \( A_{FPUperV} \) | load-store unit die area per vector-unit                                    |
| \( A_{SMperSM} \) | memory die area per SM                                                      |
| \( A_{SMperV} \) | special-function unit die area per vector-unit                              |

\[
A_{tot}(\cdot) = n_{SM} A_{SM} + A_{cache} + A_{oh} \quad (3)
\]

where \( A_{SM} \) is the cost of each SM, \( A_{cache} \) is the total area of the on-chip L1 and L2 caches, and \( A_{oh} \) is the overall overhead area cost. The term \( A_{oh} \) accounts for several components which are of only peripheral interest to us, such as metal-layer routing overheads, I/O pads, buffers, and clock-signal global distribution trees, gigathread scheduler, PCI express interface, raster engine, and memory controller. Based on our current understanding of the nVidia architecture, a best effort annotation of various functional blocks is shown overlaid on a die photomicrograph of GTX980 chip in Figure 1. The term \( A_{SM} \) denotes the area of a single SM, and we develop it next. The following micro-architectural elements comprise an SM:

- Individual vector units: The area cost of this is \( n_{V} \beta_{VU} \).
- Load-store unit (LSUs): Every core may issue independent memory requests, to either the shared memory or to global memory. Therefore the LSU has a component that is replicated per core, and also a shared component that (eventually) collects together all requests from a single warp and interfaces to the (global) memory hierarchy. Therefore \( A_{LSU} = n_{V} A_{LSUperV} + A_{LSUperSM} \).
- Special function units (SFUs): These are dedicated functional units that are used for common graphics functions, transcendentals, etc. Their number is not always exactly equal to \( n_{V} \), (e.g., in the nVidia GTX-980, there is one SFU every 8 cores) but we model it as a linear function of \( n_{V} \), i.e., \( A_{SFU} = n_{V} A_{SFUperV} \).
- Instruction fetch-decode unit (FDU): Like the I-cache, there is a single FDU per SM, so its cost is simply a constant \( A_{FDU} \).
- Various specialized “memories:” the shared memory used as scratchpad, the register file, the instruction cache, the texture and other special caches. We call this term \( A_{SMperSM} \) and develop it separately.

Of these, the memories other than register files and the FDU are shared by the entire SM, while the register files, SFU and LSU are accounted for on a per vector unit basis. Hence,

\[
A_{SM}(\cdot) = (A_{FDU} + A_{Icache} + A_{LSUperSM}) + A_{SMperSM} + n_{V}(A_{SFUperV} + A_{core} + A_{LSUperV}) \quad (4)
\]

where \( \alpha' = A_{FDU} + A_{Icache} + A_{LSUperSM} \), and \( A_{SMperSM} \) depends on the capacity of each of the individual memories. Of these, we are interested in modeling the area costs for the register file, shared (scratchpad) memory, L1 cache and L2 cache; so the others are treated as constants absorbed in \( \alpha' \). L1 cache is shared by a pair of SM units, while the L2 cache is shared by all the SM units on the chip. The register files are organized so that a few registers (512 registers each 32 bits wide in GTX980) are exclusively accessible by each vector-unit. The shared memory is accessible by all vector-units in an SM. Assuming independent linear cost models for each of these four memory types, therefore, \( A_{SMperSM}(\cdot) = n_{V} (\beta_{R} R_{VU} + \alpha_{R}) + (\beta_{M} M_{SM} + \alpha_{M}) + \frac{n_{SM}}{2} (\beta_{L1} L1_{SMpair} + \alpha_{L1}) + (\beta_{L2} L2_{SM} + \alpha_{L2}) \). Here, we have subscribed to a design philosophy where the size of the L2 cache is not proportional to the number of SM units, it is a constant. This choice seems to be the norm, in that the GTX980 chip with 16 SMs has an L2 cache of 2MB, whereas the Titan X with 24 SMs has an L2 cache of 3MB. Another design choice we make is the following – the common area overhead \( A_{oh} \), comprising the I/O pads, buffers, routing, gigathread engine, PCI and memory controllers, is also assumed to be proportional to the number of SMs\(^2\), that is, \( A_{oh} = n_{SM} \alpha_{oh} \). Substituting this result in the above equations, collecting all common overhead area contributions including \( \alpha' \) into \( \alpha_{oh} \), and further simplifying, we get:

\[
A_{tot}(\cdot) = n_{SM} n_{V} \beta_{VU} + n_{SM} n_{V} (\beta_{R} R_{VU} + \alpha_{R}) + n_{SM} (\beta_{M} M_{SM} + \alpha_{M}) + \frac{n_{SM}}{2} (\beta_{L1} L1_{SMpair} + \alpha_{L1}) + (\beta_{L2} L2_{SM} + \alpha_{L2}) + n_{SM} \alpha_{oh} \quad (5)
\]

B. Calibrating the Model

Since the overall area model involves non-linear terms, we used an incremental fitting approach to calibrate our model. We first developed linear regression models for the area contribution due to the memory elements. We then incorporated

\(^2\)This design choice is by no means the only possible one – another possibility is to also have an additional constant term, though one would need more than two GPUs in the Maxwell family with different die areas to calibrate such a model.
the memory element area model into a measurement based linear model for the area due to the SM core vector units.

Cacti model for L1 cache is a ‘cache’ type memory with a line-size of 128 bytes, and a data width of 32 bits. We also chose a conservative setting of full associativity for this cache level. There are 8 exclusive read ports for downstream access from the logic cores, and 8 exclusive write ports for upstream access from the L2 cache. The design was tailored for speed and the optimization objective was primarily propagation delay and secondarily power dissipation.

- L2 cache: For the nVidia Maxwell architecture, the L2 cache is shared by all the SM units on the chip. This GPU family, the L2 cache is on average 128kB per SM. Our Cacti configuration assumes a ‘cache’ type memory with a line-size of 128 bytes, and a data width of 256 bits on each of its 8 exclusive read ports feeding into every L1 cache on the chip downstream. There is also a exclusive read-write port for upstream interface with the memory controllers. The design objective was a weighted mix of delay and area.

Using these Cacti models, we obtained area estimates for per vector-unit register file banks of 512, 1024, 2048, 4096, and 8192 bytes each. We then derived a linear fit model for the area given the bank size. The coefficients of this model were \( \beta_R = 0.004305 \) and \( \alpha_R = 0.001947 \).

Similarly, we obtained area estimates for per SM shared memory banks of 24, 48, 96, 192, and 384 kilo-bytes size each, and derived a linear fit model. The coefficients of this linear model were \( \beta_M = 0.01565 \) and \( \alpha_M = 0.09281 \).

The L1 and L2 cache models were similarly calibrated by performing optimizations using our Cacti models as described earlier. The L1 linear fit model was obtained with per SM-pair sizes of 3, 6, 12, 24, 48, and 96 kilo-bytes each. The model parameters obtained were \( \beta_{L1} = 0.1604 \) and \( \alpha_{L1} = 0.08204 \). The L2 linear fit model was obtained with per SM sizes of 32, 64, 128, 256, and 512 kilo-bytes each. The parameters obtained were \( \beta_{L2} = 0.04197 \) and \( \alpha_{L2} = 0.7685 \). The linear regression models obtained as above are shown in Figure 2.

![Fig. 1: Best effort annotation of functional blocks in a GTX980 die photograph [15] based on current understanding of the nVidia Maxwell architecture and chip layout.](image1)

![Fig. 2: Linear regression models for various memory types on a Maxwell series GPU. The Cacti predicted area used to obtain the linear model are also shown.](image2)

nVidia publishes obfuscated die-shots of their GPU chips, though these photographs are sometimes not to scale. The
community of GPU enthusiasts and researchers have also attempted to decap packaged GPU chips and photograph the silicon dies independently. For example, Fritzchens Fritz [15] has a vast collection of nVidia die photographs which we have used in association with the obfuscated die shots published by nVidia. The nVidia official “die-shots” tend to show demarcated logical functional blocks - for SMs, this includes not only the SM core logic regions, but also the associated control, and thread-scheduler logic areas too. We have factored these aspects into account while making our area measurements. The area measurements were initially made in terms of pixels, and later normalized to mm² using the total die area from the GPU’s datasheet. As a verification of the memory area model calibration, we first measured the area of the following memory blocks on the die photograph – L2: 105 mm², L1: 7.34 mm², and shared memory: 1.27 mm². These measured areas matched quite well with the linear model predictions – L2: 98.25 mm², L1: 7.78 mm², and shared memory: 1.59 mm². Furthermore, from the die photomicrographs for GTX980 [15], [25], area per vector-unit logic core was measured to be $\beta_{VU} = 0.04282$ mm², excluding the register-file area. Similarly, measurements on GTX980 die photographs gave an area estimate of 102.65 mm² for the overhead region containing the I/O pads, buffers, memory controllers, gigathread and raster engines and PCI controller, which gives an $\alpha_{oh} = 6.4156$ mm² per SM. The total published die area for GTX980 is also known to be $A_{tot} = 398$ mm². For the Maxwell family, our overall area model is therefore given by:

$$A_{tot} = 0.0447n_{SM}n_{V} + 0.0043R_{VU}n_{SM}n_{V} + 0.015M_{SM}n_{SM} + 0.08L_{SM}n_{SM} + 0.041L_{2}n_{SM} + 7.317n_{SM}$$

(6)

C. Validating the Model

In order to validate our area model, we applied it to another member of the Maxwell family, the Titan X for which the total die area is known. Our model predicts a total area of 589.2 mm² which is within an error of 1.96% of the published die area of 601 mm².

Our area model above is only valid for the functional blocks as implemented for the specific TSMC 28-nm process used to fabricate the nVidia Maxwell chips. The newer Pascal family of nVidia GPUs are fabricated on a 16-nm technology node. If each of the constituent functional block’s chip level layouts were to remain same across technology nodes, and were only optically reduced down by a certain shrinkage factor, then the area model can be similarly rescaled and reused. However, the shift from 28-nm to 16-nm involves a non-trivial move from planar CMOS to 3D-FINFET technology, and consequently a simple area rescaling would clearly not be sufficient to predict the area parameters of Pascal family chips. However the overall methodology still remains applicable to any technology node or device family.

IV. OPTIMIZING SOFTWARE AND HARDWARE PARAMETERS

We now show how to use the analytical chip area model and our previous execution time model [27] to formulate and solve an optimization problem for simultaneously finding optimal hardware and software parameters.

A. Problem formulation

The parameters we are going to optimize are the elementary software (ES) parameters $t_s, t_s2, t_f$, and the elementary hardware (EH) parameters $n_{SM}, n_{V}$, and $M_{SM}$. For each combination of EH parameters, the corresponding running time in the objective function will be defined as the optimal time for that hardware configuration and for the stencil of interest over all possible choices of tile sizes.

This results in the following optimization problem, which finds the best EH parameters for a given stencil and a given bound on the chip area denoted by $chip\_area$

$$\text{minimize } T_{alg}(n_{SM}, n_{V}, M_{SM}, t_{S1}, t_{S2}, t_{T})$$

subject to:

$$A(n_{SM}, n_{V}, M_{SM}) \leq chip\_area$$

(7)

$$M_{tile} \leq M_{SM}/\text{threadblock}$$

(8)

$$k \leq M_{TB_{SM}}$$

(9)

$$k \cdot M_{tile} \leq M_{SM}$$

(10)

$$n_{V}, t_{S2} \text{ multiple of } 32$$

(11)

$$M_{SM} - \text{multiple of } 48k$$

(12)

$$n_{SM}, t_{T} \text{ even}$$

(13)

Note that $T_{alg}$ in (7) is in fact a function not only of the parameters $n_{SM}$, $n_{V}$, $M_{SM}$, $t_{S1}$, $t_{S2}$, and $t_{T}$, but also of the other parameters detailed elsewhere [27]. Also, for 3D stencils there is an additional parameter to function (7) which is the tile size in the third space dimension $t_{S3}$. We are only explicitly using those $T_{alg}$ parameters that are needed in the specific context. Constraint (8) guarantees that the total area for the current hardware configuration, according to the area model, does not exceed the optimization parameter $chip\_area$. Constraint (9) asks the memory required for each tile not to exceed $M_{SM}/\text{threadblock}$, the shared memory available for a threadblock, while (10) and (11) restricts the number of tiles simultaneously executed by an SM (using hyperthreading) to be no greater than the max threadblocks an SM can handle and such that the total memory of all such tiles is at most $M_{SM}$. The values of $k$ and $t_{S2}$ can be only integers, and $n_{V}, t_{S2}, M_{SM}, n_{SM}$ and $t_{T}$ should be multiples of 32, 32k, and 2, respectively, by constraints (11)–(15). We require $n_{SM}$ to be even, $n_{V}$ to be multiple of 32, and $M_{SM}$ to be multiple of 32k in order to be consistent with the patterns for these parameters chosen by the manufacturers in existing GPUs. For the tile sizes, we want $t_{T}$ to be even as it is a requirement for hybrid-hexagonal tiling [16], while $t_{S2}$ being a multiple of 32 ensures that neighboring threads in $S_2$ dimension can fit in a number of full warps, where each warp is a group of 32 threads.

The optimization problem (7)–(15) allows, given a stencil of interest (say Jacobi 2D) and specific values of the problem size parameters $S_1$ and $T$, to find a combination of software and hardware parameters that results in optimal (smallest) run time.
However, it is unlikely that one may need a hardware that will be used for just a single problem size. A more relevant problem is to optimize the hardware over a set of problem sizes. Given a set of sizes \( S_{\mathcal{Z}} = \{ (S_1^{(i)}, S_2^{(i)}, T^{(i)}) \} \) and a frequency function \( f_{\mathcal{R}}(S_{\mathcal{Z}}) \) is the expected frequency the size \( S_{\mathcal{Z}} \) becomes however further increases the number of variables, which even continuous, although this can be handled by introducing rational functions. Because of the floor and ceiling functions integer and the objective function and the constraints being case the problem is of a difficult type, with all variables being integer and the objective function and non-convex constraints and objective is nonlinear, nonconvex, and with integer variables. Fortunately, the problem can be made feasible by dividing the variables into two sets and combining exhaustive search on the first set with nonlinear programming optimization on the second.

### B. Solving the optimization problem

The main observation that helps us solve problem \( \text{(17)} \) more efficiently is the fact that, if we knew the optimal value \( h_{p, \text{opt}} \) of parameters \( HP \), then the objective \( \text{(17)} \) would become separable since \( T_{c, \text{alg}}(h_{p, \text{opt}}, SP, Sz) \) can be minimized with respect to the tile sizes independently for each \( c \) and \( Sz \). Formally, we are transforming \( \text{(17)} \) into the following equivalent problem

\[
\text{minimize } \sum_{c \in Cd, Sz \in \mathcal{Z}} f_{\mathcal{R}}(c) T_{c, \text{alg}}(hp, SP, Sz) \quad \text{subject to } T_{c, \text{alg}}(hp, SP, Sz) \leq T_{c, \text{opt}}(hp, SP, Sz).
\]

(18)

Since we don’t know \( h_{p, \text{opt}} \), then we replace \( hp \) in \( \text{(18)} \) with all feasible values of \( HP \) and, for each such value, we run a separate optimization problem with respect to \( SP \) for each combination of \( c \in Cd \) and \( Sz \in \mathcal{Z} \). As a result, instead of solving one large problem \( \text{(17)} \) with 642 variables, we do exhaustive search on the space \( HP \times Cd \times \mathcal{Z} \) and, for each point in that space, we solve using a nonlinear solver an optimization problem with only 10 integer variables. (While the variables we are interested in are only three, the optimization problem includes additional internal variables such as the optimal number of tiles for hyperthreading and variables used to simplify some nonlinearities, resulting in total number of 10.)

To further reduce the number of these problems, we will fix the range of values of the parameters as follows: \( 2 \leq n_{SM} \leq 32 \) and is even, \( 32 \leq n_{V} \leq 2048 \) and is a multiple of 32, which come from the constraints of \( \text{(15)} \). \( 48k \leq M_{SM} \leq 480k \) with the requirement \( \text{(14)} \) to be multiple of 48k and positive. In addition, we explore the sizes \( 12k, 24k, 36k \) for \( M_{SM} \).

We ran three experiments using chip areas in the range \( 200 – 650 \) mm\(^2\). Since we haven’t tied the experiments to a specific application, we assumed all six stencils equally likely, and that each size combination also equally likely; i.e., we set all coefficients in \( \text{(17)} \) to 1. For solving the optimization problems we used the open source solver bonmin [1]. The average solution time per optimization instance is 19 sec (although it varies a lot from instance to instance), so the total solution time varies between 7 and 24 hours depending on the chip area. Also note that, in the execution time model we...
use a parameter $C_{iter}$, the execution time of a single iteration on one thread. For optimal tile size selection, we measured this parameter for the different stencils. Although there was a small difference between the two platforms (GTX-980 and Titan X) we used the former value for our experiments.

V. DISCUSSION AND PERSPECTIVES

We will now illustrate how our codesign optimization can be used to explore various scenarios. Furthermore, we will see that the trick of partitioning the design space into a number of independent optimization problems, described by Eqn. (18), has added advantages of enabling investigation of a number of scenarios without re-solving optimization problems.

A. Design Space Exploration

Given a range of area budgets between 200 and 650 mm$^2$, we enumerated all feasible architecture, and solved the codesign optimization problem for each one. We separated the workload into two classes, 2D stencils and 3D stencils. Each one illustrates interesting features. For each class, we assumed a uniform frequency (each instance is equally likely, and within each instance, each problem size is also equally likely). Figure 3 shows out results. The first observation is that only about 1% of the thousands of feasible hardware designs (the Pareto optimal designs shown in blue) are worth exploring further, leading to a significant pruning of the design space.

We also show in the same figure the performance of two standard design points, Nvidia’s GTX980 and TitanX architectures. For comparable area, we can improve performance by 104% (resp., 69% wrt. TitanX) for 2D stencils, and by 123% (resp., 126%) for 3D stencils. A large part of the gains come from the fact that our proposed designs do not have caches because the HHC compiler for which our model is specialized generates codes to perform data transfers explicitly rather than relying on caches. To compensate for this, we could “delete” the caches from the GTX980 and TitanX, which reduces their areas to respectively, 237mm$^2$ and 356mm$^2$. The performance of the corresponding Pareto optimal designs for those reduced areas is 9.34% (resp., 28.44% for the cache-less TitanX) better for 2D stencils and 9.22% (resp., 33.15%) better for 3D stencils.

B. Workload Sensitivity

Eqn. (18) partitions the design space into a number of independent optimization problems. This allows us to explore other hypothetical scenarios “for free.” As an example, changing frequencies of the different programs in the benchmark suite requires us to simply recompute new weighted sums of optimal values of minimization problems that we have already solved. A specific example would be to hypothetically set the frequency for one of the benchmarks as one (and zero for the others) thereby allowing us to explore designs optimized for a single kernel. It also helps determine whether the chosen suite is representative of the mix that occurs in practice. Table ?? illustrates the architectural parameters for the best performing designs for each of the six benchmarks, for an area budget between 425–450 mm$^2$.

Observe how the parameters of the best architecture are significantly different. There are also differences in the achieved performance for each benchmark, but that is to be expected since the main computation in the stencil loop body has different numbers of operations across the benchmark. We can also observe that there is marked differences between 2D and 3D stencils. The latter seem to require larger shared memory, and well as higher number of vector units. Indeed, for designs
will lower than 48kB, the performance was nowhere near the optimal for these programs.

C. Resource Allocation

Another interesting perspective is seen in Figure 4 which plots the same design space as in Figure 3 but this time the axes are different, showing the relative percentages of the chip area devoted to memory, and to vector units. We notice the that optimal designs (blue points lie in a relative cluster. This phenomenon is even more marked for 3D stencils. At present, we do not have a clear explanation for why the points are clustered in this manner, as we plan to mine this data to determine patterns in the data.

D. Discussion

The designer can choose to fix some parameters and optimize for others. Given an application, if the architecture parameters are fixed, the designer can use our approach to optimize for compiler parameters. On the other hand, if only some of the architecture parameters are fixed, the number of vector units and the size of memories is fixed, then the designer can use our approach to tune for the number of SMs.

One limitation of our current model is register usage. It is known to be critical for performance, e.g., the size of the register file constrains the optimal tile sizes. Currently, the register file size is a fixed constant in the area model and does not appear in the execution time model. Modeling these effects analytically is an ongoing effort.

One must, however, take this with a grain of salt. Our models are approximate and there are other parameters that can play an important role in the design process. For instance, the designer might be interested in optimizing for both execution time as well as power simultaneously. Our approach can be extended to consider energy/power consumption into account. If the energy consumption details of the individual components of the architecture are known, then the objective function can be updated to be the argmin of the weighted execution times and energy components where we seek to maximize the performance. Such an optimization function can be formulated to solve power-gating problems where the designer wants to turn off certain parts of the chip.

Finally, we want to note two important aspects of this work. First, our area model is relatively simplistic, and second, the workload that we have chosen is rather artificial. Nevertheless, we have seen interesting patterns. We expect that designers in the field that have more precise (and probably proprietary) information about their specific context could easily add precision to our model and gather much more sophisticated conclusions.

VI. RELATED WORK

Our research draws upon prior work in three distinct areas.

A. Chip Reverse Engineering and Area Modeling

Chip area modeling can be formally considered a branch of semiconductor reverse engineering, which is a well researched subject area. Torrence et. al. [33] gives an overview of the various techniques used for chip reverse engineering. The packaged chips are usually decapped and the wafer die within is photographed layer by layer. The layers are exposed in the reverse order after physical or chemical exfoliation. Degate [5], for example, is a well known open source software that can help in analyzing die photographs layer by layer. The reverse engineering process can be coarse-grained to identify just the functional macro-blocks. Sometimes, the process can be very fine-grained, in order to identify standard-cell interconnections, and hence, actual logic-gate netlists. Degate is often used in association with catalogs of known standard cell gate layouts, such as those compiled by Silicon Zoo [33]. Courbon et. al. [4] provides a case study of how a modern flash memory chip can be reverse engineered using targeted scanning electron microscope imagery. For chip area modeling, one is only interested in the relatively easier task of demarcating the interesting functional blocks within the die.

B. Performance Modeling

There have been various works on time modeling and performance optimization.

Polymage [23] provides a stencil graph DSL and pairs it it with a simple analytical performance model for the automatic computation of optimal tile sizes and fusion choices. With MODESTO [17] an analytical performance model has been proposed that allows to model multiple cache levels and fusion strategies for both GPUs and CPUs as they arise in the context of Stella. For stencil GPU code generation strategies that use redundant computations in combination with ghost zones an analytical performance model has been proposed [21] that allows to automatically derive “optimal” code generation parameters. Yotov et. al [39] showed already more than ten years ago that an analytical performance model for matrix multiplication kernels allows to generate code that is performance-wise competitive to empirically tuned code generated by ATLAS [37], but at this point no stencil computations have been considered. Shirako et al. [32] use cache models to derive lower and upper bounds on cache traffic, which they use to bound the search space of empirical tile-size tuning. Their work does not consider any GPU specific properties, such as shared memory sizes and their impact on the available parallelism. In contrast to tools for tuning, Hong and Kim [15] present a precise GPU performance model which shares many of the GPU parameters we use. It is highly accurate, low level, and requires analyzing the PTX assembly code. For stencil GPU code generation strategies that use redundant computations in combination with ghost
zones an analytical performance model has been proposed \[21\] that allows to automatically derive “optimal” code generation parameters.

C. Hardware/Software Codesign

Application codesign is a well-established discipline and has seen active research for well over two decades \[28\], \[38\], \[2\], \[6\], \[34\]. The essential idea is to start with a program (or a program representation, say in the form of a CFDG—Control Data Flow Graph) and then map it to an abstract hardware description, often represented as a graph of operators and storage elements. The challenge that makes codesign significantly harder than compilation is that the hardware is not fixed, but is also to be synthesized. Most systems involve a search over a design space of feasible solutions, and various techniques are used to solve this optimization problem: tabu search and simulated annealing \[10\], \[11\] integer linear programming \[24\].

There is some recent work on accurately modeling the design space, especially for regular, or affine control programs \[26\], \[40\], \[41\]. However, all current approaches solve the optimization problem for a single program at a time. To the best of our knowledge, no one has previously considered the generalized application codesign problem, seeking a solution for a suite of programs.

There are multiple publications on codesign related to exascale computing, but they focus on different aspects. For instance, Dosanjhi et al. \[8\] focus on methodological aspects of exploring the design space, including architectural testbeds, choice of mini-applications to represent applications codes, and tools. The ExaSAT framework \[36\] was developed to automatically extract parameterized performance models from source code using compiler analysis techniques. Performance analysis techniques and tools targeting exascale and codesign are discussed in \[31\].

VII. CONCLUSION

We develop a framework for software-hardware codesign that allows the simultaneous optimization of software and hardware parameters. It assumes having analytical models for performance, for which we use execution time, and cost, for which we choose the chip area. We make use of the execution time model from Prajapati et al \[27\] that predicts the execution times of a set of stencil programs. For the chip area, we develop an analytical model that estimates the chip area of parameterized designs from the Maxwell GPU architecture. Our model is reasonably accurate for estimating the total die area based on individual components such as the number of SMs, the number of vector units, the size of memories, etc.

We formulate a codesign optimization problem using the time model and our area model for optimizing the compiler and architecture parameters simultaneously. We predict an improvement in the performance of 2D stencils by (104\% and 69\%) and 3D stencils by (123\% and 126\%) over existing Maxwell (GTX980 and Titan X) architectures.

The main focus of this paper is not on making specific design recommendations, but rather on the methodology; specifically, to develop a software-hardware codesign framework and to illustrate how models built using it can be used for efficient exploration of the design space for identifying Pareto-optimal configurations and analyzing for design tradeoffs. The same framework, possibly with some modifications, could be used for codesign on other type of hardware platforms (instead of GPU), other type of software kernels (instead of the set of stencils we chose, or even non-stencil kernels), and other kind of performance and cost criteria (e.g., energy as cost). Also, with work focused on the individual elements of the framework, the execution time and the chip area models we used could possibly be replaced by ones with better features in certain aspects or scenarios.

Despite this caveat, the analyses from this paper indicate the following accelerator design recommendations, for the chosen performance, cost criteria, and application profile:

- Remove caches completely and
- Use the area (previously devoted to caches) to add more cores on the chip.
- The more precise the workload characterization and the specific area model parameters, the more useful the conclusions drawn from the study.
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