Low-Noise Amplifier for Deep-Brain Stimulation (DBS)

Tiago Matheus Nordi 1, Rodrigo Henrique Gounella 1, Maximiliam Luppe 1, João Navarro Soares Junior 1, Erich Talamonì Fonoff 2, Eduardo Colombari 3, Murilo Araujo Romero 1 and João Paulo Pereira do Carmo 1,*

1 Group of Metamaterials Microwaves and Optics (GMeta), Department of Electrical Engineering (SEL), University of São Paulo (USP), Avenida Trabalhador São-Carlense, Nr. 400, Parque Industrial Arnold Schmitd, São Carlos 13566-590, SP, Brazil; tmnordi@usp.br (T.M.N.); rodrigogounella@usp.br (R.H.G.); maxluppe@sc.usp.br (M.L.); navarro@sc.usp.br (J.N.S.J.); murilo.romero@usp.br (M.A.R.)
2 Department of Neurology, Faculty of Medicine, Avenida Dr. Arnaldo, Nr. 455, Cerqueira César, São Paulo 01246-903, SP, Brazil; fonoffet@usp.br
3 Department of Physiology and Pathology, Faculty of Odontology, São Paulo State University (UNESP), Rua Humaitá, Nr. 1680, Araraquara 14801-385, SP, Brazil; eduardo.colombari@unesp.br
* Correspondence: jcarmo@sc.usp.br

Abstract: Deep-brain stimulation (DBS) is an emerging research topic aiming to improve the quality of life of patients with brain diseases, and a great deal of effort has been focused on the development of implantable devices. This paper presents a low-noise amplifier (LNA) for the acquisition of biopotentials on DBS. This electronic module was designed in a low-voltage/low-power CMOS process, targeting implantable applications. The measurement results showed a gain of 38.6 dB and a –3 dB bandwidth of 2.3 kHz. The measurements also showed a power consumption of 2.8 µW. Simulations showed an input-referred noise of 6.2 µVRMS. The LNA occupies a microdevice area of 122 µm × 283 µm, supporting its application in implanted systems.

Keywords: CMOS; deep-brain stimulation (DBS); low-noise amplifier; implantable devices

1. Introduction

Over the past decades, neuroscientists have been engaging the integrated circuit community to help them in the development of new tools for analyzing and understanding the brain. In this context, fundamental in vivo research on small animals has to be performed, which requires miniaturized instrumentation for long-term studies [1]. For several years, scientists have speculated that electroencephalographic (EEG) activity might provide the communication channel between brain and computer [2]. As the field has evolved, the demand for more functionally and miniaturization from the electronics community have risen. Since it is necessary to deal with low-amplitude biological signals, it is important to design amplifiers that make these signals compatible with devices such as ADCs for further analysis on computers. The amplifiers must have specific requirements, such as providing selective amplification to the physiological signal, rejecting superimposed noise and interference signals, and assuring protection from damage caused by high voltages and currents [3].

The recent developments of microelectronics have resulted in new applications involving the acquisition of biosignals both with wearable and implantable devices [4–8]. For instance, the electrocardiogram (ECG) is one of the most well-known applications, consisting of the acquisition of biosignals to allow medical doctors to diagnose heart diseases [6–10]. The electroencephalogram (EEG) is another widespread application with a large number of newly published works every year [11–13]. The neural recording has pushed the acquisition of biosignals to new levels, with new applications involving neuro-modulation [14–16]. Such applications include optogenetics, which is an emergent field of applications, where the signals are acquired from a specific part of the brain, while simultaneously, this same region of the brain can also be stimulated with light [17–20].
Then, a new paradigm of optogenetics is the concept of an electrode with a chip-in-the-tip, where a bioamplifier and the respective signal processing/control/interface electronics can simultaneously acquire the neuronal signals while stimulating the brain with light [21,22].

Another emerging field of applications is the deep-brain stimulation (DBS) [23]. Deep-brain stimulation (DBS) involves implanting, through a surgical procedure, a medical device called a neurostimulator (often also called brain pacemaker). In the procedure, implantable semi-rigid tips (with electrodes at the ends) are also inserted at strategic points in the thalamus, subthalamic region, globus pallidus, among other areas [24]. The electrodes are then connected to the neurostimulator itself by means of extension cables containing metallic wires [25]. These electrodes are normally distributed at the end of the tips [26] which is inserted into the brain, steering them towards the desired neurostimulation zones. The neurostimulator sends mild pulses to the brain through the electrodes [27]. The electrical current used is very low and is injected into points in the brain which are mostly located in deep areas.

The neurostimulator is a device with dimensions no larger than a matchbox, with an attached battery to provide energy for operation [28]. Figure 1 shows the concept of DBS [29], where a bioamplifier (also known as low-noise amplifier (LNA)) and the respective signal processing/control/interface electronics simultaneously acquire the neuronal signals and provide stimulation. The neurostimulator is usually placed in the chest or in the abdominal area, under the skin, so that no parts are exposed or visible. The electrical stimulation modifies the functioning of the neurons around the tips, when the system is turned on, relieving the symptoms of various diseases.

![Figure 1. Concept of deep-brain stimulation (DBS).](image-url)

The first current use of the DBS technique dates back to 1997, when it was authorized by the American FDA (Food and Drug Administration) for its application in the treatment of Parkinson’s disease [30]. Since then, and thanks to their proven success, these systems have become first-line devices in therapies for the relief of symptoms associated with neurological and movement disorders that cannot be achieved with other therapies [31], e.g., chronic pain [32,33], Parkinson’s disease [34,35], tremor [36,37], dystonia [38,39], morbid obesity [40], Tourette syndrome [41], essential tremor [42] and obsessive compulsive disorder [31].

Despite the great successes that were achieved, the neurostimulators are still quite large electronic devices that, in addition to using cables under the skin to connect to the head and then to the stimulation electrodes, still require the replacement of the power...
battery via an invasive surgical procedure every two to four years. In the future, the implants must become more autonomous and less invasive, in order to reduce the heavy burden of replacing their batteries and the discomfort that the implant itself causes to the patient. There exists a pressure from the medical community and patient associations to reduce the discomfort caused by the implant, by reducing the size and weight, increasing the life of the implant through an efficient energy management system, and improving the operational safety, such as when performing magnetic resonance imaging (MRI) or even computed tomography (CT).

There are two paradigms for classifying deep-brain stimulation (DBS), the open-loop DBS (also known as conventional DBS) and the closed-loop DBS (closed-loop DBS also known as adaptive DBS) [43]. In the case of open-loop DBS, a neurologist manually adjusts stimulation parameters every 3–12 months after implantation. On the other hand, in the case of the closed-loop DBS, the adjustment of the stimulation parameters is performed automatically based on measured biomarkers. Biomarkers are acquired signals and can have different natures, namely bioelectrical, psychological, biochemical, among others [43]. Biomarkers are essential indicators on the disease under treatment with closed-loop DBS, because they help to adaptively reconfigure the signals used in neurostimulation [29]. The acquisition of biopotentials is an important component in closed-loop DBS.

For these reasons, and due to the lack in the market of miniaturized systems with potential for safe implantation, the design of CMOS microdevices comprising complete DBS systems has huge socioeconomic impacts both for make available new treatment techniques and to boost the market related to the area of medical instrumentation and healthcare. Figure 2 illustrates the block diagram containing the acquisition, neurostimulator and control modules of a CMOS microdevice for application on DBS. CMOS microdevices similar to the one presented in Figure 2 allow the integration of microsystems for DBS therapies, which have high potential for implantation in the brain. In this context, this paper presents the design of a fully integrated low-noise amplifier (LNA) suitable for recording biological signal within the range of sub-Hz up to 10 kHz.

![Figure 2. A block diagram of a CMOS microdevice containing the acquisition, neurostimulator and control modules for DBS. The LNA module presented in this paper is filled with the yellow color.](image)

2. Design

A low-noise amplifier faces several challenges due to the nature of the signals to amplify, e.g., low-amplitudes and low-frequencies (and being very close to the DC component).
These types of amplifiers for neural recording typically present a mid-band gain of about 40 dB, and a bandwidth ranging from the sub-Hz to 10 kHz [44–53].

Figure 3a shows the schematic of the proposed LNA [46,47]. This amplifier is composed of the two pairs of capacitors $C_1 = 20 \text{ pF}$ and $C_2 = 200 \text{ fF}$, a transconductance operational amplifier (OTA) and a pair of resistors $R_2$. The mid-band voltage gain of this amplifier is given by:

$$A_v = \frac{C_1}{C_2} = 100 = 40 \text{ dB} \quad (1)$$

Figure 3b illustrates the schematic of the OTA, which is composed of eight PMOS and four NMOS: PMOS transistors $M_{5a}$ and $M_{5b}$ form a differential pair; NMOS transistors $M_{4b}$ and $M_{4c}$ form the differential pair load and, also one to one current mirrors with $M_{4a}$ and $M_{4d}$, respectively; PMOS transistors $M_{1a}$ and $M_{1b}$ form another one to one current mirror; PMOS transistor $M_6$ and $M_7$ form the biasing circuit; PMOS transistors $M_{2a}$ and $M_{2b}$ and NMOS transistors $M_{3a}$ and $M_{3b}$ are cascode transistors that increases the impedance of the nodes connected to their drains ($V_{out}$, for instance). The capacitor $C$ is only for understanding purposes because on the final design this one is replaced by $C_x$.

(a) 

(b) 

Figure 3. Cont.
Figure 3. Schematics (a) of the low-noise amplifier, highlighting the pseudo-resistors components, and (b) of the OTA, showing the currents. (c) The transfer function of the LNA for six combinations of $R_2$ an $C_x$.

Figure 3b illustrates the schematic of the OTA, which is composed of eight PMOS and four NMOS: PMOS transistors $M_{a1}$ and $M_{b1}$ form a differential pair; NMOS transistors $M_{a2}$ and $M_{b2}$ forms the differential pair load and, also one to one current mirrors with $M_{d1}$ and $M_{d2}$, respectively; PMOS transistors $M_{a3}$ and $M_{b3}$ forms another one to one current mirror; PMOS transistor $M_6$ and $M_7$ form the biasing circuit; PMOS transistors $M_{a4}$ and $M_{b4}$, and NMOS transistors $M_{a5}$ and $M_{b5}$ are cascode transistors that increases the impedance of the nodes connected to their drains ($V_{out}$, for instance). The capacitor $C_v$ is only for understanding purposes because on the final design this one is replaced by $C_x$.

The OTA converts a voltage difference $V_d = V^+ - V^-$ into a current $I_{out}$. The conversion is such that the current at the output of the OTA is:

$$ I_{out} = g_m \times (V^+ - V^-) \tag{2} $$

where $g_m$ is the transconductance of the OTA. The input signals $V^+$ and $V^-$ must have the same common-mode voltage $V_{CM}$ for a good working of the circuit, e.g., $V^+ = V_{CM} + V_d/2$ and $V^- = V_{CM} - V_d/2$. Under these circumstances:

$$ I_{out} = g_m \times (V^+ - V^-) = g_m V_d \tag{3} $$

The transfer function $H_{LNA}(s)$ of the LNA in terms of the different components is given by (see Appendix A):

$$ H_{LNA}(s) = \frac{V_{out}}{V_{in}} = -\left(\frac{C_v}{C}\right) \times \left[\left(\frac{C_v}{g_m}\right) \times \left(\frac{1 + \frac{C_v}{C} + \frac{C_v}{R_2}}{s^2 + \frac{C_v + C}{g_m} + \frac{C_v}{g_m} + 1}\right)\right] \tag{4} $$

where $g_m$ is the transconductance of the OTA, e.g., $g_m = I_{out}/(V^+ - V^-)$. The reason for the negative sign is explained in the demonstration in Appendix A. Appendix A presents the fully deduction of the transfer function $H_{LNA}(s)$ of the LNA. The capacitance $C_v$ includes all capacitances, either parasitic or connected, of the output node. The parasitic capacitances include the contributions of routing connections, the PADs for the exterior (when applicable), the capacitance wires used for the measurements (when applicable), and the input capacitance of measurement instruments (when applicable).
The transfer function can be simplified in terms of the zeros and poles, resulting in:

\[
H_{\text{LNA}}(s) = -\left(\frac{C_1}{C_2}\right) \times \left[ \left(\frac{C_x^2}{C_x C_1 + C_x C_2 + C_2 C_1}\right) \times \frac{(s - g_m/\pi) \times s}{(s + s_{p1}) \times (s + s_{p2})} \right] \tag{5}
\]

This transfer function can be rewritten as:

\[
H_{\text{LNA}}(s) = -\left(\frac{C_1}{C_2}\right) \times \left[ \left(\frac{C_x^2}{C_x C_1 + C_x C_2 + C_2 C_1}\right) \times \frac{(s - 2\pi f_L) \times s}{(s + 2\pi f_L) \times (s + 2\pi f_H)} \right] \tag{6}
\]

The LNA transfer function contains two zeros, one zero located in the origin and another zero located at \(f_z = g_m/(2\pi C_2)\), and two poles, one pole located in the lower cutoff frequency \(f_L = g_m/[2\pi (C_1 + (C_1/C_2 + 1)C_x)]\). It must be noted that the frequency of the second zero \(f_z\) is much higher than the frequency of any pole. Additionally, the LNA gain between \(f_L\) and \(f_H\) can be determined and its value is approximately \((C_1/C_2)\).

Figure 3b illustrates the transfer function \(H_{\text{LNA}}(f)\) for six combinations of \(R_2\) and \(C_x\). The three plots represented in blue trace use a higher \(R_2\) value and the three plots represented in dashed red traces use a lower value. Both the three blue and red plots were obtained with \(C_x\) equal to 0 pF, 3.9 pF and 9.2 pF. Since the blue plots have a higher \(R_2\), their lower cutoff frequency \(f_L\) are smaller. The upper cutoff frequency \(f_H\) decreases if the capacitance \(C_x\) increases, maintaining constant the value of \(R_2\). In conclusion, the bandwidth of the LNA increases if \(R_2\) increases or \(C_x\) decreases.

Figure 3c illustrates a Bode plot of a generic transfer function with two zeros, two poles, and their relative positions similar to the LNA zeros and poles of this work.

On a fully on-chip solution, the LNA connects internally to the next stage; thus, \(C_x\) is only due the parasitic capacitance of internal connections. However, an internal capacitor \(C_L\) or a switched capacitor array is included on many designs to trim the band, adjusting the pass-band to the desired application. This is achieved by changing the upper cutoff frequency \(f_H\), trimming the capacitance \(C_x\).

The resistor \(R_2\) must present a very high value to guarantee a low cutoff frequency \(f_L\), lower than 1 Hz. Since \(C_2\) is in the order of few tenths of pF, \(R_2\) must be in the order of \(\Omega\). These resistors cannot be implemented in a conventional form in an integrated circuit; neither are commercially available, and if it was the case, the high tolerances would unbalance the circuit in Figure 3a with the two resistors away from each other by a few \(M\Omega\) to a few \(G\Omega\). A widely known technique for implementation of high value resistors is the use of pseudo-resistors [46,53]. Figure 3a also details the implementation of resistors \(R_2\) with pseudo-resistors. These pseudo-resistors are PMOS devices, as detailed with the zoom in the figure, each one composed of six PMOS transistors connected in series. It was found that these pseudo-resistors can reach values in the order of \(\Omega\) and occupy an area many orders of magnitudes lower than the area of a conventional transistor. They are called “pseudo” because it mimics the behavior of a real resistor. The red dots in the terminal A of the pseudo-resistors \(R_2\) serves to show how these pseudo-resistors connects to the LNA. The terminal A of the pseudo-resistors connects to the bulk and source of \(M_{p1}\), while the terminal B connects to the gate and drain of \(M_{p6}\). The bulk of any PMOS \(M_{p(j)}\) connects to the respective source, while the gate connects to the respective drain. Moreover, all PMOS are connected in series.

The most important characteristic of a LNA is its noise. The noise in our LNA is largely caused by the transistors of the OTA. The noise of MOS transistors can be modeled by two current sources from drain to source, and their power spectral density are given by:

\[
\overline{i_{\text{DSIh}}^2} \approx k_b T g_m : \text{thermal noise} \tag{7}
\]
where $k_B$ and $k_f$ are parameters that depend on the fabrication process, $k$ is the Boltzmann constant, $T$ is the temperature in Kelvin, $C_{ox}$ is the gate oxide capacitance, $W$ and $L$ are the transistor dimensions, and $g_m$ is the transistor transconductance.

To evaluate the effect of noise introduced by the transistors, the following procedure is performed:

1. Transpose the transistor noise current sources to the $V_{out}$ node;
2. Find the transfer functions between a current source $I_s$ and $V_{out}$;
3. Find the transfer functions between a current source $I_{out}$ applied to the output and $V_{out}$;
4. Find the input referred noise.

The transposition of the noise current sources is easily performed since in the OTA the noise currents are mirrored to the output. Therefore, the total current at the output node is given by:

$$i_{out}^2 \approx 2k_BTg_m(s + 1) + \frac{k_f}{C_{ox}WL}\frac{R}{s + \frac{1}{R}} + 4k_BTg_m(s + 1) + \frac{k_f}{C_{ox}WL}\frac{R}{s + \frac{1}{R}}$$  \hspace{1cm} (9)

Notice that the noise of the cascode transistors does not affect the OTA noise. The transfer function $H_{out}(s) = V_{out}(s)/I_{out}(s)$ should be deduced as done with $H_{LNA}(s)$. The final expression can be found and is presented below

$$H_{out}(s) = \frac{(C_1 + C_2)}{(C_1C_2 + C_1C_x + C_2C_x)} \cdot \frac{(s + \frac{1}{R_s(C_1 + C_2)})}{(s + s_{p1}) \times (s + s_{p2})}$$  \hspace{1cm} (10)

The transfer function can be simplified, resulting in:

$$H_{out}(s) = \frac{(C_1 + C_2)}{(C_1C_2 + C_1C_x + C_2C_x)} \cdot \frac{(s + \frac{1}{R_s(C_1 + C_2)})}{(s + s_{p1}) \times (s + s_{p2})}$$  \hspace{1cm} (11)

Function $H_{out}(s)$ has the same poles as $H_{LNA}(s)$ and a unique zero: zero $= 1/(R_2(C_2 + C_2))$, $s_{p1} = 1/(R_2C_2)$ and $s_{p2} = g_m/((C_1 + (C_1/C_2 + 1)C_2))$. The pass-band of LNA is located between $s_{p1}$ and $s_{p2}$. The PSD of the noise at the output now can be written, resulting in:

$$PSD_{V_{out}}(f) = \frac{(C_1 + C_x)}{(C_1C_2 + C_1C_x + C_2C_x)} \cdot \frac{1}{(s + s_{p1}) \times (s + s_{p2})} \cdot \frac{1}{g_m} \cdot i_{out}^2$$  \hspace{1cm} (12)

In the LNA pass-band, between $s_{p1}/2\pi$ and $s_{p2}/2\pi$, the PSD value is given by:

$$PSD_{V_{out}}(f) = \frac{(C_1 + C_x)}{C_2} \cdot \frac{1}{g_m} \cdot i_{out}^2$$  \hspace{1cm} (13)

These relations point out that it is important to keep $g_m$ high in order to reduce the output noise. This goal is reached by using large widths for $M_{5a}$ and $M_{5b}$. Finally, the input referred total noise is:

$$Total\ Nois_{input} = LNA_{GAIN} \int_{-\infty}^{+\infty} PSD_{V_{out}}(f)df \approx \frac{C_2}{C_1} \int_{-\infty}^{+\infty} PSD_{V_{out}}(f)df$$  \hspace{1cm} (14)

where $LNA_{GAIN}$ is the gain of the LNA.
fer to the total value. For example, the transistors $M_{1a}$ and $M_{1b}$ with $(W/L)_1 = (13.4 \, \mu m/20 \, \mu m)$ are composed of two parallel transistors, whose dimensions are equal to $(W/L) = (6.7 \, \mu m/20 \, \mu m)$ and at the same time, containing only one finger. In another example, e.g., for the transistors $M_{5a}$ and $M_{5b}$ with $(W/L)_1 = (463 \, \mu m/0.51 \, \mu m)$ are composed of two parallel transistors, whose dimensions are equal to $(W/L) = (231.5 \, \mu m/0.51 \, \mu m)$ and, at the same time, containing 50 fingers for each parallel transistor with $(W/L)_{\text{finger}} = (4.63 \, \mu m/0.51 \, \mu m)$.

| MOSFET             | Total (W/L) | Multiplier (Parallel MOSFETs) | Fingers/Multiplier |
|--------------------|-------------|-------------------------------|-------------------|
| $M_{1a}$, $M_{1b}$ | 13.4 \, \mu m/20 \, \mu m | 2                             | 1                 |
| $M_{2a}$, $M_{2b}$ | 20.6 \, \mu m/0.28 \, \mu m | 2                             | 1                 |
| $M_{3a}$, $M_{3b}$ | 15.4 \, \mu m/0.28 \, \mu m | 2                             | 1                 |
| $M_{4a}$, $M_{4b}$, $M_{4c}$, $M_{4d}$ | 10 \, \mu m/20 \, \mu m | 2                             | 1                 |
| $M_{5a}$, $M_{5b}$ | 463 \, \mu m/0.51 \, \mu m | 2                             | 50                |
| $M_{6}$, $M_{7}$  | 2.3 \, \mu m/5.1 \, \mu m   | 1                             | 1                 |
| Pseudo-resistors  |             |                               |                   |
| $M_{P1}$ to $M_{P6}$ | 1 \, \mu m/1 \, \mu m | 1                             | 1                 |

### 3. Implementation and Simulations

#### 3.1. Layout Issues

Figure 4a illustrates the modifications made to schematics of LNA of Figure 3a for the fabrication. Each output node has a resistor of small value ($\approx 497.6 \, \Omega$) as a preventive protection against connection mistakes such as accidental short-circuits, limiting the output current. Each node with input signals, nodes with reference voltage and biasing nodes has a protection against electrostatic discharges (ESD) [54], an additional resistor $R_{\text{in}}$ of small value ($\approx 497.6 \, \Omega$) and a NMOS. Figure 4b illustrates the schematics of both the ESD protection (on left) and the resistor with NMOS (on right). This last resistance provides an additional level of protection to the gates of the internal circuits. The NMOS presents a width of 3 \, \mu m and a length of 1 \, \mu m. The resistance $R_{\text{BIAS}}$ in the biasing pin is also equal to a small value ($\approx 497.6 \, \Omega$). The capacitance $C_{\text{BIAS}}$ on bias voltage reduces the noise to provide the most stable bias voltage $V_{\text{BIAS}}$ as possible. This capacitance comprises three MIM capacitors with 2 \, fF/\mu m², each one with a total capacitance of 456 \, fF each.

The layout of ESD protections is similar to those proposed by Baker on chapter 4 of his book [55], which is composed of N$^+$ /P-sub and P$^+$ /N-well diodes. Figure 4c illustrates the layout of the ESD protections side-by-side with the respective photograph that was integrated in the fabricated CMOS microdevice. Each N$^+$ /P-sub and P$^+$ /N-well diodes are composed of the parallel of two smaller diodes measuring 16 \, \mu m × 87 \, \mu m. It must be noted that each PAD occupies an area of 62 \, \mu m × 62 \, \mu m.

The MOSFETs $M_1$ to $M_5$ of the OTA in the LNA were drawn with the technique known as common centroid, which provides circuits more resilient to process variations by matching the characteristics of the transistors [55,56]. Each MOSFET was split in two to make these devices immune from cross-chip gradients. Moreover, the gates of the MOSFETs $M_5$ (where the inverting and non-inverting input are connected) were split in several fingers to provide the best matching performance possible and reduce the parasitic capacitances, which are extremely high because of their widths [52]. Figure 5a illustrates the layout of the complete LNA side by side with the respective photograph. Figure 5b illustrated a zoomed view of the layout of the LNA without the array of capacitors $C_1$ for a better visualization. The tags (1) to (3) refers to the sets of input resistances $R_{\text{in}}$ with NMOS in Figure 4a. The capacitors $C_{\text{BIAS1}}$, $C_{\text{BIAS2}}$ and $C_{\text{BIAS3}}$ refers to the three MIM capacitor with 456 \, fF. Each one of the four capacitors $C_{2a}$ and $C_{2b}$ were also implemented with MIM capacitors with 100 \, fF. The common centroids of $M_1$ to $M_5$ of the OTA can be observed.
Figure 4. (a) Illustration of how the ESD protections, input resistance $R_{\text{in}}$ with NMOS and output resistances $R_{\text{ESD}}$ are connected to the low-noise amplifier. (b) Schematics of ESD protections (on left) and resistance with NMOS (on right). (c) Layout of the ESD protections [56].
with 456 fF. Each one of the four capacitors $C_{2a}$ and $C_{2b}$ were also implemented with MIM capacitors with 100 fF. The common centroids of M$_{1}$ to M$_{5}$ of the OTA can be observed. The simulated LNA was the complete schematic of Figure 4a, taking into account the individual contributions of the ESD protections, the input resistor $R_{in}$ with NMOS and the output resistor $R_{ESD}$. The complete schematic was simulated to obtain a better preview

3.2. Low-Noise Amplifier (LNA) Simulations

The behavior of the OTA was simulated in the H-Spice, and it was found a transconductance $g_{m5} \approx 7.58 \mu S$ for the transistors M$_{5a}$ and M$_{5b}$. Thus, the transconductance of the OTA is also $g_{m} \approx 7.58 \mu S$, because it is the same value of $g_{m5}$.

Figure 5. (a) Layout of the complete LNA side by side with the respective photograph, with a reference to the OTA and to the array of two capacitors $C_1$. (b) Zoomed view of the layout of the LNA without the array of capacitors $C_1$ for a better visualization.
of the real conditions. Moreover, simulations were performed without the capacitance $C_x$ (e.g., $C_x = 0$) and with the passive voltage probe to understand the testing conditions. The oscilloscope used in the measurements was the Tektronix model MDO34 3-BW-100. It was used the passive voltage probe Tektronix model TPP0250, with an input capacitance of 3.9 pF.

Figure 6 shows the simulated resistance response of the pseudo-resistors in terms of the voltage $\Delta V = V_{in} - V_{out}$ at its terminals, where $V_{in}$ is the terminal that connects to the bulk of the first PMOS and $V_{out}$ is the terminal that connects to the gate of last PMOS (in concordance with Figure 3a). A voltage pulse source was placed between the $V_{in}$ and $V_{out}$ terminals of the pseudo-resistor, and the voltage were varied between $-0.4$ V and 0.4 V. The current was simulated obtained, and the resistance was calculated by dividing the voltage by the current. Figure 6 shows the result of this simulation with the illustration of the voltage dependence of the pseudo resistance value.

![Figure 6. Voltage dependence of the pseudo resistance.](image)

The total capacitance seen by the LNA output is the sum of the contributions of the parasitic capacitances of the internal metals connections, the PAD for wirebonding to the package, the connections of the test-bed, the 3.9 pF of the passive voltage probe and the cables for connect into the oscilloscope. The capacitance seen by the output of LNA was measured and determined to be equal to 5.3 pF, resulting in 9.2 pF total capacitance, if the voltage probe capacitance is also taken in account.

Figure 7 shows the gain simulation for $C_x = 0$, for $C_x$ equal to the capacitance of the voltage probe ($C_x = 3.9$ pF) and for $C_x$ equal to the total capacitance seen by the LNA output ($C_x = 9.2$ pF) to better understand the effect of the measurement setup.

![Figure 7. Simulated frequency response of the LNA for $C_x = 0$ (red trace), $C_x = 3.9$ pF (blue trace), and $C_x = 9.2$ pF (green trace).](image)
The simulations showed that ideally with $C_x = 0$ the LNA presents a mid-band gain of $\approx 39.4$ dB with a $-3$ dB bandwidth of $\approx 54$ kHz. The simulations also showed that with the effect of the voltage probe, $C_x = 3.9$ pF, the LNA also presents a mid-band gain of $\approx 39.4$ dB, but a $-3$ dB bandwidth of $\approx 3.1$ kHz. For the case of $C_x = 9.2$ pF with the effect of total capacitance seen by the LNA output, the simulations showed a mid-band gain of $\approx 39.4$ dB, but with a $-3$ dB bandwidth of $\approx 1.4$ kHz.

Figure 7 shows the frequency response for frequencies higher that 0.01 Hz. The simulations revealed that this amplifier covers the range of extracellular recorded spikes, from 100 Hz to 6 kHz with a mid-band gain of $\approx 39.4$ dB for the three situations of $C_x = 3.9$ pF.

As illustrated in Figure 8, two different scenarios were supposed, in order to simulate the robustness of the LNA considering the capacitance and resistance associate to the wires that connect the electrodes to the input of the LNA. A sinusoidal input with amplitude of 100 µV and a frequency of 1 kHz was considered. Moreover, the effect of $C_x$ was not considered because it makes no difference in the conclusions. The resistance was considered around 10 Ω in the situation 1. This value is probably higher than those found in a real situation with cables of good quality, but it was an extrapolated value to confirm the previous robustness of the amplifier. The situation 1 considered a serial resistance existent between the positive electrode $E^+$ and the positive input $V_{IP}$ of the bioamplifier, and the one between $E^-$ and $V_{IM}$. The situation 2 considered a capacitor of 100 nF placed in parallel to the voltage source. This situation is merely theoretical because this value is probably higher than those found in a real situation with cables of good quality, but once again, it is also a good test to the reliability of the amplifier. On both situations, the simulations showed an output signal with amplitude of 18.5 mV$\text{pp}$, e.g., a gain of 39.3 dB.

![Figure 8. Scenarios for the simulation of the robustness of the LNA.](image)

The simulated PSD of the output noise is presented in Figure 9. The $C_x$ value considered is 9.2 pF and two curves are traced, shown by a red and a blue curve. In the red curve, only the noise of the OTA transistors is taken in account; in the blue curve, the noise of the pseudo-resistors is also taken in account. The red curve behavior is exactly as described by expression (12). When the pseudo-resistors noise is added, the low frequency noise is increased.

![Figure 9. PSD noise of the LNA: in the red curve, only the noise of the OTA transistors is taken in account; in the blue curve, the noise of the pseudo-resistors is also taken in account.](image)
The input referred noise of the LNA, find in the simulation, is 6.2 µV RMS (from 0.5 Hz to 50 kHz), when all noise sources are taken in account.

4. Experimental

4.1. Instruments and Setup

Figure 10 shows the schematic of the setup used during the measurements. This setup is composed of the microdevice under test itself, a test-bed board (shaded in gray) especially designed for the tests, an arbitrary signal generator Tektronix model AFG1022 with two simultaneous outputs and 25 MHz of bandwidth, an oscilloscope Tektronix model MDO34 3-BW-100 with four input channels and 100 MHz of bandwidth, passive voltage probes Tektronix model TPP0250, an external protoboard to facilitate the connection of bias resistors, and a multimeter to measure the voltage supply to ensure that it is within the valid tolerance range and/or other signals such as references and common mode voltages. The photograph shows a specific situation of testing. The external connections can be maintained unaltered to test other blocks in the microdevice, simply by redirecting the signals throughout dip-switches. Moreover, the dip-switches also can activate and deactivate several blocks within the microdevice. The test-bed board was designed to be supplied by a DC power jack, targeted to a typical supply voltage of 5 V. The test-bed can support supply voltages up to 16 V, whose value is limited by the voltage regulator TLV1117. This voltage regulator provides the required nominal voltage of 1.8 V to supply the CMOS microdevice. The common mode voltage $V_{CM}$ required to make the LNA work can be achieved in two ways: from an external voltage source or from an operational amplifier LM358, placed in the test-bed itself, working as voltage follower of half the nominal supply voltage, 0.9 V. A dip-switch allows the selection of the $V_{CM}$ source.

Figure 10. Schematic of the experimental setup for the characterization of the microdevice. The inset shows the setup photograph.
4.2. Results

Figure 11 shows the measured gain of the LNA and the simulated values. The amplitude of the input signals was settled to 4 mV_{pp}. The LNA presents a mid-band gain of \( \approx 38.6 \) dB, which is close to the simulated results. Moreover, the −3 dB bandwidth was \( \approx 2.3 \) kHz. For frequencies higher than 10 kHz, the measured gain approaches asymptotically to the simulated gain with \( C_x = 9.2 \) pF, although, for frequencies between 1 kHz and 10 kHz, the measured gain is slightly higher than the simulated gain.

![Figure 11. Measured gain and comparison with simulations for \( C_x = 0 \), \( C_x = 3.9 \) pF and \( C_x = 9.2 \) pF.](image)

Notice that the upper cutoff frequency of the measured results is smaller than the ideally simulated value (pink plot in Figure 11, where \( C_x = 0 \) pF). It is caused by the contributions of the parasitic capacitances seen from the LNA output. The length of the cables to connect the test-bed to the oscilloscope was the smallest possible to decrease their contribution to the total capacitance \( C_x \). The gain at 6 kHz is \( \approx 29.5 \) dB, 9 dB below the mid-band gain, and is still an acceptable value. Higher gains are expected in a definitive LNA application, where the output of the LNA is directly connects to a multiplexer, and most of the parasitic capacitances are not present anymore. In other words, the total capacitance \( C_x \) seen by the output of LNA will be drastically reduced, and therefore, the desired gain at 6 kHz will be increased.

An important test implemented is the characterization of the behavior of the gain to variations of the common-mode voltage \( V_{CM} \). Figure 12 shows the measured gain for a common-voltage variation of ±0.1 V and ±0.2 V from the nominal value \( V_{CM} = V_{dd}/2 = 0.9 \) V. It is possible to observe that the gain has no sensitivity to small variations of common-mode voltage; thus, the LNA shows to be robust to these variations.

![Figure 12. Measured gain in terms of the common-mode voltage \( V_{CM} \).](image)
Figure 13 illustrates the measurement results for these tests. The first input signals present an amplitude of 10 mVpp and interestingly, the gain was slightest higher than the gain obtained with an amplitude of 4 mVpp, with a mid-band gain of ≈39.3 dB. The output signal in this first test presented a signal excursion of $\Delta V_{out} = 920$ mVpp, e.g., $\Delta V_{out}$ is almost equal to $V_{dd}/2$. The second test was more stressful, with an input amplitude of 20 mVpp. In general, the gain is lower than those obtained with input signals with lowest amplitudes. This was almost expected because this pushes the output signal to present an excursion equal or higher than the supply voltage $V_{dd}$.

The two scenarios illustrated in Figure 8 were also tested. The amplitude of the input signals was settled to 4 mVpp. These two scenarios are exaggerated when compared with real situations, but, for this reason, they are good for validating the robustness of the LNA. The results in Figure 13 revealed that the measured mid-band gain was almost equal to the values presented in Figure 11, where the measurement conditions were optimized with cables of high quality and short length.

![Figure 13. Measured gain for two sets of stress tests: input amplitudes of 10 mVpp and 20 mVpp, and cables from the electrodes with two serial resistance of 10 Ω and with a parallel capacitance of 100 nF.](image)

The LNA was also tested with low-amplitude signals. These tests used a custom home-made signal generator able to generate sine waves with amplitudes of either 60 µVpp or 130 µVpp. The behavior was not very different from those observed in Figure 11 with an amplitude of 4 mVpp; however, the measured gain was slightly lower, e.g., ≈37.7 dB or less than 1 dB in relation to the 38.6 dB measured with the former.

A new set of tests were performed, each consisting of applying signals in saline solution with characteristics equivalent to those observed in neuronal tissues, to test the robustness of the LNA. Moreover, these saline tests were also performed to avoid ethical issues related to experimentation with in vivo human subjects and animals, and, at the same time, to get an idea about the phenomena in the brain.

In these tests, several electrodes were immersed in a jar filled with saline solution (saline solution consisting of sodium chloride solute dissolved in distilled water solvent in the proportion of 0.9%). The saline solution emulates very well the ionic species of the human tissue in terms of the electrical parameters.

Figure 14a shows the schematic of the experimental setup for these tests, which is composed of the signal generator, oscilloscope, test-bed board, CMOS microdevice and the bias resistor previously described. The power supply management is not displayed. Moreover, this setup is composed of a jar filled with a saline solution and by a tip with an array of electrodes. The tip is fabricated by additive manufacturing with 3D printing of PLA (polylactic acid) and filaments.
with a diameter of 1.75 mm. The array of electrodes comprises a pair of injection electrodes and a pair of reading electrodes. It was performed a frequency sweep applied to a sinusoidal wave injected in the two injection electrodes. Then, the signals were sensed from the saline solution with the reading electrodes and further amplified by the LNA. Figure 14b illustrates a photograph of the tip with the array of electrodes.

Figure 14. (a) Schematic of the saline solution setup. The inset shows the setup photograph. (b) Photograph of the 3D printed tip with the array of electrodes. (c) Measured gain of the LNA.
Another set of tests were performed to evaluate the transient responses of the LNA. It can be observed that the gain behavior is the same observed in the first tests for frequencies above 100 Hz, and it is slightly lower at frequencies below 100 Hz. The amplitude of the signals injected in the saline solution has 40 mV<sub>pp</sub> for all frequencies, while the amplitude of the signal sensed in the pair of reading electrodes was also 18 mV<sub>pp</sub> for all frequencies.

Another set of tests were performed to evaluate the transient responses of the LNA. These tests consisted of the injection of two square waves into the input of the LNA. The amplitudes of these waves were settled to 20 mV<sub>pp</sub>, while their frequencies were settled to 1.15 kHz and 200 Hz. Figure 15a,b shows the signals at the output of the LNA for these frequencies, respectively.

Figure 14c illustrated the measured gain of the LNA when subjected to these tests. It can be observed that the gain behavior is the same observed in the first tests for frequencies above 100 Hz, and it is slightly lower at frequencies below 100 Hz. The amplitude of the signals injected in the saline solution has 40 mV<sub>pp</sub> for all frequencies, while the amplitude of the signal sensed in the pair of reading electrodes was also 18 mV<sub>pp</sub> for all frequencies.

Figure 15. LNA response for input waves with square shape, amplitude of 20 mV and frequencies of (a) 1.15 kHz and (b) 200 Hz.

Figure 15a shows the low-pass effect due to the upper cutoff frequency <i>f_H</i>. The frequency of 1.15 kHz is very close to the upper cutoff frequency of the LNA, and it was
selected for this reason. The plot \( v_{\text{fitted},H}(t) \), in red, illustrates the effect of the upper cutoff frequency \( f_H \) and it was fitted to:

\[
v_{\text{fitted},H}(t) = V_{0,H} + A_H \times \left(1 - e^{-\frac{t}{\tau_H}}\right)
\]

where \( V_{0,H} = 0.24 \) V, \( A_H = 1.32 \) V. The time constant \( \tau_H \) was calculated in order to \( v_{\text{fitted},H}(t) \) agree the best as possible with the rising portion of the output signal. The estimation of this time constant resulted on \( \tau_H \approx 69 \) \( \mu \)s, meaning an upper cutoff frequency of \( f_H = 1/(2\pi\tau_H) \approx 2.31 \) kHz, which is practically equal to the \(-3\) dB frequency in Figure 11.

Figure 15b shows the high-pass effect due to the lower cutoff frequency \( f_L \) of the LNA. The frequency of 200 Hz was selected due to be close to the lower cutoff frequency of the LNA. The plot \( v_{\text{fitted},L}(t) \), in red, illustrates the effect of the lower cutoff frequency \( f_L \) and was fitted to:

\[
v_{\text{fitted},L}(t) = V_{0,L} + A_L \times e^{-\frac{t}{\tau_L}}
\]

where \( V_{0,L} = 1.35 \) V, \( A_L = 0.37 \) V. The time constant \( \tau_L \) was also calculated in order to \( v_{\text{fitted},L}(t) \) agree the best as possible with the falling portion of the output signal. The estimation of this time constant resulted on \( \tau_L \approx 562.9 \) \( \mu \)s, meaning a lower cutoff frequency of \( f_L = 1/(2\pi\tau_L) \approx 282.7 \) kHz. It is interesting to observe that the plot \( v'_{\text{fitted},H}(t) \) with the pink trace still illustrates the effect of the upper cutoff frequency \( f_H \) and this time was fitted to:

\[
v'_{\text{fitted},H}(t) = V'_{0,H} + A'_H \times \left(1 - e^{-\frac{t}{\tau'_H}}\right)
\]

where \( V'_{0,H} \approx 0.41 \) V, \( A'_H \approx 1.35 \) V. The red and pink plots illustrate the effects of the lower and the higher cutoff frequencies, respectively.

To finish, the common-mode voltage at the output of LNA was measured to be 898 mV (\( \approx 0.9 \) V or \( V_{dd}/2 \)) in all measurements with the input common-mode \( V_{CM} \) equal to 0.9 V.

### 5. Conclusions

This paper presented a low-noise amplifier (LNA) optimized for application on deep-brain stimulation (DBS). This LNA was designed and fabricated in the CMOS 0.18 \( \mu \)m from TSMC. The tests were performed without a buffer in the output of the LNA to achieve the best and complete characterization as possible. The drawback of the absence of a buffer was the rise of parasitic capacitances associated with the conditions of how the tests were performed that were seen by the output of the LNA, more specifically, the contributions of the internal metals of the microdevice, the PADs that connect to the packaging, the ESD protections, the tracks in the test-bed board, the wires and the passive voltage probe of the oscilloscope. Nonetheless, the total contribution was measured and agrees very well with the simulations, meaning that in a final integration this effect is hugely mitigated. Table 2 compares this LNA with few related key works found in the literature [44–53]. It was calculated the figure-of-merit (FOM) to better rank and compare this work with the best state of the art [1,44–53] with respect to thermal power-noise trade-off. The noise efficiency factor (NEF) was presented in 1987 by Steyaert et al. [57], and since then, it has been widely used and given by:

\[
NEF = IRN \times \frac{2l_{\text{total}}}{\pi \times U_T \times (4kT) \times BW}
\]

where \( l_{\text{total}} \) is the total current absorbed by the amplifier stage (this current excludes the amount absorbed by the bias stage), \( U_T \) is the thermal voltage given by \( kT/q \) (\( \approx 26 \) mV at the room temperature of 300 K), \( k \) is the Boltzmann constant given by 1.38064852 \times 10^{-23} \text{ m}^2 \text{ kg} \text{s}^{-2} \text{ K}^{-1} \), \( T \) the room temperature expressed in Kelvin, and \( IRN \) \[V_{RMS}\] the input-referred noise. It must be noted that this FOM compares the power-noise trade-off with that of a single ideal bipolar transistor. The lowest the FOM, the better will be the LNA with relation to the global noise performance. The figure-of-merit is defined as the ratio of the \(-3\) dB
bandwidth $BW_{kHz}$, expressed in kHz, by the product of the power consumption $P_{\mu W}$ in $\mu W$ with the input-referred noise (IRN) in $\mu V_{RMS}$. Table 2 lists and compares this LNA with those found in the literature.

Table 2. Comparison of this low-noise amplifier with the state of the art.

| Ref. | CMOS Process | Mid-Band Gain [dB] | Bandwidth [kHz] | Voltage [V] | Power [$\mu W$] | Area [mm$^2$] | IRN [$\mu V_{RMS}$] | FOM (e.g., the NEF) |
|------|--------------|---------------------|----------------|------------|----------------|-------------|----------------|------------------|
| This work | 0.18 $\mu$m | 38.6 | 2.3 | 1.8 | 2.8 | 0.035 | 6.2 | 6.19 |
| [1] | 0.13$\mu$m | 40.5 | 8.1 | 1 | 12.5 | 0.047 | 3.1 | 4.4 |
| [44] | 28 nm | 51.3 | 3 | 0.5 | 0.9 | N/A | 6.85 | 3.40 |
| [45] | 65 nm | 47.48 | 3 | 0.75 | 6 | N/A | 1.40 | 2.78 |
| [46] | 1.5 $\mu$m | 39.5 | 7.2 | 7.2 | 80 | 0.16 | 2.2 | 3.80 |
| [47] | 0.5 $\mu$m | 40.85 | 5.32 | 2.8 | 7.5 | 0.16 | 1.66 | 3.21 |
| [48] | 65 nm | 47.48 | 3 | 0.75 | 6 | N/A | 1.40 | 2.78 |
| [49] | 0.18 $\mu$m | 50 | 9.2 | 1.2 | 8.6 | 0.05 | 5.6 | 4.90 |
| [50] | 0.13 $\mu$m | 40 | 10.5 | 1 | 12.1 | 0.072 | 3.2 | 2.90 |
| [51] | 0.18 $\mu$m | 40 | 7.5 | 1.2 | 4.8 | 0.022 | 3.87 | 3.44 |
| [52] | 0.5 $\mu$m | 49.26 | 12.9 | 3.3 | 26 | 0.014 | 3.16 | 2.53 |
| [53] | 0.18 $\mu$m | 40 | 7.4 | 1 | 3.44 | 0.012 | 4.27 | 3.07 |

To finish, Figure 16 shows a photograph of the fabricated CMOS microdevice, which occupies 1660 $\mu$m $\times$ 1660 $\mu$m of area. Moreover, this figure also makes an emphasis to the LNA presented in this paper and an emphasis to one of the ESD protections for a better illustration and understanding.

Figure 16. Photograph of the fabricated CMOS microdevice (1660 $\mu$m $\times$ 1660 $\mu$m), with emphasis on the LNA presented in this paper and on one of the ESD protections.

Author Contributions: Conceptualization, T.M.N., R.H.G. and J.P.P.d.C.; methodology, T.M.N., R.H.G. and J.P.P.d.C.; validation, T.M.N. and R.H.G.; writing—original draft preparation, T.M.N., R.H.G. and J.P.P.d.C.; supervision, E.T.F. and E.C.; project administration, M.L., J.N.S.J., J.P.P.d.C. and M.A.R.; funding acquisition, M.L., J.N.S.J., J.P.P.d.C. and M.A.R. All authors have read and agreed to the published version of the manuscript.
Funding: This work was partially supported by the FAPESP agency (Fundação de Amparo à Pesquisa do Estado de São Paulo) through the project with the reference 2019/05248-7. The CMOS microdevice and packaging was offered by IMEC free of any charge, in the scope of IMEC-Brazil program. The CMOS microdevice was fabricated in the scope of IMEC-Brazil program. Tiago Mateus Nordi was sponsored by Federal University of São Carlos (USFCar). Rodrigo Henrique Gounella was supported with a PhD scholarship from CAPES (Coordenação de Aperfeiçoamento de Pessoal de Nível Superior). João Paulo Carmo was support by a PQ scholarship with the reference CNPq 304312/2020-7.

Acknowledgments: We would also like to acknowledge to Jacobus Swart from the University of Campinas for his kind and readily available assistance during the whole process and intermediation with IMEC.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A
Deduction of the Transfer Function of the LNA
This deduction takes into account $V_{IM} = V_{in} + V_{ref}$ and $V_{IP} = V_{ref}$, in a similar way as stated by Wattanapanitch et al. [47], where both signals include dc and ac components. According to Figure 3a, the ac output current of the output of the OTA is given by:

$$I_{out} = g_m \times (V^+ - V^-) = -g_m V^-$$  \hspace{1cm} (A1)

with $V^+ = 0$ V for ac. This current flows throughout the load impedances $Z_x = (sC_x)^{-1}$ and $Z_2 = R_2/(sR_2C_2 + 1)$ in the feedback path, e.g.,

$$I_{out} = \frac{V_{out}}{Z_x} + \frac{V_{out} - V^-}{Z_2}$$  \hspace{1cm} (A2)

The voltage $V^-$ at the inverting input of the OTA is given by:

$$V^- = \frac{Z_2}{Z_1 + Z_2} V_{in} + \frac{Z_1}{Z_1 + Z_2} V_{out}$$  \hspace{1cm} (A3)

with $Z_1 = (sC_1)^{-1}$. Thus,

$$- \frac{g_m Z_2}{Z_1 + Z_2} V_{in} - \frac{g_m Z_1}{Z_1 + Z_2} V_{out} = \frac{V_{out}}{Z_x} + \frac{V_{out} - V^-}{Z_2}$$  \hspace{1cm} (A4)

replacing the voltage $V^-$ in (A3), the previous equation becomes:

$$- \frac{g_m Z_2}{Z_1 + Z_2} V_{in} - \frac{g_m Z_1}{Z_1 + Z_2} V_{out} = \frac{V_{out}}{Z_x} + \frac{V_{out} - \frac{V_{in}}{Z_1 + Z_2} - \frac{Z_1}{Z_2(Z_1 + Z_2)} V_{out}}{Z_2}$$  \hspace{1cm} (A5)

The transfer function can be obtained after few algebraic manipulations, resulting in:

$$H_{LNA} = \frac{Z_x(1 - g_m Z_2)}{Z_x(1 + g_m Z_1) + Z_1 + Z_2}$$  \hspace{1cm} (A6)

The first proof is to check the validity of the previous equation of $H_{LNA}$. This is performed by assuming $C_x = 0$ F, thus, $Z_x = \infty$. The transfer function is then:

$$H_{LNA} = \lim_{Z_x \to \infty} \left[ \frac{Z_x(1 - g_m Z_2)}{Z_x(1 + g_m Z_1) + Z_1 + Z_2} \right] = \frac{1 - g_m Z_2}{1 + g_m Z_1}$$  \hspace{1cm} (A7)

Since $g_m Z_{1,2} \gg 1$ then:

$$H_{LNA} \approx - \frac{g_m Z_2}{g_m Z_1} = - \frac{Z_2}{Z_1} = - \frac{C_1}{C_2}$$  \hspace{1cm} (A8)
The module of $H_{\text{LNA}}$ is equal to the mid-band gain of the LNA $A_v = \vert H_{\text{LNA}} \vert = C_1/C_2$. The transfer function $H_{\text{LNA}}$ is negative, but this is not a problem because the input signal $V_{\text{in}}$ connects to the inverting input. This analysis was conducted under this assumption to facilitate the demonstration of $H_{\text{LNA}}$. For $V_{\text{IM}} = V_{\text{ref}}$ and $V_{\text{IP}} = V_{\text{in}} + V_{\text{ref}}$, the transfer function would be $H_{\text{LNA}} = +C_1/C_2$. The negative signal must be included in the end of this demonstration.

The fully transfer function in terms of all components present in the LNA can be further manipulated to obtain:

$$H_{\text{LNA}}(s) = \left( \frac{C_1}{C_2} \right) \times \left[ \frac{s^2 R_2 C_2 - s(g_m R_2 - 1)}{s^2 R_2 (C_1 + C_x + \frac{C_1 C_x}{C_2}) + s(g_m R_2 + \frac{g_m}{C_2}) + \frac{g_m}{C_2}} \right]$$  \hspace{1cm} (A9)

The transfer function can be further simplified taking into account that $g_m R_2 >> 1$ and $g_m R_2 >> C_i/C_j$ for any combination of $\{C_i, C_j\}$ equal to $\{C_1, C_2, C_x\}$. In this situation:

$$H_{\text{LNA}}(s) \approx \left( \frac{C_1}{C_2} \right) \times \left[ \frac{(s R_2 C_2 - g_m R_2) s}{s^2 R_2 (C_1 + C_x + \frac{C_1 C_x}{C_2}) + s(g_m R_2 + \frac{g_m}{C_2}) + \frac{g_m}{C_2}} \right]$$ \hspace{1cm} (A10)

and finally

$$H_{\text{LNA}}(s) = \left( \frac{C_1}{C_2} \right) \times \left[ \frac{R_2 C_2}{g_m} \times \frac{(s - \frac{g_m}{C_2}) s}{s^2 R_2 (C_1 + C_x + \frac{C_1 C_x}{C_2}) + s(g_m R_2 + \frac{g_m}{C_2}) + \frac{g_m}{C_2}} \right]$$ \hspace{1cm} (A11)

This transfer function can be simplified in terms of the zeros and poles, resulting in:

$$H_{\text{LNA}}(s) = \left( \frac{C_1}{C_2} \right) \times \left[ \frac{C_2}{C_1 C_2 + C_1 C_x + C_2 C_x} \times \frac{(s - \frac{g_m}{C_2}) s}{(s + \frac{s_p1}{2}) \times (s + \frac{s_p2}{2})} \right]$$ \hspace{1cm} (A12)

The transfer function contains one zero located in the origin and another located at $f_z = g_m/(2\pi C_2)$ and two poles $s_{p1}$ and $s_{p2}$. The poles of $H_{\text{LNA}}(s)$ are given by:

$$\begin{align*}
\frac{g_m C_2}{2(C_1 C_2 + C_1 C_x + C_2 C_x)} & \times \left( 1 - \sqrt{1 - \frac{4(C_1 C_2 + C_1 C_x + C_2 C_x)}{g_m R_2 C_2^2}} \right) \\
\frac{g_m C_2}{2(C_1 C_2 + C_1 C_x + C_2 C_x)} & \times \left( 1 + \sqrt{1 - \frac{4(C_1 C_2 + C_1 C_x + C_2 C_x)}{g_m R_2 C_2^2}} \right)
\end{align*}$$ \hspace{1cm} (A13)

A further simplification can be made with the poles relation if we consider $g_m R_2 >> 1$. In this case, we assume that:

$$\frac{4(C_1 C_2 + C_1 C_x + C_2 C_x)}{g_m R_2 C_2^2} << 1$$ \hspace{1cm} (A14)

and the poles relations are:

$$\begin{align*}
\frac{g_m C_2}{2(C_1 C_2 + C_1 C_x + C_2 C_x)} \times \left( 1 - \left( 1 + \frac{2(C_1 C_2 + C_1 C_x + C_2 C_x)}{g_m R_2 C_2^2} \right) \right) \\
\frac{g_m C_2}{2(C_1 C_2 + C_1 C_x + C_2 C_x)} \times (1 + 1) = \frac{g_m C_2}{(C_1 C_2 + C_1 C_x + C_2 C_x)}
\end{align*}$$ \hspace{1cm} (A15)
References

1. Holleman, J.; Zhang, F.; Otis, B. Ultra Low-Power Integrated Circuit Design for Wireless Neural Interfaces, 1st ed.; Springer: New York, NY, USA, 2011.

2. Wolpaw, J.R.; Birbaumer, N.; McFarland, D.J.; Pfurtscheller, G.; Vaughan, T.M. Brain–computer interfaces for communication and control. Clin. Neurophysiol. 2022, 113, 767–791. [CrossRef]

3. Nagel, H. Biopotential Amplifiers. In The Biomedical Engineering Handbook, 2nd ed.; Bronzino, E.J.D., Ed.; CRC Press LLC.: Boca Raton, FL, USA, 2000.

4. Sinnich, S.; Bahr, A.; Rieger, R. Noise Efficient Integrated Amplifier Designs for Biomedical Applications. Electronics 2021, 10, 1522. [CrossRef]

5. Castro-García, J.A.; Molina-Cantero, A.J.; Gómez-González, I.M.; Lafuente-Arroyo, S.; Merino-Monge, M. Towards Human Stress and Activity Recognition: A Review and a First Approach Based on Low-Cost Wearables. Electronics 2022, 11, 155. [CrossRef]

6. Ali, H.; Naing, H.H.; Yaqub, R. An IoT Assisted Real-Time High CMRR Wireless Ambulatory ECG Monitoring System with Arrhythmia Detection. Electronics 2021, 10, 1871. [CrossRef]

7. Taalla, R.V.; Arefin, S.; Kaynak, A.; Kouzani, A.Z. A review on miniaturizes ultrasonic wireless power transfer to implantable medical devices. IEEE Access 2018, 7, 2092–2106. [CrossRef]

8. Ballo, A.; Bottaro, M.; Grasso, A.D. A review of power management integrated circuits for ultrasound-based energy harvesting in implantable medical devices. Appl. Sci. 2021, 11, 2487. [CrossRef]

9. Chen, Q.; Kastratovic, S.; Eid, M.; Ha, S. A Non-Contact Compact Portable ECG Monitoring System. Electronics 2021, 10, 2279. [CrossRef]

10. Fernandes, M.; Correia, J.; Mendes, P. Electro-optic acquisition system for ECG wearable sensor applications. Sens. Actuators A Phys. 2013, 203, 316–323. [CrossRef]

11. Chebli, R.; Ali, M.; Sawan, M. High-CMRR Low-Noise Fully Integrated Front-End for EEG Acquisition Systems. Electronics 2019, 8, 1157. [CrossRef]

12. Dias, N.S.; Carmo, J.P.; Mendes, P.M.; Correia, J.H. Wireless instrumentation system based on dry electrodes for acquiring EEG signals. Med. Eng. Phys. 2012, 43, 972–981. [PubMed]

13. Pinho, F.; Cercqueira, J.; Correia, J.H.; Sousa, N.; Dias, N.S. MyBrain: A novel EEG embedded system for epilepsy monitoring. J. Med. Eng. Technol. 2017, 41, 564–585. [CrossRef]

14. Chen, R.; Canales, A.; Anikeeva, P. Neural recording and modulation technologies. Nat. Rev. Mater. 2017, 2, 16093. [CrossRef] [PubMed]

15. Jun, J.J.; Steinmetz, N.A.; Siegle, J.H.; Denman, D.J.; Bauta, M.; Barbarits, B.; Lee, A.K.; Anastassiou, C.A.; Andrei, A.; Aydin, Ç.; et al. Fully Integrated Silicon Probes for High-Density Recording of Neural Activity. Nature 2017, 551, 7679. [CrossRef]

16. Marblestone, A.H.; Zamft, B.M.; Maguire, Y.G.; Shapiro, M.G.; Cybulski, T.R.; Glaser, J.I.; Eamodei, D.; Estranges, P.B.; Ekalhor, R.; Dalrymple, D.A.; et al. Physical principles for scalable neural recording. Front. Comput. Neurosci. 2013, 7, 137. [CrossRef] [PubMed]

17. Boyd, E.S.; Zhang, F.; Bamberg, E.; Nagel, G.; Deisseroth, K. Millisecond-timescale, genetically targeted optical control of neural activity. Nat. Neurosci. 2005, 8, 1263–1268. [CrossRef]

18. Deisseroth, K. Optogenetics. Nat. Methods 2011, 8, 26–29. [CrossRef]

19. Deisseroth, K. Optogenetics: 10 years of microbial opsins in neuroscience. Nat. Neurosci. 2011, 14, 1213–1225. [CrossRef]

20. Park, S.I.; Brenner, D.S.; Shin, G.; Morgan, C.D.; Copits, B.A.; Chung, H.U.; Pullen, M.Y.; Noh, K.N.; Davidson, S.; Oh, S.J.; et al. Soft, stretchable, fully implantable miniaturized optoelectronic systems for wireless optogenetics. Nat. Biotechnol. 2015, 33, 1280–1288. [CrossRef]

21. Zhang, Y.; Castro, D.C.; Han, Y.; Wu, Y.; Guo, H.; Weng, Z.; Xue, Y.; Ausra, J.; Wang, X.; Li, R.; et al. Battery-free, lightweight, injectable microsystem for in vivo wireless pharmacology and optogenetics. Proc. Natl. Acad. Sci. USA 2019, 116, 21427–21437. [CrossRef]

22. Engelen, M.; Obien, J.; Deligkaris, K.; Bullmann, T.; Bakkum, D.J.; Frey, U. Revealing neuronal function through microelectrode array recordings. Front. Neurosci. 2015, 8, 1–30. [CrossRef]

23. Sui, Y.; Tian, Y.; Ko, W.K.D.; Wang, Z.; Jia, F.; Horn, A.; de Ridder, D.; Choi, K.S.; Bari, A.A.; Wang, S.; et al. Deep brain stimulation initiative: Toward innovative technology, new disease indications, and approaches to current and future clinical challenges in neuromodulation therapy. Front. Neurol. 2019, 11, 59745. [CrossRef]

24. Hickey, P.; Stacy, M. Deep Brain Stimulation: A Paradigm Shifting Approach to Treat Parkinson’s Disease. Front. Neurosci. 2016, 10, 173. [CrossRef] [PubMed]

25. Appleby, B.S.; Duggan, P.S.; Regenberg, A.; Rabins, P.V. Psychiatric and neuropsychiatric adverse events associated with deep brain stimulation: A meta-analysis of ten years’ experience. Mov. Disord. 2007, 22, 1722–1728. [CrossRef] [PubMed]

26. Sterman, J.; Cunqueiro, A.; Dym, R.J.; Spektor, M.; Lipton, M.L.; Rezvin, M.V.; Scheinfeld, M.H. Implantable Electronic Stimulation Devices from Head to Sacrum: Imaging Features and Functions. RadioGraphics 2019, 39, 1056–1074. [CrossRef]

27. Medtronic DBS Therapy for Parkinson’s Disease, Medtronic Inc., Catalog UC2016071888EE. 2020. Available online: https://asiapac.medtronic.com/content/dam/medtronic-com/uk-en/patients/documents/parkinsons-disease/pd-brochure-uc2016071888ee.pdf?bypassM=truelead (accessed on 5 March 2022).
28. Vercise™ DVBS Leads: Directions for Use, Boston Scientific Corporation, Catalog 91172963-02 REV A 2017-02. 2017. Available online: https://www.bostonscientific.com/content/dam/Manuals/eu/current-rev-da/91172963-02_Vercise%E2%84%A2_DBS_Leads_DFU_multi-0US_s.pdf (accessed on 1 December 2021).

29. Hoang, K.C.; Cassar, I.R.; Grill, W.M.; Turner, D.A. Biomarkers and Stimulation Algorithms for Adaptive Brain Stimulation. Front. Neurosci. 2017, 11, 1–15. [CrossRef]

30. Fins, J.J. Chapter 9: Deep Brain Stimulation: Ethical Issues in Clinical Practice and Neurosurgical Research. In Neuromodulation; Academic Press: Cambridge, MA, USA, 2009; pp. 81–91.

31. Kringelbach, M.L.; Jenkinson, N.; Owen, S.L.F.; Aziz, T.Z. Translational principles of deep brain stimulation. Nat. Rev. Neurosci. 2007, 8, 623–635. [CrossRef] [PubMed]

32. Owen, S.L.; Green, A.L.; Stein, J.; Aziz, T.Z. Deep brain stimulation for the alleviation of post-stroke neuropathic pain. Pain 2006, 120, 202–206. [CrossRef]

33. Marchand, S.; Kupers, R.; Bushnell, C.M.; Duncan, G.H. Analgesic and placebo effects of thalamic stimulation. Pain 2003, 105, 481–488. [CrossRef]

34. Bittar, R.G.; Burn, S.C.; Bain, P.G.; Owen, S.L.; Joint, C.; Shlugman, D.; Aziz, T.Z. Deep brain stimulation for movement disorders and pain. J. Clin. Neurosci. 2005, 12, 457–463. [CrossRef] [PubMed]

35. Cury, R.; Galhardoni, R.; Fonoff, E.T.; Lloret, S.P.; Ghilardi, M.D.S.; Barbosa, E.R.; Teixeira, M.; De Andrade, D.C. Sensory abnormalities and pain in Parkinson disease and its modulation by treatment of motor symptoms. Eur. J. Pain 2015, 20, 151–165. [CrossRef]

36. Rehncrona, S.; Johnels, B.; Widner, H.; Tornqvist, A.-L.; Hariz, M.; Sydow, O. Long-term efficacy of thalamic deep brain stimulation for tremor: Double-blind assessments. Mov. Disord. 2003, 18, 163–170. [CrossRef]

37. Ghilardi, M.G.D.S.; Ibarra, M.; Alho, E.J.; Reis, P.R.; Contreras, W.O.L.; Hamani, C.; Fonoff, E.T. Double-target DBS for essential tremor: 8-contact lead for c2l and Vim aligned in the same trajectory. Neurology 2018, 90, 476–478. [CrossRef]

38. Fonoff, E.T.; Ghilardi, M.G.d.S.; Cury, R.G. Neurocirurgia funcional para o Clínico: Estimulação Cerebral Profunda em Doença de Parkinson, Distoria e Outros Distúrbios do Movimento. In Conclusões em Neurologia, 11th ed.; Nitriti, R., Ed.; Manole Editora: Barueri, Brazil, 2016; pp. 53–67. (In Portuguese)

39. Vidalheth, M.; Vercueil, L.; Houeto, J.-L.; Krystkowski, P.; Benabid, A.-L.; Cornu, P.; Lagrange, C.; Montcel, S.T.d.; Dormont, D.; Grand, S.; et al. Bilateral deep-brain stimulation of the globus pallidus in primary generalized dystonia. N. Engl. J. Med. 2005, 352, 459–467. [CrossRef]

40. Franco, R.; Fonoff, E.T.; Alverenga, P.; Lopes, A.C.; Miguel, E.C.; Teixeira, M.J.; Damiani, D.; Hamani, C. DBS for Obesity. Brain Sci. 2016, 6, 21. [CrossRef]

41. Almeida, L.; Martinez-Ramirez, D.; Rossi, P.J.; Peng, Z.; Gunduz, A.; Okun, M.S. Chasing ticks in the human brain: Development of open, scheduled and closed loop responsive approaches to deep brain stimulation for tourette syndrome. J. Clin. Neurol. 2015, 11, 122–131. [CrossRef]

42. Herron, J.A.; Thompson, M.C.; Brown, T.; Chizeck, H.J.; Ojemann, J.G.; Ko, A.L. Chronic electrocorticography for sensing movement intention and closed-loop deep brain stimulation with wearable sensors in an essential tremor patient. J. Neurosurg. 2017, 127, 580–587. [CrossRef]

43. Parastarfeizabadi, M.; Kouzani, A.Z. Advances in closed-loop deep brain stimulation devices. J. Neuroeng. Rehabil. 2017, 14, 79. [CrossRef]

44. Ballo, A.; Pennisi, S.; Scotti, G. 0.5 V CMOS Inverter-Based Transconductance Amplifier with Quiescent Current Control. J. Low Power Electron. Appl. 2021, 11, 37. [CrossRef]

45. Ballo, A.; Grasso, A.D.; Pennisi, S. Active load with cross-coupled bulk for high-gain high-CMRR nanometer CMOS differential stages. Int. J. Circuit Theory Appl. 2019, 47, 1700–1704. [CrossRef]

46. Harrison, R.R.; Charles, C. A low-power low-noise cmos for amplifier neural recording applications. IEEE J. Solid-State Circuits 2003, 38, 958–965. [CrossRef]

47. Wattananapitch, W.; Fee, M.; Sarpeeshkar, R. An Energy-Efficient Micropower Neural Recording Amplifier. IEEE Trans. Biomed. Circuits Syst. 2007, 1, 136–147. [CrossRef] [PubMed]

48. Biederman, W.; Yeager, J.R.; Narevsky, N.; Koralek, A.C.; Carmena, J.M.; Alon, E.; Rabaey, J.M. A Fully-Integrated, Miniaturized (0.125 mm²) 10.5 µW Wireless Neural Sensor. IEEE J. Solid-State Circuits 2013, 48, 960–970. [CrossRef]

49. Gosselin, B.; Ayoub, A.E.; Roy, J.-F.; Sawan, M.; Lepore, F.; Chaudhuri, A.; Guitton, D. A Mixed-Signal Multichip Neural Recording Interface with Bandwidth Reduction. IEEE Trans. Biomed. Circuits Syst. 2009, 3, 129–141. [CrossRef] [PubMed]

50. Zhang, F.; Holleman, J.; Otis, B.P. Design of Ultra-Low Power Biopotential Amplifier for Biosignal Acquisition Application. IEEE Trans. Biomed. Circuits Syst. 2012, 6, 244–355.

51. Kwak, J.Y.; Park, S.-Y. Compact Continuous Time Common-Mode Feedback Circuit for Low-Power, Area-Constrained Neural Recording Amplifiers. Electronics 2021, 10, 145. [CrossRef]

52. Tasneem, N.T.; Mahbub, I. A 2.53 NF 8-bit 10 kS/s 0.5 µm CMOS Neural Recording Read-Out Circuit with High Linearity for Neuromodulation Implants. Electronics 2021, 10, 590. [CrossRef]

53. Kim, H.-J.; Park, Y.; Eom, K.; Park, S.-Y. An Area- and Energy-Efficient 16-Channel, AC-Coupled Neural Recording Analog Frontend for High-Density Multichannel Neural Recordings. Electronics 2021, 10, 1972. [CrossRef]

54. Ke, M.-D. ESD implantations for on-chip ESD protection with layout consideration in 0.18-µm salicided CMOS technology. IEEE Trans. Semicond. Manuf. 2005, 18, 328–337. [CrossRef]

55. Baker, R.J. CMOS, Circuit Design, Layout, and Simulation, 3rd ed.; Wiley-IEEE Press: Hoboken, NJ, USA, 2010.
56. Sharma, A.K.; Madhusudan, M.; Burns, S.M.; Mukherjee, P.; Yaldiz, S.; Harjani, R.; Sapatnekar, S.S. Common-Centroid Layouts for Analog Circuits: Advantages and Limitations. In Proceedings of the 2021 Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, 1–5 February 2021; pp. 124–1229.

57. Steyaert, M.S.; Sansen, W.M. A micropower low-noise monolithic instrumentation amplifier for medical purposes. *IEEE J. Solid-State Circuits* 1987, 22, 1163–1168. [CrossRef]