TOPICAL REVIEW

Sidewall GaAs tunnel junctions fabricated using molecular layer epitaxy

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Abstract

In this article we review the fundamental properties and applications of sidewall GaAs tunnel junctions. Heavily impurity-doped GaAs epitaxial layers were prepared using molecular layer epitaxy (MLE), in which intermittent injections of precursors in ultrahigh vacuum were applied, and sidewall tunnel junctions were fabricated using a combination of device mesa wet etching of the GaAs MLE layer and low-temperature area-selective regrowth. The fabricated tunnel junctions on the GaAs sidewall with normal mesa orientation showed a record peak current density of 35 000 A cm−2. They can potentially be used as terahertz devices such as a tunnel injection transit time effect diode or an ideal static induction transistor.

Keywords: molecular layer epitaxy of gallium arsenide, impurity doping, sidewall tunnel junction, thin film, deep level, quantum-confined tunnelling, terahertz devices

1. Introduction

A tunnel junction (Esaki tunnel diode) consists of joined, heavily doped p- and n-type semiconductor layers. The doping results in a depletion layer with a width of the order of 10 nm or less. Owing to quantum tunnelling through this layer, a negative differential resistance (NDR) region appears in the current–voltage characteristic of the diode.

The first semiconductor tunnel junction was realized by Esaki using germanium [1]. Later, tunnel junctions have been fabricated using Si [2, 3], Si/SiGe [4, 5], GaAs [6–15], InAs/Si [16], GaInAs/GaInNAs [17], InP/InGaAs [18], GaAsSb/InGaAs [19] and InAsP/GaAsP [20]. These tunnel junctions found numerous applications. For example, a tunnel junction can reduce the resistance of a semiconductor laser [21, 22]. Photovoltaic conversion efficiencies of up to 40% have been demonstrated by solar cells containing tunnel junctions of III–V semiconductors [23, 24]. Structures such as a spin-injection light-emitting diode [25] and a tunnel-injection transit time effect diode (TUNNETT) [26–29] have also been reported. Tunnel junctions have been used in transistor structures, such as tunnel transistors [30], tunnel-source field-effect transistors (FETs) [31], δ-doped tunnel FETs [32], heterojunction bipolar transistors (HBTs) with a degenerately doped emitter [33], and ideal static-induction transistors (ideal SITs) [34–36].

Recently, terahertz (THz) devices have attracted significant attention. Their (0.1–10) × 1012 Hz frequency range is suitable for a wide variety of applications, such as wireless communications, spectroscopy, biomedical and molecular imaging and high-speed signal processing. Consequently, Gunn diodes [37, 38], resonant tunnelling diodes [39, 40], quantum cascade lasers [41, 42] and emitters based on transistors [43, 44] have been investigated for use in THz oscillators, and a high electron mobility transistor [45–47], an HBT [48, 49] operated at several hundred GHz and a metal–insulator–metal THz detector [50, 51] have been developed.

In the case of a semiconductor device employing an Esaki tunnel junction, device performance is determined by the
quality of the tunnel junctions. Peak current density ($J_p$) is one of the most important factors that contribute to the output power of the device. An increase in $J_p$ effectively improves the output signal. The peak-to-valley current ratio PVCR = $J_p$/$J_v$, where the valley current density $J_v$ corresponds to the excess current, also indicates the quality of the tunnel junction—the larger the PVCR, the higher the quality. The tunnel junction demonstrates the importance of low negative resistance, because the resistance per junction area determines the maximum oscillation frequency. In addition, low zero-bias specific resistivity is required to reduce parasitic Joule heating in the device. In general, these characteristics affect the performance of semiconductor devices, including tunnel junctions. A high-quality tunnel junction should be heavily doped (a higher degeneracy level) in the $p$- and $n$-type semiconductor layers and have very steep profiles of impurities at the tunnel junction interface.

Here, we show the importance of high concentrations and abrupt profiles of impurities in the TUNNETT device and ideal SIT that we developed. The TUNNETT consists of GaAs $p^+\!n^+\!\!\!^i\!n^+$ multilayers with a $p^+\!n^+$ tunnel junction. Under a reverse bias, electrons are injected through tunnelling from the $p^+$ anode to the $i$ drift layer. The oscillation frequency and power are determined by the thickness of the $i$ layer and the tunnelling current density (i.e. doping concentration), respectively. We reported that the TUNNETT can work in the continuous-wave mode with fundamental oscillation frequencies from 60 to 700 GHz [28]. Importantly, the $n^+$ layer at the $p^+\!n^+$ tunnel junction must become a complete depletion layer that requires abrupt impurity profiles. The ideal SIT is also based on GaAs $n^+\!p^+\!n^+$ multilayers with a potential barrier induced electrostatically between the $n^+$ source and the $n^+$ drain. The barrier height formed by the completely depleted $p^+$ layer is controlled by the applied voltages of the gate and the drain, which indicates the tunnelling and ballistic transport without carrier scattering in the channel. Our group reported a tunnelling and ballistic operation with an estimated electron transit time shorter than $10^{-13}$ s, which is suitable for THz operation [35]. Both heavy doping and a very steep concentration profile are required for high barrier and short channel in this device.

We used molecular layer epitaxy (MLE) as a method of GaAs growth to fabricate the GaAs TUNNETT and GaAs ideal SIT. Nishizawa et al achieved the growth of a monomolecular GaAs epitaxial layer by applying intermittent injection of arsine (AsH$_3$) and trimethylgallium (TMG) precursors in an ultrahigh vacuum [52, 53]. In this method, the GaAs layer is epitaxially grown into a monomolecular unit by molecular reactions on the surface, which is why it is called MLE. The MLE was inspired by the Suntola’s idea of an atomic layer epitaxy for II–VI compound semiconductor polycrystals [54, 55], which provides a self-limiting mechanism and has been widely used for growth with an atomic-level thickness [56–58]. Similar self-limiting GaAs growth methods have been reported that use a combination of a carrier gas and a special technique, such as a rotating susceptor [59], a dual growth chamber [60], laser irradiation [61], a short-residence-time reactor vessel [62], a pulse jet [63] or an atmospheric pressure reactor [64].

Numerous GaAs $p^+n^+$ tunnel junctions have been reported, as shown in table 1. They had the $J_p$ values of only 10–1000 A cm$^{-2}$ or less for the tunnel junctions fabricated by molecular beam epitaxy (MBE) [6, 7, 10, 13], metal–organic vapour phase epitaxy (MOVPE) [8, 9] and metal–organic chemical vapour deposition (MOCVD) [14, 15]. We have achieved the fabrication of a sidewall GaAs tunnel junction with a record $J_p$ of 35 000 A cm$^{-2}$ [11, 12]. The advantages of MLE growth which contribute to a high $J_p$ include low temperature and the possibilities of heavy doping and control of the film thickness with atomic accuracy.

In this paper, we review the fabrication of sidewall GaAs tunnel junctions by MLE.

2. Sidewall GaAs tunnel junctions fabricated by area-selective regrowth with molecular layer epitaxy

The sidewall GaAs tunnel junction [11, 65] consists of an $n^+$- and $p^+$-GaAs epitaxial layer with a metal pad on a (001)-oriented semi-insulating GaAs substrate, as shown in figure 1(a). The junction has a 100 µm width, 50 nm depth and $6 \times 10^{-5}$ cm$^2$ area. The area can be easily lowered down to $10^{-8}$ cm$^2$, and the wide metal contact pad on the semiconductor surface can reduce the parasitic resistance. Figure 1(b) shows a cross-sectional image of the fabricated sidewall tunnel junction observed by scanning electron microscopy.

Sidewall tunnel junctions were fabricated by MLE as outlined in figure 2. Initially, a tellurium and sulphur co-doped $n^+$-GaAs layer was grown at 360°C. This epitaxial layer had a thickness of 50 nm and electron concentration of $2 \times 10^{19}$ cm$^{-3}$. Arsine and triethylgallium (TEG) were used as precursors for the epitaxial growth of GaAs, and diethyltelluride (DETe) and diethylsulphur (DES) were used for donor doping. AsH$_3$, TEG, DETe and DES were introduced separately into ultrahigh vacuum. To achieve a high impurity concentration, DETe was exposed on the gallium-stabilized surface (AG mode), and DES was introduced on the arsenic-stabilized surface (AA mode) during the MLE growth cycles [66]. Following the initial procedure, a silicon nitride (SiN$_x$) layer was deposited by remote-plasma CVD at 275°C, and SiN$_x$ windows were opened using conventional photolithography and reactive-ion etching (RIE), followed by the final slight wet etching of the remaining thin SiN$_x$. Through these windows, the GaAs sidewall mesa was formed to a depth of 60 or 120 nm using a H$_2$SO$_4$-based solution. To obtain a high-quality junction interface, an AsH$_3$ surface treatment [12, 67] was performed in the growth chamber right before the epitaxial regrowth. In this process, the SiN$_x$-patterned GaAs substrate was heated to 350°C for 30 min under an AsH$_3$ pressure of $8 \times 10^{-2}$ Pa.

After the AsH$_3$ surface treatment, area-selective epitaxial regrowth of a beryllium-doped $p^+$-GaAs layer was carried out at $\sim$290°C using bismethylicyclopentadienyl-beryllium [Be(MeCp)$_2$], Be(MeCp)$_2$ was introduced by the AG mode of MLE doping to achieve a high hole concentration of
Table 1. Comparison of GaAs tunnel junctions operated at room temperature.

| Growth method | p-type dopant | n-type dopant | $J_p$ (A cm$^{-2}$) | $V_p$ (V) | PVCR resistance (kΩ μm$^2$) | Negative specific resistivity (Ω cm$^2$) | Note | Reference |
|---------------|---------------|---------------|---------------------|---------|-----------------------------|----------------------------------------|-------|-----------|
| MBE           | C             | Si            | 400                 | –       | –                           | –                                      | –     | [6]       |
| MBE           | Be            | Si            | 1824                | 0.19    | 28.2                        | 25.1                                  | 7.8 × 10$^{-5}$                  | Containing excess arsenic | [7] |
| MOVPE         | C             | Si            | 17                  | 0.08    | 17                          | –                                     | –     | [8]       |
| MOVPE         | C             | Si            | 57                  | 0.1     | 23                          | –                                     | –     | [9]       |
| MBE           | Mn            | –             | 28                  | 0.25    | ~1                          | –                                     | –     | Magnetic semiconductor | [10] |
| MOVPE         | Be            | Te&S          | 31 000              | 0.21    | 2.1                         | 1.2                                   | 5.3 × 10$^{-6}$                  | Sidewall structure | [11] |
| MOCVD         | Be            | Te&S          | 35 000              | 0.25    | 3.2                         | –                                     | –     | Longer AsH$_3$ treatment | [12] |
| MBE           | Be            | Te&S          | 23 500              | 0.57    | 1.7                         | 0.09                                  | 2.2 × 10$^{-5}$                  | Z-type negative resistance | [12] |
| MBE           | Be            | Si            | 16 000              | 3.4     | 22                          | 0.226                                 | 1 × 10$^{-3}$                    | pin structure | [13] |
| MOCVD         | C             | Si            | 500                 | 0.17    | 4.5                         | 92                                    | 9.6 × 10$^{-5}$                  | Autocompensated impurities | [14] |
| MOCVD         | C             | Si            | 1530                | 0.63    | 6.9                         | 2.7                                   | 4.1 × 10$^{-4}$                  | –         | [15] |

Figure 1. (a) Schematic of the cross-sectional and top views of the fabricated sidewall GaAs tunnel junctions. The Ti/Au nonalloyed metal contact pad is 100 μm in length. In the top view, the arrows indicate the positions of the sidewall tunnel junctions, and ‘F’ and ‘R’ denote the first epitaxial layer and the regrowth layer, respectively. (b) Cross-sectional views of the sidewall GaAs tunnel junctions in the normal mesa orientation observed by scanning electron microscopy. (Reproduced with permission from [11] ©2002 AIP and [12] ©2004 ECS.)
3. Impurity doping characteristics in the molecular layer epitaxy of GaAs

3.1. Be doping characteristics for the p*-GaAs layer

A high concentration of impurities and abrupt profiles at the tunnel junction interface are the most important factors for achieving a high-quality tunnel junction. For acceptor doping, as widely reported in the field of MBE of GaAs [72–75], Be is a good candidate for heavy p-doping and for steep impurity profiles because of its low diffusion coefficient [76]. The covalent radius of Be is similar to the radii of Ga and As, and the lattice strain in Be-doped GaAs was expected to be small. Consequently, the Be-doped GaAs epitaxial layer was used for the sidewall GaAs tunnel junctions.

To investigate the doping characteristics, a Be-doped GaAs epitaxial layer on the GaAs substrate was grown by intermittent injection of AsH₃, TEG and Be(MeCp)$_2$ in ultrahigh vacuum [68]. The substrate was heated by an infrared (IR) lamp, and the temperatures were controlled by an IR pyrometer. Arsine and TEG were chosen as precursors for the epitaxial growth of GaAs, and Be(MeCp)$_2$ was the source gas for acceptor doping. As substrates, we used undoped semi-insulating (100), (111)A, (111)B and (110) GaAs wafers prepared by the liquid encapsulated Czochralski method.

Figure 2 shows the relationship between the Hall mobility and the hole concentration in Be-doped p*-GaAs grown on a (100) GaAs substrate and obtained from Hall-effect measurements using the van der Pauw method. Our MLE data fit well into the Hilsum’s formula [77], as well as the results reported by other groups for Be-doped GaAs grown by MBE at 600 [78], 530 [79] and 270 °C [80]. The Hall mobility of the MLE layer is nearly equal to that of the MBE-grown layer, even at a very low growth temperature (~290°C). We performed x-ray multicrystal diffractometry (XRD) analysis using the g = 004 diffraction plane with a prefixed Ge (220) asymmetric-configuration.
Table 2. Sidewall GaAs tunnel junction characteristics at room temperature.

| Sidewall mesa orientation | \( J_p \) (A cm\(^{-2} \)) | \( J_v \) (A cm\(^{-2} \)) | \( V_p \) (V) | PVCR | Negative resistance (k\( \Omega \mu \text{m}^2 \)) | Zero-bias specific resistivity (\( \Omega \text{cm}^2 \)) |
|-------------------------|------------------|------------------|--------|-------|-------------------|-------------------|
| Normal mesa             | 31 000           | 14 900           | 0.214  | 2.1   | 1.2               | 5.3 \( \times 10^{-6} \) |
| 45°-inclined configuration | 5200            | 3110             | 0.130  | 1.7   | 7.3               | 1.0 \( \times 10^{-5} \) |
| Reverse mesa            | 2100             | 1530             | 0.136  | 1.4   | 20                | 2.9 \( \times 10^{-5} \) |

Figure 3. \( J-V \) characteristics of sidewall GaAs tunnel junctions at room temperature (RT) in the (a) normal mesa, (b) 45°-inclined and (c) reverse mesa sidewall orientations. (Reproduced with permission from [65] ©2004 Elsevier.)

Figure 4. SIMS profiles for the \( p^+n^+ \) plane GaAs tunnel junction fabricated on a {001} surface by the identical regrowth conditions as the sidewall tunnel junction.

monochromator. Be-doped GaAs layers with concentrations up to \( 10^{20} \text{cm}^{-3} \) exhibited no double peaks in their XRD rocking curve implying that Be doping induced insignificant lattice strain in GaAs. These results indicate that the Be-doped \( p^+ \)-GaAs MLE layers grown at low temperatures have a high carrier concentration and good crystal quality even at heavy doping.

Figure 6 shows the SIMS depth profile of Be in a Be-doped GaAs multilayer grown on a (100) GaAs substrate at 290°C. The sample consists of a stack of undoped GaAs, Be-doped GaAs grown in AG mode, undoped GaAs, Be-doped GaAs grown in an AA mode, undoped GaAs and GaAs substrate. Here, the AA mode means that the Be(\( \text{MeCp} \)\(_2 \)) gas was introduced after the GaAs surface had been As-terminated by exposure to \( \text{AsH}_3 \), followed by evacuation. In contrast, the AG mode indicates that the impurity gas was introduced after exposure to TEG. As previously mentioned, the surface stoichiometry can be controlled by changing the timing of the introduction of the Be
dopant. In this sample, although two Be-doping layers were grown by changing only the doping mode, the incorporation of Be was enhanced when a Ga-stabilized surface was exposed to Be(MeCp)$_2$, i.e. the AG mode. A substrate-orientation dependence of Be doping in GaAs MLE was also apparent, as shown in figure 7 [81].

To achieve heavy doping of Be in GaAs, the surface stoichiometry prior to the introduction of the Be dopant gas was controlled by changing the AsH$_3$ and TEG supply times. As shown in figure 8(a), the Be concentration in AA mode decreased with increasing AsH$_3$ injection time. However, the concentration of Be was enhanced by increasing the AsH$_3$ injection time in AG mode. In the case of the TEG supply, incorporation of Be was enhanced with decreasing TEG exposure duration in AA and AG modes. It is possible to estimate the effects of surface stoichiometry on the surface reaction using rate-law considerations. The rate law for Be incorporation can be expressed as

\[ \frac{d[\text{Be}]}{dt} = k[\text{Be}(\text{MeCp})_2]^\alpha [\text{AsH}_3]^\beta [\text{TEG}]^\gamma, \]

where \( r \) is the chemical reaction rate, \([\text{Be}]\) is the Be concentration, \( t \) is the source-gas supply time, \( k \) is the rate constant, and \( \alpha, \beta \) and \( \gamma \) are the orders of the reaction. Figure 8(b) shows the AsH$_3$ supply dependences of the reaction rate for Be incorporation for the two doping modes. The order of reaction for the AsH$_3$ supply (1.3 for AA mode and 0.7 for AG mode) is smaller than that for the TEG supply (1.4 for AA mode and 1.9 for AG mode). From the theorem of monomolecular reactions [82] and unimolecular collision [83], Be(MeCp)$_2$ is less activated by the TEG supply, and thus, the order of reaction by the TEG supply tends to be 2. On the contrary, Be(MeCp)$_2$ is activated more by the AsH$_3$ supply, and thus, the order of reaction by AsH$_3$ supply tends to be 1. These results, which depend on the surface stoichiometry, are useful for obtaining high doping concentrations.

### 3.2. Alternate Te and S doping characteristics for \( n^+\)-GaAs layer

Te and S can be used as \( n \)-type dopants of GaAs. The diffusion coefficient of Te is one of the smallest among the \( n \)-type dopant impurities. Thus, Te atoms hardly diffuse during growth, and a very steep impurity profile was expected. However, a differential strain was observed in the homoepitaxial layers doped with \( 10^{19} \text{–} 10^{20} \text{ cm}^{-3} \) of Te [84]. On the contrary, differential strain was low in the heavily S-doped GaAs epitaxial layer, although the covalent radius of S is smaller than the radii of Ga and As. Sulphur is more suitable for obtaining a steep impurity profile than Se or Si.

In accordance with the previously discussed results, Te and S co-doping were expected to reduce the lattice strain, which would then enhance the incorporation of impurities because of the strain compensation. Thus, to investigate the Te and S co-doping, MLE growth on a GaAs (100) substrate was performed using AsH$_3$, TEG, DETe and DES. Previously, co-doping was studied for InGaAs:Zn and C [85], GaAs:Yb and Al [86], ZnTe:Al and N [87], ZnCrTe:I and N [88], ZnO:Al and N [89], SnO$_2$:Co and Al [90] and ZnO:Mn and N [91].
The concentration of Te increased monotonically with increasing S coverage, whereas DETe was supplied to a GaAs surface covered with S in AA mode, as shown in figure 9(a) [66]. In contrast, the S concentration decreased monotonically with increasing concentration of Te when DETe was introduced before DES was supplied in AA mode, as shown in figure 9(b). The effect of the underlying S layer on the enhanced incorporation of Te can be explained by the large electronegativity of S with respect to Te and As and its relationship with the charge distribution in DES and DETe molecules near the surface. Conversely, the effect of the underlying Te layer on the reduced incorporation of S can be explained by the small electronegativity of Te relative to that of S.

Table 3 summarizes the electrical and crystallographic characteristics of Te and S co-doped GaAs MLE layers that were investigated by Hall-effect measurements and XRD analyses. All samples were grown at the same GaAs substrate temperature of 360 °C and had an electron density of \( \sim 1.7 \times 10^{19} \text{cm}^{-3} \); this specific value is close to the effective density of electron states in degenerate GaAs. When Te-doped and alternate Te and S co-doped layers were compared, the differential strains (\( \Delta a/a \)) were almost the same at 3.1–3.6 \( \times 10^{-3} \); however, the full-width at half-maximum (FWHM) was smaller for the co-doped layer (137 arcsec). This result means that the crystal quality was improved by co-doping with Te and S, presumably because of strain compensation in the crystal structure.

4. Defect aspects in sidewall GaAs tunnel junctions

4.1. Defects at the sidewall GaAs tunnel junction interface

The identification and control of defects in semiconductors is one of the most important research fields because defects determine the electrical and optical characteristics of semiconductors and crucially affect the material quality and device performance. To reveal deep levels related to the tunnel junction interface of the sidewall GaAs tunnel junctions, a photocapacitance measurement was applied to the sidewall \( p^+ n^+ \) junctions, and the emission spectra caused by deep levels at the junction interface were obtained.

The measurement of photocapacitance allows evaluating deep levels in semiconductors and oxides. Details of the photocapacitance equipment and the measurement system are described elsewhere [92, 93]. The defects in the depletion layer are ionized by monochromatic light at low temperature, and the ionized-level density is then determined from the change in the depletion-layer capacitance. This measurement provides a more precise determination of level density...
Table 3. Room-temperature electrical and crystallographic characteristics of S-doped, Te-doped and Te and S co-doped GaAs grown by MLE.

| Dopant | Thickness (nm) | Concentration of S (cm⁻³) | Concentration of Te (cm⁻³) | n (cm⁻³) | Δα/a | FWHM (arcsec) |
|--------|----------------|---------------------------|---------------------------|----------|------|---------------|
| S      | 77             | 4.5 × 10⁹                 | –                         | 1.6 × 10¹⁰| –    | –             |
| Te     | 110            | –                         | 4.2 × 10⁹                 | 1.7 × 10⁹| 3.1 × 10⁻³| 165           |
| Te&S   | 118            | 2.3 × 10⁹                 | 4.5 × 10⁹                 | 1.6 × 10¹⁰| 3.6 × 10⁻³| 137           |

Figure 10. (a) Photocapacitance emission spectra at 6.6 K of sidewall GaAs p⁺n⁺ junctions as a function of sidewall mesa orientation. ΔC/C is the normalized change in junction capacitance, which is proportional to the deep-level density. (b) Simple flat-band energy diagram that corresponds to the observed optical transitions. (Reproduced with permission from [96] ©2006 Wiley-VCH.)

4.2. AsH₃ surface treatment for the improvement of sidewall GaAs tunnel junction characteristics

Semiconductor devices operated by tunnelling and ballistic conduction mechanisms require especially high-quality tunnel junctions in which defect states at the junction interface are well controlled. To obtain a high-quality junction, the effects of the AsH₃ surface treatment just prior to regrowth are shown for the improvement of PVCR. Figure 11 shows the PVCR as a function of AsH₃ surface treatment time (tₐ). The PVCR increases monotonically from 1.6 to 4.2, when tₐ became longer [12]. This increase occurred because of the reduction in the deep-level density at the junction interface. In addition, the ratio of Jᵥ(300 K)/Jᵥ(77 K) was almost constant for tₐ of 30 and 60 min, but an AsH₃ surface treatment for 120 min reduced that value. We conclude that a sufficient AsH₃ surface treatment with long tₐ induces shallower deep levels, which will be followed by a less-strained atomic configuration around the defects. The control of surface stoichiometry by AsH₃ surface treatment has been reported to reduce the nonstoichiometry-related defects at the regrown interface [67]. Thus, the AsH₃ surface treatment reduces the density of deep levels at the sidewall tunnel junction interface, and the Jᵥ decreases, while the PVCR increases for longer tₐ.

It is also shown that the longer AsH₃ surface treatment enhances the steepness of the Be profile and that the Be pile-up at the interface increases as the tₐ becomes longer.
shows the minimum sub-band separation
5. Tunnelling mechanism in sidewall GaAs tunnel junctions
5.1. Low-temperature current–voltage and conductance–voltage measurements of sidewall GaAs tunnel junctions
Figure 12(a) shows the current–voltage (I–V) characteristics of the sidewall GaAs tunnel junctions fabricated on the normal mesa sidewall as a function of temperature [97]. The temperature dependence of the V$_{S1}$ near the peak voltage was not observed, where V$_S$ is a voltage position of the sharp step (current step) in the NDR region. The tunnel current flowing around the V$_{S1}$ is expected to correspond to direct tunnelling. The values of V$_{S1}$ near the valley voltage exhibited a temperature dependence ranging from 0.35 to 0.5 V and indicate indirect tunnelling. The PVCR value on the normal mesa was 4.7 at 15 K.

The sidewall GaAs tunnel junctions were evaluated by conductance–voltage measurements (G–V) at 6 K and at room temperature, as shown in figure 12(b) [97]. In the differential G–V curve, the peaks at 9, 49 and 60 mV can be clearly observed only at 6 K, which corresponds to indirect tunnelling of the phonon emission type. Considering the phonon spectrum, the peaks above 37 mV can be assigned to multiphonon-assisted tunnelling. However, it is not clear whether the 9-mV peak originates from phonon-assisted tunnelling because this peak (close to 0 V) might be caused by a zero-bias anomaly [98–101]. If the peak at 9 mV does not relate to a zero-bias anomaly, the peak at 7 mV might represent a transverse-acoustic L phonon (TA(L)), and the peak at 18 mV might be attributed to tunnelling assisted by the two-phonon combination TA(L) + TA(X) (inset in figure 12(b)).

5.2. Fine structures in quantum-confined sidewall GaAs tunnel junctions
To investigate the characteristics of sidewall GaAs tunnel junctions with narrower junction depths, both $p^+$ and $n^+$-GaAs of MLE layers were thinned using a H$_2$SO$_4$-based etchant with the Ti/Au metal contact pad used as a mask. The achieved junction depths (d) of the sidewall tunnel junctions were d = 30, 20, 15 and 5 nm.

The number and voltage positions of sharp steps in the NDR region change with the junction depth [102, 103]. Three V$_S$ are observed when the junction depth is d = 50 nm, as shown in figure 12(a). The V$_{S2}$ was generated on the high-voltage side of V$_{S1}$. The voltage difference between the peak and V$_{S1}$ (= V$_{S1}$–V$_{p}$) is 8 mV at 15 K. The voltage difference between V$_{S1}$ and V$_{S2}$ (= V$_{S2}$–V$_{S1}$) is also 8 mV. Three sharp steps are observed when the junction depth is d = 30 nm, but the voltage difference between them is different, as shown in figure 13: V$_{S1}$–V$_{p}$ = 30 mV and V$_{S2}$–V$_{S1}$ = 25 mV. The number of sharp steps increased to four when the junction depth was reduced to d = 20 nm, and the V$_{S1}$–V$_{p}$ and V$_{S2}$–V$_{S1}$ are 54 mV and 45 mV, respectively. At a junction depth of d = 15 nm, only two sharp steps appeared in the temperature range 15–300 K. The voltage differences of the sharp steps were 100 mV for V$_{S1}$–V$_{p}$ and 88 mV for V$_{S2}$–V$_{S1}$. No sharp steps appeared over the entire temperature range when the junction depth was d = 5 nm.

If the GaAs layer was quantum-confined in two dimensions (2D), the change in the I–V curve appeared because of the sub-band formation in the n$^+$-GaAs conduction band. Figure 14 shows the minimum sub-band separation energy [104–107] when a 2D quantum well structure is assumed. The energy differences in the positions of sharp steps (V$_{S1}$–V$_{p}$ and V$_{S2}$–V$_{S1}$) are also plotted and fit well with the sub-band separation energy. Thus, 2D–2D tunnelling was observed with sidewall tunnel junctions of d = 50, 30 and 15 nm. However, sub-band formation at the junction depth d = 5 nm was not confirmed because of the surface depletion of the 5 nm n$^+$-GaAs layer.

Although sharp steps were observed in the I–V curves, these steps may have appeared because of oscillations in the external measurement circuit of sidewall tunnel junctions. If voltage is applied to the tunnel junction at an unstable point in the NDR region, oscillations normally occur [108]. However, because the measured differences in the positions of sharp steps correspond well with the calculated sub-band separation energy, the appearance of V$_{S2}$ and the positioning of V$_{S1}$ may be attributed to the sub-band quantisation.

6. Application of sidewall GaAs tunnel junctions for THz devices
6.1. Sidewall GaAs n$^+$p$^+$n$^+$ and p$^+$n$^+$in$^+$ structures
THz devices, such as an ideal SIT, require a high and narrow potential barrier related to a high tunnelling probability.
Figure 12. (a) Temperature dependence of the $I-V$ characteristics of a sidewall GaAs tunnel junction. The measurement temperature was varied from 15 to 300 K with a step of 5 K. (b) The differential $G-V$ characteristics of the sidewall GaAs tunnel junction at 6 K and room temperature. The inset shows deconvolution of the 9 meV peak at 6 K. (Reproduced with permission from [97] ©2008 Wiley-VCH.)

Figure 13. Temperature dependences of the $I-V$ characteristics of the sidewall GaAs tunnel junctions with the indicated junction depths $d$. (Reproduced with permission from [102] ©2006 Wiley-VCH and [103] ©2007 Elsevier.)

of the carriers. Planar-doped barrier structures such as $n-i-p-i-n$ GaAs [109–112], $n-p-n$ Si/SiGe/Si [113] and $n-p-n$ InP/InGaAsP/InGaAs [114] have been reported. The $I-V$ characteristics of a vertical-type GaAs planar-doped barrier structure grown by MLE have been also investigated [115, 116], as well as the tunnelling characteristics of sidewall GaAs $n^+p^+n^+$ and $p^+n^+i^+n^+$ structures formed by MLE [117]. To fabricate the sidewall $n^+p^+n^+$ structure, area-selective MLE of Be-doped $p^+$-GaAs was performed at 290 °C on a normal mesa sidewall. The thickness of the regrown $p^+$-GaAs layer, which forms a potential barrier, was determined by the number of dopant gas injection cycles ($N$). Although the actual doping profile on the sidewall surface cannot be obtained by SIMS measurements, its thickness is proportional
to \( N \) in the MLE growth. Accordingly, a Te and S co-doped \( n^- \)GaAs layer was regrown at 360 °C. The sidewall \( p^+ n^- \) structure was also fabricated by a similar device process, and the thickness of the first regrown \( n^- \)GaAs layer was controlled by varying \( N \).

As shown in figure 15, the current density flowing between ‘F’ and ‘R’ in the sidewall GaAs \( n^- p^+ n^- \) structure decreased with increasing thickness of the \( p^+ \)-GaAs layer, except for \( N = 240 \). The tunnelling current was dominant in this structure because of the weak temperature dependence of the \( J-V \) curve. Because no Esaki peak appeared in the \( N = 30, 60 \) and 120 samples, the \( p^+ \)-GaAs layer was expected to be almost depleted. However, an Esaki peak can be seen when the \( p^+ \)-GaAs layer is thick \((N = 240)\) because the thicker \( p^+ \)-GaAs layer was not completely depleted. This result indicates that the remains of the nondepleted layer caused by the thickness of the \( p^+ \)-GaAs layer are the reason for the Esaki peak.

Figure 16 shows the \( J-V \) characteristics of the sidewall GaAs \( p^+ n^- \) structures for the TUNNETT diode at room temperature as a function of the thickness of the regrown \( n^- \)GaAs layer at the sidewall \( p^+ n^- \) tunnel junction. When there was no growth on the first regrown \( n^- \)GaAs layer, i.e. \( N = 0 \), the reverse breakdown voltage was very high because of the sidewall \( p^+ n^- \) structure, which had an \( i \)-GaAs layer 50 nm in length. An Esaki peak was also confirmed when the \( n^- \)-GaAs layer became thicker \((N = 28)\) (inset in figure 16(a)). However, when the \( n^- \)-GaAs layer was regrown by \( N = 15 \), which corresponds to approximately 4 nm on the \{001\} surface, the reverse current increased without the threshold voltage, and no Esaki peak appeared. This shape of the \( J-V \) curve is similar to that of a vertical-type TUNNETT. Moreover, the achievement of a high current density greater than \(-1 \times 10^{7} A \cdot cm^{-2}\) is important to oscillation with high output power. Therefore, among the results of \( J-V \) characteristics in this measurement, the \( N = 15 \) sample is important for the oscillation of a TUNNETT because it is necessary to achieve a completely depleted \( n^- \)-GaAs layer to focus the electric field at the depletion layer.

6.2. GaAsSb quantum well and GaSb dot growth for THz devices

Higher tunnelling probability corresponds to the higher output power of the TUNNETT oscillator. From the tunnelling probability calculated by the Wentzel–Kramers–Brillouin approximation, a material with a narrow bandgap and a small effective mass can have a high tunnelling probability. Therefore, the growth of an antimony-containing compound semiconductor, such as GaAsSb or GaSb, from some suitable material candidates was performed by the MLE method because this type of semiconductor has almost the same lattice constant as a GaAs substrate. GaAsSb and GaSb growth are also used for manufacturing photoconductive THz emitters [118–120], THz laser [121] and double HBT structure [122].

GaAsSb/GaAs quantum wells have attracted attention for their potential applications in electronic and optoelectronic devices, and these structures have been fabricated and evaluated in several reports [123–131]. In addition, an undoped GaAsSb quantum well was grown by MLE on undoped semi-insulating (100), (111)A, (111)B and (110) GaAs substrates using trimethylantimonide [132]. Figure 17 shows the SIMS results for the GaAs/GaAsSb/GaSb single quantum well structure grown on a (100) GaAs substrate at 360°C. The Sb composition that was obtained from the fitted XRD data was GaSb\(_{0.79}\)Sb\(_{0.21}\) with a thickness.
of 11 nm. The gradient of the Sb concentration was $1 \times 10^{21} \text{cm}^{-3} \text{nm}^{-1}$, which means an approximately 10% per nm increase in Sb composition. The maximum Sb yield was achieved on the (100) substrate, and the Sb yield ratio for other orientations was (100):(111)A:(111)B:(110) = 1:0.1:0.4:0.1. Photoluminescence (PL) spectra were recorded at 77 K from the GaAs/GaAsSb/GaAs quantum well structure, and the FWHM was large (100–200 meV) for all substrates. For the (111)A and (110) substrates, a blue shift appeared when the excitation power of the light source was increased, as shown in figure 18. The phenomenon of blue shifting, which is caused by band bending (band modulation) induced by carrier accumulation, is well known for the type-II band structure of GaAsSb/GaAs quantum wells. The GaAsSb single quantum wells grown by MLE on the (111)A and (110) substrates exhibit type-II band alignment, and a very abrupt heterostructure was expected.

GaSb quantum dots [133–138] and rings [139, 140] formed on GaAs or embedded in a GaAs matrix have been reported, and the MLE growth and optical properties of GaSb dots have been investigated [132]. Figure 19 shows atomic force microscope (AFM) images of GaSb dots for different substrate orientations. The minimum average dot diameter (20 nm) and the highest dot density ($7 \times 10^{10} \text{cm}^{-2}$) were achieved on (111)A GaAs. The dots were smaller and more abundant on (100) and (111)A than (111)B and (110) substrates. A PL peak at 1.0 eV appeared for the GaAs/GaSb dot/GaAs structure at 77 K in all four orientations. This peak position is close to that for the dislocation-induced quantum
6.3. Sidewall GaAs tunnel junction with TiO$_x$ gate structure

Although Si metal–oxide–semiconductor (MOS) transistors are widely used, the GaAs MOS transistor has attracted substantial interest recently. Devices based on III–V compound semiconductors possess great advantages over Si-based devices for high-speed and high-power applications. To improve the transconductance of a GaAs transistor, high-permittivity (high-$k$) gate dielectric materials are required for fabrication. Several types of oxide films are being considered for a GaAs MOS transistor, such as Al$_2$O$_3$ formed by atomic layer deposition (ALD) [143], HfO$_2$ by ALD [144], HfO$_2$ by plasma oxidation [145], Y$_2$O$_3$ by MBE [146], ZrO$_2$ by RF sputtering [147] and Y$_2$O$_3$ by RF sputtering [148]. In addition, titanium oxide (TiO$_x$) MOS diodes were fabricated by sputtering [149], liquid-phase deposition [150] and sol–gel methods [151].

The operation of an ideal SIT has been realized, both with GaAs homojunction and AlGaAs heterojunction gate structures, and transistor operation at room temperature with ballistic electron transport has been achieved [35]. One of the most promising structures for an ideal SIT incorporates a high-$k$ dielectric gate. Recently, electrical and structural evaluations have been performed on TiO$_x$ dielectrics that had been deposited on a (100) GaAs substrate at 100°C by electron-beam evaporation of a TiO$_2$ source in a mixed oxygen/argon atmosphere [152].

From the capacitance–voltage ($C–V$) results of GaAs MOS diodes with TiO$_x$ dielectrics at room temperature under the accumulation conditions, the highest permittivity was close to 100. This permittivity is adequate in view of the film composition because the permittivity of TiO$_2$ anatase is approximately 130, and the permittivity of Ti$_2$O$_3$ would exhibit a lower value. Based on the results of XRD with a grazing incidence angle, the deposited TiO$_x$ film contains a small crystalline phase of TiO$_2$ and Ti$_2$O in the dominant TiO$_x$ amorphous matrix phase.

The bandgap of deposited TiO$_x$ was measured using the photocapacitance method and was 2.82 eV, as shown in figure 20. In addition, the dominant deep donor state is located at 1.14 eV below the conduction band of TiO$_x$. Although the origin of this deep electronic state is not yet clear, this deep level should affect the low breakdown field strength of TiO$_x$ films (0.5 MV cm$^{-1}$), which was obtained by J–V measurement of GaAs MOS diodes with TiO$_x$ dielectrics.

A TiO$_x$ film was applied to sidewall GaAs tunnel junctions as a gate dielectric to realize tunnel transistor operation. A schematic diagram of the TiO$_x$-gated $p^n$+$n^+$ tunnel transistor is presented in figure 21. A 20-nm-thick TiO$_x$-gated $p^n$+$n^+$ tunnel junction can operate as a transistor in both the enhancement and depletion modes at room temperature, as shown in figure 22. Although the transconductance was small ($\sim$5 mS mm$^{-1}$) in the present sample because the deposition and cleaning process had not yet been optimized, an ideal SIT with THz operation will be realized by applying the improved high-$k$TiO$_x$ gate structure to sidewall $n^+p^n$+$n^+$ barrier structures with a 10-nm source/drain spacing.

7. Summary

Sidewall GaAs tunnel junctions fabricated by molecular layer epitaxy were introduced in this review paper. This sidewall tunnel junction with a 50-nm junction depth showed a record peak current density of 35 000 A cm$^{-2}$. To obtain the high crystal quality of $p^+$- and $n^+$-GaAs layers, surface-stoichiometry-controlled Be-doping and Te and S co-doping were performed. The deep levels at the sidewall tunnel junction interface were revealed by photocapacitance measurements, and stoichiometry-related defects were reduced by AsH$_3$ surface treatments. The tunnelling mechanism in sidewall tunnel junctions was investigated in view of phonon-assisted tunnelling and quantum-confined tunnelling. In addition, we overviewed the recent results on the device application and fabrication...
technology for THz devices, such as sidewall planar-doped barrier structures, Sb-related materials and high-κTiO$_2$ MOS structures.

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Figure 22. Room-temperature output characteristics of a 20 nm-thick TiO$_2$-gated $p^+n^+$ tunnel transistor operated in (a) enhancement and (b) depletion mode.
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