Adjusting Thermal Stability in Double-Barrier MTJ for Energy Improvement in Cryogenic STT-MRAMs

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Abstract

This paper investigates the impact of thermal stability relaxation in double-barrier magnetic tunnel junctions (DMTJs) for energy-efficient spin-transfer torque magnetic random access memories (STT-MRAMs) operating at the liquid nitrogen boiling point (77 K). Our study is carried out through a macrospin-based Verilog-A compact model of DMTJ, along with a 65 nm commercial process design kit (PDK) calibrated down to 77 K under silicon measurements. Comprehensive bitcell-level electrical characterization is used to estimate the energy/latency per operation and leakage power at the memory architecture-level. As a main result of our analysis, we show that energy-efficient small-to-large embedded memories can be obtained by significantly relaxing the non-volatility requirement of DMTJ devices at room temperature (i.e., by reducing the cross-section area), while maintaining the typical 10-years retention time at cryogenic temperatures. This makes DMTJ-based STT-MRAM operating at 77 K more energy-efficient than six-transistors static random access memory (6T-SRAM) under both read and write accesses (–56% and –37% on average, respectively). Obtained results thus prove that DMTJ-based STT-MRAM with relaxed retention time is a promising alternative for the realization of reliable and energy-efficient embedded memories operating at cryogenic temperatures.

Keywords: Double-barrier magnetic tunnel junction (DMTJ), STT-MRAM, Cryogenic electronics, Cryogenic cache, Thermal stability relaxation, 77 K

1. Introduction

Spin-transfer torque magnetic RAMs (STT-MRAMs) have been gaining interest for cryogenic computing electronics due to their reduced area footprint, improved readout capabilities, and increased data retention time [1–3]. In this regard, recent studies have focused on STT-MRAM operating down to the liquid nitrogen boiling point (77 K), showing that it is a viable energy-efficient alternative to six-transistor static random access memory (6T-SRAM) for medium-to-large embedded memories under cryogenic operation [3–5]. In view of the above benefits,
STT-MRAMs are identified as potential candidates for future cryogenic computing applications. However, to better support cryogenic computing, energy improved memories with increased storage density are particularly sought after. To deal with this, tuning thermal stability of magnetic tunnel junction (MTJ) devices has been recently considered as a promising approach [3, 6].

In the above context, this work aims to demonstrate a potential solution to build reliable, energy-efficient, and high-density STT-MRAMs operating at cryogenic conditions (77 K). This is achieved by exploiting the reduced switching currents of the double-barrier MTJ (DMTJ) as compared to its conventional single-barrier MTJ (SMTJ) counterpart, along with the concept of relaxing its non-volatility requirement at room temperature (i.e., by reducing its cross-section area), while maintaining the typical 10-years retention time at cryogenic temperatures.

Our study is carried out using a cross-layer simulation framework, which spans from the device-level up to the memory architecture-level, passing through bitcell-level electrical simulations [4–7]. DMTJs and transistors are respectively modeled using a macrospin-based Verilog-A.
compact model [8] and a commercial 65 nm CMOS technology that was fully characterized down to 77 K. Bitcell-level simulations under cryogenic operation benchmark a 13 nm-DMTJ based bitcell with relaxed non-volatility at room temperature and 10-years retention at 77 K against its 40 nm-DMTJ based counterpart providing 10-years retention at 300 K. Our comparative analysis is extended to the architecture-level by considering cache memory sizes ranging from 64 kB up to 2 MB. In our study, we also considered the conventional 6T-SRAM, whose electrical characteristics were extracted from simulations at 77 K. Overall, while cryogenic temperatures enable STT-MRAM improvements in terms of data retention and memory window as given respectively by larger thermal stability and higher tunneling magnetoresistance (TMR) ratio, the 6T-SRAM benefits from significant static power savings. As the main outcome of our work, we show that, over the considered memory capacity range and thanks to the non-volatility of the DMTJ properly tuned for cryogenic operation, the DMTJ-based STT-MRAM operating at 77 K proves to be more energy-efficient than conventional 6T-SRAM under both read and write operations by 56% and 37% (on average), respectively.

This work details from device-level up to architecture-level the benefits of adjusting thermal stability for friendly cryogenic STT-MRAMs. It is worth mentioning that this paper extends the study presented by the authors in [6] by detailing the device-level modeling and analysis for both silicon-calibrated transistor models and DMTJ devices under cryogenic operation, while also describing the fine-grained calibration procedure for cryogenic memory architecture-level simulations. As further difference over [6], reported simulation results account for the effect of the domain-wall in DMTJs, which has been included in the adopted macrospin-based model according to the approach described in [9].

The rest of the paper is organized as follows. Section 2 describes device-level characteristics at cryogenic temperatures. Section 3 discusses bitcell- and architecture-level simulation results of cryogenic DMTJ-based STT-MRAM, while discussing the adopted simulation approach. Finally, Section 4 concludes this work.

2. Device-level modeling and analysis at cryogenic temperatures

2.1. CMOS devices under cryogenic operation

Unlike previous cryogenic computing studies [10, 11] that extend the MOSFET BSIM4 model for the target cryogenic temperature using data reported in literature, our work relies on a commercial 65 nm process design kit (PDK) whose BSIM4.7-based equations were calibrated with silicon measurements at cryogenic temperatures. Such calibration has concerned different temperature-dependent model parameters, e.g., leakage, threshold voltage, mobility, body factor, series resistances, stress effects, etc. Likewise, the adopted cryogenic-aware PDK also provides statistical models to consider the impact of manufacturing uncertainty on transistor characteristics.

Fig. 1(a)-(d) show the comparison among the original foundry PDK model, the calibrated model, and silicon measurements in terms of current-voltage characteristics at two different temperatures (300 K and 80 K) for an nMOS transistor with channel length $L = 60$ nm and channel width $W = 1$ $\mu$m. From Fig. 1(a) and (c), simulation results of the original model and calibrated model are roughly the same at 300 K, both well-tracking experimental data. However, as the temperature goes down to 80 K, the calibrated model tracks silicon measurements much more accurately, as shown in Fig. 1(b) and (d). To give a reference, the average error of the original model with respect to experimental data at 80 K is more than 18% and 70% in terms of drain-source current ($I_{DS}$) versus drain-source voltage ($V_{DS}$) for gate-source voltage $V_{GS} = 1.2$ V and
$I_{DS}$ versus $V_{DS}$ for $V_{DS} = 1.2 \text{ V}$, respectively. Conversely, for the same bias conditions, the average error achieved by the calibrated model at 80 K is respectively less than 2% and 10% as compared to silicon measurements.

Regarding the impact of cryogenic operation on CMOS characteristics, the main effects are related to increase the charge carrier mobility, saturation velocity, and threshold voltage, as well as an improvement in sub-threshold slope [11–14]. Overall, when cooling down to cryogenic temperatures, CMOS-based circuits can benefit from increased ON/OFF current ratio as shown in Fig. 1, thus resulting in better performance and reduced standby power. Indeed, from Fig. 1(a)-(d), the ON current (i.e., $I_{DS}$ for $V_{DS} = V_{GS} = 1.2 \text{ V}$) increases by about 30% when reducing the temperature from 300 K down to 80 K, whereas the OFF current (i.e., $I_{DS}$ for $V_{DS} = 1.2 \text{ V}$ and $V_{GS} = 0 \text{ V}$) decreases about 1.3 orders of magnitude.

Note that both bitcell- and architecture-level analyses, reported below, are based on the aforementioned cryogenic-aware PDK calibrated on real silicon measurements. Therefore, when compared to the use of predictive models or estimated extrapolations from PDK models calibrated within the typical commercial temperature range, this ensures more reliable simulation-based results at the operating point of 77 K.

2.2. DMTJ devices under cryogenic operation

Fig. 2 shows the structure of a perpendicular STT-DMTJ, which consists of a stack including three CoFeB ferromagnetic (FM) layers along with two thin MgO oxide barriers between the FM layers [8]. The outer FM layers act as top and bottom polarizing reference layers (RL_T and RL_B) with fixed magnetization orientation (antiparallel to each other). Conversely, the middle FM layer, named free layer (FL), has a variable magnetization orientation: parallel (P) or antiparallel (AP) with respect to that of the two RLs. In addition, the two oxide layers feature different thicknesses, i.e., that of the top barrier ($t_{OX,T}$) is greater than the bottom barrier ($t_{OX,B}$).

Overall, this implies two stable states associated with different resistances: low resistance ($R_L$) and high resistance ($R_H$) states (LRS and HRS). More specifically, the LRS (HRS) corresponds to the FL in P/AP (AP/P) configurations with respect to the RL_T/RL_B. Accordingly, $R_L = R_{PT} + R_{APB}$ and $R_H = R_{APT} + R_{PB}$, where $R_{PT/B}$ and $R_{APT/B}$ are the P and AP resistances associated with the top (bottom) barrier, respectively. As shown in Fig. 2, switching from one state to the opposite is carried out by the current-induced STT mechanism, i.e., by applying a current with appropriate direction through the device. More precisely, the $R_L \rightarrow R_H$ ($R_H \rightarrow R_L$) switching can be achieved by a current flowing from the RL_T (RL_B) to the RL_B (RL_T). Thanks to the presence of the two RLs with opposite magnetization orientation, the DMTJ implies symmetric switching across the two transitions along with reduced switching currents as compared to the conventional SMTJ [8, 15, 16]. This occurs at the cost of increased resistance and decreased tunneling magnetoresistance (TMR) ratio (as given by $TMR = (R_{H} - R_{L}) / R_{L}$) owing to the extra oxide barrier [8, 15, 16]. However, the drawback of the reduced $TMR$ is alleviated when operating at cryogenic temperatures due to the intrinsic $TMR$ increase for lower temperatures, as discussed below.

In this work, DMTJ operation is described by a macrospin-based Verilog-A compact model [8], which includes temperature-dependence of physical parameters. Table 1 reports the used parameters and resulting characteristics for two circular devices with different diameters (40 nm and 13 nm) at two operating temperatures (300 K and 77 K). 300 K model parameters of Table 1, such as resistance-area product ($RA$), spin polarization factor ($P$), saturation magnetization ($M_S$), Gilbert damping factor ($\alpha$), and interfacial perpendicular anisotropy constant ($K_I$), were calibrated according to experimental data at 300 K reported in [17, 19, 20]. Note also that,
in order to ensure full compatibility with the CMOS process, the resistance of the shrunk device is scaled down according to the trend reported in [21]. Then, the temperature dependence of some parameters such as \( P, M_S \) and \( K_i \) was modeled by using semi-empirical laws widely used in literature [22–25] as follows:

\[
P(T) = P(0)(1 - \beta T^{3/2}),
\]

\[
M_S(T) = M_S(0) \left[ 1 - \left( \frac{T}{T^*} \right)^{3/2} \right],
\]

\[
K_i(T) = K_i(0) \left( \frac{M_S(T)}{M_S(0)} \right)^{2.18},
\]

where the material-dependent fitting parameters \( \beta \) and \( T^* \) are respectively equal to \( 2 \times 10^{-5} \text{K}^{-3/2} \) [22] and 1120 K [23], whereas 0 K values (i.e., \( P(0), M_S(0), \) and \( K_i(0) \)) are set to meet 300 K values reported in Table 1. According to (1)-(3), Fig. 3(a)-(c) show the trend with

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Figure 2: Sketch of the double-barrier magnetic tunnel junction (DMTJ) device along with STT switching description.
Figure 3: Temperature-dependent physical parameters of the DMTJ device: (a) spin polarization factor ($P$), (b) saturation magnetization ($M_S$), and (c) interfacial perpendicular anisotropy constant ($K_i$).

As the temperature decreases, all three parameters increase, thus resulting in higher values at 77 K with respect to room temperature. This is in line with experimental results reported in [26, 27].

The physical parameters, mentioned above, affect DMTJ characteristics such as resistance, $TMR$ ratio, critical switching current ($I_c$), and thermal stability factor ($\Delta$), which in turn exhibit a temperature dependence as reported in Table 1. The temperature dependence of the resistance and $TMR$ ratio referred to each oxide barrier of the DMTJ is expressed by [22, 24]:

$$G(\theta) = G_T[1 + P^2 \cos(\theta)] + G_S I,$$

$$TMR(T, 0) = \frac{2P^2}{(1 - P^2) + G_S I / G_T}.$$  

Table 1: DMTJ model parameters and characteristics.

| Parameter          | Description                             | DMTJ – 300 K (40 nm, 13 nm) | DMTJ – 77 K (40 nm, 13 nm) |
|--------------------|-----------------------------------------|-----------------------------|-----------------------------|
| $t_{FL}$           | FL thickness                            | 1.2 nm                      |                             |
| $t_{OX,T}$         | Top barrier thickness                   | (1.0, 0.85) nm              |                             |
| $t_{OX,B}$         | Bottom barrier thickness                | (0.5, 0.4) nm               |                             |
| RA                 | Resistance-area product                 | (7, 2) $\Omega \cdot \mu$m$^2$|                             |
| $P$                | Spin polarization factor                | 0.66                        | 0.73                        |
| $M_S$              | Saturation magnetization                | 1.58 T                      | 1.80 T                      |
| $\alpha$           | Gilbert damping factor                  | 0.03 [17, 18]               |                             |
| $K_i$              | Interfacial perpendicular anisotropy constant | $1.3 \times 10^{-3}$ J/m$^2$ | $1.73 \times 10^{-3}$ J/m$^2$ |
| $TMR(0)$           | Tunnel magnetoresistance @ 0 V          | (141, 131)%                 | (205, 198)%                 |
| $R_L$              | Low resistance                          | (5.81, 17.8) k$\Omega$      | (5.99, 18.5) k$\Omega$      |
| $R_H$              | High resistance                         | (14.0, 41.2) k$\Omega$      | (18.3, 55.2) k$\Omega$      |
| $I_c$              | Critical switching current               | (13.6, – ) $\mu$A           | (16.6, 2.9) $\mu$A          |
| $\Delta$           | Thermal stability factor                 | (45, – )                    | (175, 60)                   |

Note that $I_c$ and $\Delta$ is not reported here, since the 13 nm-DMTJ is not thermally stable at 300 K.
\[ TMR(T, V) = \frac{TMR(T, 0)}{1 + \left(\frac{V_{\text{ox}}}{V_T}\right)^2} \]  

where \( G(\theta) \) is the conductance in P (\( \theta = 0 \)) or AP (\( \theta = \pi \)) state, \( G_T \) and \( G_{SI} \) are respectively the prefactor for direct elastic tunneling and the inelastic spin independent conductance term, \( TMR(T, 0) \) is the temperature-dependent \( TMR \) at zero bias voltage, \( TMR(T, V) \) is the \( TMR \) including both temperature and voltage dependence, \( V_{\text{ox}} \) is the voltage drop across the oxide barrier, and \( V_H \) is the voltage drop for \( TMR(T, V) = TMR(T, 0)/2 \). From (4)-(5), the \( TMR \) of each barrier increases with decreasing temperature as given by the \( P \) increase through (1). More specifically, the \( TMR \) increase at lower temperatures is associated with an increase of the antiparallel resistance, whereas the parallel resistance is practically temperature-independent, as reported in Table 1.

The \( I_c \) of the DMTJ is modeled by [8]:

\[ I_c = \frac{\alpha e \gamma_0 \mu_0 H_{k,\text{eff}} M_S V_{FL}}{\mu_B g_{\text{STT}}} \]  

where \( e \) is the electron charge, \( \mu_0 \) is the vacuum permeability, \( \gamma_0 \) is the absolute value of the gyromagnetic ratio, \( V_{FL} \) is the volume of the FL, \( \mu_B \) is the Bohr magneton, \( k_B \) is the Boltzmann constant, and \( g_{\text{STT}} \) refers to the the STT spin efficiency, which is expressed for the DMTJ as [8, 29]:

\[ g_{\text{STT}} = \frac{4P}{1 - P^4} \]  

The \( H_{k,\text{eff}} \) is the effective anisotropy field as given by [25]:

\[ H_{k,\text{eff}} = \frac{2K_i}{t_{FL} \mu_0 M_S} - (N_Z - N_{XY})M_S \]  

where \( N_Z \) and \( N_{XY} \) are respectively the effective demagnetizing factors in the perpendicular and in-plane directions, and \( t_{FL} \) is the FL thickness.

The \( \Delta \) is modeled by [9, 30]:

\[ \Delta = \begin{cases} 
K_{\text{EFF}} V_{FL} & (D \leq D_W) \ 
\pi^2 A_{\text{eff}} V_{FL} & (D > D_W) \end{cases} \]  

where, \( D \) is the device diameter, \( D_W = \pi \sqrt{A_{\text{eff}}/K_{\text{EFF}}} \) is the domain wall width, \( A_{\text{eff}} = 20 \text{ pJ/m} \) is the exchange stiffness constant, and \( K_{\text{EFF}} \) is the effective PMA energy density as given by

\[ K_{\text{EFF}} = \frac{K_i}{t_{FL}} - \frac{\mu_0 M_S^2}{2} (N_Z - N_{XY}). \]

In line with the above modeling, for a given temperature, \( \Delta \) is proportional to the anisotropy and volume of the FL when \( D \) is smaller than \( D_W \) (i.e., when single-domain magnetization reversal takes place), whereas \( \Delta \) does not scale with the device area when \( D > D_W \). Conversely,
the critical switching current $I_c$ exhibits monotonic decrease with the decrease of $D$, as reported in [9, 30]. As a consequence, the $\Delta/I_c$ ratio monotonically increases with decreasing $D$ until $D > D_W$, whereas it becomes constant for $D \leq D_W$. According to (7)-(11), under cryogenic operation, the DMTJ exhibits higher $\Delta$ (i.e., better data retention capability) at the cost of higher switching currents (see Table 1), as determined by the increase in $M_S$ and $K_i$ with decreasing temperature through (2)-(3).

The above discussed tradeoff between data retention capability and switching current can be effectively faced by properly tuning the thermal stability of DMTJ devices operating at cryo-
genic conditions [3, 6]. In other words, the idea is to significantly relax the non-volatility requirement at room temperature by reducing the cross-section area, while meeting the typical 10-years retention time at cryogenic temperatures. In this regard, Fig. 4(a) and (b) show the temperature-dependent $\Delta$ and $I_c$, respectively, as function of the DMTJ diameter. From Fig. 4(a), the DMTJ with 40 nm diameter exhibits $\Delta \approx 45$ at 300 K. According to (7)-(10), the same device shows $\Delta \approx 175$ at 77 K, which corresponds to a significant increase in the $I_c$ by about 20% (see Fig. 4(b)) with a detrimental effect on energy consumption under write access. As shown in Fig. 4(a)-(b), decreasing the cell diameter down to 13 nm allows maintaining 10-years data retention (i.e., $\Delta \approx 60$) at 77 K, while enabling significantly lower $I_c$. The latter thus results in considerably lower energy consumption during the write operation, which is particularly sought after for embedded memories operating at cryogenic temperatures [2]. This can be appreciated in Fig. 5(a)-(b), which report the switching characteristics of the DMTJ with different diameters (i.e., 40 nm and 13 nm) at 300 K and 77 K. From Fig. 5(a), the 13 nm DMTJ allows reducing the write current ($I_{\text{write}}$) to achieve a target write error rate (WER) of $10^{-7}$ [31] at 77 K for a given write pulse width ($t_p$) of 3 ns by more than 85% as compared to the 40 nm device. At the same time, for a given $I_{\text{write}} = 20 \mu A$, the $t_p$ required for WER = $10^{-7}$ at 77 K is reduced from 27.8 ns down to 0.68 ns when decreasing the cell diameter from 40 nm down to 13 nm, as highlighted in Fig. 5(b).

3. Analysis of DMTJ-based STT-MRAM at 77 K

3.1. Bitcell-level simulation results

Fig. 6 shows the schematic of the considered STT-MRAM bitcell, which includes the access transistor and the storage element, typically placed between the second and fourth metal layers (M2 and M4) [32]. Among the different DMTJ-based bitcell topologies, here we refer to the one transistor-one DMTJ in standard connection (i.e., 1T1DMTJ-SC where the minimum-sized access transistor is connected to the RL_T), which allows the best trade-off between area and energy [31, 33].

Bitcell-level analysis was performed within the Cadence Virtuoso environment using the Spectre simulator, while exploiting transistor models of the commercial 65 nm CMOS technology and the Verilog-A based DMTJ compact model described in the previous section. Extensive Monte Carlo (MC) simulations were carried out at the operating temperature of 77 K, while considering the effect of both DMTJ and CMOS process variability. For the DMTJ device, Gaussian-distributed variations were considered with a variability ($\sigma/\mu$) of 5% for the cross-section area and 1% for $t_{OX,T}$, $t_{OX,B}$, and $t_{FL}$, in line with state-of-the-art literature [8, 34–38].

Fig. 7 shows the bitcell-level MC results under both (a) write and (b) read operations when considering the DMTJs with different diameters (40 nm and 13 nm) at 77 K. More precisely, Fig. 7(a) reports the statistical distribution of the $t_p$ that ensures the target WER of $10^{-7}$ in reference to the worst-case switching transition. From this figure, thanks to the reduced $I_c$, the 13 nm DMTJ-based bitcell allows reducing the $t_p$ evaluated at the 6σ corner by ~84% as compared to its 40 nm DMTJ-based counterpart. Fig. 7(b) shows comparative results in terms of the statistical distribution of the bitcell voltage referred to the read operation. The latter is carried out using a conventional voltage sensing scheme [31], i.e., by applying a fixed read current ($I_{\text{read}}$) through the bitcell and comparing the bitcell voltage with a reference voltage by a sense amplifier. The $I_{\text{read}}$ has to be set sufficiently lower than the $I_c$ to ensure a reasonably low read disturbance rate (RDR), i.e., the probability of unintentionally switching the stored data during the read operation. Here, we considered a target RDR of $10^{-9}$ along with a read pulse width ($t_{\text{read}}$) of 1 ns [39].
Figure 5: Switching behavior of the DMTJ devices with different diameters (40 nm and 13 nm) at 300 K and 77 K: (a) write pulse width ($t_p$) to ensure a write error rate (WER) of $10^{-7}$ as a function of write current ($I_{\text{write}}$), and (b) probability distribution function (PDF) of the switching time for $I_{\text{write}} = 20 \mu\text{A}$. Data for the 13 nm DMTJ at 300 K is not reported since it is thermally unstable at room temperature according to $\Delta$ values of Fig. 4(a).

This results in $I_{\text{read}}$ equal to 15.6 $\mu\text{A}$ and 1.91 $\mu\text{A}$ for the 40 nm and 13 nm DMTJ-based bitcells, respectively. Fig. 7(b) also highlights the voltage sensing margin ($V_{\text{SM}}$), i.e., the difference between bitcell voltages corresponding to the DMTJ in HRS and LRS, estimated at both nominal and $3\sigma$ corner. From this figure, the 13 nm DMTJ-based bitcell shows smaller nominal ($3\sigma$) $V_{\text{SM}}$ by $\sim$53% ($\sim$48%) when compared to its 40 nm DMTJ-based counterpart. This is ascribed to the reduced $I_c$ and hence $I_{\text{read}}$, despite the increased resistance of the 13 nm device (see Table 1).
Finally, Table 2 summarizes bitcell-level simulation results for write and read operations at 77 K. Reported data shows that the 13 nm DMTJ-based bitcell is more energy-efficient under both write/read access (–92%/–87%), while also exhibiting better write performance as compared to its 40 nm DMTJ-based counterpart. These advantages are obtained at the cost of reduced (about halved) sensing margin during the read operation. However, this drawback can be properly addressed as proposed in [40].

3.2. Architecture-level simulation results

The memory architecture-level analysis was carried out using the DESTINY estimation tool [41] to evaluate the main STT-MRAM figures of merit, such as access latency, energy per operation and leakage power. Fig. 8 shows the overview of the modeling approach used in the DESTINY tool, where the memory bank architecture is organized as an array of sub-blocks, called Mats. Each Mat consists of multiple sub-arrays along with a predecoder. The sub-array
For the sake of accuracy and to keep consistency with the above bitcell-level analysis, the DESTINY tool was calibrated for an operating temperature of 77 K, as shown in Fig. 8. The read/write electrical characteristics reported in Table 2 were used to describe the bitcell within the memory sub-array, while also specifying information about its area and aspect ratio along with the width of the access transistor. In addition, temperature-dependent technology parameters of the adopted 65 nm CMOS process including both transistor (e.g., threshold voltage, ON/OFF current, mobility, gate capacitance, etc.) and interconnection (e.g., metal resistivity) characteristics were embedded into the source code of DESTINY for an accurate modeling of peripheral memory circuits.
At the memory architecture-level, STT-MRAMs based on DMTJs with 40 nm and 13 nm diameter were benchmarked against conventional 6T-SRAM for different cache sizes, ranging from 64 kB up to 2 MB. Fig. 9(a)-(b) and Fig. 10(a)-(b) show obtained DMTJ-based STT-MRAM results under read/write access in terms of operation latency and dynamic energy consumption, where data is normalized to 6T-SRAM. Leakage power is also reported in the inset of Fig. 10(b). From Fig. 9(a), the STT-MRAM based on 13 nm DMTJ devices exhibits increased read latency by $2.3 \times$ and $2.1 \times$ (averaged over the considered memory capacity range) as compared to the 40 nm DMTJ-based STT-MRAM and the 6T-SRAM, respectively. This is mainly due to the lower $I_{\text{read}}$ applied during read operation (refer to Table 2), which arises from the reduced $I_r$ of the 13 nm device (see Fig. 4(b)). From Fig. 9(b), both DMTJ-based STT-MRAMs exhibit a performance penalty under write access with respect to the 6T-SRAM. However, the use of 13 nm DMTJ devices with relaxed retention time allows significantly reducing this penalty. Indeed,
the 13 nm DMTJ-based STT-MRAM decreases write latency by more than 75%, on average, as compared to its 40 nm DMTJ-based counterpart. Note that, as compared to 6T-SRAM, the STT-MRAM exhibits a read/write access time penalty, although it is reduced as cache memory capacity increases [31]. As shown in Fig. 10(a)-(b), using 13 nm DMTJ devices also allows the STT-MRAM to outperform the 6T-SRAM in terms of dynamic energy consumption under both read/write accesses. From Fig. 10(a), the two STT-MRAM implementations show comparable read energy with a reduction of more than 50% (56% for the 13 nm DMTJ-based STT-MRAM) on average than the 6T-SRAM. In addition, from Fig. 10(b), the 13 nm DMTJ-based STT-MRAM halves write energy as compared to the 40 nm DMTJ-based memory, thus ensuring energy savings of –37% on average with respect to the 6T-SRAM. Looking at the leakage power shown in the inset of Fig. 10(b), the two STT-MRAM implementations exhibit similar static power consumption, which is 98% lower than the 6T-SRAM. Indeed, although the leakage is considerably
Figure 10: Architecture-level results at 77 K of 40 nm and 13 nm DMTJ-based STT-MRAMs versus 6T-SRAM in terms of (a) read and (b) write dynamic energy consumption for memory sizes ranging from 64 kB up to 2 MB. Leakage power in the inset. Data is normalized to conventional 6T-SRAM.

4. Conclusions

In this work, a solution to build reliable, energy-efficient, and high-density STT-MRAMs operating at cryogenic conditions (77 K) has been proven. It consists of using DMTJ devices to exploit their reduced switching currents, while relaxing their non-volatility requirement at room temperature (i.e., by reducing the cross-section area) and maintaining the typical 10-years retention time at 77 K. Our simulation study has been performed at bitcell-level and memory architecture-level by using a commercial 65 nm CMOS technology calibrated down to 77 K under silicon measurements and a macrospin-based DMTJ Verilog-A compact model. As the main reduced by orders of magnitude at cryogenic temperatures [42], 6T-SRAM implementations still suffers from significant static power, mainly consumed by the bitcell array [4, 5].
contribution of our work, results have shown that shrinking the DMTJ cell size (i.e., relaxing its retention time at room temperature) allows improved performance and energy consumption under write access at 77 K. This makes DMTJ-based STT-MRAM operating at 77 K more energy-efficient for both read/write operations than conventional 6T-SRAM, at the only cost of worsened read access time.

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