Flexible FPGA ECDSA Design with a Field Multiplier Inherently Resistant against HCCA

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Abstract—In this paper we describe our flexible ECDSA design for elliptic curve over binary extended fields $GF(2^l)$. We investigated its resistance against Horizontal Collision Correlation Attacks (HCCA). Due to the fact that our design is based on the Montgomery $kP$ algorithm using Lopez-Dahab projective coordinates the scalar $k$ cannot be successful revealed using HCCA, but this kind of attacks can be helpful to divide the measured traces into parts that correspond to processing of a single bit of the scalar $k$. The most important contribution of this paper is that our flexible field multiplier is resistant against horizontal attacks. This inherent resistance makes it a valuable building block for designing unified field multipliers.

Keywords—ECDSA; Montgomery $kP$ algorithm; FPGA implementation; horizontal side channel analysis (SCA) attacks; flexible field multiplier; power traces; electromagnetic traces.

I. INTRODUCTION

Elliptic Curve Cryptography (ECC) provides the same level of security as RSA based approaches with significantly shorter keys. This is especially needed in applications in which resource constraint devices are used e.g. Internet of Things, WSN, automation industry, protection of critical infrastructures. ECC can guarantee confidentiality of communication and can also be used for authentication of persons/devices. One of the potential applications is for example to ensure data integrity and authenticity of communication between cars and road side units (RSUs). Currently traffic lights can be switched without any protection and can also be used for authentication of persons/devices. One of the potential applications is for example to ensure data integrity and authenticity of communication between cars and road side units (RSUs). For signature generation corresponding to Elliptic Curve Digital Signature Standard (ECDSA) [1] each RSU has to use its ECC private key. According to Kerckhoff’s principle the private key has to be kept secret while the applied cryptographically strong cipher algorithm, its input and output values may be publicly known. The goal of attackers is to reveal the private key. Cryptographic algorithms are implemented either in SW or in HW, i.e. they run on a device. The current through the device, its electromagnetic radiation and other physical parameters are caused by each execution of cryptographic operations. If an attacker has physical access to the device, for example to an RSU, he can exploit those side channel effects to reveal its private key. Misusing the key can cause dangerous situations in the traffic, car crashes, etc. In order to avoid malicious attacks the cryptographic implementations need to be protected against a wide variety of side channel analysis (SCA) attacks such as vertical, horizontal, differential, correlation, collision-based attacks etc.

Collision-based attacks [2]-[4], classical differential power analysis [5] and correlation power analysis attacks [6] are vertical attacks. Examples of horizontal attacks are: simple power analysis attacks e.g. [7], simple electromagnetic analysis attacks e.g. [8], the Big Mac attack [9], the localized electromagnetic analysis attack [10], horizontal collision correlation analysis attacks [11]-[13], horizontal differential power analysis (DPA) and differential electromagnetic analysis (DEMA) attacks [14],[15].

Vertical DPA attacks need more measurements than horizontal attacks to be successful exploiting the fact that there is some kind of relation between the different but known processed inputs and the always constant key. Therefore, well-known countermeasures such as EC point blinding, randomization of projective coordinates of EC points or the key randomization proposed in [16] are effective against vertical attacks. But these countermeasures are not effective against horizontal attacks. Thus, protection against vertical DPA is useful only if the design is well protected against horizontal DPA.

Elliptic Curve point multiplication with a scalar, denoted usually as $kP$ operation, is the main operation for ECC. $P$ is a point of the selected EC and has two affine coordinates: $P=(x, y)$. The scalar $k$ is a big binary number; it is a private key if the decryption corresponding to the ElGamal approach [17] is performed. For signature generation the scalar $k$ is a random number. If an attacker can reveal the random scalar $k$ used for a signature generation he can calculate the private key of the signer. As a consequence, the identity of the signer can be stolen. This means that implementations of the $kP$ operation have to be resistant against SCA attacks. Designing a flexible
accelerator for EC point multiplication, i.e. one that can be used for at least two different ECs for example over extended binary fields $GF(2^l)$, is a not trivial task, especially if the design has to be resistant against horizontal SCA attacks.

The main contributions of this paper are:
- performing a HCCA against our flexible ECDSA design;
- evaluation of the resistance of our flexible field multiplier against HCCA showing its inherent resistance.

The rest of the paper is structured as follows. In section II we give a short overview of the ECDSA protocol. Our flexible ECDSA design is described in section III and the HCCA performed is given in section IV. The resistance of our flexible field multiplier is examined in section V. The paper finishes with short conclusion.

II. BACKGROUND: ECDSA

Elliptic Curve Digital Signature Algorithm (ECDSA) is an algorithm to generate digital signatures as described in the NIST documentation [1]. A generation and verification of signature can be implemented as a sequence of mathematical operations in finite fields. The signature generation and verification algorithms are sketched in TABLE I.

| TABLE I. GENERATION AND VERIFICATION OF SIGNATURE CORRESPONDING TO ECDSA |
|---|---|
| Alice has the ECC key pair $(Pub_A, key_A)$ | Bob knows Alice’s public key $Pub_A$ |
| **Signature generation** | **Signature verification** |
| 1. writes a message | 1. receives: $(message, r, s)$ |
| 2. $e = hash(message)$ | 2. $e = hash(message)$ |
| 3. generates random $k < e$ | 3. $u_1 = e/s \mod e$ |
| 4. $T = (x_T,y_T) = k \cdot G$ | 4. $u_2 = r/s \mod e$ |
| 5. $r = x_T \mod e$ | 5. $T = (x_T,y_T) = u_1 \cdot G + u_2 \cdot Pub_A$ |
| 6. $s = (e + r \cdot key_A)/k \mod e$ | 6. $r = x_T \mod e$ ? |
| 7. sends to Bob: $(message, r, s)$ | |

Corresponding to the ECDSA algorithm, public keys are points of an EC and private keys are big binary numbers, smaller than the order $e$ of the base point $G$. $e$ and $G$ are parameters of the EC that was selected for cryptographic operations; they are given in [1]. To generate the signature Alice calculates for the written message its hash $e$ of her message and performs the multiplication of the base point $G$ with a generated random scalar $k$ (see step 4 in TABLE I.), i.e. an EC point multiplication, usually denoted as $kP$ operation.

This operation is a sequence of mathematical operations in the finite field and it is the most time, energy and computation expensive part of the signing protocol. The result of the performed $k \cdot G$ operation is also a point of the EC. Its $x$-coordinate is part of digital signature, denoted as $r$. Using the calculated $r$ and $e$, the generated scalar $k$ and the private key $key_A$ Alice calculates the last part of the signature, denoted as $s$ (see step 6 in TABLE I.). Alice sends her message to Bob with its digital signature, i.e. with two numbers: $r$ and $s$.

Bob receives the signed message from Alice, and verifies the signature. To do this Bob needs to know Alice’s public key $Pub_A$. Bob calculates the hash $e$ of the received message, scalar $u_1$ and scalar $u_2$ (see steps 2-4 in TABLE I.). Then Bob performs two EC point multiplications and one point addition to calculate the point $T$ as shown in step 5 in TABLE I. If the $x$-coordinate of this point is equal to the received $r$, the signature was successfully verified. For the verification Bob doesn’t use his own key pair $Pub_B$ and $key_B$.

III. OUR FLEXIBLE ECDSA DESIGN

As the EC point multiplication is a complex and relatively slow operation, it is often implemented in hardware to accelerate the ECDSA operations. Our ECDSA design is an accelerator for EC point operations for the two NIST ECs B-233 and B-283. The functionality of our flexible ECDSA accelerator is shown schematically in Fig. 1.

![Functionality of our flexible ECDSA accelerator.](image)

Depending on the received command our accelerator selects one of the two ECs – B-233 or B-283 – and performs either a single $kP$ operation, for example a $k \cdot G$ multiplication for a signature generation, or multiple EC point multiplication $u_1 \cdot G + u_2 \cdot Pub$ for a signature verification. Here $G$ is the base point of the selected EC and $Pub$ is the public key used for the signature verification. The main part of our ECDSA design is a flexible accelerator for $kP$ operations.

Due to the fact that the Montgomery $kP$ algorithm is reported in literature as resistant against simple SCA attacks it is the most often one implemented in hardware. For binary ECs the most popular algorithm is the Montgomery $kP$ algorithm using Lopez-Dahab projective coordinates [18], see Algorithm 1.

**Algorithm 1: Montgomery $kP$ using projective Lopez-Dahab coordinates**

```
Input: $k = (k_0 \ldots k_{b-1}) \in \mathbb{Z}$ where $b = l$, $P = (x_0,y_0)$ is a point of EC over $GF(2^l)$
Output: $kP = (x_1,y_1)$
1: $x_0 \leftarrow x_0, Z_0 \leftarrow 1, X_0 \leftarrow x_0^2 + b, Z_0 \leftarrow 1$
2: for $i = l-2$ downto 0 do
3: if $k_i = 1$
4: $T \leftarrow Z_0, Z_0 \leftarrow (XZ_0 + Z_0T_0^2), X_0 \leftarrow xZ_0 + x_0Z_0T_0$
5: $T \leftarrow X_0, X_0 \leftarrow T_0 + bZ_0^2, Z_0 \leftarrow T_0Z_0^2$
6: else
7: $T \leftarrow Z_0, Z_0 \leftarrow (XZ_0 + X_0T_0), X_0 \leftarrow xZ_0 + x_0Z_0T_0$
8: $T \leftarrow X_0, X_0 \leftarrow T_0 + bZ_0^2, Z_0 \leftarrow T_0Z_0^2$
9: end if
10: end for
11: $x_1 \leftarrow X_0Z_0$
12: $y_1 \leftarrow y + (x+x_0)((X_0+xZ_0)(X_0+xZ_0)+x^2/y)(Z_0Z_0) \mod (xZ_0Z_0)$
13: return $(x_1,y_1)$
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This algorithm is a very efficient bitwise processing of the scalar $k$. Only 6 field multiplications, 5 field squarings and 3 field additions are necessary to process a bit of the scalar $k$, whereby the sequence of these operations is independent of the processed bit value. Authors of [19] modified this algorithm slightly to increase its resistance against SCA attacks. When implementing ECC in hardware area-optimized solutions are preferred due to manufacturing costs. Thus, only one field multiplier is usually implemented because the field multiplication is the most complex operation and the multiplier has a large area. A field squaring can be calculated as a field multiplication. In this case it doesn’t require additional area but the processing of each bit of the scalar $k$ consists of $6+5=11$ field multiplications that have to be performed serially. Using EC over extended binary fields $GF(2^l)$ offers the possibility to accelerate the calculation of the $kP$ operation significantly if the field squaring is implemented as follows:

$$C(t) = (A(t))^2 \mod f(t), \text{ with:}$$

$$f(t) = t^{233} + t^{14} + 1 \text{ for } B - 233;$$

$$f(t) = t^{283} + t^{12} + t^7 + t^5 + 1 \text{ for } B - 283;$$

$$(A(t))^2 = (a_{l-3}a_{l-2}a_{l-1} \ldots a_0)^2 = a_{l-3}0a_{l-2}0a_{l-1}0 \ldots 0a_l0a_0$$

If the squaring is implemented corresponding to formula (1) its area is small, the calculation requires only 1 clock cycle and can be done in parallel to multiplications. Due to these facts we implemented the squaring as an additional block in our design.

Addition of $GF(2^l)$ elements is a bitwise XOR operation. Fig. 2 shows the structure of our flexible $kP$ accelerator.

Our design uses only one field multiplier that calculates the field product of elements of $GF(2^{233})$ for EC $B-233$ or elements of $GF(2^{283})$ for EC $B-283$. Fig. 3 shows the structure of our flexible field multiplier.

The polynomial multiplication (i.e. the first step of the multiplication of elements of $GF(2^l)$) can be realized by applying the classical multiplication method. Its gate complexity can be given as a number of Boolean AND and XOR operations, i.e. as the number of used AND and XOR gates. To implement the multiplication of $n$-bit long polynomials using the classical multiplication method $n^2$ AND and $(n-1)^2$ XOR gates are necessary. This results in an expensive implementation with respect to area and energy. We implemented our field multiplier using the 4-segment Karatsuba multiplication method according to a fixed calculation plan corresponding to [20]. Two up to 283 bit long operands $A(t)$ and $B(t)$ are segmented into four parts: $A_3, A_2, A_1, A_0$ and $B_3, B_2, B_1, B_0$ respectively. The field multiplier takes 9 clock cycles to calculate a field product. In each clock cycle only one of 9 partial products of the up to 71 bit long operands is calculated according to the 4-segment Karatsuba formula. We implemented our partial multiplier using the classical MM due to the fact that it can increase the inherent resistance of the $kP$ design against selected SCA attacks. All partial products are accumulated in a register of the multiplier. The field product will be accumulated iteratively, in each clock cycle, using the calculated partial products. The reduction is also performed in each clock cycle.

We ported our design implemented in VHDL to a Xilinx Spartan-6 FPGA [21] using the Xilinx ISE Design Suite version 14.7 (nt64) Parameters of our ECDSA hardware accelerator and its flexible field multiplier are given in TABLE II.

In the next section we explain how we performed the Horizontal Collision Correlation Analysis attacks against the FPGA implementation of our ECDSA design.

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1 If the partial multiplier is implemented corresponding to the classical MM, its area is the biggest one compared to other MMs, as well as its power consumption and the fluctuation of the power. Thus, the partial multiplier can be regarded as a kind of noise source.
TABLE II. PARAMETERS OF OUR FLEXIBLE ECDSA DESIGN

| Parameter                                | Flexible ECDSA | Flexible filed multiplier only |
|------------------------------------------|----------------|-------------------------------|
| Number of Slice Registers (out of 54576) | 6370           | 2634                          |
| Number used as Flip Flops                | 6369           | 2631                          |
| Number used as Latches                   | 1              | 3                             |
| Number of Slice LUTs (out of 27288)     | 10212          | 5445                          |
| Number used as logic                     | 10160          | 5411                          |
| Number used as Memory (out of 6408)     | 10             | 24                            |
| Number used exclusively as route-thrus   | 42             | 24                            |
| Number of occupied Slices (out of 6822) | 3559           | 1612                          |
| Number of LUT Flip Flop pairs used       | 11714          | 5674                          |

IV. ATTACK DESCRIPTION

ECDSA implementations are vulnerable to SCA attacks. If an attacker can reveal the random scalar \( k \) used for a signature generation (see step 4 in TABLE I.) he can calculate the private key of Alice as follows: \( \text{key}_A = (s \cdot k - e) / r \mod z \). Finally, the attacker can examine the correctness of the revealed private key of Alice using the EC point multiplication performed for the generation of Alice’s key pair \( (\text{key}_A, \text{Pub}_A) \): \( \text{key}_A \cdot G = \text{Pub}_A \).

This demonstrates that the implementations of EC point multiplication \( kG \) have to be resistant against SCA attacks. Usually investigations related to differential SCA attacks against ECC implementations describe classical, i.e. vertical attacks that need a lot of measurements to be performed. Horizontal attacks need by far less measurements, time and computations for revealing the key than vertical attacks. Similar to the simple power analysis horizontal DPA attacks need only one measured trace for analysis, which is performed using statistical methods. Horizontal DEMA attacks are even more dangerous as they don’t require difficult preparations such as implantation of a probe resistor into the attacked board.

A. Measurement setup

For running experiments we designed our own board for the measurement of power and especially electromagnetic traces. It is equipped with a Spartan-6 FPGA from Xilinx. We measured the current through the FPGA during a \( kP \) execution. The measured current traces are the power traces. The measurement were done using the Riscure current probe [22]. For evaluation of the flexible field multiplier we measured not only the power traces but also the electromagnetic traces during the execution of field multiplications. The electromagnetic traces were measured using an MFA-R-75 EM probe from Langer [28] with an integrated amplifier. Traces were captured using a LeCroy WaveRunner 610Zi oscilloscope with a 2.5 GS/s sampling rate, i.e. with 625 measurement points per clock cycle due to the clock frequency of 4 MHz. Fig. 4 shows our measurement setup and especially a zoom in for the EM measurements.

B. Horizontal Collision Correlation Attack

In [13] a Horizontal Collision Correlation Attack on ECs was published. The main assumption is that an attacker can distinguish two multiplications with at least one common multiplicand from two multiplications with different multiplicands. This knowledge can be used for revealing the key because a point doubling can be distinguished from a point addition even in double-and-add \( kP \) algorithms obeying atomicity principle [23].

The field multiplier attacked in [13] was implemented using the classical multiplication formula. Experimental results in [24] show that Pearson’s coefficients calculated for traces of two multiplications with a common operand differ significantly from coefficients calculated for two multiplications with different operands. Using this type of attack against the Montgomery \( kP \) algorithm for binary ECs the scalar \( k \) will not be revealed but this attack can help to separate measured traces into slots. A part of a trace that corresponds to the processing of a single key bit of the scalar \( k \) is denoted as a slot.

The separation of traces into slots is a preparation step of horizontal DPA and DEMA attacks [ref]. For the Montgomery \( kP \) algorithm the separation of traces into slots can be done due to the fact that a multiplication with EC parameter \( b \) (or a multiplication with \( x \) coordinate of input point \( P \)) is executed in each slot in the main loop of Algorithm 1. In our implementation each slot consists of 6 field multiplications. The multiplication with the parameter \( b \) is the 3\textsuperscript{rd} of the 6 multiplications. The multiplication with the \( x \) coordinate of input point \( P \) is the 5\textsuperscript{th} of the 6 multiplications. All other multiplications, i.e. the 1\textsuperscript{st}, 2\textsuperscript{nd}, 4\textsuperscript{th} and 6\textsuperscript{th} of the 6 main loop multiplications have always different operands. We performed a horizontal collision correlation attack as follows:

1. We selected the part of the measured trace to be analysed. This part corresponds to the processing of the data in the main loop of the implemented \( kP \) algorithm.
2. We represented each clock cycle in the analysed part of the traces using only one value that we calculated using all measured values (samples) within the clock cycle, i.e. we compressed the measured trace as follows:

\[
\gamma_{\text{compressed}} = \frac{1}{N} \sum_{i=1}^{N} \left( \gamma_{\text{measured}} \right)^2
\]

Here \( \gamma_{\text{compressed}} \) is the averaged squared amplitude value of all samples in a clock cycle; \( N \) is the number of measured values within the clock cycle, in our measurement setup \( N=625 \). The
squaring in (2) leads to the fact that the impact of the noise in our experiments is reduced. After compressing each slot consists of 54 values and each field multiplication consists of only 9 values.

3 – We calculated an average power profile of the multiplication with the parameter \( b \) using profiles of all multiplications with this operand within \( kP \), i.e. we calculated the average profile of the 3rd of 6 multiplications in the main loop, i.e. of the clock cycles 19-27. We denote this profile as \( b \cdot M2 \). This profile consists of 9 values.

4 – We calculated Pearson’s coefficients for the averaged power profile denoted as \( b \cdot M2 \) and each multiplication during the processing of the scalar \( k \) in the main loop of implemented algorithm.

5 – We represented the calculated coefficients graphically, see Fig. 5-(a). The analysed trace contains about 1400 field multiplications performed in the main loop of the implemented algorithm for B-233 (see left graphic in Fig. 5-(a)) and about 1700 multiplications for B-283 (see right graphic in Fig. 5-(a)). The Pearson’s coefficients calculated for the averaged power profile \( b \cdot M2 \) and each multiplication with the operand \( b \) are shown as red dots, all others are blue.

6 – We calculated an average power profile of the multiplication with the \( x \)-coordinate, i.e. we calculated the average profile of the 5th of the 6 multiplications in the main loop (clock cycles 37-45) and we denoted this profile as \( Px \cdot M2 \).

7 – We calculated Pearson’s coefficients for the averaged power profile \( Px \cdot M2 \) and each multiplication within the processing of the scalar \( k \) in the main loop of the implemented algorithm.

8 – The calculated coefficients are represented in Fig. 5-(b): the left graphic shows the results for B-233 and the right graphic for B-283. The Pearson’s coefficients calculated for the averaged power profile \( Px \cdot M2 \) and each multiplication with the operand \( Px \) are marked as red dots, all others are blue.

9 – Additionally, we calculated an average power profile of the 1st of 6 multiplications in the main loop, i.e. clock cycles 1-9. We denoted this profile as \( M1 \cdot M2 \).

10 – We calculated Pearson’s coefficients for the averaged power profile \( M1 \cdot M2 \) and each multiplication during the processing of the scalar \( k \) in the main loop of implemented algorithm.

11 – The calculated coefficients are given in Fig. 5-(c): the left side shows the results for B-233 and the right side for B-283. The Pearson’s coefficients calculated for the averaged power profile \( M1 \cdot M2 \) and the 1st multiplication in each main loop iteration are marked in red, all others are blue.

The result of the analysis is: if a trace of the whole \( kP \) design is analysed the calculated Pearson’s coefficients allow to distinguish many of the investigated multiplications (marked as red dots) from other multiplications (marked in blue).

### V. INHERENT RESISTANCE OF FLEXIBLE FIELD MULTIPLIER

To evaluate the inherent resistance of our flexible field multiplier we implemented it without any countermeasures against SCA, i.e. the sequence of the multiplication was not randomized as for example in [25], and multiplications are not masked. We ported only our flexible multiplier to the FPGA. To investigate its resistance against Horizontal Collision Correlation Attack introduced by A. Bauer et. al. in [13] we performed the following experiments:

1. We measured the power traces of the product calculation for 4 multiplications with one common and two completely different operands: \( \text{mult} = a \cdot b \); \( \text{mult} = c \cdot d \); \( \text{mult} = e \cdot a \); \( \text{mult} = f \cdot g \).

2. We calculated Pearson coefficients \( K_i \) (1 ≤ i ≤ 4) using the power shape of following multiplications: \( K1 \) using \( \text{mult} \) and \( \text{mult3} \) \( \text{mult} \) here operand \( a \) is common in two multiplications; \( K2 \) using \( \text{mult2} \) and \( \text{mult} \); \( K3 \) using \( \text{mult3} \) and \( \text{mult2} \); \( K4 \) using \( \text{mult4} \) and \( \text{mult2} \). Coefficients \( K2 \), \( K3 \) and \( K4 \) correspond to multiplications with different operands.

If the coefficient \( K_i \) differs significantly from \( K1 \) and \( K4 \), the multiplications with a common operand \( \text{mult} \) and \( \text{mult3} \) are distinguishable from multiplications with different operands such as \( \text{mult2} \) and \( \text{mult3} \). Please note that this distinguishability has to be observed for each experiment (see steps 1) and 2)) for successfully revealing scalar \( k \).
performing an HCCA against double and add algorithms obeying the atomicity principle.

We performed the experiment described above 20 times for multiplicands of a length of 233 bits (for EC $B-233$) and of 283 bits (for EC $B-283$). Fig. 6 shows coefficients $K_1 - K_4$ calculated for all experiments. The coefficients $K_i$ are represented by red dots, $K_2$ by blue dots, $K_3$ by blue triangles and $K_4$ by blue crosses. It can be seen that the set of coefficients represented by red points is indistinguishable from other coefficients.

Due to the fact that the calculated Pearson coefficients do not allow to separate two groups of multiplication (see Fig. 6) i.e. multiplications with common operands cannot be distinguished from those with different operands, the inherent resistance of our investigated flexible multiplier against HCCA is high. This fact can be exploited to design a unified field multiplier, for ECs $P-224$, $P-256$, $B-233$ and $B-283$. To the best of our knowledge such a filed multiplier, based on the 4-segment Karatsuba multiplication formula, was not yet reported in literature. In comparison to a multiplier implementing the classical MM using the same field components of our design, i.e. its field multiplier. The result of our investigation is that the multiplier itself is resistant against HCCA.

**ACKNOWLEDGMENT**

This research has been funded by the Federal Ministry of Education and Research of Germany under grant number 03ZZ0527A.

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