Reversible Charge-Polarity Control for Multioperation-Mode Transistors Based on van der Waals Heterostructures

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Van der Waals (vdW) heterostructures—in which layered materials are purposely selected to assemble with each other—allow unusual properties and different phenomena to be combined and multifunctional electronics to be created, opening a new chapter for the spread of internet-of-things applications. Here, an O\textsubscript{2}-ultrasensitive MoTe\textsubscript{2} material and an O\textsubscript{2}-insensitive SnS\textsubscript{2} material are integrated to form a vdW heterostructure, allowing the realization of charge-polarity control for multioperation-mode transistors through a simple and effective rapid thermal annealing strategy under dry-air and vacuum conditions. The charge-polarity control (i.e., doping and de-doping processes), which arises owing to the interaction between O\textsubscript{2} adsorption/desorption and tellurium defects at the MoTe\textsubscript{2} surface, means that the MoTe\textsubscript{2}/SnS\textsubscript{2} heterostructure transistors can reversibly change between unipolar, ambipolar, and anti-ambipolar transfer characteristics. Based on the dynamic control of the charge-polarity properties, an inverter, output polarity controllable amplifier, p-n diode, and ternary-state logics (NMIN and NMAX gates) are demonstrated, which inspire the development of reversibly multifunctional devices and indicates the potential of 2D materials.

1. Introduction

With the continuous scaling down of electronics and the urgent need to handle data explosion, the internet of things (IoTs) has risen in use and popularity in the past decade. The IoTs comprise widely distributed devices with multifunctionality that are interconnected, providing real-time communication of the scope of what we want to know and what we want to do.[1–3] The new era of the IoTs not only highlights a productive new avenue for a whole generation of information devices but also provides an opportunity to surpass the limits of Moore’s law. A range of novel 2D materials has been actively explored for More-Moore and More-than-Moore applications because of their unique structures and optoelectronic properties.[4–6] By vertically or/and laterally assembling the 2D materials, its integration of artificial van der Waals
(vdW) heterostructures can be further used to create diverse devices including tunneling transistors,\textsuperscript{[7,8]} atomically p-n junctions,\textsuperscript{[9–12]} light-emitting diodes,\textsuperscript{[13]} reconfigurable field-effect transistors,\textsuperscript{[14,15]} nonvolatile memories,\textsuperscript{[16,17]} and even multifunctional devices.\textsuperscript{[18–24]} These atomically vdW heterostructures-based systems, possessing ultra-low-power, low-loss, and energy-efficient active features, fully satisfy the requirement of the fast-growing IoTs paradigm.

The assembled vdW heterostructures, which do not suffer from impurities or interfacial defects, have high-quality interfaces and are highly suited to use in state-of-the-art electronics with desired multi-functionalities.\textsuperscript{[25,26]} For example, in 2015, a band-to-band tunneling transistor in a MoS\textsubscript{2}/WSe\textsubscript{2} vdW heterostructure was made using a dual-gate device architecture.\textsuperscript{[18]} Under different gate-voltage ($V_g$) modulations, the vdW system behaved as either an Esaki diode, a backward diode, or a forward rectifying diode, making the device highly versatile. In 2017, a fine band-structure alignment using a broad-bandgap black phosphorus (BP) and large-bandgap MoS\textsubscript{2} stacking was achieved, in which a large current rectification ratio of 10$^7$ and a high on-off current ratio up to 10$^8$ were realized by integrating both the high-performance diode and transistor in a single device.\textsuperscript{[19]} A ternary inverter can be further achieved by matching the partition load and band structure in the vertical heterostructure. In the same year, because the charge carrier injection can be switched between tunneling and thermal activation under different bias polarities, a multifunctional device, including a diode, transistor, photodetector, and multi-state memory, was reported.\textsuperscript{[20]} A similar asymmetric configuration combined with a floating-gate charge layer was also been adopted in WSe\textsubscript{2}/hexagonal boron nitride/graphene heterostructures for multi-purpose optoelectronic applications.\textsuperscript{[21]} In addition, in BP/ReSe\textsubscript{2} heterostructures, the tunability of diverse current-transport characteristics was demonstrated using the variation of the BP layer thickness.\textsuperscript{[22]} To date, most of the above-related approaches for preparing multifunctional devices have been limited by either complexity in fabrication technology and/or inflexibility in reversible operation, which significantly limit the possibility of multifunctional integrations.

Precisely controlling the conduction behavior, such as conductive polarities or doping degrees, is the key to achieving practical applications for vdW heterostructures.\textsuperscript{[23,28–31]} In general, after choosing specified 2D materials, the vdW devices will exhibit unchanged conduction behaviors, because the conduction behaviors as well as band structure alignments, directly depend on the nature and corresponding thickness of the selected 2D materials. A convertible conducting channel in a single device based on a vdW system, which allows for higher integration and compatibility, is still lacking. Herein, we propose a new and simple strategy for dynamically controlling and optimizing the electronic properties of vdW heterostructures-based electronics, and then realize their multifunctional applications in a “single device.” MoTe\textsubscript{2} has been proved to be ultrasensitive to O\textsubscript{2},\textsuperscript{[32–36]} Charge carriers of MoTe\textsubscript{2} flakes could be easily modulated, which is primarily attributed to the amount of O\textsubscript{2} adsorptions on the MoTe\textsubscript{2} surface, particularly at its tellurium defects. Such the adsorption process is reversible when MoTe\textsubscript{2} flakes are stored in a reversed-O\textsubscript{2} condition. Therefore, in this study, through the rapid thermal annealing (RTA) strategy between dry-air (80% N\textsubscript{2}, and 20% O\textsubscript{2}, 1 atm) and vacuum conditions, a tunable charge-polarity device based on MoTe\textsubscript{2}/SnS\textsubscript{2} vdW heterostructures were fabricated. Compared with MoTe\textsubscript{2}, the electrical properties in SnS\textsubscript{2} with a suitable thickness exhibit relative stability in different O\textsubscript{2} concentrations. The simple RTA strategy in different conditions enables precise tuning of the doping level and effective modulation of the transport behavior in the MoTe\textsubscript{2} flakes in a large dynamic range, thus allowing the MoTe\textsubscript{2}/SnS\textsubscript{2} vdW heterostructure to be reversibly switched between unipolar, ambipolar, and anti-ambipolar-dominated transistors. Finally, the flexible multi-operation modes of logic-circuit applications, for example, inverter, p-n diode, output polarity controllable (OPC) amplifiers, and ternary-state NMIN and NMAX logics can be precisely engineered. Our proposed strategy for multi-operation-mode transistors is highly promising in the prospective of future electronics, as well as the growing IoTs generation.

Bulk 2H-phase MoTe\textsubscript{2} is an indirect band gap material, with a band gap in the range of 0.6–1 eV.\textsuperscript{[17]} At the beginning of research on layered MoTe\textsubscript{2} transistors, ambipolar behavior in the charge polarity has been revealed.\textsuperscript{[38]} Subsequently, it has been demonstrated that oxygen present in the environment can significantly alter the electrical properties of layered MoTe\textsubscript{2} devices. Such related research can be traced back to 2015.\textsuperscript{[34,36,39,40]} The presence of tellurium defects and the functionalization of these defect sites with O\textsubscript{2} molecules strongly dictate the electronic structure and create deep or shallow states with the optical band gap. Moreover, by varying the vacuum level during the RTA,\textsuperscript{[34,36,39,40]} electrothermal doping process,\textsuperscript{[31]} and scanning visible-light method,\textsuperscript{[42,43]} the transfer characteristics of layered MoTe\textsubscript{2} transistors can distinctly shift to show different polarities between unipolar-like and symmetric ambipolar behaviors owing to the physical or chemical adsorption and dissociation of O\textsubscript{2} associated with the energy level of these strategies.

Based on the O\textsubscript{2}-ultrasensitive MoTe\textsubscript{2} surface, Figure 1a shows a schematic diagram of reversible charge-polarity control for a multi-operation-mode vdW heterostructure, in which two layered materials, MoTe\textsubscript{2} and an O\textsubscript{2}-insensitive n-type flake, were selected to integrate with a vertical stack to form a vdW transistor. First, we considered that in ambient conditions
Figure 1. a) Simplified principle of reversible charge-polarity control for a multioperation-mode transistor. i) Schematic illustration of oxygen adsorption and desorption processes on the surface of a MoTe$_2$-based vdW heterostructure. Owing to the presence of Te vacancies on exfoliated MoTe$_2$ surfaces, the electrical properties of the MoTe$_2$-based vdW heterostructure were highly sensitive to different O$_2$ concentration environments. ii) Corresponding transfer characteristics of a MoTe$_2$ channel with different degrees of oxygen adsorption. b) Schematic diagrams of the transfer-curve shift for a MoTe$_2$-based vdW heterostructure. Under different degrees of O$_2$ adsorption, the vdW heterostructure shows i) unipolar, ii) ambipolar, and iii) anti-ambipolar charge polarity.

(i.e., relatively high O$_2$ concentration), the O$_2$ vapor naturally adsorbs on the MoTe$_2$ surface, in particular, at the tellurium defects, where charge carriers for MoTe$_2$ would be trapped, and then its polarity becomes hole dominated. An effective p-type doing of MoTe$_2$ was hence developed, as shown in the left-hand panel of Figure 1ai. However, the adsorbed O$_2$ with low adsorption energy on the MoTe$_2$ surface would potentially be removed when the MoTe$_2$-based vdW heterostructure was put in vacuum (i.e., relatively low O$_2$ concentration) condition for a period of time or a given additional energy. Such desorption of O$_2$ could release charge carriers again back to the MoTe$_2$, leading to n-type doping of the vdW heterostructure, as shown in the right-hand panel of Figure 1ai. This process of O$_2$ adsorption/desorption has been proven to be controlled and reversible, freely creating p/n charge polarity in MoTe$_2$. A typical variation of transfer characteristics of a MoTe$_2$ channel is illustrated in Figure 1aii for different degrees of O$_2$ adsorption. Schematic diagrams of the transfer curve shift for the MoTe$_2$-based vdW heterostructure with increasing adsorbed O$_2$ concentration, are shown in Figure 1b for i) unipolar, ii) ambipolar, and iii) anti-ambipolar-dominated charge-polarity transistors. Thus, through O$_2$ adsorption-evacuation cycles, the inflexibility in charge polarity for typical vdW heterostructures can be broken, achieving multioperation-mode transistors.

To realize the concept of reversible charge-polarity control for multioperation-mode transistors based on vdW heterostructures outlined in Figure 1, vertically stacked MoTe$_2$/SnS$_2$ heterostructure transistors were fabricated. A schematic diagram of the structural configuration of a MoTe$_2$/SnS$_2$ heterostructure with the circuit layout is shown in Figure 2a. To enhance the adsorbed/removed O$_2$ effect on the MoTe$_2$ surface, a few-layered MoTe$_2$ flake was intentionally stacked on top of the SnS$_2$ flake. Ti/Au films were used as metallic electrodes to optimize the electrical properties and adhesion. The electrode contact on SnS$_2$ was grounded, while a source–drain voltage ($V_{sd}$) was applied on the MoTe$_2$. The inset of Figure 2a shows an optical image of the as-fabricated MoTe$_2$/SnS$_2$ vdW heterostructure transistor. Atomic force microscopy (AFM) was performed to measure the thickness of the MoTe$_2$ and SnS$_2$ flakes. The corresponding height profiles (Figure 2b) show that the thicknesses of the MoTe$_2$ and SnS$_2$ flakes were ≈8 and 30 nm, respectively. An AFM image of the vdW heterostructure is shown in Figure S1, Supporting Information. Raman scattering measurement was then carried out on different channel areas of the as-fabricated transistor and the results are shown in Figure 2c. The peak of A$_{1g}^\text{L}$ at 172 cm$^{-1}$, E$_{2g}^\text{L}$ at 232 cm$^{-1}$, and B$_{2g}^\text{L}$ at 291 cm$^{-1}$ correspond to MoTe$_2$ (red line), while the Raman spectrum of the...
SnS$_2$ shows an A$_{1g}$ peak at 314 cm$^{-1}$ (blue line). All of these peak positions are consistent with previous reports.$^{[44]}$ In the heterostructure region (black line), the peaks show contributions from both materials, indicating the presence of two distinct materials. Figure 2d further shows transfer characteristics ($I_d-V_g$) of the as-fabricated MoTe$_2$ and SnS$_2$ transistors at $V_d = 1$ V before any annealing treatment. The transfer in the as-fabricated MoTe$_2$ is dominated by n- and p-type carriers under positive and negative gate biases, respectively, resulting in ambipolar behavior (red curve), while the as-fabricated SnS$_2$ shows n-type transport throughout the entire scan from $-60$ to 60 V (blue curve). Unlike other anti-ambipolar heterostructures reported in previous work,$^{[45]}$ our as-fabricated MoTe$_2$/SnS$_2$ heterostructure exhibits electron-dominated ambipolar transfer characteristics at different $V_d$ values before annealing, as shown in Figure 2e, primarily because the hole doping of the as-fabricated MoTe$_2$ is far from its balanced level. The corresponding output characteristic of the heterostructure has also been monitored to display no rectification, indicating the formation of good contacts at the semiconductor-metal interfaces (not shown here).

It has been demonstrated that the binding energy arising from the interaction between O$_2$ (and/or H$_2$O) and the layered MoTe$_2$ surface is only in the range of 30–60 meV,$^{[32]}$ which is comparable to room-temperature energy and strongly implies that adsorbed molecules could be desorbed by suitable thermal energy. Hence, we deliberately adopted the RTA process to accelerate the O$_2$ reaction under dry-air and vacuum conditions, then developed a versatile O$_2$ doping approach that enables highly effective and nonvolatile band modulation of the MoTe$_2$-based vdW heterostructures. Doping was done by applying the RTA process on the vdW transistor at a fixed temperature for 1 min under dry-air conditions. The vdW transistor was then put into the probe station and a transfer curve was recorded to characterize its transport behavior. The transfer characteristics for different annealing temperatures from 150 to 200 °C are shown in Figures 3a and 3b for the MoTe$_2$ and SnS$_2$ transistors, respectively. The solid and dashed lines are semilog and linear plots, respectively. It is noticed that no meaningful hysteresis loop was observed in the transfer curves, either activation condition exists or not. The magnitude of the change was qualitatively proportional to the annealing temperature. As shown in Figure 3a, the MoTe$_2$ transistor...
transforms from having electron-dominated ambipolar behavior before annealing to a highly doped unipolar p-type transistor as the annealing temperature increases from 150 to 200 °C. In contrast, the SnS2 transistors underwent the same RTA treatment and showed very little response despite a gradual reduction in on-state current ($I_d$) from 5.2 to 4.2 μA at $V_g = 60$ V (see Figure 3b). Such a relatively weak response to the RTA process mainly results from a lower surface-to-volume ratio of the thicker SnS2 channels because the molecule adsorption/desorption is a surface effect. The thickness evidence is shown in Figure S2, Supporting Information. It was found that the $I_d$ values at a fixed $V_g$ condition for a thin SnS2 transistor significantly dropped by two orders of magnitude after the RTA process, as shown in Figure S2a,b, Supporting Information, which provides direct evidence to support our expectation. Therefore, a thicker SnS2 flake was selected as an O2-insensitive n-type material to give reversible charge-polarity vdW heterostructures. Here, to maintain a suitable current on-off modulation, the range of the SnS2 thickness was typically chosen from 20 to 50 nm for vdW p-n stackings.

Figures 3c and 3d show the transfer characteristics of the MoTe2/SnS2 vdW heterostructure with different annealing temperatures from 150 to 200 °C under a dry-air condition in semilog and linear scales, respectively. The vdW transistor evolved from having electron-dominated ambipolar behavior before annealing (see Figure 2e) to highly balanced ambipolarity (gray line in Figure 3c), and then to anti-ambipolar charge transport (red line in Figure 3c) as the annealing temperature increased from 150 to 200 °C. In the linear plot of the transfer curves, the height of maximum $I_d$ values is marked as $I_{peak}$ (see Figure 3d). As the annealing temperature increases, the $I_{peak}$ gradually increases, bringing a more obvious anti-ambipolar charge transport, as well as p-type doping in the MoTe2. In addition, the positions of the corresponding $I_{peak}$ (i.e., $V_{peak}$) and threshold voltage ($V_{th}$) for the MoTe2 and SnS2 transistors are displayed as a function of annealing temperature in Figure 3e. The $V_{peak}$ and the $V_{th}$ of MoTe2 increased linearly with the annealing temperature from 150 to 200 °C, whereas the SnS2 transistor maintained a $V_{th}$ of around −45 V (inset), regardless of thermal treatment, suggesting again that the charge-polarity change of the vdW transistor is attributed to the doped MoTe2. Through the RTA doping treatment, we were able to reconfigure the MoTe2 transistor to the desired properties for a suitable device application. The outcome in Figure 3f verifies the clear formation of the anti-ambipolar vdW heterostructure at the junction of two opposite polarity transistors under 200 °C RTA treatment, in which the off-state voltages around −60 and 36 V are displayed. It is emphasized that the maximum of applied $V_d$
to the vdW heterostructure is not higher than 2 V, which makes no meaningful impact on Joule heating to alter the charge polarity. In short, using the simple RTA strategy, we can precisely control the transition from the electron-dominated ambipolar to anti-ambipolar states and accurately modulate both the $I_{\text{peak}}$ height, as well as its position, which is critical for building more functional blocks using the vdW heterostructures.

To visualize the polarity change process during the RTA treatment, the conventional equation $\mu_n, p = (L/W)C_gE_{\text{ox}}V_d$ was used, where $\mu_{n, p}$ is the field-effect mobility for electrons and holes, $L/W$ is the channel length-to-width ratio, $C_g = 1.15 \times 10^{-8}$ F cm$^{-2}$ is the gate-oxide capacitance per unit area for a 300-nm SiO$_2$ dielectric and $\mu_{n, p} = dI/dV_d$ is transconductance. The MoTe$_2$ mobility for holes was found to increase by one order of magnitude from 0.4 to 4.3 cm$^2$ V$^{-1}$ s$^{-1}$ at $V_d = 1$ V at the highest annealing temperature (i.e., 200 °C), while that for electrons decreased from 16.9 to 0.8 cm$^2$ V$^{-1}$ s$^{-1}$ at $V_d = 1$ V, as depicted in Figure 4a. Further taking the relation of $n, p = (I_d \cdot (L/W))/(qV_d\mu_{n, p})$ into consideration, where $q$ is the elementary charge, the corresponding carrier concentration ($n$) for holes increased by 1.4 times from $3.5 \times 10^{12}$ to $4.3 \times 10^{12}$ cm$^{-2}$, while that ($n$) for electrons decreased by 1.2 times from $6 \times 10^{12}$ down to $4.7 \times 10^{12}$ cm$^{-2}$, which provides consistent evidence for the adsorption of O$_2$ molecules on the MoTe$_2$ surface resulting in the down-shifted Fermi level ($E_F$) in MoTe$_2$ (see Figure 4b). In contrast, both the mobility and carrier concentration for SnS$_2$ remained constant to be 1.1 cm$^2$ V$^{-1}$ s$^{-1}$ and $6.6 \times 10^{13}$ cm$^{-2}$, respectively, as a function of annealing temperature (Figure 4c), again confirming the O$_2$-insensitive properties of SnS$_2$ at suitable flake thickness. In this work, we monitored more than ten devices treated using the same RTA strategy. There were unavoidable variations, such as doping mobility and carrier concentration for individual material or $I_{\text{peak}}$ position and on-state current for anti-ambipolar transfer characteristics due to differences in channel quality, geometry, and minute process-to-process deviations, but all devices behaved the same qualitatively in terms of reversibility between the ambipolar and anti-ambipolar states and tunability of the peak position under the RTA treatment (see Figure S3, Supporting Information). In addition, the RTA treatment doping was bidirectional and reversible when the MoTe$_2$/SnS$_2$ vdW heterostructure was exposed cyclically between the dry-air and vacuum conditions to allow O$_2$ adsorption/desorption on the MoTe$_2$ surface, as shown in Figure 4d. The corresponding reversibility for the MoTe$_2$ and SnS$_2$ transistors is shown in Figure S4, Supporting Information. Notice that the transfer curve of the vdW heterostructure can be back to the as-fabricated case, like the result presented.
in Figure 1e, if the RTA temperature applied was higher than 200 °C and the device could withstand an extended treatment time. However, this introduced a greater possibility of damage to the 2D materials, which is not within the scope of this work and is not discussed here. Since the RTA improvement of contact resistance at the metal-semiconductor interface is irreversible, the formation of oxidation is irreversible, the above description in electrical properties strongly supports again that the doping/dedoping reversibility is due to the adsorption/desorption processes of O₂ molecules onto the surface of MoTe₂. Other supplementary are provided in Figures S5 and S6, Supporting Information. Let us consider the energy-band diagrams to explain the detail of the cycle (i.e., dry-air and vacuum) of the RTA strategy for the MoTe₂/SnS₂ vdW heterostructure, as illustrated in Figure 4e. The adsorbed/desorbed O₂ molecules act as carrier acceptors/donors to donate additional holes/electrons to the MoTe₂ flakes, which results in its downward/upward E_F shift, as well as the polarity change of the vdW heterostructure. Additionally, notice that MoS₂, the most used 2D material, is an intrinsically n-type semiconducting channel because of the existence of sulfur vacancies and is relatively O₂-stable. It is widely believed that the charge polarity of MoS₂ cannot be easily changed, compared with ambipolar-type MoTe₂. Therefore, the MoS₂ potential is not considered in this work.

Integration of an O₂-ultrasensitive MoTe₂ material and an O₂-insensitive SnS₂ material to form a vdW heterostructure allows us to modulate and control the device under different degrees of oxygen adsorption. As proof of concept to multifunctionality in a single device, several operation modes of logic-circuit applications were designed and demonstrated according to unipolar-, ambipolar-, or anti-ambipolar-mode MoTe₂/SnS₂ vdW heterostructure transistors, as illustrated in Figure 5. First, an inverter function, which is one of the typical binary-states circuits and can be normally realized in as-fabricated MoTe₂/SnS₂ vdW transistors, was achieved using a unipolar vdW transistor connected to a load resistor. Figure 5a shows the transfer characteristics and the voltage gains (∼dV_out/dV_in) of the inverter at different V_DD values, where V_out, V_in, and V_DD denote the output, input, and supply voltage, respectively. With a low V_in (i.e., logic 0), a high V_out (i.e., logic 1) is achieved, and vice versa. For the ambipolar-mode feature, an OPC amplifier based on a single active device is presented. A sinusoidal signal V_in was applied to the gate electrode, while the output signal was detected using an oscilloscope. When the ambipolar MoTe₂/SnS₂ vdW transistor exhibited n-type behavior, for larger/smaller V_in, more conductive/insulating states, as well as smaller/larger V_out, can be achieved, which is called the out-of-phase or common-drain mode (see Figure 5b). In contrast, when the vdW transistor worked as a p-type channel, V_out increased synchronously with the increase of V_in, which is called the in-phase or common-source mode for the OPC amplifier, as shown in Figure 5b. The demonstration of both modes in the vdW transistors suggests that more complicated circuits could be developed such as phase-shifting key. The schemes of an inverter and OPC amplifier circuits equipped with an off-chip resistor are shown in Figure S7, Supporting Information. The MoTe₂/SnS₂ vdW heterostructure transistor treated with the highest annealing treatment was further used to demonstrate the potential of the anti-ambipolar mode feature. It is easy to understand as the vdW heterostructure is formed by a balanced p- and n-transistor in series, in which the total current reaches a maximum when both transistors are turned on, and then the anti-ambipolar behavior occurs. Therefore, a simple application using the anti-ambipolar mode transistor is a rectifying p-n diode, as shown in Figure 5c. The inset displays the feature of half-wave characteristics by applying sinusoidal V_DD at 5 Hz. Finally, we demonstrated a ternary-states inverter, which is a basic block in multivalued logic applications. Figure 5cii shows the equivalent circuit of the vdW heterostructure-based ternary inverter, which uses the MoTe₂ transistor as a load resistor and the vdW heterostructure as a driver. The inset shows the corresponding optical microscopy (OM) image. Figure 5ciii plots the V_out variation and the voltage gains of the ternary inverter as a function of V_in at different V_DD values. When V_in was low, the vdW heterostructure region was fully turned off, but the MoTe₂ transistor provided a small resistance path between V_DD and V_out, leading to the output of logic “1.” When a large V_in was applied, the load resistor (i.e., MoTe₂ transistor) was turned off, but the heterostructure reached a high conductance, and thus, the device outputs a logic “0.” At a moderate V_in, the resistances of the load resistor and the driver were almost equal, which resulted in the output values of the logic state “1/2.” It is also observed that the width of the “1/2” state plateau can be controlled by applying V_DD values. The “1/2” logic state and its gain monotonically increase with V_DD, which is attributed to how obvious is the anti-ambipolar “A” shape in the transfer characteristics. To demonstrate the applicability of the ternary-state devices for complex logic operations, NMIN and NMAX gates are further simulated. The logic circuit diagrams and the corresponding truth tables of the NMIN and NMAX are illustrated in Figure 5d, which are similar to AND and OR operations in the binary system, respectively. From Figure 5e, the transient responses of NMIN and NMAX are shown under variation of applied input voltages. The versatility described definitely demonstrates the great potential of our proposed RTA strategy for future device applications based on 2D vdW heterostructures.

2. Conclusion

In summary, we used a simple and effective RTA doping/dedoping strategy under dry-air and vacuum conditions, to realize a tunable and reversible charge-polarity device based on MoTe₂/SnS₂ vdW heterostructures from unipolar, ambipolar to anti-ambipolar behaviors. The core of the doping/de-doping reversibility is responsible for the adsorption/desorption processes of O₂ molecules onto the surface of MoTe₂. Using the MoTe₂/SnS₂ vdW heterostructures, flexible multiplexing operations, such as inverter, OPC amplifier, p-n diode, and ternary-state logic (NMIN and NMAX gates) were achieved, which provides a new doping strategy for layered electronics before integrated-circuit packaging. Our work definitely demonstrates the potential for use in next-generation electronics and will transcend the limits of Moore’s law.

3. Experimental Section

Device Fabrication: MoTe₂/SnS₂ vdW heterostructure transistors were fabricated by the dry-transfer method. First, thin flakes of SnS₂ were
mechanically exfoliated from bulk SnS$_2$ crystals onto a 300 nm thick SiO$_2$ dielectric/Si substrate, while MoTe$_2$ flakes were exfoliated from the bulk form onto a PDMS film (Gel-Pak, PF-40-X4). The PDMS film attaching the exfoliated MoTe$_2$ flakes was positioned on the arm of a micromanipulator and precisely transferred onto the top of the selected SnS$_2$ flake. Subsequently, several pairs of contact electrodes were defined via conventional electron-beam lithography. Ti/Au (20/60 nm) metal layers were then deposited at a base pressure of $2 \times 10^{-6}$ torr, followed by a lift-off approach in acetone to complete the device fabrication.

**Characterization:** The morphology and thickness of the MoTe$_2$/SnS$_2$ vdW heterostructure were investigated using OM and AFM. Raman spectra were collected on a LabRam HR-800 Raman spectrometer (Jobin

Figure 5. a) Transfer characteristics and voltage gains for an inverter operation, integrated by a unipolar MoTe$_2$/SnS$_2$ vdW heterostructure connected to a load resistor ($1 \, \Omega$). b) Oscillating signals of i) the common-drain and ii) the common-source mode measured at the output of an ambipolar MoTe$_2$/SnS$_2$ vdW heterostructure connected to a load resistor. c) Output characteristics of diode operation at $V_g = -60 \, V$ in an anti-ambipolar MoTe$_2$/SnS$_2$ vdW heterostructure. The inset shows the features of a half-wave rectifier. ii) Equivalent circuit for the ternary inverter and the corresponding OM image based on an anti-ambipolar MoTe$_2$/SnS$_2$ vdW heterostructure connected to a MoTe$_2$ transistor. iii) Transfer characteristics and voltage gains for the ternary inverter operation. d) Equivalent circuits and truth tables of NMIN and NMAX logic gates. e) Output voltages of NMIN and NMAX logic gates under applied input voltages ($V_A$ and $V_B$).
Yvon), with a laser wavelength of 532 nm. Electrical measurements were performed under vacuum (<10⁻⁵ torr) in a cryogenic probe station (Lakeshore TTPX) with an Agilent B1500A semiconductor parameter analyzer.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements
C.-F.C. and S.-H.Y. contributed equally to this work. This work was supported by the Taiwan Ministry of Science and Technology (Grant Nos. MOST 109-2112-M-005-033-MY3 and 110-2119-M-007-003-MBK). C.-F.C. and S.-T.L. acknowledge additional support from the Young Scholar Fellowship Program by the Ministry of Science and Technology (Grant No. MOST 110-2636-M-009-009) and the Center for Emergent Functional Matter Science of National Yang Ming Chiao Tung University. T. Taniguchi acknowledges financial support from the “Center for Semiconductor Technology Research of National Yang Ming Chiao Tung University” from The Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the MOE in Taiwan. W.-W.W. acknowledges the support from the “Center for Semiconductor Technology Research of National Yang Ming Chiao Tung University” from The Featured Areas Research Center Program within the framework of the Higher Education Sprout Project by the MOE in Taiwan. This work was also supported in part by the Taiwan Ministry of Science and Technology (Grant No. MOST 109-2634-F-009-027), the Natural Science Foundation of Shanghai (Grant No. 19ZB1473400), the NSAF Foundation of China (Grant No. U1830130), and the Young Scientist Project of MOE Innovation Platform, China.

Conflict of Interest
The authors declare no conflict of interest.

Data Availability Statement
Research data are not shared.

Keywords
charge-polarity control, MoTe₂, multioperation-mode transistors, SnS₂, van der Waals heterostructures

Received: December 27, 2021
Revised: April 29, 2022
Published online: July 13, 2022

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