Variable frequency finite control set model predictive control of boost converter

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Abstract: Finite control set model predictive control (MPC) is one of the popular techniques for the control of power electronic converters. In this paper we explore the effect of sampling frequency in FCS-MPC of non-minimum phase converters. Usually a higher sampling frequency is linked to an improved performance. However, due to finite duration of prediction horizon in MPC and its dependence on sampling frequency we have observed that reducing the sampling frequency could improve the performance in terms of transients, efficiency and computational complexity. Based on these observations a variable frequency control scheme has also been proposed.

Keywords: power electronics, DC-DC power converters, predictive control

Classification: Power devices and circuits

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1 Introduction

Finite control set model predictive control (MPC) is one of the emerging techniques used for the control of power electronic converters [1, 2, 3, 4]. Most of the control schemes calculate the duty ratio of the switching waveform by utilizing the averaged converter model, which could lead to inaccuracies [4]. Whereas, FCS-MPC has the ability to explicitly handle the discrete nature of semiconductor switches that can be either on or off. Therefore, the control action computed in FCS-MPC can be directly applied to the converter without the need of a demodulator [4].

In FCS-MPC an optimization problem is solved online at each sampling instant [1, 5]. Online optimization is computational intensive that could limit the real-time implementation of FCS-MPC [6]. The real-time requirements are vital due to the high switching frequencies employed in power electronic converters. Several techniques have been proposed in the literature to reduce the computational requirements of FCS-MPC. Some of them include reducing the prediction or control horizon, move blocking, sphere decoding, etc [1, 3, 7, 8, 9]. The computational complexity of MPC grows exponentially with the number of steps in the prediction horizon [1]. Therefore, reducing the number of steps in the prediction horizon is usually an obvious choice to reduce the computations. However, it could lead to degraded performance or even instability, especially in the case of non-minimum phase systems [1, 4].

Another parameter which affects the computational requirements is the sampling frequency. A reduced sampling frequency will result in reduced average computational requirements. On the other hand, reducing the sampling frequency in converters could increase the ripple in the output of the converter. There is also another implication of reducing the sampling frequency in FCS-MPC which is usually not considered. Reducing the sampling frequency (increasing the sampling time) will increase the total duration of the prediction horizon, if the number of prediction steps are kept constant. An increased duration of prediction horizon could lead to improved performance, especially in the case of non-minimum phase systems [1, 4]. Therefore, the affect of reducing the sampling frequency on converter performance is not straight forward. It may result in improved performance due to longer horizon or degraded performance due to larger ripple.

In this paper we analyze the performance of boost converter, which exhibits a non-minimum phase behavior [4], over a range of sampling frequencies. Based on the findings, we have also proposed a variable frequency FCS-MPC and compared
the results with fixed frequency FCS-MPC. Results shows improved transient response with reduced computations.

2 Finite control set model predictive control

In this paper we will use the discrete-time model of the dc-dc boost converter and the FCS-MPC technique that is given in [4]. The objective function in the FCS-MPC problem formulation is given by the following equation.

$$J = \sum_{l=k}^{k+N-1} (|v_{error}(l+1[k])| + \lambda|\Delta u(l[k])|)$$  \hspace{1cm} (1)

where $N$ is the number of steps in the prediction horizon, $v_{error}(l + 1[k])$ is the difference in the predicted output voltage at time index $l + 1$ and its reference, $k$ indicates the current time index at which the prediction is being made, $\Delta u(l[k]) = u(l[k]) - u(l-1[k])$ is the change in predicted input at time index $l$, $u(l,k) \in \{0,1\}$ is the input at time instant $l$, and $\lambda \in (0, \infty)$ is a weighting factor [10]. The cost $J$ has two terms. The first term penalizes the error in the output voltage that has to be regulated. The second term penalizes the change in the input that indicates semiconductor switch transition. It is penalized because switch transition contributes to power loss in power electronic converters. In FCS-MPC, the optimal input is calculated by minimizing the cost Eq. (1) with respect to the input sequence $U(k) = [u(k|k)u(k+1|k)\ldots u(k+N-1,k)]$. The same procedure is repeated at each sampling instant.

3 Analysis of fcs-mpc of boost converter with respect to sampling frequency

In this section, we will use simulation results to analyze the performance of FCS-MPC with different sampling frequencies. The start-up of boost converter is simulated and the performance is evaluated in terms of output voltage regulation, control effort, and average computational complexity. For the evaluation of output voltage regulation during transients, we define the following metric:

$$m_{trans} = \sum_{k=0}^{N_t} |v_{error}(k)|,$$  \hspace{1cm} (2)

where $N_t$ is the number of samples until the output voltage has settled within $\pm 10\%$ of the reference voltage. A similar metric for the evaluation of steady state voltage regulation can be introduced. However, we will utilize the voltage ripple, which is widely used in power electronics. For the control effort the following metric is defined:

$$m_u = \sum_{k=0}^{N_u} |\Delta u(k)|,$$  \hspace{1cm} (3)

where $N_u$ is the total number of samples in the simulation. In power converters the change in input contributes to power loss and efficiency. Finally, the metric used for computational complexity is $m_{comp} = N_s$.

The boost converter is simulated for start-up with FCS-MPC at different frequencies. We have kept the switching period of the converter to be equal to...
the sampling time. Circuit parameters used for simulation are: inductor $L = 300 \, \mu H$, capacitor $C = 470 \, \mu F$, input voltage $v_i = 10 \, V$, load resistance $R = 42 \, \Omega$, and inductor resistance $R_l = 0.3 \, \Omega$. Output voltage reference is $v_{ref} = 15 \, V$. Total duration of the simulation is 30 ms. The total number of prediction steps $N = 8$. A move blocking scheme [4, 8] is used with number of fine samples $N_f = 6$ and number of coarse sample $N_c = 2$. The sampling time of fine samples and course samples is $T_s = 1/f_s$ and $4T_s$, respectively. The total duration of the prediction horizon is $(N_f + 4N_c)T_s$. The performance metrics for different frequencies are shown in Fig. 1.

In Fig. 1, it can be observed that as expected the ripple magnitude is increased with the reduction in sampling frequency. All the other three performance metrics are improved with the decrease in sampling frequency. Reduction in $f_s$ improves the transient metric due to the fact that a lower $f_s$ increases the total prediction horizon. Boost converter is non-minimum phase system. A longer prediction horizon is known to improve the performance of non-minimum phase systems [4]. Reduction in $f_s$ also improves the control effort metric as the input is changed less often. Lastly the computational complexity metric is directly the inverse of $f_s$.

While the results in this section are based on simulation with specific values, they do give us insight that is valid for boost converter, or non-minimum phase converters, in general.

4 Proposed control technique

In the previous section we observed that the best steady state performance, i.e. the lowest ripple, is at a sampling frequency of around 100 kHz. Whereas, we have the best transient performance at a sampling frequency of around 20 kHz.

Based on the this observation, we propose to use a combination of these frequencies depending on the state of the boost converter. If the converter output voltage is not within $\pm 10\%$ of the reference voltage, then $f_{s,low} = 20 \, kHz$ will be used as the sampling frequency. If the converter remains within $\pm 10\%$ of the reference voltage for at least the duration $T_{net}$, then the sampling frequency will be changed to $f_{s,high} = 100 \, kHz$. Here $T_{set}$ helps to avoid rapid changes in $f_s$. It may be kept equal to $N/f_{s,low}$. We call this proposed control scheme “variable frequency FCS-MPC”. A flowchart of the variable frequency FCS-MPC is shown in Fig. 2.

![Fig. 1. Performance metrics for different sampling frequencies (a) ripple (b) computations metric (c) transient metric (d) control effort metric](image-url)
5 Simulation results for the proposed controller

In this section we compare the proposed technique variable frequency FCS-MPC with fixed frequency FCS-MPC at 100 KHz and 20 KHz. The converter was simulated with the parameters stated earlier. At start-up the voltage reference is 15 V. The voltage reference is changed to 18 V and 15 V at time $t = 5$ ms and $t = 10$ ms, respectively. The simulation results are shown in Fig. 3. The metrics are given in Table I. Besides the ripple, all the other metrics are normalized with the largest value.

As can be seen in Fig. 3, the proposed variable frequency scheme has an improved transient performance than 100 KHz fixed frequency FCS-MPC. It can also be observed in Table I that the proposed variable frequency FCS-MPC has equivalent or better metrics as compared to fixed frequency FCS-MPC at 100 KHz. Whereas, in comparison to the fixed frequency FCS-MPC at 20 KHz, the proposed scheme has a lower ripple as can be seen from the zoomed version of the output voltage in Fig. 3.

![Control algorithm](image)

**Fig. 2.** Control algorithm

![Simulation results](image)

**Fig. 3.** Simulation results (a) 100 KHz fixed freq. FCS-MPC (b) 20 KHz fixed freq. FCS-MPC (c) proposed variable sampling freq. FCS-MPC
Fig. 4(a) show the simulation results of proposed control scheme for change in load. At 10 ms load resistance $R_l$ is decreased from 42 $\Omega$ to 15 $\Omega$. Kalman filter adjusts the voltage reference without any steady state error [4]. The output voltage remains 15 V as can be seen in Fig. 4(a). Fig. 4(b) show the simulation results of proposed control scheme for change in input voltage, which is increased from 10 V to 12 V at $t = 10$ ms. The output voltage remains same without any overshoot.

### Table I. Comparison of fixed and variable sampling time

|                     | $f_s = 100$ kHz | $f_s = 20$ kHz | Var. $f_s$ |
|---------------------|-----------------|----------------|------------|
| ripple at 15 V      | 0.056 V         | 0.156 V        | 0.056 V    |
| ripple at 18 V      | 0.060 V         | 0.281 V        | 0.060 V    |
| $m_{trans}$ (start-up) | 1.000         | 0.786          | 0.786      |
| $m_{trans}$ (step-up)| 1.000          | 0.212          | 0.212      |
| $m_{trans}$ (step-down) | 1.000         | 1.000          | 1.000      |
| $m_a$ (total simulation) | 1.000          | 0.424          | 0.720      |
| $m_{comp}$ (total sim.) | 1.000          | 0.200          | 0.799      |

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### 6 Conclusion

The effect of sampling frequency in FCS-MPC of non-minimum phase power converters has been explored. Although reducing the sampling frequency increases the ripple, it increases the total duration of the horizon thereby improving the transient behavior. A reduced sampling frequency also improves the computational metric and input metric. Based on this observation we have also proposed a variable frequency FCS-MPC scheme, which is equivalent or better in term of all metrics as compared to a fixed frequency scheme.