Quantitative Evaluation of Hardware Binary Stochastic Neurons

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Recently there has been increasing activity to build dedicated Ising Machines to accelerate the solution of combinatorial optimization problems by expressing these problems as a ground-state search of the Ising model. A common theme of such Ising Machines is to tailor the physics of underlying hardware to the mathematics of the Ising model to improve some aspect of performance that is measured in speed to solution, energy consumption per solution or area footprint of the adopted hardware. One such approach to build an Ising spin, or a binary stochastic neuron (BSN), is a compact mixed-signal unit based on a low-barrier nanomagnet based design that uses a single magnetic tunnel junction (MTJ) and three transistors (3T-1MTJ) where the MTJ functions as a stochastic resistor (ISR). Such a compact unit can drastically reduce the area footprint of BSNs while promising massive scalability by leveraging the existing Magnetic RAM (MRAM) technology that has integrated 1T-1MTJ cells in ~ Gbit densities. The 3T-1SR design however can be realized using different materials or devices that provide naturally fluctuating resistances. Extending previous work, we evaluate hardware BSNs from this general perspective by classifying necessary and sufficient conditions to design a fast and energy-efficient BSN that can be used in scaled Ising Machine implementations. We connect our device analysis to systems-level metrics by emphasizing hardware-independent figures-of-merit such as flips per second and dissipated energy per random bit that can be used to classify any Ising Machine.

I. INTRODUCTION

In the era of internet of things (IoT), combinatorial optimization problems are ubiquitous. In fact, most of the real-problems that quantum computers are aiming to solve can be formulated as combinatorial optimization problems. From directing traffic flows to routing interconnections in integrated circuit design[5,30], to making financial decisions[5,31,32], drug discoveries[5,33] etc.- all involve solving a form of combinatorial optimization problems. The demand for solving these problems faster and more efficiently is ever-increasing. But such problems typically fall into the category of NP-hard or NP-complete class in complexity theory[2,5] with no known polynomial time solution, making them notoriously difficult to solve in digital computers using traditional computing methods. This has given rise to a new paradigm in computing, namely Ising computing. Ising computing maps combinatorial optimization problems to an Ising model, and solves it by searching for the ground state of the system described by[5,9,15,16]:

\[
E = -I_0 \left( \frac{1}{2} \sum_{i,j=1}^{N} J_{ij} m_i m_j + \sum_{i=1}^{N} h_i m_i \right)
\]  

(1)

where, \( m \) denotes the Ising spin, \( J \) is the coupling co-efficient, \( h \) is the external bias, and \( I_0 \) is the annealing parameter which is proportional to the inverse of temperature. In the machine learning field, the same underlying principle is used for Boltzmann Machines with the annealing parameter being 1. The binary stochastic neurons (BSNs)[35] of stochastic neural networks are well suited to function as a 'spin' in such systems, described mathematically by:

\[
m_i = \text{sgn}[\tanh(I_i) - r_i]
\]

(2)

where \( r_i \) is a random number between +1 and -1, and \( I_i = -\frac{\partial E}{\partial m_i} \) is the input to the neuron.

FIG. 1. 1MTJ-3T compact BSN hardware which utilizes the natural physics of low-barrier nanomagnets holds the promise to accelerate the simulated annealing processors (a) Shows the underlying working principle of Ising Machines. (b) Shows an implementation scheme utilizing MTJ and memristive crossbar arrays, where the BSN is the Ising spin \( m_i \), memristors (\( R_{ij} \)) implement the weight and bias co-efficients, and the feedback resistor \( R \) can control the annealing temperature electrically.

Given the importance of optimization problems, a lot of
research has gone into developing algorithms and identifying appropriate hardware for Ising computing. Various approaches including quantum computers based on quantum annealing (QA) or adiabatic quantum optimization (AQC) implemented with superconducting circuits, coherent Ising machines (CIMs) implemented with laser pulses, phase-change oscillators, or CMOS oscillators and digital annealers based on simulated annealing (SA) implemented with digital circuits are being explored.

In this paper we comprehensively evaluate and characterize a stochastic magnetic tunnel junction (sMTJ) based realization of the Ising spin (eqn[1] where random numbers are generated using the natural physics of low barrier nanomagnets in a compact design. A network of these BSN units can be coupled with a memristive crossbar array to perform the synaptic operation as shown in Fig.1 can drastically improve the area requirements and accelerate computation speed of Ising Machines. We evaluate the performance of the BSN device in terms of its energy and delay metrics and connect these to the problem and substrate-independent metric of flips per second that the probabilistic system makes.

Our evaluation of 1MTJ-3T BSN design considers different types of low-barrier nanomagnet realizations of MTJs. As the MTJ essentially functions as a two-terminal stochastic resistor (SR), we first take a general 3T-1SR design approach, classifying necessary and sufficient conditions for achieving the BSN operation for different types of SRs in Section III. We relate these conditions to the different sMTJ realizations in Section II. We report the timescale of operation, power and energy for each case based on benchmarked SPICE simulations of the BSN hardware consisting of spintronic elements from a modular circuit framework coupled to 14 nm FinFET PTM models, and provide analytical results for relevant quantities in Section IV. Lastly, we use these device performance metrics to project onto hardware performance figures of merit such as flips per second that a probabilistic sampler makes. Our projections indicate orders of magnitude improvement potential over current digital implementations.

II. GENERAL APPROACH TO DESIGN OF BSN

Binary stochastic neurons (BSNs) are well suited to function as a ‘spin’ in Ising machines for solving combinatorial optimization problems. A compact and efficient hardware realization of the BSN leveraging the natural physics of stochastic nanomagnets can be made by using unstable magnetic tunnel junctions (MTJs) as shown in Fig.1.

The compact design of BSN based on low-barrier magnet (LBM) stochastic MTJs (sMTJs) was first proposed in 2017. Using magnet and circuit physics to analyze the performance, it was reported that using an LBM in a circular disk geometry with energy barriers below kT as the free layer of an MTJ results in sub-ns response times requiring only a few fJ of energy per random bit. The proposed design and the performance analysis considers a very specific type of sMTJ which had circular in-plane magnetic anisotropy (IMA) whose fluctuations are undisturbed by the current in the circuit for typical current drive conditions. However, in 2019, a version of the BSN design that was implemented in hardware to solve an 8-bit factorization problem consisted of an sMTJ with perpendicular anisotropy (PMA) and a barrier of a few kT as its free layer. Unlike the circular in-plane design, the PMA design relied on its resistance being tunable by the spin-transfer-torque effect in order to achieve the BSN operation. This has called for an extension of our initial analysis presented in which we systematically perform in this paper.

As the MTJs in the BSN circuit effectively act as a fluctuating resistor, and the design principle is independent of this realization, for establishing the fundamental design rules we approach it from a general perspective and we hope these design rules stimulate discussion in the realization of different stochastic resistors that use different mechanisms.

A. Types of fluctuating resistances

We categorize the fluctuating $R$ into four types. First, based on the fluctuating nature it can be continuous or bipolar (telegraphic). Second, it can be tunable or non-tunable depending on whether it is affected by the current that is flowing through it.

![FIG. 2. Categorizing Resistances: (a) Fluctuation Nature: they can be continuous or bipolar. The time dynamics and distribution are shown for each category. (b) Current-Tunability: The fluctuations could be unaffected by $I$ or it could be a function of $I$ as indicated by their transfer characteristics. $I_{0}$ is the current at the 50:50 point where the resistance spends equal time in $R_P$ and $R_{AP}$ states. $I_{0}$ is the biasing current defined as the slope of the $(R \times I)$ curve at 50:50 point. The pinning current is typically $\sim 3 – 5 I_{0}$.]

A continuous resistor can have its resistance being any value between $[R_P \rightarrow R_{AP}]$ while a bipolar resistor only assumes the two values $R_P$ and $R_{AP}$ as shown in Fig.2(a). The distribution of continuous resistances can be of different types as well. It can be uniform or follow slightly bimodal distribution in the case of an MTJ as shown in the figure. Different distributions typically result in different average $R$ values,
FIG. 3. **Transfer Characteristics**: The BSN circuit is realized by coupling the fluctuating resistor which is the physical realization of the random variable \( r_i \) in the BSN equation to an NMOS which provides the tunability, and then to an inverter which thresholds the output. The four types of resistances are coupled to a 14 nm FinFET and the resistance parameters (based on experimental demonstrations of MTJs) are chosen to match the transistor characteristics. All resistance types except for the bipolar non-tunable were able to achieve BSN operation following eq. 2. To function as a BSN the bipolar resistances need some means of tuning their probability distribution.

![Image of BSN circuit](image-url)

Specifications:

| Resistance Type | Symbol | Value |
|-----------------|--------|-------|
| NTC | \( R_{ntc} \) | 17 kΩ |
| | \( R_{ap} \) | 35 kΩ |
| | \( n \) | 2 |
| | \( I_0 \) | 1 μA |
| | \( I_{50} \) | 15 μA |
| | \( V_{DD} \) | 0.8 V |
| | \( V_{OUT} \) | 15 μA |

FIG. 4. **Non-tunable Continuous vs Bipolar Resistance**: (a) Transfer Characteristics shows that while the continuous resistor results in a sigmoidal output, the bipolar gives a stair-case like function. (b) The bipolar R is unable to follow the Boltzmann distribution of the invertible AND gate (description in ref. [29]). All states remain equally probable.

![Image of BSN circuit](image-url)

B. **Performing the BSN function**

We first take a look at the transfer characteristics of the device to see whether the four types of resistance can faithfully mimic BSN operation described by eqn [2]. The fluctuating \( R \) is a physical realization of the random variable \( r_i \), the NMOS acts as a constant current source that provides tunability, and the inverter performs the \( \text{sgn} \) operation in eqn [2].

Mathematically, when the resistance is bipolar, it means \( r_i \) slightly bimodal or uniform distributions are better suited than Gaussian distributions for BSN realizations.

The current \( I \) flowing in the circuit can tune the probability distribution of the resistance fluctuations, and we call such resistors tunable resistors. When designing a BSN with current tunable R, we need to know the current where fluctuations are equal between the two extreme states (\( I_{50} \)) and the current required to pin the resistance to one of those states. An important parameter in this case is the bias current \( I_0 \), which is the slope of the R vs I curve at the 50-50 point. Typically, \( \sim 3 \)–\( 5 \) \( I_0 \) current is required to pin the fluctuating resistance to one of its states. We will later provide analytical expressions for \( I_0 \) for four cases of resistors that can be obtained by various MTJs (Fig. 9).

Based on this analysis, we categorize the fluctuating resistance into four types: Non-tunable continuous (NTC), Non-tunable bipolar (NTB), tunable continuous (TC) and tunable bipolar (TB).
is $\pm 1$. So, for any input $I$, where $|\tanh(I)| < 1$, the output $\langle m \rangle$ is equal to zero. In Fig. 3(b), if we look at a simple invertible AND gate operation, it is seen that devices with stair-case like function like this are not suitable for performing as BSNs. This has been demonstrated experimentally in ref. [25], where a stable MTJ was used as a bipolar resistor whose distribution was tuned by an external field. However, this issue could be resolved by introducing external/additional control parameters like external field as shown in the same experiment.

C. Parameter Dependence and Design Choices

Fig. 3 is created with a fixed set of parameters for the resistor and coupled with a specific transistor technology, 14 nm FinFET models. In this section we explore how the transfer characteristics are affected by different parameters of the resistors and FET characteristics and how to choose the right combination of $R$ and FET to be coupled.

**Stochastic Region:** The stochastic region, which we define next, is a function of the resistance ratio $n$ for non-tunable resistors and biasing current $I_p$ for tunable resistors as shown in Fig. 5, that needs to be matched with the transistor characteristics.

**Effect of $n$:** The resistance ratio $n = R_P/R_{AP}$ is directly related to the stochastic region $\Delta v$ through the NMOS characteristics in case of non-tunable resistor designs. The edge of the stochastic region $v^\pm$ is defined by when $V_{IN} = V_{DD}/2 - |I^+R_P, I^-R_{AP}| \approx 0$ where the current $I^\pm$ is determined by the NMOS as shown in Fig. 6(c). For a desired $\Delta v = v^+ - v^-$ (stochastic region) and NMOS transistor, the required $n = R_{AP}/R_P$ should approximately equal $I^+/I^-$. Ideally, the minimum value of the resistance should be $R_P = (V_{DD}/2)/I^+$ and to get full pinning, $\Delta v$ should be less than $V_{DD}$. For a 14 nm FinFET, to get a stochastic region of $\Delta v = 50 – 200\text{mV}$, the resistance ratio $n$ should be around $2 – 50$. The resistance ratio $n$ is a measure for tunneling magneto-resistance, $\text{TMR} = (n - 1) \times 100\%$ in case of MTJs. For the non-tunable case, TMR needs to be large enough to provide a voltage swing large enough to overcome the noise margins of the inverter and it should be small enough so that output pinning is achieved within the given input range. Typically MTJs have TMRs ranging from $100 – 300\%$ with a maximum reported TMR of $604\%$[51], so the resistance ratio of MTJs is well within the desired range, but the general requirements we outline should be applicable for other types of stochastic resistors as well.

**Effect of $I_p$:** In case of tunable resistances, the stochastic region is independent of the resistance ratio and depends on the pinning current and thus the bias current ($I^+_P \propto I_0$) instead as shown in Fig. 6(d). For large bias currents ($I_0 \gg I$), the tunable resistances act essentially like non-tunable resistances. To get the full range of $R$, the NMOS needs to be able to supply the pinning current. If the pinning current is $(3 - 5)I_0$ as shown in Fig. 3 then to get the full range of the resistance $I^+_{\text{max}}$ needs to be around $(6 - 10)I_0$. In case of 14 nm FinFETs, $I^+_{\text{max}}$ is around $\sim 40 \mu\text{A}$, restricting $I_0$ to values less than $7 \mu\text{A}$.

**Choice of $I_{SG}$:** Another parameter that is important for the
operation of tunable resistors is the \( I_{SO} \) which determines the midpoint of the sigmoid. \( I_{SO} \) is the current at which the resistance on average spends equal time in \( R_P \) and \( R_{AP} \) states. As the circuit can only support positive current values, it needs to be a positive quantity and preferably matched with the saturation point (\( V_{DS} = V_{CS} \)) current \( I_{DSat} \) of the NMOS transistor. Changing \( I_{SO} \) shifts the transfer characteristics laterally as shown in Fig. 7(a).

![Graph](image)

**FIG. 7.** (a) **Choice of \( I_{SO} \):** \( I_{SO} \) is ideally a positive quantity matched with the \( I_{DSat} \) of the transistor, changing \( I_{SO} \) results in a lateral shift of the sigmoid. (b) **R vs I relationship:** The output characteristics also depend on the nature of the resistance tunability with the circuit current \( I \). If \( R \) decreases with \( I \) (\( R_{AP} \to R_P \)), the opposing characteristics of the transistor current and resistance change result in a non-monotonic output.

**R vs I:** One last requirement is that, for current tunable resistance with increasing current \( I \), the resistance needs to increase from \( R_P \) to \( R_{AP} \). This can be understood intuitively: Increasing \( I \) means the NMOS transistor is becoming more conductive. If the MTJ concomitantly becomes more conductive as \( I \) is increasing, the transfer characteristics can show non-monotonic behavior as shown in Fig. 7(b). This requirement holds true irrespective of whether the circuit’s \( R \) branch consists of a PMOS-1R or 1R-NMOS topology.

### III. REALIZATION OF FLUCTUATING RESISTANCES WITH SMTJS

A magnetic-tunnel-junction (MTJ) whose free layer is a low-barrier magnet (LBM) could serve as a physical realization of fluctuating resistors. Depending on the nature and characteristics of the LBM magnetization fluctuations, we can get different types of \( R \). Our previous analysis\(\textsuperscript{[35]}\) was restricted to one type of LBM, the circular IMA with barrier \(< k_BT \), in this section we extend it to include all possible LBMs.

A general description of the energy associated with a magnet is given by\(\textsuperscript{[35]}\)

\[
E = \frac{1}{2} H_{k_P} M_s \Omega (1 - m_z^2) + \frac{1}{2} H_{k_i} M_s \Omega (1 - m_z^2) - H_{ext} M_s \Omega \cdot \hat{n}
\]  

where, \( H_{k_P} = 2K_s / t - 4\pi M_s \) is the perpendicular anisotropy field along the x-axis, \( K_s \) is the surface anisotropy density, \( H_{k_i} \) is the in-plane anisotropy along z-axis, \( H_{ext} \) is the external field, \( M_s \) is the saturation magnetization and \( \Omega = \pi (D / 2)^2 \) is the volume of the magnet. By adjusting the thickness or the shape of the magnet, the magnetic anisotropy of the magnet can be scaled to behave like a low-barrier magnet.\(\textsuperscript{[35]}\) Second order magnetic anisotropy effect and in-plane components of demagnetization fields have not been considered here and left for future investigation since the macroscopic models without it seems to be reasonably consistent with recent experimental results involving low barrier magnets.\(\textsuperscript{[39, 55]}\) We use the stochastic LLG module from our spintronics library\(\textsuperscript{[35]}\) to simulate the LBM dynamics in HSPICE using its transient noise function. This model has been carefully benchmarked against general Fokker-Planck based methods\(\textsuperscript{[40]}\).

**FIG. 8. Low-barrier magnet fluctuation dynamics:** We use the benchmarked stochastic LLG module to simulate LBM dynamics. The saturation magnetization is considered to be \( M_s = 1000 \text{ emu/cc} \), \( \Omega = 6.3 \times 10^{-19} \text{ cc} \), and \( H_k \) adjusted to get the indicated \( \Delta \). Each simulation is carried out with time-step at least \( \times 100 \) smaller for a time-duration \( \times 1000 \) than characteristic timescales to avoid any simulation time dependencies, the exact parameters are indicated.

\( \Delta < k_BT \) magnets have more continuous fluctuations with (b) having a more uniform distribution than (a) while slightly higher barrier magnets have a more telegraphic fluctuation. In both cases, the presence of high demagnetization fields cause faster fluctuations in IMA magnets.

**LBM Magnet Fluctuation Dynamics:** By low-barrier magnet we refer to magnets whose barrier is \(< 10k_BT \) or so, whose magnetization fluctuates randomly in the presence of thermal noise. Interestingly, the magnetization dynamics of low-barrier magnets with barrier \(< k_BT \) are different from those with a slightly higher barrier.\(\textsuperscript{[35]}\) The simple exponential dependence of retention time of the magnetization state on the barrier height is not valid around or below \( k_BT \).
| R Type          | MTJ Free Layer                     | $\tau_{\text{CORR}}$       | $I_0$       | $I_{50}$     | $H_0$   |
|----------------|------------------------------------|-----------------------------|-------------|-------------|---------|
| Non-tunable    | $\Delta < k_B T$ Circular IMA      | $\sqrt{\ln(2)} \frac{1}{\gamma} \sqrt{\frac{M_s \Omega}{H_k k_B T}}$ (sub-ns) | $2q \frac{\gamma}{h} \sqrt{\frac{2}{\pi}} \frac{H_k M_s k_B T}{H_k M_s k_B T}$ (0.1–1mA) | (n/a)   | $2k_B T M_s \Omega$ |
| Continuous     | Isotropic ‘PMA’                    | $\ln(2) \frac{1}{\gamma} \frac{M_s \Omega}{H_k k_B T}$ | $6q \frac{\gamma}{h} a k_B T$ (0.4–4μA) | $4qa \left( \frac{1}{2} H_k M_s \Omega \right)$ | $3k_B T M_s \Omega$ |
| Non-tunable    | $2k_B T < \Delta < 10k_B T$ IMA    | $\propto \frac{e^{\Delta/k_B T}}{(1 + H_k / 2H_s)}$ | $\frac{4q}{h} \frac{\Delta}{1 + (1 + (H_k / 2H_s))}$ (0.05–25μA) | (n/a)   | $10 k_B T M_s \Omega$ |
| Bipolar        | $2k_B T < \Delta < 10k_B T$ PMA    | $\propto e^\Delta/k_B T$ | $\frac{4q}{h} \Delta$ (0.5–25μA) | $\frac{4q}{h} \frac{1}{2} H_k M_s \Omega$ | $10 k_B T M_s \Omega$ |

FIG. 9. MTJ Free layer and its corresponding R type along with corresponding characteristic parameters and their analytical expression. The numbers in bracket indicates an approximate range of values for each parameter. The proportionality constant for correlation time of magnets with $\Delta > k_B T$ is $\tau_0 \sim 0.1 - 1$ ns, exact equation can be found in \cite{61}.

Current Response of LBM Magnets: Magnetic fluctuations can be tuned by spin-current. For high barrier magnets, the minimum current required to switch the magnetization is called the critical current $I_0$ which can arise in a fixed, stable layer that acts as a reference to the free layer in the MTJ. In case of high-barrier magnets, the spin-current induced magnetic switching hysteresis loop just shifts in case of PMA magnets depending on the direction of field, but for IMA magnets the shape of the hysteresis and magnet dynamics is changed $\cite{62}$. The large demagnetization field present perpendicular to the magnetization plane in IMA magnets causes the magnetization to precess around it when spin-current is applied in the opposite direction to the external field. The same is observed in low-barrier magnets as shown in Fig. 10. The larger the external field the more pronounced the effect is. The uniform precessional motion kicks in at high-field, when the current is close to the biasing current or higher applied in the opposite direction to the field. Very recently, this has been observed experimentally for low fields $\cite{62}$. While this is an undesired effect in case of our BSN operation, this can be useful in context to oscillator based network $\cite{63}$. This has important implications in terms of acting as a fluctuating resistance in a BSN circuit. IMA magnets with external fields (i.e. uncompensated dipolar fields in MTJ $\cite{64}$; greater than its pinning field is not suited to function as a tunable or non-tunable resistor. IMA magnets with continuous magnetization coupled to a transistor with small saturation current (tens of $\mu A$) compared to the biasing current of IMA (hundreds of $\mu A$) can work as non-tunable resistors, and as experimental observations in ref. $\cite{64}$ suggest, it can withstand small (compared to its pinning field) stray fields. PMA magnet MTJs with their small biasing current ($\sim$ few to few tens of $\mu A$) when coupled to typical transistors act as tunable resistors in BSN circuit. In this case the external bias field is actually preferred, since this enables positive $I_{50}$.
current\textsuperscript{23}. So, if we coupled an MTJ with a 14 nm FinFET (V\textsubscript{DD} = 0.8 and I\textsubscript{Dsat} = 15\,\mu A\textsuperscript{31}) the table in Fig. 9 summarizes the resistance mapping and the associated parameters.

IV. PERFORMANCE EVALUATION OF MTJ BASED BSN

In the final section we compare the physical performance of these different sMTJs in a BSN.

Timescale of Operation: The two relevant timescales of operation for a BSN are, the correlation time $\tau_C$ which is the average time it takes to produce a new output at given input and the response time $\tau_N$ which is defined as the average time it takes for the circuit to give a random output with correct statistics as the input is changed\textsuperscript{32}. Fig. 11 shows the two timescales for the three types of fluctuating resistances for MTJs with two different timescales. For simplicity we assumed the correlation time to be same for all types of magnets, but in reality they would follow the $\tau_{CORR}$ relations indicated in Fig. 6\textsuperscript{33,35}.

![FIG. 11. Timescales of Operation](image)

FIG. 11. Timescales of Operation for each resistor type for two fluctuation times $\tau_C \sim [160\,\text{ps}, 320\,\text{ps}]$ are shown. The resistances are engineered to have similar characteristic timescales but different fluctuation behavior (tunable, non-tunable and continuous and bipolar fluctuation) for comparison purposes.

Fig. [11] shows that the response time, $\tau_N$ for non-tunable resistor is independent of the fluctuation time of the resistance, it is rather proportional to the RC delay of the circuit. While for the tunable cases, the response time is related to the characteristic timescales of the resistor. But the time to give new numbers or flip rate $\tau_C$ at $V_N = 0$ is entirely resistance fluctuation time dependent for all cases ($\tau_C \approx \tau_{CORR}$). So for the tunable case, the two said timescales of operation are likely to be similar as they are governed by the magnet fluctuation characteristics while for the non-tunable case, the response time which is RC dependent has the potential to be very short compared to the magnet dependent correlation time. For most applications this difference may not be of importance but for some applications where the network is directed, like Bayesian inference having two different timescales seems to be a requisite\textsuperscript{28}.

Power: Our SPICE simulations indicate that the average power consumed by the BSN circuit in its stochastic region is $\langle P \rangle \approx 2 \times 32\,\mu W$. While the power is almost independent of the TMR, the resistance ratio (n) for a set 50-50 point and technology for the MTJ branch, its joule heating increases with increasing TMR ($\propto \sqrt{n}$) in the positive pinning region as the NMOS resistance reduces. So the lowest TMR that ensures a voltage swing $V_I$ greater than the noise margin of the inverter is considered best suited for BSN operation. The MTJ branch power could be reduced by operating in sub-threshold region $I_{Dsub} \sim 1\,\mu A$, $\langle P \rangle \sim 20\,\mu W$. The 2 is for the two branches, the MTJ branch and the inverter branch. This holds true for all types of resistors. For a 14 nm FinFET with $V_{DD} = 0.8$ and $I_{Dsat} \sim 15\,\mu A$, $\langle P \rangle \sim 20\,\mu W$. While the power is almost independent of the TMR or the resistance ratio (n) for a set 50-50 point and technology for the MTJ branch, its joule heating increases with increasing TMR ($\propto \sqrt{n}$) in the positive pinning region as the NMOS resistance reduces. So the lowest TMR that ensures a voltage swing $V_I$ greater than the noise margin of the inverter is considered best suited for BSN operation.

Energy: As there are two timescales associated with the BSN operation, we can define two energy as well. The energy to produce first random number after the input changes, $E_N \sim \tau_N \langle P \rangle$ and the energy required to produce new random numbers at a given input state, $E_C = \tau_C \langle P \rangle$. Fig. 12(a) shows an energy delay plot indicating the ranges for each type of MTJs. When describing the performance of a hardware BSN, we generally refer to the correlation time $\tau_C$ for delay and $E_C$ for the energy. The individual energy-delay numbers can be used to project performance parameters for processors built with them.

![FIG. 12. (a) Energy-Delay](image)

FIG. 12. (a) Energy-Delay of each type of MTJ based BSN assuming an average power of 20 $\mu W$ and timescales in Fig. 10. (b) Flips per second projections for different number of neurons for each type of MTJs. For these projections only BSN performance numbers are used, synapse would add to the power and thus energy per flip number.

Hardware Projections: Typically the performance of an Ising hardware is measured in terms of time and energy it takes to solve a specific problem. Time to solution depends not only on the physical hardware performance but also on the algorithm that is being implemented. Here, we emphasize measuring the hardware performance in terms of a purely hardware metric flips per second (fps), which refers to the maximum number of spin configurations the hardware can cycle through per second. It depends on the number of spins.
FIG. 13. \textit{flips per second (fps)} is a substrate and algorithm independent performance metric for simulated annealing processors much like the flips per second metric used for general purpose computers. It is a measure of how many flips, and hence spin configurations the system can cycle through in a second. fps can be derived from the reported performance metrics of the processors following ref. 25. The reported and derived quantities as indicated. Current CMOS based annealing processors perform at $\sim 10^{12}$ fps. We project that MTJ based hardware can increase by a few orders of magnitude.

Table: Performance Comparison

| Affiliates | Name                      | Technology          | Latest | Connectivity          | Parallel Neurons, $N_\parallel$ | Clock Frequency, $f$ | Weight Precision |
|------------|---------------------------|----------------------|--------|-----------------------|-------------------------------|----------------------|------------------|
| BIFI       | Janus II annealing machine | FPGA                 | 2014   | Local (5, N-N)        | N=2=1,000                    | 250 MHz              | 1 bit            |
| Hitachi    | Digital Annealer          | 40nm CMOS + FPGA     | 2019   | Local (8, King’s Graph) | N=4+7,500                     | 100 MHz              | 3 bit            |
| Fujitsu    | STATICA                  | 65nm CMOS            | 2018   | All-to-All            | N=512                         | 100 MHz              | 6 bit            |
| Tokyo Tech.| RBM-based                | 65 nm CMOS           | 2020   | All-to-All            | N=150                         | 320 MHz              | 5 bit            |
| UC Berkeley| Purdue-P (ApC)           | FPGA                 | 2020   | Local (5, N-N)        | N=8,100                       | 100 MHz              | 9 bit            |

| Neuron Time (MC step) $\tau = f/\tau$ | $4 \text{ ns}$ | $10 \text{ ns}$ | $10 \text{ ns}$ | $\sim 3 \text{ ns}$ | $14 \text{ ns}$ | $32 \text{ ns}$ |
|--------------------------------------|----------------|----------------|----------------|----------------|----------------|----------------|
| flips per second ($N_\parallel f/\tau$) | $2.5 \times 10^{11}$ | $7.5 \times 10^{11}$ | $10^{9}$ | $\sim 2 \times 10^{11}$ | $10^{10}$ | $\sim 2.5 \times 10^{11}$ |

in the system ($N$) and the time it takes for a spin to flip ($\tau$), $f = N/\tau$.

For the digital annealers the spin update time is usually determined by its clock period ($\tau_{\text{clk}}$) which ranges typically in tens of ns range. To ensure fidelity simultaneous updates of connected spins needs to be avoided\cite{25} forcing digital annealers that operate on clock edge to update spins sequentially. So in a network where all spins are connected effectively only one spin can update per clock cycle\cite{21}. But it need not be if some spins are unconnected (i.e. nearest neighbor\cite{19}, or king-graph\cite{20} connection, or if spins are parallelized by implementing special algorithms\cite{22,23}). Based on the reported total spin number and clock speeds of digital annealing hardware today which have about $\sim 10$K neurons that can update per $\sim 10$ns clock period, we derive an estimation of their performance at $f \sim 10^8/10^{-8} = 10^{12}$ flips per second\cite{12,29} as shown in Fig. 13.

Compared to digital annealers the Ising spin hardware we presented in this work can work autonomously, i.e., without a synchronizing clock or a sequence.\cite{22,55,65} In this mode, the speeds are governed by neuron ($\tau_{\text{neu}}$) and synapse ($\tau_{\text{syn}}$) time only, and to ensure fidelity and avoid simultaneous updates of connected BSNs the synapse needs to update faster than the the neuron ($\tau_{\text{syn}} < \tau_{\text{neu}}$). Sutton et. al.\cite{20} defines a metric $s = \tau_{\text{syn}}/\tau_{\text{neu}}$ and showed that to ensure the fidelity of operations $s$ needs to be less than 1. The exact requirements are problem and architecture dependent. Memristive crossbar arrays paired with a fast summing amplifier synapse could operate very efficiently at as low as few tens of ps speeds\cite{22,55,65,71}.

The digital annealers mimic the Ising spin using a combination of random-number generators (LFSR, Xoshiro, etc.), look-up-tables (LUT) and comparators. The random number generator (RNG) unit is one of the most are expensive elements in the design.\cite{22} Even in the most optimized design, the RNG unit take up $\sim 11\%$ of the total logic gate area.\cite{22} The 3T-1MTJ design offers drastic reduction in the area footprint, promising massive scalability leveraging existing 1T-1MTJ Magnetic RAM technology that already has 1Gbit integrated cells\cite{22,71}.

Fig. 12(b) projects fps number considering $\tau = \tau_{\text{neu}} \approx \tau_{\text{CORR}}$ for different no of spins, N. An MTJ realization with circular IMA, with $\sim$ ns timescale can offer almost two orders of magnitude speedup with $< 10$K neurons. If spins are implemented in Gbit densities all stochastic implementations seem to outperform the CMOS implementations. For such systems the upper bound for N is ultimately determined either by area or by power budget of the chip. Note that the fps number does not reflect the connectivity of the spins or the algorithm implemented by the hardware. It also does not indicate the solution accuracy obtainable for specific problems.\cite{75}

What we highlight here is that using the natural physics of the MTJ we can design a very compact realization of eq. 2 compared to current state of the art CMOS implementations, and despite being a magnetic circuit, low barrier magnet implementations even offer an overall speed up due to their fast fluctuation rates.

V. CONCLUSION

In this paper, we presented a comprehensive evaluation of naturally stochastic magnetic building blocks for implementing probabilistic algorithms compactly and efficiently. We generalized the proposed 1MTJ-3T design to a 1SR-3T design and presented necessary design rules for BSN operation that we hope will stimulate further interest in finding stochastic resistance (1SR) with suitable properties. We extended the physical performance analysis of the 1MTJ-3T BSN design to include unstable MTJ’s with different low-barrier-magnets as free layers. They are evaluated as physical realizations of the general stochastic resistor (SR) with respect to 14 nm FinFET transistors. IMA magnets with barrier $\leq k_B T$ proved to be the best option, low-barrier PMA can function as current-tunable resistors as well. While careful optimization of the fixed layer to cancel the stray fields in IMA MTJ is preferred, PMA can benefit from the presence of stray fields (can be a source of...
the $I_0$). The most challenging set of working conditions are set for telegraphic IMA magnets, even if they are highly optimized and no stray fields are present in the circuit, they need to be coupled with high current transistors due to their high pinning currents, because if paired with low current transistors like 14 nm FinFET results in a staircase-like functional behavior which does not work as a p-bit as we discussed.

These BSNs are an integral part of Ising machines which are often referred to as annealing processors. Using 1MTJ-3T BSN could speed up the operation of these processors by orders of magnitude. Another important application space for these BSN is stochastic neural networks. In fact, binary stochastic neurons are desired for deep learning networks, but are typically avoided because it is harder to generate random bits in CMOS hardware. Use of this compact neuron that relies on MTJs natural physics to provide stochastic binarization could accelerate computation in custom hardware by faster evaluation of BSN function and also encourage algorithmic advancement using BSN.

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Appendix A: Derivation for Pinning Field of LBM

Magnets are generally used to store information putting the focus on the evaluating and predicting characteristics of stable high-barrier magnets. It is interesting to note that theoretical predictions and analytical derivations regarding low-barrier magnet ($\Delta \leq k_B T$) dynamics typically receive less attention as cases of 'least practical interest'.[29] We document the analytical expressions associated with LBM in Fig. 9. The expressions for correlation time and biasing current can be found in ref.[25,27,33] in this appendix we derive the bias field.

We derive the expressions for external magnetic field $H_0$ required to pin the magnetization of an LBM with $\Delta \leq k_B T$ here. We start from the energy expression for the magnet $(E)$ and derive the expressions presented in Fig. 9 from the steady-state average magnetization defined by:

$$\langle m \rangle = \frac{\int_{\theta=0}^{\theta=\pi} \int_{\phi=0}^{\phi=\pi} \sin \theta \, d\phi \, d\theta \, m \exp(-E/k_B T)}{\int_{\theta=0}^{\theta=\pi/2} \int_{\phi=0}^{\phi=\pi} \sin \theta \, d\phi \, d\theta \, \exp(-E/k_B T)} \quad (A1)$$

where $\langle m_x, m_y, m_z \rangle \equiv (\cos \theta, \sin \theta \sin \phi, \sin \theta \cos \phi)$.

a. Perpendicular Magnetic Anisotropy (PMA)

In case of LBM with perpendicular magnetization, the anisotropy field along x-axis $H_{k_B} \rightarrow 0$ and thus for a field applied in the x-direction the energy expression eq. [1] is reduced to:

$$E = -H_{ext}M_S \Omega \, m_x \quad (A2)$$

Evaluation eq. [A1] wrt to this energy gives us:

$$\langle m_x \rangle = \coth(H_{ext}M_S \Omega / k_B T) - (H_{ext}M_S \Omega / k_B T)$$

The pinning field to any of its state $\langle m_x \rangle = \pm 1$, the required external field for PMA magnets can be approximated by:

$$|H_{ext}(PMA)| = \frac{2k_B T}{M_s \Omega} \quad (A3)$$

b. In-plane Magnetic Anisotropy (IMA)

For LBM with in-plane magnets, the anisotropy field along z-axis $H_{k_B} \rightarrow 0$ and a large demagnetization field $H_D$ exists along the z-axis which keeps the magnetization in-plane. The energy expression from eq. [1] in this case is:

$$E = H_D M_S \Omega m_z^2 - H_{ext} M_S \Omega m_z \quad (A4)$$

Once again evaluating eq. [A1] wrt to this energy for very large demagnetizing field $(H_D \rightarrow \infty)$ can be simplified to:

$$\langle m_z \rangle \approx H_{ext} M_S \Omega / 2k_B T.$$ 

The expression is independent of the demagnetization field. These empirical expressions match our SPICE simulation results quite well as shown in Fig. 14.

FIG. 14. Pinning Field of low-barrier magnets

The numerical evaluations of equations are compared to SPICE simulation for (a) isotropic magnets and (b) circular IMA magnets which have $\Delta \leq k_B T$. The pinning fields are shown to be a function of $M_S \Omega$ only where $M_S = 600 \text{emu/cc}$ and the volume of magnet $\Omega$ is varied. The pinning field values for IMA magnets indicate that it is independent of the large demagnetization field, $H_D$. The precise correspondence between the analytical formulations and the numerical simulation also constitutes as a benchmark to our finite temperature (stochastic) LLG formulation.

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