Design and simulation of three-level SVPWM based on FPGA

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Abstract. After expounding the overall design of the three-level SVPWM principle and algorithm, the SVPWM top level module using FPGA is created. And A/D conversion module, the Clarke transformation module, the adjacent vector function time module and the triangle carrier module are also established. Quartus II is used to simulation. And compared with the simulation results of MATLAB, the simulation waveforms are consistent, which verifies the correctness of the simulation results. Taking the diode clamped three-level inverter as the research object, the simulation waveforms of the different modulation M are compared, and the correctness of the three-level SVPWM control strategy is further verified.

1. Introduction
SVPWM is a relatively novel pulse width modulation strategy developed in recent years, which is the PWM wave generated in a specific switching mode. With the development of power electronics technology, three-level inverter has been widely used, and the corresponding pulse width modulation strategy is three-level SVPWM [1]. Compared with two-level SVPWM, three-level SVPWM has many advantages, such as low harmonic content and high utilization of DC voltage, so it has become a research hotspot. However, the three-level SVPWM control algorithm is complex, the parameter setting is flexible, and it is difficult to implement, so it becomes the difficulty of the research [2].

Because FPGA combines the greatest advantages of ASIC and processor-based systems, FPGA is widely used. FPGA can provide the speed and stability of hardware timing, and reprogrammed silicon chips are as flexible as software running on processor-based systems, but it is not limited by the number of available processor cores [3]. Unlike processors, FPGA belongs to real parallel processing, so different processing operations do not need to compete for the same resources. Each independent processing task is equipped with a dedicated chip part, which can operate independently without the influence of other logic blocks, and the performance of other applications will not be affected when more processing tasks are added. FPGA has the advantages of algorithm processing and speed, as well as the advantages of good real-time performance and simple design, so FPGA is used to carry out experimental research on three-level SVPWM [4].

In this article, the principle of three-level SVPWM pulse width modulation strategy is analyzed, and then the concrete scheme of designing three-level SVPWM algorithm using FPGA is given. The algorithm is simulated by Quartus II software, and compared with Matlab simulation waveforms to verify the correctness of the waveforms. Finally, the influence of M value on the waveform is analyzed, and the correctness of the three-level SVPWM control strategy is further verified.
2. The principle of three-level SVPWM algorithm

There are 27 groups of switching states corresponding to the three-level inverter, and their space vectors are shown in figure 1. The whole three-level space voltage vector consists of 6 long vectors (pnn ppn npp nnp pnp), 6 medium vectors (pon opn nop nop pno), 12 short vectors (poo ono onp opp noo ono pop oon pnp), and 3 zero vectors (ppp ooo nnn). In figure 1, long, medium, short and zero vectors are marked in different colors, where n represents low level, o represents zero level, and p represents high level. The SVPWM implementation includes three parts: sector judgment, time calculation and time state allocation [5].

2.1. Sector judgment

First of all, we can judge the large region of the reference vector, which can be divided into one area every 60° of the reference vector, and then judge the large region according to the angle between the reference vector and the α axis. The method of judging small area is introduced in detail by taking region I as an example. Let the reference vector Vref project Vα and Vβ on the α axis and β axis, respectively, and the amplitude angle is θ, then Vα=Vrefcosθ, Vβ=Vrefsinθ.

(1) When \( \theta \leq 30^\circ \), the Vref is in a small region 1 or 3 or 5. If \( V_\beta \leq -\sqrt{3}V_\alpha + \frac{\sqrt{3}}{2}V_d \), then Vref is in small area 1. If \( V_\beta \leq -\sqrt{3}V_\alpha + \frac{\sqrt{3}}{2}V_d \), then Vref is in small area 5. Otherwise, the Vref is in small area 3.

(2) When \( \theta \geq 30^\circ \), the Vref is in a small region 2 or 4 or 6. If \( V_\beta \geq -\frac{\sqrt{3}}{4}V_d \), then Vref is in small area 6. If \( V_\beta \leq -\sqrt{3}V_\alpha + \frac{\sqrt{3}}{2}V_d \), then Vref is in small area 2. Otherwise, the Vref is in small area 4.

2.2. Time calculation

According to the above-mentioned sector judgment method, it is known that the reference voltage vector falls in a specific region. According to the NTV (Nearest Triangle Vectors) rule, three basic vectors V1, V2 and V3 that synthesize the reference voltage vector are obtained, and they are substituted into the volt-second balance equations together with the reference voltage vector Vref.

\[
\begin{align*}
T_1 V_1 + T_2 V_2 + T_3 V_3 &= T_s V_{ref} \\
T_1 + T_2 + T_3 &= T_s
\end{align*}
\]  

(1)
The action time $T_1$, $T_2$ and $T_3$ of the three basic vectors can be obtained respectively.

2.3. Time state allocation
The negative short vector is selected as the starting vector of each sampling period, and its purpose is to correspond the action time and state distribution of the basic vector one to one, and the order of state action of each space vector region is shown in Table 1 (only sector I is given).

| Region | Vector state order |
|--------|--------------------|
| I1     | onn oon ooo poo ooo onn |
| I2     | oon ooo poo ppo ooo oon |
| I3     | onn oon pon ppo oon onn |
| I4     | oon pon ppo ppo onn oon |
| I5     | onn pnn pon ppo pnn onn |
| I6     | oon pon pnn ppo pnn onn |

In order to reduce the switching times and the switching loss, only one phase of the switching state is changed during each switching state transition, and the zero vector is evenly distributed in time, that is, the centrally symmetrical seven-segment SVPWM [6] is adopted. Taking the I region I cell as an example, the vector state order is onn, oon, ooo, ppo, ooo, onn, and then the corresponding switching state order can be determined. Taking the first phase as an example, the switching state order is 0110, 0110, 0110, 1100, 0110, 0110, 0110, where 0 indicates the turn-off of the switching device and 1 indicates the turn-on of the switching device. The seven-segment trigger waveform of the first phase switching device is shown in figure 2.

![Figure 2. Seven segment trigger waveform (the first phase of area 1 in area I)](image-url)

3. The implementation of FPGA design

3.1. Overall design of algorithm module
The design of the algorithm part includes three parts: the design of A/D conversion module, the design of Clarke transform module, the design of algorithm processing module and the design of triangle carrier module. The function of the algorithm processing module is to transform the sinusoidal signal outputted by the signal source into SVPWM modulated wave to generate SVPWM modulated wave [7]. The design purpose of the triangle carrier module is to compare with the SVPWM modulated wave to obtain the switching modes of each phase of the switch. The multiplier needs to be called several times during the design process [8].
3.2. The concrete design of the top-level module of SVPWM algorithm

In the SVPWM algorithm module, the input is the actual value collected, and the output is the switching mode after the triangle wave is compared with the generated SVPWM modulation wave. The SVPWM algorithm module can be divided into several small modules to design respectively, and the specific design scheme is shown in figure 3.

![Figure 3. The SVPWM top-level module design](image)

The top file of the SVPWM algorithm part invokes the A/D conversion module and the Clarke transformation module respectively to generate the adjacent vector action time module and triangle carrier module of each sector. After the completion of the above module call, it is also necessary to determine the switching time in each sector, and complete the comparison between the modulated wave and the triangular wave to generate the switching mode [9].

3.2.1. Design of coordinate transformation and action time module of adjacent vectors in each sector.

In order to make the design closer to the actual environment, the actual values are collected first, and the actual measured values are converted into A/D, and then the Clarke transformation is carried out. Clarke transform is to convert the three-phase voltage or current into a vector in the two-phase static coordinate system. Its design is relatively simple, thus the output voltage $V_\alpha$ and $V_\beta$ can be obtained. The function of the adjacent vector action time module of each sector is to judge the reference vector sector and generate the action time of each composite vector. According to the introduction of the principle part, it is easy to design this part, which will not be described in detail here [10].

3.2.2. Design of triangular carrier module.

The period and amplitude of the triangular carrier can be realized by accumulating the input clock. In general, the amplitude of the triangular carrier is set to half of the period. For each clock pulse, the triangle wave rises or falls by one step, and the rising or falling state of the triangle wave is determined by setting a flag bit. The turn-on and turn-off frequencies of the switching devices directly determine the sampling period of the triangular wave. In order to reduce the disadvantages caused by the high switching frequency, the maximum switching frequency is 10kHz.

3.2.3. Generation of SVPWM modulation wave and design of switching mode.

The generation of three-level SVPWM modulation wave is the key content of the design, and each sector uniquely corresponds to the switching time and specific transmission sequence of a group of switches, so in the top-level file, according to the sector where the reference vector is located, the three-level SVPWM modulation wave can be generated. The design of the switch mode is to get the switching time of the switching device on and off. From the point of view of the waveform, the purpose is to get the switching time of the high and low level. By comparing the generated modulation wave with the triangular carrier, the switching modes of each phase can be generated, which are represented by $T_{cm1}$, $T_{cm2}$, $T_{cm3}$, $T_{cm4}$, $T_{cm5}$ and $T_{cm6}$. Because the switching devices complement each other, only six switching times are needed. Figure 4 shows the RTL view of the module, including the basic vector action time module and the on-off time module of the switching device.
4. Simulation and result analysis

FPGA chooses Cyclone II series chip EP2C35F484C8N of ALTERA company to design using QuartusII 9.0 integrated development environment of ALTERA company. The simulation result of sector judgment time sequence based on ModelSim is shown in figure 5. It can be seen from the figure that the sector where the reference vector is located is judged. The PWM timing simulation waveform generated by three-level SVPWM is shown in figure 6. It can be seen from figure 6 that 12 PWM waves are generated, which complement each other and meet the design requirements.

In order to further verify the correctness of the three-level SVPWM algorithm, the space vector algorithm model is built in the Matlab/Simulink, and the same simulation parameters are set. The simulation waveform is shown in figure 7. As can be seen from figure 7, the waveform of Simulink is consistent with that of PWM in QuartusII environment, indicating that Quartus II implements the three-level SVPWM algorithm.
When the modulation is changed, the PWM waveform will be changed accordingly, taking $M=0.6$ and $M=0.8$ respectively. As shown in figure 8, the PWM waveform in one cycle in sector I cell is consistent with the principle analysis. From the calculation of the action time of the above basic vector, it can be seen that the turn-on time of the first switch in phase A is $T_1/2$, and the third switch is complementary to the first switch, so $T_1$ increases when $M$ increases, so $T_1$ increases. The turn-on time of the first switch becomes longer. Compared with figure 8 (a) and (b), the theoretical analysis is consistent with the simulation waveform, which effectively verifies the correctness of the theoretical analysis.

From the simulation results, we can see that for the complex SVPWM principle, making full use of the convenience and real-time advantages of FPGA design, it can be used as the processor of three-level SVPWM, through the simulation waveform can be intuitively analyzed, and then verify the correctness of the theory.

5. Conclusion
In this article, the three-level SVPWM algorithm is simulated in Quartus II software, and 12 PWM waves are generated, which is consistent with the PWM waveform generated by the SVPWM model built on the Matlab/Simulink platform, which proves the correctness of the three-level SVPWM algorithm. Moreover, the PWM waveforms under different modulation regimes are deeply analyzed to further verify the correctness of the theoretical analysis. It can be seen that the implementation of SVPWM algorithm with FPGA not only verifies the feasibility of the modulation strategy, but also solves the difficult problem of complex algorithm implementation.

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