Fabrication of Nickel Plasma Etching Mask by Nano-Imprint Lithography and Electroless Plating

Shingo Shimizu, Hideki Tanabe, Masaaki Yasuda, Yoshihiko Hirai, and Hiroaki Kawata*

Physics and Electronics, Graduate School of Engineering, Osaka Prefecture University, 1-1 Gakuen-cho, Kita-ku, Sakai, Osaka 599-8531, Japan
*kawata@pe.osakafu-u.ac.jp

Fine nickel (Ni) patterns were fabricated using the electroless plating. Poly(methyl methacrylate) (PMMA) patterns fabricated by the thermal nanoimprint lithography were used for the Ni pattern fabrication. Two processes, which were the “reverse pattern process” and the “same pattern process”, were developed. By the “reverse pattern process”, Ni pattern with the reverse to the PMMA pattern could be obtained. By the “same pattern process”, the same Ni pattern as the PMMA pattern could be obtained. Only by a slight process change, two different Ni patterns could be obtained from the same PMMA pattern. Silicon patterns were fabricated by plasma etching using the fabricated Ni patterns as an etching mask. By the “reverse pattern process”, good Si line and space pattern with about 0.2 μm width was successfully fabricated. By the “same pattern process”, a Si line and space pattern with about 0.2 μm width was also obtained, but its line edge roughness was large.

Keywords: Nickel electroless plating, Thermal nanoimprint lithography, Plasma etching

1. Introduction

Metal fine patterns are widely used for advanced optical devices [1,2], plasmon devices [3-5], plasma etching mask [6], etc. Since the metal mask usually has a very large etching selectivity, it is often used as a plasma etching mask for deep etching [7,8]. In particular, nickel (Ni) is used as a mask for deep etching because of its high plasma etching resistance [9,10]. Since Ni plasma etching is difficult, the lift-off process is often used for Ni fine pattern fabrication. In the lift-off process, a metal thin film is evaporated to resist pattern on a substrate, and the metal thin film on the resist pattern is removed during the resist remove. Then, the metal fine pattern is obtained on the substrate. When the resist pattern has an inverse taper shape, the resist remover solution can attack the resist from the resist side wall, and the lift-off process is successful (Fig. 1(a)). On the other hand, when a resist pattern has a normal taper shape, the resist can be hardly removed because the resist pattern is completely covered by metal film. Then, the lift-off process fails (Fig. 1(b)). Nanoimprint lithography (NIL) is a very powerful process for fabricating fine resist pattern [11,12]. In this process, the demolding is very important for fabricating good resist pattern [13]. For the successful demolding, the mold pattern with the normal taper is desirable [14,15]. Then, the resist pattern has the normal taper, but it is unsuitable for the lift-off process. Several processes have been proposed for successful lift-off for NIL resist patterns [16].

In this paper, a Ni electroless plating process was developed for fabricating Ni fine patterns instead of the lift-off process. This process has the following advantages over the lift-off process. (1) Even for the normal taper resist pattern, Ni fine patterns can be fabricated successfully. (2) The fabrication process is simple and easy. (3) The process time is short. (4) The metal film has a high etching resistance. (5) The fabrication process is compatible with NIL fabrication. (6) The metal film has a high thermal stability.

Fig. 1. Schematic views of lift-off, (a) for inverse taper resist pattern and (b) for normal taper resist pattern.
Successfully fabricated. (2) Since no vacuum process is used, the fabrication process is simple and the process time is short. (3) A Ni pattern, which is the same as or the reverse from the resist pattern, can be obtained by a slight process change. For both processes, the silicon patterns around 0.2 μm were fabricated by using the Ni pattern as the plasma etching mask.

2. Ni electroless plating process

A Ni film was deposited on a silicon substrate by use of the commercial Ni electroless plating process supplied by Technic Inc [17]. The process flow is shown in Fig. 2. A clean Si (Fig. 2(a)) is soaked in pretreatment solution (Techni conditioner 1221) and Pd treatment solution (Techni FPD catalyst) sequentially. Both soaking times are 60 s at the room temperature. Then, the palladium catalyst layer is deposited on the clean Si (Fig. 2(b)). This process is named as the Pd catalyst process, and the substrate with the Pd catalyst layer is called as the Pd treated substrate in this paper. The Pd treated Si substrate is soaked in the Ni plating bath (Techni Ni BG) at the temperature of 70 °C for 2-5 min. Note that the Ni film is deposited only on the Pd treated surface. (Fig. 2(c)). The process is simple and the process time is short because vacuum process, such as evaporation used in the lift-off, is not used. The Ni patterns are defined by resist patterns. Two processes, the “reverse pattern process” and the “same pattern process”, are developed as shown in Fig. 3. In the “reverse pattern process”, the Ni film is deposited on the substrate where the resist has been removed by development. Then, the fabricated Ni pattern is the reverse to the resist pattern (Fig. 3(a)). In the “same pattern process”, the Ni film is deposited on the resist remaining area. Then, the fabricated Ni pattern is the same as the resist pattern (Fig. 3(b)). The two different patterns can be obtained by a slight change of the fabrication process.

3. Reverse pattern process

One simple way to obtain the “reverse pattern process” is as follows. The Pd catalyst layer is deposited on a clean substrate by the Pd catalyst process. A resist is coated on the Pd treated substrate, and the resist is patterned by a lithography. Then, the Pd-treated surface is appeared in the area where the resist is removed. Since the Ni film is fabricated pattern by reverse pattern process using photolithography, (a) resist pattern and (b) Ni pattern.

![Fig. 2. Ni electroless plating process, (a) clean substrate, (b) Pd treated substrate, and (c) Ni deposited substrate.](image)

![Fig. 3. Schematic views of two processes, (a) the reverse pattern process and (b) the same pattern process.](image)

![Fig. 4. Fabricated pattern by reverse pattern process using photolithography, (a) resist pattern and (b) Ni pattern.](image)
deposited only on the Pd-treated surface, the Ni pattern with the reverse to the resist pattern is obtained. Figure 4 shows the results of the “reverse pattern process” by use of a conventional photo lithography. Figure 4(a) shows the line and space (LS) resist pattern with 2 μm half-pitch on a quartz substrate before the Ni plating. The four LS resist pattern areas were surrounded by the clear Pd treated quartz region. After the Ni plating, the surrounding region was covered by the opaque Ni film as shown in Fig. 4(b). This “reverse pattern process” worked well when the photo-lithography was used. However, this simple “reverse pattern process” has a serious problem when NIL is used as the resist patterning. In NIL process, the residual resist layer often remains in the resist bottom [18], and this layer is usually removed by oxygen contained plasma [19]. It was confirmed that the Pd catalyst was seriously damaged by the oxygen plasma exposure. Ni films could be hardly deposited even on the Pd-treated substrate after the residual layer remove by the oxygen plasma. In order to overcome this problem, new “reverse pattern process” was developed. The process is shown in Fig. 5. A poly(methyl methacrylate) film (PMMA film), whose average molecular weight is 350 kg/mol, is coated on a clean Si substrate, and the PMMA film is patterned by the thermal NIL (T-NIL). The T-NIL temperature, pressure, and press time are 180 °C, 10 MPa, and 10 min, respectively (Fig. 5(a)). The residual layer is removed by the oxygen plasma (Fig. 5(b)). The conventional ICP plasma etcher is used at the pressure of 2 Pa. After the PMMA pattern fabrication, the Pd catalyst process is applied to the substrate. The Pd catalyst is deposited on both the Si and the PMMA pattern surfaces (Fig. 5(c)). Since the Pd catalyst on the PMMA pattern must be removed, the substrate is soaked into the mixed solution of methyl isobutyl ketone (MIBK) and isopropyl alcohol (IPA). The mixed solution of MIBK and IPA is often used as the developer for the PMMA resist in the electron beam lithography [20]. The mixed ratio of MIBK and IPA is 1:1, and the soaking time is 10 s. Since the PMMA film is slightly etched during the MIBK/IPA soaking, the PMMA surface with the Pd catalyst layer is removed (Fig. 5(d)). The substrate is soaked in the electroless plating bath for 2 min. The Ni film is deposited only on the Si area (Fig. 5(e)). The PMMA resist is removed, and the Si substrate is etched by Bosch process [21,22]. Then, the Si pattern is fabricated (Fig. 5(f)).

![Fig. 5. Reverse pattern process using thermal nanoimprint lithography.](image)

![Fig. 6. Fabricated patterns by reverse pattern process using thermal nanoimprint lithography.](image)
fabrication results were shown in Fig. 6. Figure 6(a) shows the PMMA pattern after the MIBK/IPA soaking. It is found that a good PMMA pattern can be obtained without damage by the MIBK/IPA soaking. Figure 6(b) shows the Ni pattern after the PMMA resist remove. A good Ni pattern could be obtained. Figure 6(c) shows the fabricated Si pattern. The Ni film pattern worked well as the etching mask, and a good Si LS pattern of about 0.2 μm width could be successfully fabricated.

4. Same pattern process

The “same pattern process” is shown in Fig. 7. The Pd catalyst layer is deposited on a clean Si surface by the Pd catalyst process, and the PMMA film is coated on the Pd treated Si substrate (Fig. 7(a)). The PMMA pattern is fabricated by T-NIL under the same conditions given in the “reverse pattern process” (Fig. 7(b)). The residual layer after the imprint process is removed by the oxygen plasma at 2 Pa (Fig. 7(c)). Moreover, the Si substrate is exposed to the additional mixed gas plasma in order to completely remove the Pd catalyst (Fig. 7(d)). The mixed gas consists of 90% argon and 10% oxygen. The plasma pressure and the exposure time are 2 Pa, and 20 s, respectively. When a pure oxygen plasma is used, the additional plasma exposure may induce a serious PMMA line width loss. The mixed gas plasma is used in order to suppress the PMMA line width loss. Only the Pd catalyst under the PMMA line remains on the Si substrate. After the PMMA remove, the substrate is soaked in the electroless plating bath. Then, the Ni pattern, which is the same as the PMMA pattern, is obtained (Fig. 7(e)). The Si substrate is etched by Bosch process (Fig. 7(f)). Figures 8 show the results for the electroless plating time of 2 min. This plating time was the same as in the “reverse pattern process”. The top view of the Ni pattern after the Ni electroless plating is shown in Fig. 8(a). Many circular Ni dots were observed in the Ni line area and the Ni line had many voids. The fabricated Si pattern is shown in Fig. 8(b). The Si pattern was bad because of the poor Ni mask pattern. Since the Ni deposition seemed to be insufficient, the plating time was extended to 5 min. The top view of the Ni pattern is shown in Fig. 9(a). The line pattern shape was improved. However, the circular dots were still formed. Since the Ni circular rod size was relatively large, the line edge roughness was observed. The fabricated Si pattern is shown in Fig. 9(b). Si lines around 0.2 μm width could be fabricated, but the line width variation was clearly found because of
the line edge roughness of the Ni mask. It is considered that the Pd catalyst degradation and/or the Pd catalyst condensation must be induced during the T-NIL press at 180 °C. In order to confirm the temperature effect, the following experiment was carried out. The Pd catalyst process was performed to a clean Si substrate without PMMA pattern. The Pd treated Si substrate was baked on a hot plate for 10 min at various temperatures. After the baking, the electroless plating was performed for 2 min. Figures 10 show the results for the baking temperatures of $T_b=100 ^\circ C$, $140 ^\circ C$, and $180 ^\circ C$. The circular Ni rods were found for all baking temperatures. The Ni films clearly had voids for $T_b=140 ^\circ C$, and $180 ^\circ C$. The voids increased as increasing the baking temperature. It is confirmed that the Ni pattern degradation is induced by the high temperature process.

**5. Conclusion**

Fine nickel patterns were fabricated using the electroless plating. PMMA patterns fabricated by the thermal nanoimprint were used for the Ni pattern fabrication. Two processes, which were the “reverse pattern process” and the “same pattern process”, were developed. The “reverse pattern process” produces the Ni pattern reverse to the PMMA pattern. On the other hand, the “same pattern process” produces the same Ni pattern as the PMMA pattern. Si patterns were fabricated using the Ni patterns as a plasma etching mask. By the “reverse pattern process”, good Si line and space pattern with about 0.2 μm width was successfully fabricated. By the “same pattern process”, Si line and space pattern with about 0.2 μm width could be also obtained. However, its line edge roughness was large since the Ni line mask pattern was not good. It is confirmed that the degradation of the Pd catalyst was induced by the high temperature process during the PMMA T-NIL and the deposited Ni shape became worse. The “same pattern process” will be improved in order to obtain a good Ni mask pattern.

**Acknowledgement**

This work was partially supported by JSPS KAKENHI Grant Number 19K05274.

**References**

1. A. Barbara, P. Quémerais, E. Bustarret, and T. Lopez-Ríos, Phys. Rev. B, **66** (2002) 161403.
2. H.-S. Lee, Y.-T. Yoon, S.-S. Lee, S.-H. Kim, and K.-D. Lee, Opt. Express, **15** (2007) 15457.
3. W. L. Barnes, A. Dereux, and T. W. Ebbesen, Nature, **424** (2003) 824.
4. J. Zhao, X. Zhang, C. R. Yonzon, A. J. Hoes, and R. P. van Duyne, Nanomedicine, **1** (2006) 219.
5. Z. Wu, J. W. Haus, Q. Zhan, and R. L. Nelson, J. Nonlinear Opt. Phys., **17** (2008) 413.
6. H. Toyota, K. Takahara, M. Okano, T. Yotsuya, and H. Kikuta, Jpn. J. Appl. Phys. Part 2, **40** (2001) L747.
7. T. Ichiki, Y. Sugiyama, T. Ujiie, and Y. Horiike, J. Vac. Sci. Technol. B, **21** (2003) 2188.
8. C. T. Gabriel, R. Y. Kim, and D. C. Baker, J. Vac. Sci. Technol. A, **18** (2000) 1420.
9. S. Benchabane, L. Robert, J.-Y. Rauch, A. Khelif, and V. Laude, J. Appl. Phys., **105** (2009) 094109.
10. N. V. Toan, S. Sangu, and T. Ono, IEEJ Trans. SM, **136** (2016) 41.
11. S. Y. Chou, P. R. Krauss, and P. J. Renstrom, Appl. Phys. Lett., **67** (1995) 3114.
12. S. Y. Chou, P. R. Krauss, W. Zhang, L. Guo, and
L. Zhuang, *J. Vac. Sci. Technol. B*, **15** (1997) 2897.
13. T. Kitagawa, N. Nakamura, H. Kawata, and Y. Hirai, *Microelectron. Eng.*, **123** (2014) 65.
14. H. Kawata, K. Kubo, Y. Watanabe, J. Sakamoto, M. Yasuda, and Y. Hirai, *Jpn. J. Appl. Phys.*, **49** (2010) 06GL15.
15. T. Tochino, K. Uemura, M. Michalowski, K. Fujii, M. Yasuda, H. Kawata, Z. Rymuza, and Y. Hirai, *Jpn. J. Appl. Phys.*, **54** (2015) 06FM06.
16. T. Okada, J. Fujimori, and T. Iida, *Jpn. J. Appl. Phys.*, **50** (2011) 126502.
17. Technic Inc., https://www.technic.com/.
18. H. Hiroshima, *Microelectron. Eng.*, **86** (2009) 611.
19. N. Chaix, C. Gourgon, C. Perret, S. Landis, and T. Leveder, *J. Vac. Sci. Technol. B*, **25** (2007) 2346.
20. S. Yasin, D. G. Hasko, H. Ahmed, *Microelectron. Eng.*, **61-62** (2002) 745.
21. H. Kawata, M. Matsue, K. Kubo, M. Yasuda, and Y. Hirai, *Microelectron. Eng.*, **86** (2009) 704.
22. J. Sakamoto, H. Kawata, M. Yasuda, and Y. Hirai, *Jpn. J. Appl. Phys.*, **50** (2011) 08KC03.