Active Switched-Capacitor Embedded Quasi-Z-Source Inverter and PWM Methods for High Boost Capability and Switching Loss Reduction

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ABSTRACT This paper proposes a novel topology, named a single-phase active switched-capacitor embedded quasi-Z-source inverter (ASC-EqZSI), and two pulse-width modulation (PWM) methods, namely, PWM1 and PWM2 methods for the proposed ASC-EqZSI topology to improve the boost capability and reduce switching loss. The boost capability can be improved by using an additional non-shoot-through (NST) state, referred to as the NST2 state, besides conventional shoot-through (ST) and NST states. In the NST2 state, the switch in the impedance network is switched on to boost the dc-link voltage while generating the ac output voltage. A PWM1 method is suggested to control both the NST2 and ST time intervals with one carrier signal for improving the boost capability. A PWM2 method aims to reduce the commutation count of the switches and diodes in the proposed topology while maintaining the enhanced boost capability. The switching loss can be reduced by almost 40%. A comparative analysis between the proposed topology with the PWM2 method and five other topologies with an active switched Z-network is performed. The proposed topology with the PWM2 method has a higher ac voltage gain and efficiency with fewer components. Simulation and experimental results are carried out to validate the performances of the proposed topology and PWM methods.

INDEX TERMS Active switched-capacitor, boost capability, high voltage gain, impedance network, pulse-width modulation, quasi-Z-source inverter, switching loss.

I. INTRODUCTION

The Z-source inverter/quasi-Z-source inverter (ZSI/qZSI) composed of an impedance network and an inverter provides the buck-boost capability by a shoot-through (ST) state and short-circuit immunity of an inverter leg [1], [2]. However, the voltage gain of the classic ZSI/qZSI is not high, which makes it difficult to apply to industrial applications requiring a high voltage gain. In order to solve the boost limitation of the classic ZSI/qZSI, many modifications and improvements on the ZSI/qZSI-based topology and its modulation techniques have been proposed. Utilizing switched-inductor (SL), switched-capacitor (SC), switched-inductor-capacitor (SLC), and SL/SC structures to the classic (q-)ZSI provides high boost capability [3], [4], [5], [6], [7], [8].

By adding extra passive components into the (q-)Z-source impedance network, the new inverter topologies are referred to as continuous diode-assisted/capacitor-assisted extended-boost qZSIs [9], enhanced-boost ZSI combined with two switched Z-impedance networks [10], enhanced-boost qZSI with two switched-impedance networks (EB-qZSI) for continuous input current configuration [11], embedded switched-inductor qZSIs with two isolated dc sources [12], and high-boost qZSI combined with two quasi-Z-source networks [13]. These topologies offer high voltage gain. However, they have many passive components, which results in
increasing the cost and volume of the power converter and deteriorating the efficiency.

The switched boost inverter (SBI) based on the Inverse Watkins-Johnson topology [14] was introduced in [15]. The SBI has one extra switch to reduce the number of passive components in the impedance network. However, it has a lower boost factor than the ZSI/qZSI, and its source current is discontinuous. In order to build up to the same boost factor as the classic qZSI with a continuous dc source current, a class of quasi-switched boost inverters (qSBIs) was proposed in [16]. Compared with a classic single-phase qZSI, a single-phase qSBI has fewer passive components, one extra switch in the impedance network, and higher efficiency [17].

In order to improve the boost capability of the basic (q)SBI, various topologies with the active switched network, like the (q)SBI topology, have been proposed [18], [19], [20], [21], [22], [23], [24], [25]. By adding one diode and capacitor to the classic qSBI, switched-capacitor quasi-switched boost inverters (SC-qSBIs) [18] can achieve high voltage gain with low voltage stress across capacitors and diodes. The SC-qSBIs can be extended to an n-cell to improve the voltage gain even more. In [19], two high voltage gain quasi-switched boost inverters (HG-qSBIs) and a modulation technique were proposed to perform a high voltage gain with a low source current ripple. In comparison with the EB-qZSI [11], an enhanced-boost qZSI with an active switched Z-network (EB/ASN-qZSI) in [20] can reduce two LC pairs with the same boost factor. Additionally, the high boost non-isolated qZSI (HB-ni-qZSI) in [21] can produce a higher voltage gain with fewer components by combining with a new active switched Z-impedance network. The continuous current active SL-boost-qZSI (cASLB-qZSI) in [22] provides high boost capability with continuous input current by combining an active switched-inductor boost network. The switched ZSI based on the active switched-capacitor with a high voltage conversion ratio, referred to the capacitor assisted switched-capacitor extended boost-ZSI (CSC-EB-ZSI), was presented in [23]. The continuous input current qZSI (CC-qZSI) can be implemented by applying the concept of switched-boost-modified ZSI into the qZSI [24]. The high voltage gain active switched qZSI (HGAS-qZSI) in [25] offers a higher output voltage with proper number of components in the impedance network.

The (q)-ZSI requires special attention to its modulation strategies, because the modulation strategies for the (q)-ZSI affect the current ripple, switching loss, boost capability, and also reliability [26], [27]. Modulation strategies for the (q)-ZSI can be classified as carrier-based pulse width modulation (CB-PWM) and space vector modulation (SVM). The CB-PWM includes simple boost control [1], maximum boost control [28], and maximum constant boost control methods [29]. Among these three modulation methods, the maximum boost control method realizes the highest boost factor by turning all zero states into ST states. In [30] and [31], the hybrid PWM combined the PWM and the pulse-amplitude modulation (PAM), and the dual switching modulation are proposed, respectively, to reduce power loss of the converter. A sawtooth-carrier-based PWM (SCPWM) method with the zero-voltage switching operation is applied to qZSI to reduce the total harmonic distortion (THD) and inductor current ripple [32]. In [33], the conventional space-vector concept was modified and applied to the (q)-ZSI, due to the high voltage utilization and low current harmonics. Additionally, modified SVM methods for qZSI have been suggested to reduce the inductor current ripple, switching loss, and leakage current [34], [35], [36], [37].

The qSBI has one additional switch in the impedance network to reduce the passive elements. In the qSBI, the switches in the inverter are utilized to generate a sinusoidal output voltage, and the switch in the impedance network is used to boost the dc-link voltage. A simple boost control method has been applied to the qSBI, where the switch is turned on during the constant ST state [15]. Modified modulation strategies for the qSBI have been introduced to improve the performance [19], [38], [39], [40], [41]. A family of PWM control schemes, aiming to improve the modulation index and reduce the inductor current ripples of the qSBI, were proposed in [19], [38], and [39]. The modified PWM strategy for the dc-linked type qSBIs proposed in [40] increases the boost factor and reduces the inductor current ripple. The PWM strategies in [19] and [38], [39], [40] increase the switching loss of the additional switch and require two carrier signals with different frequency and amplitude. An SVM method for a modified qSBI with two switches to suppress the magnitude of the common-mode voltage was introduced in [41].

In this paper, a novel single-phase active switched-capacitor embedded qZSI (ASC-EqZSI) topology and two new PWM methods, namely, PWM1 and PWM2 methods for achieving high boost capability and reducing switching loss are suggested. The improved boost capability is achieved by using an additional non-shoot-through (NST) state, referred to as NST2, besides conventional shoot-through (ST) and NST states. The PWM1 method for the proposed ASC-EqZSI topology is presented to control both the NST2 and ST time intervals for increasing the boost factor. The proposed PWM2 method can reduce the switching losses of the switches and diodes in the proposed topology, while still maintaining high boost capability. The operation analysis of the proposed ASC-EqZSI topology and impedance parameter design are described. A detailed comparative analysis between the proposed ASC-EqZSI utilizing the new PWM method and five other topologies with an active switched Z-network is also performed. The performances of the proposed topology and PWM methods are verified through simulations and experiments using a prototype built in the laboratory.

II. PROPOSED TOPOLOGY

Fig. 1 shows the structure of the proposed single-phase ASC-EqZSI topology. The impedance network connected to a single-phase inverter of the proposed topology has two inductors (L1, L2), two capacitors (C1, C2), two diodes (D1, D2) and
one switch \( S_0 \). The dc source is embedded in series with the inductor \( L_2 \) in the impedance network.

**A. OPERATION PRINCIPLES OF ASC-EqZSI**

The topologies based on the SBI structure generally have two operating states: the shoot-through (ST) state and the non-shoot-through (NST) state. The additional switch \( S_0 \) is switched on during the ST state, and is switched off during the NST state. The proposed topology has one more operating state, which we refer to as the NST2 state. In the NST2 state, the switch \( S_0 \) is switched on outside of the ST time interval to step up the boost factor, while the inverter operates in the active or zero state like the conventional NST state. The conventional NST state is referred to as the NST1 state. Therefore, the proposed topology has three operating states: ST, NST1, and NST2 states. The equivalent circuits of the proposed topology for the three operating states are shown in Fig. 2. Using equivalent circuits of the proposed topology, the operation principles for the three operating states will be described.

1) **SHOOT-THROUGH STATE**

During the ST state, the dc-link of the inverter is shorted by conducting two switches of any phase leg and the switch \( S_0 \) is switched on, as shown in Fig. 2(a). The diodes \( D_1 \) and \( D_2 \) are reverse biased during the ST time interval of \( D_0 \cdot T \), where \( D \) is the ratio of the ST time to one switching period \( T \). The inductor \( L_1 \) is charged from the capacitor \( C_2 \). The inductor \( L_2 \) is charged from the dc input voltage \( V_{dc} \) and capacitor \( C_1 \). From Fig. 2(a), the inductor voltages and capacitor currents are given by

\[
\begin{align*}
V_{L1} &= V_{C2}, \quad V_{L2} = V_{dc} + V_{C1} \\
i_{C1} &= -i_{L2}, \quad i_{C2} = -i_{L1}.
\end{align*}
\]

2) **NON-SHOOT-THROUGH 1 STATE**

In the NST1 state, as shown Fig. 2(b), the proposed inverter operates in the active or zero state. The switch \( S_0 \) is switched off and two diodes \( D_1 \) and \( D_2 \) are forward biased. A single-phase inverter and load are modelled with a constant current source \( I_o \), which is the current through the inverter bridge during the NST1 and NST2 states. The capacitor \( C_2 \) is charged from the dc voltage \( V_{dc} \) and inductor \( L_2 \). The energy stored in the two inductors \( L_1 \) and \( L_2 \) is supplied to the load side and two capacitors \( C_1 \) and \( C_2 \). From Fig. 2(b), the inductor voltages, capacitor currents, and dc-link voltage are given by

\[
\begin{align*}
V_{L1} &= V_{C2} - V_{C1}, \quad V_{L2} = V_{dc} - V_{C2} \\
i_{C1} &= i_{L1} - I_o, \quad i_{C2} = i_{L2} - i_{L1} \\
i_{pm} &= V_{C1}.
\end{align*}
\]

3) **NON-SHOOT-THROUGH 2 STATE**

In the NST2 state, as shown in Fig. 2(c), the switch \( S_0 \) is switched on outside of the ST time interval while the proposed inverter operates in active or zero state like the NST1 state. The time interval in the NST2 state is \( D_0 \cdot T \), where \( D_0 \) is the ratio of the NST2 time interval to one switching period \( T \). Thus, the time interval of the NST1 state is represented as \((1-D-D_0) \cdot T\). The dc-link voltage can be boosted by controlling the duty ratio \( D_0 \) while generating the ac output voltage. The diode \( D_1 \) is reverse biased whereas the diode \( D_2 \) is forward biased during this state. The capacitor \( C_2 \) and inductor \( L_1 \) supply the energy to the capacitor \( C_1 \) and load side. The inductor \( L_2 \) is charged from the dc input voltage \( V_{dc} \). From Fig. 2(c), the inductor voltages, capacitor currents and dc-link voltage are given by

\[
\begin{align*}
V_{L1} &= V_{C2} - V_{C1}, \quad V_{L2} = V_{dc} \\
i_{C1} &= i_{L1} - I_o, \quad i_{C2} = -i_{L1} \\
i_{pm} &= V_{C1}.
\end{align*}
\]

It can be noted that the dc-link voltage in the NST2 state is the same as that in the NST1 state.

**B. BOOST FACTOR AND INDUCTOR CURRENT STRESS**

By applying the volt-second balance principle to both inductors \( L_1 \) and \( L_2 \) from (1), (3), and (6), two capacitor voltages...
can be derived as

\[ V_{C1} = \frac{1}{D^2 + (D_a - 3)D + 1 - D_a} V_{dc} \]  
\[ V_{C2} = \frac{1 - D}{D^2 + (D_a - 3)D + 1 - D_a} V_{dc}. \]

The capacitor voltage \( V_{C1} \) from (5) or (8) is a peak dc-link voltage. From (9), the boost factor \( B \) is expressed as

\[ B = \frac{\dot{V}_{pn}}{V_{dc}} = \frac{V_{C1}}{V_{dc}} = \frac{1}{D^2 + (D_a - 3)D + 1 - D_a} \]

where the boost factor \( B \) can be controlled by the ratio \( D_a \) as well as \( D \).

By applying the ampere-second balance principle to both capacitors \( C_1 \) and \( C_2 \) from (2), (4), and (7), the average of two inductor currents can be derived as

\[ \dot{i}_{L1} = \frac{(1 - D)(1 - D - D_a)}{D^2 + (D_a - 3)D + 1 - D_a} I_o \]
\[ \dot{i}_{L2} = \frac{(1 - D)}{D^2 + (D_a - 3)D + 1 - D_a} I_o. \]

III. PROPOSED PWM METHODS FOR ASC-EQZSI

Two new PWM methods (PWM1, PWM2) based on the simple boost control method suitable for the proposed ASC-EqZSI are proposed to increase the boost factor and reduce the switching losses of the switches and diodes.

A. PWM1 METHOD

Fig. 3 shows the proposed PWM1 method with a single triangular carrier signal. By using a single-phase reference voltage \( V_{ref} \), both the positive and negative modulation signals \( V_{ref,p} \) and \( V_{ref,n} \) are calculated as

\[ V_{ref,p} = \frac{1}{2} ((\text{abs}(V_{ref} + V_{ref})) \]
\[ V_{ref,n} = \frac{1}{2} ((\text{abs}(V_{ref} - V_{ref})). \]

The PWM signals of the pairs \( S_1/S_3 \) (or \( S_2/S_4 \)), which are switched complementarily, are generated by comparing a carrier signal \( V_{tri} \) with the positive modulation signal \( V_{ref,p} \) (or the negative modulation signal \( V_{ref,n} \)). By comparing the ST envelop signal \( V_{ST} \) to the carrier signal \( V_{tri} \), the ST signal \( S_{ST} \) is generated to adjust the ST time interval, \( D \cdot T \). The ST signal \( S_{ST} \) is inserted into the PWM signal \( S_1 \) (or \( S_4 \)) when the reference signal is positive (or negative) to generate the ST state. Two signals \( P_p \) and \( P_n \) are utilized to detect the polarity of the reference signal. By comparing another control signal \( V_{Da} \) to the carrier signal \( V_{tri} \), the signal \( S_{Da} \) is generated to adjust the time interval of the NST2 state, \( D_a \cdot T \). The switch \( S_0 \) control signal can be obtained from adding \( S_{ST} \) and \( S_{Da} \). The commutation count of the switch \( S_0 \) is increased two-fold due to the NST2 state. Therefore, the switching loss of the switch \( S_0 \) is increased.

B. PWM2 METHOD

Fig. 4 shows the proposed PWM2 method to reduce the commutation count of the diodes and the inverter switches as well as the switch \( S_0 \) in the proposed topology. The PWM2 method can be implemented by replacing the triangle carrier signal of the PWM1 method with a sawtooth carrier signal. The process used to generate the \( S_{ST} \), \( S_{Da} \), and PWM signals of the PWM2 method is the same as that of the PWM1 method. The logic of the switching signal generation for the proposed PWM method is illustrated in Fig. 5. The proposed PWM methods require only one carrier signal, and the PWM methods can be selected depending on whether the carrier signal is a triangular wave (\( V_{tri} \)) or a sawtooth wave (\( V_{saw} \)).

C. COMPARISON BETWEEN PWM1 AND PWM2 METHODS

The PWM2 method can reduce the commutation count of the three switches (\( S_1 \), \( S_4 \), and \( S_0 \)) in the proposed method.
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FIGURE 5. Logic of switching signal generation for the proposed PWM methods.

FIGURE 6. Efficiency and power loss comparisons between the PWM1 and PWM2 methods: (a) efficiency comparison, (b) power loss distribution comparison when the output power = 1.2 kW.

IV. PARAMETER DESIGN OF PASSIVE COMPONENTS

The proposed single-phase ASC-EqZSI topology generates low-frequency (2ω) and high-frequency ripples on the inductors and capacitors in the impedance network, similar to the classic single-phase qZSI. Assuming the 2ω ripple can be eliminated by using control methods [42], the inductors and capacitors are designed based on the high-frequency ripple when the PWM2 method is used for the proposed topology. From Fig. 7(b), the maximum peak-to-peak current ripples of the inductor \( L_1 \) during the ST state and the inductor \( L_2 \) during the NST1 state can be expressed as

\[
\Delta i_{L1} = \frac{V_{C2}}{L_1} DT, \quad \Delta i_{L2} = \frac{V_{C2} - V_{dc}}{L_2} (1 - D - D_a) T.
\]

(16)

Using (10), (11), (12), (13), (16), and the load current \( I_o = \frac{V_{pm}}{R_L} \) where \( R_L \) is the load resistance, the inductances of \( L_1 \) and \( L_2 \) are derived as

\[
L_1 = \frac{D \cdot R_L}{r_{L1} \% \cdot f_s \cdot (1 - D - D_a) \cdot B}
\]

(17)

topology by half, compared to the PWM1 method. In addition, the commutation count of one diode (\( D_1 \)) in the impedance network can be reduced by half by using the PWM2 method. Therefore, the proposed PWM2 method can reduce the overall commutation count of all switches and diodes in the ASC-EqZSI topology by 40% and 34%, respectively, as compared to the proposed PWM1 method. It can be noted that the switching losses of the switches and diodes in the ASC-EqZSI topology can be considerably decreased by adopting the PWM2 method.

Fig. 6 compares the efficiency and power loss of the proposed topology with the PWM1 and PWM2 methods, respectively. The current ripple on the inductor \( L_1 (\Delta i_{L1}) \) of the PWM2 method is the same as that of the PWM1 method. The PWM2 method has a slightly higher current ripple on the inductor \( L_2 (\Delta i_{L2}) \), as compared to the PWM1 method. Fig. 8 shows the two capacitor voltage ripples in one switching cycle using the PWM1 and PWM2 methods, respectively. The ripple voltage in \( V_{C1} (\Delta V_{C1}) \) of the PWM2 method is the same as that of the PWM1 method. The PWM2 method has a slightly higher voltage ripple on the capacitor \( C_2 (\Delta V_{C2}) \), as compared to the PWM1 method.

II. Topology Design

The proposed single-phase ASC-EqZSI topology generates low-frequency (2\( \omega \)) and high-frequency ripples on the inductors and capacitors in the impedance network, similar to the classic single-phase qZSI. Assuming the 2\( \omega \) ripple can be eliminated by using control methods [42], the inductors and capacitors are designed based on the high-frequency ripple when the PWM2 method is used for the proposed topology.
impedance network among the five topologies, and they have and CC-qZSI topologies have the fewest components in the
ogy and five other topologies. Both the proposed ASC-EqZSI
in the impedance network of the proposed ASC-EqZSI topol-
Table 1 depicts the number of passive and active components
stresses on the diodes and switch, and ST current.
and current
the same number of the inductors, capacitors, diodes, and
switch each.
B. BOOST FACTOR AND AC VOLTAGE GAIN COMPARISON
The boost factor or ac voltage gain is a critical factor to
evaluate the performance of the proposed ASC-EqZSI with
the PWM2 method and the five other topologies with the
conventional PWM method in [16]. Fig. 9(a) shows the
boost factor versus shoot-through duty ratio for the six
topologies. The proposed topology with the PWM2 method at
\( D_o = 0 \) has the lowest boost factor with CC-qZSI topology.
The boost factor can be increased by increasing the duty
ratio \( D_o \). When the duty ratio \( D_o \) of the proposed topology
increases to 0.5, the proposed topology with the PWM2 method
achieves the highest boost factor in the overall range of \( D \), followed by
HGAS-qZSI topology.
The ac voltage gain \( G \) is expressed as \( G = \frac{\hat{V}_o}{V_{dc}/2} = M \cdot \hat{B} \), where \( \hat{V}_o \) is a peak output voltage and \( M \) is a modulation
index. The relationship between \( M \) and \( D \) is determined by
the modulation strategy. As the proposed topology adopts a
simple boost control method, the shoot-through duty ratio \( D \)
is limited to \( 1 - M \) and the duty ratio \( D_o \) is limited to \( M \).
Using \( D = 1 - M \), the ac voltage gain \( G \) can be written in
terms of \( M \). Fig. 9(b) shows the ac voltage gain \( G \) versus modulation index \( M \) for the six topologies. When the duty
ratio \( D_o = 0.5 \), the proposed topology with the PWM2 method
achieves the highest ac voltage gain. When the duty
ratio \( D_o \) increases more, a higher boost factor and ac voltage
gain can be obtained.

C. VOLTAGE AND CURRENT STRESSES COMPARISON
In order to compare properly the voltage and current stresses
on the capacitors, diodes, and switch in the impedance

V. COMPARATIVE ANALYSIS
To evaluate the performance of the proposed ASC-EqZSI
topology using the PWM2 method, a comparative study is
performed with five state-of-the-art topologies with an active
switched network: EB/ASN-qZSI [20], HB-ni-qZSI [21],
CSC-EB-ZSI [23], CC-qZSI [24], and HGAS-qZSI [25]. The
comparisons focus on the number of components used in the
impedance network, boost factor, ac voltage gain, capacitor
voltage stress, inductor current stress, voltage and current
stresses on the diodes and switch, and ST current.

A. NUMBER OF COMPONENTS COMPARISON
Table 1 depicts the number of passive and active components
in the impedance network of the proposed ASC-EqZSI topol-
yogy and five other topologies. Both the proposed ASC-EqZSI
and CC-qZSI topologies have the fewest components in the
impedance network among the five topologies, and they have

B. BOOST FACTOR AND AC VOLTAGE GAIN COMPARISON

FIGURE 8. Capacitor voltage ripples in one switching cycle: (a) PWM1
method, (b) PWM2 method.

\[
L_2 = \frac{(1 - D)(1 - D - D_o)R_L}{r_{L2} \cdot f_s \cdot (1 - D) \cdot B^2} \tag{18}
\]
where the maximum permitted current ripple ranges of the
two inductors are defined as \( r_{L1} = \Delta I_{L1} / I_{L1} \) and \( r_{L2} = \Delta I_{L2} / I_{L2} \), respectively. Additionally, \( f_s \) is the switching
frequency.
From Fig. 8(b), the maximum peak-to-peak voltage ripples
of the capacitor \( C_1 \) during the ST state and the capacitor \( C_2 \)
during the NST1 state can be expressed as
\[
\Delta V_{C1} = \frac{i_{L2}}{C_1} DT, \quad \Delta V_{C2} = \frac{i_{L1} - i_{L2}}{C_2} (1 - D - D_o) T. \tag{19}
\]
Using (10), (11), (12), (13), (19), and the load current
equation, the capacitances of \( C_1 \) and \( C_2 \) are derived as
\[
C_1 = \frac{D(1 - D) \cdot B}{r_{C1} \cdot f_s \cdot R_L} \tag{20}
\]
\[
C_2 = \frac{(D + D_o)(1 - D - D_o) \cdot B}{r_{C2} \cdot f_s \cdot R_L} \tag{21}
\]
where the maximum permitted ripple ranges of the two
capacitors are defined as \( r_{C1} = \Delta V_{C1} / V_{C1} \) and \( r_{C2} = \Delta V_{C2} / V_{C2} \), respectively.

FIGURE 9. Boost factor and ac voltage gain comparison: (a) boost factor
versus shoot-through duty ratio, (b) ac voltage gain versus modulation
index.

| Components | EB/ASN-qZSI [20] | HB-ni-qZSI [21] | CSC-EB-ZSI [23] | CC-qZSI [24] | HGAS-qZSI [25] | ASC-EqZSI |
|------------|-----------------|-----------------|-----------------|--------------|-----------------|-----------|
| Inductors  | 2               | 2               | 3               | 2            | 2               | 2         |
| Capacitors | 2               | 3               | 4               | 2            | 4               | 2         |
| Diodes     | 4               | 5               | 3               | 2            | 4               | 2         |
| Switches   | 1               | 1               | 1               | 1            | 1               | 1         |
network of the six topologies, the voltage stress ratio, defined as the ratio of the voltage stress to the ac output voltage, is used for the voltage stress comparison. The current stress ratio, defined as the ratio of the current stress to ($B \cdot I_0$), is used for the current stress comparison. Table 2 summarizes the voltage stress ratios of the capacitors, diodes, and switch, and the current stress ratios of the inductors, diodes, and switch for the six topologies.

Figs. 10(a), 10(b), and 10(c) show the total voltage stress ratio comparison of the capacitor, diode, and switch, respectively, for the proposed ASC-EqZSI with the PWM2 method and the five other topologies. The proposed ASC-EqZSI topology provides the highest total capacitor voltage stress ratio, and the total diode voltage stress and switch voltage stress ratios are in the comparatively intermediate range.

Fig. 10(d) shows the ratio of the total inductor current stress to ($B \cdot I_0$). The total inductor current stress ratio of the proposed ASC-EqZSI at $D_a = 0$ is the same as that of the three other topologies like EB/ASN-qZSI, HB-ni-qZSI, and CC-qZSI. When $D_a$ increases to 0.5, the proposed ASC-EqZSI has the lowest total inductor current stress ratio. Because the total inductor current is the same as the ST current, the lowest total inductor current stress ratio saves the cost of the inductors and inverter switches. Figs. 10(e) and 10(f) show the ratios of the total diode and switch current stress to ($B \cdot I_0$), respectively. Both the proposed ASC-EqZSI and CC-qZSI can produce the lowest total diode current stress ratio. The HB-ni-qZSI topology provides the lowest switch current stress ratio, followed closely by the proposed ASC-EqZSI, CC-qZSI, and CSC-EB-ZSI topologies.

From Fig. 10, a large duty ratio $D$ at the proposed ASC-EqZSI increases the voltage stresses across the capacitors and diodes, and decreases the current stresses on the inductors, diodes, and extra switch.

To better evaluate the voltage and current stresses of the proposed topology, the switching device power (SDP) is introduced. The SDP of the switching devices is expressed as the product of their voltage and current stresses. The total SDP of the topology is defined as the summation of SDP of all switching devices used at the topology. In this paper, the SDPs for diodes and extra switch used at the impedance network are compared. Based on the definition of the peak and average SDPs in [10], the peak and average SDPs for extra switch of the proposed ASC-EqZSI with the PWM2 method are derived as

$$SDP_{(pk, \text{extra switch})} = \frac{1}{D^2 + (D_a - 3)D + 1 - D_a} P_o$$

$$SDP_{(av, \text{extra switch})} = \frac{D}{D^2 + (D_a - 3)D + 1 - D_a} P_o$$

where $P_o$ is the inverter output power.

Similarly, the peak and average SDPs for diodes are derived as follows:

$$SDP_{(pk, \text{diodes})} = \frac{D^2 - 3D + 3}{D^2 + (D_a - 3)D + 1 - D_a} P_o$$

$$SDP_{(av, \text{diodes})} = \frac{D^2 + (D_a - 2)(D - 1)}{D^2 + (D_a - 3)D + 1 - D_a} P_o$$

Fig. 11 shows the comparisons of the average and peak SDPs of diodes and extra switch versus buck-boost factor $G$ between the proposed topology and five other topologies. From Figs. 11(a) and 11(b), the peak and average SDPs for extra switch of the proposed ASC-EqZSI topology are slightly higher than CSC-EB-ZSI, and lower than the other topologies. From Figs. 11(c) and 11(d), the peak SDP for diodes of the proposed ASC-EqZSI topology is slightly higher than the CC-qZSI, and the same as the CSC-EB-ZSI. The proposed ASC-EqZSI topology has the lowest average SDP for diodes.

D. COMPONENT STRESS FACTOR COMPARISON

The component stress factors (CSFs) in each component of the six topologies are compared. Based on the definition in [43], the total inductors’ winding CSF (WCSF), capacitors’ CSF (CCSF), diodes’ CSF (DSCF), and active switch’ CSF
TABLE 2. Comparison of voltage stresses across capacitors, diodes and switch, current stresses of inductors, diodes and switch, and ST current.

| Capacitor Voltage Stress Ratio | EB/AS-qZSI [20] | HB-ni-qZSI [21] | CSC-EB-ZSI [23] | CC-qZSI [24] | HGAS-qZSI [25] | ASC-EqZSI |
|-------------------------------|-----------------|-----------------|-----------------|--------------|--------------|-----------|
| $C_i$                         | $\sqrt{2}$      | $\sqrt{2}$      | $\sqrt{2}$      | $\sqrt{2}$   | $\sqrt{2}$   | $\sqrt{2}$ |
| $C_{ij}$                      | $1/D$           | $1/D$           | $1/D$           | $1/D$        | $1/D$        | $1/D$     |
| $\sum_{i} W_{i} V_{c(i)} / V_{c(m)}$ | $2\sqrt{2}$    | $3 \cdot 2D / \sqrt{2}$ | $2\sqrt{2}$    | $\sqrt{2}$   | $\sqrt{2}$   | $\sqrt{2}$ |
| Diode Voltage Stress Ratio    | $D_1$           | $\sqrt{2}$      | $D_1$           | $\sqrt{2}$   | $\sqrt{2}$   | $\sqrt{2}$ |
| $D_{ij}$                      | $1/D$           | $1/D$           | $1/D$           | $1/D$        | $1/D$        | $1/D$     |
| $\sum_{i} W_{i} V_{d(i)} / V_{d(m)}$ | $(D^2 - 3D + 2)$ | $(D^2 - 3D + 2)$ | $(D^2 - 3D + 2)$ | $(D^2 - 3D + 2)$ | $(D^2 - 3D + 2)$ | $(D^2 - 3D + 2)$ |
| Switch Voltage Stress Ratio   | $V_{S}$         | $\sqrt{2}$      | $V_{S}$         | $\sqrt{2}$   | $\sqrt{2}$   | $\sqrt{2}$ |
| $\sum_{i} W_{i} V_{s(i)} / V_{s(m)}$ | $1/D$           | $1/D$           | $1/D$           | $1/D$        | $1/D$        | $1/D$     |
| Inductor Current Stress Ratio | $L_i$           | $(1-D)^2$       | $L_i$           | $(1-D)^2$    | $(1-D)^2$    | $(1-D)^2$ |
| $\sum_{i} W_{i} \frac{2D L_i}{Bl_{s}}$ | $(D^2 - 2D - 2) Bl_{s}$ | $(D^2 - 2D - 2) Bl_{s}$ | $(D^2 - 2D - 2) Bl_{s}$ | $(D^2 - 2D - 2) Bl_{s}$ | $(D^2 - 2D - 2) Bl_{s}$ | $(D^2 - 2D - 2) Bl_{s}$ |
| Diode Current Stress Ratio    | $D_1$           | $(1-D)^2$       | $D_1$           | $(1-D)^2$    | $(1-D)^2$    | $(1-D)^2$ |
| $D_{ij}$                      | $1/D$           | $1/D$           | $1/D$           | $1/D$        | $1/D$        | $1/D$     |
| $\sum_{i} W_{i} \frac{1}{2D} V_{d(i)} / V_{d(m)}$ | $(1-D) / (2D)$ | $(1-D) / (2D)$ | $(1-D) / (2D)$ | $(1-D) / (2D)$ | $(1-D) / (2D)$ | $(1-D) / (2D)$ |
| Switch Current Stress Ratio   | $I_{s}$         | $(D^2 - 3D + 2)$ | $I_{s}$         | $(D^2 - 3D + 2)$ | $(D^2 - 3D + 2)$ | $(D^2 - 3D + 2)$ |
| $ST_{i}$                      | $(D^2 - 2D - 2) Bl_{s}$ | $(D^2 - 2D - 2) Bl_{s}$ | $(D^2 - 2D - 2) Bl_{s}$ | $(D^2 - 2D - 2) Bl_{s}$ | $(D^2 - 2D - 2) Bl_{s}$ | $(D^2 - 2D - 2) Bl_{s}$ |

(SCSF) of the proposed topology when $D_o = 2D$ are derived as

\[
W_{CSF} = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{L_{max}}^2 L_{rms}}{P_o^2} = 8 \times D^2 (3D - 1) \cdot (10D^2 - 26D + 17) / (3D^2 - 5D + 1)^2 \quad (24)
\]

\[
C_{CSF} = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{C_{pk}}^2 C_{rms}}{P_o^2} = 2D (9D^4 - 30D^2 + 36D^2 - 18D + 4) / (1 - D)(3D^2 - 5D + 1)^2 \quad (25)
\]

\[
D_{CSF} = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{D_{rms}}^2 D_{rms}}{P_o^2} = 2 \times (3D^4 - 16D^2 + 32D^2 - 18D + 4) / (1 - D)(3D^2 - 5D + 1)^2 \quad (26)
\]

\[
S_{CSF} = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{S_{rms}}^2 S_{rms}}{P_o^2} = \frac{D}{(3D^2 - 5D + 1)^2} \quad (27)
\]

where $W_i$ is the individual weight assigned to component $i$, and $\sum_j W_j$ is the sum of the individual weights for all components of the same type in the impedance network.

Based (24)-(27), the CSF comparison between the proposed ASC-EqZSI and five other topologies is shown in Fig. 12. As shown in Figs. 12(a) and 12(b), the inductors' WCSF and CCSF of the proposed ASC-EqZSI are slightly higher than the HGAS-qZSI. From Fig. 12(c), the proposed ASC-EqZSI has the lowest DCSF among six topologies. From Fig. 12(d), the extra switch' CSF of the proposed topology is higher than the ASC-EB-ZSI and nearly the same as the CC-qZSI.

E. POWER LOSS AND EFFICIENCY COMPARISON

The power losses of the proposed ASC-EqZSI using the PWM2 method are analyzed. For the proposed topology, the total power losses can be classified as the inductor losses, capacitor losses, conduction and switching losses of IGBT switches, and conduction and reverse recovery losses of diodes.

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The power loss in the inductors consists of the winding conduction loss and core loss. The core loss can be negligible compared with the total inductor losses. The winding conduction loss is dependent on the equivalent series resistance (ESR) of the inductor $r_I$, and rms value of the inductor current. Using the approximated rms value of the inductor currents from (12) and (13), the total inductor loss can be expressed as

$$P_{L,\text{loss}} = \frac{(1 - D)^2[(1 - D - D_a)^2 + 1]}{[D^2 + (D_a - 3)D + 1 - D_a]r_I}I_o^2 \cdot r_L. \quad (28)$$

By considering the ESRs of the two capacitors $r_{C1}$ and $r_{C2}$, the total power loss in the capacitors is expressed as

$$P_{C,\text{loss}} = \frac{D(1 - D)}{[D^2 + (D_a - 3)D + 1 - D_a]r_{C1}}I_o^2 \cdot \frac{(1 - D)^2(D + D_a)(D + D_a - 1)}{[D^2 + (D_a - 3)D + 1 - D_a]r_{C2}}. \quad (29)$$

The diode loss is divided into the conduction power loss and reverse recovery loss. The conduction power loss of diodes is dependent on the forward voltage drop $V_F$ and the on-resistance $r_D$. By neglecting the ripples of the inductor currents, the total conduction power loss of the two diodes can be derived as

$$P_{D,\text{cond}} = \frac{(1 - D)}{D^2 + (D_a - 3)D + 1 - D_a}I_o \cdot V_F + \frac{(1 - D)^2(2D^2 + 2D_aD - 2D + 1)}{[D^2 + (D_a - 3)D + 1 - D_a]^2}I_o^2 \cdot r_D. \quad (30)$$

The reverse recovery loss of the two diodes can be derived as

$$P_{D,rr} = (V_{C1} + V_{C2})Q_{rr}f_s + V_{C1}Q_{ns}f_s = \frac{3 - D}{D^2 + (D_a - 3)D + 1 - D_a}Q_{rr}f_s. \quad (31)$$

where $Q_{rr}$ is the reverse recovery charge of the diode.

The power loss of IGBT consists of the conduction power loss and switching power loss. The extra switch $S_0$ is turned on during the ST and NST2 time intervals. Therefore, the conduction and switching power losses of the extra switch $S_0$ are expressed as, respectively

$$P_{S0,\text{cond}} = V_{CE(sat)}\frac{(1 - D)(D + D_a)}{D^2 + (D_a - 3)D + 1 - D_a}I_o^2 \cdot r_{CE}$$

$$P_{S0,\text{sw}} = \frac{t_{on} + t_{off}}{2}f_sV_{CE}I_o \cdot I_2$$

$$= \frac{t_{on} + t_{off}}{2}f_s\frac{(1 - D)^2}{[D^2 + (D_a - 3)D + 1 - D_a]}V_{dc} \cdot I_o \quad (32)$$

where $V_{CE(sat)}$ and $r_{CE}$ represent an insulated gate bipolar transistor (IGBT) on-state collector-emitter voltage and collector-emitter on-state resistance, respectively, and $t_{on}$ and $t_{off}$ are the turn-on and turn-off times of IGBT, respectively.

The shoot-through current $i_{ST}$ flowing through inverter switches during ST state is

$$i_{ST} = \frac{(1 - D)(2 - D - D_a)}{D^2 + (D_a - 3)D + 1 - D_a}I_o. \quad (33)$$
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Using the shoot-through current $i_{ST}$, the average and rms values of the inverter switches’ currents can be expressed as

$$I_{s(avg)} = \frac{D}{2}i_{ST} + \frac{4(1-D)P_o}{MBV_{dc} \pi \cos \phi},$$

$$I_{s(rms)} = \frac{D^2}{4}i_{ST} + \frac{16(1-D)P_o^2}{MBV_{dc} \pi \cos \phi^2}.$$

where $\cos \phi$ is the power factor of the ac load side. Using (34) and (35), the conduction power loss and switching power loss of all inverter switches can be derived as follows:

$$P_{S,\text{cond}} = 4V_{CE(sat)}I_{s(avg)} + 4r_{CE}I_{s(rms)}^2,$$

$$P_{S,\text{sw}} = 4 \times \frac{t_{on} + t_{off}}{2} \frac{f_s}{2} \frac{i_{ST}}{V_{pm}} + \frac{t_{on} + t_{off}}{2} \frac{f_s}{2} \frac{D^2}{2} + \frac{D_v}{2} + \frac{D_u}{2} + \frac{D_a}{2} - \frac{D}{2}.$$

The efficiency and power losses of the proposed ASC-EqZSI using the PWM2 method are compared with the five other topologies using the PWM1 method without NST2 state ($D_a = 0$). To compare properly the efficiency and power losses for all of topologies, it is assumed that they all have the same ESRs of the inductors and capacitors. Also, the forward voltage drop and collector-emitter on-state resistance of IGBT switch, and the forward voltage drop and on-resistance of the diodes are the same for all compared topologies.

Fig. 13 depicts the efficiency versus output power of the proposed ASC-EqZSI and five other topologies. As shown in Fig. 13, compared with other topologies, the proposed ASC-EqZSI has a higher efficiency in the whole range of output power. Fig. 14 shows the comparison of the power losses of each component for the six topologies when the output power is 1 kW. It can be noted that the proposed ASC-EqZSI provides the lowest power losses of all components. The main reasons for reducing the power losses of the proposed ASC-EqZSI topology can be summarized as follows:

- The proposed topology requires fewer number of components in the impedance network.
- An additional NST2 state is included to achieve a higher voltage gain with a lower shoot-through duty cycle.
- The proposed PWM2 method can reduce the commutation counts of all switches and diodes in the proposed topology.

### VI. SIMULATION AND EXPERIMENTAL RESULTS

To validate the effectiveness of the proposed topology and PWM methods, both simulations and experiments are performed. The system parameters used at the simulations and experiments are given in Table 3.

#### A. SIMULATION RESULTS

To verify the theoretical analysis of the proposed topology and PWM methods, simulation is performed using the PSIM program. Fig. 15 shows the simulation results of the proposed ASC-EqZSI topology with the PWM2 method when $D = 0.2$, $M = 0.8$, and $D_a = 0.4$. As shown in Fig. 15, the capacitor voltages $V_{C1}$ and $V_{C2}$ are boosted to 225 V and 181 V, respectively, and the dc-link voltage can be boosted to 225 V from a dc input voltage of 30 V. The RMS (root means square) values of the ac output voltage and current are 127 V and 1.27 A, respectively. Fig. 16 shows the simulation results of the proposed ASC-EqZSI topology when two PWM methods are used under the same operating conditions as those used in Fig. 15. The dc-link voltage in the NST2 state is the same as that in the NST1 state. The commutation counts of the switch $S_2$ and diode $D_1$ under the PWM2 method are half those of the PWM1 method. The PWM2 method has a slightly higher current ripple on the inductor $L_2$, as compared to the PWM1 method.

#### B. EXPERIMENTAL RESULTS

The experiment is performed using a laboratory prototype, as shown in Fig. 17. The laboratory prototype consists of a single-phase inverter, impedance network, LC filter, resistive
load, and control board with a 32-bit DSP 320F28335 and field programmable gate array (FPGA) for generating PWM control signals.

Fig. 18 shows the experimental results of the ASC-EqZSI with the PWM2 method at the same operation conditions as the simulation results shown in Fig. 15. According to Fig. 18, the dc-link voltage can be boosted to 216 V, which is 7.2 times the dc input voltage of 30 V. The capacitor voltage $V_{C1}$ is equal to a peak dc-link voltage. The ac output voltage and the capacitor voltage $V_{C2}$ are stepped up to 123 Vrms and 174 V, respectively. Fig. 18(c) shows the experimental waveforms of the output voltage and current when the inductive load of 30 mH is appended with a load resistor of 50 Ω for the resistive-inductive load. Fig. 18(d) shows the dynamic responses for the ac output voltage and current, the capacitor voltage $V_{C1}$ when the load resistor decreases from 100 Ω to 50 Ω with the inductive load of 30 mH. When the load resistor decreases from 100 Ω to 50 Ω, the output current increases. Also, the capacitor voltage $V_{C1}$ and output voltage are slightly reduced due to increasing the voltage drop of the components in the proposed ASC-EqZSI.

Fig. 19 shows the experimental waveform of two inductor currents $i_{L1}$ and $i_{L2}$, dc-link voltage, and gating signal of switch $S_0$ with the PWM1 and PWM2 methods. The average values of $i_{L1}$ and $i_{L2}$ with the PWM1 method are 3.93 A and 9.85 A, respectively. The average values of $i_{L1}$ and $i_{L2}$ with the PWM2 method are 4.03 A and 9.65 A, respectively. The current ripple of inductor $L_2$ with the PWM2 method is slightly higher than that with the PWM1 method. The current of inductor $L_2$ is the input current, which is continuous. The switch $S_0$ is switched on during both ST and NST2 states.

Fig. 20 shows the PWM signals of switches $S_1$, $S_2$, $S_3$, and $S_0$ with the PWM1 and PWM2 methods when the reference signal is positive. The ST signal $S_{ST}$ is inserted into the PWM signal $S_1$ to generate the ST state. The PWM2 method can reduce the commutation count of the two switches $S_1$, $S_0$ by half, as compared to the PWM1 method.
The proposed PWM2 method can reduce the commutation count of all switches and diodes in the ASC-EqZSI topology by 40% and 34%, respectively. Thus, the efficiency of the ASC-EqZSI with the PWM2 method is 2-3% higher than that with the PWM1 method due to reduction of switching loss. The PWM signals are generated by a simple logic circuit with one carrier signal.

Through the comparative analysis between the proposed topology with the PWM2 method and five state-of-the-art topologies, the proposed topology with the PWM2 method has the highest boost factor and ac voltage gain with the fewest components in the impedance network by increasing the NST2 time interval. It also provides the lowest inductor current stress and ST current, and the voltage stresses across the diodes and switch in the comparatively intermediate range, although it suffers from the highest capacitor voltage stress. Additionally, the proposed ASC-EqZSI leads to the higher efficiency in the whole range of the output power.

As demonstrated by the experiments using a prototype built in the laboratory, the dc-link voltage is stepped up to 216 V, and the inverter produces a line-to-line output voltage of 123 Vrms from a dc input voltage of 30 V when \( D = 0.2, M = 0.8, \) and \( D_a = 0.4 \). The THD of the ac output voltage filtered by an LC filter is 1.36%.

![Fig. 19. Experimental results of ASC-EqZSI when \( D = 0.2, M = 0.8, \) and \( D_a = 0.4 \): (a) PWM1 method, (b) PWM2 method.](image1.png)

![Fig. 20. Experimental results of PWM signals when \( D = 0.2, M = 0.8, \) and \( D_a = 0.4 \): (a) PWM1 method, (b) PWM2 method.](image2.png)

![Fig. 21. Experimental results of the frequency spectrum of filtered output voltage and diode voltages with the PWM2 method when \( D = 0.2, M = 0.8, \) and \( D_a = 0.4 \): (a) FFT analysis of output voltage, (b) two diode voltages.](image3.png)

Fig. 21(a) shows the frequency spectrum of the ac output voltage filtered by an LC filter with the PWM2 method. The THD of the ac output voltage filtered by an LC filter, as calculated from Fig. 21(a), is 1.36%. The experimental waveform of the two diode voltages \( V_{D1} \) and \( V_{D2} \) is shown in Fig. 21(b). The reverse voltages across the two diodes \( D_1 \) and \( D_2 \) during the ST state are \( (V_{C1} + V_{C2}) \) and \( V_{C1} \), respectively.

### VII. CONCLUSION

In this paper, a single-phase active switched-capacitor embedded quasi-Z-source inverter (ASC-EqZSI) and two PWM methods for the proposed ASC-EqZSI topology are proposed. The proposed PWM1 method can considerably increase the boost factor with fewer components in the impedance network by using an additional operating state referred to as NST2 state. The boost factor can be increased by increasing the NST2 time interval besides the ST time interval. The proposed PWM2 method can reduce the

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