Abstract—Quantum circuits of arithmetic operations such as addition are needed to implement quantum algorithms in hardware. Quantum circuits based on Clifford+T gates are used as they can be made tolerant to noise. The tradeoff of gaining fault tolerance from using Clifford+T gates and error correcting codes is the high implementation overhead of the T gate. As a result, the T-count performance measure has become important in quantum circuit design. Due to noise, the risk for errors in a quantum circuit computation increases as the number of gate layers (or depth) in the circuit increases. As a result, low depth circuits such as quantum carry lookahead adders (QCLAs) have caught the attention of researchers. This work presents two QCLA designs each optimized with emphasis on T-count or qubit cost respectively. In-place and out-of-place versions of each design are shown. The proposed QCLAs are compared against the existing works in terms of T-count. The proposed QCLAs for out-of-place addition achieve average T gate savings of 54.34% and 37.21%, respectively. The proposed QCLAs for in-place addition achieve average T gate savings of 72.11% and 35.87% respectively.

I. INTRODUCTION

Quantum circuits of arithmetic operations are needed to design quantum hardware for implementing quantum algorithms such as integer factoring, searching and quantum mechanical simulation. Quantum circuits for addition are fundamental building blocks crucial to implementing these quantum algorithms [1] [2] [3] [4] [5]. Thus, researchers have invested considerable effort in designing quantum adders such as ripple carry adders or carry lookahead adders (QCLAs) [6] [7] [8] [9] [10] [11].

Quantum circuits possess properties that make them distinct from circuits for other technologies. For example, there is a one-to-one relationship between the inputs and outputs in a quantum circuit. As a result, the quantum circuit designer will face additional sources of circuit overhead such as ancillae and garbage output. Ancillae are constant inputs to the quantum circuit. Garbage output are any circuit output that is not a circuit input or needed output. To make full use of the qubit resources of the quantum machine, the garbage output will need to be cleared. This process will add to the overall qubit cost and gate cost of a quantum circuit and is discussed in [12].

Physical quantum computers are prone to noise errors [14] [15]. Quantum circuits based on Clifford+T gates have caught the attention of researchers because they perform the addition operation in order $O(\log(n))$ circuit depth (while the ripple carry adder has a depth of $O(n)$). Low-depth circuits such as QCLAs have use in quantum hardware applications where longer computation time increases the risk of errors [24] [25] [26]. Several QCLA designs have been proposed in the literature such as [27] or [8]. Designs that replace one of the primary inputs with the sum (or qubit cost respectively . In-place and out-of-place versions of each design are shown. The proposed QCLAs are compared against the existing works in terms of T-count. The proposed QCLAs for out-of-place addition achieve average T gate savings of 54.34% and 37.21%, respectively. The proposed QCLAs for in-place addition achieve average T gate savings of 72.11% and 35.87% respectively.

TABLE I: Details of Existing Out-of-Place QCLAs

| Design             | T-count | qubits | gates used | garbage? |
|--------------------|---------|--------|------------|-----------|
| Draper et al.      | $O(35 \cdot n)$ | $O(4 \cdot n)$ | CNOT, Toffoli | no        |
| Baba et al.*       | $O(54 \cdot n)$ | $O(12 \cdot n)$ | PFA, CNOT, MIG, NFT | yes       |
| Trisovsno et al.   | $O(35 \cdot n)$ | $O(4 \cdot n)$ | CNOT, Toffoli, Hadamard, DCZ | no        |
| Lisa et al.*       | $O(26 \cdot n)$ | $O(6 \cdot n)$ | CNOT, RPA, Fredkin | yes       |
| Thapliyal et al.   | $O(35 \cdot n)$ | $O(4 \cdot n)$ | CNOT, Toffoli, Fredkin | no        |

* The PFA gate decomposes into two V gates, a V+ gate and six CNOT gates. Each V gate and V+ gate has a T-count of 3. [29] [33] [13]
2 The MIG gate decomposes into two V gates, a V+ gate and four CNOT gates. [13]
3 The NFT gate decomposes into two V gates, a V+ gate and seven CNOT gates. [23]
4 The DCZ or double controlled Z gate has a T-count of seven. [35]
5 The RPA gate decomposes into a V gate, a V+ gate and three CNOT gates. [33]
6 The Fredkin gate has a T-count of seven. [13]
7 The Fredkin gate has a T-count of seven. [13]
8 T-count and qubit cost are for the circuit after being modified to remove garbage output. We use the methodology outlined in [13] to remove the garbage outputs.
To overcome shortcomings in existing works, this work proposes a family of designs for QCLAs. The first design (FT-QCLA1) is optimized with an emphasis on T-count. The second design (FT-QCLA2) is optimized with an emphasis on number of qubits. All proposed designs enjoy reduced T gate cost and qubit cost compared to the existing works. In-place QCLA implementations (In-FT-QCLA1 and In-FT-QCLA2) and out-of-place QCLA implementations (Out-FT-QCLA1 and Out-FT-QCLA2) for each design are shown. All proposed QCLAs can be made fault tolerant with error correcting codes. The proposed QCLA designs are based on the NOT gate, CNOT gate, Toffoli gate, logical AND gate and uncomputation gate.

This work is organized as follows: Section II provides background on the Clifford+T quantum gate set, introduces the logical AND gate and the uncomputation gate. Section III presents the proposed out-of-place QCLAs. Each design (Out-FT-QCLA1 and Out-FT-QCLA2) is addressed in its own subsection within Section III. Section IV illustrates the comparison of the proposed out-of-place QCLAs against existing out-of-place QCLAs. Section V presents the proposed in-place QCLAs. Each design (In-FT-QCLA1 and In-FT-QCLA2) is addressed in its own subsection within Section V. Section VI illustrates the comparison of the proposed in-place QCLAs against existing in-place QCLAs. Section VII provides a review of the existing work in quantum carry lookahead addition.
Algorithm 1: Carry lookahead Addition

Function CLA(a, b)

Requirements:

//Takes 2 n bit values a and b as input.
//Returns the sum as an n + 1 bit number s.
1 //create carry generate and carry propagate bits.
2 For i = 0 to n - 1
3 pi = ai ⊕ bi
4 gi = ai ∧ bi
5 End
6 //synthesize sum.
7 c0 = g0 //no carry-in
8 s0 = p0
9 For i = 1 to n - 1
10 ci = pi-1 ∧ ci-1 ∨ gi-1
11 si = ci ⊕ ai ⊕ bi
12 End
13 sn = pn-1 ∧ cn-1 ∨ gn-1
14 Return s

III. PROPOSED DESIGNS OF OUT-OF-PLACE QCLA CIRCUITS

We now show our proposed out-of-place QCLA circuits. The proposed QCLA circuits have lower T-count and qubit cost than existing works. The QCLA designs save T gates by using the temporary logical-AND gate, the existing uncomputation gate or proposed uncomputation gate where possible. The out of place FT-QCLA1 (or Out-FT-QCLA1) is optimized for T-count. We also propose an out of place FT-QCLA2 (or Out-FT-QCLA2) which is optimized for qubit cost. The design methodologies of the proposed QCLAs are generic and each can be used to implement a QCLA circuit of any size.

Given two n bit inputs a and b, the CLA circuit generates the sum of a and b by executing the CLA algorithm illustrated in Figure 4. The CLA algorithm is an established technique to quickly perform addition [40, 41]. The CLA algorithm can be divided into two basic steps: (i) implement generate (gi) and propagate bits (pi) for each bit of the inputs a and b and (ii) compute the sum s by computing ci+1 = pi ∧ ci ∨ gi for 1 ≤ i ≤ n.
reuse as ancillae.

This Section is organized as follows: The proposed design of Out-FT-QCLA1 is shown in Section III-A. The proposed design of Out-FT-QCLA2 is shown in Section III-B.

A. Proposed Out-of-Place FT-QCLA Design (Out-FT-QCLA1)

The out-of-place FT-QCLA1 (Out-FT-QCLA1) is optimized for T-count. The proposed QCLA is based on the quantum NOT gate, CNOT gate, logical AND gate and uncomputation gate. The steps of the proposed design methodology to realize Out-FT-QCLA1 are shown along with an illustrative example of the QCLA circuit in Figure 5.

- **Step 1:** For \( i = 0 \) to \( n-1 \), apply the logical AND gate at locations \( A[i] \) and \( B[i] \) and an ancillae such that locations \( A[i] \) and \( B[i] \) are unchanged. The ancillae will have the result of computation. The ancillae will be renamed to the value \( g[i, i+1] \).
- **Step 2:** For \( i = 1 \) to \( n-1 \), at the locations \( A[i] \) and \( B[i] \) apply a CNOT gate such that \( A[i] \) is unchanged and location \( B[i] \) will have the result of computation. Location \( B[i] \) will be renamed \( p[i, i+1] \).
- **Step 3 (P-rounds):** We use a nested loop in this step. For \( i = 1 \) to \( \lfloor \log(n) \rfloor - 1 \) and for \( m = 1 \) to \( \lfloor \frac{m}{\log(n)} \rfloor - 1 \): At locations \( p[j, l] \), \( p[l, k] \), and an ancillae apply a logical AND gate such that locations \( p[j, l] \) and \( p[l, k] \) are unchanged and the ancillae will have the result of computation. The ancillae will be renamed \( p[j, k] \). The equation for indexes are \( j = 2^i \cdot m, k = 2^i \cdot m + 2^j \), and \( l = 2^i \cdot m + 2^j \), respectively.
- **Step 4 (G-rounds):** We use a nested loop in this step. For \( i = 1 \) to \( \lfloor \log(n) \rfloor \) and for \( m = 0 \) to \( \lfloor \frac{m}{\log(n)} \rfloor - 1 \): At locations \( g[j, l] \), \( p[l, k] \), and \( g[l, k] \) apply a Logical AND gate and uncomputation gate pair such that locations \( g[j, l] \) and \( p[l, k] \) are unchanged and location \( g[l, k] \) will have the result of computation. Location \( g[l, k] \) is renamed to \( g[j, k] \). The equation for indexes are \( j = 2^i \cdot m, k = 2^i \cdot m + 2^j \), and \( l = 2^i \cdot m + 2^j \), respectively.
- **Step 5 (C-rounds):** We use a nested loop in this step. For \( i = \lfloor \log(\frac{m}{n}) \rfloor \) to 1 and for \( m = 1 \) to \( \lfloor \frac{m}{\log(\frac{m}{n})} \rfloor \) : At locations \( g[0, l] \), \( p[l,k] \), and \( g[l,k] \) apply a Logical AND gate and uncomputation gate pair such that locations \( g[0, l] \) and \( p[l,k] \) are unchanged and location \( g[l,k] \) will have the result of computation. The equation for indexes are \( l = 2^i \cdot m \) and \( k = 2^i \cdot m + 2^j \).
- **Step 6 (P-erase-rounds):** We use a nested loop in this step. For \( i = \lfloor \log(n/2) \rfloor - 1 \) to 1 and for \( m = 1 \) to \( \lfloor \frac{m}{\log(n/2)} \rfloor \) - 1: At locations \( p[j, l] \), \( p[l, k] \), and \( p[j, k] \) apply a uncomputation gate such that locations \( p[j, l] \) and \( p[l,k] \) are unchanged and location \( p[j, k] \) will be restored to its original value. The equation for indexes are \( j = 2^i \cdot m, k = 2^i \cdot m + 2^j \), and \( l = 2^i \cdot m + 2^j \).
- **Step 7:** This step has two sub-steps:
  - **Sub-step 1:** For \( i = 1 \) to \( n-1 \), at locations \( p[i, i+1] \) and \( g[0, i] \) apply a CNOT gate such that location \( p[i, i+1] \) is unchanged and \( g[0, i] \) has the result of computation. After this step, location \( g[0, i] \) will have the sum bit \( s_i \). The sum bit \( s_n \) is at location \( g[0, n] \).
  - **Sub-step 2:** At locations \( p[0, l] \) and an ancillae apply a CNOT gate such that location \( p[0, l] \) and the ancillae will have the value \( B[0] \).
- **Step 8:** This step has two sub-steps:
  - **Sub-step 1:** For \( i = 1 \) to \( n-1 \), at locations \( p[i, i+1] \) and \( A[i] \) apply a CNOT gate such that \( A[i] \) is unchanged and \( p[i, i+1] \) is restored to its original value (\( b_i \)).

Fig. 5: Proposed out-of-place FT-QCLA1 (Out-FT-QCLA1) circuit for the case of adding two 8 bit values \( a \) and \( b \).
B. Proposed Out-of-Place FT-QCLA2 Design (Out-FT-QCLA2)

Out-FT-QCLA2 is optimized for qubit cost. A trade-off for the reduced qubit count is an increase in the T gate cost of Out-FT-QCLA2. We reduce the qubit cost by replacing logical AND gate and uncomputation gate pairs with alternative Toffoli gate implementations such as the design in [18] were appropriate. To retain a low T-count, Out-FT-QCLA2 does still incorporate logical AND gate and uncomputation gate pairs. We save qubits because the logical AND gate and uncomputation gate pairs have a qubit cost of 4 while implementations of the Toffoli gate (like the design in [18]) have a qubit cost of 3. However, alternative Toffoli gate implementations have higher T-counts (such as the design in [18] with a T-count of 7). The design methodology for Out-FT-QCLA2 is identical to the methodology for Out-FT-QCLA1 except Step 4 and Step 5. In Step 4 and Step 5, Toffoli gates based on the design in [18] are used. An illustrative example of Out-FT-QCLA2 is in Figure 6.

IV. PERFORMANCE OF PROPOSED OUT-OF-PLACE QCLA CIRCUITS

A. T-count analysis of Out-FT-QCLA-1

The T-count of Out-FT-QCLA-1 is shown for each Step of the proposed design methodology. Total T-count is determined by summing the T-count for each Step of the proposed design methodology. This design uses logical AND gate and uncomputation gate pairs to implement the Toffoli gate as shown in [19] and [23]. The pair has a T-count of 4. The total T-count is 16 · n − 8 · w(n) − 8 · ⌊log(n)⌋ − 4 where w(n) = n − ∑y=1[log(y)].

- Step 1 uses n logical AND gates. The T-count for this step is 4 · n.
- Step 2 does not need T gates.
- Step 3 uses n − w(n) − ⌊log(n)⌋ logical AND gates. The T-count for this step is 4 · (n − w(n) − ⌊log(n)⌋).
- Step 4 uses n − w(n) logical AND gate and uncomputation gate pairs. The T-count for this step is 4 · (n − w(n)).
- Step 5 uses n − ⌊log(n)⌋ − 1 logical AND gate and uncomputation gate pairs. The T-count for this step is 4 · (n − [log(n)] − 1).
- Steps 6 through 8 does not need T gates.

B. T-count analysis of Out-FT-QCLA-2

The T-count of Out-FT-QCLA-2 is shown for each Step of the proposed design methodology. Total T-count is determined by summing the T-count for each Step of the proposed design methodology. This design uses the Toffoli gate implementation in [18] which has a T-count of 7. The total T-count is 22 · n − 11 · w(n) − 11 · [log(n)] − 7 where w(n) = n − ∑y=1[log(y)].

- Step 1 uses n logical AND gates. The T-count for this step is 4 · n.
- Step 2 does not need T gates.
- Step 3 uses n − w(n) − [log(n)] logical AND gates. The T-count for this step is 4 · (n − w(n) − [log(n)]).
- Step 4 uses n − w(n) Toffoli gates. The T-count for this step is 7 · (n − w(n)).
- Step 5 uses n − [log(n)] − 1 Toffoli gates. The T-count for this step is 7 · (n − [log(n)] − 1).
- Steps 6 through 8 does not need T gates.

C. Cost Comparison of Proposed Out-of-place QCLAs

1) Cost Comparison in Terms of T-count: Table I indicates that all proposed out-of-place QCLAs have T-count costs of order O(n). The existing works also have T-counts of order O(n). All proposed QCLAs have a reduced T-count compared to the existing work. Of the proposed QCLAS, Out-FT-QCLA1 requires the fewest T gates.

The Out-FT-QCLA1 requires roughly 70.37% fewer T gates than the design by Babu et al., 38.46% fewer T gates than the design by Lisa et al., 54.29% fewer T gates than the designs by Draper et al., Thapliyal et al. and Trisetyarso et al.

The proposed Out-FT-QCLA2 requires 59.26% fewer T gates than the design by Babu et al., 15.38% fewer T gates than the design by Lisa et al., 37.14% fewer T gates than the designs by Draper et al., Thapliyal et al. and Trisetyarso et al.
TABLE III: Cost Comparison of out-of-place QCLAs

| Design                  | T-count Equation | Qubit Equation |
|-------------------------|------------------|----------------|
| Draper et al. (12)      | $35n - 21w(n) - 21 [\log(n)] - 7$ | $4n - w(n) - \lfloor \log(n) \rfloor + 1$ |
| Trisetyarso et al. (30) | $35n - 21w(n) - 21 [\log(n)] - 7$ | $4n - w(n) - \lfloor \log(n) \rfloor + 1$ |
| Thapliyal et al. (34)   | $35n - 14$       | $4n + 1$       |
| Babu et al. (29)        | $54 \cdot n$     | $12 \cdot n + 1$ |
| Lisa et al. (23)        | $26 \cdot n$     | $6 \cdot n + 1$ |
| Out-FT-QCLA1            | $16n - 8w(n) - 8 [\log(n)] - 4$ | $6n - 2w(n) - 2 [\log(n)]$ |
| Out-FT-QCLA2            | $22n - 11w(n) - 11 [\log(n)] - 7$ | $4n - w(n) - \lfloor \log(n) \rfloor + 1$ |

$w(n) = n - \sum_{v=1}^{\infty} \lfloor \frac{n}{2^v} \rfloor$

1. Circuits modified to remove garbage output. We use the methodology in [12] to remove the garbage output.
2. Out-FT-QCLA1 is optimized emphasizing T-count.
3. Out-FT-QCLA2 is optimized emphasizing qubit cost.

2) Cost Comparison in Terms of Qubits: Table III indicates that all proposed out-of-place QCLAs have qubit costs of order $O(n)$. The existing works also have a T-count of order $O(n)$. Out-FT-QCLA1 requires $2 \cdot n + w(n) + [\log(n)] - 1$ additional ancillae compared to Out-FT-QCLA2. The added qubit cost of Out-FT-QCLA1 illustrates the trade-off between qubits and T gates that occurs when logical AND gate and uncomputation gate pairs are replaced by Toffoli gates in the QCLA implementation.

Out-FT-QCLA2 requires $w(n) + [\log(n)]$ fewer qubits than the design by Thapliyal et al. and has the same qubit cost as the designs by Draper et al. and Trisetyarso et al. Furthermore, the proposed Out-FT-QCLA2 requires $8 \cdot n + w(n) + [\log(n)]$ fewer qubits than the design by Babu et al. and $2 \cdot n + w(n) + [\log(n)]$ fewer qubits than the design by Lisa et al. In contrast, the out-of-place Out-FT-QCLA1 requires $6 \cdot n + 2 \cdot w(n) + 2 \cdot [\log(n)] + 1$ fewer qubits than the design by Babu et al. and $2 \cdot w(n) + 2 \cdot [\log(n)] + 1$ fewer qubits than the work by Lisa et al.

V. PROPOSED IN-PLACE QCLA CIRCUITS

We now show our proposed in-place quantum carry lookahead (QCLA) circuits. The proposed QCLA circuits have lower T-count and qubit costs than existing works. The proposed in-place FT-QCLA1 (or In-FT-QCLA1) and the proposed in-place FT-QCLA2 (or In-FT-QCLA2) save T gates by using the temporary logical-AND gate and uncomputation gate where possible. In-FT-QCLA2 is optimized for qubit cost and the In-FT-QCLA1 is optimized for T gates. The methodologies of the proposed in-place QCLAs are generic and each can be used to implement a QCLA circuit of any size.

The proposed QCLA circuits operate as follows: Given 2 values $a$ and $b$ (each $n$ bits wide) stored in quantum registers $A$ and $B$ and an $n$ bit register $Z$ of ancillae set to $a$ and $b$, respectively. Lastly, $\text{In-FT-QCLA2 QCLA}$ requires a $n - w(n) - [\log(n)]$ (where $w(n) = n - \sum_{v=1}^{\infty} \lfloor \frac{n}{2^v} \rfloor$) and is the number of ones in the binary expansion of $n$) bit register of ancillae $X$ set to $\lfloor \frac{n}{2^v} \rfloor$. In contrast, register $X$ of the In-FT-QCLA1 has $3 \cdot n - 2 \cdot w(n) - 2 \cdot [\log(n)]$ ancillae set to $A$. At the end of computation, $A$ is restored to its initial values and $B$ will contain sum bits $0$ through $n - 1$ of the addition of $a$ and $b$. For each QCLA, the end of computation, $Z$ will contain the sum bit $s_n$ and the remaining locations in $Z$ are transformed into a register of classical states. These qubits can be restored to initial values for reuse as ancillae. In-FT-QCLA1 and In-FT-QCLA2 will transform the remaining locations in $X$ to a register of classical states. These qubits can be restored to initial values for reuse as ancillae. This Section is organized as follows: In-FT-QCLA1 is shown in Section V-A The In-FT-QCLA2 is shown in Section V-B

A. Methodology of the Proposed In-Place FT-QCLA1 (In-FT-QCLA1)

The T gate optimized fault tolerant QCLA is targeted for quantum hardware that can support the resource requirements needed for fault tolerant quantum computation. Because of the high implementation cost of the fault tolerant T gate, this QCLA is optimized for T-count. The proposed QCLA is based on the quantum NOT gate, CNOT gate, logical AND gate and the uncomputation gate presented in [23]. The steps of the methodology to implement the proposed In-FT-QCLA1 are shown along with an illustrative example of the QCLA circuit in Figure 7

- **Step 1:** For $i = 0$ to $n-1$, apply the logical AND gate at locations $A[i]$ and an ancillae $X$ such that locations $A[i]$ and $B[i]$ are unchanged. The ancillae will have the result of computation. The ancillae will be renamed to the value $g[i, i + 1]$.

- **Step 2:** For $i = 1$ to $n-1$: At locations of $A[i]$ and $B[i]$ apply a CNOT gate such that locations $A[i]$ is unchanged and location $B[i]$ will have the result of computation. Location $B[i]$ is renamed to the value $p[i, i + 1]$.

- **Step 3 (P-rounds):** We use a nested loop in this step. For $l = 1$ to $[\log(n)] - 1$ and For $m = 1$ to $[\frac{n}{2^l}] - 1$: At locations $p[j, l]$, $p[l, k]$ and an ancillae apply a logical AND gate such that locations $p[j, l]$ and $p[l, k]$ are unchanged. The ancillae will have the result of computation and will be renamed to the value $p[j, k]$. The equations for the indexes are $j = 2^l \cdot m$, $k = 2^l \cdot m + 2^l$ and $l = 2^l \cdot m + 2^l - 1$.

- **Step 4 (G-rounds):** We use a nested loop in this step. For $l = 1$ to $[\log(n)]$ and For $m = 0$ to $[\frac{n}{2^l}] - 1$: At locations $g[j, l]$, $p[l, k]$, and $g[l, k]$ apply a Toffoli gate such that locations $g[j, l]$ and $p[l, k]$ pass through unchanged. Location $g[l, k]$ holds the result of computation
We use a nested loop in this step. For $i = 1$ to $n-1$: at locations $p[i, i + 1]$ and $g[0, i]$ apply a CNOT gate such that location $g[0, i]$ is unchanged. Location $p[i, i + 1]$ will have the result of computation.

**Step 8**: This step has the following two sub-steps:

- **Sub-step 1**: At location $B[0]$ apply a NOT gate. The location $B[0]$ will be renamed to the value $p[0, 1]$.
- **Sub-step 2**: For $i = 1$ to $n-2$: At location $p[i, i + 1]$ apply a NOT gate.

**Step 9**: For $i = 1$ to $n-2$: At locations $A[i]$ and $p[i, i + 1]$ apply the CNOT gate such that location $A[i]$ is unchanged and $p[i, i + 1]$ has the result of computation.

**Step 10** (Reverse of P-erase-rounds): We use a nested loop in this step. For $t = 1$ to $\lfloor \log(\frac{n}{2^m}) \rfloor - 1$ and For $m = 1$ to $\lfloor \frac{n-2^{t-1}}{2} \rfloor$:

At locations $p[i, l]$, $p[l, k]$ and an ancillae apply a logical AND gate such that locations $p[i, l]$ and $p[l, k]$ are unchanged. The ancillae will hold the result of computation and the ancillae is renamed to the value $p[j, k]$. The equations for the indexes are $j = 2^t \cdot m$, $k = 2^t \cdot m + 2^t$, and $l = 2^t \cdot m + 2^{t-1}$.

**Step 11** (Reverse of C-rounds): We use a nested loop in this step. For $t = 1$ to $\lfloor \log(\frac{n}{2^m}) \rfloor$ and For $m = 1$ to $\lfloor \frac{n-2^{t-1}}{2} \rfloor$:

At locations $g[0, l]$, $p[l, k]$ and $g[0, k]$ apply a Toffoli gate such that locations $g[0, l]$ and $p[l, k]$ are unchanged. Location $g[0, k]$ will have the result of computation and the location will be renamed to the value $g[l, k]$. The equations for the indexes are $l = 2^t \cdot m$ and $k = 2^t \cdot m + 2^{t-1}$.

**Step 12** (Reverse of G-rounds): We use a nested loop in this step. For $t = \lfloor \log(n) \rfloor$ to 1 and For $m = 0$ to $\lfloor \frac{n}{2^m} \rfloor - 1$:

At locations $g[j, l]$ and $p[l, k]$ and $g[j, k]$ apply a Toffoli gate such that locations $g[j, l]$ and $p[l, k]$ are unchanged. Location $g[j, k]$ will have the result of computation and the location is renamed to the value $g[l, k]$. The equations for the indexes are $j = 2^t \cdot m$, $k = 2^t \cdot m + 2^t$ and $l = 2^t \cdot m + 2^{t-1}$.

**Step 13** (Reverse of P-rounds): We use a nested loop in this step. For $t = \lfloor \log(n) \rfloor - 1$ to 1 and For $m = 1$ to $\lfloor \frac{n-2^{t-1}}{2} \rfloor$:

At locations $p[j, l]$, $p[j, k]$ and $p[l, k]$ apply an uncomputation gate such that locations $p[j, l]$ and $p[l, k]$ are unchanged. Location $p[j, k]$ will be restored to its original value. The equations for the indexes are $j = 2^t \cdot m$, $k = 2^t \cdot m + 2^t$ and $l = 2^t \cdot m + 2^{t-1}$.

**Step 14**: For $i=1$ to $n-2$: At locations $A[i]$ and $p[i, i + 1]$, apply a CNOT gate such that location $A[i]$ would be unchanged and location $p[i, i + 1]$ will have the result of computation.

**Step 15**: For $i=0$ to $n-2$: at locations $A[i]$, $p[i, i + 1]$, and $g[i, i + 1]$, apply an uncomputation gate such that locations $a[i]$ and $p[i, i + 1]$ are unchanged and $g[i, i + 1]$ will be restored to its original value.

**Step 16**: Location $p[n-1, n]$ has the sum bit $s_{n,1}$ and $g[0,$
\[ n \] has the sum bit \( s_r \). For \( i = 0 \) to \( n-2 \): At location \( p[i, i+1] \) apply a NOT gate. Location \( p[i, i+1] \) will have the sum bit \( s_i \).

### B. Proposed In-Place FT-QCLA2 Design (In-FT-QCLA2)

In-FT-QCLA1 is optimized for T-count. A trade-off for the reduced T-count of In-FT-QCLA1 is an increase in the qubit cost of In-FT-QCLA1. We can reduce the qubit cost by replacing logical-AND gate and uncomputation gate pairs with alternative Toffoli gates implementations (such as the design in [18]) where appropriate. We save qubits because the logical AND gate and uncomputation gate pairs have a qubit cost of 4 while implementations like the design in [18] have a qubit cost of 3. However, alternative Toffoli gate implementations have higher T-counts (such as the design in [18] with a T-count of 7).

The steps of the methodology to implement In-FT-QCLA2 are identical to the methodology to implement In-FT-QCLA1. To implement In-FT-QCLA2, replace the logical AND gate, uncomputation gate pairs with a Toffoli gate in Step 4, Step 5, Step 11 and Step 12. An illustrative example of the In-FT-QCLA2 circuit is in Figure 8.

![In-FT-QCLA2 Circuit](image)

**Fig. 8:** In-place FT-QCLA2 (In-FT-QCLA2) for the case of adding two 8 bit values \( a \) and \( b \).

### VI. Performance of Proposed In-place QCLA Circuits

#### A. T-count analysis of In-FT-QCLA1

The T-count of In-FT-QCLA1 is shown for each Step of the proposed design methodology. Total T-count is determined by summing the T-count for each Step of the proposed design methodology. The total T-count is \( 20 \cdot n - 8 \cdot w(n) - 4 \cdot \left[ \log(n) \right] - 8 \cdot w(n-1) - 4 \cdot \left[ \log(n-1) \right] - 8 \) where \( w(n) = n - \sum_{y=1}^{\infty} \left\lfloor \frac{n}{2^y} \right\rfloor \).

- **Step 1** uses \( n \) logical AND gates. The T-count for this step is \( 4 \cdot n \).
- **Step 2** does not need T gates.
- **Step 3** uses \( n - w(n) - \left[ \log(n) \right] \) logical AND gates. The T-count for this step is \( 4 \cdot (n - w(n) - \left[ \log(n) \right]) \).
- **Step 4** uses \( n - w(n) \) Toffoli gates. The T-count for this step is \( 4 \cdot (n - w(n)) \).
- **Step 5** uses \( n - \left[ \log(n) \right] - 1 \) Toffoli gates. The T-count for this step is \( 4 \cdot (n - \left[ \log(n) \right] - 1) \).
- **Steps 6 through 9** does not need T gates.
- **Step 10** uses \( n - 1 - w(n-1) - \left[ \log(n-1) \right] \) logical AND gates. The T-count for this step is \( 4 \cdot (n - 1 - w(n-1) - \left[ \log(n-1) \right]) \).
- **Step 11** uses \( n - \left[ \log(n-1) \right] - 2 \) Toffoli gates. The T-count for this step is \( 4 \cdot (n - \left[ \log(n-1) \right] - 2) \).
- **Step 12** uses \( n - 1 - w(n-1) \) Toffoli gates. The T-count for this step is \( 4 \cdot (n - 1 - w(n-1)) \).
- **Steps 13 through 16** does not need T gates.

#### B. T-count analysis of In-FT-QCLA2

The T-count of In-FT-QCLA2 is shown for each Step of the proposed design methodology. Total T-count is determined by summing the T-count for each Step of the proposed design methodology. The total T-count is \( 40 \cdot n - 11 \cdot w(n) - 11 \cdot \left[ \log(n) \right] - 11 \cdot w(n-1) - 11 \cdot \left[ \log(n-1) \right] - 32 \) where \( w(n) = n - \sum_{y=1}^{\infty} \left\lfloor \frac{n}{2^y} \right\rfloor \).

- **Step 1** uses \( n \) logical AND gates. The T-count for this step is \( 4 \cdot n \).
- **Step 2** does not need T gates.
- **Step 3** uses \( n - w(n) - \left[ \log(n) \right] \) logical AND gates. The T-count for this step is \( 4 \cdot (n - w(n) - \left[ \log(n) \right]) \).
- **Step 4** uses \( n - w(n) \) Toffoli gates. The T-count for this step is \( 7 \cdot (n - w(n)) \).
- **Step 5** uses \( n - \left[ \log(n) \right] - 1 \) Toffoli gates. The T-count for this step is \( 7 \cdot (n - \left[ \log(n) \right] - 1) \).
- **Steps 6 through 9** does not need T gates.
- **Step 10** uses \( n - 1 - w(n-1) - \left[ \log(n-1) \right] \) logical AND gates. The T-count for this step is \( 4 \cdot (n - 1 - w(n-1) - \left[ \log(n-1) \right]) \).
- **Step 11** uses \( n - \left[ \log(n-1) \right] - 2 \) Toffoli gates. The T-count for this step is \( 7 \cdot (n - \left[ \log(n-1) \right] - 2) \).
- **Step 12** uses \( n - 1 - w(n-1) \) Toffoli gates. The T-count for this step is \( 7 \cdot (n - 1 - w(n-1)) \).
- **Steps 13 through 16** does not need T gates.

#### C. Cost Comparison of Proposed In-Place QCLAs

1) **Cost Comparison in Terms of T-count**: Table [IV] indicates that all proposed in-place QCLAs have T-count costs of...
In-FT-QCLA2 requires w

Designs by Draper et al. and Trisetyarso et al. Further, In-FT - design by Thapliyal et al. and has the same qubit cost as the design by Takahashi et al. in [8], achieves its T gate savings with only an order that the proposed in-place QCLAs have qubit costs of order O

The Existing works also have a T-count of order O(n) with the exception of Cheng et al. where the T-count is of order O(n^3). Of the proposed designs, In-FT-QCLA1 has the lowest T-count.

In-FT-QCLA2 requires roughly 79.59% fewer T gates than the design by Takahashi et al. in [8], 18.37% fewer T gates than the design by Takahashi et al. in [30], 52.38% fewer T gates than the designs by Mogensen and 42.86% fewer T gates than the designs by Draper et al. and Trisetyarso et al. and 21.18% fewer T gates than the Thapliyal et al.

The Proposed In-place In-FT-QCLA1 requires roughly 89.80% fewer T gates than the design by Takahashi et al. in [8], 59.18% fewer T gates than the design by Takahashi et al. in [30], 76.19% fewer T gates than the design by Mogensen and 71.43% fewer T gates than the designs by Draper et al. and Trisetyarso et al. and 60.59% fewer T gates compared to the design by Thapliyal et al. The In-FT-QCLA1 and In-FT-QCLA2 also achieve an order of magnitude reduction in T gates compared to the design by Cheng et al.

2) Cost Comparison in Terms of Qubits: Table IV indicates that the proposed in-place QCLAs have qubit costs of order O(n). The existing works also have a T-count of order O(n). The existing works also have a T-count of order O(n).

TABLE IV: Cost Comparison of In-Place QCLAs

| Design       | T-count Equation | Qubit Equation |
|--------------|------------------|----------------|
| Draper et al. [28] | 70n – 21w(n) – 21\log(n) – 21w(n-1) – 21\log(n-1) – 49 | 4n – w(n) – \log(n) + 1 |
| Trisetyarso et al. [30] | 70n – 21w(n) – 21\log(n) – 21w(n-1) – 21\log(n-1) – 49 | 4n – w(n) – \log(n) + 1 |
| Thapliyal et al. [31] | \frac{2w(n)}{n} – 28 | 4n + 1 |
| Takahashi et al. [8] | \approx 190n | \approx 5n |
| Takahashi et al. [30] | \approx 49n | \approx 5n |
| Cheng et al. [32] | \frac{14}{5}n^3 + \frac{2}{5}n^2 - \frac{49}{6}n | 3 \cdot n + 1 |
| Mogensen (Design 1) [18] | \approx 84 \cdot n - 56 | 3 \cdot n - 1 |
| Mogensen (Design 2) [18] | \approx 84 \cdot n - 56 | 3 \cdot n - 1 |
| In-FT-QCLA1 [37] | 20n – 8u(n) – 8u(n-1) – 4\log(n) – 4\log(n-1) – 8 | 6n – 2u(n) – 2\log(n) |
| In-FT-QCLA2 [37] | 40n – 11u(n) – 11\log(n) – 11u(n-1) – 11\log(n-1) – 32 | 4n – w(n) – \log(n) + 1 |

w(n) = n – \sum_{i=1}^{\infty} \frac{1}{2^{i-1}}

1. Mogensen (Design 1) can accept a carry in bit c0.
2. Mogensen (Design 2) does not accept a carry in bit.
3. In-FT-QCLA1 is optimized emphasizing T-count.
4. In-FT-QCLA2 is optimized emphasizing qubit cost.

VII. EXISTING WORK

Quantum carry lookahead adders (QCLA) have caught the attention of researchers and many have contributed many designs to the literature. Several designs such as [29] target reversible computing and, therefore, produce significant garbage output. Other designs such as [42] present promising designs but they are not generic, prohibiting scaling the designs to alternative input qubit lengths. Designs that can be implemented on quantum hardware include [29] and [28].

In-place and out-of-place QCLAs have been proposed. We discuss the existing work for in-place and out-of-place QCLAs in separate sections.

A. Out-of-Place QCLAs

Existing out-of-place QCLAs that can be implemented on quantum hardware include [29], [31], [28], [30], [32]. Table II summarizes important performance measures for these QCLAs. T-count, qubit cost, gates used and if the design produces garbage output are shown. The designs in [29] and [31] produce garbage output and must be made garbageless before use in quantum algorithms. As a result, the T-count cost is doubled and the qubit cost is increased by at least n + 1. The reported T-count and qubit cost reflect the added cost from removing garbage outputs. The designs in [28], [30] and [32] have no garbage outputs and can be used as is. The design in [31] offers the lowest T-count in exchange for a O(1) increase in qubit cost compared to existing works. The designs in [29] and [30] achieve the lowest qubit cost with only a modest O(1) increase in T-count compared to more T-count efficient works such as [31]. The design in [29] has the highest resource costs of the existing works. These are all interesting works that offer options with reduced qubit or T gate costs. However, with advances such as recent T gate efficient Toffoli gate implementations shown in [23], we have designed quantum QCLAs that have reduced T-count compared to these works. Further, we can design quantum QCLAs that offer T-count savings yet maintain comparable qubit costs.

B. In-Place QCLAs

Existing in-place QCLAs that can be implemented on quantum hardware include [29], [31], [28], [30], [32] and [37]. Table III summarizes important performance measures for these QCLAs. T-count, qubit cost, gates used and if the design produces garbage output are shown. All the designs have no garbage outputs and can be used as is. The in-place QCLA in [27] is based on CNOT, Toffoli gates and Multiple Control Toffoli gates. To decompose a multiple control Toffoli gate into quantum gates, first the multiple control Toffoli...
In this work, we propose quantum circuits for carry look-ahead addition. We present proposed designs for in-place QCLAs and out-of-place QCLAs. We present three designs for in-place QCLAs and three designs for the out-of-place QCLAs. The in-place FT-QCLA1 (In-FT-QCLA1) and out-of-place FT-QCLA1 (Out-FT-QCLA1) are optimized for T-count. The in-place FT-QCLA2 (In-FT-QCLA2) and out-of-place FT-QCLA2 (Out-FT-QCLA2) are optimized for qubit cost while providing low T gate cost. The proposed QCLAs are based on NOT gates, CNOT gates, Toffoli gates, logical AND gates, uncomputation gates as well as a proposed uncomputation gate for near term quantum hardware. These designs are compared and shown to have reduced T gate and qubit costs compared to the existing work. We conclude that the proposed in-place QCLAs and out-of-place QCLAs can be used in larger quantum data-path circuits where gate count and/or qubit cost is of concern. We also conclude that the proposed QCLAs can be used to increase the amount of computation possible on quantum hardware with limited coherence times.

VIII. CONCLUSION

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