Highlights

Hyperbolic Diffusion in Flux Reconstruction: Optimisation through Kernel Fusion within Tensor-Product Elements

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- The hyperbolic diffusion technique is applied to the artificial compressibility method in flux reconstruction.
- Techniques are developed to fuse large flux evaluation kernels and matrix multiplication on GPUs.
- Optimisation are explored to fully utilise compute resources, including the development of a generation-time memory manager.
Hyperbolic Diffusion in Flux Reconstruction: Optimisation through Kernel Fusion within Tensor-Product Elements

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ABSTRACT

Novel methods are presented in this initial study for the fusion of GPU kernels in the artificial compressibility method (ACM), using tensor product elements with constant Jacobians and flux reconstruction. This is made possible through the hyperbolisation of the diffusion terms, which eliminates the expensive algorithmic steps needed to form the viscous stresses. Two fusion approaches are presented, which offer differing levels of parallelism. This is found to be necessary for the change in workload as the order of accuracy of the elements is increased. Several further optimisations of these approaches are demonstrated, including a generation time memory manager which maximises resource usage. The fused kernels are able to achieve 3-4 times speedup, which compares favourably with a theoretical maximum speedup of 4. In three dimensional test cases, the generated fused kernels are found to reduce total runtime by \(\sim 25\%\), and, when compared to the standard ACM formulation, simulations demonstrate that a speedup of 2.3 times can be achieved.

1. Introduction

The application of numerical simulation to fluid flows is a versatile tool both for exploring complex flow physics and for assisting in the engineering design process. Computation has developed this role due the cost reductions it offers in comparison to experimentation, its flexibility to explore new configurations, and its ability to closely examine difficult-to-observe physics. Large eddy simulation (LES) is a term applied to scale resolving simulations in which typically \(\sim 80\%\) of the turbulent kinetic energy of the vortical motions is resolved. The effect of the turbulence which is not resolved is captured by an explicit subgrid scale model description [29] or through implicit LES (ILES), where this modelling is effectively handled by inherent numerical dissipation. The use of scale resolving simulations in fluid dynamics has allowed the detailed exploration of complex flow phenomena. However, even with powerful accelerator hardware such as graphics processing units (GPUs), these calculations remain expensive. In typical flow simulations of engineering interest, a large proportion of the degrees of freedom are concentrated within the boundary layers. The primary cause of this is that, approaching a solid wall, turbulent length scales decrease and develop greater anisotropy. Increased spatial resolution is therefore required to support the structures responsible for the mixing of momentum. Compounding this, viscous effects become increasingly important within the boundary layer, and, close to the wall, dominate the inertial effects. For these viscous effects, the temporal stability limit scales with \(h^{−2}\), where \(h\) is characteristic of the mesh spacing. This results in rapidly escalating costs for wall resolved LES. Piomelli [21] argues that the cost of wall resolved LES scales with \(Re^{2.4}\), which, given that engineering flows can range from below \(Re = 10^4\) to \(Re = 10^8\) and above, poses a significant computational challenge.

An approach that has been developed in recent years that modifies this \(h^{−2}\) dependency to \(h^{−1}\) is the method of hyperbolic diffusion, introduced by Nishikawa [16, 17]. To illustrate this method, consider a Cauchy problem in one variable and \(n\) dimensions:

\[
\begin{align*}
\partial_t u + \nabla \cdot f &= \nu \Delta u \quad \text{for} \quad u(t, x) : \mathbb{R}_+ \times \mathbb{R}^n \to \mathbb{R}, \\
\quad u(0, x) &= u_0,
\end{align*}
\]

\(\text{(1a)}\)

\(\text{(1b)}\)
where $\mathbf{f}$ is a flux tensor, and $\Delta$ is some generalised $n$-dimensional Laplacian acting on $u$. First, consider the addition of a pseudo-time derivative, to give:

$$
\partial_t u + \partial_x u + \nabla \cdot \mathbf{f} = \nu \Delta u. \quad (2)
$$

This extension of the conservation laws is useful when using implicit time integration methods as it can be used as a relaxation mechanism, with a physical time update considered as a steady-state problem with respect to pseudo-time [7]. The hyperbolic diffusion methodology also uses pseudo-time to reframe the second order terms as a set of coupled partial differential equations (PDEs):

$$
\begin{align*}
\partial_t u + \partial_x u + \nabla \cdot \mathbf{f} - \nu \operatorname{diag}(p_1, p_2, \ldots, p_n) &= 0, \\
\partial_t p_1 + \frac{1}{T_r} \partial_x u &= \frac{p_1}{T_r}, \\
\vdots \\
\partial_t p_n + \frac{1}{T_r} \partial_x u &= \frac{p_n}{T_r}.
\end{align*} \quad (3a)$$

To understand what has happened here, consider the limit as $\tau \to \infty$, where if the pseudo-time derivatives converge on zero, then $p_i \to \partial_x u$. Furthermore, a preconditioning parameter, $T_r$ has been introduced to reduce the stiffness from the auxiliary equations.

Hyperbolic diffusion has been applied to many equation sets that include second derivatives, including the Navier–Stokes equations. Although originally applied to finite volume (FV) methods, several applications have now been made to Discontinuous Galerkin (DG) methods, for example Lou et al. [12] and Li et al. [9]. To the authors’ knowledge, two previous sets of papers have also explored the application of hyperbolic diffusion to the flux reconstruction (FR) method of Huynh [6]: the works of Lou et al. [13], and those of Watson et al. [32] and McCaughtry et al. [14]. The advantage that hyperbolic diffusion offers is that by hyperbolising the equation set, the temporal stability limit is found to scale with $h^{-1}$, see Nishikawa [17], Watson et al. [32]. Given the substantial grid requirements in viscous dominated regions required for wall resolved LES, this offers a route to save considerable computational effort.

The time required for fluid dynamics simulations can also be influenced by the effects of compressibility. Solving low Mach number flows is challenging when using the compressible formulation of the Navier–Stokes equation as the governing equation. This is due to the increased stiffness of the problem as the Mach number is reduced, caused by the acoustic wavespeeds increasing relative to the convective wavespeeds. An alternative is to use one of the many methods similar to SIMPLE [20]. However, this requires the solution of a Poisson equation which requires a separate method that has its own computational challenges [5]. An alternative is to make use of the artificial compressibility method (ACM) of Chorin [4] coupled with the dual time stepping of Jameson [7]. This removes the need to solve a Poisson equation by instead allowing pressure fluctuations in pseudo-time to account for and correct non-zero divergence in the velocity field. The ACM set of equations can be straightforwardly ported to a solver for conservation equations. For example, it has been used together with FR by Loppi et al. [10]. As this method already uses pseudo-time relaxation to converge the velocity field to a divergence free condition, it is a good candidate for hyperbolic diffusion — as all that is required is an adjustment to the governing equations.

For approximating the solution to conservation laws such as those governing fluid flows, high-order discontinuous spectral element methods (DSEM) methods exhibit several attractive features. They can make more efficient use of the information in the stencil when compared to lower order approaches such as cell centred finite volumes or even to high-order finite differences [26]. The trade-off made when choosing a high-order method over a method such as second-order vertex centred finite volume is that the number of operations per update is greatly increased. However, in recent years — for both CPU and GPU hardware — there has been an abundance of FLOPs and a relative scarcity of memory bandwidth [33]. This limitation is such that the capability of a high-performance PDE solver will typically be bounded by the memory bandwidth. This can be seen in practice when using tools such as PyFR [33], deal.II [2], or MFEM [1]. For high-order approaches, this means that the high operation count has little impact on runtime and, owing to the latency of memory transactions, can make better use of the available hardware by performing computation while waiting on memory access. A feature of the DSEM and DG methods that makes them particularly attractive is the locally structured computation within elements. This allows many operations to be performed using optimised matrix-matrix multiplication libraries or via optimised pointwise kernels that aim to hide some memory latency.
Graphic processing units have been popular for some years in high performance computing as they offer a high density of FLOPs and a higher memory bandwidth than CPUs. The high flop density originates in huge parallelism, with several thousand cores being commonly found in a single GPU [18]. As has already been stated, for a number problems in computational physics, calculations are limited by available memory bandwidth. By making better use of the memory hierarchy within GPUs, computations can be effectively optimised. Consider the operation:

\[ X = MU. \]

Many stages in DSEM simplify to this, and it is typical that the operator matrix, \( M \), is constant and, in some cases, sparse. Using the sparsity and immutability of the operators, the GiMMiK library [34] produces unique matrix-matrix multiplication kernels by in-lining the operator matrix constants and fully unrolling the operation. In doing so, optimisations, such as removing multiplication by zero, can be performed at generation time. By in-lining the constants, they are streamed through the instruction cache, leaving more bandwidth for the variable matrix. This can lead to highly performant kernels; however, at high-orders or when using double-precision floating-point numbers, performance can suffer through high register pressure. A second approach was explored by Świradowsicz et al. [23]. For matrix operations in DSEM methods, tensor-product elements, such as maximal-order basis cubes, offer an opportunity for optimisation. By leveraging the tensor product construction, they were able to increase the parallelism and data locality within the memory hierarchy. This was achieved by increasing the number of threads working on a single element and using a user-allocatable L1 cache called shared memory. More recently, Trojak and Witherden [27] presented an in-line compression method for three-dimensional vectors, where a speedup of 50% could be achieved for memory bound calculations with low compression error. By applying the approaches developed in these works, we hypothesise that we may be able to perform novel optimisation of kernels used within FR when applied to ACM with hyperbolised diffusion (ACM-HD) — namely, the fusion of two or more kernels which can reduce memory transactions.

In this paper, we will explore the application of ACM-HD to FR and the opportunities for optimisation that arise. To this end, the paper is structured as follows. FR and ACM-HD are introduced in Section 2, followed by an in-depth analysis of the possibilities for kernel fusion optimisations in Section 3. In Section 4, we describe two approaches to kernel fusion and detail their computational performance. In this work we will only focus on elements with constant spatial Jacobians, and further work will be required to develop methods for non-affine elements. These kernels are then applied within the context of PyFR to a three-dimensional test case in Section 5, and the results analysed. Finally, in Section 6, conclusions are drawn.

2. Preliminaries

2.1. Flux Reconstruction

Flux reconstruction (FR) [6] is a high-order DSEM method that has been widely applied to advection-diffusion problems in computational physics. To illustrate the method, take the following first-order PDE in one dimension:

\[
\frac{\partial u}{\partial t} + \frac{\partial f(u)}{\partial x} = 0, \quad \text{for} \quad u(x,t) : \Omega \times \mathbb{R}_+ \mapsto \mathbb{R}, \quad f(u) : \mathbb{R} \to \mathbb{R}, \quad \text{and} \quad u(x,t=0) = u_0 \forall x \in \partial \Omega, \tag{4}
\]

where \( \Omega \) is the spatial domain. This domain is partitioned into \( N \) compatible sub-domains, \( K_i \), such that \( \Omega = \bigcup_{i=0}^{N} K_i \). A reference domain, \( \tilde{K} \), is specified, which in 1D is taken to be \( \tilde{K} = [-1, 1] \). A mapping \( T_i : \tilde{K} \mapsto K_i \) can then be defined between the sub-domains and the reference domain. The one-dimensional divergence of the flux at a point \( x_j \in K_i \) may then be reconstructed as:

\[
\frac{\partial f(x_j)}{\partial x} = \left( \frac{dT_i}{d\zeta} \bigg|_{x=x_j} \right)^{-1} \left( \sum_{k=0}^{p} \hat{f}(\tilde{x}_k) \frac{dl_k(\tilde{x}_j)}{d\zeta} + (f_l^I - f_l^\delta) \frac{dh_l(\tilde{x}_j)}{d\zeta} + (f_r^I - f_r^\delta) \frac{dh_r(\tilde{x}_j)}{d\zeta} \right). \tag{5}
\]

Here, \( l_k \) is the \( k \)-th Lagrange polynomial of order \( p \), and \( h_l \) and \( h_r \) are the left and right correction functions, respectively. The correction functions have two conditions, \( h_l(-1) = h_r(1) = 1 \) and \( h_l(1) = h_r(-1) = 0 \) [30]. In addition, \( f_l^I \) and \( f_r^I \) are the common interface fluxes at the left and right interfaces, respectively. These are calculated using the solutions interpolated to the interface between adjacent elements. An approximate or exact Riemann solver can then be applied, the aim being to provide physical inter-element communication which also leads to sufficient dissipation to stabilise the method. \( f_l^\delta \) is the flux interpolated to the interface.
Once the approximate divergence of the flux has been calculated, it can either be used to perform an explicit update with an appropriate ODE integration method, or as part of an implicit solver. Flux reconstruction has been successfully used in conjunction both with the dual-time stepping implicit method [7, 10] and pseudo-transient continuation with GMRES [31].

For second-order PDEs, it is necessary to take an extra step and form a continuous approximation of the solution gradient. Take the second-order PDE:

\[
\frac{\partial u}{\partial t} + \frac{\partial f(u, \nabla u)}{\partial x} = 0, \quad \text{for} \quad u(x,t) : \Omega \times \mathbb{R}_+ \rightarrow \mathbb{R}, \quad f(u, \nabla u) : \mathbb{R} \times \mathbb{R} \rightarrow \mathbb{R}, \quad \text{and} \quad u(x,t = 0) = u_0 \forall x \in \partial \Omega, \quad (6)
\]

for which the system, with an additional auxiliary equation, is solved as:

\[
q_j = \frac{\partial u(x_j)}{\partial x} = \left( \frac{d T}{d \xi} \right)_{x=x_j}^{-1} \left( \sum_{k=0}^{p} \left( \frac{d l_k(\xi)}{d \xi} + (u_l^f - u_l^\xi) \frac{d h_l(\xi)}{d \xi} + (u_l^f - u_l^\xi) \frac{d h_l(\xi)}{d \xi} \right) \right).
\]  

\[
\frac{\partial f(x_j)}{\partial x} = \left( \frac{d T}{d \xi} \right)_{x=x_j}^{-1} \left( \sum_{k=0}^{p} \left( \frac{d l_k(\xi)}{d \xi} + (f_l^f - f_l^\xi) \frac{d h_l(\xi)}{d \xi} + (f_l^f - f_l^\xi) \frac{d h_l(\xi)}{d \xi} \right) \right).
\]  

A disadvantage of this approach to second-order PDEs is that forming this point-wise \( H_{\text{div}} \) approximation to the gradient adds a significant number of algorithmic steps compared to the first-order system.

### 2.2. The Artificial Compressibility Method

At low Mach numbers, the compressible Euler and Navier–Stokes equations become extremely stiff, with the acoustic waves travelling through the domain far more quickly than the entropy and vorticity waves. This makes them computationally expensive to solve directly. As an alternative, equations which represent the flow of fluids in the incompressible limit can be derived — the incompressible Euler and Navier–Stokes equations. The artificial compressibility method (ACM) of Chorin [4] is a technique used to solve these incompressible equations with software originally developed for the compressible ones. It does this by modifying the mass conservation equation to supply the pressure field corresponding to a divergence free velocity field. This is done by adding a relaxation parameter, which is here called \( \zeta \). This destroys the intrinsic time accuracy of the equations, but it may be recovered by coupling the approach to the dual-time method of Jameson [7], allowing the pressure field to be converged in pseudo-time. The ACM as applied to the incompressible Navier–Stokes equation can be written, in two dimensions, as:

\[
\frac{\partial}{\partial t} \begin{bmatrix} 0 \\ u/v \end{bmatrix} + \frac{\partial}{\partial \tau} \begin{bmatrix} P \\ u \end{bmatrix} + \frac{\partial}{\partial x} \begin{bmatrix} \zeta u \\ u^2 + P \end{bmatrix} + \frac{\partial}{\partial y} \begin{bmatrix} \zeta v \\ uw - vq \end{bmatrix} = \nu \begin{bmatrix} 0 \\ \partial_{xx} u \end{bmatrix},
\]  

where \( \tau \) is the pseudo-time variable, and \( \nu \) is the kinematic viscosity. Following the method of [17], the diffusion terms may then be hyperbolised by writing the system of equations as:

\[
\begin{bmatrix}
0 \\
0 \\
0 \\
0
\end{bmatrix}
+ \frac{\partial}{\partial \tau} \begin{bmatrix} q_x \\
r_x \\
0 \\
0
\end{bmatrix}
+ \frac{\partial}{\partial x} \begin{bmatrix} u^2 + P - q_x \\
u^2 + P - vr_x \\
-u/T \\
v/T
\end{bmatrix}
+ \frac{\partial}{\partial y} \begin{bmatrix} \zeta v \\
uw - vq_y \\
u^2 + P - vr_y \end{bmatrix} = -\frac{1}{T} \begin{bmatrix} 0 \\
0 \\
0 \\
q_x \\
r_y \\
0 \\
r_x \\
0
\end{bmatrix},
\]  

where \( q_x \approx \partial_x u, \ r_x \approx \partial_x v, \) etc. Going further, this may also be defined in three dimensions as:

\[
\begin{bmatrix}
0 \\
0 \\
0
\end{bmatrix}
+ \frac{\partial}{\partial \tau} \begin{bmatrix} q \\
r \\
s
\end{bmatrix}
+ \nabla \cdot \begin{bmatrix} V^T \\
V \otimes V + PI - vS^T \\
-\frac{1}{T} V \otimes I
\end{bmatrix} = -\frac{1}{T} \begin{bmatrix} 0 \\
0 \\
q \\
r \\
s
\end{bmatrix},
\]  

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where $\mathbf{V} = [u, v, w]^T$, $s_x \approx \partial_x w$ etc., $\mathbf{s} = [s_x, s_y, s_z]^T$, and $\mathbf{S} = [\mathbf{q}, \mathbf{r}, \mathbf{s}]$. This system of equations, which makes use of the hyperbolic diffusion method, is herein referred to as the ACM-HD method. A test can be performed on Eq. (10) showing that the eigenvalues of the flux Jacobian are all real, and hence new governing equation is indeed hyperbolic.

3. Problem Setup

In this paper, the application of FR to low Mach problems is studied with particular emphasis on the implementation details for GPU accelerators, and although this work specifies the use of the CUDA framework, many of the ideas can be transmitted directly to other vector accelerator type hardware.

Within the last four or more generations of devices, the arithmetic capabilities of GPU devices have greatly outperformed their memory bandwidths [33], and therefore the optimisation of algorithms is, in large part, concerned with reducing the global memory access. Due to the high number of variables solved for in ACM-HD compared with standard ACM, the global memory bandwidth use in a naive implementation is considerably increased. Full benchmarking data will be presented later — it suffices at this stage to say that 3D ACM-HD takes twice as long as ACM for a full flux divergence evaluation.

However, ACM-HD presents several opportunities for optimisation. The first is independent of the numerical scheme: by comparing the flux functions in Eq. (8) to those in Eq. (9), the sparsity of the ACM-HD system can be seen. It can be straightforwardly shown that the sparsity of the ACM-HD flux function is:

$$s = 1 - \frac{1 + 2d}{1 + d + d^2}. \quad (11)$$

Taking advantage of this sparsity would provide a reduction in the bandwidth requirements. For example, with $d = 3$, the flux has a sparsity of $\sim 46\%$. However, to best leverage the opportunity afforded by this sparsity, the second optimisation opportunity is described first.

The ACM-HD approach is purely advective in nature, and so the stages in the FR algorithm concerned with the calculation of diffusion terms may be ignored completely. However, the approach gives rise to possibilities for optimisation beyond merely avoiding performing these stages. Consider the algorithmic stages of FR required for purely advective systems. These are shown in Table 1, for a $d$ dimensional domain of $n_e$ elements, $n_v$ number of variables, $n_s$ solution points, and $n_f$ flux points. Here, we use the notation that $\mathbf{U}$ and $\mathbf{F}$ are the solution and flux respectively, with sub-script $s$ and $f$ notation the variable is at the solution or flux points respectively. There are also two further terms $n$ and $S$, which are the outwards facing interface normals and spatial transformation Jacobian. The terms in square brackets of Table 1 show the memory space of each variable. It is assumed that the source terms are only dependent on the flow variables, as is the case with the ACM-HD source terms. These stages already contain an algorithmic optimisation that is used in PyFR, the partially corrected flux divergence, where three of the operators are grouped into a single matrix multiplication — see Witherden et al. [33] for more details. Regardless, it should be clear that there are several intermediate results that are only required by a single subsequent stage. These data dependencies can be seen more clearly in Fig. 1a. Blocks here represent data that is stored and arrows represent the transformation of data, which has three stages: load; compute; and store.

From considering this graph, there is clearly scope to fuse stages together, thereby reducing both the global memory I/O, and the total memory required to perform the calculation. The proposed reduced graph is shown in Fig. 1b, with the component with the greatest potential being the fusion of stages 2 and 3. Stage 6 can also be fused, but this is almost trivial and so will only be considered later as a final stage. The fusion of stages 1 and 4 will not be performed, as stage 4 occurs at the interfaces, and the fusion of M or P kernels with I kernels is not compatible due to the inter-element communication that is required.

The most complex aspect of the proposed optimisation is the fusion of a pointwise kernel and a matrix multiplication kernel. This is due to the high data reuse and the complexity of the flux functions. Due to this complexity, the simplification of only considering tensor-product elements is made, specifically maximal-order hexahedral elements. It was found in practice that quadrilateral elements were significantly less challenging due to lower memory requirements. Fig. 2 aims to show the benefit of tensor production point sets, when combined with a maximal order basis [25] many operations simplify to acting along the lines of the points. A further simplification shall be made in assuming that for both the base and fused kernels the Jacobian terms, $S_q$, will be taken as constant. This will reduce code complexity in an already complex system, and given that both the base and fused kernels will require this data, it is deemed to be a reasonable simplification. Future work will be required to include these terms.
Algorithmic stages of the FR method. Here, \textit{I} denotes interface operations, \textit{M} denotes matrix multiplication operations, and \textit{P} denotes point-wise operations.

| Type | Stage | Data in | Data out |
|------|-------|---------|----------|
| 1    | \textit{M} | Project solution at $x_f$ | $U_j[n_v,n_f]$ | $U_j[n_v,n_f]$ |
| 2    | \textit{P} | Calculate flux at $x_s$ | $U_i[n_v,n_f], S_s[d^2n_v,n_f]$ | $F_s[n_v,n_f]$ |
| 3    | \textit{M} | Partially corrected flux div. | $F_s[d^2n_v,n_f]$ | $\nabla \cdot F_s[n_v,n_f]$ |
| 4    | \textit{I} | Common interface flux | $F_s[n_v,n_f], \nabla \cdot F_a[n_v,n_f]$ | $F_s[n_v,n_f]$ |
| 5    | \textit{M} | Accumulate correction to flux div. | $F_s[n_v,n_f], \nabla \cdot F_s[n_v,n_f]$ | $\nabla \cdot F_s[n_v,n_f]$ |
| 6    | \textit{P} | Negative and source term | $\nabla \cdot F_s[n_v,n_f], U_i[n_v,n_f], S_s[d^2n_v,n_f]$ | $\nabla \cdot F_s[n_v,n_f]$ |

Figure 1: Data dependency graph for purely advective FR.

(a) Base scheme.

(b) Fused scheme.

Figure 2: Schematic of $p=4$ tensor-product point layout with Gauss–Legendre points.

Based on these assumptions, it is possible to build a simple model for the expected performance gains. If it is a fair assumption that all kernels are memory bandwidth bound, then the resulting speedup can be estimated as:

$$\text{speedup} = \frac{\text{Data I/O}_{\text{old}}}{\text{Data I/O}_{\text{new}}}$$

Considering stages 2 and 3, the baseline method will require a minimum of four reads and four writes to global memory. By fusing these steps, this can be reduced to a requirement of a minimum of one read and one write. Hence, if both kernels are bandwidth bound, and the baseline method has no additional global memory access, then the optimal speedup that can be achieved is 4×. If the source term is also fused into the kernel, again assuming it is fully memory bandwidth bound and using the source term of Eq. (10), then the optimal theoretical speedup of a single kernel replacing...
stages 2, 3, and 6 would be 5.346×.

3.1. GPU Memory Hierarchy

To design an approach for fusing these kernels, it is first useful to understand the memory hierarchy employed by recent NVIDIA GPUs [18, 19]. Fig. 3 shows a simplified view of the hierarchy of memory and caches. Stream multiprocessors (SM) are the way computation is broken down on a Volta generation GPU. Each SM has 4 schedulers, each capable of issuing instructions to 4 *warps* with a warp being a group of 32 threads. The unified cache (UC) sits at the SM level, and is partitioned into several spaces. The three important partitions for this application are: constant memory (*cmem*); L1 cache; and shared memory (*smem*); with texture and surface memory not applicable here. The constant memory partition is read only and has a fixed size — however, the split between L1 and shared memory is configurable. The maximum configurable sizes for the Volta series are shown in Fig. 3. To achieve the maximum shared memory allocation of 96 KiB per SM, dynamic shared memory has to be used, with the allocation specified at runtime. To maximise memory throughput, a mixture of the UC memory types should be used, reducing pressure on any single memory and maximising available bandwidth.

![Figure 3: Simplified NVIDIA TITAN V GPU memory overview and statistics. The bandwidth and memory capacities at the UC level and below are calculated per SM.](image)

4. Methods

Two kernel fusion approaches have been developed, following a similar pattern to that seen in Świrydowicz et al. [23]. These two methods differ in their degree of parallelism, and, consequently, in their shared memory requirements. The development of the two differing methods was motivated by a key challenge that was encountered: namely, for a fixed problem size as order increases, the cardinality of a points stencil grows. This means that the optimal level of parallelism will be dependent on order. At lower orders, the resources required to evaluate the contribution from a single tensor-product line is lower, and, therefore, to give threads sufficient work, lower parallelism and fully unrolling the kernels can be beneficial. However, as the contribution along the tensor product line becomes more significant, the resources required become higher — and hence increased parallelism and not unrolling the operation can be beneficial.

4.1. Planar Method

Due to the re-use of data within a flux function evaluation, it is logical that a collection of $N_{et}$ threads will perform all the calculation associated with a single element. This reduces the global loads and keeps the storage of an element to a single block. Furthermore, it would be ideal if all the data could be read into shared memory, which has significantly higher bandwidth and lower latency. This was the approach taken in the related work of Świrydowicz et al. [23]. For

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1 It should be noted that the constant cache does extend up the cache hierarchy, however, here use is only made of a small quantity, and hence the discussion is restricted to L1.
a tensor product element, this would then require the following number of entries:

\[
\text{Shared memory} = \frac{N_t n_v n_s}{N_{et}} = \frac{N_t (1 + d + d^2)(m^d)}{N_{et}},
\]

where \(N_t\) is the total number of threads per block and \(m = p + 1\). As an example of the memory usage required for storing the entire element in shared memory by this method, take \(N_t = 64\), \(m = 4\), \(N_{et} = m\), and \(d = 3\). This would require approximately 53 KiB FP-32 or 106 KiB FP-64 of shared memory. It is clear that, due to the high number of variables, there is a considerable demand on the shared memory, and, at higher values of \(m\), it will become unfeasible to read the entire element into shared.

\[\text{(a) Arrangement of planes.}\]

\[\text{(b) Memory stencil for first point: purple - register, green - shared, blue - global.}\]

**Figure 4:** Schematic for planar method.

Instead, the first approach proposed here is a planar method, where \(N_{et} = m\). So, for \(d = 3\), each thread computes an x-y plane of the tensor product element. In this method, instead of an entire element, a single plane will be loaded into shared at a time. Fig. 4a shows the cardinal axes and how a tensor product element is broken into planes. Sequentially, y-z planes are loaded into shared memory, and each thread calculates the flux divergence for all points along a y-line. Two or more threads accessing the same bank can cause serialization, reducing bandwidth. To overcome this, the GiMMiK framework allows for entire matrix multiplication kernels to be fully unrolled, these unrolled kernels gave significantly increased performance.

4.1.1. Static Optimisations

There are several optimisations that can be applied to Algorithm 4.1 in an attempt to further reduce run-time. At this stage there are four which we will consider. These are:

1. As Fig. 4 makes clear, there is some overlap in which a register can be used instead of performing a global load. One optimisation is to consider using the register when possible.
2. Access to shared memory at the warp level is banked, where the bank number is calculated for single-precision using the following formula:

\[
\text{bank} = \text{mod} \left(\frac{\text{addr}}{4}, 32\right).
\]

It is therefore possible for all 32 threads in a warp to access shared memory in parallel; however, if the access of two or more threads requires the same bank, the access will be serialised, reducing bandwidth. To overcome this,
Algorithm 4.1 Fusion of flux evaluation and divergence calculation with one thread per x-y plane.

1: procedure FUSEDPLANE(N, U_s, −∇ · F_a)
2:     Set global element number, \( e_g \).
3:     \( k := ((\text{threadIdx.x}) \mod \text{warp\_size}) \mod (p+1) \)
4:     if \( e_g < N \) then
5:         for \( i \in \{0, \ldots, p\} \) do \( \triangleright \) Loop over y − z planes
6:             for \( j \in \{0, \ldots, p\} \) do \( \triangleright \) Loop over points on y-line
7:                 Store \( k \)-th y-z plane of \( U_s \) in smem.
8:                 Accumulate x-line contribution to \( \nabla \cdot F_a(i, j, k) \) from gmem
9:                 Accumulate y-line contribution to \( \nabla \cdot F_a(i, j, k) \) from rmem
10:                Barrier, arrive, and wait
11:                Accumulate z-line contribution to \( \nabla \cdot F_a(i, j, k) \) from smem

A constant offset can be added to each element in a warp, such that bank conflicts can be reduced to theoretically zero. This is only theoretical, as with a fully unrolled kernel some conflicts can occur due to the compiler reordering operations.

3. The Volta series of GPUs have 64 KiB of constant memory (cmem), which uses a separate read only cache, spread throughout the cache hierarchy. In the case of a cache hit, this can reduce the need to stream constants through the instruction cache. Therefore, one strategy is to explicitly load the divergence matrix constants into cmem.

4. When directly loading a global variable into shared, it will be implicitly stored in a register within the kernel by the compiler. This is to facilitate several optimisation steps, namely if a variable in shared memory is only used by a single thread, then it may be possible to optimise away the shared load. A further and more common occurrence is that a variable is only guaranteed to be in shared after a thread sync — hence loading a variable into a register first will enable the compiler to better optimise the shared access. However, in the planar algorithm, we know a priori that y-lines will be stored in registers. Therefore, global variables can first be explicitly stored in registers then in shared, removing the use of implicit registers.

To test the effectiveness of these optimisations, we use a standardised test case at \( p = 3 \) with 1024 × 32 elements and a block size of 128 threads. As previously reported by Trojak and Witherden [27], the performance of test kernels can be significantly different if the problem fits in its entirety into L2 cache. The number of elements used here is thus made sufficiently large so that, for all orders \( p \geq 1 \), the L2 cache size of 4.5 MiB is exceeded. Tests were performed on a NVIDIA Titan V using the Nsight Compute profiling suite, and CUDA V11.2.

![Speedup Graph](image)

**Figure 5:** Effect of sequentially applying optimisation strategies 1-4 to the planar method with 128 threads per block at FP-32.

Fig. 5 shows the cumulative effect of applying these optimisation strategies on performance. It is clear that the largest improvement is made by strategy 3 — moving the matrix multiplication constants into constant memory. In
the GiMMiK package, constant memory is not generally explicitly used, as it often negatively impacts performance. However, the operator matrix used to calculate the divergence on a tensor product element has only \((p + 1)^2\) or fewer unique values. This is reduced to \(\lceil \frac{(p + 1)^2}{2} \rceil\) if the sign is removed. Hence, due to the small number of constants compared to more general sparse matrix multiplication kernels, this optimisation is effective here.

The other optimisation strategies were found to have only limited effects, although they generally led to small improvements. The exception to this was the use of optimisation strategy 1 at low \(p\), where the cache pressure is lower. At these low values of \(p\), loads are reduced in favour of registers, thereby increasing the register pressure, and overall reducing the performance.

For this previous series of tests, a block size of 128 threads was used, as, in our experience with PyFR, this value typically gives optimal performance. For the planar method, however, changing the block size will vary the number of active warps per SM due to the shared memory constraints. Fig. 6 shows the effect on the speedup as the block size is varied, for the planar method with all optimisation applied. Firstly, for single-precision, 128 threads per block is near optimal for all orders. Secondly, the double-precision results with this approach are poor for \(p > 2\). This is due to the high register usage of unrolled methods coupled to the larger 64-bit variable, requiring double the space in the register file. If register usage demands more registers than are available, then a process called spillage occur. In this process, space in the register file is freed by writing some of its contents to local memory in the L1 cache. This uses the same memory pathways as global memory access and so can reduce the bandwidth available for global memory transactions. Once the register limit is reached, spillage can quickly become significant. The consequence, due to the high local and global memory usage, is that the primary warp stall reason was given as waiting on scoreboard dependency (“Stall Long Scoreboard”). This means that threads were primarily stalled waiting for memory for long latency memory access, such as global or local memory.

![Figure 6: Unmanaged kernel runtime vs. block size.](image)

4.1.2. Greedy Memory Manager

The benchmarks displayed in Fig. 6 show that the planar approach taken in three dimensions can achieve close to peak performance in some cases. It does not, however, make full use of the shared memory available. Consequently, the number of global reads per variable is fixed at \(p + 2\) or \(p + 1\), depending on the use of optimisation strategy 1. The resulting latency was hidden somewhat through caching and compute interleaving performed either by the programmer or compiler; however, as detailed in the previous section, the primary stall mechanism was reported as long scoreboard stalls. Therefore, performance may be further improved by increasing shared memory usage, reducing the pressure on the cache.

To allow a variable amount of shared memory to be used, a more monolithic approach has to be taken. This monolithic approach will permit several novel optimisation strategies to be explored later. To enable this, we introduce the idea of a generation time memory manager — the architecture of the manager for this problem is shown in Fig. 7a.
Hyperbolic Diffusion in Flux Reconstruction

This was facilitated by producing a flexible framework of sub-managers to handle the different memory types explicitly addressable by users, namely: register; shared; and global. Due to the algorithmic requirements of our application, all global data passes through the $x$ and $y$ registers, which from Section 4.1 are intended to store a $y$-line and $x$-point.

![Diagram of memory hierarchy](image)

**Figure 7:** Memory manager architecture.

At generation time, the computation will request the location of data within the memory hierarchy from the manager, which will pass back the variable name and index within the hierarchy. A greedy approach is used to achieve this, so the manager will give preference in the order: registers over shared over global. In responding to a request, the manager can assess the state of the shared memory. If a variable is only resident in global memory, the manager can cache it into shared memory. To facilitate this, the shared memory is dynamically partitioned by the manager into four partitions: free, low, medium, and high priority, with each partition treated like a stack, as shown in Fig. 7b. The priority of a given variable is set by the computation when making a request. An example of the behaviour when no free space is available is shown in Fig. 7c; for higher priority variables, space is freed from lower priority variables. If no lower priority space is available, the data is not cached in shared. Lastly, data can have their priority escalated or de-escalated — in the planar algorithm this is important to ensure that all variables in the working plane remain in shared, and it also prevents re-loading of variables that have already been cached.

This shared partitioning has the benefit of being able to scale easily to any amount of shared memory, which, for this planar algorithm, is assumed to be greater than the minimum required to store a single plane in shared. The memory manager does account for the number of threads accessing memory — to avoid branch divergence in this algorithm, this means that the data required at a given point is stored in shared memory sequentially for each thread, permitting coalesced access. This does impose the constraint that a variable can only be cached in shared if there is sufficient space for all threads to cache it. In practice, however, this turns out to be of little consequence. The first-in last-out nature of a stack does mean that memory is not ordered in a structured way. However, by requiring that an element is handled by a single block, and furthermore that an element is handled by a single warp, it is possible to coalesce shared access with a low number of bank conflicts.

As the memory manager works at generation time, there is no recurring overhead, and the overhead at generation time is low, typically on the order of a second.

### 4.1.3. Generation Time Optimisations

At generation time, there are several optimisation approaches that may be applied line-by-line, or as post-generation actions by analysing the generated source, facilitated by the monolithic approach. We now set out some of these optimisation strategies before comparing their performance. Due to the clear increase in performance seen earlier by storing the matrix constant in $\text{cmem}$, this optimisation is assumed throughout. The other optimisations are as follows:

**Deconfliction** The first optimisation is the shared deconfliction that was used in the unmanaged kernel — it is expected
to have a larger impact here due to the increased use of shared memory.

**GSR/GRS** The second is the ordering of the explicit shared loads and opportunistic shared load operations. Although not a requirement, it is common in the planar algorithm that when global memory is loaded for storage in shared memory it is then also required in a register. Therefore, the operation can either be ordered as global to shared to registers (GSR), or global to register to shared (GRS). The reason to differentiate this is that, when loading a global variable and storing it to shared, for Volta and earlier devices, the compiler will first implicitly load the global to a register, then store the register to shared. However, by explicitly loading a variable into register and then storing to that shared, it is theorised that this is likely to alter the behaviour of the compiler.

**Load/Store** A third category of optimisations affects when loading or storing from global memory, CUDA has respectively the functions __ldX(...) and __stX(...), where X is a modifier that can influence the compiler’s choice of caching strategy. For the load instructions the choices are: ca, cs, cg, 1u, and cv. More information is available from the PTX programming guide but, briefly, these are respectively: cache in all levels, bypass L1, evict first, last use, and do not cache/fetch again. For the store instructions there are: wb, cg, cs, and wt, which are respectively write back in all levels, bypass L1, used once, and write through. As the output from the kernel is only written to once, both the cs and wt were deemed to be most applicable — with the latter found to give the best performance. For the load operations, the source can be analysed and when a variable is loaded multiple times the base g modifier may be used. However, if a variable is loaded once, or if a particular load is the last use, then the 1u modifier is used. A more complex method could be devised where the memory manager attempts to track the L1 usage in the unified cache, and the modifier could then be then set based on the predicted usage — however, this method was found to perform poorly in practice. As these modifiers only act as hints to the compiler, it is probable that the manager’s model of L1 is inaccurate, and hence changing the caching strategy reduces performance. As reported by Jia et al. [8], the actual L1 cache size can vary from the theoretical expectation depending on shared memory usage, with up to 7 KiB unaccounted for. Given the variable usage of smem, this is also a contributing factor to the inaccuracy of the approximate L1 cache model.

**Compute Interleaving** It was demonstrated by Świrydowicz et al. [23] that by interleaving computation with memory transactions, memory latency could be reduced or hidden by keeping threads busy with computation. A simple strategy was to give the compiler a good chance of interleaving computation in the generated assembly by applying an ASAP strategy. This was performed as a post generation optimisation by first categorising source lines as either memory transactions or computation. A dependency graph is then produced, and compute lines moved to be performed ASAP. There are several nuances to this. Firstly, two lines that both accumulate to the same register were deemed to independent. Secondly, thread synchronisation barriers clearly formed a hard dependency. Without a substantial ratio of computation to memory transaction, interleaving can only have a moderate impact. This can be seen from the memory latencies. For example, from Jia et al. [8], the shared latency without conflicts is approximately 19 SM warp cycles and the average L2 hit latency is 193 SM warp cycles, with a float fused multiple-add (FFMA) being 4 SM warp cycles. A differentiation is made here between clock cycles and SM warp cycles, with each SM capable of handling 4 schedulers at a time, and a SM warp cycle is defined as one cycle issuing instructions to each of the active warps in the SM.

**Compute Agglomeration** A second interleaving algorithm was produced which we will term agglomeration. This method was designed with a view to future hardware features, where shared loads can bypass register and cache levels. Rather than an ASAP interleaving strategy, we look to group the source lines into blocks of memory and computation that can then be interleaved. To do this we again categorise lines as compute or memory transactions and form a preliminary dependency graph. This graph is used to move shared loads as early as possible. Then the source is divided into blocks of compute and memory transaction. It is common to have blocks of a range of sizes, with several blocks of just a single line occurring later in the algorithm due to more data cached in shared. These smaller blocks can be agglomerated into larger ones by moving closer studying the local dependencies, moving shared loads later, with this method a minimum block size of 13 lines was used for this application. Once blocked, the larger blocks can then be broken up to a user specified length. Memory blocks can then be interleaved with compute blocks by further analysing the inter-block dependencies.

The combination of optimisation options tested is shown in Table 2, together with their speedup compared to the un-fused case. In all cases, the minimum amount of shared memory was used. Reviewing the results, the basic
Table 2
Effect of optimisation approaches at $p = 3$, single precision, with the minimum required shared memory, and 128 threads per block.

| Case | Shared | Deconflict | Interleave | Agglomerate | Load | Store | Speedup |
|------|--------|------------|------------|-------------|------|-------|---------|
| 0    | GSR    |            |            |             |      |       | 3.058   |
| 1    | GRS    |            |            |             |      |       | 3.049   |
| 2    | GSR    | ✔          |            |             |      |       | 3.110   |
| 3    | GRS    | ✔          |            |             |      |       | 3.140   |
| 4    | GSR    | ✔          | ✔          |             |      |       | 3.070   |
| 5    | GRS    | ✔          | ✔          |             |      |       | 3.045   |
| 6    | GSR    | ✔          | ✔          | ✔           |      |       | 3.104   |
| 7    | GRS    | ✔          | ✔          | ✔           |      |       | 3.091   |
| 8    | GSR    | ✔          | ✔          | ✔           |      |       | 3.052   |
| 9    | GRS    | ✔          | ✔          | ✔           |      |       | 3.050   |
| 10   | GSR    | ✔          |            | ✔          | ✔    |       | 3.049   |
| 11   | GRS    | ✔          | ✔          | ✔           |      |       | 3.104   |
| 12   | GSR    | ✔          | ✔          | ✔           |      |       | 3.177   |
| 13   | GRS    | ✔          | ✔          | ✔           |      |       | 3.250   |
| 14   | GSR    | ✔          |            | ✔           |      |       | 3.164   |
| 15   | GSR    | ✔          | ✔          | ✔           |      |       | 3.108   |
| 16   | GSR    | ✔          | ✔          | ✔           |      |       | 3.153   |
| 17   | GSR    | ✔          | ✔          | ✔           |      |       | 3.089   |

The interleaving strategy did not give a speedup; however, comparing case 2 with case 14, agglomeration interleaving could increase performance. Yet, when agglomeration is coupled to load or store optimisations, a degradation was observed, although it is not clear why. In a comparison between the GRS and GSR store strategies, GSR more often outperforms GRS; however, in the best performing case, GRS outperforms GSR by the largest margin. It should be noted that the best performing managed kernel, case 13, was outperformed by the similar unmanaged kernel, a speedup of 3.452× compared to the 3.250× obtained here. The distinction seems to stem from a single difference: the unmanaged kernel performs the shared store of plane in a block. So, all the global to register loads are in one block, followed by a block performing the register to shared stores, whereas the managed method interleaves the global to register to shared process, and as seen from case 14, this is the origin of the speedup offered by the agglomeration approach.

Regardless, the benefit of the managed approach is the ability to use more of the shared memory — and, using the optimisations of case 13, a sweep over the available shared memory was performed. The results of this are shown in Fig. 8, with the best performing kernels compared to the unmanaged approach in Fig. 9. This highlights that the planar approach can produce near optimal kernels at low orders. However, performance suffers at higher orders. Furthermore, the memory manager can increase performance at high orders, with the most stark improvement in performance occurring with the FP-64 kernels. As order increases, so too does the workload per thread and register usage. For FP-32, the register limit is reached at $p = 4$, and at $p = 3$ for FP-64. This is the cause of the steep degradation in the performance with order. Therefore, an alternative method should be sought to improve the performance at higher orders.

In general the memory manager approach was able to give small performance when the register limit is not reached, and larger improvement once spillage occurs. The memory manager also introduces several parameters, in practical applications software developers have three potential options. The first is to run a sweep over the parameter space and find the best performing kernel in each case a priori, the second is to repeat this at run time, however this will add significant overhead. The third option is to set the block size to 128 threads and the shared memory based on the underlying hardware, in this case $3 \times 2^{14}$ bits. This configuration was generally performant and will translate well to other architectures, such as AMD GPUs. Finally, the benefit of memory manager are small given the time required to develop the memory manager. However, this approach is useful in a many runtime code generation application where shared memory can be leveraged, and we foresee that the agglomeration approaches will be increasingly useful as asynchronous shared memory acceleration gains adoption.
4.2. Lines Method

Although the planar method was able to produce performant fused kernels, it is clear that, due to the deficiencies already discussed, at higher values of \( p \), there is a significant drop off. To remedy this, an alternative approach may be used where a thread is allocated a line in \( z \) to calculate, increasing the number of threads per element from \( p + 1 \) to \( (p + 1)^2 \). Alternative approaches in which a thread works on a single flux variable were attempted, however the significant branch divergence, coupled to a constant number of threads per element, limited performance.

In the procedure for this lines based method, the \( x \)-\( y \) planes are first sequentially stored into shared memory, with each thread loading a single point from the plane. An optimisation that will be described in more detail later is the changing of the number of variables stored in shared. Once the variables have been stored, to ensure there visibility to other threads a synchronisation is required, after which each thread can then calculate and accumulate the \( x \) and \( y \) contributions to the flux divergence. For a single thread, this is shown diagrammatically for the first and second plane in Figs. 10a and 10b. After all planes have been stored in shared, the \( z \) line contribution can be calculated and stored in global, shown diagrammatically in Fig. 10c. The stages of the calculation are fully outlined in Algorithm 4.2.

The generation procedure for this method was straightforward as an unrolled strategy was not used in this case. This was done as it was found to give significantly reduced performance, and did not solve the stated problem of high
register usage compared to the planar method, which did benefit from full unrolling.

Algorithm 4.2 Fusion of flux evaluation and divergence calculation with one thread per z-line.

1: **procedure** FUSEDLINES($N, U_s, -\nabla \cdot F^a$)
2: Set global element number, $e_g$.
3: $i := \text{mod}(\text{threadIdx}.x/n, p + 1)$
4: $j := \text{mod}(\text{threadIdx}.x/(n(p + 1)), p + 1)$
5: **if** $e_g < N$ **then**
6: **for** $k \in \{0, \ldots, p\}$ **do**
7: Store k-th x-y plane of $U_s$ in smem.
8: Barrier, arrive and wait
9: Accumulate x line contribution to $\nabla \cdot F^a(i, j, k)$
10: Accumulate y line contribution to $\nabla \cdot F^a(i, j, k)$
11: Barrier, arrive and wait
12: **for** $k \in \{0, \ldots, p\}$ **do**
13: Accumulate z line contribution to $\nabla \cdot F^a(i, j, k)$.
14: Store $\nabla \cdot F^a(i, j, k)$ in global.

**Figure 10:** Progression of the method of lines for one thread. Red indicates data that is present in shared memory, green indicated the point being worked on by the current thread, and blue shows the data requirements for the current point.

As was discussed for the unmanaged planar kernel, the storage pattern used for the shared memory can have a significant impact on performance through bank conflicts, and the differences between the planar and lines based algorithm required a different deconfliction approach. A naive AoSoA shared layout will lead to a situation that almost guarantees banks conflicts. To design a memory layout, two things have to be considered: first, how is the global data arranged, and secondly, how will shared memory be used. In response to the former, the global data, inherited from PyFR, uses an AoSoA structure where the same variable for multiple elements are stored sequentially. Therefore, to achieve coalesced global loads, sequential threads should work on sequential elements. Therefore, if a block works on $n$ elements with $n(p + 1)^2$ threads, the global element number for a thread is calculated as:

$$e_g = \text{mod}(\text{threadIdx}.x, n) + n(\text{blockIdx}.x).$$

The $i$ and $j$ indices may then be subsequently calculated as shown in Algorithm 4.2. When shared memory is used, it will be loaded one variable at a time by all threads in a warp. Therefore, after elements, $i$ and $j$ are the next major indices, followed by $k$, and with variable numbering last. Combining this we can produce the following indexing:

$$U_s(e_j, i, j, k, v) \rightarrow e_j + n \left( i + j(p + 1) + k(p + 1)^2 + v(p + 1)^3 \right).$$
where \( e_l \) is the block local element number, \( e = \text{mod}(\text{threadIdx.x}, n) \). For single-precision numbers, the effect of this layout is that, when loading or storing either a variable or accumulator to shared, each thread uses a different shared memory bank. There is one exception to this: for some values of \( k \) aliasing can lead to a small number of bank conflicts. However, this number is generally very small and in practice the number of bank conflicts was in the range \( 0 \sim 5\% \).

### 4.2.1. Static Optimisations

The base method shown in Algorithm 4.2 results in all accumulation stages being performed using variables from shared. This change, together with not fully unrolling the kernel, makes several new optimisations possible. Firstly, it is not necessary to store pressure, as it could be combined with several of the gradient terms. Furthermore, in the flux kernel the gradients are always multiplied by the viscosity, therefore rather than repeatedly multiplying by \( v \) the following are actually stored in shared memory:

\[
\begin{bmatrix}
u & -vq_x + P & -vq_y \\
r_x & -vr_y + P & -vr_z \\
s_x & -vs_y & -vs_z + P
\end{bmatrix}
\]

Consequently, together with the accumulator the base method requires 25 variables per point to be allocated in shared memory.

A further optimisation can be made by recognising that the first term in the flux divergence can be straightforwardly reconstructed from 3 of the other flux divergence terms, thereby reducing the total number of variables to 24 per point. The final optimisation is to vary the number of variables stored in shared memory. As there is one point per line per element, decreasing the shared memory usage can increase the block size, which may help to increase occupancy at higher \( p \). A second effect of reducing the number of variables in shared memory is that it will increase the maximum theoretical bandwidth. Consider the \( z \)-line accumulation: once all variables are in shared, the global bandwidth is then under utilised. To determine the validity of this hypothesis, the several options for which variables are stored were tested, see Table 3 for these configurations.

Several unsuccessful optimisation approaches were also attempted, and we would like to briefly mention one of note. Several vector types are defined in CUDA, such as \( \text{float4} \), and, when preforming a global load or store operation, it is possible to increase the sectors per request by ensuring memory alignment and then utilising these types. However, due to the global AoSoA data layout of PyFR \([33]\), this necessitates that the elements per block is divisible by the vector width and, furthermore, that only some threads participate in the load. As a result, a more optimal sectors per request was produced — but at a lower bandwidth, due to the overhead of the synchronisation and data shuffle steps required.

As the block size is set by the number of elements per block, we will investigate the performance with order and precision, from one element up to the maximum number of elements per block based on shared memory size. The results for the base method with 25 values per point is shown in Fig. 11. Here the vertical dashed line indicates 48 KiB. The results for 12 values per point, i.e. all values read from global, are presented in Fig. 12, and additionally the other variable configurations can be found in Appendix A.

Firstly, it is worth noting the change that occurs for \( \text{smem} > 48 \text{ KiB} \), which is half the maximum size of shared memory. Around this value, the performance curve flattens, and in some cases, there is a dip in performance. This is caused by a reduction in the occupancy, as once \( \text{smem} > 48 \text{ KiB} \), only a single block per SM can be operated on at a time. For example, take \( p = 3 \) with 18 values per point and 160 threads per block, so the shared memory usage

| No. variables | No. accumulators | Total | Variables stored                        |
|---------------|------------------|-------|----------------------------------------|
| 12            | 13               | 25    | Velocity and pressure augmented gradients|
| 12            | 12               | 24    | Velocity and pressure augmented gradients|
| 6             | 12               | 18    | Velocity, \((-vq_x + P), (-vr_y + P), \) and \((-vs_z + P)\) |
| 3             | 12               | 15    | Velocity                               |
| 0             | 12               | 12    | None                                   |
is just below half. Therefore, two blocks can be worked on at once, with an achieved warp occupancy of 9.5 warps per SM. Compare that with 176 threads per block, where only a single block can be worked on due to shared memory exceeding half of the max, this achieved 5.85 warps per SM. This also links to a shift in performance between lower $p$ and higher $p$. At lower $p$, higher thread counts are possible with lower shared memory usage, therefore leading to high occupancy, whereas at higher $p$ performance becomes more monotonic with shared memory.

Studying Fig. 13, it can be seen that reducing the usage of shared memory in favour of greater diversity of memory access can increase performance at higher order, most notably for FP-64. The advantage comes from increasing the global memory bandwidth. Fig. 13a shows that even for these highly optimised kernels, at higher order it is difficult to achieve high global memory bandwidth. By reducing the amount of data stored in shared, this defers some global access. The effect is reduced pressure on shared memory, but by adding a second memory location to some parts of the calculation, the effective bandwidth is increased. The latency of shared and global memory are significantly different, 19 SM warp cycles compared to 193 SM warp cycles for L2 on Volta, and given that parts of the flux function involve multiple terms, there is not a clear relationship to inform how much of shared should be deferred to global. But the general trend of Fig. 13b is a flattening of the bandwidth curve with order.

**Figure 11:** Method of lines performance with 25 variables and varying shared memory usage.

**Figure 12:** Method of lines performance with 12 variables and varying shared memory usage.
Although these line-based approaches were developed for the Volta architecture, we do not foresee any limitations in porting them to other GPUs. However, as is evident from the performance curves, the general trend is that more shared memory leads to better performance. Given that this method aims to avoid global memory bottlenecks, this is to be expected, but consequently some architectures that have limited shared memory may not perform as well. However, it does appear that trend in new generations of GPU devices is for the shared memory per block to increase, suggesting that the methods outlined here will perform well on forthcoming devices.

5. Application of Methods

In the previous section, two approaches were outlined, and it was shown that it was possible to fuse together two ACM-HD kernels, which provided a speedup over the un-fused method. These kernels have been implemented in the open-source solver PyFR [33]. Currently, two simplifying restrictions have been made: the mesh must have a constant Jacobian, and it must be composed solely of hexahedral elements. With this in mind, the Taylor–Green vortex (TGV) [3, 24] test case was used to benchmark the methods. The domain for the TGV is a three-dimensional periodic
Table 4
Optimal kernel configuration with polynomial order for FP-32 working precision.

| $p$ | Method                | Configuration          |
|-----|-----------------------|------------------------|
| 1   | Planar, un-managed    | blockDim.x = 128      |
| 2   | Planar, un-managed    | blockDim.x = 128      |
| 3   | Planar, managed       | smem = 66 KiB, blockDim.x = 128 |
| 4   | Lines, 24             | smem = 93.75 KiB, blockDim.x = 200 |

Table 5
Optimal kernel configuration with polynomial order for FP-64 working precision.

| $p$ | Method               | Configuration          |
|-----|----------------------|------------------------|
| 1   | Planar, managed      | smem = 42 KiB, blockDim.x = 128 |
| 2   | Planar, managed      | smem = 59 KiB, blockDim.x = 128 |
| 3   | Lines, 15            | smem = 90 KiB, blockDim.x = 192 |
| 4   | Lines, 12            | smem = 93.75 KiB, blockDim.x = 200 |

box, $\Omega = [0, 2\pi]^3$, with the initial condition defined as:

$$u = \sin(x) \cos(y) \cos(z),$$  

$$v = -\cos(x) \sin(y) \cos(z),$$  

$$w = 0,$$  

$$P = \frac{1}{\gamma M^2} + \frac{1}{16} \cos(2z + 2) [\cos(2x) + \cos(2y)].$$

where $\gamma$ is the ratio of specific heats and $M$ is the Mach number, which we take to be 0.08. To initialise the gradient terms, the exact derivative of the initial condition may be straightforwardly found. The Reynolds number was set at 1600 and the artificial compressibility parameter to $\zeta = 2.5$, with a time period of $T = 5 \times 10^{-3}$. From the prior testing, the optimal kernels for single-precision floating-point were used, the configurations of which are shown in Tables 4 and 5.

Initially, we consider the case of $p = 4$, FP-32, for a grid of $32^3$ elements and a single pseudo-time step run on a single NVIDIA V100 GPU. The results of this are presented in Figs. 17a and 18a for single and double precision floating-point respectively, in which each shows three bars. These bars represent the time taken for a time step by: ACM-HD without any fusion, ACM-HD; ACM-HD with flux divergence fusion, ACM-HD (F); and ACM-HD with flux divergence and source term fusion, ACM-HD (FS). These results show that when applied with PyFR the fused flux divergence kernel (in blue) achieves a 2.46× speedup for both precisions, which is slightly lower than expected given the results from the tests in Section 4, and is attributable to the differences between the Titan V and V100 architectures — namely, the different FLOPS to bandwidth ratio. When the source term is also fused into the flux divergence kernel, the speedup was measured to be 2.83× and 2.32× for single and double precision, respectively. The flux and source fusion is lower than optimal primarily due to the performance prior to the source term fusion being less than the expected optimal. Furthermore, fusing the source term has a larger than expected cost, increasing the kernel runtime by ~14.3% and ~33.8%, and is a result of not storing $q_x$, $r_y$, and $s_z$ directly in shared memory; which is why the cost doubles when moving from single to double precision. Although fusing the source term does give a net reduction in run time, one of the other strategies may be better suited in this case. A final point on the comparison in Figs. 17a and 18a is that several optimisation routes are known to the authors which are able to reduce the runtime of pseudo-time update stage, causing the impact of the fused kernel to be proportionally greater in the future. We intend to improve the performance of this kernel through a combination of fusing what are currently individual AXPY type kernels together, and by increasing their granularity such that multiple threads are assigned to each element (whereas currently one thread loops through all solution points — something which can limit the ability of the kernel to fully saturate global memory bandwidth). Beyond this, there are medium term goals to further fuse this revised kernel into the final update kernel involved in an RHS evaluation, further saving memory bandwidth and reducing overhead.
We now consider running from $t = 0$ to $t = 10$ for both single and double precision. In doing so, we will use several established convergence acceleration methods, namely $P$-multigrid [10] and spatially varying pseudo-time stepping [11]. For the double-precision run the same number of pseudo-iterations were used as single-precision for each physical step. Based on the work of Loppi et al. [11] and Trojak and Witherden [28], we made use of the asymmetric $P$-multigrid cycle shown diagrammatically in Fig. 15.

![Figure 15: $P$-multigrid cycle: [(4, 1), (3, 1), (2, 1), (1, 4), (2, 1), (3, 1), (4, 7)].](image)

The physical time-integration was performed with a BDF2 scheme with $\Delta t = 0.01$. The pseudo iterations were performed using a RK34 embedded pair method with locally adaptive pseudo-stepping with the initial $\Delta t/\Delta \tau = 10$. The single-precision convergence was monitored via the $l_2$ residual in velocity field with a tolerance of $2 \times 10^{-4}$. As the stability of the pseudo-stepping increases when spatial order decreases, the $\Delta t$ may be increased within the $P$-multigrid cycle. For this, a constant factor of 1.75 was found to be appropriate. The exact input files used can be found in the ESM. For the common interface flux, a Rusanov type approximate Riemann solver was used for the hyperbolic portion of the Riemann solve. For the standard ACM formulation, the viscous common interface flux was approximated using LDG with $\beta = 0.5$ and $\tau = 0.1$. For ACM-HD, it was found that taking the mean of left and right flux at the interfaces for the additional equations was sufficient.

To ensure the validity of the numerical results, the global integral property — enstrophy — was calculated. This functional has the following form:

$$
\epsilon(t) = \frac{\nu}{|\Omega|} \int_{\Omega} \nabla(t, x)^T \nabla(t, x) \, dx
$$

(17)

where $|\Omega|$ is the volume of the domain, and $\nabla = \nabla \times \nabla$. Here, the slightly modified definition of enstrophy is used, as, in the incompressible limit, this form should be identical to the kinetic energy dissipation rate. A comparison between the ACM and ACM-HD results is made in Fig. 16, which shows that only a small difference is visible when the kinetic energy dissipation rate is at its peak. From the work of Mengaldo et al. [15], the observed difference is within the range of the effect of the approximate Riemann solver, which changes between the two runs due to one system being purely hyperbolic and the other mixed.

Figs. 17b and 18b displays a comparison of the conventional mixed hyperbolic-parabolic ACM approach with the various ACM-HD approaches. A single conventional ACM step is faster than an ACM-HD (FS) step; for example, by $\sim 9.8\%$ at $p = 4$ FP-32. However, ACM-HD has an increased rate of convergence, and, as the system is purely hyperbolic, the stability limit scales with $h^{-1}$ rather than $h^{-2}$ [32]. In combination, kernel fusion and hyperbolic diffusion in this case is found to give a significant speedup of $\sim 2.3\times$ and $\sim 2.2\times$, for FP-32 and FP-64 respectively.
Figure 16: TGV enstrophy comparison at FP-32 with reference DNS data from van Rees et al. [22] with ACM and ACM-HD, \( p = 4 \) and \( 160^3 \) grid points. The reference DNS was calculated with a pseudo-spectral method for \( 512^3 \) grid points.

(a) Single step runtime comparison of ACM-HD fusions, \( p = 4 \).

(b) Runtime comparison with \( P \)-multigrid, \( p = 4 \) for \( t_{\text{end}} = 10 \).

Figure 17: TGV runtime comparison, FP-32, on a NVIDIA V100.
Figure 18: TGV runtime comparison, FP-64, on a NVIDIA V100.
6. Conclusions

In this work, the hyperbolic diffusion technique has been applied to the artificial compressibility method used to solve the incompressible Navier–Stokes equations. The resulting system of equations was solved with the high-order flux reconstruction method, where, due to the removal of the algorithmic steps needed to construct the viscous terms, optimisation could be performed. In particular, it was found that the evaluation of the fluxes could be fused with the calculation of the flux divergence to give a theoretical speedup of $4\times$ over the un-fused operation.

This work has focused on the treatment of tensor product elements with constant Jacobians and NVIDIA GPU architectures. To this end, two approaches were taken to fuse the kernels, which offered differing degrees of parallelism. These were a planar method and a lines method, in which each thread formed the calculation for a plane and line, respectively. For the reduced parallelism of the planar method, it was found that a fully unrolled approach could produce optimal kernels at low orders, but, due to high register usage, high orders were challenging. To maximise the use of GPU resources, a novel generation time memory manager was developed which was able to increase the performance of the planar method in some cases. The lines method was able to successfully increase the performance of fused kernels at higher orders, largely due to increased parallelism. Furthermore, the lines method did not benefit from unrolling, and instead varying the shared memory used per point was successful in increasing performance by diversifying memory usage.

Finally, the optimal kernels were applied to the Taylor–Green vortex test case via the PyFR solver framework. It was observed that the kernel fusion could reduce the runtime of the hyperbolised ACM system by $\sim25\%$. A comparison was then made between the standard ACM formulation and the optimised hyperbolic form, and it was found that the latter was $\sim2.3\times$ faster when converged to the same accuracy. This not only facilitates the faster computation of incompressible flows, but also demonstrates the more general utility of these kernel fusion approaches.

Future work will be required to generalise these approaches to non-constant spatial Jacobians, although it is expected that in the case of linear elements this will not pose a significant challenge. This is because only the locations of the element corners need to be loaded — a strategy that is already applied in the PyFR flux kernels. However, for fully non-linear elements more complex fusion strategies will be needed that incorporate the Jacobian into the shared memory layout. Furthermore, AMD has indicated that the quantity of shared memory on their upcoming future architectures will increase, which will broaden the scope of the techniques developed here.

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A. Lines Appendix

Figure 19: Method of lines performance with 24 variables and varying shared memory usage.

Figure 20: Method of lines performance with 18 variables and varying shared memory usage.
Figure 21: Method of lines performance with 15 variables and varying shared memory usage.

B. Example Function Listings

Source code not included on ArXiv.