HPC AI500:
THE METHODOLOGY, TOOLS, ROOFLINE PERFORMANCE MODELS, AND METRICS FOR BENCHMARKING HPC AI SYSTEMS

AUTHORS’ CONTRIBUTION

SECTION 1 IS CONTRIBUTED BY JIANFENG ZHAN AND ZIHAN JIANG. SECTION 2 IS CONTRIBUTED BY JIANFENG ZHAN, ZIHAN JIANG, AND FEI TANG. SECTION 3 IS CONTRIBUTED BY JIANFENG ZHAN. SECTION 4 IS CONTRIBUTED BY XINGWANG XIONG, ZIHAN JIANG, LEI WANG, WANLING GAO, AND JIANFENG ZHAN. SECTION 5 IS CONTRIBUTED BY ZIHAN JIANG, LEI WANG, CHUNJIE LUO, WANLING GAO, JIANFENG ZHAN, AND HONGXIAO LI. SECTION 6 IS CONTRIBUTED BY LEI WANG, ZIHAN JIANG, WANLING GAO, AND JIANFENG ZHAN. SECTION 7 IS CONTRIBUTED BY ZIHAN JIANG, XINGWANG XIONG, LEI WANG, WANLING GAO, CHUNXIN LAN, AND JIANFENG ZHAN. SECTION 8 IS CONTRIBUTED BY ZIHAN JIANG, LEI WANG, WANLING GAO, AND JIANFENG ZHAN. SECTION 9 IS CONTRIBUTED BY JIANFENG ZHAN.

BenchCouncil: International Open Benchmarking Council
Chinese Academy of Sciences
Beijing, China
http://www.benchcouncil.org/HPCAI500/index.html

TECHNICAL REPORT NO. BENCHCOUNCIL-HPCAI500-2020-1
JUNE 30, 2020
HPC AI500: The Methodology, Tools, Roofline Performance Models, and Metrics for Benchmarking HPC AI Systems*

Zihan Jiang\(^1,3\), Lei Wang\(^1,2\), Xingwang Xiong\(^1,3\), Wanling Gao\(^1,2\), Chunjie Luo\(^1,2\), Fei Tang\(^1,3\), Chuanxin Lan\(^1\), Hongxiao Li\(^1,3\), and Jianfeng Zhan\(^*1,2,3\)

\(^1\)State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences, \{jiangzihan, wanglei, xingwangxiong, gaowanling, luochunjie, lanchuanxin, tangfei, lihongxiao, zhanjianfeng\}@ict.ac.cn

\(^2\)BenchCouncil (International Open Benchmarking Council)

\(^3\)University of Chinese Academy of Sciences

June 30, 2020

1 Abstract

The recent years witness a trend of applying large-scale distributed deep learning algorithms in both business and scientific computing areas, whose goal is to speed up the training time to achieve a state-of-the-art quality. The HPC community feels a great interest in building the HPC AI systems that are dedicated to running those workloads. The HPC AI benchmarks accelerate the process. Unfortunately, benchmarking HPC AI systems at scale raises serious challenges. None of previous HPC AI benchmarks achieve the goal of being equivalent, relevant, representative, affordable, and repeatable.

This paper presents a comprehensive methodology, tools, Roofline performance models, and innovative metrics for benchmarking, optimizing, and ranking HPC AI systems, which we call HPC AI500 V2.0. We abstract the HPC AI system into nine independent layers, and present explicit benchmarking rules and procedures to assure equivalence of each layer, repeatability, and replicability. On the basis of AIBench—by far the most comprehensive AI benchmarks suite, we present and build two HPC AI benchmarks from both business and scientific computing: Image Classification, and Extreme Weather Analytics, achieving both representativeness and affordability. To ranking the performance and energy-efficiency of HPC AI systems, we propose Valid FLOPS, and Valid FLOPS per watt, which impose a penalty on failing to achieve the target quality. We propose using convolution and GEMM—the two most intensively-used kernel functions of AIBench to measure the upper bound performance of the HPC AI systems, and present HPC AI roofline models for guiding performance optimizations. The evaluations show our methodology, benchmarks, performance models, and metrics can measure, optimize, and rank the HPC AI systems in a scalable, simple, and affordable way. The specification, source code, datasets, and benchmarking data are publicly available from \texttt{http://www.benchcouncil.org/benchhub/hpc-ai500-benchmark}.

2 Introduction

The huge success of AlexNet\(^1\) in the ImageNet\(^2\) competition marks the booming success of deep learning (DL) in a wide range of commercial application areas. Many commercial fields, like image recognition, and natural language processing achieve unprecedented accuracy, even outperforming common

\(^*\)Jianfeng Zhan is the corresponding author.
human being’s capability. Though it is much challenging to obtain high quality labeled scientific data sets, there is an increasing trend in applying DL in scientific computing areas [3–6].

With massive training data available, the recent years witness a trend of applying distributed DL algorithms at scale in both commercial and scientific computing areas. Motivated by these emerging HPC AI workloads, the HPC community feels a great interest in building HPC AI systems to reduce time-to-quality—the training time to achieve a convergent quality. For example, the Summit system [7] is built to tackle huge AI challenges. The benchmark accelerates the process [8, 9], as it provides not only design inputs, but also evaluation and optimization metric and methodology [10, 11]. However, there are several challenges in benchmarking HPC AI systems.

First, it is nontrivial to prove the equivalence of two AI benchmark implementations on different systems or even the same system with different scales. Equivalence quantifies how equivalent two benchmarks implementations on different systems or the same system with different scales. There are complex interactions among hardware and software systems, which is further aggravated by the AI algorithm complexity. Even for the same AI algorithms, there are huge parameters significantly impacting learning dynamics [9]. ImageNet/ResNet-50 (Image Classification) training is one well-known showcase for optimizing HPC AI systems. Table 1 summarizes the state-of-the-art and state-of-the-practice optimization approaches in ImageNet/ResNet-50 training. Unfortunately, without equivalent benchmarking rules explicitly stated, we can not objectively derive the performance edge of one system against the others from Fig. 1.

The second challenge inherits from the the conflict of two classical benchmarking methodologies with the emphasis of different requirements. On one hand, as no single benchmark or metric can measure the performance of computer systems on all applications [12], being relevant, representative, and diverse is
of paramount importance [10]. On the other hand, TOP500 [13] establishes the de facto super computer benchmark standard in terms of three defining characteristics: scalable, simple, and affordable.

- **Learning rate policies and batchsize setting**
- **Other hyper-parameters settings**
- **Workload (Algorithm)**
- **Programming Model**
- **AI Framework (e.g. TensorFlow)**
- **AI Accelerators and libs (e.g. GPU, CUDA)**
- **Communication libs (e.g. Horovod)**
- **OS**
- **Hardware (e.g. CPU, Network)**

**Figure 2:** The equivalent perspective of HPC AI500 V2.0 Methodology. We abstract the HPC AI system into nine independent layers: put each layer under test while keeping other layers intact. We provide three high levels of benchmarking: hardware, system, and free: put the related layers together under test while keeping other layers intact with only allowed changes stated in the benchmarking rules.

In the AI domain, there are massive AI tasks and models with different performance metrics. For example, by far the most comprehensive and representative AI benchmark suite–AIBench [10, 11, 14, 15] contains seventeen AI tasks. It is not affordable to implement so many massive benchmarks and further perform benchmarking at scale. So what are the criteria for deciding the benchmarks that can fairly and objectively measure the HPC AI systems.

Third, the benchmark mandates being repeatable, while the nature of AI is stochastic, allowing multiple different but equally valid solutions [9]. The uncertainty of HPC AI is manifested by run-to-run variation in terms of epochs-to-quality and the effect of scaling training on time-to-quality [9, 16]. For the first time, Tang et al. [10] quantify the variations of seventeen AI benchmarks of AIBench. They found that the run-to-run variations vary from 0% to 38.46% in terms of the ratio of the standard deviation to the mean of the training epochs to achieve a convergent quality.

None of previous HPC AI benchmarks achieve the goal of being equivalent, relevant, representative, affordable, and repeatable. They either are not representative or even irrelevant to HPC AI workloads in terms of kernel functions [17, 18], or overlook the differences of HPC AI workloads between scientific and business computing [9], or fail to specify fair and equivalent benchmarking rules across different HPC AI systems [9]. Moreover, they fail to propose simple and AI domain-specific metric to score and rank HPC AI systems.

The micro benchmark like HPL-AI [18], which only contains LU decomposition, is affordable to perform a fair comparison of competing systems by isolating hardware and software from statistical optimizations [9]. However, we found it is irrelevant to most AI workloads in Section 3.2. Moreover, the traditional micro or kernel benchmarking methodology, widely used in the HPC communities, can lead to misleading conclusion, as the mixed precision optimizations indeed improve the FLOPS of a micro benchmark like convolution, while significantly impact time-to-quality of an AI task like image classification as discussed in Section 3.2.

This paper presents HPC AI500 V2.0—a comprehensive HPC AI benchmarking methodology, tools, performance models, and metrics. As shown in Fig. 2 we abstract the HPC AI system into nine...
independent layers. To perform fair benchmarking across different systems or the same system with
different scales, we present explicit benchmarking rules to assure equivalence of each layer, repeatability,
and replicability of those two benchmarks. We put each layer under test while keeping the other layers
intact. Also, We propose three high levels of benchmarking: hardware, system, and free (Fig. 2): put the
related layers under test while keeping the other layers intact unless otherwise stated.

On the basis of AIbench, we present two benchmarks: Image Classification with state-of-the-art
quality on the ImageNet dataset (business computing), and Extreme Weather Analytics (EWA) with
state-of-the-art quality on the EWA dataset (scientific computing) to measure HPC AI systems. These
two benchmarks represent two clusters of AI benchmarks—thirteen AI benchmarks from AIbench from
perspectives of computing areas (business vs. scientific computing), diversity of model complexity (from
0.03 million to 68.39 million in terms of model parameters ), computational cost (from 0.09 MFLOPs to
157.80 GFLOPs in terms of a single forward computation), and convergence rate (from 6 epochs to 304
epochs). Moreover, our decision also takes into account their repeatability, and whether these benchmarks
have widely-accepted metrics or not.

To rank HPC AI systems, we propose two metrics, named Valid FLOPS, and Valid FLOPS per watt,
to emphasise the vital importance of achieving the state-of-the-art quality, and an auxiliary metrics—time-
to-quality.

We propose using convolution and GEMM (GEneral Matrix to Matrix Multiplication)—two most
intensively-used kernel functions of AIbench to measure the upper bound performance of the HPC AI
systems, and present corresponding single-node and distributed-system HPC AI roofline models for
guiding performance optimizations.

The evaluations show our benchmarks can fairly measure the HPC AI systems in a scalable, simple,
and affordable way. Our Roofline models are helpful to system optimizations. Our metrics can be used to
rank HPC AI systems in a simple and visual manner.

3 The challenges of HPC AI benchmarking

The challenges of HPC AI benchmarking inherit from the complexity of benchmarking scalable
hardware and software systems, which are further exaggerated by the uncertainty of AI algorithms.

3.1 Equivalence

For the same AI algorithms, there are huge parameters significantly impacting learning dynamics [9].
Even for the same system with different scales, the interactions among system size, minibatch size, and
learning dynamics have a significant impact on time-to-quality and computation overhead in terms of
FLOPS [9][19][26]. So for the same AI task, it is non-trivial to prove the equivalence of two benchmark
implementations on different systems or even the same system with different scales.

ImageNet/ResNet-50 training is one widely-used showcase for optimizing HPC AI systems. Fig. 1
shows the systems performance varies wildly: the performance gap in terms of FLOPS is 50x. Accordingly,
Table 1 summarizes the state-of-the-art and state-of-the-practice work on ImageNet training at scale. In
addition to the system-level optimizations (e.g. more efficient communication typologies), some algorithm-
level optimizations involve changing model architectures (e.g. optimizations on batch normalization) or
learning rate policies, i.e., LARS [26]. As there are prohibitively complex interactions among hardware
systems, software systems, and algorithms, previous work fails to clearly state the equivalent rules of each
hardware or software layer for benchmarking HPC AI systems.

3.2 Representative, Affordable, and Relevant

The second challenge inherits from the conflict of two classical benchmarking methodologies with the
emphasis of different requirements.
Table 1: The summary of the utilized optimization approaches in ImageNet/ResNet-50 training. The optimization approaches of each system are inconsistent or inequivalent. Please note that only the optimizations items in *italics* are allowed to change in the HPC AI500 benchmarking rules (defined in Section 6).

| System-level | Algorithm-level |
|--------------|-----------------|
| parallel Mode | Communication | Precision | Data Staging | Learning Rate Policy | Data Argumentation | Model Architecture | Others |
| **Facebook** | Data parallelism | Recursive halving and doubling and ring all-reduce. | N/A | N/A | Linear scaling and warm up [20]. | N/A | N/A | Momentum correction; Data shuffling based on the workers. |
| **Intel** | Data parallelism | Intel MLSL [22] | N/A | N/A | Linear scaling and warmup; final collapse. | N/A | N/A | Collapsed ensembles; Dynamically change weight decay. |
| **IBM** | Data parallelism | Topology aware | N/A | N/A | Linear scaling, warmup [20] | N/A | N/A | Momentum correction; Data shuffling based on the workers. |
| **Berkeley** | Data parallelism | Intel MLSL [25] | N/A | N/A | Linear scaling and warmup [20]; LARS [26]. | N/A | N/A | N/A |
| **Preferred Networks** | Data parallelism | Ring all-reduce; Communication compression. | N/A | N/A | Linear scaling, RMSprop warmup, and slow-start; | N/A | N/A | Batch normalization: without moving averages. |
| **Sony** | Data parallelism | 2D-Torus all-reduce; Communication compression; Communication tensor fusion. | N/A | N/A | Mixed precision training: BFLOAT16 & FP32; Adding, scaling, rotations etc | N/A | N/A | N/A |
| **Tencent** | Data parallelism | Hierarchical all-reduce; Communication compression; Communication tensor fusion. | N/A | N/A | Efficient input pipeline | Linear scaling and warmup [20]; LARS [26]. | N/A | Batch normalization: eliminating weight decay. |
| **Google** | Data parallelism | 2D-Mesh all-reduce; | Mixed precision training: BFLOAT16 & FP32 | Efficient input pipeline | Linear scaling and warmup [20]; LARS [26]. | Fused JPEG decode and cropping | Distributed batch normalization | N/A |
| **Fujitsu** | Data parallelism | Communication tensor fusion; Optimal scheduling by grouping layers; Calculate the norms of layers in parallel. | Mixed precision training: BFLOAT16 | N/A | Linear scaling and warmup [20]; LARS [26]. | N/A | N/A | Label smoothing [33] |

On one hand, the SPECCPU [34], PARSEC [35], and TPC benchmarks, like TPC-DS [36] witness the paramount importance [10] of being representative and diverse, as no single benchmark or metric can measure the performance of computer systems on all applications [12].

On the other hand, TOP500 [13] defines three distinctive characteristics of the de facto super computer
benchmark standard: affordable, simple, and scalable. Affordable has two implications: first, the benchmark is easy to port to a new system or architecture; second, the benchmarking cost is affordable for measuring a systems at scale. Simple indicates the number of the metric is not only linear, orthogonal, and monotony \[13\], but also easily interpretable and understandable. Scalable means the benchmark can be used to measured different scales of system, and the problem size can be scaled up and down.

In the AI domain, there are massive AI tasks and models with different performance metrics. For example, AIBench \[10\] contains seventeen representative AI tasks, including Image Classification, Object Detection, Learning to Rank, Image Generation, Text-to-Text Translation, Image-to-Text, Image-to-Image Translation, Speech Recognition, Face Embedding, 3D Face Recognition, Recommendation, Video Prediction, Image Compression, 3D Object Reconstruction, Text Summarization, Spatial Transformer, and Neural Architecture Search. For HPC AI benchmarking, it is not affordable to implement so many massive benchmarks and further perform benchmarking at scale.

The traditional micro or kernel benchmarking methodology, which is widely in the HPC communities, can lead to misleading conclusion, as the mixed precision optimizations indeed improve the FLOPS of a micro benchmark like convolution, while significantly impact time-to-quality of an AI task like Image Classification. Fig. 4 shows that the mixed precision implementation increases the FLOPS of both micro and component benchmarks, while incurring accuracy drop as the system scale increases.

Last but not least, the relevancy \[37\] of a benchmark indicates that it must measure the peak performance and price/performance of systems when performing typical operations within that problem domain. The micro benchmark like HPL-AI \[18\], which only contains LU decomposition, is affordable to perform a fair comparison of competing systems by isolating hardware and software from statistical optimizations \[9\]. However, we found it is irrelevant to most of AI workloads in AIBench. As shown in Fig. 3 the dominated kernel functions are convolution and matrix multiplication.

![Figure 3: The kernel function breakdown of the 17 representative AI workloads from AIBench \[10\], indicating the LU factorization is irrelevant.](image)

![Figure 4: With respect to the FP32 implementation, the mixed precision one speeds up 2x the FLOPS of two micro benchmarks: Conv and GEMM and a component benchmark: ResNet-50 (LEFT), while incurring deteriorated accuracy drop of ResNet-50 when the system scale increases (Right): 0.12% at 1 node while about 1% at 8 nodes.](image)
3.3 Repeatability

Repeatability [38,39] refers to the variation in repeat measurements of different runs of the same benchmark implementation, by the same team, on the same system under the identical configurations.

Table 2 shows run-to-run variations of 17 benchmarks from AIBench varying from 0% to 38.46%. As shown in Fig. 5, the variation of 3d Face Recognition is high as 38.46%. There are diverse reasons for the uncertainty of different benchmarks. For NAS (network architecture searching), it constructs the network architecture by randomly sampling building blocks (e.g. convolution) from a predefined search space. In addition, the complex design itself, which involves many hyper-parameters, makes AutoML hard to evaluate [40].

Table 2: The run-to-run variations of seventeen AI benchmarks of AIBench [10]

| No.  | Component Benchmark       | Variation | Repeat Times |
|------|---------------------------|-----------|--------------|
| DC-AI-C1 | Image Classification     | 1.12%     | 5            |
| DC-AI-C2 | Image Generation         | Not available | N/A         |
| DC-AI-C3 | Text-to-Text Translation | 9.38%     | 6            |
| DC-AI-C4 | Image-to-Text            | 23.53%    | 5            |
| DC-AI-C5 | Image-to-Image           | Not available | N/A         |
| DC-AI-C6 | Speech Recognition       | 12.08%    | 4            |
| DC-AI-C7 | Face Embedding           | 5.73%     | 8            |
| DC-AI-C8 | 3D Face Recognition      | 38.46%    | 4            |
| DC-AI-C9 | Object Detection         | 0         | 10           |
| DC-AI-C10 | Recommendation        | 9.95%     | 5            |
| DC-AI-C11 | Video Prediction        | 11.83%    | 4            |
| DC-AI-C12 | Image Compression       | 22.49%    | 4            |
| DC-AI-C13 | 3D Object Reconstruction | 16.07%    | 4            |
| DC-AI-C14 | Text Summarization      | 24.72%    | 5            |
| DC-AI-C15 | Spatial Transformer     | 7.29%     | 4            |
| DC-AI-C16 | Learning to Rank        | 1.90%     | 4            |
| DC-AI-C17 | Neural Architecture Search | 6.15%  | 6            |

Figure 5: The worst unrepeatable benchmark from AIBench is 3D Face Recognition. Its run-to-run variation is high as 38.46%. The variation is defined as the ratio of the standard deviation to the mean of the training epochs to the achieved quality [10].

Without the equivalent benchmarking rules being explicitly stated, ImageNet/ResNet-50 training is not qualified for ranking the performance and energy efficiency of HPC AI systems.
4 Benchmarking Methodology

This section presents our methodology to achieve the goal of being equivalent, relevant, representative, affordable, and repeatable.

4.1 Equivalence

To perform fair benchmarking across different systems or the same system with different scale, we propose two approaches to assure the equivalence.

First, as shown in Fig. 2, we abstract the system under test into nine independent layers, and put each layer under test while keeping the other layers intact unless otherwise stated.

Layer 1 is the hardware, including CPUs and networks. Layers 2, and 3 are the related system software, including the operating system (Layer 2), and the communication libraries (Layer 3). Layer 4 is the AI accelerators, i.e., GPU, and libraries, i.e., CUDA and cuDNN. Layer 5 is the AI framework, such as TensorFlow [41] and PyTorch [42]. Layer 6 refers to programming model, including parallel mode (data parallelism or model parallelism), and synchronous or asynchronous training. Layer 7 refers to the workloads used in HPC AI500 V2.0 benchmark. Layer 8 refers to hyper-parameters policies or settings. Layer 9 refers to problem domain, including datasets, target quality, and epochs.

Second, for the sake of simpleness, we propose three high levels of benchmarking and put several related layers together under test.

1. The hardware level. This high level is for benchmarking HPC AI hardware systems and their related system software (Layers 1, 2, 3, 4). In this context, the other layers should be kept intact unless otherwise stated in the benchmarking rules. The benchmark users should compile the source code of the benchmark implementation, provided by the benchmark committee, on their hardware directly with allowed changes. Luo et al. [43] show that the same model on different frameworks has different accuracy. So in addition to the same data set, and AI model, we mandate that the benchmark implementations also use the same AI framework. The benchmark users can change hardware, OS, compiler settings, communication libraries. For the other layers, the benchmark users can only change parallel modes in Layer 6 or tune learning rate policies and batchsize settings in Layer 8. It is the benchmark committee’s duty to assure the equivalence of Layers 6, 7, 8, 9 across different benchmark implementations upon the users’ requests.

2. The system level. Because of the portability cost, some benchmark users may opt for one specific AI framework without the support of the other, so specifying a fixed framework has a limited purpose. So in the system level, we put the hardware system in addition to the AI framework under the test (Layers 1, 2, 3, 4, and 5), which we call the system level. We mandate that the benchmark implementations use the same data set, and AI model. In addition to the changes allowed in the hardware level, the users are allowed to re-implement the algorithms on different or even customized AI framework (Layer 5). The other layers should be kept intact unless otherwise stated in the benchmarking rules.

The benchmark committee or an independent group need double-check the equivalence of Layers 6, 7, 8, 9 between the two benchmark implementations.

3. The free level. In this high level, the specification of an AI task is stated in a paper-and-pencil manner separating from its specific implementation. That is to say, the same data set, target quality, and training epochs are defined in Layer 9 while the other layers are open for optimizations. The emphasis is advancing the state-of-the-art of software and hardware co-design, so the benchmark users can change any layers from Layer 1 to Layer 8 while keeping Layer 9 intact. Meanwhile, the benchmark users are encouraged to disclose the details.

4.2 Representative vs. Affordable

We investigate and compare the state-of-the-art and state-of-the-practice of AI benchmark suites, including MLPerf [9], AIBench [10], Deep500 [44], HPC AI500 V1.0 [45]. We present the detailed analytics in
Section 9. Fortunately, we found the methodology of AIBench and its subset combines the merits of two methodologies discussed in Section 3.

On one hand, AIBench [10] is by far the most representative and comprehensive AI benchmark suite. It contains seventeen representative AI tasks. These workloads are diverse in terms of model complexity, computational cost, and convergent rate, computation and memory access patterns, hotspot functions, and other micro-architecture characteristics.

On the other hand, for affordability, AIBench carefully selected a minimum subset from the seventeen AI tasks from perspectives of model complexity, computational cost, convergent rate, run-to-run variation, and having widely accepted evaluation metrics or not. As shown in Fig. 6, the AIBench subset includes three AI tasks—Image Classification, Object Detection, and Learning to Rank.

Figure 6: The three subset of AIBench with respect to the full benchmarks [10]. The clustering is based on the patterns of computation and memory access of seventeen AIBench component benchmarks, which described by five metrics listed in Table 3. For visualization, five dimensional data are downscaled into two-dimension ones by the t-SNE clustering approach [46].

Table 3: The metrics used by the t-SNE clustering approach [10].

| Metrics        | Meaning                                                                 |
|----------------|--------------------------------------------------------------------------|
| achieved_occupancy | The ratio of the average active warps per active cycle to the maximum number of warps provided by a multiprocessor |
| ipc efficiency  | The ratio of the executed instructions per cycle to the theoretical number. |
| gld_efficiency  | The ratio of the requested global memory load throughput to the required global memory load throughput |
| gst_efficiency  | The ratio of the requested global memory store throughput to the required global memory store throughput |
| dram utilization | The utilization level of the device memory relative to the peak utilization |

Tang et al. [10] systematically quantify the run-to-run variation of seventeen AI tasks of AIBench in terms of the standard deviation to the mean of the training epochs to achieve a convergent quality. The variation of image classification, object detection, and learning ranking is 1.12%, 0%, and 1.90%, respectively, and they are the most repeatable benchmarks, which is the other reason for including them into the subset.

So we choose the AIBench subset as the HPC AI500 V2.0 candidate benchmarks for implementing scalable HPC AI benchmark tools.
4.3 Repeatability and Replicability

In line with the experimental sciences discussed in [47], we propose the benchmarking procedures for assuring repeatability and replicability [48]. We adopt the definition similar to that of the Association for Computing Machinery [39]. Different from reproducibility, which requires changes, repeatability and replicability avoid changes [47].

Repeatability (same team): The benchmarking is performed on the same HPC AI system, using the same benchmark implementation under the same configurations, following the same benchmarking procedures, on multiple trials [47].

The team should submit the raw data of all trials, including the average numbers in addition to its variations. The variation is measured in terms of the ratio of the standard deviation to the mean of the numbers of all trials.

To mitigate the influence of stochastic of the AI algorithm, each benchmark should mandate the least valid runs of benchmarking. The number of all trials should be more than the least valid runs of benchmarking.

Replicability (Different team) [39]: The replicability refers to that the other team verifies the benchmarking results on the same HPC AI system, using the same benchmark implementation under the same configurations, following the same benchmarking procedures, on multiple trials.

For replicability, The benchmark committee or an independent group need verify the numbers on the same system, and report the raw data of all trials, including the average numbers in addition to its variation.

5 Benchmark Design and Implementation

In this section, we firstly illustrate how to choose the workloads according to our benchmarking methodology (Section 4). Then we present the datasets, AI models, and reference implementations of HPC AI500. Finally, we introduce the metrics.

5.1 How to choose the workloads?

With respect to other AI benchmarks, there are two unique differences of HPC AI benchmarking. First, the challenges of HPC AI benchmarking inherit from the complexity of benchmarking scalable hardware and software systems at scale, i.e., tens of thousands of nodes, significantly different from that of IoT [43] or datacenter [11]. On this point, we need consider the cost of benchmarking at scale. Second, HPC AI domains cover both commercial and high performance scientific computing. Currently, business applications are pervasive. Because of the difficulty of recruiting qualified scientists to label scientific data, the applications in scientific computing lag behind but are promising. In general, the scientific data are often more complex than that of the MINST or ImageNet data: the shape of scientific data can be 2D images or higher-dimension structures with hundreds of channels, while the popular commercial image data like ImageNet often consist of only RGB [45]. So we should include the scientific data in the HPC AI benchmarks.

According to our benchmarking methodology discussed in Section 4, we choose the AIBench subset as the HPC AI500 candidate benchmarks for implementing scalable HPC AI benchmark tools.

5.1.1 Representative and Affordable

As the broad HPC AI applications cover both scientific [5,7,49,50] and commercial field [27,30], we choose the most representative workloads and data sets from these two fields.

EWA is one of the pioneering work that uses deep learning algorithm to replace the rules predefined by human expert and achieve excellent results [5]. Most important of all, the goal of EWA is to identify various extreme weather patterns (e.g. tropical depression), which is essentially object detection—one of
the three benchmarks of the AIBench subset. In 2018, a deep learning based EWA implementation \cite{7} won the Gordon Bell Prize, which is the first AI application to win this award.

**Image Classification** is widely used in many applications of *commercial fields*, which is a fundamental task in AI research. With the developing of large-scale deep earning, Image Classification has become a well-known showcase optimizing HPC AI systems \cite{27,29}, as summarized in Table 1. Image Classification is also one of the three benchmarks of the AIBench Subset.

We exclude Learn to Ranking because it has the lowest computation complexity in terms of FLOPS, which is only 0.08 MFLOPs in terms of a single forward computation. According to \cite{10}, Image Classification and Object Detection is more complex than that by one or two orders of magnitude, respectively.

### 5.1.2 Repeatability

As the stochastic nature of AI, we need to ensure the repeatability by choosing relatively stable workloads in various AI tasks. According to the randomness analytics of AIBench \cite{10}, the two most repeatable AI benchmarks are Object Detection and Image Classification, whose variation is 0% and 1.12%, respectively. So they satisfies the property of a good benchmark–being repeatable.

### 5.1.3 Scaling Characteristics

For comprehensive evaluation, the workloads we choose have distinct characteristics in terms of scaling characteristics. We use scaling ratio to depict the difficulty when scaling a workload from a single node to multiple nodes. As shown in Table 5, the scaling ratio of EWA and Image Classification is 16.85 and 117.76, respectively, reflecting very different scaling characteristics.

### 5.1.4 Different Levels of Stringent Quality Requirements

When ranking HPC system, we consider not only its performance, but also the achieved quality. Different AI tasks have different levels of stringent quality requirement. Our benchmark decision also consider this factor. In our two benchmarks, EWA has much more stringent quality requirement than that of Image Classification.

### 5.2 Data sets and AI models

#### 5.2.1 EWA

**Dataset.** The EWA dataset \cite{50} is made up of 26-year climate data. The data of every year is available as one HDF5 file. Each HDF5 file contains two data sets: images and boxes. The images data set has 1460 example images (4 per day, 365 days per year) with 16 channels. Each channel is 768 * 1152 corresponding to one measurement per 25 square km on earth. The box dataset records the coordinates of the four kinds of extreme weather events in the corresponding images: tropical depression, tropical cyclone, extratropical cyclone and the atmospheric river.

**Model.** Faster-RCNN targets real-time Object Detection \cite{51}. As one of the latest models of an RCNN family \cite{52,55}, it deprecates the selective search that has been used in the previous RCNN version. Instead, Faster-RCNN proposes a dedicated convolutional neural network, named region proposal network (RPN), to achieve nearly cost-free region proposals. With such design, Object Detection is much faster. As a result, Faster-RCNN wins the 1st-place entries in ILSVRC’15 (ImageNet Large Scale Visual Recognition Competition).

**Quality** The target quality is $\text{MAP}@[\text{IoU} = 0.5] = 0.35$, which is our best training result. MAP means the average precision, which is a dedicated metric for object detection. The IoU means the intersection over union, used to measure how much our predicted boundary overlaps with the ground truth.
5.2.2 Image Classification

**Dataset.** ImageNet [2] is a large visual database designed for use in visual object recognition research. More than 14 million images have been hand-annotated according to the WordNet hierarchy. Both the original images and bounding boxes are provided. The data size is more than 100 GB.

**Model.** ResNet is a milestone in Image Classification [54], marking the ability of AI to identify images beyond humans in a particular domain. The spirit of ResNet is its success in reducing the negative impact of the degradation problem. The degradation problem means in the very deep neural network, the gradient will gradually disappear in the process of back-propagation, leading to poor performance. Therefore, with ResNet, it is possible to build a deeper convolution neural network and archive the higher accuracy. Researchers successfully build a ResNet with 152 layers. This ultra-deep model won all the awards in ILSVRC’15.

**Quality** The target quality is Top1 Accuracy = 0.763, which is the highest accuracy by far in training ImageNet/ResNet50 at scale [30]. The Top-1 accuracy refers to that only the output with the highest probability is the correct answer.

| Table 4: The Summary of Image Data Sets of HPC AI500 V2.0 Benchmarks |
|---------------------------------------------------------------|
| **Dataset** | **Channels** | **Resolution** | **Size** |
| The extreme weather dataset [50] | 16 | 768*1052 | 558 GB |
| ImageNet dataset [2] | 3 | 256*256 | 137 GB |

| Table 5: The scaling ratio of HPC AI500 v2.0 workloads |
|---------------------------------------------------------------|
| **Workloads** | **Comm (Parameters/Step)** | **Comp (GFLOPs/Step)** | **Comp/Comm (GFLOPs/Parameters)** |
| EWA | 41 million | 691 | 16.85 |
| Image Classification | 25 million | 2944 | 117.76 |

5.3 Reference Implementation

The reference implementation of HPC AI500 V2.0 benchmark is summarized as shown in Table 6. At present, we provide the implementations using TensorFlow [41], which is a popular deep learning framework in the HPC community [55]. For communication, we adopt Horovod [56] instead of the default GRPC protocol in TensorFlow, which is not extendable for large-scale cluster [57] due to the limitation of the master-slave architecture and socket-based communication. Horovod is a library originally designed for scalable distributed deep learning using TensorFlow. It implements all_reduce operations using ring-based algorithms [58] and other high efficient communication algorithms that are widely used in the traditional HPC community.

5.4 Metrics and Scoring Rules

5.4.1 Valid FLOPS

We propose two metrics, called Valid FLOPS (in short VFLOPS) and Valid FLOPS per watt (in short VFLOPS per watt), to quantify the valid performance and energy efficiency that consider both the system throughput and model quality. The goal of these two metrics is to impose an penalty on failing to achieve a target quality. VFLOPS and VFLOPS per watt is calculated according to the formulas as follows.

\[ VFLOPS = FLOPS \times \text{penalty\_coefficient} \]  

(1)
The penalty coefficient is used to penalize or award the FLOPS if the achieved quality is lower or greater than the target quality. Its definition is described as follows:

\[
\text{penalty\ coefficient} = \left(\frac{\text{achieved\ quality}}{\text{target\ quality}}\right)^n
\]

Here, \( \text{achieved\ quality} \) represents the actual model quality achieved in the evaluation. \( \text{target\ quality} \) is the state-of-the-art model quality that has been predefined in our benchmarks. The value of \( n \) is a positive integer, which is used to define the sensitivity to the model quality. The higher the number of \( n \), the more loss of quality drop. As EWA has much more stringent quality requirement than that of Image Classification. We set \( n \) as 10 for EWA and 5 for Image Classification by default.

We propose VFLOPS per watt to evaluate energy efficiency.

**Table 6: HPC AI500 V2.0 benchmark suite.**

| Problem Domains | Models | Datasets | Target Quality | AI Frameworks | Comm Lib\(^1\) | AI Acc Lib\(^2\) | Epochs |
|-----------------|--------|----------|----------------|---------------|----------------|----------------|--------|
| EWA             | FasterRCNN \[51\] | EWA \[50\] | mAP@[IoU=0.5]=0.35 | TensorFlow   | Horovod       | CUDA, cuDNN, NCCL | 50     |
| Image Classification | ResNet50 v1.5 \[54\] | ImageNet \[2\] | TOP 1 Accuracy=0.763 | TensorFlow | Horovod       | CUDA, cuDNN, NCCL | 90     |

\(^1\) Comm Lib refers to the communication libraries.
\(^2\) AI acc lib refers to AI accelerators libraries.

### 6 Benchmarking Rules and Procedures

For the fairness and equivalence of benchmarking different HPC AI systems, a series of clear and unambiguous benchmarking rules are mandatory.

Our fundamental benchmarking rule is that we put each independent layer (Shown in Fig. 2) under test while keeping the other layers intact.

Furthermore, for the hardware-level and system-level benchmarking presented in Section 4, we give a detailed description from perspectives of each layer. Finally, we introduce the benchmarking procedures.

#### 6.1 The Benchmarking Rules for the Hardware Level

Based on our nine-layer model (Fig. 2), we specify the rules of each layer from top to bottom.

**6.1.1 Problem Domain Layer**

- The dataset and target quality must be in accordance with the specification of HPC AI500 V2.0 benchmark that we have discussed in Section 5.
- The training epoch number should be the same like the reference implementation to guarantee the equivalent computational cost, namely 90 epochs for ImageNet and 50 epochs for EWA. Note that an epoch is an iteration over the entire data set, while a step refers to one update of the model parameters. The number of epochs is based on our experimental observation, and it should be updated in the future as well as the target qualities.

**6.1.2 Hyper-parameters Setting Layer**

The rules of hyper-parameters setting layer include three parts, namely batchsize setting, learning rate policies, and other hyper-parameters settings.
**Batchsize Setting**  The batchsize of a training step is allowed to change, to fully utilize the computing capability of the system.

**Learning Rate Policies**  Previous work shows the increase of batchsize leads to a fall of the model quality [59]. In this context, many learning rate policies are proposed [19][20][26][60]. With state-of-the-art learning rate policies, we can increase the training batch size to fully utilize the hardware’s resources while preserving the model quality at the same time. As each learning rate policy has its limitation in terms of the maximum supporting batchsize, our rule allows benchmark users to propose new learning rate policies to fully utilize the hardware’s resources. Meanwhile, we provide a default learning rate policy.

**The default learning rate policy:**  The default learning rate policy of HPC AI500 is a linear scaling rule and a warm-up rule. The description is as follows:

- A linear scaling rule: multiply the base learning rate $\eta$ by $k$ when the batch size is multiplied by $k$. The goal of the linear scaling rule is to make SGD updates similar in both distributed and single-worker training [19].

- A warm-up rule: gradually increase the learning rate from a small to a large number until it equals to $\eta \times k$. After warmup, the learning rate starts the original learning rate schedule (e.g. cosine decay). The warm-up rule is proposed since using linear scaling rule alone breaks down when the weight of the neural network is changing rapidly in the early training stage [19].

Fig. 7a shows the learning rate changing curve after applying linear scaling and warm-up rules. We also perform a series of experiments to show the effect of this policy on model quality. As shown in Fig. 7b, linear scaling and warm-up rules can improves the top1 accuracy from 61.48% to 76.34% in Image Classification when the batchsize is 8192.

![Learning rate curve](image1.png) ![Accuracy curve](image2.png)

*Figure 7:* The learning rate curve and its effect on accuracy with linear scaling and warm-up rules. The benchmark is Image Classification and the system scale is 64 GPUs. The experiment configuration is consistent with that of Table 9. The batchsize is 8192.

**Other learning rate policies:**  Except for the linear scaling and warmup scheme, using state-of-the-art learning rate policies (e.g. LARS [26] and LAMB [60]) are allowed. For new proposed ones, benchmarking users should open source their methods.

**Other Hyper-parameters Setting**  Except for batchsize and learning rate policy, other hyper-parameters such as weight decay, momentum must be as the same as the reference implementation.
6.1.3 Workload Layer

The AI algorithms in the workload must be the same as the reference implementation.

6.1.4 Programming Model Layer

- Data parallelism and model parallelism are both allowed as long as the mathematical equivalence is preserved.
- Synchronous Stochastic Gradient Descent (SGD) must be used in training, since asynchronous SGD may a) introduce the randomness, b) destroy the mathematical equivalence, c) decrease the accuracy.

6.1.5 AI Framework Layer

The AI framework must be the same as the reference implementation.

6.1.6 Communication Libraries Layer

In synchronous communication, the workers in the cluster must wait until all the workers have finished, to proceed to next iteration. We allow different communication policies in an synchronous mode.

| Table 7: Some common communication typologies of allreduce. |
|----------------------------------------------------------|
| **Topologies**    | **Applications** |
|-------------------|------------------|
| Butterfly         | OpenMPI [61]     |
| Double binary tree| NCCL [62]        |
| Ring              | Baidu DeepSpeech [63], Horovod [56] |
| Hierarchical ring | Horovod          |

- Based on AllReduce. Table 7 shows the common topology used in AllReduce implementations. The benchmark users are allowed to utilize these existing ones or propose new typologies according to the configuration of the systems. For example, the researchers from Lawrence Berkeley National Laboratory archived Exascale FLOPS by customizing a communication topology of AllReduce on SUMMIT [7].

- Based on MapReduce. The communication topology is determined by the implementation of MapReduce. The distributed training of Spark MLlib, SystemML, and REEF are all based on MapReduce. Users are allowed to implement customized MapReduce on their systems.

- Based on parameter server. It is mandatory that only the synchronous mode is used for the parameter server, while it also supports asynchronous training.

6.1.7 The AI Accelerators and Libraries Layer

- Benchmark users can choose the AI accelerator library to achieve the best performance out of the system.
- The single-precision floating point (FP32), half precision (FP16, BFLOAT16 [31]), and quantization (INT8, INT4) are allowed.
6.1.8 OS Layer

- Benchmark users can adjust OS configurations (such as CPU-Affinity setting) to achieve the best performance out of the system.

- Benchmark users can choose ‘-O2’ compiler optimization option when compiling the benchmarks and the run time environment software.

6.1.9 Hardware Layer

Benchmark users can adjust hardware configurations (such as hyper-threading setting, memory-prefetching setting) to achieve the best performance out of the system.

6.2 The Rules for The System Level

As discussed in Section 4.1, in the system level, we put the hardware system in addition to the framework under test. Therefore, in addition to the rules defined in the hardware level, benchmark users are allowed to reimplement the benchmark using a different or even customized AI framework at the AI framework layer.

6.3 The Benchmarking Procedures

6.3.1 Deployment

Benchmark users need to download the source code of the benchmarks from the Benchcouncil Web site.

6.3.2 Measurement

- Timing rules: timing starts when the workload reads the first batch training data and ends when the target epochs is reached.

- Runs: according to the variation of EWA and Image Classification from Table 2, the least number of runs is 5 and 10, respectively, to reduce run-to-run variation. For reporting, we drops the runs with the highest and lowest variations, than calculate the arithmetic mean of the remaining results.

- Benchmarking scores:
  1) time-to-quality is the training time to its achieved quality;
  2) FLOPS refers to the single-precision floating point operations (or equivalent operations) per second. The equivalent operations of the single-precision floating point operations include but not limited with FP16, BFLOAT16, INT8, and INT4;
  3) VFLOPS and VFLOPS per Watt refers to the definitions in Section 5.4.1

6.3.3 Reporting Procedure

The reporting results should include the following parts:

- The description of system under test, including but not limited to:
  1) detail descriptions of parameters of CPUs and AI accelerators in a single-node;
  2) detail descriptions of parameters of intra-node connection in a single-node;
  3) detail descriptions of parameters of OS in a single-node;
  4) detail descriptions of parameters of run time environment software in a single-node;
  5) detail descriptions of parameters of inter-node connection in the system;
  6) detail descriptions of parameters of run time environment software in the system.
• Benchmark configurations, including but not limited to:
  1) all hyper-parameter setting;
  2) detail descriptions of communication.

• Benchmarking scores, including time-to-quality, FLOPS, FLOPS per Watt, VFLOPS and VFLOPS per watt in all runs. These metrics should be submitted with the output log of the benchmark.

• The source code, relevant document, and running script should be uploaded to Benchhub, which is the official code repository managed by BenchCouncil.

The BenchCouncil community is responsible for checking the replicability of the reported results and reviewing the code.

### 6.4 Why Equivalent Benchmarking Rules Matter?

A lot of previous work \cite{27,30} focuses on accelerating Image Classification/ResNet-50 training. These efforts reduce the training time from hours to minutes. In this section, we take Image Classification as an example to explain why equivalent benchmarking rules matter for fair ranking HPC AI systems.

Batch normalization is a common effective method to improve the model generalization \cite{64}. The trainable parameters of batch normalization $\gamma$ and $\beta$ are used to restore the representation ability of the network. Jia et al. \cite{29} propose eliminating the weight decay on $\gamma$ and $\beta$ of batch normalization layer, which is a significant algorithm innovation in their work. We re-implement this algorithm-level optimization in accordance with \cite{29}. Further, we use the VFLOPS as the metric to quantify the performance gap.

The benchmarking results are shown in Table 8. The accuracy gain and corresponding VFLOPS ratio are reported against the one without removing the weight decay. We find that as the system scale becomes larger, this optimization has a greater impact on the achieved quality. The accuracy gain is 0.45% on the scales of 16 and 32 GPUs, and then jumps to 1.38% on the scale of 64 GPUs, which is a notable improvement. We calculate the VFLOPS ratio according to the formula discussed in Sec 5.4 for each system scale. On the system scale of 64 GPUs, the VFLOPS ratio is high as 1.10, which is essentially the gain contributed solely by the algorithm innovation.

Consider the following case: we perform a comparison between two HPC AI systems using the same benchmark. One benchmark user leverages this algorithm innovation, while the other does not. If we do not exclude this case in the benchmarking rules, the benchmarking results will be unfair. That is the reason why we mandate that the other hyper-parameter settings in Layer 8 must keep intact as shown in Fig. 2.

Someone may question why we allow changing learning rate policies in Layer 8 in our rules as shown in Fig. 2. Just as discussed in Section 6, this is because to fully utilize the hardware resources, the users have to change the learning rate policies.

| System Scale | Batchsize | Accuracy Gain | VFLOPS Ratio$^1$ |
|--------------|-----------|---------------|------------------|
| 16 GPUs      | 2048      | +0.45%        | 1.03             |
| 32 GPUs      | 4096      | +0.45%        | 1.03             |
| 64 GPUs      | 8192      | +1.38%        | 1.10             |

$^1$ The VFLOPS ratio refers to the ratio of the VFLOPS after the optimization against the one without optimization.
7 The HPC AI Roofline Performance Model

Given a specific HPC AI system, the theoretical peak performance number can be calculated according to hardware configurations. However, the theoretical peak one is hard to achieve. Hence, we need a performance model to help achieve the upper bound performance of an HPC AI system.

The previous Roofline model \[65\] is a upper bound performance model based on FLOPS and operation intensity (OI)—the total number of floating point instructions divided by the total byte number of memory accesses. With the aid of a Roofline model, we can decide a workload is memory-bound or compute-bound. Moreover, potential optimization strategies can be recommended according to the different ceilings of the Roofline model. To date, there is no such a performance model available for HPC-AI systems. In this section, we first analyze the distinctive characteristics of an HPC-AI system, and then propose an HPC-AI Roofline Model.

7.1 The Architecture of an HPC AI System

An HPC AI system is a distributed system consisting of multiple nodes, each of which is heterogeneous and equipped with multiple CPUs and AI accelerators, as shown in Fig 8. The CPUs of each node are responsible for scheduling tasks and communicating with other nodes. The AI accelerators are responsible for AI calculations. Each AI accelerator loads or stores data from its memory units through memory channels. And all AI accelerators of each node are connected with a specific high-speed network (e.g. NVLink for GPUs). The distributed nodes are interconnected by a general high-speed network (e.g. high speed Ethernet). Hence, the communications include both inter-node and intra-node ones. Our analytics in Section 8.4 reveals the communication efficiency is one of the dominant factors that impact its performance.

When proposing HPC-AI Roofline models, we consider the distinctive characteristics of HPC AI systems and the huge impact of communication efficiency on the performance of HPC AI systems. Significantly different from the original Roofline model \[65\], which emphasizes the impact of computation (FLOPS) and memory access (OI) on the overall performance, our HPC-AI Roofline model emphasizes the impact of communication and computation. We propose an innovative metric, named communication operation intensity (in short, COI), to replace OI. COI is defined as the total number of floating point instructions divided by the total byte number of communication.

Considering the different communication modes of inter-node communication (general high speed network) and intra-node communication (specific high speed network), our HPC-AI Roofline model is a combination of a single-node model with a distributed model.
We use FLOPS as the metric to depict the upper bound performance. Unlike the original Roofline model\cite{65} using the double-precision floating point operations per second, we use the single-precision floating point operations or equivalent operations, such as mixed-precision floating point operations per second. This is because double-precision floating point operations are rarely required for deep learning workloads, while single-precision or mixed-precision floating point operations are prevalent.

Intentionally, we do not choose VFLOP as the performance metric. This is because the purpose of the Roofline model is to decide the performance bound of the workload and guide its system-level and hardware-level optimizations. Instead, VFLOP is a composite metric reflecting both performance and accuracy to rank the HPC AI systems.

### 7.2 The Single-Node HPC-AI Roofline Model

The single-node HPC-AI model is formulated as follows.

\[
\text{FLOPS}_{\text{Attained}} = \min(\text{FLOPS}_{\text{Peak}}, \text{ComBand}_{\text{Peak}} \times \text{COI})
\]  

(3)

\(\text{ComBand}_{\text{Peak}}\) is the theoretical peak communication bandwidth of a single-node HPC AI system, which is the bandwidth of interconnections among AI accelerators. \(\text{FLOPS}_{\text{Peak}}\) is the theoretical peak FLOPS of a single-node HPC AI system, which is the aggregate theoretical peak FLOPS of all AI accelerators. The communication operation intensity--\(\text{COI}\)--is obtained by \(\text{COI} = \frac{\text{FLOPS}}{\text{CT}}\) where \(\text{CT}\) is short for the communication traffic--the total number of communication bytes among AI accelerators. To more accurately reflect the performance bottleneck of a given workload, different ceilings are added to help locate the bottlenecks and provide potential optimization recommendations.

We use CONV (convolution) and GEMM (GEneral Matrix to Matrix Multiplication) to measure the upper bound performance of the system. On one hand, they are two most frequently-appearing kernel functions of the seventeen benchmarks of AIBench; On the other hand, their computing patterns, i.e., their multiplying and adding calculations can be fused, allow them to make more efficient use of accelerators. \(\text{FLOPS}_{\text{Attained}}\) is the performance that a workload can attain, and the attained performance bound of a given workload under ceilings is formulated as follows.

\[
\text{FLOPS}_{\text{Attained}} = \min(\text{FLOPS}_{\text{Ceiling}}, \text{ComBand}_{\text{Ceiling}} \times \text{COI})
\]  

(4)

### 7.3 The Distributed HPC-AI Roofline Model

For the distributed model, we propose using COI (communication operation intensity) and FLOPS to depict the upper bound performance. The model is formulated as follows.

\[
\text{FLOPS}_{\text{Attained}} = \min(\text{FLOPS}_{\text{Peak}}, \text{ComBand}_{\text{Peak}} \times \text{COI})
\]  

(5)

The \(\text{ComBand}_{\text{Peak}}\) is the theoretical peak communication bandwidth of the distributed system, i.e., the theoretical bandwidth of the high speed Ethernet. \(\text{FLOPS}_{\text{Peak}}\) is the theoretical peak FLOPS of the distributed system, which is the aggregate theoretical FLOPS of all AI accelerators in the distributed system. The communication operation intensity--\(\text{COI}\)--is obtained by \(\text{COI} = \frac{\text{FLOPS}}{\text{CT}}\), where the communication traffic--\(\text{CT}\)--is the total byte number of communications among all AI accelerators in the distributed system. To more accurately reflect the performance bottleneck of a given workload, we add several ceilings, and the attained performance bound of a given workload is formulated as follows.

\[
\text{FLOPS}_{\text{Attained}} = \min(\text{FLOPS}_{\text{Ceiling}}, \text{ComBand}_{\text{Ceiling}} \times \text{COI})
\]  

(6)
7.4 A Case Study of the HPC-AI Roofline Models

We perform a case study of our HPC AI Roofline models on an experimental system. The system consists of eight nodes, each of which is equipped with one Intel(R) Xeon(R) Platinum 8268 CPU and eight NVIDIA Tesla V100 GPUs. Each GPU in the same node has 32 GB HBM memory, connected by NVIDIA NVLink high-speed GPU interconnection that has theoretical peak 300GB/s bi-directional bandwidth. The nodes are connected with an Ethernet networking with a bandwidth of 10 Gb/s. Each node has 1.5 TB of system memory and 8 TB of NVMe SSD disk.

7.4.1 A Case Study of the Single-Node HPC-AI Roofline Model

As shown in Fig. 9a, the y-axis is the performance in terms of floating-point operations per second, while the x-axis is the communication operation intensity—the floating-point operations divided by the total byte number of communication. In Fig. 9a, the peak computation rate forms the ‘flat’ part, while the communication bandwidth turns into the ‘slanted’ part. So, if the communication operation intensity is lower, the workload is communication-bound, under the slanted part of the roofline. With the sufficient communication operation intensity, the workload is compute-bound.

We add four computation ceilings: mixed-precision GEMM (the performance of the mixed-precision floating point implementation of GEMM), single-precision GEMM, mixed-precision CONV, and single-precision CONV. Single-precision setting is commonly-used in the AI domain, while mixed-precision is one of the optimization features on some advanced AI accelerators.

The best-case performance of eight GPUs is that the communication and computation totally overlap, and the memory bandwidth becomes the bottlenecks. We add one communication ceiling – memory bandwidth. In Fig. 9a, the theoretical peak number of mixed-precision FLOPS, the mixed-precision GEMM ceiling, the mixed-precision CONV ceiling, the single-precision GEMM ceiling, the single-precision CONV ceiling is 1040 TFLOPS, 636 TFLOPS, 176 TFLOPS, 115 TFLOPS, 112 TFLOPS, respectively. Note that the gap between the theoretical peak number with the actual one is because that the performance of CONV and GEMM is affected by the dimension and sparsity of input data, NCHW format and output channels. Additionally, the convolution kernel also impacts the performance of CONV greatly. The different input size of CONV and GEMM leads to different performance numbers. The NVLink ceiling is the theoretical peak bandwidth of the communications among GPUs~300 GB/S, and the memory bandwidth ceiling is the theoretical peak bandwidth of the memory~1134 GB/S.

7.4.2 A Case Study of the Distributed HPC-AI Roofline Model

Our system consists of eight nodes. All the GPUs in the same node are connected by NVIDIA NVLink, and the nodes are connected with an Ethernet networking. In Fig. 9b, the peak computation rate forms the
Table 9: Hardware configuration details.

| System Configurations | Single-Node Configurations |
|------------------------|-----------------------------|
| Num of Nodes           | 8                           |
| CPU Type               | Intel(R) Xeon(R) Platinum 8268 CPU |
| GPUs per Node          | 8                           |
| Memory                 | 1.5TB, DDR4                 |
| Total num of GPUs      | 64                          |
| Disk                   | 8TB, NVxMe SSD              |
| Peak Theoretical performance (FP32) | 960 TFLOPS          |
| GPU Type               | Nvidia Tesla V100           |
| Peak Theoretical performance (Mixed) | 7680 TFLOPS               |
| GPU Memory             | 32GB, HBM                   |
| Interconnection        | Ethernet, 10Gb/s            |
| Intraconnection        | NVLink                      |

‘flat’ part, while the communication bandwidth (Ethernet networking bandwidth) turns into the ‘slanted’ part. The theoretical Peak FLOPS of the system is 8320 TFLOPS, and the communication ceiling is 1.2 GB/S.

We add four computation ceilings: mixed-precision GEMM, single-precision GEMM, mixed-precision CONV, and single-precision CONV. Their numbers are 5091, 920, 2376, and 976 TFLOPS, respectively.

The best-case performance of the HPC-AI system is that the communications are within the nodes. So we add one communication ceilings–NVLink bandwidth. The NVLink bandwidth ceiling is 300 GB/S.

8 Evaluation

In this section, we introduce the experimental configurations in Section 8.1, present how to measure FLOPs in Section 8.2. Then, we perform an in-depth performance analysis of a single node in Section 8.3 and multiple nodes in Section 8.4 respectively. Finally, we demonstrate how to use our roofline model to guide the optimizations of the HPC AI systems in Section 8.5.

8.1 Experimental Configurations

Our experiments are conducted on an HPC AI system, consisting of eight nodes, each of which is equipped with one Intel(R) Xeon(R) Platinum 8268 CPU and eight NVIDIA Tesla V100 GPUs. Each GPU in the same node has 32GB HBM memory, connected by NVIDIA NVLink–a high-speed GPU interconnection whose theoretical peak bi-directional bandwidth is 300GB/s. The nodes are connected with an Ethernet networking with a bandwidth of 10 Gb/s. Each node has 1.5 TB system memory and 8 TB NVMe SSD disk.

The details of the architecture of each NVIDIA Tesla V100 GPU–NVIDIA Volta architecture are as follows. The NVIDIA Volta architecture is equipped with 640 Tensor Cores to accelerate GEMM and convolution operations. Each Tensor Core performs 64 floating-point fused-multiply-add (FMA) operations per clock, delivering up to 125 TFLOPs of theoretical peak performance. When performing mixed precision training with a Tensor Core, we uses FP16 for calculation and FP32 for accumulation [18].

We use TensorFlow v1.14, compiled with CUDA v10.1 and cuDnn v7.6.2 backend. We use Horovod v0.16.4 for synchronous distributed training, compiled with OpenMPI v3.1.4 and NCCL v2.4.8. NCCL is short for the NVIDIA Collective Communications Library, which is a closed-source library of multi-GPU collective communication primitives that are topology-aware.

8.2 Performance Measurement

The source-code level measurement of FLOPs is difficult for a complex AI model implemented with a complex AI framework. The mainstream frameworks like TensorFlow and PyTorch adopt computational graphs and map them to specific computing engines, e.g., GPU and cuDNN. This process invokes numerous kernels, and each of which contributes to a portion of FLOPs. Hence, we need to figure out the
implementation of each invoked kernel to obtain the FLOPs of an entire AI model. Unfortunately, the source code is not publicly available as the NVIDIA libraries, like CUDA and cuDnn, are not open source.

We use NVProf [66]—a performance analysis tool for NVIDIA GPUs—to measure the FLOPs in our experiments. NVProf can be used to collect the profiling data from hardware performance counters. But it has a huge overhead, slowing down the execution time more than hundreds of times. Thus, profiling the whole training session of a deep learning model is prohibitively costly. The previous work [67, 68] has found that each iteration of model training has the same computation logic and the iteration number has little impact on micro-architectural behaviors. So we sample a partial training set and calculate the FLOPs for efficiency. As the image size of the EWA and ImageNet datasets is 13.14k and 1280k, respectively, so we sample 500 images and 12800 images from the EWA and ImageNet datasets, respectively. The throughput is calculated according to the following equation: 

\[ \text{Throughput} = \frac{N \times R \times C}{T} \]

Here, N is the number of images processed by each training process per second, R is the total number of ranks (the number of training processes), and C is the FLOPs per image.

| Dataset               | Image Sample Size | Total FLOPs   | FLOPs Per Image |
|-----------------------|-------------------|---------------|-----------------|
| EWA                   | 500               | 345.66 TFLOPs | 691 GFLOPs      |
| Image Classification  | 12800             | 2877.06 TFLOPs| 23 GFLOPs       |

Table 11: The performance summary of a single node

| Workloads       | Models             | Precision | GFLOP (Per Image) | Throughput (Images/s) | Attainable Performance¹ (TFLOPS) | Achieved Performance Ratio² (%) |
|-----------------|--------------------|-----------|-------------------|-----------------------|----------------------------------|---------------------------------|
| Image Classification | ResNet-50 V1.5 | FP32      | 23                | 2624                  | 58                               | 48                              |
|                 | Mixed³             |           |                   | 5734                  | 126                              | 105                             |
| EWA             | FasterRCNN         | FP32      | 691               | 46                    | 31                               | 26                              |

1 The attainable performance refers to the performance obtained in the testing.
2 The achieved performance ratio refers to the ratio of the attainable performance against the theoretical peak performance (FP32).
3 Mixed refers to FP32 & FP16 mixed precision.

Figure 10: The details of single-node performance analytics of Image Classification and EWA. We classify the kernels invoked on the GPU into eight categories and use three metrics to depict their characteristics: the proportion of time, instruction per cycle (IPC) and dram utilization. The GPU utilization during the overall training session is also recorded. An asterisk (*) is used to indicate the number is negligible, less than 0.001%.
8.3 Single-node Evaluation

In this subsection, we first report the execution efficiency on a single node, and then perform communication and computation analytics to recover the factors that impact the performance significantly. We use the HPC AI500 V2.0 benchmarks.

8.3.1 Performance Efficiency

Based on the methodology described in Section 8.2, we report the performance efficiency of two benchmarks on a single node: Image Classification and EWA. We evaluate both the FP32 precision and mixed precision implementations, which uses the Tensor Core to accelerate the training session. As the memory footprint required by the mixed precision implementation is nearly a half of that of FP32 precision, we double the batch size in each training step for mixed precision without breaking the benchmarking rule defined in Section 6. Table 11 shows the performance efficiency of the above two benchmarks. The achieved performance ratio is the ratio of the attainable performance against the theoretical peak performance of the FP32 precision implementation. In our experiments, the theoretical peak number is 120 TFLOPS, which is the theoretical peak performance of the single-precision (FP32) implementation (15 TFLOPS) multiplied by 8—the number of NVIDIA Tesla V100 SXM2 GPUs. From Table 11, we find that the performance efficiency of EWA is extremely low with respect to that of Image Classification. We further characterize their computation and communication characteristics to uncover the factors.

![Horovod Communication Timeline](image)

**Figure 11:** The timeline of Horovod communication.

8.3.2 Communication and Computation Analytics

We first perform communication analytics using a timeline analysis tool [69] to record all activities of the Horovod communication, since its synchronous distributed manner may significantly affect the performance. As shown in Fig. 11, the communication timeline of Horovod is divided into two phases: negotiation and processing. In the negotiation phase, all training processes send a signal to the first process to ensure their status are ready for the subsequent tensor reduction. In the processing phase, the tensor reduction is performed. Specifically, the processing phase is further divided into six steps. Steps 1 (Wait_for_data) and 2 (Wait_for_other_data) are waiting for the data produced by GPU computing, which is the input to all_reduce operations. Step 3 (Queuing) happens only when the previous all_reduce has not finished. Steps 4 (Memcpy_in) copies data into the fusion buffer. Step 5 (NCCL Allreduce) is the core part that executes all_reduce operation across all the training processes. Steps 6 (Memcpy_out) removes the data out of the fusion buffer.

We profile the average wall clock time of all steps and compare EWA against Image classification. We find the long negotiation phase is one main factor that leads to inefficient communication of EWA. As shown in Table 12, the average negotiation allreduce of EWA accounts for 28.5% of the total duration of Horovod communication, 2.5 times than that of Image classification. The root cause is the side effect of the centralized schedule strategy of the Horovod negotiation. As mentioned before, the first process during...
Table 12: The time breakdown of the Horovod communication.

| Phases            | Steps                  | EWA   | Image Classification |
|-------------------|------------------------|-------|----------------------|
| Negotiation       | Negotiation Allreduce  | 54.837 ms | 22.836 ms           |
| Processing        | Wait_for_data          | 1.746 ms  | 85.418 ms          |
| Processing        | Wait_for_other_data    | 2.961 ms  | 27.036 ms          |
| Processing        | Queuing                | 65.863 ms | 0.043 ms           |
| Processing        | Memcpy_in              | 0.108 ms   | 1.256 ms           |
| Processing        | NCCL Allreduce         | 66.228 ms | 4.153 ms           |
| Processing        | Memcpy_out             | 0.197 ms   | 0.993 ms           |

the negotiation acts as a centralized scheduler to avoid deadlock by reordering all the all_reduce operations across processes. It receives the message from all processes and sends back the correct tensor list that should be reduced. EWA needs to execute all_reduce operation more than one hundred times and has about 41 millions of gradients in total to be reduced during each training step, and thus spends too much time on the first process. Another factor is the sub-optimal overlap between computation and communication. According to Table 12, we find the total duration of wait_for_data and wait_for_other_data in EWA and Image Classification is 4.6, 112.4 ms, respectively; in the duration of NCCL Allreduce it is 66.2 ms and 4.15 ms in EWA and Image Classification, respectively. These numbers indicate EWA has a worse overlap between computation and communication than that of Image classification. Besides, queuing is up to about 65.8 ms, showing the NCCL Allreduce operation has to wait for a longer duration. Accordingly, the duration of queuing and wait_for_data of Image Classification is 0.043 and 85.4 ms, respectively, indicating Image Classification has better overlap between communication and computation than that of EWA.

In addition to the communication analytics, we also conduct computation analytics through a thorough profiling of GPU activities using NVProf [66]. Fig. 10 shows the results. There are thousands invocations of CUDA kernel during each training step. For simplicity, we classify all the kernel functions into eight categories. Each category represents a kind of operation, namely convolution, GEMM, batch normalization, element wise, pooling, memcpy, NCCL Allreduce, and transformation. For EWA, we find NCCL Allreduce (35.97%) and memcpy operations occupy 50.62% in total, leading to poor performance. For ImageNet Classification, the most time-consuming kernel is convolution, namely 35.02% and 22.18% in the FP32 and mixed precision implementations, respectively. We also notice the overhead of data arrangement occupies 15.61% in the mixed precision implementation, while less than 0.0001% in the FP32 implementation. The huge overhead in the mixed precision implementation is incurred by converting different data layouts between the TensorFlow and CUDA kernels. The data layout of the TensorFlow kernels is represented in a quadruple tuple (batch size, height of data sample, width of data sample, channels), abbreviated as NCHW. While, the data layout of the CUDA kernels is represented in a quadruple tuple (batch size, height of data sample, width of data sample, channels), abbreviated as NHWC. That inconsistency incurs a huge overhead. It explains why the speedup of mixed precision version of Image Classification is only 2.16x. It is much smaller than the results published by Nvidia [70], which claims that the mixed precision training can bring up to 8x speed up on the Tesla V100 GPU.

8.4 Multiple-node Evaluation

We perform several scaling experiments on the distributed system, described in Section 8.1. Both EWA and Image Classification experiments are scaled out from 8 GPUs to 64 GPUs. We take the 8-GPU experiments (single node) as a baseline. Our communication topology is the double binary tree [62], which is implemented by NCCL 2.4. We report the performance numbers of these experiments and
8.4.1 Image Classification

For the FP32 precision implementation of Image Classification, the parallel efficiency is 0.91, 0.85 and 0.71 on 16, 32 and 64 GPUs, respectively. For the mixed implementation, the parallel efficiency is slightly lower: 0.89, 0.82 and 0.67, respectively. There is a notable loss of parallel efficiency when the system scale is 64 GPUs.

We also notice that the communication compression does not bring any performance improvement when the system scale is 32 GPUs or less. However, when the scale is 64 GPUs, it contributes a lot. For the FP32 version, the performance improves from 345 to 414 TFLOPS. For the mixed version, the performance improves from 718 to 939 TFLOPS. According to our HPC AI Roofline model shown in Fig. 9b, we find that there is a performance bound shift when the system scale changes from 32 to 64 GPUs. Specifically, when the system scale is less or equal to 32 GPUs, Image Classification’s communication ceiling is dominated by NVLink’s bandwidth, and it is computation-bound. Hence, communication compression cannot improve the performance. However, when the system increases to 64 GPUs, the communication ceiling is dominated by Ethernet’s bandwidth, so it turns into communication-bound. This is why communication compression works. The highest performance of Image Classification that we achieve is 939 TFLOPS through both mixed precision optimization and communication compression, as shown in Fig. 12e.

8.4.2 EWA

For the FP32 precision implementation of EWA, the parallel efficiency is 0.50, 0.37, and 0.36 at the system scale of 16, 32, and 64 GPUs, respectively. According to the Roofline model shown in Fig. 9b, the bottleneck is always communication bandwidth. Therefore, communication compression achieves good results. When communication compression is used, the performance gain persists when the scale increases from 8 to 16, 32, and 64 GPUs, and the speedup is 1.2, 1.4, 1.6, and 1.5, respectively. The highest performance of EWA achieved through communication compression is 109 TFLOPS.
8.4.3 Why EWA and Image Classification Have Different Parallel Efficiencies?

For EWA and Image Classification, we found their different parallel efficiencies are due to distinct communication bandwidth consumption. As shown in Fig. 13, we measure the communication bandwidth consumption of the FP32 precision implementations of EWA and Image Classification. EWA consumes much higher communication bandwidth than that of Image Classification. In the contrast, the performance of Image Classification largely depend on the computation efficiency especially when the scale is less than and equal to 32 GPUs. In conclusion, 10 Gb/s Ethernet can not satisfy the communication requirement of EWA, and hence results in poor parallel efficiency.

8.4.4 The VFLOPS Ranking of HPC AI Systems Using Image Classification

The metric of VFLOPS emphasizes both the performance and quality. Fig. 14 shows the rankings of different scale HPC AI systems with mixed-precision or FP32 implementations. The highest performance is 642 TVFLOPS, achieving through the mixed optimization at the scale of 64 GPUs. Meanwhile, another auxiliary metric–time-to-quality is also reported. Generally, our metric is simple and visual.

Figure 13: The distinctive communication bandwidth consumption of the FP32 implementations of EWA and Image Classification.

Figure 14: The VFLOPS Rankings of HPC AI Systems Using Image Classification.
8.5 The Case Study of Using HPC-AI Roofline Models

This section presents a case study on how to use our proposed HPC AI Roofline models to identify the bottleneck and guide optimizations.

8.5.1 Bottleneck Identification

We use the proposed roofline models to the 16-GPU HPC AI system. The theoretical peak number is calculated according to the hardware configurations shown in Table 9. We use the roofline model to identify potential bottlenecks of EWA and Image Classification.

From Fig. 15, we have the following observations. EWA is bounded by the communication bandwidth as it falls in the slanted part of the roof, while Image Classification is bounded by the computation as it falls in the flat part.

![Figure 15: The roofline model at the system scale of 16 GPUs. The blue point represents EWA, and the red point represents Image Classification.](image)

8.5.2 Optimizations

We adopt two optimization strategies: communication compression and mixed precision optimization.

**Communication compression.** In order to optimize the communication, we perform communication compression, which encodes and compresses the tensor precision into FP16 for communication and then decodes into FP32 for computation. This optimization halves the amount of communication for each training step, which is equivalent to doubling the communication bandwidth. As the amount of computation remains the same, the COI of EWA and Image Classification also doubles. As shown in Fig. 15, our results show that the performance of EWA increases from 25.99 to 36.97 TFLOPS after communication compression. On the other hand, the performance of Image Classification is not improved because it is computation bound. Its COI indeed increases.

**Mixed precision training.** In order to improve the performance of Image Classification, we adopt the mixed precision optimization, which makes use of Tensor Core to perform arithmetic calculation in an FP16 format, achieving higher amount of computation operations per second. As shown in Fig. 15, the rightest red point represents using the mixed precision training. It brings about 2.16x speedup. Moreover, the COI is also improved. This is because that the mixed precision training requires lower memory...
footprint, so we double the batchsize, and the larger batchsize leads to higher COI (higher amount of computation per step). In the near future, we will try mixed precision optimization for EWA, too.

9 Related Work

We summarize the related work in a chronological order (according to the publication dates of the referred papers or publicly available technique reports) from the perspectives of HPC benchmarking, AI benchmarking, and HPC AI benchmarking.

9.1 HPC Benchmarking

HPL (1994) [71] is the famous HPC benchmark for the Top500 [13] ranking. HPL is short for High Performance Linpack, which is designed to solve dense linear equations. For the TOP500 ranking, users are allowed to optimize MPI [61] and the BLAS [72] library to achieve the best performance. Since solving the Linpack problem is very regular, the HPC system can achieve very high performance. So, the performance of HPL can be described as the upper bound performance of the target HPC system. HPL is open source and publicly available from https://www.netlib.org/benchmark/hpl/.

NPB (1994) [73] is the NAS Parallel Benchmark suite, whose workloads are derived from the computational fluid dynamics (CFD) applications. CFD is a typical traditional HPC application. Based on the pencil-and-paper specification, NPB 1.0 consists of five kernels and three pseudo-applications, and the lastest NPB 3.4.1 includes 12 workloads. NPB is open source and publicly available from https://www.nas.nasa.gov/publications/npb.html.

HPCC (2005) [74] is an HPC Challenge benchmark suite, which includes seven different workloads. HPCC covers the spectrum of spatial locality and temporal locality of the HPC workloads. So, the HPCC benchmarks are designed for measuring a range of memory access patterns of the HPC system. HPCC is open source and publicly available from https://icl.utk.edu/hpcc/.

Graph500 (2010) [75] is designed for the data-intensive supercomputer applications. The workloads of Graph500 are the search and shortest-path programs of the weighted undirected graph. The Graph500 workloads exhibit very low spatial and temporal locality. Its metric is not the FLOPS but the TEPS (traversed edges per second). Graph500 is open source and publicly available from https://graph500.org/.

HPCG (2013) [76] is another benchmark for the Top500 ranking. HPCG means High Performance Conjugate Gradients (HPCG). Computational and data access patterns of HPCG are more close to the real HPC applications. As a kernel workload extracted from the traditional HPC workloads, the HPCG benchmark is intended as a complement to the High Performance LINPACK (HPL) benchmark, and the FLOPS of HPCG is far lower than that of HPL on the same platform. HPCG is open source and publicly available from https://github.com/hpcg-benchmark/hpcg.

9.2 AI Benchmarking

BenchNN (2012) [77] uses neural networks algorithms to re-implement the well-known PARSEC benchmark [35]. Their main propose is to illustrate the potential application scope of neural networks algorithms. The models adopted in BenchNN are simple shallow neural networks such as multi-layer perceptron, and thus they cannot reflect the state of the art. BenchNN is not open source so far.

DeepBench (2016) [78] is a micro benchmark suite that aims to benchmark basic operations in deep neural networks such as convolution and dense matrices multiply. The methodology of DeepBench is to reflect the characteristics of these operations by using different input sizes. Since only operator level is concerned, DeepBench cannot provide full-model level evaluation. DeepBench is open source and publicly available from https://github.com/baidu-research/DeepBench.

Both Fathom (2016) [79] and TBD (2018) [80] consists of representative AI workloads, covering a broad range of application domains. Their evaluation only focus on throughput while ignoring model
quality. Fathom is open source and publicly available from https://github.com/rdadolf/fathom. TBD is open source and publicly available from https://github.com/tbd-ai/tbd-suite.

DawnBench (2017) [81] aims to end-to-end deep learning benchmarking as it firstly proposes time-to-accuracy as the main metric, which requires to train a model to the state-of-the-art accuracy. It has two workloads including image classification and question answering. The limitation of DawnBench is ignoring the equivalent benchmarking rules. DawnBench is open source and publicly available from https://github.com/stanford-futuredata/dawn-bench-entries.

The BenchCouncil AI benchmark suites (2018) present a series of AI benchmarking work, including AI Bench [10, 11, 14, 15] for datacenter AI benchmarking, AloTBench [82] for mobile and embedded device intelligence benchmarking, Edge AI Bench [83] for edge computing benchmarking, and the previous version of HPC AI500 [45]. The BenchCouncil AI benchmarks are by far the most comprehensive AI benchmark suites covering datacenter, IoT, edge, and HPC. For example, AI Bench adopts a scenario-distilling benchmarking methodology for the first time, which considers scenario benchmarks, component and micro benchmarks as three indispensable parts of a benchmark suite. This methodology bridges a huge gap from real-world application deployments to simulator-based architecture research, and balances the subtly different requirements of earlier-stage benchmarking (portability and affordability for new architectures) and later-stage benchmarking (representativeness and comprehensiveness) [11]. The BenchCouncil AI benchmark suites are open source and publicly available from http://www.benchcouncil.org/benchmarks.html.

BenchIP (2018) [84] focuses on benchmarking intelligent processors. It contains two sets of benchmarks: micro-benchmarks and macro-benchmarks. Micro-benchmarks consists of single-layer networks that are used to system optimizations. Macro-benchmarks consists of various neural networks that are used to offer realistic benchmarking. BenchIP also ignores the equivalent benchmarking rules. In addition, it only focuses on throughput. BenchIP is not open source so far.

MLPerf (2019) [9] includes seven benchmarks for training and five benchmarks for inference. The MLPerf training benchmark proposes a series of benchmarking rules to eliminate the side effect of the stochastic nature of AI. Nevertheless, The MLPerf rules can not be used to assure the equivalency, repeatability, and replicability of HPC AI benchmarking. It lacks the specific parallelism and communication rules. MLPerf is open source and publicly available from https://github.com/mlperf.

9.3 HPC AI Benchmarking

HPC AI500 (V 1.0) (2018) [45] is the first HPC AI benchmarks based on the real-world scientific dataset, covering three representative HPC AI applications, namely high energy physics, cosmology, and extreme weather analytics. The HPC AI500 (V 1.0) is open source and publicly available from http://www.benchcouncil.org/benchhub/hpc-ai500-benchmark.

The HPL-AI benchmark (2019) [17] is designed for 32-bit and even lower floating-point precision AI computing. Using the solver formulation of the decades-old HPL framework of benchmarking, HPL-AI strives to unite traditional HPC and state-of-art AI. HPL-AI algorithm is a combination of low-precision (state-of-art AI precision) LU factorization and iterative refinement performed afterwards to bring the solution back to 64-bit accuracy (traditional HPC precision). However, the LU factorization operation is irrelevant to most of AI workloads. As a micro-benchmark, HPL-AI benchmark is more suitable for evaluating the upper bound performance of the HPC AI system. The HPL-AI benchmark is open source and publicly available from https://icl.bitbucket.io/hpl-ai/.

Deep500 (2019) [85] is a reproducible customized benchmarking infrastructure for high-performance deep learning. It has four levels of abstraction to provide a full-stack evaluation. However, its reference implementation uses commercial open source data sets and simple deep learning models, hence cannot reflect real-world HPC AI workloads. Moreover, it fails to propose rules to assure the equivalency, repeatability, and replicability of HPC AI benchmarking. Deep500 is open source and publicly available from https://github.com/deep500/deep500.

AAH (2020) [86] uses AutoML [87] to benchmark HPC AI systems. AutoML is highly compute-intensive and extensible, which fits the requirement of benchmarking HPC systems. However, as a
complicated AI workload, AutoML involves many hyper-parameters, which usually makes it hard to evaluate [40]. Moreover, the variance of its essential workload—Neural Architecture Search is also high as 6.15%, according to the evaluation in [10].

9.4 ImageNet/ResNet50 Training Optimization

Some specific AI workloads also play an important role in evaluating the HPC AI system. ImageNet/Resnet50 is a well-known showcase for optimizing HPC AI systems, motivating a series of research on learning rate scheduling algorithms and efficient communication strategies [19, 23, 24, 26, 27, 29, 32].

The researchers of Facebook (2017) [19] formally propose linear scaling rule and warmup schema for the first time and summarized several pitfalls in large scale deep learning. They finish the training in 60 minutes with a top1 accuracy of 76.3%.

The researchers of Berkeley (2017) [26] firstly propose LARS (Layer-wise Adaptive Rate Scaling), which is a novel learning rate policy. By utilizing this policy, they successfully scale the batch size of ResNet50 to 32K and reduce the training time to 20 minutes.

Preferred Networks (2017) [27], IBM (2017) [23], Tencent (2018) [29], Sony (2018) [28], Google (2018) [30], and Fujitsu (2019) [32] all focus on high efficient communication strategies (scale to larger HPC systems) and other system-level optimizations (e.g. mixed precision training). Their learning rate policy or other algorithm-level optimizations follow the work from Facebook [19] and Berkeley [26]. These work have reduced the training times from hours to minutes. So far, the fastest training time is 74 seconds, which is from Fujitsu (2019) [32].

10 Conclusion

This paper proposes a comprehensive HPC AI benchmarking methodology that achieves the goal of being equivalent, relevant, representative, affordable, and repeatable. Following this methodology, we present open-source benchmarks, and Roofline performance model to benchmarking and optimizing the systems. We propose two innovative metrics: Valid FLOPS, and valid FLOPS per watt to rank the performance and energy-efficiency of HPC AI systems.

The evaluations show our methodology, benchmarks, performance models, and metrics can measure, optimize, and rank the HPC AI systems in a scalable, simple, and affordable way. The specification, source code, and benchmarking data are publicly available from [http://www.benchcouncil.org/benchhub/hpc-ai500-benchmark](http://www.benchcouncil.org/benchhub/hpc-ai500-benchmark).

11 Acknowledgments

We thank the PengCheng Laboratory for hardware support. We also thank Shaomeng Cao, Xuhui Shao, Yongheng Liu, Changsong Liu, and Jingfei Qiu for technical support in using those systems.
References

[1] A. Krizhevsky, I. Sutskever, and G. E. Hinton, “Imagenet classification with deep convolutional neural networks,” in Advances in neural information processing systems, pp. 1097–1105, 2012.

[2] J. Deng, W. Dong, R. Socher, L.-J. Li, K. Li, and L. Fei-Fei, “Imagenet: A large-scale hierarchical image database,” in 2009 IEEE conference on computer vision and pattern recognition, pp. 248–255, Ieee, 2009.

[3] https://www.oreilly.com/ideas/a-look-at-deep-learning-for-science.

[4] S. Ravanbakhsh, J. B. Oliva, S. Fromentceau, L. Price, S. Ho, J. G. Schneider, and B. Póczos, “Estimating cosmological parameters from the dark matter distribution,” in ICML, pp. 2407–2416, 2016.

[5] Y. Liu, E. Racah, J. Correa, A. Khosrowshahi, D. Lavers, K. Kunkel, M. Wehner, W. Collins, et al., “Application of deep convolutional neural networks for detecting extreme weather in climate datasets,” arXiv preprint [arXiv:1605.01156], 2016.

[6] A. Mathuriya, D. Bard, P. Mendi gras, L. Meadows, J. Arnemann, L. Shao, S. He, T. Kärnä, D. Moise, S. J. Pennycook, et al., “Cosmoflow: Using deep learning to learn the universe at scale,” in SC18: International Conference for High Performance Computing, Networking, Storage and Analysis, pp. 819–829, IEEE, 2018.

[7] T. Kurth, S. Treichler, J. Romero, M. Mudigonda, N. Luehr, E. Phillips, A. Mahesh, M. Matheson, J. Deslippe, M. Fatica, et al., “Exascale deep learning for climate analytics,” in SC18: International Conference for High Performance Computing, Networking, Storage and Analysis, pp. 649–660, IEEE, 2018.

[8] J. L. Hennessy and D. A. Patterson, Computer architecture: a quantitative approach. Elsevier, 2011.

[9] P. Mattson, C. Cheng, C. Coleman, G. Diamos, P. Micikevicius, D. Patterson, H. Tang, G.-Y. Wei, P. Bailis, V. Bittorf, et al., “Mlperf training benchmark,” arXiv preprint [arXiv:1910.01500], 2019.

[10] F. Tang, W. Gao, J. Zhan, C. Lan, X. Wen, L. Wang, C. Luo, J. Dai, Z. Cao, X. Xiong, et al., “Aibench: An industry standard ai benchmark suite from internet services,” arXiv preprint [arXiv:2004.14690], 2020.

[11] W. Gao, F. Tang, J. Zhan, X. Wen, L. Wang, Z. Cao, C. Lan, C. Luo, and Z. Jiang, “Aibench: Scenario-distilling ai benchmarking,” arXiv preprint [arXiv:2005.03459], 2020.

[12] J. Gray, “Database and transaction processing performance handbook.” 1993.

[13] J. J. Dongarra, H. W. Meuer, E. Strohmaier, et al., “Top500 supercomputer sites,” Supercomputer, vol. 13, pp. 89–111, 1997.

[14] W. Gao, C. Luo, L. Wang, X. Xiong, J. Chen, T. Hao, Z. Jiang, F. Fan, M. Du, Y. Huang, et al., “Aibench: towards scalable and comprehensive datacenter ai benchmarking,” in International Symposium on Benchmarking, Measuring and Optimization, pp. 3–9, Springer, 2018.

[15] W. Gao, F. Tang, L. Wang, J. Zhan, C. Lan, C. Luo, Y. Huang, C. Zheng, J. Dai, Z. Cao, et al., “Aibench: an industry standard internet service ai benchmark suite,” arXiv preprint [arXiv:1908.08998], 2019.

[16] J. Zhan, L. Wang, W. Gao, and R. Ren, “Benchcouncil’s view on benchmarking ai and other emerging workloads,” arXiv preprint [arXiv:1912.00572], 2019.

[17] https://icl.bitbucket.io/hpl-ai/
[18] P. Micikevicius, S. Narang, J. Alben, G. Diamos, E. Elsen, D. Garcia, B. Ginsburg, M. Houston, O. Kuchaiev, G. Venkatesh, et al., “Mixed precision training,” arXiv preprint arXiv:1710.03740, 2017.

[19] P. Goyal, P. Dollár, R. Girshick, P. Noordhuis, L. Wesolowski, A. Kyrola, A. Tulloch, Y. Jia, and K. He, “Accurate, large minibatch sgd: Training imagenet in 1 hour,” arXiv preprint arXiv:1706.02677, 2017.

[20] A. Krizhevsky, “One weird trick for parallelizing convolutional neural networks,” arXiv preprint arXiv:1404.5997, 2014.

[21] V. Codreanu, D. Podareanu, and V. Saletore, “Scale out for large minibatch sgd: Residual network training on imagenet-lk with improved accuracy and reduced time to train,” arXiv preprint arXiv:1711.04291, 2017.

[22] S. Sridharan, K. Vaidyanathan, D. Kalamkar, D. Das, M. E. Smorkalov, M. Shiryaev, D. Madhigere, N. Mellemupudi, S. Avancha, B. Kaul, et al., “On scale-out deep learning training for cloud and HPC,” arXiv preprint arXiv:1801.08030, 2018.

[23] M. Cho, U. Finkler, S. Kumar, D. Kung, V. Saxena, and D. Sreedhar, “Powerai ddl,” arXiv preprint arXiv:1708.02188, 2017.

[24] Y. You, Z. Zhang, C.-J. Hsieh, J. Demmel, and K. Keutzer, “Imagenet training in minutes,” in Proceedings of the 47th International Conference on Parallel Processing, ICPP 2018, (New York, NY, USA), Association for Computing Machinery, 2018.

[25] https://www.intel.cn/content/www/cn/zh/high-performance-computing/ai-hpc-is-happening-now-report.html

[26] Y. You, Z. Zhang, J. Demmel, K. Keutzer, and C.-J. Hsieh, “Imagenet training in 24 minutes,” arXiv preprint arXiv:1709.05017, 2017.

[27] T. Akiba, S. Suzuki, and K. Fukuda, “Extremely large minibatch sgd: Training resnet-50 on imagenet in 15 minutes,” arXiv preprint arXiv:1711.04325, 2017.

[28] Y. Tanaka and Y. Kageyama, “Imagenet/resnet-50 training in 224 seconds,”

[29] X. Jia, S. Song, W. He, Y. Wang, H. Rong, F. Zhou, L. Xie, Z. Guo, Y. Yang, L. Yu, et al., “Highly scalable deep learning training system with mixed-precision: Training imagenet in four minutes,” arXiv preprint arXiv:1807.11205, 2018.

[30] C. Ying, S. Kumar, D. Chen, T. Wang, and Y. Cheng, “Image classification at supercomputer scale,” arXiv preprint arXiv:1811.06992, 2018.

[31] https://cloud.google.com/tpu/docs/bfloat16

[32] M. Yamazaki, A. Kasagi, A. Tabuchi, T. Honda, M. Miwa, N. Fukumoto, T. Tabaru, A. Ike, and K. Nakashima, “Yet another accelerated sgd: Resnet-50 training on imagenet in 74.7 seconds,” arXiv preprint arXiv:1903.12650, 2019.

[33] C. Szegedy, V. Vanhoucke, S. Ioffe, J. Shlens, and Z. Wojna, “Rethinking the inception architecture for computer vision,” in Proceedings of the IEEE conference on computer vision and pattern recognition, pp. 2818–2826, 2016.

[34] https://www.spec.org/cpu2017/
[35] C. Bienia, S. Kumar, J. P. Singh, and K. Li, “The parsec benchmark suite: Characterization and architectural implications,” in Proceedings of the 17th international conference on Parallel architectures and compilation techniques, pp. 72–81, 2008.

[36] http://www.tpc.org/tpcds/

[37] J. Gray, “The benchmark handbook for database and transaction systems,” Morgan Kaufmann, San Mateo, 1993.

[38] J. Bartlett and C. Frost, “Reliability, repeatability and reproducibility: analysis of measurement errors in continuous variables,” Ultrasound in Obstetrics and Gynecology: The Official Journal of the International Society of Ultrasound in Obstetrics and Gynecology, vol. 31, no. 4, pp. 466–475, 2008.

[39] https://www.acm.org/publications/policies/artifact-review-badging

[40] A. Yang, P. M. Esperança, and F. M. Carlucci, “Nas evaluation is frustratingly hard,” arXiv preprint arXiv:1912.12522, 2019.

[41] M. Abadi, P. Barham, J. Chen, Z. Chen, A. Davis, J. Dean, M. Devin, S. Ghemawat, G. Irving, M. Isard, et al., “Tensorflow: A system for large-scale machine learning,” in 12th {USENIX} symposium on operating systems design and implementation ({OSDI} 16), pp. 265–283, 2016.

[42] A. Paszke, S. Gross, F. Massa, A. Lerer, J. Bradbury, G. Chanan, T. Killeen, Z. Lin, N. Gimelshein, L. Antiga, et al., “Pytorch: An imperative style, high-performance deep learning library,” in Advances in neural information processing systems, pp. 8026–8037, 2019.

[43] C. Luo, X. He, J. Zhan, L. Wang, W. Gao, and J. Dai, “Comparison and benchmarking of ai models and frameworks on mobile devices,” arXiv preprint arXiv:2005.05085, 2020.

[44] W. Bhimji, S. A. Farrell, T. Kurth, M. Paganini, E. Racah, et al., “Deep neural networks for physics analysis on low-level whole-detector data at the lhc,” in Journal of Physics: Conference Series, vol. 1085, p. 042034, IOP Publishing, 2018.

[45] Z. Jiang, W. Gao, L. Wang, X. Xiong, Y. Zhang, X. Wen, C. Luo, H. Ye, X. Lu, Y. Zhang, et al., “Hpc ai500: a benchmark suite for hpc ai systems,” in International Symposium on Benchmarking, Measuring and Optimization, pp. 10–22, Springer, 2018.

[46] https://scikit-learn.org/stable/modules/generated/sklearn.manifold.TSNE.html

[47] C. Drummond, “Replicability is not reproducibility: nor is it good science,” 2009.

[48] H. E. Plessner, “Reproducibility vs. replicability: a brief history of a confused terminology,” Frontiers in neuroinformatics, vol. 11, p. 76, 2018.

[49] T. Kurth, J. Zhang, N. Satish, E. Racah, I. Mitliagkas, M. M. A. Patwary, T. Malas, N. Sundaram, W. Bhimji, M. Smorkalov, et al., “Deep learning at 15pf: supervised and semi-supervised classification for scientific data,” in Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, pp. 1–11, 2017.

[50] E. Racah, C. Beckham, T. Maharaj, S. E. Kahou, M. Prabhat, and C. Pal, “Extremeweather: A large-scale climate dataset for semi-supervised detection, localization, and understanding of extreme weather events,” in Advances in Neural Information Processing Systems, pp. 3402–3413, 2017.

[51] S. Ren, K. He, R. Girshick, and J. Sun, “Faster r-cnn: Towards real-time object detection with region proposal networks,” in Advances in neural information processing systems, pp. 91–99, 2015.
[52] R. Girshick, “Fast r-cnn,” in Proceedings of the IEEE international conference on computer vision, pp. 1440–1448, 2015.

[53] R. Girshick, J. Donahue, T. Darrell, and J. Malik, “Rich feature hierarchies for accurate object detection and semantic segmentation,” in Proceedings of the IEEE conference on computer vision and pattern recognition, pp. 580–587, 2014.

[54] K. He, X. Zhang, S. Ren, and J. Sun, “Deep residual learning for image recognition,” in Proceedings of the IEEE conference on computer vision and pattern recognition, pp. 770–778, 2016.

[55] https://https://www.jlab.org/indico/event/247/session/8/contribution/30/material.slides/0.pdf.

[56] A. Sergeev and M. Del Balso, “Horovod: fast and easy distributed deep learning in tensorflow,” arXiv preprint arXiv:1802.05799, 2018.

[57] A. Mathuriya, T. Kurth, V. Rane, M. Mustafa, L. Shao, D. Bard, V. W. Lee, et al., “Scaling grpc tensorflow on 512 nodes of cori supercomputer,” arXiv preprint arXiv:1712.09388, 2017.

[58] http://research.baidu.com/bringing-hpc-techniques-deep-learning.

[59] S. L. Smith, P.-J. Kindermans, C. Ying, and Q. V. Le, “Don’t decay the learning rate, increase the batch size,” arXiv preprint arXiv:1711.00489, 2017.

[60] Y. You, J. Li, S. Reddi, J. Hseu, S. Kumar, S. Bhojanapalli, X. Song, J. Demmel, K. Keutzer, and C.-J. Hsieh, “Large batch optimization for deep learning: Training bert in 76 minutes,” arXiv preprint arXiv:1904.00962, 2019.

[61] https://www.open-mpi.org/

[62] https://developer.nvidia.com/nccl.

[63] A. Hannun, C. Case, J. Casper, B. Catanzaro, G. Diamos, E. Elsen, R. Prenger, S. Satheesh, S. Sengupta, A. Coates, et al., “Deep speech: Scaling up end-to-end speech recognition,” arXiv preprint arXiv:1412.5567, 2014.

[64] S. Ioffe and C. Szegedy, “Batch normalization: Accelerating deep network training by reducing internal covariate shift,” arXiv preprint arXiv:1502.03167, 2015.

[65] S. Williams, A. Waterman, and D. Patterson, “Roofline: an insightful visual performance model for multicore architectures,” Communications of the ACM, vol. 52, no. 4, pp. 65–76, 2009.

[66] https://docs.nvidia.com/cuda/profiler-users-guide/index.html.

[67] W. Gao, J. Zhan, L. Wang, C. Luo, D. Zheng, X. Wen, R. Ren, C. Zheng, X. He, H. Ye, et al., “Big-databench: A scalable and unified big data and ai benchmark suite,” arXiv preprint arXiv:1802.08234, 2018.

[68] H. Zhu, M. Akrout, B. Zheng, A. Pelegris, A. Phanishayee, B. Schroeder, and G. Pekhimenko, “Tbd: Benchmarking and analyzing deep neural network training,” arXiv preprint arXiv:1803.06905, 2018.

[69] http://https://horovod.readthedocs.io/en/latest/timeline.html.

[70] https://www.nvidia.com/en-us/data-center/v100/.

[71] J. J. Dongarra, P. Luszczek, and A. Petitet, “The linpack benchmark: past, present and future,” Concurrency and Computation: practice and experience, vol. 15, no. 9, pp. 803–820, 2003.

[72] http://www.netlib.org/blas/.
L. Humphrey, B. Guilfoos, H. B. Smith, A. Warnock, J. Unpingco, B. H. Elton, and A. Chalker, “Evaluating parallel extensions to high level languages using the hpc challenge benchmarks,” pp. 410–415, 2009.

K. Ueno and T. Suzumura, “Highly scalable graph search for the graph500 benchmark,” pp. 149–160, 2012.

J. Dongarra, M. A. Heroux, and P. Luszczek, “High-performance conjugate-gradient benchmark: A new metric for ranking high-performance computing systems,” The International Journal of High Performance Computing Applications, vol. 30, no. 1, pp. 3–10, 2016.

T. Chen, Y. Chen, M. Duranton, Q. Guo, A. Hashmi, M. Lipasti, A. Nere, S. Qiu, M. Sebag, and O. Temam, “Benchmn: On the broad potential application scope of hardware neural network accelerators,” in 2012 IEEE International Symposium on Workload Characterization (IISWC), pp. 36–45, IEEE, 2012.

R. Adolf, S. Rama, B. Reagen, G.-Y. Wei, and D. Brooks, “Fathom: Reference workloads for modern deep learning methods,” in 2016 IEEE International Symposium on Workload Characterization (IISWC), pp. 1–10, IEEE, 2016.

H. Zhu, M. Akroot, B. Zheng, A. Pelegris, A. Jayarajan, A. Phanishayee, B. Schroeder, and G. Pekhimenko, “Benchmarking and analyzing deep neural network training,” in 2018 IEEE International Symposium on Workload Characterization (IISWC), pp. 88–100, IEEE, 2018.

C. Coleman, D. Narayanan, D. Kang, T. Zhao, J. Zhang, L. Nardi, P. Bailis, K. Olukotun, C. Ré, and M. Zaharia, “Dawnbench: An end-to-end deep learning benchmark and competition,” Training, vol. 100, no. 101, p. 102, 2017.

C. Luo, F. Zhang, C. Huang, X. Xiong, J. Chen, L. Wang, W. Gao, H. Ye, T. Wu, R. Zhou, et al., “Aiot bench: towards comprehensive benchmarking mobile and embedded device intelligence,” in International Symposium on Benchmarking, Measuring and Optimization, pp. 31–35, Springer, 2018.

T. Hao, Y. Huang, X. Wen, W. Gao, F. Zhang, C. Zheng, L. Wang, H. Ye, K. Hwang, Z. Ren, et al., “Edge aibench: towards comprehensive end-to-end edge computing benchmarking,” in International Symposium on Benchmarking, Measuring and Optimization, pp. 23–30, Springer, 2018.

J.-H. Tao, Z.-D. Du, Q. Guo, H.-Y. Lan, L. Zhang, S.-Y. Zhou, L.-J. Xu, C. Liu, H.-F. Liu, S. Tang, et al., “Bench ip: Benchmarking intelligence processors,” Journal of Computer Science and Technology, vol. 33, no. 1, pp. 1–23, 2018.

T. Ben-Nun, M. Besta, S. Huber, A. N. Ziogas, D. Peter, and T. Hoefler, “A modular benchmarking infrastructure for high-performance and reproducible deep learning,” in 2019 IEEE International Parallel and Distributed Processing Symposium (IPDPS), pp. 66–77, IEEE, 2019.

Z. Ren, Y. Liu, T. Shi, L. Xie, Y. Zhou, H. Chen, H. Fu, Y. Ouyang, J. Zhai, Y. Zhang, Y. Zhang, and W. Chen, “Aah: Automated machine learning as an ai-hpc benchmark,” Technical Report of Pengcheng Lab and Tsinghua University, 2020.

H. Jin, Q. Song, and X. Hu, “Auto-keras: An efficient neural architecture search system,” in Proceedings of the 25th ACM SIGKDD International Conference on Knowledge Discovery & Data Mining, pp. 1946–1956, 2019.