Abstract

To improve the accuracy and stability of piezoresistive sensors based on polysilicon nanosized thin films (PNTFs), 80nm-thick PNTFs were deposited on Si substrates by LPCVD at different temperatures and fabricated into cantilever beams. The electrical trimming characteristics and dependences of gauge factor, TCR and TCGF on resistor trim were measured. Based on interstitial-vacancy model, the electrical trimming is due to the mobility increase caused by current-induced recrystallization of grain boundaries (GBs). The changes in GF, TCR and TCGF with resistor trim are due to the GB state variation (including scattering center, GB width, tunneling current, localized and extended state conductions).

Keywords: Polysilicon; Current-induced recrystallization; Piezoresistive; Electrical trimming; Interstitial-vacancy pair; Deposition temperature

1. Introduction

As a piezoresistive material, polysilicon has many advantages over single crystal silicon, such as low cost, facile processing and no need for p-n junction isolation. Our previous research work [1, 2] indicates that polysilicon nanosized thin films (PNTFs, ~80nm in thickness) exhibit larger gauge factor (GF $\geq 34$) and better temperature stability than polysilicon thick films (> 200nm in thickness, GF is 20~25) at high doping level. It makes PNTFs potential for the fabrication and application of piezoresistive sensors with low temperature drift and high sensitivity.

For sensors with Wheatstone bridge structure, the resistance matching is a significant ingredient determining the zero-point output, measurement accuracy and temperature stability. Thus, it is necessary to trim the resistance mismatch caused by fabrication errors. Usually, the trimming methods include laser trimming and Zener sapping. However, the former could introduce stress due to local heating and be affected by the heat treatment during packaging, while the latter could waste chip area and increase fabrication cost. The electrical trimming (ET) was

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discovered in polysilicon [3] and then testified to exist in other polycrystalline materials [4]. This method overcomes the drawbacks in above two methods and could be applied in resistor trimming. In this paper, the ET phenomenon of PNTFs with different deposition temperatures and its influence on piezoresistive properties were investigated.

2. Experimental details

2.1. Sample preparation and characterization

The 80nm-thick PNTFs were deposited by LPCVD on 500μm-thick Si (111) substrates coated with SiO2 layers at 580~670°C. The samples of 580°C and 600°C were pre-annealed at 950°C for 30min to reduce amorphous contents. By ion-implantation and annealing at 1080°C for 30min, all the samples were doped with boron and the doping concentration is 2×10²⁰cm⁻³. In Fig. 1, the SEM images show that the grain size increases with elevating deposition temperature; the broad peaks (2θ=85~100°) in XRD patterns indicate that there are less amorphous contents in 620°C films than other samples. Based on photolithography and wet etching, the cantilever beam samples (26mm×4mm) with PNTF resistors were fabricated, as shown in Fig. 2(a).

2.2. Measurement of electrical trimming, piezoresistive and temperature properties

For electrical trimming test, a constant current was applied to PNTF resistors for 30s in every measurement and the current amplitude was incremental gradually. Then, the GF, temperature coefficients of resistance (TCR) and GF (TCGF) were measured with different resistor trim values utilizing the testing setup shown in Fig. 2. In all the experiments, the resistance values were measured by a Keithley 2000 digital multimeter.

Fig. 1. Characterization of PNTFs with different deposition temperatures. (a)-(d) SEM images; (e) XRD patterns.

Fig. 2. Testing setup for measuring gauge factor
3. Results and discussions

3.1. Electrical trimming properties and interstitial-vacancy model of grain boundary

In ET phenomenon, when the applied current surpasses a certain threshold, the resistance is reduced; the trimmed resistance is stable and fall off with the trimming current increasing. In order to explain this phenomenon, the grain boundaries (GBs) are modeled as the accumulation of interstitial-vacancy (IV) pairs. The resistance reduction is due to the recrystallization of IV pairs at GBs induced by Joule heat under large current density, and the current-induced recrystallization (CIRC) decreases the number of scattering centers and increases mobility and conductivity. Some electrical and ET parameters of PNTFs deposited at difference temperatures are provided in Table 1.

Table 1. Electrical and ET parameters of PNTFs deposited at different temperatures.

| Deposition temperature (°C) | Resistivity (Ω cm) | Sheet resistance (kΩ/□) | Trimming threshold current density (×10^5 A/cm²) |
|----------------------------|-------------------|--------------------------|-----------------------------------------------|
| 580 (pre-anneal at 950°C)  | 5.20×10⁻²         | 6.506                    | 0.45±0.1                                        |
| 600 (pre-anneal at 950°C)  | 2.59×10⁻²         | 3.233                    | 0.71±0.1                                        |
| 620                        | 2.81×10⁻²         | 3.510                    | 0.425±0.05                                 |
| 670                        | 4.90×10⁻³         | 0.608                    | 2.02±0.1                                        |

3.2. Influence of current-induced recrystallization (CIRC) on GF, TCR and TCGF

The dependences of changes in GFs on deposition temperature and resistor trim are provided in Fig. 3(a) and (b), respectively. Fig. 3(a) indicates that the GF variation in 620°C samples is much smaller than other samples in the low trim range. Moreover, in Fig. 3(b), the relative changes in GF (ΔGF/GF) of 620°C samples are in the range of ±0.5% for 0–14% resistor trim. For 580°C and 600°C samples with more amorphous contents and small grains, the CIRC decreases the GB width and increases tunneling current through GBs. It enhances the tunneling piezoresistive effect [2] and increases the GF. For 670°C samples with large grains, the further reduction of scattering centers at GBs decreases the proportion of GB resistivity in film resistivity, and the variation in GB width could be neglected compared to large grain size. It causes the falloff of ΔGF/GF with resistor trim in the high trim range.

The temperature characteristics of resistance of 620°C samples with different resistor trims and the relationship between TCR and resistor trim are shown in Fig. 4(a) and (b), respectively. In the low trim range, TCR increases with resistor trim. It is due to that CIRC decreases the proportion of GBs (with negative TCR) in films and the positive TCR of grain neutral regions is dominant (depending on lattice scattering). In the high trim range, the further IV pair combination makes the conducting mechanism of GBs transfer from the localized state conduction to extended state conduction. The strong negative TCR of extended state conductivity results in the reduction of TCR with resistor trim. The temperature characteristics of GF of 620°C samples with different resistor trims and the relationship between TCGF and resistor trim are shown in Fig. 5(a) and (b), respectively. Figure 5 indicates that TCGF is negative and its magnitude increases slightly with resistor trim.

Fig. 3. (a) Changes in GF before and after trimming; (b) ΔGF/GF vs. resistor trim with different deposition temperatures.
4. Conclusions

The electrical trimming based on CIRC and its influences on GF, TCR and TCGF of PNTF resistors were investigated here. By IV model of GBs, the ET phenomenon is explained as the mobility increase due to the IV pair combination induced by Joule heat. The changes in GF, TCR and TCGF with resistor trim depend on the variation of GB states (e.g. scattering center, GB width, tunneling current, localized and extended state conductions, etc.).

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