Si-based Ka-band SIW band-pass filter using wafer level manufacturing process

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Abstract In this letter, a SIW (substrate integrated waveguide) linear coupling band-pass filter working in Ka-band is presented, it is designed to be a part of a Ka-band receiver front end. Due to the super heterodyne structure of the receiver, the system contains lots of chips, therefore stacked packaging structure is used. Considering the heat dissipation efficiency, process accuracy and cost, novel wafer-level silicon manufacturing process is adopted to fabricate the SIW filter. The design of the filter employs the coupling coefficients extraction method. Finally, a fourth-order band-pass filter was designed, manufactured and tested. The measured results are in good agreement with the simulation results, verifying the practicability of the silicon-based SIW filter in RF front end microsystem.

Keywords: band-pass filters, coupling coefficients, substrate integrated waveguide, Si-based, system-in-package, wafer-level process

Classification: Microwave and millimeter-wave devices, circuits, and modules

1. Introduction

With the development of the mobile Internet, new services and applications are emerging one after another, which makes the data transmission rate and spectrum resources of the existing mobile communication network have been greatly challenged. In response to this explosive growth in communication traffic, the fifth-generation mobile communication network came into being [1, 2, 3]. The working band of the 5G network is divided into the FR1 frequency band below 6 GHz and the millimeter wave FR2 frequency band from 24.25 to 52.6 GHz. In the millimeter-wave frequency, Ka-band receives the most attention for high frequency band for 5G [4, 5, 6, 7], therefore, the Ka-band TX/RX front end and Ka-band band-pass filters have become a major focus of recent research. However, in Ka-band, the traditional microstrip filter often suffers from electromagnetic leakage due to its semi-open structure, which results in large insertion loss [8, 9, 10]. Due to the high quality factor and low loss at high frequency, as well as the advantage of easiness for planar integration, SIW (substrate integrated waveguide) filter has become a good choice for filter design in Ka-band.

The concept of substrate-integrated waveguide was first proposed by professor Wu Ke in 2003 [11]. The substrate integrated waveguide consists of a low-loss dielectric substrate, top and bottom metal planes and two rows of metalized through-holes through the substrate. Wu Ke and his team studied the connections of high-frequency transmission characteristics between substrate integrated waveguide and traditional rectangular waveguide [12, 13, 14, 15]. Based on their research results, researchers have designed and fabricated many millimeter wave components using SIW structure like filters [16, 17, 18, 19] or laminate ceramic [20, 21], silicon is rarely applied in the design of millimeter wave SIW filters, mainly because the leakage current of silicon materials at high frequency makes the insertion loss of filter increase. But the silicon-based process has its own advantages: mature, accurate, and more matching CTE (coefficient of thermal expansion) with chips. This makes the silicon-based process still a considerable choice when implementing SIW filters used in complex stacked RF front ends.

In this letter, a band-pass filter for Ka-band receiver is proposed. The receiver system architecture is shown in Figure 1, the whole system is constructed on silicon interposers for miniaturized heterogeneous integration. The requirements of the receiver system for the Ka-band filter are that the in-band insertion loss is within 4 dB, and the flatness in the passband is less than 1 dB. Being an important passive device in the receiver, the filter can be embedded in the RF microsystem through wafer-level Si-based manufacturing process, therefore reducing the extra insertion loss introduced by common interconnection. To demonstrate the practicality of silicon-based process in SIW filter design and fabrication, a Ka-band SIW band-pass filter was designed and manufactured, the through holes of the SIW structure were made using wafer-level TSV (Through Silicon Via) process. In the design phase, coupling coefficient extraction method was applied to determine the key dimensions of the filter. Finally, the filter was tested, the measured results are consistent with the simulation results and meet the designing goals, verifying the practicability of the Si-based process in the production of Ka-band SIW filters.
2. Design of the filter

The structure of the filter is shown in Fig. 2, it consists of four linearly coupled SIW resonators, center frequency is 29.8 GHz with a fractional bandwidth of 5%. GSG transmission line is used as feed-in/out structure. Using the rectangular waveguide design method in [29], the element parameters of a four-order Chebyshev low-pass prototype with 0.1 dB pass-band ripple are found to be:

- \( g_0 = 1 \),
- \( g_1 = 1.088 \),
- \( g_2 = 1.3061 \),
- \( g_3 = 1.7703 \),
- \( g_4 = 0.8180 \),
- \( g_5 = 1.3554 \).

Based on these element value and fractional bandwidth of the filter, the required values of coupling coefficient between SIW cavities and external quality factor can be calculated according to Eq. (1). The calculated coupling coefficients and external quality factors are:

- \( M_{12} = M_{34} = 0.0415 \),
- \( M_{23} = 0.0329 \),
- \( Q_{ei} = Q_{eo} = 22.176 \).

In order to determine the specific size of the filter, Ansys HFSS electromagnetic simulation software was used to extract these coupling coefficients and external quality factors from the simulation model. Due to the limitation of process capability, the TSV diameter is limited to 20um, this extremely small structure leads to time-consuming simulation cycle of the SIW filter model. For the purpose of shortening design time and speeding up the simulation cycle, during the simulation, equivalent rectangular waveguide model was constructed to replace the SIW structure. First, the eigen-solving mode of HFSS was used to determine the original size of rectangular resonant cavity when the resonant frequency of TE\(_{101}\) mode was 29.8 GHz, the field distribution of TE\(_{101}\) mode is shown in Fig. 3(a).

After determination of single cavity size, the dual-mode extraction method was adopted to extract the coupling coefficient when two resonant cavities use magnetic coupling openings [30], the simulation model with electric-field distribution is presented in Fig. 3(b). Using eigen-solving mode of Ansys HFSS, two adjacent mode resonant frequencies \( f_1 \) and \( f_2 \) were calculated, the coupling coefficients \( M \) can be then obtained based on Eq. (2). To acquire the original dimensions of magnetic coupling openings \((O_1 \text{ and } O_2)\), parameter sweep of opening width \( O \) was set up and simulated. According to the simulation results, the relationship graph of opening width and coupling coefficients was plotted and presented in Fig. 4. Based on Fig. 4 as well as the coupling coefficients obtained from Eq. (1), original opening width were determined.

After construction of single-port cavity simulation model in HFSS as shown in Fig. 5, a group of \( S_{11} \) curves corresponding to different feed-in depth \( d \) were simulated and obtained, the external quality factors were calculated based on Eq. (3), in which \( \omega_0 \) is the resonant frequency of the single port model, and \( \tau_{S_{11}}(\omega_0) \) is the group delay of \( S_{11} \) at the resonant frequency. Similar to coupling coefficient extraction, a graph of relationship between feed-in depth and external quality factor was plotted, based on the graph, the depth of the feed-in line was obtained.

Finally, the external quality factor of the resonant cavity feed-in line can be extracted based on the group delay of return loss. After constructing a single-port cavity simulation model, the \( S_{11} \) curves were simulated and obtained, the external quality factors were calculated based on Eq. (3), in which \( \omega_0 \) is the resonant frequency of the single port model, and \( \tau_{S_{11}}(\omega_0) \) is the group delay of \( S_{11} \) at the resonant frequency. Similar to coupling coefficient extraction, a graph of relationship between feed-in depth and external quality factor was plotted, based on the graph, the depth of the feed-in line was obtained.
After the design of equivalent rectangular waveguide filter was completed, dimensions of the actual SIW filter can be then determined according to Eq. (4). In Eq. (4), \(a\) is the substrate integrated waveguide width, \(d\) is the diameter of the through hole, \(p\) is the pitch between two adjacent through holes, and \(a_{\text{eff}}\) is the width of the equivalent rectangular waveguide [13].

With final adjustments to SIW filter model, the simulation results of both models were relatively close when the pitch between two adjacent TSVs was 40\(\mu\text{m}\), the unloaded quality factor of a single SIW resonator is 171.3. The final simulation model of the SIW filter and comparison between both simulated results are presented in Fig. 6.

\[
Q_e = \frac{\omega_0 S_{11}(\omega_0)}{4} \quad (3)
\]

\[
a_{\text{eff}} = a - \frac{d^2}{0.95p} \quad (4)
\]

3. Fabrication process of the filter

The SIW filter designed was fabricated on silicon substrate with dielectric permittivity \(\varepsilon_r = 11.9\), dielectric loss tangent \(\tan \sigma = 0.002\) and thickness \(h = 0.2\ \text{mm}\), using a 12-inch wafer-level silicon-based process. The overall process flow is shown in Fig. 7. The first step was TSV etching with a diameter of 20\(\mu\text{m}\) and depth of 200\(\mu\text{m}\). The second step was PECVD (Plasma Enhanced Chemical Vapor Deposition) of silicon dioxide on the front side of the silicon wafer and sidewalls of TSVs, the thickness of silicon dioxide is 1\(\mu\text{m}\), the third step was PECVD of barrier and seed layer on the side walls of TSVs, followed by electroplating copper in TSV, the next step was lithography of redistribution layer copper and polyimide passivation layer on the front side, the last step of front side process was UBM (under-ball metal) electroplating. After the front side process was over, the wafer was turned over and bonded with a carrier wafer, preparing for back side process. During back side process, the first step was wafer thinning, followed by chemical wet etching in order to open the other head of the TSV copper pillar. Then polyimide was deposited as the first passivation layer. After that, similar to front side process, back-side redistribution layer copper was electroplated followed by second-layer polyimide chemical vapor deposition. The final step was polyimide opening and LGA (Land Grid Array) pad electroplating. When all steps mentioned above were finished, the carrier wafer was removed and the filter wafer was cleaned and diced, the SIW filter wafer fabricated and single sample of SIW filter are presented in Fig. 8. The final dimensions of the SIW filter are listed in Table I.

![Fabricated silicon wafer of the SIW filter](image1)

![Comparison of a single SIW filter and a 1-yuan coin](image2)

| Table I: Final dimensions of the SIW filter. |
|--------------------------------------------|
| Cavity length1 (a1)                      | 2.32 mm |
| Cavity length2 (a2)                      | 2.12 mm |
| Filter width (b)                         | 2.015 mm |
| Opening1 (l1)                            | 630 \(\mu\text{m}\) |
| Opening2 (l2)                            | 625 \(\mu\text{m}\) |
| Opening3 (l3)                            | 575 \(\mu\text{m}\) |
| GSG feed-in line width (w)               | 100 \(\mu\text{m}\) |
| GSG feed-in line depth (d)               | 703 \(\mu\text{m}\) |
| GSG Signal-to-ground gap1 (g1)           | 71 \(\mu\text{m}\) |
| GSG Signal-to-ground gap2 (g2)           | 125 \(\mu\text{m}\) |
4. Simulated and Measured Results

Single sample of the proposed SIW filter was tested on a Keysight high-frequency GSG probe measurement platform, as shown in Fig. 9. After calibration of probes, S parameters of the fabricated SIW filter were measured. Fig. 10 shows the comparison between measured and simulated results of the SIW band-pass filter. It can be observed from Fig. 10 that measured results are consistent with the simulation results. The pass-band of the fabricated SIW filter is centered at 29.8 GHz with a fractional 3 dB bandwidth of 5%. Insertion loss at center frequency is 3.45 dB, mainly because of the leakage current and dissipation factor of the silicon substrate, loss at center frequency is 3.45 dB, mainly because of the leakage current and dissipation factor of the silicon substrate, the return loss in the pass-band is below −12 dB and out-of-band rejection at 26.8 GHz is better than 57 dB, all of which meet the requirements for the RF filter as part of a Ka-band rejection at 26.8 GHz is better than 57 dB, all of which meet the requirements for the RF filter as part of a Ka-band rejection at 26.8 GHz is better than 57 dB, all of which meet the requirements for the RF filter as part of a Ka-band rejection at 26.8 GHz is better than 57 dB, all of which meet the requirements for the RF filter as part of a Ka-band rejection at 26.8 GHz is better than 57 dB, all of which meet the requirements for the RF filter as part of a Ka-band rejection at 26.8 GHz is better than 57 dB. The slight discrepancy between the measured and simulated insertion loss in the pass-band may be due to the mismatch of silicon conductivity in simulation model and actual SIW filter.

Fig. 9 (a) Keysight high-frequency GSG probe measurement platform used in filter test, (b) SIW filter sample under test, (c) and (d) micrograph of high frequency probe during test.

Fig. 10 The comparison between the simulated and measured results.

5. Conclusion

In this letter, a SIW filter used in a silicon-based 3D stacked RF receiver microsystem is designed, fabricated and tested. The filter is fabricated using a novel 12-inch silicon wafer process, the design and manufacturing process have been listed in detail in this letter. The tested and simulated results of the filter are in good agreement, and the key performance indicators meet the requirements of the receiver system for RF band-pass filters. The proposed filter has the merits of small size, high selectivity, mass production and easiness for 3-D integration. Thus, the feasibility of silicon-based technology in the design of Ka-band SIW filters is verified.

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