A 51.3 TOPS/W, 134.4 GOPS In-memory Binary Image Filtering in 65nm CMOS

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Abstract—Neuromorphic vision sensors (NVS) can enable energy savings due to their event-driven that exploits the temporal redundancy in video streams from a stationary camera. However, noise-driven events lead to the false triggering of the object recognition processor. Image denoise operations require memory-intensive processing leading to a bottleneck in energy and latency. In this paper, we present in-memory filtering (IMF), a 6T-SRAM in-memory computing based image denoising for event-based binary image (EBBI) frame from an NVS. We propose a non-overlap median filter (NOMF) for image denoising. An in-memory computing framework enables hardware implementation of NOMF leveraging the inherent read disturb phenomenon of 6T-SRAM. To demonstrate the energy-saving and effectiveness of the algorithm, we fabricated the proposed architecture in a 65nm CMOS process. As compared to fully digital implementation, IMF enables > 70× energy savings and a > 3× improvement of processing time when tested with the video recordings from a DAVIS sensor and achieves a peak throughput of 134.4 GOPS. Furthermore, the peak energy efficiencies of the NOMF is 51.3 TOPS/W, comparable with state of the art in-memory processors. We also show that the accuracy of the images obtained by NOMF provide comparable accuracy in tracking and classification applications when compared with images obtained by conventional median filtering.

Index Terms—In-memory computing, neuromorphic vision sensors, median filter, image denoising, address event representation.

I. INTRODUCTION

The proliferation of sensors in the Internet of Things (IoT) combined with emergence of ultra low-power electronics and almost pervasive connectivity has marked the emergence of many new applications. Image-sensors producing video streams hold an unique position among all the sensors due to both the rich information carried in it as well as the requirement of extremely high network bandwidth and concomitant energy needed for its transmission [1]. Edge computing [2] offers an alternative by processing the information locally using advanced machine learning techniques like deep neural networks (DNN); however, most state of the art DNN models are memory and compute intensive requiring significant energy dissipation as well [3].

One option to reduce computations is to downsample the image—however, this leads to loss in accuracy. Another option for stationary cameras is to exploit the temporal redundancy in video streams, i.e. background information is not changing from frame to frame. Bio-inspired neuromorphic vision sensors (NVS) [4], [5] that detect change in temporal contrast at the pixel level are ideally suited for this purpose since the pixels generate events only on detecting changes [6]. However, in real scenarios, many spurious events are generated due to noise which requires the use of noise filtering or denoise operations [7], [8]. While event-driven filtering [7], [8] was proposed initially, hybrid frame-event approach [9] is more suited for IoT operations. Since the event generated in the NVS will not reset until it is readout, they propose to sample the sensor memory in a burst after a regular interval \( t_f \), to create an event-based binary image (EBBI) frame. It allows the processor to reduce energy consumption by duty cycling once the processing ends. This also simplifies the noise filtering to a median filter operation and frames without valid objects (with all pixel values equal to 0 due to absence of events) need not be processed by the object recognition DNN.

Fig. 1 shows the potential energy benefits from this approach. The classification energy of a DNN processor is assumed to be 1076.6nJ based on the average of numbers reported in recent works [10], [12] in the range of 730nJ to 1700nJ. Analyzing the frames from the traffic dataset in [13], we find \( \approx 51\% \) of frames to be empty (frames without a valid object). Using energy estimates from measurements of the designed \( 320 \times 240 \) memory read (0.916pJ/bit) and write energy (6pJ/bit) for a conventional digital implementation of median filter, we find that the average energy requirement reduces by only \( 32 - 39\% \) due to the high energy requirement of the median filter itself which in turn is largely due to memory access. In contrast, emerging in and near-memory computing framework eliminates the data transfer cost point-

| DNN | MF+DNN | MFRB+DNN | IMC+NOMF+DNN |
|-----|--------|----------|--------------|
| 0.68× | 0.61×  | 0.49×    |              |

Fig. 1. The energy required to run a DNN for object recognition on each frame can be reduced by not operating on empty frames which comprises \( \approx 51\% \) of all frames. Including a conventional median filter to denoise the images requires significant energy overhead while IMC based approximate median filter enables exploiting the temporal redundancy fully.
ing to potential for great improvement.

In near or in-memory computing (IMC), the processing is done either on the boundary [14] or inside the memory. It not only gets rid of the data movement but also enables highly parallel processing due to its simultaneous access to multiple cells [15]. In general, the SRAM-based realization of near or in-memory computing can be categorized as charge sharing [16], [17], current summation [18], [19], delay-based [20] and xor-based digital [21] implementation. While the majority of the works on IMC are focused on the classification of the objects, in this paper, we use SRAM-based IMC for efficient denoising of the event-based binary image (EBBI).

Fig. 1 shows that our approach allows full exploitation of the temporal redundancy in video data enabling average energy per frame to go down by ≈ 51% equivalent to the sparsity in input data.

In this paper, we propose a non-overlap median filter (NOMF) for image denoising. Even though the NOMF introduces approximation in computation [22], it: 1) reduces the number of computes, explained later in section III-F, and 2) enables hardware implementation of image denoising, leveraging inherent read disturb phenomenon of 6T-SRAM. Our significant contributions in this paper are as follows:

1) We propose a 6T-SRAM in-memory computing-based image denoising integrated circuit for event-based binary images leveraging read disturb of SRAM. This article is an extended version of [23], providing the characterization and measurement results of NOMF in four fabricated chips. The proposed NOMF enables ~114× energy savings compared to a digital counterpart when tested with the video recordings from a DAVIS sensor [24] and achieves a peak throughput of 0.58 frames/µs for 240 × 180 binary images.

2) We evaluate the performance of an overlap-based tracker as well as an object classifier (LeNet inspired Convolutional neural network) using images from the median filter and NOMF. The performance of the object classifier and overlap-based tracker for both images is comparable.

3) We characterize the unwanted bit flip scenario and discuss different design aspects to prevent it in detail.

4) Also, a near memory computing circuit is proposed for valid frame detection tracking the bit line voltages during the filtering operation.

We organize the remaining part of the paper as follows. In section II, we review the basics of a median filter and proposed non-overlapped median filter. We discuss the IMF processor architecture and present a 6T SRAM-based hardware implementation of the non-overlap median filter in section III. Section IV presents measurement results and performance evaluation and comparison of the proposed NOMF with the conventional median filter in the applications of object tracking and detection. In section V, we propose a near memory computing circuit for valid frame detection, followed by a conclusion in section VI.

II. IMAGE DENOISING

In this section, we will give a brief overview of a median filter and the proposed approach of noise filtering.

A. Median Filter

A median filter slides an $n \times n$ window over an input image and replaces the center pixel of the $n \times n$ output patch by the median value of the $n^2$ pixels associated with the window [25]. We can express the nonlinear operation of the median filter mathematically as Eq. (1) where $i, j \in \mathbb{Z}^+$ and $P_{mf}(i,j)$ denotes the filtered pixel at $(i, j)$ position.

$$P_{mf}(i,j) = \text{median}(\{ P(i+k,j+l) \mid k,l \in \mathbb{Z} \} \cap \{ \lfloor -\frac{n-1}{2}, \ldots, \frac{n-1}{2} \rfloor \})$$ (1)

Usually, a realization of the median filter requires sorting an array carrying $n^2$ pixels up to the mid-position. However, for a binary image, the implementation is quite simple and involves counting the number of occurrences of “1” in an $n \times n$ patch. If the count equals or exceeds $\lceil \frac{n^2}{2} \rceil$, a “1” is assigned to the center pixel of the filtered image. The mathematical operation of a median filter for a binary image follows Eq. (2)

$$P_{mf}(i,j) = \begin{cases} 1, & \text{if } \Sigma P(i+k,j+l) \geq \lceil \frac{n^2}{2} \rceil \\ 0, & \text{otherwise} \end{cases}$$ (2)

where $\lfloor . \rfloor$ rounds a number to its nearest higher integer.

B. Proposed Non-overlap Median Filter

In a conventional median filter, an $n \times n$ window slides over an image in an overlap fashion where the stride, $s = 1$ as shown in Fig. 2(a). A simple implementation of the same following von Neumann architecture requires $n^2+1$ clock cycles and associated energy to fetch and sum up $n^2$ pixels bit by bit followed by a comparison and a write operation in a separate memory. In contrast, since the neighboring pixels of an image have similar characteristics, we propose to apply the decision of an $n \times n$ window to all the $n^2$ pixels instead of the center one. This is equivalent to having stride $s = n$ (Fig. 2(b)), resulting in a non-overlap median filter (NOMF) that we use in this work. While the proposed approach changes the object boundary slightly, it reduces the processing and memory access time by a factor of $n^2$ and enables the same memory to be utilized to store the filtered image. Furthermore, it facilitates circuit-level filter implementation for image denoising leveraging read disturb phenomenon of a 6T-SRAM.
may further trigger electromigration induced reliability issues. Furthermore, the strength and area of BL and BLB drivers need to be very high to clear all 240 SRAM cells at once (worst case scenario). To address these concerns, we enable 16 WLs in every clock cycle involving \( 240/16 = 15 \) clock cycles to erase the memory.

2) Write Memory: Since the addresses of the events are non-contiguous by nature, unlike a conventional SRAM, either a single byte or word cannot be written. Consequently, we implement a single bit writing circuitry enabling particular WL and bit-line pair (BL to \( VDD \) and BLB to \( 0 \) V) pointed by the yaddr and xaddr signals, respectively. We discuss the memory write and its associated circuitry in section III-B in detail.

3) Filter Image: In general, background comprising “0” valued pixels surrounds a noise pixel, and the noise should be removed by a filtering operation. To implement an \( n \times n \) window of a filter, the IMF controller enables \( n \) WLs and shorts \( n \) BLs and BLBs separately using transmission gates \( (n \in \{3,5\}) \). Initially, both bitlines (BL and BLB) get precharged to \( VDD \). Once \( n \) WLs are asserted high, one of the bit-lines discharges faster and causes bit flips. Next, we talk about the theory of the proposed filter and its circuit-level design.

### III. IN-MEMORY FILTERING (IMF)

This section describes the top-level architecture of in-memory filtering, and the detailed circuit-level implementation of the proposed NOMF utilizing the read disturb phenomenon of a 6T-SRAM. Performance analysis of the proposed method is presented at the end of this section.

#### A. System Overview

The proposed IMF processor architecture shown in Fig. 3 consists of an address event representation module (AER), a \( 128 \times 32 \) bit asynchronous buffer, an IMF controller, and a \( 320 \times 240 \) SRAM macro. The AER module follows an address event representation (AER) protocol \[26\] to receive the event data asynchronously. It has a 10-bit data (address and polarity of an event) line and two control lines—‘Req’ and ‘Ack’ for synchronization and uses a 4-phase handshake mechanism. The IMF has two clock domains: ‘sysClk’ for filtering, and ‘aerClk’ for processing raw events from an NVS. Since the asynchronous AER communication protocol takes multiple aerClk cycles to transfer an address of an event, the frequency of aerClk can be kept higher than the sysClk without overloading the asynchronous buffer whose size can also be reduced as a result. The IMF controller performs three primary operations sequentially: clear memory, write memory, and filter image, as shown at the bottom of Fig. 3. The row and column signals from the IMF controller are 240-b and 320-b, respectively, following the dimensions of the macro except the bank select (BS). All signals are controlled either in parallel or independently to perform the three primary operations.

1) Clear Memory: Since the NVS only reports pixels with value 1 which are generally sparse, the memory is fully cleared before writing 1 at these few addresses. Bit-line (BL) and its complement (BLB) are driven to 0 and \( VDD \) respectively to clear the SRAM macro. Once a word line (WL) is made high, all SRAM cells in that particular row get cleared. Enabling a WL in every clock cycle stretches the execution time (240 clock cycles). In contrast, asserting all WLs high leads to a higher surge current at the bit-line pair (BL/BLB), which coupled with small size due to layout constraints
BLB) gets discharged due to the stored value in the SRAM. Likewise, having charged BL and BLB lines to VDD in a half cycle, if multiples WLs are enabled simultaneously in the next half keeping BL and BLB floating, one of the stored bits (“1” or “0”) in the selected SRAM cells dominates and discharges one of the BL lines faster than other line similar to a read disturb situation. Consequently, the faster discharged line causes a bit flip to the SRAM cells. For instance, if the IMF controller enables three SRAM cells storing “010”, BL gets discharged faster than BLB. As a result, the SRAM cell storing “1” flips to “0”. At the end of this process, all the three SRAMs store “0” indicating a majority operation.

We follow the above procedure of an SRAM read disturb to implement the NOMF for noise removal from an image since median filtering for a binary image is equivalent to the majority operation. The IMF controller enables n consecutive word-lines (WL) to discharge BL and BLB simultaneously. BLs and BLBs of n successive columns are connected separately using transmission gates to implement a 3 × 3 patch/window, as shown in the inset (right-middle). This enables highly parallel noise filtering of 320 × 3 cells in two clock cycles.

![Fig. 4. Architecture of a 320 × 240 SRAM macro for image denoising. In filter mode, the IMF controller enables three consecutive word-lines (WL) to discharge bit-line (BL) and bit-line bar (BLB) simultaneously. BLs and BLBs of three successive columns are connected separately using transmission gates to implement a 3 × 3 patch/window, as shown in the inset (right-middle). This enables highly parallel noise filtering of 320 × 3 cells in two clock cycles.](image)

![Fig. 5. Timing diagram of different signals in filter mode.](image)

where $i_s$ denotes the discharging current of each SRAM cell, and $C_{BL}$ is a combination of the parasitic capacitor of metal routing of BL or BLB and diffusion capacitor of access transistors (NA1 or NA2). Post-layout simulation after parasitic extraction provides $C_{BL} \approx 140fF$. The IMF controller keeps all the bank select signals high, facilitating highly parallel processing in the memory. It processes 320 × n cells simultaneously in two clock cycles and repeats the procedure until all the rows are filtered requiring a total of 240/n repetitions of the above operation. At every alternate period, BLs and BLBs get precharged to VDD followed by the enabling of n successive WLs in the next cycle (timing diagram is shown in Fig. 5) causing (n × n) SRAM cells to discharge BLs and BLBs simultaneously, as shown in Fig. 6(a).

Intuitively, the n × n patch can be thought of as a circuit where two latches of different strength and stored values are connected to BL and BLB. Whichever wins in discharging BL...
D. Effect of Statistical Variations

In this section, we analyze the effect of statistical variations on the filtering operation. While discharging BL and BLB, a voltage difference between the lines builds up after WL is enabled and finally a bit is latched on the entire patch with the trip point of the latch is reached. Denoting by $\Delta t$ the time difference between reaching of trip point on BL and BLB, we get:

$$\Delta t = n C_{BLB}(B) \left( \frac{V_{BL,trip}(k)}{I_{BL}(k)} - \frac{V_{BLB,trip}(k)}{I_{BLB}(k)} \right)$$

where $k$ denotes the number of non-zero (or “1”) pixels in the patch and we assume mismatch between capacitances on BL and BLB are negligible, trip points are denoted by $V_{BLB,trip}(k)$ and discharge currents by $I_{BLB}(k)$ where the dependence on $k$ is made explicit. Each of these terms are also affected by statistical variations and this leads to a probability of error, $\epsilon$. To formalize this, we first note that ideally, we expect $\Delta t > 0$ for $k \geq \left\lceil \frac{n^2}{2} \right\rceil$ and $\Delta t < 0$ otherwise. Then, we can express the probability of error, $P(\epsilon)$ as follows:

$$P(\epsilon) = P(\Delta t < 0) \text{ for } k \geq \left\lceil \frac{n^2}{2} \right\rceil$$

$$+ P(\Delta t > 0) \text{ for } k < \left\lceil \frac{n^2}{2} \right\rceil$$

While we cannot obtain closed form solutions for these equations and need to resort to Monte Carlo simulations, we can gain some insight by analyzing extreme cases. For $k = 0$ or $k = n^2$, one of $I_{BLB}$ or $I_{BL}$ equals 0 and the mismatch does not affect the final decision resulting in $P(\epsilon) = 0$. On the contrary, the NOMF takes the longest time to flip the minority pixels when the difference between the number of “0’s and “1” is one (i.e. $k = \left\lceil \frac{n^2}{2} \right\rceil$ or $\left\lceil \frac{n^2}{2} \right\rceil$). This deteriorates further due to the mismatch of the discharging current and capacitor and could force the majority pixels to flip wrongly.

However, the probability of $\left\lceil \frac{n^2}{2} \right\rceil$ noise pixels appearing inside the faulty image patch is quite low. By analyzing the dataset described in section V.B we observe that the probability of four noisy pixels occurring in a 3x3 image patch is only $\approx 0.001$ making the net bit flip error ratio (BER) quite small. The unintended bit flips reduce the object boundary when the majority pixel is “1” and inserts a new object in the frame in the opposite scenario. Reduction of object boundary is not very critical since classification by CNN is not very sensitive to reduction of few boundary pixels; moreover, it can be corrected by a following region proposal block. The insertion of a new object in the frame is critical since it increases the processing in the subsequent stages but could potentially be corrected by a tracker operating on these regions across many frames [13].

Nevertheless, the memory cell is designed to minimize bit errors due to variations. Intuitively, since BL and BLB are discharged by NOMF transistors with $I_d$ denoting unit cell discharge current, to reduce $\frac{\mu}{l}(I_b)$, size of the bit-cell transistors and overdrive voltage ($V_{GS} - V_T$) can be increased [30]. In our case, width and length of NA1, NA2, ND1, and ND2 are increased by a factor of 2 from its minimum value supported by the process (increased $W=240\text{nm}$, $L=120\text{nm}$), and low VT devices are used to maximize overdrive voltage. Fig. 6(b) tabulates the results of Monte Carlo simulations at VDD = 0.7 V and 1.2 V, respectively, for a minimum sized SRAM cell and the redesigned one, showing almost error free operation at 1.2 V and $\approx 8X$ reduction in BER (BER = $\frac{\text{# unwanted bit flips}}{\text{# MC iterations}}$) at 0.7 V.

Since we are using the low-VT (LVT) devices, a trade-off exists between the choice of devices and leakage current. To explore this, we have simulated the leakage current, and normalized standard deviation of BL/BLB discharge current ($\sigma$) of an SRAM cell for low-VT (LVT), medium-VT (MVT), and high-VT (HVT) NMOS. The discharge current variation is significant at lower supply voltage and higher VT devices due to lower overdrive.
In a post-layout simulation, we have observed that the parasitic capacitance on the BL and BLB are almost the same (139.6fF and 140.4fF). However, due to inaccuracies of fabrication steps, there can be a difference in parasitic capacitance (ΔC) between BL and BLB. To see the effect of unbalanced capacitance, we have simulated 1000 points Monte Carlo simulation at the worst-case pattern (5"1"s\_4\_0"s) and several supply voltages for different BL capacitance values. The BER is plotted in Fig. 8, where the x-axis represents the percentage variation of BL capacitance. The variation of the parasitic capacitance (ΔC) in opposite the direction reduces the BER for 5"1"s\_4\_0"s pattern. Similar analysis can be performed for 4"1"s\_5\_0"s pattern for different BL capacitance values. The capacitance mismatch can be partially corrected by connecting small capacitors (~5−10fF) on both BL and BLB lines and enabling one of them if required.

### E. Effect of Temperature variations

To evaluate the robustness of the proposed NOMF across temperature, we have performed 8000 point Monte Carlo (MC) simulations of a 3 × 3 image patch initialized at five random discrete 5"1"s\_4\_0"s patterns (inset of Fig. 9(a)) chosen randomly out of \((\binom{4}{3})^5\) possible patterns. Fig. 9(a) presents the BER (BER = \# unwanted bit flips / \# MC iterations) of an SRAM with 3 × 3 filter window at different temperatures and VDD = 0.7V. The Fig. 9(a) illustrates that with an increase in temperature, the number of unwanted bit flips reduces. This is reasonable since at a higher temperature, the threshold voltage of an NMOS reduces, which in turn lowers the normalized standard deviation of BL/BLB discharge current (\(\frac{\gamma}{\alpha} (I_b)\)). The increased error at low-temperature can be nullified by increasing the supply voltage/WL drive linearly with lower temperatures [31]. Fig. 9(b) presents the 1000 points Monte Carlo simulation across different corners. As expected, the BER increases at SS corner due to the lower overdrive of the transistors.

### F. Performance

The advantages of the proposed in-memory computing-based NOMF are four-fold. Firstly, it reduces the dynamic power consumption while reading SRAM cells for filtering by a factor of \(n\). The proposed approach charges \(n\) BL and BLB lines once to filter out \(n^2\) pixels, whereas the traditional method requires to charge \(n^2\) BL and BLB lines to read the same number of pixels. Secondly, it eliminates the usage of a sense amplifier to detect a voltage difference between BL and BLB lines. The \(n \times n\) SRAM cells act as a sense amplifier and decides on the basis of the majority bit. Thirdly, the proposed approach does not consume any BL and BLB dynamic power during writing the filtered value to the \(n \times n\) SRAM cells since the discharges of BL and BLB are related to the read operation. Lastly, it consumes minimal energy to flip the minority pixels (only noise and boundary pixels of an object).

A comparison of the proposed in-memory computing-based NOMF with other event and frame based denoising techniques are shown in Table I for processing a \(W \times H\) image. The event-based nearest neighbour filter (NN-filt) [32] stores the timestamp of an incoming event using \(\beta_t (\beta_t=16)\) bit per timestamp [9]. Further, it marks the event as valid if the difference of timestamps in an \(n \times n\) spatial neighbourhood is less than a specified threshold. The parameter, \(\gamma\) represents the average number of events during the frame duration, which can be estimated as the average object size (\(<0.7%\) (bike)-12% (truck))—given in Table I [13] times the average firing rate (\(< 2\)) of a single pixel. As discussed, IMC reduces the number of memory read while filtering images by a factor of \(n\). Parameter \(\alpha\) represents the fraction of the pixels that need to be flipped for the filter implementation (only noise and boundary pixels of the objects). We estimate \(<\alpha> \approx 0.015\) by analyzing 300k image frames from a DAVIS camera recording traffic scenes resulting in \(<135\times memory writes for our proposed system compared to NN-filt.

Compared to digital implementations of both median filter and NOMF, the proposed IMC based NOMF has at least \(n\) times the average firing rate (\(< 2\)) of a single pixel. As discussed, IMC reduces the number of memory read while filtering images by a factor of \(n\). Parameter \(\alpha\) represents the fraction of the pixels that need to be flipped for the filter implementation (only noise and boundary pixels of the objects). We estimate \(<\alpha> \approx 0.015\) by analyzing 300k image frames from a DAVIS camera recording traffic scenes resulting in \(<135\times memory writes for our proposed system compared to NN-filt.

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**Table I**

| Input   | # memory read | # memory write | # operations | # SRAM Cells |
|---------|---------------|---------------|--------------|--------------|
| NN-filt | Events \(\beta_t \gamma n M\) | \(\gamma n M\) | \(\beta_t M\) |              |
| Median Filter | EBBI \(n^2 M\) | M | \(n^2 M\) | 2M |
| NOMF | EBBI M | M | M | M |
| NOMF+IMC | EBBI M/\(n\) | \(\alpha M\) | 0 | M |

\(\beta_t = 16, \gamma \approx 12.7\%, M = HW, \alpha \approx 1.5\%, n \in \{3, 5\}\).
times less memory reads and $\frac{1}{6}$ times less memory writes. Furthermore, no operations by an external processor are needed in the proposed NOMF since all operations are done within the memory.

IV. RESULTS

We implement the proposed NOMF filter in a 65nm LP CMOS process. The unit SRAM cell layout and micrograph image of the prototype chip are shown in Fig. 10(a) and (b) respectively. The prototype occupies $0.55 \text{mm}^2$ and has utilization of 78.6% and a capacity of 75kb. We do not include the AER and asynchronous FIFO areas in the calculation of area utilization since they are outside the macro. An Opal Kelly FPGA is used to interface the PC with the test chip as shown in Fig. 10(c) and is responsible for sending noisy images to the chip and relaying filtered images back to the PC for further analysis. In the following sections, we present results of characterization of the designed IC in detail and compare the performance of the proposed NOMF with the conventional median filter in the applications of object tracking and detection.

A. Mismatch Characterization

In this section, we measure the effect of unit cell current and latch trip point variation on the filtered image. Since the memory has a capacity of 75 kb, the whole memory can be regarded as 8480 $3 \times 3$ image patches. The $n \times n$ patches in the memory are initialized with particular patterns of $k$ “1”s and $(n^2 - k)$ “0”s where $k \in \{3, 4, 5, 6\}$ and $n = 3$. The IMF controller enables the denoising operation once the initialization is over. Eventually, the external FPGA board (shown in Fig. 10(c)) is used to read out the filtered image and detect the unintentional bit flip due to mismatches of the $n^2$ SRAM cells. We carry out the same experiment for $\left(\frac{n^2}{k}\right)$ discrete patterns of $k$ “1”s and $(n^2 - k)$ “0”s initialized in all patches.

Fig. 11 shows the BER ($\text{BER} = \frac{\# \text{ unwanted bit flips}}{\# \text{ patches}}$) of four devices due to the discharge current mismatch of nine SRAM cells of a $3 \times 3$ filter patch where $\# \text{ patches} = 8480$. The measurement is carried out for 126 $5^1$‘s $4^0$‘s discrete patterns across supply voltages at nominal temperature.

Fig. 12. Mean BER of the IMC based NOMF measured for 1000 noisy images at VDD = 0.7V and 1.2V.

B. Image Denoising

To show the effect of the unintentional bit flip in real video recordings, we fed 1000 event-based binary images (EBBI) from the traffic dataset [13] captured using a DAVIS

TABLE II

| Location | Car/Van | Bus | Bike | Truck |
|----------|---------|-----|------|-------|
| Location 1 | $16 \times 42$ | $31 \times 94$ | $15 \times 21$ | $22 \times 50$ |
| Location 2 | $25 \times 47$ | $52 \times 107$ | $17 \times 22$ | $35 \times 61$ |
| Location 3 | $34 \times 82$ | $64 \times 180$ | $26 \times 44$ | $50 \times 104$ |

1Dataset: https://zenodo.org/record/3839231
camera [28]. We describe the dataset in brief for completeness. A DAVIS setup was deployed at three places to collect three recordings of varying duration at different lens settings. Subsequently, events are aggregated at a frame rate of 15Hz ($t_f = 66$ms) to create event-based binary image (EBBI) frames. Table I summarises the sizes of different objects at three different locations. We randomly select 1000 frames. Table II summarises the sizes of different objects at three different locations. We randomly select 1000 frames. To evaluate the effect of NOMF filtering images at the system level and compare with the conventional median filter, we feed both of them $\approx 70k$ raw noisy images from the earlier dataset and the filtered images are sent as input to the object tracking pipeline described in [13]. Since data transfer between the PC and the IC is a bottleneck in terms of speed and there is little differences between the chip output and software NOMF operation (average 1.7 and 0.048 errors per image at 0.7V and 1.2V) respectively as shown in Fig. 13, we perform this system evaluation entirely in software. Moreover, the error occurs at the boundary of the object, as shown in Fig. 14 this gets mitigated by scaling down the image as part of the region proposal [13].

Note that the tracking involves region proposal network, and we follow connected component labeling (CCL) [33] algorithm to estimate the region of interests (ROIs) followed by an overlap tracker (OT) [13] which is a simplified form of Kalman filter. In order to evaluate the system performance, we calculated the weighted $F1 - score$, $F1_{thr}^{wgt}$ using all tracks predicted for all test recordings as follows:

$$\text{IoU} = \frac{A_{GT}}{A_{GT} \cup A_{P}}$$  \hspace{1cm} (7)

$$\text{Precision}, P_i^{thr} = \frac{\text{true positive regions}}{\text{total proposed regions}}$$  \hspace{1cm} (8)

$$\text{Recall}, R_i^{thr} = \frac{\text{true positive regions}}{\text{total ground truth regions}}$$  \hspace{1cm} (9)

$$F1 - score, F1_i^{thr} = \frac{2 \times P_i^{thr} \times R_i^{thr}}{P_i^{thr} + R_i^{thr}}$$  \hspace{1cm} (10)

$$F1_{thr}^{wgt} = \frac{\sum_{i=1}^{r} N_i^{tracks} \times F1_i^{thr}}{\sum_{i=1}^{r} N_i^{tracks}}$$  \hspace{1cm} (11)

where $A_{GT}$ and $A_{P}$ denote the area of manually annotated ground truth and region proposed by the OT encapsulating an object, respectively. If the IoU of a proposed region is greater than a threshold, $thr$ the region is assumed to be a

C. System evaluation

1) Object Tracking: To evaluate the effect of NOMF filtering images at the system level and compare with the conventional median filter, we feed both of them $\approx 70k$ raw noisy images from the earlier dataset and the filtered images are sent as input to the object tracking pipeline described in [13]. Since data transfer between the PC and the IC is a bottleneck in terms of speed and there is little differences between the chip output and software NOMF operation (average 1.7 and 0.048 errors per image at 0.7V and 1.2V) respectively as shown in Fig. 13, we perform this system evaluation entirely in software. Moreover, the error occurs at the boundary of the object, as shown in Fig. 14 this gets mitigated by scaling down the image as part of the region proposal [13].

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$$\text{IoU} = \frac{A_{GT}}{A_{GT} \cup A_{P}}$$  \hspace{1cm} (7)

$$\text{Precision}, P_i^{thr} = \frac{\text{true positive regions}}{\text{total proposed regions}}$$  \hspace{1cm} (8)

$$\text{Recall}, R_i^{thr} = \frac{\text{true positive regions}}{\text{total ground truth regions}}$$  \hspace{1cm} (9)

$$F1 - score, F1_i^{thr} = \frac{2 \times P_i^{thr} \times R_i^{thr}}{P_i^{thr} + R_i^{thr}}$$  \hspace{1cm} (10)

$$F1_{thr}^{wgt} = \frac{\sum_{i=1}^{r} N_i^{tracks} \times F1_i^{thr}}{\sum_{i=1}^{r} N_i^{tracks}}$$  \hspace{1cm} (11)

where $A_{GT}$ and $A_{P}$ denote the area of manually annotated ground truth and region proposed by the OT encapsulating an object, respectively. If the IoU of a proposed region is greater than a threshold, $thr$ the region is assumed to be a
true positive region. \( N_{i, \text{tracks}} \) denotes the number of tracks in recording \( i \) and \( 1 \leq i \leq r \), where \( r \) represents the total number of recordings. We use the \( F1 - score \) as a metric that combines both precision and recall to compare different filtering methods.

Fig. 12 presents a MATLAB simulation of the weighted \( F1 - score \) of an overlap based tracker (OT) using filtered images following conventional median filter and NOMF for different IoU thresholds ranging from 0.1 to 0.9. This allows us to evaluate the performance of the system over a range of thresholds and the area under this curve (AUC) is a good metric to compare robustness and performance of all methods. Following the method in [13], we scale down the images for the CCL algorithm used in the analysis as follows

\[
I_{a,b}^{i,j} = \bigvee_{k=0,l=0}^{a-1,b-1} I(ai + k, jb + l)
\]

where \( I(i,j) \in \{0,1\} \) and \( a, b \) are rescaling factors along the horizontal and vertical axis, respectively, and \( \bigvee \) represents the logical-OR operation on a \( a \times b \) window. \( w \) and \( h \) denote the width and height of an image frame, respectively. We noticed that the rescaling of images in CCL majorly helps in handling the fragmentation observed in the recordings at the original resolution. This fragmentation occurs due to the invariance in illumination on the glass windows of the objects. Hence, an appropriately chosen downscaling may be able to merge the fragmented objects such as buses, trucks, etc.

It is essential for the region proposal block to correctly identify the regions for the tracker to run properly and to improve the \( F1 - score \) characteristics. Therefore, we varied the rescaling factors along the horizontal and vertical axis of an image frame and noticed that the performance of the NOMF is nearly the same (difference of \( < 0.008 \) of area under the curve) as the conventional filter (OMF) for \( 8 \times 6 \) and \( 8 \times 3 \) rescaling factors. It is worth mentioning that for other values of the rescaling factors, the area under the curve of the weighted \( F1 - score \) for the images from both filters is lower than 0.23.

2) Object Classification: To assess the effect of approximation of NOMF on object classification, we have also classified vehicles into 4 categories (Car, Bus, Truck/Van and Bike) from the above traffic dataset following [34]. Objects in each frame are manually labelled and also the same objects across frames are assigned the same track identifier—this comprises the ground truth. We employ a modified LeNet5 architecture [35] consisting of two convolutional (\( 5 \times 5 \times 6 \) and \( 5 \times 5 \times 16 \)) layers and three fully connected (FC) layers (\( 120 \times 84 \times 4 \)) where the last layer had a softmax nonlinearity while others had ReLU. A \( 2 \times 2 \) average pooling layer follows each convolutional layer. Since the LeNet5 architecture requires a fixed size input, we have selected a \( 42 \times 42 \) image patch around the centre of a valid object from EBBI. The \( 42 \times 42 \) patches are filtered using both conventional median filter (OMF) and NOMF to produce two different datasets for the same LeNet5 model. For a fair comparison, the same LeNet5 model is trained and tested separately using 91885 and 9063 filtered images from the conventional median filter and NOMF, respectively, following the methodology used in [34].

Table III shows the per sample and per track accuracy for all test samples across different categories. To estimate per track accuracy, the final category is obtained by voting across the classification scores for all the images in a track across multiple frames [34]. We use balanced accuracy as a metric to overcome the imbalance in number of test samples across classes. Even though the balanced sample-wise classification accuracy using NOMF filtered images is \( \approx 2\% \) lower than that using OMF, it can be seen that the track-wise accuracy for NOMF is slightly higher, as shown in the right column of Table III. While it could require more data to test if this difference is statistically significant, we can conclude that the system level performance of NOMF filtered images is similar to OMF ones.

### Table III

| Category | per sample (%) | per track (%) |
|----------|----------------|---------------|
|          | Median Filter  | NOMF | Median Filter | NOMF |
| Car      | 83.72          | 83.53 | 95.24         | 95.24 |
| Bus      | 92.38          | 86.72 | 96.55         | 96.55 |
| Truck/Van| 67.39          | 70.48 | 75             | 78.12 |
| Bike     | 65.98          | 63.07 | 100            | 100   |
| Balanced | 75.25          | 73.42 | 90.52         | 91.56 |

D. Energy Measurement

As mentioned in Fig. 1, it is imperative to have a very low energy dissipation for the image denoise operation needed to detect blank image frames. For normal operation, the measured read and write energy of the memory, are \( 0.916 \) and \( 6 \) pJ per bit at \( 1 \) V respectively, close to the corresponding simulated values of \( 0.626 \) and \( 5.1 \) pJ, respectively.

The more critical component is the energy dissipated for image filtering. Fig. 15 (left Y axis) shows the average current consumption across different frequencies as well as supply voltages for this operation. It can be seen from the fig. that the IMF operates at power supply voltage closer to \( 0.7 \) V. However, the maximum operating frequency decreases due to read and write failure of configuration registers at this voltage. Note that, even though the current consumption is measured up to \( 48 \) MHz, the prototypes are operational at \( 70 \) MHz. The total current consumption of the test chip during NOMF operation can be formulated as:

![Fig. 15. Measured current (mA) consumption (left Y axis) and energy/pixel (right Y axis) vs frequency at different supply voltages.](image-url)
\[ I_{total} = I_{bit\text{flip}} + I_{leakage} + I_{IMF} + I_{ch} \]
\[ \approx I_{IMF} + (\rho + \lambda) N_{col} C_{BL(B)} + n C_{WL} V_{DD} \frac{f}{2} \]  

(13)

where \( I_{bit\text{flip}} \) represents the current due to the bit flip operation during read-disturb, \( I_{IMF} \) is the current consumed by the digital controller and \( I_{ch} \) is the BL and BLB precharge current. Also, \( N_{col} (=320) \) denotes the number of columns, \( \rho = \Delta V_{fmin} \) and \( \lambda = \Delta V_{fmin} \) represent the fraction of BL and BLB discharge with reference to VDD, respectively. \( I_{bit\text{flip}} \) can be neglected since its magnitude from simulations is small (≈ 0.68% of \( I_{ch} \) at \( k = 1 \) from Fig. 16(a)). \( I_{leakage} \) denotes the leakage current, which is also negligible at higher operating frequencies (<1%)—this is measured from the current consumed when no clock is supplied to the chip.

To estimate the fraction of power dissipated in \( I_{IMF} \), we use the above model in Eq. (15) to estimate the last term \( I_{ch} \) by calibrating the parameters from simulations and estimating the values of \( \rho \) and \( \lambda \) based on the input. For a blank (all “0”s) or a full (all “1”s) image patch, \((\rho, \lambda) = (0, 1) \) and \((\rho, \lambda) = (1, 0) \), respectively. However, in the case of a noisy image having \( k \) pixels in each \( n \times n \) window, we can show that \( 1 \leq \rho + \lambda \leq 1 + \beta \frac{\min(k,n^2-k)}{\max(k,n^2-k)} \) where \( \beta = 1 - \frac{V_{trip}}{V_{DD}} \) and \( V_{trip} \) denotes the trip point voltage of a latch (back to back inverters) in the 6T-SRAM. It is seen from SPICE simulation that \( \beta = 0.7 \), \( C_{WL} = 330fF \) and \( C_{BL} = C_{BLB} = 140fF \). It is worth noting that the IMF controller takes two clock cycles to filter out \( n \) rows for the ease of implementation. Hence, we use the factor \( \frac{1}{n} \) in the formulation for total current. Implementation of denoising of \( n \) rows in a single clock cycle would have doubled the throughput of the system. However, energy consumption would remain the same to a first order approximation.

The left Y axis of Fig. 16(a) presents the simulated and modelled BL and BLB charging current for \( n = 3 \) across different values of \( k \) at \( VDD=1.2V \) and 48MHz, where \( k \) denotes the number of “1”s in all \( 3 \times 3 \) patches. We can see an excellent match across all values of \( k \). Analyzing the image statistics from the dataset in [13], we can see from Fig. 16(b) that only 9.5% of total patches contain a single noisy pixel \( (k=1) \), resulting in \( \rho + \lambda \approx 1.01 \). Hence, the average value of \( I_{ch} \) can be estimated to be \( \approx 1.331 \) mA in real settings. Now, using this calibrated model from simulations, we can estimate from the measured results of Fig. 15 that the IMF controller current, \( I_{IMF} \), contributes \( \approx 36\% \) of the total current.

Fig. 15 (right Y axis) presents the processing energy per pixel of the proposed prototype IC across different operating frequencies and supply voltages for the \( 3 \times 3 \) filter window. The figure illustrates that the leakage energy dominates at lower operating frequencies. However, at higher frequencies, the curves remain flat. It is worth mentioning that the proposed NOMF consumes 30fJ to process a pixel at \( VDD=0.7V \) for the \( 3 \times 3 \) filter window. Moreover, at higher filter sizes (e.g., \( 5 \times 5 \)), processing efficiency increases by \( \approx \frac{3}{5} \times \).

E. Comparison

Fig. 17 compares the performance of the proposed test chip (IMF) with a spatio-temporal filter [36] and digitally implemented median filter. Furthermore, several works on hardware implementation of image denoising are compared in Table V. Note that the spatio-temporal filter [36] works on the asynchronous events from an NVS, whereas the IMF and digital counterpart process event-based binary image. They reported \( \approx 1mW \) simulated power for 50Meps (million events/second) resulting in 20pJ/bit. Since the IMF (configuration register read and write operations) ceases to work beyond 24MHz at \( VDD = 0.7V \), we assume the maximum operating frequency to 24MHz for the estimation of processing per pixel of the digital counterpart. We have estimated the energy and processing time for four different digital implementations of conventional median filter. (a) Median filter (MF): This architecture features single pixel read and process in every clock cycle-the execution time for this implementation is \((n^2+1)WH\) clock cycles \((W = \text{image weight}, H = \text{image width})\).
TABLE V

COMPARISON OF DIFFERENT PUBLISHED IMC WORKS

| Technology | This Work | ICASSP’15 [36] | TCAS-II’20 [37] | ASP-DAC’20 [38] |
|------------|----------|----------------|-----------------|-----------------|
| SRAM type  | 6T       | 6T             | 6T (split WL)   | 6T (split WL)   |
| Algorithm  | Image denoising | CNN | BNN | Versatile DNN | BNN | BNN |
| SRAM capacity | 9.375kB | 9.468kB | 2kB | 102kB | 2kB | 2kB |
| Operating voltage (V) | 0.7-1.2 | 1.3-2.5 | 1.1 | 1.1 | 1.1 | 1.1 |
| input/weight precision | 15b/15b | 15b/15b | 15b/15b | 15b/15b | 15b/15b |
| Peak Throughput (GOPS) | 134.4 | 278.2 | 278.2 | 3180 | 615 | 8 |
| Peak Energy Efficiency (TOPS/W) | 51.3 | 51.3 | 51.3 | 300 [55.6] | 51.3 |
| Area Efficiency (TOPS/mm²) | 0.243 | 0.243 | 0.243 | 0.243 | 0.243 |

| Technology | This Work | JSSC’18 [10] | TCAS-I’19 [39] | JSSC’19 [16] |
|------------|----------|---------------|-----------------|---------------|
| SRAM type  | 65nm     | 65nm          | 65nm            | 65nm          |
| Algorithm  | Image denoising | CNN | BNN | Versatile DNN | BNN | BNN |
| SRAM capacity | 9.375kB | 9.375kB | 9.375kB | 9.375kB |
| Operating voltage (V) | 0.7-1.2 | 0.7-1.2 | 0.7-1.2 | 0.7-1.2 |
| input/weight precision | 15b/15b | 15b/15b | 15b/15b | 15b/15b |
| Peak Throughput (GOPS) | 134.4 | 278.2 | 278.2 | 3180 |
| Peak Energy Efficiency (TOPS/W) | 51.3 | 51.3 | 51.3 | 300 [55.6] |
| Area Efficiency (TOPS/mm²) | 0.243 | 0.243 | 0.243 | 0.243 |

TABLE VI

COMPARISON OF DIFFERENT PUBLISHED IMC WORKS

| Technology | This Work | ICASSP’15 [36] | TCAS-II’20 [37] | ASP-DAC’20 [38] |
|------------|----------|----------------|-----------------|-----------------|
| SRAM type  | 6T       | 6T             | 6T (split WL)   | 6T (split WL)   |
| Algorithm  | Image denoising | CNN | BNN | Versatile DNN | BNN | BNN |
| SRAM capacity | 9.375kB | 9.468kB | 2kB | 102kB | 2kB | 2kB |
| Operating voltage (V) | 0.7-1.2 | 1.3-2.5 | 1.1 | 1.1 | 1.1 | 1.1 |
| input/weight precision | 15b/15b | 15b/15b | 15b/15b | 15b/15b | 15b/15b |
| Peak Throughput (GOPS) | 134.4 | 278.2 | 278.2 | 3180 |
| Peak Energy Efficiency (TOPS/W) | 51.3 | 51.3 | 51.3 | 300 [55.6] |
| Area Efficiency (TOPS/mm²) | 0.243 | 0.243 | 0.243 | 0.243 |

a) Assuming energy efficiency to 65nm implementation following energy efficiency ∝ \( \frac{1}{(Tech/node)^2} \).
b) Assume the filter kernel is convoluted over the binary image and all the filter weights are 1.

height). This is a scalable architecture where more cycles are needed for bigger images but the hardware cost is fixed. (b) Median filter with pipelined read (MFPR): This architecture has a pipelined design and reads W pixels simultaneously. This implantation takes 2nH clock cycles to denoise an image and requires W processing elements (adder). It is to be noted that for different values of n, we need different n-bit adders. This results in a higher silicon area; it is also difficult to scale up with a higher resolution image due to area constraints. (c) Median filter with Row Buffering (MFRB): This design reads a single pixel at a time and has n-1 row buffers of width W. In this case, n − 1 consecutive rows of an image are stored in the buffer and used in the subsequent filtering operation while stride moves in the vertical direction. The oldest row is replaced by the new row read. This will save 2n memory read energy. (d) Median filter with pipelined read and row buffer (MFPRBB): The last architecture combines both pipelining and row buffering. This parallel-pipelined and row buffered implementation takes approximately 2H clock cycles to process an image. Since IMF takes two clock cycles to process n rows, the proposed design takes 2H cycles to denoise an image. Therefore the IMF is \( 3 - 4800 \times \) faster than the digital implementation of the median filter for \( n = 3 \).

We have estimated the energy/bit of the median filter from the read (0.916pJ) and write energy (6pJ) measurements of the designed 320 × 240 SRAM memory. The increased size 6T-SRAM designed for NOMF has 1.57× (140fF/89fF) higher parasitic capacitance on BL lines. Therefore, during the energy estimation of the conventional median filter, we have taken into account the lower parasitic capacitance. For a fair comparison, we scale down the estimated energy consumption of the digital implementation at 0.7V. Table [IV] compares the energy consumption of different filter implementations. Please note that we only consider the memory read and write energy of a single-pixel of the designed chips to estimate the conventional median energy. Even though the memory read energy will be lower by \( n \) for the parallel read implementations (MFPR, MFPRBB), and the energy dissipated by the processing element will nullify the benefit to some extent.

It can be seen from Fig. [17] that the IMF achieves 512× and > 70× energy improvement over the state-of-the-art spatio-temporal filter and digital implementation, respectively.

Similarly, it can be estimated from Fig. [14] that the NOMF achieves 1.24× energy improvement compared to the conventional median filter in object recognition system. Considering the per frame execution time of [12] at 70MHz, the object recognition system along with NOMF is 1 − 3.74× faster than that with the conventional median filter. Therefore, NOMF achieves ∼ 1.24 − 4.6× energy-delay-product improvement at the system level.

Table VI compares the performance of IMF with the recently published IMC works on Binary Weighted Network (BWN: stored weights in the SRAM are binary) and Binary Neural network (BNN: inputs and stored weights are binary). A major difference of this work with other neural networks is that we store the image in the memory and operate on it, while for the neural networks, the weights are typically stored in memory and the image pixels are streamed as inputs. To calculate the peak throughput and energy efficiency, we assume the filter kernel is convoluted over the binary image, and all the filter weights are “1”. Since the IMF processes 320 × 3 pixels in a cycle, the peak throughput is \( 2 \times 320 \times 3 \times 70M = 134.4 \) GOPS at 70 MHz. Furthermore, minimum energy consumption, 39J per pixel, translates to 51.3 TOPS/W energy efficiency at \( VDD = 0.7V \) (2 operations/pixel), which is comparable with the state-of-the-art. Note that the peak throughput depends on the operating frequency, image patch size, level of parallelism. Hence, it can be enhanced further by increasing the patch size at the cost of more approximation or by separating the memory into multiple sections along the column to increase the level of parallelism. Moreover, the
It is worth mentioning that the proposed architecture does not support multi-bit images. However, the RGB images can be transformed to event-based binary images by detecting changes (events) at the same pixel across frames comparing both linear and logarithmic pixel intensities and apply the proposed method for denoising to get the energy savings in the subsequent image processing steps for multi-bit operation.

VI. CONCLUSION

This paper presents a 6T-SRAM based image denoising hardware architecture for event-based binary image that exploits read-disturb operation. The proposed hardware consumes as low as 39fJ to process a pixel and takes 1.7μs to denoise a 240 × 180 image frame. We demonstrated that the test chip achieves a > 210× improvement of energy-delay product (EDP) compared to a fully digital implementation of the conventional median filter. This enormous gain of EDP can be attributed to the NOMF algorithm and in-memory computing, which enables the parallelism in denoising of an image. Even though NOMF introduces approximation in computation, we show that the system level metrics of object detection and tracking are minimally affected compared to the conventional median filter. The extremely low energy dissipation indicates that the proposed in-memory computing based image denoising hardware can be the right candidate for triggering ON more energy hungry object detection CNNs while maintaining low energy for blank frames and thus exploiting the temporal sparsity of video streams in IoT.

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