Investigation of Short Channel Effects on Device Performance for 60nm NMOS Transistor

U Chinnappan1 and R Sanudin1
1Nano Simulation Research Group (NanoSIM), Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia, 86400 Parit Raja, Johor, MALAYSIA

Corresponding author: rahmats@uthm.edu.my

Abstract. In the aggressively scaled complementary metal oxide semiconductor (CMOS) devices, shallower p-n junctions and low sheet resistances are essential for short-channel effect (SCE) control and high device performance. The SCE are attributed to two physical phenomena that are the limitation imposed on electron drift characteristics in channel and the modification of the threshold voltage ($V_{th}$) due to the shortening channel length. The decrement of $V_{th}$ with decrement in gate length is a well-known attribute in SCE known as “threshold voltage roll-off”. In this research, the Technology Computer Aided Design (TCAD) was used to model the SCE phenomenon effect on 60nm n-type metal oxide semiconductor (NMOS) transistor. There are three parameters being investigated, which are the oxide thickness ($T_{ox}$), gate length ($L$), acceptor concentration ($N_a$). The simulation data were used to visualise the effect of SCE on the 60nm NMOS transistor. Simulation data suggest that all three parameters have significant effect on $V_{th}$, and hence on the transistor performance. It is concluded that there is a trade-off among these three parameters to obtain an optimized transistor performance.

1. Introduction
There does not seem to be any fundamental physical limitation that would prevent Moore’s Law from characterizing the trends of integrated circuits. However, sustaining this rate of progress is not a straightforward achievement [1-4]. Figure 1 shows that the trend of power supply voltage, threshold voltage, and gate oxide thickness versus channel length for high performance CMOS logic technologies [5]. Sub-threshold non-scaling and standby power limitations bound the threshold voltage to a minimum of 0.2V at the operating temperature. Thus, a significant reduction in performance gains is predicted below 1.5V due to the fact that the threshold voltage decreases more slowly than the historical trend, leading to more aggressive device designs at higher electric fields [6, 7].
As the channel length is reduced to increase both the operation speed and the number of components per chips the SCE will arise. The critical geometry parameters which determine device short-channel behaviours spatially $V_{th}$ roll-off are gate length, fin thickness, fin height, $T_{ox}$ and channel doping [8]. The decrease of $V_{th}$ with decrease in L is a well-known SCE. For shorter channel lengths, the value of $V_{th}$ reduces. The effect of short channels becomes more pronounced as the channel length is reduced further. Short channel device has channel length which is comparable to depth of drain and source junctions and depletion width and causes threshold voltage and $I/V$ curve variations [9, 10].

Due to excellent control of the SCE, lower gate leakage current, higher on-current, and better subthreshold slope, symmetrical double-gate silicon (DG) MOSFETs with extremely short-channel length have the appropriate features to constitute the devices for nanoscale circuit design [11-13]. As for bulk MOS devices, the SCE threshold voltage is important for assessing device performance and gaining insights into device designs. Compared to single-gate devices, the $V_{th}$ of the DG devices may be difficult to define due to the co-existence of the front and the back channels [14-16].

In general, the $V_{th}$ of a MOSFET is independent on either L or gate width (W). However, when the L or W is reduced to dimensions that are comparable to the edge-affected region, then the $V_{th}$ experiences dependence on the L or W. The equation of $V_{th}$ is given as in (1), assumes that bulk depletion charge is only due to the electric field created by the $V_g$, while the depletion charge near n+ source and drain region is actually induced by PN junction band bending.

$$V_{th} = V_{FB} + 2\phi_F + \left(\frac{1}{C_{ox}}\right)\sqrt{2q\varepsilon_s N_A (2|\phi_F|)} + \frac{qD_j}{C_{ox}}$$

Therefore, the amount of bulk charge the $V_g$ support is overestimated, leading to a larger $V_{th}$ than the actual value [15]. When L becomes smaller, the $V_{th}$ begins to decrease due to the two-dimensional field effect of the drain junction. $V_{th}$ changes due to the reduction of charges in the depletion layer for reduction of L. For shorter L, the value of $V_{th}$ reduces. The conventional process such as ion implantation cannot be used to control $V_{th}$ of a vertical MOS transistor [17, 18].

The gate-oxide capacitance per unit area is defined as $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$, where $\varepsilon_{ox}$, is the permittivity of oxide and $T_{ox}$ is the oxide thickness. As the $T_{ox}$ is decreased, less $V_g$ is required for strong inversion. The oxide capacitance increases with the decrease in $T_{ox}$ and the oxide capacitance is directly proportional to the $V_{th}$. The parameters of $V_{th}$ increase with reducing the L or increasing the channel thickness [8].

---

**Figure 1.** Trends of power supply voltage $V_{dd}$, threshold voltage $V_{th}$, and gate oxide thickness $T_{ox}$ versus channel length for CMOS technologies [5].
In short-channel devices, the centre of the channel has higher electrostatic potential than anywhere because of the influence of the source/drain potential and the weak gate control below threshold, becoming the leakiest path. The short-channel devices that for appropriate device structure parameters and bias conditions, a normally-off device may also be turned normally-on if the L is made shorter than the previous one [14].

The probability of electron occupancy of an allowable state is based on the doping level in semiconductor. As the substrate doping increases, the initial threshold voltage increases and the short channel threshold shift also becomes larger. $V_{th}$ roll-off also depends on $N_a$. As the thickness of oxide is decreased, less $V_g$ is required for strong inversion [19]. Based on the carrier concentration at the minimum channel potential located at a depth $x$ of the channel, an analytical expression of the subthreshold slope has been derived in terms of the natural L [20, 21].

In this paper, the relationship between parameters that affect the threshold voltage is being investigated. These changing trend of threshold voltage will be visualised to see whether the targeted parameters are improving or withholding the device performance.

2. Modelling of SCE

Main focus of this study is to model the phenomena of SCE in 60nm NMOS transistor and its relationship with the affected parameters in device performance. The values of $T_{ox}$, $N_a$ and L were varied to study the effect of these parameters on the short channel $V_{th}$. The $C_{ox}$, potential, $x_{dT}$ width and $V_{th}$ are calculated using formula that models the SCE phenomenon. The changing trend of $V_{th}$ with respect to independent parameters are then visualised using Sentaurus TCAD. The phenomena were specified to the $V_{th}$ of SCE and study the effect of parameters in the $V_{th}$ equation as shown in (2).

$$
\Delta V_{th} = -\frac{eN_a x_{dT}}{C_{ox}} \left[ \frac{r_j}{L} \left( \sqrt{1 + \frac{2x_{dT}}{r_j}} - 1 \right) \right]
$$

(2)

The $C_{ox}$ and $x_{dT}$ can be determined using (3) and (4), respectively:

$$
C_{ox} = \frac{\varepsilon_{ox}}{\varepsilon_{ox}}
$$

(3)

$$
x_{dT} = \sqrt{\frac{4\varepsilon_s |\phi_{FP}|}{eN_a}}
$$

(4)

$$
\phi_{FP} = -V_{th} ln \left( \frac{N_a}{n_i} \right)
$$

(5)

Where $\varepsilon_{ox} = \varepsilon_r \varepsilon_0$, $V_{th}$ is the threshold voltage, $r_j$ is the junction depth of drain and source, L is the length of gate, $C_{ox}$ is the oxide capacitance, $\varepsilon_{ox}$ is the dielectric constant of silicon dioxide (SiO$_2$), $\varepsilon_0$ is the vacuum permittivity, $T_{ox}$ is oxide thickness, $N_a$ is the concentration of acceptor atoms and $n_i$ is the intrinsic carrier concentration.

2.1. Determination of $V_{th}$ against $N_a$ for different L

The $V_{th}$ is determined by varying the value of $N_a$, and the other two variables $T_{ox}$ and $r_j$ are fixed for several values of gate length. In this case, both $T_{ox}$ and $r_j$ were set at 25nm, whereas L was varied from 10nm to 130nm.
2.2. Determination of Vth against T\text{ox} for different L
Next, the Vth is determined by varying the value of T\text{ox}, with both N\text{a} and r\text{j} were set at 1×10^{16} \text{cm}^{-3} and 25nm, respectively. Similar in the case of sub section 2.1, L was varied between 10nm to 130nm.

2.3. Determination of Vth against L for different N\text{a}
Thirdly, the Vth is determined against various L while both T\text{ox}, and r\text{j} are fixed. Vth is calculated against L for T\text{ox}=25nm and r\text{j}=25nm, whereas N\text{a} was set in the range of 1.4×10^{15} \text{cm}^{-3} and 1×10^{17} \text{cm}^{-3}.

2.4. Determination of Vth against T\text{ox} for different L
Next, the Vth is determined against various T\text{ox} while both L and r\text{j} are fixed. In this case, L and r\text{j} were set at 60nm and 25nm, respectively. N\text{a} was set in the range of 1.4×10^{15} \text{cm}^{-3} and 1×10^{17} \text{cm}^{-3}.

2.5. Determination of Vth against T\text{ox} for different L
Fifthly, the Vth is determined by varying the value of L, N\text{a} and r\text{j} were set at 1×10^{16} \text{cm}^{-3} and 25nm, respectively and T\text{ox} was in the range between 10nm and 65nm.

2.6. Determination of Vth against T\text{ox} for different L
Finally, the Vth is determined by varying the value of N\text{a} with both L and r\text{j} were set at 60nm and 25nm, respectively. The range T\text{ox} in this case was between 10nm and 65nm.

In each case, the simulation was carried out in Sentaurus TCAD starting from Sentaurus Workbench (SWB), which determining the changing parameters, up to the Inspect, a tool to visualise the electrical characteristic of the NMOS transistor. The whole process is depicted in Figure 2.

![Flow chart of process simulation in Sentaurus TCAD to study the effects of short channel effects for 60nm transistor](image-url)
3. Results and discussion

In this section, the device performance will be presented in the presence of SCE according to six cases of study outlined in Section 2. There are five graphs presented to visualise the effect of these parameters over \( V_{th} \). Those graphs were plotted based on numerical simulations carried out in the Sentaurus TCAD.

3.1. \( V_{th} \) against \( L \) with varying \( N_a \)

The values of each parameter used for simulation were recorded in Table 1. Figure 3 shows the trend of \( V_{th} \) changes against \( L \) for various \( N_a \).

| \( T_{ox} \) (nm) | \( L \) (nm) | \( V_{th} \) (V) \( N_a = 1 \times 10^{16} \text{cm}^{-3} \) | \( V_{th} \) (V) \( N_a = 2 \times 10^{16} \text{cm}^{-3} \) |
|-----------------|-------------|---------------------------------|---------------------------------|
| 25              | 10          | -1.2404                          | -1.5148                          |
|                 | 45          | -0.2756                          | -0.3366                          |
|                 | 60          | -0.2067                          | -0.2525                          |
|                 | 90          | -0.1378                          | -0.1683                          |
|                 | 130         | -0.0954                          | -0.1165                          |

![Figure 3: Changing of \( V_{th} \) against \( L \) with varying \( N_a \)](image)

From Figure 3, it is observed that the \( V_{th} \) in both graphs changes sharply when \( L \) is less than 60nm. Beyond this point, the fluctuation of the \( V_{th} \) is comparatively less. The \( V_{th} \) changes due to the reduction of charges in the depletion layer for reduction of \( L \). It is also worth to note that as the \( N_a \) increases the \( V_{th} \) decreases. In general, the \( V_{th} \) obtained is higher when \( N_a = 1 \times 10^{16} \text{cm}^{-3} \) compared with \( N_a = 2 \times 10^{16} \text{cm}^{-3} \).

3.2. \( V_{th} \) against \( L \) with varying \( T_{ox} \)

The values of each parameter that used for simulation were recorded in Table 2 and the associated graph is shown in Figure 4.
Table 2. Values of $V_{th}$ for different $L$ and $T_{ox}$

| $N_a$ (cm$^{-3}$) | $L$ (nm) | $V_{th}$ (V) $T_{ox} = 25$nm | $V_{th}$ (V) $T_{ox} = 40$nm |
|------------------|----------|-----------------------------|-----------------------------|
| $1 \times 10^{16}$cm$^{-3}$ | 10       | -1.2644                     | -1.9547                     |
|                  | 45       | -0.2756                     | -0.441                      |
|                  | 60       | -0.2167                     | -0.3348                     |
|                  | 90       | -0.1378                     | -0.2425                     |
|                  | 130      | -0.0854                     | -0.1527                     |

Figure 4. Changing of $V_{th}$ against $L$ with varying $T_{ox}$

Referring to Figure 4, the trend of $V_{th}$ is almost similar with the trend shown in Figure 3. In general, as $L$ becomes smaller, the value of $V_{th}$ reduces significantly. It is also observed that the $V_{th}$ falls with the increasing of $T_{ox}$. This observation suggests that as the $T_{ox}$ increases, the gate control over the channel diminishes leading to an increase of short channel effects towards the $V_{th}$.

3.3. $V_{th}$ against $L$ with varying $T_{ox}$

The values of each parameter that used for simulation were recorded in Table 3 and the associated graph is shown in Figure 5.

Table 3. Values of $V_{th}$ for different $N_a$ and $L$

| $T_{ox}$ (nm) | $N_a$ (cm$^{-3}$) | $V_{th}$ (V) $L = 45$nm | $V_{th}$ (V) $L = 60$nm |
|--------------|------------------|-------------------------|-------------------------|
| 25           | $1.4 \times 10^{15}$ | 0.276                   | 0.260                   |
|              | $4.0 \times 10^{15}$ | 0.314                   | 0.274                   |
|              | $1.0 \times 10^{16}$ | 0.308                   | 0.271                   |
|              | $2.0 \times 10^{16}$ | 0.288                   | 0.262                   |
|              | $1.0 \times 10^{17}$ | 0.168                   | 0.149                   |
In Figure 5, it is observed that the $V_{th}$ increases a bit before drops significantly as $N_a$ increases. For $L = 45$ nm, the increment of $V_{th}$ is notable when $N_a$ is between $10^{15}$ and $10^{16}$ before it decreases as $N_a$ increases to $10^{17}$. For $L = 60$ nm, $V_{th}$ is almost unchanged when $N_a$ is between $10^{15}$ and $10^{16}$ and starts to decrease as $N_a$ increases to $10^{17}$. The decrement of $V_{th}$ is due to the higher number of free carriers as the number of dopant increases. These carriers are contributing to higher possibility of drive current to exist in the transistor channel.

3.4. $V_{th}$ against $L$ with varying $T_{ox}$

The values of each parameter that used for simulation were recorded in Table 4 and the associated graph is shown in Figure 6.

| $T_{ox}$ (nm) | $N_a$ (cm$^{-3}$) | $V_{th}$ (V) | $T_{ox}$= 25nm | $T_{ox}$= 40nm |
|--------------|------------------|-------------|---------------|---------------|
| 60           | $1.4 \times 10^{15}$ | 0.276       | 0.260         |
|              | $4.0 \times 10^{15}$ | 0.314       | 0.274         |
|              | $1.0 \times 10^{16}$ | 0.308       | 0.271         |
|              | $2.0 \times 10^{16}$ | 0.288       | 0.262         |
|              | $1.0 \times 10^{17}$ | 0.168       | 0.149         |
Figure 6 illustrates the curve of $V_{th}$ as the $T_{ox}$ changes from 25nm to 40nm. Observation in Figure 6 shows that as the $N_a$ increases, the $V_{th}$ decreases for both cases of $T_{ox}$ values. In both cases of $T_{ox}$, $V_{th}$ is almost flat when $N_a$ is between $10^{15}$ and $10^{16}$ before it drops significantly as $N_a$ increases to $10^{17}$. This observation suggests that as $N_a$ increases, so too the number of free carriers in the channel. As free carriers flooding the channel, the potential barrier will lower and thus drive current will starts to flow in the channel.

3.5. $V_{th}$ against $T_{ox}$ with Varying $N_a$

The values of each parameter that used for simulation were recorded in Table 5 and the associated graph is shown in Figure 7.

| $L$ (nm) | $T_{ox}$ (nm) | $V_{th}$ (V) $N_a = 1 \times 10^{16}$cm$^{-3}$ | $V_{th}$ (V) $N_a = 2 \times 10^{16}$cm$^{-3}$ |
|---------|-------------|---------------------------------------------|---------------------------------------------|
| 60      | 10          | -0.015                                      | -0.149                                      |
|         | 25          | -0.02                                       | -0.201                                      |
|         | 40          | -0.071                                      | -0.216                                      |
|         | 50          | -0.12                                       | -0.275                                      |
|         | 65          | -0.157                                      | -0.333                                      |
Figure 7. Changing of $V_{th}$ for different $T_{ox}$ and $N_a$

Figure 7 depicts the trend $V_{th}$ change against $T_{ox}$. It is observed that the $V_{th}$ decreases as the $T_{ox}$ increases. Since $T_{ox}$ is inversely proportional to the $V_{th}$, therefore the oxide capacitance will increase as $T_{ox}$ decreases. It is also noted that the $V_{th}$ drops more than double as $T_{ox}$ increases by 50nm. This shows strong effect of $T_{ox}$ over $V_{th}$ in the presence of SCE in NMOS transistor.

4. Conclusion

In this work, modelling of SCE has been carried out and investigation of SCE over the transistor performance is presented. The transistor performance is benchmarked at $V_{th}$ and simulated against three parameters; L, $N_a$, and $T_{ox}$. Observation on simulation results show that the $V_{th}$ is directly proportional to L and inversely proportional to both $N_a$ and $T_{ox}$. The presence of SCE in 60nm transistor shows the $V_{th}$ is highly dependent on those three parameters; L, $N_a$, and $T_{ox}$. Improvement in device performance, as suggested by the simulation results, can be achieved by increasing the channel length, and reducing both the $N_a$ and $T_{ox}$ beneath the gate terminal.

5. References

[1] Olukotun, K 2016 Scaling data analytics with moore's law in 2016 International Conference on Parallel Architecture and Compilation Techniques (PACT)
[2] Yeric, G 2015 Moore's law at 50: Are we planning for retirement? in 2015 IEEE International Electron Devices Meeting (IEDM)
[3] Oates, A S 2014 Will reliability limit Moore's law? in Proceedings of Technical Program - 2014 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)
[4] Sutardja, S 2014 Slowing of Moore's law signals the beginning of smart everything in 2014 44th European Solid State Device Research Conference (ESSDERC)
[5] Taur, Y 1999 CMOS scaling beyond 0.1 µm: how far can it go? in 1999 International Symposium on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers. (Cat. No.99TH8453)
[6] Kaul, H, Anders, M, Hsu, S, Agarwal, A, Krishnamurthy, R and Borkar, S 2012 Near-threshold voltage (NTV) design: opportunities and challenges in DAC Design Automation Conference 2012
[7] Ryu, M and Kim, Y 2014 Analysis of structural variation and threshold voltage modulation in 10-nm double gate-all-around (DGAA) transistor in 2014 International SoC Design Conference (ISOCC)
[8] Rezali, F A M, Hatta, S F W M and Soin, N 2015 Scaling impact on design performance metric of sub-micron CMOS devices incorporated with halo in 2015 IEEE Regional Symposium on Micro and Nanoelectronics (RSM)

[9] Manohari, M R, Pandian, M K and Balamurugan, N B 2013 Performance analysis and threshold voltage modeling of Surrounding Gate Silicon Nanowire Transistors in 2013 International Conference on Emerging Trends in VLSI, Embedded System, Nano Electronics and Telecommunication System (ICEVENT)

[10] Shur, M 2012 Ballistic transport in short channel field effect transistors in 2012 8th International Caribbean Conference on Devices, Circuits and Systems (ICCDCS)

[11] Chopade, S S and Padole, D V 2014 Design of Double Gate MOSFET and FDSOI using high k material for nano scaled Circuits in TENCON 2014 - 2014 IEEE Region 10 Conference

[12] Sarkhel, S, Bagga, N and Sarkar, S K 2015 Analytical modeling and simulation of Work Function Engineered gate junctionless high-k dielectric Double Gate MOSFET: A comparative study in Michael Faraday IET International Summit 2015

[13] Srivastava, V M 2015 Design optimization of high-k dielectric based double-gate MOSFET and it's performance in 2015 Annual IEEE India Conference (INDICON)

[14] Keunwoo, K, Fossum, J G and Ching-Te, C 2003 Physical compact model for threshold voltage in short-channel double-gate devices in International Conference on Simulation of Semiconductor Processes and Devices, 2003. SISPAD 2003.

[15] Liu, F, Ionica, I, Bawedin, M and Cristoloveanu, S 2015 A simple compact model for carrier distribution and its application in single-, double- and triple-gate junctionless transistors in EUROSOI-ULIS 2015: 2015 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon

[16] Razavi, P and Orouji, A A 2008 Dual material gate oxide stack symmetric double gate MOSFET: Improving short channel effects of nanoscale double gate MOSFET in 2008 11th International Biennial Baltic Electronics Conference

[17] Riyadi, M A 2013 Performance comparison of asymmetric drain/source topology in nanoscale Double Gate vertical MOSFET in 2013 International Conference on Information Technology and Electrical Engineering (ICITEE)

[18] Riyadi, M A, Darjat, Prakoso, T and Suseno, J E 2015 The depletion influence on the non-planar vertical MOSFET threshold voltage in 2015 2nd International Conference on Information Technology, Computer, and Electrical Engineering (ICITACEE)

[19] Hu, C 2013 Compact modeling for the changing transistor in 2013 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)

[20] Hiblot, G, Rafhay, Q, Boeuf, F and Ghibaudo, G 2014 Impact of quantum modulation of the inversion charge in the MOSFET subthreshold regime in 2014 44th European Solid State Device Research Conference (ESSDERC)

[21] Shujuan, Y 2015 The compact Vth model for biaxial strained Si NMOSFET in 2015 IEEE 11th International Conference on ASIC (ASICON)