Deep Neural Network Augmented Wireless Channel Estimation on System on Chip

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Abstract—Reliable and fast channel estimation is crucial for next-generation wireless networks supporting a wide range of vehicular and low-latency services. Recently, deep learning (DL) based channel estimation is being explored as an efficient alternative to conventional least-square (LS) and linear minimum mean square error (LMMSE) based channel estimation. Unlike LMMSE, DL methods do not need prior knowledge of channel statistics. Most of these approaches have not been realized on system-on-chip (SoC), and preliminary study shows that their complexity exceeds the complexity of the entire physical layer (PHY). The high latency of DL is another concern. This paper considers the design and implementation of deep neural network (DNN) augmented LS-based channel estimation (LSDNN) on Zynq multi-processor SoC (ZMPSoC). We demonstrate the gain in performance compared to the conventional LS and LMMSE channel estimation schemes. Via software-hardware co-design, word-length optimization, and reconfigurable architectures, we demonstrate the superiority of the LSDNN architecture over the LS and LMMSE for a wide range of SNR, number of pilots, preamble types, and wireless channels. Further, we evaluate the performance, power, and area (PPA) of the LS and LSDNN application-specific integrated circuit (ASIC) implementations in 45 nm technology. We demonstrate that the word-length optimization can substantially improve PPA for the proposed architecture in ASIC implementations.

Index Terms—Channel estimation, Deep learning, Least-square, Linear minimum mean square error, System on chip, FPGA, ASIC, hardware software co-design

I. INTRODUCTION

Accurate channel state information estimation is crucial for reliable wireless networks [1]–[4]. Conventional least square (LS) based channel estimation is widely used in long-term evolution (LTE) and WiFi networks due to its low complexity and latency. However, it performs poorly at a low signal-to-noise ratio (SNR) [5]. Other techniques like linear minimum mean square error (LMMSE) offer better performance than LS but need prior knowledge of noise, and second-order channel statistics [6]. Furthermore, it is computationally intensive [6], [7]. The limited sub-6 GHz spectrum has led to the coexistence of heterogeneous devices with limited guard bands. This has resulted in poor SNR due to high noise floor and adjacent-channel interference. This has led to significant interest in improving the performance of the conventional LS and LMMSE channel estimation approaches [8] [9]. With the integration of vehicular and wireless networks, the radio environment has become increasingly dynamic, posing serious challenges in establishing reliable communication links. Furthermore, high-speed ultra-reliable services demand ultra-low latency of the order of milliseconds [10].

Recent advances in artificial intelligence, machine and deep learning (AI-MDL) have been explored to improve the performance of wireless physical layer such as channel estimation, symbol recovery, link adaptation, localization, etc. [11]–[19]. Various studies have shown that data-driven AI-MDL approaches have potential to significantly improve the performance and offer increased robustness towards imperfections, non-linearity, and dynamic nature of the wireless environment and radio front-end [10], [20]–[23]. In the June 2021 3GPP workshop, various industry leaders presented the framework for the evolution of intelligent and reconfigurable wireless physical layer (PHY), emphasizing the commercial potential of the AI-MDL based academic research in the wireless domain. Though intelligent and reconfigurable PHY may take a few years to get accepted commercially, some of these initiatives are expected to be included in the upcoming 3GPP Rel-18.

Few works have replaced the LS, and LMMSE channel estimation with computationally complex deep learning (DL) architectures [24]–[28]. However, most existing works have not been realized on system-on-chip (SoC). In this context, this work focuses on improving the performance of the channel estimation in wireless PHY, where we design and implement deep neural network (DNN) augmented LS estimation (LSDNN) on Xilinx ZCU111 from Zynq multi-processor SoC (ZMPSoC) family comprising of qual-core ARM Cortex A53 processor and ultra-scale field-programmable gate array (FPGA). Compared to existing works, we augment the LS with a Fully Connected Feedforward DNN instead of replacing it with computationally intensive DL networks. We demonstrate the performance gain over the conventional LS and LMMSE approaches. We provide an extensive study of the effects of training SNR on the performance of the LSDNN channel estimation.

Through software-hardware co-design, word-length optimization, and reconfigurable architectures, we demonstrate the superiority of the proposed LSDNN architecture over LS and LMMSE architectures for a wide range of SNRs, number of pilots, preamble types, and wireless channels. Experimental results show that the proposed LSDNN architecture offers lower complexity and a huge improvement in latency over the LMMSE. Next, we evaluate the performance, power, and area (PPA) of the LS and LSDNN on application-specific integrated circuit (ASIC) implementations in 45 nm technology. We demonstrate that the word-length optimization can substantially improve PPA for the proposed architecture in ASIC implementations. The AXI-compatible hardware IPs and ZYNQ-based graphical user interface (GUI) demonstrating the real-time performance comparison on the ZMPSoC are physical deliverables of this work. Please refer to [29] for

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source codes, datasets, and hardware files used in this work. The rest of the paper is organized as follows. Section II reviews the work related to applications of AI-MDL approaches for wireless PHY. In Section III, we present the system model and introduce LS, and LMMSE-based channel estimation approaches. The proposed LSDNN algorithm and simulation results comparing the performance of LS, LMMSE, and LSDNN are given in Section IV followed by their architectures in Section V. The functional performance and complexity results of fixed-point architectures are analyzed in Section VI. The ASIC implementation and results are presented in Section VII. Section ?? concludes the paper along with directions for future works.

**Notations:** Throughout the paper, vectors are defined with lowercase bold symbols \( \mathbf{x} \) whose \( k \)-th element is \( x[k] \). Matrices are written as uppercase bold symbols \( \mathbf{X} \).

### II. Literature Review: DL in Wireless PHY

Various studies and experiments have demonstrated that conventional frameworks such as Shannon theory [30], detection theory [31], and queuing theory [32] based wireless PHY suffer from performance degradation due to randomness and diversity of wireless environments. Instead of exploring approximate frameworks, recent advances in AI-MDL approaches and their ability to address hard-to-model problems offer a good alternative for making the wireless PHY robust [33] [34]. Numerous works have shown that traditional ML techniques have been successful in combating complex wireless environments and hardware non-linearities [21]. However, they need manual feature selection. The DL approaches offer the capability to extract features from the data itself, thereby eliminating the need for manual feature extraction. This has lead to numerous AI-MDL based approaches for various problems such as modulation classification [35], [36], direction-of-arrival estimation [37] [38], spectrum sensing [39], multiple-input multiple-output (MIMO) high-resolution channel feedback [40] [41], mobility and beam management [42], link adaptation [18], localization [19]. With the evolution of heterogeneous large-scale networks, existing frameworks suffer from scaling issues due to the high cost of exhaustive searching and iterative heuristic algorithms [43] [44]. Such scaling issues can be handled more efficiently using AI-MDL approaches [45] [46]. To bring DL-aided intelligent and reconfigurable wireless PHY into reality, issues such as potential use cases, achievable gain and complexity trade-off, evaluation methodologies, dataset availability, and standard compatibility impact need to be addressed [10], [20]–[23].

The DL-based PHY can be categorized in two approaches: 1) Complete transmitter and receiver are replaced with respective DL architectures [27], [47]–[49] 2) Independent DL blocks for each sub-block or combination of sub-blocks in PHY [24]–[26], [28], [36], [48]. The drawback of the first approach is that it may not provide intermediate outputs such as channel status indicator, precoding, and channel rank feedback, making them incompatible with existing standards. Furthermore, existing works cannot support high throughput requirements. In this paper, we focus on the second approach addressing the channel estimation task in wireless PHY.

ChannelNet [25] treats the LS estimated values at pilot sub-carriers in an OFDM frame as a low-resolution 2D image and develops a CNN-based image enhancement technique to increase the resolution to obtain accurate channel estimates at data sub-carriers. Its performance is sensitive to the SNR conditions, which demand SNR-specific models resulting in high reconfigurable time and large on-chip memory. This model is further enhanced [26] by replacing the two CNN models with a single deep residual neural network (ReEsNet) to reduce its complexity and improve performance. Interpolation-ResNet in [48] replaces the transposed convolution layer of ReEsNet with a bilinear interpolation block to reduce the complexity further and make the network flexible for any pilot pattern. The computational complexity and memory requirements of these models are high, even higher than the complexity of PHY. In this work, we focus on augmenting the conventional channel estimation with DL instead of DL-based channel estimation [49], [50].

The validation on synthetic datasets is another concern in DL-based approaches. This has been addressed in some of the recent works, such as [28] where DL-based channel estimation is performed using real radio signals, demonstrating the feasibility in practical deployment. This works provides a detailed process and addresses the concerns regarding dataset creation from the RF environment and training and testing the models using real radio signals. The authors in [47] used the concept of transfer learning in [51] to devise a two-phase training strategy to train a DL-based PHY using real-world signals and demonstrated over-the-air communication. It offered similar performance as conventional PHY validating the feasibility of DL-based approaches in a real-radio environment. However, limited efforts have been made on hardware realization of the DL-based wireless PHY [52]–[54]. Hence, there is limited knowledge of their performance on fixed-point hardware, latency, and computation complexity. The impact of the hardware-specific constraints such as high cost and area of on-chip memory and a limited number of memory ports on the training approaches have not been highlighted in the literature yet. The work presented in this paper addresses these issues and offers innovative solutions at algorithm and architecture levels for channel estimation in wireless PHY.

### III. System Model

This paper considers orthogonal frequency-division multiplexing (OFDM) based transceivers with frame structure based on IEEE 802.11p standard shown in Fig. 1. The transmitted frame consists of a preamble header including ten short training sequences and two long training symbols (LTS), followed by the signal and data fields. The LTS consists of predefined fixed symbols known to both transmitter and receiver and used for channel estimation at the beginning of the frame. There are total \( K = 64 \) sub-carriers with the sub-carrier spacing of 156.25 KHz, and the corresponding transmission bandwidth is 10 MHz. Each LTS consists of 64 sub-carriers in a single OFDM symbol, of which 12 are NULL sub-carriers, and 52 are sub-carriers carrying BPSK modulated preamble sequence. Each data symbol carries 48 data and 4 pilot sub-carriers. In this work, we assume that the channel is static over the course of frame transmission, and hence, only the preamble-based channel estimated is discussed.

The block diagram of the IEEE 802.11p PHY transceiver is shown in Fig. 2. The data to be transmitted is modulated using an appropriate modulation scheme such as QPSK/QAM, followed by sub-carrier mapping. The set of 64 sub-carriers is passed through OFDM waveform modulation comprising IFFT and cyclic prefix addition. The length of cyclic prefix
is $K_{cp} = 16$. The scheduler inserts the preamble OFDM symbols at the beginning of each frame, comprising a certain number of data symbols. Next, the complete OFDM frame is transmitted through the wireless channel. At the receiver, OFDM symbols containing the LTS preamble are detected and extracted, followed by OFDM demodulation. Then, channel estimation and equalization operations are performed.

The frequency-domain input-output relation between the transmitted and the received OFDM frame at the receiver can be expressed as follows

$$Y[k, i] = H[k, i]X[k, i] + V[k, i].$$  

(1)

Here, $X[k, i]$, $H[k, i]$, $Y[k, i]$, and $V[k, i]$ denote the transmitted OFDM frame, the frequency domain channel gain, the received OFDM frame, and the additive white Gaussian noise (AWGN) with zero mean and variance, $N_0$. $k$ and $i$ denote the sub-carrier and OFDM symbol indices within the received frame, respectively.

Recall that the channel estimation is performed once per frame using the received preamble symbols, therefore (1) can be rewritten as

$$Y[k, p] = H[k, p]D[k, p] + V[k, p],$$  

(2)

where $D[k, p] = d_p[k]$ denote the $p$-th predefined transmitted preamble symbol, where $1 \leq p \leq K_p$ and $K_p$ is the total number of the transmitted preamble symbols within the frame.

In this context, the LS channel estimation [6] can be expressed as

$$\hat{H}_{LS}[k, p] = \frac{\sum_{q=1}^{K_p} Y[k, q]}{K_p D[k, p]}.$$  

(3)

The LS estimation is easy to implement in hardware and does not require prior channel and noise information. On the other hand, the LMMSE channel estimation [6] needs prior knowledge of the second order channel and noise statistics. Mathematically, the estimated channel gain at the $k$-th sub-carrier can be expressed as

$$\hat{H}_{LMMSE}[k, p] = R_{pp}^{-1} \left( K N_0 E_p \right)^{-1} \hat{H}_{LS}[k, p].$$  

(4)

where $R_{pp}$ is the channel auto-correlation matrix, and $E_p$ denotes the power per preamble symbol. It can be observed that the LMMSE improves the performance of the LS, and the improvement depends on the prior knowledge of the channel and noise statistics.

IV. DEEP NEURAL NETWORKS BASED CHANNEL ESTIMATION

In this section, we present LSDNN design details and simulation results using floating-point arithmetic comparing various channel estimation approaches.

A. LSDNN based Channel Estimation

Deep Neural Networks (DNN) is a subset of DL that tries to mimic how information is passed among biological neurons. A fully-connected neural network is shown in Fig. 3. It has a layered structure, with each layer feeding to the next layer in a forward direction. The first layer is called an input layer representing the input to the DNN, and the last layer is called an output layer from which the outputs are taken.

The layers between the input layer and output layer are called hidden layers. The output and hidden layers contain parallel processing elements called neurons, which take the inputs from the previous layer and send output to the next layer. A neuron performs the summation of weighted inputs followed by a non-linear activation function, as shown in Fig. 3. These functions include Sigmoid, tanh, ReLU, leaky ReLU [55]. For DNN with $L$ layers, including input and output layers, the output of $j$-th neuron in layer $l$, $1 < l < L$ is given as

$$y_j^l = f^{(l)} \left( \sum_{i=0}^{N_l} (w_{ij}^{l-1} y_i^{l-1}) + b_j^l \right).$$  

(5)
where $N_l$ is the total number of neurons in $l$-th layer, $b^l_j$ is the bias of $j$-th neuron of $l$-th layer, $w_{ij}$ is the weight from $i$-th neuron of $(l-1)$-th layer to $j$-th neuron of $l$-th layer, and $f^{(l)}(\cdot)$ is the activation function of $l$-th layer.

The proposed DNN augmented LS estimation approach processes the output of the LS estimator using the DNN, thereby reducing the effect of noise on LS estimates. The DNN is trained to reduce the loss function $J_{\Omega,h}(\hat{H}, y, \hat{H}_{LS})$ over one long training symbol, where $H$ is the original channel impulse response and $\hat{H}_{LS}$ is the channel estimated using the LS approach. Training is an iterative process where the model parameters are updated using optimization functions to minimize the loss over time. Various optimization functions such as stochastic gradient descent, root mean square prop, and adaptive moment estimation (ADAM) can be used [56].

Hyper-parameters for the DNN architecture is chosen manually. Multiple iterations were performed with different hyper-parameters until the one with the best accuracy and low latency was found. We restricted our search to only a few hidden layers to reduce the complexity of the overall design. For illustrations, we consider two DNN architectures: 1) LSDNN1: DNN with a single hidden layer of size $K_{in}$, and 2) LSDNN2: DNN with two hidden layers of size $2 \times K_{in}$. Each model is trained for 500 epochs with Mean Square Error (MSE) as a loss function and ADAM as an optimizer. Table I summarises the specifications of neural network. After training, the next step is inference, in which a trained DNN model is tested on new data to evaluate its performance. The hardware realizations of DNN focus on accelerating the inference phase.

**B. Simulation Results on Floating Point Arithmetic**

For the system model discussed in Section III, we have used six channel models considering vehicle-to-vehicle (V2V) and roadside-to-vehicle (RTV) environments as discussed in [57]. We have considered two performance metrics: 1) Normalized mean square error (NMSE) and 2) Bit-error-rate (BER) to analyze the performance of channel estimation and wireless PHY, respectively.

In Fig. 4(a), we compare the average NMSE of LS, LMMSE, and LSDNN architectures (LSDNN1 and LSDNN2) for a wide range of SNR, and the corresponding BER results on end-to-end wireless transceiver are shown in Fig. 4(b). We assume Rayleigh fading channel with AWGN. We consider an LSDNN architecture trained on a single SNR referred to as training SNR. Here, the training SNR is selected as 10 dB, and the testing SNR range is from -50 dB to 50 dB. Please refer to Section VI-C for more details on the selection of training SNR.

As shown in Fig. 4, the performance of the conventional LS and LMMSE architectures matches with their analytical results, and the error for the LMMSE estimator is less than that of the LS estimator. It can be observed that the LMMSE improves the performance of the LS, and the improvement depends on the prior knowledge of the channel and noise statistics. When prior channel statistics are not known accurately, the LMMSE performance degrades, and the NMSE becomes worse than LS at high SNR, as shown in Fig. 4. The BER of the LSDNN1 and LSDNN2 are close to that of the ideal channel estimation approach and significantly outperforms the LS and LMMSE at all SNRs. The NMSE performance of the LSDNN improves with the increase in SNR until the training SNR of 10 dB. Even though LSDNN1 has less complexity, it offers superior performance than LSDNN2. The NMSE is also a function of the number of training samples; hence, the dataset should be sufficiently large. Similar results are also observed for different wireless channels and preamble types. Corresponding plots are not included to avoid the repetition of results.

The improved performance of the LSDNN can be attributed to the capability of the DNN to extract channel features and learn a meaningful representation of the given dataset. Specifically, it accurately learns to distinguish between the AWGN noise and the channel gain. The LS estimation does not consider noise, resulting in noisy estimates at low SNRs. As SNR increases, the noise content in the LS estimation reduces, resulting in improved performance. This is evident from Fig. 5 where we have analyzed the plots of estimated channel gain magnitudes at different OFDM sub-carriers for three different SNRs. It can be observed that LSDNN and LMMSE performance is close to ideal channel estimation even at low SNR, with the former better than the latter at all sub-carriers. The erroneous knowledge of channel parameters leads to degradation in LMMSE performance, as shown in Fig. 5. Such prior knowledge is not needed in the LSDNN.

![Fig. 4](image-url) (a) NMSE and (b) BER comparisons of various channel estimation approaches using floating point arithmetic.
Fig. 5: Magnitude plot for channel estimation corresponding to subcarriers in an OFDM symbol for (a) 0dB SNR, (b) 20dB SNR, (c) 45dB SNR.

V. CHANNEL ESTIMATION ON SoC

In this section, we discuss the algorithm to architecture mapping of three channel estimation approaches, LS, LSDNN, and LMMSE, on FPGA (hardware) part of the ZMPSoC. The software implementation of these algorithms on an ARM processor is straightforward, and corresponding results are given in Section VI. We begin with the LSDNN architecture, which includes LS estimation as well.

A. LSDNN Architecture

At the receiver, the LTS samples are extracted from the data obtained after the OFDM demodulation, as shown in Fig. 2. LSDNN uses these symbols for channel estimation, and it involves five tasks: 1) Data extraction, 2) LS-based channel estimation, 2) Pre-processing, 3) DNN, and 4) Post-processing, as shown in Fig. 6. In this section, we present the architectures to accomplish these tasks.

The serial data with complex samples received after OFDM demodulation are extracted with independent real and imaginary parts. For the chosen system model with an OFDM symbol comprising of 52 sub-carriers, the input to LS estimation is a vector with 104 real samples. Another input to LS estimation is a reference LTS sequence of the same size. The LS estimation involves the complex division operation of the received (yp) and reference (xp) versions of the LTS. The complex division can be mathematically expressed as shown below, and the corresponding architecture is shown in Fig. 6.

\[
\hat{H}_{LS} = \frac{y_p}{x_p}
\]

\[
= \frac{x_r \times y_r + x_i \times y_i}{x_r^2 + x_i^2} + \frac{x_r \times y_i - x_i \times y_r}{x_r^2 + x_i^2}
\]

\[
(6)
\]

where \(x_r\), \(x_i\), \(y_r\), and \(y_i\) denote the real and imaginary parts of received and reference versions of the LTS, respectively.

The LS estimation of each sub-carrier requires six real multiplications, one real division, three additions, and one subtraction operation. We have explored various architectures of simultaneous calculation of the LS estimation of multiple sub-carriers by appropriate memory partitioning to have parallel access to data and pipelining to improve the utilization efficiency of hardware resources. Please refer to Section VI for more details. Further optimizations can be carried out depending on the modulation type of the LTS sequence. For instance, the LS estimation of QPSK modulated LTS sequence needs only one complex multiplication operation. In the case of IEEE 802.11p, the LTS and pilot symbols are BPSK modulated. The LS estimation is reduced to choosing either the received complex value or its two’s complement based on whether the LTS is +1 or -1, respectively.

The output of the LS channel estimation is further processed using DNN architecture. Before DNN, pre-processing is needed to normalize the DNN input to have zero mean and unit standard deviation. The estimation of mean and standard deviation during inference is not feasible due to limited on-chip memory and latency constraints. Hence, we use the pre-calculated values of the mean and standard deviation using the training dataset. Similarly, the DNN output is de-normalized so that transmitted data can be demodulated for BER-based performance analysis of the end-to-end transceiver. At the architecture level, pre and post-processing incur additional costs in terms of multipliers and adders, as shown in Fig. 6.

The DNN architecture mainly consists of one or more hidden layers followed by the output layer, and it is based on a fully connected neural network framework. This means each layer consists of multiple processing elements (PE), also referred to as neurons, where each PE in a layer communicates the output to all the PEs in the subsequent layer. There is no communication and dependency between the various PEs of a given layer. Also, the data communications between layers happen only in the forward direction, thereby allowing the parallel realization of all PEs of a layer.

As shown in Eq. 5 and Fig. 6, each PE consists of a multiplier and adder unit to perform element-wise multiplications between outputs of all PEs of the previous layer and layer-specific weights stored in internal memory. In the end, the output is added with the layer-specific bias term. This means each PE needs to store \(N_{l+1}\) weights and one bias value in its memory, where \(N_{l+1}\) is the number of PEs in the previous layer. The output of each layer is stored in memory which is completely partitioned to allow parallel access from the PEs in the subsequent layer. The PE functionality is realized sequentially using the counter and multiplexers. Though the parallel realization of all multiplication and addition operations inside the PE is possible due to memory partitioning at PE output, this significantly increases resource utilization and power consumption. ReLU block is added at the end of each hidden layer to introduce non-linearity. It is a hardware-friendly activation function that replaces the negative PE output with zero. As shown in Fig. 7, the output of the first PE of the previous layer is processed by all PEs in the layer simultaneously, and the output is stored in their respective buffers. Next, the output of the second PE of the previous layer is processed, followed by accumulation with the previous intermediate output in the buffer. This process is repeated until the outputs of all PEs in the previous layer have
LS Estimation per \( M \) sub-carrier.

The LMMSE channel estimation requires prior knowledge of the channel correlation matrix \( R_s \) and SNR in addition to LTS symbols. The LMMSE architecture is shown in Fig. 8 and is based on Eq. 4. In the beginning, \( R_s \) is separated into real and imaginary matrices, and the term \((1/\text{SNR})\) is added with each diagonal element of the real matrix of \( R_s \). Then, the inverse of the \( R_s \) matrix is performed. This is followed by various matrix multiplication and addition operations. We have modified Xilinx’s existing matrix multiplication and matrix inversion reference examples to support the complex number arithmetic since the baseband wireless signal is represented using complex samples. The well-known lower-upper (LU) decomposition method is selected for matrix inversion. We parallelize individual operations like element-wise division and matrix multiplication on the FPGA. Every element in the matrix is parallely processed to compute division, and every row column dot product in matrix multiplication is performed in parallel to speed up the computation. In the end, multiple instances of these IPs are integrated to get the desired LMMSE functionality, as shown in Fig. 8.

C. Hardware Software Co-design and Demonstration

In Fig. 9, various building blocks of the channel estimation tasks such as LS, LMMSE, LSDNN, scheduler, DMA, interrupt, and GUI controller is shown. For illustration, we have shown all channel estimation approaches on the FPGA. To enable this, we have developed AXI-stream compatible hardware IPs and interconnected them with PS via direct-memory access (DMA) in the scatter-gather mode for efficient data transfers. Later in Section VI, we considered various architectures via hardware-software co-design by moving the blocks between ARM Processor and FPGA. We have deployed PYNQ based operating system on the ARM processor, which takes care of various scheduling and controlling operations. It also enables graphical user interface (GUI) development for real-time demonstration. As shown in Fig. 9, GUI allows the user to choose various parameters such as channel estimation schemes, SNRs, and word-length.
VI. PERFORMANCE AND COMPLEXITY ANALYSIS

This section presents the performance analysis of different channel estimation architectures implemented on the ZSoC for a wide range of SNRs, word-length, and wireless parameters such as channels, preamble type, etc. The resource utilization, execution time, and power consumption of various architectures obtained via word length optimization, hardware-software co-design, and reconfigurability are compared. The need for reconfigurable architectures and challenges in training DNN for wireless applications are highlighted at the end.

A. Word Length Impact on Channel Estimation Performance

In Section IV-B, we have analyzed the performance of various channel estimation approaches on floating-point arithmetic in Matlab. To optimize the execution time and resource utilization without compromising the functional accuracy, we have explored the architectures with various WLs and realized them on ZSoC. In Fig. 10(a) and (b), we compare the NMSE and BER performance of the various LSDNN architectures, respectively, for six different WLs along with the single-precision floating point (SPFP) architecture of the LS and double precision floating point (DPFP) architecture of the LMMSE. The architectures with the half-precision floating
point (HPFL) and fixed-point architectures with WL below 24 lead to significant degradation in the NMSE. However, degradation in NMSE may not correspond to degradation in the BER due to data modulation in the wireless transceiver. This is evident from Fig. 10(b), where the architecture with HPFL offers the BER performance as that of the SPFL architecture. On the other hand, the BER of the fixed-point architecture with WL below 24 leads to significant degradation in the performance.

The WL selection is architecture-dependent; hence, the WL for the LS may not be the same as that of LSDNN. Based on the detailed experimental analysis, the LS architecture with fixed-point WL of 18 bits or higher offers the same performance as its SPFL architecture, as shown in Fig 11(a). In the case of LMMSE, fixed-point architecture is not feasible. Even SPFL architecture fails to offer the desired performance, especially at high SNRs; hence, DPFL is needed. Further analysis revealed that only the matrix inverse sub-block needs DPFL WL while the rest of the sub-blocks can be realized in SPFL WL as shown in Fig. 11(b). Such analysis highlights the importance of experiments on the SoC for different WL since such results can not be obtained using simulations.

B. Resource, Power and Execution Time Comparison

In this section, we compare the resource utilization, execution time, and power consumption of various architectures on the ZSoC platform. In Table II, we consider three different WL architectures of the LS and LMMSE and six different WL architectures of the LSDNN. It is assumed that the complete architecture is realized in the FPGA (PL) part of the SoC. The execution time of the LS architecture is the lowest, while the execution time of the LMMSE architecture is the highest. The execution time of the LSDNN is significantly lower than that of LMMSE and is around 1.5-2 times that of the LS architecture. Similarly, resource utilization and power consumption of the LSDNN are higher than that of the LS. This is the penalty paid to gain significant improvement in channel estimation performance. However, the LSDNN offers a significantly lower execution time than the LMMSE, and resource utilization is also lower, especially in terms of BRAM and DSP units which are limited in numbers on FPGA. The use of fixed-point architectures leads to significant improvement in all three parameters. In case of LSDNN, we also considered two additional architectures: 1) Serial-parallel architecture where 2 PEs share the same hardware resources, and 2) Fully serial architecture where all PEs share the same hardware resources. As we move from a completely parallel architecture to these two architectures, we can gain significant savings in the number of resources, especially DSPs. However, the execution time increases, which is still significantly lower than the LMMSE. Further improvement is possible if the input data type of the architecture is changed to fixed-point so that fixed-to-floating point conversion overhead at the input and output can be removed.

Next, we consider various LSDNN architectures obtained via hardware-software co-design. For this purpose, LSDNN is divided into three blocks – LS (B1), normalization and

![Fig. 11: NMSE Comparison of various WL architectures of (a) LS and (b) LMMSE on the ZSoC.](image)

**TABLE II:** Resource utilization and latency comparison of LS, LMMSE, and DNN-Augmented LS channel estimation for different word length implementations.

| Sr. No | Architectures | Word Length | Execution time (ms) | BRAMs | DSPs | LUTs | FFs | PL Power (W) | SoC Power (W) |
|--------|---------------|-------------|---------------------|-------|------|------|----|-------------|--------------|
| 1      | LS            | FP (18,9)   | 0.0155              | 7     | 24   | 14665| 16649| 0.373       | 1.969        |
| 2      | LS            | FP (18)     | 0.0133              | 14    | 96   | 14721| 15094| 0.438       | 1.969        |
| 3      | MMSE          |             |                     |       |      |      |     |             |              |
| 4      | MMSE          | DPFL        | 248.41              | 191.5 | 522  | 44444| 43485| 1.158       | 2.669        |
| 5      | MMSE          | SPFL        | 214.7               | 99.5  | 194  | 24249| 24778| 0.621       | 2.152        |
| 6      | MMSE          | DPFL INV-SP | 219.75              | 139.5 | 338  | 36225| 34898| 0.918       | 2.449        |
| 7      | LSDNN         |             |                     |       |      |      |     |             |              |
| 8      | LSDNN         | SPFL        | 0.0266              | 88    | 322  | 62895| 58064| 1.078       | 2.138        |
| 9      | LSDNN         | HPFL        | 0.0298              | 32    | 260  | 30436| 32866| 0.569       | 2.138        |
| 10     | LSDNN         | FP (32,8)   | 0.0186              | 88    | 520  | 157130| 151544| 2.46       | 4.029        |
| 11     | LSDNN         | FP (24,8)   | 0.0179              | 91    | 260  | 85155| 82221| 1.318       | 2.849        |
| 12     | LSDNN         | FP (24,8)   | 0.236               | 22.5  | 17   | 15450| 16025| 0.373       | 1.904        |

**TABLE III:** Execution times for different Hw/Sw codesign approaches for DNN Augmented LS Estimation.

| Sr. No | Blocks in PS | Blocks in PL | Execution time (us) | Acceleration factor | BRAM | DSP | LUT | FF | PL Power(W) | SoC Power (W) |
|--------|--------------|--------------|---------------------|---------------------|------|-----|-----|----|-------------|--------------|
| 1      | B1,B2,B3     | NA           | 558                 | 1                   | 80   | 130 | 26622| 25807| 0.453       | 2.021        |
| 2      | B1,B2        | B3           | 49                  | 11                  | 82   | 130 | 26456| 28136| 0.453       | 2.022        |
| 3      | B1           | B2,B3        | 30                  | 18                  | 88   | 322 | 62895| 58064| 1.078       | 2.647        |
| 4      | NA           | B1,B2,B3     | 26                  | 21                  | 88   | 322 | 62895| 58064| 1.078       | 2.647        |
denormalization (B2), and DNN (B3). In Table III, we consider four architectures: 1) B1, B2, B3 in PS, 2) B1, B2 in PS, and B3 in PL, 3) B1 in PS, and B2, B3 in PL, and 4) B1, B2, B3 in PL. (Same as Table II). Moving DNN to PL gives 11x improvement in execution time with respect to PS implementation as FPGA can exploit inherent parallelism in DNNs, as explained in section V-A, to speed up the processing. Normalization and denormalization can also be performed in parallel as there is no data dependency for these operations and thus can be accelerated by moving to PL. Execution time can further be reduced by moving LS to PL and processing multiple subcarriers in parallel, thus achieving an overall acceleration factor of 21x when all the data processing blocks are implemented in PL compared to complete PS implementation. Reducing execution time by moving blocks to PL and introducing parallelism increases the FPGA fabric’s resource utilization and power consumption. Thus, when choosing a particular architecture, there is a trade-off between latency and resource utilization/power consumption.

With the evolution of wireless networks, the transmission bandwidth and hence, the FFT size of the OFDM PHY is also increasing. The increase in FFT size leads to an increase in the complexity of the channel estimation architecture, which in turn demands efficient acceleration via FPGA on the SoC. In Table IV, we compare the effect on execution time and corresponding acceleration factor for different FFT sizes. It can be observed that the gain in acceleration factor increases with the increase in the FFT size mainly due to more opportunities for parallel arithmetic operations. Thus, LSDNN architecture has the potential to offer a significant improvement in performance and execution time for next-generation wireless PHY.

C. Effect of Training SNR

For the results presented till now, the LSDNN model is obtained using the training SNR of 10 dB. Training a DNN on a single SNR allows it to converge faster and model the channel better as the DNN does not have to encounter multiple noise distributions during the training phase, thus reducing training complexity. However, faster training should not compromise the functional performance of the LSDNN. For in-depth performance analysis, we analyze the effect of training SNR on the performance of the LSDNN model.

We initially consider various architectures of the LSDNN model trained using the dataset comprising all SNR samples ranging from -50 dB to 50 dB. As shown in Fig.12, the NMSE and BER performance is poor due to the reasons mentioned before. However, the selection of training SNR is not trivial since optimal training SNR may vary depending on the testing SNR, i.e., the deployment environment. For instance, as shown in Fig. 13 (a) and (b), single training SNR affects the performance of LSDNN considerably, especially at high testing SNRs. To address this issue, we consider the selection of training SNR based on the testing SNR range, and corresponding results are shown in Fig. 14. It shows the NMSE for different testing SNRs plotted against the selected training SNR. For each testing SNR, the NMSE first decreases as the training dataset SNR is increased till it reaches its minimum value and then starts increasing. The best training SNR is where the NMSE is minimum, e.g., for the testing SNR range of 0 dB - 20dB, the lowest NMSE corresponds to a training SNR of 10dB. Similarly, for testing SNR of -10 dB to 10 dB, the optimal training SNR is 0 dB. Note that

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**TABLE IV: Resource utilization and latency comparison of LSDNN for wireless PHY with different FFT size**

| Sr. No | FFT Size | Execution time (us) | Acceleration factor | BRAM | DSP | LUT | FF | PL Power(W) | SoC Power (W) |
|--------|----------|---------------------|---------------------|------|-----|-----|----|-------------|---------------|
| 1      | 64       | 26                  | 21                  | 88   | 322 | 62895 | 58064 | 1.078       | 2.647         |
| 2      | 128      | 48                  | 28                  | 195  | 512 | 83193 | 80679 | 1.474       | 3.005         |
| 3      | 256      | 85                  | 31                  | 339  | 832 | 119043 | 118606 | 2.206       | 3.737         |

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**Fig. 12:** BER performance of the LSDNN architecture trained with dataset containing samples from complete SNR range of -50dB to 50dB.

**Fig. 13:** (a) NMSE and (b) BER comparisons of various LSDNN architectures trained on different training SNRs.
training SNR is irrelevant at low SNRs due to the significant impact of noise on the received signal, and DNN is unable to learn the channel properties, resulting in high NMSE and BER. Such dependence on the testing SNR demands reconfigurable architecture that can switch between various LSDNN models depending on the given testing SNR range. Such architecture is presented in the next section.

D. Reconfigurable Architecture

Though the LSDNN approach offers better performance than LMMSE without the need of prior channel knowledge, LSDNN performance depends on the efficacy of the training dataset with respect to the validation environment. For instance, the performance of LSDNN may degrade if the parameters such as testing SNR, preamble type, pilot type, etc., of the training and validation environment do not match. For instance, the performance of the LSDNN trained on model M1 degrades significantly on two different models, M2 and M3, as shown in Fig. 15. This is expected because for a DNN to perform satisfactorily, the training and testing conditions should remain the same. To address this challenge, we need a reconfigurable architecture for LSDNN so that an on-the-fly switch between various LSDNN models can be enabled.

We propose a reconfigurable architecture for LSDNN where the parameters of various LSDNN trained models are pre-computed and stored in memory. Thus, the same hardware architecture can be used across multiple testing environments. In Table V, we consider two architectures based on the type of memory on the SoC. In the first architecture, external DRAM is used to store the model parameters, and the parameters of the selected LSDNN models are transferred to the PL via DMA. Such architecture suffers from high reconfiguration and execution time due to external memory. However, on-field reconfigurability is possible since future models can be added in DRAM using PS without needing hardware reconfiguration. In the second approach, all model parameters are stored in the BRAM of the PL, resulting in lower execution and reconfiguration time. Due to limited BRAM, such an approach limits the number of supported models, and adding new models requires FPGA configuration. Note that FPGA reconfiguration can still be done remotely without requiring product recall. As part of future works, the second architecture can be enhanced to optimize BRAM utilization via dynamic partial reconfiguration, thereby making the BRAM utilization independent of the number of models. Such reconfigurable architecture also needs intelligence to detect the change in environment and reconfigure the hardware. The design of intelligent and reconfigurable channel estimation architecture is an important research direction.

### VII. ASIC Implementation

In addition to FPGA, ASIC is another popular hardware platform for wireless PHY. In this section, we assess the PPA delivered by various architectures in the ASIC implementation using 45 nm CMOS technology. First, we synthesize the Verilog code used for FPGA implementation, using suitable constraints, to obtain the gate level netlist. We verify the functional correctness of the design using a combinational equivalence checker and ensure its temporal safety using static timing analysis. The validated gate-level netlist is converted into the final Graphic Data System (GDS) using the physical design steps such as floor-planning, placement, clock-tree synthesis, and routing. Finally, we carry out various sign-off checks on the ASIC implementation using physical verification and timing analysis tools. We report the PPA of the implementations with various channel estimation architectures in

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**Table V: Comparison of various reconfigurable LSDNN architectures**

| Model | External DDR Memory | On-chip BRAM |
|-------|---------------------------------|--------------|
|       | Execution time (ms) | LUT | FF | BRAM | DSP | PL power (W) | SoC power (W) |
| LSDNN M1 | 0.257 | 65926 | 68424 | 70634 | 2.423 | 0.854 | 2.668 | 2.69 |
| LSDNN M2 | 70100 | 63802 | 63802 | 2.69 | 324 | 0.0264 | 0.854 | 2.668 |
| LSDNN M3 | 253.5 | 63814 | 70634 | 2.69 | 324 | 0.029 | 0.854 | 2.69 |

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**Fig. 14:** Comparison of effect of training SNR on the NMSE for various ranges of the testing SNR.

**Fig. 15:** (a) NMSE and (b) BER comparisons of various channel estimation approaches on different models. The LSDNN model is trained on model M1.
Fig. 16: Comparative analysis of PPA in ASIC implementations of channel estimation techniques (Vdd = 1V, technology = 45 nm)

Further, we study the effect of word-length optimizations on the ASIC implementations of different channel estimation techniques. We found that upon word-length optimization of LS from 32 bits to 16 bits, the 18-bits LS achieves 1.5× higher operating frequency compared to 32-bits LS (from 350 MHz to 500 MHz). Moreover, the 18-bits LS takes 3.5× less area and consumes 1.8× less power than the 32-bits LS at their peak operating frequencies. Likewise, upon word-length optimization of LSDNN from 32 bits to 24 bits, the 24-bits LSDNN achieves 1.4× higher operating frequency compared to 32-bits LSDNN (from 200 MHz to 285.7 MHz). Moreover, the 24-bits LSDNN takes 1.8× less area and 1.2× less power compared to the 32-bits LSDNN at their peak operating frequencies. Thus, the word-length optimization delivers PPA improvements in ASIC implementations also, both for the LS and LSDNN architectures.

VIII. CONCLUSIONS AND FUTURE DIRECTIONS

In this work, we proposed a deep neural network (DNN) augmented least-square (LSDNN) based channel estimation for wireless physical layer (PHY). We have compared the performance, resource utilization, power consumption, and execution time of LSDNN with conventional LS and linear minimum mean square estimation (LMMSE) approach on Zynq multiprocessor system-on-chip (ZMPSoC) and application-specific integrated circuits (ASIC) platforms. Numerous experiments validate the superiority of the LSDNN over LS and LMMSE. The AXI-compatible hardware IPs and PYNO-based graphical user interface (GUI) demonstrating the real-time performance comparison on the ZMPSoC are a physical deliverable of this work.

Future works include an extension of the proposed approach for multi-antenna systems and integration with the RFSoC platform for validation in a real-radio environment. We would also like to explore the application of the proposed approach for upcoming standards such as IEEE 802.11 ad/ay/ax, in which reference signals are spread over the data frame.

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