A Comparative Study of Ring Oscillator PUFs Implementation on Different FPGA Families

Muslim Mustapa\(^1\), Mohammed Niamat\(^3\)

\(^1\)Advanced Computing, Center of Excellence (CoE), Universiti Malaysia Perlis (UniMAP), Perlis, Malaysia

\(^2\)Faculty of Electronic Engineering Technology, Universiti Malaysia Perlis (UniMAP), Perlis, Malaysia

\(^3\)Electrical Engineering and Computer Science Department, University of Toledo, Toledo, OH, USA

muslim@unimap.edu.my

Abstract. Physical Unclonable Function (PUF) is an irreversible function that utilizes the process variation which occurs during silicon chip fabrication. The process variation is uncontrollable; thus, it cannot be modeled and is unique for each chip. Ring Oscillator PUF (ROPUF) has been used in the past to enhance the physical security of FPGAs by generating unique IDs which exploit the process variation introduced during the manufacturing process of the FPGA. In this paper, we describe the implementation and analysis of ROPUF on two different Xilinx FPGA families using 28 nm (Artix-7) and 90 nm (Spartan 3E) technologies. In each case, the ROPUF design is evaluated in terms of five parameters, namely, uniqueness, reliability, uniformity, bit aliasing, and diverseness. The reliability is measured based on responses generated from ROPUF at various temperature and voltage settings. The accelerated aging experiment results are also presented in the reliability evaluation. Our results show that the Artix-7 family yields the best results for uniqueness (45.15%) and diverseness (3.88). Based on the experimental results obtained, we suggest the scheme to increase the ROPUF’s reliability on both Spartan 3E and Artix-7 FPGAs by selecting ROs comparison pairs that have high frequency difference. We showed that the ROPUFs security is not been compromised by applying the scheme.

1. Introduction

ROPUF utilizes ring oscillators (ROs) to exploit the process variation inside a silicon chip to generate a unique ID. A typical ROPUF comprises of ring oscillators, multiplexers (MUXs), counters, and a comparator. A ROPUF can generate a binary bit stream (response) from a given input bit stream (challenge). A ROPUF can generate multiple sets of responses from different sets of challenges. A challenge that produces a response is known as a challenge-response pair (CRP).

Earlier studies have shown that ROPUF can be implemented on FPGAs [1][2]. The fact that ROPUF circuits do not need to be symmetric compared to other types of PUFs, such as Arbiter PUF (APUF) and Butterfly PUF (BPUF) that require a stringent symmetric circuit makes the ROPUFs attractive. The only requirement in ROPUF circuit is that the ROs need to be identical, and this can be achieved by creating
a hard macro for the RO and instantiating it as many times as needed. If two ROs are identical then the
difference in the frequencies generated is due to process variation.

FPGA security is a concern among the FPGA manufacturers. FPGAs are prone to several security
issues such as IP protection, cloning, side channel attack and tampering. Xilinx, for example, has
introduced Device DNA as the additional security feature in some of its FPGA [3]. ROPUF can be used
as an additional security feature in FPGAs. Any tampering attempt by hackers will change the unique
parameters of the process variation [2].

Current FPGA families are fabricated using the latest silicon technology which provides smaller
transistor size. Smaller transistors size gives better performance on the FPGA in terms of speed and
power consumption, but in terms of the performance of ROPUF implementation on FPGA, it still needs
to be studied [4]. As the silicon technology shrinks, the process variation parameters will also change
[5]. In this paper, we analyze ROPUF parameters on two different Xilinx FPGA families that use
different silicon technologies; 28 nm technology (Artix 7) and 90 nm technology (Spartan 3E). The main
contributions of our work are:

1) **ROPUF’s comparison on two FPGA families that used different silicon technologies:**
We compare ROPUF’s responses from two different FPGA families in terms of five
parameters; uniqueness, reliability, uniformity, bit aliasing, and diverseness.

2) **Temperature, voltage, and aging effects:** For reliability, we compare the responses
generated at different temperature and voltage settings. We also compare the responses
generated through the accelerated aging experiment.

3) **Scheme to enhance ROPUF reliability:** Based on the experimental results obtained we
propose a scheme that can enhance ROPUF reliability.

The rest of the paper is organized as follows. Section II covers the parameters used to measure
ROPUF. Section III explains the experimental setup. Section IV discusses the results, and finally,
Section V concludes this paper.

### 2. Background

#### 2.1. Ring Oscillator PUF response

Process variation exitance causes delay differences in silicon chip. RO that is mapped at different
locations on FPGA generates two different frequencies: $f_a$ and $f_b$. Those frequencies will be compared
to generate PUF response.

#### 2.2. Number of stages in Ring Oscillator

Based on the results we obtained from the previous experiment, we decided to use 5-stage ROs. The 5-
stage RO is build using one NAND gate and 4 NOT gates as shown in Figure 1.

![Figure1.5-stage RO](image)

#### 2.3. ROPUF parameters

For PUF implementations, different researchers use different parameters have been used in the past
[6][7][8]. In this paper, we use five of the most common parameters. These parameters are uniqueness,
reliability, uniformity, bit-aliasing and diverseness. The uniqueness can be measured by comparing the
Hamming Distance (HD) between responses from different FPGAs in the same family. The equation
used to measure the uniqueness is shown in equation 1:

$$Uniqueness = \frac{2}{m(m-1)} \sum_{u=1}^{m-1} \sum_{v=u+1}^{m} \frac{HD(R_u, R_v)}{n} \times 100\%$$  \hspace{1cm} (1)
where, \( m \) is the number of FPGAs used, \( u \) and \( v \) are the two FPGAs being compared, and \( n \) is the number of responses generated. \( R_u \) and \( R_v \) are the response from the same challenge \( C \) for FPGAs \( u \) and \( v \). HD is the hamming distance between the responses generated from FPGAs \( u \) and \( v \). The higher uniqueness percentage represents the better uniqueness in the response generated from ROPUF. But considering the large number of response bits, a good uniqueness percentage should be around 50%. This means that at least 50% of the responses generated from FPGA \( u \) and \( v \) differ from each other (responses obtained by given the same challenge to FPGA \( u \) and \( v \)).

The reliability can be measured by comparing the response from the same FPGA that is generated under different environmental conditions such as temperature and voltage. The equation used to measure the reliability is shown in equation 2 and 3. \( R_s \) is the response from FPGA \( i \) at normal operating condition (at room temperature and normal operating voltage). \( R_{s,t} \) is \( t \)-th sample of \( R \)'s response from FPGA \( i \) at a different operating condition such as different temperature and voltage settings [9][10][11]. A good reliability value is 100%. As can be seen in Equation 3, if the HD intra is low or zero, then the reliability will be around 100%.

\[
HD \text{ Intra} = \frac{1}{k} \sum_{t=1}^{k} \frac{HD(R_s, R_{s,t})}{n} \times 100\% 
\]

\[
Reliability = 100\% - HD \text{ Intra} 
\]

The uniformity and bit-aliasing parameters can be measured by using Hamming Weights (HWs) as shown in equation 4 and 5 where \( r_{s,l} \) is the \( l \)-th binary bit [12][13][14]. The HW of the response from an FPGA represents the uniformity and the HW of the responses from different FPGAs represents the bit-aliasing. The HW for bit aliasing is measured across the same bit location in responses from different FPGAs. A good value for uniformity and bit aliasing is around 50%, which means the response from RO is well distributed between ‘0’s and ‘1’s.

\[
Uniformity = \frac{1}{n} \sum_{l=1}^{n} r_{s,l} \times 100\% 
\]

\[
Bit - aliasing = \frac{1}{m} \sum_{l=1}^{m} r_{s,l} \times 100\% 
\]

The diverseness of the frequency can be measured by using standard deviation as shown in equation 6, 7 and 8. Diverseness represents the range of the frequency generated from the ROs [15][16][17]. A ROPUF’s diverseness that has a value which is close to 0 shows that the ROs’ frequencies tend to be very close to the ROs’ mean frequency. While a high diverseness shows that the frequencies are spread out over a wider range of values. The advantages of having higher diverseness have been discussed in detail [6]. In equation 6, \( h \) is the number of ROs, \( f_{i,j} \) is frequency for each RO, \( f_{i,j,q} \) is the \( q \)-th frequency sample of the \( j \)-th RO in the \( i \)-th FPGA. \( f_{avg} \) is the average frequency of the ROs on an FPGA.

\[
Diverseness = \sqrt{\frac{1}{h-1} \sum_{j=1}^{h} (f_{i,j} - f_{avg})^2} 
\]

\[
f_{i,j} = \frac{1}{q} \sum_{q=1}^{q} f_{i,j,q} 
\]

\[
f_{avg} = \frac{1}{h} \sum_{j=1}^{h} f_{i,j} 
\]

3. Experimental Setup

There are works that have been done to study ROPUF performance on FPGA. Large scale characterization of ROPUF on Spartan 3E (90 nm silicon technology) FPGAs has been done by [maiti].
They show that the average inter-die hamming distance (HD) for ROPUF is 47.31% and the average intra-die HD is 0.86% at normal operating condition. In this paper, ROPUF performance on 29 Xilinx Spartan 3E and 20 Xilinx Artix-7 FPGAs is analyzed. Test circuitry that runs completely on the FPGA has been developed. The ROs’ frequencies are recorded using Agilent 16801A logic analyzer. The architecture of the design is shown in Figure 2. The explanation details can be referred in our previous work that has been published [6].

The frequency is computed using equation 9 where \( x \) is the cycle counts from each RO and \( y \) is the cycle counts for the 50 MHz reference clock. The preset value for \( y \) is set to 10000 cycles implying that the RO cycles are measured within a 0.2 ms period. The accuracy of the measurement is 0.005 MHz/cycle which is good enough to measure the differences between frequencies generated from ROs.

\[
x \times \frac{50}{y}
\]  

(9)

For the accelerated aging experiment on Spartan 3E and Artix-7 FPGAs, each RO is activated every 64 ms and 107.5 ms respectively. Each activation will turn the RO on for a time period of 0.4 ms. Therefore, each RO is activated 1.3 million times a day for Spartan 3E and 0.8 million times a day for Artix-7. This aging experiment is conducted for 30 days. The number of ROs mapped on Spartan 3E and Artix-7 is 120 and 171 respectively. ROs are numbered according to the location they are mapped as shown in Figure 3. Responses are generated by using a chain-like neighbor coding where RO(n) is compared with RO(n+1). In total, there are 119 response bits generated from 120 ROs for Spartan 3E and 170 response bits are generated from 171 ROs for Artix-7.

4. Results and analysis
ROs are mapped on all the CLBs available on the Spartan 3E FPGAs, and on half of the CLBs available on Artix-7 to record the frequencies. Responses are generated from the frequencies recorded. Chain-like neighbor coding technique is used to select the RO comparison pair [2]. The equation used to generate the response is shown in equation 10. Table 1 shows the uniqueness, uniformity, bit aliasing, diverseness, and reliability results for both FPGA families used in this experiment.
Response bit = \begin{cases} 
1 & \text{if } f_a > f_b \\
0 & \text{otherwise}
\end{cases}  \quad (10)

Table 1. ROPUF’s Parameters Comparison

| Parameter          | Spartan 3E (90nm) | Artix-7 (28nm) |
|--------------------|-------------------|----------------|
| Uniqueness (%)     | 39.79             | 45.15          |
| Uniformity (%)     | 51.25             | 50.17          |
| Bit aliasing (%)   | 50.54             | 50.17          |
| Diverseness        | 2.09              | 3.88           |
| Reliability (%)    | 96.34             | 97.28          |

4.1. ROPUF Uniqueness

ROPUF responses on Artix-7 have the highest uniqueness percentage (45.16%) compared to Spartan 3E (39.79%). Each response from Artix-7 and Spartan 3E contains 780 bits and 239 bits, respectively. The Artix-7 used in this experiment has 101,440 logic cells compared to the Spartan 3E that has 2160 cells. Thus, Spartan 3E has a limited resource compared to Artix-7. The maximum number of ROs that can be mapped on Spartan 3E is 240. Artix-7 uniqueness is shown to be closer to the ideal uniqueness value 50%. Spartan 3E uniqueness seems to be a little bit far from the ideal uniqueness value.

Figure 4 shows three-dimensional graphs of RO’s frequency versus RO’s location for Spartan 3E and Artix-7. These graphs are plotted to better understand the uniqueness difference in ROPUF responses between these two FPGA families. Figure 4 (i) shows ROs’ frequencies from three Spartan 3E FPGAs. The dark blue blocks are the inaccessible area on the FPGA. It can be observed that ROs with high frequency are mostly distributed in the red circle. The same observation is found throughout 29 Spartan 3E FPGAs where most of the ROs with high frequency are in the middle of the FPGA. Figure 4 (ii) shows ROs’ frequencies for the three Artix-7 FPGAs. In Figure 4 (ii), (a) and (b), it can be observed that most of the ROs with high frequency are in the top part of the FPGAs. But this same observation is not found in the 20 Artix-7 FPGAs.

![Figure 4](image-url)
The observation of ROs with high frequency distributed on the same FPGA location throughout the Spartan 3E FPGAs used in this experiment simulates the effect of systematic variation. There are two types of process variation: systematic and stochastic variation [4]. The systematic variation is usually caused by the mask, lithographic, and reticle stepper errors. Systematic variation has high correlation on all ICs that are manufactured on the same line. The stochastic variation is caused by the vibrations during lithography, wafer unevenness and non-uniformity in resist thickness. Stochastic variation possesses more random characteristics, which will be different from each chip [4]. Stochastic variation’s effect can be observed when there is a random high and low ROs’ frequencies distribution. On the contrary, systematic variation’s effect can be observed when there is a certain pattern of high or low ROs’ frequencies distribution in a group of FPGAs. ROPUF’s responses uniqueness decreases due to the systematic variation on FPGAs. Response bits generated from ROs located in an area that affected by systematic variation tend to be the same.

4.2. ROPUF Uniformity
For uniformity, the Spartan 3E and Artix-7 FPGAs have good uniformity percentages (51.25% and 50.17%) which represent a good balance between bits ‘1’ and ‘0’ in the responses. The uniformity result shows that the ROPUF carry the randomness feature in the response within the FPGA regardless of the change in the silicon technologies used. This result also shows that the systematic variation effect that observed in the Spartan 3E FPGAs does not affect the ROPUF’s responses uniformity.

4.3. ROPUF Bit aliasing
The bit aliasing percentages for Spartan 3E (50.54%) and Artix-7 (50.17%) FPGAs are close to the ideal value of 50%. These results represent that there is a balance in the bits ‘1’ and ‘0’ composition across the same bit location in the responses from different FPGAs. The ROPUF responses are observed to carry the randomness feature between the FGPAs in the same family regardless of the change in the silicon technologies used.

4.4. ROPUF Diverseness
The Artix-7 has the highest ROPUF’s diverseness value, 3.89, which represents the high gap between the maximum and minimum frequencies. High diverseness is a good feature for ROPUF as it increases
the number of CRPs generated [6]. Spartan 3E diverseness is found to be slightly lower than Artix-7, 2.09. It is observed that the diverseness increases when advanced silicon technologies are used. This is due to the reduced transistor size used in the advanced silicon technology which increases the RO’s frequency. Therefore, slight change in the process variation will be amplified by the higher RO’s frequency.

4.5. ROPUF Reliability
The ROPUF’s responses are generated at different temperature and voltage settings to measure the reliability. Temperature variation experiment is done using temperature chamber. Four different temperature settings are used: 0°C, 20°C, 45°C, and 70°C. For voltage variations, three different internal core supply voltages (VCCINT) are used for Spartan 3E; 1.2V (normal), 1.3V, and 1.4V. For Artix-7 two different VCCINT are used; 1.0V (normal) and 1.2V. The responses that are generated at the different temperature and voltage settings are compared with the responses that are generated at room temperature. The 30-day accelerated aging experiment is also implemented to extend the ROPUF’s reliability study on FPGAs that are fabricated using different silicon technologies.

The average ROPUF’s reliability for Spartan 3E and Artix-7 is 96.34% and 97.28% respectively. Table 2 shows the individual ROPUF’s reliability due to temperature, voltage, and aging effect on ROPUF. Artix-7 reliability is higher than Spartan 3E for temperature, voltage, and aging. The lowest ROPUF’s reliability for both Spartan 3E and Artix-7 is caused by the voltage variations that are 94.26% and 94.82% respectively. The ROPUF’s reliability on the temperature and voltage effects for both Spartan 3E and Artix-7 is high.

Table 2. ROPUF’s Reliability due to Temperature, Voltage, and Aging.

| Reliability (%) | Spartan 3E | Artix-7 |
|-----------------|-----------|---------|
| Temperature     | 97.10     | 98.16   |
| Voltage         | 94.26     | 94.82   |
| Aging           | 97.67     | 98.86   |
Figure 5. Spartan 3E

(i) ROs’ Frequencies changes with respect to the temperature variations

(ii) ROs’ Frequencies changes with respect to the voltage variations

Figure 6. Artix-7

(i) ROs’ Frequencies changes with respect to the temperature variations

(ii) ROs’ Frequencies changes with respect to the voltage variations

Figure 7 shows the aging effect on the 10 ROs’ frequencies on Spartan 3E and Artix-7. For Spartan 3E, the frequencies from 10 ROs are observed to have normal fluctuations. There is no increasing or decreasing frequency’s pattern observed. However, for Artix-7, the frequencies from 10 ROs are
observed to have the similar decreasing pattern. In average, the ROs’ frequencies on Artix-7 are reduced by 0.5 MHz at the end of the aging experiment. This observation suggests that the aging affects RO’s frequency uniformly despite of the RO’s location.

Figure 7. ROs’ Frequencies changes with respect to the aging
ROPUF’s reliability decreases as the bit flip occurrence increases. Bit flip occurrence is depicted by Figure 8 (i). Two ROs’ frequencies with respect to the temperature changes are shown; blue and green ROs. Figure 8 (i) shows how the response bit can flip as the ROs’ frequencies change with respect to the temperature. The frequency of blue RO is higher than the green RO at low temperature. As the temperature increases, the frequency of blue RO is decreasing at much higher rate compared to the green RO. Therefore, the frequency of green RO can be seen to be higher than the blue RO at high temperature. Figure 8 (ii) shows how the bit flip occurrence can be avoided by having a high frequency difference in the RO comparison pair. It can be seen that although the blue RO’s frequency is decreasing at much higher rate than the green RO’s frequency, the blue RO’s frequency is remained to be higher than the green RO’s frequency.

Figure 8. ROs’ Frequencies

Figure 9 shows the probability of bit flip occurrence with respect to the frequency difference in RO comparison pair for both Spartan 3E and Artix-7 FPGAs. The probability of bit flip occurrence is observed to be higher when the frequency difference in RO comparison pair is low. As the difference in the RO comparison pair is increases, the probability of bit flip occurrence is observed to be decreasing. This observation is found on both Spartan 3E and Artix-7. For Spartan 3E, the bit flip occurs when the frequency difference in RO comparison pair is in the range of 0 to 0.9 MHz. For Artix-7, the bit flip
occurs in the range of 0 and 1.99 MHz the range of frequency difference in RO comparison pair where the bit flip occurs is found out to be two times higher in Artix-7 compared to Spartan 3E.

5. Scheme to enhance ROPUF’s reliability

ROPUF reliability can be improved by having a scheme to select the ROs comparison pairs that have high frequency difference. Table 3 shows the numbers of ROs comparison pairs that exceeded the certain amount of frequency difference threshold for Spartan 3E and Artix-7 FPGAs. These numbers are generated from 100 ROs. O(n²) complexity is used to select the RO pair. In average, the numbers of ROs comparison pairs that exceeded the frequency difference threshold for Artix-7 are higher compared to Spartan 3E. The higher number of ROs comparison pairs that exceeded the frequency difference threshold in Artix-7 is due to the high diverseness in the ROs’ frequencies.

| Frequency Difference Threshold (MHz) | Spartan 3E | Artix-7 |
|--------------------------------------|-----------|---------|
|                                      | 2         | 3       | 4       | 2         | 3       | 4       |
| FPGA 1                               | 2933      | 2186    | 1579    | 3112      | 2294    | 1696    |
| FPGA 2                               | 2331      | 1374    | 745     | 2906      | 2043    | 1390    |
| FPGA 3                               | 2783      | 1993    | 1306    | 3525      | 2877    | 2304    |
| FPGA 4                               | 2592      | 1694    | 997     | 2896      | 2078    | 1387    |
| FPGA 5                               | 2255      | 1254    | 622     | 3082      | 2393    | 1817    |

Figure 10 shows the example of ROPUF’s challenges construction. There are 6 ROs used; three ROs are connected to each multiplexer (MUX). From the 6 ROs, 9 ROs comparison pairs are available by using the O(n²) complexity. Each ROs comparison pair has its own 4 bits binary numbers assignment which represents the MUX selection inputs. One-bit response is generated from one ROs comparison pair. The challenges are constructed from the available ROs comparison pairs using combinations without repetition (n!/(n-r)!r!). n is the number of available ROs comparison pairs and r is the length of response bits. In Figure 10, three bits responses are used as an example. In total there are 84 challenge and response pairs can be constructed in this example, but only 9 are shown in Figure 10. For every 3 bits of response, there are 12 bits of challenge. This example suggests that there are abundance of challenge and response pairs can be constructed from 100 ROs in Spartan 3E and Artix-7. For an example, there are 1254 ROs comparison pairs available in Spartan 3E FPGA 5 when the frequency difference threshold is set to be 3 MHz. If the response length is 128 bits, there are 1.2 x 10¹⁷⁸ of challenge and response pairs can be constructed. A higher number of challenge and response pairs are
required for ROPUF applications. A challenge and response pair can be only used once for better security purpose.

Figure 10. ROPUF’s challenge construction.

In this section we showed that by having a higher frequency difference threshold in the ROPUF on both Spartan 3E and Artix-7, does not compromise the ROPUF’s number of challenge and response pairs.

6. Conclusion

In this paper, we have implemented ROPUFs on 20 Artix-7 FPGA chips and 29 Spartan 3E chips which cover a wide range of silicon technologies. We have recorded and analyzed thousands of ROs’ frequencies from each FPGA. Five parameters are used to measure the ROPUF on both Spartan 3E and Artix-7: uniqueness, uniformity, bit-aliasing, diverseness, and reliability. The results showed that the ROPUFs on both Spartan 3E and Artix-7 have reasonable scores for the 5 parameters. The significant difference between Spartan 3E and Artix-7 can be noticed in the uniqueness and diverseness parameters. ROPUF’s uniqueness percentage in Spartan 3E is found to be lower than Artix-7 due to the systematic variation observed in Spartan 3E. Diverseness in the ROs’ frequencies on Artix-7 appears to be higher compared to Spartan 3E because of the smaller transistor size used in Artix-7. Based on the experimental results obtained, we suggest a scheme to increase the reliability of an ROPUF on FPGA. We showed that by choosing ROs comparison pairs that have high frequency difference will not compromising the ROPUF’s security.

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