A hybrid switched inductor with flexible high voltage gain boost converter for DC micro-grid application

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Abstract
A hybrid switched inductor with flexible high voltage gain boost converter for 400 V DC microgrid application is presented in the paper. The three operating modes of the converter are controlled using three switches by two-duty ratios. The proposed converter provides flexibility in the selection of the duty cycle to achieve desired output voltage. Moreover, with two duty ratio, high gain with a wide duty range is accomplished in the proposed converter while an individual switch does not need to operate at a very large duty ratio. The power circuit analysis, operating principles, steady-state voltage gain analysis during continuous conduction mode (CCM) and discontinuous continuous mode (DCM), boundary condition, efficiency analysis, comparison, and circuit parameter design of the proposed converter are presented. A closed-loop controller design and small-signal modeling are discussed. The dynamic behavior of the proposed converter is validated with a change in duty ratio, input voltage, and load power. A laboratory prototype converter is designed and developed to verify the model, and feasibility of different operation modes. The prototype is tested for a power range of 100 W–500 W for different duty cycles.

1 | INTRODUCTION
From the last decade, the DC microgrid has been continuously gaining attention due to the penetration of RES in the distributed generation energy system with the help of power electronics converters. However, the DC microgrid system is mainly powered through Photovoltaic (PV), Fuel Cell (FC), or Energy Storage System (ESS)/batteries through power conversion units [1, 2]. Therefore, the number of PV or FC can be connected in series or in parallel connection to meet the load demand. However, it is not a viable solution that results in lower efficiency and also requires large space for the installation and has higher cost. Therefore, to overcome this shortcoming, a high gain, efficient, and high power density DC–DC converter is accommodated at the source end in the microgrid system [3, 4]. In literature, numerous non-isolated converters based on the switched inductor, switched capacitor, voltage multiplier etc. are addressed to achieve high gain [7, 12]. In order to achieve high voltage, operating a conventional boost converter with a high duty ratio causes several issues such as diode reverse recovery problem, increased level of switching losses, impaired transient response, high voltage/current spikes, and low efficiency [13, 14].

In cascaded and quadratic boost converter, more components are required to achieve high voltage gain, which increases the complexity and results in poor efficiency. The converters employing switched capacitor circuits for achieving high gain can easily boost up the voltage according to the number of Switched Capacitor (SC) cell [9, 12]. These converters do not need any inductive element; however, the main drawbacks concerned with these topologies are ripples in input current, poor voltage regulation during wide load variations, and the required large number of capacitors. The Voltage Multiplier (VM) based DC–DC converters have a modular structure, reduced voltage stress across the switch along high voltage gain. The high capacitor charging transient current and power handling capability of VM capacitors are the major drawbacks associated with VM-based DC–DC converter. However, these boosting techniques increase the complexity, cost, and affect the efficiency of the system. In [15], three different configurations (namely converter I, II, and III) have been presented by modifying the switched inductor boost converter. With the help of two
switches, the switch current stress and conduction loss caused by switched inductors have been overcome. Further, this converter is extended by the addition of diode and capacitor structure to extend the voltage gain. However, in these converters, both switches are controlled with a single-duty ratio. Therefore, the voltage gain of converter-I, II, and III is restricted due to the limitation of duty ratio alike traditional boost converter. Moreover, the shortcomings of [15] converter configurations have been overcome by a non-isolated step-up converter as given in [16] by adding one additional unidirectional controlled switch.

In the [16] converter, the voltage gain has been increased with the adjustment of the two-duty ratio. With the addition of one extra diode and capacitor in the [16] converter, the voltage has been increased and can be controlled in a wide duty range in Double Duty Triple Mode (DDTM) converter as presented in [17]. With the same number of components as in [17] converter with the proper arrangement, the voltage gain of [17] converter has been boosted as presented in [18]. Furthermore, the use of more diodes leads to an increase in the instantaneous power loss by the diodes, needing additional heat sinks. The increased switching frequency significantly increases the switching power loss in the switching devices. In [16, 18], the load side switch is connected with a diode to evade the reverse current flow and short circuit of input supply. With this arrangement, the switching operation of the load side switch is dependent on the series-connected diode. Therefore, this can obstruct the performance of the converter at higher frequencies [19]. However, from [16, 17], it is noticed that the diodes of power circuitry have more contribution to power loss as compared to switches and also affecting the and directly affects the efficiency of the converter.

This article presents a new transformer-less high gain boost converter to achieve high voltage gain with a reduced number of diodes at a lower duty range as compared to the discussed converter. Additionally, the advantage of the proposed converter are: (1) the high duty ratio limitation is overcome by controlling three switches with two distinct duty pulses, (2) continuous input current, (3) current stress of three switches can be controlled optimally with the additional degree of freedom introduced by the two duty pulses, and 4) The lowest average voltage stress on switches and higher efficiency as compared to the converter in [16, 17].

2 | PROPOSED HYBRID SWITCHED INDUCTOR FLEXIBLE HIGH VOLTAGE GAIN BOOST CONVERTER

Figure 1 shows the power circuit topology of the proposed converter. The proposed power circuitry is derived with two inductors ($L_X, L_Y$), two capacitors ($C_I, C_0$), three power MOSFETs ($S_X, S_Y, S_Z$), and one diode $D_0$. The inductance value of both the inductors $L_X$ and $L_Y$ are the same; hence, $L_X = L_Y = L$. In the proposed converter, both switches ($S_X, S_Y$) operate in synchronization and are controlled by a single gate pulse ($k_1$), whereas switch ($S_Z$) is operated through gate pulse ($k_2$) with the delay of $k_1 T_S$.

FIGURE 1 Power circuitry of the proposed converter

Few assumptions are made prior in order to analyse the proposed circuit in CCM and DCM: The components used in the circuit are assumed to be ideal such that the effects of ON-state resistance of switches, forward voltage drops across diodes, and ESR of inductances and capacitances are negligible. Moreover, all the inductors are chosen identical and have equal values.

2.1 | CCM operation

The proposed converter has two different duty pulses, which indicates that the converter operates in three different modes as CCM-I ($0$ to $k_1 T_S$), CCM-II ($k_1 T_S$ to $k_2 T_S$), and CCM-III ($k_2 T_S$ to $T_f$) in CCM.

2.1.1 | CCM-I ($0$ to $k_1 T_S$)

In this mode, switch $S_Y$ and $S_Y$ are turned ON and its corresponding circuitry is illustrated in Figure 2(a). The input voltage supply is in parallel with both inductor ($L_X$ and $L_Y$) and capacitor $C_I$. Therefore, capacitor $C$ charges through switch $S_Y$ and diode $D_Z$ (antiparallel diode of switch $S_Z$) with the current path as $V_{in-SY-C-I-DZ-SX-Vin}$. Capacitor $C$ reverse bias the diode $D_0$ continuously delivering its energy to the resistive load ($R$) as illustrated in Figure 2(a). The equivalent inductor and capacitor voltages in CCM-I is express as

$$
\begin{align*}
\text{CCM-I} & \left\{ 
\begin{array}{l}
(V_{LX})' = (V_{LY})' = (V_{C1})' = V_{in} \\
(V_{C0})' = V_{0}
\end{array}
\right. 
\end{align*}
$$

(1)

2.1.2 | CCM-II ($k_1 T_S$ to $k_2 T_S$)

In this mode, switch $S_Z$ is in conducting state and its corresponding circuitry is illustrated in Figure 2(b). The inductors ($L_X$ and $L_Y$) and capacitor $C_I$ are in series with input supply ($V_{in}$). Therefore, switch $S_Z$ allows both inductor $L_X$ and $L_Y$ to be serially magnetized from the series combination of input supply ($V_{in}$) and capacitor $C_I$ ($V_{in-LXSZ-C1-LY-Vin}$). The
capacitor $C_0$ continuously supplies the energy to the resistive load. Therefore, the following equation can be written:

$$\text{CCM}_{II} \begin{cases} (V_{LX,Y})_{II} = (V_{in} + V_{C1})/2 \\ (V_{C0})_{II} = V_0 \end{cases}.$$ \hfill (2)

### 2.1.3 CCM_{III} ($k_2T_S$ to $T_S$)

In CCM_{III}, three switches ($S_X$, $S_Y$, and $S_Z$) are turned OFF and their corresponding circuit is illustrated in Figure 2(c). The inductors and capacitor $C_I$ are in series connection with input supply along with capacitor $C_0$. Therefore, inductors and capacitor $C_I$ demagnetize/discharge to charge the capacitor $C_0$ and deliver energy to the load ($V_{in} - LX - D_0 - C_0/R - C_1 - LY - V_{in}$).

Therefore, the following equation can be written as

$$\text{CCM}_{III} \begin{cases} (V_{LX,Y})_{III} = (V_{in} + V_{C1} - V_0)/2 \\ (V_{C0})_{III} = V_0 \end{cases}.$$ \hfill (3)

By applying the inductor voltage second balance principle for inductor $L_X$, the resultant output voltage of the proposed converter in CCM is expressed as

$$G_{CCM} = \frac{V_0}{V_{in}} = \frac{2}{1 - k_1 - k_2}. \hfill (4)$$

Figure 3 illustrates the characteristics waveform of the proposed converter in CCM in ideal condition. From (4), It is noted that the proposed converter operates with very few limitations as, at the same time, both duty ratio ($k_1$ and $k_2$) should not be equal to 0.5. The addition of both should, however, not be more than one. Figure 4 illustrates the voltage gain curve MBC-AG with different duty ratio ($k_1$, $k_2$). It is noted that for a different combination, the maximum voltage gain obtained from the proposed converter is 40 with an ailment of ($k_1 + k_2 = 0.95$).

### 2.2 DCM operation

The proposed converter can be operated in DCM mode either by change in load value, switching frequency, or inductance. The proposed converter has four operating modes in DCM operation, out of which the first two modes are similar to the CCM operation. The third mode of CCM ends when the inductor current reaches zero at ($k_3$) and the fourth mode will start after the end of the third mode. The switching diagram of DCMIV is shown in Figure 5(a) and the characteristics waveform in DCM is shown in Figure 5(b). The equivalent current equations in all
four modes can be calculated as

\[
\text{DCM}_I \quad \left\{ (i_{LX})_p = (i_{LY})_p = \frac{V_m k_1 T_S}{L} \right. , \\
\text{DCM}_{II} \quad \left\{ (i_{LX})_p = \frac{V_m (k_1 + k_2) T_S}{L} , \\
\text{DCM}_{III} \quad \left\{ (i_{LX})_p = \frac{(V_0 - 2V_m) k_3 T_S}{2L} .
\right.
\]

In DCM IV, the energy stored in capacitor \( C_0 \) is discharged to the load. Therefore, from (5)–(7),

\[
k_3 = \frac{2V_m (k_1 + k_2)}{(V_0 - 2V_m)}
\]
Therefore, the average capacitor \( C_0 \) current can be expressed as follows:

\[
i_{C0} = \frac{\left( i_{LX}\right)_p k_3 T_S - 2i_0 T_S}{2 T_S} = \frac{\left( i_{LX}\right)_p k_3}{2} - i_0, \quad (9)
\]

\[
i_{C0} = \frac{V_{in}^2 (k_1 + k_2)^2 T_S}{2L(V_0 - 2V_{in})} - \frac{V_0}{R}, \quad \text{(10)}
\]

where \( i_{C0} \) is the current through capacitor \( C_0 \). In the steady-state condition, the average current through capacitor \( C_0 \) is zero. Hence,

\[
\frac{V_{in}^2 (k_1 + k_2)^2 T_S}{L(V_0 - 2V_{in})} = \frac{V_0}{R}. \quad (10)
\]

Using (9), the voltage gain of the proposed converter in DCM mode is derived as

\[
G_{DCM} = \frac{V_0}{V_{in}} = 1 + \sqrt{1 + \frac{(k_1 + k_2)^2}{\tau_L}}, \quad \tau_L = \frac{L}{RT_S}, \quad (11)
\]

where \( \tau_L \) is the generalized inductor time constant. Figure 6(a) shows the voltage gain of the proposed converter in DCM modes at different duty ratio. Using (4) and (11), the boundary for CCM and DCM can be obtained as follows:

\[
\tau_B = \frac{(k_1 + k_2)(1 - k_1 - k_2)^2}{4}, \quad (12)
\]

where, \( \tau_B \) is boundary normalized inductor time constant.

The curve of \( \tau_B \) versus duty cycles is shown in Figure 6(b). In this graph, the part above each curve indicates the CCM area of the proposed converter at that particular duty ratio, whereas, the area below the curve indicates the DCM part of the proposed converter. When \( \tau_B \) is higher than \( \tau_L \), then the proposed converter operates in DCM. Nevertheless, the condition to operate converter in CCM is as follows:

\[
\left( \tau_{LB} = \frac{(k_1 + k_2)(1 - k_1 - k_2)^2}{4} \right) < \left( \tau_L = \frac{L}{RT_S} \right). \quad (13)
\]

### 3 | EFFICIENCY ANALYSIS OF PROPOSED CONVERTER

Figure 7 illustrates the circuit of the proposed converter with the ESR of components. In Figure 7, \( R_{LX}, R_{LY}, R_{C1}, \) and \( R_{C0} \) represent ESR of inductor \( L_X, L_Y, \) capacitor \( C_1, \) and \( C_0, \) respectively. \( R_X, R_Y, \) and \( R_Z \) are the ON-state resistance of switches \( S_X, S_Y, \) and \( S_Z, \) respectively. Diode \( D_0 \) is replaced with their internal resistance \( R_{D0} \) and forward blocking voltage \( V_{FD0}. \) Therefore, the related voltage and current non-ideal equations

**FIGURE 6** Waveform of (a) change in voltage gain \( (G_{DCM}) \) w.r.t. duty ratios \( (k_1 \) and \( k_2) \) and (b) curve of normalized inductor time constant \( (\tau_B) \) versus duty ratios \( (k_1 \) and \( k_2) \) at \( \tau_L = 0.01 \)

**FIGURE 7** Proposed converter power circuitry with ESR of inductors, diodes and capacitors
are expressed as:

\[
\begin{align*}
   (V_{LX})' &= L_{LX} \frac{d}{dt} i_{LX} = V_{in} - i_{LX} (R_{LX} + R_{SX}), \\
   (V_{LY})' &= L_{LY} \frac{d}{dt} i_{LY} = V_{in} - i_{LY} (R_{LY} + R_{SY}), \\
   (V_{C1})' &= V_{0} - i_{C1} (R_{C1} + R_{SX} + R_{SY} + R_{DFZ}) \\
   (V_{C0})' &= (1 - k_{C1}) (V_{0} - V_{0}) = \frac{V_{0} - V_{0}}{R_{C0}} \\
   (i_{C1})' &= \left( \begin{array}{c}
   i_{C1} (1 - k_{C1}) \\
   i_{C1}
   \end{array} \right) = \left( \begin{array}{c}
   \frac{V_{0} - V_{0}}{R_{C0}} \\
   \frac{V_{0} - V_{0}}{R_{C0}}
   \end{array} \right), \\
   (i_{C0})' &= \left( \begin{array}{c}
   \frac{dV_{C0}}{dt} \\
   \frac{dV_{C0}}{dt}
   \end{array} \right) = \left( \begin{array}{c}
   \frac{V_{0} - V_{0}}{R_{C0}} \\
   \frac{V_{0} - V_{0}}{R_{C0}}
   \end{array} \right).
\end{align*}
\]

Therefore, the resultant output voltage of the proposed converter is

\[
V_{0} = 2V_{in} - (B + C)(1 - k_{1} - k_{2}) + \frac{A}{R(1 - k_{1} - k_{2})},
\]

where

\[
A = \left[ \begin{array}{c}
   (R_{LX} + R_{LY} + R_{SX})(1 + k_{1}) + R_{SY} k_{2} \\
   + R_{C1}(1 - k_{1}) + (R_{SX} + R_{SY})(1 + k_{1})
   \end{array} \right],
\]

\[
B = \frac{-i_{C1}}{1 - k_{1} - k_{2}} \left[ R_{C1}(1 - k_{1}) + (R_{SX} + R_{SY})(1 + k_{1}) \right],
\]

\[
C = V_{f} + i_{C0} R_{C0}.
\]

The voltage drop contributed by each circuit component is presented in (18)–(20). It is worth noting that the voltage gain of the proposed converter is limited by ON-state resistance of switches and diodes, ESR of inductors, and capacitors. The input and output power of the proposed converter is derived as

\[
\begin{align*}
   P_{in} &= V_{in} \left[ (i_{LX} + i_{LY} + i_{C1}) k_{1} + (i_{LX/Y/C}) k_{2} \right] + P_{SW} \\
   &= \frac{V_{in} V_{0}(1 - k_{1} - k_{2})}{R(1 - k_{1} - k_{2})} + i_{C1} k_{1} + P_{SW} \\
   R_{L} &= V_{0}^{2} / R
\end{align*}
\]

where \( P_{SW} \) is switching losses by each switch and it is obtained by

\[
\begin{align*}
   P_{SW} &= P_{SW,X} + P_{SW,Y} + P_{SW,Z} = \left\{ \begin{array}{c}
   V_{SX} I_{SX}(t_{X} + t_{Y}) f_{s} \\
   + V_{SY} I_{SY}(t_{Y} + t_{Z}) f_{s} \\
   + V_{SZ} I_{SZ}(t_{Z} + t_{Y}) f_{s}
   \end{array} \right\},
\end{align*}
\]

where \( V_{XX}, V_{YY}, V_{ZZ}, \) and \( ISX, ISY, ISZ \) are the average voltage and current across/through switches \( S_{X}, S_{Y}, \) and \( S_{Z} \), respectively. Whereas, \( t_{X}, t_{Y}, \) and \( t_{Z} \) and \( f_{X}, f_{Y}, \) and \( f_{Z} \) are the rising and falling time for the switches \( S_{X}, S_{Y}, \) and \( S_{Z} \), respectively. Therefore, the efficiency of the proposed converter can be obtained by

\[
\eta = \frac{P_{in}}{P_{out}} = \frac{V_{0}^{2}(1 - k_{1} - k_{2})}{V_{in}^{2}(1 + k_{1}) + (i_{C1} k_{1} + P_{SW})(1 - k_{1} - k_{2})}.
\]

Equation (23) expresses the theoretical expression for the efficiency of the proposed converter.

### 4 COMPARATIVE ANALYSIS

To summarize the advantageous features of the proposed converter, it is compared with the recently published high voltage gain topologies and gathered in Table I. It is noticed that the traditional boost converter is controlled through single-duty pulses, whereas, the voltage gain is restricted by ESR and diode recovery issues. However, by adding switched inductor structure [15] and using several capacitors [12], the voltage gain of boost converter has been increased. However, the voltage gain is not improved substantially with multiple capacitors and inductors. With two inductors and two switches operated by a single duty ratio, three different configurations have been presented in [15]. However, in disregard of two switches and two inductors, the voltage gain of the converters presented is not high. Moreover, it can be seen that the voltage gain of [12, 15] configurations are controlled with single duty ratio and cannot be worked within a wide range of duty cycles. In [16], an extra switch converter is added to increase the output voltage. These three switches, however, are operated by two distinct duty ratios, offering versatility in the choice of the duty ratio and overcoming the duty ratio cap. Moreover, to address the shortcoming of these converters, a DDTM converter topology has been presented in [17]. The
Voltage gain of the DDTM converter is significantly increased with the addition of two more capacitors and two diodes as compared to [17], whereas the voltage gain of [16] and [17] are not equally dependent on both duty ratios. The voltage gain of [16] is more dependent on the first duty ratio, whereas the gain of [17] on the second duty ratio. The voltage gain of the proposed converter is the same as the gain of [18] converter with a reduced number of diodes. In [18], the switching operation of switch $SZ$ is dependent on diode $D2$ as both are connected in series. However, the capacitor $C1$ charging current has to pass through diode $D1$. Hence, diode $D1$ also contributes to countable power loss in an overall loss.

So, it is worth noting that, the voltage gain of the proposed converter is comparatively high as compared to discussed high gain converters and equal to converter-I. Figure 8 represents the curve of change in voltage gain with respect to the duty ratio.

Besides, the high output voltage can be achieved with a minimum number of components as observed from Table 1. From Figure 3, it is noted that the duration of voltage stress across three switches is short as compared to [15, 17] at the same duty ratios. In the [20] converter, the voltage gain is high as compared to the proposed converter with the compromise of more number components. Also, the current stress of the switches increases along with the voltage gain. The reported efficiency is 94.6% at 500 W which is lower due to the more components. It also observed from Table 1, the current stress of the switches is lower as compared to the other converter and equal to the converters of [17, 18]. In the proposed converter, the voltage gain equally depends on both duty ratio, therefore no restriction on adjustment of duty ratio.

### 4.1 Parameter design

#### 4.1.1 Inductor ($L_X$ and $L_Y$) design

The inductor value is selected on the basis of the average value of the charging current, its ripples, duty ratio, and switching frequency. Both inductors with an equivalent inductance ($LX = LY = L$) may be selected based on the operating principle. Therefore, for the CCM operation of the proposed converter, the critical values of each inductor can be calculated as

$$\left( I_{X,Y} \right)_{crit} = \frac{V_{in}(k_1 + k_2)}{f_{j} \Delta i_{X,Y}},$$  \hspace{1cm} (24)$$

where the values of ripple currents for the inductors $L_{X}/Y$ are indicated by $\Delta i_{X}/Y$, respectively. For good estimation, the value of inductor ripple current ($\Delta i_{X}/Y$) is selected between 20% and 40% of the average inductor current.

| Topologies | Components | Voltage gain ($V_{0}/V_{in}$) | Inter capacitor ($V_{CL}/V_{in}$) | Max. blocking voltage across switches ($V_{DS}/V_{0}$) | PIV of diodes ($V_{PK}/V_{0}$) | Current stress of switch | Efficiency |
|------------|------------|-------------------------------|----------------------------------|-----------------------------------------------|-------------------------------|-------------------------|------------|
| [11]       | 2 1 2 3    | (1+k)/ (1-k)                  | –                                | $V_{S1,2} = 1/2$                              | 1                             | $kI_{in}/2, kI_{in}$    | 97.1% at 500 W |
| [12]       | 2 4 1 3    | (2-k)/ (1-k)                  | 1                                | $V_{S1,2} = 1/(1+k)$                         | 3/(2-k)                      | $I_{in}$                 | 90% at 40 W  |
| [15]       | 2 1 2 1    | (1+k)/ (1-k)                  | –                                | $V_{S1,2} = 1/(1+k)$                         | 2/(1+k)                      | $2I_{in}/(1-k)$        | 91.8% at 48 W |
| [15]       | 2 2 2 2    | 2/(1-k)                       | 1                                | $V_{S1,2} = 1/2$                             | $V_{DS} = 1/2, V_{DS2} = 1$ | $I_{in}$                 | 91.8% at 48 W |
| [15]       | 2 3 3 3    | (1+3k)/ (1-k)                 | 1                                | $V_{S1,2} = (k-1)/2(1+3k)$                   | $V_{DS} = 2k/(1+3k), V_{DS2} = 4k/(1+3k)$ | $2I_{in}/(1-k)$        | 91.8% at 48 W |
| [16]       | 2 1 3 2    | 1+k/ (1-k)                    | –                                | $V_{S1,2} = (2-k)/(2-k1-1)\), V_{DS} = 1$  | $V_{DS} = (1-k2)/(1-k1-1), I_{in}/2, I_{in}$ | $I_{in}$                 | 93.6% at 100 W |
| [17]       | 2 2 3 3    | 2-k/ (1-k)                    | 1                                | $V_{S1,2} = 1/2, V_{DS} = 1/2$               | $I_{in}$                      | 94.6% at 500 W         |
| [18]       | 2 3 3 3    | 2/(1-k)                       | 1                                | $V_{S1,2} = 1/2, V_{DS} = 1/2$               | $I_{in}$                      | 94.6% at 500 W         |
| [20]       | 4 3 2 3    | (1+3k)/ (1-k)                 | –                                | $V_{S1,2} = (1/2)+ (1/2G), V_{DS} = 1$      | $V_{DS} = (1/G), V_{DS2} = (1/G)$ | $I_{in}/2, I_{in}k_{2}$ | 94.9% at 500 W |
| Proposed   | 2 2 3 1    | 2/(1-k)                       | 1                                | $V_{S1,2} = 1/2, V_{DS} = 1$                 | $V_{DS} = 1/(1/G)$           | $I_{in}k_{2}/2, I_{in}k_{2}$ | 96% at 500 W  |

Abbreviations: $I_{in}$, Inductor; $C$, Capacitor; $S$, Switch, $D$, Diode; $G$, Voltage gain.
4.2 Capacitor \((C_0 \text{ and } C_1)\) design

The capacitor value is controlled by its charging current, the voltage ripple across it, duty ratio, and switching frequency. During CCM, the capacitor \(C_1\) is being charged and being discharged during CCMII and CCMIII with a value of current equal to \(i_0\). Thus, the capacitor voltage ripple for \(C_1\) can be obtained as follows:

\[
\Delta V_{C1} = \frac{i_0(1-k_1)}{C_1 f_s}, C_1 = \frac{i_{in}(1-k_1)}{\Delta V_{C1 f_s}},
\]

(25)

where \(\Delta V_{C1}\) is the voltage ripple contents of the capacitors \(C_1\) and \(i_{in}\) is the input current. The capacitors \(C_0\) are discharged in CCM and CCMII with a value of current equal to \(i_0\). Thus, the capacitor voltage ripple for \(C_0\) can be obtained as

\[
\Delta V_{C0} = \frac{i_0(k_1 + k_2)}{C_0 f_s}, C_0 = \frac{i_0(k_1 + k_2)}{\Delta V_{C0 f_s}},
\]

(26)

where \(\Delta V_{C0}\) is the voltage ripple contents of the capacitors \(C_0\) and \(i_2\) is the output current. For good estimation, the value of capacitor ripple voltage \((\Delta V_{C0})\) is selected within 1% of the respective capacitor voltage with a voltage rating given by (1).

4.3 Switches \((S_X, S_Y, \text{ and } S_Z)\) and diodes selection

From the analysis and Figure 3, the voltage stress across switches \((S_X, S_Y, \text{ and } S_Z)\) are expressed as

\[
\begin{align*}
(V_{DS})_{X,Y} & = \begin{cases} 
0 : \text{CCM}_I \\
0 : \text{CCM}_II \\
(V_0/2) : \text{CCM}_III 
\end{cases} \\
(V_{DS})_{Z} & = \begin{cases} 
0 : \text{CCM}_I \\
0 : \text{CCM}_II \\
(V_0) : \text{CCM}_III 
\end{cases}
\end{align*}
\]

(27)

Therefore, switches should be selected with reverse blocking capacity as below:

\[
(V_{DS})_{X,Y} > V_0/2, \\
(V_{DS})_{Z} > V_0.
\]

(28)

However, diode \(D0\) handles the Peak Inverse Voltage (PIV) equal to the output voltage \((V_0)\) in CCM and CCMII as observed from Figure 3. Therefore, diode \(D0\) should be selected with PIV handling capability more than the output voltage.

\[
(V_{DS}) > V_0.
\]

(29)

5 | DYNAMIC BEHAVIOUR OF THE PROPOSED CONVERTER

5.1 Closed-loop controller

The dynamic response of the converter is observed with respect to change in input quantity as (a) change in input voltage, (b) change in load, and (c) change in duty ratio.

The control objective in this converter is to control the output voltage during perturbations in input voltage, output resistance, and duty ratio. Unlike other DC-DC converters consisting of only one switch, the proposed converter consists of three switches \((S_X, S_Y, \text{ and } S_Z)\). As switches \(S_X\) and \(S_Y\) are switched simultaneously, the number of switches to be controlled is reduced to two. Conditions governing the control algorithm are given below:

a. The duty cycle of the two switches must follow the inequality \((S_X + S_Z < 1)\), as power stored in the charged inductors is supplied to the load only when all the switches are open. Thus, the sum of two duty cycles must never be greater than 1.0.

b. Depending upon the operating mode, that is, \(S_X < S_Z\) or \(S_X > S_Z\) saturation limits of the two duty cycles must be appropriately selected.

c. There are three states in a switching cycle operation. Switch \(S_Z\) must be turned ON just before switches \(S_X\) and \(S_Y\) have been turned OFF.

Considering these constraints, the two duty cycles are dependent upon each other. Thus, only one control loop is required to achieve the closed-loop performance of the converter. The other duty cycle can be determined by using the lookup table based on the recorded steady-state performance of the converter.

With the above-discussed strategy, the control algorithm is shown in Figure 9. Error obtained by subtracting output voltage reference with actual output voltage is represented by \(e(t)\). This error is passed through PI controller block to generate a \(X_1(t)\) which will be passed through lookup table to generate a signal of \(X_2(t)\). Both the constant value signal \(X_1(t)\) and \(X_2(t)\) are compared with carrier signal of 50 kHz frequency to generate the duty cycles. The respective duty pulses of both switches are obtained by doing the XOR logic operation as shown in Figure 9.
5.2 Small signal modelling of the proposed converter

The state-space matrix of the proposed converter in CCMI, CCMII, and CCMIII can be obtained as follows:

\[
\begin{bmatrix}
\frac{di_L}{dt} \\
\frac{dV_{C1}}{dt} \\
\frac{dV_{C0}}{dt}
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 \\
-2/C_1 & 0 & 0 \\
0 & 0 & -1/RC_0
\end{bmatrix}
\begin{bmatrix}
i_L \\
V_{C1} \\
V_{C0}
\end{bmatrix} +
\begin{bmatrix}
1/L \\
0 \\
0
\end{bmatrix} [V_{in}]
\]

\[
V_0 = \begin{bmatrix} 0 & 2 & [i_L] \\ 0 & 0 & V_{C1} \\ 1 & 0 & V_{C0} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} [V_{in}]
\]

\[
\begin{bmatrix}
\frac{di_L}{dt} \\
\frac{dV_{C1}}{dt} \\
\frac{dV_{C0}}{dt}
\end{bmatrix} =
\begin{bmatrix}
0 & 1/2L & 0 \\
1/C_1 & 0 & 0 \\
0 & 0 & -1/RC_0
\end{bmatrix}
\begin{bmatrix}
i_L \\
V_{C1} \\
V_{C0}
\end{bmatrix} +
\begin{bmatrix}
1/2L \\
0 \\
0
\end{bmatrix} [V_{in}]
\]

\[
V_0 = \begin{bmatrix} 0 & 1 & [i_L] \\ 0 & 0 & V_{C1} \\ 1 & 0 & V_{C0} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} [V_{in}]
\]

\[
\begin{bmatrix}
\frac{di_L}{dt} \\
\frac{dV_{C1}}{dt} \\
\frac{dV_{C0}}{dt}
\end{bmatrix} =
\begin{bmatrix}
0 & 1/2L & -1/2L \\
1/C_1 & 0 & 0 \\
0 & 0 & -1/RC_0
\end{bmatrix}
\begin{bmatrix}
i_L \\
V_{C1} \\
V_{C0}
\end{bmatrix} +
\begin{bmatrix}
1/2L \\
0 \\
0
\end{bmatrix} [V_{in}]
\]

\[
V_0 = \begin{bmatrix} 0 & 1 & [i_L] \\ 0 & 0 & V_{C1} \\ 1 & 0 & V_{C0} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} [V_{in}]
\]

\[
A = \begin{bmatrix}
0 & (1 - k_1)/2L & -(1 - k_1 - k_2)/2L \\
(1 - k_1)/C_1 & 0 & 0 \\
0 & 0 & -1/RC_0
\end{bmatrix}
\]

\[
B = \begin{bmatrix}
(1 + k_1)/2L \\
0 \\
0
\end{bmatrix} ;
C = \begin{bmatrix}
0 & (1 + k_1)^T \\
0 & 1
\end{bmatrix}
\]

When a disturbance occurs or is introduced (perturbations), the system response consists of a steady-state part and a transient part. After introducing the perturbations, the obtained system is having two components as the DC part and the AC part obtained by (34). The state-space model of proposed converter in terms of the control parameter (output voltage and duty ratio) is obtained as

\[
\begin{bmatrix}
\frac{d\hat{i}_L}{dt} \\
\frac{d\hat{V}_{C1}}{dt} \\
\frac{d\hat{V}_{C0}}{dt}
\end{bmatrix} =
\begin{bmatrix}
0 & (1 - k_1) & -(1 - k_1 - \hat{k}_2) \\
-\hat{k}_1/2L & -k_2 - \hat{k}_0/2L \\
(1 - k_1 - \hat{k}_0)/C_1 & 0 & 0 \\
0 & 0 & -1/RC_0
\end{bmatrix}
\begin{bmatrix}
\hat{V}_{C1} \\
\hat{V}_{C0}
\end{bmatrix} +
\begin{bmatrix}
\gamma_i \\
\gamma_{C1} \\
\gamma_{C0}
\end{bmatrix} \begin{bmatrix} 0 & (1 + \hat{k}_1)/2L \\
\hat{V}_{C1} \\
\hat{V}_{C0} \end{bmatrix}
\]

\[
\begin{bmatrix}
\hat{V}_{C1} \\
\hat{V}_{C0}
\end{bmatrix} = \begin{bmatrix}
0 & 0 & \hat{V}_{C1} \\
0 & 1 & \hat{V}_{C0}
\end{bmatrix}
\]

By controlling only duty ratio (k_1) and respective control logic between duty ratio (k_1 and k_2), the state-space model of the proposed converter with only duty ratio (k_1) is obtained as

\[
\begin{bmatrix}
\frac{d\hat{i}_L}{dt} \\
\frac{d\hat{V}_{C1}}{dt} \\
\frac{d\hat{V}_{C0}}{dt}
\end{bmatrix} =
\begin{bmatrix}
0 & (1 - k_1)/2L & -(1 - k_1 - \hat{k}_2)/2L \\
(1 - k_1)/C_1 & 0 & 0 \\
0 & 0 & -1/RC_0
\end{bmatrix}
\begin{bmatrix}
\hat{V}_{C1} \\
\hat{V}_{C0}
\end{bmatrix} +
\begin{bmatrix}
\gamma_i \\
\gamma_{C1} \\
\gamma_{C0}
\end{bmatrix} \begin{bmatrix} 0 & (1 + k_1)/2L \\
\hat{V}_{C1} \\
\hat{V}_{C0} \end{bmatrix}
\]

\[
\begin{bmatrix}
\hat{V}_{C1} \\
\hat{V}_{C0}
\end{bmatrix} = \begin{bmatrix}
0 & 0 & \hat{V}_{C1} \\
0 & 1 & \hat{V}_{C0}
\end{bmatrix}
\]
The transfer function of the system can be obtained from the relation $TF = C(SI-A)^{-1}B$. The matrix form between the output voltage and duty ratio is obtained as follows:

$$\hat{V}_0 \hat{k}_1 = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & \frac{1}{2L} \left( 1 - k_1 \right) \frac{1}{2} & \frac{1}{C} & 0 \\ \frac{1}{2L} \left( 1 - k_1 \right) \frac{1}{2} & \frac{1}{C} & 0 & \frac{-i_L}{RC} \\ 0 & 0 & -i_L/C_1 \\ 0 & 0 & 0 \\ \end{bmatrix} \begin{bmatrix} (V_{C0} - V_{C1})/2L \\ \frac{1}{RC0} (S^2 + S) (V_{C0} - V_{C1}) + k_1 (RC0) S + 1 \frac{i_L}{C_1} I \\ \end{bmatrix}$$

(36)

$$\hat{V}_0 \hat{k}_1 = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & \frac{1}{2L} \left( 1 - k_1 \right) \frac{1}{2} & \frac{1}{C} & 0 \\ \frac{1}{2L} \left( 1 - k_1 \right) \frac{1}{2} & \frac{1}{C} & 0 & \frac{-i_L}{RC} \\ 0 & 0 & -i_L/C_1 \\ 0 & 0 & 0 \\ \end{bmatrix} \begin{bmatrix} (V_{C0} - V_{C1})/2L \\ \frac{1}{RC0} (S^2 + S) (V_{C0} - V_{C1}) + k_1 (RC0) S + 1 \frac{i_L}{C_1} I \\ \end{bmatrix}$$

(37)

6 HARDWARE RESULT DISCUSSION

A 500 W laboratory prototype of the proposed converter is developed to validate the theoretical analysis as shown in Figure 10. A list of specifications for the different circuit components of the prototype is presented in Table 2. The two gate pulses are generated through Virtex-5 FPGA with a 50% duty cycle ($k_1$) to control switches $S_X$ and $S_Y$. Also, the gate pulse with a 35% duty cycle is generated to control switch $S_Z$ with a delay of the ON period of switch $S_X$ and $S_Y$.

Figure 11(a) illustrates the waveform of input–output voltage and current at $k_1 = 0.5$ and $k_2 = 0.35$. The proposed converter achieves 400 V at the output from 31 V input voltage. It can be seen that input current is having highest peak value in CCMI as it addition of both inductor current and capacitor $C_1$ current. The inductors and capacitor $C_1$ current is equal to input current in CCMII with same positive slope as in CCMI, whereas in CCMIII, with a negative current slope, the input current begins to decrease as both inductors and capacitor begin demagnetizing/discharging in the load. The average values of output voltage and output current are observed as 400 V and 1.26 A, while

![Figure 11](image-url)
### TABLE 2 Designing parameters of the proposed converter

| Parameters | Ideal     | Prototype          |
|------------|-----------|--------------------|
| Power      | 500 W     | 500 W              |
| Input Voltage \((V_{in})\) | 30 V     | 25–36 V           |
| Duty ratio \(k_1 = 0.5, k_2 = 0.35\) | \(k_1 = 0.5, k_2 = 0.35\) |
| Output voltage \((V_0)\) | 400 V | 400 V               |
| Load       | 320 Ω     | 322 Ω              |
| Switching freq. | 50 kHz  | 50 kHz            |
| Inductor \(L_X\) and \(L_Y\) | >18 μH | \(\approx 200 \mu H, 20 A\) (shell type) |
| Capacitor \(C_i\) | >0.3 μF | \(\approx 22 \mu F, 100 V\) (film) |
| Capacitor \(C_0\) | >0.15 μF | \(\approx 22 \mu F, 450 V\) (film) |
| Switches \(S_X, S_Y, S_Z\) | \(\approx 400 V, 20 A\) | \(V_{DS,X} = 900 V, i_T = 36 A, R_{ON} = 65 m\Omega\) (C3M0065090D) |
| Diode \(D_0\) | \(\approx 600 V, 20 A\) | \(V_{RMM} = 600 V, i_T = 30 A, R_{ON} = 0.01\Omega, V_F = 0.8 V\) (STTH30R04/6) |

The input voltage with non-ideality and input current average values are observed as 31 V and 16.93 A. It is worth to note that the proposed converter operate with 96% efficiency at 500 W power.

Figure 11(b) depicts the waveform of output voltage \(V_0\), inductor \(L_X\) current \(i_LX\), inductor \(L_Y\) current \(i_LY\), and input current \(i_{in}\). Both the inductors are magnetized in CCMI and CCMIII; therefore, both inductors have a positive charging slope in CCMII and CCMIII and a negative slope in CCMIII. The experimentally observed average inductor \((L_X\) and \(L_Y\)) currents are 8.3 and 8.4 A, respectively. Figure 11(c) depicts the waveform of the inductor’s current and voltage. Both inductors are individually charged with 31 V in CCMI and CCMII. On the other hand, the voltages across both inductors in the CCMIII are equal to \((-169 V)\). Slight fluctuations are observed in both inductor voltage waveforms in CCMIII due to unequal voltage sharing of input and capacitor \(C_I\) between both inductors along with the slight practical difference in inductor ESR.

Figure 12(a) illustrates the waveform of voltage across switches (drain to source). It is noticed that the maximum voltage stress across switch \(S_X\) and \(S_Y\) is (200 V) in CCMIII only. Similarly, switch \(S_Z\) handles 400 V \((V_{DZ})\) in CCMIII only. Figure 12(b) shows the dynamic behaviour of the proposed converter with a change in duty ratio \(k_2\) from 0.35 to 0.2 while \(k_1 = 0.5\). It is worth noting from experimentally obtained results, the proposed system giving stable output voltage and current and regulating for the entire range of duty ratio. Figure 12(c) depicts the experimental efficiency of the proposed converter at different power with different duty ratios and at constant load. It is noted that 96.1% efficiency is achieved at 500 W power. From Figure 12(d), it is observed that the proposed converter effectively works and is regulated for the entire range of duty ratio. With the help of (28) and (29), the power loss distribution across each component in the proposed converter is graphically represented in Figure 12(d).
at $k_1 = 0.5$ and $k_2 = 0.35$ with consideration of $R_{LX/Y} = 200 \text{ m}\Omega$, $R_{C1/Y} = 200 \text{ m}\Omega$, $R_{S/X/Y/Z} = 65 \text{ m}\Omega$, $R_{D0} = 0.01 \text{ \Omega}$, and $V_{F0} = 0.8 \text{ V}$. It is investigated that three switches have more loss contribution as compared to other components, whereas output capacitor $C_0$ has less contribution to power losses.

To validate and check the dynamic response of the proposed converter under a change in input voltage ($V_{in}$), and load power ($P_0$), two tests are conducted by adding an input capacitor at the source end to reduce the input current ripple as below:

### 6.1 Test I: Response under input voltage ($V_{in}$) perturbation

To observe the dynamic performance of the proposed converter with perturbation in input voltage, the input voltage with perturbation of (31 to 26.5 V) is applied to the system and the reference output voltage set to +400 V. The experimental results obtained under test-I are shown in Figure 13(a) which shows the input voltage ($V_{in}$), input current ($i_{in}$), output voltage ($V_0$) and output current ($i_0$) waveform with perturbed input voltage. It is observed that a constant of 400 V is achieved at the output even though input voltage is varied from 31 to 26.5 V. Moreover, to support the investigation, input current ($i_{in}$) and output current ($i_0$) are also shown. From the input current waveform, it is investigated that, the mean value of input current is increased in corresponding to decrease in input voltage to maintain the power equality at input and output side. To maintain the constant output voltage with respective changes in input voltage, the duty cycle ($k_1$ and $k_2$) needs to be adjusted by the PI controller according to the error signal.

### 6.2 Test II: Response under perturbation of load power

Figure 13(b) depicted the output voltage ($V_0$), input voltage ($V_{in}$), output current ($i_0$), and input current ($i_{in}$) waveforms when load power ($P_0$) changes. It is observed that the constant output voltage 400 V is achieved from 31 V even power changed. The input and output current changed accordingly to satisfy the power balance at the input and output side.

### 7 Conclusion

For 400 V DC microgrid applications, a new transformer-less modified boost converter with an adjustable voltage gain at a wide range of duty ratios is presented. The high voltage gain is achieved with the fine adjustment of two separate duty ratios without the use of the high duty ratio for the individual switch. The waveform of the CCM and DCM characteristics is studied and the CCM-DCM boundary is elaborated in detail in efficiency analysis. It is worth noting that, with a minimal number of components, the proposed converter provides high voltage gain and reduces voltage stress through switches and diodes.
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