Abstract—Designing efficient and scalable sparse linear algebra kernels on modern multi-GPU based HPC systems is a daunting task due to significant irregular memory references and workload imbalance across the GPUs. This is particularly the case for Sparse Triangular Solver (SpTRSV) which introduces additional two-dimensional computation dependencies among subsequent computation steps. Dependency information is exchanged and shared among GPUs, thus warrant for efficient memory allocation, data partitioning, and workload distribution as well as fine-grained communication and synchronization support. In this work, we demonstrate that directly adopting unified memory can adversely affect the performance of SpTRSV on multi-GPU architectures, despite linking via fast interconnect like NVLinks and NVSwitches. Alternatively, we employ the latest NVSHMEM technology based on Partitioned Global Address Space programming model to enable efficient fine-grained communication and drastic synchronization overhead reduction. Furthermore, to handle workload imbalance, we propose a malleable task-pool execution model which can further enhance the utilization of GPUs. By applying these techniques, our experiments on the NVIDIA multi-GPU supernode V100-DGX-1 and DGX-2 systems demonstrate that our design can achieve on average 3.53× (up to 9.86×) speedup on a DGX-1 system and 3.66× (up to 9.64×) speedup on a DGX-2 system with 4-GPUs over the Unified-Memory design. The comprehensive sensitivity and scalability studies also show that the proposed zero-copy SpTRSV is able to fully utilize the computing and communication resources of the multi-GPU system.

Index Terms—Sparse Linear Algebra Kernels, Triangular Solver, Multi-GPU Systems, Task Model

I. INTRODUCTION

Multiple Graphics Processing Units (GPUs) based server architectures such as NVIDIA DGX-1K2 [1] become increasingly popular in modern HPC systems for further enhancing the acceleration of high throughput workloads. Due to the ever-increasing size of data, the demand of out-of-memory execution is ever-increasing in emerging domains including deep learning, big data analytics, and planet-scale applications. Since the recent GPUs on multi-GPU systems have their own local memory and distributed memory space, executing large-scale sparse linear algebra operations on these multi-GPU systems presents several challenges, especially for the case of Sparse Triangular Solver (SpTRSV) kernel in which strong inner-dependency among the computation steps is inherent. However, the existing optimization techniques (e.g., synchronization-free execution [2], [3]) for sparse linear algebra kernels either focus on multi-CPUs system where dependency can be handled by sequentially execution [4] or assume that the problem data always fits into a single GPU [2], [3], [5]. They do not offer orchestrated strategies to improve the scalability in multi-GPU platforms.

SpTRSV is considered as the main kernel for many important HPC applications, such as numerical simulation, power grid simulation and optimization, computational chemistry, and climate modeling, in the direct solution of linear systems and least squares problems, structured-grid problems, the preconditions of iterative methods, etc [4], [6]–[14].

Given \( Lx = b \) or \( Ux = b \), where \( L \) is the Lower triangular matrix, \( U \) is the Upper triangular matrix, \( b \) is the vector of values, SpTRSV seeks the solution for vector \( x \). We refer to an entry of \( x \) as a component. Solving a component may require certain dependencies to be met. In this paper, we consider designing SpTRSV on a single compute node with multiple GPUs (i.e., scaling-up). We partition the larger matrices among the GPUs. Hence, to calculate the dependencies for each component, GPUs may require to share information with each other. Unless proper consideration is given, such inter-GPU information exchange can introduce severe inter-GPU data movement and synchronization problems. Additionally, due to the partitioning strategy of columns of \( L \) matrix and \( b \) in the baseline distribution model, components are solved in the ascending order (Section III). This can adversely affect workload balance due to uneven waiting time of the GPUs which, in turn, can degrade the performance of SpTRSV on a multi-GPU system.

To tackle the challenges above, we propose an efficient and scalable design for the parallel execution of Sparse Triangular Solver on modern multi-GPU systems.

First, to facilitate easy data sharing and memory allocation, the state-of-the-art method involves using the unified memory introduced by the major vendors (e.g., NVIDIA), which spans across all the processors (CPU and GPUs) in the system. However, we find that enabling the Unified Memory for efficient data exchange is often counterproductive (Section III). To improve this, we employ the latest
NVSHMEM \cite{15} technology based on the OpenSHMEM \cite{16,17} specification. NVSHMEM provides high-level application programming interface for partitioned global address space. It supports fine-grained one-sided get and put operations, and peer-to-peer (P2P) communication directly from GPU kernels which result in opportunities to overlap computation and communication. With NVSHMEM, we propose a ‘zero-copy’ mechanism to eliminate page migration and avoid memory contention. In our proposed design, the dependencies of SpTRSV are accumulated on each GPU’s symmetric heap and asynchronously communicated using the get operation. Experiments demonstrate that our NVSHMEM-based design overcomes the limitations of the Unified Memory approach and improves the performance of SpTRSV significantly.

Second, to tackle workload imbalance on GPUs, we propose a task distribution model that not only distributes component more evenly among GPUs but also ensures that the independent calculations are scheduled on different GPUs, thus ensuring high utilization of the GPU hardware. We finally demonstrate that a combination of fine-grained communication, efficient overlapping between computation and communication, synchronization-free execution, and thoughtfully designed load balancing helps achieve better overall performance and scalability. In summary, this paper makes the following contributions:

- Through performance characterization, we identify that applying the state-of-the-art Unified Memory for data sharing among GPUs may cause severe performance penalty (Section \textbf{III}).
- We leverage the new NVSHMEM technology to design an efficient and scalable algorithm for the SpTRSV kernel executing on a multi-GPU system setup. It has profound design implication for a spectrum of applications that have inherent irregular memory accesses and strong inner-task dependencies (Section \textbf{IV}).
- For better workload balancing, a novel task scheduling scheme is further introduced (Section \textbf{V}).
- We demonstrate the performance benefit and scalability of our proposed SpTRSV design on a range of inputs that require out-of-core execution (Section \textbf{VI}).

\section{Background}

\subsection{Dependencies of SpTRSV}

The sparse triangular solver operation (SpTRSV) is an important building block of many numerical linear algebra applications, which is to solve the following linear equations:

\begin{equation}
    Lx = b \quad \text{or} \quad Ux = b
\end{equation}

where $L$ and $U$ are square lower and upper triangular matrices, $x$ and $b$ are the solution and right-hand-side vectors. Based on the processing order, solving $Lx = b$ is often referred to as \textit{forward substitution} while solving $Ux = b$ is referred to as \textit{backward substitution}.

In comparison with other sparse basic linear algebra subprograms (BLAS) \cite{18} such as sparse matrix-vector multiplication (SpMV) and sparse-sparse matrix-matrix multiplication (SpGEMM), SpTRSV is more challenging to parallelize due to the inherent complex dependencies within the linear system. Since backward substitution follows the similar procedure as forward substitution (i.e., solving $x$ in descending order), in this work, without loss of generality, we use forward substitution for illustration.

Algorithm 1 shows a typical serial implementation for solving a dense $Lx = b$. The algorithm accesses all columns in ascending order (Line 3) to solve each component of the solution vector $x$ using an intermediate array $\text{left.sum}$ (Line 2). $\text{left.sum}$ maintains the partial sums computed during the intermediate steps corresponding to the nonzero entries of the columns in $L$. In each step, the value of one component, $x_i$, is calculated and then $\text{left.sum}_j$ values are updated by computing $x_i \times l_{ij}$ and adding this value to $\text{left.sum}_j$ (Line 6). In the subsequent iterations, these $\text{left.sum}_j$ values are used to compute $x_{i+1}$ components.

Two types of dependencies in the algorithm make it challenging to parallelize the SpTRSV kernel. First, all $l_{ij}$ in the same row $i$ need to be accessed to update $\text{left.sum}_i$, which creates \textit{column dependency}. Second, the $\text{left.sum}_j$ depends on $x_i$ and $l_{ij}$, which causes \textit{row dependency}. Figure 1(a) shows an example of $L$ matrix and the column and row dependencies for the non-zero values (nnz) at the last row and the first column, respectively. In order to calculate a component $x_3$, components $x_0$, $x_3$ and $x_4$ have to be calculated due to the column dependency while all of $\text{left.sum}_1$, $\text{left.sum}_3$, $\text{left.sum}_5$ and $\text{left.sum}_7$ is row dependent on $x_0$.

If we assume the input matrix $L$ is stored in the compressed sparse column (CSC) format, even if the zero-valued entries of $l_{ij}$ can be skipped, the row and column dependencies still exist.
B. Parallel SpTRSV

The parallel solutions of sparse triangular linear systems have been studied by many researchers [2], [4], [5], [10], [19]–[24]. The common strategy comes from the observation that some components are independent and can be processed simultaneously. For example, in the dependence graph of Figure 1a, components $x_1$, $x_3$ and $x_5$ only depend on component $x_0$. Therefore, they can be processed in parallel after $x_0$. By analyzing the $L$ matrix firstly, the components can be reorganized into a number of level-sets where the components within a set can be solved in parallel as shown in Figure 1b. Naumov [5] first proposed the single GPU version of sparse triangular solver based on this strategy using CUDA’s parallel programming paradigm. However, the performance of the parallel algorithm based on level-sets can be limited for several reasons, especially when the matrices exhibit higher number of dependencies among different components. First, the number of components within each set may be small which reversely lead to reduced utilization of the system due to low workload on GPUs. Second, there can be a very large number of levels generated from the complex dependencies among the components. In this case, synchronization after each level is mandatory, which can be problematic. Finally, the analysis phase of generating the dependency graph can incur substantial preprocessing overhead, degrading the efficiency of parallel execution if the solver phase is only invoked a few times.

C. Synchronization-Free SpTRSV

To address the inefficiency of level-based parallel SpTRSV algorithm on GPUs, Liu et al. [2] propose a fast synchronization-free algorithm for parallel SpTRSV on GPUs. The basic idea is to activate all components on GPUs at the beginning. However, each component will not be processed until the dependencies are satisfied. To track how many dependencies are currently outstanding, a simple preprocessing step calculates the in-degrees (dependencies) for each component. Each of these components are separated into two phases: lock-wait and solve-update. In the lock-wait phase, a component waits in the loop until the column dependency is satisfied. After that, the component is unlocked to solve the value and then update its dependants based on the row dependence. Rather than the expensive prepossessing step that involves dependency graph computation and synchronization, the components are scheduled by the hardware scheduler of the GPU. Compared with the level-based parallel SpTRSV, synchronization-free mechanism can immediately solve the component as long as all the dependencies are met.

III. SpTRSV with Unified Memory

A. Communication Through Unified Memory

The main objective of this work is to design an efficient parallel SpTRSV algorithm on a multi-GPU system. To enable inter-communication among the GPUs to exchange the dependency information, we first attempt to leverage CUDA’s Unified Memory programming model on modern GPUs. Unified Memory provides a single memory address space, where a pool of managed memory is accessible from both CPUs and GPUs using a single pointer within a multi-GPU system [25], [26]. One of the most salient feature of Unified Memory is that the system automatically migrates data allocated in Unified Memory (using cudaMemcpyManaged API) between the host and device.

Inspired by the aforementioned work [2] (Section II-C), our algorithm leverages synchronization-free execution mechanism to handle the dependencies among the components and eliminates the cost of system-level barrier synchronization. Algorithm 2 shows the pseudocode for our multi-GPU SpTRSV algorithm with Unified Memory. We assume that each solution component $x$, the related right-hand-side vectors $b$ and the columns of matrix $L$ are evenly distributed on the multi-GPU system. Matrix $L$ is represented in a compressed sparse column (CSC) format consisting of three arrays: col.ptr, row.idx, and val. We maintain two intermediate arrays, in.degree and left.sum of size $n$, to keep track of the number of unfinished dependencies and the partial sums calculated from previously calculated components respectively. Compared to aforementioned work [2], the distributed data post several unique algorithmic design distinctions discussed below.

To keep track of the dependencies and enable inter-communication between GPUs, our algorithm allocates the intermediate arrays in the unified memory space ($s.left.sum$ and $s.in.degree$ in Lines 2–5) to enable data sharing and remote inter-communication. In addition, for device-local updates and

Algorithm 2: SpTRSV on multiple GPUs with unified memory

| Input: | col.ptr, row.idx, val, $B_n$ |
| Output: | $X_n$ |
| 1: | procedure SpTRSV-UNIFIED |
| 2: | cudaMemcpyManaged(*s.left.sum, n) |
| 3: | cudaMemcpyManaged(*s.in.degree, n) |
| 4: | cudaMemcpy(*s.left.sum, 0) |
| 5: | cudaMemcpy(*s.in.degree, 0) |
| 6: | Get in.degree for all $x$ |
| 7: | for all $d \in ngpu do$ \quad parallel in GPUs |
| 8: | for all $i \in nz do$ \quad parallel in threads |
| 9: | s.atomic.incr(&s.in.degree[row.idx[i]]) |
| 10: | \textbf{Solve: $X_n$} |
| 11: | for all $d \in ngpu do$ \quad parallel in GPUs |
| 12: | cudaMemcpy(*d.left.sum[d], dev_n[d]) |
| 13: | cudaMemcpy(*d.in.degree[d], dev_n[d]) |
| 14: | cudaMemcpyManaged(*d.left.sum[d], 0) |
| 15: | cudaMemcpyManaged(*d.in.degree[d], 0) |
| 16: | for all $i \in n do$ \quad parallel in warps |
| 17: | while d.in.degree[d][i]+1 ≠ s.in.degree[i] do |
| 18: | Lock() |
| 19: | $x[i] \leftarrow b[i] - d.left.sum[d][i] - s.left.sum[i]$ |
| 20: | $x[i] \leftarrow x[i]/val[col.ptr[i]]$ |
| 21: | for all $j \in nz, do$ \quad parallel in threads |
| 22: | rid $\leftarrow$ row.idx[j] |
| 23: | if rid $\in dev_d$ then |
| 24: | d.atomic.add(&d.left.sum[d][rid], val[j]*x[i]) |
| 25: | d.atomic.incr(&d.in.degree[d][rid]) |
| 26: | else |
| 27: | s.atomic.add(&s.left.sum[rid], val[j]*x[i]) |
| 28: | s.atomic.decr(&s.in.degree[rid]) |
faster access during intermediate calculation for dependencies, the algorithm also allocates device-local arrays (d.left.sum and d.in.degree in Lines 12–15). By distinguishing between the device-local updates and unified memory updates the algorithm reduces unnecessary remote data access between two GPUs which has been shown to be a major obstacle for performance scaling on multi-GPU systems \cite{27}, \cite{28}.

However, after workload profiling, we observe two major disadvantages of this approach due to the invisible data migration of Unified Memory and unidirectional dependency feature of the triangular matrix. Figure 2 illustrate the data communication model of the Unified Memory approach. In this figure, two GPUs are connected with NVLink. The GPUs communicate the dependency values in degree using both unified and device memory. The left.sums are also allocated similarly so we do not show them in this figure. From the figure, we observe that all x₁, x₂ and x₃ components solved by GPU 0 need to access the s.in.degree of x₄ remotely to update the value while the busy-wait loop of x₄ on GPU 1 also needs to access the value on unified memory continuously to check if all dependencies have been met. Since the unified memory is designed to manage the data transparently to users, GPU 0 and GPU 1 will compete for the s.in.degree value of x₄. As a result, a huge number of page thrashing is generated and the pages containing the data bounce back and forth between GPU 0 and GPU 1. In addition, we can see that system-wide atomic updates are unidirectional, i.e., the components with larger numbers (x₄, . . . ,7) always depend on proceeding components (x₀, . . . ,3) in forward substitution. Consequently, GPU 1 has longer waiting time than GPU 0. This can severely limit the scalability of SpTRSV on a multi-GPU system.

### B. Characterising the Page Thrashing of Unified Memory

To evaluate the performance implication of page thrashing on SpTRSV with the Unified Memory approach more extensively, we perform experiments on a NVIDIA V100-DGX-1 multi-GPU system. The DGX-1 system is equipped with eight of the NVIDIA Tesla V100 GPUs. The GPUs are organized in a hybrid cube-mesh interconnection network topology. The twelve edges of the cube are connected through NVLink and two of the six faces have their diagonals connection \cite{29}.

Figure 3 shows the profiling results of running SpTRSV algorithm on DGX-1 with the Unified Memory approach using four representative matrices from SuiteSparse \cite{30}. The results are reported by normalizing to the 2-GPU execution since we want to make observations on multi-GPU systems. Figure 3a demonstrates that the number of page faults caused by the data contention on Unified Memory increases with the growing number of GPUs. This is due to the fact that the memory allocated on the unified memory to compute and track the dependencies (in-degrees) gets updated by system-wide atomic operations (e.g. s.atomic.decr) by all GPUs. In this case, the required pages containing the shared data bounce back-and-forth among different GPUs to update different operations, which in turn have detrimental effect on the execution time of SpTRSV as shown in Figure 3b. For example, except for matrix nlpkkt160 which has the highest potential for parallelism with the least amount of dependencies, other matrices exhibit performance degradation on the increasing number of GPUs (from 2 to 8) even though there are more computing resources allocated progressively on a 8-GPU system.

In summary, due to the high amount of page faults caused by the updates from multiple GPUs on shared data in the Unified Memory space, it is not viable to employ Unified Memory in designing multi-GPU SpTRSV.

### IV. Zero-copy SpTRSV with NVSHMEM

In this section, we design a novel zero-copy sparse triangular solver on multi-GPU systems that employs NVIDIA's NVSHMEM technology based on OpenSHMEM \cite{15}–\cite{17} for efficient inter-communication among GPUs. This approach avoids memory contention among GPUs and eliminates the automatic data migration through the Unified Memory.

#### A. NVSHMEM Overview

NVSHMEM \cite{15} extends OpenSHMEM’s interface to allocate pinned memory on NVIDIA GPUs that are distributed and interconnected with NVLink or PCIe. Each GPU can be considered as a processing element (PE) and NVSHMEM allocates symmetric heap on each PE. These symmetric heaps together constitute the global address space, hence conforming...
to the Partitioned Global Address Space (PGAS) programming model. In addition, for better overlapping between communication and computation, NVSHMEM enables GPU-initiated fine-grained point-to-point communication with *get* and *put* operations. NVSHMEM also provides synchronization primitives for data allocation on the heap.

Figure 4 shows the memory layout and communication model of NVSHMEM. During initialization, each instance GPU is assigned with a unique ID, called the PE ID. PEs within a NVSHMEM job can share data through the globally accessible memory that is allocated using the NVSHMEM allocation API (e.g. `nvshmem_malloc`). Otherwise, memory allocated using any other CUDA methods (e.g. `cudaMalloc`) is private to the allocating PE and is not accessible by other PEs. Shared memory objects allocated in the global address space (e.g., `x` and `y` in Figure 4) are collective and symmetric across all the PEs in a job. This requires all PEs to participate in the allocation call and pass the same value in the size argument during data allocation. For communication, PEs use `put/get` API of NVSHMEM to write/read the shared data value to/from remote GPUs. For example, GPU 0 uses command `PUT(&y, &x, 1)` in Figure 4 to translate the local source pointer to the destination pointer at GPU 1.

**B. SpTRSV Design with NVSHMEM**

**Challenges in accessing shared memory.** Although NVSHMEM provides support for fine-grained GPU-initiated communication mechanism, if the intermediate data structures for maintaining dependencies and partial sums of SpTRSV are distributed across GPUs evenly and are allocated on the symmetric heap, accessing and updating such data (dependencies and partial sums) across GPUs can still create contention. In this regard, the next challenge in designing SpTRSV is to efficiently update the intermediate arrays (`in.degree` and `left.sum`) without using the system-wide atomic operations. A naive approach is to apply `Get-Update-Put` operations to remotely read the intermediate data from the target PE and then write back the updated value. However, this naive approach introduces data-race hazard when multiple threads compete to update the same value simultaneously. Since NVSHMEM relaxes the total ordering requirement for get operation, to ensure correctness, an `nvshmem_fence` operation is required for each of the get operations to access the shared data. In addition, to ensure completeness of get/put operations of symmetric data objects as well as to ensure visibility of the updates to all the PEs, SHMEM quiet semantics (with `shmем_quiet`) needs to be enforced. However, these requirements are too restrictive. As a result of these restrictions, during the solver phase, only one PE will be able to operate on shared data while others have to wait until the memory is free and visible as Figure 4 shows. Similar to the unified memory approach, the naive approach also suffers from data contention that will adversely affect the performance.

**Read-only Inter-GPU Communication.** To circumvent these restrictions of the naive approach, we propose a read-only inter-GPU communication model to avoid the data race and update the intermediate arrays asynchronously across all the PEs, as shown in Figure 3. On each PE, we allocate two intermediate arrays of size `n` on the symmetric heap to hold the system-wide `in.degree` and `left.sum` (`s.in.degree` and `s.left.sum`), where `n` is equal to the number of solutions. Thus, each PE first accumulates updates locally during system-wide intermediate data update. Once local computation is done, the final intermediate value for a component `x_i` is computed by collecting all system-wide intermediate values of `x_i` from different GPUs by using the asynchronous `get` API. We read the values from different PEs into different threads within the same warp to achieve parallel remote memory access and fully utilize the interconnect bandwidth. To sum the values together, we employ the warp-level parallel reduction mechanism to reduce the complexity of the sum-loop operation from `O(#PE)` to `O(log(#PE))` by using `__shiftdown_sync()` operation.

Algorithm 3 shows the pseudocode of our SpTRSV design with NVSHMEM. In this design, every GPU in the system is considered as one PE and executes the same program to solve the linear system. The algorithm maintains two device-wide intermediate arrays (`d.in.degree` and `d.left.sum`) on the private memory for fast updating intermediate values within the same thread block (Lines 5–8). The algorithm also initializes the system-wide intermediate arrays using `nvshmem_malloc()` API (Lines 9–12). To indicate how many warps have to be finished in advance before each component can proceed to the solver step, the algorithm calculates the system-wide `in.degree` sim-
Algorithm 3: SpTRSV on multiple GPUs with NVSHMEM

Input: col.ptr\(_i\), row.idx\(_{\text{nnz}}\), val\(_{\text{nnz}}\), \(B_n\)
Output: \(X_n\)

1: procedure SpTRSV-NVSHMEM
   2: for all PE do \(\triangleright\) parallel in GPUs
      3: dev.x ← allocate x for device \(\triangleright\) parallel in warps
      4: dev.n ← size of x in device
      5: cudaMemcpy(*d.left.sum, dev.n)
      6: cudaMemcpy(*d.in.degree, dev.n)
      7: cudaMemcpy(*d.left.sum, 0)
      8: cudaMemcpy(*d.in.degree, 0)
      9: nvshmemMalloc(*s.left.sum, n)
     10: nvshmemMalloc(*s.in.degree, n)
     11: Memset(*s.left.sum, 0)
     12: Memset(*s.in.degree, 0)
     13: Get s.in.degree for device x: \(\triangleright\) parallel in threads
        14: d.atomic.incr(&d.in.degree[rid]) \(\triangleright\) parallel in threads
     15: if r.in.degree[d] \(\neq\) 0 then
        16: d.in.degree[d] ← get(s.in.degree[i],d)
        17: x.in.degree[i] ← reduction(r.in.degree[i])
        18: for all \(d \in\) ngpu do \(\triangleright\) parallel in threads
          19: x.in.degree[i] ← x.in.degree[i] - d.left.sum[i] - x.left.sum[i]
        20: end for
     21: end if
     22: x.in.degree[i] ← row.idx[i]
     23: for all \(j \in\) nnz do \(\triangleright\) parallel in threads
       24: if rid ∈ dev.x then
         25: d.atomic.add(&d.left.sum[rid], val[j]*x[i])
       26: else
         27: d.atomic.add(&s.left.sum[rid], val[j]*x[i])
       28: end if
     29: end for
   30: end for

Fig. 6: Grouping components in tasks for effective workload distribution.

to solve the component \(x\) and update the intermediate data locally for its dependents using hybrid memory system (line 28–35). Note that this method still employs device-wide atomic operations to update the intermediate value as multiple updates from different warps of one PE may happen simultaneously.

By employing the read-only inter-GPU communication model to design SpTRSV with NVSHMEM on a multi-GPU platform, we isolate the execution for each PE and avoid page migration cost from data contention and system-wide synchronization compared to the Unified Memory approach.

V. FINE-TUNING WORKLOAD DEPENDENCY

In the previous section, we have discussed the general strategies for reducing contention and exchanging data in SpTRSV, particularly allocating shared data on the symmetric heap and relying on the one-sided communication primitives in NVSHMEM for inter-GPU communication. However, the performance of SpTRSV is still restricted by execution time imbalance arising from dependency disparity across different components (i.e., \(x_i\)).

Static distribution of workload forces GPUs with larger IDs to always wait longer than the smaller ID ones, since the former can only resume work when all the dependencies from GPUs with smaller ID have been met. As we mentioned in Section II because the baseline workload distribution model of multi-GPU system partitions components \(x\), columns of \(L\) matrix and right-hand-side \(b\) and allocates the partitions to each GPUs in the ascending order of the component number, the dependencies among the GPUs are essentially unidirectional. This may negate execution time balance and performance of SpTRSV on multi-GPU systems.

To tackle the unidirectional dependency issue, we propose a fine-tuned task distribution module to utilize the spatial locality of dependent components in SpTRSV on multi-GPU systems. As shown in figure 6, we first divide total components into small component-tasks and group them together based on a user-specified parameter for component count in a component task. Each task has the same number of components \(x\), columns of the \(L\) matrix and right-hand-side \(b\). This process is done during the data distribution. Each task is considered as the smallest unit of workload to schedule. Tasks are allocated to the GPUs in a round-robin order based on the available memory of the GPUs. During the execution of SpTRSV, each...
task is launched as one GPU kernel and the components within the task are assigned to thread warps for parallel execution. Note that, all tasks scheduled on the same GPU share same sets of intermediate arrays in the NVSHMEM global address space. Atomic operations ensure proper updates of the intermediate arrays by different tasks on the same GPU.

Our task distribution module enables scheduling the smaller ID components aggressively so that the waiting time before starting the solvers for larger ID components is reduced. However, finer granularity of tasks lower the amount of components in each kernels and may incur more overhead in kernel launching. In this case, determining optimal number of tasks becomes a new trade-off between fine-grained task scheduling and long kernel scheduling overhead. In our work, we conduct a sensitivity study about this trade-off and we observe that even with a small number of tasks per GPU (e.g. 4 tasks per GPU), our SpTRSV algorithm is able to balance the execution time of each GPU on a multi-GPU system. We present our experimental results in Section VI.

VI. EVALUATION

In this section, we report our experimental results and provide detailed analysis on our proposed SpTRSV design for multi-GPUs system. These include overall performance, sensitivity study for determining the optimal number of tasks to schedule per GPU and scalability of our algorithm with increasing number of GPUs (strong scaling).

A. Experimental Setup

Platform. We implemented our NVSHMEM-based zero-cop SpTRSV with task model using CUDA 10.1 and test it on the NVIDIA V100-DGX-1 and NVIDIA V100-DGX-2 multi-GPU systems. The DGX-1 system is equipped with eight NVIDIA Tesla V100 GPUs with 16GB memory, where GPUs are inter-connected via NVLinks with 64GB/s maximum inter-communication bandwidth. The DGX-2 system is equipped with 16 V100 GPUs where GPUs are all-to-all connected through NVSwitch with around 100GB/s bandwidth per node. The two multi-GPUs system is operated by two 20-Core Intel Xeon E5-2698 v4 CPUs with 512 GB memory. Since NVSHMEM communication only can be initiated between P2P-connected GPUs currently, we perform NVSHMEM implementations on up to 4 GPUs on the DGX-1 system that are fully connected [29]. We used the native mpirun job launcher of NVSHMEM — hydra, to launch MPI processes on each GPU node and execute the GPU kernels for the proposed zero-copy SpTRSV.

Test Matrices. Table I lists the 14 sparse matrices we selected for our experiments. These metrics have been collected from SuiteSparse [30] matrix collection and have been used in previous studies of sparse matrix computations [4], [5], [10], [19]–[24]. We factorized these matrices to generate the sparse L decomposition using MA48 [31] from the Harwell Subroutine Library (HSL) [32] following the approach of the previous work [2]. These matrices cover a variety of application scenarios, as well as a wide range for the size of the components and the number of level-sets as listed in Table I. Two of these matrices, twitter7 and uk-2005, are out-of-memory matrices which have original 21.6GB and 16.8GB input files, respectively. In our design, we first decompose the original matrices and then execute SpTRSV on the generated lower triangular matrices. On average, the intermediate arrays consume 10% of total memory requirement across all matrices in our experiment. For each benchmark, we ran SpTRSV 100 times and report the average execution time.

B. Performance Evaluation

To evaluate the effectiveness of our proposed SpTRSV design, we first compare the performance on a 4-GPU DGX-
1 system under several design scenarios as shown in Figure 7: (i) 4GPU-Unified – the synchronization-free SpTRSV with Unified Memory (Section 3); (ii) 4GPU-Unified+8task – the task-model enabled SpTRSV-Unified with 8 tasks per GPU; (iii) 4GPU-Shmem - the NVSHMEM-based SpTRSV with continued component distribution (Section 4); and (iv) 4GPU-Zerocopy - the proposed task-model enabled zero-copy SpTRSV with 8 tasks per GPU (Section 5). We sum up the execution time of the analysis phase and the solver phase, and normalize the total execution time in each case with respect to the execution time of 4GPU-Unified. From the figure, we obtain several observations.

First, directly imposing the task model on unified memory exacerbates the page fault thrashing problem. Compared to 4GPU-Unified, the performance of 4GPU-Unified+8task reduces by ≈11% on average. This is because with finer granularity of tasks, the number of page faults and data contention increase on multi-GPU system. Second, we observe that 4GPU-Shmem outperforms 4GPU-Unified by about 2.33× on average (up to 8.1×). Using NVSHMEM and the read-only communication model, 4GPU-Shmem successfully avoids the page-fault and page thrashing across the multi-GPU system. Second, we observe that 4GPU-Shmem outperforms 4GPU-Unified by about 2.33× on average (up to 8.1×). Using NVSHMEM and the read-only communication model, 4GPU-Shmem successfully avoids the page-fault and page thrashing across the multi-GPU system. Finally, the proposed design scenario, 4GPU-Zerocopy, improves the overall performance by 3.53× (up to 9.86×) over 4GPU-Unified. In addition, we observe that 4GPU-Zerocopy achieves even better performance for the matrices with higher degree of parallelism (e.g., dc2, nlpkt160, powersim and Wordnet3). This is because with our task model, spatial locality is exploited among dependent components dispatched to the same GPU, achieving better workload balance than 4GPU-Shmem.

Next, we conduct the same experiment on DGX-2 systems where GPUs are connected with different network topologies. Figure 8 shows the performance of multi-GPU SpTRSV on DGX-1 and DGX-2 with 4 GPUs and 8 tasks per GPU. We normalize the result in each case to DGX-1-Unified. From this figure, we observe that the proposed Zero-copy SpTRSV can achieve similar performance improvement (3.53× for DGX-1 and 3.66× for DGX-2) under both systems. Although the DGX-2 system has higher available inter-connection bandwidth than DGX-1, the algorithm achieves similar speedup in both cases. This indicates that our proposed algorithm can effectively overlap communication in the Lock-Wait phase with the computation in the solve-update phase. In this case, the algorithm fully leverages the bandwidth of the communication channels as well as the computing resources of all the GPUs.

C. Sensitivity Study

As mentioned in Section V, the number of tasks per GPU can affect the efficiency of NVSHMEM-based SpTRSV on a multi-GPU system. To understand how the task model impacts the design choice, we examine the workload balance and performance gain of zero-copy SpTRSV under a variety of choices on the number of tasks per GPU.

Figure 9 shows the average performance gain across all benchmarks with different number of tasks when executing zero-copy SpTRSV using 4 GPUs. The performance is normalized to the result of the 4 tasks per GPU scenarios. From the figure, we can observe that due to a better workload balance and performance gain of zero-copy SpTRSV under a variety of choices on the number of tasks per GPU.

Figure 9 shows the average performance gain across all benchmarks with different number of tasks when executing zero-copy SpTRSV using 4 GPUs. The performance is normalized to the result of the 4 tasks per GPU scenarios. From the figure, we can observe that due to a better workload balance, finer granularity of tasks often contributes to the higher performance improvement. Specifically, comparing with 4 tasks per GPU, allocating 16 tasks per GPU can bring on average 22% and up to 78% performance enhancement.

Nevertheless, increasing the tasks number per GPU is not always beneficial for some matrices. For instance, “webbase-1M” attains its best performance (i.e., 69% over 4 tasks) when there are 8 tasks per GPU. With extra tasks, the performance starts to degrade. This is essentially a trade-off: more tasks per GPU leads to finer-grained communication and better
workload balance, but at the same time, suffer from higher scheduling overhead to issue tasks to different GPUs.

D. Scalability Study

We also evaluate the scalability of our design with increased number of GPUs. For the DGX-1 system, since the current NVSHMEM only supports GPUs directly connected (P2P) with NVLinks, we can only implement our NVSHMEM on up to 4 GPUs. For the DGX-2 system, we scale up to 16 GPUs since the GPUs in DGX-2 are all-to-all connected with NVSwitch. We fix the total number of tasks to 32 and normalize the execution time to the single-GPU `csrssv2()` kernel from NVIDIA’s cuSPARSE library.

Figure 10a compares the scalability of our SpTRSV in DGX-1 system with up to 4 GPUs. In addition to the average speedups, we also show the 5 matrices that exhibit distinct characteristics. As can be seen, the proposed zero-copy SpTRSV outperforms the `csrssv2()` thanks to the fine-grained communication, synchronization-free execution [2], and orchestrated load balancing design. On average, zero-copy SpTRSV presents scalable performance improvement, with 34% and 91% speedups using 4 GPUs over 2-GPU and 3-GPU execution, respectively. This is mainly because involving more GPUs in the DGX-1 system increase the computing resources as well as the active communication bandwidth per GPU.

We also observe that the performance of the single-GPU execution is mostly superior than the 2-GPU and 3-GPU execution due to high-speed on-broad communication while some matrices (e.g., Wordnet3 and nlpkt160) exhibit superior performance improvement (e.g., 2.69× from 2 to 4 GPUs). To explore which types of matrices can take better advantage from the increasing number of GPUs, we define a dependency metric as the average non-zero values per component (dependency = NNZ/nRow) and a parallelism metric as the average available components per level (parallelism = nRow/nLevel) for each matrix (as shown in table I). We find that matrices with lower dependency as well as high parallelism can get more benefits from scaling up the number of GPUs.

Figure 10b shows the strong scaling results of the zero-copy SpTRSV on the DGX-2 system with up to 16 GPUs. We observe that the average performance improvement from the increasing number of GPUs for DGX-2 is flatter compared to the scaling results on the DGX-1 system. For such a system architecture where all GPUs are P2P-connected through switches, we observe the active bandwidth per GPU will maintain constant with more GPUs involved.

In summary, the scalability of SpTRSV (e.g., in future systems with a larger number of GPUs) not only depends on the dependency and parallelism metrics for a sparse matrix, but also on the intra-node network design and the signaling technologies.

VII. RELATED WORK

Dependency Elimination for SpTRSV. Concurrent data structures are fundamental building-blocks for real-world applications. Existing works have proposed various novel data structures to handle the dependencies inside SpTRSV [4], [6]–[10], [34]. For better reusing the right-side-hands on Sunway architecture, Wang et al. [4] tile the sparse matrix to control the data flow and explore inter-level parallel for SpTRSV. Ramakrishnan et al. [10] propose a 3D sparse structure to replicate the dependent data for avoiding expensive communication. Comparatively, our framework load from the raw CSC data directly, avoiding unnecessary data-format conversion to a specific data-format. Additionally, our task-pool based inter-GPU communication mechanism is perpendicular to these existing techniques.

One-Sided Communication for SpTRSV. Previous work [12] transmits the dependency values of SpTRSV asynchronously between MPI ranks through one-sided broadcast. Compared to this work, our proposal aims for enabling fine-grained P2P communication across multi-GPUs by exploring the OpenShmem like NVSHMEM which is different from achieving data passing through CPU-based methodology such as MPI. Furthermore, our method achieves synchronization-free value updating by proposing read-only communication as MPI. Furthermore, our method achieves synchronization-free value updating by proposing read-only communication mechanism without pre-analyzing the critical path for matrices.

Communication in Multi-GPU System. There have been multiple works discussing multi-GPU communication technologies [15], [27], [28], [35]–[37]. Some of them [27], [28] conduct architectural optimizations to reduce inter-GPU memory traffic for GPGPU applications, while others present new software API for speeding up remote memory access [15], [35], including the hint API for avoiding page-fault when using the unified memory. However, for SpTRSV, the inner dependency and structural information is data-dependent, and are only known at runtime. Thus, it is not feasible to provide such a hint for pinning specific data in a specific region at development time. As a comparison, our zero-copy SpTrSV approach leverages the latest NVSHMEM library for fine-grained communication and efficient memory sharing, achieving considerable performance advantages.

In addition, targeting multi-node multi-GPU systems, several works [36], [37] leverage CPU to build point-to-point communication for multi-GPU. For example, in the software level, Gravel [36] proposes message queue to pass data to target GPUs while in the hardware-level, GPU DMA [37] builds
a direct access channel between GPU and main memory to share data. Comparing to these works, our work targets single-node multi-GPU platform where the communication channel is directly built among the GPUs. We efficiently leverage the fast inter-GPUs interconnect (e.g., NVLink and NVSwitch) and the latest NVSHMEM library for achieving fine-grained communication towards the complex dependencies of SpTRSV.

VIII. CONCLUSION

In this work, we propose a multi-GPU zero-copy SpTRSV algorithm to effectively handle the inherent dependencies of sparse triangular solver. Employing NVIDIA's latest NVSHMEM technology as the channel to convey fine-grained dependency information among GPUs, we construct a read-only inter-GPU communication model to avoid severe interconnect and memory contention. Additionally, a task-pool execution model is further proposed to balance the workload among GPUs while overcoming the unidirectional dependency challenge. Evaluations on state-of-the-art NVIDIA V100-DGX-1 and DGX-2 platforms demonstrate that our optimized multi-GPU SpTRSV algorithm can achieve on average 3.79× and 3.66× speedup on DGX-1 and DGX-2, with respect to the Unified-Memory design when using 4 GPUs, showing great performance scalability.

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