ReconROS Executor: Event-Driven Programming of FPGA-accelerated ROS 2 Applications

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Abstract—Many applications from the robotics domain can benefit from FPGA acceleration. A corresponding key question is how to integrate hardware accelerators into software-centric robotics programming environments. Recently, several approaches have demonstrated hardware acceleration for the robot operating system (ROS), the dominant programming environment in robotics. ROS is a middleware layer that features the composition of complex robotics applications as a set of nodes that communicate via mechanisms such as publish/subscribe, and distributes them over several compute platforms.

In this paper, we present a novel approach for event-based programming of robotics applications that leverages ReconROS, a framework for flexibly mapping ROS 2 nodes to either software or reconfigurable hardware. The ReconROS executor schedules callbacks of ROS 2 nodes and utilizes a reconfigurable slot model and partial runtime reconfiguration to load hardware-based callbacks on demand. We describe the ReconROS executor approach, give design examples, and experimentally evaluate its functionality with examples.

I. INTRODUCTION

Many robotics applications are computationally very demanding, in particular when they process large amounts of data sensed from their environment and run involved algorithms to compute state information and next actions to take. In the last years, efficient implementations of robotics applications on high-performance embedded platforms comprising multi-core CPUs, general-purpose GPUs, or FPGAs have been studied and several works have shown the potential advantage of FPGAs over CPUs and GPUs with respect to performance, energy consumption, and latency, e.g., [1]–[4].

A key question for FPGA acceleration of robotics applications is how to integrate hardware accelerators into software-centric robotics programming environments. Recently, several approaches targeted the robot operating system (ROS), which is the dominant programming environment in robotics. ROS is essentially a middleware layer that allows for the decomposition of complex robotics applications into a set of nodes that communicate via mechanisms such as publish/subscribe. The nodes can then be distributed over several compute platforms. Most approaches partition a ROS node and map the computation intensive kernels to reconfigurable hardware. A few approaches go further and support the mapping of complete ROS nodes to hardware, which greatly increases flexibility and facilitates design space exploration. However, the mapping of ROS nodes to either software or hardware is static and event-driven programming, which is central to ROS 2, the latest version of ROS, is not supported.

In this paper, we present the ReconROS executor for event-driven programming of ROS 2 applications with flexible hardware acceleration. The ReconROS executor registers ROS 2 node functions as callbacks and dispatches them to run in software on one of several processor cores or in hardware in the reconfigurable fabric. While the executor builds on the architecture and functionality of ReconROS [5], [6], a previously presented open source framework for hardware acceleration in robotics, the main novelty is that the ReconROS executor employs partial hardware reconfiguration with a reconfigurable slot model to load and execute hardware-mapped ROS 2 callbacks on demand, and that it can dispatch callbacks for either software or hardware execution. As a result, ROS 2 developers can exploit the benefits of hardware acceleration from their standard programming environment.

The remainder of the paper is organized as follows: Section II provides background, in particular an overview over ROS and the ROS executor for event-driven programming, and a discussion of related work that aims at integrating FPGA hardware acceleration with ROS. Section III explains the hardware architecture and design concept for the novel ReconROS executor, before Section IV presents an example for the configuration and coding steps when developing a ReconROS application. Section V reports on experiments to demonstrate the functionality and advantages of our approach. Finally, Section VI concludes the paper and gives an outlook to future work.

II. BACKGROUND AND RELATED WORK

In this section, we first introduce to the robot operating system ROS, then focus on the functionality of the ROS executor and, finally, review related approaches for making hardware acceleration available to ROS-based robotics applications.

A. The Robot Operating System

The Robot Operating System (ROS) is the dominant framework for robotics programming. ROS comprises a middleware layer for data communication within a computer network and tools and libraries for rapid and modular development of large and complex applications. ROS decomposes an application
into a set of ROS nodes that can communicate by exchanging messages using three possible mechanisms: An publishesubscribe mechanism and two 1:1 mechanisms denoted as services and actions, that follow a client-server model. Services allow for nodes to access functionalities of other nodes in a manner similar to remote procedure calls, and actions are more elaborate and combine two service requests with a publish-subscribe communication for regular feedback information.

ROS applications are often represented as computation graphs, in which the nodes represent ROS nodes and the edges represent a ROS-supported form of communication [7]. The nodes of a computation graph are then mapped to compute platforms in a distributed system. Figure 1 outlines an example for a computation graph using publish-subscribe communication. The ROS node /camera captures images from a camera and publishes them to the topic /image_raw. The sobel /filter node subscribes to this topic and publishes the filtered images to the topic /image_filtered. The /viewer node displays the filtered images. The second part of the application implements a control loop for servo control, where the node /pid_ctrl runs a PID control algorithm on position sensor input, the node /inv_kinematics determines the required new position and, finally, the node /actor_driver sets the motor signals accordingly.

The most recent version ROS 2 builds on several layers on top of the operating system Linux. As communication layer, ROS 2 uses the data distribution service (DDS), a common standard for publish-subscribe communication specified by the Object Management Group (OMG) [8]. The ROS middleware layer (rmw) in combination with a DDS implementation-specific adaptor in the ROS 2 stack allow for interchangeability of different DDS implementations. There are several different DDS implementations available, e.g., the eProsima FastRTPS or RTI Connext DDS. Additionally, shared-memory based communication between nodes is enabled by, for example, iceoryx. On a higher level, the rcl library comprises the standard framework for providing ROS concepts. High-level libraries (rclcpp for C++ or rclpy for Python) wrap rcl and provide more advanced functionalities, e.g., execution management.

Another key part of the ROS framework is the message infrastructure. Messages can be hierarchically composed out of basic built-in elements such as integers or floats using a common description language. Further, ROS includes standard message packages, e.g., for images or positional data. The ROS tool flow comprises tools for translating such message definitions into data representations suitable for inclusion in high-level language programs in, for example, Python and C++.

B. The ROS 2 Executor

The ROS nodes mapped to one computation platform can execute as Linux processes or threads using the underlying Linux scheduler. In such a case the nodes need to regularly poll the communication layer for available messages. However, the more common model under ROS 2 is the event-driven model, where nodes register callbacks that are executed when specific events occur. There are four categories of callbacks: Callbacks executed by any node when a (periodic) timer event occurs, callbacks executed by a subscriber on a received message, callbacks executed by a ROS 2 service server on a received service request, and callbacks executed by a ROS 2 service client on a received service response.

ROS 2 provides a so-called executor function that interacts with the underlying communication layer and timer infrastructure to catch events and execute callbacks in a run-to-completion mode utilizing one or more worker threads. That is, callbacks are not preempted.

By default, ROS 2 offers standard single-threaded and multi-threaded executors for C++ and Python applications that implements the scheduling algorithm sketched in Figure 2. The algorithm comprises two nested loops. In the outer loop, the executor interacts with the DDS layer to collect all ready subscriber, server, and client callbacks into a readySet. In the inner loop, the executor checks for timer-triggered callbacks and, if such are available, executes them. Then, subscriber, server, and client callbacks are considered in that order and if such a callback is ready, it is executed and removed from the readySet. If there is no more callbacks ready, the next iteration of the outer loop is started after a configurable waiting time.

The ROS 2 executor implicitly implements priorities in the sense that timer-triggered callbacks get high priority, and the other callbacks lower priorities, since they are first collected in the outer loop and then executed in the inner loop in the order shown in Figure 2. Within one callback category, requests are ordered by the sequence of their initial registration at the executor.

The real-time behavior of the ROS 2 executor was studied in [9]. The authors analyzed the response time of ROS 2 applications and provided a scheduling model, a worst-case response time analysis, and general insights into the real-time behavior of ROS 2. In follow-up work [10] the precision of the response time analysis was improved. There are also alternatives to the standard ROS 2 executor. For example, in [11] an executor for micro ROS platforms [11] equipped with embedded micro controllers was presented. This executor is fully coded in C, supports domain-specific requirements, and improves on the analysis of real-time aspects.

C. Related Approaches for ROS-FPGA Integration

In the last years, several approaches have been presented for integrating reconfigurable hardware accelerators into the ROS
Architecture. Most of these approaches partition a ROS software node and map the runtime-intensive parts as acceleration kernels to reconfigurable hardware, while the remaining parts stay on the CPU. The works [12]–[15] follow this model and focus on the automated generation of the interfaces between software and acceleration kernels, the minimization of communication time between them, and the use of high-level synthesis to increase productivity. The ReconROS framework [16] implements shared-memory communication between the software and the acceleration kernels to further reduce communication effort.

A different approach is followed in [17], [18], where one or more complete ROS nodes can be mapped to hardware. All these hardware-mapped ROS nodes connect to an AXI-based gateway followed by a protocol generator and a TCP/IP interface to allow for communication with other ROS nodes of the application. A central manager coordinates the communication between the hardware-mapped ROS nodes and the gateway.

ReconROS [5], [6] also allows for mapping complete ROS nodes to hardware and combines the reconfigurable hardware operating system ReconOS [19], [20] with ROS 2. ReconOS features multithreaded programming with hardware and software threads, i.e., both hardware and software threads use operating system services, such as semaphores and mutexes, in exactly the same way. Additionally, all threads can access the common virtual shared memory address space. ReconROS extends the functionality of ReconOS by adding ROS 2 primitives, turning complete ROS 2 nodes into hardware threads, and allowing them to use the ROS communication mechanisms publish-subscribe, services, and actions. Since the ReconROS architecture and build system are available in open source, we have been using it as starting point for the work presented in this paper.

Industry has also taken up the ROS-FPGA integration. For example, Xilinx develops the KRIA robotics stack [21], [22], which merges ROS build tool flows with the Vitis software platform. There, compute intensive calculations are outsourced to reconfigurable logic as so-called acceleration kernels.

### III. The ReconROS Executor

In the existing ReconROS framework, ROS 2 hardware nodes have to be statically placed in reconfigurable logic where they remain until the application terminates. The hardware nodes run in while(1)-loops, that start with blocking reads for new input data, process the data, and write the output. As main novelty we introduce partial hardware reconfiguration with a reconfigurable slot model to be able to load and execute hardware-mapped ROS 2 nodes on demand, and we devise a ROS 2 executor that can dispatch callbacks for either software or hardware execution, if hardware versions of the callbacks are available.

As a result, (i) robotics application developers can exploit hardware acceleration from their known programming environment and event-driven programming model, and (ii) the limited hardware resources are operated in an efficient manner. In the following, we discuss the hardware architecture and the design concept of the ReconROS executor.

### A. Hardware Architecture

Figure 3 highlights the architecture for ReconROS using our novel ROS 2 executor. According to the underlying ReconOS architecture, the programmable logic part of a platform FPGA contains a set of $n$ reconfigurable slots (RS) that can accommodate hardware threads, which implement the hardware-mapped ROS 2 callbacks. The number and sizes of these reconfigurable slots is application-specific and configured during the design process. Each such reconfigurable slot is connected to an operating system interface (OSIF) for communication with the host operating system Linux running on the processor cores, and to a memory interface (MEMIF) for accessing shared external memory. Another component omitted Figure 3 for simplicity is the memory subsystem that provides arbitration between the MEMIFs and includes a memory management unit to allow the hardware threads to work with virtual addresses.

ROS 2 hardware-mapped callbacks are loaded into reconfigurable slots on demand during runtime with a partial reconfiguration process utilizing the ZyCAP implementation [23]. ZyCAP comprises an ICAP (internal configuration access port) interface and a DMA block on the hardware side, and a Linux kernel driver and user libraries on the software side. Library functions are available to load reconfigurable slots by setting up DMA transfers from external memory to the ICAP interface.

We have chosen ZyCAP over using the processor configuration access port (PCAP) or the ICAP directly for two reasons: First, ZyCAP nominally features $3 \times$ higher performance for writing bitstreams, i.e., 382 MByte/s for the ZyCAP compared to 128 MBytes/s for PCAP [23]. Second, ZyCAP includes a DMA controller that lowers CPU load for partial reconfiguration and, in turn, frees the CPU for executing ROS 2 callbacks. In the hardware architecture, the ZyCAP block is connected to the processing system (PS) via a high
B. Executor Design

The main steps in designing the ReconROS executor are providing timers and coming up with a scheduling or dispatching algorithm, respectively, that utilizes all available processor cores and reconfigurable slots for callbacks.

In the ROS 2 stack, timers are part of the high-level libraries rclcpp (C++) or rclpy (Python) and use the operating system to measure wall clock time. Since ReconROS builds on rcl, the underlying standard framework for ROS primitives, we have added a corresponding timer primitive to that. Our implementation uses the ARM Cortex-A9 global timer (see Figure 3) as its main time reference, and a low-overhead function ros_timer_is_ready() to check whether a time interval has expired.

The development of an executor algorithm is more challenging. In contrast to the standard ROS 2 executor (see Section II-B) that dispatches ready to execute callbacks to a number of identical software worker threads, typically one per available processor core, the ReconROS executor can either execute callbacks in software or hardware and, if executed in hardware, in specified reconfigurable slots. Therefore, our executor implementation is structured into an executor main thread, one software worker thread per processor core, and one hardware worker thread per reconfigurable slot. The main thread maintains four callback lists that include all callbacks registered at the executor, i.e., one for timers, one for subscribers, one for service servers, and the last one for service clients. Each entry in such a callback list comprises a unique identifier, a pointer to the received message in case of non-timer callbacks, and a ResourceMask that contains a field for software and each reconfigurable slot. If the execution mode is software, the corresponding field includes a function pointer to the callback code. If the execution mode is hardware, the corresponding fields contain pointers to callback bitstreams for the reconfigurable slots.

The overall $m$ software and $n$ hardware worker threads are started during the initialization of the executor. Each of these threads implements the inner loop of Figure 2. Figure 4 displays the functionality of the hardware worker thread for reconfigurable slot $x$. The thread accesses the callback lists in the order of timers, subscribers, service servers, and service clients and searches for ready callbacks (CB) with a matching entry $x$ in the ResourceMask. If such an entry is found (CB not zero), the thread checks whether the corresponding bitstream is already loaded in the reconfigurable slot $x$. If so, the callback is simply started; otherwise partial reconfiguration is performed to load the callback bitstream. The worker thread then waits until the callback is finished and runs into the next loop iteration.

The standard ROS 2 executor shown in Figure 2 collects ready non-timer callbacks before entering the inner loop. This ensures that all callbacks collected up to a certain time will actually be executed before new non-timer callbacks are considered. Very frequently appearing subscriber callbacks, for example, can thus not lead to starving callbacks for service servers and service clients. Since our ReconROS executor uses more independent worker threads, we resort to a different
mechanism to avoid starvation. Each worker thread maintains an OffsetVector that holds for each non-timer callback list an entry Position that identifies the callback last served. Whenever the worker thread checks the list for the next ready callback, it starts the search from Position+1. After serving the callback, Position is incremented. Position is initialized with the length of the list and wrapped around to zero when the end of the callback list is reached. Software worker threads are identical, except that they start callback functions in software.

Our ReconROS executor tries to mimic the behavior of the ROS 2 standard executor and requires the designer to specify the size of the reconfigurable slots, and for each hardware callback the possible reconfigurable slots to which the callback can be mapped. Obviously, different and improved ReconROS executor designs are conceivable. For example, for callbacks that can be run in software and hardware, the executor could decide at runtime which mode to choose. Moreover, involved resource management problems arise if the reconfigurable slots are of different size and hardware callbacks are available for different reconfigurable slots. Such improved executor scenarios are left to future work.

**IV. DESIGN EXAMPLE**

As an example we elaborate on the ROS 2 application from Figure 4 comprising six nodes. The ReconROS application from this design example handles the nodes /filter and /inv_kinematics. The remaining nodes are assumed to be developed and compiled with ROS 2 design flows and mapped to other compute platforms.

Both considered ROS 2 nodes comprise subscriber functionality for getting input data. According to the event-based programming approach, callbacks are invoked after the arrival of messages. In this example, the two callbacks are implemented in hardware and designed for execution in a reconfigurable slot.

Listing 1 shows the ROS 2 related part of the ReconROS configuration file for the overall ReconROS design project. The file starts with a block for the specification of the reconfigurable slot, which will accommodate the hardware callbacks. The specification is done by lists of contiguous resources for each type (LUT Slices, DSP, BRAM18, BRAM36). This lists can be derived by drawing phbloks using Xilinx Vivado and reading the resulting constraints. The information for the ROS 2 nodes is organized into so-called resource groups. Lines 6–10 specify the /filter node, beginning with the definition of a rosnode object named "/filter" in line 7. In line 8, the message object of type ROS 2 Image message is defined with further references to a ROS 2 message package (sensor_msgs/msg) and the communication (msg) as well as message types (Image). Lines 9 and 10 declares primitives for the subscription of input data from topic /image_raw and the publication of filtered data to topic /image_filtered.

Lines 12–16 specify the /inv_kinematics node, including the rosnode object named "inv_kinematics". Similar to the /filter node, it comprises a message type definition (here inverse_msg) and a publisher and subscriber for topic /ctrl_out and /tf_out.

Listing 1: Configuration file (Partial reconfiguration / ROS 2 related part) for the RECONROS application shown in Figure 1

Listing 2: C/C++ code (partial) for the HLS implementation of the subscriber callback for the /filter ROS 2 node

In Listing 2, C/C++ code for the HLS implementation of the subscriber callback of the /filter node is presented. The presented code is not performance optimized. The callback starts with accessing the initial data of the callback, which provides a pointer to the message object in main memory. At this point, the message is already in the memory and ready for access. The position of the image data is calculated using the OFFSETOF macro in line 3. Using the resulting pointer, the first use of MEM_READ macro reads the address of the image and then, with the second use of the macro, the callback reads the image into the ram memory within in FPGA. After the execution of the Sobel filter function, the callback writes the filtered image back to main memory via the MEM_WRITE macro. After that, the callback publishes the filtered image by using the node-related publisher.
Listing 3 displays a similar procedure for the /inv_kinematics node, which basically relies on the same procedure as described in Listing 2. Again, the received data from the subscriber is loaded into the FPGA internal memory, processed, and then written back to main memory before publishing to the output topic.

Listing 3: C/C++ code (partial) for the HLS implementation of the subscriber callback for the /inv_kinematics ROS 2 node

```c
1 // Initdata contains pointer to message
2 pMsg = THREAD_GETINITDATA();
3 // Get pointer to ctrl out in memory and
4 // copy it to FPGA-internal memory
5 MEM_READ(pMsg, pPayloadInverse, 4);
6 MEM_READ(pPayloadInverse[0], ram, 4);
7 // Get pointer to resources inverse
8 resourcesinverse_inverse_msg);
9 // Write outputdata to memory and publish result
10 MEM_WRITE(ram, pPayloadInverse[0], 4);
11 ROS_PUBLISHER_PUBLISH(resourcesinverse_pubdata,
12 resourcesinverse_inverse_msg);
13
14 // Init the ReconROS executor without sw workers and one hw worker
15 ReconROS_Executor_Init(&reconros_executor, 0, 1,
16 "mnt/bitstreams/");
17
18 ReconROS_Executor_Add_HW_Callback(&
19 reconros_executor, "/inv_kinematics", 1,
20 ReconROS_SUB, resourcesinverse_subdata,
21 resourcesinverse_inverse_msg);
22
23 ReconROS_Executor_Add_HW_Callback(&
24 reconros_executor, "/filter", 1,
25 ReconROS_SUB, resourcesobel_subdata,
26 resourcesobel_image_msg);
27
28 ReconROS_Executor_Spin(&reconros_executor);
```

The last needed user-created file for this example application is the main file, in which the ReconROS executor is instantiated and configured. The Listing 4 shows the needed steps. In line 2, the ReconROS executor is initialized for execution without sw workers but with one hardware worker using the ReconROS_Executor_Init function. The fourth argument for calling that function is the path to the partial bitstreams in the local filesystem. In line 3–4, the hardware callbacks are registered at the executor. The list of arguments comprises the executor instance, the ROS 2 node name, the ResourceMask, the ReconROS primitive type, the callback-creating ReconROS primitive instance and the ReconROS target message primitive. The last line of the code spins the executor and blocks until the application is terminated.

Listing 4: C/C++ code (partial) main thread of the ReconROS application

```c
1 // Init the ReconROS executor without sw workers and one hw worker
2 ReconROS_Executor_Init(&reconros_executor, 0, 1,
3 "mnt/bitstreams/");
4
5 ReconROS_Executor_Add_HW_Callback(&
6 reconros_executor, "/inv_kinematics", 1,
7 ReconROS_SUB, resourcesinverse_subdata,
8 resourcesinverse_inverse_msg);
9
10 ReconROS_Executor_Add_HW_Callback(&
11 reconros_executor, "/filter", 1,
12 ReconROS_SUB, resourcesobel_subdata,
13 resourcesobel_image_msg);
14
15 ReconROS_Executor_Spin(&reconros_executor);
```

V. EXPERIMENTS

This section reports on experiments to show the functionality of our ReconROS executor. First, we measure the execution times for a set of ROS 2 callbacks. Then, we determine the reconfiguration times for differently sized reconfigurable slots on our platform FPGA. Finally, we present a ROS 2 application comprising a desktop PC and a FPGA board and experiment with three different hardware/software mappings.

A. Callback Execution Times

As a first part of the evaluation of the ReconROS executor, we have measured the runtimes for five ROS 2 nodes, more precisely their callbacks:

- **Sobel filter:** This callback implements a Sobel image filter [24] operating on three channels (RGB) of dimension 640 × 480. The filter applies two filter kernels on each channel of the image and calculates the absolute value of the dot product as an approximation for the geometric mean. The ROS 2 input and output messages are of the type Image from the ROS 2 sensor message package.

- **Number sorting:** This callback provides a ROS 2 service which sorts an array of 32 Bit unsigned integers based on the odd-even transposition sort algorithm [25]. The algorithm is based on a comparator network that employs n stages with n comparisons each to sort n numbers. The ROS 2 node on the PC generates random numbers and publishes messages comprising 2048 numbers as an array.

- **MNIST classifier:** This callback classifies handwritten digits from the MNIST dataset by implementing a neural network. The classifier is implemented using ROS 2 publish / subscribe communication. It subscribes for input images of size 28 × 28 and publishes the estimated digit as unsigned integer. The classifier consists of three convolution layers, three pooling layers and two fully connected layers. The achieved accuracy is about 97%.

- **Inverse kinematics:** This callback computes control signals for driving a servo motor that sets a joint angle based on a desired position and orientation of a robotic manipulation platform. The application is part of a larger mechatronic system for controlling the movements of a Stewart platform [26] with six degrees of freedom. The computation involves coordinate transformations and an iterative implementation of the arctan() function. The ROS 2 input message is an unsigned 32 Bit integer packed with two fixed-point numbers in Q8.6 format that represent the desired rotation angles of the platform around the x-axis and the y-axis. The ROS 2 output messages is also a 32 Bit unsigned integer containing a 10 Bit unsigned integer which is the pulse width coded control signal for the motor.

- **Hash calculation:** The hash calculation callback is implemented for the demonstration of a callback triggered by a periodic timer. At each run, the algorithm reads a 1920 × 1080 image with 24 bit color depth from main memory and calculates its SHA256 hash value. Afterwards, the hash value is published to a ROS 2 topic as an unsigned integer array with 8 elements.

All callback functions have been coded in C/C++ and synthesized with Xilinx Vivado HLS to a Zynq Z7100 on a
TABLE I: Execution times for five ROS 2 callbacks in hardware ($t_{exec-HW}$) and software ($t_{exec-SW}$), and the resulting speedup

| ROS 2 callback          | $t_{exec-HW}$ [ms] | $t_{exec-SW}$ [ms] | Speedup |
|-------------------------|--------------------|--------------------|---------|
| Sobel filter            | 16.50              | 42.00              | 2.5     |
| Number sorting          | 0.85               | 41.00              | 48.2    |
| MNIST classifier        | 11.90              | 16.50              | 1.4     |
| Inverse kinematics      | 0.35               | 1.30               | 4.3     |
| Hash calculation        | 81.00              | 94.00              | 1.2     |

TABLE II: Reconfiguration slots with resources (Z7100 slices LUTs, DSPs, and Block RAMs), bitstream size and reconfiguration time

| Reconfigurable slot     | Slice LUTs | DSPs | Block RAMs | S [Byte] | $t_{rc}$ [ms] |
|-------------------------|------------|------|------------|----------|--------------|
| RS #0                   | 20800      | 160  | 60 / 120   | 2838976  | 24.0         |
| RS #1                   | 20800      | 160  | 60 / 120   | 2838976  | 24.0         |
| RS #2                   | 41600      | 320  | 240 / 120  | 5285728  | 38.4         |
| RS #3                   | 40800      | 280  | 200 / 100  | 4883328  | 36.9         |

B. Reconfiguration Overheads

For quantizing the reconfiguration time, we have created a ReconROS setup with four reconfigurable slots, RS #0, . . . , RS #3. Table II shows the number of available resources per reconfigurable slot, the resulting bitstream size $S$, and the measured reconfiguration times $t_{rc}$ for the four reconfigurable slots.

Using linear regression on the measured reconfiguration times and a reconfiguration time model that includes a constant offset part $t_{offset}$ and a bitstream size dependent part $S/B$, where $B$ denotes the transfer bandwidth, i.e., $t_{rc} = S/B + t_{offset}$, our measurements result in $t_{offset} = 6.8$ms and $B \approx 160 MByte/s$. The achieved bandwidth is much lower than the results reported in [23]. The authors of [23] apparently used a bare-metal implementation of the ZyCAP driver without operating system. Our current implementation suffers from copying the bitstream between user and kernel space. An improved implementation of the Linux driver with a zero-copy approach, e.g., based on get_user_pages, would increase the performance.

The reconfiguration times reported in Table II are directly depending on the size of the reconfigurable slot and the corresponding bitstream size, but they are basically independent on the hardware callback’s functionality. The reconfiguration time adds to the execution time of a hardware callback only if the targeted reconfigurable slot is not yet configured with the required bitstream.

C. Example Application

In the last experiment we compare the performance of a ROS 2 application in software using the standard ROS 2 executor with two different hardware/software mappings using our ReconROS executor. The experimental setup comprises the Zynq Z7100 MiniITX FPGA board and a desktop PC with an Intel i7-8000 series CPU, connected via a Gigabit Ethernet connection. Both platforms run Ubuntu 18.04 LTS with ROS 2 dashing. All software components are compiled with optimization level O3.

The ROS 2 setup is illustrated in Figures 5(a) and (b). On the desktop PC, there are five ROS 2 client nodes programmed in C++ an compiled against the ROS 2 rclcpp library. These client nodes, i.e., the Sort client, Inverse client, Sobel client, and MNIST client nodes, comprise a publisher and a subscriber. Starting with an initial published message, the client’s subscriber waits for a response from the corresponding server node on the FPGA. After receiving a new message for the topic, the clients immediately publish a new message for their server counterpart. The resulting roundtrip times are logged during the experiment. The Hash client node forms a special case. Since the hash server node only publishes messages, the
client on the desktop PC just receives the messages and reports the times between consecutive messages.

Figure 5(a) sketches an all-software mapping, where a multi-threaded standard ROS 2 executor with two software worker threads on the FPGA dispatches the callbacks from the server nodes to two processor cores. Figure 5(b) displays the setup with the ReconROS executor and additional four hardware worker threads that dispatch callbacks to four reconfigurable slots. We have evaluated two mappings under the ReconROS executor, a mixed software/hardware mapping where the four callbacks with the highest speedups according to Section V-A, i.e., Number sorting, Inverse kinematics, Sobel filter, and MNIST classifier, are executed in hardware and the Hash calculation callback is executed in software. The all-hardware mapping finally runs all callbacks in hardware.

Figure 6 analyzes the resulting roundtrip times for the three mappings. The figure plots for each of the five ROS 2 nodes and the three mappings the relative frequency over the roundtrip time. The dashed lines denote the averages. Going from the all-software over the software/hardware to the all-hardware mapping, the speedups based on the averaged roundtrip times are 6.21 an 6.29 for Inverse kinematics, 0.97 and 1.00 for the MNIST classifier, 1.03 and 1.15 for the Sobel filter, 18.18 and 20.97 for Number sorting, and 1.00 for the Hash calculation. Overall, we make the following observations:

- The speedups for the individual ROS 2 nodes within the overall application follow the trends for the callbacks measured in isolation, shown in Table I, although generally lower due to the communication between desktop PC and FPGA board, the ROS 2 communication layers, and the executors. For Number sorting, Inverse kinematics, and to some extent the Sobel filter, distinct speedups are realized.
- The hash calculation is triggered with a 250 ms period. The distribution of roundtrip times shows entries with less and more than 250 ms since the ROS 2 client on the desktop PC measures times between arriving messages from this callback. Some messages are delayed, which then likely reduces the time for the next message.

VI. CONCLUSION AND FUTURE WORK

In this paper, we have introduced the ReconROS executor that enables event-based programming for hardware accelerated ROS 2 applications. In contrast to related work, the ReconROS executor leverages partial reconfiguration for loading hardware-mapped callbacks on demand to predefined reconfigurable slots on the FPGA’s logic resource. Additionally, the ReconROS executor extends the ROS 2 standard executor and allows it to schedule or dispatch callbacks to software and hardware.

In future work, we plan to expand the mapping and scheduling strategies of the ReconROS executor to optimize the hardware/software mapping and the resource management. In particular, callbacks that can run in both software and hardware will allow for taking runtime mapping decisions. With respect to resource management, techniques that minimize the unused resources within loaded slots or preloading of hardware callbacks are worth investigating.

REFERENCES

[1] M. Qasaimeh, K. Denolf, J. Lo, K. Vissers, J. Zambreno, and P. H. Jones, “Comparing Energy Efficiency of CPU, GPU and FPGA Implementations for Vision Kernels,” in Proc. 2019 IEEE International Conference on Embedded Software and Systems (ICESS), 2019, pp. 1–8.
[2] C. Brugger, L. Dal’Aqua, J. A. Varela, C. D. Schryver, M. Sadri, N. Wehn, M. Klein, and M. Siegrist, “A quantitative cross-architecture study of morphological image processing on CPUs, GPUs, and FPGAs,” in Proc. 2015 IEEE Symposium on Computer Applications Industrial Electronics (ISCAIE), 2015, pp. 201–206.
[3] O. Ulusel, C. Piccardo, C. B. Harris, S. Reda, and R. I. Bahar, “Hardware acceleration of feature detection and description algorithms on low-power embedded platforms,” in Proc. 2016 26th International Conference on Field Programmable Logic and Applications (FPL), 2016, pp. 1–9.
[4] S. I. Venieris and C.-S. Bouganis, “FpgaConvNet: Mapping Regular and Irregular Convolutional Neural Networks on FPGAs,” IEEE Transactions on Neural Networks and Learning Systems, vol. 30, no. 2, pp. 326–342, 2019.
[5] C. Lienen, M. Platzner, and B. Rinner, “Reconros: Flexible hardware acceleration for ros2 applications,” in 2020 International Conference on Field-Programmable Technology (ICFPT), 2020, pp. 268–276.
[6] C. Lienen and M. Platzner, “Design of distributed reconfigurable robotics systems with reconros,” ACM Trans. Reconfigurable Technol. Syst., vol. 15, no. 3, dec 2022.

[7] L. Joseph, Mastering ROS for Robotics Programming. Packt Publishing, 2015.

[8] J. Schlesselman, G. Pardo-Castellote, and B. Farabaugh, “Omg distribution service (dds): architectural update,” in IEEE MILCOM 2004. Military Communications Conference, 2004., vol. 2, 2004, pp. 961–967 Vol. 2.

[9] D. Casini, T. Blaß, I. Lütkebohle, and B. B. Brandenburg, “Response-time analysis of ros 2 processing chains under reservation-based scheduling,” in 31st Euromicro Conference on Real-Time Systems (ECRTS 2019). Schloss Dagstuhl-Leibniz-Zentrum fuer Informatik, 2019.

[10] Y. Tang, Z. Feng, N. Guan, X. Jiang, M. Lv, Q. Deng, and W. Yi, “Response time analysis and priority assignment of processing chains on ros2 executors,” in 2020 IEEE Real-Time Systems Symposium (RTSS), 2020, pp. 231–243.

[11] J. Staschulat, I. Lütkebohle, and R. Lange, “The rcl executor: Domain-specific deterministic scheduling mechanisms for ros applications on microcontrollers: work-in-progress,” in 2020 International Conference on Embedded Software (EMSOFT), 2020, pp. 18–19.

[12] K. Yamashina, T. Okhawa, K. Ootsu, and T. Yokota, “Proposal of ROS-compliant FPGA component for low-power robotic systems (retraction notice),” in Proc. International Conference on Intelligent Earth Observing and Applications 2015, vol. 9808, 2015, p. 98082N.

[13] K. Yamashina, H. Kimura, T. Okhawa, K. Ootsu, and T. Yokota, “CREComp: Automated Design Tool for ROS-Compliant FPGA Component,” in Proc. IEEE 10th International Symposium on Embedded Multicore/Many-Core Systems-on-Chip, MCoC 2016. IEEE, 2016, pp. 138–145.

[14] Y. Sugata, T. Okhawa, K. Ootsu, and T. Yokota, “Acceleration of Publish/Subscribe Messaging in ROS-Compliant FPGA Component,” in Proc. of the 8th International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART2017). ACM, 2017.

[15] T. Okhawa, Y. Sugata, H. Watanabe, N. Ogura, K. Ootsu, and T. Yokota, “High level synthesis of ROS protocol interpretation and communication circuit for FPGA,” in Proc. 2019 IEEE/ACM 2nd International Workshop on Robotics Software Engineering (RoSE), 2019, pp. 33–36.

[16] M. Eisoldt, S. Hinderink, M. Tassemeier, M. Flottmann, J. Vana, T. Wiemann, J. Gaal, M. Rothmann, and M. Pormann, “Reconros: Running ros on reconfigurable socs,” in Proc. 2021 Drone Systems Engineering and Rapid Simulation and Performance Evaluation: Methods and Tools Proceedings, ser. DroneSE and RAPIDO ’21. New York, NY, USA: Association for Computing Machinery, 2021, p. 16–21.

[17] A. Podlubne and D. Gühringer, “FPGA-ROS: Methodology to Augment the Robot Operating System with FPGA Designs,” in Proc. 2019 International Conference on ReConFigurable Computing and FPGAs (ReConFig), 2019.

[18] A. Podlubne, J. Mey, R. Schöne, U. Allmann, and D. Gühringer, “Model-based approach for automatic generation of hardware architectures for robotics,” IEEE Access, vol. 9, pp. 140 921–140 937, 2021.

[19] E. Lübbers and M. Platzner, “ReconOS: Multithreaded Programming for Reconfigurable Computers,” ACM Transactions on Embedded Computing Systems, vol. 9, no. 1, pp. 8:1–8:33, 2009.

[20] A. Agne, M. Happe, A. Keller, E. Lübbers, B. Plattner, M. Platzner, and C. Plessl, “ReconOS: An Operating System Approach for Reconfigurable Computing,” IEEE Micro, vol. 34, no. 1, pp. 60–71, 2014.

[21] V. Mayoral-Vilches and G. Corradi, “Adaptive computing in robotics, leveraging ros 2 to enable software-defined hardware for fpgas,” arXiv preprint arXiv:2109.03276, 2021.

[22] V. Mayoral-Vilches, “Kria Robotics Stack,” https://www.xilinx.com/applications/industrial/robotics/wp540-kria-robotics-stack.html, 2021, accessed: 2022-01-13.

[23] K. Vipin and S. A. Fahmy, “Zycap: Efficient partial reconfiguration management on the xilinx zynq,” IEEE Embedded Systems Letters, vol. 6, no. 3, pp. 41–44, 2014.

[24] R. Gonzalez and R. Woods, Digital Image Processing. Pearson, 2018.

[25] D. Knuth, The Art of Computer Programming: Volume 3: Sorting and Searching. Pearson Education, 1998.

[26] D. Stewart, “A Platform with Six Degrees of Freedom,” in Proc. of the Institution of Mechanical Engineers, vol. 180, no. 1, 1965, pp. 371–386.