ABSTRACT The Analytical Full Capacitance Model (AFCM) for amorphous oxide semiconductors thin film transistors (AOSTFTs) is first validated, using a 19-stages Ring Oscillator (RO) fabricated and measured. The model was described in Verilog-A language to use it in a circuit simulator in this case SmartSpice from Silvaco. The model includes the extrinsic effects related to specific overlap capacitances present in bottom-gate AOSTFT structures. The dynamic behavior of the simulated circuit, when the TFT internal capacitances are increased or decreased and for different supply voltages of 10, 15 and 20 V, is compared with measured characteristics, obtaining a very good agreement. Afterwards, the AFCM is used to simulate the dynamic behavior of a pixel control circuit for a light emitting diode active matrix display (AMOLED), using an AOSTFT.

INDEX TERMS Circuit simulator, dynamic model, Verilog-A, capacitances model.
the transistors, as well as variation of the supply voltage, are taken into account.

II. EXPERIMENTAL PART

A photo of one of the fabricated and measured Ring Oscillator (RO), consisting of 19 a-IGZO TFTs inverter is shown in Fig. 1 a). The inverters with a saturated load configuration (stages), are shown in Fig. 1 b). The output buffer circuit consists of an additional inverter with the same configuration. The fabricated load TFTs had a width of $W = 15 \mu m$ and a channel length of $L = 15 \mu m$, while the drivers had a width of $W = 150 \mu m$ with the same channel length of $L = 15 \mu m$.

Figure 2 a) shows the cross section of an a-IGZO TFTs. The gate dielectric layer consists of a stack of $Si_3N_4/SiO_2$, with a thickness of 200 nm and an equivalent dielectric constant of 5.2. The IGZO layer used as semiconductor material is 45 nm thick, with a relative dielectric constant of 9. As metal contacts for $D$, $G$ and $S$, a stack of Mo/Cr was used.

As etch stopper layer (ESL) another stack of $Si_3N_4/SiO_2$ was used. In Figure 2 b), the length of the typical overlap $L_{ov}$ associated to the D/S contacts is indicated, as well as, the top overlap TOV corresponding to the part of the D/S contacts located on top the ESL layer. The effects on the electrical performance of these geometrical overlaps in the devices are considered in the full capacitance model for AOSTFTs reported in [6].

A Keithley 4200 Semiconductor voltage source for the supply voltage, an Agilent Waveform Generator for the input signal and a Tektronix TDS 3032 Oscilloscope were used to obtain the DC, AC and transient measurements of the analyzed circuits.

III. ANALYSIS AND DISCUSSION OF THE RESULTS

The AFCM, including the current-voltage and the capacitance-voltage models [5] and [6], respectively, was described in Verilog-A language, and used in SmartSpice from Silvaco, to simulate the analyzed circuits. As already indicated, the AFCM includes the extrinsic effects of the overlaps on the internal capacitances of the transistors shown in Fig. 2 (b), also allowing the calculation of the internal current through the device capacitances.

The equivalent circuit to represent the TFT with their internal nodes and contacts used in the simulations is shown in Fig. 3. The values of $R_d$ and $R_s$ are used to represent the respective conductance associated to the drain and source contact of the device. As usual, of the 9 capacitances in the device, the most significant for the dynamic behavior of the transistors are $C_{gd}$, $C_{gs}$. To represent the effect of these capacitances in the dynamic regime, the variation of the capacitances with time is calculated as the internal currents ($I_{gs}$, $I_{gd}$) represented as the derivate of the charge associated to the capacitances ($Q_{gs}$, $Q_{gd}$) with respect to the time as (in Verilog-A language):

$$I_{gs} = TYPE \ast ddt(Q_{gs});$$
\( I_{gd} = TYPE \ast \frac{d}{dt}(Q_{gd}); \)
\( I(G, dp) \leftarrow I_{gd}; \)
\( I(G, sp) \leftarrow I_{gs}; \)

The charges \( Q_{GS} \) and \( Q_{GD} \) are calculated as:

\[ Q_{gd} = C_{gd} \ast V(G, dp); \]
\[ Q_{gs} = C_{gs} \ast V(G, sp); \]

where \( dp \) and \( sp \) are the internal nodes of the capacitances for the transistors, as can be seen in Fig. 3.

The extraction of the required model parameters was done as reported in [5], [6], after which obtained parameters were introduced in the simulator. The extracted values are shown on Table 1.

Fig. 4 shows the comparison of the output signal measured and simulated of the saturated load inverter from one of stage of the RO from Fig. 1 a) at \( V_{DD} = 10 \) V.

The maximum voltage that the output signal of our saturated load inverter should ideally reach would be approximately 9.5 V. However, our devices present an output resistance in the order of \( M\Omega \), which causes that a voltage divisor appears between the resistance of the measurement probe of the oscilloscope and the measurement system in general, verified with a Boonton Capacitance Meter.

The dynamic model was also validated using the 19-stages RO from Fig. 1 a). Figure 5 shows the measured and simulated output signal of the Ring Oscillator formed by 19 inverters and one output buffer (additional inverter). The measured oscillation frequency was 22 kHz. The oscillator output signal simulated has an excellent coincidence with the ring oscillator output signal measured.
The effect at different internal capacitance values of the transistors on the oscillation frequency is clearly observed in the simulated output signal. The oscillation frequency is inversely proportional to the inverter delay time, that is, to the capacitance. When \( C_{gd} = C_{gs} \) was increased 1.5 times, the frequency reduced to 17 kHz, as can be seen in the Fig. 6. When \( C_{gd} = C_{gs} \) was reduced to half its value, the frequency, as expected, increased from 22 kHz to 33 kHz.

Since the operation frequency and hence, the propagation delay per stage, are function of the supply voltage \( V_{DD} \), Fig. 7 (a) and (b), show that the oscillation frequency of the circuit increases with the applied \( V_{DD} \), reaching a maximum value around 60 kHz for a \( V_{DD} = 20 \) V.

Finally, we evaluate and compare the dynamic response of the a-IGZO TFT circuit shown in Fig. 8 a). Fig. 8 b) and c) show the simulation of the circuit, which corresponds to a pixel control circuit used in a light emitting diode active matrix displays (AMOLED). The waveforms applied to the transistors follows the specifications for Ultra High Definition resolution on displays given by the pulse width or load time margin \( (t_{cm}) \) applied to the gate of 16 \( \mu s \), for others two \( t_{cm} \) values of 30 and 40 \( \mu s \), in order to determine the maximum load value of the storage capacitor \( (C_{st}) \).

Fig. 8 b) shows the expected behavior of the pixel control circuit for \( t_{cm} \). When the voltage applied to the gate of the transistor commute from a high state to low state the output voltage remains constant. This voltage value is due the capacitor \( C_{st} \) and it is called feedback voltage \((\Delta V)\).

With the aim to see the impact of the capacitor \( C_{st} \) on the dynamic response of the pixel control circuit we obtained by simulation the output voltage of the same circuit at different values of \( C_{st} \) as can be seen in Fig. 8 c). For these simulations
IV. CONCLUSION

Using the AFCM for AOSTFTs described in Verilog-a language we reproduced the dynamic behavior of a 19-stages ring oscillator and a saturated load inverter based on a-IGZO TFTs. In the case of the ring oscillator circuit the model was validated for different supply voltages obtaining the expected behavior of the output signal. The oscillation frequencies obtained for 10 V was 22 kHz, for 15 V was 37 kHz and for 20 V was around 60 kHz. The model was also capable to reproduce the expected dynamic behavior when the internal capacitances values of the transistors were changed. On the other hand, the output voltage for an inverter with a saturated load configuration in both rise time and fall time was obtained with an excellent agreement between the simulated and measured characteristic.

A pixel control circuit for AMOLEDs was simulated. The results obtained were the expected and they were able to describe the behavior of the feedback voltage ($\Delta V$), which is the voltage related to the storage capacitance ($C_{st}$), one of the most important parameters to control in this kind of circuits.

The results obtained in this work are very a good evidence that the AFCM is ready for using in the design circuits based on AOSTFTs.

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