A fourth-order incremental ADC in three-step

Jia-Sheng Huang  |  Shih-Che Kuo  |  Chia-Wei Kao  |  Yu-Cheng Huang
  |  Che-Wei Hsu  |  Chia-Hung Chen

Department of Electrical and Computer Engineering, National Yang Ming Chiao Tung University, Hsinchu 300, Taiwan

Abstract

This letter presents a second-order incremental ADC (IADC) operated in three steps, which extends the performance of a second-order IADC close to that of a fourth-order IADC with only two amplifiers. It performs a second-order noise-shaping quantization in the first step operation. Reusing the same hardware, the circuit is reconfigured to perform fine quantization as a first-order IADC in the second and third step. Within a conversion time of 60 clock periods (oversampling ratio OSR = 60), 35 dB signal-to-quantization-noise ratio is boosted. The proposed topology is very suitable for low-bandwidth high-resolution data conversion.

1 | INTRODUCTION

For low-bandwidth and high-resolution data conversion, incremental analogue-to-digital converters (IADCs) are excellent candidates [1–3]. With a global reset signal, the memoryless IADCs provides the advantages of simpler decimation filter, easy to multiplex, low latency and less idle tone power. To accomplish higher resolution with better energy efficiency, higher-order modulators are usually employed. However, high-order modulators suffer from instability, and the input non-overloading range is much narrower. In this letter, we proposed an IADC in three-step operation. It increases the noise-shaping order by two with the same hardware within the same conversion time.

2 | OPERATION OF SINGLE-LOOP IADCs

Using the same circuitry of ΔΣ ADCs and adding a global reset, the IADCs can process and accumulate a finite length of analogue samples. Figure 1 illustrates a first-order IADC (IADC1), and the simplified timing control. The oversampling ratio (OSR = M) is defined as the numbers of the oversampling clock periods within one conversion period. With the input feed-forward path, the residue voltage is generated by the last integrated stage. The amplitude is bounded by the internal quantization maximum error. With a multi-level quantizer, the modulator can be more stable than 1-bit counterparts. The overall quantization error of a Nth-order L-level IADC [2] and the signal-to-quantization-noise ratio (SQNR) are

$$E_{IADC} \approx \frac{V_{fs}}{L-1} \cdot \frac{N!}{M^N}$$

$$SQNR_{IADC} \approx N \cdot 20 \log(M) + 20 \log(L-1) - 20 \log(N!)$$

To achieve high resolution for a given conversion time, high-order modulation is the preferred approach. However, high-order modulators might be less stable and end up with much narrower dynamic range. In addition, since the different weights of each sampled period, higher-order IADCs suffer from more sampled thermal noise [4]. Figure 2 plots the thermal noise penalty factor against OSR for IADCs of different orders.
3 | PROPOSED THREE-STEP IADC

The z-domain block diagrams of the proposed three-step IADC (IADC211) are illustrated in Figures 3, 4 and 5. The conversion begins with the first step, during which the circuit operates as a conventional second-order IADC (IADC2) for $M_1$ clock periods. The quantization residue is accumulated at $W_2$ in the end of the first step conversion and is ready for fine quantization [2, 5]. Figure 4 shows the second step, and now the residue voltage is hold by the second integrator and delivered to the first integrator. The circuit acts as an IADC1 to covert the residue voltage for $M_2$ clock periods. When the second step finished, another residue voltage at $W_1$ is available for further fine quantization. The third step, shown in Figure 5, reconfigures the same circuits as another IADC1. The two integrators exchange their roles to give the fine quantization. With proper scaling, the digital outputs of three steps are summed as a complete digital code and the quantization error and SQNR can be estimated

$$E_{IADC_{211}} \approx \frac{V_{FS}}{L} \frac{2}{M_1} \frac{1}{M_2^2} \frac{1}{M_3}$$

$$SQNR_{IADC_{211}} \approx 20 \log(M_1^2 M_2 M_3) + 20 \log(L-1) - 4.26$$

The second-order noise-shaping is thus boosted up to fourth-order with the same hardware in the same conversion period (OSR = $M_1 + M_2 + M_3$). The optimal ratio $M_1:M_2:M_3 = 2:1:1$ can be chosen [2] so that the highest SQNR can be achieved for a given OSR. The thermal noise penalty of the fourth-order IADC211 is same as an IADC2. The thermal noise contributed by the IADC1s in the second and third step...
can be negligible when referred to the input of IADC211. It is simple to reconfigure the switched-capacitor circuits among three steps by just enabling or disabling the gate signals of the switches and comparators. The circuitry of the timing generator to switch among the three steps is simple and the simplified timing control diagram is shown on Figure 6.

4 | SIMULATION RESULTS

The proposed IADC211, using a 5-level internal quantizer, is simulated with a -2 dBFS input sine and the spectral are plotted in Figure 7. Total OSR \( M = 60 \), and OSR of each step \( M_1 = 30 \), \( M_2 = 15 \), \( M_3 = 15 \) were chosen. It indicates that the IADC achieves an SQNR of 63.5 dB over a 20 kHz bandwidth during the first step. Then the second and third step enhance the SQNR to 88.4 and 111.7 dB respectively. Figure 8 plots the simulated SQNR against the input amplitude for the three IADCs. With the same OSR (\( M = 60 \)), the proposed three-step IADC is nearly 16 dB and 35 dB higher than the two-step IADC [2] and a single-loop IADC2, respectively. Figure 9 plots the simulated SQNR as a function of errors in the modulator coefficients for each step. It shows that the IADC is more sensitive to the coefficient mismatch of first step, since it introduces error in the coarse quantization. For switched-capacitor circuits, it is not difficult to meet the error requirements about \( \pm 0.5\% \). Figure 10 plots the simulated SQNR of the proposed IADC as a function of the finite opamp gain. It shows that the SQNR begins to degrade when the opamp gain is lower than 75 dB. The simulated INL/DNL is plotted in Figure 11. The \( kT/C \) thermal noise is added in simulation, and the result is relative to 17-bit resolution.

This scheme functions like the multi-stage noise-shaping (MASH) modulators [6] by further quantizing the coarse residue in different period. The key innovation is the hardware reusing to boosts up the SQNR as higher order and remains the stability as a low-order loop. However, comparing to the single loop modulators, the requirements of the hardware become more stringent as the conventional MASH counterparts [6]. For example, as shown in Figures 9 and 10, the coefficient matching is more sensitive and the required opamp gain is higher than the single-loop modulators.

5 | CONCLUSION

An IADC2 operated in three-step operation was proposed. The conversion begins with an IADC2 in the first step. In the second and third step, it is reconfigured as an IADC1 to convert the residue voltage in previous step. For a given OSR, it achieves nearly fourth-order noise-shaping by reusing the same hardware of an IADC2. The simulated SQNR shows 35 dB improvement compared to a single-loop IADC2. The proposed three-step IADC appears to be a highly power-efficient solution for low-bandwidth high-resolution data conversion.
FIGURE 6  Simplified timing diagram for three-step operation

FIGURE 7  Simulated spectral with -2 dBFS input signal for the proposed three-step IADC (IADC211)

FIGURE 8  Simulated SQNR versus the input amplitude for the three IADCs

FIGURE 9  Simulated SQNR loss as a function of errors in the modulator coefficients for each step

FIGURE 10  Simulated SQNR versus the finite opamp gain

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ORCID
Jia-Sheng Huang  https://orcid.org/0000-0002-8955-8021
Chia-Hung Chen  https://orcid.org/0000-0001-7753-1721
FIGURE 11  Simulated INL/DNL in 17-bit resolution

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