Analysis of Using Holes as Carriers in the Film in an 8K Stacked CMOS Image Sensor Overlaid with a Crystalline-Selenium Multiplication Layer

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Abstract A prototyped 8K stacked CMOS image sensor overlaid with a crystalline-selenium-based avalanche-multiplication layer, in which holes are used as traveling carriers in the film, was fabricated. Analysis of energy-band diagrams through the film to the n-type floating-diffusion region revealed that (i) large spot noise in the captured image could be suppressed and (ii) the high voltage required for avalanche multiplication could be applied to the film by using holes as carriers even when defects existed in the film. According to the results of experiments, no large spot noise occurred when the voltage applied to the film was +5 V. Additionally, the photoelectric-conversion current was increased by 1.4 times compared to the saturation-signal level when the applied voltage was +21.6 V. These results confirm charge multiplication in a crystalline-selenium-based stacked CMOS image sensor.

Keywords: 8K, Stacked CMOS image sensor, Avalanche multiplication, Hole, Carrier.

1. Introduction

The demand for high-reality video systems is increasing. Accordingly, 8K Super Hi-Vision (SHV) has been developed as a next-generation ultrahigh-definition TV (UHDTV) broadcasting system for conveying a sense of presence and reality to viewers. 8K SHV regular broadcasting services via satellite has started since 2018. The full-featured 8K SHV system is required to have a 7680(H) × 4320(V) pixel count, 120-Hz frame frequency with progressive scanning, wide color gamut, 12-bit tone reproduction and high dynamic range. A 33-Mpixel 120-fps CMOS image sensor for a full-featured SHV camera has been reported. In addition, high functionality can be achieved by stacking a photoelectric conversion film on a CMOS image sensor, as shown in Fig. 1. Previously, organic photoelectric-conversion films have been used for stacked CMOS image sensors. At FUJIFILM Corporation, stacked CMOS image sensors with organic films have been studied because they bring the advantages of a narrow absorption band, reduced pixel size, and optical advantages of slanting rays of light. At Panasonic Corporation, functions such as high saturation, a global shutter, wavelength selectivity, and wide dynamic range have been reported. A configuration known as a three-transistor pixel circuit is typically used for stacked CMOS image sensors. However, reset noise is large because of incomplete charge transfer from the storage node to the power source of the reset transistor. Feedback-amplifier noise cancellers to suppress reset noise and expand the signal-to-noise ratio have been reported.

Fig. 1. (a) 3D schematic and (b) cross-sectional images of stacked CMOS image sensors overlaid with photoelectric conversion films.
However, the above-mentioned studies did not address enhancing the sensitivity of image sensors, and a breakthrough technology for manufacturing photoelectric-conversion materials is desirable. Avalanche multiplication is an attractive approach for enhancing the sensitivity of image sensors. It is caused by impact ionization of photogenerated carriers due to a strongly applied electric field, and it results in a high internal gain in a photoelectric conversion film. Amorphous selenium (a-Se) has been used as a photoelectric-conversion and avalanche-multiplication layer in a CMOS imager hybridized to an avalanche-multiplication film\(^{18}\). However, a-Se photodetectors suffer from a low long-wavelength spectral response and require a high operating voltage for avalanche multiplication. Because of the high spectral response of crystalline selenium (c-Se)-based photodiodes over the entire visible spectrum, as shown in Fig. 2, c-Se is an attractive candidate for a photoelectric-conversion film. Avalanche multiplication was first observed in a c-Se-based film fabricated on a glass substrate at a relatively low applied voltage, which exhibits high external quantum efficiency of over 100\\%\(^{19}\). However, avalanche multiplication could not be observed on pixel circuits with a silicon substrate\(^{20}\).

This paper is organized as follows. In Section 2, the mechanism of generation of large spot noise is analyzed by drawing the energy-band diagram of the pixel structure in the case that electrons are used as carriers in the film. In Section 3, a mechanism for suppressing large spot noise by using holes as carriers in the film is proposed. In Section 4, device fabrication and the specifications of an 8K stacked CMOS image sensor overlaid with an avalanche-multiplication film are described. The observation of charge multiplication in the film on pixel circuits with a silicon substrate is confirmed. In Section 5, the results of this study are summarized.

2. Mechanism of generation of large spot noise

2.1. Pixel structure and captured image

Fig. 3 shows a schematic cross-sectional image of the pixel structure in a previous stacked CMOS image sensor overlaid with an n-Ga\(_2\)O\(_3\)/p-c-Se heterojunction photodiode\(^{20}\). A 20-nm-thick n-Ga\(_2\)O\(_3\) layer (which acts as a hole-blocking layer), a 300-nm-thick p-c-Se layer (a photoelectric-conversion and avalanche-multiplication layer), and a 30-nm-thick indium tin oxide (ITO) layer (a transparent electrode) are formed on the pixel electrode, which is connected to an n-type floating diffusion (FD) node region through the metal VIA. Pixel circuits are constructed by n-type MOS transistors surrounded by a p-type well on a p-type substrate. A negative voltage, which is the voltage of the ITO electrode (\(V_{ITO}\)) with respect to the reset voltage of the pixel electrode (\(V_{RST}\),
is applied to the film. The traveling carriers in the film are electrons.

**Fig. 4** shows a 4K image captured under dark conditions. Large spot noise is generated. The noise is spread over a wide range of pixels centering on film defects. The voltage applied to the film is –5 V; this is lower than that applied for observing avalanche multiplication, which has not been observed on pixel circuits because of generation of the noise.

### 2.2. Mechanism of generation of large spot noise

The mechanism by which the large spot noise is generated when electrons are used as carriers in the film is analyzed by using an energy-band diagram of the pixels. The method of drawing the energy-band diagram is described in Appendix A.

**Fig. 5** shows the simulated energy-band diagram of the pixel structure along line A-A’ in Fig. 3. The bottom of the conduction band \(E_C\) and the top of the valence band \(E_V\) are shown in the film and silicon regions. The floating-diffusion voltage \(V_{FD}\) is equal to the quasi-Fermi potential of the n-type region, and the ground voltage \(V_{GND}\) is equal to that of the p-type region in silicon. Fermi levels are shown in the ITO electrode and the pixel electrode. \(V_{ITO}\) is –11.7 V, \(V_{RST}\) and \(V_{FD}\) are 3.3 V, and \(V_{GND}\) is 0.0 V, for which the FD-node capacitance is reset. These voltages indicate a relative potential relationship. The voltage applied to the film is –15 V, which is equivalent to \(V_{ITO}\) with respect to \(V_{RST}\). Carrier concentration of holes in the p-c-Se is \(1 \times 10^{16}\) cm\(^{-3}\).

**Fig. 6** shows the simulated energy-band diagram of the pixel structure for which \(V_{FD}\) is 2.3 V. It shows the case in which the film has no defects and the FD-node capacitance is saturated. Electron-hole pairs are generated by incident light, shown by "A" in the figure. Electrons move to the pixel electrode under the electric field in the film and enter the FD-node region. \(V_{FD}\) decreases from \(V_{RST}\) of 3.3 V because electrons have a negative charge, shown by "B". The potential difference of the FD-node capacitance, \(V_{FD} - V_{RST}\), is the signal output. This voltage-fluctuation range is normal if it is within the input range of readout circuits.

**Fig. 7** shows the simulated energy-band diagram of the pixel structure for which \(V_{FD}\) is 0.0 V. It shows the case in which the film has defects and the FD-node capacitance is oversaturated.
capacitance is oversaturated. The potential difference of the FD-node capacitance, \( V_{FD} - V_{RST} \), is larger than the saturation voltage. If defects exist in the film, the resistance of the film decreases, and an excessive current of electrons flows to the ITO electrode from the FD-node region, shown by "A". In addition, \( V_{FD} \) becomes smaller than the saturation voltage, and electrons therefore overflow to adjacent pixels, shown by "B". As a result, large spot noise occurs in the captured image. Furthermore, since a forward bias is applied between the ITO electrode and the p-type substrate, an excessive current flows, shown by "C", and, since a parasitic series resistance exists in a closed circuit in Fig. 3, \( V_{ITO} \) drops. As a result, the voltage necessary for avalanche-multiplication cannot be applied to the film.

3. Mechanism of suppression of large spot noise

3.1. Pixel structure

To prevent large spot noise spreading greatly, a mechanism of suppressing the noise by using holes as carriers in the film is proposed. Fig. 8 schematically shows a cross-sectional image of the pixel structure in our newly-developed stacked CMOS image sensor overlaid with a p-c-Se/n-Ga2O3 heterojunction photodiode. Traveling carriers in the film are holes.

3.2. Mechanism of suppression of large spot noise

Fig. 9 shows the simulated energy-band diagram of the pixel structure for traveling carriers in the film of holes. \( V_{FD} \) and \( V_{RST} \) are 2.3 V and the FD is reset. Fig. 10 shows the simulated energy-band diagram of the pixel structure without a defect for traveling carriers in the film of holes. \( V_{FD} \) is 3.3 V and the FD is saturated. Electron-hole pairs are generated by incident light, shown by "A" in the figure. Signal holes move to the pixel electrode under the electric field in the film. When signal holes enter the FD-node region, \( V_{FD} \) increases from \( V_{RST} \) of 2.3 V because holes have positive charge, shown by "B". Since the potential increases when holes enter, the signal output is inverted from that when electrons are used as carriers in the film. The signal is inverted by an evaluation camera to restore white and
black in the image. This fluctuation range is normal if it is within the input range of readout circuits.

**Fig. 11** shows the simulated energy-band diagram of a pixel structure with film defects for which $V_{FD}$ is 5.3 V and the FD-node capacitance is oversaturated. If defects exist, a large current of holes flows from the ITO electrode to the FD-node region, shown by "A" in the figure. When signal holes enter the FD-node region, $V_{FD}$ becomes larger than the saturation voltage. Because the potential difference between $V_{FD}$ and $V_{GND}$ is increased, electrons, which are the majority carrier in n-type MOS transistors, do not overflow to adjacent pixels, shown by "B". As a result, large spot noise is suppressed. Since $V_{ITO}$ does not drop, $V_{ITO}$ is applied to the set value required for avalanche multiplication. In this state, $V_{FD}$ from $V_{GND}$ is reversed bias, so excessive current does not flow, shown by "C".

### 4. Stacked CMOS image sensor overlaid with avalanche multiplication layer

#### 4.1. Device fabrication

A prototyped 8K stacked CMOS image sensor overlaid with an avalanche-multiplication film was fabricated by using holes as carriers in the film. **Fig. 12** shows the designed layout of the 8K CMOS image sensor, which is the readout-circuit part of the 8K stacked CMOS image sensor on the silicon substrate. A 300-nm-thick a-Se film was deposited in vacuum on the sensor chip, and it was annealed at 200 °C to convert a-Se to c-Se. A 20-nm-thick n-Ga$_2$O$_3$ film was then formed by RF magnetron sputtering, and a 30-nm-thick ITO film was deposited on it by DC magnetron sputtering. **Table 1** shows the specifications of the 8K CMOS image sensor. The optical format is Super35mm, chip size is 32 mm(H) × 25.76 mm(V), total number of pixels is 7816(H) × 4360(V), and number of effective pixels is 7472(H) × 4320(V). The area of test pixels is located as indicated on the far right, and the number of pixels is 208(H) × 4320(V). The pixel size is 3.2-µm square, and the pixel type is a three-transistor configuration. The analog-to-digital converter (ADC) is a two-stage cyclic, with a resolution of 12 bits. The output interface is LVDS 192 lanes. The frame frequency is 60 Hz, and the power consumption is 3.0 W. Digital correlated double sampling circuits are implemented on a board to reduce reset noise.

#### 4.2. Captured image and measured data

**Fig. 13** shows a 4K clipping image captured by the sensor under dark conditions. The number of pixels of

| Item                  | Values                  |
|-----------------------|-------------------------|
| Optical format        | Super35mm               |
| Chip size             | 32 mm(H) × 25.76 mm(V)  |
| Number of total pixels| 7816(H) × 4360(V)       |
| Number of effective pixels| 7472(H) × 4320(V)     |
| Number of test pixels | 208(H) × 4320(V)        |
| Pixel size            | 3.2 µm × 3.2 µm         |
| Pixel type            | 3 transistors           |
| ADC type              | 2-stage cyclic          |
| ADC resolution        | 12 bit                  |
| Output interface      | LVDS 192 lanes          |
| Frame frequency       | 60 Hz                   |
| Power consumption     | 3.0 W                   |
the sensor including test pixels is 8K. The output image is divided into four 4K resolution images by the output interfaces of the evaluation camera. The voltage applied to the film is +5 V. Defects occur in the film regardless of whether the carriers in the film are electrons or holes; the difference between using electrons and holes as carriers is how spot noise spreads. When electrons are used as carriers, small spot noise of film defects is spread widely and roundly in the captured image, as shown in Fig. 4. However, when holes are used as carriers, film defects become small spot noise, which does not spread in the captured image. Therefore, the large spot noise that occurred when electrons were used as carriers is suppressed by using holes. Fig. 14 shows an example of a 4K clipping image captured by the 8K stacked CMOS image sensor. A good 4K image of a skin-color chart with no large spot noise is captured.

Here, the observation of charge multiplication on pixel circuits is described. Since suppressing large spot noise prevents an excessive current from flowing, $V_{THO}$ can be applied as the voltage required for generating charge multiplication. Fig. 15 shows the dependences of photo-current and dark current on voltage applied to the film. The photo-current is calculated by subtracting the measured current under dark conditions from the measured signal current when light is irradiated. The photo-current is saturated when the applied voltage is +15.6 V. It is confirmed that the photo-current at the applied voltage of +21.6 V is approximately 1.4 times higher than that when the applied voltage is +15.6 V. Thus, charge multiplication was observed in the film on pixel circuits with the silicon substrate.

There are two types of photoconductive target layer: the injection type and the blocking type. In the case of an injection target layer, a high quantum efficiency of greater than unity can be obtained, but it suffers from the disadvantages of a time lag and a high dark current. A blocking target layer has the advantage of high sensitivity, which is greatly in excess of unity quantum efficiency at a high target voltage by using the avalanche multiplication mode. Fig. 16 shows the avalanche-multiplication mechanism, which is discussed hereafter. Electron-hole pairs are generated by photoelectric conversion. If the electric field is high, the electrons and holes move with increasing kinetic energy and acquire sufficient kinetic energy before their collision with the lattice. Another electron-hole pair is generated by the collision, and that phenomenon is called "impact ionization". The effect of the avalanche multiplication of carriers is caused by impact ionization on the current through a semiconductor device. As shown in Fig. 9, a c-Se avalanche-multiplication layer is fully depleted at the applied voltage of +15 V, and as shown in Fig. 15, charge multiplication is observed at the applied voltage of +21.6 V. Although the dark current increases, the mechanism of charge multiplication limits the dark current.
generation of electron-hole pair by impact ionization

Fig. 16 Mechanism of avalanche multiplication by impact ionization.

Multiplication is thought to be avalanche multiplication. As shown in Fig. 9, the potential barrier for electron between the c-Se layer and the pixel electrode is small. Since a high electric field is applied to the c-Se layer, the effective potential-barrier width becomes narrower. Consequently, electrons can flow from the FD-node region to the ITO electrode as a dark current. We will attempt to reduce the dark current by inserting an electron-blocking layer between the avalanche-multiplication layer and the pixel electrode. That layer is expected to increase the multiplication factor by increasing the electric field applied to the film.

5. Conclusion

An 8K stacked CMOS image sensor over laid with an avalanche-multiplication film was fabricated. Large spot noise was found to be generated when electrons were used as carriers in the film. A mechanism of preventing this large spot noise, namely, using holes as carriers in the film, was proposed. The structure and bias voltage of the avalanche-multiplication film were changed so that holes instead of electrons act as carriers in the 8K stacked CMOS image sensor. When a voltage of +5 V was applied to the film, no large spot noise occurred in the image captured by the sensor. Charge multiplication was observed in the film on pixel circuits with the silicon substrate when the applied voltage was +21.6 V.

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Appendix

A. Method of drawing energy-band diagram

Poisson’s equation is given by
\[
div(\varepsilon \text{grad}(V)) + q(p - n + N_D - N_A) = 0
\] (1)

where \( V \) is potential, \( \varepsilon \) is dielectric constant, \( q \) is elementary charge, \( p \) is hole concentration, \( n \) is electron concentration, \( N_D \) is donor concentration, and \( N_A \) is acceptor concentration. The carrier-continuity equations are given by
\[
\frac{dn}{dt} + div(\mu_n n \text{grad}(V) - D_n \text{grad}(n)) - GR = 0
\] (2)
\[
\frac{dp}{dt} - div(\mu_p p \text{grad}(V) + D_p \text{grad}(p)) - GR = 0
\] (3)

where \( \mu_n \) is electron mobility, \( \mu_p \) is hole mobility, \( D_n \) is electron-diffusion coefficient, \( D_p \) is hole-diffusion coefficient, and \( GR \) is generation-recombination rate. Relationships between the carrier concentration and potential are given by
\[
n = n_i \exp\left(\frac{q(V - V_n)}{kT}\right)
\] (4)
\[
p = n_i \exp\left(\frac{q(V_p - V)}{kT}\right)
\] (5)

where \( n_i \) is intrinsic carrier concentration, \( V_n \) is the quasi-Fermi potential of an electron, \( V_p \) is the quasi-Fermi potential of a hole, \( k \) is Boltzmann’s constant, and \( T \) is absolute temperature.

The solution to Poisson’s equation is shown below. The relationship between grid points I and J on axes I and J is shown in Fig. A1.

The following normalization (6) is incorporated in a program:
\[
kT/q = 1, n_i = 1, q/\varepsilon = 1
\] (6)

Electric field \( E_j \) acting on the area surrounded by grid points I and I-1 is expressed by potentials \( V_I \) and \( V_{I-1} \) and interval \( \delta x \) as
\[
E_j = -\frac{V_I-V_{I-1}}{\delta x}
\] (7)

The difference in the electric fields, \( E_{j+1} - E_j \), is derived from the space charge stored in the region represented by grid point I. It is represented by hole concentration \( p_I \), electron concentration \( n_I \), donor concentration \( N_{D,j} \), and acceptor concentration \( N_{A,j} \) at grid point I by
\[
E_{j+1} - E_j = (p_i - n_i + N_{D,j} - N_{A,j}) \delta x
\] (8)

From Equations (7) and (8), Poisson’s equation is represented by
\[
-\frac{(V_{j+1} - V_j)}{\delta x} - \frac{(V_j - V_{j-1})}{\delta x} = \left( p_i - n_i + N_{D,j} - N_{A,j} \right) \delta x
\] (9)

Equation (9) is transformed to
\[
-V_{j-1} + 2V_j - V_{j+1} = \left( p_i - n_i + N_{D,j} - N_{A,j} \right) \delta x^2
\] (10)

The approximate solution of the potential is defined as \( V_{j} \), and the error is defined as \( \delta V_{j} \). Since \( n_i \) and \( p_i \) are strongly dependent on potential \( V_{j} \), the first-order Taylor expansion is applied to Equation (10):
\[
-(V_{j-1} + \delta V_{j-1}) + 2(V_j + \delta V_j) - (V_{j+1} + \delta V_{j+1}) = \left( p_i + \frac{dp}{dV} \delta V_j \right) - \left( n_i + \frac{dn}{dV} \delta V_j \right) + N_{D,j}
\] (11)

Equation (11) is transformed to
\[
-V_{j-1} + \left[ 2 - \left( \frac{dp}{dV} \right) \delta V_j \left( \frac{dn}{dV} \right) \delta V_j \right] \delta V_j - \delta V_{j+1} = \left( p_i - n_i + N_{D,j} - N_{A,j} \right) \delta x^2
\] (12)

The following approximation of the thermal-equilibrium state holds even in the non-thermal equilibrium state:
\[
\frac{dn}{dV} = n, \text{ from } n = \exp(V - V_n)
\] (13)
\[
\frac{dp}{dV} = -p, \text{ from } p = \exp(V_p - V)
\] (14)
Equations (13) and (14) are used to express Equation (12) as

\[-\delta V_{i-1} + [2 + (p_i + n_i)\delta x^2]\delta V_i - \delta V_{i+1} = V_{i-1} - 2V_i + V_{i+1} + (p_i - n_i + N_{Df} - N_{Af})\delta x^2 \]  \hspace{1cm} (15)

The solution to the tridiagonal matrix for \(\delta V_i\) is calculated from \(V_i\):

\[V_i + \delta V_i \rightarrow V_i \]  \hspace{1cm} (16)

By repeating the substitution of Equation (16), the distribution of \(V_i\) in the film is calculated. \(E_C\) and \(E_V\) are 3.5 and 5.3 eV in c-Se, and 3.3 and 8.1 eV in Ga\(_2\)O\(_3\), respectively. Since the film is fully depleted, \(E_C\) and \(E_V\) are calculated from the distribution of \(V_i\) in the film. The distribution of \(V_i\) in the silicon is extracted from a device simulator. \(E_C\) and \(E_V\) are calculated from the distribution of \(V_i\) in the silicon. The pixel electrode under the film and that on the silicon are joined so that they have the same Fermi level.