Understanding the role of threading dislocations on 4H-SiC MOSFET breakdown under high temperature reverse bias stress

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Abstract
The origin of dielectric breakdown was studied on 4H-SiC MOSFETs that failed after three months of high temperature reverse bias stress. A local inspection of the failed devices demonstrated the presence of a threading dislocation (TD) at the breakdown location. The nanoscale origin of the dielectric breakdown was highlighted with advanced high-spatial-resolution scanning probe microscopy (SPM) techniques. In particular, SPM revealed the conductive nature of the TD and a local increase of the minority carrier concentration close to the defect. Numerical simulations estimated a hole concentration 13 orders of magnitude larger than in the ideal 4H-SiC crystal. The hole injection in specific regions of the device explained the failure of the gate oxide under stress. In this way, the key role of the TD in the dielectric breakdown of 4H-SiC MOSFET was unambiguously demonstrated.

Keywords: dielectric breakdown, threading dislocation, 4H-SiC, power MOSFET

(Some figures may appear in colour only in the online journal)

Introduction
Silicon carbide (4H-SiC) is a suitable material for high power and high temperature electronics [1]. In particular, metal oxide semiconductor field effect transistors (4H-SiC MOSFETs) are desired in automotive applications, as they guarantee a better efficiency in power conversion [2]. In this context, the 4H-SiC MOSFETs instability during long term interdiction under high temperature reverse bias stress (HTRB) is object of intensive investigations [3–5].

Since 4H-SiC MOSFETs are typically fabricated using SiO₂ as a gate insulator, one would expect a breakdown kinetics similar to the SiO₂/Si system. However, the breakdown kinetics of the SiO₂/4H-SiC system is more complex. In fact, while the behaviour of thin thermal gate oxides obeys to the percolation theory [6, 7], for oxide thickness exceeding 10 nm, a deviation from the percolation theory is observed and explained by the presence of carbon-related defects in the oxide [8, 9].

Premature failure for SiO₂/4H-SiC system, i.e. breakdown at zero time, has been often attributed the presence of crystalline killer defects (pipes, carrots, bars, etc) [10], and to the step-bunching on the 4H-SiC surface [11, 12]. However, the role of other crystalline defects is still controversial. In particular, it is still unclear whether threading dislocations (TDs) (threading screw dislocations (TSDs) and threading edge dislocations (TEDs)) behave as killer defects in 4H-SiC MOSFETs. Indeed, these crystalline defects have been blamed [13, 14] and absolved [15, 16] of causing premature device breakdown.

It should be pointed out that literature studies on the breakdown kinetics are typically based on the characterization of small MOS capacitors, which are unlikely to represent the behaviour of real power MOSFETs (i.e. having a larger area and a different geometry). In addition, due to the nanoscale...
size of the TDs and the large area of power MOSFETs, only local analyses based on advanced high-spatial-resolution techniques can enable to explain the origin of the breakdown in real devices.

This paper reports a clear correlation between TDs and dielectric breakdown (BD) on 4H-SiC planar MOSFETs, by the use of several advanced nanoscale electrical and structural characterization techniques. In fact, since the TDs appear on the 4H-SiC as narrow spot-like defect having a radius < 100 nm, only high-spatial-resolution measurements can provide useful insights on the physics involved in the device failure. Furthermore, numerical TCAD simulations explained the impact of the TD in terms of electric field and minority carrier distribution.

**Experimental details**

Several hundreds of 4H-SiC MOSFETs, designed to operate at 650 V, were stressed in a HTRB test at 140 °C and $V_{DS} = 600$ V for $10^7$ s (three months). The population of devices that survived to the stress test was a large fraction (98%) of all the tested devices. The remaining 2% of failed devices—showing a high slope in the Weibull distribution—was studied to understand the origin of the long time HTRB ‘intrinsic’ failure mechanisms.

The fabrication starts from zero-micropipe production grade $n^+$ substrates followed by CVD epitaxy process. After the growth of the epitaxial layer (Nitrogen doping of about $10^{16}$ cm$^{-3}$), the concentration of threading dislocation is about hundred per squared centimetre. The MOSFET body material is fabricated by ion implantation of aluminium (about 1017 cm$^{-3}$). The 45 nm thick SiO$_2$ layer is deposited and then subjected to a post deposition annealing. The metal gate is fabricated by n-type poly-silicon.

The HTRB test was performed using an Infinity 1000 Qualitau Equipment, able to collect simultaneously the current flows for each device. This capability is fundamental to distinguish the failed device and to record the information on each single BD event, defined from the abrupt increase of the gate current.

First, a PHEMOS1000 Emission microscopy (EMMI) was used to identify the coordinates of the breakdown event and a focussed ion dual beam (FIB) to mark the position of the breakdown. Afterward, the devices were completely delayered to expose the 4H-SiC bare surface. The delayering is obtained by dicing the device out of package in a HF acid 40%-solution for 20 min. Nanoscale resolution current and capacitance mapping on the 4H-SiC surface were carried out by conductive atomic force microscopy (C-AFM) and scanning capacitance microscopy (SCM), respectively, using a DI3100 AFM by Veeco equipped with a Nanoscope V controller. Transmission electron microscopy (TEM) were performed using a Hitachi HD2300 STEM operated at 200 kV. Current–voltage ($I-V$) measurements were carried out using an Agilent B1505A parameter analyser. Numerical simulations of the electric field and carrier concentration were performed using Silvaco TCAD tools.

**Results and discussion**

Figure 1(a) reports the gate current as a function of the HTRB stress time at 140 °C and $V_{DS} = 600$ V, showing the abrupt increase of the current at the breakdown. It has to be remarked that the sharp gate current increase shown in figure 1(a) demonstrates that the breakdown event occurred in the gate insulator. Figure 1(b) compares the $I_{G}-V_{G}$ characteristic of the failed device with that of a reference device survived to the HTRB test. As can be seen, the failed device shows a degradation of the output characteristics, as the drain current cannot be modulated by the gate bias after the HTRB. By repeating three times the $I_{G}-V_{G}$ ($V_{DS} = 0.5$ V) transfer characteristics (figure 1(c)), the failed device shows a shift of the transfer characteristics, indicating the occurrence of a charge trapping. The presence of charge trapping is also responsible for the behaviour of the $I_{G}-V_{G}$ characteristic shown in figure 1(d), where a significant increase of the gate current is observed at $V_{G} > 2$ V for the failed device. It is worth noting that during the HTRB some trapping phenomena occurred. In fact, the gate current at fixed bias (figure 1(a)) decreases with increasing the HTRB time, thus indicating the occurrence of holes trapping in the oxide layer until the hard breakdown occurs. In particular, during HTRB holes are accumulated at the SiO$_2$/4H-SiC interface and they can be injected in the oxide via Fowler–Nordheim (FN) tunnelling [17].

After the HTRB test, the breakdown spot was identified by EMMI (figure 2(a)) and marked with a FIB cut. After the complete device delayering, the bare 4H-SiC surface in the FIB mark was investigated by SEM, revealing the presence of a triangular features having the vertex in the centre of the JFET region (figure 2(b)).

The nature of the defect found at the breakdown spot was clarified by means of TEM analysis. In fact, TEM in cross section (figure 3) allowed to identify a threading dislocation (TD) running along the epitaxial layer. The TEM dual beam investigation demonstrated the coexistence of a contrast in the images obtained using the transmitted beam and the diffraction spots [18] alternatively on the parallel and on the orthogonal directions to the surface—along the directions [11–19] and [0002]—as shown in figures 3(a) and (b). This is a proof of the mixed nature of the TD under investigation. In fact, the dislocation shows up with the [11–19] spot (edge) and with the [0002] spot (screw).

To explore the electrical behaviour of the TD, a nanoscale electrical characterization was carried out using the conductive atomic force microscopy (C-AFM) [11]. In particular, C-AFM allowed determining the morphological shape of the surface (figure 4(a))—a triangle with the vertex in the [11–19] direction—about 25 nm deeper than the surface of the JFET region where it is located. Even in the triangular region (highlighted with a dashed line), the surface conductivity is rather homogeneous (figure 4(b)). Noteworthy, the current is at least two orders of magnitude larger on the isosceles triangle vertex, i.e. where the TD is reaching the surface (figure 4(b)). Hence, the electronic transport properties close
to the TD (radius <100 nm) are significantly different from the surrounding material.

Then, local capacitance mapping [19] was performed using the SCM. During the surface scan with the metal tip, a modulating bias with amplitude $\Delta V$ at 100 kHz frequency is applied to the sample and the capacitance variation $\Delta C$ in response to this modulation is recorded with the SCM sensor.

Figure 1. (a) MOSFET gate current versus time under HTRB at $V_{DS} = 600$ V at 140 °C. (b) Comparison of the $I_{DS}$—$V_{G}$ collected on a fresh reference device and a failed HTRB device. (c) Comparison of hysteresis loop of the $I_{DS}$—$V_{G}$ ($V_{DS} = 0.5$ V) collected on a fresh reference device and a failed HTRB device. (d) Comparison of hysteresis loop of the $I_{G}$—$V_{G}$ collected on a fresh reference device and a failed HTRB device.

Figure 2. (a) EMMI micrograph showing the location of the breakdown (BD) event. (b) SEM micrograph showing the delayered MOSFET, revealing the presence of epitaxial defect in the JFET region.

Figure 3. (a) Cross section transmission electron microscopy in 2-beams configuration [11–19]. (b) Cross section TEM in 2-beams configuration [0002].

Besides the SCM signal amplitude $|\Delta C|$, which is related to the net active dopants concentration $N_{A} - N_{D}$ in the semiconductor underneath the tip, also the phase signal is recorded, which is very sensitive to the type of majority carriers in...
the region underneath the tip. Figures 4(c) and (d) show the maps of the $\Delta C$ amplitude and phase measured in the same region where the C-AFM (figure 4(b)) was collected. The amplitude is not affected by the presence of the defect, thus indicating no significant variation of dopants concentration in the defect region. On the other hand, a difference in the phase map is observed between the triangular region and the rest of the n-type doped JFET area. As discussed in the following, this change in the phase signal can be ascribed to an increase of the density of minority carriers (holes) in this region.

Using the Read’s model [20], Chung et al [21] considered the TD in the JFET n-type semiconductor region as a core containing acceptor-type states capable of trapping electrons, leading to a negatively charged dislocation core. They supposed the charge screened by a positive space charge in a cylindrical configuration of ionized donors. However, according with the SCM experimental data, the real scenario seems to be more complex. Figure 4(e) schematically describes the non-cylindrical space charge distribution found in the TD region. On the left side—in the centre of the JFET region—an electron accumulation (blue colour) is demonstrated. On the other hand, inside the triangular region (green colour), a hole (minority carrier) accumulation produces a SCM phase variation that maintains the charge neutrality. Clearly, the TD produces a variation in the local electronic structure of the JFET region of the MOSFET.

The electronic structure of the TD has been theoretically investigated in literature [22, 23]. Łazewski et al [23] employed density functional theory methods to calculate the energy levels and the effective band gap of the TD. Accordingly, inside the TD some additional localised broad states appeared, producing an effective reduction of the magnitude of the insulating gap. In particular, the TD possesses an identical conduction band edge but the effective band gap results approximately one forth smaller than in 4H-SiC, i.e. the valence band edge of the TD is 0.8–1 eV higher than in 4H-SiC. We used this information to quantify the impact of a TD located in the centre of the JFET of our MOSFET in HTRB configuration.

Figure 5 shows the 3D schematic of a power MOSFET having a cylindrical TD of radius 10 nm in the centre of the JFET region. The band gap of the TD is assumed to be 2.3 eV with a common $E_C$ value but with a $E_V$ 1 eV higher than the defect-free 4H-SiC. Figure 6(a) shows the cross section on the...
electric field distribution inside the MOSFET unitary cell in HTRB configuration (at $V_{DS} = 600 \text{ V}$), calculated using TCAD simulations. A cross section on the SiO$_2$ gate insulator at 25 nm from the physical interface (figure 6(b)) shows that the oxide electric field increases from the channel region toward the JFET region reaching its maximum ($\sim 4.6 \text{ MV cm}^{-1}$) at the edge of the unitary cell. To understand the TD behaviour inside the JFET region, the oxide electric field was calculated in both the ideal (reference) structure and in the structure containing the TD. A zoom in the centre of the JFET region reveals an increase of the oxide electric field of about 0.3% with respect to the reference ideal structure (inset in figure 6(b)).

The higher valence band offset and the lateral confinement of the TD produces the creation of a quantum well. Considering the ideal conduction contribution—i.e. the ideal FN tunnelling [24] and the quantum confinement that inhibits the FN tunnelling from the bottom of the quantum well [25]—the oxide electric field produces a minor increase of the hole current through the insulator layer. Besides the calculated increase of the electric field due to the TD band gap narrowing, also the surface morphology plays a role [12]. However, this local increase of the oxide electric field should not be prominent, as an acceleration of the breakdown kinetics would result in the MOSFET failure in a short time. It has to be emphasized that in the ideal case, a reduction of the TDs will produce a benefit in terms of the power MOSFET gate oxide reliability.

The band gap narrowing produces a quantum well for holes (‘hot spots’) that are collected from the surrounding 4H-SiC material (figure 6(c)). Hence, TD quantum well becomes a source for hot holes injection into the insulated (figure 6(c)). In fact, the calculated intrinsic carrier concentration ($n_i$) and holes concentration ($n_h$) increase in the TD of several orders of magnitude. Figure 6(d) shows that the electron density ($n_e$) increases in the MOSFET profile following the electric field profile (figure 6(b)) while an abrupt increase of 13 and 9 orders of magnitude for $n_h$ and $n_e$ respectively is found.

It is well known [26], the intrinsic carrier concentration exponentially depends on the band gap amplitude. Assuming that the doping concentration in the TD is unchanged—in agreement with the SCM amplitude signal (figure 4(c)—the holes concentration can be written as:

$$n_h = n_i \exp \left( -\frac{E_i - E_F}{kT} \right),$$

where $n_i$ is the intrinsic carrier concentration (that is exponential function of the band gap), $E_i$ is the intrinsic energy level, $E_F$ is the Fermi level, $k$ is the Boltzmann constant and $T$ is the temperature.

The local holes confinement can accelerate the oxide degradation. This demonstrates that the premature BD is not due to an intrinsic insulator weakness but the local variation of the semiconductor electronic properties in the presence of the TD in the JFET region.

**Conclusion**

Nanoscale structural and electrical investigations were carried out on large area power MOSFETs to clarify the role of the threading dislocation in the 4H-SiC epitaxial layer on the dielectric breakdown under high temperature reverse bias operation. The nanoscale inspection at the breakdown location of failed devices always revealed the presence of a threading dislocation. Hence, we can conclude that TDs have a major role on the origin of the breakdown. Furthermore, C-AFM revealed an enhanced conductivity inside the TD. High-spatial-resolution SCM revealed a triangular spatial charge distribution surrounding the TD, compatible with a local band gap narrowing and an increase on the minority carrier concentration, 13 orders of magnitude larger than in the 4H-SiC bulk. Hence, the TD behaves as hot spot with a high concentration of holes that accelerate the breakdown kinetics.

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