Performance Assessment of Dual Material Stack Gate Oxide TFET using Dielectric Pocket

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Abstract This paper investigates the impact of low-K and high-K dielectric pockets on DC characteristics, analog/RF, and linearity performance of dual material stack gate oxide-tunnel field-effect transistor (DMSG-DP-TFET). For this, a stack gate oxide with work-function is considered to enhance the ON-state current (I_{ON}), lower ambipolar current (I_{amb}) and lower the subthreshold swing. For this case, the gate electrode is tri-segmented, named as tunnel gate (M_1), control gate (M_2) and auxiliary gate (M_3) with different gate lengths (L_1, L_2, L_3) and work functions (\phi_1, \phi_2, \phi_3), respectively. To maintain dual-work functionality, the possible combinations of these work functions are considered. Technology computer-aided design (TCAD) simulations are performed and noted that the workfunction combination (\phi_1 = \phi_3 < \phi_2) outperforms as compared to other combinations. Where \phi_3 on the source side is used to enhance the I_{ON}, while \phi_3 (equal to \phi_1) is used on the drain side to minimize the I_{amb}. To further enhance the device performance, a high-K dielectric pocket is considered at the drain junction to suppress the I_{amb} whereas, a low-K dielectric pocket is employed at the source junction to enhance the I_{ON}. Moreover, length of gate segments, dielectric pocket height, and thickness are optimized to achieve a better switching ratio, subthreshold swing (SS) and reduce the I_{amb} which helps in the gain of device and design of analog/RF circuits. The proposed device as compared to dual material control gate-dielectric pocket-TFET (DMCG-DP-TFET) with SiO_2 gate oxide shows improvement in I_{ON}/I_{OFF}(\sim 4.23 times), 84 % increase in transconductance (g_m), 136 % increase in cut-off frequency (f_T), 126 % increase in gain bandwidth product (GBP), point subthreshold swing (15.8 mV/decade) and other significant improvements in linearity figure of merits (FOMs) making the proposed device useful for low power switching, analog/RF and linearity applications.

Keywords Dual material · Ambipolarity · Dielectric pocket · Auxiliary gate · Control gate · Linearity

1 Introduction

MOSFETs are widely used for low-power switching, analog/RF design, and wireless communication systems. To further improve the performance and increase the packing density, MOSFET dimensions are aggressively down-scaling [1, 2]. This inevitably results in some critical issues, such as high subthreshold leakage current, short channel effects (SCEs), and SS restriction of 60 mV/decade [3, 4]. These challenges make conventional MOSFETs unfavorable for future low power switching and analog/RF applications.

To address the above issues, an alternate device structure based on quantum tunneling-FET (TFET) is considered one of the possible replacements of MOSFETs for low-power switching circuits due to lower leakage current, steeper SS below 60 mV/decade and immunity to SCEs [5]-[7]. These features make TFETs more favourable for low-power, energy-efficient circuits. However, the major limitations of this device is inferior I_{ON} and ambipolar behavior [8]. TFETs can be used in digital complementary logic circuits and high-frequency applications only if the ambipolar current of the device is suppressed. Ambipolar current implies the flow
of current for both positive and negative $V_{GS}$ [9]. This happens as the tunneling junction is transferred from source to drain side by applying $V_{GS} < 0$ (in case of n-type TFET). Because of ambipolar current, SS degra-
dation and efficiency of the device for the complimen-
tary digital logic circuits and high-frequency applica-
tions is limited [10, 11].

The ON-current of the TFETs is inferior due to in-
adequate band-to-band tunneling (BTBT) rate at the source junction. In TFET, high lateral electric field is re-
quired across the source junction to lower the tunnel-
ing barrier width and improve the tunneling current. As per the Wentzel-Kramers-Brillouin method, the BTBT prob-
bility depends exponentially on width of the tunneling barrier, effective bandgap, the effective mass of charge carrier, and the energy band overlap [24].

In recent literature, researchers have made numer-
ous efforts and proposed different methods to suppress the ambipolar current, improve the DC, analog/RF and linearity performance. Raad et al. [12] proposed a TFET based on hetero dielectric and workfunction engineer-
ing (HGD-DW TFET) and reported an $I_{ON}/I_{OFF}$ ratio of

\[ 9.8 \times 10^{-1} \text{ mS}, \ g_m = 0.290 \text{ mS}, \ f_T = (\sim 59.6 \text{ GHz}) \]

Kondekar et al. [13] proposed TFET based on electric-
dally doping (ED-TFET) to enhance the analog and ra-
dio frequency performance and reported an $I_{ON}/I_{OFF}$ ratio of

\[ \sim 10^{12}, \ g_m = 1.02 \text{ mS}, \ f_T = (100 \text{ GHz}) \]

Nigam et al. [14] proposed a charge plasma based TFET (DMCG-CPTFET) and obtained an $I_{ON}/I_{OFF}$ ratio of

\[ \sim 6 \times 10^{12}, \ I_{amb} = 1 \times 10^{-17} \text{ A/}\mu\text{m}, \ f_T = (\sim 28 \text{ GHz}) \]

Ashita et al. [15] investigated a inverted-C TFET (ICTFET) with SCOPs which provides both lateral and vertical tunneling to boost the ON cur-rent.

The authors have reported $I_{ON}/I_{OFF}$ ratio of

\[ (4.5 \times 10^8), \ SS = \text{48 mV/decade}, \ f_T = 1.19 \text{ GHz} \]

Chandan et al. [16] proposed a metal strip based TFET (MS-ED-
TFET) to overcome low switching ratio, SS and analog/RF performance and achieved an $I_{ON}/I_{OFF}$ of

\[ (8.92 \times 10^8), \ SS = (8.07 \text{ mV/decade}), \ g_m = 0.007 \text{ mS}, \ f_T = (0.17 \text{ GHz}) \]

Shaikh et al. [17] presented a quadruple-
gate TFET with drain engineering (DE-QG-TFET) and

achieved an $I_{ON}/I_{OFF}$ ratio of

\[ (1.79 \times 10^{12}), \ f_T = (\sim 34 \text{ GHz}) \]

Kumar et al. [18] proposed a stack-gate ap-proach TFET with dual material (DMDODG-TFET) to and reported an $I_{ON}/I_{OFF}$ ratio of

\[ (5 \times 10^{13}), \ SS = (18.5 \text{ mV/decade}), \ f_T = (8.8 \text{ GHz}) \]

Joshi et al. [19] investigated an extended source TFET (ESDG-TFET) and reported an $I_{ON}/I_{OFF}$ of

\[ (2.57 \times 10^{12}), \ SS = (12.24 \text{ mV/decade}), \ g_m = 0.238 \text{ mS}, \ f_T = (37.7 \text{ GHz}) \]

In this work, we propose DMSGO-DP-TFET to add-
ress the ON-current, ambipolarity, and improve the analog/RF, and linearity performance. For this, the combination of ($\phi_1 < \phi_2$) workfunction and high-K dielectric pocket at the drain junction leads to an in-
creased tunneling barrier width and reduced lateral elec-
tric field. As a result, ambipolar current reduces when negative $V_{GS}$ is applied. Similarly, ($\phi_1 < \phi_2$) work function and the low-K dielectric pocket at the source junction reduces the tunneling width ($\lambda$) and increases the lateral electric field, which results in an improved tunneling current.

This paper is organized as follows: Section 2 presents the structural, simulation details and process flow. Section 3 presents the structural optimization results. Section 4 describes the DC, analog/RF, and linearity performance. Lastly, Section 5 concludes the main findings of this work.

2 Device structure, parameters, simulation setup and process flow

![Fig. 1 Cross-sectional view of proposed DMSGO-DP-TFET](image)

The 2D structural view of the proposed DMSGO-DP-
TFET for the parameters listed in Table 1 is illus-
trated in Fig. 1. The length of the stack gate ($\text{SiO}_2 + \text{HfO}_2$) is considered 50 nm with $\text{SiO}_2$ layer thickness of (0.8 nm) and $\text{HfO}_2$ oxide layer thickness of (1.2 nm) [18]. Further, the entire gate is split into three segments la-belled as tunnel gate ($M_1$), control gate ($M_2$) and aux-iliary gate ($M_3$) with lengths ($L_1, L_2, L_3$) and work functions ($\phi_1, \phi_2, \phi_3$) respectively. In the case of single-material stack gate oxide-dielectric pocket-TFET (SMGSO-
The proposed device can be fabricated using the similar method reported in [19, 26]. The conceptual process flow of the proposed device is illustrated in Fig. 3(a)-(j). Firstly, a p-i-n structure can be formed using epitaxial growth process as shown in Fig. 3(a) and Fig. 3(b) shows the deposition of high-K and low-K dielectrics at the drain and source junctions. In the next step, etching is done to form the dielectric pocket as shown in Fig. 3(c). Then, SiO₂ can be grown on the p-i-n structure by the oxidation process as illustrated in Fig. 3(d). Atomic layer deposition (ALD) is used to deposit a thin HfO₂ film as illustrated in Fig. 3(e). In the next step, as shown in Fig. 3(f), cre-ation of the control gate can be done using masking and metallization of molybdenum (Mo) material. Moreover, auxiliary and tunnel gates can also metalized with alu-minium (Al) material using the self-aligned symmet-rical spacer method as illustrated in Fig. 3(g). Next, selective etching can be done for electrode formation as illustrated in Fig. 3(h). Similarly, the back gate formation can be done as illustrated in Fig. 3(i). Finally, Fig. 3(j) presents the metallization and patterning of source and drain contacts using Mo material as it provides the workfunction ranges from 4.36 eV to 4.95 eV.

3 Results and discussion

3.1 Workfunction optimization Results

To align the band structure at the source and drain junctions and to modulate the carriers through the channel, the entire gate length of DMSGO-DP-TFET is tri segmented known as tunnel gate (M₁), control gate (M₂), and auxiliary gate (M₃) with workfunctions φ₁, φ₂, and φ₃, respectively as illustrated in Fig. 1. By fixing
(\(\phi_1\) and \(\phi_3\)) and varying (\(\phi_2\), better switching ratio and minimum ambipolar current is observed for the combination (\(\phi_1 = \phi_3 < \phi_2\)) as illustrated in Fig. 4(a) and Table 2. Fig. 4(b) and Fig. 4(c) shows ON-state and the OFF-state band diagrams for the proposed DMSGO-DP-TFET by varying (\(\phi_2\)) and fixing (\(\phi_1 = \phi_3 = 4.0\) eV). From Fig. 4(c), it can be seen that tunneling width increases with an increase in (\(\phi_2\)). This results in band overlap decrease on the source side and decreases the tunneling current. Whereas, the band overlap has been noted at the drain junction for (\(\phi_2 > 4.4\) eV) and tunneling is observed in the OFF state, also (\(\phi_2\)) work function variation in the ON-state does not show a significant change in the tunneling current until the work-function (\(\phi_2 = 4.4\) eV). Also, as shown in Fig. 4(c), a decrease in band overlap is seen for (\(\phi_2 > 4.4\) eV), which results in a decrease in ON-state current (\(I_{ON}\)).

### 3.2 Dielectric pocket optimization results

To further improve \(I_{ON}\) and minimize the ambipolar current, optimized low-K and high-K dielectric pockets are inserted at the source and drain junctions, respectively. Fig. 5(a) shows the comparative \(I_{DS}-V_{GS}\) characteristics for different dielectric materials at the source and drain junctions in DMSGO-DP-TFET. Results demonstrate that combination of low-K dielectric pocket (air) at the source junction and high-K dielectric pocket (\(HfO_2\)) at the drain junction shows higher \(I_{ON}\) and minimum ambipolar current because of tunneling width and band alignment at the source and drain junctions. Fig. 5(b) shows \(I_{DS}-V_{GS}\) characteristics of DMSGO-DP-TFET for various dielectric pocket heights at the source junction by fixing the dielectric pocket height on the drain side. From the results, it has been noted that, dielectric pocket of 4 nm height at the source junction shows better \(I_{ON}\) because of increased electric field and decrease in tunneling width. Similarly, as shown in Fig. 5(c), fixing the height of the low-K dielectric pocket and varying the high-K dielectric pocket, it has observed that at the drain junction, dielectric pocket of 4 nm height shows minimum ambipolar current with better switching ratio (\(I_{ON}/I_{OFF}\)). Fig. 5(d) depicts the comparative \(I_{DS}-V_{GS}\) characteristics of DMSGO-DP-TFET for different pocket thicknesses. From the same figure, it can be noted that pocket thickness of 2 nm at the tunneling junction shows better tunneling current \(I_{ON}\) and minimum ambipolar current due to the band alignments at the source and drain junctions, respectively.

### 3.3 Gate length optimization

In this section, the gate segments of the proposed device is optimized. In this regard, Tables III–V shows the variations in \(I_{ON}, I_{OFF}, I_{amb}, I_{ON}/I_{OFF}\) for various combinations of \(L_1, L_2\) and \(L_3\). The optimization of \(L_3\) at constant \(L_1 = 10\) nm is shown in Table III. Further, the optimization of \(L_1\) at constant \(L_3 = 15\) nm is shown in Table IV. Table V shows the \(L_1\) and \(L_3\) variations at \(L_1 = L_3\). From this analysis, it has been noted that \(L_3 = 15\) nm performs better in terms of \(I_{ON}, I_{OFF}, \ldots\)
Table 2 Impact of $\phi_2$ on $I_{ON}/I_{OFF}$ with ($\phi_1 = \phi_3$)

| $\phi_2$ (eV) | $I_{ON}/\mu m$ | $I_{OFF}/\mu m$ | $I_{ON}/I_{OFF}$ | $I_{amb}/\mu m$ |
|---------------|----------------|------------------|-----------------|----------------|
| 4.0 eV        | 1.36x10^-5     | 2.96x10^-13     | 4.58x10^7       | 3.58x10^-16    |
| 4.2 eV        | 1.23x10^-5     | 1.26x10^-15     | 9.79x10^9       | 3.70x10^-16    |
| 4.4 eV        | 1.02x10^-5     | 4.58x10^-17     | 2.23x10^11      | 3.76x10^-16    |
| 4.6 eV        | 8.11x10^-6     | 6.18x10^-17     | 1.31x10^11      | 3.79x10^-16    |
| 4.8 eV        | 5.36x10^-6     | 7.31x10^-17     | 7.33x10^10      | 3.80x10^-16    |

$I_{amb}$, however, $L_1 = L_3 = 10$ nm shows better results in terms of $I_{ON}/I_{OFF}$ and is considered as optimized gate lengths in this work.

For the optimized dielectric pockets illustrated in Fig. 1, based on ($\phi_1, \phi_2, \phi_3$), various device structures can be formed as presented in Table 6. Further, a comparative analysis among these devices is done in terms of their carrier concentration, band diagrams, tunneling rate, surface potential, electric field variation, and $I_{DS}-V_{GS}$ characteristics. For SMSGO-TFET, all the three workfunctions ($\phi_1, \phi_2, \phi_3$) of the gate material has been considered equal (4.4 eV). Fig. 6(a) depicts the carrier concentration variation with distance for SMSGO-DP-TFET, DMSGO-DP-TFET1, DMSGO-DP-TFET2 and DMSGO-DP-TFET. From the figure, it has been noted that, due to the dielectric pocket at the source junction and dual material with work-function combination ($\phi_1 = \phi_3 < \phi_2$), higher electron concentration is observed for DMSGO-DP-TFET due to decrease in tunneling width as illustrated in Fig. 6(b). Therefore, bet-ter band-to-band tunneling rate is observed for DMSGO-DP-TFET as shown in Fig. 6(c). Further, large increase in surface potential and electric field is observed at the source junction for DMSGO-DP-TFET as illustrated in Fig. 6(d) and Fig. 6(e), respectively. Thus, maximum tunneling occurs at the source junction, as the BTBT rate ($G_{BTBT}$) at the tunneling junction depends on the
Fig. 5 Comparative optimization results for (a) Dielectric materials (b) Low-K dielectric pocket height (c) high-K dielectric pocket height (d) Dielectric pocket thickness by fixing heights in proposed DMSGO-DP-TFET.

Table 3 $L_3$ Gate segment optimization at constant $L_1 = 10$ nm

| $L_3$ | $I_{ON} (A/\mu m)$ | $I_{OFF} (A/\mu m)$ | $I_{ON}/I_{OFF}$ | $I_{amb} (A/\mu m)$ |
|-------|------------------|------------------|------------------|------------------|
| 5 nm  | 1.51x10^{-4}    | 3.16x10^{-14}   | 4.78x10^{9}      | 4.09x10^{-13}    |
| 10 nm | 1.48x10^{-4}    | 5.23x10^{-17}   | 2.83x10^{12}     | 5.21x10^{-16}    |
| 15 nm | 1.59x10^{-4}    | 4.36x10^{-14}   | 3.65x10^{9}      | 3.65x10^{-16}    |
| 20 nm | 1.62x10^{-4}    | 6.21x10^{-14}   | 2.61x10^{9}      | 3.64x10^{-16}    |

Table 4 $L_1$ Gate segment optimization at constant $L_3 = 15$ nm

| $L_1$ | $I_{ON} (A/\mu m)$ | $I_{OFF} (A/\mu m)$ | $I_{ON}/I_{OFF}$ | $I_{amb} (A/\mu m)$ |
|-------|------------------|------------------|------------------|------------------|
| 5 nm  | 8.51x10^{-5}    | 3.24x10^{-17}   | 2.63x10^{12}     | 3.66x10^{-16}    |
| 10 nm | 1.59x10^{-4}    | 4.36x10^{-14}   | 3.65x10^{9}      | 3.66x10^{-16}    |
| 15 nm | 1.79x10^{-4}    | 1.86x10^{-11}   | 9.62x10^{6}      | 3.66x10^{-16}    |
| 20 nm | 1.88x10^{-4}    | 3.8x10^{-11}    | 4.96x10^{6}      | 3.66x10^{-16}    |

Table 5 $L_1$ and $L_3$ Gate segments optimization with $L_1 = L_3$

| $L_1$ | $I_{ON} (A/\mu m)$ | $I_{OFF} (A/\mu m)$ | $I_{ON}/I_{OFF}$ | $I_{amb} (A/\mu m)$ |
|-------|------------------|------------------|------------------|------------------|
| 5 nm  | 8.45x10^{-5}    | 9.01x10^{-17}   | 9.38x10^{11}     | 4.09x10^{-13}    |
| 10 nm | 1.48x10^{-4}    | 5.23x10^{-17}   | 2.83x10^{12}     | 5.21x10^{-16}    |
| 15 nm | 1.79x10^{-4}    | 1.86x10^{-11}   | 9.62x10^{6}      | 3.66x10^{-16}    |
| 20 nm | 1.97x10^{-4}    | 4.0x10^{-11}    | 4.91x10^{6}      | 4.91x10^{-16}    |
Fig. 6 Comparative results of (a) Carrier concentration variation (b) Band variation (c) Tunneling rate (d) surface potential variation (e) Electric field variation (f) $I_{DS}$-$V_{GS}$ characteristics for SMSGO-DP-TFET, DMSGO-DP-TFET1, DMSGO-DP-TFET2 and DMSGO-DP-TFET at ($V_{DS}$ = 1.0V, $V_{GS}$ = 1.5V) 

Table 6 Possible devices with different work functions

| Possible device     | $\phi_1$ | $\phi_2$ | $\phi_3$ |
|---------------------|----------|----------|----------|
| SMSGO-DP-TFET       | 4.4 eV   | 4.4 eV   | 4.4 eV   |
| DMSGO-DP-TFET1      | 4.0 eV   | 4.4 eV   | 4.4 eV   |
| DMSGO-DP-TFET2      | 4.4 eV   | 4.4 eV   | 4.0 eV   |
| DMSGO-DP-TFET       | 4.0 eV   | 4.4 eV   | 4.0 eV   |
electric field ($\varepsilon$) leads to an increase in BTBT rate as per the expression [22].

\[ G_{BTBT} = A\varepsilon^\sigma \exp \left( -\frac{B}{\varepsilon} \right) \]  \hspace{1cm} (1)

Where $A$, $B$ are constants which are related to the electron’s effective mass and the tunneling probability, $\varepsilon$ is the electric field and $\sigma$ is the transition constant. Further, the probability of tunneling of the carrier ($T_{WKB}$) at the tunneling barrier is analyzed by the approximation of Wentzel–Kramer–Brillouin (WKB) [23].

\[ T_{WKB} \propto \exp \left[ -\frac{4\sqrt{2m^*}}{3q}\sqrt{E_g^3} \right] \]  \hspace{1cm} (2)

Where $m^*$ is the effective mass of an electron, $q$ represents the electron charge, $h$ represents Planck’s constant, $E_g$ is the effective bandgap, $\lambda$ is the width of tunneling barrier, and $\Delta \phi$ represents the energy overlap where the tunneling occurs. Therefore, as shown in Fig. 6(f), a significant increase in tunneling current is observed. Fig. 6 and Table 7 show that DMSGO-DP-TFTET performs better than other device structures.

4 DC, analog/RF and linearity performance

4.1 DC characteristics

In this section, comparative DC characteristics of DMCG-TFTET, DMCG-DP-TFET, DMCG-DP-TFET and DMSGO-DP-TFET has been analyzed. In this regard, the electric field variation with distance for the above device structures are illustrated in Fig. 7(a). From the simulation results, a higher electric field at the source junction is noted for DMSGO-DP-TFET, as a result, mini-mum tunneling barrier width is noted for DMSGO-DP-TFET as illustrated in Fig. 7(b). Further, Fig. 7(c) illustrates the comparative $I_{DS}$-$V_{GS}$ characteristics variation of DMCG-TFTET, DMCG-DP-TFET, DMSGO-TFET and DMSGO-DP-TFET. From the figure, a significant increase in ON-state current is observed for DMSGO-DP-TFET because BTBT depends on the electric field and tunneling width at the source junction [22]. Fig. 7(d) depicts the comparative output characteristics for various device structures at $V_{GS} = 1$ V. From the figure, it can be noted that the tunneling
current $I_{DS}$ rises at first as $V_{DS}$ increases from 0 to 0.8 V, then saturates because of velocity saturation as $V_{DS}$ increases beyond 0.8 V. The tunneling current does not change significantly from $V_{DS} = 0.8$ V onwards, so the current remains constant. Further, noted that due to employment of dielectric pockets at the source and drain junctions, reduced $V_T$, improved ON-state current, reduced ambipolar current, steep subthreshold slope(SS) and a higher switching ratio ($2.83 \times 10^{12}$) was observed for DMSGO-DP-TFET compared with other structures as illustrated in Fig. 7 and Table 8.

4.2 Analog/RF figure of merits

This section presents performance analysis of DMCG-TFET, DMCG-DP-TFET, DMSGO-TFET and DMSGO-
Table 7 Performance comparison of single material and dual material TFET with dielectric pockets

| Parameters          | SMSGO-DP-TFET | DMSGO-DP-TFET1 | DMSGO-DP-TFET2 | DMSGO-DP-TFET |
|---------------------|---------------|----------------|---------------|---------------|
| $I_{ON} \, (A/\mu m)$ | 1.37×10^{-5}  | 1.41×10^{-4}  | 1.35×10^{-5}  | 1.48×10^{-4}  |
| $I_{OFF} \, (A/\mu m)$ | 1.78×10^{-16} | 1.78×10^{-16} | 5.18×10^{-17} | 5.22×10^{-17} |
| $F_F$               | 7.68×10^{10}  | 7.91×10^{11}  | 2.61×10^{11}  | 2.83×10^{12}  |
| $V_{TH}(V)$         | 0.63          | 0.29           | 0.63          | 0.29          |
| $SS(mV/dec.)$       | 32.7          | 17.3           | 28.7          | 15.8          |
| Electric field (MV/cm) | 5.15        | 5.55           | 5.16          | 5.56          |
| $g_m(e)$            | 8.19×10^{-4}  | 9.79×10^{-4}  | 8.27×10^{-4}  | 1.01×10^{-3}  |

DP-TFET in terms of various analog/RF figure of merits (FOMs) such as $g_m$, $g_{DS}$, $R_o$, $C_{gs}$, $C_{gd}$, $f_T$, TGF, $I_{max}$, TFP, GBP and transit time. Transconductance ($g_m$) is one of the critical parameters in the analog/RF and linearity performance analysis of the device. Higher $g_m$ results in the higher gain of the device and plays a critical role in attaining higher values of $f_T$ and GBP in designing analog circuits [25]. In this regard, Fig. 8(a) depicts the comparative plots of $g_m$ variation with $V_{GS}$ at $V_{DS} = 1$ V. From the figure, it has been noted that in the subthreshold region $g_m$ of all the devices are very small, and it starts increasing due to increase in the ON-state current. Moreover, it decreases after a particular value of $V_{GS}$ due to mobility degradation [24]. Results also show that DMSGO-DP-TFET exhibits higher $g_m$ as compared to other device structures.

The next analog/RF performance parameter considered for analysis is output conductance ($g_{DS}$). A device with higher ($g_{DS}$) is preferred as it provides higher intrinsic gain. In this regard, Fig. 8(b) depicts the variation of $g_{DS}$ with drain voltage ($V_{DS}$). Results demonstrate higher output conductance for DMSGO-DP-TFET due to higher $\Delta I_{DS}$ shown by DMSGO-DP-TFET for the similar changes in $V_{DS}$. Fig. 8(c) shows the comparative $R_o$ variation with $V_{DS}$ for constant $V_{GS}$. From the results, lower $R_o$ is observed for DMSGO-DP-TFET as $g_{DS}$ is higher. The variation of $C_{gs}$ and $C_{gd}$ obtained from small-signal ac analysis at 1MHz frequency is illustrated in Fig. 8(d) and Fig. 8(e). From the results, it has been noted that DMC-G-DP-TFET shows the minimum value of $C_{gs}$, and for DMSGO-DP-TFET, a significant increase of $C_{gd}$ is noted above $V_{GS} = 0.85$ V.

Another critical parameter for RF performance analysis of the device is cutoff frequency ($f_T$). It is the frequency at which the current gain becomes unity [24]. Fig. 8(f) depicts $f_T$ variation with $V_{GS}$ for DMC-G-DP-TFET, DMC-G-DP-TFET, DMSGO-DP-TFET and DMSGO-DP-TFET. Results demonstrate that, initially, $f_T$ rises with $V_{GS}$ due to an increase in $g_m$, then decreases with $V_{GS}$ after reaching the peak value due to an increase in $C_{gd}$ and decrease in $g_m$ due to mobility degradation. From the results, a higher $f_T$ is obtained for DMSGO-DP-TFET which indicates that the proposed device structure is more favourable for radio frequency applications. The $f_T$ of the device is formulated as per the expression [24].

$$f_T = \frac{g_m}{2\pi(c_{gs} + c_{gd})}$$ (3)

GBP is another important parameter for the radio frequency performance analysis of the device, for a specified dc voltage gain of 10, it is calculated using the expression [24].

$$GBP = \frac{g_m}{2\pi 10 c_{gd}}$$ (4)

The GBP variations with $V_{GS}$ for DMC-G-DP-TFET, DMC-G-DP-TFET, DMSGO-DP-TFET and DMSGO-DP-TFET are illustrated in Fig. 9(a). Results demonstrate that, GBP initially increases as $V_{GS}$ increases, but it decreases for higher $V_{GS}$ due to the similar reasons as discussed earlier for $f_T$. Also, maximum GBP is noted for DMSGO-DP-TFET compared to other device structures. The TGF parameter indicates how efficiently the current reaches a certain transconductance value. In this regard, Fig. 9(b) shows the comparative TGF variation with $V_{GS}$. From the results, for DMSGO-DP-TFET, higher TGF is observed at lower $V_{GS}$ and with increase in $V_{GS}$ it starts decreasing as the variation in $I_{DS}$ is small. The TGF is obtained as follows

$$TGF = \left( \frac{g_m}{I_{DS}} \right)$$ (5)

Fig. 9(c) shows the comparative variation of TFP with $V_{GS}$ at $V_{DS} = 1$ V. From the results, it can be noted that DMSGO-DP-TFET shows higher TFP due to high $g_m$ and $f_T$. The TFP is obtained as follows

$$TFP = \left( \frac{g_m}{I_{DS}} \right) f_T$$ (6)

Fig. 9(d) depicts the comparative transit time (tau) variation with $V_{GS}$ at $V_{DS} = 1$ V. It is the time taken for carriers to move from the source to the drain [20].
The results show that as $V_{GS}$ increases, transit time decreases due to increased $f_T$. Also, the minimum transit time was noted for DMSGO-DP-TFET.

$$\tau = \frac{1}{2\pi f_T}$$  \hspace{1cm} (7)

The maximum oscillating frequency ($f_{max}$) is another crucial parameter for radio frequency performance analysis. It is calculated by using the equation

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{gd} R_{gd}}}$$  \hspace{1cm} (8)

Here, $R_{gd}$ represents the gate resistance. Fig. 9(e) shows the $f_{max}$ variation with $V_{GS}$ for DMCG-TFET, DMCG-DP-TFET, DMSGO-TFET and DMSGO-DP-TFET at $V_{DS} = 1.0$ V. From the figure, it has been noted that DMSGO-DP-TFET shows higher value of $f_{max}$ due to higher value of $f_T$. 

**Fig. 9** Comparative performance of (a) GBP (b) TGF (c) TFP (d) Transit time (e)$f_{max}$ variations for DMCG-TFET, DMCG-DP-TFET, DMSGO-TFET and DMSGO-DP-TFET.
This VIP2 is defined as follows:

\[ V_{IP2} = 4 \times \left( \frac{g_{m1}}{g_{m2}} \right) \]  

4.3 Linearity figure of merits

This section presents the linearity and distortion FOMs, such as \( g_{m3} \), VIP2, VIP3, IIP3, and IMD3 for DMCG-TFET, DMCG-DP-TFET, DMSGO-TFET and DMSGO-DP-TFET which has been explained in [25]. These are defined as follows:

\[ V_{IP2} = 4 \times \left( \frac{g_{m1}}{g_{m2}} \right) \]  

\[ V_{IP3} = \sqrt{24 \times \left( \frac{g_{m1}}{g_{m3}} \right)} \]  

\[ IMD3 = \left[ \frac{9}{2} \times (V_{IP3})^2 \times (g_{m3}) \right]^2 \times R_S \]  

\[ IIP3 = \frac{2}{3} \times \left( \frac{g_{m1}}{g_{m2} \times R_S} \right) \]  

Fig. 10(a) and Fig. 10(b) shows the comparative \( g_{m3} \) and \( g_{m1} \) variations with \( V_{GS} \) at \( V_{DS} = 1.0 \) V. From the
Table 8 Performance comparison of SiO₂ gate and stack gate TFET with and without dielectric pockets

| Parameters                  | DMCG-TFET | DMCG-DP-TFET | DMSGO-TFET | DMSGO-DP-TFET |
|-----------------------------|-----------|--------------|------------|---------------|
| I_D (A/μm)                 | 5.02 × 10⁻⁷ | 2.25 × 10⁻⁵ | 1.03 × 10⁻⁵ | 1.48 × 10⁻⁴  |
| I_OFF (A/μm) I_D/I_OFF     | 2.89 × 10⁻¹⁷ | 3.36 × 10⁻¹⁷ | 4.57 × 10⁻¹⁷ | 5.22 × 10⁻¹⁷ |
| f (GHz)                     | 1.73 × 10¹⁰ | 6.69 × 10¹¹ | 2.25 × 10¹¹ | 2.83 × 10¹²  |
| V_TH(V) SS(mV/decade)       | 0.84      | 0.51         | 0.53       | 0.29         |
| Electric Field V            | 29.4      | 17.9         | 31.4       | 15.8         |
| FM (MV/cm) g_m(S)           | 3.77      | 5.01         | 4.51       | 5.56         |
| f (GHz)                     | 4.88 × 10⁻⁵ | 5.49 × 10⁻⁴ | 2.79 × 10⁻⁴ | 1.01 × 10⁻³  |
| F_PMAX (GHz)                | 5.34      | 81.6         | 20.8       | 193          |
| GDP (GHz/V)                 | 56.6      | 383          | 172        | 525          |
| VIP2 (V)                    | 0.579     | 10.4         | 2.69       | 23.6         |
| VIP3 (V)                    | 0.77      | 1.84         | 1.66       | 2.67         |
| IIP3 (dBm)                  | 1.35      | 3.71         | 3.38       | 11.57        |
| IDM3 (dBm)                  | 0.09      | 8.49         | 8.03       | 18.71        |
| -7.19                       | 20.81     | 12.42        | 27.75      |

Table 9 Performance comparison of proposed DMSGO-DP-TFET with other devices

| Possible device | I_D/I_OFF | SS (mV/dec) | g_m (mS) | f_P (GHz) |
|-----------------|-----------|-------------|----------|-----------|
| HGD-DW TFET     | 9.8 × 10¹¹ | 18.5        | 0.290    | 59.6      |
| ED-TFET         | ~1 × 10¹²  | -           | 1.02     | 190       |
| CPTFET          | ~6 × 10¹²  | -           | -        | 28        |
| [16]MS-ED-TFET  | 4.5 × 10⁶   | -           | -        | 1.19      |
| DE-QG-TFET      | 8.92 × 10⁶ | 8.07        | 0.007    | 0.17      |
| DMDQG-TFET      | 1.79 × 10¹² |             | 0.261    | 34        |
| ESDG-TFET       | 5 × 10¹⁴     | 18.5        | 0.09     | 8.8       |
| Proposed work   | 2.57 × 10¹² | 12.24       | 0.238    | 37.7      |
|                 | 2.83 × 10¹² | 15.8        | 1.01     | 193       |

figure, peak values of g_m3 and g_m3 can be seen at lower V_GS in DMSGO-DP-TFET as compared with other devices. A higher values of VIP2 and VIP3 is required for better linearity and minimal distortion. In this re-gard, Fig. 10(c) and Fig. 10(d) depicts the comparative VIP2 and VIP3 variations with V_GS at V_DS = 1.0 V. Simulation results demonstrate that VIP2 and VIP3 of DMSGO-DP-TFET is higher than the other struc-tures. This indicates that DMSGO-DP-TFET is more linear than other devices. The next linearity and dis-tortion performance parameter for analysis is IMD3, it originates from the non-linearity characteristics of I_DS - V_GS and seems to be a disturbing signal in wireless sys-tems. Devices with lower IMD3 values can have the ability to withstand higher signal distortion. In this re-gard, Fig. 10(e) shows the comparative IMD3 variation with V_GS at V_DS = 1.0 V. From the figure, IMD3 of DMCG-TFET is noted to be smallest, indicating that the DMCG-TFET intermodulation distortion performance is the best of the above devices. The next lin-earity performance parameter for analysis is IIP3, for better linearity of the device IIP3 value should be high. In this regard, Fig. 10(f) shows the comparative IIP3 variation with V_GS at V_DS = 1.0 V. Results demon-strate that IIP3 for DMSGO-DP-TFET is much higher, which indicates that DMSGO-DP-TFET is more linear as compared to other structures.

5 Conclusion

In this work, a DMSGO-DP-TFET with dielectric pock-ets at the drain and source junctions is proposed. The structural parameters like gate lengths (L1, L2, L3), work functions (φ1, φ2, φ3), pocket height and thick-ness are optimized to achieve better switching ratio and reduce the ambipolar current. The performance of the proposed device is analyzed using TCAD device simu-lator. Finally, a comparative performance analysis of the proposed device is done with other device struc-tures and noted the combination of low-K and high-K dielectric pockets at the source and drain junctions and workfunction combination (φ1 = φ3 < φ2) on the stack gate oxide in the proposed device shows significant improve-ments in I_D/I_OFF, SS, g_m, f_P, R_O, transit time (τ), GDP, TGF, TFP, f_PMAX, VIP2, VIP3, IMD3 and IIP3 given in table 8. The performance of the proposed device is compared with the recent literature shown in Table 9 which shows that the proposed device useful for low power switching, high frequency and linearity applications.
Declarations

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