A hot hole-programmed and low-temperature-formed SONOS flash memory

Yuan-Ming Chang¹², Wen-Luh Yang¹, Sheng-Hsien Liu¹², Yu-Ping Hsiao¹², Jia-Yo Wu³⁴ and Chi-Chang Wu⁵*

Abstract

In this study, a high-performance TiₓZrᵧSiᶻO flash memory is demonstrated using a sol–gel spin-coating method and formed under a low annealing temperature. The high-efficiency charge storage layer is formed by depositing a well-mixed solution of titanium tetrachloride, silicon tetrachloride, and zirconium tetrachloride, followed by 60 s of annealing at 600°C. The flash memory exhibits a noteworthy hot hole trapping characteristic and excellent electrical properties regarding memory window, program/erase speeds, and charge retention. At only 6-V operation, the program/erase speeds can be as fast as 120:5.2 μs with a 2-V shift, and the memory window can be up to 8 V. The retention times are extrapolated to 10⁶ s with only 5% (at 85°C) and 10% (at 125°C) charge loss. The barrier height of the TiₓZrᵧSiᶻO film is demonstrated to be 1.15 eV for hole trapping, through the extraction of the Poole-Frenkel current. The excellent performance of the memory is attributed to high trapping sites of the low-temperature-annealed, high-κ sol–gel film.

Keywords: Sol–gel; Hole trapping; Flash memory

Background

Silicon-oxide-nitride-oxide-silicon (SONOS)-type memory is widely used for nonvolatile memory [1]. Compared to conventional floating-gate memory, SONOS-type memory has the advantage of high date retention, high endurance, and fast program/erase (P/E) speed [2]. However, the primary drawback of this memory type is that a higher voltage (typically >10 V) is required to inject carriers into the charge trapping layer, which results in excessive power consumption and leakage current. A device with low operation voltage is necessary for the development of high-performance memory [3].

Recently, high-κ materials have been considered as an effective charge storage material to achieve a faster program speed and improved charge retention [4,5]. Numerous technologies have been developed for the preparation of various high-κ films, including the sol–gel method, atomic layer deposition, physical vapor deposition, and chemical vapor deposition [6-9]. Among them, the sol–gel method is an appealing technique. Using this method, the high-κ film can be easily synthesized by mixing many types of materials in a solvent, followed by a post-anneal process after spin-coating on a substrate [10]. The advantages of the sol–gel method include simplicity, low cost, good uniformity, and compatibility with the current production lines of semiconductor plants [11]. However, performing high-temperature post-annealing to obtain a satisfying high-κ film was unavoidable in previous studies [6, 10-13]. The high-temperature post-annealing, which is typically above 900°C, hinders the wide application of the sol–gel method, such as in thin-film transistors or flexible devices.

In this study, a high-quality TiₓZrᵧSiᶻO film was synthesized using the sol–gel method and low-temperature post-anneal. The sol–gel-derived TiₓZrᵧSiᶻO film was applied as the charge storage layer of the SONOS-type flash memory. Identical to the high-temperature sample, the low-temperature post-annealed memory shows a noteworthy hot hole trapping characteristic and exhibits a lower operation voltage, faster P/E speed, and better data retention than previously demonstrated.

Methods

The fabrication of sol–gel-derived memory was started with a local oxidation of silicon isolation process on a
p-type (100), 6-in. Si substrate. A 4-nm tunneling oxide was thermally grown at 925°C in a furnace. A sol–gel solution containing zirconium tetrachloride (ZrCl$_4$), silicon tetrachloride (SiCl$_4$), and titanium tetrachloride (TiCl$_4$) was then spin-coated onto the substrate at 3,000 rpm for 60 s at ambient temperature. The sol–gel solution used ethanol as the solvent, and the molar ratio of the mixture for ZrCl$_4$/SiCl$_4$/TiCl$_4$/ethanol was 1:1:1:1,000.

After the sol–gel film was coated, a rapid thermal annealing (RTA) process was conducted at 600°C for 60 s in an oxygen ambiance. During the RTA process, a compound layer of metal-oxide-silicate containing titanium and zirconium was formed. A 10-nm blocking oxide film and 200-nm amorphous Si film were then deposited subsequently. The blocking oxide was grown by plasma-enhanced chemical vapor deposition, using silane (SiH$_4$) and nitrous oxide (N$_2$O) as the precursors to form a 10-nm SiO$_2$. The 200-nm amorphous Si film, used as the gate electrode, was deposited in the same system using the SiH$_4$ precursor. After gate patterning, As$^+$ ions were implanted at 20 keV with a dosage of 5E15 cm$^{-2}$ and annealed at 600°C for 24 h to define the source and drain. Finally, a 500-nm tetraethyl orthosilicate oxide was formed as the passivation layer, and the subsequent processes were used to fabricate the memory. The schematic structure of the Ti$_x$Zr$_y$Si$_z$O flash memory is shown in Figure 1. The channel width and length of the memory were 10 and 0.35 μm, respectively.

**Results and discussion**

Figure 2 shows the cross-sectional transmission electron microscopy (TEM) image of the sol–gel-derived Ti$_x$Zr$_y$Si$_z$O film annealed at 600°C. A continuous and smooth film of 2 nm in thickness was observed, suggesting that no obvious film morphology occurred in the sample annealed at 600°C. The composition of the sol–gel-derived Ti$_x$Zr$_y$Si$_z$O film was analyzed by X-ray photoelectron spectroscopy (XPS), and the Si 2$p$, O 1$s$, Zr 3$d$, and Ti 2$p$ spectra of the Ti$_x$Zr$_y$Si$_z$O film are shown in Figure 3a,b,c,d, respectively. The peaks in the figures indicate the component formation of the Ti$_x$Zr$_y$Si$_z$O film.

Figure 4 shows the $I_d$-$V_g$ curves of the Ti$_x$Zr$_y$Si$_z$O memory in fresh, program, and erase states. The measured condition for the program operation was $V_g = -8$ V, $V_d = 8$ V, and 1 ms, and that for the erase operation was $V_g = 8$ V, $V_d = 8$ V, and 1 ms. The characteristic curve shows a 3.7-V leftward shift after the program operation and then a shift back to the original, fresh state after the erase operation. Instead of applying a positive gate bias for programming previous cases, a negative gate bias was used to program the Ti$_x$Zr$_y$Si$_z$O memory. That is, a band-band hot hole (BBHH) was used to program, whereas a channel hot electron (CHE) was used to erase this memory. Programming was also attempted by injecting the electrons into the charge trapping layer, according to the method most previous studies reported, by applying a positive voltage to both gate and drain electrodes. However, only a minimal shift of the curve was observed.

Based on the $I_d$-$V_g$ measurement results, band diagrams of the Ti$_x$Zr$_y$Si$_z$O memory in the program and
erase operations are illustrated in Figure 5a,b, respectively. For the program operation, a BBHH was used; therefore, hot holes were injected from the silicon substrate and captured by the hole traps in the charge trapping layer, as shown in Figure 5a. In the erase operation, positive gate and drain voltages were applied. Channel hot electrons were injected and then recombined with the holes in the trap site, as shown in Figure 5b.

To demonstrate the thermal emission of carriers in the trap of the TiₓZrₓSiₓO memory, the Poole-Frenkel current was measured. The Poole-Frenkel current explains the hot hole trapping effect of the memory [14,15]. The expression for current density according to the Poole-Frenkel emission can be written as [16]:

\[ \frac{J_{FP}}{E} = a E_{ox} \exp \left[ \frac{b E_{ox}^{1/2} - \varphi_i}{k_b T} \right], \]

where \( K_b, T, a, b, \) and \( \varphi_i \) are the Boltzmann constant, the measurement temperature, a constant that depends on the trap density, a constant that depends on the electric permittivity, and the depth of the trap potential well, respectively.

If hot hole trapping is the dominant mechanism for programming the TiₓZrₓSiₓO memory, the extracted current should follow the Poole-Frenkel emission, that is, a linear slope for the plot of current density \((J/E)\) versus the square root of the applied electrical field. Therefore, a negative bias from 0 to −20 V was applied to the gate electrode with a constant 4-V drain bias at measurement to simulate the hot hole program of the memory. Figure 6a shows the plot of current density versus the square root of the applied electrical field under various measuring temperatures at hot hole program operation. Linear regions of the plot imply that the current of TiₓZrₓSiₓO memory
follows the Poole-Frenkel emission. Figure 6b shows an Arrhenius plot of the memory extracted from Figure 6a. The linear dependence of the current densities versus temperatures implies that the charges exhibit a thermally activated behavior, which is consistent with the Poole-Frenkel emission. The barrier height of the Ti$_x$Zr$_y$Si$_z$O film to silicon oxide can be extracted as approximately 1.15 eV for hole trapping, using the Poole-Frenkel current, which is shown in Figure 6c.

In addition to hot hole trapping, the Poole-Frenkel current of the hot electron program was also measured by applying a positive gate voltage. However, the result showed a nonlinear curve. Conversely, the measured result showed a linear dependence of current density, divided by the electric field squared, versus the reciprocal electric field (Figure 7a), which is represented by Fowler-Nordheim tunneling. This result may indicate that the energy band of the Ti$_x$Zr$_y$Si$_z$O film exhibits shallow trap potential well that could not preserve electrons when applying a positive gate voltage. Therefore, electrons were injected into the charge trapping layer and then went through the blocking oxide to the gate electrode. The band diagram of the Fowler-Nordheim (FN) operation is illustrated in Figure 7b. The expression of Fowler-Nordheim tunneling on an electric field can be given by [17]:

$$ J_{FN} = cE_{ox}^2 \exp(-d/E_{ox}), $$
where \( c \) represents a constant that depends on the energy barrier height and \( d \) is a constant that depends on the electric effective mass for tunneling.

Figure 8a,b shows the program and erase speeds, respectively, of the Ti\(_x\)Zr\(_y\)Si\(_z\)O memory under various operation conditions. Because the memory exhibited the hot hole trapping property, BBHH was applied to programming and CHE was applied to erasing.

As shown in Figure 8a, the threshold voltage \( (V_t) \) shift increased with increasing operation voltage; therefore, more ‘hot’ holes were generated and injected into the charge storage layer. The maximum memory window can be as large as 8 V. The program speed is 16 \( \mu \)s with a −2-V \( V_t \) shift for the program conditions of \( V_g = -8 \) V and \( V_d = 8 \) V. Compared with the erase speed shown in Figure 8b, only 1.7 \( \mu \)s is required for a 2-V \( V_t \) shift. It is reasonable that the erase speed is approximately ten times faster than the program speed because this memory is programmed by BBHH and erased by CHE. Even at only 6-V operation, the P/E speed can be as fast as 120:5.2 \( \mu \)s with a 2-V \( V_t \) shift. The fast P/E speed at such low operation voltage is superior to that demonstrated in previous studies [18-20] and is beneficial to the development of high-performance memory. This favorable result is ascribed to the formation of more trapping sites in the Ti\(_x\)Zr\(_y\)Si\(_z\)O film at 600°C annealing, and hence, more carries can be captured in the traps.

A highly reliable charge retention characteristic of the memory is demonstrated in Figure 9a. The normalized \( V_t \) shift is defined as the ratio of the \( V_t \) shift at the time of interest and at the beginning. The curve is obtained under the program conditions of \( V_g = -7 \) V and \( V_d = 7 \) V for 1 ms at 85°C and 125°C, respectively. As time extrapolated up to \( 10^6 \) s, the data retention measured at 85°C shows only 5% charge loss and that at 125°C shows only 10% charge loss. Figure 9b shows the endurance characteristics of the Ti\(_x\)Zr\(_y\)Si\(_z\)O memory. The measurement conditions are \( V_g = -6 \) V and \( V_d = 6 \) V for programming and \( V_g = V_d = 6 \) V for erasing. Despite a small drift of the
threshold voltage for both P/E operations, the memory window remained at around 2 V after $10^4$ P/E cycles. No substantial window narrowing was observed. The threshold voltage downward shift is mainly caused by the interface trap generation and hole trapping in the tunneling oxide.

The electrical performance of the Ti$_x$Zr$_y$Si$_z$O memory is summarized in Table 1 and compared with other sol–gel-derived memories [8,13,21]. As seen in the table, the Ti$_x$Zr$_y$Si$_z$O memory in this study exhibits improved electrical performance, particularly in retention properties. The Ti$_x$Zr$_y$Si$_z$O memory at either 600°C or 900°C annealing can be operated at much higher erase speeds compared to other materials. This is because the erase of the Ti$_x$Zr$_y$Si$_z$O memory is operated by CHE. Moreover, the operation voltage of the sol–gel-derived Ti$_x$Zr$_y$Si$_z$O memory can be decreased to only 6 V, without sacrificing its performance.

**Conclusion**

We demonstrated a high-performance sol–gel-derived Ti$_x$Zr$_y$Si$_z$O memory in this study. The memory exhibits a notable hot hole program characteristic, and hence, a much higher erase speed is achieved. The barrier height for the Ti$_x$Zr$_y$Si$_z$O film to silicon oxide was estimated to be approximately 1.15 eV for hole trapping, using the Poole-Frenkel emission model. Unlike other sol–gel-derived memories that require a higher temperature annealing process, this Ti$_x$Zr$_y$Si$_z$O memory with relatively low-temperature annealing exhibits excellent electrical performance such as low-voltage operation, fast P/E speed, and robust data retention.

### Table 1 Comparison of P/E speed and data retention of the sol–gel-derived high-κ memory devices

|                      | This work (Ti$_x$Zr$_y$Si$_z$O with 600°C annealing) | Ti$_x$Zr$_y$Si$_z$O NC with 900°C annealing [13] | Zr$_x$Hf$_y$Si$_z$O NC with 900°C annealing [6] | HfSi$_x$O$_y$ with 900°C annealing [21] |
|----------------------|------------------------------------------------------|-------------------------------------------------|-------------------------------------------------|----------------------------------------|
| **Program speed**    |                                                      |                                                 |                                                 |                                        |
| (2-V shift)          | 1.6x10^{-5} s                                        | 2.4x10^{-5} s                                  | 3x10^{-5} s                                     | 2x10^{-7} s                           |
| ($V_g = -8\,V, V_d = 8\,V$) | 1.2x10^{-4}                                        | ($V_g = -8\,V, V_d = 8\,V$)                  | ($V_g = 10\,V, V_d = 9\,V$)                    | ($V_g = V_d = 10\,V$)                 |
| ($V_g = -6\,V, V_d = 6\,V$) | 1.7x10^{-6}                                        | 1.9x10^{-6} s                                  | 2x10^{-3} s                                     | 5x10^{-5} s                           |
| **Erase speed**      |                                                      |                                                 |                                                 |                                        |
| (2-V shift)          | 5.2x10^{-6} s                                        | ($V_g = V_d = 8\,V$)                          | ($V_g = -10\,V, V_d = 9\,V$)                   | ($V_g = -10\,V, V_d = 10\,V$)        |
| ($V_g = V_d = 6\,V$) | 1.7x10^{-6} s                                        | 1.9x10^{-6} s                                  | 2x10^{-3} s                                     | 5x10^{-5} s                           |
| **Retention at 85°C**| 5% loss ($10^6$ s)                                   | 12% loss ($10^6$ s)                           | 11% loss ($10^6$ s)                             | 20% loss ($10^5$ s)                   |
| **Retention at 125°C**| 10% loss ($10^6$ s)                                  | 22% loss ($10^6$ s)                           | 30% loss ($10^6$ s)                             | NA                                     |

NC nanocrystal.
Abbreviations
BBHH: Band-band hot hole; CHE: Channel hot electron; J/E: Current density; P/E: Program/erase; SiCl4: Silicon tetrachloride; RTA: Rapid thermal annealing; SONOS: Silicon-oxide-nitride-oxide-silicon; TEM: Transmission electron microscopy; TiCl4: Titanium tetrachloride; ZrCl4: Zirconium tetrachloride; XPS: X-ray photoelectron spectroscopy.

Competing interests
The authors declare that they have no competing interests.

Authors’ contributions
Y-YC, S-HL, Y-PH, and C-CW carried out the experiment and measurement. J-YW and C-CW prepared the manuscript. W-LY and C-CW technically supported the study. All authors read and approved the final manuscript.

Acknowledgements
This work was financially supported by Taipei Medical University and Taipei Medical University Hospital under the contract number 101TMU-TMUH-07.

Author details
1. Department of Electronic Engineering, Feng Chia University, Taichung 407, Taiwan.
2. Department of Dentistry, Taipei Medical University Hospital, Taipei 110, Taiwan.
3. Department of Electronics and Materials Engineering, Feng Chia University, Taichung 407, Taiwan.
4. School of Dentistry, College of Oral Medicine, Taipei Medical University, Taipei 110, Taiwan.
5. Graduate Institute of Biomedical Materials and Tissue Engineering, College of Oral Medicine, Taipei Medical University, Taipei 110, Taiwan.

Received: 19 May 2013 Accepted: 23 July 2013

References
1. Su CJ, Su TK, Tsai TI, Lin HC, Huang TY: A junctionless SONOS nonvolatile memory device constructed with in situ-doped polycrystalline silicon nanowires. Nanoscale Res Lett 2012, 7:1–6.
2. Liu S-H, Yang W-L, Wu C-C, Chao T-S: A novel ion-bombarded and plasma-passivated charge storage layer for SONOS-type nonvolatile memory. IEEE Electr Device Lett 2012, 33:1393–1395.
3. Mao LF: Dot size effects of nanocrystalline germanium on charging dynamics of memory devices. Nanoscale Res Lett 2013, 8:21.
4. Khomenkova L, Sahu BS, Slaoui A, Gourbilleau F: Hf-based high-k materials for Si nanocrystal floating gate memories. Nanoscale Res Lett 2011, 6:172.
5. Ray SK, Das S, Singh SA, Manna S, Dhar A: Structural and optical properties of germanium nanostructures on Si(100) and embedded in high-k oxides. Nanoscale Res Lett 2011, 6:24.
6. Wu C-C, Tsai Y-J, Chu M-C, Yang S-M, Ko F-H, Liu P-L, Yang W-L, You H-C: Nanocrystallization and interfacial tension of sol–gel derived memory. Appl Phys Lett 2008, 92:123111.
7. Huang LY, Li AD, Fu YY, Zhang WQ, Liu XJ, Wu D: Characteristics of GDy2LaO3 high-k films by metal-organic chemical vapor deposition. Microelectron Eng 2012, 94:38–43.
8. Pandita D, Taeng TY: Growth, dielectric properties, and memory device applications of ZrO2 thin films. Thin Solid Films 2013, 531:1–20.
9. Lanza M, Iglesias V, Porti M, Nafria M, Aymerich X: Polycrystallization effects on the nanoscale electrical properties of high-k dielectrics. Nanoscale Res Lett 2011, 6:108.
10. Wu C-C, Tsai Y-J, Liu P-L, Yang W-L, Ko F-H: Facile sol–gel preparation of nanocrystal embedded thin film material for memory device. J Mater Sci Mater Electron 2012, 24:423–430.
11. Wu C-C, Yang W-L, Chang Y-M, Liu S-H, Hsiao Y-P: Plasma-enhanced storage capability of SONOS flash memory. Int J Electrochem Sc 2013, 8:6678–6685.
12. You H-C, Wu C-C, Ko F-H, Lei T-F, Yang W-L: Novel coexisted sol–gel derived poly-SiOx-oxide-nitride-oxide-silicon type memory. J Vac Sci Tech B: Microelectron Nanometer Struct 2007, 25:2568.
13. Wu C-C, Ko F-H, Yang W-L, You H-C, Liu F-K, Yeh C-C, Liu P-L, Tung C-K, Cheng C-H: A robust data retention characteristic of sol–gel derived nanocrystal memory by hot-hole trapping. IEEE Electr Device Let 2010, 31:746–748.
14. Kim DH, Park S, Seo Y, Kim TG, Kim DM, Cho H: Comparative investigation of endurance and bias temperature instability characteristics in metal-Al2O3-nitride-oxide-semiconductor (MANOS) and semiconductor-oxide-nitride-oxide-oxide-semiconductor (SONOS) charge trap flash memory. J Semicond Sci Tech 2012, 12:449–457.
15. Han B, Lee SW, Park K, Park CO, Rha SK, Lee WJ: The electrical properties of dielectric stacks of SiO2 and Al2O3 formed by atomic layer deposition method. Curr Appl Phys 2012, 12:434–436.
16. Kolodzey J, Chowdhury EA, Adam TN, Qui GH, Rau J, Olowolafe JO, Suehle JS, Chen Y: Electrical conduction and dielectric breakdown in aluminum oxide insulators on silicon. IEEE T Electron Dev 2000, 47:121–128.
17. Lee JD, Park JK: Nonvolatile hybrid memory cell embedded with Ni nanocrystals in poly(3-hexylthiophene). Jpn J Appl Phys 2012, 51:120020.
18. Ishida T, Mine T, Hisamoto D, Shimamoto Y, Yamaida R: Electron-trap and hole-trap distributions in metal/oxide/nitride/oxide/silicon structures. IEEE T Electron Dev 2013, 60:865–869.
19. Chen HR, Chang CY, Hung MF, Tang ZY, Cheng YC, Wu YC: A 2-bit/cell gate-all-around flash memory of self-assembled silicon nanocrystals. Jpn J Appl Phys 2013, 52:021902.
20. You HC, Hsu TH, Ko FH, Huang JW, Yang WL, Lee TF: SONOS-type flash memory using an HfO2 as a charge trapping layer deposited by the sol–gel spin-coating method. IEEE Electr Device Let 2006, 27:653–655.

doi:10.1186/1556-276X-8-340
Cite this article as: Chang et al.: A hot hole-programmed and low-temperature-formed SONOS flash memory. Nanoscale Research Letters 2013 8:340.