A Novel Sixteen Switch Three-Phase Nine-Level Voltage Source Inverter

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Abstract—A novel method for a 3-phase nine-level voltage source inverter using sixteen switch is introduced. The given technique employs conventional 3-phase bridges of two-level as a diode clamped model. A dc link voltage is supplied in such a way that the cascaded H-bridge produces the nine voltage levels. The switching patterns are stated as the levels increases then the pattern is difficult to produce three-phase outputs with fundamental modulation techniques. Here a solution for n-level inverter to produce required voltage-level with less number of power electronic components by setting up in the look-up tables. This study outlines the comparisons between nine-level voltage source inverters in different configurations and proposed novel sixteen switch three-phase inverter designed with less number of power electronic components and simulated in MATLAB/SIMULINK.

Keyword - Multilevel inverters, Look-up tables, Bidirectional Switches,

I. INTRODUCTION

The conventional voltage source inverter enables the synthesis of sinusoidal output voltage from several steps of voltages. The word multilevel has started with the three-level converter followed by numerous multilevel converter topologies. A wide range of topologies and control strategies are presented in literature [1]-[3]. A stack of multilevel inverter modules is designed for achieving low \( \frac{dv}{dt} \) characteristics, low switching losses low harmonics in the output voltage and current and better electromagnetic interference. Due to several advantages, multilevel inverters have been applied in various application fields [4]-[8].

The cascaded multilevel inverter is developed by a number of single-phase H-bridge inverters and is categorized into symmetric and asymmetric based on the magnitude of the dc voltage sources. In the symmetric multilevel inverter, the magnitudes of the dc voltages are equal while, the asymmetric multilevel inverter, the values of the dc voltages are unequal. Recently, asymmetrical multilevel inverter and hybrid multistage topologies are becoming on of the most interested research area. This topology reduces the cost and size of the inverter and improves the reliability since minimum number of power electronic components, capacitors, and dc supplies used. The hybrid multistage converters consist of different multilevel configurations with unequal dc voltage supplies. With such converters, different modulation strategies and power electronic components technologies are needed [9]–[15].

However, the purpose of improving the performance of the conventional single and three-phase inverters, different topologies employed with different types of bidirectional switches has presented. By comparing the unidirectional and bidirectional switches, bidirectional switch is capable to conduct the current and withstand the voltage in two-directions. For achieving the higher voltage levels, bidirectional switches with an appropriate modulation technique can improve the performance of voltage source inverter in terms of reducing the semi-conductor components and minimizing the withstanding voltages. Based on the technical background, this paper suggests a novel topology for a three-phase nine-level voltage source inverter with sixteen switches. Also extended structure for N-level is presented and compared by different trending topologies.

II. PROPOSED TOPOLOGY

A. Modelling

The proposed nine level voltage source inverter consists three-bidirectional switches (S1-S6), two diodes (Da1-Da2), are added to the conventional three-phase two-level bridge (Q1-Q6) as shown in Fig.1. The function of these bidirectional switches is to block the higher voltage and ease current flow to and from the midpoint (o). There by VSI is fed with a fixed voltage of 4Vdc and two cascaded bridges are fed with to unequal voltages Vdc and 2Vdc are connected to (+, -, o) terminals. Hence the presented VSI is functioned to generate nine equal and different voltage levels, the power circuit of the cascaded H-bridge makes use of two series cells having unequal voltage supplies. In each cell two switches are turned On and OFF under inverted conditions to output two voltage levels.
Fig.1. Circuit diagram for proposed sixteen switch nine-level voltage source inverter.

with corresponding voltages \( V_{dc}, 2V_{dc}, 3V_{dc}, 4V_{dc}, 0 \) \(-V_{dc}, -2V_{dc}\). The first cell dc voltage supply \( V_{dc}\) is added if switch \( T1 \) is turned ON leading to \( V_{mg}=V_{dc} \) where \( V_{mg} \) is the voltage at node (m) with respect to inverter ground (g) or bypassed if switch \( T2 \) is turned ON leading to \( V_{mg}=0 \). Likewise, the second cell dc voltage supply \( 2V_{dc} \) is added when switch \( T3 \) is turned ON resulting in \( V_{om}=+2V_{dc} \) where \( V_{om} \) is the voltage at midpoint (o) with respect to node (m) or bypassed when switch \( T4 \) is turned ON resulting in \( V_{om}=0 \). The peak voltage rating of the switches of the conventional two level bridge (\( Q1-Q6 \)) is \( 4V_{dc} \) whereas the bidirectional switches (\( S1-S6 \)) have a peak voltage rating of \( 3V_{dc} \). In CHB cells, the peak voltage rating of second cell switches (\( T3 \) and \( T4 \)) is \( 2V_{dc} \) while the peak voltage rating of \( T1 \) and \( T2 \) in the first cell is \( V_{dc} \). By total \( V_{ab}, V_{bc}, V_{ca} \) with corresponding voltages \( V_{dc}, 2V_{dc}, 3V_{dc}, 4V_{dc}, 0 \) \(-V_{dc}, -2V_{dc}, -3V_{dc}, -4V_{dc}\) as shown in Fig.2.

Fig.2. Simulated waveforms of \( V_{ab}, V_{bc}, V_{ca} \) with corresponding voltages \( V_{dc}, 2V_{dc}, 3V_{dc}, 4V_{dc}, 0 \) \(-V_{dc}, -2V_{dc}, -3V_{dc}, -4V_{dc}\)

The balanced load voltages can be achieved if the proposed inverter operates on the switching states depicted in Table I. The inverter may have 24 different modes within a cycle of the output waveform. The inverter line-to-line voltage waveforms \( V_{ab}, V_{bc}, V_{ca} \) with corresponding switching gate signals are depicted in Table I.

\[
\begin{bmatrix}
V_{ab} \\
V_{bc} \\
V_{ca}
\end{bmatrix} = \begin{bmatrix}
1 & -1 & 0 \\
0 & 1 & -1 \\
-1 & 0 & 1
\end{bmatrix} \times \begin{bmatrix}
V_{ag} \\
V_{bg} \\
V_{cg}
\end{bmatrix}
\]


| Table I: Look-Up Tables Sequence of the Proposed Nine-Level Inverter |
|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| S       | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | S1 | S2 | S3 | S4 | S5 | S6 | T1 | T2 | T3 | T4 | VA | VB | VC |
|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| t1      | 1  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  |
| t2      | 1  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 4  | 1  |
| t3      | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 4  |
| t4      | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 4  |
| t5      | 1  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 4  |
| t6      | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 1 | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 3  | 4  | 0  |
| t7      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 2  |
| t8      | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 4  | 0  |
| t9      | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 4  |
| t10     | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 1  |
| t11     | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 4  |
| t12     | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  |
| t13     | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| t14     | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| t15     | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 0  | 2  |
| t16     | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 4  |
| t17     | 0  | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| t18     | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  |
| t19     | 0  | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 2  |
| t20     | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 0  | 1  | 0  | 3  |
| t21     | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 4  |
| t22     | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 2  |
| t23     | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| t24     | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

It is worth noting that all simulated waveforms are obtained at t1 = t2 = ··· = t24 = 0.02/24 s. In order to plot the space vector diagram of the proposed inverter in a stationary d-q reference frame, the following equations can be used to derive d and q voltage components for all inverter vectors:

\[ V_d = \frac{4V_{dc}}{\sqrt{3(N-1)}} (2S_a - S_b - S_c) \]  
\[ V_q = \frac{4V_{dc}}{\sqrt{3(N-1)}} (S_c - S_b) \]  
\[ V = V_d - jV_q \]

where Vab, Vbc, and Vca are related to Vag, Vbg, and Vcg.

### III. SWITCHING ALGORITHM

The carrier based is the simplest modulation technique for unequal voltages sources. Carrier with Selective harmonic is the most common modulation technique used to control the fundamental output voltage as well as to eliminate the undesirable harmonic components from the output voltages. However, an iterative method such as Newton-Rapson method is normally used to find the solutions to (N-1) nonlinear transcendental equations. The difficult calculations and the need of high performance controller for the real application are the main disadvantages of such method.

Therefore, an alternative method is proposed to generate the inverter’s switching gate signals. It is easier to control the proposed inverter and achieve the required output voltage waveforms in terms of Sa, Sb, and Sc as shown in Fig.3. The basis of the proposed method can be explained as following: For a given value of modulation index Ma and within a full cycle of the operation of the proposed inverter, the switching states Sa, Sb, and Sc are determined instantaneously.
IV. EXTENDED STRUCTURE

We can observe that there is a possibility to reach an output voltage with higher number of steps in the proposed voltage source inverter by adding cascaded H-bridge in series as shown in Fig. 4. In order to achieve the desired number of voltage levels, the following method for the magnitudes of dc voltage supplies are:

![Circuit diagram of the proposed three-phase N-level voltage source inverter.](image)

By making the binary relationship between the dc supplies of the cascaded h-bridge structure as follows:

MATLAB/Simulink model of the proposed inverter shown in Fig. 1 has been developed to study the conduction and switching power losses. The proposed inverter is designed to deliver output power of $P_{out}=1.9$ kW. Three-phase series resistive–inductive (23Ω–3 mH /Phase) in star connection is used as load. The multilevel dc link is determined as $V_{dc}=75$ V, $2V_{dc}=150$ V, and $V_{fix}=4V_{dc}=300$ V and the proposed carrier modulation technique at $M_a=1$ is implemented to generate the appropriate switching gate signals. Three different types of semiconductor components are selected to build the prototype of the proposed inverter power circuit as following: IGBT (HGTG20N60B3D) 600 V/40 A for the two-level Bridge and CHB switches, IGBT (IRG4BC40W) 600 V/20 A for bidirectional switches, and Diode (RHRP1540) 400 V/15 A for embedded diodes in bidirectional switches and freewheeling diodes.
V. COMPARISON STUDY

| Topology                        | Clamped Diodes | Flying Capacitors | Cascaded H-bridge | Proposed |
|--------------------------------|----------------|-------------------|-------------------|----------|
| Power Semiconductor Switches   | 48 S           | 48 S              | 48 S              | 16S      |
| Clamped Diodes three phase     | 18             | 0                 | 0                 | 12       |
| DC bus capacitor               | 8              | 8                 | 4                 | 3        |
| Balancing capacitors three phase | 0              | 28                | 0                 | 0        |
| Voltage unbalancing            | Average        | High              | Very small        | small    |

Based on the comparison carried among the proposed method, the following observations are taken.

1) Compared to all the aspects, Proposed three-phase voltage source inverter requires less power electronics components and less size with low voltage handling stress.

2) On the other hand, the voltage and current ratings of the power components have an effect on the cost and realization of the voltage source inverter.

Assuming that all power components have an equal current rating which is the rated current of the load (IL), the voltage ratings of these components depend on the magnitude of dc voltage supplies, voltage stress, and structure of the inverter.

Considering that all inverters have the same input dc link which equals (N–1) Vdc.

The proposed inverter is designed to deliver output power of Pout=1.9 kW. Three-phase series resistive-inductive (23Ω–3 mH/Phase) in star connection is used as load. The multilevel dc link is determined as Vdc=75 V, 2Vdc=150 V, and Fix =4Vdc =300 V and the proposed carrier modulation technique at Ma=1 is implemented to generate the appropriate switching gate signals. Three different types of semiconductor components are selected to build the proposed inverter power circuit as following: IGBT (HGTG20N60B3D) 600 V/40 A for the two-level Bridge and CHB switches, IGBT (IRG4BC40W) 600 V/20 A for bidirectional switches, and Diode (RHRP1540) 400 V/15 A for embedded diodes in bidirectional switches and freewheeling diodes.

VI. CONCLUSION

In this paper, a novel control technique suitable for high power low switching frequency sixteen switch three-phase nine-level inverter is introduced. In order to minimize the switching devices different voltage sources as configured by bridge circuit and clamped by diode. Therefore the proposed topology results in reduction of installation area and cost. The fundamental frequency modulation was comfortably employed and showed high flexibility and simplicity in control. Moreover, the proposed technique was extended to N-level with different methods. The proposed topology was compared with the different kinds of techniques in literature from different points of view. According to the comparison results, the proposed topology requires a lesser number of power diodes, IGBTs, driver circuits, and dc voltage sources. The performance accuracy of the proposed sixteen switch three-phase nine-level inverter was verified through the MATLAB simulation.

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VIII. BIOGRAPHIES

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