Acquiring a portable high density charged particles trap might consist of an array of micro-Penning-Malmberg traps (microtraps) with substantially lower end barriers potential than conventional Penning-Malmberg traps [1]. We report on the progress of the fabrication of these microtraps designed for antimatter storage such as positrons. The fabrication of large length to radius aspect ratio (1000 : 1) microtrap arrays involved advanced techniques including photolithography, deep reactive ion etching (DRIE) of silicon wafers to achieve through-vias, gold sputtering of the wafers on the surfaces and inside the vias, and thermal compression bonding of the wafers. This paper describes the encountered issues during fabrication and addresses geometry errors and asymmetries. In order to minimize the patch effects on the lifetime of the trapped positrons, the bonded stacks were gold electroplated to achieve a uniform gold surface. We show by simulation and analytical calculation that how positrons confinement time depends on trap imperfections.

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I. INTRODUCTION

The accumulation and storage of the large quantities of low-energy positrons is becoming increasingly important in different fields. Positron plasmas can be confined by static electric and magnetic fields and be in a state of thermal equilibrium for long periods of time [2]. To accomplish the goal of energy storage, one of the fundamental limitations of conventional PM traps needs to be overcome: the required electrostatic confining potentials rise to large and impractical values as the charge stored in a PM trap is increased. A design has been proposed by one of the authors (K. G. Lynn) [3] in order to increase positron storage by orders of magnitude, which consists of an array of microtraps, as shown schematically in Fig. 1, with a large length to radius aspect ratio (1000 : 1) and a low confinement voltage (10 V). The metallic electrodes screen the charge in each microtrap.

![FIG. 1: Schematic configuration of an array of microtraps. The image is not to scale.](image)
which avoids all plasma complications and pushes the density over the Brillouin limit, and permits confinement times limited only by vacuum conditions. The fabrication of microtrap arrays of 100 µm diameter and 100 mm length was proposed in this study. This goal can be achieved by deep etching 200 silicon dies of 500 µm thickness and 38 mm diameter (each die contains thousands of 100 µm holes) which were then aligned and stacked over one another to create thousands of long tubes as shown in Fig. 2. Computationally, more than one hundred million positrons can be trapped in one tube of this dimension (100 µm diameter and 100 mm length) when the applied electric field to the tube ends in only 10 V. Thus, the entire trap would hold more than $10^{12}$ positrons. There were two types of dies in the trap design which create a 10-section trap (10 mm per section). The type 1 dies isolate each trap section from one another with SiO₂ as an electrical barrier enabling us to apply different voltages on trap sections which would be required to inject and accumulate positrons, while providing a physical constraint through their tab features. The Au side contains electrodes for the electrical connection. Each trap segment between two type 1 dies is fabricated by bonding type 2 dies together, which transmit the electric potential through the segment.

However, some difficulties have been reported using thick films of SU-8 including formation of edge bead [10] and air bubbles [11] during the spin coating, as well as film adhesion issues during development [12]. There are several techniques for achieving thick, vertical silicon structures after fabrication of a suitable mask with the desired pattern. Cryoetching is a process relying on cooling the silicon to cryogenic temperatures, which we applied previously [13] for fabrication of the trap. We encountered several issues using this process such as bowing, masking, notching, and undercutting. In this study we used a Bosch process, which is a patented technique developed by Robert Bosch [14]. There are also some other techniques based on anisotropic wet chemistry. However, they are sensitive to crystallographic orientation and they have a lower mask selectivity [1]. In the Bosch process, a fluorine plasma is used to etch the silicon (etch step) after which a fluorocarbon plasma passivates the sidewalls (deposition step). Repeating these steps leads to deep and vertical etch profiles. Just as for the Cryo process, SF₆ gas is used in the etch step to provide a plasma of free radical fluorine. The difference between these techniques is the mechanism of sidewalls protection. In the Cryoetching process, adding oxygen to the plasma causes a layer of oxide/fluoride (SiOF) to condense on the due to the cryogenic temperatures which prevents etching of the sidewalls. While in the Bosch process C₄F₈ provides the passivation in the deposition step by breaking into longer chain radicals in the plasma and deposits as a fluorocarbon polymer. The higher process temperatures used in Bosch versus Cryoetching increases the etch rate of the mask material. Moreover, the Bosch process should be operated at higher bias voltages than the Cryoetching and it results in additional attack on the mask material and further decreases the selectivity. By tuning the parameters in each step and the time ratio of the two steps, the etch profile and the mask selectivity can be controlled. Thin gold films are used for many applications in electronics. Following the etching, gold sputtering on the surface enables us for thermal compression bonding of wafers. However, the precise alignment of the vias during the bonding is crucial. It has been found in experiments that the confinement time of positrons in PM traps is independent of pressure when the pressure is below $10^{-7}$ Torr, and it exhibits scaling almost as $L_p^{-2}$ ($L_p$ is the plasma length) [15]. The anomalous loss is mainly caused by azimuthal asymmetries [4]. Hence, loses arise on experiments by trap imperfections such as misalignment of microtraps, asymmetries, and magnetic field misalignment. Simulations will help to investigate these effects and find out the amount of deviations from perfectness tolerable in our design. Other intrinsic asymmetries, such as patch effects, are also present. The patch effects encompass various phenomena, for instance, physically imperfect surfaces (plateaus, steps, scratches, etc.),

![FIG. 2: The trap configuration showing axially stacked holey dies each including 20, 419 number of 100 µm holes. Two types of dies form the whole trap.](image)

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1 Depth etched into silicon versus depth etched into mask.
chemical impurities, and random atomic lattice orientation, which give rise to boundary regions. These all result in a variation of the local surface work function \( \Phi \) and induce local electric fields, which can influence the charged particles and might play an important role especially when the walls get very close to the particles. The effects of these potential asymmetries on the lifetime of a positron flying inside the microtrap can be very important. Gold sputtering and electroplating of the wafers inside the vias will help us to reduce these effects. Gold is favorable since it is a good electrical conductor and it is not easily oxidized.

II. EXPERIMENTAL DETAILS AND RESULTS

A. Photolithography

P-type Si wafers of 100 mm diameter, 540±5 \( \mu m \) thick, \(< 100 >\) oriented with a long primary flat and a secondary flat at a 90\(^\circ\) angle and a resistivity range of 1 – 20 \( \Omega \cdot cm \) were used in the experiments. The trap pattern was transferred to the SU-8 photoresist onto the wafers using photolithography mask shown in Fig. 3. A pattern of three dies per wafer was used, which yielded 20,419 holes of 100 \( \mu m \) diameter per each die in a hexagonal pattern with a fill factor of 0.5. The center-to-center distance of the holes was 200 \( \mu m \) and they were arranged on a 60\(^\circ\) triangular pattern. Each die was 38 \( mm \) in diameter and had six 3 \( mm \) holes for future alignment and bonding of the dies. Different size features reached varying depths in a given time during etching. The etch rate of trenches was adjusted to match that of holes and the size of 40 \( \mu m \) for the trench width was found by experimentation in which all features are etched thorough at the same time.

![Photolithography mask](image)

To etch the features completely through the Si wafers using the Bosch process, 80 \( \mu m \) thick SU-8\( ^{TM} \) would be required which was found by experimentation. The SU-8 2025 (from Micro-Chem Corp., Newton, MA, USA) is the least viscous photoresist of SU-8\( ^{TM} \) resists which can produce such a thick mask. The photolithography procedure with satisfactory results was found by doing a matrix of experiments and it is summarized in Table I.

TABLE I: Photolithography procedure of 80 \( \mu m \) SU-8\( ^{TM} \) on 100 \( mm \) diameter silicon wafers.

| Ti adhesion layer | Dehydration bake | Spin coat (time, speed, Acc.) | Soft bake | UV Exp. | Post bake | Development |
|------------------|-----------------|-----------------------------|----------|--------|----------|-------------|
| 50 nm            | 5 min 200\(^\circ\)C | 10, 500, 100 32, 1500, 300 25, 0, 50 | 5 min 65\(^\circ\)C | 12 min 95\(^\circ\)C 1200 J/cm\(^2\) 10 min 95\(^\circ\)C | 5 min 65\(^\circ\)C |

We found that applying a 50 \( nm \) thick Ti adhesion layer via sputtering and not using the Omnicoat\( ^{TM} \) adhesion promoter yielded a film with a better adhesion. It was also proved that dehydrating the surface before coating was another key factor and skipping this step always caused adhesion problems. Thus, thoroughly cleaned Ti coated wafers were baked on a hotplate at 200\(^\circ\)C for 5 min prior to coating. Spin coating the resist was done after allowing the substrate to reach the room temperature. Blowing nitrogen gas after installing the wafer on the spin coater and right before pouring the resist also helped to improve dehydration and to promote adhesion. Planarization defects such as edge bead and air bubbles are more troublesome when the viscosity and thickness of the SU-8 increase \[17, 18\]. The edge bead was removed by gently cutting it off with a clean razor blade. To prevent trapping air bobbles in the resist after spin coating due to the high viscosity of this resist, a big volume of SU-8 was poured on the center of the wafer (\( \approx 10 \) \( mL \)). The spinning was started when the resist approached the edge of the wafer, which normally took 1-2 seconds. Leaving the coated wafer on the spinner for 1 minute helped to relax the SU-8. Sometimes, we ended up with small bob-

\(^2\) The fraction of total surface of holes to the trap volume.
bles which went away during first step of the soft baking process (65°C). Almost one out of ten wafers was not bubble-free after soft baking using this technique. Spin coating produced fairly uniform films with 2 μm deviation. However, spin chuck vacuum was causing a circular mark at the center due to the deforming of the substrate. The chuck mark was avoided to some extent by removing the O-ring on the spin chuck. During the prebake step, the film temperature was brought above the glass transition temperature of SU-8 on the hotplate for enough time to remove the solvents and also relieve stresses incurred by spin coating. Prebaking on the hotplate was preferred because it reduces the chance of trapped solvents inside the film. Underbaked resists resulted in partial or complete delamination of the mask during development and also caused to patterns with lower resolutions. When the wafer stuck to the mask after the exposure it was a sure sign of underbaking. On the other hand, overbaking the wafer stuck to the mask after the exposure it was a sure sign of underbaking. The mask delamination. It has been known that the adhesion is due to process parameters such as the soft bake and the post-exposure bake times and temperatures, exposure level, and development times (12). The adhesion quality of SU-8 mask was traced carefully during the development as a matter of delamination time and extent. Observation during matrix experiments after each step of process were also recorded which helped to determine the conditions that would lead to good adhesion without any delamination. We did not have any success without using a sputtered Ti adhesion layer. Even applying HMDS (hexamethyl disilane) and/or removing the Si oxide layer to promote adhesion were fruitless. The large difference of thermal expansion coefficient between Si (2.6 ppm/K) and SU-8 (50 ppm/K) causes high values of internal stress in the mask as the resist is heated and cooled several times and it becomes more brittle as the solvent level decreases. Applying a Ti seed layer substantially decreased this stress (thermal expansion coefficient of Ti is 8.3 ppm/K) and along with optimized processing parameters led to good adhesion of the SU-8 film.

B. Deep reactive ion etching

The exposed Si from the photolithography process was then etched by DRIE. An Oxford Plasmalab™ 100 machine (Oxford Instruments plc, Abingdon, Oxfordshire OX13 5QX United Kingdom) was used for this process. The machine has an RF plasma power of up to 300 W at 13.56 MHz, ICP power up to 3,000 W at 13.56 MHz, and a substrate temperature range from −150 to +400°C. Achieving a good process requires an understanding of the mechanisms occurring. Initially, the ICP power ranging from 450 to 1600 W and an RF power ranging of 10 to 50 W was studied. These power values were limited to avoid burn the resist. The SF6 and C2F8 flow was adjusted so that the profile was anisotropic. The temperature of the substrate holder was maintained at 15°C and the helium backside flow ensured a good thermal conduction to the substrate. Adjusting the process was done by changing the ratio of each step in order to achieve a vertical profile by balancing between the polymer deposition and etching without changing the ions energy. Pressure is one the key parameters in this technique, which substantially affects the plasma properties and so the surface chemistry. Figure 4 shows examples of unsuccessful etches due to the improper SF6 and C2F8 flows, pressure, and ratio of etch and deposition time steps. Above a certain flow the etch rate dropped and the profile became anisotropic.

Running a series tests with different parameters led us to the recipe shown in Table IV while the corresponding etch profile is shown in Fig. 5. Lower pressures allowed better controlling of the profile since it reduces the ion scattering by collisions. Decreasing the pressure also prevents the gas interference. So we were able to etch through the whole thickness without micromasking of the walls at the bottom. A semiconductor tape on the backside of the wafers was added and we were able to get all features resolved in the wafer as shown in Fig. 6 while simultaneously separating the dies from wafer. The tape also aided in keeping the wafer and dies together while it was removed from the DRIE machine. Increasing the SF6 gas flow along with lowering the pressure, which decreases the radicals density, caused to increase the etch rate from 1.2 to 2.1 μm/min. The mask selectivity of 7 : 1 was obtained in this run. Trenches with different widths were processed and it revealed that the trench width of 40 μm had the same etch rate as the 100 μm holes. This is important as we needed the all features to be etched completely through the wafer at the same time.

The minimum length of etch and deposition steps were restricted by response speed of the pressure and mass flow...
(a) isotropic etch due to the improper SF$_6$ and C$_4$F$_8$ flows (85 sccm and 60 sccm)

(b) Negative tapering (deviation from 90° angle) due to the improper ratio of etch and deposition time steps

(c) Micromasking and rough walls at deeper sections due to using high pressure (30 mTorr).

FIG. 4: Examples of unsuccessful etchings.

TABLE II: Optimized Bosch process recipe. The corresponding etch profile is shown in Fig. 5 exhibits a 20% bowing defect.

| Process       | SF$_6$ flow (sccm) | C$_4$F$_8$ flow (sccm) | Time step (s) | Pressure (mTorr) | Backside He pressure (Torr) |
|---------------|--------------------|------------------------|---------------|-----------------|----------------------------|
| Etch          | 100                | 1                      | 28            | 26              | 7                          |
| Deposition    | 1                  | 100                    | 14            | 20              | 7                          |

controllers and also the error lapse time in the software. This time was 14 seconds for Oxford Plasmalab$^{TM}$ 100 machine which was found by experimentation. In the following experiment we decreased the cycle times to 12 s and 6 s for etch and deposition steps respectively, where the ratio of two were equal to previous cases. Figure 7 exhibits the profiles obtained with this process. While less bowing defect was experienced using decreased time steps, strong striations were seen at the walls and the profile showed micromasking defects at deep sections. As the depth of the etch increased, the attack on the sidewalls due to ion bombardment became less and so resulted in polymer buildup and micromasking at the bottom of the holes. The mask selectivity was also improved in this experiment from 7 : 1 to 33 : 1 which would help us by utilizing a thinner resist and improve the bowing defect even further by avoiding ions deflection charged by hitting the resist walls. The mask selectivity was almost insensitive to the nature of the resist (as we also tried other resists such as AZ photoresists) and even hard baking of the resist prior to etching did not improve it. Sidewall striation observed in the results was a sign of overpassivated sidewalls of the holes. Increasing the RF power and so the bias voltage in the etching step would improve the passivation layer removal from the sidewalls and prevent micromasking but it would also increase ions attack to

(a) Bowing effect of 20% at the top section of the holes. This sample is not etched completely through the thickness.

(b) Backside of the sample which is etched thoroughly showed a back-notching due to the excessive etching. Wafer backside is not polished.

FIG. 5: The etch profile using the optimized Bosch process recipe in Table II

FIG. 6: One die etched completely through. All the features were resolved.
the walls and consequently worsen the bowing defect or result in a positive taper.

In the recent experiment, the pulses were not long enough to stabilize the plasma and obtain a reasonable duty cycle. Our Oxford Plasmalab™ 100 machine was originally designed for the Cyroetching process and lack some of the equipment used for the Bosch technique. Firstly, this process needs fast response mass controllers which exceed SEMI standard E17-91. The response time of these controllers should be below one second as the flow reaches within 2% of the set point. Also, the time delay between opening these controllers and reaching the gas to the chamber are minimized in these systems. These allow having short etch and deposition time steps which was not doable in our system. Due to the fact that we were not able to eliminate the bowing defect completely and also that we would need a high rate of production to fabricate all 200 silicon dies needed to complete the trap, we got the entire samples with the same pattern from RTI International Institute and we continued fabrication of the trap by gold-coating and bonding the dies at our research center at Washington State University (WSU). All of the dies were inspected thoroughly and those which had more than 10 plugged holes in total or had excessive back notching were rejected.

C. Gold sputtering

In order to bond the dies together and fabricate the segments shown in Fig. 8, we sputtered a thin film of gold on the dies surfaces (1.5 µm). The native oxide layer of silicon was stripped first with dipping into the BOE (Buffered oxide etch of NH₄-HF 10 : 1) solution for 10 s. A TiW layer of 40 nm thick was sputtered to get good adhesion of the gold on the samples which was qualitatively checked by the typical tape test. It was also crucial to have gold coated on the inside of the holes to obtain a uniform potential throughout the holes. A sample die was gold coated flat and parallel to the sputtering target. However, the result showed a resistivity of 4 kOhm through the holes due to the absence of gold inside the holes. The solution resided on sputtering both side of the dies with an angle (tan⁻¹(D/L) ≈ 11°, where D is the diameter and L is the length of the holes) from horizontal state while it was rotating off-axis of target as illustrated in Fig. 8. The flipping axis to the second side of the die was also important to get all the inside surfaces coated.

The electrical tests using an ohmmeter proved continuity through the holes but this method did not demonstrate anything about the uniformity of the coating. We also had concerns about electric potential variations from hole-to-hole. Thus, the sample die was cleaved after sputtering both sides. The broken area of the die exposed several of the holes. By applying a 9.4 VDC bias to the die and using a voltmeter with a very fine wire (48 AWG), we were able to probe the exposed holes. Each of the holes confirmed the 9.4 VDC bias. It was also noted that probing the bare silicon between the holes gave a much lower voltage reading (∼ 3 VDC). To further check the consistency between holes, the 48 AWG wire was used to probe additional holes in the die. A 2 mm length was stripped.
at the end of the wire, the wire was pushed all the way through the hole, and the 2 mm tip was then bent and the wire was slowly pulled back through the hole. This provided good contact to the hole surface while observing the voltage as the wire was pulled through the hole. Several holes were checked in this manner across the die and all read a constant 9.4 VDC while the tip of the wire was inside the hole. The SEM image in Fig. 9 shows inside the holes before and after gold sputtering. The scalloping size of the walls due to the Bosch process was measured about 400 nm. After gold sputtering the sample with the described technique, the gold grains were detected all over the surface except in some micro-caves with dimension of 500 nm at maximum. These caves were mostly found near the middle depth of the holes where the gold ions had difficulty reaching.

The entire jig along with the dies were loaded into a furnace (Barnstead Thermolyne 1400) that was stable at the bonding temperature. The jig (with the dies and sapphire rods) was baked for 60 min to allow coming to equilibrium before adding pressure to the dies. Several bonding attempts were made at the temperatures ranging from 200 to 300°C and pressures from 16 to 1230 psi and bonding time from 20 to 60 min. Many authors report either much higher bonding temperatures (≈ 400°C) or much higher pressures (≈ 1,800 psi) [20, 21]. Successful bonding in our jig occurred at temperature of 250°C and pressure of 1,230 psi (9.7 kN) for 60 min and proved to be a reliable and reproducible process. One experiment yielded a bonded stack of thirteen etched dies. Analysis was needed to evaluate the quality of the bond and alignment precision. A rudimentary drop test from a 5 cm height was performed and successfully demonstrated reliable bond strength. An IR transmission microscope image from an area of the stack is shown in Fig. 11, representing a very successful alignment. The SEM images were taken from an example hole, though it was not possible to focus on all 13 dies. The misalignment of the dies was measured at about 4 µm, as shown in the Fig. 12.

D. Bonding

After gold sputtering the dies, we used gold thermocompression bonding to bond the etched dies. Initially, the gold coated dies were cleaned. An alignment and bonding jig made of Invar36 shown in Fig. 10 was precision-machined and used for the bonding. The top plate (1) contained a screw that presses plate (2) against plate (3). The dies were threaded onto the sapphire rods in between plate (2) and (3). The sapphire rods used for bonding were 3.004 ± 0.0005 mm diameter and 50 mm long with a straightness of 6 µm over the entire length. There were two kinds of 3 mm holes on the Si dies. Three out of six holes, named Tight-tolerance holes, had diameter of 3.0096 ± 0.0005 mm, were utilized with the sapphire rods when bonding took place. The other three holes, named as Regular holes, had diameter of 3.0299 ± 0.0005 mm, and used for handling and coarse alignment of dies and bonded segments.

E. Gold electroplating

The bonded stacks were then gold electroplated in order to fill the micro-caves which might not be coated during gold sputtering shown in Fig. 9. The ‘24k Pure Gold’
gold plating solution (from Gold Plating Services company, Kaysville, Utah) was used in experiments which is designed to produce a gold electrodeposi t with higher purity than 99.9%. The samples surfaces were cleaned and activated with HCl acid for 5 min prior to electroplating. A Platinized Titanium plates used as anodes (also from Gold Plating Services). A series of experiments were done to find the optimum parameters, which gave a good throwing power through the holes, and the current density found to be the most important parameter. A moderate agitation also helped circulating of the solution inside the holes. The successful electroplating of 2 µm thick gold is summarized in Table III.

One single die was electroplated with the described process. The quality of the plated layer inside the holes was studied with SEM after cleaving the die, shown in Fig. 13. The results showed a uniform gold layer throughout the holes and convinced us that we could also have the bonded stacks electroplated with the same parameters and enough gold would be plated even inside the longer holes. Figure 14 shows the bonded stack of 13 dies, which was also electroplated. Due to the grain structure of this type of gold deposit the reflective qualities of the surface became matt.

| Temperature (°C) | Anode to Cathode Ratio | Current Density (mA/in²) | Time (min) |
|------------------|------------------------|--------------------------|-----------|
| 55 ± 1           | 3.5 : 1                | 20                       | 10        |

### III. EFFECTS OF TRAP IMPERFECTIONS ON CONFINEMENT TIME OF POSITRONS

#### A. Patch effects

If the entire surface inside the tubes is coated with gold with no roughness, the effect of potential asymmetries on the lifetime of a positron flying inside the microtrap can be estimated. With a work function variation (Δφ) of less than 1 mV for an evaporated gold surface, and estimation of the RMS potential variation along the axis...
of a cylindrical electrode, $RMS\Phi$, as \[22\]

$$RMS\Phi = \frac{0.6 \Delta \Phi l_c}{R_w}, \tag{1}$$

it is calculated that $RMS\Phi < 10^{-6}\,V$, when $R_w = 50\,\mu\text{m}$ and patch length, $l_c$, is comparable to the grain size of sputtered gold onto a silicon made microtrap, $0.1\,\mu\text{m}$.

The perpendicular drift velocity of a positron due to the patch field can be assumed as

$$V_\perp = \frac{E}{B}, \tag{2}$$

and also the movement as

$$\Delta x = V_\perp \frac{l_c}{V_0}, \tag{3}$$

where $V_0$ is the velocity by which the positron passes over the patch length (almost equal to the total velocity in a high magnetic field). The movement due to $N$ equal patches can be written then as

$$X^2 = N(\Delta x)^2. \tag{4}$$

Since $Nl_c = V_0 t$, by substituting $N$ and $\Delta x$ in Eq. \[1\] we obtain $t$ as

$$t = \frac{B^2 X^2 V_0}{E^2 l_c}. \tag{5}$$

One calculates $t \approx 4000\,s$, the time for the positron to get from the microtrap axis to the gold coated wall when $X = R_w = 50\,\mu\text{m}$ is the microtrap radius, $B = 7\,T$, $V_0 = 1.32 \times 10^6\,\text{m/s}$ for a $5\,\text{eV}$ positron, $l_c = 0.1\,\mu\text{m}$, and $E = (1\,\text{mV})/(50\,\mu\text{m}) = 20\,\text{V/m}$. The patch effects can be more problematic when there are areas of bare silicon, which result in more variation of the local surface work function. Thus we subjected the dies to gold electroplating after bonding in order to fill the micro-caves with gold.

### B. Dies and magnetic field misalignments

Magneto- and electrostatic errors which arise from misalignment of the trap cylinders or misalignment of the magnetic field direction with the microtrap longitudinal axis could be very problematic in microtraps. It has been reported \[4\] that with improvements in conventional PM traps fabrication and less sectors misalignment (0.1%), the trapped particles survived longer in experiments. Simulation conducted here helped us to better understand the importance of these parameters. Modeling simulations were carried out with WARP, a code used extensively in plasma physics \[23\]. In WARP, the particle-in-cell (PIC) method is employed. A discrete number of real particles positrons in this case are combined to so called macro-particles. The Lorentz equation of motion is employed to advance macro-particles in time. Following each time step, the charge density is calculated via a linear interpolation of the macro-particles position onto a mesh. By solving Poissons equation, the electrostatic potential is then calculated from the charge density. Since the rotational symmetry of the microtrap is broken in our cases, the three dimensional version of WARP is used for simulation. It uses a $xyz$ field solver with constant potential boundary conditions (i.e. Dirichlet conditions) at the electrode walls. A schematic of a $50\,\mu\text{m}$ radius microtrap modeled in our simulations is shown in Fig. 15. Modeling parameters are listed in Table I. The microtrap is composed of a central perfectly conducting, grounded tube and two end electrodes. The microtrap is immersed in a uniform, constant magnetic field of $7\,T$. The end electrodes potential are constant at $10\,V$. The startup parameters of the plasma played a vital role in reducing the computational effort. The major simulation parameters such as time step and mesh size were chosen carefully. Discordant values of them cause a large numerical instability. The choice of values for the parameters with the largest influence on numerical noise is discussed in another study \[1\]. The initial uniform plasma radius is $1/\sqrt{3}$ of the microtrap radius and its positron density is equal to $4.8 \times 10^{11}\,\text{cm}^{-3}$. With this density the space charge potential at the plasma axis is equal to $3.75\,V$ which is confined axially by $10\,V$ end electrodes.

FIG. 15: The schematic geometry of a microtrap and a plasma. The image is not to scale.

The central tube includes two $0.5\,\text{mm}$ long sectors misaligned to each other at the cases D2 and D3 while the magnetic field is perfectly axial ($\alpha = 0$). The misalignment, $\Delta$, is equal to $2\,\mu\text{m}$ and $5\,\mu\text{m}$, respectively. Figure 16 compares the histograms of trapped particles in these cases to the symmetrical microtrap in the case D1 with $\Delta = 0$ and $\alpha = 0$. Higher misalignment caused increasing the loss rate of positrons. When the misalignment is $5\,\mu\text{m}$, the loss rate accelerated in time. Almost linear loss rate was experienced for the $2\,\mu\text{m}$ misalignment, suggesting that the only one percent of positrons would be lost after $1\,s$.

In the cases B1 through B5, the main tube is a perfect cylinder with $\Delta = 0$. The simulation used two different lengths of the tube, $L_g$, equal to $0.5\,\text{mm}$ and $5\,\text{mm}$, which are consistent with underway experiments.
TABLE IV: The modeling parameters of the simulation.

| Case No. | ∆t (ps) | ∆R (µm) | PW (eV) | T₀ (µm) | α (°) | ℓ₀ (mm) |
|----------|---------|----------|--------|---------|-------|---------|
| D1       | 2.5     | 3.35     | 5      | 0.5     | 0     | 0       |
| D2       | 2.5     | 3.35     | 5      | 0.5     | 2     | 0       |
| D3       | 2.5     | 3.35     | 5      | 0.5     | 5     | 0       |
| B1       | 2.5     | 3.35     | 5      | 0.5     | 0    | 0.01    |
| B2       | 2.5     | 3.35     | 5      | 0.5     | 0    | 0.05    |
| B3       | 2.5     | 3.35     | 5      | 0.5     | 0    | 0.1     |
| B4       | 2.5     | 3.35     | 5      | 0.5     | 0    | 1       |
| B5       | 2.5     | 3.35     | 5      | 0.5     | 0    | 2       |

a Time step
b Mesh size
c Positron weight: the number of real particles that each simulation macro-particle represents.
d Overall length of the central tube

FIG. 16: The time histories of the number of trapped positrons in the cases D1, solid line, D2, dashed line, and D3, dot line.

The SU-8 photolithography was studied to obtain 80 µm uniform resist on 100 mm Si wafers. We have also studied Bosch process for deep reactive ion etching of high aspect ration holes. The trench width were optimized in order to resolve the entire features in the same time and avoid back notching at the hole bottoms. The Bosch etching technique proved to be successful process for anisotropic etching although we were not be able to eliminate the bowing effect completely due to the equipment limitation. The mask selectivity and the bowing defect were improved by reducing the etch and deposition step times (while the ratio of two steps kept constant) although strong striation was experienced since the pulses were not long enough to stabilize the plasma and obtain a reasonable duty cycle. We were able to gold sputter the entire surface inside the holes by sputtering the rotating dies on angle. However, some micro-caves were detected which were covered with gold during the gold electroplating of bonded stacks. We estimated the patch effects addressed in this study on the confinement times of the positrons and so the holes were gold electroplated in order to fill the micro-caves. More realistic effect of these stray electric fields on the lifetime of a confined particle ensemble in the plasma regime could be a subject of simulation while it is not expected to be a dominant factor since variations in the tube diameter, which

FIG. 17: The fraction of trapped positrons as the WARP simulation proceeds for different values of \( L_g \) and \( \alpha \).

FIG. 18: The fraction of trapped positrons versus the value of \( \alpha (L_g)^2 \). The data is fitted with the linear function, \( y = ax + b \), when \( a = -6.32 \pm 1.53 \) and \( b = 79.81 \pm 1.96 \).

IV. CONCLUSION

The SU-8 photolithography was studied to obtain 80 µm uniform resist on 100 mm Si wafers. We have also studied Bosch process for deep reactive ion etching of high aspect ration holes. The trench width were optimized in order to resolve the entire features in the same time and avoid back notching at the hole bottoms. The Bosch etching technique proved to be successful process for anisotropic etching although we were not be able to eliminate the bowing effect completely due to the equipment limitation. The mask selectivity and the bowing defect were improved by reducing the etch and deposition step times (while the ratio of two steps kept constant) although strong striation was experienced since the pulses were not long enough to stabilize the plasma and obtain a reasonable duty cycle. We were able to gold sputter the entire surface inside the holes by sputtering the rotating dies on angle. However, some micro-caves were detected which were covered with gold during the gold electroplating of bonded stacks. We estimated the patch effects addressed in this study on the confinement times of the positrons and so the holes were gold electroplated in order to fill the micro-caves. More realistic effect of these stray electric fields on the lifetime of a confined particle ensemble in the plasma regime could be a subject of simulation while it is not expected to be a dominant factor since variations in the tube diameter, which
are about $\approx 2\mu m$ with the current fabrication process, play a bigger role than that calculated from Eqs. 1 and 5. The work function of the electroplated surface will be measured by Kelvin probe technique. Smoother gold thin films are reported to be formed by thermal annealing at temperature of 160°C or above in the UHV chamber. Aligning and bonding of the dies were done using a precision-machined jig. Bonding proved to be successful while a misalignment of 4 $\mu m$ was achieved. Particle-in-cell WARP simulations showed that confinement of pure positron plasma columns in microtraps depends strongly on the alignment of the dies and magnetic field. Dies misalignments higher than 2 $\mu m$ affect largely on the storage capacity of the microtraps and cause accelerated losses due to the broken symmetry. Therefore, we will try to improve the alignment further during bonding. We also need to align the magnetic field carefully with microtraps axis. For the small values of field misalignment, the percentage of the trapped particles scaled with the value of $\alpha^{-1}(L_g)^{-2}$, where $L_g$ is the length of the trap in millimeters and $\alpha$ is the misalignment angle in degrees. Further experimental results using the fabricated array of microtraps to store charged particles will be published once the desired goals are achieved.

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