CMOS pixel sensor development for the ATLAS experiment at the High Luminosity-LHC

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Abstract: The current ATLAS Inner Detector will be replaced with a fully silicon based detector called Inner Tracker (ITk) before the start of the High Luminosity-LHC project (HL-LHC) in 2026. To cope with the harsh environment expected at the HL-LHC, new approaches are being developed for pixel detectors based on CMOS technology. Such detectors can provide charge collection, analog amplification and digital processing in the same silicon wafer. The radiation hardness is improved thanks to multiple nested wells which give the embedded CMOS electronics sufficient shielding. The goal of this programme is to demonstrate that depleted CMOS pixels are suitable for high rate, fast timing and high radiation operation at the LHC. A number of alternative solutions have been explored and characterised. In this document, test results of the sensors fabricated in different CMOS processes are reported.

Keywords: Particle tracking detectors (Solid-state detectors); Radiation-hard detectors; Solid state detectors
1 Introduction

The upgrade project of the LHC, called the High Luminosity-LHC (HL-LHC), is planned to be ready during 2026 after two years of installation and commissioning. This project intends to increase the instantaneous luminosity of the proton-proton collisions to more than $7.5 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, with an average of 200 expected inelastic interactions per bunch crossing (pile-up).

During the same period, major upgrades of the ATLAS detector will be installed. The upgrades are required to cope with increased particle multiplicity, large pile-up and huge radiation doses. Particular attention is needed in the design and construction of the Inner Tracker (ITk), which will replace the current inner detector. The ITk will be a fully silicon based detector which will be able to maintain good performance up to fluences of $2 \cdot 10^{16} n_{eq}/\text{cm}^{2}$ and doses of 1.7 GRad for the innermost part.

The current design foresees a strip detector in the outer part of the ITk. The strip detector will be composed of four barrel layers and six disks on each side of the end-cap [1]. A pixel detector composed of five barrel layers and four end-cap ring layers will be installed in the inner part to provide hermetic tracking coverage up to $|\eta| = 4$. The innermost layers of the pixel detector will consist of hybrid detectors, with planar or 3D silicon sensors bump-bonded to front-end readout chips. Hybrid detectors are produced with well established technologies and have proved to be reliable up to a fluence of more than $10^{16} n_{eq}/\text{cm}^{2}$.

In parallel to planar or 3D hybrid sensors, a monolithic CMOS sensor technology is been investigated for the outer layers of the pixel detector. In this region the requirements for radiation hardness and hit rate can be relaxed and a fully monolithic design could be a viable approach. This technology would reduce the budget material and potentially the power consumption per chip. Furthermore, production costs would be reduced and production yields is improved. The most striking difference with respect to the hybrid sensors is the absence of the bump bonding process. The monolithic CMOS technology can house the charge collection, the analog amplification and the digital electronics in the same silicon wafer. The charge collection is obtained by applying a reverse bias voltages (HV) of the order of 100 V. The combination of high voltage and CMOS technology is a novel concept for a monolithic devices [2]. Thanks to this a fast charge collection is possible, profiting from the signal obtained by charge drift. The analog and digital circuitries are
usually implemented in the a deep n-wells to be decoupled from the charge collection region in the p-substrate.

Two different sensor designs have been developed in the ATLAS CMOS Collaboration with the goal to produce a fully monolithic CMOS module.

**Small fill factor.** In this design the electronics are placed outside the charge collection wells. In addition the analog and digital circuitries are placed in separate wells minimising their cross talk. Noise and power consumption are minimised by the small capacitance between the electronic and the charge collection well. In order to increase the depletion region and further increase radiation hardness a process modification was developed by implanting a planar n-layer in epitaxial layer $p^+$ [3]. Figure 1 shows a schematic cross section of a sensor with small fill factor. This design is been investigated using the TowerJazz\(^1\) 180 nm CMOS process (manufactured by Tower Semiconductor).

![Schematic cross-section of a CMOS sensor with small fill factor](image)

**Figure 1.** Schematic cross-section of a CMOS sensor with small fill factor technologies with implantation of a planar n-layer in epitaxial layer $p^+$ [3].

**Large fill factor.** This design maximises the charge collection with a large electrode. The digital and the analog circuitries are implemented inside a common charge collecting well. Radiation hardness is achieved due to the electrode size and the depletion thickness. This design is based on AMS\(^2\) and LFoundry\(^3\) manufacturing technologies.

For the digital part of the chip, different architectures have been studied. In the Parallel Pixel-to-Periphery (PPtP) design [4] the hit information (address and timestamp) are transferred from pixels to the trigger buffer. Using the MonoPix readout [5, 6] the hit are firstly memorised in the active matrix and then transmitted using a synchronous column drain architecture. Alternatively, in the MALTA readout [6, 7], all of the hits are asynchronously transmitted to the end of column logic and no clock is distributed over the active matrix.

In this document, the results for chips using the large fill factor design produced by AMS are reported. In section 2, the test beam results on a small prototype of HV-CMOS pixel sensor in

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1http://towerjazz.com/

2Austria Micro Systems http://ams.com/

3http://www.lfoundry.com/
180 nm process are presented. In section 3, results for a larger chip are presented focusing on test beam and TCT results.

2 Test beam results for AMS H18 HV-CMOS pixel sensor prototype

Results for a sensor prototype produced using the HV-CMOS technology by the AMS foundry are presented. This sensor, referred to as \textit{CCPDv4}, is the 4\textsuperscript{th} revision of a series of prototypes using the AMS H18 process in 180 nm. The resistivity of the substrate is 10 $\Omega$cm with a total sensor size of 2.4 $\times$ 2.9 mm$^2$ and a thickness of 250 $\mu$m (figure 2). Different pixel types are implemented in this sensor. The results are focused on the \textit{STime} Pixel on the HV-CMOS sensor with a pixel size of 33 $\times$ 125 $\mu$m$^2$. Each pixel contains an amplifier and a discriminator, together with a 4-bit in-pixel DAC that allows for the tuning of the individual pixel thresholds. All the electronics are implemented in the deep N-well (figure 3). The CCPDv4 sensors are glued to the FE-I4B readout chip \cite{8} using Araldite 2011 non-conductive epoxy glue.

![Figure 2](image2.png)

\textbf{Figure 2}. Assembly of a FE-I4 pixel readout chip to HV-CMOS CCPDv4 sensor via capacitive coupling \cite{9}.

![Figure 3](image3.png)

\textbf{Figure 3}. Schematic cross section of a HV-CMOS sensor: the deep n-well is the charge-collecting electrode and also contains additional CMOS circuits such as a preamplifier \cite{9}.
In order to test the radiation tolerance of the sensor, samples have been irradiated with 1 MeV neutron equivalent dose of $1 \times 10^{15}$ n$_{eq}$/cm$^2$ and $5 \times 10^{15}$ n$_{eq}$/cm$^2$ at the TRIGA reactor in Ljubljana [10]. Further irradiation campaigns have been performed at the Bern Cyclotron Laboratory [11] using 18 MeV protons at $1.3 \times 10^{14}$ n$_{eq}$/cm$^2$ and $5 \times 10^{14}$ n$_{eq}$/cm$^2$.

The samples have been tested in November 2015 at the H8 beamline of the CERN SPS (Super Proton Synchrotron), that provides a 180 MeV $\pi^+$ beam. The FE-I4 Telescope [12] based on RCE readout system was used for this test. This telescope consists of 6 planes of ATLAS Insertable B-Layer (IBL) [13] double-chip (DC) pixel modules [14] arranged in two arms of three module each. Upper limits on the spatial resolution of the telescope were found to be 11.7 $\mu$m and 8.3 $\mu$m in the XY plane at the device under test (DUT) position.

The reconstructed charged particle trajectories (tracks) are compared to the hit position in the DUT. The hit efficiency has been calculated as the ratio between the number of clusters in the DUT that match the reconstructed tracks from the beam telescope and the number of good reconstructed tracks that are predicted to penetrate the DUT within its active area.

The results of this study are reported in figure 4. The hit efficiency is shown as a function of the bias voltage for different samples irradiated with neutrons or protons. A plateau is reached after about 40 V. Increasing the bias voltage results in a higher efficiency in particular for the lowest and highest fluence. The results show an increase of efficiency between $1.3 \times 10^{14}$ n$_{eq}$/cm$^2$ and $5 \times 10^{14}$ n$_{eq}$/cm$^2$ and then a loss of efficiency with increasing dose. This behaviour is due to acceptor removal phenomena and is supported also by the edge-TCT results show in this document. For each sample the threshold has been optimised in order to equalise the response of the individual pixel sensors.

![Figure 4. Average hit efficiency as a function of applied bias voltage obtain using the FE-I4 Telescope at the SPS H8 beamline with 180 MeV pion beam. The inset shows the sudden increase in efficiency between 80 and 85 V, which can be attributed to charge multiplication. The thresholds of 70, 80, 90 and 100 mV are assumed to be equivalent to 600, 690, 770 and 860 $e^-$ [9].](image-url)
Figure 5. a) Layout of the H35 Demonstrator. The reticle dimensions are 18.49 mm × 24.40 mm. (b) Layout of one pixel from the second analog matrix. The pixel dimensions are 50 µm × 250 µm. Detail of the prototype can be found in this article [15].

3 Characterization of H35 Demonstrator sensor

The H35 Demonstrator, shown in figure 5, is a large demonstrator chip (18.49 × 24.40 mm²) produced using the 350 nm HV-CMOS technology from AMS [15]. The chip has been produced in different resistivities 20, 80, 200 and 1000 Ω cm. The layout of the sensor is composed of four different pixel matrices:

- **Standalone nMOS matrix** (300 × 16 pixels): this matrix contains digital pixels with in-pixel Charge Sensitive Amplifiers (CSAs) shapers and nMOS discriminators embedded in the same deep N-well acting as a collecting electrode. The nMOS discriminator output signal is connected to the periphery of the matrix where an additional CMOS discriminator is included in the readout cell. Different pixel types are included in this matrix: half of the pixels have time-walk compensation.

- **Two analog matrices** (300 × 32 pixels): containing in-pixel amplification that can be capacitively coupled to the ATLAS FE-I4 readout chip. Five different types of pixels with different amplification gains and time response are implemented.

- **Standalone CMOS matrix** (300 × 16 pixels): in this matrix the pixel structure is the same as the nMOS matrix but does not include the in-pixel discriminator. The analog signals are directly transmitted to the CMOS discriminator in the periphery. Only one pixel type is present in this matrix.
The pixel size for all of the four matrices is $50 \times 250 \mu m^2$. In addition to these four matrices, the chip contains a $3 \times 3$ pixel matrix test structure. Each pixel is characterised by a pixel area of $50 \times 250 \mu m^2$. Three deep N-wells are present in each pixel: a central N-well of $50 \times 110 \mu m^2$ containing a deep P-well and two external wells of $50 \times 70 \mu m^2$.

**Test beam measurement.** The CMOS matrix of the $200 \Omega cm$ sensor has been characterised in the H8 line at the CERN SPS using the FE-I4 Telescope [12]. In order to operate the CMOS matrix, a readout system has been developed by the Institut de Fisica d’Altes Energies (IFAE). This readout is synchronised with the telescope through a busy-signal scheme [16]. The CMOS matrix has been tuned globally using an external voltage. The pixel thresholds can be adjusted using the dedicated on-chip 4-bits DAC register. In the results presented in this section this feature was not exploited. An example of tuned threshold distribution is shown in figure 6. The matrix has been divided in two Region Of Interest (ROI) since different behaviours of the threshold have been observed. In figure 7 the hit efficiency is presented for the two region of the matrix as a function of the pixel threshold voltage.

![Figure 6](image)

**Figure 6.** Pixel threshold tuning of the CMOS matrix of a $200 \Omega cm$ H35 Demonstrator chip [16].

**Edge TCT results.** A characterisation of the depletion region at different distances from the implant surface of the H35 Demonstrator chip has been performed. This measurement is important since a minimum ionising particle crossing a silicon sensor induces a signal of amplitude proportional to the depth of the depleted volume. The measurement has been done measuring the charge collected using a Transient-Current-Technique (TCT). The set-up consists of a 1064 nm infra-red (IR) pulsed laser that illuminates the detector under test (DUT) which is mounted on a movable stage. The IR laser light penetrates the silicon bulk and generates electron-hole pairs along its trajectory. The electron-hole pairs drift in the electric field and induce a current pulse which is acquired. In order to study the depletion depth the laser has been mounted to illuminate the edge of the sensor rather than the top surface in a configuration called **edge-TCT**. The optical system can
be moved along the beam axis to focus the laser on the DUT. The laser beam area at its focus has a Gaussian width of about 10 $\mu$m. The study has been done using both unirradiated and irradiated sensors. A full characterisation of a H35 Demonstrator irradiated with protons at TRIGA reactor has also been performed [17].

Figure 8 shows the depth of the depleted volume as a function of the bias voltage for different stages of neutron irradiation. The depleted volume increases with irradiation, reaching a maximum
Figure 9. Depletion depth against bias voltage for the 200Ωcm sample for different fluence steps up to $1.6 \cdot 10^{15} n_{eq}/cm^2$. This sample was irradiated with proton at the Bern Cyclotron. The pink dashed arrows indicate the consecutive fluence steps.

after a cumulative fluence of $1 \cdot 10^{15} n_{eq}/cm^2$. It decreases after exposition to a total fluence of $2 \cdot 10^{15} n_{eq}/cm^2$, converging to a larger depletion depth than the one observed before irradiation. Preliminary results for the samples irradiated with 18MeV protons at the Bern Cyclotron are presented in figure 9. For protons the maximum of the depletion region was found to be at lower dose $1 \cdot 10^{14} n_{eq}/cm^2$.

4 Conclusion

Pixel sensor based on CMOS technology can be a valid option for the ATLAS ITk upgrade. A possible area of application would be the outer layers of the pixel detector of ITk. In this document, results for a sensors with large fill factor have been presented focusing on test beam and TCT characterisations.

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