Neuromorphic Computing with Deeply Scaled Ferroelectric FinFET in Presence of Process Variation, Device Aging and Flicker Noise

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Abstract—This paper reports a comprehensive study on the applicability of ultra-scaled ferroelectric FinFETs with 6 nm thick hafnium zirconium oxide layer for neuromorphic computing in the presence of process variation, flicker noise, and device aging. An intricate study has been conducted about the impact of such variations on the inference accuracy of pre-trained neural networks consisting of analog, quaternary (2-bit/cell) and binary synapse. A pre-trained neural network with 97.5% inference accuracy on the MNIST dataset has been adopted as the baseline. Process variation, flicker noise, and device aging characterization have been performed and a statistical model has been developed to capture all these effects during neural network simulation. Extrapolated retention above 10 years have been achieved for binary read-out procedure. We have demonstrated that the impact of (1) retention degradation due to the oxide thickness scaling, (2) process variation, and (3) flicker noise can be abated in ferroelectric FinFET based binary neural networks, which exhibits superior performance over quaternary and analog neural network, amidst all variations. The performance of a neural network is the result of coalesced performance of device, architecture and algorithm. This research corroborates the applicability of deeply scaled ferroelectric FinFETs for non-von Neumann computing with proper combination of architecture and algorithm.

Index Terms—Ferroelectric FinFET, Process Variation, Flicker Noise, Device Aging, Neuromorphic Computing, Multi-level coding.

I. INTRODUCTION

The advent of LeNET[1, 2] in recent times has made machine learning or neural network-based computation an inevitable choice for solving many complex tasks. But the artificial neural networks (ANN) implemented in such traditional von-Neumann computing system endure severe bottleneck during the data transfer between segregated memory unit and processing unit. Therefore, this computer science-based approach of [3, 4] ANN in these data centers fails to imitate the true brain functions in terms of power consumption and speed of operations. Therefore, a notable interest in the area of emerging non-volatile memory based non-Von-Neumann computing oriented implementation of low power neural networks[5, 6, 7, 8, 9, 10, 11, 12, 13, 14] has grown and the arrivals of Loihi chip from Intel[15] and TrueNorth[16] from IBM rang the bell for next generation computing architecture. Amidst many developments the research on the feasibility of implementing neural networks on hardware and the quest for finding a perfect synaptic device is still on.

The implementation of neuromorphic chip should take into following considerations;

- Vulnerability of synaptic devices towards scaling.
- Non-volatility of the synaptic devices.
- Architecture and algorithm optimization.

 Pronounced ferroelectricity in single layer thin film of hafnium zirconium oxide (HZO)[17], fast switching, high on/off ratio, excellent linearity in analog synaptic weight updates, bi-directional operation and good endurance are the key technological factors, which makes ferroelectric field effect transistors (FE-FET) superior to phase change memory, resistive memory and magnetic memories for synaptic devices. However, it is well-known that the device to device variations in FE-FETs increases with scaling[18] and the switching becomes stochastic, which inhibits reliable program and erase method in deeply scaled FE-FETs. Although recent research has shown 3bit/cell operations in FE-FETs [19], which came with additional power consumption, device size and latency, making it awry for neural network applications.

In this work we present a 16nm technology node compatible deeply scaled FE-FinFET as a synaptic device. We have investigated DNN applications focusing on the offline training scenario, where pre-trained weights are programmed to FE-FinFET devices via a novel closed-loop adaptive-program-and-read algorithm to mitigate the impact of systematic variation on DNN inference accuracy. Apart from the variation during program and erase operation, flicker noise and device aging also plays a pivotal role in FE-FinFET based neural networks. This work is the first demonstration of the combined impact of process variation, device aging and flicker noise on the neural network application. The cornerstone of this work is to mitigate the impact of process, device aging and flicker noise induced variations in all-FE-FinFET based CIM operation without affecting device scaling, power requirements and latency.

II. EXPERIMENTS

We begin our investigation by fabricating HZO based FE-FinFETs with minimum fin width of 18nm and gate length of 50nm. 6nm thick HZO was deposited on top of an 1.5nm...
thick interfacial layer (IL) of SiO$_2$ by atomic layer deposition (ALD). Fig. 1a shows the schematic and fig. 1b shows the transmission electron microscopic (TEM) micrograph of our fabricated device.

![Schematic of the fabricated device](image1)

Following the fabrication of our device, we have conducted dc characterization using B1500A semiconductor analyzer and pulsed program-erase operations and retention test have been conducted using B1530A module from Keysight Technologies. The flicker noise analysis was conducted by 9812B from proplus solutions. The system neuromorphic simulation was conducted using CIMulator platform[20]. In the following section we shall discuss the results of the above mentioned experiments along with the implications of process variation, device aging and flicker noise on the performance of deep neural network for MNIST hand-written digit recognition task.

III. RESULTS AND DISCUSSION

Fig. 2 depicts counter clockwise swing (CCW) in the $I_{ds}$ - $V_g$ characteristics of FE-FinFET obtained by slowly varying gate voltage at constant drain voltage of 100mV. The counter clockwise swing in n-type FE-FinFET corroborated the dominance of ferroelectricity over traps in the fabricated device. The threshold voltage ( $V_{th}$) is extracted at constant drain current of 20nA and we can observe a memory window (MW) of 0.75V, which is defined as the difference in threshold voltage during forward ($V_{th}^f$) and reverse ($V_{th}^r$) sweep (MW=$\Delta V_{th}$=$V_{th}^f$-$V_{th}^r$). The maximum theoretical limit of MW of FE-FinFET with 6nm thick ferroelectric layer is 1.2V[21]. The reduction of the static MW from the ideal value can be attributed to the channel side trapping[22]. Although MW is an important parameter for any memory device, the leakage current and the ratio of "ON" and "OFF" current is more important aspect for the neuromorphic applications, where power consumption should be as low as possible without inhibiting the performance. The leakage current of the fabricated FE-FinFET is around few tens of pA and the ON-OFF ratio is $10^6$.

Apart from the magnitude of OFF current and ON/OFF ratio, symmetry and linearity in analog programming is an important aspect to be considered. Fig. 2b shows highly symmetric and linear modulation of $V_{th}$ obtained by applying 100ns wide pulses of increasing(decreasing) amplitude with a step size of 100mV(-100mV). During program and erase operation the source and drain terminal of the device were kept at ground and the pulse was applied to the gate terminal and during read operation we applied 100mV at drain terminal, keeping source at ground and a non-destructive fast voltage sweep was performed at the gate terminal. Owing to the availability of fewer domains, the switching characteristics in planar deeply scaled FE-FETs are abrupt[23] and only shows two distinct $V_a$ levels, but in case of FE-FinFETs the presence of ferroelectric domains around the side walls of the fin facilitate the analog programming phenomena also in the deeply-scaled devices.

![Normalized Pulse Number vs Gate Voltage](image2)

We have achieved highly linear and symmetric 32 distinct memory states. Fig. 2c compares the linearity of the analog states with other state of art devices and it is evident from the Fig. 2c that the fabricated device shows excellent linear and symmetrical analog states under the applied pulse scheme.
Cycle to cycle variation during program and read operation is another important parameter to be considered. Fig. 2d shows cycle to cycle variation during read operation and Fig. 2e shows the cycle to cycle variation during program and erase operations. It is evident from the Fig. ?? and ?? that the fabricated device depicts very low cycle to cycle variation, which can be attributed to good interfacial oxide quality and optimized ALD process.

Although the characterization of a stand-alone single device depicts low leakage current, 32-different conducting states and low cycle to cycle variation, the device to device variation should also needs to be analyzed for enabling the multi-level-coding operation using ultra-scaled devices for system level applications. The root cause for device to device variation can be attributed to ferroelectric switching process, random distribution of remnant polarization, coercive voltage, ferroelectric-dielectric domains, presence of different trapping sites and surface roughness at the interface[24, 25]. The impact of these variations becomes acute, when the device is further scaled down. Fig. 5 shows the cumulative impact of these variations while the device is programmed using voltage pulse of small pulse width and amplitude. The resultant high infidelity in the change of channel conductance ($G_{ch}$) states for deeply scaled devices, when a single pulse is applied to program has been show in fig. 5. Although, voltage pulses of higher amplitude and width can abate the variations, but they will also increase the latency and power consumption. Therefore, in this work we exploit a novel closed loop program and read approach to reduce these variations. The program and erase technique has been shown in fig. 6. For gate length independent fast(100ns) low power programming with high fidelity, we used 100ns write pulse to program and erase the FE-FinFETs. The stability of read gate voltage ($V_{g}^{read}$) is of utmost important to implement this algorithm. $V_{g}^{read}$ should not alter the programmed state and should be free from flicker noise. Therefore, a sanity check of $V_{g}^{read}$ induced $G_{ch}$ check is done at the beginning. While we find a stable range of $V_{g}^{read}$, we program the device to lowest resistance state (11) using a 100ns pulse at 4.5V and a read operation is performed. If, the $G_{ch}$ is found to be within the desired range, we erase the device to highest resistance state (00); otherwise we alter $V_{g}^{read}$ to obtain the desired $G_{ch}$. Similar operation is conducted for the states “01” and “10”.

Fig. 4b shows proposed architecture for implementing this algorithm at the array level. Array-level inference throughput optimization for the proposed scheme requires further system level study. Fig 4c shows the resultant states obtained through such closed-loop adaptive program and read scheme. Random Gaussian distribution of $G_{ch}$ is formed with measured mean and variance after closed-loop write operation to evaluate the variation for each state (4d).

![Figure 3](image1.png)  
**Figure 3.** The overlapping channel conductance states show that process-variation prevents fast programming and erase operation in deeply scaled devices.

![Figure 4](image2.png)  
**Figure 4.** (a) System level adaptive-program-read operations algorithm deployed in this work for abating the device to device variation and facilitate multi-level coding in sub-10nm HZO based devices. (b) Proposed block-diagram for implementing adaptive-program-read operations. (c) The 4-level-coding in 6nm HZO based FE-FinFET. (d) The histogram for depicting the variation in 4-level multi-level cell operations.

**Table: I Device Level Bench-marking**

| Attributes               | This Work | [19] | [26] | [27] |
|-------------------------|-----------|------|------|------|
| Cell Area($\mu$m$^2$)   | 10$^{-3}$ | 0.25 | 0.025| 0.026|
| FE Thickness(nm)        | 6         | 20   | N/A  | 15   |
| Program Pulse           | ±4.5V     | ±10V | ±4.2V| ±10V |
|                         | 100ns     | 300ns| 10ns | 300ns|
| Endurance               | ≥ 10$^8$  | 10$^7$| 10$^7$| 10$^8$|

Table I shows the benchmarking of our fabricated device with other state of art FE-FETs. This is the first demonstration of 2-bit/cell operation in such small FE-FinFET device with 6nm ferroelectric layer. The pulse width and amplitude used for program and erase operation also ensures low power consumption. The endurance of our measured device is above 10$^8$ program-erase cycles, which also makes our device suitable for online training.

Fig.5a shows the neural network architecture, where both online and offline training process can be implemented. In this
work we present only the impact of variations during offline training as offline training will reduce the power consumption as well as it will also increase the device life time. The training operation uses a data-set of 60000 MNIST images, the inference operation is conducted on 10000 MNIST data. During the offline training process the network is pre-trained by the software and the FE-FinFET devices are programmed to the desired conductance state. The training process is supervised, which means it has both feed forward and back propagation functions. During the inference operation, we only use feed forward method for offline training. The stored weights will not be changed during inference and thus we evaluate the stability and fidelity of the FE-FinFET devices in the CIMulator[20].

Finally, we evaluate the conductance drift due to device aging(Fig. 6a) and flicker noise(Fig.6b) induced variation in our fabricated devices. We have used 100ns wide pulse of amplitude ±2.5V to program and erase the device. We observe a 22.6% change in $G_{th}$ for HRS and 73.4% in $G_{th}$ for LRS. The change of $G_{th}$ for the intermediate states were obtained by linear interpolation. The change in $G_{th}$ was captured using a macro model to apply in system level neural network simulation. The flicker noise characterization 6b at various bias conditions depicts that drain current fluctuation is less than 0.7%. At lower bias voltage, while the trapping and de-trapping is limited, we can observe a Lorentzian trend [28] in flicker noise measurement and gradually the flicker noise takes 1/f trend when the bias voltage increases. This flicker noise measurement gives us an insight about the read voltage optimization for reducing the impact on flicker noise during read operation.

![Image](210x379 to 220x382)

Table: II Impact of Variations on DNN Inference

|                | Digital | 2-bit/cell | Analog |
|----------------|---------|------------|--------|
| Baseline       | 96.4%   | 97.6%      | 95.9%  |
| Device-to-device $G_{th}$ Variation | $[\Delta G_{th} = 15\%]$ | $[\Delta G_{th} = 15\%]$ | $[\Delta G_{th} = 15\%]$ |
| Device Aging $G_{th}(t) = \sim -23\%$ | 96.1% | 95.9% | 10% |
| Flicker Noise $\alpha L = 0.7\%$ | 96.0% | 46.3% | 10% |
| C2C Variation | 96.0% | 45.8% | 10% |

Figure 6. (a) The retention characteristics shows steep degradation of programmed conductance level over time owing to high depolarization field.(b) The flicker noise follows Lorentz model at low gate voltage and as the gate voltage is increased the trapping and de-trapping increases and the flicker noise follows 1/f trend.

To fathom the impact of device to device variations on binary-cell and 2-bit/cell devices we have trained the neural network using binary and 4-level/cell synapses on two separate occasions. DNN training process for MNIST digits recognitions for both binary and 4-level/cell (multi-level cell, MLC) synapse, achieving maximum accuracy of 95.5% and 97.5% (Fig. 5b), respectively. The impact of device to device (D2D) variation that arise from inaccurately programmed $G_{th}$ shows a mere 0.3% degradation for the MLC and 0.06% for binary cell (Fig. 5c).

![Image](250x316 to 259x356)

Figure 5. (a) The neural network architecture used for simulating the performance of FE-FinFET based synaptic devices. The input is an image of hand-written digit. For simplifying the task of hardware implementation the image is converted to gray scale image with a size of 28x28 pixels. Therefore, the neural network has 784 input layers which corresponds to 28x28 pixels, 200 hidden layers and 10 output layers. The conductance variation, device aging and flicker noise models have been included while evaluating the performance of the fabricated FE-FinFET devices. (b) Accuracy vs of Epochs for binary and 4-level operations. The simulation is conducted without considering device to device variation present. The 4-level cell shows better performance then binary cell. (c) The degradation in MNIST data recognition accuracy is only 0.3% in presence of device to device variation. Device to device variation is insignificant in CIM operations.

Table: II shows the system level performance of all FE-FinFET based neural network. We have considered three scenarios where the first case is all-digital binary neural network (BNN) case, where the variation-induced accuracy degradation minimal. Scenario B is the closed-loop programmed 4-level
states (as in Fig. 4). The accuracy degradation due to device to device variation and device aging is not severe in this case, however a significant accuracy degradation is observed due to flicker noise and cycle to cycle variation. Scenario C is the analog synapse, where the impact of device to device variation can be abated by the neural network architecture, but the impacts of device aging, flicker noise and cycle to cycle variation becomes severe for this case.

IV. CONCLUSION

We have fabricated, characterized and evaluated the performance of 6nm HZO based deeply scaled FE-FinFETs for neuromorphic computing. The device to device variation, cycle variation, flicker noise impact and conductance drift as an aftermath of device aging was modelled and we observed that the digital synapse is the key to robust DNN inference. Although the impact of device to device variation of digital, analog and 2-bit/cell synapse can be abated by the neural network, the degradation in accuracy due to cycle to cycle variation, device aging and flicker noise becomes severe for analog and 2-bit/cell synapses. It may also be noted that systematic variation has a stronger impact than random variation. Therefore, we conclude that for robust DNN application with deeply scaled FE-FinFETs digital synapse is the way.

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