Quantized Neural Network Inference with Precision Batching

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Abstract

We present PrecisionBatching, a quantized inference algorithm for speeding up neural network execution on traditional hardware platforms at low bitwidths without the need for retraining or recalibration. PrecisionBatching decomposes a neural network into individual bitlayers and accumulates them using fast 1-bit operations while maintaining activations in full precision. PrecisionBatching not only facilitates quantized inference at low bitwidths (< 8 bits) without the need for retraining/recalibration, but also 1) enables traditional hardware platforms the ability to reactualize inference speedups at a finer granularity of quantization (e.g: 1-16 bit execution) and 2) allows accuracy and speedup tradeoffs at runtime by exposing the number of bitlayers to accumulate as a tunable parameter. Across a variety of applications (MNIST, language modeling, natural language inference) and neural network architectures (fully connected, RNN, LSTM), PrecisionBatching yields end-to-end speedups of over 8× on a GPU within a < 1% error margin of the full precision baseline, outperforming traditional 8-bit quantized inference by over 1.5×-2× at the same error tolerance.

1. Introduction

Recent advances in deep learning have demonstrated the wide range of the applications of neural networks (Krizhevsky et al., 2012; Hochreiter & Schmidhuber, 1997; Sutskever et al., 2014; Graves et al., 2013; Bengio et al., 2003; Rajpurkar et al., 2016; Wang & Jiang, 2015; Dao et al., 2019). Applying a neural network to make predictions, termed inference, is computationally expensive, exacts high energy costs and often demands specific latency requirements (e.g: a speech recognition neural network must be fast enough in decoding human language for a real time virtual assistant). Research in quantization aims to reduce the computational costs and thus improve the speed of neural network inference (Hubara et al., 2016; 2017; Xu et al., 2018; Sze et al., 2017). Generally, quantization reduces the precision of neural network weights / activations and speeds up inference by facilitating the use of high throughput low precision operations and by reducing the amount of memory transfers (Lin et al., 2015; Xu et al., 2018; Krishnan et al., 2019).

Importantly, quantization incurs an increasingly larger accuracy penalty when quantizing to lower bitwidths (Hubara et al., 2017; Choi et al., 2018). For this reason, state of the art quantization methods often retrain or recalibrate their neural networks to achieve sufficient accuracy at lower bitwidths (Choi et al., 2018; Zhu et al., 2016; Xu et al., 2018; Han et al., 2015; 2016b; Lam, 2018; Zhou et al., 2017). It is also common to require architectural changes to the neural network in addition to retraining (Zhu et al., 2016; Xu et al., 2018). At the time of writing, state of the art quantization methods for bitwidths < 8 typically involve retraining and recalibration. There are two key issues with this: 1) retraining a neural network for a target bitwidth is computationally expensive, often taking much longer to train than its full precision counterpart, requiring a separate hyperparameter tuning process for convergence and best results (Hubara et al., 2016; Choi et al., 2018; Hubara et al., 2017) and 2) retraining/recalibrating a neural network requires access to data that matches the distribution of the training/test set (Wu, 2018; Li et al., 2017), which may not be available (e.g: a machine-learning service provider like Google Cloud or Amazon Web Services may have access only to the model but not the data). Thus, a core motivation is the development of a quantized inference method that works out of the box and can extend to below 8 bits with corresponding speedups while maintaining accuracy.

Additionally, research on quantized neural networks often involve the development of specialized hardware and it is unclear how their techniques translate to inference speedups on traditional hardware architectures (e.g: GPUs and CPUs) (Choi et al., 2018; Albericio et al., 2017; Sharma et al., 2017). Concretely, traditional CPUs and GPUs lack the necessary datatypes for more unusual bitwidths (e.g: 2-bit, 3-bit). Thus, another core motivation is the development of a quantized inference algorithm that can be leveraged in context of existing hardware platforms to speed up inference at lower bitwidths (< 8 bits).
We present PrecisionBatching an ad-hoc algorithm for quantized inference targeted to traditional hardware platforms. PrecisionBatching is based on the following observations:

1. Weights and activations may be decomposed into a sum of 1-bit tensors. Fast 1-bit operations may be leveraged for computation involving these terms. By accumulating more bitlayers, higher precision and accuracy may be attained at higher computational cost.

2. Activations are harder to quantize than weights as they not only may have a larger spread (via multiply accumulate) but dynamically change depending on the input to the neural network. This motivates keeping activations in higher precision to avoid significant loss of accuracy and the need to retrain/recalibrate. Activations are kept in higher precision by batching the decomposed 1-bit tensors; results are obtained by reducing the batch after the forward operation.

3. Neural network inference in deployed applications typically involves small batch sizes indicating that computation is primarily limited by how fast data can be moved between the compute and memory units. Although batching across precision increases the amount of compute operations, this extra cost is hidden by memory accesses. An overall speedup is obtained by reducing the amount of memory accesses performed and is proportional to the number of bitlayers accumulated.

The key idea of PrecisionBatching is to leverage the high compute efficiency of traditional hardware platforms to operate over higher precision activations, leading to significant gains in model quality while maintaining the speed of low bitwidth quantized inference. By reframing \( n \)-bit weight, \( k \)-bit activation operations as a sum of 1-bit operations, any level of quantized execution (e.g. 1-16 bit) may be performed on traditional hardware platforms (Figure 1). As each product is performed over a binary matrix, memory is reduced by \( 32 \times \) per term, yielding a net speedup despite a \( k \times \) increase in compute. We highlight that our algorithm is targeted for inference at deployment with a batch size of 1 to minimize latency (Fowers et al., 2018; NVIDIA, 2015; Han et al., 2016a).

To demonstrate the value of PrecisionBatching, we develop optimized computational kernels to perform our algorithm on the GPU and evaluate our method against standard quantized inference implementations (NVIDIA’s Cutlass linear algebra library (NVIDIA, 2018)) on various applications including fully connected networks for MNIST and LSTMs/RNNs for language modeling and natural language inference. Across this range of applications and models we demonstrate significant end-to-end speedups over using standard quantized inference methods (> \( 10 \times \) over full precision inference, \( 1.5 \times - 2 \times \) over standard 8-bit quantized inference, at the same error margins). Our contributions are as follows

- We develop PrecisionBatching an algorithm for quantized neural network inference targeted to traditional hardware platforms (e.g. CPU and GPU). PrecisionBatching enables quantized inference at lower bitwidths and achieves better speedup per accuracy over standard quantized operations (e.g. 8/16-bit weights and activations operations) without retraining.

- We evaluate PrecisionBatching over a variety of applications (MNIST, language modeling, natural language inference) and neural network architectures (fully connected, LSTM, RNN) and show net speedups of > \( 10 \times \) over the full precision baseline (> \( 1.5 \times - 2 \times \) over standard 8-bit quantized inference) within the same error tolerance. Furthermore, we leverage the finer granularity of precisions supported by PrecisionBatching to boost speed vs model quality.

- We release optimized GPU kernels for our algorithm (and corresponding baselines) in the form of PyTorch modules.

2. Related Work

2.1. Post Training Quantization

Post training quantization is the standard method for quantizing neural networks without retraining and involves clipping the values of a pre-trained model based on statistics (Zhao et al., 2019). Various methods for post training quantization have been researched. Naively, post training quantization involves casting weight and activation values to the nearest \( n \)-bit representation. More sophisticated techniques involve clipping the weights and activations so as to minimize some form of error between the quantized and real values (Wu, 2018; Zhao et al., 2019). Even more advanced techniques change the underlying floating point format to enhance speed/accuracy (Tambe et al., 2019; Lee et al., 2017;
Pre-existing research in post training quantization methods often omit details as to how the resulting quantized weights/activations may be leveraged on existing CPU and GPU platforms to speed up inference. More unusual bitwidths (e.g: 2/3/4/5) lack a corresponding data type on traditional hardware platforms and hence it is unclear how these levels of quantization improve inference. The implied benefit of post training quantization methods on these bitwidths is either space/memory savings or deployment to specially developed hardware accelerators for which fixed point operations for various bitwidths may be developed. By framing n-bit fixed point inference operations as a sum of binary operations, PrecisionBatching is an effective solution to realize these quantization gains on traditional hardware platforms. Hence, PrecisionBatching extends the memory-savings benefits of various post training quantization methods to speed gains on traditional hardware architectures.

2.2. PACT

The importance of activations in quantization quality has been noted in research. Specifically, PACT (Parameterized Clipping Activation for Quantized Neural Networks) (Choi et al., 2018) demonstrated that neural network weights and activations may be quantized to very low bitwidths (< 4) if an activation scale is optimized during training. Although PACT requires changes to the training process (and hence does not work out of the box), their research demonstrates the importance and difficulty of quantizing activations in maintaining quantization quality. Motivated by their findings, PrecisionBatching opts to keep activations in higher precision (8, 16, 32 bit) to maintain accuracy at very low quantization level. This comes at minimal cost during inference as compute is dominated by memory access times. Thus, PrecisionBatching circumvents the need to maintain a quantization scale at training time by giving more bits of precision to activations at inference time.

2.3. Outlier Channel Splitting

Recently, research into quantization without retraining has emerged as a topic of interest. One notable work is Outlier Channel Splitting (Zhao et al., 2019), which eliminates large magnitude weights/activations (which increase quantization error) by splitting them into separate channels, then applying standard post training quantization on the split weights, improving quantization performance. Outlier Channel Splitting demonstrates better performance-per-bit by using their technique in conjunction with standard post training quantization methods. Importantly, the authors note that outlier channel splitting may also be done to activations at runtime, though this is computationally difficult as it requires repeatedly finding the maximum of a matrix and adding rows to it. PrecisionBatching eliminates this need by using more bits to represent activations, improving accuracy. Like many standard post-training quantization methods, Outlier Channel Splitting may be applied along with PrecisionBatching to improve quantization quality and to extend their memory-saving gains to speed gains on traditional hardware platforms.

2.4. Bitserial Computation

In hardware architecture research, bitserial computation is a technique similar to PrecisionBatching for quantized inference and similarly operates by decomposing fixed point operations into bitwise operations (Judd et al., 2016; Albericio et al., 2017; Sharma et al., 2017). Like PrecisionBatching, bitserial computation frames n-bit fixed point operations as a sum of bitwise operations and accumulates the result layer by layer. Importantly, this technique/formulation is applied primarily to develop specialized hardware accelerators for machine learning and realizing the technique requires dedicated hardware constructs. Various hardware accelerators that leverage the bitserial formulation to reduce energy costs include (Judd et al., 2016; Albericio et al., 2017; Sharma et al., 2017). PrecisionBatching differs as it targets traditional CPU and GPU platforms and does not require the development of specialized hardware. The key idea is that on traditional architectures low batched inference is memory bound and by batching the decomposed 1-bit vectors the extra overhead in compute is negated by the reduction in memory accesses, yielding a net speedup.

2.5. Streamlined Deployment for Quantized Neural Networks

Another related work to PrecisionBatching is Streamlined Deployment for Quantized Neural Networks (Umuroglu & Jahre, 2017), which leverages a bitserial formulation to speed up deployment on the CPU. Similar to PrecisionBatching, Streamlined Deployment for Quantized Neural Networks frames quantized operations in terms of 1-bit operations. However, the key difference is that Streamlined Deployment separates the the bitlayers of the activations into different product terms, rather than batching them into one large matrix multiplication. As shown in their paper, the impact is that both weights and activations must be kept in very low precision (e.g: 2-bit activations) due to the computational overhead of performing multiple matrix products, which naturally leads to significant degredation in accuracy. The key observation of PrecisionBatching is that activation bitlayers may be batched together into one single matrix and a single large matrix product may be performed over this batch at high efficiency. This allows quantized inference with activations at or near full precision with minimal computational overhead, enhancing quantization performance.
3. Precision Batching

3.1. Precision Batching Quantized Inference

At a high level, PrecisionBatching decomposes weights and activations into 1-bit tensors and replaces the main matrix-vector multiplication operation with a sum of 1-bit matrix-matrix operations. The core operation of neural network inference with a batch size of 1 is matrix-vector multiplication.

\[ L_i(x) = Wx \]

\( L_i \) represents the function that transforms activation input \( x \) at the specific layer of the neural network and \( W \) is the trained weights of the neural network at layer \( i \). Assuming that \( W > 0 \) and \( x > 0 \), we can decompose \( W \) and \( x \) into a sum of bitlayers (binary tensors) as in fixed point format

\[ W = \frac{1}{2^{16}}(2^{n-1}W_1^{(b)} + \ldots + 2^0W_n^{(b)}) \text{ where } W_i^{(b)} \in [0, 1] \]

\[ x = \frac{1}{2^{16}}(2^{k-1}x_1^{(b)} + \ldots + 2^0x_k^{(b)}) \text{ where } x_i^{(b)} \in [0, 1] \]

In the decomposition above, \( n \) and \( k \) represent the precision at which weights and activations are quantized to, respectively. Making \( n \) and \( k \) larger provides more accurate approximations of \( W \) and \( x \). \( n \) describes the precision at which \( W \) is estimated and represents the number of bitlayers to accumulate. The fraction \( \frac{1}{2^{16}} \) represents the location of the fixed point and enables representation of values 16 binary digits \(< 1 \). The fixed point may be changed depending on the scale of values of the weights and activations. Substituting back into the first equation and rearranging we get

\[ L_i(x) = Wx \]

\[ = \frac{1}{2^{32}}(2^{n-1}W_1^{(b)} + \ldots + 2^0W_n^{(b)})(2^kx_1^{(b)} + \ldots + 2^0x_k^{(b)}) \]

The key observation is that the terms of the sum above can be rewritten as a single matrix multiplication. The idea is to batch together the bitlayer decomposition of \( x \) into a single matrix and to frame the equation as a sum of matrix-matrix products.

\[ \sum_{i=0}^{n} 2^{n-i-1}(W_i^{(b)}[x_1^{(b)} \ldots x_k^{(b)}])(2^k \ldots 2^0) \]

The main workload \( W_i^{(b)}[x_1^{(b)} \ldots x_k^{(b)}] \) exclusively consists of terms that are binary and facilitates efficient computation using 1-bit operations on CPU and GPU. Memory is reduced by a factor of approximately \( \frac{32}{n} \), given that the matrix \( W \) dominates the majority of memory accesses. Note that the number of compute ops is increased by a factor of \( k \) as separating out the sum induces more work. However, as the reformulation leverages batching, the cost of the extra compute is negated by the higher computational efficiency of the matrix-matrix multiplication, and the reduction in memory accesses yields a net speedup. Concretely, memory overheads are often \( 10 \times -100 \times \) slower than a typical operation (Norvig, 2015) and significant gains may be attained by reducing these memory operations at the cost of extra arithmetic instructions.

As indicated, by choosing \( n \) and \( k \), any precision of weights and activations can be attained. In this paper \( k \) (activation precision) is set to either 8, 16 or 32. Note that higher activation precision does not linearly impact performance due to the increase in computational efficiency. However, for CPUs that are less efficient (more compute bound), setting \( k \) to be lower may significantly improve overall speed versus accuracy; hence \( k \) and \( n \) are parameters that determine the precision and speedup for quantized execution and may be tuned to the platform and requirement at hand. We analyze the impact of varying \( n \) and \( k \) on both speed and accuracy in the results.

Note that both the inputs and outputs of the PrecisionBatching algorithm (as well as intermediate values such as partial sum accumulators) are full precision. The overhead of maintaining inputs and outputs as full precision is minimal as much of the computational and memory costs are attributed to large matrix multiply routines which are quantized (much of the memory costs are from loading the weights, rather than loading activations/inputs). Thus, keeping the intermediate inputs/activations in full precision is still aligned with the high level goal of speeding up inference.

Additionally, while the PrecisionBatching formulation primarily targets matrix-vector multiplication (appropriate under the assumption that execution over a batch size of 1 is a matrix-vector multiply), this technique can be extended to any matrix-matrix product and hence handle any routine that involves general matrix multiplication.

In this work, we primarily investigate models where inference over a batch size of 1 is handled by a matrix-vector multiplication, which limits us to feed forward networks, RNNs and LSTMs. Important future work involves the extension of this technique to general matrix products, which may be applied to CNNs, transformers and batched low precision training.

3.2. Extending to Negative Values

Note in the previous formulation that we assume \( W > 0 \) and \( x > 0 \). Here we extend the formulation to any real valued \( W \) and \( x \) matrix. Allowing any real valued input and matrix is important as it enables PrecisionBatching to handle weights with negative values and cases where the input is
not passed through a positive activation function (e.g. the first layer of the neural network whose inputs are real and may potentially contain negative values). The simple but effective idea is to leverage two’s complement by adding an extra bitlayer with a negative scale to handle negative values.

\[
W = \frac{1}{2^n}(-2^n W_0^{(b)} + 2^{n-1} W_1^{(b)} + \ldots + 2^0 W_n^{(b)}), \quad W_i^{(b)} \in [0, 1]
\]

\[
x = \frac{1}{2^n}(-2^k x_0^{(b)} + 2^{k-1} x_1^{(b)} + \ldots + 2^0 x_k^{(b)}), \quad x_i^{(b)} \in [0, 1]
\]

Here, the first bitlayer for both \(x\) and \(W\) are negated, allowing for a complete representation of values between \([-2^n, 2^n - 1]\). This formulation is logically equivalent to two’s complement format. Note that this technique incurs an extra bitlayer of computational overhead (for weights) and thus increases the computational and memory costs; we found in practice that the extra bitlayer of computational overhead for activations is minimal.

### 3.3. Weight/Activation Quantization

In the PrecisionBatching formulation, \(W\) and \(x\) are effectively converted into fixed point format and quantized to reduce computation and memory accesses. However, any standard post training quantization technique (e.g.: KL divergence, MSE, etc) can be applied to \(W\) and \(x\) to improve accuracy, as long as the resulting set of quantization values are linearly spaced.

For applications, we use standard post training quantization before quantized execution.

\[
Q(W) = d \times \text{round}\left(\frac{W}{d}\right), \quad d = \frac{\max(W) - \min(W)}{2^n}
\]

Effectively, this rounds \(W\) to the corresponding closest \(n\)-bit representable fixed point values. We found that in practice, rounding produces significantly better results than truncation at very lower bitwidths (< 4 bits). Additionally, for quantizing to 1 bit, we found it extremely beneficial to exclude representing 0 and instead opt to represent a positive and negative value. After the \(n\)-bit rounding, \(Q(W)\) is applied in the PrecisionBatching algorithm where the corresponding bitlayers and scales are deduced. Additionally, we also optimize over a clipping threshold to find a quantized matrix with the smallest mean error versus the full precision weight matrix. Note that quantizing \(W\) is a preprocessing step that is done offline and hence does not affect inference performance measurements.

Quantizing activations \(x\) utilizes a much simpler and efficient algorithm as it has to be done at runtime: truncation. For \(x\) we simply convert \(x\) from floating point to 32-bit fixed point (integer format) with a multiplication and a cast, which naturally drops bits outside the 32-bit range.

The full PrecisionBatching algorithm is broken into two stages: a preprocessing step which converts full precision weights to bitlayers, listed in algorithm 1, and the inference stage which makes predictions given a full precision input, listed in algorithm 2.

#### Algorithm 1 PrecisionBatching Quantization Preprocessing

| Input          | Output          |
|----------------|-----------------|
| \(W\)          | Bitlayers \(W^{(b)}\) |
| \(n\) Number of bits to quantize | Scales \(S^{(b)}\) |

1: \(W_q \leftarrow \text{Int}(\text{QuantizeRound}(W, n) \times 2^{16})\)
2: \(\text{max}_b \leftarrow \max(\log_2(|W_q|))\)
3: \(W^{(b)} \leftarrow [W_q \land (1 \ll i) \text{ for } i \text{ in } \text{max}_b - n .. \text{max}_b + 1]\)
4: \(S \leftarrow [1 \ll i \text{ for } i \text{ in } \text{max}_b - n .. \text{max}_b + 1]\)
5: \(S[0] \leftarrow S[0] \times -1\)
6: return \(W^{(b)}, S\)

#### Algorithm 2 PrecisionBatching Quantized Inference

| Input          | Output          |
|----------------|-----------------|
| \(W^{(b)}\) Weight bitlayers | Full precision prediction |
| \(S^{(b)}\) Weight bitlayer scales | \(z\) |
| \(x\) Full precision input |  |

1: \(z \leftarrow 0\)
2: \(x_q \leftarrow \text{Int}(x \times 2^{16})\)
3: for \(W_b, \text{scale in } W^{(b)}\), \(S\) do
4: \(z \leftarrow z + \frac{\text{scale}}{2^{30}} \times (W_b x_q)[-2^{31}, 2^{30} .. 2^0]\)
5: end for
6: return \(z\)

#### 3.4. Efficient Implementation

As indicated above, the core computation is an accumulation of products of binary tensors.

\[
W_i^{(b)} [x_1^{(b)} ... x_k^{(b)}]
\]

As all values are 0 or 1, memory is reduced by packing the 0s and 1s into the bits of an integer array, yielding \(32\times\) reduction in memory for each product of bitlayers. Operating over these packed formats is inspired by standard binary quantized neural networks which uses logical operations and popcounts for implementing multiply accumulate. An important difference is that typical binary quantized neural network weights contain values that are -1 or 1 rather than 0 or 1. Hence, instead of the \(\text{xor}\) operation we use the \(\text{and}\) operation to simulate 1-bit multiplication. To leverage these instructions, the floating point input vector must be converted to fixed point and then packed in such a way to layout the bits to be conducive to the \(\text{and/popcount}\) instruction. Conversion to fixed point is a simple multiply and cast.
Rearranging the bits is done with a bitwise matrix transpose, for which there are efficient implementations on both CPUs and GPUs that leverage parallelism / SIMD. In practice, we found the bitwise matrix transpose to have negligible overhead. We furthermore note that multiple bitlayers may be stacked together so that the entire product across bitlayers can be performed with a single operation. However, in practice we found that there is negligible performance difference in accumulating multiple bitlayers separately.

3.5. Integer Quantized Inference

Standard quantized inference methods quantize both weight and activation to the same precision before execution (so that both operands are the same datatype); for example, 8-bit quantized execution quantizes both weights and activations to 8-bit ints before operation. Weights and activations are scaled down before quantization (so that the maximum value is representable in the quantized range), then dequantized after the operation. Like in PrecisionBatching we apply the same quantization preprocessing steps (rounding, optimizing a clipping threshold) to weights before evaluation. Traditional CPU and GPU platforms provide support for 8-bit integer matrix operations and 16-bit floating point operations; more recent GPUs with tensorcores also support 4-bit and 1-bit integer matrix multiply operations. In our experiments, we leverage NVIDIA’s T4 tensorcore capability (via NVIDIA’s Cutlass linear algebra library) in the implementation of the standard quantized inference baselines.

4. Results

4.1. Precision Batching Kernel Performance

We implement optimized GPU kernels for the PrecisionBatching algorithm and measure the speedup of the kernel over the full precision (32-bit) operation (provided by NVIDIA’s Cutlass linear algebra library) across multiple precisions and matrix sizes. Inference times include all activation processing steps necessary for the algorithm, for example, transposing the activation bitmatrix before 1-bit execution. Baseline 4, 8 and 16 bit matrix multiplies utilize the NVIDIA Cutlass library which performs low-precision matrix multiply using WMMA (warp matrix multiply accumulate) hardware operations that leverage Tensorcores for compute. In all experiments the batch dimension is 1.

We perform all performance benchmarks on NVIDIA’s Tesla T4 GPU. We measure the wall-clock time of performing 1000 iterations of the target algorithm (to amortize setup and cache costs). Note that performance gains on applications may be higher than those reported in kernel measurements as applications access more memory than in the benchmarks.

Table 1 shows the performance of the PrecisionBatching kernel with weight bits \( b \in \{1, 2, 4, 8\} \) and activation bits \( a \in \{8, 16, 32\} \), along with baseline quantized inference kernels (Int1, Int4, Int8, Float16, Float32). We see that at fewer bits, the PrecisionBatching kernel achieves significant speedups over full precision inference: 10-14x speedup for 1-bit, 5-7x for 4-bit (note that the optimal speedup for PBatch-n is \( \frac{32}{n+1} \) with the sign layer taken into account). Using fewer activation bits increases performance only slightly as compute is not the main bottleneck in these operations.

Generally, higher performance is seen at larger matrix sizes as the effect of the reduction in memory on performance is more pronounced. Baseline kernels (Int1, Int4, Int8 especially) perform much better at larger matrix sizes; we believe this is the case as their kernels are more optimized than ours and leverage Tensorcore capability for more efficient compute.

4.2. Benefits of Higher Precision Activations

Next we show that using higher precision for activations leads to significantly better model accuracy at low bitwidths. We benchmark model accuracy across three applications: MNIST, language modeling and natural language inference. For each we train one baseline full precision model and evaluate the effects of various levels of weight and activation quantization on the model’s end performance. For each model/application we quantize weights and activations to 1, 4, 8, 16 and 32 bits.

For the MNIST task (LeCun & Cortes, 2010), we train a 3-layer fully connected neural network with a hidden size of 4096 for 20 epochs, reaching a baseline accuracy of 98%. We uniformly quantize the weights and activations of each layer to the target precisions.
Table 2. Benefits of using more precision for activations on model quality, evaluated on MNIST, language modeling (Wikitext-2) and natural language inference (SNLI). Generally, using higher level activations allows quantizing twice as many bits (e.g: from 8-bits to 4-bits) with little degradation of model accuracy. Note that for accuracy (acc), higher is better, whereas for perplexity (ppl) lower is better (the best score for each weight precision is bolded).

For language modeling, we train a model with a 1-layer 2048 unit LSTM (Hochreiter & Schmidhuber, 1997) as the encoder, and a 1-layer 2048 unit fully connected as the decoder (a common architecture used in language modeling (Melis et al., 2017)). We apply dropout with a factor of .5 to the inputs of the encoder LSTM’s recurrence, and to the encoder LSTM’s output. We train the model on the Wikitext-2 dataset (Merity et al., 2016) for 40 epochs, reaching a baseline perplexity of 93. During evaluation of quantization on model accuracy, we quantize the LSTM’s input and hidden layers to the same weight and activation levels; however, we keep the final fully connected decoder in full precision.

For natural language inference, we train a model with a 1-layer 3072 unit LSTM encoder and a 3-layer 3072 unit fully connected decoder (a larger version of that seen in (Bowman et al., 2015)). We train on the SNLI dataset (Bowman et al., 2015) for 10 epochs and reach a baseline accuracy of 78%. During evaluation of quantization on model accuracy, we uniformly quantize both the weights and activations of the LSTM encoder and the fully connected decoder to the target precisions.

Table 2 shows model performance (accuracy for MNIST and natural language inference, perplexity for language modeling) for different weight and activations precisions. For weight bitlevels < 8, keeping activations at higher precision (8, 16 or 32 bit) greatly increases model accuracy; generally, keeping activations at a higher precision allows quantizing twice as many bits, from 8-bits to 4-bits, without significant loss in model accuracy. For MNIST, with 1-bit weights, using higher precision activations is the difference between 85% accuracy and random guessing (10% accuracy); with 4-bit weights, higher precision activations maintains within <1% of the full precision model’s performance. Similarly, for language modeling, with 1-bit weights, higher precision activations reduces perplexity from 800 to 180; for 4-bit weights, higher precision activations reduce perplexity from 180 to within a few points of the full precision performance.

For natural language inference, using full precision activations allows us to quantize down to 1-bit with only a couple percentages of accuracy degradation (78% to 76%), whereas quantizing activations to 1-bit degrades to random guessing (33%). Interestingly, for language inference, the 8-bit quantized model outperformed the full precision result, a known phenomenon seen in quantization literature (Krishnan et al., 2019; Xu et al., 2018).

4.3. End to End Performance Gains

We combine the observations from our previous results: we leverage the high runtime performance of the Precision-Batching kernel and the better model accuracy of keeping activations in higher precision to attain significant end-to-end speedups over the full precision model while maintaining model quality. We use the same applications (MNIST, language modeling (Wikitext-2) and natural language inference (SNLI)) with the same model architectures and training parameters described previously.

We apply each target quantized inference algorithm as follows. For the MNIST model, we replace each linear layer with the corresponding quantized inference algorithm; for the language modeling and natural language inference Seq2Seq model, we replace each linear layer of the encoder 1-layer LSTM with the target quantized inference algorithm, however we keep the final fully connected decoder in full precision.

Additionally, for both the baseline quantized inference and Precision-Batching, we use variable-bit quantization on different layers (e.g: 1-bit quantization on layer 1, 4-bit quantization on layer 2, etc) to further boost performance per accuracy. Accordingly, we perform an exhaustive grid search over weight/activation precision assignments. On the 3-layer fully connected for MNIST, for baseline quantized inference we assign each layer a precision ∈ {1, 4, 8, 16, 32} (note that for quantized inference activations are the same precision as weights); for Precision-Batching, we assign each layer a precision ∈ {1, 2, 3, 4, 8} and activations ∈ {8, 16, 32}. On the Seq2Seq LSTM for language modeling and natural language inference, for baseline quantized inference we assign each layer a precision ∈ {1, 4, 8, 16}; for Precision-Batching, we assign each layer a precision ∈ {1, 2, 4, 8} and activations ∈ {8, 16, 32}.

In benchmarking the runtime performance of each model/application, we measure the wall clock time of inference with a batch size of 1 for 10 iterations on a given input repeated over 10 runs and take the minimum. We measure speedups by comparing the model with the target quantized inference algorithm against the model with the baseline quantized inference method.

Figure 2 shows the Pareto curves of the end-to-end speedups...
We present PrecisionBatching, a quantized inference algorithm for speeding up neural network execution on traditional hardware platforms at low bitwidths without the need for retraining or recalibration. Across various models (fully connected, LSTMs, RNNs) and applications (MNIST, language modeling, natural language inference) we show that PrecisionBatching yields end-to-end speedups of over 8× that of full precision inference (1.5× - 2× that of standard 8-bit quantized inference) at the same error tolerance. Importantly, we see this work as a modest yet significant step towards tackling the broad and long-standing challenge of maintaining high system efficiency during neural network execution. In many areas of neural network execution performance is bottlenecked by the massive amount of memory transfers necessary for the task. PrecisionBatching demonstrates that more precision for activations may be attained at minimal cost by leveraging the higher compute efficiency of traditional hardware platforms, leading to significant gains in model accuracy at low bitwidths. While this work demonstrates the gains on a GPU, important future work involves engineering this technique to peak performance on CPUs. Although the authors have made significant efforts to attain the same speedups on the CPU, the lack of vectorized popcount instructions on current hardware limited success; we believe future hardware with these capabilities (e.g: Intel’s Ice Lake Processor) will facilitate significant performance gains on CPUs. Additionally, while this work focuses on matrix-vector multiplication (low batch dimension), it is extensible to general matrix-matrix products; important future work involves applying PrecisionBatching to a broader range of models such as CNNs and attention-models as well as extending it to a training and federated learning setting.

5. Discussion

We present PrecisionBatching, a quantized inference algorithm for speeding up neural network execution on traditional hardware platforms at low bitwidths without the need for retraining or recalibration. Across various models (fully connected, LSTMs, RNNs) and applications (MNIST, language modeling, natural language inference) we show that PrecisionBatching yields end-to-end speedups of over 8× that of full precision inference (1.5× - 2× that of standard 8-bit quantized inference) at the same error tolerance. Importantly, we see this work as a modest yet significant step towards tackling the broad and long-standing challenge of maintaining high system efficiency during neural network execution. In many areas of neural network execution performance is bottlenecked by the massive amount of memory transfers necessary for the task. PrecisionBatching demonstrates that more precision for activations may be attained at minimal cost by leveraging the higher compute efficiency of traditional hardware platforms, leading to significant gains in model accuracy at low bitwidths. While this work demonstrates the gains on a GPU, important future work involves engineering this technique to peak performance on CPUs. Although the authors have made significant efforts to attain the same speedups on the CPU, the lack of vectorized popcount instructions on current hardware limited success; we believe future hardware with these capabilities (e.g: Intel’s Ice Lake Processor) will facilitate significant performance gains on CPUs. Additionally, while this work focuses on matrix-vector multiplication (low batch dimension), it is extensible to general matrix-matrix products; important future work involves applying PrecisionBatching to a broader range of models such as CNNs and attention-models as well as extending it to a training and federated learning setting.

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