Design of Capacitor-less LDO applied to Low Power Supply with High-precision Bandgap

Sheng Li1,a, Xiaoning Xin2,b, Ren Jian3,c*, and Jinghang Pang4,d

1School of Information Science and Engineering, Shenyang University of Technology, Shenyang, Liaoning Province, China
2School of Information Science and Engineering, Shenyang University of Technology, Shenyang, Liaoning Province, China
3School of Information Science and Engineering, Shenyang University of Technology, Shenyang, Liaoning Province, China
4School of Information Science and Engineering, Shenyang University of Technology, Shenyang, Liaoning Province, China

aemail: lisheng950@163.com, bemail: xinxn2007@163.com,
demail: 1356868430@qq.com.com,
c*Corresponding author’s e-mail: renj@sut.edu.cn

Abstract. This paper proposes a capacitor-less low dropout regulator (LDO) applied to low power supply to meet the needs of low power consumption and highly integration. In order to improve the transient response of the system, a dynamic bias circuit is designed, which can automatically track the change of load current. In addition, the temperature coefficient of bandgap reference in conventional LDO is generally 20-100 ppm/°C. The bandgap reference circuit proposed in this paper can achieve 1.73 ppm/°C without trimming, and the accuracy is better than 1% at all process corner. The design and simulation are based on TSMC 0.18 μm CMOS process, the simulation results show that the LDO output voltage is 1 V when input power supply voltage is 1.2 V. The proposed regulator can operate with a minimum dropout voltage of 200 mV when load current is 50 mA. The maximum undershoot and overshoot voltages are 34 mV and 28 mV, respectively, with 1mA-50mA and 50mA-1mA step load current.

1. Introduction
With the development of portable electronic devices, wearable electronics and a variety of 5G devices, there is an increasing demand for chip integration. LDO are widely used as the most critical module in the chip to provide stable power for the system. For battery-powered circuits, such as some portable electronic devices, require low power consumption to extend standby time and are highly integrated[1]. Conventional LDO requires a several μF capacitor off-chip, which increases the area and is not conducive to integrate. This also dictates that the development trends of LDO are low supply voltage and capacitance-less[2],[3]. However, the lack of off-chip capacitance can cause transient response degradation, resulting in the LDO failing to operate properly when the load change, so it is essential to design transient response boost circuit. Meanwhile, the output voltage of conventional bandgap reference circuit in LDO is usually above 1.2 V, which cannot meet the demand of low input voltage.
of LDO. And the accuracy of the output voltage of bandgap reference directly affects the output of LDO, so it is necessary to design a low output voltage and high precision bandgap[4].

2. Structure of proposed LDO

![Figure 1. Top-level block structure of proposed NMOS LDO.](image)

In the proposed approach, resistance feedback loop circuit is not needed. Figure 1 shows the block diagram of the LDO voltage regulator, which consists of an error amplifier (EA), a bandgap reference (BG), a non-overlapping circuit (NOV), a charge pump (CP), and a NMOS regulation FET (MN). The CP is used to increase the gate drive voltage of the regulation FET to ensure that the MN has a large enough VGS, and the BG provides an accurate reference voltage for the system.

3. Analysis and design of LDO

3.1. Bandgap reference circuit

The conventional bandgap reference output voltage is generally above 1.2 V with a temperature coefficient (TC) of 20-100 ppm/℃, the trimming technology will greatly increase the cost[5]. In this paper, a V-shaped voltage curvature compensation (VSCC) bandgap reference circuit is designed to offset the curvature of output voltage $V_{REF}$ over a wide range of temperature, effectively narrow the variation of reference voltage, and have a TC of less than 2 ppm/℃ and high accuracy.

![Figure 2. Schematic diagram of bandgap reference circuit.](image)

In order to get a temperature-independent current, a positive-TC and a negative-TC current is required. In the diagram of Figure 2, OPA1 and OPA2 are error amplifiers, the ratio of Q1 and Q2 is 8:
1. Due to the clamping effect of the amplifier, the voltage of A, B and C is equal. ΔVEB is a positive-TC voltage while VEB is a negative-TC voltage. Therefore, IPTAT and ICTAT are given by:

\[
I_{PTAT} = \frac{\Delta V_{EB}}{R_1}
\]

(1)

\[
I_{CTAT} = \frac{V_{EB}}{R_4}
\]

(2)

\[
I_{REF} = K_1I_{PTAT} + K_2I_{CTAT}
\]

(3)

As shown in Figure 3, the slope of IPTAT is 9.34 nA/℃ and the slope of ICTAT is -17.8 nA/℃ in the range of -40 ℃ to 140 ℃. Temperature-independent current IREF can be obtained by adjusting the size of M10 and M11. M3-M9 form a V-shaped voltage curvature compensation circuit. When \(K_3I_{PTAT}\) is larger than \(K_4I_{CTAT}\), the transistor M8 get into the triode region and the dominant component of \(I_V\) is \(K_4I_{CTAT}\), and when \(K_4I_{CTAT}\) is larger than \(K_3I_{PTAT}\), the transistor M8 operates in the saturation region while \(K_3I_{PTAT}\) is the main current. The bandgap output voltage \(V_{REF}\) is given as follows:

\[
V_{REF} = I_{REF}R_2 + (I_{REF} - I_1)R_3 = (K_1I_{PTAT} + K_2I_{CTAT})(R_2 + R_3) - I_1R_3
\]

(4)

\(I_1R_3\) in (4) is an inverted V-shaped voltage, the output of bandgap is a convex curve voltage without VSCC. The temperature compensation range can be adjusted by adjusting the width of M3 and M4[6].

![Figure 3. IPTAT and ICTAT.](image)

![Figure 4. Bandgap output voltage VREF.](image)
The bandgap reference output voltage is shown in Figure 4, the $V_{REF}$ varies by 0.249 mV from -40 °C to 140 °C with a TC of 1.73 ppm/°C.

3.2. Voltage doubler charge pump

Figure 5 is the cross-coupled charge pump used in this paper, QB, Q is not overlapping clock signal, to avoid the charge leakage caused by M13, M14 conduction at the same time. M13 and M14 are switch FET that control the power supply to charge C1 and C2, M15 and M17 keep the body of M16 and M18 always at high potential, and M16 and M18 control C1 and C2 to alternately charge the output capacitor C4. The output voltage of the charge pump can be raised to approximately 2VIN, the charge pump output ripple $V_{RIPPLE}$ is given by:

$$V_{RIPPLE} \approx \frac{I_{OUT} T}{C_4}$$

In equation (5), $T$ is the charge pump clock period, $I_{OUT}$ is the charge pump output current. It can be seen that the higher the clock frequency, the smaller the output ripple; the larger the output terminal capacitance, the smaller the output ripple. Considering the output ripple and the chip area, the capacitance $C_4$ in the charge pump output is set to 50pF and the clock frequency is 10MHz.

3.3. Transient response boost circuit

The dynamic bias NMOS LDO structure proposed in this paper is shown in Figure 7. MN is the regulation FET, M38, M39, M40 is the current sampling circuit. M33, M34, M35, M36, M37 constitute the dynamic bias circuit, and M19-M30 constitute the error amplifier (EA). $V_{CP}$ is the voltage doubler charge pump output voltage, which is approximately 2.3V at an input voltage of 1.2V and a clock oscillation frequency of 10MHz, to raise the gate voltage of MN above $V_{IN}$. The EA adopts a two-stage cross coupled common gate and cascode structure, with M19-M22 constituting the error amplifier cross coupled input stage. The source of M19 and M21 connected to the reference voltage and the source of M20 and M21 connected directly to the LDO output. M23-M30 form the output stage of the EA, the cascode output provide a high output impedance and enhanced the drive
capability of EA. Dynamic bias and current sampling circuit enhance LDO transient response when load current $I_{LOAD}$ is changed.

Figure 7. Proposed dynamic biased LDO with NMOS regulation FET.

4. LDO measurement results

In this paper, the LDO is designed and simulated based on TSMC 0.18 $\mu$m CMOS process. As shown in Figure 8, when $I_{LOAD}$ change from 1 mA to 50 mA within 1 $\mu$s, the undershoot voltage is 34 mV. When the $I_{LOAD}$ change from 50 mA to 1 mA within 1 $\mu$s, the overshoot voltage is 28 mV.

Figure 8. Measured load transient reponse.

Figure 9. Line regulation.
The power supply ripple rejection is expressed as the ability of the output to suppress power supply noise, it can be expressed as:

$$ PSR = 20 \log_{10} \frac{V_{OUT-ripple}}{V_{IN-ripple}} $$  

The linear regulation reflects the ability of the LDO to suppress changes in the DC voltage of the power supply. As shown in Figure 9, simulating the power supply voltage from 1.2 V to 1.5 V at a full $I_{LOAD}$ of 50 mA, the linear regulation is 16.3 mV/V. As shown in Figure 10, the $I_{LOAD}$ of the LDO in this paper is simulated from 1 mA to 50 mA, the load regulation is 5 mV/A.

5. Conclusion
The LDO regulator without off-chip capacitor with NMOS regulation FET is experimentally simulated for all parameters in this paper, which employs a high-precision bandgap reference circuit and an adaptive bias circuit that can operate at low supply voltage and significantly improve the load transient response of the regulator. The proposed LDO is an appropriate candidate for portable power management applications.

References
[1] C. Yang, K. Ye and M. Tan, "A 0.5-V Capless LDO With 30-dB PSRR at 10-kHz Using a Lightweight Local Generated Supply," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 10, pp. 1785-1789, Oct. 2020.
[2] H. Mo and D. Kim, "Multiple-output LDO regulator applying with constant feedback factor," 2017 International SoC Design Conference (ISOCC), Seoul, 2017, pp. 194-195.
[3] N. Adorni, S. Stanzione and A. Boni, "A 10-mA LDO With 16-nA IQ and Operating From 800-mV Supply," in IEEE Journal of Solid-State Circuits, vol. 55, no. 2, pp. 404-413, Feb. 2020.
[4] K. Sanborn, D. Ma and V. Ivanov, "A Sub-1-V Low-Noise Bandgap Voltage Reference," in IEEE Journal of Solid-State Circuits, vol. 42, no. 11, pp. 2466-2481, Nov. 2007.
[5] X. Xin and Y. Fu, "A Precision Constant Current Source Design with Trimming and Compensation," 2012 International Conference on Control Engineering and Communication Technology, Liaoanig, 2012.
[6] C. Lee et al., "A High-Precision Bandgap Reference With a V-Curve Correction Circuit," in IEEE Access, vol. 8, pp. 62632-62638, 2020.
[7] J. Ren, F. Wang, R. Min and X. Xin, "Parallel Integrated State Variable Filter Circuit Design," 2018 IEEE 3rd International Conference on Integrated Circuits and Microsystems (ICICM), Shanghai, 2018.