VersaGNN: a Versatile accelerator for Graph Neural Networks

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Abstract—Graph Neural Network (GNN) is a promising approach for analyzing graph-structured data that tactfully captures their dependency information via node-level message passing. It has achieved state-of-the-art performances in many tasks, such as node classification, graph matching, clustering, and graph generation. As GNNs operate on non-Euclidean data, their irregular data access patterns cause considerable computational costs and overhead on conventional architectures, such as GPU and CPU. Our analysis show that GNN adopts a hybrid computing mode. The Aggregation (or Message Passing) phase performs vector additions where vectors are fetched with irregular strides. The Transformation (or Node Embedding) phase can be either dense or sparse-dense matrix multiplication. In this work, We propose VersaGNN, an ultra-efficient, systolic-array based versatile hardware accelerator that unifies dense and sparse matrix multiplication. By applying this single optimized systolic-arrays to both aggregation and transformation phases, we have significantly reduced chip sizes and energy consumption. Then divide the computing engine into blocked systolic arrays to support the Strassen’s algorithm for dense matrix multiplication, dramatically scaling down the number of multiplications and enabling high-throughput computation of GNNs. To balance the workload of sparse-dense matrix multiplication, we also introduced a greedy algorithm to combine sparse sub-matrices of compressed format into condensed ones to reduce computational cycles. Compared with current state-of-the-art GNN software frameworks, VersaGNN achieves on average 3712× speedup with 1301.25× energy reduction on CPU, and 35.4× speedup with 17.66× energy reduction on GPU.

I. INTRODUCTION

Graph Neural Networks (GNNs) have achieved state-of-the-art performances in node classification [18], [26], link prediction [25], [48], graph classification [46], graph generation [25], [40], and clustering [39], [46] on arbitrarily structured graphs. The power of representation learning on graphs comes from feature embedding, which includes extracting structured, low dimensional features from unstructured, high dimensional graphs.

On one hand, traditional Convolutional Neural Networks (CNNs) [29] that operate on Euclidean data are characterized by local connections and shared weights, and are able to extract multi-scale localized spatial features. Euclidean data, such as images, can be represented as regular grids in the Euclidean space. Thus, a CNN is able to exploit the shift-invariance and local connectivity of Euclidean data. On the other hand, GNNs inherit the irregular computing patterns and processing dataflow of graph analytics, resulting in the inefficient use of CPUs and GPUs.

Meanwhile, the majority of real-world graphs for GNNs follow the Power-Law distribution - the number of nodes with degree \( N \) is proportional to \( N^{-\alpha} \) for some constant \( \alpha \) [14]. Thus, a minority of nodes share high degrees, leading to remarkably unbalanced adjacency matrices. Therefore, hardware architectures must adapt to the varying shapes of the high-dimensional convolutions in GNN. Generally, two primary execution phases, Aggregation and Transformation, occupy the most execution time [11], [18], [43], [45].

Aggregation (Message Passing) Phase: GNN follows a neighborhood aggregation strategy in which each node’s representation is updated by aggregating features of its adjacency. Common aggregation strategies include Sum, Average, Mean, and Max. After \( N \) iterations of aggregation, a node’s representation captures the structural information within its \( N \)-hop network neighborhood. The main computation kernels are data loading, which collects feature vectors that are indexed by the neighboring node’s addresses, and the execution of aggregation. Due to their sparsity, the feature vectors can be efficiently fetched by coalescing their elements. Within the feature matrix, the feature vectors of adjacent nodes can be separated by strides. Poor use of these inter-vertex data parallelism can incur significant cache misses and address calculations.

Transformation (Node Encoding) Phase: This phase is usually expressed as a Multi-layer Perceptron (MLP) that transforms node feature vectors to lower dimensional embeddings using Matrix-Vector Multiplication (MVM). The matrix multiplication can be either dense or sparse, depending on the sparsity of feature matrices at different convolutional layers. A non-linear activation function is applied to each vertex to yield the outputs. This phase is characterized by regular computational graph and homogeneous data access patterns.

To accelerate GNN-based applications that harness these two distinct stages and process highly variable real-world graphs, we propose several optimization approaches for accelerating GNN with a software/hardware co-design paradigm. Our main contributions are:

- We unify the processing of Aggregation and Transformation stages using a single processor that is competent in handling the irregular data access patterns and the hybrid computing mode of GNNs.
- We apply the classic Strassen’s algorithm to accelerating dense matrix multiplication, significantly reducing the number of costly multiplications.
We exploit an ultra-efficient, greedy-based load-balancing approach that achieves considerable speedup in sparse-dense multiplication.

We propose VersaGNN, a high-throughput and memory-efficient Graph Neural Network accelerator based on the well-known systolic array design.

We implement our architecture design using Chisel HDL [3], and test our VersaGNN using four well-known GNN models on six benchmark graph datasets. Compared to the state-of-the-art software frameworks, our work achieves on average 3712× speedup with 1301.25× energy reduction on CPU, and 35.4× speedup with 17.66× energy reduction on GPU, respectively.

II. BACKGROUND

In this section, we review the core concepts of Graph Neural Networks. Table I lists the notations of GNNs used throughout the paper.

| Notation | Description |
|----------|-------------|
| E        | edges of G  |
| e_{i,j}  | edge between node i and j |
| Θ(·)     | Neural Networks |
| A, A_{i,i} | adjacency matrix, element at (i,j) |
| H_{0}    | initial state of feature matrix |
| n_{i}    | degree of node v |
| N_{i}    | neighbors of node v |
| h_{i}    | aggregated feature vector of v at layer i |
| W^{(i)}  | weight matrix of i-th layer |
| σ(·)     | activation function |

A. Graph Convolutions

Graph Neural Networks utilize the message passing mechanism [43], [49] for graph node embedding, usually generated by graph convolutions. A classic GNN is constructed with a stack of two or three graph convolution layers, whose structure is illustrated in Fig.1. A graph convolution layer takes the feature matrix as the input, arranged by graph node signals, and performs convolution on the feature matrix, followed by one or two optional nonlinear operators, such as nonlinear activation (e.g. ReLU, LeakyReLU) and pooling.

Convolutional GNNs can be categorized as spectral-based GNNs or spatial-based GNNs [43]. Spectral-based approaches such as [7], [22], [26] define graph convolutions by adopting filters from the perspective of graph signal processing [37]. The graph convolution operations are interpreted as removing noises from graph signals. Spatial-based approaches, including [1], [15], [31], exploits the information propagation paradigm and aims at collecting features of each node from its K-hop neighbors.

The convolution operator in a graph convolution layer consists of two consecutive phases, the Aggregation (or Message Passing) phase, and the Transformation (or Node Encoding) phase. Equation (1) gives a mathematical formulation of the message-passing network [11],

\[
\hat{h}^{(k)}_{i} = \Theta_{i}^{(k)} \left( \{ \hat{h}^{(k-1)}_{j}, \Xi_{j \in N(i)} \} \right)
\]

where \( \Xi \) embodies a differentiable and permutation-invariant aggregation function, e.g., Sum, Mean, or Max. \( \Theta_{i} \) and \( \Theta_{j} \) indicate neural networks or linear transformations.

B. Direct Aggregation

GraphSAGE [18] exploits vertex features such as text attributes and node degrees to learn an embedding function, formulated as:

\[
h'_{i} = \frac{\hat{h}_{i}}{\| \hat{h}_{i} \|_{2}}
\]

where the feature aggregation is the mean operator marked in Equation (2). Instead of training individual node-wise embedding vectors, GraphSAGE generates embeddings through uniform sampling and feature aggregation from the node’s neighbors, thus taking into account both the node’s own features as well as its neighboring features, and balance execution overhead with accuracy.

GIN [44] utilizes the Graph Isomorphism Operator to enhance the representation power of GNNs. For each graph node, GIN recursively aggregates and transforms representation vectors of its adjacent nodes. With its high expressive power, GIN is able to capture the structural information of both large and small graphs.

\[
h'_{i} = \Theta \left( (1 + \epsilon) \cdot h_{i} + \sum_{j \in N(i)} h_{j} \right)
\]

\( \epsilon \) is a learnable parameter that improves the node’s self-confidence, and \( \Theta \) represents a Multi-Layer Perceptron (MLP).

GIN uses summation as its aggregation operator, which can represent universal functions over multisets, as marked in Equation (3).

C. Weighted Aggregation

GCN [26] is composed of two or three convolutional layers with residual connections.

\[
H' = \hat{D}^{-1/2} \hat{A} \hat{D}^{-1/2} H \Theta
\]

\( \hat{A} = A + I \) denotes the adjacency matrix with self-loops, and \( \hat{D}_{i,i} = \sum \hat{A}_{i,j} \) represents its diagonal degree matrix. Expanding Equation (4), we get

\[
h^{(k)}_{i} = \Theta \left( \sum_{j \in N(i) \cup \{i\}} \frac{1}{\sqrt{\text{deg}(i)} \cdot \sqrt{\text{deg}(j)}} \cdot h^{(k-1)}_{j} \right)
\]
We observe from Equation (5) that the feature aggregation phase performs a weighted summation (aggregation) of neighbor features. The coefficients within the marked region are derived from the degree matrix and perform a degree-based normalization.

GAT [38] leverages masked self-attention layers in feature aggregation to assign computation importance to each node. It does not require costly matrix operations as well as pre-knowledge of graph structural information, and is able to achieve computation efficiency including intra-graph parallelization.

\[
\begin{align*}
    h_i' &= \alpha_{i, j} \Theta h_i + \sum_{j \in N(i)} \alpha_{i, j} \Theta h_j \\
    &= \Theta \left( \sum_{j \in N(i) \cup \{i\}} \alpha_{i,j} h_j \right) \quad (6)
\end{align*}
\]

The attention coefficient \( \alpha_{i,j} \) denoting the importance of node \( j \)'s features to node \( i \) is computed as

\[
\alpha_{i,j} = \text{SoftMax} \left( \text{LeakyReLU} \left( a^T [\Theta h_i \parallel \Theta h_j] \right) \right) \quad (7)
\]

Equation (6) uses attention coefficients for the weighted aggregation of neighbor node embeddings. The denominator marked in Equation (7) also has a form similar to aggregation, where SoftMax is a normalization performed after the node-level exponential operation \( e^{x p(\cdot)} \).

### III. Motivation

GNNs can be considered as an extension of classic deep neural networks with irregular topology that support graph-structured inputs and outputs. Specialized architecture designs for GNNs are required because existing machine learning accelerators are not suited to GNNs for the following reasons.

**Compounded Execution Mode** Most GNN models are shallow with approximately three layers. The weight matrices \( W \) are generally dense as the result of layer-wise node aggregation. Current sparse matrix accelerators are specialized solely in processing sparse data formats, but will suffer significant overhead with dense matrix operations. However, the execution flow of GNNs follows a hybrid mode. Despite the sparsity of the input node feature matrices, the following aggregation operations will gradually populate the intermediary node embeddings with non-zero values. On the other hand, node feature transformation involves dense matrix multiplications. Present GNN accelerators are designed either to undertake the sparsity in Aggregation, or to employ the regularity in dense matrix multiplications that constitute Transformation, but lack the generality to handle both cases.

**Workload Imbalance** The irregular access and computation patterns of the Aggregation phase, which involves graph traversals that require tremendous memory access relative to only small amounts of calculation, make the mainstream computation platforms unsuitable for GNNs. CPUs and GPUs are not capable of irregular data movements and computations that constitute GNN operations. Their inefficiency in memory access causes the waste of off-chip memory bandwidths. Although modern GPUs such as NVIDIA A100 support sparse matrix multiplication with pruning techniques; for many real-world graph datasets, their feature matrices cannot be pruned, as the features are represented using binary values. Meanwhile, the adjacency matrices are subject to significant loss of graph structural information, making compression unrealistic despite their sparsity.

For traditional computation platforms including GPUs, their performance bottleneck on GNNs originates from their inability to settle the irregularity in Aggregation phase. Their relatively high performance on GNNs is mostly attributed to the high-bandwidth memory, which incurs considerable energy consumption. Furthermore, although they leverage the regularity in Transformation phase, the data copying and synchronization between threads for parameter reusing are expensive. Meanwhile, graph analytics accelerators are only optimized to alleviate irregularity or exploit regularity.

**Usecase Generality** Aggregation can be direct aggregation or weighted aggregation. The weighted one is not just performing summation or other aggregation operation. Neighbor node’s feature vector is scaled with a factor before applying the aggregation operator, e.g., Equation 6 of GAT. Current GNN accelerators such as EnGN [30] and HyGCN [45] are only optimized for the directed aggregation case. This scaling issue can be solved by sparse-dense matrix multiplication and is more efficient than other designs.

HyGCN [45] is a GNN accelerator with a hybrid architecture. To harness the hybrid execution patterns of GNNs, HyGCN separates the modules for the regular neural network processing and irregular graph processing. The Aggregation Engine and Combination Engine, used for node aggregation and transformation respectively, each require separate on-chip buffers which consume considerable chip area. Despite their potentials for pipelining, the distinct computing patterns of these two processing stages make it difficult to harness both modules for efficient processing of general GNN structures.

EnGN [30] adopts the Ring-Edge-Reduce (RER) dataflow to tame the poor locality of sparsely connected vertices, and manipulates the ring-edge-reduce (RER) PE-array to practice RER dataflow. However, RER’s storage of neighbor node indices consumes enormous local registers. Moreover, the index comparisons incurred by RER data movements may induce considerable latency and soaring computation cycles.

Fig. 2: Unify transformation and aggregation phases

The characteristics of Aggregation phase reveals that it can adopt sparse matrix multiplication, then it provides an option to unify the Transformation phase and Aggregation phase into one single arithmetic operation, i.e., matrix multiplication,
but aggregation phase tends to be sparse-dense case. Fig.2 demonstrates the possibility of unification.

**Our Solution** Therefore, we propose to accelerate the two phases with one versatile accelerator. We propose a unified hardware design that can reuse the limited on-chip buffers among the different processing stages. We can turn the aggregation stage into pseudo sparse matrix multiplication. Our design is scalable and efficient parallel processing engine and support large-scale GNNs.

### IV. Microarchitecture

In this section, we discuss the hardware design of VersaGNN, with its system-level overview outlined in Fig.3. VersaGNN consists of a general-purpose processor, a memory management interface, a multi-purpose bus, and an accelerator. The processor is used to control the whole system, send instructions to both the accelerator and the memory system, and collect the status of the accelerator. The accelerator comprises an instruction queue, a DMA engine, a scratchpad memory with several banks, and the systolic array tiles which are interconnected side-by-side in a chain/ring fashion. An additional Block Address Mapping module is equipped for address matching when tiling is applied, and a Result Reordering module is used for the write-back phase of sparse-dense matrix multiplications (SpMM). Since the bulk of GNN calculations are matrix computations, our accelerator targets the acceleration of both dense and sparse matrix addition and multiplication.

#### A. Systolic Style Matrix Multiplier

The Transformation phase of the Graph Neural Network, formed by Multi-Layer Perceptrons (MLP), is essentially a multiplication of node feature matrix with layer weight matrix [43], [49] that maps the high dimensional node features to lower dimensional spaces. The input feature vector of a graph node is usually very sparse [43], implying that a node does not hold all its defined features, with absent features holding zero values. The intermediary node embeddings are gradually populated with non-zero values as feature aggregation proceeds, whereas most weight matrices for these layers are dense. To fuse matrix operations among these disparate structures, GNN requires a versatile accelerator architecture to tackle both dense and sparse matrix calculations.

1) **Revisiting Strassen’s Algorithm:** Before diving into systolic array tile design, we revisit Strassen’s algorithm [42], and expand it to block-based dense matrix multiplications to reduce the volume of expensive arithmetic multiplications. Given two matrices (or matrix tiles) \(A\) and \(B\) as input, we partition each of them into 4 sub-blocks: \(A_{0}, \ldots, A_{3}\) for \(A\), and \(B_{0}, \ldots, B_{3}\) for \(B\). Similarly, the result matrix \(C\) can be divided into \(C_{0}, \ldots, C_{3}\).

We rearrange the equations of Strassen’s algorithm into 6 groups, as shown in Equation (8). Equations inside each group are performed in parallel, and the right-hand side of some equations in identical groups also share their operands, e.g., \(A_{0}, B_{0}\) in the right-hand side of the upper-left equation. To harness this element-wise parallelism, the three groups in the left column can be executed in pipeline mode, the same for the three groups in the right column. For example, after calculating \(M_{5}\), we can directly apply it to computing \(C_{2}\), and simultaneously forward \(M_{3}\) to the next group and calculate \(C_{0}\) without saving or fetching the intermediate result.

With the above analysis, we group the tiles of the systolic array into clusters (or meshes). Fig.4(a) illustrates the layout of a systolic array cluster. Unlike the mesh architecture of Gemmini [13], data across rows and columns are also shared in diagonal directions. The shared buffers act as interfaces to the scratchpad memory. Our systolic method minimizes the I/O cost by allowing each row or column of matrix operands to enter the processing element array only once for all its associated matrix computations [27]. Since matrix additions are element-wise operations, addition along rows and columns are independent. Further, the matrix additions can overlap with matrix multiplications as the pipeline proceeds. In our case, every systolic array receives the result of row or column addition from a pair of 1-D adder arrays. Each 1-D adder array is either a column or a row of adders located at one side of a systolic array, as shown in Fig.4 (a). The systolic arrays can forward the data through interconnections between neighboring systolic arrays within the ring structure.

Fig.4 (b-d) demonstrates the execution of the right three groups in Equation (8). The left three groups can be performed similarly and pipelined with the right three groups. Within each cycle, every 1-D adder array imports data from shared buffers to produce a row or column, and feed them to systolic array for matrix multiplication. 1-D adder arrays and systolic arrays orchestrate in a pipeline mode. Once the marginal PEs of systolic array receives the resultant row and column, they...
Algorithm 1: One cycle in each PE of the systolic array for hybrid mode matrix multiplication.

Input:
- \( a_{col} \): column index of \( A[\text{row}, \text{col}] \) if sparse;
- \( a_{val} \): input value of dense or sparse matrix;
- \( b_{row} \): row index counter of dense \( B[\text{row}, \text{col}] \);
- \( b_{val} \): input value of dense \( B[\text{row}, \text{col}] \);
- \( \text{a\_sparse, a\_dense} \): \( A \) is sparse or not;
- \( \text{direct\_aggr} \): direct or weighted aggregation;
- \( \text{FA} \): circular FIFO_CAM (increasing order)

\begin{itemize}
  \item \( \text{found} \leftarrow \text{false} \)
  \item if \( \text{a\_dense} \) or (\( \text{a\_sparse} \) and \( a_{col} = b_{row} \)) then
    \begin{itemize}
      \item \( a_{buf} \leftarrow a_{val}; b_{buf} \leftarrow b_{val}; \text{found} \leftarrow \text{true} \)
      \item if \( \text{a\_sparse} \) then
        \begin{itemize}
          \item \( \text{purge}(\text{FA}) \)
        \end{itemize}
    \end{itemize}
  \item else if \( a_{col} > b_{row} \) then
    \begin{itemize}
      \item \( \text{Find&Skip}(\text{FA}, b_{row}) \)
      \item \( b_{buf} \leftarrow b_{val}; \text{push}(\text{FA}, a_{col}, a_{val}) \)
    \end{itemize}
  \item if \( \text{found} \) then
    \begin{itemize}
      \item if \( \text{direct\_aggr} \) then
        \begin{itemize}
          \item /* reduction operation can be add, min, max, or mean */
          \item \( c_{val} \leftarrow \text{ reduction\_operation}(c_{val}, b_{buf}) \)
        \end{itemize}
      \item else
        \begin{itemize}
          \item if \( \text{a\_sparse} \) then
            \begin{itemize}
              \item \( (c_{\text{b\_idx}}, c_{\text{a\_idx}}) \leftarrow (a_{\text{row}}, b_{\text{col}}) \) /* indices used for write-out phase when sparse */
              \item \( b_{row} \leftarrow b_{row} + 1; \text{found} \leftarrow \text{false} \)
            \end{itemize}
          \item else
            \begin{itemize}
              \item \( c_{val} \leftarrow c_{val} \)
            \end{itemize}
        \end{itemize}
        \begin{itemize}
          \item \( a_{out} \leftarrow (a_{val}, a_{col}); b_{out} \leftarrow b_{val} \)
        \end{itemize}
    \end{itemize}
\end{itemize}

Fig. 4: Scenario of Strassen’s Algorithm: dataflow and processing

Algorithm 2: Find&Skip

Input:
- \( \text{FI} \): circular FIFO_CAM of nonzero indices;
- \( \text{FV} \): circular FIFO of nonzero values;
- \( \text{idx} \): an index value to be found;
- \( \text{mask} : [\cdot] \): indicates existence of \( \text{idx} \);

Output:
- \( \text{val} \): the value of nonzero found;
- \( \text{found} \): found

\begin{itemize}
  \item \( \text{mask} [\cdot] \leftarrow 1 \)
  \item \textbf{forall} \( i < \text{FI}.\text{size} \) \textbf{do}
    \begin{itemize}
      \item if \( \text{FI}[i].\text{idx} < \text{idx} \) or \( i < \text{FI}.\text{head} \) then
        \begin{itemize}
          \item \text{mask}[i] \leftarrow 0
          \item /* use the leading zero detector to find the position of first bit-one. And set the new head of FIFO */
        \end{itemize}
      \item \( \text{FI}.\text{head} \leftarrow \text{LeadingZeros(mask)} \)
      \item \( \text{val} \leftarrow \text{FV} [\text{FI}.\text{head}] \)
    \end{itemize}
  \item \( \text{found} \leftarrow \text{equal} (\text{idx}, \text{FI}.\text{head}) \)
\end{itemize}

Fig. 5: A simulated cycle-level illustration of the execution in a systolic tile of the Strassen’s Algorithm. All 4 systolic tiles execute in parallel

perform the MAC (Multiply-Accumulate) and forward the inputs to their neighboring PEs to perform MAC of \( M_i \), as shown in Fig.4 (b). The MAC starts execution one cycle after the adder array as the row of Fig.5. As the results of matrix multiplication \( M_i \) are stored in the local register of PEs (in output stationary mode), we want to reuse them for the following matrix additions, then they are transferred to the neighboring systolic array in the ring, as shown in Fig.4 (c). As the two \( C_i = C_i + M_j \) operations in Fig.4 (b) and (c) are independent, they can be pipelined along with data forwarding of \( M_i \), but the one in stage 3 need to transmit \( M_i \) to be align with those at the same coordinates in the systolic
arrays prior to performing addition. All PEs perform addition simultaneously during the last cycle, as shown in the 4th row of Fig.5.

With this hardware-level implementation of Strassen’s algorithm, we decrease the volume of multiplication and data transfer of operands from memory by profiting the internal bandwidth among PEs, as well as reading and writing of intermediate results from and to the scratchpad memory. Strassen’s algorithm takes an asymptotic complexity of $O(N^{2.8074})$ when applied in recursive manner, compared with $O(N^3)$ of standard matrix multiplication. As shown in Fig.4 (b), the four tiles of systolic array execute in parallel and form a cluster, with skid buffers serving as bridges for inter-tile communication and the interface to local memory. Compared with the case in which four tiles are consolidated into one large systolic array, our design adopts a data source at the geometric center of the tile cluster, which effectively halved the data transmission path. Meanwhile, The hardware approach in VersaGNN is in 1-level Strassen’s, and the software support of 2-level Strassen’s can be combined with this design for further performance gain. [23]

2) Hybrid Mode Processing Elements: Fig.7(b) shows the internal structure of the processing element. To enable high-throughput operations on both dense and sparse matrix data structures, we devise an efficient hybrid mode processing element (PE) of the systolic array, it equips with dedicated searchable FIFOs, with which we call it FIFO_CAM. The FIFO_CAM can search a target element within its elements and skip unused elements as depicted in Algorithm 2 and Fig.7 (c). Instead of using a shared storage structure, we leverage distributed FIFO_CAMs design. Our design accepts the COO (Coordinate list) and CSR/CSC (Compressed Sparse Row/Column) formats [41]. The row is interpreted as a graph node and the column indices in such row are the node’s neighbors. As the column indices moving in and out of the FIFO_CAM, it only needs to keep a relatively small sliding window for the indices under processing. Thus, it is not necessary to store a whole list of neighbors for a graph node in the FIFO_CAM of a PE. Empirical result shows that 4 entries of FIFO_CAM is big enough to accommodate ongoing data.

As described in previous section, Transformation phase of intermediate layers of GNNs is simply a dense-dense matrix multiplication. In Algorithm 1, the PE conduct directly the MAC operation for the dense matrix multiplication, the dataflow is shown as the light green and red curve lines in Fig.8 (a), the FIFOs for operating sparse data are bypassed and concealed.

Recall the general mathematical expression of the convolution layer of GNN:

$$X' = XW; \quad X'' = AX'$$  \hspace{1cm} (9)

In order to reuse $X'$, the result of dense matrix multiplication of Transformation phase, and to avoid transferring $X'$ back to scratchpad memory, we introduce an additional dataflow path from bottom to top in PE and stored locally into register $d$ of PE, as shown in Fig.6 (b). At the initial cycle of Aggregation, the PE selects the value of $c$ register by setting signal $prop\_c$ to 1 and passes it down to the south neighbor PE. After this cycle, each PE sets $prop\_c$ back to 0 and transfer value of $c$ register as $b$ of dense matrix. At bottom row of systolic array, PEs feed back the $c$ to $d$ register of PEs, the matrix $X'$ turns back from bottom to top inside the systolic array, as shown in Fig.7 (b) and (c). This manner avoids the long distance data transfer leaping across all rows used in the ring structure of RER in EnGN [30] which leads to imbalance of data transfer rate between rows of processing array.

For the weighed aggregations, we treat them as SpMM ($AX'$). Instead of using $b$ register of PE, now the dataflow uses $d$ register of PE, which flows into PE in opposite direction, as dense matrix element for MAC operation. The sparse data (from matrix $A$) are fed into PEs, in horizontal direction, from west to east. As described in Algorithm 1 and shown in Fig.6(b), PE possesses a counter, $b_{row}$, for the row number of dense matrix, it augments itself at each cycle. When condition $a_{col} = b_{row}$ satisfies, the PE performs the MAC directly as the dense-dense case. However, if condition $a_{col} > b_{row}$ meets, the PE checks whether FIFO_CAM of A contains indices smaller than or equal to $b_{row}$, if there exists $a_{col} = b_{row}$, it fetches the corresponding nonzero value $a_{col}$ from FIFO of nonzero, performs the MAC operation, and puts $a_{col}$ and the corresponding nonzero into FIFO_CAM and FIFO, respectively. All $a_{col} < b_{row}$ and their corresponding nonzeros are expelled from FIFO’s for sparse $A$. Note that indices are enqueued into the FIFO_CAMs in increasing order, thus are already in sorted order in FIFO_CAMs. Algorithm 2 describes the logic that performs searching and skipping mechanism, and we can integrate FIFO with such logic into our FIFO_CAM, as shown in Fig.7(c). The detection in FIFO_CAM is performed in parallel with all elements as Fig.7(c). With the help of these FIFO_CAMs, the PE can produce one result per cycle without any inter-cycle stalls.

Fig.8 delivers a concrete example. Suppose that in Fig.8(a), $S$ and $D$ are a sparse matrix and a dense matrix, respectively. The dataflow traversing $PE_{(0,0)}$ are the first row of $S$ in compressed format and first column of $D$ that enter the PE from left and above in Fig.8(b), respectively. Fig.8(c) demonstrates the cycle-by-cycle execution. In the first two cycles, the comparison operator does not find the matching index of current element. Thus, the FIFO_CAM stores them, and the MAC bypasses the data of dense matrix to neighboring PEs. At Cycle2, the FIFO_CAM performs parallel comparisons of row indices of $S$ it stored with the incoming column index of $D$, and fetch the nonzero value of matched entry. Since the FIFO_CAM and MAC are fully pipelined, at Cycle3, MAC performs the multiplication and accumulation on the data fetched from previous cycle, and FIFO_CAM performs the comparison of new incoming index in parallel. The MAC utilization rate relates to the number of matched indices. This issue can be solved with the algorithm introduced in Section V-B.

The direct Aggregation can be seen as a special case of
weighted Aggregation, where every nonzero is value one. Therefore, it is useless to perform multiplication with value one. As the light-red dataflow shown in Fig.7 (c), when indices \( a_{col} \) and \( b_{row} \) matches each other or its found a column index in FIFO_CAM equal to \( b_{row} \), PE directly performs the addition of \( c \) and \( d \) register of PE without touching multiplier.

V. SOFTWARE APPROACH

A. Tile Traversal strategy

The vast majority of real-world graphs that GNNs operate on cannot be fitted to the limited on-chip memory of accelerators. Thus, the algorithms often divide these large-scale graphs into tiles using grid partition approaches before applying arithmetic operations, and then merge individual tiles into the full result layout.

There exist several tiling traversal strategies, including row/column-major, Z-Morton, U-Morton, and Hilbert layouts.
that can be harnessed by GNN accelerators. However, the shape of feature matrix $X$ and weight matrix are constantly changing through different layers. The feature matrix tends to become narrower and taller as the layers going deeper, whereas the weight matrix becomes smaller in size. As modern deep learning libraries support batched matrix multiplication with which the feature matrix can be seen as batched independent smaller matrices. In such way, small matrices are streamed into accelerator consecutively. In this work, we utilize two tile mapping strategies. For Transformation phase, we directly map the 4 tiles in a bigger square onto the ring of systolic arrays from both input and weight matrices, as shown in Fig.9 (c). In this way, the four systolic arrays in a ring perform the dense Strassen’s algorithm as described in Section8. While, for the SpMM of Aggregation phase, we adopt an alternative strategy. After tiling, only tiles with nonzeros will take into account, those empty tiles are eliminated directly; the non-consecutive nonzero tiles in the same column are mapped onto the four systolic arrays, which is now in a chain, the dense tile from input matrix $X$ is then traversing the four tiles. with such manner, the systolic arrays perform the batched SpMM, as shown in Fig.9 (b).

Fig. 10: The greedy algorithm used for workload balancing: Given two tiles in CSR (or COO) format, each row represents one graph node, and the number in each row represent the column indices $col$ (or neighboring nodes) belonging to that row (or node).

B. Greedy Workload Balancing

As the sparse matrix elements are irregularly distributed, some graph nodes may have relatively more neighbors. For sparse matrices in compressed formats, e.g., CSR or COO, each row of systolic array PEs processes features of a single node and aggregates its neighbor nodes’ information. PEs in different rows will be assigned different workloads. The imbalanced workload can cause significant idling of PEs, with modules having less assigned workload finishing earlier and kept idle while waiting for those with heavier workload before the advent of next data stream, which will lead to degradation of the overall system-level performance. To remedy these issues, we introduce an effective greedy algorithm for workload balancing, which is an offline software scheme that groups tiles of sparse matrices into condensed ones. Our algorithm first sets a sparsity threshold $\alpha\%$, e.g. $40\% < \alpha \leq 50\%$. Assume the sparse adjacency matrix is split into tiles, and each tile is stored in CSR or COO format. For each tile with sparsity greater than $\alpha\%$, the algorithm searches for a complementary tile with sparsity less than $\alpha\%$ to combine with, as shown in Fig.10. Note that the number in each cell represents the column index of sparse matrix but not the value of non-zeros. Rows of the two tiles are sorted in reverse order according to their number of elements and then combined (or packed) into one single tile. As shown in Fig.10, the column indices are arranged in increasing order. Duplicated elements are eliminated in each row, which prevents overlapping summation of feature vectors that belong to the same neighboring node when multiple vertices share a common set of neighbors. Our approach exploits an element mask as an identifier to trace the affiliation relationship between cells and their corresponding tiles. For combination of two tiles, each entry will have a single bit. Meanwhile, we adopt two 1-D arrays, i.e. two reorder vectors, to record the original row ordering of tile elements. When this combined tile is fed into the systolic array, almost every PE is utilized to its full capacity during each cycle. The mask and reorder vectors are utilized by the Reordering Module in the accelerator to direct the final results back to the scratchpad memory. Each entry of the combined tile, in form of $((row, col), val)$, is fetched with:

$$\begin{align*}
row & \leftarrow row\_reordering[i, masks[i, j]] \\
col & \leftarrow b_{col} \\
val & \leftarrow values[i, j]
\end{align*}$$

The execution of Reordering Module can be coordinated with that systolic arrays whenever the output is ready, causing execution overhead that is generally negligible. Further, to facilitate packed sparse tiles, both CSR and COO formats are treated internally as COO within systolic arrays. This approach is extensible to combine 3 or more tiles.

VI. EVALUATION

In this section, we begin with the experimental datasets and hardware configurations. Then, we deliver the detailed analysis of our optimizations.

A. Experiment Configurations

Methodology We implemented our accelerator, VersaGNN, along with the baselines using Chisel3 Hardware Design Language (HDL) [3] Our design is also inspired by Gemmini [13] and HardFloat [36]. The systolic array adopts the output-stationary fashion with 16-bit floating point input and 32-bit floating point output. We evaluated the performance of the entire system and individual modules of VersaGNN with FireSim [24], a highly efficient, open-source simulator that simulates ASIC RTL designs with timing-accurate system components, which is of several magnitudes faster than software-based RTL simulation. We used FireSim to facilitate the full-system simulation by enabling integration of the simulated SoC with accurate peripheral and system-level interface models such as DDR3 memory or High Bandwidth Memory (HBM) and a last-level-cache (LLC). We synthesized VersaGNN using open-source Yosys and the TSMC 16nm process technology. Power and area are evaluated using a Cadence VLSI flow with TSMC 16 nm FinFET technology libraries. The placement and routing of the physical design were performed using Innovus,
and power estimation using Voltus. The accelerators aim at achieving frequency of 1 GHz. To afford the high-throughput request volume, we equip the accelerator with HBM 2.0 interface with 256GB/s bandwidth, and a 256 KiB L2 Cache and a 4MiB last level cache (LLC). The energy of HBM 2.0 is estimated with 3.9 pJ/bit as in [32]. The configuration of VersaGNN and the baselines are described in Table II.

**Baselines** We choose three distinct types of baseline architectures for performance and energy efficiency comparison, including the general-purpose processors (GPP), i.e. CPU and GPU, and two state-of-the-art GNN accelerators including HyGCN and EnGN. We selected the server processor, an Intel Xeon (Skylake) 6151@3.0GHz processor with 512GiB DRAM, as the CPU platform. The GPU platform is equipped with NVIDIA Tesla V100 and 32GiB HBM2. The software environment for the two platforms is PyTorch [34] and PyTorch Geometric (PyG) [11]. PyG is the state-of-the-art library for geometric deep learning that provides the majority of mainstream GNN models. We denote CPU and GPU platforms running PyG as PyG-CPU and PyG-GPU, respectively. The configuration of HyGCN and EnGN are listed in Table II.

**Benchmark Graph Datasets** Table III shows the statistics of benchmark graph datasets. The Feature column specifies the length of initial feature vector ($H_0$ from Table I). The Class column marks the number of labels. The graphs in all listed datasets do not contain edge attributes. The sparsity of adjacency matrix is determined by the ratio of the number of graph edges to the square of the number of graph nodes. As we have stated in previous section, the Aggregation phase, i.e. $A \times X'$, is essentially SpMM, so we focus on how the sparsity affects the efficiency of the accelerator in executing SpMM. Lengths of node feature vectors determine tiling sizes and strategies of the dense matrix multiplication in the Transformation phase.

**GNN models** We benchmark the performance of VersaGNN using 4 GNN models, including GCN [26], GraphSAGE (GSA) [18], GIN [44], and GAT [38]. The first three models are mainly used for semi-supervised classification, while GAT can also be applied to inductive tasks, such as graph edge prediction and node feature prediction. To make the GAT profiting the sparse matrix multiplication and addition, we reformulate the calculation of the attention coefficients of Equation 6 and 7. Equation 6 can be expressed in matrix form, 

$$H' = AHW$$

(11)

where $A$ is the adjacency matrix and $A[i,j]$ corresponds to $\alpha_{i,j}$ of Equation 6. Suppose trainable vector $a$ of Equation 7 can be split into two sections:

$$a^T[h_i][h_j] = (a_1||a_2)^T[h_i][h_j] = a_1^T \cdot h_i + a_2^T \cdot h_j$$

(12)

where $h_i' = \Theta h_i$ and $h_j' = \Theta h_j$. Turning it into matrix form, we get $H'_1 = H \cdot a_1$, $H'_2 = H \cdot a_2$. And the calculation of attention coefficient matrix $A$ becomes:

$$A = \text{Softmax} \left( \sigma \left( \text{Diag}(H'_1) \cdot A + A \cdot \text{Diag}(H'_2) \right) \right)$$

(13)

where $A$ is the adjacency matrix and $\sigma$ is the activation function LeakyReLU. We then implement our customized code and replace the one in PyG. Most parts of Equation 11, and 13 can be executed by SpMM, thus GAT can also benefit from our highly efficient SpMM engine.

**Evaluation Metrics** We conduct our experiment with several metrics. We estimate 1) performance through the end-to-end inference time of GNN models; 2) throughput by billion operations per second (GOPS); and 3) energy-efficiency by billion operations per second per Watt (GOPS/W).

**B. Results of experiment**

**Power & Area** We summarize the power and area of HyGCN, EnGN, and VersaGNN in Table II. As reported by the CAD tool, the 4 banked 512 KiB scratchpad memory and 128 KiB L2 Cache are the biggest part in our place-and-route design. In the floor plan we organize the SRAMs of the accelerator in a semi-ring around the computational tiles. The second contributor of the area is the wires of the interconnections between tiles of systolic array. Due to the limit of process technology at 16nm, the power of VersaGNN is higher than EnGN but still achieves a higher energy efficiency than both EnGN and HyGCN. Static timing analysis at net-list level shows that there is still some positive slack, signifying potential for further frequency increases of our design. Fig.13 provides the breakdown of the energy consumed by arithmetic operations, memory accesses, and interconnect between tiles for the model of GCN and GAT. As the figures illustrates that the sparser dataset tends to be compute-bound and denser dataset tends to be memory-bound. It is crucial to improve the cache utilization for the denser dataset while sparser graph’s neighbors having larger stride crossing several tiles cause cache to evict more frequently.

**TABLE II: Configurations of system**

|                  | PyG-CPU | PyG-GPU | HyGCN | EnGN | VersaGNN |
|------------------|---------|---------|-------|------|----------|
| Compute Unit     | 3.0GHz  | 1.25GHz | 1GHz  | 1GHz | 1GHz     |
| On-Chip Memory   | 65 cores| 5120 cores| 32 SIMD 16 cores| 32 PE units in VPU| 32x32 arrays|
| Peak Performance (GOPS) | - | - | 8704 | 6144 | 8192 |
| Area ($\text{mm}^2$) | - | - | 7.8 (12nm) | 4.54 (14nm) | 4.78 (16nm) |
| Power (W)        | 150     | 120     | 6.7   | 2.56 | 3.58     |
| Energy Efficiency (GOPS/W) | - | - | 1.30 | 2.4 | 1.71     |
| Area Efficiency (GOPS/mm²) | - | - | 1.16 | 1.35 | 1.65     |

**TABLE III: Dataset Statistics**

| Dataset | Nodes | Edges | Features | Classes | Storage | Sparsity | Ave. Degree |
|---------|-------|-------|----------|---------|---------|-----------|-------------|
| Cora (A) | 2,708 | 10,930 | 1,435 | 7,568 | 1.24E-01 |
| Citeseer (C) | 3,327 | 4,683 | 3,703 | 7,568 | 8.22E-04 |
| Pubmed (P) | 19,717 | 41,581 | 500 | 38,528 | 2.28E-04 |
| IMDB-BIN (B) | 2,467 | 28,624 | 336 | 5,556 | 4.09E-03 |
| Reddit (R) | 23,286 | 114,615,892 | 602 | 41,972,56 | 2.11E-03 |
| Amazon (M) | 5,688 | 231,884 | 86 | 22,36,MiB | 3.13E-06 |
| COLLAB (CL) | 12,887 | 1,446,010 | 492 | 3 | 28,5 | 9.90E-03 |
Performance The performance of VersaGNN is compared with baseline platforms including PyG-CPU and PyG-GPU, HyGCN, and EnGN. The original implementation of PyG adopts the Pytorch Scatter Library [9] for the Aggregation phase. Our experimental results show that the average performance speedup of all models on all datasets compared with PyG-CPU is $3712 \times$, as shown in Fig.11. For the case of GPU, we rewrite the Aggregation function as SpMM by using PyTorch Sparse library [10] and solved the memory leakage problem for the version that we used in this experiment. As the writing of this work, PyG has announced the re-implementation of the Aggregation phase as SpMM in its future release. We obtained an average $35.4 \times$ speedup compared to PyG-GPU over all models on all datasets, as shown in Fig.11. Compared to HyGCN and EnGN, VersaGNN achieves higher performance speedup on both small and big datasets, especially for the model with weighted Aggregation since prior to perform the summation the neighbor node’s feature vector, it needs to scale up with the coefficient, e.g., the fraction of degree term in GCN, and the attention coefficient in GAT. Finally, VersaGNN is $6.32 \times$ faster than HyGCN and $2.73 \times$ faster than EnGN.

Throughput Through our experiments, we observe that datasets with higher densities of graph connections (the number of edges) or longer node feature vector tend to yield higher throughput. This is because longer feature vectors are well-suited to dense-dense matrix multiplication due to their superior memory coalescing mechanisms, whereas their high graph connectivity facilitates the memory access pattern since connected nodes are more likely to share neighbors, which

C. Analysis of Optimization of VersaGNN

In this section, we evaluate the performance improvement of each optimization for Transformation and Aggregation, respectively.

Strassen’s Algorithm This optimization is applied only to the Transformation phase which consists primarily of dense-dense matrix multiplication. The normalized execution time and the bandwidth utilization in Fig.14 show that VersaGNN achieves $1.7 \sim 3.1 \times$ speedup when Strassen’s algorithm is applied at hardware level. The performance gain is due to the parallelism from simultaneous matrix multiplications by 4 tiles of systolic array instead of one large tile, and the data transmission traversing the boundaries of neighboring tiles is achieved by utilizing the internal bandwidth of systolic arrays, which facilitates data reuse and reduces the data write-backs. This demonstrates that through collaboration, smaller spatial accelerators are able to achieve superior results than a single large module.

Greedy Workload Balancing The greedy algorithm introduced in Section V-B can be utilized by both direct and weighted Aggregation phases. The efficiency of this greedy approach is also affected by the sparsity of datasets, with sparser
graphs bearing more tiles to be coalesced. Graphs with higher average degree tend to produce denser tiles, and better sparse tile packing strategy delivers more parallelism and utilizes less operation cycles to improve the utilization of PEs. To further evaluate the improvement in SpMM of Aggregation phase, we use the SCNN, specialized for sparse model, as baseline. Experiments show that SCNN is less efficient for GNN, since Cartesian Product-based SpMM consumes most of time in processing massive irregular reduction of intermediate results, and the out-of-order scattering operation causes stall when multiple intermediate results are written into same memory location; while VersaGNN’s greedy algorithm feed the operands according to the increasing order of indices in pipeline, which guarantees free of stalling, as shown in Fig.15. This greedy algorithm is also affected by the tiling strategy described in Section V-A, since the sparsity varies according to the tile size and the distribution of node neighbors. Generally, the greedy workload balancing algorithm afford great improvement in performance of speed and energy saving. Since it is a static data pre-processing method prior to the execution of model, greedy workload balancing improves the utilization of PEs and packs the sparse tiles to increase more useful workload, as shown in Fig.16. Our greedy algorithm is more flexible than the tile packing algorithm used in EnGN, which requires two tiles with fully compatible empty slots. Moreover, HyGCN’s window sliding strategy cannot remove zero-entries inside the tiles.

VII. RELATED WORK

There have been ongoing researches on tackling the hybrid computing pattern of Graph Neural Networks [2], [8], [14], [45], [47]. GraphACT [47] devises an algorithm to exploit redundant operations by looking for neighbor pairs. HyGCN [45] and EnGN [30] design high-performance ASIC accelerators with two individual computing components for Aggregation and Transformation phases, respectively. GraphZoom [8] proposes an efficient clustering algorithm to condense the graph, reducing considerable inference latency.

Deep Learning Acceleration on Sparse Structures The latest machine learning models, especially those for embedded and mobile systems [6], reduce their weight volumes by driving smaller weight parameters towards zeros in the feature maps and filters, leading to highly sparse models. Several works have been proposed for accelerating SparseNN and sparse matrix computing [19]–[21], [28], [35]. [28] describes a novel approach of packing sparse networks into denser formats for efficient implementation using systolic arrays. [6] proposes Eyeriss v2 for execution of both compact and sparse DNNs. Architectures such as [33] and [16] are committed to the sparse model design. Although the Cartesian-product in [33] avoids the index matching in producing products, the calculation of destination addresses corresponding to indices of products are still required while doing the partial sums, which can be seen as a postponed index matching. SparTen [16] provides an effective inner join mechanism, but their vector-vector multiplier cannot share broadcast inputs internally as the highly-efficient systolic array. The bandwidth is wasteful, and the broadcasting demands an intricate protocol for data synchronization.

Graph Analytics Systems solve graph-related problems from different dimensions. Generally, they optimize conventional graph algorithms using a deterministic approach. Node in these graph structures typically do not possess high-dimension attributes. Therefore, the software and hardware solutions targeting these types of graphs [4], [17] are ineffective for GNN models.

VIII. CONCLUSION

The hybrid computation mode of Graph Neural Networks impose huge obstacles in acceleration of GNN architectures. In this paper, we tackled GNN acceleration by first generalizing its computation pattern into two stages, Aggregation and Transformation. Aggregation phase is essentially formed by sparse matrix multiplication, whereas the Transformation phase is dominated by dense matrix calculation. Then, we propose VersaGNN, a high-throughput and memory-efficient GNN accelerator based on the systolic array paradigm. To offer the flexibility towards both dense and sparse matrix multiplication, we re-factor the processing element of systolic arrays. We further design the architecture of multiple tiles that form a computing cluster, which supports efficient execution of Strassen’s algorithm. This hardware-level Strassen’s algorithm dramatically reduces the computation and memory access. At the same time, We also designed a greedy workload balancing algorithm from software perspective to improve the efficiency...
of sparse matrix multiplication. Our vast experiments have demonstrated that, under the state-of-the-art GNN software frameworks, VersaGNN achieves on average 3712× performance gain with 1301.25× energy reduction on CPU, and 35.4× speedup with 17.66× energy reduction on GPU.

IX. ACKNOWLEDGEMENTS

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