Evaluation of three optical-encoder-based speed estimation methods for motion control.

Yeny Vazquez-Gutierrez¹, Dara L. O’Sullivan², Richard C. Kavanagh¹

¹School of Engineering, University College Cork, Ireland
²Analog Devices Inc, Cork, Ireland

E-mail: yeny.vazquez.gutierrez@umail.ucc.ie

Abstract: Three speed estimation methodologies: pulse count, elapsed time, and constant sample-time digital tachometer (CSDT) methods, used with optical incremental encoders, are implemented and compared in a closed-loop system setup using a specialised Analog Devices CM403f DSP. Dedicated hardware for quadrature encoders on the DSP facilitates the implementation of advanced speed estimation methods, such as the CSDT, by minimising the delay resulting from software intervention. The error of each methodology is evaluated theoretically and experimentally. The CSDT has limited error over all its speed range. The error of the elapsed time method increases as the speed increases. On the contrary, the relative error of the pulse count method (which is often substantial) decreases with increased speed. Several filtering techniques can be used to reduce the error of the elapsed time method; here an oversampling technique is implemented with that aim.

1 Introduction

Quadrature optical encoders are frequently used in motion control for servo-systems, industrial automation, and robotics. Speed and position can be estimated by counting the number of encoder pulses during a given time interval (sampling interval, $T_s$). Inaccurate or delayed estimation of the speed impacts on the stability and performance of the system, potentially reducing quality and throughput in automation/robotic applications and increasing acoustic noise and vibrations [1].

The optical incremental encoder sensor is a disc with $R$ nominally evenly spaced slits, which transmits the light of a photodiode located at one side of the disc and on the other side a photo detector provides a voltage proportional to the amount of light sensed from the disc. The wave shape of that voltage is approximately sinusoidal, but is squared by a Schmitt trigger.

The resolution of the encoder is determined as (1) in degrees and represented as:

$$\theta = \frac{360°}{L \cdot R}$$

where $R$ is the encoder resolution in pulse per revolution (ppr) and $L$ is a resolution increasing factor that can be 1, 2, and 4 which depends on the encoder peripheral configuration. The optical incremental encodes has two channels (Channel A and Channel B) with one shifted by approximately 90°, as shown in Fig. 1. $L = 1$ if only the rising edges or falling edges of a single channel is considered, and $L = 4$ if rising and falling edges of both Channel A and Channel B are used, the latter configuration being commonly known as the quadrature configuration mode. The quadrature configuration of the sensor facilitates the detection of the direction of the rotation by detecting the relative phasing of the two channels.

The pulse count (PC) and elapsed time (ET) are two well-known methods [2] for the speed estimation, based on encoder edge count over a fixed time interval, and time measurements in revolutions per minute (rpm), using the following equations:

$$N_{PC} = \frac{\Delta\text{pulse}}{T_s} \times \frac{60}{R \times L}$$

(2)

$$N_{ET} = \frac{1}{T_e} \times \frac{60}{R \times L}$$

(3)

The term $T_e$ represents the fixed sample time of the motion control loop. $\Delta\text{pulse}$ represents the number of encoder pulses (transitions) between consecutive sampling instants and $T_e$ is the time between consecutive encoder pulses.

A more recent method, the constant sample-time digital tachometer (CSDT), is introduced in [3]:

$$N_{CSDT} = \frac{\Delta\text{pulse}}{T_s + \Delta t} \times \frac{60}{R \times L}$$

where

$\Delta t = t(i-1) - t(i)$

The error of the elapsed time method increases as the speed increases. On the contrary, the relative error of the pulse count method (which is often substantial) decreases with increased speed. Several filtering techniques can be used to reduce the error of the elapsed time method; here an oversampling technique is implemented with that aim.

Fig. 1 Different encoder configurations with different resolutions
The auxiliary time, $\Delta t$, is used to modify the time $T_{ns}$, so that an integer number of encoder transitions are used to estimate the speed as detailed in Fig. 2.

The use of this auxiliary time greatly improves the accuracy of the speed estimation. Previous works in [3, 4] present experimental results for this method. The implementation of the CSDT, on a single chip, using a new targeted Analog Devices advanced digital signal processor (ADSP), is a novel contribution of this work.

Specifically, the paper presents an experimental comparison of the aforementioned speed estimation methods on the CM403f DSP from Analog Devices [5]. Fig. 3 shows the setup used for closed-loop testing. A theoretical comparison study of the static errors of the speed estimation methods is presented first. Next, the static error found in a practical implementation of the methods is measured with a signal generator that emulates an ideal optical incremental encoder, thereby isolating the characteristic static error of each method.

The speed estimation errors can be divided in two main categories: static error and dynamic error, corresponding to the accuracy of the speed measurement and the capability of the system to track a variable signal, i.e. accelerations. This paper is focused on the static error characteristic of the above-mentioned three methods.

### 2 Theoretical analysis of measurement errors.

The speed estimation errors can be divided in two main categories: static error and dynamic error, corresponding to the accuracy of the speed measurement and the capability of the system to track a variable signal, i.e. accelerations. This paper is focused on a comparison study of the static error characteristic of the above-mentioned three methods.

#### 2.1 Measurement errors

Several factors can affect the accuracy of the measurement over one transition (the theoretical location of encoder edge and actual location) as shown in Fig. 4.

The term $\theta$ in Fig. 4 represents the position of the expected ideal transition. The term $\theta_1$ is an error in the location of the transition due to incorrect assembly, manufacturing tolerances, and the electric circuit that is used to condition and square the optical signal from the photodetector [6]. Those errors are periodic and their impact is often significant on the speed estimation, especially in a quadrature configuration at high speed. Those errors are sometimes reduced by using filters, but this will affect the dynamic performance of the system. The term $\theta_2$ represents variations on the speed measurement produced by motor accelerations like motor friction and unbalances. The effect of $\theta_2$ in the speed measurement can be reduced in a closed-loop configuration.

Additionally, the acquisition system, the CNT peripheral of the ADSP, introduces some errors because it is a digital device with quantised peripherals, thereby potentially degrading the quality of the speed measurement slightly.

### 3 Implementation of the methods on the ADSP

This section will cover the practical information required to implement the three different speed estimation methodologies under study here and describe the characteristic error of each methodology.

#### 3.1 Processor description and implementation of the speed estimation methods

The ADSP CM403f is a mixed-signal control processor with an ARM Cortex-M4 architecture. It includes a floating-point unit, a 24-channel analog front-end (AFE) with 24 sixteen-bit analog-to-digital converters (ADCs) and 2 twelve-bit digital-to-analog converters (DACs). The core clock frequency is 240 MHz [5]. A counter unit (CNT) provides dedicated counting/timing circuitry that facilitates processing of the encoder output, unaffected by other control software. The CNT on-chip circuitry, combined with the general-purpose timer (TIMER), allows several speed estimation methods to be implemented.

Fig. 5 shows a diagram of the relevant registers for the motion control of the ADSP, where the SYSCLK is an 80 MHz free-running clock used by the CNT peripheral for time measurement. Simultaneously, a different timer generates an interrupt at a user-defined sample interval $T_{ns}$ which is the control interval at which the CNT peripheral is sampled. Channel A and Channel B represent the quadrature encoder signals. Relevant registers of the CNT for motion control are as follows:

The TIMER_TMRn_CNT register shows the number of SYSCLK cycles since the last transition. The TIMER_TMRn_PER register records the time between the two preceding transitions. These registers are related to the time count feature of the CNT peripheral. Both are reset by hardware with each encoder transition. The CNT_CNTr register provides the total increasing (non-restartable) number of encoder edges (transitions) since some arbitrary initial start time. It is stored in a 32-bit register.

#### 3.2 Classical speed estimation methods

The subscripts $k$ and $k-1$ are used to refer to adjacent samples in the following expressions.

(i) For the pulse count (PC) method.
3.3 Errors of classical speed estimation methods.

The characteristic percentage error \( e \) for each methodology can be analysed as presented in (9).

\[
e = \frac{|N_{Th} - N_{Act}|}{N_{Th}} \times 100\%
\]

where \( N_{Th} \) and \( N_{Act} \) represent the theoretical and the actual measured speeds, respectively.

The symbol \( \delta \) represents any deviation from the theoretical register result. The PC method counts the number of encoder pulses, while the ET and CSDT methods count the number of pulses \( m \) of a high-frequency clock (SYSCLK). Typically, the error due to the \( \delta \) is \( \pm 1 \) pulse counts [7]. The expressions (5), (6), and (7) are redefined by including the effect of spurious pulse counts.

\[
N_{PC,real} = \frac{\Delta \text{Pulse count} \pm \delta \text{Pulse count}}{T_s} \times \frac{60}{L \times R}
\]

\[
N_{ET,real} = \frac{1}{m \pm \delta m} \times \frac{60}{L \times R}
\]

\[
N_{CSDT,real} = \frac{\Delta \text{Pulse count} \pm \delta \text{Pulse count}}{T_s} \times \frac{60}{L \times R}
\]

where \( m = \text{TIMER}_n\text{TMRn}_\text{PER} \)

The ADSP's dedicated hardware, for counting/timing of the register is reset by hardware; consequently, the latency is reduced.

For the constant sample-time digital tachometer (CSDT),

\[
N_{CSDT} = \frac{\Delta \text{Pulse count}}{T_s + \frac{\Delta T}{\text{SYSLCLK frequency}}}
\]

where \( \Delta T = \text{TIMER}_n\text{TMRn}_\text{CNT} - \text{TIMER}_n\text{TMRn}_\text{CNT} \)

\[
N_{ET} = \frac{\Delta \text{Pulse count} \times \frac{60}{\text{L} \times R}}{\text{TIMER}_n\text{TMRn}_\text{PER} \times \text{L} \times R}
\]

where \( \Delta \text{Pulse count} = \text{CNT}_n\text{CNT} - \text{CNT}_n\text{CNT} \)

3.4 Experimental validation of the implemented methods with an ideal encoder emulator.

In this section, only the processor performance is analysed for the PC, ET, and CSDT methods. This can be done by emulating the encoder using a signal generator (TTi 50 MHz Dual Function/Arb/ Pulse Generator TG5012A) to produce the encoder signals. The emulated speed is set at 1038 rpm in quadrature configuration mode, \( R \times L = 4000 \), and a sampling control interval of \( T_s = 1 \) ms.

In Fig. 7a, PC has the highest percentage speed error of 1.1561%. Speed measurement is affected by a variable number of transitions per \( T_s \) (69–70), as can be seen in (b). The ET method indicates a speed error of 0.1793%, this corresponds to a minimum theoretical count error \( \pm 2 \) counts twice that of the theoretical minimum \( \pm 1 \) counts. As can be seen in (c), the maximum count error is \( \pm 2 \) counts because the timer register is incremental and is reset with every incoming transition. Finally, the CSDT presents the lowest speed error of 0.00488%, through the use of the auxiliary time \( \Delta T \), see (d).

In terms of implementation, the PC method is the simplest method because it only requires a single peripheral to detect edges or transitions. The ET method is implemented by combining a timer and an edge or transition detector. The implementation of the CSDT involves a more sophisticated peripheral configuration, as already explained.

5 Closed-loop experimental validation.

In this section, each methodology is tested with a real optical incremental encoder coupled to the shaft of the encoder. The DC
motor is controlled by a digital proportional and integral (PI) regulator.

Initially, the test is performed at low speed, when the number of transitions per sampling interval \( n \) is less than one (<1 tr./\( T_s \)). At low speed, only the ET is used to estimate the speed for feedback purposes.

Next, the test is performed at high speed (>1 tr./\( T_s \)). The armature current spectrum of each method is included as a figure of merit in order to compare the influence of the different methods on the current control loop. Additionally, an oversampling technique is implemented to reduce the error of the ET method at high speed.

### 5.1 Closed-loop low-speed test.

The ET methodology is used to estimate the speed at low speed. Fig. 8 shows the speed reference step from 60 rpm (0.1 tr./\( T_s \)) to 540 rpm (0.9 tr./\( T_s \)). The characteristic error of the ET is smaller at low speed and increases as the speed increases. As the speed reduces, the system becomes unstable as a consequence of the reduction of the phase margin. To cope with this problem, the gain of the digital PI regulator is reduced.

### 5.2 Closed-loop high-speed tests.

Fig. 9 shows the response of the closed-loop system to a speed reference step from 600 to 1100 rpm. The encoder resolution is \( L \times R = 4000 \text{ ppr} \) (encoder in quadrature configuration) and the control sampling interval is 0.1 ms. Three tests are performed with PC, TE, and CSDT methods as the feedback signal.

As can be seen in Fig. 9a, the accuracy of the PC method improves at higher motor speeds due to an increased number of transitions per \( T_s \). Conversely, the accuracy of ET diminishes as the motor speed increases. At high speed, the number of SYSCLK cycles between transitions is lower, thereby increasing the effect of a spurious count of SYSCLK cycles. In addition, the impact of errors described in section 2.2 is more noticeable in the measurement of the ET at high speed. The CSDT method output is by far the most accurate as a consequence of including the auxiliary time \( \Delta T \).

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**Fig. 6** Percentage error

**Fig. 7** Experimental results of open-loop testing. In (a) Estimated speed symbols are: '*' is PC, '∥' is ET and 'Δ' is CSDT, theoretical speed is 1380 rpm. In this figure, (b) Is the number of transitions per \( T_s \), (c) Represents the time elapsed between preceding transitions and, (d) Is the auxiliary time \( \Delta T \).

**Fig. 8** Speed reference step test from 60 rpm (0.1 tr./\( T_s \)) to 540 rpm (0.9 tr./\( T_s \)). Speed estimation based on the ET method. \( R = 1000 \text{ ppr} \)

**Fig. 9** Variation of motor drive efficiency (a) Speed reference step test from 200 rpm (1.33 tr./\( T_s \)) to 1200 rpm (8 tr./\( T_s \)). \( R \cdot L = 4000 \text{ ppr} \). The green line is the speed estimated when the ET is used to close the loop; the black line is the PC and the red line corresponds to the speed when the CSDT closes the loop, (b) Represents the signal measured with the tachometer. Note that the tachometer is used for display purposes only, and not for the feedback. The green line is ET, the black line is PC and the red line is the CSDT method.
Additionally, the speed step test response of each method demonstrates a similar dynamic performance of each speed estimation method at high speed.

Fig. 9(b) shows the result of the speed measured simultaneously by a tachometer when using each one of the speed estimation methods to close the loop. By using this sensor, the performance of the motor shaft motion can be evaluated in similar conditions over the three performed speed reference step tests.

By comparing Figs. 9(a) and (b), it can be seen that the motor, the driver, and the digital PI controller filter the noise that can be seen in the speed estimated signal used to feedback the speed control loop as shown in Fig. 9(b). From the motion control loop perspective and regardless of the accuracy of the methodology used, all the methodologies perform similar due to the natural filter of the mechanical motor pole and the PI that filter the noise.

However, in motor applications with a double control loop (an inner current loop and outer speed loop), the control loop has a wide bandwidth (BW) so that the noise affects the current loop, as demonstrated in Fig. 10. The current spectra of the ET at low speed are similar in magnitude to the current spectra of the PC and the CSDT methods (see Fig. 10(a)). On the contrary, at high speed, the magnitude of the ET current spectra is higher as a consequence of the corresponding error of the ET (see Fig. 10(a)).

In order to filter the noise, an oversampling technique is applied to the ET signal. It is based on oversampling the TIMER_TMRn_PER register at a higher rate than \( T_s \). To do that, a timer interrupt service routine (ISR) is set and a circular buffer of length \( P \) stores the last \( P \) samples of the time elapsed between consecutive transitions. The average ET between transitions is obtained from the circular buffer as in (16).

\[
N_{\text{rpm}} = \frac{1}{(\sum_{i=1}^{P-1} \text{TIME}\_\text{TMRn}_{\text{PER}}) / P} \times \frac{1}{(\text{SYSCLK frequency})} \\
\times \frac{1}{60 \times L \times R}
\]  

A speed reference step test from 600 to 1100 rpm is presented. The oversampling technique is evaluated at the frequency of 100 kHz and \( (P = 100) \). Fig. 11 shows the resulting reduction of the errors in both low and high speeds.

6 Conclusions

Three speed estimation methods: PC, ET, and CSDT are successfully implemented on the ADSP and tested in closed-loop configuration. The ET presents high-speed error as the speed increases. In opposition, the PC has lower speed error at high speed. The CSDT has consistently the lowest speed error. While the speed error does not affect the speed control loop because the mechanical pole of the motor and the PI controller filter the noise, it does affect the current loop. To reduce the noise of the ET at high speed, an oversampling technique is applied. In terms of implementation requirements, the PC can be implemented by means of an edge detector and counter. The ET, which is based on the inverse proportionality of the speed and the elapsed time between consecutive pulses, requires a timer; the higher the frequency of the timer, the lower the error will be. Conversely, the CSDT requires a peripheral that combines pulse count and time count. The integrated and targeted functionality of the ADSP devices minimises the latency involved in the speed estimation, which can improve the overall servo-system control.

8 References

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Fig. 10 Current spectra of the armature when the ET (green), the PC (black) and the CSDT (red) are used to feedback the control loop

Fig. 11 Oversampling technique applied to the ET to filter the inherent noise of this technique at high speed

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