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Oxide semiconductor thin-film transistors with nano-splitting and field-surrounding channels fabricated by subwavelength photolithography

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Abstract

Oxide semiconductors feature high tunability of carrier concentrations under the control of electric field. In thin film transistors (TFTs), applying dual gate has been reported to be efficient in enhancing the coupling between the gate field and the channel accumulation. In this work, we demonstrate nano-splitting and field-surrounding semiconducting channels (based on InGaZnO) in TFTs, which is fabricated by facile subwavelength photolithography. In such TFTs, semiconducting channels have 200 nm gaps parallel to the drain field, are wrapped by oxide insulators and thus the gate field. The devices show enhanced performance as compared with dual-gate and single gate TFTs, exhibiting higher drain current and steeper subthreshold swing. The maximum transconductance $g_m$ is 27.9% higher than dual gate TFT and 73.1% higher than single gate TFT. According to device simulation, the improvement of the wrapping insulators device correlates with the three-dimensional accumulation of carriers and increased gate electric field near the semiconductor-dielectric interface. These surrounded-channel effects become noticeable in the device with the gap distance less than 1 $\mu$m, with gate electric field squeezing in the submicron gaps. The proposed approach offers an alternative way to take advantage of the oxide semiconductors and their application in TFTs with related circuits.

1. Introduction

Oxide semiconductors with high tunability of carrier concentrations, as major components of thin film transistors (TFTs), are widely applied in the field of sensors [1, 2], optoelectronic [3, 4] and the driving circuits of liquid-crystal display [5, 6] as well as organic light-emitting diode [7, 8]. With the development of the application, the requirement of the device performance synchronously increases, such as enhancing the output current, field-effect mobility and improving the switching speed. Recently, several groups have been proposed that double gate or dual gate structure could effectively optimize the characteristics of oxide TFTs [9–12]. Three mechanisms have been reported for the improved performances of the dual gate TFT. Firstly, dual-gate structure can reduce the proportion of electron trapped by the shallow trap states to all accumulated electrons [13]. Secondly, the larger output current induces higher temperature in dual-gate TFT, thereby increases the mobility for the semiconductor positively correlated with temperature [14]. Thirdly, the active layer is ‘electrically surrounded’ by gate electric field, since the top and bottom gate electrodes are short-circuited. Electrostatic control and carrier accumulation are strengthened by the extension from two-dimension (interfaces) to three dimensions (bulk) [15, 16]. Besides, semiconductor layer with nano- or micro-structures have drawn much attention in TFT fabrication with the advantages, such as better mechanical stability in flexible electronics [17] and optimizing crystalline orientations in organic semiconductor [18–20]. Furthermore, patterns in semiconductor can create nanorods or splits structure, offering the possibility to realize finlike TFT with stronger gate controllability [21]. Refer to concept of dual gate devices [9, 10], we suppose that a wrapping
insulators configuration TFT with nano-splitting active layer could take full advantages of surrounded-channel effects in gate electric field to obtain much better performance than ordinary dual gate and single gate transistors. Nowadays, the pattern methods have been reported in nano- or micro-structures transistors are conventional lithography [17, 22, 23], electron beam lithography [19], nanoimprint lithography [18, 21, 24], lithographically controlled wetting [20, 25], etc. However, these technologies have their shortcomings in resolution, cost of facility, application, and repeatability. Therefore, we apply the newly reported subwavelength photolithography technology to fabricate oxide transistors with nano-splitting channels [26]. In this cost-effective strategy, the tips of total-reflective polydimethylsiloxane (PDMS) soft photomask focus the exposure light to generate subwavelength photoresist patterns through ordinary lithography equipment. Thus, it is capable for us to fabricate the device with nanoscale patterns and study the physical mechanism of these nanostructures.

In this work, wrapping insulators oxide transistors with nano-splitting active layers are investigated. The split IGZO layers were patterned by cost-effective subwavelength photolithography with the gap distance around 204 nm. Based on the dual gate devices, this configuration has connected the top and the bottom gates, with SiO2 dielectric layer filling in the gaps and wrapping the nano-splitting active layers. Compared to the dual gate transistors with uniform and continuous semiconductor layer, wrapping insulators devices have the shorter channel width, but achieve improved electrical performance including 35.6% larger drain current, 27.9% higher transconductance, and steeper subthreshold swing with the value of 160 mV/dec. The physical principle of the wrapping insulators TFT is researched by device simulation. Owing to this particular structure, the three-dimensional accumulation of carriers is observed in nano-splitting active layers. The enhanced carrier density and gate controllability contribute to the improved performances. These surrounded-channel effects become noticeable in the wrapping insulators device with the gap distance less than 1 μm, with gate electric field squeezing in the submicron gaps. The present work reveals the correlation between nano-splitting active layers and the enhanced performance in transistors, offering an alternative way to take advantage of the oxide semiconductors and their application in TFTs with related circuits.

2. Experimental section

The wrapping insulators IGZO TFTs were fabricated on 2 cm × 2 cm heavily doped p-type Si substrate or Si wafer with a 100 nm thick SiO2 layer. A 30 nm IGZO film was deposited onto the substrate with dielectric layer by radio frequency sputtering. Then, the IGZO layer was patterned by double exposure with subwavelength photolithography [26] and conventional lithography, as shown in figures 1(a), (b). Firstly, a layer of 20% (v/v) diluted positive-tone photoresist was spin-coated at 500 rpm for 10 s and 4000 rpm for 40 s onto IGZO layer. The photoresist-coated samples were soft baked on a hot plate at 120 °C for 2 min. In the first exposure, the textured PDMS photomask was placed on sample surface and the samples were exposed for 1 s with UV light of wavelength 365 nm. The light control principle and the detailed procedure of subwavelength photolithography have been reported in the previous work [26]. The samples were subsequently exposed for 20 s with Cr mask as conventional lithography. The exposed photoresist layer was developed for 2 min and the IGZO films were then etched in hydrochloric acid solution (38% hydrochloric acid: deionized water = 1 ml:150 ml) for 2 min. After
removing the residual photoresist, the patterned IGZO films were post-annealed at 350 °C in N₂ atmosphere for 1 h. The source and drain electrodes consisted of 100 nm thick Mo deposited by direct current (DC) sputtering through shadow masks. After that, a 300 nm SiO₂ as top gate dielectric layer was deposited by plasma enhanced chemical vapor deposition (PECVD) at 180 °C. The via holes, source and drain electrodes contact holes were defined by photolithography and the SiO₂ layer was dry-etched by reactive ion etching. Finally, the top gate electrodes consisted of 100 nm thick Mo deposited by DC sputtering through shadow masks. For comparison, dual-gate or single gate IGZO TFTs with uniform and continuous active layer as the control group were fabricated in the same condition without the procedure of subwavelength photolithography. In DG-TFT and WI-TFT, top gate connects with bottom gate through the via hole. During electrical tests, the gate voltage simultaneously sweeps at both top and bottom gate to realize dual-gate-driving. All the devices were electrically characterized by a semiconductor parameter analyzer (Agilent B1500A) under ambient conditions in the dark at room temperature unless stated otherwise. All the TFT simulation results shown in figures 4 and 5 were calculated by the technology computer-aided design (TCAD) 2D device simulations.

3. Results and discussion

Utilizing the fabrication method of nano-splitting active layers, we produce wrapping insulators IGZO TFT as shown in figure 2(a). Based on the configuration of early reported dual gate TFT [9, 10], WI-TFT replaces the uniform active layer with split active layers. Notably, the direction of nanostructured stripes is parallel with the length of the TFT channel, hence the IGZO layers are separated in cross-section view from the direction of channel width as the red dash line in figure 2(a). The optical microscope and scanning electron microscopy images of split IGZO layers in figure 2(d) show the gaps are 204 nm wide. Because the period of the textures on PDMS mask is 4 μm, the widths of split IGZO layers are around 3.8 μm. During the fabrication process, an extra SiO₂ layer was deposited by PECVD on the patterned IGZO layer. The SiO₂ layer fills in the nano-gaps and serves as both the top and bottom dielectric layers wrapping the nano-splitting IGZO channels, as seen in the cross-section schematic (figure 2(c)). For comparison, SiO₂ dielectric layers and uniform IGZO active layer exhibit sandwich structure in dual gate TFT. An extra Mo top-gate electrode is connected with the bottom-gate electrode by via holes so that the top and bottom gates simultaneously tune the field and carrier concentrations.

The electrical properties of wrapping insulators and the reference dual gate devices are directly compared in figure 3. As shown in the transfer curve in the saturated regime (V_D = 15 V), both devices achieve negligible hysteresis effect and good device performance. The subthreshold swing (S.S.) is calculated from the transfer curves with the equation of S.S = (∂log(I_D)/∂V_G)⁻¹. In figure 3(b), DG-TFT exhibits a S.S. of 291 mV/dec, while
WI-TFT shows a markedly decreased S.S. of 160 mV/dec. In addition, WI-TFT has lower values of S.S. than DG-TFT in the entire subthreshold regime ($V_G=0.5$–$4$ V). The steeper subthreshold swing indicates that WI-TFT achieves stronger gate control ability than DG-TFT. For the output characteristic curves, DG-TFT exhibits slightly current crowding effect at low drain voltage, because of the oxidation of Mo electrode during the fabrication process. More interestingly, although WI-TFT has shorter channel width than DG-TFT due to the split IGZO active layers with subwavelength gap, wrapping insulators device obtains obviously larger drain current and shows no obvious current crowding effect. The maximum drain current $I_D\text{max}$ of WI-TFT is 179 $\mu$A at $V_G = V_D = 15$ V, which is 35.6% higher than that of DG-TFT ($I_D\text{max} = 132 \mu$A). Note that the carrier concentration does not follow formula for the ideal transistors in devices with different structure, hence we utilize transconductances $g_m = \partial I_D/\partial V_G$ rather than calculate field-effect mobility as the figure of merit for valuing the gate-tunability of conductance and the output current. The transconductances $g_m$ of the reference single gate TFT (SG-TFT), DG-TFT and WI-TFT are compared in figure 3(e). Due to the stronger coupling between the gate and the channel [10], the maximum $g_m$ of DG-TFT increases from 16.7 to 22.6 $\mu$S at $V_G = 15$ V. Such effect is even reinforced, in WI-TFT, the maximum $g_m$ is even higher with the value of 28.9 $\mu$S at $V_G = 15$ V, corresponding to an increase of 27.9% to DG-TFT and 73.1% to SG-TFT, respectively. The higher output current and transconductance manifest that the advantages of the structure effect in wrapping insulators device far beyond the shortcoming of the reducing channel width. Similar trends are observed in the differential factor between square root of drain current $\sqrt{I_D}$ and gate voltage $V_G$ ($\partial \sqrt{I_D}/\partial V_G$), which can reflect the relationship between the field-effect mobility and gate voltage (figure 3(f)). WI-TFT shows larger value of this differential factor and gradually saturated as the increasing gate voltage. According to transport model in amorphous oxide semiconductor [27], WI-TFT realizes percolation-dominance transport with strong gate-field inducing high Fermi-level crossing the conduction band edge. By contrast, the differential factors in SG-TFT and DG-TFT exhibit gate voltage dependence as the property between trap-limited conduction and percolation transport, which indicates that the Fermi-levels in these devices are around or below the conduction band. The detailed parameters extracted from these three types of transistors are summarized in table 1.
To investigate the structural effects, we employed the TCAD two-dimensional simulation to visually reveal the working state of the devices. As shown in figures 4(a), (b), for wrapping insulators device, the simulated active layer is separated with nano-gap of 200 nm, while the active layer is continuous and uniform in the dual gate device structure. In this simulation, we mainly focus on the relation between the device structure and the gate control ability, thus 2D simulation areas are the cross-section of the device from the direction of channel width without regard to the effect of drain voltage. These settings of simulation are based on the following three reasons. Firstly, the drain voltage acts as the driving force of carriers’ drift during the device operation. When the devices with different structures compare at the same testing condition, the same value of V_D is irrelevant to the improvement of the output current according to the current equation of TFT, especially in the saturated regime. Secondly, nano-gaps are parallel to transverse electric field induced by drain voltage, which hardly influences the intensity of electric field in this direction. Thirdly, split active layers greatly impact the formation of conductive channel, which is electrostatic coupled by the gate voltage with the carrier accumulation at the interface between semiconductor and dielectric layer. This structural effect can be clearly reflected through the distribution of carrier concentration and electric field in view of our simulation structures.

In figures 4(c)–(f), the distributions of vertical electric field and electron concentration inside the split and uniform active layer are directly exhibited in the simulation result. Both devices are operated at V_G = 40 V with the same simulation parameters except for the devices’ geometries. Induced by the gate voltage from top and bottom gate electrodes, both wrapping insulators and dual gate devices show strong electric field at the lower and upper interface between semiconductor and dielectric layer, where was named as front-channel and back-channel, respectively. Especially, the intensity of the electric field is strengthened at the edge of split active layers in WI-TFT. For more details about the operation in the channel area, we extracted the simulated data from the front-channel and back-channel area as the cutline shown in figure 4(a). From figure 5(c), wrapping insulators devices achieve stronger gate-control ability with enhanced electric field not only at the edge but also in the entire split active layer, compared with double gate device. With stronger vertical electric field, more electron would accumulate at the interface of split active layers and dielectric layer in wrapping insulators device, as shown in figures 4(e), (f) and 5(d). What’s more, three-dimensional accumulation of carriers is obtained by enhanced electrostatic coupling, as the nano-splitting active layers are electrically surrounded gate electric field. Thus, electron accumulation of wrapping insulators device is different from the 2D accumulation in common TFT device, and the equations of ideal transistor might be no longer applicable. For accuracy, we use transconductances instead of field-effect mobility in above analysis.

The improvement of device performance in WI-TFT can be explained by above simulation results. Firstly, the higher electron concentration caused by surrounded-channel effects in wrapping insulators device increases the conductance of channel area in active layer, which contributes to the larger output current than dual gate device. Secondly, the higher carrier concentration induced by the structure can suppress the Schottky barrier and current crowding effect. Thirdly, The stronger charge accumulation and higher carrier density result in enhanced field-effect mobility of disordered semiconductors (i.e. IGZO in this case), according to the trap-limited or percolation transport model [27]. As a result, WI-TFT exhibits higher transconductances than DG-TFT and SG-TFT, although with shorter channel width.

For subthreshold swing, the relationship of the capacitance and S.S. in dual gate transistor depends on the following equation [11]:

### Table 1. Parameters extracted from single gate transistor, dual gate transistor and wrapping insulator transistor.

| Structure          | Nanostructured channels | µ* (cm² V⁻¹ s⁻¹) | V_TH (V) | g_m (µS) | ∂/∂v/I_D/(A/V²) / V | S.S. (mV/dec) | I_D-max (µA) | I_D/I_D-off |
|--------------------|-------------------------|-----------------|----------|----------|---------------------|---------------|--------------|-------------|
| Single gate        | w/o                     | 5.58            | 1.65     | 16.7     | 7.52 × 10⁻⁴         | 444           | 102          | 10⁰         |
| Dual gate          | w/o                     | 2.03            | 22.6     | 8.79 × 10⁻⁴ | 291             | 132           | 10⁰         |
| Wrapping insulator | With                    | 2.20            | 28.9     | 1.04 × 10⁻³ | 160             | 179           | 10⁰         |

* Field-effect mobility in the saturation region (V_D > V_G – V_TH) extracted from the transfer curve by using the equation µ* = 2eD/(V_TH)^2. Here, I_D is the drain current, V_D is the drain voltage, V_G is the gate voltage, V_TH is the threshold voltage, W and L are the width and length of the channels, respectively, and C_G is the capacitance of the gate dielectric per unit area.

b Maximum transconductances g_m at V_G = V_D = 15 V.

c In WG-TFTs, we do not calculate field-effect mobility as the carrier concentration does not follow the formula for the ideal transistors. The differential factors are extracted from the slope of a certain segment in √/V_D − V_G curves (saturated regime).

d Maximum drain current I_D-max at V_G = V_D = 15 V.
where \( C_{IGZO}, C_{OX1} \), and \( C_{OX2} \) are the capacitances of the semiconductor and gate dielectric at front and back channels, \( C_{it1} \) and \( C_{it2} \) are the interface trap capacitances of back and front channels, \( k \) is the Boltzmann constant, \( T \) is the temperature in Kelvin, \( q \) is the charge of an electron. As DG-TFT and WI-TFT are fabricated with the same procedures, these two devices are assumed to share the same values of interface trap and dielectric capacitances. Thus, the only variate in equation (1) is \( C_{IGZO} \). Taking the derivative of equation (1) with respect to \( C_{IGZO} \), it easy to find that subthreshold swing is a monotony decrease function of \( C_{IGZO} \). As proved by above simulation, WI-TFT exhibits higher electron concentration in active layer. With the relation of \( C = Q/U \), WI-TFT has larger capacitance of IGZO than DG-TFT under the same condition, and thereby achieves lower subthreshold swing.

The concept of splitting active layer in single layer oxide TFTs has been reported. In the previous work, the excellent device performance and the improvement were correlated to metal-F bonds from NF3 plasma during etching stopper patterning [17]. For the proposed wrapping insulator transistor, such fabrication factors are excluded and only the surrounded-channel effects caused by the nano-structure are attributed to the improvement.

In the next simulation, we further investigate the relationship between the nano-gap distances and improvement of gate-control ability. A series of WI-TFT with various gap distances and a fixed split width of 3.8 \( \mu m \) are simulated in the same condition. The values of electric field \( F \) and electron concentration \( n \) extracted from the front channel and the back-channel in WI-TFT with various gap distances and DG-TFT are directly compared in figures 5(c), (d). For the WI-TFT with 2 \( \mu m \) gap distance, both \( F \) and \( n \) are greatly enhanced at the...
edge of the split IGZO layer, yet almost unchanged in the middle of IGZO layer as compared with those in the conventional devices. As the gap distances decrease, the \( F \) and \( n \) in IGZO layer gradually increase and reach saturation with the gap distance less than 1 \( \mu \)m. In addition, the channel width of the device shortens as the gap distance enlarges at the same device size. The output current of the device will be greatly attenuated by the large gap distance. These results testify the necessity of subwavelength photolithography technology and producing active layer with nanostructures, because of insufficient resolution of the conventional photolithography in lab.

To discover the reason for these differences, the vertical electric field in dielectric SiO\(_2\) layers in wrapping insulators device with 200 nm and 2 \( \mu \)m gap distances are simulated as shown in figures 5 (a), (b). The vertical electric field is much larger when the gap is 200 nm as compared with that when the gap is 2 \( \mu \)m, which is squeezed in the submicron gaps due to the increased height-to-width ratio of the gap. This additional gate field from surrounded-channel effects not only induces 3D accumulation of carriers at the edge but also enhances the gate control ability of the devices. Such effect might be even stronger with the ultra-thin semiconductor layer because of the bulk accumulation. However, the mechanism of reducing semiconductor thickness is more complicated [16, 28]. A complete experiment will be carried out in future work to thoroughly analyze the relation between thickness and the surrounded-channel effect in WI-TFT. In summary, the simulation results well illustrate how nano-splitting semiconducting channels feature strengthened gate-tuning in the conductance with higher on-current and steeper subthreshold swing, which offers a new option to optimize the performance of TFTs.

Figure 5. Results of TCAD two-dimensional simulation. (a), (b) The intensity of vertical electric field between the gap of split IGZO channels with 200 nm and 2 \( \mu \)m gap, respectively. (c), (d) The sum of the values of electric field and electron concentration extracted from the front-channel and the back-channel in WI-TFT with various gap distances and DG-TFT \((V_G = 40 \text{ V})\), respectively.
4. Conclusions

We report a new oxide TFT with nano-splitting and field-surrounding semiconductor channels to improve device performance. The split channels IGZO layers with the gap distance of 204 nm are fabricated by a cost-effective subwavelength photolithography technology, which only requires common lithography facilities to produce nanoscale patterns. The wrapping insulators TFT achieved 35.6% higher drain current and steeper subthreshold swing than conventional dual gate TFT with uniform channel layer. The maximum transconductance $g_m$ in WI-TFT is 27.9% higher than DG-TFT and 73.1% higher than SG-TFT, although WI-TFT with the shorter channel width due to the split structure. The improved performances are attributed to the 3D accumulation of carriers and enhanced gate control at front-channel and back-channel area and the edge of split active layer, proved by 2D device simulation. Such surrounded-channel effect emerges in the wrapping gate device with the gap distance less than 1 μm, with enhanced gate electric field squeezing in the submicron gaps due to the increased height-to-width ratio of the gaps. These experiments and simulation results of wrapping insulators devices offer an alternative way to take advantage of the oxide semiconductors and their application in TFTs with related circuits.

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