Investigation of bilayer HfN$_x$ gate insulator utilizing ECR plasma sputtering

Nithi Atthi$^a$) and Shun-ichiro Ohmi$^b$)

Department of Electronics and Applied Physics, Tokyo Institute of Technology, J2–72, 4259 Nagatsuta, Midori-ku, Yokohama 226–8502, Japan

$^a$) atthi.n.aa@m.titech.ac.jp

$^b$) ohmi.s.aa@m.titech.ac.jp

Abstract: In this paper, we have investigated bilayer HfN$_x$ gate insulator utilizing ECR plasma sputtering especially for the electrical properties with metallic-phase HfN$_{0.5}$ gate electrode which was formed by in-situ process. After PMA of 500°C/10 min in N$_2$/4.9%H$_2$ ambient, the bilayer of HfN$_{1.3}$ (1.7 nm)/HfN$_{1.1}$ (0.9 nm) gate insulator formed on Si(100) showed the EOT of 0.61 nm, leakage current density ($@V_{FB}−1$ V) of 5.5 × 10$^{-3}$ A/cm$^2$ and density of interface states (D$_{it}$) of 5.5 × 10$^{11}$ cm$^{-2}$ eV$^{-1}$. The n-MISFET with bilayer HfN$_x$ gate insulator exhibited saturation mobility ($\mu_{sat}$) of 47 cm$^2$/V s, which is higher than the device with directly deposited HfN$_{1.3}$ gate insulator. HfN$_x$ interfacial layer (IL) with low nitrogen concentration was found to significantly improve the interface properties of HfN$_x$ gate stacks.

Keywords: bilayer, ECR plasma sputtering, hafnium nitride, nitrogen concentration, high-$\kappa$ gate insulator, interfacial layer

Classification: Electronic materials, semiconductor materials

References

[1] J. Robertson and R. M. Wallace: Mater. Sci. Eng. Rep. 88 (2015) 1. DOI: 10.1016/j.mser.2014.11.001
[2] Q. Zeng, A. R. Oganov, A. O. Lyakhov, C. Xie, X. Zhang, J. Zhang, Q. Zhu, B. Wei and L. Grigorenko: Acta Crystallogr. C 70 (2014) 76. DOI:10.1107/S20532961302786
[3] S. Ohmi, S. Kudoh and N. Atthi: IEEE Trans. Semicond. Manuf. 28 (2015) 266. DOI:10.1109/TSM.2015.2431375
[4] S. Ohmi: IEICE Electron. Express 11 (2014) 20142006. DOI:10.1587/exle.11.20142006
[5] G. Bersuker, C. S. Park, J. Barnett, P. S. Lysaght, P. D. Kirsch, C. D. Young, R. Choi, B. H. Lee, B. Foran, K. V. Benthem, S. J. Pennycook, P. M. Lenahan and J. T. Ryan: J. Appl. Phys. 100 (2006) 094108. DOI:10.1063/1.2362905
[6] H. S. Han and S. Ohmi: IEICE Electron. Express 9 (2012) 1329. DOI:10.1587/exle.9.1329
[7] H. S. Han, D. H. Han and S. Ohmi: Electron. Lett. 49 (2013) 500. DOI:10.1049/el.2013.0319
[8] N. Atthi, D. H. Han and S. Ohmi: MRS Proc. 1588 (2014) 1. DOI:10.1557/opl.2014.223
[9] T. Sano and S. Ohmi: Jpn. J. Appl. Phys. 50 (2011) 04DA09. DOI:10.7567/
1 Introduction

Metal gate/high-κ gate dielectric (MG/HK) stacks are promising candidates to replace the conventional poly-Si/SiON gate stack structures to overcome the limitations of scaling in complementary metal-oxide-semiconductor field-effect transistors (CMOS) technology [1]. Among the high-κ materials, Hf-based high-κ gate insulator such as HfO2, HfON and HfSiON has emerged as one of the promising candidates [2, 3, 4]. However, scaling down an equivalent oxide thickness (EOT) beyond 0.5 nm is a great challenge for CMOS technology. This is because the interfacial layer (IL) with relatively low-dielectric constant between high-κ/Si interfaces is formed easily when the oxide-based high-κ gate insulator is used [5]. Therefore, nitride dielectrics are the candidate materials as a gate dielectric to overcome the problems of oxide-based high-κ materials to suppress IL formation [6, 7]. We have reported that 0.5 nm EOTs were obtained by using hafnium nitride (HfN) gate insulator (I) formed by electron-cyclotron-resonance (ECR) plasma sputtering with ex-situ Al gate electrode (G) [8]. However, the contamination and the oxidation during ex-situ Al deposition severely degraded the electrical properties such as mobility. Therefore, in-situ deposition of thermally stable gate electrode is used instead of Al for gate-first process [9].

We have reported that in-situ deposition of HfNx (x < 1.0) gate electrode improves the electrical properties of HfNx gate stacks [10]. The high nitrogen (N) concentration, such as Hf5N4 or higher, would be required for EOT scaling below 0.5 nm since the increase of the N concentration would lead to higher dielectric constant [11]. However, direct contact of HfNx gate insulator with high N concentration (x ≥ 1.2) on Si substrate severely degrades the electrical properties of HfNx gate stacks due to the degradation of interface properties at HfNx/Si interfaces [10, 11]. Various oxide-based IL such as chemical oxide and thermally grown SiO2 have been reported to improve the quality of high-κ/Si interface [12]. However, bilayer gate insulator with oxide-based IL limits the scaling down of an EOT. Therefore, nitride-based IL insulator with low nitrogen concentration is required to prevent the IL formation [13].
In this paper, bilayer of HfN\(_{1.3}\)/HfN\(_x\) (\(x = 1.0–1.2\)) gate insulator utilizing ECR plasma sputtering on the electrical properties of HfN\(_x\) gate stack structures is proposed. The effects of nitrogen concentration in high-\(\kappa\) HfN\(_x\) IL with low nitrogen concentration on the electrical properties of HfN\(_x\) gate stack structures were studied. The influence of post-metallization annealing (PMA) in N\(_2\)/4.9%H\(_2\) forming-gas (FG) ambient was investigated. Furthermore, characteristics of an n-MISFET with bilayer HfN\(_x\) gate insulator were demonstrated.

### 2 Experimental procedure

The metal-insulator-semiconductor (MIS) diodes and n-MISFET device with HfN\(_{0.5}\) (10 nm)/HfN\(_{1.3}\) (1.7 nm)/HfN\(_x\) IL (0.9 nm)/p-Si(100) gate stack structures were \textit{in-situ} fabricated in accordance with schematic structures shown in Fig. 1(a) and Fig. 1(b), respectively. To fabricate the MIS-diode with bilayer HfN\(_x\) gate insulator, p-Si(100) substrates (\(N_A: 1 \times 10^{15} \text{ cm}^{-3}\)) were cleaned by sulfuric peroxide mixture (SPM) and diluted hydrofluoric acid (DHF). Then, 0.9 nm-thick HfN\(_x\) IL with different Ar/N\(_2\) gas flow ratio of 20/8 sccm (N\(_2\): 28.8%, 0.20 Pa), 16/12 sccm (N\(_2\): 44%, 0.20 Pa) and 12/16 sccm (N\(_2\): 57%, 0.20 Pa) were deposited on p-Si(100) by using ECR plasma sputtering (JSW AFTY: AFTEX-3400) [9]. The \(\mu\)-wave/RF power was 500/400 W. The 1.7 nm-thick HfN\(_{1.3}\) (I) layer was \textit{in-situ} deposited on IL utilizing ECR plasma sputtering with Ar/N\(_2\) gas flow ratio of 8/20 sccm (N\(_2\): 71%, 0.20 Pa). The \(\mu\)-wave/RF power was 500/500 W.

Then, 10 nm-thick metallic-phase HfN\(_{0.5}\) gate electrode (\(\phi_{\text{HfN}}: 4.8\text{ eV}\)) was \textit{in-situ} deposited on HfN\(_{1.3}\) (I) using Ar/N\(_2\) gas flow ratio of 10/0.2 sccm (N\(_2\): 2%, 0.09 Pa). The \(\mu\)-wave/RF power was 500/400 W. The PMA was carried out at 500°C/10 min in N\(_2\)/4.9%H\(_2\) FG ambient (1 SLM) by silicon-wafer-covering (SWC) process utilizing rapid thermal annealing (RTA) system [14].

The 40 nm-thick Al contact layer was \textit{ex-situ} evaporated on HfN\(_x\) gate stacks. Al contact layer was patterned by H\(_3\)PO\(_4\):HNO\(_3\) mixed solution (50:3) for 60 s. Then, HfN\(_x\) gate stacks were patterned by DHF (1%) for 90 s. The size of gate electrode was \(90 \times 90 \mu\text{m}^2\). The backside Al contact was deposited by evaporation.
Direct contact of HfNx gate insulator with high N concentration such as 2.5 nm-thick HfN_{1.3} (I) layer on p-Si(100) was fabricated for comparison by using ECR plasma sputtering with Ar/N$_2$ gas flow ratio of 8/20 sccm (N$_2$: 71%, 0.20 Pa). The μ-wave/RF power was 500/500 W. The Al contact/HfN$_{0.5}$ (G) stack layers were deposited on HfN$_{1.3}$ (I) layer by using the same process condition as bilayer HfNx gate insulator MIS-diode.

The n-MISFET was fabricated using conventional gate-last process [7]. After local oxidation of Si (LOCOS) isolation and channel stop formation, source/drain (S/D) was formed by ion implantation of PH$_3$ at 20 keV with a dose of 5 × 10$^{15}$ cm$^{-2}$. The activation annealing was carried out in N$_2$ ambient at 1000°C/2 min. The HfNx gate stacks with HfN$_{1.1}$ IL was deposited by using the same process condition as MIS-diode. After contact holes formation, Al pads were patterned for source, drain and gate electrodes. The gate width (W) was 90 µm and gate length (L) was 10 µm.

The capacitance-voltage (C-V) and current-voltage (J-V) characteristics of bilayer HfNx gate insulator MIS-diode were measured utilizing Agilent 4284A and Agilent 4156C, respectively. A dual-frequency method was used to evaluate the C-V characteristics. The EOTs were extracted from C-V with quantum mechanical correction [15], and the density of interface states (D$_{it}$) was evaluated by Terman method. The film thickness was measured by ellipsometer, and the x-ray photoelectron spectroscopy (XPS) was carried out to evaluate the film composition. The I$_D$-V$_D$ and I$_D$-V$_G$ of n-MISFETs were also characterized.

3 Results and discussion

Fig. 1(c) shows the N$_2$/(Ar+N$_2$) gas flow ratio dependence of N1s spectra on HfN$_x$ films. The nitrogen concentration in HfN$_x$ film was determined by N/Hf fraction, which calculated by the products of peak area of Hf4f and N1s spectra and atomic sensitivity factor (ASF) [16]. The nitrogen concentrations were evaluated as HfN$_{0.5}$, HfN$_{1.0}$, HfN$_{1.2}$ and HfN$_{1.3}$ when the N$_2$ gas flow ratio was changed as 2%, 28.8%, 57% and 71%, respectively. The peak of Hf4f spectra for insulating-phase HfN$_{1.3}$ film was chemically shifted to higher binding energy than metallic-phase HfN$_{0.5}$ film, which attributed to the higher concentration of nitrogen in HfN$_{1.3}$ film [16].

Fig. 2(a) shows the effects of nitrogen concentration of HfNx IL (x = 1.0–1.2) on the C-V characteristics (100 kHz) of as-deposited HfN$_x$ gate stack structures. The HfN$_{1.1}$ IL (N$_2$: 44%) shows the smallest EOT, although as-deposited films show large frequency dispersion in C-V characteristics (not shown). When the N$_2$ gas flow ratio increased, the flat-band voltage (V$_{FB}$) shifted toward positive voltage direction due to decrease of positive fixed charges.

Moreover, the HfN$_x$ gate stacks without IL has higher leakage current density such as J$_g$(@V$_{FB}$ − 1 V) of 5.2 A/cm$^2$ compared to the HfN$_x$ gate stacks with HfN$_{1.1}$ IL (3.8 A/cm$^2$). Whether the HfN$_x$ film with higher nitrogen concentration is required for EOT scaling below 0.5 nm due to its higher dielectric constant, excess nitrogen concentration in HfN$_x$ IL such as HfN$_{1.2}$ IL (N$_2$: 57%) generates high D$_{it}$, which degrades the interface qualities and leads to high leakage paths.
Therefore, HfN\textsubscript{x} IL with N\textsubscript{2} gas flow ratio of 44\%, which corresponds to HfN\textsubscript{1.1} IL, is suitable to improve the interface qualities for bilayer HfN\textsubscript{x} gate insulator.

Fig. 2(b) shows that by using PMA in N\textsubscript{2}/4.9\%H\textsubscript{2} FG ambient with SWC process at 500°C/10 min, the frequency dispersion in C-V characteristics and leakage current density of bilayer HfN\textsubscript{x} gate insulator MIS-diode was well suppressed compared to as-deposited HfN\textsubscript{x} gate stacks (not shown). However, large hysteresis was observed in C-V characteristics so that the PMA process condition should be further optimized.

The dual-frequency method was used to compensate the frequency dispersion and calculate the exact value of EOT. By using PMA in N\textsubscript{2}/4.9\%H\textsubscript{2} FG ambient at 500°C/10 min, the EOT of 0.61 nm with $\Delta V_{FB}$ of $-0.93$ V and $J_g(\@V_{FB} - 1)$ V of $5.5 \times 10^{-3}$ A/cm\textsuperscript{2} were obtained for HfN\textsubscript{x} gate stacks with HfN\textsubscript{1.1} IL. The Dit of annealed HfN\textsubscript{x} gate stacks with HfN\textsubscript{1.1} IL is able to be reduced to $5.5 \times 10^{11}$ cm\textsuperscript{−2} eV\textsuperscript{−1}.

Fig. 3 shows the $I_D$-$V_D$ and $I_D$-$V_G$ characteristics of n-MISFETs device (L/W: 10/90 \mu m) with bilayer HfN\textsubscript{x} gate insulator. The saturation mobility ($\mu_{sat}$) extracted from the results was 47 cm\textsuperscript{2}/(V s), which is higher than our previous reported data [7]. At $V_D$ of 0.05 V, the n-MISFET exhibits excellent performance in terms of near ideal subthreshold swing (SS) of 77 mV/dec. When the $V_D$ increased from 0.05 to 1.0 V, the $V_{th}$ was slightly shifted from $-0.04$ to $-0.03$ V. Furthermore, the SS degraded from 77 to 90 mV/dec, and off leakage current increased two orders of magnitude. This is because the effects of drain-induced barrier lowering (DIBL). Therefore, the superior electrical properties, especially the saturation mobility, are probably attributed to the lower nitrogen concentration of HfN\textsubscript{x} IL improved the interface properties of MISFETs.
4 Conclusions

We investigated the bilayer HfNx gate insulator formation utilizing ECR plasma sputtering for the first time. The EOT of 0.61 nm with low Jg was achieved by using HfN1.1 IL. The n-MISFET device exhibits $\mu_{sat}$ of 47 cm$^2$/V s. It was confirmed that bilayer HfNx gate insulator with low nitrogen concentration of HfN1.1 IL shows significantly improved the interface qualities, which leads to the superior electrical properties of HfNx gate stacks.

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