Survey of Crystal-Oscillator Based Reference Frequency Quadrupler for Frequency Synthesizer

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Abstract. Implementing low phase noise frequency synthesizers often utilizing a high reference frequency input. This paper analyses the reason why increasing the reference frequency can improve the phase noise performance of frequency synthesizers, describes three state of art crystal-oscillator based reference frequency quadruplers, and then summarizes their performance, advantages, and disadvantages.

1. Introduction
Low phase noise or low jitter frequency synthesizers are critical building blocks widely used in modern digital systems and various wireline and wireless applications [1-3]. To meet various requirement, many different phase-locked loop (PLL) based frequency synthesizers are proposed. However, the core of most frequency synthesizers is the basic PLL depicted in Figure 1. It consists of a voltage-controlled oscillator (VCO) and loop components incorporate a phase frequency detector/charge pump (PFD/CP), a loop filter (LF), and an N divider [4]. The noise of the VCO and the noise of loop components dominate the out-band phase noise and in-band phase noise of the PLL, respectively. The in-band phase noise can be approximated as follows:

\[ \text{PLLnoise}_{\text{in-band}} = PN1Hz + 10 \cdot \log \left( \frac{f_{\text{ref}}}{1Hz} \right) + 20 \cdot \log(N) \]  

Where \( PN1Hz \) is the 1Hz normalized phase noise, \( f_{\text{ref}} \) is the reference frequency or the frequency of PFD, and \( N \) is the feedback divider value [1].

As illustrated in Figure 1., the relation between the VCO frequency \( f_{\text{out}} \) and the reference frequency \( f_{\text{ref}} \) can be represented as follows:

\[ f_{\text{out}} = N \cdot f_{\text{ref}} \]
Therefore, given a VCO frequency, increasing the reference frequency $f_{ref}$ by a factor $M$ makes the $N$ decrease by $M$. By this, from (1) that the phase noise can improve by a factor of $10 \cdot \log(M)$. In addition, for a fractional-N frequency synthesizer involved $\Sigma \Delta$ modulator, a higher reference frequency $f_{ref}$ can push the quantization noise from the $\Delta \Sigma$ modulator toward to a higher frequency. And thus, the shaped quantization noise can be attenuated more effectively by the loop filter. The quantization noise spectrum of an $m$th-order MASH-type $\Sigma \Delta$ modulator can be modelled by

$$S_{\Sigma \Delta} = \frac{(2\pi)^2}{12f_{ref}} \left[ 2 \sin \left( \frac{\pi f}{f_{ref}} \right) \right]^{2(m-1)}$$

From (3), we can conclude that the quantization noise has a $3(2m-1)$dB/octave slope improvement with reference frequency $f_{ref}$ increase [5].

2. The Effectiveness of Multiplying Reference Frequency

In [2], when the $f_{ref}$ is 125MHz, the integrated jitter from 10kHz to 40MHz is about 480 fsrms. Whereas, when the reference frequency doubler is turned on, i.e. the $f_{ref}$ is 250MHz, the integrated jitter is about 337 fsrms [2]. In [6], when $f_{ref}$ is 125MHz, $N$ is 10, the $1\sigma$ random jitter is 1.99ps. Whereas, when $f_{ref}$ is 250MHz, $N$ is 5, the $1\sigma$ random jitter is 1.74ps. In [7], the $f_{out}$ is kept the same 20GHz, the phase noise is -113dBc/Hz@1MHz when the $N$ is 20, whereas, the phase noise is -123dBc/Hz@1MHz when the $N$ is 8. Where the high reference frequency and injection-locked techniques improve the phase noise together. [1], [8], and [9] also used reference frequency doublers to achieve better performance. In [10], a low noise injection locked integer-N digital bang-bang PLL that multiplies a 50MHz reference to an 800MHz clock is cascaded with an LC fractional-N PLL to achieve low phase noise. The whole cascaded PLL has a reference frequency multiplier with a factor of 16 and achieves the worst-case RMS jitter of 356 fsrms over 100Hz to 40MHz integration bandwidth. These cases demonstrate the efficacy of multiplying reference frequency.

3. The Emerged Quadrupler Schemes

![Figure 2](image-url)

**Figure 2.** The differential XO based quadrupler: (a) the architecture, (b) the principle.

The reference signal usually derived from a low-noise and low-cost Crystal Oscillator (XO) which has typically less than 60MHz output frequency. How to implement reference frequency multiplier with more than double is a research focus. An XOR gate is usually used to implement reference frequency double. However, using multiple doublers in series simply to realize more than double
multiplier is impossible because the duty-cycle of the output of the first doubler is non-50%. This non-50% duty-cycle error directly results in period jitter at the output of the next doubler [3, 11]. On the other hand, using an injection locked integer-N PLL or MDLL to realize the reference multiplier makes power consumption and area is high [11].

In recent years, three compact reference frequency quadrupler schemes are proposed [3, 11, 12]. The principle of them is analysed in this section. And the performance comparisons are described in next section.

3.1. The Differential Xo Based Quadrupler Scheme

In general, a sinusoidal wave can be modeled mathematically as follows:

\[ V(t) = A \cdot \sin(2\pi ft) + V_{CM} = A \cdot \sin(\theta(t)) + V_{CM} \]  

(4)

Where \( A \) is the amplitude, \( f \) is the frequency, \( \theta(t) \) is the phase, and \( V_{CM} \) is the common level i.e. direct current portion of the sinusoidal signal. As illustrated in Figure 2 (b), when the voltage is \( V_{CM} - A/\sqrt{2} \), it corresponds two points in a period \( T_{OX} \). The temporal relation between these two points is \( T_{OX}/4 \), i.e. 25% duty-cycle. When the voltage is \( V_{CM} + A/\sqrt{2} \), the case is also the same. The first reference frequency quadrupler with sub-picosecond jitter is presented in [11], as depicted in Figure 2. A differential XO generates a pair of complementary sinusoidal waveforms. These two waveforms are fed to two skewed inverters whose threshold voltages are adjusted by Duty Cycle Correction (DCC) feedback to \( V_{CM} + A/\sqrt{2} \), to produce two 25% duty cycle square waves. Because the temporal relation between two square waves is \( T_{OX}/4 \), they can be XORed to form a 50% duty cycle 2X clock whose frequency is the double the XO frequency. Because directly generated from the XO signal, both rising and falling edges of the 2X clock are low noise. And then, they are used to generate 4X clock by a conventional XOR-plus-delay based frequency doubler after an inverter buffer. Although the falling edges of the 4X clock are corrupted by the delay \( \tau \), the rising edges are low jitter and can be used as a clean reference for edge-triggered systems.

3.2. The Single-Ended Xo Based Quadrupler Scheme

Instead of adjusting the threshold voltages of the inverters, the single-ended XO based quadrupler with constant threshold inverters is proposed in [3], as illustrated in Figure 3. The XO output is AC coupled separately to inputs of the two inverters with constant threshold voltages VCM. By adjusting
the common levels of the sinusoids at the inputs of the inverters, it extracts the 25% duty cycle square waveforms from them. And then, the two 25% duty cycle square waveforms are XNORed to generate the double XO frequency signal V3 with 50% duty cycle. Both the rising and falling edges of the V3 are utilized to generate quadruple XO frequency signal V4 by a conventional XOR-plus-delay based frequency doubler. A background calibration unit based on the least-mean-square (LMS) algorithm is used to adjust the common levels of the sinusoid and fine tuning digital-controlled delay line DCDLCAL to minimize the duty cycle errors.

3.3. The Three-point Calibration Quadrupler Scheme

![Diagram of the three-point calibration quadrupler](image)

**Figure 4.** The three-point calibration quadrupler: (a) the architecture, (b) the principle.

Different from the two schemes described above which extract 25% duty cycle square waveforms from XO output sinusoid, the three-point calibration quadrupler presented in [12] firstly converts the XO output sinusoid to two complementary 50% duty cycle square waveforms by the DCC unit. And then, they go through a 2-to-1 multiplexer gate controlled by the signal SEL to generate the double frequency signal g(t) with 50% duty cycle. The signal g(t) can be utilized to generate the quadruple frequency signal y(t) by a conventional XOR-plus-delay based frequency doubler. The y(t) is compared with the output x(t) of the calibration phase-locked loop (PLL) CalPLL by a bang-band phase detector (BBPD) to minimize the duty cycle errors.

4. Comparisons

|                            | Differential XO [11] | Single-ended XO [3] | Three-point calibration [12] |
|-----------------------------|----------------------|----------------------|-----------------------------|
| Technology [nm]             | 28                   | 65                   | 28                          |
| Supply Voltage [V]          | 1.0                  | 1.0                  | N/R                         |
| XO Architecture             | Differential @48MHz  | Single-ended @54MHz  | Single-ended @40MHz         |
| Current [mA]                | 5.5 (XO: 1.5)        | 1.45(XO: 0.2)        | N/R                         |
| Double Clock Phase noise [dBc/Hz] | -139.8@10KHz         | -141.8@10KHz         | N/R                         |
|                            | 148.3@100KHz         | 154.1@100KHz         | N/R                         |
|                            | -151.9@1MHz          | -158.8@1MHz          | N/R                         |
| Double Clock Jitter [fs rms] | 184 [10k-10MHz]      | 77 [10k-10MHz]       | N/R                         |
| Self-Calibration            | Yes                  | No                   | Yes                         |

N/R refers to not reported
The performance comparisons are listed in Table 1. The differential XO based quadrupler uses the High VT and Zero VT transistors, makes it be not effective for all processes. The single-ended XO based quadrupler features low power, low noise, and low jitters. But the calibration method is complicated makes the quadrupler be not self-calibration. The three-point calibration quadrupler does not provide more detail information by the authors. However, it needs a calibration PLL CalPLL to calibrate the duty cycle errors, makes the design complex.

5. Summary
This paper analyses the principle of the three emerged quadruplers, compares performances among them, and gives their advantages and drawbacks.

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