SoftNeuro: Fast Deep Inference using Multi-platform Optimization

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Abstract—Faster inference of deep learning models is highly demanded on edge devices and even servers, for both financial and environmental reasons. To address this issue, we propose SoftNeuro, a novel, high-performance inference framework with efficient performance tuning. The key idea is to separate algorithmic routines from network layers. Our framework maximizes the inference performance by profiling various routines for each layer and selecting the fastest path. To efficiently find the best path, we propose a routine-selection algorithm based on dynamic programming. Experiments show that the proposed framework achieves both fast inference and efficient tuning.

Index Terms—SoftNeuro, Inference engine, deep learning, optimization

I. INTRODUCTION

Deep neural networks (DNNs) have shown remarkable accuracy improvement in various domains, including computer vision, speech recognition, and natural language processing. In the field of computer vision, models based on convolutional neural networks (CNNs) have produced state-of-the-art results in object recognition, detection, and segmentation [19], [21], [35]. Text generation and translation using the transformer mechanism are also attracting attention in natural language processing [4]. More and more real-world applications have come to take advantage of these technologies.

DNN models can be trained by well-known frameworks such as PyTorch [24], TensorFlow [1], and MXNet [6]. These frameworks achieve efficient training by taking advantage of well-optimized libraries. However, those libraries are only tuned for a narrow range of environments with sufficient resources such as GPUs. These frameworks will not run as well on edge devices, such as smartphones, AR/VR devices, and industrial equipment, or even less powerful servers, due to limited computational resources and memory. Improving computational capability is often prohibitively expensive or impractical, be it from material costs, thermal issues, or even power consumption related costs or environment-friendliness. Inference optimization is thus an important task; with sufficiently fast inference, those devices can be used practically, without additional computation capability.

With the above motivation, several inference focused libraries have been released for fast inference on edge devices. TensorFlow Lite [13] and PyTorch Mobile [11] are representative examples of such toolsets, and efficiently perform inference of models trained by the aforementioned frameworks. These toolsets maximize performance by carefully tuning operations for each device and optimizing models with well-known techniques such as quantization and pruning. Meanwhile, hardware vendors have also released inference engines such as OpenVINO [9], TensorRT [23], and SNPE [26]. These engines would be most effective when the deployment target hardware is predetermined, as each vendor optimizes for their own hardware. Furthermore, although these inference libraries are successful in optimizing individual operations of DNNs, they do not provide sufficient optimization at the graph level.

Another framework, named TVM [7], optimizes inference on various devices by appropriately scheduling operations. AutoTVM [8] has also been proposed to tune parameters using machine learning. However, the search space is limited to a small part of the many possible scheduling combinations, often making optimization insufficient. Moreover, its tuning is quite time-consuming, as shown in our experiments.

In this paper, we address the aforementioned issues by introducing a framework that enables efficient tuning over large search spaces at the graph level. The framework performs fast inference of deep learning models trained by the learning frameworks on a wide range of platforms, including CPUs, GPUs, and DSPs. The main idea behind efficient tuning is separating algorithmic routines from network layers of DNN models (Section III).

Our framework maximizes inference performance by using actual execution measurements on target devices. This optimization takes into account multiple aspects: target deployment devices (e.g., CPUs, GPUs, and DSPs), data types (e.g., float32, float16, and qint8), data layout (e.g., channels-last and channels-first), and algorithms used (e.g., direct, Winograd, and sparse). Since a naive algorithm to find the best routines at the graph level may hit combinatorial explosions, we propose an optimization algorithm based on dynamic programming (Section IV).

Experiments in Section V show that our framework is as much as 3 times faster than other inference frameworks on a Galaxy S8 smartphone equipped with a Snapdragon 835 SOC. In addition, the tuning of our framework can be 500 times faster than that of TVM for the VGG16 model [29].
II. RELATED WORK

We review related work from the viewpoint of accelerating the convolution operation because it occupies considerable inference time, making its efficient calculation essential [20]. There are two important factors towards accelerating convolutions’ computation [2]: (1) how computations are performed (algorithms) and (2) how computations are divided and in which order they are executed (scheduling). Scheduling optimization is described in Section II-A and algorithmic improvements are summarized in Sections II-B and II-C.

A. Automatic Scheduling

Most inference frameworks simply select computation methods based on some heuristics [15], [16]. Other frameworks such as Halide [27] and TVM [7] optimize scheduling independently of employed algorithms. Halide [27] uses a genetic algorithm to search for an approximate optimal schedule solution. In [2], improvements to Halide are proposed by enabling larger search spaces of schedules and employing a tree search algorithm based on beam search. TVM [7] separates hardware intrinsics from algorithms and scheduling, supporting unseen devices. To optimize scheduling, they predict running times of schedules with machine learning models based on XGBoost [3] by using features such as access to various memories.

While the above methods can optimize model inference as a whole, the number of scheduling combinations is quite large and expensive to search, so limiting the scheduling space and improving search efficiency are still important issues. We address these issues by introducing the concepts of routines and layers with an efficient optimization algorithm based on profiling.

B. Winograd Algorithm

Winograd’s minimal filtering [33] was originally proposed as a method to minimize the number of multiplications during convolution in the context of digital signal processing. Nevertheless, it can also be extended to convolution in CNNs [18], and is implemented by various inference frameworks. The Winograd algorithm simultaneously calculates convolution over tiles for a specific tile size, but the optimal tile size needs to be properly chosen for the best performance. Some inference frameworks estimate the appropriate tile size based on input characteristics such as data sizes [16]. We address this issue by measuring the performance with multiple tile sizes and selecting the best setting.

C. Quantization

Quantization of weights and activations is another common technique to reduce the model size and computational cost of DNNs [30]. Quantization expresses values (e.g., 32-bit floating point number) at a lower-precision (e.g., 8-bit) integer and a small number of parameters. Some training frameworks such as TensorFlow [1] have introduced a quantization-aware training mechanism to improve accuracy [17]. In addition, inference engines such as TensorFlow Lite [13], PyTorch Mobile [11], and NVIDIA TensorRT [23] support 8-bit integer quantization. SoftNeuro also implements quantization-based routines to accelerate convolutions, as well as other computations.

III. FRAMEWORK FEATURES

This section gives an overview of SoftNeuro features: how deep learning models are deployed in SoftNeuro (Section III-A), how it represents deep learning models (Section III-B), and how it optimizes model execution on various platforms (Section III-C). It also introduces childnets, structures that facilitate the implementation of additional, high-performance routines by reusing existing ones (Section III-D).

A. Model Deployment

A DNN model can be deployed with SoftNeuro in three major steps: (1) Import a DNN model trained by popular deep learning frameworks, converting it into SoftNeuro’s dnn format. (2) Tune the model to maximize the inference speed on the target platform. (3) Perform inference using the tuned model. A brief description of the main components (importers, profiler, and optimizer) needed for deployment follows. Importers are responsible for two tasks: (1) Convert a given DNN model into SoftNeuro’s format, and (2) Optimize the computational graph of the model. Importers currently support conversion from TensorFlow [1] and ONNX 1 (which in turn supports Caffe2 [10], Chainer [31], Microsoft Cognitive Toolkit [34], MXNet [6], PyTorch [24], and PaddlePaddle [3]). When converting a model, importers automatically optimize the model’s computational graph. For instance, ReLU activation and batch normalization layers are fused into their previous layers, reducing computational cost without affecting accuracy.

The profiler and optimizer tune models to run on a given target platform as fast as possible. To this end, SoftNeuro separately considers layers and routines. Layers are an abstract concept that define only what kind of computation should be performed (e.g., ReLU and 2D convolution). On the other hand, routines are actual implementations of layer computations optimized for various hardware platforms (e.g., Intel CPUs, NVIDIA GPUs) and data types (e.g., float32, qint8). A dnn model can be regarded as a graph of layers, and tuning is accomplished by selecting each layer’s fastest routine. For tuning, the profiler measures the processing times of available routines for each layer, and by using the profiling data, the optimizer selects the best routines for layers. Further details can be read in Sections III-B and III-C.

B. Model Representation

A dnn model consists of a net, a directed acyclic graph (DAG) of layers. Nodes of the graph are layers, and edges represent computational dependencies between layers. A net handles input in the first layer, and the net output is obtained from the last layer. Other layers between input and output perform computations to calculate the final output.

1https://onnx.ai/
A layer is an abstract structure that takes one or more n-dimensional tensors, or blobs, performs some computations, and outputs the resulting blob. Every layer has a type, which defines what kind of computation should be performed. For instance, a layer of the conv2 type takes an input blob, carries out 2D convolution with a layer-specific kernel and bias, and outputs the convolution result.

Layers contain two kinds of attributes, namely layer parameters and weights. Layer parameters specify how to execute the layer type’s computation, and weights are trained specific to the layer. For instance, layer parameters of a conv2 layer include dilations, strides, and padding, while the weights would be the kernel and bias.

C. Routines and Profiling

Routines are concrete implementations of layers, and many implementations can exist in SoftNeuro for each layer. To discriminate routines, we introduce routine descriptors. A descriptor specifies the platform, algorithm, and data type each routine was made for. For instance, the \texttt{cuda:float16/cudnn} routine for a conv2 layer uses the cuDNN library \cite{cuDNN} to perform 2D convolution in half-precision on a compatible GPU.

The part before the slash (\texttt{cuda:float16} in the example) is called routine schema. It defines a routine’s platform and data type. If schemas are different between routines of two adjacent layers, the data format or data location must be changed appropriately. For instance, if a layer has a cpu routine and the next layer has a cuda routine, data must be transferred to a GPU before computing the second layer. To this end, SoftNeuro automatically inserts an adapt layer between such two layers. Adapt layers handle three kinds of jobs: (1) data transfer between heterogeneous devices, (2) casting data types, and (3) changing data layout.

Given there are multiple routines, we need to select each layer’s best routine when deploying models. However, each routine’s performance heavily depends on its algorithm and various characteristics of the target platform (e.g., cache structures). Thus, it is practically impossible to determine in advance the best combination of routines for all possible platforms. We address this issue by profiling available routines first, and then selecting the best-performing routine.

To accommodate diverse characteristics of multiple devices, we add routine parameters to each routine. Routine parameters specify values of internal variables used in routines. For instance, the \texttt{cpu/wgc64_avx} routine\footnote{A conv2 routine that utilizes AVX for computation.} has two routine parameters: cache size and task granularity. Each parameter is a list of integers, and the profiler considers all of the possible combinations of the parameters, thereby enabling SoftNeuro to select the best performing routines on many kinds of devices.

Actual profiling is divided into two steps: (1) unit profiling, which profiles routines in a layer-by-layer fashion, and (2) integrated profiling, which considers all of a net’s routines as a whole. This division aims to reduce the computational cost of integrated profiling. Ideally we would perform integrated profiling from scratch, but the search space for a whole net can be combinatorially large. On the other hand, performing only unit profiling can be an alternative strategy, but it is insufficient due to possible differing performance between unit and integrated cases, mainly due to cache behavior. Therefore we opt for using unit profiling to filter out unpromising routine patterns, reducing the combinations for integrated profiling. Specifically, our current implementation selects routine patterns performing better in unit profiling so that the number of patterns in integrated profiling is judiciously limited to a searchable amount.

D. Childnet

We introduce a mechanism called childnet, which enables us to implement a new routine by reusing existing ones, for the following two objectives: (1) to facilitate the implementation of additional routines, and (2) to allow for efficient profiling. In the following, we describe how childnets achieve the objectives by using Figure 1 as examples.

In Figure 1(a), we demonstrate that childnets can easily implement a dense routine. Three sub-layers compose the routine: reshape, conv2, and reshape. The first reshape layer changes the input shape from $C$ to $1 \times 1 \times C$. The conv2 layer uses the reshaped blob for 2D convolution with a kernel of shape $1 \times 1 \times C \times K$. The result of convolution is reshaped from $1 \times 1 \times K$ to $K$ in the last layer. In this way, a new, efficient routine can be easily constructed by combining existing routines.

In addition, childnets allow for efficient profiling of specific routines by exploiting the integrated-profiling mechanism. An example of such routines is a Winograd routine for 2D convolution. A naive implementation of the routine without childnet contains four kinds of routine parameters. In this case, profiling needs to be performed for all combinations of routine parameters. On the other hand, a Winograd routine can also be implemented using the childnet mechanism as shown in Figure 1(b). This Winograd routine consists of three sub-layers: wgenc, wgcov, and wgdec. Each routine of these layers has only a single routine parameter, and the Winograd routine itself also has a routine parameter. In this case, we can reduce the number of patterns to be profiled with the filtering mechanism of integrated profiling, thereby achieving efficient profiling.

IV. Algorithm for Performance Optimization

In this section, we describe the proposed algorithm for performance optimization of routines using the profiling results. If we could assume only a single routine schema, it would be sufficient to use a simple algorithm that selects each layer’s fastest routine. However, the difficulty arises when we handle multiple schemas with adapt layers, because we also need to incur the cost of adaptation performed by the adapt layers (e.g., data format conversion). Such tuning scenarios are called hybrid tuning in this paper, and our algorithm for hybrid tuning
is named **dynamic programming for routine selection**, or **DPRS** for short.

In the following, we first give basic notations and definitions in Section IV-A. Then Sections IV-B-IV-E explain the algorithm from the simplest case to gradually complex cases. Section IV-F summarizes the algorithm workflow by describing its pseudo-code.

### A. Notations and Definitions

Our algorithm’s objective is to select the best routine for each layer, given a net, a set of routine schemas, and profiling data. To formulate the problem, we begin with a formal definition of nets.

A net is a DAG with one input and one output (**1-in-1-out net**) consisting of *n* layers. The layers are denoted as $L_1, \ldots, L_n$ in topological order, where $L_1$ is the input layer and $L_n$ is the output layer. Each layer $L_i$ has a set $R_i$ of routines. A set $R_i(\lambda)$ is the subset of $R_i$ that contains the routines with schema $\lambda$. We define the fastest routine $F_i(\lambda)$ within $R_i(\lambda)$ as

$$F_i(\lambda) \equiv \arg \min_{r \in R_i(\lambda)} T(r),$$

(1)

where $T(r)$ is the execution time of routine $r$ measured by profiling.

Given these notations, we provide the definition of **routine path** as follows.

**Definition 1 (Routine path).** A routine path $S$ is a possible set of routine combinations for a given net. It consists of each layer’s routine as $S = \{r_i \in R_i \mid 1 \leq i \leq n\}$. When the edge $(L_i, L_j)$ exists in the net and their routines ($r_i$ and $r_j$) have different schemas, the adapt routine $r_{i,j}^\alpha$ is also included in the set $S$.

Based on this definition, we define the **optimal routine path**, which is the desired result for hybrid tuning.

**Definition 2 (Optimal routine path).** The optimal routine path $S^*$ is the path with the minimum overall processing time among all routine paths for a net. In other words, it is the solution of the following combinatorial optimization:

$$S^* = \arg \min_S T(S),$$

(2)

where $T(S) = \sum_{r \in S} T(r)$ for routine path $S$.

### B. Straight Net

We first consider the simplest case illustrated as the net A in Figure 2 over the routine schemas $\Lambda = \{\alpha, \beta\}$. In this case, the size of search space for $S^*$ is $O(2^n)$ because we have two options (i.e., $\alpha$ and $\beta$ routines) for each of $n$ layers. To reduce the computational complexity to $O(n)$, we employ a simple dynamic-programming approach, formulated as the following recurrence relation:

$$S_i(\alpha) = \{ F_i(\alpha) \} \cup \text{fastest} \left\{ S_{i-1}(\beta) \cup \{ F_{i-1}^a(\beta \rightarrow \alpha) \} \right\},$$

(3)

where $F_{i,j}^a(\beta \rightarrow \alpha)$ denotes the fastest adapt routine for layer $i$ to layer $j$, and at $i = 1$, $S_1(\lambda) = \{ F_1(\lambda) \}$ for $\lambda \in \Lambda$. The fastest construct is an operation that takes routine paths and finds the fastest path.

The relation means that the optimal routine subpath at layer $i$ can be obtained by selecting the fastest routine for layer $i$ and computing the optimal routine subpath at layer $i - 1$. The latter is either $S_{i-1}(\alpha)$ or $S_{i-1}(\beta)$ with an adapt routine, because we need to include the adaptation cost when schemas change. While the above relation is for schema $\alpha$, a similar relation for schema $\beta$ also holds. By using the relations, we can show the following proposition.

**Proposition 1 (Optimality of DP).** The routine path $S = \text{fastest}_{\lambda \in \Lambda} S_n(\lambda)$ is optimal.

**Proof.** It is shown by induction that for any $i$, $S_i(\lambda)$ is the optimal routine subpath of $L_1, \ldots, L_i$, where routine $r_i$ has schema $\lambda$. This induction is clear from the equation.

### C. Branching Net

We then examine networks where a layer output is branched into two layers, as shown in Figure 2’s net B. By extending the idea for the straight case, we can calculate the optimal routine subpath $S_5(\lambda_5)$ at layer 5 as the union of $S_3(\lambda_3)$ and $S_4(\lambda_4)$ with adapt routines connecting layers 3 and 4 to layer 5. However, this computation requires that schemas for layer 1 in $S_3(\lambda_3)$ and $S_4(\lambda_4)$ are identical; otherwise $S_5(\lambda_5)$ may have two routines for layer 1 and is invalid. To handle such cases, we modify the definition of $S_i(\lambda)$ to include a constraint $C_i$ as $S_i(\lambda; C_i)$. For example, $S_5(\lambda; \lambda_1 = \alpha)$ means that the routine for layer 1 must have schema $\alpha$.

With this extension, the optimal routine subpath at layer 5 can be obtained incrementally by the following equation:

$$S_5(\alpha; \lambda_1 = \alpha) = \{ F_2(\alpha) \} \cup \text{fastest} \left\{ S_3(\alpha; \lambda_1 = \alpha) \cup S_4(\alpha; \lambda_1 = \alpha) \right\},$$

$$S_5(\beta; \lambda_1 = \alpha) \cup \{ F_{3,5}^a(\beta \rightarrow \alpha) \} \cup S_4(\alpha; \lambda_1 = \alpha),$$

$$S_5(\beta; \lambda_1 = \alpha) \cup \{ F_{3,5}^a(\beta \rightarrow \alpha) \} \cup S_4(\beta; \lambda_1 = \alpha) \cup \{ F_{4,5}^a(\beta \rightarrow \alpha) \},$$

(4)

The fastest term considers union of the optimal routine subpaths at layers 3 and 4 (i.e., $S_3$ and $S_4$). For each subpath, there are two candidates depending on the selected schema, as in the straight case. Thus the fastest term evaluates the four
candidates in total. Similar relations for $S_5$ exist for different combinations of the schema and constraint.

More generally, the constraint can be regarded as an element of the $m$th Cartesian power of routine schemas $\Lambda$ when there are $m$ constraint layers. The $m$th Cartesian power of $\Lambda$ is

$$\Lambda^m = \Lambda \times \cdots \times \Lambda.$$ \hfill (5)

When we let $A = \{a_1, \ldots, a_m\}$ be a set of indices of $m$ constrained layers, a tuple $\lambda_A = (\lambda_{a_1}, \ldots, \lambda_{a_m}) \in \Lambda^m$ represents a combination of schema constraints for the layers. When $\lambda_A$ is in the constraint, the fastest routine for layer $j$ with schema $\lambda_j$, $F_j(\lambda_j)$, must be included in the constrained optimal routine path, $S_j(\lambda_j; \lambda_A)$. Based on this notation, we can show the following proposition.

**Proposition 2** (Optimality of constrained DP). The routine path $\hat{S}$ obtained by the constrained optimal routine subpath as follows is optimal.

$$\hat{S} = \text{fastest}_{\lambda_A} S_N(\lambda; \lambda_{C_n}).$$ \hfill (6)

*Proof.* Derived by the definition of constrained DP variables and generalizing the recurrence formula (Equation 4) in merging branches.

**D. Multi-branching Net**

Now we inspect networks with multiple branches illustrated by the net $C$ in Figure 2. As a naive extension, we could apply the idea for branching nets by constraining each branch. For instance, layers 1 and 2 need to be constrained in the example. In this case, we need to evaluate eight patterns in total to compute the optimal routine subpaths of layers at the downstream of layer 2 (i.e., layers 3, 4, 5, and 8), because the unconstrained layers also have two schema options. In short, a naive extension of the branching case results in $2^b$ combinations of schemas for nets with $b$ branches.

To alleviate this cost, we relax the constraint when merging branches. For example, when merging the subpaths of layers 5 and 7 for layer 8, the necessary constraint is only the schema of layer 1. This is because the constraint on layer 2 must be already satisfied at layer 5, when merging layers 3 and 4. Thus, the constraint on layer 2 can be relaxed at layer 5 as follows:

$$S_5(\alpha; \lambda_1 = \alpha) = \text{fastest} \left\{ \begin{array}{l} S_5(\alpha; \lambda_1 = \alpha, \lambda_2 = \alpha), \\ S_5(\alpha; \lambda_1 = \alpha, \lambda_2 = \beta). \end{array} \right.$$

In this equation, we remove the constraint of $\lambda_2$ by selecting the faster subpath. Similar relaxation can also be applied for $S_5(\alpha; \lambda_1 = \beta), S_5(\beta; \lambda_1 = \alpha)$, and $S_5(\beta; \lambda_1 = \beta)$. A more general condition for the relaxation is summarized as the following proposition.

**Proposition 3** (Condition for relaxing constraints). Let $A_i$ be a set of layers through which all downstream paths of branching layer $L_i$ pass. The constraint on $L_i$ at $L_j$ can be relaxed if and only if $L_j \in A_i$.

*Proof.* If $L_j \in A_i$, then all downstream paths of $L_i$ go through $L_j$. At the downstream of $L_j$, merging with a constraint on $L_i$ does not occur. Hence we can relax the constraint on $L_j$ in this case.

Conversely, if $L_j \notin A_i$, then there is a path $\rho$ that passes through $L_i$ without travelling $L_j$. Besides, there exists a path $\rho'$ at the downstream of $L_j$ that intersects $\rho$ at $L_k(j < k \leq n)$, because a net has only one output. Since the constraint on $L_i$ is required at the intersecting point, we cannot relax the constraint at $L_j$.

**E. Multi-input, Multi-output Net**

So far, we have explored only 1-in-1-out networks, but networks with multiple inputs and outputs have recently been utilized for tasks such as synthesizing images and multi-task learning [12, 32]. To adapt the above discussion to such cases as well, we introduce auxiliary input and output layers as shown in the net $D$ (Figure 2). The auxiliary input layer connects to all input layers, and the auxiliary output layer merges all output layers. The auxiliary layers have a single routine with zero processing time, so there is no impact on performance optimization.

**F. Algorithm**

Algorithm [1] shows the pseudo-code for hybrid tuning, a generalization of the above discussion. The algorithm receives...
We run inference 20 times per experiment for obtaining the VGG16. This is because it considers not only the inference speed, but also the conversion costs between float32 and qint8 routines. It is of note that float32-only tuning achieved better results than qint8, except for MobileNetV2. This reveals that float32 routines can be faster than qint8 routines in some conditions, in this case, due to Winograd’s efficiency for float32. In fact, qint8 routines were selected for only six layers of VGG16, as shown in Table III. Specifically, the qint8 routines are used for block5 pooling, block5 pooling, flatten, fc1, fc2, and fc3. Note

### V. Experiments

We evaluate inference performance on the VGG16 [29], ResNet50 [14], MobileNetV2 [28] and MobileNetV3 [15] models, which are commonly used for classification or as backbones for other tasks. Inference performance was measured on a Samsung Galaxy S8 containing a Snapdragon 835 SOC [28]. We run inference 20 times per experiment for obtaining the averages and standard deviations. We also compare the tuning and inference speeds of SoftNeuro with those of TVM.

#### A. Hybrid Tuning Performance

We compare the inference speeds of four cases: (1) without tuning, (2) tuning only for float32 routines, (3) tuning only for qint8 routines, and (4) hybrid tuning of float32 and qint8. The result is summarized in Table II.

Hybrid tuning achieves the best result for all tested models, by as much as 9.6% compared to float32-only tuning on VGG16. This is because it considers not only the inference speed of each routine, but also the conversion costs between float32 and qint8, allowing for the optimal combination of float32 and qint8 routines. It is of note that float32-only tuning achieved better results than qint8, except for MobileNetV2. This reveals that float32 routines can be faster than qint8 routines in some conditions, in this case, due to Winograd’s efficiency for float32. In fact, qint8 routines were selected for only six layers of VGG16, as shown in Table III. Specifically, the qint8 routines are used for block5 pooling, block5 pooling, flatten, fc1, fc2, and fc3. Note

### Table I

| Network     | float32 (w/o tune) | float32 | qint8  | hybrid      |
|-------------|--------------------|---------|--------|-------------|
| VGG16       | 458.442 (±16.904)  | 219.603 (±0.963) | 372.658 (±1.251) | 198.453 (±3.758) |
| ResNet50    | 128.698 (±0.871)   | 152.172 (±0.766) | 14.931 (±0.019)  | 102.544 (±1.373) |
| MobileNetV2 | 25.730 (±0.639)    | 55.653 (±0.031)  | 14.931 (±0.019)  | 198.453 (±3.758) |
| MobileNetV3 | 7.479 (±0.036)     | 5.695 (±0.066)   |        |             |

### Table II

| Network     | TensorFlow Lite | PyTorch Mobile | Ours       |
|-------------|-----------------|---------------|------------|
| VGG16       | 403.062 (±12.053) | N/A           | 198.453 (±3.758) |
| ResNet50    | 128.698 (±0.871) | 102.544 (±1.373) |             |
| MobileNetV2 | 25.730 (±0.639) | 14.931 (±0.019) |             |
| MobileNetV3 | 7.479 (±0.036)  | 5.695 (±0.066)  |             |

### Table III

| Layer       | Routine Descriptor | Routine Parameters |
|-------------|--------------------|--------------------|
| block1 conv1 | cpu/owc32_neon     | cache:8192 task_ops:32768 |
| block1 conv2 | cpu/wg2            | tile_size:4        |
| block1 pool  | cpu/neon           | tile_size:8        |
| block2 conv1 | cpu/wg2            | tile_size:6        |
| block2 conv2 | cpu/wg2            | tile_size:8        |
| block2 pool  | cpu/neon           | tile_size:8        |
| block3 conv1 | cpu/wg2            | tile_size:8        |
| block3 conv2 | cpu/wg2            | tile_size:8        |
| block3 conv3 | cpu/wg2            | tile_size:8        |
| block3 pool  | cpu/qint8/ neon    | tile_size:6        |
| block4 conv1 | cpu/wg2            | tile_size:6        |
| block4 conv2 | cpu/wg2            | tile_size:6        |
| block4 conv3 | cpu/wg2            | tile_size:6        |
| block4 pool  | cpu/qint8/ neon    | tile_size:6        |
| flatten      | cpu/qint8          |                    |
| fc1          | cpu/qint8          |                    |
| fc2          | cpu/qint8          |                    |
| fc3          | cpu/qint8          |                    |
| softmax      | cpu/naive          |                    |
Algo. 1 DPRS for Hybrid Tuning

1: **Input:** 1-in-1-out set \( \{L_i\} \), Layer-wise optimal routines \( \{F_i^i\} \), \( \{F_{i,j}^n\} \), Routine schema set \( \Lambda \)

2: **Output:** Optimal routine path \( S^* \)

3: \( C_0 \leftarrow \emptyset \)

4: for \( \lambda \in \Lambda \) do

5: \( S_0(\lambda; \emptyset) \leftarrow \emptyset \)

6: end for

7: for \( i \) in 1, ... , \( N \) do

8: \( H \leftarrow \text{Indices of layers directly connected to } L_i \)

9: \( C_i \leftarrow C_h \text{ from one of } h \in H \text{ (All } C_h \text{ are equal)} \)

10: for \( \lambda \in \Lambda \) do

11: for \( \lambda_{C_i} \in \Lambda_{\mid C_i\mid} \) do

12: \( S_i(\lambda; \lambda_{C_i}) \leftarrow \{F_i(\lambda)\} \cup \left\{ \text{fastest } \lambda_j \in \Lambda_{\mid H\mid} \mid j \in H \right\} \)

13: end for

14: end for

15: if \( L_i \) is a merging layer then

16: \( K \leftarrow \text{Subset of } C_i \text{ to be relaxed at } L_i \)

17: \( C_i \leftarrow C_i \cup K \)

18: for \( \lambda \in \Lambda \) do

19: for \( \lambda_{C_i} \in \Lambda_{\mid C_i\mid} \) do

20: \( S_i(\lambda; \lambda_{C_i}) \leftarrow \text{fastest } S_i(\lambda; \lambda_{C_i}, \lambda_K) \)

21: end for

22: end for

23: end if

24: if \( L_i \) is a branching layer then

25: for \( \lambda \in \Lambda \) do

26: for \( \lambda_{C_i} \in \Lambda_{\mid C_i\mid} \) do

27: \( S_i(\lambda; \lambda_{C_i}, \lambda_i = \lambda) \leftarrow S_i(\lambda; \lambda_{C_i}) \)

28: end for

29: end for

30: \( C_i \leftarrow C_i \cup \{i\} \)

31: end if

32: end for

33: \( S^* \leftarrow \text{fastest } S_N(\lambda; \emptyset) \)


that block4 pooling is situated between float32 routines. Such routine selection is enabled by hybrid tuning; the tuning algorithm determines that the qint8 routine is faster than float32 routines even if quantization and dequantization need to be performed.

### B. Comparison with Other Frameworks

We compare SoftNeuro inference speeds with two inference frameworks: TensorFlow Lite (ver. r2.4) and PyTorch Mobile (ver. 1.7.1). Table IV shows the result of experiments. PyTorch Mobile does not have readily available VGG16 and MobileNetV3 models, so these were not measured. For a fair comparison with hybrid tuning, quantized models were used in TensorFlow Lite and PyTorch Mobile.

SoftNeuro outperforms TensorFlow Lite and PyTorch Mobile for all models. Notably, SoftNeuro is more than 2 times faster than TensorFlow Lite on VGG16. Compared with PyTorch Mobile, SoftNeuro is more than 3 times faster on MobileNetV2.

### C. Tuning Speed

We measured the tuning and inference speeds for VGG16 and ResNet50 using TVM and SoftNeuro on an Intel Xeon Gold 6126 CPU (Table IV). TVM was set to quantize models to 8-bit and tune with 2,000 trials per operation, matching the configuration used in the TVM paper [7]. SoftNeuro shows more than an order of magnitude faster tuning over TVM while also achieving as much as thrice faster inference speeds.

### VI. Conclusions and Future Work

In this paper, we have described a novel, performance-optimized inference framework. The core idea is to separate routines from layers, thereby enabling efficient and flexible performance optimization. The optimization has been formulated as a problem of finding the fastest routine at each layer while taking into account the adaptation cost. To efficiently solve the problem, we have proposed the DPRS algorithm based on dynamic programming. Our experiments show that the proposed framework achieves faster inference and more efficient tuning than other frameworks.

In future we plan to optimize the processing time with restrictions of accuracy and memory usage. SoftNeuro currently considers only processing time when tuning the performance. However, quantization may degrade accuracy beyond acceptable limits. Meanwhile, the Winograd algorithm may consume a large amount of memory due to kernel sizes that increase with tile sizes. Such accuracy degradation and excessive memory consumption should be alleviated in the future.

### References

[1] Abadi, M., Barham, P., Chen, J., Chen, Z., Davis, A., Dean, J., Devin, M., Ghemawat, S., Irving, G., Isard, M., Kudlur, M., Levenberg, J., Monga, R., Moore, S., Murray, D. G., Steiner, B., Tucker, P., Vasudevan, V., Warden, P., Wicke, M., Yu, Y., and Zheng, X. (2016). TensorFlow: A system for large-scale machine learning. In *OSDI*, pp. 265–283.

[2] Adams, A., Ma, K., Anderson, L., Baghdadi, R., Li, T.-M., Gharbi, M., Steiner, B., Johnson, S., Fatahalian, K., Durand, F., and Ragan-Kelley, J. (2019). Learning to optimize halide with tree search and random programs. *ACM Trans. Graph.*, 38(4), Article 121.

[3] Baidu. (2021). PaddlePaddle. Retrieved from https://github.com/PaddlePaddle/Paddle
