Josephson Junction Field-Effect Transistors for Boolean Logic Cryogenic Applications

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Abstract—Josephson junction FETs (JJ-FETs) share design similarities with MOSFETs, except for the source/drain contacts being replaced by superconductors. Similarly, the super current due to proximity effect is tunable by the gate voltage. In light of recent advances in novel materials and fabrication techniques, we examine here the feasibility of JJ-FET-based Boolean logic and memory elements for cryogenic computing. Using a 2-D ballistic transport JJ-FET model, we implement circuit-level simulations for JJ-FET logic gates and discuss criteria for realizing signal restoration, as well as fan-out. We show that the JJ-FET is a promising candidate for very low-power, clocked voltage-level dynamic logic at cryogenic temperatures.

Index Terms—Ballistic transport, Josephson junction (JJ), superconducting logic device.

I. INTRODUCTION

Reducing temperature ($T$) improves several key device metrics of the MOSFETs. Examples include enhanced channel mobility and reduced subthreshold swing (SS), which scales linearly with $T$ as $SS = 2.3 (kT/e)$/decade; $k$ is Boltzmann’s constant and $e$ is the electron charge. Channel injection efficiency can be improved in the absence of phonon scattering [1], and the resistance of metal interconnects is expected to decrease at lower temperatures. It is, therefore, important to investigate under what conditions cryogenic computing provides a net benefit in terms of dissipated energy per switching operation and whether other devices can offer a benefit in performance at reduced temperatures. For a given technology with supply voltage $V_{DD}$, the energy dissipated per switching operation is $CV_{DD}^2/2$, where $C$ represents the device capacitance. Assuming $V_{DD}(T)$ can be reduced at lower $T$, by requiring that the total energy dissipated per switching operation, including the cooling cost, does not exceed the room temperature value, we arrive at the following energy balance equation:

$$\frac{CV_{DD}(300K)^2}{2} = \frac{CV_{DD}(T)^2}{2} + \frac{300K-T}{T} \cdot \frac{CV_{DD}(T)^2}{2}. \quad (1)$$

The second term on the right-hand side (RHS) of (1) represents the cooling cost at the ideal Carnot efficiency, corresponding to reservoir temperatures of 300 K and $T$. Equation (1) leads to the following simple scaling law for the operating voltage to break even in the ideal cooling limit:

$$V_{DD}(T) = V_{DD}(300K) \sqrt{\frac{T}{300K}} \quad (2)$$

For example, a $V_{DD}$ value of 0.7 V at room temperature will translate to a break-even value of 83 mV at 4.2 K, the liquid He boiling point, which is further reduced to ~26 mV if one factors in realistic cooling efficiencies of 5%–10% [2]. The gate delay associated with load and parasitic capacitance being charged/discharged will scale with reducing $V_{DD}$, while the transit time delay of channel being switched may not scale down proportionally because of low Fermi velocity at low carrier concentration and reduced thermal excitation of carriers [3]. While the above arguments contain a number of simplifications, they clearly indicate that cryogenic computing using CMOS concepts is subject to significant constraints if a net benefit is expected over room-temperature operation with cooling cost factored in. It is, therefore, highly relevant to examine if other devices operating at or below the break-even $V_{DD}$ value may be used for cryogenic computing applications.

Josephson-logic devices can operate at $V_{DD}$ values in the millivolt range utilizing superconductivity [4], the most spectacular material property that emerges at low temperatures as a result of electrons forming Cooper pairs. The devices are based on the Josephson junction (JJ), a two-terminal device consisting of two superconductor contacts separated by a weak link, allowing current flow without dissipation (supercurrent) due to proximity effect. The feasibility of JJ-FET, a three-terminal device with gate-tunable supercurrent, for logic operation was discussed decades ago [5], [6]. The JJ-FET design is similar to a MOSFET except that the source and drain are superconducting at cryogenic temperatures, and the channel length is sufficiently short to allow coherent transport of Cooper pairs through the channel. JJ-FETs have been experimentally demonstrated on various material platforms, including Si, Ge, and III–V compounds [7]–[9]. Advances in
Depending on the interplay between the development of transparent semiconductor/superconductor as nanowires, III–V quantum-wells, and graphene, as well as fabrication techniques and emerging channel materials, such as nanowires, III–V quantum-wells, and graphene, as well as the development of transparent semiconductor/superconductor interfaces render the topic of JJ-FETs timely [10]–[13].

In this article, we address the feasibility of JJ-FETs for digital applications. We employ a JJ-FET device model that allows gate-controlled ballistic and coherent transport of Cooper pairs through the channel to examine the criteria for signal restoration of several logic gates. We present the results of transient analysis of JJ-FET logic gates, evaluate the impact of fan-out on device behavior, and discuss various design considerations.

II. JJ-FET DEVICE MODEL

We begin by introducing a device model for the JJ-FET. The device, schematically shown in Fig. 1, has the following key length scales: the channel length (L), the Cooper pair coherence length (ξ0), and Cooper pair mean free path (λ). Depending on the interplay between L, ξ0, and λ, the JJ can operate in either short or long ballistic or diffusive regimes. The JJ is short if L < ξ0 or long if L > ξ0. The Cooper pair transport is ballistic if L < λ or diffusive if L > λ.

Here, we consider the case of a short ballistic JJ device, which satisfies the Ambegaokar–Baratoff formula [14]

$$V_0 = I_C \cdot R_N = \pi \Delta$$

where $I_C$ is the critical current, $R_N$ is the normal resistance of the JJ, and Δ is half the superconductor gap voltage. The conductance of a 2-D ballistic transport layer, divided by the average velocity along the channel direction, is

$$g_n = \frac{2}{h} \cdot \frac{2}{\pi} \cdot \sqrt{2\pi n}$$

where W is the device width, h is the Planck constant, and n is the carrier density. The carrier density can be related to gate capacitance ($C_G$) and gate voltage ($V_G$) via $n = C_G(V_G - V_T)/e$; $V_T$ is the threshold voltage. Using (3) and (4)

$$I_C = g_n \cdot V_0 = 2V_0W \cdot \frac{2e}{h} \cdot \sqrt{\frac{2eC_G(V_G - V_T)}{\pi}}.$$  

It is instructive to introduce an equivalent conductance for the $I_C$ dependence on $V_G$ as

$$\beta = \frac{dI_C}{dV_G} = \frac{dg_n}{dV_G} = \frac{V_0W}{V_G} \cdot \frac{2e}{h} \cdot \sqrt{\frac{2eC_G}{\pi(V_G - V_T)}.}$$

If we assume the device is in the overdamped limit, where $I$–$V$ characteristics are nonhysteretic [15], [16], the static $I$–$V$ characteristics are relatively simple

$$V_{DS} = R_N \sqrt{I_{DS}^2 - I_C^2} \quad (I_{DS} > I_C)$$

$$V_{DS} = 0 \quad (I_{DS} < I_C)$$

where $V_{DS}$ is the voltage drop across the drain and source contacts and $I_{DS}$ is the drain current. Because Nb and Al are two commonly used superconductors [17], [18], we consider here the cases where the source/drains consist of either Nb or Al with Δ values of 1.5 or 0.22 mV, respectively [19]. Fig. 2 shows the static $I$–$V$ characteristics of JJ-FETs with the two metal contacts.

A critical question for a logic gate is if the output voltage is sufficiently large to switch the next stage. To address this question let us assume the output of one JJ-FET is directly driving the gate of a second JJ-FET, whose $I_C$ value, in turn, needs to be sufficiently modulated for a switch. Equation (7) indicates that $V_{DS}$ will be of the order of $V_0$ if $I_{DS}$ is comparable to $I_C$ [4]. The relative change in $I_C$ corresponding to a gate swing of $V_0$ is [20]

$$\alpha_R = \frac{\beta V_0}{I_C} = \frac{V_0}{2(V_G - V_T)}.$$  

To achieve signal restoration $\alpha_R \sim 1$, hence $V_G - V_T$ needs to be comparable to $V_0$. This is an intrinsic requirement of JJ-FET logic gate, independent of device scaling and geometry. Fig. 3 shows the plots of $\alpha_R$ against $V_G - V_T$ for both Nb- and Al-contact JJ-FETs.
output swing, namely $V_{\text{back}}$ yields an SRAM cell [see Fig. 4(c)], where and investigate its performance, ignoring any parasitic capacitance will reach a stable state of complementary values. and zero otherwise. Connecting two JJ-FET inverters back to output swing. Similarly, in a JJ-FET NOR gate [see Fig. 4(b)], the finite $V_{\text{OUT}}$ when both inputs are at logic low, leading to $V_{\text{OUT}}$ and $V_{\text{OUT}}$ is zero. Consequently, we have $V_{\text{OUT}} = 0$ since the JJ-FETs are cascaded in logic circuits. Signal restoration indicates the finite $V_{\text{OUT}}$ at $V_{\text{IN}} = V_{G,\text{Lo}}$ at least equal to $V_{G,\text{Hi}}$ to drive the input of the next stage, i.e., the same input–output swing. Similarly, in a JJ-FET NOR gate [see Fig. 4(b)], the sum of $I_C$ of the two JJ-FETs is smaller than $I_{\text{Bias}}$ only when both inputs are at logic low, leading to a finite $V_{\text{OUT}}$ and zero otherwise. Connecting two JJ-FET inverters back to back yields an SRAM cell [see Fig. 4(c)], where $V_1$ and $V_2$ will reach a stable state of complementary values.

Next, we design the JJ-FET inverter using the static model and investigate its performance, ignoring any parasitic capacitance and resistance of the JJ-FET itself. Though this model may be oversimplified, it sheds lights on the dc operating point, i.e., $V_T$ and $I_{\text{Bias}}$ values will produce the same input–output swing, namely $V_{G,\text{Hi}} = V_{\text{OUT}}(V_{G,\text{Lo}}) = R_S(V_{G,\text{Lo}}) \cdot \sqrt{(I_{\text{Bias}}^2 - I_C^2(V_{G,\text{Lo}}))}$ and optimal power or speed; the variables in parentheses denote the $V_{\text{IN}}$ values. We can estimate the power consumption of the JJ-FET as $\alpha I_{\text{Bias}} V_{G,\text{Hi}}$. Hypothetically, we could have an arbitrarily small swing and thus power consumption by choosing $I_{\text{Bias}}$ close to $I_C(V_{G,\text{Hi}})$. We could also have an arbitrarily large swing since $R_S(V_{G,\text{Lo}})$ diverges when $V_T$ approaches zero. Hence, for any given swing, we have a solution to the bias point by appropriately choosing $V_T$ and $I_{\text{Bias}}$, albeit with tradeoffs. Therefore, we chose to design the bias point of the logic gates based on speed.

The rising delay ($t_r$) is not expected to be reduced compared to that of the traditional counterpart, e.g., an NMOS inverter, because when $V_{\text{IN}}$ switches to low, the JJ-FET becomes resistive instead of being cut off. Moreover, the JJ-FET draws additional current to the resistive component, namely the Josephson current ($I_J$), effectively further slowing down the charging speed at the output node. On the other hand, $I_J$ will assist to discharge the output node when $V_{\text{IN}}$ switches to high. The falling delay ($t_f$) is, therefore, smaller than that of an NMOS inverter, and more importantly, the superconducting JJ-FET can fully discharge the output. Fig. 5(a) presents the plot of minimum total delay $\tau_{\text{min}}$ as a function of $|V_T|$ for an Nb-contact JJ-FET inverter. The device has the same geometry as that assumed in Fig. 2 and an output capacitance $C_L = 10 \text{ fF}$, chosen as fan-out of four plus interconnect capacitance. For reference, the gate capacitance of a JJ-FET with $W = 1 \mu m$ and $L = 50 \text{ nm}$ is 1.7 fF. We note the actual value of $C_L$ is insignificant to demonstrate the logic operation here, since the characteristics of JJ-FET logic gates using the static $I-V$ model will not change with $C_L$, except for the delay to scale linearly. For a fixed $V_T$, a given $I_{\text{Bias}} > I_C(V_{G,\text{Lo}})$ decides $V_{\text{OUT}}(V_{G,\text{Lo}})$ and therefore the output swing. Meanwhile, $I_{\text{Bias}}$ cannot exceed $I_C(V_{\text{OUT}}(V_{G,\text{Lo}}))$ so there is a matched input swing. Hence, we have multiple solutions of various $I_{\text{Bias}}$ to the bias point at each $V_T$. We first determine those quiescent points, then extract $t_f$ and $t_r$ for individual point from transient analysis, and finally obtain $\tau_{\text{min}}$ at that $V_T$ as the minimum of $(t_f + t_r)$ among those points. Effectively, the curve in Fig. 5(a) is the projection of a trace along the contour plot for ($t_r + t_f$) against $V_T$ and $I_{\text{Bias}}$. We find that $\tau_{\text{min}}$ reaches a global minimum at $V_T \approx -0.8 A$, where the $V_{\text{IN}}$ swing is $4 A$. Using this bias point, an example of transient analysis for the Nb-contact JJ-FET inverter is shown in Fig. 5(b). It is clear that the falling edge of $V_{\text{OUT}}$ is more linear than exponential compared with the rising edge thanks to $I_J$, which remains

III. JJ-FET LOGIC GATES

A. Static Analysis

In this section, we consider logic gates based on JJ-FETs. Fig. 4(a)–(c) shows the schematics of the JJ-FET inverter, NOR gate, and static random access memory (SRAM), respectively. A NOR gate is universal and can be the building block for any combinatorial logic circuit. In this article, we assume all logic devices are biased with ideal dc current ($I_{\text{Bias}}$) sources for simplicity. The logic gates operate as follows: For a JJ-FET inverter [see Fig. 4(a)], when the input voltage at the gate ($V_{\text{IN}}$) is at logic low ($V_{G,\text{Lo}}$), the corresponding $I_C < I_{\text{Bias}}$ and the JJ-FET is resistive, leading to a finite output voltage ($V_{\text{OUT}}$). On the other hand, when $V_{\text{IN}}$ is at logic high ($V_{G,\text{Hi}}$), the corresponding $I_C > I_{\text{Bias}}$, the JJ-FET is superconducting, and $V_{\text{OUT}}$ is zero. Consequently, we have $V_{\text{OUT}} = 0$ since the JJ-FETs are cascaded in logic circuits. Signal restoration indicates the finite $V_{\text{OUT}}$ at $V_{\text{IN}} = V_{G,\text{Lo}}$ at least equal to $V_{G,\text{Hi}}$ to drive the input of the next stage, i.e., the same input–output swing. Similarly, in a JJ-FET NOR gate [see Fig. 4(b)], the sum of $I_C$ of the two JJ-FETs is smaller than $I_{\text{Bias}}$ only when both inputs are at logic low, leading to a finite $V_{\text{OUT}}$ and zero otherwise. Connecting two JJ-FET inverters back to back yields an SRAM cell [see Fig. 4(c)], where $V_1$ and $V_2$ will reach a stable state of complementary values.

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\[ I_C \approx I_C \text{ and does not linearly decrease with } V_{OUT} \text{ as the resistive counterpart. The } t_i \text{ and } t_f \text{ values are 6.4 and 2 ps in this case. Similarly, a NOR gate can be constructed by simply doubling } I_{Bias} \text{ since } 2I_{Bias} < I_C(V_{G,H}) + I_C(V_{G,Lo}). \]

Applying the same set of parameters for the Nb-contact JJ-FET inverter in Fig. 5(b), Fig. 6(a) shows the transient response of the output voltages \( V_1 \) and \( V_2 \) for the two JJ-FET inverters in an SRAM cell. The initial voltage values at the two outputs are associated with the metastable state \( (V_1 = V_2 \approx 1.5 \text{ mV}) \). In the presence of any disturbance, which is ubiquitous in an actual circuit, the feedback loop will stabilize the two inverters to their respective conditions. The final state is one of the two stable states, where \( V_1 \) and \( V_2 \) have opposite logic values. In this example, the metastable state ends due to a disturbance at 25 ps and the cell reaches the stable state where \( V_1 = 5.9 \text{ mV} \) and \( V_2 = 0 \text{ mV} \), representing a bit “1” stored in the cell. Other initial conditions will work as if the disturbance is already given. Fig. 6(b) presents the voltage transfer curves of the two JJ-FETs in the same SRAM cell with the static noise margin indicated in a dashed-line box. The intersection of the two curves in the middle indicates the metastable state while the two at the ends represent the stable states pointed by arrows.

**B. Dynamic Analysis**

Although we can design the dc operating point of JJ-FET logic gates with the static model, we have made a critical assumption that the JJ-FETs are overdamped in the transient analysis. If a JJ works in the overdamped regime and carries a current exceeding \( I_C \), it is nonhysteretic and will become superconducting immediately when the current falls below \( I_C \). For an overdamped and resistive JJ-FET, it means the transistor will become superconducting as soon as \( V_G \) is increased such that \( I_C > I_{DS} \). However, a JJ or JJ-FET is overdamped only when the Stewart–McCumber parameter \( Q = 2\pi R^2 C I_C / \Phi_0 \) is small \( (Q \ll 4) \) [15], [16], where \( R \) and \( C \) are the resistance and capacitance across the junction, and \( \Phi_0 \) is the magnetic flux quantum. On the other hand, a JJ becomes underdamped if \( Q \) is large, which means it remains in the resistive state even when the junction current is reduced below \( I_C \), leading to \( I-V \) hysteresis. The assumption of overdamped operation becomes questionable if we acknowledge that a logic device has fan-out, and therefore, has larger \( C \) as well as \( Q \) than a single transistor. Moreover, by ignoring the Josephson inductance \( L_C = h/2e I_C \), the estimation of gate delay is no longer accurate, as the dominant time constant of an overdamped JJ-FET is the Josephson time constant \( \tau_{RL} = L_C/R_N = h/(ne\Delta) \). To address these dilemmas, we implement the resistively and capacitively shunted junction (RCSJ) model to describe the device. The \( I-V \) characteristics are controlled by the time-dependent variable \( \varphi(t) \), which is the macroscopic phase difference of the superconducting contacts

\[
I_{DS}(t) = C \frac{dV_{DS}(t)}{dt} + \frac{V_{DS}(t)}{R} + I_C\sin(\varphi(t))
\]

\[
V_{DS}(t) = \frac{h}{2e} \frac{d\varphi(t)}{dt}
\]

where \( I_C\sin(\varphi(t)) \) represents \( I_I \). We assume the load is purely capacitive and ignore the resistance of the biasing circuitry. Therefore, a JJ-FET inverter’s device resistance \( R = R_N \) and capacitance \( C = C_L + C_J \), where \( C_J \) is the junction capacitance assuming gate capacitance splits symmetrically to the source and drain. The gate-tunable \( \tau \) for a JJ-FET inverter writes

\[
Q_{inv} = \frac{R^2 C I_C}{\Phi_0 / 2\pi} = \frac{x^{3/2} V_0 (C_J + C_L)}{\sqrt{2eC_G(V_{IN} - V_T)}}
\]

where \( C_J \) and \( C_L \) are normalized to \( W = 1 \mu m \) of the active JJ-FET. We have \( C_L \propto C_G \) if the output is driving inputs of other JJ-FETs, and hence, for a JJ-FET logic inverter, \( Q_{inv} \propto (C_G/(V_{G} - V_T))^{1/2} \).

Fig. 7 presents the results of transient analysis for both Nb- and Al-contact JJ-FET inverters with device parameters adapted from the static analysis based on \( V_T \approx -0.8 \Delta \). Fig. 7(a) and (b) shows the input waveforms for the Nb- and Al-contact JJ-FET inverters, respectively. Fig. 7(c) and (d) shows the output waveforms for the Nb- and Al-contact JJ-FET inverters with \( C_L = 1 \text{ fF} \). Similarly, the output waveforms for the Nb- and Al-contact JJ-FET inverters with \( C_L = 5 \text{ fF} \) are shown in Fig. 7(e) and (f). The values of \( C_L \) in the dynamic analysis section are chosen to represent the respective operation regime whether hysteresis will latch the JJ-FET in the resistive state or not. Table I summarizes the values of \( Q \) associated with different \( C_L \) and zero \( V_{IN} \) for both Nb- and Al-contact JJ-FET inverters. Comparing the output waveforms to those using the static model, superimposed oscillations emerge because of the Josephson effect. Similar to a parallel \( RLC \) circuit, the amplitude is attenuated by larger \( C_L \), and the frequency is higher for the Nb-contact device due to smaller \( L_C \). The Nb-contact JJ-FET inverter is significantly faster than its Al-contact counterpart, e.g., \( t_I = 0.25 \) and 2.5 ps, respectively, with \( C_L = 1 \text{ fF} \). The difference in their \( t_I \) is comparable to that of their \( \tau_{RL} \). If we compare Fig. 7(c) and (d) with Fig. 7(e) and (f), a distinct difference that can be seen is that JJ-FET inverters fail to be reset into the superconducting states when \( V_{IN} \) switches from zero to high when \( C_L \) is increased from 1 to 5 fF. Consequently, the finite \( Q \) must be accounted for when designing JJ-FET logic gates to avoid an undefined \( V_{OUT} \). In the simulation, we find
**Table I**

| Contact and \( C_L \) | \( V_{IN} - V_T = 1.2 \text{ mV} \) | \( V_{IN} - V_T = 0.2 \text{ mV} \) |
|----------------------|----------------------|----------------------|
| Nb, 1 fF            | 3.5                  | 1.0                  |
| Nb, 5 fF            | 15.5                 | 4.4                  |
| Al, 1 fF            |                      |                      |
| Al, 5 fF            |                      |                      |

\( Q \approx 4 \) is the critical value for the Nb-contact JJ-FET inverter to be properly reset and slightly lower for the Al-contact device as \( Q \approx 2.5 \). The critical value of \( Q \) is closely related to the ratio of \( \frac{I_{Bias}}{I_C(V_{IN},H)} \) due to the hysteretic \( I-V \) characteristics. This ratio is 0.5 and 0.7 for the parameter set our Nb- and Al-contact JJ-FET inverter assumes, in agreement with the ratio of return current over \( I_C \) corresponding to the critical \( Q \) in a hysteretic JJ [16].

Similarly, we can write \( Q \) for a JJ-FET NOR gate as

\[
Q_{NOR} = \frac{R^2 C(I_{C1} + I_{C2})}{\Phi_0/2\pi} = \frac{\pi^{3/2}V_0(2C_J + C_L)}{2eC_G \cdot (\sqrt{V_{IN1} - V_T} + \sqrt{V_{IN2} - V_T})} \tag{11}
\]

where \( I_{C1} \) and \( I_{C2} \) are the critical current of the two JJ-FETs. Fig. 8 presents the results of transient analysis for JJ-FET NOR gates with the same device parameters used in JJ-FET inverters and doubled \( I_{Bias} \). Fig. 8(a)–(d) shows the input waveforms for the Nb- and Al-contact JJ-FET NOR gates, respectively. The signal at \( V_{IN2} \) has twice the period and is in phase with that at \( V_{IN1} \) to enumerate all four possible logic combinations at the inputs. The output waveforms for the Nb- and Al-contact JJ-FET NOR gates are shown in Fig. 8(e) and (f) with \( C_L = 1 \text{ fF} \) and Fig. 8(g) and (h) with \( C_L = 2.5 \text{ fF} \). Finally, output waveforms for the Nb- and Al-contact JJ-FET NOR gates with \( C_L = 5 \text{ and } 7 \text{ fF} \) are shown in Fig. 8(i) and (j).

**Table II**

| \( C_L \) | \( V_{IN1} \) | \( V_{IN2} \) |
|---------|------------|------------|
| \( V_{OUT} \) |                          |

\( Q \) is crucial to determine the behavior of the JJ-FET NOR gates. In Fig. 8(e) and (f), \( V_{OUT} \) correctly reproduces the response of a NOR gate, e.g., \( V_{OUT} \) only becomes finite when both inputs are low. However, when \( C_L \) is increased from 1 to 2.5 fF, \( V_{OUT} \) fails to be reset to zero when only one of the inputs switches from low to high and outputs an undefined intermediate state [see Fig. 8(g) and (h)]. When \( C_L \) is further increased to 5 and 7 fF for the Nb- and Al-contact JJ-FET NOR gates, \( V_{OUT} \) remains finite even when both inputs switch to high. Consequently, there are two undefined intermediate states, as shown in Fig. 8(i) and (j).

**C. Global Clock to Reset JJ-FETs**

In the previous section, we showed that the \( Q = 0 \) approximation is not applicable if the fan-out load capacitance is taken...
TABLE II
Q OF JJ-FET NOR GATE

| Logic values of \( V_{IN1} \) and \( V_{IN2} \) | 00 | 01 or 10 | 11 |
|---------------------------------------------|----|----------|----|
| Nb-contact, \( C_L = 1 \text{ fF} \)       | 7.1| 2.9      | 2.0|
| Nb-contact, \( C_L = 2.5 \text{ fF} \)    | 12.6| 6.7      | 4.3|
| Nb-contact, \( C_L = 5 \text{ fF} \)      | 21.8| 12.0     | 8.0|
| Al-contact, \( C_L = 1 \text{ fF} \)      | 2.54| 1.0      | 0.7|
| Al-contact, \( C_L = 2.5 \text{ fF} \)    | 4.5 | 2.3      | 1.5|
| Al-contact, \( C_L = 7 \text{ fF} \)      | 10.4| 5.6      | 3.8|

Table 2: Logic values of \( V_{IN1} \) and \( V_{IN2} \) for different Q values for JJ-FET NOR gate.

Indeed, since the logic value of \( V_{OUT} \) must be evaluated when \( V_{CLK} = 0 \), the waveform half-period should exceed \( t_{PW} + t_\text{f} + t_\text{h} \), where \( t_\text{h} \) is the hold time. It is noteworthy that \( V_{CLK} \) may be synchronized with the clock in a dynamic logic gate.

**IV. Discussion**

The model we employ in this article ignores the mesoscopic effects and applies to ideal contacts. It is, therefore, necessary to examine the validity of our assumptions. First, mesoscopic effects can potentially change the \( I_1 \) value. For example, while Kondo resonances can suppress this magnitude, we expect a minimal effect for the device in the short ballistic regime [21]. The experimentally observed \( V_0 \) value is close to the ballistic limit \( \pi \Delta \) [11], suggesting that the JJ-FET is not operating in the Kondo effect-dominated regime. Second, mesoscopic effects can change the dependence of \( I_1 \) on \( \varphi(t) \). Fortunately, this current-phase relation remains sinusoidal for a short ballistic junction in nanoscale [22]. On the other hand, in a realistic device, carriers will observe a tunnel barrier at the channel/contact interface, a key ingredient to validate the sinusoidal current-phase relation [23]. It is noteworthy that the current magnitude is similar to the case where there is no tunnel barrier, since the reduction of current due to normal reflections at the disordered junction is compensated by the current increase from Andreev reflections [24]. We, therefore, assess that a realistic JJ-FET with finite transparency between...
the channel and contacts can still achieve $V_0$ at the short ballistic limit.

Additionally, in our analysis throughout, we have assumed the JJ-FET gate overdrive $V_G - V_T$ controls the gate charge ($q_G$) and therefore $I_C$ by modulating the weak link in the channel. However, this unidirectional JJ-FET model where $I_{DS}$ is set by $q_G$ without a back reaction is thermodynamically unsound [25]. The energy of a JJ-FET is

$$E_{JF} = \frac{q_G^2}{2WLC_G} + \frac{\hbar}{2e} I_C(q_G)(1 - \cos \phi(t))$$

(12)

where $I_C(q_G)$ is $I_C$ with gate charge $q_G$. Since $V_G - V_T = \tilde{\gamma} E_{JF}/\tilde{q}_G$, we find $q_G$ is reduced, compared to the unidirectional model

$$q_G = WLC_G(V_G - V_T) - \frac{\hbar \beta(q_G)}{2e} (1 - \cos \phi(t))$$

(13)

where $\beta(q_G)$ is $\beta$ with gate charge $q_G$. The back reaction is negligible when the RHS second term is small, namely $\gamma = \hbar \beta(q_G)/2WLC_G(V_G - V_T) \ll 1$, a condition which does not hold for the logic device operation regime discussed here.

For the parameters used in the Nb-contact JJ-FET inverter at zero $V_{IN}$, i.e., $V_G - V_T = 1.2$ mV, $W = 1 \mu m$, and $L = 50$ nm, the two terms of (13) RHS are comparable.

We note that $\beta$ decreases with increasing $V_G - V_T$; hence, the back reaction becomes particularly important when $V_{IN}$ is low. This implies that if we ignore the back reaction, the channel can be fully depleted and $V_{OUT}$ will be in an undefined state. The back reaction can be compensated by shifting $V_T$ to a more negative value. For example, the operation of an Nb-contact JJ-FET inverter is restored by setting $V_T = -3.5$ mV. While the back reaction adds extra complexity to the design of JJ-FET logic gates, if it is properly compensated at zero $V_{IN}$, at high $V_{IN}$, its impact is reduced.

It is of interest to investigate how advances in nanofabrication will influence the JJ-FET logic gates. Transistor scaling effectively produces smaller $L$ and larger $C_G$. In order to validate the model used in this article, $L$ needs to be sufficiently short compared to the superconducting coherence length

$$\tilde{\xi}_0 = \frac{\hbar v_F}{\pi e \Delta} = \frac{\hbar^2 2\pi C_G(V_G - V_T)}{m^* \pi e^{3/2} \Delta}$$

(14)

where $v_F$ and $m^*$ are the Fermi velocity and effective electron mass in the semiconductor channel, which are crucial to achieve a significant $\tilde{\xi}_0$ at the low $V_G - V_T$ required by JJ-FET logic gates. A large $C_G$ in the scaled JJ-FET device promises a long $\tilde{\xi}_0$ and small $\gamma$. Alternatively, it may also allow a lower $V_G - V_T$ to reduce power consumption. However, $Q$ will increase consequently, which imposes a design tradeoff of $C_G$ and potentially justifies the necessity of $V_{CLK}$.

The choice of superconductor contacts is another important factor. Choosing a low $\Delta$ contact has various benefits. In light of the requirements of finite $V_G - V_T$ for reasonable $\gamma$, $\tilde{\xi}_0$, and $Q$, and appreciable $\sigma_R$ for signal restoration, we usually have $V_G - V_T \sim \Delta$. Then, we can approximate the power consumption $P \propto I_C V_0 \propto \Delta^{5/2}$ and power-delay product $P \tau_{RL} \propto \Delta^{3/2}$, indicating that smaller $\Delta$ yields more efficient JJ-FET logic gates. Additionally, we have $Q \propto \sqrt{\Delta}$ and $\tilde{\xi}_0 \propto 1/\sqrt{\Delta}$, promoting the overdamped operation and relaxing the requirement of reduced $L$ and $m^*$. However, we also have $\gamma \propto 1/\sqrt{\Delta}$, which indicates a low $\Delta$ JJ-FET is less immune to the back reaction. Also, a larger $\Delta$ is favored for faster speed given $\tau_{RL} \propto 1/\Delta$. The above arguments impose a design tradeoff for $\Delta$.

Although JJ-FET logic gates cannot relax the requirement of ultraprecise control of $V_T$ compared with cryogenic CMOS, they provide a better circuit tolerance in the sense that JJ-FETs are always in the ON state while a CMOS device has to make a transition between ON and OFF states within the operating voltage window. Moreover, the speed of the JJ-FET logic gate is limited by $\tau_{RL}$ if designed properly for overdamped operation, as opposed to the $RC$ time constant in a CMOS device, which can be unacceptably high for the low carrier concentrations due to small $V_{DD}$ at cryogenic temperature.

On the other hand, JJ-FET logic gates possess a smaller break-even operating voltage than cryogenic CMOS if we factor in the static power consumption. JJ-FET logic gates also demonstrate great compatibility with emerging material platforms, e.g., the III–V quantum-well JJ-FET is a depletion-mode n-type device [11]; the graphene channel can reach its charge neutrality point at a slightly negative $V_G$ [10] and the proposed JJ-FET logic gates can circumvent the issue of low ON–OFF ratio for CMOS [26], [27]. Moreover, the low $m^*$ and high $v_F$ in III–V quantum-well, and especially in graphene, mitigate the conflict between long $\tilde{\xi}_0$ and low $V_G - V_T$, e.g., Dirac electrons in graphene have an $\tilde{\xi}_0 = 70$ and 470 nm in Nb- and Al-contact JJ-FETs [28], respectively.

### V. Conclusion

When cooling costs are factored in, the operating voltage of CMOS-based circuits has to be scaled down significantly for cryogenic computing to provide a net power reduction. JJ-FET Boolean logic can harness the superconducting property of these devices at these cryogenic temperatures and provide low operating voltage on the order of superconductor gap voltage. Assuming a short ballistic transport length, we employ the static and RCSJ model to capture the behavior of JJ-FET logic gates with fan-out. A global clock can mitigate the underdamped operation, if necessary. Transistor scaling and the choice of different superconducting contacts have notable impacts on the device operation. For example, reduced gate dielectric thickness guarantees better back-reaction immunity but favors underdamped operation, and larger gap voltage ensures a faster operation speed but at the cost of reduced coherence length, hence channel length. We find JJ-FET logic gates can be a promising candidate for dynamic logic elements with ultrashort fall times and can utilize the advantages of emerging channel materials like III–V quantum wells and graphene.

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### References

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