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LOW POWER PIPELINED DWT-IDWT ARCHITECTURE FOR OFDM SYSTEM ON FPGA

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Abstract

OFDM systems are widely used in most of the wireless communication systems. OFDM achieves better bandwidth efficiency and data rate. FFT module in OFDM system is being replaced with DWT to reduce complexities in hardware implementation. In this paper, we propose a modified Distributive Arithmetic (DA) based DWT architecture for OFDM system. The proposed module is implemented on FPGA and its performances are compared with parallel and pipelined DA DWT architecture. The proposed DWT logic operates at a maximum frequency of 378MHz and consumes power less than 26 mW. The memory size is reduced from 256 bytes to 16 bytes thus saving large storage space on FPGA. Functional verification of the developed system is carried out using modelsim. Simulink models for the OFDM unit are developed and performances are estimated.

Key words: Distributive arithmetic; DWT; OFDM; Low power; High speed; FPGA.

1. Introduction

Orthogonal frequency division multiplexing system is one of the most promising technologies for current and future wireless communications. It is a form of multicarrier modulation technologies where data bits are encoded to multiple sub-carriers, while being sent simultaneously [1]. Each sub-carrier in an Orthogonal Frequency Division Multiplexing (OFDM) system is modulated in amplitude and phase by the data bits. Modulation techniques typically used are binary phase shift keying, Quadrature Phase Shift Keying (QPSK), Quadrature Amplitude Modulation (QAM), 16-QAM, 64-QAM etc., The process of combining different subcarriers to form a composite time-domain signal is achieved using Fast Fourier Transform (FFT) and Inverse FFT (IFFT) operations.[2] The main problem in the design of a communications system over a wireless link is to deal with multi-path fading, which causes a significant degradation in terms of both the reliability of the link and the data rate. Multi-path fading channels have a severe effect on the performance of wireless communication systems even those systems that exhibits efficient bandwidth, like OFDM [3]. There is always a need for developments in the realization of these systems as well as efficient channel estimation and equalization methods to enable these systems to reach their maximum performance [4]. The OFDM receiver structure allows relatively straightforward signal processing to combat channel delay spreads, which was a prime motivation to use OFDM modulation methods in several standards [5, 6, 7].

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In transmissions over a radio channel, the orthogonality of the signals is maintained only if the channel is flat and time-invariant, channels with a Doppler spread and the corresponding time variations corrupt the orthogonality of the OFDM sub-carrier waveforms. In a dispersive channel, self interference occurs among successive symbols at the same sub-carrier causing Inter Symbol Interference (ISI), as well as among signals at different sub-carriers causing Inter Carrier Interference (ICI). For a time invariant but frequency-selective channel, ICI, as well as ISI, can effectively be avoided by inserting a cyclic prefix before each block of parallel data symbols at the cost of power loss and bandwidth expansion [2].

Conventional OFDM/QAM systems are robust for multi-path channels due to the cyclically prefixed guard interval which is inserted between consequent symbols to cancel ISI. However, this guard interval decreases the spectral efficiency of the OFDM system as the corresponding amount [8]. Thus, there have been approaches of wavelet-based OFDM which does not require the use of the guard interval. It is found that OFDM based on Haar orthonormal wavelets (DWT-OFDM) are capable of reducing the ISI and ICI, which are caused by the loss in orthogonality between the carriers [9,10,11,12,13].

The paper is organized as follows. In section 2 we describe the OFDM system and provide the algorithm for computing the mapping data; in section 3 we describe and provide a fast discrete wavelet transform computation algorithm used in proposed system design; in section 4 we describe the proposed low power pipelined wavelet OFDM system and in section 5 we discuss on the obtained results; finally in section 6, a conclusion is presented to summarize the main outcomes of this paper.

2. OFDM system and DWT

The block diagram of a transmitter and receiver of a typical communication system using OFDM is as shown in figure1. Input data (voice or video) is scrambled and encoded. The encoded data is modulated using OFDM technique and is converted to analog data. The analog data is modulated to higher frequency and is amplified and transmitted. At the receiver, the analog data is digitized using an ADC, the message is demodulated using OFDM and is decoded and unscrambled. The unscrambled data forms the message or information.
2.1. DWT-IDWT

The DWT can be looked at as the multiresolution decomposition of a sequence. It takes a length N sequence \( z(n) \) as input and generates a length N sequence as the output. The output can be viewed as the multiresolution representation of \( z(n) \), and has N/2 values at the highest resolution and N/4 values at the next resolution and so on. That is the frequency resolution is low at the high frequencies and high at the low frequencies, while the time resolution is high at the higher frequencies and low at the lower frequencies. It essentially consists of multiplying the input sequence by translates and dilates of the wavelet (though this will not be obvious from the equation shown below). Let N = \( 2^J \) and let the number of frequencies or resolutions, be \( J \), considering \( J \) octaves. Therefore the frequency index varies as, 1, 2, .., \( J \) corresponding to the scales \( 2^1 \), \( 2^2 \), .., \( 2^J \). The DWT is given by Equation (1) and Equation (2)

\[
W(n, j) = \sum_{m=0}^{2^n} W(m, j-1)w(2n - m) \\
W_H(n, j) = \sum_{m=0}^{2^n} W(m, j-1)h(2n - m)
\]

Where \( W(n, j) = z(n) \) and \( w(n) \) and \( h(n) \) are Quadrature Mirror Filters derived from the wavelet. To span our data domain at different resolutions, the analyzing wavelet is used in a scaling equation shown in Equation (3).

\[
W(x) = \sum_{k=-2}^{-2} (-1)^k c_{k} \phi(2x + k)
\]

Where \( W(x) \) in the Equation (3) is the scaling function for the mother function \( \phi \); and \( c_k \) are the wavelet coefficients. Figure 2 shows the DWT-IDWT pair. \( X(n) \) is decomposed to \( L(n) \) and \( H(n) \) using the low pass (analysis filters) and high pass filters (synthesis filters), and the decomposed signals are reconstructed using filters that are biorthogonal to the filters at the decomposition stage.

![Figure 2: DWT-IDWT pair model](image)

For OFDM applications, the analysis and synthesis stages are interchanged. DWT-IDWT form a transform pair, at the transmitter input signal from modulator with I and Q signal is passed through IDWT, the transformed time domain signal is passed through the channel. At the receiver, DWT block reconstructs the time domain signal into frequency samples of I and Q data.
2.2. Software reference model for OFDM using DWT

The OFDM block consists of a QAM modulator and IDWT at the transmitter and QAM demodulator and DWT at the receiver. Figure 3 shows the simulink model for OFDM transmitter and receiver. In this analysis, the channel is considered as AWGN, with 20 dB SNR. The input signal is modulated using QAM; the output of QAM produces a complex signal which is up sampled and processed through IDWT. The time domain signal output from IDWT is transmitted through channel with low signal power. The receiver receives the signal with noise; DWT decomposes the time signal into two sub bands and are demodulated to retrieve the message signal. Based on the input signal transmitted and the output signal received at the receiver, BER is computed for various SNR levels in the channel. The results obtained are compared with the OFDM model using FFT.

Figure 3: Simulink model of OFDM with QAM and DWT
3. Distributed Arithmetic approach for DWT

Distributed arithmetic [14] is an efficient method for computing the inner product operation, which constitutes the core of the discrete wavelet transform. In this section, distributed arithmetic algorithm is discussed. DWT implementation using distributive arithmetic approach is compared with parallel & pipelined DA DWT architecture for area, power and speed parameters. Based on the results obtained, new architecture is proposed for improvement in speed and power performances [15, 16].

Mathematical derivation of distributed arithmetic is extremely simple; a mix of Boolean and ordinary algebra. Let the variable $Y$ hold the result of an inner product operation between a data vector $x$ and a coefficient vector $a$. The conventional representation of the inner product operation is given as follows:

$$Y = \sum_{i=0}^{N-1} a_i x_i = \sum_{j=0}^{B-1} \left[ \sum_{i=1}^{N} x_i 2^{-j} \right]$$  \hspace{1cm} \text{(4)}$$

Where the input data words $x_i$ has been represented by the 2’s complement number presentation in order to bound number growth under multiplication. The variable $x_{ij}$ is the $j^{th}$ bit of the $x_i$ word which is Boolean, $B$ is the number of bits of each input data word and $x_{0i}$ is the sign bit. Interchanging the order of summation of Eq. (4), Eq. (5) is obtained:

$$Y = \sum_{j=0}^{N} \left[ \sum_{i=1}^{B-1} a_i 2^{j} + \sum_{i=0}^{N} x_i 2^{-j} \right] - F$$

$$= \sum_{j=0}^{N} \left[ 2^{j} 2^j \right] - F$$ \hspace{1cm} \text{(5)}$$

Distributed arithmetic is based on the observation that the function $F_j$ can only take $2N$ different values that can be pre-computed offline and stored in a look-up table. Bit $j$ of each data $x_{ij}$ is then used to address this look-up table. Eq. (5) clearly shows that only three different operations are required for calculating the inner product. First, a look-up table to obtain the value of $F_j$, then addition or subtraction, and finally a division by two that can be realized by a shift. In its most obvious and direct form, distributed arithmetic computations are bit-serial in nature, i.e., each bit of the input samples must be indexed in turn before a new output sample becomes available. When the input samples are represented with $B$ bits of precision, $B$ clock cycles are required to complete an inner-product calculation. An example of a distributed arithmetic implementation of a 4- element inner product operation is shown in Fig. 4(b) along with the conventional implementation of the same product operation in Figure 4 (a).

![Figure 4 (a): Conventional Implementation](image-url)
4. Low power pipelined DWT for OFDM

In this work, low power pipelined architecture is designed and implemented on FPGA for the DWT-IDWT pair. The proposed design can be used in OFDM system for low power applications. Figure 5 shows the proposed distributive arithmetic logic based DWT architecture.

To speed up the process we can go for the parallel implementation of the Distributive Arithmetic (DA). The structure is as shown in the Figure 5. In parallel implementation, we divide the input data into even samples and the odd samples based on their position. Even we can split the filter coefficients into even and odd samples. So, the even samples convolve with the even and odd filter coefficients and at the same time the odd samples also convolve with the same coefficients. So, by the same time we are getting the result for both even and odd samples of input.

4.1 Architecture comparison

The size of DA architecture depends on the selection of wavelets. Considering 9/7 wavelet, that consists of 9 filter coefficients in the low pass and 7 in the high pass. The size of LUT for low pass is $2^9$ and $2^7$ locations. In order to reduce the number of memory locations of the LUT, split parallel architectures are proposed. As the number of coefficients is odd number, the LUT is the input registers or data samples and are split into two sections of 5 and 4, thus the LUT size required is $2^5$ and $2^4$, for low pass and $2^4$ and $2^3$ for the high pass. Thus the memory size is reduced of the LUT is reduced from ($2^9$ to $2^5 + 2^4$) and $2^7$ to ($2^4 + 2^3$). In order to further reduce the memory size; in this work we have proposed a modified DA-DWT architecture as shown in figure 5. In this architecture, the LUT size is decomposed to combinations of $2^1$. Thus the total number of LUTs required for a 8 tap wavelet filter consists of 16 LUTs each of size $2^1$. Reducing the size of LUTs reduces the architecture complexity, but as the number of LUTs are increased the adders also significantly increase, thus in order to minimize the delay in the adder section, the addition of partial products is computed in parallel. As the carry chain logic of FPGAs is being utilized the adders are realized using the dedicated logic available on the FPGA, thus optimizing the resources. Table 1 below compares the reduction in LUT size for the proposed architecture for an 8 input 8 filter structures.
Table 1 Comparison of hardware complexity of DA architecture

| Parameter          | Parallel DA | Modified DA |
|--------------------|-------------|-------------|
| Memory size        | 32          | 16          |
| Adders             | 3           | 15          |
| Latency            | 8 clock cycles | 12 clock cycles |
| Throughput         | 8 clocks    | 1 clock cycle |
| Resource utilized  | Dedicated adders | LUTs and carry chain |
| on FPGA             |             |             |

Modified DA architecture has higher throughput and also the carry chain logic on the FPGA is utilized to realize the adder structure, thus the design is optimized for area efficient and low power applications. The modified DA is modelled using Verilog HDL and implemented on FPGA.

5. Results

The software reference model for DWT based OFDM system is analyzed for its performance. Further, the DWT-IDWT module is implemented on FPGA and is optimized for area and speed performances. An input
sine wave at low frequency (KHz) is modulated using QAM modulator with a carrier frequency (MHz). The modulated data is up sampled and is passed through the IDWT processor. The output of IDWT is transmitted through the channel and is demodulated at the receiver using the QAM demodulator and DWT. DWT/IDWT forms one of the major signal processing unit in the OFDM modulator. Table 2 shows the BER comparison of DWT based OFDM with FFT based OFDM system.

Table 2: BER for various modulation schemes for FFT and DWT OFDM systems of different wavelets at 20db

| Modulation scheme | FFT       | Haar | Db-3 | Db-4 | Bior5.5 |
|-------------------|-----------|------|------|------|---------|
| 16-QAM            | 0.00005499| 0.000012| 0.0758| 0.099 | 0.0749  |
| 32-QAM            | 0.00682600| 0.003742| 0.0994| 0.0842| 0.0902  |
| 64-QAM            | 0.08712000| 0.060610| 0.0992| 0.069 | 0.0999  |
| 128-QAM           | 0.24610000| 0.201000| 0.92000| 0.94300 | 0.9660  |

From the results presented in the table, it is very clear that DWT based OFDM is superior than FFT based OFDM system in terms of BER, and hence is very much suitable for OFDM applications with noisy environments. The proposed DA based logic is modelled using HDL and is synthesized using Xilinx ISE. The design is targeted on Virtex V FPGA device and also Spartan IIIE FPGA device. The synthesis results obtained are compared with the existing results of DWT implementation on FPGA. Table 3 shows the comparison of FPGA implementation results of DWT.

Table 3: Comparison of FPGA synthesis results

| Parameters                  | Parallel & pipelined design | Proposed design (Spartan IIIE) | Proposed design (Virtex V) |
|-----------------------------|-------------------------------|--------------------------------|-----------------------------|
| Basic elements              | 2403                          | 2403                           | 1204                        |
| Number of LUTs              | 1256                          | 982                            | 472                         |
| Maximum clock frequency     | 60 MHz                        | 115 MHz                        | 378 MHz                     |
| Maximum power dissipation   | 43mW                          | 32 mW                          | 26 mW                       |
| Memory size                 | 256 x 8 bits                  | 16 x 8 bits                    | 16 x 8 bits                 |

From the results obtained it is found that the proposed architecture consumes less power than the reference design. Also the memory size is reduced by almost 75%. The frequency of operation is increased by twice on Spartan device and is almost increased by 8 times on Virtex devices. Thus the developed DWT module is suitable for low power and high speed applications.

6. Conclusions

In this paper, we have proposed a modified low power high speed DWT architecture for OFDM system. A software reference model is developed using simulink to compare the performances of OFDM system with FFT and DWT. Different wavelets have been chosen to compute performance of OFDM system. The simulink model is validated for its functionality and BER is computed for various SNRs. From the results it is found that
the DWT based OFDM unit exhibits better performance compared to FFT based OFDM. Further, a modified DA based DWT algorithm is developed and implemented on FPGA. The implemented design is faster and also consumes less power and is thus suitable for low power applications. The performances of the DWT module can be further improved by addressing the number representation schemes. The designed DWT module can be used as an IP core.

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