FPGA Implementation of Simplified Spiking Neural Network

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Abstract—Spiking Neural Networks (SNN) are third-generation Artificial Neural Networks (ANN) which are close to the biological neural system. In recent years SNN has become popular in the area of robotics and embedded applications, therefore, it has become imperative to explore its real-time and energy-efficient implementations. SNNs are more powerful than their predecessors because they encode temporal information and use biologically plausible plasticity rules. In this paper, a simpler and computationally efficient SNN model using FPGA architecture is described. The proposed model is validated on a Xilinx Virtex 6 FPGA and analyzes a fully connected network which consists of 800 neurons and 12,544 synapses in real-time.

I. INTRODUCTION

With Moore’s law being transformed into more than Moore, the scientific community is exploring alternate avenues for faster, cheaper, and more efficient computing, and Neuromorphic Computing is found to be one of the viable replacements of the present computing paradigm. Neuromorphic computing can be realized efficiently by utilizing Spiking Neural Networks (SNN). It aims at realizing the architecture and performance of a brain in silicon. The brain, being the most efficient system present, processes complex information much faster than any existing computer. In recent years, the popularity and application of spiking neural networks have increased considerably. SNN is prominently used in many applications such as event detection, classification, speech recognition, spatial navigation, and autonomous motor control. It has demonstrated its effectiveness in detecting analog signals from sensors [1]; designing controllers for autonomous robots [2]; performing detection and recognition tasks [3]; processing cortical data [4] and tactile form-based recognition [5].

With the advent of autonomous robots and self-driving vehicles and due to the rise in the realtime applications of embedded systems, it has become imperative to realize machine learning models on compact and energy-efficient platforms. The existing neural network models [6], are computationally intensive and require huge memory for their realization, therefore making them unsuitable for realtime and energy-efficient applications. Although SNN has been realized in Applications Specific Integrated Circuits (ASIC) such as SpiNNaker [7], BrainScaleS [8], SyNAPSE [9] Neuropipe-chip [10], etc. their objective is mainly to provide a solution for large scale simulations rather than for low power embedded applications. The SNN model proposed in this paper is aimed towards its energy-efficient, portable and realtime implementation for improvising the performance of electronic systems.

Conventionally, Field Programmable Gate Arrays (FPGA) are utilized for the validation of electronic systems as well as in the implementation of time-critical systems. FPGAs are also well-suited for providing a low power solution for massively parallel and computationally less complex models [11]. Although parallelism can be achieved using Graphics Processing Units (GPU) as well, FPGA implementations are advantageous where power consumption is an issue [12].

In today’s era, it is becoming mandatory for the intelligent system to learn efficiently in realtime from its surroundings. Existing FPGA models of SNN [13], [14] do not support the training of the network and, if the weights must be changed, the hardware has to be reprogrammed, rendering it unsuitable for realtime applications. The proposed solution combines the neuron membrane model and on-line spike-time dependent plasticity (STDP) learning.

II. RELATED WORK

Multiple hardware accelerators for SNN have been designed and implemented. The central aim of these architectures is to eradicate the limitations of software simulators like BRIAN [15], NEST [16], and NEURON [17], which are widely accepted in the research community. However, they hit scaling issues and become too slow for large scale networks due to lack of parallel computations [18]. In this section, we present an account of the previously implemented architectures. Table I summarizes the similar works and corresponding time resolutions, number of neurons, and synapses simulated and resources consumed per neuron. Comparing resources used per neurons takes into account the size of the network and is favorable for bigger networks that consume more resources.

The FPGA architecture by [19] simulates a fully connected network of 1,440 Izhikevich (IZ) neurons. The design updates all neurons at every time step regardless of the spiking activity. The time resolution recorded is 0.1 ms. Our proposed design is event-driven and updates a neuron only if there is any spiking activity. This implementation is more energy-efficient and gives two orders of magnitude lesser time resolution (2.5 us). In terms of resource usage, our architecture (800 neurons, 12,544 synapses) is far more efficient than theirs (1,440 neurons, 16 synapses). Also, their fixed-point representation of weights provides lesser flexibility than our floating-point representation. Although floating-point has higher latency, simplified equations compensated for it.

Another implementation is NeuroFlow [20], which can simulate an impressive number of neuronal units (600,000),
both LIF and IZ, on a 6-FPGA system. When compared to this setup, our design provides a sampling rate of 400kHz against their 1kHz.

The same applies to large scale hardware implementations like SpiNNaker [7], which are not well suited for low-power, compact embedded applications and cost very much. Our implementation aims at providing a comparatively small scale and energy-efficient solution. On the other hand, several neural implementations based on Application Specific Integrated Circuits (ASIC) have also been proposed [21]. Although they exhibit better performance and are more energy-efficient, there is a growing interest in the use of FPGA for this. FPGA provides the user the freedom to reconfigure fully or partially the configuration bitstream. Also, they facilitate the creation of multiprocessor systems (as on ASIC) due to the presence of IP cores [19].

III. SIMPLIFIED NEURAL NETWORK MODEL

As far as classic leaky integrate-and-fire (LIF) neuron model [6] is concerned, it is computationally very complex and has large memory requirements. In the literature [22], a simplified version of the LIF model with computationally less complex membrane potential update equations. Let $P_i$ be the membrane potential (function of time) which is altered by each incoming spike $S_{it}$, $i = [1...n]$ by a value of synapse weight $W_i$, along with the voltage leakage factor, $D$,

$$P_i(t) = \begin{cases} 
    P_{i-1} + \sum_{t=1}^{n} S_{it} W_i - D & \text{if } P_{i-1} < P_{\text{threshold}} \\
    P_{\text{refract}} & \text{if } P_{i-1} \geq P_{\text{threshold}} \\
    R_p & \text{if } P_{i-1} \leq P_{\text{min}}
\end{cases} \quad (1)$$

At every time constant $t$, the membrane potential decreases by a fixed factor $P_i = P_{i-1} - D$ given that $P_{i-1}$ is greater than $R_p$, the resting potential. This simplified equation can be easily implemented in hardware unlike classic models which require large number of look up tables. When $P_i > P_{\text{threshold}}$ a spike is fired and the neuron transits into refractory phase where it blocks any input for a duration of $t_{\text{refract}}$.

IV. SPIKE TIME DEPENDENT PLASTICITY

Spike Time Dependent Plasticity (STDP) is a biological process, first discovered by Bi and Poo [23], which changes the connection strengths between neurons (synapses) in the brain. It is an unsupervised learning algorithm that operates upon the time difference between post-synaptic and pre-synaptic spikes. In a given synapse, if the post-synaptic spike occurs in a specific time window (STDP window) after pre-synaptic spike, the synaptic strength is increased, and if it occurs before pre-synaptic spike, the strength is decreased.

Equation 2 describes the simplified weight change rule. STDP window is described as $t \in [2, 20]$ in both directions. Weights are kept within the range $w_{\text{min}} < w < w_{\text{max}}$.

$$w_{\text{new}} = \begin{cases} 
    w_{\text{old}} + \sigma \Delta w (w_{\text{max}} - w_{\text{old}}) & \text{if } \Delta w > 0 \\
    w_{\text{old}} + \sigma \Delta w (w_{\text{old}} - w_{\text{min}}) & \text{if } \Delta w \leq 0
\end{cases} \quad (2)$$

$\Delta w$ is calculated using the exponential reinforcement curve employed in classic LIF. It has only 19 entries on either side and, hence, requires very few memory resources (lookup tables) for implementation. Equation 3 describes the determination of change in weights; $\Delta t$ is the time difference between pre-synaptic and post-synaptic spikes and $A^+$ and $A^-$ are the constants for positive and negative $\Delta t$ values, respectively; $\tau_+$ and $\tau_-$ are steepness time constants in both directions. Weights are kept within the range $w_{\text{min}} < w < w_{\text{max}}$.

$$\Delta w = \begin{cases} 
    A^- \exp(\frac{\Delta t}{\tau^-}) & \text{if } \Delta t \leq -2 \\
    0 & \text{if } 2 < \Delta t < 2 \\
    A^+ \exp(\frac{\Delta t}{\tau^+}) & \text{if } \Delta t \geq -2
\end{cases} \quad (3)$$

V. KEY DESIGN ELEMENTS

Spike Time Dependent Plasticity is the backbone of the spiking neural networks as it enables the learning process. A complete system aiming to replicate the biological neural model requires feature extraction, relativity of neural activity based on input strength, and competition among neurons for a particular class. These are described as follows.

A. Visual Receptive Field

Receptive Field is the area of an image which produces the input for a visual neuron. As the neural layers go deeper the receptive fields get bigger, convolving inputs from the previous layers. It can be expressed as a convolution filter for a variety of operations like edge detection, sharpening, and blurring. In our system we have implemented the receptive field, RF as a low pass blurring filter on the image.
B. Spike Generation

In a biological neuron, the input excitation is transmitted as time-domain impulses. The frequency of the impulses is proportional to the excitation. We have replicated this by taking the output of the receptive field $RF$, the maximum membrane potential $R_{\text{max}}$, and the minimum refractory period $RP_{\text{min}}$ to generate firing rate of the neuron $FR$.

$$FR = \begin{cases} \frac{1}{RP_{\text{min}} + R_{\text{max}}} & \text{if } RF > 0 \\ 0 & \text{if } RF \leq 0 \end{cases}$$

(4)

C. Variable Threshold and Lateral Inhibition

The voltage threshold at which a neuron fires is kept variable for each image. This is to make sure that images irrespective of their relative brightness produce uniform output for subsequent layers. The voltage threshold is kept as one third the maximum input spike frequency of the layer.

Lateral Inhibition is used to induce competition among output layer neurons for a particular class. When the first output neuron fires for a particular image, the potential of all the other neurons is reduced by half the threshold potential. This 'winner takes all' strategy ensures selectivity of the winner neuron for the class as the firing activity of other contending neurons is suppressed. Lateral inhibition is from biological neural networks where strengthening of one neural pathway weakens the neighbouring ones.

D. Hardware Algorithm

Spiking neural networks rely on the temporal information carried by spike trains and hence require a notion of time. A Time Unit block has been used in our system to keep track of time steps during training and classification. Although the number of time units is fixed for every data sample in training or classification phases, the number clocks to process one is highly adaptive as shown in Fig.2.

VI. RESULTS

A. Resource Usage

The network with 784 input ($I$) and 16 output ($O$) neurons and with 12,544 synapses using 24 bits to represent a membrane potential and weights ($W$) was implemented on Xilinx XC6VLX240T device. A single Block RAM of size 36Kb was used as FIFO for each output neuron to store synapse weights. Additionally, four DSP48E1 slices capable of addition and multiplication were used for single output neuron in its Potential Adder and Weight change blocks. The Table II provides resource usage for the complete system.
TABLE II
RESOURCE USAGE

| Resource         | Used  | Available | % Used | Resource Complexity |
|------------------|-------|-----------|--------|---------------------|
| Flip-flops       | 23,238| 301,440   | 8%     | I.O.W               |
| Slice LUTs       | 56,230| 150,720   | 37%    | I.O.W               |
| BRAMs            | 16    | 416       | 4%     | O                   |
| DSP48E1          | 64    | 768       | 8%     | O                   |

B. Timing Analysis

The proposed architecture has exploited the sparsity of spiking neural network for improvement in speed by morphing Time Units dynamic according to the spiking activity in input and output neurons (Fig. 2). Table III and Table IV provides timing analysis for classification and training of N images at an operating frequency of 100MHz.

TABLE III
TIMING ANALYSIS FOR CLASSIFICATION

| Operation              | Time Unit - Maximum | Time Unit - Average | Single Image | Classifying 10,000 images |
|------------------------|---------------------|---------------------|--------------|---------------------------|
| Time                   | 8.5us               | 2.5us               | 0.5ms        | 5s                        |
| Time Complexity        | I.O.W               | I.O.W               | I.O.W        | N.(I.O.W)                 |

TABLE IV
TIMING ANALYSIS FOR TRAINING

| Operation              | Time Unit - Maximum | Time Unit - Average | Single Image | Training 60,000 images |
|------------------------|---------------------|---------------------|--------------|------------------------|
| Time                   | 17us                | 5us                 | 1.1ms        | 65s                    |
| Time Complexity        | I.O.W               | I.O.W               | I.O.W        | N.(I.O.W)              |

Table V presents the comparison of training and classification timings of a single image from the MNIST dataset over FPGA and CPU. Our FPGA architecture showcases a speedup of 256x for classification and 187x for training. The results account for the massive parallelism provided by FPGA at a low energy cost.

TABLE V
COMPARISON WITH SERIAL COMPUTATION

| Operation | FPGA    | CPU     |
|-----------|---------|---------|
| Classification | 0.5ms   | 128ms   |
| Training  | 1.08ms  | 202ms   |

VII. CONCLUSION

In this paper, we described an architecture for Simplified Spiking Neural Network which is implemented on FPGA and optimized for low power embedded applications with real-time learning. The simplification of the STDP algorithm doesn’t compromise with the classification and learning capabilities of the network and rather reduces the computation complexity which in turn helps in developing a hardware accelerator with minimum resource usage. The system is designed to take advantage of the sparsity of the network and fabricate each time unit according to the activity in the network. Also, an account of parameter analysis is presented which showcases our methodology of choosing efficient parameter values.

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