State-of-Charge Balancing Control for Optimal Cell Utilisation of a Grid-Scale Three-Phase Battery Energy Storage System Using Hybrid Modular Multilevel Converter Topology Without Redundant Cells

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ABSTRACT Cell state-of-charge (SoC) balancing within each branch of a three-phase battery energy storage system (BESS) and among three branches is crucial to overcome the inability to fully utilise the available capacity of a three-phase BESS. The proposed topology is constructed with one branch instead of three branches to take advantage of its idle cells/modules (Ms) (one-third of the total cells/Ms) and to eliminate the need of SoC balancing among the branches. Contrary to conventional topologies, idle cells/Ms can serve as redundant cells/Ms or can be dropped out of a BESS, thereby leading to a reduction in the cost, control complexity, size, and losses of a BESS. A novel SoC balancing strategy for the proposed topology of a three-phase BESS is introduced in this paper. Moreover, the cell/M activation algorithm is implemented to minimise the duration needed to activate the cells/Ms required to generate voltage for the phases, thereby leading to an improvement of battery operational efficiency. Based on the simulation results, SoC balancing among 3996 cells, 2664 cells, 333/222 Ms, and 12 cells in M with the lowest and the highest average SoC is achieved in 53 min, 48 min, 38 min, 18 min and 53 min, respectively.

INDEX TERMS Battery energy storage system, cell balancing, state-of-charge balancing, hybrid modular multilevel converter, redundant cells.

I. INTRODUCTION

The wide use of distributed generation based on renewable energy is one of the most effective solutions in the power industry for addressing global environmental issues [1]. However, voltage instability, poor power grid quality, frequency fluctuation, and load discrepancy are the main notable challenges faced during the integration of renewable energy sources (RESs) [2]. The integration of energy storage systems (ESSs) with RESs into the power grid is a promising solution to overcome these limitations and to obtain grid stability [2]. In addition, it can improve power quality through voltage and frequency regulation as well as avoiding power fluctuations by providing backup electricity [3], [4]. Consequently, many ESS technologies have emerged in recent years that can be classified into mechanical, electrical, chemical, and electrochemical storage systems. Electrochemical energy storage technologies are rechargeable battery energy storage systems (BESSs) that store electrical energy in the form of chemical energy [5]. Compared with batteries, such as nickel-cadmium cell and lead-acid cell, lithium-ion (Li-ion) cells have been widely used in BESSs because they are characterised by several features such as high energy density, fast charge/discharge capability, long life span, and low self-discharge rate [6], [7]. Nevertheless, cell parameter difference poses major drawback, which occurs during BESS
operation or due to manufacturing tolerance. Accordingly, the state-of-charge (SoC) imbalance occurs among the cells within a BESS [8].

In the conventional topology, a three-phase BESS is constructed using three branches. Each branch (phase) consists of numerous cells, which are connected in series and/or parallel to generate the required voltage and capacity [9]. The available capacity of the BESS is limited by the cells with the lowest/highest capacity where cells must not be overcharged and/or deeply-discharged, otherwise cells will be damaged and thus destroying the entire BESS eventually [10]. Therefore, during charging and as a result of cell parameter differences, the strongest cell (highest capacity) within a BESS reaches its upper voltage limit firstly, thereby terminating the charging operation, while the remaining cells are not completely charged. On the other hand, the weakest cell (lowest capacity) reaches its cut-off voltage firstly during discharging, thereby terminating the discharging operation, while the capacity of the remaining cells is not yet exhausted (still available) [11], [12]. Consequently, BESS typically requires a SoC balancing system [13].

Cell balancing circuits are either passive or active according to their energy handling ways [14]. In passive balancing, excess energy is eliminated through resistors, whereas in active balancing, additional storage devices (inductors, capacitors) are used to transfer the energy among the cells via small shunt currents [15]. The passive balancing circuit is the most common approach because of its low-cost and easy implementation [16]. However, its disadvantage is that energy is dissipated as heat, which is inefficient and difficult to deal with, particularly in space-restricted applications. On the other hand, active balancing circuits are not dissipative, but rather the circuits seek to individually monitor and control the SoC of cells during charging and discharging so that SoC balancing among cells is achieved at all times of BESS operation. Though numerous types of active balancing approaches have been proposed, they mainly focus on the architecture of the cell-balancing circuits which can be classified into three main categories: the adjacent cell-to-cell (A-C2C) [17], [18], the direct cell-to-cell (D-C2C) [19], [20], and the cell-to-pack (C2P) [21], [22]. The A-C2C architecture involves balancing circuits based on the switched capacitor converter, the Ćuk converter, and the bidirectional buck-boost converter. The A-C2C owns advantages such as simple structure, low cost, and modular design. However, its main drawback is that energy can only be transferred between adjacent cells, which consequently increase cell balancing duration and energy losses. Contrary to A-C2C, the D-C2C architecture can transfer the energy between any two cells regardless of their positions. However, since there is only one balancing circuit, only two selected cells can be balanced at the same moment. Thus, the balancing duration will be increased significantly when a high number of cells is imbalanced. The D-C2C architecture includes balancing circuits based on the quasi-resonant, the shared inductor, and the flying capacitor converters. Flexible balancing is provided in the C2P architecture by transferring energy between the individual cell and a pack of cells. In the C2P architecture, multiple transformers or multi-winding transformer is used where each cell requires a winding to step up the voltage [21]. Thus, compared to A-C2C and D-C2C architectures, C2P architecture suffers from increased cost, losses, and volume. However, it has the highest balancing speed.

Duty cycle balancing (DCB) architecture is a subcategory of active cell balancing circuits. Cell balancing is implemented by controlling the duty cycle of each cell based on their corresponding SoC [23]. Contrary to the previous architectures where all the cells are in the current path at all time, the fundamental idea of DCB is to bypass the cells during the system operation which requires integrating additional switches (in form of L-bridge or H-bridge) into each cell and/or a pack of cells [24]. Accordingly, the inclusive of redundant cells is a requirement for DCB circuits to meet the desired output voltage when some cells are bypassed. Modular multi-level converter using a cascaded H-bridge (CHB) has been widely used in BESS applications because they are characterised by using MOSFET switches, reducing output voltage harmonics, and possessing inherent modularity [25]. Moreover, SoC balancing among phases and cells/Ms within a single phase can be obtained in a CHB-BESS without additional balancing circuits [26], [27]. However, the zero-sequence voltage (ZSV) injection method is required to obtain SoC balancing among three phases, which cannot be applied without redundant cells/Ms [28]–[30]. The ZSV injection method has been described in [26], [29]. Note that the inclusion of the redundant cells/Ms in BESS increases the total cost of the BESS, control complexity, size, and losses. However, it is required in the conventional topology to prevent unnecessary shut-down of a BESS when several cells are dropped out for replacement/maintenance [31].

In [32], [33], CHB multilevel converter is used to integrate cells to the grid where each pack of cells (M) is linked to a single H-bridge. SoC balancing among Ms can be obtained by controlling their duty cycle, whereas it cannot be achieved among the cells within each M. In [26], [28], [33], ZSV injection method is used to obtain SoC balancing among three phases of a BESS. Nevertheless, an auxiliary battery management system (BMS) is necessary to obtain SoC balancing within each M (internal cells), which is achieved in [28] by developing a multi-level BMS where a multi-winding transformer is utilised to obtain SoC balancing among the cells, whereas SoC balancing among Ms is obtained by linking each M into H-bridge and releasing its power (of each M) according to its corresponding SoC. In [11], [26], each cell is integrated into an H-bridge to obtain SoC balancing at cell level without additional BMS or components. Moreover, controlling and monitoring each cell can be obtained by integrating each cell into H-bridge. Consequently, the BESS reliability can be increased by isolating (dropping out) the failed cells for replacement/maintenance without affecting the entire system. In [26], the control complexity of a BESS is addressed through a hierarchical control strategy.
its drawbacks involve utilising a huge number of switches, the inclusion of the redundant cells/Ms, and requires peak sharing algorithm [26]. The number of switches is reduced by using the hybrid modular multi-level converter in [34], whereby each cell is linked to L-bridge, while each M is linked to H-bridge. Moreover, an additional circuit (parallel module dual L-bridge) is used to minimise the duration needed to obtain SoC among cells/Ms, but SoC balancing among phases cannot be addressed. Note that in a grid-scale BESS, a significant number of cells is necessary to generate the desired output voltage ($V_{out}$), thereby determining the cells required to generate each level of $V_{out}$ during a short duration (normally corresponds to 10 ns [35]) is crucial. In [26], [35], the required cells are activated one after another until $V_{out}$ is closer to $V_{ref}$. The total voltage of the activated cells is compared to $V_{ref}$ after activating each cell. Therefore, a long duration is required to activate all the cells required to generate each level of $V_{out}$. Accordingly, a new algorithm is necessary to minimise the duration needed to activate the cells/Ms required to generate each level of $V_{out}$.

In the literature, when various balancing circuits are compared, evaluation criteria such as the efficiency, balancing speed, size, and cost are often qualitatively evaluated by assigning grades such as ‘excellent/high’, ‘good/medium’, and ‘poor/low’ [16]. Moreover, all compared cell balancing circuits should be designed under the same considerations; otherwise the quantitative comparisons will not be very meaningful. A summary of efficiency, reliability, control complexity, cost, size, losses and, control and monitoring of each cell for the proposed SoC balancing strategy compared to existing balancing strategy is presented in Table 1. In Table 1, efficiency and reliability are evaluated based on balancing speed, cost, size, losses, the ability to control and monitoring each cell, and the ability to meet $V_{ref}$ when several cells/Ms are dropped out for replacement/maintenance. Control complexity is evaluated according to the number of control and sensing signals.

This paper has two main contributions. First, a new topology of a three-phase BESS using three cascaded hybrid modular multi-level converters (TCHMMC) is proposed. Compared to the conventional topologies, the proposed topology is designed to generate output voltage for a three-phase BESS via one branch rather than three branches without redundant cells. As a result, one-third of the total cells is idle and isolated from the system. These idle cells can serve as redundant cells or they can be eliminated from a three-phase BESS. Therefore, the total number of the required cells for a three-phase BESS can be reduced by one-third without affecting its output power rating ($P_{out}$). Accordingly, control complexity, size, losses, and BESS total cost can be reduced. Moreover, in the proposed topology, SoC balancing among branches (phases) is not required, where one branch is utilised to generate a three-phase multi-level output voltage ($V_{outa}$, $V_{outb}$, and $V_{outc}$).

The second contribution is that a novel SoC balancing strategy of a three-phase grid-scale BESS is proposed. Moreover, a novel cell/M activation algorithm is proposed to minimise the duration needed to activate the cells/Ms required to generate each level of $V_{out}$, $V_{outb}$, and $V_{outc}$ by activating most of the required cells/Ms as explained in Section III with improved operational efficiency of a BESS. Contrary to the different SoC balancing strategies introduced in the literature, the proposed SoC balancing strategy begins by using current-prioritised (as explained in Section III) which aims to take advantage of the highest current among the three-phase currents to charge or discharge the cells/Ms with the highest priority during each time step of the duty cycle. Accordingly, the proposed SoC balancing strategy can be summarised in two main steps: First, based on $M$-prioritised (as explained in Section III), Ms with lowest priority will be activated to generate two output voltages that have the lowest two relative currents. Second, based on cell-prioritised (as explained in Section III), cells with highest priority will be activated to generate the output voltage that has the highest relative current. Note that the use of the highest current with cell-prioritised aims to address SoC balancing among cells in $M$. The methodology of the proposed topology is described in Section II. The SoC balancing strategy for the proposed

| TABLE 1. Comparison of the proposed SoC balancing strategy with the existing balancing strategy in literature. |
|---------------------------------------------------------------|
| Balancing strategy | Chatzinikolaou et al. [11] | Ooi, C.A [26] | Ahmad et al. [14] | Maharjan et al. [33] | Proposed SoC balancing strategy |
| Number of branches used to generate voltage for a three-phase | 3 | 3 | 3 | 3 | 1 |
| Requirements of redundant cells/Ms and SoC balancing strategy among phases? | Yes | Yes | Yes | Yes | No |
| Ability to control and monitoring each cell? | Yes | Yes | Yes | No | Yes |
| Number of switches required to balance K cell in Z module into a three-phase BESS | 12K | 12KZ + 12Z | 6KZ + 32Z | 12Z | 2KZ + 15Z |
| Cost, size, and losses | L | H | H | L | M |
| Efficiency and reliability | M | M | M | L | H |
| Control complexity | M | L | H | L | M |
| H: | High, | M: | Medium, | L: | Low |
topology of a three-phase BESS is explained in Section III. The simulation results of the proposed SoC balancing strategy are discussed in Section IV. The experimental set-up is presented in Section V while the conclusion of the study is provided in Section VI.

II. METHODOLOGY
A. PROPOSED TOPOLOGY CONFIGURATION
The proposed topology configuration of a three-phase BESS and operational statuses of each H-bridge and L-bridge are illustrated in Fig. 1. Compared to the conventional topologies, the proposed topology is constructed using one branch instead of three branches to generate voltages, the proposed topology is constructed using one branch through TCHMMC. The proposed topology consists of Z Modules (Ms), N cells/Sub-modules (SMs), three cascaded H-bridges (TCHB) (from $H_{sw_{a1}}$, $H_{sw_{b1}}$, and $H_{sw_{c1}}$ until $H_{sw_{a2}}$, $H_{sw_{b2}}$, and $H_{sw_{c2}}$), and an auxiliary switch linked to each H-bridge ($sw_{az}$, $sw_{bz}$, and $sw_{cz}$). Z, K, and $N = Z \times K$ refer to the number of Ms, the number of cells/SMs in $M$, and the total number of cells/SMs, respectively. In this paper, $K$ is unified for all Ms [36].

In Fig. 1a, three $H$-bridges connected in parallel of TCHB are linked to the next three $H$-bridges, which are connected in parallel via three ports, and so on (e.g., $H_{sw_{a1}}$, $H_{sw_{b1}}$, and $H_{sw_{c1}}$ are linked to $H_{sw_{a2}}$, $H_{sw_{b2}}$, and $H_{sw_{c2}}$, respectively). The upper three ports of TCHB are linked to the electrical grid to generate $V_{refa}$, $V_{refb}$, and $V_{refc}$ whereas the lower three ports of TCHB are linked together. Each phase is linked to a certain CHB of TCHB. To avoid the overlapping of three-phase currents of the electrical grid (short-circuit), an auxiliary switch is linked between the upper end of each $H$-bridge and its corresponding $M$, as presented in Sub-section B, Section II. Each cell is linked to L-bridge. M consists of $K$ cells connected in series via cascaded L-bridge. The lower end of each $H$-bridge and its corresponding $M$ are connected together. Accordingly, before a BESS starts operation, each $M$ is linked to its related $H$-bridges in parallel and series with other Ms via TCHB, whereas during the BESS operation, each $M$ is linked to a single $H$-bridge of its related $H$-bridges in parallel and in series with other Ms, which are linked with the same CHB, as presented in Sub-section B, Section II. The proposed topology is, therefore, constructed within one branch. Fig. 1b and 1c show $M$ related switches statuses (either $ON$ ($1$ or $−1$) or $OFF$ ($0$)) and their effect on the voltage across $M$ and SM ($V_M$ and $V_C$). The voltage across $H$-bridge ($H_{swz}$) will be equal to $+V_M$, $−V_M$, and $0$ when $H$-bridge is $1$, $−1$, and $0$, respectively as shown in Fig. 1b. Note that current (I) will not pass through $M$ when the voltage across its related $H$-bridge is equal to $0$. The voltage across $L_{swk}$ will be equal to a cell voltage $+V_C$ or $0$ (i.e., the cell is idle) when $L_{swk}$ is $1$ or $0$, respectively as shown in Fig. 1c. Consequently, $V_M$ value is selected according to the number of its activated cells (e.g., assume that $M$ contains eight cells, six cells are activated while the remaining two cells are unutilised. Therefore, the $V_M$ value is equal to the sum of the voltages of these activated cells).

B. OPERATING PRINCIPLE AND CELLS/MODULES DISTRIBUTION INTO A THREE-PHASE
Each cell is independently controlled by linking it with an L-bridge. The failed cells can, therefore, be dropped out for replacement/maintenance without affecting the BESS operation. Many cells/SMs are linked with each other in series to generate $V_{out}$ close to $V_{ref}$. During BESS operation, each $M$ is linked into an $H$-bridge to generate a sinusoidal $V_{out}$ as shown in Fig. 2. In Fig. 2, each duty cycle ($0$ to $π$) is split into several $T_S$, where a certain level of $V_{out}$ is generated during each $T_S$. At the beginning of each $T_S$ ($t_1$, $t_2$, and so on), the cells/SMs required to generate each level of $V_{out}$ is activated based on the cell/M activation algorithm as explained in Section III. During each $T_S$, the cells’ statuses ($1$ or $0$) are determined based on SoC balancing strategy presented in Section III. The
The fundamental idea of the proposed topology involves using one branch rather than three branches to generate \( V_{\text{refa}}, V_{\text{refb}}, \) and \( V_{\text{refc}} \) via \( TCHB \). As a result, one-third of the total cells/Ms is idle and isolated from the remaining cells/Ms [36]. During each \( T_S \), Ms are split into three isolated groups and idle Ms as shown in Fig. 3. Splitting Ms into three groups can be obtained by controlling their corresponding switches as presented in Fig. 4. To avoid the overlapping of three-phase currents of the electrical grid (short-circuit), complete isolation among these groups must be obtained

\[
T_S < \frac{V_c}{\omega f V_{\text{peak}}}
\]  

(1)

prior to the utilisation of their corresponding Ms. All the cells/Ms take part to generate each level of \( V_{\text{refa}}, V_{\text{refb}}, \) and \( V_{\text{refc}} \). Nevertheless, there is no certain cell/M for a specific phase. Note that during each \( T_S \), each \( M \) can only be used in a single group. In Fig. 3, each group consists of a single cascaded hybrid modular multi-level converter (CHMMC). The first, second, and third groups are from \( M_{a1} - M_{aw}, M_{b1} - M_{by}, \) and \( M_{c1} - M_{ce} \), respectively, whereas the idle Ms are from \( M_{a1} - M_{iu} \). These groups are used to generate \( V_{\text{refa}}, V_{\text{refb}}, \) and \( V_{\text{refc}} \), respectively. Note that, \( V_{\text{refa}}, V_{\text{refb}}, \) and \( V_{\text{refc}} \) values are changed synchronously with each other. Accordingly, the number of the cells/Ms activated in each group varies with time according to its corresponding \( V_{\text{ref}} \) value. The terms \( w, y, \) and \( e \) are the number of the Ms activated to generate \( V_{\text{refa}}, V_{\text{refb}}, \) and \( V_{\text{refc}} \), respectively, while \( u \) is the number of the idle Ms during each \( T_S \). The \( u \) value is calculated in (2).

The term \( \text{Block} \) is the activated \( H\)-bridge (1 or -1) and its corresponding auxiliary switch. Fig. 4 shows three scenarios to activate \( M_1 \) during each specific \( T_S \). \( M_1 \) is connected to different phase (\( P_{ha}, P_{hc}, \) or \( P_{ha} \)) during each scenario. Moreover, Fig. 4 shows the method utilised to isolate \( M_1 \) from the remaining phases once it is selected to be within a certain phase (e.g., once \( M_1 \) is selected to be within \( P_{ha} \), it is isolated from \( P_{ha} \) and \( P_{hc} \) as shown in Fig. 4a).

In Fig. 3 and Fig. 4a, during each \( T_S \), only a single \( H\)-bridge of three \( H\)-bridges connected in parallel, are linked (ON (1 or -1)) into their corresponding \( M \), while the remaining two \( H\)-bridges are OFF (0). In Fig. 3, the total voltage across \( (M_{a1} - M_{aw}, (M_{b1} - M_{by}), \) and \( (M_{c1} - M_{ce}) \) should be as close as possible to \( V_{\text{refa}}, V_{\text{refb}}, \) and \( V_{\text{refc}} \), respectively. In Fig. 4, \( M_1 \) is linked to three \( H\)-bridges (\( Hsw_{a1}, Hsw_{b1}, \) and \( Hsw_{c1} \)) of \( TCHB \) via their auxiliary switches (\( sw_{a1}, sw_{b1}, \) and \( sw_{c1} \)) before starting the operation of the BESS. Nevertheless, during each specific \( T_S \), only a single \( H\)-bridge is linked (ON (1 or -1)) to \( M_1 \) once starting the operation of the BESS, while the remaining two \( H\)-bridges are OFF (0) as presented in Fig. 4a, Fig. 4b, and Fig. 4c. In Fig. 4a, \( M_1 \) is linked only to \( Hsw_{a1} \) (\( Hsw_{a1} \) is ON (1 or -1)), which means that \( I_a \) flows through \( M_1 \). In Fig. 4a, \( Hsw_{b1} \) and \( Hsw_{c1} \) are OFF (0), which means that \( I_b \) and \( I_c \) do not flow through \( M_1 \). Similarly, in Fig. 4b and Fig. 4c, \( M_1 \) is linked only to \( Hsw_{b1} \) and \( Hsw_{c1} \), respectively.

\[
\begin{align*}
\Delta n &= Z - (w + y + e) \\
\text{(2)}
\end{align*}
\]

The proposed topology is able to create a huge number of idle cells/Ms (up to more than one-third of the total cells/Ms) at any given time of the BESS operation. Accordingly, the proposed SoC balancing strategy is designed to be able to achieve SoC balancing among cells/Ms with/without a huge number of idle cells/Ms as described in Section III. However, the major drawback of conventional topologies is the inability to
to take advantage of idle cells/Ms. On the other hand, the proposed topology has key advantages, involving the result of dealing with its idle cells using three methods [36]. First, they can be dropped out of the BESS plant, while still achieve the desired $P_{out}$. Second, they can be served as redundant cells and, therefore, the inclusion of the redundant cells is not required. Third, during peak demand, they can be used to meet the desired $P_{out}$. As a result, the total cost of the BESS, control complexity, size, and losses were significantly reduced, whereas reliability increased.

C. THE DIFFERENCE IN THE NUMBER OF IDLE CELLS DURING CHARGING/DISCHARGING

The cell involves an internal cell voltage ($V_{\text{int}}$) and an internal resistance ($R_{\text{int}}$) according to the basic concept of cell configuration [12]. Therefore, during charging and discharging, (3) is used to calculate the cell output voltage ($V_C$) based on Kirchhoff’s Second Law. As observed in (3), the $V_C$ value slightly increases during charging and slightly decreases during discharging due to $R_{\text{int}}$. Therefore, the number of cells required to obtain $V_{\text{out}}$ reduced during charging and increased during discharging. Accordingly, the total number of idle cells/Ms during charging is higher than the number of idle cells/Ms during discharging.

$$
\begin{cases}
V_c = V_{\text{int}} + \bar{I}R_{\text{int}}, & \text{Charging.} \\
V_c = V_{\text{int}} - \bar{I}R_{\text{int}}, & \text{Discharging.}
\end{cases}
$$

(3)

D. CELL SoC ESTIMATION

The accuracy of the SoC estimation is one of the important keys in cell balancing. Therefore, numerous ways have been developed to achieve an accurate SoC estimation as presented in [37]. In this paper, cell SoC balancing relies on the Coulomb Counting method to estimate SoC, which is designed according to (4). The method algorithm and details are presented in [26].

$$
\text{SoC}(t) = \text{SoC}_0 + \frac{1}{Q_{\text{max}}} \int_0^t I(t)dt
$$

(4)

$Q_{\text{max}}$, SoC0, and $I(t)$ refer to a maximum capacity limit of a cell, initial SoC, and current going either in/out of a cell, respectively.

III. SOC BALANCING STRATEGY OF A THREE-PHASE GRID-SCALE BESS FOR THE PROPOSED TOPOLOGY USING CONTROL STRATEGY

In TCHMMC, $V_{outa}$, $V_{outb}$, and $V_{outc}$ are generated by controlling its -TCHMMC- switching statuses as explained in Section II. In comparison with the conventional topologies, TCHMMC is constructed using one branch rather than using three branches. Accordingly, during each $T_S$, Ms are split into three isolated groups (each group consists of numerous Ms, which are connected in series) and idle Ms, where each group is linked to a certain phase ($Ph_a$, $Ph_b$, and $Ph_c$) as illustrated in Fig. 3. Each individual $M$ may belong to any group of these groups by controlling its related switching statuses (through the control strategy as described in Section II). Note that in conventional topologies, the ZSV method is used to obtain SoC balancing among three branches (three-phase). The ZSV method requires the inclusion of the redundant cells/Ms to be applied, which increases the total cost of BESS, control complexity, size, and losses as explained in Section I. On the contrary, in the proposed topology, $V_{\text{refa}}$, $V_{\text{refb}}$, and $V_{\text{refc}}$ are generated via only one branch and, therefore, SoC balancing among branches (phases) is not required (i.e., there is no need to include the redundant cells/Ms), which is the main contribution of the proposed topology in terms of the redundant cells/Ms and SoC balancing control among phases. In this paper, the control strategy aims to obtain SoC balancing among the cells/Ms of the proposed topology.

Some control strategies have been proposed in the literature [11], [26], [34] to achieve the cells/Ms SoC balancing into each branch of the BESS branches based on the priority list. The basic concept of the priority list is to prioritise the cells with the lowest SoC during each $T_S$ of the duty cycle during charging and vice versa. Therefore, it is wise to use the priority list to obtain SoC balancing among the cells/Ms in BESS constructed by a multi-level converter, whereby each cell/M is linked to H-bridge/L-bridge. However, the cells can be organised in a hierarchal structure (e.g., the cells in [26]...
are organised in a hierarchical structure, which consists of four levels as modules, sub-banks, banks, and phases. The cells in [34] are organised on three levels as sub-modules, modules, and phases). Thus, prioritising SoC balancing to cells level before Ms level (cell-prioritised) and the other way round (Ms-prioritised) had been proposed in [34]. Accordingly, two priority lists can be generated, including a cell priority list (C\textsubscript{PL}) and M\textsubscript{s} priority list (M\textsubscript{PL}). In C\textsubscript{PL}, cells are sorted depending on their SoC, while in M\textsubscript{PL}, Ms are sorted depending on their average SoC. The average SoC of M\textsubscript{s} is calculated using (5). M\textsubscript{SoC} and C\textsubscript{SoC}\textsubscript{K} refer to the average SoC of M and cell SoC, respectively. K is the number of cells in M. Note that the cells in cell-prioritised are used to generate V\textsubscript{ref} based on C\textsubscript{PL}, regardless of M\textsubscript{PL} (i.e., based on C\textsubscript{PL}, the cells with the lowest SoC will be activated during charging even if some of them are integrated into Ms which have the highest average SoC). The opposite occurs in M\textsubscript{s}-prioritised, where cells are activated depending on the activated Ms based on M\textsubscript{PL}, regardless of C\textsubscript{PL} (i.e., when Ms is activated based on M\textsubscript{PL}, all its related cells will be activated regardless of their SoC. Accordingly, several cells with the highest SoC will be activated during charging and vice versa). Note that in the proposed topology (one branch), even if only one cell is activated in M (to generate a certain voltage), M will be considered as active and, therefore, its remaining cells cannot be used to generate voltage for the remaining two phases.

The cells in the proposed topology are organised in a hierarchical structure (SMs (cells) and Ms). However, SoC balancing cannot be achieved with cell-prioritised or M\textsubscript{s}-prioritised alone in the proposed topology for the following reasons: 1) The fundamental idea of the control strategy when using cell-prioritised alone is to activate the cells, one after another, during each Ts of the duty cycle based on C\textsubscript{PL} to generate the desired V\textsubscript{out}. Accordingly, it is suitable for conventional topologies, which use three branches to generate V\textsubscript{outa}, V\textsubscript{outb}, and V\textsubscript{outc}. The proposed topology (one branch) is designed to generate V\textsubscript{outa}, V\textsubscript{outb}, and V\textsubscript{outc}, and the phases are generated one after another depending on the current-prioritised method as explained in this section. Thus, the activated cells and their related Ms are, therefore, assigned in a group to generate the desired V\textsubscript{out} for a phase before the cells can be used to generate voltage for the remaining two phases. The optimal number of Ms, which should be activated (NUM\textsubscript{s}) to generate the desired V\textsubscript{out}, is calculated in (6). NUM\textsubscript{s} is the number of cells activated to generate the desired V\textsubscript{out}, while \( \left\lceil \frac{\text{NUM}_{S}}{K} \right\rceil \) is the least integer after dividing NUM\textsubscript{s} by K (number of cells in M). The worst-case scenario happens when the number of Ms activated is close to NUM\textsubscript{s}, which leads to the inclusion of many cells/ Ms in only one group. Accordingly, when using cell-prioritised alone in the proposed topology, the drawback can occur when the remaining number of cells/Ms (after producing the desired V\textsubscript{out} for a phase) is insufficient to generate voltage for the remaining two phases of V\textsubscript{outa}, V\textsubscript{outb}, and V\textsubscript{outc}. Note that the activated Ms in the first group cannot be used again to generate the remaining two phases of V\textsubscript{outa}, V\textsubscript{outb}, and V\textsubscript{outc} during the same Ts. 2) The drawback of using M\textsubscript{s}-prioritised alone is that SoC balancing among cells is not achieved because all the internal cells of the activated Ms are activated to generate the desired phase of V\textsubscript{outa}, V\textsubscript{outb}, and V\textsubscript{outc} (except for the last activated M, where its cells are activated one after another until obtaining the desired V\textsubscript{out} close to V\textsubscript{ref}) regardless of their SoC compared with other cells in the inactivated Ms. Note that to achieve SoC balancing among the cells, an additional SoC balancing circuit is used in [34]. In M\textsubscript{s}-prioritised, NUM\textsubscript{s} is less than or equal to the number of the activate Ms multiplied by K. Accordingly, there are potential drawbacks when using cell-prioritised or M\textsubscript{s}-prioritised alone to achieve SoC balancing in the proposed topology. Therefore, a novel SoC balancing strategy is proposed in this paper to use cell-prioritised and M\textsubscript{s}-prioritised strategy, together to achieve SoC balancing among cells/Ms in the proposed topology. Fig. 7 illustrates the proposed SoC balancing strategy.

Generally, to determine the number of the cells required to generate each level of V\textsubscript{out}, cells are activated one after another until V\textsubscript{out} is closer to V\textsubscript{ref}. Thus, as a result of including a significant number of cells in a grid-scale BESS, a long duration is needed to activate the cells/Ms required to generate each level of V\textsubscript{out}. Accordingly, to minimise the required duration, the cell/M activation algorithm is proposed in this paper as illustrated in Fig. 5 and Fig. 6, respectively (cell activation algorithm is used with the cell-prioritised, while the M\textsubscript{s} activation algorithm is used with the M\textsubscript{s}-prioritised). It activates almost all the required cells/Ms from the first step of looking for the required cells/Ms, thereby leading to an improvement in the operational efficiency of the SoC balancing strategy. Note that cell-prioritised and M\textsubscript{s}-prioritised are used together during each Ts of the duty cycle in the proposed SoC balancing strategy to generate V\textsubscript{outa}, V\textsubscript{outb}, and V\textsubscript{outc} as shown in Fig. 7. In Figs. 5-7, a minimum number of cells (C\textsubscript{a,b,c}\textsubscript{min}) and Ms (M\textsubscript{a,b,c}\textsubscript{min}) required to generate any level of V\textsubscript{ref}, V\textsubscript{refb}, or V\textsubscript{refc} is calculated by (7) and (8), respectively. A maximum number of cells (C\textsubscript{a,b,c}\textsubscript{max}) required to generate any level of V\textsubscript{ref}, V\textsubscript{refb}, or V\textsubscript{refc} is calculated by (9). HV\textsubscript{C} and LV\textsubscript{C} are the highest and the lowest cell voltage, respectively, whereas HV\textsubscript{M} is the highest M voltage. The term \( |V\text{ref}_{(a,b,c)}| \) refers to the absolute value of V\textsubscript{ref}, V\textsubscript{refb}, or V\textsubscript{refc}.

\[
C_{a,b,c}^\text{min} = \left\lceil \frac{|V\text{ref}_{(a,b,c)}|}{HV_C} \right\rceil \quad (7)
\]

\[
M_{a,b,c}^\text{min} = \left\lfloor \frac{|V\text{ref}_{(a,b,c)}|}{HV_M} \right\rfloor \quad (8)
\]
ing close to each other because the difference between $M_s$ and the exact number of cells is not considered when $(Vref = Vref_a, Vref_b, or Vref_c)$. Note that the lowest number and the LV manufacturer setting is not considered when dividing $Vref$ into three groups for only one time and using each certain current ($I_{a}$, $I_{b}$, or $I_{c}$) (e.g., the cells/Ms with the highest priority will be activated to generate $Vref_a$, $Vref_b$, and $Vref_c$ consecutively) depending on which $Vref$ has the highest absolute value of its corresponding current ($I_{a}$, $I_{b}$, or $I_{c}$) (e.g., the cells/Ms with the highest priority will be activated to generate $Vref_a$, $Vref_b$, and $Vref_c$ consecutively when $|I_{a}| > |I_{b}| > |I_{c}|$, thereby taking advantage of the highest current ($I_{a}$) [see Fig. 8] to charge or discharge the cells/Ms with the highest priority throughout the BESS operation. This reduces the duration required to obtain SoC balancing among the cells/Ms compared to the following methods. First, the cells/Ms with the highest priority will be activated to generate $Vref_a$, $Vref_b$, and $Vref_c$ consecutively regardless of which one of them has the highest corresponding current (e.g., $Vref_a$, $Vref_b$, and $Vref_c$ will be generated consecutively even if $|I_{a}| > |I_{b}| > |I_{c}|$). Second, dividing the cells/Ms into three groups for only one time and using each certain group of them to generate a certain $Vref$ throughout the BESS operation (e.g., $M_1$-$M_{111}$ are used to generate $Vref_a$, $M_{112}$-$M_{522}$ are used to generate $Vref_b$, and $M_{523}$-$M_{333}$ are used to generate $Vref_c$). Note that using a certain current ($I_{a}$, $I_{b}$, or $I_{c}$)
to continuously charge or discharge a certain group of cells compared with using current-prioritised method (I_h is used to charge and discharge the cells with the highest priority), results in charging or discharging the cells with the highest priority by a small current during numerous T_s of each duty cycle because a grid reference current is in a sinusoidal waveform as shown in Fig. 8 and Table 2. Fig. 8 demonstrates a three-phase grid reference current (I_a, I_b, and I_c) and I_h during each T_s of the duty cycle. Table 2 illustrates the absolute values of the number of coulombs (Q = \int_0^{T_s} I(t)dt) flowing through the cell with the highest priority during the first half of the duty cycle for Fig. 8. I_h and I_a are used to calculate Q_h and Q_a, respectively. In Fig. 8 and Table 2, I_a, I_h, I_c, and I_b values are based on (10). As a result, the total number of coulombs (T_Q_a and T_Q_h) flowing through the cell with the highest priority increased by 50% (T_Q_h/2) compared with using a certain grid reference current (T_Q_a = 2 I_peak) as presented in Table 2. Therefore, the duration required to obtain SoC balancing among all cells will be reduced. Note that SoC balancing among cells in each M should be achieved before Ms, which is achieved by using cell-prioritised and current-prioritised method (cells with the highest priority are charged/discharged by I_h) as presented in Fig. 7. Without using current-prioritised method, the speed of achieving SoC balancing among cells in each M will drop steeply once SoC balancing among Ms is achieved as a result of using Ms-prioritised to generate voltage for two phases (when M is activated based on M_PL, all its related cells will be activated regardless of their SoC) as explained at the beginning of Section III. Thus, the duration required to obtain SoC balancing among all cells will be increased. The proposed SoC balancing strategy will utilise cell-prioritised and current-prioritised to make sure that SoC balancing among all cells and Ms is achieved in almost the same duration.
TABLE 3. Comparison of the proposed SoC balancing strategy with the existing balancing strategy.

| Balancing strategy            | SoC balancing approach                                                                                                                                                                                                 | Major limitations                                                                                     |
|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|
| Chatzinikolaou et al. [11]    | Cell SoC balancing is achieved by utilising the cell’s energy based on the priority list. Cell SoC balancing relies on the pseudo-open circuit voltage method to estimate SoC.                                                   | SoC balancing among phases is not addressed. SoC estimation is inaccurate.                              |
| Ooi, C.A. [26]                | A hierarchical control strategy is used. Utilising cell’s/M’s energy based on their SoC. ZSV method is used to achieve SoC balancing among the phases.                                                                 | Requires redundant cells/Ms and an additional peak sharing algorithm. Takes a long duration to achieve SoC balancing among cells. A high number of switches is used. |
| Ahmad et al. [34]             | The energy is transferred among cells/Ms (from cells/Ms with the highest SoC to cells/Ms with the lowest SoC) using a supplementary balancing strategy (SBS). Moreover, cell’s/M’s energy is utilised based on their SoC. | A supplementary balancing strategy is necessary to reduce the required duration to achieve SoC balancing among cells/Ms. Requires a high number of switches. SoC balancing among phases is not addressed. SoC balancing among cells is not addressed. Redundant cells/Ms are necessary to achieve SoC balancing among the phases. A high number of switches is used. |
| Proposed SoC balancing strategy| One branch instead of three branches is used to generate voltage for a three-phase, thus, SoC balancing among the phases is not required. Ms-prioritised, cell-prioritised, and current-prioritised are used to generate voltage for a three-phase, thus, cell/M SoC balancing is achieved by utilising the cell’s/M’s energy based on their SoC. |                                                                                                      |
in [38]. The proposed SoC balancing strategy is validated in the proposed topology using two case studies. The different number of cells/Ms is used in each case study. In case study 1, 3996 cells (333 Ms) are used, while in case study 2, 2664 cells (222 Ms) are used. Note that in case study 1, the rated energy capacity equals 290 kWh (= 3996 × 20 × 3.65), whereas it equals 194 kWh (= 2664 × 20 × 3.65) for case study 2.

Fig. 10 and Fig. 11 highlight the proposed topology features, while Fig. 12 and Fig. 13 demonstrate the simulation results of the proposed SoC balancing strategy. Fig. 14 shows the process of splitting Ms into three groups during each TS to generate \(V_{outa}, V_{outb}, \) and \(V_{outc}.\)

Fig. 10 shows the ability of the proposed topology to achieve \(V_{outa}, V_{outb},\) and \(V_{outc} (3.6 \text{ kV})\) and a three-phase AC rated active power \((P_{outa}, P_{outb}, \text{ and } P_{outc}) (60 \text{ kW})\) when using 3996 cells (333 Ms) or 2664 cells (222 Ms). The number of idle Ms when using 333 Ms or 222 Ms is presented in Fig. 11. In Fig. 10a, \(V_{outa}, V_{outb},\) and \(V_{outc}\) are generated with 3996 cells (333 Ms) and 2664 cells (222 Ms). Note that the number of cells/Ms is still high enough to generate its corresponding reference voltages even after reducing the number of cells/Ms to two-thirds (2664 cells (222 Ms)) as shown in Fig. 10a and Fig. 11b. The voltage step equals the cell voltage as a result of using a short \(T_S (T_S = 133 \mu s).\)

The peak voltage (3.6 kV) for a three-phase of the reference voltage and the output voltage are identical. In Fig. 10b, \(P_{outa}, P_{outb}, \text{ and } P_{outc}\) are generated in both cases of the number
FIGURE 12. The simulation results of the proposed SoC balancing strategy in the three-phase proposed topology using 3996 cells (333 Ms). SoC balancing among (a) cells, (b) Ms, (c) cells in M with the highest average SoC, and (d) cells in M with the lowest average SoC.

FIGURE 13. The simulation results of the proposed SoC balancing strategy in the three-phase proposed topology using 2664 cells (222 Ms). SoC balancing among (a) cells, and (b) Ms.

FIGURE 14. The distribution process of Ms into three groups to generate a three-phase output voltage by controlling their corresponding switches (M₁ and its corresponding switches are chosen to illustrate it).

of cells/Ms (3996 cells (333 Ms) and 2664 cells (222 Ms)). $P_{outa}$, $P_{outb}$, and $P_{outc}$ of $-55$ kW and $5$ kW are generated during charging whereas $55$ kW and $-5$ kW are generated during discharging. The positive and negative polarities of $P_{outa}$, $P_{outb}$, and $P_{outc}$ refer to discharging and charging operation, respectively (i.e., when $PF = 1$ (ideal case), $P_{out}$ has a negative polarity during charging due to the
voltage (V) and the current (I) have different polarities during each $T_S$ ($\cos(\theta) = 1$, $P_{out} = IV \cos(\theta)$). Similarly, the $P_{out}$ polarity is positive during discharging, where the polarity of $V$ and $I$ is negative or positive during each $T_S$. Nevertheless, in practical cases ($PF < 1$), there is a discharging status (its length depends on $PF$ value) during the BESS charging operation and vice versa, as a result of a phase shift ($\theta$) between $I$ and $V$ [see Fig. 12]. In Fig. 10b, the total of the maximum AC rated active power of a three-phase is equal to 180 kW (60 kW for a phase). In conventional topologies, $P_{out}$ (60 kW) and $V_{out}$ (3.6 kW) will not be obtained when the total number of cells/MS is reduced to two-thirds compared to the proposed topology.

Fig. 11a shows a significant range of idle MSs from 164 to 188 and from 142 to 176 of total 333 MSs during charging and discharging, respectively. Note that 142 MSs are equal to 1704 cells ($= 142 \times 12$). Thus, $V_{out}$ of each phase of $V_{outa}$, $V_{outb}$, and $V_{outc}$ can be increased by at least 1420 V ($= (1704 \times 2.5) / 3$) or the total number of cells/MS can be reduced by 142 MSs (1704 cells), 2.5 V is the cell cut-off voltage. Note that more than one-third of the total cells/MS is idle. The range of idle cells/MSs during discharging is lower than the range of idle cells/MSs during charging because of the cell voltage drop during discharging (i.e., requires a higher number of cells/MS to generate $V_{out}$) and increases during charging as given in (3). Fig. 11b shows the number of idle MSs into the proposed topology after reducing its total number of MSs from 333 to 222 MSs. However, even with 222 MSs (two-thirds), it has idle MSs, which ranges from 61 to 84 MSs and from 28 to 56 MSs during charging and discharging, respectively. Accordingly, the proposed topology is able to isolate idle cells/MSs from activated cells/MSs during the production of $V_{outa}$, $V_{outb}$, and $V_{outc}$ as shown in Fig. 10 and Fig. 11, which is the most attractive feature of the proposed topology. These idle cells/MSs can serve as redundant cells/MS or are dropped out of a three-phase BESS, thereby, reducing the total number of the required cells. However, the desired $P_{out}$ can be achieved, thereby leading to a reduction in the total cost of BESS, control complexity, size, and losses. Accordingly, the proposed SoC balancing strategy has been validated in the proposed topology when idle cells/MS serve as redundant cells/MS (case study 1 (3996 cells in 333 Ms)) as shown in Fig. 12 and when they are eliminated from BESS plant (case study 2 (2664 cells in 222 Ms)) as shown in Fig. 13.

It has been substantiated by the simulation results that the proposed SoC balancing strategy achieved the SoC balancing convergence among cells/MS regardless of the existing number of idle cells/MS. Note that SoC balancing among branches (phases) is not required for the proposed topology in this paper as explained in Section III. SoC balancing among cells, MSs, cells in M with the highest average SoC, and cells in M with the lowest average SoC are shown in Fig. 12a, Fig. 12b, Fig. 12c, and Fig. 12d, respectively. Note that M with the highest/lowest average SoC is determined upon the start of BESS operation. In Fig. 12a, SoC balancing convergence among 3996 cells is achieved in 53 min. Note that in 53 min, the average SoC among all the cells is 70 %, which is identical to the SoC of the cell with the highest initial SoC as illustrated in Table 4. Many cells’ traces are horizontal (there is no change in their SoCs) during 0 - 53 min, which refers to the idle cells. During 30 - 53 min, some of the cells are charging without following the fundamental concept of the priority list (the cells with the highest SoC are charged although there are inactivated cells, which have less SoC). This occurs as a result of using M-prioritised to generate voltage for the two-phase of $V_{outa}$, $V_{outb}$, and $V_{outc}$ (cell-prioritised is used to generate voltage for the phase with the highest absolute current ($I_a$, $I_b$, or $I_c$)) as explained at the beginning of Section III. This issue arises when M-prioritised is used to activate the cells (as explained at the beginning of Section III), while SoC difference among MSs is small [see Fig. 12b during 30 - 53 min] and SoC balancing among cells in each single M has not been achieved [34]. However, the drawback of using M-prioritised is addressed by using the current-prioritised method in the proposed SoC balancing strategy (SoC among cells is achieved in 53 min) in this paper [see Fig. 7]. In Fig. 12b, SoC balancing convergence among 333 Ms is achieved in 38 min. Some Ms are charged, whereas others are discharged during the BESS charging operation (0 – 58 min). This occurs as a result of the existence of a phase-shift between I and V ($PF < 1$) of each phase. Therefore, each phase status is changed from charging to discharging for a short period during each duty cycle of the charging operation, and vice versa as explained at the beginning of Section IV. In Fig. 12c, SoC balancing convergence among 12 cells in M with the highest average SoC is achieved in 53 min compared with 18 min for 12 cells in M with the lowest average SoC as shown in Fig. 12d. The cells in M with the highest average SoC are discharged at the beginning of the BESS charging operation, whereas the cells in M with the lowest average SoC are charged as shown in Fig. 12c and Fig. 12d, respectively. Accordingly, the priority list used in the proposed SoC balancing strategy is validated, where the cells/MSs with the highest priority (cells/MSs with high and low SoC during discharging and charging, respectively) are activated firstly during discharging/charging. The cells’ traces in Fig. 12c and Fig. 12b are steeply sloped during 0 - 15 min of the charging operation due to the use of $I_h$ (current-prioritised method) to discharge/charge the cells with the highest priority, which increases the speed of their discharging/charging compared to other cells. In Fig. 13 (case study 2), SoC balancing convergence among 2664 cells is achieved in 48 min as shown in Fig. 13a while SoC balancing convergence among 222 Ms is achieved in 38 min as shown in Fig. 13b. During 0 - 58 min, most of the cells’ traces are rising, which indicates that most of the cells/MSs are activated. In case study 1, around 164 Ms (1968 cells) are idle during charging as shown in Fig. 11a, whereas in case study 2, 61 Ms (732 cells) are idle during charging as shown in Fig. 11b. Accordingly, SoC balancing convergence among cells, Ms, and cells in M are achieved using the proposed SoC balancing strategy for both case studies [see Table 4] regardless of the...
existing number of idle cells/\(M_s\) as shown in Fig. 12 and Fig. 13. At any given time, the average SoC among cells/\(M_s\) is different when 3996 cells (333 \(M_s\)) are used compared to 2664 cells (222 \(M_s\)) (e.g., in Fig. 12, the average SoC among the cells/\(M_s\) is 73 % in 60 min, while it is 83.4 % as shown in Fig. 13.

During each \(T_s\), the activated \(M_s\) are distributed into three groups (based on SoC balancing strategy proposed in Section III) by controlling their corresponding switches (\(sw_{az}, sw_{bz}, and sw_{cz}\)) as \(ON\) (1) or \(OFF\) (0) as explained in Subsection B, Section II. \(M_1\) and its corresponding switches are selected to demonstrate the distribution principle of \(M_s\) as shown in Fig. 14. \(Hsw_{az}, Hsw_{bz}, and Hsw_{cz}\) are used to generate a sinusoidal \(V_{out}\) for a three-phase (-1 and 1 for the negative and the positive side, respectively, while 0 for \(OFF\) status). Each \(M\) can be activated in any group to generate any \(V_{out}\). Nevertheless, it can be activated only in a single group to generate a certain \(V_{out}\) every \(T_s\) as shown in Fig. 14 (e.g., at any given time, only one of \(sw_{a1}, sw_{b1}, and sw_{c1}\) is \(ON\). However, \(M_1\) is activated via \(sw_{a1}, sw_{b1}, and sw_{c1}\) at different time steps), \(Hsw_{a1}, Hsw_{b1}, and Hsw_{c1}\) statuses (\(ON\) or \(OFF\)) follow its corresponding switches (\(sw_{a1}, sw_{b1}, and sw_{c1}\), respectively) statuses (e.g., only \(sw_{a1}\) and \(Hsw_{a1}\) are \(ON\) at 13 s whereas \(sw_{b1}, sw_{c1}, Hsw_{b1}, and Hsw_{c1}\) are \(OFF\)).

V. EXPERIMENTAL SET-UP

The experimental work is still going on. Consequently, a general overview of the experimental set-up with some initial results is provided in this paper. The experimental set-up includes twelve cells (Panasonic NCR18650) with a 3.6 V nominal voltage and a 3.35 Ah nominal capacity. Each cell is integrated into an \(L\)-bridge while the four \(L\)-bridges are integrated into three parallel \(H\)-bridges (phase a, phase b, and phase c). These \(L\)-bridges and \(H\)-bridges are located in a single printed circuit board (PCB) as shown in Fig. 17. Each module (a single PCB) is designed for four cells. Note that the final experimental system will include nine PCBs integrated with 36 cells. The converter control and cell SoC balancing algorithm are implemented in a C2000 LAUNCHXL-F28379D device. Switching signals are sent through a shift register (74HC595) / 8-bit serial-in, parallel-out as decimal numbers using the SPI interface. The voltage of each individual cell is measured through a difference amplifier (INA117P) and an analog to digital converter (ADC/MCP3208) using the SPI interface. The general block diagram of the experimental set-up of TCHMMC is presented in Fig. 15. The experimental set-up of TCHMMC is presented in Fig. 16 while the detailed breakdown of a single module/PCB of TCHMMC with its relative switches is presented in Fig. 17. The results obtained from this experimental set-up are presented in Figs. 18-21.

In Fig. 15, in order to implement converter control and SoC balancing algorithm, 12-bit ADCs are used to measure a three-phase current and cells’ voltages during each time step. In addition, a shift register (serial-in, parallel-out) unit is used to overcome the limited number of digital signal pins. In Fig. 16, three modules are used to generate a three-phase voltage where each module is integrated into four cells.
leading to an improvement in the operational efficiency of the SoC balancing strategy. In the proposed topology, one branch instead of three branches (compared to the conventional topology) is used to generate $V_{\text{outa}}$, $V_{\text{outb}}$, and $V_{\text{outc}}$ by integrating each $M$ with three H-bridges connected in parallel. Each cell is independently controlled by linking each one of them with an L-bridge. Accordingly, a three-phase bidirectional direct AC-DC conversion is achieved. Furthermore, a three-phase AC rated active power (60 kW) is generated when 3996 cells (333 $M$s) are used and reduced by two-thirds (2664 cells (222 $M$s)). Accordingly, slightly more than one-third of the total cells/$M$s is idle (compared to the conventional topology). Therefore, the total cost of the BESS, control complexity, size, and losses are reduced by eliminating these idle cells/$M$s from the BESS plant or by using as redundant cells/$M$s. The proposed SoC balancing is, therefore, designed to achieve SoC balancing among cells/$M$s with/without these idle cells/$M$s (case study 1 and case study 2). In the proposed topology, SoC balancing convergence among branches (phases) is not required compared to the conventional topology. The simulation results of the proposed SoC balancing strategy showed a satisfactory performance, where SoC balancing convergence among 3996 cells, 2664 cells, and 333/222 $M$s is achieved in 53 min, 48 min, and 38 min, respectively. During the production of the desired $V_{\text{out}}$ (3.6 kV for a phase), a significant range of $M$s from 164 to 188 and from 142 to 176 of 333 $M$s (case study 1) are idle during charging and discharging, respectively, whereas the idle $M$s ranged from 61 to 84 and from 28 to 56 of 222 $M$s (case study 2) during charging and discharging, respectively. During charging, SoC balancing convergence among 12 cells in $M$ with the lowest average SoC is achieved in 18 min compared to 53 min for 12 cells in $M$ with the highest average SoC. The converter was experimentally validated using a TCHMMC which includes twelve Panasonic NCR18650 cells divided into three modules.

Further studies on improving the accuracy of SoC estimation, reducing control complexity, and adding a further parameter called State-of-Health (SoH) can be performed in the existing SoC balancing strategy.

VI. CONCLUSION

A novel SoC balancing strategy for the proposed topology of a three-phase grid-scale BESS is introduced in this paper. Moreover, a novel cell/$M$ activation algorithm is proposed to minimise the duration needed to activate the cells/$M$s required to generate each level of $V_{\text{outa}}$, $V_{\text{outb}}$, and $V_{\text{outc}}$, thereby

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