The MOMMS Family of Matrix Multiplication Algorithms
Tyler M. Smith and Robert A. van de Geijn

ABSTRACT
As the ratio between the rate of computation and rate with which
data can be retrieved from various layers of memory continues to
deteriorate, a question arises: Will the current best algorithms for
computing matrix-matrix multiplication on future CPUs continue
to be (near) optimal? This paper provides compelling analytical
and empirical evidence that the answer is "no". The analytical re-
sults guide us to a new family of algorithms of which the current
state-of-the-art "Goto’s algorithm" is but one member. The empirical
results, on architectures that were custom built to reduce the
amount of bandwidth to main memory, show that under different
circumstances, different and particular members of the family be-
come more superior. Thus, this family will likely start playing a
prominent role going forward.

KEYWORDS
matrix multiplication, dense linear algebra, performance, caches

ACM Reference format:
Tyler M. Smith and Robert A. van de Geijn. 2019. The MOMMS Family of
Matrix Multiplication Algorithms. In Proceedings of The International Con-
ference for High Performance Computing, Networking, Storage, and Analysis,
Denver, CO, November 17–27, 2019 (SC19), 12 pages.
DOI: 10.1145/nnnnnn.nnnnnnn

1 INTRODUCTION
For almost two decades, the so-called Goto’s algorithm for matrix-
matrix multiplication (MMM) has guided practical implementations
on current CPUs [6, 7]. The algorithm orchestrates computation
so as to keep a packed copy of a roughly square submatrix (block)
of A in the L2 cache and a packed copy of a row panel of B in the
L3 cache. Major innovations of Goto’s algorithm include stag-
ing a block of A in the L2 cache rather than the L1 cache to re-
duce the amount of data movement by allowing the block of A
to be larger, packing the block of A and panel of B into specially-
formatted contiguous buffers for better spatial locality, and show-
ing that translation-lookaside buffer (TLB) misses can be a perform-
ance impediment that is alleviated by reducing the footprint of
the block of A.

For years, the rate of peak computation and the memory move-
ment have been diverging [22], and MMM has been predicted to
soon become a memory-bound operation based on such hardware
trends [2], taking into the hardware requirements for this computa-
tion to be balanced [17]. While Goto’s algorithm is well-suited to

the relative speeds of caches in current memory hierarchies, we
show, through analysis and empirical studies, that this will not
continue to be the case as bandwidths between various memory
layers continue to deteriorate relative to the rate of computation.
Figure 1 reports the attained performance of various implemen-
tations on a custom-built computer that allows the bandwidth to dif-
ferent memory layers to be artificially reduced1. The curve labeled
MOMMS Goto uses Goto’s algorithm and we believe MKL uses
an algorithm similar to it, and the curve labeled MOMMS C3A2C0
uses an algorithm that more effectively utilizes the L3 cache. The
performance degradation of Goto’s algorithm on such an architec-
ture is significant.

As MMM becomes near memory bound, it is essential that algorithms for this extremely widely-used
operation to utilize the memory hierarchy as effectively as possible.

This paper first reviews recent theoretical results by Smith et
al. [26] that establish an (essentially) tight lower bound on the
memory traffic incurred by a MMM under a simple model. It then
makes a number of new contributions:

- With these theoretical results as a foundation, it proposes
  the Multilevel Optimized Matrix-matrix Multiplication Sand-
  box (MOMMS) family of practical algorithms of which Goto’s
  algorithm is a member.
- It analyzes tradeoffs in the number of transfers between
  layers of the memory hierarchy that arise when simulta-
  neously optimizing for multiple levels of cache. These
  tradeoffs are not explained by current state-of-the-art the-
 oretical results.
- It analytically exposes different scenarios under which dif-
  ferent algorithms in the family exhibit beneficial charac-

1Details of the experiment are given in Section 5.
• It empirically demonstrates the benefits of different algorithms on custom-built hardware that allows memory bandwidths to be varied.

Together, these lay the foundation for practical solutions if and when the balance between computation and memory bandwidth changes in the future.

2 THEORY AND FUNDAMENTAL SHAPES

We briefly review the state-of-the-art theoretical lower bounds for the I/O complexity for MMM, and describe algorithms that attain those bounds and thus are optimal for a simple model of a two-level memory hierarchy. These algorithms become our fundamental components from which we compose practical algorithms for multiple levels of cache, in Section 3.

2.1 An I/O lower bound for MMM

Smith et al. [26] starts with a simple model of memory with two layers of memory: a small, fast memory with capacity of $M$ elements and a large, slow memory with unlimited capacity. It shows that any algorithm for ordinary MMM\(^2\) must read at least $2mnk/\sqrt{M} - 2M$ elements from slow memory and additionally write at least $mn - M$ elements to slow memory. Adding these two lower bounds gives a lower bound on the number of transfers between slow and fast memory, called the I/O lower bound, of approximately $2mnk/\sqrt{M}$. Importantly, this lower bound is tight, modulo lower order terms. It improves upon previous work \cite{3,13,15}.

2.2 Resident algorithms for MMM

In \cite{26}, it is shown that three algorithms, named Resident A, Resident B, and Resident C, attain the lower bound on the number of reads from slow memory\(^3\). Additionally, Resident C attains the lower bound on the number of writes to slow memory\(^4\). In each algorithm, the elements of one of the operand matrices are read from slow memory only once, and each of the other two operand matrices is reused approximately $\sqrt{M}$ times each time it is brought into fast memory. While the Resident A algorithm was described as early as 1991 \cite{18}, and all three appear in \cite{10}, their optimality was first noted in \cite{26}.

2.2.1 Resident C. The operation MMM $Z := XY$ can be computed by the sequence of rank-1 updates $Z := x_0y_i^T + x_1y_i^T + \cdots$, where $x_i$ and $y_i^T$ are a row and column of $X$ and $Y$, respectively. This is illustrated in Figure 2 (left), where $Z$ is the square block on the left, $X$ is the middle operand, and $Y$ is the operand on the right. The vectors $x_i$ and $y_i^T$ are represented by the thin partitions of $X$ and $Y$.

Suppose we have (larger) matrices $C$, $A$, and $B$. We compute $C := AB$ in the following way. Partition:

$$C \rightarrow \begin{pmatrix} C_{0,0} & \cdots & C_{0,n-1} \\ \vdots & \ddots & \vdots \\ C_{m-1,0} & \cdots & C_{m-1,n-1} \end{pmatrix}, A \rightarrow \begin{pmatrix} A_0 \\ \vdots \\ A_{m-1} \end{pmatrix}, B \rightarrow \begin{pmatrix} B_0 \\ \vdots \\ B_{n-1} \end{pmatrix}. $$

where $C_{i,j}$ is $m_c \times n_c$, $A_i$ is $m_c \times k$, and $B_j$ is $k \times n_c$, except at the margins. Then we compute the suboperation $C_{i,j} := A_iB_j$, using the described algorithm for $Z := XY$. Now, $C_{i,j}$ is read from slow memory once at the beginning of the suboperation, and resides in fast memory during the rest of the duration, and $A_i$ and $B_j$ are streamed one row and column at a time from slow memory. Each element of each operand is read once for each $i, j$, and there are $\lceil \frac{mnk}{M} \rceil$ such suboperations. Overall, this algorithm incurs $mn$ reads and $mn$ writes for matrix $C$, $\lceil \frac{mnk}{n_c} \rceil$ reads for matrix $A$, and $\lceil \frac{mnk}{m_c} \rceil$ reads for matrix $B$. When $m_c \approx n_c \approx \sqrt{M}$, the I/O cost is $2mnk/\sqrt{M} + 2mn$. The highest ordered term in the I/O cost of the Resident C algorithm is the same as the I/O lower bound for MMM. Thus the algorithm is essentially optimal.

2.2.2 Resident A and B. Similarly, in the MMM $Z := XY$, each column of $Z$ can be computed by the matrix-vector multiplication $z_i := \sum y_i$, where $z_i$ and $y_i$ are columns of $Z$ and $Y$, respectively. This is illustrated in Figure 2 (middle), $Z$, $X$, and $Y$ are the left, middle, and right operands, respectively.

Consider $C := AB$. Partition:

$$C \rightarrow \begin{pmatrix} C_0 \\ \vdots \\ C_{m-1} \end{pmatrix}, A \rightarrow \begin{pmatrix} A_0 \\ \vdots \\ A_{m-1} \end{pmatrix}, \quad B \rightarrow \begin{pmatrix} B_0 \\ \vdots \\ B_{n-1} \end{pmatrix},$$

where $C_i$ is $m_c \times n$, $A_{i,p}$ is $m_c \times k_c$, and $B_{j,p}$ is $k_c \times n$, except at the margins. Then we compute the suboperation $C_i := A_{i,p}B_{j,p}$ using the described MVM-based algorithm for $Z := XY$. In Resident A, $A_{i,p}$ is read from slow memory once at the beginning of the suboperation, and $C_i$ and $B_{j,p}$ are streamed from slow memory one column at a time. The total I/O costs associated with each matrix are: $\lceil \frac{mnk}{k_c} \rceil$ reads and $\lceil \frac{mnk}{k_c} \rceil$ writes of elements of $C$; $mk$ reads of elements of $A$; $\lceil \frac{mnk}{m_c} \rceil$ reads of elements of $B$. If $k_c \approx n_c \approx \sqrt{M}$, the input cost is approximately $2mnk/\sqrt{M} + nk$, and the output cost is approximately $mnk/\sqrt{M}$. The input cost attains near the lower bound on reads from slow memory.

The Resident B algorithm is the obvious symmetric equivalent to the Resident A algorithm, built upon the suboperation in Figure 2 (right). Its I/O costs mirror that of the Resident A algorithm.

The above descriptions “stream” rows and/or columns of two matrices while keeping a block of the third matrix resident in fast memory. Notice that one can instead stream row panels instead of rows and/or column panels instead of columns as long as the “small” dimension of the panel is small relative to the sizes of the block that is resident in fast memory. This still achieves the I/O lower bound modulo a lower order term. This insight becomes crucial when we discuss blocking for multiple levels of memory.

2.3 Algorithms for different shapes of MMM

The number of reads and writes from slow memory for the Resident A, B, and C algorithms depend on the shape of the input matrices: There are cases where one of the algorithms is more efficient than the other two, where we define efficiency by flops per memop (I/O operations). There are $2mnk$ flops performed during

\footnote{$m_c$ and $n_c$ must be slightly less than $\sqrt{M}$ to make room for a row of $A_i$, and a column of $B_j$ in fast memory.}
MOMMS Family of Matrix Multiplication Algorithms

**Figure 2:** The three shapes of MMM exposed by the algorithms Resident C (left), Resident A (middle), and Resident B (right). Each algorithm can be implemented as two loops around its corresponding shape.

MOMMS, and the I/O lower bound is $2mnk/\sqrt{M}$. Thus our goal for efficiency is $\sqrt{M}$ flops per memop. We examine the cases for which algorithms are efficient, assuming that $m$, $n$, and $k$ are at least $\sqrt{M}$.

Resident C is efficient if and only if $k$ is large. It reads $\left\lceil \frac{mnk}{M_c} \right\rceil + \left\lceil \frac{mn}{M_c} \right\rceil + mn$ elements from slow memory during MMM. If $m_c = n_c = \sqrt{M}$, this is approximately $2mnk/\sqrt{M} + mn$. This gives an efficiency of $\left( \frac{\sqrt{M}}{M_c} + \frac{mn}{2k} \right)^{-1}$. When $k$ is large, this is approximately $\sqrt{M}$. We can analyze Resident A and Resident B similarly. Here we ignore the I/O cost for writes. If the sizes of the resident blocks are chosen to be equal to $\sqrt{M}$, Resident B has an efficiency of $\left( \frac{\sqrt{M}}{M_c} + \frac{mn}{2k} \right)^{-1}$, which is approximately $\sqrt{M}$ when $m$ is large. Resident A has an efficiency of $\left( \frac{\sqrt{M}}{M_c} + \frac{mn}{2k} \right)^{-1}$, which is approximately $\sqrt{M}$ when $n$ is large.

This shows that one must choose the right algorithm depending on the shape of the problem. For each of the Resident A, B, and C algorithms, there is a minimal shape that can be implemented efficiently. For Resident C this occurs when $m \approx n \approx \sqrt{M}$, and $k$ is large. For Resident B this occurs when $k \approx n \approx \sqrt{M}$, and $m$ is large. For Resident A this occurs when $m \approx k \approx \sqrt{M}$, and $n$ is large. In each case, the resident matrix fits into fast memory, and the dimension shared by the other two operands should be large so that the cost of moving the resident matrix into fast memory can be amortized.

The fact that one must choose a different algorithm for MMM depending on problem shape and size was previously noted for distributed memory MMM [19, 24], and for hierarchical memory MMM [10, 31].

### 2.4 A balancing act

So far in this section, we have assumed that the costs associated with accessing an element is the same, no matter if it is an element of $A$, $B$, or $C$. In doing so, we arrived at the following strategy: Place a square block of the resident matrix in fast memory, streaming the other two from slow memory. This amortizes the I/O costs associated with the resident matrix, and equalizes the number of accesses of the two streamed matrices.

We now re-analyze the Resident A, B, and C algorithms in the case that the costs associated with accessing elements of the different operands are unequal. This can happen if, e.g., if we add a third layer of memory of intermediate size and access cost. In this case, at the start of a multiplication with submatrices one operand may reside in slow memory while another resides in some intermediate layer. Furthermore, in many cases reads and writes cannot be overlapped (e.g. main memory is often not dual-ported), and hence it is more expensive to access elements of $C$ since $C$ must be both read and written. One way to address this is to select the algorithm where blocks of the operand that is most expensive to access are kept in fast memory as much as possible. Another is to adjust the sizes used for the the resident block in fast memory.

We now walk through an example of the second solution. Suppose we are employing the Resident A algorithm, with an $m_c \times k_c$ block of $A$ in fast memory. If the cost of accessing an element of $B$ costs $\beta_B$, and accessing an element of $C$ costs $\beta_C$, when $m$, $n$, and $k$ are large, the efficiency in terms of flops per memop is $\frac{2mn}{\beta_B} + \frac{2k}{\beta_C}$.

This is maximized when $m_c = \sqrt{\frac{\beta_B}{\beta_C}} M$ and $k_c = \sqrt{\frac{\beta_C}{\beta_B}} M$. With this, the total cost of I/O (rather than the number of accesses) associated with accessing the streamed matrices are equalized and thus the cost minimized (modulo lower order terms).

### 2.5 Summary

The ingredients to an efficient algorithm are: (1) Fill fast memory with a submatrix of one of the operands (the resident matrix), (2) Amortize the I/O cost associated with (1) over enough computation, (3) Choose dimensions for the resident block that equalize the I/O costs (rather then the number of accesses) associated with the two streamed matrices.

## 3 MULTIPLE LEVELS OF CACHE

We now extend the ideas from Section 2 to MMM for computers with multiple layers of fast memory. We carefully build up a particular algorithm for a computer with three layers of memory: a slow main memory, a medium cache, and a fast cache, with each level of cache faster and smaller in capacity than the one before it. We name the fast and medium caches $L_f$ and $L_m$, and name their capacities $M_f$ and $M_m$, respectively.

We start by partitioning the matrices so that the computation is orchestrated as a double loop over a particular subproblem, one of the shapes in Figure 2, that that effectively utilizes the $L_m$ cache. The question then becomes how to implement the subproblem in a way that effectively utilizes $L_f$. 
3.1 A motivating example

For our motivating example, we choose the Resident A algorithm when blocking for \( L_m \).

Effectively utilizing \( L_m \). To effectively utilize \( L_m \), we select the partitioning that casts computation in terms of a double loop around the middle shape in Figure 2. We call this subproblem the \( L_m \) block-panel multiply.

Effectively utilizing \( L_f \). The question now becomes how to orchestrate the \( L_m \) block-panel multiply in a way that effectively utilizes \( L_f \). This suggests again a double loop around one of the shapes in Figure 2. It is not hard to see that creating a double loop that again implements a Resident A algorithm is problematic: Partitioning \( A \) for \( L_f \) would expose panels of \( B \) and \( C \) that by design are too large to fit into \( L_m \), and these panels are used in multiple \( L_f \) subproblems. Either these panels of \( B \) or \( C \) would need to be brought into \( L_m \) multiple times or the sizes of the various matrix partitions would need to be reduced. Either way the effect would be that the operation would no longer be near-optimal with respect to the number of transfers between \( L_m \) and slower levels of memory. We conclude that the block-panel multiply should be implemented in terms of a Resident C or Resident B algorithm. Which of these depends on the choice of the outer and inner loop, which we discuss next.

Choosing the outer loop for the \( L_f \) cache. In order to attain near the lower bound, each element in the two long panels of \( B \) and \( C \) must be used \( \approx \sqrt{M} \) times each time it is brought into \( L_m \). This leads us to first partition along the \( n \) dimension with blocksize \( n_c \), yielding partitions of \( B \) and \( C \) that are small enough to fit into the \( L_m \) cache along with the block of \( A \).

The inner loop for the \( L_f \) cache. The next step is to further partition the matrices to optimize for \( L_f \). The subproblem exposed by each iteration of the \( L_f \) outer loop is a block of \( A \) times a skinny panel of \( B \) updating a skinny panel of \( C \). The \( L_f \) inner loop will partition this subproblem along one of the two dimensions that the \( L_f \) outer loop did not. We can choose either of these. For this example, we will choose the \( k \) dimension (with blocksize \( k_c \)). This \( L_f \) inner loop exposes a new subproblem that we will call the \( L_f \) subproblem. In this case, the \( L_f \) subproblem is a tall and skinny panel of \( A \) times a \( k_c \times n_c \) block of \( B \), updating a tall and skinny panel of \( C \). If \( k_c \approx n_c \approx \sqrt{M_f} \), then the \( L_f \) subproblem corresponds to the furthest left shape seen in Figure 2. Then, the block of \( B \) will reside in the \( L_f \) cache, and the panels of \( A \) and \( C \) will be streamed from lower levels of cache for the duration of this subproblem.

3.2 Building a Family of Algorithms

In the motivating example, we started with a problem resembling the middle shape from Figure 2, and used two loops to partition the problem, resulting in a problem resembling one of the other two problem shapes. This suggests the following methodology to optimize for any number of levels of cache: We begin with one of the three shapes in Figure 2, optimizing for the I/O cost for the \( L_k \) cache. Then, to optimize for the next smaller and faster level of cache, the \( L_{k-1} \) cache, we first partition the problem along the long dimension, and then partition along along one of the other two dimensions. The result is one of the other two shapes shown in Figure 2. We name the outermost of these two loops the \( L_{k-1} \) outer loop and the innermost the \( L_{k-1} \) inner loop. This process is shown in Figure 3.

We note that [10] claimed that it was locally optimal to encounter a subproblem that corresponds to one of the three optimal subproblems at every level of the memory hierarchy. However that paper did not give details on how this could be accomplished, nor did it analyze the claim in terms of any I/O lower bounds.

3.3 Classifying matrix operands and algorithms

The two loops for \( L_{k-1} \) have exposed partitions of matrices that differ in terms of access frequency and size. From these properties, we can classify these different matrix partitions.

The \( L_k \) resident block is the block that is designed to remain and reside in the \( L_k \) cache during the duration of the \( L_k \) subproblem. The other two operands of an \( L_k \) subproblem are called the \( L_k \) streamed panels, as small partitions of the streamed panels are brought into \( L_k \) during an iteration of the \( L_{k-1} \) outer loop, used for computation, and then not used again during the \( L_k \) subproblem.

The \( L_{k-1} \) inner loop partitions the \( L_k \) resident block and one of the \( L_k \) streamed panels. The remaining \( L_k \) streamed panel is left unpartitioned. The matrix partition not partitioned by the \( L_{k-1} \) inner loop is used during every iteration of the \( L_{k-1} \) inner loop. Guided by the principle that each element of the \( L_k \) subproblem should only by read into \( L_k \) once, it must remain in cache during the entire inner \( L_{k-1} \) loop. We name this matrix partition the \( L_k \) guest panel. Compare this to the resident block of the \( L_k \) cache. The elements of the \( L_k \) guest matrix, like the elements of the \( L_k \) resident block, are reused from \( L_k \) across iterations of a loop. The difference is that the \( L_k \) resident block is reused across every iteration of the outer \( L_{k-1} \) loop, and the \( L_k \) guest matrix is reused across the iterations of the inner \( L_{k-1} \) loop.

After the two \( L_{k-1} \) loops, we have exposed one of the three shapes associated with our algorithms Resident A, Resident B, and Resident C. The small block that will then reside in \( L_{k-1} \) will be known as the \( L_{k-1} \) resident block.

The algorithms that arise from our methodology can be identified by the operand that the resident block is from in each level of cache. We introduce a naming convention for the algorithms that states the level of cache and the operand that resides in it. For instance if an algorithm has \( B \) as the resident block of the \( L_2 \) cache, \( A \) as the resident block of the \( L_1 \) cache, and \( C \) as the resident block in registers, it is called \( B_2A_1C_0 \).

3.4 Optimizing for registers

In our family of algorithms, we think of the register file as \( L_0 \): the smallest and fastest level of cache. For practical reasons, it should be treated as a special case. In many implementations of MMM, the innermost kernel implements the Resident C algorithm [7, 11, 29, 30]. There are good reasons for this. The latency of the computation instructions dictates that there is a minimum number of registers that must be used to store elements of \( C \) to avoid the instruction latency becoming a bottleneck. The number of elements of \( C \) that are stored in registers must be at least the product of the
When simultaneously optimizing for multiple levels of cache, there are tensions between I/O costs at the different levels of cache.

4 MULTILEVEL CACHE TRADEOFFS

When simultaneously optimizing for multiple levels of cache, there are tensions between I/O costs at the different levels of cache.

4.1 Optimizing for \(L_{h-1}\) impacts the \(L_h\) I/O cost

When simultaneously optimizing for both \(L_{h-1}\) and \(L_h\), the size of the \(L_h\) resident block is reduced relative to its size when optimizing only for \(L_h\), since larger portions of the \(L_h\) streamed panels must fit in \(L_h\). When optimizing for both \(L_h\) and \(L_{h-1}\):

- At minimum, the \(L_h\) resident matrix and \(L_h\) guest matrix must fit into \(L_h\).
- If \(L_h\) is inclusive, meaning that everything in \(L_{h-1}\) must also be in \(L_h\), then there must also be space in \(L_h\) for the \(L_{h-1}\) resident matrix.
- If \(L_h\) is inclusive and has a LRU policy, then in order for an element to remain in \(L_h\), fewer than \(M_h\) elements may be accessed in between accesses of the element for it to remain in cache and hence every matrix partition exposed by the \(L_{h-1}\) outer loop must fit in \(L_h\).

These conditions represent a tradeoff between optimizing for \(L_h\) and \(L_{h-1}\). The larger \(L_{h-1}\) is, the more data must fit into it, and the smaller the \(L_h\) resident block can be. With the simplifying assumptions that the resident blocks of both \(L_h\) and \(L_{h-1}\) must be square, the I/O cost for \(L_h\) when optimizing for both \(L_h\) and \(L_{h-1}\) can be determined by the ratio \(M_h/M_{h-1}\).

Sometimes, it is counter-productive or of limited value to optimize for \(L_{h-1}\) when optimizing for \(L_h\). In this case:

1. A simple option is to treat \(L_{h-1}\) as if it were smaller than it is, reducing the size of the \(L_{h-1}\) resident block.
2. If \(L_h\) is LRU, another option is to tweak the blocksize for \(L_{h-1}\) slightly. The portions of the \(L_h\) streamed panels that must fit into \(L_h\) alongside the \(L_h\) resident block depends on the tiling of the \(L_{h-1}\) outer loop but not on the blocksize of the \(L_{h-1}\) inner loop. Therefore, one can tweak the shape of the \(L_{h-1}\) resident block accordingly.
3. A third option is that one could "skip" optimizing for \(L_{h-1}\) and instead simultaneously optimize for \(L_h\), and \(L_{h-2}\).

Blocking for the \(L_{h-1}\) cache adversely affects the number of transfers into and out of the \(L_h\) cache but blocking for further (smaller and faster) levels of cache does not, because the entire \(L_{h-2}\) subproblem fits within the data that must be in the \(L_h\) cache.

4.2 Optimizing for \(L_h\) impacts the \(L_{h-1}\) I/O cost

Simultaneously optimizing for \(L_h\) and \(L_{h-1}\) adversely affects transfers into and out of \(L_h\). We now argue that it also has an adverse effect on the transfers into and out of \(L_h\).

When optimizing for only one cache of size \(M\), the streamed matrices are each associated with an aggregate I/O cost of \(\approx mnk/\sqrt{M}\). When optimizing for both \(L_h\) and \(L_{h-1}\), however, the I/O cost associated with the \(L_{h-1}\) resident matrix becomes cubic because each element of the \(L_{h-1}\) resident matrix is moved into \(L_{h-1}\) once per \(L_h\) subproblem.
When optimizing for both $L_h$ and $L_{h-1}$, the I/O cost associated with the $L_{h-1}$ resident matrix will be $\approx mnk/\sqrt{M_n}$, whereas when only optimizing for the $L_h$ cache, the I/O cost associated with the $L_h$ resident matrix is equal to the number of compulsory reads and writes. The I/O costs for the streamed matrices are not affected.

While optimizing for the $L_h$ cache has increased the $L_{h-1}$ I/O cost, optimizing for $L_{h+1}$, $L_{h+2}$, etc., does not affect it, because optimizing for further levels of cache does not reduce the number of times each element is used every time it is brought into the $L_{h-1}$ cache.

### 4.3 Skipping caches

We have seen that tradeoffs occur when simultaneously optimizing for the I/O cost of multiple levels of cache. Sometimes these tradeoffs are too great, so instead of optimizing for both $L_h$ and $L_{h-1}$, one may forego the $L_{h-1}$ cache, and instead simultaneously optimize for $L_h$ and $L_{h-2}$ I/O costs, where the $L_{h-1}$ cache is intermediate between $L_h$ and $L_{h-2}$. We call this skipping the $L_{h-1}$ cache.

When the $L_{h-1}$ cache is skipped, an optimal subproblem is encountered at the $L_h$ level and at the $L_{h-2}$ level, but not at the $L_{h-1}$ level. However, this does not mean that the $L_{h-1}$ is not useful. Recall that the $L_h$ guest matrix is reused during each iteration of the $L_{h-2}$ level, so instead of reusing the $L_{h-1}$ cache, if that cache is skipped.

- In idealized circumstances, only the $L_h$ guest matrix should need to be in the $L_{h-1}$ cache.
- If the $L_{h-1}$ cache is LRU, then a panel of the $L_h$ resident matrix must also fit into the $L_{h-1}$ cache.
- If the $L_{h-1}$ cache is inclusive, then the $L_{h-2}$ resident block must also fit into the $L_{h-1}$ cache.

In this case, the $L_h$ guest matrix is reused from $L_{h-1}$, but is not square, and the I/O cost associated with reading the other two operands is suboptimal. Furthermore, in many cases this panel occupies only a fraction of $L_{h-1}$, reducing its size and further increasing the I/O cost.

Goto’s algorithm is a member of the MOMMS family. It skips optimizing for the $L_3$ and $L_1$ caches. Since $A$ is the resident matrix of the $L_2$ cache, and $C$ is the resident matrix of the registers, Goto’s algorithm is named $A_2C_0$ according to the convention in Section 3.3.

### 5 EXPERIMENTS

We now evaluate algorithms created by our methodology. We do so by performing experiments on architectures with a varying number of levels of cache.

For current CPUs, Goto’s algorithm attains excellent performance [28] that is difficult to exceed despite the fact that it does not attain close to the I/O lower bound on computers with an $L_3$ cache. In order to evaluate the I/O cost of different algorithms, we artificially vary the cost of accessing main memory. In all experiments, we perform double precision MMM.

### 5.1 Experimental setup

We have implemented the described family of algorithms as the Multilevel Optimized Matrix-Matrix Multiplication Sandbox (MOMMS). MOMMS implements algorithms for MMM by composing components like matrix partitioning, packing, and parallelization at compile time. MOMMS is written in Rust [21], a modern system programming language focusing on memory safety. Most of this safety is enforced at compile-time through Rust’s borrow checker. In Rust, memory is freed when it goes out of scope, and there is no garbage collector. From Rust, one can call C functions with very low overhead. For low-level kernels, MOMMS calls the BLIS microkernel [29] coded in C and inline assembly language.

We custom built two computers. One has an Intel i7-7700K CPU with two 8GB DIMMS of DDR4-3200 RAM and a motherboard with an Intel Z270 chipset. The other has an Intel i7-5775C CPU with two 8GB DIMMS of DDR3-2400 RAM and a motherboard with an Intel Z97 chipset. We refer to these computers by their processor names. We chose the Z270 and Z97 chipsets because these are enthusiast motherboards for consumers interested in overclocking, and they provide the ability to change the memory multiplier. The i7-7700K computer has a 4-core Intel Kaby Lake CPU with 64KB $L_1$, 256KB $L_2$, and 6MB $L_3$ caches. We chose this because it is a recent readily available Intel processor with an $L_3$ cache. The i7-5775C is a 4-core Intel Broadwell CPU. It also has 64KB $L_1$, 256KB $L_2$, and 6MB $L_3$ caches. Most notably it has 128MB of eDRAM, functioning as an $L_4$ cache.

All experiments were performed with hyperthreading disabled. A userspace CPU governor was used to set the CPUs to the nominal CPU frequency: 4.2 GHz for the i7-7700K and 3.3 GHz for the i7-5775C.

The bandwidth to main memory can be determined by the product of the number of memory channels, the base clock rate, the number of bytes per transfer, and the memory multiplier. With DDR RAM, this is doubled since it transfers on both the leading and trailing edges of the clock signal. We increase the ratio of the rate of I/O to the rate of computation via the BIOS settings. Reducing the memory multiplier and the number of memory channels decreases the rate of I/O without changing the rate of computation.

### 5.2 Optimizing for the $L_3$ cache

We here describe an algorithm implemented in MOMMS that optimizes for both $L_3$ and $L_2$ labeled $B_3A_2C_0$. We compare this algorithm to our re-implementation of Goto’s algorithm (also implemented in MOMMS), and to vendor and state-of-the-art open source BLAS [4] implementations. Figure 4 compares Goto’s algorithm with other MOMMS algorithms optimized for both the I/O cost of $L_3$ and $L_2$.

We now describe the $B_3A_2C_0$ algorithm as implemented for the i7-7700K and illustrated in Figure 4 (second from the left). First, we partition for $L_3$ cache. The $L_3$ outer loop partitions the matrices in the $n$ dimension with blocksize 768. Then the $L_3$ inner loop partitions in the $k$ dimension, also with blocksize 768. This reveals a $768 \times 768$ block of $B$ that becomes the $L_3$ resident matrix. Next, we partition for the $L_2$ cache. Since $B$ is the $L_3$ resident matrix, the $L_2$ outer loop must be in the $m$ dimension, and it is with blocksize 120.
The $L_2$ inner loop then partitions the $k$ dimension with blocksize 192, making a block of $A$ resident in $L_2$, and a $120 \times 768$ panel of $C$ the guest matrix of $L_3$. We skip $L_1$, since it is a quarter the size of $L_2$, making it not beneficial to optimize for both $L_2$ and $L_1$. The next two loops make a $4 \times 12$ block of $C$ the resident matrix of registers, and a $192 \times 12$ panel of $B$, the guest panel of $L_2$. This guest panel of $L_2$ is designed to be reused in the (skipped) $L_1$ cache. Finally, we call a $4 \times 12$ micro-kernel provided by BLIS [29].

We compare this to Goto’s algorithm with similar block sizes as follows: $n_r$ is 3000, $k_r$ is 192, $m_r$ is 120, $m_r$ is 4, and $n_r$ is 12. Our implementation of Goto’s algorithm uses the same micro-kernel from BLIS as does $B_4A_2C_0$. For both algorithms, we parallelize the second loop around the micro-kernel with 4 threads. This quadruples the bandwidth requirements of our algorithms without increasing the amount of the $L_3$ cache that must be set-aside for elements of $A$ [27].

### Rooflines

The roofline model is a simple model used to give an upper bound on performance based on the arithmetic intensity of an algorithm for a specific computer [32]. The computer is characterized by its rate of computation and the rate at which it can transfer data between main memory and cache. The arithmetic intensity of an algorithm is the number of flops per byte transferred between memory and cache during the execution of that algorithm. When the arithmetic intensity is low it is bandwidth bound, and when the arithmetic intensity is high it is compute bound. The roofline model is thus a plot where the $x$-axis is the arithmetic intensity and the $y$-axis is maximum rate of computation for that arithmetic intensity. The roofline that serves as an upper bound on performance is formed by two linear curves that intersect when the minimum time spent for computation for an algorithm is equal to the minimum time spent for I/O. Algorithms are plotted on the roofline model according to their arithmetic intensity and measured performance as a way to explain their performance and to explain whether or not they could perform better. One can either measure the arithmetic intensity of an algorithm or analyze it. We choose to analyze the arithmetic intensity of the algorithms plotted.

When the matrices are large, Goto’s algorithm has an efficiency of \( \frac{1}{t + \frac{m_r}{256}} \) flops per element. With the block sizes we used, this is 23.26 flops per byte. The algorithm $B_4A_2C_0$, with a $768 \times 768$ block of $B$ in the $L_3$ cache, has an efficiency of 64 flops per byte.

In Figure 5, we show the roofline model for the i7-7700K for the case of one channel of DDR4-800 RAM, and for the case of...
two channels of DDR4-3200 RAM. These cases represent the minimum and the maximum memory bandwidth that we configure the computer for. We plot the modeled efficiency of Goto’s algorithm and the algorithm \( B_3A_2C_0 \) against each algorithm’s measured performance. The roofline plot clearly shows that in the high-bandwidth case, either algorithm is capable of achieving the peak performance of the CPU based on its arithmetic intensity, but for the low-bandwidth case, only \( B_3A_2C_0 \) can. The improved arithmetic intensity is caused by its more effective utilization of the \( L_3 \) cache.

**Varying Bandwidth.** Figure 6 reports the achieved performance of Goto’s algorithm and \( B_3A_2C_0 \) for square matrices, varying the amount of bandwidth to main memory. Packing is often used to achieve spatial locality during an algorithm. Otherwise blocks that are designed to reside in cache may not be able to do so due to cache conflict issues [12]. Packing incurs extra memory movements that do not fundamentally need to happen during MMM. This paper is concerned with the fundamentals of temporal locality during MMM, and hence we sidestep the spatial locality issue during an algorithm. Otherwise blocks that do not fundamentally need to happen during MMM. and hence we sidestep the spatial locality issue during an algorithm. Otherwise blocks that do not fundamentally need to happen during MMM. Packing incurs extra memory movements that do not fundamentally need to happen during MMM.

Comparing with existing implementations. In Figure 7, we compare our implementations of Goto’s algorithm and \( B_3A_2C_0 \) against the DGEMM routines in ATLAS [31] (3.10.3), BLIS (0.2.1), and Intel’s Math Kernel Library (MKL 2017 Release 2) [14]. It would not be fair to compare against implementations of MMM if we did not need to pack, so for this experiment, input matrices are stored in column major order, and our implementations of Goto’s algorithm and \( B_3A_2C_0 \) pack matrices the first time they become the resident or guest matrix at some level of cache. This packing (and the fact that \( C \) is not stored hierarchically for Goto’s algorithm) account for the performance difference seen for the Goto and \( B_3A_2C_0 \) curves between Figures 6 and 7. We see that for high bandwidth scenarios, BLIS, the MOMMS implementation of Goto’s algorithm, and \( B_3A_2C_0 \) all attain roughly 75% of peak, and that MKL outperforms the other implementations. For low bandwidth, implementations that use Goto’s algorithm (or something similar) exhibit poorer performance as they do not effectively utilize the \( L_3 \). In this case, \( C_3A_2C_0 \) performs best, with \( B_3A_2C_0 \) close behind. For large problem sizes, ATLAS performs almost as well as the algorithms implemented in MOMMS that optimize for the \( L_3 \) I/O cost but it does not perform nearly as well for the high bandwidth case.

**5.3 Optimizing for the \( L_4 \) cache**

In this section, we demonstrate that our methodology can be efficiently applied to the Intel i7-5775C, which has four levels of cache, where the \( L_4 \) cache is 128MB of eDRAM. We implemented an algorithm called \( C_4A_2C_0 \) for this architecture. Figure 8 shows the loop ordering and the block sizes used for \( C_4A_2C_0 \). In \( C_4A_2C_0 \), a 3600×3600 block of \( C \) resides in the \( L_4 \) cache, and a 120×192 block of \( A \) resides in the \( L_2 \) cache. We decided to skip blocking for the \( L_3 \) cache, as there is sufficient bandwidth from the \( L_4 \) cache without optimizing for the number of \( L_3 \) cache misses. Nonetheless, the \( C_4A_2C_0 \) outperforms Goto’s algorithm for large problem sizes.

Figure 9 compares the performance of Goto’s algorithm and \( C_4A_2C_0 \) for square matrices across several bandwidths. In this experiment, matrices are stored hierarchically, and so packing is not performed. For high bandwidths, Goto’s algorithm and \( C_4A_2C_0 \) exhibit similar performance, but when bandwidth is low, \( C_4A_2C_0 \) outperforms Goto’s algorithm for large problem sizes.

Figure 10 compares the performance on square matrices of our implementations of Goto’s algorithm and \( C_4A_2C_0 \). Here, matrices are stored in column-major order and accordingly packing is performed when partitions of \( A \) and \( B \) become resident or guest matrices of some level of cache. In \( C_4A_2C_0 \), \( C \) is unpacked when it is
no longer resident in $L_4$. In both Figures 9 and 10, the top of the graphs is the peak computational rate of the CPU.

Because $L_4$ is so large, we ran quite large problems since otherwise the matrices would completely fit in cache. Performance for Goto’s algorithm and MKL do not fall off until the problem size becomes $m = n = k \approx 5000$. We can see that Goto’s algorithm does not optimally use $L_4$ and neither does Intel’s MKL.

While BLIS’s performance does not fall off as severely for the other implementations when the problem size grows, its overall performance is not as high. The algorithmic differences between BLIS and the MOMMS implementation of Goto’s algorithm are parallelism and blocksizes. BLIS uses a larger $k_c$ and a smaller $m_c$ than MOMMS and parallelizes the 2nd and 3rd loops around the micro-kernel, whereas MOMMS parallelizes the 2nd loop around the micro-kernel. Modifying either the parallelism or the blocksizes so that they match that of the MOMMS implementation of $C_4A_2C_0$ algorithm can be very large, so the algorithm does not need much bandwidth from main memory, but even algorithms that do not take advantage of $L_4$ by using such large block sizes benefit from having the 128MB cache. The large capacity cache can facilitate the hiding of latency to main memory, through techniques such as hardware prefetching.

5.4 Algorithms for different shapes of matrices

Algorithm $A_3B_2C_0$ partitions the matrices such that a square block of $A$ is resident in $L_3$ and a block of $B$ is resident in $L_3$. It then calls an inner kernel updating a panel of $C$ whose elements are in $L_4$.
We have developed a new family of algorithms for MMM that effectively utilizes a cache hierarchy with multiple layers of fast memory, using two loops at each level of the memory hierarchy. We then demonstrated performance improvements over state-of-the-art implementations of MMM when I/O cost to main memory is a limiting factor. Algorithms like this are key to delaying the inevitable situation where MMM becomes memory bound.

We chose to focus on potential performance benefits of these algorithms and demonstrated those benefits in our experiments. However memory movements cost far more energy than flops do [25], so algorithms that reduce I/O costs are beneficial for the additional reason that they reduce energy usage.

Many algorithms in libraries that implement higher-level linear algebra, such as LAPACK [1] or libflame [9], take advantage of the fact that MMM implementations in BLAS libraries are efficient when the $k$ dimension is relatively small, on the order of a couple of hundred, as Goto’s Algorithm reaches its maximal efficiency when $k$ is equal to the blocksize $k_c$. We expect future computers to be bandwidth bound when executing MMM in such situations, and algorithms for MMM that have larger blocksizes will be used. To take advantage of algorithms that use larger blocksizes, LAPACK and FLAME can use larger blocksize, however this is currently disadvantageous because the larger their blockizes are, the more time is spent during inefficient unblocked subproblems. According to this line of thought, LAPACK and FLAME would benefit from algorithms that do not suffer from this weakness. One possibility is to use recursive algorithms, as advocated in Pease and Bientinesi [23].

Hard drives and other similarly slow storage devices can be thought of as another layer of the memory hierarchy. Because

6 \hspace{1em} \textbf{SUMMARY}

We have developed a new family of algorithms for MMM that effectively utilizes a cache hierarchy with multiple layers of fast memory, using two loops at each level of the memory hierarchy. We then demonstrated performance improvements over state-of-the-art implementations of MMM when I/O cost to main memory is a limiting factor. Algorithms like this are key to delaying the inevitable situation where MMM becomes memory bound.

We chose to focus on potential performance benefits of these algorithms and demonstrated those benefits in our experiments. However memory movements cost far more energy than flops do [25], so algorithms that reduce I/O costs are beneficial for the additional reason that they reduce energy usage.

Many algorithms in libraries that implement higher-level linear algebra, such as LAPACK [1] or libflame [9], take advantage of the fact that MMM implementations in BLAS libraries are efficient when the $k$ dimension is relatively small, on the order of a couple of hundred, as Goto’s Algorithm reaches its maximal efficiency when $k$ is equal to the blocksize $k_c$. We expect future computers to be bandwidth bound when executing MMM in such situations, and algorithms for MMM that have larger blockizes will be used. To take advantage of algorithms that use larger blockizes, LAPACK and FLAME can use larger blockizes, however this is currently disadvantageous because the larger their blockizes are, the more time is spent during inefficient unblocked subproblems. According to this line of thought, LAPACK and FLAME would benefit from algorithms that do not suffer from this weakness. One possibility is to use recursive algorithms, as advocated in Pease and Bientinesi [23].

Hard drives and other similarly slow storage devices can be thought of as another layer of the memory hierarchy. Because
of this, we believe the methodology in this paper can be used to instantiate out-of-core algorithms for MMM. A major difference between such out-of-core algorithms and the ones in this paper targeting LRU caches is that out-of-core algorithms may require explicit transfers to disk and explicit overlapping of I/O and computation. Future work is to generalize the MOMMS family of algorithms to other dense linear algebra operations, much in the way that Goto’s algorithm [7] was generalized to the rest of the level-3 BLAS [8]. The key point is that most suboperations during the other level-3 BLAS operations (that operate on structured matrices) are regular, unstructured MMM operations [16].

REFERENCES

[1] Edward Anderson, Zhaojun Bai, Christian Bischof, L Susan Blackford, James Demmel, Jack Dongarra, Jeremy Du Croz, Anne Greenbaum, Sven Hammarling, Alan McKenney, et al. 1999. LAPACK Users’ guide. SIAM.

[2] Kent Czechowski, Casey Battaglino, Chris McClanahan, Aparna Chandramowlishwaran, and Richard W Vuduc. 2011. Balance Principles for Algorithm-Architecture Co-Design. HotPar 11 (2011), 9–9.

[3] Jack Dongarra, Jean-François Pineau, Yves Robert, Zhai Shi, and Frédéric Vivien. 2008. Revisiting matrix product on master-worker platforms. International Journal of Foundations of Computer Science 19, 06 (2008), 1317–1336.

[4] Jack J. Dongarra, Jeremy Du Croz, Sven Hammarling, and Iain S. Duff. 1990. A set of level 3 basic linear algebra subprograms. ACM Transactions on Mathematical Software (TOMS) 16, 1 (1990), 1–17.

[5] Gianluca Frison, Dimitris Kouzoupis, Tommaso Sarto, Andrea Zanelli, and Moritz Diehl. 2018. BLASPEO: Basic linear algebra subroutines for embedded optimization. ACM Transactions on Mathematical Software (TOMS) 44, 4 (2018), 42.

[6] Kazushige Goto and Robert van de Geijn. 2002. On reducing TLB misses in matrix multiplication. Technical Report TR-02-55. Department of Computer Sciences, The University of Texas at Austin.

[7] Kazushige Goto and Robert van de Geijn. 2008. Anatomy of high-performance matrix multiplication. ACM Transactions on Mathematical Software (TOMS) 34, 3 (May 2008), 12.

[8] Kazushige Goto and Robert van de Geijn. 2008. High-performance implementation of the level-3 BLAS. ACM Transactions on Mathematical Software (TOMS) 35, 1 (2008), 4.

[9] John A. Gunnels, Fred G. Gustavson, Greg M. Henry, and Robert A. van de Geijn. 2001. FLAME: Formal linear algebra methods environment. ACM Transactions on Mathematical Software (TOMS) 27, 4 (2001), 422–455.

[10] John A. Gunnels, Greg M. Henry, and Robert A. van de Geijn. 2001. A Family of High-Performance Matrix Multiplication Algorithms. In Proceedings of the International Conference on Computational Sciences. Springer-Verlag, 51–60.

[11] Alexander Heinecke, Greg Henry, Maxwell Hutchinson, and Hans Pabst. 2016. LIBXSMM: accelerating small matrix multiplications by runtime code generation. In Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis. IEEE Press. 84.

[12] Greg Henry. 1992. BLAS based on block data structures. Technical Report. Cornell University.

[13] Jia-Wei Hsing and Hsiang-Tsung Kung. 1981. I/O complexity: The red-blue pebble game. In Proceedings of the thirteenth annual ACM symposium on Theory of computing. ACM, 326–333.

[14] Intel. [n. d.]. Math Kernel Library. ([n. d.]). https://software.intel.com/

[15] Dror Irony, Sivan Toledo, and Alexander Tiskin. 2004. Communication lower bounds for distributed-memory matrix multiplication. Journal of Parallel and Distributed Comput. 64, 9 (2004), 1017–1026.

[16] Bo Kågström, Per Ling, and Charles Van Loan. 1998. GEMM-based Level 3 BLAS: High Performance Model Implementations and Performance Evaluation Benchmark. ACM Transactions on Mathematical Software (TOMS) 24, 3 (1998), 268–302.

[17] Hsiang-Tsung Kung. 1985. Memory requirements for balanced computer architectures. Journal of Complexity 1, 1 (1985), 147–157.

[18] Monica S. Lam, Edward E. Rothberg, and Michael E. Wolf. 1991. The cache performance and optimizations of blocked algorithms. In ACM SIGARCH Computer Architecture News. Vol. 19. ACM, 63–74.

[19] Jin Li, Anthony Skjellum, and Robert D. Falgout. 1996. A poly-algorithm for parallel dense matrix multiplication on two-dimensional process grid topologies. Master’s thesis. Mississippi State University. Department of Computer Science.

[20] Tze Meng Low, Francisco D. Igual, Tyler M. Smith, and Enrique S. Quintana-Orti. 2016. Analytical modeling is enough for high-performance BLAS. ACM Transactions on Mathematical Software (TOMS) 42, 2 (2016), 12.

[21] Nicholas D. Matsakis and Felix S. Klock Ii. 2014. The rust language. In ACM SIGAda Ada Letters. Vol. 34. ACM, 183–194.

[22] JD McCalpin. 1995. Memory bandwidth and machine balance in high performance computers. IEEE Technical Committee on Computer Architecture (TCCA) Newsletter (December 1995).

[23] Elmar Peise and Paolo Bientinesi. 2017. Algorithm 979: Recursive Algorithms for Dense Linear Algebra on the ReLAPACK Collection. ACM Transactions on Mathematical Software (TOMS) 44, 2 (2017), 16.

[24] Martin D. Schatz, Robert A. van de Geijn, and Jack Poulson. 2016. Parallel matrix multiplication: A systematic journey. SIAM Journal on Scientific Computing, 38, 6 (2016), C748–C781.

[25] John Shalf, Sudip Dosanjh, and John Morrison. 2010. Exascale computing technology challenges. In International Conference on High Performance Computing for Computational Science. Springer, 1–25.

[26] Tyler M. Smith, Bradley Lowery, Julien Langou, and Robert A van de Geijn. 2019. A Tight I/O Lower Bound for Matrix Multiplication. arXiv preprint arXiv:1702.02017 (2019).
[27] Tyler M. Smith, Robert van de Geijn, Mikhail Smelyanskiy, Jeff R. Hammond, and Field G. Van Zee. 2014. Anatomy of high-performance many-threaded matrix multiplication. In 2014 IEEE 28th International Parallel and Distributed Processing Symposium (IPDPS). IEEE, 1049–1059.

[28] Field G. Van Zee, Tyler M. Smith, Bryan Marker Bryan, Tze Meng Low, Robert van de Geijn, Francisco D. Igual, Mikhail Smelyanskiy, Xianyi Zhang, Michael Kistler, Vernon Austel, John Gunnels, and Lee Killough. 2016. The BLIS framework: Experiments in portability. ACM Transactions on Mathematical Software (TOMS) 42, 2 (2016), 12.

[29] Field G. Van Zee and Robert A. van de Geijn. 2015. BLIS: A framework for rapidly instantiating BLAS functionality. ACM Transactions on Mathematical Software (TOMS) 41, 3 (2015), 14.

[30] Qian Wang, Xianyi Zhang, Yunquan Zhang, and Qing Yi. 2013. AUGEM: automatically generate high performance dense linear algebra kernels on x86 CPUs. In Proceedings of the International Conference on High Performance Computing, Networking, Storage and Analysis. ACM, 25.

[31] R. Clint Whaley and Jack J. Dongarra. 1998. Automatically tuned linear algebra software. In SC’98: Proceedings of the 1998 ACM/IEEE conference on Supercomputing. IEEE, 38–38.

[32] Samuel Williams, Andrew Waterman, and David Patterson. 2009. Roofline: An insightful visual performance model for multicore architectures. Commun. ACM 52, 4 (2009), 65–76.

[33] Kamen Yotov, Xiaoming Li, Gang Ren, MJS Garzaran, David Padua, Keshav Pingali, and Paul Stodghill. 2005. Is search really necessary to generate high-performance BLAS? Proc. IEEE 93, 2 (2005), 358–386.