A new digital predictive control strategy for boost PFC converter

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Abstract: A new digital predictive control strategy for a single-phase boost power factor correction (PFC) converter is presented in this paper, to reduce the harmonic distortion and improve the dynamic response. Based on the converter circuit structure, the values of output voltage and inductor current of next switching cycle are predicted in advance. The steady-state algorithm and the dynamic-state algorithm are implemented respectively, the duty cycle is calculated only via the predicted output voltage and inductor current values during the steady process, and the optimized duty cycle is predicted during the dynamic process, to improve the characters of PFC converter. The single-phase boost PFC converter with the proposed digital predictive control strategy has been implemented via the field programmable gate array (FPGA). The experimental results indicate that the proposed digital control strategy can improve the power factor and the dynamic response of PFC converter simultaneously.

Keywords: power factor correction, digital control, predictive strategy, high power factor, fast dynamic response

Classification: Integrated circuits

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1 Introduction

With the development of electronic technology, power factor correction (PFC) converters have been widely used in switching power conversion systems, to reduce the harmonic pollution and improve the power factor [1]. For a long time, analog control has been the conventional control method [2], while many PFC converters have been implemented by digital control recently [3, 4], due to the advantages offered by digital control, such as programmability, lower sensitivity to parameter variations, and possibilities to improve performance. However, the performance improvement of digital PFC converter is often limited by relatively complex digital calculation, resulting in unacceptable calculation burden in every switching cycle and digital control latency for the whole control loop [5].

Several digital control methods have been proposed to realize the power factor correction function, while simplifying the digital calculation. A digital predictive dead-beat control method is introduced to update the duty cycle through several switching cycles, instead of every switching cycle, so as to reduce the calculation burden [6], but the power factor of PFC converter is obviously decreased. The desired duty cycle for each switching cycle is updated via the values of previous duty cycle, input inductor current, input voltage and output voltage in [7], but the calculation error of the digital control loop is accumulated, and the accuracy of the duty cycle value is reduced. A direct duty cycle calculation algorithm is proposed in [8], to update the duty cycle in advance with low calculation requirement, but the regulation capability is not satisfactory under wide load variation. Meanwhile, many digital control methods have also been proposed to improve the dynamic response of PFC converter, while maintaining high power factor. By utilizing the insensitive region of the analog-to-digital converter (ADC), a dead-zone digital controller is proposed to improve the dynamic response of PFC converter [8], but limit cycle oscillation can be observed. A simple digital filter is designed to filter out the low frequency ripple of output voltage [9], but the digital control loop is unstable.

In this paper, a new digital predictive control strategy for a single-phase boost PFC converter is proposed, to improve the power factor and the dynamic response of digital PFC converter simultaneously. Based on the converter circuit structure, the values of output voltage and inductor current of next switching cycle is predicted in advance, to reduce the affection of the digital control loop latency. Meanwhile, the steady-state algorithm and the dynamic-state algorithm are imple-
mented respectively, according to the different operating conditions. The steady-state algorithm is implemented only via the predicted output voltage and inductor current values, to simplify the current control loop and reduce the digital calculation burden. The dynamic-state algorithm is implemented to predict the optimized duty cycle during dynamic process, to improve the dynamic response of digital PFC converter.

2 Proposed digital predictive control strategy

The boost PFC converter structure with the proposed digital predictive control strategy is shown in Fig. 1. The input voltage $V_{in}$, output voltage $V_o$, input inductor current $i_L$ and output current $i_o$ are sampled by ADCs, respectively. The proposed digital predictive control strategy is implemented to obtain the desired digital duty cycle value via the sampled values. The digital pulse width modulator (DPWM) is utilized to realize the digital-to-analog conversion.

The proposed digital predictive control strategy is derived based on the assumptions that the boost PFC converter operates in continuous conduction mode (CCM) and all the devices and components of PFC converter are ideal. Meanwhile, because the switching frequency of PFC converter is much higher than the line frequency, the input voltage of PFC converter can be assumed as a constant during every switching cycle.

For PFC converter, two operating states are mainly included: the steady-state and the dynamic-state. During the steady-state, the PFC converter is expected to regulate the input current to follow the input voltage perfectly, so as to reduce the harmonic distortion and improve the power factor. During the dynamic-state, fast dynamic response and small output-voltage overshoot are expected for the PFC converter, when input voltage or load current is changed.
2.1 The prediction module

In digitally controlled PFC converter, the corresponding duty cycle value for each switching cycle is often updated during the next switching cycle, because of the existence of the digital control latency [5]. As shown in Fig. 1, whenever the PFC converter is in steady-state or dynamic-state, according to the boost PFC circuit structure, the inductor current of converter cannot change instantaneously, so the relationship of inductor voltage and current can be described as

$$\frac{di_L}{dt} = \frac{V_L}{L} = \begin{cases} \frac{V_{in} - V_o}{L}, & \text{MOSFET is off} \\ \frac{V_{in}}{L}, & \text{MOSFET is on} \end{cases}.$$ (1)

Where $L$ is the inductance of the boost inductor. Meanwhile, the relationship between the output capacitor voltage and current can be also described as

$$\frac{dV_C}{dt} = \frac{i_C}{C} = \begin{cases} \frac{i_L - i_o}{C}, & \text{MOSFET is off} \\ \frac{i_o}{C}, & \text{MOSFET is on} \end{cases}.$$ (2)

Where $V_C$ is the output capacitor voltage, which is equal to the output voltage $V_o$. $i_C$ is the capacitor current and $C$ is the capacitance of the output capacitor.

Based on the relationship mentioned above, if input voltage $V_{in}$, output voltage $V_o$, inductor current $i_L$ and output current $i_o$ of the $k_{th}$ switching cycle are sampled, the inductor current $i_L$ and output voltage $V_o$ of the $(k+1)_{th}$ switching cycle can be predicted in advance, and the principle of prediction module can be described as

$$i_L[k+1] = i_L[k] + \frac{V_{in}[k]}{L} \cdot dT_s + \frac{V_{in}[k] - V_o[k]}{L} \cdot (1 - d) T_s.$$ (3)

$$V_o[k+1] = V_o[k] - \frac{i_o[k]}{C} \cdot dT_s + \frac{i_L[k] - i_o[k]}{C} \cdot (1 - d) T_s \\
= V_o[k] - \frac{i_o[k]}{C} \cdot dT_s + \frac{i_{in}[k] - i_o[k]}{C} \cdot (1 - d) T_s.$$ (4)

Where $T_s$ is the switching period, $d$ is the duty cycle of the $k_{th}$ switching cycle. To reduce the digital calculation error, the inductor current $i_L[k]$ is replaced by the approximate average inductor current $i_{av}[k]$ during the $k_{th}$ switching cycle, and it can be calculated as

$$i_{av}[k] = \frac{3i_L[k] + 2 \cdot \frac{V_{in}[k]}{L} \cdot dT_s + i_L[k+1]}{4}.$$ (5)

Based on the predicted inductor current and output voltage values, the desired duty cycle value for next switching cycle can be calculated and updated in advance, which can reduce the affection of digital control latency and improve the dynamic response of PFC converter.

Regardless of the complicated scheme or the simplified scheme, for digital PFC converter, it is difficult to realize high power factor and fast dynamic response, simultaneously [9, 10]. Considering the different regulation demands for digital PFC converter during the two different operating states, the steady-state algorithm and the dynamic-state algorithm are implemented, respectively.
2.2 The steady-state algorithm

Comparing the output voltage and the reference voltage of PFC converter, if the voltage error between them is smaller than the threshold value, the PFC converter will enter into the steady-state. During such state, the output voltage is expected to be stable near the reference voltage, and the input current is expected to follow the input voltage perfectly.

To regulate the output voltage to the reference voltage, PI compensator is often used [9], and the discrete time control law of the compensator can be described as

\[ v_m[k] = v_m[k-1] + K_p e_v[k] + K_i e_v[k-1]. \] (6)

Where \( v_m[k] \) and \( v_m[k-1] \) are the output values of digital compensator, and \( e_v[k] \) and \( e_v[k-1] \) are the voltage errors between the output voltage and the reference voltage during the \( k_{th} \) and \( (k-1)_{th} \) switching cycle, respectively. To reduce the input current distortion caused by the output voltage ripple, the control bandwidth of digital compensator is often limited in the 10–15 Hz range.

To aim high power factor, the input current should follow the input voltage. Under such condition, the whole PFC converter can be equivalent to the resistance \( R_c \). Meanwhile, when the PFC converter operating in continuous conduction mode, the relationship between the input voltage \( V_{in} \), the output voltage \( V_o \) and the duty cycle \( d \) can be expressed as

\[ V_{in} = V_o (1 - d) i_L R_c. \] (7)

From Ref. [10], assuming \( v_m = (V_o * R_c) / R_e \), (7) can be concluded as

\[ R_s i_L = R_e V_o (1 - d) = v_m (1 - d), \quad 0 \leq t \leq T. \] (8)

Where \( R_s \) is the equivalent current detection resistance of the PFC converter, and \( v_m \) is the output value of the digital compensator. During the steady-state, the desired duty cycle value \( d[k] \) can be derived as

\[ d[k] = 1 - \frac{R_s}{v_m[k]} i_L[k]. \] (9)

Based on (9), the steady-state algorithm is implemented only via the output voltage and input current values. The complicated digital calculation in traditional digital control loop is without need [9]. Meanwhile, because the output voltage and input current values are predicted through the prediction module, the desired duty cycle value for next switching cycle can be calculated and updated in advance.

2.3 The dynamic-state algorithm

When input voltage, output current or reference voltage changes, the voltage error between the output voltage and the reference voltage exceeds the threshold value, the PFC converter will enter into the dynamic-state. During such state, the output voltage is expected to be close to the reference voltage with small output-voltage overshoot as soon as possible.

In the conventional feedback control during the dynamic-state, the duty cycle value is linearly modulated, to reduce the voltage error. Therefore, the duty cycle value cannot change instantaneously, resulting in the inevitable output-voltage overshoot. Meanwhile, many switching cycles are required to reduce the voltage
error of the output voltage step-by-step and make the PFC converter regain the steady-state.

The proposed dynamic-state algorithm is based on the relative value of output voltage and input current to their reference values. As shown in Fig. 1, for the PFC converter, the input voltage after the rectifier bridge is a half-sinusoidal waveform. Near the peak point of input voltage, if large duty cycle value is applied, the output voltage of PFC converter can vary rapidly, so it is possible to improve the dynamic response.

Based on the principle discussed in 2.1, the inductor current and output voltage values of next switching cycle can be predicted. For the specific duty cycle value, if the inductor current of next switching cycle does not exceed the current limit and the output voltage is closer to the reference voltage, such duty cycle value can be regarded as the optimal value and applied for the actual regulation. If not, the dichotomy is applied to calculate the desired duty cycle value to meet the above conditions.

3 Experimental results

A single-phase boost PFC converter with the proposed digital predictive control strategy has been implemented via the field programmable gate array (FPGA). The hardware experimental prototype is shown in Fig. 2.

![Fig. 2. Photograph of the experimental prototype](image)

The parameters of the boost PFC converter are listed as follows: input voltage range $V_{in} = 90–265$ V, output voltage $V_o = 400$ V, line frequency $f_{line} = 50$ Hz, and rated output power $P_o = 300$ W. The switching frequency of converter is 100 kHz. The proposed digital predictive control strategy is coded in very-high-speed integrated circuit hardware description language (VHDL) and implemented on the FPGA control board.

The input voltage and current waveforms of PFC converter during the full load under the steady-state are shown in Fig. 3. From the figure, it can be seen that the input current can follow the input voltage. The reading of the voltmeter shows the power factor value is 0.992. The PFC converter based on the proposed digital control strategy can achieve high power factor under the steady-state.

The dynamic responses of PFC converter with the proposed digital predictive control strategy for load variation are shown in Fig. 4(a) and Fig. 4(b), respectively.
From the figure, it can be seen that the PFC converter with the proposed strategy has fast dynamic response and small output-voltage overshoot.

Table I shows the performance comparison with previously reported works. From the table, it can be observed that the PFC converter with the proposed digital control strategy has excellent performance, including high power factor, fast dynamic response and small output-voltage overshoot.

From the figure, it can be seen that the PFC converter with the proposed strategy has fast dynamic response and small output-voltage overshoot.

Table I. Performance comparison

|                                | [8]  | [9]  | [10] | This Work |
|--------------------------------|------|------|------|-----------|
| Input Voltage (VAC)            | 55   | 110  | 156  | 220       |
| Output Voltage (V)             | 100  | 375  | 230  | 400       |
| Output Power (W)               | 300  | 250  | 300  | 300       |
| Switching Frequency (kHz)      | 400  | 200  | 100  | 100       |
| Boost Inductor (mH)            | 0.1  | 0.75 | 2    | 1         |
| Filter Capacitor (µF)          | 550  | 100  | 440  | 440       |
| Power Factor                   | 0.990| 0.980| 0.985| 0.992     |
| (Input Voltage/Power)          | (55 V/300 W) | (110 V/250 W) | (156 V/300 W) | (220 V/300 W) |
| Dynamic Response (ms)          | 130  | 120  | 100  | 80        |
| Overshoot (%)                  | 3    | 4.6  | 5    | 3.5       |
| Load Change (%)                | 60 → 100 | 60 → 100 | 50 → 100 | 50 → 100 |
4 Conclusions

This paper presents a new digital predictive control strategy for a single-phase boost PFC converter. Based on the circuit structure of the boost PFC converter, the values of output voltage and inductor current of next switching cycle is predicted in advance. According to the different regulation demands for the different operating conditions, the steady-state algorithm and the dynamic-state algorithm are implemented, respectively, to improve the characters of digital PFC converter. The single-phase boost PFC converter with the proposed digital predictive control strategy via the FPGA control board has been implemented, to verify the effectiveness and validity of the proposed digital control strategy. The experimental results indicate that the proposed digital control strategy can improve the power factor and the dynamic response of digital PFC converter simultaneously.