Analysis on One-Stage SSHC Rectifier for Piezoelectric Vibration Energy Harvesting

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Abstract

Conventional SSHI (synchronized switch harvesting on inductor) has been believed to be one of the most efficient interface circuits for piezoelectric vibration energy harvesting systems. It employs an inductor and the resulting RLC loop to synchronously invert the charge across the piezoelectric material to avoid charge and energy loss due to charging its internal capacitor ($C_P$). The performance of the SSHI circuit greatly depends on the inductor and a large inductor is often needed; hence significantly increases the volume of the system. An efficient interface circuit using a synchronous charge inversion technique, named as SSHC, was proposed recently. The SSHC rectifier utilizes capacitors, instead of inductors, to flip the voltage across the harvester. For a one-stage SSHC rectifier, one single intermediate capacitor ($C_T$) is employed to temporarily store charge flowed from $C_P$ and inversely charge $C_P$ to perform the charge inversion. In previous studies, the voltage flip efficiency achieves 1/3 when $C_T = C_P$. This paper presents that the voltage flip efficiency can be further increased to approach 1/2 if $C_T$ is chosen to be much larger than $C_P$.

I. INTRODUCTION

Along with the development of Internet of Everything, wireless sensing networks (WSN) act as essential roles interconnecting between the real world and the Internet. Although electrochemical batteries have remained the primary energy sources for such systems due to the high energy density, certain sensors and sensor systems require to operate over significant periods of time much longer than the lifetime of electrochemical batteries. Battery usage may be both impractical and costly due to the requirement for periodic re-charging and/or replacement [1]–[4]. In order to address this challenge and extend the operational lifetime of wireless sensors, there has been an emerging research interest on harvesting ambient vibration energy.

Piezoelectric materials are widely used in vibration energy harvesters (VEH) as mechanical-to-electrical transducers due to their relatively high power density, scalability and compatibility with conventional integrated circuit technologies [5]. MEMS technology is also widely used for piezoelectric vibration energy harvesters and different kinds of resonant sensors [6]. A typical piezoelectric VEH can provide a power density of around 10 - 500 $\mu$W $\cdot$ cm$^{-2}$, which sets a significant constraint on designing the associated power conditioning interface circuit. The interface circuit not only must consume ultra low power, but it also should be able to recover the power as effectively as possible from the piezoelectric transducer (PT). Full-bridge rectifiers are widely used in commercial energy harvesting systems due to their simplicity and stability; however, they set high threshold voltages for the generated energy to be extracted by the circuit [7]–[9].

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II. SSHC INTERFACE CIRCUIT

In order to improve the power efficiency and minimize the charge waste due to charging \( C_P \), many active interface circuits have been reported, including MPPT (maximum power point tracking) \[10\]–\[12\], active rectifications, etc \[13\]–\[15\]. Among all interface circuits for piezoelectric VEH, SSHI (Synchronized Switch Harvesting on Inductor) rectifier, proposed by Badel et al \[16\], is one of the most efficient circuits with nearly no charge waste (if the inductor is chosen large enough). It performs synchronous charge inversion on \( C_P \) through an RLC system using an inductor controlled by synchronized switches. However, the limitation of the SSHI rectifier
is the need for a large off-chip inductor. This section presents the design of a rectifier, named as synchronized switch harvesting on capacitor (SSHC), which performs the energy extraction using switched capacitors instead of inductors.

Fig. 2 shows the design of a one-stage SSHC rectifier where a temporary charge storage switched capacitor $C_T$ is used to synchronously flip the voltage $V_{PT}$. In order to perform the charge inversion, five analogue switches driven by three pulse signals ($\phi_p$, $\phi_0$ and $\phi_n$) are used. The three non-overlapping switching signals are synchronously generated to turn ON the five switches sequentially in a given order. The order of the three pulses depends on the polarization of the voltage $V_{PT}$.

Fig. 3 shows the working principle of the one-stage SSHC rectifier. Before $I_P$ reaches zero-crossing point, the generated charge by the piezoelectric transducer flows into the storage capacitor $C_S$, as shown in first sub-figure. The polarization of voltage across the piezoelectric transducer is assumed that $V_{PT} > 0$; hence the top and the bottom diodes are conductive and $V_{PT} = V_S + 2V_D$ during this time. At the moment of $I_P$ zero-crossing point, a pulse $\phi_p$ is generated to let some charge in $C_P$ flow into $C_T$. At the next phase, $\phi_0$ turns ON the switch across the piezoelectric transducer and clears the remaining charge in $C_P$. At the phase of $\phi_n$, $C_T$ is connected to the piezoelectric transducer in an opposite sense, hence $V_{PT}$ goes to a negative value and a part of charge is inverted as a result. After the phase $\phi_n$, the polarization of $I_P$ changes and $V_{PT}$ goes to $-(V_S + 2V_D)$ until the middle two diodes become conductive to start charging $C_S$ again. In the voltage inversion process shown in Fig. 3, the order of the three signals is $\phi_p \rightarrow \phi_0 \rightarrow \phi_n$ because $V_P > V_N$ before the zero-crossing moment and $V_{PT}$ is aimed to be inverted from $V_S + 2V_D$ to a negative value. While in the other case of $V_P < V_N$, the order of the three signals should be $\phi_n \rightarrow \phi_0 \rightarrow \phi_p$.

Fig. 4a shows the simulated waveforms of $V_{PT}$, $\phi_p$, $\phi_0$ and $\phi_n$ for five periods of $I_P$. For each zero-crossing moment, the three pulse signals are generated sequentially and it can be seen that $V_{PT}$ is partially inverted. Fig. 4b presents the voltage inversion in more detail while $V_{PT}$ is inverted from positive to negative. In this case, the switch $\phi_p$ is first turned ON and the capacitors,
Fig. 3: Working principle of proposed SSHC rectifier to perform

\( C_P \) and \( C_T \) are connected in the same polarization. From the waveform of \( V_{PT} \), it can be seen that it goes down a little because the charge in \( C_P \) is shared between the \( C_P \) and \( C_T \). At the \( \phi_0 \) phase, \( C_P \) is shorted and the remaining charge in it is cleared; hence \( V_{PT} \) goes to 0 V. At the \( \phi_n \) phase, \( C_T \) and \( C_P \) are connected in an polarization opposite to the phase \( \phi_p \). At this state, some charge in \( C_T \) flows into \( C_P \) until they have the same voltage values across them and \( V_{PT} \) goes to a negative value as a result. In the simulation, \( V_{PT} \) equals to 2.4 V before the zero-crossing moment and it goes to \(-0.8\) V after the inversion process. Fig. 4c shows waveforms while \( V_{PT} \) is inverted from negative to positive and the order that the three pulse signals to be generated is \( \phi_n \rightarrow \phi_0 \rightarrow \phi_p \). In addition to the order, the three signals should also be non-overlapping to avoid any unwanted charge flow.

A. Performance analysis with \( C_T = C_P \)

As discussed, the SSHC rectifier is able to invert some charge stored in \( C_P \) and it is useful to calculate how much charge is inverted and the condition to achieve this performance. Before
When a zero-crossing moment occurs, it is assumed that $V_{PT}$ is positive and it equals to $V_S + 2V_D$, noted as $V_0 = V_S + 2V_D$ for simplicity. $C_T$ is assumed to have no charge at the beginning hence $V_T = 0$ V. At the first zero-crossing moment of $I_P$, $\phi_p$ is first be turned ON because $V_{PT}$ is positive. $C_P$ and $C_T$ are connected and the charge flows into $C_T$ until the voltages across the two capacitors are equal. As the total charge keeps unchanged, the voltage across $C_P$ and $C_T$ at the end of the first phase is:

$$V_{PT1} = V_{T1} = \frac{C_P}{C_P + C_T}V_0$$  \hspace{1cm} (2)

At the second phase, a pulse $\phi_0$ is generated. The remaining charge in $C_P$ is cleared and the charge in $C_T$ is unchanged. Hence, the voltage across $C_P$ and $C_T$ at the end of the second phase is:

$$V_{PT2} = 0$$

$$V_{T2} = V_{T1} = \frac{C_P}{C_P + C_T}V_0$$  \hspace{1cm} (3)

At the phase $\phi_n$, $C_T$ is connected with $C_P$ again in an opposite sense to charge $C_P$ to a negative voltage. As the total charge in the two capacitors is the remaining charge in $C_T$ shown in (3), hence the voltages of $V_{PT}$ and $V_T$ at the end of this phase are:
\[ V_{PT3} = -V_{T3} = -\frac{C_PC_T}{(C_P + C_T)^2}V_0 \] (4)

It can be seen that \( V_{PT} \) is a negative value at the end of the zero-crossing moment. By setting the derivative of the expression in (4) at 0, it can be found that \( V_{PT3} \) attains its minimum value while \( C_T = C_P \). Therefore, the minimum value of \( V_{PT} \) at the end of the first charge inversion is:

\[ V_{PT3} = -V_{T3} = -\frac{1}{4}V_0 \quad \text{(while } C_P = C_T \text{)} \] (5)

The resulting voltage in (5) is obtained after the first charge inversion and the initial voltage across \( C_T \) is assumed at 0 V at the beginning. However, before the second zero-crossing moment, \( V_T \) is no longer 0 V, but \( \frac{1}{4}V_0 \). \( V_{PT} \) now equals to \( -V_0 \) because it needs to be inverted from negative to positive. Assuming \( C_T = C_P \) is chosen for future calculations, \( V_{PT} \) and \( V_T \) values after each phase of \( \phi_n \), \( \phi_0 \) and \( \phi_p \) at the second charge inversion stage are:

\[
\begin{align*}
\text{before } \phi_n : \quad & V_{PT} = -V_0, \quad V_T = \frac{1}{4}V_0 \\
\Rightarrow \text{after } \phi_n : \quad & V_{PT} = -V_T = -\left(\frac{1}{4} + 1\right)\frac{1}{2}V_0 \\
\Rightarrow \text{after } \phi_0 : \quad & V_{PT} = 0 V, \quad V_T = \left(\frac{1}{4} + 1\right)\frac{1}{2}V_0 \\
\Rightarrow \text{after } \phi_p : \quad & V_{PT} = V_T = \left(\frac{1}{4} + 1\right)\frac{1}{4}V_0 = \left(\frac{1}{4}\right)^2 + \frac{1}{4}V_0 = \frac{5}{16}V_0
\end{align*}
\] (6)

As \( \frac{5}{16} > \frac{1}{4} \), more charge is inverted in the second zero-crossing moment compared to the first one. Due to the accumulation of remaining charge in \( C_T \), the resulting \( |V_{PT}| \) at the end of the \( n^{th} \) inversion stage is:

\[
|V_{PT}| = \left(\left(\frac{1}{4}\right)^n + \cdots + \left(\frac{1}{4}\right)^2 + \frac{1}{4}\right)V_0 = \sum_{1 \leq i \leq n} \left(\frac{1}{4}\right)^iV_0 = \frac{\frac{1}{4} - \left(\frac{1}{4}\right)^n}{1 - \frac{1}{4}}V_0
\]

\[
\Rightarrow \lim_{n \to \infty} |V_{PT}| = \frac{1}{3}V_0
\] (7)

While \( n \) tends to infinity, \( |V_{PT}|_{n \to \infty} = \frac{1}{3}V_0 \), which means one third of charge can be inverted theoretically while \( C_T = C_P \). Fig. [5] shows the simulated voltage flip efficiencies for the first 10 flip cycles when \( C_T = C_P \). It can be seen that the flip efficiency goes fast to approach 1/3 after several cycles.
Fig. 5: Voltage flip efficiency for the first 10 flip cycles when \( C_T = C_P \).

B. Performance analysis with \( C_T >> C_P \)

Since \( C_T \) is assumed to be off-chip implemented, it is possible to achieve \( C_T >> C_P \) with a tiny SMD capacitor for \( C_T \) because \( C_P \) is usually as small as several nF. When \( C_T >> C_P \), the charge stored in \( C_T \) will accumulate much slower. However, after sufficient number of flip cycles, voltage across \( C_T \) will approach half of the voltage across \( C_P \) before flipping starts. Since \( C_T \) is very large, the voltage across \( C_T \) barely decreases after charge is dumped back from \( C_T \) to \( C_P \) to finish voltage flipping. In this case, the remaining voltage across \( C_P \) keeps almost constant. Hence, the voltage flip efficiency can be as high as 50% in this case.

Fig. 6 shows the simulated voltage flip efficiencies for the first 300 flip cycles when \( C_T >> C_P \). In this simulation, \( C_T = 100C_P \) is used. From this figure, it can be seen that the flip efficiency takes much more flip cycles to achieve the optimal level compared to the Fig. 5. This is because \( C_T \) is much larger now and it needs more charge from \( C_P \) to charge \( C_T \) to the sufficient level of voltage. The figure shows the voltage flip efficiency approaches 50%, which is higher than 1/3, simulated for the case \( C_T = C_P \).

III. Conclusion

An SSHC (synchronized switch harvesting on capacitor) rectifier with one switched capacitor for piezoelectric vibration energy harvesters is analyzed in this paper. Similar to most of other highly-efficient active rectifiers (such as SSHI), it performs synchronous voltage inversion across the piezoelectric transducer every half cycle to minimize energy loss due to discharging and charging the internal capacitor. However, different from those rectifiers, the SSHC rectifier does not employ any inductor to perform the voltage inversion; it utilizes a capacitor instead. In previous studies, The capacitance of the employed capacitor is suggested to be equal to the internal capacitor of the piezoelectric transducer in order to achieve the performance to invert
1/3 of charge. In this paper, the voltage flip efficiency is simulated to be up to 50% when the capacitance of the switched capacitor $C_T$ is much higher than the internal capacitor of the piezoelectric transducer $C_P$.

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