Research on high precision ADC test based on modular hardware

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Abstract. The design of digital systems in modern communication systems, network transmission systems, and computer multimedia systems has developed by leaps and bounds. The speed and accuracy of the interface circuit between analog and digital have become the key and bottleneck for the vigorous development of digital systems in the future. Correspondingly, the requirements for high-precision ADC performance testing technology and functional verification schemes are also getting higher and higher, and they have gradually been upgraded to an important technical obstacle that needs to be resolved, blocking the innovation of information technology in my country. This thesis first briefly introduces the static and dynamic test principles and techniques of high-precision ADC chips, summarizes the performance indicators of ADCs, and expounds the definitions of commonly used test parameters in more detail. Subsequently, modular equipment was used to build a high-performance test platform and a functional verification platform, and a software and hardware test platform was built with PXI modular equipment as the core to complete the system debugging and data processing of each part. The static parameters, Dynamic parameter indicators are measured and analyzed. The test verification system and research program of this program show that it meets the key index test and functional characteristic verification of high-precision ADC, and its test method has good flexibility, completeness, programmability, and versatility.

1. Introduction

Digital discrete signals 0 and 1 are the main ways for digital circuits to process signals. However, the various forms of realistic information surrounding us are basically displayed in the state of continuous analog signals. In order to obtain the digital signals, we need to process in the circuit system. In digital systems, the important role of analog-to-digital conversion technology plays a decisive role. When
building a bridge between the analog world and the digital world, the interface circuit between analog and digital, ADC (Analog-to-Digital Converter), is indispensable. The speed and accuracy of ADC will greatly restrict the data processing capability of digital systems. At the same time, the requirements for high-precision ADC performance testing techniques and functional verification solutions are getting higher and higher. Due to the performance characteristics of high-precision ADCs, some external environmental factors, such as clock jitter, signal driving capability, power supply noise crosstalk, will force its performance to degrade, thereby increasing the difficulty of performance testing. In summary, it can be seen that the research on the performance test technology of high-precision ADC has great practical significance[1-3].

2. High-precision ADC test principle

There are several different architectures for ADCs. The three most common ADC architectures are successive approximation registers (SAR), delta integral (ΔΣ), and pipeline converters[4]. Each type of converter can convert an analog signal into a digital output, but there are subtle differences in the implementation process. SAR samples and saves the analog input, then converts it into a digital signal and outputs it. The sigma-delta converter takes the average value of the samples over a period of time, and then converts it into a digital signal. The pipeline converter divides the conversion process into multiple stages to achieve ultra-fast conversion speed. Each of these converters has advantages and disadvantages. The SAR architecture is easy to use and usually has the advantages of low power consumption, low latency and high accuracy. The sigma delta converter has the advantages of extremely high resolution, high stability, low power consumption and low cost, but its operating speed is much lower than that of SAR and pipeline architecture. The working speed and bandwidth of the pipelined ADC are relatively high, but the resolution is low, and more power consumption is required[5,6].

The main indicators of ADC are divided into two categories: static indicators and dynamic indicators. The static indicators mainly include: Differential Non-Linearity (DNL)、Integral Non-Linearity (INL)、Offset Error、Full Scale Gain Error, etc[7,8]. The dynamic indicators mainly include: Total harmonic distortion (THD), Signal-to-noise plus distortion (SINAD), Effective Number of Bits (ENOB), Signal-to-noise ratio (SNR) and Spurious free dynamic range (SFDR).

There are different methods for testing ADC structure and different indicators. The static index of ADC is calculated indirectly by the histogram statistics of the amplitude distribution of the sampling data of the sine wave. The dynamic index of the ADC is calculated indirectly by performing FFT spectrum analysis on the sampled data of the sine wave. An ideal sine wave is sampled by A/D and then subjected to spectrum analysis. It may become the shape as shown in the figure below. In addition to the main sine wave component, it also produces a lot of noise, harmonics and spurs. By calculating these components, you can get the dynamic parameters of the ADC[9].

2.1. Principles and techniques of static testing

In the static test, we mainly discuss the test principles of DNL and INL. For ADC, each digital code output corresponds to a small input analog range[10]. When the input voltage is within this range under ideal noise-free conditions, the ADC output will maintain the same digital code. All digital codes (except the maximum and minimum) correspond to the same analog range, and the ideal value is recorded as 1 LSB. This process of converting a certain range of voltages into the same output value will introduce so-called "quantization errors."

The actual ADC cannot always obtain the ideal transfer characteristic curve due to the working principle, design defects, process accuracy and other reasons. The voltage range corresponding to each digital code (hereinafter referred to as the code width) is not always strictly equal to the LSB. This process of converting a certain range of voltages into the same output value will introduce so-called "quantization errors."

Differential nonlinearity (DNL) is defined as: the largest difference between two adjacent scales of ADC is called differential nonlinearity. Unit is LSB. Integral nonlinearity (INL) is defined as: the error...
value of the point where the error between the analog value and the real value corresponding to the ADC device at all numerical points is the largest, that is, the maximum distance that the output value deviates from the linearity. Unit is LSB. There are also many methods for calculating nonlinear differential and integral errors, including: back-to-back method, intersection graph method, servo loop method, etc. The method of calculating INL and DNL is the histogram method, which counts the ADC digital output and draws a histogram. The input signal uses a linear or sine histogram. The test method is: 1. Output no less than 20 analog signals for each digital code, and increase them one by one. 2. Calculate the actual number of each digital code and record it as $h(n)_{ACTUAL}$. 3. Calculate the number of theoretical occurrences of each digital code and record it as $h(n)_{THEORETICAL}$. 4. Calculate the non-linear DNL(n) of each digital code, and integrate to get INL.

$$DNL(n) = \frac{h(n)_{ACTUAL}}{h(n)_{THEORETICAL}} - 1$$

According to the different signal sources, there are Ramp and Sinewave test methods, the differences are:

1) The Ramp test method requires the signal source to emit a Ramp or triangle wave, and its static performance is better; the Sinewave test method uses a sine wave as the signal source, which requires the instrument to have better dynamic performance.

2) Compared with the triangular wave signal source, since the probability of the input signal falling in each digital code area is no longer equal, the calculation method of DNL is different. See the corresponding section for details.

3) For the test of high-precision ADC, the Ramp test method will be faster than the Sinewave test method.

The input signal of Ramp test method is shown in the figure below:
The period of the scanning source and the setting of the ADC sampling rate need to ensure that an average of 20 points can fall within each digital code range in a period of scanning (corresponding to the DNL measurement accuracy of 0.05 LSB); or the source frequency is not the ADC sampling rate. There is no common divisor for the two harmonics, and then a multi-period measurement is performed to achieve a similar effect. As mentioned earlier, it is very difficult to obtain a triangular wave with high linearity, and it will take a long time to test a high-precision ADC.

For the Ramp test method, theoretically, the histogram distribution of each code output should be uniform, but there must be deviations in practice. As shown below:

![Comparison between actual and ideal ADC output coding](image)

Figure 3 Comparison between actual and ideal ADC output coding

The algorithm is relatively simple. The calculation of DNL is to calculate the actual code distribution—calculating the number of ideal codes, which can be calculated according to formula 1, and INL is the accumulation of DNL. The histogram test method using a sine wave as a signal source is more general, because a sine wave with high linearity is easier to obtain (more use of band-pass filters and other methods to improve linearity), and the test time is much less. The amplitude and offset of the sine wave need to be adjusted so that the swing of the signal covers the entire input range of the ADC and slightly exceeds the range, resulting in clipping. How much it exceeds requires experience; especially for bias adjustment, it is necessary to ensure that the midpoint of the waveform is exactly the same as the midpoint of the ADC measurement range, which can be confirmed by whether the ADC upper and lower half-scale counts are close to the same. It is necessary to grab enough points to make the code distribution close to the theoretical curve (as shown in the figure below). The measured 14-bit requires 1M points or more, and 18-bit requires 4M or more. When calculating, discard the codes at both ends (the largest and smallest parts). Because the conversion is too fast or too slow at both ends, there is a certain error.

\[
p(n) = \frac{1}{\pi} \left[ \sin^{-1} \left( \frac{V_{FS}(n - 2^{N-1})}{A \cdot 2^{N}} \right) - \sin^{-1} \left( \frac{V_{FS}(n - 2^{N-1})}{A \cdot 2^{N}} \right) \right]
\]

(2)

This equation is represented by the figure below. Note that the probability of sine wave peaks near ±VFS increases because dv/dt is less than at the zero-crossing point where dv/dt is the highest (fewer clicks per box) (each Boxes with fewer clicks)

![Equation 2 is shown in the figure](image)
For sine wave input, the theoretical number of clicks for nTH encoding is

\[ h(n)_{THEORETICAL} = p(n)M_T \]  

(3)

The DNL error corresponding to this code is

\[ DNL(n) = \frac{h(n)_{ACTUAL}}{p(n)M_T} - 1 \]  

(4)

In order to obtain accurate results, several precautions must be taken. Sine wave histogram test, such as the triangle test waveform discussed above, the sine wave frequency must not be the sub-harmonic of the sampling frequency. When choosing the amplitude of sine wave input A, the ADC should be slightly overdriven at both ends of its range. Then, the sine wave should be adjusted to eliminate the influence of the offset so that there are equal clicks above and below the middle scale point, that is, the number of clicks from code 0 to code 2N-1-1 should be equal to the number of clicks from code 2N-1 to Number of hits for code 2N-1

\[ \sum_{n=0}^{2^{N-1}-1} h(n) = \sum_{n=2^{N-1}}^{2^N-1} h(n) \]  

(5)

Finally, the value of A should be estimated using the actual histogram data in the following equation

\[ A_{ESTIMATE} = \frac{V_{FS}}{\sin \left( \frac{M_T}{2} \right) \left( \frac{h(0) + h(2^{N-1}-1)}{2} \right)} \]  

(6)

The estimated value of A predicted by Formula 6 is applied to Formula 2 to calculate the p(n) value of each code. It is important that these steps take into account the ADC gain and offset in the actual test setup in order to use Equation 2 to obtain an accurate p(n) value for the final DNL calculation.

The dynamic index of ADC refers to the frequency spectrum analysis of the input analog sine wave digitized sampling data. ADC dynamic index test process: 1. SMU provides correct Vref. 2. The signal source provides a sine signal of full scale and specified frequency according to the ADC manual. 3. Digital Instruments obtains the ADC digital pin output, and performs window function and FFT processing on the signal. Among them, the 7th order Blackman-Harris is the best window function. 4. According to the dynamic test items, different calculation formulas are used. 5. Change the frequency and repeat the above test items.

3. Realization of high-precision ADC test system

To verify these many indicators of the ADC, the basic method is to input an ideal signal to the input of the ADC, and then collect and analyze the data after the ADC conversion. Therefore, the performance test of the ADC requires the cooperation of multiple instruments and the use of software. Analyze the test results.

3.1. Test system hardware structure

The basic principle of ADC test is: give ADC a high-precision signal source, and then first collect and analyze the digital data obtained after ADC conversion. So indispensable in the test system are its analog
output equipment and digital acquisition equipment, in addition to power supply, reference voltage, sampling clock and so on. The components of each part include: arbitrary signal generator, high-precision signal source, high-precision source measurement unit, digital instrument for IC control and data analysis, high-precision synchronous clock source (optional), input matching circuit (optional), Filter (optional).

The hardware structure diagram of ADC automatic test platform is as follows:

![Figure 6 Block diagram of ADC automatic test system](image)

3.2. Test system software

The test system software includes the driver, soft panel, debugger, user test program development environment and test program library for each instrument module.

NI LabVIEW is the most popular system design software in the instrument automation industry. Using a graphical development environment to build custom applications, through programming control can reduce human errors in repeated measurements and save the time required for testing. This article mainly uses LabVIEW to realize test automation. The automation of testing mainly relies on the device driver and instrument application program interface (API) provided by LabVIEW: The device driver cooperates with the computer operating system to establish a communication mechanism between the computer and PXI hardware; the instrument API is a set of Easy-to-understand high-level functions are used in LabVIEW to control and communicate with the instrument. Use LabVIEW for programming, get the data measured by the automated test system through initialization, configuration of the instrument, execution of operations, shutdown of the device, and error handling, and further analyze and process the test data to calculate the performance parameters of the ADC. The above test process only needs to be controlled by a well-written LabVIEW program, which realizes the automatic test of ADC.

The test system software can configure the signal source, clock, digital module, power supply module and test items, and set the ADC sampling rate, sampling points, resolution, etc. at the same time. After clicking "Run", you can see the corresponding static parameter measurement result or dynamic parameter measurement result on the corresponding interface.
4. Test system verification
We choose AD4002 of ADI Company as the test verification chip of the high-accuracy ADC test system. AD4002 is an 18bit SAR ADC, its main parameters are as follows:
1) Throughput rate: 2 MSPS/1 MSPS/500 kSPS
2) INL: ±3.2 LSB
3) Guarantee 18-bit accuracy, no missing codes
4) Low power consumption: 70 µW @ 10 kSPS, 14 mW @ 2 MSPS
5) SNR: Typical value 95 dB @ 1 kHz, VREF = 5 V
6) THD: Typical value -125 dB @ 1 kHz, VREF = 5 V
7) Static measurement results: DNL < ±1.2 LSB, INL < ±2.5 LSB
Dynamic measurement results:
1) SNR: 93 dB @ 1 kHz, VREF = 5 V;
2) THD: -118 dB @ 1 kHz, VREF = 5 V;
The above test results are basically consistent with the indicators of AD4002.

5. Conclusion
This paper mainly designs a performance test scheme for high-precision ADC, and successfully realizes its test and function verification system. From the actual test results and the comparison of a foreign ADC index, it can be seen that the expected design goal has been achieved, which has a certain reference significance and guiding value for the future test of ADC.

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