A 256-kb 9T Near-Threshold SRAM With 1k Cells per Bitline and Enhanced Write and Read Operations

Ghasem Pasandi, Student Member, IEEE, and Sied Mehdi Fakhraie

Abstract—In this paper, we present a new 9T SRAM cell that has good write ability and improves read stability at the same time. Simulation results show that the proposed design increases read static noise margin and $I_{ON}/I_{OFF}$ of read path by 219% and 113%, respectively, at supply voltage of 300-mV over conventional 6T SRAM cell in a 90-nm CMOS technology. The proposed design lets us reduce the minimum operating voltage of SRAM ($V_{DD\min}$) to 350 mV, whereas conventional 6T SRAM cannot operate successfully with an acceptable failure rate at supply voltages below 725 mV. We also compared our design with three other SRAM cells from recent literature. To verify the proposed design, a 256-kb SRAM is designed using new 9T and conventional 6T SRAM cells. Operating at their minimum possible $V_{DD\min}$, the proposed design decreases write and read power per operation by 92% and 93%, respectively, over the conventional rival. The area of the proposed SRAM cell is increased by 83% over a conventional 6T one. However, due to large $I_{ON}/I_{OFF}$ of read path for 9T cell, we are able to put 1k cells in each column of 256-kb SRAM block, resulting in the possibility for sharing write and read circuitries of each column between more cells compared with conventional 6T. Thus, the area overhead of 256-kb SRAM based on new 9T cell is reduced to 37% compared with 6T SRAM.

Index Terms—Low power, memory, RAM, sense amplifier, SRAM.

I. INTRODUCTION

For many years, there was little interest in low-power design and design trend was toward increasing the speed and working frequency of digital systems [1]. Recently, some applications, such as implantable devices in man’s body, portable applications, and Wireless Sensor Networks that need low-power circuits, increase the importance of low-power and ultralow-power design [2].

SRAMs are an important part of most of the digital chips and consume a large percent of area and power of each chip [3], so decreasing the power and area of SRAMs can lead to a decrease in the overall power and area of chips. Due to quadratic relation between power and supply voltage of transistors [4], one effective and common method to reduce the power consumption is to decrease the supply voltage.

By further decreasing the supply voltage, it will be lower than threshold voltage of transistors, so the circuit will operate in subthreshold region. Unfortunately, conventional designs cannot work properly in the subthreshold region, so new configurations are needed to let the digital systems work successfully in this region. In this paper, we present a new 9T SRAM cell that solves the problems of write and read operations at low supply voltages, thus leading the SRAM to operate at smaller supply voltages.

The rest of this paper is organized as follows. In Section II, write and read operation problem of conventional 6T SRAM cell is mentioned and some recently published SRAM cells for resolving this problem are discussed. Section III presents our new design for SRAM cell. In Section IV, simulation results for our design and other SRAM cells are compared. Finally, Section V concludes this paper.

II. PROBLEM STATEMENT AND PREVIOUSLY WRITE- AND READ-ENHANCED SRAM CELLS

Conventional 6T SRAM cell faces problems of write failures at low supply voltages [5]. Actually, at low supply voltages, weak write-access transistors in this cell cannot overcome to the strong feedback of inverters of the cell. Therefore, during the write operation, access transistors cannot enforce the input to the desired cell.

In addition, at low supply voltages, conventional 6T SRAM cell faces read failures during read operation, and content of the selected cell is subject to change with large likelihood. However, it is possible to increase the read stability of conventional 6T cell using minimum size access transistors, but this will degrade write ability of this cell. Moreover, problem of small read static noise margin (RSNM) is left unresolved. Another challenge of conventional 6T SRAM cell is small $I_{ON}/I_{OFF}$ of read-access transistors that does not let integrate a large number of cells in each column of SRAM array. At supply voltage of 200 mV in a 0.13-μm technology, this ratio decreases to 240 at the worst case pattern for data of cells in the same bitline [6]. It means that at this supply voltage, the number of cells sharing same bitline must be fewer than 240, so that the difference between ON current of selected cell and accumulated OFF currents of other cells can be distinguished by available sense amplifiers. It is desired to increase $I_{ON}/I_{OFF}$ for read-access path to integrate more cells in the same bitline. Integration of more SRAM cells in the same bitline makes it possible to share write and read circuitries of each column between more cells, translating to...
saving area and power of these circuitries and hence total area and power of SRAM block.

To benefit from power lowering with supply voltage scaling, several designs were proposed in recently published papers. Some of them tried to resolve challenges related to write operation to improve the write-ability at small supply voltages. In general, there are two possible solutions to improve write-ability: the first one is to make write-access transistors stronger during write operation. Sharifi Khani and Sachdev [7] used boosted (larger) voltage to control the write-access transistors during write operation, and Kim et al. [8] make access transistors stronger by employing reverse short-channel effect [using access transistors with larger \((3 \times)\) channel length]. The second solution to improve write-ability of conventional SRAM cell is to make the feedback loops between inverters of the cell weaker or to brake this feedback loop during write operation [6], [9]–[12].

Some other designs tried to resolve problems related to read operation. To decrease the read failure probability, a 7T [13] and two 8T SRAM cells were proposed [14], [15]. To increase RSNM, several forms of buffering read (sensing voltage of internal node by gate of a transistor) were proposed [13], [16]–[18]. In these cells due to buffering read operation, RSNM is increased to the level of hold SNM (HSNM), but in all of these designs, problem of small \(I_{ON}/I_{OFF}\) for read-access path is still remained unresolved.

Calhoun and Chandrakasan [19], Kim et al. [20], and Verma and Chandrakasan [21] used a modified version of Schmitt trigger-based SRAM cell (ST-2). This SRAM cell increases write-ability due to stacked transistors in the inverters of the cell and improves read operation using individual added access transistors. Wen et al. [24] introduced single-ended 8T SRAM cell (WEN cell) that can improve write and read operations at lower supply voltages. There are some SRAM cells proposed in recently published papers that can improve write and read operations at the same time. Kulkarni and Roy [23] changed the design in [22] and proposed a modified version of Schmitt trigger-based SRAM cell (ST-2). This SRAM cell increases write-ability due to stacked transistors in the inverters of the cell and improves read operation using individual added access transistors. Wen et al. [24] introduced single-ended 8T SRAM cell (WEN cell) that can improve write and read operations at the same time. We proposed an 8T SRAM cell in our previous work [25] that improves write ability due to ability of the cell to make one of the inverters of the cell weaker during write operation. This cell also improves read operation due to single-ended write and read operations that let to avoid access transistors sizing conflict [write- and read-enhanced 8T SRAM cell (WRE8T)].

In the SRAM cell used in [25], one nMOS and one pMOS transistor were added to each cell of SRAM that become OFF during write operation and provide floating power and ground rails. In this cell, to control the gate of added nMOS transistor, a separate wordline (WL) is needed. These added transistors and WLs impose area overheads. The point is that, it is not necessary to add these two transistors to each cell to have floating power and ground rails. We can use one nMOS and one pMOS transistor that provide these floating rails and distribute these rails among the sharing cells. There are some possible strategies for sharing the floating rails. Fig. 3 shows three architectures. In Fig. 3(a) and (b), there are cells that are not selected but become weaker during write operation. The less stable cells are shown with light color in this figure and are called half-selected cells (their WL are 0 but power rail of them are floated). Simulations at supply voltage of 500 mV show that mean of SNM of half-selected cells in 1000 runs of Monte Carlo (MC) simulations is 0.33 mV while it is 167.4 mV for not-selected cells. This margin is very small and even at room temperature, thermal noise can flip the content of the cell.

Yamaoka et al. [12] used architecture of Fig. 3(b) for designing the SRAM and shared power line of all cells in the same column. In this design, there is a possible state for content of the cells in the same column that will lead to increased write power due to existence of sneaky current. This strategy and sneaky current are shown in Fig. 4. In this figure, only the left inverter of the SRAM cells is shown. As seen, to write 0 to the selected cell, if voltage of right
Fig. 2. Three write- and read-enhanced SRAM cells from recent literature used for comparison with this paper. (a) New Schmitt trigger-based 10T SRAM cell (ST-2) [23]. (b) Single-ended 8T SRAM cell (WEN cell) [24]. (c) WRE8T [25].

Fig. 3. Three possible architectur es for sharing power and ground rails. (a) Sharing virtual rails for all cells in the array. (b) Each column and (c) each row has individual virtual rail and all cells in the same column (row) share it.

internal nodes in the other cells sharing the column are set to 0, the pMOS transistors in these cells will be ON and let the sneaky current to pass through shared floating line and discharge the voltage of internal nodes in not-selected cells. Thus, activity of nodes and hence, write power will increase. To test the effect of this sneaky current on power consumption, a column of SRAM cells with one selected and 64 other nonselected cells were designed using this architecture and write power for writing 0 was extracted. Two strategies were considered.

1) Case 1: Voltage of right internal nodes in nonselected cells is 0 so sneaky current will exist.
2) Case 2: Voltage of right internal nodes in nonselected cells are \( V_{DD} \) so, path for sneaky current will not exist.

Extracted power for case 1 is 1.18 \( \mu W \) and for case 2 is 0.1 \( \mu W \).

Due to discussed problems for architectures of Fig. 3(a) and (b), we choose third architecture [Fig. 3(c)] for implementing our SRAM. Even in this architecture, state of half selection will exist if we decide to select each bit individually. To solve the disturbance in this state, we apply our half-selection disturb-free scheme introduced in [25].

In this scheme, before first write operation in consecutive writes, the content of each cell in the selected row are read and then, using embedded inverters in each column, they are written back on the corresponding write bitlines.

B. Read Enhancement Techniques in Proposed SRAM Cell

One method to increase RSNM is sensing voltage of internal nodes of SRAM cell through gate of a transistor in read operation. The simplest way of buffering is using two transistors that one of them (buffer transistor) senses internal voltage of SRAM cell, and the other one is controlled by read wordline (RWL) signal [17]. In the case that buffer transistor is ON, for unselected cell, leakage current is large. In [26] and [27], three transistors are used in read path. Depending on the internal voltage of SRAM cell, there are two or three OFF transistors in read path for unselected SRAM cells. Equation (1) shows the dominating part of leakage current, that is subthreshold current [28].
For $V_{DS}$ larger than 50 mV, we can ignore the second term to reach to (2) [28]

$$I_{D_{sub}} = I_t \frac{(V_{GS} - \phi_F - \phi_M)}{2} \left(1 - 10^{-\frac{V_{GS}}{2} \lambda} \right) \quad (1)$$

$$I_{D_{sub}} \approx I_t \frac{(V_{GS} - \phi_F - \phi_M)}{2} \lambda \quad (2)$$

Now, the worst case leakage current for two and three stacked transistors (one of stacked transistors is ON) can be expressed by (3) and (4), respectively. Assuming that $V_T = 300$ mV, $\lambda = 1.5$, and $S = 80$ mV (typical values [28]), for $V_{DD} = 1$ V, ratio of the worst case leakage current for three stacked transistors ($I_{31}$), to the worst case of two stacked transistors ($I_{22}$) can be expressed by $I_{31}/I_{22} = 10^{(-1.5-3\times1.5-2\times1.5)/(6\times1.5+9\times1.5+5\times1.5)}V_{DD}/S \approx 10^{-5}$. As seen, leakage current is decreased by exponential order if one stacked transistor is added to read path.

In [26], one of three stacked transistors in the read path is shared among all cells in the array, so it is OFF only in idle modes, so, the worst case for leakage current flowing through read path is that two of stacked transistors are ON and one of them is OFF. Leakage current for this case can be expressed by (5) that shows 80% increasing compared with (4)

$$I_{22} = I_t \frac{V_{DD}}{2} \lambda \quad (3)$$

$$I_{31} = I_t \frac{V_{DD}}{2} \lambda \quad (4)$$

$$I_{32} = I_t \frac{V_{DD}}{2} \lambda \quad (5)$$

In addition to this increment of leakage current in SRAM cell of [26], there is a possible state that read bitline will be discharged falsely. Fig. 5 shows SRAM cell used in [26]. In Fig. 6, a possible state is illustrated that can lead to falsely discharging RBL_1 bitline falsely (another type of sneaky current).

To solve the challenges of SRAM cells used in [26] and [27], we are proposing a new design for SRAM cell. Fig. 7 shows a circuit diagram of our 9T SRAM cell. In this design, added pMOS transistor M9 is ON for not selected cells so the voltage of node Qc will rise to reach $V_{DD}$ for these cells. This will reduce the leakage current passing through M6 for two reasons. The first reason is that by increasing the voltage of source of M6, its threshold voltage will increase according to (6) [4]. Increasing $V_T$ will decrease the subthreshold leakage current $I_{D_{sub}}$ (that is the main component of leakage current) due to (1). The second reason behind decreasing leakage current is that by increasing voltage of source of M6, $V_GS$ of this transistor will decrease and due to (1) this will reduce subthreshold current $I_{D_{sub}}$ exponentially.

As mentioned earlier, challenge of design used in [27] is that a large leakage current flows through read-access path for a specific data pattern in selected cells. In this case, despite the stored data in the selected cell, leakage current can discharge the read-bitline capacitance falsely. In our design, for selected cells, added pMOS transistor M9 is OFF but still passes some leakage current to node Qc. This will increase voltage of node Qc a little, and due to (1) and (6), reduce leakage current flowing through M6.

$$V_T = V_T0 + \gamma (\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}) \quad (6)$$
Fig. 8(d) shows ON to OFF current ratios for read-buffered transistors in read path for the three designs (typical corner, and $T = 27 ^\circ$ C). In this figure, voltage of internal node is assumed to be $V_{DD}$. As seen, $I_{ON}/I_{OFF}$ of read path for our proposed design is considerably larger than the two others. For example, at $V_{DD} = 0.8$ V, $I_{ON}/I_{OFF}$ of WRE9T design is 8.66 times larger than 9T cell in [27]. Thus, it is possible to integrate a larger number of cells sharing same bitline in our design compared with two others, resulting in saving the area and power of peripheral circuits used for each column in SRAM array.

IV. SIMULATION RESULTS AND DISCUSSION

Since our proposed SRAM cell in this paper is write and read enhanced, thus in this part we extract and compare different working parameters of this cell with other write- and read-enhanced SRAM cells and also conventional 6T SRAM cell. HSPICE 2011 was used for simulations and circuits were designed in a 90-nm industrial CMOS technology.

To make the comparison of conventional 6T SRAM cell with our proposed SRAM cells more fair, we also consider Isoarea 6T (I.A.6T) SRAM cell [23]. In I.A.6T SRAM cell, transistors were upsized so that the area of this cell becomes equal to WRE9T SRAM cell.

A. $I_{ON}/I_{OFF}$ of Read Path

Fig. 9 shows distribution of $I_{ON}/I_{OFF}$ for proposed SRAM cell and conventional one in presence of process variation at supply voltage of 300 mV. As seen, mean of $I_{ON}/I_{OFF}$ for proposed design is larger than conv. 6T. Worst case ratio for proposed design is 1080 and is 78 for 6T.

For the case that voltage of storage node is such that the related bitline should not be discharged, leakage current of selected and not selected cells become very important. As the leakage of read path become larger, voltage of read bitline decreases much faster and this will lead to read the stored data falsely. Fig. 10 shows voltage of read bitline (for differential cells, voltage of the bitline that should not be discharged) when it should not be discharged at supply voltage of 500 mV. As seen, voltage drop for WRE9T cell since RWL asserted (at 980 ns) until 120 ns later, is almost 7 mV, whereas for the best of others (conventional 6T), this voltage drop is almost 250 mV. Voltage of read bitline for ST-2 and WRE8T reach to $V_{DD}/2$ after 30 ns. Thus, if voltage of this bitline is read after this time, read error will occur. In our design, using stacking effect and also by adding the pMOS transistor M9, leakage current through read path is very small. In the read path of
SRAM cells used in [19] and [20] also the path between read bitline and ground is broken, so it is expected that voltage drop of read bitline for these cells becomes small similar to our design. Fig. 11 shows the voltage of read bitline for WRE9T cell and those of [19] and [20]. Voltage drop for the cell [19] after 120 ns is almost 127 mV and remains above $V_{DD}/2$. Voltage drop of the cell [20] is almost equal to WRE9T cell and is acceptable.

B. Read, Write, and Hold SNMs

One of the most important drawbacks of conventional 6T SRAM cell is small RSNM at low supply voltages. This does not let scaling of supply voltage and going to subthreshold region to benefit from power saving of it [29]. Fig. 12 shows distribution of RSNM for WRE9T and four other SRAM cells at supply voltage of 500 mV. Mean of RSNM for our design is better than conventional and ST-2 by $2.53 \times$ and $1.23 \times$, respectively. In WEN SRAM cell [24], voltage of left node in the cell is kept floating during read operation. At typical corner and room temperature, leakage of pMOS pull up transistors in this cell is considerable that leads to destroying the dynamic voltage of left storage node. Thus, RSNM for this cell is very small at these conditions (mean is 0.3 mV and sigma is 1.8 mV).

C. Minimum Operating Voltage: $V_{DD_{min}}$

To benefit from power saving of voltage scaling, it is desired to design SRAMs that can operate successfully at lower supply voltages. There are two different methods to determine minimum supply voltage for SRAMs. The first one is based on SNM [23] that does not capture the transient behavior of the cell. The second one considers the transient behavior of the cell but uses some approximations that lead to large errors at the tail of the distribution where the sensitive failure probabilities exist [30]. In this paper, minimum operating voltage is extracted, while the circuits operate at their real operating modes so that transient behavior is captured. Assuming not having error correcting code in data, and considering
TABLE I
MINIMUM SUPPLY VOLTAGE FOR WRITE, READ, ACCESS, AND DATA RETENTION AND VDDmin (V)

| Design  | WRE9T | WRE8T | 6T   | ST-2 | WEN | I.A.6T |
|---------|-------|-------|------|------|-----|--------|
| Read    | 0.320 | 0.430 | 0.725| 0.340| 0.355| 0.390  |
| Access  | 0.310 | 0.405 | 0.555| 1.20 | 1.20 | 0.375  |
| Write   | 0.340 | 0.320 | 0.455| 0.375| 0.315| 0.480  |
| Retention | 0.350 | 0.350 | 0.350| 0.350| 0.350| 0.275  |
| VDDmin  | 0.350 | 0.430 | 0.725| 1.20 | 1.20 | 0.480  |

*These cells could not reach to failure probability of 10^{-6} at lower voltages, thus, nominal voltage was chosen for them.

To have accurate results and to model the process variation effect, MC simulations were used. In this simulation, different parameters, such as threshold voltage, channel length, gate oxide thickness, carrier mobility, and channel doping concentration were varied with Gaussian distributions.

To extract the failure probability in above simulations, dynamic criteria proposed in [31] was used and the outputs were measured at the end of the operation cycle. Table I shows minimum operating voltages for different modes of operation. VDDmin for each design is the maximum of these minimum voltages. As seen, VDDmin for our proposed design, WRE9T is lower than others.

D. Power Consumption

1) Leakage Power: In Section IV-C, minimum operating voltage of different SRAM cells were extracted. Assuming that the mentioned SRAMs are used in low-power circuits, they are expected to operate at their VDDmin; thus, we extracted leakage power of each cell at its VDDmin. Fig. 15 shows the leakage power of different cells. These results were extracted in typical corner and at temperature of 110 °C.

2) Total Power Consumption for Single Write Operation: Fig. 16 shows power consumption for single write operation for different SRAM cells. This power consumption is average of power consumption for writing one 0 and one 1 to the desired SRAM cell. As seen, power consumption for WRE8T, WRE9T, and WEN SRAM cells are smaller than three others. This is mainly due to single-ended write operation in these SRAM cells, that leads to have smaller charging-discharging on write-bitlines (for single-ended cells there is one write-bitline compared with differential ones that there are two write-bitlines).

E. Layout Area

Fig. 17(a) shows the layout of the proposed cell and Fig. 17(b) shows the layout of conventional 6T SRAM cell in a 90 nm industrial CMOS technology. Table II shows area of compared SRAM cells in this technology. As seen, conventional design has the minimum area, whereas ST-2 cell occupies larger area in the silicon.

Area of proposed WRE9T cell is greater than 6T by 83%. However, simulation results for I.A.6T shows that, in the same consumption of silicon area for WRE9T and I.A.6T, VDDmin, RSNM, ION/IOFF for read-access path, are better for proposed design. Only HSNM of I.A.6T is better than WRE9T cell. Therefore, conventional 6T SRAM cell with the same area cannot have capabilities similar to WRE9T. However, there is a drawback for WRE9T in physical implementation compared with conventional 6T SRAM cell; layout of WRE9T cell is not fully symmetric, and will be subject to systematic differences in processing variation.

F. 256-kb SRAM

We designed a 256-kb SRAM using proposed WRE9T, and conventional 6T SRAM cells. As mentioned in Section IV-A, worst case value of ION/IOFF for WRE9T and 6T cells are 1080, and 78, respectively. Thus, we put 1k cells in each column of the proposed SRAM block and 64 cells in each column of SRAM block using 6T cells. Table III lists write and read power and delays for both of these SRAMs. We have mentioned the results assuming that each SRAM is operating at its minimum possible supply voltage. In this table, write delay is the time between activation of decoder until voltages of internal nodes of selected cell become equal. Read delay is the time between activation of decoder until 50-mV voltage difference between two bitlines occurs [18] (for WRE9T that there is one bitline for read operation, this difference is between voltage of read bitline and VDD). Write power and write delay reported here are average of writing 1 and 0, and read power is average of reading 1 and 0. However, since we assume that bitline is precharged to VDD, read delay is the delay for reading 0.
There are several papers, such as [6], [32], and [33] that discussed about single-ended and differential read operations in SRAM cells, and their differences in different characteristics especially read delay. These comparisons and statements can be applied for all single-ended and differential SRAM cells, and also to our single-ended and conventional differential SRAM cells. However, in this paper, we mostly focus on characterizing and comparing single SRAM cells. Thus, in the measurements of read delay, we did not consider the effect of sense amplifiers. As seen, proposed design consumes lower power consumption for both read and write operations. Write and read circuitries of each column of SRAM block are shared among more cells when using new 9T cells compared with conventional 6T cells. This results in reducing area overhead of 256-kb SRAM based on new 9T SRAM cells from 83% (for comparing single SRAM cells) to 37% compared with block design with conventional 6T. In this section, several electrical design metrics were considered and the SRAM cells were compared and the best designs for each criterion were determined as listed in Table IV. Our proposed design WRE9T is the best in four metrics. Thus, we conclude this design can be the best choice to operate at low voltages.

V. CONCLUSION

In this paper, a new 9T SRAM cell was presented. This SRAM cell improves write-ability and read stability at the same time. In this SRAM cell, $I_{ON}/I_{OFF}$ of read-access path is increased considerably that lets to integrate more cells in the same column of SRAM array. This property allows sharing write and read peripheries that can directly translate to saving area and power. Proposed design decreases minimum possible operating voltage of SRAM by 375 mV over conventional 6T and by 130 mV over I.A.6T SRAM cell. Area of the proposed cell is >6T cell by 83%. This overhead is reduced to only 37% by the potential of sharing write and read circuitry of each column in a 256-kb SRAM.

REFERENCES

[1] A. Wang, B. H. Calhoun, and A. P. Chandrakasan, *Sub-Threshold Design for Ultra Low-Power Systems*. New York, NY, USA: Springer-Verlag, 2005.

[2] K. Wang, “Ultra low-power fault-tolerant SRAM design in 90 nm CMOS technology,” M.S. thesis, Dept. Electr. Comput. Eng., Univ. Saskatchewan, Saskatoon, SK, Canada, 2010.

[3] G. Pasandi and S. M. Fakhraie, “A new sub-300 mV 8T SRAM cell design in 90 nm CMOS,” in Proc. 17th CSI Int. Symp. Comput. Archit. Digit. Syst. (CADS), Oct. 2013, pp. 39–44.

[4] J. M. Rubaey, A. P. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*. Upper Saddle River, NJ, USA: Prentice-Hall, 2003.

[5] G. Pasandi and S. M. Fakhraie, “A new sub-threshold 7T SRAM cell design with capability of bit-interleaving in 90 nm CMOS,” in Proc. 21st Iranian Conf. Elect. Eng. (ICEE), May 2013, pp. 1–6.

[6] B. Zhai, S. Hanson, D. Blaauw, and D. Sylvester, “A variation-tolerant sub-200 mV 6-T subthreshold SRAM,” *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2338–2348, Oct. 2008.

[7] M. Sharifkhani and M. Sachdev, “Segmented virtual ground architecture for low-power embedded SRAM,” *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 2, pp. 196–205, Feb. 2007.

[8] T.-H. Kim, J. Liu, and C. H. Kim, “A voltage scalable 0.26 V, 64 kb 8T SRAM with $V_{min}$ lowering techniques and deep sleep mode,” *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1785–1795, Jun. 2009.
[9] R. E. Aly, M. I. Faisal, and M. A. Bayoumi, “Novel 7T SRAM cell for low power cache design,” in Proc. IEEE Int. Soc. Conf., Sep. 2005, pp. 171–174.

[10] G. Pasandi, E. Qasemi, and S. M. Fakkhrai, “A new low-leakage T-gate based 8T SRAM cell with improved write-ability in 90 nm CMOS technology,” in Proc. 22nd Iranian Conf. Elect. Eng. (ICEE), Tehran, Iran, May 2014.

[11] K. Kanda, H. Sadaaki, and T. Sakurai, “90% write power-saving SRAM using sense-amplifying memory cell,” IEEE J. Solid-State Circuits, vol. 39, no. 6, pp. 927–933, Jun. 2004.

[12] M. Yamaoka et al., “90-nm process-variation adaptive embedded SRAM modules with power-line-floating write technique,” IEEE J. Solid-State Circuits, vol. 41, no. 3, pp. 705–711, Mar. 2006.

[13] Z. Liu and V. Kursun, “Characterization of a novel nine-transistor SRAM cell for low-VDD and high-speed applications,” IEEE J. Solid-State Circuits, vol. 41, no. 1, pp. 113–121, Jan. 2006.

[14] R. Saeidi, M. Sharifkhani, and K. Hajsadeghi, “A subthreshold symmetric SRAM cell with high read stability,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 61, no. 1, pp. 26–30, Jan. 2014.

[15] S. Hassanzadeh, M. Zamani, K. Hajsadeghi, and R. Saeidi, “A novel low power 8T-cell sub-threshold SRAM with improved read-SMN,” in Proc. 8th Int. Conf. Design Technol. Integr. Syst. Nanoscale Era (DTIS), Mar. 2013, pp. 35–38.

[16] Z. Liu and V. Kursun, “Characterization of a novel nine-transistor SRAM cell,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 16, no. 4, pp. 488–492, Apr. 2008.

[17] L. Chang et al., “A 5.3 GHz 8T-SRAM with operation down to 0.41 V in 65 nm CMOS,” in Proc. IEEE Symp. VLSI Circuits, Jun. 2007, pp. 252–253.

[18] A. Islam and M. Hasan, “Leakage characterization of 10T SRAM cell,” IEEE Trans. Electron Devices, vol. 59, no. 3, pp. 631–638, Mar. 2012.

[19] B. H. Calhoun and A. P. Chandrakasan, “A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation,” IEEE J. Solid-State Circuits, vol. 42, no. 3, pp. 680–688, Mar. 2007.

[20] T.-H. Kim, J. Liu, J. Keane, and C. H. Kim, “A 0.2 V, 480 kb subthreshold SRAM with 1 k cells per bitline for ultra-low-voltage computing,” IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 518–529, Feb. 2008.

[21] N. Verna and A. P. Chandrakasan, “A 256 kb 65 nm 8T subthreshold SRAM employing sense-amplifier redundancy,” IEEE J. Solid-State Circuits, vol. 43, no. 1, pp. 141–149, Jan. 2008.

[22] J. P. Kulkarni and K. Roy, “A 160 mV robust Schmitt trigger based subthreshold SRAM,” IEEE J. Solid-State Circuits, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.

[23] J. P. Kulkarni and K. Roy, “Ultra-low-voltage process-variation-tolerant Schmitt-trigger-based SRAM design,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2, pp. 319–332, Feb. 2012.

[24] L. Wen, Z. Li, and Y. Li, “Single-ended, robust 8T SRAM cell for low-voltage operation,” Microelectron. J., vol. 44, no. 8, pp. 718–728, 2013. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026269213001031

[25] G. Pasandi and S. M. Fakkhrai, “An 8T low-voltage and low-leakage half-selection disturb-free SRAM using bulk-CMOS and FinFETs,” IEEE Trans. Electron Devices, vol. 61, no. 7, pp. 2357–2363, Jul. 2014.

[26] H. Jiao and V. Kursun, “Power gated SRAM circuits with data retention capability and high immunity to noise: A comparison for reliability in low leakage sleep mode,” in Proc. Int. SoC Design Conf. (SoCC), Nov. 2010, pp. 5–8.

[27] S. A. Verkila, S. K. Bondada, and B. S. Amrutur, “A 100 MHz to 1 GHz, 0.35 V to 1.5 V supply 256 × 64 SRAM block using symmetric 9T SRAM cell with controlled read,” in Proc. 21st Int. Conf. VLSI Design (VLSID), Jan. 2008, pp. 560–565.

[28] J. Rabaey, Low Power Design Essentials. New York, NY, USA: Springer-Verlag, 2009.

[29] S. K. Gupta, A. Raychowdhury, and K. Roy, “Digital computation in subthreshold region for ultralow-power operation: A device-circuit-architecture codesign perspective,” Proc. IEEE, vol. 98, no. 2, pp. 160–190, Feb. 2010.

[30] J. Wang, A. Singh, R. A. Rutenbar, and B. H. Calhoun, “Statistical modeling for the minimum standby supply voltage of a full SRAM array,” in Proc. 33rd Eur. Solid State Circuits Conf. (ESSCIRC), Sep. 2007, pp. 400–403.

[31] D. E. Khalil, M. Khellah, N.-S. Kim, Y. Ismail, T. Karnik, and V. K. De, “Accurate estimation of SRAM dynamic stability,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 16, no. 12, pp. 1639–1647, Dec. 2008.

[32] Y. Ye, M. Khellah, D. Somasekhar, and V. De, “Evaluation of differential vs. single-ended sensing and asymmetric cells in 90 nm logic technology for on-chip caches,” in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2006, pp. 963–966.

[33] Y. Zhao, J. Li, and K. Mohanram, “Multi-port FinFET SRAM design,” in Proc. 23rd ACM Int. Conf. Great Lakes Symp. VLSI (GLSVLSI), 2013, pp. 293–298.

Ghasem Pasandi (S’13) received the B.Sc. and M.Sc. degrees in electrical and electronics engineering from the University of Tehran, Tehran, Iran, in 2011 and 2014, respectively.

He has authored several conference and journal papers. His current research interests include low power and ultralow-power static random access memory design, low power and energy efficient logic design, reliable and fault-tolerant static and dynamic CMOS circuit and system design, VLSI signal processing, and VLSI implementation of digital systems.

Sied Mehdi Fakkhrai received the M.Sc. degree in electronics from the University of Tehran, Tehran, Iran, in 1989, and the Ph.D. degree in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 1995.

He was a Professor with the School of Electrical and Computer Engineering, University of Tehran. He was the Director of the Silicon Intelligence and VLSI Signal Processing Laboratory, the Director of Electrical and Electronics Engineering, and the Director of Computer Hardware Engineering with the School of Electrical and Computer Engineering, University of Tehran. He was a Visiting Professor with the University of Toronto, in 1998, 1999, and 2000, where he was involved in efficient implementation of artificial neural networks. He was with Valve Semiconductor Inc., Irvine, CA, USA, from 2000 to 2003. He was in Dubai, United Arab Emirates, and Markham, Canada Offices of Valence as the Director of Application Specified Integrated Circuit (ASIC) and System-on-a-Chip Design, and the Technical Leader of integrated broadband gateway and family radio system baseband processors. He was involved in many industrial integrated circuit design projects, including design of network processors and home gateway access devices, DSL modems, and digital signal processors for personal and mobile communication devices. He has co-authored a book entitled VLSI-Compatible Implementations for Artificial Neural Networks (Boston, MA, USA: Kluwer, 1997). He has authored or co-authored over 230 reviewed conference and journal papers. His last research interests include system design and ASIC implementation of integrated systems, novel techniques for high-speed digital circuit design, and system-integration and efficient VLSI implementation of intelligent systems. He passed away on December 7, 2014.