A digital intensive clock recovery circuit for HF-Band active RFID tag

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Abstract: A digital intensive Clock Recovery Circuit applied to HF-Band active RFID tag is proposed in this paper. Based on the signal interface of ISO/IEC 14443 Type-A protocol, in order to achieve the coherent demodulation in receiving mode, a modified digital intensive PLL is utilized to accurately extract the carrier’s frequency and phase information from the received ASK 100% modulation signal. Meanwhile, in transmitting mode, the proposed PLL can also effectively calibrate the system clock’s frequency error and phase deviation in a discontinuous mode. The whole chip of Clock Recovery Circuit was implemented in 180 nm EEPROM technology. The measurement results show that the maximum power consumption of Clock Recovery Circuit is about \(900 \mu\text{W}\) at 1.8 V power supply, and the phase deviation in the demodulation and modulation period is respectively less than 10° and 20°.

Keywords: Clock Recovery Circuit (CRC), HF-Band, Radio Frequency Identification (RFID), Phase Locked Loop (PLL), Time-to-Digital Converter (TDC)

Classification: Integrated circuits

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1 Introduction

Nowadays, HF-Band (High Frequency band, 13.56 MHz) passive RFID tag has been widely used in supply chain market and smart card for payment [1]. However, passive RFID tag must rely on the RF energy
transferred from RFID reader so that passive RFID tag can be only read at short distance with large antenna to receive enough power. Compared with passive RFID tag, due to supplying power by a battery, active RFID tag has longer read distance and relatively higher sensitivity with the coherent demodulation method [2]. In addition, with the continuous expansion of mobile electronic products, such as Smart Phone, Intelligent Watch or Google Glass, there is a wonderful chance that active RFID tag with relatively small antenna footprint can be integrated into these mobile electronic terminals as a personal application. Hence, the original disadvantages of active RFID tag such as large chip size and limited operational lifetime may be overcome by System on Chip (SoC) and sharing battery with mobile devices.

For small antenna in a mobile device, envelop-detector method (normally used for HF-Band RFID tag) suffers from EMI noise from other electronic components closely. Hence, to integrate tag with mobile device, the coherent demodulation is a more attractive option in tag’s receiving mode because of its theoretical 3 dB better noise figure. Furthermore, to be fully compatible with existing HF reader, the transmitted signal from active RFID tag should exactly has the same carrier’s frequency (less than 7 kHz according to Type-A protocol) and phase (or opposite phase in BPSK) as RFID reader. Hence, a Clock Recovery Circuit (CRC) is needed to recover the synchronous clock signal during receiving mode and to keep the clock’s frequency and phase unchanged during transmitting mode.

In this paper, according to ISO/IEC 14443 Type-A protocol, a digital intensive CRC applied to HF-Band active RFID tag is proposed. Based on a modified digital intensive PLL, this CRC can not only extract the synchronous clock from the received signal in the receiving mode but also calibrate the frequency and phase deviation in the transmitting mode.

The paper is organized as follows: the system architecture of CRC is presented in Section 2. The block details are given in Section 3. The experimental results are provided in Section 4. Finally, conclusion is in Section 5.

2 System architecture and analysis

2.1 System architecture of Clock Recovery Clock

Fig. 1 (a) shows the communication signals between HF-Band RFID reader and active tag [3]. At the beginning of receiving mode, there is a period of in-field time to make the active tag started up. In this 1 ms in-field time, the tag will receive the continuous carrier signal from RFID reader. However, after the in-field time, due to ASK 100% modulation and 106 kbit/s Modified Miller code, the received carrier information from RFID reader will become discontinuous. Meanwhile, in transmitting mode, due to 106 kbit/s ASK-Manchester code, the transmitted modulation data (simultaneously modulated by 848 kHz subcarrier and 13.56 MHz carrier) will just occupy a half cycle of per bit and another half cycle time is idle, as shown in Fig. 1 (a). In addition, during the transmitting time of tag, RFID reader will still transmit the continuous carrier signal.

According to the above description of signal interface, the system architecture of proposed CRC is shown in Fig. 1 (b). This proposed CRC is based on a modified digital intensive PLL which basically includes a Time
to Digital Converter (TDC), a Loop Filter, a digital controlled Oscillator (DCO) and a DCO Interface. TDC is used to detect the phase difference between DCO output and received signal from antenna. Loop filter is a digital PI (Proportional + integral) filter so as to realize a type II PLL. DCO is composed of a Sigma-Delta Digital-to-Analog Converter (ΣΔDAC) and a Voltage Controlled Oscillator (VCO). The output of DCO is the recovered clock signal (CKV). DCO Interface is a digital limiter which deals with the overflow of Oscillator Tuning Word (OTW, the output of Loop Filter) in the recovering and calibrating process.

During the 1 ms in-field time, the whole digital intensive CRC can easily finish the synchronization between CKV and received carrier signal. Meanwhile, the Phase Error (PE) of TDC output will become about zero. After the in-field time, with the carrier information in the received ASK modulation signal, CKV can be still synchronized. However, when the received ASK modulation signal is zero and without any carrier information, the output of TDC will be set to be zero by the signal EN_Ctrl_R. Due to type II PLL, the integral branch of Loop Filter will hold OTW value so that the whole PLL will become a free running DCO without any feedback loops. Hence, recovering process and free running of DCO will become alternate according to the received ASK modulation signal, which means the entire synchronous process will also become discontinuous.

In transmitting mode, another half cycle time of per bit which is idle will be utilized by CRC to receive the carrier signal from RFID reader so that the frequency and phase deviation of CKV can be calibrated. According to the base-band 106 kbit/s data, an accurate EN_Ctrl_T signal can be generated to control tag’s antenna and TDC. When EN_Ctrl_T is 1, the carrier signal from RFID reader will be received and CKV will be calibrated by the whole CRC loop. On the contrary, when EN_Ctrl_T is 0, the base-band data will be transmitted and CKV will be just generated by a free running DCO. Similar to receiving mode, the whole calibrating process will also become discontinuous.
2.2 System analysis

Fig. 2 shows the s-domain system model of proposed CRC. In this loop model, a 3rd or 4th-order LPF Filter is used to remove the high-frequency quantization noise of ΣΔDAC. Parameter \( \alpha \) and \( \rho \) are used to control the loop bandwidth of the whole CRC. \( K_{TDC} \) and \( K_{DCO} \) are the gains of TDC and DCO.

![Fig. 2. The s-domain system model of proposed CRC](image)

Generally, based on a small loop bandwidth, the z-domain model can be approximated by the s-domain model effectively. Hence, the open-loop transfer function of s-domain model is

\[
H_{ol}(s) = K_{TDC} \cdot \left( \frac{\alpha + \rho \cdot f_V}{s} \right) \frac{K_{DCO}}{s} \cdot f_{LPF}(s)
\]

where \( f_{LPF}(s) \) is the transfer function of 3rd or 4th-order LPF Filter. And the close-loop error transfer function can be expressed as

\[
H_{cl, error}(s) = \frac{\phi_R - f_V}{\phi_R} = \frac{f_R - f_V}{f_R} = \frac{1}{1 + H_{ol}(s)}
\]

\[
= \frac{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s \cdot f_{LPF}(s) + \omega_n^2 \cdot f_{LPF}(s)}{s^2}
\]

\[
\omega_n = \sqrt{\rho \cdot K_{TDC} \cdot K_{DCO} \cdot f_V}
\]

\[
\zeta = \frac{\alpha \cdot \sqrt{K_{TDC} \cdot K_{DCO}}}{2 \cdot \sqrt{\rho \cdot f_V}}
\]

where \( f_V \) and \( \Phi_V \) are the frequency and phase of CKV, \( f_R \) and \( \Phi_R \) are the frequency and phase of received carrier signal. Assuming that \( f_{LPF}(s) \) is about equal to 1 inside loop bandwidth, \( H_{cl, error}(s) \) will become a classical two-pole system transfer function.

In fact, due to the free running time of per bit, every time at the beginning of recovering or calibrating, there will be both a frequency error step \( (\Delta f_n) \) and a phase deviation step \( (\Delta \Phi_n) \) inputted into the CRC and their step responses are given by

\[
\varepsilon_{CKV\_FREQ,n}(s) = \frac{\Delta f_n}{s} \frac{s^2}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2}
\]

\[
\varepsilon_{CKV\_PHASE,n}(s) = \frac{2\pi \cdot \Delta f_n}{s^2} + \frac{\Delta \phi_n}{s} \frac{s^2}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2}
\]

where \( \varepsilon_{CKV\_FREQ,n} \) and \( \varepsilon_{CKV\_PHASE,n} \) are the frequency error and phase deviation of CKV after recovering or calibrating. According to the Eq. (5),
(6) and inverse Laplace transformation, the time-domain step response can be given by

\[ \varepsilon_{\text{CKV\_FREQ, } n}(t) = \Delta f_n \cdot \frac{e^{-\zeta \omega_c t}}{\sqrt{1 - \zeta^2}} \sin \left( \sqrt{1 - \zeta^2} \omega_c t + \theta \right) \]  

\[ \varepsilon_{\text{CKV\_PHASE, } n}(t) = \Delta \phi_n \cdot \frac{e^{-\zeta \omega_c t}}{\sqrt{1 - \zeta^2}} \sin \left( \sqrt{1 - \zeta^2} \omega_c t + \theta \right) + 2\pi \cdot \Delta f_n \cdot \frac{e^{-\zeta \omega_c t}}{\omega_n \sqrt{1 - \zeta^2}} \sin \left( \sqrt{1 - \zeta^2} \omega_c t \right) \]  

\[ \theta = \arctan \left( \frac{\sqrt{1 - \zeta^2}}{\zeta} \right) + \frac{\pi}{2} \]  

After the next free running time \( T_{\text{Free\_Running}} \), the next step \( \Delta f_{n+1} \) and \( \Delta \phi_{n+1} \) can be given by

\[ \Delta f_{n+1} = \varepsilon_{\text{CKV\_FREQ, } n} \]  

\[ \Delta \phi_{n+1} = \varepsilon_{\text{CKV\_FREQ, } n} \cdot T_{\text{Free\_Running}} + \varepsilon_{\text{CKV\_PHASE, } n} \]  

For example, as shown in Fig. 1 (a), assume that the maximum free running time of DCO is about 9.4 \( \mu \)s (1/106k) and the minimum recovering or calibrating time is about 4.7 \( \mu \)s (in the transmitting mode). Meanwhile, \( \zeta \) is set to be 0.707 and the loop bandwidth \( \omega_C \) is about equal to 2\( \omega_n \). If the step \( \Delta f \) and \( \Delta \Phi \) is about 100 kHz and 180°, as long as \( \omega_C \) is larger than 300 kHz, the \( \varepsilon_{\text{CKV\_FREQ}} \) and \( \varepsilon_{\text{CKV\_PHASE}} \) will be less than 1 kHz and 1° after 4.7 \( \mu \)s recovering or calibrating time, as shown in Fig. 3.

![Fig. 3. With different loop bandwidth \( \omega_C \) and step \( \Delta f \), the \( \varepsilon_{\text{CKV\_FREQ}} \) and \( \varepsilon_{\text{CKV\_PHASE}} \) after 4.7 \( \mu \)s recovering or calibrating time are shown.](image)

If there is a large step \( \Delta f_n \) (for example, \( \Delta f_n=1 \) MHz) generated by sudden PVT variation or random noise, according to the Eq. (7), (8), (10) and (11), the whole discontinuous calibrating process is shown in Fig. 4. The durations of per calibrating and per free running are about 4.7 \( \mu \)s and 9.4 \( \mu \)s. Whatever \( \omega_C \) is 200 kHz or 300 kHz, the proposed CRC can...
gradually calibrate the step $\Delta f_n$ and $\Delta \phi_n$ into much small error (less than 500 Hz and 1°) within 33 $\mu$s

3 Circuit implementation

3.1 Time to Digital Converter

The circuit structure of TDC core is based on a delay line sampled by CKV, as shown in Fig. 5 (a). The phase difference is determined by passing the received signal through a chain of buffers and using an array of registers to sample the different phase outputs of buffers. In this arrangement there will be a series of 1’s and 0’s at the outputs of registers. The rising-edge position of received signal will be the same as the position of first 1 to 0 edge in the sampling results [4]. Thus, the phase difference between CKV and the received signal will correspond to the detected position of first 1 to 0 edge. However, when the received signal is zero and without any carrier information, all the outputs of registers such as Q1, Q2, ..., Q64 will be equal to zero. Hence, the signal EN_CTRL_R will become zero so that the output of TDC will be set to be zero, as shown in Fig. 5 (c).

Fig. 4. The discontinuous calibrating process of a 1MHz step frequency error

Fig. 5. The circuit structure and transfer function of TDC, (a) TDC Core, (b) Transfer function at the decoder output, (c) Boundary Expanding of TDC, (d) Transfer function of TDC
In this design, the total delay of 64-stage buffer chain can only cover a cycle of CKV so that the detectable phase range of TDC is just from \(-\pi\) to \(\pi\), which is too small to calibrate a large step frequency error. Hence, with the finite buffer stages, a Boundary Expanding block should be utilized to expand the detectable phase range of TDC. As shown in Fig. 5 (b) and (c), if \(f_v\) is larger than \(f_R\), the phase difference will become larger and larger. When the phase difference changes from \(\pi - \Delta\theta\) to \(\pi + \Delta\theta\), Decoder_Out will also change from 0.5 to \(-0.5\). However, in the Boundary Expanding block, the abs of difference between current and previous Decoder_Out will be compared with 0.5. Hence, in this situation, because the abs of difference is larger than 0.5, TDC_Out will hold the previous Decoder_Out. On the contrary, when the phase difference changes from \(2\pi - \Delta\theta\) to \(2\pi + \Delta\theta\), Decoder_Out will become larger than zero and the abs of difference will become smaller than 0.5, so TDC_Out will output the current Decoder_Out. Thus, the final transfer function of TDC is shown in Fig. 5 (d). In addition, because TDC can only detect the phase difference in nature, the frequency of CKV is dangerous to be locked at \(f_R/2\) or \(2f_R\). Hence, the frequency range of CKV must be satisfied by
\[
\frac{3f_R}{4} < f_v < \frac{3f_R}{2}
\] (12)

If the condition of Eq. (12) is met, as long as \(f_v\) is always larger than \(f_R\), according to Fig. 5 (d), TDC_Out will always output the positive value, and vice versa. Moreover, due to type II PLL, the integral branch of Loop Filter will guarantee the negative feedback of the whole loop. Therefore, with the Boundary Expanding block, the detectable phase range of TDC will become infinite and can be given by
\[
2\pi(n - 1) \leq \Delta\phi \leq 2\pi(n + 1), n = \ldots -1, 0, 1 \ldots
\] (13)

### 3.2 DCO Interface

Due to the finite frequency range of DCO, DCO control bit is limited in 17 bits. In order to cover the range of DCO control bit and avoid their overflow, the bit width of OTW is set to be 20 bits and a digital limiter is utilized to deal with the overflow of OTW in the recovering or calibrating process.

As shown in Fig. 6, OTW is a 20 bits complement code. The method of limiting 20 bits into 17 bits is very similar to that of limiting 4 bits into 3 bits. For example, if the value of 4 bits complement code doesn’t overflow the range of 3 bits complement code, the first 2 bits must be 11 or 00.

**Fig. 6.** DCO Interface is a digital limiter utilized to deal with the overflow of OTW
Analogously, for example, if the value of OTW is within the range of 17 bits complement code, the first 4 bits must be 1111 or 0000. On the contrary, if the value of OTW overflows the range of 17 bits complement code, OTW will be limited at the minimum or maximum value of 17 bits complement code.

Finally, before entering into the DCO input, the signed DCO control bits will be converted into unsigned bits.

### 3.3 Digital Controller Oscillator

DCO is composed of a $\Sigma\Delta$ DAC and a VCO, as shown in Fig. 7 (a). The $\Sigma\Delta$ DAC is realized by using a Sigma Delta Modulator to control the current through resistor. The architecture of Modulator is a traditional 18 bits (17 bits input and 1 bit dithering) second-order Sigma Delta Modulator, as shown in Fig. 7 (b). In order to avoid the mismatch of the current source, Modulator just has a 1 bit output to dither the current source $I_1$ between resistor $R_1$ and $R_0$. Moreover, in order to avoid the big voltage ripple on the resistor $R_0$, $I_1 \times R_1$ should be about equal to $I_0 \times R_0$. In addition, due to the noise shaping in Modulator, there is a 3rd or 4th-order RC filter at the output of source follow to filter the high frequency quantization noise.

The VCO is a simple ring oscillator which only includes three inverters and a tail MOS resistor. The signal Vctrl can control the transfer current of three inverters through the tail MOS resistor so as to change the frequency of oscillator. The $K_{DCO}$ can be adjusted by varying the size of tail MOSFET and the value of $I_1 \times R_0$.

### 4 Experimental results

The prototype chip layout of RFID Tag implemented in a 180 nm EEPROM technology is shown in Fig. 8. On this chip, CRC block is located in the lower right corner. Its active area is about $380 \mu m \times 720 \mu m$. With 13.56 MHz recovered clock signal (CKV), the maximum power consumption of whole CRC block is about 900 $\mu W$ at 1.8 V power supply.
The whole frequency range of CRC block is from 10.5 MHz to 17.5 MHz.

Fig. 9 shows the testing results of PLL locking state with unmodulated carrier signal from RF200-LT RFID Reader. If the abs of TDC output is less than 4 and keep it for several periods, which mean the phase deviation has been less than 22.5°, the signal PLL_LOCKD will become high level voltage. Under different loop bandwidth such as 30 kHz to 300 kHz, the settling time of PLL is always less than 1 ms, which means the proposed CRC block can definitely finish the synchronization between CKV and received carrier signal within the in-field time. On the contrary, Fig. 10 shows the testing results of PLL locking state with modulated carrier signal. The waveform of modulated carrier corresponds to a “Select” command in receiving mode. When the received modulation carrier signal is zero, EN_CTRL_R will become zero, which means that the output of TDC will become zero and the CRC will become a free running DCO. Moreover, in this receiving period, PLL_LOCKD is equal to 1 all the time, which means the phase error is always less than 22.5°.

Fig. 11 gives some waveforms corresponding to an “Authen” command, which depicts the recovering or calibrating accuracy of CRC in receiving and transmitting mode. With 200 kHz loop bandwidth, the maximum phase deviation during demodulation period (in receiving mode) is 10° and...
Fig. 10. PLL locking state with modulated carrier

Fig. 11. Recovering or calibrating accuracy in receiving and transmitting mode

Fig. 12. (a) The process of in-field detection, (b) The process of off-field detection and from in-field to off-field state conversion
the maximum phase deviation during modulation period (in transmitting mode) is 20°, which are equivalent to 2.9 kHz and 5.9 kHz frequency error accumulated in 9.4 μs free running time. Because the free running time of per bit in transmitting mode is longer than that in receiving mode, the phase deviation in transmitting mode is larger than that in receiving mode.

Fig. 12 (a) exhibits the function verification of in-field detection. For the whole RFID tag system, when Mode_Ctrl <1:0> is 11, the state will become standby; when Mode_Ctrl <1:0> is 01, the state will become normal operation; when Mode_Ctrl <1:0> is 00, the state will become monitoring. Based on the locking state of the proposed CRC, the chip state can change from standby to normal operation. The time of finishing in-field process is about 280 μs. Fig. 12 (b) exhibits the function of off-field detection and the function of in-field/off-field state conversion. Similarly, the chip state can change from standby state to normal operation state, and verse vice.

Finally, the summary of proposed CRC is shown in the Table I. It is worth mentioning that the frequency error is always less than 7 kHz, which absolutely meets the requirement of ISO/IEC 14443 Type-A protocol.

| Table I. Summary of Proposed Clock Recovery Circuit |
|-----------------------------------------------------|
| Output Freq. | 13.56MHz |
| Freq. Range  | 10.5M to 17.5MHz |
| Freq. Resolution | <1kHz |
| Freq Error   | <7kHz |
| Phase Deviation | <20° |
| In-field time | About 280μs |
| Power Dissipation | <900μW at 1.8V |

5 Conclusion

According to ISO/IEC 14443 Type-A protocol, based on a modified digital intensive PLL, the proposed Clock Recovery Circuit applied in HF-Band active RFID tag can not only recover the synchronous clock in the receiving mode but also calibrate the clock’s frequency and phase deviation in the transmitting mode. In the proposed Clock Recovery Circuit, a special Time-to-Digital Converter which has a large phase-detection range is used to deal with the discontinuous recovering or calibration process. Implemented in 180 nm EEPROM technology, the testing results show that the maximum power consumption of Clock Recovery Circuit is about 900 μW at 1.8 V power supply, and the maximum phase deviation in the demodulation and modulation period is respectively less than 10° and 20°.