Contribution to digital power factor correction controllers in high intensity discharge lamps electronic ballast applications

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Abstract: Utility voltage fluctuations not compensated by the low-frequency voltage loop of the power factor correction (PFC) stage cause a perceptible variation in the light emitted by lamps, unpleasant for the human eye and known as flicker effect. A novel extension of the digital control for PFC stages analyses the input voltage, detects the fluctuations in the range of human flicker sensitivity and modifies the PFC output voltage controller to avoid their propagation to the DC bus. The purpose of the controller is to make the PFC compatible with any second stage lamp driver, assuring the mitigation of the lamp light variation caused by utility disturbances in consistent with the human eye perception. The controller is implemented in a field programmable gate array. A constant lamp luminance is achieved with this digital controller with no dependence on the next ballast stage.

1 Introduction

Nowadays, the power conversion systems leverage the digital control capabilities to introduce more flexible power conversion strategies and increase the reliability. A detailed analysis of the benefits of using digital control-based controllers in power electronics and drive applications is found in [1–8]. The designers have the choice between two main families of digital device technologies for fast prototyping. The first family [1–4] is associated to microcontrollers and digital signal processor (DSP) controllers. These components integrate a performing microprocessor core along with several peripherals. The alternative family is the field programmable gate arrays (FPGAs) technology [9, 10]. These devices consist of predesigned elementary cells and interconnections that are fully programmable by the end user.

In DC/DC conversion, it is common that digital controllers pay close attention on the voltage regulation, with improved dynamic performance under input voltage and load transients [11, 12].

The key properties of high intensity discharge (HID) lamps include higher energy efficiency, compact size, good colour rendering, whiter light (higher colour temperature) and longer lifetime [13–19]. Typical applications range from car headlamps, greenhouse lighting, interior lighting, industrial sector and urban lighting applications. Since the urban lighting consumption represents a non-negligible part of the total energy amount consumed on Earth, improvements in the supply, efficiency and light quality are investigated. Digital control is a key technology to provide higher performance [14–16] to the ballast system. In Fig. 1a, a typical two-stage electronic ballast solution is shown, including a power factor correction (PFC) [20] and an inverter. On the other hand, the same system is depicted in Fig. 1b with a digital controller.

Light emitted by HID lamps is very sensitive to voltage supply fluctuations, producing an effect on the human visual perception, known as flicker [21–26]. Flicker is a very uncomfortable effect, which would cause a lot of human physiological effects, as it is indicated in [24, 25]; so it is addressed as a safety and health issue at work. These fluctuations can be caused by the connection and disconnection of important loads (high-power motors, PFC bank capacitors etc.), compressors, resistive welding machines or arc furnaces. Flicker frequency can be perceived by the eye–brain set, when it is within a range of frequency that extends from 0.5 to 25 Hz [23]; and the maximum flicker perception occurs at around 10 Hz [26].

In two-stage electronic ballast, where the inverter may operate in open loop, the PFC outer loop and its output bulk capacitor, C, are the elements that attenuate the propagation of the utility voltage fluctuation to the DC bus and then contribute to reduce the light variation in HID lamps. This work presents an extension of the PFC control technique presented in [11, 12] specifically adapted to prevent the lamp flickering. This extension can also be applied to digital PFC controllers that use input current sensor to improve the performance in lamp driver applications. The present work has precedents in the...
conference papers [23, 27, 28]. An update over those works includes a more detailed presentation of the signals acquisition circuit, identification of the conventional voltage regulator, the additional regulator to prevent the lamp flickering and the hardware connection to achieve a consistent operation. A novel algorithm to detect the fluctuations over the nominal incoming voltage level and select the condition to activate the additional controller to prevent the lamp flickering is presented in this work. Also, the experimental results have been updated including frequency response oscillograms. The amplitude of the low-frequency PFC output ripple voltage caused by the fluctuation in the utility voltage is attenuated by increasing the PFC output capacitance. This technique can also be applied to attenuate the propagation of the utility disturbances that cause flickering, but a larger capacitor increases the volume and size of the converter and as long as the electrolytic capacitor cannot be replaced by other technology, the circuit lifetime is penalised [29–32]. An alternative is the implementation of a wide bandwidth controller in the inverter stage [19]. In [33], two control algorithms are presented for distribution static synchronous compensator (DSTATCOM) to mitigate voltage fluctuation caused by electric arc furnace loads. Representative works on utility voltage detections are [34, 28], where a technique to monitor voltage fluctuations in the power system with a least-squares-Kalman optimisation technique for fundamental frequency voltage phasor estimation and an input instantaneous voltage detection algorithm, under ideal utility mains, are presented, respectively.

The proposed digital compensation of the voltage fluctuation does not modify the original PFC output voltage controller if low-frequency fluctuations of the input voltage are not detected. When these fluctuations appear, the proposed controller changes the voltage loop dynamic response to minimise the DC voltage ripple at the fluctuation frequency, assuring a constant light luminance in the lamp and avoiding the optical flicker perception. No extra cost and no extra analogue components are introduced whenever the FPGA can host the small additional digital block. To clearly show the performance achieved, a practical application with a 150 W high pressure sodium (HPS) lamp supplied by an open-loop resonant inverter (RI) as second stage (Fig. 1) is presented.

The objectives of this paper are: (i) to develop a universal voltage fluctuation detection method that fits the standard definition human perception range; (ii) to use the lowest PFC output capacitance, $C$, by extending the capabilities of the digital output voltage loop and (iii) to minimise the flicker perception for the human eye caused by the utility disturbances.

For further hardware simplification of the lamp driver-oriented PFC controller, the implementation has been carried out as an extension of the digital control technique presented in [11, 12], which requires neither current sensor nor high-speed analogue-to-digital converter.

The paper is organised in five sections. After introduction, the proposed digital PFC controller is presented in Section 2; with a first subsection about the input current control and a second subsection with the digital outer voltage loop. In Section 3, the voltage fluctuation detection algorithm is shown. In Section 4, the experimental results with a HID lamp are presented, finalising with conclusions.

2 Digital PFC controller

2.1 Inner current loop

Some advantages that motivate the use of digital control in PFC stages include: reduction of discrete components, ease of controller implementation and extension of its performance limits, reduction of size and reduction of sensitivity to parameter tolerances [35–37].

The principle of operation of the digital current control to achieve PFC used in this work, and depicted in Fig. 2, has been presented in [11, 12, 35, 36] where an input current
(i_{in}) estimator removes the need for current analogue-to-digital (A/D) conversion, and the input and output voltages are measured using the analogue-to-digital converters (ADCs) represented in green in Fig. 2. Avoiding the current measurement means a step-forward with respect to analogue controllers, which also helps to increase efficiency and reduce the total cost and complexity. The input and output voltages measurements (v_{inADC} and v_{oADC}) are used to estimate the input current digitally (i_{inreb}). As ADCs, first-order ad hoc sigma–delta converter with a low quantity of analogue components (an RC filter and a comparator) [11] is used in the output voltage measurement. A commercial ADC is used for the input voltage A/D conversion. The analogue circuitry used to substitute the current sensing circuit is presented in blue.

Drain-to-source metal-oxide semiconductor field-effect transistor voltage is adapted as digital input signal (v_{ds}) in order to measure and compensate drive signal’s delays. With this digital controller, a sinusoidal current waveshape is obtained, independently of the voltage or power conditions.

2.2 Outer voltage loop

In steady-state operation, the PFC output voltage loop has a low bandwidth (up to 10 Hz) so not to interfere with the inner loop that keeps the current shape proportional to the input voltage to comply with the IEC 61000-3-2 standard for class C equipment [20].

The action of the low bandwidth cannot reject the low-frequency fluctuations and they are propagated through the PFC and inverter stages, perturbing the lamp current and voltage, as is depicted in Fig. 3a. The current fluctuation causes the lamp light variation, and then the flicker effect. To attenuate this flicker effect, the capacitance of the output bulk capacitor (C shown in Fig. 2) in the PFC stage could be chosen higher than the calculated with (1), which determines the capacitance needed to limit the amplitude of the voltage ripple at twice the line frequency, \( \Delta V_o \), below a given value \( \Delta V_{o_{min}} \), supplying a power rate \( P \), where \( V_{o} \) and \( V_{o_{min}} \) are the average and minimum output voltage in steady state, respectively, and \( T_u \) is the utility period.

\[
C > \frac{PT_{\mu}}{V_o^2 - V_{o_{min}}^2} \tag{1}
\]

This solution needs electrolytic capacitors that limit the useful life of the ballast system.

Fig. 3 Waveforms

- a Under voltage fluctuations situation: utility voltage, \( v_{in} \), PFC stage output voltage, \( V_o \), and lamp current, \( i_{lamp} \)
- b \( v_{in} \), \( V_o \), \( i_{lamp} \), and utility current, \( i_{in} \), changing the voltage loop. Low bandwidth loop during steady state and extended bandwidth loop under utility voltage fluctuation

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bandwidth and a current shape proportional to the input voltage and also has an extended bandwidth loop in the utility voltage fluctuations situation with current distortion. Standard IEC 61000-3-2 class C [20] is not applied in the presence of these utility transients. A constant PFC stage output voltage \( (v_o) \) is achieved despite input voltage low-frequency fluctuations. With this, constant lamp current \( (i_{\text{lamp}}) \), and then constant lamp light luminance are also achieved.

In the previous work [27], the design of a small-signal model of the non-linear-carrier (NLC) controlled boost rectifier and the analysis to obtain the control-to-output transfer function \( G(s) \) were presented following [38]. The output voltage control loop has been designed using the \( G(s) \), whose expression is

\[
G(s) = \frac{V_o(s)}{V_m(s)} = \left( \frac{V_{\text{in,RMS}}}{V_o} \right)^2 \frac{R}{3r_s} \frac{1}{1 + s(RC/3)}
\]

where \( r_s \) is the virtual current sensor resistor, \( R \) is the load and \( C \) the output capacitor, as shown in Fig. 4, while \( V_m \) is the NLC control voltage. The details of the sequence to obtain (2) are given in the Appendix.

A digital voltage loop is shown in Fig. 4a, where a low bandwidth compensator, \( C_{ss}(z) \) is implemented to assure that the output voltage that supplies the second stage follows the reference \( (v_{oref}) \). The block diagram of the proposed digital controller is presented in Fig. 4b, where the block ‘Current Loop’ represents the NLC controller presented in Fig. 2. When utility disturbances appear, an utility voltage fluctuations detector, presented in Section 3, activates the compensator \( C_{\text{fluc}}(z) \) in order to extend the bandwidth of the PFC outer loop, avoiding their propagation to the lamp at the expense of increasing the

| \( C \) | \( G(z) \) | \( C_{ss}(z) \) | \( C_{\text{fluc}}(z) \) |
|---|---|---|---|
| 68 \( \mu \text{F} \) | \( 1.995 \times 10^{-7} \) \( \frac{z}{z - 0.9998} \) | 0.75 \( \frac{z}{z - 0.9375} \) | 4096 \( \frac{1}{z(z - 0.9375)} \) |

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**Fig. 5 Detection of the fluctuation**

a Voltage levels defined to detect the utility voltage fluctuations

b Input voltage fluctuation detection algorithm flowchart
utility current distortion. With this capability, a low C value can be utilised. The design of the controllers was presented in the previous works [27, 28], using the following sequence: (i) A proportional–integral (PI) action is selected for both controllers as the right option to obtain high loop gain at very low frequency and around 90° phase lag at the cross-over frequency. At least 52° phase margin (pm) is desired to prevent transient oscillations. (ii) \( C_{ss}(z)\) is designed to set the loop gain crossover frequency, \( f_c \), around 1 Hz, thus avoiding line current distortion in steady state [3]. (iii) \( C_{fluc}(z)\) is designed to set, \( f_c \), around 100 Hz, a decade above 10 Hz, which determines the upper flicker detection limit of the human eye. (iv) To simplify the digital implementation in the FPGA, the coefficients of both controllers are approximated to powers of 2, verifying the resulting \( f_c \) and pm with MATLAB–SISOTOOL®. Table 1 shows the plant and the designed controllers in the z-domain.

3 Input voltage fluctuations detection algorithm

The utility peak voltage value (\( v_{in,peak} \)) is obtained, cycle by cycle, with a digital peak detector of the digital input voltage (\( v_{in,ADC} \)). With this value, the steady-state utility peak voltage and three different voltage levels are defined, as is shown in Fig. 5a. The algorithm defines the non-fluctuation band (called ‘In’ in Fig. 5a), with the steady-state utility peak voltage, \( v_{in,peak} \pm 2\% \).

When the utility peak voltage is found outside this band, that is, ‘Above’ or ‘Below’ in Fig. 5a, the algorithm determines whether there is a fluctuation in the most sensitive frequency range of the human eye, between 0.5 and 25 Hz. It is assumed that fluctuation component of the utility voltage is approximately a symmetric function, that is, it can be reflected around a specific time location. Consequently, if the fluctuation period is \( T_f \) for every \( T_f/2 \) the utility voltage envelope crosses the limits of the voltage band. When the first change in the peak value is detected, the algorithm measures the time (\( T_f \)) throughout and the peak voltages are maintained in each band. If \( T_f \) lasts between 0.0 and 1 s (half period of a 25 and 0.5 Hz fluctuation, respectively), it is considered that there is a utility voltage fluctuation. Therefore, precise fluctuation frequency is only measured, if it is in the 0.5–25 Hz range, where it produces an unpleasant optical flicker perception.

The input voltage fluctuation detection algorithm flowchart is shown in Fig. 5b. The signal ‘Fluctuation’ is set to ‘1’ under flicker situation, and therefore the time during the wide bandwidth voltage loop has to be applied (\( T_{wide-loop} \)) is determined.

4 Experimental results

Laboratory experiments that illustrate the performance of the digital controller have been carried out with electronic ballast for a 150 W HPS lamp (LUCALOX). A boost converter has been used as PFC stage. The values of the components are: \( L=3.2 \text{ mH} \), \( V_{in}=230 \text{ V} (50 \text{ Hz}) \), \( f_{sw}=73 \text{ kHz} \), \( V_o=420 \text{ V} \) and \( P_o=150 \text{ W} \). The output bulk capacitance is 68 \( \mu \text{F} \).

A LCC half-bridge RI is used as second stage. It provides the required ballast action at reduced cost and behaves as an input voltage-dependent power source. Since the
compensation of the utility fluctuation is carried out by the PFC stage, it can be connected to other type of second stage and light sources [14, 15, 28, 39].

The LCC resonant circuit is designed to have zero resonant current phase lag at the end of the lamp lifetime, and it works in a frequency window free of acoustic resonance, which is a valid solution for 150 W HPS lamps [14]. This inverter operates in the open loop, so it is a system without the capability for compensation of input voltage disturbances, being a good example to illustrate the performance of the proposed digital controller. Zero voltage switching is guaranteed in the RI along with a minimum reactive component in the resonant tank considering the whole life span of the lamp. Using the design sequence described in [14], the RI design is defined by $Z_p = R_{lamp}/Q_p = 170 \Omega$, $L_r = 115 \mu H$, $C_p = 5.7 \text{nF}$ and $C_s = 330 \text{nF}$.

For laboratory test purposes, the digital control circuit is implemented in a Xilinx Spartan 3 family XC3s200e FPGA. In order to measure the behaviour of the system with the proposed digital control, an APDS-9007 ambient light photo sensor is used. This photo sensor has a spectral response close to the standard photopic observer. The photo sensor is placed in front of the lamp to get an output voltage proportional to the brightness of the lamp light, according to what human eye perceives). An Agilent 6813B AC programmable power source is used to supply the HID lamp power supply.

Fig. 6a shows the PFC stage input current ($i_{in}$) and the input voltage ($v_{in}$) waveforms in steady-state situation. Despite not measuring the input current, PFC is successfully achieved. The measured power factor was 0.991 with 168 W input power ($P_{in}$).

In Fig. 6c, the fast Fourier transform (FFT) on the input current in comparison with the IEC 61000-3-2 class-C limits shows that all current harmonics are below the limits recommended by the standard.

Fig. 6b shows the PFC stage input current ($i_{in}$) and the input voltage ($v_{in}$) waveforms during utility fluctuation with the wide bandwidth outer loop. In this case, the power factor is 0.91. The input current is distorted because of the faster dynamic response. Fig. 6d shows that the harmonic content of the input current does not comply with the IEC 61000-3-2 class C limits, but in the utility fluctuation case the mentioned standard does not apply [20].

The phase margin and the crossover frequency are 73° and 0.61 Hz for the reduced bandwidth voltage loop (Figs. 6a and c),

Fig. 7 Bode plots of the different voltage loops
Light grey: Bode plot for steady-state condition with reduced bandwidth
Dark grey: Bode plot for transient state during fluctuation of the input voltage with wider bandwidth

Fig. 8 PFC stage output voltage ($v_o$), the lamp lightlux level measured by the photo sensor ($I_{x\_LAMP}$) and input voltage ($v_{in}$) under 10% $V_{in\_rms}$ and 10 Hz fluctuation
$v_{in} = 230–207 \text{Vrms}$, $50 \text{Hz}$, $v_{o} = 420 \text{Vdc}$, $P_{in} = 150 \text{W}$ and $C = 68 \mu F$ output capacitor

a With a reduced voltage loop bandwidth
b With a wide voltage loop bandwidth. Ch2 input voltage, 50 V/div, Ch1 lamp light flux. Ch3 output voltage 50 V/div. Time scale: 40 ms/div
and 78.8° and 149 Hz for the wide bandwidth loop (Figs. 6b and d). Output voltage reference is the same for both controllers; in this case 420 Vdc. Fig. 7 shows the bode diagrams of the extended bandwidth (blue) and the reduced bandwidth (green) output loops.

The PFC stage DC output voltage ($v_o$), the lamp light lux level measured by the photo sensor ($I_{L,\text{LAMP}}$) and the input voltage ($V_{in}$) to the PFC stage under a 10% fluctuation ($\Delta V$) in the input voltage (programmed in the AC power source) are shown in Fig. 8a when the PFC uses the slow PFC outer loop, and in Fig. 8b when the PFC uses the fast PFC outer loop to compensate the fluctuation sensitivity.

Fluctuation frequency has been set close to the maximum level of human eye flicker perception, that is, 10 Hz. Fig. 8 shows the same input voltage and the differences on $I_{L,\text{LAMP}}$ and $v_o$ waveforms between applying or not the extended bandwidth outer loop. In Fig. 8a, the $I_{L,\text{LAMP}}$ signal has a fluctuation of 10 Hz (added to the output voltage 100 Hz fluctuation, imperceptible by the human eye). On the other hand, in Fig. 8b this fluctuation is highly attenuated, because the wide bandwidth voltage loop is applied. In this case, lamp light variation and flicker perception disappear.

Fig. 9 shows the behaviour of the input voltage fluctuation detection algorithm. Fig. 9a displays the signal ‘Fluctuation’ under different utility voltage conditions. At first, a 230 Vrms (325 V peak) utility voltage is applied. After 27 s, a step down of 30 Vrms is applied; and then, after 30 s, 210 Vrms (297 V peak) input voltage is applied. In this situation, a 10% and 10 Hz fluctuation is imposed (210–189 Vrms).

The algorithm determines the steady-state peak voltage and defines the ±2% ‘In’ band. When the fluctuation is detected, the signal ‘Fluctuation’ turns to ‘1’. The extended bandwidth voltage loop is applied during the time $T_{\text{wide-loop}}$. Fig. 9b demonstrates the result of the algorithm behaviour at the end of the fluctuation. It can be seen that a 1 s period is necessary to determine that the fluctuation has finished.

5 Conclusions

A digital controller for PFC circuits applied to HID lamp electronic ballast has been proposed. This controller, implemented in a FPGA, makes the utility current to meet the IEC 61000-3-2 class C limits in steady-state and rejects input voltage fluctuations to avoid lamp flicker [20].

The proposed controller extension, specific for ballast application, is applied to a PFC controller which requires no current sensor to shape the input current. The input current of the ballast system is estimated from the input and output voltages of the PFC stage. Avoiding the current measurement is a significant advantage with respect to other controllers because it eliminates a hot spot in the circuit and improves the noise immunity of the control circuit.

A voltage fluctuation detection algorithm is used to avoid the propagation of the fluctuations to the lamp. The algorithm measures the steady-state utility peak voltage and detects low-frequency voltage fluctuations in the most sensitive frequency range of the human eye. Depending on the detected disturbances, the digital controller modifies the voltage-loop speed of the PFC stage, reducing the light flicker emission within the frequency band of human perception of the flickering. The proposed digital controller is a valid solution even though the higher bandwidth (149 Hz) voltage loop distorts the input current. This is compatible with the IEC 61000-3-2 standard because the essay to define the standard compliance is defined in steady-state and the utility voltage level fluctuation implies a transient state.

A two-stage ballast system (boost PFC + resonant inverter) that supplies a 150 W HPS lamp has been subjected to low-frequency utility fluctuations. These fluctuations have been programmed with an AC power electronic source in order to produce a variation in the light emitted close to the maximum level of human eye flicker perception, emulating an industrial environment under grid disturbances.

A constant light luminance in the lamp is achieved despite frequency utility mains fluctuations and without extra components in the external digital circuit. Moreover, the size of the PFC output capacitor is reduced, decreasing the volume and cost, and increasing the lifetime of the converter.

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7 References

1 Monmasson, E., Idkhajine, L., Cristea, M.N., Bahri, I., Tisan, A., Naouar, M.W.: ‘FPGAs in industrial control applications’, IEEE Trans. Ind. Inf., 2011, 7, (2), pp. 224–243.
2 Monmasson, E., Cristea, M.: ‘Guest editorial special section on field programmable gate arrays (FPGAs) used in industrial control systems’, IEEE Trans. Ind. Electron., 2007, 54, (4), pp. 1807–1809.
3 Maksimovic, D., Zane, R., Erickson, R.: ‘Impact of digital control in power electronics’. Proc. IEEE Int. Symp. Power Semiconductor Devices and ICs (ISPSD 2004), 24–27 May 2004, pp. 13–22.
4 Kazmierkowski, M.P., Jasinski, M., Wrona, G.: ‘DSP-based control of grid-connected power converters operating under grid distortions’, IEEE Trans. Ind. Inf., 2011, 7, (2), pp. 204–211.
Appendix

The implemented non-linear controller (inner current control) defines $d$ by comparing $(i_L(t_0) + i_L(t))T$ multiplied by a real or artificial sensor resistance $r_s$ with the carrier signal $v_m(1 - (t - t_0)/T)$ in each switching period. The variable $v_m$ is the control variable that will be provided by the outer voltage loop. The function $i_L(t)$ represents the current through the inductor in the time domain and $i_L(t_0)$ is the current through the inductor at the beginning of a given switching period. Therefore, the condition

$$\frac{i_L(t_0) + i_L(t)T}{2} r_s = v_m \left(1 - \frac{t - t_0}{T}\right)$$

results in

$$\frac{i_L(t_0) + i_L(t) + iT}{2} r_s = v_m \left(1 - \frac{T + iT}{T}\right)$$

Assuming that the computed value is the current through the inductor averaged over the switching period, $T$, $i_L(t)_T$ the previous expression can also be rewritten for each switching period as

$$\langle i_L(t) \rangle_T r_s = v_m(1 - d)$$

Assuming also high switching frequency in comparison with the dynamics of the averaged variables, this equation can be defined in the time-domain

$$\langle i_L(t) \rangle_T r_s = v_m(t) \frac{v_m}{(v_m)_T}$$

The quasi-static approximation, which assumes ac line variations much slower than the converter dynamics, reveals that the non-linear controller shapes the current to be proportional to the input voltage when the ripple of the output voltage is low, as desired for the PFC application, justifying the proposed non-linear controller.
Perturbing the control variable \( v_m \) around a given operation point defined by the DC output voltage \( V_o \), inductor current \( I_L \) and control signal \( V_m \), values with \( V_o = (V_{in}(1 - D)) \), \( I_L = (V_{in} / R(1 - D)) \) and \( I_L/T_w = V_{in}(1 - D) \), the following transfer function is obtained

\[
I_L(s) = V_m(s) \frac{V_{in}}{R_o V_o} - V_o(s) \frac{V_m V_{in}}{R_o} \quad (7)
\]

From \( \langle i_L \rangle_T \) in (6), the averaged current through the RC load, that is, the load resistor \( R \) and the output filter capacitor \( C \) shown in Fig. 4b, in the switching period, \( \langle i_{RC} \rangle_T \) is obtained as

\[
\langle i_{RC} \rangle_T = \langle i_L \rangle_T (1 - d) = \langle i_L \rangle_T \frac{V_{in}}{V_o} \quad (8)
\]

Assuming sinusoidal input voltage and using the notation \( \langle i_L \rangle_{T, \max} \), \( \langle i_{in} \rangle_{T, \max} \), for the averaged input current and voltage at the ac utility angle \( \pi/2 \), the output voltage results from averaging the converter operation over half line period \( (T_u/2) \), and the transfer function that defines the plant is the response of the averaged over the utility period model, \( \langle v_o \rangle_{T, \max} \) to perturbations of \( v_{in} \).

The quasi-static approximation with low output voltage ripple assumes \( \langle v_o \rangle_T = \langle v_o \rangle_{T, \max} \). Therefore, the current through the load averaged over the utility period is calculated as

\[
\langle i_{RC} \rangle_{T, \max} = \frac{1}{\pi} \int_{-\pi/2}^{\pi/2} \frac{\langle i_L \rangle_{T, \max} \langle v_{in} \rangle_{T, \max}}{\langle v_o \rangle_T} \sin^2 (\omega t) d(\omega t)
\]

\[
= \frac{\langle i_L \rangle_{T, \max} \langle v_{in} \rangle_{T, \max}}{2\langle v_o \rangle_{T, \max}} = \frac{\langle p \rangle_{T, \max}}{\langle v_o \rangle_{T, \max}}
\]

From the result defined in the time-domain, a small-signal expression, in this case defined in the Laplace domain can be obtained, where the upper case notation without the Laplace complex argument \( s \) is used for the DC values. Therefore, \( I_{RC}(s) \), \( I_{L, \max}(s) \), \( V_{in, \max}(s) \) and \( V_o(s) \) correspond to the small-signal perturbation of \( \langle i_{RC} \rangle_{T, \max} \), \( \langle v_{in} \rangle_{T, \max} \) and \( \langle v_o \rangle_{T, \max} \), respectively. \( V_{in, \max} \), \( I_{L, \max} \), \( V_o \) and \( R \) define the DC operation point

\[
I_{RC}(s) = I_{L, \max}(s) \frac{V_{in, \max}^2}{2V_o} + V_{in, \max}(s) \frac{I_{L, \max}}{2V_o} - V_o(s) \frac{1}{R} \quad (10)
\]

The plant to be controlled by the outer loop is obtained by introducing (7) into (10), and using \( V_m(s) \) as the only input, that is, \( V_{in, \max}(s) = 0 \).

\[
I_{RC}(s) = V_m(s) \frac{V_m^2}{2V_o} - V_o(s) \frac{2}{R} \quad (11)
\]

\[
V_o(s) = I_{RC}(s) \frac{R}{1 + sRC} \quad (12)
\]

The use of a resistance as the small-signal load is justified because here it is considered the case of the next section, that is, the inverter, operating in open loop and the range of the small-signal perturbation frequency is low. A closed-loop controlled inverter would modify its small-signal behaviour as a load.

\[
G(s) = \frac{V_o(s)}{V_m(s)} = \left( \frac{V_{in, \max}}{V_o} \right)^2 \frac{R}{3r_o} \frac{1}{1 + sRC/3} \quad (13)
\]