Front-end Electronics for Timing with pico-second precision using 3D Trench Silicon Sensors

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ABSTRACT: The next generation of collider experiments require tracking detectors with extreme performance capabilities in terms of spatial resolution (tens of µm), radiation hardness ($10^{17} \text{ 1 MeV n}_{eq}/\text{cm}^2$) and timing resolution (tens of ps). 3D silicon sensors, recently developed within the TimeSPOT initiative, offer a viable solution to cope with such demanding requirements. In order to accurately characterize the timing performance of these new sensors, several read-out boards, based on discrete active components, have been designed, assembled, and tested. The same electronics is also suitable for characterization of similar pixel sensors whenever timing performance in the order and below 10 ps is a requirement. This paper describes the general characteristics needed by front-end electronics to exploit solid-state sensors with fast timing capabilities and in particular, showcases the performance of the developed electronics in the testing and characterization of fast 3D silicon sensors.

KEYWORDS: Particle tracking detectors (Solid-state detectors); Radiation-hard detectors; Solid state detectors; Timing detectors

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1 Introduction

An increasingly important requirement in experimental high energy physics concerns the need of introducing timing measurements at the level of the single pixel sensor. As an example, the Upgrade-II of the LHCb experiment at the CERN LHC has requirements of concurrent space and time resolutions of the order of 10 μm and at least 50 ps respectively at the single pixel level [1]. The necessary spatial resolution can be obtained using pixels with an appropriate pitch (e.g. ~ 50 μm), whilst regarding the requirement on temporal resolution, different technologies for sensors have been proposed in recent years, both with and without internal gain [2, 3]. A crucial requirement to remember is that the high constraints on spatial and temporal resolution must be maintained simultaneously alongside high radiation resistance against fluences \( \phi = 10^{17} \) 1 MeV n_{eq}/cm² [4].

To fulfill these extreme requests, a possibility is to use 3D pixel sensors coupled with suitable electronics [5, 6]. The TimeSPOT initiative [7] (standing for TIME and SPace real-time Operating Tracker) aims at developing a full prototype detection system (based on 3D sensors) suitable for particle trackers of future particle physics experiments. The TimeSPOT project also includes the development of dedicated electronics through the production of an ASIC (Application Specific Integrated Circuit) with a 28 nm process, which includes an analog front-end and a TDC for each pixel. Pixels are arranged in a 32 × 32 matrix, giving a total of 1024 channels [8]. The final goal is to realize a final demonstrator, consisting of a complete 4D tracking system that satisfies the desired...
performances. The obtainable performances can be strongly limited by the characteristics of the electronics, in particular if strong constraints are present. For example, due to power dissipation capabilities, the LHCb detector has a maximum allowed power of about $1.5 \text{ W/cm}^2$.

While the integrated electronics is developed, characterization of the temporal performance with these 3D sensors has been performed using the discrete component electronics described in this paper. These electronics were designed in order to obtain the best possible timing performance without worrying about power consumption. The aim was to understand what could be the maximum performance obtainable from the system if operated in the best possible conditions. This has been done, starting from the study of the characteristics of the input signal that the electronics receive, i.e. the current generated in the pixel by a Minimum Ionising Particle (MIP).

We therefore start with section 2 where some general concepts are introduced. In section 3, the 3D silicon sensors developed within the TimeSPOT collaboration are presented as well as the characteristics of the signals that these sensors produce. Section 4 is dedicated to a description of the circuit topology chosen for the analog front-end, the discrete active component characteristics needed and the results of Spice simulations about the expected performance of the system. In section 5, the single channel and multi-channel boards that have been built are shown, whilst in section 6, some examples of applications and results obtained with our boards are presented.

2 Time resolution of the System

In this paper, any system designed for timing consists of a solid-state sensor (or pixel) and its related electronics. Neglecting Time-to-Digital-Conversion (TDC) resolution, and assuming a suitable discrimination method to correct for time-walk variations, there are two dominant contributions to the timing resolution of a sensor+electronics system,

$$\sigma_t^2 \cong \sigma_{\text{sens}}^2 + \sigma_{\text{ej}}^2.$$  \hspace{1cm} (2.1)

$\sigma_{\text{ej}}$ is electronic jitter, and depends both on the output noise of the amplification stage $\sigma_v$ and on the slope of the signal at the chosen discrimination threshold $V_{\text{thr}}$,

$$\sigma_{\text{ej}} \equiv \frac{\sigma_v}{V_{\text{thr}}}.$$  \hspace{1cm} (2.2)

The term $\sigma_{\text{sens}}$ represents contributions to the timing resolution due to the pixel. Our aim is to design a front-end electronics stage that can minimize both contributions ($\sigma_{\text{ej}}$ and $\sigma_{\text{sens}}$) to the timing resolution $\sigma_t$.

The effect of the system on the input signal given by the sensor current $I_D(t)$ (assuming such system as linear) can be represented by its transfer function. This is normally expressed in the Laplace domain as a function $R_m(s)$ such that,

$$V_{\text{out}}(s) = I_D(s)R_m(s),$$  \hspace{1cm} (2.3)

where $V_{\text{out}}(s)$ and $I_D(s)$ are the Laplace transforms of the time domain signals $V_{\text{out}}(t)$ and $I_D(t)$ respectively. The timing performances of the system are measured through the output voltages $V_{\text{out}}(t)$ and depend on both the characteristics of the input currents supplied by the sensor and on
the shaping action of the electronics enclosed in the transfer function \( R_m(s) \). Transfer functions commonly used for shaping are unipolar signal shaping transfer functions \([9]\), defined by,

\[
R_m(s) = \frac{R_{m0}}{(1 + s\tau)^n}. \tag{2.4}
\]

The transfer function \( R_m(s) \) is a Trans-impedance as it converts an input current to a voltage output, \( \tau \) is its time constant, while \( R_{m0} \) is the DC-Trans-impedance of the system measured in Ohms.

Moving to the Fourier domain with the substitution \( s = j2\pi f \) we find the frequency \( f_{-3\text{dB}} \) at which the modulus of eq. (2.4) drops by a factor \( \sqrt{2}/2 \). The frequency \( f_{-3\text{dB}} \) will be the bandwidth of the trans-impedance \( R_m(s) \) and is given by,

\[
f_{-3\text{dB},n} = \frac{1}{2\pi \tau} \left( 2^{\frac{1}{n}} - 1 \right)^{\frac{1}{2}}. \tag{2.5}
\]

Characteristics of the output signal such as the maximum amplitude \( V_{\text{peak}} \), the peaking time \( T_{\text{peak}} \) and SNR (signal to noise ratio) will depend on the shape and amplitude of the input current, the \( R_{m0} \) value and the time constant \( \tau \) of the system. This will be better clarified later when the theoretical estimates of the performance of the chosen circuit for the electronics developed in section 4.2.1 are shown.

### 3 TimeSPOT 3D silicon sensors

Different solutions for solid-state planar sensor geometries have been proposed over the years, with or without gain mechanisms \([2, 3]\) and showing very good timing performance. An interesting alternative to such sensors is to consider a pixel with vertical (3D) geometry \([5, 6]\). This solution completely decouples the thickness of the pixel from its inter-electrode distance. The former establishes the amount of charge produced by a MIP by linear energy deposit, whilst the latter determines the duration of the induced current signal. This feature can give the decisive advantage of larger freedom in the optimisation of the pixel geometry towards maximum timing performance. Such advantage was exploited in the TimeSPOT project \([7]\), which developed a specific and optimised 3D silicon sensor, characterized by a trench geometry \([10–13]\). The optimised geometry of the single pixel is shown in figure 1c). The pixel features a pitch of 55 \( \mu \text{m} \) \([12]\). Two ohmic trenches (represented in blue in figure 1c) of dimensions 2.5 \( \times \) 55 \( \times \) 150 \( \mu \text{m}^3 \) are located at the two opposite sides of the pixel. A third trench of dimensions 5x40x130 \( \mu \text{m}^3 \) is placed at the pixel centre, parallel to the two ohmic electrodes and serves as readout electrode. 3D-trench sensors have been produced with several layouts: single pixels, double pixels, and strips with multiple single pixels connected together. The amount of charge carriers generated by an ionizing particle depends on the thickness of the pixel and on the Linear Energy Transfer (LET) of the particle; for one MIP on a pixel 150 \( \mu \text{m} \) thick, the released charge corresponds to a Most Probable Value (MPV)

\[
Q_{\text{MPV}} \sim 2 \text{fC}. \tag{3.1}
\]

A key feature of a solid state sensor is its capacitance, which imposes a limit on system performance as it affects sensitivity, noise and jitter. Measurements \([14]\) on the devices of the first batch produced in 2019 showed a value of the single pixel capacitance \( C_D \) of

\[
C_D \sim 70 \div 75 \text{fF}. \tag{3.2}
\]

Strip detectors have a bigger capacitance according to the number of pixel connected together.
Figure 1. 3D-trench sensors fabricated at Fondazione Bruno Kessler (FBK, Trento, Italy) within the TimeSPOT project: A) single pixel sensor, B) strip sensors with multiple single pixel connected together, C) geometry and size of the single pixel.

Current signals induced by ionising particles in the electrodes of this sensor type have been studied and simulated extensively using a dedicated custom software package: TCoDe [12, 15]. In 3D geometries, the duration of current signals depends on the position of the track with respect to the electrodes. To define the duration of the signals of the measured signals, a possible criterion is to consider the time necessary to induce a significant fraction of the total induced charge (e.g. 99.9%). Calculating time in this way will give the collection time \( t_c \) of the considered current. The set of all collection times relating to the entire active area of the sensor can be included in a characteristic distribution, called Charge Collection Time distribution (CCT) and shown in figure 2. The CCT distribution indicates an average charge collection time \( t_c \sim 200 \) ps and a standard deviation \( \sigma_{t_c} \sim 50 \) ps. Great effort has been made to optimize the geometry of these sensor types [15], with the goal of reducing the variation of signal duration and shape, and minimizing the standard deviation \( \sigma_{t_c} \) which is directly related to the intrinsic resolution of the sensor \( \sigma_{\text{sens}} \).

An example of a typical current signal is shown in figure 3 (left). As a reasonable approximation, it can be assumed as a simple rectangular pulse with duration equal to the charge collection time \( t_c \). Considering the frequency domain, the spectrum of this rectangular pulse of figure 3 (left), is given by the known Sinc function: figure 3 (right).

The signal bandwidth is typically considered to be \( f_{\text{BW}} = \frac{1}{t_c} \), and for \( t_c = 200 \) ps, \( f_{\text{BW}} = 5 \) GHz, however the spectrum of the signal (figure 3 (right)), shows that the frequency components exhibit gradually decreasing amplitudes as frequency increases. It is therefore reasonable to determine the signal bandwidth as the frequency at which the current spectrum amplitude drops by a factor of \( \frac{1}{\sqrt{2}} \). This can be done with a second order approximation of the Sinc function, finding,

\[
f_{-3\text{dB}} \sim \left( \frac{6(2 - \sqrt{2})}{2} \right)^{\frac{1}{2}} \frac{1}{\pi t_c} \approx 0.42 \frac{1}{t_c}.
\]  

(3.3)
Figure 2. CCT distribution of the currents of the TimeSPOT 3D trench detector obtained with the custom package TCode [12, 15]. The average charge collection time is $t_c = 234$ ps while the standard deviation is $\sigma_{t_c} = 53$ ps.

Figure 3. Figure on the left: an example of a simulated current of the single pixel obtained with TCode (purple line) and the modeled current as a rectangular pulse with duration $t_c$ equal to the charge collection time (green line). Figure on the right: same currents of the plot on the left but in the frequency domain: it can be seen how most of the signals is concentrated a low frequencies. The black line represent the signal bandwidth as defined in eq. (3.3).

The average bandwidth of the signal is therefore equal to

$$f_{3dB} \sim 2.1 \text{ GHz.} \quad (3.4)$$

The signal bandwidth found in eq. (3.4) places strong constraints on the characteristics of the electronics in order to appreciate the speed of such sensors. As an example, a model for the electronics is considered, given by a first-order transfer function with time constant $\tau = R_{in}C_{in}$. 
$R_{in}$ represents the input resistance of the electronics and $C_{in}$ represents the total input capacitance given by the sum of the capacitance $C_D$ of the sensor and the one given by the electronics. The bandwidth of a first order transfer function is simply given by $f_{BW} = \frac{1}{2\pi\tau}$ (eq. (2.5)), and we want the system to have a bandwidth equal to eq. (3.4). If we now consider a low input resistance of $R_{in} = 50 \, \Omega$, (this is a typical value with discrete components, especially if impedance matching is required and high frequency signals are involved), the total input capacitance $C_{in}$ would have to be on the order of $C_{in} \approx 1 \, pF$. This gives a first hint about the characteristics the input stage should have. Starting from this initial estimate, in order to obtain the best timing resolution of the system, it is now necessary to choose an appropriate circuit topology that can guarantee the best performance.

4 Circuit description

This section describes the type of transistors chosen to realize the front-end amplifier and the circuit topology used. First, some of the basic characteristics of the chosen configuration will be examined, looking at the small signal model of the circuit, and finally the results of Spice-based simulations of the full circuit will be outlined.

4.1 Use of RF bipolar transistors in fast sensor read-out

In the previous section we have seen the typical characteristics of signals from a 3D-trench TimeSPOT sensor. They present an average duration of 200 ps, which corresponds to a wide bandwidth in the frequency domain. In order to fully exploit the speed of this signal, a sufficiently fast active component is required. The speed of a transistor is normally characterized by its transition frequency $f_T$, i.e. the frequency at which the current gain is unity. In recent years, discrete component transistors capable of providing the best performance in terms of low noise and high transition frequency $f_T$ have been Silicon-Germanium hetero-junction bipolar transistors (HBT Si-Ge) [16]. These devices are able to provide transition frequencies on the order of 100 GHz as well as very small values of internal capacitance, which is necessary to sustain the wide bandwidth of our sensor signals. There are several examples of the use of such devices in designing front-ends for timing applications, with planar sensors without internal gain [17], and LGADs (Low Gain Avalanche Detectors) [18, 19]. In the case of LGAD readout, an excellent example is provided by the board developed at the University of California Santa Cruz [20] which made it possible to obtain a timing resolution of about 30 ps [21]. A modified version of this board, designed in the INFN laboratories at Genoa, was used for the first characterization tests on 3D TimeSPOT sensors, measuring a time resolution of about 20 ps [11]. In the same tests it was also clearly demonstrated [11] that the results on timing measurements were limited by the performance of the front-end electronics.

In the following sections, we demonstrate that it is possible to go further and obtain even better timing resolution from 3D TimeSPOT by using HBT Si-Ge transistors and further optimization of the read-out electronics.

4.2 Feedback Trans-Impedance Amplifier circuit

From the circuit point of view, the sensor is usually modeled as an ideal current generator in parallel with the capacitance $C_D$ of the detector. This generator is connected to a TIA (Trans-Impedance Amplifier) that converts the input current into an output voltage signal. The most common TIA
configuration is the “voltage-current” (or “shunt-shunt”) feedback topology, where a negative feedback network senses the voltage at the output and returns a proportional current to the input. This type of feedback is chosen because it lowers both the input and output resistance. A low input resistance leads the front-end to behave like a good current meter, while a low output resistance allows a better drive capability. A simple implementation of this solution is given by the so-called self-biased circuit (figure 4, left) [22]. This topology can be analyzed in detail [23] using the corresponding small signal model (figure 4, right) and finding the following second order transfer function,

$$R_m(s) = \frac{R_{m_0}}{(1 + s\tau)^2}. \tag{4.1}$$

When a current like the one shown in figure 3 is processed by such electronics, the output signal $V_{out}$ has the following characteristics,

$$T_{peak} = \frac{e^{t_c}}{e^{\frac{t_c}{\tau}} - 1}, \tag{4.2}$$

and,

$$V_{peak} = I_0 R_{m_0} e^{-\frac{T_{peak}}{\tau}} (e^{\frac{t_c}{\tau}} - 1). \tag{4.3}$$

In our case, $I_0 = \frac{Q_{ave}}{I_c} \sim 10 \mu A$, while $R_{m_0}$ is the DC trans-impedance introduced in section 2, which depends on the resistances of the circuit and on the trans-conductance $g_m$ of the transistor,

$$R_{m_0} = \frac{r_\pi g_m R_C R_f - r_\pi R_C}{R_f + R_C + r_\pi (1 + g_m R_C)}. \tag{4.4}$$

Thanks to the wide bandwidth of the Si-Ge in use, and the high value of the trans-conductance $g_m$, we see the dominant contribution to the noise is given by the fluctuation of the bias current $I_b$ at the base of the transistor, which can be written [23],

$$\sigma_{V,b} \sim \sqrt{\frac{k_B T R_{m_0}}{4r_\pi \sqrt{T}}}, \tag{4.5}$$

where $r_\pi = \frac{V_f}{I_b}$ is the dynamic input resistance of the bipolar transistor, $V_T = \frac{k_B T}{e}$ is the thermal voltage and $k_B$ is the Boltzmann constant.
The maximum slope of the signal, when the time constant $\tau$ is smaller than the duration of the current pulse $t_c$, is equal to

$$V_{\text{out}}' = \frac{I_0 R_{m_0}}{\tau e}. \tag{4.6}$$

The electronic jitter $\sigma_{e_j}$ (eq. (2.2)) can therefore be written,

$$\sigma_{e_j,b} = \sqrt{\frac{k_B T}{4\pi I_0}} \sqrt{\tau}. \tag{4.7}$$

The electronic jitter $\sigma_{e_j}$ increases with the square root of the time constant $\tau$, while the maximum possible value for $V_{\text{peak}}$ is given by $V_{\text{peak}} = I_0 R_{m_0}$ and is reached ideally for $\tau = 0$. We can now choose a time constant for our system (sensor+electronics) that allows the best signal to noise ratio (SNR), which shows a maximum when,

$$SNR_{\text{max}} = \left( \frac{V_{\text{peak}}}{\sigma_{v,b}} \right)_{\text{max}} \rightarrow \tau \sim 0.335 \ t_c \approx 70 \ ps. \tag{4.8}$$

Since eq. (4.1) is the transfer function of a second order system, eq. (2.5) gives the $-3$ dB frequency as,

$$f_{-3dB} \sim \frac{0.54}{2\pi \tau} = \frac{0.54}{2\pi \ 0.335 \ t_c} \approx 0.26 \ \frac{1}{t_c}, \tag{4.9}$$

and using an average value for the charge collection time of $t_c = 200$ ps,

$$f_{-3dB} \approx 1.3 \ GHz. \tag{4.10}$$

Using this simplified model we find that the bandwidth optimising the SNR is smaller than the bandwidth of the signal, as defined in eq. (3.4). On the other hand, we are still neglecting the contribution of the other noise sources such as the resistances $R_f, R_C$ and the fluctuations of the bias current $I_C$. Taking these effects into account, the best time constant will have a slightly higher value than given by eq. (4.8). We must also consider that the current duration is not constant, as shown by the CCT distribution (figure 2). In the case of signals that are longer than the average time $t_c$, too short a time constant $\tau$ leads to integration of a smaller proportion of the total charge and, according to eq. (4.3), leads to an output signal of lower amplitude. To understand the performance achievable by this configuration we need to consider realistic values for the trans-conductance $g_m$, the resistances of the circuit and the supply voltage $V_{CC}$ and find the best value for the trans-impedance $R_{m_0}$ that leads to the best time constant $\tau$.

### 4.2.1 Theoretical performance estimate

To fully exploit the speed of our 3D sensors we need a transistor with a high transition frequency $f_T$. HBT Si-Ge RF transistors can typically sustain bias currents $I_C$ of the order of a few tens of mA, which corresponds to values of trans-conductance $g_m$ close to unity. The values of the internal capacitance $C_{be}$ (base-emitter) and $C_{ce}$ (collector-emitter) are smaller than 1 pF, while the capacitance $C_{cb}$ (collector-base) working in feedback in our common emitter configuration is smaller than 100 fF. It can be shown [23] that the time constant of the chosen circuit can be written as,

$$\tau = \sqrt{\frac{R_f R_C r_{\pi} \xi}{r_{\pi} (1 + g_m R_C) + R_C + R_f}} \approx \sqrt{\frac{R_{m_0} \xi}{g_m}}, \tag{4.11}$$
with the quantity $\xi$ given by,

$$\xi = (C_L C_{in} + C_L C_f + C_{in} C_f),$$

and contains all the capacitance involved in the circuit,

$$C_{in} = C_D + C_{be} \quad C_f = C_{cb} \quad C_L = C_{ce}.$$ (4.13)

We are still not considering any parasitic capacitance nor load capacitance of the following stage. Having a fixed value for the capacitance means the problem to define the time constant $\tau$ is now related to the value of the power $V_{CC}$ and the resistances $R_f$ and $R_C$. The correct choice has to be made, taking into account the stability of the circuit that can be established considering the circuit damping factor $\zeta$, which is a function of its resistances, capacitance and transistor trans-conductance (see [23] for a wide explanation). An under-damped system can lead to an unwanted oscillating behavior, while an over-dumped system might not exploit the full potential of the active component.

A numerical example, with realistic values for all components and considering the performance of the best-in-class ultra low noise HBT transistors [16], can be found in [23]. This shows that with a single stage and an input charge $Q_{MPV} \approx 2 fC$, the output voltage can be of the order of

$$V_{peak} \approx 10 \text{ mV},$$ (4.14)

while the time constant is about,

$$\tau \approx 180 \text{ ps}.$$ (4.15)

This time constant corresponds to a trans-impedance $R_m(s)$ bandwidth $f_{-3\text{dB}} \approx 480 \text{ MHz}$. The $V_{peak}$ value found, to be compared with a typical noise of a few hundreds of $\mu$V, also shows that it is opportune to add a second amplification stage in order to increase the amplitude of the signal. The choice in this case is to use the same self-biased trans-impedance configuration with the same ultra low noise Si-Ge transistor, optimizing the operating point and the size of the components in such a way to reach the best performance in terms of SNR and electronic jitter. A second stage further reduces the bandwidth, which can be exploited to optimize the overall time constant to limit ballistic deficit. With the data-sheet values of the components and the working point established in [23], we find that the estimated electronic jitter can still be of the order of

$$\sigma_{ej} \approx 7 \text{ ps}.$$ (4.16)

The value of the jitter $\sigma_{ej}$ in eq. (4.16) depends on the capacitance of the pixel $C_D$, which in the example was chosen to be $C_D \approx 1 \text{ pF}$. Also the transistor input capacitance, which is enhanced by the Miller effect, has a typical value of the same order. For values of $C_D < 1 \text{ pF}$, we expect to observe a higher SNR and a lower jitter performance, while for values of $C_D$ significantly higher than 1 pF, both the SNR and the $\sigma_{ej}$ are expected to be worse.

4.3 Spice simulations

Together with the analytic model shown in the previous section, Spice-based simulations are very useful to evaluate circuit performance. Component manufacturers usually provide Spice models that are suitable to perform transient, frequency, and noise analysis simulations. Figure 6 shows an example of transient simulation of the two-stage circuit based on the self-biased topology (figure 5).
Figure 5. Simplified schematic of the two stages circuit used for the electronics front-ends developed.

Figure 6. Transient simulation of the two stages circuit for a rectangular input current as the one shown in figure 3 and corresponding output signal (blue waveform). The output signal has been reversed for better viewing.

These simulations can help to evaluate the operating point of the active components and the stability of the system. In particular, parametric simulations are very useful, where the effect of varying the value of a particular component or of the power supply can be investigated. Through AC simulations, it is possible to control the bandwidth of the front-end, while through noise analysis, it is possible to evaluate the Noise Amplitude Spectrum Density (NASD) produced by all noise sources (figure 7 green line), such as Johnson-Nyquist noise, shot noise etc. The integral of the NASD gives the
RMS value of the noise at the node of interest. Considering the simulation illustrated in figure 6, the output voltage shows $V_{\text{peak}} \sim 160 \text{ mV}$, while with the noise analysis we find $\sigma_v \sim 6.1 \text{ mV}$. The bandwidth is $f_{-3\text{dB}} \sim 780 \text{ MHz}$ and the mid-band trans-impedance is $R_m \sim 35 \text{ k}\Omega$. The obtainable electronic jitter $\sigma_{ej}$ is estimated using eq. (2.2), where the slope at the chosen threshold is calculated on the signal obtained with the transient simulation, while the output noise, is taken from the result of the noise analysis. The estimated electronic jitter $\sigma_{ej}$ at the output was found to be 7 ps. On the other hand, this simulation doesn’t take into account any parasitics or losses. The complexity of the simulation can be increased, modeling the effect of parasitic capacitance and transmission lines, so as to gain indications on the PCB design and signal integrity, which is of particular importance at high frequencies. An accurate evaluation of these effects is decisive for the success of the design implementation, and the results must be correctly interpreted so as to not overestimate the performance of the system.

![Figure 7. Results of simulations in the frequency domain of the two stage board and noise analysis. The measured bandwidth is $f_{-3\text{dB}} \sim 780 \text{ MHz}$ while the integrated voltage noise of the NASD at the output is $\sigma_v \sim 6.1 \text{ mV}$.](image)

5 Electronics boards

This section shows the timing front-end electronics fabricated for the TimeSPOT 3D sensors. Several single channel versions have been designed, from the first prototypes to later versions, optimized to reduce high frequency losses and improve stability. In addition, a four-channel version has been produced, which allows characterization of neighboring sensors of the same test structure for charge sharing studies.

5.1 Single channel boards

The first single channel board, **TFE v1.0**, is shown in figure 8. It consists of a double TIA stage like the one described in the previous section, based on the Si-Ge ultra low noise transistors produced by Infineon [16]. The board is equipped with a $4.0 \times 4.0 \text{ mm}^2$ pad for sensor housing. The usable pad
surface for gluing the sensor is $3.0 \times 1.5 \text{ mm}^2$ due to the footprint of the bypass capacitors. The board allows the supply of the High Voltage bias of the sensor, which can be bonded to the input of the electronics channel by means of a $0.8 \times 0.5 \text{ mm}^2$ pad. The PCB has a four layer stack-up and impedance-controlled tracks with $Z = 50 \Omega$. The passive components of the front-end have packaging 0402 ($1.0 \times 0.5 \text{ mm}^2$) and the surface finish is ENIG (Electro-less Nickel Immersion Gold), which facilitates wire bonding.

Two later versions of the board were then developed. The second version TFE v1.1 (figure 9), has the same layout for the front-end but a different size of the PCB which has been equipped with holes to facilitate mounting in measurement setups. The holes have been positioned such that the test structure (which normally has multiple sensors) is in the center of the symmetry axes (figure 9B). This allows rotation of the board by $90^\circ$ without the need for re-alignment, and gives more freedom in the creation of a measurement setup.

The sensor housing pad has a hole with a size of $500 \mu\text{m}$, which can be enlarged from the bottom if necessary. This reduces the material with which a particle interacts. In addition, an RF shield
has been added (figure 10A). The third version \textbf{TFE v1.1 GC} has the same footprint as the \textbf{TFE v1.1} but the front-end has been carefully redesigned with the aim of preserving the high frequencies of the signal and limiting losses due to impedance mismatch (figure 10B). Passive components with packaging 0201 (0.3 × 0.6 mm²) were used and the stack-up was modified to eliminate track width changes. A fourth version of the board \textbf{TFE v1.1 GC RF} was also produced using high frequencies substrates between the conductive layers of the PCB (i.e ROGERS RO4450 for the core and ROGERS RO4350 for the pre-preg) in order to have tight control on dielectric constants and maintain low losses at high frequency.

5.1.1 Boards performance

Characterization of the boards was done using a setup equipped with an oscilloscope with 8 GHz analogue bandwidth and 20 GSa/s sampling, and a 200 fs pulsed, 1030 nm wavelength laser with a minimum spot size on its target of 5 μm [24] (figure 11). The amplitude, rise-time, noise and SNR values were measured directly using the measurement functions of the oscilloscope used. For time resolution measurements, a second board was used for time reference. This board houses another 3D sensor onto which a reflection of the laser is directed. Since the equivalent deposit on this time reference is about 10 MIPs, the electronic jitter is strongly reduced and a jitter of 907 fs is obtained. The electronic jitter $\sigma_{ej}$ of the DUT is therefore calculated as the standard deviation of the measurement of the delay between the signal from the DUT and the one of the time reference. As described in section 2, the action of the system on the currents produced by the sensor can be represented by a transfer function $R_m(s)$. However, this function includes internal characteristics of both the electronics and the sensor, which means that different sensors connected to the same electronics correspond to different transfer functions $R_m(s)$. The type of connection (e.g. wirebonding), the presence of parasitic capacitance and the length of the transmission line can also influence the trans-impedance $R_m(s)$. An accurate trans-impedance measurement therefore requires the sensor to be connected to the electronics. For this reason the trans-impedance in the frequency domain (figure 13) was calculated by following a semi-empirical method [12]. This method consists in pulsing the sensor with the laser and measuring the average output signal (figure 12). By means of a simulation with the TCode package [15], the current corresponding to the deposition of the
laser in the chosen position is obtained. Finally the trans-impedance of the system is obtained by means of a deconvolution made with the software TFBoost [25].

The measured values for the main quantities of the different boards are summarized in table 1, which shows the values of integrated noise $\sigma_v$, the SNR, the rise time $t_r$ from 20% to 80% of the $V_{\text{peak}}$, and the jitter $\sigma_{ej}$ corresponding to the MPV of charge deposit of a MIP in the sensor ($Q_{\text{MPV}} = 2$ fC). The precision on the values shown in the tables is of the order of 1%. The amplitude for each board corresponding to a MIP deposit was calibrated considering the results obtained from measurements made during several test-beams [26, 27] and represents a typical value with a voltage bias of 100 V.
Table 1. Main values of the boards measured using the setup described in [24]. * Values with a strip of ten single pixel. ** Values with a single pixel. The precision on the values shown is of the order of 1%.

| Board          | TFE v1.1 * | TFE v1.1 GC * | TFE v1.1 GC_RF ** |
|----------------|------------|---------------|-------------------|
| $\sigma_v$ [mV] | 2.5        | 3.5           | 3.3               |
| $V_{peak}$ [mV]| 50         | 70            | 80                |
| SNR            | 20         | 20            | 23                |
| $t_r$ [ps]     | 105        | 95            | 80                |
| $\sigma_{ej}$ [ps] | 7       | 6             | 6                 |
| Power Consumption [mW] | 70       | 70            | 70                |

The boards versions TFE v1.1 and TFE v1.1GC showed major differences. In particular, the layout optimization and the use of passive components of smaller packaging allowed a considerable increase of the front-end bandwidth. A trans-impedance of $27 \, k\Omega$ was obtained with a power bandwidth higher than 500 MHz when connected to a strip sensor of ten pixel (figure 13A). The increase in bandwidth is also visible from the values reported in table 2. This allows a larger signal amplitude, while maintaining the same SNR.

Table 2. Frequency characteristic of the pulse response of the boards obtained with the semi-empirical method and with a strip detector of 10 pixel ($C_P \sim 1 \, pF$)

| Board          | TFE v1.1 | TFE v1.1 GC | TFE v1.1 GC_RF |
|----------------|----------|------------|---------------|
| Power Bandwidth| 326 MHz  | 526 MHz    | 515 MHz       |
| Bandwidth      | 745 MHz  | 1.02 GHz   | 980 MHz       |
| Mid-band $R_{m_0}$ | 26 k\Omega | 27 k\Omega | 26 k\Omega |

The version of the board made with ROGERS laminate has shown excellent performance in terms of bandwidth, especially with lower capacity sensors such as the single pixel. It is also slightly more sensitive to external noise sources and requires more accurate shielding. Figure 13 B shows a comparison of the board TFE v1.1 GC with the one used at the PSI test beam in 2019 [11], where the measured electronic jitter was $\sigma_{ej} \sim 15 \, ps$. The improvement with the TFE v1.1 GC board in terms of bandwidth and response uniformity over the whole spectrum is remarkable. In addition to this, it exhibits greater stability which has been tested with several sensors with different capacitance values, and always provides excellent performance.

5.2 Multi-channel board

The four-channel version of the board TFE4CH v1.0 is shown in figure 14. It was designed to characterize the timing performance of TimeSPOT sensors, taking into account the charge sharing between adjacent pixels. The test structure that is positioned in the central pad must now be connected to different electronics channels that need to be properly decoupled to minimize cross-talk. Therefore, particular care has been taken in designing the ground layer in order to allow the current from the sensor to have the correct return path towards the relevant electronics channel.
Figure 13. A) Trans-impedance in the frequency domain of the three single channel boards produced with $C_D \approx 1\, \text{pF}$. B) Comparison of the trans-impedance in the frequency domain of (TFE v1.1 GC) with the board used in the test beam at PSI in [11].

Figure 14. A) The TFE4CH v1.0 board with the test structure glued to the center of the pad. The wire-bonding to the individual electronics channels are visible. B) The RF shields designed for the individual front-ends.

The power layer has also been optimized, with two separate power supplies used for the upper and lower channels of the board. The optional use of individual RF shields for the electronics channels has also been provided (figure 14B). The size of the PCB is similar to that of the single channel board and the same principle of symmetrical holes has been used with respect to the sensor pad which makes it particularly easy to use in a measurement set-up. The board showed excellent decoupling between channels with negligible cross-talk. This can be seen from figure 15 A) and B), which show the signals acquired on two adjacent channels of the multi channel connected to two single pixels of the same test structure. By injecting a high amplitude noise into one of the channels (simply touching the input of the transistor with a metal object), we have no effect in the channel pulsed with the laser. The bandwidth of the multichannel has not yet been calculated with
the semi-empirical method described in section 5, but oscilloscope measurements (figure 15) show that the risetime and signal shape agree with what is obtained with the single channel version.

6 Applications

The boards described were designed and assembled between 2019 and 2020. In the past years they have been used extensively to carry out many types of measurements. This section summarizes some of the applications of the produced boards. The first application was the use of the board in a setup for a complete in-laboratory characterization of 3D trench-type silicon pixel sensors. The setup is described in detail in [24, 28, 29] and one of the key features is to provide a time reference for time resolution measurements with the impressive resolution of $\sigma_t = 907$ fs. This result was possible thanks to higher charge deposit (about 10 MIPs) and the property of 3D sensors to behave as ideal sensors with $\sigma_{\text{sens}} \approx 0$ when stimulated in the same position, leaving only $\sigma_e$ as contribution to the time resolution.

Another application was to measure the time resolution of the 3D TimeSPOT sensor using a $^{90}\text{Sr}$ radioactive source set-up [30] (figure 16). Recent results [26, 27], obtained with an intensive measurement campaign with non-irradiated and irradiated 3D sensors at the SPS test-beam facility, have shown a temporal resolution of the detector + electronics system of about 11 ps, which is about half of the value obtained in 2019 in the first test-beam at PSI [11]. The highly optimized electronics contributed significantly to this result, making the 3D TimeSPOT sensor the best temporally performing solid-state detector (in terms of timing resolution) without a gain mechanism currently. The TFE boards are still in heavy use in the characterization campaigns of TimeSPOT sensors and further results will be surely published in the near future.

7 Conclusions

In order to characterize the timing performance of 3D-trench sensors produced within the TimeSPOT collaboration, various Si-Ge transistor-based boards have been designed, assembled and tested. The boards are single channel and multi-channel two-stage TIA, optimized in order to provide the
best performance, both with single 3D pixels and with several pixels (strips) read out together, corresponding to capacitance values up to some pF. The measured jitter of the read-out channel for a charge deposit of 2 fC is lower than 7 ps.

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References

[1] LHCb collaboration, Framework TDR for the LHCb Upgrade II — Opportunities in flavour physics, and beyond, in the HL-LHC era, CERN-LHCC-2021-012, CERN, Geneva (2021).

[2] M. Ferrero et al., Evolution of the design of ultra fast silicon detector to cope with high irradiation fluences and fine segmentation, 2020 JINST 15 C04027.

[3] G. Iacobucci et al., Efficiency and time resolution of monolithic silicon pixel detectors in SiGe BiCMOS technology, 2022 JINST 17 P02019 [arXiv:2112.08999].

[4] A. Lai, 4D-tracking in the 10-ps range: A technological perspective, Front. in Phys. 10 (2022) 1019262.

[5] S.I. Parker, C.J. Kenney and J. Segal, 3-D: A New architecture for solid state radiation detectors, Nucl. Instrum. Meth. A 395 (1997) 328.

[6] S.I. Parker, A. Kok, C. Kenney, P. Jarron, J. Hasi, M. Despeisse et al., Increased speed: 3D silicon sensors. Fast current amplifiers, IEEE Trans. Nucl. Sci. 58 (2011) 404.

[7] A. Lai et al., First results of the TIMESPOT project on developments on fast sensors for future vertex detectors, Nucl. Instrum. Meth. A 981 (2020) 164491.
[8] L. Piccolo, S. Cadeddu, L. Frontini, A. Lai, V. Liberali, A. Rivetti et al., *First measurements on the Timespot1 ASIC: a fast-timing, high-rate pixel-matrix front-end*, 2022 JINST 17 C03022 [arXiv:2201.13138].

[9] W. Blum, W. Riegler and L. Rolandi, *Particle Detection with Drift Chambers*, Particle Acceleration and Detection, Springer Berlin Heidelberg (2008).

[10] A. Lai et al., *First results of the TIMESPOT project on developments on fast sensors for future vertex detectors*, Nucl. Instrum. Meth. A 981 (2020) 164491.

[11] L. Anderlini et al., *Intrinsic time resolution of 3D-trench silicon pixels for charged particle detection*, 2020 JINST 15 P09029 [arXiv:2004.10881].

[12] D. Brundu et al., *Accurate modelling of 3D-trench silicon sensor with enhanced timing performance and comparison with test beam measurements*, 2021 JINST 16 P09028 [arXiv:2106.08191].

[13] M. Boscardin, S. Ferrari, F. Ficorella, A. Lai, R. Mendicino, M. Meschini et al., *Advances in 3D Sensor Technology by Using Stepper Lithography*, Front. Phys. 8 (2021) 647.

[14] G.T. Forcolin, R. Mendicino, M. Boscardin, A. Lai, A. Loi, S. Ronchin et al., *Development of 3D trenched-electrode pixel sensors with improved timing performance*, 2019 JINST 14 C07011.

[15] A. Loi, A. Contu and A. Lai, *Timing Optimisation and Analysis in the Design of 3D silicon sensors: the TCoDe Simulator*, 2021 JINST 16 P02011 [arXiv:2008.10730].

[16] Infineon Technologies, *Ultra low-noise Si-Ge:C transistors for use up to 12 GHz*, 2022.

[17] M. Benoit, R. Cardarelli, S. Débieux, Y. Favre, G. Iacobucci, M. Nessi et al., *100ps time resolution with thin silicon pixel detectors and a SiGe HBT amplifier*, 2016 JINST 11 P03011 [arXiv:1511.04231].

[18] R. Arcidiacono et al., *Test of Ultra Fast Silicon Detectors for the TOTEM upgrade project*, 2017 JINST 12 P03024 [arXiv:1702.05180].

[19] E. Bossini and N. Minafra, *Diamond Detectors for Timing Measurements in High Energy Physics*, Front. in Phys. 8 (2020) 248.

[20] UCSC board Twiki page, https://twiki.cern.ch/twiki/bin/view/Main/UcscSingleChannel, 2020.

[21] N. Cartiglia et al., *Beam test results of a 16 ps timing system based on ultra-fast silicon detectors*, Nucl. Instrum. Meth. A 850 (2017) 83 [arXiv:1608.08681].

[22] B. Razavi, *Design of Integrated Circuits for Optical communications*, John Wiley & Sons (2012).

[23] A. Lai and G.M. Cossu, *High-resolution timing electronics for fast pixel sensors*, arXiv:2008.09867.

[24] M. Aresti, A. Cardini, A. Lai, A. Loi, G.M. Cossu, M. Garau et al., *Laboratory Characterization of Innovative 3D Trench-design Silicon Pixel Sensors Using a Sub-Picosecond Precision Laser-Based Testing Equipment*, in Proceedings of IEEE Nuclear Science Symposium and Medical Imaging Conference , Boston, MA, U.S.A., 31 October–7 November 2020, pp. 1–6.

[25] D. Brundu, A. Contu, G.M. Cossu and A. Loi, *Modeling of solid state detectors using advanced multi-threading: The TCoDe and TFBoost simulation packages*, Front. Phys. 10 (2022) 804752.

[26] A. Cardini, *10 ps timing with 3D trench silicon pixel sensors*, talk given at 15th Pisa Meeting on Advanced Detectors, La Biodola, Isola d’Elba, Italy, 22–28 May 2022.

[27] A. Lampis et al., *10 ps timing with highly irradiated 3D trench silicon pixel sensors*, talk given at the 23rd International Workshop on Radiation Imaging Detectors, Riva del Garda, Italy, 26–30 June 2022 [arXiv:2209.14632].
[28] M. Aresti, A. Cardini, G.M. Cossu, M. Garau, A. Lai, A. Lampis et al., *A Sub-Picosecond Precision Laser-Based Test Station for The Measurement of Silicon Detector Timing Performances*, in *Proceedings of IEEE Nuclear Science Symposium and Medical Imaging Conference*, Boston, MA, U.S.A., 31 October–7 November 2020, pp. 1–4.

[29] A. Lampis, *Sub-pixel characterization of innovative 3D trench-design silicon pixel sensors using ultra-fast laser-based testing equipment*, talk given at 16th “Trento” Workshop on Advanced Silicon Radiation Detectors, FBK, Trento, Italy, 16–18 February 2021.

[30] M. Garau, *Laboratory characterization of 3D-trench silicon pixel sensors with a 90Sr radioactive source*, talk given at 16th “Trento” Workshop on Advanced Silicon Radiation Detectors, FBK, Trento, Italy, 16–18 February 2021.