Design of Memory Test System for Measuring Transmission Lines Galloping

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Abstract. A machine in order to warn of transmission lines galloping, reduce the loss caused by transmission lines galloping. Aiming at a transmission system, a set of lines galloping storage and testing device is developed. The device takes STM32 as the control core to realize signal conditioning, data storage, serial communication and other functions. In the design of the software, the method of single external trigger and multiple internal trigger is adopted to effectively avoid the false trigger phenomenon in weak oscillation, so as to test and store the acceleration of the wire when it gallops violently. The acceleration sensor and the storage test device directly install on electric wire, and it can detect and record the acceleration data in the process of wire galloping. After the test, the recovery device uses the upper computer to read the detected data and display the waveform, which can provide important experimental basis for the theoretical analysis and parameter setting of the lines galloping.

1. Preference

Project Supported by Science and Technology Project of State Grid Liaoning Electric power Supply Co., Ltd. (2018-YF32). In recent years, with the social economy develop fast, the growing demand for electricity, power grid scale expands unceasingly in our country. There is a problem to be solved: in recent years, our country affected by extreme weather, transmission lines covered by ice and snow, lines galloping accident is more and more frequent, and the trend of increase year by year, seriously affected the safety and stable operation of power grid. Especially along with our country in recent years, a number of such as newly built the three gorges project, 1000kV uhV ac, uhv dc + 800kV power transmission project. These lines are general in terrain complex by region, climate changeable, under the certain condition of climate, galloping accidents extremely easily, conductor wave, large amplitude makes wire tension increased significantly, could damage to tower, even make the tower down. Therefore, reliable device is needed to measure the acceleration of power line galloping, which can provide important experimental basis for theoretical analysis and parameter setting of power line galloping later. The research on the occurrence mechanism, propagation model and online monitoring of wire galloping is of great significance for strengthening the bearing capacity of tower and pole structure and ensuring the safe operation of power grid in galloping areas.
Storage test technology can solve the above problems. In order to solve the above problems and study wire galloping better, a set of wire galloping storage and test system is designed. This device has the advantages of high reliability, small size, long acquisition time, accurate and repeated acquisition and so on. Based on the storage test technology, the method of using one external trigger and multiple internal triggers is added, which effectively solves the phenomenon of false triggering and accurately captures the acceleration of the wire when it is galloping. In other words, the device can collect data in the state of wire galloping, while the wire is not in the state of non-galloping. The storage test system can detect whether the wire is in the process of galloping, collect and store the acceleration data, and the power failure data is not lost.

2. Overall scheme design
The system acceleration sensor has a range of ±500g. The storage test device is designed for the sensor and installed on the power line. The test system consists of a storage test device (lower computer) and a data analysis computer (upper computer LABVIEW terminal). Among them, the storage and test circuit is mainly composed of sensor signal conditioning module, A/D conversion module, data storage module, power supply module, data communication module and STM32 main control module. After the data collection is completed, it is transmitted back to the upper computer through the serial port, and the acceleration waveform is displayed on the LABVIEW terminal.

2.1. System hardware design

2.1.1. Acceleration sensor type selection and signal conditioning circuit design
Piezoelectric acceleration sensor adopts piezoelectric effect material as pressure sensor, which has the characteristics of wide frequency response range, high sensitivity, good dynamic characteristics, strong anti-interference ability, etc. and can meet the requirements of wire dancing detection. The acceleration sensor of this system is CA-YD-180 piezoelectric sensor of Jiangsu Lianneng electronic technology company, which belongs to two-wire IEPE acceleration sensor. Its main technical indicators are shown in table 1.

| Serial number | Technical parameters     | Index      |
|---------------|--------------------------|------------|
| 1             | Reference sensitivity     | 10mv/g     |
| 2             | Frequency range           | 1~10000Hz  |
| 3             | Acceleration range        | ±500g      |
| 4             | Working current           | 2~10mA     |

The actual figure of acceleration sensor is shown in figure 1.

The CA-YD-180 sensor requires 2-10mA constant current source power supply. In this paper, a three-terminal adjustable integrated constant current source chip LM134 is used to construct a constant current source circuit. The acceleration sensor is powered by the way shown in figure 2. At this time, the constant current value generated by LM134 is 8.33mA.
Figure 2. LM134 supplies power to the acceleration sensor

After constant current source power supply, the sensor output is a dynamic signal with dc bias, and RC high-pass filter circuit is adopted to achieve the isolation and direct coupling, the specific circuit is shown in figure 3. The latter stage builds a voltage follower based on operational amplifier LF353, which plays the role of impedance matching. By setting the value of resistance and capacitance, the lower limit cut-off frequency of high-pass filter circuit is determined to be 0.2Hz:

$$f_p = \frac{1}{2\pi (R_{104} + R_{102})C_{101}}$$  \hspace{1cm} (1)

Figure 3. High pass filter circuit

In order to avoid aliasing distortion in the test site, a low-pass filter is set at the back stage of RC high-pass filter circuit, which can effectively eliminate high-frequency interference.

Based on operational amplifier LF353, this paper designs a classical two-order active butterworth low-pass filter, as shown in figure 4. The cut-off frequency of 12kHz is determined by setting the value of resistance and capacitance:
\[ f_c = \frac{1}{2\pi \sqrt{R_{107} R_{108} C_{1.4} C_{1.8}}} \] (2)

2.1.2. Data acquisition and storage circuit design
STM32 is selected as MCU, whose built-in ADC range is 0~3.3v. Since the range of the sensor is -500g~500g, the reference sensitivity of the sensor is about 10mV/g. Therefore, the range of output voltage of the sensor is -5V~5V, which is obviously inconsistent with the range of ADC. Therefore, the corresponding step-down and dc bias circuit needs to be designed to adjust the output signal of the sensor into the range of ADC. Voltage-reduced circuit is shown in figure 3, section 3.1. which reduces the sensor signal into +1.6 V~1.6 V (marked signal_104) in the way of these resistances in series. The DC bias circuit is shown in figure 5 below. According to the analysis of the superposition theorem of the circuit: (1) if the input signal of the operational amplifier is grounded, then the circuit output 1.6V dc voltage is connected to the ADC acquisition port; (2)+5V input grounding, the circuit is converted to a voltage follower and a RC high-pass filter circuit in series, and the circuit output is an alternating signal signal_104; (3) if the above two signals are superimposed, the signal signal_104 can be raised by 1.6V. In this way, the sensor signal is adjusted to the range of 0V~+3.2v, within the range of ADC.

![Figure 5. DC bias circuit](image)

Since the frequency of acceleration signal generally does not exceed 10KHz, the sampling rate of ADC and the storage rate of memory chip are not too high. Winbond serial NOR Flash chip W25Q64 (8M bytes) was selected as the memory chip. Its page (256 bytes) write time is approximately, so the Flash chip's storage rate is about 10 times higher than the acceleration signal frequency, enough to store acceleration data.

2.1.3. Power supply design
Battery selection is the core of power supply design, mainly considering the following four factors: (1) battery volume and weight; (2) the overload resistance of the battery; (3) battery voltage; (4) battery capacity.

Because the storage test device is installed on the power line, the battery is required to be small in size, light in weight and large in capacity. Secondly, the battery bears acceleration load in the process of moving with the wire, so the battery needs to have certain overload resistance. Polymer lithium battery has the advantages of strong impact resistance, light weight, small thickness, customizable shape and so on. This paper selects polymer lithium battery as the power supply battery of the system. The voltage of the battery needs to be combined with the power supply voltage required by each module of the system. In order to reduce the volume of the storage test device, lithium battery with a voltage of 12V was selected in this paper, and the voltages of +5V, +3.3V and -5V were obtained by stabilizing the voltage chip HT7350, HT7333 and reversing the chip ICL7660, respectively. Finally,
the digital circuit is powered by +3.3v, the constant current source circuit is powered by +12V, and the operational amplifier is powered by. The capacity of the lithium battery is 600mah, and the power consumption current of the circuit board is 60mA after the actual measurement and storage test. It can be calculated that the circuit can work continuously for 10 hours and meet the test time requirements.

2.1.4. Use and interface design
Use method: press 1 to power the system and the green light starts flashing. Press 2 to erase the external flash data. The system starts to pre-collect and wait for the trigger. At this point, the red light flashes once and then goes out. After triggering, acceleration data will be collected. When the system detects that the dancing process is terminated, the collection will be completed. Green light flashing, red light long light, signal collection success. Other status of indicator light indicates collection failure.

1 power switch 2 trigger button 3 charging port 4 serial port communication interface 5 signal indicator light (red) 6 signal indicator light (green) 7 acceleration sensor

Figure 6. Interface diagram of acceleration test system

Figure 7. Picture of real product acceleration test system

2.2. System software design
ADC data acquisition is the main part and key function of the test system software, and its program flow is shown in figure 8 below.

Figure 8. data collection process
After the test system is energized and initialized, wait for external trigger signal. If the external trigger signal arrives, the Flash memory chip is erased, which means that the data collected and stored in Flash last time is cleared. After that, the CPU continuously detects whether the acceleration signal reaches the internal trigger threshold. If not, the collected data will be recorded in the pre-sampling cache in a loop [7]. If the internal trigger threshold is reached, formal sampling is performed, stored in RAM and transferred to Flash in a "double-cached" fashion.

When a formal sampling is completed, the CPU determines whether the total number of internal triggering times has reached. If not, the CPU continues to judge the internal triggering threshold to determine whether the formal sampling is carried out. If the total number of internal triggers is reached, the sampling storage procedure ends. The main innovation of this part of software is one external trigger and multiple internal triggers. Multiple internal triggers can avoid the phenomenon that the installation of storage test device or other uncertain factors such as field interference can lead to false triggering and the acceleration during dancing cannot be recorded. Multiple internal triggers can ensure that the effective acceleration data can be recorded by the storage test device.

This system software uses “double cache” method to realize data storage. So-called double cache storage methods: is in the internal microprocessor, RAM opened two same size of the cache, collecting data to populate the cache first 1, full of later transferred to the external Flash, in the process of transferring data, collect data, but data fill in the cache 2, such as the cache after 2 full can then transfer the data to the external Flash, collect data, in turn, to fill the cache 1 again. Adjust the size of the cache so that data collection and stored procedures are not interrupted.

Since the frequency of acceleration signal generally does not exceed 10KHz, according to Nyquist sampling theorem, the sampling rate of 100KHZ can meet the requirements of data collection of this system. On the software, the conversion time of STM32 built-in ADC is configured as 1.17us (855KHz). The sampling rate is controlled to be 100KHz by STM32 internal timer, that is, the result of A/D conversion is stored in RAM cache in timer interrupt service program every 10us.

Specifically, we set up two cache BUF1 and BUF2 in STM32 memory RAM, each of which is 1000 bytes. When the sampling rate is controlled by a timer to be 100KHz, it takes 5ms to store 1000 bytes of data into the cache. It took 3.76ms to write 1000 bytes of cached data into Flash by actual measurement. Therefore, it can be known that "double caching" can be implemented with a cache (1000 bytes) as the unit of storage, and the time to write Flash is less than the time to save RAM.

3. Conclusion
In view of the swing test of a transmission line, a special small-volume and anti-overload storage and testing device is designed by using the storage and testing technology and combining the actual object under test with the environment. The test system adopts the method of one external trigger and multiple internal triggers in the software design, which effectively avoids the phenomenon of misfiring during the test and failing to remember the acceleration of wire dancing process. It can provide important experimental basis for theoretical analysis of transmission line movement, transmission line construction and transformation. However, this design requires that the test device can only be read after the end of the test, and there are some limitations in data acquisition efficiency. Then, research on wireless reading is required.

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