Herein, a method for the electrical characterization of a fully depleted silicon-on-insulator (FDSOI) high-k dielectric-metal-gate stack is proposed. The method is based on assessing low-field mobility in FDSOI field-effect transistor (FET) from current–voltage measurements at various temperatures in the gate voltage range up to strong inversion. In addition to assessing the value of the low-field mobility for the stack itself, it allows specifying the impact of various carrier-scattering mechanisms on the total stack mobility. Further, the application of double-gate operation in the optimal coupling mode for the FET allows analysis of the impact of the gate interfaces on mobility. The method can be used in the monitoring of stack quality and in the design and development of stack fabrication processes.

1. Introduction

Determination and control of device characteristics are an essential part of the development and fabrication of the semiconductor device industry. The permanent reduction in the size of modern electronic devices dramatically complicates characterization and control of their properties, not only technologically, but also conceptually. In the case of contemporary devices, such fundamental material feature as carrier mobility obviously requires reconsideration. Modern device dimensions approach the order of (or even become less than) carrier mean-free path, which determines mobility.[1] Simply speaking, a “defect-free” device inside a die can occur with nonzero probability.[2] On the one hand, the actual size of the device and not the material properties will determine mobility for such devices. On the other hand, development and control during the fabrication will gain much if mobility can be monitored on each die inside at the processed wafer. A possible way is to search for a proper device structure that can represent the material and stack properties correctly.

The mobility, a fundamental feature for a volumetric (3D) material, can be applied for the characterization of low-dimensional structures only conditionally.[3] For fully depleted (FD) silicon-on-insulator (SOI) high-k metal-gate (HKMG) field-effect transistors (FETs), the mainstream of the modern semiconductor technology (see refs. [4,5]), assessment of mobility requires careful consideration of the dimensionality factor, the influence of closely spaced interfaces, and intentional or unintentional stresses formed during fabrication.

Formally, for a FET, the material mobility (3D) must be amended using properties of the stack (2D) and corrected for the actual dimensions and stresses in the channel (1D). From the viewpoint of the device-fabrication process development, correction and improvement at each of the stages (3D, 2D, and 1D) are essential. While 3D mobility is well studied and documented, only a combination 2D + 1D is considered in most of the related publications (see, e.g., refs. [4,6-12] and references therein). Joint improvement of numerous, mutually influencing parameters for the 2D + 1D combination presents an extremely complicated task and requires a separate approach for each kind of device. Therefore, for proper development of the technology, it will be advantageous to determine a suitable device structure for characterization of “stack (2D) mobility” separately. Moreover, similar structures can be used for monitoring of mobility in further production quality control.

In the previous publication,[13] we presented a method for characterization of interface-trap density distribution \( D_{IT}(E_{IT}) \) at the front (FG) and back gates (BG) in SOI HKMG FETs using subthreshold swing (STS) measurements. Carrier mobility in a stack and interface trap density are closely interrelated[6] since Coulomb scattering from charged interface traps is one of the main mechanisms suppressing the mobility. In contrast, low mobility can strongly suppress the current related to the traps in STS mode. Due to this, we used possibly short channel devices for trap detection in ref. [13]. For FETs with the channel length in the range of free carrier path,[13] the temperature dependence of mobility is suppressed[12] and its value is mainly determined by the actual channel length and not by the free path of the carriers. This allowed the determination of \( D_{IT}(E_{IT}) \) in ref. [13].

In the present study, we attempted to use current–voltage characteristics of HKMG FD SOI FETs in the gate voltage range before strong inversion for the determination of mobility in the
stack. We show that proper choice of the device dimensions, modification of the measurements, and parameter extraction techniques allow characterization of carrier mobility, determination of the mechanisms affecting its value, and estimating the impact of interfaces.

2. Extraction of Carrier Mobility from Current–Voltage Dependencies

A methodology for extraction of various parameters for FD SOI metal-oxide-semiconductor field-effect transistor (MOSFET) from drain current characteristics was presented and refined in several publications (see, e.g., refs. [6,7,9–11]). It implies fitting the experimental current–voltage data for the FET with the relevant \(I_d(V_g)\) dependence, where \(I_d\) is the drain current and \(V_g\)–gate bias. Such parameters as low-field mobility \(\mu_0\) quality (or ideality) factor \(n\) (a ratio of experimental subthreshold slope to the theoretical at a given temperature), threshold voltage \(V_{th}\), and mobility attenuation coefficients \(\theta_1\) and \(\theta_2\) are extracted from the best fit. The expressions corresponding to the \(I_d(V_g)\) dependence are presented by Equation (1)–(3). These expressions, mainly based on refs. [7,8,10,11], were conformed and refined.

\[
I_D = \mu_T \mu_0 Q \frac{W_{CH}}{L_{CH}} \left[ 1 - \exp \left( -\frac{V_{DS}}{\mu_T} \right) \right]
\]  

(1a)

where \(\mu_T = q/\kappa_B T / \kappa_B\) is Boltzmann’s constant, \(T\) is temperature, and \(q\) is the elementary charge; \(W_{CH}, L_{CH}\) are the channel (gate) width and length and \(V_{DS}\) is the applied drain–source voltage. Equation (1a) is strictly valid in weak inversion and for lower \(V_g\) values. For the higher \(V_g\) range and for small enough \(V_{DS}\), an Ohmic version of Equation (1a) can be used (see ref. [10])

\[
I_D = \mu_n Q \frac{W_{CH}}{L_{CH}} V_{DS}
\]  

(1b)

The expression for the inversion charge \(Q\) is given in ref. [8] by

\[
Q_i(V_g) = n_{uT} C_{FOX} L W \left( \frac{V_g - V_{th}}{V_{th}} \right)
\]  

(2)

where \(C_{FOX}\) is the front oxide capacitance and “LW” stands for Lambert W function. This equation is valid for FD SOI with not thin back oxide (BOX), when \(C_{FOX} >> C_{BOX}\), and for \(V_{BG} = 0\). It is easy to show that Equation (2) is valid not only in the case of single (front) gate operation but also for the double-gate (DG) operation in the conditions of optimal coupling, namely for the case when \(d\phi_{BC}/dV_{FG} = d\phi_{BC}/dV_{BG}\), where \(\phi\) is potential at the FG and BG interfaces and \(V\) is applied bias.

Finally, the mobility in strong inversion is expressed as

\[
\mu_n = \frac{\mu_0}{1 + \theta_1 (Q_i/C_{FOX}) + \theta_2 (Q_i/C_{FOX})^2}
\]  

(3)

Front oxide capacitance, \(C_{FOX}\) can be assessed from the separate experiments based on the full-split capacitance–voltage (FSCV) measurement method. We previously applied this method in ref. [13] to obtain capacitance values for the layers in the stack.

For an illustration of the quality for the fitting using Equation (1)–(3), several experimental and fitted \(I_d(V_g)\) dependencies are presented in Figure 1. Note that the same data in the logarithmic and linear scale for \(I_d\) are shown for the measurements on each device. The fitting quality is very good for the six orders of \(I_d\) magnitude change. As it was suggested, the extraction routine is processed in two steps for optimization of the accuracy. During the first step fitting of nonlinear regression is performed with the \(\log(I_d)\) versus \(V_g\) data, in a relatively high \(V_g\) range up to strong inversion. This allows determining \(V_{th}\), with high accuracy, which can be confirmed by other methods for verifying threshold voltage (see below). During the second step, \(V_{th}\), value is preserved and \(\mu_0\) and \(n\) are extracted for a range of lower \(V_g\) values. We did not attempt extracting mobility attenuation coefficients in this study.

It is important to clarify that for the proper fitting of the \(I_d(V_g)\) dependence, the measured data should include the \(V_g\) values above the threshold voltage. The necessary value could be easily checked by one of the methods proposed earlier for \(V_{th}\) determination from the \(I_d(V_g)\) dependence (see ref. [17] and references therein). We applied the second-derivative method for a rough estimation of \(V_{th}\) values.

DG regime is essential and advantageous for FD SOI MOSFET operation. DG mode not only allows flexible control of the device but also can significantly improve the performance by boosting its mobility. Significant reduction of low-frequency noise was also reported recently for the FETs operating in DG regime. The main mechanism behind the effect is attributed to a shift of the current distribution maxima from the vicinity of the FG interface region to the center of the channel. Obviously, application of a static BG bias \(V_{BG} = \text{const.}\) allows optimization of current distribution for a specific value of the FG bias. For preserving the current distribution in the channel for any \(V_{FG}\), simultaneous changes of both biases should be used. Due to minimizing the influence of the interfaces, the optimal coupling conditions (see previous
section) will correspond to the maximum mobility in the channel for the bias range used. Defining the gate bias ratio for the optimal coupling, $K_{GC} = V_{BG}/V_{FG}$ can be done using the procedure\cite{12,22} applied during the $D_{TT}$ measurements. Since Equation (2) is valid for the optimal coupling and we are interested only in low-field mobility, we can apply similar procedures and Equations (1) and (2) for the $\mu_{Koc}$ extraction as will be used for $V_{BG} = 0$ V case.

Temperature dependence of mobility can provide valuable information about carrier scattering mechanisms in the stack\cite{3,12,22,23}. For estimating the impact of Coulomb, neutral defect-related, and phonon-scattering mechanisms on the mobility, measured temperature dependence is decomposed on three components according to Matthiessen’s rule and the empirical model first proposed in ref. [22]

$$\frac{1}{\mu_0(T)} = \frac{T}{300\mu_{Ph}} + \frac{300}{T\mu_C} + \frac{1}{\mu_N}$$ (4)

where $\mu_{Ph}$, $\mu_C$, and $\mu_N$ represent mobility components responsible for phonon, Coulomb, and neutral defect scattering, respectively.

3. Experimental Section

3.1. Samples

For correlation of the stack characteristics obtained during estimation of interface trap density\cite{13} with mobility data, we used similar samples in the present investigation. The devices under test (DUTs) were FDSOI MOSFETs provided by Globalfoundries and were produced using 22 nm node technology.\cite{5} They were fabricated on (100) SOI wafers with highly scaled BOX and silicon channel thickness. The gate stack consisted of a high-k gate dielectric on top of a SiON interfacial layer, with an equivalent oxide thickness (EOT) for front gate about 1 nm and TiN metal gate (labeled as SG devices below). As a variation, we also investigated devices with an additional thin SiO2 layer atop of the channel (with EOT ≈ 3 nm for the front gate, labeled EG devices). Similar, low-doped Si layers were used in n-channel nSG, nEG, and p-channel pEG devices. In the case of p-channel pSG devices, Si$_1-x$Ge$_x$ was used with $x = 5\%$. The BOX thickness in both cases was ~20 nm. The devices applied for the mobility measurements were standard FET structures with a rectangular channel and four separated contacts for FG, BG, source (S), and drain (D). The connection scheme can be viewed in ref. [13] (see Figure 1A there). The channel lengths of the FETs varied in the range of 18 nm $\leq L_{CH} \leq 1$ $\mu$m for $W_{CH} = 1$ $\mu$m and channel width varied in the range of 150 nm $\leq W_{CH} \leq 10$ $\mu$m for $L_{CH} = 160$ $\mu$m. For the $C_{FOX}$ values, the data obtained similarly as in ref. [13] were used. For comparison of the influence of various fabrication processes on mobility and for comparison to the $D_{TT}$ measurement results, we also studied three wafers with the same stacks. One of the wafers labeled process of record (POR) was produced under reference conditions, the other two labeled R and O were subjected to small intentional variations of the fabrication process.

3.2. Setup and Measurements

The sample holder with a sample attached was placed inside the PS-100 model probe-station (Lake Shore) allowing measurement at cryogenic temperatures under vacuum conditions. We used a range of temperatures from 120 to 400 K in our measurements. Cooling of the sample stage was done by cryogenic $N_2$ flow. Control and regulation of temperature of the sample stage and the thermal shield, surrounding the sample stage, was performed using the “Lake Shore model 336” temperature controller with ±0.5 K accuracy. High stability of the temperature is crucial for the measurements in STS mode not only because of high influence of the temperature on the values measured, but also due to possible impact of heater current pulses (an electrical impact) on the detected pA level currents. Therefore, measurements were carried out only after complete stabilization of the temperature (30–40 min after reaching the set temperature), under stable flow of coolant and corresponding stable regime of heater.

Electrical contact to the pins of a DUT was accomplished using four micromanipulated stages equipped with probe arms and 25 $\mu$m “continuously variable temperature probes” with tungsten tips. Electric circuitry was assembled using triaxial cables. A microscope (7:1 zoom), equipped with a CCD camera, light source, and monitor, was used for observation of the sample during contacting. During measurements, the sample was protected from outside illumination.

Electrical measurements were performed using B1500A semiconductor Device Analyzer (Agilent) equipped with four 100 mA/100 V, 10 fA/0.5 $\mu$V resolution medium power source/monitor unit (SMU) modules, and multifrequency capacitance measurement unit. Measurements were performed using specially designed measurement routines written in the frame of the “EasyEXPERT” software installed on the B1500 setup.

4. Results and Discussion

4.1. Selecting the Optimal Device Configuration

For finding an optimal device configuration for mobility assessment, we analyzed FETs with all available $L_{CH}$ and $W_{CH}$ variations at 300 K. The results extracted using Equation (1) and (2) for low-field mobility and quality factor are presented in Figure 2. Mobility for the devices varies more than 30 times, while only <6% variation was detected for the quality factor.

The obtained results correspond well to those presented previously in the publications related to similar devices (see, e.g., refs. [10-12,24]). The strong increase in mobility with a decrease in $W_{CH}$ should be probably attributed to the increase in the built-in stress.\cite{24} Indeed, change for $n$ during $W_{CH}$
variation is minor, suggesting small changes in scattering related to traps, and therefore only stress mechanism may be responsible for the effect. Our estimations showed an expected logarithmic growth dependence for the recalculated mobility–stress curve. Contrary to $W_{\text{CH}}$, a decrease in $L_{\text{CH}}$ causes a non-monotonic decrease in mobility (see Figure 3). Therefore, only after $L_{\text{CH}} > 200$ nm (4 in Figure 3), the mobility related to the stack can be assessed. The synchronized decrease in $n$ (Figure 2b) and increase in $\mu_0$ (Figure 2a and 3) suggests the possible influence of the extraction procedure. Indeed, since the decrease in $n$ suggests the decrease in the interface trap density that cannot vary with $L_{\text{CH}}$, this change should be attributed to the increasing recombination of carriers while measuring in STS regime. Accordingly, the diminished $n$ during the fitting causes the increase in $\mu_0$ values. This is one of the reasons why $D_{\text{IT}}$ should be estimated for possibly small $L_{\text{CH}}$, and in the best case for $L_{\text{CH}} < \lambda_{\text{eff}}$, as it was done in ref. [13]. Therefore, for the relevant low-field mobility, we should choose the one corresponding to the $1 \mu m > L_{\text{CH}} > 200$ nm range. This was the reason that we selected $L_{\text{CH}} = 500$ nm and $W_{\text{CH}} = 1 \mu m$ DUTs for temperature-dependent measurements.

4.2. Temperature Dependence of Low-Field Mobility

The experimental and fitted $I_d(V_g)$ dependencies for various temperatures for the nEG sample with $L_{\text{CH}} = 500$ nm and $W_{\text{CH}} = 1 \mu m$ are presented in Figure 4. Similarly to that in Figure 1, data and fitting are presented in both logarithmic and linear scales and show very high quality for fitting. Similarly, good fitting was achieved for all investigated samples. Only at $T_{\text{meas}} = 400$ K for the nSG and pSG samples enhanced drain/substrate leakage caused additional noise at low fields and due to this fitting quality was much degraded. We excluded these data from further consideration.

![Figure 2. a) Low-field mobility $\mu_0$ and b) quality factor $n$ data for devices under test (DUTs) with various channel length and width extracted from the $I_d(V_g)$ measurements at 300 K.](image-a)

![Figure 3. Change of low-field mobility $\mu_0$ with length ($L_{\text{CH}}$) for width ($W_{\text{CH}}$) = 1$\mu m$ extracted from the $I_d(V_g)$ measurements at 300 K. Error bars originate from measurements at multiple DUTs with similar dimensions (from 3 to 10 DUTs were measured for each $L_{\text{CH}}, W_{\text{CH}}$ pair). Various ranges (1–4) of $L_{\text{CH}}$ are discussed in the text.](image-b)
The values of the mobility components $\mu_{\text{ph}}, \mu_{\text{C}},$ and $\mu_N$ for the investigated samples extracted using Equation (4) are presented in Figure 6. The fitted mobility values for $T_{\text{MEAS}} = 300$ K are also presented. The presented data can be analyzed in numerous aspects. Several, most clear and remarkable tendencies are as follows. The mobility related to the Coulomb scattering, $\mu_C$, is larger for the EG stacks. This suggests larger FG interface trap densities and the increase in the related Coulomb scattering for the SG stacks. For the EG-type stacks, strong increase in the values of $\mu_N$ is seen for the change of the measurement conditions from $K = 0$ to $K = K_{\text{OC}}$. A similar increase was not detected for the SG-type devices. Moreover, $\mu_N$ values were smaller for SG stacks. This may indicate that the additional oxidation for the FG in the EG-type stack suppresses the neutral scattering centers at the FG and, moreover, makes their profile steeper. The increase in value of $\mu_{\text{ph}}$ is well seen for Si-SiGe alteration of the channel material for the pEG to pSG samples. Unfortunately, small values for the other two mobility components for this variation, leave the $\mu(300)$ unchanged and overall mobility lower for the pSG sample. Interestingly, phonon scattering is also smaller for EG→SG variation in n-type channels. This suggests that at least a part of the improvement in $\mu_{\text{ph}}$ for Si-SiGe variation can be attributed to the absence of the oxide layer in the SG stack, that is, to the absence of phonons related to that layer.

Using the described method, similar stacks subjected to slightly different fabrication processes (from so-called split wafers) can also be compared. We studied the same type nSG stacks from three wafers, subjected to the reference POR and two slightly modified fabrication processes R and O. The details of the applied processes are not the subject of the present publication and will be presented somewhere else.

Temperature dependencies $\mu_0(T)$ for the POR, R, and O samples with nSG stack for $K = 0$ and $K = K_{\text{OC}}$ are presented in Figure 7. As can be seen, the near-FG mobility is nearly similar for the POR and O case, but suppressed at high temperatures in R. However, the mobility in optimal coupling mode is noticeably improved in R and O stacks compared to that in POR.

The fitting and decomposition procedures, in this case, was simplified by the fact that we did not expect much difference in the $\mu_{\text{ph}}$ between the samples, so this parameter was optimized for the three samples at the same time. The results of mobility decomposition are presented in Figure 8. Interestingly, $\mu_C$ value varies only slightly between the samples. Contrary to that, changes in $\mu_N$ are more substantial. The analyses suggest that compared to POR, for the R sample neutral scatterers are redistributed closer to the FG region. As a result, the near-gate mobility is suppressed, however, the mobility in optimal coupling mode is increased substantially. For the O process compared to P, the near-interface mobility is slightly improved and the mobility in optimal coupling mode is improved further. Such analyses can definitely characterize the influences of the various fabrication processes on the stack characteristics and suggest ways for further improvements.

4.3. Comparison of Temperature Dependencies for $D_{\text{IT}}$ and $\mu_0$

Further possibilities for the analyses and characterization can follow from a comparison of the results obtained during $D_{\text{IT}}(E_{\text{IT}})$...
Figure 5. Temperature dependencies for low-field mobilities in four type of samples and two measurement conditions: a) – nEG and pEG samples for $K = 0$; b) – nEG and pEG samples for $K = K_{OC}$; c) – nSG and pSG samples for $K = 0$; d) – nSG and pSG samples for $K = K_{OC}$. Dotted curves represent best fitting using Equation (4).

Figure 6. Results for the decomposition of the temperature dependence of low-field mobility on components according to Equation (4) in nEG, pEG, nSG, and pSG samples and for $K = 0$ and $K = K_{OC}$ operation modes.
and \( \mu_0(T) \) data for the same stacks. We should remind that for FSCV, \( D_{IT}(E_{IT}) \), and \( \mu_0(T) \) measurements, different DUTs from the same chip were used. Namely (see ref. [13] for more details), the devices applied for the \( D_{IT}(E_{IT}) \) measurements were standard FET structures with a rectangular channel and four separated contacts for the FG, BG, source (S), and drain (D). The channel length of the FETs was \( L_{CH} = 100 \, \text{nm} \) and channel width \( W_{CH} = 150 \, \text{nm} \). For the FSCV measurements, 144 FETs connected in parallel (three contacts: FG, BG, S + D), with dimensions \( L_{CH} = W_{CH} = 2 \, \mu\text{m} \), each were applied. We will show here the results for the nSG stacks from the POR, R, and O samples.

In Figure 9, the data for the POR, R, and O samples are presented with double-ordinate axes, linear (left axis) in mobility, and logarithmic (right axis) for \( D_{IT} \). Note that \( D_{IT}(T) \) dependencies instead of \( D_{IT}(E_{IT}) \) are presented in the figures to correlate trap density with \( \mu_0(T) \). As it was mentioned earlier (see Figure 7, and the discussion there), in several cases mobility values significantly deviated from the fitted temperature dependencies and these effects were repeated for different dies. We wanted to find a possible explanation for the “fine structure” in the \( \mu_0(T) \) dependencies detected for the samples. Since the interface–trap density is a parameter strongly affecting mobility,[6] it will be logical to search for correlations between irregular behavior in \( \mu_0(T) \) and peaks in \( D_{IT}(T) \).

A considerable deviation from the \( \mu_0(T) \) dependence was observed in the O stack for \( K = 0 \) at \( T = 250 \, \text{K} \) (see Figure 9, O). At the same time, smaller suppression in \( \mu_0(T) \) for the \( K = K_{OC} \) was observed at \( T = 275 \, \text{K} \). At this temperature, peaks in \( D_{IT} \) can be seen correspondingly for the FG and for the BG interfaces. We can suppose that these features are correlated and
the appearance of charged traps related to front and back interfaces at 250 and 275 K causes a decrease in $\mu_C$ and in overall $\mu_0$. A somewhat similar effect is observed for the P stack in the $T = 250–300$ K range (see Figure 9, POR). On the contrary, an increase in $\mu_0(T)$ for R sample at $T = 250$ K (see Figure 9R) may be associated with $D_{IT}$ minima at that temperature for the FG interface. Moreover, relatively high $D_{IT}$ in R stack in the $T = 300–400$ K range suppresses overall near-FG mobility in the channel.

The results and tendencies presented in Section 4.2 and 4.3 can be analyzed further, especially if better statistics will be collected. However, even presented correlations indicate the extended potential of the method for characterization and for further improvement of the stacks.

### 4.4. Possible Applications of the Method and Limitations

The proposed method can be applied for the characterization of stack mobility in FDSOI FETs in three modes. Considering the purpose of the characterization and following the approach from ref. [13], we can label those modes as “monitoring,” “verification,” and “design” modes. Specially designated FET with appropriate parameters (e.g., with $L_{CH} = 500$ nm and $W_{CH} = 1 \mu m$) should be used for the characterization. The monitoring mode implies relatively fast, even in-line assessment of mobility at a single temperature (e.g., at 298 K) and for $K = 0$ at the specified location(s) of the wafer. This mode could be extended to the mapping of mobility for the whole wafer area.

For the verification mode, $I_d(V_G)$ measurements are performed at a single temperature and for stacks to be verified. Here, the parameters for the stack are confirmed using FSCV measurements, and the optimal coupling conditions ($K = K_{OC}$) are determined in separate preliminary measurements for each FET to be analyzed. After that, the $I_d(V_G)$ scans are performed for $K = 0$ and $K = K_{OC}$ conditions and the corresponding values for low-field mobility are obtained. This mode will allow distinction between the influence of interface and channel properties on mobility.

**Figure 9.** Results for the temperature dependencies in the POR, R, and O samples with the nSG stack for $\mu_0$ $K = 0$ (solid squares) and $K = K_{OC}$ (open squares) operation modes and $D_{IT}$ for front gate (FG) interface (solid circles) and back gate (BG) (open circles). Ordinate axes are linear (left) for mobility and logarithmic (right) for trap density. Curves present fitted dependences for $\mu_0(T)$ dependencies. $D_{IT}$ data points are connected with the lines to guide the eye.
The most powerful characterization mode requires measurements in a large range of temperatures (e.g., 100–400 K) and during the extended time, which makes this mode more appropriate for laboratory investigation. Moreover, considering the capabilities of the existing probers, only cutout dies could be analyzed at low temperatures. In return, in addition to the information that can be obtained in verification mode, it will be possible to estimate the influence of various scattering mechanisms for the stacks, behavior of mobility at various temperatures. Further valuable information can be obtained if parallel estimations for \( D_{\text{IT}}(T) \) will be performed for the stack(s).

As a limitation for the mobility measurements for a stack, we can see only a high leakage current between the gate(s) and source and drain in the FET. The fitting procedure of the measurement data and extraction of low-field mobility using Equation (1) and (2) showed high reliability. Substantially more care should be taken for decomposition of the obtained \( \mu_0(T) \) dependence on the components using the empirical expression (4). This process requires several rounds of multistep fitting. It is also worth remembering that decomposition is based on the semiempirical model\(^{[12,23]} \) and therefore the related interpretations should be done with care. Correlation of mobility data with the results for \( D_{\text{IT}}(E_{\text{IT}}) \) estimation for the same samples gives further clues for the interpretation of the characterization results.

5. Summary

Results of our study suggest that low-field mobility for the carriers in the FDHKMG SOI stacks can be assessed from measurements of \( I_d(V_C) \) dependencies in the range up to strong inversion for the FETs with specially selected dimensions. We further refined the expression for \( I_d(V_C) \) for the case under consideration including analyses of the DG operation mode for characterization of specific stack mobility.

Measurements of \( I_d(V_C) \) at various temperatures, various stacks, and channel types with the subsequent fitting of the obtained temperature dependencies of low-field mobility were performed. We also performed decomposition for \( \mu_0(T) \) dependencies on components related to a phonon, Coulomb, and neutral-defect carrier-scattering mechanisms using the existing semiempirical model. The obtained results clearly indicate the variation of carrier-scattering mechanisms for different stacks and the influence of applied fabrication processes. Moreover, comparing mobility values assessed from single-gate measurements and those assessed from DG operation in optimal coupling mode, it became possible to assess the vertical distribution of scattering centers in the stack. We also were able to detect a direct correlation between \( \mu_0(T) \) and \( D_{\text{IT}}(E_{\text{IT}}) \) distributions for the stacks.

The proposed characterization method of FDSOI HKMG stacks allows monitoring, characterization, and design of their properties. The method can be also useful in the analyses of the changes in the stacks during reliability measurements. Complementing this method with the earlier developed method for analyses of interface trap distribution opens additional possibilities for the understanding of mechanisms influencing device performance.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

Keywords
carrier mobility, FDSOI, HKMG FET, stack characterization

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