Quantum Circuit Transformations with a Multi-Level Intermediate Representation Compiler

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Abstract—Quantum computing promises remarkable approaches for processing information, but new tools are needed to compile program representations into the physical instructions required by a quantum computer. Here we present a novel adaptation of the multi-level intermediate representation (MLIR) integrated into a quantum compiler that may be used for checking program execution. We first present how MLIR enables quantum circuit transformations for efficient execution on quantum computing devices and then give an example of compiler transformations based on so-called mirror circuits. We demonstrate that mirror circuits inserted during compilation may test hardware performance by assessing quantum circuit accuracy on several superconducting and ion trap hardware platforms. Our results validate MLIR as an efficient and effective method for collecting hardware-dependent diagnostics through automated transformations of quantum circuits.

Quantum computing has emerged in recent years as a revolutionary approach to processing information using the principles of quantum mechanics. The quantum computational model is known to offer remarkable advances in algorithmic speed up for a number of problems that challenge conventional models, and there are many efforts to demonstrate quantum computational advantage. This includes theoretical results such as the algorithmic speedup available for factoring integers as well as experimental results such as the recent experimental demonstrations...
of so-called ‘quantum supremacy’ [1]. The success of these efforts depends on transforming algorithmic statements made within the model of quantum computing into instructions carried out by control hardware linked to quantum devices. Whereas a programmer routinely expresses quantum algorithms using a variety of high-level languages [2], the translation of these statements into executable instructions benefits greatly from the use of automated compilation tools.

Transforming quantum algorithms into physical instructions relies on compiling high-level languages into sequences of operations that act on the information stored in a quantum hardware register [3]. There are a variety of technologies being developed for quantum registers, including superconducting transmon qubits, trapped ions or atoms, and atomically doped silicon. Each technology supports a unique set of physical instructions and imposes a unique set of constraints that limit how these instructions may be executed. Tools that automate the decisions and translation of algorithms into technology-specific representations are vital for ensuring efficient and accurate execution [4].

A natural and easy-to-understand representation of the logical instructions executed during a quantum algorithm is the quantum circuit. An example of a quantum circuit is shown in Fig. 1 to highlight a series of gates acting on a pair of quantum register elements. Additional notation is defined below. This diagrammatic representation emphasizes the placement and assignment of instructions acting on individual registers, but it does not easily convey the temporal and spatial constraints imposed by a given technology. In addition, transforming such circuit representations into alternative logically equivalent forms requires the use of known rewriting rules. The quantum circuit representation has therefore been augmented with a variety of intermediate representations, which have been developed to represent and transform these quantum instructions.

Here we extend a novel adaptation of the multi-level intermediate representation (MLIR) for compiling quantum programs. MLIR was recently put forth by Nguyen and McCaskey as a powerful paradigm for expressing, parsing, and transforming quantum circuit representations at both the logical and physical levels [5]. Using LLVM infrastructure, their approach uses MLIR to demonstrate efficient transformations of a variety of quantum circuits.

We expand this use of MLIR to now implement transformations that create circuits for testing quantum circuit executions on noisy quantum computing hardware. These methods for verification and validation of quantum computers are based on a form of circuit transformation known as mirror circuits [6]. We present details on the methodology and implementation of these transformation alongside experimental results obtained from compiling test circuits to several different quantum computing hardware targets. These methods reveal characteristic differences in technologies and demonstrate the utility of combining MLIR with quantum compilation.

Quantum Compiling

The quantum circuit representation is a useful, human readable, and diagrammatic description of quantum computer programs. At the machine level, specific intermediate representations (IR), often not intended for human reading, and native to specific architectures, are used. Various IRs, MLIR included, can be derived from quantum assembly language (QASM), which itself is frequently compiled from higher level circuit representations. The IR thus represents an endpoint in a tool-chain or compiler/transpiler stack that reduces high-level user input, often expressed in a quantum circuit paradigm, to a machine-readable format. Many current quantum computer programming and compilation tool stacks offer such an IR endpoint.

Within this compiler concept, users often think of quantum programs visually. Users may envision a program as a circuit directly, and subsequently take on the task of translating the circuit into a high level language such as qiskit, which is then compiled (and in many cases, transpiled) by the remainder of the qiskit toolchain. It is useful to outline in brief then, the concepts contained at this high level, before outlining their reduction to MLIR.

In Fig. 1, the qubit register is denoted by the labels $q_i$, while the corresponding classical register, which is used to store the values obtained after quantum measurements, is denoted $c$. These two registers differ greatly in terms of the physics
of their representation of information: a qubit exists in a continuum of possible states on the Bloch sphere, with states along the surface of the sphere representing superpositions of the states “0” and “1” (which are themselves represented by the poles). The classical register, on the other hand, consists of the traditional binary, or “bit” representation of information, in which each information carrier can exist in either the state “0” or “1”, but not superpositions thereof (this also rules out concepts like entanglement from the classical register).

Quantum circuits typically end with the measurement gate performed on a portion of the quantum register, and subsequent storage in the classical register for return to classical computer resources. The measurements report the resulting quantum computation that occurs throughout the circuit. Key elements of the quantum circuit include quantum gates, often acting on single and two-qubit subsets, although three or more qubit quantum gates are possible and can be expressed in this notation. Figure 1 shows several of the key gate components required for universal quantum computation: quantum “bit flip” (\(X\)) gates, Hadamard (\(H\)) gates, which are specific rotations along the Bloch sphere, rotations about specific axes of the sphere (see \(R_y(\theta)\) in Fig. 1), and finally the controlled-not gate (CNOT, represented by the node, or control, connected to the crossed-circle, representing the target). These quantum logic gates are somewhat analogous to their classical logical counterparts with a key exception. The truth table of the CNOT gate, when applied to quantum superpositions, results in “entanglement”, which means that the two qubits involved in the gate have become quantum-correlated. Measurements reveal these correlations, while subsequent quantum gates in the circuit may exploit these correlations to establish key advantages in quantum programs over their classical counterparts. The circuit diagram, and the resulting MLIR can fully capture this abstract concept within their logical notations.

Quantum Circuit Transformations

The expression of a given quantum algorithm in terms of quantum logic gates acting on a qubit register is not unique as the same composite unitary operation can be decomposed into a product of simpler unitary operations in many ways. Since different quantum devices provide different sets of native quantum gates implemented in physical hardware, the final form of a gate-based IR for a given quantum circuit must consist of only those gates which are natively implemented by the target quantum processing unit (see Fig. 2). Additionally, the final gate-based IR must respect the physical connectivity between qubits, thus necessitating the insertion of the SWAP gates into the IR such that all 2-qubit quantum gates act on physically connected qubits (qubits that can directly interact and entangle with each other).

Given physical hardware constraints, a typical quantum circuit IR transformation is aimed at reducing the depth of the circuit and/or the total number of elementary gates, especially single-qubit \(T\) gates and multi-qubit entangling gates, which is a hard optimization problem with complexity growing rapidly with the circuit size [7], [8]. Importantly, for some quantum algorithms such quantum circuit transformations result in a constant depth IR [9], [10]. Reducing the depth of the quantum circuit typically increases the fidelity of its output on a noisy quantum computing device. However, different quantum gates have different fidelities or error rates, and accounting for this requires a more complex circuit transformation with an optimization functional based on individual gate fidelities [11].

Traditionally, quantum circuit transformations include the following stages: circuit synthesis, postsynthesis optimization, and technology mapping [12]. Such multi-stage quantum circuit transformations can benefit from gradual IR lowering introduced by MLIR. Below we describe an ad-
Mirror Circuit Transformations

Mirror circuits are a method for estimating the error in a quantum processor’s implementation of some circuit $C$ [13]. Mirror circuits are designed to address the problem that the output of $C$ cannot be efficiently verified as correct in general. This is because a general quantum circuit $C$ cannot be efficiently simulated on a classical computer, so the output from running a quantum circuit $C$ on a quantum computer cannot be compared to what we would have got if $C$ had been run without any errors. Mirror circuits are circuits that are similar to $C$, but whereby each mirror circuit will always output the same easily predictable bit string if run without error. This makes it easy to quantify the error in the execution of these circuits, and from this we can approximate the error with which $C$ has or could be implemented.

A set of mirror circuits $\{M(C)\}$ is constructed from a “base” circuit, which is the circuit we want to quantify a particular quantum processor’s performance on. The version of mirror circuits used in this work is introduced in Ref. [13] and it is defined for any circuit containing only Clifford gates and $Z(\theta)$ gates (arbitrary rotation around the $Z$ axis). This encompasses many widely used universal gate sets. A mirror circuit consists of a “compute-then-uncompute” structure alongside randomized elements that are added in to guarantee sensitivity to all errors that impact $C$ (some kinds of coherent errors can be echoed away by a compute-then-uncompute Loschmidt echo). Each mirror circuit $M(C)$ consists of (1) the circuit $C$, (2) a layer of random Pauli gates, (3) a “quasi-inverse” circuit, (4) a measurement of each qubit in the computational basis. The “quasi inverse” consists of $C$ in reverse with each gate replaced with its inverse except that the angles of the $Z(\theta)$ gates are updated to commute the central Pauli through the circuit. A complete description is given in Ref. [13].

Each mirror circuit $M(C)$ has a corresponding “target” bit string $s$ that it will always output if the circuit is run without errors. The theory in Ref. [13] shows that the probability of observing this bit string ($P$) is closely related to the fidelity with which the tested processor can implement $C$. In this work, we use a performance metric for $C$ computed from $\epsilon = (1 - \sqrt{P}) \approx (1 - P)/2$. We square root $P$ to remove the contribution of errors in the quasi-inverse circuit to $P$’s deviation from 1, so $\epsilon$ is then an estimate for the error in $C$. In particular, we report the mean and minimum of $\epsilon$ over the ensemble of (random) mirror circuits constructed and executed alongside a given $C$.

Quantum Circuit Transformations using MLIR with QCOR

We implement the transformation required by the mirror circuit theory using the QCOR programming framework. As shown in Figure 4, QCOR is a full-stack quantum compilation and execution framework based on the LLVM’s MLIR infrastructure. Specifically, quantum programs in various languages are parsed and transformed into a unified MLIR leveraging the quantum dialect that was developed previously [5]. QCOR provides a collection of passes, which represent the basic infrastructure for transformation.
and optimization within the MLIR. These passes are specific to quantum computing and includes techniques for quantum gate simplification and substitution.

In MLIR, the transformation of the IR tree is managed by a PassManager that configures and schedules a pipeline of passes. For example, QCOR defines various optimization levels, each of which enables a different set of circuit optimization passes to balance the compilation runtime and the optimality of the resulting quantum executable. Passes operate on Operation instances which are the main abstraction of MLIR. For instance, sub-routine (function) level transformations are associated with MLIR’s FuncOp representing callable function objects. Similarly, the global transformation of the whole program is defined by ModuleOp passes, whereby ModuleOp is MLIR abstraction for top-level container operation.

A pertinent pattern of QCOR transformation passes is the IR tree traversal via static single assignment (SSA) use-def chain tracing and in-place replacement or removal of MLIR Operation nodes. By following the use-def chain of qubit lines, we can establish the directed acyclic graph (DAG) representation of the compiled program amenable to quantum circuit transformation protocols, e.g., gate optimization or circuit mirroring. Once a pass identifies an IR sub-tree matching its target pattern, it will perform the corresponding transformation, such as canceling quantum gate operations or replacing a sequence of gates by an equivalent yet more optimal substitute.

Here, we focus attention on a specific type of IR transformation for verification and validation (V&V) based on the mirror circuit method outlined above. In digital computing technology, compilers often provide V&V toolings, e.g., injecting extra debug symbols or instrumentation into the binary executable in certain build modes. These tools assist developers with error detection and localization, especially in complex codebases. In QCOR, we put forward a custom V&V compiling mode for quantum programs leveraging the mirror circuit technique, as shown in Figure 5.

The mirror circuit validation module consists of a compiler instrumentation transformation pass and a run-time library. The compile-time IR transformation modifies the MLIR tree to insert its instrumentation around the main quantum execution zone. It is worth noting that in an IR tree, there are a variety of node types declaring variables and functions, yet there should only be one so-called entry point function defining the main program flow. Thus, in the validation build mode, QCOR instruments this entry point IR segment with LLVM function calls into the QCOR run-time library to facilitate the mirror circuit construction, execution, and post-processing. This results in a custom V&V binary for the input quantum program whose execution involves both the original algorithmic quantum circuit and a set of corresponding Pauli-randomized mirror circuits (see Figure 5). Subsequently, the execution results, e.g., bit-string distribution, are annotated with validation data, such as the estimated success probability of the algorithmic circuit.

We use the example of the quantum circuit first presented in Figure 1 using the diagrammatic representation and now presented in Figure 6 as a snippet in a quantum program written in OpenQASM version 3.0. QCOR supports parsing of this high-level programming language into the MLIR. In this program, we define a simple quantum kernel, named ansatz (lines 5-13), to construct a parameterized quantum circuit designed to solve the Deuteron ground state energy with the variational quantum eigensolver (VQE) algorithm [14]. In the main program flow, we
Figure 5. MLIR transformation for V&V of backend execution. When V&V is enabled, qcor compiler will inject additional operations to the IR, and hence the resulting binary executable to run mirror circuits alongside the algorithmic circuit on the target QPU. The results of these mirror circuits are used to compute a fidelity estimate of the base circuit execution for V&V purposes.

allocate some qubits (line 15) then invoke the kernel with a randomly selected parameter value for demonstration purposes.

Figure 6 also demonstrates the use of the QCOR command-line executable qcor to compile the OpenQASM code. This command accepts a compiler switch, -validate, that enables the mirror circuit IR transformation by adding an MLIR pass that implements the instrumentation injection into the IR tree. In addition, as a re-targetable compiler, QCOR targets a growing list of hardware backends via the -qpu flag. Passing the backend name in the format of <provider name>:<device name> instructs the compiler to output a program representation that can be executed on the given target, as described in more detail elsewhere [15].

We test compilation and execution of the demonstration program on commercial quantum computing hardware from Honeywell Quantum Solutions, IBM, and IonQ as well as a numerical simulator. We test on the IBM ibmq_lima and ibmq_bogota devices, which are part of the second-generation Falcon family of transmon architectures. Public information from IBM shows ibmq_bogota and ibmq_lima have a quantum volume of 32 and 8, respectively, with the former expected to be more performant. For trapped-ion devices, we test IonQ’s 11-qubit hardware developed in 2019 and the Honeywell Quantum Solutions 12-qubit H1 hardware labeled HQS-LT-S2. We also test the Honeywell Quantum Solutions emulator HQS-LT-S1-SIM, which is intended to provide a high-fidelity model for a closely related H1 device labeled HQS-LT-S1.

In these tests, we configure the program to use 32 Pauli-randomized mirror circuits with each circuit sampled by 1024 measurement shots. This suffices for the small test circuit used here, but larger quantum circuits are expected to require additional randomized trials. The average and minimum success probability are recorded as $P' = \sqrt{P} = 1 - \epsilon$ with $\epsilon$ the error in the circuit. The results of executing the code on all of these devices is shown in Fig. 6, and the mirror circuit validation mode on various backends are summarized in Table 1.

Our tests show that the results for success probability prediction $P'$ correlate with four commonly-used measures of statistical similar-
Table 1. Results of mirror circuit validation on different quantum hardware and emulator accelerators. $P'$ is the prediction for the circuit’s success probability based on the success probability of mirror circuits. We run 32 mirror circuits and report the average and minimum values of $P'$. The probability distribution distance measures are computed against the theoretical distribution obtained by numerical simulation of the algorithmic circuit. Here, we present the Wasserstein (W) distance (also known as Earth mover’s distance), the Energy (E) distance, the Kullback–Leibler (KL) and Jensen–Shannon (JS) distance for comparison.

| Name                | Descriptions                          | mean($P'$) | min($P'$) | Probability Distribution Distance |
|---------------------|---------------------------------------|------------|-----------|-----------------------------------|
| HQS-LTS1-SIM        | Honeywell Quantum Systems, H1 Emulator| 0.992175   | 0.988212  | W 0.009 | E 0.071 | KL 0.035 | JS 0.018 |
| HQS-LTS2            | Honeywell Quantum Systems, H1 Hardware| 0.991576   | 0.980274  | W 0.006 | E 0.055 | KL 0.020 | JS 0.010 |
| ibmq_lima           | IBM, Falcon r4T processor, 5 qubits   | 0.951753   | 0.91714   | W 0.016 | E 0.089 | KL 0.046 | JS 0.023 |
| ibmq_bogota         | IBM, Falcon r4L processor, 5 qubits   | 0.935946   | 0.913584  | W 0.012 | E 0.088 | KL 0.038 | JS 0.019 |
| IonQ-2019           | IonQ trapped ion processor (11 qubits)| 0.962767   | 0.855436  | W 0.022 | E 0.107 | KL 0.082 | JS 0.041 |

...ity. The latter compare experimental outcomes against the idealized results and, as shown in Table 1, measures for i) the Wasserstein distance, ii) the energy distance, iii) Kullback–Leibler divergence, and iv) the Jensen–Shannon distance correlate with the success probability prediction. It is notable that these varying distance metrics weigh divergence between the ideal and actual results differently and, for the current data set, the measures all show the same trends.

The in-situ validation information provided by mirror circuits is valuable for evaluating programs on near-term quantum devices. This information helps account for performance variations that arise between qubits on the same chip or from drift during calibration cycles. For example, the ibmq_bogota device is reported to have a larger quantum volume than ibmq_lima, but the latter demonstrated similar success probability min($P'$) for the mirror-circuit validation runs. This is corroborated by similarities in the energy distance metric. However, many different factors may contribute to changes in the distance measures, including performance drift between execution of the base and mirror circuits and a proportional difference in terms of gate noise versus readout error between devices. The in-lined testing provided by the transformed circuits enable an efficient assessment of such differences. Our current analysis method for the mirror circuit data is known to be more accurate when gate errors dominate the overall circuit error, and future improvements will help quantify the impact of readout error.

Conclusions

We have presented the first example of using MLIR for automatic generation of quantum circuit transformations that allow for collection of additional information for verification and validation of quantum circuit execution. This additional information is collected via coordinated execution of additional mirror circuits that allow one to estimate the fidelity of the original application circuit’s execution on a given hardware platform. Our implementation with the QCOR compiler generates the required hardware instructions to run the original application circuit as well as the mirror circuits upon activation by a compilation flag. We have validated our implementation on several available quantum devices and discovered notable trends with other measures of similarity that corroborate our results.

We anticipate that the MLIR, and its implementation, will prove useful for other tasks required by the verification, validation and debugging of quantum computers. These tasks require hardware-derived information about the quality of program execution that will become increasingly important as classical simulations of rapidly scaling quantum computers become intractable in the near future [1], [16]. For example, recently introduced methods for using mirror circuits to provide debugging information about quantum circuits through local circuit inversions [17] would natural map to the automated workflow enabled by using MLIR for circuit transformations. Our demonstrations of MLIR within in QCOR, and the accessibility of these transformation at compile, offer a robust and convenient methods for quantum programming. In summary, we advocate for the view that automated circuit trans-
formations and implementation of debugging and verification tasks in a manner that requires little user intervention are promising applications of advanced quantum compilation techniques.

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