Noise-Induced Performance Enhancement of Variability-Aware Memristor Networks

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Towards the implementation of more robust resistive switching systems

Performance Enhancement
“Based on Stochastic Resonance”

Programming Signal

Nonlinear System

NOISE

IN

OUT

Memristor and/or Memristive system

Stochastic Resonance Peak

Noise magnitude
Memristor Devices and Applications

Memristor-based Cell and Memristor Crossbar

Variability in Memristor Crossbar

Stochastic Resonance on Memristance Enhancement

Noise-induced Bit-Error-Rate Reduction

Conclusions
Memristor Devices and Applications

Wide range of devices

Wider range of Applications

Memory

Computing

Both

In-Memory Computing

Memristor-based logic
(IMPLY, MAGIC, MRL)
Memristor ANNs

[Meijer, G.I., Science 319(5870) (mar 2008) 1625–1626]
[Intel Corporation: Revolutionizing Memory and Storage]
[Kvatinsky, S., Belousov, D., Liman, S., Satat, G., Wald, N., Friedman, E.G., Kolodny, A., Weiser, U.C., IEEE TCAS:II (2014)]
[E. Lehtonen, J. H. Poikonen, and M. Laiho, IEEE ISCAS, Seoul, South Korea, May 2012]
[Kvatinsky, S., Wald, N., Satat, G., Kolodny, A., Weiser, U.C., Friedman, E.G., CNNA 2012]
## Metal Oxide: Bipolar Filament

| Metric                          | Value                      | Quality |
|--------------------------------|----------------------------|---------|
| Scalability                    | $F_{\text{min}} < 10\text{nm}$ | ✅✅     |
| MLC                            | Possible                   | ✅      |
| 3D integration                 | Feasible                   | ✅✅     |
| Fabrication cost               | Low                        | ✅✅     |
| Retention                      | Long (>10yrs)              | ✅✅     |
| Latency                        | Medium (0.3-10us)          | ✅      |
| Power                          | Medium                     | ✅      |
| Demonstrated Write Endurance   | Medium ($\leq 1\text{E}10$ cycles) | ✅     |
| Variability                    | Problematic                | ❌      |

[Table BC2.7 in the International Roadmap for Devices and Systems. “Beyond CMOS,” 2018.]
Stanford-PKU Metal-Oxide Memristor Model

Conductive Filament Evolution

Conductive Filament Dynamics

Conductive Filament Construction

Conductive Filament Disruption

Conductive Filament Variability

Do not forget the Temperature

Currents through the Device

Device Parasitics

[Li, H., Jiang, Z., Huang, P., Wu, Y., Chen, H. Y., Gao, B., Liu, X. Y., Kang, J. F. & Wong, H. S., DATE 2015]
1T1R Configuration for Memristor Crossbar

1T1R ReRAM-based Memory Cell

SET and RESET Processes of the ReRAM Cell

Diagram showing the schematic of a 1T1R ReRAM-based memory cell and the voltage-time graphs for SET and RESET processes.
ReRAM Crossbar Configuration

ReRAM crossbar array with the read/write peripheral circuitry.

Writing (long pulses) and Reading (short pulses) of words in the crossbar array.
SET and RESET variations in the Crossbar Array

Device-to-Device

DAC Output under variations

Both Device-to-Device Cycle-toCycle
Stochastic Resonance
(from the perspective of Engineers):

“An *increase* to the input noise can result in an *improvement* in the output signal-to-noise ratio (SNR)”

Where to find Stochastic Resonance?
- Earth’s climate changes
- Electronic circuits
- Differential equations
- Lasers
- Neural models
- Physiological neural populations and networks
- Chemical reactions
- Ion channels
- SQUIDs (superconducting quantum interference devices)
- Ecological models
- Cell biology
- Financial models
- Psychophysics
- Carbon nanotube transistors
- Nanomechanical oscillators
- Organic semiconductor chemistry
- Social systems

Stochastic Resonance requires:
(a) A form of Threshold
(b) A driving signal
(c) A source of noise (inherent or external)

Performance(noise+nonlinearity) > Performance(nonlinearity)

[Gammaitoni, L., Hänggi, P., Jung, P., & Marchesoni, F. (1998). Reviews of modern physics, 70(1), 223.]
[McDonnell, M. D., & Abbott, D. (2009). PLoS computational biology, 5(5)]
Stochastic Resonance on Memristance Enhancement

**SR through intrinsic Noise**

**SR by external noise excitation**

[Ntinas, V., Rubio, A., Sirakoulis, G. Ch., Cotofana, S. ISCAS 2019]

[Stotland, A., & Di Ventra, M. (2012). Physical Review E, 85(1)]

[Ntinas, V., Rubio, A., Sirakoulis, G. Ch., Rodriguez, R., Nafria, M. NANOARCH 2019]
SR-based Performance Enhancement

Noisy Write Signal Applied to Each Row

SR vs Cycle-to-Cycle Variability

SR vs Device-to-Device Variability

SR vs Both kinds of Variability
Conclusions

• High levels of **fabricated memristor’s variability** postpones the scaling of memristor-based memories

• A **noisy disturbance** delivers **reduced Bit-Error-Rate** by assisting the writing process of the devices in the Memristor Crossbar Array.

Future Work

• A **transistorless** Memristor Crossbar configuration will be investigated

• **Experimental** demonstration of SR-based Performance Enhancement using externally applied **white noise**
Thank you for your attention