Thermal resistance of GaN/AlN graded interfaces

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Compositionally graded interfaces in power electronic devices eliminate dislocations, but they can also decrease thermal conduction, leading to overheating. We quantify the thermal resistances of GaN/AlN graded interfaces of varying thickness using *ab initio* Green’s functions, and compare them with the abrupt interface case. A non-trivial power dependence of the thermal resistance versus interface thickness emerges from the interplay of alloy and mismatch scattering mechanisms. We show that the overall behavior of such graded interfaces is very similar to that of a thin-film of an effective alloy in the length scales relevant to real interfaces.

The common strategy of interfacing two pure semiconductors via a gradual alloyed region poses a design trade-off: on the one hand, a thicker alloyed region is desirable in order to accommodate the lattice mismatch; on the other hand, a thick alloy will also negatively impact the thermal conductance across the interface, possibly degrading a device’s lifetime. For example, common substrate designs for High Electron Mobility Transistors (HEMTs) include a graded transition region between GaN and AlN as thick as 1.5 µm [1]. For substrates grown on Si, this region contributes only 3% of the total substrate thermal resistance. But if one replaces Si by diamond, the graded interface thermal resistance amounts to 20% of the total. For common operating conditions in HEMTs this translates into a 10–20°C higher temperature of the active region, shortening the device’s lifetime by one half [2].

Thus, it may pay off to try to make the graded region as thin as possible while still satisfying some minimum structural constraints. To do this one needs to know how the interface thermal resistance depends on its thickness and composition profile. Theoretically quantifying it is, however, a nontrivial problem due to the simultaneous emergence of quasiballistic transport, wave interference effects, and the interplay between large-scale features and atomic-scale disorder. All this leads to a thermal resistance that no longer depends linearly on thickness when the latter gets below the µm range. Experimentally one can only access the thermal conduction of the structure as a whole, which typically includes many different material interfaces in a single sample. This makes it difficult to quantify the upper limits to interface conductance based on experiments alone. It is therefore very important to theoretically predict the thermal conductance of graded interfaces, to know how much the grading strategy is degrading the performance of devices, and how much improvement could be achieved by other schemes, like reducing thickness or using digital structures. We tackle this question here for the technologically important case of GaN/AlN interfaces, which are ubiquitous in power electronics where thermal dissipation issues are a major concern.

The use of graded interfaces to reduce threading dislocation density was theoretically tackled by Tersoff using an analytical model, and has been deeply explored in subsequent modeling studies for two decades [3, 4]. The specific grading length and profile to satisfy structural constraints (e.g. dislocation density or strain) depends on the particular problem in hand. The structural constraint aspect is not the goal of this paper, and we refer the reader to earlier literature. In contrast, the thermal limiting aspect of graded interfaces does not appear to have been theoretically investigated before. Current approaches to investigate interface thermal conductance atomistically are based on Green’s functions [5–11]. However, when the interface is structurally complex or disordered in an extended region of space, like in the case of graded interfaces, it is impractical to simulate the whole atomically disordered interface. Doing so would require approximating the disordered interface by multiple realizations of exceedingly large supercells, periodic in the directions parallel to the interface [8].

A method to overcome this limitation was demonstrated in Refs. 12 and 13. The basic idea is that the perturbation part of the Hamiltonian can be written as the sum of a contribution from the average perturbation over the layer (the “compositional profile” contribution), plus the local deviation with respect to this average for each atom (the “disorder” contribution). The total phonon scattering intensity is the sum of the scattering intensities of each of the two contributions separately, plus the interference term between them, which is neglected on the grounds of phase cancellation due to disorder. The “compositional profile” scattering term preserves the phonon quasimomentum component parallel to the interface, and can be efficiently calculated using atomistic Green’s functions. The “disorder” term does not preserve quasimomentum, and it is computed within the framework of the virtual crystal approximation. Using realistic compositional profiles and *ab initio* calculated force constants, a good agreement with experiment was obtained for superlattices with periods comprising up to 45 atomic layers, without using any adjustable parameters [12, 13].

The approach implemented for superlattices is not di-
The transmission is subsequently used within the Monte Carlo solver implemented in almaBTE [18]. For each incoming mode, only outgoing modes which conserve the parallel wavevector and the frequency are considered (for transmission or reflection).
tance is negligible compared to the scattering from alloy disorder. In this context, one can model the step graded structure as an effective alloy in which the mass disorder scattering contribution is similar to that of an alloy with concentration $\text{Ga}_x\text{Al}_{1-x}\text{N}$ such that

$$\tilde{x}(1 - \tilde{x}) = \frac{1}{N} \sum_{i < N} x_i (1 - x_i),$$

where $x_i$ the concentration in each layer of the alloy. A similar approach has been shown to give excellent results in the context of superlattices [13]. Here, $\tilde{x} \simeq 0.24$ and in the continuous limit $\tilde{x} = 1/2 - \sqrt{3}/6$. At the same time, the phonon spectrum, average masses and three-phonon properties of this effective alloy correspond to those of the average alloy (here with concentration $\text{Ga}_{0.5}\text{Al}_{0.5}\text{N}$). Finally, the finite length of the interface limits the mean-free path of the phonons, as described in Ref. [19]. As shown in Figure 2, such an approximation gives excellent results in the range of lengths applicable to real interfaces, from nanometer to micrometer scales. We also observe in the lower panel a power law similar to the one found for AlGaN alloys thin films [19].

In the limit of an infinitely long interface, the resistance should follow an asymptotic trend equal to the total length divided by the average of the bulk conductivities of the different alloys, here 25.9 W/(m K) compared to the bulk conductivity of the effective alloy of 22.8 W/(m K). In the limit of an infinitely thin interface, the conductivity becomes limited by the transmission probability and the resistance of an abrupt interface is computed to be 2 m$^2$ K/GW. In contrast, a step graded interface of 9 nm already has a resistance of 3.4 m$^2$ K/GW, showing that the alloy scattering will start to dominate for longer interfaces. Interestingly, this latter value is very much in line with the resistance of the effective alloy (see middle panel of Figure 2). Indeed, at these small length scales the resistance originating from mismatch scattering is partially compensated by a lowering of the resistance caused by alloy scattering, due to the simultaneous filtering of phonon modes at the successive interfaces.

This effect is illustrated by Figure 3, which displays the energy-resolved spectral heat flux of a structure including a GaN/AlN (001) step graded interface of 90 nm. The successive interfaces are very transparent to the main conduction channels at low energies, while the alloy scattering strongly limits the mean free path of the optical modes around 50 rad/ps compared to the pure materials. The high-frequency features above 100 rad/ps are due to the redistribution of phonon population, since their mean-free path is barely impacted by alloy scattering compared to the aforementioned modes around 50 rad/ps.

We now discuss the potential optimization of such interfaces. On the one hand, making the graded interface thicker lowers the density of threading dislocations. This improves overall performance in a device-dependent fashion that can be complex to quantify. On the other hand, thicker interfaces can also reduce performance because of device heating resulting from an increased thermal resistance. The balance between these counteracting ef-
FIG. 3: Energy-resolved spectral heat flux in a GaN/AlN (001) step graded interface of 90 nm, as computed from Monte Carlo simulations. Upper panel: full structure including the buffer layers; lower panel: zoom close to the interface.

Effects will lead to an optimal grading thickness, which should be optimized on a case-by-case basis for each device. Some current devices are grown on silicon substrate that can be 1000 µm, which adds a thermal resistance of ~7700 m²K/GW. In such cases the device thermal resistance is dominated by the substrate, making it advantageous to have thick graded regions, since the gain in electrical performance by reducing dislocations is greater than the thermal penalty they contribute.

The picture is very different, however, if a good thermally conducting substrate is employed. For example, diamond’s thermal conductivity is 17 times higher than silicon’s, translating into a ~450 m²K/GW thermal resistance for 1000 µm thickness. As Figure 2 shows, in this case the resistance contributed by the graded interfaces in the device would already be a non-negligible part of the total. A difficulty in making good conducting substrates is related to the thermal resistance of the bonding between the substrate and the device. However, very low thermal resistances have recently been achieved for diamond/GaN and SiC/GaN, of 36 and 4.1 m²K/GW respectively [20–22]. On such new-generation substrates it can pay off to reduce the thickness of the graded regions to some extent, at the expense of an increased dislocation density, to decrease overheating and enhance efficiency and device lifetime.

An increased dislocation density can also lead to increased thermal resistance. However, ab initio calculations and analysis of experimental data indicate that, for dislocation densities under $1 \times 10^{10} \text{cm}^{-2}$ the thermal conductivity reduction in GaN due to dislocations is minimal, and has been overshadowed by thin film effects in previous experiments [23]. The threading dislocation density in GaN directly grown on sapphire, SiC, or Si (111) is typically between $1 \times 10^{8}$–$1 \times 10^{10} \text{cm}^{-2}$ [24].

The mean-time-to-failure (MTF) of a device is affected by different mechanisms, and its temperature dependence depends on the particular device in hand [25–28]. Common temperature dependences of GaN device MTFs follow exponential behaviors, and may decrease by one order of magnitude for every $\sim 50 \, ^\circ \text{C}$ increase in the temperature of the active region. The operation temperature of High Electron Mobility Transistors can reach well above one hundred degrees Celsius. In the well-bonded diamond substrate case above, the over 20% thermal resistance contributed by a 1 µm-thick graded interface may thus lead to overheating by $20 \, ^\circ \text{C}$ and shorten the device’s MTF by half.

In conclusion, using an ab initio Green’s function approach we have computed the lattice thermal resistances of a series of GaN/AlN (001) step graded interfaces of different lengths. We find that mismatch scattering is very weak in the main conduction channels, such that alloy scattering becomes dominant in the regime relevant for real interfaces (10 nm to 1 µm). The computed resistance of the step graded interface is well approximated by that of a model thin-film of an effective alloy, and it strongly deviates from the classical Fourier law predictions. The resistance of 1 µm and 100 nm thick interfaces exceeds conventional estimates by twofold and fourfold respectively. In the case of well-sunk devices, graded interfaces add a non-negligible contribution to overheating, and it can be advisable to shorten the thickness of the step graded interfaces at the expense of a larger density of threading dislocations. The thermal resistances calculated in this article represent a valuable information for the optimization of GaN-based power electronic devices.

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