Area-Scalable $10^9$-Cycle-High-Endurance FeFET of Strontium Bismuth Tantalate Using a Dummy-Gate Process

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Abstract: Strontium bismuth tantalate (SBT) ferroelectric-gate field-effect transistors (FeFETs) with channel lengths of 85 nm were fabricated by a replacement-gate process. They had metal/ferroelectric/insulator/semiconductor stacked-gate structures of Ir/SBT/HfO$_2$/Si. In the fabrication process, we prepared dummy-gate transistor patterns and then replaced the dummy substances with an SBT precursor. After forming Ir gate electrodes on the SBT, the whole gate stacks were annealed for SBT crystallization. Nonvolatility was confirmed by long stable data retention measured for $10^5$ s. High erase-and-program endurance of the FeFETs was demonstrated for up to $10^9$ cycles. By the new process proposed in this work, SBT-FeFETs acquire good channel-area scalability in geometry along with lithography ability.

Keywords: FeFET; ferroelectric; nonvolatile; semiconductor memory; SBT

1. Introduction

Ferroelectric-gate field-effect transistors (FeFETs) comprising SrBi$_2$Ta$_2$O$_9$ (SBT) or Ca$_x$Sr$_{1-x}$Bi$_2$Ta$_2$O$_9$ (CSBT) ferroelectrics have unique characteristics of high endurance against at least $10^8$ cycles of program and erase operations [1–12]. CSBT is a kind of SBT family which was derived from original SBT by Sr-site substitution with Ca. The material natures of SBT [13–32] and CSBT [33–36] have been intensively studied previously. FeFETs using CSBT with about $x = 0.2$ showed larger memory windows than those with SBT [5]. The invention of long-retention FeFET was first reported in 2002 and consisted of a metal/ferroelectric/insulator/semiconductor (MFIS) stacked-gate structure of Pt/SBT/(HfO$_2$)$_{0.75}$/(Al$_2$O$_3$)$_{0.25}$/(HAO)/Si [37]. Since then, we have investigated characteristics of (C)SBT-FeFETs [1–3,38–44], improved the device performance [4–8,45,46], and developed FeFET-integrated circuits [9–12,47–52]. For improving the single FeFET performance, we succeeded in reducing gate voltage ($V_g$) from the initial 6–8 [1] to 3.3 V [8]. Another progress was in shrinking gate-metal length ($L_m$) from the initial 10 µm [1] to 100 nm [7].

The conventional (C)SBT-FeFETs were formed by etching the gate stacks. By decreasing the FeFET gate length, SBT etching-damage problems [29–32] on the gate-stack sidewalls became significant. Since we recognized that $L_m = 100$ nm was approaching the shortest limit by the conventional method based on etching, we changed the fabrication strategy to shape the gate stacks from etching-down to filling-up. The new (C)SBT-FeFET process is outlined as follows: Dummy-gate transistor patterns with self-aligned source- and drain regions are prepared in advance. The dummy substance is selectively removed to leave grooves which are later filled up with SBT precursor. Gate electrodes are formed. Finally, whole gate stacks of Ir/SBT/HfO$_2$/Si are annealed for SBT crystallization. In the new FeFET process, the (C)SBT sidewall of the gate stack is not exposed to etching plasma. The sidewall is thus free from etching damage problem [6]. Consequently, the ferroelectric becomes more controllable in terms of quality and more scalable in terms of geometry than by the etching. The new FeFET dimensions follow good lithography progress with an
adequate height of (C)SBT to show large memory windows increasing with the ferroelectric thickness \cite{3,45}. In this work, SBT-FeFETs with gate channel lengths \( L_{ch} = 85 \) nm were first reported by adopting the proposed process. Excellent characteristics were demonstrated such as 10\(^9\) cycle erase-program endurance and long stable retention for 10\(^5\) s. The endurance and retention were as good as those of the conventional (C)SBT-FeFETs formed by the gate-stack etching \cite{1-12}.

2. Materials and Methods

2.1. Device Fabrication Process

The fabrication process (schematic drawings shown in Figure 1) in this work is as follows:

- **Step 1: Si substrate preparation.** A \( p \)-type Si substrate patterned with FET active areas was prepared. Local-oxidation-of-silicon (LOCOS) process was used in the patterning for device isolation. The LOCOS patterns with various channel widths (\( W \)) were designed in a sample chip. Areas for source-, drain- and substrate-contact holes on the Si were heavily ion-doped. Sacrificial Si\( \text{O}_2 \) on Si was removed with buffered hydrogen fluoride.

- **Step 2: Insulator deposition.** A 5 nm thick Hf\( \text{O}_2 \) was deposited on the Si substrate by a large-area pulsed-laser deposition system (Vacuum Products Corporation, Kodaira, Tokyo, Japan) \cite{53}. A KrF laser was irradiated on a ceramic Hf\( \text{O}_2 \) target in 15.3 Pa N\( \text{O}_2 \) ambient \cite{54}. The substrate temperature was 220 °C.

- **Step 3: Lithography.** Electron-beam (EB) lithography was performed by spin-coating an organic resist, exposing 130 kV EB, and developing. Resist patterns 550 nm tall were left on the Hf\( \text{O}_2 \)/Si. They were later used as ion-implantation mask in Step 4 and as dummy gates in Step 7.

- **Step 4: Ion implantation.** Hf\( \text{O}_2 \) uncovered with resist was etched out by inductively-coupled-plasma reactive-ion etching (ICP-RIE). On the exposed Si, As\(^+\) ions were implanted for source and drain. The energy and dose conditions were 4 keV and 5.0 \( \times \) 10\(^{12}\) \( \text{cm}^{-2} \).

- **Step 5: Si\( \text{O}_2 \) deposition.** An 830 nm thick Si\( \text{O}_2 \) was deposited to cover the resist patterns on the substrate by 300 W rf sputtering in 0.1 Pa Ar.

- **Step 6: Flattening Si\( \text{O}_2 \).** The Si\( \text{O}_2 \) was etched back and flattened by ICP-RIE with 1.0 Pa Ar-CF\( \text{4} \) mixed gas until tops of the resists or dummy gates were exposed.

- **Step 7: Leaving grooves on gates.** The dummy-gate substances were selectively removed by O\( \text{2} \) plasma ashing. There remained grooves in a 410 nm tall Si\( \text{O}_2 \) isolation. The grooves were located on the Hf\( \text{O}_2 \) with self-aligned source and drain regions prepared in Step 4. The whole chip was rapidly annealed at 800 °C in ambient N\( \text{2} \).

- **Step 8: Ferroelectric deposition.** SBT precursor film was deposited to fill up the grooves by a metal-organic-chemical-vapor deposition (MOCVD) system (WACOM R&D, Nihonbashi, Tokyo, Japan). Sources of Bi(C\(_5\)H\(_{11}\)O\(_2\))\(_3\), Sr[Ta(OC\(_2\)H\(_5\))\(_5\)(OC\(_2\)H\(_4\)OCH\(_3\))]\(_2\) and Ta(OC\(_2\)CH\(_3\))\(_3\) (Tri Chemical Laboratories Inc., Uenohara, Yamanashi, Japan) were used \cite{6}. As-deposited precursor-film thickness was estimated as 80 nm on a flat place of the substrate.

- **Step 9: Metal deposition.** Ir was deposited by rf sputtering on the SBT precursor layer. Resist mask was patterned for gate electrodes by EB lithography.

- **Step 10: Forming gate electrodes.** Ir uncovered with resist was etched out by Ar\(^+\) ion milling. Then, the resist mask was removed by O\( \text{2} \) plasma ashing.

- **Step 11: FeFET completed.** SBT precursor was deposited again by MOCVD to cover the substrate \cite{6}. The whole substrate was annealed for crystallization of the SBT to show ferroelectricity. The annealing condition was at 780 °C in \( \text{O}_2\)-N\( \text{2} \) mixed gas we investigated before \cite{8}. Finally, contact holes for gate, source, drain and substrate were formed by ultraviolet g-line lithography and Ar\(^+\) ion milling.
2.2. Reason for Using SBT in FeFET

The gate stack of MFIS should be regarded as MFI(IL)S, as shown in Figure 2a, where F, I, IL, S are connected in series. The IL is an interfacial layer between I and S which is formed during the ferroelectric crystallization annealing process of FeFETs [8,39,55–57]. The main component of IL is silicon dioxide with an electric permittivity ($\varepsilon_{IL}$) of $\varepsilon_{IL} = 3.9$. In the MFI(IL)S, $|P_F| \approx \varepsilon_0 \varepsilon_I |E_I| = \varepsilon_0 \varepsilon_{IL} |E_{IL}| = |Q_S|$ is satisfied in any time. The $P_F$ is ferroelectric polarization. $E_I$ and $E_{IL}$ are electric fields in the I and the IL. The $Q_S$ is charge area density in the semiconductor surface. The $\varepsilon_I$ is a relative permittivity of I. The $\varepsilon_0$ is the vacuum dielectric constant of $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m. For a simplified explanation, we assumed a virtual equivalent circuit of series capacitance as drawn in Figure 2a which is expressed by $|P_F| \approx |Q_I| = |Q_{IL}| = |Q_S|$ with virtual charges $Q_I$ and $Q_{IL}$ on I and IL, respectively. In MFII(IS), the IL suffers from a stress of field $|E_{IL}| \approx |P_F| / (\varepsilon_0 \varepsilon_{IL}) = 8.7$ MV/cm even at a small $|P_F| = 3 \mu C/cm^2$. For example, real IL thickness is 2.6 nm [8] or about 1 nm [55–57]. Electric-field-assisted tunnel current through such a thin SiO$_2$ [58,59] brings charge injection into the gate stack from S across IL. In erase-and-program operations, a large $E_{IL}$ derived from a large $P_F$ swing induces significant trapped-charge accumulation which accelerates endurance degradations [2,52]. According to our experience [43,52,60], $|P_F|$ should normally be less than 2.5 $\mu C/cm^2$ all the time and should not exceed 2.0 $\mu C/cm^2$ for further high-endurance requirements of the FeFET.
Ferroelectric materials show $P_F$ versus $E_F$ hysteresis loops as illustrated in Figure 2b. The $E_F$ is the electric field across the F. We defined $E_{\text{max}}$ as the positive maximum $E_F$ and $P_{\text{max}}$ as the $P_F$ at $E_F = E_{\text{max}}$. Similarly, $E_{\text{min}}$ and $P_{\text{min}}$ are the negative minimum $E_F$ and the $P_F$ at $E_F = E_{\text{min}}$. The loop is called “major” loop when the $E_{\text{max}}$ and $E_{\text{min}}$ are strong enough to force $P_F$ saturated, whereas it is called “minor” loop when $P_F$ is unsaturated by moderate $E_F$ swing. In SBT-FeFETs, restrictions of $P_{\text{max}} \leq 2.5 \mu C/cm^2$ corresponding to the minor loops are used during all operations as we emphasized in early works [39,43,52,60].

Regarding a ferroelectric hidden in MFI(IL)S, an exact symmetric swing maximum, i.e., $P_{\text{max}} = |P_{\text{min}}|$ or $E_{\text{max}} = |E_{\text{min}}|$, is difficult because $Q_S$ versus $Q_S$ is very asymmetric [61,62]. The $Q_S$ is the charge area density of the semiconductor surface and $Q_S$ is the surface potential. Presence of the flat-band voltage $V_{\text{fb}}$ makes the symmetric swing further difficult. However, to simplify the physical explanation, $P_{\text{max}} = |P_{\text{min}}|$, $E_{\text{max}} = |E_{\text{min}}|$ are assumed as shown in Figure 2b with $V_{\text{fb}} = 0$V. In every $P_F$-$E_F$ loop, the $E_F$ width at $P_F = 0$ is defined as $E_w$ being related with a voltage memory window ($V_w$) by an approximate expression $E_w = 2E_c = V_w/d_F$, where the $E_c$ is a coercive field and $d_F$ is ferroelectric thickness. According to a method we proposed before [43], an important characteristic $E_{\text{max}}$ of the ferroelectric can be evaluated which has not been measurable by direct probing on a FeFET. If $P_{\text{max}}$ is provided, a gate voltage $V_g$ to achieve a target memory window $V_w = E_w/d_F$ can be estimated as a sum of $E_{\text{max}}d_F$, $E_1d_1$, $E_2d_2$, and $Q_S$ at $Q_S = P_{\text{max}}$. An exact discussion can be found in the paper [43].

For instance, Pt/SBT/HAO/Si FeFETs showed $E_w = 18$ kV/cm at $P_{\text{max}} = 2.0 \mu C/cm^2$ and $E_{\text{max}} = 25$ kV/cm [43]. By adopting an advanced process [8], Ir/CSBT/HfO$_2$/Si FeFETs had the best improved values of $E_w = 65$ kV/cm at $P_{\text{max}} = 2.0 \mu C/cm^2$ and $E_{\text{max}} = 140$ kV/cm [3,43]. A good reason for using (C)SBT in Si-based FeFETs is the (C)SBT ferroelectric nature of a convenient minor $P_F$-$E_F$ loop [14,17,20] which has $E_w$ available and is controllable in a restricted $P_F$ range of $P_{\text{max}} \leq 2 \mu C/cm^2$ with $E_{\text{max}} \leq 140$ kV/cm.

There are some other ferroelectric materials also intensively studied for applications in Si-based MFIS FeFETs. Regarding Pb$_5$Ge$_3$O$_{11}$ (PGO), attempts to develop replacement-gate-type Pt/PGO/ZrO$_2$/Si FeFETs were reported [63] but the erase-program-test results of the FeFETs were not found although the ferroelectric itself showed a good potential $P_{\text{max}}$ $E_{\text{max}}$ and $E_w = E_{\text{max}}$ judging from hysteresis loops of the PGO metal/ferroelectric/metal capacitors [64]. Regarding another candidate, the ferroelectric HfO$_2$ family [55–57,65–70], the intrinsic material nature may not be suitable for applying to Si-based FeFETs. Informative minor hysteresis loops were reported on Y-doped HfO$_2$ in which $E_w$ seemed nearly equal to 0 V/cm at $P_{\text{max}} = 2.0 \mu C/cm^2$, although it was as large as about 1 MV/cm at $P_{\text{max}} = 10 \mu C/cm^2$ [66]. Operation of the FeFETs under the restriction of $P_{\text{max}} \leq 2 \mu C/cm^2$ may be difficult. Some reports suggested that HfO$_2$-FeFETs cannot help using a large $P_{\text{max}}$ ($>>2 \mu C/cm^2$) [52,53]. The large $P_{\text{max}}$ may induce significant charge injection into the gate.
As far as we know, fair works on HfO$_2$-FeFETs have not cleared $10^8$ cycles endurance in spite of using sophisticated production facilities [56,67–70].

3. Results and Discussion

3.1. Device Dimensions

A cross-sectional scanning-electron-microscope photograph of an Ir/SBT/HfO$_2$/Si FeFET fabricated by the new proposed process is shown in Figure 3a. Figure 3b shows the same picture added with support lines to clarify the material boundaries. The schematic drawing of the FeFET was assigned with four terminals of gate, drain, source and substrate (Figure 3c). The gate-channel length ($L_{CH}$) was $L_{CH} = 85$ nm. The gate-channel width was $W = 100$ µm depending on the initial LOCOS pattern designed in Step 1 in Section 2.1. The metal-gate length $L_m$ was 150 nm which could be shorter but was not the focus in this work. The SBT precursor film thickness was about 80 nm measured on a flat place. By filling gate grooves with SBT precursor (Step 8 in Section 2.1.), the effective SBT height ($H$) was finally about 450 nm which was a distance between Ir and HfO$_2$. Area scalability of the new FeFET was equivalent to that of the dummy gates which are organic resist patterns made by lithography. From the viewpoint of Si transistor technology, $L_{CH} = 10$ nm is expected to be the critical limit [71]. A significant Curie-temperature decrease in SBT started when particle were sizes of around 20 nm [25]. Thus, the prospective shortest limit of $L_{CH}$ by our proposed FeFET process may be around 20 nm.

![Figure 3](image_url) Cross-section of a FeFET with $L_{CH} = 85$ nm fabricated in this work. (a) Original photo by SEM observation and (b) the photo with supporting lines added to clarify material boundaries. (c) Schematic drawing assigned with gate, drain, source and substrate terminals for electrical characterizations.

3.2. Electrical Characterizations

In this study, memory windows, endurance and retention of FeFETs were investigated at room temperature. A semiconductor parameter analyzer (4156C, Keysight Technologies, Santa Rosa, CA, USA) was used for measuring static drain current versus gate voltage ($I_d$–$V_g$) curves of the FeFETs. A pulse generator (81110A, Keysight Technologies, Santa Rosa, CA, USA) was used to apply $V_g$ pulses. The instruments were computer-controlled using programs written by the language of LabVIEW (ver. 10, National Instruments, Austin, TX, USA).

3.2.1. Memory Windows

As an elementary test of the FeFETs, $I_d$–$V_g$ hysteresis loops were investigated (Figure 4). The $I_d$ was measured by $V_g$ increments and decrements with 0.1 V steps. The $V_g$ sweeping ranges were $V_g = 1 ± 4$ V, $1 ± 5$ V and $1 ± 6$ V. Drain voltage ($V_d$), source voltage ($V_s$) and substrate voltage ($V_{sub}$) were fixed to $V_d = 0.1$ V and $V_s = V_{sub} = 0$ V during the measurements. The $I_d$–$V_g$ showed hysteresis loops drawn in counter-clockwise directions because the FeFET was an $n$-channel-type one. In an $I_d$–$V_g$ curve, threshold voltage ($V_{th}$) was defined as a $V_g$ value at $I_d/W = 1 × 10^{-7}$ A/cm. Two $V_{th}$ values were extracted from the left- and right-side curves in an $I_d$–$V_g$ hysteresis loop. A memory window was defined...
as the \( V_{th} \) difference. In this work, we call this a static memory window (\( V_w \)) because \( V_g \) sweep by 4156C is slow. The static \( V_w \) was, for instance, 1.0 V by sweeping \( V_g \) from −5 to 7 V then back to −5 V, or at \( V_g = 1 \pm 6 \) V as expressed in Figure 4. During the measurement of a wide-range \( I_d \) from \( 10^{-12} \) to \( 10^{-4} \) A as indicated in Figure 4, \( V_g \) sweep speed depends on the current range. Therefore, an \( I_d-V_g \) hysteresis curve only gives reference information that is not suitable for accurate discussion.

![Figure 4. Static static drain current versus gate voltage (\( I_d-V_g \)) curves of a FeFET with \( L_{ch} = 85 \) nm. The channel width was \( W = 150 \) \( \mu \)m. \( V_g \) ranges were \( V_g = 1 \pm 4 \) V, \( 1 \pm 5 \) V and \( 1 \pm 6 \) V.](image)

For an accurate understanding, the FeFET performance, a pulsed \( V_g \) with a controlled time width, was applied to the FeFETs for the erase (\( Ers \)) or program (\( Prg \)) operation. The \( V_g \) pulse heights with the time widths were (\( V_E \), \( t_E \)) for Ers, and (\( V_P \), \( t_P \)) for Prg, respectively. For the n-channel-type FeFET, the \( V_E \) was negative (\( V_E < 0 \) V) and \( V_P \) was positive (\( V_P > 0 \) V) [9]. The pulse time widths \( t_E \) and \( t_P \) were the same with each other in this work (\( t_E = t_P = t_{EP} \)). After, Ers and Prg, \( I_d-V_g \) curves were individually measured with a small common \( V_g \) range for Read. Two \( V_{th} \) values were defined in the \( I_d-V_g \) curves as the \( V_g \) at \( I_d/W = 1 \times 10^{-7} \) A/cm. They were expressed as \( V_{thE} \) after Ers and \( V_{thP} \) after Prg. The \( V_{thE} \) was larger than the \( V_{thP} \) [9]. The \( V_{th} \) difference of \( \Delta V_{th} = V_{thE} - V_{thP} \) was defined as a memory window obtained by read operation after erase-and-program pulse applications. The memory window \( \Delta V_{th} \) is normally smaller than the above-mentioned static \( V_w \), because slow switching components in a ferroelectric do not respond to short pulses [27,72,73]. The \( V_{thE} \) and \( V_{thP} \) were investigated by repeating a series of operations: Ers, Read, Prg, Read, in this order (Figure 5a). In Ers, a pulsed \( V_g \) of (\( V_E, t_E \)) was applied with keeping \( V_d = V_s = V_{sub} = 0 \) V. In Read after Ers, a \( V_{thE} \) was extracted from an \( I_d-V_g \) curve drawn by narrow-range varying \( V_g \) from 0 to 1.1 V at \( V_d = 0.1 \) V and \( V_s = V_{sub} = 0 \) V. In Prg, a pulsed \( V_g \) of (\( V_P, t_{EP} \)) was applied, keeping \( V_d = V_s = V_{sub} = 0 \) V. In Read after Prg, a \( V_{thP} \) was extracted from an \( I_d-V_g \) curve drawn exactly the same conditions as those in Read after Ers.

Figure 5b shows \( V_{thE} \) and \( V_{thP} \) by Read after Ers and Prg for three sets of (\( V_E, t_{EP} \)) and (\( V_P, t_{EP} \)) of \( |V_E| = V_P = 6, 7 \) and \( 8 \) V. Every marker corresponds to the measured \( V_{thE} \) and \( V_{thP} \). Memory windows, \( \Delta V_{th} = V_{thE}-V_{thP} \), as a function of pulse height \( |V_E| = |V_P| \) (Figure 5c) and width \( t_{EP} \) (Figure 5d) can be seen in Figure 5b, where the \( V_{thE} \) and \( V_{thP} \) results (not shown in Figure 5b) of other \( V_P \) (\( = V_E \)) conditions were also used. Short \( V_g \) pulses of \( t_P = 50 \) ns were available for Ers and Prg of the FeFET. Memory windows of \( \Delta V_{th} > 0.7 \) V were obtained using 8 and 8.5 V pulses.
Figure 5. Investigation of $V_{\text{thE}}$ and $V_{\text{thP}}$ by applying $V_g$ pulses to a FeFET with $L_{\text{ch}} = 85 \, \text{nm}$. The channel width was $W = 100 \, \mu\text{m}$. (a) The measurement procedure; (b) measured original $V_{\text{thE}}$ and $V_{\text{thP}}$; (c) pulse-height dependence of $\Delta V_{\text{th}} = V_{\text{thE}} - V_{\text{thP}}$ and (d) pulse width dependence of $\Delta V_{\text{th}}$.

Figure 5c,d show a clear monotonic $\Delta V_{\text{th}}$ increases when raising either the pulse height or width. Good analog $V_{\text{thE}}$ and $V_{\text{thP}}$ controllability was suggested by smooth and linear $\Delta V_{\text{th}}$ growths with raising $\log(t_{\text{EP}})$ as shown in Figure 5d. The similar tendencies of $\Delta V_{\text{th}}$ and $t_{\text{EP}}$ have already been reported in our previous works [3,5,7,9,52]. In the prior FeFETs, poly-crystalized ferroelectrics were visualized by electron backscatter diffraction (EBSD) [44]. The EBSD indicated that the (C)SBT consisted of multi-grains with various crystal orientations in the FeFETs. The poly-crystalized ferroelectrics may bring the analog $V_{\text{thE}}$ and $V_{\text{thP}}$ controllability to the FeFETs. In the present FeFET, there must be numerous grains in channel-width direction with $W = 100 \, \mu\text{m}$ whereas a single grain or a few were expected in channel-length with $L_{\text{ch}} = 85 \, \text{nm}$ which was smaller than average diameters of SBT grains freely grown in-plane [44].

In a preferable geometry of the replacement-gate FeFET in the future, only the channel area $L_{\text{ch}} \times W$ will be intensively scaled down with remaining the height $H$. The $H$ is decided by the gate-groove depth in Step 7 in Section 2.1 and Figure 1. The $\Delta V_{\text{th}}$ in this report was not yet at its best ability considering the ferroelectric height $H = 450 \, \text{nm}$. In the vertical direction of FeFET, a gate stack by filling SBT should be essentially the same as a large $L_{\text{ch}}$ conventional one by etching SBT. Therefore, potential $\Delta V_{\text{th}}$ will become the same as that of conventional FeFETs by improving the details in the fabrication process in Section 2.1. An immediate target for the present FeFET will be realizing $\Delta V_{\text{th}} = 0.7 \, \text{V}$ by $Ers$ of $(-6 \, \text{V}, 10 \, \mu\text{s})$ and $Prg$ of $(6\, \text{V}, 10 \, \mu\text{s})$ for $H = 190 \, \text{nm}$ as demonstrated before using Pt/CSBT/HfO$_2$/Si FeFETs [7].

3.2.2. Retention

Retention of a FeFET was measured by the procedures as shown in Figure 6a,b. After program ($Prg$), Retain and Read were repeated during the scheduled time. In $Prg$, a $V_g$ pulse of $(V_P, t_{\text{EP}})$ was applied with $V_d = V_s = V_{\text{sub}} = 0 \, \text{V}$. In Retain, all the terminals were kept at
zero as \( V_g = V_d = V_s = V_{sub} = 0 \) V. In \textit{Read} at a certain time \( t \), an \( I_d-V_g \) curve was drawn by varying \( V_g \) in a narrow range from 0 to 1.0 V at \( V_d = 0.1 \) V and \( V_s = V_{sub} = 0 \) V. A \( V_{thP} \) was extracted from the \( I_d-V_g \) and plotted with a marker at \( t \) as shown in Figure 6c. After completing the \( V_{thP}-t \), \( V_{thE}-t \) started to be measured. In erase (Ers), a \( V_g \) pulse of \((V_E, t_{EP})\) was applied with \( V_d = V_s = V_{sub} = 0 \) V. After Ers, Retain and Read were repeated during the scheduled time. The Retain and Read conditions for \( V_{thE}-t \) were the same as those for \( V_{thP}-t \). In the Read at a certain time \( t \), an extracted \( V_{thE} \) was plotted with a marker at \( t \) as shown in Figure 6c. In this work, \( V_P = 8 \) V, \( V_E = -8 \) V and \( t_{EP} = 10 \) µs. The retention was measured for \( 10^5 \) s in each of \( V_{thP}-t \) and \( V_{thE}-t \). At \( t > 10^3 \) s, they were still distinguishable with a difference \( \Delta V_{th} = 0.26 \) V. When \( t > 10^3 \) s, as shown in Figure 6c, the gradient of the \( V_{thP}-\log(t) \) and \( V_{thE}-\log(t) \) curves appeared to be nearly zero. A possible ten-year retention was suggested by extrapolation lines drawn on the last three markers in each branch. The present \( L_{ch} = 85 \) nm FeFET showed a good retention to the same extent as those of the conventional (C)SBT FeFETs [1–9,11,12,37–40,42,45,46,52].

**Figure 6.** Retention investigation after applying \( V_g \) pulses to a FeFET with \( L_{ch} = 85 \) nm. The channel width was \( W = 100 \) µm. The measurement procedures for the retentions of (a) \( V_{thP} \) after \( Prg \) of \((V_P, t_{EP})\) and (b) \( V_{thE} \) after Ers of \((V_E, t_{EP})\). (c) The measured retentions for \( 10^5 \) s each. Dashed lines are extrapolations of \( V_{thP}-\log(t) \) and \( V_{thE}-\log(t) \) for estimating \( V_{thP} \) and \( V_{thE} \) after ten years.

### 3.2.3. Endurance

Endurance of a FeFET was measured by the procedure shown in Figure 7a. After imposing endurance cycles on FeFETs, pairs of \( V_{thE} \) and \( V_{thP} \) were obtained. The endurance cycles consisted of periodic bipolar \( V_g \) pulses for an alternate Ers of \((V_E, t_{EP})\) and \( Prg \) of \((V_P, t_{EP})\) with \( V_d = V_s = V_{sub} = 0 \) V. The endurance-cycle application was interrupted at certain scheduled cycle numbers (\( N \)). After the \( N \) cycle application, \( V_{thE} \) and \( V_{thP} \) were read as follows: a series operation of Ers, Read, \( Prg \), and Read, in this order was performed. In Ers, a single \( V_g \) pulse of \((V_E, t_{EP})\) was applied with \( V_d = V_s = V_{sub} = 0 \) V. In Read after Ers, an \( I_d-V_g \) was measured by varying \( V_g \) in a narrow range from 0 to 1.5 V at \( V_d = 0.1 \) V.
and \(V_s = V_{\text{sub}} = 0\) V. A \(V_{\text{thE}}\) was extracted from the \(I_d-V_g\) and plotted with a marker at \(N\) as shown in Figure 7b. In \(Prg\), a single \(V_g\) pulse of \((V_{P}, t_{\text{EP}})\) was applied with \(V_d = V_s = V_{\text{sub}} = 0\) V. In \(Read\) after \(Prg\), an \(I_d-V_g\) was measured under the same conditions with \(Read\) after \(Ers\). The obtained \(V_{\text{thP}}\) was plotted with a marker at \(N\) as shown in Figure 7b.

![Figure 7. Endurance of a FeFET with \(L_{\text{ch}} = 85\) nm. The channel width was \(W = 80\) \(\mu\)m. (a) The measurement procedures of applying endurance cycles and reading \(V_{\text{thE}}\) and \(V_{\text{thP}}\). (b) Endurances were measured up to \(N = 10^{8}\) cycles for 7.5 \(V\) \(V_g\) pulse heights and \(N = 10^{9}\) cycles for 8 \(V\).

As shown in Figure 7b, the \(Ers\) of \((-7.5\) V, 10 \(\mu\)s) and \(Prg\) of (7.5 \(V\), 10 \(\mu\)s) were first applied for an endurance up to \(N = 10^{8}\) cycles. Next, a stronger input of \((-8\) V, 10 \(\mu\)s) and (8 \(V\), 10 \(\mu\)s) was applied to the same FeFET up to \(N = 10^{9}\) cycles. No significant shifts of \(V_{\text{thE}}\) and \(V_{\text{thP}}\) were observed throughout the measurements. By taking the minimum of the \(V_{\text{thE}}\) and the maximum of the \(V_{\text{thP}}\) in the endurance test, \(\Delta V_{\text{th}} = 0.40\) \(V\) for \(|V_E| = V_P = 7.5\) \(V\) and \(\Delta V_{\text{th}} = 0.57\) \(V\) for \(|V_E| = V_P = 8\) \(V\) were obtained. These were margins for distinguishing \(V_{\text{thE}}\) from \(V_{\text{thP}}\) as indicated in Figure 7b. In spite of using the rather complicated dummy-gate process, the \(L_{\text{ch}} = 85\) nm FeFET fabricated showed high endurance up to \(10^{8}\)~\(10^{9}\) cycles. This is the same as the endurance level that (C)SBT-FeFETs inherently have [1–12].

4. Summary

A new fabrication process of a FeFET was proposed and demonstrated. Dummy-gate patterns with self-aligned sources and drains were prepared on a Si substrate. HfO\(_2\) with a thickness of 5 nm was inserted in advance between the dummy-gate substance and the Si substrate. The dummy substance was selectively removed to form a self-aligned groove on the gate. A thin SBT precursor film was deposited to fill up the groove. After forming the Ir gate electrode on the SBT, the whole gate stack was annealed for the SBT crystallization. The finished FeFET of Ir/SBT/HfO\(_2\)/Si had a channel length \(L_{\text{ch}} = 85\) nm. The FeFET exhibited a \(10^{9}\) cycle-high endurance and long stable retentions measured for \(10^{5}\) s. By adopting the replacement-gate process, area-scalable SBT-FeFETs with the high endurance and long retention were successfully produced.
**Author Contributions:** Conceptualization followed by numerous improvements with respect to the device structure and processing, M.T.; the anneal and MOCVD processes, S.S.; SEM observation, M.T.; creation of PC-controlled measurement programs, S.S.; electrical measurement of the devices, S.S.; data analysis and discussion, S.S. and M.T.; writing—original draft preparation, M.T.; writing—review and editing, M.T. and S.S. All authors have read and agreed to the published version of the manuscript.

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