A Derivation of Technology Roadmaps for SOC Design Services in the Post Moore’s Law Era

Chi-Yo Huang* and Yu SUN

Department of Industrial Education, National Taiwan Normal University, Taipei 106, Taiwan
*Corresponding author

Keywords: System-on-Chip, Design service, Technology mining, Decision making trial and evaluation laboratory, Technology roadmap.

Abstract. The design service firms can play dominant roles is the post Moore's law era. However, how the SOC design service industry could evolve in the post Moore’s law era were seldom discussed. Further, how future technologies may migrate from the aspects of integrated circuit design techniques, SOC, and VLSI technology were seldom discussed from the service aspect. In this work, the technology roadmaps will be developed based on patent mining results. The confidence can be effectively used to measure the relationship between two keywords. Based on the calculation of confidence, the relationship between keywords can be determined. The results of measuring association rules can be derived. Based on the matrices, the influence relation maps (IRMs) can be derived by using the DEMATEL. These maps are the prototypes of the technology maps which will further be confirmed in the future. Further, the keywords will be confirmed, and the time frame will be added based on experts' opinions.

Introduction

The Moore’s Law, which has successful predicted the number of devices that can be fabricated on a chip doubled every 18 months, is reaching the theoretical physical limits. The ceasing of the Moore’s law can happen in future 10 years, with 7nm being the last commercial processing node [1]. The termination of the Moore’s Law can be the strategic inflection point to the Systems-on-Chip (SOC) designers. As the cost of each new process node increases, design teams will have to find other means to create more complex systems while achieving better performance and power dissipation; SOC designers who select to reconfigure existing designs, choose more efficient system structures, and enhance communication on the chip will succeed in this mega trend [2].

The SOC design service is a business model which aims to finish the SOC specification definition or the SOC design. The service providers can help finish the rest of the design processes being needed for SOC innovation. The competences being required by the providers include the application capabilities of the most advanced IC/SOC technologies, specialized SOC design, layout, and manufacturing skills, as well as domain knowledge, etc. The SOC design services include SOC front end logical design, physical design services, turnkey services, and silicon intellectual property (SIP) transactions and integration services. As the IC industry migrates to the post Moore’s Law era which is characterized by limitations in further chip performance enhancement, power reductions and smaller form factors.

The SOC service providers are facing opportunities being introduced by the coming termination of the Moore’s law. From the aspect of SOC front end and backend designs, the termination of the Moore’s law introduces opportunities for SOC design engineers to enhance the efficiency of future chips from resizing the devices and chips, increase the efficiency of the manufacturing process, shorten the time of on-chip signal transportations and faster turn-around time [2]. Further, the SOC design efficiency can be improved by considering the power consumption, design cost and time at the same time and achieve the aspired level. Assembly and packaging of the SOC can be another focus. The proven circuits in the format of hard IPs can be integrated with other hard IPs or circuits as an
electronic system being packaged into a 3D IC. The introductions of such well-verified and proven hard IPs can greatly reduce the design risk, time, and thus cost [3] for the SOC being fabricated by using the most advanced techniques. Finally, from the aspect of design automation tools, the electronic design automation (EDA) tools can increase the productivity and reduce the complexity of system level design by reducing the developing time [4].

However, how the SOC design service industry may evolve in the post Moore’s law era were seldom discussed. Further, how future technologies may evolve from the aspects of SOC front and backend design, turnkey services, and SIP provision and integration were seldom discussed from the service aspect. Not to mention how these R&D as well as service capabilities of an SOC design service firm can expand in future five to ten years.

Therefore, the author aims to define a multiple rule decision making (MRDM) methods based analytic framework for resolving the problems. The trend of IC design techniques will be derived by using the patent mining technique.

Literature Review

Robert Galvin, the CEO of Motorola in the 1980s, defined the technology roadmap as “an extended look at the future of a chosen field of inquiry composed from the collective knowledge and imagination of the brightest drives of change in that field” [5-8]. Kostoff and Schaller defined the technology roadmap as an agreement regarding to future science and technology; the tool can be used as a basis for decision makers’ identification, evaluation, and selection of possible strategies being used to achieve science or technology goals or targets of research and development (R&D) [9, 10]. The technology roadmap demonstrates an overview of future science and technology R&D plans in the format of maps. The road-mapping procedure is the illustration of the roadmap which always contains a multiple layers time-based graphical illustration of a R&D plan. The plan links future devices, technology, sub-systems, and end-products with target markets [11].

The technology roadmap has long been regarded an important strategic planning tool for future technology [12, 13]. Further, technology roadmaps can be used to generate of novel concepts or ideas for R&D of future products and technology as well as forecasting trends of technology as well as identifying future technology with good potential [14, 15]. Thus, the technology roadmap and the associated roadmapping techniques have already interested numerous scholars and real-world managers. The roadmaps have widely been adopted by many firms and research institutes [16].

The roadmapping processes usually need to identify the influence relationships between different layers, which mean various devices, components, sub-systems, techniques, etc. The time for the introduction and correlation between each component of the roadmaps should be clearly identified.

One of the widely adopted roadmapping approach is the one being proposed by the European Industrial Research Management Association [17] which contains the market, product, and technology layers. The identification of correlations between layers is mainly based on opinions being provided by experts [10, 18]. In the era of big data analytics, a practical process of integrating the data into roadmaps is becoming feasible and more dominant.

Research Methods

The SOC design service roadmap will first be developed according to following three keywords (1) IC design techniques, (2) SOC, (3) VLSI. Then, the patents being related to either one of the three keywords will be mined. The frequency of the technology terms happening in the literature will first be confirmed by experts as important. Then, the texts will be grouped by using the clustering analysis. Then, the high frequency texts which be selected as candidates for deriving the “if-then” inferential rules by using the Dominance Based Rough Set Approach (DRSA). The core attributed being derived by the DRSA will serve as the dominant technologies. One dominant technology belonging to one of the five layers which may influence another dominant technology belonging to other layers will be
selected as the conditional variable while the dominant technology being influenced will be selected as the decision variable. The decision rules being derived will then be clustered into three groups based on the coverage ratios. The high coverage ratio rules will then be introduced into the DEMATEL. The condition variables being introduced in the decision rules being derived will be introduced as the ones which influence the decision variable(s) in the same rule. The support between the dominant technologies will be introduced as the degree of influence relationship belonging to two dominant technologies. Then, the total influence relations will then be derived. The total influence relation map will be defined as the keyword-relational map.

Empirical Study Results

In order to verify the method being proposed, an empirical study based on patent researching on United States Patent and Trademark Office (USPTO) will be applied in this section. The patent mining program was programmed by using the R language. Based on the keywords which include VLSI, IC Design Automation, and SOC, related patents were retrieved. In this Section, the empirical study results will be demonstrated.

The first step of text mining is patent retrieval. In order to obtain sufficient patent information, we use the R language for patent exploration. We chose United States Patent and Trademark Office (USPTO) as our patent database, it is an agency of the United States Department of Commerce which provides patent protection, commodity trademark registration and intellectual property certifications for inventors and their inventions.

The VLSI, IC Design Automation, and SOC are used as the keyword for patent retrieval. And limit in the patent title. The top 200 patents with the highest citation rate were being searched separately by using the key works, VLSI, “IC Design Automation” and SOC. And then, the top 30 keywords with the highest frequency are derived. Then, the top patents being mined were mined by using the R language based text mining tool, TM, for data mining.

After all patent documents in the patent data set were parsed, preliminary keywords were selected. Then, the top 30 keywords can be derived from the patents related to VLSI, IC Design Automation, and SOC based on the frequency of these keywords. The next step is to construct the keyword vector, which will be used for measuring relationships between the each other technology layer and the product layer. Two types of association rules were identified by using the support and confidence. Support is measured between the two keyword affinity, which means "how close two keywords is connected". Confidence measures the dependencies between two keywords, which try to measure the occurring probability of some specific keyword when another keyword occurs. Therefore, the confidence can be regarded as the conditional probability of y given x, which is closely related to the dependences between two keywords. The confidence can be effectively used to measure the relationship between two keywords.

Based on the calculation of confidence, the relationship between keywords can be determined. The results of measuring association rules can be derived. Based on the matrices, the influence relation maps (IRMs) can be derived by using the DEMATEL. These maps are the prototypes of the technology maps which will further be confirmed in the future research project. Further, the keywords will be confirmed and the time frame will be added based on experts’ opinions.

Conclusions

The Moore's Law has successfully predicted that the number of devices that can be manufactured on a chip to double every 18 months. The coming end of Moore's Law in the next decade could be a strategic turning point for the SOC design industry. How the SOC design service firms can leverage the opportunities and develop strategic plans is very critical. In this work, a patent mining based roadmapping framework was proposed based on the DRSA and the DEMATEL. Technology roadmaps for VLSI, IC Design Automation, and SOC was derived. These roadmaps can serve as the basis for future plan of SOC design services as well as techniques.
Figure 1. Technology Roadmap on “IC Design Automation”. Figure 2. Technology Roadmap on “VLSI”. Figure 3. Technology Roadmap on “SOC”.

Acknowledgement
This research was financially supported by the MOST, Taiwan.

References
[1] The Economist. (2015, 2016). Beyond Moore's law. Available: http://www.economist.com/news/science-and-technology/21652051-even-after-moores-law-ends-chip-costs-could-still-halve-every-few-years-beyond
[2] K. Shuler. (2014). Moore’s Law is Dead: Long Live SoC Designers. Available: https://www.design-reuse.com/articles/36150/moore-s-law-is-dead-long-live-soc-designers.html

[3] B. Martin. (2014). Are We at an Inflection Point with Silicon Scaling and Homogeneous ICs? Available: http://semimd.com/blog/2014/10/15/are-we-at-an-inflection-point-with-silicon-scaling-and-homogeneous-ics/

[4] K. Morris. (2016, 2016/12/25). A New Era for EDA? What's Next After Moore’s Law. Available: http://eejournal.com/archives/articles/20160808-newera

[5] D. Çetindamar, R. Phaal, and D. Probert, Technology management: activities and tools. Palgrave Macmillan, 2016.

[6] R. Galvin, "Science roadmaps," Science, vol. 280, no. 5365, pp. 803-803, 1998.

[7] R. Galvin, "Roadmapping—a practitioner's update," Technological forecasting and social change, vol. 71, no. 1, pp. 101-103, 2004.

[8] R. Harring, "Motorola's use of the product technology roadmap," in The National Communication Forum, 1984, pp. 78-80.

[9] Y. Jeong and B. Yoon, "Development of patent roadmap based on technology roadmap by analyzing patterns of patent development," Technovation, vol. 39-40, pp. 37-52, 2015.

[10] R. N. Kostoff and R. R. Schaller, "Science and technology roadmaps," IEEE Transactions on engineering management, vol. 48, no. 2, pp. 132-143, 2001.

[11] M. M. Carvalho, A. Fleury, and A. P. Lopes, "An overview of the literature on technology roadmapping (TRM): Contributions and trends," Technological Forecasting and Social Change, vol. 80, no. 7, pp. 1418-1437, 2013.

[12] R. Phaal, C. J. Farrukh, and D. R. Probert, "Technology roadmapping—a planning framework for evolution and revolution," Technological forecasting and social change, vol. 71, no. 1-2, pp. 5-26, 2004.

[13] S. Lee and Y. Park, "Customization of technology roadmaps according to roadmapping purposes: Overall process and detailed modules," Technological Forecasting and Social Change, vol. 72, no. 5, pp. 567-583, 2005.

[14] S. Saad, T. Perera, N. N. Gindy, B. Cerit, and A. Hodgson, "Technology roadmapping for the next generation manufacturing enterprise," journal of manufacturing technology management, vol. 17, no. 4, pp. 404-416, 2006.

[15] J. H. Lee, H.-i. Kim, and R. Phaal, "An analysis of factors improving technology roadmap credibility: A communications theory assessment of roadmapping processes," Technological Forecasting and Social Change, vol. 79, no. 2, pp. 263-280, 2012.

[16] J. H. Lee, R. Phaal, and C. Lee, "An empirical analysis of the determinants of technology roadmap utilization," R&D Management, vol. 41, no. 5, pp. 485-508, 2011.

[17] E. I. R. M. Association and E. I. R. M. Association, "Technology Roadmapping: Delivering Business Vision," Working Group Reports, EIRMA, 1997.

[18] S. Lee, S. Lee, H. Seol, and Y. Park, "Using patent information for designing new product and technology: keyword based technology roadmapping," R&d Management, vol. 38, no. 2, pp. 169-188, 2008.