Z-domain modeling methodology for homodyne digital optical phase-locked loop

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Abstract Homodyne optical phase-locked loop (OPLL) is one kind of PLLs applied in optical field to achieve phase locking between two optical signals. Although there are already some software emulation and s-domain modeling methods studied for homodyne OPLL, few studies about z-domain model of OPLL are reported. For homodyne digital OPLL (DOPLL), the performance of homodyne DOPLL can be analyzed more accurately by z-domain model. So a z-domain modeling methodology for homodyne DOPLL is proposed in the letter. In the proposed methodology, optical related components and analog to digital converter (ADC) are treated as one group. Then with formula transformation, z-domain model for homodyne OPLL is built successfully. Finally, a case study is given, several simulations by z-domain model and Simulink behavioral model are made with the same design parameters. These simulation results agree very well and verify the correctness of z-domain model.

Keywords: homodyne digital optical phase-locked loop, z-domain, modeling methodology

Classification: Optical hardware (fiber optics, microwave photonics, optical interconnects, photonic signal processing, photonic integration and modules, optical sensing, etc.)

1. Introduction

Homodyne optical phase-locked loop is one kind of optical phase-locked loops (OPLLs) applied in optical field, such as coherent optical communications [1, 2, 3, 4, 5], resonant fiber optical gyroscopes (RFOG) [6, 7, 8, 9, 10], and so on. Via feedback technology, phase locking between input optical signal and local optical signal can be achieved by homodyne OPLL. Since the operation of homodyne OPLL is complicated, the performance of homodyne OPLL is usually analyzed by two methods which are software emulation and frequency domain modeling.

Software emulation is a dynamic simulation analytical method. VPI [11, 12, 13] and Simulink [14, 15, 16] are the examples of software emulation method. These software emulation tools construct homodyne OPLL behavioral model to emulate the operation of homodyne OPLL first, then make transient analysis for each node of homodyne OPLL. But the analysis results of software emulation rely on initial condition during emulation. For performance analysis of entire loop, test vectors of software emulation are numerous, and the complete procedures with software emulation are time-consuming.

On the other side, frequency domain modeling is a static analytical method which is based on signal processing theory of linear system. The most popular frequency domain modeling methods are s-domain modeling and z-domain modeling. Both of two frequency domain modelling methods are widely adopted in the research of PLL [17, 18, 19, 20, 21]. But traditional PLL frequency domain model can’t be employed directly in analyzing homodyne OPLL. The reason is the structure of homodyne OPLL is different from the structure of traditional PLL [22, 23, 24, 25]. Up to now, only s-domain modeling method of homodyne OPLL is reported [26, 27]. But for homodyne digital OPLL with digital loop filter, signals in digital loop filter are discrete type and not suitable to be modelled by s-domain modeling method.

In this letter, a z-domain modeling methodology for homodyne digital OPLL (DOPLL) is proposed. The biggest contribution in this letter is developing a z-domain model for optical related components. Although the signals in optical related components are continuous, the last output of optical related components is sampled by analog to digital converter (ADC) periodically. So we treat optical related components and ADC as one group which is called optical phase detector part in this letter. Furthermore, the digitalized signal by ADC is a cosine signal which is difficult to be modelled in z-domain. After transforming with a phase shift of π/2, the cosine signal is transformed to a sine signal. Then optical phase detector part can be regarded as a sine phase detector, and z-domain model for homodyne OPLL is built successfully. To the best of our knowledge, this is the first report to describe z-domain modeling methodology for homodyne DOPLL. After that, a design example is given, and the corresponding Simulink behavioral model of homodyne DOPLL is developed. Then the stability, the step response, and the transfer function of homodyne OPLL is analyzed by z-domain model and Simulink behavioral model. The good agreements between the corresponding simulation results which are obtained by z-domain model and Simulink behavioral model verify the correctness of the proposed z-domain modeling methodology.

The rest of the letter is organized as follows. Section 2 describes the structure and operation of homodyne DOPLL. Proposed z-domain modeling methodology of homodyne DOPLL is presented in Section 3. In Section 4, an example design of homodyne DOPLL is given, and correctness of

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z-domain model is verified. Finally, conclusion is provided in Section 5.

2. Structure and operation of homodyne DOPLL

Seen from Fig. 1, the structures of homodyne DOPLL can be divided into three main parts: optical phase detector part, loop filter part, and tunable laser part.

![Fig. 1 The structure diagram of homodyne DOPLL.](image)

Optical phase detector part includes 180° optical hybrid, photoelectric detector (PD) and ADC. 180° optical hybrid realizes the optical hybrid function of the lights which are emitted by master laser and slave laser, respectively. PD converts the output optical signal of 180° optical hybrid into electrical signal. The output signal of PD is a beat sine signal whose frequency and phase is related to the phase difference between master laser and slave laser. Then ADC converts analog beat signal to digital beat signal and sends the digitalized beat signal to loop filter part.

Loop filter part includes only one module which is loop filter (LF). Based on the output of ADC, LF generates digital control signal for tunable laser part.

Tunable laser part consist of digital to analog converter (DAC) and slave laser. DAC converts the digital control signal from LF into analog control voltage, and the frequency of slave laser is tuned by the output of DAC.

Based on the above parts, homodyne OPLL tries to decrease the phase difference between master laser and slave laser into a constant which is usually zero.

In DPLL, there are three clocks, which are sampling clock for ADC, system clock for LF, and conversion clock for DAC. To work correctly and stably, the three clocks in DPLL needs to synchronize with each other. It indicates that the highest frequency of the three clocks is integer times of the frequencies of the other two clocks. Then the phase differences among the three clocks are kept as zero or a constant.

3. Z-domain modeling of homodyne DOPLL

3.1 Analysis of optical phase detector part

Shown from Eq. (1) and Eq. (2), the beam of master laser is defined as \( E_S(t) \) and the beam of local slave laser is defined as \( E_{Lo}(t) \).

\[
E_S(t) = \sqrt{P_S} e^{j\theta_S(t)} \tag{1}
\]

\[
E_{Lo}(t) = \sqrt{P_{Lo}} e^{j\theta_{Lo}(t)} \tag{2}
\]

where \( P_S \) is the optical power of master laser, \( P_{Lo} \) is the optical power of local slave laser, \( \theta_S(t) \) is the phase of master laser, and \( \theta_{Lo}(t) \) is the phase of local slave laser.

180° optical hybrid receives the light emitted by master laser and slave laser, and outputs two beams \( E_1(t) \) and \( E_2(t) \). The beams \( E_1(t) \) and \( E_2(t) \) are described by Eq. (3) and Eq. (4), respectively.

\[
E_1(t) = \frac{1}{\sqrt{2}} (E_S(t) + E_{Lo}(t)) \tag{3}
\]

\[
E_2(t) = \frac{1}{\sqrt{2}} (E_S(t) - E_{Lo}(t)) \tag{4}
\]

Then \( E_1(t) \) and \( E_2(t) \) pass through PD to generate beat electric signal \( V(t) \). Shown in Eq. (5), the beat electric signal \( V(t) \) contains information about the phase difference between master laser and slave laser.

\[
V(t) = -2r \sqrt{P_S P_{Lo}} \cos(\theta_S(t) - \theta_{Lo}(t)) \tag{5}
\]

where \( r \) refers to photoelectric responsivity, and \( R \) refers to transimpedance.

\( \theta_S(t) \) and \( \theta_{Lo}(t) \) are defined as Eq. (6) and Eq. (7).

\[
\theta_S(t) = \omega_S t + \Phi_S \tag{6}
\]

\[
\theta_{Lo}(t) = \omega_{Lo} t + \Phi_{Lo} \tag{7}
\]

where \( \omega_S \) is the angular frequency of master laser, \( \omega_{Lo} \) is the angular frequency of local slave laser which is tuned by tunable laser part, \( \Phi_S \) is the initial phase of master laser, and \( \Phi_{Lo} \) is the initial phase of local slave laser.

Taking Eq. (6) and Eq. (7) into Eq. (5), Eq. (5) can be rewritten as Eq. (8).

\[
V(t) = -2r R \sqrt{P_S P_{Lo}} \cos(\theta_{BEAT}(t)) \tag{8}
\]

where \( \theta_{BEAT}(t) = (\omega_S - \omega_{Lo}) t + \Phi_S - \Phi_{Lo} \).

Seen from Eq. (8), the period of \( V(t) \) is inversely proportional to the frequency difference between master laser and slave laser.

Then given by Eq. (9), ADC samples \( V(t) \) periodically and generates the digitalized value \( D[T_{a,i} + t_{ADC}] \).

\[
D[T_{a,i} + t_{ADC}] = K_{ADC} V[T_{a,i}] = -K_d \cos(\theta_{BEAT}[T_{a,i}]) \tag{9}
\]

where \( T_{a,i} \) is the time when ADC samples and digitalizes \( V(t) \) for the \( i \)-th time, \( t_{ADC} \) is the digitalized latency for ADC, \( K_{ADC} \) is gain of ADC, \( K_d = 2r R \sqrt{P_S P_{Lo}} \).

In the following, the digitalized result of ADC is sent to LF directly. Based on the principle of locking process, LF is sensitive to the digitalized values of ADC, and is indifferent to the phase of the digitalized results. So Eq. (9) can be transformed to Eq. (10).

\[
D[T_{a,i} + t_{ADC}] = -K_d \cos(\theta_{BEAT}[T_{a,i}]) + \frac{\pi}{2} = K_d \sin(\theta_{BEAT}[T_{a,i}]) \tag{10}
\]

where \( \theta_{BEAT}[T_{a,i}] = \theta_{BEAT}[T_{a,i}] + \frac{\pi}{2} \).

From Eq. (10), it is seen that \( D[T_{a,i} + t_{ADC}] \) can be regarded as sine signal. So optical phase detector part can be seen as a sine phase detector.
When $\theta_{BEAT}[T_{a,i}]$ is very small and close to 0, $D[T_{a,i} + t_{ADC}]$ is approximated as Eq. (11).

$$D[T_{a,i} + t_{ADC}] \approx K_d \theta_{BEAT}[T_{a,i}]$$  \hspace{1cm} (11)

Seen from the above analysis, signals in 180° optical hybrid and photoelectric detector are continuous, the corresponding optical modules can not be modelled in z-domain independently. Fortunately, the output of optical phase detector part is sampled by ADC periodically. Then it is found that the optical phase detector part can be grouped together and modelled in z-domain. In addition, deduced from Eq. (11), the entire loop will try to track the phase $\theta_{BEAT}$, and keep a constant phase difference of $\pi/2$ with $\theta_{BEAT}$.

$$\theta_d(z) = \text{round}(\theta_{BEAT}(z); T)$$  \hspace{1cm} (12)

Based on Eq. (11), the z-domain model of optical phase detector part is shown in Fig. 2 and the z-domain transfer function is given by Eq. (12).

$$H_D(z) = \frac{D(z)}{\theta_{BEAT}(z)} = K_d z^{-a}$$  \hspace{1cm} (12)

where $a = \text{round}(t_{ADC}/T_a)$, $T_a$ is the discrete interval time for optical phase detector part. The function $\text{floor}(x)$ is rounding $x$ to the nearest integers towards minus infinity.

### 3.2 Analysis of loop filter

Usually, infinite impulse response (IIR) digital filter is chosen as loop filter for the advantages of easy realization and convenient adjustment. During implementation, the proportional gain $K_1$ and integral gain $K_2$ in digital filter are usually the power of 0.5 to simplify the calculation.

The difference equation of IIR digital filter is given by Eq. (13).

$$F[T_{f,j}] = F[T_{f,j-1}] + K_1 D[T_{f,j}] - K_1 D[T_{f,j-1}] + K_2 D[T_{f,j}]$$  \hspace{1cm} (13)

where $T_{f,j}$ is the $j$-th discrete interval time in loop filter.

The z-domain model of filter is shown in Fig. 3. The z-domain transfer function of filter is given by Eq. (14).

$$H_F(z) = \frac{F(z)}{D(z)} = \frac{K_1 + K_2 - K_1 z^{-1}}{1 - z^{-1}}$$  \hspace{1cm} (14)

### 3.3 Analysis of tunable laser part

At first, the output of loop filter $F[T_{d,k}]$ is converted to analog control voltage $U[T_{d,k}]$ by DAC. The difference equation for DAC is given by Eq. (15).

$$U[T_{d,k} + t_{ADC}] = K_{DAC} F[T_{d,k}]$$  \hspace{1cm} (15)

where $T_{d,k}$ is the $k$-th discrete interval time in tunable laser part, $t_{ADC}$ is the conversion latency for DAC. $K_{DAC}$ is the gain of DAC.

The relationship between the angular frequency of local slave laser $\omega_{Lo}[T_{d,k}]$ and control voltage $U[T_{d,k}]$ is defined as Eq. (16).

$$\omega_{Lo}[T_{d,k}] = \omega_0 + K_L U[T_{d,k}]$$  \hspace{1cm} (16)

where $\omega_0$ is free running angular frequency of local slave laser and $K_L$ is gain of slave laser.

Then the laser is tuned by the output of DAC, the phase of local slave laser can be written as follows:

$$\theta_{Lo}[T_{d,k+1}] = \theta_{Lo}[T_{d,k}] + \tau_d \omega_{Lo}[T_{d,k}]$$  \hspace{1cm} (17)

where $\tau_d$ is the discrete interval time for tunable laser part.

According to Eq. (17), the transfer function of tunable laser part can be obtained.

$$H_L(z) = \frac{\theta_{Lo}(z)}{F(z)} = \frac{K_{DAC} K_L T z^{1-\beta}}{1 - z^{-1}}$$  \hspace{1cm} (18)

where $\beta = \text{round}(t_{ADC}/T_d)$.

### 3.4 Z-domain modeling of homodyne DOPLL

In Eqs. (12), (14) and (18), the physical meanings of $z^{-1}$ indicates the discrete interval time for the corresponding part which can be different. But based on the operation of homodyne DOPPLL described in Section 2, it is a reasonable choice that the update rate of homodyne DOPPLL is determined by the slowest update rate among the update rates of optical phase detector part, loop filter part, and tunable laser part.

If the update rate of optical phase detector part is lower than that of loop filter part, loop filter samples every digitalized value by ADC more than one times. It costs a lot of unnecessary power and only increases the gain of loop filter. But the gain of loop filter can also be increased by increasing the loop parameters of loop filter. In another view, if the update rate of optical phase detector part is higher than the update rate of loop filter part, some of the digitalized values will be flushed before loop filter samples them. When the update rates of optical phase detector part and loop filter part are the same, it looks good that every digitalized value is sampled by loop filter correctly. Due to the similar reason, if the update rate of tunable laser part is the slowest, it’s a good tradeoff that choosing the update rate of tunable laser part as the update rate of DOPPLL system.

Therefore, we adopts the slowest update rate as the global update rate in DOPPLL. Then the open-loop transfer function
$O(z)$ is given by Eq. (19).

$$O(z) = H_P(z)H_F(z)H_L(z) = K_{loop} \frac{z^{-1}(\alpha + \beta)(K_1 + K_2 - K_1 z^{-1})}{(1 - z^{-1})^2}$$  \hspace{1cm} (19)

where $K_{loop} = K_L K_{DAC} K_{IF} T$. $z^{-1}$ indicates one delay element where the frequency of delay element is the slowest update rate in DOPLL, and $T$ is the reciprocal of DOPLL update rate.

4. Design example

In this section, a design example of z-domain modeling methodology for homodyne DOPLL is presented. Typical parameters for homodyne DOPLL are given in Table I. Here the type of ADC is ADC12DL3200 [28], and the type of DAC is EV12DS130xZP [29].

Following the development method of Simulink behavioral models [30], Simulink model of homodyne DOPLL is developed and shown in Fig. 4. The parameters chosen for the homodyne DOPLL simulation are listed in Table I.

4.1 Parameters and simulink model of homodyne DOPLL

The parameters for homodyne DOPLL are given in Table I. Here the type of ADC is ADC12DL3200 [28], and the type of DAC is EV12DS130xZP [29].

Following the development method of Simulink behavioral models [30], Simulink model of homodyne DOPLL is developed and shown in Fig. 4. The parameters chosen for the homodyne DOPLL simulation are listed in Table I.

### Table I  The parameters for homodyne DOPLL simulation

| Parameter                          | Quantity     |
|-----------------------------------|--------------|
| Initial frequency offset $\delta$ | 2MHz         |
| Master laser power $P_s$          | 0.65mW       |
| Slave laser power $P_{sl}$        | 0.65mW       |
| PD photoelectric responsivity $r$ | 0.9A/W       |
| PD Transimpedance $R$             | 16KΩ/A       |
| $K_{DAC}$                         | 2048V⁻¹      |
| $t_{ADC}$                         | 26 sampling cycles=1.5ns |
| LF coefficient $K_1$              | 1/16         |
| LF coefficient $K_2$              | 1/32         |
| $K_{DAC}$                         | 1/4096V      |
| $t_{DAC}$                         | 4 conversion cycles |
| Laser tuning coefficient $K_L$    | 50MHz/V      |
| Laser tuning bandwidth $B_L$      | 100MHz       |
| Sampling clock frequency $F_{sam}$| 3.20GHz      |
| System clock frequency $F_{sys}$  | 200MHz       |
| Conversion clock frequency $F_{con}$| 3GHz        |

Fig. 4  Simulink behavioral model of homodyne DOPLL

4.2 Z-domain model of homodyne DOPLL

From Table I, it is seen that laser tuning bandwidth $B_L$ is 100MHz. It indicates that the maximum update rate for tunable laser part is 100MHz. Due to the discussion in Section 3.4, the update rate for loop filter should be adjusted to 100MHz. Therefore, loop filter is modified to generate digital control signal at 100MHz, even if the frequency of system clock is 200MHz.

Meanwhile, the frequencies of sampling clock and conversion clock are both 200MHz. However, loop filter samples the output of ADC at 100MHz. The other values output by ADC are discarded. The input of DAC is the output of loop filter which is also updated at 100MHz. Therefore, 100MHz is the update rate for the whole DOPLL.

Moreover, the values of $t_{ADC}$ and $t_{DAC}$ depend on the number of clock cycles. Since the periods of sampling clock and conversion clock are short, the values of $t_{ADC}$ and $t_{DAC}$ are relatively very small which are given by Eq. (20).

$$\begin{align*}
t_{ADC} &= 9.6\text{ns} \\
t_{DAC} &= 1.3\text{ns}
\end{align*}$$  \hspace{1cm} (20)

Then $\alpha$ and $\beta$ are given by Eq. (21).

$$\begin{align*}
\alpha &= \text{round}(t_{ADC}/T) = 1 \\
\beta &= \text{round}(t_{DAC}/T) = 0
\end{align*}$$  \hspace{1cm} (21)

where $T$ is the reciprocal of update rate for the whole DOPLL, and the value of $T$ is 10ns here.

The closed-loop transfer function of homodyne DOPLL is given by Eq. (22).

$$H(z) = \frac{O(z)}{1 + O(z)} = \frac{K_{loop}(K_1 + K_2)z - K_{loop}K_1}{z^2 + [K_{loop}(K_1 + K_2) - 2]z + 1 - K_{loop}K_1}$$  \hspace{1cm} (22)

where the value of $K_{loop}$ is 2.26.

4.3 Stability analysis of homodyne DOPLL

The pole-zero plot is chosen to analyze the system stability of homodyne DOPLL.

As shown in Fig. 5, the z-domain model of homodyne DOPLL with selected gains can satisfy the system stability requirement.

The simulation result of feedback voltage $U(t)$ is presented in Fig. 6. The initial conditions of simulation are given in Table I. The frequency offset value of two lasers can be locked to zero. Therefore, the final feedback voltage $U(t)$ converges to 0.04V, which verifies the accuracy of the z-domain model of homodyne DOPLL.

4.4 $|H(f)|$ of homodyne DOPLL

The magnitude of $|H(f)|$ is given in Fig. 7. The red solid line represents the amplitude frequency response for homodyne DOPLL calculated in z-domain model. The blue dash-dot line shows the amplitude frequency response for homodyne DOPLL obtained by Simulink behavioral model.

The amplitude of output jitter signal is obtained by measuring the phase of slave master. When the jitter frequency is small, the homodyne DOPLL is in locked state and can be analyzed with z-domain model.
The letter proposes a z-domain modeling methodology for homodyne DOPLL and verified by Simulink behavioral model. Based on the proposed z-domain modeling methodology, the z-domain model for homodyne DOPLL can be developed easily. Then the z-domain model can be adopted to select the loop coefficients and analyze the performance of homodyne DOPLL rapidly and precisely. The z-domain modeling methodology can help designers to shorten design cycle and increase design efficiency.

Therefore, the two lines are more consistent with each other, which can verify the accuracy of z-domain model. When the jitter frequency is large, the homodyne DOPLL cannot be approximated as a linear system, and z-domain model is not suitable for performance analysis. So there is an obvious deviation between two lines.

5. Conclusion

The letter proposes a z-domain modeling methodology for homodyne DOPLL and verified by Simulink behavioral model. Based on the proposed z-domain modeling methodology, the z-domain model for homodyne DOPLL can be developed easily. Then the z-domain model can be adopted to select the loop coefficients and analyze the performance of homodyne DOPLL rapidly and precisely. The z-domain modeling methodology can help designers to shorten design cycle and increase design efficiency.

References

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[1] K. Balakier, et al.: “Integrated semiconductor laser optical phase lock loops,” IEEE J. Sel. Topics Quantum Electron. 24 (2018) 1 (DOI: 10.1109/JSTQE.2017.2711581).
[2] Y. Liu, et al.: “Design of a phase sensor applied in the optical phase-locked loop based on a high-speed coherent laser communication system,” IEEE Access 6 (2018) 22131 (DOI: 10.1109/ACCESS.2018.2828026).
[3] Y. Okamura, et al.: “Pump phase-locking to fiber-transmitted QPSK phase-conjugated twin waves for non-degenerate phase-sensitive amplifier repeaters,” IEICE Commun. Express 6 (2017) 566 (DOI: 10.1587/comex.2017XBL0098).
[4] H. Peng, et al.: “Laser phase noise measurement by using offset optical phase locked loop,” IEEE JIFS-IAF (2020) 1 (DOI: 10.1109/JIFS-IAF.2019.923483).
[5] L. Paillier, et al.: “Space-ground coherent optical links: ground receiver performance with adaptive optics and digital phase-locked loop,” J. Lightw. Technol. 38 (2020) 5716 (DOI: 10.1109/JL.T.2020.300356).
[6] E. Benser, et al.: “Development and evaluation of a navigation grade resonator fiber optic gyroscope,” IEEE ISS (2015) 1 (DOI: 10.1109/InertialSensors.2015.7314259).
[7] J. Wu, et al.: “Resonator fiber optic gyro with high backscatter-error suppression using two independent phase-locked lasers,” 24th International Conference on Optical Fibre Sensors 9634 (2015) 96341O (DOI: 10.1117/12.2195220).
[8] C. Zhang, et al.: “Free spectral range measurement using homologous heterodyne optical phase-locked loop based on acousto-optic modulation,” Applied Optics 58 (2019) 5817 (DOI: 10.1364/AO.58.005817).
[9] Y. Zhang, et al.: “Design of real-time free spectral range measurement based on HQLP technique,” IEEE Sensors J. 20 (2020) 10607 (DOI: 10.1109/JSEN.2020.2994001).
[10] G.A. Sanders, et al.: “Improvements to signal processing and component miniaturization of compact resonator fiber optic gyroscopes,” IEEE ISS (2018) 1 (DOI: 10.1109/InertialSensors.2018.8577190).
[11] J. Zhang, et al.: “Phase-modulated microwave-photonic link with optical-phase-locked-loop enhanced interferometric phase detection,” J. Lightw. Technol. 26 (2008) 2549 (DOI: 10.1109/JLT.2008.927593).
[12] L. Li, et al.: “Direct power control of DFSG system without phase-locked loop under unbalanced and harmonically distorted voltage,” IEEE Trans. Energy Convers. 33 (2017) 395 (DOI: 10.1109/TEC.2017.2741473).
[13] F.T. Pantano, et al.: “SILPLL based forced opto-electronic oscillator using a phase modulator in a Sagnac loop,” IEEE WiSNet (2018) 66 (DOI: 10.1109/WiSNet.2018.831156).
[14] D. Ding, et al.: “Stability, noise, and nonlinear distortion analysis of a sampling OPLL,” J. Lightw. Technol. 36 (2018) 2783 (DOI: 10.1109/JLT.2018.2820732).
[15] L. Xu, et al.: “ACP-OPLL performance in presence of out-of-band interference,” J. Lightw. Technol. 32 (2014) 2636 (DOI: 10.1109/JLT.2014.2331551).
[16] D. Ding, et al.: “Theoretical analysis on OPLL-based phase modulated RF photonic links,” Asia Communications and Photonics Conference (2020) M4A.344 (DOI: 10.1109/ACPC.2020.M4A.344).
[17] J.P. Hein and J.W. Scott: “z-domain model for discrete-time PLL’s,” IEEE Trans. Circuits Syst. 35 (1988) 1393 (DOI: 10.1109/31.144643).
[18] F.M. Gardner: Phaselock Techniques (John Wiley & Sons, 2005) 65.
[19] X. Chen, et al.: “A contribution to the discrete Z-domain analysis of ADPLL,” 2007 7th International Conference on ASIC (2007) 185 (DOI: 10.1109/ICASIC.2007.415598).
[20] R.E. Best: *Phase-locked Loops Design, Simulation and Application* (McGraw-Hill Press, 2003) 5th Ed. 166.

[21] N. Tripathi and S.N. Pradhan: “Design of power efficient all digital phase locked loop (ADPLL),” IEEE WiSPNET (2016) 778 (DOI: 10.1109/WiSPNET.2016.7566259).

[22] Z. Xu, et al.: “A digital optical phase-locked loop based on field programmable gate array and its applications,” IEEE International Conference on Information Science, Electronics and Electrical Engineering 2 (2014) 795 (DOI: 10.1109/InfoSCEE.2014.6947776).

[23] A. Fujii, et al.: “Stable QPSK demodulation using a digital optical phase-locked loop,” IEEE Photon. Technol. Lett. 26 (2014) 1847 (DOI: 10.1109/LPT.2014.2337888).

[24] L. Qing and Y. Pesla: “Analysis of stability of an optical phase-locked loop,” IEEE Region 10 International Conference on Computers, Communications and Automation 3 (1993) 474 (DOI: 10.1109/TENCON.1993.328027).

[25] D. Zaccarin, et al.: “Performance analysis of optical heterodyne PSK receivers in the presence of phase noise and adjacent channel interference,” J. Lightw. Technol. 8 (1990) 353 (DOI: 10.1109/50.50732).

[26] M. Grant, et al.: “The performance of optical phase-locked loops in the presence of nonnegligible loop propagation delay,” J. Lightw. Technol. 5 (1987) 592 (DOI: 10.1109/JLT.1987.1075532).

[27] M. Lu, et al.: “An integrated 40 Gbit/s optical costas receiver,” J. Lightw. Technol. 31 (2013) 2244 (DOI: 10.1109/JLT.2013.2265075).

[28] 12-bit, dual 3.2-GSPS or single 6.4-GSPS, RF-sampling analog-to-digital converter (LVDS interface), https://www.ti.com/product/ADC12DL3200.

[29] EV12DS130xZP, https://www.teledyne2v.com/products/semiconductors/dac/ev12ds130/.

[30] M. Firus and T.N.K. Hoan: “Wavelength re-generation and re-modulation using optical phase lock loop techniques for 100-Gb/s DQPSK up-stream transmission in DWDM passive optical networks,” Photonic Network Communications 19 (2010) 265 (DOI: 10.1007/s11107-009-0231-9).