Nonvolatile Resistive Switching in Nanocrystalline Molybdenum Disulfide with Ion-Based Plasticity

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Non-volatile resistive switching is demonstrated in memristors with nanocrystalline molybdenum disulfide (MoS₂) as the active material. The vertical heterostructures consist of silicon (Si), vertically aligned MoS₂, and chrome/gold metal electrodes. Electrical characterizations reveal a bipolar and forming-free switching process with stable retention for at least 2500 s. Controlled experiments carried out in ambient and vacuum conditions suggest that the observed resistive switching is based on hydroxyl ions (OH⁻). These originate from catalytic splitting of adsorbed water molecules by MoS₂. Experimental results in combination with analytical simulations further suggest that electric field driven movement of the mobile OH⁻ ions along the vertical MoS₂ layers influences the energy barrier at the Si/MoS₂ interface. The scalable and semiconductor production compatible device fabrication process used in this work offers the opportunity to integrate such memristors into existing Si technology for future neuromorphic applications. The observed ion-based plasticity may be exploited in ionic-electronic devices based on transition metal dichalcogenides and other 2D materials for memristive applications.

1. Introduction

Next-generation computing is strongly believed to be the way forward to accommodate the vastly growing demands on computing, storage, and communication.[3] Neuromorphic computing falls into this category and envisions the realization of artificial neural systems using electronic circuits to mimic the functioning of the human brain.[2–4] A neuromorphic computer, such is the hope, should be able to emulate the low power operation, highly efficient processing, and real-time complex multi-tasking (parallel information processing) capabilities of the brain.[5,6] Significant research efforts are directed toward imitating neural synaptic plasticity, which is a feature that enables the brain to learn and process new information.[7–11] Electronic devices that can mimic this feature even to a certain extent are becoming highly desirable. Memristors (memory resistors), which are two-terminal passive circuit elements, are seen as primary candidates owing to the reversible resistive switching (RS) behavior they exhibit.[12,13] Memristors typically consist of metal–insulator–metal (MIM) structures, in which the insulator acts as the RS medium. The RS media of conventional MIM memristors are often based on phase change materials[14,15] or transition metal oxides.[13,14,16–19] The latter form and retract conductive filaments (CF) to trigger the RS effect and often require high currents initially to form the filaments. Recently, 2D transition metal dichalcogenides (TMDs) have also been investigated for their potential use as an RS medium in memristor devices.[20–32] So far, mostly planar or lateral devices based on horizontally aligned TMD layers obtained either by mechanical exfoliation or by chemical vapor deposition have been studied. Molybdenum disulfide (MoS₂) is a prominent member of the 2D TMD family that is getting considerable attention on account of its interesting electronic properties, including a thickness-dependent band gap[33–35] and memristive behavior. The latter has so far been attributed to bias-induced migration of sulfur vacancies and grain boundaries in the case of single-layer MoS₂[20,23] and lattice distortion, reversible modulation of MoS₂ phases, and migration of oxygen ions in multilayers.[21,24,36] Also, very recently, low-power RS was demonstrated in “Au/bi-layer MoS₂/Cu” memristors and the effect was attributed to diffusion of Cu into MoS₂ to form a metallic conductive path.[37] Nevertheless, the origin and mechanism of the RS behavior of MoS₂ is still under debate.

Recently, we demonstrated the presence of hydroxyl (OH⁻) ions and their field-induced movement in vapor-phase grown MoS₂ with vertically aligned layers.[3,4] Here, we demonstrate...
the existence and investigate the origin of nonvolatile resistive switching in silicon (Si)/MoS$_2$/metal heterostructure devices, where MoS$_2$ with vertically aligned layers serves as the RS medium. In analogy to the conventional MIM configuration, we name the devices in this work semiconductor/semiconductor/metal (SSM) memristors. The OH$^-$ ion-mediated RS behavior is observed in vertically aligned MoS$_2$ layers in a vertical device architecture, which is preferred for practical applications due to its potential for ultimately small footprints.\[24\] The fabrication process used in this work is scalable and semiconductor manufacturing compatible and includes the growth of large-area MoS$_2$ directly on Si. This is an important aspect toward future integration of such devices with the existing Si-technology platform.

2. Results and Discussion

Raman spectroscopy studies conducted on the as-grown MoS$_2$ films confirm a 2H-MoS$_2$ phase formation. Figure 1a shows the acquired Raman spectrum with the two prominent peaks corresponding to the E$_{2g}^{1}$ and A$_{1g}$ modes of the 2H-MoS$_2$ phase.\[38\] The peak intensity of the A$_{1g}$ mode is nearly four times higher than that of E$_{2g}^{1}$, indicating the formation of vertically aligned MoS$_2$ layers.\[39,40\] The thickness of the as-grown films was measured using atomic force microscopy (AFM) technique and confirmed to be $\approx 15$ nm (Figure 1b). Transmission electron microscopy (TEM) was also employed to investigate the cross-section of the device structure. The cross-sectional TEM image in Figure 1c depicts a polycrystalline MoS$_2$ with predominantly vertical orientation of MoS$_2$ layers that are standing on the Si substrate. This is in agreement with the Raman studies where the vertical orientation of the layers is manifested by the large A$_{1g}$/E$_{2g}^{1}$ peak intensity ratio (Figure 1a). The TEM image also reveals a $\approx 2.5$ nm interfacial silicon oxide layer (IL) between Si and MoS$_2$ that has formed during the sulfurization process. The IL is very leaky compared to standard silicon dioxide (SiO$_2$) of similar thickness at comparable bias level\[41\] and is therefore nearly transparent to electrons under direct current (DC) bias. Hence, the charge carrier transfer between Si and MoS$_2$ is presumably unaffected by the presence of this layer. A schematic of the device structure is depicted in Figure 1d.

DC current–voltage (I–V) and current–time measurements were conducted on the SSM memristors in a Lakeshore cryogenic probe station using a Keithley 4200SCS parameter analyzer. The DC measurements were conducted in both ambient and vacuum conditions, at room temperature. Voltage was applied to the top electrode (V$_{TE}$) while keeping the Si grounded as illustrated in the wiring setup shown in the inset of Figure 2a. First, different DC sweep ranges were applied to determine the window of operation for RS. The switching effect in the negative bias regime becomes observable only for V$_{TE}$ $\leq$ –4 V and generally scales with the magnitude of the applied bias (Figure S1, Supporting Information). To avert potential device damage caused by voltage stress during measurements, further I–V measurements were limited to $\pm 5$ V. Figure 2a shows a representative I–V characteristics of the SSM memristors in ambient conditions. It exhibits a forming free and bipolar RS behavior, in which the resistance state is modulated between two resistance
levels, namely the high resistance state (HRS) and the low resistance state (LRS). Transition from the HRS to LRS (SET process) is observed in the negative bias regime, while the reverse transition from the LRS to HRS (RESET process) happens in the positive bias regime. This bipolar switching process is similar to valence change switching in transition metal oxides, albeit different underlying mechanisms apply. The I–V measurements were carried out in the following sequence. First, $V_{TE}$ was swept from 0 to $-5$ V (sweep 1), during which the onset of the SET process is observed at around $-4$ V. As a result, the device switches from the HRS to the LRS leading to the observed current increase. Next, $V_{TE}$ was swept from $-5$ V back to 0 V (sweep 2) during which the device remains in the LRS. Afterward, $V_{TE}$ was swept from 0 to $+5$ V (sweep 3) and finally back to 0 V (sweep 4). The device maintains the LRS during sweep 3, but it switches to the HRS during sweep 4. It is observed that the switching ratio of the RESET process is much smaller than that of the SET process. In addition to the observed hysteretic behavior, which is the main focus of this work, the I–V characteristics in Figure 2a also exhibit asymmetric behavior indicating that the charge carrier transport in the present devices is mainly determined by the interface transport. Zhu et al. have reported similar I–V characteristics, that is, a larger switching ratio in the SET than in the RESET regime for Au/Li$_2$MoS$_2$/Au lateral structures and have demonstrated RS phenomenon by field-induced migration of lithium ions (Li$^+$) in MoS$_2$ layers.

In the present devices, the observed RS effect can be explained by movement of OH$^-$ ions inside the layered MoS$_2$. The presence of OH$^-$ ions in MoS$_2$ have been experimentally observed in a previous study through time-of-flight secondary ion mass spectroscopy and electrical characterizations. There, it was also demonstrated that the OH$^-$ ions move presumably along the van der Waals gaps toward (away from) the Si/MoS$_2$ interface in response to a negative (positive) bias applied on the top electrode. These ions are expected to originate from water molecules that have been split by the catalytic effect of MoS$_2$ to water.$^{[43–45]}$ This is in line with other reports where the layered crystal structure of MoS$_2$ and the associated anisotropic electronic properties facilitate ion transport along the layers.$^{[28,46,47]}$

To visualize how the RS effect takes place in the present system, schematic band diagrams are provided in Figure 2b–e. The figure illustrates alignments of the bands during thermal equilibrium (Figure 2b), the SET process (Figure 2c), the RESET process (Figure 2d), and the READ (Figure 2e) conditions. For the present devices, this means that a negative $V_{TE}$ (SET) pushes the OH$^-$ ions toward the Si/MoS$_2$ interface and lowers the energy barrier at the interface compared to a situation where the ions are located farther away from the Si/MoS$_2$ interface. As a result, the devices switch to the LRS (red curve in Figure 3). On the other hand, the OH$^-$ ions move away from the Si/MoS$_2$ interface when a positive $V_{TE}$ is applied (RESET). Now, the MoS$_2$ band alignment results in a relatively higher interface barrier. Hence, the positive bias switches the device resistance to the HRS (black curve in Figure 3). During READ, the bands align in such a way that holes move from Si to MoS$_2$ overcoming the hole barrier at the Si/MoS$_2$ interface, while electrons move in the opposite direction. Due to the high barrier encountered by electrons at the chromium (Cr)/MoS$_2$ interface in this particular configuration (Figure 2e), the RS in the devices is dominated by hole transport, which in turn is controlled by the Si/MoS$_2$ hole barrier. The field-driven movement of the OH$^-$ ions thus tunes the energy barrier at the Si/MoS$_2$ interface and therefore controls the charge carrier transfer from Si to MoS$_2$. This in turn gives rise to modulation of the device’s resistance between LRS and HRS and hence the observed memristive behavior.

Non-volatility of RS, and in particular endurance and state-retention, are important figures of merit for device applicability. Endurance is a measure of how many times a memristor device can be switched between the LRS and HRS while maintaining a reasonable switching ratio.$^{[13,22]}$ State-retention...
is also commonly used to test if the resistance states are stable over a period of time, following the SET and RESET transitions. To achieve reliable results during endurance tests, determining the right programming time and program- ming voltages for the SET and RESET processes is very crucial and can only be done empirically. Initial experiments to this end can be found in Figure S2, Supporting Information. After obtaining appropriate measurement parameters, we carried out endurance tests for 140 manual DC switching cycles in ambient conditions. The endurance data was acquired by reading out the resistance values from the current levels at \(-1.5\) V immediately after applying the SET and RESET voltages of \(-3.5\) and \(+4\) V, respectively, for 2 s. Each READ was done immediately after a SET and RESET at programming voltages of \(-3.5\) and \(+4\) V, respectively, which were applied as step voltage signals held for 2 s. The results obtained are shown in Figure 3a, where a clear RS behavior is evident for 140 manual DC switching cycles. The endurance data exhibits a distinct resistance shift at the beginning. This may be attributed to an initial reduction of negative ions inside MoS\(_2\) due to their interaction with holes in the Si or to an initial redistribution of the ions from an equal distribution to a more concentrated (Gaussian) distribution during electric field stress. The data also show a less pronounced resistance drift in further cycles, which requires future investigation. As shown in Figure S3a,c, Supporting Information, similar drift characteristics were also observed in endurance measurements on other devices. Despite the general similarity, slight variations in the absolute resistance values among different devices are noticed. Such a cell-to-cell (spatial) variability is in fact a major challenge for RS devices in general, and it is believed to hinder their use for computing and memory applications. In 2D TMD memristors, this may be partially attributed to the lack...
of spatial homogeneity in the large area TMD films,[23] an issue that can be expected to be solved by further maturing the manufacturing technology.

State retention measurements were also performed in ambient atmosphere according to the following procedure. First, a SET voltage of $-4 \text{ V}$ was applied for 2 s to switch the device to the LRS, followed by 400 subsequent READ operations at $-1.5 \text{ V}$. Next, immediately after the 400th readout cycle in the LRS, a RESET voltage of $+4 \text{ V}$ was applied for 2 s to switch to the HRS. Then, another 400 subsequent READ operations were performed in the HRS. Figure 3b shows the resulting retention data demonstrating that the devices are able to retain the resistance states for at least 2500 s, albeit with a slight resistance shift in the LRS after 1900 s (after the 300th readout cycle). This shift appears to be random and is not fully understood. It may be due to a parasitic influence on the OH$^{-}$ ions during the READ phase, which can be addressed with a more suitable READ voltage in the future. Nevertheless, the overall stable state retention data suggests that the mobile OH$^{-}$ ions dictating the RS effect drift substantially only during the programming phases, and not during the READ phase.

We performed analytical simulations that take into account the position of the ions within the MoS$_2$ and found that it determines the electric field distribution in the structures. This in turn influences the MoS$_2$ band alignment with respect to Si and thereby the energy barriers at the Si/MoS$_2$ interface. Figure 3c illustrates an assumed Gaussian distribution of OH$^{-}$ ions in MoS$_2$ at randomly selected positions for three cases: i) starting position with no bias (blue), ii) a position shifted toward the Si/MoS$_2$ interface for negative bias (red), and iii) a position shifted away from the interface for positive bias (black). Calculations of the corresponding MoS$_2$ valence bands ($E_{\text{V}}$) demonstrate that the energy barrier at the Si/MoS$_2$ interface is modulated by the position of the OH$^{-}$ ions with respect to the interface (Figure 3d). This influences the charge carrier transfer from Si to MoS$_2$ and gives rise to different resistance states depending on the position of the mobile charges. The fundamentals and details behind the analytical calculations can be found in ref. [48].

We also investigated the influence of voltage sweep rates on the RS behavior and noticed an increase in the switching ratio and a decrease in the onset-voltage of the SET process for a decreasing sweep rate (Figure 4a). A similar observation was
reported by Ge et al., who attributed the decrease in SET voltage to an enhanced ionic diffusion as a result of the additional time that the slower sweep rate offers.\[24\]

Measurements in vacuum at 7 × 10^{-5} mbar were carried out to confirm the hypothesis that the driving force behind the RS phenomenon originates from catalytically split water adsorbates. The devices were kept in the vacuum chamber with active pumping for about 64 h prior to the measurements to ensure that water molecules were extracted efficiently. Figure 4b shows I–V characteristics measured in vacuum under the same biasing conditions as used in ambient. A device in vacuum exhibits very low switching ratios compared to ambient conditions (see Figure 2a). This is confirmed by endurance data in vacuum, which also shows a negligible difference between the HRS and LRS (Figure 4c). Similar trends were obtained from endurance tests carried out in vacuum conditions on other devices, as shown in Figure S3b,d, Supporting Information.

Finally, we conducted an experiment where endurance tests were carried out first in ambient, then in vacuum, and then again in ambient conditions on the same device. As results in Figure 4d–f show, the strong RS effect is restored in ambient condition after it disappeared in vacuum, affirming our initial premise. There exist very few experimental reports on RS of two-terminal MoS2 memristors with a vertical architecture in vacuum conditions. Sangwan et al. have reported gate-modulated RS in vacuum for single layer polycrystalline MoS2-based three-terminal memtransistors with a lateral architecture and have attributed the RS effect to migration of grain boundaries and sulfur vacancies.\[20,23\] The absence of considerable switching windows in our measurements under vacuum, however, rules out a dominating role of grain boundaries and sulfur vacancies in the RS. Kalita et al. have reported a volatile threshold switching effect in graphene/vertical MoS2/Ni structures that is reduced in vacuum. They attributed the effect to oxygen in ambient conditions,\[30\] different to the results and conclusions presented here.

3. Conclusion
Vertical Si/MoS2/Cr memristors with vertically aligned MoS2 layers grown directly on Si are fabricated using scalable and semiconductor production compatible processes. Non-volatile resistive switching behavior is demonstrated in these devices and the main origin of the phenomenon is investigated. DC I–V characterization results showed forming-free bipolar RS, in which the SET and RESET transitions are achieved at negative and positive biases, respectively. Endurance and state-retention tests performed on the devices demonstrate that the observed non-volatile RS behavior is quite stable over a period despite successive biasing. Comparison of measurements carried out in ambient and vacuum conditions provide plausible arguments that the observed RS effect is due to OH\(^{-}\) ions that stem from catalytic splitting of adsorbed water molecules, in agreement with previous findings.\[36\] Analytical simulations support experiments and suggest that the movement of such ions toward (away from) the Si/MoS2 interface in response to negative (positive) electric-fields dictates the observed RS behavior by tuning the energy barriers at the interface. The vertically aligned MoS2 layers on Si are favorable for vertical crossbar device architectures for memristive applications. Furthermore, the scalable fabrication processes employed in this work lays out a path for easy integration of novel 2D materials-based memristors with existing semiconductor technology.

4. Experimental Section
To fabricate the SSM heterostructure memristors, MoS2 films were grown directly on p-type Si (100) substrates through thermally assisted conversion of Mo thin films in sulfur atmosphere. Details of the MoS2 synthesis process are described in Supporting Information and in ref. [36]. After MoS2 growth, top electrodes were defined on the MoS2 films by employing a photolithography step followed by evaporation of a stack of 20 nm Cr and 120 nm gold (Au) and a lift-off process. Next, a Cr/Au metal back contact was formed on the Si substrates through evaporation. In the resultant SSM memristors, MoS2 with vertically aligned layers is sandwiched between Cr and Si. The complete fabrication process scheme and a top-view scanning electron microscope image are provided in Figure S4a,b, Supporting Information. The MoS2 phase formation in the as-grown films was confirmed using micro Raman spectroscopy at a laser wavelength of 532 nm using a WITec alpha 300R Raman system with a WITec apyron confocal Raman microscope and a UHTS 600 ultrahigh throughput spectrometer. AFM was used to measure the thickness of the as-grown films, while TEM was employed to investigate the cross-section of the device structure. Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements
The authors would like to thank Gregor Schulte (University of Siegen) for his help in depositing the initial molybdenum films and Prof. Joachim Mayer and Maximilian Kruth for TEM imaging. The authors also thank Dr. Daniel Neumeier (AMO GmbH) for fruitful discussions. Financial support from the European Commission and the German Ministry of Education and Research, BMBF (NEUROTEC, 16ES1134) is gratefully acknowledged. (Graphene Flagship, 785219, QUEFORMAL, 829035).

Conflict of Interest
The authors declare no conflict of interest.

Keywords
2D materials, ion transport, memristors, molybdenum disulfide, non-volatile resistive switching

Received: August 20, 2019
Revised: November 13, 2019
Published online: January 14, 2020

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