TensorFlow Doing HPC

An Evaluation of TensorFlow Performance in HPC Applications

Steven W. D. Chien¹, Stefano Markidis¹, Vyacheslav Olshevsky¹, Yaroslav Bulatov², Erwin Laure³, Jeffrey S. Vetter³
¹ KTH Royal Institute of Technology, Stockholm, Sweden
² South Park Commons, San Francisco, USA
³ Oak Ridge National Laboratory, Oak Ridge, USA

Abstract

TensorFlow is a popular emerging open-source programming framework supporting the execution of distributed applications on heterogeneous hardware. While TensorFlow has been initially designed for developing Machine Learning (ML) applications, in fact TensorFlow aims at supporting the development of a much broader range of application kinds that are outside the ML domain and can possibly include HPC applications. However, very few experiments have been conducted to evaluate TensorFlow performance when running HPC workloads on supercomputers. This work addresses this lack by designing four traditional HPC benchmark applications: STREAM, matrix-matrix multiply, Conjugate Gradient (CG) solver and Fast Fourier Transform (FFT). We analyze their performance on two supercomputers with accelerators and evaluate the potential of TensorFlow for developing HPC applications. Our tests show that TensorFlow can fully take advantage of high performance networks and accelerators on supercomputers. Running our TensorFlow STREAM benchmark, we obtain over 50% of theoretical communication bandwidth on our testing platform. We find an approximately $2 \times$, $1.7 \times$ and $1.8 \times$ performance improvement when increasing the number of GPUs from two to four in the matrix-matrix multiply, CG and FFT applications respectively. All our performance results demonstrate that TensorFlow has high potential of emerging also as HPC programming framework for heterogeneous supercomputers.

Index Terms

TensorFlow, Emerging Programming Environments, Parallel Computing, Heterogeneous Supercomputers, HPC Applications

I. INTRODUCTION

TensorFlow is a fast growing open-source programming framework for numerical computation on distributed systems with accelerators. It was originally developed by Google and made open-source in November 2015. Since then, TensorFlow grew at a considerable pace counting on the work of thousands of active developers spreading across the world. In 2017, the TensorFlow code repository recorded more than a thousand commits per month, making it one of the fastest growing open-source software projects.

TensorFlow lowers the difficulty of programming accelerators in distributed environments by avoiding HPC low-level programming interfaces, such as CUDA, OpenCL and MPI. These concepts are essential for programming any HPC application. As such, TensorFlow enables the use of cloud systems with accelerators, such as Volta GPUs [1], TPUs [2] and current preexascale supercomputers, such as Summit and Sierra supercomputers, easily accessible and usable.

While TensorFlow was originally designed after Google’s DistBelief [3] for solving Machine Learning (ML) problems, the ultimate goal of TensorFlow is to solve a much broader range of numerical problems. In fact, the TensorFlow code repository webpage states “TensorFlow is an open source software library for numerical computation”. However, few examples of how to use TensorFlow for solving generic numerical problem on HPC systems exist, making it difficult to evaluate the impact of TensorFlow framework outside of the ML domain. In addition, TensorFlow is mostly deployed on local workstations or on the cloud, thus few performance data of TensorFlow running on supercomputers exist. This work aims to fill this gap by designing and developing a set of HPC applications and measuring their performance on supercomputers with accelerators.

Motivated to understand the overall impact of TensorFlow in HPC field, we design and implement four main benchmarks and computational kernels which are widely used by the HPC community: STREAM, matrix-matrix multiply, a Conjugate Gradient (CG) linear solver and Fast Fourier Transform (FFT). In the formulation of such algorithms, we follow a "data-driven" approach similar to that of a ML pipeline, where we tile the input matrices or arrays in smaller tiles and offload calculation to accelerator using the distributed TensorFlow. We develop a TensorFlow adaptor for the Slurm resource manager [4] to easily deploy TensorFlow applications on supercomputers. In addition, we run scaling and performance tests of our HPC applications on two supercomputers with GPUs. Our main contributions are to show that i) By using TensorFlow, application developers can easily develop parallel applications capable of using supercomputers with GPUs without having to deal with MPI, CUDA or OpenCL. ii) TensorFlow applications, designed to follow a “data-driven” approach, show relatively good performance and scaling as the number GPUs increases. Overall, we show that potential of TensorFlow uptake by the HPC community is high, especially when considering the current difficulty of programming large supercomputers with accelerators.

The paper is organized as follows. We first provide an overview of the TensorFlow programming environment, focusing on HPC aspects in Section [1]. We follow by describing how to deploy a TensorFlow application on supercomputers in Section [III] and present the HPC applications using TensorFlow in Section [IV]. The experimental set-up is described in Section [V] and we
present the performance results in Section VI. We describe previous and related work on TensorFlow programming environment and other ML frameworks in Section VII and finally summarize and discuss the results, outlining future work in Section VIII.

II. AN OVERVIEW OF TENSORFLOW

TensorFlow’s name is inspired by the idea of tensors propagating through computation graph. As stated in the GitHub TensorFlow repository, in a data flow graph, “the graph nodes represent mathematical operations, while the graph edges represent the multidimensional data arrays (tensors) that flow between them”. All data in TensorFlow are represented as n-rank tensors that are in practice n-dimensional arrays of basic data-types: a 0 dimensional tensor represents a scalar, a one-dimensional tensor represents a vector, a two-dimensional tensor represents a matrix and higher dimension tensors corresponds to higher dimension matrices. Tensor in TensorFlow has two properties: data type and shape which correspond to the number of dimensions and size for each dimension. All kinds of Tensors in TensorFlow, such tf.placeholder, tf.constant and tf.SparseTensor, are immutable with the exception of tf.Variable.

TensorFlow uses dataflow computing paradigm: computation of tensors is expressed in terms of the dependencies between individual operations [5]. In TensorFlow, a dataflow graph is first defined, then the dataflow graph or parts of the graph are executed across a number of local and remote devices through a TensorFlow session. The major advantages of using dataflow computing in HPC context are:

- With dependencies between operations known before running the DAG, TensorFlow can identify operations that can execute in parallel.
- TensorFlow uses information of dataflow between operations to perform parallelization.
- TensorFlow can use information of the dataflow graph to optimize execution, for instance merging subsequent operations to avoid data movement.

In addition, the use of dataflow graph allows portability because dataflow graph is a language-independent representation of the program. For instance, the graph can be constructed through one language binding, e.g. in Python, and be reopened later in a C++ code.

The current version of TensorFlow uses a deferred execution model (called Graph mode in TensorFlow) where the graph is constructed and operations are subsequently executed as soon as a TensorFlow Session is instantiated and executed. We note that TensorFlow also supports eager execution that follows an imperative style and it will likely become the default execution mode in future releases of TensorFlow.

Operations on a computation graph can be deployed through manual or automatic pinning with tf.device(). At the moment, the two available device types are cpu and gpu. Support for other devices can be implemented through designing a respective computation kernel and a wrapper API. If no device is specified, a simple device placement is used: if an operation supports both CPU and GPU execution, GPU devices will be chosen. In case when multiple GPUs are available, the first GPU will be chosen. Another approach is soft device placement. When an operation is pinned to a device with no supporting computation kernel, it can be automatically pinned to another device with a supporting kernel instead. In a heterogeneous environment with two GPUs, one CPU and no device specification, a matrix multiplication tf.matmul() will be pinned to the first GPU (GPU with device number zero).
Listing 1. Computing a matrix multiplication where A and B are generated in CPU while multiplication is done on GPU

```python
import tensorflow as tf
g = tf.get_default_graph()
with g.as_default():
    with tf.device('/cpu:0'):
        a = tf.random_uniform(shape=[3, 3],
                              dtype=tf.float32)
        b = tf.random_uniform(shape=[3, 3],
                              dtype=tf.float32)
    with tf.device('/gpu:0'):
        c = tf.matmul(a, b)

with tf.Session(graph=g) as sess:
    ret_c = sess.run(c)
```

Listing 1 illustrates an example of a matrix multiplication where two random matrices are generated on a CPU while the multiplication is performed on GPU. The code snippet generates a graph similar to that of in Fig. 1. Data movement between host and GPU memory is automatically handled and scheduled by the runtime without the user needing to handle any allocation.

A. Distributed Model

Before developing a TensorFlow distributed application, it is important to master few TensorFlow concepts, such as TensorFlow server, cluster, tasks and jobs, and to have it clear that TensorFlow uses a Remote Procedure Call (RPC) service-client model.

To run TensorFlow in a distributed environment, we need first to set-up a TensorFlow cluster. A TensorFlow cluster consists of multiple TensorFlow servers, also called tasks. A TensorFlow job is a named set of tasks that have common function. Typically, two kinds of jobs are defined: the parameter server or `ps` jobs host nodes that store and update variables; worker jobs are responsible for compute-intensive tasks and host stateless variables.

Listing 2. A TensorFlow Cluster specification that comprise of two jobs: parameter server and workers. Each job has a list of addresses and port numbers to TensorFlow servers.

```python
cluster = tf.train.ClusterSpec({
    'ps': ['t01n01:8888'],
    'worker': ['t01n02:8888', 't01n03:8888']
})
```

The Cluster is set-up by using a cluster specification, defining jobs and tasks. Listing 2 shows how cluster specification comprising two jobs with one and two tasks respectively looks like. A dictionary of jobs is specified in a cluster specification and each job consists of a list of addresses and port numbers to TensorFlow servers that are responsible for that particular task.

A `tf.train.Server` object then needs to be created with the cluster specification as an argument so that communications to other servers can be established. TensorFlow allows more than one task to be launched per node. If the servers use different GPUs in a node, we need to ensure that the respective GPUs are exposed. This can be done through configuring CUDA environment variable. If more than one server are using one GPU, we need to ensure that the two tasks share the GPU memory. In fact, by default each TensorFlow instance takes all the GPU memory. For this reason, configurations on how memory is allocated will need to be explicitly specified in this case.

The RPC service-client model is a popular model to design data-driven applications [6]. RPC is simple and usually platform and language independent. RPC protocols are typically designed on top of message passing systems. In TensorFlow, the Google RPC library [1] is used. gRPC is a library that provides language independent RPC service between clients and server. It uses Protocol Buffers [2] as underlying message serialization and exchange. ProtoBuf is a language and platform independent serializable data structure developed by Google. Apart from communication, it is widely used by TensorFlow such as for representation and serialization of dataflow graph.

TensorFlow supports two parallelism models:

- **Model Parallelism**: The computational graph is split across different devices such as in Fig. 1
- **Data Parallelism**: A graph is replicated for each task and they individually execute their own graph. According to computation results they update parameters on the parameter server. In each computational step, each task fetches different data for computation.

In this work, we focus on data parallelism, where each task individually executes a graph with different data source. The two main ways of handling data movement is through the Dataset API, where data are loaded, pre-processed and prefetched as tensors through an input pipeline such that data is ready for immediate consumption [7], another method is based on the Queue API, where tasks can push tensors into or extract tensors from a shared queue.

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1. https://grpc.io
2. https://developers.google.com/protocol-buffers/docs/overview
APIs (Python, C, C++, Java, Haskell, Go, Rust)

Distributed Runtime (C++)

Tools (tfdbg, Timeline)

Network
- gRPC
- RDMA
- MPI

File Systems
- POSIX
- gCloud
- AWS

Device Layer (GPU, CPU)

Kernel Implementations (MatMul, Conv, ...)

Fig. 2. TensorFlow software stack, adapted from Ref. [8].

Fig. 3. Execution TensorFlow Timeline of a particular stage of our CG solver. The individual time lines of a device show parallel execution of models.

B. The TensorFlow Programming Environment

One of the main strengths of TensorFlow software framework is that it combines high-level APIs with a lower level distributed C++ runtime system. TensorFlow’s software stack is illustrated in Fig. 2. It provides a set of high level APIs, below which, is supported by a runtime written in C++. The runtime uses different low level modules, such as device execution kernels, file I/O and network communication modules to support execution. To build a graph, a client program executes different operation construction APIs provided by the TensorFlow API. It finally establishes a session to their own server to run the graph. While TensorFlow provides a variety of APIs, among which C, Java, Haskell, Go and Rust APIs, the most used API is the Python API since it has complete support for all the functionalities and can be combined with other Python modules for numerical computation, such as Numpy and scikit-learn. As most of the TensorFlow users, we also use the Python API in this work.

The C++ runtime is the core of TensorFlow and provides HPC implementations for handling communication across the network, operations on accelerators, and I/O to the devices. Particularly important for HPC, apart from gRPC, TensorFlow supports the use of InfiniBand Verbs RDMA which was contributed by Yahoo; and MPI for data transfer. When these protocols are used, gRPC is typically still responsible for administrative purposes such as to establish initial connections.

One feature that might be of interest to HPC application users is its ability to take checkpoints and restart from an execution state. When a snapshot is taken, the graph structure, checkpoint identification and actual data stored in variables are recorded and stored as files [7]. Computation can be restarted later by restoring the graph structure and data stored in graph variables. Snapshot taking and restoration can be controlled through the TensorFlow API.

TensorFlow provides developers tools to perform runtime performance analysis. One example is TensorFlow Timeline. During session execution, session run metadata which consists of information on such as CUDA stream, and graph execution statistics are collected and can be visualized in form of a time line. Fig. 3 shows an example of a time line analysis of an execution of our CG solver application. tfdbg is an interactive debugger which gives a command line interface and is mainly for runtime debugging inside a computation graph. With tfdbg it is possible to inspect contents of tensors and computation during execution.
One current limitation of running distributed TensorFlow on HPC systems is the lack of integration of TensorFlow and job schedulers, such as Slurm on the systems. TensorFlow introduces “Cluster Resolver” that is responsible for fetching job and computing node configurations thus allow easy launching of tasks. Resolvers for launching job on TPUs and Google Cloud Service are already provided. In this work, we have developed a TensorFlow Resolver to automatically specify TensorFlow Cluster specifications and for launching tasks on a supercomputer.

Jobs in HPC systems are commonly managed by workload managers such as Slurm through a batch queuing system and the computing nodes allocated are not known in advance. In addition, these computing nodes are not directly accessible to end-users. Launching and placement of tasks are handled by the workload manager. For this reason, we extended the tf.contrib.cluster_resolver module to support cluster specification resolution for jobs launched by Slurm. tf.contrib.cluster_resolver is an object that automatically generates a cluster specification with given parameters. Our implementation supports homogeneous job allocation with default Slurm plane distribution. The object is created by specifying a list of jobs, number of tasks on each node and how GPUs on nodes are allocated to tasks. The Resolver reads a list of hosts through Slurm’s scontrol command and determine how jobs and tasks will be distributed. GPUs will also be exposed automatically to processes in case multiple TensorFlow instances are running on the same node.

IV. FROM ML TO HPC APPLICATIONS

TensorFlow has been designed with ML data-driven workloads in mind. In typical ML frameworks, data, such as images, are ingested at a fast pace. Data is preprocessed via an input pipeline on host device and moved to accelerator memory where computation is performed. Finally, parameters are updated according to results of computation. With training data-driven ML workloads, the amount of data being moved to the GPU is typically large, thus performance is often limited by communication bandwidth.

To achieve high-performance with TensorFlow on supercomputers, HPC application algorithms need to be reformulated as data-driven problem. We choose to design and implement four main applications which are widely used in the HPC applications. When developing our applications in TensorFlow, we also use additional modules, such as Numpy, for merging and other auxiliary operations.

A TensorFlow STREAM. STREAM is among the most famous HPC benchmarks. It measures the sustained bandwidth to memory systems. We implement a STREAM [9] like application to study the communication performance between two GPUs, also CPUs located on two computing nodes. We create a simple TensorFlow cluster with two tasks, a parameter server and a worker on the two nodes. A vector of floating point numbers with a specified size is created on each GPU belonging to the two computing nodes. We create an assign add operation which pushes the vector located on the GPU of the worker to parameter server and performs addition with the vector located on the GPU of parameter server. The application supports the use of gRPC, MPI and InfiniBand Verbs as underlying transfer protocol. To measure the estimated cost of transfer, we open a session to the worker and invoke the assign add operation through the session. Time used for invoking the operation can be conceived as the estimated cost of transfer between the two devices. When invoking an operation through a session, TensorFlow automatically returns the evaluated value from the graph in form of a Numpy array. In the case of bandwidth measure, this means additional data transfer. For this reason, we explicitly specify not to have the evaluated value returned to the Python session.

Tiled Matrix Multiplication. We implement matrix-matrix multiplication of large matrices similar to that in Fig. 4. With “large”, we mean that the whole matrices cannot be stored in the memory of one GPU. We reformulate computation similar to that of a ML training pipeline. To parallelize computation, we use a standard technique used in GPU programming, called tiled matrix-matrix multiply: two large matrices are divided into equally sized tiles. These tiles are stored and loaded as Numpy arrays. We create a dataset which gives a list of indexes of tiles to be multiplied and their resulting index. The list is shared by workers and they individually load these tiles from files. These tiles are loaded to GPU memory and multiplication is performed. The resulting tile is pushed into a First-In-First-Out queue of a reducer. The reducers extract these tiles and locally accumulate them to their respective targets. The algorithm is embarrassingly parallel and resembles a map-reduce paradigm, where tiles are multiplied and sent to the respective queues (map) and finally accumulated and stored by reducers (reduce). Furthermore, the input pipeline resembles a typical ML training data input pipeline, where samples (tiles) are loaded and sent through a computation pipeline (matrix multiplication) on GPU. In our implementation all computations are performed in single precision (32-bit).

Conjugate Gradient Linear Solver. Linear solvers are widely used to solve Partial Differential Equations (PDE) that arise in engineering, physics and chemistry problem. CG is an iterative linear solver for semi-definite positive matrices. The parallelizable elements in the algorithm include matrix vector multiplication and dot product. Matrix vector multiplication can be independently computed by horizontally splitting the matrix and distributing to worker such that each workers are responsible for one part of the multiplication. For example, a \(8192 \times 8192\) matrix can be split into \(2048 \times 8192\) blocks for four workers such that they can compute a share of the result vector. The final result can be obtained by merging the vectors. A dot product of two vectors can be computed in parallel by distributing subset of vectors to workers. Workers compute their
Fig. 4. A simplified illustration of tiled matrix multiplication application. Blocks of two matrices to be multiplied are fetched into a dataset with an index of which tile the multiplication result should be accumulated to. Workers continuously obtain tiles from dataset, perform matrix multiplication of the tiles and push results to one or more queues with the target index. One or more reducers executed inside the session on the reduce job: collecting multiplication results from its respective queue and accumulate to the respective Numpy array.

Fig. 5. A simplified illustration of data-driven reduction workflow between workers in the CG application. Workers participate in a reduction by sending their respective values into the incoming queue of a reducer, then wait to dequeue from the outgoing queue. The reducer extracts values from the incoming queue and performs requested operation. The reduced value is distributed to workers through the outgoing queue. A number of copies equivalent to the total number of workers will be pushed into the queue. Each worker which is waiting to dequeue obtains a copy of the reduced value and proceeds with own execution.

share of dot product and the final result can be obtained by summing all the partial dot products. Our approach of expressing the algorithm resembles similarities to what was presented in Ref. [10], where the algorithm is presented as a dependency specified dataflow graph for FPGAs.

One limitation of TensorFlow is that computation graphs, which are represented as ProtoBuf, cannot exceed two gigabyte in size. This imposes significant limitation to problem size. This can be overcome by creating uninitialized variables and explicitly update them inside a session through dictionary feeding. For example, one can represent the results of calculation of a loop as a single unrolled TensorFlow graph. However, this can exceed the two gigabyte limitation on the size of computation graph. Instead, one can represent only the body of the loop as the computation graph, and use TensorFlow persistent storage (tf.Variable) to keep the state between iterations. For this reason, we introduce data locality by loading and storing tiles from a matrix directly to workers to be reused every iteration.

We reformulate the synchronization and reduction steps with data-driven approach. When performing distributed synchronous learning, TensorFlow provides a SyncReplicasOptimizer where updates to a variable will be collected from workers and averaged before being applied. It uses a token queue as an implicit barrier and distributes updated step counters to worker after variable updates by populating a queue, where workers dequeue from. We follow this approach and implement a reducer where workers push updates to the reducer through a queue and extract the reduced value from the reducer through another queue. As illustrated in Fig. 5 two queues are created for each reduction step in the algorithm: one for workers sending in partial values for reduction operation and the second for distributing reduced value back to workers.

For example, each worker individually computes intermediate values and pushes them into the incoming queue of reducer and enters a blocking wait for output queue. The reducer collects all scalars being sent by the workers, performs computation and populates an outgoing queue with the updated scalar. Workers extract the updated scalar and proceed to next stage of computation. In that sense, data are driven continuously between workers and reducers. Our solver performs computation in double precision (64-bit).
Fast Fourier Transform (FFT). FFT is the algorithm for performing Fourier transform on a discrete signal of size \( N \) in \( O(N \log(N)) \) operations. FFT is a key algorithm for computational physics that is widely used in signal processing, spectral analysis and for solving PDEs. We implement the Cooley-Tukey 1D FFT algorithm as illustrated in Fig. 6 where a vector is split into interleaving smaller chunks and FFT is performed over each chunk, and later merged. As in the matrix multiplication algorithm, these tiles with interleaving elements are stored in files and are loaded individually by workers which are responsible for their share of work. They perform a 1D FFT on those vectors and push the index and result to the merger’s queue. The merger extracts the tiles and puts them back in place to the original vector. Once all the small vectors are collected, it computes twiddle-factors and performs merging locally with Python. We implement the solver in complex double precision (128-bit).

V. EXPERIMENTAL ENVIRONMENT

TensorFlow has been specifically designed to run on distributed systems with GPUs. For this reason, we run our applications on two supercomputers, both equipped with GPUs:

- **Tegner** is a GPU cluster. Each node has two Intel E5-2690v3 Haswell processors with 512 GB of RAM. Depending on the node used each node has either one NVIDIA Quadro K420 or one K80 GPU through PCI-E. They provide 1GB and 24GB of RAM respectively. In case of K80, each card contains two GK210 GPU engines with 12 GB of RAM. The parallel file system in use is Lustre and operating system is CentOS 7.4.1708. The nodes are connected by EDR InfiniBand network. We compiled TensorFlow 1.11 with support of Python 3.6, NVIDIA CUDA, OpenMPI and InfiniBand. The versions in use are CUDA 9.1, cuDNN 7.0.5, OpenMPI 3.0 and the compiler used is GCC 6.2.0.

- **Kebnekaise** is another GPU cluster. Each node has two Intel Xeon E5-2690v4 processors with 128 GB of RAM. There are two types of GPU nodes: K80 nodes or V100 nodes through PCI-E. Each K80 node has either two to four Nvidia K80 GPUs each containing two GK210 GPU engines with 12 GB of RAM or two NVIDIA V100 GPUs with 16GB of RAM. Each V100 node has two Nvidia V100 GPUs with 16 GB of RAM. The GPUs are connected through PCI-E. The operating system is Ubuntu Xenial (16.04 LTS). The nodes are connected by FDR InfiniBand network. We compiled TensorFlow 1.11 with support of Python 3.6, CUDA, OpenMPI and InfiniBand. The versions in use are CUDA 9.2.88, cuDNN 7.1.4.18 and OpenMPI 3.1.1. All tests are executed with distributed TensorFlow with InfiniBand verbs enabled. The compiler used is GCC 7.3.0.

On Tegner, we use both nodes that contain K420 and K80 GPUs. For nodes with K420, we run one instance of TensorFlow; for nodes with K80, we run two instances of TensorFlow per node and expose one GPU engine for each instance. On Kebnekaise, we use nodes that contain two K80s and V100. For K80 nodes, we run four instances of TensorFlow per node and expose one engine to each instance; similarly, for nodes with V100, we run two instances of TensorFlow per node and exposes one GPU for each instance. The number of processes running on each node is summarized in Table I. We also show the available memory of the GPU hosted on the node. We note that in subsequent text when we refer to K80 GPU, we refer to one GK210 GPU engine.
TABLE I

NUMBER OF INSTANCE OF TENSORFLOW per node for different type of nodes in our testing platforms.

| Type of Node   | GPU Memory | No. processes per node |
|----------------|------------|-------------------------|
| Tegner K420    | 1GB        | 1                       |
| Tegner K80     | 12GB ×2    | 2                       |
| Kebnekaise K80 | 12GB ×2    | 4                       |
| Kebnekaise V100| 16GB       | 2                       |

Fig. 7. Communication performance in MB/s between two computing nodes on Tegner and Kebnekaise.

For each experiment, we repeat the test from five to 10 times and report the median result. We observe a minimal performance variability in all the performance tests, except for matrix-multiply on Kebnekaise K80 and FFT on Tegner with two GPUs. The applications used in this paper are hosted in a code repository[^3].

VI. RESULTS

The goal of this work is to evaluate the potential and scalability of distributed TensorFlow for traditional HPC applications running on supercomputers with GPUs. We present the performance evaluation of the applications we designed and developed.

A. STREAM Benchmark

High performance interconnect is an important component of HPC system which supports synergy of parallel applications. Our testing shows that TensorFlow’s RDMA module can take advantage of these infrastructures to transfer tensors residing on computing nodes. We evaluate communication performance with our STREAM micro-benchmark tool for three protocols: MPI, InfiniBand Verbs (RDMA) and gRPC. In each test, we invoke communication 100 times to create a stream of transfer and report average MB/s. We vary transfer size from two to 128 MB. We perform the tests with K420 nodes on Tegner and K80 nodes on Kebnekaise. On Tegner we test for when tensors reside in host and GPU memories. We specifically note that we use the default transfer configuration by TensorFlow MPI module for the tests with MPI. It means that instead of performing direct transfer of data to and from GPUs, tensors are first copied and serialized to host memory before transfer. This is due to that GPU Direct is not supported on our testing platforms.

Our results suggest that RDMA provides the best communication performance and we record peak bandwidth of over 6 GB/s on Tegner when tensors are placed in CPU host memory. The theoretical bandwidth on Tenger is 12 GB/s, which represents more than 50% of bandwidth utilization. Fig. 7 shows the estimated communication performance in MB/s on Tegner and

[^3]: https://github.com/steven-chien/tensorflow-solvers.git
Fig. 8. Performance of tiled matrix multiplication with different GPUs on Tegner and Kebnekaise in Gflops/s for different problem sizes.

Kebnekaise. When using RDMA, bandwidth saturates at approximately 1300 MB/s on Tegner where tensors are hosted on K420 GPUs; on Kebnekaise, bandwidth saturates at below 2300 MB/s where tensors are hosted on K80 GPUs.

When communicating through MPI, bandwidth is less satisfactory. We measure approximately 318 MB/s on Tegner when tensors are hosted on K420 GPUs and MPI is used for communication; on Kebnekaise, we measure approximately 480 MB/s when tensors are hosted on K80 GPUs. One reason is due to copy and serialization process between GPU, host memory and inter-node transfer.

Finally, we show that gRPC gives the lowest bandwidth on Tegner. We note that this is due to gRPC connection is resolved to communicate through Ethernet. On Kebnekaise communicating through gRPC gives similar bandwidth to that of MPI.

B. Tiled Matrix Multiplication

Our tiled matrix multiplication is implemented as a communication intensive application. Matrix tiles and results continuously flow through GPUs and the network. We show that the application gives good scalability on one of our test platform but gives sub-optimal scaling on another. We evaluate the performance of the application with three problem sizes: $16384 \times 16384 (2^{14})$, $32768 \times 32768 (2^{15})$ and $65536 \times 65536 (2^{16})$. The problems consist of randomly generated dense matrices. The matrices are pre-processed into tiles with tile size $4096 \times 4096$ and $8192 \times 8192$.

We test the application on Tegner and Kebnekaise. On Tegner we perform tests with two to eight K420 and K80 GPUs and on Kebnekaise we test with two to 16 K80 GPUs. To increase utilization, we use tile size $4096 \times 4096$ for K420 and run all problem sizes. For K80, we use tile size $8192 \times 8192$ and only run problem size $32768 \times 32768$ and $65536 \times 65536$. We run strong scaling tests by varying the number of GPUs being used and report results in Gflops/s. We estimate the flop count as $2N^3 - N^2$. In our implementation we use two reducers to accumulate tiles with target index being odd number and even number.

We observe good scaling on Tegner. Fig. 8 shows the performance results for tests conducted on different platforms. We measure approximately $2 \times$ increase in performance when increasing the number of GPUs from two to four with K420 GPUs on Tegner for problem size $32768 \times 32768$. We observe similar performance improvement for this setting when increasing the number of GPUs in use from four to eight. For K80 GPUs on Tegner, we obtain roughly $1.8 \times$ improvement when scaling from two to four GPUs with problem size $65536 \times 65536$.

We perform similar tests on K80 nodes on Kebnekaise. The scaling result is however less satisfactory. We measure peak performance of 2478 Gflops/s when running on 16 K80 GPUs for problem size $32768 \times 32768$. We obtain scaling of $1.4 \times$ when scaling from two to four GPUs for the same problem size.
To try understanding why scaling is sub-optimal on Kebnekaise we look at the configuration topology of its computing node. One possible explanation is due to the data-driven nature of the application where matrices are constantly flowing in and out of the systems. Fig. 9 shows the topology of a GPU node of Kebnekaise where two K80 GPUs are located on two NUMA islands while I/O and network communication are only connected to either one island. With four instances of TensorFlow running per node comparing to only one or two instances on Tegner potentially means that the amount of data flowing and competing for bandwidth can be large, thus creating bottlenecks.

C. Conjugate Gradient Solver

Our CG solver exhibits generally good scaling across all of our testing platforms. We test the application on Tegner and Kebnekaise. On Tegner we test from two to eight K80 GPUs; on Kebnekaise we test with two to 16 K80 GPUs and with two to eight V100 GPUs. We run strong scaling tests for three problem sizes: $16384 \times 16384$, $32768 \times 32768$ and $65536 \times 65536$ on Tegner and Kebnekaise with K420, K80 and V100 GPUs. Results are reported in Gflops/s. 

4https://www.hpc2n.umu.se/resources/hardware/kebnekaise
The matrices are pre-processed by splitting into tiles where the size depends on the number GPUs used. For K80 GPUs on Tegner and V100 GPUs on Kebnekaise, we do not report result for problem size $65536 \times 65536$ due to insufficient memory and insufficient number of GPUs available; for K80 GPUs on Kebnekaise, we only report results for problem size $65536 \times 65536$ from eight to 16 GPUs. We report performance in Gflops/s and estimate flop count to be $500 \times 2 \times N^2$, where 500 is the number of iterations we run per test and $N^2$ belongs to run time dominating matrix vector multiplication.

The test results are summarized in Fig. [10]. We are only able to obtain little scaling for problem size $16384 \times 16384$ across different platforms. This is likely due to underutilization of GPUs after splitting the problem. This is particular obvious for tests on V100 GPUs on Kebnekaise as it is a powerful GPU. We observe a scaling of $1.6\times$ in performance when increasing from two to four K80 GPUs on Kebnekaise with problem size $32768 \times 32768$. When increasing the number of K80 GPUs in use from four to eight for the same setting, scaling drops to $1.3\times$, which is consistent with the expected behaviour of strong scaling. Similarly, we observe improvement of $1.36\times$ when scaling from eight to 16 K80 GPUs. Tests on V100 nodes on the other hand give $1.26\times$ improvement in performance when scaling the number of GPUs from two to four with problem size $32768 \times 32768$. When increasing the number of GPUs from four to eight improvement drops to $1.16\times$, indicating ratio between problem size and computation power must be optimized. We obtain similar scaling result on Tegner. We measure an approximately $1.74\times$ improvement in performance when scaling from two to four K80 GPUs with problem size $32768 \times 32768$.

Comparing to the performance of the matrix-matrix multiplication application, the CG solver gives better scaling on both Tegner and Kebnekaise. A key difference is that the amount of data flowing between GPUs and reducer is relatively little, consisting mostly of vectors and scalars instead of dense matrices.

Despite the difficulty in direct comparison against other frameworks, we refer to several related works on CG solver implementation on GPU for an overview of related performance results. A similar implementation of task-based CG algorithm was implemented in Ref. [11] with StarPU on a system with three NVIDIA Tesla M2070 GPUs and they recorded performance close to 30 Gflops/s on three GPUs. Ref. [12] ports and evaluates NekBone, a computational fluid dynamics mini-application to GPU with OpenACC which relies on a CG solver. They evaluated the implementation on a cluster with NVIDIA K20 GPUs and reached up to 43 Gflops/s on a single node. Our CG solver, running on eight V100 GPUs gave over 300 Gflops/s.

### D. Fast Fourier Transform

The scaling performance of our FFT application is overall satisfactory. We test the application on Tegner with both K420 and K80 GPUs. For K420, we evaluate problem size $2^{29}$ with 64 tiles with size $2^{23}$; for K80, we evaluate problem size $2^{31}$ with 128 tiles with size $2^{24}$. We perform strong scaling tests and scale from two to eight GPUs. Since we perform serial merging of results in Python with one process, the cost is theoretically constant regardless of the number of GPUs used. For this reason, we only report scaling results from the beginning of the application to when all tiles are collected by the merger. Results are reported in Gflops/s and we estimate the flop count of the application with $5 \times N \log_2 N$.

We observe good scaling when increasing the number of GPUs in use from two to four for both GPUs. The results are reported in Fig. [11]. When increasing from two to four GPUs for both configurations there is an approximately $1.6\times$ to $1.8\times$ increase in performance. However when increasing from four to eight GPUs the performance improvement clearly flattens out. One reason is underutilization of GPUs when the number of tiles processed per GPU decreases.

## VII. Related Work

The TensorFlow programming framework was released open-source in 2015 and presented in a seminal paper by Abadi et al. [8] at the USENIX Symposium on Operating Systems Design and Implementation in 2016. This paper presents the basic TensorFlow concepts and design. A hands-on description of how to use TensorFlow in distributed environment is included in the book [13]. The performance evaluation of TensorFlow under ML workloads was presented in Ref. [7] and Ref. [14] studied TensorFlow application running on supercomputers.

In terms of communication performance, Ref. [15] designed a benchmark suite to study the communication performance of TensorFlow. Refs. [16] and [17] investigated the use of MPI collectives for communication between TensorFlow processes. Studies have also been done to investigate different implementation of RDMA on TensorFlow to improve communication efficiency [18][19][20].

The main competitor of TensorFlow is PyTorch [21], an open-source Python framework. PyTorch supports execution of application on distributed systems with GPUs. The main difference with TensorFlow is that PyTorch is based on eager execution model instead of the current TensorFlow default deferred execution model. As it is easier to program and debug code in eager mode, an increasing number of users begins to use PyTorch. However, it is likely that future release of TensorFlow will have eager execution mode by default.

Some other deep-learning frameworks that are increasingly being adopted in HPC systems include Caffe [22]. Caffe focuses on GPU training on a single node. S-Caffe extends Caffe and provides distributed GPU training on a cluster through co-designing the framework with CUDA-aware MPI to provide better interoperability between CUDA and MPI [23].
Fig. 11. Performance of FFT solver on Tegner with problem size $2^{31}$ in 128 tiles of problem size $2^{29}$ with K80 GPUs in Gflops/s; problem size $2^{29}$ in 64 tiles of size $2^{23}$ with K420 GPUs in Gflops/s.

HPC frameworks that are using computational graph and are similar to TensorFlow despite not designed for ML workloads, are PaRSEC (Parallel Runtime Scheduling and Execution Controller) and StarPU. PaRSEC [24] is a programming framework for distributed many-core heterogeneous architectures. Applications in PaRSEC are expressed as a Direct Acyclic Graph (DAG) of tasks with edges representing dependencies. StarPU [25] is a task-based programming framework where tasks are represented as a series of DAG.

VIII. DISCUSSION AND CONCLUSION

In this paper we introduced the development paradigm of HPC application with TensorFlow. We designed and implemented four common HPC applications and performed experiments on different HPC platforms with GPUs. We also introduced and discussed the distributed programming model of TensorFlow. TensorFlow currently supports a parameter server-worker model where workers perform individual work with new data and update parameter. This however, presents a challenge when developing HPC applications that are based on domain decomposition. In addition, this hampers the scalability of large scale deployment with large number of machines. Some of the efforts to increase support to these applications include Uber’s Horovod [12] and Cray’s Machine Learning Plugin[14]. These plugins enable the development of application with MPI like interfaces through an MPI communication backend for functions such as allreduce without needing the use of dedicated servers for parameters.

During our development, one difficulty is the reformulation of algorithms that require reduction, where we have to implement our reducer with queue dataflow mechanisms. Another limitation is imposed by Python. One example is the Global Interpreter Lock which prevents concurrent thread execution, which QueueRunners are dependent on. Another example is the Python’s relatively low performance in numerical computation. This hampers performance of applications where logic are difficult to express in computation graph or applications that are partly programmed with TensorFlow and partly in Python. An example is our FFT application. The process of merging in Python takes considerably longer execution time then the computation part by TensorFlow. In fact we initially discovered that directly performing slicing insertion into a local Numpy array during the extraction of tiles from the graph already hampers overall performance thus preventing any scaling during the computation of FFT on tiles by TensorFlow.

https://www.cray.com/products/analytics/urika-xc
Despite all of that, TensorFlow is a rapidly growing programming framework that can be used for development of HPC applications on supercomputers with accelerators. It provides a complete programming environment ranging from high-level APIs to a C++ runtime for device management and communication. The high level APIs allow easy development and deployment of distributed algorithms without needing in-depth knowledge into concepts such as CUDA and MPI. In fact, our distributed CG solver with checkpoint-restart capability only consists of less than 300 lines of code and our matrix multiplication application consists only of less than 240 lines of code. TensorFlow’s deferred execution model presents an opportunity for runtime optimization and improved auto parallelization.

Our performance results demonstrated that TensorFlow is a promising framework. All of our applications which are formulated with data-driven approach show good scaling when the number of GPUs being used increases, without requiring the use of low level APIs such as CUDA and MPI. We showed that TensorFlow has high potential to become a HPC programming framework for heterogeneous supercomputers.

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**REFERENCES**

[1] S. Markidis, S. W. D. Chien, E. Laure, I. B. Peng, and J. S. Vetter, “NVIDIA Tensor Core Programmability, Performance & Precision,” in 2018 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW), May 2018, pp. 522–531.

[2] N. P. Jouppe, C. Young, N. Patil, D. Patterson, G. Agrawal, R. Bajwa, S. Bates, S. Bhatia, N. Boden, A. Borchers et al., “In-datacenter performance analysis of a Tensor Processing Unit,” in Computer Architecture (ISCA), 2017 ACM/IEEE 44th Annual International Symposium on. IEEE, 2017, pp. 1–12.

[3] J. Dean, G. Corrado, R. Monga, K. Chen, M. Devin, M. Mao, A. Senior, P. Tucker, K. Yang, Q. V. Le et al., “Large scale distributed deep networks,” in Advances in neural information processing systems, 2012, pp. 1223–1231.

[4] A. B. Yoo, M. A. Jette, and M. Grondona, “Slurm: Simple Linux Utility for Resource Management,” in Workshop on Job Scheduling Strategies for Parallel Processing. Springer, 2003, pp. 44–60.

[5] M. Abadi, M. Isard, and D. G. Murray, “A computational model for TensorFlow: an introduction,” in Proceedings of the 1st ACM SIGPLAN International Workshop on Machine Learning and Programming Languages. ACM, 2017, pp. 1–7.

[6] F. Kleppmann, Designing data-intensive applications: The big ideas behind reliable, scalable, and maintainable systems. “ O’Reilly Media, Inc., 2017.

[7] S. W. D. Chien, S. Markidis, C. P. Sishtla, L. Santos, P. Herman, S. Narasimhanurthy, and E. Laure, “Characterizing deep-learning I/O workloads in TensorFlow,” 2018 IEEE/ACM 3rd International Workshop on Parallel Data Storage & Data Intensive Scalable Computing Systems (PDSW-DISCS), 2018.

[8] M. Abadi, P. Barham, J. Chen, Z. Chen, A. Davis, J. Dean, M. Devin, S. Ghemawat, G. Irving, M. Isard et al., “TensorFlow: A system for large-scale machine learning,” in OSDI, vol. 16, 2016, pp. 265–283.

[9] J. D. McCalpin et al., “Memory bandwidth and machine balance in current high performance computers,” IEEE computer society technical committee on computer architecture (TCCA) newsletter, vol. 2, no. 19–25, 1995.

[10] F. Nowak, I. Besenfelder, W. Karl, M. Schmidtobreick, and V. Heuveline, “A data-driven approach for executing the CG method on reconfigurable high-performance systems,” in Architecture of Computing Systems – ARCS 2013, 2013, pp. 171–182.

[11] E. Agullo, L. Giraud, A. Guermouche, S. Nakov, and J. Roman, “Task-based Conjugate Gradient: From multi-GPU towards heterogeneous architectures,” in Euro-Par 2016: Parallel Processing Workshops, 2016, pp. 69–82.

[12] S. Markidis, J. Gong, M. Schliephake, E. Laure, A. Hart, D. Henty, K. Heisey, and P. Fischer, “OpenACC acceleration of the Nek5000 spectral element code,” The International Journal of High Performance Computing Applications, vol. 29, no. 3, pp. 311–319, 2015.

[13] A. Géron, Hands-on machine learning with Scikit-Learn and TensorFlow: concepts, tools, and techniques to build intelligent systems. ” O’Reilly Media, Inc.”, 2017.

[14] A. Mathuriy, D. Bar, P. Mendygral, L. Meadows, J. Arnemann, L. Shao, S. He, T. Karna, D. Moise, S. J. Pennycook et al., “CosmoFlow: using deep learning to learn the universe at scale,” arXiv preprint arXiv:1808.04728, 2018.

[15] R. Biswas, X. Lu, and D. K. Panda, “Designing a micro-benchmark suite to evaluate gRPC for TensorFlow: Early experiences,” arXiv preprint arXiv:1804.01138, 2018.

[16] A. Vishnu, C. Siegel, and J. Daily, “Distributed TensorFlow with MPI,” arXiv preprint arXiv:1603.02339, 2016.

[17] A. Sergeev and M. D. Balso, “Horovod: fast and easy distributed deep learning in TensorFlow,” arXiv preprint arXiv:1802.05799, 2018.

[18] C. Jia, J. Liu, X. Jin, H. Lin, H. An, W. Han, Z. Wu, and M. Chi, “Improving the performance of distributed TensorFlow with RDMA,” International Journal of Parallel and Distributed Processing, Sep 2017.

[19] J. Xue, Y. Miao, C. Chen, M. Wu, L. Zhang, and L. Zhou, “RPC considered harmful: fast distributed deep learning on RDMA,” arXiv preprint arXiv:1805.08430, 2018.

[20] B. Yi, J. Xia, L. Chen, and K. Chen, “Towards zero copy dataflows using RDMA,” in Proceedings of the SIGCOMM Posters and Demos, ser. SIGCOMM Posters and Demos ’17. ACM, 2017, pp. 28–30.

[21] A. Paszke, S. Gross, S. Chintalas, G. Chanan, E. Yang, Z. DeVito, Z. Lin, A. Desmaison, L. Antiga, and A. Lerer, “Automatic differentiation in PyTorch,” 2017.

[22] Y. Jia, E. Shelhamer, J. Donahue, S. Karayev, J. Long, R. Girshick, S. Guadarrama, and T. Darrell, “Caffe: Convolutional Architecture for Fast Feature Embedding,” in Proceedings of the 22nd ACM International Conference on Multimedia, ser. MM ’14. ACM, 2014, pp. 675–678.

[23] A. A. Awan, K. Hamidouche, J. M. Hashmi, and D. K. Panda, “S-Caffe: Co-designing MPI Runtimes and Caffe for Scalable Deep Learning on Modern GPU Clusters,” in Proceedings of the 22Nd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, ser. PPoPP ’17. ACM, 2017, pp. 193–205.

[24] G. Bosilca, A. Bouteiller, A. Danalis, M. Faverge, T. Hérault, and J. J. Dongarra, “Parsec: Exploiting heterogeneity to enhance scalability,” Computing in Science & Engineering, vol. 15, no. 6, pp. 36–45, 2013.

[25] C. Augonnet, S. Thibault, R. Namyst, and P.-A. Wacrenier, “StarPU: a unified platform for task scheduling on heterogeneous multicore architectures,” Concurrency and Computation: Practice and Experience, vol. 23, no. 2, pp. 187–198, 2011.