Preliminary Design of Readout Electronics for CDEX-10 in CJPL

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Abstract. CDEX (China Dark Matter Experiment) is now upgraded to about 10 kg HPGe (High Purity Germanium) detectors and new dedicated readout electronics is in operation. The readout system is interfaced to the front preamplifiers, which have two “slow” outputs with typical 20 µs shaping time and two “fast” output with typical 200 ns shaping time. 8 channels 14-Bit 100 MSPS FADC and 2 channels 12Bit 2000 MSPS FADC are embedded in the readout 6U prototype board. The RAIN1000Z2 readout module based on ZYNQ SoC is used for readout with Gigabit Ethernet.

1. Introduction

The CDEX experiment in CJPL (China Jinping Underground Laboratory) is located in Xichang, Sichuan province, China. The mass of a new generation of HPGe detectors will be increased to about 10 kg in 10 modules. New readout electronics are needed for pulse digitization.

As is well known, Germanium detectors are extensively used for gamma spectroscopy and are generally readout with charge sensitive amplifiers, which convert the charge signals from the detectors to voltage signals whose amplitude depends on the physical events and the value of a known feedback capacitor. Germanium detectors are operated in a cryogenic environment and the preamplifiers’ circuit also must operate at low temperature.

There are four identical energy-related output signals of the preamplifiers located near by the Germanium detector which we used in the CDEX experiment. Two of them are distributed into shaping amplifiers with high gain for low energy region (0-12 keV) at different shaping time, 6 µs and 12 µs, respectively. The Gauss shaping is useful for high precision energy measurement. The other two outputs are connected to timing amplifiers, one with high gain for medium energy region (0-20 keV) and another with low gain for high energy (0-1.3 MeV). Relatively accurate time information will help to discriminate the bulk and surface events within the Germanium detector and understand the background origin.

Totally there are two “slow” signals whose shaping time is about several 10 µs, and two “fast” signals which rising time (10% - 90%) is about 300 ns. The “slow” signals are used for energy measurement and background elimination near by the threshold, which requires relatively high precision or resolution of digitization. The “fast” signals are helpful to distinguish the surface events and the background events with digitization of the fast rising edge, which requires high speed (about 1 GHz sampling speed) and more data buffers for electronics.
The preliminary design of readout electronics is catered to the pulse digitization and readout of two “slow” signals and two “fast” signals. Figure 1 depicts the overall system architecture of CDEX experiment and the details of readout electronics.

### 2. Hardware design

With the two kind of signals output from main amplifiers (shaping amplifiers and timing amplifiers), the “slow” signal has 10 µs typical shaping time and the “fast” signal has 300 ns typical shaping time, and the signals from photomultiplier coupled to NaI(TI) Anti-Compton detector, two kinds of FADC are embedded in the 6 U size readout electronics prototype board.

The 8 channel 14-Bit 100 MSPS FADC (high resolution for energy measurement) and 2 channel 12-Bits 1000 MSPS FADC (high speed for rising edge digitization) are combined and used for pulse shape digitization. The Kintex XC7K325T FPGA from Xilinx is used for the system control and DDR3 SDRAMs buffer control. The 64-Bit 1600 MHz DDR3 SDRAM is implemented in system and associated to the Kintex FPGA for high speed data throughput, high capacity data buffer.

The readout module RAIN1000Z2 [1] which was developed for compact readout application based on ZYNQ SoC is used for high speed data exchange to PC or data servers. The gigabit Ethernet interface is used for communication. The actual picture is shown in figure 2.

One of the design’s challenges is the PCB layout for 2 GHz FADC and 1600 MHz 64-Bit DDR3 SDRAM. As calculated, the input data band width is about 59.2 Gbps, include 8 channel 14-Bit 100 MSPS FADC’s data and 4 channel 12-Bit 1000 MSPS FADC’s data. In many situation, we need buffer the real-time data stream in the external buffers for trigger system to select the right physical valid event. The 1600 MHz 64-Bit DDR3 SDRAMs are deployed for external buffer. 1600 MHz is the art of state for high performance digital electronics design, signal length match and impedance control are very critical for this design.

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The fly-by topology is used for address and control signals of the DDR3 SDRAMs, and point to point topology is used for data signals. Figure 3 illustrate the address and control signals layout rules and mechanism. Figure 4 show the PCB layout’s detail where the DDR3 SDRAMs are connected to FPGA with trace tuning and length matched.

As it is in most ultra-high-speed hardware PCB layout designs, SI (signal integrity) is the key issue. Simultaneously, with the fly-by topology, the high-speed 1600 MHz memory interface of DDR3 SDRAM should keep, not only the trace on the PCB to be 40-Ohm impedance-controlled and length-matched, but the flight time in the silicon package also had to be considered and compensated. The twists and turns of PCB traces in different layers can be observed in figure 4.
The thermal design is also important for high speed FADC and FPGA. Due to the compact size of the readout board, several compact heat-sink cap are designed for FADC and FPGA. With the heat-sink cap assembled, the FPGA chip cools down from 73°C to 53°C.

3. System design
The Vivado IDE (Integrated Development Environment) from Xilinx is used for system design. Embedded Linux is running within the RAIN1000Z2 readout module and TCP/IP is used for data transport. A user interface program which is developed based on gcc in Ubuntu is used for data real time storage, monitor and analysis.

4. Performance test and result
The system performance is tested based on the HDL and C program, the ENOB of two kinds of FADC is tested and the data throughput between Kintex FPGA RAIN1000Z2 readout module is also tested. The TCP/IP raw data throughput with the Gigabit Ethernet interface is more than 700 Mbps with the RAIN1000Z2 readout module and associated software in PC or servers.

Initial ENOB of the 100 MSPS 14-Bit FADC is about 11.5-Bit and 8.7-Bit for the 1000 MSPS 12-Bit FADC. More in-depth test will be processed in the future.

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References
[1] T. Xue, W. Pan, G. Gong, M. Zeng, H. Gong, and J. Li, "Design of Giga bit Ethernet readout module based on ZYNQ for HPGe," IEEE-NPSS Real Time Conference (RT), May, 2014.