Design and Application of a Series and Parallel-summation Logarithmic Video Amplifier

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Abstract: Starting with the concept of logarithmic video amplifier, this paper mainly derives the transfer functions of different logarithmic video amplifiers. The practical application of logarithmic video amplifier in the radar warning receiver is designed, and three pieces of conclusion about logarithmic video amplifier in RWR have been reached. Firstly, logarithmic transformation is completed for obtaining the azimuth information. Secondly, compressing the dynamic range is realized so that to the subsequent circuits signal processing becomes easier. Thirdly, the signal is amplified for improving the sensitivity of the receiver. A three-parallel-summation and single-series logarithmic video amplifier is used in a RWR so its direction finding precision is up to 8°, its dynamic range is up to 140dB, its sensitivity is up to -80dBm and its technique is in a higher level.

1. Introduction

Logarithmic video amplifier, which is called LVA for short, is a component which can amplify and transform video pulse logarithmically. In radar reconnaissance system, the receiver usually processes pulse signals which are very narrow, intensive, randomly variable, and the pulse signals usually change about 70dB to 120dB in a short time. On the one hand, automatic gain control circuits are limited in practical use. On the other hand, the limiting amplifier limits pulse amplitude information. Logarithmic video amplifier is probably the best in the case.

A new series and parallel-summation logarithmic video amplifier is designed. It can amplify the faint signals with high-gain and automatically reduce gain for the strong signals, so the amplitude of the output signals is stable. This makes it easy for the subsequent circuit to measure and process the video pulse. It is applied in the direct-detection radar warning receiver, so its dynamic range is up to 140dB and its sensitivity is up to -80dBm.

2. Circuit Structure Analysis

From the degree of completing logarithmic transformation, logarithmic video amplifier may be divided into the true logarithmic video amplifier and the approximate logarithmic video amplifier. According to the structure of the logarithmic video amplifier, it may be divided into three types: the series logarithmic video amplifier, the parallel-summation logarithmic video amplifier, and the series and parallel-summation logarithmic video amplifier. Each of them will be discussed in turn.
2.1. The Series Logarithmic Video Amplifier

Figure 1 shows the topology of the most widely used series-summation logarithmic video amplifier [1].

In Figure 1, the units $A_1$, $A_2$, $A_3$, $A_n$, are limiter amplifiers in differential structure and they are linear before limiting. The gain of each unit is $A$. $V_{cc}$, $V_{ee}$, Bias respectively provide collector supply voltage, emitter supply voltage and bias voltage for the units. When the input voltage $V_{in}$ rises to the break point voltage $E_k$, the output voltage is a constant $V_L$. The output of every stage adds at the summation amplifier, and $V_{out}$ is the output voltage of the summation amplifier. $A_i$ is the gain of the summation amplifier. $V_{Li}$ is the break point voltage of the summation amplifier. Every unit is same in structure, so their transmission characteristics are also same.

$$A_1 = A_2 = \cdots = A_n = A_{n+1} = A$$

Therefore,

$$V_{out} = A_0 V_{in} (1 + A_1 + A_2 A_3 + \cdots + A_1 A_2 A_3 \cdots A_n) = A_0 V_{in} (1 + A + A^2 + A^3 + \cdots + A^n)$$  \hspace{1em} (1)$$

When the input signal $V_{in}$ is less than or equal to $V_{Li}/A^n$, every amplifier is in the range of linearity. So the total magnification of the summation amplifier is $1 + A + A^2 + A^3 + \cdots + A^n = A^n$. Therefore

$$V_{out} = A^n A_0 V_{in}$$  \hspace{1em} (2)$$

At the moment, the small-signal gain is

$$G_{eq} = 20 \log \left( \frac{V_{out}}{V_{in}} \right) = 20 \log (A^n A_0)$$  \hspace{1em} (3)$$

The gain is the maximum when all the amplifiers are in the range of linearity. When the input signal $V_{in}$ is increasing gradually and its amplitude is in $[V_L/A^n, V_L]$, they will come to limit state step by step following the subsequence of $A_n \rightarrow A_{n-1} \rightarrow \cdots \rightarrow A_2 \rightarrow A_1$.

When the input voltage $V_{in}$ rises to $V_{in} = V_L/A^n$, the $n^{th}$ amplifier comes to a saturation state while the rest are in the range of linearity. At the moment, the output voltage is

$$V_{out1} = A_0 V_{in} (1 + A + A^2 + A^3 + \cdots + A^{n-1}) + A_1 V_L$$  \hspace{1em} (4)$$

When the input voltage $V_{in}$ rises to $V_{in} = V_L/A^{n-1}$, the $n^{th}$ and $(n-1)^{th}$ amplifiers come to a saturation state while the rest are in the range of linearity. At the moment, the output voltage is

$$V_{out2} = A_0 V_{in} (1 + A + A^2 + A^3 + \cdots + A^{n-2}) + 2A_1 V_L$$  \hspace{1em} (5)$$

And so on, $n$ amplifiers come to the saturation state when the input voltage $V_{in}$ rises to $V_{in} = V_L/A$.
At the moment, the output voltage is

\[ V_{\text{state}} = A_0 V_{\text{in}} + nA_V L \]  

(6)

When the input voltage \( V_{\text{in}} \) rises to \( V_{\text{out}(n+1)} = V_{L1} \), \( n \) amplifiers and the summation amplifier come to saturation state. At the moment, the output voltage is

\[ V_{\text{out}(n+1)} = A V_{L1} + nA V = A_L (V_{L1} + nV_L) \]  

(7)

Figure 2 shows the transmission curve of the series-summation logarithmic video amplifier.

![Figure 2](image_url)

Figure 2. The transmission curve of the n-stage series-summation logarithmic video amplifier.

The series-summation logarithmic video amplifier approaches logarithmic function sectionally in nature and the relationship between its output and its input is approximately logarithmic. So it is an approximate logarithmic video amplifier. There is a contradiction between the quantity of the stages, the gain of every stage and dynamic range, the bandwidth, and the transition error in the series-summation logarithmic video amplifier. The more the stages of the series and each stage gain are, the wider the dynamic range becomes. However, the more the stages of the series are, the narrower the bandwidth is and the more unstable the circuit becomes. The more each stage gain is, the lower the transition precision is and the greater the transition error becomes. So the number of stages is about 4 or 5 and the dynamic range of the series-summation logarithmic video amplifier is less than or equal to 100dB.

2.2. **Parallel-summation Logarithmic Video Amplifier**

Figure 3 shows the topology of the parallel-summation logarithmic video amplifier\(^2\):

![Figure 3](image_url)

Figure 3. The topology of the parallel-summation logarithmic video amplifier.

There are \( n \) branches \( G_{p1}, G_{p2}, \ldots, G_{pn} \) in figure 3 and each branch includes the proportional and
operational amplifier \( A_k (k = 1, 2, 3, \ldots, n) \), the limit transconductance unit \( g_m \) and the current-summation unit. The magnification of each branch is \( A_1 = 1, A_2 = A \cdot 1, A_3 = A(A \cdot 1), A_4 = A^2(A \cdot 1), \ldots, A_n = A^{n-1}(A \cdot 1) \) in turn. The operational amplifiers and the transconductance unit transform the input signal into a current signal. After summation the currents from the branches are transformed into voltage signals by the resistive load.

Figure 4 shows the transmission curve of the parallel-summation logarithmic video amplifier\(^3\). Suppose that the constant \( A \) is defined as the factor increase in the input voltage between the cusps of the logarithmic approximation, if \( D \) is defined as the dynamic range of the logarithmic video amplifier, the constant \( A \) is chosen as \( \frac{1}{N D} \). The current \( I_{s} \) is defined as the increase in output current between the cusps of the approximation and that is the saturate output current of the limit transconductance unit \( g_m \). So \( I_s = I_L \). The voltage \( V_{min} \) is defined as the break point voltage of the limit transconductance unit \( g_m \).

When the input voltage \( V_{in} \) is less than \( V_{min} \), no limit transconductance unit is in the saturation state. So the total output current is

\[
I_{out} = V_{in} (A_1 g_m + A_2 g_m + \cdots + A_n g_m)
\]

When the input voltage \( V_{in} \) is equal to \( V_{min} \), no limit transconductance unit is in the saturation state. So the total output current is

\[
I_{out} = V_{min} A (A g_m + A g_m + \cdots + A g_m) = V_{min} g_m (A_1 + A_2 + \cdots + A_n) = V_{min} g_m A^{n-1} = C
\]

When the input signal is increased gradually, the limit transconductance units will come to the limit state step by step following the subsequence of the \( n^{th} \) branch→the \( (n-1)^{th} \) branch→…→the \( 2^{nd} \) branch→the \( 1^{st} \) branch.

When the input voltage \( V_{in} \) rises to \( AV_{min} \), the output voltage of the \( n^{th} \) amplifier is too high and its limit transconductance unit \( g_m \) comes to the saturation state while the rest are in the range of linearity. So the total output current is

\[
I_{out} = AV_{in} (A_1 g_m + A_2 g_m + \cdots + A_n g_m) + I_s = AV_{min} g_m (A_1 + A_2 + \cdots + A_n) + I_s = AV_{min} g_m A^{n-1} + I_s = V_{min} g_m A^{n-1} + I_s = C + I_s
\]

When the input voltage \( V_{n} \) rises to \( A^n V_{min} \), the output voltages of the \( n^{th} \) and the \( (n-1)^{th} \) amplifier are too high. Their limit transconductance unit \( g_m \) comes to the saturation state while the
rest are in the range of linearity. So the total output current is

\[ I_{\text{out}} = A V_{m}(A g_{n} + A_{2}g_{n} + \cdots + A_{2}g_{n}) + 2I_{S} = A V_{m}g_{n}(A_{1} + A_{2} + \cdots + A_{2}) + 2I_{S} \]

\[ = A V_{m}g_{n}[I + (A - 1) + A(A - 1) + A^{2}(A - 1) + \cdots + A^{n-2}(A - 1)] + 2I_{S} = A V_{m}g_{n}A^{n-1} + 2I_{S} = V_{m}g_{n}A + 2I_{S} = C + 2I_{S} \]  

\( (10) \)

Similarly, when the input voltage rises to \( A^{n}V_{\text{min}} \), the output voltages of the \( n^{th} \), the \( (n - 1)^{th} \), \( \ldots \), the \( 2^{nd} \) amplifier are too high. Their limit transconductance unit \( g_{m} \) comes to the saturation state whereas the \( 1^{st} \) is in the range of linearity. So the total output current is

\[ I_{\text{out}(n-1)} = A^{n}V_{\text{min}} A g_{m} + (n - 1) I_{S} = A^{n}V_{\text{min}}g_{m} + (n - 1) I_{S} = V_{\text{min}}g_{m}A^{n-1} + (n - 1) I_{S} = C + (n - 1) I_{S} \]  

\( (11) \)

When the input voltage rises to \( A^{n}V_{\text{min}} \), \( n \) limit transconductance units comes to the saturation state. So the total output current is

\[ I_{\text{out}} = C + nI_{S} \]  

\( (12) \)

If the \( k^{th} \) branch is limited, the \( (N - k)^{th} \) branches with higher gain are limited while from the \( 1^{st} \) branch to the \( (k - 1)^{th} \) branch are in the range of linearity. So the total output current is

\[ I_{\text{out}} = (N - k)I_{S} + V_{m}(A g_{n} + A_{2}g_{n} + \cdots + A_{k-2}g_{n}) = (N - k)I_{S} + V_{m}g_{n}(A_{1} + A_{2} + \cdots + A_{k-2}) \]

\[ = (N - k)I_{S} + V_{m}g_{n}[I + (A - 1) + A(A - 1) + \cdots + A^{k-2}(A - 1)] = (N - k)I_{S} + V_{m}g_{n}A^{k-1} \]  

\( (13) \)

Suppose the \( k^{th} \) branch happens to be on the critical point, the input is

\[ V_{\text{in}} = V_{m} = I_{S} \frac{g_{m}}{A k^{2}(A - 1)} \]  

\( (14) \)

From (14), we can obtain,

\[ k = \log_{A} \left[ \frac{A^{2}I_{S}}{g_{m}V_{\text{in}}(A - 1)} \right] \]  

\( (15) \)

Substituting (14) and (15) into (13), we get,

\[ I_{\text{out}} = (N - k)I_{S} + V_{m}g_{n}A^{k-1} = (N - k)I_{S} + \frac{I_{S}}{g_{m}A^{k-2}(A - 1)} g_{m}A^{k-1} = (N - k)I_{S} + \frac{A I_{S}}{A - 1} \]

\[ = I_{S}(N + A) = I_{S}(N + A) - \log_{A} \left[ \frac{A^{2}I_{S}}{g_{m}V_{\text{in}}(A - 1)} \right] = I_{S}(N + A) + \log_{A} \left[ \frac{g_{m}V_{\text{in}}(A - 1)}{A^{2}I_{S}} \right] \]  

\( (16) \)

From (16) we know that the relationship between the output current \( I_{\text{out}} \) and the input voltage \( V_{\text{in}} \) is ideal logarithmic. The parallel-summation logarithmic video amplifier approaches logarithmic function sectionally in nature. Compared with the series-summation structure, the parallel-summation logarithmic video amplifier can avoid such shortcomings as too narrow bandwidth and unstable circuit caused by too many stages. However, there is a contradiction between the quantity of the stages, the gain of every stage and dynamic range, the bandwidth, and the transition error in the parallel-summation logarithmic video amplifier. The more the gain is, the greater the transition error is. Although the dynamic range will be larger with the more stages, the gain of the preamplifier processing the small signal will be larger. This increases the complexity of the circuit so much as not to be realized. Therefore, the number of stages is 4-5 and the dynamic range is less than or equal to 100dB in the practicable parallel-summation logarithmic video amplifier.
2.3. Series and Parallel-summation Logarithmic Video Amplifier

Figure 5 shows the topology of the series and parallel-summation logarithmic video amplifier. In figure 5, the series and parallel-summation logarithmic video amplifier consists of \( n \) preamplifiers \( A \) with different magnification, \( n \) series-summation logarithmic video amplifiers \( L \), and the parallel-summation circuit.

![Figure 5. Topology of the series and parallel-summation logarithmic video amplifier.](image)

The series and parallel-summation logarithmic video amplifier aggregates the advantage of the series logarithmic video amplifier as well as the parallel logarithmic video amplifier. It enlarges the dynamic range and overcomes such shortcomings as narrow bandwidth, instability, slow response caused by too many stages. It is of great practical significance[4].

3. Design and Application of the series-parallel LVA

3.1. Design of the Series-Parallel logarithmic video amplifier

Figure 6 shows a three-parallel-summation and single-series logarithmic video amplifier designed by us.

![Figure 6. A three-parallel-summation and single-series logarithmic video amplifier.](image)
In figure 6, the magnification of three preamplifiers is $A^1$, $A^2$, $A^3$ in turn. The first logarithmic video amplifier $L_1$ consists of two limit amplifiers which are in series. The second $L_2$ and the third $L_3$ consist of five limit amplifiers which are also in series. The gain $A$ of each limit amplifier is 6, so the input dynamic range is 140dB. The circuit is analyzed as follows.

When the input is a small signal, no unit is in the saturation state. So the total output voltage is

$$V_{out} = V_{out} + V_{out} + V_{out}$$

$$= (G_1 + G_2 + G_3 )V_n + (G_4 + G_5 + G_6 + G_7 )V_n + (G_8 + G_9 + G_{10} + G_{11} + G_{12} )V_n$$

$$= (A^1 + A^2 + A^3 )V_n + (A^4 + A^5 + A^6 AA + A^7 AA^2 )V_n + (A^8 + A^9 + A^10 )V_n$$

$$= A^1 + A^2 + A^3 + A^4 + A^5 + A^6 + A^7 + A^8 + A^9 + A^{10}$$

(17)

In (17), $G_1$, $G_2$, and $G_3$ are gains of the first logarithmic video amplifier. $G_4$, $G_5$, $G_6$, and $G_7$ are gains of the second logarithmic video amplifier. $G_8$, $G_9$, $G_{10}$, $G_{11}$, and $G_{12}$ are gains of the third logarithmic video amplifier.

If the input signal is increasing and the $k^{th}$ limit amplifier is in the saturation state, the total output voltage is

$$V_{out} = \sum_{i=0}^{k-1} A^i V_{in} + (n - k + 1) V_L$$

(18)

In (18), the series logarithmic video amplifier formed with three parallel branches has the same transmission characteristic as the single series logarithmic video amplifier.

The practical results indicated that under the same logarithmic precision, the dynamic range of the series and parallel-summation logarithmic video amplifier with will be 140dB if the dynamic range of the series is 60dB[4].

3.2. Application of the series-parallel logarithmic video amplifier

To sum up, the logarithmic video amplifier has three features. Firstly, its output is in proportion to the logarithm of input and it is one-to-one correspondence in the range of logarithmic precision. Secondly, it can dynamically compress the input signals, that is to say, compressing large dynamic range signals into small dynamic range signals. Thirdly, it can process signals instantaneously[5]. Because of this, it is widely used[6][16], especially in radar and radar reconnaissance systems. Figure 7 shows the block diagram of a radar warning receiver.

![Block diagram of a radar warning receiver](image)

Figure 7. Block diagram of a radar warning receiver.

A radar warning receiver acquires azimuth quickly by adopting 8-channel amplitude-comparison direction-finding. The principle is that it allocates eight antennas with 45° beam width to the eight positions of 360° azimuth and the included angle of adjacent axial lines is 45°. By comparing
amplitudes of electromagnetic waves which receive with direction finding antennas in two adjacent directions, it gets identifications of radar emitters. According to the 8-channel amplitude-comparison direction-finding principle, $u_a$ is defined as the received signal amplitude from an antenna, $u_b$ is defined as the received signal amplitude from an adjacent antenna, $2\theta_{0.5}$ is defined as the 3dB beam width of the antennas, and the letter $S_\theta$ is defined as the included angle of adjacent antenna’s axial lines, so the azimuth $\theta$ is

$$\theta = \frac{(2\theta_{0.5})^2}{12S_\theta - 10\log \frac{u_a}{u_b}}$$

Since the 8-channel amplitude-comparison direction-finding is adopted, $\theta_i$ and $2\theta_{0.5}$ are equal to $\pi/4$, so

$$\theta = \frac{(\pi/4)^2}{12(\pi/4)} - 10\log \frac{u_a}{u_b} = \frac{\pi}{48} - 10\log u_a - \frac{\pi}{48} - 10\log u_b$$

There are two methods of completing direction-finding. The first is that division operation is completed by the divider before logarithmic operation is completed by the logarithmic amplifier. The second is that logarithmic operation is completed by the logarithmic amplifier before subtraction operation is completed by the subtracter. Considering that the subtracter is easier than the divider in practical circuit, the second method is widely used in radar warning receivers. Three pieces of conclusion about logarithmic video amplifier in RWR have been reached. Firstly, logarithmic transformation is completed for obtaining the azimuth information. Secondly, compressing the dynamic range is realized so that signal processing becomes easier for subsequent circuits. Thirdly, the signal is amplified to improve the sensitivity of the receiver. A three-parallel-summation and single-series logarithmic video amplifier designed by us is used in a RWR, so its direction finding precision is up to 8°, its dynamic range is up to 140dB, its sensitivity is up to -80dBm and its technique is in a higher level.

References
[1] J. Li, Y. B. Pang, F. Yang, D.X.Liu and CH.Yang. Logarithmic video amplifier optimal design based on OrCAD[J]. Microelectronics, 2019, 49(2) :193-197.
[2] C. D. Holdenried and J. W. Haslett. A DC-6GHz, 50dB dynamic range, SiGe HBT true logarithmic amplifier[J], Int Symp Circ and Syst, 2004, 289-292.
[3] C. D. Holdenried, J. W. Haslett, J. G. McRory, R. D. Beards, and A. J. Bergsma.A DC-4GHz true logarithmic amplifier: theory and implementation[J].IEEE J. of Solid-State Circuits, 2002, 37(10) :1290-1299.
[4] H. S. Yu, Y. G. Liu, and M. Zhu. Improvement of video logarithmic amplifier dynamic range[J]. Control and Instruments in Chemical Industry, 2010 , 37(5) :64-67.
[5] K. J. Huang, Y. B. Pang, and W. G. Tu.High performance logarithmic amplifiers for radar receivers[J],Microelectronics, 1999, 29(1):50-53.
[6] M. Ferrarini, V. Varoli, A. Favalli, M. Caressana and B. Pedersen.A wide dynamic range BF3 neutron monitor with front-end electronics based on alogarithmic amplifier[J].Nuclear Instruments and Methods in Physics Research, 2010,A613:272-276.
[7] B. S. Li and G. G. Yao.Research on radar IF receiver based on true logarithmic amplifier[J]. Chinese Journal of Electron Devices, 2011, 34(2):163-167.
[8] Y. Lu and W. G. He.Theory of true logarithmic amplifier and analysis of its characteristics[J].Microelectronics, 2011, 41(1):48-52.
[9] X. M. Tian, C. F. Bai, J.H. Wu, M.Zhang and X. C. Ji.A low power dB-linear RSSI based on
logarithmic amplifier[1]. *IEICE Electronics Express*, 2014, 11(12):1-8.

[10] M. Shaterian, A. Abrishamifar and H. Shamsi. Analysis and design of the true piecewise approximation logarithmic amplifiers[J]. *Analog Integrated Circuits and Signal Processing*, 2012, 72:193-203.

[11] R. Wang, Z. G. Wang, J. Xu and Z. Q. Guan. A novel loss-of-signal detector with programmable assert threshold for intelligent limiting amplifier[J]. *Analog Integrated Circuits and Signal Processing*, 2012,72:187-192.

[12] C. Huang and S. Chakrabartty. Current-input current-output CMOS logarithmic amplifier based on translinear Ohm’s law[J]. *Electronics Letters*, 2011, 47(7):433-434.

[13] J. Ramos, J. L. Ausín, J.F.Duque-Carrillo and G. Torelli. Design of limiting/logarithmic amplifier for wideband bioimpedance measuring devices[J]. *Proc. IEEE biomedical circuits and systems conference*, 2010, 290-293.

[14] Z. H. Derafshi and J. Frounch. Low-noise low-power front-end logarithmic amplifier for neural recording system[J]. *International Journal of Circuit Theory and Applications*, 2014, 42:437-451.

[15] J. Ramos, J.L.Ausín, G. Torelli and J.F. Duque-Carrillo. Design tradeoffs for sub-mW CMOS biomedical limiting amplifiers[J]. *Microelectronics Journal*, 2013, 44:904-911.

[16] L.D.Alessandro, M.Palomba, S.Colangeli and E.Limiti. Robust GaN Successive-Detection Logarithmic Video-Amplifier for EW Applications[J]. IELCONF, 2015, 978-1-4673-6496-6.

[17] G. Q. Zhao, radar countermeasures principle, 2st ed. Xian, CN: Xidian University Press, 2012, chapter 3 pp 54-63.