Pixel detector system development at Diamond Light Source

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Abstract. Hybrid pixel detectors consisting of an array of silicon photodiodes bump-bonded to CMOS read-out chips provide high signal-to-noise ratio and high dynamic range compared to CCD-based detectors and Image Plates. These detector features are important for SAXS experiments where a wide range of intensities are present in the images. For time resolved SAXS experiments, high frame rates are compulsory. The latest CMOS read-out chip developed by the MEDIPIX collaboration provides high frame rate and continuous acquisition mode. A read-out system for an array of MEDIPIX3 sensors is under development at Diamond Light Source. This system will support a full resolution frame rate of 1 kHz at a pixel counter depth of 12-bit and a frame rate of 30 kHz at a counter depth of 1 bit. Details concerning system design and MEDIPIX sensors characterization are presented.

1. Introduction
SAXS requires fast X-ray area detectors with high spatial resolution over a large active area. Fast-readout can be obtained with multi-wire gas detectors working in coincidence mode such as the RAPID detector in use on the I22 beamline at the Diamond Light Source (DLS) [1]. A drawback of this gas detector technology is a low maximum global count rate due to the coincidence read-out mode and cumbersome ancillary equipment required to flush gas in the detector chamber. For less demanding experiments, standard CCD+scintillator detectors offer a straightforward solution. Hybrid pixel detectors are an alternative detector technology which fills the gap between CCD-based detectors and fast gas detectors. Hybrid pixel detectors provide excellent performance in terms of signal-to-noise ratio, dynamic range, maximum global count rate and frame rate. Hybrid pixel detectors consist of a pixellated read-out chip electrically connected to a pixellated semiconductor sensor (e.g. silicon) with small solder or indium bumps. X-rays interacting in the silicon sensor are converted into an electrical charge which is amplified and filtered locally in each pixel of the read-out chip. X-ray induced pulses which pass above a preselected threshold increment a counter implemented in each pixel. The counters are read out after the exposure time. Hybrid pixel detectors with 172 µm x 172 µm pixels capable of covering active areas up to 43 cm x 45 cm are commercially available (PILATUS detectors by DECTRIS Ltd. [2]) and are in use in a number of synchrotron beamlines around the world. A hybrid pixel detector with a pixel size of 130 µm (XPAD [3]) was also developed for X-ray scattering and diffraction experiments at SOLEIL, the French national synchrotron facility. MEDIPIX2 developed at CERN [4] is a hybrid pixel detector with pixels of 55 µm size. MEDIPIX2 chips are the core component of the MAXIPIX detector system developed by ESRF for synchrotron

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experiments [5]. Single-chip MEDIPIX2 detectors have also been used for X-ray diffraction and imaging experiments on DLS synchrotron beamlines [6].

2. Charge-sharing in hybrid pixel detectors with small pixels

The main issue arising when reducing the pixel size of hybrid detectors is an increased proportion of X-ray hits generating a charge which is shared between two or more neighboring pixels. Due to the single-photon counting approach enabled by the presence of a signal discriminator in each pixel, charge-sharing between pixels will result in a strong dependence of the detector response on discriminator threshold and X-ray energy. When detecting monochromatic X-rays, a detection threshold set at 50% of the X-ray energy minimizes count loss or double counts at pixel edges. This nonetheless reduces the detection efficiency since X-rays interacting at pixel corners where charge is shared between more than two pixels are not detected. Count loss at pixel corners is visible in figure 1.a showing the response of a MEDIPIX2 detector when a 15 keV X-ray beam focused down to a 6 µm x 4 µm spot size was scanned across a 55 µm sided pixel. This data was acquired on B16 beamline at the Diamond Light Source for a MEDIPIX2 threshold set to 7.5 keV, i.e. 50% of the X-ray energy [7].

Detection efficiency loss is reduced even further when setting the detection threshold at a value higher than 50%, as is sometimes required in order to separate sample fluorescence background from the diffracted X-ray signal. Detection efficiency loss as a function of threshold is shown by the slope of the first part of the S-curve in figure 1.b, obtained by scanning the detection threshold of a MEDIPIX2 sensor illuminated with monochromatic X-rays.

![Figure 1](image)

**Figure 1.** (a) Mean detected count rate as a function of beam position when a 15 keV X-ray beam is scanned across a pixel of a MEDIPIX2. (b) S-curve obtained by plotting the number of X-ray counts as a function of detector threshold while illuminating the whole detector with X-rays of energy 6, 10 and 16 keV.

Discriminator thresholds are not uniform across the read-out chip of a hybrid pixel detector due to variations in the parameters of the CMOS components across the chip. Threshold trimming is usually performed to reduce threshold dispersion across the detector. Charge-sharing results in a higher sensitivity of the detector response to variations in the effective discriminator threshold set in each pixel and makes threshold trimming more difficult.

One of the aims of the new pixel architecture implemented in the read-out chip recently developed by the MEDIPIX3 collaboration is to suppress the effect of charge-sharing on image quality, as described in the following section.
3. MEDIPIX3 read-out chip

The MEDIPIX3 chip was developed by an international collaboration led by CERN, including several synchrotron radiation facilities [8]. It consists of an Application Specific Integrated Circuit (ASIC) designed in 0.13 µm CMOS technology which can be bump-bonded to a pixellated semiconductor sensor. A bare chip (without a sensor) is shown in figure 2.

![MEDIPIX3 read-out chip](image)

**Figure 2.** MEDIPIX3 read-out chip mounted on a carrier board developed by CERN

The chip is mounted on the carrier board and wire-bonds are used to connect the input/output lines of the chip to the carrier board in order to interface the chip with control and data acquisition electronics. Wire-bond connections are located on one side only of the chip so that MEDIPIX3 could be 3-side buttable, allowing several chips to be tiled together to form large detection areas with minimum dead-space. The main characteristics of the MEDIPIX3 chip are listed in table 1. Additional features of the MEDIPIX3 chip which are of interest for SAXS experiments on synchrotron beamlines are listed in the following sections.

| Table 1 Basic specifications of a MEDIPIX3 read-out chip |
|----------------------------------------------------------|
| Pixel size | 55 µm x 55 µm |
| Format | 256 x 256 pixels |
| Active area | 1.41 x 1.41 cm² |
| Count rate per pixel | 5x10⁵ counts/s @ 20% dead time |
| Count rate per mm² | 1.65 x 10⁸ count/s @ 20% dead time |
| Counter depth | Configurable 1,4,12,24 |
| Noise level | 70 e- rms (single pixel mode) |
| | 144 e- rms (charge summing mode) |
| Power consumption | <1.5 W |

1.1. Charge-sharing effect suppression

The MEDIPIX3 chip can be operated in the so-called “Charge Summing Mode” which prevents interacting X-rays from being detected more than once or from not being detected. This is performed by introducing interconnection between pixels so that analogue signals are summed in clusters of four pixels before in-pixel arbitration logic allocates a single hit to the interacting X-ray. This scheme maintains the spatial resolution of 55 µm. Since the signal from four read-out channels is summed before performing signal discrimination, rms noise which adds up quadratically is twice the rms noise present when operating the detector in Single Pixel Mode, where pixels work independently from each others. Charge Summing Mode therefore results in an increased noise level which leads to higher minimum detection levels compared to Single Pixel Mode.
1.2. Colour-mode operation
Each 55 µm x 55 µm pixel of the MEDIPIX3 chip contains 2 discriminators and 2 counters. In Colour Mode, pixels are grouped in 2x2 clusters to form 110 µm x 110 µm detecting elements each containing 8 counters associated with 8 discriminators. Since these 8 discriminators can be programmed with different discrimination thresholds, the detector can perform energy-sensitive (or “colour”) X-ray imaging. This Colour Mode with 8 energy bins can be implemented in Single Pixel Operation where pixels operate independently as well as in Charge Summing Mode. Charge Summing Mode will suppress the effect of charge sharing on energy resolution while maintaining a spatial resolution of 110 µm x 110 µm corresponding to the size of the 2x2 pixel clusters.

1.3. Continuous read-write mode
A particular feature of MEDIPIX3 pixel architecture is the presence of two configurable 12-bit counters per pixels. These two counters can be operated separately and associated with a single discriminator. This allows continuous image acquisition without dead-time between frames since one counter can be read-out when the other is counting. In this mode of operation, a dead-time free frame rate of at least 2 kHz can be achieved with a 12-bit pixel depth. Counters can be configured to operate with one bit depth, allowing a dead-time free frame rate of 30 kHz. These two counters can also be combined to provide a pixel bit depth of 24 bits.

1.4. Option for edgeless tiling
MEDIPIX3 I/O architecture includes Though Silicon Via (TSV) pads in addition to wire-bond pads. TSV is a recently developed interconnection technique where signals are transferred from one side of a silicon chip to the other by drilling and metal plating via connections passing through the silicon thickness. The wire-bond pad section of the MEDIPIX3 chip can be diced away and TSV pads used to connect I/O, ground and sensor bias. This feature allows MEDIPIX3 to be four-side buttable and reduces the percentage of inactive area in a multi-chip detector assembly.

4. MEDIPIX3 data acquisition system based on a FPGA development kit
The MEDIPIX3 read-out chip must be interfaced with read-out electronics via LVDS I/O communications lines. A simple read-out set-up, shown in figure 3, is under design at the Diamond Light Source, based on a National Instruments PXI-7952R FlexRIO FPGA development kit including a Virtex-5 FPGA and 128 MB of onboard DDR2 DRAM. This set-up will allow image acquisition from a single MEDIPIX3 detector assembly at full frame rate and testing of the various modes of operation of the chip. It will also allow the development and test of calibration procedures such as equalization of discriminator thresholds across the chip. The chip carrier board is connected to an interface supplying chip bias voltages and performing LVDS to LVTTL conversion of I/O lines to allow the interfacing of the chip with the FPGA card. The FPGA and RAM module is connected to a PCI bus capable of 60 Mbytes/s data transfer rates.
5. Conclusion
The MEDIPIX3 chip developed by the CERN based international collaboration offers a number of innovative design features such as small pixel size with charge-sharing effect suppression, potential for edgeless tiling, high frame rate without dead-time between frames and colour mode operation. Read-out electronics are under development at Diamond Light Source to operate a single-chip detector. The long-term goal of such project is to exploit the features of MEDIPIX3 by developing multi-chip modules covering a large active area. Synchrotron applications such as coherent diffraction could benefit from the pixel size and speed of such a detector. A modular design could also be scaled to fulfil the detector requirements of various applications including SAXS where a fast frame rate photon counting detector would overcome the limitations of CCD-based detectors and allow time-resolved experiments currently performed with gas detectors.

6. References
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