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The Design of The Moebius Mod-6 Counter Using Electronic Workbench Software

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Abstract

The article proposes the design, testing and simulations of asynchronous counter directly Moebius modulo 6. We use JK flip-flop circuits because they are of order 2 and no state of indetermination. The circuit diagram drawing is very simple, resulting from mathematical calculations and logical function minimization condition. Testing and simulation of a counter we achieve using Electronic Workbench software. Counter for checking scheme Electronic Workbench has a "LED indicator" that "light up" in exceeding the 2.5V (TTL logic 1) and below this level remains "off". With this "LED indicator" is very easy to follow table states the counter.

Keywords: Moebius counter, mod-6, design, testing, functional state, J-K flip-flop

1. Several introductory notions on the Electronics Workbench Software

The Electronics Workbench programme, developed by the company Interactive Image Technologies Ltd. is a CAD application ("Computer Aided Design"). It is the same company that merges in 2005 with National Instruments becoming National Instruments Electronic Workbench Group. This new Company develops another version of the program, named MultiSim, an application superior to the Electronic Workbench soft, but maintaining

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most of its characteristics. It is intended for the design and simulation of electrical and electronic circuits. Besides the creation of circuits and the simulation of their functioning with the help of different indicating symbols, of measuring devices, power supplies and signal generators. The programme allows the performance of some complex analysis on the operation of the electronic circuits (the direct voltage display in the marked points of the diagram, the lay-out of the amplitude-frequency and phase-frequency characteristics, the analysis of transient operation, the display of the signal harmonic components, the waveform, etc.) for digital circuits. It provides TTL logic levels (indicator +V_{cc} used in conducting logic diagrams of the counter in this paper) as well as CMOS logic levels (indicator +V_{dd}). In order to simplify, we can use at the digital circuit output a so-called „indicator lamp”, which in case of ignition (red in the present paper) indicates the logic value 1. Else, if not lit, it indicates the logic value 0. It is very useful in testing the presented counter diagram, because we can easily follow the correlation between the states table and the logical sequence of the states at the counter output at each clock pulse. Basically, this type of indicator confirms or disproves the proper functioning of the counter through its „ignition”. Figure 1 presents a representative image of the Electronic Workbench testing and simulation software. In the simulation and testing of the counter we used the Electronic Workbench soft, version 5.12; but there are much newer versions (10.1 being the last one). We should mention is that if an electronic component does not exist in the libraries of the respective programme, then it can be created, almost all of its functional characteristics and basic properties can be developed, it can be saved in the Electronic Workbench libraries and used in simulations.

2. The Counters concept

This Counter is a special one, as opposed to traditional direct counters. Part of counters with binary sequences of length 2^n (n is the number of bits) is similar to a ring counter, but it "twisted tail" to counter the ring has Hamming length= 1. The numerator in the ring with Hamming length=2 and was therefore widely used in implementing FPGA’s, especially those made by the company Xilinx. These types of counters are easily programmed using
modern programming languages used for FPGA’s programming Xilinx firmed.

According to the mathematical formula $n = \lceil \log_2 p \rceil + 1 = \lceil \log_2 6 \rceil + 1 = 3$, we need 3 bits in order to represent the functional states of a direct counter in $p=6$. Thus, we are talking about a 3-bit counter. In the formula, we noted with $n$ the number of required bits, and $\lceil \cdot \rceil$ is the mathematical function integer part. This mathematical relation is established for the Boolean algebra, but only valid for $p \neq 2^n$, thus when $p$ is a power of 2. The number of bits required for the representation of the counter functioning states (modulo $2^p$/MOD-2$^p$) is $n$. There are two types of mathematical theories in the counter design: one for the case in which $p$ is a power of 2, and a more general one, when $p \neq 2^n$, which we will approach in this paper.

For the 3 bits (noted here with $Q_0, Q_1, Q_2$), the complete number of states at time $t$ is of course 8. First, however, we need to design a direct counter that should count to 6 (MOD-6). Hence, we will have two redundant states at time $t+1$, versus time $t$.

This is rendered in table 1 presented in the following paragraphs (the table of states for this type of counter).

We propose to implement this type of MOD-6 J-K flip-flop direct counter because, together with the T type flip-flops, the J-K flip-flops are usually used in creating the counters (being flip-flops order 2).

### 3. Mathematical Calculation, the Design And Testing Of The Moebius Mod-6 Counter

First we build the table of logical functioning states of the counter (Table 1).

Unlike the classic counters that count directly, we also have less known version of a mod-6 counter design, called the Moebius version.

It has a rather general character, the Moebius counters belonging to the category $2n$, also known as the twisted ring counters. For this reason they are also called Johnson counters.

Next we will present the flowchart of this version according to Moebius rules of elaborating the states truth table: instead of the redundant states “x” from a regular table built for a direct classic counter (associated to the clock pulses 6 and 7). We can consider as redundant the states associated to the clock pulses 3 and 6, i.e. the logic states “2” and “5”, and Table 1 of states is the following:

| Table1. The table of logical functioning states of the counter |
|---------------------------------------------------------------|
| State / Number of clock pulses | State at moment $t$ | State at moment $t+1$ | Observations |
|--------------------------------|------------------|------------------|---------------|
| Bits →                         | $Q_0$ | $Q_1$ | $Q_2$ | $Q_0$ | $Q_1$ | $Q_2$ |               |
| state 0/ “1”                  | 0    | 0    | 0    | 0    | 0    | 1    |               |
| state 1/ “2”                  | 0    | 0    | 1    | 0    | 1    | 1    |               |
| state 2/ “3”                  | 0    | 1    | 0    | x    | x    | x    | Redundant state |
| state 3/ “4”                  | 0    | 1    | 1    | 1    | 1    | 1    |               |
| state 4/ “5”                  | 1    | 0    | 0    | 0    | 0    | 0    | Redundant state |
| state 5/ “6”                  | 1    | 0    | 1    | x    | x    | x    |               |
| state 6/ “7”                  | 1    | 1    | 0    | 1    | 0    | 0    |               |
| state 7/ “8”                  | 1    | 1    | 1    | 1    | 1    | 0    |               |

Thus, considering the previous state table, for the MOD-6 direct counter, as well as the J-K flip-flop equations, we need to calculate and minimize (using the Veitch-Karnaugh diagram) the logic functions of the state transition. That is, $Q_i^{t+1}$ will be a logic function dependent on the variables $\overline{Q_i^t}$ and $Q_i^t$ which must be brought to the mathematical form of the equation that characterizes a J-K flip-flop:

$$Q_i^{t+1} = J_i \cdot \overline{Q_i^t} + K_i \cdot Q_i^t,$$

(2.1)

and $i = 0, 1, 2$ in the case given.

Hence, minimizing with the Veitch-Karnaugh diagrams, we will obtain the state equations for the variables $Q_{2}^{t+1}$. 


Thus, $Q_{2}^{t+1} = \overline{Q_{2}^{t}} \cdot Q_{1}^{t} + Q_{2}^{t} \cdot Q_{1}^{t}$, i.e. the variables $J_{2}$ and $K_{2}$ will have the values:

\[
\begin{cases}
J_{2} = Q_{1}^{t} \\
K_{2} = Q_{1}^{t}
\end{cases}
\]  \hspace{0.5cm} (2.2)

For $Q_{1}^{t+1}$ we have:

Thus, $Q_{1}^{t+1} = Q_{1}^{t} \cdot Q_{0}^{t} + Q_{1}^{t} \cdot Q_{0}^{t}$, i.e. the variables $J_{1}$ and $K_{1}$ will have the values:

\[
\begin{cases}
J_{1} = Q_{0}^{t} \\
K_{1} = Q_{0}^{t}
\end{cases}
\]  \hspace{0.5cm} (2.3)

For $Q_{0}^{t+1}$ we have:

Thus $Q_{0}^{t+1} = \overline{Q_{0}^{t}} \cdot \overline{Q_{2}^{t}} + Q_{0}^{t} \cdot \overline{Q_{2}^{t}}$ (we deliberately minimized the expression like this); i.e. the variables $J_{0}$ and $K_{0}$ will have the expressions:

\[
\begin{cases}
J_{0} = \overline{Q_{2}^{t}} \\
K_{0} = \overline{Q_{2}^{t}}
\end{cases}
\]  \hspace{0.5cm} (2.4)

Therefore, according to the relations 2.2, 2.3, 2.4, the 3 bits diagram will be:
We can notice that the name *twisted ring counter* is justified.

This type of counter is a counter belonging to those with binary sequences of length $2n$, a twist taking place after these "$n" states (according to the Moebius strip). The $n$ states work after the Gray code, i.e. only one state bit is modified between consecutive states! In the present paper the number of bits is $n=3$. For this reason we excluded the states 2 and 5! This can be observed in Table 1 as well. The initial state in our case is state "0" at moment $t$ or "4" at moment $t+1$ (see Table 1 of the direct MoebiusMOD-6 counter states).

The functional states of the counter, according to the previous table, are tested and checked within the Electronic Workbench program and presented in the next figures.

The logical functional states are presented exactly in the order of their appearance according to the logic sequence of clock pulses (from 1, 2,..., 8); the switching of flip-flops is made on the decreasing front of the pulses:

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**Fig.2** Initial state, corresponding to the 5th clock pulse (it’s an even state).

**Fig.3** State corresponding to the binary number „1” at moment $t+1
Fig. 4 State corresponding to the binary number „3” at the moment $t+1$

Fig. 5 State corresponding to the binary number „7” at the moment $t+1$

Fig. 6 State corresponding to the binary number „6” at the moment $t+1$
After this last counting sequence we return to the state corresponding to number „0” represented on 3 bits at moment \( t+1 \). It does not pass through the states corresponding to the clock pulses „3” and „6” at moment \( t+1 \) because they are redundant as seen in Table1 (the counter is MOD-6, thus we have 8-2=6, 2 being the number of redundant states).

4. Results and observations

As regards the diagram chosen in the design of the synchronous MoebiusMOD-6 counter, the states corresponding to the clock pulses „2” and „5” were eliminated from the functioning of the counter because it breaks the principle of the Gray code, increasing the number of errors, such as: combinational hazard. The Gray coding supposes a fast calculation and programming, being used in most calculators and programming program! The flip-flops are synchronized from the same clock pulse, the counter is synchronous. There are also asynchronous versions of Moebius MOD-6 counters. Consequently, we can generalize schemes of Moebius (Johnson) counters, similar to the principle of mathematical induction. It can develop general schemes, according to the issues stated and verified at second paragraph, corresponding to states \( 2^n \). This facilitates us to pass to general schemes of Moebius MOD-\( 2^n \) counters, being very useful in the teaching process. This is why we started with a particular case of Moebius MOD-6 counter (\( n=3 \)). Moreover, a general scheme with \( n \) flip-flops where \( n \) is a high number (almost infinite) cannot be simulated and tested in Electronic Workbench. An example of a state table for \( 2n \) clock pulses that has a matrix structure is given by the following relation:

\[
\begin{bmatrix}
0 & 0 & \ldots & 1 \\
0 & 0 & \ldots & 1 \\
0 & 0 & \ldots & 1 \\
0 & 0 & \ldots & 1 \\
\vdots & \vdots & \ddots & \vdots \\
1 & 1 & \ldots & 1 \\
1 & 1 & \ldots & 1 \\
1 & 1 & \ldots & 1 \\
1 & 1 & \ldots & 1 \\
\end{bmatrix}
\]

\( (4.1) \)

The relation is a matrix one, type \( (2n\text{-}lines}) \times \( (n\text{-}columns}) \), being configured from two blocks. Obviously, the first matrix block type \( n \times n \) (the block of odd number) is completed with logic 1 starting from \( LSB \) (Last Significant Bit) to \( MSB \) (Most Significant Bit), from top to bottom.

We notice that it has a symmetrical structure compared to the secondary diagonal of the representation matrix.
The second matrix block, that of odd numbers, type \((n-l) \times n\) is completely reversed, with logic 1 from MSB to LSB, from top to bottom. This has the same type of symmetry.

The area of junction of the two blocks, where the highest even number is a neighbour with the highest odd number, is a „twist“ area. This is why we deal with a Moebius counter.

Through mathematical induction we can obtain a general scheme for a **synchronous Moebius MOD-2n counter**, presented in the following figure 8:

![General scheme for a synchronous Moebius MOD-2n counter](image)

The switching of the clock signal from logic 1 to 0 within the Electronic Workbench program is made with the space key, as noticed in the presented figures. However, any other key may be set. The structure of this type of counter is simple, usually being a series of flip-flops, „the twist“ from the first to the last flip-flop in the line. We also notice that they can be easily implemented using the *shift registers*. Also, D-flip-flops can be used in the implementation of logical schemes, the resulted schemes being moresimple. Such a scheme together with the signal diagrams afferent to the logical Boolean functions \(Q_2\), \(Q_1\) and \(Q_0\) is shown in figure 9:

![Scheme together with the signal diagrams afferent to the logical Boolean functions](image)

We preferred, as mentioned at point 1, the J-K flip-flops because they are the best, being of order 2 without representing states of indetermination. In figures, \(Q_2\) is *LSB* and \(Q_0\) is *MSB*, and here the switching of the flip-flops is made on the decreasing front of the clock signal.
5. Conclusions and future directions

We can concluded, that the reason why we choose to design Moebius counter modulo 6, is because it allows the extension study some more general scheme Moebius count modulo p (where p is an even number). Although we use an older version 5.12 of the Electronic Workbench software in simulation and testing, it is sufficient for scientific and teaching purpose. Regarding the practical performance of the counter, it can be easily implemented in logic TTL using maximum two integrated circuits of 14 pins/chip (IP 74107 which is an integrated circuit existing in the Electronic Workbench bibliotheca, containing two J-K flip-flops) or using two integrated circuits of 16 pins/chip (IC 7473, 7476 or 7478 existing in the same libraries having two J-K flip-flops on the chip). As applicable and directions for future we enumerate the study and design of the shift registers, FPGA manufactured by Xilinx Company programming and simulations of other types of Moebius and ring count for student use. As future recommendation we can suggest other simulation program’s such us PSpice, Multisim, Proteus 7.9. software, etc.

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