Memory effects in black phosphorus field effect transistors

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Abstract
We report the fabrication and the electrical characterization of back-gated field effect transistors with a black phosphorus (BP) channel. We show that the hysteresis of the transfer characteristic, due to intrinsic defects, can be exploited to realize non-volatile memories. We demonstrate that gate voltage pulses allow to trap and store charge inside the defect states, which enable memory devices with endurance over 200 cycles and retention longer than 30 min. We show that the use of a protective poly(methyl methacrylate) layer, positioned on top of the BP channel, does not affect the electrical properties of the device but avoids the degradation caused by the exposure to air.

1. Introduction

Black phosphorus (BP) is a layered material in which, similarly to graphite, individual atomic layers are held together by van der Waals interactions [1]. In the single-layer limit, BP is also known as phosphorene and has a numerically predicted direct band gap of \( \sim 2 \) eV at the \( \Gamma \) point of the first Brillouin zone [2]. With increasing number of layers, the interlayer interactions reduce the bandgap to a minimum of \( 0.3 \) eV for bulk BP [3] moving the direct gap to the Z point [4].

Similarly to transition metal dichalcogenides [5–12], BP’s band structure has attracted a lot of attention for possible electronic and optoelectronic applications. Indeed, the presence of a finite bandgap makes BP suitable for the realization of field-effect transistors (FETs), and the thickness-dependent direct bandgap may lead to applications in optoelectronics, especially in the infrared region. Several devices have already been proposed and studied; Li et al [13] achieved reliable transistor performance with five orders of magnitude drain current modulation and charge-carrier mobility up to \( \sim 1000 \) cm\(^2\) V\(^{-1}\) s\(^{-1}\) obtained from 10 nm thick samples. Ren et al [14] used BP nanosheets to realize self-powered photodetectors with superior photoresponse activity under light irradiation and environmental robustness, showing that BP is a promising building block for optoelectronic devices. One of the practical problems that still needs to be solved to obtain high performance is to optimize the contacts between the metallic leads and the BP. The choice of the metal is of fundamental importance as it is mainly responsible for the height of the Schottky barrier that is usually formed. Chang et al [15] investigated titanium contacts on BP based upon the theory of thermionic emission proposing a useful method to avoid the effects of hysteresis on the extraction of the Schottky barrier height. More recently, Li et al [16] reported top-gated submicron BP transistors with local contact bias electrodes to induce doping in the contact region resulting in reduced contact resistance. Moreover, BP has been also proposed for solar cells [17], as humidity sensor [18], or for live cell imaging [19].

A remarkable application of BP has been in the field of memory devices. Common non-volatile FET-based memories use a charge-trapping layer to accumulate and retain the electric charge induced by a gate pulse. Similar devices, with a channel based on several 2D-materials, including BP, have been already proposed and demonstrated. In particular, Feng et al [20] reported that few-layer BP channel
FETs with a $\text{Al}_2\text{O}_3$/HfO$_2$/Al$_2$O$_3$ charge-trapping gate stack enable memory devices with a programming window exceeding 12 V, due to the extraordinary trapping ability of high-$k$ HfO$_2$, and endurance exceeding 120 cycles. Tian et al. [21] used a similar structure, where the charge trapping layer consisted only of Al$_2$O$_3$, to demonstrate an ambipolar BP charge-trap memory device with dynamically reconfigurable and polarity-reversible memory behaviour. In such a device, the polarity of the carriers in the BP channel can be reversibly switched between electron- and hole-dominated conduction allowing four different memory states and, hence, two-bit per cell data. However, it had already been demonstrated by Li et al. [22] that Al$_2$O$_3$ capping can significantly degrade transistor performances, resulting in lower on-state current and ON/OFF ratio. Lee et al. [23] reported few-layered BP-based nonvolatile memory transistor with a poly(vinylidenedifluoride-trifluoroethylene) (P(VDF-TrFE)) ferroelectric top gate insulator. They also combined this device with an n-type MoS$_2$ nanosheet obtaining a memory inverter circuit that displayed a clear memory window of 15 V and memory output voltage efficiency of 95%. Finally, Lee et al. [24] showed that gold nanoparticles as charge trapping layer for mechanically-exfoliated few-layered BP FETs enable large memory window (58.2 V), stable retention ($10^4$ s), and cyclic endurance (1000 cycles).

However, the practical implementation of these promising devices is hindered by the intrinsic instability of mono- and few-layer BP. While bulk crystals are quite stable in air, BP flakes thinner than 10 nm degrade in few days, or even in few hours if the thickness is reduced to a single layer [1]. Indeed, when exposed to oxygen, devices obtained through mechanical exfoliation [25] or solvent exfoliation [26] of bulk crystals are affected by fast oxidative degradation [27, 28]. Moreover, the degradation process can be enhanced by exposure to light through photo-oxidation [29]. To tackle this issue, different stabilization processes have been tried. As first attempt, BP has been functionalized through TiO$_2$, Al$_2$O$_3$, titanium sulfonate ligand (TL$_4$), polyimide, or aryl diazonium [30–34]. Encapsulation with other 2D materials, such as graphene and boron nitride, has been considered as well [35]. Furthermore, it has been reported that the use of ionic liquids can suppress BP degradations for months [36].

Although these first approaches have provided encouraging results, an efficient stabilization of BP, also compatible with standard fabrication processes of high performance devices remains still an ongoing challenge.

In this work, we report the fabrication and the electrical characterization of back-gated BP FETs. We exploited the presence of intrinsic and BP/SiO$_2$ interface defects to realize non-volatile memories with good endurance and retention properties. By comparing samples exposed directly to the air with others covered by poly(methyl methacrylate) (PMMA), we demonstrate that PMMA does not affect the electrical properties of the devices but prevents the channel degradation at least for 1 month.

2. Materials and methods

Figure 1(a) shows the crystal structure of BP where the layered structure is composed of sheets with the phosphorus atoms arranged in a puckered honeycomb lattice. Ultrathin BP flakes were exfoliated from bulk BP single crystals (Smart Elements) using a standard mechanical exfoliation method by adhesive tape. The flakes were transferred onto degenerately doped p-type silicon substrates, covered by 90 nm thick SiO$_2$, on which they were located through optical microscopy. Because of the rapid degradation of BP in ambient conditions a first roughly determination of the thickness of the BP flakes is obtained via their optical contrast prior the PMMA capping layer was deposited. By this, we estimate the thickness of the flakes to be about 10 nm, meaning that the bandgap of BP has already reached its bulk value of around 0.3 eV [37]. This value has been also confirmed by atomic force microscope measurements after PMMA removal revealing a thickness of 8.5 nm. A standard photolithography process followed by electron beam evaporation was used to deposit 10 nm Cr/100 nm Au electrodes, as shown in figure 1(b). A back-gate contact was formed covering the scratched area of the Si substrate with silver paste. We used the standard E-Beam resist AR-P 632.04 by Allresist for the capping layer and spincoated it onto the samples with 4000 rpm for 60 s. With these parameters the thickness of the PMMA capping layer is around 60 nm.

Electrical measurements were carried out in two- and four-probe configurations in a Janis ST-500 Probe Station equipped with four nanoprobe connected to a Keithley 4200 SCS (semiconductor characterization system), working as source-measurement unit with current and voltage sensitivity better than 1 pA and 2 µV, respectively. The electrical measurements were performed by lowering the pressure from 1 bar (room pressure) to $10^{-7}$ mbar. The air in the chamber was evacuated by a rough and a turbo pump. To evaluate the electrical response under light the device was irradiated through a super-continuous white laser source (NKT Photonics, Super Compact, wavelength ranging from 450 to 2400 nm, at 50 mW mm$^{-2}$).

3. Results and discussion

Figure 2(a) reports a schematic of the device showing a standard four-probe characterization set-up. The current ($I_{on}$) is forced between the outer contacts
Figure 1. (a) Crystal structure of few-layer BP. (b) Optical image of the device showing a BP flake covered by four Cr/Au contacts.

Figure 2. (a) Schematic of the setup used for the four-probe electrical characterization. The current ($I_{xx}$) is forced between the outer contacts while the voltage drop ($V_{ds}$) is measured between the inner contacts. (b) $I-V$ characteristics measured in two- and four-probe configuration. (c) Output characteristic of the device recorded in two-probe configuration with the gate voltage ranging from $-60$ to 60 V (red lines are referred to positive gate voltages). (d) Transfer characteristic measured over a loop of the gate voltage between $-60$ and 60 V. The dashed red line represents the linear fit used to estimate the field effect mobility. The inset shows the transfer curve with the current on a logarithmic scale.

while the voltage drop ($V_{ds}$) is measured between the inner contacts. Figure 2(b) shows the characteristics for both four-probe ($I_{xx} - V_{ds}$) and two-probe ($I_{ds} - V_{ds}$) configurations resulting in a channel resistance of 3.5 and 3.6 kΩ, respectively. Since the difference between the two methods is less than 3%, indicating that the contacts are ohmic with low contact resistance [38, 39], in the following we use the two-probe configuration for easier measurements. The electrical characterization of the BP transistor at room temperature is reported in figures 2(c) and (d).

The output characteristics, i.e. the drain-source current ($I_{ds}$) as a function of the voltage drop between two inner contacts ($V_{ds}$) with the gate-source voltage ($V_{gs}$) as control parameter, exhibit a linear behaviour. The application of a negative gate bias leads to an increase of the channel current, typical of a p-type device, and does not affect the linearity of the
$I_{ds} - V_{gs}$ characteristics [39]. The transfer characteristic, i.e. the $I_{ds} - V_{gs}$ curve measured at fixed $V_{th} = 10$ mV over a loop of the gate voltage is reported in figure 2(d), confirming the p-type behaviour, with a modulation of about two orders of magnitude. We did not fully reach the off state of the transistor in the applied voltage range, which was intentionally limited to avoid the breakdown of the gate dielectric. Considering the non-linear behaviour of the transfer characteristics, the channel current can be expressed as:

$$I_{ds} = \frac{W}{L} \mu_{FE} C_{ox} V_{ds} \left| V_{gs} - V_{th} \right|^\alpha$$

where $W = 10 \ \mu m$ and $L = 5 \ \mu m$ are the channel width and length, respectively, $\mu_{FE}$ is the field-effect mobility, $C_{ox} = 3.84 \times 10^{-8} \ F \ cm^{-2}$ is the capacitance per unit area of the gate dielectric, $V_{th}$ is the threshold voltage and $\alpha \geq 1$ is a dimensionless parameter that accounts for a possible $V_{gs}$-dependence of the mobility [40]. According to equation (1), when the $I_{ds} - V_{gs}$ curve is linear, $\alpha = 1$, and the mobility can be obtained as:

$$\mu_{FE} = \frac{L}{W C_{ox} V_{ds}} \frac{dI_{ds}}{dV_{gs}}.$$  

From the linear fit, we obtained a relatively high $\mu_{FE} \sim 30 \ cm^2 V^{-1} s^{-1}$, considering that the sample was not subjected to any functionalization, that is slightly below both the theoretically predicted [41, 42] and the experimentally measured mobilities in similar devices [43, 44]. We note that such a mobility is higher or comparable with the one obtained in SiO$_2$ back-gate FETs fabricated with other 2D materials [45–48].

The large hysteresis width, $H_w \sim 60 \ V$, here defined as the $V_{gs}$ difference corresponding to the current of 1.5 $\mu A$, is mainly due to charge trapping impurities and has already been reported for similar devices [22, 49–51]. Gate-induced hysteresis can be ascribed to charge transfer from/to intrinsic and extrinsic trap states. Intrinsic traps correspond mostly to BP crystal defects such as phosphorus vacancies or grain boundaries. In particular, Li et al [52] demonstrated that single and double phosphorus vacancies can deeply affect BP electronic properties. When a single vacancy is present, a structural deformation occurs and P atom below the vacancy site moves toward the direction of the vacancy site, forming two bonds with nearby P atoms in the layer of vacancy. The main outcome of this process, that has a formation energy of 2 eV, is the splitting of the valence band into two bands. Double vacancy defects resulted to have a more stable configuration with a minimum formation energy of 0.72 eV/vacancy, that is strongly correlated with the large structural deformation. Their presence leads to sp$^3$ hybridization for P atom resulting in the delocalization of the valence band state. Guo et al [53] have reported that grain boundaries have formation energies ranging from 0.90 to 2.43 eV nm$^{-1}$, much lower than those in graphene, but do not severely affect the electronic properties of BP. Indeed, in presence of grain boundaries the band gap of perfect BP is preserved and the electron mobilities are only slightly reduced. Extrinsic traps are related to environmental adsorbates, like water and oxygen molecules, defects located at the metal/BP interface, and at the BP/SiO$_2$ interface [22].

Although oxidation of the surface involves the dissociative chemisorption of oxygen that causes the decomposition of BP and the decrease in FET performance, we expect that water and oxygen play a marginal role in the formation of hysteresis because the electrical measurements were carried out in high vacuum to remove the surface adsorbates. Thus, traps at the BP/SiO$_2$ interface, intrinsic BP defects and border traps in SiO$_2$ as well as mobile charges in the SiO$_2$ layer are most likely responsible for the device hysteresis.

To better understand the origin of hysteresis we measured the transfer characteristics at different sweeping times. Figure 3(a) shows several transfer characteristics with $H_w$ increasing as function of the voltage sweep duration in the range 12–322 min. The exponential fit, shown in figure 3(c), reveals a RC-growth with a single time constant $\tau = 191 \ min$ (R and C are the total resistance and capacitance of the circuit). Even if their contribution cannot be completely neglected, such a long characteristic time reduces the probability that BP/SiO$_2$ interface traps play an important role in the hysteretic behaviour. Indeed, it has been demonstrated in several theoretical and experimental studies that these traps present fast saturation time constants and their contribution is relevant mainly in very degraded devices [54–56]. Then, slow trap states can be ascribed to both BP and SiO$_2$ trap states. Particularly, slow border traps in SiO$_2$ have already been reported and attributed to trivalent silicon dangling bonds or hydrogenic defects [57]. From the time constant $\tau$, it is possible to evaluate the involved capacitance as $C = R/\tau$, where R is the inverse of transconductance $g_m = \partial I_{ds}/\partial V_{gs} \sim 0.3 \ nS$. We obtain $C \sim 3 \ \mu F$, which is higher than the gate oxide capacitance, on the order of $pF$, implying that the trap-related capacitance is the dominant one.

Such a capacitance can also be obtained through the sub-threshold swing SS that is the gate voltage change corresponding to one-decade increase of the transistor current. Indeed, SS is a function of the charge trap capacitance and the depletion layer capacitance according to the following relation:

$$SS = \frac{dV_{gs}}{d\log(I_{ds})} \approx \log(10) \frac{kT}{q} \left( 1 + \frac{C_T + C_{DL}}{C_{ox}} \right)$$

where, $k$ is the Boltzmann constant, $T = 300 \ K$ is the temperature and $q$ is the electric charge. By neglecting the depletion layer capacitance, $C_{DL}$, with respect to the charge trap capacitance, $C_T$, (a reasonable
Figure 3. (a) Transfer characteristics recorded at different sweeping times ranging from 12 to 322 min. The horizontal red line indicates the current value used to evaluate the hysteresis width. (b) Transfer characteristics measured under supercontinuous white laser illumination (black line) and in the dark every 10 min after the laser was switched off. (c) Exponential fit of the hysteresis width as function of the gate voltage sweeping time, revealing a time constant of 191 min. (d) Double exponential fit of the hysteresis width obtained from figure (b) revealing a fast characteristic time of 5 s and a long one of 42 min.

assumption considering the low modulation of the current) and, having obtained SS ∼ 30 V dec⁻¹, we estimated a trap capacitance, \(C_T \sim 20 \mu F\), that is consistent with the one previously obtained.

To corroborate the hypothesis that slow trap states contribute to hysteresis we measured the transfer characteristic while irradiating the device with a super-continuous white laser source at 50 mW mm⁻²; after that, we repeated the measurements in the dark every 10 min. Figure 3(b) shows that under illumination (black line) the device conductance and the hysteresis width are enhanced. This result is expected as the illumination causes both the generation of electron–hole pairs and excitation of trapped charges, which increase the carrier concentration in the material. Charged traps, emptied of free carriers, induce an enlargement of the hysteresis. By repeating the measurements in the dark, the conductance as well as the hysteresis decrease until they stabilize after about an hour. Figure 3(d) shows how \(H_w\) varies after light irradiation. The best fit is obtained through a double decreasing exponential, one with a small time constant (≈5 s) and a predominant one with a long characteristic time (≈42 min). The fast time constant is related to electron–hole pair recombination, while the longer one supports the conclusion that hysteresis is dominated by intrinsic deep slow traps.

Although the presence of trap states is detrimental to FET performance, we here show that the charge trapping can be exploited to realize a memory device. We highlight that in such a way we realize non-volatile memory devices with good performance without using an additional charge-trapping layer, but just exploiting the presence of BP and SiO₂ defects.

Figure 4(a) shows the transient behaviour of the device, investigated through a series of \(V_{gs} = \pm 60\) V pulses while the \(I_{ds}\) current is monitored over time. While the gate pulse is in the high positive or negative state the channel current is not constant, but it increases/decreases in an exponential way. This is due to trapping/detrapping of charge inside the trap states. When the gate voltage is set to 0 V, the current tends to return to its initial value. However, the transient behaviour after a positive and a negative gate pulse shows that \(I_{ds}\) stabilizes at two different values, distinct from the initial one (figure 4(b)). This separation is retained for a time longer than 30 min, which
Figure 4. (a) Channel current (black line) recorded under gate pulses (red line) at ±60 V showing single set–read–reset–read cycles of the non-volatile memory. (b) Transient behaviour of the channel current after the gate pulses at ±60 V revealing a retention time longer than 30 min. (c) Repeated set–read–reset–read cycles of the memory device showing an endurance over 200 cycles. (d) Repeated set–read–reset–read cycles measured after a month air exposure of a device covered with PMMA (black line) and an uncovered one (red line). (e) Transfer characteristics of two BP FETs, one covered with PMMA (black line) and the other exposed to air (red line), recorded immediately after the device fabrication. (f) Transfer characteristics of the same devices of (e), measured after one-month exposure to air.

is comparable with the retention time observed in non-volatile BP memories with charge trapping layers [20, 21, 24]. Then, we tested the endurance of the device by continuously applying pulses of 1 min width at $V_{gs} = ±60$ V. Figure 4(c) shows that the device response is stable after 200 cycles, consistent with similar non-volatile memories realized with other 2D materials [46].

Finally, since the main obstacle to the realization of BP-based devices is the lack of stability in air, we covered several BP devices with a PMMA layer. Then, we performed endurance tests on two similar devices, with and without PMMA. Initially, the devices have similar behaviour but, after exposure to air for a month, the PMMA protected device maintains its current while the unprotected device shows evident signs of current deterioration (figure 4(d)). Figure 4(e) compares the transfer characteristics of the PMMA covered and uncovered devices immediately after the fabrication process. The similarity of the two curves confirms that encapsulation by PMMA does not significantly alter the BP device. The transistor covered with PMMA has a slightly larger hysteresis because PMMA can contribute to charge
trapping. Indeed, it has been reported by Li et al. [58] that the PMMA layer induces positive fixed charges at the interface that need to be balanced by an equal amount of charges with opposite sign in the BP. This process leads to a reduction of the effective Schottky barrier for electrons and to an increase of the effective Schottky barriers for holes, resulting in a negative shift of the charge neutral point and a reduction of the OFF state drain current. These changes have not been observed in this study as the transistor was monitored far from the OFF state where the effects of PMMA are less evident. Figure 4(f) shows the same transfer characteristics recorded after that both devices were left exposed to the air for a month. The device covered with PMMA does not show any signs of deterioration while the uncovered FET exhibits an evident reduction in conductivity and a much noisier current due to surface oxidation. This result confirms that PMMA encapsulation is a simple and effective method of avoiding the deterioration of air exposed BP memory FETs.

4. Conclusion

In conclusion, the fabrication and the electrical characterization of BP field effect transistors have been reported. The hysteresis width has been investigated as a function of the voltage sweep duration and during air exposure after irradiating the device with a super-continuous white laser source, revealing that the slow intrinsic trap states are the main responsible for the hysteretic behaviour. It has been demonstrated that it is possible to realize BP-based non-volatile memory devices without adding a dedicated charge-trapping layer to accumulate and retain the electric charge. Finally, encapsulating BP with a PMMA protective layer has been used as a simple way to preserve the electrical properties of the memory over a month. These results may pave the way for the realization of simple-to-make memory-type devices based on BP or others 2D materials with intrinsic defects. New studies will be dedicated to further investigate the protective role of PMMA as well as to explore other insulating materials, e.g. 2D h-BN, as the capping layer to enhance BP stability and charge storage capability for high performance memory devices compatible with standard fabrication processes.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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