Design of 9:2 compressor using FinFET

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Abstract. Multiplier is an essential component that is used commonly in any digital circuits. In general, for any digital circuits, multipliers occupy larger area; have long latency and their power consumption is more. Thereby, enhancing the performance of multipliers is quite important. Compressors are used to reduce the partial products so that the improved performance of multipliers can be achieved. In this paper, a new structure of 9:2 compressor is proposed in which the circuit is implemented with different combinations of 3:2, 4:2, 5:2 and 6:2 compressors. In this work, instead of bulk CMOS technology, circuits are implemented using FINFETs as they provide better gate control property, lower short channel effects. All the compressor circuits have been implemented using Cadence Virtuoso Simulator with FINFET 32nm technology. All the circuits are implemented to analyze the performance in terms of power, delay and transistor count.

1. Introduction

Arithmetic modules are essential in most of the digital circuits. In many complex executions, multipliers have been demanding, and imperative elements in governing the complete circuit efficacy when power estimation and speed are to be examined. Generally multipliers have three parts – generation of partial products, reduction of partial products and the final addition [2], [7]. The reduction of partial product consumes much time and more power. Several techniques were proposed to reduce the partial products. Among all those, usage of compressor technique has major benefits. And to achieve better performance, higher order compressors are considered instead of conventional compressors [5]-[6].

The basic idea of a n:2 compressor is that n operands are reduced to two, by adding and while keeping the sum and the carry separately, i.e. basically these compressors are implemented using full adders [3]. The fundamental compressor is 3:2 compressor. Using the lower order compressors, the higher order compressors could be implemented.

In this paper a new design of 9:2 compressor is proposed for better power efficiency and delay. Different models of 9:2 Compressor is built using XOR, MUX – Model 1, XOR-XNOR, MUX – Model 2, XOR, MUX implemented using NAND – Model 3, 4:1 MUX – Model 4 are implemented using Cadence Virtuoso Simulator and the technology used is 32nm. Here FINFETs are used in place of the bulk CMOS. Power, delay and PDP are also calculated for different models and the comparative results are shown.

2. Background

2.1. Functionality of n:2 Compressor

In an n:2 compressor, n operands are reduced to two keeping the sum and carry separate. n:2 compressor has X1,n primary inputs and C(n-1)n-3 carry inputs which are received from neighboring compressors. It generates Sum, Carry and Cout(n-3) as outputs. Its functionality is described by the equation (1) [9].
\[ X_1 + X_2 + X_3 + X_4 + \ldots + X_n + C_{in1} + C_{in2} + \ldots + C_{in(n-3)} = \text{Sum} + 2^*(C_{out1} + C_{out2} + \ldots + C_{out(n-3)} + \text{Carry}) \]  
\( (1) \)

9:2 compressor has total of 15 inputs of which \( X_{1-9} \) are primary inputs and the other inputs are \( C_{in1-6} \) which are received from neighboring compressors. It generates \( \text{Sum} \), \( \text{Carry} \) and \( C_{out1-6} \) as outputs. Its functionality is described by the equation (2).

\[ X_1 + X_2 + X_3 + X_4 + X_5 + X_6 + X_7 + X_8 + X_9 + C_{in1} + C_{in2} + C_{in3} + C_{in4} + C_{in5} + C_{in6} = \text{Sum} + 2^*(C_{out1} + C_{out2} + C_{out3} + C_{out4} + C_{out5} + C_{out6} + \text{Carry}) \]  
\( (2) \)

2.2 FinFET

Fin Field-effect Transistors was developed on double gate or multiple gate for the improvement of performance of certain parameters (mainly the size of the transistor), FinFETs are fabricated in 32nm, 22nm and recent 14nm technology. FinFET as an alternative to conventional bulk MOSFET, exhibits smaller Drain Induced Barrier Lowering (DIBL), smaller sub threshold swing and higher Ion/Ioff ratio by increasing electrostatic stability and reducing threshold voltage (VT) roll-off [1] [4]. FinFETs exhibit more drive current, achieve higher frequency for low power. The power reduction comes from high-drive standard cells and to operate with a lower supply voltage for given amount of leakage.

3. Proposed Design

In constructing the 9:2 compressor, 3:2 compressor is used as the main building block. 3:2 compressor is basically a full adder. Here the full adder is implemented using different combinations of XOR and MUX circuits. The 9:2 compressor circuit is as shown in Figure 1, is designed with four different models which are discussed as Model 1, Model 2, Model 3, Model 4, where 3:2 compressors are used. Here \( X_{1,3} \) given to 1\(^{st}\) 3:2 compressor, sum output of 1\(^{st}\) 3:2 compressor and \( X_{4,5} \) is given as input to the 2\(^{nd}\) 3:2 compressor, sum output of 2\(^{nd}\) 3:2 compressor and \( X_{6,7} \) is given as input to the 3\(^{rd}\) 3:2 compressor, sum output of 3\(^{rd}\) 3:2 compressor and \( C_{in3-4} \) is given as input to the 4\(^{th}\) 3:2 compressor, sum output of 5\(^{th}\) 3:2 compressor and \( C_{in5-6} \) is given as input to the 6\(^{th}\) 3:2 compressor, sum output of 6\(^{th}\) 3:2 compressor and \( C_{in5-6} \) is given as input to the 7\(^{th}\) 3:2 compressor. The outputs of 1\(^{st}\) to 6\(^{th}\) 3:2 compressors are \( C_{out1-6} \) respectively, the final Sum

![Figure 1. 9:2 compressor using 3:2 compressor](image-url)
and Carry are taken from the 7th 3:2 compressor. Internal 3:2 compressor is different for the four models and is explained briefly as follows:

3.1 Model 1: (XOR, MUX based)
In this design implementation seven 3:2 compressors are used. The 3:2 compressor is built with two XOR and one MUX circuit with reference to [2]. The XOR and MUX circuits are designed with reference to [2] where instead of pass transistors FinFETs are used. The circuit is as shown in Figure 2.

![Figure 2. 3:2 compressor (XOR,MUX based)](image)

The Internal Circuit of XOR and MUX are as shown in Figure 3 and Figure 4 respectively. The transistor count for the 3:2 compressor is 14 i.e. each XOR circuit has 4 and MUX has 6 transistor count.

![Figure 3. XOR circuit](image)

3.2 Model 2: (XOR-XNOR based)
In this design implementation, seven 3:2 compressors are used. The 3:2 compressor is built using a XOR-XNOR circuit and two MUX circuit and an inverter. The Sum and Carry are taken from each of the MUX respectively and Inputs are given to the XOR-XNOR.
The Internal Circuit of XOR-XNOR and MUX are as shown in Figure 5 and Figure 4 respectively. The transistor count for the 3:2 compressor is 20 i.e. each XOR-XNOR circuit has 8 and MUX has 6 transistor count.

Figure 4. MUX circuit

3.3 Model 3: (XOR, MUX using NAND)
In this design implementation seven 3:2 compressors are used. Here the 3:2 compressor is built using two XOR circuits and one MUX circuit. The Internal Circuit of XOR and MUX are implemented using NAND. The advantage of NAND gate is that it can perform all basic logical operations and NAND-NAND realization needs only one type of gate that minimizes IC package counter. The transistor count for the 3:2 compressor is 48 i.e. each XOR circuit has 16 and MUX has 16 transistor count.

3.4 Model 4: (MUX Based)
In this design implementation seven 3:2 compressors are used. Here the 3:2 compressor is built based on two 4:1 MUX and one inverter. All the circuits built based on Pass transistors. The circuit is as shown in Figure 6.
The Internal circuit of 4:1 MUX is as shown in Figure 7. The transistor count for the 3:2 compressor is 24 i.e. each 4:1 MUX has 12 transistors count.

After the above designed circuits, few more combinations are tried to analyze which would be better in terms of power and delay. One combination is, using one 4:2 compressor and five 3:2 compressors. The 4:2 compressor is designed with reference to [1]. Here the inputs $X_{1:9}$ is given to three 3:2 compressor, $C_{in1:3}$ given to one 3:2 compressor, $C_{in4:6}$ and sum output of two 3:2 compressors are given as inputs to 4:2 compressor. One more 3:2 compressor has inputs from carry and sum outputs of other 3:2 compressors. The sum and carry output of 4:2 compressor is considered as the sum and carry output of 9:2 compressor. The 9:2 compressor using 3:2 and 4:2 is as shown in Figure 8.
Figure 8. 9:2 Compressor using one 4:2 and five 3:2 compressors

The other combination is using two 5:2 compressors and one 3:2 compressor. The 5:2 compressor structure designed is based on [2]. Here the inputs $C_{in1}, C_{in2}, X_{1-5}$ is given to one 5:2 compressor and output of sum of 1st 5:2 compressor, $X_{6-9}$, $C_{in3}, C_{in4}$ given as input to other 5:2 compressor and output of sum of 2nd 5:2 compressor, $C_{in5}, C_{in6}$ given as input to 3:2 compressor. Sum and Carry are taken from the 3:2 compressor for the 9:2 compressor. 3:2 compressor using (XOR, MUX based). The circuit is as shown in Figure 9.

Figure 9. 9:2 Compressor using two 5:2 and one 3:2 compressor

The other combination is using one 6:2 compressor and three 3:2 compressors. Here the inputs $X_{1-7}$ is given the three 3:2 compressor, $X_{8-9}, C_{in1-6}$ as inputs to 6:2 compressor. Sum and output is taken from 6:2 compressor. The circuit is as shown in Figure 10.
4. Comparative Results
The compressors discussed in section 3 are simulated using Cadence Virtuoso Simulator with FINFET 32nm technology. Table 1 shows the comparative results of power, delay, power delay product and transistor count for the different proposed circuit models.

Table 1. Comparison of 9:2 compressors using different models

| Models           | Power(W) | Delay(sec) | PDP (J)     | Transistor Count |
|------------------|----------|------------|-------------|------------------|
| 9:2 using 3:2 M1| 1.669 n  | 19.89 m    | 0.033x10^9  | 98               |
| 9:2 using 3:2 M2| 783.9 p  | 3.621 n    | 2.838x10^18 | 140              |
| 9:2 using 3:2 M3| 198.0 p  | 7.95 m     | 0.0015x10^18| 336              |
| 9:2 using 3:2 M4| 291.8 p  | 472.4 n    | 14.9 x10^-18| 148              |
| 9:2 using 4:2    | 5.335 u  | 20.00 m    | 106.7x10^9  | 122              |
| 9:2 using 5:2    | 1.475 n  | 23.1 n     | 12.9 x10^-18| 98               |
| 9:2 using 6:2    | 1.751 n  | 15.75 n    | 27.5 x10^-18| 98               |

M1 – Model 1 (XOR, MUX)
M2 – Model 2 (XOR-XNOR, MUX)
M3 – Model 3 (XOR, MUX using NAND)
M4 – Model 4 (MUX)
5. Conclusion

In this paper a new design for 9:2 compressor circuit has been reported. Different 9:2 compressors using XOR::MUX, XOR-XNOR::MUX, XOR::MUX(using NAND), 4:1 MUX, 9:2 Compressor with five 3:2 compressors and one 4:2 compressor, 9:2 Compressor with two 5:2 compressors and one 3:2 compressor, 9:2 Compressor with three 3:2 compressors and one 6:2 compressor simulated. And among them less power of value 291.8 pW is consumed for 9:2 compressor using 3:2 Model 4(using MUX), less delay of value 3.621 nsec is observed for 9:2 compressor using 3:2 Model 2 and Overall PDP of value 14.9 x 10^-18 Joules is better in 9:2 compressor using 3:2 Model 4(using MUX). In order to perform higher order multiplications different compressors like 7:2, 8:2 and 9:2 compressors will help reduce the area, power consumption and increases the speed of operation. And in order to completely analyze the performance, the work can be extended to layout to chip level where the delays due to wires and interconnects are included.

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