Design of a Reconfigurable Information Collection and Identification System for Packages Storage and Checkout

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Abstract. With the continuous and rapid development of e-commerce, the requirements of logistics informatization are also increasing. At present, the barcode collection and identification device used in the operation of packages storage and checkout is generally based on ASIC chip, which is not fast enough. Therefore, this paper proposes a reconfigurable information acquisition and identification system, which is applied to the operation of package storage and delivery. This system uses FPGA + ARM architecture to realize the functions of identifying, storing and uploading the barcode information on the outer surface of the package to the host computer through UDP protocol. Because the parallel operation structure of FPGA is used to design the barcode image processing accelerator circuit, the data processing capacity of the soft core processor is reduced, and the recognition speed of the system is improved as a whole. The test shows that this system is faster and more accurate than the package barcode information recognition device based on ASIC technology.

Keywords: Packages storage and checkout; Barcode identification; Image preprocessing; Reconfigurable.

1. Introduction
In recent years, with the rapid development of e-commerce in China, the number of packages in 2020 has exceeded 80 billions. With the development of express business, the logistics management also needs to meet the corresponding requirements, that is, using computer, artificial intelligence, big data and other technologies to upgrade the traditional logistics management. Generally, the whole transportation process of a package includes packaging, labeling, transportation, sorting, warehousing and delivery. At present, the existing one-dimensional and two-dimensional barcode (two-dimensional code) information detection systems are based on high-performance ASIC chips. Due to the limitation of serial operation structure of ASIC processor, it is difficult for ASIC circuit to improve the barcode recognition speed. Therefore, this paper proposes a reconfigurable package barcode information collection and recognition solution based on FPGA chip. The solution adopts the architecture of FPGA + Arm, which not only gives full play to the Arm processor ability, but also combines the acceleration characteristics of FPGA in parallel structure, so that the whole system has the characteristics of fast recognition speed and high real-time performance[1,4].

2. System Design
The hardware circuit of this system is composed of camera module, FPGA, TF card, network cable, upper computer and power supply. The structure block diagram of the system is shown in Figure 1. The system uses FPGA to assist Arm in data acquisition and processing. Firstly, a median filter and binary acceleration circuit is designed to process the barcode image collected by the camera in
advance. Then, QR decoding is performed on the processed image in CM3 processor. Finally, the identified barcode information is written into TF card through the designed APB2SPI bus peripheral interface circuit, and through Xilinx's Axi_EthernetLite IP core uploads the barcode information to the host computer in the form of UDP protocol.

![System structure](image)

**Figure 1.** System structure.

### 2.1. Circuit Design of Barcode Image Processing Accelerator

Because the image collected by the camera has noise, which has a great impact on the quality of image recognition[2]. Therefore, it is necessary to process the image in advance. This system adopts the parallel operation structure of FPGA, and designs an accelerating circuit of image median filtering and binarization. Median filtering is based on the theory of statistical ranking. Its core operation is to sort the data in the template, so that the noise is arranged at both ends of the data sequence, and the middle value of the data sequence is generally not the noise value, so the purpose of noise removal is realized. In order to use FPGA to realize the parallel operation of median filtering, this paper adopts the fast 3x3 median filtering algorithm, and the algorithm principle is shown in Figure 1. A 3x3 window is designed to scan the row and column of a 640 * 480 image collected by the camera. The scanning direction is from left to right and from top to bottom.

![Principle of 3x3 matrix median filter](image)

**Figure 2.** Principle of 3x3 matrix median filter.

In Figure 2, for a 3x3 window matrix, calculate the maximum value, the median value and the minimum value of each row respectively, and then compare the maximum value of three rows to get the minimum value. The filtering result is taken as the median of 9 pixels. The calculation of each 3x3 window matrix is realized by designing a three-stage pipeline. The pipeline structure is shown in Figure 3.
2.2. **Interface Circuit Design of APB2SPI**

SPI bus interface consists of four signal lines, which are clock line signal (SCLK), chip selection signal (nCS), master out slave in signal (MOSI) and master in slave out signal (MISO). The transmission mode of SPI bus is realized by setting the values of clock polarity register (CPOL) and clock phase register (CPHA) registers in CM3 controller. In this design, set CPOL register and CPHA register to 1. When SPI bus is ready to transmit data, firstly pull down chip selection nCS signal, send data to MOSI signal line at the second clock edge, receive data from MISO signal line at the same time, and pull up chip selection signal after receive data[6].

The interface circuit structure of APB2SPI is shown in Figure 4, including APB interface, SPI mode configuration register, SPI data register, clock generator, transmit receive register and chip selection control register. The APB interface part is responsible for receiving and sending the data of APB bus protocol, and transferring the configuration data and transmission data from CM3 controller to SPI mode configuration register and SPI data register. The SPI data register writes the data to the transmit shift register for data transmission, and sends the value of the receive shift register to SPI data register, and transmitted it to CM3 controller through APB interface. The SPI register groups and their respective address allocation involved in the design of the interface circuit are listed in Table 1.

![Figure 3. Pipeline implementation of 3x3 matrix median filter.](image)

![Figure 4. Circuit structure of APB2SPI.](image)
Table 1. SPI register group and address allocation.

| SPI Register group    | Register bit allocation            | Register address |
|-----------------------|-----------------------------------|-----------------|
| SPI_CONFIG Register   | [31:10] Reserved, [9]Req, [8]Ncs, [7:0]F_Div | 0x300000000     |
| SPI_DATAIN Register   | [31:8] Reserved, [7:0]Data_in      | 0x300000040     |
| SPI_DOUT Register     | [31:8] Reserved, [7:0]Data_out     | 0x300000080     |
| SPI_ACK Register      | [31:30] Reserved, [0]Ack           | 0x3000000C0     |

3. Digital Circuit Simulation and System Test

3.1. Simulation of Acceleration Circuit Function of Median Filter

Firstly, the median filter processing acceleration circuit of barcode image is designed by using Verilog HDL language. Secondly, the logic synthesis of the prepared digital circuit is carried out by using vivado software. Finally, the function simulation of the acceleration circuit is operationed by using modelsim. The Modelsim simulation of the median filter function is shown in Figure 5.

It can be seen from the waveform that when the first rising edge of the first clock comes, the values of the input nine pixels are {20, 60100}, {60100140}, {100140, 30}. At the third clock rising edge, the median value of nine pixels output numbers of data is 100, which indicates that the extraction of median value is successful. However, if the circuit based on ASIC is used to achieve the same function, and the bubble sorting algorithm executed by serial sorting is used, at least 12 clock cycles are needed. Therefore, the median filter circuit of barcode image designed has the function of accelerating image preprocessing.

Figure 5. Simulation test of median filter acceleration circuit.

3.2. Function Simulation of apb2spi Interface Circuit

In the simulation, the bus clock of APB is configured as 20MHz, and the APB2SPI interface circuit is mounted to the APB bus address of 0x30000000. The CM3 controller reconfigures the clock of APB2SPI circuit, and sets the SCLK clock to 2MHz for the storage operation of package information. At the same time, CM3 controller writes data 0x55 to SPI interface circuit through APB bus. Figure 6 shows the output data waveform of SPI interface circuit. It can be seen from the figure that the data output by MOSI pin in turn is 01010101, which is consistent with the data written by CM3 controller.

Figure 6. Output data waveform of SPI interface.

3.3. System Function Test

CM3 processor software program is written in keil, including QR code decoding program, FatFs file system program and LwIP protocol stack program. Burne the ELF file into the off chip flash chip of FPGA board through JTAG downloader, and then set the FPGA to start from the external flash chip. Connect the IP address and port number of the UDP server running on the FPGA through the upper computer software. Randomly generate four two-dimensional codes containing the express order number and the sender information for testing. The function test results of the system are shown in Figure 7. The upper computer software received four pieces of package information one after another, corresponding to the four QR codes on the left. It can be seen that the system can upload package information to upper computer in real time.
4. Conclusion

Based on the architecture of FPGA + Arm, this paper adopts the parallel operation structure of FPGA to speed up the processing speed of barcode image. For the image data collected by Cortex_M3 soft core processor, median filtering and other preprocessing are carried out to reduce the data processing capacity of the soft core processor, so improve the recognition speed of the system as a whole. The test shows that this system can recognize the two-dimensional code information of the package in real time, and upload the package information to the upper computer completely. Compared with the general ASIC chip solution, it has the advantages of flexible structure and fast processing speed.

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