Realization of a Generalized Switched-Capacitor Multilevel Inverter Topology with Less Switch Requirement

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Abstract: Conventional multilevel inverter topologies like neutral point clamped (NPC), flying capacitor (FC), and cascade H bridge (CHB) are employed in the industry but require a large number of switches and passive and active components for the generation of a higher number of voltage levels. Consequently, the cost and complexity of the inverter increases. In this work, the basic unit of a switched capacitor topology was generalized utilizing a cascaded H-bridge structure for realizing a switched-capacitor multilevel inverter (SCMLI). The proposed generalized MLI can generate a significant number of output voltage levels with a lower number of components. The operation of symmetric and asymmetric configurations was shown with 13 and 31 level output voltage generation, respectively. Self-capacitor voltage balancing and boosting capability are the key features of the proposed SCMLI structure. The nearest level control modulation scheme was employed for controlling and regulating the output voltage. Based on the longest discharging time, the optimum value of capacitance was also calculated. A generalized formula for the generation of higher voltage levels was also derived. The proposed model was simulated in the MATLAB®/Simulink 2016a environment. Simulation results were validated with the hardware implementation.

Keywords: multilevel inverter (MLI); switch count; switched-capacitor cell; capacitor voltage balancing

1. Introduction

Conversion of power from DC to AC or AC to DC is a key technology involved in the generation, transmission, distribution, and utilization of electrical energy. With the advent of fast and high rating power electronics devices, digital controllers, and sensors the power converter industry is seeing a revolution. Inverters form the backbone of drives and grid integration applications. They can be classified based on the nature of the output waveform, such as square wave inverter, quasi square wave inverter, two-level pulse width modulated inverters, and multilevel inverter [1,2]. Although the realization of conventional two-level inverters is simple, it has many shortcomings. High total harmonic distortion (THD) with the requirement of higher blocking voltage rating devices and the better design of filters for improving the power quality restrict their application to a small power range. To overcome the shortcomings of the conventional two-level inverter, a multilevel inverter was proposed [3–5]. Multilevel inverters are composed of semiconductor switches and DC power supplies/capacitive voltage sources. A multiple-step voltage waveform with variable and controllable
frequency, phase, and amplitude are obtained by suitable connection and control of the switches using a modulation scheme [6]. Because of the inherent superior harmonic profile and less voltage stress across switches, MLI has replaced a two-level counterpart for high power applications. MLIs find wide usage in motor drive applications [7]. Neutral point clamped (NPC), flying capacitor (FC), and cascade H bridge (CHB) are the conventional MLI topologies. Separate DC voltage sources are required for the generation of multistep voltage in a CHB. CHB has a modular structure and can be more easily extended to achieve higher voltage levels. FC requires a complex control mechanism to ensure that the voltage across the capacitor is maintained constant. Therefore, conventional MLI is not suitable for voltage levels beyond five [8]. A large number of modified/hybrid conventional topologies that were proposed required a large number of power semiconductor switches for the generation of higher voltage levels [9]. Each switch requires a separate driver circuit and heat sink. Consequently, size and complexity increase. To avoid these issues, authors in [10–14] presented reduced device count topologies of MLI. Although a higher number of voltage levels are generated with a smaller number of device counts, they do not possess the voltage boosting capability. This boosting feature is available in the switched capacitor multilevel inverter (SCMLI) in which the capacitor acts as a voltage source, which was introduced by authors of [15] in 1998. They obtained a 31-level output voltage with the help of two sub-circuits. Each sub-circuit contained 15 basic cells. One basic cell consisted of two diodes, two MOSFETs, and one capacitor. The topology requires a complex control algorithm for balancing the capacitor voltage. Authors of [16,17] introduced reduced device count MLI topologies having a capacitor, but the capacitor voltage balancing issue remained. This problem was overcome by adding an auxiliary circuit reported in [18,19]. However, it increased the overall cost and complexity of the system. In [20], authors developed a novel switched capacitor-multilevel inverter known as a Marx inverter. It is capable of synthesizing the different output voltage levels and also maintaining the capacitor voltage at the desired level. Seven level output voltage is obtained with the help of ten switches. By cascading SC cells (consist of switches and capacitors), higher voltage levels can be achieved. In [21] authors proposed a new basic unit having two switches, one diode, and one capacitor. The topology has self-boosting capability without any transformer. Seventeen and twenty-five level output voltage with experimental results were reported. Since the boosting factor of this basic unit is two times of DC supply voltage, therefore for the generation of a higher number of voltage levels, cascading of basic units is needed. However, the cascading will increase the complexity and total standing voltage (TSV) of the circuit. Authors in [22] presented a switched capacitor multilevel inverter; this circuit can generate higher number of voltage levels with fewer switches in asymmetric configuration, but the TSV of the structure is significant. By the simultaneous charging and discharging of capacitors, authors in [23] obtained multilevel output voltage. However, it requires a large number of bidirectional switches and it also increases the TSV of the circuit significantly. In [24], authors introduced a novel structure of the switched-capacitor multilevel inverter. Its basic unit generates nine level output voltage with the help of ten switches, two capacitors, one diode, and one DC supply. The extended structure of this switch capacitor multilevel inverter was also discussed for symmetric and asymmetric DC supply configurations. However, the structure again suffers from a high TSV level for a higher voltage level. Authors in [25] proposed a new basic unit cell where the boosting factor is three times the DC supply voltage with the help of five semiconductor switches, two capacitors, and one diode. The structure promises to be a competitive topology for SCMLI.

In this paper, a generalized topology taking the basic unit of [25] is proposed. The paper is organized into eight sections. In Section 1, the working of the basic unit is explained. Section 2 deals with a symmetric DC supply configuration and its modes of operation. Further, in Sections 3–5, an asymmetric DC supply configuration, selection procedure of capacitance, and an extension of the proposed topology are discussed, while Section 6 deals with comparative analysis of the proposed generalized scheme. Section 7 presents simulation and hardware results, and the paper is concluded in Section 8. The nearest level control modulation scheme (NLC), which comes under the fundamental switching frequency scheme [26], is employed for controlling the switches.
2. Basic Unit

The basic unit cell of the switched-capacitor multilevel inverter is shown in Figure 1. It is comprised of one voltage source, one diode, two capacitors, and five IGBT (Insulated-gate bipolar transistor) semiconductor switching devices. A DC voltage supply is connected between capacitor legs \( L_1 \) and \( L_2 \). Switches \( (S_1, S_2) \) in capacitor leg \( L_1 \) and \( (S_3, S_4) \) in capacitor leg \( L_2 \) are complementary to each other. Charging leg CH1 is realized by a power switch along with a power diode. This leg starts conducting when capacitor \( C_1 \) or \( C_2 \) is charging. Table 1 shows the switching scheme of the basic unit; 1 stands for the switch-on condition, and 0 stands for the switch-off condition. \( D \), \( C \), and \( NC \) stand for discharging, charging, and not connected states of capacitors, respectively.

![Figure 1. Basic unit of switched-capacitor multilevel inverter.](image)

| \( S_1 \) | \( S_2 \) | \( S_3 \) | \( S_4 \) | \( S_{CH1} \) | \( C_1 \) | \( C_2 \) | Level |
|----------|----------|----------|----------|-------------|--------|--------|-------|
| OFF      | ON       | OFF      | ON       | OFF         | NC     | NC     | V     |
| OFF      | ON       | ON       | OFF      | ON          | C      | D      | 2V    |
| ON       | OFF      | ON       | OFF      | ON          | D      | C      | 2V    |
| ON       | OFF      | ON       | OFF      | OFF         | D      | D      | 3V    |

The basic unit acts as a boost converter that can generate \( V \), \( 2V \), and \( 3V \) voltage levels, which is shown with the help of Figure 2. The output voltage is taken between points A and N. The conducting path for each level generation is indicated by red color. For obtaining \( +V \) voltage between the point A and N, switch \( S_2 \) and \( S_4 \) are in the on condition, and capacitors \( C_1 \) and \( C_2 \) both are not connected, i.e., both the capacitors are neither in the charging nor in the discharging state. Figure 2 shows an equivalent circuit diagram of this voltage level generation. There are two ways for generating the \( +2V \) voltage level at the output between A and N, as shown in Table 1.

As shown in Figure 2b, it is necessary that capacitor \( C_2 \) is charged up to DC source voltage. Therefore, by closing the switches \( S_2 \) and \( S_3 \), capacitor \( C_2 \) discharges and is connected in series with the supply voltage to produce a 2 V voltage level. Simultaneously, capacitors \( C_1 \) is charged up to supply voltage \( V \) by providing a path from \( S_2 \), \( SCH_1 \), and \( S_3 \). Further, as shown in Figure 2c, by switching ON of \( S_1 \) and \( S_4 \), capacitor \( C_1 \) discharges and is connected in series with the supply voltage. At the same time, with the help of switch \( SCH_1 \), \( S_1 \), \( S_4 \), and the power diode, capacitor \( C_2 \) charges up to the supply voltage. It is to be noted that the charging leg comes into the picture when either capacitor \( C_1 \) or \( C_2 \) is in the charging state. For the sake of better understanding, charging states of capacitors are represented
by a blue color. For generating +3 V at the output switch, pair $S_1, S_3$ is in the ON condition, and both the capacitors discharge and are connected in series with the supply voltage, as shown in Figure 2d.

![Figure 2. Generation of different voltage levels of the basic unit at $V_{AN}$. (a) V, (b) 2V ($C_1$ in charging state), (c) 2V ($C_2$ in charging state), (d) 3V (both $C_1$ and $C_2$ in discharging state).]

3. Symmetric Configuration

3.1. Circuit Diagram

Figure 3 shows the circuit diagram of 13 level SCMLI. The switching table of this configuration is given by Table 2. It consists of two H-bridges and two basic units. For each basic unit, a DC voltage supply of equal rating is used. The two H-bridges are cascaded with the load. IGBT acts as a switch for this circuit. Each capacitor of the basic unit is charged up to the DC supply voltage. Since each basic unit generates three voltage levels, therefore 13 level output voltage can be achieved by this configuration.

![Figure 3. Circuit diagram of proposed extension for 13 level SCMLI.]


Table 2. Switching states of the proposed symmetrical 13 level SCMLI.

| $S_1$ | $S_3$ | $S_{CH1}$ | $T_1$ | $T_3$ | $S_5$ | $S_7$ | $S_{CH2}$ | $T_5$ | $T_7$ | Level | $C_1$ | $C_2$ | $C_3$ | $C_4$ |
|-------|-------|-----------|-------|-------|-------|-------|-----------|-------|-------|-------|-------|-------|-------|-------|
| 0     | 0     | 0         | 1     | 1     | 0     | 0     | 0         | 1     | 1     | 0V    | NC    | NC    | NC    | NC    |
| 0     | 0     | 0         | 1     | 0     | 0     | 0     | 0         | 0     | 0     | $V$   | NC    | NC    | NC    | NC    |
| 0     | 0     | 0         | 1     | 0     | 0     | 0     | 0         | 1     | 0     | 2V    | NC    | NC    | NC    | NC    |
| 0     | 1     | 1         | 1     | 0     | 0     | 0     | 0         | 1     | 0     | 3V    | C     | D     | NC    | NC    |
| 1     | 0     | 1         | 1     | 0     | 1     | 1     | 0         | 1     | 0     | 4V    | D     | C     | C     | D     |
| 1     | 1     | 0         | 1     | 0     | 1     | 0     | 1         | 1     | 0     | 5V    | NC    | NC    | D     | C     |
| 1     | 1     | 0         | 1     | 0     | 1     | 0     | 1         | 1     | 0     | 6V    | D     | D     | D     | D     |
| 0     | 0     | 0         | 0     | 1     | 0     | 0     | 0         | 1     | 1     | $-V$  | NC    | NC    | NC    | NC    |
| 0     | 0     | 0         | 0     | 1     | 0     | 0     | 0         | 0     | 1     | $-2V$ | NC    | NC    | NC    | NC    |
| 0     | 1     | 1         | 0     | 1     | 0     | 0     | 0         | 0     | 1     | $-3V$ | C     | D     | NC    | NC    |
| 1     | 0     | 1         | 0     | 1     | 1     | 0     | 1         | 0     | 1     | $-4V$ | D     | C     | C     | D     |
| 1     | 1     | 0         | 0     | 1     | 1     | 0     | 1         | 0     | 1     | $-5V$ | NC    | NC    | D     | C     |
| 1     | 1     | 0         | 0     | 1     | 1     | 0     | 0         | 0     | 1     | $-6V$ | D     | D     | D     | D     |

3.2. Modes of Operation

There are 13 modes of operation related to this configuration arrangement. The positive modes (including 0V) are described here with reference to Figure 4.

- **Mode 0**

  As shown in Figure 4a, the amplitude of the output voltage across the load is zero. It can be achieved by switching ON $T_1$, $T_3$, $T_5$, and $T_7$. Switches $S_2$, $S_4$, $S_6$, and $S_8$ are also ON, but these switches do not play any role in generating the zero voltage level at the output.

- **Mode 1**

  In this mode, the amplitude of the output voltage across the load is equal to $V$. This voltage level is produced by switching ON the transistors $S_2$, $S_4$, $T_2$, $T_4$, $S_6$, $S_8$, $T_6$, and $T_8$, as shown in Figure 4b.

- **Mode 2**

  In this mode, the voltage developed across the output is 2V. Here, each basic unit (upper and the lower) generate V voltage levels. This is shown in Figure 4c. Switches $S_2$, $S_4$, $S_6$, $S_8$, $T_1$, $T_4$, $T_5$, and $T_8$ are ON for the generation of this voltage level.

- **Mode 3**

  In this mode, the voltage developed across the output is 3V. The upper basic unit generates a 2V voltage level, while the lower basic unit produces the V voltage level. This is to be obtained by switching on the transistor $S_2$, $S_3$, $S_6$, $S_8$, $T_1$, $T_4$, $T_5$, and $T_8$. Capacitor $C_1$ is in charge up to the V voltage level, which is indicated by blue color. Figure 4d shows the circuit arrangement for the generation of this voltage level.

- **Mode 4**

  In this mode, the voltage developed across the output is 4V. Both the basic units generate 2V. Capacitor $C_2$ and $C_3$ are charging while $C_1$ and $C_2$ are discharging. Switches $S_1$, $S_4$, $S_6$, $S_7$, $T_1$, $T_4$, $T_5$, and $T_8$ are ON for this sinewave. Figure 4e shows the conduction for the generation of this voltage level.
• **Mode 5**

In this mode, the voltage developed across the output is 5V. The contribution of the upper and lower unit is 3V and 2V, respectively. Capacitors $C_1$, $C_2$, and $C_3$ are in the discharging state, while capacitor $C_4$ is in the charge state up to the DC source voltage because it comes in parallel with DC supply voltage. Switches $S_1$, $S_3$, $S_5$, $S_8$, $T_1$, $T_4$, $T_5$, and $T_8$ are ON for this mode, as shown in Figure 4f.

• **Mode 6**

In this mode, the voltage developed across the output is 6V. All the capacitors are discharged and connected in series with DC source voltage and the load. Both the units generate 3V, and the output is the summation of these two voltage levels. Switches $S_1$, $S_3$, $S_5$, $S_7$, $T_1$, $T_4$, $T_5$, and $T_8$ are ON for this mode, as shown in Figure 4g.

![Figure 4. Positive modes of 13 level SCMLI (a): Mode 0; (b): Mode 1; (c): Mode 2; (d): Mode 3; (e): Mode 4; (f): Mode 5; (g): Mode 6.](image)

4. **Asymmetric Configuration**

In the asymmetric configuration, the voltage of the DC supply in the lower basic unit is four times higher than the upper basic unit, for maximum level generation. The upper basic unit generates $V$, 2V, and 3V voltage levels, while the lower basic unit generates 4V, 8V, and 12V voltage levels. Maximum voltage stress across each switch in the upper basic unit and H bridge is $V$ and 3V volt, while for the lower basic unit, it is 4V and 12V. Therefore, in the lower basic unit, higher ratings of switches are required.

4.1. **Modes of Operation**

There are 31 voltage levels, out of which only positive voltage levels are shown in Figure 5. For the generation of $V$, 2V, and 3V, only switches of the upper basic unit play a role. Table 3 gives...
information about the generation of the voltage level and conducting states of switches and capacitors for all positive modes. For the generation of a negative voltage level (−V, −2V, etc.) the same switches are ON in both upper and lower basic units, just like the generation of V, 2V, while complementary switches of H bridges are ON. In both symmetric as well as asymmetric configurations, basic units behave as a level generator, while the cascaded H bridge acts as a polarity generator.

Figure 5. All positive mode of 31 level SCMLI. (a) Mode 1; (b) Mode 2; (c) Mode 3; (d) Mode 4; (e) Mode 5; (f) Mode 6; (g) Mode 7; (h) Mode 8; (i) Mode 9; (j) Mode 10; (k) Mode 11; (l) Mode 12; (m) Mode 13; (n) Mode 15; (o): Mode 15; (p): Mode 16.
Table 3. Switching for the generation of 31 voltage level.

| Modes | Conducting Switches | Capacitor States | Upper Basic Unit | Lower Basic Unit | Voltage Level |
|-------|---------------------|------------------|------------------|------------------|---------------|
| 1     | S2 S4 S6 T1 T3 T5 T7 | NC NC NC NC    | 0V 0V 0V        |                  | 0V           |
| 2     | S2 S4 S6 T1 T4 T6 T8 | NC NC NC NC    | 0V 0V V         |                  | V            |
| 3     | S2 S3 S5 S7 T1 T4 T6 T8 | D C NC NC    | 2V 0V 2V        |                  |               |
| 4     | S1 S2 S4 S6 T1 T4 T6 T8 | D D NC NC    | 3V 0V 3V        |                  |               |
| 5     | S2 S4 S6 T1 T3 T5 T7 | NC NC NC NC    | 0V 4V 4V        |                  |               |
| 6     | S2 S4 S6 T1 T4 T6 T8 | NC NC NC NC    | 0V 4V 5V        |                  |               |
| 7     | S1 S2 S4 S6 S8 T1 T4 T6 T8 | D C NC NC    | 2V 4V 6V        |                  |               |
| 8     | S2 S4 S6 T1 T4 T5 T8 | D D NC NC    | 3V 4V 7V        |                  |               |
| 9     | S2 S4 S6 S8 T1 T3 T5 T7 | NC NC C D    | 0V 8V 8V        |                  |               |
| 10    | S2 S4 S6 S8 T1 T4 T6 T8 | NC NC D C    | 8V 9V 9V        |                  |               |
| 11    | S2 S3 S5 S7 S8 T1 T4 T6 T8 | C D C D    | 2V 8V 10V       |                  |               |
| 12    | S1 S2 S4 S6 S8 T1 T4 T5 T8 | D D D C    | 3V 8V 11V       |                  |               |
| 13    | S2 S4 S6 T1 T3 T5 T7 | NC NC D D    | 0V 12V 12V      |                  |               |
| 14    | S1 S2 S4 S6 T1 T4 T6 T8 | NC NC C D    | 12V 13V 13V     |                  |               |
| 15    | S1 S2 S4 S6 S8 T1 T4 T6 T8 | D C D D    | 2V 12V 14V      |                  |               |
| 16    | S2 S4 S6 S8 T1 T4 T5 T8 | D D D D    | 3V 12V 15V      |                  |               |
| 17    | S2 S4 S6 S8 T1 T3 T5 T7 | NC NC NC NC    | V 0V –V       |                  |               |
| 18    | S2 S3 S5 S7 S8 T1 T4 T6 T8 | C NC NC NC    | 2V 0V –2V       |                  |               |
| 19    | S1 S2 S4 S6 T2 T3 T5 T7 | D D NC NC    | 3V 0V –3V       |                  |               |
| 20    | S2 S4 S6 S8 T2 T4 T6 T8 | NC NC NC NC    | 0V 4V –4V       |                  |               |
| 21    | S2 S4 S6 S8 T2 T3 T5 T7 | NC NC NC NC    | V 4V –5V       |                  |               |
| 22    | S1 S2 S4 S6 S8 T2 T4 T6 T8 | C NC NC NC    | 2V 4V –6V       |                  |               |
| 23    | S2 S4 S6 S8 T2 T3 T5 T7 | D D NC NC    | 3V 4V –7V       |                  |               |
| 24    | S2 S4 S6 S8 T2 T4 T6 T8 | NC NC C D    | 0V 8V –8V       |                  |               |
| 25    | S2 S4 S6 S8 T2 T3 T5 T7 | NC NC D C    | V 8V –9V       |                  |               |
| 26    | S2 S3 S5 S7 S8 T2 T4 T6 T8 | C D C D    | 2V 8V –10V      |                  |               |
| 27    | S1 S2 S4 S6 S8 T2 T3 T5 T7 | D D C D    | 3V 8V –11V      |                  |               |
| 28    | S2 S4 S6 S8 T2 T4 T6 T8 | NC NC D D    | 0V 12V –12V     |                  |               |
| 29    | S2 S4 S6 S8 T2 T3 T5 T7 | NC NC D D    | V 12V –13V     |                  |               |
| 30    | S1 S2 S4 S6 S8 T2 T4 T6 T8 | D C D D    | 2V 12V –14V     |                  |               |
| 31    | S1 S2 S4 S6 T2 T3 T5 T7 | D D D D    | 3V 12V –15V     |                  |               |

4.2. Calculation of Capacitance

This section gives the procedure for the selection of a suitable Value of capacitance. It is done by evaluating the longest discharging time (LDT) of each capacitor. Based on the switching state, which is shown in Table 3, the longest discharging time for different capacitors is shown in Figure 6.

Figure 6. Thirty-one level output Voltage waveform (inverted negative cycle) with LDT for different capacitors.
It is to be noted that during the LDT, the capacitor discharges the maximum amount. The amount of discharging charge depends upon the load current and LDT duration. From Figure 6, it can be concluded that the discharging duration of capacitor $C_3$ is larger as compared to other capacitors. Mathematically, the amount of discharging of the switched capacitor $C_3$ can be expressed by the following equation:

$$Q_{C_3} = 2 \times \int_{t_{11}}^{t} i_0(t) dt \quad (1)$$

Similarly, for $C_1$, $C_2$, and $C_4$,

$$Q_{C_1} = 2 \times \int_{t_{14}}^{t} i_0(t) dt \quad (2)$$

$$Q_{C_2} = 2 \times \int_{t_{15}}^{t} i_0(t) dt \quad (3)$$

$$Q_{C_4} = 2 \times \int_{t_{12}}^{t} i_0(t) dt \quad (4)$$

Now the optimum Value of capacitance is expressed by

$$C_{opt} \geq \frac{Q_{C_1} or Q_{C_2} or Q_{C_3} or Q_{C_4}}{\rho \times V_{dc}} \quad (5)$$

where $\rho$ signifies the ripple in capacitor Voltage from the maximum allowable capacitor Voltage and where $Q$ denotes electric charges.

Now for a resistive load condition, the load current during the longest discharging time (LDT) can be expressed by the following equation:

$$i_0(t) = \frac{11V_{dc}}{R_L} \text{ for } t_{11} \leq t \leq t_{12} \quad (6)$$

For the fundamental switching frequency scheme, the time $t_{11}$ can be calculated using the following steps:

Let $\Delta t$ be a small Value. By adding and subtracting this small Value of $\Delta t$ in $t_{11}$ with these two Value, the following are obtained:

$$V_m \sin(\omega(t_{11} - \Delta t)) = 10 \quad (7)$$

$$V_m \sin(\omega(t_{11} + \Delta t)) = 11 \quad (8)$$

Adding Equations (7) and (8) and after manipulating by trigonometric identities, we get

$$2V_m \sin(\omega t_{11}) = 21 \quad (9)$$

Since the maximum Value of the sine wave is 1, therefore,

$$t_{11} = \frac{\sin^{-1}(\frac{21}{2V_m})}{2\pi f} \quad (10)$$

Using Equations (1), (5), (6) and (10), the optimum Value of capacitance for the resistive load can be expressed by the following equation:

$$C_{opt} \geq \frac{17.55}{2\pi \times f \times \rho \times R_L} \quad (11)$$
Referring to Equation (11), the optimum Value of the capacitor is inversely proportional to the load resistance, output frequency, and the percentage of Voltage Ripple. The corresponding Figure 7 shows the Variation of capacitor Value with load resistance for different percentage of Voltage Ripple (ρ).

Figure 7. Variation of capacitance with resistance for different Value of ripple Voltage of capacitor (a) for $C_3$, (b) for $C_4$, and (c) for $C_1$. 
For a resistive-inductive load condition, the load current during LDT can be expressed by the following equation:

\[ i_0(t) = I_{0\text{max}} \sin(2\pi f - \varphi) \] (12)

The optimum value of capacitance for \( C_3 \) can be calculated by solving Equation (13) using Equations (1), (10), and (12).

\[ C_{3,\text{opt}} \geq \frac{2I_{0\text{max}}}{\alpha \rho V_{dc}} \left[ \cos(0.7753 - \varphi) - \sin \varphi \right] \] (13)

Figure 8 is obtained for \( I_{0\text{max}} = 3A, V_{dc} = 72V \), and \( f = 50 \text{ Hz} \), which shows the Variation of optimal capacitance for different Values of phase angle (between R and L) \( \varphi \) and the percentage of Voltage Ripple \( \rho \).

Similarly,

\[ C_{1,\text{opt}} \geq \frac{2I_{0\text{max}}}{\alpha \rho V_{dc}} \left[ \cos(1.1197 - \varphi) - \sin \varphi \right] \] (14)

\[ C_{2,\text{opt}} \geq \frac{2I_{0\text{max}}}{\alpha \rho V_{dc}} \left[ \cos(1.3116 - \varphi) - \sin \varphi \right] \] (15)

\[ C_{4,\text{opt}} \geq \frac{2I_{0\text{max}}}{\alpha \rho V_{dc}} \left[ \cos(0.8758 - \varphi) - \sin \varphi \right] \] (16)

Figure 8. Variation of capacitance with phase angle for different Values of ripple Voltage of capacitor \( C_3 \).

5. Extension of Proposed Scheme

For the generation of the higher number of Voltage levels with reduce device count and for improving the harmonic profile of multilevel inverter extension of MLI, a topology is carried out in this section. It is done by adding capacitor legs in each side of the DC source; these legs are called charging legs. Figure 9 shows the structure of the proposed scheme for symmetric configuration up to the \( m = 4 \) stage or charging leg. The proposed topology is also applicable to asymmetric configuration. It is to be mentioned that the selection of the DC Voltage source in the lower basic unit cell is dependent on the Voltage levels generated by the upper basic unit. For example, when charging leg \( m = 2 \), the basic unit acts as a Voltage source which generates a 3V Voltage level; therefore, with the turning on of switches \( (S_{10,2}, S_{11,2}) \), \( (S_{CH3,2}) \), capacitor \( C_{5,2} \) is charged up to the 3V Voltage level. Similarly, capacitor \( C_{6,2} \) is charged up to the 3V Voltage level by providing a current flow path by switching on \( (S_{9,2}, S_{11,2}) \), and \( (S_{CH3,2}) \). When both the capacitors are connected in series with the DC source, nine Voltage levels are obtained across the output. Hence the boosting factor of the basic unit is increasing in the order of \( 3^m \). The lower basic unit obtains the same Voltage level (9V). Therefore, the Voltage
The following equations give a generalized formula for both symmetric and asymmetric configuration in terms of charging legs or stages (m). Several diodes, switches, capacitors, and voltage sources are the same for both the configurations.

Number of level \( (N_L) = (4.3^m + 1) \) (for symmetric configuration)

\[ = (3^m + (3^m + 1)3^m) \times 2 + 1 \) (asymmetric configuration) \]  

Number of diodes \( (N_D) = 2m \) \]  

Number of switches \( (N_S) = 10m + 8 \) \]  

Number of gate drivers \( (N_G) = 10m + 8 \) \]  

Number of capacitors \( (N_C) = 4m \) \]

The current rating of the switches in a multilevel inverter is equal to the rated load current. However, this is not true for the voltage rating of switches; it affects the total cost of the inverter. Therefore, for evaluating the multilevel inverter topology from the viewpoint of blocked voltage by power switches and the total cost of the system, standing voltage criteria are defined, which are equal to the sum of all blocked voltages by power switches in a converter. In the symmetric configuration,
the total standing Voltage of the basic unit and H bridge is 5V and 12V, respectively. This topology consists of two H bridges and basic units. Hence the total standing Voltage of this topology is 34 and 5.66 (in terms of per unit). The following formula gives the generalized formula for TSV:

\[
T_{SV} = 2 \sum_{m=1}^{n} 3^{m-1} + 3^m \quad (8)
\]

\[
T_{SV} (\text{pu}) = \frac{T_{SV}}{4.3^m / 2} \quad (22)
\]

Similarly, for asymmetric configuration, the generalized formula of TSV is given by the following equation:

\[
5 \sum_{m=1}^{n} 3^{m-1} + 5 \sum_{m=1}^{n} 3^{m-1} + 4.3 + 4.3(3^m + 1)
\]

\[
T_{SV} (\text{pu}) = \frac{T_{SV}}{(3^m + 3^m(3^m + 1))} \quad (25)
\]

With the help of Equation (17), the relation between circuit components and the number of levels can be achieved.

Since

\[
N_L = 4(3^m) + 1,
\]

\[
\frac{N_L - 1}{4} = 3^m
\]

Taking log on both sides,

\[
m = \log_3 \left( \frac{N_L - 1}{4} \right)
\]

Now the no. of capacitors, diodes, and switches can be written as

\[
N_C = 4 \log_3 \left( \frac{N_L - 1}{4} \right) \quad (26)
\]

\[
N_D = 2 \log_3 \left( \frac{N_L - 1}{4} \right) \quad (27)
\]

\[
N_S = 8 + 10 \log_3 \left( \frac{N_L - 1}{4} \right) \quad (28)
\]

Similarly, the relation between circuit components and the number of levels for asymmetric configuration are given by the following equations:

\[
N_C = 4 \log_3 \left[ -1 + \sqrt{ \frac{N_L + 1}{2} } \right] \quad (29)
\]

\[
N_D = 2 \log_3 \left[ -1 + \sqrt{ \frac{N_L + 1}{2} } \right] \quad (30)
\]

\[
N_S = 8 + 10 \log_3 \left[ -1 + \sqrt{ \frac{N_L + 1}{2} } \right] \quad (31)
\]

6. Comparison of Proposed with Other Existing SCMLI Topology

Table 4 shows the comparison of some existing SCMLIs and proposed topology in terms of device counts. The proposed topology was better as compared to topology proposed by the authors in [4,5] concerning the number of DC sources. Although authors [6] obtained seVenteen levels by using 18
switches, they required some bidirectional switches. The topology presented in [7] is comparable with the proposed topology in terms of capacitors, diodes, and TSV for the generation of 13 levels of the output Voltage, and 37 levels (when $m = 2$) of the output Voltage were obtained by extending the structure of the proposed scheme. It exhibited better results in terms of device count and TSV as compared to the topology ($m = 2$) presented in [5]. From Table 5, it can be concluded that the proposed structure with asymmetric DC sources was not significantly beneficial as compared to suggested topologies for producing lower output Voltage levels. However, it required a smaller number of devices for the generation of higher Voltage levels. A generalized formula for finding the number of switches and capacitors with the number of levels is shown in Table 6. Here $m$ represents the stage. All the topologies discussed in table are modular in structure. Therefore, extension of these topologies is possible for achieving a higher number of Voltage levels. Figure 10 shows the relation between the number of levels and stages; it can be concluded that the proposed topology (both symmetric and asymmetric) is better than the others. Additionally, fewer capacitors and switches are required for the generation of higher Voltage levels, as can be seen in Figures 11 and 12. Therefore, the proposed topology is far better than other topologies for the generation of higher Voltage levels with a smaller number of device counts.

**Table 4.** Comparison of proposed topology with other symmetric SCMLI.

| SCMLI Presented In | $N_L$ | $N_{dc}$ | $N_S$ | $N_C$ | TSV |
|-------------------|------|---------|------|------|-----|
| [27]              | 13   | 3       | 18   | 3    | 5   |
| [28] ($m = 1$)    | 17   | 4       | 20   | 4    | 5   |
| ($m = 2$)         | 33   | 4       | 32   | 8    | 6   |
| [29]              | 13   | 2       | 14   | 4    | 5.3 |
| [24]              | 17   | 2       | 18   | 4    | 5   |
| [25]              | 13   | 2       | 16   | 4    | 5.6 |
| Proposed ($m = 1$)| 13   | 2       | 18   | 4    | 5.66|
| ($m = 2$)         | 37   | 2       | 28   | 8    | 5.66|

**Table 5.** Comparison of proposed with other asymmetric SCMLI.

| SCMLI Presented In | $N_L$ | $N_{dc}$ | $N_S$ | $N_C$ | TSV |
|-------------------|------|---------|------|------|-----|
| [28]              | 49   | 2       | 16   | 4    | 6.25|
| [29]              | 31   | 2       | 14   | 4    | 5.33|
| [24]              | 49   | 2       | 18   | 4    | 6   |
| [25]              | 31   | 2       | 16   | 4    | 5.67|
| Proposed ($m = 1$)| 31   | 2       | 18   | 4    | 5.66|
| ($m = 2$)         | 199  | 2       | 28   | 8    | 5.66|

**Table 6.** Comparison with other extended. Structure of SCMLI.

| Topologies         | $N_L$  | $N_S$  | $N_C$  |
|--------------------|--------|--------|--------|
| CHB                | $2m + 1$ | $4m$  | $0$    |
| [30]               | $6m + 1$ | $10m$ | $3m$   |
| [31]               | $4m + 1$ | $6m$  | $2m$   |
| [32]               | $2m + 1$ | $5m - 1$ | $m - 1$ |
| [33]               | $2m + 3$ | $m + 5$ | $m$    |
| [28]               | $4m - 1$ | $6m - 2$ | $2m - 1$ |
| Proposed symmetric | $4(3^m + 1)$ | $10m + 8$ | $4m$   |
| Proposed asymmetric| $2(3^m + (3^m + 1)3^m) + 1$ | $10m + 8$ | $4m$   |
Figure 10. Variation in number of levels with number of stages.

Figure 11. Variation in number of switches with number of levels.

Figure 12. Variation in number of capacitors with number of levels.
7. Simulation and Hardware Results

The proposed topology (symmetric as well as asymmetric configuration) was simulated and hardware results were also presented. For the simulation, MATLAB 2016 was used. A TMS320F28335 digital signal processor was used for the generation of switching pulses for IGBT switches. The driver circuit was developed using TLP 250. Table 7 shows the parameters used in both simulations as well as in hardware. Figure 13a–h shows the gating signals of switches of the 13 level switched capacitor multilevel inverter. Since switches \( T_2, T_4, T_6, T_8, S_2, S_4, S_6, S_8 \) are complementary switches to switches \( T_1, T_3, T_5, T_7, S_1, S_3, S_5, S_7 \), therefore, states of these switches were always opposite to the corresponding complementary switches. Figure 14i, j shows the output Voltage and current of the 13 level inverter for the resistive load condition. To represent the output current on the same graph, the amplitude of the current was multiplied by a hundred times of the actual value of current. The peak Values of Voltage and current were 72 Volts and 0.288 A, respectively. Figure 14k–n shows the Voltage across capacitor \( C_1 \) to \( C_4 \). The maximum Voltage across each capacitor was 12 Volts, and the variation in the capacitor Voltage (ripple Voltage) with respect to time was less than 10% observed in simulation results. The Voltage stress across each switch of the basic unit was \( V \) Volts and across each switch of cascaded H-bridge was \( 3V \) Volts. Figure 14o, p shows the Voltages across switches \( S_1 \) and \( T_1 \).

Table 7. Parameters used in simulation and hardware.

| Parameters/Components | Attributes |
|-----------------------|------------|
| Two DC Voltage supply | 12 V each for symmetric, 7.5 and 30 V for asymmetric configuration |
| Fundamental frequency | 50 Hz |
| Switching frequency   | 50 Hz |
| Four electrolytic capacitors | 4700 \( \mu \)F, 50 V |
| Two power diode       | 10 A |
| Eighteen IGBT Switches| 1200 V, 25 A |
| Load                  | 250 \( \Omega \) |

Some of the switching pulses (simulation and hardware) of 31 level switch capacitor multilevel inverters are depicted in Figure 15a–d. The peak amplitude of output Voltage of 112.5 Volts was observed in simulations, and almost similar results were obtained in hardware, as shown in Figure 15e,f. Voltage stress across capacitor \( C_1 \) was more as compared to \( C_2 \) and \( C_3 \). The simulated capacitor Voltages are shown in Figure 15g, and the experimental result is shown in Figure 15h. Figure 16 indicates the THD in the output Voltage for both symmetric (13 levels) and asymmetric (31 levels) SCMLI, namely 6.36% and 2.36% THD in output Voltage in 31 levels and 31 levels SCMLI, respectively. This THD Value is satisfied with the IEEE-519 2014 THD level standard.

![Simulation Result](image1)

![Hardware Result](image2)

Figure 13. Cont.
Figure 13. Gating signal of 13 level SCMLI: (a) and (b) Switching pulses for $T_1$, $T_3$ and $T_5$ (simulated and hardware respectively); (c) and (d) Switching pulses for $T_7$, $S_1$ and $S_3$ (simulated and hardware respectively); (e) and (f) Switching pulses for SCH$_1$, $S_5$ and $S_7$ (simulated and hardware respectively); (g) and (h) Switching pulses for SCH$_2$ (simulated and hardware respectively).

Figure 14. Cont.
Figure 14. (i) and (j) Output Voltage (20.5 V/diV) and output current (× 100) (0.205 A/diV). (i–l) Voltage across capacitors $C_1$, $C_2$, $C_3$, and $C_4$. (m–p) Voltage across switches $S_1$ and $T_1$.

Figure 15. Cont.
Figure 15. (a–d) Switching pulses across switches $T_1$, $T_3$, $T_5$, $T_7$, $S_1$, $S_3$. (e) and (f) Output Voltage of 31 level inVerter 31.25 V/diV. (g) and (h) Voltage across capacitors $C_1$, $C_2$, and $C_3$.

Figure 16. THD in output Voltage; (a) symmetric, (b) asymmetric.

8. Conclusions

In this paper, a boost switched-capacitor multileVel inVerter is proposed, which is the combination of a switched-capacitor cell and a cascaded H-bridge module. The capacitor in the switched capacitor cell behaVes as a DC source, and when they are connected in series with the DC source Voltage, the maximum output Voltage leVel is obtained. Using the nearest leVel modulation scheme, 13 leVels of symmetric and 31 leVels of asymmetric or output Voltage were achieVed. Determination of the rating of capacitance in terms of the longest discharging time for R and R-L load were also deriVed. MoreoVer, for achieVing a higher number of Voltage leVels, an extended structure of the proposed scheme was presented. The required number of deVice counts in terms of the number of stages for the higher number of Voltage generation was also deriVed. A comparatiVe analysis with other switched capacitor multileVel inVerters was also presented. Output Voltage THD was also analyzed and it satisfied the IEEE 519-1992 THD standard. Finally, the effectiVeness of the proposed scheme’s seVeral simulation and hardware results was presented.

Author Contributions: A.A. and M.A.: theoretical analysis, simulation and deVelopment of hardware prototype. J.A.: conceptualization and simulation. A.S. and M.Z.: conceptualization and Verification of the experimental results. M.T. and A.R.B.: Verified the mathematical analysis and simulation results and oVerall content of the paper. All authors have read and agreed to the published version of the manuscript.
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