A novel TDC/ADC hybrid reconstruction ROIC for LiDAR

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Abstract: A novel low complexity TDC/ADC hybrid reconstruction readout circuit (ROIC) is proposed for LiDAR. Compared with other TDC-based receivers, the proposed circuit can provide a higher sampling speed, while consuming less power than ADC-based receivers. The circuit structure is constructed based on a sampler circuit to realize full waveform reconstruction. To further reduce power consumption, a Time Control Technique (TCT) is utilized to enable the sampler circuit to work only when needed. More specifically, the bandwidth, gain and input referred noise current spectral density of analog front-end (AFE) circuit are set as 150 M, 83 dB and 3.25 pA/sqrt (Hz), respectively. The experiment results demonstrate the feasibility that the sampler circuit can reach more than 3 GHz sampling frequency with only 2.8 mW power consumption.

Keywords: LiDAR, sampler, TDC, ROIC

Classification: Integrated circuits

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1 Introduction

LiDAR, which can measure the distance from laser emitter to targets, is essential for autopilot, and the LiDAR can establish a 3D image and map, which can be utilized to achieve refinement of object recognition, navigation and collision avoidance. The pulse LiDAR readout circuit usually has two types of structures. One is based on time-to-digital-converter (TDC), which is composed of trans-impedance amplifier (TIA), TDC and comparator. The other is based on analog-to-digital converter (ADC), known as full waveform method, which is consisted of TIA and ADC. For the TDC based LiDAR, it has the digital conversion ability through threshold detection, and it can achieve high accuracy in short-range applications. However, the TDC based LiDAR is not able to obtain the strength information of the return pulse and may lose the characteristics of target objects. Also, it’s difficult for the LiDAR to identify the secondary return pulse, which is caused by multiple objects, following the primary one. Moreover, the walk time error caused by limited slew rate and response time with comparator can deteriorate the timing accuracy [1, 2, 3, 4]. For the ADC based LiDAR, it can extract more information, including peak and intensity which is relevant to the material and the rate of surface reflectivity of the target objects, from the digitalized full waveforms [5]. Therefore, with sophisticated extraction algorithm, ADC-based structure can provide much more comprehensive environment awareness. However, the precision of the whole waveform method depends on the sampling rate, and the ADC-based LiDAR consumes more power with higher sampling rates [6, 7, 8]. In order to solve the aforementioned problems, the work proposes a low complexity TDC/ADC hybrid reconstruction read-out circuit (ROIC) structure with TCT. Compared with
other TDC-based receivers, the proposed circuit can provide a higher sampling speed, while consuming less power than ADC-based receivers.

2 Architecture

Fig. 1 shows the implementation of the readout circuit. The transmitter generates a narrow pulse laser to illuminate the target. The receiver is used to sense the pulsed echo through a linear-mode Avalanche photodiode (APD) then capture the intensity signal and mark the timing point of the received echo in the ROIC circuits [9].

In the analog front-end (AFE) of the readout channel, the current generated by the laser detector is transferred to voltage by a TIA, and the signal is amplified and buffered into a high speed sampling network and a comparator. Then the capacitor array begins to sample the input at a constant interval continuously when the LiDAR initiates the scan process and sets the START signal high. When the first primary return pulse arrives, whose output voltage of readout channel comes cross the threshold voltage of comparator, the STOP signal is triggered. The capacitor array will stop sampling till a pre-defined delay time is reached, then the scan process is over. The exact time for the arrival of the first primary pulse is determined by a TDC block. After the scan process, the sample voltages on capacitor array and TDC result are readout sequentially, and the analog voltage can be converted to digital output with slow speed ADC. The time of the signal peak is  \( T \), define in Equation (1), where  \( T_N \) is TDC stop time, and  \( T_M \) is the time from signal peak to  \( T_N \), which can be calculated according to the sampling period.

\[
T = T_N - T_M
\]  

(1)

Similar design as the image sensor with burst mode is applied as the core of the circuit, and it is composed of a high speed sampling and analog storage array. The necessary sample clock in the circuit is generated by a shared delay chain and
distributed to all the receiver channels, and the equivalent sampling period is determined by the delay cell.

The typical operating frequency of laser transmitter is about 20 KHz, which means the time interval between two emitter lasers is 50 µs. For the detection range of 300 m, which is usually required in autonomous vehicles, the time of flight of the laser is around 2 µs. So this indicates only 4% of the laser emission period is effective. As for the width of laser pulse, a range from 5 ns to 10 ns is a reliable option and is short enough to achieve the desired accuracy. Taking the above timing parameters into consideration, the laser receiver stays idle for great proportion of the whole operation period, so the time occupied by return pulse is shorter. Therefore, it is feasible that high-speed sampling only during short effective time then the sampled signal is slowly quantized by low-speed ADC successively during idle time. Therefore, when multiple channel’s high-speed sampling working in a short effective period, it is feasible for the sampled signal to be slowly quantized by low-speed ADC in turn during idle time. It is obvious that the proposed TDC/ADC circuit can provide more detailed information compared with TDC-based receivers, while consuming lower power than ADC-based receivers [10].

3 Circuit implementation

3.1 Sampler

Fig. 2 shows a simplified schematic of the sampler cell, which is utilized to freeze the current signal in the sampling capacitors that is 250 fF. The sampler which is also called wave reconstruction circuit is basically a series of double inverters, capacitors and output buffers.

The circuit starts working when the START signal is set high. After setting the DELAY-EN signal high, a wave traverses through these inverters will produce the write signals for the sampling cells. A current source connected to the inverter allows to control the delay time $\Delta t$ at any time via the DELAYTIME-CON signal. For different applications, $\Delta t$ can be adjusted according to the pulse signal, and the range of the delay time is 290 ps–1 ns. Due to the limitation of the number of the capacitor array, the sampling operation proceeds in a cyclic manner. More specifically, after the last capacitor $C_{N-1}$ in the array samples the input, the first capacitor $C_0$ re-samples the coming input signal afterwards. The pulse width should not be longer than the product of the capacitor array number $N$ and the sampling interval $\Delta t$, otherwise the primary pulse will be overwritten by the cyclical sampling operation. $N$ can be defined in Equation (2),

$$N = 2 \cdot \frac{T_p}{\Delta t}$$

Where $T_p$ is echo pulse width, constant 2 makes the number of sampling points is twice as much as the minimum sampling points, to ensure that sampling circuit can complete to an input signal sampling. For example, $\Delta t = 500$ ps in which equivalent sampling frequency is 2 GHz, when pulse-width is 10 ns, so $N$ is 40. Even in the case of 3 G equivalent sampling rate, 40 capacitor can complete the sampling.

To reduce power consumption and pressure of the output buffer in AFE, the number of capacitors that works simultaneously is smaller than $N$. The number,
which can be viewed as sampling width $n$, can be defined in Equation (3), where $T_c$ is width of WIN-CON.

$$n = \frac{T_c}{\Delta t} \tag{3}$$

When the TRIGGER signal comes, the capacitor array will stop sampling till a predefined delay time is reached. Then the switch controlled by ENREAD gradually delivers the signals stored in the capacitors outputs to signal processing that includes low-speed ADC. Within 50 $\mu$s, the variation of sampling signal with time is ignored, so the external circuit has enough time to obtain the signal for processing.

To cancel the charge injection error and the effect of clock feed through, the sampler cell is realized leveraging the bottom plate sampling technique and delay units, Delay-$n_1$ and Delay-$p_1$, are added to make sure MN$_1$ and MP$_1$ will be closed after the MN$_0$ and MP$_0$. The structure of switches in sampler cell is shown in Fig. 2. Because the mobility of electrons and holes is different, Delay-$n_0$ and Delay-$p_0$ are added in order to make MN$_0$ and MP$_0$ open at the same time.

The area consumption is indeed a disadvantage of this method. In the work, in order to reduce the demand of the system for high-speed ADC, it is necessary to pay the cost of area within the receiving range. The selection of more advanced CMOS process can largely make up for this defect.

### 3.2 TIA

The main function of a TIA that depicted in Fig. 3 is to convert an input current from APD to voltage output [11]. In the design of the TIA, pseudo difference signal...
is used to improve the anti-interference ability. The structure of the main amplifier designed in TIA is shown in Fig. 3, which adopts the design scheme of a two-stage amplifier followed by a source follower. The first stage is a single-end output telescopic cascode amplifier, the second stage is a single-end output differential operation amplifier, and the final output is through the source follower which can effectively reduce the output impedance of the main amplifier, thus avoiding the load effect possibly caused by the feedback resistor Rf in the TIA structure [12]. VIN is the detector current input terminal, and the common mode bias voltage of VIP is generated by the resistance partial pressure. The input terminal voltage VB0 of the second stage amplifier is generated by a bias circuit, and the output of the second stage amplifier is adjusted by the source follower to the output common mode voltage. The pseudo difference reference voltage is connected to the unit gain buffer and output outwards. To ensure that the gain error of the unit gain buffer is small, the amplifier needs to have a higher open-loop gain. Therefore, a telescopic cascode amplifier is adopted, followed by a primary source follower, to realize the short connection between the amplifier output end and the negative input end.

3.3 TDC

TDC circuit, shown in Fig. 4, is used to measure the flight time of photons and counts how many clock periods have passed during the photon’s TOF. In this work, TDC is realized by a combination of two segments, which are a coarse TDC and a fine TDC [9]. For the coarse TDC to function as a conventional counter, a 15-bit linear feedback shift register (LFSR) has been applied. Taking up less circuit area is the most excellent advantage of LFSR over other counters. The fine TDC is the one to offer binary vernier bits. A higher temporal resolution has been achieved in fine TDC using the interpolation technique. The delay-line type fine TDC, which is made up of a 6-bit delay line and a parallel-to-serial module, is adopted to divide one clock period. Both outputs of the TDC are thermometer code and are converted into binary numbers.

4 Simulation results

The LiDAR ROIC simulation results in a 180 nm CMOS technology, the power supply voltage is 3.3 V. A sampling frequency from 800 MHz to 3.3 GHz is
achieved. Suppose the laser pulse period is 50 µs, the average power consumption of sampler block is 2.3 mW at 3.3 GHz, compared to the 50 mW without the TCT. Fig. 3 demonstrates TIA performance, where the 83 dB gain segment is reached at 150 MHz with a 3 dB cut-off frequency. For the TDC performance, a high precise temporal resolution of 290 ps is achieved.

Fig. 5 shows the simulated waveform of system. Input signal is a sinusoidal current in which amplitude is 50 µA, offset current is 53 µA. (a) (b) is the result of 100 M frequency, (c) (d) is the result of 150 M frequency.

Fig. 4. TDC structure
improve the driving ability, a source follower which is treated as a buffer is followed by the each sampler. The output voltage of sampler is raised after passing through the source follower, this limits the input range of current signals.

Table I is a comparison with state-of-art LiDAR SOCs, it shows that the structure proposed in this paper have a well compromise between power consumption and sampling rate.

5 Conclusion

A low complexity and low additional power cost wave reconstruction TDC-ADC Hybrid ROIC for pulse LiDAR is proposed. The novel ROIC adopts TCT to resolve the power consumption of high sampling rate requirement. Compared with the existing pulse LiDAR ROICs, the proposed scheme’s sampling frequency can vary from 900 MHz to 3.3 GHz only with an additional power consumption of 1.2 mW and 2.8 mW, respectively. With a high precise temporal resolution of 290 ps, the TDC based-LiDAR ROIC is an economic choice for the reliable self-driving programs.

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| Table I. Comparison with state-of-art LiDAR SOCs |
|--------------------------------------------------|
| [10] | [9] | [5] | This work |
| Technology | 28 nm | 180 nm | 180 nm | 180 nm |
| Full waveform | YES | NO | NO | YES |
| Amplitude | YES | NO | YES | YES |
| Sample rate | 400M | NO | NA | 800M -3G |
| Digital | YES | NO | NO | YES |
| Walk error | NO | 0.85 ns | NO | NO |
| CAPD (pF) | NA. | 1.5 | NA. | 2 |
| ZR,TIA (dB) | NA. | 106 | NA | 81.9 |
| f-3 dB (MHz) | 100 | 153 | NA | 150 |