The Undecidability of Network Coding with some Fixed-Size Messages and Edges

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Abstract

We consider a network coding setting where some of the messages and edges have fixed alphabet sizes, that do not change when we increase the common alphabet size of the rest of the messages and edges. We prove that the problem of deciding whether such network admits a coding scheme is undecidable. This can be considered as a partial solution to the conjecture that network coding (without fixed-size messages/edges) is undecidable. The proof, which makes heavy use of analogies with digital circuits, is essentially constructing a digital circuit of logic gates and flip-flops within a network coding model that is capable of simulating an arbitrary Turing machine.

Index Terms

Network coding, undecidability, uncomputability, digital circuits, entropic region.

I. INTRODUCTION

Network coding [1], [2] concerns the setting where messages are transmitted through a network of nodes, where each node is capable of performing encoding and decoding operations (instead of being limited to routing operations). There is a wealth of algorithms and computability results for network coding, e.g. [3], [4], [5], [6]. However, the other side of the picture – the hardness of network coding – is less clear. While linear network codes [2], [6] are usually simpler to design and analyze, they are generally insufficient in achieving the capacity [7], [8]. It was shown by Rasala Lehman [9] that deciding whether a network admits a coding scheme with a given alphabet size is NP-hard. Langberg, Sprintson and Bruck [10] showed that determining the minimum number of encoding nodes in a multicast network is NP-hard. Langberg and Sprintson [11] showed that approximating the capacity of a network is NP-hard. Refer to [12], [4], [13], [14] for more results on the hardness of network coding.

Nevertheless, the NP-hardness results do not completely settle the question on the hardness of network coding. It is currently unknown if network coding is even decidable, i.e., if there exists an algorithm where, given the network as input, outputs whether the network admits a coding scheme satisfying the decoding requirements [9], [15], [16], [17], [18], [19], [20]. For arguments in favor of the decidability of network coding, Rasala Lehman [9] noted that network coding would be decidable if one can compute a finite upper bound on the alphabet size given a network. If only routing is allowed, then the routing capacity of the network is computable, as shown by Cannons et al. [15]. For general network codes, computable inner bounds (e.g. [15]) and computable outer bounds (e.g. [21]) are known, though the computability of the capacity is unknown.

For arguments against decidability, Kühne and Yashfe [20] showed that the problem of finding whether a network admits a vector linear network code is undecidable, by proving an undecidability result about matroids and invoking the relationship between vector linear network codes and matroids in [22], though the relationship for general network codes is less clear. Dougherty [16] proposed a possible approach to prove undecidability via a reduction from Rhodes’ problem (the identity problem for finite groups), which is conjectured to be undecidable [23] (though there are holes in the arguments in [16]; also see [17]).

A closely related line of research is the characterization of the the entropic region $\Gamma_n^*$ and the almost-entropic region $\bar{\Gamma}_n^*$ (the closure of $\Gamma_n^*$) [24], [25], [26]. Their relation with network coding was elucidated in [27], [8], [28]. Non-Shannon-type inequalities, which are bounds on $\Gamma_n^*$, were studied in [24], [29], [30], [31], [32], [33]. It was shown by Li [34] that the problem of deciding whether $\Gamma_n^*$ intersects a given affine subspace is undecidable. See [19], [35], [36], [37], [38] for other works related to the decidability or undecidability of problems regarding $\Gamma_n^*$.

In this paper, we consider a network coding setting, which we call the partially fixed-size network, where some of the messages and edges have fixed alphabet sizes. All other messages and edges have a common alphabet size $k$. We show that the problem of deciding whether there exists $k$ such that this network admits a coding scheme is undecidable. This is the first undecidability result about general (linear or nonlinear) network codes. Note that if none of the messages and edges have fixed sizes, then the problem becomes the original network coding problem, and its decidability is unknown [9], [16]. On the other hand, if all messages and edges have fixed sizes, then the problem is clearly decidable by the arguments in [9] (since one can enumerate all encoding and decoding functions). It is perhaps surprising that combining these two cases makes the problem undecidable.
Due to the equivalence between network coding and index coding [39, 40] proved in [22, 41], we can also show the undecidability of an index coding problem where the sizes of some messages are fixed.

The undecidability is proved via a reduction from the periodic tiling problem [42, 43, 44, 45]. This is the same strategy employed in the proof of the undecidability of conditional affine information inequalities and conditional independence implication with a binary constraint by Li [34]. The proof in this paper shares many similarities with the proof in [34]. Nevertheless, the network coding setting is significantly more restrictive than the information inequality and the conditional independence setting in [34] (e.g., it is impossible to enforce that the signals along two edges are independent in network coding), making the proof in this paper considerably more challenging.

In the proof, we use several analogies with digital circuits, such as XOR gates, tristate buffers, switches, flip-flops and memory arrays. Using these components, we construct the tiles of the periodic tiling problem, which in turn can be used to model using digital circuit components. This approach is perhaps unexpected. While hardware implementation of network coding using digital circuits has been studied (e.g. [47]), it is quite unusual to liken the communication network itself to a digital circuit (with “wires” being the communication links, and “logic gates” being composed of nodes in the network).

A consequence of our result is that there is an explicit construction of a partially fixed-size network, where the non-existence of a coding scheme is unprovable in ZFC (assuming ZFC is consistent). This is because there is a Turing machine such that whether it halts is independent of ZFC, assuming ZFC is consistent [48, 49].

Notations

We write \( \mathbb{N}_0 = \{0, 1, \ldots\}, \mathbb{N}_+ = \{1, 2, \ldots\}, [a..b] := \mathbb{Z} \cap [a, b], [n] := \{1, \ldots, n\} \), \( X^b_a := (X_a, X_{a+1}, \ldots, X_b), X^n_a := X^n_a \). For a finite set \( S \subseteq \mathbb{N}_+ \), we write \( X_S := (X_{a_1}, \ldots, X_{a_k}) \), where \( a_1, \ldots, a_k \) are the elements of \( S \) in ascending order. For a random variable \( X \), write \( X' \) for its support, and \( |X| \) for its alphabet size. For a probability mass function \( p_X \), write \( \text{supp}(p_X) = \{x \in X : p_X(x) > 0\} \) for its support. For a countable set \( S \), write \( \mathcal{P}(S) \) for the set of probability measures over the sample space \( S \). The indicator of an event or statement \( E \) is written as \( 1\{E\} \in \{0, 1\} \).

II. Problem Formulation

A partially fixed-size network is represented by a directed acyclic graph \((V, E)\). Write the set of in-neighbors and out-neighbors of \( v \in V \) as \( N_{\text{in}}(v) \subseteq V \) and \( N_{\text{out}}(v) \subseteq V \) respectively. There are \( l \) independent messages \( M_1, \ldots, M_l \). The alphabet size of the message \( M_i \) is \( s_M(i) \in \mathbb{N}_0 \), where \( s_M(i) = 0 \) is a special value which means that \( M_i \) has size \( k \), where \( k \in \mathbb{N}_+ \) is the common default alphabet size of the network. We have

\[
M_i \sim \text{Unif}[0..s_M(i)] + k \cdot 1\{s_M(i) = 0\} - 1,
\]

i.e., the range of \( M_i \) is \( 0, \ldots, s_M(i) - 1 \) if \( s_M(i) > 0 \), and \( 0, \ldots, k - 1 \) if \( s_M(i) = 0 \). If \( s_M(i) = 0 \), we call \( M_i \) a default-size message. Otherwise, we call \( M_i \) a fixed-size message. Node \( v \in V \) has access to messages \( M_{A_v} \), and wants to decode the messages \( M_{B_v} \), where \( A_v, B_v \subseteq [l] \).

Let the signal transmitted along edge \((u, v) \in E\) be \( X_{u,v} \in \mathbb{N}_0 \). Each edge \((u, v) \in E\) has size \( s_E(u, v) \in \mathbb{N}_0 \), where \( s_E(u, v) = 0 \) is a special value with the same meaning as \( s_M(i) = 0 \). If \( s_E(u, v) = 0 \), we call \((u, v) \) a default-size edge. Otherwise, we call \((u, v) \) a fixed-size edge. Let the encoding function for edge \((u, v) \) be

\[
f_{u,v} : \mathbb{N}_0^{\{A_u\} \cup \{N_{\text{in}}(u)\}} \to [0..s_E(u, v) + k \cdot 1\{s_E(u, v) = 0\} - 1].
\]

We have

\[
X_{u,v} = f_{u,v}(M_{A_u}, \{X_{t,u}\}_{t \in N_{\text{in}}(u)}).
\]

The decoding function at node \( v \) is \( g_v : \mathbb{N}_0^{\{N_{\text{out}}(v)\}} \to \mathbb{N}_0^{\{B_v\}} \). The encoding and decoding functions do not need to be linear. The decoding constraint is that \( g_v(X_{u,v})_{u \in N_{\text{in}}(v)} = M_{B_v} \) almost surely for all \( v \in V \).

We call the network \((V, E, \{A_v\}, \{B_v\}, s_M, s_E) \) solvable if there exists \( k \in \mathbb{N}_+ \) and a coding scheme \((\{f_{u,v}\}, \{g_v\})\) such that the decoding constraint is satisfied. In the following sections, we will prove the following undecidability result.

**Theorem 1.** The following problem is undecidable: Given a partially fixed-size network \((V, E, \{A_v\}, \{B_v\}, s_M, s_E) \), decide whether it is solvable.

\(^1\)We remark that a natural approach to prove the undecidability of partially fixed-size network is to invoke the result that deciding whether \( \Gamma_n^\pm \) intersects a given affine subspace is undecidable [33], and the duality result between \( \Gamma_n^\pm \) and network coding [8]. This approach does not work since [33] only shows the undecidability of the intersection problem, not the problem of deciding whether a given vector is in \( \Gamma_n^\pm \). Nevertheless, [8] requires a specific vector \( h \) in order to design the capacities of the edges in the network that is asymptotically solvable if and only if \( h \in \Gamma_n^\pm \).

\(^2\)The undecidability of the periodic tiling problem [42, 45] was proved via a reduction from the halting problem [46].
Note that many previous models of network coding (e.g. [12], [9], [13], [7], [11]) assume the alphabet sizes for all messages and edges are the same. This corresponds to the case where we always have $s_M(i) = 0$ and $s_E(u, v) = 0$. The decidability of the solvability of a network in this case is still open. Another case is where we always have $s_M(i) > 0$ and $s_E(u, v) > 0$. In this case, the solvability is clearly decidable using the argument in [9], since we can simply enumerate all combinations of $\{f_{u,v}\}$ (which are functions with domains and codomains of bounded sizes) \(\mathcal{A}\). It is perhaps surprising that combining these two cases makes the solvability undecidable.

## III. GATES AND CHECKERS

In this section, we prove the main result by constructing a class of undecidable partially fixed-size networks. We will make heavy use of analogies with digital circuits in the proof, e.g. XOR gates, tristate buffers, switches and 2D memory organization.

A checker for the condition $Q \subseteq \mathcal{P}(\mathbb{N}_0^n)$ (a set of $n$-dimensional probability distributions) is a subnetwork of the communication network with $n$ inputs $X_1, \ldots, X_n$, with a purpose of checking that $p_{X^n} \in Q$. For example, the XOR checker described later has three inputs $M_1, M_2, Y \in \{0, 1\}$, and checks that $Y = M_1 \oplus M_2$ (up to relabelling of the values of $Y$, i.e., $Y = 1 - M_1 \oplus M_2$ is also valid). A checker does not have any output. A gate for the condition $Q \subseteq \mathcal{P}(\mathbb{N}_0^n)$ is a subnetwork with inputs $X_1, \ldots, X_n$, and outputs $Y_1, \ldots, Y_{n^2}$, where $p_{X^n} Y \in Q$ is guaranteed to be satisfied (note that a gate may also check certain conditions on the inputs). For example, the XOR gate described later has two inputs $M_1, M_2 \in \{0, 1\}$, and an output $Y \in \{0, 1\}$ which satisfies $Y = M_1 \oplus M_2$ (up to relabelling).

### A. XOR Gate and Checker

We construct the gate and checker for the exclusive or (XOR) function. We first state a simple fact about XOR: for $X_1, \ldots, X_n \sim\text{Bern}(1/2)$ and $Y \in \{0, 1\}$, we have $H(X_i | X_{[n]\{i\}}, Y) = 0$ for all $i \in [n]$ if and only if $Y = X_1 \oplus \cdots \oplus X_n$ or $Y = 1 - X_1 \oplus \cdots \oplus X_n$. We give the proof for the sake of completeness. Since $H(X_1 | X_{[n]\{1\}}, Y) = 0$, $Y$ is a function of $X^n$ (otherwise assume $p_{Y|X^n}(\cdot|x^n)$ is nondegenerate for some $x^n$, and then it is impossible to decode $X_1$ given $Y$ and $X^n = x^n$). Let $Y = f(X^n)$. Since $H(X_1 | X_{[n]\{1\}}, Y) = 0$, we have $f(x_1, \ldots, x_n) \neq f(1 - x_1, x_2, \ldots, x_n)$, and hence $f(x_1, \ldots, x_n) = 1 - f(1 - x_1, x_2, \ldots, x_n)$. By repeated use of this relation, we have $f(x_1, \ldots, x_n) = f(0, \ldots, 0)$ if $\sum x_i$ is even, $f(x_1, \ldots, x_n) = 1 - f(0, \ldots, 0)$ if $\sum x_i$ is odd. The result follows.

Given messages $M_1, M_2 \sim\text{Unif}[0, 1]$ and random variable $Y \in \{0, 1\}$, we can check whether $Y = M_1 \oplus M_2$ (up to relabelling of the values of $Y$) by checking $H(M_1 | Y, M_2) = H(M_2 | Y, M_1) = 0$. We denote this condition as $\mathsf{XOR}(M_1, M_2, Y)$.

Figure 1 shows the XOR checker. The label on an edge is its size $s_E(u, v)$. Unlabelled edges are assumed to have unlimited size (this is technically not allowed in the partially fixed-size network, though we will circumvent this problem at the end)

1. Actually it suffices to have $s_E(u, v) > 0$ for all $(u, v) \in E$ in order to show decidability, since it is always better to choose $k = 1$ in this case. Also, it suffices to have $s_M(i) > 0$ for all $i$ in order to show decidability, since we can choose $k$ large enough such that each edge $(u, v)$ with $s_E(u, v) = 0$ can simply forward the received signals at node $u$.

| Network coding component | Digital circuit analogy | Definition |
|--------------------------|------------------------|-----------|
| Edge in network          | Wire                   |           |
| Broadcast node           | Junction               |           |
| Source node / message    | Power supply           |           |
| Message signal to gate/checker | Power supply pin of a chip | Section III-A |
| Condition signal to gate/checker | Ground pin of a chip | Section III-A |
| Butterfly network        | XOR gate               | Section III-A |
| Tristate buffer gate     | Tristate buffer        | Section III-B |
| Switch                   | 2x2 crossbar switch / Flip-flop | Section III-C |
| Conditional switch       | Memory chip            | Section III-D |
| Conditional switch with tori select signal | 2D memory organization | Section III-F |

Table I

VARIOUS COMPONENTS AND CONSTRUCTIONS IN NETWORK CODING USED IN THIS PAPER, AND THEIR CORRESPONDING DIGITAL CIRCUIT ANALOGUES.
of the proof). The circles in the diagram (white circles and black dots) represent nodes in the network. The black dots are broadcast nodes (with in-degree one and with all outgoing edges having unlimited size) where, without loss of generality, can be assumed to be sending its input signal to each of its outgoing edge. The black dots can also be considered as junctions in the circuit diagram (crossings without dots are considered “no contact”). The “→” has to decode the message \( M_1 \). Therefore, the inputs \( M_1, M_2 \) to the XOR checker must be messages, though \( Y \) can come from the intermediate signals in the edges of the network. The small diamonds at the inputs \( M_1, M_2 \) indicate that these inputs must be messages (or combinations of messages). They are called the message signals to the checker.

Note that it is impossible to check for precise values of \( Y \), and it is impossible to distinguish between \( Y = M_1 + M_2 \) and \( Y = 1 - M_1 + M_2 \). In general, a checker can only check a condition on the random variables up to relabelling of those random variables.

Technically, the XOR checker is a checker for \( Q \) that is the set of joint distributions of \((M_1, M_2, Y)\), where \( Q \) satisfies that if \( p_{M_1, M_2, Y} \) has \( |\text{supp}(p_Y)| \leq 2 \), then \( p_{M_1, M_2, Y} \in Q \) if and only if \( p_{M_1, M_2, Y} \) is a relabelling of the joint distribution \( p_{M_1, M_2, Y} \) of \( M_1, M_2 \sim \text{Bern}(1/2) \), \( Y' = M_1 + M_2 \). Note that the checker assumes that the support size of \( Y \) is at most 2, and fails to check the XOR condition if this is not satisfied. The \( Q \) for all checkers and gates are defined via the same general pattern (if the non-message inputs have the prescribed sizes, then the condition is satisfied up to relabelling), and will be omitted in the remainder of the paper.

The XOR gate (Figure 1) is constructed by creating an output which is a binary function of \( M_1, M_2 \) that must satisfy the XOR condition enforced by the XOR checker. Note that the XOR gate is identical to the butterfly network [1], where the optimal code for binary alphabet uses the XOR operation.

We may also construct the conditional XOR checker, which has four inputs \( M_1, M_2, Y, W \) (where \( M_1, M_2 \sim \text{Unif}[0..1] \) is independent of \( W \); \( W \) is called the condition signal), and checks that \( Y = M_1 + M_2 + \eta_W \), where \( \eta_w \in \{0, 1\} \) for any \( w \). Intuitively, conditional on any \( W = w \), we have \( Y = M_1 + M_2 \) up to relabelling, where the relabelling can depend on \( w \) (since \( Y \) is binary, a relabelling of \( Y \) can be expressed as XOR with \( \eta_w \)). In general, the conditional version of a checker for \( Q \subseteq \mathcal{P}(\mathbb{N}_2^\alpha) \) conditioned on \( W \), which checks whether \( p_{X^n|W=w} \in Q \) for every \( w \in \mathcal{W} \) (i.e., checking whether the constraint of the checker holds conditioned on any \( W = w \)), can be constructed by adding the input \( W \) to every non-broadcast node in the checker. To see why this construction is valid, note that for each \( w \), if \( p_{X^n|W=w} \in Q \), then there exists encoding and decoding functions for nodes in the (unconditional) checker for \( Q \) which accepts \( X^n \sim p_{X^n|W=w} \). For an edge \((u, v)\), we can combine its encoding functions \( f_{u,v}(Z) \) for different \( w \)'s together to form one encoding function with an additional input \( W: f_{u,v}(Z, W) := f_{u,v,W}(Z) \). Therefore, by adding \( W \) to the input of each non-broadcast node, the resultant network accepts \( p_{X^n,W} \). Refer to Figure 1 for the conditional XOR checker.

Remark 2. The condition signal and message signal of a checker are analogous to the ground pin (GND) and the power supply pin (VCC) of an IC chip respectively. The ground is often connected to each internal component of the chip, whereas the
condition signal is connected to each non-broadcast node of the checker. The ground is connected to zero volts by default, whereas the condition signal is not connected to any message by default (i.e., connected to “zero information”), which reduces the conditional checker to the original unconditional one. A chip works when there is a voltage difference between the ground and the power supply (otherwise it may lead to unexpected and undesirable outcomes), whereas a checker works when there is a difference in information between the condition signal and the message signals. If the message signals are not connected (connected to “zero information”), or if the condition signal is connected to all messages (the highest amount of information), the checker will always accept its inputs, and a gate will produce meaningless outputs (that are any functions of the inputs).

Nevertheless, unlike an IC chip where the inputs to the ground and power supply pins are not supposed to change, we can choose a suitable condition signal to a checker in order to “selectively disable” the effect of some messages. Also, a checker can have multiple message signal inputs.

**B. Tristate Buffer Gate and Checker**

In digital circuits, the **tristate buffer** has two inputs $X, Y \in \{0, 1\}$, and the output $Z \in [0..2]$ satisfies $Z = 2$ (the high impedance state) if $Y = 0$, and $Z = X$ if $Y = 1$. Assuming that $X$ is independent of $Y$, we can check this by checking whether there exists $\tilde{Z} \in [0..2]$ such that

$$H(Y | Z) = H(Y | \tilde{Z}) = H(\tilde{Z} | X, Y) = H(X | Z, \tilde{Z}) = 0.$$ 

To check this, note that $H(Y | Z) = 0$ and $Z \in [0..2]$ implies that $p_{Z|Y=y}$ is degenerate for at least one value of $y$. Same for $p_{\tilde{Z}|Y=y}$. Since $H(X | Z, \tilde{Z}) = 0$, we know $p_{\tilde{Z}|Y=y}$ and $p_{\tilde{Z}|Y=y}$ must be nondegenerate for different values of $y$. This implies that $p_{Z|Y=y}$ is nondegenerate for one value of $y$. This gives us the desired distribution for $Z$. Refer to Figure 2 for the construction of the tristate buffer checker (assuming $X, Y$ are messages).

We can generalize this to a construction, which we call the $(b + 1)$-state buffer, which has two inputs $X \in \{0, 1\}$ and $Y \in [1..b]$, and output $Z \in [0..b]$ with $Z = Y$ if $Y \geq 2$, and $Z = X$ if $Y = 1$. Note that we use a different labelling of values compared to the tristate buffer. Assuming that $X$ is independent of $Y$, we can check this (up to relabelling) by checking whether there exists $Z_2, \ldots, Z_b$ (let $Z_1 = Z$) such that $Z_i \in [0..b]$ and $H(Z_i | X, Y) = 0$ for $i \in [2..b]$, $H(Y | Z_i) = 0$ for $i \in [1..b]$, and

$$H(X | Z^b) = 0. \quad (1)$$

We call the aforementioned conditions BSTATE$_b(X, Y, Z)$. The proof and the construction are similar to the tristate buffer.

**C. Switch**

In circuit-switching networks, a $2 \times 2$ crossbar switch is a device with two inputs $M_0, M_1 \in \{0, 1\}$, two outputs $Z_0, Z_1 \in \{0, 1\}$, and a state $\theta \in \{0, 1\}$, where $(Z_0, Z_1) = (M_0, M_1)$ if $\theta = 0$ (the “bar” state), and $(Z_0, Z_1) = (M_1, M_0)$ if $\theta = 1$ (the “cross” state). Assuming $M_0, M_1 \sim \text{Unif}[0..1]$ are messages, we can check whether $(M_0, M_1, Z_0, Z_1)$ forms a switch up to relabelling (for some fixed $\theta \in \{0, 1\}$) by checking whether

$$H(M_0, M_1 | Z_0, Z_1) = H(M_0, M_1 | Z_0, M_0 \oplus M_1) = H(M_0, M_1 | Z_1, M_0 \oplus M_1) = 0. \quad (2)$$

To prove this, note that if the above condition holds, then we have $H(Z_0, Z_1 | M_0, M_1) = 0$ and $H(Z_0, Z_1) = 2$, implying $Z_0, Z_1$ must be two distinct choices out of the following three choices: $M_0, M_1$ and $M_0 \oplus M_1$ (up to relabelling). If $Z_0 = M_0 \oplus M_1$, $Z_1$...
then we cannot have \( H(M_0, M_1 | Z_0, M_0 \oplus M_1) = 0 \). Hence we have \((Z_0, Z_1) = (M_0, M_1)\) or \((Z_0, Z_1) = (M_1, M_0)\). Refer to Figure 3 for an illustration of the switch gate.

While the switch is functionally almost identical to the 2 \( \times \) 2 crossbar switch in circuit-switching networks, for the purpose of our construction, a more suitable analogy would be a bistable multivibrator circuit which has two stable states (e.g., a flip-flop). Consider the inputs \( M_0, M_1 \) as two different “voltages”. The outputs \((Z_0, Z_1)\) can be either at the voltages \((M_0, M_1)\) or \((M_1, M_0)\), and both states are “stable” (i.e., satisfy the decoding requirements). Similar to how flip-flops can serve as the basic memory units of a digital circuit, we also regard the state \( \theta \in \{0, 1\} \) of the switch as the memory of our construction.

Consider an array of \( n \) switches, with the same input \((M_0, M_1)\), with outputs \((Z_{1,0}, Z_{1,1}), \ldots, (Z_{n,0}, Z_{n,1})\), and with states \( \theta_1, \ldots, \theta_n \). We call this a physical memory array (to distinguish from the “virtual memory array” in the next section). We can impose the constraint that \((\theta_1, \ldots, \theta_n) \neq (a_1, \ldots, a_n)\) for any fixed \( a_1, \ldots, a_n \in \{0, 1\}\) by requiring that \( H(M_1 | Z_{1,a_1}, \ldots, Z_{n,a_n}) = 0 \) (since \( Z_{i,a_i} = M_1 \) if \( \theta_i \neq a_i \)). By repeated uses of this constraint, we can impose the constraint that \((\theta_1, \ldots, \theta_n) \in \Theta\) for an arbitrary set \( \Theta \subseteq \{0, 1\}^n\). We call a checker that checks this constraint a set checker for \( \Theta \). Refer to Figure 4 for an example where we impose that \((\theta_1, \ldots, \theta_3)\) is a one-hot encoding (exactly one of them is 1).

D. Conditional Switch and Virtual Memory Array

Similar to the conditional XOR checker, we can also define the conditional switch on \( M_0, M_1, Z_0, Z_1, W \) (where \( M_0, M_1 \sim \text{Unif}[0..1] \) is independent of \( W \)) by conditioning on \( W \) on each term in \( (2) \) (refer to Figure 3 for an illustration). This allows the state to depend on \( W \), i.e., we have

\[
(Z_0, Z_1) = (M_0 \oplus \eta_{0,W}, M_1 \ominus \theta_W \oplus \eta_{1,W}),
\]
where \( \theta_w, \eta_{0,w}, \eta_{1,w} \in \{0, 1\} \) for any \( w \in W \). The terms \( \eta_{0,w}, \eta_{1,w} \) are needed since the switch checker is only checking the distribution of \((M_0, M_1, Z_0, Z_1)\) up to relabelling, and hence in the conditional version of the switch checker, the labelling for each \( w \) may be different, and \( Z_0 \) may be flipped in different ways for different \( w \).

Therefore, one can create a virtual memory array \( \{\theta_w\}_{w \in W} \) without physically adding more switches. The \( w\)-th bit \( \theta_w \) can be “retrieved” by fixing the input \( W = w \). This is analogous to a memory array in digital circuit, with \( W \) being the select signal.

While a virtual memory array has the advantage of requiring fewer switches (the number of nodes in the construction does not need to scale with the number of bits in the memory), the operations that can be performed are significantly more limited compared to a physical memory array. For example, it is impossible to enforce that \( \theta_w = 0 \) for a fixed \( w \). One cannot even specify a value \( w \) in a well-defined manner since the network coding setting is invariant under relabelling of the random variables. Therefore, any condition that can be enforced on \( \{\theta_w\}_{w \in W} \) must be invariant under permutation of the values in \( W \).

Assume \( W \sim \text{Unif}[1..b] \). We can check whether \( \theta_1 = \cdots = \theta_b \) by checking whether there exists \( G \in \{0, 1\} \) such that \( H(G|Z_0, W) = 0 \) and \( H(M_0, M_1|G, M_0 \oplus M_1) = 0 \). Note that \( H(M_0, M_1|G, M_0 \oplus M_1) = 0 \) implies that \( G = M_0 \) or \( G = M_1 \) (up to relabelling), which implies \( \theta_1 = \cdots = \theta_b \) (otherwise it is impossible to determine \( M_0 \) from \( W \) and \( Z_0 = M_{\theta_0} \oplus \eta_{0,w} \), and it is also impossible to determine \( M_1 \)). For the other direction, if \( \theta_1 = \cdots = \theta_b = 0 \), we can take \( G = Z_0 \oplus \eta_{0,w} \), which equals \( M_0 \). The case for \( \theta_1 = \cdots = \theta_b = 1 \) is similar. Refer to Figure 5 for the construction, which we call the virtual equality checker with select signal \( W \).

The conditional virtual equality checker is the conditional version of the virtual equality checker. Assume \( W = (W_1, W_2) \), where \( W_1 \sim \text{Unif}[1..b_1] \) is independent of \( W_2 \sim \text{Unif}[1..b_2] \). The conditional virtual equality checker (conditioned on \( W_1 \)) is obtained by adding \( W_1 \) to the input of all non-broadcast nodes of the virtual equality checker with select signal \( W = (W_1, W_2) \). It checks that \( \theta_{w_1,1} = \cdots = \theta_{w_1,b_2} \) for all \( w_1 \in [1..b_1] \). Refer to Figure 5 for the illustration.

Assume \( W \sim \text{Unif}[1..b] \). We can check whether \( (\theta_1, \ldots, \theta_b) \neq (0, \ldots, 0) \) by checking whether there exists \( G \in [0..b] \) such that \( H(G|Z_0, W) = 0 \), and the \((b+1)\)-state buffer condition \( \text{BSTATE}_{b_1}(M_1, W; G) \) holds. To prove this, note that if \( \theta_1 = 1 \), then we can take \( G = W \) if \( W \geq 2 \), and \( G = Z_0 \oplus \eta_{0,1} = M_1 \) if \( W = 1 \). For the other direction, if \( (\theta_1, \ldots, \theta_b) = (0, \ldots, 0) \), then we have \( Z_0 = M_0 \oplus \eta_{0,w} \) independent of \( M_1 \), so \( G \) must be independent of \( M_1 \), and \( \text{BSTATE}_{b_1}(M_1, W; G) \) cannot hold. Refer to Figure 5 for the construction, which we call the virtual b-ary OR checker with select signal \( W \) (note that \( W \) must be a message, or a combination of messages, due to the construction of \((b+1)\)-state buffer).

The conditional virtual b-ary OR checker is the conditional version of the virtual b-ary OR checker. Assume \( W = (W_1, W_2) \), where \( W_1 \sim \text{Unif}[1..b_1] \) is independent of \( W_2 \sim \text{Unif}[1..b_2] \). The conditional virtual \( b_2 \)-ary OR checker (conditioned on \( W_1 \)) is obtained by adding \( W_1 \) to the input of all non-broadcast nodes of the virtual \( b_2 \)-ary OR checker with select signal \( W = (W_1, W_2) \). It checks that \( (\theta_{w_1,1}, \ldots, \theta_{w_1,b_2}) \neq (0, \ldots, 0) \) for all \( w_1 \in [1..b_1] \).

Note that it is possible to combine virtual and physical memory arrays by having a physical array of conditional switches. We call this a virtual-physical memory array, which is an array of \( n \) conditional switches, with the same input \((M_0, M_1, W)\), with

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5Note that it uses the \((b_2+1)\)-state buffer instead of the \((b_1,b_2+1)\)-state buffer. Although \( W \) has alphabet size \( b_1b_2 \) which seems to violate the requirement of \( \text{BSTATE}_{b_2} \), it does not violate the conditional version of \( \text{BSTATE}_{b_2} \) conditioned on \( W_1 \) since the conditional cardinality of \( W \) given \( W_1 \) is \( b_2 \).
Figure 6. The cycles gate. The edge labelled $k$ has the default size $k$ (i.e., $c_E(u, v) = 0$).

outputs $(Z_{1,0}, Z_{1,1}), \ldots, (Z_{n,0}, Z_{n,1})$, and with states $\{\theta_{w,i}\}_{w \in W, i \in [n]}$. As in the case of physical memory array, a conditional set checker for $\Theta$ (which is the conditional version of the set checker where $W$ is added to the input of all non-broadcast nodes) checks that $(\theta_{w,1}, \ldots, \theta_{w,n}) \in \Theta$ for all $w \in W$, where $\Theta \subseteq \{0,1\}^n$ is an arbitrary set.

E. Cycles

Some of the constructions in Sections 3II-E and 3III-F are similar to those in 34, though we present them here in a different way using the digital circuit analogy.

In this section, we construct a network to check the cycles constraint CYCS$(X_1, X_2)$ in 34, which is the constraint that $X_1, X_2$ are uniform with the same alphabet size, the pair $(X_1, X_2)$ is uniformly distributed over its support, and all vertices in their characteristic bipartite graph have degree 2, that is, the characteristic bipartite graph consists of disjoint cycles. We also define $U \sim \text{Unif}\{0,1\}$ as in 34, which corresponds to the color in a 2-coloring of the edges of the bipartite graph such that no two edges sharing a vertex have the same color. Given $X_1 \sim \text{Unif}\{0..k-1\}$ (a default-size message) independent of $U \sim \text{Unif}\{0,1\}$ (a fixed-size message), we can check whether $X_2$ satisfies the cycles constraint by checking that $|X_2| \leq k$, and

$$H(U|X_1, X_2) = H(X_2|X_1, U) = H(X_1|X_2, U) = 0.$$  

It is straightforward to check that the above conditions are satisfied if the cycles constraint is satisfied. For the other direction, assume the above conditions are satisfied. Since $H(X_1, U|X_2) = 0$, $H(X_1|U) = \log(2k)$ and $H(X_2) \leq \log k$, we have $U$ independent of $X_2$. The rest follows from the same argument as in CYCS$(X_1, X_2)$ in 34. Refer to Figure 6 for the construction.

F. 2D Memory Organization and Undecidability

In the periodic tiling problem 42, 43, 44, 45, we try to tile a torus with a set of square tiles, where each side of the square is colored by one of $c$ colors. Given a set of tiles (each specified by a 4-tuple of colors), the problem is to decide whether one can tile a torus using the set of tiles (repeated use of the same tile is allowed, but no rotation or reflection is allowed), such that adjacent tiles have the same color on their touching sides. By treating sides of squares as vertices in a torus, we obtain the grid of the torus (rotated 45\(^\circ\) compared to the grid of the tiles). Therefore, the periodic tiling problem is equivalent to coloring the vertices of a torus such that the 4 vertices in each even face of the torus (like the black squares in a chess board) must have a 4-tuple of colors that is in the set of allowed 4-tuples. Refer to Figure 7 for an illustration.

The main idea of the proof of the reduction from the periodic tiling problem in 34 is to enforce the color restriction of the torus using conditional independence relations and affine existential information predicates (AEIPs) 50, 34. Here we will follow the same general idea, but use gates and checkers instead of AEIPs to enforce the color restriction.

By taking two independent copies of cycles on $(X_1, X_2, U)$ and $(Y_1, Y_2, V)$ (i.e., letting $X_1, Y_1 \sim \text{Unif}\{0..k-1\}$, $U, V \sim \text{Unif}\{0,1\}$ all independent), we obtain a collection of tori. Each tuple $(x_1, u, y_1, v)$, or equivalently, a tuple $(x_1, x_2, y_1, y_2)$ within the range of $(X_1, X_2, Y_1, Y_2)$ (recall that by the definition of cycles, one can deduce $U$ from $X_1, X_2$, and deduce $X_2$ from $X_1, U$), corresponds to a vertex in the collection of tori. Regard $(x_1, x_2)$ as the horizontal coordinates of the vertex, and $(y_1, y_2)$ as the vertical coordinates of the vertex. Following the definitions in 34, two vertices $(x_1, x_2, y_1, y_2)$ and $(\tilde{x}_1, \tilde{x}_2, \tilde{y}_1, \tilde{y}_2)$ are connected by a horizontal edge in the tori if $(x_1, y_1, y_2) = (\tilde{x}_1, \tilde{y}_1, y_2)$ or $(x_2, y_1, y_2) = (\tilde{x}_2, \tilde{y}_1, y_2)$. Those vertices are connected by a vertical edge in the tori if $(x_1, x_2, y_1) = (\tilde{x}_1, \tilde{x}_2, y_1)$ or $(x_1, x_2, y_2) = (\tilde{x}_1, \tilde{x}_2, y_2)$. We call a set of four vertices a type 11 face if their $x_1$ and $y_1$ coordinates are the same. We call a set of four vertices a type 22 face if their $x_2$ and $y_2$ coordinates are the same. The type 11 faces and the type 22 faces are the even faces of the tori. It was proved in 34 that as long as we can enforce the following three types of conditions, then the color restriction in the periodic tiling problem can be enforced, and hence the coloring problem of the tori (satisfying a list of such conditions) is undecidable:

1) **Horizontal edge equality condition.** The colors $c_1, c_2$ of the two vertices on each horizontal edge must satisfy $1\{c_1 \in C\} = 1\{c_2 \in C\}$, where $C$ is any fixed set of colors. The vertical edge equality condition is defined similarly 6

2) **Horizontal edge OR condition.** The colors $c_1, c_2$ of the two vertices on each horizontal edge must satisfy $c_1 \in C$ or $c_2 \in C$, where $C$ is any fixed set of colors. The vertical edge OR condition is defined similarly 7

6The characteristic bipartite graph is the graph with edge $(x_1, x_2)$ if and only if $p_{X_1, X_2}(x_1, x_2) > 0$.
7This is used in the restriction SAT\(_{\neq 1/2}\) in 34 that the sign of the colors within a torus must be the same.
8This is used in the restriction SAT\(_{\leq 1/2}\) in 34 that each horizontal edge connect a group 1 vertex and a group 2 vertex, or a group 3 vertex and a group 4 vertex; and that each vertical edge connect a group 1 vertex and a group 4 vertex, or a group 2 vertex and a group 3 vertex.
3) **Type 11 face OR condition.** The colors $c_1, \ldots, c_4$ of the four vertices in each type 11 face must satisfy that $c_i \in C$ for some $i \in [4]$, where $C$ is any fixed set of colors. The type 22 face OR condition is defined similarly.\footnote{This is used in the restriction SAT \( \leq 3/4 \) in \cite{34} that enforces that each even face have colors that is in the set of allowed 4-tuples of colors.}

We now prove that these conditions can be enforced via gates and checkers. Consider a virtual-physical memory array with $n$ conditional switches, with $(X_1, U, Y_1, V)$ being the select signal. The memory of this array is $\{\theta_{x_1,u,y_1,v,i}\}$ with $4nk^2$ bits. This is analogous to the 2-dimensional memory organization in memory chips\footnote{Technically, it is closer to the “2.5D” organization which contains a row decoder and a column decoder.} with $(X_1, U)$ being the column select signal, and $(Y_1, V)$ being the row select signal. Let the set of colors be $[N]$. Each color $c \in [N]$ is encoded into $n = 2^N - 2$ bits $\phi(c) \in \{0,1\}^{2^N-2}$, where each entry of $\phi(c)$ is indexed by a nonempty proper subset $A \subseteq [N]$, and $(\phi(c))_A = 1\{c \in A\}$.

We can therefore use the states of $n$ switches (indexed by subsets of $[N]$) to represent a color.

Let the color of the vertex $(x_1, u, y_1, v)$ be $c(x_1, u, y_1, v)$. We encode the collection of colors in the tori using the virtual-physical memory array by $\theta_{x_1,u,y_1,v,A} = (\phi(c(x_1, u, y_1, v)))_A$. We first need to enforce that $\{\theta_{x_1,u,y_1,v,i}\}$ is a valid encoding. This can be enforced by a conditional set checker (Section III-D) for $\Theta = \{\phi(c) : c \in [N]\}$, conditioned on $(X_1, U, Y_1, V)$.

To enforce the horizontal edge equality condition for a set of colors $C \subseteq [N]$, we use the conditional virtual equality checker (Section III-D) on the $C$-th switch with select signal $(X_1, U, Y_1, V)$, conditioned on $(X_1, Y_1, V)$. To enforce the face OR condition for type 11 faces, we use the conditional virtual 2-ary OR checker. To enforce the face OR condition for type 11 faces, we use the conditional virtual 4-ary OR checker with select signal $(X_1, U, Y_1, V)$, conditioned on $(X_1, Y_1, V)$. To enforce the face OR condition for type 22 faces, we use the conditional virtual 4-ary OR checker with select signal $(X_1, U, Y_1, V)$, conditioned on $(X_2, Y_2)$. Note that we cannot use the select signal $(X_2, U, Y_2, V)$ since the select signal of the virtual OR checker must be messages ($X_1$ is a message, but $X_2$ is not). Nevertheless, using $(X_1, U, Y_1, V)$ has the same effect since they contain the same information as $(X_2, U, Y_2, V)$. Refer to Figure 3 for an illustration of the checker for type 22 face OR condition.

Recall that we assume all unlabelled edges in the diagrams have unlimited sizes. It suffices to take the size of unlabelled edges to be the product of the sizes of the messages in the network. If this exceeds $k$, create enough parallel edges for each unlabelled edge (e.g. if the product of sizes of messages is $10k^2$, then create three parallel edges with sizes 10, $k$ and $k$ for each unlabelled edge). While technically the definition of the partially fixed-size network does not allow parallel edges, we can create a relay node for each parallel edge to make the edges distinct.

The proof is completed by invoking the reduction from the periodic tiling problem to the problem of coloring the torus satisfying the aforementioned three types of conditions proved in \cite{34}.

**IV. INDEX CODING**

We define one particular problem on index coding \cite{39, 40}, which we call partially fixed-size index coding. The messages are defined in the same manner as partially fixed-size network. There are $l$ independent messages $M_1, \ldots, M_l$. The alphabet...
size of the message $M_i$ is $s_M(i) \in \mathbb{N}_0$, where $s_M(i) = 0$ means that $M_i$ has size $k$, where $k \in \mathbb{N}_+$ is the common default alphabet size. We have

$$M_i \sim \text{Unif}[0..s_M(i) + k \cdot 1\{s_M(i) = 0\} - 1].$$

The server observes $M^l$ and outputs $X = f(M^l)$, where $f : \mathbb{N}_0^k \rightarrow [0..ak^b - 1]$, where $a \in \mathbb{N}_+$, $b \in \mathbb{N}_0$ are fixed (we enforces that the alphabet size of $X$ is at most $ak^b$). There are $n$ clients, where client $j \in [n]$ observes $X$ and $M_{A_j}$, $A_j \subseteq [l]$, and wants to decode $M_{B_j}$, $B_j \subseteq [l]$. The decoding function of client $j$ is $g_j : \mathbb{N}_0^{k+|A_j|} \rightarrow \mathbb{N}_0^{B_j}$. The decoding requirement is that $g_j(f(M^l), M_{A_j}) = M_{B_j}$ for all $j \in [n]$ almost surely.

By the equivalence between network coding and index coding proved in [41], the partially fixed-size index coding problem is also undecidable.

**Corollary 3.** The following problem is undecidable: Given a partially fixed-size index coding problem $(s_M, a, b, \{A_j\}, \{B_j\})$, decide whether there exists $k \in \mathbb{N}_+$, encoding function $f$ and decoding functions $\{g_j\}$ such that the decoding requirement is satisfied.

**V. Future Work**

We have proved that whether a given partially fixed-size network admits a coding scheme is undecidable. By tracing the construction in the proof, we can see that the only messages are $M_0, M_1, U, V$ (size 2) and $X_1, Y_1$ (default size $k$), and only the sizes 2, 3, 5 and $k$ are required for edges. We conjecture that only the sizes 2 and $k$ are needed to prove undecidability.

**Conjecture 4.** The following problem is undecidable: Given a partially fixed-size network $(V, E, \{A_u\}, \{B_v\}, s_M, s_E)$ where $s_M(i), s_E(u, v) \in \{0, 2\}$ for all $i, u, v$, decide whether it is solvable.

The main obstacle is to enforce the tristate and $(4 + 1)$-state buffer conditions using only size-2 edges.

Another future direction is to study the asymptotic almost solvability of the partially fixed-size network. In this setting, we have a default size $k_1$ for default-size messages, and another default size $k_2$ for default-size edges. The asymptotic capacity of the network is

$$\limsup_{k_2 \to \infty} \frac{\log k_1^*(k_2)}{\log k_2},$$

where $k_1^*(k_2)$ is the largest possible $k_1$ for a fixed $k_2$ such that the network admits a coding scheme. We conjecture that finding the capacity is also undecidable.
Conjecture 5. The following problem is undecidable: Given a partially fixed-size network \((V, E, \{A_v\}, \{B_v\}, s_M, s_E)\), decide whether its asymptotic capacity is at least 1.

It was shown in [13] that allowing the rate to be slightly below capacity can reduce the alphabet size drastically. Therefore, it is unclear if the asymptotic almost solvability of the partially fixed-size network is as hard as exact solvability.

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REFERENCES
[1] R. Ahlswede, N. Cai, S.-Y. Li, and R. W. Yeung, “Network information flow,” IEEE Transactions on information theory, vol. 46, no. 4, pp. 1204–1216, 2000.
[2] S.-Y. Li, R. W. Yeung, and N. Cai, “Linear network coding,” IEEE transactions on information theory, vol. 49, no. 2, pp. 371–381, 2003.
[3] S. Jaggi, P. Sanders, P. A. Chou, M. Effros, S. Egner, K. Jain, and L. M. Tolhuizen, “Polynomial time algorithms for multicast network code construction,” IEEE Transactions on Information Theory, vol. 51, no. 6, pp. 1973–1982, 2005.
[4] N. J. A. Harvey, “Deterministic network coding by matrix completion,” Ph.D. dissertation, Massachusetts Institute of Technology, 2005.
[5] Z. Li, B. Li, D. Jiang, and L. C. Lau, “On achieving optimal throughput with network coding,” in Proceedings IEEE 24th Annual Joint Conference of the IEEE Computer and Communications Societies., vol. 3. IEEE, 2005, pp. 2184–2194.
[6] T. Ho, M. Médard, R. Koetter, D. R. Karger, M. Effros, J. Shi, and B. Leong, “A random linear network coding approach to multicast,” IEEE Transactions on Information Theory, vol. 52, no. 10, pp. 4413–4430, 2006.
[7] R. Dougherty, C. Freiling, and K. Zeger, “Insufficiency of linear coding in network information flow,” IEEE transactions on information theory, vol. 51, no. 8, pp. 2745–2759, 2005.
[8] T. Chan and A. Grant, “Duality between entropy functions and network codes,” IEEE Trans. Inf. Theory, vol. 54, no. 10, pp. 4470–4487, 2008.
[9] A. R. Lehman, “Network coding,” Ph.D. dissertation, Massachusetts Institute of Technology, 2005.
[10] M. Langberg, A. Sprintson, and J. Bruck, “The encoding complexity of network coding,” IEEE Transactions on Information Theory, vol. 52, no. 6, pp. 2386–2397, 2006.
[11] M. Langberg and A. Sprintson, “On the hardness of approximating the network coding capacity,” IEEE Transactions on Information Theory, vol. 57, no. 2, pp. 1008–1014, 2011.
[12] A. R. Lehman and E. Lehman, “Complexity classification of network information flow problems,” in Proceedings of the fifteenth annual ACM-SIAM symposium on Discrete algorithms, 2004, pp. 142–150.
[13] ——, “Network coding: Does the model need tuning?” in SODA, vol. 5, 2005, pp. 499–504.
[14] H. Yao and E. Verbin, “Network coding is highly non-approximable,” in 2009 47th Annual Allerton Conference on Communication, Control, and Computing (Allerton). IEEE, 2009, pp. 209–213.
[15] J. Cannons, R. Dougherty, C. Freiling, and K. Zeger, “Network routing capacity,” IEEE Transactions on Information Theory, vol. 52, no. 3, pp. 777–788, 2006.
[16] R. Dougherty, “Is network coding undecidable?” in Applications of Matroid Theory and Combinatorial Optimization to Information and Coding Theory, 2009.
[17] R. Dougherty, C. Freiling, and K. Zeger, “Network coding and matroid theory,” Proceedings of the IEEE, vol. 99, no. 3, pp. 388–405, 2011.
[18] R. Bassoli, H. Marques, J. Rodriguez, K. W. Shum, and R. Tafazolli, “Network coding theory: A survey,” IEEE Communications Surveys & Tutorials, vol. 15, no. 4, pp. 1950–1978, 2013.
[19] A. Gómez, C. Mejía, and J. A. Montoya, “Network coding and the model theory of linear information inequalities,” in 2014 International Symposium on Network Coding (NetCod). IEEE, 2014, pp. 1–6.
[20] L. Kühne and G. Yashfe, “Representability of matroids by c-arrangements is undecidable,” in 2006 IEEE ISIT. IEEE, Jun 2007, pp. 233–236.
[21] K. Makarychev, Y. Makarychev, A. Romashchenko, and N. Vereshchagin, “A new class of non-Shannon-type inequalities for entropies,” Information theory and network coding, 2006.
[22] Z. Zhang and R. W. Yeung, “On characterization of entropy function via information inequalities,” IEEE Trans. Inf. Theory, vol. 44, no. 4, pp. 1440–1452, 1998.
[23] R. Yeung, Information theory and network coding. Springer Science & Business Media, 2008.
[24] X. Yan, R. W. Yeung, and Z. Zhang, “An implicit characterization of the achievable rate region for acyclic multisink network coding,” IEEE Trans. Inf. Theory, vol. 58, no. 9, pp. 5625–5639, 2012.
[25] K. Makarychev, Y. Makarychev, A. Romashchenko, and N. Vereshchagin, “A new class of non-Shannon-type inequalities for entropies,” Communications in Information and Systems, vol. 2, no. 2, pp. 147–166, 2002.
[26] R. Dougherty, C. Freiling, and K. Zeger, “Six new non-Shannon information inequalities,” in 2006 IEEE ISIT. IEEE, Jul 2006, pp. 233–236.
[27] F. Matiž, “Infinitely many information inequalities,” in 2007 IEEE ISIT. IEEE, Jun 2007, pp. 41–44.
[28] W. Xu, J. Wang, and J. Sun, “A projection method for derivation of non-Shannon-type information inequalities,” in 2008 IEEE ISIT. IEEE, 2008, pp. 2116–2120.
[29] R. Dougherty, C. Freiling, and K. Zeger, “Non-Shannon information inequalities in four random variables,” arXiv preprint arXiv:1104.3602, 2011.
[34] C. T. Li, “The undecidability of conditional affine information inequalities and conditional independence implication with a binary constraint,” *arXiv preprint arXiv:2104.05634*, 2021.

[35] A. Gómez, C. Mejía, and J. A. Montoya, “Defining the almost-entropic regions by algebraic inequalities,” *International Journal of Information and Coding Theory*, vol. 4, no. 1, pp. 1–18, 2017.

[36] A. R. Gómez Ríos, “On the theory of polynomial information inequalities,” Ph.D. dissertation, Departamento de Matemáticas, Universidad Nacional de Colombia, Bogotá, Colombia, 2018.

[37] M. A. Khamis, P. G. Kolaitis, H. Q. Ngo, and D. Suciu, “Decision problems in information theory,” *arXiv preprint arXiv:2004.08783*, 2020.

[38] C. T. Li, “First-order theory of probabilistic independence and single-letter characterizations of capacity regions,” *arXiv preprint arXiv:2108.07324*, 2021.

[39] Z. Bar-Yossef, Y. Birk, T. Jayram, and T. Kol, “Index coding with side information,” *IEEE Transactions on Information Theory*, vol. 57, no. 3, pp. 1479–1494, 2011.

[40] E. Lubetzky and U. Stav, “Nonlinear index coding outperforming the linear optimum,” *IEEE Transactions on Information Theory*, vol. 55, no. 8, pp. 3544–3551, 2009.

[41] M. Effros, S. El Rouayheb, and M. Langberg, “An equivalence between network coding and index coding,” *IEEE Transactions on Information Theory*, vol. 61, no. 5, pp. 2478–2487, 2015.

[42] H. Wang, “Proving theorems by pattern recognition-II,” *Bell system technical journal*, vol. 40, no. 1, pp. 1–41, 1961.

[43] R. Berger, *The undecidability of the domino problem*. American Mathematical Soc., 1966, no. 66.

[44] Y. S. Gurevich and I. Koryakov, “Remarks on Berger’s paper on the domino problem,” *Siberian Mathematical Journal*, vol. 13, no. 2, pp. 319–321, 1972.

[45] J. Mazoyer and I. Rapaport, “Global fixed point attractors of circular cellular automata and periodic tilings of the plane: undecidability results,” *Discrete Mathematics*, vol. 199, no. 1-3, pp. 103–122, 1999.

[46] A. M. Turing, “On computable numbers, with an application to the Entscheidungsproblem,” *Proceedings of the London mathematical society*, vol. 2, no. 1, pp. 230–265, 1937.

[47] T. Yoon and J. Park, “FPGA implementation of network coding decoder,” *IJCSNS Int. J. Comp. Sci. Netw. Secur*, vol. 10, no. 12, pp. 34–39, 2010.

[48] P. Michel, “The busy beaver competition: a historical survey,” *arXiv preprint arXiv:0906.3749*, 2009.

[49] A. Yedidia and S. Aaronson, “A relatively small Turing machine whose behavior is independent of set theory,” *arXiv preprint arXiv:1605.04343*, 2016.

[50] C. T. Li, “An automated theorem proving framework for information-theoretic results,” in *2021 IEEE International Symposium on Information Theory (ISIT)*, 2021, pp. 2750–2755.