A Blocker-Resilient Receiver with Second-order Impedance Mapping for NB-IoT Applications

Tingting Shi¹, Sizheng Chen¹, Na Yan¹ and Hao Min¹

Abstract Wideband receiver used in IoT applications operating at sub-GHz suffers from strong interferes. This paper presents a blocker-resilient wideband receiver architecture for NB-IoT applications. By exploiting the impedance mapping characteristic of N-Path filter and a low noise amplifier with negative feedback, a high-order filtering characteristics of baseband is mapped to RF input so as to implement wideband impedance matching and blocker suppression. To further improve the out-of-band linearity, a dual mixer structure is employed to cancel the out-of-band blockers before the TIA. Measurements show the RX out-of-band IIP3 is +17.6 dBm, while in-band IIP3 is -13 dBm.

key words: receiver; Internet of things; blocker-resilient; blocker-cancelling; low power

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Narrowband Internet of Things (NB-IoT) plays an important role in a fifth generation (5G) system, and it will support 5G Low power Wide Area (LPWA) use cases in the foreseeable future [1, 2, 3, 4, 5]. According to the NB-IoT protocol, NB-IoT system supports multiple bands from 729 MHz to 960 MHz in Low Band (LB) applications and the receiver needs to sense weak wanted signal among strong interferes which are from other sub-GHz protocols, such as GSM [6], IEEE 802.11ah [7]. Therefore, what is needed in NB-IoT system is a blocker-resilient receiver covering a wide range of frequencies, while the consuming power is low.

Conventionally, in order to cover large number of frequency bands and reject nearby interferes, multiple narrowband frontends and external RF filters are employed. This solution filters interferers, but it comes at the expense of area and cost both in on-chip and off-chip. For low power and low cost IoT applications, wideband receivers without external RF filter are required. Recently different techniques have been employed in the literatures to improve out-of-band linearity performance. Due to the high linearity of passive mixer, mixer-first receiver has garnered much attention [8, 9, 10, 11, 12, 13]. However, the excellent linearity comes at the cost of noise figure because of the lack of low noise amplifier (LNA). To reduce the noise figure of blocker-tolerant receiver, noise cancelling techniques from noise-cancelling LNA [14, 15, 16] have been improved in [17, 18, 19] to cancel the matching resistor noise by employing multiple down-conversion paths which increases the hardware complexity and power consumption.

In this paper, we propose a low-power blocker-resilient receiver for NB-IoT applications. A LNA with negative feedback and N-path filters are introduced to form a high-Q impedance matching at RF input. To further reject blockers, we introduce a blocker-cancelling technique which employs two separated down-conversion mixer structure.

2. Circuit design

2.1 Receiver Topology

The proposed wideband blocker-resilient dual-mixer receiver designed for NB-IoT applications is shown in Fig. 1. The main path begins with a LNA, which provides better noise performance, compared to mixer-first receiver. This single-ended LNA is followed by a four-phase non-overlapping clock pulses. The ON resistance of the passive mixer switch in main path is designed at about 10 Ω to avoid a large voltage gain at blocker frequencies. After down-converted to baseband by mixer,
the current signal is converted to a voltage through a transimpedance amplifier (TIA). Furthermore, for a better blocker-resilient performance, this TIA contains a second-order filter, and the analog baseband employs a third-order Butterworth filter.

### 2.2 LNA

According to N-path filtering theory, the frequency response of the band-pass filter is centered at the LO frequency [20, 21, 22, 23]. As a result, the proposed receiver is equivalent to a wideband and center frequency configurable receiver with selective band-pass characteristic. The input impedance of mixer-first receiver is calculated as follows [10]:

$$Z_{in}(\omega) = R_{sh} + \frac{2}{\pi^2} \cdot Z_{sh}(\omega - \omega_{lo}) \| R_{sh}$$  \hspace{1cm} (1)

where $Z_{BB}$ is the impedance of baseband circuits, and $R_{sh}$ is equivalent resistance of harmonic mixing.

The main part of LNA (shown in Fig. 2) used in this receiver has an active feedback between the RF port and mixer’s input [24]. It makes the baseband impedance further mapped to the RF port, without sacrificing noise performance. In addition, an auxiliary compensation path is added to enhance the linearity of amplifier [25]. The IIP3 of LNA is improved about 6 dB with only 0.13 mA current added and 0.2 dB NF degraded. The input impedance of receiver is given below:

$$Z_{in} = \frac{1}{g_{m1} + g_{m2} \cdot R_{L,\text{LNA}}} + R_{L,\text{LNA}} \| Z_{new}(\omega)$$  \hspace{1cm} (2)

where $g_{m1}$ and $g_{m2}$ are the transconductance of transistor M1 and transistor M2 in Fig. 2, respectively. $R_{L,\text{LNA}}$ is the output resistance of LNA and $R_{L,\text{LNA}}$ is the feedback resistance in the negative feedback loop.

According to (2), we could set the input impedance value in order to match with the source impedance by designing proper transconductance of transistors and base band impedance.

### 2.3 TIA with second-order filtering

To realize a higher order RF bandpass filtering, a second-order low-pass filtering TIA with high in-band impedance is employed [26]. A negative feedback is used to implement the second-order characteristics of both input impedance and transfer function. As shown in Fig. 3, the output voltage at TIA’s output goes through a high-pass path, and then the out-of-band blocker voltage is converted to current at the input of TIA by a Gm unit. The negative feedback current is combined with input blocker current out of phase. Therefore, the blockers are suppressed at the input of TIA, enhancing the linearity of TIA. The transfer function is calculated below with $R_1=9.8\,\text{k}\Omega$, $R_2=10\,\text{k}\Omega$, $C_1=3\,\text{pF}$, $C_2=6\,\text{pF}$:

$$I_{in} \cdot V_{out} \cdot sC_2 \left( R_2 + 1/sC_2 \right) sC_1 = V_{out} / R_1 \quad \hspace{1cm} (3)$$

$$V_{out} / I_{in} = R_1 / (s^2 / \omega_0^2 + s / \omega_0 + 1) \quad \hspace{1cm} (4)$$

where $\omega_0 = \sqrt{1/C_2 R_2}$, $Q = \sqrt{R_2 C_2 / (R_1 C_2)}$.

The input impedance of TIA is calculated as follows:

$$Z_{in} = 1 / \left( s^2 C_2 C_1 R_2 + (1 + A_0) \cdot s C_1 \right) \quad \hspace{1cm} (5)$$

where $A_0$ is the open-loop gain of OTA. It is clear that the transfer function and input impedance of this architecture has second-order filtering characteristic, as described in (3) and (4).

The advantage of this TIA is that the transfer function of this negative feedback loop is high-pass. Therefore, the noise of resistor and Gm unit is significantly attenuated by this high-pass feedback loop.

Substituting (5) into (2), it is obvious that the second-order filtering characteristics of the baseband are mapped to the RF port.

### 2.4 Analog filter

Fig. 4 shows the employed analog filter structure, which is a 3rd-order Butterworth low-pass filter. It contains two
stages filters and a variable gain amplifier. For a better linearity, a first-order filter is followed by Two-Thomas biquad filter. Resistors and capacitors in this circuit is designed to programmable resistor and capacitor arrays to adjust gain and compensate for process variations. It could provide 0~72 dB variable gain.

3. Frequency translational impedance mapping and blocker cancelling technique

Fig. 5 shows the impedance characteristics at different positions in the receiver. At the RF port, a blocker is standing with a wanted signal. The wanted signal is well matched with RF port, but the blocker is mismatched in order to reflecting its power. After LNA, the wanted signal and blocker are converted to currents. Because of second-order band-pass characteristic here, the wanted signal current is amplified, but blocker current is sharply suppressed, which enhance the linearity of the receiver.

To further improve the linearity, an auxiliary path in Fig. 1 is added by using a mixer-first structure, which contains only mixers and RC filter. The currents of the two paths come into the shared TIA.

Dual mixer structure separates wanted signal and blocker signal at baseband by using resistors, $R_A=10 \text{kΩ}$, and capacitors, $C_A=6 \text{pF}$, of auxiliary path, as shown in Fig. 5. Because of the existence of $C_A$, for wanted signal which has small baseband offsets, it’s a high impedance path, and wanted signal will go through the resistance path. On the contrary, the blocker current will pass through the capacitance path because it’s a low impedance path for large baseband offsets. Meanwhile, the main path has both wanted signal and blocker at the input of TIA. Therefore, feeding blocker current IBK+ and IBK- from auxiliary path back to the IBK- and IBK+ coming from main path at the input of TIA respectively, makes the blocker currents combined out of phase and significantly cancelled. In order to cancel the blocker current perfectly, the current gain of main path and auxiliary path should be equal at the baseband. The current gain and transconductance of LNA for perfect blocker cancellation are given as follows:

$$g_{m,LNA} \left( R_{SW,AUX} + \frac{2}{\pi} Z_{BB}(\Delta \omega) \right) = \frac{R_A}{R_A + Z_{BB}(\Delta \omega)}$$  \hspace{1cm} (6)

$$g_{m,LNA} \approx \frac{R_A C_A(\Delta \omega)}{R_{SW,AUX} \left[ R_A C_A(\Delta \omega) \right]^2 + 1} \approx \frac{1}{R_{SW,AUX}}$$  \hspace{1cm} (7)

To achieve a complete linearity compensation not only requires carefully design, but also requires symmetry of layout.

4. Noise analysis

The frontend of the proposed dual-mixer structure receiver also has noise cancelling characteristic. The noise from the added auxiliary path could be cancelled by properly connection. As shown in Fig. 6, the load resistor $R_{L,AUX}$ connects to the in-phase input of TIA. The noise from auxiliary path $I_{AUX}$ consist of load resistor noise $I_{R,AUX}^2$ and noise of mixer in auxiliary path $I_{SW,AUX}^2$. This noise current is converted to a noise voltage $V_{aux}^2$ at the receiver input, which includes all the local oscillator harmonics. And all these noises are down-converted to the input of TIA through the main path. Because of the inversing characteristic of LNA, the resulted noise is $-g_{m,LNA} I_{AUX}^2 R_A$. The baseband noise current $I_{AUX,BB}$ in auxiliary path only contains the noise of passive mixer’s switch resistance in the auxiliary path which is down-converted to baseband and the noise of $R_{L,AUX}$ at low frequency. With proper connection, the baseband noise current of the main path and auxiliary paths can be added in reverse, and the noise introduced by the load resistor branch N-Path can be cancelled. Meanwhile, the signals going through the two paths are added in-phase, so the energy of signal is not attenuated.

5. Measurement results

The die micrograph of proposed receiver is shown in Fig. 7.
The test chip has been fabricated in 55 nm CMOS technology. Fig. 7 shows the die micrograph of the receiver. The core area of the chip is 0.85 mm x 1 mm.

Fig. 8(a) shows the measured DSB noise figure (NF) at baseband frequency of the proposed receiver. The minimum NF is 4.2 dB at 0.4 MHz with the LO frequency of 900 MHz. To evaluate the noise performance in the presence of blocker, a sinewave blocker at 80 MHz offset is applied with different level. Fig. 8(b) plots the receiver NF with blocker. According to the requirement of NB-IoT protocol, the NF should be less than 5 dB. For this proposed receiver, the NF degrades to 5 dB in the presence of a -11 dBm blocker.

![Image](51x410 to 56x439)

![Image](53x560 to 58x579)

![Image](58x402 to 65x406)

![Image](60x568 to 65x572)

![Image](60x585 to 65x589)

![Image](60x603 to 65x607)

![Image](60x450 to 65x454)

![Image](60x550 to 65x554)

![Image](60x434 to 65x438)

![Image](62x533 to 65x537)

![Image](63x418 to 65x422)

![Image](64x380 to 71x386)

![Image](64x386 to 185x390)

![Image](64x406 to 185x410)

![Image](64x416 to 185x420)

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![Image](64x1097 to 185x1101)

![Image](64x1107 to 185x1111)

![Image](64x1117 to 185x1121)

![Image](64x1127 to 185x1131)

![Image](64x1137 to 185x1141)

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![Image](64x1157 to 185x1161)

![Image](64x1167 to 185x1171)

![Image](64x1177 to 185x1181)

![Image](64x1187 to 185x1191)

![Image](64x1197 to 185x1201)

![Image](64x1207 to 185x1209)

![Image](64x1211)
N-path filter to implement frequency translational impedance mapping. By employing two separated down-conversion mixer path to cancel blocker before TIA, the out-of-band linearity of receiver is further improved. The receiver achieves 4.2 dB noise figure with 96 dB gain from 0.6 to 1 GHz, and +17.6 dBm out-of-band IIP3, while consuming only 20.4 mW.

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