Noise-Adaptive Quantum Compilation Strategies Evaluated with Application-Motivated Benchmarks

Davide Ferrari\textsuperscript{1,2} and Michele Amoretti\textsuperscript{1,2}

\textsuperscript{1}Department of Engineering and Architecture - University of Parma, Italy
\textsuperscript{2}Quantum Information Science @ University of Parma, Italy

Abstract

Quantum compilation is the problem of translating an input quantum circuit into the most efficient equivalent of itself, taking into account the characteristics of the device that will execute the computation. Compilation strategies are composed of sequential passes that perform placement, routing and optimization tasks. Noise-adaptive compilers do take the noise statistics of the device into account, for some or all passes. The noise statistics can be obtained from calibration data, and updated after each device calibration.

In this paper, we propose a novel noise-adaptive compilation strategy that is computationally efficient. The proposed strategy assumes that the quantum device coupling map uses a heavy-hexagon lattice. Moreover, we present the application-motivated benchmarking of the proposed noise-adaptive compilation strategy, compared with some of the most advanced state-of-art approaches. The presented results seem to indicate that our compilation strategy is particularly effective for deep circuits and for square circuits.

\textbf{keywords} - Noise-adaptive quantum compilation; Quantum programming tools; Quantum benchmarking

1 Introduction

Current quantum computers are noisy, characterized by a reduced number of qubits (5-50) with non-uniform quality and highly constrained connectivity. These systems and near-term ones (with 1000 qubits or less), which are denoted as Noisy Intermediate-Scale Quantum (NISQ), may be able to surpass the capabilities of today’s most powerful classical digital computers, for some problems. However, noise in quantum gates limits the size of quantum circuits that can be executed reliably. To reliably process information, the physical qubits should maintain the quantum state for sufficiently long. The qubits should also support sufficiently precise operations to allow for correct state manipulation during the coherence window. Last but not least, the qubits should support accurate measurement operations.

Quantum compilation is the problem of translating an input quantum circuit into the most efficient equivalent of itself [1], taking into account the characteristics of the device that will execute the computation. In general, the quantum compilation problem is NP-Hard [2, 3].

Compilation strategies are composed of sequential \textit{passes} that perform placement, routing and optimization tasks. Placement is performed once, at the very beginning of the compiling process. It is the task of defining a mapping between the virtual qubits of the input quantum circuit and the physical qubits of the device. Routing is the task of modifying the circuit in order to move through subsequent mappings, by means of a clever swapping strategy, in order to conform to the
qubit layout of the device. Optimization is the task of minimizing some property of the circuit in order to reduce the impact of noise. Several routing and optimization passes may be executed within a compilation strategy.

Noise-adaptive compilers do take the noise statistics of the device into account [4, 5, 6, 7], for some or all passes. The noise statics can be obtained from calibration data, and updated after each device calibration. For example, Qiskit\(^1\) allows for programmatic retrieval of IBM Q devices’ calibration data.

In the literature, compiled circuits are frequently evaluated in terms of depth and gate count overhead with respect to the input circuits. Calculating these figures of merit does not require to execute the compiled circuit. Another common method is to run the compiled circuit many times with a figure of merit being the success rate, i.e., the fraction of runs that resulted in a correct (classical) answer. The Hellinger fidelity [8] is a measure of the distance between two random distribution. It is frequently used to compare the sampled distribution of the results of a quantum computation to the theoretical distribution (provided that the latter one is known).

Recently, Mills et al. [9] have presented a framework for application-motivated benchmarking of full quantum computing stacks. The benchmarks defined there have a circuit class, describing the type of circuit to be run on the system, and a figure of merit, quantifying how well the system did when running circuits from that class. The idea is that a circuit class should represent a particular application domain. The application-motivated circuit classes proposed by Mills et al. draw inspiration from quantum algorithmic primitives [10] and from the literature on near-term quantum computing applications (e.g., machine learning and chemistry).

1.1 Our Contributions

The first contribution of this paper is a novel noise-adaptive compilation strategy that is computationally efficient. The proposed strategy assumes that the coupling map, i.e., the device-specific directed graph whose vertices correspond to the physical qubits and edges correspond to permitted CNOT gates, uses a heavy-hexagon lattice. In Section 3, we describe the proposed strategy and we thoroughly analyze its theoretical performance.

The second contribution is the application-motivated benchmarking of the proposed noise-adaptive compilation strategy, compared with some of the most advanced state-of-art approaches. In Section 4, we summarize the features of three notable circuit classes (deep, square and shallow) and we recall the definitions of five significant figures of merit. Then, in Section 5, we show and discuss the evaluation results.

2 Related Work

Despite the quantum compilation problem has been studied for years, there are still few noise-adaptive compiling strategies.

Qiskit’s \texttt{NoiseAdaptiveLayout} placement pass associates a physical qubit to each virtual qubit of the circuit using calibration data, based on the heuristic method proposed by Murali et al. [4]. The pass maps virtual qubit pairs in order of decreasing frequency of the CNOT occurrences between them. If a pair exists with both qubits unmapped, the pass picks the best available physical qubit pair, based on CNOT reliability, to map it. If a pair has only one qubit unmapped, the pass maps that qubit to a location that ensures maximum reliability for CNOTs with previously mapped

\(^1\)https://qiskit.org/
qubits. In the end if there are unmapped qubits, the pass maps them to any available physical qubit.

Nishio et al. [6] proposed a placement pass and a routing pass. The placement pass, which is denoted as Greatest Connecting Edge Mapping, leverages a strategy that is very similar to the one proposed by Murali et al. [4]. The routing pass is a beam search algorithm with an heuristic cost function based on the estimated success probability of candidate SWAP gates.

t|ket⟩’s NoiseAwarePlacement [7] searches for candidate partial placements of virtual qubits to the physical ones. This is done by casting the problem as finding a subgraph monomorphism between the coupling map and a graph representing virtual qubit CNOT interactions in the circuit. Where different possible candidates placement are found, using a heuristic approach, the pass chooses the one with the maximum expected overall fidelity.

Recently, Niu et al. [5] have implemented a hardware-aware routing pass (HA), inspired by the work of Li et al. [11], that iteratively selects the best scoring SWAP with respect to calibration data as well as qubits distance. The influence of each of these factors on the cost function can be set by means of tunable weights.

3 Proposed Compilation Strategy

We introduce an heuristic-based compilation strategy consisting of two compilation passes that account for calibration data such as gate reliability and readout errors. The first one is a placement pass, i.e., a pass that finds an initial mapping of virtual qubits to physical ones. The second pass is a routing strategy to make all two-qubits gates compliant with hardware connectivity. Both passes exploit device calibration data with the aim of improving the quality of the states produced by the compiled circuit. In the following we assume a heavy-hexagon lattice for the coupling map of the device, such as the one used by IBM superconducting devices [12]. In heavy-hexagon lattices, the qubits are located on the nodes and edges of each hexagon. Each qubit has either two or three neighbors, meaning the graph has vertices of degree 2 or 3. As a consequence, only three different frequency assignments are necessary for the superconducting qubits, as opposed to a square lattice, which naturally requires at least five different frequencies for addressability. The heavy-hexagon lattice also greatly reduces crosstalk errors since, in principle, only qubits on the edges of the lattice need to be driven by cross-resonance (CR) drive tones [13].

3.1 Placement

In the proposed placement pass, a sequence of qubits connected in a line is detected. On a coupling map with heavy-hexagon connectivity, it not possible to find a line connecting all qubits. However, it is possible to find lines that traverse a good portion of the graph, with leftover qubits that could later be used for swapping across segments of the line. Fig. 1 shows the coupling map of the 65 qubits ibmq_manhattan device, with the sequence of qubits used for the initial mapping highlighted in light-blue.

To find a line of qubits, one can leverage the features of the graph, such as its regular structure and the fact that every qubit is identified by a number in \{0, ..., n − 1\}, where n is the number of qubits in the device. This is done starting from node 0 and traversing the graph while keeping track of already visited nodes, backtracking if a dead end is reached before having explored the entire graph.

If the found sequence contains more qubits than needed by the circuit, the pass selects a best subset based on two-qubit gates reliability using a sliding window technique. On the other hand, if there are not enough qubits in the sequence, the pass proceeds to insert qubits from the leftover
ones, depicted in dark gray in Fig. 1, until the necessary number of qubits is reached. These qubits are first scored based on calibration data, and then inserted into the chain after one of their neighboring qubits, starting form the one with the highest score.

3.2 Noise Adaptive Swap

Given an initial mapping of virtual qubits to physical ones, the \texttt{NoiseAdaptiveSwap} pass proceeds to compute a front layer of non hardware-compliant CNOT gates.

\textbf{Definition 3.1.} Let $C_k$ be a quantum circuit on $k$ qubits and $U_i(Q_i)$ a quantum gate acting on a set of qubits $Q_i$ with $0 < |Q_i| \leq k$. A layer $\mathcal{L}$ is a set of consecutive gates that can be applied concurrently such that:

1. $Q_i \cap Q_j = \emptyset$ for all $U_i, U_j \in \mathcal{L}$, with $i \neq j$

2. $\sum_{U_i \in \mathcal{L}} |Q_i| \leq k$

\textbf{Definition 3.2.} The front layer is a layer $\mathcal{F}$ such that $|Q_i| = 2$ for all $U_i \in \mathcal{F}$.

For convenience, we reformulate circuits by means of the Directed Acyclic Graph (DAG) circuit formalism, as it enables to effectively represent gates dependencies in quantum circuits.

\textbf{Definition 3.3.} A DAG circuit is a directed acyclic graph where vertices represent gates and directed edges represent qubit dependencies. A directed edge $e_q(i, j)$ between vertices $i$ and $j$ represents a dependency between gate $i$ and gate $j$ with respect to qubit $q$, i.e., gate $i$ must be executed before $j$ and both gates act on qubit $q$.

\textbf{Definition 3.4.} Given a directed graph $G = (V, E)$, a topological order of $G$ is a linear ordering over vertices in $V$ such that, for all directed edges $(v, w) \in E$, $v$ precedes $w$ in the ordering.

\textbf{Definition 3.5.} Let $v_0v_1...v_n$ be a topological ordering on graph $G = (V, E)$. Then $v_j$ is a direct topological successor of $v_i$ iff $j > i$ and $\exists e \in E$ such that $e = (v_i, v_j)$. 

Figure 1: Initial mapping on the 65 qubits of the \texttt{ibmq\_manhattan} device, highlighted in light-blue.
To compute the front layer of non hardware-compliant CNOT gates, the pass iterates over all gates in the circuit, in topological order. Gates that do not need routing, such as one-qubit gates or hardware-compliant CNOT gates are added to the set of executed gates $\mathcal{X}$. CNOT gates that need to be properly mapped and do not interact with qubits already interested by a CNOT gate in the front layer, are added to the latter. Every gate that is a successor of a CNOT gate in the front layer, is added to the set of not executed gates $\bar{\mathcal{X}}$.

From the front layer, the pass computes a list of possible SWAP operations involving at least one qubit interested by a CNOT in the front layer. These SWAP operations are scored with an heuristic cost function $h(s)$, where $s$ denotes the considered SWAP gate. The cost function is computed over all gates in the front layer $\mathcal{F}$ plus a set of upcoming gates $\mathcal{U} \subset \bar{\mathcal{X}}$, as shown in Eq. 1, where $\pi_s(g_c)$ and $\pi_s(g_t)$ are the physical qubits corresponding to the control and target of gate $g$ with mapping $\pi_s$.

$$h(s) = \frac{\alpha}{|\mathcal{F} \cup \mathcal{U}|} \sum_{g \in \mathcal{F} \cup \mathcal{U}} R(\pi_s(g_c), \pi_s(g_t)) + \frac{1 - \alpha}{|\mathcal{F} \cup \mathcal{U}|} \sum_{g \in \mathcal{F} \cup \mathcal{U}} 1 - D(\pi_s(g_c), \pi_s(g_t))$$ (1)

Here, $R$ and $D$ are respectively the swap paths reliability matrix and the distance matrix for every qubits pair in the coupling map. Matrix $R$ stores in entry $(i, j)$ the reliability of the most reliable swap path between qubits $i$ and $j$, where the reliability of a single SWAP along an edge of the coupling map is computed with regard to CNOT gate and readout error rates. Matrix $D$ is the distance matrix and stores at entry $(i, j)$ the shortest distance between qubits $i$ and $j$. The swap path reliability and the distance between qubits are important components that one would like to maximize and minimize, respectively. The coefficient $\alpha$ gives the opportunity to set equal or opposite weights for them, in the context of the heuristic cost function $h(s)$.

Definition 3.6. The reliability of SWAP gate $s$ between qubits $i$ and $j$ is $r(s) = \mu(i, j)^3$, where $\mu(i, j)$ is the success rate of a CNOT($i, j$) between qubits $i$ and $j$, obtained from calibration data.

In the previous definition, it is assumed that the SWAP gate is composed of 3 CNOT gates.

Definition 3.7. Let $S = s_0s_1...s_k$ be a sequence of SWAP gates (SWAP path) and denote the reliability of SWAP gate $s$ as $r(s)$. Then the reliability of $S$ is given by $\prod_{i=0}^{k} r(s_i)$.

Definition 3.8. Given a quantum device with $n$ qubits, the SWAP paths reliability matrix $R \in \mathbb{R}^{n \times n}$, is the real matrix that stores in entry $(i, j)$ the maximum reliability or, equivalently, success rate at which qubit $i$ can be moved to a neighbor of qubit $j$ through a sequence of SWAP gates.

Definition 3.9. Given a quantum device with $n$ qubits, the distance matrix $D \in \mathbb{N}^{n \times n}$, is the matrix that stores in entry $(i, j)$ the minimum distance between qubit $i$ and a neighbor of qubit $j$.

Both matrices can be efficiently precomputed using the Floyd–Warshall algorithm [14]. Matrix $R$ is computed with edge weights corresponding to SWAP reliability, while matrix $D$ has edge weights equal to 1. The SWAP reliability can be easily derived from CNOT calibration data, as each SWAP is usually achieved with three consecutive CNOTs. As matrix $D$ contains entries with incompatible scales with respect to $R$, both matrices in Eq. 1 are normalized.

The first part of Eq. 1 sums over the swap reliability of all gates involved in $\mathcal{F} \cup \mathcal{U}$ and divides by $|\mathcal{F} \cup \mathcal{U}|$ to obtain a mean value. The second part follows a similar approach with the distance matrix, except that the sum must be over $1 - D$, as the goal is to maximize the reliability while minimizing the normalized distance.
3.3 Computational Complexity

**Theorem 3.1.** The execution of the Placement pass takes $O(n)$ time, where $n$ is the number of qubits in the device.

**Proof.** In order to find the initial placement of qubits, the Placement pass needs to iterate over all nodes in the coupling map, taking $O(n)$ time, where $n$ is the number of qubits in the device. □

As previously stated, the $R$ and $D$ matrices are precomputed using the Floyd–Warshall algorithm, whose time complexity is $O(n^3)$.

**Theorem 3.2.** Assuming a coupling map with heavy-hexagon connectivity, computing the $h(s)$ score of a candidate SWAP gate $s$ takes $O(n^2)$ time, where $n$ is the number of qubits in the device.

**Proof.** Computing the score of a candidate SWAP gate requires retrieving SWAP paths reliability and distance information for all non-compliant CNOT gates in the front layer, and a few additional ones from subsequent layers (by default 5, which can be treated as a constant factor and therefore ignored). There can be at most $n/2$ CNOT gates in one layer, where $n$ is the number of qubits. Thus, computing the $h(s)$ score takes $O(n)$ time. Assuming a coupling map with heavy-hexagon connectivity, the number of possible different SWAP gates candidates in a layer is $O(n)$. Consequently, to obtain the most promising SWAP gates for the current layer the score function must be computed $O(n)$ times, taking a total of $O(n^2)$ time. □

A beam search algorithm is used to look up for a new possible mapping through a sequence of SWAP gates, with respect to either the initial mapping or the one from a previous iteration of the routing pass. The beam search algorithm is characterized by beam width $w$ and search depth $k$, which gives an $O(w^k n^2)$ time complexity, taking into account the statement from Theorem 3.2.

**Theorem 3.3.** Assuming a coupling map with heavy-hexagon connectivity, the NoiseAdaptiveSwap pass takes $O(\frac{w^k}{k} gn^{2.5})$ time, where $g$ is the number of CNOT gates in the circuit.

**Proof.** Beam search with beam width $w$ and search depth $k$ takes $O(w^k n^2)$ time. Given a coupling map with heavy-hexagon connectivity, the distance between any qubit pair can be reasonably approximated to $O(\sqrt{n})$. In the worst case scenario, one would need to search $O(\sqrt{n})$ mappings for every CNOT gate in the circuit. This can be relaxed to $O(\sqrt{n}/k)$, as each new mapping search will insert $k$ SWAP gates on average. It follows that the whole compilation process should then take $O(g \frac{\sqrt{n}}{k} w^k n^2) = O(\frac{w^k}{k} gn^{2.5})$, where $g$ is the number of CNOT gates in the circuit. □

The $w^k$ factor is due the fact that the pass does not just pick the best scoring SWAP at each iteration, but instead searches over the $k$ best SWAPs, as the best scoring one may not necessarily lead to the best final solution. We could further assume that $w = k$, giving a time complexity of $O(k^{k-1} gn^{2.5})$.

3.4 Implementation

A Python implementation of the proposed noise-adaptive compiler is available on GitHub. It has been designed as a Qiskit pass [12], thus it can be used with any quantum device supported by Qiskit.

https://github.com/qis-unipr/noise-adaptive-compiler
4 Application-Motivated Benchmarks

With reference to the recent paper by Mills et al. [9], we consider three circuit classes, namely deep, square and shallow.

Deep circuits are constructed from several layers of Pauli gadgets [15], which are quantum circuits that implement an operation corresponding to exponentiating a tensor product of Pauli matrices. For example, in quantum chemistry, deep circuits are used to build UCC trial states used in the variational quantum eigensolver (VQE) [16].

Square circuits are random circuits built from two-qubit gates. They provide a benchmark at all layers of the quantum computing stack. Indeed, they have been suggested as a means to demonstrate quantum computational supremacy [17]. Square circuits avoid favoring any device in particular, because they allow two-qubit gates to act between any pair of qubits in the uncompiled circuit.

The class of shallow circuits is a subclass of Instantaneous Quantum Polytime (IQP) circuits [18]. IQP circuits consist of gates diagonal in the Pauli-Z basis, sandwiched between two layers of Hadamard gates acting on all qubits. Shallow circuits are characterized by limited connectivity between the qubits and by a depth that increases slowly with width. Thus, shallow circuits are useful for understanding the performance of a device being utilized for applications whose circuit depth grows less quickly than their qubit requirement.

In Section 5, the compiled circuits are evaluated in terms of a few figures of merit that are described below. Let us denote an $n$ qubit circuit as $C$, the ideal output distribution of $C$ as $p_C$ and the output distribution produced by the compiled implementation of $C$ as $D_C$.

- **Hellinger fidelity** - The Hellinger fidelity between $D_C$ and $p_C$ is

  \[ F_C = \left( \sum_{x \in \{0,1\}^n} \sqrt{D_C(x)p_C(x)} \right)^2. \]  

  We would like that $F_C = 1$.

- **Heavy Output Generation (HOG)** - An output $z \in \{0,1\}^n$ is heavy for a quantum circuit $C$, if $p_C(z)$ is greater than the median of the set $\{p_C(x) : x \in \{0,1\}^n\}$. The HOG probability of $D_C$, i.e., the probability that samples drawn from from $D_C$ will be heavy outputs in $p_C$, is

  \[ \text{HOG}(D_C, p_C) = \sum_{x \in \{0,1\}^n} D_C(x)\delta_C(x) \]  

  where $\delta_C(x) = 1$ if $x$ is heavy for $C$, and $\delta_C(x) = 0$ otherwise. We would like HOG($D_C, p_C$) > 1/2, as it would help us distinguish between a good implementation of $C$ and an attempt to mimic it by generating random bitstrings. Of course this is true if $p_C$ is sufficiently far from uniform.

- **$l_1$-norm distance** - The $l_1$-norm distance between $D_C$ and $p_C$ is

  \[ l_1(D_C, p_C) = \sum_{x \in \{0,1\}^n} |D_C(x) - p_C(x)|. \]  

  We would like that $l_1(D_C, p_C) = 0$.

- **CNOT Count** - In a quantum circuit, the number of CNOT gates is denoted as CNOT count.
• **CNOT Depth** - In a quantum circuit, the number of layers containing CNOT gates is denoted as CNOT depth.

In Section 5, as suggested in [9], we approximate $D_C$ using samples obtained by running the compiled implementation of $C$ several times. That is, given samples $S = \{x_i, \ldots, x_m\}$ from $D_C$, let $S_x$ be the number of times $x$ appears in $S$ and define $\tilde{D}_C(x) = S_x / m$.

## 5 Evaluation

We have evaluated the proposed noise-adaptive compilation strategy, compared with some of the most advanced state-of-art approaches, over the circuit classes presented in Section 4, with 200 circuits for each class and different number of qubits, as in [9]. For each circuit the ideal output distribution $p_C$ has been obtained using Qiskit’s statevector simulator. The same simulator has been used to sample noisy circuits from the noise model obtained with calibration data of the IBM *ibmq_casablanca* 7-qubit device.

We have tested the following compilers:

- `qiskit` is the Qiskit standard compiler with optimization level 3;
- `qiskit.noise` is the Qiskit compiler with `NoiseAdaptiveLayout` and optimization level 3;
- `pytket` is the `t|ket⟩` compiler with `NoiseAwarePlacement` and maximum optimization level;
- `na` are the proposed noise-adaptive placement and routing passes integrated with Qiskit and optimization level 3;
- `qiskit_na` is the proposed routing pass combined with Qiskit’s `NoiseAdaptiveLayout` and optimization level 3;
- `t` denotes the application of CNOT cascade transformations, as described in [19].

For each of the above we have used Qiskit v0.23.6 and `t|ket⟩` v0.7.2. We remark that the `pytket_na` compiler was not tested, as the integration of `pytket` and `na` is possible only with regards to swap passes, not for the placement ones.

The results are reported in Fig.2, Fig.3 and Fig.4. For each compiler configuration, we have used box plots to depict the distributions of the resulting values for the figures of merit described in Section 4. A box plot is constructed of two parts, a box and a set of whiskers. The box is drawn from the lower quartile to the upper quartile with a horizontal line drawn in the middle to denote the median. For the whiskers, the lowest point is the minimum of the data set and the highest point is the maximum of the data set.

The reader may observe that, for deep and square circuits, the best results in Hellinger fidelity, HOG, and $l_1$-norm are those achieved with `qiskit_na`. Interestingly, with this compiler, the CNOT depth is worst than with the other compilers. Indeed, improving the quality of a quantum computation with a noise-adaptive compilation strategy does not forcedly imply reducing the depth of the circuit. Regarding shallow circuits, `qiskit_na` and `pytket` have the same performance.

Regarding the impact of $\alpha$, one may observe that, with deep circuits, $\alpha = 0.9$ produces better Hellinger fidelity. Instead, with square and shallow circuits, $\alpha = 0.5$ seems a better choice. The difference is nevertheless minimal. This could be due to the small number of qubits in the circuits and in the considered device.
Figure 2: Comparison of compilation strategies with deep circuits using (2a) Hellinger fidelity, (2b) HOG, (2c) $l_1$-norm, (2d) CNOT count and (2e) CNOT depth as metrics. Qiskit’s statevector simulator has been used to sample noisy circuits from the noise model obtained with calibration data of the IBM ibmq_casablanca 7-qubit device.

6 Conclusions

In this work, we presented a novel noise-adaptive quantum compilation strategy that is computationally efficient. The contributed strategy assumes heavy-hexagon topologies for quantum devices,
Figure 3: Comparison of compilation strategies with square circuits using (3a) Hellinger fidelity, (3b) HOG, (3c) $l_1$-norm, (3d) CNOT count and (3e) CNOT depth as metrics. Qiskit’s statevector simulator has been used to sample noisy circuits from the noise model obtained with calibration data of the IBM *ibmq_casablanca* 7-qubit device.

which is particularly crucial for the placement pass. Moreover, the assumption simplifies the derivation of the computational complexity upper bounds. Nevertheless, the proposed routing pass is general enough to be effective independently of the coupling map of the target quantum device.

The presented results seem to indicate that our compilation strategy is particularly effective for
Figure 4: Comparison of compilation strategies with shallow circuits using (4a) Hellinger fidelity, (4b) HOG, (4c) $l_1$-norm, (4d) CNOT count and (4e) CNOT depth as metrics. Qiskit’s statevector simulator has been used to sample noisy circuits from the noise model obtained with calibration data of the IBM <em>ibmq_casablanca</em> 7-qubit device.

circuits characterized by great depth and/or randomness. On the other hand, we are aware that the performed evaluation is not exhaustive and further work is necessary to fully characterize the proposed approach, for example in designing a reasonable method for tuning the $\alpha$ parameter in
Eq. 1. In particular, we plan to extend the evaluation to circuits and devices with more qubits, and to distributed quantum computing architectures as well [20, 21, 22].

As a final remark, it is worth noting that it is possible to further mitigate the effect of noise by using an ensemble of diverse mappings (EDM) approach, as suggested by Tannu and Qureshi [23]. In the near future, we shall integrate this method into our quantum compiling library.

Acknowledgements

This research benefited from the HPC (High Performance Computing) facility of the University of Parma, Italy.

References

[1] A. D. Córcoles, A. Kandala, A. Javadi-Abhari, D. T. McClure, A. W. Cross, K. Temme, P. D. Nation, M. Steffen, and J. M. Gambetta. Challenges and Opportunities of Near-Term Quantum Computing Systems. *Proceedings of the IEEE*, 108(8):1338–1352, 2020.

[2] A. Botea, A. Kishimoto, and R. Marinescu. On the Complexity of Quantum Circuit Compilation. In *The Eleventh International Symposium on Combinatorial Search (SOCS 2018)*, 2018.

[3] M. Soeken, G. Meuli, B. Schmitt, F. Mozafari, H. Riener, and G. De Micheli. Boolean satisfiability in quantum compilation. *Phil. Trans. Royal Soc. A*, 378(2164):1–16, 2019.

[4] P. Murali, J. M. Baker, A. Javadi-Abhari, F. T. Chong, and M. Martonosi. Noise-Adaptive Compiler Mappings for Noisy Intermediate-Scale Quantum Computers. In *Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems*, ASPLOS ’19, page 1015–1029, New York, NY, USA, 2019. Association for Computing Machinery.

[5] S. Niu, A. Suau, G. Staffelbach, and A. Todri-Sanial. A Hardware-Aware Heuristic for the Qubit Mapping Problem in the NISQ Era. *IEEE Transactions on Quantum Engineering*, 1:1–14, 2020.

[6] S. Nishio, Y. Pan, T. Satoh, H. Amano, and R. Van Meter. Extracting Success from IBM’s 20-Qubit Machines Using Error-Aware Compilation. *ACM Journal on Emerging Technologies in Computing Systems*, 16(3), May 2020.

[7] S. Sivarajah, S. Dilkes, A. Cowtan, W. Simmons, A. Edgington, and R. Duncan. t|ket⟩: a retargetable compiler for NISQ devices. *Quantum Science and Technology*, 6(1):014003, nov 2020.

[8] David Pollard. *A User’s Guide to Measure Theoretic Probability*. Cambridge Series in Statistical and Probabilistic Mathematics. Cambridge University Press, 2001.

[9] D. Mills, S. Sivarajah, T.L. Scholten, and R. Duncan. Application-Motivated, Holistic Benchmarking of a Full Quantum Computing Stack. *Quantum*, 5(415), 2021.

[10] R. Blume-Kohout and T.C. Young. A volumetric framework for quantum computer benchmarks. *Quantum*, 4(362), 2020.
As stated in Section 4, the compilation strategies have been evaluated on the circuits proposed by Mills et al. [9]. The circuits are divided into three classes. Figure 5 shows the distributions of the number of gates in the considered circuits, for each class and number of involved qubits.

https://doi.org/10.5281/zenodo.3832121
Figure 5: Distributions of the number of gates for each class of circuit, depending on the number of involved qubits. By construction, all the square circuits have the same number of gates, which increases with the number of involved qubits.