Upgrade of the ALICE Inner Tracking System

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ABSTRACT: ALICE (A Large Ion Collider Experiment) is studying heavy-ion collisions at the CERN LHC, with the aim of forming, under extreme conditions of temperature and energy density, a Quark-Gluon Plasma (QGP) and studying its properties. The ALICE Collaboration is preparing a major upgrade of the experimental apparatus, planned for installation in the second long LHC shutdown in the years 2018–2019. A key element of the ALICE upgrade is the construction of a new, ultra-light, high-resolution Inner Tracking System (ITS). The primary focus of the new ITS is on improving the performance for detection of heavy-flavour hadrons, and of thermal photons and low-mass di-electrons emitted by the QGP. With respect to the current detector, the new ITS will significantly enhance the determination of the distance of closest approach of a track to the primary vertex, the tracking efficiency at low transverse momenta, and the read-out rate capabilities. This will be achieved by seven concentric detector layers based on a 50 μm thick CMOS pixel sensor with a pixel pitch of about 30 × 30 μm². A key feature of the new ITS, which is optimized for high tracking accuracy at low transverse momenta, is the very low mass of the three innermost layers, which feature a material thickness of 0.3% X₀ per layer. This contribution describes the design goals and layout of the new ALICE ITS, a summary of the R&D activities, with focus on the technical implementation of the main detector components, and the projected detector performance.

KEYWORDS: Particle tracking detectors; Particle tracking detectors (Solid-state detectors)
1 Introduction

ALICE (A Large Ion Collider Experiment) is one of the four LHC experiments, focused on the study of strongly interacting matter, using proton-proton, proton-nucleus and nucleus-nucleus collisions [1]. The ALICE collaboration is preparing a major upgrade of the experimental apparatus in the second long shutdown of the LHC in the years 2018–2019 [2]. The main physics objective of the upgrade are high-precision measurements of rare probes down to low transverse momenta. Due to the high combinatorial background these probes cannot be selected with a hardware trigger. The upgraded experimental apparatus is therefore designed to read out all Pb-Pb interactions up to the maximum collision rate (50 kHz) delivered by the LHC after LS2. The goal is to collect an integrated luminosity of more than 10 nb$^{-1}$, corresponding to an increase in terms of statistics by a factor of up to 100 with respect to the programme until LS2. In order to achieve the physics goals, the upgraded experimental apparatus will have to cope with the higher readout rate and provide an excellent tracking and vertexing, in particular for low-$p_T$ particles. One of the crucial parts of the upgrade programme, which involves most of the subdetectors as well as online and offline systems, is therefore the upgrade of the Inner Tracking System (ITS) [3]. The current ALICE ITS consists of two layers of silicon pixel detectors, two layers of silicon drift detectors and two layers of double-sided silicon strip detectors. In the upgrade the entire tracking system will be replaced by a pixel-only tracker, described in the following.

2 The upgraded ALICE ITS

The main goals of the upgrade of the Inner Tracking System are an improved reconstruction of primary and secondary vertices and an improved performance in the tracking of low-momentum particles. At a transverse momentum of 500 MeV/c an improvement in the impact parameter resolution by a factor of 3 (5) in the $r\phi$ ($z$-) direction is required. The three main measures to achieve
this are: a reduction of the radius of the innermost layer from 39 mm to 22 mm; a reduction of the material budget down to 0.3% $X_0$ in the innermost and $\sim 0.9% X_0$ in the outer and middle layers, compared to 1.14% $X_0$ per layer in the current ALICE Silicon Pixel Detector [1]; a pixel size in the order of 30 $\mu$m × 30 $\mu$m, compared to 50 $\mu$m × 425 $\mu$m in the current pixel detector. In combination with a slightly increased number of seven instead of the present six silicon tracking layers, this also leads to an improvement in the tracking efficiency and momentum resolution.

Figure 1 shows the layout of the upgraded ALICE ITS. It will be an all-pixel tracker with seven concentric barrel layers with radii between 22 mm for the innermost and 400 mm for the outermost layer. In the following the three inner layers will be referred to as Inner Barrel (IB), middle and outer layers together as Outer Barrel (OB), with the only difference between middle and outer layers being their lengths and radii. The tracker will cover the pseudo-rapidity range of $|\eta| < 1.22$ for the 90% most luminous region; the radial positions of the different layers have been optimised in order to achieve the best combined performance in terms of pointing resolution, tracking efficiency and transverse momentum resolution. The active surface of the tracker will be approximately 10 m$^2$ with a total of 12.5 billion pixels. It is designed such as to allow easy removal and insertion during the yearly shutdown. In order to evaluate the physics performance of the upgraded ITS extensive Monte-Carlo simulations have been performed. As shown in figure 2, the pointing resolution is expected to improve by the required factor of 3 (5) in the $r\phi$ ($z$-) direction. Furthermore, the tracking efficiency at low momenta will significantly improve.

### 3 The pixel chip

The central part of the upgraded ALICE ITS is the pixel chip. Table 1 summarises the requirements for the chip that arise from the physics programme and the operation environment. The most challenging requirements for the tracker are the high spatial resolution and the extremely low material budget, in particular for the inner layers. These requirements, together with the modest radiation environment compared to the other LHC trackers, led to the choice of Monolithic Active Pixel Sensors (MAPS). In the past decade there has been significant progress in the field of MAPS, such that they can now be considered a viable option for the construction of tracking system in high energy physics experiments. The ULTIMATE chip of the STAR PXL detector at RHIC is a
Table 1. General requirements on the pixel chip [3].

| Parameter                        | Inner barrel | Outer barrel |
|----------------------------------|--------------|--------------|
| Chip dimensions                  | 15 mm × 30 mm ($r\phi \times z$) |              |
| Sensor thickness                 | 50 µm        |              |
| Spatial resolution               | ≲5 µm        | ≲10 µm       |
| Detection efficiency             | >99%         |              |
| Fake hit rate                    | < $10^{-5}$ event$^{-1}$pixel$^{-1}$ |              |
| Integration time                 | < 30 µs      |              |
| Power density                    | < 300 mW/cm$^2$ | < 100 mW/cm$^2$ |
| Temperature                      | 20°C to 30°C |              |
| TID radiation hardness$^a$       | 700 krad     | 10 krad      |
| NIEL radiation hardness$^a$      | $1 \times 10^{13}$ 1 MeV n$_{eq}$/cm$^2$ | $3 \times 10^{10}$ 1 MeV n$_{eq}$/cm$^2$ |

$^a$These values include a safety factor of ten.

first successfully running example of a large-scale HEP application [4]. However, further R&D is required to meet the stringent requirements of the ITS upgrade in terms of integration time, power consumption and radiation hardness.

The Pixel Chip of the upgraded ALICE ITS will be produced in the TowerJazz 0.18 µm CMOS imaging process, as illustrated in figure 3. The process allows the use of a high-resistive epitaxial layer on a p-substrate. Being a quadruple-well process, it offers a deep PWELL, which can be used to shield the NWELL of PMOS transistors. This makes the use of full CMOS circuitry in the pixel area possible without the drawback of parasitic charge collection by those NWELLS. In addition, applying a moderate negative voltage to the substrate can be used to increase the depletion zone around the collection diode and this way improve both the charge collection and the signal-to-noise ratio by decreasing the pixel capacitance.
Figure 3. Schematic drawing of a monolithic pixel in the TowerJazz technology. The deep PWELL shields the PMOS transistor, allowing for full CMOS circuitry in the active area of the chip. The indicated depletion zone can be increased by means of a moderate negative substrate voltage.

Figure 4. Photographs of (a) the pALPIDEfs chip and (b) a full-scale building block (FSBB) of the MISTRAL architecture.

Three main pixel architectures, the ALPIDE architecture and the ASTRAL/MISTRAL architectures, are under study for the use in the upgraded ALICE ITS, with the goal to select a common design in the first half of 2015. In both architectures several small scale prototypes have been produced and characterised in order to optimise the sensor pixel and the front-end. These prototypes have demonstrated that the requirements in terms of performance and radiation hardness can be met [3]. The first full scale prototypes with the final dimensions of $15 \times 30 \text{mm}^2$ have been received in May 2014 and already on this short time scale a comprehensive program of lab and test beam measurements has been carried out, including tests with irradiated chips and chips thinned to 50 $\mu$m. First results of these measurements confirm the positive outcome of the tests of the small scale prototypes. Two examples are given in figures 5 and 6 (for a more detailed description of the pixel chip development the reader is referred to [5]). Figure 5(a) shows a measurement of the discriminator transfer function of a quasi-final-size prototype of the MISTRAL architecture, called MISTRAL-FSBB (“Full Scale Building Block”, figure 4(b)), measured with analogue test injections. One sees an S-curve for each pixel with the response increasing from 0 to 100% when the threshold voltage is decreased. Figure 5(b) shows the noise and threshold values for all pixels. The first histogram gives the ENC noise extracted from the slope of the S-curves. The second his-
Figure 5. Performance examples of the FSBB of the MISTRAL architecture: (a) discriminator transfer functions and (b) extracted noise and threshold distributions.

Figure 6. First preliminary testbeam results with the pALPIDEfs chip. Figure (a) shows noise occupancy and efficiency as a function of the average threshold. Figure (b) shows the residual widths and the cluster size as a function of the average threshold. Both figures contain the results for three different pixel types.

togram shows the 50%-points of the S-curves; its width is a measure of the threshold dispersion. The double-peak structure is due to a layout problem, that has been identified and corrected in the following submission. For the different chip architectures and pixel geometries noise values between \(\sim 5\) e and \(\sim 15\) e have been determined.

Figure 6 shows a measurement of the performance of the first full-scale prototype chip of the ALPIDE architecture, called pALPIDEfs (figure 4(a)), in the test beam. Figure 6(a) shows the efficiency and the noise occupancy as a function of the average threshold for three different pixel types implemented on the chip.\(^1\) For thresholds below approximately 150 e the efficiency reaches a value of \(> 99\%\) whereas the noise occupancy is below \(10^{-5}\) hits/pixel/trigger for all settings of

\(^1\)For test purposes pixels with two different reset circuits and with different spacings around the collection electrode have been implemented in the chip.
the threshold. It has been found that the noise occupancy is not dominated by random noise, but by fixed pattern noise in a very small number of pixels ($\mathcal{O}(10^{-3})$), the origin is still under investigation. The spatial resolution, shown in figure 6(b) is slightly above the required 5 $\mu$m for the inner layers, taking into account that the values plotted here still include the telescope resolution, which is estimated to be in the order of 3 $\mu$m.

4 Flexible printed circuits and interconnection

Signals and Power for the pixel chips are routed on two-layer flexible printed circuits (FPC). In the inner barrel the nine chips of a stave are serviced by one FPC; in the outer barrel, where the data rate per chip is much lower but the number of chips larger, the pixel chips are grouped into modules with 14 chips, with each module having its own FPC. Figure 7 shows cross-section and a layout detail of an inner barrel FPC prototype. One sees the power planes for digital and analogue voltage as well as the 11 differential pairs for clock, configuration and the individual data lines of the 9 chips. The FPC is made from a low-CTE polyimide in order to reduce the CTE-mismatch between FPC and pixel chips. Power planes and signal lines are made from aluminium in the Inner Barrel FPC to reduce the material budget as much as possible and from copper in the Outer Barrel.

The interconnection between FPC and pixel chip is made by laser soldering. The principle of this connection technique is shown in figure 8. The FPC has metallised vias in the positions of the connection pads of the pixel chip, which are distributed over the whole surface of the chip. Solder balls are placed in the vias and heated with a short laser pulse, such that they melt and establish the connection between the metallisation of the via and the chip pad. The correct wetting of both contacts can be nicely seen in a cross section, as shown in the last photo of figure 8. The connection by means of laser soldering has been successfully adopted to the ITS design. It has been exercised with great reliability on many daisy chain chips and first samples of fully functional pALPIDEfs chips have successfully been laser-soldered and read out through the FPC. As can be seen from figure 7 the laser soldering also allows for a different arrangement of the contact pads than in conventional wire bonded modules: whereas the signal pads are at the chip border, the power and ground connection pads are located over the matrix. This allows for a more homogeneous distribution of the power and saves an additional routing layer on the FPC.
Figure 8. Connection of pixel chips and FPC by laser soldering. Top row: cross section of the FPC on top of the chip and schematic drawing of the laser soldering procedure. Bottom row: photos of the solder balls after deposition, a single ball before and after reflow and a cross section through a single contact after soldering.

Figure 9. (a) Material distribution in the inner barrel and (b) exploded schematic view of an inner barrel stave.

5 Mechanics and cooling

As mentioned before, the upgraded ITS consists of an inner barrel (IB) and an outer barrel (OB). The IB layers are located at radii 22 mm, 31 mm and 39 mm, the OB layers at radii 194 mm, 247 mm, 353 mm and 405 mm. The inner barrel staves will have a length of 270 mm, the outer barrel will have two layers with a stave length of 843 mm and two with a length of 1475 mm. Due to the large range in dimensions a slightly different design is needed for inner and outer barrel. An inner barrel stave, as shown in figure 9(b), consists of a carbon spaceframe, a cold plate with polyimide cooling ducts as well as the nine pixel chips with the FPC. Figure 9(a) shows the material distribution of the inner barrel stave; it exhibits an average material budget of 0.3\% \( X_0 \) with peaks in the overlap region and in the regions of the cooling ducts. In case of the outer barrel a stave is subdivided into two half-staves, which in turn consist of modules with 14 chips each. Prototypes of
Figure 10. Cooling performance measurement with a prototype IB stave equipped with resistive heaters. The plot shows the heater temperature as a function of the water flow rate for different power densities.

As summarised in table 1 the chips have to be kept at room temperature at a maximum power dissipation of 300 mW/cm$^2$ in the Inner Barrel and 100 mW/cm$^2$ in the Outer Barrel. This will be achieved by a “leakless” water cooling system, which is operated such that the pressure is below 1 bar everywhere in the detector. Both for the Inner and the Outer Barrel, tests with resistive heaters have shown that the cooling system satisfies the requirements. This is shown in figure 10 for the Inner Barrel. The figure shows the heater temperature as a function of the flow rate for different power densities. One sees that even for power densities exceeding the pixel chip specifications a temperature well below 30$^\circ$C can be maintained. At the same time for all flow rates the pressure drop within the cooling circuit was significantly below 1 bar ($<$ 0.3 bar), which is necessary to fulfil the condition of a leakless system.

6 Summary and outlook

ALICE will replace its entire Inner Tracking System by a MAPS-based pixel-only tracker in the second long shutdown of the LHC (LS2) in 2018/2019. The upgrade will significantly improve impact parameter resolution, momentum resolution and tracking efficiency as well as readout rate capabilities. All R&D aspects of the project are currently in a close-to-final state: for the sensor, large-scale prototypes of two separate design architectures are currently being characterised and have shown satisfactory results. The mechanical structures have been prototyped and successfully tested. Also the novel laser soldering technique to establish the connection between the pixel chips and the flexible printed circuit has been successfully applied to working prototype chips. The important steps in the coming year will be characterised by the engineering of final prototypes and the preparation for the start of the construction in 2016. In particular, the sensor design will be
finalised, first inner barrel staves and outer barrel modules with working chips will be built and mass production and test procedures will be finalised.

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