An 8-bit In Resistive Memory Computing Core with Regulated Passive Neuron and Bit Line Weight Mapping

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Abstract—The rapid development of Artificial Intelligence (AI) and Internet of Things (IoT) increases the requirement for edge computing with low power and relatively high processing speed devices. The Computing-In-Memory(CIM) schemes based on emerging resistive Non-Volatile Memory(NVM) show great potential in reducing the power consumption for AI computing. However, the device inconsistency of the non-volatile memory may significantly degenerate the performance of the neural network. In this paper, we propose a low power Resistive RAM (RRAM) based CIM core to not only achieve high computing efficiency but also greatly enhance the robustness by bit line regulator and bit line weight mapping algorithm. The simulation results show that the power consumption of our proposed 8-bit CIM core is only 3.61mW (256*256). The SFDR and SNDR of the CIM core achieve 59.13 dB and 46.13 dB, respectively. The proposed bit line weight mapping scheme improves the top-1 accuracy by 2.46% and 3.47% for AlexNet and VGG16 on ImageNet Large Scale Visual Recognition Competition 2012 (ILSVRC 2012) in 8-bit mode, respectively.

Index Terms—In-memory computing, Non-volatile memory, Neuromorphic chip, Resistance inconsistency, Weight quantization and mapping

I. INTRODUCTION

In the past decade, with internet of things, cloud computing, computer vision, and artificial intelligence becoming increasingly connected to do perception, cognition, decision, and interaction, sensing devices in intelligent products are going to be the key interfaces to the real world. However, communication, storage, information retrieval, computation, and recognition will face great challenges due to the extremely large amount of sensing data. Because of the separation of the data acquisition, processing, and analysis, the conventional intelligent systems are suffering from problems like high construction cost, high power consumption, low efficiency, and long latency [1]. To address these issues, the majority of AI computations will be moved to light-weight IoT devices [2]. Nevertheless, Moores Law has come to an end and the processor performance will be benefited little at the end devices with limited computation capability and storage resources.

The high density and low power emerging resistive Non-Volatile Memory (NVM) [3]–[11] which enables massive parallel Computing In-Memory (CIM) is a promising candidate to solve the above-mentioned issues [12]–[14]. The majority of works are utilizing the multilevel resistance of the resistive memory for both storage and computation [15]–[18]. For example, Hewlett Packard Laboratories (HPL) proposed a Dot Product Engine (DPE) with the inverting amplifier [19], [20] designed In-Situ Analog Arithmetic in Crossbars (ISAAC) which utilizes eight 4 level RRAM cells to represent 16-bit weight. Though resistive NVM provides a potential solution as the CIM unit, its non-ideal properties greatly degenerate the reliability of the system. A few widely known properties of resistive NVM are the non-linear resistance value with different biasing voltage, level to level resistance variation, and cell to cell resistance variation, which will cause significant errors in quantization, resulting in the accuracy loss in the network. To reduce the mapping errors and improve the linearity of the CIM system, a more reliable design is needed which may be at the cost of the increasing of the computing energy.

[21], [22] proposed Serial-Input Non-Weighted Product (SINWP) whose inputs are modulated by time instead of the analog voltage, which will address the non-linearity issue caused by the biasing voltage. However, the digital-to-time converter will greatly increase the computing time at high data width. [23] proposed a novel Multiple Binary RRAM with Active Integrator (MBRAI) CIM core architecture, where multiple binary RRAM cells are used to store one weight. MBRAI could save a lot of power because binary code is used at the input instead of a time signal. Therefore, it requires only n CIM computations instead of $2^n$. The n-bit input data are sequentially computed by the CIM core and weighted at the output neurons, which greatly improves the linearity because of the identical input voltage. However, the power consumption of this scheme is dominated by the operational amplifier (>95%) [23], which reduces the computing efficiency of the CIM core to 0.61 Tera-Multiply-Accumulates per Second per Watt (TMACs/s/W). What’s more, the accuracy is still be influenced by the quantization and the inconstancy of the resistive NVM cells. To reduce power consumption, a CIM core with regulated passive integrators is proposed in this paper. A pseudo-binary weight quantization and bit line weight mapping method aimed at solving the resistance inconsistency is also introduced. The simulation results show that the power

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consumption of the proposed 256*256 CIM core in 8-bit mode is reduced by 98.2% compared with MBRAI.

The rest of this paper is organized in the following manner. Section II introduces the background of CIM with resistive NVMs. Section III shows the proposed circuit, problems brought by resistance inconsistency, and corresponding optimization. Finally, simulation results are presented in Section IV with the conclusion in Section V.

II. BACKGROUND AND RELATED WORKS

The majority of the computations in the neural network are matrix multiplication and accumulate operations, which can be well implemented by crossbar architecture as shown in Fig. 1. The processing units shown as black dots multiply the input from word lines by the stored weight. The neuron represented by the triangle accumulates the multiplication results at the same bit line.

Fig. 1. Microarchitecture of a CIM core. The word lines get input data from the former neurons while the bit lines is to accumulate data at the neurons (triangles). The black dots are the computing unit.

In conventional schemes, the weight of the neural network is stored in SRAM. For example, [24] proposed a 7-bit input and 1-bit weight MAC using a 1T1 SRAM cell. However, the precision is limited by the 1-bit weight and the area is large due to the SRAM array. Emerging NVMs which have high density and simpler structure as memory unit will greatly improve the precision of the weight and reduce the core area for its application on CIM. A design of CIM core with NVM in DPE is shown in Fig. 2. It employs memristor crossbar for matrix multiplication where memristor stores the weight by its resistance. Once the input is converted to analog voltage by DAC, the output voltage is determined by the conductance of the resistance as \( V_{out} = \sum V_{in}GR_f \), where \( R_f \) is the feedback resistance, and \( G \) is the conductance of the cross-point memristor device. After that, the output voltage is digitalized by the ADC for data transmission. DAC and ADC, which are power-hungry components, are necessary to resist the noise and signal deformation in data transmission. MBRAI proposed in [23] moves the input DACs to the output and shares the ADC for lower power consumption. RRAM is utilized in MBRAI proposed in [23] moves the input DACs to the output and shares the ADC for lower power consumption. RRAM is chosen as the storage unit for its reconfigurability, high density, and low power consumption. However, it is a great challenge to precisely control the resistance value of RRAM. Therefore, MBRAI utilizes n RRAM cells with binary resistance states whose high resistance state (HRS) is 0 and low resistance state (LRS) is 1, to represent an n-bits weight to achieve a high Effective Number of Bits (ENOB) for weight mapping. Fig. 3 is the simplified integration circuit of MBRAI. The input is sent in bit by bit from Least Significant Bit (LSB) to Most Significant Bit (MSB), which is more computing reliable since every bit is identical in computation. The importance of each bit of the input data and network weights are weighted by the charge redistribution at the neurons.

Though MBRAI achieves better computing reliability, there are still two critical issues that need to be addressed. Firstly, the power consumed by amplifiers in active integrators accounts for more than 95% of the energy cost of the whole CIM core. Secondly, the resistance of the RRAM cells has a wide distribution, resulting in significant quantization errors when mapping weights of the neural network into the RRAM array. To address the first issue, a passive integrator is proposed. An regulator is designed to improve the linearity of the integration results. The details will be introduced in Section III.A. To address the second issue, a pseudo-binary quantization and bit line weight mapping method is proposed to reduce the impact.
III. PROPOSED CIM CORE AND MAPPING METHOD

Although a passive integrator can significantly reduce power consumption by removing the amplifier, it has a serious non-linear problem. Fig. 4 shows the passive integrator circuit and its integration process where the current decreases with the decreasing of the integrating voltage $V_C$. To improve the linearity of the circuit, we design an optimized n-bit integral multiplier shown in Fig. 5.

1) We switch the position of RRAM and transistor in 1R1T so that the reading voltage on the RRAM cell is mainly determined by the gate and threshold voltages of the transistor. To differentiate from the conventional structure, the new structure is named as 1R1T.

2) The saturation current of the transistor in 1R1T can be influenced by the change of the integrating voltage because of the channel length modulation effect. To minimize the impact of the integrating voltage, we add NMOS $T_0$ at bit line to isolate the integrating voltage and drain voltage of 1R1T and thus reduce the variation of the integrating current.

3) Because the load of the bit line is affected by the number of input lines and the weights’ values, the linearity of the circuit is still influenced by the change of the source voltage of $T_0$ (the drain voltage of the 1R1T). Therefore, a regulator is added at $T_0$ to make sure the stability of the drain voltage of 1R1T.

4) Besides the nonlinearity in the bit line voltage, the cell to cell variation makes the devices’ integrating current inconsistent which decreases the robustness of the system. To improve reliability, we propose a pseudo-binary quantization and bit line weight mapping method with corresponding circuit which utilizes the uncertainty of resistive NVM to reduce quantization error.

A. CIM Core with Regulated Passive Integrator

1) Core Design: Assuming the n-bit input sequence is $X_1, X_2, ..., X_l$ and the weight is $W_1, W_2, ..., W_l$, the multiplication and accumulation (MAC) can be expressed as

$$Y = \sum_{i=1}^{l} X_i W_i = \sum_{i=0}^{n-1} 2^i x_{i,j} W_i$$

$$= \sum_{i=1}^{l} \sum_{j=0}^{n-1} 2^i \sum_{k=0}^{n} 2^k x_{i,j} w_{i,k}$$

where $x_{i,n-1}x_{i,n-2}...x_{i,0}$ and $w_{i,n-1}w_{i,n-2}...w_{i,0}$ is the binary format of $X_i$ and $W_i$ for $x_{i,j}, w_{i,k} \in (0, 1)$. It can be observed from Eq. (1) that there are three consecutive accumulations. The proposed CIM core utilizes n integrator cells to get $\sum_{i=1}^{l} x_{i,j} w_{i,k}$ by charge integration, and the results are stored in the passive regulated neuron composed by the capacitance array in Fig. 3 for charge redistribution to get the $\sum_{i=1}^{l} x_{i,j} W_i$. The $\sum_{i=1}^{l} x_{i,j} W_i$ is also added up by charge redistribution to get $\sum_{i=1}^{l} X_i W_i$. The integration for the resistances in the same bit line will be finished simultaneously by sharing the integrator so that the MAC can be finished parallelly to achieve a smaller core area and faster computing speed. Multiple neurons are enabled at a time in the integration phase when the inputs are divided into n cycles and calculated from LSB to MSB. After integration and charge redistribution, the data conversion phase is started for neurons to convert the analog results into digital output.

2) Integral Multiplier: The word line inputs shown in Fig. 5 are sent in once a bit from LSB to MSB. The process of multiplication in the integral multiplier includes the integration phase and the charge redistribution phase. When in the integration phase, $S_2$ is closed, $S_1, S_3,$ and $S_4$ are open. After the integration, the charge is redistributed with $S_1$ and $S_2$ open and $S_3$ and $S_4$ closed in the charge redistribution phase. Taking $C_{n-1}$ as an example, the integrating voltage after the integration phase is

$$V_{c,n-1} = V_{c,n} - \frac{V_{D2} \sum_{i=0}^{l-1} D_i T}{C_f R_i}$$

where $V_{c,n}$ is the initial voltage of $C_{n-1}$, $D_i$ is one input bit of the $i_{th}$ input line, $l$ is the number of input lines, T is the integration time, $R_i$ is the equivalent resistance of the 1R1T unit of the $i_{th}$ input line and $V_{D2}$ is the drain voltage of 1R1T unit. The capacitances satisfy the following constraint

$$C_f = 2C_{n-1} = 2^2 C_{n-2} = 2^3 C_{n-3} = \ldots = 2^n C_0$$

Assuming there is only one input line and the initial integrating voltage is set to $V_{c}^-$, the integrating voltage $V_{s}$ after one step of charge redistribution is

$$V_s = \frac{V_{c,n-1} C_{n-1} + V_{c,n-2} C_{n-2} + \ldots + V_{c,0} C_0 + V_{c}^- C_0}{C_{n-1} + C_{n-2} + \ldots + 2C_0}$$

$$= V_{c}^- - \frac{V_{D2} T}{C_f} \left( 2^l \sum_{i=0}^{l-1} \frac{D_i C_{n-1}}{R_i} + 2^2 \sum_{i=0}^{l-1} \frac{D_i C_{n-2}}{R_i} + \ldots + 2^n \sum_{i=0}^{l-1} \frac{D_i C_0}{R_i} \right)$$

(4)
ADC’s sampling capacitance $C_S$ which is connected to the integrator’s capacitance array is in the meantime used to add up the $n$ partial products. Let $C_S = C_f$, the new $V_{out}$ is

$$V_{out} = 2^{-1} (V_S + V_{out})$$  \(5\)

where $V_{out}$ represents the former voltage of the $C_S$. Assuming the initial voltage of the $C_S$ is $V_{init}$, then after $n$ steps of the charge redistribution, the voltage change is

$$\Delta V_{out} = V_{init} - (2^{-n}V_{init} + 2^{-n}V_{S,0} + \ldots + 2^{-1}V_{S,n-1})$$

$$= 2^{-n} \left[ (V_{init} - V_{S,0}) + \ldots + 2^{n-1} (V_{init} - V_{S,n-1}) \right]$$

$$= 2^{-n} \sum_{j=0}^{n-1} 2^j \Delta V_{S,j}$$  \(6\)

where $V_{S,n-1}$ is the $(n-1)_{th}$ integrating voltage of $V_S$ and $\Delta V_{S,j}$ is the voltage change of $V_S$ in the $j_{th}$ integration. As long as the $\Delta V_{S,j}$ is designed to represent the result of the $\sum_{i=0}^{l} x_{i,j} W_i$, Eq.\(6\) gives the result of $\sum_{i=0}^{l} \sum_{j=0}^{n-1} 2^j x_{i,j} W_i$.

3) Regulated Passive Integrator: By switching the position of 1T1R in Fig.\(3\) to 1R1T in Fig.\(5\) we can get the following equations

$$I = \frac{1}{2} K_2 (V_{G2} - V_R - V_{th2})^2$$  \(7\)

$$I = \frac{V_R}{R}$$  \(8\)

where $K_2$ is the device parameter of $T_2$, $V_{th2}$ is its threshold voltage, $R$ is the resistance of RRAM device, $V_R$ is resistance’s read voltage, $I$ is the integrating current passing through the 1R1T unit. According to Eq.\(7,8\) we can get

$$V_R = V_{G2} - V_{th2} - \sqrt{\frac{2K_2 R(V_{G2} - V_{th2})^2 + 1 - 1}{K_2 R}}$$  \(9\)

The drain voltage of $T_2$ ($V_{D2}$), which is isolated from the integrating voltage by $T_0$, satisfies the following equation

$$I_b = \frac{1}{2} K_0 (V_{G0} - V_{D2} - V_{th0})^2$$  \(10\)

where $I_b$ is the integrating current of the bit line, $K_0$ is the device parameter of $T_0$. The proposed regulator circuit shown in Fig.\(5\) stabilizes the $V_{D2}$ of the 1R1T units by applying a negative feedback. $T_1$ works at the saturation region, which satisfies the following equation

$$I_{ref} = \frac{1}{2} K_1 (V_{D2} - V_{th1})^2$$  \(11\)

where $K_1$ is the device parameter of $T_1$, $V_{th1}$ is the threshold voltage of $T_1$. According to Eq.\(10,11\) we get

$$V_{G0} = V_{th1} + \sqrt{\frac{I_{ref}}{K_1}} + V_{th0} + \frac{I_b}{K_0}$$  \(12\)

$$V_{D2} = V_{th1} + \sqrt{\frac{I_{ref}}{K_1}}$$  \(13\)

Since $I_{ref}$ is a constant, the drain voltage $V_{D2}$ of the 1R1T unit is stabilized by the regulator.
B. Pseudo-binary Quantization and Bit Line Weight Mapping Method

As the weight of the neural network is quantized to \( n \) bits rather than a continuous value, the quantization errors when mapping the weight of the neural network into the CIM system will influence the accuracy of inference. What’s more, the resistance distribution of resistive NVM may worsen the quantization. Therefore, it’s necessary to discuss the quantization method and the corresponding errors in this section. To reduce the quantization error caused by the cell to cell variation, a pseudo-binary quantization and bit line weight mapping method is proposed.

1) Quantization Error with NVM: Quantization is an important method for compressing the neural network and accelerating the computation speed, among which uniform quantization is a basic one. The typical quantizer of uniform quantization can be expressed as

\[
Q(x) = \Delta \cdot \left\lfloor \frac{x + \frac{1}{2}}{\Delta} \right\rfloor
\]

(14)

where \( \Delta \) is the quantization step size of some value, \( x \) is the value to be quantized. When the quantization step size (\( \Delta \)) is small relative to the variation in the signal being quantized, it is simple to show that the mean squared error which is also called the quantization noise power produced by such a rounding operation will be \( \Delta^2/12 \). The calculation process is

\[
QE = \int_0^\Delta \frac{1}{2} x^2 dx = \frac{\Delta^2}{12}
\]

(15)

The maximum (\( w_{\text{max}} \)) and the minimize (\( w_{\text{min}} \)) of the data range and the quantization bits \( n \) determine the quantization step size since they usually have the relationship

\[
\Delta \times 2^n = (w_{\text{max}} - w_{\text{min}})
\]

(16)

Considering the resistance distribution, the practical non-linear quantizer is shown as follows

\[
\sum_{i=1}^{2^n} \Delta_i = (w_{\text{max}} - w_{\text{min}})
\]

(17)

Assuming the resistance distribution is a general normal distribution represented as

\[
f(x|\mu, \sigma^2) = \frac{1}{\sqrt{2\pi}\sigma}e^{-\frac{(x-\mu)^2}{2\sigma^2}}
\]

(18)

The Probability Density Function (PDF) of the quantization error is the noncentral chi-squared distribution with one degree of freedom. Then, the mean value of the quantization error is given by

\[
\mu = k + \frac{\lambda}{12} = 1 + \frac{\Delta^2}{12} = 1 + \frac{(w_{\text{max}} - w_{\text{min}})^2}{12 \times 2^{2n}}
\]

(19)

and the variance of the quantization error is

\[
\sigma^2 = 2(k + 2\lambda) = 2 + 4\mu^2 = 2 + 4\Delta^2
\]

(20)

\[
= 2 + \frac{(w_{\text{max}} - w_{\text{min}})^2}{2^{2(n-1)}}
\]

As we can see, the quantization error is greatly increased when there is a distribution in resistance. Since the quantization errors are accumulated in the network, the accuracy will be greatly reduced.

2) Resistance Measurement: The proposed quantization and mapping method needs the resistance value of the RRAM array in LRS, so we firstly set all memory units to LRS and read the resistance of the RRAM array by ADC in resistance reading phase. The reading process consists of integration phase and charge redistribution phase when the switches are set different from multiplication. For example, when reading the resistance unit \( R_{n-1,m-1} \) in Fig. 5, the switches in the same bit line with \( R_{n-1,m-1} \) are used while the others stay open. In the integration phase, \( S_1, S_3, \) and \( S_4 \) are open, \( S_2 \) is closed and the input of \( (m-1)_{th} \) line word line is 1 while the others are 0. The integration result is a typical result of Eq. 2 where \( l=1, D=1 \). When ADC read the integrating voltage during the charge redistribution, \( S_2, S_3, \) and \( S_4 \) are closed and \( S_1 \) is open. The voltage read by ADC is

\[
V_{out} = \frac{V_{\text{init}} + V_S}{2}
\]

(21)

where \( V_{\text{init}} \) is the initial voltage for both sampling capacitances and integration capacitances, and \( V_S \) is the integration result. The integration process satisfies

\[
V_{\text{init}} - V_S = \frac{IT}{C_f} = \frac{V_{D2}T}{RC_f}
\]

(22)

where \( I \) is the integrating current passing through 1R1T unit, \( T \) is the integration time, \( R \) is 1R1T’s resistance and \( V_{D2} \) is the read voltage of the bit line. Therefore, we can get

\[
R = \frac{V_{init}T}{2C_f(V_{\text{init}} - V_{out})}
\]

(23)

3) Quantization and Mapping Method: Since the normalized resistance in LRS is not exactly digital 1, a pseudo-binary code whose importance of bits from MSB to LSB is still the same as the conventional binary code is proposed in our mapping schemes. The main difference is that the value of the pseudo-binary code is related to the resistance of the memory unit, which is given by

\[
\hat{w} = r_{n-1} \times 2^{n-1} + r_{n-2} \times 2^{n-2} + \ldots + r_0 \times 2^0
\]

(24)

where for the LRS, \( r_i \) is the normalized resistance of the \( i_{th} \) bit (mean value is 1) of the weight. For the high resistance, since the resistance can be much larger than the low resistance, \( r_i \) is set as 0, and the uncertainty of the high resistance is ignored in this paper. The weight quantization procedure is from MSB to LSB and we define the condition as follows

\[
q = \left\{ \begin{array}{ll}
1 & \left[ (r_i \times 2^{i-1} - w_{\text{res}}) > 0.5 \right] \\
0 & \left[ (r_i < 0.5) \left( r_i \times 2^{i-1} > 2 \times w_{\text{res}} \right) \right]
\end{array} \right.
\]

(25)

where \( r_i \) is the \( i_{th} \) bit of normalized memory resistance, and \( w_{\text{res}} \) is the remaining weight after partial quantization. The component \( (r_i < 0.5) \) is to abandon the device with too large resistance in LRS and \( r_i \times m_i - w_{\text{res}} > 0.5 \) is to check if the remaining weight is larger than the product of
the importance of the bit and the resistance of the memory. The component $r_i \times m > 2 \times w_{res}$ is to minimize the quantization error of the LSB. Because of the memory resistance distribution, $|r_0 \times m_0 - w_{res}|$ could be larger than $w_{res}$. In other words, the memory should be in high resistance in case $|r_0 - w_{res}| > w_{res}$ to minimize the quantization errors.

However, the initial memory sequence may not be the best solution to minimize the quantization error. For example, assuming $w=13.4$, and four memory units with normalized resistance 1.05, 1.1, 1.125, 0.93 are used to quantize the weight. The conventional binary code may give a quantization error of 0.4 (4'b1101). Based on the given sequence, the resistance states of the four cells are low, low, high, low, which reduce the quantization error to -0.33. Furthermore, if we switch the third cell with MSB, the resistance of the four cells will be 1.25, 1.1, 1.05, and 0.93. In such a sequence, the resistance states of the four cells can be set to low, low, high, high, and high to minimize the quantization error to 0. This example shows that the sequence of the memory units is very important to minimize the quantization error.

The traversal algorithm can be used to search all possible sequences, and the sequence for the minimal quantization error is picked and configured in the chip. However, it may require a long searching time and its computation complexity is $O(n!)$.

Moreover, the cells in the same bit line should be in the same sequential position. Assuming the size of the weight matrix need to be quantized is $R \times 1$ and the size of RRAM array is $R \times C$ where $C$ means the weight is quantized to $C$ bits, we propose a greedy mapping algorithm whose loss when quantizing the $i_{th}$ bit is defined as

$$\text{loss} = \max_{j \in R} \left( w_{i-1,j} - \hat{w}_{i,j} \right) \sum_{j=1}^{j=R} \left( w_{i-1,j} - \hat{w}_{i,j} \right)^2 \quad (26)$$

where $w_{i-1,j}$ is the remaining value of the $j_{th}$ weight after partial quantization and $\hat{w}_{i,j}$ is the value quantized by the pseudo-binary quantization method in the $i_{th}$ bit of the $j_{th}$ row. Eq. (26) has taken both the worst case and the average case of the searching results into consideration. This bit line selection is started from MSB which influences the mapping result most to LSB. The algorithm traverses the remaining bit lines and chooses the bit line with minimum loss as the $i_{th}$ bit. To apply the algorithm in the circuit, the $n^\ast$ MUXn in Fig. 5 is used for switching the connection between the bit lines of the RRAM array and the integrators. When mapping the weights to the core, all the RRAMs are set to LRS at first. Then, according to the proposed mapping method, RRAMs with value 0 are set to HRS. By using this bit line weight mapping method, the computation complexity is reduced from $O(n!)$ to $O(n^2)$.

IV. Simulation Results

In this section, we do the functional verification of the multiplication and resistance reading process. Then we evaluate the circuit with dynamic performance, energy cost on circuit level and compare it with other CIM schemes on core level and network level. Finally, we present the robustness of the circuit. The circuit simulations are done in Cadence Analog Mixed Signal (AMS) with a 45nm generic Process Design Kit (PDK) and the network simulations are done on caffe platform.

A. Functional Verification

1) Multiplication Process Verification: We simulate the computing process shown in Fig. 6 to check the correctness of the proposed circuit in 8-bit mode. Fig. 6(a) presents the integration phase in an integrator, the integrating voltage $V_C$ shown in Fig. 5 is reset to 1V at 384 ns, and the integration phase starts at 393 ns. After 20 ns, the integration phase is completed and $V_C$ is decreased to 745.2mV. Then the charge redistribution starts at 415 ns. When charge redistribution is done, the 8 integrating voltages are converted to $V_{out}$. After that, $V_C$ is reset to 1V for the next integration. Fig. 6(b) shows the whole multiplication process of an 8-bit input (8'b10111010) and 8-bit weight (8'b11101100). The input
sequence is sent in from LSB to MSB and after 8 cycles of integration and charge redistribution, the output voltage $V_{out}$ is 831.6mV. Then ADC converts it to digital result as 8’b10101011. The theoretical results of the output voltage and digital result are 831.5mV and 8’b10101011, respectively. Therefore, the design achieves its functional requirement.

2) Resistance Measurement Verification: Fig.7 presents the resistance measuring process of one 1R1T unit where the state of the switches in the same bit line is simulated. The output voltage is set to 1V at first and the integration phase is started at 190 ns. Since only one 1R1T is working, the integrating current is small and thus the integrating time is set to 110 ns which is much longer than that of MAC operation. After integration, the sampling phase (i.e. the charge redistribution phase) starts at 440ns and the output voltage is 0.994 V. Then the ADC converts it to digital output.

B. Performance Evaluation

1) Circuit Level Performance: Table I shows the dynamic performance comparison between MBRAI and the proposed core. The computing speed, SFDR, SNDR, ENOB of the proposed CIM core are 1.85Ms/s, 59.13dB, 46.13dB, and 7.37bit, which are close to the performance indicators of MBRAI. Table II gives the power cost comparison between the proposed scheme and MBRAI. MBRAI consumes 0.22mW on amplifiers for stable read voltage while the proposed scheme and MBRAI. Table II gives the power cost comparison between MBRAI and the proposed CIM core.

C. Robustness Analysis

1) Linearity Analysis: The linearity comparison of integration results under different initial integrating voltage (0.7~1V) between the integrator without 1T1R unit position switching, integrator without $T_0$, and integrator with $T_0$ is shown in Fig. 8(a), Fig. 8(b), and Fig. 8(c), respectively. The Differential Nonlinearity (DNL) and Integration Nonlinearity (INL) are used to evaluate the performance. The INL/DNL is (-1.66~0.89)/(-2.19~1.95) LSB for the integrator without 1T1R unit position switching, (-0.63~0.95)/(-1.24~1.35) LSB for integrator without $T_0$, and (-0.40~0.60)/(-0.79~0.87) LSB for the integrator with $T_0$ which confirms that the linearity of the integration process is greatly improved by 1T1R unit position switching and $T_0$. Fig. 9(a) and Fig. 9(b) present the linearity evaluation of the proposed integral multiplier with different input and weight by the code density measurement. The circuit achieves INL/DNL of (-0.51~1.35)/(-0.87~0.28) LSB, (-0.60~0.001)/(-0.14~0.17) LSB corresponding to input value and weight, respectively. The linearity comparison of the integral multiplier under different input lines between the circuit with regulator and without regulator is shown in Fig. 9(c) and Fig. 9(d) respectively. The INL/DNL is (-2.01~0.38)/(-0.01~0.01) LSB for the circuit with regulator and (-12.7~4.26)/(-0.2~0.62) LSB for the circuit without regulator, which shows that the linearity in terms of the number of input lines is significantly improved by the regulator for providing a relatively stable drain voltage of 1R1T when the loads of bit line change.

2) PVT Simulation: To verify the robustness of the circuit, different combinations of process, voltage, and temperature...
### TABLE III
Core level comparison between the proposed scheme and other CIM schemes

| Structure                  | Technology | Crossbar Size | Weight/Data Bit | Throughput(GMAC/s) | Power(mW) | Efficiency(TMAC/s/W) |
|---------------------------|------------|---------------|-----------------|-------------------|-----------|---------------------|
| SINWP [21]                | 55nm       | 256*512       | fixed-3/fixed-1 | —                 | —         | 53.17               |
| MBRAI [23]                | 45nm       | 256*256       | fixed-3/fixed-2 | —                 | —         | 21.9                |
| A 22nm 2Mb ReRAM CIM Macro [26] | 22nm       | 512*512       | fixed-3/fixed-1 | 1524              | 19.6      | 77.76               |
| Proposed                  | 45nm       | 256*256       | fixed-4/fixed-1 | —                 | —         | 121.38              |
| A CIM SRAM Macro in 7nm FinFET CMOS [27] | 7nm       | 4kb           | fixed-4/fixed-4 | 1092.2            | 1.975     | 553.01              |

### TABLE IV
Accuracy and energy estimation of different RRAM-based scheme

| Network                  | The Number of Operations | Structure            | System Frequency | Data Bit | Crossbar Size | top-1 error Rate | Energy(uf/Jmg) | Saving(%) |
|--------------------------|--------------------------|----------------------|------------------|----------|---------------|------------------|----------------|-----------|
| LeNet on MNIST           | 0.42M                    | MBRAI [23]           | 100MHz           | 1        | 128*128       | 1.40%            | 6.68           | 99.81%    |
| AlexNet on ILSVRC 2012  | 720M                     | MBRAI [23]           | 25MHz            | 8        | 256*256       | 0.97%            | 0.71           | 98.17%    |
|                          |                          | Proposed             | 10MHz            | 8        | 256*256       | 13.00%           | 101.3         | —         |

### TABLE V
PVT simulation on ENOB

| Process | Temperature( °C) | Voltage(V) | ENOB(bit) |
|---------|------------------|------------|-----------|
|         | 25               | 0.9        | 7.36      |
| A       | 40               | 1.1        | 7.3      |
| B       | 60               | 0.9        | 7.25      |
| C       | 80               | 0.9        | 7.27      |

Fig. 8. The INL/DNL comparison of integration results under different simulating conditions: (a) integrator with ITR unit position switching, (b) integrator without T0, and (c) integrator with T0.

### 3) Quantization and Mapping Methods Comparison

To add the impact of resistance distribution into the weight of the neural network, the resistance reading phase is needed when the ADC is used to read the resistance of the RRAM array. To make things easy, the process of ADC reading IRIT circuit with fixed resistance is firstly simulated by 1400 Monte Carlo simulations to evaluate the impact of the transistor variation, then the resistance inconsistency is evaluated by adding a normalized Gaussian distribution. The normalized distribution of RRAM array read by ADC is shown in Fig [10], where the standard deviation of the normalized Gaussian distribution is 0.2. Fig. [11] shows the comparison of 1400 Monte Carlo simulations on the computation error of combination of input 180, weight 75, number of input lines 128 between normal mapping and bit line weight mapping method. The average value and the standard deviation of the error in normal mapping method are 0.124 LSB and 1.744LSB, respectively, while those of the errors in bit line weight mapping method are 0.013 LSB and 0.104 LSB, respectively. The mapping result indicates that the bit line weight mapping method significantly improves our CIM core’s robustness to variations of device inconsistence.

To test the effect of the bit line weight mapping method on network level, three quantization and mapping methods are simulated. The first one is normal binary quantization and mapping method, which quantifies the weight to digital 8-bit value and set the resistance HRS/LRS according to the corresponding digital bit 0/1. The second one is resistance based quantization and mapping method that quantifies the weight according to Eq [25]. The third one is resistance based quantization and bit line weight mapping method proposed in this paper. Fig. [12] shows the quantization error ratio (sum of absolute values of quantization error/sum of absolute

are chosen to do the PVT simulation where ENOB is used to evaluate the core’s performance. The ENOBs in these PVT combinations are all greater than 7 bits as shown in Table [V] which indicates that the proposed circuit is reliable with variations of process, voltage, and temperature.
Fig. 9. The evaluation of linearity in terms of (a) different input (0-255) and (b) different weight (0-255) and the INL/DNL comparison between (c) integral multiplier with regulator and (d) integral multiplier without regulator under different input lines (1-256).

values of weight) and the loss of top-1 accuracy comparison between three methods under different quantization bits (the deviation of normalized resistance is 0.2) and different standard deviation of normalized resistance distribution (the quantization bits is 8) on AlexNet and ILSVRC 2012; Fig. 12(b) presents the quantization error ratio and the loss of top-1 accuracy comparison between quantization methods with different quantization bit (the deviation of normalized resistance is 0.2) and standard deviation of the resistance distribution (the quantization bits is 8) on VGG16 and ILSVRC 2012. As shown in Fig. 12, the optimized quantization and bit line weight mapping method helps reduce the quantization errors and improve the inference accuracy both on AlexNet and VGG16. For example, the accuracy loss in 8-bit mode with 0.2 deviation on AlexNet are 2.97% and 0.51% for normal binary mapping method and bit line weight mapping method, respectively, and those on VGG16 are 2.70% and 0.39% for normal binary mapping method and bit line weight mapping method, respectively. What’s more, with the uncertainty of the resistance increasing the effect of the optimization is more evident.

V. CONCLUSION

In this paper, an 8-bit RRAM based CIM core with regulated passive neuron and bit line weight mapping method has been proposed. The non-linearity brought by the passive integrator and the errors caused by quantization and the cell to cell variation have been discussed. To address the above issues, the detailed regulated integral multiplier and the bit line weight mapping method have been presented. The circuit level simulation has shown that the proposed CIM core achieves 3.61mW on power consumption with the size of 256*256.
Fig. 12. The accuracy comparison between A: Resistance based quantization and bit line weight mapping method, B: Normal binary quantization and mapping method, and C: Resistance based quantization and normal mapping method. The left two figures are quantization error ratio (sum of absolute values of quantization error/sum of absolute values of weight) and loss of top-1 accuracy of AlexNet on ILSVRC 2012 with different quantization bits (the deviation of normalized resistance is 0.2) while the right two are quantization error/sum of absolute values of weight) and loss of top-1 accuracy of AlexNet on ILSVRC 2012 with different standard deviation of normalized resistance distribution (the quantization bits is 8). The left two figures are quantization error ratio and loss of top-1 accuracy of VGG16 on ILSVRC 2012 with different quantization bits (the deviation of normalized resistance is 0.2) while the right two are quantization error ratio and loss of top-1 accuracy of VGG16 on ILSVRC 2012 with different standard deviation of normalized resistance distribution (the quantization bits is 8).

![Graphs showing accuracy comparison.]

in 8-bit input and 8-bit weight mode, which is reduced by 98.2% compared with MBRAI while the SFDR and SNDR of the CIM core achieve 59.13 dB and 46.13 dB, respectively. The network level simulation has shown that the CIM core achieves 0.90% top-1 error rate with 0.013 uJ/img on LeNet and 43.60% top-1 error rate with 16.65 uJ/img on AlexNet, which are better than other schemes. The linearity and PVT simulation has been done to verify the robustness of the circuit. The simulation on mapping methods has shown that compared with normal mapping method, the proposed bit line weight mapping scheme achieves better performance which improves the top-1 accuracy by 2.46% and 3.47% for AlexNet and VGG16 on ILSVRC 2012 in 8-bit mode.

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