Automatic Generation of Complete Polynomial Interpolation Hardware Design Space

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Abstract—Hardware implementations of complex functions regularly deploy piecewise polynomial approximations. This work determines the complete design space of piecewise polynomial approximations meeting a given accuracy specification. Knowledge of this design space determines the minimum number of regions required to approximate the function accurately enough and facilitates the generation of optimized hardware which is competitive against the state of the art. Targeting alternative hardware technologies simply requires a modified decision procedure to explore the space.

Index Terms—datapath, elementary function, interpolation

I. INTRODUCTION

A common challenge in hardware design is how best to compute complex functions such as the reciprocal, sine, cosine etc. Hardware algorithms to compute elementary functions generally use one of the following techniques: digit-recurrence [1], CORDIC (COordinate Rotation Digital Computer) [2] or piecewise polynomials [3]. In this paper we focus on piecewise quadratic or linear implementations. The degree and number of polynomials used to approximate a function depends on the required precision and target error bound. For binary32 interpolation, quadratic is usually sufficient.

We study the following question. Given a fixed-point function to approximate to within some error bound, what is the complete design space of all feasible piecewise quadratic/linear approximations, constrained only by the underlying architecture, described in Figure 1. Knowledge of the complete design space allows us to tailor the design space exploration for different hardware targets, without needing to re-generate the design space. Interpreting mathematical bounds as polynomial design space constraints is not a novel concept [4] but is extended and generalised in this work.

Automatic tools for generating efficient piecewise polynomial hardware already exist [5–7], one example being FloPoCo [8, 9] which uses Sollya [10] to generate its polynomial approximations. Sollya uses a modified Remez algorithm [11], which computes minimax polynomial approximations subject to the constraints of finite precision coefficients. Such an approach explores a constrained design space, allowing it to quickly generate high precision approximations.

We present the mathematics to generate the complete design space of piecewise polynomial approximations to a given function. An example decision procedure is presented along with the resulting hardware.

Fig. 1. Quadratic interpolation hardware architecture. The most significant bits, \( r \), of the input are passed to a lookup table (LUT). The least significant bits, \( x \), are used in the polynomial evaluation [4].

II. DESIGN SPACE GENERATION

The target function, \( f \), and accuracy are specified via input and output precisions along with upper and lower bounds across all inputs. Using upper and lower bounds provides maximal flexibility and can even accommodate asymmetric error bounds on a function. Determining the space of feasible quadratic interpolations is reduced to a series of inequalities.

We use fixed-point notation \( n.m \) to denote a format with \( n \) integral bits and \( m \) fractional bits. Given \( f : n.m \rightarrow p.q \) and integer upper and lower bound functions \( u, l : n + m \rightarrow p + q \). For a fixed number of lookup bits, \( R \), define the following.

\[
Z = z_{n-1} \ldots z_0 . z_{-1} \ldots z_{-m} \quad \text{(input fixed-point value)}
\]

\[
r = z_{n-1} \ldots z_R \quad \text{(unsigned integer)}
\]

\[
x = z_{n-R} \ldots z_{-m} \quad \text{(unsigned integer)}
\]

Let \( I_R(r, x) = l(\{x, r\}) \) and \( u_R(r, x) = u(\{x, r\}) \), where \( \{,\} \) denotes concatenation. Under these definitions the bounds satisfy \( 2^{-q}l_R(r, x) \leq f(Z) \leq 2^{-q}u_R(r, x) \). Fixing an \( R \) also fixes an interval for \( x \in I = [0, 2^{n+m-R} - 1] \), so for a given value of \( r < 2^R \), a feasible quadratic is defined by the quad \( (a, b, c, k) \), where \( k \) is the difference between the polynomial evaluation precision and output precision, which satisfies:

\[
\forall x \in I, l_R(r, x) \leq \left( \frac{ax^2 + bx + c}{2^k} \right) \leq u_R(r, x)
\]
or equivalently (the $x \in I$ being implied in the remainder)
\[
\forall x \quad l_R(r, x) \leq \frac{ax^2 + bx + c}{2^k} < u_R(r, x) + 1.
\]
Rearranging gives necessary and sufficient existence conditions for $c$:
\[
2^k l_R(r, x) - ax^2 - bx \leq c < 2^k (u_R(r, x) + 1) - ax^2 - bx \quad (1)
\]
If a feasible $c$ exists then $\forall x, y$:
\[
2^k l_R(r, x) - ax^2 - bx < 2^k (u_R(r, y) + 1) - ay^2 - by. \quad (2)
\]
Introducing,
\[
d(r, x, y) = \frac{u_R(r, y) + 1 - l_R(r, x)}{y - x},
\]
reminiscent of a numerical derivative, we can bound $b$, under some assumptions. Eqn. (2) is trivially true for $x = y$.
\[
x < y \Rightarrow b < 2^k d(r, x, y) - a(x + y) \quad (3)
\]
\[
x > y \Rightarrow b > 2^k d(r, x, y) - a(x + y) \quad (4)
\]
If a feasible $b$ exists then $\forall x < y$ and $w < z$:
\[
2^k d(r, y, x) - a(x + y) < 2^k d(r, w, z) - a(z + w). \quad (5)
\]
Eqns. (2) & (5) are necessary and sufficient conditions on existence since $k$ can be increased until the intervals contain an integer. Finally we bound $a$, using expressions that are closely related to numerical second derivatives.
\[
x + y = w + z : d(r, y, x) < d(r, w, z) \quad (6)
\]
\[
x + y < w + z : \frac{a}{2^k} < \frac{d(r, w, z) - d(r, y, x)}{w + z - x - y} \quad (7)
\]
\[
x + y > w + z : \frac{a}{2^k} > \frac{d(r, y, x) - d(r, w, z)}{x + y - w - z} \quad (8)
\]
Introducing further definitions,
\[
M(r, t) = \max_{x < y \atop x + y = t} d(r, y, x), \quad m(r, t) = \min_{x < y \atop w < z \atop w + z = t} d(r, w, z).
\]
The necessary and sufficient conditions for the existence of a feasible polynomial over a given region specified by $r$ are:
\[
\forall t \quad M(r, t) < m(r, t) \quad (9)
\]
\[
\max_{t < s} \frac{M(r, s) - m(r, t)}{s - t} < \min_{t < s} \frac{m(r, s) - M(r, t)}{s - t}. \quad (10)
\]
These bounds are intuitive because we bound the $b$ coefficient by something resembling a first derivative and $a$ by a second derivative term.

To generate the design space for a value of $R$, we test whether Eqns. (9) & (10) hold for all $r \in [0, 2^R - 1]$. Satisfiability implies existence of at least one feasible quadratic in each region, and we proceed to establish a dictionary of coefficients. Eqns. (7) & (8) determine an interval $[a_0, a_1]$ of valid $a$ values for $k = 0$. Then $\forall a \in [a_0, a_1]$, we solve Eqns. (9) & (10) to generate the interval $[b_0, b_1]$ of valid $b$ values, increasing $k$ if necessary to ensure we obtain at least one valid $b$ in each region. Lastly, for each valid $(a, b)$ pair we solve Eqn. (11) yielding an interval of valid $c$ values. Across all regions $k$ is constant. The result of this process is a nested dictionary of valid polynomial coefficients for fixed $k$ and $R$ values.

This dictionary represents the complete design space of feasible quadratic polynomials that satisfy the given upper and lower bound functions across the complete input space. If $\forall r \in [0, 2^R - 1], 0 \in [a_0, a_1]$ then a piecewise linear approximation will suffice, resulting in smaller and faster hardware.

A. Performance

Design space generation involves many 2-D searches across a potentially large search space, evaluating expressions of the form $\max_{x,y} D(x, y)$, where $D(x, y) = \frac{g(y) - h(x)}{y - x}$, for some $g$ and $h$, or the minimum of such expressions. To improve scalability we optimise these searches. A naive implementation would iterate across the complete 2-D space. In practice, we skip iterations of this search due to claim (11).

Claim II.1. Let $(x', y')$ be the arguments which maximise $D(x, y)$ across all $x < x'$. Then for $x > x'$,
\[
D(x', y') \leq \frac{h(x) - h(x')}{x - x'} \Rightarrow \exists y \text{ s.t. } D(x, y) > D(x', y').
\]

Proof. Suppose $\exists x > x'$ and $y > x$ s.t. $D(x, y) > D(x', y')$, it follows that $D(x, y) > D(x', y)$, since $D(x', y')$ maximal. Expanding the definition of $D$ and re-arranging,
\[
(x - x')g(y) + x'h(y) > y(h(x) - h(x')) + xh(x').
\]
Subtracting $x'h(x')$ from both sides and re-arranging,
\[
D(x', y') > \frac{h(x) - h(x')}{x - x'}.
\]

Since $D(x', y') \geq D(x', y)$, we have exactly the converse of the condition in our claim. □

Using this optimization the runtime of the design space generation is five times faster for a 16 bit reciprocal approximation running single threaded on an Intel Xeon E3-1270 CPU.

There is a computational tradeoff between the number of regions the input interval is sub-divided into ($R$), versus the input range that each polynomial must span, corresponding to the number of inputs to check for each polynomial. Empirical results for a 16 bit design suggest the runtime is $O(R^{-5})$. The design space generation algorithm scales exponentially in the number of bits of precision so these speedup techniques can improve runtimes in practical cases but do not substantially expand the space of computationally feasible designs.

III. Design Space Exploration

Having generated the design space, we must now derive efficient methods to explore this space. The exploration procedure can be tailored to the target hardware technology, one of the major advantages of generating the complete design space. In the procedures presented here we will have a target number of lookup bits to be used, as the optimal lookup table (LUT) size is non-obvious as we shall see in IV.
There are two distinct paths through the hardware design presented in Figure 1: one through the square operation and one through the LUT, since these two execute in parallel. In this work we will assume that the square path is critical and target optimized ASIC designs. Optimisations performed on one part of the design restrict the available optimisations in other parts of the design, so decision procedure tuning is important. The decision procedure used in this work is the following.

1) Minimize $k$ - minimize polynomial evaluation precision
2) Maximize square input truncation
3) Maximize linear input truncation
4) Minimize $a$, then $b$, then $c$ bitwidths

The procedure begins by minimizing $k$, which is found via Eqns. 2 & 5. We then maximise the square truncation, asking what is the maximum integer $i$, such that a valid $a(x|m − 1 : i)|² + bx + c$ exists in all regions, where $m$ is the bitwidth of $x$. Intuitively, we often think of higher order terms as correction terms, so we can tolerate some error in them, to gain performance. Such truncation is found in other approaches [6]. Only a subset of the polynomials $(a, b, c)$ for each region can tolerate the error induced by the maximal square truncation, so we discard those that cannot. We then similarly calculate maximal $j$, such that $a(x|m − 1 : i)|² + bx[m − 1 : j] + c$ is still valid, introducing further error and hence further candidates are discarded. Lastly, we minimise the precision required to represent the coefficients, $a$ then $b$ and finally $c$. For each coefficient, we have a set of valid integer values per region, which we separate into positive and negative sets (and take absolute values), then run Algorithm 1 on each set and take the minimum of the two returned precisions. With the precision of the coefficient defined we then prune the dictionary, removing any candidates that require a higher precision. From the remaining feasible polynomials we pick the first polynomial for each region.

Algorithm 1 Precision Minimization Algorithm

Require: $S = \{S_r \subseteq \mathbb{N} \mid r = 0...2^R − 1\}$
// Number of trailing zeros for each element
for $r = 0...2^R − 1$, $s \in S_r$, do
    $T_{r,s} = \max_i ((s >> i) << i = i) \triangleright$ trailing zeros
end for

$T = \min_{r < 2^R} \max_{s \in S_r} T_{r,s} \triangleright$ max valid truncation
// Calculate the optimal number of zeros to truncate
for $t = 0...T$, $r = 0...2^R − 1$ do
    $S_{t,r} = \{s \mid s \in S_r \text{ and } T_{r,s} \geq t\} \triangleright$ prune each set
    $P_{t,r} = \min_{s \in S_{t,r}} (\lceil \log_2(s + 1) \rceil − t) \triangleright$ num bits for $s$
end for

$P = \min_{t \leq T} \max_{r < 2^R} P_{t,r} \triangleright$ min precision

Alternative decision procedures were explored, such as prioritizing LUT optimisation, but this yielded inferior area-delay profiles for the generated hardware. Further optimisations such as sum of product truncation were also explored but again yielded worse hardware.

IV. RESULTS

We implemented a piecewise polynomial generating tool using PyPy 3.7. Upper and lower bounding functions are produced using Python’s math library or standard integer computations. We automatically generated Register Transfer Level (RTL) implementations of three complex functions: reciprocal, base two logarithm and base two exponential, at relevant precisions and all possible LUT height targets with an accuracy of one unit in the last place (ULP), which matches the default accuracy of FloPoCo [8] and DesignWare [12]. Hardware was generated on an Intel Xeon E3-1270 CPU and synthesised using Synopsys Design Compiler for a TSMC 7nm cell library.

For the reciprocal function, behavioural RTL producing both Round to Zero and Round to $+\infty$ can be written using only integer operations. The generated reciprocal is verified against this behaviour using Synopsys HECTOR technology, a formal equivalence checking tool. For logarithm and exponential, we verified that the hardware generated a result between our Python generated bounds using HECTOR.

Table II presents logic synthesis results for a number of fixed-point designs and compares them against the industrial state of the art, Synopsys DesignWare [12]. On average the proposed implementations improve the area-delay product by 7%. In floating point implementations of functions such as reciprocal and logarithm, the piecewise polynomial approximation is the resource intensive computation since exponent handling is comparatively cheap. These designs could easily be combined with parameterised exponent handling code to generate complete floating point architectures.

Figure 2 presents complete area-delay profiles for the competing 23 bit implementations of the reciprocal function. We note that the proposed hardware is competitive across the delay spectrum offering area improvements at several delay targets. This is respectable since Designware is not static as the architecture selected by logic synthesis varies with delay.
Fig. 3. Area-delay points at the minimum obtainable delay target for competing 10 and 16 bit implementations of the base 2 logarithm. Point labels indicate the number of lookup bits used (or DesignWare).

TABLE I
LOGIC SYNTHESIS RESULTS FOR MINIMUM OBTAINABLE DELAY TARGET COMPARING AGAINST EQUIVALENT DESIGNWARE COMPONENTS. WE SELECT THE NUMBER OF LOOKUP BITS (LUB) FOR THE PROPOSED RTL BASED ON THE BEST AREA-DELAY PRODUCT.

| Function | $x \rightarrow y$ | Num Bits | Runtime | LUB | Proposed | Area ($\mu m^2$) | Area $\times$ Delay | Delay (ns) | DesignWare | Area ($\mu m^2$) | Area $\times$ Delay |
|----------|------------------|-----------|---------|-----|----------|----------------|-------------------|-----------|-------------|----------------|-------------------|
| $0.1y = \frac{1}{1+x}$ | $10 \rightarrow 10$ | 0.5 sec | 6 (lin) | 0.125 | 43 | 5.4 | 0.143 | 79 | 11.3 |
| $0.1y = \log_2(1+x)$ | $10 \rightarrow 71$ | 0.3 sec | 6 (lin) | 0.125 | 55 | 5.4 | 0.143 | 79 | 11.3 |
| $0.1y = 2^{0.1x}$ | $10 \rightarrow 10$ | 0.6 sec | 7 (lin) | 0.190 | 69 | 191.5 | 0.275 | 176 | 70.5 |

The exponential runtime scaling discussed in [4] is apparent in these results with the 23 bit reciprocal approaching the computational limit. In practice, this is not concerning as piecewise polynomial methods are rarely used for high precision approximations.

One advantage is the ability to easily explore different LUT height architectures. Figure 3 highlights the challenge of optimising LUT height according to different metrics.

To compare against the Remez algorithm, we generated equivalent implementations using FloPoCo [8], with the results presented in Table II. FloPoCo generates narrower tables for the larger bitwidth at the expense of wider $x$ values than produced here, resulting in larger $\alpha \times x^2$ multiplication arrays. FloPoCo runs in seconds for all testcases. FloPoCo targets FPGAs, so it is not a relevant logic synthesis comparison point.

V. CONCLUSION

This paper demonstrates a method to generate the complete design space of piecewise polynomial approximations to a complex function for arbitrary accuracy specifications using the given architecture. We generated RTL approximations to the reciprocal, base two logarithm and base two exponential functions and showed that they were competitive with state of the art implementations. Knowledge of the complete design space facilitates easy re-targeting. Generating the complete design space is computationally expensive and therefore only suitable up to binary32 implementations.

Future work will investigate a decision procedure to choose the optimal number of lookup bits. Integration with MPFR would provide arbitrary precision and trusted bounds. Scalability concerns could be addressed by introducing parallelism.

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