A new type of single-phase five-level inverter

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Abstract: At present, Neutral Point Clamped (NPC) multilevel inverter is widely applied in new energy field. However, it has some disadvantages including low utilization rate of direct current (DC) voltage source and the unbalance of neutral potential. Therefore, a new single-phase five level inverter is proposed in this paper. It has two stage structure, the former stage is equivalent to three level DC/DC converter, and the back stage uses H bridge to realize inverter. Compared with the original central clamp type inverter, the new five level inverter can improve the utilization of DC voltage, and realize the neutral point potential balance with hysteresis comparator.

1 Introduction

In many new energy power generation systems, such as photovoltaic power generation, wind power generation, multi-level inverters have been used more and more widely[1,2]. Compared with the two level inverter, the multilevel inverter device has little stress and effectively improves the power level. Under the same switching frequency, the harmonic distortion is reduced and the quality of the output waveform is improved. However, in practical application, there are some problems such as low utilization of DC voltage and unbalance of neutral point potential in neutral point clamped multilevel inverters.

At present, there is a method to increase the utilization ratio of DC voltage by using three harmonic injection[3]. The space vector modulation theory can improve the DC voltage utilization to 1. The algorithm is complex. When the level is greater than 3, the switching state vector is too much, which makes it very difficult to achieve[4,5]. Moreover, the multi-target of predictive control is also used. In the penalty function, the neutral point potential is increased, and the neutral point current is reduced effectively, thus suppressing the neutral point potential imbalance[6]. All of the above methods improve the utilization of DC voltage and balance the neutral point potential from the point of view of control logic. It can’t be applied to single-phase circuits and the level is greater than 3. In this paper, a new two stage single phase five level inverter is proposed by optimizing the topology. The fore-stage three-level DC/DC circuit is adopted to improve DC voltage utilization ratio, capacitor voltage balance can be achieved via monocyclic ring or hysteresis, backward stage modulation and control strategy are simplified.

2 Topology of five-level inverter

The single-phase five-level inverter mentioned in this paper is shown in Figure 1, from which it can be seen as a two-stage circuit. Its fore-stage is a multilevel DC converter consisting of voltage source, switch tube, diode, and capacitance; its backward stage is H bridge. $C_i, C_j$ - DC side split capacitance; $V_{e1}, V_{e2}$ - DC side split capacitor voltage; $Q_i, Q_j$ - capacitance $C_i, C_j$ charge-discharge control switch; $S_i$
- three-level DC converter output level option switch, i=0, 1, 2; \( V_h \) - three level DC converter output level; 
\( H_j \)-H bridge arm switch, j=1, 2,3,4; U-H bridge output level.

There are 12 working modes for five-level inverters. When \( V_{c1}=V_{c2} \), capacitance \( C_1, C_2 \) are equivalent as DC voltage source. 12 working modes are simplified to 6 modes, see Figure 2. \( i_o \) is output current. Three working modes in positive semi-period is shown in Figure 2 (a), (b) and (c). It’s worth noting that there is only one breakover for \( S_0, S_1, S_2 \). When \( S_i \) is connected, \( V_h = i(i=0, 1, 2) \), namely, output level of DC converter is decided by \( S_i \). When \( H_1, H_4 \) are connected and \( H_2, H_3 \) are cut off, then \( U=-V_h \).

The following analysis of the five level inverter works. It is assumed that the capacitor value of the DC side capacitor \( C_1 \) and \( C_2 \) of the front circuit is equal. The capacitance voltage is \( V_{c1} \) and \( V_{c2} \) respectively. During work, \( Q_1 \) and \( Q_2 \) alternate conduction. When \( Q_1 \) is switched on, the capacitor \( C_2 \) charges. When \( Q_2 \) is switched on, the capacitor \( C_1 \) charges. If \( Q_1 \) and \( Q_2 \) are alternately switched on, the duty cycle is 0.5, then \( V_{c1} = V_{c2} = V_{in} \). Each half cycle of the inverter can be divided into ascending and descending stages. When the H bridge arm \( H_1 \) and \( H_4 \) are turned on and the \( H_2 \) and \( H_3 \) turn off, the inverter operates in the positive half cycle. Rising stage: switch tubes \( S_0, S_1 \) and \( S_2 \) are connected in turn. \( V_h \) changes from 0 to \( V_{in} \), to \( 2V_{in} \), and outputs \( U=V_h \). Descent stage: switch tube \( S_2, S_1, S_0 \) alternately conduction. \( V_h \) has changed from \( 2V_{in} \) to \( V_{in} \), to 0, and output \( U=V_h \). When the bridge arm \( H_2 \) and \( H_3 \) are turned on and the \( H_1 \) and \( H_4 \) turn off. The inverter operates in the negative half cycle. Rising stage: switch tubes \( S_0, S_1 \) and \( S_2 \) are connected in turn. \( V_h \) changes from 0 to \( V_{in} \), to \( 2V_{in} \), and outputs \( U=-V_h \). Descent stage: switch tubes \( S_2, S_1 \) and \( S_0 \) are sequentially connected. \( V_h \) has changed from \( 2V_{in} \) to \( V_{in} \) to 0 and output \( U=-V_h \).

To sum up, \( V_{c1} \) and \( V_{c2} \) are decided by connection time of \( Q_1 \) and \( Q_2 \). The output level of three-level DC converter is decided by switch tube \( S_i \). The frequency and initial phase of inverter output waveform are controlled by switch tube \( H_j, Q_1, Q_2 \) and \( S_i, H_j \) are separated for independent control. The frequency and phase of \( S_i \) and \( H_j \) need to be synchronized.
3 Simulation experiment model

In this paper, carrier cascaded technology is used to modulate the single-phase five level inverter. The coordinate plane is divided into 5 regions using four carriers. The modulation wave is compared with the four carrier wave. From bottom to top corresponds to five levels of -2, -1, 0, +1 and +2. Use this method to obtain the PWM wave needed to control the switch tube. At the same time, a hysteresis comparison module is used to achieve neutral point potential balance. When the DC side split capacitor C1 and C2 capacitor voltage imbalance occurs, through real-time acquisition and comparison of Vc1, Vc2. The neutral point potential balance can be achieved by comparing the results of the next cycle Q1 and Q2 turn-on time allocation ratio.

By using carrier stack modulation strategy, a MATLAB/Simulink single-phase five level inverter simulation platform is built, in which inductance is 1.5 mH, capacitance is 25 uF, resistance is 25, and carrier frequency is 10 kHz. The following output waveforms can be obtained:
Fig. 3 is a closed loop output waveform with an output voltage of 200 V. As can be seen from Figure 3, the inverter output waveform distortion rate is low, and the inverter effect is better. Figure 4 (a) and (b) are the capacitor voltage balancing processes at $V_{c1}=180$ V, $V_{c2}=220$ V, $V_{c1}=220$ V, $V_{c2}=180$ V. In the case of two unbalanced voltages, the capacitor C1 and C2 achieve voltage balancing after 3ms and 6ms respectively. Therefore, the new five level inverter has good working effect.

4 Conclusion
A single-phase five-level inverter is proposed in the present paper. Compared with the conventional clamping multilevel inverters, the new five level inverter improves the utilization of DC voltage and achieves the neutral point potential balance. In this paper, the topology of the inverter is described in detail, and the working state of each switch tube in the operation process is described. A model is built to simulate the effect of the inverter, which shows that the new inverter proposed in this paper has good performance.

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