Accelerating Monte-Carlo Tree Search on CPU-FPGA Heterogeneous Platform

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Abstract—Monte Carlo Tree Search (MCTS) methods have achieved great success in many Artificial Intelligence (AI) benchmarks. The in-tree operations become a critical performance bottleneck in realizing parallel MCTS on CPUs. In this work, we develop a scalable CPU-FPGA system for Tree-Parallel MCTS. We propose a novel decomposition and mapping of MCTS data structure and computation onto CPU and FPGA to reduce communication and coordination. High scalability of our system is achieved by encapsulating in-tree operations in an SRAM-based FPGA accelerator. To lower the high data access latency and inter-worker synchronization overheads, we develop several hardware optimizations. We show that by using our accelerator, we obtain up to 35× speedup for in-tree operations, and 3× higher overall system throughput. Our CPU-FPGA system also achieves superior scalability w.r.t number of parallel workers than state-of-the-art parallel MCTS implementations on CPU.

Index Terms—Artificial Intelligence, MCTS, FPGA

I. INTRODUCTION

Monte Carlo Tree Search (MCTS) is a planning algorithm that combines a best-first search tree with random simulations in order to find optimal decisions in a system. MCTS methods have shown a massive potential due to their success in situations where deterministic algorithms fail to deliver optimal solutions in a reasonable amount of time, especially when applied in domains with extremely vast search space. For example, it is applied in many Artificial Intelligence (AI) benchmarks such as Constraint Satisfaction Problems [1], Computer Games [2], and Neural-Architecture Search [3].

MCTS manages a tree as the policy to guide an agent towards an optimal decision. The tree is dynamically constructed by collecting statistics through simulations. These statistics are used to update the tree. Recent advances in MCTS parallelization have shown that using multiple workers, simulations can be embarrassingly parallelized without increasing the total simulation cost to achieve the same domain performance as sequential MCTS [4]. Additionally, deep neural network (DNN) has been used to replace time-consuming simulation with DNN inference [2]. The bottleneck for large-scale parallel MCTS system shifts from simulations to in-tree operations. However, it is challenging to efficiently accelerate in-tree operations on multi-core CPUs because (1) intrinsic dependencies between workers operating on a shared tree lead to large thread-level synchronization overheads, and (2) in-tree operations have low-arithmetic intensity and incur high-latency memory access overhead.

In this work, we define the first CPU-FPGA system for general parallel MCTS. Unlike existing FPGA implementations that focus on accelerating application-specific simulations [5], [6], our system’s generality is in the flexibility of the accelerator to interface with the software simulations for various applications on the CPU. The major contributions are:

- We propose a novel decomposition of the MCTS decision tree into two separate data structures, State Table (ST) and Upper Confidence-bounded Tree (UCT). We show that this reduces the PCIe data traffic and memory requirement on the FPGA.
- We map the UCT onto the FPGA and develop an SRAM-based accelerator for in-tree operations with optimizations specialized for MCTS, including:
  1) A hardware design that exploits both data- and pipeline-parallelism for in-tree operations.
  2) Tree partitioning and mapping to SRAM banks to eliminate bank conflicts in in-tree operations.
- We provide an efficient CPU-FPGA interface for coordinating communication with the accelerator and synchronizations among the CPU threads in Tree-Parallel MCTS.
- We replace the CPU process for in-tree operations with the FPGA accelerator in two state-of-the-art parallel MCTS implementations. This leads to up to 35× speedup for in-tree operations, and our system achieves up to 3× higher throughput than the CPU-only implementation.

II. BACKGROUND

A. Sequential Monte-Carlo Tree Search

Monte Carlo Tree Search (MCTS) is a model-based Reinforcement Learning algorithm performed by an agent that explores a global environment, and plans the best action at each time step by constructing a tree using one or multiple workers [7]. The tree is built using simulations on copies of the global environment called local environments. In the search tree, each node \( s \) represents a visited state, its adjacent edge \( (s, \hat{s}) \) denotes an action taken at that state, and its child node \( \hat{s} \) denotes the state it transits to after taking the action. Fig. 1 shows the phases conducted by a worker. The Selection phase traverses the existing search tree by iteratively choosing one child node at each tree level according to Eq. 1 [8] (a leaf node is a node whose child nodes \( \hat{s} \) have not been all expanded):

\[
s \leftarrow \arg \max_{\hat{s} \in \text{Children}(s)} \{ uct(s, \hat{s}) \} = \arg \max_{\hat{s}} \left( V_{\hat{s}} + \beta \sqrt{\frac{\ln N_{\hat{s}}}{N_s}} \right) \tag{1}
\]

where \( V_{\hat{s}} \) is the average expected utility value (i.e., reward) that can be received through \( \hat{s} \), and \( N_{\hat{s}} \) (\( N_s \)) denotes the
Fig. 1: MCTS procedure. An MCTS iteration is defined as one round of Selection-Expansion-Simulation-BackUp by one (or multiple) worker(s). An MCTS step is the entire process that, after the number of tree nodes reaches a limit $X$, the agent takes one step in the global environment and flushes the tree.

number of times the nodes $s$ has been visited. $uct(s, \hat{s})$ is the weight of the edge $(s, \hat{s})$, $\beta$ is a parameter controlling the tradeoff between exploitation (first term) and exploration (second term). When leaf node $s$ is selected, the Expansion phase chooses a new (un-expanded) edge $(s, s')$, runs local environment 1-step simulation from the state of $s$ to reach a new state, and inserts a newly expanded child node, $s'$ that represents the new state. The Simulation phase runs local environment simulation from $s'$, and returns a reward $V$. Note that this can be done either using a simulation software that runs until termination [7], or via a DNN inference that approximates the expected $V$ [2], [9]. Finally, the BackUp phase uses the received $V$ to update the $V_s$ term of $uct$ for all the traversed edges during Selection. In practice, the above phases are repeated until a resource budget $X$ (the maximum number of nodes maintained by the tree) is reached [7]. Afterwards, the agent takes a step in the global environment by choosing the best action (based on Eq. 1) at the root, and the best child becomes the new root while the rest of the tree are flushed (i.e., no longer accessed by in-tree operations in future MCTS steps). We call this a Tree Flush (Fig. 1).

B. Tree-Parallel MCTS

There are many approaches to parallelize MCTS (Sec. VI-A). The most popular method among them is the Tree-Parallel MCTS, because it can scale to larger number of workers without increasing the total simulation cost for achieving certain reward [4]. In Tree-Parallel MCTS, after a worker traverses a certain path during Selection, a virtual loss $VL$ is subtracted from $uct$ of selected edges to lower their weights, thus encouraging other workers to take different paths. It also creates dependencies between workers during the Selection phase. $VL$ is recovered later in the BackUp phase. Note that $VL$ can either be a pre-defined constant value [10], or a number tracking visit counts of child nodes [4].

In Tree-Parallel MCTS, we refer to in-tree operations as all the operations that access the tree in Selection, Expansion and BackUp phases. They are defined in Algorithm 1.

C. Motivation and Objective

A typical Tree-Parallel MCTS system is composed of a master process coordinating the in-tree operations for all workers, and multiple simulation processes (threads) responsible for independent Simulations [4]. Although Tree-Parallel MCTS enables high-throughput simulation that is scalable to larger number of workers, the in-tree operations (especially Selection) become the bottleneck. We profile the execution time breakdown of two implementations: a) parallel MCTS for Atari games [4] using OpenAI-gym simulation software, and b) parallel implementation of MCTS for Gomoku game using DNN-based simulation [9] on a CPU. We observed that the Selection and BackUp total latency in an MCTS iteration grows from 10% (8 workers) to 40% (128 workers) for a), and 38% (2 workers) to 70% (32 workers) for b). Such bottleneck is hard to eliminate on a multi-core CPU even with one thread per worker for Selection, because the expensive thread-level synchronizations are needed to resolve dependencies between workers due to race conditions. As shown in Algorithm 1, lines 4-5 (line 15) is the RAW (WAW) critical region that protect the shared tree to be only accessed by a single thread at any time. This essentially serializes Selection by different workers by a synchronization interval, $T_{sync}$. $T_{sync}$ on CPU involves the sequential process where the same shared tree in DRAM is read by a thread after written by another thread. This incurs high memory access latency (i.e., $T_{sync} \geq 2 \times T_{mem}$, where $T_{mem}$ is the tree data access latency. Typical $T_{mem} > 100$ CPU cycles [11]). As a result, the system throughput is constrained by the latency of the Selection phase.

Motivated by the above observations, in this work, we aim to alleviate the bottleneck in Tree-Parallel MCTS system by developing a SRAM-based accelerator. We (1) utilize the FPGA SRAM capacity and bandwidth to minimize $T_{mem}$ to a single FPGA cycle; and (2) exploit deep pipelining that minimizes the interval $T_{sync}$ such that the system throughput on a typical CPU-FPGA platform can be scaled to more workers without being bounded by the Selection phase.

Algorithm 1 In-tree Operations for a single worker in Tree-Parallel MCTS

1: procedure SELECTION
2: $s \leftarrow \text{root}$, $i = 1$
3: while $s$ is not leaf and tree level $i \in [1, D]$ do
4: $\hat{s} \leftarrow \text{RHS of Eq. 1}$; \hspace{1em} $\triangleright$ Read $uct$ from tree level $i$
5: $uct(s, \hat{s}) \leftarrow VL$; \hspace{1em} $\triangleright$ Apply $VL$: Write to tree level $i$
6: $E_i[i] \leftarrow (s, \hat{s})$; $s \leftarrow \hat{s}$, $i = i + 1$
7: return $F_{\text{it}}, s$

8: procedure EXPANSION($s$)
9: send state($s$) to Simulation process;
10: send unexpanded action($s, s'$) to Simulation process;
11: receive state($s'$) from Simulation process;
12: tree.InsertNode($s'$), InsertEdge($s, s'$);
13: procedure BACKUP($E_i$)
14: receive reward $V$ from Simulation process;
15: for tree level $i \in [1, D]$ do
16: tree.UpdateEdge($V, VL, uct(E_i[i]))$; $\triangleright$ Update tree nodes

Note: $D$ is the tree height limit. $E_i$ and $s$ denote the traversed edges and selected leaf node in the Selection phase. $s'$ denotes the node to be expanded. $state(s)$ denotes the application-specific environment state represented by node $s$. $VL$ is the virtual loss. Lines with highlighted comments are the critical regions that create RAW (WAW) dependencies between pair of workers.
III. System Design

We consider a CPU-FPGA heterogeneous platform interconnected by PCIe interface. We map the Simulation phase (and the 1-step simulation for the Expansion phase) of $p$ workers onto $p$ CPU Simulation threads. We map the in-tree operations by all the workers onto the FPGA.

A. Memory component decomposition and mapping

The tree in MCTS stores the nodes, weighted edges and application-specific environment states represented by all the leaf nodes. The size of the tree is thus $O(X\gamma)$, where $X$ is the number of tree nodes, and $\gamma$ is the memory requirement for storing a simulation environment state. Simply storing the entire tree on the FPGA device results in $O(rp\gamma)$ PCIe data traffic during the Expansion phase, as shown in Algorithm 1 lines 8,10. To alleviate the memory burden on the FPGA accelerator and reduce the PCIe traffic, we decompose the tree into two memory components: Upper Confidence-Bound Tree (UCT) and State Table (ST). The UCT maintains the node and edge information in the tree except the environment states. The ST is implemented as a table with $X$ entries, where the index of each entry is a unique node index maintained in the UCT, and the value is an application-specific environment state represented by that node. The UCT is stored on the FPGA and the ST is stored in the CPU DRAM. Accordingly, the 1-step simulation for the Expansion phase) of the UCT is stored on the FPGA SRAM with tens of megabytes capacity.

As shown in Fig. 2, we define a shared Send buffer of size $p$ to store rewards $V$ produced by Simulation threads. Its data is migrated to the FPGA after barrier synchronization of all the threads. After the Selection and Node Insertion on FPGA are completed, node indices $s,s'$ are written into a Receive buffer where each entry can be independently accessed by a thread. We define a constrained communication rule for the BSP: each thread $j \in [1..p]$ must access the same index $j$ of the Receive buffer and the Send buffer. Similarly, each worker on FPGA also access the same unique index of the Receive buffer and the Send buffer. This ensures the correct matching between $V$ and traversed $E_t$ of each worker in the BackUp phase (Algorithm 1).

CPU Data Concurrency: The parallel program for each CPU thread is shown in Algorithm 2. Note that concurrent accesses to ST during State Insertion do not require any thread-level synchronization, because MCTS guarantee all workers expand different nodes $s'$, and any expanded $s'$ are different from any selected node $s$. This means all the threads write into different ST entries (Algorithm 2 line 5), and no ST read (Algorithm 2 line 3) depends on the ST write of any other thread. Therefore, ST operations will not become the bottleneck in system throughput when increasing $p$.

Correctness of System Execution: Consider a baseline CPU program for $p$-worker in-tree operations (Algorithm 1). Our CPU-FPGA system yields the exact same outputs as that of a CPU-only system. We prove this from two aspects: The FPGA acceleration avoids any race conditions in BackUp, Selection and Expansion phases. First, the 3 phases by all workers are performed in sequence to avoid data race between workers in different phases. Second, the key concept of FPGA acceleration is to utilize a pipeline where each stage only access a particular UCT level. The pipeline avoids any RAW (Selection, Expansion) and WAW (BackUp) race conditions between workers by ensuring only one worker is processed in a stage at any time.

IV. ACCELERATOR IMPLEMENTATION

A. Accelerator Overview

The overview of the accelerator is depicted in Fig. 3. The accelerator is composed of a worker distributor using the root level information to assign workers to different pipelines, and $n$ pipelines working on strictly separate subtrees. Given the tree fanout $F$, and the number of workers $p$, we allocate pipelines that support concurrency of up to $F$ sub-trees and avoid hardware under-utilization. Thus, we set

Algorithm 2 An MCTS Iteration on thread $j \in [1,p]$

1: $s,s' \leftarrow$ Selection and Node Insertion using FPGA;
2: Receive buffer[$j$] $\leftarrow$ s, $s'$; $\triangleright$ PCIe O($p$)
3: state($s$) $\leftarrow$ ST[$s$]; $\triangleright$ Concurrent read ST
4: simulate 1 step with initial state($s$), initial action($s',s'$);
5: ST[$s'$] $\leftarrow$state($s'$); $\triangleright$ State Insertion, Concurrent write ST
6: $V_j \leftarrow$ Simulation phase from state($s'$) until termination;
7: Send buffer[$j$] $\leftarrow$ $V_j$; $\triangleright$ PCIe O($p$)
8: barrier synchronization;
9: migrate $V$ from the Send buffer to FPGA; $\triangleright$ PCie O($p$)
10: BackUp using FPGA;

Fig. 2: System Diagram and Interface

Expansion phase of a worker is decomposed into two parts: Node Insertion to UCT and State Insertion to ST. All the in-tree operations operating on the UCT in Selection, Node Insertion and BackUp are accelerated by the FPGA. The interactions with respect to ST (CPU) and UCT (FPGA) are further explained in Sec. III-B. This decomposition reduces the PCIe traffic to $O(p\gamma)$ by eliminating the need to communicate large simulation states between CPU and FPGA during Expansion (only node indices need to be transferred in lines 8, 10 of Algorithm 1). Additionally, the memory requirement on the FPGA is reduced since the UCT only requires $O(X)$ memory. For typical MCTS game benchmarks (e.g. Atari games and board game benchmarks [4],[9]), $X$ ranges from $1K−100K$. This means that the entire UCT can typically be stored on the FPGA SRAM with tens of megabytes capacity.

B. Tree-Parallel MCTS: Bulk Synchronous Processing

The CPU-FPGA system execution model is shown in Fig. 2. It can be viewed as a Bulk Synchronous Process (BSP) with constrained communication at the end of each iteration.

CPU-FPGA Interface and Constrained Communication: As shown in Fig. 2, we define a shared Send buffer of size $p$
n = min(p, F). As motivated in Sec. II, The key objectives of the accelerator design are to support low data access latency $T_{mem}$ (Sec. IV-B), and minimize both the intra-pipeline $T_{sync}$ (Sec. IV-C) and inter-pipeline $T_{sync}$ (Sec. IV-D).

B. Minimizing $T_{mem}$.

We adopt a compact adjacency list data structure to store the UCT in on-chip memory banks. Each node entry in a memory bank is a node index followed by all of its adjacent edge information (edge weights and child node indices). The UCT is partitioned and mapped to the FPGA SRAM. The Root Level Memory Bank stores a single root node entry with fully partitioned adjacency edge array. To support both data parallelism across pipelines, we partition the UCT into n subtrees rooted at different child node(s) of the root (each stored in a Sub-Tree Memory Bank Group). To support stage parallelism within a pipeline, for each sub-tree, we partition node entries by UCT levels (different levels are stored in separate banks). At compile time, we statically allocate SRAM banks with the capacities to store a full-F-ary UCT with height $D$ that can store number of nodes $> X$, where $X$ is the maximum number of tree nodes. These techniques guarantee no bank conflicts occur between workers, and ensure single-cycle accesses to the UCT by all the workers.

C. Minimizing Intra-Pipeline $T_{sync}$.

Each stage of the Sub-Tree Selection Pipeline involves a 2-input comparator that loops over $F$ adjacent edges sequentially. HLS-generated floating point comparator takes multiple cycles to compute $\hat{s}$ in 1 cycle for arbitrary $F$. Specifically, to obtain the maximum of $F$ edge weights, we assign $C_{v}^{F} = \binom{F}{2}!2!$ comparators, each compares a unique pair of edge weights, and outputs a 1-bit result of comparison. The concatenation of these results (a $C_{v}^{F}$-bit number) is used to index a Comparison Look-Up Table (CLUT) that outputs the best child index $\hat{s}$ (Eq. 1). The CLUT output $\hat{s}$ is connected to a 1-to-$n$ crossbar to distribute the worker to one of $n$ pipelines. The size of a CLUT is $2^{C_{v}^{F}}$ entries to cover all the possible permutations in $F$ edge weights. To constrain the CLUT size for large fanout $F$, we develop multi-level hierarchy of smaller CLUTs. For example, when $F = 20$, we distribute the edge weights to 5 CLUTs, each CLUT has $f = 4$. The results of these 5 CLUTs in the first level are passed to the next level with a $f = 5$ CLUT to output the maximum of 20 edge weights and the associated child index. This design allows 1-cycle response to any changes in $F$ edge weights. By consuming additional comparators and memory only in the Root Level (Worker Distributor), we allow concurrent execution of workers to operate on the same UCT level in different pipelines. We thus minimized inter-pipeline $T_{sync}$ to be constantly 2 cycles (1 cycle for comparison, 1 cycle for $VL$ update at the root) when a single CLUT is used.

D. Minimizing Inter-Pipeline $T_{sync}$.

The root-level Worker Distributor assigns incoming workers to different Sub-Tree Selection Pipelines based on the maximum of $F$ edge weights at the root. To fully exploit the data parallelism provided by multiple pipelines, the Worker Distributor needs to process workers with minimized interval (i.e., we need inter-pipeline $T_{sync} <$ intra-pipeline $T_{sync}$). Therefore, we design the Worker Distributor to compute $\hat{E} = eq.$ in 1 cycle for arbitrary $F$. Specifically, to obtain the maximum of $F$ edge weights, we assign $C_{v}^{F} = \binom{F}{2}!2!$ comparators, each compares a unique pair of edge weights, and outputs a 1-bit result of comparison. The concatenation of these results (a $C_{v}^{F}$-bit number) is used to index a Comparison Look-Up Table (CLUT) that outputs the best child index $\hat{s}$ (Eq. 1). The CLUT output $\hat{s}$ is connected to a 1-to-$n$ crossbar to distribute the worker to one of $n$ pipelines. The size of a CLUT is $2^{C_{v}^{F}}$ entries to cover all the possible permutations in $F$ edge weights. To constrain the CLUT size for large fanout $F$, we develop multi-level hierarchy of smaller CLUTs. For example, when $F = 20$, we distribute the edge weights to 5 CLUTs, each CLUT has $f = 4$. The results of these 5 CLUTs in the first level are passed to the next level with a $f = 5$ CLUT to output the maximum of 20 edge weights and the associated child index. This design allows 1-cycle response to any changes in $F$ edge weights. By consuming additional comparators and memory only in the Root Level (Worker Distributor), we allow concurrent execution of workers to operate on the same UCT level in different pipelines. We thus minimized inter-pipeline $T_{sync}$ to be constantly 2 cycles (1 cycle for comparison, 1 cycle for $VL$ update at the root) when a single CLUT is used.

E. Other modules and optimizations

Memoization: To eliminate the $O(D)$ overhead of sequentially back-tracing from leaf to node in BackUp, a BackUp Memoization Buffer with size of $D - 1$ words is associated with each worker to memorize the node entries to be updated in BackUp during Selection. Thus for each worker, BackUp can be completed in 2 cycles.

Node Insertion and Tree Flush: A node insertion is performed by directly writing into the SRAM location of the expanded leaf node returned by the pipeline, after the Selection phase for all the workers are completed. Insertions in different
pipelines work concurrently. Upon Tree Flush, We clear the counters for tracking expanded child nodes for all node entries, and update the Root Level Memory bank using the new root information. At the same time, the corresponding entries in ST is also deleted on the CPU.

In summary, the hardware optimizations described in this section make the FPGA in-tree accelerator scale to larger number of workers compared with multi-core CPUs by greatly reducing $T_{\text{sync}}$ - we are able to achieve $T_{\text{mem}} = 1$ cycle, inter-pipeline $T_{\text{sync}} = 2$ cycles for any fanout $F$ that can be contained using a single CLUT, and intra-pipeline $T_{\text{sync}} = F + 1$ cycles.

V. EVALUATION

The objectives of our work are to achieve low latency in-tree operations in Tree-Parallel MCTS, and improve the scalability of the system throughput to larger number of workers. We first evaluate our optimizations for in-tree operations, and compare them to their baseline performance on a CPU master process (Sec. V-B). We then analyze the throughput and scalability of the CPU-FPGA system, and compare with CPU-only baselines (Sec. V-C).

A. Experimental Setup

Benchmark environments: We choose two widely-used game benchmarks for MCTS: the Atari game Pong [4], and the board game Gomoku [9]. For the Atari game, both the Simulation phase and the 1-step simulation for the Expansion phase use OpenAI-gym library. Its action space (i.e., fanout $F$ of the tree) is 6, tree height limit $D$ is 9, and the maximum number of tree nodes $X$ is 56K. For Gomoku, in each worker, the Expansion phase expands all $F$ (instead of one) child nodes of each selected node, and the Simulation phase is a DNN inference that takes a board state as the input and outputs the utilities (expected rewards) for all its child nodes. The DNN is trained with a Gomoku simulation program [9]. The 1-step simulation for Expansion phase also uses the simulation program. We set 6x6 board ($F = 36$), $D = 5$, and use $X = 48K$. The choice of $D$ and $X$ in both benchmarks are the same as those in existing CPU implementations.

Platforms: Our CPU baseline experiments are conducted on an Intel(R) Xeon(R) Gold 5120 server with 2 sockets (56 hardware threads in total) at 2.2GHz, and 19MB L3 cache. The CPU-FPGA platform consists of the same CPU and a Xilinx Alveo U200 board [13] connected by PCIe gen4x16. In all the experiments, $p$ denotes both the number of workers and the total number of CPU software Simulation threads. We use one Simulation thread per worker. For Gomoku, $p$ ranges from 2 to 128. For Pong, the OpenAI-gym simulation time for $p < 8$ is greater than 99% of an MCTS iteration time, the advantage of using FPGA when $p < 8$ is marginal. So, we show results for larger $p$ that ranges from 8 to 128.

Accelerator specifications: We develop a parameterized FPGA kernel template using High-Level Synthesis (HLS) for quick customization. We follow VITIS development flow [14] for bitstream generation. The design achieves 200MHz frequency. OpenCL is used to implement the data transfer between the CPU and FPGA. The resource utilization of our accelerator for both benchmarks obtained at the largest $p$ are shown in Table I.

B. Evaluation of In-Tree Operations

Fig. 4 shows the total latency of in-tree operations in BackUp, Selection and Expansion phases in one MCTS iteration for various number of workers. The reported in-tree operations latency is the average over all the iterations in an MCTS step. For the measurement on our CPU-FPGA system, apart from the FPGA kernel latency, we also include both the PCIe transfer time before Simulation and after BackUp, and the additional ST operations executed on CPU for Expansion. The PCIe data transfer time is obtained using Xilinx Run-time (XRT) Profiler [15]. For a given benchmark, the FPGA kernel performing in-tree operations on the UCT always has lower latency than CPU. Also, for a given $p$, in-tree operations for Gomoku take longer than that for Pong on CPU, this is because larger $F$ lead to higher $T_{\text{sync}}$ in Selection. We point out that the impact of $F$ on Selection latency on the FPGA is smaller, because we optimized $T_{\text{sync}}$ between workers to be as low as 2 (3) FPGA cycles for $F = 6$ ($F = 36$). As a result, the latency of FPGA kernel for in-tree operations scale well wrt both $F$ and $p$. The PCIe overhead increases very little as $p$ increases, because the reduced PCIe data transfer only takes negligible amount of time compared to the fixed PCIe initiation latency ($\sim 0.04$ ms). The tradeoff for lower PCIe data traffic is the

![Table I: FPGA Resource Utilization](image)

**TABLE I: FPGA Resource Utilization**

| Benchmark | SRAM | DSP | LUT | FF |
|-----------|------|-----|-----|----|
| Atari-Pong | 24 MB | 123 | 118K | 160K |
| (p = 128, n = 6) | (69%) | (2%) | (14%) | (9%) |
| Gomoku | 16 MB | 465 | 308K | 608K |
| (p = 128, n = 56) | (46%) | (7%) | (36%) | (34%) |

Note: For the Worker Distributor, we use a CLUT with $f = 6$ for Pong. We use 2 levels of CLUTs, each with $f = 6$ for Gomoku.

![Fig. 4: Latency of the in-tree operations. Y-axes are in log scale for better breakdown visualization.](image)
additional accesses to ST. The ST operations involve reading or writing 256 (432) bytes representation of environment state for Pong (Gomoku). The ST operation latency does not incur thread-level synchronization overheads and also scales well to increasing \( p \). Overall, we observe a range of 6 to \( 35 \times \) speedup for in-tree operations.

C. Evaluation of System Performance

The **System Throughput** is defined as the number of simulation requests processed per second. A simulation request refers to one local-environment simulation (or batch-1 DNN inference) by a single worker in an MCTS iteration. Fig. 5 shows the system throughput of the two benchmarks for various \( p \). The CPU-only system throughput improvement cannot linearly scale up with increasing \( p \) because the increasing latency of in-tree operations becomes the bottleneck. The proposed FPGA acceleration alleviates this bottleneck by reducing \( T_{\text{sync}} \) between workers and improves the system scalability. Note that the system throughput stops increasing after \( p > 56 \) because there are only 56 hardware CPU threads. Note that the speedup using FPGA will further increase if more parallelism were enabled for simulation. Higher system throughput improvements from CPU-FPGA system are consistently observed for larger \( p \), because when \( p \) increases, fewer MCTS iterations are needed to reach \( X \) tree nodes in an MCTS step, the total simulation time decreases, while the total in-tree operations time on CPU does not drop significantly such that its bottleneck becomes more significant. For the Gomoku benchmark, for large \( p \), the gap between ideal speedup and actual throughput on the CPU is especially big because the latency of largely sequential in-tree operations exceeds that of the Simulation phase (parallel DNN inference). Our system closed such gap by realizing low-latency in-tree operations, thus improved the scalability to larger \( p \) in both benchmarks. Overall, we obtain up to \( 1.59 \times \) and \( 3.02 \times \) higher throughput for the two benchmarks than the CPU-only baselines.

VI. RELATED WORK

A. MCTS Parallelization

In addition to Tree-Parallel MCTS, other algorithms have been developed to parallelize MCTS. The objective is to speedup each MCTS step while reducing the negative impact on algorithm performance (algorithm performance is measured by achievable reward using a fixed total number of simulations). Popular parallelization approaches include Leaf-Parallel MCTS (LeafP) [16] that parallelizes simulations at the same leaf node, and Root-Parallel MCTS (RootP) [17] that create multiple trees at different workers and aggregates their statistics of the subtrees before all the workers complete an MCTS step. [18], [19] proposed block parallelism - a combination of leafP and rootP for GPU acceleration. Recent work WU-UCT [4] proposes a variant of Tree-Parallel MCTS (TreeP), and shows that it maintains superior algorithm performance compared with the other parallelization approaches. In this work, we target TreeP because of its superior algorithm performance. The difference in variants of Tree-Parallel MCTS is in how the virtual loss \( VL \) is computed: it can be a value proportional to the number of visits to child nodes as proposed in [4], or a constant [10]. Note that our accelerator design can support both these variants by a simple modification to the Sub-Tree Selection pipelines.

B. Hardware-Accelerated MCTS

There is limited work in hardware acceleration of MCTS. [5], [6] design Blokus Duo Game solvers on FPGA that uses MCTS. Their accelerators target Blokus Duo game only and implement the simulator circuit on FPGA. Different from their work, our objective is to develop a general system for MCTS by keeping software simulations on the CPU.

VII. CONCLUSION & FUTURE WORK

In this work, we proposed the first CPU-FPGA system design for accelerating Tree-Parallel MCTS that is portable to various applications. Our system achieved higher throughput and better scalability to larger number of parallel workers than state-of-the-art CPU-only implementations. Parallel MCTS also lead to many further opportunities for efficient acceleration. For example, our accelerator design poses a limit on the supported tree height since it allocates SRAM banks for the full tree. In the future, runtime dynamic SRAM bank management methodologies can be explored to better support arbitrary-shaped tree growth. Additionally, new algorithmic optimizations can be explored to reduce data race between workers in TreeP and enable higher data parallelism.

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REFERENCES

[1] B. Satomi, Y. Joe, A. Iwasaki, and M. Yokoo, “Real-time solving of quantified csp based on monte-carlo game tree search,” in Twenty-Second International Joint Conference on Artificial Intelligence, 2011.

[2] J. Schrittwieser, J. Antonoglou, T. Hubert, K. Simonyan, L. Sifre, S. Schmitt, A. Guez, E. Lockhart, D. Hassabis, T. Graepel et al., “Mastering atari, go, chess and shogi by planning with a learned model,” Nature, vol. 588, no. 7839, pp. 604–609, 2020.

[3] L. Wang, Y. Zhao, Y. Jinnai, Y. Tian, and R. Fonseca, “Neural architecture search using deep neural networks and monte carlo tree search,” in Proceedings of the AAAI Conference on Artificial Intelligence, vol. 34, no. 06, 2020, pp. 9983–9991.

[4] A. Liu, J. Chen, M. Yu, Y. Zhai, X. Zhou, and J. Liu, “Watch the unobserved: A simple approach to parallelizing monte carlo tree search,” in International Conference on Learning Representations, 2020. [Online]. Available: https://openreview.net/forum?id=BJQdJSKDB

[5] A. Jahanshahi, M. K. Taram, and N. Eskandari, “Blokus duo game on fpga,” in The 17th CSI International Symposium on Computer Architecture & Digital Systems (CADS 2013). IEEE, 2013, pp. 149–152.

[6] E. Qasemi, A. Samadi, M. H. Shadmehr, B. Azizian, S. Mozaffari, A. Shirian, and B. Alizadeh, “Highly scalable, shared-memory, monte-carlo tree search based blokus duo solver on fpga,” in 2014 International Conference on Field-Programmable Technology (FPT). IEEE, 2014, pp. 370–373.

[7] C. B. Browne, E. Powley, D. Whitehouse, S. M. Lucas, P. I. Cowling, P. Rohlfshagen, S. Tavener, D. Perez, S. Samothrakis, and S. Colton, “A survey of monte carlo tree search methods,” IEEE Transactions on Computational Intelligence and AI in games, vol. 4, no. 1, pp. 1–43, 2012.

[8] L. Kocsis and C. Szepesvári, “Bandit based monte-carlo planning,” in European conference on machine learning. Springer, 2006, pp. 282–293.

[9] J. Song, “Alphazero agent for solving gomoku.” [Online]. Available: https://github.com/junxiaosong/AlphaZeroGomoku

[10] G. M.-B. Chaslot, M. H. Winands, and H. Herik, “Parallel monte-carlo tree search,” in International Conference on Computers and Games. Springer, 2008, pp. 60–71.

[11] Intel. (2018) Skylake specification. [Online]. Available: https://www.7-cpu.com/cpu/Skylake.html

[12] J. de Fine Licht, M. Besta, S. Meierhans, and T. Hoefler, “Transformations of high-level synthesis codes for high-performance computing,” IEEE Transactions on Parallel and Distributed Systems, vol. 32, no. 5, pp. 1014–1029, 2020.

[13] Xilinx, “Alveo u250 data center accelerator card.” [Online]. Available: https://www.xilinx.com/products/boards-and-kits/alveo/u250.html

[14] V. Kathail, “Xilinx vitis unified software platform,” in Proceedings of the 2020 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, 2020, pp. 173–174.

[15] A. Xilinx. (2022) Xrt profiling. [Online]. Available: https://docs.xilinx.com/r/en-US/tg1393-vitis-application-acceleration/Profiling-the-Application

[16] T. Cazenave and N. Jouandeau, “On the parallelization of uct,” in Computer games workshop, 2007.

[17] H. Kato and I. Takeuchi, “Parallel monte-carlo tree search with simulation servers,” in 2010 International Conference on Technologies and Applications of Artificial Intelligence. IEEE, 2010, pp. 491–498.

[18] K. Rocki and R. Suda, “Parallel monte carlo tree search on gpus,” in Eleventh Scandinavian Conference on Artificial Intelligence. IOS Press, 2011, pp. 80–89.

[19] N. A. Barriga, M. Stanescu, and M. Buro, “Parallel uct search on gpus,” in 2014 IEEE Conference on Computational Intelligence and Games. IEEE, 2014, pp. 1–7.