Digital Control of Photovoltaic based Multilevel Converter for Improved Harmonic Performance

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Abstract

Objectives: In the last two decades, various control algorithms have been proposed for several multilevel converter topologies each having their pros and cons compared with improvement in harmonic performance and efficiency. The multicarrier modulation strategy seems to be the most common thread for multilevel topologies. Methods/Statistical Analysis: The harmonic observations for phase shifted and phase disposition multicarrier strategy is different for cascaded and neutral point clamped topologies. The exemplification of mathematical analysis and hardware in loop results with Nexys 4 FPGA digital controller with Xilinx and MATLAB/Simulink for digital control modulation of Marx multilevel inverter for photovoltaic application is discussed. Findings: The balanced charging and discharging of the capacitor will lead to less leakage current, further reducing the health hazards to the working personals in the region. The analysis and implementation of the most suitable carrier based control strategy technique show superiority over the harmonic content for different techniques for the aforementioned topology. The hardware results show the similarity with the simulated version with comparison with pre-existing topologies. Application/Improvements: The paper discusses the application with real-time hardware photovoltaic implementation of self-boost capable Marx multilevel inverter with an added advantage of equalization with capacitor charge. An improved total harmonic distortion evaluation with preexisting topologies is presented.

Keywords: Field Programmable Gate Array (FPGA), Multilevel Inverters (MLI), Photovoltaic System (PVS), Total Harmonic Distortion (THD), Xilinx System Generator (XSG)

1. Introduction

Multilevel inverters find its application majorly in DC-AC energy conversion for medium and high energy applications. The word multilevel represents; the many levels of voltage are existent in desired producing waveform. As discussed in, the output voltage signal is achieved by the various voltage levels with less harmonic contents with the reduced rating of voltage devices producing reduced stress on each switching elements. In 1980, the neutral point clamped and capacitor clamped multilevel topologies were introduced with exemplary features of handling high power applications in renewable energy along with many other advantages creating huge interest in the recent decades amongst researchers and industries.

With the increased number of levels in waveform and application in power delivery actively in motor drives, these topologies perplex over the charge balancing issue in capacitor circuits. This, in turn, increases the leakage current in the photovoltaic applications producing various hazards to working personals. Hence, such issues with transformerless multilevel converters are complex for such applications. The solution of this issue was proposed by with the introduction of generalized topology for the multilevel converter with self-voltage attuning. The major deficiency with this generalized circuit is a quantitative increase in the switching devices which engender complex switching states. Another topology came in existence to mitigate these anterior concerns with economized potential rating of switching devices and thereby augmenting
voltage output with the step up capability. Proposed circuitry may suit its application in photovoltaic system applications with reduced leakage current. The details of proposed application, switching operation and analysis of this topology are discussed in later section.

The main remonstrance brought in with Marx topology is the selection of the most appropriate Pulse Width Modulation (PWM) strategy for capacitors utilized in topology must be adequately charged and discharged with its on-off switching cycles of conduction. When charging of the capacitor is not acquiring with desired output voltage, this brings generation in distortion of the output voltage producing unsymmetrical conduction. FPGA based digital control algorithm along with the choice of relevant capacitance size is discussed in detail in later section.

FPGA based digital controlling of the power electronics converters has provided an attractive solution to the researchers. The platform consisting microprocessors, microcontroller, Programmable Logic Device (PLD), Digital Signal Processors (DSP), ASIC have added various advantages for implementation of various control algorithms. The features like high computational speed with reduced complexity of design have motivated the research community to focus on digitized control schemes for power electronics converters. The specific challenges for a power electronic designer as discussed in references to offer precision with flexibility, reliability, cost effective and highly efficient system. Analog control system basically suffered a major drawback of having a large number of components affecting the reduction in reliability with poor computational capabilities and limited bandwidth.

The paper discusses the real-time implementation of the carrier based control technique on Marx multilevel inverter with a photovoltaic interface and its comparison over the other topologies like Diode Clamped Multilevel Inverter (DCMLI) and Cascaded Multilevel Inverter (CMLI). The major improvement with the fundamental voltage and current in total harmonic distortion is observed and discussed in simulation and hardware sections.

2. Photovoltaic Energy Conversion

With the increase in the energy demands with a constant reduction in the supplies of the conventional fuel and excessive emission of carbon dioxide traces have led the foundation of the current research scenarios, majorly in the area of alternative energy resources. Amongst various resources the energy from the photovoltaic cell is considered as the most suitable with least environmental impact, its source is free and present in the abundance and distributed over the earth. A great advantage of the PV cells in the curtailment of carbon dioxide exudation targeting the year 2030 the CO₂ emission will be reduced by 1 Gton/year compared to India’s equivalent emission in the year 2004 or discharge from three hundred coal plants.

The general block diagram of the photovoltaic electrical system is displayed in Figure 1. In this, the series-parallel combination of the PV panels is connected first to generate the desired voltage and current. The regulation of the output voltage is further ensured by the use of DC-DC converter such as Buck-boost, Single Ended Primary Inductor Converter (SEPIC) or some other whose switching is ensured at the maximum power peak (mpp) of the PV array to achieve the maximum available power at any instant. The regulated DC voltage is then fed to the inverter topology, which converts it to the AC with suitable switching frequency. The harmonic distortion produced from this stage can be further minimized by the use of a filter in the output interface module and connected to the local loads. The use of control and monitoring is very important for the efficient operation of the overall system. Hence choosing a fast controller with reliable and fast response may increase the system time.

The PV panel exhibits highly nonlinear characteristics which depend on the level of solar irradiation and temperature Figure 2 shows the simulated PV and IV characteristics curve with a unique of operation where the peak power is available is generally termed as the maximum power point. Several methods for achieving this objective have been proposed in the literature.

Table 1 depicts the electrical ratings of the photovoltaic panel which is used to simulate the characteristics curves in Figure 1.

| Table 1. Electrical ratings of the SunPower SPR-305 |
|---------------------------------------------------|
| Maximum Power (Watts) Pmax | 305 |
| Voltage at MPP (Volts) Vmp | 54.7 |
| Current at MPP (Ampere) Imp | 5.58 |
| Open Circuit Voltage (Volts) Voc | 64.2 |
| Short Circuit Current (Ampere) Isc | 5.96 |
3. Marx Multilevel Converter

The multilevel converters have attracted the researchers for the generation of the most approximately sinusoidal output. It is capable of producing N output level where N is greater than two. Mostly these numbers of levels are generated from the multiple tapped capacitor voltage divider networks. In 1981, the DCMLI and flying capacitor multilevel inverter topologies were the first proposed.

Figure 1. General flow of the PVS with digital monitoring and control module.

![Diagram](image)

Figure 2. PV and IV characteristics of the PV module with various solar irradiation levels.

The motivation for the development of the Marx multilevel converter is laid from the major drawbacks observed from the previous developed multilevel topologies, which is the issue of capacitor voltage balancing while delivering the real power. In the year 2001, a generalized multilevel converter topology came in existence which had resolved the issue with self-voltage balancing; unfortunately, it also suffered a major drawback as the active switching devices grew largely with the number of levels.

3.1 Fundamental Notion of Marx Inverter

The presented topology works on a concept of high voltage level circuit termed as Marx generator. The basic ideology behind the working of the proposed circuit is that it can generate high voltage level by charging a parallel capacitor bank and discharging them in a series configuration. The series connection of the capacitor is made by a switching circuit comprising of spark gaps.

If we replace these spark gaps by some switching devices like MOSFET or IGBT based on the regulation of frequency, it provides ease of control to the number of capacitors in series connection with the load. Hence, this topology can generate desired voltage levels by DC bus addition.

![Diagram](image)

Figure 3. Elementary single phase Marx topology (a) Single phase three-level Marx inverter, (b) Primary Marx cell and (c) Conventional half-bridge inverter.
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The three-level proposed converter is displayed in Figure 3(a). An insight of Marx inverter is perhaps the generation of a huge voltage stroke by charging a set of capacitors switched in a parallel configuration and getting them discharged in series. This topology is the summation of the elementary Marx structural cell and typical half-bridge inverter. The circuit configuration for primary Marx structure is exhibited in Figure 3(b) and for primary half-bridge converter is demonstrated in Figure 3(c).

3.2 Postulate of Control

The function switching sequence of Marx converter is inferable by probing the operation of its primitive cell displayed as Figure 3(b). The primary Marx structure has a capacitor as C, with three switching devices which work in parallel connection (through S11, S12) with the capacitor using the DC connection or to conjoin it in series (through S12'). When the MOSFETs S11, S12 are switched on then the capacitor C is connected in parallel to DC bus and charged to VDC (Vc = VDC) and output of primary Marx structure is:

\[ V_0 = V_{DC} \]  

(1)

When the switch S12' is switched on the capacitor will be associated in series connection with the supply and the output of basic marx structure is represented as:

\[ V_0 = V_{DC} + V_C \]  

(2)

The primary half-bridge converter is used to equate the output connection voltage V0 to either +Vc (through SPC) and -Vc (through SPC'), SPC represents the polarity changing device.

The working principle of single phase three-level Marx inverter is as exhibited in Figure 4. The switching devices that are switched on are highlighted in thick while the device which is switched off is displayed with low shade. For instance, in Figure 4(a), switches S11, S12 and SPC are switched on to equate null voltage (V0 = 0, the zero voltage is correlated with negative supply of the DC), in Figure 4(b), S12', SPC is switched on to equate V0 = VDC and in Figure 4(c), switches S12' and SPC' are switched on to achieve the output voltage as V0 = 2VDC.

N is the number of levels above zero signals which is achieved by utilizing marx converter with (N-2) primary structures associated to half-bridge converter, with a number of MOSFETs equal to (3N-4). Three-level Marx converter have one primary structure cell and a half bridge converter along with five MOSFET devices.

4. Digital Controller Design and Implementation

The control of any multilevel inverter is a challenging task based on its analytical and harmonic study. Carrier based modulation maneuverings form a common thread between all the mentioned multilevel topologies with little alteration for each of them. Hence, the conventional control scheme can be adopted by the comparison of overall performance. The analytic solution and harmonics advantage for the various schemes of modulation strategies for multilevel operation is discussed in12. The mathematical analysis of the multicarrier modulation for Marx topology is discussed in13.

Here for Z number of levels Marx converter arranges Z-1 high-frequency triangular carrier with identical frequency and amplitude over the range of +Vdc and -Vdc.
The comparison of these triangular carriers is done with the single low-frequency sinusoidal carrier to produce the switched voltage output of the converter. Based on the position of the carrier these techniques can be subclassified as\textsuperscript{14,16}.

- Phase Disposition (PD)
- Phase Opposition Disposition (POD)
- Alternative Phase Opposition Disposition (APOD)

As shown in Figure 5, the comparison of carrier and the reference waveform for five levels Marx converter with four triangular carriers in each. In phase disposition scheme, all the carrier signals are in the identical phase and amplitude. In POD, the triangular signals above the reference zero point are 180 degrees out of phase with the below signals. In APOD, each of the carrier signals is shifted by 180 degrees from its adjacent signal.

The PD approach in line to line sense is better\textsuperscript{17}, as it locates less energy in the sideband and more in the main carrier harmonics is the main concern for choosing it for Marx topology over all others. The time deviating swapped phase voltage Van (t) for this is perhaps exhibited in specifications of the fundamental, harmonic constituents and the side band components by Equation 3.

\[
V_{an}(t) = V_{DC} M \cos(\omega_0 t + \phi) + \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2V_{DC}}{2\pi} \cos(k \omega_0 t + \phi) \cos(k \omega_n t)
\]

Here M represents the modulation index ranging between 0 and 1. In Table 2, the switching cycle of the reference signal is marked as a product of modulation index and cosine function and its comparison with the carrier produces the staircase output.

Xilinx System Generator (XSG) for Digital Signal Processing (DSP) is the leading simulating real-time tool for implementing better performing systems using almost all programmable devices. With XSG, the ease of implementation and creating high-quality algorithms is simplified compared to traditional tools. It provides simulation, modeling and automatic code generation from MATLAB/Simulink and Xilinx interface. The generated code is reusable on any platform; hence, it provides a tangible solution with listing the industry’s most advanced FPGA. System generator for digital signal control is part of the Xilinx System Edition (XSE) design suite. The tool system generator for digital signal processing provides developers with little design experience the facility to create production quality FPGA base implementations of design and algorithms with a reduced development period.

Design cycle for this tool is discussed in\textsuperscript{18}. In Figure 6, the reference sinusoidal signal is produced by the count based approach in the ROM. A step by step increment in the counter leads to the generation of this low-frequency signal. Similarly, the high-frequency triangular signals which are phase disposed of are generated. The comparison of these two generated signals further generates the switching signals, which are then sending to the output pins of the FPGA. Figure 7 shows the switching generation for the compared high-frequency carrier signals in Xilinx environment. Once the integration is completed the logic utilization summary is displayed which is shown in Table 3, which shows this Nexys4 FPGA board has not even utilized one percent of its efficiency.

**Figure 5.** The comparisons of the Sinusoidal low-frequency carrier and high-frequency carrier wave for five-level Marx inverter with PD modulation.

**Table 2.** Switching function f (x, y) for five level Marx topology

| F(x,y)   | When \(-\Pi \leq x \leq 0\) | When \(0 < x \leq \Pi\) |
|----------|-----------------------------|---------------------------|
| +2V_{DC} | \(M \cos y > \frac{1}{2} - \frac{x}{2\Pi}\) | \(M \cos y > \frac{1}{2} + \frac{x}{2\Pi}\) |
| +V_{DC}  | \(-\frac{x}{2\Pi} < M \cos y < \frac{1}{2} - \frac{x}{2\Pi}\) | \(\frac{x}{2\Pi} < M \cos y < \frac{1}{2} + \frac{x}{2\Pi}\) |
| 0        | \(-\frac{1}{2} < M \cos y < \frac{1}{2}\) | \(-\frac{1}{2} + \frac{x}{2\Pi} < M \cos y < \frac{x}{2\Pi}\) |
| -V_{DC}  | \(-\frac{x}{2\Pi} < M \cos y < -\frac{1}{2} - \frac{x}{2\Pi}\) | \(-\frac{1}{2} + \frac{x}{2\Pi} < M \cos y < -\frac{x}{2\Pi}\) |
| -2V_{DC} | \(-\frac{x}{2\Pi} < M \cos y < -\frac{1}{2} - \frac{x}{2\Pi}\) | \(-\frac{1}{2} + \frac{x}{2\Pi} < M \cos y < -\frac{x}{2\Pi}\) |
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\[-2V_{dc} \quad M \cos y < -1 - \frac{x}{2\Pi} \quad M \cos y < -\frac{1}{2} + \frac{x}{2\Pi}\]

5. Simulation and Hardware Discussions

The functional differentiation of multicarrier modulation techniques like (PD, APOD and POD) for DCMLI and CMLI is exhibited in [12]. The modulation index of 0.9 and carrier signal with 3 kHz in Table 4 shows the comparison of the phase disposition algorithms implemented on five level topologies (DCMLI, CMLI and MMLI) with RL load of 100 ohm and 10 mH and input voltage of 200 volts. The comparison shows the improvement of around five percent in the fundamental voltage and current with the three percent reduction in the voltage total harmonic distortion by using Marx multilevel inverter.

Figure 6. Snapshot of the multicarrier modulation technique implemented in Xilinx system generator.

Figure 7. Simulated pulses achieved from the proposed modulation strategy in Xilinx environment.

Figure 8. (a) Power circuit of Marx multilevel inverter and (b) Hardware setup of single phase five level Marx topology.

In this section, the different characteristics of multicarrier modulation approaches for Marx inverter in a real-time environment are discussed. The power circuit for simulation and the entire hardware of five level topology is exhibited in figure 8 (a) (b). The hardware is accomplished near a maximum voltage of a PV panel as discussed in the previous section with input associated to this the output is 30 volts with 50 Hz frequency with a carrier frequency of \(f_c = 3\ kHz\). The evaluation for the capacitors is measured according to the modulation techniques specified in the method addressed in [12], for Marx inverter with the aforementioned output voltage and 5 A of output current and Modulation Index 0.9. Four chan-
nel solar PV emulator will provide the isolated DC supply, it emulates the exact characteristics of the PV panel and this is fed to the power the circuit of the Marx inverter. The isolated power supply is made for each with and an optocoupler 6N135 is used in the driver circuit for the generation of the pulses from the Nexys 4 FPGA board.

This section deals with the PDPWM implementation for the Marx topology. The voltage waveform of five-level Marx multilevel converter is displayed in Figure 9(a). The PD modulation places the harmonic energy near carrier component for the single phase output voltage. Figure 9(b) represents the total harmonic distortion for a 3 kHz carrier signal about 20.3% which is without the filter. The Figure 9(c) represents the capacitor voltage levels for charging and discharging which is quite similar in nature reducing the issue of capacitor voltage balancing in the power circuit and the pulses generated in real time.

Table 3. Device utilization summary of digital controller

| Logic Utilization         | Used | Available | Utilization |
|---------------------------|------|-----------|-------------|
| Number of Slice Registers | 7    | 126800    | 0%          |
| Number of Slice LUTs      | 109  | 63400     | 0%          |
| Number of fully used LUT-FF | 3  | 113       | 2%          |
| Number of bonded IOBs     | 9    | 210       | 4%          |
| Number of BUFG/BUFGCTRLs  | 1    | 32        | 3%          |

Table 4. Comparison of DCMLI, CMLI and MMLI

| Topology | \( V_{fun} \) (Volts) | \( V_{thd} \)% | \( I_{fun} \) (Amps) | \( I_{thd} \)% |
|----------|-----------------------|----------------|----------------------|---------------|
| DCMLI    | 171                   | 35.64          | 1.709                | 14.71         |
| CMLI     | 179                   | 32.94          | 1.796                | 12.85         |
| MMLI     | 180.1                 | 32.6           | 1.8                  | 12.68         |

6. Conclusion

The simulation and hardware results from observation for the implementation of the single phase five level Marx topology for the photovoltaic application leads to the conclusion that phase disposition modulation verifies a superiority in line sense compared to the harmonics performance over other topologies for multilevel modulation. The suitable choosing of a capacitor bank in Marx primary cell converter and a suitable multicarrier modulation strategy will result in symmetrical operation with output voltage THD with appropriate filter circuit for optimized output in accordance with various industrial standards. The control has been observed with the use of
Nexys4 FPGA, which is quite advanced in the industrial application and the device utilization summary has been captured. The use of Xilinx system generator will reduce the effort of learning the hardware description language, to realize the logic in real time on the wide range of the programming devices. The balanced charging and discharging of the capacitor will lead to less leakage current, further reducing the health hazards to the working personnel in the region.

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