A study on electrical characteristics of Pentacene based MOS diodes and transistors

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Abstract. Recently, organic electronics has become an object of research in field of electronic devices because organic semiconductor materials have many advantages such as flexibility, low-cost production and low-temperature process. The purpose of this research is to fabricate metal-oxide-semiconductor (MOS) diodes and transistors using organic semiconductor materials called pentacene which is commonly used p-type organic semiconductor to fabricate organic devices such as MOS diodes and transistors because of its availability and stability. The lowest minimum capacitance in depletion region and the highest maximum capacitance in accumulation region obtained in this research were 0.1 μF/cm² at 5 V and 0.9 μF/cm² at -5 V, respectively. The highest magnitude of drain current measured in this research was around 1.4 μA at drain and gate voltage of -5 V.

1. Introduction
Organic thin film transistors have many potentials to be used in low cost, large area, light and flexible electronics. Moreover, organic thin film transistors can be fabricated by low-temperature process like thermal evaporation and spin coating. There was a laboratory group that fabricated inverter using organic thin film transistors [1]. Pentacene has become an attention because of its stability, performance and availability. In many publications, the mobility of pentacene based organic thin film transistors varies from 0.01 – 1 cm²/(Vs) which is close to that of amorphous silicon. Pentacene based devices are expected to be used as humidity sensors because, it is very sensitive to humidity [2, 3]. The surface energy of pentacene is around 38 mJ/m² [4]. Organic electronics have become so far from being just specific research [5]. The development of organic semiconductor material offers the probability to fabricate organic devices on a large surface [6]. Organic electronics also has many advantages like being light, flexible, and environmentally friendly so it attracts many researchers over the world [7]. Organic devices have many applications like RFID, sensor and displays [8]. Even though organic devices have lower mobility and larger subthreshold swing value than silicon based conventional devices, organic devices can be applied for flexible electronics. There is a laboratory who have fabricated analogue and digital circuit using organic material [9]. Devices fabricated from organic semiconductor pentacene can be in forms of MOS diodes, bottom contact and top contact transistors [10]. Pentacene is deposited using thermal evaporation and its performance depends on what it is deposited, surface treatment and process condition like deposition rate, substrate temperature and annealing after deposition [11]. Organic devices fabricated from pentacene can also be applied for humidity sensor because it is very sensitive towards water vapor and gases [12]. The purpose of this
research was to investigate the electrical characteristics of pantacene based MOS diodes and transistors.

2. Methods

Figure 1(a) and (b) illustrate how pentacene MOS diodes and transistors were fabricated and figure 1(c) and (d) describe how they were measured. Overall, there were 4 steps to fabricate pentacene MOS diodes and transistors. The pentacene MOS diodes and transistors were fabricated at the same time using different masks. First of all, the n$^+$-Si (100) wafer was cleaned to remove the organic material from its surface. Secondly, SiO$_2$ gate insulator was grown using thermal oxidation method. Then, the organic semiconductor material, pentacene was deposited on the SiO$_2$ using thermal evaporation method. Lastly, the Au electrodes were formed using shadow masks. The C-V characteristics of pentacene MOS diodes and the I_D-V_D characteristics of pentacene transistors were measured using C-V meter and semiconductor parameter analyzer.

Figure 1. The schematic of fabrication of (a) pentacene MOS diode, (b) pentacene transistor, (c) MOS diode measurement points and (d) transistors measurement points.

3. Result and discussion

The experiment results are shown from figure 2 to figure 4. Figure 2 shows how the capacitance changed when the applied voltage was changed and how C-V characteristics were influenced by different frequencies and by different pentacene thickness. The SiO$_2$ grown by thermal oxidation thickness was around 9 nm. Overall, the capacitance increased when the applied gate voltage was decreased from 5 V to -5 V and when the frequency was increased from 15 kHz to 1 MHz. The capacitance was higher when the pentacene thickness was around 15 nm. The horizontal axis and vertical axis represents applied gate voltage measured in volt and capacitance measured in $\mu$F/cm$^2$, respectively.

In figure 2 (a), with regards to frequency of 15 kHz, the capacitance began at 0.2 $\mu$F/cm$^2$ at 5 V and then increased rapidly to 0.5 $\mu$F/cm$^2$ at around 0 V before remaining almost constant at 0.5 $\mu$F/cm$^2$ when the voltage was decreased to -5 V. In terms of frequency of 110 kHz, the capacitance was around 0.2 $\mu$F/cm$^2$ at 5 V and then rose significantly to 0.4 $\mu$F/cm$^2$ at around 1.5 V before staying the same at 0.4 $\mu$F/cm$^2$ until the voltage was reduced to -5 V. Likewise, the capacitance started at 0.2 $\mu$F/cm$^2$ at 5 V and rose rapidly to around 0.35 $\mu$F/cm$^2$ at 1 V before remaining the same. In figure 2...
(b), in terms of frequency of 15 kHz, the capacitance began at just 0.1 \( \mu \text{F/cm}^2 \) at 5 V and remained almost constant until the voltage was 2 V before increasing rapidly to around 0.45 \( \mu \text{F/cm}^2 \). When the frequency was increased to 110 kHz, the maximum capacitance decreased by around half to 0.2 \( \mu \text{F/cm}^2 \). The maximum and the minimum capacitance differed slightly at around 0.1 – 0.15 \( \mu \text{F/cm}^2 \) when the frequency was further increased.

Figure 2. The frequency dependence of C-V characteristics of Au/Pentacene/SiO\(_2\) (9 nm)/n\(^+\)-Si(100) with pentacene of (a) 15 nm (b) 120 nm.

Figure 3 illustrates how parameters like applied gate voltage, pentacene thickness and SiO\(_2\) thickness affected the capacitance of pentacene MOS diodes. Overall, the capacitance of diodes whose pentacene thickness was 15 nm was higher for compared to that of diodes with pentacene of 120 nm. Moreover, when the SiO\(_2\) thickness increased, the total capacitance in the accumulation region decreased.

In figure 3(a), when the SiO\(_2\) thickness was around 5 nm, the minimum capacitance at the depletion region was around 0.25 \( \mu \text{F/cm}^2 \) at 5 V and the maximum capacitance at accumulation region was around 0.9 \( \mu \text{F/cm}^2 \) at -5 V. As the SiO\(_2\) thickness was increased to 9 nm, the minimum capacitance decreased slightly from 0.25 \( \mu \text{F/cm}^2 \) to 0.2 \( \mu \text{F/cm}^2 \) but the maximum capacitance decreased significantly from 0.9 \( \mu \text{F/cm}^2 \) to around 0.5 \( \mu \text{F/cm}^2 \). When the SiO2 thickness was further increased to 13 nm, the minimum capacitance remained constant at 0.2 \( \mu \text{F/cm}^2 \) but the maximum capacitance further decreased to 0.35 \( \mu \text{F/cm}^2 \).

In figure 3(b) where the pentacene thickness was 120 nm, the minimum capacitance at depletion region did not vary even though the SiO\(_2\) thickness was changed from 5 nm to 13 nm but the maximum capacitance at accumulation region decreased from 0.7 \( \mu \text{F/cm}^2 \) to 0.2 \( \mu \text{F/cm}^2 \) when the SiO\(_2\) thickness was increased from 5 nm to 13 nm.

Figure 4 shows how the drain current of the transistors changed when the applied drain voltage \( V_D \) and gate voltage \( V_G \) were changed. Overall the magnitude of the drain current in the linear region increased when the drain and gate voltage were changed to the more negative voltage. When the gate voltage was changed from 0 V to –5 V, the magnitude of drain current increased to around 1.4 \( \mu \text{A} \) in case of the transistors with pentacene of 15 nm and 0.75 \( \mu \text{A} \) for the transistors with pentacene of 120 nm.
**Figure 3.** The SiO$_2$ thickness dependence of C-V characteristics of Au/Pentacene/SiO$_2$/n$^+$-Si(100) with pentacene of (a) 15 nm (b) 120 nm.

**Figure 4.** The pentacene thickness dependence of transistor ID-VD characteristics. (a) pentacene 15 nm (b) pentacene 120 nm.

### 4. Conclusion

The metal-oxide-semiconductor diodes and transistors were fabricated using organic semiconductor material, pentacene. The results show that in the MOS diodes, the capacitance increased when the pentacene thickness was decreased. However, the maximum capacitance in the accumulation region also depended on the measurement frequency. The maximum capacitance in the accumulation region decreased when the measurement frequency was increased. Moreover, in case of equal pentacene thickness, the maximum capacitance in the accumulation region increased when the SiO$_2$ thickness was decreased. In transistors, the magnitude of drain current increased when the pentacene thickness was decreased.
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