A Thermal Machine Learning Solver For Chip Simulation

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ABSTRACT

Thermal analysis provides deeper insights into electronic chips’ behavior under different temperature scenarios and enables faster design exploration. However, obtaining detailed and accurate thermal profile on chip is very time-consuming using FEM or CFD. Therefore, there is an urgent need for speeding up the on-chip thermal solution to address various system scenarios. In this paper, we propose a thermal machine-learning (ML) solver to speed-up thermal simulations of chips. The thermal ML-Solver is an extension of the recent novel approach, CoAEMLSim (Composable Autoencoder Machine Learning Simulator) with modifications to the solution algorithm to handle constant and distributed HTC. The proposed method is validated against commercial solvers, such as Ansys MAPDL, as well as a latest ML baseline, UNet, under different scenarios to demonstrate its enhanced accuracy, scalability, and generalizability.

1 INTRODUCTION

It is well known that thermal issues can severely degrade the performance and reliability of chips Chandra [2], Emilio [4], Kumar et al. [8], Mutschler [9], Sun et al. [16]. Overlarge peak temperatures and stiff thermal gradients can fatally impact transistor performance, stress, aging, electro-migration (EM), voltage drops and timing Peach et al. [10], Zhong and Wong [18]. Hence accurate prediction of the maximum temperature and thermal gradient on the chip becomes important for the performance and reliability of chip-packaging systems used in several applications such as 5G, automobiles and computational hardware for Artificial Intelligence. Conventional Finite Element Analysis (FEA) or Computational Fluid Dynamics (CFD) based thermal analysis is computationally expensive due to the enormous system parameter space in the form of stiff powermaps and wide range of Heat Transfer Coefficients (HTCs), die thicknesses and chip sizes. As a result, batches of simulations are required to be solved from scratch every time new system parameters of electronic chips are considered.

Recently, a multitude of machine learning methods have been proposed to enhance and accelerate physics based numerical solvers in the context of electronic chip simulations. For example, a Deep Neural Networks (DNN) based fast static thermal solver has been proposed in Wen et al. [17] to generate a high-resolution Delta T map. In a new branch of study, researchers have employed Physics-Informed Neural Networks (PINNs) Russi and Karmiadakis [11] to solve chip problems Cai et al. [1]. Hennigh et al. [7] use PINNs to predict temperature profiles resulting due to variations in the FPGA heat sink geometry for a uniform power map. Similarly, Ranade et al. [13] and He and Pathak [6] use discretization-based techniques in combination with neural networks to predict temperatures on chips for powermaps sampled from a Gaussian distribution. Stipsitz and Sanchis-Alepuz [15] presented a proof-of-concept approach to provide approximate predictions of steady-state temperatures using convolutional neural networks. Chhabria et al. [3] use a convolutional encoder-decoder network to learn a mapping between powermap and temperature. Most studies in relation to thermal simulation of chips make simplifying assumptions about the power map or other system parameters such as HTC. The high dimensional parameter space involved in on-chip thermal simulations usually makes it challenging for conventional deep learning models to predict accurate temperatures for unseen input parameters.

In this paper, we propose a thermal ML-Solver, which is based on a recent work, Ranade et al. [12], for accurately simulating temperatures on electronic chips subjected to a wide range of system parameters. Our approach extends the previous method to modeling the complicated use case of electronic chips as well as proposes a slight modification to the solution algorithm to account for global...
system parameters as well as distributed HTCs. The input distributions considered in this paper have noticeable discontinuities and wider ranges of magnitudes and spatial distributions, which are extremely challenging to model. This paper demonstrates how the proposed approach can accurately model the temperature prediction widely ranging distributions of powermap and HTCs. The ability of this approach to accurately model such high-dimensional power maps and HTCs makes it unique and different from other ML approaches.

**Significant contributions:**

- We propose a thermal ML-simulator based on Ranade et al. [12] for electronic chip simulations over a wide range of parameters with varying spatial distributions.
- We modify the existing solution algorithm to handle global system parameters. This work can be considered as one of the first implementations of ML to handle distributed HTCs.
- Our approach entails solving a constrained equilibrium during evaluation, similar to traditional PDE solvers. This results in better stability, robustness and accuracy as opposed to blackbox ML methods.

### 1.1 Chip Thermal Analysis

Chip thermal analysis may involve multiple components of the chip and various system parameters with high dimensionality and huge parameter space. This study focuses on a simplified three-layer chip model consisting of a Si substrate, an insulation layer and an interconnection layer. The schematic of the three-layer model is illustrated in Fig. 1. An arbitrary tile-based power map, which consists of rectangular regions of different heat source, each representing a different functional block on the chip, is sandwiched between the insulation layer and interconnection layer. For instance, a 4000μm x 4000μm chip with 200μmx200μm tile size will lead to a 20x20 array power map. An example of such power map is shown in Fig. 2. Temperature distribution of the chip, especially the heating plane where the power map is applied, is of significant interest. In practice, such tile-based power could be random and incur drastic power gradient, which makes it challenging for conventional data-driven based approaches to learn, not to mention generalization to any unseen random power maps. Additionally, the temperature distribution on the heating plane is greatly affected by system parameters such as HTCs distribution on the boundary or die thickness, the effect of which is difficult to capture. Hence, in this study we only focus on accurately modeling chip temperature predictions on the heating plane across a wide range of parameters.

In a system-level simulation, the three-layer die is cooled either by natural or forced convection. The cooling effect of air is modeled here using HTC distributions on top and bottom surfaces.

![Figure 1: Schematic of the simplified three-layer chip model.](image1)

**Figure 2: Example of powermap and temperature on chip.**

### 1.2 Data Generation

In this paper, we present two use cases with varying levels of complexity. In the first case, the input parameters consist of a power map distribution on the heating plane, HTCs on boundaries and die thickness. Constant HTC values are applied on the top and bottom boundaries of the die, whereas other boundaries have adiabatic boundary conditions. The HTC varies in between $1e^{-6}$ and $1e^{-5}$, while the die thickness varies between 20μm and 200μm. 5000 numerical simulations are carried out utilizing a high-fidelity numerical solver, Ansys MAPDL, for simulating the heat transfer on a 4000μm chip with a grid resolution of 256x256x32 for random power maps, heat transfer coefficients and Die thicknesses. Examples of the power map and the corresponding temperature on the chip are shown in Fig. 2.

The second use case presents a more challenging scenario close to industrial applications, where the HTCs specified on the top and bottom boundaries also have a spatial tile-based distribution similar to that of the power map and the tile size is smaller. The HTC distribution on each tile are varied randomly from $1e^{-6}$ to $1e^{-5}$. Additionally, we reduce the tile size of powermap and HTC from 200 μm down to 50μm. In this case, 2500 numerical simulations are carried out using Ansys MAPDL for random power maps and HTCs.

In both cases, other parameters such as interconnection layer thickness, insulation layer thickness, Si substrate thermal conductivity, insulation layer thermal conductivity and interconnection layer conductivity are kept constant. The power on each tile is randomly sampled between 0 and 300mW and the total power on the chip is conserved among all the training samples. Even though the data is generated on a 3-D die, the solutions are retained only on the chip where the power map is applied. Hence, the temperature is predicted only on a surface but its spatial distribution and magnitude are affected by system parameters such as HTC and die thickness. As a result, these parameters are accounted for in the thermal ML-Solver along with power map. The division between the training and testing datasets is 80/20.
2 THERMAL ML-SOLVER DETAILS

A schematic of our model is described in Fig. 3. Here we describe the components of our thermal ML-solver and the modifications to the existing algorithm found in Ranade et al. [12].

1) Decomposition of computational domain: The computational domain corresponding to the 2-D chip (or plane of interest in Fig. 1) is decomposed into subdomains of equal physical sizes, where each subdomain consists of $m^2$ computational elements. As prescribed in Ranade et al. [12], based on an extensive ablation study, the value of $m$ is set to 16 resulting in around 256 subdomains for the 400μm chip.

2) Encoding on subdomains: An initial temperature of $T = 300K$ and a given power map, $P$ are encoded into lower-dimensional encodings $\eta$ and $s$ on every subdomain using pre-trained encoders. The global system parameters, $\gamma = HTC, Die_{x,y}$ are kept constant across all the subdomains in the first use case. The conditioning of all the subdomains with global parameters improves the predictive capability of the solver. In the second use case, HTC’s on top and bottom surfaces are decomposed into subdomains and encoded similar to the powermap but $Die_{x,y}$ is used as a global parameter. Even though the HTC is applied on the top and bottom surface of the die, they are considered to be applied on the plane of the chip for the sake of modeling a 2-D problem.

3) Constrained Thermal solver: A constrained equilibrium problem is solved using fixed point iterations where the encodings $(\eta, s, \gamma)$ on each subdomain and its neighbors are evaluated iteratively using a pretrained flux conservation autoencoder. In each iteration, the output encoding corresponding to temperature, $\eta'$, evaluated by the flux conservation autoencoder, is used to replace the input temperature encoding, $\eta$ for the next iteration. Other encodings such as $s$ and $\gamma$ are kept fixed. The fixed encodings serve as hard constraints and steer the temperature encoding towards an equilibrium, which resembles the encoding of converged temperature. The fixed point iteration is stopped when the following condition is met, $L_2(\eta - \eta') < 10^{-8}$.

4) Decoding on subdomains: The converged temperature encodings on subdomains at the end of the fixed point iterations are decoded into temperatures and post-processed on the entire computational domain.

It may be observed that our approach strongly draws ideas and inspiration from traditional PDE solvers. The novel iterative inference approach is designed to provide stability and robustness to the solution methodology in comparison to blackbox ML methods. Being the workhorse of our approach, the flux conservation autoencoder is useful in exchanging information amongst neighboring subdomains and from the boundary to the interior. This is similar to traditional solvers where flux conservation is employed between computational elements using numerical approximations for the same purpose. Finally, it is important to note that the training portion in this method corresponds to simply training 3 autoencoders in use case 1 and 4 in use case 2. Autoencoders are an unsupervised ML technique to obtain lower-dimensional encodings from higher-dimensional fields Goodfellow et al. [5]. It is important to note that we don’t explicitly train a model to learn a mapping between the inputs (power map, HTC and thickness) and outputs (Temperature). Instead, we solve a constrained equilibrium problem in the lower-dimensional latent space during inference to predict the temperature for a fixed set of inputs, such as power map, HTC and die thickness, which are specified by the user. The implementation of this component is unique and differentiates our approach from common ML methods.

2.1 Autoencoders in Thermal ML-Solver

In Figure 4, we describe the network architectures of autoencoders used in our algorithm. The autoencoders in Fig. 4A are CNN-based encoder-decoder networks. The encoder part of this network downsamples the subdomain field into a corresponding lower-dimensional encoding. The decoder part of the network upsamples the encoding back to the original input field. Separate autoencoders are trained for temperature and powermap for both use cases. Additionally, an autoencoder for distributed HTC is also trained in use case 2. On the other hand, the flux conservation autoencoders are DNN-based encoder-decoder networks. The temperature, powermap and system parameters on a 2-D stencil of 5 subdomains are encoded using the pretrained encoders and stacked together as shown in Fig. 4B to form the input for this network. All the autoencoders are trained in Tensorflow 2.0 using an Adam optimizer with mean absolute error loss. We choose autoencoders over other compression techniques because non-linear autoencoders have powerful generalization and denoising capabilities with reasonable compression ratios Goodfellow et al. [5]. This improves the stability, robustness and ultimately the convergence of the constrained equilibrium solve employed during the evaluation of our approach.

2.1.1 Specific architecture details:

Solution and Condition autoencoder: These are CNN based encoder-decoder networks. The encoder part of the network has a series of 3 convolution layers followed by max pooling. The number of filters in the convolution layers are 16, 32 and 64 respectively. The output of the convolution layer is flattened and passed through 2 dense layers of size 1024 and 21, where 21 is the size of the latent vector. In this work, the solution, power map and distributed HTC fields are encoded to the same latent size. The decoder part of the network is exactly symmetric to the encoder. 

Flux conservation autoencoder: The flux conservation autoencoder has an input size of 230 in the case of constant HTC and die thickness and 330 with distributed HTC. This is a fully-connected encoder-decoder based network. The encoder part of the network has 2 hidden layers with sizes 1024 and 512. The latent vector for this network has a size of 35. The decoder part of the network is exactly symmetric to the encoder.

3 RESULTS AND DISCUSSION

In this section, we present results obtained from our approach for unseen test cases across both the use cases and compare it with Ansys MAPDL. For the first use case with constant HTC, we provide additional experiments to demonstrate the generalizability of our approach for varying chip sizes as well as tile size and out-of-range HTC values. Finally, we compare our solver with a popular ML
Figure 3: Solution algorithm

A) Temperature/Power autoencoder

B) Flux conservation autoencoder

Figure 4: A) Temperature and power map autoencoder architecture and B) Flux conservation autoencoder architecture
network, UNet Ronneberger et al. [14], across all the experiments. It must be noted that different instances of the solver are trained for the 2 use cases due to the differences in HTC inputs.

3.1 Use case 1: Constant HTC

3.1.1 Unseen test cases. In this experiment we test the thermal ML-Solver for unseen, randomly sampled powermaps, HTC and die thickness. The testing is carried out on 500 samples not included in the training set. The relative $L_2$ error, defined as $\epsilon = \frac{L_2(T_{true} - T_{pred})}{L_2(T_{true})}$, is 0.078. The relative $L_2$ error serves as the most suitable metric in this case because the system parameters can result in a wide range of chip temperature magnitudes. Randomly selected samples are plotted in Fig. 5 and show that the thermal ML-Solver matches well with results obtained from Ansys MAPDL.

3.1.2 Generalization to larger chips. In this experiment, we test the generalizability of our approach to chips of size 8000 $\mu$m and 16000 $\mu$m. It should be noted that all models are trained on a chip of physical size of 4000 $\mu$m. The testing is carried out on 5 testing samples for each chip size with randomly varying powermaps, HTC and die thickness. The relative L-2 error for the 8000 $\mu$m and 16000 $\mu$m chips are 0.058 and 0.089 respectively. The prediction accuracy of our thermal solver to larger chips may be attributed to the local learning approaches coupled with iterative inferencing schemes. Additionally, in Fig. 7 we compare the contour plots of our approach with Ansys MAPDL for randomly selected testing samples. It may be observed that for both chip sizes, the thermal ML-Solver accurately models the temperature. Although not shown here, we expect our solver to scale to even larger chip sizes because of the local learning approach employed in our approach.

3.1.3 Generalization to a different tile size. Next, we demonstrate generalization to a different tile size of the powermap equal to 250 $\mu$m. It should be noted that all models are trained on tile sizes of 200 $\mu$m. The testing is carried out on 5 testing samples for each chip size with randomly varying powermaps, HTC and die thickness. The relative L-2 error obtained is 0.14. It may be observed from the contour plots in Fig. 8 that the results match reasonably well with respect to Ansys MAPDL.

3.1.4 Generalization to out-of-range HTCs. In this section, we test the performance of the thermal ML-Solver in the extrapolation regime of HTC. We generate 5 samples for HTC $1e^{-4}$, $2e^{-4}$, $3e^{-4}$, $4e^{-4}$ and $5e^{-4}$ for a die thickness of 150 $\mu$m and random power distribution. The average relative $L_2$ error is 0.098. It may be observed from the contour plots in Fig. 8 that the results match reasonably well with respect to Ansys MAPDL and the error progressively increases as we go further away from the training HTCs.

3.2 Use case 2: Distributed HTC and 50 $\mu$m tile

3.2.1 Unseen test cases: In this section, we test the thermal solver on 250 testing samples with unseen HTC and power map spatial distributions. Distributed HTCs can have a greater impact on temperature distribution making it more challenging to model. Additionally, the smaller tile sizes results in more local heating and stiffer peaks in temperature which are also difficult to model. Despite the challenges, our approach performs reasonably well with average relative L-2 errors of 0.045 across all samples. It may also be observed from the contour plots in Fig. 6 that the temperature predictions between our thermal ML-Solver and Ansys MAPDL...
match well. Although not shown here, but our solver continues to generalize to bigger chip sizes for this use case as well with the same accuracy as the previous case.
Table 1: Comparison between thermal ML-Solver and UNet

| Experiment         | Thermal ML-Solver | UNet |
|--------------------|-------------------|------|
| Section 3.1.1      | 0.042             | 0.049|
| Section 3.1.2 (8000\(\mu\)m) | 0.058             | 1.05 |
| Section 3.1.2 (16000\(\mu\)m) | 0.089             | 1.18 |
| Section 3.1.3 (250\(\mu\)m)  | 0.14              | 0.2  |
| Section 3.1.4      | 0.098             | 0.35 |

3.3 Comparison with other ML baselines

Next, in table 1, we report the relative \(L_2\) comparisons between our approach and another popular approach, UNet Ronneberger et al. [14] for all the test cases considered in this paper. The significantly better accuracy of results observed in table 1 demonstrates the superior generalization capability of our approach. Moreover, since our approach operates like a solver it can successfully scale to bigger chip sizes where traditional ML approaches cannot.

3.4 Computational time comparison

The computational time required by MAPDL on a 4000\(\mu\)m chip is about 30 min on a single CPU. On the other hand, the thermal ML-Solver converges in less than 10 seconds on a single CPU. Moreover, since our approach has similarities with traditional solvers it can be easily scaled to multiple CPUs and GPUs. The savings in time increases proportionally as the chip size increases. Finally, it must be noted that our approach employs iterative evaluation and can be slower than black-box ML models but it compensates by providing better accuracy, generalizability and scalability. For example, UNet requires less than 1 second to compute the solution but has a degraded accuracy and generalizability.

4 CONCLUSION

In this work, we introduce a thermal ML-Solver, which is based on the recently proposed CoAEMLSim approach Ranade et al. [12], to accurately predict temperature for electronic chips across the high-dimensional system parameters in the form of power map, HTC, die thickness etc. In this paper, we show two use cases with constant and distributed HTC’s, and demonstrate the accuracy of temperature predictions with respect to Ansys MAPDL on unseen test cases. Moreover, we provide additional experiments to test the generalizability of our approach across varying chip sizes, tile sizes and out-of-range HTCs and demonstrate our superior performance in comparison to a state-of-the-art ML baseline. Although the thermal solver demonstrated in this work is trained and tested for powermap tile sizes of 200\(\mu\)m x 200\(\mu\)m, the same approach can be easily extended to smaller tile sizes ranging from 1 – 10\(\mu\)m.

In future, we would like to extend the approach to transient chip problems and chip packages with geometric complexities and material variations.

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