Hybrid Crossbar Architecture for a Memristor Based Memory

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Abstract—This paper describes a new memristor crossbar architecture that is proposed for use in a high density cache design. This design has less than 10% of the write energy consumption than a simple memristor crossbar. Also, it has up to 4 times the bit density of an STT-MRAM system and up to 11 times the bit density of an SRAM architecture. The proposed architecture is analyzed using a detailed SPICE analysis that accounts for the resistance of the wires in the memristor structure. Additionally, the memristor model used in this work has been matched to specific device characterization data to provide accurate results in terms of energy, area, and timing.

Index Terms—Memristor, cache, memory, device, SPICE.

I. INTRODUCTION

As CMOS devices have shrunk into the nanoscale regime, the increase in power density in CMOS systems has stopped the increase in single core processor performance. For this reason CPUs are now based on multicore architectures. There are two main factors that limit the performance of these architectures. First, there is currently not enough on-chip memory to effectively handle the instruction and data load that the multicore architecture is capable of processing. Second, power consumption limits the number of cores and on-chip memory, thus limiting performance.

As an alternative to traditional SRAM, Resistive Random Access Memory (RRAM) is a promising solution to the forthcoming memory wall problem in conventional CPUs. These memories work based on different resistive switching mechanisms where a dynamic resistance value determines the memory state of the device. The three main types of RRAM include memristors [1]-[2], Phase Change Random Access Memory (PCRAM) [3], and Spin-Torque Transfer Magnetic Random Access Memory (STT-MRAM) [4].

In 2008, the first physical realization of the memristor (initially theorized in 1971 [1]) was published [2]. Furthermore, memristor crossbar arrays have been proposed [5] as the potential building block of an ultra-high density memory system. The problem with these high density crossbar arrays is that the power consumption will increase dramatically with the size of the crossbar [6]. This is due to the many alternate current paths lowering the effective resistance of the array. Additionally, read errors are much more likely due to these alternate current paths. To solve this, a 1 transistor-1 memristor (1T1M) bit cell can be used which is commonplace in STT-MRAM architectures [7],[8]. Unfortunately, this will lower the density of the memristor memory system to that of a single transistor array.

This paper presents a memristor based memory system that is capable of achieving more than 4 times the density of a typical STT-MRAM array. Additionally, it has dramatically reduced power consumption when compared to a high-density transistor-less memristor crossbar. This is done by tiling many smaller memristor arrays for partially isolated resistive grids.

The analysis of this memory design is performed through SPICE simulation. To model the memristors, a previously published device model [9] is utilized that is capable of reproducing memristor characteristics very accurately. Both the wire resistance and the isolating transistors in the array are simulated to provide a more complete crossbar analysis. This work describes a very accurate device level simulation of a novel memristor based memory architecture, and provides results for energy consumption and noise margin within the circuit. An accurate area analysis is also performed that describes the layout of the memory system. Very few crossbar simulations [10],[11] account for wire resistance, and these were completed with less accurate device models.

This paper is organized as follows: Section II provides a comparison of the existing resistive memory devices and crossbar memory designs. Section III describes the design of the proposed memory architecture and Section IV discusses the procedure used to analyze the simulated crossbar tiles. Section V displays the results of the crossbar tile analysis and Section VI concludes the paper.

II. RESISTIVE MEMORY TECHNOLOGY

A. Resistive Memory Devices

Resistive switching devices such as STT-MRAM, PCRAM, and memristor devices have all been proposed as possible solutions for the development of high density memory. These different types of resistive memory devices are used in a similar manner, although their properties differ slightly.
Previous research suggests [8][12] that STT-MRAM is the most promising candidate for the future of high-density, non-volatile, resistance switching memories. The $R_{OFF}/R_{ON}$ ratio of STT-MRAM is typically only about 2.5 [4],[13], so it is not likely that an STT-MRAM memory system would work without an access transistor for each individual memory device. This creates a problem where the maximum areal density of this type of memory system is limited by the size of an access transistor (similar to Fig. 1(a)) and not the nanoscale magnetic switching element.

PCRAM is another promising new memory technology. It has the lowest endurance in terms of switching cycles before failure, and generally has a longer switching time (50 to 100ns) [14] when compared to memristors and STT-MRAM. For these reasons, the majority of the PCRAM based memory systems are proposed as a replacement for DRAM as opposed to SRAM. However, PCRAM has the advantage of unipolar switching [3], so diodes can be used to limit unwanted current paths in a higher density design.

The memristor device that was selected for the final results in this paper has a relatively fast switching time (10ns) and very low current draw with an on state resistance of 125kΩ [5]. Additionally, the device has a very large off to on ratio (about $10^6$) that will be very useful in the proposed design since a limited number of unwanted current paths will be present. A number of other memristor devices [15],[16] were tested for use in the system, but according to our simulations they either had a power consumption that was too large, or a $R_{OFF}/R_{ON}$ ratio that was too small.

B. Crossbar Array Designs

A common solution to eliminate alternate current paths in a resistive memory system is to place an access transistor alongside each memory element (see Fig. 1(a)). This technique greatly reduces the chance of a read error and limits the power consumptions since greater control is placed on the path of the current flow. The disadvantage of this type memory system is that the areal density of the system is now limited by the area of the transistors and not the area of the memory devices.

The circuit diagram and layout for a high density memory crossbar can be seen in Fig. 1(b) and (c). In this design nanoscale memory elements can be packed at a much higher density. Each memory element will consume an area of just $4F^2$ [17] where $F$ is the minimum feature size of the fabrication technique. The schematic in Fig. 1(b) illustrates the problem with this type of crossbar. When voltages are applied to the wires $a_1$ and $b_1$, nothing is stopping current from flowing through other devices. This can lead to read errors in a large crossbar because the current sensed at $b_1$ could be due to a chain of devices in a low resistance state when the selected memristor is in a high resistance state. This also increases the power consumption of the crossbar, as the current draw increases due to the many alternate current paths.

Some preliminary simulation results show how the energy consumption of a high density crossbar increases with crossbar size in Fig. 1(d). The value plotted is the energy required to write a single bit. Since the simulations were performed in SPICE, a 16×16 crossbar containing 256 memristors was the largest system that could be simulated. If assumed to be linear, the data can be extrapolated to show that large crossbars quickly reach a level of energy consumption that would be unrealistic for a competitive memory technology. This study was performed assuming a 500Ω wire resistance between all memristors modeled after the device in [5] using 10ns ±7V write and erase pulses.

As a possible solution to this problem, one publication [18] presents a memristor device with current suppression in one direction. This reduces the problem of alternate current paths, although the switching time of this device is too large for an on-chip memory application (100μs).

![Fig. 1. Memristor crossbars including (a) a 1T1M architecture schematic, and (b) a high density unconstrained crossbar displaying the target memristor path (green) as well as two possible alternate current paths (red). For the circuit in (b) we show the (c) layout, and (c) write energy consumption.](image)

III. PROPOSED HYBRID CROSSBAR DESIGN

The proposed hybrid crossbar architecture is a combination between a high density array, and one with transistor isolation. In this design, transistors are used to isolate small crossbars within a larger array. These smaller memristor arrays will be referred to as tiles. Fig. 2 displays a portion of the circuit design for the hybrid memory system.

In this example, 4 memristor tiles are displayed, each consisting of 16 memristors arranged into a 4×4 square. The top of the circuit displays a pulse generator block, which is responsible for sending data to a single row in each tile (through either $D_{R1}$, $D_{R2}$, $D_{R3}$, or $D_{R4}$) and grounding the rest. Additionally, a row decoder containing the row select signals ($S_1$ through $S_4$) is designed to turn on only one row of tiles during a parallel read or write operation. During a read or write operation, data from the selected row of tiles will be processed by the column circuits. This design allows for all
unwanted current paths to be contained within the small 4x4 crossbars with twice the bit-cell density of a 1T1M design.

A write operation in this design is a two-step process [19] that writes to an entire row of memristors in each of the selected tiles (see Fig. 3). The first step is to apply a voltage of \( V_r/2 \) to a selected row (grounding the other 3), and to apply a voltage of \(-V_r/2\) to all columns where a 1 (low resistance state) should be written (where \( V_r \) is the write voltage). Furthermore, a voltage of \( V_r/2 \) should be applied to all global column wires were a 0 (high resistance state) should be written (through the write enable transistors). This will result in writing a 1 to only the memristors in the selected row that need to be set to 1. During the second step in the write process, a voltage of \(-V_r/2\) is applied to the selected row, and all global column wires are set as they were in step one. This will result in writing a 0 to the rest of the memristors in the row.

A parallel read operation is performed by setting a selected row of memristors to a voltage below the switching threshold, and activating the read enable transistors in each column circuit. The analog read voltage across \( R_S \) (in Fig. 2) is converted to a binary signal using a comparator and the constant threshold resistance \( R_T \).

**IV. HYBRID CROSSBAR ANALYSIS**

**A. Memristor Device Model**

To perform a device level analysis of a memristor crossbar memory system, a SPICE equivalent of the memristor model first proposed in [9] was utilized. This model was set to match the characterization data of one of the memristor devices published in [5] (see Fig. 4). This device was chosen for use in the proposed memory design because it had a large \( R_{OFF}/R_{ON} \) ratio (10^4) while still retaining a relatively low switching time (about 10 ns). It also has a large on state resistance of about 125kΩ (determined by the 8µA current from a 1V read pulse).

The simulation result in Fig. 4 shows the minimum and maximum resistances of the model to be 124.95kΩ and 125.79×10^3Ω respectively, which correlates very closely to the characterization [5]. Applying a +7V pulse successfully switches the device into a low resistance state, and applying a -7V pulse drives the model into a high resistance state. These strong simulation results show that a reliable device model has been developed, and this will lead to more accurate results when simulating memristors.

**B. SPICE Circuit Simulation**

To determine the maximum noise margin and energy consumption of both the 4x4 and 8x8 tiles, a large string of read and write signals was applied to a crossbar simulation. Crossbar circuit operation varies based on the resistance values of memristors within the crossbar, so a large number of randomized signals were applied to obtain an average result.

To complete this task, the signals were generated in MATLAB and then saved in a text file that could be interpreted in LTSpice (see Fig. 5). The signals generated included switching signals for the transistors to select the correct memristors, as well as the data signals that contained...
the read and write pulses.

![Block diagram for MATLAB/SPICE simulation process.](image)

The row of memristors that was to be written was chosen at random by the MATLAB script. The data that was written in the memristors was also randomized by choosing to apply either a +7 or -7V pulse signifying a write or erase operation respectively. These voltages were chosen to match the switching characteristics in [5]. After each write operation was performed, a read operation was performed that read each of the memristors in the crossbar one row at a time.

A 3-dimensional binary answer matrix (x-dimension: crossbar row, y-dimension: crossbar column, z-dimension: simulation cycle) was also generated at the time of the random signal creation in MATLAB. This answer matrix held the result after each write cycle. The total energy consumption in the circuit was then evaluated using the signals generated in MATLAB. This answer matrix held the data in the crossbar tiles. When considering transistor and high nano-wire resistances [20], write errors can be a more common occurrence even when using a write technique [19] thought to eliminate write errors. Write voltage must be increased in the presence of wire resistance to ensure the selected memristor devices would be fully switched. However, increasing the write voltage also increases the probability that a voltage drop across a half-selected device (see Fig. 3) will be greater than the memristor write threshold, leading to unwanted changes in the stored data. When comparing the two tile designs, Table 1 shows that the 8x8 crossbar provides twice the bit density. Although, it has a lower noise margin and consumes more energy due to the alternate current paths.

To perform this task, the analog read voltages ($V_r$) across the sense resistors ($R_s$) were imported into MATLAB and the voltage peaks at each read were extracted. These values were compared to the data in the answer matrix as the dead zone between 1 and 0 was increased. The maximum width of the dead zone (in mV) that did not produce a read error was considered to be the noise margin (see Fig. 6). It should be noted that previous publications [19] have proposed methods for determining the sense resistance value to produce maximum noise margin. However these methods did not hold true in our case most likely due to the added wire resistance.

!![](image)

**Fig. 6.** Noise margin in memristor crossbars.

To determine the write energy, a large number of write pulses (without reading afterward) were applied to the crossbar tile. The total energy consumption in the circuit was then divided by the number of writes to determine the average write energy per bit. Determining the read energy was a similar process where a series of reads (without writes) was applied to the crossbar initialized with a random data pattern to determine the average read energy per bit.

### V. CROSSBAR TILE RESULTS

#### A. Energy Analysis

A large number of simulations were completed to determine the optimal sense resistance and write voltage that would maximize the noise margin (see Table 1) for the 4x4 and 8x8 crossbar tiles. When considering transistor and high nano-wire resistances [20], write errors can be a more common occurrence even when using a write technique [19] thought to eliminate write errors. Write voltage must be increased in the presence of wire resistance to ensure the selected memristor devices would be fully switched. However, increasing the write voltage also increases the probability that a voltage drop across a half-selected device (see Fig. 3) will be greater than the memristor write threshold, leading to unwanted changes in the stored data. When comparing the two tile designs, Table 1 shows that the 8x8 crossbar provides twice the bit density. Although, it has a lower noise margin and consumes more energy due to the alternate current paths.

### Table 2. Performance comparison of different memory cell designs.

| Memory Architecture | SRAM Active | SRAM Leakage | STT-MRAM Hybrid (4x4) | Hybrid (8x8) | 1kB Crossbar |
|----------------------|-------------|--------------|-----------------------|-------------|-------------|
| Bit Density (Gbits/cm²) | 0.338 | 0.760 | 1.98 | 3.95 | 12.35 |
| Read Energy (Ω/bit) | 0.7 | 27.7 | 60.4 | 5.506 | 6.849 | 21 |
| Write Energy (Ω/bit) | 0.7 | 27.7 | 1177 | 3118 | 6372 | 70000 |
| Read Time (ns) | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 |
| Write Time (ns) | 0.3 | 0.57 | 10 | 10 | 10 |
B. Area Analysis

If the system utilizes 4x4 tiles, then it will require 8 transistors to drive a tile consisting of 16 memristors (an average of 2 memristors per transistor). This system was also analyzed where each of the tiles consisted of 64 memristors in an 8x8 arrangement. The 8x8 tile consists of 16 transistors and 64 memristors (an average of 4 memristors per transistor). In these designs the size of the transistors is still the limiting factor in memory density. However, the 4x4 and 8x8 tile systems provide an increase in density over a 1T1M system by a factor of 2 and 4 respectively. The layouts for the 4x4 and 8x8 tiles can be seen in Fig. 7, where the red squares represent memristors. Standard CMOS design rules limit the transistor cell size to 50µm². For the memristor layers, nanoscale fabrication methods should be able to pack memristors at a higher density [2],[18] than standard fabrication methods.

The peak drain current of any single transistor during a write in the 4x4 tile was about 120µA, and about 200µA in the 8x8 tile. These currents are significantly lower than the requirement for energy efficient STT-MRAM cells [4],[8]. For this reason the transistor packing density in the hybrid array can be the same or higher than that of STT-MRAM.

VI. CONCLUSION

A new hybrid memory system has been proposed that can provide up to 5.2 times the memory density of an STT-MRAM system. The proposed system has a significantly lower energy consumption compared to a large high density memristor crossbar. A detailed analysis of the design including wire resistance and accurate device modeling was performed in SPICE. Future work includes a further study of the memory system to see if larger tiles would benefit the system. Our existing simulations show that a 16x16 tile is not capable of producing a significant noise margin, although it may be possible to correct this by modeling alternative memristor devices. If larger tiles are used, it may be possible for this system to approach the bit density of a transistor-less crossbar.

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