High performance differential Colpitts VCO with a linearized tuning range using a series resonator

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Abstract: This paper proposes a novel low-phase noise Colpitts voltage-controlled oscillator (VCO) using a series LC network. For the series LC network, two capacitors are connected to each node of a parallel inductor-varactor tank (PLC). Each series connection node of the network is cross-coupled to the gates of switching transistors, and a large signal swing is achieved at each connection node. Also, the fixed biasing current sources of the differential Colpitts VCO are modified to operate as switched biasing current sources to lower the phase noise. Designed in 65 nm CMOS technology, the proposed VCO achieves a linearized tuning range from 3.73 to 3.97 GHz. The VCO consumes about 0.89 mW from a 0.4 V supply voltage, and achieves the phase noise of –123.3 dBc/Hz at 1 MHz offset. The calculated figure of merit of the VCO is about –195.5 dBc/Hz/mW.

Keywords: CMOS, Colpitts, low-power, voltage-controlled oscillator

References

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1 Introduction

A differential cross-coupled VCO is widely used for its ease of implementation and start-up. But, it has a disadvantage that the maximum phase noise
sensitivity coincides with the zero-crossing of the differential outputs. On the other hand, Colpitts topology features superior phase noise characteristics since the noise generated from the active devices is maximum when the oscillator is least sensitive to injected noise. However, the conventional Colpitts VCO has the weakness of poor start-up. Differential Colpitts VCOs are developed to overcome the poor start-up while keeping the low phase noise characteristic [1, 2]. Also, a switched biasing technique for the tail current source is developed to suppress the phase noise in the low offset frequency [1, 3].

In this letter, a novel low-phase noise Colpitts VCO is proposed using a series resonator and the switched biasing technique.

### 2 Circuit design

Fig. 1(a) shows a conventional Colpitts VCO, which suffers from poor start-up characteristics; i.e., higher power consumption is required to make reliable start-up [2]. Fig. 1(b) shows a differential Colpitts VCO in [2] which cross-couples the switching transistors rather than providing a fixed bias to the gate as in [1]. Fig. 1(c) shows the proposed VCO in which a series network is inserted between the drain nodes of the switching transistors. The negative small-signal conductance for Fig. 1(a) is given by

$$Re(Y_{m, Fig. 1(a)}) = -\frac{g_{m1}\omega^2C_1C_2}{g_{m1}^2 + \omega^2(C_1 + C_2)^2}$$  \hspace{1cm} (1)

where $g_{m1}$ is the transconductance of the switching transistor and $\omega$ is the angular frequency [2]. The negative conductance looking into the drain of $M_1$ or $M_2$ for Fig. 1(b) is given by

$$Re(Y_{m, Fig. 1(b)}) = -\frac{g_{m1}\omega^2C_1C_2(2 + C_2/C_1)}{g_{m1}^2 + \omega^2(C_1 + C_2)^2}$$  \hspace{1cm} (2)

From (2), it is seen that the magnitude of negative conductance of Li’s VCO is increased by a factor $(2 + C_2/C_1)$ compared to that of the conventional Colpitts VCO [2].
Fig. 1(c) shows the proposed Colpitts VCO in which a series network is inserted between the drain nodes of the switching transistors. In the series network, each node of a parallel inductor-capacitor (varactor) is connected to a capacitor in series and cross-coupled to the gates of the switching transistors. The oscillation frequency of the proposed VCO is determined by the series network. The inductor $L_1$ just plays the role of a choke to supply the dc current. However, it is optimized to cancel out the total capacitance at the drain node of the switching transistors, resulting in the maximized swing at the drain nodes. The voltage gain from the drain to gate in the series network in Fig. 1(c) is approximately given by

$$A_G = \frac{v_{y+}}{v_{d+}} \approx \frac{\omega L_2}{R_{s2}}.$$ \hspace{1cm} (3)

where $L_2$ is the inductance and $R_{s2}$ is the series resistance of $L_2$. From (3), it is seen that there is a voltage gain in the series network. Finally, the negative conductance of the proposed Colpitts VCO is given by

$$Re(Y_{in, Fig. 1(c)}) = \frac{-g_{m1}\omega^2 C_2 (2C_1 + C_2)}{g_{m1}^2 + \omega^2 (C_1 + C_2)^2} + \frac{g_{m1}^2 L_1 C_1}{\omega^2 L_2 C_1 (g_{m1}^2 - \omega^2 (C_1 + C_2))} \frac{g_{m1}^2 L_1 C_1}{\omega^2 (C_1 + C_2)^2}$$ \hspace{1cm} (4)

From (1), (2) and (4), it is clearly seen that the negative conductance of the proposed Colpitts VCO is increased compared to that of the conventional Colpitts VCO and Li’s VCO. With the increased negative conductance, the proposed Colpitts VCO enables easy start-up with less power consumption [2]. Fig. 2 shows the differential impedance looking at the drain and gate nodes of the Li’s VCO and the proposed VCO. From Fig. 2, the magnitude of impedance at the drain node is comparable for both VCOs. However, the magnitude of impedance at the gate node of the proposed VCO is much higher compared to that of the drain nodes, which results in a higher quality factor of the series resonator of the proposed VCO and better phase noise performance.
3 Simulation results

The proposed VCO is designed in 65 nm CMOS technology. To compare the Li’s VCO and the proposed VCO, transistors and the capacitors are designed to have the same sizes, and the inductors and varactors in the resonator are optimized to have the similar oscillation frequency for the same power consumption. Fig. 3 shows the voltage swing of the Li’s VCO and the proposed VCO. For the proposed VCO, the maximum differential voltage swing at the drain and gate nodes can reach up to $2V_{DD}$ and $4V_{DD}$, respectively. Fig. 4 shows the simulation result of the tuning range, VCO gain, and the phase noise performance of the Li’s VCO and the proposed VCO. It has been known that the frequency tuning range is more linearized with the increased output swing [4]. As shown in Fig. 4(a) and (b), it is seen that the tuning range is linearized for the proposed VCO due to the increased voltage swing at the gate nodes of the switching transistors given by (3). At around 3.8 GHz, Fig. 4(c) shows the simulated phase noise of two VCOs. The phase noise of the proposed VCO is about $-74$ dBc/Hz and $-123.3$ dBc/Hz at $10$ kHz and $1$ MHz offset frequency, which is about $10.5$ dB lower phase noise compared to that of the Li’s VCO. From $0.4$ V supply voltage, the proposed VCO consumes about $0.89$ mW dc power. The figure of merit (FOM) of VCO is defined as

$$FOM = L(\Delta f) + 10 \log(P_{dc}) - 20 \log(f_0/\Delta f)$$

where $L(\Delta f)$ is the phase noise at an offset frequency $\Delta f$, $P_{dc}$ is dc power consumption in mW, and $f_0$ is the oscillation frequency. The calculated FOM is about $-195.5$ dBc/Hz/mW. For the Li’s VCO, the calculated FOM is $-183.5$ dBc/Hz/mW for the same power consumption.

Fig. 3. Voltage swing of (a) Li’s VCO and (b) the proposed VCO.
4 Conclusion

A novel series resonator based differential Colpitts VCO is proposed. A series network is inserted between the drain nodes of the switching transistors to increase the negative conductance and output voltage swing. Also, a switched biasing technique is applied to the VCO. Implemented in 65 nm CMOS technology, the proposed VCO has a linear tuning range from 3.73 to 3.97 GHz, achieves the phase noise of $-123.3 \text{ dBc/Hz}$ at 1 MHz offset, and consumes about 0.89 mW from 0.4 V low supply voltage. The calculated FOM is about $-195.5 \text{ dBc/Hz/mW}$.

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