FeCAM: A Universal Compact Digital and Analog Content Addressable Memory Using Ferroelectric

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Abstract—Ferroelectric field effect transistors (FeFETs) are being actively investigated with the potential for in-memory computing (IMC) over other non-volatile memories (NVMs). Content Addressable Memories (CAMs) are a form of IMC that performs parallel searches for matched entries over a memory array for a given input query. CAMs are widely used for data-centric applications that involve pattern matching and search functionality. To accommodate the ever expanding data, it is attractive to resort to analog CAM for memory density improvement. However, the digital CAM design nowadays based on standard CMOS or emerging nonvolatile memories (e.g., resistive storage devices) is already challenging due to area, power, and cost penalties. Thus, it can be extremely expensive to achieve analog CAM with those technologies due to added cell components. As such, we propose, for the first time, a universal compact FeFET based CAM design, FeCAM, with search and storage functionality enabled in digital and analog domain simultaneously. By exploiting the multi-level-cell (MLC) states of FeFET, FeCAM can store and search inputs in either digital or analog domain. We perform a device-circuit co-design of the proposed FeCAM and validate its functionality and performance using an experimentally calibrated FeFET model. Circuit level simulation results demonstrate that FeCAM can either store continuous matching ranges or encode 3-bit data in a single CAM cell. When compared with the existing digital CMOS based CAM approaches, FeCAM is found to improve both memory density by 22.4× and energy saving by 8.6/3.2× for analog/digital modes, respectively. In the CAM-related application, our evaluations show that FeCAM can achieve 60.5×/23.1× saving in area/search energy compared with conventional CMOS based CAMs.

Index Terms—Ferroelectric FET, Content addressable memory

I. INTRODUCTION

Data transfer and processing is a bottleneck for the conventional Von-Neumann architecture in the era of big data. This is especially concerning for deploying applications such as deep learning on Internet-of-Things (IoT) devices, which typically demands real-time processing and power efficiency while constrained by power and computation resources. Therefore, in-memory computing (IMC) that helps reduce data movement and address the memory challenge are being extensively explored.

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Content addressable memories (CAMs) are a special form of IMC circuits widely used in high-speed searching applications, e.g., network routing and CPU caching [1]. As shown in Fig. 1, CAM can compare input query against a list of stored data in parallel, and return the address of matching data or the stored data itself. Thanks to high parallelism and in-memory computation, CAMs have found new utility in emerging deep learning applications [2], [3]. However, there exists two practical challenges preventing the deployment of conventional CMOS static random access memories (SRAMs) based CAMs for deep learning (especially on IoT devices): (1) non-trivial power consumption [4]; and (2) large area overhead (16 transistors per cell) [5].

To address the aforementioned issues of power and area penalties for SRAM based CAM, recent research efforts have been devoted to exploit emerging nonvolatile memories (NVMs) for CAM designs, including resistive RAM.
(ReRAM) [6], magnetic tunnel junction (MTJ) [8], and ferroelectric FET (FeFET) based Ternary CAM (TCAM) cells [9], [10]. These NVM-based CAM designs can help reduce area and power consumption while enabling acceleration of various neural network architectures [2], [11]. MTJ based CAM designs, e.g., 9T-2MTJ CAM cell [12], mitigates the memory density bottleneck, but the small $R_{ON}/R_{OFF}$ ratio and large write power of MTJs significantly degrades the CAM performance. The CAM designs based on resistive memory devices, including ReRAM [7] and phase change memory (PCM) [6], are advantageous in memory density, but have limited $R_{ON}/R_{OFF}$ ratio and significant write power, which is challenging to overcome. In addition, the design also incurs additional complexity and cost due to the necessity of connecting transistors to the back-end-of-line storage elements. Given those challenges, we have designed an ultra-compact 2FeFET based digital TCAM cell by exploiting the large $R_{ON}/R_{OFF}$ ratio, high $R_{OFF}$, three terminal device structure and highly energy-efficient electric field driven write mechanism of FeFETs [2], [10]. Therefore, ferroelectric TCAM is highly promising as the most competitive binary/ternary digital CAM candidate [10], [13].

However, most of the proposed CAM designs to date only support digital storage and search functionality [6], [7], [9], [10], [12], [14], limiting the CAM density and its functionality. As illustrated in Fig. 1(a), only binary or ternary values are stored and searched in a digital CAM, where the matching cells are colored in green and mismatching cells in red. To avoid the aforementioned limitations, there is a strong need to go beyond binary/ternary CAM by enabling analog search and storage functionality for CAMs. An analog CAM can store and search analog values within a continuous range, as shown in Fig. 1(b). By exploiting the MLC states in NVMs, such as ReRAM, an analog CAM stores quantized upper and lower bounds of a continuous range, which defines the continuous interval for searching. Therefore, multiple bits can be encoded as the number of non-overlapping continuous ranges for searching (e.g., 3 bits per cell means 8 non-overlapping continuous ranges, as shown in Fig 1(b)), thus improving the memory density compared with its binary/ternary digital CAM counterparts and expanding the functionality. Highly promising as it is, designing analog CAMs can be challenging especially when the following characteristics are desired:

- **Universal:** In near-term applications, digital CAMs, rather than analog CAMs, are dominating CAM based applications. However, to accommodate the data explosion for future scenarios, it is essential to have the analog CAM design that provides scalable direct analog processing capability for energy and area efficient processing. The analog CAM design based on ReRAM [15] adopts a different structure from its digital counterpart, thus incurring significant additional cost when both digital and analog specialized CAM designs are required. Therefore the integration of both digital and analog modes can be complex and costly, if not impossible, in implementation. An efficient and universal CAM implementation has never been created so far;

- **Compactness:** To achieve high CAM density, minimum (ideally none) transistor overhead is desired to augment a single digital CAM cell to achieve analog functionalities, especially for two-terminal NVM devices. For example, ReRAM based analog CAM design [15] employs 6 transistors and 2 ReRAMs for just one analog CAM cell, consuming a significant area overhead.

Thus, it is highly desirable to have a universal and compact CAM design solution that addresses the aforementioned challenges. In this work, we propose, for the first time, an FeFET based universal and compact CAM design, FeCAM, which can simultaneously serve as a digital and an analog CAM without any area overhead. Utilizing an experimentally calibrated FeFET model [16], we have performed device-circuit co-design approach of FeCAM. We show that by leveraging the MLC states in FeFETs, a 2FeFET based CAM design with analog search and storage capabilities is possible. By integrating the proposed analog CAM design with the digital CAM design in [10], our proposed analog CAM design can be expanded to an universal CAM design. As a result, our proposed universal and compact CAM is a highly competitive candidate for associative memory, allowing denser memory density (60.5×), more energy efficiency (23.1×) and flexible digital/analog processing in CAM-related applications compared with conventional CMOS based CAMs.

### II. Analog States in FeFET

The recent discovery of ferroelectric HfO$_2$ has spurred intense research activities in designing CMOS-compatible and high density FeFETs for nonvolatile memory applications [18].
The device operates by applying positive/negative gate pulses to set the ferroelectric polarization direction pointing toward the channel/gate metal direction, setting the FeFET to the low-$V_{TH}$ and high-$V_{TH}$ state, respectively. Unlike other types of NVM devices requiring a large DC conduction current for memory write, a FeFET exhibits superior write energy efficiency since it only relies on the electric field to switch the polarization. Though most of the current research efforts have been focusing on the binary memory property [13], [19], ferroelectric multi-level cell (MLC) has been studied to increase the memory density [20], [21]. Further device optimization and innovation in the future are likely to be conducted to further boost FeFET memory performance.

The intermediate $V_{TH}$ states between the low-$V_{TH}$ and high-$V_{TH}$ states have also been utilized for the design of synaptic weight cell in neural network accelerators [22], [23]. The intermediate states are obtained through partial polarization switching, which can be induced by varying applied pulse amplitude or pulse width, as illustrated in the metal-ferroelectric-metal (MFM) capacitor shown in Fig. 2(a). Ferroelectric HfO$_2$ thin film is composed of multiple domains with a distribution of their coercive field [17]. Different pulse amplitudes samples different portions of that distribution, inducing partial polarization switching. Fig. 2(c) shows the measured intermediate polarization states in a 10nm Hf$_{0.5}$Zr$_{0.5}$O$_2$ MFM capacitor, whose $Q_{FE}$-$V_{FE}$ hysteresis loop is shown in Fig. 2(b), under pulse trains with increasing amplitudes. The MFM device details are presented in [17]. These intermediate polarization states lead to different $V_{TH}$ states in a FeFET, as shown in Fig. 3.

The experimentally measured $I_D$-$V_G$ transfer characteristics of FeFET written with pulses of increasing amplitudes are shown in Fig. 3(b). The FeFET details are presented in [18]. The device $V_{TH}$ is gradually reduced with increasing pulse amplitudes. Fig. 3(c) shows the simulated transfer characteristics of a calibrated FeFET compact model [16], which qualitatively reproduces the experimentally observed FeFET analog properties. This model is used for the demonstration of the FeCAM in this work. With the demonstrated analog states in FeFET, the FeFET based CAM can provide a viable solution to the analog CAM design. We describe below our proposed FeFET based universal and compact CAM design integrating both analog and digital modes.

III. FeCAM DESIGN AND OPERATION

A. Operating Principles of FeCAM

FeCAM is universal in that it can simultaneously function as digital and analog CAM. Fig. 4(a) shows the schematic of the proposed FeCAM cell, which consists of only 2 FeFETs. The gates of the FeFETs connect to the searchline $SL$ and inverted searchline $S\bar{L}$. The $SL$ is generated from the $SL$ using a clocked inverter (Fig. 4(a)). Since the input of the FeCAM cell is an analog value, an analog inverter with a large transition window in the transfer characteristic is desired. The clock-gated PMOS in Fig. 4(a) is used to precharge the matchline $ML$ before the search operation. A sense amplifier (SA) consisting of three buffers is applied. Fig. 4(b) illustrates conceptually search and storage operations.

Since the digital CAM operations have been discussed in prior works [2], [10], here we only focus on the analog operations of CAM. Each FeCAM cell can store a continuous range of values, which is defined by an upper bound and a lower bound, for matching against the input voltage $V_{SL}$ as shown in Fig. 4(b). When the $V_{SL}$ is smaller than the range
upper bound, defined by the blue FeFET (Fig. 4(a)), the blue FeFET is turned off, causing negligible discharge current from ML and hence leaving ML high. When \( V_{SL} \) is larger than the upper bound, the blue FeFET turns on, discharging ML and hence leaving ML low. Due to symmetry, the same behavior can be observed for the red FeFET, with respect to its own gate voltage, \( V_{TH} \). When plotted as a function of \( V_{SL} \), however, its characteristic is flipped horizontally, forming the lower bound for the voltage range. The interval between the two bounds represents the stored voltage range for search. When \( V_{SL} \) is between the lower and upper bounds, neither of the device is turned on, resulting in a match output for a range of \( V_{SL} \) values. When \( V_{SL} \) is outside the defined bound, one of the two FeFETs turns on and discharges ML. As a result, the cell keeps the SA output at high level only when the input \( V_{SL} \) falls between the bounds. By properly adjusting the \( V_{TH} \) of the FeFETs using the partial polarization switching in Sec. II, thus shifting the upper and lower bounds, FeCAM allows continuous range storage and searching in multiple bounded regions, as shown in Fig. 4(c). These bounds are determined by the two FeFETs \( V_{TH} \). As a result, the number of \( V_{TH} \) levels corresponds to the number of discrete upper/lower bounds, thus enabling multi-bit quantized range searching (e.g., 8 different upper/lower bounds correspond to 3 bits quantized range searching).

B. FeCAM Cell Characteristics

Fig. 5(a) demonstrates the transient waveforms obtained from SPICE simulations for the search operation in an FeCAM cell. The sense amplifier output at three different input voltages \( (V_{SL}=0.3V, 0.5V, 0.7V) \) are shown, corresponding to below the lower bound, within the bound, and above the upper bound, respectively. The search operation of the FeCAM cell starts after the precharge phase, where the clock signal \( CLK \) is low. The inverter that drives the inverted searchline \( SL \) is powered by \( CLK \). When \( CLK \) transits to high, the circuit starts to perform the search operation based on \( V_{SL} \). From Fig. 5(a), after a search operation begins, the SA output stays high when \( V_{SL} \) is at 0.5V (within the bound), indicating a match, but falls to low when \( V_{SL} \) is at either 0.3V (below the lower bound) or 0.7V (above the upper bound) for a mismatch. The transient SA outputs for \( V_{SL} \) across the entire voltage range is shown in Fig. 5(b). It suggests that the search result (i.e., whether the search voltage is within the stored range or not) can be measured from the transient SA output at a certain time point following the search, where the voltage difference (i.e., sensing margin) between a match and a mismatch is large enough for sensing. The simulated SA outputs at 10ns following the search operation for different \( V_{SL} \) is shown in Fig. 5(c), indicating that the example FeCAM cell stores a continuous voltage matching range of (0.4V, 0.6V).

Moreover, since the lower and upper bounds of the CAM cell can be independently configured by programming the two FeFETs, respectively, as illustrated in Fig. 5(c), the CAM cell can be configured, according to the FeFET characteristics (Fig. 5), to match multiple continuous ranges with discrete upper/lower bounds. Fig. 5(d) demonstrate eight ranges, corresponding to 3-bit discrete upper/lower bound levels. This multi-bit storage can greatly improve the FeCAM information density at a minimal hardware cost. The operating principle and simulations of FeCAM presented above clearly demonstrate that the proposed FeCAM cell implements the desired analog search functionality and can be used as both a digital and analog CAM.

C. FeCAM Array Characteristics

The design of a single FeCAM cell and its operation in Sec. II-A and II-B clearly demonstrate the capability of multi-bit storage and search at the cell level. However, when extending from the cell to the array level, the parasitics and accumulated signal deterioration may actually prevent distinguishing different states, causing search failure at the array level. In this subsection, we provide design guidelines to ensure correct search and storage functionality at the array level without incurring additional design cost. Before presenting the details, we first discuss the multi-bit search behavior of FeCAM in large arrays.

We simulated the FeCAM arrays based on the array architecture shown in Fig. 6(a). We vary the number of rows and columns to investigate the impact of array size on the multi-bit search and storage functionality. The wiring parasitics at the FeCAM array are extracted from DESTINY [24]. As shown in Fig. 6(a), the proposed FeCAM array cells can operate in both digital and analog mode simultaneously even at the granularity of single cell level, depending on the write schemes applied. This is quite different from the previous CAMs that can only be either digital or analog [6]–[10], [12], [15], where only one type of value is stored and searched. Such
universal operating mode of FeCAM may enable efficient data analytic applications where both exact search (digital mode), approximate search (analog mode) functions are desired.

Fig. 6(b) summarizes the write operations of the FeCAM array. In addition to the write scheme for the digital mode of FeCAM similar to [10], we propose the write scheme for the analog mode of FeCAM array. It is based on the inhibition bias schemes, \( V_{W}/2 \), presented in [25]. The write for FeCAM array is conducted row-wise, namely one row is written at a time. For the selected row to be written, write pulses are applied to the associated \( SL \) and \( SL \) according to the FeFET characteristics shown in Fig. 3(c), and the associated source lines, \( ScLs \), are grounded, so that the corresponding write voltage values are applied to the targeted devices. For the unselected rows, the associated \( ScLs \) are set to 2V or -2V depending on the analog state to be written to the cell in the selected row and the same column. Since the max voltage of the write pulses is 4V, the gate-source voltages of the FeFETs in unselected cells should not exceed 2V. It has been shown that with write voltage of less than 2V, the FeFET state can be free from the disturbance [25]. Without loss of generality, we simplify the array write operation by applying the same write pulse to all cells, so that each cell stores the same matching range for the search operation.

During the search phase, we sweep all the search line associated with the array cells from 0 to 1V, and plot the transient SA outputs vs different \( V_{SL} \) values similar to Fig. 3(b). The search time of the array is determined according to the time required to maintain the pre-defined matching range stored in the cells. The results are demonstrated in Fig. 6(c-f). It is found that with the same search time, the FeCAM storage and search functionality is not significantly affected by the number of rows in the FeCAM array (Fig. 6(c) and 6(d)), which is reasonable as the parasitics associated with search lines (i.e., the FeFET gates) have negligible impact on the matchline. However, on the column line, the increasing number of columns equivalently adds additional discharge paths to the matchline, thus inevitably affecting the matchline discharge rate.

To ensure the matching range integrity as the number of columns increases, we propose to adapt the search time according to the different number of columns, which can be pre-characterized at the design time. In this way we can still keep the same matching bounds and the storage capability. Specifically, the associated capacitance of a matchline grows linearly with the number of columns as in Eq. 1.

\[
C_{ML} \approx C_{PMOS} + N \times (C_{\text{drain}} + C_{\text{parasitic}})
\]  

(1)

where \( C_{ML} \), \( C_{PMOS} \), \( C_{\text{drain}} \) and \( C_{\text{parasitic}} \) are the associated capacitance of the matchline, drain capacitance of the precharge PMOS, total drain capacitance of a FeCAM cell, and the parasitic capacitance of the interconnect for each cell, respectively. \( N \) is the number of columns in the array. The discharge time \( \Delta t \) for the matchline to drop by \( \Delta V_{ML} \) is described as in Eq. 2 and 3.

\[
\Delta t = \frac{C_{ML} \times \Delta V_{ML}}{\sum I_{\text{discharge},i}} = \frac{C_{ML} \times \Delta V_{ML}}{N \times I_{\text{discharge}}}
\]  

(2)

\[
\Delta t \approx \frac{\Delta V_{ML}}{I_{\text{discharge}}} \times (C_{PMOS}/N + C_{\text{drain}} + C_{\text{parasitic}})
\]  

(3)

where \( I_{\text{discharge},i} \) is the \( i_{th} \) single cell discharge current when the corresponding search line input \( V_{SL,i} \) is at the boundary of the stored value range, and \( I_{\text{discharge}} \) denotes as the average discharge current per cell from matchline to ground during the search. As the search time follows the same trends as the discharge time \( \Delta t \), Eq. 2 shows that the search time should be decreased as the number of columns increases in order to keep the upper and lower bounds of the matching range for the FeCAM array. We can use the Eq. 3 to set the search time for a given number of columns to ensure the same matching bounds and storage capability. Fig. 6(c) and 6(f) summarizes the results for the matching bounds and the corresponding search time, respectively, which is consistent with the analysis above. It can be anticipated that as the number of columns increases, the search time will eventually reach a bound.

IV. EVALUATION AND Benchmarking

In this section we benchmark the performance of the proposed FeCAM design in terms of its area, search energy, search delay, etc. We also present a straightforward application of FeCAM in implementing a routing look up table for high-performance routers.
2.78 TCASII '17, this work
53.9 CICC '06, 47.2 VLSI Symp. '06
22.4 JSSC '08, 1.69 JSSC '13
10.74 JSSC '11, 17.1 CICC '04
6.73 CICC '03, 19.5 JSSC '09

250     180     130       90       65      45
2FeFET
(Nonvolatile)
10T-4MTJ
(Nonvolatile)

17.5 JSSC '03
1.12  projection
Digital 
TCAM
Analog 
CAM

A. FeCAM Cell

As discussed in Sec. III-B, the analog mode of FeCAM can encode multiple bits. We sketch the layout of the 2X2 FeCAM array in Fig. 7(a), estimate the area per bit of FeCAM and compare the results with other existing TCAM work in Fig. 7(b). Since previous sections suggests that the analog mode of FeCAM is capable of storing continuous range for matching with 8 discrete upper/lower bound levels in one cell, which is equivalent to the functionality of 3 TCAM cells, the area per bit of our FeCAM is 1/3 of that of the 2FeFET TCAM cell in [2], [10]. Fig. 7 shows that the area per bit of the analog mode of FeCAM is just 4.5% of that of a projected 16T CMOS TCAM design at 45nm technology node as red starred in the chart. This area efficiency can enable compact CAM arrays, where fewer cells per row and fewer rows are required than a digital CAM design to store the same number of bits data. We present an IP router example as in Sec. IV-B.

3In this paper we use 3-bit/cell, as experimental proof of the 3bit FeFET memory device has already been reported [21], further design and write scheme optimizations can enable more improvements in the memory density.

B. FeCAM Application

We perform a thorough study on FeCAM, and compare it with the conventional CMOS TCAM at array and application levels. We evaluate the search energy per bit for CMOS TCAM, digital and analog modes of FeCAM assuming 64-cell, 64-, and 22-cell (one cell storing 3 bits) word sizes, respectively. We use an IP packet classification case to demonstrate the efficiency of FeCAM over other CAMs. While a typical CMOS 16T CAM array consumes 0.590 fJ/bit for the array search, the proposed FeCAM array can achieve 0.182 fJ/bit under digital mode (3.2× reduction w.r.t. CMOS TCAM) and 0.069 fJ/bit under analog mode for 3-bit search (8.6× reduction w.r.t. CMOS TCAM). Thus, the proposed FeCAM can provide not only stronger search capability and better memory density, but also more energy saving. Note that the current design and simulations mainly validate the functionality of FeCAM analog mode concept, while FeCAM can be further optimized w.r.t. energy and performance.

Without loss of generality, a representative application of CAM array is demonstrated for IP address routing table in network devices (Fig. 8). As shown in Fig 8(a), a routing table with 24 bits routing prefix is considered, corresponding to 24 leading 1-bits in the subnet mask. A randomly chosen IP address range from 98,305 to 14,712,838 is then implemented in CMOS TCAM and FeCAM array, respectively, as shown in Fig. 8. To cover that range, 27 digital TCAM entries are necessary with 24 cells per entry; whereas only 10 entries and 8 cells per entry are required for a 3 bits/cell analog FeCAM array, indicating a considerable reduction (8.1×) of the array cells compared with the CMOS equivalent. Taking the cell area into consideration, the area and energy reduction of FeCAM based routing table can be 60.5× and 23.1× respectively, compared with the CMOS TCAM based routing table. These savings can be further improved by designing a 4 bits/cell analog FeCAM through device and design level optimization.

Fig. 8. Implementing a routing table covering a randomly chosen IP address range from 98,305 to 14,712,838 in the 24 bits IP address space with (a) binary/ternary CAM array; (b) 3 bits/cell analog FeCAM array. (c) Up to 8.1x reduction in the number of CAM cells can be achieved with FeCAM.

Fig. 7. (a) 2X2 FeCAM array layout. Note that Λ represents half feature size $F$; (b) Comparisons of CAM cell area overhead per bit.
V. DISCUSSIONS

In summary, compared with the prior CAM designs, the proposed FeCAM are featured with: (1) Higher flexibility. With the same CAM cell structure, FeCAM can function as both digital and analog CAMs depending on the write and search schemes; (2) Better array scalability. The increasing size of the FeCAM array will not affect the functionality of both digital and analog CAM functionality, which is explained in Sec. III-C; (3) Superior Energy efficiency. Due to the superior energy-efficient electric field driven write mechanism of FeFETs, FeCAM can exhibit ultra-low write energy consumption. On the other hand, the reduced number of CAM cell in analog FeCAM compared with its digital counterpart also reduces the search energy consumption; (4) Higher memory density. Sec. III-B shows that per FeFET controllable programming characteristics, a 3-bit data storage and search functionality can be achieved in the analog mode of FeCAM; (5) Direct analog signal processing capability. The analog mode of FeCAM enables novel computing functionality in analog domain, allowing the direct analog signal processing without analog to digital conversion, which may be very promising in IoT sensor scenarios.

This work represents an early exploratory device-circuit co-design of a universal FeCAM cell, which focuses on the demonstration of working principles of FeCAM cell and array. The non-idealities of FeFET technologies are not the focus of this work, but they are highly important for practical implementation of FeCAM. Given that HfO$_2$ based FeFET is still in its early development stage, several challenges still exist for this technology, especially for the analog/MLC states utilized in this work. The most important aspect is the degraded device-to-device variation for scaled FeFET [26]. Significant variation would limit the number of distinct upper/lower bounds that can be faithfully achieved in a FeCAM array. Improvement in this direction is still under intensive research. But several promising results have been demonstrated so far. For example, excellent cycle-to-cycle variation has been shown in a reasonably small (W/L=500nm/500nm) FeFET with 3 bits per cell [27]. For a large FeFET (W/L=10µm/10µm), even 3 bits per cell with well controlled device-to-device variation has been demonstrated [21]. Another aspect is about the endurance of FeFET, which is limited to be around $10^5$ cycles [18]. But as discussed in [2] for digital FeCAM, the CAM applications, in general, may not require frequent write operations, as the search operations would likely be the most frequent, which is just FeFET read operations. Moreover, novel ferroelectric memory device structure is also actively pursued to bridge the endurance gap of FeFET and intrinsic ferroelectric [28]. Therefore, based on the discussions above, the benefits of the proposed FeCAM can be fully exploited with FeFET technology given the device improvement in the future.

VI. CONCLUSION

In this paper, we proposed a universal and compact CAM to support simultaneous digital and analog modes by exploiting the programmable analog/MLC states of FeFETs for the first time. A conceptual demonstration of analog CAM, as well as a FeFET based CAM cell design have been demonstrated. Practical simulations show that the proposed FeCAM can encode multiple continuous ranges for matching with discrete upper/lower bound levels using just 2 FeFETs, thus significantly improving the memory density, area and energy efficiency compared to the conventional 16T CMOS TCAM. This universal CAM design with both digital and analog search capabilities enables the compact memory array as well as flexible digital and analog signal processing in sensors, which is particularly critical for IoT applications.

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