Superconducting V₃Si for quantum circuit applications

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V₃Si thin films are known to be superconducting with transition temperatures up to 15 K, depending on the annealing temperature and the properties of the substrate underneath. Here we investigate the film structural properties with the prospect of further integration in silicon technology for quantum circuits. Two challenges have been identified: (i) the large difference in thermal expansion rate between V₃Si and the Si substrate leads to large thermal strains after thermal processing, and (ii) the undesired silicide phase VSi₂ forms when V₃Si is deposited on silicon. The first of these is studied by depositing layers of 200 nm V₃Si on wafers of sapphire and oxidized silicon, neither of which react with the silicide. These samples are then heated and cooled between room temperature and 860 °C, during which in situ XRD measurements are performed. Analysis reveals a highly non-linear stress development during heating with contributions from crystallization and subsequent grain growth, as well as the thermal expansion mismatch between silicide and substrate, while the film behaves thermoelastically during cooling. The second challenge is explored by depositing films of 20, 50, 100 and 200 nm of V₃Si on bulk silicon. For each thickness, six samples are prepared, which are then annealed at temperatures between 500 and 750 °C, followed by measurements of their resistivity, residual resistance ratio and superconducting critical temperature. A process window is identified for silicide thicknesses of at least 100 nm, within which a trade-off needs to be made between the quality of the V₃Si film and its consumption by the formation of VSi₂.

I. INTRODUCTION

Quantum technologies based on solid state matter are now spreading from academic laboratories to the most advanced semiconductor foundries.¹,² Among the materials to be integrated, superconducting thin films are of major interest as they are part of many quantum architectures. For instance, such films can be used to manipulate, read and couple superconducting or spin qubits with the use of superconducting resonators³,⁴ are developed for non-dissipative interconnections or can even be part of the quantum device itself when integrated as source and drain contacts of CMOS transistors. Since silicon technology is by far the most advanced method of nanofabrication, it is important to identify superconducting materials that are fully compatible with such an environment. Among these, silicides appears as the most suitable materials⁵,⁶, and as V₃Si has the highest known critical temperature of any silicide known so far⁷,⁸, it is a prime candidate for these applications. In working towards integration of V₃Si, two key problems have been identified: (i) a reduction in the superconducting critical temperature due to increased thermal strain after annealing⁹, and (ii) the formation of the non-superconducting phase VSi₂ at the interface with a silicon channel or substrate.

In systems where reservoirs of both Si and V are available, the undesired phase VSi₂ is expected to form, which is both the first phase to nucleate and is thermodynamically favored.¹⁰ This rules out the self-aligned silicide (SALICIDE) process for the formation of the desired V₃Si, in which pure metal is deposited on exposed silicon contacts. Instead, it has motivated the adoption of V₃Si sputtering from compound targets¹²,¹³, after which an annealing step is required to trigger the crystallization. This thermal processing leads to the build-up of strain in the final silicide film, which is known to negatively affect its critical temperature¹⁴–¹⁹. Earlier work has shown that this strain depends strongly on the mismatch in thermal expansion coefficient (TEC) between the silicide and the substrate, and can lead to a suppression in superconducting critical temperature Tc by 2 K on silicon.²⁰ Section II provides a detailed analysis of the impact of crystallization, grain growth and thermal expansion mismatch on the strongly temperature-dependent development of stress in V₃Si thin films.

Besides causing the buildup of large tensile stresses, thermal processing of V₃Si on silicon substrates also leads to the formation of VSi₂. The presence of VSi₂ at the interface between the superconducting V₃Si and the Si substrate may not be a problem per se. It is imperative, however, that a layer of V₃Si with a thickness on the order of its superconducting coherence length remains. The simultaneous formation of the two silicide phases after the deposition of amorphous V₃Si on bulk silicon wafers is discussed in section III. We find that when 50 nm or less of V₃Si is deposited, no superconductivity is observed after crystallization annealing. For layers of 100 or 200 nm, the superconducting critical temperature of the film is found to initially improve with annealing temperature, until at some point superconductivity disappears when all V₃Si is consumed by a growing layer of VSi₂.

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II. IN-SITU XRD ANALYSIS

Sputtering a V₃Si target leads to the deposition of an amorphous layer of the desired intermetallic compound which presents superconductivity at temperatures of around 1 K, far below that of the crystalline form (measured but not shown). In order to nucleate the crystalline V₃Si phase, heat has to be applied. During the experiment described in the present section, the V₃Si was isolated from any potential element (V and Si especially) that would affect the crystallization phenomenon. Thus, depositing the intermetallic compound on oxides (silica and sapphire) offers the possibility to study the isolated film by itself, affected by the substrate only mechanically. The evolution of the stresses in the V₃Si film as a function of the annealing temperature was monitored by in-situ X-ray diffraction (XRD) using a Smartlab Rigaku X-ray diffractometer equipped with a copper (Cu Kα) source, a punctual detector and a DHS 1100 Anton Paar furnace using a nitrogen atmosphere at a pressure slightly above ambient, i.e. 1.25 bar, to avoid atmospheric contamination.

Layers of 200 nm V₃Si were deposited on two types of substrates: oxidized silicon with a 20 nm thick surface oxide, and sapphire. Both in-plane and out-of-plane XRD measurements were performed on different samples of each substrate. For both measurements, a parallel slit analyzer with an angular aperture of 0.114° for out-of-plane measurement and 1° for in-plane ones, is positioned in front of the detector in order to be insensitive to peak shift due to the radial displacement of the sample induced by thermal expansion of the sample holder. This way, the observed peak shift is only related to a real d-spacing variation. For both measurements, 2θ–ω scans around the V₃Si (210) close to 2θ = 43° were performed. Profiles were acquired while heating the samples from 50 °C up to 860 °C and then during cooling from 860 °C to room temperature. The temperature profile versus time is given in Fig. 1.

Peak fitting was performed with the HighScore Plus software from PANalytical, from which the d-spacing and the integral breadth of the V₃Si (210) peak were considered. The V₃Si crystallization followed by in-situ XRD is shown as a contour map for the out-of-plane measurements in Fig. 2 and the in-plane measurements in Fig. 3.

During heating, for both substrates, a characteristic peak of (210) V₃Si is observed above 500 °C, which marks the crystallization temperature of the as-deposited amorphous V₃Si layer. One can thus deduce that the nucleation temperature of V₃Si crystalline phase is close to 500 °C. From in-plane and out-of-plane peak positions, one can extract the stress and the temperature-dependent stress-free lattice parameter of the layer. Assuming a bi-axial state of stress in the layer, it can be deduced following the sin²ψ methodology:

\[
\varepsilon_\psi = \frac{(d_\psi - d_0)}{d_0} = \frac{1}{2} S_2(hkl) \sigma \sin^2 \psi + 2 S_1(hkl) \sigma, \tag{1}
\]

where \( \sigma \) is the in-plane bi-axial state of stress, \( \varepsilon_\psi \) and \( d_\psi \) are the strain and the d-spacing along the direction \( \psi \), respectively, \( d_0 \) is the stress-free d-spacing and \( \psi \) is the angle between the considered direction and the normal to the surface. \( \frac{1}{2} S_2(hkl) \) and \( S_1(hkl) \) are the X-ray Elastic Constants.
(XEC) for the hkl plane considered. The XEC can be easily calculated\textsuperscript{21} by knowing the single-crystal elastic constants of the V\textsubscript{3}Si structure\textsuperscript{22}. For the (210) plane, using the arithmetic average of the Voigt and Reuss XEC, known as the Neerfeld limit, we found $\frac{1}{2} S_2(210) = 6.69 \times 10^{-6} \text{MPa}^{-1}$ and $S_1(210) = -1.66 \times 10^{-6} \text{MPa}^{-1}$. The in-plane stress is then given by\textsuperscript{20}

$$\sigma = \frac{2}{S_2(hkl)} \left( d_{\parallel} - d_0 \right)$$

(2)

and the stress-free d-spacing, $d_0$, by

$$d_0 = \frac{d_{\perp} - Ad_{\parallel}}{1 - A}, \quad \text{where} \quad A = \frac{4S_1(hkl)}{S_2(hkl) + 4S_1(hkl)}.$$  

(3)

In Fig. 4a, the stress evolution deduced from this analysis is plotted versus the annealing temperature for both types of substrate. In both cases, the initial stress at crystallization is highly tensile, around +1500MPa. This is in agreement with the expected volume shrinkage that occurs during the crystallization, assuming that the density of the amorphous phase is smaller than the density of the crystalline phase. This tensile stress is then partially relaxed.

In Fig. 4c,d the integral breadth (IB) evolution of the (210) peak vs annealing temperature is plotted, which can be correlated to the crystallite size through the Scherrer equation\textsuperscript{23,24}. This figure shows that the IB is high at the crystallization temperature and then goes down with increasing temperature, a behavior that is similar for the in-plane and out-of-plane directions, and can be interpreted as a crystallite size increase. However, one should note that the in-plane and out-of-plane setup was different and can not be compared directly.

Indeed, for the in-plane setup, the IB decreased down to 1° at 650°C and stayed constant during further annealing. This value of 1° is the instrumental width given by a silicon reference powder, which implies that the in-plane crystallite size is very large above 650°C and can no longer be estimated from IB broadening. As we observe an increase of the crystallite size out of plane up to 860°C, we may assume that the lateral crystallite size also continues to grow up to this temperature. In the case of the out-of-plane measurements, the setup was more accurate, and the estimated crystallite size is about 30nm for the highest annealing temperature. It can clearly be concluded that there is a strong anisotropy in grain size on both substrates. On both substrates, the in-plane IB stabilizes at 650°C due to saturation of the instrument resolution, while the detected out-of-plane crystallite size increases continuously to the maximum temperature of the experiment.

During cooling, the stress evolution exhibits a linear behavior, in agreement with a pure thermoelastic stress induced by the TEC mismatch between the film and the substrate. This is confirmed by looking at the in-plane lattice parameter evolution with temperature (Fig 4b). The behavior is linear as expected, but more interestingly, the slope of these straight lines is $7.3 \times 10^{-6} \text{°C}^{-1}$ and $4.2 \times 10^{-6} \text{°C}^{-1}$ for the sapphire and Si substrate respectively, in good agreement with the in-plane TEC of (0001) sapphire ($6.5 \times 10^{-6} < \alpha < 7.6 \times 10^{-6} \text{°C}^{-1}$ in the temperature range 300–800°C)\textsuperscript{25}, and with the TEC

![FIG. 4: (a) Stress evolution versus annealing temperature for both the sapphire and the silicon substrates. (b) Strain of the V\textsubscript{3}Si layer versus the annealing temperature during cooling. (c,d) Out-of-plane and in-plane integral breadth of the V\textsubscript{3}Si (210) peak versus annealing temperature.](image-url)
of Si \( (3.6 \times 10^{-6} < \alpha < 4.3 \times 10^{-6} \text{C}^{-1}) \) in the temperature range \( 200-800 \text{C} \). From the stress-free lattice parameter extraction, we calculated a TEC of the \( V_3\text{Si} \) phase of \( 9.2 \times 10^{-6} \text{C}^{-1} \). The TEC mismatch between the film and the substrate should therefore have added a tensile stress to the stress measured at 860 °C, in agreement with the observation in Fig. 4a. As expected, since the TEC mismatch is larger with the Si substrate than with the sapphire, the tensile stress increases faster on Si than on sapphire. Extrapolating this thermoeleastic behavior to the device operating temperature (i.e. a few K), a stress level of 0.87(7) GPa is obtained for \( V_3\text{Si} \) on sapphire and 0.91(3) GPa for \( V_3\text{Si} \) on silicon. Of course these values depend on the initial residual stress before cooling, and thus on the thermal budget applied to the samples. Since the slow cooling occurred entirely thermoelectrically and followed the TEC of the substrate, it is not expected that the rate of cooling has any impact on the final stress obtained. The difference in room-temperature strain between this report and those found in earlier experiments where in-situ XRD analysis was performed up to 1000 °C is thus attributed to differences in the maximum temperature that was reached.

III. COMPETITION BETWEEN \( V_3\text{Si} \) AND \( \text{VSi}_2 \) FORMATION

A second set of experiments was performed to study the stability of the superconducting \( V_3\text{Si} \) phase on a silicon substrate. After sputter deposition of \( V_3\text{Si} \) on a silicon substrate, an intermixing layer of Si and V can be expected to form where the atomic concentration of vanadium ranges from zero in the substrate to \( 3/4 \) within the deposited layer. Above this mixed zone, the precise matching of the deposited atomic ratio to the stoichiometry of \( V_3\text{Si} \) will prevent the formation of \( \text{VSi}_2 \). Within the mixed zone however, \( \text{VSi}_2 \) nucleation is likely to occur. Since this mixed zone is interfaced from below by pure silicon, and from above by \( V_3\text{Si} \), its disappearance or consumption by \( V_3\text{Si} \) formation would require that V move upwards while leaving progressively purified Si behind. Such movement is prevented by the chemical potential, as the thermodynamically stable state in the presence of excess silicon is for the vanadium to be bound in \( \text{VSi}_2 \). Furthermore, even if a V reservoir were present in the form of a superstoichiometric vanadium concentration (i.e. above 75%) in the deposited layer, it is unlikely that the mixed zone would be consumed by \( V_3\text{Si} \) formation. Since silicon is the dominant diffusing species in \( \text{VSi}_2 \) and at the V/Si interface, with diffusion rates of two orders of magnitude higher than that of V in \( V_3\text{Si} \), any part of the intermixing layer with lower vanadium concentration than that of \( V_3\text{Si} \) is expected to quickly extend downward and decrease in V content due to upward Si diffusion, preventing \( V_3\text{Si} \) growth and aiding the formation of \( \text{VSi}_2 \).

Once \( \text{VSi}_2 \) and \( V_3\text{Si} \) are both present, competition will arise between the further growth of either silicide. While \( V_3\text{Si} \) (\( V_{0.75}\text{Si}_{0.25} \)) has a larger effective heat of formation (EHF) from pure V and Si per mole of atoms involved in total \( 11 \), the energy gain per vanadium atom is greater for \( \text{VSi}_2 \) (\( V_{0.33}\text{Si}_{0.67} \)), of which three times as many molecules can be formed for a fixed amount of vanadium. When \( V_3\text{Si} \) interfaces with silicon, it is therefore energetically favorable for the following reaction to occur (EHF indicated below),

\[
V_3\text{Si} + 5\text{Si} \rightarrow 3\text{VSi}_2,
\]

where an energy of 181 kJ/mol is gained per mole of \( V_3\text{Si} \) that is transformed. Scanning electron microscope (SEM) images of the growth of the \( \text{VSi}_2 \) phase during thermal processing are shown in Fig. 5.

To study this interplay, a different set of samples was prepared in addition to those discussed in section II. Layers with thicknesses of 20, 50, 100 and 200 nm of \( V_3\text{Si} \) were deposited onto 200 mm (100)-oriented silicon wafers from a compound \( V_3\text{Si} \) target using RF magnetron sputtering equip-
ment. This target had a measured silicon content of between 22.7 ± 0.2 at.% (WDXRF) and 25.7 ± 0.2 at.% (supplier data), which could further differ from the final Si content in the deposited layer by 1 at.%\textsuperscript{13}. These wafers were cleaned with hydrofluoric acid (HF) before entering the sputtering chamber. Smaller pieces of 2 × 2 cm\textsuperscript{2} were then annealed during 2 minutes in a Jipelec furnace with a 20 °C/min ramp rate. For each thickness of V\textsubscript{3}Si, six different samples were thermally processed at temperatures between 500 and 750 °C, as indicated in Fig. 6. These samples were then characterized by measuring their room-temperature sheet resistance (corrected for their shape and size by calculating the sheet resistance ratio of multiple unannealed wafer-sized and 2 × 2 cm\textsuperscript{2} samples), and by following the resistance of smaller samples during slow cooling to cryogenic temperatures of 2 K in order to extract both the superconducting critical temperature and the residual resistance ratio (RRR).

At 500 °C, the resistivity of the thinner layers (20, 50 and 100 nm) was found to be comparable to that of as-deposited amorphous V\textsubscript{3}Si (180(10) µΩcm), while it exceeded this value by multiple orders of magnitude for the thicker layer of 200 nm (out of range for our instruments), as shown in Fig. 6a. For all thicknesses, the resistivity then decreased with annealing temperature, to values below that measured for a reference sample with 200 nm V\textsubscript{3}Si on non-reacting sapphire annealed at 900 °C (77.1 µΩcm, indicated as a red dashed line). Since this reference value is the lowest resistivity that we have found for any layer of crystallized V\textsubscript{3}Si, in a sample where we confirmed by XRD measurements that no other vanadium-rich compound was formed, we take any value lower than this on silicon substrates to indicate the presence of VSi\textsubscript{2}. The formation of VSi\textsubscript{2} was confirmed by XRD analysis and identified at the Si/V\textsubscript{3}Si interface by SEM imaging (see Fig. 5, bottom).

Smaller samples of 4 × 10 mm were then wire bonded for four-point resistance measurements during both cooling and heating between 300 and 2 K in a Physical Properties Measurement System (PPMS). The residual resistance ratio of each sample was calculated as the ratio between the resistances at 260 K and 20 K, shown in Fig. 6b. This ratio gives insight into the material properties of the silicide layer since the resistivity at low temperatures is dominated by impurity and defect scattering\textsuperscript{29}. For higher annealing temperatures the RRR is greater for thicker layers (with the exception of the 200 nm sample annealed at 750 °C, which is also an outlier in terms of resistivity), which is consistent with the lower quality of thinner films as reported before\textsuperscript{12}. After annealing at 550 °C, however, we find that the RRR is highest in samples where only 20 nm of V\textsubscript{3}Si was deposited, followed by 50 nm and 100 nm, in that order. This could be an indication that a nearly homogeneous VSi\textsubscript{2} layer has already started to form at the V\textsubscript{3}Si/Si interface in the thinnest of these films, with inhomogeneity increasing for thicker films of 50 and 100 nm. Complete homogenization of a 20 nm film during two minutes would suggest however that Si, the dominant diffusing species in VSi\textsubscript{2} formation\textsuperscript{27}, has diffused with a diffusivity of at least 1.8 nm\textsuperscript{2}s\textsuperscript{-1}, values that have only been reported for annealing temperatures of 650 °C\textsuperscript{30}. The higher RRR at 550 °C of the sample with 200 nm deposited V\textsubscript{3}Si suggests that this layer is too thick for diffusion to have already caused mixing throughout the entire film, and this relatively high value could be attributed to crystallization of V\textsubscript{3}Si.

The appearance of crystalline V\textsubscript{3}Si at temperatures of around 500 °C is consistent with the in-situ XRD analysis on non-reactive substrates discussed in section II (see especially Fig. 2). This is further corroborated by the appearance of superconductivity with critical temperatures above 2 K as shown in Fig. 6c, to be contrasted with the critical temperature of 0.9 K of amorphous 200 nm-thick V\textsubscript{3}Si layers on silicon sub-

![FIG. 6: (a) The resistivity of each annealed sample, the red dashed line indicates the lowest resistivity expected for V\textsubscript{3}Si (see main text). (b) The residual resistance ratio (RRR). (c) The critical temperature, taken to be the point where 50% of the normal-state resistance is lost, with error bars indicating temperatures at which 10% and 90% of normal-state resistance is observed. Arrows down (↓) indicate that the critical temperature (if any) is below 2 K.](image-url)
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strates prepared under identical conditions. A critical temperature of 10.62 K (10% and 90% transitions at 10.32 and 11.00 K, respectively) was attained after annealing at 650 °C in a 200 nm deposited film, identical to that obtained on samples where VSi$_2$ formation was prevented by a 20 nm film of SiO$_2$, with a superconducting transition that is only 12% wider. This suggests that the nearby formation of VSi$_2$ does not have a significant impact on the superconducting properties of the remaining V$_3$Si. Meanwhile, the absence of superconductivity above 2 K in samples with 20 or 50 nm deposited V$_3$Si, after annealing at any temperature, confirms that Si diffusion and VSi$_2$ formation rapidly remove V$_3$Si or even prevent its crystallization altogether in thinner films.

IV. DISCUSSION

Instead of forming vanadium silicide by reactive diffusion, V$_3$Si was directly sputtered from a compound target at the right stoichiometry, giving the advantages of having a sharp interface between the deposited layer and the substrate, and requiring no solid-state reaction to reach the desired phase. However, the interface must be better controlled in terms of impurities, and the V$_3$Si is amorphous after deposition. First, the crystallization was studied on 2 types of substrate, oxidized silicon with a 20 nm thick SiO$_2$ surface layer and monocrystalline sapphire (Al$_2$O$_3$). It was clear that no reaction occurred with either of these substrates at any temperature. Earlier work showed that the mismatch in TEC with the substrates strongly impacts the stress built up during the growth of V$_3$Si, which can lower the superconducting critical temperature.

Layer crystallization started at 500 °C, leading to high tensile stress on either substrate up to 650 °C. This stress then relaxed with increasing temperature, both due to atomic diffusion and the relatively low TEC of the substrates. From 650 °C to around 700 °C, an increase in tensile stress together with a decrease in the out-of-plane IB can be explained by grain growth in fair agreement with the model of P. Chaudan. During cooling, the V$_3$Si stress behavior matches perfectly with TEC of silicon and sapphire substrate, indicating a purely thermoelastic behavior. It is thus clear that the thermo-mechanical properties of the substrate strongly impact the stress evolution in the V$_3$Si film, which can be mitigated by proper choice of annealing conditions.

Since V$_3$Si is amorphous after deposition, crystallization by subsequent thermal processing is required to achieve the desired superconducting properties. However, on a silicon substrate this has the undesired side effect of VSi$_2$ nucleation. In fact, in the thinnest films that were studied, with 20 and 50 nm of deposited silicide, a nearly homogeneous VSi$_2$ layer had already started to form at the interface with the substrate before any crystallization of V$_3$Si was observed by critical temperature measurements. Full consumption of the deposited V$_3$Si occurred at higher temperatures between 600–650 °C and 650–700 °C for layers of 100 and 200 nm, respectively, allowing for V$_3$Si crystallization, as well as grain growth. The critical temperatures thus obtained on a silicon substrate prior to complete V$_3$Si consumption are identical, within experimental error, to those obtained on SiO$_2$, indicating no detrimental effect of diminished thickness or proximity to growing VSi$_2$ on the quality of the superconductor. This is in contrast with earlier results obtained by V$_3$Si sputtering from a compound target on heated Si substrates with 800 nm of thermal SiO$_2$, where a strong dependence of film thickness was found below 200 nm. This variation in thickness was at the time attributed to the presence of impurities such as oxygen, while earlier reports had argued that the chemical composition of the layer was unimportant, and any variations that it causes in $T_c$ are due to a change in lattice parameter. Since no reaction with the substrate occurs on SiO$_2$ (see Fig. 5), and the critical temperature is independent of the thickness of crystalline V$_3$Si itself, the reduced $T_c$ reported in this earlier study could also be attributed to differences in grain growth, or stress development during cooling from 560 °C, at which the layers were deposited, to cryogenic temperatures in the range of 10–15 K.

V. CONCLUSION

Superconducting thin films are of increasing interest as solid-state quantum technologies are scaled up. To facilitate large-scale fabrication, as well as co-integration with classical electronics, it is important that the choice of superconducting material is compatible with CMOS technology. This report addresses two challenges for the integration of V$_3$Si, which as a silicide with a superconducting critical temperature of up to 17 K is a natural candidate in this context.

The first is the reduction in critical temperature due to thermal strain. While V$_3$Si is compatible with the oxides of silicon and aluminum, both currently used in VLSI devices, it is necessary to mitigate the stresses induced by the interplay between crystallization, grain growth and TEC mismatch with the substrate. It is found that the final stress obtained on either substrate depends strongly on the thermal budget that the samples are subjected to, identifying annealing as a key process step to control the critical temperature of the film.

Second, thermal processing also provides a means of controlling the formation of the undesired phase VSi$_2$ on HF-cleaned silicon substrates. For V$_3$Si films with a thickness of 100 nm or more, there exists a process window where it can be crystallized before consumption by the VSi$_2$ phase, with a temperature range that depends on the thickness of the film.

Direct applications of V$_3$Si could be in high-frequency resonators on oxides or oxidized substrates, where the impact of a potential stress residual on the quality factor has to be evaluated. A further interest would be to fabricate Josephson junctions, where the weak link could either be an oxide in a vertical geometry, or silicon in a planar junction. In the latter case, a Josephson field effect transistor could be fabricated by forming V$_3$Si in the source and drain contacts of a CMOS transistor, in which case one is faced with a trade-off between improving the V$_3$Si critical temperature and limiting the growth of the VSi$_2$ phase.
VI. DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

VII. ACKNOWLEDGMENTS

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