Programmable skyrmion logic gates based on skyrmion tunneling

Naveen Sisodia, Johan Pelloux-Prayer, Liliana D. Buda-Prejbeanu, Lorena Anghel, Gilles Gaudin, and Olivier Boulle

Univ. Grenoble Alpes, CNRS, CEA, SPINTEC, F-38000 Grenoble, France
(Dated: May 18, 2022)

Magnetic skyrmions are promising candidates as elementary nanoscale bits in logic-in-memory devices, intrinsically merging high density memory and computing capabilities. Here we exploit the dynamics of skyrmions interacting with anisotropy energy barriers patterned by ion irradiation to design programmable logic gates. Using micromagnetic simulations with experimental parameters, we show that a fine tuning of the barrier height and width allows the selective tunneling of skyrmions between parallel nanotracks triggered by skyrmion-skyrmion interaction. This can be leveraged to design skyrmion De-multiplexer (DMux) logic gate which works solely using skyrmions as logic inputs. By cascading and connecting demultiplexer gates with a specific topology, we develop a fully programmable logic gate capable of producing any possible logic output as a sum of all minterms generated by a given set of inputs without requiring any complex additional electric/magnetic interconversion. The proposed design is fully conservative and cascadable and paves a new pathway for full skyrmionic-based logic-in-memory devices.

I. INTRODUCTION

The information technology industry is currently facing major challenges related to power dissipation and energy consumption [1, 2]. The conventional Moore’s approach of CMOS technology is currently out of breadth: the continuously decreasing size of the MOS transistors in the logic and memory units leads to critical power dissipation and energy consumption issues. Another major bottleneck relates to the Von Neumann architecture, in which the constant transfer of data between the memory and computing units leads to a considerable cost in energy and limited bandwidth. In addition, since the current technologies use volatile on-chip memory modules, the static power consumption used to maintain the stored data is significant even if state of the art low power strategies are used. Recently, logic-in-memory architectures, merging non-volatile memories and logic circuits, have attracted increased attention, as they are expected to realize ultra-low-power, higher bandwidth and shorter interconnection delays. Such an architecture opens the way for “normally-off / instant–on” computing with no “standby power” and wider memory bandwidth. This has led to the search for technologies that combine memory and computing capabilities in the same device.

Topological spin textures named magnetic skyrmions [3, 4] have emerged recently as a promising candidate to act as the building blocks of logic-in-memory technologies that intrinsically merge high density non-volatile storage memories and logic operations. Magnetic skyrmions are local whirling of the magnetization. Their nanometric scale, topological protection, mutual repulsion, fast and low power manipulation can be exploited to code data and perform computation at the nanoscale. Different types of logic devices based on skyrmions have been proposed in recent years. [5] [13]. The primary physical phenomenon driving these devices is the mutual repulsion of skyrmions resulting from the dipolar and exchange interactions. Skyrmions are also very sensitive to local variations of the magnetic properties, which can be exploited to design local potential wells that guide the skyrmion trajectory in logic circuits [14] [30].

As the anisotropy can be modulated using a gate electric field, programmable skyrmion switches and routers controlled by gate voltage have been proposed, which can be utilized to perform boolean logic as well as neuromorphic and stochastic computing [12, 31]. However, such an approach is plagued by the need for densely packed gates with bulky electrical circuitries and multiple voltage/skyrmion signal interconversion stages, resulting in a prohibitively large energy and footprint cost.

A more promising approach lies in a local modulation of the magnetic parameters through engineering of the material. In particular, light ion irradiation is a powerful tool to tailor the magnetic properties of ultrathin films, via a gentle intermixing of the interfaces [32]. In ultrathin Pt/Co/MgO films, we have shown that it leads to a decrease of the magnetic anisotropy and Dzyaloshinkii-Moriya interaction [14]. This can be exploited to create and guide skyrmions in racetracks defined by ion irradiation, which acts as local potential wells for the skyrmions [14].

In this work, we investigate the interactions of skyrmions with anisotropy energy barriers and show that a fine tuning of the barrier height and width allows the selective tunneling of skyrmions between parallel nanotracks triggered by skyrmion-skyrmion interaction. This can be leveraged to design a skyrmion De-multiplexer (DMux) logic gate which works solely using skyrmions as logic inputs. By cascading three demultiplexer logic gates, a fully programmable logic gate is proposed which allows the realization of any desired logic output from a set of given inputs. The developed logic design is fully conservative, i.e., no skyrmion is destroyed during the process and all skyrmions can be recovered at the end of the logic operation, which makes it suitable for conservative reversible logic. This also removes the need for continuous generation of skyrmions which is an energy expensive process. The developed logic design
can significantly reduce the number of elementary logic operations required to perform complex arithmetic computations. Moreover, the proposed implementation also provides a modular design template for creating large scale logic networks by re-purposing DMux gates.

II. SKYRMION DYNAMICS IN PRESENCE OF AN ENERGY BARRIER

In this section, we establish the basic understanding of the dynamics of a single skyrmion interacting with an energy barrier created by a sudden change in anisotropy and DMI induced by He-ion irradiation. We performed micromagnetic simulations with magnetic and transport parameters consistent with our prior experimental work (see Appendix A for details regarding the micromagnetic model and parameters) [14].

We considered an ultrathin film with a single skyrmion moving under the influence of spin orbit torque (SOT). An energy barrier of width \( W \) and height \( \Delta B_K \) is present in the system, located at \( y = 0 \). The barrier height \( \Delta B_K \) is defined as the difference between the values of the effective anisotropy field of the barrier (non-irradiated) and the outer (irradiated) region, \( \Delta B_K = B_{K, non-irr} - B_{K, irr} \). The skyrmion moves along an oblique direction at an angle of \( \sim 68^\circ \) (skyrmion Hall angle) with the x-axis due to the current flowing along +x-direction (current density, \( J = 5 \times 10^{10} \text{A/m}^2 \)). Figure 1 (a) shows the trajectories of the skyrmion for different values of the barrier height \( \Delta B_K \) and with a fixed barrier width of \( W = 12 \text{nm} \). The anisotropy of the outer region is fixed at \( B_{K, irr} = 7 \text{mT} \). We find that for low \( \Delta B_K \), the skyrmion can pass through the energy barrier while for large enough \( \Delta B_K \), the skyrmion does not pass and eventually moves along the barrier (see \( \Delta B_K = 65 \text{mT} \)). Interestingly, when the skyrmion passes through the barrier, we observe that the trajectories are shifted along the x-direction, the magnitude of this shift being dependent on the value of \( \Delta B_K \). Similar behavior was also observed for skyrmions crossing energy steps \([33, 34]\). The possibility of crossing the barrier also depends on the barrier width \( W \). We show in Fig. 1 (b), the trajectories of skyrmions for different \( W \) with a fixed barrier height of \( \Delta B_K = 65 \text{mT} \). For low width \( (W = 6 \text{nm}) \), the skyrmion easily crosses the barrier while for all other cases \((W = 12, 18 \text{ and } 24 \text{nm})\), the skyrmion is blocked and moves along the barrier (see supplementary video SV1). Physically, this can be understood by considering the fact that, in the case of a narrow barrier, only a small portion of the skyrmion falls inside the energetically unfavourable barrier region during the crossing from the lower to the upper region. Thus, the energy increase due to the skyrmion moving inside the non-irradiated region is not very high and can be overcome by the force due to the skyrmion Hall effect. We perform similar simulations for a range of \( \Delta B_K \) and \( W \) and present a corresponding map in Fig. 1 (c) depicting the set of \( \Delta B_K-W \) values for which the skyrmion can either cross the barrier (low \( \Delta B_K \) and \( W \)) or be blocked by it (high \( \Delta B_K \) and \( W \)). The boundary between both regimes depends on the injected current: for a higher value of the current density, we expect the boundary to shift toward higher \( \Delta B_K \) and \( W \), as the skyrmion has more energy to cross the energy barrier.

A. Skyrmion motion inside irradiated nanotrack

The possibility for a skyrmion to cross or not an energy barrier depending on the external parameters can be exploited to guide and control the skyrmion trajectory in tracks defined by ion irradiation. Figures 2 (a) and (b) show the trajectory of a skyrmion in a nan-
otrack with lower anisotropy driven by a current density of $J = 5 \times 10^{10} \text{A/m}^2$ and $J = 11 \times 10^{10} \text{A/m}^2$, respectively. For a fixed $\Delta B_K$, there exists a threshold current density beyond which the skyrmion cannot be confined inside the track. For our simulation parameters, a threshold $J_{\text{th}} = 10 \times 10^{10} \text{A/m}^2$ is found. In the following, we use a current density of $5 \times 10^{10} \text{A/m}^2$ which is half of this threshold, such that the skyrmion stays confined in the track.

Next, we consider the motion of skyrmions in parallel nanotacks. To minimize the area of the device which is critical for energy consumption, it is necessary to densely pack many tracks. In Fig. 2(c) and (d), we show the motion of a skyrmion in two parallel tracks separated by a barrier of width $W = 12\text{nm}$ and $W = 6\text{nm}$, respectively, for a fixed current density of $J = 5 \times 10^{10} \text{A/m}^2$. Skyrmion motion in two parallel nanotacks separated by a barrier region of width, $W = 12\text{nm}$ having an inter-connecting channel of width $6\text{nm}$ (e) and $12\text{nm}$ (f), respectively, at the center of the barrier. Movies corresponding to all cases (a)-(f) are shown in supplementary video SV2.

**FIG. 2.** Skyrmion motion in 80nm wide nanotack for current density (a) $J = 5 \times 10^{10} \text{A/m}^2$ and (b) $J = 11 \times 10^{10} \text{A/m}^2$, respectively. The dashed white lines on the track represent a discontinuity along the x-scale which we use to show the motion for a longer time-scale ($t = 0 - 100\text{ns}$). The skyrmion has a diameter $\sim 57\text{nm}$. Skyrmion motion in two parallel nanotacks separated by a non-irradiated barrier region of width $W = 12\text{nm}$ (c), and $W = 6\text{nm}$ (d), respectively, for a fixed current density of $J = 5 \times 10^{10} \text{A/m}^2$. Skyrmion motion in two parallel nanotacks separated by a barrier region of width, $W = 12\text{nm}$ having an inter-connecting channel of width $6\text{nm}$ (e) and $12\text{nm}$ (f), respectively, at the center of the barrier. Movies corresponding to all cases (a)-(f) are shown in supplementary video SV2.

The concepts of skyrmion movement within and passing between parallel nano-tracks can be exploited to design a skyrmion-based De-multiplexer (DMux) logic gate. A DMux gate is a logic gate which connects an incoming signal to one of the multiple output streams based on the value of selector input. We will here discuss a 1-to-2 DMux which takes a single selector ($X_1$) input (“0” or “1”) and connects the incoming signal ($G$) to one of the two outputs ($O_1$ or $O_2$) (see Fig. 3(a) and (b)). In our device, the input “1” is represented by a single skyrmion, while the absence of skyrmion will correspond to input “0”. Two different DMux gate designs are presented, both of which are based on skyrmions moving inside parallel nanotacks but differ in their working principle. These two different DMux gates can be connected to build programmable logic gates as will be shown later in Sec. II.C.

**B. Skyrmion based De-multiplexer**

The concepts of skyrmion movement within and passing between parallel nano-tracks can be exploited to design a skyrmion-based De-multiplexer (DMux) logic gate. A DMux gate is a logic gate which connects an incoming signal to one of the multiple output streams based on the value of selector input. We will here discuss a 1-to-2 DMux which takes a single selector ($X_1$) input (“0” or “1”) and connects the incoming signal ($G$) to one of the two outputs ($O_1$ or $O_2$) (see Fig. 3(a) and (b)). In our device, the input “1” is represented by a single skyrmion, while the absence of skyrmion will correspond to input “0”. Two different DMux gate designs are presented, both of which are based on skyrmions moving inside parallel nanotacks but differ in their working principle. These two different DMux gates can be connected to build programmable logic gates as will be shown later in Sec. II.C.

**De-multiplexer : Type A**

Figures 3(c) and (d) show the working principle of our first DMux gate design, named “DMux Type A”. The width of each track is 80nm with a barrier width $W = 12\text{nm}$ separating each track. The incoming skyrmion en-
FIG. 3. (a) and (b) show the schematic and operation of a 1-to-2 DMux gate which produces a 0(1) output at $O_1$ and 1(0) at $O_2$ if the selector input is $X_1 = 1(0)$. The input “G” is assumed to be fixed at “1”. (c) and (d) show the micromagnetic simulation of a skyrmion based DMux gate where the incoming signal “G” is a skyrmion in track $T_1$. The selector input is a skyrmion (or no-skyrmion) in track $T_0$. The current density is $J = 5 \times 10^{10} \text{A/m}^2$. (e) and (f) shows the micromagnetic simulations of a different design implementation of skyrmion based DMux with an additional channel in the barrier. For this case, the track for selector input is above the “G” input. Movies corresponding to (c)-(f) are shown in supplementary video SV3.

ters the system from the left-hand side of the $T_1$ track (“G” input) while the selector input ($X_1$) is in the $T_0$ track. A uniform DC current along the $\hat{x}$-direction ($J = 5 \times 10^{10} \text{A/m}^2$) moves the skyrmion with a positive velocity $v_x$ in the $\hat{x}$-direction as discussed previously. For the case where the selector input “$X_1$” is “0” [Fig. 3(c)], i.e., there is no skyrmion in the $T_0$ track, the skyrmion input “G” moves along the $T_1$ track leading to the output $O_1 = 1$. The output $O_2$ remains “0” as no skyrmion is present in the corresponding track. The Fig. 3(d) shows the operation of DMux if the selector input is “1”, i.e., a skyrmion is present in the $T_0$ track. This skyrmion in the track $T_0$ cannot move along the +x-direction during the current injection as it is blocked by the energy barrier. When the skyrmion in the track $T_1$ gets closer to the skyrmion in the track $T_0$, which remains almost fixed due to the barrier, it experiences a repulsive force due to the skyrmion-skyrmion interaction. This repulsive force enhances the transverse force already acting on the skyrmion in track $T_1$ due to the skyrmion Hall effect. The resulting force is enough to push the moving skyrmion through the barrier between track $T_1$ and $T_2$, and this skyrmion ends its trajectory at output $O_2$. From the results in Fig. 3(c) and (d), we conclude that the overall functionality of DMux is achieved: the incoming skyrmion from the left of the $T_1$ track (“G”) is guided to either the output $O_1$ or the output $O_2$ depending upon the presence of skyrmion in the $T_0$ track (selector input). The outputs can be expressed as: $O_1 = X_1$ and $O_2 = X_1$ (for $G = 1$).

De-multiplexer : Type B

In the design of DMux Type A, the track for the selector input $X_1$ is below the track for the “G” input. In our programmable logic gate design, we will also require a DMux gate in which the moving skyrmion (“G” input) is below the selector input ($X_1$). The principle of this DMux Type B design functionality is shown in Fig. 3(e) and (f). Similar to our previous design, we use irradiated tracks to confine the skyrmion, however, we remove the track $T_0$ where the input $X_1$ was kept in DMux Type A. Instead, we divide the track $T_2$ in two parts by adding a vertical barrier of width $W = 12 \text{nm}$ in the middle of the $T_2$ track. The input $X_1$ is now sent from the left of the track $T_2$. Additionally, we connect the track $T_1$ with the right part of $T_2$ by introducing a small channel in the barrier, which allows a skyrmion moving in track $T_1$ to pass to the track $T_2$. In Fig. 3(e), the incoming skyrmion enters from the left of the $T_1$ track and moves along +x-direction. If there is no skyrmion in the upper track ($X_1 = 0$), the skyrmion will move towards the upper track $T_2$ tunneling through the interconnecting channel and will arrive at the output $O_2$. However, if the track $T_2$ has a skyrmion ($X_1 = 1$) [Fig. 3(f)], the skyrmion in the track $T_1$ moves straight to the right end towards the output $O_1$ due to the mutual repulsive force. Overall, as in the previous case, the DMux logic here is achieved as the skyrmion is guided to the right side at either output $O_1$ or output $O_2$ depending on the selector input ($X_1$). The output of DMux Type B can be expressed as: $O_1 = X_1$ and $O_2 = X_1$ (for $G = 1$).
Designing this programmable gate with skyrmion based DMux gates involves that (i) the input $X_2$ (a skyrmion) must be conserved (stored) or duplicated and pass through both DMux2 and DMux3 gates and (ii) the output of the first DMux gate has to reach the input of the next DMux gate (cascading) without altering its value. We first focus on Stage 1 of this logic circuit and propose a design in Fig. 4(b), which is based on the previously described DMux gates Type A and Type B. The tracks in DMux2 and DMux3 which carry the selection input (track $T_2$) are merged to avoid the need for duplication of input $X_2$. This is possible only if we use the Type A design for the DMux2 and Type B design for the DMux3 as shown in Fig. 4(b). This merging also reduces the total number of required tracks, reducing the total area of the device, which further minimizes the energy consumption for the operation.

**Performing Logic operations (Stage 1)**

Figure 5 shows the operation of our programmable logic gate design proposed in Fig. 4(b) using micromagnetic simulations. Here, we assume that the inputs $X_1$ and $X_2$ are already correctly placed in the tracks $T_0$ and $T_2$ at their respective positions. The exact protocol to place these inputs is discussed in Appendix B. For the case of $X_1 = 1$ and $X_2 = 0$ [Fig. 5(a)], the skyrmion input “G” enters through track $T_1$ and is pushed to track $T_2$ due to the repulsion from the skyrmion in track $T_0$ (input $X_1$). The skyrmion then passes through the large opening in the barrier into track $T_3$. In track $T_3$, the skyrmion keeps moving straight (along $+x$-direction) and is obtained at the output end $O_3$. For the case of $X_1 = 0$ and $X_2 = 1$ [Fig. 5(b)], the skyrmion enters through track $T_1$ and initially moves straight without facing any repulsion (as input $X_1$ is “0”). The skyrmion then experiences repulsion from the skyrmion in track $T_2$ (input $X_2$). Due to this repulsion, the moving skyrmion cannot tunnel through the channel between tracks $T_1$ and $T_2$ and is forced to move in the same track $T_1$, to finally exit through the output end $O_1$. For inputs $X_1 = 1$ and $X_2 = 1$ [Fig. 5(c)], the input skyrmion “G” follows the same pattern as in Fig. 5(a) till it reaches the track $T_3$. While moving in the track $T_3$, it is repelled from the skyrmion input $X_2$ lying in the track $T_2$ which pushes it to the uppermost track $T_4$, i.e. output $O_4$ (see also supplementary video SV4). Lastly, for the case of $X_1 = 0$ and $X_2 = 0$, the input skyrmion “G” in the track $T_1$ moves straight along the track till it reaches the interconnecting channel between tracks $T_1$ and $T_2$. After tunneling through the channel to the $T_2$ track, the skyrmion then reaches the $O_2$ output. Using the previous expressions for Type A and Type B DMux gates, we can write the mathematical notation for each of the output gates $O_1 - O_4$ as follows: $O_1 = (X_2 \cdot X_1)$, $O_2 = (\overline{X_1} \cdot X_2)$, $O_3 = (X_1 \cdot X_2)$, and $O_4 = (X_1 \cdot X_2)$. These outputs can now be combined in the Stage 2 operation of the logic circuit for obtaining the desired operation as discussed in the next section.
interacting with each other during the merging operation.

The full design is shown in Fig. 6(a) where the regions between the new track and the four parallel tracks is kept to the parallel tracks combining all four output tracks in our design by simply adding another track at an angle to the parallel tracks. Depending on the inputs \( X_1 \) and \( X_2 \), the skyrmion “G” entering through track \( T_1 \) reaches one of the outputs \( O_1 \) – \( O_4 \). Note that for each set of inputs \( X_1 \) and \( X_2 \), only one of the output tracks \( (O_1 – O_4) \) has a skyrmion (“1”) and the rest are “0”.

Combining Outputs (Stage 2)

The Stage 2 of Fig. 4(a) involves passing the four outputs from Stage 1 through an ON/OFF gate and combining them afterward. These ON/OFF gates can simply be constructed as tracks with/without an energy barrier in the track which prevents/allows the skyrmion to pass. Note that the programmability in this design is limited to modifying the tracks to obtain any desired logic functionality which is known at the time of device fabrication. However, a dynamically reconfigurable design can also be achieved by replacing these barriers with voltage-controlled gates which can modify the magnetic anisotropy locally and can thus reconfigure the logic functionality even after fabrication. The output obtained after each of these gates is finally merged to obtain the final output \( Y \). This merging is relatively easy to implement in our design by simply adding another track at an angle to the parallel tracks combining all four output tracks \( (O_1 – O_4) \). For faster skyrmion motion, the angle between the new track and the four parallel tracks is kept at 68° which is the same as the Skyrmion Hall Angle. The full design is shown in Fig. 6(a) where the regions \( G_a – G_d \) represent the gates and the final output \( Y \) is obtained from the uppermost track. It may be noted here that for any combination of inputs \( X_1 \) and \( X_2 \) only one of the outputs \( O_1 – O_4 \) contains a skyrmion (“1”) and the rest are empty (“0”). Therefore, there is no possibility of multiple skyrmions arriving from two different tracks and interacting with each other during the merging operation through the non-parallel track.

To demonstrate the working principle of this design using micromagnetic simulations, we use the expression for XOR gate as an example of our desired output. Other logic functionalities can also be obtained by changing the values of parameters \([a,b,c,d]\) as given in Table I. The XOR gate is mathematically represented as:

\[
Y = X_1 \cdot \overline{X}_2 + \overline{X}_1 \cdot X_2
\]

For the case \( (X_1 = 1, X_2 = 0) \) [Fig. 6(b)] and \( (X_1 = 0, X_2 = 1) \) [Fig. 6(c) and supplementary video SV5] the output skyrmion of Stage 1 proceeds to the uppermost output track giving the final output \( Y = 1 \). For the case of \( (X_1 = 1, X_2 = 1) \) [Fig. 6(d)] and \( (X_1 = 0, X_2 = 0) \) [Fig. 6(e)], the output from Stage 1 is received in \( O_1 \) and \( O_2 \), respectively, both of which are blocked by the energy barriers. Thus, the final output for both these cases is \( Y = 0 \).

Operational Characteristics

For the material parameters and dimensions used in the micromagnetic simulations, the operation time for the designed gate varies from 76 – 120 ns for Stage 1 and 45 – 70 ns for Stage 2 with a current of 0.1 mA which corresponds to a maximum energy dissipation of...
238 fJ (Stage 1 + Stage 2) by Joule heating. Note that the magnetic and transport parameters of the material stacks were extracted from proof of concept experiments, which were not designed for logic gates implementations. Faster operations with lower energy can be easily achieved by designing the gate with magnetic materials with lower damping, larger spin orbit torques, higher anisotropy in the non-irradiated track and lower device dimensions. For instance, by considering materials with 10 nm skyrmions, a magnetic damping of 0.05 and assuming the lateral dimensions decreased by a factor 5 due to smaller skyrmion size, a total operation time of 6.3 ns with a current of 20 µA and an energy dissipation of 0.32 fJ is anticipated for $J = 5 \times 10^{10}$ A/m². Note that these values do not include the delay and energy dissipated in the addressing transistors and contact lines. These figures should be compared with the energy dissipation and delay in interconnects for the data to reach the CMOS logic in a conventional Von Neumann architecture, which is typically of the order of the pJ for 1mm interconnect, combined with the write time in SRAM cache memory, around the ns. Thus, we expect a drastic decrease in the energy consumption as compared to a standard Von Neumann architecture.

III. CONCLUSIONS

To conclude, we have proposed a programmable logic gate design based on skyrmion-skyrmion interactions. The gate exploits the skyrmion guiding and selective crossing of energy barrier designed by local patterning of the magnetic parameters, which can be realized using light ion-irradiation. The gate is conservative and cascadable and since it relies purely on skyrmion interactions, does not require complex electric/magnetic interconversion gates. Since skyrmions can be used at nanoscale to represent elementary bits, the proposed gate could form the basis of logic-in-memory devices that intrinsically merge high density memory and computing capabilities.

ACKNOWLEDGMENTS

The authors acknowledge financial support from the French national research agency (ANR) (Grant Nos. ANR-15-CE24-0015-01 and ANR-17-CE24-0045) and the American defense advanced research project agency (DARPA) TEE program (Grant No. MIPR HR0011831554). This work has been partially supported by MIAI@Grenoble Alpes, (ANR-19-P3IA-0003).

Appendix A: Micromagnetic simulations

The simulations are performed in a micromagnetic framework by numerically solving the Landau-Lifshitz-Gilbert (LLG) equation using the open-source Mmumax3 package [37]. We consider a stack composed of ferromagnetic/heavy metal (FM/HM) ultrathin films. Due to the spin-orbit interaction at the ferromagnetic/heavy metal (FM/HM) interface, a spin current flows in the perpendicular (+`z`) direction through the FM if a charge current is injected in the in-plane +`x`-direction in the HM. The direction of polarization of the electrons $e_p$ is along the $−`y$-direction, i.e orthogonal to the direction of flow of

---

**TABLE I.** Values of parameters (a,b,c,d) for obtaining different logic operations. The output is represented by $Y =aX_1X_2 + bX_1\overline{X_2} + c\overline{X_1}X_2 + d\overline{X_1}\overline{X_2}$

| Logic Gate | a | b | c | d |
|-----------|---|---|---|---|
| AND       | 1 | 0 | 0 | 0 |
| OR        | 1 | 1 | 0 | 1 |
| XOR       | 0 | 1 | 0 | 1 |
| NAND      | 0 | 1 | 1 | 1 |
| NOR       | 0 | 0 | 1 | 0 |
| XNOR      | 1 | 0 | 1 | 0 |
charge current as well as the flow of spin current. We include the additional torque on the FM due to this spin current using the Slonczewski model.

\[
\frac{d\mathbf{m}}{dt} = -\gamma (\mathbf{m} \times \mathbf{B}_{\text{eff}}) + \alpha (\mathbf{m} \times \frac{d\mathbf{m}}{dt}) - \mathcal{T} (\mathbf{m} \times (\mathbf{m} \times \mathbf{e}_p) + \mathbf{e}_p) \\
\mathcal{T} = \frac{\hbar q m J_c}{2 |e| M_S d}
\]

where, \( \mathbf{m} \) is the normalized local magnetic moment, \( \gamma \) is the gyromagnetic ratio of the electron, \( \alpha \) is the Gilbert damping constant and \( \mathcal{T} \) represents the strength of spin orbit torque. \( J \) is the charge current through the HM flowing in \( +\hat{x} \)-direction, \( |e| \) is the electronic charge, \( M_S \) is the saturation magnetization and \( d \) is the thickness of the ferromagnetic film. We use \( \theta_H = 0.1 \) as the spin Hall angle and \( \epsilon = 0.015 \) as the ratio of field-like to damping-like SOT torque. \( \mathbf{B}_{\text{eff}} \) is the effective field which includes contributions from the external field (\( \mathbf{B}_{\text{ext}} \)), the magnetostatic interactions (\( \mathbf{B}_m \)), the exchange interactions (\( \mathbf{B}_\text{exch} \)), the perpendicular magnetic anisotropy (\( \mathbf{B}_\text{an} \)) and Dzyaloshinskii Moriya interaction (\( \mathbf{B}_\text{DMI} \)).

To achieve realistic predictions, we use the material parameters corresponding to our previous experimental work on skyrmion confinement in He irradiated nanotrails [14] given in Table II with an external field of \( \mathbf{B}_{\text{ext}} = 33 \text{mT} \hat{z} \). Note that we obtain the value of effective anisotropy field (\( B_K \)) from experiments which can be translated to the uniaxial anisotropy constant using the expression: \( K = (B_K M_S^2)/2 \) + \( \mu_0 M_S^2/2 \). The total area of the simulated system in Stage 1 is 1024nm \( \times \) 512nm with 0.9nm FM thickness. The area of Stage 2 design is 512nm \( \times \) 512nm. The resistivity of the HM (Pt in our case) is 30\( \Omega \mu \text{m} \) from experimental measurements. For solving the LLG equation, we discretize the entire FM into cuboidal cells of 2nm \( \times \) 2nm \( \times \) 0.9nm and use the 4\( ^{th} \) order Runge-Kutta method with an adaptive time-step.

**Appendix B: Setting and recovering inputs**

In order to perform the operations shown in Fig. 5, the inputs \( X_1 \) and \( X_2 \) have to be set at proper positions. We mention below the protocol followed to achieve this. The input skyrmion \( X_2 \) is sent through the track \( T_1 \) at time \( t = 0 \). The injected current is \( J = 5 \times 10^{10} \text{A/m}^2 \). The skyrmion then moves along the track \( T_1 \) to the right. At \( t = 40 \text{ns} \), we increase the current to \( J = 10 \times 10^{10} \text{A/m}^2 \) [see Fig. 7 (a)]. For this value of current, the skyrmion can pass through the energy barrier. Hence the skyrmion moves from track \( T_1 \) to the track \( T_2 \). The current is again reduced back to \( J = 5 \times 10^{10} \text{A/m}^2 \) at \( t = 50 \text{ns} \) once the skyrmion has already entered track \( T_2 \). At this point, the skyrmion corresponding to input \( X_1 \) is also injected from the track \( T_0 \). After another \( t = 30 \text{ns} \) with \( J = 5 \times 10^{10} \text{A/m}^2 \), both the inputs are placed at their respective positions. We then proceed to perform the logic operations shown in Fig. 5. Once the operation is finished, to recover the skyrmion, we simply use a current density with negative polarity \( J = -5 \times 10^{10} \text{A/m}^2 \) for 50ns. The skyrmion input \( X_1 \) is collected back from the track \( T_0 \) and the skyrmion input \( X_2 \) can be collected from the track \( T_2 \). The motion of the skyrmion input \( X_2 \) during the entire SET and RECOVER cycle is shown in Fig. 7 (b).

**Appendix C: Scalability via Cascading**

The designed logic gates can be combined to make large-scale networks via cascading. In Fig. 8, we show a schematic of two cascaded logic gates each having their own Stage 1 and Stage 2 components. The inputs \( X_1 \), \( X_2 \) and \( X_3 \) will be set by sending them through the tracks \( T_0 \), \( T_1 \) and \( T_5 \), respectively. The fixed input \( G_1 \) is then sent.

---

**TABLE II. Simulation Parameters**

| Parameter | Irradiated | Non-irradiated |
|-----------|------------|----------------|
| \( M_s \) (MA/m) | 1.32 | 1.32 |
| \( \mu_0 B_K \) (mT) | 7 | 72 |
| \( |D| \) (mJ/m²) | 1.082 | 1.122 |
| \( A \) (pJ/m) | 16 | 16 |
| \( \alpha \) | 0.3 | 0.3 |

FIG. 7. (a) Set of current pulses used to set the inputs \( X_1 \) and \( X_2 \) at their corresponding positions (b) motion of the skyrmion input \( X_2 \) during a full SET and RECOVER cycle.
FIG. 8. Schematic of two cascaded logic gates (each with a Stage 1 and Stage 2 operation) for performing \((X_1 \oplus X_2) \oplus X_3\).

through the track \(T_1\) to perform the first logic operation \((O_1 = X_1 \oplus X_2)\) followed by sending \(G_2\) through the track \(T_5\) to perform the second logic operation \((O_2 = O_1 \oplus X_3)\). At the end of the operation, the inputs \(X_1, X_2, X_3\) and outputs \(O_1\) (also an input for the second operation), \(O_2\) can be retrieved through the tracks \(T_0, T_2, T_6\) and \(T_1, T_5\), respectively, by sending a negative polarity current.

Appendix D: Effect of thermal noise

In our simulations, we have used the material parameters which were experimentally measured at room temperature. Therefore, we automatically account for the effect of finite temperature on material parameters (reduced \(A, B_k, D\) and \(M_S\)). Nevertheless, in Fig. 9(a), we show the simulation of Stage 1 for inputs \(X_1 = 1\) and \(X_2 = 1\) with stochastic noise corresponding to \(T=30\text{K}\) obtaining a correct logic operation. Note that the quantitative value of temperature used in these simulations may not correspond to real temperatures due to (i) double calculation of thermal effect due to the use of stochastic noise as well as room temperature parameters, (ii) limitations of micromagnetic approach (dependence of thermal field on simulation cell size) and (iii) absence of statistical data (ideally several simulation runs with same parameters but different initial seeds should be performed but this is computationally prohibitive due to long simulation times).

We also calculate the energy of the skyrmion as a function of position from our micromagnetic model. For the parameters used in the main text \((W = 12\text{nm} \text{ and } \Delta B_K = 65\text{mT})\), we obtain a barrier energy of \(\sim 7k_B T\). Assuming an attempt frequency of 1GHz, the retention time of the skyrmion is \(\sim 1\mu s\) which is about 5 times the operation time for the designed logic gate. Moreover, the energy barrier and the retention time can be easily enhanced by increasing \(\Delta B_K\) as shown in Fig. 9(b).

Appendix E: Tolerance w.r.t the variation of \(W\) and \(\Delta B_K\)

We carried out simulations for DMux Type A logic gate for varying barrier widths \(W\) and height \(\Delta B_K\). The obtained results are shown in Fig. 10. The green squares and red circles represent a correct and incorrect logic operation, respectively. In general, the DMux Type A logic gate works for a range of \(W\) and \(\Delta B_K\) values. For fixed \(W = 12\text{nm}\), the logic operation is correctly performed in the range of \(\Delta B_K = 61 - 71\text{mT}\) allowing \(\sim 15\%\) of variation \(\Delta B_K\). Higher (lower) barrier width can also be used to design the logic gate, provided that the barrier height is decreased (increased) accordingly.

[1] T. N. Theis and H.-S. P. Wong, The End of Moore’s Law: A New Beginning for Information Technology, Computing in Science Engineering 19, 41 (2017).
FIG. 10. Map showing the values of barrier widths $W$ and height $\Delta B_K$ for which a correct (green squares) or incorrect (red circles) logic outputs is obtained for DMux Type A.

---

[2] V. Zhirnov, R. Cavin, J. Hutchby, and G. Bourianoff, Limits to binary logic switch scaling - a gedanken model, Proc. IEEE 91, 1934 (2003)

[3] N. Nagaosa and Y. Tokura, Topological properties and dynamics of magnetic skyrmions, Nat. Nanotech. 8, 899 (2013)

[4] A. Fert, N. Reyren, and V. Cros, Magnetic skyrmions: advances in physics and potential applications, Nat. Rev. Mater. 2, 17031 (2017)

[5] X. Zhang, M. Ezawa, and Y. Zhou, Magnetic skyrmion logic gates: conversion, duplication and merging of skyrmions, Sci. Rep. 5, 1 (2015).

[6] X. Xing, P. W. Pong, and Y. Zhou, Skyrmion domain wall collision and domain wall-gated skyrmion logic, Phys. Rev. B 94, 054408 (2016).

[7] Z. He, S. Angizi, and D. Fan, Current-induced dynamics of multiple skyrmions with domain-wall pair and skyrmion-based majority gate design, IEEE Magn. Lett. 8, 1 (2017).

[8] S. Luo, M. Song, X. Li, Y. Zhang, J. Hong, X. Yang, X. Zou, N. Xu, and L. You, Reconfigurable skyrmion logic gates, Nano Lett. 18, 1180 (2018).

[9] Z. Zhang, Y. Zhu, Y. Zhang, K. Zhang, J. Nan, Z. Zheng, Y. Zhang, and W. Zhao, Skyrmion-based ultra-low power electric-field-controlled reconfigurable (super) logic gate, IEEE Electron Device Lett. 40, 1984 (2019).

[10] M. Chauwin, X. Hu, F. Garcia-Sanchez, N. Betrabet, A. Paler, C. Moutafis, and J. S. Friedman, Skyrmion logic system for large-scale reversible computation, Phys. Rev. Appl. 12, 064053 (2019).

[11] M. Song, M. G. Park, S. Ko, S. K. Jang, M. Je, and K.-J. Kim, Logic device based on skyrmion annihilation, IEEE Trans. Electron Devices (2021).

[12] H. Zhang, D. Zhu, W. Kang, Y. Zhang, and W. Zhao, Stochastic computing implemented by skyrmionic logic devices, Phys. Rev. Appl. 13, 054049 (2020).

[13] L. Gnoli, F. Riente, M. Vacca, M. Ruoo Roch, and M. Graziano, Skyrmion logic-in-memory architecture for maximum/minimum search, Electronics 10, 155 (2021).

[14] R. Juge, K. Bairagi, K. G. Rana, J. Vogel, M. Sall, D. Mailly, V. T. Pham, Q. Zhang, N. Sisodia, M. Forster, L. Aballe, M. Belmeguenai, Y. Roussigné, S. Aufret, L. D. Buda-Prebeannu, G. Gaudin, D. Ravelosona, and O. Boule, Helium ions put magnetic skyrmions on the track, Nano Lett. 21, 2989 (2021).

[15] M. Song, K.-W. Moon, S. Yang, C. Hwang, and K.-J. Kim, Guiding of dynamic skyrmions using chiral magnetic domain wall, Appl. Phys. Express 13, 063002 (2020).

[16] I. Purnama, W. L. Gan, D. W. Wong, and W. S. Lew, Guided current-induced skyrmion motion in 1D potential well, Sci. Rep. 5, 10620 (2015).

[17] P. Lai, G. P. Zhao, H. Tang, N. Ran, S. Q. Wu, J. Xia, X. Zhang, and Y. Zhou, An Improved Racetrack Structure for Transporting a Skyrmion, Sci. Rep. 7, 45530 (2017).

[18] H. T. Fook, W. L. Gan, I. Purnama, and W. S. Lew, Mitigation of Magnus Force in Current-Induced Skyrmion Dynamics, IEEE Trans. Magn. 51, 1 (2015).

[19] D. Toscano, J. P. A. Mendonça, A. L. S. Miranda, C. I. L. de Araujo, F. Sato, P. Z. Coura, and S. A. Leonel, Suppression of the skyrmion Hall effect in planar nanomagnets by the magnetic properties engineering: Skyrmion transport on nanotrails with magnetic strips, J. Magn. Magn. Mater. 504, 166555 (2020).

[20] S. Bhatti and S. N. Piramanayagam, Effect of Dzyaloshinskii–Moriya Interaction Energy Confinement on Current-Driven Dynamics of Skyrmions, Phys. Status Solidi RRL 13, 1000990 (2019).

[21] R. P. Loreto, X. Zhang, Y. Zhou, M. Ezawa, X. Liu, and C. I. L. de Araujo, Manipulation of magnetic skyrmions in a locally modified synthetic antiferromagnetic racetrack, J. Magn. Magn. Mater. 482, 155 (2019).

[22] C. C. I. Ang, W. Gan, and W. S. Lew, Bilayer skyrmion dynamics on a magnetic anisotropy gradient, New J. Phys. 21, 043006 (2019).

[23] J. Iwasaki, W. Koshibae, and N. Nagaosa, Colossal Spin Transfer Torque Effect on Skyrmion along the Edge, Nano Lett. 14, 4432 (2014).

[24] P. Lai, G. P. Zhao, F. J. Morvan, S. Q. Wu, and N. Ran, Motion of Skyrmions in Well-Separated Two-Lane Racetracks, SPIN 07, 1740006 (2017).

[25] X. Zhang, G. P. Zhao, H. Fangohr, J. P. Liu, W. X. Xia, J. Xia, and F. J. Morvan, Skyrmion-skyrmion and skyrmion-edge repulsions in skyrmion-based racetrack memory, Sci. Rep. 5, 7643 (2015).

[26] Z. Yan, Y. Liu, Y. Guang, J. Feng, R. Lake, G. Yu, and X. Han, Robust Skyrmion Shift Device Through Engineering the Local Exchange-Bias Field, Phys. Rev. Appl. 14, 044008 (2020).

[27] C. C. I. Ang, W. Gan, G. D. H. Wong, and W. S. Lew, Electrical Control of Skyrmion Density via Skyrmion-Stripe Transformation, Phys. Rev. Applied 14, 054048 (2020).

[28] M. V. Sapozhnikov, S. N. Vдовичев, O. L. Ermolaeva, N. S. Гусев, A. A. Фраерман, S. A. Гусев, and Y. V. Петров, Artificial dense lattice of magnetic bubbles, Appl. Phys. Lett. 109, 042406 (2016).

[29] D. Toscano, S. A. Leonel, P. Z. Coura, and F. Sato, Building traps for skyrmions by the incorporation of magnetic defects in nanomagnets: Pinning and scattering traps by magnetic properties engineering, J. Magn. Magn. Mater. 480, 171 (2019).
[30] M. V. Sapozhnikov, O. V. Ermolaeva, E. V. Skorokhodov, N. S. Gusev, and M. N. Drozdov, Magnetic Skyrmions in Thickness-Modulated Films, Jetp. Lett. 107, 364 (2018).

[31] D. Pinna, F. Abreu Araujo, J.-V. Kim, V. Cros, D. Querlioz, P. Bessiere, J. Droulez, and J. Grollier, Skyrmion gas manipulation for probabilistic computing, Phys. Rev. Applied 9, 064018 (2018).

[32] C. Chappert, H. Bernas, J. Ferré, V. Kottler, J.-P. Janet, Y. Chen, E. Cambril, T. Devolder, F. Rousseaux, V. Mathet, and H. Launois, Planar Patterned Magnetic Media Obtained by Ion Irradiation, Science 280, 1919 (1998).

[33] R. M. Menezes, J. Mulkers, C. C. d. S. Silva, and M. V. Milošević, Deflection of ferromagnetic and antiferromagnetic skyrmions at heterochiral interfaces, Phys. Rev. B 99, 104409 (2019).

[34] J. Castell-Queralt, L. González-Gómez, N. Del-Valle, A. Sanchez, and C. Navau, Accelerating, guiding, and compressing skyrmions by defect rails, Nanoscale 11, 12589 (2019).

[35] S. M. Lewis, M. S. Hunt, G. A. DeRose, H. R. Alty, J. Li, A. Wertheim, L. De Rose, G. A. Timco, A. Scherer, S. G. Yeates, et al., Plasma-etched pattern transfer of sub-10 nm structures using a metal–organic resist and helium ion beam lithography, Nano Lett. 19, 6043 (2019).

[36] W. Kluge, Computation of switching functions using input-pattern-conserving magnetic-bubble manipulations, Electronics Letters 8, 313 (1972).

[37] A. Vansteenkiste, J. Leliaert, M. Dvornik, M. Helsen, F. Garcia-Sanchez, and B. Van Waeyenberge, The design and verification of MuMax3, AIP Adv. 4, 107133 (2014).