Page Table Management for Heterogeneous Memory Systems

Sandeep Kumar∗
Intel Labs
Bengaluru, India

Aravinda Prasad
Intel Labs
Bengaluru, India

Smruti R. Sarangi
IIT Delhi
New Delhi, India

Sreenivas Subramoney
Intel Labs
Bengaluru, India

Abstract
Modern enterprise servers are increasingly embracing tiered memory systems with a combination of low latency DRAMs and large capacity but high latency non-volatile main memories (NVMMs) such as Intel’s Optane DC PMM. Prior works have focused on efficient placement and migration of data on a tiered memory system, but have not studied the optimal placement of page tables.

Explicit and efficient placement of page tables is crucial for large memory footprint applications with high TLB miss rates because they incur dramatically higher page walk latency when page table pages are placed in NVMM. We show that (i) page table pages can end up on NVMM even when enough DRAM memory is available and (ii) page table pages that spill over to NVMM due to DRAM memory pressure are not migrated back later when memory is available in DRAM.

We study the performance impact of page table placement in a tiered memory system and propose an efficient and transparent page table management technique that (i) applies different placement policies for data and page table pages, (ii) introduces a differentiating policy for page table pages by placing a small but critical part of the page table in DRAM, and (iii) dynamically and judiciously manages the rest of the page table by transparently migrating the page table pages between DRAM and NVMM. Our implementation on a real system equipped with Intel’s Optane NVMM running Linux reduces the page table walk cycles by 12% and total cycles by 20% on an average. This improves the runtime by 20% on an average for a set of synthetic and real-world large memory footprint applications when compared with various default Linux kernel techniques.

1 Introduction
The performance of the memory subsystem, both at the software and the hardware layer, is getting increasingly important in the digital era due to the explosive growth in the amount of data generated, processed and stored. This along with DRAM scaling challenges [16, 20, 22] has led to the exploration of several new hardware memory technologies with diverse capabilities and capacities such as Intel’s Optane PMM non-volatile main memory (NVMM) [17].

Modern servers typically use both DRAM and NVMMs to exploit the low latency capabilities of DRAM and high capacities of NVMMs [13, 15, 35]. Such tiered memory systems bring in additional challenges in terms of managing or tiering the placement and the migration of data between DRAM and NVMM. Several prior works [9, 19, 24, 31, 37] have studied these challenges for data pages and proposed solutions to identify and migrate hot data pages from NVMM to DRAM. However, they have not studied this in the context of page table pages. We argue that explicit and efficient management of page table pages is crucial for system performance for the following reasons.

First, large memory footprint applications, with terabytes of memory, incur frequent TLB misses [5, 28, 32] as TLBs cover only a small portion of the total physical memory (covering few MBs of physical memory with 4K page size and covering up to 3 GB with 2 M pages). As a consequence, a significant fraction of the memory accesses require a page table walk.

Second, the access latency of NVMMs is significantly higher than DRAM. For example, on Intel’s Optane DC PMM, the read latency is 3x higher than DRAM, mainly due to the Optane’s longer media latency [38]. Consequently, a

Figure 1. Redis populating 1 TB of key-value pairs. The inflection at around 500 seconds is when Linux starts allocating both data and page table pages on NVMM. In contrast, Radiant efficiently manages the placement of page table pages between DRAM and NVMM while the data pages follow the Linux kernel’s placement policy.

∗Work done during an internship at Intel Labs, Bengaluru, India.
hardware page table walk incurs higher walk latency when a page table page is placed in NVMM. As a page table walk requires up to 4 memory accesses upon a TLB miss (for a 4-level page table), the page table walk latency can be significantly higher in such cases which negatively impacts the application’s performance (as shown in Figure 1). Radiant efficiently places the page table pages between DRAM and NVMM to reduce cycles spent in page table walks which in turn improves the start-up time of Redis by 22% (Figure 1).

Third, a typical page table occupies a small fraction of DRAM. For example, the page table size of an application with 2 TB memory footprint is around 4 GB which is around 1% of DRAM on our evaluation system. Despite its relatively small size, page table pages can end up on NVMM even when there is enough free memory in DRAM. For instance, existing operating systems do not differentiate between page table and data page allocations; they apply the same allocation policy for both of them [4, 9, 12]. Hence, when memory interleave policy is selected for data pages, page table pages are also allocated in a round robin order on all nodes, including NVMM nodes, even when DRAM has free memory.

Lastly, operating systems do not support migration of page table pages [4]. Once the page table pages are allocated, they remain fixed for their lifetime; they are reclaimed only when either the corresponding data pages are freed or the process is terminated. In contrast, data pages enjoy the flexibility of migration between DRAM and NVMM based on the application’s memory access pattern.

A simple and straight forward approach to avoid page table pages spilling to NVMM is to bind the page table to DRAM. However, this approach results in pathological behavior where applications are killed by the out-of-memory (OOM) handler even when significant amount of free memory is available in the system (details in §3.5). In addition, as all the page table pages are not frequently accessed, placing the complete page table on high-performance DRAM memory is not merited. Hence, we argue for judiciously managing the placement of page table pages across DRAM and NVMM.

In this paper, we propose Radiant, an efficient and transparent page table management technique for tiered memory systems. Radiant differentiates between a data and a page table page allocation by applying different placement policies to them. It also considers the underlying memory heterogeneity while deciding on the placement of the page table pages.

Additionally, Radiant employs the following techniques for efficient page table management:

- **Placement**: introduces a differentiating placement policy within the page table by placing a small but critical part of the page table in DRAM. This differentiating placement strategy is based on the observation that the top three levels of a page table tree forms a small portion of the page table but are frequently accessed during a page table walk (3 out of 4 accesses during a page walk are from the higher levels of a page table).

- **Migration**: efficiently identifies and transparently migrates the last level page table pages between memory tiers by employing a novel data-page-migration triggered page table migration technique.

We implement Radiant in the Linux kernel and evaluate the performance benefits on a real system equipped with Intel’s Optane PMM persistent memory. Radiant reduces the page table walk cycles by 12% and total cycles by 20% on an average. This improves the runtime by 20% on an average for a set of synthetic and real-world large memory footprint applications when compared with the various default Linux kernel techniques.

The main contributions of the paper are as follows:

- Based on extensive characterization and experimentation on a diverse set of workloads, we argue that different placement and migration policies are required for data and page table pages in tiered memory systems.
- To the best of our knowledge, this is the first work that focuses on efficient placement and migration of page tables on tiered memory systems.
- A differentiating placement policy within the page table where a small but critical part of page table pages are allocated on DRAM while the rest of the page table pages are dynamically managed by migrating between memory tiers.

The rest of the paper is organized as follows: we provide the necessary background in Section 2 followed by the motivation for the paper in Section 3. We present our design in Section 4 and implementation details in Section 5. We evaluate the performance of Radiant in Section 6. We briefly discuss related works in Section 7 and finally, conclude in Section 8.

# 2 Background

In this section, we cover the necessary background required for the rest of the paper.

## 2.1 Optane Persistent Memory

Intel’s Optane Persistent Memory Module is a high-capacity non-volatile memory that is DDR4 socket compatible and fits into standard DIMM slots [17]. Optane can be used either as a high-capacity volatile main memory (Memory Mode and Flat Mode) or as a persistent memory (App Direct Mode) [18, 29, 38]. High capacity volatile memory is useful for large memory footprint applications as they can exploit the advantage of the additional memory capacity without requiring application modifications. For example, Optane can seamlessly enable large-scale in-memory graph analytics for graphs with billions of edges [13].
In this work, we use Optane as a high-capacity volatile memory in Flat Mode (also referred to as DRAM-NVMM hybrid mode [29]). The difference between Memory Mode and Flat Mode is that in Memory Mode, Optane acts as a byte-addressable volatile main memory while DRAM acts as a cache. In Flat Mode, both DRAM and Optane memory can be accessed as a unified, but heterogeneous, byte-addressable memory. The advantage with Flat Mode is that the applications can control and optimize the placement of data between low latency DRAM and high latency Optane [15, 35]. We configure the system in Flat Mode using ndctl tool [27] and daxctl utility [10]. Step by step guide to configure Optane as a hot-plugged main memory is available in Persistent Memory Development Kit (PMDK) [30]. Once configured in Flat Mode, Optane memory is reflected as “no-CPU” NUMA nodes in the system as shown in Figure 2 (node 2 and node 3). Support for Flat Mode is already part of the Linux kernel [14] and hence all the NUMA features (e.g., placement and balancing) in Linux are readily available for Optane-backed NUMA nodes as well.

**2.2 Page tables**

A page table maintains virtual address (VA) to physical address (PA) translations and is organized as a multi-leveled tree (x86_64 supports both 4-level and 5-level page tables; we use 4-level page table for the discussions in the rest of the paper\(^1\)) where a page global directory (PGD or L1) is the root of the tree. Each active entry in PGD points to a physical page containing an array of page upper directory (PUD or L2) entries. Similarly, each active entry in PUD points to a physical page containing an array of page middle directory (PMD or L3) entries. PMDs in turn point to a physical page (PTE or L4) containing an array of page table entries. A PTE entry contains the physical page address of the data page corresponding to the virtual address as shown in Figure 3.

\(^1\)A 4-level page table can map up to 256 TB of memory.

Upon a CPU TLB (Translation Lookaside Buffer) miss, the hardware – being aware of the page table tree layout – performs a page table walk to insert an entry in the TLB. Therefore, a TLB miss on a 4-level page table requires 4 memory accesses to walk the page table. As TLBs cover only a small portion of the total physical memory, most of the memory accesses by large memory footprint workloads cause a TLB miss requiring a page table walk.

In modern operating systems, page tables are dynamically allocated: the root of the page table tree for a process is allocated when the process is created. The physical pages to store the intermediate and leaf-level pages of the page table are allocated whenever the process page-faults on a valid virtual address for the first time.

**2.3 Userspace data page allocation and migration**

Modern operating systems such as Linux provide a stable and transparent technique for data page allocation on a multi-socket system. Additionally, they also provide mature interfaces or APIs for applications to explicitly control data page allocation. By default, Linux employs a first-touch policy [4, 12], which allocates data pages on a local NUMA node and falls back to remote nodes when there is not enough memory on the local node. Apart from this, an interleaved allocation policy [12] is also available where the data pages are allocated on all NUMA nodes in a round robin order. This improves memory bandwidth utilization by distributing the data pages across nodes and thus, avoids skewed allocation to a set of nodes [12].

In a NUMA system, accessing data from a remote node causes significant memory overheads incurring 2–4× higher latency than accessing the data from a local node [4]. Many solutions have been proposed over the last few decades to mitigate such performance issues [9, 23, 39]. One of the solutions that is widely accepted and used is to migrate the data pages from the remote NUMA node to a local NUMA node where the application is running.
Operating systems such as Linux provides well defined userspace APIs to trigger data page migrations between NUMA nodes [1]. In addition, operating systems are capable of transparently migrating frequently accessed data pages between NUMA nodes (e.g., AutoNUMA in Linux [7]). However, it is important to note that the page migration support is only available for userspace data pages; such support is not available for kernel pages and consequently, page table pages.

3 Motivation

In this section, we present a page table analysis for large memory footprint applications including the placement and distribution of page table pages, migration of page table pages and performance impact of page table placement. We draw important observations based on our analysis and design Radiant based on these observations and insights.

We run our experiments on a 2-socket Intel-Xeon Gold 6252N system with 192 GB DRAM and 800 GB Optane per socket running Linux kernel version 5.6 (system and configuration details in Table 1).

3.1 TLB misses

Large memory footprint applications running terabytes of memory usage incur frequent TLB misses as TLBs cover only a small portion of the total physical memory. Figure 4 shows the TLB Misses-Per-Kilo-Instructions (MPKI) for applications with large memory footprint (600 GB to 1 TB). A higher MPKI implies that a significant fraction of the memory accesses incurs TLB misses, thus requiring page table walks.

Due to high TLB misses, these applications spend up to 68% of the total execution cycles in page table walks. It is important to note that MMU employs caching techniques to cache the page table entries. Additionally, page table entries are also cached in system memory caches as MMU units access the page table through the memory hierarchy. Despite MMU caching and other TLB optimization techniques, large memory footprint applications still spend significant fraction of the total execution cycles in page table walks. Hence, optimizing page table walks are important for such applications.

Figure 4. TLB MPKI for applications with large memory footprint. Benchmark details in Table 2.

Figure 5. Page table distribution for Memcached when around 338 GB of data has been populated with interleaved allocation policy. Around 50% of page table pages end up in NVMM even when 190 GB of DRAM is free.

3.2 Page table placement

Operating systems dynamically allocate pages for all the four levels of page table on-demand, i.e., when the corresponding virtual address page faults for the first time. However, the NUMA node on which a page table page is allocated depends on multiple factors including the socket on which the allocating thread is running and the memory allocation policy of the application [9, 12]. It is important to note that operating systems employ the same allocation and placement policy for both data and page table pages.

When the memory interleave policy (round-robin allocation of pages across all NUMA nodes) is applied for an application, the Linux kernel applies the same data page allocation policy for the page table pages also and allocates them across all NUMA nodes. Figure 5 shows the placement of page table pages and data pages when around 338 GB of data has been populated in Memcached. It can be observed that around 50% (0.32 GB) of page table pages are allocated in Optane despite having around 190 GB free memory in DRAM.

Furthermore, when first-touch allocation policy is applied, allocation of page table pages spills over to Optane when DRAM is almost full. However, later when a part of DRAM memory is freed, data pages are migrate from Optane to DRAM. However, page table pages remain in Optane as they cannot be migrated.

As a result, in one scenario, page table pages can be allocated in NVMM even when enough free memory is available in DRAM and in another scenario page table pages allocated on NVMM remains on NVMM even when enough memory is freed on DRAM (Observation 1).
3.3 Page walk latency

The access latency of NVMMs are significantly higher than DRAM mainly due to the longer media latency. Hence, a hardware page table walk incurs higher walk latency when a page table entry is placed in NVMM. Additionally, a page table walk requires up to 4 memory accesses to NVMM when all the four levels of page table pages are allocated in NVMM. This further increases the page walk latency. It has also been observed that concurrent access to NVMMs, especially Optane, from multiple CPUs in a multi-core system can degrade performance due to limited internal buffers [38].

We measure the page walk latency when populating Redis with 1 TB of key-value pairs. We use the default placement policy (first-touch policy) which allocates data and page table pages from DRAM until the free memory in DRAM reaches a critical mark before falling back to NVMM. This further increases the page walk latency. It has also been observed that concurrent access to NVMMs, especially Optane, from multiple CPUs in a multi-core system can degrade performance due to limited internal buffers [38].

We measure the page walk latency when populating Redis with 1 TB of key-value pairs. We use the default placement policy (first-touch policy) which allocates data and page table pages from DRAM until the free memory in DRAM reaches a critical mark before falling back to NVMM. Page walk latency increases significantly (Figure 6) when the page table page allocation spills to NVMM (Observation 2).

3.4 Migration support

Techniques employed by operating systems and userspace applications to identify and migrate frequently accessed pages from NVMM to DRAM to improve application performance are restricted to data pages. To the best of our knowledge, most modern operating systems do not support migrating a page table page because page table pages are part of the kernel pages, which are unmovable. Once the page table pages are allocated, they remain fixed for their lifetime; they are reclaimed only when either the corresponding data pages are freed or the process is terminated. As a result, page table pages allocated on NVMM remain in NVMM.

Migrating a page table page is a non-trivial operation as it requires fixing the page table tree structure (a kernel data structure) to ensure that the virtual to physical address mappings are intact. In addition, page table page migration on a multi-core system requires careful handling of race conditions. For example, the page table page under migration can either be accessed by hardware during a page walk or can be accessed/modified by other CPUs to serve a page fault.

3.5 Page table binding

![Figure 7. L4 page table page allocation latency in case of the default Linux kernel and when the entire page table is binded to DRAM.](image)

A simple and straightforward approach to avoid page table pages spilling to NVMM is to bind the page table to DRAM. Even though this looks like a viable option, it results in pathological behaviour as we demonstrate by evaluating the Linux kernel patches [36] that propose to bind the page table to DRAM.\(^2\)

On a freshly booted system with 384 GB DRAM and 1.6TB Optane memory, we start populating Memcached with the default first-touch allocation policy. Initially, all new page allocations (both data and page table pages), as per first-touch policy, are directed to DRAM resulting in DRAM nodes filling up before Optane nodes (on our system DRAM is 19% of the total system memory). Once DRAM is almost full, new data page allocations are directed to Optane nodes, while the page table pages are still directed to DRAM due to DRAM binding. Forcing the allocation on almost-full DRAM nodes results in higher allocation latencies (Figure 7) because the buddy allocator falls back to slowpath functions.

In addition, continued page table allocation requests on almost-full DRAM nodes invokes page reclamation daemon. However, after a while, the Linux kernel fails to reclaim enough DRAM pages to serve page table page allocation and as a result triggers the out-of-memory (OOM) handler. OOM handler kills the Memcached server even when 700 GB of free memory is available in Optane NUMA nodes.

Out-of-memory issues can be mitigated to some extent by employing aggressive page reclamation heuristics, however, we address these challenges by efficiently handling the allocation and placement of page table pages across memory tiers. Our approach is to allow page table pages to spill over to NVMMs when allocation on DRAM is not possible and

\[^2\]These patches are not included in the Linux kernel; Linux kernel v5.6 still allows allocation of page table pages on Optane NUMA nodes.
then dynamically and transparently migrate the page table pages between the memory tiers.

3.6 Summary
To summarize, we argue that with the growing relevance of large tiered memory systems, it is important to explore efficient page table allocation and placement technique across memory tiers, which has received least attention till now.

4 Radiant design
We propose an efficient and transparent page table management technique to reduce page walk overheads on tiered memory systems. In this section, we present the design of Radiant.

4.1 Design considerations
Differentiate between data and page table pages: Large memory footprint applications with terabytes of memory incur frequent TLB misses. The performance of such applications is sensitive to the placement of page table pages in a tiered memory system. Hence, it is necessary to consider different allocation and placement policies for data and page table pages.

Differentiate between NVMM and DRAM memory: Carefully consider the underlying memory heterogeneity (e.g., capacity, latency) while deciding on the placement of page table pages.

We propose the following two techniques that incorporate the above design considerations along with the observations made during page table analysis in §3.

4.2 Binding critical page table pages to DRAM
The read latency on NVMM is 3× higher than DRAM mainly due to the longer media latency. As a page table walk requires 4 memory accesses, the page table walk latency is significantly higher when all the four levels of the page table pages are allocated on NVMM. Even though a typical page table for a large memory footprint application can occupy a small fraction of DRAM, binding the entire page table to DRAM can result in pathological behaviour as demonstrated in §3.5.

We observe that a majority of the page table memory is consumed by leaf level or L4 page table pages; L1, L2, and L3 page table pages together consume insignificant amount of memory. For example, an application with around 2 TB memory footprint requires around 4 GB memory for L4 pages and collectively requires around 7.62 MB for L1, L2 and L3 page table pages (size estimation in Figure 3). We exploit this insight to significantly reduce the amount of time spent on page table walks.

Our placement strategy is to dynamically allocate and bind L1, L2, and L3 page table pages in DRAM. With such a placement technique, during a 4-level page walk, 3 out of 4 memory accesses are guaranteed from low latency DRAM thus drastically reducing the page walk cycles. It is important to note that we achieve this by strategically placing less than 0.18% of page table pages in the critical DRAM memory.

Such a policy not only improves the application execution time but also improves startup or initialization time for large memory footprint applications. For example, when populating initial key-values in an in-memory database, initializing a large graph or restoring a VM snapshot, a large portion of L1, L2, and L3 page table pages are initialized and accessed (e.g., zeroing a newly allocated page table page). Hence, placing them in DRAM reduces the startup time of applications.

Our strategy, as opposed to placing the entire page table in DRAM [36] has several advantages. First, we drastically minimize the amount of page table pages that requires binding to DRAM. For example, we bind only 7.62 MB for a 2 TB workload which is less than 0.0019% of DRAM on our evaluation system. In contrast binding the entire page table requires 4 GB of DRAM. Second, by using less than 0.0019% of DRAM for binding we guarantee 75% of page table pages from DRAM. Finally, even under extreme memory pressure operating systems can allocate L1, L2, and L3 page table pages in DRAM by reclaiming a small amount of DRAM memory. While binding the entire page table requires reclaiming few GBs of DRAM memory which can trigger out-of-memory handler.

4.3 Page table migration
We allow allocation of L4 page table pages, which constitutes the majority of the page table, on both DRAM and NVMM. Further, we use data-page-migration triggered page table migration technique to efficiently identify and migrate L4 pages between DRAM and NVMM.

The rational behind such an approach is that a data page migration provides crucial hint on the placement of the corresponding L4 page table page. For example, migration of a hot data page from NVMM to DRAM hints that the corresponding L4 page table page, if present on NVMM, should also be migrated. Because, for a large memory footprint application with terabytes of memory even a hot data page incurs frequent TLB misses (as the amount of hot data far more exceeds the TLB reach) resulting in frequent accesses to L4 page by the hardware page walker. Therefore, when a data page is migrated between memory tiers we trigger the migration of the corresponding L4 page table page.

Operating systems such as Linux provides well defined userspace API [1] to trigger data page migrations to enable novel userspace techniques to efficiently identify and migrate data pages between memory tier. For example, identifying and migrating hot and cold data pages between memory tiers or speculatively pre-migrating a set of data pages between DRAM and NVMM based on the application’s memory access patterns. In addition, operating systems are capable of
Algorithm 1 Algorithm to migrate an L4 page

1: procedure Migrate_Data(data_page, dest_node)
2:    data_page_new ← alloc_page(dest_node)
3:    rc=migrate_data_page(data_page, data_page_new, dest_node)
4:    if rc==SUCCESS then
5:        migrate_L4(data_page_new, dest_node)  // Migrate L4 page
6:    end if
7:  end procedure

8: procedure migrate_L4(data_page_new, dest_node)
9:    /* Walk the page table */
10:    (L4, L3) ← get_pt_entries(data_page_new)
11:    L4_node ← page_node(L4)  // Get L4’s node
12:    if L4_node == dest_node then
13:        return  // Already in destination
14:    end if
15:    if L4_node in DRAM and dest_node in DRAM then
16:        return  // Already in DRAM (similarly for NVMM)
17:    end if
18:    if any data page pointed by L4 in DRAM then
19:        return  // L4 pointing to a page in DRAM
20:    end if
21:    if lock(L4 and L3) then  // Lock L4 and L3 pages
22:        return  // Allocate a L4 page on the destination NUMA node!
23:    end if
24:    L4_new ← alloc_page(dest_node)
25:    tlb_flush()  // Invalidate L4 old mappings
26:    memcpy(L4_new, L4, 4096)  // Copy the L4 page
27:    update_L3(L4_new)  // Sync. point
28:    unlock(L3 and L4)  // Unlock the L3 and L4 pages
29: end if
30: end procedure

4.4 Page table migration details

Algorithm 1 and Figure 8 show the steps involved in migrating an L4 page table page. Whenever a data page migration is initiated either by an userspace program or by the kernel (e.g., AutoNUMA), we trigger the migration of the corresponding page table page. The L4 page migration is initiated after the corresponding page data page migration is successfully completed (Line 4).

To migrate a page table page we first fetch L4 and L3 pages corresponding to the new data page (data_page_new) by performing a software page table walk (Line 11). Once we have L4 page, we get its NUMA node. We skip the migration if L4 page is already in the destination NUMA node (Line 14) or if the migration is from one DRAM (or NVMM) node to another DRAM (or NVMM) node (Line 16). We also skip the migration of L4 page from DRAM to NVMM if any data page pointed by L4 is in DRAM (Line 19).

On meeting all the necessary conditions, we start the migration by locking L4 and L3 page tables. Locking is required to synchronize between parallel data or L4 migrations, which is common in multi-core systems. Now we allocate a new L4 page (L4_new) on the destination NUMA node. If successful, we flush the TLB and MMU caches to invalidate any entries pointing to old L4 page and then copy the contents from old L4 page to L4_new and update L3 to point to L4_new (Line 27).

TLB flushing forces a hardware page walk on CPUs that concurrently attempt to access the old L4 page under migration, while an invalid old L4 entry triggers a page fault. The operating system’s page fault handler being aware of the ongoing L4 migration waits for the migration to complete before inserting the updated mapping.

4.4.1 Page table consistency. In a multi-core system, multiple CPUs can concurrently try to access an L4 page under migration in the software page fault handler. Furthermore, similar to a data page migration, an L4 page migration can also be triggered simultaneously, thus, requiring explicit synchronization during a page table migration. We also need to ensure that the hardware page table walker sees a consistent state of the page table at all the times.

Even though Algorithm 1 provides generic steps to migrate an L4 page, the actual implementation and sequence of steps (e.g., when to flush TLB entries) may vary depending on the underlying architecture and the operating system.

5 Implementation

In this section, we explain the implementation details of Radiant for x86_64 architecture in the Linux kernel. We use...
the Linux kernel’s terminology to refer to different levels of a page table; L1 is referred as PGD, L2 as PUD, L3 as PMD, and L4 as PTE.

As explained before, the default kernel only migrates data pages during a migration. Enabling PTE migration on a multi-core system is not trivial; a simple pointer flip at the PMD-level and freeing of the old PTE page is not enough. We list down a few challenges in implementing PTE migrations on a production-class operating system such as Linux:

1. Multiple CPUs in a multi-core system, upon a TLB miss, can concurrently perform page walk by accessing the page table pages using the physical addresses. Hence, we need to ensure that the hardware always sees a consistent page table.

2. As a PTE page points to 512 data pages, it is possible to have multiple concurrent migrations of these data pages to different NUMA nodes. Every such instance of successful data migration triggers a PTE page migration. We need to ensure that the page table is consistent without causing a significant performance overhead.

In the subsequent sections, we explain implementation details including challenges and solutions.

5.1 Binding the page table pages

The default Linux kernel allows us to specify memory policies for applications to bind to specific NUMA nodes. However, Linux does not support binding page table pages independent of the data pages. We modify the page table page allocation functions in the kernel, pgd_alloc, pud_alloc, and pmd_alloc, to add support to bind PGD, PUD, and PMD pages in DRAM.

We extend the numactl utility to select the processes for which the high-level pages of a page table should be placed in DRAM. Placement of high-level page table pages is independent of data page placement for processes enabled with numactl binding. Rest of the processes in the system follow the data page placement policy for page table pages.

5.2 PTE migrations

The Linux kernel ensures that a data page under migration is completely isolated from the rest of the system. Any page fault on this page waits either on the locked PTE or the locked data page until the migration is complete.

As shown in Figure 8, we first try to acquire the PMD lock. If successful, a new PTE page is allocated on the destination NUMA node using alloc_pages_node() function. Then, we copy the page content from the old PTE page to the new PTE page and fix the page table (update the PMD entry to point to this new PTE).

We also flush the TLB entries and MMU cache to clear the old PMD to PTE mappings. But, the PTE to data page mappings are still valid as we copy the contents of old PTE page to the new PTE page (see Figure 8). After the PMD to new PTE page mapping is updated in the page table, any TLB miss will use the new PTE page instead of the old PTE page; the hardware need not wait for the release of the lock on the old PTE page.

5.3 Performance implications

The page table of a process has three types of locks; a page table lock, a per-PMD page lock, and a per-PTE page lock (see Figure 3). The per-PTE page lock allows for parallel updates across different PTE pages without locking the whole page table. This significantly improves the performance of operations on the last level of the page table in a multi-core system [8, 11].

As explained in Section 4.4, we obtain the PMD lock prior to updating the PMD entries. This is required to avoid a race condition where a parallel migration on another CPU updates the PMD entry. However, locking the PMD serializes the migration of data pages mapped within the PMD with the migration of the corresponding PTE pages. This delays the completion of a data page migration, which in turn increases the page fault latency as the Linux kernel’s fault handler has to wait for the completion of the migration. To mitigate the latency overheads, we try to lock the PMD using try_lock() prior to migrating a PTE page. If we cannot get the lock, we skip the PTE page migration. As a PTE page points to 512 data pages, it is possible that we will get many more opportunities to migrate the PTE page.

6 Evaluation

In this section, we evaluate the performance of Radiant on a suite of real-world applications and synthetic benchmarks, and compare it with the Linux kernel’s memory allocation policies and management techniques. Table 1 provides details on the experiment setup. Support for transparent huge page (THP) is disabled unless otherwise stated. We use an unmodified Linux kernel 5.6 for all our baseline evaluations and enhance it to implement Radiant. Table 2 lists the workloads and Table 3 lists the conventions used for the evaluation.

6.1 Evaluation strategy

We contrast the performance of Radiant techniques with two memory allocation policies in the default Linux kernel.
A key computational kernel of RSS Size benchmarks for index look-ups in-memory key-value store. A benchmarks for hash-table probing used in database and other large applications. A key computational kernel of the Monte Carlo neutron transport algorithm. A graph traversal algorithm.

| Name         | Description                                                                 | RSS Size (Page table size) |
|--------------|-----------------------------------------------------------------------------|----------------------------|
| Memcached [25] | A commercial distributed in-memory object caching system. Setting: VC3B [6]: 2M objects. Read using a Zipfian distribution [26]. | 1 TB (1.9 GB)              |
| Redis [21]   | A commercial in-memory key-value store. Setting: Same as Memcached.          | 1 TB (1.9 GB)              |
| BTree [2]    | A benchmarks for index look-ups used in database and other large applications. Setting: 7.3B elements with 40 M look-ups. | 666 GB (1.2 GB)            |
| HashJoin [3] | A benchmark for hash-table probing used in database applications and other large applications. Setting: 6 B elements. | 838 GB (1.6 GB)            |
| XSBench [34] | A key computational kernel of the Monte Carlo neutron transport algorithm [34]. Setting: 2M grid points. | 1 TB (1.9 GB)              |
| BFS [33]     | A graph traversal algorithm. Setting: Real order 30 graph [33]               | 600 GB (1.1 GB)            |

Table 2. Workloads used to evaluate the performance of Radiant

| Radiant techniques | Description                                                                 |
|--------------------|-----------------------------------------------------------------------------|
| BHi                | Bind high-level (PGD, PUD and PMD) page table pages in DRAM                 |
| Mig                | Enable migration of last-level (PTE) page table pages                       |
| BHi+Mig            | Enabling binding of high-level page table pages along with migration for the last-level of the page table. |

Table 3. Conventions used in the paper for discussion

First is the default first-touch policy [4, 12]. In this case, the NUMA node for the page table pages are selected based on the data page allocation policy, i.e., a page table page is allocated on the same NUMA node where the data page that is running the application is located. This policy allocates a page table close to the CPU; however, allocations can spill over to remote nodes when an allocation request cannot be served from the local NUMA node [12].

Second is the interleaved policy where the Linux kernel distributes the data uniformly across all the NUMA nodes in a round-robin order to improve memory bandwidth utilization.

To enable PTE migrations, we rely on the Linux kernel’s memory management technique called AutoNUMA to get data page migration hints. By default, AutoNUMA dynamically migrates data pages only (not page table pages) across NUMA nodes to improve local NUMA accesses from a CPU. We run the experiments with AutoNUMA enabled unless otherwise mentioned.

Our evaluation strategy is as follows:

- **Full-system run**: Run the workloads with full system capacity utilizing maximum possible resources, which reflects a typical real-world data center scenario. We compare the performance of Radiant (BHi and BHi+Mig) with Linux kernel’s first-touch policy, and show that enabling PTE migrations improves the performance.

- **Multi-tenant scenario**: Evaluate the performance benefits of Radiant in a multi-tenant environment (a typical cloud setting), where different applications can start and exit at any point in time. We show that enabling PTE migration (BHi+Mig) for applications significantly improves performance.

- **Interleaved setting**: Compare the performance of Radiant (BHi) with the interleaved memory allocation policy, with AutoNUMA disabled. We show that differentiating between allocation of data and page table pages improves the performance.

- **Start up time**: At the startup of a large memory footprint application, a significant portion of high-level (PGD, PUD, and PMD) page table pages are initialized. We evaluate the performance benefits of BHi in such scenarios.

- **Huge page impact**: Evaluate the performance benefits of Radiant when huge pages are enabled.

### Run Time Cycles Walk Cycles Stall Cycles

|          | Full system run: First-touch policy | Multi-tenant scenario: First-touch policy | Interleaved: AutoNUMA disabled, Interleaved policy |
|----------|-------------------------------------|------------------------------------------|-----------------------------------------------|
| BHi      | 2.79% 3.32% 4.56% 5.68%             | BHi+Mig 17.95% 19.85% 32.62% 23.25%       | BHi+Mig 10.41% 10.02% 10.53% 9.01%         |
| BHi+Mig  | 20.39% 20.71% 12.38% 20.9%            |                                             |                                               |

### Start up time improvement: AutoNUMA disabled (Redis)

| Time     | Avg Lat. | Max Lat. | 95thtile Lat. | 99thtile Lat. |
|----------|----------|----------|---------------|---------------|
| BHi      | 22.81% 22.82% 17.35% 25.56% 20.70% |

Table 4. Radiant performance improvement summary (geometric-mean across all the workloads). A higher value indicates better performance improvement with Radiant.

6.2 Full-system run

We evaluate the performance with the memory footprint size as specified in Table 2 utilizing maximum possible system resources. We compare the performance of the Linux kernel’s first-touch policy (baseline) with Radiant (BHi and BHi+Mig) techniques (see Figure 9).

**BHi**: The high-level page table pages are frequently accessed.
during a page table walk. Binding them to DRAM ensures a low-latency access during a page table walk and reduces the walk cycles by up to 17.31%. Placement on DRAM also reduces the stall cycles by up to 19.18%. This translates into a reduction of total cycles by up to 11.43% and a run-time improvement of up to 9.08% (see Table 4).

**BHi+Mig** : With PTE migrations enabled, the percentage of page table pages in DRAM increases (e.g., from 19.6% to 34.0% for Redis). This reduces the walk cycles by up to 28.06% and the stall cycles by up to 59.57%. This causes a reduction in the total cycles by up to 61.19% and improves the run-time by up to 60.88% (see Figure 9a).

### 6.3 Multi-tenant scenario

In a typical cloud setting, where tiered memory is likely to be deployed, many applications co-exits in parallel in a given period of time. Here, different applications may start or exit at any time.

An application (V) started when DRAM is almost full is allocated memory (data and page table pages) on NVMM. At a later point in time when other applications using DRAM exit, DRAM becomes free resulting in the migration of the data pages of V from NVMM to DRAM. However, with the default Linux kernel, page table pages are not migrated from NVMM to DRAM. However, with the default Linux kernel, page table pages are not migrated from NVMM to DRAM. It is observed that DRAM is almost full when an application starts, followed by the free of significant portion of DRAM memory. This triggers migration of the benchmark application’s data pages from NVMM to DRAM.

To setup the environment, we first launch applications that fills up DRAM. These applications also frequently access the data pages in DRAM. Then we launch our benchmark application. As DRAM memory is full, all the benchmark application’s memory is allocated on NVMM. After this, we terminate the applications that filled up DRAM resulting in freeing of significant portion of DRAM memory. This triggers migration of the benchmark application’s data pages from NVMM to DRAM.

| Workload | Data page migrations | Successful migration | Already in destination | With in DRAM |
|----------|----------------------|----------------------|------------------------|--------------|
| Memcached| 66,644,738           | 30,601               | 39,272,431             | 26,763,450   |
| Redis    | 33,315,590           | 69,731               | 27,461,927             | 5,783,941    |
| BTree    | 11,820,636           | 17,061               | 7,791,351              | 4,012,620    |
| HashJoin | 1,945,151            | 50,209               | 1,867,027              | 27,915       |
| XSBench  | 371,977              | 574                  | 285,933                | 85,470       |
| BFS      | 6,967,564            | 20,957               | 6,942,269              | 4,338        |

**Table 5.** Number of data page and PTE migrations in the controlled setting.

For this experiment, the system configurations remain the same as full-system run, however we run with a smaller input.

### Figure 10

**Figure 10.** Performance comparison of Radiant (Mig) in a multi-tenant environment with AutoNUMA (baseline). Bars in (a) show total cycles. Bars are color-coded to differentiate between the Linux kernel’s and Radiant techniques.
size (see Figure 10). BHi+Mig reduces the walk cycles by up to 61.34% and stall cycles by up to 54.88%. This reduces the total cycles by up to 50.75% and improves the run-time by up to 50.77% (see Figure 10). Table 5 shows the number of data page migrations triggered and the number of successful PTE migrations. We also show the reason for not migrating a PTE page (a PTE page is already in DRAM or in the destination NUMA node). As a PTE page points to 512 data pages, the first data page that is migrated to DRAM triggers a PTE page migration; for the rest 511 data page migrations, PTE migration is not required as it is already in DRAM.

Figure 11. Performance evaluation of Radiant (BHi) for Memcached in an interleaved setting with AutoNUMA disabled.

6.4 Interleaved vs. Radiant
Interleaved memory allocation policy allocates the page table pages and the data pages on DRAM and NVMM in a round robin manner. Radiant still follows the interleave policy for data pages, but binds the high-level page table pages to DRAM. We compare the performance of BHi with the default kernel allocation (Figure 11). As AutoNUMA is disabled for this experiment, page table pages are not migrated and hence we do not report BHi+Mig statistics. We can clearly observe that having a different placement and allocation policy for data and page table pages is beneficial.

BHi: Binding the high-level pages in DRAM reduces the walk cycles up to 49.48% and stall cycles by up to 43.42%. This reduces the total cycles by up to 50.51% and improves the run-time by up to 51.75%. It can be further observed from Figure 12 that page walk latency decreases when we bind the high-level page table pages in DRAM as the interleaved allocation policy spreads the high-level page table across the DRAM and NVMM nodes.

6.5 Improving application start up time
During an application start up there are many data page faults that requires a page table walk. By placing the high-level page table pages in DRAM, we reduce the cycles spent on page table walks. While inserting 1 TB of data in Redis, we reduce the total page walk cycles by $\approx 9\%$. This results in a 21% reduction in total stalls cycles, that corresponds to an improvement of 22% in total start up time, when compared with default first-touch policy (see Figure 1 and Table 4).

6.6 Huge page impact
We evaluate the performance of Radiant when transparent huge page (THP) support is enabled. Figure 13 shows that BHi improves performance when THP is enabled. BHi binds PGD, PUD, and PMD levels of the page table to DRAM. For a huge page as a PMD page is the last or leaf-level page (no PTE page), BHi is effectively binding the entire page table resulting in performance improvement. However, BHi+Mig does not improve performance as there are no PTE-level pages to migrate.

6.7 Discussions
In a modern out-of-order CPU, a page table walk performed by the Page Miss Handler (PMH) in the hardware can overlap with other work [4]. Hence, a reduction in page table walk cycles need not always result in the reduction in execution cycles. We use the hardware performance counters to reason and understand the impact of reduction in page table walk cycles.

Figure 14 shows the counters for BFS from full system run (§6.2). It can be observed that the instructions executed,
Finally, Radiant employs the novel data-page-migration triggered page table page migration technique to identify and migrate page table pages between DRAM and NVMM. Mitosis neither identifies nor migrates relevant page table pages.

| Radiant | Mitosis |
|---------|---------|
| Tiered Memory Support | Yes | No |
| Migration Support | Direct | Via replication |
| Migration b/w DRAM and NVMM | Yes | No |
| Page table DRAM binding | L1, L2, L3 | None |
| Replication | No | Yes |
| Page table sync. overheads | No | Yes |
| Hot PTE page identification | Yes | No |

Table 6. Comparison of Radiant with Mitosis

7.2 Linux kernel community

Linux kernel patches [36] posted in the Linux Kernel Mailing List (LKML) propose to bind all the page table pages in DRAM to avoid accessing it from NVMM (this patch is not a part of the Linux kernel). However, such an approach results in pathological behaviour mentioned in §3.5. Radiant proposes to bind only 0.18% of the page table pages in DRAM (i.e., L1, L2 and L3 pages) and dynamically migrates L4 pages between DRAM and NVMM.

8 Conclusion

In this paper, we show that explicit and efficient management of page table on tiered memory systems with terabytes of memory is important. We study the performance impact of page table placement and argue that different placement and migration policies are required for data and page table pages. We demonstrate that binding a small but critical page table pages to DRAM and dynamically managing the rest of the page table pages by enabling migration results in significant performance improvement on systems with terabytes of NVMM memory.

References

[1] [n. d.]. move_pages(2) - Linux man page. https://linux.die.net/man/2/move_pages. ([n. d.]).
[2] Reto Achermann. 2020. mitosis-project/mitosis-workload-btree: The BTree workload used for evaluation. https://github.com/mitosis-project/mitosis-workload-btree. (September 2020). (Accessed on 10/03/2020).
[3] Reto Achermann. 2020. mitosis-project/mitosis-workload-hashjoin: The HashJoin workload used for evaluation. https://github.com/mitosis-project/mitosis-workload-hashjoin. (September 2020). (Accessed on 10/03/2020).
[4] Reto Achermann, Ashish Panwar, Abhishek Bhattacharjee, Timothy Roscoe, and Jayneel Gandhi. 2020. Mitosis: Transparently Self-Replicating Page-Tables for Large-Memory Machines. In Proceedings of the Twenty-Fifth International Conference on Architectural Support
Page Table Management for Heterogeneous Memory Systems

for Programming Languages and Operating Systems (ASPLOS ‘20). Association for Computing Machinery, New York, NY, USA, 283–300. https://doi.org/10.1145/3373376.3378468

[5] Arkaprava Basu, Jayneeel Gandhi, Jichuan Chang, Mark D. Hill, and Michael M. Swift. 2013. Efficient Virtual Memory for Big Memory Servers. In Proceedings of the 40th Annual International Symposium on Computer Architecture (ISCA ’13). Association for Computing Machinery, New York, NY, USA, 237–248. https://doi.org/10.1145/2485922.2485943

[6] Brian F. Cooper, Adam Silverstein, E. Tam, R. Ramakrishnan, and R. Sears. 2010. Benchmarking cloud serving systems with YCSB. In SoCC ’10.

[7] Jonathan Corbet. 2012. AutoNUMA: the other approach to NUMA scheduling [LWN.net]. https://lwn.net/Articles/488709/. (March 2012). (Accessed on 10/04/2020).

[8] Jonathan Corbet. 2013. Split PMD locks [LWN.net]. https://lwn.net/Articles/568076/. (September 2013). (Accessed on 09/30/2020).

[9] Mohammad Dashi, Alexandra Fedorova, Justin Funston, Fabien Gaud, Renaud Lachaize, Baptiste Lepers, Vivien Quema, and Mark Roth. 2013. Traffic Management: A Holistic Approach to Memory Placement on NUMA Systems. SIGPLAN Not. 48, 4 (March 2013), 381–394. https://doi.org/10.1145/2499368.2451157

[10] DAXCTL. [n. d.]. DAXCTL Man Pages - NDCTL User Guide. https://docs.pmem.io/ndctl-user-guide/daxctl-man-pages. ([n. d.]). (Accessed on 10/05/2020).

[11] Linux Kernel documentation. [n. d.]. Split page table lock — The Linux Kernel documentation. https://www.kernel.org/doc/html/latest/vm/split_page_table_lock.html. ([n. d.]). (Accessed on 09/30/2020).

[12] Fabien Gaud, Baptiste Lepers, Justin Funston, Mohammad Dashi, Alexandra Fedorova, Vivien Quema, Renaud Lachaize, and Mark Roth. 2015. Challenges of Memory Management on Modern NUMA Systems. Commun. ACM 58, 12 (Nov. 2015), 59–66. https://doi.org/10.1145/2814328

[13] G. Gill, Roshan Dathathri, Loc Hoang, R. Peri, and K. Pingali. 2020. Single machine graph analytics on massive datasets using Intel optane DC persistent memory. Proceedings of the VLDB Endowment 13 (2020), 1304 – 1318.

[14] Dave Hansen. 2019. Allow persistent memory to be used like normal RAM. https://patchwork.kernel.org/cover/10829019/ . (Feb 2019).

[15] Mark Hildebrand, Jawad Khan, Sanjeev Trika, Jason Lowe-Power, and Venkatesh Akella. 2020. AutoTM: Automatic Tensor Movement in Heterogeneous Memory Systems Using Integer Linear Programming. In Proceedings of the Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS ’20). Association for Computing Machinery, New York, NY, USA, 875–890. https://doi.org/10.1145/3373376.3378465

[16] S. Hong. 2010. Memory technology trend and future challenges. (2010). 12.4.1–12.4.4.

[17] Intel. [n. d.]. Intel Optane DC Persistent Memory. https://www.intel.com/content/dam/www/public/us/en/documents/product-briefs/optane-dc-persistent-memory-brief.pdf. ([n. d.]).

[18] Joseph Izraelevitz, Jian Yang, Lu Zhang, Juno Kim, Xiao Liu, Amir-samn Memaripour, Yun Joon Soh, Zixuan Wang, Yi Xu, Subramanya R. Dullouro, Jishen Zhao, and Steven Swanson. 2019. Basic Performance Measurements of the Intel Optane DC Persistent Memory Module. (2019). arXiv:1903.05714

[19] S. Kannan, A. Gavrilova, V. Gupta, and K. Schwan. 2017. HeteroOS – OS design for heterogeneous memory management in datacenter. In 2017 ACM/IEEE 44th Annual International Symposium on Computer Architecture (ISCA). 521–534.

[20] K. Kim. 2008. Future memory technology: challenges and opportunities. (2008). 5–9.

[21] Redis Labs. [n. d.]. Redis. https://redis.io/. ([n. d.]). (Accessed on 10/05/2020).

[22] Benjamin C. Lee, Engin Ipek, Onur Mutlu, and Doug Burger. 2009. Architecting Phase Change Memory as a Scalable Dram Alternative. In Proceedings of the 36th Annual International Symposium on Computer Architecture (ISCA ’09). Association for Computing Machinery, New York, NY, USA, 2–13. https://doi.org/10.1145/1555754.1555758

[23] Baptiste Lepers, Vivien Quema, and Alexandra Fedorova. 2015. Thread and Memory Placement on NUMA Systems: Asymmetry Matters. In Proceedings of the 2015 USENIX Conference on Usenix Annual Technical Conference (USENIX ATC ’15). USENIX Association, USA, 277–289.

[24] L. Liu, S. Yang, L. Peng, and X. Li. 2019. Hierarchical Hybrid Memory Management in OS for Tiered Memory Systems. IEEE Transactions on Parallel and Distributed Systems 30, 10 (2019), 2223–2236.

[25] Memcached. 2020. memcached - a distributed memory object caching system. https://memcached.org/. (/). (Accessed on 10/03/2020).

[26] N. Unnikrishnan Nair, P.G. Sankaran, and N. Balakrishnan. 2018. Chapter 8 - Multivariate Lifetime Models. In Reliability Modelling and Analysis in Discrete Time, N. Unnikrishnan Nair, P.G. Sankaran, and N. Balakrishnan (Eds.). Academic Press, Boston, 387 – 428. https://doi.org/10.1016/B978-0-12-801913-9.00008-7

[27] NDCTL. [n. d.]. NDCTL Man Pages - NDCTL User Guide. https://docs.pmem.io/ndctl-user-guide/ndctl-man-pages. ([n. d.]). (Accessed on 10/05/2020).

[28] Chang Hyan Park, Taekyung Heo, Jungi Jeong, and Jaehyuk Huh. 2017. Hybrid TLB Coalescing: Improving TLB Translation Coverage under Diverse Fragmented Memory Allocations. (2017), 444–456. https://doi.org/10.1145/3079856.3080217

[29] Onkar Patil, Latchesar Ionkov, Jason Lee, Frank Mueller, and Michael Lang. 2019. Performance Characterization of a DRAM-NVM Hybrid Memory Architecture for HPC Applications Using Intel Optane DC Persistent Memory Modules. In Proceedings of the International Symposium on Memory Systems (MEMSYS ’19). Association for Computing Machinery, New York, NY, USA, 288–303. https://doi.org/10.1145/3357526.3357541

[30] PMEM.IO. [n. d.]. Volatile use of persistent memory as a hotplugged memory region. https://pmem.io/2020/01/20/memkind-dax-kmem.html. ([n. d.]).

[31] Georgios Psaropoulos, Ismail Oukid, Thomas Legler, Norman May, and Anastasia Allamaki. 2019. Bridging the Latency Gap between NVM and DRAM for Latency-Bound Operations. In Proceedings of the 15th International Workshop on Data Management on New Hardware (DaMoN’19). Association for Computing Machinery, New York, NY, USA, Article 13, 8 pages. https://doi.org/10.1145/3329785.3329917

[32] Jee Ho Ryoo, Nagendra Gulur, Shuang Song, and Lizy K. John. 2017. Re-thinking TLB Designs in Virtualized Environments: A Very Large Part-of-Memory TLB. (2017). 469–480. https://doi.org/10.1145/3079856.3080210

[33] J. Shun and G. Blelloch. 2013. Ligra: a lightweight graph processing framework for shared memory. In PPOPP ’13.

[34] John R Tramm, Andrew R Siegel, Tansima Islam, and Martin Schulz. 2014. XSbench - The Development and Verification of a Performance Abstraction for Monte Carlo Reactor Analysis. In PHYSOR 2014 - The Role of Reactor Physics toward a Sustainable Future. Kyoto. https://www.mcs.anl.gov/papers/P5064-0114.pdf

[35] T. Wang. [n. d.]. Baidu Feed Stream Services Restructures Its In-Memory Database with Intel Optane Technology. https://newsroom.intel.com/wp-content/uploads/sites/11/2019/08/baidu-feed-case-study.pdf. ([n. d.]).

[36] Fengguang Wu. 2018. x86/gptable: allocate page table pages from DRAM. https://lkml.org/lkml/2018/12/26/145. (Dec 2018).

[37] Z. Yan, Daniel Lustig, David Nellans, and Abhishek Bhattacharjee. 2019. Nimble Page Management for Tiered Memory Systems. In Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS ’19). Association for Computing Machinery, New York, NY, USA, 331–345.
[38] Jian Yang, Juno Kim, Morteza Hoseinzadeh, Joseph Izraelevitz, and Steve Swanson. 2020. An Empirical Guide to the Behavior and Use of Scalable Persistent Memory. In 18th USENIX Conference on File and Storage Technologies (FAST 20). USENIX Association, Santa Clara, CA, 169–182. https://www.usenix.org/conference/fast20/presentation/yang

[39] Kaiyuan Zhang, Rong Chen, and Haibo Chen. 2015. NUMA-Aware Graph-Structured Analytics. In Proceedings of the 20th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP 2015). Association for Computing Machinery, New York, NY, USA, 183–193. https://doi.org/10.1145/2688500.2688507