A Full X-Band Phased-Array Transmit/Receive Module Chip in 65-nm CMOS Technology

HYOHYUN NAM\textsuperscript{1}, (Student Member, IEEE), VAN-VIET NGUYEN\textsuperscript{1}, (Student Member, IEEE), VAN-SON TRINH\textsuperscript{1}, (Graduate Student Member, IEEE), JEONG-MOON SONG\textsuperscript{1}, (Student Member, IEEE), BOK-HYUNG LEE\textsuperscript{2}, AND JUNG-DONG PARK\textsuperscript{1}, (Senior Member, IEEE)

\textsuperscript{1}Division of Electronics and Electrical Engineering, Dongguk University, Seoul 04620, South Korea
\textsuperscript{2}Yongin Research Institute, Hanwha Systems, Gyeonggi-do 17121, South Korea

Corresponding author: Jung-Dong Park (jdpark@dongguk.edu)

This work was supported in part by the Grant-in-Aid of Hanwha Systems, and in part by the National Research Foundation of Korea grant funded by the Korea Government (MSIP) under Grant 2019M3F6A1106118.

ABSTRACT In this paper, we present a phased-array transceiver chip operating in full X-band (8–12 GHz) in 65-nm CMOS technology. The presented transceiver for the transmit/receive module (TRM) consists of a 6-bit passive phase shifter, a 6-bit attenuator, a bi-directional gain amplifier (BDGA), and a single pole double throw (SPDT) switch connected to the internal power amplifier (PA) and the low-noise amplifier (LNA) to serve as a duplexer. A 64-bit SPI scan-chain is integrated for digital TRM control. The transmitter achieves greater than 15 dB of power gain with 11.84 dBm at the output 1-dB compression point (OP1dB). To achieve a wideband operation of the passive phase shifter, we assigned two different resonant frequencies for the phase leading and lagging networks and aligned the slopes of their phase responses to have the desired phase shifts at the center frequency. The RMS phase error is less than 5°, and the RMS amplitude error is less than 0.45 dB for all phase and attenuation states within 8–12 GHz while dissipating 216 mW dc power from a 1 V power supply. The receiver shows greater than 15 dB of power gain and has a noise figure (NF) of less than 8.4 dB for the entire X-band. The RMS phase error and the RMS amplitude error are less than 5° and 0.45 dB, respectively, for all control states within 8–12 GHz. The receiver consumes 110 mW with a 1 V power supply. The transceiver chip occupies an area of 4 × 1.88 mm\textsuperscript{2}.

INDEX TERMS CMOS, phased arrays, phase shifter, transceivers, wideband.

I. INTRODUCTION

Active phased-array antenna (APAA) systems have been extensively spotlighted in areas such as satellite communications, wireless communications, and radar applications owing to their increased channel capacity, reduced transmit power requirement, improved signal-to-noise ratio, and immunity to strong interference.

Until recently, phased array systems have been used primarily in defense and space applications since an electrically scanned APAA can support much faster beam scanning in a more compact volume than a mechanically scanned antenna. The traditional phased-array antenna system in defense and space applications has employed an expensive transmit/receive module (TRM) assembled with high-cost and bulky III-V MMICs [1], [2] combined with a silicon-based baseband and digital control chip to achieve high performance.

Since hundreds or even thousands of TRMs can be incorporated in a phased array antenna system, depending on the application, it is essential that the TRM be compact, be low-cost, and have a low-power design without compromising its performance. Therefore, enormous amounts of research have been directed at silicon-based (SiGe BiCMOS or CMOS) fully integrated transceiver for the TRM in X-band APAA systems to resolve this challenging issue [3]–[16]. A successful design solution in conventional digital CMOS technology must address power consumption and production cost.

An all-RF phase shifting architecture (phase-shifting performed at RF frequencies) is usually used to construct typical APAA systems. Compared to an architecture that uses local oscillator (LO) or IF phase-shifting methods, an
passive phase shifter, we misaligned the resonant frequency lower power consumption.

In this paper, we present a fully integrated TRM chip operating in full X-band (8 – 12 GHz) in 65-nm CMOS technology. Compared with the previous work [15], the proposed TRM chip utilizes not only a single SPDT (three SPDT switches in [7]), but also shared phase shifter and attenuator (separate phase shifters and attenuators for Tx and Rx path [8]) by employing a bi-directional gain amplifier (BDGA) in Tx and Rx operations. Therefore, the proposed architecture has the advantage of reducing path loss and chip occupancy. Moreover, a wideband operation of the passive phase shifter could be achieved by assigning two separate resonant frequencies for the leading/lagging networks for the phase-shifting units where we controlled the slopes of their phase responses to meet the desired phase shifts at the center frequency.

Since the output power and the noise figure of the bi-directional transceiver with two-ports [13], [15] was limited by the performance of the BDGA, we implement a TRM chip with an SPDT switch to add PA and LNA separately. Also, the SPDT switch was used as a duplexer to select the Rx/Tx signal for bi-directional operation. The Rx path of the SPDT switch is connected to the output of the LNA from the Rx input, while the Tx path is connected to the PA for improved Tx output power. The TRM chip was fabricated in 65-nm CMOS technology with eight copper metal layers and one aluminum metal layer, and the top layer (3 µm) was used for passive component design.

This paper is structured as follows: Section II describes the detailed designs for the core blocks including the phase shifter, attenuator, switches, and amplifiers for wideband operation. The measurements of the chip are presented in Section III, followed by the conclusion in Section IV.

II. X-BAND TRANSCEIVER DESIGN

A. 6-BIT BROADBAND PASSIVE PHASE SHIFTER

The typical structure of an HP/band-pass(BP)/LP phase-shifting cell includes third-order T-type HP filters, L-C-L BP filters, C-L-C BP filters and π-type LP filters as shown in Fig. 2 to minimize the number of inductors required. In comparison with [13], [15], we designed a 5.625° phase shift cell with BP and LP networks instead of switch to significantly enhance the operating frequency range. Inductors usually consume most of the chip area. The element values of each HP and LP network from the center frequency using derived formulae. With this approach, more than 50 % of the operating range under 5° of RMS phase error was enhanced. A detailed analysis with derived design equations is presented in Section II.

A block diagram of the proposed X-band TRM chip is illustrated in Fig. 1. In comparison with [7], [8], the proposed TRM chip utilizes not only a single SPDT (three SPDT switches in [7]), but also shared phase shifter and attenuator (separate phase shifters and attenuators for Tx and Rx path [8]) by employing a bi-directional gain amplifier (BDGA) in Tx and Rx operations. Therefore, the proposed architecture has the advantage of reducing path loss and chip occupancy. Moreover, a wideband operation of the passive phase shifter could be achieved by assigning two separate resonant frequencies for the leading/lagging networks for the phase-shifting units where we controlled the slopes of their phase responses to meet the desired phase shifts at the center frequency.

In this paper, we present a fully integrated TRM chip operating in full X-band (8 – 12 GHz) in 65-nm CMOS technology. Compared with the previous work [15], the proposed TRM chip utilizes not only a single SPDT (three SPDT switches in [7]), but also shared phase shifter and attenuator (separate phase shifters and attenuators for Tx and Rx path [8]) by employing a bi-directional gain amplifier (BDGA) in Tx and Rx operations. Therefore, the proposed architecture has the advantage of reducing path loss and chip occupancy. Moreover, a wideband operation of the passive phase shifter could be achieved by assigning two separate resonant frequencies for the leading/lagging networks for the phase-shifting units where we controlled the slopes of their phase responses to meet the desired phase shifts at the center frequency.

Since the output power and the noise figure of the bi-directional transceiver with two-ports [13], [15] was limited by the performance of the BDGA, we implement a TRM chip with an SPDT switch to add PA and LNA separately. Also, the SPDT switch was used as a duplexer to select the Rx/Tx signal for bi-directional operation. The Rx path of the SPDT switch is connected to the output of the LNA from the Rx input, while the Tx path is connected to the PA for improved Tx output power. The TRM chip was fabricated in 65-nm CMOS technology with eight copper metal layers and one aluminum metal layer, and the top layer (3 µm) was used for passive component design.

This paper is structured as follows: Section II describes the detailed designs for the core blocks including the phase shifter, attenuator, switches, and amplifiers for wideband operation. The measurements of the chip are presented in Section III, followed by the conclusion in Section IV.
where \( \phi_1 \) and \( \phi_2 \) are insertion phases of HP and LP networks at their resonant frequencies \( f_1 \) and \( f_2 \), respectively. In conventional design methodology, HP and LP networks are considered to resonate at the same frequency, that is, the center frequency of operation \( f_0 \). It is also assumed that each network has half of the expected insertion phase shift but with opposite signs at \( f_0 \). Each circuit element is calculated from (1) – (4) by setting \( f_1 = f_2 = f_0 \) and \( \phi_1 = -\phi_2 = \Delta \phi_0/2 \).

However, this simplification undesirably limits the design space, which prohibits the network from operating at wideband. Thus, we eliminate this simplification in our work to significantly improve the phase error performance over the frequency band of interest. The phase responses of HP and LP networks, \( \phi_{HPN} \) and \( \phi_{LPN} \), as a function of frequency \( f \) are presented in (5) and (6), respectively.

\[
\begin{align*}
C_1 &= \frac{1}{2\pi f_1 Z_0 \tan(\phi_1/2)} \quad (2) \\
L_2 &= -\frac{Z_0 \sin(\phi_2/2)}{2\pi f_2}; \quad (3) \\
C_2 &= -\frac{\tan(\phi_2/2)}{2\pi f_2 Z_0}. \quad (4)
\end{align*}
\]

\[
\begin{align*}
\phi_{HPN}(f) &= \tan^{-1} \left[ \frac{f_1}{f} \tan \left( \frac{\phi_1}{2} \right) \frac{1 + \cos^2(\phi_1/2) - (f_1/f)^2 \sin^2(\phi_1/2)}{1 - 2(f_1/f)^2 \sin^2(\phi_1/2)} \right]; \quad (5) \\
\phi_{LPN}(f) &= \tan^{-1} \left[ \frac{f}{f_2} \tan \left( \frac{\phi_2}{2} \right) \frac{1 + \cos^2(\phi_2/2) - (f/f_2)^2 \sin^2(\phi_2/2)}{1 - 2(f/f_2)^2 \sin^2(\phi_2/2)} \right]. \quad (6)
\end{align*}
\]

A derivative of (5) and (6) with respect to \( f \) represents the slope of the insertion phases of two networks, as expressed in (7) and (8):

\[
\begin{align*}
\frac{d}{df} \phi_{HPN}(f) &= \frac{f_1}{f} \frac{a_1}{f^2} \frac{[2f_1^2 (f_1/f)^4 + 2c_1 (2b_1 - 3) (f_1/f)^2 + b_1]}{[1 - 2c_1 (f_1/f)^2]^2 + a_1^2 (f_1/f)^2 [b_1 - c_1 (f_1/f)^2]^2}, \quad (7)
\end{align*}
\]

\[
\begin{align*}
\frac{d}{df} \phi_{LPN}(f) &= \frac{1}{f_2} \frac{a_2}{f^2} \frac{[2f_2^2 (f/f_2)^4 + 2c_2 (2b_2 - 3) (f/f_2)^2 + b_2]}{[1 - 2c_2 (f/f_2)^2]^2 + a_2^2 (f/f_2)^2 [b_2 - c_2 (f/f_2)^2]^2}, \quad (8)
\end{align*}
\]

where \( a_1, b_1, c_1, a_2, b_2, c_2 \) are simplified as in

\[
\begin{align*}
a_1 &= \tan(\phi_1/2); \quad b_1 = 1 + \cos^2(\phi_1/2); \quad c_1 = \sin^2(\phi_1/2) \\
a_2 &= \tan(\phi_2/2); \quad b_2 = 1 + \cos^2(\phi_2/2); \quad c_2 = \sin^2(\phi_2/2)
\end{align*}
\]

To achieve wideband operation of the phase shifter with HP/LP networks, the slope of the phase response of each filter network should be equal and kept constant over the target frequency band. Figure 3 shows the phase responses of the HP and LP filter network for a 90° phase shift and their corresponding slopes. It can be observed that the slope of the phase response of the HP network is steadier in the high-frequency region about its resonant frequency \( f_2 \). Thus, to have the minimum phase error over the target frequency band, it is necessary to shift the resonant frequency of the HP network \( f_1 \) lower than the center frequency and that of the LP network \( f_2 \) higher than \( f_0 \). By setting the phase responses of each HP and LP network in opposite directions, we can achieve a flatter phase response slope in the band of interest. With this approach, the phase error is significantly improved within the band. The phase shift of a specific cell is the difference between the two transmission phases as expressed in (9). The phase slopes of the two networks at the center frequency \( f_0 \) should be aligned to achieve a constant phase shift over a specific frequency range. In other words, the optimized phase error happens when (10) and (11) are satisfied.

\[
\begin{align*}
\Delta \phi(f) &= \phi_{HPN}(f) - \phi_{LPN}(f) \quad (9) \\
\Delta \phi(f_0) &= \Delta \phi_0 \quad (10) \\
\Delta \phi(f_0) &= \frac{df}{df} \phi_{HPN}(f_0) - \frac{df}{df} \phi_{LPN}(f_0) \quad (11)
\end{align*}
\]

As can be observed from (7) and (8), (11) naturally happens when setting these constraints: \( f_1 f_2 = f_0^2 \) and \( \phi_1 = -\phi_2 \).
Applying the above constraints, (9) becomes

\[
\Delta \phi_0 = \tan^{-1} \left[ \frac{f_1 \tan \left( \frac{\phi_1}{2} \right) \left( 1 + \cos^2(\phi_1/2) - (f_1/f_0)^2 \sin^2(\phi_1/2) \right)}{f_0 \tan \left( \frac{\phi_1}{2} \right) \left( 1 - 2(f_1/f_0)^2 \sin^2(\phi_1/2) \right)} - \tan^{-1} \frac{f_0 \tan \left( -\phi_1/2 \right) \left( 1 + \cos^2(-\phi_1/2) - (f_0/f_2)^2 \sin^2(-\phi_1/2) \right)}{f_2 \tan \left( -\phi_1/2 \right) \left( 1 - 2(f_0/f_2)^2 \sin^2(-\phi_1/2) \right)} \right]
\]

(12)

The values of \( \phi_1 \) can be obtained by solving the above equation with \( f_1 \) and \( f_2 \) corresponding to the frequency band of interest. The value of each element in the HP and LP networks can be calculated from (1)-(4).

The circuit size of HP/LP phase shifters depends on their operating frequency range. For some frequency bands, the above topology and analysis generate impractical inductance and capacitance values. Therefore, it is necessary to employ a different configuration as a realizable solution. One of the candidates uses the BP configuration shown in Fig. 2 as the leading phase network, while the lagging phase network is realized with a third-order LP filter. The transmission phase of the BP network as a function of frequency is expressed in (13).

\[
\phi_{BPN}(f) = \tan^{-1} \left( 1 - \frac{af^2}{bf^2} \right)
\]

(13)

where \( a = 8\pi^2L_1C_1 = 1/f_1^2 \), \( b = 4\pi Z_0C_1 \), and \( f_1 \) is the resonant frequency. The derivative of (13) concerning the frequency \( f \) is the slope of the transmission phase of the BP network as shown in (14) where \( \phi_{B0} \) is the transmission phase at \( f_0 \).

\[
\frac{d}{df} \phi_{BPN}(f) = \frac{[(f_0/f_1)^2 - 1][f/f_1]^2 + f_0 \tan \phi_{B0}}{[1-(f_0/f_1)^2]^2 + [1-(f/f_1)]^2} = \frac{\phi_{B0}}{(f_0 \tan \phi_{B0})^2}
\]

(14)

From the condition \( \Delta \phi = \phi_{BPN}(f_0) - \phi_{LPN}(f_0) \), we have

\[
\phi_{B0} = \tan^{-1} \left[ \frac{f_0 \tan \left( \frac{\phi_2}{2} \right)}{f_2} \left( 1 + \cos^2(\phi_2/2) \right) - \frac{f_0^2 \sin^2(\phi_2/2)}{1 - 2f_0^2 \sin^2(\phi_2/2)} \right] + \Delta \phi_0
\]

(15)

From the condition \( d/df [\phi_{BPN}(f_0)] = d/df [\phi_{LPN}(f_0)] \), we have

\[
\frac{\phi_{B0}}{(f_0 \tan \phi_{B0})^2} = \frac{\phi_{B0}}{f_2 \tan \phi_{B0} \left[ 1 - (f_0/f_1)^2 \right] + \phi_{B0} \tan \phi_{B0} \left[ 1 - (f_0/f_1)^2 \right] + \phi_{B0} \tan \phi_{B0} \left[ 1 - (f_0/f_1)^2 \right]}
\]

(16)

where \( a_2 = \tan(\phi_2/2) \), \( b_2 = 1 + \cos^2(\phi_2/2) \), and \( c_2 = \sin^2(\phi_2/2) \).

The value of \( \phi_2 \) can be obtained from (15) and (16) with \( f_1 \) and \( f_2 \) as the frequency band of interest. The value of \( L \) and \( C \) for each network can then be easily calculated. Because the analysis does not take parasitic elements into account for simplicity, there are errors in the relative phase shift between the calculation and the simulation results.

The basic structures utilized in the proposed wideband phase shifter are third-order HP and LP filters. The phase response of each network is determined by the location of its poles and zeros. Thus, the shape of the phase response of the networks can be manipulated to increase phase error bandwidth by appropriately adjusting the relative location of the poles and zeros. For a qualitative examination, the transfer function of the HP network is expressed in (17):

\[
S_{21} = \frac{s^3}{(s + \frac{1}{Z_0C})(s^2 + \frac{Z_0^2}{2L} s + \frac{1}{2LC})}
\]

(17)

The network has a simple pole and a pair of complex poles as follows:

\[
p_1 = \frac{1}{Z_0C}; \quad p_{2,3} = -\frac{Z_0}{4L} \pm \frac{1}{2} \sqrt{\frac{Z_0^2}{4L^2} - \frac{2}{LC}}
\]

(18.a) \quad (18.b)

Capacitance and inductance values can be calculated at the resonant frequency \( f_1 \) given by

\[
L_1 = \frac{Z_0}{\omega_1 \sin(\phi_1)}
\]

(19)

\[
C_1 = \left[ \frac{Z_0 \omega_1 \tan(\phi_1/2)}{4L} \right]^{-1}
\]

(20)

Substituting (19) and (20) into (18.a) and (18.b) leads to

\[
p_1 = \omega_1 \tan(\phi_1/2)
\]

(21.a)

\[
p_{2,3} = \omega_1 \sin(\phi_1/2)
\]

(21.b)
Similar results for the LP network can also be obtained as in (22). Substituting (19) and (20) into (18.a) and (18.b) leads to

$$p_1 = \frac{\omega_2}{\tan(\phi_2/2)}; \quad (22.a)$$

$$|p_{2,3}| = \frac{\omega_2}{\sin(\phi_2/2)} \quad (22.b)$$

As can be seen from (21) – (22), the pole locations are directly proportional to the resonance frequencies of the networks. Thus, when a resonant frequency is shifted, its pole locations move accordingly. If the resonant frequency of the LP network is increased and that of the HP network is decreased, the poles of the LP network will be pushed further apart, and the poles of the HP network will be pulled nearer together on the frequency axis. By doing that, the transition area of the phase responses of the two networks is expanded, resulting in a constant relative phase shift over a broader range of frequency. A phase-shifter with the proposed method is compared with a conventional one, which illustrates a definite bandwidth improvement as shown in Fig. 3.

The phase-shifting cells for 5.625°, 11.25°, and 22.5° are constructed with a combination of L-C-L BP and T-type LP networks designed with the available sizes of inductances and capacitances. The phase-shifting cell of 45° is constructed with a C-L-C BP and a π-type LP network to minimize its area consumption compared with a T-type network configuration. The phase-shifting cell for 90° comprises a T-type HP filter and a π-type LP filter with third-order filter networks, while 180° phase shifting is formed with two 90° cells in series. Figure 4 shows the relative phase shift levels which are very flat over the entire X-band. The RMS phase error is less than 2.3° in 8-12 GHz which is much smaller than that of the conventional design as presented in Fig. 5.

A low loss switching mechanism is required to perform the phase-shifting function with coverage of 360° in steps of 5.625°. The SPDT and DPDT switches configure the path through the phase-shifting elements to produce the desired insertion phase shift. The phase shifter employs two SPDT (single pole double throw) switches and four DPDT (double pole double throw) switches as shown in Fig. 6 [15]. For the SPDT switch, the series transistor (M1) performs the primary switching function. Shunt transistors (M2) are added to improve the isolation between different paths. In the design of the SPDT and DPDT switches, the gate terminals are biased through a large resistor $R_G$ to reduce fluctuations of $V_{GS}$ and $V_{GD}$ due to voltage swings at drain and source. This $R_G$ will keep the on-resistance of the transistors unchanged and avoid excessive voltage across the gate dielectric which causes breakdown issues. The SPDT switch is also used as a duplexer in the proposed transceiver.

B. 6-BIT STEP ATTENUATOR

There are two basic topologies commonly employed in the digital attenuator designs: resistive π-type attenuators, and resistive T-type attenuators. These conventional structures consist of series/shunt switches and resistors. The switches are usually realized as a single NMOS transistor, so NMOS transistors are crucial elements in determining the performance of a digital step attenuator. Explicitly, NMOS switches can be approximately modeled by the resistor $R_{ON}$ in the ON state and the capacitor $C_{OFF}$ in the OFF state.

In this design, a 6-bit CMOS digital attenuator is designed with a resistive π-type structure as depicted in Fig. 7. The attenuator covers the range of 0 to 31.5 dB with steps of 0.5 dB. The relative attenuation level is obtained by taking the
difference between the attenuation state and the thru state as controlled by single NMOS switches. One of the challenges in designing an attenuator is to sustain reasonable impedance matching for both of its states. The large resistor \( R_2 \) at the gate keeps \( V_{GS} \) and \( V_{GD} \) almost the same during its operation, which relieves the impedance changes that depend on the switch states. By using two inverters with large resistors to bias source and drain terminals of the series switch, the contrast of the channel resistance of the series switch (M1) for ON/OFF states can be improved to provide less insertion loss of the attenuator at the thru state than that of the attenuators in [13], [15].

### C. CASCADED DISTRIBUTED AMPLIFIERS

Distributed gain amplifiers (DGA) have been widely used in wideband applications in the microwave regime due to their excellent input and output matching characteristics as well as their wideband frequency response [21], [22]. However, the summing nature of the distributed amplifier cells results in a power gain limitation, which is typically less than 10 dB. A wideband low-noise amplifier (LNA) and bi-directional gain amplifiers (BDGAs) composed of cascading distributed amplifiers with a common source (CS) stage in the middle were used to provide higher power gain as illustrated in Figs. 8 and 9. Furthermore, a transformer was used to reduce area occupancy, minimizing the number of inductors used for the artificial transmission line by combining the parasitic capacitance of the DGA transistors.

The schematic diagram for the BDGA is presented in Fig. 8. The circuit is composed of four-stage bi-directional distributed gain amplifiers (BDGAs) and a cascading connection stage for gain-boosting in the middle. Like the conventional BDGA, on-chip transformers and the parasitic capacitance of transistors form artificial transmission lines at the input and output, enabling the amplifier’s broadband operation. Because of the cascading connection between the BGA stages, the cascaded BDGA takes advantage of multiplicative gains.

The schematic and the device parameters for the LNA are presented in Fig. 9. The LNA consists of gain amplifiers (GAs) and the cascading connection stage for gain-boosting in the middle. It is noteworthy that the center frequency of the LNA is around 12 GHz since the phase shifter has quite a large amount of insertion loss at this frequency. In other words, the LNA is designed to compensate for the loss in the whole transceiver at that frequency.

### D. WIDEBAND POWER AMPLIFIER

The wideband PA was employed after the SPDT duplexer for Tx operation to enhance the output power and provide a proper power gain of the transmitter as shown in Fig. 10. The PA is constructed from two stages of push-pull amplifiers using a cascode configuration combined with two stages of a transformer-based distributed amplifier. The push-pull...
FIGURE 9. Schematic and all device parameters of the transformer-based LNA.

FIGURE 10. Schematic and all device parameter of the full X-band PA.

FIGURE 11. Chip-photograph of the fabricated X-band phased-array transceiver in 65-nm CMOS technology.

FIGURE 12. The measurement setup for the S-parameters, phase shift, attenuation, and output power of the chip in Rx/Tx operation.

III. MEASUREMENT RESULTS

The X-band phased-array TRM chip was fabricated in 65-nm CMOS technology. Figure 11 shows the chip-photograph of the implemented transceiver, which occupies 4 mm \(\times\) 1.88 mm, including all the pads. As shown in Fig. 12, the TRM chip was measured with on-chip probing. A 64-bit serial-peripheral-interface (SPI) scan-chain was integrated for digital control of each block. The equipment used for measurement was as follows: Agilent E4407B spectrum analyzer, Keysight DSO-X 6002A digital oscilloscope, Agilent 83623B signal generator, and Keysight N5224A network analyzer.
TABLE 1. Comparison with previously reported state-of-the-art X-Band Phased-Array Transceivers.

| Ref. | This work | [1] | [2] | [3] | [4] | [5] | [6] | [7] | [8] | [9] | [10] | [11] | [12] | [13] | [14] | [15] | [16] |
|------|-----------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Tech. | 65nm CMOS | 0.2µm pHEMT | 0.25µm pHEMT | 0.25µm SiGe | 0.25µm SiGe | 0.15µm SiGe | 0.15µm SiGe | 0.15µm SiGe | 0.15µm CMOS | 0.15µm CMOS | 0.15µm CMOS | 0.15µm CMOS | 0.15µm CMOS | 0.15µm CMOS |
| f₀ (GHz) | 8-12 | 9-12 | 8.5-11.5 | 8.11 | 8.11 | 6.18 | 8.10-7.9 | 9-11 | 8.12 | 8.16 | 9-12 | 8.5-10.5 | 8.5-10.5 | 7.9-9.6 | 8.10-5.10 |
| Phased- | 6/6 | 7/7 | 6/3 | 5/5 | 5/5 | 4/NA | 5/NA | 5/NA | 6/6 | 7/7 | 6/8 | 5/NA | 6/3 | 6/3 | 6/3 | 6/3 |
| shifter/ | | | | | | | | | | | | | | | | |
| Alternat | | | | | | | | | | | | | | | | |
| # of bits | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Function | Rx/Tx | Rx/Tx | Rx/Tx | Rx/Tx | Rx | Rx | Rx/Tx | Rx/Tx | Rx/Tx | Rx/Tx | Rx/Tx | Rx/Tx | Rx | Rx/Tx | Rx/Tx | Rx/Tx |
| # of channel | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Rx/Tx | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 |
| Gain (dB) | /15 | /15 | /15 | /15 | /15 | /15 | /15 | /15 | /15 | /15 | /15 | /15 | /15 | /15 | /15 | /15 |
| RMS | 15/8.84 | 15/9 | 15/19 | 15/29 | 15/29 | 15/29 | 15/29 | 15/29 | 15/29 | 15/29 | 15/29 | 15/29 | 15/29 | 15/29 | 15/29 | 15/29 |
| phase | 5 | 15 | 8 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| error (deg.) | | | | | | | | | | | | | | | | | |
| RMS | 0.45 | 0.08 | 5.5 | 1.5 | 2 | 0.9 | 0.6 | 1.2 | 0.25 | 0.3 | 0.5 | 0.4 | 0.25 | 0.8 | 0.5 | 0.5 | 0.4 |
| amplitude | 5 | 15 | 8 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 | 6 |
| (dB) | | | | | | | | | | | | | | | | | |
| Chip area [mm²] | 7.52 | 18.48 | 20 | 8.4 | 16 | 5.39 | 13.3 | 15.6 | 9 | 16 | 54 | 7.25 | 12.8 | 12 | 0.7 | 5.6 | 2.8 |
| /[mm²] | /214 | /900 | /2100 | /1500 | /800 | /560 | /350 | /350 | /215 | /290 | /144 | /2070 | /1854 | /1870 | /506 |
| Rx/Tx | 110 | 600 | 1200 | 1500 | 800 | 560 | 350 | 350 | 215 | 290 | 144 | 2070 | 1854 | 1870 | 506 |
| DC power [mW] | 46 | 55 | 66 | 77 | 66 | 77 | 88 | 88 | 77 | 88 | 99 | 88 | 99 | 99 | 99 | 99 |

FIGURE 13. Simulated and measured results for (a) the $S_{11}$, $S_{22}$, and (b) Tx gain of the transceiver in Tx operation depending on 64 different phase-shift states.

In Tx mode, the simulated and measured $S_{11}$ and $S_{22}$ for 64 different phase states are presented in Fig. 13(a). Between 8 and 12 GHz, the input and output return losses are better than 10 dB. Figure 13(b) shows the simulated and measured gain of the Tx for 64 different phase states. The gain flatness is about ±2 dB. As shown in Fig. 14(a), the measured relative phase-shift in the X-band has a resolution of 5.625° and...
attenuation level of the transceiver in the Rx operation is shown in Fig. 19(a). It shows a resolution of 0.5 dB in the X-band. The simulated and measured RMS amplitude error of the transceiver in the Rx operation is illustrated in Fig. 19(b). In full X-band, the measured RMS amplitude error is less than 0.45 dB which is smaller than the resolution. The simulated and measured noise figure (NF) of the transceiver in the Rx operation is presented in Fig. 20. The NF measurement was carried out from the Y-factor method, showing a minimum NF of 8.4 dB in the whole X-band.

Table 1 compares the implemented transceiver with previously published III-V chipsets and SiGe based transceivers for X-band phased-array systems. It shows that the implemented TRM chip shows the highest $OP_{1dB}$, gain, and widest operating frequency range among the CMOS based phased-array chips and has RF performance comparable with SiGe transceivers and III-V chipsets with much lower power consumption.

IV. CONCLUSION

We demonstrated a full X-band transmit/receive module (TRM) chip for phased-array antenna systems in 65-nm CMOS technology. The implemented TRM chip integrates a BDGA, a 6-bit attenuator, a 6-bit passive phase shifter with a resonant frequency misalignment technique to expand the operating frequency range. A wideband PA and LNA were also integrated with an SPDT switch as a duplexer for bi-directional operation of the half-duplex transceiver. The measurement results demonstrated that the performance of the implemented TRM chip achieved the highest $OP_{1dB}$,
gain and widest operating frequency range among recently reported CMOS based phased-array chips. The TRM has RF performance comparable with several recently reported SiGe transceivers and III-V TRM chipsets with a distinct advantage of low-power dissipation.

REFERENCES

[1] A. de Boer and K. Mouthaan, “GaAs mixed signal multi-function X-band MMIC with 7 bit phase and amplitude control and integrated serial to parallel converter,” in Proc. 30th Eur. Microw. Conf., Oct. 2000, pp. 1–4.

[2] M. van Heijningen, A. de Boer, J. A. Hoogland, M. van Wanum, A. P. de Heik, F. E. van Vliet, and H. Brounus, “Multi function and high power amplifier chipset for X-band phased array frontends,” in Proc. Eur. Microw. Integr. Circuits Conf., Sep. 2006, pp. 237–240.

[3] J. C. Jeong and J. B. Yom, “X-band high power SiGe BiCMOS multi-function chip for active phased array radars,” Electron. Lett., vol. 47, no. 10, pp. 618–619, Dec. 2011.

[4] D. Carosi, A. Bettidi, A. Nanni, L. Marescialli, and A. Cetronio, “A mixed-signal X-band SiGe multi-function control MMIC for phased array radar applications,” in Proc. 39th Eur. Microw. Conf., Oct. 2009, pp. 240–243.

[5] K.-J. Koh and G. M. Rebeiz, “An X-and Ku-band 8-element phased-array receiver in 0.18-µm SiGe BiCMOS technology,” IEEE J. Solid-State Circuits, vol. 43, no. 6, pp. 1360–1371, Jun. 2008.

[6] J. P. Comeau, M. A. Morton, W.-M. Lance Kuo, T. Thrivikraman, J. M. Andrews, C. M. Grens, J. D. Cressler, J. Papapolymerou, and M. Mitchell, “A silicon-germanium receiver for X-band transmit/receive radar modules,” IEEE J. Solid-State Circuits, vol. 43, no. 9, pp. 1889–1896, Sep. 2008.

[7] C. Liu, Q. Li, Y. Li, X.-D. Deng, X. Li, H. Liu, and Y.-Z. Xiong, “A fully integrated X-band phased-array transceiver in 0.13-µm SiGe BiCMOS technology,” IEEE Trans. Microw. Theory Techn., vol. 64, no. 2, pp. 575–584, Feb. 2016.

[8] P. Lohmiller, R. Reber, P. Schuh, M. Oppermann, and S. Chartier, “SiGe BiCMOS X-band transceiver chip for phased-array systems,” in Proc. 47th Eur. Microw. Conf. (EuMC), Oct. 2017, pp. 1253–1256.

[9] P. Saha, S. Muralidharan, J. Cao, O. Gurbuz, and C. Hay, “X/Ku-band four-channel Transmit/Receive SiGe phased-array IC,” in Proc. IEEE Radio Freq. Integ. Circuits Symp. (RFIC), Jun. 2019, pp. 51–54.

[10] Z. Hao and W. Chuanchuan, “A 8–12 GHz 4-element SiGe BiCMOS multi-function chip for phased array systems,” in Proc. IEEE 4th Int. Conf. Integ. Circuits Microsyst. (ICICM), Oct. 2019, pp. 95–99.

[11] D. Shin and G. M. Rebeiz, “A high-linearity X-band four-element phased-array receiver: CMOS chip and packaging,” IEEE Trans. Microw. Theory Techn., vol. 59, no. 8, pp. 2064–2072, Aug. 2011.

[12] K. Gharibdoust, N. Mousavi, M. Kalantari, M. Mocezzi, and A. Medi, “A fully integrated 0.18-µm CMOS phased-array transceiver for X-band phased-array systems,” IEEE Trans. Microw. Theory Techn., vol. 60, no. 7, pp. 2192–2202, Jul. 2012.

[13] S. Sim, L. Jeon, and J.-G. Kim, “A compact X-Band bi-directional phased-array T/R chipset in 0.13 µm CMOS technology,” IEEE Trans. Microw. Theory Techn., vol. 61, no. 1, pp. 562–569, Jan. 2013.

[14] D. Shin, C.-Y. Kim, D.-W. Kang, and G. M. Rebeiz, “A high-power packaged four-element X-band phased-array transmitter in 0.13-µm CMOS for radar and communication systems,” IEEE Trans. Microw. Theory Techn., vol. 61, no. 8, pp. 3060–3071, Aug. 2013.

[15] V. N. Nguyen, H. Nam, Y. Choe, B.-H. Lee, and J.-D. Park, “An X-band bi-directional Transmit/Receive module for a phased array system in 65-nm CMOS,” Sensors, vol. 18, no. 8, p. 2569, 2018.

[16] S. Sim, B. Kang, J.-G. Kim, J.-H. Chun, B. Jang, and L. Jeon, “A four-channel bi-directional CMOS core chip for X-band phased array T/R modules,” in Proc. IEEE Radar Conf. (RadarCon), May 2015, pp. 1198–1201.

[17] K.-J. Koh and G. M. Rebeiz, “0.13-µm CMOS phase shifters for X-, Ku-, and K-band phased arrays,” IEEE J. Solid-State Circuits, vol. 42, no. 11, pp. 2535–2546, Nov. 2007.

[18] M. A. Morton, J. P. Comeau, J. D. Cressler, M. Mitchell, and J. Papapolymerou, “Sources of phase error and design considerations for silicon-based monolithic high-pass/low-pass microwave phase shifters,” IEEE Trans. Microw. Theory Techn., vol. 54, no. 12, pp. 4032–4040, Dec. 2006.

[19] B.-W. Min and G. M. Rebeiz, “Single-ended and differential ka-band BiCMOS phased array front-ends,” IEEE J. Solid-State Circuits, vol. 43, no. 10, pp. 2239–2250, Oct. 2008.
JEONG-MOON SONG (Student Member, IEEE) received the B.S. degree in electrical and electronics engineering from Dongguk University, Seoul, South Korea, in 2019, where he is currently pursuing the M.S. degree in electrical and electronics engineering.

His research interest includes phase shifter designs for phased-array systems.

BOK-HYUNG LEE received the B.S., M.S., and Ph.D. degrees in electronics engineering from Dongguk University, Seoul, South Korea, in 1999, 2001, 2006, respectively.

He is currently a Principal Research Engineer with Hanwha Systems. His research interests include various microwave/millimeter-wave components for active phased-array systems.

JUNG-DONG PARK (Senior Member, IEEE) received the B.Sc. degree from Dongguk University, Seoul, South Korea, in 1998, the M.S. degree from the Gwangju Institute of Science and Technology (GIST), Gwangju, South Korea, in 2000, and the Ph.D. degree in EECS from the University of California at Berkeley, Berkeley, CA, USA, in 2012.

From 2000 to 2002, he worked at the Institute for Advanced Engineering (IAE), Yongin, South Korea, where he was involved with the design of 35 GHz radar/radiometer transceivers. From 2002 to 2007, he was a Senior Researcher with the Agency for Defense Development (ADD), Daejeon, South Korea, where he was responsible for the development of millimeter-wave (mmW) passive/active sensors and related mmW modules. From 2007 to 2012, he was with the Berkeley Wireless Research Center (BWRC), where he worked on silicon-based RF/millimeter-wave/terahertz circuits and systems. From 2012 to 2015, he worked with Qualcomm Inc., San Jose, CA, USA, where he designed various RF/analog integrated circuits. He is currently an Associate Professor with the Division of Electronics and Electrical Engineering, Dongguk University. His research interests include wireless communications, remote sensors, microwave electronics, analog, RF, mixed-signal, and millimeter-wave circuits.

Dr. Park was a recipient of the 2017 Most Frequently Cited Papers Award as a Lead Author from 2010 to 2016 at the 2017 IEEE Symposium on VLSI Circuits, Kyoto.

* * *