An Operational Framework for Specifying Memory Models using Instantaneous Instruction Execution

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Abstract
There has been great progress recently in formally specifying the memory model of microprocessors like ARM and POWER. These specifications are, however, too complicated for reasoning about program behaviors, verifying compilers etc., because they involve microarchitectural details like the reorder buffer (ROB), partial and speculative execution, instruction replay on speculation failure, etc. In this paper we present a new Instantaneous Instruction Execution (I\(\text{E}\)) framework which allows us to specify weak memory models in the same style as SC and TSO. Each instruction in I\(\text{E}\) is executed instantaneously and in-order such that the state of the processor is always correct. The effect of instruction reordering is captured by the way data is moved between the processors and the memory non-deterministically, using three conceptual devices: invalidation buffers, timestamps and dynamic store buffers. We prove that I\(\text{E}\) models capture the behaviors of modern microarchitectures and cache-coherent memory systems accurately, thus eliminating the need to think about microarchitectural details.

Categories and Subject Descriptors C.0 [General]: Modeling of computer architecture

Keywords Weak memory models, Operational semantics

1. Introduction
Computer architects make microarchitectural optimizations in processors which ensure that single-threaded programs can be run unmodified, but often create new and unexpected behaviors for multi-threaded programs. The effect of these optimizations manifests itself through load and store instructions because these are the only instructions through which threads can communicate with each other. Memory models abstract hardware in a way that is useful for programmers to understand the behaviors of their programs.

There are ongoing efforts to specify memory models for multi-threaded programming in C, C++ [57] and other languages. These efforts are influenced by the type of memory models that can be supported efficiently on existing architectures like x86, POWER and ARM. While the memory model for x86 [46, 51, 54] is captured succinctly by the Total Store Order (TSO) model, the models for POWER [52] and ARM [25] are considerably more complex. The formal specifications of the POWER and ARM models have required exposing microarchitectural details like speculative execution, instruction reordering and the state of partially executed instructions, which, in the past, have always been hidden from the user. In addition, details of the memory system like write-through vs write-back caches, shared vs not-shared memory buffers, etc., were also needed for a precise specification of these two models.

Even though empirical evidence is weak, many architects believe that weak memory models, such as the ones for ARM, POWER, Alpha and RMO, offer some performance advantage or simpler implementation over TSO and other stronger memory models. We think that architects are unlikely to give up on weak memory models because of the flexibility they provide for high-performance implementations. It is, therefore, important to develop a framework for defining weak memory models, which, like SC and TSO operational models, does not involve microarchitecture and memory system details. This paper offers such a framework based on Instantaneous Instruction Execution (I\(\text{E}\)).

In the I\(\text{E}\) framework, instructions are executed in order and atomically, and consequently, the processor always has the up-to-date state. The model descriptions use a multi-ported monolithic memory which executes loads and stores instantaneously. The data movement between the processors and the memory takes place asynchronously in the background. For specifying weak memory models, we combine I\(\text{E}\) with three new conceptual devices: invalidation buffers to capture instruction reordering, timestamps to enforce data dependencies, and dynamic store buffers to model shared store buffers and write-through caches in a topology independent way. We present several different weak memory models – WMM and WMM-D which are similar to the Alpha and RMO models; and WMM-S which is similar to the ARM and POWER models.

To convince the reader that we have not ruled out any fundamental and important microarchitectural optimizations, we give an abstract description of a speculative microarchitecture (OOO\(\text{VP}\)) with a coherent pipelined memory system (CCM). The structure of OOO\(\text{VP}\) is common to all high-performance processor implementations, regardless of the memory model they support; implementations of stronger memory models based on OOO\(\text{VP}\) use extra hardware checks to prevent or kill some specific memory behaviors. We prove that our weakest memory model, WMM, allows all sorts of microarchitecture optimizations, that is, CCM+OOO\(\text{VP}\)⊆ WMM.

One optimization that has been discussed in literature but has not been implemented in any commercial microprocessor yet is load-value speculation [29, 49, 57, 48]. It allows us to predict a value for a load; the load is killed later if the predicted value does not match the load result from the memory system. Even if load-value speculation is included, our result CCM+OOO\(\text{VP}\)⊆ WMM holds. Surprisingly, if value speculation is permitted in the implementation then we can also prove that WMM ⊆ CCM+OOO\(\text{VP}\), that is, the WMM and CCM+OOO\(\text{VP}\) become equivalent. We show via a common programming example that an extra fence needs to be inserted in WMM to enforce data-dependencies. This is an unnecessary cost if we know for sure that our implementation would not use value speculation. WMM-D is a slight modification of WMM to enforce ordering of data-dependent loads using timestamps. We also prove that OOO\(\text{VP}\) (the OOO\(\text{VP}\) implementation without load-value speculation) is equivalent to WMM-D.

ARM and POWER microarchitectures use shared store-buffers and write-through caches, and unfortunately, such memory systems introduce behaviors not seen in other weak memory mod-

arXiv:1705.06158v1 [cs.PL] 16 May 2017
els. The ISA for these machines include "weaker" and "stronger" fences with slightly different functionality because weaker fences have smaller performance penalty than the stronger ones. This requires memory fence instructions to enter store buffers, muddying the clean separation between the cache-coherent memory systems and processors. We introduce HMB, an abstract model for hierarchy of shared store buffers or write-through caches, which is adapted from the storage subsystem in the Flowing Model of [25]. We define WMM-S, an extension of WMM, specifically to deal with such multi-copy non-atomic store systems and show that HMB+OOO \( \subseteq \) WMM-S, in which OOO\( ^P \) is the processor implementation adapted from OOO\( ^P \) to be compatible with HMB.

In summary, this paper makes the following contributions:

1. \( i^2E \), a new framework for describing memory models with three new conceptual devices: invalidation buffers, timestamps, and dynamic store buffers;
2. WMM and WMM-D memory models which are like the RMO and Alpha models;
3. WMM-S model to embody ARM and POWER like multi-copy non-atomic stores;
4. OOO\( ^P \), an abstract description of the microarchitecture underlying all modern high performance microprocessors;
5. A proof that CCM+OOO\( ^P \) = WMM-D; and
6. A proof that HMB+OOO\( ^P \) \subseteq \) WMM-S.

Paper organization: Section 2 presents the related work. Section 3 defines CCM+OOO\( ^P \), an implementation scheme of multiprocessors. We introduce the \( i^2E \) framework in Section 4. We use \( i^2E \) and invalidation buffers to define WMM in Section 5. Section 6 defines WMM-D using timestamps to capture data dependency. Section 7 defines WMM-S using dynamic store buffers to model multi-copy non-atomic memory systems. Section 8 offers the conclusion.

2. Related Work
SC [33] is the most intuitive memory model, but naive implementations of SC suffer from poor performance. Gharachorloo et al. proposed load speculation and store prefetch to enhance the performance of SC [25]. Over the years, researchers have proposed more aggressive techniques to preserve SC [10, 21, 22, 31, 32, 36, 39, 56, 52]. Perhaps because of their hardware complexity, the adoption of these techniques in commercial microprocessor has been limited. Instead the manufacturers and researchers have chosen to present weaker memory model interfaces, e.g. TSO [53], PSO [61], RMO [61], x86 [46, 51, 54], Processor Consistency [30], Weak Consistency [24], RC [27], CRF [55], POWER [33] and ARM [9]. The tutorials by Adve et al. [1] and by Manaret et al. [44] provide relationships among some of these models.

The lack of clarity in the definitions of POWER and ARM memory models in their respective company documents has led some researchers to empirically determine allowed/disallowed behaviors [8, 25, 41, 52]. Based on such observations, in the last several years, both axiomatic models and operational models have been developed which are compatible with each other [8, 5, 7, 8, 25, 41, 52, 53]. However, these models are quite complicated; for example, the POWER axiomatic model has 10 relations, 4 types of events per instruction, and 13 complex axioms [41], some of which have been added over time to explain specific behaviors [42, 43]. The abstract machines used to describe POWER and ARM operationally are also quite complicated, because they require the user to think in terms of partially executed instructions [52, 53]. In particular, the processor sub-model incorporates ROB operations, speculations, instruction replay on speculation failures, etc., explicitly, which are needed to explain the enforcement of specific dependency (i.e., data dependency). We present an \( i^2E \) model WMM-D in Section 6 that captures data dependency and sidesteps all these complications.

Another source of complexity is the multi-copy non-atomicity of stores, which we discuss in Section 7 with our solution WMM-S.

Adve et al. defined Data-Race-Free-0 (DRF0), a class of programs where shared variables are protected by locks, and proposed that DRF0 programs should behave as SC [2]. Marino et al. improves DRF0 to the DRFx model, which throws an exception when a data race is detected at runtime [45]. However, we believe that architectural memory models must define clear behaviors for all programs, and even throwing exceptions is not satisfactory enough.

A large amount of research has also been devoted to specifying the memory models of high-level languages, e.g. C/C++ [12, 15, 17, 34, 35, 47, 49, 57] and Java [18, 20, 23, 42, 43]. There are also proposals not tied to any specific language [19, 22]. This remains an active area of research because a widely accepted memory model for high-level parallel programming is yet to emerge, while this paper focuses on the memory models of underlying hardware.

Arvind and Maessen have specified precise conditions for preserving store atomicity even when instructions can be reordered [10]. In contrast, the models presented in this paper do not insist on store atomicity at the program level.

There are also studies on verifying programs running under weak memory models [11, 30, 39]. Simple memory model definitions like \( i^2E \) models will definitely facilitate this research area.

3. Implementation of Modern Multiprocessors
Modern multiprocessor systems consist of out-of-order processors and highly pipelined coherent cache hierarchies. In addition to pipelining and out-of-order execution, the processor may perform branch prediction, i.e. predict the PC of the next instruction during instruction fetch in order to fetch and execute the next instruction, memory dependency speculation, i.e. issue a load to memory even when there is an older store with unresolved address, and even load-value speculation, i.e. predict the result of a load before the load is executed. The memory systems also employ pipelining and out-of-order execution for performance. For example, the memory system may not process requests in the FIFO manner (consider a cache miss followed by a cache hit). These optimizations are never visible to a single-threaded program but can be exposed by multi-threaded programs. In this section, we present "physical" models that describe the operations (e.g. the ones mentioned above) inside high-performance processors and cache hierarchies. These physical models are similar to those in [25, 52], but here they only serve as a reference to capture the behaviors of modern multiprocessors precisely; we use them to verify the \( i^2E \) memory models proposed later. It should be noted that the physical models are presented in an abstract manner, e.g., the inner structure of the branch predictor is abstracted by a function which may return any value. The model also abstracts away resource management issues, such as register renaming, finite-size buffers and associated tags by assuming unbounded resources.

We associate a globally unique tag with each store instruction so that we can identify the store that each load reads from. The tag is also saved in memory when the store writes the memory. Such tags do not exist in real implementations but are needed in our model for reasons that will become clear in Section 5.

While the processor remains similar for all implementations, it is difficult to offer a common model for two dominant cache hierarchies. Machines, such as Intel x86, have used write-back cache-coherent memory systems. In contrast, ARM and POWER machines employ shared store-buffers and write-through caches in their memory systems. We will first discuss CCM, model of a write-back cache-coherent memory system, and postpone the discussion of HMB, the write-through cache system, until Section 7.
3.1 CCM: the Semantics of Write-Back Cache Hierarchies

Figure 1 shows how out-of-order processors (OOO\textsuperscript{VP}) and a write-back cache hierarchy (CCM) are connected together. A processor \(i\) can send load and store requests to CCM by calling the following methods of port \(i\) of CCM:

- reqLd\((t^L, a)\): a load request to address \(a\) with tag \(t^L\).
- reqSt\((a, v, t^S)\): a store request that writes data \(v\) to address \(a\) with tag \(t^S\).

Note that the processor also attaches a tag \(t^L\) to each load request in order to associate the future load response with the requesting load instruction. The memory sends responses back to a processor by calling the following methods of the processor:

- respLd\((t^L, res, t^S)\): \(res\) is the result for the load with tag \(t^L\), and \(t^S\) is the tag for the store that supplied \(res\) to the memory.
- respSt\((a)\): \(a\) is the store address.

Store response is needed to inform the processor that a store has been completed. No ordering between the processing of requests inside the memory should be assumed by the processor.

![Figure 1. Multiprocessor system](image)

CCM consists of \(n\) memory request buffers \(mrb[1] \ldots n\), one for each processor, and a monolithic memory \(m\). A monolithic memory location \(m[a]\) contains \((v, t^S)\), in which \(v\) is the value written by a store with tag \(t^S\). The reqLd and reqSt methods simply insert the incoming requests from processor \(i\) into \(mrb[i]\). CCM processes requests by picking any request from any \(mrb\). If the request is a load \((Ld, t^L, a)\) from \(mrb[i]\), then CCM calls method \(\text{respLd}(t^L, v, t^S)\) of processor \(i\), where \((v, t^S) = m[a]\). If the request is a store \((St, a, v, t^S)\), then we update \(m[a]\) to \((v, t^S)\), and call method \(\text{respSt}(a)\) of processor \(i\). The behavior of CCM is shown in Figure 2.

![Figure 2. CCM operational semantics](image)

We describe the behavior of a system as a set of state-transition rules, written as

\[
\text{predicates on the current state} \quad \text{the action on the current state}
\]

The predicates are expressed either by pattern matching or using a when\((\text{expression})\) clause. \(mrb[i]\).any() returns any entry in \(mrb[i]\), and \(mrb[i]\).remove\((en)\) removes entry \(en\) from \(mrb[i]\).

To understand how such a simple structure can abstract the write-back cache-coherent hierarchy, we refer to the cache coherence proof by Vijayaraghavan et al. [60]. It shows that a request can complete only by reading or writing an L1 cache line when it has sufficient permissions, and that under such circumstances a write-back cache-coherent hierarchy is exactly equivalent to the monolithic memory abstraction. However, the order of responses may be different from the order of requests due to the out-of-order processing inside the hierarchy. Such reordering is captured by \(mrb\).

3.2 OOO\textsuperscript{VP}: the Model of Out-of-Order Processors

We will first give an informal description of the behavior of a speculative out-of-order processor OOO\textsuperscript{VP}, shown in Figure 3, the actual rules are presented later.

The processor fetches an instruction from the address given by the PC register, and updates PC based on the prediction by a branch predictor. The fetched instruction is decoded and enqueued into the reorder buffer (ROB). ROB contains all the in-flight instructions in the fetched order but executes them out of order. An instruction can be executed when all of its source operands have been computed, and the result of its execution is stored in its ROB entry. The computed source operands come from either an older ROB entry or the register file. The ROB then commits the instructions in the fetched order. In-order commitment is required to implement precise interrupts and exceptions. After an instruction is committed, it is removed from the ROB and the register file is updated with the result of the instruction’s execution.

When a branch instruction is executed, if the branch target is not equal to the address of the next instruction that was fetched, then all instructions in ROB after the branch are “flushed” (i.e. discarded) and the PC is set to the correct branch target, allowing the correct set of instructions to be fetched.

A store instruction is executed by computing the store address and data, and is enqueued into the store buffer at commit. In the background, the store buffer can send the oldest store for an address into the memory, and delete that store when the response comes back from the memory.

In contrast, the execution of a load instruction splits into two phases. The first phase is to compute the load address. In the second phase, a load will search older entries in the ROB and the store buffer for the latest store to the same address. If such a store is found, that store’s value (and tag) is read – this is called “data forwarding” or “data bypassing”. Otherwise, a load request is sent to the memory with a unique tag (we use the index of the ROB entry). Eventually, the memory system can send a response back to the processor with a load result; the ROB entry for the load (identified with the tag) is updated with the result.

A load can be issued to memory at any time as long as its address is available, even when there are older unresolved branches or stores with uncomputed addresses. If an older store is executed later and writes to the same address, then any such loads that were executed earlier have violated memory dependency and should be flushed. The details will be discussed later. Note that loads which have been issued to the memory can be flushed from ROB for various reasons, and the responses for the flushed loads are discarded.

The processor may also employ a load-value predictor, which predicts the result of any load that does not have a value. The predicted result can be used in the execution of other instructions. When the load gets its value from data forwarding or memory and the value is not equal to the predicted one, all instructions younger than the load are flushed.

There are two fences: Commit and Reconcile. The Commit fence stalls at the commit slot until the store buffer is empty. The Reconcile fence prevents a younger load from being issued to memory, and also stops the data forwarding across the fence.

In the following we give a precise description of how OOO\textsuperscript{VP} operates. (We will directly use the variable names in Figure 3, e.g., \(per\) stands for the PC register.) We never reuse ROB entries, and
follow the convention that younger entries will have larger indices. We refer to the oldest entry in ROB as the commit slot.

### 3.2.1 Component Functionality

Since the implementation has to deal with partially executed instructions, we need to keep information about in-flight instructions in ROB (all srcs fields represent source register names):

- (Nm, op, srcs, dst, val): A non-memory instruction (e.g. ALU and branch instructions). op is the type of operation, val represents the computed value for the destination register dst and is initially ϵ. These instructions include branch instructions.
- (Ld, srcs, dst, a, v, t): A load instruction to address a. v is the load result for destination register dst, and t is the tag of the store that provides value v. All of a, v and t are initially ϵ.
- (St, srcs, a, v, t): A store instruction that writes data v to address a. t is the unique tag for this store assigned at decode time. Both a and v are initially ϵ.
- (Commit) and (Reconcile) fences.

We use the fetch(pc) function to fetch an instruction from memory address pc and decode it into the above form.

per is updated speculatively when a new instruction ins is fetched into ROB using the predict(ins) method of bp. We assume that bp always predicts correctly for non-Nm instructions. rf is updated conservatively when an instruction ins is committed from ROB using the update(ins) method. Each sb entry also contains an iss bit, which indicates whether the store has been issued to the memory or not. The following methods are defined on sb:

- enq(a, v, t): enqueues the (address, value, tag) tuple (a, v, t) into sb, and initializes the iss bit of the new entry as False.
- empty(): returns True when sb is empty.
- anyAddr(): returns any store address present in sb; or returns ϵ if sb is empty.
- oldest(a): return the (store data, tag, iss bit) of the oldest store for address a in sb.
- issue(a): sets the iss bit of the oldest store for address a to True.
- rmOldest(a): deletes the oldest store to address a from sb.

An ROB entry is defined as (pc, npe, ins, ex), where pc is the PC of the instruction in the entry, npe is the (predicted) PC of the next instruction, ins is the instruction in this entry, and ex is the state of the instruction. ex has one of the following values: Idle, Ex, ReEx, and Done. An instruction is Idle before it starts execution, and will become Done after execution finishes. Both Exe and ReEx are only used for Ld instructions to indicate that the load request is being processed in CCM. ReEx additionally implies that the load needs to be re-executed because the result of the current load request in memory is going to be wrong. We initialize the ex field of an instruction ins using function initEx(ins), which returns Done for fence instructions and returns Idle otherwise.

If is for filtering out load responses from CCM for the killed instructions. It is a bit vector of the same length as rob (so it is also infinitely long in our description). If[idx] is True if and only if a Ld instruction at idx has been flushed from rob while its load request is still being processed in the memory.

Load-value speculation is modeled by the predict(en) method of vp, which can predict the load result for ROB entry en.

All methods defined for rob are listed in Table 1. Besides, we use rob[idx] to refer to the ROB entry at index idx. We also use rob[idx].pc, rob[idx].npc, rob[idx].ins and rob[idx].ex to refer to the pc, npe, ins and ex fields of rob[idx], respectively.

| Method | Description |
|--------|-------------|
| enq(en) | enqueues a new entry en into rob. |
| getReady(): | finds an entry for which all source register values are ready, and returns the (index, entry) pair of it. |
| getLd(): | finds any entry containing a Ld instruction, and returns the (index, entry) pair of it. |
| getCommit(): | returns the commit slot of rob. |
| computeNrm(idx): | computes the result of the Nrm instruction at idx using values in rf and rob, and returns (next PC, computed val field). |
| computeAddr(idx): | computes and returns the address of the memory instruction at idx using values in rf and rob. |
| computeStdData(idx): | computes and returns the store data of the St instruction at idx using values in rf and rob. |
| findBypass(idx, a): | if the value for Ld a at idx by searching older entries in the rob and then in sb, and returns a (value, tag) pair if it finds an executed store to address a. If the search finds nothing, then a ⊤ is returned so that the load can be issued to memory. The search is also terminated if a Reconcile fence is encountered and in that case ϵ is returned to indicate that the load should be stalled. |
| findAffectedLd(idx, a): | this method is called when a store at idx resolves its address to a. It identifies Ld a instructions in rob affected by this store by searching for Ld a instructions from idx + 1 to the youngest entry. The search stops if another St a is encountered. Since there can be several affected loads, it lists a pair of their indices. If a load has not started execution yet (i.e. ex field is Idle), it will not be affected by St a and thus will not be returned. |
| findStaleLd(idx, a, t): | this method is called when a Ld a at idx reads from a store with tag t in memory. It identifies Ld a instructions in rob which are younger than the load at idx but read values staler than the value of store t. The method searches from idx + 1 to the youngest entry for the first executed Ld a instruction (i.e. ex field is Done), which reads from a store with tag t’ ≠ t, and returns the index of that instruction in rob. The method returns ⊤ if no such load is found or a St a is encountered first. |

Table 1. Methods for rob

### 3.2.2 Rules to Describe OOOVP Behavior

Figure 4 shows the rules of OOOVP, where ccm represents the CCM port connected to the processor, and Figure 5 shows the interface methods of OOOVP to process the responses from memory.

Rule OOO-LdReq sends a load request to CCM. However, if has to be checked to avoid sending a request with a duplicated idx to memory. (Since we never reuse rob indices here, this check will always pass). When the load response arrives as shows in the respLd(idx, res) method in Figure 5, we check if to see if it corresponds to a Ld instruction which has already been killed. If so, we throw away the response and reset the If bit. Otherwise, we check the ex field of the original requesting ROB entry. If it is ReEx, the load response is discarded and the ex field is set to Idle so that the load can be re-executed later. Otherwise, we record the load result and flush rob in case of load-value misprediction. If there is no load-value misprediction, we kill eagerly executed younger loads which get results staler than the current load response using the findStaleLd method.

There are two points worth noticing about loads. First, the load address can be computed from some unverified predicted values, so two loads can be executed out-of-order even if one load uses
the result of the other as load address. Second, two loads to the same address on the same processor can return from \( \text{CM} \) out-of-order as long as they read from the same store, making the loads still appear to be executed in order. While this mechanism assumes that the load result has the unique tag associated with the store read by the load, in a real implementation there are no unique tags for stores. In actual implementations, the processors monitor the coherence messages during the period between these two load responses: if the cache-line read by the younger load is invalidated, then the younger load is killed. This mechanism helps maintain the SC for a single address property at the program level while imposing minimum restrictions on the out-of-order execution in hardware. POWER and ARM processors also employ this mechanism [25, 52]. (Notice that the tags for stores are solely for the purpose of detecting whether two loads read from the same store). We do not use \( \text{findStaleLd} \) to kill loads in \( \text{OOO-LdBypass} \), because such loads must have already been killed by the store that forwards the data, as explained below in the \( \text{OOO-StEx} \) rule.

Rule \( \text{OOO-StEx} \) computes the store address and data of a \( \text{St} \) instruction, and searches for younger loads to the same address which violate memory dependency. The \( \text{for} \) loop is used to process all violating loads from the oldest to the youngest. If the load has not finished execution, we mark its \( \text{ex} \) field for re-execution. Otherwise, the load may have propagated the wrong result to younger instructions, so we kill it and flush the subsequent instructions from \( \text{rob} \).

Figure 5. \( \text{OOO}^{\text{VP}} \) interface methods

4. Defining Memory Models Using \( \text{I}^2 \text{E} \)

The \( \text{I}^2 \text{E} \) framework defines memory models using the structure in Figure 6a. The state of the system with \( n \) processors is defined as \( (\text{ps}, m) \), where \( m \) is an \( n \)-ported monolithic memory which is connected to the \( n \) processors. \( \text{ps}[i] \) represents the state of the \( i \)th processor. Each processor contains a register state \( s \), which represents all architectural registers, including both the general purpose registers and special purpose registers, such as PC. Cloud represents additional state elements, e.g., a \text{store buffer}, that a specific memory model may use in its definition.

Since we want our definitions of the memory models to be independent from ISA, we introduce the concept of \textit{decoded instruction set} (DIS). A \textit{decoded instruction} contains all the information of an instruction after it has been decoded and has read all source registers. Our DIS has the following five instructions:

- \( \text{Nnm, dst, v} \): instructions that do not access memory, such as ALU or branch instructions. It writes the computation result \( v \) into destination register \( \text{dst} \).
- \( \text{Ld, a, dst} \): a load that reads memory address \( a \) and updates the destination register \( \text{dst} \).
- \( \text{St, v, t} \): a store that writes value \( v \) to memory address \( a \).
- \( \text{Commit} \) and \( \text{Reconcile} \): the two types of fences.

Figure 4. \( \text{OOO}^{\text{VP}} \) operational semantics

The Commit and Reconcile fences already appeared in \( \text{OOO}^{\text{VP}} \), and later we will define their semantics in proposed \( \text{I}^2 \text{E} \) models.

Since instructions are executed instantaneously and in-order in \( \text{I}^2 \text{E} \) models, the register state of each processor is by definition always up-to-date. Therefore we can define the following two methods on each processor to manipulate the register state \( s \):

- \( \text{decode}() \): fetches the next instruction and returns the corresponding decoded instruction based on the current \( s \).
- \( \text{execute}() \): updates \( s \) (e.g. by writing destination registers and changing PC) according to the current decoded instruction \( \text{dIns} \). A \( \text{Ld} \) requires a second argument \( \text{ldRes} \) which
should be the loaded value. For other instructions, the second argument can be set to don’t care (“<”).

In 
\(I^2E\), the meaning of an instruction cannot depend on a future store, so all \(I^2E\) models forbid stores from overtaking loads. This automatically excludes all thin-air read behaviors, and matches the in-order commit property of OOO\(^\text{19}\).

5. WMM Model

Our first \(I^2E\) model, WMM (Figure 6b), adds two conceptual devices to each processor: a store buffer \(ib\) and an invalidation buffer \(sb\). Despite the simplicity of these two devices, they make WMM equivalent to CCM+OOO\(^\text{19}\). It is notable that WMM can capture the subtle effects induced by various speculations in OOO\(^\text{19}\).

The \(sb\) in WMM is almost the same as the one in OOO\(^\text{19}\) except that it does not need the issue method here and thus the \(ss\) bit is also not needed. (The store tag is also not needed here). We change the \(rm\) method of \(sb\) to return the (address, value) pair of the oldest store for address \(a\) in addition to the deletion of that store. We also define the following two new methods on \(sb\):
- \(\text{exist}(a)\): returns True if address \(a\) is present in \(sb\).
- \(\text{youngest}(a)\): returns the youngest store data to address \(a\) in \(sb\).

Buffering stores in \(sb\) allows loads to overtake stores, and enables reorderings of stores. A Commit fence will flush all stores in the local \(sb\) into the monolithic memory to make them globally visible.

In case of load-load reordering, a reordered load may read a stale value, and this behavior is simulated by the \(ib\) of each processor in WMM. \(ib\) is an unbounded buffer of \((\text{address}, \text{value})\) pairs, each representing a stale memory value for an address that can be observed by the processor. A value enters \(ib\) when some store buffer pushes a value to the monolithic memory. When ordering is needed, stale values should be removed from \(ib\) to prevent younger loads from reading them. In particular, the Reconcile fence will clear the local \(ib\). The following methods are defined on \(ib\):
- \(\text{insert}(a, v)\): inserts \((\text{address}, \text{value})\) pair \((a, v)\) into \(ib\).
- \(\text{exist}(a)\): returns True if address \(a\) is present in \(ib\).
- \(\text{getAny}(a)\): returns any value \(v\) for address \(a\) in \(ib\), and removes all values for \(a\), which are inserted into \(ib\) before \(v\), from \(ib\).
- \(\text{clear}(a)\): removes all contents from \(ib\) to make it empty.
- \(\text{rmAddr}(a)\): removes all (state) values for address \(a\) from \(ib\).

5.1 Operational Semantics of WMM

Figure 7 shows the operational semantics of WMM. The first 7 rules are the instantaneous execution of decoded instructions, while the WMM-DqSb rule removes the oldest store for any address (say \(a\)) from \(sb\) and commits it to the monolithic memory. WMM-DqSb also inserts the original memory value into the \(ib\) of all other processors to allow \(Ld\) a in these processors to effectively get reordered with older instructions. However, this insertion in \(ib\) should not be done if the corresponding \(sb\) on that processor already has a store to \(a\). This restriction is important, because if a processor has address \(a\) in its \(sb\), then it can never see stale values for \(a\). For the same reason, when a \(St\ a v\) is inserted into \(sb\), we remove all values for \(a\) from the \(ib\) of the same processor.

\begin{table}
\begin{tabular}{|c|c|}
\hline
\textbf{WMM-Nm rule (Nm execution).} & \(\begin{aligned}
\{\text{Nm, dest, } v\} &= \text{ps}[i].\text{decode}(); \\
\text{ps}[i].\text{execute}(\{\text{Nm, dest, } v\})
\end{aligned}\\
\text{WMM-LdSb rule (Ld execution: bypass from store).} & \(\begin{aligned}
\{\text{Ld, a, } \text{dest}\} &= \text{ps}[i].\text{decode}(); \text{if } (\text{ps}[i].\text{sb}.\text{exist}(a)) \{
\text{ps}[i].\text{execute}(\{\text{Ld, a, } \text{dest}\}), \text{ps}[i].\text{ib}.\text{rmAddr}(a);
\}\text{else }
\{\text{Ld, a, } \text{dest}\} & \text{exists in } \text{ps}[i].\text{sb}.
\end{aligned}\\
\text{WMM-LdMem rule (Ld execution: read memory).} & \(\begin{aligned}
\{\text{Ld, a, } \text{dest}\} &= \text{ps}[i].\text{decode}(); \text{if } (\text{ps}[i].\text{sb}.\text{exist}(a)) \{
\text{ps}[i].\text{execute}(\{\text{Ld, a, } \text{dest}\}), \text{m}[a]; \text{ps}[i].\text{ib}.\text{rmAddr}(a);
\}\text{else }
\{\text{Ld, a, } \text{dest}\} & \text{exists in } \text{ps}[i].\text{ib}.
\end{aligned}\\
\text{WMM-LdIb rule (Ld execution: read stale value).} & \(\begin{aligned}
\{\text{Ld, a, } \text{dest}\} &= \text{ps}[i].\text{decode}(); \text{if } (\text{ps}[i].\text{sb}.\text{exist}(a)) \{
\text{ps}[i].\text{ib}.\text{rmAddr}(a);
\}\text{else }
\{\text{Ld, a, } \text{dest}\} & \text{is present in } \text{ps}[i].\text{ib}.
\end{aligned}\\
\end{tabular}
\end{table}

\begin{table}
\begin{tabular}{|c|c|}
\hline
\textbf{WMM-Commit rule (Commit execution).} & \(\begin{aligned}
\{\text{Commit}\} &= \text{ps}[i].\text{decode}(); \text{when } (\text{ps}[i].\text{sb}.\text{empty}());
\text{ps}[i].\text{execute}(\{\text{Commit}\} , -);
\end{aligned}\\
\text{WMM-Rec rule (Reconcile execution).} & \(\begin{aligned}
\{\text{Rec}\} &= \text{ps}[i].\text{decode}();
\text{ps}[i].\text{execute}(\{\text{Rec}\} , -);
\end{aligned}\\
\textbf{WMM-DqSb rule (dequeue store buffer).} & \(\begin{aligned}
a &= \text{ps}[i].\text{sb}.\text{anyAddr}(); \text{old} = \text{m}[a]; \text{when } (a \neq e);
\text{ps}[i].\text{ib}.\text{clear}(); \text{ps}[i].\text{execute}(\{\text{Rec}\} , -);
\text{ps}[i].\text{ib}.\text{rmAddr}(a);
\end{aligned}\\
\end{tabular}
\end{table}

Figure 7. WMM operational semantics

Load execution rules in Figure 7 correspond to three places from where a load can get its value. WMM-LdSb executes \(Ld\ a\) by reading from \(sb\). If address \(a\) is not found in \(sb\), then the load can read from the monolithic memory (WMM-LdMem). However, in order to allow the load to read a stale value (to model load reordering), WMM-LdIb gets the value from \(ib\). (Since getAny has side-effects, we use \(v\) to bind its return value to a free variable). The model allows non-deterministic choice in the selection of WMM-LdMem and WMM-LdIb. To make this idea work, WMM-LdMem has to remove all values for \(a\) from \(ib\), because these values are staler than the value in memory. Similarly, WMM-LdIb removes all the values for \(a\), which are staler than the one read, from \(ib\).

Synchronization instructions: Atomic read-modify-write (RMW) instructions can also be included in WMM. RMW directly operates on the monolithic memory, so the rule to execute RMW is simply the combination of WMM-LdMem, WMM-St and WMM-DqSb.

5.2 Litmus Tests for WMM

WMM executes instructions instantaneously and in order, but because of store buffers (\(sb\)) and invalidation buffers (\(ib\)), a processor can see the effect of loads and stores on some other processor in a different order than the program order on that processor. We explain the reorderings permitted and forbidden by the definition of WMM using well-known examples.

Fences for mutual exclusion: Figure 8 shows the kernel of Dekker’s algorithm in WMM, which guarantees mutual exclusion by ensuring registers \(r_1\) and \(r_2\) cannot both be zero at the end. All four fences are necessary. Without the Reconcile fence \(I_3\), \(I_4\) could read 0 from \(ib\), as if \(I_4\) overtakes \(I_1\) and \(I_2\). Without the Commit fence \(I_2\), \(I_1\) could stay in the \(sb\), and \(I_1\) gets 0 from memory.

Fences for message passing: Figure 9 shows a way of passing data 42 from \(P_1\) to \(P_2\) by setting a flag at address \(f\). Fences \(I_2\) and \(I_3\)
are necessary. Without the Commit fence I₂, the two stores on P₁ may get reordered in writing memory, so I₀ may not see the new data. Without the Reconcile fence I₇, I₀ could see the stale value 0 from ib. It is as if the two loads on P₂ are reordered.

Memory dependency speculation: WMM is able to capture the behaviors caused by memory dependency speculation in hardware. For example, the behavior in Figure 10 is possible in CCM+OOO⁵⁶ due to memory dependency speculation, i.e. P₂ predicts that the store address of I₅ is not a, and execute I₆ early to get value 0. WMM allows this behavior because I₆ can read 0 from ib.

Load-value speculation: WMM can capture the behaviors caused by load-value speculation in hardware. For instance, the behavior in Figure 11 is the result of such speculation in CCM+OOO⁵⁶, i.e. P₂ can predict the result of I₄ to be a and execute I₅ early to get value 0. When I₄ returns from memory later with value a, the prediction on I₄ turns out to be correct and the result of I₅ can be kept. WMM allows this behavior because I₅ can read 0 from ib.

SC for a single address: WMM maintains SC for all accesses to a single address, i.e. all loads the stores to a single address can be put into a total order, which is consistent with the program order (ps[i]), read-from relation (rf[i]), and coherence order (co[i]). The coherence order is a total order of stores to this address; in WMM it is the order of writing the monolithic memory. This property holds for WMM because both sb and ib manages values of the same address in a FIFO manner. This property also implies the following two axioms: [12][44][57] (L₁, L₂, S₁, S₂ denote loads and stores to the same address):

CoRR (Read-Read Coherence): L₁ po → L₂∧ S₁ rf → L₁∧ S₂ rf → L₂ ⇒ S₁ = S₂ ∨ S₁ co → S₂.

CoWR (Write-Read Coherence): S₂ rf → L₁∧ S₁ po → L₁ ⇒ S₁ = S₂ ∨ S₁ co → S₂.

WMM satisfies these two axioms. As for CCM+OOO⁵⁶, the coherence order is the order of writing the monolithic memory in CCM, and these two axioms hold due to the findAffectedLd and findStaleLd methods used in OOO⁵⁶ (see Appendix C for the proof).

SC for well-synchronized programs: The critical sections in well-synchronized programs are all protected by locks. To maintain SC behaviors for such programs in WMM, we can add a Reconcile after acquiring the lock and a Commit before releasing the lock.

Fences to restore SC: For any program, if we insert a Commit followed by a Reconcile before every Ld and St instruction, the program behavior in WMM will be sequential consistent.

In summary, WMM can reorder stores to different addresses, and allows a load to overtake other loads (to different addresses), stores and Commit fences. A load cannot overtake any Reconcile fence, while dependencies generally do not enforce ordering.

5.3 Equivalence of CCM+OOO⁵⁶ and WMM

Theorem 1. CCM+OOO⁵⁶ ◊ WMM.

Proof. First of all, for any execution in CCM+OOO⁵⁶ which contains flushes on rob, if we exclude the flushes and the part of the execution, of which the effects are canceled by the flushes, we will get a new execution with the same program results. Similarly, we could exclude any load re-execution (i.e. a store sets the ex field of a load to ReEx). Thus, we only need to consider executions in CCM+OOO⁵⁶ without any rob flush or load re-execution. For any such execution E in CCM+OOO⁵⁶, we could simulate E in WMM using the following way to get the same program behavior:

• When an instruction is committed from an ROB in E, we execute that instruction in WMM.

• When a store writes the monolithic memory of CCM (ccm.m) and is dequeued from a store buffer in E, we also dequeu that store and writes the monolithic memory (m) in WMM.

After each step of our simulation, we prove inductively that the following invariants hold:

1. The WMM states of m and all store buffers are the same as the CCM+OOO⁵⁶ states of ccm.m and all store buffers.

2. All instructions committed from ROBs in CCM+OOO⁵⁶ have also been executed in WMM with the same results.

The only non-trivial case is when a load L to address a is committed from the ROB of processor i (oo[i],rob) in CCM+OOO⁵⁶ and L is executed correspondingly by ps[i] in WMM. Assume that L reads from store S in CCM+OOO⁵⁶ (via memory, store buffer or ROB). We consider the status of S in CCM+OOO⁵⁶ when L is committed from ROB. If S is still in the store buffer (oo[i],ps) or ccm.m, then WMM can execute L by reading from ps[i],sb or m. Otherwise S must have been overwritten by another store in ccm.m before L is committed from ROB. In this case, WMM will insert the value of S into ps[i],ib when the overwrite happens in WMM, because there cannot be any store to a in oo[i],sb at the time of the overwrite. Now we only need to show that the value of S is not removed from ps[i],ib by any store. Reconcile or load before L is executed in WMM so that L could read the value of S from ps[i],ib in WMM. We consider the time period after the overwrite and before the commit of L in CCM+OOO⁵⁶, as well as the corresponding period in WMM (i.e. after the overwrite and before the execution of L). Since there cannot be any store to a or Reconcile fence committed from oo[i],rob during that period (otherwise L cannot read from S), the value of S will not be removed from ps[i],ib by stores or Reconcile fences during that period, and ps[i],sb will not contain any store to a when L is executed. Furthermore, the CoRR axiom of CCM+OOO⁵⁶ implies that each load L to address a committed from oo[i],rob during that period must read from either S or another S which writes ccm.m before S. Thus, the execution of L in WMM cannot remove S from ps[i],ib, and L can indeed read S from ps[i],ib.

Theorem 2. WMM ◊ CCM+OOO⁵⁶.

Proof. For any WMM execution E, we could construct a rule sequence E’ in CCM+OOO⁵⁶, which has the same program behavior. The first part of E’ is to fetch all instructions executed in E into the ROB of each processor (using OOO-Fetch rules), then predict the value of every load to the result of that load in E (using OOO-LdPred rules), and finally compute all Rm instructions, load/store addresses and store data. The rest of E’ is to simulate each rule in WMM using the following way:

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When a store is dequeued from \( ps[i] \) and \( sb \) and written into \( m \) in WMM, we also fire the OOO-StReq and CCM-St rules consecutively to write that store into \( ccm.m \) and dequeues it from \( ooo[I], sb \) in CCM+OOO\(^{VP} \).

When an instruction \( I \) is executed by \( ps[i] \) in WMM, we commit \( I \) from \( ooo[I].rob \) in CCM+OOO\(^{VP} \). If \( I \) is a Ld, we additionally schedule rules to execute this load in CCM+OOO\(^{VP} \).

If \( I \) reads from \( ps[i] \), \( sb \) in WMM, then we fire an OOO-LdBypass rule for \( I \) right before it is committed from ROB.

If \( I \) reads from \( m \) in WMM, then we fire an OOO-LdReq rule and a CCM-Ld rule consecutively to execute it right before the load value (which \( I \) gets in WMM) is overwritten in \( ccm.m \).

Although the construction of the rule sequence is not in order, the sequence constructed after every step is always a valid rule sequence in CCM+OOO\(^{VP} \) for all instructions already executed by WMM. When we schedule rules for an instruction \( I \) in CCM+OOO\(^{VP} \), the constructed \( E' \) does not contain any rule for instructions younger than \( I \) in program order, and thus the rules for \( I \) will not affect any existing rule in \( E' \). Besides, all operations that the execution of \( I \) depends on (e.g., executing an instruction older than \( I \), or writing a store, which \( I \) will read from \( ccm.m \) in the scheduled rule, into \( ccm.m \)) are already in the constructed \( E' \), so the scheduled rules for \( I \) will not depend on any rule scheduled in the future construction. We can prove inductively that the following invariants hold after each construction step:

1. The states of \( m \) and all \( sb \) in WMM are the same as the states of \( ccm.m \) and all \( sb \) in CCM+OOO\(^{VP} \).
2. All instructions executed in WMM have also been executed (with the same results) and committed from ROBs in CCM+OOO\(^{VP} \).
3. There is no ROB flush or load re-execution in \( E' \).

The only non-trivial case is that a load \( L \) to address \( a \) reads the value of a store \( S \) from \( ps[i] \), \( ib \) in WMM. In this case, the overwrite of \( S \) in \( ccm.m \) must happen in the constructed \( E' \), and \( L \) must be in \( ooo[I].rob \) at the time of overwrite. Since \( S \) is inserted into \( ps[i], ib \) and is not removed by any store or Reconcile before \( L \) is executed in WMM, there is no store to \( a \) or Reconcile fence older than \( L \) in \( ooo[I].rob \) or \( ooo[I].sb \) right before the overwrite in CCM+OOO\(^{VP} \). Thus the OOO-LdReq and CCM-Ld rules are able to fire and read the value of \( S \) at that time. The CoRR axiom of WMM implies that any load \( L' \) to \( a \) which is older than \( L \) must read from either \( S \) or another store that writes \( m \) before \( S \). Thus \( L' \) must get its result (not predicted values) before the overwrite in CCM+OOO\(^{VP} \), and \( L \) cannot be killed by \( L' \) (\( L \) cannot be killed or re-executed by any store because all OOO-SiEx rules are fired at the beginning).

6. Modeling Data Dependency

Current commercial processors do not use load-value speculation, and these processors can be modeled by CCM+OOO\(^{VP} \), in which OOO\(^{VP} \) is derived by removing the value predictor \( vp \) and related operations (e.g. the OOO-LdPred rule) from OOO\(^{VP} \). The removal of \( vp \) implies the enforcement of data-dependency ordering in hardware (CCM+OOO\(^{VP} \)). For example, the behavior in Figure 11 is forbidden by CCM+OOO\(^{VP} \). However, it requires inserting a Reconcile fence between \( I_1 \) and \( I_2 \) to forbid this behavior in WMM. This fence may cause performance loss because it would prevent the execution of loads that follow \( I_2 \) but do not depend on \( I_1 \). This is an unnecessary cost if programs are running on commercial hardware captured by CCM+OOO\(^{VP} \). To avoid extra Reconcile fences, we present WMM-D, an \( 1^2E \) model equivalent to CCM+OOO\(^{VP} \).

WMM-D is derived from WMM by introducing timestamps to exclude exactly the behaviors that violate data-dependency orderings.

6.1 Enforcing Data Dependency with Timestamps

We derive our intuition for timestamps by observing how OOO\(^P \) works. In Figure 11, assume instruction \( I_k \) (\( k = 1 \ldots 5 \)) gets its result or writes memory at time \( t_k \) in CCM+OOO\(^P \). Then \( t_5 \geq t_4 \) because the result of \( I_4 \) is a source operand of \( I_5 \) (i.e., the load address). Since \( I_4 \) reads the value of \( I_3 \) from memory, \( t_4 \geq t_3 \), and thus \( t_5 \geq t_3 \geq t_1 \). As we can see, the time ordering reflects enforcement of data dependencies. Thus, a natural way to extend WMM to WMM-D is to attach a timestamp to each value, which will, in turn, impose additional constraints on rule firing in WMM. Now we explain how to add timestamps to WMM to get WMM-D.

Let us assume there is a global clock which is incremented every time a store writes the monolithic memory. We attach a timestamp to each value in WMM, i.e. an architecture register value, the \( (\text{address, value}) \) pair of a store, and a monolithic memory value. The timestamp represents when the value is created. Consider an instruction \( r_1 = r_1 + r_2 \). The timestamp of the new value in \( r_3 \) will be the maximum timestamp of \( r_1 \) and \( r_2 \). Similarly, the timestamp of the \( (\text{address, value}) \) pair of a store \( (St \ a \ v) \), i.e. the creation time of the store, is the maximum timestamp of all source operands to compute \( (a, v) \). The timestamp of a monolithic memory value is the time when the value becomes visible in memory, i.e. one plus the time when the value is stored.

Next consider a load \( L \) (\( Ld \ a \) on processor \( i \), which reads the value of a store \( S \) (\( St \ a \ v \)). No matter how WMM executes \( L \) (e.g. by reading \( sb \), memory, or \( ib \)), the timestamp \( ts \) of the load value (i.e. the timestamp for the destination register) is always the maximum of (1) the timestamp \( ats \) of the address operand, (2) the time \( rts \) when processor \( i \) executes the last Reconcile fence, and (3) the time \( vts \) when \( S \) becomes visible to processor \( i \). Both \( ats \) and \( rts \) are straightforward. As for \( vts \), if \( S \) is from another processor \( j \) (\( j \neq i \)), \( S \) is visible after it writes memory, so \( vts \) is timestamp of the monolithic memory value written by \( S \). Otherwise, \( S \) is visible to processor \( i \) after it is created, so \( vts \) is the creation time of \( S \).

A constraint for \( L \), which we refer to as stale-timing, is that \( ts \) must be \( \leq \) the timestamp \( ts_E \) when \( S \) is overwritten in memory. This constraint is only relevant when \( L \) reads from \( ib \). This constraint is needed because a load cannot return a value in CCM+OOO\(^P \) if the value has been overwritten in CCM at the time of load execution.

To carry out the above timestamp calculus for load \( L \) in WMM, we need to associate the monolithic memory \( m[a] \) with the creation time of \( S \), and the processor that created \( S \), when \( S \) updates \( m[a] \). When \( S \) is overwritten and its \( (a, v) \) is inserted into \( ps[i], ib \), we need to attach the time interval \( [vts, ts_E] \) (i.e. the duration that \( S \) is visible to processor \( i \)) to that \( (a, v) \) in \( ps[i], ib \).

It should be noted that PC should never be involved in the timestamp mechanism of WMM-D, because the PC of each instruction can be known in advance due to the branch predictor \( bp \) in OOO\(^P \).

By combining the above timestamp mechanism with the original WMM rules, we have derived WMM-D.

6.2 WMM-D Operational Semantics

Figure 12 shows the operational semantics of WMM-D. We list the things one should remember before reading the rules in the figure.

- The global clock name is \( gts \) (initialized as 0), which is incremented when the monolithic memory is updated.
- Each register has a timestamp (initialized as 0) which indicates when the register value was created.
- Each \( sb \) entry \( (a, v) \) has a timestamp, i.e. the creation time of the store that made the entry. Timestamps are added to the method calls on \( sb \) as appropriate.
• Each monolithic memory location \( m[a] \) is a tuple \((v, (i,sts, mts))\) (initialized as \((0, (-,0), 0))\), in which \( v \) is the memory value, \( i \) is the processor that writes the value, \( sts \) is the creation time of the store that writes the value, and \( mts \) is the timestamp of the memory value (i.e. one plus the time of memory write).

• Each \( ib \) entry \((a,v)\) has a time interval \([ts_1, ts_3]\), in which \( ts_1 \) is the time when \((a,v)\) becomes visible to the processor of \( ib \), and \( ts_3 \) is the time when \((a,v)\) is overwritten in memory and gets inserted into \( ib \). Thus, the insert method on \( ib \) takes the time interval as an additional argument.

• Each processor \( ps[i] \) has a timestamp \( rts \) (initialized as 0), which records when the latest Reconlate was executed by \( ps[i] \).

Some of the timestamp manipulation is done inside the decode and execute methods of each processor \( ps[i] \). Therefore we define the following methods:

• \( \text{decodeTS}() \): returns a pair \((dIns, ts)\), in which \( dIns \) is the decoded instruction returned by the original decode() method, and \( ts \) is the maximum timestamp of all source registers (excluding PC) of \( dIns \).

• \( \text{executeTS}(dIns, ldRes, ts) \): first calls the original method \( \text{execute}(dIns, ldRes) \), and then writes timestamp \( ts \) to the destination register of instruction \( dIns \).

We also replace the getAny method on \( ib \) with the following two methods to facilitate the check of the stale-timeing constraint:

• \( \text{any}(a) \): returns the \((value, time interval)\) pair of any stale value for address \( a \) in \( ib \). If \( ib \) does not contain any stale value for \( a \), \( (\_\_\_, \_\_\_\_) \) is returned.

• \( \text{rmOlder}(a, ts) \): removes all stale values for address \( a \), which are inserted into \( ib \) when \( gts < ts \), from \( ib \).

In Figure 12, WMM-D-Nm and WMM-D-St compute the timestamps of a \( \text{Nm} \) instruction result and a store \((a,v)\) pair from the timestamps of source registers respectively. WMM-D-Rec updates \( ps[i].rts \) with the current time because a Reconlate is executed. WMM-D-DeqSb attaches the appropriate time interval to the stale value inserted into \( ib \) as described in Section 6.3.

In all three load execution rules (WMM-D-LdSb, WMM-D-LdMem, and WMM-D-Ldlb), the timestamp of the load result is \( \geq \) the timestamp of the address operand \((ats)\) and the latest Reconlate execution time \((ps[i].rts)\). Besides, the timestamp of the load result is also lower-bounded by the beginning time that the value is readable by the processor of the load \((ps[i])\). In WMM-D-LdSb and WMM-D-Ldlb, this beginning time \((i.e. \text{sts or ts}_L)\) is stored in the \( sb \) or \( ib \) entry; while in WMM-D-LdMem, this beginning time is one of the two times \((i.e. \text{sts and ts}_L)\) stored in the monolithic memory location depending on whether the memory value \( v \) is written by \( ps[i] \) (i.e. whether \( i \) is equal to \( j \)). In WMM-D-Ldlb, the stale-timeing constraint requires that \( \text{max(ats, ps[i].rts, ts}_L) \) (i.e. the timestamp of the load value) is no greater than \( ts_0 \) (i.e. the time when the stale value is overwritten). Here we only compare \( ats \) with \( ts_1 \), because \( ts_1 < ts_0 \) is obvious, and the clearing of \( ib \) done by Reconlate fencies already ensures \( ps[i].rts \leq ts_0 \).

### 6.3 Litmus Tests for WMM-D

**Enforcing data dependency:** First revisit the behavior in Figure 11. In WMM-D, the timestamp of the source operand of \( I_3 \) (i.e. the result of \( I_2 \)) is 2, while the time interval of the stale value 0 for address \( a \) in the \( ib \) of \( P1 \) is \([0,0]\). Thus \( I_2 \) cannot read from \( ib \), and the behavior is forbidden. For a similar reason, WMM-D forbids the behavior in Figure 13 in which \( I_4 \) carries data dependency to \( I_7 \) transitively. This behavior is also impossible in CCM+OOGP.

**Allowing other speculations:** WMM-D still allows the behavior in Figure 10 which can result from memory dependency speculation in hardware. As we can see, WMM-D still allows implementations to speculate on all dependencies other than data dependency.

**Loads to the same address:** Remember that any load to the same address can be executed out of order in OOGP as long as they read from the same store. WMM-D captures this subtle optimization. Consider the Read-from-Same-Write (RSW) program in Figure 12. The behavior is observable in CCM+OOGP, because \( I_7 \) to \( I_9 \) can be executed before \( I_4 \) to \( I_6 \). It is fine for \( I_9 \) and \( I_7 \), which read the same address \( c \), to be executed out-of-order, because they both read from the initialization store. WMM-D allows this behavior, because the timestamp of the address operand of \( I_9 \) is 0, and \( I_9 \) can read stale value 0 from \( ib \). (This behavior is also observable on POWER and ARM processors.)
6.4 Equivalence of WMM-D and CCM+OOO^D

To simplify the proof, we change the findBypass(idx) method in OOO^D to return \( \epsilon \) whenever there is a Reconcile fence at index smaller than idx in ROB, i.e., a load will always be stalled when there is an older Reconcile in ROB. This change in findBypass only affects one scenario: a load used to be able to bypass from a store when there is a Reconcile fence older than both the load and store in ROB, and operations dependent on the load result could change in the processor, they can still be performed with the same effects immediately after the Reconcile is committed from ROB. Thus, the change in findBypass does not affect the semantics of OOO^D.

**Theorem 3.** CCM+OOO^D \( \subseteq \) WMM-D.

**Proof.** We also introduce the global clock gts to CCM+OOO^D; gts is be incremented whenever the CCM-St fires. This proof is almost the same as that of Theorem 1 except for a new invariant: The timestamp computed for each instruction result (i.e. Nrm result, store address and data, and load value) in WMM-D is \( \leq \) the the value of gts when the instruction gets its result in CCM+OOO^D. See Appendix A for the complete proof.

**Theorem 4.** WMM-D \( \subseteq \) CCM+OOO^D.

**Proof.** We also introduce the global clock gts to CCM+OOO^D; gts is be incremented whenever the CCM-St fires. This proof is similar to the proof for Theorem 3 except for the following two points:

1. Without a value predictor in OOO^D, the time when an instruction can be executed in CCM+OOO^D is subject to when the source operands of the instruction become ready. When constructing the execution for CCM+OOO^D (to simulate the behavior of WMM-D), we always fire the instruction execution rule as early as possible. In particular for each Ld instruction, we execute it (by firing the OOO-LdAddr and OOO-LdBypass rules or the OOO-LdAddr, OOO-LdReq, and CCM-Ld rules) as soon as the source operands are ready and the expected load value (i.e. the value read in WMM-D) becomes visible to the processor.

2. A new invariant: the value of gts in CCM+OOO^D when an instruction gets its result (Nrm result, store address and data, or load value) is equal to the timestamp of that result in WMM-D. See Appendix A for the complete proof.

7. Modeling Multi-Copy Non-Atomic Stores

Unlike the multi-copy atomic stores in WMM, stores in ARM and POWER multiprocessors are multi-copy non-atomic, i.e., a store may become visible to different processors at different times. This is caused by sharing store buffers or write-through caches in the memory system. If multiple threads share a store buffer or a write-through cache, a store by any of these threads may be seen by all these threads before other processors. Although we could tag stores with thread IDs in the store buffer, it is infeasible to distinguish between stores by different threads in the write-through cache. While CCM cannot model such store behaviors, the storage subsystem of the Flowing model is believed to have captured precisely the behaviors of this multi-copy non-atomicity given a topology of the hierarchy of shared store buffers or write-through caches.

In this section, we first introduce a new \( l^2E \) model, WMM-S, which captures the multi-copy non-atomic store behaviors in a topology-independent way. WMM-S is derived from WMM by changing the store buffers to a new conceptual device: dynamic store buffers. Next we introduce HMB+OOO^S, the physical model for multiprocessors with multi-copy non-atomic stores; HMB is the memory abstraction taken from the Flowing model and OOO^S is the processor model adapted from OOO^D. We will finally prove HMB+OOO^S \( \subseteq \) WMM-S.

7.1 WMM-S: Copying From One Store Buffer into Another

We can model the multi-copy non-atomicity of stores by introducing a background rule to make copies of a store in a store buffer into other store buffers. We refer to these store buffers with the ability of copying stores as dynamic store buffers. (We will still use store buffers to refer to dynamic store buffers in the rest of this section). However, we need to ensure that all stores for an address can be put in a total order, i.e. the coherent order (\( \langle \nu \rangle \)), and the order seen by any processor is consistent with this total order (i.e. SC for a single address). WMM-S is an \( l^2E \) model to generate such behaviors.

To identify all the copies of a store in various store buffers, we assign a unique tag \( t \) when a store is inserted in the store buffer, and this tag is copied when a store is copied from one store buffer to another. When a store is committed from the store buffer to the memory, all its copies must be deleted from all the store buffers which have them. A store can be committed only if all its copies are the oldest store for that address in their respective store buffers.

All the stores for an address in a store buffer are kept as a strictly ordered list, where the youngest store is the one that entered the store buffer last. We make sure that all ordered lists are can be combined transitive to form a strict partial order, which has now been understood in terms of the tags on stores because of the copies. By the end of the program, this partial order on the stores for an address becomes the coherence order, so we refer to this partial order as the partial coherence order.

Consider the states of store buffers shown in Figure 15. A, B, C and D are different stores to the same address, and their tags are \( t_A, t_B, t_C \) and \( t_D \), respectively. \( A' \) and \( B' \) are copies of \( A \) and \( B \) respectively created by the background copy rule. Ignoring \( C' \), the partial coherence order contains: \( t_B \xrightarrow{\text{copy}} t_B \xrightarrow{\text{copy}} t_A \) (\( A \) is older than \( t_B \), and \( B \) is older than \( A \) in P2), and \( t_{C} \xrightarrow{\text{copy}} t_{B} \) (\( C \) is older than \( C' \) in P3). Note that \( t_B \) and \( t_C \) are not related here.

At this point, if we copied \( C \) in P3 as \( C' \) into P1, we would add a new edge \( t_A \xrightarrow{\text{copy}} t_C \), which would break the partial order by introducing the cycle \( t_A \xrightarrow{\text{copy}} t_C \xrightarrow{\text{copy}} t_B \xrightarrow{\text{copy}} t_A \). Therefore copying of \( C \) into P1 should not be allowed in this state. Similarly, a copying with tag \( t_A \) into P1 or P2 should be forbidden because it would immediately create a cycle: \( t_A \xrightarrow{\text{copy}} t_A \). In general, the background copy rule must be constrained so that invariance of the partial coherence order after copying is maintained.

![Figure 15. Example states of store buffers (primes are copies)](image-url)

The operational semantics of WMM-S is defined by adding/replacing three rules to that of WMM (Figure 7). These new rules are shown in Figure 16. A new background rule WMM-S-Copy is added to WMM and the WMM-S-St and WMM-S-DeqSb rules replace the WMM-St and WMM-DeqSb rules of WMM, respectively. Before reading these new rules, one should note the following facts:

- The decode method now returns \( \langle \text{St}, a, t, v \rangle \) for a store, in which \( t \) is the unique tag assigned to the store. Each store buffer entry becomes a tuple \( \langle a, t, v \rangle \), in which \( t \) is the tag. Tags are also introduced into the methods of \( \text{sb} \) appropriately.
- The \( \text{sb} \) now has the following three methods:
  - \( \text{hasTag}(t) \): returns True if \( \text{sb} \) contains a store with tag \( t \).
• oldest(a): returns the (value, tag) pair of the oldest store to address a in sb. It returns (ε, ε) if sb does not contain a.
• any(): returns the (address, value, tag) tuple of any store present in sb. It returns (ε, ε, ε) if sb is empty.

A new function noCycle(a, t, j) is defined to check whether the background rule could copy a store with tag t for address a into the sb of processor j. It returns True if the partial coherence order among the tags of all stores for address a does not contain any cycle after doing the copy.

\[
\text{noCycle}(a, t, j) = \begin{cases} \\
\end{cases}
\]

1. HMB-Reorder: Two consecutive requests \( r_{\text{new}} \) and \( r_{\text{old}} \) in the same segment \( r_{\text{new}} \) is closer to the top of the list of the segment can be reordered except for the following two cases:

(a) \( r_{\text{new}} \) and \( r_{\text{old}} \) are memory accesses to the same address.

(b) \( r_{\text{new}} \) is a Commit and \( r_{\text{old}} \) is a store.

2. HMB-Preempt: When a load request \( r = \langle \text{Ld}, pid, idx, a \rangle \) (i.e. a load to address a from the ROB entry with index \( idx \) of processor \( pid \)) and a store request \( r' = \langle \text{St}, a, t, v \rangle \) (i.e. a store to address a with data v and tag t) are two consecutive requests in the segment \( r' \) is closer to the bottom of the segment, we can remove \( r \) from the segment and call method \text{respld}(idx, v, t, \langle \text{Ld}, pid, idx, a \rangle) \) of processor \( pid \) (i.e. \( r \) is satisfied by \( r' \)).

3. HMB-Flow: The request \( r \) at the bottom of segment \( s[i] \) can be removed from \( s[j] \). If the parent of \( s[j] \) is another segment \( s[j'] \), we add \( r \) to the top of \( s[j'] \) (i.e. \( r \) flows from \( s[j] \) to its parent \( s[j'] \)). Otherwise, the parent of \( s[i] \) is m, and we take the following actions according to the type of \( r \):

- If \( r \) is \( \langle \text{Ld}, pid, idx, a \rangle \), we call method \text{respld}(idx, v, t, \langle \text{Ld}, pid, idx, a \rangle) of processor \( pid \), in which pair \( (v, t) \) is the current state of \( m[a] \).
- If \( r \) is \( \langle \text{Commit}, pid, i \rangle \), a Commit fence from processor \( pid \), we call method \text{respc}(\langle \text{Commit}, pid, i \rangle) \) (which is defined later) of processor \( pid \) to indicate the completion of the fence.
• If $r$ is $(S_t, a, v, t)$, we update $m[a]$ to be $(v, t)$. No response is sent for the store request.

We adapt OOO$^3$ to OOO$^3$ to fit the new memory system. The operational semantics (the changed part) and the interface methods of OOO$^3$ are shown in Figures 19 and 20 respectively, where $hmb$ represents the HMB interface port connected to the processor, and method rob.setCommit$(en)$ sets the commit slot of ROB to $en$.

The first change for OOO$^3$ is to remove $sb$ from each processor, because store buffering is already modeled inside HMB. Thus, when a store is committed from ROB in rule OOO$^3$.StCom, the store request is directly sent to HMB. The second change is sending a Commit request to HMB when a Commit fence reaches the commit slot of ROB as shown in rule OOO$^3$.ComReq. When the Commit response comes back from HMB via method respCom, the fence is committed from ROB. To avoid duplicate Commit requests to HMB, we change function initExe to also return fId to a Commit fence, and hence the ex field of a Commit fence will be set to fId in rule OOO-Fetch. When the Commit request is sent to HMB in rule OOO$^3$.ComReq, we set the ex field to Exe.

The last change is about detecting whether the out-of-order execution of loads to the same address in the same processor violates SC for single address. The detection is harder in case of HMB than that in CCM, because loads can be satisfied in any segment or monolithic memory inside HMB, while loads can only be satisfied in the monolithic memory in case of CCM. The original Flowing model has specified complicated conditions of this check to avoid unnecessary flush of loads, but we believe those conditions may still cause some loads to be flushed unnecessarily. Instead of further complicating the check, we simply guarantee that loads to the same address are issued to HMB in order. Since HMB keeps the order of memory accesses to the same address, this can ensure SC for single address. Rule OOO$^3$.LdReq enforces the in-order issue by killing younger loads in the same way as the OOO-StEx rule does. This also makes OOO$^3$.CCM obey the CoRR and CoWR axioms (see Appendix C for the proof).

### 7.4 WMM-S Abstracting HMB+OOO$^5$

**Theorem 5.** $HMB+OOO^5 \subseteq WMM-S$.

**Proof.** Similar to the proof of Theorem 1, we only consider executions in $HMB+OOO^5$ without any ROB flush or load re-execution.

At any moment in $HMB+OOO^5$, we define a store $S$ is observed by commits of processor $i$ (oooi) if and only if $S$ has been committed from ooo[i].rob or $S$ has been returned by a load $L$ which has been committed from ooo[i].rob. For two stores $S_1$ and $S_2$ both observed by commits of a processor, we say $S_1$ is closer to the root than $S_2$ in HMB, when the segment of $S_1$ is closer to the root than that of $S_2$ in the tree hierarchy of HMB (assuming each edge in the tree has length 1), or when $S_1$ and $S_2$ are in the same segment and $S_1$ is closer to the bottom of the segment.

For any execution $E$ in $HMB+OOO^5$, we simulate it in WMM-S using the following way:

- When a store request flows into the monolithic memory inside HMB ($hmb.m$) using the HMB-Flow rule of $HMB+OOO^5$, WMM-S fires a WMM-S-DeqSb rule to dequeue that store from all store buffers and write it into the monolithic memory ($m$).
- When a Nm, Reconcile, or St instruction is committed from ROB in $HMB+OOO^5$, we execute that instruction in WMM-S.
- When a Commit fence is committed from ROB in the respCom method called by a HMB-Flow rule in $HMB+OOO^5$, we execute that fence in WMM-S.
- When a Ld instruction $L$, which reads from a store $S$, is committed from $oooi.rob$ in $HMB+OOO^5$, we execute $L$ using the following actions in WMM-S according to the status of $S$ right before the commit of $L$ in $HMB+OOO^5$.
  - If $S$ is in $hmb.m$ at that time, then WMM-S executes $L$ by reading from $m$.
  - If $S$ has been overwritten in $hmb.m$ before the commit of $L$, then $L$ can read $ps[i].sb$ in WMM-S.
  - If $S$ is in a segment inside HMB at that time, then $L$ should read $ps[i].sb$ in WMM-S. In case $S$ is not observed by commits of $oooi$ right before the commit of $L$, we fire a WMM-S-Copy rule to copy $S$ into $ps[i].sb$ right before $L$ reads $ps[i].sb$.

After each step of the simulation, we could prove inductively that the following invariants hold:

1. All stores in $ps[i].sb$ in WMM-S are exactly the set of stores, which are in the segments of HMB and observed by commits of ooo[i]. The segments that contain these stores must be on the path from the root to port $i$ in the tree hierarchy of HMB.
2. In case $S_1$ and $S_2$ are two stores to the same address in $ps[i].sb$, $S_1$ is older than $S_2$ in $ps[i].sb$ if and only if $S_1$ is closer to the root than $S_2$ in HMB.

We do not take any action in WMM-S when requests flow between segments in HMB or when requests are reordered in HMB. These operations in $HMB+OOO^5$ do not affect the above invariants.

Here we only consider the final case, i.e. a load $L$ to address $a$, which reads from a store $S$, is committed from $oooi.rob$ in $HMB+OOO^5$, and $S$ remains in a segment of HMB at the commit time of $L$. If $S$ has already been observed by commits of $oooi$ before the commit of $L$, the CoRR and CoWR axioms of HMB+OOO$^5$ imply that there cannot be any store to $a$ which is also observed by commits of $oooi$ and is further from root than $S$ in HMB. Thus, $S$ must be the youngest store to $a$ in $ps[i].sb$ and $L$ can read from it in WMM-S. Otherwise, $S$ is not observed by commits of $oooi$ right before the commit of $L$, and the CoRR and CoWR axioms of HMB+OOO$^5$ imply that $S$ must be further from root in the tree hierarchy of HMB than any store observed by commits of $oooi$ at that time. Therefore, if we insert $S$ into $ps[i].sb$, both invariants still hold. Since there is no cycle in the tree hierarchy of HMB and the order of stores to the same address in any store...
buffer in WMM-S is the same as the order of distance from the root of those stores in HMB, the noCycle check in the WMM-S-Copy rule which copies $S$ into $ps[i].sb$ must succeed. Then $L$ can read from $S$ in $ps[i].sb$. See Appendix B for remaining cases.

8. Conclusion

We provide a framework which uses simple hardware abstractions based on $I^2E$ processors, monolithic memory, invalidation buffers, timestamps and dynamic store buffers to capture all microarchitectural optimizations present in modern processors. We have proved the equivalences between the simple abstractions and their realistic microarchitectural counterparts; we believe this work can be useful for both programmers to reason about their programs on real hardware, and on architects to reason about the effect of their optimizations on program behavior.

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Proof. In order to relate the time in CCM+OOOP to that in WMM-D, we also introduce the global clock \(gts\) to CCM+OOOP. \(gts\) is incremented by one whenever the CCM-St rule fires, i.e. when the monolithic memory of CCM (ccm.m) is written. In the rest of this proof, we mean the value of \(gts\) when referring to time. Similar to the proof of Theorem 1 (i.e. CCM+OOOP \(\subseteq\) WMM in the paper), we only need to consider executions in CCM+OOOP without any ROB flush or load re-execution.

For any execution \(E\) in CCM+OOOP, we simulate it using the same way as in the proof of Theorem 1, i.e. when CCM+OOOP commits an instruction from ROB or writes a store into ccm.m, WMM-D executes that instruction or writes that store into \(m\). After each step of simulation, we maintain the following invariants (\(oo[i]\) represents processor \(i\) in CCM+OOOP):

1. The states of \(m\) and all \(sb\) in WMM are the same as ccm.m and all \(sb\) in CCM+OOOP.
2. The \(gts\) in WMM is the same as that in CCM+OOOP.
3. All instructions committed from ROBs in CCM+OOOP have also been executed with the same results in WMM.
4. The \(rts\) of each processor \(ps[i]\) in WMM is equal to the time when the last Reconcile fence is committed from \(oo[i].ro\).
5. The timestamp of the result of each Nm or Ld instruction in WMM is \(\leq\) the time when the instruction gets its result in CCM+OOOP by the OOO-NmEx, OOO-LdBypass, or OOO-Ld rule.
6. The timestamp of each store in any \(sb\) in WMM is \(\leq\) the time when the store is executed in CCM+OOOP by the OOO-StEx rule.
7. For each monolithic memory location \(m[a] = (v, (i, \text{sts}, \text{mts})\) in WMM, \(\text{sts}\) is \(\leq\) the time when the store that writes \(v\) to memory is executed in \(oo[i].ro\) in CCM+OOOP, and \(\text{mts}\) is equal to the time right after that store writes ccm.m in CCM+OOOP.
8. For each invalidation buffer entry \((a, v, \langle ts_L, ts_U\rangle)\) of \(ps[i].ib\) in WMM, \(ts_U\) is the time right before value \(v\) is overwritten by another store in ccm.m. If the store that writes \(v\) to memory is from processor \(i\), then \(ts_L\) is \(\leq\) the time when that store is executed in \(oo[i].ro\) by the OOO-StEx rule. Otherwise, \(ts_L\) is equal to the time right after \(v\) is written to ccm.m.

The above invariants can be proved inductively in the same way used in the proof of Theorem 1.

In particular, we consider the case that CCM+OOOP commits a load \(L\) to address \(a\), which reads the value of store \(S\) from \(oo[i].ro\). In this case, WMM executes \(L\) on \(ps[i]\) according to the status of \(S\) in CCM+OOOP when \(L\) is committed from \(oo[i].ro\).

- If \(S\) is still in \(oo[i].sb\) when \(L\) commits from ROB, then WMM-D can execute \(L\) by reading \(ps[i].sb\) (i.e. the WMM-D-LdMem rule).
- If \(S\) is in ccm.m at that time, then WMM-D executes \(L\) by reading \(m\) (i.e. the WMM-D-LdMem rule). Note that \(S\) may be from processor \(i\) or another processor \(j\). In either case, the WMM-D-LdMem rule maintains all the invariants.

The final case is that \(S\) has been overwritten by another store in ccm.m before \(L\) is committed from ROB. In this case, WMM-D executes \(L\) by reading \(ps[i].ib\) (i.e. the WMM-D-LdDb rule). For the same reason used in the proof of Theorem 1, the value of \(S\) will be in \(ps[i].ib\) when \(L\) is executed in WMM-D. We assume the time interval of \(S\) in \(ps[i].ib\) is \([ts_L, ts_U]\). The guard of the WMM-D-LdB rule, i.e. \(ats < ts_L\) (\(ats\) is the timestamp of the load address), will be satisfied, because timestamps in WMM is always \(\leq\) the corresponding time in CCM+OOOP, and the source register values for the load address must have been computed before the load value is overwritten in ccm.m in CCM+OOOP.

No matter \(S\) is from processor \(i\) or another processor, the way of setting \(ts_L\) when \(S\) is inserted into \(ps[i].ib\) ensures that the timestamp computed for the load result in the WMM-D-LdB rule conforms to all the invariants.

\[\square\]

**Theorem 4.** WMM-D \(\subseteq\) CCM+OOOP.

Proof. We still introduce \(gts\) into CCM+OOOP, and \(gts\) is incremented by one whenever a store writes ccm.m. Since multiple rules of CCM+OOOP may fire under the same \(gts\), we introduce a pair \((ut, ll)\) to specify the exact time when each rule fires; \(ut\) is the upper time, which specifies the value of \(gts\) when the rule fires; \(ll\) is the lower time, a rational number inside \((0, 1]\), which is used to order rules with the same upper time. When comparing two time pairs, we first compare the \(ut\) part, and only compare the \(ll\) part when \(ut\) parts are equal. All OOO-StReq rules must have \(ll = 1\), while all other rules in CCM+OOOP must have \(0 < ll < 1\).

For any WMM execution \(E\), we could construct a rule sequence \(E'\) in CCM+OOOP, which has the same program behavior. In the construction of \(E'\), we always fire the OOO-StReq and CCM-St rules atomically to write a store to ccm.m, so we only use OOO-StReq to denote this sequence in the rest of the proof. Similarly, we always fire OOO-LdAddr and OOO-LdBypass atomically to forward data to a load, and always fire OOO-LdAddr, OOO-LdReq, and CCM-Ld rules atomically to satisfy a load from ccm.m, so we will only mention the OOO-LdBypass and OOO-LdReq rules to refer to the above two atomic sequences in the rest of the proof.

The first part of \(E'\) is to fetch all instructions executed in \(E\) into the ROB of each processor (using OOO-Fetch rules). The construction of the rest of \(E'\) is similar to that in the proof of Theorem 2 (i.e. WMM \(\subseteq\) CCM+OOOP in the paper), i.e. when WMM-D writes a store to \(m\) or executes an instruction, we write that store to ccm.m or schedule rules to execute and commit that instruction in CCM+OOOP. We maintain the following invariants after each step of construction (the states of CCM+OOOP refers to the states after firing all rules in the constructed \(E'\)):

1. The states of \(m\) and all \(sb\) in WMM are the same as the states of ccm.m and all \(sb\) in CCM+OOOP.
2. The \(gts\) in WMM is the same as that in CCM+OOOP.
3. The upper time assigned to each rule in \(E'\) is equal to the value of \(gts\) when the rule fires. The lower time assigned to each OOO-StReq is 1, while the lower time assigned to other rule is within \((0, 1]\).
4. All instructions executed in WMM have also been executed (with the same results) and committed from ROBs in CCM+OOOP.
5. The value of \(gts\) when each instruction is executed or each store is written into \(m\) in WMM-D is equal to the upper time of the rule to commit that instruction from ROB or write that store to ccm.m in CCM+OOOP.
6. For each Nm, St or Ld instruction executed in WMM-D, the timestamp computed for the execution result (i.e. Nm instruction result, store address and data, or load result) in WMM-D is equal to the upper time of corresponding rule in CCM+OOOP (i.e. OOO-NmEx, OOO-StEx, OOO-LdBypass, or OOO-LdReq) that executes the instruction.

7. No flush or load re-execution happens in any ROB.

Besides proving the above invariants, we also need to show that the rules scheduled in \(E'\) can indeed fire, e.g., the time of a rule to execute an instruction is smaller than the time of committing that instruction, but is larger than the time of each rule that computes the source operand of that instruction.

The detailed way of constructing \(E'\) to simulate each rule in WMM is shown below (the current states of CCM+OOOP refers to the states after firing all existing rules in the constructed \(E'\)):
• When WMM-D writes a store from \texttt{ps[i], sb} into \texttt{m}, we fire the \texttt{OOO-StReq} rule to write that store from \texttt{ooo[i], sb} to \texttt{ccm.m} at time \langle \texttt{ut}, 1 \rangle in \texttt{E}', in which \texttt{ut} is the current \texttt{gts} in \texttt{CCM+OOOP}.

• When an instruction \texttt{I} is executed by \texttt{ps[i]} in WMM-D, we commit \texttt{I} from \texttt{ooo[i], rob} in \texttt{E}' at time \langle \texttt{ut}_{c}, \texttt{lt}_{c} \rangle, in which \texttt{ut}_{c} is the current \texttt{gts} in \texttt{CCM+OOOP}, and \texttt{lt}_{c} is chosen so that this commit rule happens after all existing rules in \texttt{E}'. If \texttt{I} is Nm, St or Ld, we also need to schedule rules to execute it. Assume the maximum time among all the rules to compute the source register values of \texttt{I} is \langle \texttt{ut}_{a}, \texttt{lt}_{a} \rangle. (All such rules must have been decided in the previous construction steps).

  • If \texttt{I} is \texttt{Nm} or \texttt{St}, then we schedule the corresponding \texttt{OOO-NmEx} or \texttt{OOO-StEx} rule for \texttt{I} to fire at time \langle \texttt{ut}_{a}, \texttt{lt}_{a} \rangle; \texttt{lt}_{a} is chosen so that \texttt{lt}_{a} < \texttt{ut}_{a} < 1 and \langle \texttt{ut}_{a}, \texttt{lt}_{a} \rangle < \langle \texttt{ut}_{c}, \texttt{lt}_{c} \rangle.

  • If \texttt{I} is \texttt{Ld}, we assume that \texttt{I} reads from a store \texttt{S} in \texttt{E}, and that \texttt{ooo[i]} commits the last Reconcile older than \texttt{I} at time \langle \texttt{ut}_{e}, \texttt{lt}_{e} \rangle in the previously constructed \texttt{E}'.

    - If \texttt{S} and \texttt{I} are from the same processor (i.e. \texttt{ooo[i]}), let \langle \texttt{ut}_{s}, \texttt{lt}_{s} \rangle be the time of the \texttt{OOO-StEx} rule for \texttt{S} in the previously constructed \texttt{E}'. Fire either a \texttt{OOO-LdBypass} rule or a \texttt{OOO-LdReq} rule (depending on where \texttt{S} is at the rule firing time) to execute \texttt{I} at time \texttt{E}' in \texttt{E}' at time \langle \texttt{ut}_{e}, \texttt{lt}_{e} \rangle, in which \texttt{ut}_{e} = \max(\texttt{ut}_{s}, \texttt{ut}_{a}, \texttt{ut}_{e}, \texttt{ut}_{w}, 1) \cdot \texttt{lt}_{e} is chosen so that \langle \texttt{ut}_{e}, \texttt{lt}_{e} \rangle > \langle \texttt{ut}_{e}, \texttt{lt}_{e} \rangle > \max(\langle \texttt{ut}_{e}, \texttt{lt}_{e} \rangle, \langle \texttt{ut}_{e}, \texttt{lt}_{e} \rangle) \cdot \texttt{lt}_{e} < 1.

    - Otherwise, \texttt{S} and \texttt{I} are from different processors, and \langle \texttt{ut}_{s}, 1 \rangle be the time of the \texttt{OOO-StReq} rule that writes \texttt{S} into \texttt{ccm.m} in the previously constructed \texttt{E}'. Fire a \texttt{OOO-LdReq} rule to execute \texttt{S} at time \langle \texttt{ut}_{e}, \texttt{lt}_{e}, \texttt{lt}_{e} \rangle in which \texttt{ut}_{e} = \max(\texttt{ut}_{s}, \texttt{ut}_{a}, \texttt{ut}_{e}, \texttt{ut}_{w}, 1) \cdot \texttt{lt}_{e} is chosen so that \langle \texttt{ut}_{e}, \texttt{lt}_{e} \rangle > \langle \texttt{ut}_{e}, \texttt{lt}_{e} \rangle > \max(\langle \texttt{ut}_{e}, \texttt{lt}_{e} \rangle, \langle \texttt{ut}_{e}, \texttt{lt}_{e} \rangle) \cdot \texttt{lt}_{e} < 1.

Note that \texttt{lt}_{e} always exists, because \langle \texttt{ut}_{e}, \texttt{lt}_{e} \rangle is larger than the time of any existing rule in \texttt{E}'.
that \( I \) reads the value of \( S \) from \( m \), we can deduce the following implications:

1. \( S \) is in \( ccm.m \) when \( L \) is committed from ROB, so \( S \) must have not been overwritten in \( ccm.m \) at time \( \langle ut_e, lt_e \rangle \) (\( \prec \langle ut_e, lt_e \rangle \)), i.e. \( S \) is in \( ooo[i].rob, ooo[i].sb \) or \( ccm.m \) at that time (note that \( S \) is visible to \( ooo[i] \) at that time).

2. If \( i \) is equal to \( j \), then there is no store to \( a \) between \( I \) and \( S \) in processor \( j \); otherwise there is no store to \( a \) older than \( i \) in \( ooo[i].rob \) or \( ooo[i].sb \) ever since \( S \) is written into \( ccm.m \).

3. Any load older than \( I \) in \( ooo[i] \) must read from either \( S \) or some other store which writes \( ccm.m \) before \( S \).

The first and second implications ensure that \( I \) can read the value of \( S \) at time \( \langle ut_e, lt_e \rangle \), and \( I \) will not be killed or forced to re-execute by any older store. The second and third implications ensure that \( I \) will not be killed by any older load, for the same reason used in the previous case where \( I \) reads from \( ps[i].ib \).

\[ I \text{ is executed by reading } ps[i].sb \text{ (i.e. the WMM-D-LdSb rule):} \]

In this case, \( i \) is equal to \( j \), i.e. \( S \) is also from processor \( i \). For the timestamp \( st_s \) of the store buffer entry read in the WMM-D-LdSb rule for \( I \), \( st_s \) is the timestamp computed in the WMM-D-St rule for \( S \), and it is equal to \( ut_e \) according to invariants. Then the computed timestamp of the load value of \( I \) in WMM-D-LdMem rule must be equal to \( ut_e \).

Now we only need to show that \( I \) can read the value of \( S \) in CCM+OOO\(^5\) at time \( \langle ut_e, lt_e \rangle \), and that \( I \) will not be killed or forced to re-execute later. According to invariants and the fact that \( I \) reads the value of \( S \) from \( ps[i].sb \), we can deduce the following implications:

1. \( S \) is in either \( ooo[i].rob \) or \( ooo[i].sb \) at time \( \langle ut_e, lt_e \rangle \) (note that the store address and data of \( S \) have been computed at this time).

2. There is no store to \( a \) between \( I \) and \( S \) in \( ooo[i] \).

3. Any load to \( a \) between \( I \) and \( S \) in \( ooo[i] \) must also get the value of \( S \) as its result.

The first two implications ensure that \( I \) can read the value of \( S \) at time \( \langle ut_e, lt_e \rangle \), and \( I \) will not be killed or forced to re-execute by any older store. The last implication ensures that \( I \) will not be killed by any older load.

\[ \square \]

B. Proof of WMM-S Abstracting HMB+OOO\(^5\)

**Theorem 5.** \( \text{HMB} + \text{OOO}\(^5\) \subseteq \text{WMM-S} \).

**Proof.** We use \( ooo[i] \) to denote processor \( i \) in HMB+OOO\(^5\), and use \( hmb.m \) to denote the monolithic memory in HMB. Section 7.4 in the paper has already stated the invariants and the way to simulate the behavior of HMB+OOO\(^5\) in WMM-S. That section has also proved the correctness in case that a load \( L \) to address \( a \), which reads from a store \( S \), is committed from \( ooo[i].rob \) in HMB+OOO\(^5\), and that \( S \) remains in a segment of HMB at the commit time of \( L \). Here we complete the proof for the remaining cases:

- In case a store \( S \) to address \( a \) is flowed into \( hmb.m \) in the HMB-Flow rule, \( S \) must be closer to the root (i.e. \( hmb.m \)) than any other stores in HMB. According to invariants, in WMM-S, all the copies of \( S \) must be the the oldest stores to \( a \) in their respective store buffers. Thus, WMM-S can fire the WMM-S-DeqSb rule to write \( S \) into the monolithic memory (\( m \)), and all the invariants still hold.

- In case a \( \text{Nm, Reconcile, or St} \) instruction is committed from \( ooo[i].rob \), it is trivial to prove that WMM-S can fire a WMM-Nm, WMM-Rec, or WMM-S-St rule to execute that instruction, and all the invariants still hold.

- In case a Commit fence is committed from \( ooo[i].rob \), the Commit response from HMB ensures that there must not be any store in any segment of HMB which are observed by commits of \( ooo[i] \) at that time. Therefore, \( ps[i].sb \) in WMM-S should also be empty, and the Commit fence can be executed.

- Consider the case that a load \( L \) to address \( a \), which reads from a store \( S \), is committed from \( ooo[i].rob \) in HMB+OOO\(^5\), and that \( S \) is in \( hmb.m \) at the commit time of \( L \). In this case, there cannot be any store to \( a \) in any segment of \( hmb \) which are observed by commits of \( ooo[i] \), because otherwise either the CoRR or CoWR axiom will be violated in HMB+OOO\(^5\). Thus, \( ps[i].sb \) cannot have any store to \( a \) and \( L \) can read the value of \( S \) from \( m \) in WMM-S.

- Consider the case that a load \( L \) to address \( a \), which reads from a store \( S \), is committed from \( ooo[i].rob \) in HMB+OOO\(^3\), and that \( S \) has been overwritten in \( hmb.m \) before the commit of \( L \). In this case, there cannot be any store to \( a \) in any segment of \( hmb \) which are observed by commits of \( ooo[i] \) right before the overwrite of \( S \), because otherwise either the CoRR or CoWR axiom will be violated in HMB+OOO\(^3\). Thus, \( ps[i].sb \) cannot have any store to \( a \) right before \( S \) is overwritten in \( m \) in WMM-S, so the value of \( S \) will be inserted into \( ps[i].ib \). According to the CoRR and CoWR axioms of HMB+OOO\(^3\), during the period between the overwrite and the commit of \( L \), no store to \( a \) can be committed from \( ooo[i].rob \), and no load to \( a \) committed from \( ooo[i].rob \) can read from a store which writes \( hmb.m \) after \( S \). In addition, no Reconcile fence can be committed during that period, otherwise the Reconcile fence will forbid \( L \) from reading across it to get the value of \( S \). Thus, the value of \( S \) will stay in \( ps[i].ib \) until \( L \) is executed by the WMM-Ldbf rule in WMM-S.

\[ \square \]

C. CoRR and CoWR Axioms for Physical Models

In the paper, we have introduced the following axioms (\( L_1, L_2, S_1, S_2 \) denote loads and stores to the same address):

**CoRR** (Read-Read Coherence): \( L_1 \xrightarrow{\text{ps}} L_2 \land S_1 \xrightarrow{\text{rf}} L_1 \land S_2 \xrightarrow{\text{rf}} L_2 \implies S_1 = S_2 \lor S_1 \fallows S_2 \).

**CoWR** (Write-Read Coherence): \( S_2 \xrightarrow{\text{ws}} L_1 \land S_1 \xrightarrow{\text{ps}} L_1 \implies S_1 = S_2 \lor S_1 \fallows S_2 \).

We have used the fact that physical models (i.e. \( \text{CCM+OOO}^{vp} \), \( \text{CCM+OOO}^{bp} \) and \( \text{HMB+OOO}^{3} \)) satisfy these two axioms in the proofs of the relations between \( \text{F}^{E} \) models with physical models. Now we formally prove that these axioms hold for all the physical models. We will directly use \( L_1, L_2, S_1, S_2 \) in the proofs, and all the operations about \( L_1 \) and \( L_2 \) discussed in the proofs are the final operations of \( L_1 \) and \( L_2 \) to get their load results, i.e. \( L_1 \) and \( L_2 \) should not be killed or forced to re-execute afterwards.

C.1 CoRR and CoWR Axioms for CCM+OOO\(^{vp}/OOO\(^{bp}\)

**Lemma 1.** \( \text{CCM+OOO}^{vp} \) satisfies the CoRR axiom.

**Proof.** We assume \( L_1 \) and \( L_2 \) are both from processor \( i \) (\( ooo[i] \)). We do a case analysis on how \( L_1 \) get its final result, i.e. the value of \( S_1 \), and prove that \( S_2 \fallows S_1 \) is impossible in each case.

First consider the case that \( L_1 \) gets its final result via the OOO-LdbfPass rule. In this case, \( S_1 \) is also from \( ooo[i] \). If we have \( S_2 \fallows S_1 \), then \( L_2 \) must get its final result, i.e. the value of \( S_2 \), before the OOO-StEx rule for \( S_1 \) has fired. However, in this case, \( L_2 \) will be killed later when the OOO-StEx rule for \( S_1 \) fires.

Next consider the case that \( L_1 \) reads the value of \( S_1 \) from the monolithic memory of \( \text{CCM} (ccm.m) \). If we have \( S_2 \fallows S_1 \), then \( L_2 \) must get its final result before \( L_1 \) gets the response from CCM, and there should not be any store to \( a \) between \( L_1 \) and \( L_2 \) in \( ooo[i] \).

\[ \square \]
Lemma 2. CCM+OOO\textsuperscript{VP} satisfies the CoWR axiom.

Proof. We assume \( L_1 \) and \( S_1 \) are both from processor \( i \) (ooo\([i]\)). If we have \( S_2 \xrightarrow{co} S_1 \), then \( L_1 \) must get its final result, i.e. the value of \( S_2 \), before the OOO-StEx rule for \( S_1 \) has fired. However, in this case, \( L_1 \) will be killed later when the OOO-StEx rule for \( S_1 \) fires.

Since CCM+OOO\textsuperscript{D} \( \subseteq \) CCM+OOO\textsuperscript{VP}, CCM+OOO\textsuperscript{D} also satisfies the CoRR and CoWR axioms.

C.2 CoRR and CoWR Axioms for HMB+OOO\textsuperscript{S}

Lemma 3. HMB+OOO\textsuperscript{S} satisfies the CoRR axiom.

Proof. We assume \( L_1 \) and \( L_2 \) are both from processor \( i \) (ooo\([i]\)). We do a case analysis on how \( L_1 \) get its final result, i.e. the value of \( S_1 \), and prove that \( S_2 \xrightarrow{co} S_1 \) is impossible in each case.

First consider the case that \( L_1 \) gets its final result via the OOO-LdBypass rule. In this case, \( S_1 \) is also from ooo\([i]\). If we have \( S_2 \xrightarrow{co} S_1 \), then \( L_2 \) must get its final result, i.e. the value of \( S_2 \), before the OOO-StEx rule for \( S_1 \) has fired. However, in this case, \( L_2 \) will be killed later when the OOO-StEx rule for \( S_1 \) fires.

Next consider the case that \( L_1 \) reads the value of \( S_1 \) from HMB. If we have \( S_2 \xrightarrow{co} S_1 \), then before \( L_1 \) issues its request to HMB, \( L_2 \) must either issue its request to HMB or get bypassing from ROB. Furthermore, there should not be any store to \( a \) between \( L_1 \) and \( L_2 \) in ooo\([i]\) (otherwise \( L_2 \) will be killed by the store). However, in this case, when \( L_1 \) issues its request to HMB, it will kill \( L_2 \).

Lemma 4. HMB+OOO\textsuperscript{S} satisfies the CoWR axiom.

Proof. The argument is the same as that for CCM+OOO\textsuperscript{VP}.