Two phase clocked subthreshold adiabatic logic circuit

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Abstract: Energy harvesting is a technique that captures an effective power source. However, the energy obtained from power resources in the environment is insufficient, as only low levels of voltage/current can be generated from it. Therefore, the power consumption of logic circuits for energy harvesting has to be reduced. To achieve low power consumption, we may consider two low-power techniques: the adiabatic logic circuit and the sub-threshold CMOS logic circuit. In this paper, we propose a new CMOS logic circuit that combines the adiabatic logic circuit with the sub-threshold logic circuit. The proposed circuit employs two-phase clock supply voltages that have different amplitude and frequency. We design and implement NAND, XOR, half-adder, full-adder, and $4 \times 4$-bit multiplier circuits using the proposed method. The simulation and the measurement results show that the proposed circuit has an ultra-low-power characteristic compared with the conventional circuit.

Keywords: subthreshold, adiabatic, ultra-low power energy harvesting

Classification: Integrated circuits

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1 Introduction

The need for ultra-low power devices such as wireless sensor, RFID, and medical embedded equipment is increasing. These devices are required to operate for a long time, even though the power supply is limited. The power consumption of a CMOS digital circuit is reduced by power supply voltage scaling. By operating the MOSFET at a lower voltage than the threshold voltage (i.e., in the subthreshold region), it is possible to reduce the power consumption significantly [1]. In recent years, basic circuits such as the adder and advanced processors operating in the subthreshold region have been proposed [2, 3]. The other way of making CMOS digital circuits consume low power is adiabatic logic circuits. The adiabatic logic circuit uses AC power sources instead of DC power sources. Various logic circuits using adiabatic logic have been proposed up to now. They have been shown to achieve greater reduction of energy consumption than the conventional static CMOS logic [4, 5, 6, 7, 8, 9]. However, the proposed circuits operate over the threshold region (i.e., the applied supply voltage is higher than the threshold voltage.)

In recent years, adiabatic logic circuits that operate in the subthreshold region have been reported [10, 11]. In [10], the simulation results of a full adder and an 8 × 8-bit carry-save multiplier designed using the conventional adiabatic logic (2N2N2P [4], SAL [7]) have been shown.

In this paper, we propose a new adiabatic logic circuit that operates in the subthreshold region. We design and implement NAND, XOR, half adder, full adder, and 4 × 4-bit multiplier using a 0.18-μm CMOS process. We simulate operation of the designed circuits by conventional CMOS logic, CMOS logic in the subthreshold region, and the proposed method (i.e., adiabatic logic in the subthreshold region), and we also measure an LSI chip. From the simulation and the measurement results, it is evident that the proposed circuits can reduce power consumption compared with the conventional circuits.

2 Adiabatic logic

The general CMOS inverter consists of a PMOS, NMOS, and load capacitance $C_L$ as shown in Fig. 1. Both PMOS and NMOS transistors can be regarded as an ideal switch, resistor, and capacitance connected in series.

As shown in Fig. 2(a), the conventional CMOS uses DC voltage as the power supply. In Fig. 2(a), when the switch is turned on, the current flows immediately...
through the resistor. As a result, a charge \( Q = C_L V_{DD} \) is stored in the capacitance \( C_L \). The total amount of energy supplied by the power supply in the charging operation is \( E_{supply} = QV_{DD} = C_L V_{DD}^2 \). Half of the energy is consumed by the resistor; the other half is stored in the capacitor. Therefore, the energy consumption of the charging operation is expressed as follows:

\[
E_{charge} = \frac{1}{2} C_L V_{DD}^2. \tag{1}
\]

In the discharge operation, the charge stored in the capacitor is discharged to ground through the NMOS. Therefore, the same amount of energy as in the charging operation is consumed in the discharging operation. From the aforementioned operation, the total amount of energy that the conventional CMOS inverter consumes during the inverter’s charging and discharging operation can be calculated by the following equation:

\[
E_{total} = E_{charge} + E_{discharge}
= \frac{1}{2} C_L V_{DD}^2 + \frac{1}{2} C_L V_{DD}^2
= C_L V_{DD}^2 \tag{2}
\]

On the other hand, the adiabatic logic uses a supply voltage that changes gradually, such as a sinusoidal or ramp voltage. As shown in Fig. 2(b), the current that flows through the resistance is reduced because the potential difference across the resistance is decreased by using the power ramp. In other words, it is possible to reduce the energy consumption of the charging-discharging operation of the inverter by reducing the potential difference across the resistor. When the inverter
is driven by a ramp wave power supply of period $T$ (frequency $f = 1/T$), the power consumption is expressed as $P = E_{\text{total}} = C_L V_{DD}^2 f$. In this case, the energy consumption of the inverter is given by the following equation:

$$E_{\text{adiabatic}} = \xi \frac{RC_L}{T} C_L V_{DD}^2.$$  

where $\xi$ is the shape factor, which depends on the shape of the clock edges (1 for ramp wave voltage, $\pi^2/8$ for sinusoidal voltage). From Equation (3), we consider that the energy consumption of the inverter can be reduced significantly by making the period $T$ of the power supply sufficiently long.

3 Operation of subthreshold region

The $I_d-V_{gs}$ characteristic of an NMOS transistor obtained from simulation results using a 0.18 $\mu$m CMOS process have shown in Fig. 3. The L/W ratio of the transistor is set 1.0 $\mu$m/1.0 $\mu$m. It is seen that the drain current $I_d$ does not flow when the gate-source voltage $V_{gs}$ is lower than the threshold voltage of transistor $V_t$. The region where the gate-source voltage is lower than the threshold voltage is called “subthreshold region”. In the strong inversion region, the major element of the drain current is the drift current, but in the subthreshold region, the major element is the leak current. The drain current in the subthreshold region increases exponentially as the gate-source voltage is increased. In this case the drain current is expressed by the following equation:

$$I_{ds} = I_0 e^{V_{gs}-V_{th}} \frac{1}{n'r},$$  

$$I_0 = \mu C_{ox} \frac{W}{L} (n-1)V_t^2,$$

where $\mu$ is the mobility, $C_{ox}$ is the gate oxide film capacity, $n$ is the subthreshold slope parameter ($n = 1 + C_d/C_{ox}$), $C_d$ is the depletion layer capacitance, $L$ is the channel length, $W$ is the channel width, and $V_T$ is the thermal voltage $V_T = kT/q$ which is equal to 26 mV at 300 K.

In the subthreshold region, the energy consumption of the transistor is very small because the transistor is operated by a very small current in the nanoampere to microampere range. However, the delay time is inversely proportional to the current, so the operation of the circuit becomes slower. Therefore, the subthreshold region operation is thought to desirable for devices that require low power and that do not require high speed.
4 Subthreshold adiabatic logic circuit

4.1 Operation of inverter
We propose an adiabatic logic circuit operating in the subthreshold region [12]. As already mentioned, the subthreshold circuit and adiabatic logic circuit come with a cost: the circuit delay is increased. Further, the characteristics of the subthreshold circuit change owing to variation in the supply voltage, temperature, or process. However, the benefits of reducing the energy consumption by combining the two techniques are significant. Fig. 4 shows the inverter circuit made up of the proposed subthreshold adiabatic logic and the waveforms. The MOS structure is the same as that of the conventional CMOS inverter, but the AC power supply $V_{PC}$ is connected to the top of the PMOS, and $V_{PC}$ is connected to bottom of the NMOS. The body of PMOS and NMOS are connected to ground. The frequency of $V_{PC}$ is twice that of $V_{PC}$, and the amplitude of $V_{PC}$ is set to half that of $V_{PC}$ as shown in Fig. 4(b). Switching of the input signal is performed when $V_{PC}$ and $V_{PC}$ are at the same potential. When the IN node is “High”, M1 is turned off and M2 is turned on, so the voltage of $V_{PC}$ is outputted to the OUT node as “Low”. On the other hand, when the IN node is “Low”, M1 is turned on and M2 is turned off, so voltage of $V_{PC}$ is outputted to OUT node as “High”.

4.2 Comparison with conventional adiabatic logic
We design the inverter circuit using the conventional adiabatic logic, which are 2N2N2P [4], ECRL [5], PFAL [6], and SAL [7]. We simulate the conventional adiabatic logic inverters and the proposed inverter, which are operated in the subthreshold region using SPICE. Fig. 5 shows a comparison of the energy consumption. We find that the proposed inverter has a lower energy consumption than conventional adiabatic logic inverters in subthreshold region operation.

5 Fundamental circuits
We simulated NAND, XOR, half adder, and full adder circuits by SPICE using a 0.18 µm CMOS standard process, and then we measured an implemented LSI chip to examine the operation and energy consumption of subthreshold adiabatic logic. The transistor size of the all MOSs is set to $L/W = 1.0 \mu m / 1.0 \mu m$. We also simulated and measured conventional static CMOS and subthreshold CMOS to compare with the proposed circuit.
5.1 Simulation results

The circuit diagrams of NAND, XOR, half adder, and full adder circuits are shown in Figs. 6(a)–9(a). Each of the waveforms operated by the proposed method is shown in Figs. 6(b)–9(b). In these simulations, the operating frequency is 1 kHz. We found that the proposed circuits exhibited good functionality, and the energy consumption of the proposed circuits is lower than that of the conventional circuits.

The comparison of the energy consumption per cycle is shown in Fig. 10. The energy consumption is calculated from the following equation:

\[ E = \int (V_{PC}(t)I_{PC}(t) + V_{\overline{PC}}(t)I_{\overline{PC}}(t))dt \]  \hspace{1cm} (6)

5.2 Measurement results of LSI

The LSI chip measurement system in this study is depicted in Fig. 11. The input signals and supply voltages are generated by a function generator. The input and
The energy consumption per cycle is given by the following equation:

$$E = \frac{I_{vpc} \times V_{P_{\text{peak}}}}{f},$$

(7)

where $I_{vpc}$ is the current value obtained from a current meter, $V_{P_{\text{peak}}}$ is the supply voltage, and $f$ is the operating frequency. The waveforms obtained from LSI measurement are shown in Figs. 6(c)–9(c). A comparison of the energy consumption of each circuit is shown in Fig. 12. The proposed circuits have lower energy consumption compared with the conventional circuits. The energy consumption values of the measurement results are higher than those of the simulation results. We attribute these results to the parasitic parameter of the cable used for the measurement.

Table 1. The parameters of power supply voltages.

| Voltage | static CMOS | sub-$V_I$ CMOS | 2PC2AL [13] | proposed |
|---------|-------------|----------------|-------------|----------|
| $V_{PC}$ | 1.8[V]DC | 0.6[V]DC | 0.3–0.6[V]AC | 0–0.6[V]AC |
| $V_{PC}$ | GND | GND | 0–0.3[V]AC | 0–0.3[V]AC |
| $V_{bp}$ | 1.8[V]DC | GND | GND | GND |
| $V_{bn}$ | GND | GND | GND | GND |
| $V_{th}$ | 0.4[V] | 0.4[V] | 0.4[V] | 0.4[V] |
We designed a 4 x 4-bit multiplier as application circuit. The post-layout simulation results and LSI measurement results when the circuits were operated by conventional CMOS, subthreshold CMOS, conventional adiabatic logic (2PC2AL [13]), and the proposed method are shown.

Fig. 8. Half adder.

Fig. 9. Full adder.
Fig. 10. Comparison of energy consumption obtained from simulation result.

Fig. 11. System of LSI chip measurement.

Fig. 12. Comparison of energy consumption obtained from measurement result of LSI.
6.1 Simulation results

Fig. 13(a) shows the $4 \times C2^4$-bit multiplier circuit diagram. The multiplier consists of 16 ANDs, 4 half adders, and 6 full adders. $a_0$–$a_3$ are the multiplicands, $b_0$–$b_3$ are the multipliers, and $p_0$–$p_7$ are the output nodes. The waveform at 1 kHz operation is shown in Fig. 13(a). We found that the operation functionality is good. Fig. 13(c) shows a comparison of the energy consumptions of the $4 \times C2^4$-bit multiplier. Each of power supply voltage parameters are shown in Table I. $V_{bp}$ is the body bias voltage of PMOS transistor and $V_{bn}$ is the body bias voltage of NMOS transistor. The proposed multiplier has the lowest energy consumption over all frequencies. The energy consumption of the proposed is 99.4% lower than that of the conventional static CMOS, 85.2% lower than that of the subthreshold CMOS, and 29.9% lower than that of the 2PC2AL.

6.2 Measurement results of LSI chip

Fig. 14(a) shows a micrograph of the implemented $4 \times C2^4$-bit multiplier. The area of the multiplier is $193 \times 123.7 \, \mu m^2$. The waveform at 1 kHz operation is shown in Fig. 14(b). The correct multiplication results have been outputted. The comparison of energy consumption per cycle is shown in Fig. 14(c). The red lines are the energy consumption obtained from measurement. The measurement results show inferior performance compared with the simulation results because the measurement results include a parasitic effect of measurement cable or substrate. To confirm the parasitic effect of cable, we simulated $4 \times C2^4$-bit multiplier which was considered the parasitic effect of measurement cable. Fig. 15 shows the simulated circuit diagram. We connected 30 kΩ resistance and 20 pF capacitance to power supply in
parallel as the parasitic effect. In Fig. 13(c), the black lines are the energy consumption of the circuit which was added the parasitic effect of cable. The simulation results were consistent to measurement results. Therefore we estimate that the measurement results include the power dissipation by the parasitic effect of cable. The blue lines indicate the energy consumption of LSI chip that excepted the energy dissipation of the parasitic effect of cable. The proposed multiplier has the lowest energy consumption.

7 Conclusion

We have proposed a new adiabatic logic circuit operating in the subthreshold region. We found that the proposed circuits have significantly lower energy
consumption compared with the conventional CMOS and subthreshold CMOS from results of simulation and measurement of fundamental circuits and a $4 \times 4$-bit multiplier.

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