1/f Noise Reduction using In-Pixel Chopping in CMOS Image Sensor

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Abstract—In this paper, an in-pixel chopping technique to reduce the low-frequency or 1/f noise of the source follower (SF) transistor in active pixel sensor (APS) is presented. The SF low-frequency noise is modulated at higher frequencies through chopping, implemented inside the pixel, and in later stage eliminated using low-pass filtering. To implement the chopping, the conventional 3T APS architecture is modified, with only one additional transistor of minimum size per pixel. Reduction in the noise also enhances the dynamic range (DR) of the image sensor. The test circuit is fabricated in UMC 0.18 μm standard CMOS technology. The measured results show a reduction of 1/f noise by approximately 22 dB for 50 MHz chopping frequency (fch).

Index Terms—Low-frequency noise, 1/f noise, chopper amplifier, CMOS image sensors, dynamic range.

I. INTRODUCTION

In the present era, CMOS image sensors are being extensively used in digital imaging systems. High dynamic range (DR) is one of the primary performance defining parameters for a CMOS image sensor. The dynamic range is limited by the output swing and high noise. The primary sources of noise in an active pixel sensor (APS) of a CMOS imager are the thermal noise from the switches and the low-frequency noise from the source follower (SF). The thermal noise from reset switch of the pixel can efficiently be reduced using correlated double sampling (CDS). The low-frequency or 1/f noise of the SF remains as a major source of noise in an active pixel.

The 1/f noise results from the random telegraph signal (RTS) which causes the discrete fluctuation of the conducting current or the threshold voltage and eventually produces the blinking output behavior of the pixel. The image quality is severely affected by this random behavior as the blinking is very visible to human eyes. To reduce the 1/f noise a pMOS SF transistor is used in [1]. The use of pMOS transistor reduces the fill-factor of the pixel. In [2] a buried channel SF while, in [3] a thin oxide pMOS transistor is used to reduce the 1/f noise. The 1/f noise reduction technique in [2] and [3] needs process modifications and thus, would increase the cost. The cycling of a MOS transistor between strong inversion and accumulation also reduces 1/f noise [4]–[6].

Chopping [7] is used for 1/f noise reduction, in which the low-frequency noise is modulated to the chopping frequency (fch) far beyond the frequency band of interest. Chopping needs extra switches and would hamper the fill-factor of the pixel and thus has never been used in a pixel. In this work, a novel technique is presented to implement chopping inside a conventional 3T pixel. The basic building block of the proposed in-pixel chopping is shown in Fig. 1. The photodiode (PD) output signal is modulated to the chopping frequency (fch) using the first chopper (CH I) before being buffered by the SF. The output of the SF is fed to the input of the amplifier stage I (AMP I). The output of the AMP I is composed of the amplified modulated PD signal, amplified low-frequency noise from the SF, and the noise and output offset of the AMP I. The output of the AMP I is chopped again using the second chopper (CH II). The AMP I and the CH II are placed in the column and does not affect the fill-factor of the pixel. The CH II demodulates the PD signal to its original baseband frequency whereas, modulates the low-frequency noise of the SF and AMP I, and amplifier offset voltage to fch. After CH II the signals are further amplified by the amplifier stage II (AMP II). The output of the AMP II is fed back to the other input of CH I to complete the closed loop unity gain feedback configuration. A low-pass filter (LPF) followed by CH II suppresses the up-modulated offset and 1/f noise and also blocks the spikes in the output at the frequency fch, generated due to chopping action.

The modified pixel read-out helps in achieving the functionality as well as a reduction in the low-frequency noise. An additional minimum sized transistor is used in-pixel as compared to 3T pixel. To compensate the fill-factor a minimum sized SF is used, the noise of which is reduced using in-pixel chopping. The low-frequency noise power reduces by 22 dB, as compared to a conventional 3T APS without chopping. The rest of the paper is organized as follows: in-pixel chopping implementation is described in section II simulation and experimental results are presented in section III and the paper is concluded in section IV.

II. SYSTEM DESIGN

The circuit diagram for the in-pixel chopping in active pixel sensor of a CMOS imager is shown in Fig. 2. The two pixels A and B consist of photodiodes PD_A, PD_B, chopper switches S1, S3 (of CH I), select switches Sel_A, Sel_B, and source followers SF_A, SF_B. The remaining two switches S2, S4 of CH I, AMP I, CH II (switches S5–S8), AMP II, and a low-pass filter are...
placed in column level circuits. At the onset, the photodiodes of Pixel$_A$ and Pixel$_B$ are reset to $V_{ref}$ using RST switch. Light is then integrated on the photodiodes. After the integration time, the photodiode output signals $V_{PD,A}$ and $V_{PD,B}$ are modulated to chopping frequency $f_{ch}$ using switches $S_1$-$S_4$ of CH I. The non-overlapping clock signals $\phi$ and $\phi'$ run at the fundamental chopping frequency $f_{ch}$. During readout, Pixel$_A$ and Pixel$_B$ are selected together using the select signal SEL at the input of switches Sel$_A$ and Sel$_B$. The row decoder of the image sensor selects two rows at a time for simultaneous selection of two adjacent pixels in the column. The SF output of Pixel$_A$ and Pixel$_B$ are amplified using AMP I. The AMP I is realized using a folded cascode differential input differential output amplifier.

The clock signal $\phi$ turns the switches $S_1$, $S_2$, $S_3$, and $S_5$, $S_6$, $S_7$ ON for a time interval $t_1$ and the clock signal $\phi'$ turns the switches $S_2$, $S_3$, and $S_6$, $S_7$ ON for $t_2$ ($t_1$ and $t_2$ are non-overlapping and equal time intervals). After modulation of the photodiode signals $V_{PD,A}$ and $V_{PD,B}$ through CH I and buffered by the SF, the input of the AMP I can be given as

$$V_{SF,A} = V_{PD,A}(t_1) + V_{out}(t_2) + N_{sf,A},$$  
$$V_{SF,B} = V_{PD,B}(t_2) + V_{out}(t_1) + N_{sf,B},$$

where $N_{sf,A}$ and $N_{sf,B}$ are the low-frequency noise from SF$_A$ and SF$_B$, respectively. The notation of $V_{PD,A}(t_1)$ is chosen to denote the signal $V_{PD,A}$ during $t_1$ time interval and also applicable to similar terms. In next stage the output of AMP I is chopped using CH II, which demodulates the photodiode signal to the baseband and modulates the offset and low-frequency noise to $f_{ch}$. CH II consists of switches $S_5$, $S_6$ operated on same non-overlapping clocks $\phi$ and $\phi'$. The differential output of the CH II is amplified by single-ended difference amplifier AMP II. The output of AMP II is fed back to the Pixel$_A$ and Pixel$_B$ to close the loop. Thus, AMP I and II both are required to form a closed loop unity gain system.

If AMP I and AMP II has a voltage gain of $A_1$ and $A_2$, offset of $V_{off1}$ and $V_{off2}$, low-frequency noise of $N_{Am1}$ and $N_{Am2}$, respectively, the output signal $V_{out}$ is expressed as

$$V_{out} = [V_{PD,A}(t_1) + V_{PD,B}(t_2)] + [N_{sf,A}(t_1) - N_{sf,A}(t_2)]$$
$$- [N_{sf,B}(t_1) - N_{sf,B}(t_2)] + N_{Am1}(t_1) - N_{Am1}(t_2)$$
$$+ V_{off1}(t_1) - V_{off1}(t_2) + \frac{N_2 + V_{off2}}{A_1}$$

(2)

If the small signal voltage gain values $A_1$ and $A_2$ are very high, then only the photodiode signals $V_{PD,A}$ and $V_{PD,B}$ along with $1/f$ noise from the source followers dominate and the output signal $V_{out}$ can be simplified as

$$V_{out} \approx [V_{PD,A}(t_1) + V_{PD,B}(t_2)] + [N_{sf,A}(t_1) - N_{sf,B}(t_2)] - [N_{sf,B}(t_1) - N_{sf,B}(t_2)].$$

(3)

In (2) and (3), it is assumed that the chopping frequency is much higher than the low-frequency noise corner frequency and the noise pairs like $N_{sf,A}(t_1)$ and $N_{sf,B}(t_2)$ are correlated due to high $f_{ch}$.

To suppress the overall input referred noise and offset at the output (from the amplifier stages), a two-stage high gain amplifier is designed for column readout circuit. The amplifier system has 20-MHz unity gain-bandwidth with a phase margin of $65^0$ and maximum power consumption of $200\ \mu$W. The first stage of the opamp is a differential input/differential output folded cascode amplifier (AMP I with small signal voltage gain of 68 dB), which is followed by a difference amplifier with a single-ended output (AMP II with small signal voltage gain of 40 dB) to achieve an overall small signal voltage gain of 108 dB.

The output signal $V_{out}$ is continuous and composed of Pixel$_A$ output for time duration $t_1$ and Pixel$_B$ output for time duration $t_2$, periodically. The switches used for chopping
introduces ripples at the output. These ripples are generated due to clock feed-through of the overlapping capacitance present between drain and gate of the switching transistors. A switched capacitor low-pass filter is used to block the ripples present in the output signal [8].

As the dynamic range of a conventional APS is limited by the noise level, the technique also enhances the DR of the pixel. The photodiode signal gets buffered through a chopper amplifier including SF, high gain amplifier stage I and II (configured in closed loop with unity gain) and the final output is fed back to one of the inputs of first chopper CH I. Hence, the continuous output of the closed-loop chopper amplifier is virtually short with the photodiode output node. The high gain of the amplifier (108 dB) make the output follow the photodiode node linearly for a wide range of light integration, increasing the the output swing and dynamic range.

The read-out timing diagram for the in-pixel chopping operation and the output waveforms of the critical nodes are shown in Fig. 3(a)-(d). The read-out is based on conventional rolling shutter mode as in 3T pixel. The conventional and proposed read-out modes are shown in Fig. 3(a) and (b), respectively. However, in the proposed architecture instead of a single row, two adjacent rows, Row\textsubscript{X,A} and Row\textsubscript{X,B} (X is used to denote the row number, for example, Row\textsubscript{1,A} and Row\textsubscript{1,B}) are selected together for readout. Charge integration on photodiode, charge to voltage conversion, chopping/de-chopping of the photodiode signal, signal due to light/reset level sample and hold, double sampling (DS) and low-frequency noise filtering are carried out on the pixel pairs (i.e. Pixel\textsubscript{0,A}-Pixel\textsubscript{0,B}, Pixel\textsubscript{1,A}-Pixel\textsubscript{1,B}, Pixel\textsubscript{2,A}-Pixel\textsubscript{2,B}... ) for Row\textsubscript{X,A} and Row\textsubscript{X,B} together. The timing diagram of the in-pixel chopping architecture is shown in Fig. 3(c) and (d).

The double sampling circuit is modified to sample and hold the reset and signal of the pixel pair of adjacent rows, as shown in Fig. 3. The reset signal of Pixel\textsubscript{A} and Pixel\textsubscript{B} of Row\textsubscript{X,A} and Row\textsubscript{X,B} are sampled on capacitors C\textsubscript{RST,A} and C\textsubscript{RST,B}, while the signal after a variable integration period is sampled on capacitors C\textsubscript{SG,A} and C\textsubscript{SG,B}, respectively. Switches S/H\textsubscript{RST,A} and S/H\textsubscript{RST,B} are ON for repetitive and non-overlapping time intervals t\textsubscript{1} and t\textsubscript{2}, respectively, sampling the reset levels, while, switch S/H\textsubscript{SG,A} and S/H\textsubscript{SG,B} are ON similarly, sampling the output signals. The output of all pixels of Row\textsubscript{A} and Row\textsubscript{B} are then, sequentially read by turning the switch Read\textsubscript{Row,A} and Read\textsubscript{Row,B} ON, respectively.

III. SIMULATION AND MEASUREMENT RESULTS

The post-layout noise PSD simulation results, shown in Fig. 5 (a) are generated by the periodic steady state (PSS) and Pnoise analysis in Cadence IC-615 using Star-Hspice 49 models for UMC 0.18\textmu m process. The output noise power (integrated in the frequency band from 1 Hz to 10 kHz) without chopping is -65.01 dB. Whereas, with chopping the integrated noise power reduces to -93.55 dB, -94.28 dB, -99.91 dB, and -100.27 dB for f\textsubscript{ch} equal to 800 kHz, 1 MHz, 2 MHz, and 5 MHz, respectively for an input signal of 50 kHz.
The in-pixel chopping architecture is fabricated in 0.18 μm 1P6M standard CMOS process and the microchip photograph is shown in Fig. 4(a). The design under test (DUT) consists of two-pixels with the chopper amplifier. The test pixel is without photodiode and the input signal for the SF is a replica of photodiode output signal, generated from a function generator during measurements. The measurement setup is shown in Fig. 4(b) and is similar to that reported in [6]. The measured noise PSD of the DUT for varying frequency span of 100 Hz, 800 Hz, and 10 kHz is shown in Fig. 5 (b), (c), and (d), respectively. For each span, the noise PSD of the pixel is shown, without chopping and with in-pixel chopping for \( f_{ch} \) equal to 800 kHz, 1 MHz, 2 MHz, and 5 MHz. To improve the measurement accuracy, each noise PSD curve is plotted after taking an RMS average of 1000 measured samples.

The in-pixel chopping reduces the \( 1/f \) noise for all \( f_{ch} \) greater than twice the fundamental frequency of the input signal (50 kHz) during measurements. The \( 1/f \) corner frequency which is around 10 kHz without chopping is shifted to below 1 kHz (around at 800 Hz) with chopping. The integrated noise power from 1 Hz to 10 kHz without chopping is -75.74 dB (163.23 \( \mu V_{RMS} \)), whereas with chopping the integrated noise power reduces to -95.90 dB (16.023 \( \mu V_{RMS} \)), -96.15 dB (15.53 \( \mu V_{RMS} \)), -97.36 dB (13.55 \( \mu V_{RMS} \)), and -98.05 dB (12.51 \( \mu V_{RMS} \)) for 800 kHz, 1 MHz, 2 MHz, and 5 MHz, respectively. This shows the noise reduction of 20.16 dB, 20.41 dB, 21.62 dB, and 22.31 dB for chopping frequencies of 800 kHz, 1 MHz, 2 MHz, and 5 MHz, respectively.

The low-frequency noise reduction using in-pixel chopping is compared with recently reported noise performances for CMOS imager in Table I. The integrated RMS noise for 1 Hz to 10 kHz frequency band, at the output of the SF without chopping is 163.23 \( \mu V_{RMS} \), which gets reduced to 12.5 \( \mu V_{RMS} \) using in-pixel chopping for 5 MHz chopping frequency. As observed from the Table I the proposed work results in the lowest noise as compared to other methods. The use of buried channel nMOS and thin oxide pMOS SF needs process modifications. However, the proposed method uses the conventional fabrication process. Further use of pMOS SF reduces the pixel fill-factor in [6]. The proposed in-pixel chopping uses an nMOS SF thus, does not compromise much with the fill-factor of the pixel.

**TABLE I**  
**Performance comparison of the noise in CMOS imagers**

| Technique                  | Noise [\( \mu V_{RMS} \)] | Reference          |
|---------------------------|-----------------------------|--------------------|
| pMOS in-pixel Amplifier   | 258                         | ISSCC’11 [1]       |
| Buried Channel nMOS SF:   | 31.5                        | ISSCC’12 [2]       |
| Multiple Sampling with SSADC | 74                          | TED’16 [3]         |
| Thin Oxide pMOS SF        | 12.5                        | This Work          |

The in-pixel chopping is applied to the conventional 3T pixel which reduces the low-frequency noise of the source follower. A reduction in the integrated noise power of 22 dB with 5 MHz chopping frequency, is obtained. The reduction in the low-frequency noise improves the dynamic range of the image sensor and hence, can be used to improve the quality of the image. The reduction in the fill-factor due to an extra in-pixel switch can partially be compensated by choosing a minimum size source follower. The noise of the minimum size source follower is reduced using in-pixel chopping.

**REFERENCES**

[1] C. Lotto, P. Seitz, and T. Baechler, “A sub-electron readout noise CMOS image sensor with pixel-level open-loop voltage amplification,” in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC), 402–404, Feb. 2011.

[2] Y. Chen, Y. Xu, Y. Chae, A. Mierop, X. Wang, and A. Theuwissen, “A 0.7\( \mu V_{rms} \) temporal-readout-noise CMOS image sensor for low-light-level imaging,” in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC), pp. 384–386, Feb. 2012.

[3] A. Boukhayma, A. Peizerat, and C. C. Enz, “Temporal Readout Noise Analysis and Reduction Techniques for Low-Light CMOS Image Sensors”, IEEE Trans. on Elect. Devices, vol. 63, no. 1, pp. 384–386, Jan. 2016.

[4] I. Bloom and Y. Nemirowsky, “1/f noise reduction of metal-oxide-semiconductor transistors by cycling from inversion to accumulation,” Appl. Phys. Lett., vol. 58, no. 15, pp. 1664-1666, Apr. 1991.

[5] S. L. J. Gierkink, E. Klumperink, A. van der Wel, G. Hoogzaad, E. V. Tuijl, and B. Nauta, “Intrinsic 1/f device noise reduction and its effect on phase noise in CMOS ring oscillators,” IEEE J. Solid-State Circ., vol. 35, no. 7, pp. 1022-1022, Jul. 1999.

[6] K. Jainwal, M. Sarkar, and K. Shah, “Analysis and Validation of Low-Frequency Noise Reduction in MOSFET Circuits using Variable Duty Cycle Switched Biasing,” IEEE J. Electron Devices Society, vol. 6, pp. 420–431, Feb. 2018.

[7] C. C. Enz, E. A. Vintoz, and F. Krümmenacher, “A CMOS chopper amplifier,” IEEE J. Solid-State Circ., vol. 22, pp. 335-342, June 1987.

[8] Y. P. Tsividis, “Integrated continuous-time filter design-An overview,” IEEE J. Solid-State Circ., vol. 29, pp. 166-176, Mar. 1994.

**IV. CONCLUSION**
Fig. 5. (a) Post layout $1/f$ noise PSD Simulation (PSS + PNoise) results (using Cadence simulator tool - Spectre) with and without in-pixel chopping, Measured low-frequency noise PSD (Fig. (b), (c), and (d)) for variable chopping frequencies $f_{ch}$ (from 800 kHz to 5 MHz) and sampling frequency span of (b) 100 Hz, (c) 800 Hz, and (d) 100 kHz. [The input signal fundamental frequency for all results is 50 kHz].