Migrating CUDA to oneAPI: A Smith-Waterman Case Study

Manuel Costanzo\textsuperscript{1}, Enzo Rucci\textsuperscript{1}, Carlos Garcia Sanchez\textsuperscript{2}, Marcelo Naiouf\textsuperscript{1}, and Manuel Prieto-Matias\textsuperscript{2}

\textsuperscript{1}III-LIDI, Facultad de Informática, Universidad Nacional de La Plata - CIC, La Plata, Buenos Aires, Argentina, \{mcostanzo,erucci,mnaiouf\}@lidi.info.unlp.edu.ar
\textsuperscript{2}Dpto. Arquitectura de Computadores y Automática, Universidad Complutense de Madrid. Madrid (28040), España, \{garsanca,mpmatias\}@dacya.ucm.es

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Abstract

To face the programming challenges related to heterogeneous computing, Intel recently introduced oneAPI, a new programming environment that allows code developed in Data Parallel C++ (DPC++) language to be run on different devices such as CPUs, GPUs, FPGAs, among others. To tackle CUDA-based legacy codes, oneAPI provides a compatibility tool (\texttt{dpct}) that facilitates the migration to DPC++. Due to the large amount of existing CUDA-based software in the bioinformatics context, this paper presents our experiences porting \textit{SW#db}, a well-known sequence alignment tool, to DPC++ using \texttt{dpct}. From the experimental work, it was possible to prove the usefulness of \texttt{dpct} for \textit{SW#db} code migration and the cross-GPU vendor, cross-architecture portability of the migrated DPC++ code. In addition, the performance results showed that the migrated DPC++ code reports similar efficiency rates to its CUDA-native counterpart or even better in some tests (approximately +5%).

Keywords— oneAPI SYCL GPU CUDA Bioinformatics

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1 Introduction

At present, heterogeneous computing and massively parallel architectures have proven to be an effective strategy for maximizing the performance and energy efficiency of computing systems [20]. That is the main reason why the programmers typically rely on a variety of hardware, like CPU, GPU, FPGAs, and other kinds of accelerators. This raises the need for specialized libraries, tools, and APIs that increase the programming cost and complexity, and complicate future code maintenance and extension.

On the one hand, Khronos Group has proposed SYCL [1], an open standard, to face some of the programming issues related to heterogeneous computing. Although SYCL shares some characteristics with OpenCL (such as being royalty-free and cross-platform), it can actually be seen as an improved, high-level version of the latter. SYCL is an abstraction layer that enables code for heterogeneous systems to be written using standard, single-source C++ host code including accelerated code expressed as functions or kernels. SYCL implementations are often based on OpenCL, but also have the flexibility to use other backends like CUDA or OpenMP. Furthermore, SYCL features asynchronous task graphs, buffers defining location-independent storage, interoperability with OpenCL, among other characteristics oriented to increase productivity [18, 6].

On the other hand, Intel recently introduced the oneAPI programming ecosystem that provides a unified programming model for a wide range of hardware architectures. The core of the oneAPI environment is a simplified language to express parallelism in heterogeneous platforms, named Data Parallel C++ (DPC++), which can be summarized as C++ with SYCL. In addition, oneAPI also comprises a runtime, a set of domain-focused libraries and supporting tools [1].

In this scenario, GPUs can be considered the dominant accelerator and CUDA is the most popular programming language for them nowadays [14]. Bioinformatics and Computational Biology are some of the communities that have been exploiting GPUs for more than two decades [12]. Lots of GPU implementations can be found in sequence alignment [5], molecular dynamics [9], molecular docking [13], prediction and searching of molecular structures [11], among other application areas. Even though some applications achieve a better performance with CUDA, their portability to other architectures is strongly restricted due to their proprietary nature.

To tackle CUDA-based legacy codes, oneAPI provides a compatibility tool (dpct) that facilitates the migration to the SYCL-based DPC++ programming language. A few preliminary studies assessing dpct usefulness can be found in simulation [1], math [19, 2], and cryptography [10]; however, to the best of our knowledge, no study assess their utility in Bioinformatics arena. In this paper, we present our experiences porting a biological software tool to DPC++ using dpct. In particular, we have selected SW#db [8]: a CUDA-based, memory-efficient implementation of the Smith-Waterman (SW) algorithm, that can be used either as a stand-alone application or a library. Our contributions are:

- An analysis of the dpct effectiveness for the CUDA-based SW#db migration, including a detailed summary of the porting steps that required manual modifications.
- An analysis of the DPC++ code’s portability, considering different target platforms and vendors (Intel CPUs and GPUs; NVIDIA GPUs).
- A comparison of the performance on different hardware architectures (Intel CPUs and GPUs; NVIDIA GPUs).

https://www.khronos.org/registry/SYCL/specs/sycl-2020/pdf/sycl-2020.pdf
This work can be considered the starting point for a more exhaustive evaluation exploration of CUDA-based biological tool migration to oneAPI. The remaining sections of this article are organized as follows: in Section 2, the background is presented. Next, in Section 3 the migration process is described, and in Section 4 the experimental work carried out is detailed and the results obtained are analyzed. Finally, in Section 5 the conclusions and possible lines of future work are presented.

2 Background

2.1 The oneAPI Programming Ecosystem

oneAPI is a unified programming model for application development that can be used on different architectures, such as CPUs, GPUs, and even FPGAs. oneAPI seeks to facilitate the hard task of developing applications on a different set of hardware. Using oneAPI, the coding task can be performed at various levels: (1) invoking one of the multiple optimized libraries (oneMKL, oneDAL, oneVPL, etc) that takes advantage of offloading technology in a transparent way to the programmer, or (2) direct programming using the SYCL heterogeneous programming language supported by the Data Parallel C++ (DPC++) language. The DPC++ programming language (supported by Intel’s dpcpp compiler) combines the C++ language with SYCL, allowing the same source code to be compiled and executed across different accelerators.

oneAPI comprises several programming tools and one of the most interesting considering code migration is a compatibility one named as dpct. This tool converts applications written in the proprietary CUDA language to SYCL. According to Intel, this tool automatically migrates 80%-90% of the original CUDA code to SYCL. In addition, regarding non-ported code, dpct inlines comments (through warning messages) that help the programmer to migrate and tune the final DPC++ code. [4].

The migration process consists of 3 stages:

1. Run the dpct tool that performs the automatic code migration.
2. Modify the migrated code attending all dpct warnings to reach a first, executable version following the diagnostics reference.
3. Verify the correctness and efficiency of the resulting oneAPI program and make the necessary modifications accordingly.

2.2 Smith-Waterman Algorithm

This algorithm was proposed by Smith and Waterman [17] to obtain the optimal local alignment between two biological sequences. SW employs a dynamic programming approach and presents quadratic time and space complexities. Furthermore, it has been used as the basis for many subsequent algorithms and is often employed as a benchmark when comparing different alignment techniques [5].

The SW algorithm can be used to compute (a) pairwise alignments (one-to-one) or (b) database similarity searches (one-to-many). Both cases have been parallelized in the literature. In case (a), a single SW matrix is calculated and all Processing Elements (PEs) work collaboratively (intra-task parallelism). Due to inherent data dependencies, neighbour PEs communicate in order to exchange border elements. In case (b), multiple SW matrices are calculated simultaneously without communication between the PEs (inter-task parallelism) [3].

[4] Diagnostics Reference of Intel® DPC++ Compatibility Tool available at: https://software.intel.com/content/www/us/en/develop/documentation/intel-dpcpp-compatibility-tool-user-guide/top/diagnostics-reference.html

[5] https://www.oneapi.com/
2.3 **SW#**

SW# is a tool to compute biological sequence alignments that can be used as an API-based library or as a standalone command-line executable. It is considered a versatile tool since it works with both protein and DNA sequences, being able to compute pairwise alignments as well as database similarity searches.

SW#db is the package for fast exact similarity searches, which works by simultaneously utilizing CPU and GPU(s). The GPU part is based on CUDA and follows both inter-task and intra-task parallelism approaches (depending on the sequence length). On its behalf, CPU just exploits inter-task parallelism through multithreading and SIMD instructions. Through dynamic work distribution and dynamic communication between the CPU-GPU, SW#db significantly reduces execution time.

3 **Implementation**

3.1 **Differences between CUDA and DPC++**

Before migrating a code from CUDA to oneAPI, some differences should be considered.

3.1.1 **Memory model:**

on the one hand, CUDA provides two different types of memory model:

1. Conventional model: it is mandatory to specify all memory operations between the CPU and GPU.
2. Unified Memory (UM): introduced in CUDA 6, this model creates a shared memory pool between the CPU and GPU, where both access the data through pointers in a transparent manner to the programmer.

On the other hand, oneAPI offers three abstractions for managing memory:

1. Buffers: they are data abstractions that represent one or more objects of a given C++ language type. Buffers represent data objects rather than specific memory addresses, so the same buffer can be allocated to several different memory locations on different devices, or even on the same device, for performance reasons.
2. Images: they are a special type of buffer created especially for image processing. They include support for special image formats, image reading through sampling objects, among others.
3. Unified Shared Memory (USM): it consists of creating a unified virtual memory space where pointers are shared between the CPU and the device (similar to the CUDA UM).

3.1.2 **Verbosity:**

in DPC++, all variables used within a kernel must be declared and explicitly sent to the functions, as well as other aspects that in CUDA are not mandatory. On the contrary, in CUDA it is possible to indicate the variables that you want to send to the device and implicitly use them in the kernels. These issues may cause the oneAPI code to be longer than its CUDA counterpart.

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4In particular, it makes use of the OPAL library for the CPU part: [https://github.com/Martinsos/opal](https://github.com/Martinsos/opal)
3.2 Migrating CUDA Codes to DPC++

As a general, dpct is not able to generate a fully functional DPC++ code. Thus, it is required to perform hand-tunned adaptations. However, the dpct tool reports list of warnings which facilitates successful refactoring.

3.2.1 Warnings generated by dpct:

These warnings vary among simple recommendations (i.e. to improve the performance) to more complex issues, such as fragments code not successfully migrated. In this section, we will detail the messages reported by the migration dpct tool when porting the SW# and the manual adaptation made to obtain the final DPC++ code.

DPCT1003: Migrated API does not return error code. (∗, 0) is inserted. You may need to rewrite this code.

DPCT1009: SYCL uses exceptions to report errors and does not use the error codes. The original code was commented out and a warning string was inserted. You need to rewrite this code.

Both warnings occur when using native CUDA functions, such as CUDA error codes (Fig. 1a). Since dpct cannot translate them, it modifies the code to still keep it functional (Fig. 1b). Generally, this technique is used when exchanging data with the device. Figs. 1a and 1b show memory allocations on the GPU using CUDA and oneAPI, respectively. By default, dpct tries to use the USM model because it produces less volume of code and allows dpct to support more memory-related APIs.

DPCT1005: The SYCL device version is different from CUDA Compute Compatibility. You may need to rewrite this code.

This problem is related to the previous one and appears when querying for intrinsic CUDA attributes. While dpct can obtain information from the GPU, such as the number of registers, maximum memory size, among others, some CUDA-proprietary attributes (e.g. CUDA driver information) are not translatable. Fig. 2a shows that, in the original code, the number of CUDA blocks and threads depends on the driver version. Fig. 2b presents the migrated code, showing that it is possible to obtain information about GPU properties, with the exception of those specific to CUDA.

Figure 1: CUDA SAFE CALL example

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https://docs.oneapi.io/versions/latest/dpcpp iface/device.html
cudaDeviceProp properties;
cudaGetDeviceProperties(&properties, card);
int threads;
int blocks;
if (properties.major < 2) {
    threads = THREADS_SM1;
    blocks = BLOCKS_SM1;
} else {
    threads = THREADS_SM2;
    blocks = BLOCKS_SM2;
}

(a) CUDA

dpct::device_info properties;
dpct::dev_mgr::instance().get_device(card).get_device_info(properties);
int threads;
int blocks;
if (false) {
    threads = THREADS_SM1;
    blocks = BLOCKS_SM1;
} else {
    threads = THREADS_SM2;
    blocks = BLOCKS_SM2;
}

(b) oneAPI

Figure 2: Querying device properties

dpct::get_default_queue().submit([&](sycl::handler &cgh) {
    cgh.parallel_for(sycl::nd_range<3>(sycl::range<3>(1, 1, blocks) *
        sycl::range<3>(1, 1, threads)),
        [=](sycl::nd_item<3> item_ct1) {
            solveShort(...);
        });
    });

(a) CUDA

(b) oneAPI

Figure 3: Kernel launch with dynamic work-group size

DPCT1049: The workgroup size passed to the SYCL kernel may exceed the limit. To get the device limit, query info::device::max_work_group.size. Adjust the workgroup size if needed.

To run the CUDA kernel, both block and thread sizes must be configured; however, each device have a different size limit. dpct alerts the programmer that the migrated code may exceed the maximum work-group limit that the underlying architecture supports. In addition, it recommends adjusting the code if necessary. Fig. 3a shows how to run the kernel in CUDA, while Fig. 3b shows the DPC++ counterpart.

DPCT1065: Consider replacing sycl::nd_item::barrier() with sycl::nd_item::barrier(sycl::access::fence_space::local_space) for better performance if there is no access to global memory.

On this situation, dpct recommends the programmer to use an additional parameter when synchronizing threads within the kernel as long as no global memory is used. By default, the tool does not automatically optimize this issue because it cannot discern whether this memory is being used. An example of the CUDA thread synchronization and the migrated oneAPI code can be seen in the Figs. 4a and 4b respectively.

DPCT1084: The function call has multiple migration results in different template instantiations that could not be unified. You may need to adjust the code.
In CUDA, generic functions are a common way to reduce code size, since they permit code reusing for data of different type. Although oneAPI supports this programming feature, it cannot automatically port this kind of code due to the multiplicity of possible migration options. Fig. 4a shows a CUDA example where instructions depend on the type of parameter sent to the kernel function. Fig. 4b shows the corresponding migrated code.

DPCT1059: SYCL only supports 4-channel image format. Adjust the code.

In CUDA, texture memory variables can contain from 1 to 4 channels. In SYCL, texture memory is accessed through images. As it was reported by the dpct warning, SYCL only supports the use of 4-channel images, so the programmer must adapt the parts of the code where images of different sizes are used. In Fig. 5a a 1-channel texture variable is declared in CUDA (placed in the device) and finally a data is read from it. Fig. 5b presents a possible adjustment to corresponding code to convert a texture 1-channel variable to an equivalent 4-channel one. As it can be seen, this conversion requires to modify the indexes through which the memory is accessed to obtain the correct data. In that sense, a 2-bit right shift (equivalent to DIV 4) combined with a logical AND 3 operation (equivalent to MOD 4) must be performed in the corresponding read operation.

3.2.2 Runtime and results check:

once the code compiles correctly, it must be verified that there are no execution errors and that the results obtained are correct. In this case, although the oneAPI program compiled correctly, the following runtime error appeared:

For a 1D/2D image/image array, the width must be a Value >= 1 and <= CL\_DEVICE\_IMAGE\_2D\_MAX\_WIDTH

This error appears because SYCL images have a limited size, being the maximum size of the 1D images (vectors) smaller than their 2D counterparts (matrices). To solve this issue, this image object must be converted to another DPC++ memory abstraction: buffers or USM. We have chosen USM because the required modifications were simpler compared to the other option.

Fig. 6a shows how a 2-level texture memory is allocated on the GPU, while Fig. 6b illustrates how to use USM to send a the array to the device. In that sense, the read mechanism also changes, both in CUDA (Fig. 6a) and in DPC++.
Figure 5: Generic functions

4 Experimental Results

4.1 Experimental design

All tests were carried out using the platforms described in Table 1 oneAPI and CUDA versions are 2022.0 and 11.5, respectively, and to run DPC++ codes on NVIDIA GPUs, we build a DPC++ toolchain with support for NVIDIA CUDA, as it is not supported by default on oneAPI. The performance was evaluated by carrying out similar experiments to those in previous works [13, 16], searching 20 query protein sequences against the well-known UniProtKB/Swiss-Prot database (release 202104).

- The input queries range in length from 144 to 5478, and they were extracted from the Swiss-Prot database (accession numbers: P02232, P05013, P14942, P07327, P01008, P03435, P42357, P21177, Q38917, P27895, P07756, P04775, P19096, P28167, P0C6B8, P20930, P08519, Q7TMA5, P33450, and Q9UKN1).

6https://intel.github.io/llvm-docs/GetStartedGuide.html
7Swiss-Prot: https://www.uniprot.org/downloads
1. texture<char> colTexture;
2. int colSize = colsGpu * sizeof(char);
3. char *colGpu;
4. cudaMemcpy(colGpu, colCpu, colSize, TO_GPU);
5. cudaBindTexture(NULL, colTexture, colGpu, colSize);
6. char v = tex1Dfetch(colTexture, 10);

(a) CUDA

1. dpct::image_wrapper<char, 1> colTexture;
2. int colSize = colsGpu * sizeof(char);
3. char *colGpu;
4. colGpu = (char *)sycl::malloc_device(colSize, dpct::get_default_queue());
5. dpct::get_default_queue().memcpy(colGpu, colCpu, colSize).wait();
6. colTexture.attach(colGpu, colSize);
7. char v = colTexture.read(10 >> 2)[10 & 3];

(b) oneAPI

Figure 6: 4-channel texture memory

1. texture<int, 2, cudaReadModeElementType> seqsTexture;
2. static int *seqsGpu;
3. cudaArray *sequencesGpu;
4. cudaMemcpy(sequencesGpu, seqsTexture.channelDesc);
5. cudaMallocArray(sequencesGpu, sequencesCols, sequencesRows);
6. cudaMemcpyToArray(sequencesGpu, 0, 0, sequences, sequencesSize, TO_GPU);
7. cudaBindTextureToArray(seqsTexture, sequencesGpu);
8. dpct::get_default_queue().memcpy(seqsGpu, sequences, sequencesCols * sequencesRows * sizeof(int)).wait();

(a) CUDA

1. dpct::image_wrapper<sycl::char4, 1> seqsTexture;
2. static int *seqsGpu;
3. cudaArray *sequencesGpu;
4. cudaMemcpy(sequencesGpu, seqsTexture.channelDesc);
5. cudaMallocArray(sequencesGpu, sequencesCols, sequencesRows);
6. cudaMemcpyToArray(sequencesGpu, 0, 0, sequences, sequencesSize, TO_GPU);
7. cudaBindTextureToArray(seqsTexture, sequencesGpu);
8. dpct::get_default_queue().memcpy(seqsGpu, sequences, sequencesCols * sequencesRows * sizeof(int)).wait();

(b) oneAPI

Figure 7: CUDA 2-D texture memory adaptation using DPC++ USM

1. int columnCodes = tex2D(seqsTexture, colOff, j + rowOff);
2. int columnCodes = seqsGpu[(j + rowOff) * sequencesCols + colOff];

(a) CUDA

1. int columnCodes = seqsGpu[(j + rowOff) * sequencesCols + colOff];

(b) oneAPI

Figure 8: Data accessing in 2D array
Table 1: Experimental platforms used in the tests

| ID  | CPU Processor | RAM Memory | GPU Model (Type) | GPU Model (Architecture) | GFLOPS peak (SP) |
|-----|---------------|------------|------------------|--------------------------|-----------------|
| Core-i5 | Intel Core i5-7400     | 16 GB       | NVIDIA (Discrete) | Titan X (Pascal) | 10970          |
| Core-i3 | Intel Core i3-4160     | 8 GB        | NVIDIA (Discrete) | RTX 2070 (Turing) | 7465           |
| Core-i9 | Intel Core i9-10920X   | 32 GB       | Intel (Discrete)  | Iris Xe MAX Graphics (Gen 12.1) | 2534         |
| Xeon  | Intel Xeon E-2176G     | 65 GB       | Intel (Integrated) | UHD Graphics P630 (Gen 9.5) | 441.6         |

- The database contains 204173280 amino acid residues in 565928 sequences with a maximum length of 35213.
- BLOSUM62 and 10(2) were set as the scoring matrix and gap insertion (extension) penalty, respectively.

As SW#db is a hybrid CPU-GPU software, just a single thread was configured at CPU level (flag \(T=1\)) to minimize its impact on the overall performance. Besides, different work-group sizes were configured for kernel execution. Finally, each particular test was run twenty times and the performance was calculated as their average to avoid variability.

4.2 Performance Results

GCUPS (billion cell updates per second) is commonly used as the performance metric in the context of SW [15]. Fig. 9 presents the performance of both CUDA and DPC++ versions on two NVIDIA GPUs when varying work-group size. First, it can be noted that both codes are sensitive to the work-group size. In fact, the best performances are reached using work-group sizes different to the ones that SW#db set as default. Regarding the performance on each NVIDIA GPU, there are no significant differences between both codes on the Titan. However, on the RTX, this situation gets reversed; the DPC++ version outperforms its CUDA counterpart (approximately 5%).

Fig. 10 deepens the above analysis presenting the performance of both CUDA and DPC++ versions on the NVIDIA GPUs when varying the query length (optimal work-group size is used for each case). It can be noted that all versions benefit from larger workloads. As expected, the CUDA code achieves the same GCUPS as the DPC++ one for all query lengths on the Titan. Both DPC++ and CUDA versions present practically the same performance on the RTX, outperforming the latter to the former on the largest sequences.

To verify cross-GPU vendor portability, the DPC++ code was executed on two different Intel GPUs varying the query length (see Fig. 11). Due to the absence of an optimized version for both Intel devices, little can be said about its performance. However, it is important to remark that only two minor changes were necessary to carry out these tests: (1) setting the appropriate work-group size and (2) setting the corresponding backend. As the ported code was compiled and executed with minimal tuning, there is probably room for further improvement.

Finally, Fig. 12 presents the performance of the DPC++ code on 4 different Intel CPUs, demonstrating its cross-architecture portability. Considering performance,

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*A DPC++ work-group is equivalent to a CUDA block.*
more GCUPS are reached as the query length increases. Once again, running the migrated code just required minimal intervention and its performance could be improved through fine tuning.

5 Conclusions and Future Work

The recently introduced Intel oneAPI ecosystem aims to respond to the programming challenge related to heterogeneous computing. In this paper, we present our experiences migrating a CUDA-based, biological software tool to DPC++ using the oneAPI framework. Among the main contributions of this research we can summarize:

- **dpct** proved to be an effective tool for SW#db code migration to DPC++. While it was not able to translate the complete code, dpct did most of the work and gave hints to the programmer on the pending parts.

- The migrated code could be successfully executed on CPUs and also GPUs from different vendors, demonstrating its cross-architecture, cross-GPU vendor portability.

- Performance results showed that the migrated DPC++ code is comparable to the original CUDA one. In fact, DPC++ can be even faster in some cases. As the ported code was compiled and executed with minimal tuning, there is probably room for further improvement.

Future work will focus on:
• Understanding the gap in performance between DPC++ and CUDA codes, and optimizing DPC++ codes to reach their maximum performance.
• Carrying out more exhaustive experimental work. In particular, considering other alignment operations, larger workloads, multi-GPU execution, among others, to increase the representativeness of this study.
• Running the DPC++ code on other architectures like FPGAs, to verify its cross-architecture portability.

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