A High Voltage Multiplier Using Stacked Hybrid Cockcroft–Walton/Dickson Multipliers

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Abstract. A high voltage multiplier is one of the most important components for shockwave non-thermal food processing systems. In the design of the high voltage multiplier for shockwave non-thermal food processing systems, not only high voltage gain but also high speed operation and low voltage stress of circuit components are required. In this paper, a novel high voltage multiplier with stacked topology is proposed for shockwave non-thermal food processing systems. Unlike conventional high voltage multipliers, the proposed multiplier is designed by stacking hybrid Cockcroft-Walton/Dickson multipliers (HCWDMs). In the proposed multiplier, high speed operation is achieved, because the stacked topology can reduce the number of multiplier stages. Furthermore, voltage drop of higher multiplier stages and voltage stress are mitigated by the stacked topology using HCWDMs. The validity of the circuit design is confirmed by the laboratory experiments regarding the prototype of the shockwave non-thermal food processing system. The experimental results demonstrate that the proposed multiplier can generate about 3.9 kV within 113 s by converting the ac input 100 V at 60 Hz.

1. Introduction
In a modern aging society, non-thermal food processing technologies [1, 2] are receiving much attention, because soft and nutritious foods are necessary for elderly persons. In past studies, some non-thermal food processing techniques have been proposed, for example, high hydrostatic pressure technology [3], high voltage arc discharge technology [4], pulsed electric field technology [5], cold plasma technology [6], and so on. Among others, the non-thermal food processing utilizing underwater shockwave [7, 8] is one of the most promising technologies, because low coat non-thermal food processing can be achieved by this technology. The shockwave non-thermal food processing system mainly consists of a high voltage multiplier, a pressure vessel filled with water, and a relay switch. For this reason, to realize a light-weight non-thermal processing system, several high voltage multipliers using low turn-ratio transformers have been proposed in past studies. Among others, the Cockcroft-Walton voltage multiplier [9-12] is usually used in the shockwave non-thermal food processing systems, because a high voltage gain can be achieved by increasing the number of multiplier stages. In past studies, the Cockcroft-Walton voltage multiplier has been studied by many researchers. For example, Lamantia et al. analyzed the dynamic of the Cockcroft-Walton voltage multiplier theoretically [9], Iqbal et al. proposed a bipolar Cockcroft-Walton voltage multiplier [10]. Mudeng et al. developed a symmetrical...
Cockcroft-Walton voltage multiplier [11], and Eguchi et al. designed a stacked Cockcroft-Walton voltage multiplier [12]. However, it is known that the output voltage of the Cockcroft-Walton voltage multiplier begins to sag according to the number of multiplier stages. Of course, to avoid the voltage sag in a higher multiplier stage, the Dickson voltage multiplier [13, 14] is one of the best solutions. However, the Dickson voltage multiplier requires high voltage capacitors, because it suffers from high voltage stress in higher multiplier stage. To overcome these problems, Park et al. suggested the hybrid Cockcroft–Walton/Dickson multiplier (HCWDM) [15]. The HCWDM is the middle ground between the Cockcroft–Walton voltage multiplier and the Dickson voltage multiplier. However, the HCWDM requires large number of multiplier stages to realize a high voltage gain.

For non-thermal food processing systems, we propose a novel high voltage multiplier with stacked topology in this paper, where the stack topology consists of HCWDMs. The proposed technique is a compromise between the stacked Cockcroft-Walton multipliers and the stacked Dickson multipliers. In the proposed multiplier, a high voltage gain is provided by the stack topology. Furthermore, high speed operation is achieved by reducing the number of multiplier stages. In addition, voltage drop of higher multiplier stages and voltage stress are mitigated by HCWDMs. The properties of the proposed multiplier are revealed by theoretical analysis and laboratory experiments. Furthermore, the comparison between the proposed multiplier and conventional multipliers, such as bipolar Cockcroft–Walton voltage multiplier [16], series-connected bipolar Cockcroft–Walton voltage multiplier [17, 18], bipolar doubler [19], and parallel bipolar Cockcroft–Walton voltage multiplier [20], is performed.

This paper is organized as follows: First, section 1 is the introduction part. Next, section 2 is the explanation of the circuit configuration of the proposed multiplier. Then, section 3 is the theoretical analysis of the proposed multiplier with 24 gain, where output voltage and power efficiency of the stacked HCWDMs are analyzed using a four-terminal equivalent model. After that, section 4 is the experimental verification of the proposed topology, where the output voltage of the proposed multiplier is measured experimentally using a laboratory prototype. Finally, section 5 is the summary of this study.

2. Configuration of the proposed multiplier

The circuit configuration of the proposed multiplier is illustrated in figure 1. As this figure shows, the proposed multiplier is composed of an input transformer, two full waveform rectifiers (FWRs), a pulse generator, and a stacked HCWDMs. In the stacked HCWDMs, the hybrid Cockcroft–Walton/Dickson multiplier with the 8 gain is used as a module. In the proposed multiplier, first, the input ac voltage $V_{ac}$ is converted to $V_{max}$ and $-V_{max}$ by the FWRs. Next, by driving the IGBT switches Q1 and Q2 by non-overlapped two-phase pulses $\Phi_1$ and $\Phi_2$, high speed pulses for the stacked HCWDMs are generated from the pulse generator. Finally, the following high stepped-up voltage is generated by the stacked HCWDMs, because the voltage of the capacitors $C_{1,1}$, $C_{1,2} (=C_{i,5}=C_{i,6})$, $C_{1,3}$, and $C_{1,4} (=C_{i,7}=C_{i,8})$ becomes $V_{max}$, $2V_{max}$, $3V_{max}$ and $4V_{max}$, respectively, in steady state:

$$V_{out} \approx 3 \times 8(V_{max} - V_{th})$$

$$= 24(V_{max} - V_{th}).$$

(1)

where $V_{th}$ denotes the threshold voltage of diodes. The output voltage $V_{out}$ is charged into a 200 μF capacitor. In other words, the output voltage of the proposed multiplier is about 3.4 kV (= 100 V × $\sqrt{2}$ × 24) if the input ac voltage $V_{ac}$ is 100 V. The application of the proposed multiplier shown in figure 1 is the non-thermal fruits processor utilizing underwater shockwaves, because fruits such as apples can be processed by discharging a 200 μF capacitor charged to 3.5 kV. Of course, the voltage gain of the proposed multiplier is proportion to the number of modules and multiplier stages. As it can be seen from the capacitor voltage $C_{ij}$ ($i=1, 2, \ldots, 8$), the proposed multiplier can achieve smaller voltage stress from the conventional Dickson multiplier. Concretely, the voltage stress of the proposed multiplier is $4V_{max}$. On the other hand, the voltage stress of the Dickson multiplier is $7V_{max}$ when the voltage gain is 8. Regarding the stacked HCWDMs, the characteristics, such as output voltage and power efficiency, are analyzed theoretically in the following section.
3. Theoretical analysis of the stacked HCWDMs

In this section, the output voltage of the proposed multiplier will be analysed by using a four-terminal equivalent model [21, 22] shown in figure 2. In this figure, $m_i$ is the conversion ratio of an ideal transformer and $R_{SCI}$ is the internal resistance. By deriving the parameters $m_i$ and $R_{SCI}$ from the instantaneous equivalent circuits shown in figure 3, the output voltage of the proposed multiplier is obtained, where we assume that the diode can be modelled by the series-connection of an ideal switch, the on-resistance $R_d$, and the forward threshold voltage $V_{th}$. The four-terminal equivalent model shown in figure 2 can be expressed by the following K-matrix:

$$
\begin{bmatrix}
V_{in,i} \\
I_{in,i}
\end{bmatrix} =
\begin{bmatrix}
1/m_i & 0 \\
0 & m_i
\end{bmatrix}
\begin{bmatrix}
R_{SCI} \\
L
\end{bmatrix}
\begin{bmatrix}
V_{out,i} \\
I_{out,i}
\end{bmatrix}
$$

(2)

Therefore, we can obtain the output voltage $V_{out,i}$ and the power efficiency $\eta$, as

$$
V_{out} = m_i V_{in,i} \times \left( \frac{R_L}{R_L + R_{SCI}} \right)
$$

(3)

and

$$
\eta = \frac{R_L}{R_L + R_{SCI}}.
$$

(4)

where $R_L$ denotes an output load.

First, the conversion ratio $m_i$ is considered in the $i$-th module. In a steady state condition, the four-terminal equivalent model of the $i$-th module can be analysed as follow. When the switch Q1 is on and the switch Q2 is off, the variation of the electric charge in the input and output terminals, $\Delta q_{T_1,v_{in,i}}$ and $\Delta q_{T_1,v_{out,i}}$, are expressed as

Figure 1. Circuit configuration of the proposed stacked HCWDMs.
Figure 2. An example of the four-terminal equivalent model [21, 22].

Figure 3. Instantaneous equivalent circuits: (a) Q1 is off and Q2 is on (State $T_1$) and (b) Q1 is on and Q2 is off (State $T_2$).

\[ \Delta q_{T_1,v_{in}} = -\Delta q_{T_1}^{L_1} - \Delta q_{T_1}^{L_3}, \]  
\[ \Delta q_{T_1,v_{out}} = \Delta q_{T_1}^{L_7} + \Delta q_{T_1}^{L_9}. \]
\[ \Delta q_{T_2}^{i_1} + \Delta q_{T_1}^{i_2} = 0, \]  
(7)

and

\[ \Delta q_{T_1}^{L_5} + \Delta q_{T_1}^{L_6} = 0. \]  
(8)

In the \( i \)-th module, the relationship of symmetry yields

\[ \Delta q_{T_2}^{i_1} = -\Delta q_{T_2}^{i_2} = \Delta q_{T_1}^{L_5} = -\Delta q_{T_1}^{L_6}, \]  
(9)

\[ \Delta q_{T_1}^{L_5} = -\Delta q_{T_1}^{L_4}, \]  
(10)

and

\[ \Delta q_{T_1}^{L_7} = -\Delta q_{T_1}^{L_8}. \]  
(11)

On the other hand, when Q1 is off and Q2 is on, the variation of the electric charge in the input and output terminals, \( \Delta q_{T_2,\text{in},i} \) and \( \Delta q_{T_2,\text{out},i} \), are expressed as

\[ \Delta q_{T_2,\text{in},i} = \Delta q_{T_1}^{L_1} + \Delta q_{T_2}^{L_3}, \]  
(12)

\[ \Delta q_{T_2,\text{out},i} = \Delta q_{T_1}^{L_8}, \]  
(13)

and

\[ \Delta q_{T_2}^{L_6} + \Delta q_{T_2}^{L_7} = 0. \]  
(14)

Here, in a steady state condition, the input current \( I_{\text{in},i} \) and the output current \( I_{\text{out},i} \) can be expressed by the average of the electric charge variation over period \( T \). Therefore, we have \( I_{\text{in},i} \) and \( I_{\text{out},i} \) as follows:

\[ I_{\text{in},i} = \left( \Delta q_{T_2,\text{in},i} + \Delta q_{T_2,\text{in},i} \right)/T \]  
(15)

and

\[ I_{\text{out},i} = \left( \Delta q_{T_2,\text{out},i} + \Delta q_{T_2,\text{out},i} \right)/T. \]  
(16)

Inserting (5) – (14) into equations (15) and (16), the relationship between \( I_{\text{in},i} \) and \( I_{\text{out},i} \) is obtained as

\[ I_{\text{in},i} = -8 I_{\text{out},i}. \]  
(17)

From equation (17), the conversion ratio of the ideal transformer, \( m_\text{i} \), is 8 in the \( i \)-th module.

Next, the internal resistance \( R_{\text{SCI}} \) is considered in the \( i \)-th module. From the instantaneous equivalent circuits shown in figure 3, we develop a system of equations for the consumed energy to obtain the internal resistance \( R_{\text{SCI}} \). In figures 3 (a) and (b), the consumed energy \( W_{T_1,i} \) and \( W_{T_2,i} \) are expressed as

\[ W_{T_1,i} = \frac{R_d}{T_1} \left( \Delta q_{T_1}^{L_1} \right)^2 + \frac{R_d}{T_1} \left( \Delta q_{T_1}^{L_5} + \Delta q_{T_1}^{L_7} \right)^2 + \frac{R_d}{T_1} \left( \Delta q_{T_1}^{L_8} \right)^2 + \frac{R_d}{T_1} \left( \Delta q_{T_1}^{L_{10}} \right)^2, \]  
(18)

and

\[ W_{T_2,i} = \frac{R_d}{T_2} \left( \Delta q_{T_2}^{L_1} \right)^2 + \frac{R_d}{T_2} \left( \Delta q_{T_2}^{L_2} \right)^2 + \frac{R_d}{T_2} \left( \Delta q_{T_2}^{L_5} \right)^2 + \frac{R_d}{T_2} \left( \Delta q_{T_2}^{L_6} \right)^2. \]  
(19)
Rearranging equations (18) and (19), we get the consumed energy over the period $T$, $W_{T,i}$, as follows:

$$W_{T,i} = W_{T_1,i} + W_{T_2,i} = \left(\frac{176R_d}{9}\right)(I_{out,i})^2T.$$

(20)

From equation (20), the internal resistance, $R_{SCi}$, is $176R_d/9$ in the $i$-th module. Therefore, combining $m_i$ and $R_{SCi}$, the four-terminal equivalent model can be expressed by figure 4. Finally, we can obtain the output voltage $V_{out,i}$ and the power efficiency $\eta_i$ as

$$V_{out} = 24(|V_{max}| - V_{th}) \times \left(\frac{R_L}{R_L+176R_d/3}\right) \quad \text{and} \quad \eta = \frac{R_L}{R_L+176R_d/3}.$$

(21)

As it can be seen from equations (1) and (21), the equation (21) is equal to the equation (1) if $V_{th}$ and $R_d$ are negligibly small.

Figure 4. Four-terminal equivalent model of the proposed multiplier.

4. Experimental Evaluation

To confirm the validity of circuit design, experimental evaluation was performed regarding the laboratory prototype of the shockwave non-thermal food processing system shown in figure 5. The laboratory prototype consists of a high voltage multiplier, a high voltage relay, a high voltage big capacitor, and a water tank. In the experimental circuit, the proposed multiplier with 3 modules was used to generate more than 3.5 kV from a 100 V at 60 Hz input, where the IGBT switches were operated at 10 kHz. The proposed multiplier was assembled by the circuit components shown in table 1.

Figure 5. Laboratory prototype of the shockwave non-thermal food processing system used in the experimental evaluation.

Figure 6 shows the measured output voltage of the proposed multiplier as a function of time. As this figure shows, the experimental circuit of the proposed multiplier can generate a 3.91 kV output within
Due to the error of the transformers, the measured output voltage is higher than that of the theoretical output voltage shown in equation (12). Table 2 shows the characteristic comparison between the proposed multiplier and conventional multipliers. From these results, we can confirm the effectiveness of the proposed multiplier. The proposed multiplier can achieve not only high voltage gain but also high speed operation. Of course, the conventional multiplier reported in [20] is faster than the proposed multiplier, because the ac input of the conventional multiplier [20] is much larger than that of the proposed multiplier. Furthermore, the output voltage of the conventional multiplier [20] is an ideal value obtained by a computer simulation.

**Table 1.** Circuit components to assemble the experimental circuit.

| Description   | Part                          |
|---------------|-------------------------------|
| Diode         | 1N4007                        |
| IGBT Switch   | GT50JR22                      |
| Driver        | IC IR2110PBF                  |
| Internal Capacitor | R463W510050M1K 630VDC 10μF  |
| Output Capacitor | TOEI Corp. 200μF/4000VDC     |

**Figure 6.** Measured output voltage of the proposed stacked voltage multiplier with three modules.

**Table 2.** Characteristic comparison.

| Type                          | Input Voltage | Output Voltage | Rise Time          |
|-------------------------------|---------------|----------------|--------------------|
| Proposed                      | 100 V at 60 Hz| 3.91 kV        | 113 s (Experiment) |
| Bipolar Cockcroft-Walton [16] | 100 V at 60 Hz| 3.93 kV        | 281 s (Experiment) |
| Series-connected Cockcroft-Walton [17, 18] | 100 V at 60 Hz | 3.95 kV (Ideal) | 220 s (Experiment) |
| Bipolar Doubler [19]          | 100 V at 60 Hz| 3.19 kV        | 110 s (Experiment) |
| Parallel bipolar Cockcroft-Walton [20] | 220 V at 50 Hz | 3.58 kV        | 600ms (Simulation) |

5. Conclusion
For shockwave non-thermal food processing, a novel high voltage multiplier has been proposed in this paper. The proposed multiplier has stacked topology consisting of three HCWDM modules. The topology enables high speed operation and high voltage gain by reducing the number of multiplier stages in HCWDMs. The validity of the circuit design was confirmed by theoretical analysis and laboratory experiments. In the experiment, the measured output voltage reached about 3.9 kV within 113 s for a 100 V at 60 Hz input. Furthermore, the effectiveness was verified by comparing the proposed multiplier with conventional multipliers. The comparison result demonstrated that the proposed multiplier outperforms the conventional multipliers. The detailed mathematical analysis of the dynamic behaviour of the proposed multiplier is left for future study.
6. References

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