Assessment of Junction Termination Extension Structures For Ultrahigh-Voltage Silicon Carbide Pin-Diodes; A Simulation Study

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ABSTRACT The junction termination extension (JTE) structures for ultrahigh-voltage (UHV) devices consumes a considerable part of the semiconductor chip area. The JTE area is closely related to chip performance, process yield and ultimately device cost. The JTE lengths for UHV devices (i.e., > 30 kV) are still unknown, not visible in the scientific literature and have therefore been predicted in this study by means of two-dimensional numerical simulations using the Sentaurus based technology computer-aided design (TCAD) tool. A previously reported space-modulated, two-zone JTE (SM-JTE) structure has been used as an input to set up a suitable TCAD model, which is further scaled to JTE lengths required for 40 kV class and 50 kV class SiC PiN diodes. The simulation results indicate that the SM-JTE requires an 1800 μm one-sided JTE length with 27 guard rings for a 40 kV theoretical PiN diode and 2700 μm with 36 guard rings for a 50 kV device, resulting in breakdown voltages of 41.4 kV and 51.7 kV, respectively. Moreover, the design considerations of different JTE categories are discussed with focus on the adaptability of the termination structures in ultrahigh-voltage devices, e.g., V_B > 30 kV, which results in a comparison of the SM-JTE structure with other high-voltage JTE designs.

INDEX TERMS 4H-SiC device, JTE structure, junction termination extension design, PiN Diode, ultrahigh-voltage device, wide bandgap device.

I. INTRODUCTION

High-Voltage semiconductor devices are required in various power electronic applications (e.g., in high-voltage direct-current (HVDC) systems, flexible AC transmission systems (FACTS), solid-state transformers (SST), and solid-state (hybrid) circuit breakers (SSCB)), where devices with high blocking voltage capability may reduce the number of medium-voltage devices in series connection and thus simplify the converter system in several aspects (i.e., reduce the total amount of devices and gate drivers, system complexity, cooling-requirement, and station footprint with better environmental impact) [1], [2]. Moreover, long-term visionary device candidates with ultrahigh blocking capability may have sufficiently high nominal voltage to facilitate low-complexity converter systems with e.g., two-level or three-level converter topologies aiming for LV/MV SST applications etc. The material properties of (4H-) Silicon Carbide (SiC) allow manufacturing of devices that withstand higher electric fields than Silicon (Si) based counterparts and thus achieves higher breakdown voltage, V_B, capabilities, theoretically up to 50 kV [3]–[5]. The persistent research effort in developing SiC material processing and semiconductor device design, has demonstrated bipolar charge-carrier devices with blocking voltage capabilities as high as 27 kV [6]–[9]. However, a carefully designed junction termination extension (JTE) structure is required to relax the electric field at/around the active region of the device and re-distribute the field through lateral variation of equipotential flux contours into the termination region.
Thus, a successfully implemented JTE structure allows breakdown voltages to reach close to the parallel-plane breakdown voltage, $V_{B,PP}$, [10], [11]. Note, that the blocking voltage instability as a result of charge accumulation at the SiO$_2$/SiC interface in the JTE regions during high-temperature reverse bias (HTRB) testing and high-humidity HTRB (H3TRB) testing has earlier been investigated [12]. Oxide thickness variation and resulting field oxide non-uniformity over extended surface regions for high-voltage devices are additional concerns leading to pre-mature time dependent dielectric breakdown. It is, therefore, more critical to suppress the magnitude of the surface electric field ($<3–4$ MV/cm) especially when realizing ultrahigh voltage devices working at elevated temperatures.

Research-level SiC device prototypes with blocking voltage capabilities above 15 kV have been demonstrated using floating field/guard rings (FFR/FGR) [6], [13]–[15], multi-zone (MZ)-JTE [16]–[18], optimized implantation-free (O)-JTE [19], negative bevel based (NB)-JTE [20], [21], and space-modulated (SM)-JTE [7]–[10], [22] termination structures, offering each design concept with its specific set of advantages and disadvantages. The floating guard-ring structure is processed without additional manufacturing steps but requires more than 100 rings for devices with >10 kV blocking voltage capability [23], [24]. A 1500 $\mu$m FGR structure was used to alleviate the electric field in a 230 $\mu$m thick drift region of a SiC n-IGBT, enabling a sustained blocking voltage of 27.5 kV [6]. However, the ring width and spacing may be difficult to optimize, especially with the influence of oxide traps and charges at the SiO$_2$/SiC interface [11], [25]. Single-zone (SZ)-JTE structures are less sensitive to width and spacing but have a narrow processing (implanted dose) window [7], [26]. In contrast, multi-zone JTE structures have a wider dose window but encounter high electric field peaks in the border between the zones [27], [28]. Similar field peaks are also visible in the transition points caused by vertical etched steps [19], [29], [30], [48], but they may be relaxed using a low-angle bevel step approach [29]. Note, that JTE structures formed by p-type epitaxial growth (e.g., anode doping) and step etch JTE, minimize crystal defects due to lack of ion implantation processing [48]. Further simplifications are provided by negative bevel termination structures (and smoothly tapered structures [31]), which are area-efficient and facilitate low leakage currents. These structures are, however, mainly targeting p-type thyristor structures [20], [21], [32]. Termination structures that combine guard-rings with single/multiple JTE regions (i.e., ring-assisted-JTEs [26], [33], hybrid-JTE [26] SM-JTE [7], [10], multiple-ring-modulated JTE [34], and counter-doped (CD)-JTE [25]) provide high breakdown voltages (i.e., close to ideal $V_{B,PP}$) in combination with a wide dose margin, yet with a small process increase [25], [26]. Moreover, ion implantation combined with step etching [23], [24] are relatively area-efficient but may be sensitive to processing spread of the ring width and charges at the oxide interface [23] and, hence, offer a narrow processing window. Y. Wen et al., [23] have recently, demonstrated a 30.4 % decrease in one-sided JTE length, $l_{JTE}$, by introducing an additional etching step to the conventional field-limiting-ring termination. The JTE length efficiency (i.e., $V_{B}/l_{JTE}$) of selected JTE structures with drift region doping concentrations of 1–2 $\times$ 10$^{14}$ cm$^{-3}$ [7], 2 $\times$ 10$^{14}$ cm$^{-3}$ [8], [13], [30], [33], [35], [37], 2.5 $\times$ 10$^{14}$ cm$^{-3}$ [6], 3 $\times$ 10$^{14}$ cm$^{-3}$ [36], 4.5 $\times$ 10$^{14}$ cm$^{-3}$ [31], and 5 $\times$ 10$^{14}$ cm$^{-3}$ [11], [23], [24], are summarized in Fig. 1. The differences in doping concentration may cause small shifts in length efficiency, however, the figure provides an overall reasonable comparison of JTE structures. Note, that the semiconductor performance, yield, and cost are closely related to the active/total area ratio, which is set by the required termination length and is more critical for UHV devices. Generally speaking, the termination structure consumes a large area in a reliable high voltage SiC device, and, therefore, it significantly contributes to the cost [49]. In the SiC low/medium voltage (i.e., 1.2 kV) device segment, A. Bolotnikov et al., demonstrated a JTE length requirement of approximately 3–5 times the device thickness [49]. However, the increasing design challenge for high voltage devices (i.e., 20–30 kV) usually requires longer JTE lengths (i.e., 4–9 times [6], [7], [13]), as it varies with JTE design complexity and material process maturity.

In the research literature, neither any 2/3-terminal SiC bipolar device prototype above 30 kV is manufactured, nor any simulation studies have been carried out to predict the JTE length requirements for 30–50 kV devices, to the best knowledge of the authors. It is, therefore, still important to determine and refine these quantities (e.g., $l_{JTE}$) as an integral part of the unit process development to allow accurate comparison and benchmarking for UHV SiC-based devices in high-power applications, and hence further support UHV device design and futuristic device technology development. With these aspects in mind, two-dimensional numerical simulations present the most computationally efficient scenario to accurately predict the required JTE length for devices with 30–50 kV blocking voltage capability.
This paper aims to predict the one-sided JTE length required for UHV devices (i.e., 20–50 kV SiC PiN diodes), thus determine the active area for devices in the different UHV blocking voltage classes, which is a fundamental requirement for benchmarking studies between e.g., medium voltage devices and UHV devices. Moreover, the design considerations of different JTE categories are discussed with focus on the adaptability of the termination structures in ultrahigh-voltage devices (e.g., $V_B > 30$ kV), which results in a comparison between two suitable UHV JTE candidates, namely the SM-JTE and the etched-single-zone (ESZ)-JTE. Here, the etched-single-zone (ESZ)-JTE utilizes an additional implantation step before the RIE etching, which enables step-etch charge shaping for devices with n-type background/drift layer doping, similar as in [48]. An n-type drift doping is predicted for UHV bipolar SiC devices, as it provides better static and dynamic characteristics than p-type counterparts [3], [17], [50]. The junction termination structures relevant to this paper are summarized in Table 1, along with its acronyms and references.

### II. TCAD SIMULATION SETTINGS AND JUNCTION TERMINATION STRUCTURE DESIGN

The numerical simulations of 4H-SiC PiN diodes with different JTE structures are performed using the Sentaurus TCAD simulation platform [38]. The evaluation of JTE designs using TCAD simulations provides a relatively realistic view of the possible capability of JTE structures and is the preferred method in early JTE design assessment. As a starting point, the state-of-art SM-JTE design [7] is implemented and compared to previously reported results to verify the simulation settings. Therefore, a small part of the active region of the PiN diode was implemented along with the complete, one-sided junction termination. For device calibration, the active region of the PiN diode TCAD model is implemented according to the UHV SiC PiN diode structure by N. Kaji et al., [7] (i.e., intrinsic-layer thickness (doping) = 150 μm $(1 \times 10^{14}$ cm$^{-3}$), buffer layer thickness (doping) = 8 μm $(1 \times 10^{18}$ cm$^{-3}$), two-layer anode with thickness (doping) = 2 μm + 0.2 μm $(1 \times 10^{19}$ cm$^{-3}$ and $2 \times 10^{20}$ cm$^{-3}$). To achieve UHV devices with 20–30 kV blocking voltage capability, the model is modified with intrinsic-layer thicknesses and doping concentrations according to Table 2, while keeping the remaining physical parameters the same. The ideal breakdown voltage for respective structure is calculated using Konstantinov’s ionization coefficients [39]. In general, a fine mesh is used at the pn-junctions. The density of the mesh gradually increases with a factor of 1.4–2.8, starting from 1.5 nm and a coarser mesh size of 0.5–2.5 μm has been adopted in less critical regions of the device, resulting in a total number of mesh points in the range of 48000–310000 for the complete device model. More details of the termination region are presented in the following sections.

The implementation of the diode and termination structure in Sentaurus is performed with a series connected resistor, that facilitates good convergence during breakdown voltage simulations [38]. The temperature dependent impact ionization coefficients determined by Y. Zhao et al., [40] are employed in the crystal direction parallel to the c-axis (0001) while coefficients derived by T. Hatakeyama et al., [41] are implemented in the perpendicular crystal direction (1120). The list of the implemented physics-based models is stated in Table 3. The simulations are performed at room temperature (i.e., RT = 300 K) and with an ambipolar charge carrier lifetime of $\tau_A = 10 \mu s$.

### TABLE 1. Junction Termination Structure Acronyms and References

| Junction termination extension (JTE) Design | Acronym | Reference |
|------------------------------------------|---------|-----------|
| Counter doped                            | CD-JTE  | [25]      |
| Etched-single-zone                        | ESZ-JTE | -         |
| Etching uniform field limiting ring       | EU-FLR  | [23]      |
| Field-plate and guard ring assisted       | FPR-assist | [28]   |
| Floating field/guard rings                | FFR/FRG | [6,13,15,26] |
| Graded JTE                               | G-JTE   | [49]      |
| Hybrid JTE                               | -       | [26,36]   |
| Multiple floating zone                    | MFZ-JTE | [26]      |
| Multiple ring-modulated                   | MRM-JTE | [34]      |
| Multiple-step-modulated                   | MSM-JTE | [24]      |
| Multistep guard-ring-assisted             | MS-GR-JTE | [33]  |
| Multi-zone                                | MZ-JTE  | [16,17,18,36] |
| Multizone gradient-modulated             | MGM-GR  | [11]      |
| guard ring                               |          |           |
| Negative bevel                           | NB-JTE  | [20,21,32] |
| Optimized implantation-free              | O-JTE   | [19,30,43,44] |
| Ring-assisted                            | RA-JTE  | [26]      |
| Single zone                              | SZ-JTE  | [26,35,36,49] |
| Single-zone negative bevel               | SZNB-JTE| -        |
| Smoothly tapered                         | ST-JTE  | [31]      |
| Space-modulated buffer trench            | SMBT    | [30,37,45] |
| Space-modulated, two-zone                | SM-JTE  | [7–10,22] |
| Ultralow angle bevel-etched              | UL-A-BE | [29]      |

### TABLE 2. 20–50 kV SiC PiN Diode Intrinsic-Region Parameter Set

| $V_B$ Class | Thickness | Doping Concentration | Ideal Breakdown Voltage |
|-------------|-----------|----------------------|-------------------------|
| 20 kV       | 160 μm    | $1.75 \times 10^{14}$ cm$^{-3}$ | 23.5 kV |
| 30 kV       | 260 μm    | $1.50 \times 10^{14}$ cm$^{-3}$ | 35.0 kV |
| 40 kV       | 360 μm    | $1.25 \times 10^{14}$ cm$^{-3}$ | 45.6 kV |
| 50 kV       | 460 μm    | $1.00 \times 10^{14}$ cm$^{-3}$ | 56.5 kV |

### TABLE 3. Physics-based Models Used in the TCAD Simulations

- **Fermi-Dirac Statistics**
- **Incomplete Ionization**
- **Impact Ionization (Okuto-Crowell)**
- **4H-SiC Bandgap Properties + Bandgap Narrowing (Sloooom)**
- **Mobility: Anisotropic, Temperature and Doping dependent, High-Field Effects (Canali/Caughhey-Thomas)**
- **Carrier-Carrier Scattering (Conwell-Weisskopf)**
- **Enormal (Lombardi), Phonon scattering**
- **Recombination: Shockley-Read-Hall (Scharfetter), Radiative/Band-to-band (direct), Surface SRH, Auger**
A. SPACE-MODULATED, TWO-ZONE JTE (SM-JTE)

The space-modulated, two-zone JTE (SM-JTE) is one of the most efficient experimentally demonstrated termination structures, as indicated in Fig. 1, which has been used in state-of-art devices reaching blocking voltage levels up to 27 kV [7]–[9]. Therefore, SM-JTE is used as a baseline structure for the termination region in the TCAD model to predict the required length for UHV devices.

In [7], the processing of the SM-JTE is performed by initial etching to form the mesa-combined structure, followed by a two-step ion implantation process. Here, the mesa-combined structure is processed by capacitively coupled plasma reactive ion etching (RIE) with a SiO$_2$ bevel mask [35], achieving a rounded bevel edge [7], [10], [34], [35]. Moreover, the 600 $\mu$m long, SM-JTE is performed with multiple Al$^+$ implantation steps of energy levels ranging between 25–700 keV, achieving a dose ratio of dose$_1$/dose$_2$ = 4 with the space and width patterns of the JTE-zones/guard-rings as declared in [7].

In this paper, the TCAD model is implemented to reflect the SM-JTE structure by employing a combined-mesa etch of 3 $\mu$m [7] with the bevel angle of 70 degrees [35]. Here, the rounded bottom is simplified to a straight/tilted line, similar to the TCAD (i.e., Synopsis Dessis tool) simulations in [7]. Moreover, the same JTE/ring pattern, dose ratio, one-sided JTE length, intrinsic-layer thickness, and doping concentrations are also implemented. With the stated implantation energy levels, the Al$^+$ particles are assumed to penetrate 0.8 $\mu$m into the SiC material [7], which is well represented by a gaussian distribution of Al$^+$ in the device simulations. As a reference, the gaussian penetration depth range is between 0.25 $\mu$m and 1 $\mu$m in previously reported JTE studies [23], [33], [36]. The TCAD implemented SM-JTE structure is visible in Fig. 2a.

B. SINGLE-ZONE NEGATIVE-BEVEL JTE AND SINGLE-ZONE ETCHED-STEP JTE DESIGNS FOR ULTRAHIGH-VOLTAGE DEVICES

The ideal termination structure has a constantly decreasing effective charge, moving towards the edge of the chip, which allows for a wide spread of the electric field over the complete termination region, thus relaxing the field in the active region of the device. The majority of the JTE structures strives towards the ideal effective charge by employing various patterns of ion implanted guard rings [11], [26], JTE zones [26], [27], or combinations of the two [7], [25], [26], [33], [34]. The same applies for different beveled termination structures [20], [21], [31], [32] and etched-step (ES)-JTE structures [19], [29], [30], [37], [43]–[45], [48].

In theory, a simple, yet effective termination structure is a single-zone JTE structure submitted to a bevel etch, (SZNB)-JTE, to achieve an ideal effective charge, according to Fig. 3a. The SZ implant introduces an additional region, besides the P$^+$ anode region (or gate layer in e.g., thyristors), where bevel etch or step etch charge shaping are possible. Here, the
TABLE 4. Ultrahigh-voltage JTE Design Guidelines

| Category, subtype and selected references | Max. V₆ | Challenges for UHV JTE design | Main design parameters (Besides JTE length) | Suitability / probability for UHV JTE implementation |
|-----------------------------------------|---------|--------------------------------|---------------------------------------------|--------------------------------------------------|
| Single (SZ) / Multiple-zone (MZ) JTE: SZ-JTE: [35], MZ-JTE: [16]-[18], GTJE [49]. | 16.5 kV | Similar challenges as for LV/MV design: Narrow processing window. Electric field peak between zones. In addition for MZ in UHV devices, increasing number of implant steps and electric field peaks between zones. | SZ and MZ: Implant dose. MZ: Number of zones and zone lengths. | SZ: Low. MZ: Medium. Due to similar drawbacks as for LV/MV JTE designs. More complex manufacturing with increasing number of implant steps. |
| Floating Field / Guard Ring (FFR) JTE FFR-JTE: [6], [13]-[15]. | 27.5 kV | Large number of rings (e.g., 100-6 rings for UHV devices). Low termination efficiency requires large termination area for UV devices. More FFRs to spread electric field employed with gradually changing spacing/widths may be compromised due to processing limitations. Increasing spacing may interrupt depletion layer lateral spread. | Implant dose, number of rings, ring width and spacing. | Medium. Simple processing implementation but with low termination efficiency, thus requires large portion of the chip area for termination. However, larger viability with future larger chip sizes. |
| Hybrid JTE / Combinations of MZ and FFR SM-JTE: [7]-[10], [13], Other: [25], [26], [33], [34], [36]. | 27.5 kV | Wide dose margin, small process increase. (e.g., 10-4 rings for UHV devices). | Implant dose, implant dose ratio, number of rings, ring pattern (modulated width, space), and zone length. | High. The process is scalable towards UHV designs, as the required number of rings is maintainable. The methods hold several design parameters and provide high termination efficiency. |
| Negative Bevel Etch (NBE) JTE NBE: [20], [21], [29], [32], ST-JTE: [31], SZN-JTE [-]. | 20.0 kV | Mainly suitable for p-type devices (e.g., p-GTO). Approx. 2.5 μm gate layer thickness for charge balancing requires bevel angles about 0.05-0.24° for 20-50 kV class. SZNB-JTE enable JTE for n-type but with lower charge balancing height (i.e., height of SZ-JTE implant, e.g., 0.8 μm) and requires < 0.05° bevel angles. | Bevel etch angle and/or shape. Implant dose for SZNB-JTE. | Low. Today, bevel etch angle to low for practical implementation in UHV devices. However, further development in e.g., ST methods may enable future designs with lower bevel angles. |
| Etched Multistep JTE O-JTE: [19], [43], [44], [48], EU-FLR: [23], MM-JTE: [24], SMBT-JTE: [30], [37], ESZ-JTE [-]. | 15.8 kV | Mainly suitable for p-type devices (n-type preferred for UHV devices). Peak fields between etched step. ESZ-JTE enable JTE for n-type. | Etch height, number of trenches/steps, etch pattern (modulated width, space). Implant dose for SZ-based JTE designs, e.g., ESZ-JTE. | High. The large set of design parameters enables charge shaping in various ways, which allows for flexible termination structure design suitable for UHV design. |

bevel etch requires a low angle to etch along the complete JTE length, which may be realized for short termination lengths by an ultralow bevel etch (1.9° angle [29]) or a smoothly tapered etch method (5 nm/μm ~ 0.29° angle [31]). However, this structure is unsuitable for UHV devices since the requirements of the bevel etch become unrealistic (e.g., either < 0.05° bevel angle or > 6 μm ion implant penetration depth for JTE designs targeting > 30 kV). If, instead, a single-zone JTE structure is combined with a number of RIE steps to form the triangular-shaped effective charge profile, the processing requirements are relaxed compared to the low bevel etch, thus forming the ESZ-JTE design. This design is a combination of SZ-JTE and ES-JTE which enables step-etch charge shaping within devices, within either p-type or n-type background doping, thus also suitable for UHV devices with n-drift layers, e.g., PiN diodes. This is similar to the processing of R. Ghandi et al. [48], but instead of the p-type epitaxial growth layer, the ESZ-JTE uses ion implantation to form the JTE region. In ES-JTE structures, the step height ranges from 40 nm to 1.5 μm [19], [43], [45], [48], with an accuracy of approximately 0.1 nm [23], [24]. In the case of an etched-single-zone JTE with an ion implant penetration depth of e.g., 0.8 μm, the etching process may be repeated several times to achieve the requested number of etch levels and, thus, effective charge accuracy. As an example, applying one etching step (e.g., 0.4 μm) results in a two-zone/level JTE structure (e.g., 0 μm and 0.4 μm) as shown in Fig. 3b. Moreover, applying two etching steps (e.g., 0.4 μm and 0.2 μm) results in a four-zone/level JTE structure (e.g., 0, 0.2, 0.4 and 0.6 μm) as shown in Fig. 3c, and so on (three steps ~ eight-zone/level JTE in Fig. 3d). The TCAD implemented three-step ESZ-JTE structure is visible in Fig. 2b. Similar to other termination structures, the effective JTE dose may be tailored at the cost of adding more etching/implantation steps, and thus more complicated/costly device processing. Moreover, the different JTE designs offer various design parameters to tune the termination structure, which in the end will be more or less suitable for JTE designs with UHV blocking voltage levels. Termination methods that are suitable for low/medium voltage devices may appear less attractive for high voltage JTE structures, as the design complexity processing methods and/or process tolerances are limited. A summary of the adaptability of ultrahigh voltage implementation for the different JTE design categories are presented in Table 4, which concludes the overall JTE design suitability and guidelines with respect to challenges and its main design parameters. Here, it is proposed that the hybrid/SM-JTE designs (or similar) along with etched multistep JTE structures are well-suited candidates for n-type UHV device implementation. The FFR-JTE structures provide a relatively simple processing but holds a relatively
low termination efficiency, almost half of the SM-JTE [8]. Thus, it is predicted that the termination structure will consume a large portion of the total chip area, especially for > 30 kV class devices. Therefore, the SM-JTE and ESZ-JTE designs are benchmarked in the following section. It should be kept in mind that the SiC material quality has evolved significantly during the last decades, as the chip size, drift thickness and blocking capability have increased from 1x1 mm$^2$, 1 mm, and 3 kV, respectively, in 2001 [51], 10x20 mm$^2$, 160 mm, and 20 kV, respectively, in 2013 [20], to 3.5x3.5 mm$^2$, 230 mm, and 26.8 kV, respectively, in 2020 [8]. The development of epitaxial growth methods has enabled high growth speeds (i.e., > 100 mm/h [52]) and with low levels of critical traps and dislocations (i.e., deep-level trap density < 1 x 10$^{11}$ cm$^{-3}$ [52]). Sufficiently good material results in high performance devices with charge carrier lifetimes above 20 μs (i.e., [7], [53]). The determined effort for SiC material research may enable high quality devices with larger chip areas, thicker epitaxial regions and high blocking voltage capability in the future.

III. TCAD SIMULATION RESULTS AND DISCUSSION

A. 20 KV CLASS SiC PIN DIODE COMPARISON

First of all, the simulated forward voltage characteristics (i.e., anode current vs. anode-cathode voltage, $I_A$–$V_{CA}$) of a SiC PiN diode with a 148 μm thick intrinsic-layer are compared to previously reported experimental values [7] in Fig. 4. With a set of process dependent parameters ($\tau_A = 10.8$ μs lifetime, p-type contact resistivity $= 6.1 \times 10^{-4} \ \Omega \text{cm}^2$) and with the same set of device geometrical parameters and physical models as in [42], the simulated diode characteristics are correlating sufficiently well with the experimental $I_A$–$V_{CA}$ curve. The reverse characteristics of a 150 μm thick intrinsic-layer SiC PiN diode with accompanying SM-JTE termination are simulated with different implant doses and are compared to previously reported findings [7], as shown in Fig. 5. Note that the various sets of impact ionization parameters [38] generates a relatively large variation in breakdown voltage capability, however, by employing Y. Zhao [40] and T. Hatakeyama [41] coefficients, the simulated result correlates reasonably well with [7], but with discrepancies for lower ion implantation doses. The dose window by N. Kaji et al. [7], achieves a wider dose plateau, while our TCAD simulation results indicate a more triangular-shaped dose window, similar to the SM-JTE simulations (Synopsys Dessis) in [9]. The highest breakdown voltage of approximately 21.3 kV is achieved for an implant dose $= 2.6 \times 10^{13} \ \text{cm}^{-2}$. Here, the internal electric field distribution, obtained from a lateral cut-line at 1.5 μm from the top surface, and the impact ionization current distribution, Fig. 6. Here, the highest impact ionization rate is visible at
TABLE 5. SM-JTE Width and Space Parameter Set for 40–50 kV Class Diodes

| Ring no. | Width (μm) | Space (μm) | Ring no. | Width (μm) | Space (μm) |
|----------|------------|------------|----------|------------|------------|
| 1 (dose1) | 920        |            | 1 (dose1) | 1520       |            |
| 2-4      | 30         | 10         | 2-5      | 30         | 10         |
| 5-8      | 25         | 15         | 6-10     | 25         | 15         |
| 9-16     | 10         | 10         | 11-20    | 10         | 10         |
| 17-20    | 10         | 15         | 21-25    | 10         | 15         |
| 21-22    | 10         | 20         | 26-28    | 10         | 20         |
| 23-24    | 10         | 25         | 29-31    | 10         | 25         |
| 25-26    | 10         | 30         | 32-34    | 10         | 30         |
| 27       | 10         | 40         | 35-36    | 10         | 40         |

Remaining length of dose2 = 40 μm Remaining length of dose3 = 40 μm

The last dose1-implemented region (i.e., \( x \approx 570 \, \mu\text{m} \)), and as the avalanche current increases, the largest impact ionization current redistributes to the end of the first dose1 JTE-zone (i.e., \( x \approx 210 \, \mu\text{m} \)), where the largest current is visible. The peak electric field reaches 2.41 MV/cm at the edge of the SM-JTE, where the initial breakdown occurs.

As a conclusion, it is the opinion of the authors that the implemented SM-JTE TCAD model is sufficiently accurate for the purpose of this study, to predict the required JTE-length for SiC devices with UHV blocking voltage capabilities.

B. 20–50 kV CLASS SiC PiN DIODES WITH SM-JTE

The active regions of the SiC PiN diodes are extrapolated to 20–50 kV class devices by the intrinsic-layer modifications according to Table 2. To achieve high voltage devices, the drift region thickness is increased while the doping concentration is reduced. With lower doping concentrations, the critical electric field reduces which further increases the requirements on the JTE structure design to further relax the peak electric field and thus sustain high voltages. The SM-JTE termination regions are modified by increasing the JTE length to 1800 μm and 2700 μm, respectively, with more implanted Al⁺ rings (i.e., 27 and 36 rings, respectively), as stated in Table 5. The length of the first (dose1) ring is approximately half of the total JTE length, but with minor modifications to obtain equal expansion of the ring pattern (i.e., space and width) for each \( V_B \) class. Otherwise, the simulation settings remained the same with the same ring width and spacing (no width/spacing below 10 μm) as for the 20 kV class diode, only more rings were inserted here. With an ion implantation dose of dose1 = \( 2.6 \times 10^{13} \, \text{cm}^{-2} \), the simulated breakdown voltage of the ultrahigh-voltage diodes are 21.1, 31.0, 41.4, and 51.7 kV, respectively. The leakage current and breakdown voltage characteristics are visualized in Fig. 7. The leakage current is well maintained to very low levels (< 50 nA) up to the blocking voltage avalanche initiation process. The internal electric field profile and impact ionization current distribution in a 50 kV PiN diode are presented in Fig. 8. As for the 20 kV class diode, the initial point of breakdown occurs in the last dose1 region (i.e., \( x \approx 2680 \, \mu\text{m} \)) followed by a redistribution of current closer to the anode contact, at the end of the first dose1. The electric field reaches to 2.35 MV/cm at the initial point of breakdown. Moreover, the simulation results indicate that the space-modulated rings share the electric field well among the rings. The resulting active area and area ratio (i.e., active/total area) of square and circular semiconductor chips are presented in Table 6. A larger active area for circular devices is expected, however, the square chip design is preferred due to simpler manufacturing. Note that, as the epitaxial growth processing evolves and less critical defects are visible, the future generations of SiC devices may be employed as full wafer devices (e.g., in capsule/presspack power modules), similar as for silicon diodes, thyristors, and GCTs, thus 1 inch and 2 inch wafer areas are included in Table 6 for comparison.

C. 40–50 kV CLASS SiC PiN DIODES WITH ESZ-JTE

To achieve ultrahigh blocking voltage capability, the efficient junction termination technique is primarily critical in device design and fabrication so to alleviate the growing influence of electric field crowding at the edges of the device, especially when a packaged device is under continuous high-field stress during operation. Thus, alternative termination structures may
TABLE 6. Area Ratio (i.e., active/total) for 20–50 kV Class Pin Diodes with Respectively One-Sided JTE Length for Different Chip Areas

| V<sub>b</sub> Class (kV) | JTE Length (cm) | Chip Size (cm²) | Circular Chip | Square Chip |
|------------------------|-----------------|----------------|--------------|------------|
|                        |                 |                | Active Area | Active Area |
|                        |                 |                | Area Ratio (%) | Area Ratio (%) |
|                        |                 |                |              |              |
| 20                     | 0.06            |                 | 0.80        | 0.80        |
|                        |                 |                | 80          | 77          |
|                        |                 |                | 1.71        | 1.63        |
|                        |                 |                | 86          | 84          |
|                        |                 |                | 4.60        | 4.54        |
|                        |                 |                | 91          | 90          |
|                        |                 |                | 19.3        | 19.2        |
|                        |                 |                | 95          | 95          |
|                        |                 |                | 5.1 (""')   | 5.1 (""')   |
|                        |                 |                | 4.15        | 4.04        |
|                        |                 |                | 82          | 80          |
|                        |                 |                | 18.4        | 18.2        |
|                        |                 |                | 91          | 90          |
|                        |                 |                | 0.46        | 0.41        |
|                        |                 |                | 46          | 41          |
|                        |                 |                | 1.20        | 1.11        |
|                        |                 |                | 60          | 56          |
|                        |                 |                | 3.73        | 3.58        |
|                        |                 |                | 74          | 71          |
|                        |                 |                | 17.5        | 17.2        |
|                        |                 |                | 86          | 85          |
|                        |                 |                | 0.27        | 0.21        |
|                        |                 |                | 27          | 21          |
|                        |                 |                | 0.88        | 0.76        |
|                        |                 |                | 44          | 38          |
|                        |                 |                | 3.14        | 2.93        |
|                        |                 |                | 62          | 58          |
|                        |                 |                | 16.2        | 15.7        |
|                        |                 |                | 80          | 77          |

FIGURE 9. TCAD simulated breakdown voltages for the ESZ-JTE structure and the SM-JTE structure for different implant doses.

be required for UHV devices, especially as the length and process complexity increases with breakdown voltage capability. Additional processing steps may be required to relax/circumvent issues such as large number of guard rings [23], [24], to small bevel angle [29], [31] and large influence of SiO<sub>2</sub>/SiC surface charges [33], [46], voltage transient stability [47] and/or device degradation/reliability over time [12], [24].

The ESZ-JTE structure for UHV devices is evaluated and compared to the SM-JTE design, both simulated with the same one-sided termination length for each blocking voltage class for fair comparison. Considering a three step etch sequence which results in an eight zone/level ESZ-JTE, where the length of each step/plateau is equally distributed across the complete JTE length, \( l_{JTE, tot}/8 \). Hence, the step length is 225 µm for a 40 kV class diode. With the same implant dose as for the SM-JTE (i.e., dose = 2.6 × 10<sup>13</sup> cm<sup>-2</sup>), the ESZ-JTE achieves breakdown voltages of 38.4 kV and 49.2 kV as shown in Fig. 9, which is slightly lower than for the corresponding SM-JTE structure (i.e., 41.4 kV and 51.7 kV).

The electric field profiles for the SM-JTE, SZNB-JTE, and the ESZ-JTE, here dimensioned for 50 kV class diodes with dose<sub>1</sub> = 2.6 × 10<sup>13</sup> cm<sup>-2</sup>, are demonstrated in Fig. 10 along with the impact ionization current distribution of the ESZ-JTE. The SZNB-JTE structure requires an impractical bevel angle of 0.017° (approximately 20 times lower angle than in [31]) and is only added as a theoretical comparison to the SM-JTE and ESZ-JTE structures. However, the JTE structure reaches 50.0 kV (88% of \( V_{B, PP} \), \( V_{B}/l_{JTE} = 18.5 \) kV/µm. The SZNB-JTE structure shows a relatively uniform electric field distribution up until the electric field peak at approximately \( x = 2250 \) µm, followed by a decreasing electric field towards the edge. Note, that the electric field peak profile for the SM-JTE is non-uniform laterally over the JTE length and reaches the high value 2.25 MV/cm at the JTE edge.

The electric field profile of the ESZ-JTE structure, however, may be engineered with the implant dose level, and thus modifying the peak/inflection point along the JTE length, as demonstrated by the electric field profiles from structures with implant doses in the range of 1.5 × 10<sup>13</sup> to 3.0 × 10<sup>13</sup> cm<sup>-2</sup> in Fig. 11a. The equipotential flux contours of the structures with implant doses of 1.5 × 10<sup>13</sup> and 2.6 × 10<sup>13</sup> cm<sup>-2</sup> are presented in Fig. 11b and Fig. 11c, respectively. Here, the decreasing electric field towards the chip edge, especially for low implant doses, is favorable and may strengthen the operational reliability of a packaged device under long term continuous high-field stress. For the ESZ-JTE structures, a peak field at the outer edge of the JTE of 1.91, 1.65, 1.27, 0.96 and 0.64 MV/cm have been obtained for varying implant doses of 3.0 × 10<sup>13</sup>, 2.6 × 10<sup>13</sup>, 2.0 × 10<sup>13</sup>, 1.5 × 10<sup>13</sup> and 1.0 × 10<sup>13</sup> cm<sup>-2</sup>, respectively. Note, that the minimum implant dose is limited by the growing impact of the electric field (i.e., field increases) close to the active area and enhancing the uniform electric field profile laterally (i.e., in the region up to 1500 µm) that may lead to pre-mature breakdown of the device. Moreover, a relatively flat plateau is visible at/in the
vicinity of the electric field peak and the vertical transitions are smoother (i.e., (MV/cm)/dx) (similar as in [29]) compared to the ES-JTE [19], [30], [37] and MZ-JTE [28], [33], [36]. As stated before, multi-zone JTE structures suffer from high electric field in the steps between the JTE doses. Similarly, in the ES-JTE structures, where the electric field peaks are located in the vertical steps. In the ESZ-JTE structure, the JTE effective dose transitions are on the top-side of the JTE, leaving a smooth junction on the bottom side, which is less sensitive to the submitted electric field. Furthermore, the JTE dose acts effectively as a damping parameter to the vertical steps that is normally the critical part of the implantation-free, etched step termination structure.

The ESZ-JTE simulation results indicate a wider dose window than compared to the SM-JTE method, both for the 40 kV class and 50 kV class diodes. The breakdown voltage reaches above 53.1 kV for an implant dose of 3.0 \times 10^{13} \text{cm}^{-2} and the breakdown termination length efficiency is above 18 V/\mu m for a wide range of implant doses (i.e., doses from 1.0 \times 10^{13} to 3.0 \times 10^{13} \text{cm}^{-2}). Simulations of an ESZ-JTE step height deviation of 1–10 nm per etch step, which is approximately a factor of 2.5–100 larger than etch processing margins (i.e., 0.1–0.4 nm [23], [24], [54]–[57]), results in a blocking voltage deviation of approximately 150–200 V, which indicates a relatively low sensitivity to height processing margins. With this in mind, the ESZ-JTE may be a suitable alternative to SM-JTE, and in addition, the ESZ-JTE structure may be further optimized in different ways. For example, the ESZ-JTE structure has besides the implant dose and implant depth, also the advantage of keeping the etch depth and length of the different regions as process parameters, which may further be used to optimize the device performance. H. Elahipanah et al., have recently, demonstrated that the breakdown voltage can potentially be increased by 20 % by optimizing the length of the termination etch zones, instead of using equally spaced etching lengths, at no extra/added cost [44]. Moreover, implementing a space-modulated pattern with etched trenches similar to [30], [37], [45] is yet another extended concept for further improvement of the ES/ESZ structural design and process. Note, that C.-N. Zhou et al., have demonstrated a higher breakdown voltage for SiC p-GTO thyristors as well as a wider relative remaining dose window (\Delta d/d window) by applying a space-modulated etch-step design (i.e., \( V_B = 13.3 \text{ kV} \) and \( \Delta d/d = 0.52 \)) rather than etching one additional planar step (i.e., \( V_B = 12.9 \text{ kV} \) and \( \Delta d/d = 0.30 \)) [37].

**IV. CONCLUSION**

The one-sided JTE length for UHV SiC PiN diodes has been determined by numerical simulations using the Sentaurus based TCAD design platform. The SM-JTE structure with 27 guard rings and a length of 1800 \mu m is capable to withstand breakdown voltages up to 41.4 kV and the structure with 36 guard rings and with a length of 2700 \mu m is capable to cope with voltages up to 51.7 kV. The presented findings are required to determine the active area of UHV devices, which is a fundamental requirement for comparing devices in benchmarking studies, e.g., between medium voltage devices and UHV devices. The various JTE design categories have been evaluated with consideration on UHV design challenges, resulting in the comparison between the SM-JTE and etch-single-zone JTE structure which demonstrates similar breakdown voltage characteristics. Moreover, a slightly increased dose window margin for the ES design is visible compared to SM-JTE concept. The ESZ-JTE structure with an implanted dose of 3.0 \times 10^{13} \text{cm}^{-2} endures voltages above 53 kV with the same simulation settings as the SM-JTE. The ESZ-JTE may have a more complex manufacturing process with additional etch steps, but offers benefits as several design parameters (i.e., implant dose and etched step pattern, length and depth) to optimize the JTE performance and a decreasing electric field profile towards the outer edge of the chip which may benefit the device transient tolerance (dv/dt, di/dt) and reliability concerns.

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