DEEP LEARNING ON EDGE TPUS

A SURVEY

Yipeng Sun, Andreas M. Kist
Department Artificial Intelligence in Biomedical Engineering
Friedrich-Alexander-University Erlangen-Nürnberg
Germany
yipeng.sun@fau.de, andreas.kist@fau.de

ABSTRACT
Edge computing is important in remote environments, however, conventional hardware is not optimized for utilizing deep neural networks. The Google Edge TPU is an emerging hardware accelerator that is cost, power and speed efficient, and is available for prototyping and production purposes. In this article, we review the Edge TPU platform, the tasks that have been accomplished using the Edge TPU, and which steps are necessary to deploy a model to the Edge TPU hardware. The Edge TPU is not only capable of tackling common computer vision tasks, but also surpasses other hardware accelerators, especially when the entire model parameters can be stored in the Edge TPU memory. Co-embedding the Edge TPU in cameras allows a seamless analysis of primary data. We further discuss future development directions, potential applications and limitations of the Edge TPU. In summary, the Edge TPU is a maturing system that has proven its usability across multiple computational tasks.

Keywords: Edge TPU · Deep Learning · Neural Network · Classification · Semantic Segmentation

1 Introduction

Deep neural networks (DNNs) have revolutionized image processing and computer vision, including object recognition, image classification and semantic segmentation [1–3]. These advances have led to significant paradigm changes, for instance in the field of healthcare [4] and self-driving cars [5]. Different end-to-end deep learning platforms, such as Caffe, TensorFlow and Torch, are important milestones in enabling the machine learning community to use deep neural networks. In particular, high-level packages, such as Keras and PyTorch, lowered the barriers to leveraging DNNs. Even with just a few lines of code, beginners can create, train, and evaluate for example a multilayer perceptron without the need for precise mathematical basics.

However, even with small DNNs the advantage of dedicated hardware, commonly graphical processing units (GPUs) is clear: faster training and inference, sometimes multiple orders of magnitude [6]. This becomes especially important in cases where DNNs are used in constrained environments, such as embedded solutions. Here, dedicated integrated circuits (ICs) will provide more efficient reasoning, i.e., more computation with less power and less latency, thus enabling real-time services. One idea is to utilize flexibly programmable field-programmable gate arrays (FPGAs) [8–10], and another idea relies on dedicated ICs developed specifically for DNNs. Multiple platforms are already available, such as the NVIDIA Jetson family [11], Intel Movidius VPUs [12] and Google’s Edge TPUs [13] using a variety of frameworks [14].

In this overview, we highlight the usage of Edge TPUs across deep neural network architectures and emphasize the authors’ efforts in utilizing Edge TPUs on their specific tasks. We also discuss the future development, potential applications and limitations of Edge TPU.

2 Overview of Deep Learning

In order to explain the techniques discussed in this paper, we first provide a brief overview of deep learning.
Deep Learning on Edge TPUs

Deep learning prediction algorithms, are representational learning methods with multiple levels of representations, which is obtained by composing simple but nonlinear layers, as shown in Figure 1. When the input data passes through the layers, each layer applies matrix operations to it. In most cases, the output of one layer is the input for the next. As a result of the final layer of data processing, a feature or classification output is generated. The neural network are called DNNs when they contains many layers in sequence. [15].

To optimize the parameters of matrix multiplications in each layer, the ground truth, also called training labels, are passed multiple times through the layers from the last layer to the first layer. That means in deep learning training, computations are reversed. A classical technique, Stochastic gradient descent (SGD) is usually used to minimize the error between prediction and ground truth, called training loss, in this case a small batch of samples is randomly selected and used to update the gradient according to the ground truth. With the continuous development of deep learning, more optimization algorithm are being developed. A single pass through the entire training dataset is referred to as a training epoch [16].

During the training of DNNs, numerous calculations are performed, resulting in DNNs models with a large number of parameters, which Leads to latency problems on the device. In addition, there are many choices of hyperparameters on how to design the DNNs model (e.g., number of parameters per layer and number of layers), causing the model design to be challenging. For example, DNNs with higher accuracy may require more memory, while DNNs with fewer parameters may run faster and use fewer computational resources, but can not meet the accuracy requirements of the practical application [17]. This problem was improved with the advent of hardware accelerators based on ICs, optimized specifically for deep learning algorithms, which provide a dramatic increase in the speed of running large-scale parametric models on these hardware accelerateors compared to conventional computing devices.

Figure 1: DNN example of image classification. A picture of a cat is passed into a DNN used to identify dogs and cats, which finally yields a 0.96 probability of being a cat and a 0.04 probability of being a dog.

3 The Edge TPU

The Edge TPU is a new machine learning application-specific integrated circuit (ASIC) with a small footprint of 5 × 5 mm from Google. It allows fast TensorFlow Lite model inference at low power. The available operations on the Edge TPU are constantly growing [18], and are updated regularly. The number of operations currently available (July 2021) is shown in figure 2. Interestingly, over time the ratio of the number of operations with known limitations to all operations supported by the Edge TPU remains constant by approximately 50 %. Among the recent updates, it is worth mentioning that the introduction of long and short-term memory (LSTM) units has enabled the use of recurrent neural networks (RNNs) on the Edge TPU.

With a power consumption of only two watts, the Edge TPU is well suited for low power environments. Specifically, on selected deep neural networks the Edge TPU outperforms other hardware accelerators when measuring images per second per Watt [19]. Each Edge TPU IC can operate at four trillion operations per second (TOPS), resulting in two TOPS per Watt. Currently, multiple hardware platforms are available for prototyping and production purposes (Table 1).

4 Computing on the Edge

With the Coral platform, Google provides a comprehensive library of models that can be directly utilized. Figure 3 shows the tasks that were successfully completed using the Edge TPU. In the following, we will take a closer look to each of the tasks. In general, recent work has focused on comparing the Edge TPU with other hardware accelerators in terms of accuracy, inference time, and power consumption. Specifically, they focus on the compatibility of Edge TPUs
Figure 2: Supported operations by the Edge TPU (black) and operations with known limitations (gray). Dates were retrieved from Wayback Machine and are not actual updates by Coral.

Table 1: Systems for Edge TPU inference

| product                                    | purpose       | vendor         | TOPS | est. costs |
|--------------------------------------------|---------------|----------------|------|------------|
| Dev Board                                  | Prototyping   | Coral / Google | 4    | 129.99 USD |
| Dev Board Mini                             | Prototyping   | Coral / Google | 4    | 99.99 USD  |
| Dev Board Micro                            | Prototyping   | Coral / Google | 4    | 79.99 USD  |
| USB Accelerator                            | Prototyping   | Coral / Google | 4    | 59.99 USD  |
| Mini PCIe Accelerator                      | Production    | Coral / Google | 4    | 24.99 USD  |
| M.2 Accelerator (A+E or B+M key)           | Production    | Coral / Google | 4    | 24.99 USD  |
| M.2 Accelerator (Dual Edge TPU)            | Production    | Coral / Google | 8    | 39.99 USD  |
| System-on-Module (SoM)                     | Production    | Coral / Google | 4    | 99.99 USD  |
| AI Accelerator PCIe Card (8/16 Edge TPUs)  | Production    | Asus           | 32/64| 1200 USD (8) |
| Accelerator Module (IC)                    | PCBs          | Coral / Google | 4    | 19.99 USD  |

with existing architectures. A comprehensive approach was provided in [20]. The authors suggest a new benchmark (EDLAB) to compare hardware accelerators and show that the Edge TPU is leading in power consumption and is essentially equal in accuracy compared to other hardware accelerators. Interestingly, in their study the Edge TPU is slower in inference compared to its competitors, which is contrary to most observations below. Another study performed a bottleneck analysis of the Edge TPU, tested 24 neural networks, and found three shortcomings of the Edge TPU in terms of computational throughput, energy efficiency, and memory access handling. Aiming for improving these issues, they proposed a new framework, Mensa, that improves energy efficiency and throughput by 3.0x and 3.1x over the Edge TPU. It is promising that Mensa could enable the design and adoption of future heterogeneous accelerators, especially Edge TPUs, to support the type of DNNs models that have not yet been developed.

Figure 3: Tasks accomplished using the Edge TPU

Classification

Edge TPU

Semantic Segmentation

Object detection

Pose Estimation

Image Restoration
4.1 Classification

In [22], the authors tested Edge TPUs with multiview convolutional neural networks [23] to classify objects from various views and specialized convolutional neural networks. They found that the Edge TPU outperformed the CPU, ARM CPU and the Intel Movidius NCS by a large margin. The Edge TPU had a latency of less than 5 ms, and was highly power efficient providing 451.8 forward passes per Watt per second [22]. However, the authors did not compare the accuracy of the Edge TPU model (uint8) to the classification accuracy of the competing platforms (float32). In [24], the authors compared different neural architectures for object classification deployed to the Edge TPU. Their results suggest that the combination of Raspberry Pi 3 or 4 with the Edge TPU is feasible across different architectures, allowing an increase in the number of processed frames per second without significant loss in accuracy. The use of Siamese networks on Edge TPUs has been shown in [25], where the authors showed that Edge TPUs are capable of providing inferences at 60 frames per second, and quantization does not hinder the performance. Notably, the authors observed a small increase in performance. The analysis of audio spectrograms on Edge TPUs was assessed by [26], where the authors showed that the Edge TPU is on par in accuracy with CPU-based deep neural networks. However, they also found that the power efficiency of Edge TPUs is superior to CPUs only when the complete set of model parameters are deployed to the Edge TPU [26]. A direct comparison of NVIDIA Jetson Nano and the Edge TPU revealed that architectures that cache their complete parameter set to the Edge TPU SRAM are approximately five times faster (peak inference 417 frames per second) than their Jetson Nano counterpart [27]. In agreement, architectures with uncached parameters were of the same order as the Jetson Nano. In summary, Edge TPU has a great speed advantage over traditional embedded computing processing units in processing classification tasks in remote computing scenarios. However, in the above experiments, they did not compare the accuracy of the Edge TPU model with int8 precision and competitors with float32 precision.

4.2 Object detection

In the COVID-19 pandemic, the automatic detection of face masks is important for the prevention of infections. The authors of [28] showed that a single-shot detector (SSD) [29] with a MobileNetV2 backbone [30] is portable to the Edge TPU to classify detected faces for mask and no-mask in 6.4 ms per frame. A similar configuration was reported in [31]. It is worth mentioning that, the authors tested the MobileNetV2-SSD architecture on the MS COCO dataset and found that the mean average precision (mAP) was for the Edge TPU quantized variant 0.2248, only slightly lower than the float32 competitors (Raspberry Pi 3 mAP 0.2530, with Intel Movidius NCS 0.2459). However, the Edge TPU surpassed the competitors in inference time by providing 55 frames per second. An SSD has been additionally used with MobileNetV1 and MobileNetV2 to analyze wine trunks, where the Edge TPU served as the acceleration module [32]. The average inference time across MobileNets was approximately 20-24 ms, which the authors compared to Tiny YOLO-V3 on an NVIDIA Jetson platform (54 ms). The Edge TPU SSDs also outperformed the Tiny YOLO-V3 in terms of average precision.

4.3 Pose estimation

Real-time pose estimation is a feasible approach in the training of pose-relevant sports to provide immediate feedback to the trainee. In a recent study, the Edge TPU was used to extract pose information from golfing footage [33]. Using a combination of the Edge TPU prediction and a Savitzky-Golay filter, the authors were able to obtain a pose estimation accuracy of up to 81.2 %. Edge TPUs have recently been used for 3D pose estimation [34]. The authors utilized the Edge TPU to allow real-time 3D pose estimation of three persons in a single camera frame at 30 Hz. In detail, each image crop took approximately 4.5 ms, and in each second the Edge TPU-based object detection took another 20 ms.

4.4 Image denoising

The authors of [35] ported TomoGAN [36], a generative adversarial network, to the Edge TPU to denoise X-ray images at the edge. The authors highlighted that quantizing the model decreases the structural similarity index (SSIM) [37]. However, the SSIM can be rescued by fine-tuning the model [35].

4.5 Semantic segmentation

The first description of using Edge TPUs for semantic segmentation was in [38]. The authors mined different segmentation architectures: the SegNet [39], the DeepLabV3+ [40] and the U-Net [41] architecture. Specifically, by dynamically scaling the U-Net architecture, smaller U-Net derivatives can be completely deployed by maintaining high segmentation accuracy [38]. When using large images, the resizing operations on the Edge TPU are mapped to the CPU to avoid precision loss [18]. However, this yields the fact that not all operations are fully mapped to Edge
Deep Learning on Edge TPUs

TPU resulting in slow inference speeds. By using a custom upsampling algorithm consisting of tiling, upsampling and merging, the authors showed that they were able to fully deploy the network to the Edge TPU, dramatically increasing the throughput without a significant drop in segmentation accuracy [38].

5 From TensorFlow/Keras to Edge TPU

5.1 Porting existing and implementing novel architectures

As described in the previous sections, many works have ported existing architectures to the Edge TPUs. However, due to the lack of adequate operations, the one-to-one porting is sometimes neither possible [38] nor desired, as shown in [42]. The authors showed that an Edge TPU-specific version of the EfficientNet-family that uses ordinary convolutions and the ReLU activation function is faster and more accurate compared to the separable convolutions and the swish activation function typically used in EfficientNets [43]. [44] developed a model that estimates the latency of an architecture deployed to the Edge TPU with a high accuracy of 97%. For this model, the authors utilized more than 423,000 unique convolutional neural networks (CNNs) leading to a reliable estimate to allow rapid evaluation of architectural design choices. Accelerator-aware optimization is therefore key for future DNN architectures that are efficient on the Edge TPU.

Table 2 illustrates that most networks available through tf.keras.applications (TensorFlow 1.15 as recommended by Coral) can be easily deployed to the Edge TPU without any further modifications. The code used to generate this table is available at https://github.com/anki-xyz/edgetpu. The Edge TPU compiler in version 16 was used in the Google Colab environment. In detail, MobileNets are the only available networks through tf.keras.applications that are completely mapped to the Edge TPU and do not occupy the full Edge TPU SRAM allowing fast inference. The NASNet family, as well as the Xception architecture have unsupported subpaths early in the graph resulting in limited mapping of operations to the Edge TPU.

| model            | SRAM full | Total OPs | OPs on Edge TPU |
|------------------|-----------|-----------|-----------------|
| MobileNet ✓      | no 39     | 39        |
| MobileNetV2 ✓    | no 72     | 72        |
| DenseNet121      | yes 384   | 384       |
| DenseNet169      | yes 533   | 533       |
| DenseNet201      | yes 622   | 622       |
| InceptionResNetV2| yes 395   | 395       |
| InceptionV3      | yes 162   | 162       |
| NASNetLarge x    | no 1331   | 2         |
| NASNetMobile x   | no 991    | 1         |
| ResNet101        | yes 145   | 145       |
| ResNet101V2      | yes 249   | 249       |
| ResNet152        | yes 213   | 213       |
| ResNet152V2      | yes 368   | 368       |
| ResNet50         | yes 77    | 77        |
| ResNet50V2       | yes 130   | 130       |
| VGG16            | yes 24    | 24        |
| VGG19            | yes 27    | 27        |
| Xception x       | no 128    | 11        |

5.2 Deployment

The deployment of DNNs to the Edge TPU is a multistep process (Figure 4). First, a TensorFlow or Keras model is converted to the TFLITE format. As the model will be quantized (int8 or uint8), the model should be either trained in quantize-aware mode or post-training quantized, where the former is preferred for the best performance. In this step, it may be necessary to provide a representative dataset for effective quantization. Next, the Edge TPU compiler uses the TFLITE file to compile it into a special Edge TPU TFLITE format, deciding which operations are mapped to the Edge TPUs or to the CPU. Even though all operations can be mapped to the Edge TPU, it may happen that weights and parameters have to be transferred to the Edge TPU during inference because of the limited SRAM of the Edge TPU (see also Table 2). Although deployment and inference are platform independent, the Edge TPU compiler needs a UNIX environment. However, one can utilize the Google Colab platform to compile TFLITE files. Typically, the
Deep Learning on Edge TPUs

The purpose of the Edge TPU is inference. Nevertheless, there are two options to retrain the DNN on the Edge TPU to allow transfer learning [45]. One method is the retraining of the last layer using backpropagation and cross entropy. The other method uses weight imprinting. Here, the embedding of the pre-last layer is used to compute the new weights in the final model layer.

Figure 4: Deployment of neural networks to the Edge TPU. Asterix denotes that models should either be trained in quantization aware mode or quantized after conventional training.

6 Embedded Edge TPUs

Edge TPUs can be easily incorporated on PCBs and interfaced with PCIe and USB 2.0. Multiple companies already included Edge TPUs in network-attached storage (NAS) or telematic solutions such as network switches. A very promising application is the integration of Edge TPUs in cameras. These so-called smart cameras allow the direct processing of acquired images and can provide not only the raw image but also direct information about what is in the image. Table 3 provides an overview of commercially available cameras that contain an Edge TPU. The only system that has an industry standard objective mount (C-Mount) is the Vision AI platform. The MP Cam and JeVois cameras are prototyping platforms, whereas the Darcy camera comes in a production-friendly package.

Table 3: Smart cameras with Edge TPUs

| product   | vendor          | camera chip | resolution [px]   | est. cost |
|-----------|-----------------|-------------|-------------------|-----------|
| MP Cam    | Siana Systems   | OV5640      | 2592×1944 (5 MP)  | 275 USD   |
| Vision AI | IMAGO Technologies | -     | 2560×1936 (5 MP)  | 1500 USD  |
| Darcy     | edgeworx        | -           | 1024×768 (0.8 MP) | not known |
| JeVois    | JeVois Inc.     | -           | 1280×1024 (1.3 MP)| 50 USD    |

7 Discussion

7.1 Edge TPUs in Computer Vision

As Figure 3 shows, the current focus and therefore, main application of Edge TPUs is the analysis of images. When deploying DNNs to the Edge TPU, one may observe performance drops that can be rescued by adjusting the architecture [38] or fine-tuning the model [35]. As the Edge TPU is one hardware accelerator out of many, it is important to compare it to other candidates [22, 27, 32], to identify if the Edge TPU is the most appropriate technological platform. Standardized benchmarks, as suggested by [20], for different computer vision tasks, or for identifying power efficiency are crucial to ensure fair comparisons across hardware accelerators. Across most of the studies, the Edge TPU outperformed non-accelerating platforms (CPU, Raspberry Pis) and other hardware accelerators. However, it has to be noted that other hardware platforms have an easier deployment due to the richer repertoire of supported operations (NVIDIA Jetson family supports native TensorFlow) and operate not only in int8 precision. Here, both main competitors, NVIDIA Jetson and Intel Neural Compute Stick 2, are able to use not only int8, but also floating point 16 (FP16) or even FP32 precision (NVIDIA Jetson) as well. This additional accuracy could be crucial on selective tasks, such as identity verification.
7.2 Future applications

The Edge TPU is an embedding-friendly hardware accelerator. Therefore, in future we expect to see more Internet of Things (IoT) devices that will incorporate the Edge TPU. A potential application that has not been touched is the deployment of DNNs with multimodal input, such as videos that contain both, audio and image signals [46]. This is potentially interesting for intelligent vehicles relying on multiple sensors, or medical assessment. We envision that an ideal application for the Edge TPU is the pure inference of large datasets, for example for data categorization by providing high-level embedding [47]. Furthermore, embedding the Edge TPU together with adjacent hardware, such as cameras, is highly promising and the first approaches are already commercially available. This close proximity to the camera hardware allows a manifold of image prepossessing, such as image denoising and restoration, super-resolution applications, and camera setting adjustments. Ideally, the Edge TPU allows the direct analysis of primary data and only transmits the inference results to downstream receivers.

8 Conclusion

The Edge TPU is a powerful platform, especially for accelerating inference on the edge and in remote settings. Despite its major usage in the image analysis domain (Figure 3), DNNs that integrate multiple sources of data are possible. Although the Edge TPU has limitations in supported operations [18] and is limited to int8 precision, with architecture adjustments [38] and fine-tuning [35], one is able to achieve competitive results.

Acknowledgment

Thanks Michael Döllinger, Tobias Schraut and René Groh for their critical comments on the manuscript.

Declarations

Funding

N/A

Conflicts of interest/Competing interests

The authors declare no competing interests.

Availability of data and material

All primary data is available at https://github.com/anki-xyz/edgetpu.

Code availability

All code to generate primary data is available at https://github.com/anki-xyz/edgetpu.

Authors’ contributions

Andreas M. Kist and Yipeng Sun conceived, wrote and edited the article, generated primary data and created figures and tables.

References

[1] Y. LeCun, Y. Bengio, and G. Hinton, “Deep learning,” nature, vol. 521, no. 7553, pp. 436–444, 2015.
[2] T. J. Sejnowski, The deep learning revolution. MIT press, 2018.
[3] A. Garcia-Garcia, S. Orts-Escolano, S. Oprea, V. Villena-Martinez, and J. Garcia-Rodriguez, “A review on deep learning techniques applied to semantic segmentation,” arXiv preprint arXiv:1704.06857, 2017.
[4] A. Esteva, A. Robicquet, B. Ramsundar, V. Kuleshov, M. DePristo, K. Chou, C. Cui, G. Corrado, S. Thrun, and J. Dean, “A guide to deep learning in healthcare,” Nature medicine, vol. 25, no. 1, pp. 24–29, 2019.
Deep Learning on Edge TPUs

[5] Q. Rao and J. Frtunikj, “Deep learning for self-driving cars: Chances and challenges,” in Proceedings of the 1st International Workshop on Software Engineering for AI in Autonomous Systems, 2018, pp. 35–38.

[6] J. Bergstra, F. Bastien, O. Breuleux, P. Lamblin, R. Pascanu, O. Delalleau, G. Desjardins, D. Warde-Farley, I. Goodfellow, A. Bergeron et al., “Theano: Deep learning on gpus with python,” in NIPS 2011, BigLearning Workshop, Granada, Spain, vol. 3. Citeseer, 2011, pp. 1–48.

[7] Y. E. Wang, G.-Y. Wei, and D. Brooks, “Benchmarking TPU, GPU, and CPU Platforms for Deep Learning,” arXiv:1907.10701 [cs, stat], Oct. 2019, arXiv: 1907.10701. [Online]. Available: http://arxiv.org/abs/1907.10701

[8] C. Wang, L. Gong, Q. Yu, X. Li, Y. Xie, and X. Zhou, “Dlau: A scalable deep learning accelerator unit on fpga,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 36, no. 3, pp. 513–517, 2016.

[9] C. Zhang, P. Li, G. Sun, Y. Guan, B. Xiao, and J.Cong, “Optimizing fpga-based accelerator design for deep convolutional neural networks,” in Proceedings of the 2015 ACM/SIGDA international symposium on field-programmable gate arrays, 2015, pp. 161–170.

[10] A. Shawahna, S. M. Sait, and A. El-Maleh, “Fpga-based accelerators of deep learning networks for learning and classification: A review,” IEEE Access, vol. 7, pp. 7823–7859, 2018.

[11] S. Mittal, “A survey on optimized implementation of deep learning models on the nvidia jetson platform,” Journal of Systems Architecture, vol. 97, pp. 428–442, 2019.

[12] S. Kaarmukilan, A. Hazarika, S. Poddar, H. Rahaman et al., “An accelerated prototype with movidius neural compute stick for real-time object detection,” in 2020 International Symposium on Devices, Circuits and Systems (ISDCS). IEEE, 2020, pp. 1–5.

[13] S. Cass, “Taking ai to the edge: Google’s tpu now comes in a maker-friendly package,” IEEE Spectrum, vol. 56, no. 5, pp. 16–17, 2019.

[14] R. Hadidi, J. Cao, Y. Xie, B. Asgari, T. Krishna, and H. Kim, “Characterizing the deployment of deep neural networks on commercial edge devices,” in 2019 IEEE International Symposium on Workload Characterization (IISWC). IEEE, 2019, pp. 35–48.

[15] I. Goodfellow, Y. Bengio, and A. Courville, Deep learning. MIT press, 2016.

[16] S. Ruder, “An overview of gradient descent optimization algorithms,” arXiv preprint arXiv:1609.04747, 2016.

[17] J. Chen and X. Ran, “Deep learning with edge computing: A review,” Proceedings of the IEEE, vol. 107, no. 8, pp. 1655–1674, 2019.

[18] “TensorFlow models on the Edge TPU.” [Online]. Available: https://coral.ai/docs/edgetpu/models-intro/

[19] L. Kljucaric, A. Johnson, and A. D. George, “Architectural Analysis of Deep Learning on Edge Accelerators,” in 2020 IEEE High Performance Extreme Computing Conference (HPEC). Sep. 2020, pp. 1–7, iSSN: 2643-1971.

[20] H. Kong, S. Huai, D. Liu, L. Zhang, H. Chen, S. Zhu, S. Li, W. Liu, M. Rastogi, R. Subramaniam, M. Athreya, and M. Anthony Lewis, “EDLAB: A Benchmark for Edge Deep Learning Accelerators,” IEEE Design Test, pp. 1–1, 2021, conference Name: IEEE Design Test.

[21] A. Boroumand, S. Ghose, B. Akin, R. Narayanaswami, G. F. Oliveira, X. Ma, E. Shiu, and O. Mutlu, “Mitigating Edge Machine Learning Inference Bottlenecks: An Empirical Study on Accelerating Google Edge Models,” arXiv:2103.00768 [cs]. Mar. 2021, arXiv: 2103.00768. [Online]. Available: http://arxiv.org/abs/2103.00768

[22] C. Wisultschew, A. Otero, J. Portilla, and E. de la Torre, “Artificial Vision on Edge IoT Devices: A Practical Case for 3D Data Classification,” in 2019 XXXIV Conference on Design of Circuits and Integrated Systems (DCIS), Nov. 2019, pp. 1–7, iSSN: 2640-5563.

[23] H. Su, S. Maji, E. Kalogerakis, and E. Learned-Miller, “Multi-view Convolutional Neural Networks for 3D Shape Recognition,” arXiv:1505.00880 [cs]. Sep. 2015, arXiv: 1505.00880. [Online]. Available: http://arxiv.org/abs/1505.00880

[24] A. A. Asyraaf Jainuddin, Y. C. Hou, M. Z. Baharuddin, and S. Yussof, “Performance Analysis of Deep Neural Networks for Object Classification with Edge TPU,” in 2020 8th International Conference on Information Technology and Multimedia (ICIMU), Aug. 2020, pp. 323–328.
[26] S. Hosseininoorbin, S. Layeghy, B. Kusy, R. Jurdak, and M. Portmann, “Scaling Spectrogram Data Representation for Deep Learning on Edge TPU,” in 2021 IEEE International Conference on Pervasive Computing and Communications Workshops and other Affiliated Events (PerCom Workshops), Mar. 2021, pp. 572–578.

[27] P. Kang and J. Jo, “Benchmarking Modern Edge Devices for AI Applications,” IEICE Transactions on Information and Systems, vol. E104.D, no. 3, pp. 394–403, Mar. 2021. [Online]. Available: https://www.jstage.jst.go.jp/article/IEICE-E104.D/3/E104.D_2020EDP7160/_article

[28] K. Park, W. Jang, W. Lee, K. Nam, K. Seong, K. Chai, and W.-S. Li, “Real-time Mask Detection on Google Edge TPU,” arXiv preprint arXiv:2010.04427, 2020.

[29] W. Liu, D. Anguelov, D. Erhan, C. Szegedy, S. Reed, C.-Y. Fu, and A. C. Berg, “Ssd: Single shot multibox detector,” in European conference on computer vision. Springer, 2016, pp. 21–37.

[30] M. Sandler, A. Howard, M. Zhu, A. Zhmoginov, and L.-C. Chen, “Mobilenetv2: Inverted residuals and linear bottlenecks,” in Proceedings of the IEEE conference on computer vision and pattern recognition, 2018, pp. 4510–4520.

[31] P. Puchtler and R. Peinl, “Evaluation of Deep Learning Accelerators for Object Detection at the Edge,” in KI 2020: Advances in Artificial Intelligence, ser. Lecture Notes in Computer Science, U. Schmid, F. Klügl, and D. Wolter, Eds. Cham: Springer International Publishing, 2020, pp. 320–326.

[32] A. S. Aguiar, F. N. D. Santos, A. J. M. De Sousa, P. M. Oliveiera, and L. C. Santos, “Visual Trunk Detection Using Transfer Learning and a Deep Learning-Based Coprocessor,” IEEE Access, vol. 8, pp. 77 308–77 320, 2020, conference Name: IEEE Access.

[33] T. T. Kim, M. A. Zohdy, and M. P. Barker, “Applying Pose Estimation to Predict Amateur Golf Swing Performance Using Edge Processing,” IEEE Access, vol. 8, pp. 143 769–143 776, 2020, conference Name: IEEE Access.

[34] S. Bultmann and S. Behnke, “Real-Time Multi-View 3D Human Pose Estimation using Semantic Feedback to Smart Edge Sensors,” Robotics: Science and Systems XVII, Jul. 2021, arXiv: 2106.14729. [Online]. Available: http://arxiv.org/abs/2106.14729

[35] V. Abeykoon, Z. Liu, R. Kettimuthu, G. Fox, and I. Foster, “Scientific Image Restoration Anywhere,” in 2019 IEEE/ACM 1st Annual Workshop on Large-scale Experiment-in-the-Loop Computing (XLOOP), Nov. 2019, pp. 8–13.

[36] Z. Liu, T. Bicer, T. Bicer, R. Kettimuthu, D. Gursoy, D. Gursoy, F. D. Carlo, I. Foster, and I. Foster, “TomoGAN: low-dose synchrotron x-ray tomography with generative adversarial networks; discussion,” JOSA A, vol. 37, no. 3, pp. 422–434, Mar. 2020, publisher: Optical Society of America. [Online]. Available: https://www.osapublishing.org/josaa/abstract.cfm?uri=josaa-37-3-422

[37] Z. Wang, A. Bovik, H. Sheikh, and E. Simoncelli, “Image quality assessment: from error visibility to structural similarity,” IEEE Transactions on Image Processing, vol. 13, no. 4, pp. 600–612, Apr. 2004, conference Name: IEEE Transactions on Image Processing.

[38] A. M. Kist and M. Döllinger, “Efficient biomedical image segmentation on edgetpus at point of care,” IEEE Access, vol. 8, pp. 139 356–139 366, 2020.

[39] V. Badrinarayanan, A. Kendall, and R. Cipolla, “Segnet: A deep convolutional encoder-decoder architecture for image segmentation,” IEEE transactions on pattern analysis and machine intelligence, vol. 39, no. 12, pp. 2481–2495, 2017.

[40] L.-C. Chen, G. Papandreou, F. Schroff, and H. Adam, “Rethinking atrous convolution for semantic image segmentation,” arXiv preprint arXiv:1706.05587, 2017.

[41] O. Ronneberger, P. Fischer, and T. Brox, “U-net: Convolutional networks for biomedical image segmentation,” in International Conference on Medical image computing and computer-assisted intervention. Springer, 2015, pp. 234–241.

[42] S. Gupta and B. Akin, “Accelerator-aware neural network design using automl,” arXiv preprint arXiv:2003.02838, 2020.

[43] M. Tan and Q. V. Le, “EfficientNet: Rethinking Model Scaling for Convolutional Neural Networks,” arXiv:1905.11946 [cs, stat], Nov. 2019, arXiv: 1905.11946. [Online]. Available: http://arxiv.org/abs/1905.11946

[44] A. Yazdanbakhsh, K. Seshadri, B. Akin, J. Laudon, and R. Narayanaswami, “An evaluation of edge tpu accelerators for convolutional neural networks,” arXiv preprint arXiv:2102.10423, 2021.

[45] “TensorFlow models on the Edge TPU - transfer learning on device.” [Online]. Available: https://coral.ai/docs/edgetpu/models-intro/#transfer-learning-on-device
[46] P. Tzirakis, G. Trigeorgis, M. A. Nicolaou, B. W. Schuller, and S. Zafeiriou, “End-to-end multimodal emotion recognition using deep neural networks,” IEEE Journal of Selected Topics in Signal Processing, vol. 11, no. 8, pp. 1301–1309, 2017.

[47] A. Frome, G. Corrado, J. Shlens, S. Bengio, J. Dean, M. Ranzato, and T. Mikolov, “Devise: A deep visual-semantic embedding model,” 2013.