Low Voltage Operating 2D MoS₂ Ferroelectric Memory Transistor with Hf₁₋ₓZrₓO₂ Gate Structure

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Abstract

Ferroelectric field effect transistor (FeFET) emerges as an intriguing non-volatile memory technology due to its promising operating speed and endurance. However, flipping the polarization requires a high voltage compared with that of reading, impinging the power consumption of writing a cell. Here, we report a CMOS compatible FeFET cell with low operating voltage. We engineer the ferroelectric Hf₁₋ₓZrₓO₂ (HZO) thin film to form negative capacitance (NC) gate dielectrics, which generates a counterclock hysteresis loop of polarization domain in the few-layered molybdenum disulfide (MoS₂) FeFET. The unstabilized negative capacitor inherently supports subthermionic swing rate and thus enables switching the ferroelectric polarization with the hysteresis window much less than half of the operating voltage. The FeFET shows a high on/off current ratio of more than 10⁷ and a counterclockwise memory window (MW) of 0.1 V at a minimum program (P)/erase (E) voltage of 3 V. Robust endurance (10³ cycles) and retention (10⁴ s) properties are also demonstrated. Our results demonstrate that the HZO/MoS₂ ferroelectric memory transistor can achieve new opportunities in size- and voltage-scalable non-volatile memory applications.

Keywords: Nonvolatile memory, Ferroelectric, MoS₂, 2D, Field-effect transistor, HZO

Background

The system on chip (SoC) embedded memory market is currently in an era of tremendous growth, which requires the memory are capable of achieving faster operation, smaller cell size, and less power consumption [1–6]. Ferroelectric memory, one of the most promising candidates, has been reconsidered, due to the discovery of ferroelectric hafnium oxide in 2011 [7].

In the past decades, FeFET did not perform well in all these aspects includes low voltage requirements for memory operation, process step’s simplicity, and minimally complementary metal-oxide-semiconductor (CMOS) integration process and limited contamination concerns [8–11]. To address this, recently, tremendous investigation on 2D FeFET nonvolatile memory (NVM) has been performed based on various ferroelectric materials, including PbZrTiO₃ (PZT), and [P(VDF-TrFE)] polymer [12–18], which is due to the promising properties of 2D material in “more than Moore era.” In the FeFET, the two stable spontaneous polarization states of a ferroelectric material incorporated into a transistor gate stack are utilized for data storage via the controllable threshold voltage enabled by applied shrunken P/E gate voltages. It is reported that the reproducible hysteresis behaviors, a high on/off ratio of 10⁴, good retention properties up to 10⁸ s, and stable switching operation have been achieved in PZT/MoS₂ FeFET [19]. Noticeably, a maximum mobility of 625 cm²/V·s, a large MW of 16 V for a ± 26 V gate—voltage range and a high on/off ratio of 8 × 10⁵ have also been demonstrated by an n-type [P(VDF-TrFE)] polymer/MoS₂ FeFET [15]. However, there are so many fundamental issues, which could prevent its practical application, like, CMOS
compatibility, scaling capability, and the interface states between Fe and 2D material. Ferroelectric hafnium oxide, a kind of novel ferroelectric material, has excellent CMOS compatibility and scaling capability, which could serve for the advanced FeFET NVM at sub-5 nm technology node in the next 5-10 years [20]. Accordingly, a batch of HfO₂-based dielectric stacks have been incorporated into 2D FeFETs, which are targeted to achieve negative capacitance field-effect transistors (NCFET) with steep ON/OFF switching via sub-60 mV/decade slope and hysteresis-free characteristics [21–26]. Although mass experiments based on NC dielectric stack with alternate 2D channel materials have drawn fantastic conclusions, they highlighted the surge requirements to distinguish between NCFET’s and FeFETs. There is still a lack of systematical investigation regarding the physics and viability of the device technology on one-transistor ferroelectric memory based on MoS₂ and ferroelectric HZO.

In this work, a FeFET with a few-layered HZO MoS₂ transistor has been proposed. It is capable of scaling the P/E voltage via the NC effect induced by gate stack engineering under a shrunken P/E voltage. We experimentally demonstrated that a counterclockwise MW of 0.1 V with sub-60 mV/decade slope has been achieved in HZO MoS₂ FeFET, which can be attributed to local carrier density modulation in the 2D channel by fast flipping of ferroelectric dipole. We attributed the decreased hysteresis of the HZO/MoS₂ FeFET as drain voltage increasing to negative drain-induced barrier lowering (DIBL) effect. In addition, it was also systematically studied retention, endurance characteristics, and the dependence of the threshold voltage on the drain voltage of HZO MoS₂ FeFET, opening a feasible pathway to design HZO MoS₂ FeFET NVM and its practical applications.

**Methods**

6 nm Hf₁⁻ₓZrₓO₂ film and 2 nm Al₂O₃ was deposited on p⁺ Si substrate using ALD at 300 °C, with [(CH₃)₂N]₄Hf(TDMAHf), [(CH₃)₂N]₄Zr(TDMAZr), and H₂O vapor as the Hf precursor, Zr precursor, and oxidant precursor, respectively. Subsequently, the substrate underwent rapid thermal annealing (RTA) at 450 °C for 30 s in N₂ ambient. After that, few-layer MoS₂ flakes were mechanically exfoliated and transferred onto the substrate. The diameter of p⁺ Si substrate used to deposit HZO (6 nm)/Al₂O₃ (2 nm) is 6 inches. We employed electron beam lithography (EBL) to pattern contact pads in poly(methyl methacrylate) (PMMA) A5 resist. The spin parameters, baking parameters, and imaging parameters are 500 r/min (9 s) + 4000 r/min (40 s), 170 °C (5 min), MIBK:IPA = 1:3 (15 s), respectively. Then, the source/drain electrodes (Ti/Au, 5/65 nm thickness) were evaporated using an e-beam evaporation (EBE) system and etched by acetone solution. After lift-off, the device was annealed at 300 °C for 2 h to enhance the contact. We carried out the electrical characterization of our fabricated MoS₂/HZO field-effect transistors using a probe station with a micromanipulator. The back gate voltage (V_GS) was applied on the p type heavily doped Si substrate. A semiconductor characterization system (PDA) was used to measure the source-drain voltage (V_DS), the back gate voltage (V_GS), and the source–drain current (I_DS).

**Results and Discussion**

We prepared a few-layer MoS₂ by mechanical exfoliation of bulk crystal and transferred the MoS₂ nanoflake onto the 2 nm Al₂O₃/6 nm HZO/p⁺ Si substrate (see more details in the “Experimental” section). Figure 1a and b display a 3D schematic view and cross section of the HZO/ MoS₂ FeFET structure, respectively. A top-view scanning electron microscopy (SEM) image of the HZO/MoS₂ FeFET is shown in Fig. 1c. The width and length of the MoS₂ channel are 2 μm and 12 μm, respectively. As shown in Fig. 1d, the thickness of the MoS₂ channel was confirmed using atomic force microscopy (AFM). The measured thickness of 1.57 nm indicates the presence of 4 layer of MoS₂ [26].

As shown in Fig. 1c and d, the elemental and bond composition of HZO was examined by the X-ray photoelectron XPS) measurements. Peaks are found to be 19.05 eV, 17.6 eV, 185.5 eV, and 183.2 eV, which correspond to the Hf 4f½, Hf 4f½, Zr 3d½, and Zr 3d½, respectively [27]. The atomic concentration along the depth profile in Fig. S1e further confirms the distribution of the Al₂O₃/HZO/p⁺ Si tri-layer structure. All the above confirm that the HZO film grown via our atomic layer deposition (ALD) system is highly crystalline.

Before investigating the characterization of HZO/ MoS₂ FeFET, the ferroelectric behavior of the Au/2 nm Al₂O₃/6 nm HZO/p⁺ Si gate stack using polarization-voltage measurement is shown in Fig. 2a. Clearly, our fabricated 6 nm HZO/2 nm Al₂O₃ capacitors exhibit polarization-voltage hysteresis loops (measured at 1 kHz). Meanwhile, the remnant polarization P_r and the coercive voltage V_c increase with increasing the maximum sweeping voltage, implying the P-V hysteresis loops transform from minor loop to major loop. As the maximum sweeping voltage increases from 2 to 4 V, P_r reaches 0.66 μC/cm², 0.86 μC/cm², and 1.1 μC/cm², respectively and V_c reaches 1.12 V, 1.9 V, and 2.04 V, respectively. Extracted P_r and V_c within 10⁵ enduring DC sweeping cycles are shown in Fig. 2b and c. Obviously, significant wake-up and fatigue effects within 10⁵ cycles are observed in the 6 nm HZO/2 nm Al₂O₃ capacitor. The wake-up and fatigue can be attributed to the diffusion and redistribution of the oxygen vacancies under the electric field. The fatigue effect is generally...
associated with charge trapping at the defect sites related to oxygen vacancies [28]. The hysteresis behaviors for the \( PRphase \) and butterfly-shaped loop for the \( PRampl \) using piezoresponse force microscopy (PFM) are displayed in Fig. S1b and c, indicating a polarization switching as a function of the sweep bias voltage. Considering different contact resistances between polarization-voltage measurement and piezo response-voltage measurement, the measured \( V_c \) in Fig. S1b and c is not so consistent with the values obtained in Fig. 2a.

Additionally, it is observed that there is an increase in MW accompanied with the raised sweeping voltage range of gate voltage (\( V_{GS,range} \)). Usually, poly-crystal HZO film exists as multi-domain status [29], and the coercive field distribution of these domains satisfies Gaussian distribution. Thus, there must be an increased dependence on the raised \( V_{GS,range} \). The coercive filed \( E_C \) corresponds to the value of the external electric field which can reduce the remanent polarization to zero. Therefore, the \( V_{GS,range} \) used to switch the polarization in the HZO film becomes larger with higher related coercive voltage \( V_C \). This is the reason why polarization-voltage loops of HZO film are extended with a larger \( V_{GS,range} \), which has been demonstrated in Fig. 2a. In other words, the enhanced polarization intensity and ferroelectric switching occur with the raised \( V_{GS,range} \).
leading to the aforementioned phenomena of the extended counterclockwise MW produced by the increased $V_{GS,\text{range}}$. At $V_{GS,\text{range}} = (-2, 2 \, V)$, the MW are almost vanished and nearly hysteresis-free characteristics emerge, which means the almost complete compensation between the effects of ferroelectric switching and charge trapping/de-trapping.

In order to further investigate the effect of ferroelectric switching, the $V_{GS,\text{range}}$ has been continuously increased to $(-6, 6 \, V)$ and $(-6.5, 6.5 \, V)$. The measured $I_{DS}$-$V_{GS}$ curves of the HZO MoS$_2$ FeFET at $V_{GS,\text{range}} = (-6, 6 \, V)$, and $(-6.5, 6.5 \, V)$ are shown in Fig. 3a. Similarly, the counterclockwise memory window is increased with the extended $V_{GS,\text{range}}$. At $V_{GS,\text{range}} = (-6.5, 6.5 \, V)$, the counterclockwise MW is above 4 $V$ and the on/off ratio also increases to $10^7$, which is due to the enhanced polarization switching under a larger external applied voltage. Generally, the mechanism underlying the hysteresis behaviors shown in the $I_{DS}$-$V_{GS}$ curves during the bi-direction sweeping of $V_{GS}$ is threshold voltage shift, which can be modified by the predominant effects of polarization switching, that is NC effect [30–32], resulting in counterclockwise hysteresis. A further study of improved subthreshold characteristics was carried out in the other device under a shrunken $V_{GS,\text{range}}$. The measured $I_{DS}$-$V_{GS}$ and extracted point SS-$I_{DS}$ curves of the other device at $V_{GS,\text{range}} = (-3, 3 \, V)$ are plotted in Fig. 3b. It is demonstrated that at $V_{GS,\text{range}} = (-3, 3 \, V)$, HZO/MoS$_2$ FeFET exhibits SS$_{\text{For}} = 51.2 \, \text{mV/decade}$ and SS$_{\text{Rev}} = 66.5 \, \text{mV/decade}$, respectively. That is to say, the SS of sub-60 mV/decade and a MW of 0.48 $V$ can be simultaneously achieved in HZO/MoS$_2$ FeFET at room temperature, which will be a hint to distinguish between NCFET and FeFET.

As it is known, in NCFET, the SS can be smaller than 60 mV/decade at room temperature due to the incorporation of the negative gate dielectric capacitance ($C_{\text{ins}}$), which can be obtained via the negative slope segment of $dP/dE < 0$ induced by ferroelectric film, contributing to the gate stack factor (m) < 1. The mechanism underlying the NC effect [33] is the depolarization field generated by ferroelectric film [34–38]. It is experimentally reported that due to the incomplete screening at the interface of ferroelectric film [39], the residual polarization charge could produce an internal electrical field across ferroelectric film, which has the opposite direction with the externally applied voltage, leading to the re-distribution of the voltage across the gate stack and the amplified channel surface potential, named as “voltage amplification effect” [40–42]. The voltage amplification usually can be divided into two parts, the accelerated variation of channel surface potential and the subsequent boosted value, providing the steep ON/OFF switching and improved $I_{\text{ON}}$/$I_{\text{OFF}}$, respectively. However, for FeFET, there is another story. According to the concept of capacitance matching between ferroelectric capacitance ($C_{\text{FE}}$) and metal-oxide-semiconductor capacitance ($C_{\text{MOS}}$) [43–45], when $|C_{\text{FE}}| > C_{\text{MOS}}$, the theoretical total capacitance ($C_{\text{total}}$) is positive and the system is stable, resulting in the same polarization behaviors during the bi-direction sweeping of $V_{GS}$ and the stable hysteresis-free NCET. However, good matching resulting in improved SS and transconductance is very tricky to achieve, since both $C_{\text{MOS}}$ and $C_{\text{FE}}$ are very non-linear, bias dependent capacitors. Additionally, $|C_{\text{FE}}| > C_{\text{MOS}}$ needs to be ensured for all the operating voltage range to avoid hysteresis. Instead, once $|C_{\text{FE}}| < C_{\text{MOS}}$, the theoretical $C_{\text{total}}$ is negative and the system is unstable, a separated polarization behavior must occur during the bi-switching of $V_{GS}$ to keep the $C_{\text{total}}$ positive, which could

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**Fig. 3** The direct current (DC) test of the HZO/MoS$_2$ FeFET when drain voltage ($V_{DS}$) is 0.5 $V$. (a) The comparison between transfer curves with 6 $V$ and 6.5 $V$ as maximum of the back gate voltage. (b) Enlarged view of transfer curves at 0 to $-2 \, V$ interval of $V_{GS,\text{range}} = (-3, 3 \, V)$. Point subthreshold slope (SS) as a function of drain current ($I_{DS}$) of the HZO/MoS$_2$ FeFET is (b) inset. The device exhibits SS$_{\text{For}} = 51.2 \, \text{mV/dec.}$
produce the counterclockwise hysteresis in FeFET for NVM application. Here, it is mentioned that the hysteretic behaviors is the subsequent effect of separated polarization switching, which means that the width of hysteresis window can be easily modified based on the concept of capacitance matching, such as, which can be manipulated by the variation of $V_{DS}$. With an appropriate capacitance matching, even with a much shrunk $V_{GS, range} = (-3, 3 \, \text{V})$, HZO/MoS$_2$ FeFET still exhibits an obvious hysteresis window, and the steep switching of $SS_{for} = 51.2 \, \text{mV/dec}$ at the same time, which further suggests the existence of the NC effect (ferroelectric polarization effect) in the subthreshold region as well. Although NCFET and FeFET are different, FeFET can also be adopted as logic devices with a comparable smaller MW, maintaining a deep sub-60 mV/dec $SS$, and a higher $I_{ON}/I_{OFF}$ ratio as well due to NC effect.

The impact of $V_{DS}$ on the width of MW has been carefully investigated. The $I_{DS}-V_{GS}$ curves on logarithmic scales under different $V_{DS}$ are characterized in Fig. S3. It is exhibited that, at a fixed $V_{GS, range} = (-2, 2 \, \text{V})$, the values of $V_{GS}$ extracted at $I_{DS} = 70 \, \text{nA}$ for the bidirectional sweeping of $V_{GS}$ all shift to the negative direction. Meanwhile, it is also demonstrated that the variation in forward sweeping of $V_{GS}$ is much more obvious over that of reverse sweeping, indicating the significant phenomena of negative DIBL. It should be noted that the negative DIBL effect always occurs with a NC effect [46, 47].

After the above direct current (DC) test of the HZO/MoS$_2$ FeFET, we further carried out the measured MWs for different P/E $V_{GS}$ pulses with 10 ms width in Fig. 4a. MW is defined as the maximum change $\Delta V_{TH}$ after P/E $V_{GS}$ pulses. During the pulsed $V_{GS}$ application, the other terminals were fixed to $V_S = V_D = 0 \, \text{V}$. For the read (R) operation, $V_{GS}$ was ranged from $-1 \, \text{V}$ to $1 \, \text{V}$ with $V_D = 0.5 \, \text{V}$ and $V_S = 0 \, \text{V}$. As shown in Fig. 4a, the extracted MWs become larger as P/E $V_{GS}$ pulses increase. When the imposed P/E $V_{GS}$ pulse is $\pm 3 \, \text{V}$, the extracted MW is $0.1 \, \text{V}$. When the imposed P/E $V_{GS}$ pulse is $\pm 5.5 \, \text{V}$, the extracted MW is $0.275 \, \text{V}$. Compared with the counterclockwise MWs of $4 \, \text{V}$ and $0.48 \, \text{V}$ in Fig. 3a and b, the extracted MWs after P/E $V_{GS}$ pulse is greatly reduced. This is possibly due to a higher density of trapping states induced by high humidity in the air [48]. Thus, the charge trapping/de-trapping mechanism is enhanced and the counterclockwise hysteresis loop is decreased eventually. Furthermore, we studied the cycling endurance and data retention of the HZO/MoS$_2$ FeFET under P/E pulses with $\pm 5.5 \, \text{V}$ height in Fig. 4b. The program $V_{GS}$ pulse was $10 \, \text{ms}$ wide with $V_S = V_D = 0 \, \text{V}$. Figure 4b

![Fig. 4](image)

Fig. 4 Memory performances of the HZO/MoS$_2$ FeFET under P/E pulses. a Extracted MWs (MWs) under P/E pulses with $\pm 3 \, \text{V}$, $\pm 4 \, \text{V}$, $\pm 5 \, \text{V}$, and $\pm 6 \, \text{V}$ heights. b Endurance measurements under P/E pulse conditions. c Retention characteristic of the HZO/MoS$_2$ FeFET. d Endurance of the HZO/MoS$_2$ FeFET for $10^3$ cycles under the P/E pulses with $\pm 3 \, \text{V}$ heights.
illustrates the measured MWs as a function of endurance cycles. The endurance cycle is formed by back-gate voltage periodic P/R/E/R pulses. Voltages applied to the back gate of the height of P, E, R were $+5.5 \text{ V}$, $-5.5 \text{ V}$ and $0 \text{ V}$, respectively. And the pulse width of P and E was $10 \text{ ms}$. Clearly, an MW of $0.3 \text{ V}$ can be maintained without significant degradation after $10^3 \text{ P/E cycles}$. As the number of endurance cycle increased, the MW increases to $0.38 \text{ V}$ after $10 \text{ cycles}$ and then decreases back to $0.28 \text{ V}$ after $600 \text{ cycles}$. The first broaden MW is called wake-up effect and the later shrunken MW is called fatigue effect. The wake-up effect corresponds to domain-wall de-pinning, leading to an increase of switchable polarization domains of the HZO film [49]. The fatigue effect corresponds to newly injected charges that pin the domain walls after great numbers of P/E cycles [50]. The data retention at room temperature is shown in Fig. 4c. Here, the MW degradation is negligible after $10^4 \text{ s}$. Therefore, a MW about $0.3 \text{ V}$ can be expected to be sustainable over 10 years by the dotted extrapolation lines. As presented in Fig. 4d, the device is stable after $10^3 \text{ cycles}$ under the P/E pulses with $\pm 3 \text{ V}$ heights. The stability of the HZO/MoS$_2$ FeFET shows a great perspective of applications in nonvolatile memory technology.

A comparison of figure-of-merit with FeFET-based devices combining MoS$_2$ and ferroelectric gate dielectrics is provided in Table 1. Here, the device structure, remnant polarization, coercive electric field, hysteresis loop direction, MW, working voltage, endurance cycles, and retention time are listed. It is obvious that the device we fabricated exhibits the thinnest ferroelectric layer of 6 nm HZO and the lowest working voltage compared with other works [12–18], which is important for the future 2 nm or 3 nm process node of the back end of line (BEOL) memory. By scaling the thickness of the ferroelectric layer, a MW of about $0.1 \text{ V}$ was achieved under a low working voltage of $\pm 3 \text{ V}$. Such a low working voltage can be attributed to the intrinsic characteristics of HZO layer compared with their counterparts, such as P(VDF-TrFE) or HfO$_2$, which has much higher thickness. Furthermore, our device possesses lower remnant polarization $P_{r}$ of $1.1 \mu \text{C/cm}^2$ compared with other reported FeFETs. The fast decay of retention loss in a FeFET is due to the existence of depolarization field $E_{dep}$ which comes from the incomplete charge compensation due to the existence of the Al$_2$O$_3$ layer. Here, $E_{dep}$ is directly proportional to the remanent polarization $P_{r}$ [51]. Thus, the high $E_{c}$ and low $P_{r}$ make the ratio $E_{dep}/E_{c}$ in MoS$_2$/HZO FeFET much small, leading to a much small retention loss associated with the depolarization field effect. Although the retention performances of MoS$_2$ FeFETs based on HZO and P(VDF-TrFE) are both around $10^5 \text{ s}$, the P(VDF-TrFE) film needs to be 150 nm [17].

**Conclusions**

In conclusion, we investigated few-layered, MoS$_2$-based ferroelectric memory transistor devices using an HZO back gate dielectric. Our fabricated devices exhibit counterclockwise hysteresis induced by ferroelectric polarization. In addition, our HZO/MoS$_2$ ferroelectric memory transistor displayed excellent device performances: a high on/off current ratio of more than $10^7$ and a counterclockwise MW of $0.1 \text{ V}$ at a P/E voltage of 3 V, which has the endurance ($10^3 \text{ cycles}$) and retention ($10^4 \text{ s}$) performance. We

| Table 1 Comparison among the figure of merits of ferroelectric FETs based on MoS$_2$. |
|---|---|---|---|---|---|---|---|
| MoS$_2$ (thickness) | Ferroelectric layer (thickness) | Control gate (position) | $P_r$ ($\mu \text{C/cm}^2$) | $E_c$ (MV/cm) | Hysteresis | MW [V] | Working voltage [V] | Endurance [cycles] | Retention [s] | Ref. |
| few layers | HZO (6 nm) | P$^+$ Si (back) | 1.1 | 1.62 | Counter-clockwise | 0.3 | ± 5.5 | $10^3$ | $10^4$ | This work |
| 3 L | PZT (100 nm) | SrRuO$_3$ (back) | 65 | 2 | Counter-clockwise | 20 | (−10, 30) | − | − | [12] |
| 4 L | PZT (260 nm) | Pt (back) | 56.03 | 8 | Clockwise | 2.5 | ± 4 | − | − | [13] |
| 3 L | P(VDF-TrFE) ($\approx$ 300 nm) | Al (top) | 7 | 0.75 | Counter-clockwise | 25 | ± 40 | − | − | [14] |
| 5 L | P(VDF-TrFE) (220 nm) | Au (top) | 6.5 | 0.55 | Counter-clockwise | 16 | ± 26 | − | 600 | [15] |
| 1 L | P(VDF-TrFE) (200 nm) | Al (top) | 10 | 0.5 | Counter-clockwise | 15 | ± 20 | − | $10^3$ | [16] |
| Several layers | P(VDF-TrFE) (150 nm) | Pt/Si (back) | 8 | 0.6 | Counter-clockwise | 16 | ± 26 | $10^3$ | $3 \times 10^4$ | [17] |
| 1 L | Al doped HfO$_2$ (16 nm) | P$^+$ Si (back) | 3 | 1.5 | Counter-clockwise | 0.125 | ± 10 | $2 \times 10^4$ | − | [18] |
| 3 L | P(VDF-TrFE) (100 nm) | P$^+$ Si (back) | 40 | 0.3 | Clockwise | 4.5 | ± 6 | 500 | $10^4$ | [19] |
thus believe that the results of our MoS2-based non-volatile ferroelectric memory transistors exhibit promising perspectives for the future of 2D low-power non-volatile memory applications.

 Supplementary Information
Supplementary information

Additional file 1: Supplementary Information. Characterization of ferroelectric HZO substrate and more transfer curves of the HZO/MoS2 FeFET(PDF). Fig. S1 a Optical image of the MoS2/HZO FeFET. b PRphase and c PRampl of the HZO capacitor. XPS analysis of the 2 nm Al2O3/6 nm HZO/2p* Si shows pristine d Hf and e Zr peaks. f XPS depth profile of the Al2O3/HZO/2p* Si tri-layer structure. A top-view optic image of the HZO/MoS2 FeFET is shown in Fig. S1a. As shown in Fig. S1b and c, PRphase and PRampl of the HZO capacitor suggest ferroelectric behavior after 450 °C rapid thermal annealing (RTA) measured at 1MHz. As shown in Fig. S1d and e, the elemental and bond composition of HZO were examined by the X-ray photoelectron (XPS) measurements. Peaks are found to be 19.05 eV, 17.6 eV, 185.5 eV, and 183.2 eV, which correspond to the Hf 4f, Zr 4f, Zr 3d 3/2 and Zr 3d 5/2, respectively [27]. The atomic concentration along the depth profile in Fig. S1f further confirms the distribution of the Al2O3/HZO/2p* Si tri-layer structure. All the above confirm that the HZO film grown via our ALD system is highly crystalline. Fig. S2. Transfer curves of the HZO/MoS2 FeFET at increasing gate voltage (Vg,DS) ranges with the linear y-axis. For a start, the transfer curves of the HZO/MoS2 FeFET under different back gate voltage sweep ranges (VGS,range) and different drain voltages (VDS) have been characterized in Fig. S2. It is demonstrated that, the counterclockwise hysteresis windows have been obtained at various gate voltage range (Vg,range) from (-5, 5V) to (-2, 2V).

Simply, the mechanism underlying the hysteretic behaviors shown in the transfer curves during the bi-direction sweeping of VDS is threshold voltage shift, which can be modified by the effects of trapping/de-trapping [52] and polarization switching [53]. If the applied voltage is not high enough to switch the polarization in HZO film, charge trapping/de-trapping mechanism dominates and will cause clockwise hysteresis. The energy band at the interface between the MoS2 channel and ferroelectric back gate tends to bend downward after the positive back gate voltage. The more traps located below the Fermi-level, the more electrons are captured close to the interface. This will increase the threshold voltage after the positive gate pulse. The energy band at the interface between the MoS2 channel and ferroelectric back gate tends to bend upward after the negative back gate voltage. The more traps locate above the Fermi-level, the more electrons are released close to the interface. This will decrease the threshold voltage after the negative gate pulse [52]. If the applied voltage exceeds the coercive voltage in the HZO film, ferroelectric polarization mechanism dominates and will cause anti-clockwise hysteresis window [54–57]. Thus, it is easily concluded that the electrical performance of the device shown in Fig. S2 is dominated by ferroelectric switching. When the back-gate sweeps are in small ranges of 2V in Fig. S2a, we observed the nearly hysteresis-free switching. The hysteresis loops in Fig. S2b are counterclockwise for the back-gate sweep range of 6 V from -3 V to 3 V. The minimum voltage under the drain is VDS = 2 V at Vg,DS = 2 V with Vg,DS = 1 V, which should be larger than the coercive voltage Vc to switch the ferroelectric at the drain side. The estimated coercive voltage is consistent with Vc, of 1.9 V when the maximum sweeping voltage is 3 V in Fig. 2a. When the applied voltage in HZO film exceeds +Vc, the ferroelectric polarization points into the MoS2 channel. Therefore, the electron charges in the MoS2 channel accumulate and the threshold voltage decreases. When the applied voltage in HZO film exceeds −Vc, the ferroelectric polarization points away from the MoS2 channel. Therefore, the electron charges in the MoS2 channel deplete and the threshold voltage increases. Nonetheless, we observed that the wider back-gate voltage range leads to larger counterclockwise hysteresis loops in Fig. S2c and d. Due to the increment of Vc in Fig. 2a with increasing applied voltage, the ferroelectric polarization switching in the HZO film can be enhanced with a larger shift in threshold voltage. Fig. S3 Transfer curves of the HZO/MoS2 FeFET on logarithmic scales with a VDS = 0.05 V, b VDS = 0.2 V, c VDS = 0.4 V, d VDS = 0.2 V, and e VDS = 0.4 V. The drain current (IDS) equals to 70 nA with different VDS. Notably, besides the impact of Vg,range, it is found that VDS can definitely adjust the memory window as well, which requires a further investigation. The IDS-VDS curves on logarithmic scales under different VDS are characterized in Fig. S3. It is exhibited that, at a fixed Vg,range = (-2, 2 V), the values of VDS extracted at IDS = 70 nA for the bi-directional sweeping of VDS all shift towards the negative direction and the variation in forward sweeping of VDS is much more obvious over that of reverse sweeping, indicating the significant phenomena of negative drain induced barrier lowering (DBL) [46, 58–61]. Generally, DBL is a conventional short channel effect. With a short enough channel length, the increased VDS can easily push down the barrier between source/drain and enable a negative shift of threshold voltage, which is the so called effect of DBL. However, for a ferroelectric FeFET, an increased VDS is capable of producing a reduction of channel surface potential via the coupling between gate and drain induced by the parasitic capacitance between gate and drain (CGD), which means a positive shift of threshold voltage and can be called as negative DBL.

Authors’ Contributions
Y.L. and X.W conceived the idea. S.Z fabricated the devices and performed measurements. J.R.Z. and M.M helped measure the devices. B.Z, L.L. and X.S helped to sample preparation and device fabrication. G.H., J.C.Z., Y.S. and Y.H supervised this project. All authors discussed and analyzed the data. S.Z, Y.L., J.R.Z., and X.W wrote the paper. The author(s) read and approved the final manuscript.

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Availability of Data and Materials
The authors declare that the materials, data, and associated protocols are available to the readers, and all the data used for the analysis are included in this article.

Competing Interests
The authors declare that they have no competing interests.

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