Performance Enhancement in Active Power Filter (APF) by FPGA Implementation

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Abstract — The generated electrical power in present days is not able meet its end user requirement as power demand is gradually increasing and expected to be increasing more in future days. In the power quality management the parameters/factors like harmonic currents (HC) and reactive power (RP) yields the major issues in the power distribution units causing transformer heating, line losses and machine vibration. In order to overcome these issues several control mechanisms has been presented and implemented in recent past. The mechanism procedure based on synchronous reference frame (SRF) offers better response by dividing the HC and RP. But the SRF based mechanism procedure requires better synchronization among the utility voltage and input current. To achieve this, the existing researches have used digital signal processing (DSP) and microcontroller but these systems fails to provide better performance as they face issues like limited sampling time, less accuracy and high computational complexity. Thus, to enhance the performance of active power filter (APF) we present FPGA based methodology. Also, the performance authorization of the proposed approach, we have used Xilinx 14.7 and Modelsim (6.3f) simulator and compared with the work of [14]. From the results analysis it is found that the approach has got better performance than [14].

Keyword: Active Power Filter, FPGA, PLL and Directed Current Control.

I. INTRODUCTION

The role of power electronics in power system has been widespread in almost all the sectors like industries, commercials etc. But, when the end users load of power system is non-linear these power electronics devices generates harmonic currents (HC) and reactive power (RP) and which impacts on the power quality [1]. Hence, to resolve the HC and RP issues and achieve the significant power quality passive filters (PF) were designed. but, PFs lags with the some of the issues concerning size, fixed compensation and resonance problems. These limitations of the PF has lend towards the design of active filters (AF) [2, 3]. The AF has got more significant features over the PF to tackle the power quality issue. The power quality indicates the interaction between source power and hardware component.

- The undamaged operation of power system at normal operating condition is known as good power quality.

- In case the hardware is malfunctioned /damaged in power system at normal operation then it is power of poor quality.

The power quality represents wellness of electrical power towards end user devices. The main reason for the power quality issues is harmonic waveforms. The power harmonics exhibit different undesirable consequences in the distribution system [5]. The harmonic waveforms causes various issues like voltage distortion, higher voltage stresses, resistive losses, lower motor proficiency etc, in the power system. Various harmonics generating devices have made power management requirements. A the harmonic are generated due to the abnormal behavior of load and also demands the control over these harmonics. The significant way to maintain these aspects is by using the combination of APF for harmonic suppression and harmonic compensation. The APF is more prominent solution because it reduces both RP and HC and is smaller in size and doesn’t need any prerequisites as in PF [5].

The SRF based approaches were used to divide HC and RP, by which good power quality, can be achieved. But, it needs proper synchronization between the utility voltage and input current. Hence, DSP and other software based mechanisms were used that causes computational complexity, low/limited sampling rate and less accuracy. As these mechanisms consumes higher CPU time that causes computational latency [6, 7]. Thus, recently AFs proposed by implementing the multi-dimensional DSP. The control algorithms were used with single-DSP in low pass filter (LPF) for low sampling rate and time delay compensation. These implemented methods can bring more hardware complication and software design patterns and also in many of the cases causes the accuracy and performance issue.

In this paper, a FPGA based mechanisms for APF performance enhancement is presented. The paper is composed with various sections like: Section 2 gives APF system configuration. The section 3 gives the problem description. The section 4 gives the research methodology of FPGA implantation in APF. Section 5 algorithms implementation and the section 6 gives results analysis and conclusion of the paper is explained with the significance of the proposed method in section 7.

1. OPERATING PRINCIPLE OF APF

The current power system based industries uses more number of semiconductor based devices in furnaces, uninterrupted power supplies (UPS), computer-power supplies etc. These devices were widely used because of there low cost, flexibility, energy efficiency and also bring the improvement
in the power quality by reducing HC and utilizing RP. But, these processes can cause resonance issue, generation of more neutral current, low power-factor etc. Thus, PF were presented to solve these HC and RP issues caused due to non-linear load. But, PFs got larger size and resonance issues. Later, the APFs were presented to solve the limitations of the PF and bring the improvement in the power quality. The main significance of AF over the PF is that it has smaller size and more flexible functional applications [9].

2.2 APF Configuration

The Figure. 1, indicated with the SRF mechanism [10, 11, 12] based system configuration of APF and the blocks of it are explained below.

Figure.1. APF Configuration

Figure.2. Current-Reference (C-R) Generator

i. Distortion detection: The block contains RP and HC as current identifiers and the clock detects the distorted parameters of load current i.e. \( i_r, abc \) and derive the Voltage Source Inverter (VSI) reference current \( i_{ref} \).

ii. Phase Locked Loop (PLL): The PLL mechanism based block that can able to detect the synchronized phase information’s of \( (v_a, v_b, and v_c) \) instantaneously.

iii. Inverter-current (I-C) control: This block uses a PWM that ensures that the output VSI current \( i_c \) which tracks accurate reference waveform.

iv. VSI module: This block act as power converter and injects the waveforms of load current. In this, dc capacitor is used as supply for converter as voltage source. In the figure.2, current reference (C-R) generator is discussed which is having 3\( \phi \) load current and is transformed as \( dqz \) vector forms.

From Parks transformation principles,

\[
i_{pqz} = [i_p, i_q, i_z]^T
\]

\[
\rightarrow i_{pqz} = P \times [i_{La}, i_{Lb}, i_{Lc}]^T
\]  

Later, the \( abc \) frame components can become a dc current terms i.e., \( i_{pd}, i_{zd} \) and \( i_{qd} \) of \( dqz \) frame. Also, harmonics are transformed as the ac components using frequency shift. The negative component \( i_{qd} \) is set as zero in order to compensate the RP currents. The instantaneous active power (AP) currents can be obtained by using inverse Parks transformation, the AP current obtained from dc component are here \( i_{fa}, i_{fb} \) and \( i_{fc} \),

\[
i_{fabc} = [i_{fa}, i_{fb}, i_{fc}]^T = P^{-1} \times [i_{pd}, i_{qd}, i_{zd}]^T
\]

The distorted component is obtained from difference of \( i_{fabc} \) and \( i_{Labc} \) The obtained, current are considered as instantaneous reference currents in VSI module.

Considering equation I and II:

\[
P = \frac{2}{\sqrt{3}} \begin{bmatrix} \cos wt & \cos(wt-2/3\pi) & \cos(wt+2/3\pi) \\ -\sin wt & -\sin(wt-2/3\pi) & -\sin(wt+2/3\pi) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}
\]

\[
P^{-1} = \begin{bmatrix} \cos wt & -\sin wt & 1 \\ \cos(wt-2/3\pi) & -\sin(wt-2/3\pi) & 1 \\ \cos(wt+2/3\pi) & -\sin(wt+2/3\pi) & 1 \end{bmatrix}
\]

In case the value of \( i_c \) becomes similar to \( i_r \), reaches then compensation of RP and HC is done through APF, which leads to sinusoidal source current in phase with voltages. The system in figure.III, with load parameters in APF will leads to low total harmonic distortion (THD). here dc voltage regulator can be taken into consideration and output \( i_{dc} \) can be generated, which depends on difference between reference voltage \( v_{ref} \) and dc-bus voltage \( v_{bc} \). In case fluctuation in dc voltage occurs, then regulator starts controlling RP transfer and receive between dc capacitor and ac grid to attain constant dc voltage. The zero sequence \( i_z \) components compensate the zero sequence current in 3\( \phi \), 4-wire systems, and are zero in this application [12, 13].
2. Problem Identification

In the power distribution system the RP and the HC may offer some of the serious issues causing transformer heating, line losses, malfunctioning of power equipments and machine vibration. Various control mechanisms were examined from which Synchronous Reference Frame (SRF) for control algorithm makes significant results with simple implementation and efficient response. This algorithm offers capability of decomposition or separation of the RP and HC. Also, these algorithms demands utility voltage phase information by which necessity of synchronizer for better synchronization of S-C with the utility voltages. Various algorithms such as protection module, dc voltage regulator, analog to digital (A-D) converter drivers and directed-current (d-c) controller etc., are need to be used for synchronization. The above process leads digital controller realization in a system having high sampling rate. The DSP based and other software based mechanisms provide allowable flexibility and computational ability. The implementation of these systems with control algorithm consumes higher CPU time causing computation latency. Also, APF with multi-DSP or single-DSP were used but which leads low sampling rate and time delay compensation among the low power filter (LPF).

The above method causes the complication during designing software and hardware that may injects the reduction of compensation accuracy and APF performance. Thus, the implementation of FPGA based control algorithms will execute all the above stated procedures/steps simultaneously with hardware implementation.

3. Research Methodology

In this, a system is presented based on FPGA (figure.3). However, the challenge is to reduce the number of functional units. Here the APF is signal-processing unit: three-phase PLL, and directed current controller are discussed.

3.1 3-Phase PLL System

A. The voltage distortion caused by nonlinear load can be handled by installing the APF’s at significant point which will take care of quality phase voltage information and handle crucial conditions. Usually PLL system is employed to obtain phase information synchronized with the utility voltage in real time. The method Zero-crossing point-1 detection is largely implied, but it has relatively poor response to harmonics, frequency-variation, unbalance or noise condition. Here three-phase PLL has tremendous tracking ability under these conditions.

In ideal operation, the input data can be represented with 1 p.u. amplitude as:

$$V_{abc} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} \sin \theta \\ \sin(\theta - \frac{2\pi}{3}) \\ \sin(\theta + \frac{2\pi}{3}) \end{bmatrix}$$

(5)

3φ voltages in dqz frame can be got by using Park’s transformation from (III) to (V), the

$$V_{abc} = \begin{bmatrix} V_d \\ V_q \\ V_z \end{bmatrix}^T = P \times V_{abc}$$

(6)

Vd can be found from by (VI) under PLL-locked (steady state) condition, considering the reference component to zero.

$$V_d = \lim_{\theta \to \theta'} \sin(\theta' - \theta) = \theta' - \theta = \Delta$$

(7)

From above equation $V_d = \Delta$, when $\sin(\theta' - \theta)$ is equal to $\theta' - \theta$ when $\theta'$ approaches $\theta$ and will approach zero under phase-locked condition. A proportional-integral (PI) controller is a result of the loop error ($\Delta$) and angular frequency ($\omega$) and the phase output is obtained using an integrator. From (VII), we can know that $\Delta$ is derived from $V_d$ only, for reducing the computation $V_q$ and $V_z$ are neglected to reduce computing-resource consumption. Thus, the equation of the phase-error detection can be simplified as

$$\Delta = V_d = V_a \times \cos(\theta) + V_b \times \cos(\theta - \frac{2\pi}{3}) + V_c \times \cos(\theta + \frac{2\pi}{3})$$

(8)

Using above model the figure.4, a condensed 3φ PLL system is presented in Figure.5. From above, equation VII, $V_d = \Delta$, and which includes loop error calculation. Thus, the result forwarded to PI controller uses positive sign in the feedback loop in figure 4, then $\Delta$ is to be multiplied by constants (Kp,Ki) and Ki is taken as power of two the product can be replaced by a shifting operation, which is much modest and area-efficient in FPGA claims and also Np bit shifter is used for proportional calculation.

to truncate the output to the same width of the proportional action an Ni bits shifter is added in integral procedure. With look up table method using internal RAM of FPGA has been fulfilled sinusoidal function T(θ) Which will save the RAM resource and has met with symmetrical relation of sinusoidal function ($0 \sim \pi$).

The entire process is shown in algorithm 1:
Algorithm 1: for PLL:
Input: va, vb, vc
Output: sine/cosine signals
Start:
Step-1: Define 3φ va, vb, vc
Step-2: set Vdr=0
Step-3: Get \( V_d = \Delta \), (\( \Delta \) --is loop error)
Step-4: Generate phase output by integrator
Step-5: multiply constants Kp and Ki
Step-6: Get the output from shifters Np and Ni add to adder
Step-7: Use sinusoidal table (0 \( \sim \) \( \pi/2 \)) for sinusoidal function
Step-8: Perform post processing
Step-9: Obtain sine/cosine signals
End

A postprocessor has to be designed to produce the correct outputs from the compressed table which will result an address generator has to introduce to generate six different lookup addresses from single input \( \theta \). The address generator and postprocessor are both controlled by a finite-state machine as shown in Fig. 6.

B. 4.1.4 Directed Current Controller
The output recompensed APF currents is complex and vary continuously. Thus, high tracking accuracy is reached by inverter-current controller. When the instantaneous magnitude of the error-current (IM) is beyond the outer hysteresis tolerance Mo, the outer control loop is activated. In this mode, the magnitude of \( I \) is so large that the PWM pattern should force \( I \) to change back to the origin in the opposite direction as rapidly as possible. If the \( I \) locates in region I, then \( V1 \) should be selected because of its strongest capability to reduce \( I \) effectively. When IM is beyond the inner hysteresis tolerance Mi and within the outer tolerance, the inner control loop will be activated. In this mode, the reference voltage vector (Vref) is essentially an intermediate variable, which can be predicted as the following expression where \( L \) is the ac inductor and \( T \) is the sampling period.

\[
V_{ref} = V^n + \frac{L}{T} \Delta I
\]  

(IX)

A detailed prediction criterion of the reference voltage vector is discussed, and there is also the criterion of the optimal switching output \( V^n \), which is determined by the previous PWM output vector \( V^{n-1} \) and the region of \( I \). Furthermore, when \( V^{n-1} = V6 \), then the optimal voltage space vector should be V2. The V2 can force \( I \) to the opposite direction, and the voltage stress (Vref \( \cdot \) V2) applied to the ac inductor is the lowest one of the seven possible values. The lower the voltage stress applied to the ac inductor, the longer time the error-current vector remains in the hysteresis. Therefore, a lower switching frequency can be achieved using this strategy.
The hardware implantation is briefly explained with the following algorithm.

**Algorithm 2: for hardware implementation:**

**Input:** $R_i$

**Output:** PWM

**Start:**

- **Step-1:** Define $3\phi R_i$
- **Step-2:** Convert “$3\phi R_i$” to “$2\phi R_i$”
- **Step-3:** Generate “Magm” from $2\phi R_i$
- **Step-4:** Generate “Si” by decoder table
- **Step-5:** Combine “Magm+Si”
- **Step-6:** Get PWM

**End**

The algorithm for hardware implementation gives the detailed block of hardware implementation. In first step we consider $3\phi$ reference input i.e. $R_i$. In step 2 the $R_i$ is converted to $2\phi$ by using the shifter (Sh) and adders (ad) shown in figure.7. Later magnitude module (Magm) and sector identification (Si) is generated using $2\phi$ and decoder respectively. Then the generated outputs are applied to generate pulse width modulation (PWM) outputs by using the switching generators (Sg) and switching table (St).

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### Table 1. Improved sector identification

| Bit $[d1-d0]$ | Sector No. | Sector angle |
|---------------|------------|--------------|
| 1 X 1         | 001        | (30°,90°)    |
| 1 1 0         | 010        | (30°,90°)    |
| 0 1 0         | 011        | (90°,150°)   |
| 0 1 1         | 100        | (150°,210°)  |
| 1 1 0         | 101        | (210°,270°)  |
| 1 1 1         | 110        | (270°,330°)  |

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### Table 2. Switching output

| $\Delta f$ | $\Delta f < M_1$ | $\Delta f \geq M_2$ |
|------------|------------------|---------------------|
| 1          | 4 5 6 7 4 4 4    | 4 6 6 2             |
| 2          | 6 0 6 2 6 4 6    | 4 6 6               |
| 3          | 2 3 2 2 6 2 2    | 7 2 2               |
| 4          | 3 3 2 2 6 1 2    | 1 2 2               |
| 5          | 1 1 1 1 1 1 1    | 5 4 5               |
| 6          | (0,7) (1)        | (2) (3) (4) (5) (6) |

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**4. RESULTS**

The outcome of the proposed study is simulated using soft-computational approach using modelsim 6.3f and Xilinx ise14.7 and Spartan 3 FPGA board.

### 4.1 3φPLL Module Results

In the RTL (Figure.9), the inputs to this system are voltages $va_in$, $vb_in$, $vc_in$ and system clock $clk$ and system reset $rst$, and output are $cosa$, $cosb$, $cosc$ and $sina$, $sinb$ and $sinc$. Simulation results of 3φ PLL system is shown in figure.10. Here we have used active high reset. When the reset switch is low, the 3φ PLL System yields sine and cosine waves with different phases as shown in figure.10.
5.3 Direct current controller

The RTL schematic of the Direct current controller is represented with figure 11. The inputs to this system are delia, delib, deltic, mi, mo and system clock clk and system reset rst and the outputs are pwma, pwmb and pwmc. From the simulation (figure 12.) results of direct current controller we can see that the three pulse width modulation outputs will change according to the changes in the inputs delta_a, delta_b and delta_c.

Table 3. Design summary of Direct Current Controller

| Logic utilization | Utilization |
|-------------------|-------------|
| Slices            | 4%          |
| Slice Flip Flops  | 1%          |
| 4-input LUTs      | 2%          |
| Bonded IOBs       | 7%          |
| MultiBx1SIOs      | 32%         |
| GoLks             |             |

Table 4. 3φ PLL System design summary

| Logic utilization | Utilization |
|-------------------|-------------|
| Slices            | 2%          |
| Slice Flip Flops  | 34%         |
| 4-input LUTs      | 15%         |
| Bonded IOBs       | 4%          |
| MultiBx1SIOs      |             |
| GoLks             |             |

5. CONCLUSION

This paper deliberates an APF system based on FPGA to bring the lively performance in APF. The system is instigated with 3φ phase locked loop (PLL) and directed current controller. The performance of the proposed model is compared with Charles and Vivekananadan [14] and analyzed by Xilinx 14.7. and simulated using Model sim 6.3f Simulator. The results obtained tabled in table 5.

Table 5. Performance analysis

| Parameters         | Charles and Vivekanandan [14] | Proposed model |
|--------------------|--------------------------------|----------------|
| Logic Utilization  | 9%                             | 2%             |
| Flipflop slices    | 41%                            | 6%             |
| LUT                | 49%                            | 7%             |

From the above table 7, the flipflop slices, LUT and slices occupied are less utilized than the [14], which indicates the less area utilization and with better performance.

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