Tuning of Mixture-of-Experts Mixed-Precision Neural Networks

Semester Project II

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Abstract

Deep learning has become a useful data analysis method, however mainstream adoption in distributed computer software and embedded devices has been low so far. Often, adding deep learning inference in mainstream applications and devices requires new hardware with signal processors suited for convolutional neural networks.

This work adds new data types (quantized 16-bit and 8-bit integer, 16-bit floating point) to Caffe in order to save memory and increase inference speed on existing commodity graphics processors with OpenCL, common in everyday devices. Existing models can be executed effortlessly in mixed-precision mode. Additionally, we propose a variation of mixture-of-experts to increase inference speed on AlexNet for image classification.

We managed to decrease memory usage up to $3.29 \times$ while increasing inference speed up to $3.01 \times$ on certain devices.

We demonstrate with five simple examples how the presented techniques can easily be applied to different machine learning problems. The whole pipeline, consisting of models, example python scripts and modified Caffe library, is available as Open Source software.
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Chapter 1

Caffe Library Implementation

1.1 Introduction

Caffe has originally been created by Yangqing Jia, Evan Shelhamer, and Jeff Donahue [1]. Originally, Caffe was only intended for CPU and CUDA usage. We subsequently developed an OpenCL backend, based on ViennaCL [2], to support a variety of commodity hardware in 2015 [3–5].

Adaption for commodity hardware such as integrated GPUs, present in most modern computers, and embedded devices such as Raspberry Pi [6] and the Asus Tinkerboard [7] has been low, however. This is in part due to too slow inference speeds, which is a task that would typically be carried out in end-user applications.

A possible usage scenario of our software would be to train a network on a discrete GPU for a robot, and then build the robot with a small, energy efficient embedded system-on-a-chip computer.

In this work, we attempt to increase inference speed on both desktop and mobile GPUs by adding lower precision (quantized 8/16-bit integer and 16-bit floating point) and mixed precision networks.

Additionally, we demonstrate how mixed-precision networks could potentially be combined with mixture-of-expert techniques to increase inference speed even further.

Important terminology used throughout this work:

- **BLAS**: Basic linear algebra system: Matrix-matrix, matrix-vector, matrix-scalar, vector-vector and vector-scalar operations.
- **FP32**: 32-bit floating point (full or single precision).
- **FP16**: 16-bit floating point (half precision).
- **INT16**: Quantized 16-bit integer.
- **INT8**: Quantized 8-bit integer.
- **Caffe**: Refers to OpenCL Caffe implementation [3].
1. Caffe Library Implementation

- **LibDNN**: Our own cuDNN replacement library that provides a BLAS, convolution- and pooling-operators for INT8, INT16, FP16 and FP32. It can be compiled and executed at runtime for all CUDA and OpenCL enabled devices.

- **cuDNN**: Convolution, pooling and auxiliary operator library for CUDA enabled GPUs [8].

- **CLBlast**: BLAS library for FP16 and FP32 for OpenCL enabled devices [9].

- **MOE**: Mixture-of-experts networks, where multiple sub-networks are added according to a gating-network [10].

- **GEMM**: General matrix-matrix multiplication.

1.2 Contributions

The largest part of the work has been to improve the Caffe [3, 11] library to accommodate the lower precision floating point and quantized integer data types. The changes can be grouped into adaptions on different levels, which amounted to the task of reprogramming Caffe almost from scratch, while keeping backward- and forward-compatibility with existing trained models and Python interface code.

The tasks in chronological order of implementation:

- Merge existing efforts by Zhigang Gong on 16-bit floating point [12].

- Add CLBlast [9] as drop-in OpenCL BLAS for 16-bit floating point.

- Remove the old dual-code path, where OpenCL and CUDA code was implemented separately in each Caffe layer.

- Add a new single-code path, where a generic C-based kernel can be written into strings inside each layer. These kernels will then be interpreted as either OpenCL or CUDA code and compiled at runtime (see Section 1.3.2).

- Implement a caching system that stores precompiled kernels in a SQLite database so that subsequent execution of a network can load much faster. This was necessary to achieve the speed of the original CUDA implementation, where kernels are compiled at host code compile time. The new mode of compilation has several advantages (see Section 1.3.2).

- Add new INT8 and INT16 data types.

- Include boilerplate code to use gemmlowp [13] for integer matrix multiplication. Gemmlowp has also been used to verify the LibDNN and Caffe native quantized operators for correctness (see Section 1.3.1).

- Implement quantization layers, quantization operators and quantized operators in Caffe and LibDNN (see Section 1.4).

- Add the new data types to the Python interface to allow access from NumPy.

- Write Python interface examples for demonstrating and testing the mixture-of-experts mixed-precision neural networks (see Chapters 2 and 4).
1.2. Contributions

- Implement a mixture-of-experts layer (see Section 1.5), which can run nested Caffe networks as gating- and expert-networks.

- Write usage examples for single-neuron (celsius-farenheit, Section 2.1), dual-fully-connected (MNIST, Section 2.2), LeNet [14], ImageNet [15] and ImageNet-MOE (see Sections 1.5 and 3) [16].

- Implement OpenMP support to preprocess the ILSVRC2012 images on the CPU faster, using multiple threads, before passing them to the network.

- Add a CMake cross-compile build system that allows compilation for ARM devices such as the Raspberry Pi 3 and the Asus Tinkerboard.

These changes sum up to 180,000 new and 170,000 removed lines of code over more than 150 commits of my own work, excluding merged contributions by others [3].
1.3 Caffe Software Architecture

Caffe is accessible through an easy to use Python interface (see Chapter 2). The Caffe library itself (written in C++), contains the three main elements users are interacting with: Solvers (also called optimizers), networks (graphs) and layers (operators). Layers store parameters, carry out computation and consume and produce blobs (tensors) in the process (see Figure 1.2).

Computations within solvers, networks and layers can be executed on either the GPU or CPU backend. In this work, the GPU backend is unified into a single code path for both OpenCL and CUDA (see Section 1.3.2). Many computations are
offloaded to device specific external libraries, since these are often more optimized for the target device than the generic implementations inside Caffe (see Section 1.3.1).

### 1.3.1 Library Overview

Caffe depends on a number of external libraries to carry out common operators in a deep neural network. Not every library offers support for all operators (such as GEMM or convolution) or backends (CPU, OpenCL or CUDA), devices (ARM Mali, nVidia GeForce, AMD Polaris/Vega) or data types (FP16, FP32, INT8, INT16). It is therefore essential to have a multiplexer within Caffe, which can decide on the most appropriate library for each case.

Generally, the Caffe multiplexer first looks for operators which are optimized for a certain device or backend. If no operator can be found, LibDNN operators can replace any convolution, pooling or BLAS operator for both CUDA and OpenCL (see Table 1.1).

| Library     | cuDNN | cuBLAS | CLBlast | ViennaCL clBlas | LibDNN |
|-------------|-------|--------|---------|-----------------|--------|
| CUDA        | yes   | yes    | no      | yes, not used   | yes    |
| OpenCL      | no    | no     | yes     | yes, yes        | yes    |
| INT8        | no    | no     | no      | no, no          | yes    |
| INT16       | no    | no     | no      | no, no          | yes    |
| FP16        | partial, not used | partial, not used | yes | no, no | yes |
| FP32        | yes   | yes    | yes     | yes, yes        | yes    |
| Convolution | yes   | no     | no      | no, no          | yes    |
| Pooling     | yes   | no     | no      | no, no          | yes    |
| BLAS        | no    | yes    | yes     | yes, yes        | yes    |
| Mobile GPUs | partial | partial | yes | partial | no |

Table 1.1: Features of GPU oriented libraries used in Caffe

Since there was no library offering quantized INT8 and INT16 types for all Caffe operators utilizing OpenCL yet, we had to program our own set of quantized operators within LibDNN. Convolutions can either be carried out in LibDNN, or through a transformation (im2col, col2im) plus a GEMM operator. For our benchmarks (see Chapter 4), we always used convolutions and pooling through LibDNN, except where cuDNN and cuBLAS have faster alternatives and support the data type fully (see Table 1.1).

On CPUs, for which we do not assess performance in this work, a different set of libraries is used. Some CPUs also support OpenCL, however, the operators in OpenCL libraries are not optimized for CPUs at all. The Caffe multiplexer therefore chooses CPU libraries or Caffe native operators (see Table 1.2) even when run in OpenCL mode (see Figure 1.1).
Most notably, with this work, we also included gemmlowp [13] for fast INT8 computations on various CPUs.

| Library   | Atlas | OpenBLAS | MKL  | gemmlowp | Caffe native |
|-----------|-------|----------|------|----------|--------------|
| INT8      | no    | no       | no   | yes      | yes          |
| INT16     | no    | no       | no   | no       | yes          |
| FP16      | no    | no       | no   | no       | yes          |
| FP32      | yes   | yes      | yes  | no       | yes          |
| Convolution | no    | no       | yes, not used | no | yes |
| Pooling   | no    | no       | no   | no       | yes          |
| BLAS      | yes   | yes      | yes  | gemm only | yes          |

Table 1.2: Features of CPU oriented libraries used in Caffe

1.3.2 Device Abstraction

Before this project, Caffe consisted of two GPU code paths: One for OpenCL and one for CUDA. This was no longer viable when adding new data types (FP16, INT16, INT8), since CUDA kernels are typically built into the host code and are also compiled with it. This requires the kernels to be fully configured before compile time (including C++ templates). This would have meant to implement all four data types on two backends, resulting in up to eight code path variants plus additional CPU fallback code.

Because this was not a viable option to maintain, and due to advantages of generating layer parameter specific kernels at run-time, we decided to implement a fully device-abstracted backend to Caffe (see Figure 1.1). This approach allows to have one code path for all data types and GPU backends.

We will explain the abstracted backend with the rectified linear unit (ReLU activation) layer as an example.

Caffe Device Abstracted Host Code

Each layer has three data types, which are declared as template (see Listing 1.2 and 1.1, line 1):

- **Dtype**: The compute data type. The compute type dictates the type of the trainable layer parameters and the internal computation precision.
- **MIttype**: The bottom (input) data type to a layer. This dictates the data type of all bottom blobs consumed by a layer.
- **MOtype**: The top (output) data type to a layer. This dictates the data type of all top blobs generated by a layer.

It is left open to the layer implementation to choose which data type combinations are allowed as MItype, MOtype and Dtype. For ReLU, all types must be equal,
but can be FP32, FP16, INT16 or INT8. Quantizer layers (see Section 1.4) and MOE layers (see Section 1.5) can have a differing M|type and M|otype, but the Dtype (internal computation) is coupled to the M|type.

Additionally, the layer can derive two additional data types from the template types (see Listing 1.1 and 1.2, lines 6-7):

- **Difftype**: Difference type for quantized data types. This is typically a data type which is twice as large as the quantized type, and is signed. If such a large data type is not available, the largest supported signed integer type is used. While quantized data types are typically unsigned (see Section 1.4), a Difftype must be able to store differences of the quantized type, which can become negative. For floating point data types, the Difftype is equivalent to the Dtype.

- **Acctype**: Accumulation type for quantized data types. This is a data type which accumulates the result of one or multiple Difftype or Dtype multiplication or addition results. Because the multiplication of two 16-bit integers can only fit into a 32-bit integer, the accumulation type is typically four times as large as the quantized type. This can seriously hinder the performance of quantized computation, as demonstrated in Chapter 4.

Listing 1.1: Caffe device abstracted kernel builder code

```cpp
template<typename Dtype , typename M|type , typename M|otype>
void ReLULayer<Dtype , M|type , M|otype>::GenerateProgram()
{
    this->device_program = this->device->CreateProgram();
    stringstream ss;

typed typename std::conditional<float_is_same<M|type>::value , M|type ,
typed typename std::conditional<sizeof(M|type) == 1 , int16_t , typename std::conditional<sizeof(M|type) == 2 , int32_t , int64_t >::type>::type Difftype;
typed typename std::conditional<float_is_same<M|type>::value , M|type ,
typed typename std::conditional<sizeof(M|type) == 1 , int32_t , int64_t >::type>::type Acctype;
if (is_integer_type<M|type>()) {
    if (this->device->template preferred_vector_width<int64_t>() > 0) {
        ss << this->device_program->template define_vector_type<int64_t>(
            "Multtype" , 0 , 16);
    } else {
        ss << this->device_program->template define_vector_type<int32_t>(
            "Multtype" , 0 , 16);
    }
}
ss << this->device_program->setup();
ss << this->device_program->template define_type<Dtype>("Dtype");
ss << this->device_program->template define_type<M|type>("M|type");
ss << this->device_program->template define_type<M|otype>("M|otype");
ss << this->device_program->template define_type<Difftype>("Difftype");
ss << this->device_program->template define_type<Acctype>("Acctype");

KernelArgs fw_args;
fw_args.push_back(this->device_program->template create_kernel_arg<
    uint_tp >("n", KERNEL_ARG_CONST));
```
The device abstracted kernel builder (Listing 1.1) allows to programatically define the function arguments (lines 25-41). The function arguments have several attributes that need to be defined:

- A type, which will be adjusted to a valid OpenCL or CUDA type internally. The type can be a pointer or C data type. On OpenCL, FP16 arguments are only supported as pointers, but not values. Our device abstraction implementation will cast such values to FP32 on execution.
• A name, which is how the defined values can be addressed within the generated kernel. Pointer types on OpenCL are converted to a memory object plus an offset at which the data begins, since OpenCL does not have unified memory mapping. CUDA supports pointers directly, so the offset does not need to be passed to the kernel.

• Additional flags that declare if an argument is supposed to be a pointer to local memory, pointer to global memory or constant.

The kernel name itself (in this case ReLUForward) needs to be exclusive to the current compilation scope.

From lines 42 to 61, the actual kernel computation is defined. Since this code builds the kernel at runtime (lines 62-63), the required code for quantized integer computation (lines 48 to 58) or floating point (lines 44 to 46) can be selected at runtime, depending on the requested layer data types.

Listing 1.2: Caffe device abstracted host launch code

```cpp
1 template<typename Dtype, typename MItype, typename MOtype>
2 void ReLULayer< Dtype , MItype , MOtype >::Forward_gpu(
3   const vector<Blob<MItype>*>* bottom,
4   const vector<Blob<MOtype>*>* &top) {
5   typedef typename std::conditional<
6       float is same<MItype>::value , MItype ,
7       typename std::conditional<sizeof(MItype) == 1 , int16_t ,
8       typename std::conditional<sizeof(MItype) == 2 , int32_t , int64_t >::type >::type DiffT;
9   typedef typename std::conditional<float is same<MItype>::value , MItype ,
10      typename std::conditional<sizeof(MItype) == 1 , int32_t , int64_t >::type >::type Acctype;
11
12   vptr<const Dtype> bottom_data = bottom[0]->gpu_data();
13   vptr<Dtype> top_data = top[0]->mutable_gpu_data();
14   const int tp count = bottom[0]->count();
15   Dtype negative_slope = this->layer_param_.relu_param().negative_slope();
16   shared_ptr<DeviceKernel> kernel = this->device_program_->GetKernel("ReLUForward");
17   vector<size_t> work_size(1, count);
18   vector<size_t> group;
19   vector<size_t> local;
20   this->device_)->get_threads(&work_size, &group, &local, kernel.get(),
21      true);
22   kernel->add_arg(&count);
23   kernel->add_arg(&bottom_data);
24   kernel->add_arg(&top_data);
25   if (is_float_type<Dtype>()) {
26     kernel->add_arg(&negative_slope);
27   } else {
28     int8_t shift Bits =
29         (this->device_)->template preferred_vector_width<
30          int64_t >() > 0 ? 32 :
31            16 / sizeof(MItype) - 1;
32     Acctype mult;
33     int8_t shift;
```
In our kernel execution device abstraction (Listing 1.2), on the host code, the GPU memory is referenced with virtual pointers (vptr, lines 9-10). These virtual pointers hide either a CUDA pointer or an OpenCL memory object plus offset.

When executing the generated and compiled kernels, the order of operations is as follows:

1. The kernel is retrieved from the current compilation scope (line 14).
2. Appropriate local and global work sizes (threads and thread groups) are selected according to the number of work items in the program (lines 16-20). This query is device and implementation dependent.
3. The kernel arguments are populated (Listing 1.2, lines 22-46) in accordance to the function definition (Listing 1.1, lines 25-38).
4. Computation is scheduled for execution on the current backend (line 48). The computation can run asynchronously to the host code.

**Emitted OpenCL Runtime Code**

Listing 1.3: Emitted OpenCL code for FP32 ReLU
Listing 1.4: Emitted OpenCL code for INT8 ReLU

```c
__kernel
void ReLUForward(const uint32_t n, __global const uint8_t* in, __global
uint8_t* out, const int8_t shift_bits, const int16_t in_zero, const
int32_t mult, const int8_t shift, const int32_t out_zero, const
int32_t out_min, const int32_t out_max) {
    for (uint_t index = get_global_id(0); index < (n); index +=
        get_global_size(0)) {
        Dtype relu = max((Dtype)((Dtype)(in[index]) − in_zero), (Dtype)0);
        Acctype reg = ((Acctype)(((Multtype)relu) * (Multtype)mult)) / ((Multtype)1 << shift_bits));
        if (shift >= 0) {
            reg = reg >> shift;
        } else {
            reg = reg << −shift;
        }
        out[index] = (Dtype)(min(max(reg + out_zero, out_min), out_max));
    }
}
```

**Emitted CUDA Runtime Code**

Listing 1.5: Emitted CUDA code for FP32 ReLU

```c
extern "C" __global__ void
ReLUForward(const uint32_t n, const float* in, float* out, const float
negative_slope) {
    for (uint_t index = blockIdx.x * blockDim.x + threadIdx.x; index < (n);
        index += blockDim.x * gridDim.x) {
        out[index] = in[index] > (Dtype)0 ? in[index] : in[index] *
            negative_slope;
    }
}
```

Listing 1.6: Emitted CUDA code for INT8 ReLU

```c
extern "C" __global__ void
ReLUForward(const uint32_t n, const uint8_t* in, uint8_t* out, const
int8_t shift_bits, const int16_t in_zero, const int32_t mult, const
int8_t shift, const int32_t out_zero, const int32_t out_min, const
int32_t out_max) {
    for (uint_t index = blockIdx.x * blockDim.x + threadIdx.x; index < (n);
        index += blockDim.x * gridDim.x) {
        Dtype relu = max((Dtype)((Dtype)(in[index]) − in_zero), (Dtype)0);
        Acctype reg = (Acctype)(((Multtype)relu) * (Multtype)mult)) / ((Multtype)1 << shift_bits));
        if (shift >= 0) {
            reg = reg >> shift;
        } else {
            reg = reg << −shift;
        }
        out[index] = (Dtype)(min(max(reg + out_zero, out_min), out_max));
    }
}
```
When looking at the emitted code (Listings 1.3, 1.4, 1.5, 1.6), it is apparent that
the computation part is only different between the FP32 and INT8 versions, where
FP32 additionally supports a negative slope, while INT8 requires to offset and
shift the operands to do the quantized operation correctly (see Section 1.4).

CUDA and OpenCL, since both are based on the C language, do not differ signi-
ficantly, which is why it makes sense to have a device abstracted code generator.
Semantically, OpenCL and CUDA declare the function slightly different, with ad-
ditional qualifiers before function and argument names. This is handled by the
kernel builder, within the same macro that defines the kernel function, given a
name and a list of arguments (Listing 1.1, line 41).

The code generator also automatically selects the proper way to retrieve the con-
current thread indices (Listing 1.1, line 42), which is different for CUDA and
OpenCL (see Listing 1.3, line 3 and Listing 1.5, line 3).

Conclusively, the device abstracted backend allows the Caffe code base to remain
small, hierarchical and easy to maintain. Code duplication is kept minimal, and
all data types and devices are serviced from a single, unified host code. Adding
additional backends such as HIP [17] in the future will be easy, and will not require
modification to most of the Caffe layers, networks or solvers (see Figure 1.1).

1.4 Quantization

Quantized neural networks have gained increasing popularity due to their re-
duced memory and computation footprint (see Section 4.2). Often, INT8 and
INT16 or even lower precisions still deliver close to the same accuracy as networks
using FP32 or PF16 data types (see Section 4.4).

Our implementation of INT8 closely follows gemmlowp [13]. However, gemmlowp
is only suitable for CPU execution and optimized heavily for instruction sets found
within common ARM and x86-64 processors. The library cannot be used for either
CUDA or OpenCL.

We currently only support a quantized forward (inference) pass in Caffe. Train-
ing at lower precisions is not implemented. If a model trained in FP32 needs
quantization, the necessary parameters can be estimated (see Section 1.4.2) and
allow lower precision execution thereafter. Additionally, quantizer operators sup-
port pseudo-quantization, where the network computes at FP32 precision, but
every blob (tensor), that is scheduled for quantization, is binned to the appropri-
ate amount of distinct values (255 values for INT8 or 65535 values for INT16).

1.4.1 Quantization Integration to Caffe

Since we wanted to make quantization in Caffe intuitive for the users (see Section
2), we had to find a way to retrofit it into Caffe, which makes all network models
forward- and backward-compatible with existing trained networks.

The solution we chose was to add quantizer objects at strategic points within Caffe.
Every layer now has a set of quantizers integrated (see Figure 1.2):
• Every bottom (input) blob to a layer has a quantizer within the layer associated with it. It mediates between the MItype and Dtype of a layer.

• Every top (output) blob to a layer has a quantizer within the layer associated with it. It mediates between the Dtype and MOtype of a layer.

• Every trainable set of network parameters has a quantizer within the layer associated with it. It mediates between the Dtype of a layer and the Dtype of the solver and network.

![Figure 1.2: Caffe layer architecture with newly introduced quantizers.](image)

A quantizer object has several tasks, depending on the location of the quantizer, current precision and state of the layer:

• During training in FP32 precision, the quantizers are either passive or perform pseudo-quantization on the bottom and top blobs.

• When testing in FP32 mode, the quantizers are either passive or in observational mode. When observing, the quantizer records the maximum and minimum observed values throughout inference, which are then used to estimate quantization parameters for a subsequent inference at lower precisions (see Section 1.4.2 and Chapter 2 for usage examples).

• During reduced-precision inference (INT8, INT16), all quantizers provide
the layer computations with quantization parameters such as value range, scale, and offsets (see Section 1.4.3). An example of this particular use case can be found in Listing 1.2.

• Optionally, the layer computations are allowed to use the quantizers to convert data from MItype to Dtype, Dtype to MOtype and vice-versa. This feature is currently only utilized by the quantization layer, which sits between two layers with differing input- and output types and connects them by converting the blobs to the appropriate type.

### 1.4.2 Parameter Estimation

Quantization parameters need to be estimated from the maximum ($f_{\text{max}}$) and minimum ($f_{\text{min}}$) of the observed floating point values per blob (tensor). Additionally, zero ($i_0$) and one ($i_1$) should be representable as accurately as possible, because otherwise we might introduce an unwanted additive and multiplicative bias [13].

First, the scale $s$ is estimated, combining the range of floating point values observed ($f_{\text{max}} - f_{\text{min}}$) with the representable range of the quantized type ($i_{\text{max}} - i_{\text{min}}$). For INT8, we have $i_{\text{max}} = 255$ and $i_{\text{min}} = 0$:

$$s = \frac{f_{\text{max}} - f_{\text{min}}}{i_{\text{max}} - i_{\text{min}}}$$  \hspace{1cm} (1.1)

With the scale, we can then estimate the zero-point $i_0$:

$$i_0 = \min(\max(\lfloor i_{\text{min}} - \frac{f_{\text{min}}}{s} \rfloor, i_{\text{min}}), i_{\text{max}})$$  \hspace{1cm} (1.2)

And the one-point $i_1$ is trivially defined as:

$$i_1 = \frac{1}{s} + i_0$$  \hspace{1cm} (1.3)

The parameters are estimated in full precision and are cast to the quantized data type before being passed to quantized operators within Caffe.

### 1.4.3 Quantized Operations

Quantized operations sometimes require additional operations. The most usual example is multiplication, because multiplication of values with different quantization parameters requires adjusting the offset and scale of the result, which can then be stored in yet again another format with different parameters. Our implementation is equivalent to gemmlowp [13], but rearranges the order of operators slightly to suit GPUs rather than CPUs.

We define a simple multiplication in full precision as:

$$c = a \cdot b$$  \hspace{1cm} (1.4)
If we want to carry out the equivalent multiplication in quantized types, the operation becomes:

\[
c = \left( (a - i_0^{(a)}) \cdot (b - i_0^{(b)}) \right) \cdot \frac{s^{(a)} \cdot s^{(b)}}{s^{(c)}} + i_0^{(c)}
\]  

(1.5)

where \(i_0^{(a)}, i_0^{(b)}\) and \(i_0^{(c)}\) are the respective estimated zero-points of \(a, b\) and \(c\). The scale terms \(s^{(a)}, s^{(b)}, s^{(c)}\) rescale the result into the target domain.

The computation can be separated, which is done in our GEMM and convolution kernels, as well as in gemmlowp [13], and allows to use faster code paths such as nVidia DP4A/DP2A [18]. The faster code can be used because, as we have seen in Section 1.3.2, differences for an INT8 operation are stored in INT16, while sums of multiplications are stored in INT32. If we compute differences before multiplication, then the multiplication has to be carried out in INT16. But when executing the multiplications first, they can be done in INT8 and accumulated into either INT16 or INT32, depending on the expected size of the result sum.

Changing the order of operations also reduces the number of computations in matrix multiplications trivially, since all \(i_0\) remain constant during the operation, and only \(a, b\) and \(c\) change throughout the rows and columns of a matrix.

\[
c = (a \cdot b - b \cdot i_0^{(a)} - a \cdot i_0^{(b)} + i_0^{(a)} \cdot i_0^{(b)}) \cdot \frac{s^{(a)} \cdot s^{(b)}}{s^{(c)}} + i_0^{(c)}
\]  

(1.6)

Unfortunately, since we want to carry out all operators as integer types only, rescaling with \(\frac{s^{(a)} \cdot s^{(b)}}{s^{(c)}}\) is not an option. Instead, we search an integer multiplier \(m\) and integer arithmetic right shift value \(h\) that fulfill the following equation:

\[
(x \cdot m) \gg h = x \cdot \frac{s^{(a)} \cdot s^{(b)}}{s^{(c)}}
\]  

(1.7)

The shift and multiplier values can be determined once and remain constant. The equation can be fulfilled because an arithmetic shift is equivalent to dividing by a power of two. The resulting operation becomes:

\[
c = \left( (a \cdot b - b \cdot i_0^{(a)} - a \cdot i_0^{(b)} + i_0^{(a)} \cdot i_0^{(b)}) \cdot m \right) \gg h + i_0^{(c)}
\]  

(1.8)

In practice, additional rounding and clipping operations are in place to ensure no overflow or bias are introduced into the neural network. We omit detailed explanation of these additional steps, because they are use-case dependent and vary greatly from operator to operator. These operations can be found in the Caffe operators in the source code [3].

1.5 Mixture of Experts

Mixture of experts neural networks combine different sub-networks in a larger network. These have typically been used to save inference time, add more parameters
to a model or make multi-GPU training faster and easier [10]. MOE networks can be seen as member of a class of networks that have divergent computation paths. Other examples of such networks include networks with conditional computations and early exits [19].

For our work, we chose to use MOE networks to accelerate inference on low-end devices such as the Intel Iris Pro 540 and ARM Mali T764 (see Section 4.1). These devices profit from selectively processing more, but smaller neural network operators.

The mixture-of-experts network consists of four parts:

- The main network, which is a regular convolutional neural network before and after the mixture-of-experts stage.
- A collection of experts with identical input and output tensor dimensions.
- A gating network, of which we take the output to decide which experts to use, usually combined with a noise and softmax stage.
- A gating selection stage, which selects the most useful experts and mixes their output. It is important to note that the experts are selected differently for every element of a batch during minibatch training and inference, since the choice of expert depends on a single sample only.

Unfortunately, the gating selection stage reinforces good experts to be used more often, which means after some training time, a few experts are very well trained, while others are untrained and completely disabled. A similar problem has been noted in previous work [10].

To mitigate the problem, we use a noisy gating function, using additive and multiplicative noise, to compute probabilities $p_i$ for each expert:

$$q_i = \exp(w_i^{(a)} x + w_i^{(b)} x \cdot \mathcal{N}(\mu = 0, \sigma = 1) + w_i^{(c)} \cdot \mathcal{N}(\mu = 0, \sigma = 10))$$ (1.9)

$$p_i = \frac{q_i}{\sum_{j=1}^{N} q_j} \quad \forall i \in [1, N]$$ (1.10)

Where $x$ is the gating network output. The network is expected to start with noisy gating and should slowly select experts smarter through the trainable weights $w^{(a)}$, while decreasing the noise regulating weights $w^{(b)}$ and $w^{(c)}$ towards zero.

The probabilities $p_i$ are normalized so that they are non-zero only for selected experts and add up to one. The network then only computes the top $K$ selected experts from $N$ total experts, and sums their output weighted by the normalized probabilities $p_i$.

Additionally, we use a $L2$ regularization loss on the discrete number of times an expert has been used, compared to the expected average if every expert is used equally often:

$$l_2 = \frac{1}{N} \sum_{i=1}^{N} \left( \frac{K}{B} - c_i \right)^2$$ (1.11)

Where $c_i$ is the observed number of times expert $i$ has been used in the current batch of batch-size $B$. 

1. CAFFE LIBRARY IMPLEMENTATION
1.5. Mixture of Experts

Our ImageNet-MOE configuration is explained in Section 3.2, with complete network graphs in Appendix A.2.
These examples demonstrate the ease of use of the new data types through the python interface. Larger examples (LeNet and ImageNet) have been omitted in text-form, but can be found online [16].

2.1 Celsius-Farenheit

This example uses a single neuron to compute the farenheit value corresponding to a celsius value. A single neuron is sufficient since this operation is linear:

\[ y = ax + b \]  

(2.1)

The network has to train in full precision (FP32) to arrive at the estimated parameters of \( a = 1.8 \) and \( b = 32.0 \).

Listing 2.1: Creating the celsius-farenheit network

```python
import sys
sys.path.append('..')
from caffe_examples_setup import *

# We create the network for float, half, int16 and int8
data_types = [caffe.data_type.CAFFE_HALF, caffe.data_type.CAFFE_FLOAT,
              caffe.data_type.CAFFE_INT8_QUANTIZED, caffe.data_type.CAFFE_INT16_QUANTIZED]
data_types_names = ['half', 'float', 'int8', 'int16']

for data_type in zip(data_types, data_types_names):
    net = caffe.NetSpec()
    net.celsius = L.Input(input_param=dict(shape=dict(dim=[1,1,1,1])), ntop=1)
    net.farenheit = L.Input(input_param=dict(shape=dict(dim=[1,1,1,1])),
                            ntop=1, include=dict(phase=0))

    net.neuron = L.InnerProduct(net.celsius,
                                bottom_data_type = data_type[0],
                                compute_data_type = data_type[0],
                                top_data_type = data_type[0],
                                inner_product_param = dict(num_output = 1,
                                                           weight_filler = dict(type='constant')),
```
2. Examples

```python
bias_filler = dict(type='constant'))
net.output = L.Quantizer(net.neuron,
    bottom_data_type = data_type[0],
    compute_data_type = data_type[0],
    top_data_type = caffe.data_type.CAFFE_FLOAT)
net.euclidean = L.EuclideanLoss(net.output, net.fahrenheit, include=dict(
    phase=0))
protonet = net.to_proto()
protonet.name = 'net'
with open(protonet.name + '_' + data_type[1] + '.prototxt', 'w') as f:
    print(protonet, file=f)
```

In the past, it was necessary to write each Caffe network as a protocol text. In more recent versions, programmatically creating networks has been made easy. In Listing 2.1, we create a single-neuron network for FP32, FP16, INT16 and INT8 data types and store them on disk. As described in Section 1.4.1, each layer now has additional parameters to describe its input (bottom), compute and output (top) data type. Our neuron is always using the selected precision (lines 16-18). The network output is always a floating point number, converted by a quantizer layer (lines 22-25). Network inputs and the loss are also computed at full precision.

Listing 2.2: Training the celsius-fahrenheit network

```python
import sys
sys.path.append('..')
from caffe_examples_setup import *

# Choose the precision (half, float, int8 or int16).
precision = 'float'

# Define the training and testing data
values_celsius = np.array([(float)(c) for c in range(-273,1000)])
# We know that fahrenheit = celsius * 1.8 + 32.0
values_fahrenheit = np.array([c*1.8+32.0 for c in values_celsius])

# Split data into training (90%) and testing (10%)
indices = np.random.permutation(values_celsius.shape[0])
training_idx, test_idx = indices[:int(90*values_celsius.shape[0]/100)],
    indices[int(90*values_celsius.shape[0]/100):]
values_celsius_train = values_celsius[training_idx]
values_fahrenheit_train = values_fahrenheit[training_idx]
values_celsius_test = values_celsius[test_idx]
values_fahrenheit_test = values_fahrenheit[test_idx]

# Create a solver with a few typical parameters
# The solver will perform SGD on our data
solver_config = caffe.SolverParameter()
solver_config.train_net = 'net.' + precision + '.prototxt'
solver_config.base_lr = 1.0
solver_config.momentum = 0.99
solver_config.weight_decay = 0.00005
solver_config.lr_policy = 'inv'
solver_config.gamma = 0.01
solver_config.power = 0.75
solver_config.max_iter = 2000
```
In Listing 2.2, lines 1-64 describe the usual training process. Additionally, since we want to run the network in quantized mode later, we need to add lines 66-82. This part of the code runs a few test examples through the network at full precision and collects statistics about the value domain of each blob and parameter in the network (see Section 1.4). The resulting values are stored as quantization
parameters together with the trained network (line 81).

Listing 2.3: Testing the celsius-farenheit network

```python
import sys
sys.path.append('..')
from caffe_examples_setup import *

# Choose the precision (half, float, int16 or int8)
precision = 'float'

# Define the training and testing data
values_celsius = np.array([[float(c) for c in range(-273,1000)]])
values_fahrenheit = np.array([c+1.8+32.0 for c in values_celsius])

# Split data into training (90%) and testing (10%)
indices = np.random.permutation(values_celsius.shape[0])
training_idx, test_idx = indices[:int(90*values_celsius.shape[0]/100)],
                        indices[int(90*values_celsius.shape[0]/100):]
values_celsius_train = values_celsius[training_idx]
values_fahrenheit_train = values_fahrenheit[training_idx]
values_celsius_test = values_celsius[test_idx]
values_fahrenheit_test = values_fahrenheit[test_idx]

# Test how accurate the network has learned it’s task
error = []
testnet = caffe.Net(str('net.' + precision + '.prototxt'), caffe.TEST,
                    weights='net_trained.caffemodel')
for c,f in zip(values_celsius_test,values_fahrenheit_test):
    testnet.blobs['celsius'].data[0] = c
    testnet.forward()
    predicted_f = testnet.blobs['output'].data[0,0]
    print('Celsius: ' + str(c) + ' C, predicted: ' + str(predicted_f) + ' F, actual: ' + str(f) + ' F')
    error.append(abs(f-predicted_f))
print('Average error: ' + str(np.array(error).mean()) + ' F')
```

Listing 2.3 demonstrates how easily different inference precisions can be selected (line 6). The network will load the full-precision or already quantized weights (line 24), quantize them (if necessary) and run the inference according to the estimated quantization parameters.

The accuracy of the different inference precisions can be found in Section 4.4.1.

2.2 MNIST

This example uses two fully connected layers to recognize hand-written digits from 1 to 9.

Listing 2.4: Creating the simple MNIST network

```python
import sys
sys.path.append('..')
from caffe_examples_setup import *
```
# Create a simple network with just one hidden layer and a flat 784 size input vector

# We create the network for float, half, int16 and int8
data_types = [caffe.data_type.CAFFE_HALF, caffe.data_type.CAFFE_FLOAT,
              caffe.data_type.CAFFE_INT8_QUANTIZED, caffe.data_type.CAFFE_INT16_QUANTIZED]
data_types_names = ['half', 'float', 'int8', 'int16']

for data_type in zip(data_types, data_types_names):
    net = caffe.NetSpec()
    net.mnist_image = L.Input(input_param=dict(shape=dict(dim=[1,1,1,784])), ntop=1)
    net.label = L.Input(input_param=dict(shape=dict(dim=[1,1,1,1])), ntop=1)

    net.hidden_layer = L.InnerProduct(net.mnist_image,
                                       bottom_data_type=data_type[0],
                                       compute_data_type=data_type[0],
                                       top_data_type=data_type[0],
                                       inner_product_param=dict(num_output=30,
                                                    weight_filler=dict(type='xavier'),
                                                    bias_filler=dict(type='constant', value=0.0)))
    net.output_layer = L.InnerProduct(net.hidden_layer,
                                       bottom_data_type=data_type[0],
                                       compute_data_type=data_type[0],
                                       top_data_type=data_type[0],
                                       inner_product_param=dict(num_output=10,
                                                    weight_filler=dict(type='xavier'),
                                                    bias_filler=dict(type='constant', value=0.0)))

    net.loss = L.SoftmaxWithLoss(net.output_layer, net.label, include=dict(phase=0))
    net.pred = L.Softmax(net.output_layer, include=dict(phase=1))

    protonet = net.to_proto()
    protonet.name = 'net'
    with open(protonet.name + '_' + data_type[1] + '.prototxt', 'w') as f:
        print(protonet, file=f)

import sys
sys.path.append('..')
from caffe_examples_setup import *

# Choose the precision (half, float, int16 or int8).
precision = 'float'

# Load the data
f = open('..data/mnist.pkl', 'rb')
training_data, validation_data, test_data = cPickle.load(f, encoding='latin1')
f.close()

# Create a solver with a few typical parameters
# The solver will perform SGD on our data
solver_config = caffe.SolverParameter()
2. Examples

```python
solver_config.train_net = 'net_' + precision + '.prototxt'
solver_config.base_lr = 0.01
solver_config.momentum = 0.99
solver_config.weight_decay = 0.0001
solver_config.lr_policy = 'inv'
solver_config.gamma = 0.0001
solver_config.power = 0.75
solver_config.max_iter = 16000
solver_config.snapshot = 4000
solver_config.snapshot_prefix = 'net'
solver_config.type = 'Adam'
solver_config.display = 100

# Do the training
losses = []
plt.ion()
plot_obj, = plt.plot(losses)
ax = plt.gca()
plt.show()
plt.pause(0.001)
solver = caffe.get_solver(solver_config)
for i in range(0, solver_config.max_iter):
    # Pick a random sample for training
    k = random.randint(0, len(training_data[0]) - 1)
    # Load the sample into the network
    solver.net.blobs['mnist_image'].data[:] = np.reshape(training_data[0][k], (784)).astype(float)/255.0
    solver.net.blobs['label'].data[0] = training_data[1][k]
    # Train one step
    loss = solver.step(1)
    # Display the learning progress every 20 steps
    if (i % 100 == 0):
        losses.append(loss)
        plot_obj.set_data(range(0, len(losses)), losses)
        ax.relim()
        ax.autoscale_view(True, True, True)
        plt.draw()
        plt.pause(0.001)

    # Run a few test steps to observe the value ranges (for quantization)
    error = 0
testnet = caffe.Net(str('net_' + precision + '.prototxt'), caffe.TEST,
                      weights='net_iter_' + str(solver_config.max_iter) + '.caffemodel')
    # Enable quantizer observation
    testnet.quant_mode = caffe.quantizer_mode.CAFFE_QUANT_OBSERVE
    for k in range(0, len(validation_data[0])):
        testnet.blobs['mnist_image'].data[:] = np.reshape(validation_data[0][k], (784)).astype(float)/255.0
        testnet.forward()
        if (k % 100 == 0):
            print(k)
    # Store the network parameters, including obtain quantizer information
    testnet.save('net_trained.caffemodel')
print("Done.")
```
Listing 2.6: Testing the simple MNIST network

```python
import sys
sys.path.append('..')
from caffe_examples_setup import *

# Choose the precision (half, float, int16 or int8)
precision = 'float'

# Load the data
f = open('..../data/mnist.pkl', 'rb')
training_data, validation_data, test_data = cPickle.load(f, encoding='latin1')
f.close()

# Test how accurate the network has learned its task
error = 0
testnet = caffe.Net(str('net_') + precision + '.prototxt'), caffe.TEST,
weights='net_trained.caffemodel')
for k in range(0, len(validation_data[0])):
    testnet.blobs['mnist_image'].data[:] = np.reshape(validation_data[0][k], (784)).astype(float)/255.0
    testnet.forward()
    predicted_number = np.argmax(testnet.blobs['pred'], data[:])
    print('Predicted: ' + str(predicted_number) + ', actual: ' + str(validation_data[1][k])
    if not (predicted_number == validation_data[1][k]):
        error += 1
print('Errors: ' + str(error) + ' of ' + str(len(validation_data[0])) + ' (' + str(100.0 - 100.0*(float(error)/(float(len(validation_data[0]))))) + '% accuracy)'
```

The accuracy of the different inference precisions can be found in Section 4.4.2.
Chapter 3

ImageNet

To assess the memory, storage and compute requirements of our methods, we chose the well-established AlexNet/ImageNet [15] on the 1000-way image classification task ILSVRC2012. The input size of the network is an RGB image with $227 \times 227$ pixels.

3.1 ImageNet Configuration

As a baseline, we used the standard AlexNet/ImageNet [15] bundled with Caffe [3]. It has a single compute path, defined by following operations:

- Convolution (kernel size 11, stride 4, 96 feature maps) + ReLU
- Pooling (kernel size 3, stride 2) + LRN
- Convolution (kernel size 5, pad 2, group 2, 256 feature maps) + ReLU
- Pooling (kernel size 3, stride 2) + LRN
- Convolution (kernel size 3, pad 1, 384 feature maps) + ReLU
- Convolution (kernel size 3, pad 1, group 2, 384 feature maps) + ReLU
- Convolution (kernel size 3, pad 1, group 2, 256 feature maps) + ReLU
- Pooling (kernel size 3, stride 2)
- Fully connected (4096 feature maps) + ReLU + Dropout
- Fully connected (4096 feature maps) + ReLU + Dropout
- Fully connected (1000 feature maps) + Softmax

The network graph can be found in Appendix A.1.
3. ImageNet

3.2 ImageNet-MOE Configuration

We build the MOE network configuration according to the method description in Section 1.5.

3.2.1 MOE Main Network

- Convolution (kernel size 11, stride 4, 48 feature maps) + ReLU
- Pooling (kernel size 3, stride 2) + LRN
- Mixture-of-Experts (16 experts, 4 experts per sample, 2048 feature maps) + ReLU + Dropout
- Fully connected (1000 feature maps) + Softmax

The main network includes the first and last few layers of the original ImageNet, with slightly altered feature map counts.

3.2.2 MOE Gating Network

Our gating network is substantially smaller and cheaper to compute than the expert network, because it is usually enough to get approximate hints out of the gating network. Smaller networks are also easier to train in this case, since the regularization loss and noise (see Section 1.5) complicate the training.

- Convolution (kernel size 5, pad 2, group 2, 64 feature maps) + ReLU
- Pooling (kernel size 3, stride 2) + LRN
- Fully connected (128 feature maps) + ReLU
- Fully connected (16 feature maps)

In more complex, hierarchical tasks, it would be possible to additionally train the gating network with a task such as predicting the class an object belongs to, while the whole network would classify the exact object type.

3.2.3 MOE Expert Network

The expert network in our model is repeated 16 times, with each layer, except the output layer, having four times fewer output feature maps compared to the original AlexNet. This makes each expert network approximately 16 times cheaper to compute, since the number of computations depends on the product of input- and output-feature maps of each layer. Per forward pass, the MOE layer chooses 4 of 16 experts, reducing computation requirements four times. The mixture-of-experts layer and the gating network add some overhead again, however.

- Convolution (kernel size 5, pad 2, group 2, 64 feature maps) + ReLU
- Pooling (kernel size 3, stride 2) + LRN
- Convolution (kernel size 3, pad 1, 96 feature maps) + ReLU
- Convolution (kernel size 3, pad 1, group 2, 96 feature maps) + ReLU
3.2. ImageNet-MOE Configuration

- Convolution (kernel size 3, pad 1, group 2, 64 feature maps) + ReLU
- Pooling (kernel size 3, stride 2)
- Fully connected (1024 feature maps) + ReLU + Dropout
- Fully connected (2048 feature maps)

The expert network includes the middle hidden layers of the original ImageNet, which are not included in the main MOE network. Combining the two parts results in a forward-backward path with equivalent feature map sizes to the original ImageNet.

The network graph can be found in Appendix A.2.
In order to assess performance and accuracy of both the mixture-of-experts networks and mixed-precision computations, we used the classic ImageNet/AlexNet [15] as a case study (see Chapter 3).

4.1 Devices

We benchmarked following devices:

| Device Name     | AMD Vega FE [20] | AMD RX 480 [21] | nVidia GTX 1080 [22] |
|-----------------|------------------|------------------|----------------------|
| Compute Units   | 64 (4096)        | 36 (2304)        | 20 (2560)            |
| Memory [GiB]    | 16               | 8                | 8                    |
| TFLOPS FP16     | 26.2             | 5.8(2)           | 0.6(3)               |
| TFLOPS FP32     | 13.1             | 5.8              | 8.9                  |
| TOPS INT8       | 52.4(1)          | 5.8              | 35.6(4)              |
| TOPS INT16      | 26.2(1)          | 5.8              | 17.8(4)              |

| Device Name     | nVidia GT 1030 [22] | Intel Iris Pro 540 [23, 24] | ARM Mali T764 [7, 25] |
|-----------------|----------------------|-------------------------------|----------------------|
| Compute Units   | 3 (384)              | 2 x 3 (48)                    | 4 (64)               |
| Memory [GiB]    | 2                    | 5                             | 0.25                 |
| TFLOPS FP16     | 0.018(3)             | 1.504(5)                      | 0.16                 |
| TFLOPS FP32     | 1.127                | 0.752                         | 0.08                 |
| TOPS INT8       | 4.508                | 0.752                         | 0.32                 |
| TOPS INT16      | 2.254                | 0.752                         | 0.16                 |

Table 4.1: Devices used for benchmarks and their features.

(1) Only fast integer for some operators, which are not useful to Caffe inference.
(2) Uses FP32 path for computation and FP16 for storage only.
(3) Has a FP16 code path for computation, but is limited at 1/64 FP32 speed.
(4) Using nVidias DP4 and DP2 instructions [18].
(5) Not working due to OpenCL driver issues on Intel Beignet.
4.2 Memory and Storage Consumption

4.2.1 Storage

| Network    | ImageNet MiB | ImageNet-MOE MiB |
|------------|--------------|------------------|
| FP32       | 243.9 MiB    | 309.9 MiB        |
| FP16       | 121.9 MiB    | 155.0 MiB        |
| INT16      | 121.9 MiB    | 155.0 MiB        |
| INT8       | 61.0 MiB     | 77.5 MiB         |

Table 4.2: Network parameter storage size.

Figure 4.1: Network parameter storage size.

Caffe now has the possibility to also store the trained weights in reduced precision. As expected, storage requirements drop linearly with the number of bytes per weight. With FP32, 4 bytes per weight are consumed, while with the lowest precision, INT8, it is only one byte. The mixture-of-experts variant of ImageNet uses slightly more memory (27%), which can mostly be attributed to the gating network and the increased number of weights when transiting from the main network into the expert networks and back again.

The quantization parameters, which are always stored as FP32, do not add significantly to the storage requirements.
4.2. Memory and Storage Consumption

4.2.2 Memory

For memory consumption, we measured only the GPU memory, while ignoring the overhead memory on the CPU. All memory related tests have been executed for a batch size of 512 images.

| Network          | ImageNet | ImageNet-MOE | ImageNet-MOE | ImageNet-MOE |
|------------------|----------|--------------|--------------|--------------|
| Reduced memory   | no       | yes          | no           | yes          |
| CUDA FP32        | 3351 MiB | 2281 MiB     | 6753 MiB     | 3991 MiB     |
| CUDA FP16        | 2389 MiB | 1407 MiB     | 1409 MiB     | 1209 MiB     |
| CUDA INT16       | 2391 MiB | 1409 MiB     | 4535 MiB     | 2631 MiB     |
| CUDA INT8        | 1815 MiB | 1209 MiB     | 3361 MiB     | 2061 MiB     |
| OpenCL FP32      | 3275 MiB | 2047 MiB     | 6211 MiB     | 3449 MiB     |
| OpenCL FP16      | 2341 MiB | 1379 MiB     | 4329 MiB     | 2432 MiB     |
| OpenCL INT16     | 2343 MiB | 1361 MiB     | 4361 MiB     | 2457 MiB     |
| OpenCL INT8      | 1771 MiB | 1165 MiB     | 3187 MiB     | 1887 MiB     |

Table 4.3: Network memory consumption.

Using the lowest precision, INT8, reduces the memory consumption by 54% compared to FP32. Since we use mixed-precision, some layers such as the LRN layer are still executed at full precision, even when using INT8. This means we get less than linear improvement.

With an additional technique, which reuses the blobs in the network graph as often as possible (denoted RM in Figures 4.2 and 4.3), we can reduce the memory con-
4. Benchmarks

...sumption by an additional 68%. The downside of reusing memory is that inspection of intermediate results in the network is impossible, but this is not a problem in typical inference applications. When debugging a network, the memory sharing can easily be disabled. During training, no blobs in the network are allowed to be overwritten, since they are needed for gradient computations. Therefore, the reduced memory option is always disabled during training.

In total, we claim up to $3.29 \times$ less memory consumption, using a combination of low-precision and reduced-memory inference.

![Network memory consumption using the OpenCL backend.](image)

OpenCL typically uses less memory than CUDA, which we tracked down to pre-allocated memory inside the external libraries that Caffe makes use of. Such temporary memory can be used to store intermediate results of reduction, convolution and other operators that require global working memory.
4.3 Inference Throughput

4.3.1 ImageNet

| GPU                  | Backend | Batch | FP32  | FP16  | INT16 | INT8  |
|----------------------|---------|-------|-------|-------|-------|-------|
| nVidia GTX 1080      | CUDA    | 512   | 510 ms| 22.33 ms| 2350 ms| 565 ms|
| nVidia GTX 1080      | OpenCL  | 512   | 728 ms| n/a   | 1425 ms| 715 ms|
| nVidia GT 1030       | CUDA    | 64    | 353 ms| 18.01 ms| 1595 ms| 437 ms|
| nVidia GT 1030       | OpenCL  | 64    | 542 ms| n/a   | 1258 ms| 594 ms|
| AMD Vega FE          | OpenCL  | 512   | 863 ms| 380 ms| 828 ms| 931 ms|
| AMD RX 480           | OpenCL  | 512   | 1675 ms| 1014 ms| 1863 ms| 2038 ms|
| Intel Iris Pro 540   | OpenCL  | 64    | 1209 ms| n/a | 24737 ms| 9926 ms|
| ARM Mali T764        | OpenCL  | 4     | 4321 ms| 2461 ms| 4045 ms| 3606 ms|

Table 4.4: ImageNet inference time.

Figure 4.4: ImageNet throughput.

Using FP16 increases the throughput on both AMD GPUs and on the ARM Mali T764 GPU, however, not by the same amount. Because the AMD Vega FE and Mali GPU can execute twice the amount of FP16 operations compared to FP32 (see Table 4.1), their throughput increases by 128.8% and 75.3% respectively. The AMD RX 480 card, which can do FP16 computations, but uses FP32 internally, gains 65% through memory bandwidth savings on the global, local and register memory. For nVidia and Intel GPUs, the FP16 data type is not useful.
The integer quantized types are, at large, not useful to increase the inference speed on any GPU we tested. Since the speed of integer types is consistent on the AMD GPUs, it may still be a viable option if memory is the limiting factor (see Section 4.2)

nVidia GPUs use DP4A and DP2A [18] instructions to accelerate INT8 computations, but the compute and memory overhead of the quantized types negate any performance gains in our implementation. We confirmed that the DP4A and DP2A instructions are actually compiled into the compute kernels using assembly code analysis. Additional kernel tuning and probably hand-tuned algorithms would be required to reach higher throughputs.

Since INT8 quantized computation also requires INT16 and INT32 operations (see Section 1.4.3), GPUs like the ARM Mali T764 and AMD Vega FE, which could execute some pure INT8 operations (addition, subtraction, quad-absolute-sum-of-differences) at faster speeds, do not profit from the lower precision inference paths. Intrinsics that perform fused-multiply-add from INT8 to INT32 on vector types are likely required to increase performance, but are not implemented in the hardware.
4.3. Inference Throughput

4.3.2 ImageNet-MOE

| GPU                | backend     | Batch | FP32   | FP16   | INT16  | INT8   |
|--------------------|-------------|-------|--------|--------|--------|--------|
| nVidia GTX 1080    | CUDA        | 512   | 587 ms | 79.77 ms | 7743 ms | 1626 ms |
| nVidia GTX 1080    | OpenCL      | 512   | 1541 ms | n/a    | 4776 ms | 2342 ms |
| nVidia GT 1030     | CUDA        | 64    | 385 ms | 63.93 ms | 5136 ms | 1267 ms |
| nVidia GT 1030     | OpenCL      | 64    | 1124 ms | n/a    | 3884 ms | 1824 ms |
| AMD Vega FE        | OpenCL      | 512   | 1353 ms | 10.17 ms | 2433 ms | 2797 ms |
| AMD RX 480         | OpenCL      | 512   | 2453 ms | 2373 ms | 5002 ms | 5881 ms |
| Intel Iris Pro 540 | OpenCL      | 64    | 3600 ms | n/a    | 41403 ms | 14789 ms |
| ARM Mali T764      | OpenCL      | 4     | 2422 ms | 1435 ms | 5837 ms | 6096 ms |

Table 4.5: ImageNet-MOE inference time.

![Figure 4.6: ImageNet-MOE throughput.](image)

Performance on our ImageNet-MOE network is consistently slower on all GPUs except the ARM Mali T764. This was an expected outcome, since the larger GPUs profit from executing a network for a large batch at once. For the GPUs using a batch-size of 512 and for the nVidia GT 1030 (see Table 4.5), we configured the MOE layer so that all experts are always computed for the whole batch. Executing the experts only for the necessary samples resulted in even lower throughputs, because the individual computations are too small to utilize the whole GPU.

We tried to mitigate the performance reduction problem by at least executing all experts in parallel, using up to 8 streams/queues. But because each operator in
the expert networks also have fewer operations, due to reduced input- and output-
feature maps (see Section 3.2), getting the same utilization as a normal ImageNet
is not possible. We therefore conclude that mixture-of-experts only become useful
on large GPUs when the individual experts are expensive to compute and can be
executed for a large batch of samples using the same experts at once.

An alternative use-case is low-latency inference, where for example a live-stream
from a camera has to be passed through a neural network, making large batches
inherently impossible. In this case, using MOE networks may also make sense on
large GPUs.

On the Intel Iris Pro 540 and ARM Mali T764, only computing the necessary ex-
perts selected by the gating network per-sample (see Section 1.5) results in higher
inference speed (see Figures 4.6 and 4.7).

For the ARM Mali T764, the inference speed increases 77% compared to the nor-
mal ImageNet at FP32, and 71% at FP16.

Using a combination of FP16 inference and MOE technique, we achieve the claimed
3.01× throughput, compared to normal ImageNet FP32 inference.

![Figure 4.7: ImageNet-MOE throughput (log scale).](image-url)
4.4 Inference Accuracy

4.4.1 Celsius-Farenheit

We included the accuracy of the celsius-farenheit example (see Section 2.1) because on this example, the accuracy results can very easily be explained.

|     | FP32 | FP16 | INT16 | INT8  |
|-----|------|------|-------|-------|
| Error [°F] | 2.51804 | 2.26494 | 2.42341 | 6.93617 |

Table 4.6: Celsius to farenheit conversion error for different precisions.

We see in Table 4.6 that FP32, FP16 and INT16 have negligible difference in accuracy. This is explained by each of these data types being able to sufficiently represent the range of values for both the input in °C in the range of \([-273.0, 1000.0]\) as well as the output in °F in the range of \([-394.6, 1832]\). The same is trivially true for the learned weight \((a = 1.8)\) and bias \((b = 32.0)\) parameters. For INT16, we have 65,535 binned values (see Section 1.4), which would allow the error to be as low as 0.017 °F with sufficient training.

INT8, on the other hand, only has 255 binned values. This restricts the error to be greater or equal to 4.3658 °F, which is why INT8 performs worse than the other data types. This should be kept in mind when designing neural networks. Especially the input and output stages might benefit from higher precisions in order to accurately represent the value domains.

4.4.2 MNIST

|     | FP32 | FP16 | INT16 | INT8  |
|-----|------|------|-------|-------|
| Top-1 Accuracy [%] | 85.26 | 85.30 | 85.27 | 85.36 |

Table 4.7: MNIST accuracy.

We recognize that MNIST [26] can be predicted to a much higher accuracy with models such as LeNet [14]. However, for simplicity, as an usage example of mixed-precisions, we demonstrate a simple network with only two fully connected layers (see Section 2.2). The more complex LeNet example can be found online [16]. All data types achieve the same accuracy. Since the input domain is pixel values in \([0, 255]\) and the output is discrete in \([0, 9]\), this problem does not suffer from domain binning restrictions by quantization, unlike converting celsius to farenheit values (see Section 4.4.1). Another aspect is that the model has more weights, making the precision of each single weight less important.
4. Benchmarks

4.4.3 ImageNet

|                  | FP32 | FP16 | INT16 | INT8 |
|------------------|------|------|-------|------|
| Top-1 accuracy (train) [%] | 79.113 | 79.059 | 54.566 | 59.840 |
| Top-5 accuracy (train) [%]   | 93.887 | 93.852 | 77.262 | 83.277 |
| Top-1 accuracy (test) [%]   | 56.875 | 56.813 | 42.690 | 44.750 |
| Top-5 accuracy (test) [%]   | 79.980 | 79.973 | 66.320 | 70.043 |

Table 4.8: Original ImageNet accuracy

The standard pre-trained ImageNet reaches a test-set accuracy of up to 56.875%. Using the lower precision inference FP16 is a good choice, since it does not drop the accuracy significantly, does not require fine-tuning and reaches over 100% increased throughput over FP32 on some devices (see Section 4.3.1).

Using INT8 and INT16 reduces accuracy up to 12% without fine-tuning the network with pseudo-quantization (see Section 1.4).

4.4.4 ImageNet-MOE

|                  | FP32 | FP16 | INT16 | INT8 |
|------------------|------|------|-------|------|
| Top-1 accuracy (train) [%] | 66.804 | 66.734 | 12.805 | 53.410 |
| Top-5 accuracy (train) [%]   | 86.933 | 86.906 | 25.531 | 78.363 |
| Top-1 accuracy (test) [%]   | 36.125 | 36.078 | 8.980  | 30.305 |
| Top-5 accuracy (test) [%]   | 59.473 | 59.468 | 19.359 | 53.355 |

Table 4.9: ImageNet-MOE accuracy

The ImageNet-MOE model only reached 36.125% on the ILSVRC validation set, however the training set scores hint that the network is fully capable of learning the task. It is likely that our choice of gating selector (see Section 1.5) is not optimal yet. It is difficult to tune the amount of noise and the learning rate of the regularizer so that the experts learn optimally. We still observed some experts being disabled completely, while one expert was used for every sample. This reduces the learning capability of the network drastically. A more elaborated gating selector [10] might also improve accuracy.

Interestingly, for both ImageNet and ImageNet-MOE, the INT16 score is lower than on INT8, hinting at possible integer value casting problems either in the implementation or the compilers. Since there are not many reasons to use the INT16 data type on the devices and networks we tested, it is probably not a good choice for any real use-case, except for toy examples like the celsius-farenheit conversion example (see Section 4.4.1 and 2.1) or on embedded devices with no hardware floating point capabilities.
Chapter 5

Conclusion

5.1 Implications

We successfully implemented a more versatile backend for Caffe, allowing to use a large variety of compute libraries, hardware backends, devices and data types. The added flexibility will allow more use cases for Caffe, and position it as a go-to choice in applications that have to be distributed over a large variety of different hardware.

Our new models, compute paths and improvements to the memory system of Caffe also enable up to $3.29 \times$ less memory usage, while increasing inference speed up to $3.01 \times$ on certain devices. This can make the difference of being able to use neural networks on low-power devices or not.

5.2 Difficulties Encountered

While implementing quantizers (see Section 1.4) and device abstraction (see Section 1.4) was challenging from a software engineering perspective, the most annoying and difficult issues were bugs in the drivers of GPUs from all vendors. Until the latest updates (May 2018) were available from both AMD (ROCm 1.8) and nVidia (CUDA 9.2), certain operators (FP16 and INT8) did not work at their full speed, and certain kernels did not compile at all. This was most likely due to immature compilers that did not handle the OpenCL and CUDA kernels optimally for the latest GPU architectures. For the Intel GPU, no update was released yet to remedy their bugs on the FP16 implementation (see Table 4.1).

Finally, finding the right hyper-parameters to configure the MOE layer (see Section 1.5) and train the modified ImageNet/AlexNet [15] was frustrating, since it only becomes apparent if a model will converge or not at a rather late stage in training, typically after 5 to 8 hours (100'000 iterations). Only when training a seemingly non-working configuration from start to finish once, did it suddenly begin to work. It seems like neural networks, when becoming increasingly complex, such as adding divergent code paths, remain black boxes [27] and definitely have a personality on their own.
Unfortunately, the very extensive scope of this project, unusual circumstances and computer driver problems made it difficult to arrive at the desired results in a reasonable time-frame.

## 5.3 Reproducibility of Results

The results obtained in this project can be reproduced by the use of the following software pipeline, using CUDA or OpenCL hardware equivalent to the hardware used in this project.

Repositories belonging to the OpenCL Caffe Project:

- Caffe OpenCL development branch [3]
  URL: [https://github.com/naibaf7/caffe](https://github.com/naibaf7/caffe)
- Caffe OpenCL release branch [3]
  URL: [https://github.com/BVLC/caffe/tree/opencl](https://github.com/BVLC/caffe/tree/opencl)
- Caffe Examples [16]
  URL: [https://github.com/naibaf7/opencl_caffe_examples](https://github.com/naibaf7/opencl_caffe_examples)

## 5.4 Outlook

While the new Caffe code provides a solid basis for future developments, allowing to now easily program for both OpenCL and CUDA, without divergent code paths, there are still many points that need improvement:

- Performance on ARM devices and mobile GPUs is still not optimal. Additional hardware-specific libraries such as the ARM compute library [28] should offer improvement over the current approach of using LibDNN as a fallback library for all devices.

- OpenCL performance for desktop GPUs can be improved further. Adding AMD's new HIP [17] compute backend and accompanying compute libraries may help with performance.

- The Python interface could now easily include a way to write GPU layers. This would allow the users to prototype GPU layers without the hassle of changing the Caffe core library and recompiling.

- MobileNets [29] have been deemed suitable for low-power and embedded application. These could also be ported to Caffe and be optimized for lower precision, embedded GPUs, and could potentially be improved even further by applying mixed-precision and the mixture-of-experts pattern (see Section 1.5).
5.5 Final Words

This project, for now, concludes our development efforts on OpenCL Caffe. Through working on the OpenCL Caffe project since 2014 [4, 5], I gained a full-stack development experience in the realm of deep learning. These efforts, as a cumulative product, enable more people to use deep learning effectively. I was able to implement most of the originally planned features and to gain deep learning community interest in the project.

Continued hardware sponsoring and collaboration by Intel [30] and AMD [31] shows that such efforts to diversify the development of deep learning libraries continue to be highly important for industry, end-users and scientific progress.
Appendix A

Models
A. Models

A.1 Caffe-ImageNet

Figure A.1: Standard AlexNet/CaffeNet/ImageNet [15]
A. Models

A.2 Caffe-ImageNet-MOE

A.2.1 Main Network

Figure A.2: Main mixture-of-experts ImageNet
A.2.2 Gating Network

The gating network is executed within the MOE-Layer.

Figure A.3: Gating network of the mixture-of-experts ImageNet
Figure A.4: Gating network of the mixture-of-experts ImageNet
A.2.3 Expert Network

The expert network is repeated 16 times within the MOE-Layer.

![Expert Network Diagram]

Figure A.5: Expert network of the mixture-of-experts ImageNet
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