Method for reducing phase fluctuations of a precision frequency response meter for microwave quantum generators

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Abstract: The principle of operation of the device for measuring frequency characteristics is considered. Block diagram of a device for measuring the frequency characteristics of a digital frequency comparator with correlation quadrature processing and description of their components is illustrated. The block diagram of the frequency multiplier is given. The accuracy characteristics of the developed meter design are evaluated. They are compared with the characteristics of previously used devices. The improve accuracy characteristics and increased stability of operation were found.

1. Introduction
In modern navigation systems, without determining the exact time and frequency, it is impossible to achieve the required accuracy in determining the coordinates of the object [1-10]. The data on the coordinates of the object are necessary when solving problems of environmental monitoring, carrying out various works, etc. [10-19]. In operating satellite navigation constellations, quantum frequency standards (QFS) are actively used to determine the exact time [1, 2, 8, 20-24]. There are a number of problems with these devices [23-27]. One of them is the work of a precision meter. A precision meter helps to solve the problem of the occurrence of phase fluctuations introduced by the frequency multiplier [20-22, 25, 27-31]. In the precision meters of the old generation, there were fluctuations in the signal phase, when it exposed to noise, pulsation of power sources, spurious signals at the input and noise on the reactive circuits of frequency multipliers. Phase fluctuation is a form of linear distortion caused by the deviation of the transmitted signal from the carrier frequency.

This frequency comparator in precision counting frequencies is designed to measure frequency instability and estimate the spectral density of phase fluctuations of signals of quantum frequency standards [30-37]. Precision meters have been developed for a long time, but still need to be upgraded. Device development is important to test the onboard system with higher accuracy.

2. Methods of measuring frequency characteristics

2.1 The method of electronic counting frequency meter
The principle of operation of digital meters is to count the number of pulses by an electronic counter, which is a function of the measured value, during the counting of t.
The device is a device that registers, depending on the operating mode, the number of cycles of the test signal or the sample frequency signal for the time set by one of these signals. The main elements of the electronic counting frequency meters are an electronic pulse counter, a forming device, a time selector, and a selector control device [20-29, 30-34, 38].

![Block diagram of an electronic counting frequency meter.](image)

Figure 1. Block diagram of an electronic counting frequency meter.

2.2 The prototype

An analog-to-digital conversion of the measured signal is performed with a time sampling interval determined by the frequency $f_s$ of the sampling signal formed from a reference signal with a frequency $f_0$ in accordance with the expression $f_s = 4f_0$.

A device for measuring the frequency of a harmonic signal, adopted as a prototype, implementing the prototype method, contains a series-connected generator of the measured signal, an analog-to-digital converter, a random-access memory device and a digital signal processing processor connected by a data exchange bus with a personal computer. The synchronization input of the analog-to-digital converter is connected to the output of the frequency synthesizer of the quantization signal, the input of which is connected to the output of the reference signal generator. The synchronization input of the analog-to-digital converter is connected to the output of the frequency synthesizer of the quantization signal, the input of which is connected to the output of the reference signal generator. In the process of implementing the prototype method, the measured signal generator generates a harmonic (sinusoidal) signal at its output, which is fed to the signal input of the analog-to-digital converter. The synchronization input of the analog-to-digital converter receives a sampling signal (quantizing pulses). Quantizing pulses are formed using a quantization signal frequency synthesizer, which performs the operation of multiplying "by four" the frequency $f_0$ of the reference signal coming from the output of the reference signal generator to the signal input of the quantization signal frequency synthesizer. The analog-to-digital converter performs analog-to-digital conversion of the measured signal with a time sampling interval determined by the sampling signal that is, $t_s = \frac{1}{4f_0}$. This ensures a phase shift between adjacent samples of the measured signal equal to $\frac{\pi}{2}$.

The disadvantage of the prototype method and the prototype device is a significant limitation of the frequency range of the compared signals. Indeed, let be the maximum operating frequency of analog-to-digital conversion and digital sample storage operations. Then the frequency range of the amplified signals is limited from above by the following relation: $f_s \leq \frac{f_{\text{max}}}{4}$.

In difference to the prototype, an analog-to-digital conversion of the reference signal is additionally performed with a time sampling interval determined by the specified frequency $f_s$ of the sampling signal formed in accordance with the expression: $f_s = \frac{4f_0}{5(2+2j+1)}$, where $j = -\frac{2}{5}, 0, 1, 2, 3, ...$ it depends on the frequency range of the compared signals.

For example: let the maximum operating frequency of the hardware implementing the prototype method and the claimed method be 20 MHz. When comparing signals with a nominal frequency of 5
MHz, as is done in the example implementation of the prototype method, the sampling signal frequency \( f_s = 20 \text{ MHz} \). Exactly the same sampling frequency can be selected for the claimed method at \( j = -\frac{2}{5} \). Suppose you want to measure the frequency difference with nominal values of 100 MHz. For the prototype method, \( f_s = 400 \text{ MHz} \gg 20 \text{ MHz} \), which makes the prototype inoperable with the specified implementing hardware. The claimed method remains workable for measuring frequencies with such a nominal value, since, taking \( j = 2 \), we get \( f_s = 16 \text{ MHz} \leq 20 \text{ MHz} \).

The frequency response measurement device is designed to measure the frequency characteristics of quartz oscillator signals, frequency and time standards, and frequency synthesizer signals [1, 2]. An integral part of the operation of this device is the formation of a time discredit signal synchronized with one of the input matched signals, and the conversion of the input signal voltages into digital codes of quadrature components, storing these codes in the receiving computing device [2, 3]. As well as the power supply device of the board converts the AC voltage (220±22 V) 50 Hz into a DC reference voltage power supply plus 24 V.

The reliable stability of the master generator is \( 10^{-15} \), therefore, the precision meter must be at least 3 times more accurate to detect problems [2, 3].

![Block diagram of frequency response measurement device](image)

**Figure 2.** Block diagram of frequency response measurement device of a digital frequency comparator with correlation quadrature processing, where 1 and 3 are an ADC, 2 – frequency multiplier by 4, 4 – digital signal processor (DSP), 5 – field-programmable gate array (FPGA), 6 - Micro Controller Unit (MCU).

The PLL circuit is designed for coherent synthesis of the generator output signal with the sinusoidal signal of the measuring channel. Switching scheme – for controlling the modes of operation of the frequency response measurement device. ADC of the reference channel – for converting the voltage of a reference sinusoidal signal with the clock frequency of a quartz oscillator coherent with the measured signal into a hexadecimal bit code. ADC of the measuring channel - for continuous conversion of the voltage of the measured sinusoidal signal with the clock frequency of a quartz oscillator coherent with the measured signal into a hexadecimal bit code. FPGA – for managing the modes of operation of the frequency response measurement device.

The frequency of one of the matched signals is multiplied by four and the signal from the output of the frequency multiplier is used to take digital samples of the harmonic input signal. The digital signal processor receives digital codes of voltage samples of the measured signal, averages them and filters them to form a code proportional to the phase difference and frequency of the compared signals. A time sampling signal with a nominal frequency of 20 MHz allows you to calculate phase samples of the measured signal every 50 ns. at the same time it forms the quadrature components of the compared
signals. Therefore, at the data inputs of the digital signal processing processor (DSP), there are four types of samples: \( a_i \); \( b_i \); \( c_i \); \( d_i \), following with a nominal period of 0.2 microseconds in each channel.

Depending on the processor speed, the DSP processes the codes of these samples, for example, after a time interval of 1 microsecond, it depends on the processor speed.

- \( S_a, 1 \text{ мкс} = \{ a_1, a_2, ..., a_N \} \)
- \( S_b, 1 \text{ мкс} = \{ b_1, b_2, ..., b_N \} \)
- \( S_c, 1 \text{ мкс} = \{ c_1, c_2, ..., c_N \} \)
- \( S_d, 1 \text{ мкс} = \{ d_1, d_2, ..., d_N \} \)

The DSP processor converts the sample data into a phase difference and a frequency difference.

3. The 1321HD1U chip

The radio receiver chip 1321HD1 allows to receive and process a radio signal at frequencies in the range of 10-300 MHz. To amplify the received signal and transfer it to an intermediate frequency, a built-in low-noise amplifier, a mixer and a PLL system with a fractional division coefficient are used. The received signal is divided into a direct and a quadrature signal and converted into a digital code by a band-pass \( \Sigma \Delta \)-ADC and a digital quadrature demodulator. The chip implements an AGC system with a range of 24 dB, as well as the ability to manually adjust the gain of the LNA in the range of up to 15 dB. The ADC and the digital filter block are clocked from an internal PLL with a built-in active part of the VCO. Also, the chip allows to process a signal with a minimum noise factor in the band up to 25 kHz and in the band up to 200 kHz with some degradation of the noise factor.

3.1 Description of the operation of the chip

The input signal at a carrier frequency from 10 MHz to 300 MHz, passing through an external 50-ohm matching chain of the signal source, with a 500-ohm input of the built-in LNA, is amplified with a gain of 17 to 0 dB, depending on the user's settings, and converted to an IF frequency, which is \( F_{clk}/8 \), where \( F_{clk} \) is the clock frequency of the ADC. The frequency of the local oscillator can be supplied either from an external oscillator or generated using an internal PLL with a fractional division coefficient. To eliminate blockers, the chip provides two tunable first-order filters, which also act as anti-reflection filters before the ADC input. The cut-off bands of these filters are also configured via the control registers. To eliminate quantization noise and obtain the required sampling frequency of the direct and quadrature channels, the signal from the output of the digital quadrature demodulator is fed to the input of digital decimator filters with an adjustable decimation coefficient. After filtering, the signal is formatted according to the specified format, and transmitted to the user via the SSI interface. The values are written to the control registers via the SPI interface.

3.2 The composition of the 1321HD1U chip

The integrated circuit consists of:

- low-noise amplifier (LNA), with the possibility of reducing consumption while reducing the gain in steps of 3-4 dB;
- mixer, with the possibility of reducing consumption by reducing IIP3;
- active low-pass filter (LPF), with tunable cut-off band;
- Bandpass Delta-Sigma ADC;
- digital demodulator;
- a block of digital decimator filters, with a programmable decimation coefficient;
- PLL of the local oscillator, with the fractional and integer parts of the output frequency divider;
- reference frequency buffers;
PLL of the clock signal synthesiser;
SPI interface, for IC programming;
SSI interface, for transmitting digital samples for further processing;
reference voltage and current sources

4. Conclusion
Our review shows that the claimed group of inventions is feasible and provides the achievement of a technical result, which consists in increasing the accuracy of measuring the frequency of a harmonic signal while expanding the frequency range of the compared signals.

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