FPGA Realization of ANFIS Controller Using a Proposed Digital Design

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Abstract. The design and realization of Adaptive Neuro-Fuzzy Inference System (ANFIS) controller based on Field Programmable Gate Array (FPGA) is presented in this paper. The controller intended to control the temperature of medical oven. A novel design of digital ANFIS is presented here for the implementation process. Different controllers are designed and their results are compared using MATLAB program to show the ANFIS superiority. The designed controllers tested for cell cultures application at 37.5°C. A reduction is made for the designed digital ANFIS due to the used FPGA limitations. The reduced design minimizes the utilized slices from 366% to 3% and LUTs from 364% to 3%. The reduced design reached an optimum size for this controller to utilize a smallest memory size. A real-time FPGA implementation of the proposed digital ANFIS have been done and verified through Xilinx ISE 14.6 using the VHDL language. The VHDL code for the controller is produced, aggregated and downloaded on the FPGA Spartan 3A/AN FPGA kit. A comparison between the simulation and implementation results is made. The matching between these results proves the effectiveness and robustness of the proposed digital ANFIS and the excellent performance of the FPGA based controller.

Keywords: Medical Oven Modeling; PID; NN; ANFIS; Digital ANFIS; FPGA.

1. Introduction
The control of temperature of sensitive for many applications such as medical and biological is an important issue especially when the temperature is a critical condition. The examination of precise and proficient automation that fit for serving such applications is the purpose for the choice of a powerful and appropriate regulator to meet these prerequisites.

The medical ovens take an extraordinary unmistakable quality for their delicate essentials of an exact control. The customary strategies don't give the necessary control exactness; such stoves need profoundly adjusted regulators to guarantee a high quality and well-being creation [1].

FPGA is a pure hardware, so it’s suitable to control the temperature. The reliable, field programmable, flexible in design and small size characteristics of FPGA increase its suitability [2]. Different control procedures were applied on temperature frameworks, such as Proportional Integral Derivative (PID), Neural Network (NN), Fuzzy Logic Controller (FLC) and others [3]. The mix of the two technologies; Artificial Neural Networks (ANN) and Fuzzy Inference System (FIS) can give better technology that can take the advantages of each methodology’s strength, and simultaneously overcome some of the individual techniques limitations. The hybrid Neuro Fuzzy controller is a powerful technique that used to limit the disadvantages of the Fuzzy Logic System (FLS) and ANN. The challenge is the
implementation of these intelligent controllers on integrated circuits. The most competitive one is the FPGA which is the best in capacity and performance. The FPGA is convenient for fast implementation and verification [4].

A number of researches are made in the field of implementing NN and FL on FPGA with different systems.

Z. Runjing et al (2011), proposed Fuzzy controller based on FPGA that controlling the temperature in order to meet the clinical requirements [2]. Bouhedda M. (2013), presented ANFIS linearizer based on FPGA to linearize the nonlinear sensor's characteristic [5]. T. Tamas et al (2015), presented an implementation and design flow of NFC Intellectual Property core (IP) for FPGA by using Xilinx Vivado the High-Level-Synthesis tool (HLS) and C-language, the design implemented using the integer operation only [6]. C. eddine LACHOURI et al (2016), introduced an (FPGA) execution of "(ANFIS)" for controlling temperature and humidity inside a tomato nursery. The recreation results have indicated the productivity of the actualized regulator [7]. H. Layla et al (2018), the reason for utilizing the single neuron PID regulator is to produce an ideal mixture rate as a control signal by self-adjustment for PID regulator boundaries and afterward execute it on FPGA. The Simulation results show the effectiveness of the recommended control conspires in following the ideal BIS for every one of patients' cases [8]. M. Reem et al (2018), proposed a mobile robot with an “Artificial Neural Network (ANN)” regulator executed on Altera FPGA small board with remote ability to move to a particular distance by staying away from the deterrent. This framework utilizes a Nios II/e delicate center processor started up in ANN control of the motors dependent on the information given by the sensors. The plan shows adaptability in equipment and programming, where the plan can be adjusted effectively by embedding more mind boggling capacities because of the limit of FPGA as opposed to a current microcontroller or microchip based plan. [9]. A. H. Issa et al (2021), proposed a reconfigurable intelligent controller for mobile robot. The control system architecture was modified by software called reconfigurable control system, and the controller was designed and executed utilizing “Field Programmable Gate Array (FPGA)” technology [10].

For reducing complexity and cost, a proposed digital ANFIS controller designed in this research. A real-time FPGA implementation has been accomplished and verified through Xilinx ISE 14.6 of the proposed digital design for the medical oven. The VHDL code for the controller is produced, aggregated and downloaded on Spartan 3A/AN FPGA kit.

This paper made out of six sections, the first sections is the introduction and related works, the second is to clarify the essential idea of the heating system modeling, the third explains the architecture of ANFIS, the simulations and results in section four, the section fifth explain the FPGA implementation, the last section is the conclusions.

2. Heating System Modeling

![Figure 1. The controlled heating system block diagram.](image-url)
The mathematical model for the Laboratory Oven has been inferred relying upon heat move conditions [11], [12], and the Laboratory Oven configuration highlights it is a blend of radiation and convection, as given in the equations (1) to (10) respectively [13].

\[ Q_{acc}(t) = Q_{in}(t) - Q_{loss}(t) \]  
\[ \text{Where, } Q_{acc}(t) \text{ presents the accumulated heat, } Q_{in}(t) \text{ is the input heat and } Q_{loss}(t) \text{ is the lost heat.} \]

\[ M C_p \frac{dT_o}{dt} = Q_{in}(t) - (Q_{conv} + Q_{rad}) \]  
\[ M \text{ represents the Mass flow; } C_P \text{ is Specific heat under constant pressure, } T_o \text{ is the Oven temperature, } Q_{conv} \text{ is convection heat and } Q_{rad} \text{ is radiation heat.} \]

\[ \frac{dT_o}{dt} = \frac{1}{M C_p} Q_{in}(t) - \left[ \frac{(h_{conv} + h_{rad}) h_{wall}}{M C_p} (T_{wall} - T_{air}) \right] \]  
\[ \text{Where, } h_{conv} \text{ and } h_{rad} \text{ are the convection and radiation coefficients of heat transfer respectively.} \]

\[ R = \frac{1}{h A} \]  
\[ \text{To simplify the analysis} \]

\[ C = M C_p \]  
\[ \text{And by compensation equation (5) in equation (3) yields} \]

\[ \frac{dT_o}{dt} = \frac{1}{RC} [R Q_{in}(t) - (T_{wall} - T_{air})] \]  
\[ \text{In steady state:} \]

\[ RC \frac{dT_o}{dt} = R Q_{in}(t) - T_o \]  
\[ \text{Let, } \tau \text{ is time constant } = R C , T_o = X \text{ and } R = K , \text{ substitute in (7):} \]

\[ \tau \frac{dx}{dt} + X = K Q_{in}(t) \]  
\[ \text{By using Laplace transform for equation (8) we get} \]

\[ \tau S X(S) + X(S) = K Q_{in}(S) \]  
\[ \text{Finally, the transfer function is:} \]

\[ G(S) = \frac{K}{(\tau s + 1)} e^{-\tau a s} \]  

3. **Architecture of ANFIS**

The learning stage based the adaptation reliant; it is a trademark ANFIS feature [14]. The architecture of ANFIS is shown in Figure 2. The primary request Takage-Sugeno ANFIS regulator planned here to have two data sources (error (e) and change in error (de)) and one yield. The hybrid-algorithm is the pre-owned learning procedure for information preparing. Ordinarily, the ANFIS component has two data sources and one yield dependent on the normal IF-THEN Takage-Sugeno rule [15], [16]:

Related to Figure 2;

*If e is Ai and de is Bi, then;*

\[ P_j = k_{0j} + k_{1j} + k_{2j} \]  
\[ \text{Where, } P_j \text{ is the output, } j \text{ is the principles number and } k \text{ is resulting boundary.} \]

The ANFIS structure has 5 functions of fundamental layers’ as given:

**Layer-1:** This layer creates the MFs (**Fuzzification layer**).
Layer-2: The terminating strength is produced present here as the principles input space (Rules layer).
Layer-3 This layer normalizes the layer-2 outputs (Normalization layer).
Layer-4 ascertains the guidelines weighted resulting parameters (Defuzzification layer).
Layer-5 ascertains the general outcomes of the ANFIS (Summation layer).

The algorithm of ANFIS learning is a mixture which is a mixing of two sections:

1- Move forward to ascertain the output (parameters of subsequent) till layer-4 using the algorithm of Least Square method.
2- Move backward to ascertain parameters of the input MFs (parameters of premise) utilizing the algorithm of steepest-descent method.

Figure 2. The ANFIS architecture.

4. Simulation Results
The medical oven is a practical laboratory oven has a transfer function with first order and time delay as:

\[ G(s) = \frac{0.7}{13.35 + 1}e^{-26s} \]  \hspace{1cm} (12)

The program is simulated in MATLAB for heating system. The open loop reaction of the oven is appeared in Figure 3. The close loop framework recreated with various regulators to show the ANFIS prevalence over different regulators and over give the appropriate preparing information to the ANFIS. The time of sampling is 1 second, the signal of control reaches from 0 watt - 250 watts as indicated by the heater constraints. The heater constrained by a TRIAC power switch utilizing various regulators recorded as, PID, NN and the ANFIS to make the oven temperature keep at 37.5°C for cell cultures application. The simulation results are shown in Figure 4; it very well may be seen from the outcomes that the designed ANFIS regulator give some ideal outcomes surpasses different regulators.
5. FPGA Implementation
In order to implement the ANFIS controller on FPGA board, a proposed digital ANFIS is designed here. The proposed design architecture and performance will be clarified in the next sections.

5.1 Proposed Digital ANFIS Design
The new design is depending on the simplified output equation of the ANFIS controller as given in (13).

\[
O_f = \frac{\sum_{i=1}^{\vartheta} w_i Z_i}{\sum_{i=1}^{\vartheta} w_i}
\]  

(13)

Where, \(O_f\) represents the final output of the digital ANFIS controller, \(Z_i\) is the polynomial of the premise parameters as indicated in Figure 5.
Therefore, the new design is reduced in size with exactly the same output response as indicated in Figure 6 in a comparison with the MATLAB-based ANFIS controller.

A reduction process has been made on the digital ANFIS, where only the effective parts of the design are taken. This process reduces the number of Membership Functions (MFs), rules and consequently, the utilized blocks of the digital ANFIS. The reduced design represents the optimum design of the proposed digital ANFIS. The reduction process minimized the controller size to be suitable for the implementation on Spartan 3A/AN FPGA. The comparison of the reduced and unreduced digital ANFIS is shown in Figure 7.
The next step is the implementation of the digital ANFIS on FPGA. The implementation and verification process has been done through connecting the FPGA kit with the Laptop which represents the simulated heating system via USB cable as shown in Figure 8.

5.2 FPGA Realization

The design summery reports for the implementation of the unreduced and reduced digital ANFIS are shown in tables (1) and (2) respectively.
As shown in Table (1) and (2), the reduced digital ANFIS controller used 364 of the input LUTs so utilizes 3% of the available and 437 as total number of the four input LUTs where still utilizes 3% of the total available number. The number of occupied slices is 229 so, it utilizes 3% of the available number of slices, and took an 11 of MULT18X18SIOs so utilizes 55% from the available number.

The reduced digital ANFIS controller gives an optimum design for the used application. The reduced design takes a very small area from the available of Spartan 3A/AN FPGA saving in that the chip size and cost.

After downloading the digital ANFIS, the FPGA externally connected to the PC (Laptop). The conventional controller of the heating system in MATLAB Simulink replaced by the real FPGA kit as
the hardware ANFIS controller for the Lab Oven as illustrated in Figure 9 and then making the verification.

![Figure 9. The controlled heating system based Real-Time FPGA controller.](image)

The verification of the implemented ANFIS controller based on the FPGA is shown in Figure 10.

![Figure 10. Implementation and verification setup.](image)

After running the heating system simulation with the FPGA as the ANFIS controller, the results for the cell cultures application were obtained. These results compared with the simulation results of the reduced digital ANFIS controller before the implementation as indicated in Figure 11.
Figure 11. The heating system response comparison for the reduced digital ANFIS controller before and after hardware implementation based on the FPGA.

6. Conclusion
The obtained results show that the ANFIS controller is more suitable for sensitive medical applications. The proposed digital ANFIS controller gives results that very close to that of MATLAB-based ANFIS controller. The basic Digital ANFIS design can be used for any other application just with varying the constants. It can easily use without the need for recalling the FIS of the designed ANFIS controller every time it opens and run with the system simulation. The digital ANFIS controller has the possibility to be reduced to an optimum size. The reduced digital ANFIS controller gives exactly the same response as the controller before reduction with smaller size. The ANFIS controller of reduced size can be implemented on a smaller chip reserves in that the size and consequently the cost. A real time FPGA implementation has been accomplished and verified using representation of system in PC and that gives a lessening as expected and cost with exact performance.

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