Implementation of digital constant fraction timing based on field programmable gate array

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Abstract. Compared with analog circuits, FPGA(Field Programmable Gate Array) had the advantages of redevelopment and low cost. Compared with MCU, FPGA used hardware description language to construct the circuit, which had the advantages of simple structure and fast parallel operation speed. In this paper, the simulation of digital Constant Fraction Timing can be realized based on FPGA, and the feasibility and accuracy of the design can be proved by using the simulation waveform of Modelsim and the waveform can be captured by signaltap. Modelsim can verify the correctness of the timing between modules, and signaltap can verify the actual running effect of the program on the board.

1. Introduction

In the field of trigger detection of high-frequency pulse signal, the requirements of signal detection technology keep rising with the development of electronic technology. The timing discriminator can detect the trigger signal. It can quickly convert the analog signal into digital signal to count the high frequency pulse and accurately record the arrival time of the pulse to deal with the time relationship of physical events. It is mostly used for nuclear signal detection and radar signal processing.

The purpose of the timer is to accurately correspond the output digital signal with the input analog signal in time. According to different timing principles, there are Leading Edge Timing (LED), Constant Fraction Timing (CFD) and Zero Crossing Timing (ZCD) [1]. This paper mainly analyzes the Implementation of digital CFD.

CFD was originally designed and manufactured by M. M. Maier in 1980 [2]. It is an important timing technology, which is used to accurately determine the incident time of particles in particle physics and nuclear physics experiments.

Before CFD was put forward, Led was often used, but Led was greatly affected by the change of signal amplitude. CFD technology can adjust the trigger ratio by adjusting the attenuation coefficient, which is a new generation of timing technology developed on the basis of zero crossing timing. CFD generates zero crossing at a constant proportional point of the input pulse amplitude [3]. It not only uses ZCD technology, but also can adjust the trigger ratio to the best to reduce time jitter. Therefore, CFD combines the advantages of ZCD and LED, greatly improves the timing accuracy, and is the most widely used timing method in particle physics and nuclear physics [4]. The principle of CFD greatly improves the time error caused by the change of signal amplitude. With the characteristic that
its trigger is independent of the pulse amplitude, it can adapt to the advantages of digital signal trigger of a variety of pulse signals, and is widely used in the field of time measurement [5].

CFD has analog CFD and digital CFD, and at present, analog CFD is widely used. Analog CFD circuit consists of amplifier, delay circuit and high-speed comparison circuit. There are many disadvantages in CFD based on analog circuit. One is high cost, complex operation and many mistakes, which need to be investigated one by one [6]. Second, the analog circuit has a natural defect in the realization of delay, because it can not register in the middle and store data for a long time, so it is difficult to realize CFD based on analog circuit. However, digital CFD has a natural advantage, which can realize the intermediate storage of data, realize the delay of signal, and has a higher anti-interference ability, which can greatly avoid the interference of environment and equipment, and also can improve the accuracy of timer to a certain extent. Compared with analog CFD, digital CFD is more convenient and widely used because of its programmability. This paper will implement the simulation of digital CFD based on FPGA.

2. Principle

CFD generally consists of three parts: attenuation, delay and comparison. The principle of CFD is to take the constant proportion point of the front edge of the input analog signal for timing trigger to form a standard digital signal [7]. The trigger point of the digital signal is only related to the constant proportion point of the leading edge, and has nothing to do with the amplitude of the signal or the width of the leading edge. In general, CFD divides the input signal into two parts according to the flow chart in Figure 1, one part of the original signal is delayed, the other part is attenuated by the attenuation circuit, and then the delayed signal and the attenuated signal are compared and triggered by the comparator to form a digital signal [8].

![Figure 1. CFD flow chart.](image)

In the process of CFD processing, the selection of constant proportion point is very important. Before Constant Fraction timing, the original signal needs to be measured to obtain the maximum amplitude U and leading edge time t of the signal. Then the constant ratio timing delay time T is calculated, and the delay time T needs to satisfy \( T = (1 - f)t \), where f is the attenuation ratio, and the attenuation ratio of f can be adjusted.

In this paper, FPGA is used to process the signal, so ADC is needed to convert the analog signal into digital signal in the front-end of signal acquisition. The signal processing part will use CFD design to process the signal, and the signal output part will use uart serial port to transmit to the host computer. The upper computer can adjust the attenuation index f in real time, so as to adjust the delay time t. the attenuation index and delay time t satisfy \( t = (1 - f)T_{\text{max}} \), which can ensure the accuracy of signal trigger.

The upper computer is mainly composed of waveform acquisition monitoring and constant ratio control. Through waveform acquisition monitoring, the original signal and trigger signal are sent to the upper computer through serial port, and then displayed on the upper computer through waveform chart, so as to better observe the effect of signal acquisition and trigger. Constant ratio proportional control
can process more different types of pulse signals by setting transverse ratio proportional coefficient, which improves the application scope of the design.

3. Experimental design
This paper uses Verilog language to realize CDF, which is mainly divided into five parts: original signal storage, mean filtering, signal delay, signal attenuation and comparator. The original signal stored in the ROM block is filtered by the mean filtering module, one is delayed and the other is attenuated. Finally, the trigger signal is obtained by comparing the attenuated and delayed signal through the comparator.

The procedure is as follows:

3.1. Using ram block ROM of IP core to store original signal
Create a new IP core file single port ROM, set the depth of ROM to 1024 and the width to 8bit, and call MIF file to complete the single port ROM call. ROM core is used to store the collected signal.

3.2. Mean filtering
Mean filtering algorithm is to remove high-frequency noise by adding the continuous data to get the mean value. The Formula is as follows:

\[ y = \frac{\sum_{i=n}^{n+1} x_i}{n} \]

Select \( n \) as 16. In order to realize the mean filtering, 1024 values need to be divided into 64 groups with 16 values in each group. The register \( a_{-p} \) is set to zero. When the count value \( i \) is 1023, register \( a_{-p} \) is set to zero. In order to register 16 consecutive values in register \( a_{-p} \), the lower 4 bits of \( i \) are assigned to register \( a \) with the join operator (the value of \( i \) is the same as the address addr of reading the original signal), the data is read into register \( a_{-p} \) from 0 to 15 by using case statement, and then the values in register \( a_{-p} \) are added every time, and the average value is taken to get the signal \( \text{data\_in\_lvbo} \) after mean filtering. The mean filter code is shown in Figure 2.

![Figure 2. Program implementation of mean filter.](image)

3.3. Signal attenuation
The procedure of signal attenuation is shown in Figure 3 where \( f \) is the attenuation index, \( \text{data\_register\_a} \) stores the attenuated data for the attenuation register, and attenuates the data at each rising edge of the clock after reset.
3.4. Signal delay

The program of signal delay is shown in Figure 4, where data_register_b is the delay register, which stores the data after delay, and the delay $t$ should meet the relationship of $(1 - f) \times T_{\text{Max}}$. $T_{\text{Max}}$ is the leading edge time of the signal.

```verilog
always@(posedge clk or negedge rst)
begin
    if(!rst)
        data_register_a<="b00000000;
    else
        begin
            data_register_a=data_in_lvbo; // data_in;
        end
end
```

**Figure 4.** Program implementation of Signal delay.

3.5. Comparator

The comparator program is shown in the Figure 5, where data_out is the final output data. In each clock cycle, judge whether the attenuation signal is less than or equal to the delay signal, if so, trigger the signal data_out is set to 1, otherwise it is set to 0.

```verilog
always@(posedge clk or negedge rst)
begin
    if(!rst)
        data_out<='b0;
    else if(data_register_a<data_register_b)
        data_out<='b1;
    else
        data_out<='b0;
end
```

**Figure 5.** Program implementation of Comparator.
uart serial port sending module is divided into frequency division module and sending module. The frequency division module is composed of transmission control module, baud rate selection module, frequency division clock module and counting module. The control module selects to set the flag bit uart_state to 1, 0 or remain unchanged by the input control signal send_en. When send_en signal is 1 (send_en signal only holds one clock cycle), the flag bit uart_state is set to 1. When the tx_done signal is 0, the uart_state signal remains unchanged during the next few clock cycles. When tx_done signal is 1, uart_state is set to 0. Baud rate selection module, by setting baud rate parameter baud_set, select the baud rate to confirm the maximum count value baud_dr of a frequency division counting clock cycle. The frequency division clock sending module generates the frequency division clock signal bps_clk according to the maximum value of the frequency division count. The counting module provides address for the data selector to send data in each frequency division counting clock cycle.

The serial port receiving module is similar to the serial port sending module, which consists of three parts: frequency division module, receiving module and baud rate selection module. By setting the baud rate parameter baud_set and using the 5-bit selector structure to select the baud rate to confirm the maximum count value baud_dr of a frequency division counting clock cycle. The frequency division clock sending module generates the frequency division clock signal baud_clk according to the maximum value of the frequency division count. The counting module provides address for the data selector to send data in each frequency division counting clock cycle. The frequency division clock sending module generates the frequency division clock signal baud_clk according to the maximum value of the frequency division count. The counting module provides an address for the data selector to receive data in each frequency division counting clock cycle.

Because the baud rate of serial port is relatively fixed and can not be synchronized with CDF processing, a dual port ram is designed to store the waveform data after triggering. The dual port ram stores the trigger signal from the CFD trigger module. In order to avoid the loss of the signal, the write address of the dual port ram follows the rate of the constant ratio timing trigger module, and each clock cycle automatically increases once, while the read address follows the clock bps_clk after the frequency division of the serial port sending module. Because of this design, in the face of the original signal instability, signal loss may occur, so this design can only deal with the collected stable original signal.

4. Discussion and analysis

4.1. Modelsim simulation part

In the testbench file, the timescale is set to 1ns / 1ns, the clock cycle is set to 20ns, the reset is set to 0, and the delay is set to 1 after 21ns. In testbench, the address bits should be sent to the module every other clock cycle, and the output signal should be received. The simulation program of Testbench is shown in Figure 6.

```
initial clk = 1;
ablest #(\clk_period/2) clk = ~clk;
initial begin
  rst=0;
  #(\clk_period +1) rst=1;
  #(\clk_period * 5000);
  $stop;
end
always @(posedge clk or negedge rst)
begin
  if(rst)
    addr<-10'd0;
  else if(addr<11'd1024)
    addr<-addr+10'd1;
  else addr<-10'd0;
end

Figure 6. The simulation program of Testbench.
```
When building a project, it needs to select Modelsim as the simulation tool and set Verilog as the programming language. After compiling, it can enter Modelsim by RTL simulation. The simulated waveform is shown in Figure 7:

![Figure 7. Simulation waveform in Modelsim.](image)

In the process of simulation, it is found that if the waveform is not thresholded, the output of the trigger signal will be triggered in advance by the noise signal and lead to output confusion, which makes the output waveform distortion and cannot achieve the ideal constant ratio timing effect. Therefore, this paper uses a very small amplitude waveform threshold processing, such processing has a certain impact on the width of the trigger signal, but has no impact on the signal trigger point. After mean filtering, the original signal noise is eliminated. As shown in Figure 8.

![Figure 8. Simulation waveform after mean filtering.](image)
4.2. The verification part of signaltap

In the process of grabbing the waveform by signaltap, in order to prevent the noise signal from interfering with the output waveform and unable to form an ideal digital signal, it is necessary to thresholding the data in the MIF file, and set the data points whose amplitude is less than the threshold y to zero.

The clock in signaltap is used as on-chip clock, and the pins that need to be grasped are extracted into signaltap. After compiling the integrated module, download the program into the board and observe the waveform as shown in Figure 9. Through comparison, it can be found that the waveform meets the design requirements:

5. Conclusions

In this paper, a digital CFD based on FPGA was designed for constant fraction timing algorithm, and the lower computer program design part of the design scheme was completed, including constant fraction timing processing module and serial port transceiver module. Through the waveform comparison between Modelsim simulation and signaltap, the logic feasibility of the program was verified.

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