A 8 bits, 6.2 ps resolution two-step time-to-digital converter with set-reset-based arbiters and signal tracking mechanism

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2. The proposed TDC

As Fig. 1 (a) shows, the proposed two-step TDC consists of CTDC, Coarse-Fine Interface and FTDC. The CTDC has two functions: performing the first step coarse quantization in working mode; 2) generating the calibration signals in calibration mode. TDC calibration mode will be illustrated in section 3. In working mode, CTDC first quantizes the time error between Start and Stop inputs and outputs the quantization result codewords C_{[0:14]}. In addition, the CTDC delays the Start and Stop inputs and sends the delayed signals Sa_{[0:15]} and So_{[0:15]} to the Coarse-Fine Interface. The Coarse-Fine Interface generates the time residue, which is the time error of StartF and StopF and is smaller than CTDC’s resolution. As the resolution of CTDC is a buffer’s delay time, the FTDC can only need to cover a small range of tens of picoseconds. The FTDC quantizes residue signal and outputs codewords F_{[0:15]}. Finally, in order to calculate the fractional phase error of ADPLLs, the outputs of the whole TDC are sampled by the retimed reference clock (CKR) which is the system clock of ADPLL’s digital part [7, 8].

The inputs of the TDC are illustrated in Fig. 1 (b). T_{in} is the input phase error to be measured. Start comes first, Stop signal comes later and it triggers the entire TDC sampling devices. As CTDC’s sampling devices are latch structure, it is reset when STOP are low. The outputs of the TDC C_{[0:14]} and F_{[0:15]} are sampled by ADPLL system clock CKR, which is the case for TDCs used in ADPLLs [9, 13, 23, 24, 25, 26]. It should be emphasized that the time interval T_{pre} between Stop and CKR signals is several digitally controlled oscillator (DCO) cycles [9, 25, 26], and this time can be determined during the design phase based on the simulation result of the whole TDC conversion time T_{conv}. In this design, thanks to the simplified samplers and no use of TA, the simulation result shows that T_{conv} is less than 5 DCO cycles. As a result, the T_{conv} is much less than (T_{pre} + T_{margin}) since the frequency division ratios of most ADPLLs are greater than 10 or even greater [7, 8, 9, 25, 26], so there is sufficient time for CKR to sample stable CTDC’s outputs C_{[0:14]} before the C_{[0:14]} are reset. Meanwhile, as the sampling devices of FTDC are flip-flops, the stable outputs can also be sampled.

2.1 Coarse-TDC

As shown in Fig. 2, the proposed CTDC is completely based on the delay-line structure. In TDC working mode, Cal signal is high. Input Start first propagates along the delay-line and is sampled by arbiters (Ar) when Stop is high. Since there are 15 arbiters to be triggered by Stop, a large size multiplexer is adopted. The other multiplexer have the same size with it to balance two inputs’ load.

Ar consists of two cross-coupled NAND gates and two buffers, as is shown in Fig. 3. The Ar is triggered by Stop rising edge to sample Start, and it outputs “0” if Stop is high and outputs “1” if Start is low. As its SR-based latch structure, its output C is reset to “1” when Stop is low. The two buffers here are mainly for relaxing metastable problem. Take Ar_{[0]} as an example, theoretically, if the phase error between Start and Stop is a buffer’ delay, which is about 80 ps in 180 nm CMOS process, the high-level Start signal should be sampled and the output of Ar_{[0]} should be 0. However, according to simulation analysis, the output of Ar can be stable only when the phase error is greater than 85 ps. Therefore, in order to get stable output, the Ar is deliberately designed to need extra 5 ps to respond to input. So these two buffers are designed with different delays to make the Ar have a stable output. Also, they have another function to make Start chain and Stop chain load equal. It should be emphasized that the around 5 picoseconds’ hysteresis time can also be sampled.
does not cause an erroneous TDC output, because it will be added to the residue and finally measured by FTDC.

Stop travels along the chain which has 16 switches (Sw) on it. The Sw is turned on when control signal C is low and is turned off when C is high. If Sw is on, the delayed Stop signal Out can pass through the switch to generate output signal So. In the design of Sw, two main factors are made critical: 1) the stage in which the control signal C acts should be moved backward as far as possible to make it have enough time to reach stable state; 2) the number of transistors should be as less as possible to reduce the power. Sw consists of an inverter and a NOR gate, using only 6 transistors. As Sw(0) is the first Sw in Stop chain, its control signal C(14) is the critical path. In this Sw, the Out(0) is delayed by one inverter more than C(14), which ensures that C(14) can reach stable state according to the simulations. Unlike Stop, which outputs So signals from Sw, Start passes through the entire delay chain and outputs Sa from Sw_a.

The signal tracking mechanism enables Stop to catch up with Start in steps of CTDC’s resolution. By sampling the Start with Stop, outputs C can indicate the number of buffers N (N ≤ 15) that Stop lags behind Start. In order to catch up with Sa, Stop needs to delay N less buffers than Start. So switches from Sw(15 − N) to Sw(14) are all turned on by C. Although there are (N + 1) outputs from So(15 − N) to So(15) the first output So(15 − N) is the most important because its phase error with Sa is less than a buffer’s delay, and this phase error is the phase error residue. As C(0:14) are the outputs of Ar, the result of coarse quantization is actually used as control signal to select the So(15 − N) which has the minimum delay time with Sa. For example, if the outputs from C(0) to C(14) are “001111111111111”, it indicates that Stop lags at least 2 buffers behind Start. As the whole delay time of Start is (T_{MUX} + 16 \times T_{buffer} + T_{Sw}), Stop needs to only delay (T_{MUX} + 14 \times T_{buffer} + T_{Sw}), so switches from Sw(13) to Sw(15) are all turned on and the first output So(13) meets the condition.

All CTDC’s arbiters and switches are designed the same size for good linearity. Sw_a is always on because its control signal is constant value “0”. In case the initial phase error of Start and Stop is less than a buffer’s delay and arbiters’ outputs are all high, Sw(15)’s control signal is also always low to delay Stop the same time with Sa.

2.2 Coarse-fine interface and fine-TDC

As shown in Fig. 4, Coarse-Fine Interface consists of two identical 16-input OR gates. There is a challenge in the design of the OR gate: it must have the same output response to 16 inputs, which means the gate delay must be the same for 16 inputs. Details of the OR gate are illustrated in Fig. 4. The OR gate adopts dynamic logic and it is precharged by Pre_Chrg signal, which is CTDC dummy buffer’s output. It uses two PMOS instead of one to form a symmetrical structure for output. Although the dynamic logic itself has the advantage of fast speed, the 16 NOMS of the OR gate are designed large size to further increase the speed in the evaluation stage to minimize the impact of large fan-in. In addition, the dynamic logic has another advantage of using less transistors. Under the action of OR gates, the time error between StartF and StopF is equal to the phase error residue, and this residue is measured by FTDC.

The FTDC is a Vernier delay-line structure to obtain fine resolution. As the output time residue of CTDC is less than a buffer’s delay, theoretically, the FTDC only needs to cover a buffer’s delay time. In our design, considering the PVT variations the dynamic range of FTDC is designed a little larger, which guarantees that in the worst situation the FTDC can also cover the range of CTDC’s accuracy. Since VDL-TDC is an asynchronous circuit, sense-amplifier-based flip-flop (SAFF) [27, 28] is used as sampling devices because of its very narrow sampling window. The metastability resolution window of this SAFF is less than 1 ps [29, 30], which ensures no “bubbles” in TDC’s outputs. Fig. 5 shows the SAFF and it is abbreviated as SA in Fig. 4. The SAFF’s outputs are second step fine quantification results.

3. Resolution normalization

The above descriptions are all about the TDC working mode. Before the working mode of the TDC, it needs to be calibrated for resolution normalization. The proposed TDC has a built-in calibration mechanism. Suppose that the resolution ratio of CTDC and FTDC is \( K_{res} \), the quantization result of the entire TDC should be:

\[
\varepsilon = K_{res} \times C_{out} + F_{out} \tag{1}
\]
where $\epsilon$ is the input phase error of TDC and $C_{out}$ and $F_{out}$ are the outputs of coarse and fine TDCs. So the resolution ratio $K_{res}$ needs to be calculated before TDC start working. When ADPLL starts to work, only the integer phase error is significant and the TDC does not need to work [4]. Therefore the TDC can be in calibration mode at this stage, as shown in Fig. 6. In this mode the Cal of CTDC in Fig. 2 is set to 0. The input of TDC is only Start and the time error of $Sa$ and $So(14)$ is CTDC’s resolution. The two OR gates’ outputs StartF and StopF keep the timing relation of $Sa$ and $So(14)$ and therefore a buffer’s time residue is quantized by FTDC. The number of high levels in the FTDC output is the ratio $K_{res}$. In order to violate PVT variations, the ratio $K_{res}$ needs to be calibrated multiple times to get the average value. After resolution normalization, Cal is set to 1 and TDC enters working mode. In fact, TDC always has enough time for calibration every time ADPLL performs frequency switching [2].

### 4. Experiment results and discussions

The proposed TDC is implemented in 180 nm CMOS process and its post-layout is simulated by SPICE. The TDC transfer curve is shown in Fig. 7 and it is almost a straight line. The average resolution is 6.2 ps and the dynamic range of the TDC is designed to be 1400 ps. Fig. 7 also shows a partial enlarged view of the TDC transfer curve. It can be seen that this curve is stepped and the width of the step is the resolution of TDC, which is also called the quantization error.

To further investigate the linearity of TDC, Monte-Carlo post-layout simulated DNL and INL with three different process variations (Fast Fast, Typical Typical and Slow Slow) are shown in Fig. 8. Thanks to TDC’s delay-line structure, DNL is less than 0.9 LSB and INL is less than 0.8 LSB. Since the worst INL value is less than 1 LSB, there will be no error code in outputs. The sawtooth shape of INL curve is an inherent problem with VDL-TDC using single port SAFF. According to the simulation analysis, the reason is that the input load capacitance of SAFF’s StartF port in Fig. 5 is not a constant value. The gate capacitance of NMOS M1 is affected by the amount of drain and source charges. There are different timing relationships between StartF and StopF ports of 16 SAFFs in the whole FTDC, resulting in different charging times of drain and source of NMOS M1, and finally different input loads of 16 SAFFs. This causes the variations of FTDC’s resolution and degrades the linearity of FTDC. The linearity of FTDC can be improved by careful layout or adding relay devices between SAFF input and delay chain. Also, the trends of DNL and INL curves are almost horizontal, which proves that the delay-line structure CTDC has good linearity. Fig. 9 shows 1K-Monte-Carlo simulation with two constant inputs at both ends of the TDC range. Standard deviation (STD) of the output codes is less than 1 LSB at small phase error and is a little more than one LSB when input is large.

Post-layout simulation shows the TDC consumes only 520 $\mu$W at 25 MHz conversion rate. The TDC performance is summarized in Table I [31], together with those of the other works. Because the performance of TDC is related to dynamic range, power consumption, INL, and conversion...
rate, many TDC papers adopt a FoM that includes all the above indicators [7, 19, 20]. In this paper the FoM is also adopted. Owing to the low power consumption, good linearity and large dynamic range, the proposed TDC shows the best figure-of-merit (FoM) compared with other state-of-the-art TDCs.

5. Conclusion

By using SR-based arbiters and signal tracking mechanism, the power consumption of CTDC and the required stages of FTDC are reduced. FTDC also employs Vernier delay-line to obtain fine resolution. As CTDC and FTDC both adopt linear delay-line structure, good linearity is acquired. Coarse-Fine Interface uses dynamic logic OR gates instead of TA, which also contributes to good linearity. The proposed TDC has a built-in calibration mechanism to violate PVT variations. Implemented in 180 nm CMOS process, the TDC achieves 6.2 ps resolution and 8 bits. It consumes only 520 μW and achieves the best FoM compared with other state-of-the-art TDCs. What’s more, the TDC has good portability, and its range and resolution can be easily adjusted to match other target ADPLLs.

Fig. 9 Monte-Carlo simulation of single-shot code distribution. (a) At 19. (b) At 217.

| Table I Performance summary and comparison. |
|--------------------------------------------|
| Reference | JSSC | [19] | [20] | [21] | [31] |
| Architecture | TA-DC | TA-DC | TA-DC | TA-DC | TA-DC |
| Tech. (nm) | Sim | Sim | Sim | Sim | Sim |
| Resol. [ps] | 0.9 | 5.3 | 2 | 9.4 | 30 | 6.2 |
| Conversion Rate (MSS) | 50 | 30 | 1.3 | 251 | 29.4 | 25 |
| Bits | 4 | 8 | 16 | 8.94 | 10 | 8 |
| N fuera [log] | 5.68 | 6.07 | 2.38 | 7.86 | 8.24 | 2.152 |
| DNL [LSB] | 0.2 | 0.9 | 1.5 | 0.57 | 1 | 0.9 |
| INL [LSB] | 0.25 | 2.8 | 4.2 | 1.1 | 2.38 | 0.8 |
| Power [mW] | 0.2 | 1.1 | 18 | 24.2 | 2.769 | 0.52 |
| FoM** | 0.31 | 0.54 | 0.43 | 0.48 | 0.31 | 0.15 |

**Fixed** = Fixed

* N fuera = N fuera + log(INL+1)
* FoM = Power/(2.355 + Fs)[ps/conv-step]

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