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Cite as: APL Mater. 7, 071113 (2019); https://doi.org/10.1063/1.5097317
Submitted: 25 March 2019 . Accepted: 23 June 2019 . Published Online: 26 July 2019

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Note: This paper is part of the special topic on Emerging Materials in Neuromorphic Computing.

ABSTRACT

Analog synaptic weight modulation that is linear, symmetric, and exhibits long-term stability is demonstrated by the resistance changes in a Pt/indium-tin-oxide (ITO)/CeO$_2$/Pt memristor. Distinct from a Pt/CeO$_2$/Pt memristor without the ITO layer, which shows highly nonlinear and asymmetric resistance changes, the Pt/ITO/CeO$_2$/Pt memristor exhibits linear and symmetric resistance changes in proportion to the number of voltage applications with opposite polarities for potentiation and depression behaviors. The Pt/CeO$_2$/Pt memristor also displays high long-term stability of modulated synaptic weight over time, which originates from the ITO layer acting as a reservoir of oxygen ions drifted from the CeO$_2$ layer to retain the resistance change. Comparison of the results for the Pt/CeO$_2$/Pt and Pt/ITO/CeO$_2$/Pt memristors confirms the role of ITO in the linearity, symmetry, and long-term stability of the resistance change in CeO$_2$-based memristors for use as artificial synapses in neuromorphic systems.

Artificial synapses in brain-inspired neuromorphic systems perform signal processing and consequently update their synaptic weight to achieve adaptive learning and memory operations. Among the various synaptic devices developed for use in artificial synapses to date, memristors with two-terminal metal/resistive-switching-layer/metal structures, which are analogous to presynaptic-neuron/synapse/postsynaptic-neuron in biological systems, have been actively investigated. Analog resistive switching memristors are particularly desirable to emulate the analog tuning of synaptic weight in biological synapses. Analog switching has been achieved using various switching materials such as HfO$_2$, SiN$_x$, IGZO/HfO$_2$, TiO$_2$/TiO$_2$, TaO$_x$, TaO$_x$/TaO$_y$, TaO$_x$/SiO$_2$, MnO/TaO$_2$, and SrTiO$_3$/reduced-graphene-oxide. Besides analog behavior, linearity of the resistance change, representing the identical incremental tuning of synaptic weight with the repetition of input pulses, is requisite for fast learning with simple neuron circuit operation by determining the synaptic weight change using only the pulse repetition number. The symmetric tuning of synaptic weight for synaptic potentiation and depression is also preferred because it allows the neuron circuit to generate voltage pulses with the same amplitude but opposite polarities for potentiation and depression. In addition, analog resistance changes need to display long-term stability to guarantee stable signal processing, adaptive learning, and memory functions. All of these characteristics should be obtained under the conditions of low power and low energy consumption.

In this study, we demonstrate the synaptic behavior of a Pt/indium-tin-oxide (ITO)/CeO$_2$/Pt memristor, in which the ITO layer plays a decisive role in regulating synaptic behavior. We previously reported the strong analog resistance change emulating potentiation and depression motions in a Pt/CeO$_2$/Pt memristor without an ITO layer. The CeO$_2$ layer has high oxygen ion conductivity, variable valence states of Ce cations (Ce$^{3+}$ and Ce$^{4+}$), and compatibility with current microelectronics as a potential high-k gate dielectric layer and switching element for resistive random access memory (RRAM) because of its high relative...
permittivity (~26) and wide bandgap (~6 eV). However, the displayed potentiation and depression motions of the Pt/CeO$_2$/Pt memristor were nonlinear and asymmetric despite its symmetric structure. In addition, similar to other analog switching devices that operate mostly by a non-filamentary route, the device suffered from memory loss, which limits the stability of its analog or multilevel synaptic weight tuning. In the current study, a CeO$_2$-based memristor with an inserted ITO electrode is investigated because the ITO layer acts as an oxygen-reactive electrode whose conductivity increases with the concentration of oxygen vacancies. Therefore, oxygen ions are expected to be exchanged between the CeO$_2$ and ITO layers in the Pt/ITO/CeO$_2$/Pt memristor, thereby stably modulating the resistance. The presented synaptic characteristics demonstrate the improved linearity and symmetry of potentiation and depression as well as the long-term stability, which make the proposed Pt/ITO/CeO$_2$/Pt memristor a potential candidate for artificial synapses in neuromorphic systems.

The Pt/ITO/CeO$_2$/Pt memristor was fabricated as follows. A 60 nm-thick CeO$_2$ layer was deposited on a Pt bottom electrode on a Ti/SiO$_2$/Si substrate by radio-frequency (rf) magnetron sputtering with a CeO$_2$ target in an Ar environment and subsequently annealed at 400 °C for 1 h in an O$_2$ environment. The CeO$_2$ layer was previously confirmed to have a composition of O/Ce ~ 2 and consist of mostly Ce$^{4+}$ and lattice oxygen anions with small amounts of Ce$^{3+}$ and defective oxygen anions using Rutherford backscattering spectroscopy, energy-dispersive spectroscopy in transmission electron microscopy, and X-ray photoelectron spectroscopy. An ITO electrode with a thickness of ~60 nm was deposited on the CeO$_2$ layer by rf magnetron sputtering with an In$_2$O$_3$ target containing 10 wt. % SnO$_2$ at room temperature in an Ar environment. The ITO electrode had a diameter of ~100 μm, which was prepared using a shadow mask during the deposition process. A top Pt electrode was successively deposited by electron-beam evaporation. For comparison, a reference device with the structure of Pt/CeO$_2$/Pt was also prepared by following the same procedure except for the deposition of an ITO layer. Current-voltage (I-V) measurements using voltage sweeps and pulses were carried out using an Agilent 4156B semiconductor parameter analyzer with an Agilent 41501B pulse generator. The voltage was applied to the top Pt electrode and the bottom Pt electrode was kept grounded.

Figures 1(a) and 1(b) show the I-V sweep curves of the reference Pt/CeO$_2$/Pt and Pt/ITO/CeO$_2$/Pt devices, respectively. As illustrated in Fig. 1(a), the current of the reference device increased gradually during five repeated positive voltage sweeps of 0 → +5 V → 0 V and decreased reversibly under five successive negative voltage sweeps of 0 → −5 V → 0 V. Although the curves showed history-memorized memristive characteristics, the succeeding forward curve (0 → +5 V) was a little lower than the preceding reverse curve (+5 → 0 V) because of a retention loss. In addition, the current values and their changes at positive bias were orders of magnitude higher than those at negative bias. These results indicate that the resistance change is rather unstable over time and asymmetric with respect to the voltage polarity even though the Pt/CeO$_2$/Pt structure is symmetric. Asymmetric current in symmetric structures has been reported similarly for other systems such as Pt/(Ba,Sr)TiO$_3$/Pt$^{18}$ and Pt/SrTiO$_3$/Pt$^{19}$. This behavior has been attributed to different Schottky barrier heights between top and bottom interfaces depending on the processing conditions or an asymmetric internal field arising from fixed charges.

On the other hand, the $I$-$V$ curves of the Pt/ITO/CeO$_2$/Pt memristor in Fig. 1(b) showed that the current gradually increased. The succeeding forward curves followed the previous reverse curves during ten repeated positive voltage sweeps of 0 → +8 → 0 V. Repeating ten negative voltage sweeps of 0 → −4 → 0 V sequentially lowered the current. In addition, the current levels were more symmetric at both polarities than those of the reference device, which is beneficial for symmetric potentiation and depression. The symmetric current levels are thought to be derived from the lower work function of the ITO than that of the Pt bottom electrode, which nullifies the factor causing the higher current at positive bias in the reference device. It is also noted that both the current levels and their changes in the Pt/ITO/CeO$_2$/Pt device during repeated voltage sweeps were lower than those of the reference device, which is thought to originate from the increased electrode resistance induced by inserting the ITO layer.

Figure 2 shows the current changes of the reference Pt/CeO$_2$/Pt device during voltage pulse measurements that mimicked synaptic potentiation and depression behaviors. The procedures of applying potentiation pulses and conducting read operations were repeated 30 times for each potentiation condition. The repeated application of depression pulses and read operations were then conducted. The potentiation pulse amplitude was varied from +5 to +12 V with a fixed pulse width of 50 ms. The read operation was carried out at +2 V to minimize the read disturbance. The depression pulse amplitude ranged from −3 to −10 V. These pulse amplitudes and widths could be further decreased by optimizing the thickness of the CeO$_2$ layer. Similar to the voltage sweep results in Fig. 1, the repeated positive-bias potentiation pulses lowered the resistance, i.e., increased the read current, in an analog fashion. The current then decreased back reversibly upon applying repeated negative-bias depression pulses. The current change $\Delta I$ ranged from a few nanoamperes at low pulse amplitude, e.g., +5 and −3 V for potentiation and depression [Fig. 2(a)], to a few tens of microamperes at high amplitude [+12 and −10 V in Fig. 2(b)]. This wide dynamic range of potentiation and depression expands the adaptive learning/memory window of the device. Besides the range of $\Delta I$, the linearity of synaptic weight change with respect to the pulse repetition number $n$ was assessed with the parameter $\beta$ using the relation $\Delta I \propto n^\beta$, where $\beta = 1$ for completely linear proportionality. The $\beta$ was measured to be 0.46–0.68 during the potentiation at positive bias in Fig. 2, which is far from complete linearity. Furthermore, the linearity during the depression at negative bias was out of the measurable range, exhibiting an abrupt decrease of current during the first negative voltage pulse irrespective of the pulse amplitude. The resulting nonlinear and asymmetric potentiation and depression of the Pt/CeO$_2$/Pt device would be obstacles to fine adjustment of synaptic weight.

Figure 3 presents $\Delta I$ of the Pt/ITO/CeO$_2$/Pt memristor during pulse measurements. Inserting an ITO layer induced linear and symmetric $\Delta I$ during potentiation and depression, but decreased their magnitude compared with those of the reference device. Repeated positive bias application increased the current linearly with $\Delta I$ ranging from ~0.3 to 26 nA as the pulse amplitude was increased from +6 to +11 V. The current change was reliable during the repeated pulsing more than a 1000 times, ensuring the
FIG. 1. I-V curves of (a) Pt/CeO$_2$/Pt reference device during five repeated voltage sweeps of $0 \rightarrow +5 \rightarrow 0$ V and five successive sweeps of $0 \rightarrow -5 \rightarrow 0$ V and (b) Pt/ITO/CeO$_2$/Pt during ten repeated voltage sweeps of $0 \rightarrow +8 \rightarrow 0$ V and ten successive sweeps of $0 \rightarrow -4 \rightarrow 0$ V.

endurance for the repeated operations. The $\beta$ during potentia-
tion of the Pt/ITO/CeO$_2$/Pt memristor at positive bias was in the
range of 0.56–0.67 at the lowest amplitude in Fig. 3(a), and it was
increased with the increase of amplitude, for example, to the range of
1.11–1.34 in Fig. 3(f). The $\beta$ during depression ranged from 0.44
to 0.57 from Figs. 3(b)–3(f), except at the lowest amplitude with
$\beta \sim 0.26–0.41$ in Fig. 3(a). It implies that the higher voltage operation
is more desirable for the linear synaptic weight modulation. These
results verify that the Pt/ITO/CeO$_2$/Pt memristor has more linear
potentiation and depression characteristics than those of the refer-
dence device. As well as the linearity of the Pt/ITO/CeO$_2$/Pt memrist-
itor, its $\Delta I$ were symmetric at both polarities during potentiation and
depression.

Although the linearity and symmetry of potentiation and
depression could be improved by inserting ITO layer, it did not
exhibit ideal linearity yet. Indeed, the synaptic weight range modula-
tion is determined by several factors such as the internal states of the
CeO$_2$ and ITO layers depending on their thicknesses, compositions,
microstructures as well as the interface state with the electrodes. In
addition, the conditions of pulse amplitude, width, repetition num-
ber, and the read voltage determine measured synaptic weight. In
this regard, the linearity and symmetric characteristics would be fur-
ther improved by optimizing these conditions with the benefit of
inserted ITO layer.

The operation with a relative high pulse amplitude and
long width to modulate synaptic weight was due to the use of
FIG. 2. Read current of the Pt/CeO$_2$/Pt reference device at a read voltage of +2 V upon consecutively repeating potentiation and depression pulse applications with amplitudes of (a) +5/−3 V, (b) +6/−4 V, (c) +7/−5 V, (d) +8/−6 V, (e) +9/−7 V, (f) +10/−8 V, (g) +11/−9 V, and (h) +12/−10 V.
thick CeO$_2$ layer of $\sim$60 nm. Since the synaptic weight modulation is induced by electric-field driven oxygen ion migration, the pulse amplitude and width could be further reduced in proportional to the decrease of CeO$_2$ layer thickness. However, the reduction of CeO$_2$ thickness should be carefully optimized because consequently increased electric-field would cause the abrupt change of resistance that degrades the linearity of potentiation and depression.

Biological synapses exhibit memory loss over time that depends on the input conditions, unlike typical nonvolatile memory that ensures long-term retention of memory states. The current decay over time after potentiation of the reference Pt/CeO$_2$/Pt and Pt/ITO/CeO$_2$/Pt devices are presented in Figs. 4(a) and 4(b), respectively. To compare the current decay at the same range, pulses with different amplitudes were applied to the reference Pt/CeO$_2$/Pt and Pt/ITO/CeO$_2$/Pt devices. For the reference device, voltage pulses

FIG. 3. Read current of Pt/ITO/CeO$_2$/Pt at a read voltage of +2 V upon consecutively repeating potentiation and depression pulse applications with amplitudes of (a) +6/−4 V, (b) +7/−5 V, (c) +8/−6 V, (d) +9/−7 V, (e) +10/−8 V, and (f) +11/−9 V.
The retention properties of the memristors were then examined by reading the current without further potentiation pulses. For the reference Pt/CeO$_2$/Pt device in Fig. 4(a), the current increased from 7.5 to 49 nA during repeated +9 V pulses and then decreased to 11 nA after a retention time of 1000 s. The Pt/ITO/CeO$_2$/Pt device achieved slightly higher retention; its current increased from 6.9 to 37 nA after potentiation and then decreased to 16 nA after 1000 s, as shown in Fig. 4(b). The retention properties of both devices are closely related to the mechanisms of resistance change, which are hard to unveil because the resistance changed instantaneously upon voltage application and then decayed over time. Even the conduction mode analysis was not sufficiently accurate to confirm the switching mechanism of the devices.

Nevertheless, the distinguishable results for the Pt/ITO/CeO$_2$/Pt device from those of the reference device provide plausible clues for their operation mechanism with regard to the presence of ITO. Because the reference Pt/CeO$_2$/Pt device does not have an oxygen-reactive electrode such as an ITO layer, the electrical charging or internal redistribution of oxygen ions or vacancies in the CeO$_2$ layer would induce the resistance change. In contrast, the Pt/ITO/CeO$_2$/Pt device with an oxygen-reactive ITO layer has an additional route to change the resistance alongside the electrical charging or internal redistribution of oxygen ions. The ITO layer in the Pt/ITO/CeO$_2$/Pt memristor contains oxygen vacancies that are able to store oxygen ions that come from the CeO$_2$ layer upon applying a voltage.\textsuperscript{22} In our previous study of an ITO/CeO$_2$/Si capacitor, the resistance of the ITO layer was found to increase upon applying a positive bias to ITO because of the decrease of oxygen vacancy concentration caused by combination with oxygen ions migrating from the CeO$_2$ layer.\textsuperscript{22} Similarly, the oxygen ion migration into the ITO layer of the Pt/ITO/CeO$_2$/Pt device upon positive bias application modifies the oxygen-vacancy trap sites, Ce cation valence state, and interface state density in the CeO$_2$ layer, consequently leading to the resistance change. Because the resistance change in the Pt/ITO/CeO$_2$/Pt device involves the redistribution of oxygen ions between the ITO and CeO$_2$ layers, this device displays better retention properties than those of the reference device. However, it still exhibits the decay particularly at the initial stage. Based on the plausible mechanism of resistance change involving oxygen ion redistribution, the retention is thought to be determined by how stable oxygen ions are stored in the ITO layer. It indicates that the decay would be retarded by proper engineering of the ITO layer such as increasing oxygen vacancy concentration in the ITO to reserve oxygen ions.

The retention properties of the Pt/ITO/CeO$_2$/Pt device improved with increasing pulse repetition number $n$ as shown in Figs. 5(a) and 5(b). For example, the current increased with $\Delta I(0)$ of $\sim$140 nA upon repeating pulses 3000 times and then decayed to $\Delta I(t) \sim$50 nA after 500 s. In contrast, $\Delta I(0)$ was $\sim$3.3 nA upon repeating pulses 100 times and $\Delta I(t) \sim$0.8 nA after 500 s. The fast decay at small $n$ coincides with short-term memory (STM) characteristics. The improved retention with increasing $n$ corresponds to long-term memory (LTM), mimicking the characteristics of the transition from STM to LTM that realizes various memory hierarchy levels in the human brain.\textsuperscript{24} As depicted in Fig. 5(b) in the linear scale, the more repetition of pulses causing the larger $\Delta I$ also led to the faster decay at the initial stage although the remaining window was the large. Then, it narrowed the difference between the current levels with
changes induced by repeated the voltage application. In contrast, the Pt/ITO/CeO$_2$ reversible, and symmetric potentiation and depression were demonstrated in a Pt/ITO/CeO$_2$/Pt memristor through the resistance change. These results for the Pt/ITO/CeO$_2$/Pt memristor reveal a potential strategy to engineer synaptic characteristics such as linearity, symmetry, and long-term stability of synaptic weight modulation by using a proper combination of materials for the switching element and electrode.

In summary, synaptic characteristics with analog, linear, reversible, and symmetric potentiation and depression were demonstrated in a Pt/ITO/CeO$_2$/Pt memristor through the resistance changes induced by repeated the voltage application. In contrast, the Pt/ CeO$_2$/Pt reference device without an ITO layer showed nonlinear and asymmetric behaviors. The retention and PPF properties of the Pt/ITO/CeO$_2$/Pt device were superior to those of the reference one because the ITO layer acted as a reservoir for oxygen ions migrating from the CeO$_2$ layer under the applied voltage, which stabilized the consequent resistance change. These results for the Pt/ITO/CeO$_2$/Pt memristor reveal a potential strategy to engineer synaptic characteristics such as linearity, symmetry, and long-term stability of synaptic weight modulation by using a proper combination of materials for the switching element and electrode.

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (Grant No. NRF-2017R1D1A1B03029093).

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