High-κ field-effect transistor with copper-phthalocyanine

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Abstract
The use of SrTiO3 dielectrics as high-permittivity insulator in organic thin-film field-effect transistors (FET) is evaluated. FETs with sputtered SrTiO3 and copper-phthalocyanine (CuPc) as semiconducting layer were fabricated. The device preparation was performed in situ in an ultra-high-vacuum chamber system. The dielectric in the transistors had a permittivity of up to 200 which led to low driving voltages of 3 V. The FETs were p-type and reached mobilities of about $\mu = 1.5 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and an on/off ratio of $10^3$. These properties are compared to devices based on other dielectric materials.

(Some figures in this article are in colour only in the electronic version)

1. Introduction
Over the past 15 years remarkable progress has been made in the development of thin-film transistors (TFTs) based on organic semiconductors. In several key figures of merit, such as e.g. the on-to-off current ratio, the field-effect mobility, and the threshold voltage, the best organic TFTs can now compete with commercial amorphous silicon TFTs. The gate dielectric plays a crucial role in this regard. It is responsible for the reliability of the device, governs the required driving voltages and also limits the polarizations which can be achieved at the interface. In organic TFTs the most common dielectric is SiO2. It is well known and characterized from its use in the conventional semiconductor industry, and has the advantages of chemical stability and excellent insulation with low leakage currents. The required silicon wavers with an oxide dielectric layer are commercially available and the source and drain electrodes can be easily fabricated by lithography or by deposition through a shadow mask. Various groups have in this way prepared transistors with different organic layers such as pentacene or copper-phthalocyanine [1, 2]. This approach allows for concentrating on the growth of the active organic layers, but limits the experiments to the regime of low charge carrier concentrations.

Many organic materials show electronic interactions which are strongly influenced by the charge carrier concentration. Examples are charge transfer salts based on organic molecules such as tetrathiofulvalene-tetracyanoquinodimethane (TTF)-(TCNQ) [3–5] or K$^+\text{TCNQ}^-$ [6] which show the behaviour of a Peierls or Mott insulator [7]. Large changes in the charge carrier concentration may even induce a Mott metal–insulator transition, allowing for a so called Mott transition field-effect transistor (MTFET) [6, 8]. It is therefore interesting to grow these materials in transistor structures where high polarizations can be reached. But also for other organic semiconductors, where no Mott metal–insulator transition occurs, the utilization of high-κ dielectrics is interesting, because the high polarizations result in transistors with low driving voltages.

The charge carrier concentration at the insulator surface which can be induced in field-effect experiments is the product of breakdown field and dielectric constant evaluated at the breakdown field [9]. It therefore depends on the intrinsic properties of the material. With SiO2 as dielectric, a breakdown field of $E_{BD} = 10 \text{ MV cm}^{-1}$ and polarizations of up to $3 \mu \text{C cm}^{-2}$ are possible at best, while with complex oxide dielectrics with a perovskite structure polarizations in the range from 10–40 $\mu \text{C cm}^{-2}$ can be achieved under carefully optimized conditions [10].

2. Materials
From the perovskite class SrTiO3 is one of the best characterized materials. It has a cubic crystal structure with a lattice constant of $a = 3.905 \text{ Å}$ and the advantage of a high dielectric constant of $\varepsilon_r = 300$ for bulk material at room temperature. Thin films of SrTiO3 have been grown with...
For the growth of the SrTiO$_3$ layers RF sputtering was used. The dielectric constant and breakdown voltage in thin-film samples is in general lower than in bulk samples most likely due to defects and inhomogeneities of the electric field caused by surface roughness [11]. Furthermore, SrTiO$_3$ can be doped with niobium, which results in a conductive crystalline substrate material, ideally suited for the growth of an epitaxial dielectric SrTiO$_3$ layer [14].

In this work, to demonstrate the capability of SrTiO$_3$ as high-$\kappa$ dielectric for organic thin-film field-effect transistors (FETs), the well-known organic p-type semiconductor copper phthalocyanine was chosen as the active layer. CuPc (CuN$_8$C$_32$H$_{16}$) is a crystalline synthetic blue pigment from the group of phthalocyanine dyes. It has been used by various groups in field-effect experiments, usually with SiO$_2$ as the dielectric when deposited as thin films, but also already with high-permittivity insulators [1, 15].

### 3. Device preparation

An ultra-high-vacuum (UHV) system was employed for the preparation of the devices. It consisted of distinct chambers used for the individual process steps. The growth of the dielectric layer, active layer and the contact preparation was studied separately before they were combined to fabricate FETs completely in situ.

#### 3.1. SrTiO$_3$ sputtering

For the growth of the SrTiO$_3$ layers RF sputtering was used. The growth of sputtered SrTiO$_3$ was characterized with x-ray diffraction employing Cu-K$_\alpha$ radiation in parallel beam mode and optical microscopy and optimized with respect to high crystallinity, a smooth surface and a sufficient growth rate. The growth of sputtered SrTiO$_3$ was characterized with x-ray diffraction employing Cu-K$_\alpha$ radiation in parallel beam mode and optical microscopy and optimized with respect to high crystallinity, a smooth surface and a sufficient growth rate.

The sputtering target had a diameter of two inches and was at a distance of about 15 cm from the substrate.

For the final FET structure preparation SrTiO$_3$ layers had to be grown on Nb-doped SrTiO$_3$ (100) substrates. Since by x-ray diffraction thin-film and substrate related Bragg reflexions can in this case hardly be discriminated, the dielectric layer growth was optimized on MgO (100) substrates. The thus obtained sputtering parameters were then used for FET preparation on Nb-doped SrTiO$_3$ (100) employing an argon/oxygen mixture of 2:1 at a chamber pressure of 0.025 mbar, a substrate temperature of 720 °C and a forward sputter power of 100 W. The films were post annealed inside the chamber at 890 °C for 1 h in an oxygen atmosphere of 0.01 mbar. The deposition time was 90 min for FET preparation which resulted in a nominal thickness of about 450 nm. During the optimization on MgO, the SrTiO$_3$ films grew preferentially in the (100) direction. The Bragg peaks of the sputtered films were shifted to lower 2$\theta$ values as compared to bulk SrTiO$_3$. This was probably related to the larger lattice constant of MgO ($a = 4.216$ Å) compared to SrTiO$_3$ ($a = 3.905$ Å) which caused a tensile stress due to the misfit [16]. Post annealing further improved the crystalline quality of the SrTiO$_3$ films. This was demonstrated in situ in an oven at 800 °C for 24 h, so that the sample properties could be compared before and after annealing. The SrTiO$_3$ films showed an increase in the height of the Bragg peak and a shift in position in direction of bulk SrTiO$_3$, as is exemplarily shown in figure 1.

#### 3.2. CuPc growth

The organic semiconductor as active layer was prepared by organic molecular beam deposition in a UHV chamber with base pressure of 10$^{-10}$ mbar. The source material was commercial CuPc and it was used without further purification. The deposition rates were kept low, between 0.4 and 0.02 nm min$^{-1}$. CuPc growth was studied at different substrate temperatures on $\alpha$-Al$_2$O$_3$ (100) and SrTiO$_3$ (100). No difference in growth behaviour between these different substrates could be observed. In contrast to this the substrate temperature had a strong impact on the growth, as observed by x-ray diffraction. The temperature influence was studied in the range from room temperature to 140 °C. The films changed with increasing substrate temperature from smooth, with small angle oscillations and only a small Bragg peak to higher crystallinity, with a larger Bragg peak and a rougher surface with few or no small angle oscillations. A selection of Bragg scans is shown in figure 2 for films grown on $\alpha$-Al$_2$O$_3$ (100).

The Bragg peaks for all films and substrates were detected at an angle of $2\theta = 6.8^\circ$ which corresponds to a distance between molecular planes of 1.3 nm. The Bragg peak is in agreement with the (2 0 0) plane of the $\alpha$-phase of CuPc. The $\alpha$-phase is frequently reported for vacuum deposition of CuPc at moderate substrate temperatures [17], while the $\beta$-phase can be found at high substrate temperatures or deposition rates [18]. In the $\alpha$-phase the molecules are oriented close to edge-on with respect to the substrate. For the FETs prepared in this study an intermediate substrate temperature of 85 °C was chosen. This...
Figure 2. Small angle x-ray diffraction pattern of the CuPc thin films prepared in the OMBD chamber on α-Al₂O₃ substrates. The films were deposited on substrates at different temperatures. The film prepared at 50 °C showed pronounced Kiessig fringes but only a small Bragg peak. It was observed that this changed with higher substrate temperature—the Kiessig fringes disappeared in favour of Laue oscillations. The inset shows the corresponding rocking curves. The width (FWHM) of the rocking curve from film 009 was 0.038 Å. Deposition time was 2 h for all films. Effusion cell curves. The width (FWHM) of the rocking curve from film 009 was 0.038 Å. Deposition time was 2 h for all films. Effusion cell curves. The width (FWHM) of the rocking curve from film 009 was 0.038 Å. Deposition time was 2 h for all films. Effusion cell curves. The width (FWHM) of the rocking curve from film 009 was 0.038 Å. Deposition time was 2 h for all films. Effusion cell curves.

Figure 3. Schematic drawing of a top contact (a) and bottom contact (b) TFT with bottom gate geometry. The bottom gate is realized by a conducting substrate, here Nb-doped SrTiO₃, with the dielectric layer grown on top. With the use of shadow masks both top and bottom contact devices can be realized by altering the deposition order of contact and active layer deposition.

temperature was selected to balance the somewhat conflicting requirements of high crystallinity and layer smoothness.

FETs in thin-film geometry with CuPc as active layer and SrTiO₃ as dielectric were prepared in situ on (1 0 0) Nb-doped SrTiO₃ substrates in bottom gate geometry. The source and drain electrodes were made of a 30 nm gold layer by evaporation through shadow masks. Transistors were prepared in bottom contact (contact preparation before active layer) and top contact (contact preparation after active layer) geometry as sketched in figure 3. The channel length was 20 µm and the channel width was 1 mm. The shadow masks had a four-segment arrangement, so that there were always four (identical) transistors prepared, one in each sector of the substrate.

4. Results

When measured, the four FETs on one substrate showed comparable results. The dielectric layer was characterized at room temperature.

The capacitance was routinely measured with an LCR meter at a test frequency of 100 Hz. To further characterize the dielectric, the capacitance was also measured with frequencies up to 100 kHz. Up to 10 kHz the dielectric frequency response was almost constant with a loss of about 1%. At 100 kHz the measured capacitance dropped by about 5% as compared to the low frequency value. The dielectric constant of the dielectric layer was calculated from the capacitance of the electrodes. The values obtained for κ from the transistors with SrTiO₃ as the dielectric layer were typically around 180 to 200 and the dielectric could usually withstand voltages of about 3 V which corresponds to a breakdown voltage of about 700 kV cm⁻¹ and a polarization of 1.3 µC cm⁻². To calculate mobilities from the FET characteristics the capacitance per unit area was required, which was calculated from the measured capacitance and the area of the electrodes to about 413 nF cm⁻².

All CuPc transistors showed p-type semiconducting behaviour. For all transistors, only low voltages were necessary to achieve a pronounced modulation of the source drain current. The response characteristics of the transistors were measured multiple times with increasing voltages. The voltages were ramped up and down slowly and often a hysteresis was observed. The top contact transistors showed a better performance (i.e. higher mobility), possibly due to an annealing effect of the active layer during contact preparation, i.e. Au evaporation through a shadow mask. The response curve of a top contact FET is shown in figure 4. The transfer curves were measured for different fixed source drain voltages. The gate voltage was ramped up and down and also a hysteresis behaviour was observed. A hysteretic behaviour in organic FETs is not uncommon and usually related to trapped charges [19].

For positive gate voltages the conductivity was suppressed and the drain current decreased below the zero gate voltage current, which can be interpreted as a depletion behaviour. Saturation was hardly obtained for drain currents exceeding the gate voltage. This indicates a negative build in zero (threshold) voltage which biased the transistor. This FET had an on/off ratio of about 10³, which is comparable to literature results [15].

The mobility of the transistors can be obtained in different ways. From the current voltage curve the mobility can be calculated in the saturation regime by [20, 21]

$$\mu = \left( \frac{\partial I_D}{\partial V_G} \right)^2 \frac{2L}{CWI}. \quad (1)$$
where \( L \) is the channel length, \( W \) is the channel width, \( C_1 \) is the capacitance per unit area of the gate insulator, \( I_D \) is the drain current and \( V_G \) is the gate voltage. In the linear regime the mobility is obtained from the transfer curve by [20, 21]

\[
\mu = \frac{\partial I_D}{\partial V_G} \frac{L}{W C_1 V_D}
\]  

(2)

or from the slope of a plot, where the slopes of the response curves in the linear regime at constant gate voltage are plotted over gate voltage by [20, 21]

\[
\mu = \frac{\partial I_D}{\partial V_D} \frac{L}{W C_1 (V_G - V_T)}.
\]  

(3)

where \( V_D \) is the drain and \( V_T \) is the threshold voltage. The mobility obtained in the linear regime was derived from transfer curves to \( \mu = 1.8 \times 10^{-3} \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \). Additionally, the mobility was determined from the slopes of the response curves for small drain voltages. A plot of the derived slopes is presented in figure 5. From a fit to these values a mobility of \( \mu = 1.5 \times 10^{-3} \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \) and a threshold voltage of \( V_T = 0.27 \text{V} \) was calculated.

The mobility was also extracted from the saturation current as depicted in figure 6. The currents at \( V_D = -3 \text{V} \) were obtained from the response curves from figure 4. The square roots of these currents were then plotted over the gate voltage and from the slope the mobility was calculated to \( \mu = 1.1 \times 10^{-3} \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \) and the threshold voltage to \( V_T = 0.98 \text{V} \). The plot showed the typical increase in slope towards higher gate voltages [21].

5. Conclusions

In summary, FETs with SrTiO\(_3\) as dielectric and CuPc as semiconductor were prepared in situ. The values derived for the mobility in the linear and the saturation regime were in good agreement and amounted to \( \mu = 1.5 \times 10^{-3} \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \). These mobilities were obtained without optimization of the CuPc layer with respect to transport properties. In the literature the highest mobilities of about \( \mu = 1.5 \) to \( 2.0 \times 10^{-2} \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \) were reported for a substrate temperature of 125 °C by Bao et al [1] using a SiO\(_2\) dielectric and 150 °C by Okuda et al [15] using a SiO\(_2\) and a high-permittivity PbZr\(_{0.5}\)Ti\(_{0.5}\)O\(_3\) (PZT) insulator. Both groups report a dramatic field-effect mobility increase with substrate temperature, in conjunction with higher crystalline order. At even higher substrate temperatures, the field-effect mobilities decreased again, which was attributed to gaps between large non-space-filling crystals. Our field-effect mobility is well in agreement with the mobilities obtained by Bao et al on SiO\(_2\) at a substrate temperature of 85 °C. Further evidence that our lower mobilities can be attributed to the growth of the CuPc and not, for instance, to the roughness of the dielectric is the low SrTiO\(_3\).
surface roughness as evident from the large number of Kiessig fringes observed in the thickness measurements of the SrTiO\textsubscript{3} films (see figure 1). Furthermore, Okuda et al [15] reported very similar mobilities for devices prepared on SiO\textsubscript{2} and PZT although the PZT films had a 20 times larger surface roughness as compared to the SiO\textsubscript{2} layer. We therefore conclude that mobilities comparable to other substrates can be reached on SrTiO\textsubscript{3} by optimizing the growth of the CuPc layer. The on/off ratio in our devices (10\textsuperscript{3}) is comparable to the PZT devices, but lower than the best SiO\textsubscript{2} FETs (10\textsuperscript{5}). The driving voltages (3 V) are also comparable to the PZT devices (2 V) and much lower than the SiO\textsubscript{2} FETs (100 V). These results show that organic transistors with low driving voltages can be realized with a SrTiO\textsubscript{3} dielectric. Further optimization of the SrTiO\textsubscript{3} insulator is required to fully utilize its potential to achieve high polarizations and enable organic MTFETs, as well as basic research on the effects of large induced interface charges in organic charge transfer materials [22, 23].

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