Implementation of a new Bi-Directional Switch multilevel Inverter for the reduction of harmonics

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Abstract. In the current scenario, multilevel inverter plays a major role in heavy duty drive systems. MLI is one of the most advanced power converters for highly efficient AC output. But there is more to the requirement of number of control switches and total number of input sources which often generates more losses. This paper presents a new multilevel inverter design with limited number of control switches and with just one DC source to reduce these demerits. It uses a smaller number of Bi-directional switches. So that complexity of the circuit is reduced. Finally, an eleven-level inverter is designed and simulated using MATLAB/SIMULINK and THD reduction has been analyzed. This paper also provides a comparative statement of required components for various conventional methods.

1. Introduction

Staggered inverters are a truly appropriate setup to arrive at high power evaluations and excellent yield waveforms. In the group of staggered inverter, topologies dependent on arrangement associated H-spans are especially appealing a result of their measured quality and straight forwardness of control structure for the uncompromising electric drives would require electronic forced control inverters to meet the needs. Staggered converters do not cursively generate low mutilation voltages, but also minimize $dv/dt$-tension, thus reducing problems with electromagnetic compatibility. Shockingly, staggered converters have a few detrimentals. One inconvenience is the large number of semi-conductor switch requirement. The possibility of using low voltage control switches, each switch requires a driver circuit. This may make the general framework gradually very expensive and complex.

The Harmonics can be reduced by increasing the levels. It is compulsory that an output voltage with low THD is required, but greater the number of levels requires more elements; also the control will be very complex.

For eleven level yield voltages, five helper switches, four principle switches and five capacitors are required. To demonstrate the decrease in segment numbers accomplished by this rearranged H-connect staggered inverter arrangement, Table I present the quantity of part required to actualize an eleven level inverter utilizing disentangled H-connect staggered inverter and three recently characterized ones:

The two which were considered the usual staggered stages, the clipped diode and the tapped condenser, and another Fig. shows the block diagram of simplified H-bridge inverter: the symmetric course setup. The new topology accomplishes an around 40%.

The new arrangement decreases the quantity of diodes and capacitors, when contrasted and diode clamped setup. The new arrangement lessens the quantity of capacitors, when contrasted and the
capacitor clamped setup. Furthermore, since five capacitors are connected in parallel with the basic dc control supply, no critical condenser voltage swing is delivered during ordinary activity, keeping away from a problem that in some other staggered design can restrain working extent.

2. Block Diagram:
Circuit has single DC source with some number of split source capacitor with some number of bi-directional bridge structure. Each bridge is responsible for producing two levels, one from positive and the other from negative. Only one H-Bridge is connected, and this produces three level output (i.e.) one positive level, one negative level and one zero level. Gate driver circuit is used to trigger the switches.

Table 1: Components of Eleven level Inverter for various types of MLI

| S. no. | Types                         | Number of switches needed | Number of Diodes Needed | Number of Capacitors Needed |
|-------|-------------------------------|---------------------------|-------------------------|-----------------------------|
| 1     | Diode Clamped Type Inverter   | 20                        | 90                      | 10                          |
| 2     | Flying Capacitor Type Inverter| 20                        | -                       | 55                          |
| 3     | Cascaded H-Bridge Type Inverter| 20                        | -                       | -                           |
| 4     | Modified H-Bridge Type Inverter| 8                        | 16                      | 5                           |

Reduction of the quantity of simple circuit needed just eight operated power switches instead of twenty necessary in each of the other three arrangements. The helper switch voltage and current ratings are lower than the once required by the principle-controlled switches.

3. Circuit Diagram

The circuit diagram has five splitter Capacitors, these capacitors are used to divide the source voltage equally. In order to equal the voltage level, the value of all the capacitors should be same. Then there are four switches surrounded by 4 diodes each, these are responsible for producing two level output. And the H-bridge is used to produce three level output so that totally \(2+2+2+3=11\) levels can be achieved.
4. Modes of Operation

4.1. Zero Output Level
The two primary switches S2 and S4 are ON, short-circuiting the load. All remaining control switches turned down; the voltage at the load terminal becomes zero thus which produces circulating current.

4.2. Higher Output Level (Vdc/5)
The assistant adjustment S8 is closed, associating output +ve terminal, through diodes D13 and D16 also the adjustment switch S4 is going closed, interfacing the output Lower terminal point to ground. All remaining control switches are down; the potential at the output terminal is Vdc/5.
4.3. Higher Output Level (2Vdc/5)
The helper switch S7 is closed, connecting to the output +ve terminal point, through diodes D9 and D12, also S4 is closed, associating the lower terminal point to ground. Remaining control switches are Down, the potential at the terminal is 2Vdc/5.

4.4. Higher Output Level (3Vdc/5)
The helper switch S6 is closed, connecting to the output +ve terminal, through diodes D5 and D8, and S4 is closed, interfacing the lower terminal point to ground. All remaining control switches are down, the potential at stack terminal is 3Vdc/5.
4.5. Higher Output Level (4Vdc/5)
The assistant switch S5 is closed connecting to the output +ve terminal point, through diodes D1 and D4, also S4 is closed, associating the output lower terminal point to ground. All remaining control switches are down, the potential at stack terminal is 4Vdc/5.

4.6. Higher Output Level (5Vdc/5=Vdc)
S1 is closed, interfacing output +ve terminal point to Vdc and contact S4 is closed, associating the output lower terminal point to ground. All remaining control switches are down. The potential at stack terminal is Vdc.
4.7. Lower Output Level (-Vdc/5)
The assistant switch S5 is closed connecting to the output +ve terminal point through diodes D3 and D2, also S3 is closed, associating the output lower terminal. All remaining control switches are down, the potential at stack terminal is - Vdc/5.

4.8. Lower Output Level (-2Vdc/5)
The assistant switch S6 is closed connecting to the output +ve terminal, through diodes D7 and D6, also S3 is closed, associating the output lower terminal. All remaining control switches are down, the potential at stack terminal is - 2Vdc/5.
**4.9. Lower Output Level (-3Vdc/5)**

The helper switch S7 is getting closed connecting to the output +ve terminal, through diodes D11 and D10, also S3 is closed, interfacing the output lower terminal. All remaining control switches are down, the potential at stack terminal is -3Vdc/5.

**4.10. Lower Output Level (-4Vdc/5)**

The assistant switch S8 is closed connecting to the output +ve terminal, through diodes D15 and D14, also S3 is closed, associating the output lower terminal. All remaining control switches are down, the potential at stack terminal is -4Vdc/5.
4.11. Lower Output Level (-5Vdc/5=-Vdc)
S2 is Triggered, associating the output +ve terminal also S3 is closed, interfacing the load lower terminal. All remaining control switches are reduced, output potential at the output terminal is – Vdc.

5. Output voltage according to switch condition

| Volt | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 |
|------|----|----|----|----|----|----|----|----|

![Diagram](image-url)
| Vdc  | ON | OFF | OFF | ON | OFF | OFF | OFF | OFF |
|------|----|-----|-----|----|-----|-----|-----|-----|
| 4Vdc/5 | OFF | OFF | OFF | ON | ON | OFF | OFF | OFF |
| 3Vdc/5 | OFF | OFF | OFF | ON | OFF | ON | OFF | OFF |
| 2Vdc/5 | OFF | OFF | OFF | ON | OFF | OFF | ON | OFF |
| Vdc/5 | OFF | OFF | OFF | ON | OFF | OFF | OFF | ON |
| 0    | OFF | ON  | OFF | ON | OFF | OFF | OFF | OFF |
| -Vdc/5 | OFF | OFF | ON  | OFF | ON | OFF | OFF | OFF |
| -2Vdc/5 | OFF | OFF | ON  | OFF | OFF | ON  | OFF | OFF |
| -3Vdc/5 | OFF | OFF | ON  | OFF | OFF | OFF | ON  | OFF |
| -4Vdc/5 | OFF | OFF | ON  | OFF | OFF | OFF | OFF | ON |
| -Vdc  | OFF | ON  | ON  | OFF | OFF | OFF | OFF | OFF |

6. Simulation Result

![Simulation Output](image)

Figure 14. Simulation Output

7. Total Harmonic Distortion
Figure 15. Simulation results of Seven Level Inverter Total Harmonic Distortion

Figure 16. Simulation results of Eleven Level Inverter Total Harmonic Distortion

8. Conclusion

For huge electrical drives a staggered inverter with single dc source has been proposed. Reproduction and test results have shown that the switches are controlled by a control device at the critical recurrence; these converters have low yield voltage, low THD and high productivity.
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