Small-signal and noise GaAs pHEMT modeling for low noise amplifier design

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Abstract. Small-signal and noise GaAs pHEMT modeling techniques that include analytical extraction followed by optimization are demonstrated. The following measurement processing steps were carried out before the parameter extraction: de-embedding, data smoothing and selecting the bias mode appropriate for the extraction of parasitic resistances and inductances. A low-noise amplifier operating in 5G frequency band was designed using the resulting model. A comparison between simulation and measurements of noise factor and S-parameters of the obtained low-noise amplifier is presented.

1. Introduction
GaAs pHEMTs have been established as the most preferable semiconductor devices for microwave electronics design [1]. Over the years, many studies on characterization and modeling of GaAs pHEMTs have been developed. Primarily, a research interest in this topic is determined by evolution of a microwave semiconductor manufacturing technology and, consequently, by increasing the transistor performance. A successful circuit design is straighly related to the accuracy of models being utilized. For example, when designing a transceiver module, an engineer relies on several transistor characteristics such as scattering (S-) and noise parameters [2]. These data are used for designing low noise and buffer amplifiers which, in turn, determine an output performance of both receive and transmit path.

This study is focused on small-signal and noise GaAs pHEMT modeling in various bias points. The high-frequency transistor characterization consists in measuring S- and noise parameters which are further used for model parameter extraction and verification. S- and noise parameters were measured in the frequency range of 0.1–50 GHz and 1–50 GHz, respectively. An automated parameter extraction technique was applied in order to build small-signal GaAs pHEMT models in various bias points. Each small-signal equivalent circuit has been augmented with equivalent noise temperatures of the resistors to reproduce noise parameters. During the noise modeling a smoothing algorithm was applied to measured noise parameters data. The validity of the proposed modeling technique is confirmed by a good agreement between simulated and measured S- and noise parameters. On the basis of the obtained small-signal models a test monolithic integrated circuit (MIC) of a two-stage low-noise amplifier (LNA) for the frequency range of 17–24 GHz has been designed.
The remainder of this paper is structured as follows: section 2 presents a description of a transistor under test and the characterization setup, a short summary of the techniques for small-signal and noise model parameter extraction is given in section 3, section 4 reports on the results of small-signal and noise modeling, section 5 demonstrates the simulation results of the test two-stage LNA MIC for the frequency range of 17–24 GHz (minimum gain ratio $|S_{21}|$ 13 dB, minimum input and output reflection coefficients -18 dB, maximum noise figure 2.9 dB, single-supply operation 5V, current consumption 30 mA), and, finally, section 6 gives the discussion of the research results.

2. A description of a device under test and the characterization setup

The device under test is a GaAs pHEMT with a 4×40 um total gate width. $S$- and noise transistor parameters were measured at nine bias points ($V_{DS} = 2.5V; 3V; 4V, I_{DS} = 10mA; 15mA; 20mA$).

The characterization of the GaAs pHEMT transistor in terms of both $S$- and noise parameters was carried out using Keysight N5247A PNA-X Microwave Network Analyzer (0.01–67 GHz). Noise parameters were measured by means of the cold source method using an impedance tuner at the input of the device under test. The noise factor $NF$ was measured for at least four source impedances synthesized by the tuner.

3. Small-signal and noise model parameter extraction

A small-signal equivalent circuit of the investigated GaAs pHEMT (Figure 1) consists of eight bias independent extrinsic elements ($C_{pg}, C_{pd}, L_g, L_s, L_d, R_g, R_s$ and $R_d$), and eight bias dependent intrinsic elements ($C_{gs}, C_{gd}, C_{ds}, R_{gs}, R_{gd}, R_{ds}, g_m$ and $\tau$).

![Figure 1. GaAs pHEMT small-signal equivalent circuit](image)

At the previous stages of the study we have developed a technique which enables to obtain a reasonably accurate small-signal model of the transistor and also allows automation. The extrinsic elements of the equivalent circuit are calculated from the measured $S$-parameters under a cold-mode ($V_{DS} = 0 V$).

At the first step the measured $S$-parameters under a regime when the channel of a transistor is pinched off ($V_{GS} \ll V_{PO}$) are converted to $Y$-parameters. From the slope of the imaginary part of these parameters versus radian frequency $\omega$ extrinsic capacitances $C_{pg}$ and $C_{pd}$ are calculated. A low frequency range (less than 5 GHz) is preferable for this step because an equivalent circuit within this frequency range can be assumed as purely capacitive if an imaginary part of $Y$-parameters is considered [3]. Therefore, the extrinsic capacitances $C_{pg}$ and $C_{pd}$ are calculated by means of the linear regression algorithm. Parasitic inductances and resistances of a transistor are extracted using $Z$-parameters at zero gate voltage ($V_{GS} = 0 V$). The extraction procedure is based on the technique proposed in [4]. However, instead of averaging the calculated values of the parasitic resistances over a certain frequency range, in this study we also applied the linear regression. It was found that applying the linear regression one can eliminate the measurement errors and possible frequency dependence of a real part of $Z$-parameters which may
occur due to incomplete de-embedding of the extrinsic capacitances. The intrinsic elements of the equivalent circuit are calculated using the procedure, described in [5], from the Y-parameters at the certain bias point. It is worth noting that before calculating the intrinsic parameters one has to de-embed from this Y-parameters all the extrinsic elements, determined earlier. To automate the calculation of the intrinsic parameters the technique [5] has been enhanced with the procedure which selects the appropriate intrinsic values from the whole frequency dependence. The calculated intrinsic values are then used in the optimization step as an initial guess. Finally, the obtained models were verified by comparing the measured and simulated S-parameters.

The equivalent circuit parameter extraction technique described above has been implemented in the HEMT modeling wizard for commercial EDA Cadence AWR Design Environment [6]. The EDA has also been used to optimize the equivalent circuit parameters, compare the measured and modeled characteristics and also to design a test MMIC as will be shown in the following sections.

After the optimization of the small-signal equivalent circuit parameters, the noise models were obtained, adjusting equivalent noise temperatures of the resistors $R_{gs}$ and $R_{gd}$ [7]. A noise models were verified by comparing the measured and simulated 50 Ohm noise figure $NF_{50}$. Typically, the measured noise figure of a mismatched device has significant outliers. Therefore, we applied the moving-average algorithm which is commonly used in the field of signal processing in order to smooth the data of the noise figure measurement. The results of the data processing are presented in the following section.

4. The results of small-signal and noise modeling

The validity of the small-signal models is estimated by comparing the measured and simulated S-parameters at a certain bias point. For demonstration purposes such a comparison is presented for the measured and simulated data in one bias point (Figure 2). We also present the measured and processed data of 50 Ohm noise figure for this bias point as well as the results of simulation (Figure 3).

![Figure 2. Comparison between measured and simulated S-parameters at $V_{DS} = 3$ V, $I_{DS} = 10$ mA](image-url)
The analysis of comparison has shown that the maximum error in each bias point does not exceed 0.5 dB in magnitude and 7° in phase for the frequency range of 0.1–50 GHz. A good agreement between measured and simulated data confirms that the obtained models can be used for the low-noise amplifier design.

5. Design of the LNA MIC for the frequency range of 17–24 GHz

In order to further verify obtained small-signal and noise GaAs pHEMT model, a test two-stage LNA MIC has been designed. The basic requirements for the designed LNA are to provide a gain factor more than 12 dB and noise factor less than 3 dB, for the frequency range of 17–24 GHz. To implement these requirements, two stages are used with input, output and interstage matching network. The block-diagram of the designed LNA is shown below (Figure 4).

![Block-diagram of the designed LNA](image)

**Figure 4.** The block-diagram of the designed LNA

The matching circuit includes correcting networks, a bias-tee and a self-bias network, shown in more detail on the circuit schematic of the microwave low-noise amplifier (Figure 5).

A pHEMT with a 4×40 um total gate width is used as an active element of each amplifier stage (*see section 2*). Under a typical operation mode, the first stage of the LNA consumes 10 mA, the second stage – 20 mA. A comparison between simulated and measured microwave characteristics of the test MMIC is shown on Figure 6.
As we can see on Figure 6, obtained gain factor and noise factor have a good agreement on the given frequency range. A gain factor $|S_{21}|$ is $13.8 \pm 1.2$ dB, noise factor is less than 3.2 dB, which differs from the simulation results by 0.3 dB. The presented results correspond to the given requirements and the validity of the model.

6. Discussion of the research results

The results of the small-signal and noise modeling of a 4×40 um GaAs pHEMT in multiple bias points are demonstrated. Parameters of the small-signal equivalent circuit have been extracted by means of a new automated extraction technique. A comparison of the measured and simulated S-parameters confirms the validity of the obtained models: maximum error in each bias point does not exceed 0.5 dB in magnitude and $7^\circ$ in phase for the frequency range of 0.1–50 GHz. During the noise modeling procedure, a moving average-based algorithm was applied in order to smooth measured noise figure data. It was found that the measured data preprocessing enables to increase the accuracy of the resulting noise models. On the basis of the obtained small-signal models a test two-stage LNA MMIC for the frequency range of 17–24 GHz (minimum gain ratio $|S_{21}|$ 12.6 dB, maximum noise figure 3.2 dB, single-supply operation 5 V, current consumption 30 mA) has been designed. Obtained characteristics from test MMIC satisfy the requirements that indicates the validity of the developed model.
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