A wideband quasi-asymmetric Doherty power amplifier with a two-section matching-phase difference compensator network design using GaAs technology

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Abstract
In this paper, a quasi-asymmetric Doherty power amplifier (PA) is designed without load modulation using the GaAs 0.25 μm pHEMT technology to reach an enlarged output power back-off (OPBO) with circuitry solutions in order to overcome technology restrictions. To prevent power leakage in auxiliary PA (PA aux) due to its extremely low off-state impedance (Z off), a Wilkinson power combiner is added to the output. Moreover, an input asymmetric power divider is designed to guarantee that no considerable power is delivered to the main PA (PA main) in the high-power region to make it saturated. A two-section matching network is proposed for PA main, which simultaneously compensates for phase differences of the main and auxiliary amplification paths. To control the significant impedance variation of PA aux versus sweeping power and the different impedance trajectories of the main and auxiliary amplification paths, the bias and dimension selection of PA aux are analyzed to reach the desired output power profile versus input power. These methods overcome impedance variations and linearity degradation. To achieve the aimed 10% fractional bandwidth, appropriate low-quality LC-networks are selected as matching networks. The simulation results indicate the utility of the proposed structure for microwave link applications. Continuous-wave simulations imply that the proposed PA has a 33 dBm maximum output power and a 13.5 dB power gain with less than 1 dB power gain compression in the desired frequency range (7.6–8.4 GHz). The drain efficiency of 30% at the highest input power, minimum of second and third harmonic powers of −140 dBm and −130 dBm, respectively, and OPBO of 7.5 dB are also obtained.

Keywords Asymmetric · Back-off · Doherty power amplifier · MMIC · PAPR · Wideband

1 Introduction
To overcome the issue of efficiency roll-off in basic PAs, a Doherty power amplifier (DPA) was introduced [1]. Due to the potency of DPA for performance optimization at output power as well as its bandwidth and efficiency scopes, numerous researches have been conducted on its various structures [2–14]. Many structural modifications in the scientific research trend of DPA design are done by changing the concept of the conventional DPA [12–25]. One such change leads to more contribution of PA aux to output power compared to PA main, and this DPA is called asymmetric DPA (ADPA) [2]. This PA provides an extended output power back-off and, consequently, the increased PA’s high-PAPR signal capability. One of the critical challenges in designing DPA is the realization of a proper load modulation in the high-power region. In the conventional DPA, this is done with a quarter wavelength transmission line (¼TL), which has an inherently narrowband behavior.

In fact, before the high-power region, PA aux is inactive, and also the transistor Z off is extremely small. This
impedance loading on the PA\textsubscript{main} output results in power leakage into PA\textsubscript{aux}. Due to very small off-state impedance in this technology, the absorption technique, which is a narrowband method, is not viable for the wideband approach. Therefore, it is mandatory to use a strategy for load modulation, by which an enlarged output power back-off like that of an asymmetric wideband ADPA is reached.

In this work, to realize a design without load modulation, the power divider is designed in a manner so that no considerable power is delivered by the main branch at a high-power level and the non-saturation status of PA\textsubscript{main} is guaranteed. At the output, a power combiner is used to increase the isolation of these paths, which contributes to preventing the power leakage. Meanwhile, the phase difference of the main and auxiliary amplification paths, which is conventionally compensated by adding a $\frac{1}{4}TL$ to the PA\textsubscript{aux} input, is for the first time, reimbursed in the presented output matching network of PA\textsubscript{main}. This network is designed to present the maximum possible wideband behavior. Moreover, for the sake of linear operation, appropriate allocation of different power gains, dimensions, and biases to both PA\textsubscript{main} and PA\textsubscript{aux}, which we call them sub-PAs hereafter, are also studied in this work.

2 Design considerations

2.1 The topology of the circuit

A transistor by default is an unstable element, and thus using a stabilizer network is mandatory [26]. One of the most famous stabilizer networks is a parallel RC circuit. To gain roll-off prevention at higher frequencies, the capacitor of that network should be as large as possible. However, a large capacitor for PA\textsubscript{aux} leads to an undesirable amplification and PA\textsubscript{aux} linearity disruption. Thus the assigned capacitor should have a relatively low capacitance, which leads to gain reduction. To make a compromise between gain reduction and linearity degradation, a two-stage amplifying topology is selected for the auxiliary path. To make both paths of amplification as similar as possible, PA\textsubscript{main} is also designed in a two-stage structure (see Fig. 1).

2.2 Transistor dimension assignment

To prevent the saturation of the following stages in a multi-stage structure, the first stages are designed with lower dimensions. At low-level $P_{\text{in}}$, the first stage of PA\textsubscript{main} should receive most of the power and amplify it. Since, in stabilizing an extremely short-dimension transistor, a large resistor is necessary, amplifying is not accomplished in a tolerable trend, even in the presence of a proper capacitor, and it will be acceptable only at high-level $P_{\text{in}}$. Accordingly, in this work, the smallest size transistor that can be stabilized by a rational resistor is selected ($4 \times 150 \mu m$).

From another scope, satisfying the unequal amount of main and auxiliary output powers can be done by setting proper dimensions of transistors according to their output power ratios (Eq. 1, [26]).

$$P_{\text{Back-off}} = -10 \cdot \log(1 + \delta^2)$$  \hspace{1cm} (1)

where $\delta$ is the size ratio of $P_{\text{aux}}/P_{\text{main}}$.

Before dimension allocation, for sub-PAs to satisfy Eq. 1, some technology-based restrictions should be addressed. The transistor in this technology has two challenging issues in wideband scope. The first issue is the inconvenient variation of the transistor $Z_{\text{out}}$ when $P_{\text{in}}$ sweeps, and the second issue is impedance variation with sweeping frequency.

Figure 2 indicates the output impedance trajectory of the second stage of PA\textsubscript{aux} versus $P_{\text{in}}$.

It is interpreted that the real part of this impedance has approximately 240% proportional variation, and Fig. 3 depicts that this sub-PA has different impedance trajectories in frequency and $P_{\text{in}}$ sweeps.

Moreover, Fig. 4 shows the large-signal load mapper simulation result and also indicates the variation of the second stage’s $Z_{\text{in,aux}}$ when its $Z_{\text{out,aux}}$ changes. In other words, the amount and phase of the second stage’s $Z_{\text{in,aux}}$ are highly sensitive to this variation. This sensitivity increases the probability of matching disturbance at the inter-stage part. By considering these technology-based issues, to facilitate the output power combining process, both amplifying paths should be as resembling as possible. For a better impedance variation control, dimensions of both second stages are selected similarly, and their biases are chosen as similar as possible. At first, it is necessary to find proper auxiliary second stage dimensions to provide the desired output power, although it correlates with the selection of the PA\textsubscript{aux} first stage dimension. That is to say, due to extreme impedance variations in the auxiliary amplification path, first, the size of the second stage sub-PA of PA\textsubscript{aux} will be chosen. Then the size of the first stage sub-PA of PA\textsubscript{aux} will be selected so that the more capable $Z_{\text{out,first stage}}$ trajectory can be presented with the $Z_{\text{in,second stage}}$ trajectory. In this regard, using source and load-pull simulations with swept input power and fulfilling them repeatedly for the PA operating frequency band shows that two parallel 8 $\times$ 150 $\mu$m transistors can present rational impedance variation in power and frequency sweep aspects. As a result, designing OMN is more realizable using a proper output power and phase trend. Given the design goal that more output power is expected from PA\textsubscript{aux}, even if it receives more input power, because of
intensive biasing, the similar dimensions of the second stages of PA main and PA aux imply that the first stage of PA aux will be considerably larger than the first stage of PA main.

Moreover, two stages of PA aux should have relatively similar dimensions to participate in the amplification process with close power gains, and the second stage is not assigned to completely perform power amplification. As shown in Fig. 5, by setting the size of the first stage of PA aux as approximately similar to that of its second stage, impedance variations are closer in the two stages in comparison to the situation where the first stage is taken as a low-size driver. However, when the first stage is designed as a low-size driver, the power profile is only reached when the two stages have negative impedances, which is not acceptable, and their high impedance difference results in

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Fig. 1 Schematic of the proposed Q-ADPA

Fig. 2 Second stage’s $Z_{out}$ variation in the auxiliary way versus sweeping input power. The real part is shown above

Fig. 3 Second stage’s $Z_{out}$ variation of auxiliary path versus sweeping power and frequency, which shows different trajectories

Fig. 4 Influence of large-signal $S_{11}$ variation on $Z_{out}$ variation
two completely different stages that barely match. Under these circumstances and by considering the PA aux’s swept input power and frequency source-pull results, two parallel 6 × 150 µm transistors are selected to operate as the first stage of PA aux.

As a graphical investigation, Fig. 6 shows the transistors’ size influence on the output power contours of the second stages of sub-PAs. The similarity of these stages leads to the further analogy of the contours. It means that variation of adjacent paths results in a more flexible combination of their output powers.

Figure 7 indicates the sb-PAs’ amplifying trends according to the described conditions. Based on the desired unequal amplifying trend of sub-PAs, the absorbed input power by the main path is extremely low in spite of its amplifying capacity, and at the high-level power, almost all the power is absorbed by the auxiliary path. For the linear operation insurance of quasi-ADPA, gain compression should be traced when the nonlinear component of this structure, i.e., PA aux, commences the amplification process. Figure 8 shows that gain compression is less than 1 dB, implying the linear amplifying of the proposed quasi-ADPA.

2.3 Analysis of auxiliary power amplifier (PA) biasing

According to the linearity concept, the linearity of the auxiliary path is more sensitive to the second stage. As a consequence, it should be as linear as possible. Therefore, the first stage of PA aux is biased more intensively. The
efficiency of PA based on the following three cases of biasing is scrutinized (the first case is selected).

Case 1: The first stage is biased more intensively.
Case 2: The two stages have the same biasing scheme.
Case 3: The second stage is biased more intensively.

Figure 9 shows that undesired harmonics suppression in the output power by utilizing the first case of biasing leads to more efficient performance.

2.4 Input power divider

To assure the non-saturation regime for \( P_{\text{main}} \), the \( Z_{\text{characteristic}} \) of the main branch of the power divider is matched to its \( Z_{\text{opt}} \) in low-level \( P_{\text{in}} \), and its auxiliary branch is matched to its \( Z_{\text{opt}} \) in high-level \( P_{\text{in}} \). Therefore, when power increases, a high mismatch prevents \( P_{\text{main}} \) from receiving a considerable degree of power, and thus it will not become saturated according to [27]. However, this divider has two main challenges. The first challenge is a considerable difference in the \( Z_{\text{in}} \) of the two sub-PAs, and the second challenge is their significant variations in different impedance trajectories when receiving variable power. Both challenges lead to high inequality in the power divider elements, which imposes a considerable phase difference to both amplification paths. In this regard, phase equalization at the output will be complicated (discussed in Sect. 2.7).

Moreover, the selection of 50 \( \Omega \) for the \( Z_{\text{characteristic}} \) of the power divider branches will result in extremely low capacitances in the lumped-element model of the TLs of the power divider, introducing significant parasitical effects. To avoid using these small capacitors, \( Z_{\text{characteristic}} \) is set to 25 \( \Omega \), and the least capacitances with ignorable undesired effects (in this case, 110 \( \mu F \)) are set; then, other elements are attained corresponding to them. A low-pass filter is used for 25 \( \Omega \) to 50 \( \Omega \) matching at the input.

To avoid intolerably variation of auxiliary sub-PA power gain in presence of the large capacitor as a DC blocks, a resonance LC-network is placed to reduce its destructive effect. To have more similarity in both amplification paths, the same LC-network is used for the main path (see Fig. 10).

The power splitting of the described power divider is shown in Fig. 11. Figure 12 indicates the first stages of the proposed quasi-ADPA.

2.5 Inter-stage matching networks

To deliver the maximum \( P_{\text{out}} \) of the first stage to the second stage, the optimal output impedance (\( Z_{\text{out,opt}} \)) of the first stage should be matched to the optimal input impedance (\( Z_{\text{in,opt}} \)) of the second stage, which are both elicited from load/source-pull results, respectively by reasonably low-quality LC-networks. To avoid unrealizable elements (very large or very small capacitor or inductor) of matching the complex number of \( Z_{\text{out,opt}} \) to the \( Z_{\text{in,opt}} \), which is also a complex number, each of these numbers, which are extracted from source/load pull simulations, are matched to a same real impedance. This impedance is selected to be 50\( \Omega \). These matching networks are depicted in Fig. 13.

2.6 The compensating phase and matching network selection

In this design, due to power leakage in the low-power region, for combining the maximum power, two conditions should be satisfied as follows:
1. Adequate isolation of terminals of both amplifying paths to avoid power leakage  
2. Acceptable wideband performance

By considering the trajectory of $Z_{\text{out,aux}}$, the $\lambda/4$ TL meets none of them. Therefore, it is imperative to use a wideband matching network by adding an extra block to satisfy adequate isolation (discussed in Sect. 2.8). To have an efficient structure, the delivered output powers of both amplification paths should be in-phase or at least have a tolerable phase inequality. Since here, its value is not as low as possible to be ignored (almost $120^\circ$), phase and impedance matching equations should be considered simultaneously. In other words, in this work, for the first time, the phase compensating and impedance matching

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**Fig. 10** Schematic of input power divider with DC blocks

**Fig. 11** Delivered power to main and auxiliary ways

**Fig. 12** Schematic of the first stages of both paths: **a** main way, **b** auxiliary way
networks are merged at the end of these two paths. There are three approaches to design the phase compensating network as follows:

Case 1: Merge in the OMN of the class AB
Case 2: Merge in the OMN of the class C
Case 3: Merge in the power combiner

The second case is not appropriate since it intensifies the inherent narrowband characteristic of the class C PA. In the third case, linear power combining has poor controllability on phase compensation, and merging these two networks will result in sacrificing the linearity. Thus in the first case, to make a trade-off between the increased wideband performance of this OMN and its decreased insertion loss, a two-section matching network is selected. The aimed value of the phase that should be compensated is split between them, which are modeled by two TLs with the parametric $Z_{\text{characteristic}}$ and electrical lengths. To this end, $Z_{\text{out,main}} = 10.6 + j 5.7$, should be matched to a 50 $\Omega$ resistor using a two-step impedance transfer function. To do so, 10.6 + j5.7 is first matched to a 25 $\Omega$ resistor and then to a 50 $\Omega$ resistor. After that, impedance matching formulas are written as an objective function. The desired phase compensation is considered as a constraint equation for the objective function. Finally, a constrained genetic algorithm is applied using MATLAB to obtain results. The outputs of the genetic algorithm are two characteristic impedances and two electrical lengths. Based on the transmission line theory, the following equations lead to finding the object function. For the first TL, we have:

$$10.6 + j 5.7 = Z_{o1} \frac{25 + j Z_{o1} \tan(\theta_1)}{Z_{o1} + j 25 \tan(\theta_1)}$$  \hspace{1cm} (2)

Then, for the second one, we have:

$$25 = Z_{o2} \frac{50 + j Z_{o2} \tan(\theta_2)}{Z_2 + j 50 \tan(\theta_2)}$$  \hspace{1cm} (3)

Therefore:

Object Function = $25Z_{o1} + j(Z_{o1}^2) \tan(\theta_1)$

$- (25Z_{o1} + j 625 \tan(\theta_1)) + 50Z_{o2}$

$+ j(Z_{o2}^2) \tan(\theta_2) - (50Z_{o1} + j 2500 \tan(\theta_2))$  \hspace{1cm} (4)

In the circuitry model of the transmission line, to achieve realizable elements (especially appropriate capacitors) in this technology, a low-pass filter is chosen with series inductors. Figures 14 and 15 indicate the schematics of this network and the output stages of both paths, respectively.

It should be noticed that although all of this design’s matching networks are designed to deliver power, these networks, as passive networks, also may provide passive gains. The voltage gain and insertion loss of them are reported in Table 1.

### 2.7 Output power combining

One of the appropriate structures to avoid power leakage due to low off-state impedance of PAaux is the inverted DPA structure [14]; however, this solution suffers from the narrowband behavior of the transmission line and using extremely large capacitors in its circuitry model, which are not appropriate for the MMIC design. Therefore, in this work, the output powers of the amplifying paths are combined by using a power combiner with the proper isolation.

![Fig. 14 Proposed OMN schematic (resistors are put to show the target impedance of each section)](image-url)
(−11 dB is needed) of its terminals. Because of the acceptable isolation and wideband behavior of the Wilkinson power combiner, an asymmetric Wilkinson combiner is chosen to combine the main and auxiliary output powers with a power ratio of about $0.53(\frac{P_{out,\text{main}}}{P_{out,\text{aux}}})$. This combiner is shown in Fig. 16. This ratio leads to a nuance in the phase of each power combiner terminal. Figure 17 shows that this difference is reasonably small, and thus there is no concern about unsatisfying power combining.

Table 1 Insertion loss and voltage gain of matching networks of this work

|                  | IMN of main’s first stage | IMN of main’s inter-stage | IMN of main’s output stage | IMN of Aux’s first stage | IMN of Aux’s inter-stage | IMN of Aux’s output stage |
|------------------|---------------------------|---------------------------|---------------------------|--------------------------|---------------------------|---------------------------|
| Insertion loss (dB) | −2.57                     | −4.8                      | −3.194                    | −4.1                     | −0.99                     | −2.5                      |
| Voltage gain (dB)  | −0.6                      | 2.8                       | −0.09                     | 0.17                     | −6.4                      | 10                        |

Fig. 15 Schematic of the second stages of both ways: a main path, b auxiliary path

Fig. 16 Output power combiner schematic terminations

Fig. 17 The phase of power combiners’
By using this approach, Fig. 18 depicts $Z_{out}$ trajectories of this design’s second stage sub-PAs at their drains. This figure indicates the very low impedance of $Z_{off,aux}$ that engenders power leakage in low-power region. Besides, in comparison by the concept of the conventional DPA, $Z_{out,aux}$ of this work, is also low in high-power level therefore, the conventional load modulation can not be used in this design.

S-parameters of this work’s MNs are depicted in Fig. 19, and Fig. 20 indicates power gains of each sub-PAs.

Figure 21 shows the proposed quasi-ADPA drain efficiency, output power, and power gain. Moreover, the drain efficiency of the proposed quasi-ADPA at different frequencies is indicated in Fig. 22.

2.8 The study of the high-order harmonics

In this work, power in the second and third harmonics is too low, so that the harmonic cancelation network design can be ignored. This issue is checked by imposing a continuous-wave-signal, which shows that almost no amplifying occurs at the second and third harmonics. As a result, the harmonic cancelation network design is skipped, as shown in Fig. 23.

2.9 Study of the stability of the whole circuit

To make a guarantee that the designed PA will be stable in both linear and nonlinear regimes, the relevant simulations of the proposed quasi-ADPA’s stability are provided in Fig. 24 that shows the stable performance of the PA.

3 Results

To design a PA with increased output power back-off, a quasi-ADPA using GaAs 0.25 μm pHEMT technology is designed. This PA presents maximum power gain of 13.5 dB, which leads to $P_{out,max}$ of 33 dBm, and drain
efficiency of 30%. The main path drains biases are 4 V and 5.5 V for its first and second stages, and the auxiliary path drains biases are 5 V and 7.25 V for its first and second stages, respectively. The dimensions of these sub-PAs are selected $4 \times 150 \mu m$, $8 \times 150 \mu m$, $6 \times 150 \mu m$ and $8 \times 150 \mu m$ for the first and second stages of the $PA_{main}$ and $PA_{aux}$, respectively, according to the best results of their swept input power source/load-pull simulations. To achieve proper circuitry elements with the lowest destructive influence on bandwidth and linearity, a two-section LC-matching network with sufficiently low quality is proposed to match and compensate for phase differences in both paths. To prevent output power leakage into the auxiliary path due to its low off-state impedance, a Wilkinson power combiner is used. As a result, the desired 10% fractional bandwidth is attained at the 7.6–8.4 GHz frequency range. The gain compression is less than 1 dB, which implies the linear operation of PA. The power study of the minimum second and third harmonics demonstrates that there is no significant power in these harmonics, $-140$ dBm and $-130$ dBm, respectively, and thus almost all the output power is in the desired signal. Figure 25 indicates the total layout of quasi-ADPA. The performance of the proposed quasi-ADPA is compared with the other recently reported MMIC ADPAs in Table 2.

4 Conclusion

In this work, for the first time, a quasi-ADPA was designed without load modulation. This PA was designed using the GaAs 0.25 μm pHEMT technology, which confronted serious technological bottlenecks. All efforts were based on a step by step circuit-level solution to investigate and overcome these limitations. The size and power delivery rates of transistors to each path were arranged to attain a 7.5 dB output power back-off. An asymmetric Wilkinson power divider was used in the input to deliver all power in low power to $PA_{main}$ and almost all power to $PA_{aux}$ in high-power region. Then, a multi-stage structure with the coarse to fine biasing of auxiliary PAs prevented linearity and
efficiency degradation due to the non-existence of large capacitors in the stabilizing network and also prevented the emergence of undesired harmonics. Finally, our proposed matching network, which was inserted at the end of the main amplifying path, simultaneously compensated for the phase difference of these paths.

Moreover, a Wilkinson power combiner blocked power leakage into the auxiliary amplifying path when it was inactive. By these strategies, the designed wideband quasi-ADPA was simulated. The result of EM simulations of the proposed quasi-ADPA showed the maximum output power of 33 dBm, drain efficiency of 30%, and power gain of 13.5 dB on the condition that power gain compression was less than 1 dB. As a result, the quasi-ADPA linear performance was insured. Further, the minimum second and third output power harmonics of −140 dBm and −130 dBm implied that no destructive harmonic was in the output power.

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**Table 2** Comparing the designed quasi-ADPA performance with other recent MMIC ADPAs

| Technology       | [9]a | [10]b | [11]c | This work   |
|------------------|------|-------|-------|-------------|
| Frequency (GHz)  | 0.2–1.5 | 25.8 | 24    | 7.6–8.4     |
| Peak power (dBm) | 25   | 25.1  | 32.78 | 33          |
| OPBO (dB)        | < 6  | < 1   | 6     | 7.5         |
| Peak drain efficiency (%) | 20 | > 16a | 35 | 30         |
| Power gain (dB)  | 30   | 7     | 11.5  | 13.5        |
| Consumed area (mm²) | N/A  | 2.25  | 8.88  | 5.35        |

a For power gain compression less than 3 dB
b Measured results, simulation ones are not reported

c It is estimated
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