Scalability of spin FPGA: A Reconfigurable Architecture based on spin MOSFET

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(Dated: January 19, 2013)

Scalability of Field Programmable Gate Array (FPGA) using spin MOSFET (spin FPGA) with magnetocurrent (MC) ratio in the range of 100% to 1000% is discussed for the first time. Area and speed of million-gate spin FPGA are numerically benchmarked with CMOS FPGA for 22nm, 32nm and 45nm technologies including 20% transistor size variation. We show that area is reduced and speed is increased in spin FPGA owing to the nonvolatile memory function of spin MOSFET.

PACS numbers:

INTRODUCTION

Spin metal-oxide-semiconductor field-effect transistor (spin MOSFET) is a novel MOSFET whose source and drain are contacted with ferromagnetic materials [1]. Ferromagnetic materials provide stable and robust nonvolatile memory [2]. Fig.1(a) shows a spin MOSFET in which the write process is carried out by using magnetic tunneling junction (MTJ) [3,4,1]. Spin MOSFET directly couples logic element with nonvolatile memory element, opening up a path to a new style of logic-in-memory architecture [5].

Field Programmable Gate Array (FPGA) has a great advantage in that a chip is completely programmable and reconfigurable. However, conventional FPGA includes a lot of static random access memory (SRAM), which is a volatile memory composed of six transistors and faces the fabrication limitation of Si MOSFET. Thus, new FPGA based on novel devices has been expected. Here, for the first time, we report on numerical benchmark for an island-style FPGA using 22nm, 32nm and 45nm spin MOSFETs (spin FPGA) [4] by improving standard benchmark tools [6]. Compared with other proposals [2,8], spin FPGA has an advantage in that it is based on Si transistor equipping stable nonvolatile magnetic memory. Moreover, SRAM (six transistors) can be replaced by one spin MOSFET. Many SRAMs are used in FPGA such as in Lookup tables (LUTs) and interconnect area of pass transistors. Therefore, this replacement reduces transistors and FPGA area. Because the speed of FPGA is governed by the length of wire part, smaller area of spin FPGA leads to faster performance. Monte Carlo simulation based on the Predictive Technology Model [9] is carried out to consider variation of device size assuming fabrication difficulties. Although experiments on MTJ [2] at present show the maximum magnetocurrent (MC) ratio is 260% (RA ≈ 100μm²), in this paper we treat 100% ≤ MC ratio ≤ 1000% assuming future realization of larger MC.

Spin MOSFET.—We model the spin MOSFET by changing SPICE parameter (mobility) such that MC defined by $MC = (I_P - I_{AP})/I_{AP}$ coincide with a given MC ratio (I_P and I_{AP} are parallel and antiparallel currents, respectively.) For I_P, we use the same SPICE parameters as those of the conventional MOSFET (Fig.1(b)). Although there is extra resistance owing to the existence of MTJ in spin MOSFET, as Ref.[10] reported, the resistance of 50 nm square MTJ can be controlled to less than 400Ω and this resistance is negligible compared to the resistance of conventional MOSFET of the order of 10 kΩ.

Spin Cluster Logic Block.—Fig. 2 shows our spin LUT structure [11] for 4-inputs and 1-output, which is a typical set of LUT parameters [6]. Transistor sizes of amplifiers are adjusted such that the input pulse signal is appropriately transferred to the output of LUT.

Pass transistor.—We propose a spin control pass transistor depicted in Fig. 3(a). SPICE simulations show that the speed of pass transistor in Fig. 3(a) is of the same order as that in Fig. 3(b) by adjusting the width of control transistors (total transistor area of Fig. 3(a) is four in unit of minimum transistor size). Although this pass transistor structure has a disadvantage, namely, a leak-
FPGA AREA REDUCTION BY SPIN MOSFET

First, let us compare the number of transistors in spin LUT and CMOS LUT. In ref. [11], we only counted the number of transistors of a spin LUT. Here, we estimate the number of transistors by a general clustered logic block (CLB) in which four CLBs are clustered with 10 inputs and 4 outputs. For K-input LUT, 2^K SRAM and 2^{K+1}−2 pass transistors (multiplexer trees) are required with three input buffers. Then the total number of transistors in a complementary MOS (CMOS) LUT N_{lut}^{(cmos)} is given by 2^{K+3}−2+6K. In a spin LUT (Fig.2), the leftmost SRAMs are replaced by spin MOSFETs with an additional write/erase transistor. In addition, a sense amplifier (five transistors), a reference transistor and two power supply transistors are required. Thus, the number of transistor required in the spin LUT is given by N_{lut}^{(spin)} = 3×2^K + 6(K+1). Thus, we have N_{lut}^{(cmos)}−N_{lut}^{(spin)} = 5×2^K−8. For example, 4-input LUT conventionally has 150 transistors whereas spin LUT includes 78 transistors (48% reduction).

Circuit area is calculated by the minimum-width transistor area model [6], in which each transistor area is estimated by a unit of minimum-width NMOS. When W_{min} and S_{min} are width and area of minimum NMOS, respectively, a width ZW_{min} transistor is estimated as having an area of (1+Z)S_{min}/2. Width of PMOS is determined such that an inverter changes at half of a drain voltage. For PMOSs of 22nm, 32nm and 45nm nodes,

\[ Z_{22nm}^{(pmos)} = 1.53, \quad Z_{32nm}^{(pmos)} = 2.22, \quad Z_{45nm}^{(pmos)} = 2.57 \quad (1) \]

(PMOS is scaled down more than NMOS because of advanced technologies such as strain effects.) Area of recent FPGA is mostly occupied by an interconnect or wiring part. Wire resistance and capacitance are calculated from Ref. [13].

BENCHMARK RESULTS AND DISCUSSION

Area and speed of spin FPGA over 20 typical million-gate circuits are benchmarked with modified VPR ver.5 [6] for 22nm, 32nm and 45nm transistors. We take standard parameters such as Fc = 3 (Wilton switch box), Fe\_in = 1.0 and Fe\_out = 0.25 with length 1 wire segment [6]. Fig.2 show the average results over 200 Monte Carlo simulations for up to 20% (3 sigma) variations of length and width in 22 nm transistors, where the vertical axes show advantage of area, critical path delay and area-delay product defined by (\Theta^{(cmos)}−\Theta^{(spin)})/\Theta^{(spin)} for \Theta = \{A\ (area), t_{delay} \ (critical\ path\ delay), A \times t_{delay}\ (area-delay\ product)\}. Area-delay product is treated as a metric of FPGA performance. Fig.1 and Table I show that area of spin FPGA is greatly reduced compared with CMOS FPGA. For 22 nm transistor, an average of 16% area reduction is realized. This area reduction leads to small critical path delay of circuits resulting in faster operation in spin FPGA. In Fig.3 speed is improved by an average of 24%. As MC ratio increases, P/AP signals that go into an amplifier in spin LUT (Fig.2) become clearer. This leads to more robust operation against the variation of transistors, resulting in shorter delay in Fig.5. Thus, area-delay product is improved on average by 43%. Fig.7 shows summarized results of benchmark from 22 nm to 45 nm transistors. As mentioned above, as transistor scale decreases, ratio of PMOS area to NMOS area decreases. This means that the effect of area reduction by spin MOSFET (NMOS) becomes larger resulting in better performance of small transistor nodes.

One of the advantages of spin MOSFET compared with CMOS with interlayer MRAM system is that, for spin MOSFET, MC ratio change directly affects subthreshold region of MOSFET which leads to more efficient device operations. The effect of direct injection of spin into channel on device performance will be clarified in more detail in the near future.
Spin FPGA was numerically benchmarked for 22nm, 32nm and 45nm transistors. We showed that the performance of spin FPGA becomes superior to that of conventional CMOS FPGA as transistor size decreases and MC ratio increases.

**TABLE I**: Area of a single CLB and interconnect. Result of interconnect is taken from Fig. 4.

| CLB area ($\mu m^2$) | Interconnect area ($\times 10^3$)($\mu m^2$) |
|----------------------|---------------------------------------------|
|                      | CMOS | SpinMOS | CMOS | SpinMOS |
| 22nm                 | 118.6| 97.2    | 237.8| 207.0   |
|                      |      |         | 208.2| 206.9   |
|                      |      |         | 208.1|        |
| 32nm                 | 124.1| 102.7   | 242.8| 210.3   |
|                      |      |         | 211.6| 207.8   |
|                      |      |         | 212.1|        |
| 45nm                 | 250.7| 208.3   | 483.0| 416.7   |
|                      |      |         | 418.4| 421.8   |
|                      |      |         | 413.9|        |

**CONCLUSION**

Spin FPGA was numerically benchmarked for 22nm, 32nm and 45nm transistors. We showed that the performance of spin FPGA becomes superior to that of conventional CMOS FPGA as transistor size decreases and MC ratio increases.

[1] S. Sugahara and M Tanaka. Appl. Phys. Lett. 84 2307 (2004).
[2] J. Hayakawa, S. Ikeda, F. Matsukura, H. Takahashi, and H. Ohno Jpn. J. Appl. Phys. 44, L587 (2005).
[3] T. Marukame, T. Inokuchi, M. Ishikawa, H. Sugiyama and Y. Saito, IEDM 2009-215.
[4] T. Inokuchi, T. Marukame, T. Tanamoto, H. Sugiyama, M. Ishikawa, Y. Saito, VLSI Symp 2010, p119.
[5] W. H. Kautz: IEEE Trans. Comput. 18 (1969) 719.
[6] V. Betz, J. Rose and A Marguardt *Architecture and CAD for Deep-Submicron FPGAs*, Kluwer Academic Publishers, February 1999. ISBN 0-7923-8460-1
[7] A. DeHon, ACM Journal on Emerging Technologies in Computing Systems 1, 109 (2005).
[8] C. Dong, D. Chen, S. Haruehanroengra, and W. Wang, IEEE Trans. Circuits and Systems I, 54, 2489, (2007).
[9] W. Zhao and Y. Cao. http://www.eas.asu.edu/~ptm/.
[10] Y. Nagamine, H. Maehara, K. Tsunekawa, T. Inokuchi and Y Saito, Int. Conf. Solid State Devices and Materials, 2008, pp670-671.
[11] H. Sugiyama, T Tanamoto, T Marukame, M Ishikawa, T Inokuchi and Y Saito, Int. Conf. Solid State Devices and Materials, 2008, pp670-671.
[12] Y. Gao, C. Augustine, D.E. Nikonov, K. Roy, M.S. Lundstrom, VLSI Symp 2010, p117.
[13] International Technology Roadmap for Semiconductors, http://www.itrs.net/