Relational Memory: Native In-Memory Accesses on Rows and Columns

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ABSTRACT

Analytical database systems are typically designed to use a column-first data layout to access only the desired fields. On the other hand, storing data row-first works great for accessing, inserting, or updating entire rows. Transforming rows to columns at runtime is expensive, hence, many analytical systems ingest data in row-first form and transform it in the background to columns to facilitate future analytical queries. How will this design change if we can always efficiently access only the desired set of columns?

To address this question, we present a radically new approach to data transformation from rows to columns. We build upon recent advancements in embedded platforms with re-programmable logic to design native in-memory access on rows and columns.

Our approach, termed Relational Memory, relies on an FPGA-based accelerator that sits between the CPU and main memory and transparently transforms base data to any group of columns with minimal overhead at runtime. This design allows accessing any group of columns as if it already exists in memory. We implement and deploy Relational Memory in real hardware, and we show that we can access the desired columns up to 1.63× faster than accessing them from their row-wise counterpart, while matching the performance of a pure columnar access for low projectivity, and outperforming it by up to 1.87× as projectivity (and tuple reconstruction cost) increases. Moreover, our approach can be easily extended to support offloading of a number of operations to hardware, e.g., selection, group by, aggregation, and joins, having the potential to vastly simplify the software logic and accelerate the query execution.

1 INTRODUCTION

OLTP vs. OLAP vs. HTAP. Over the past few years, large-scale real-time data analytics has soared in popularity as more and more applications need to analyze fresh data. This has been exacerbated by new technological trends like 5G, Internet-of-Things, and the advent of cloud computing as an always-on data platform [23, 33]. This leads to the need for systems that can perform both Online Transactional Processing (OLTP) and Online Analytical Processing (OLAP), known as Hybrid Transactional/Analytical Processing (HTAP) [58].

However, OLTP and OLAP systems adopt very different designs. OLTP systems are generally optimized for write-intensive workloads aiming to support high-volume point queries using indexes. In contrast, OLAP systems are optimized for read-only queries that access large amounts of data. Recent efforts for HTAP systems have been bridging OLAP and OLTP requirements by maintaining multiple copies of data in different formats [18, 62] or converting data between different layouts [13, 15, 49, 53, 70].

Data Layout. Efficient access to useful data is a key design goal for all data-intensive systems. Typically, this manifests as finding the optimal data layout, with the traditional schism being row-stores vs. column-stores. Transactional systems employ row-stores, meaning that the physical organization of data items in memory is structured in sequential rows. Row-stores are ideal for queries that either update the contents of a single row, append a new row, or focus on the full information contained in several rows. On the other hand, most analytical systems store data in a columnar fashion that supports fast scan of specific attributes. Column-stores focus on grouping together the same attribute of different rows, hence allowing for efficient analytical querying, i.e., where typically information from multiple rows is aggregated [1].

In order to bridge the analytical and transactional requirements, many HTAP systems use a single architecture that ingests data in row-format, and once data hit the disk, converts them into a columnar format [58]. By doing so, HTAP systems fuse the pipelines of ingesting data and performing analytics, leading to a single data-store maintaining the fresh data and efficient analytics on that same data set. Analysis of systems with adaptive layouts, like H2O [8], Hyper [45], Peloton [15], and OctopusDB [27] showed that every query has an optimal layout which is neither a column-store nor a row-store. However, defining and maintaining multiple layouts carries a large amount of extra complexity, which leads to...
runtime inefficiency arising from heavy book-keeping overheads. The additional complexity of the codebase also results in scalability and maintainability issues.

**What if the optimal layout was always available?**

In other words, “what if the underlying hardware allows us to access only the desired groups of columns while the data is stored in memory as a row-store?” Typically, when using a row-store, we always have to fetch the entire row through the memory hierarchy, irrespectively of the projectivity of the query. On the other hand, column-stores allow us to bring only the desired columns with increasing tuple reconstruction cost as we increase projectivity. This leads to higher query latency when projectivity is close to 100% [8]. The resulting expectation of query cost as a function of projectivity is shown in Figure 1. Ideally, we would want to pay only for the useful data and have negligible tuple reconstruction cost. This could be achieved by seamlessly switching between column-store and row-store depending on what constitutes the better choice, given the projectivity of the query at hand. Prior work on systems that support adaptive layouts via code generation [8, 44, 45] fix a base storage that uses either a row-store or a column-store as a starting point, and the adaptive layout is generated via copying only the relevant data. In turn, this approach creates the need for managing and invalidating these copies upon updates.

*In this paper, we propose a paradigm shift. We propose a novel hardware design for a data reorganization engine that (1) can be implemented in existing commercial platforms, (2) is capable of intercepting CPU-originated memory requests, and (3) of producing responses where the supplied data items are always transparently arranged in the most efficient layout, whilst (4) the source data tables are always stored in physical memory according to the same format—i.e., as a row-store. We show how to integrate this new hardware design with clean abstractions for data system developers to benefit from it without having to redesign the entire database engine.*

**Relational Memory.** To offer native access to any group (whether it be continuous or non-contiguous) of columns without overhead, we create new specialized hardware that acts as an on-the-fly data transformer from rows stored in memory to any group of columns shipped through the memory and cache hierarchy toward the processor. We utilize commercially available systems-on-chip (SoCs) that include programmable logic (PL) and a traditional multi-core processing subsystem (PS) on the same chip. These PS-PL SoCs allow the design and deployment of resource management primitives and create usable proof-of-concept prototypes to assess performance benefits with realistic applications.

Specifically, we capitalize on recent advancements in reprogrammable hardware [65] that allow us to implement programmable logic between the memory and the processor. To ensure ease of programmability, we do not directly expose the specialized hardware to the data system engineer. Instead, we expose a simple abstraction that allows them to request the desired column groups and transparently use the underlying machinery. We refer to the ability to provide an on-the-fly representation of the data that optimizes relational operators as **Relational Memory.**

**Ephemeral Variables.** In a database management system (DBMS) implementation, every relational table loaded in memory is accessible through a variable. By default, this points to the base row-oriented representation of the data, tailored for accessing entire rows and updating or inserting data. Different analytical queries, however, might require a different subset of the relation’s columns. To support this, we introduce **ephemeral variables**, a particular type of variable that identifies a specific subset of columns to access. These variables are never instantiated in the main memory. Rather, upon accessing such a variable, the underlying machinery is set in motion and generates on-the-fly a projection of the requested columns according to the format that maximizes data locality.

The philosophy behind Relational Memory pivots on three main points: (1) pushing relational operators closer to data storage; (2) reorganizing and compacting data items before they are moved toward CPUs to improve locality; and (3) relying on traditional CPUs for data processing once good locality has been achieved. Operating closer to the data also introduces opportunities to exploit the inherent parallelism of memory cells—e.g., by issuing outstanding parallel requests to separate DRAM banks. Note that hardware prefetching can benefit from the memory cells parallelism as long as the accesses follow a sequential logic. Relational Memory, however, has semantic knowledge that helps to perform operations out of sequence and still exploits the inherent memory parallelism. Reorganizing data to improve locality minimizes the waste of constrained CPU cache estate. In turn, this translates to better efficiency for the query at hand and lower cache pollution. Lastly, we enable seamless integration with existing data management systems by limiting our design to data reorganization while relying on CPUs to implement arbitrarily complex analytics.

Figure 2 shows a high-level diagram of the proposed design. The Relational Memory Engine (RME) is located in the programmable logic between the memory and the processor. Upon receiving a request that triggers it, the engine transforms data rows to any desired combination of columns on-the-fly. The processor directly accesses data in the optimal layout through pointers to **ephemeral variables** that triggered the transformation.

**Contributions.** To the best of our knowledge, Relational Memory is the first hardware/software co-design that allows native access to both rows and column-groups over data stored in a row-wise format in memory. Our prototype FPGA implementation supports projection and lays the groundwork for pushing more functionality, i.e., selection, aggregation, group by, and join pre-processing.

![Figure 2: Architecture of the proposed Relational Memory Engine. The engine pushes relational operators closer to data and provides the optimal layout for a given workload via on-the-fly data reorganization.](image-url)
Pushing projection to the hardware creates opportunities for fundamental changes in software/hardware co-design for data systems by enabling systems to have native access to any data layout. In turn, this leads to better cache utilization and eventually paves the way towards a unified HTAP architecture even in the presence of queries with very different access patterns and requirements, essentially taking a fundamental step towards truly HTAP systems. Our work offers the following concrete contributions:

- We present Relational Memory, a novel SW/HW co-design paradigm for general-purpose query engines;
- Relational Memory ensures that every query has always access to the optimal data layout;
- We propose ephemeral variables, a simple and lightweight abstraction to use Relational Memory;
- We implement an FPGA proof-of-concept prototype that already demonstrates the viability and the potential impact of our design;
- We experimentally show that the implemented RME performs native accesses to groups of columns, as if the ideal layout is available in memory with no extra cost to transform rows to columns, leading to higher cache efficiency.

2 BACKGROUND

We now introduce the key concepts necessary to explain the design of Relational Memory. First, we briefly introduce the nuts and bolts of the FPGA technology and the typical organization of PS-PL platforms. Next, we discuss the Programmable Logic In-the-Middle (PLIM) approach that this work builds upon. Lastly, we discuss the key principles for data organization in database systems.

2.1 FPGA Background

Field-Programmable Gate Arrays. FPGAs are programmable devices that can be configured to synthesize hardware functional blocks [47, 75]. FPGAs are becoming increasingly popular in modern platforms because of their high parallelism, reconfigurability, specializability, and power efficiency. In comparison to more traditional CPUs, co-processors, and GPUs, they do not rely on the execution of a set of instructions. Instead, using a bitstream mapping of a synthesized version of the logic to its internal components, they are capable of directly emulating the logic of any digital circuit. This unique capability makes them attractive in many applications as such tailored designs provide high performance because of specific data manipulation, near perfect locality of the data, and many levels of parallelism (e.g., pipelining). For this reason, FPGA technology has been widely used to implement specialized accelerators.

An FPGA device is organized as a large number of programmable logic blocks surrounded by an interconnect fabric. Lookup tables (LUTs) are the main building block in programmable logic. Each LUT is essentially an n-input, 1-output table to be configured with an arbitrary boolean function [6, 66]. Nowadays, multi-output LUTs are also available [76]. Multiple LUTs can be connected using the configurable interconnect fabric. In addition to the logic circuits, an FPGA has both a small memory in the forms of registers or flip-flops and a larger local memory implemented as Block RAM, or BRAMs for short, and can access large but slow off-chip memories through the DRAM controllers. Internal memory can reach TB/s scale bandwidth with sub-microsecond latency, whereas off-chip memories’ bandwidth can reach GB/s [55].

PS-PL Platforms. Recent years have seen the advent of PS-PL platforms, heterogeneous System-on-Chip (SoC) where a traditional system (referred to as PS-side) is associated with a tightly integrated piece of programmable-logic, i.e., an FPGA (referred to as PL-side). The interest surrounding these platforms has gained some momentum with the proliferation of available models produced by Intel [39], Xilinx [77], ETHZ [11, 28], and Microsemi with PolarFire SoC [54]. As shown in Figure 3, the PL domain can communicate through high-performance PS-PL communication interfaces (1, 2, 4), or Interrupt lines (3) with the rest of the system. On-chip communications are carried out using a high-performance, synchronous, high-frequency, multi-primary/secondary communication interface between functional blocks.

These platforms use the popular, open specification, and widely adopted Advanced eXtensible Interface (AXI) protocol [14]. The latter supports asynchronous read and write transactions through dedicated channels operating in parallel between a primary (a processor) and secondary (a memory device). In addition, the protocol allows the primaries to emit multiple outstanding transactions. Each sequence of transactions is identifiable through a given ID [14].

2.2 Programmable Logic in The Middle

Traditionally, in PS-PL platform, the PL-side is used to map hardware accelerators that work in a load-unload fashion. However, Rozokhosh et al. [65] have prompted a shift in paradigm with the introduction of the Programmable Logic in the Middle (PLIM) approach. This approach differentiates itself from the others in light of the way it considers and uses the PL-side. In fact, this approach advocates the use of the PL-side as a secondary route to main memory that can entirely or partially replace the normal route. As illustrated in Figure 3, instead of using the normal data path (highlighted in yellow), CPU traffic can be redirected through the PL-side before reaching the main memory (highlighted in blue).

The principal advantage of PLIM resides in its ability to intercept, inspect and manipulate any PS-originated memory transactions before they reach the main memory. This capability of inspecting memory traffic at the granularity of individual transactions has already been leveraged to address and tackle bedeviling problems. For instance, PLIM demonstrates how by simply manipulating each transaction address, memory fragmentation introduced by address coloring can be mitigated [65]. The same authors have also shown that the same type of module can be integrated into a wider framework in order to address the problem of memory traffic scheduling [37]. Interestingly, PLIM modules have also been used to
highlight the possibility of memory-based on-chip denial-of-service attacks from remote cores under special conditions [38].

2.3 Data Layouts

A key decision for any data system is the employed data layout, which is tightly connected with the type of workloads it primarily targets. In general, there are two extremes according to which DBMS’s store data: the n-ary storage model (row-stores) and the decomposition storage model (column-stores). Row-stores follow the volcano-style processing model where data is organized as tuples, and all the attributes for each tuple are stored sequentially [36, 59]. This design allows superior performance for OLTP workloads [7] since the queries in transactions generally tend to operate on individual tuples. Traditional DBMS like Oracle [9], IBM DB2 [21], SQL Server [4] follow this paradigm. In contrast, column-stores are organized as columns following the decomposition storage model. They process data one column at a time, hence are better suited for OLAP workloads [1] where the queries tend to operate on multiple tuples but only access a small fraction of the attributes. Most contemporary data systems like Vertica [50], Actian Vector (formerly Vectorwise [80]), MonetDB [20], Snowflake [25] use columnar storage. Even traditional row-stores have developed new variants that allow to store data in columnar format [18, 48, 51]. Because of these design principles, OLTP queries are costly in column-stores while OLAP queries are expensive for row-stores. Systems targeting hybrid workloads support hybrid layouts in the form of column-groups via the flexible storage model [15] or adaptive layouts [8, 27, 45]. These systems dynamically adapt the storage layout depending on the workload by keeping the same data in different layouts and by converting the data between row and columnar formats for transactions and analytics, respectively. Because of these conversions and multiple layouts, these systems generally have high complexity, high materialization cost, and heavy book-keeping overheads.

3 RELATIONAL MEMORY

We now present the high-level design of our Relational Memory Engine (RME) and the interface that allows its transparent use.

Implementing Relational Algebra Operators in Hardware.

The core innovation introduced with the Relational Memory paradigm is the implementation of relational algebra operators in hardware to achieve transparent near-data processing. Relational Memory represents a novel software-hardware co-design approach with a clean architecture and a simple abstraction that is exposed to the application level.

The fundamental physical relational operators are projection, selection, sorting, aggregation, group-by, and join. In this paper, we focus on projections that require the capability to fetch a subset of the data residing in memory (projecting the desired columns). Realizing near-data projection lays the groundwork for pushing the highest degree of processing to the hardware as long as data movement represents the performance bottleneck.

Current state-of-the-art systems that support hybrid layouts create the desired column-groups in software, therefore, the data has to pass through the memory hierarchy and get copied in order to create the desired layout. On the contrary, we propose to make any layout available on the fly by creating a special memory address that is an alias of the original data pointer—a.k.a. an ephemeral variable. CPU accesses to ephemeral variables are intercepted by our RME that constructs a response to each memory request. The response payload is produced by packing only useful data. Therefore, from a CPU’s standpoint, the data appears as always structured according to the optimal layout for the query at hand. Two key benefits are that (1) we do not duplicate data in memory as the ephemeral variables provide a reorganized view of the original data; and (2) unlike traditional hardware accelerators, the CPU can immediately access partial results without having to wait for the RME to complete a full pass over the original data. In fact, only memory requests for non-ready data chunks are stalled by the RME.

A Low-Level Example. One can think of a row in a database table as a struct of the type struct row table[]. If one wants to access only the numeric field (num_field) from all the rows, i.e., perform a column access, this creates a stride-pattern data access, where 8 bytes are accessed every few hundred bytes of data. This is inefficient because (1) each new row always pulls an entire cache line from memory; (2) the large strides are not handled well by hardware prefetchers; and (3) in general, more data is transported from main memory to the processors than what is strictly required for the requested type of access. In the considered example, with a cache line size of 64 bytes, only 1/8 of a cache line is utilized.

A column-store optimizes these types of accesses by storing each attribute separately, hence allowing for accessing only the numerical field through an array of the type: long num_field_array[]. Indeed, in this case, only data items strictly required for the final computation are transported from main memory, resulting in a highly localized access pattern. However, this comes at the cost of having an inefficient layout for insertion and deletion, and paying increasing tuple reconstruction cost with higher productivity.

Near-Data Projection. To offer contiguous access to a specific column (or group of columns), we design our RME leveraging the PLIM paradigm. The PLIM [65] design is conceptually similar to Processing-In-Memory (PIM) [52] and Near-Memory Processing (NMP) [17] as they all execute logic close to memory. The key innovation of the proposed RME is that it creates data that does not exist in main memory, which the CPU can use transparently as if it exists in main memory. RME can be implemented in FPGA in a PS-PL platform. As we demonstrate in Section 6, our FPGA prototype already provides a significant performance advantage. Nonetheless, we envision that additional benefits can be unlocked by embedding a similar design within the memory controller itself. The RME creates memory aliases to expose non-contiguous content as if it were contiguous. In other words, the module enables accessing the same...
content in main memory under different strides, but always as if it were stored contiguously from the perspective of the main CPUs. This is drastically different compared to traditional scatter-gather strategies [69] initiated by typical DMA-capable accelerators (e.g., SIMD processors) because data transformation is performed in-line with the instruction stream, with fine-grained information on the exact byte-wise location of data items that are useful for the computation at hand; and because it allows predicting and exploiting data reuse across processing micro- and macro-phases. The RME receives as input the intended access stride of the query (that maps to the physical addresses of the columns to be accessed). It then issues parallel main memory requests for the target data. Finally, it assembles multiple entries in a single packed cache line to be sent to the processor.

This abstraction creates non-materialized in-memory aliases of column-groups that push up to the memory hierarchy arbitrary subsets of columns in dense memory addresses from the cache memory perspective. That way, both efficient column-oriented and row-oriented accesses can be supported while minimizing CPU cache pollution with unnecessary attributes.

Ephemeral Variables. In order to provide control to use and initialize the proposed hardware, we propose a lightweight software/hardware interface. Specifically, to use Relational Memory, the data system developer shall use a new type of memory pointers termed ephemeral variables, which do not correspond to a real main memory location. Any CPU access on ephemeral variables (that leads to a cache miss) is routed to and satisfied by the PL. To understand the semantics, the expected content, and the versatility of ephemeral variables, let us consider a concrete example.

Suppose that a full relational table is loaded in memory and structured as a classic 2-D array, as previously discussed. For instance, the table under analysis corresponds to the array struct row table[], where each row is defined as:

```
Listing 1: C-style relational table row definition.
1 struct row {
2   long key; /* 8 bytes */
3   char text_fld1 [8]; /* 8 bytes */
4   char text_fld2 [12]; /* 12 bytes */
5   char text_fld3 [20]; /* 20 bytes */
6   char text_fld4 [16]; /* 16 bytes */
7   long num_fld1; /* 8 bytes */
8   long num_fld2; /* 8 bytes */
9   long num_fld3; /* 8 bytes */
10  long num_fld4; /* 8 bytes */
11  long num_fld5; /* 8 bytes */
12};
```

In order to have direct access to a single column, or to a group of columns, we create an ephemeral variable that is registered with the RME. Accessing the newly created ephemeral variable from the CPU’s perspective is equivalent to having direct access to a subset of columns with a packed view of the relevant fields. Following our example, to access only columns num_fld1, num_fld3, and num_fld4, we create an ephemeral variable of the type:

```
Listing 2: C-style ephemeral type definition.
1 struct column_group_1 {
2   long num_fld1; /* 8 bytes */
3   long num_fld3; /* 8 bytes */
4   long num_fld4; /* 8 bytes */
5};
```

The ephemeral variable with type column_group_1 provides access to the three desired columns as a contiguous array. This comes with three advantages. First, only useful information is propagated through the cache hierarchy, dramatically reducing cache pollution and working-set size, and thus improving cache reuse and locality. Second, RME orchestrates data accesses to main memory in a way that is DRAM structure-aware to maximize throughput—much like a DMA would. Third, having turned a stride access, potentially spanning multiple pages, into a sequential pattern over a smaller buffer greatly improves the effectiveness of CPU-side prefetching.

The Lifetime of a Memory Access. Here, we demonstrate the lifetime of a memory access targeting an ephemeral variable, through a sample analytic query:

```
Listing 3: Sample projection-aggregation query.
1 SELECT sum(num_fld1 * num_fld4)
2   FROM the_table
3 WHERE num_fld3 > 10;
```

This query only requires accessing three out of the ten columns, and can be evaluated using an ephemeral variable as follows:

```
Listing 4: Query logic in C language.
1 struct row the_table[];
2 /* Autogenerated Code Block - START*/
3 struct column_group_1 {
4   long num_fld1;
5   long num_fld3;
6   long num_fld4;
7};
8 struct column_group_1 cg[] =
9   register_var(the_table, num_fld1,
10   num_fld3, num_fld4);
11 /* Autogenerated Code Block - END */
12 int sum = 0;
13 for (int i = 0; i < cg.length; i++) {
14   if (cg[i].num_fld3 > 10) {
15     sum += cg[i].num_fld1 * cg[i].num_fld4;
16   }
17 }
```

Note that this is a simplified code snippet. To optimize for performance, one can implement state-of-the-art approaches including predication [10, 16] to avoid branch misprediction and vectorization [19] to increase locality and computation efficiency. Orthogonally to those optimization strategies, we focus on minimizing data movement. Ephemeral variables fetch only relevant columns from memory leading to optimal cache utilization. The moment an ephemeral variable is registered (Listing 4, line 9), the geometry of the access is defined (that is, the pattern of scattered accesses on the original data), and when the data is first accessed—i.e., when the statement cg[i].num_fld3 > 10 is evaluated—the RME starts projecting only the relevant columns. We present the design of RME in detail in Section 5.

4 DISCUSSION

Updates & MVCC Transactions. While Relational Memory offers native access to both rows and columns, the base data are stored in-memory in a row-oriented format. We treat all ephemeral variables as read-only columns or group-of-columns that accelerate analytical queries. Updates are handled by accessing the read/write row-oriented base data. Specifically, new rows are appended in the base data. In order to support in-place updates and deletion we use two timestamp fields for every row, storing potentially multiple versions. The first timestamp is set when the row is inserted and
marks the beginning of its validity, and the second is set when the row is deleted or replaced by a newer version, marking the end of its validity. Every time an ephemeral variable is accessed, it generates the (group of) column(s) that contain the rows that are valid at the time of the query. Using the timestamp scheme discussed above, RME also support MVCC transactions via snapshot isolation.

**Compression.** Relational Memory natively supports dictionary and delta (frame of reference) encoding that is frequently used in state-of-the-art column-store systems [1, 2, 81]. Note that both can be used in row-oriented data and hence, they can benefit any groups of columns requested by ephemeral variables.

Another compression scheme used in column-store systems is run-length encoding (RLE) [2]. Contrary to dictionary and delta encoding, RLE has an expensive decoding step and relies on the data being sorted. RLE achieves typically higher compression rates, but is less frequently applicable, hence, typically, is not preferred over dictionary and delta compression [81].

**Indexes & Execution Strategies.** Base data indexes on the row-major data can still be very useful when updating the data (using the MVCC approach outlined earlier) and when we have a very selective query. Note that Relational Memory revolutionizes the software design of query engines by offering at the same time native access to both columns and rows. Hence, at runtime, the query optimizer can decide to execute one query with indexes and another query with columns, alternating between a row-at-a-time and column-at-a-time execution strategy depending on what is the best fit for each query. In this paper, we provide the hardware infrastructure for this radical paradigm shift and showcase the opportunity of accessing any data layout on a per-query basis. Implementing a full-fledged hybrid query engine is left for future work.

**Fractured Mirrors without the Mirrors.** Essentially, in this paper, we take a big step from the fractured mirrors approach [61, 62] to offer access to both a row-store and a column-store version of the data, along with everything in-between (arbitrary groups of columns), without maintaining multiple copies of the data.

5 **H/W DESIGN AND IMPLEMENTATION**

The goal of our design is to enable in-memory data storage in a single format (i.e., row-stores) while offering a reorganized view of the same data with ideal locality. To do so, we interpose a PL engine between CPUs and main memory. The data organization in main memory never changes but the semantics of memory accesses performed by the CPUs are re-defined on the fly. The proposed data reorganization engine goes under the name of RME. The engine uses knowledge of the target relation’s geometry to make the retrieved data appear as if they were initially stored in compacted projections.

As depicted in Figure 5, our RME is comprised of six modules: (1) Configuration Port, (2) Monitor Bypass, (3) Trapper, (4) Requestor, (5) Fetch Unit, and (6) Relational Buffers. The RME interacts with the PS through two primary and one secondary AXI port. This section provides a bird-eye’s view of the RME operating mode and the role of each of its sub-components.

**Configuration Port.** The architecture features a configuration port that enables the DBMS to specify the location and geometry—that is, the database tuple width, tuple count along with size and positions of the requested columns—of the targeted database table.

![Figure 5: Abstract overview of the RelBuffer components and interconnections with the PS-side.](image-url)
within a set of bus-width-aligned transactions. Each descriptor also indicates the positions where to store the extracted columns. The descriptor is generated such that the resulting main memory size chunk of data from main memory and then directing it to the Fetch Unit. Each Fetch Unit is responsible for retrieving one fixed-size chunk of data from main memory and then directing it to the designated place in the Reorganization Buffer. The unit is internally structured in several distinguished sub-component, namely the Reader, the Column Extractor, and Writer, briefly described below.

The Reader directly interacts with the main memory controller. It primarily produces memory fetch requests that reflect the specifications of the descriptor passed by the Requestor. The Reader uses the AXI protocol to perform variable-burst memory requests towards main memory at the granularity of a single bus beat (i.e., bus-width, which is typically a fraction of the cache-line size). The data payload obtained by the Reader is passed to the Column Extractor module.

The Column Extractor module extracts the individual bytes that correspond to the portion of the columns of interest (Listing 4, lines 8–10). If the target column(s) spans multiple bus lines, it waits until all the required data items are accumulated and indicates the output’s validity by setting the enable signal. If necessary, it performs appropriate shifting to pack useful data into contiguous chunks. It finally passes the packed data to the Writer module.

The Writer receives the data from the Column Extractor, along with the location where to store the packed data in the Reorganization Buffer. It then forms a single write request with said data payload towards the Reorganization Buffer. Any write operation emitted by a Writer module passes through the Monitor Bypass.

### 5.1 Data-path and Work-flow

In this section, we go over the workflow of the RME following a given CPU-originated read transaction. We will consider two scenarios. First, (1) we consider the case where the requested data has already been fetched from main memory and re-organized. Thus, it can be immediately sent to the requesting CPU (Reorganization Buffer hit). Next, (2) we cover the case in which the target data needs to be fetched from main memory (Reorganization Buffer miss). We consider the two cases separately and refer to Figure 5 as we discuss each step of the flow.

The accelerator is designed to be generic and to operate with various data layouts. Therefore, the software must initially configure the RME with the geometry of the target relation as described in

| Parameter          | symbol | Address               | Description                                                                 |
|--------------------|--------|-----------------------|-----------------------------------------------------------------------------|
| Row size           | R      | base+0x00             | database tuple width                                                         |
| Row count          | N      | base+0x04             | database tuple count                                                        |
| Software reset     | SW     | base+0x88             | software triggered reset request                                             |
| Enabled columns count | Q      | base+0x8c             | amount of columns of interest                                               |
| Column width       | Ca     | base+0x10j*%j*2      | j-th column width j ∈ [0, 11]                                               |
| Column offset      | Co     | base+0x26j*%j*2      | j-th column offset j ∈ [0, 11]                                              |
| Frame number       | F      | base+0x3c             | filtered table frame number                                                 |

Table 1: RME configuration port: addresses and description.
the Monitor Bypass. The latter checks whether the new request can be immediately served (Reorganization Buffer hit) or if it must be stalled (Reorganization Buffer miss). The check is done by using the A field to fetch the cache-line status from the Metadata SPM. Speculatively, the (possibly valid) content of the requested cache-line is fetched from the Data SPM.

**Reorganization Buffer Hit.** If the cache-line was marked as complete, the Monitor Bypass can immediately send its content—i.e., the tuple \([ID, RD]\)—to the Trapper \(\mathcal{A}\). Then, using this information, the Trapper forms an AXI compliant transaction to reply to the CPU’s initial request \(\mathcal{B}\).

**Reorganization Buffer Miss.** If part of the data composing the requested cache-line is missing, the request must be stalled. In this case, the request \(ID\) is stored in the metadata SPM. Once enough data returns from the Fetch Units and the cache-line becomes complete, the \(ID\) is removed and the \([ID, RD]\) tuple is sent to the Trapper \(\mathcal{A}\). If the miss in question is the first miss of the frame, a signal is sent the Requestor module to start the descriptor generation.

As described in Section 5, the Requestor has a crucial role in orchestrating the Fetch Units and their interaction with main-memory, data extraction, and data forwarding to the Reorganization Buffer. The Requestor prepares a series of descriptors for the Fetch Units using Eq. 1–6. It keeps track of which Fetch Unit is currently busy and provides the next descriptor to any available Fetch Unit \(\mathcal{B}\).

Upon receipt of a new descriptor, the Fetch Unit sends a request for a burst of \(R_{\text{burst}}\) data responses towards main memory at location \(R_{\text{addr}}\). Once the full response is received, the Column Extractor performs data filtering using the parameters \(F_{\text{src}}\) and \(F_{\text{dst}}\). Next, the filtered data is sent to the Reorganization Buffer at the address specified by \(W_{\text{addr}}\). On its way to the Reorganization Buffer, the filtered data chunks go through the Monitor Bypass \(\mathcal{C}\). The latter simultaneously updates the record of the newly (partially) filled cache-lines in the Metadata SPM \(\mathcal{D}\). More importantly, the Monitor Bypass recognizes if the recent update was the last missing part of any incomplete cache-line. In other words, by simultaneously fetching both metadata and data record of the most recently updated cache-line \(\mathcal{E}\), the Monitor Bypass checks for any full cache-line. In which case, the Monitor Bypass immediately sends the corresponding \(R0\) back to the Trapper \(\mathcal{F}\) to de-queue any pending \([A, ID]\) request. The Trapper then replies to the CPU by forming a \([ID, RD]\) response \(\mathcal{G}\).

### 5.2 Toward Efficiency and Parallelism

The memory subsystem is a well-known performance bottleneck in modern SoCs. This is due to the characteristic latency of the main memory cells (e.g., DRAM) or due to the constrained bandwidth between PL and main memory. Common strategies for taking full advantage of memory subsystems include (1) making memory accesses more efficient by re-ordering the requests to benefit from an already-open DRAM row, and (2) improving DRAM bank-level parallelism to improve throughput. Taking inspiration from the mentioned techniques, we consider the design described in Section 5.1 as the baseline. We have then implemented a number of revisions to our design with increasing level of refinement to improve memory parallelism.

We consider the design presented earlier in this section as our Baseline Design (or BSL). The first revision of the BSL design consists in the integration of an intermediate buffer inside the Fetch Unit. The rationale behind this modification is that a sizable amount of time is lost when the data is being written to the BRAM once it has been read and filtered by the Reader and the Column Extractor. By introducing a simple register in charge of packing the filtered columns and only writing their content to the BRAM once a full cache-line has been extracted, we reduce the amount of accesses to the Reorganization Buffer. Following the addition of this packer, we identify this revision as PCK. The second and final revision of the design aims at increasing the utilization of the bus between the Reader and the DRAM controller by enhancing the Memory Level Parallelism capability of the design. Hitherto only one outstanding read transaction was supported by the Reader whereas, in the MLP revision, the Fetch Unit has been augmented to emit up to 16 independent outstanding transactions.

### 6 EVALUATION

We now show experimentally that RME offers efficient native accesses of any group of columns, outperforming direct row-wise accesses, and in most cases also columnar accesses.

#### 6.1 Target Platform

We implement RME using a Xilinx Zynq UltraScale+ MPSoC platform [77]. The development board, Xilinx UltraScale+ ZCU102, is equipped with 4 Cortex-A53 cores each associated with a private 32 KB L1 data cache and grouped together by a shared unified L2 cache of 1 MB. On the PL-side, RME employs two internal memory blocks: the Data SPM and the Metadata SPM. The former, a large chunk of 2 MB directly impacts the critical path and prevents the design from reaching higher frequencies. For that reason, the presented design is constrained to 100 MHz (i.e., one-third of the maximum reachable frequency). The PL-side resource utilization is discussed in Section 6.4. The benchmark queries are compiled with GCC 7.3.1 for ARM64 and executed on Linux 4.14.

#### 6.2 Relational Memory Benchmark

We designed a synthetic benchmark to test the behavior of RME under a number of representative query access patterns. The benchmark, termed Relational Memory Benchmark, consists of six queries focusing on projection, selection, and aggregation. The queries are executed assuming that all data is in main memory. The queries are shown in Listing 5. \(Q0\) is the simplest query that calculates an aggregate of a single column. \(Q1\) is a projection of \(k\) columns (non-contiguous or contiguous), where \(k\) can be varied. \(Q2\) projects one column and imposes a selection condition on a second column. \(Q3\) performs an aggregation (sum) over a subset of column, selected based on a predicate on another column. \(Q4\) further generalizes \(Q3\) by adding a group by statement based on a third column. Finally, \(Q5\) performs a hash join query over two distinct tables.

In all the queries except for \(Q5\), the benchmark only accesses a relation \(S\) with \(n\) columns \(A_1, \ldots, A_n\). Each column \(A_i\) has a tunable width \(C_{A_i}\). \(Q5\) also accesses a second table \(R\) with similar structure.
Benchmarks & Measurement Setup. Unless otherwise stated, the row-size of the benchmark data is 64 bytes and the column-size is 4 bytes. Throughout our experimentation we test with varying values of both to see their impact as well. Further, the data size is by default 32MB and we increase it up to 2GB for the scalability experimentation. When reporting latency numbers, we avoid measurement anomalies by repeating each experiment 30 times and reporting averages and standard deviations.

6.3 Experimental Results

Impact of Hardware Revisions. Our first experiment shows the impact of the different hardware revisions introduced in Section 5. Figure 6 shows the execution time of Q0 where we calculate the sum over one column. The y-axis varies the offset of the projected column, and the seven different lines correspond to the following configurations: three RME versions (BSL, PCK, MLP, see Section 5.2) either cold or hot and direct DRAM access. We observe that there is a progressive performance improvement from our hardware revisions. Initially, cold BSL is 16× slower than loading data directly from a row-oriented layout from main memory due to the lack of memory parallelism. On the contrary, with our most optimized revision (MLP) even without having the projected column in the Reorganization Buffer (MLP cold, shown in the solid purple line), RME is faster than a direct access in the row-oriented data in memory (blue dotted line). Note that all hot (dashed) lines coincide irrespectively of the hardware revision. Further, we observe that projecting cold columns (i.e., the requested columns are not initially buffered in the Reorganization Buffer) incurs up to 20% lower latency than going through the normal route for our MLP design (purple line in the figure). The reason is that (1) RME better exploits the internal memory bandwidth to fetch only the desired data items at bus-width granularity, and (2) the CPU caches are not polluted with unwanted fields and are therefore used more efficiently.

In the rest of our experimentation, we use the MLP hardware revision. As a result, in the remainder of this section, when using RME we refer to the performance of the MLP hardware revision.

Column Offset does not Impact Performance. Figure 6 has a second important message. By varying the offset $O_A$ of the projected column $A_1$, we identify that the offset from which we are reading from, generally does not affect performance. The experiment considers a table of 64-byte rows and a target column width $C_A = 4$ bytes. We observe that the value of the offset has no impact on latency, especially when DRAM is directly accessed and when RME is hot, regardless of the considered revision. We observe three spikes (at 13 to 15, 29 to 31, and 45 to 47) for the cold cases (i.e., when the targeted data is not yet ready in the Reorganization Buffer). The reason behind these spikes is that as we increase $O_A$, the descriptors emitted by the Requestor vary. In fact, most of the time, the 4 bytes of interest fit within 16 bytes (i.e., the width of the bus), leading the Requestor to create a read transaction with a burst length of 1. However, when the offset plus the size of the data does not fit in a single bus width (e.g., 13+4, 29+4, 45+4, ...), the Requestor must emit read requests with a burst length of 2, leading to a slightly higher latency.

Since the offset of the targeted column does not affect query performance, in the remainder of our experiments, the first targeted column will always be $A_1$ that starts at the beginning of the row.

RME Enables Native Columnar Accesses. Our first experiment shows that RME can efficiently access—and propagate through the cache hierarchy—individual columns when reading row-oriented data. We now evaluate Q1 with $k = 3$. The three target columns are not contiguous, with offsets $O_{A_1} = 0$, $O_{A_2} = 24$, and $O_{A_3} = 24$ (i.e. $A_3$ has offset $0+24+24=48$ from the beginning of the row) respectively. All three columns have same width which varies in the range [1,16] bytes. Figure 7 shows the normalized execution time to complete Q1. We compare the time to access the data directly from the row-oriented organization in main memory (Direct Row-wise access) and through our RME. We consider MLP with both hot and cold accesses. Finally, we also compare against direct access to data already structured in columnar format (Direct Columnar access).

Figure 7 shows that RME outperforms direct row-wise access irrespective of whether accesses are cold or hot. The takeaway is twofold. First, accessing a group of columns via RME delivers the data with the optimal layout and outperforms direct accesses to a row-oriented version of data in memory. Second, RME achieves an average latency that is comparable to pure columnar accesses. Specifically, Figure 7 shows that for column size 16 bytes and above, Q1 is faster through RME rather than through a pure column-store. Therefore, data can be simply stored row-wise in memory while any
hybrid layout can be delivered by the RME with no row-to-column data transformation latency.

**Cache Miss Ratio.** The benefits from MLP observed in Figure 7 for \( Q_1 \) can be further explained if we take a careful look at the composition of cache requests and misses. Figure 8 shows the L1 (top) and L2 (bottom) cache requests/misses for the MLP design. We observe that RME causes better cache utilization in both L1 and L2, which explains the significant performance savings despite the cost of routing data through the accelerator. Note that the total size of the target columns does not fit in L1, but since the column is accessed sequentially, the L1 pre-fetcher can drastically reduce the L1 misses. The high number of L2 requests is attributed to the L1 pre-fetcher. Overall, RME provides ideal cache locality as no extra data items are ever propagated to the CPU caches beyond what strictly required to execute the query at hand. Conversely, accessing the three columns in the column-store creates three independent sequential access streams. The CPU in our target SoC supports up to four independent pre-fetch streams. Therefore most of the memory access cost is successfully hidden. On the other hand, directly accessing a few columns from a row-wise data representation in memory fetches a lot of unnecessary (columns), leading to poor locality.

**RME Has Stable Performance as Projectivity Increases.** When comparing with columnar accesses we have to also take into account the tuple materialization cost. In our next experiment we vary the projectivity from 1 to 11 columns. Figure 9 shows that for low projectivity (between 1 and 4) reading from a columnar database is faster than RME. For projectivity of more than 5 columns, RME outperforms direct columnar accesses because of the tuple reconstruction cost. In addition, through our profiling we observed that the pre-fetcher can recognize up to four parallel sequential streams of accesses, which helped the column access for low projectivity. Overall, RME consistently outperforms direct row-wise accesses that pollute the caches with unwanted fields and outperform columnar access beyond a projectivity threshold.

**Setup for \( Q_2 \) through \( Q_5 \).** We continue our experimentation with \( Q_2 \) through \( Q_5 \) from our benchmark from Section 6.2, focusing on the comparison between RME and direct row-wise access. Two sets of experiments are conducted for each query. First, we vary the column size of a table with 64 byte-wide rows; second, we access 4 byte-wide columns while varying the row size. The default cardinality of the base table is 44K rows.

**RME Offers Efficient Near-Memory Projection.** We now discuss the performance of \( Q_2 \) that has around 90% selectivity. \( Q_2 \) benefits by fetching only the two desired columns instead of the entire row, while the selection of \( Q_2 \) takes place on the software side. The performance graph is shown in Figure 10a. We observe that RME offers faster execution time in both cold and hot cases. Figure 11a shows that the performance gain of RME increases for larger row size (up to 1.4x). We note that RME’s latency remains virtually the same as it accesses exactly the desired amount of data. However, answering the query via the direct access of the row-oriented data leads to poor cache utilization as larger rows lead to higher cache pollution. This shows that RME has a much stable and predictable performance irrespective of the row size.

**Selection, Projection, and Aggregation Queries.** In our next experiment, we consider the more complex queries \( Q_3 \) and \( Q_4 \), that test selection, projection, aggregation, and group by. The selectivity of \( Q_3 \) and \( Q_4 \) is less than 10%. Similarly to before, we stress the RME using two different sets of experiments. Figures 10b and 11b show the normalized latency of \( Q_3 \) when varying the column size with fixed row size, and when varying the row size with fixed column size, respectively. When the RME is used, the execution time is faster than the traditional data access to main memory. For \( Q_4 \), in particular, the cost of group by dominates the execution time compared to data accessing, thus, the performance improvement is reduced as shown in Figures 10c and 11c. We note that both \( Q_3 \) and \( Q_4 \) have a performance drop for column width 16 bytes. This is attributed to the fact that in some cases we need to fetch data spanning 32-bytes, i.e., half the cache line size. This happens more frequently due to the low selectivity. As a result, the 2x increase in efficiency in the cache utilization is canceled out by the overheads of routing through PL memory.

**RME Reduces Data Movement for Joins (\( Q_5 \)).** When considering queries that join multiple tables (\( Q_5 \)), RME can help to project only the relevant columns, that is, the columns of the join attributes and the column(s) projected in the SELECT statement of the query. In this experiment, we join using a state-of-the-art hash-based join algorithm with a single-pass hash table generation, which is then probed by the second relation. Half of the entries of the outer relation have a match in the inner relation. Figure 12a shows the normalized query latency while varying target column sizes. We observe that joining through RME gives a benefit between 5% and 10%. Figure 12b compares the execution time of this query for different row sizes. RME reduces the total runtime by up to 12% depending the row width. The graph also shows that the CPU overhead (solid portion of the bars) of hashing constitutes the majority of the
Figure 10: Aggregation queries with varying column size. Depending on the query, the benefit of using RME varies. However, RME outperforms row-oriented direct memory accesses since it accesses only useful data.

Figure 11: Aggregation queries with varying row size. Depending on the query characteristics and projectivity, the benefit varies. However, RME enables more efficient accesses by providing the optimal layout.

Figure 12: RME performs join faster than traditional row-store join by minimizing data movement.

Figure 13: RME scales with data size.

runtime which is constant across RME and direct row-wise access, while, RME can optimize the data movement by up to 41% as the row size increases because of its lower cache misses, better strided accesses, and higher cache utilization.

RME Scales with Data Size. RME supports arbitrary data sizes despite having a small data SPM due to the space limitations imposed by the platform. To evaluate RME’s scalability, we repeat Q1 while projecting four target columns in larger tables ranging from 32 MB to 2 GB. Every time we fill the data SPM, we use the light-weight reset mechanism introduced in Section 5. Figure 13 compares Q1 execution time with RME normalized by the direct row-wise access. We observe that the benefit from using RME remains virtually unchanged for any data size, because RME always provides the optimal layout.

RME Provides Better Performance in All Queries. Overall, the experimental analysis shows that our RME outperforms direct DRAM accesses over row-oriented data, even though data accesses through the FPGA can be quite inefficient. This result demonstrates that it is possible to achieve native in-memory columnar accesses over data that is stored in row-oriented format. Additional experiments that were omitted due to space constraints are available in an extended technical report [64].

Long-Term Potential and Impact. Even though the underlying PLIM approach [65] provides fine-grained observability and management of memory traffic between processors and memory hierarchy, it forces transactions to cross through a lower-frequency domain, i.e., that of the PL (100 MHz in our case). Because of this, an additional latency is added to each transaction due to the clock domain crossing (CDC) overhead [37, 38, 65]. This means that under PLIM, the latency of individual memory transactions can be significantly worse than what observed with direct memory accesses. This effect is particularly strong in the considered hardware platform, as documented in [37]. Nonetheless, as we observe in our experiments, the benefits by RME fully offset the described effect. This observation sets the basis for our long-term vision that is twofold. On the one hand, our RME is expected to provide even larger performance benefits in newer platforms with better PS-PL integration and lower-latency communication interfaces. On the other hand, the ability to offer significant performance advantages...
even at low synthesis frequencies makes our design suitable for integration directly within the main memory controller.

### 6.4 PL Resource Utilization and Timing

After the synthesis and the implementation of the design on the ZCU102 development board using Vivado 2017.4, we obtained reports regarding the PL resources utilization of the MLP RME design.

As mentioned earlier, all the designs presented and tested in this article run at 100 MHz. Despite being only one third of the achievable frequency on the target board, the MLP design has proved the utilization of the resources at hand to be efficient. As shown in Table 2, the area utilization never exceed 3% except for BRAM for which we purposefully maximize the size of the SPMs to improve the performance of RME. The compactness of the design paves the way for more ambitious revisions where modules could be duplicated (e.g., a design featuring multiple Fetch-Units) and pipelines extended. Moreover, a low utilization means that proposed architecture could fit in smaller PS-PL platforms such as the Zybo z7-10, making our approach a good fit for edge and cloud computing.

| Resources | LUT | FF | BRAM | DSP |
|-----------|-----|----|------|-----|
| Utilization (%) | 2.78 | 0.68 | 60.69 | 0.08 |

Table 2: Post-implementation area report for the MLP design implemented on the Xilinx ZCU102.

### 7 RELATED WORK

#### Hybrid Layouts

Following the one size does not fit all rule [73], many HTAP systems use the row-format to ingest data and then convert it to columnar-format for analytical processing [58]. Examples include SAP HANA [31], Oracle TimesTen [49], MemSQL [70]. Thus, these HTAP systems fuse the data ingestion and data analytics pipelines. The optimal layout is more often neither a column-store or a row-store [8]. Systems like H2O [8], Hyper [45], Peloton [15], and OctopusDB [27] use adaptive layouts depending on the query access patterns. For example, OctopusDB maintains several copies of a database stored in different layouts. It thus so by means of a logical log as its primary storage structure and then creating secondary physical layouts from the log entries. H2O is another hybrid system which dynamically adapts the storage layout depending on the workload. It materializes parts of the data in various patterns depending on the query and as the workload changes, the storage and access patterns keep adapting accordingly. Peloton also uses an adaptive policy, however instead of an immediate policy, it adopts an incremental data reorganization policy. Besides, H2O uses multiple execution engines to keep the same data in different layouts, whereas Peloton uses a single execution engine. These systems need to store multiple layouts of the data and also need to convert between formats which increases the complexity, materialization overhead and maintenance cost.

#### FPGA in DBMS

FPGAs can be integrated either by using it as a filter by placing it between the data source and CPU or by using it as a co-processor to accelerate the workload [30, 40–42]. In the former approach, the FPGA is used as a decompress-filter between the data source and the CPU to improve the effective bandwidth. This approach has been adopted by a number of systems like Netezza [32], Mellanox [57], and Napatech [56]. In contrast, in the latter approach, the FPGA can access the host memory directly and communicate with the CPU via shared memory, thus avoiding the extra copying of data from/to the device memory. Although this approach is still quite new, a few systems have deployed FPGAs as co-processors [24, 34, 67, 71]. Following this direction, different operators of DBMS like selection [74], aggregation [26], compression [60], decompression [29], sort [79], groupby [3], and joins have [35, 78] been accelerated. Another popular technique is to integrate FPGA to the CPU as an I/O device to accelerate database analytics especially where CPUs are the bottleneck. Contrary to the co-processor technique, the CPU and FPGA have their own memory in this architecture. The FPGA is connected to the CPU through buses. When the FPGA receives tasks from the CPU, it copies the data from the host memory to the device memory, then it fetches data from the memory, writes the results back to the device memory after processing, and finally copies the results back to the host memory. A number of systems like Kickfire’s MySQL Analytic Appliance, dbX have implemented this architecture [22, 68].

Many FPGA-based accelerators report high throughput, however, the low bandwidth between FPGA and host memory (or CPU) is a bottleneck [43]. In addition, the transfer latency of data from the host to FPGAs is significant. Thus, designing accelerators is challenging for systems with unpredictable memory access patterns.

Another interesting line of work is query accelerators in the network layer [5, 12, 46, 63, 72], that access non-local memory. However, there are common aspects with database systems that these works aim to reduce the number of network traversals to access non-local memory, the data movement inefficiencies, and network overhead by accelerating operators. Particularly, Farview [46] accelerates a wide range of operators, including projection, selection, aggregation, grouping, and encryption/decryption.

In contrast to the abovementioned approaches, we present a completely new approach where we transparently transform data from rows to columns with the help of re-programmable logic. Our approach does not require to copy additional data, has minimal runtime overhead, and shows promising performance.

### 8 CONCLUSION AND FUTURE WORK

In this paper, we present a radically new approach to offer access to both row-oriented and columnar layouts. We build on recent developments in reprogrammable hardware to implement logic between the memory and the processor, which is able to on-the-fly convert rows to arbitrary groups of columns. Our approach, named Relational Memory pushes projection from software to hardware and allows the same software implementation to have native access to both row-oriented and column-oriented data layouts.

Our prototype implementation demonstrates this functionality and offers access to arbitrary groups of columns at no additional latency than accessing directly the optimal data layout. This groundbreaking result opens a new avenue for software/hardware co-design of data systems since it allows a single code path to have access to the desired data layout for each query.

Overall, Relational Memory is the first step to a new class of data systems architectures, as implementing projection in hardware lays the groundwork for other relational operators (selection, aggregation, group by, join pre-processing). Finally, the low-end hardware used in our prototype underlines that it is feasible to integrate this logic in memory controllers widening its impact.
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