Fast matrix multiplication for binary and ternary CNNs on ARM CPU

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Abstract—Low-bit quantized neural networks (QNNs) are of great interest in practical applications because they significantly reduce the consumption of both memory and computational resources. Binary neural networks (BNNs) are memory and computationally efficient as they require only one bit per weight and activation and can be computed using Boolean logic and bit count operations. QNNs with ternary weights and activations (TNNs) and binary weights and ternary activations (TBNs) aim to improve recognition quality compared to BNNs while preserving low bit-width. However, their efficient implementation is usually considered on ASICs and FPGAs, limiting their applicability in real-life tasks. At the same time, one of the areas where efficient recognition is most in demand is recognition on mobile devices using their CPUs. However, there are no known fast implementations of TBNs and TNN, only the daBNN library for BNNs inference. In this paper, we propose novel fast algorithms of ternary, ternary-binary, and binary matrix multiplication for mobile devices with ARM architecture. In our algorithms, ternary weights are represented using 2-bit encoding and binary - using one bit. It allows us to replace matrix multiplication with Boolean logic operations that can be computed on 128-bits simultaneously, using ARM NEON SIMD extension. The matrix multiplication results are accumulated in 16-bit integer registers. We also use special reordering of values in left and right matrices. All that allows us to efficiently compute a matrix product while minimizing the number of loads and stores compared to the algorithm from daBNN. Our algorithms can be used to implement inference of convolutional and fully connected layers of TNNs, TBNs, and BNNs. We evaluate them experimentally on ARM Cortex-A73 CPU and compare their inference speed to efficient implementations of full-precision, 8-bit, and 4-bit quantized matrix multiplications. Our experiment shows our implementations of ternary and ternary-binary matrix multiplications to have almost the same inference time, and they are 3.6 times faster than full-precision, 2.5 times faster than 8-bit quantized, and 1.4 times faster than 4-bit quantized matrix multiplication but 2.9 slower than binary matrix multiplication.

I. INTRODUCTION

Convolutional neural networks (CNNs) are the primary tool for solving various computer vision problems: pattern recognition [1], detection of different objects [2], [3], semantic segmentation [4] and many others. Although new transformer-based [5], [6] or deep MLP-based [7], [8] neural networks sometimes outperform CNNs on challenging datasets, they are usually harder to train, have more parameters and require more computational resources for inference [8], [9]. That is why CNNs remain irreplaceable in practical applications.

The high performance of CNNs is essential for on-device intelligence systems, which allows for solving computer vision problems directly on a mobile device without the transmission of information to an external server and thus solve them faster, as well as in a more energy-efficient and secure way [10].

The most computationally-challenging operation in a CNN is a discrete convolution of a feature map with a convolution kernel. A widely used approach for its efficient computation is a general matrix multiplication-based (GeMM-based) approach. Using this approach, the feature map and the convolution kernel are unrolled to matrices and then multiplied with the help of optimized BLAS libraries [11]. The most common method for transforming a feature map to a matrix is the im2col method. Unfortunately, it suffers from significant memory overhead, which is why several more resource-efficient methods were proposed [12], [13].

It is worth mentioning that efficient algorithms for discrete convolution are not limited to GeMM-based. For example, FPGAs, ASICs, and sometimes GPUs can benefit from the reduction of the number of multiplications using Winograd’s minimal filtering algorithms [14] but also can use more straightforward algorithms [15]. At the same time, on CPUs it is critical to optimize data flow in memory, so that the number of cache misses is low and data-parallel execution with Single Instruction Multiple Data (SIMD) instructions is possible. That can be achieved with the help of just-in-time code generation of direct convolution for specific kernel sizes [16]. However, all mentioned algorithms are specific to devices and/or convolution parameters, so GeMM-based algorithms are still widely used in practice.

One of the most efficient ways to speedup and reduce the memory footprint of a CNN is to replace floating-point values of weights and activations with integers. This process is called quantization, and a neural network with integer weights is referred to as quantized neural network (QNN) [10]. Widely used 8-bit quantization allows for a 4-times reduction of network size and significant speedup on mobile CPUs while maintaining the quality close to full precision models [17]. 4-bit QNNs demonstrate a noticeable drop in recognition quality on challenging tasks [18], [19]; still, 4-bit quantization can be used to accelerate CPU inference of small CNNs significantly [20]. The most memory-efficient quantization is
binarization: in binary QNNs (BNNs), weights and activations only take the values of 1 or −1 and require a single bit for storage. In BNNs, convolutions and matrix multiplications can be computed using only XOR/XNOR and bit count operations [21]. That makes such networks exceptionally computationally efficient, especially on FPGAs and ASICs. There is also a CPU implementation of BNNs available in daBNN library [22].

Although training techniques for binary networks have improved in the past few years [23], [24], they still show a significant gap in accuracy in comparison with full-precision ones. Ternary neural networks (TNNs) allow weights and activations take the values 1, 0 or −1 [25]. They show higher quality than BNNs and can be efficiently implemented on ASICS and FPGAs [26], [27]. Ternary-binary networks (TBNs), which have ternary activations and binary weights, take medium place between TNNs and BNNs in terms of computational complexity and show almost the same recognition quality as TNNs [28]. However, no computationally-efficient CPU-oriented algorithms of ternary and ternary-binary convolution and/or matrix multiplications were previously published to the best of our knowledge.

In this paper, we propose novel algorithms for high-performance matrix multiplication of binary, ternary, and ternary-binary matrices for CPUs with ARMv8 architecture. They can be used in convolutional and fully-connected (linear) layers of BNNs, TNNs, and TBNs to obtain computationally efficient inference of such networks on mobile devices. Our algorithms use binary logic operations instead of multiplications and accumulate their products in 16-bit integer values. It allows us to take full advantage of data-parallel computing with the help of SIMD extension NEON of ARM CPUs.

In the experimental section of our work, we compare the performance of the proposed algorithms to computationally-efficient algorithms of matrix multiplication for different data types: 32-bit floating-point, 8-bit integer from Google’s gemm-lowop library [29], 4-bit presented in [20], and binary from daBNN library [22].

II. EFFICIENT MATRIX MULTIPLICATION ON CPUs

A. High-performance GeMM

In this section, we discuss commonly used high-performance matrix multiplication computation methods. We use $A$ to denote left matrix of size $m \times k$, $B$ to denote right matrix of size $k \times n$ and $C = AB$ to denote their product. We refer to $m$, $n$ and $k$ as “height”, “width” and “depth” of matrix multiplication respectively. $X_{ij}$ denotes element of $X$ in row $i$ and column $j$.

Most modern machine-learning and linear algebra libraries implement matrix multiplication in the following way: they split the matrix $A$ along rows, the matrix $B$ along columns, and possibly both along the depth, then they use a high-performance function called “inner-kernel” or “microkernel” to compute small block of matrix $C$. Actually, there are several ways in which matrices $A$, $B$, and $C$ could be split as described in detail in [30]. One of them is presented as Algorithm 1. Here matrix $A$ is first split by blocks of $m_{blk}$ rows, values in those blocks are reordered by function PackNRowsA so that small blocks of its rows can be easily processed by microkernel, the result is stored in $A_{buf}$. Likewise matrix $B$ is split by blocks of $n_{blk}$ columns, reordered by PackNColsB and stored into $B_{buf}$. After that algorithm extracts smaller blocks: $m_{mk}$ rows and $k_{eff} \leq k_{blk}$ columns from $A_{buf}$, and $n_{mk}$ columns and $k_{eff}$ rows from $B_{buf}$. Those blocks are multiplied by the microkernel. Values of $m_{mk}$ and $n_{mk}$ as well as the storage order of values in buffers $A_{buf}$ and $B_{buf}$ depend on the microkernel implementation. Values of $k_{blk}$, $m_{blk}$ and $n_{blk}$ are independent of the microkernel. They are chosen so that reordered buffers fit into the L2 CPU cache and smaller buffers that microkernel processes fit into the L1 cache. This way, the number of cache misses is minimized, so multiplication computes faster.

Input: $m$, $n$, $k$ – height, width, depth;
$A$ – left matrix $m \times k$;
$B$ – right matrix $k \times n$;
Output: $C$ – matrix $m \times n$, $C = AB$

for $y \leftarrow 0$; $y < m$; $y \leftarrow y + m_{mk}$ do

for $d \leftarrow 0$; $d < k$; $d \leftarrow d + k_{blk}$ do

for $c \leftarrow 0$; $c < n_{eff}$; $c \leftarrow c + n_{mk}$ do

for $r \leftarrow 0$; $r < e_{eff}$; $r \leftarrow r + m_{mk}$ do

$C[j; j + m_{mk} - 1]\left[r; i + n_{mk} - 1]\leftarrow$ microkernel

$A_{buf} \left[r; r + m_{mk} - 1]$,

$B_{buf} \left[c; c + n_{mk} - 1], k_{eff}$

end

end

Algorithm 1: General high-level GeMM algorithm

If we consider neural network inference, the matrix $B$ is a weights matrix. It is usually small enough to fit into the L2 cache. Also, it does not change during inference of the neural network, so one can reorder it and store it in the PackedB buffer beforehand. Taking it into consideration, we use a little simpler algorithm to compute convolutions (Algorithm 2). In our version of the algorithm, buffer $A_{buf}$ is noticeably smaller: it contains only $m_{mk}$ rows and $k_{eff} \leq k_{blk}$ columns from the matrix $A$. That can help the inference on mobile devices where memory is limited.

In Algorithms 1 and 2 height and width ($n$ and $m$) are assumed to be multiples of microkernel height and width ($m_{mk}$ and $n_{mk}$) respectively. In practice, several microkernels of different shapes are implemented to compute multiplications on matrices of arbitrary shapes. Most computations are performed with a bigger microkernel, and smaller microkernels compute the remains.
Input: m, n, k – height, width, depth;
A – left matrix m \times k;
PackedB – pre-reordered right matrix k \times n;
Output: C – resulting matrix m \times n, C = AB
for d \leftarrow 0; d < k; d \leftarrow d + k_{blk} do
\begin{align}
k_{eff} & \leftarrow \min(k_{blk}, k - d) \\
for r \leftarrow 0; r < m; r \leftarrow r + m_{mk} do
\quad A_{buf}[0 : m_{mk} - 1] & \leftarrow \text{PackNRowsA}(A, r, m_{mk}) \\
\quad for c \leftarrow 0; c < n; c \leftarrow c + n_{mk} do
\quad \quad C[r : r + m_{mk} - 1][c : c + n_{mk} - 1] & \leftarrow \\
\quad \quad \text{microkernel}(\tilde{A}_{buf}, \text{PackedB}[c : c + n_{mk} - 1], k_{eff})
\end{align}
end

Algorithm 2: Our high-level GeMM algorithm

The values m_{mk} and n_{mk} should be chosen as high as possible to minimize the number of loads and stores from memory but low enough so that the result of matrix multiplication can be stored in CPU registers. This way, in the inner loop, the microkernel loads values from Ablock and Bblock, multiplies them, and accumulates results in registers. After whole multiplication is computed, the results are offloaded to memory. So, the shape of the microkernel depends on the number of registers available on specific CPU architecture and bit-width of values used in computation (the smaller it is, the more values can be stored in a single register). For example, AArch64 (ARMv8) CPUs have 32 128-bit SIMD registers.

B. Integer GeMM

Now let us point out key differences between floating-point matrix multiplication in CNNs and integer matrix multiplication in QNNs. The first is that CNNs just multiply matrices. On ARM CPUs multiplication microkernel can use FMLA instruction that for 3 SIMD registers a, b and c (each holding four 32-bit floating-point values) computes \text{FMLA}(a, b, c) = a + bc element-wise.

In QNNs, integer computations are used to approximate floating-point computations of CNNs. That can be done through linear quantization – the procedure in which all floating-point values of a neural network layer weights or activation are approximated with integers according to:

\[ \hat{x} = \max \left( \min \left( \frac{x}{s}, z \right)Q, 0 \right), \]

where Q is a maximal quantized value, s is a floating-point value called “scale” and 0 \leq z < Q is an integer value called “zero-point” (\(0 = z\)). \lfloor y \rceil denotes integer part of y. For n-bit quantization Q = 2^n – 1. Strategies to obtain scale and zero-point can vary [29], [19], [18].

Let us consider \( \tilde{A} \) to be a quantized approximation of matrix A with scale \( s_A \) and zero-point \( z_A \). We use similar notation for \( \tilde{B}, B, s_B, \) and \( z_B \). Then matrix multiplication can be approximated as:

\[ C_{ij} = \sum_{t=1}^{k} A_{it}B_{tj} \approx \sum_{t=1}^{k} s_A(\tilde{A}_{it} - z_A)s_B(\tilde{B}_{tj} - z_B) = \]

\[ = s_A s_B \sum_{t=1}^{k} (\tilde{A}_{it} - z_A)(\tilde{B}_{tj} - z_B) = s_A s_B \tilde{C}_{ij}, \]

where \( \tilde{C}_{ij} \) can be computed using integer-only arithmetic. In gemmlowp [29] and [20] it is done with the following transformation:

\[ \tilde{C}_{ij} = \sum_{t=1}^{k} (\tilde{A}_{it} - z_A)(\tilde{B}_{tj} - z_B) = \sum_{t=1}^{k} (\tilde{A}_{it}\tilde{B}_{tj} - z_B) \]

\[ = \sum_{t=1}^{k} \tilde{A}_{it} \tilde{B}_{tj} + kz_Az_B. \]

The first term of (3) presents matrix multiplication of quantized matrices: 8-bit with 32-bit product in case of gemmlowp and 4-bit with 16-bit product in case of [20]. The second and third terms do not depend on j and i respectively, so they are easier to compute: in terms of algorithmic complexity, the first term requires \( O(mnk) \), the second – \( O(nmk) \), the third – \( O(nk) \), and the fourth – \( O(1) \) operations.

It is worth mentioning that integer accumulators can overflow, which limits the depth of matrix multiplication. If matrices A and B hold p-bit values, and their product is accumulated in q-bit accumulators, then maximum depth that guarantees the absence of overflow is:

\[ k_{max} = \left\lfloor \frac{(2^q - 1)}{2^p - 1} \right\rfloor. \]

In GeMM-based convolution it limits the number of channels in the input feature map [20]. Let us consider convolution with \( H_k \times W_k \) kernel. Then the maximum number of channels in the input feature map, for which the absence of overflow in guaranteed is:

\[ C_{in-max} = \left\lfloor \frac{k_{max}}{H_kW_k} \right\rfloor. \]

III. LOW-BIT MATRIX MULTIPLICATION

In this section we present our algorithms for matrix multiplication of binary, ternary and ternary-binary matrices.

We consider matrix multiplication \( A \times B = C \) for three cases:

- **BNN** A and B are binary (\( A_{ij} \in \{-1, 1\}, B_{ij} \in \{-1, 1\} \)).
- **TNN** A and B are ternary (\( A_{ij} \in \{-1, 0, 1\}, B_{ij} \in \{-1, 0, 1\} \)).
- **TBN** \( A \) is ternary and \( B \) is binary (\( A_{ij} \in \{-1, 0, 1\}, B_{ij} \in \{-1, 1\} \)).

For all the cases we assume that \( C \) holds integer values stored in signed 16-bit representation.
A. Values, encoding and multiplication

In the considered algorithms values of matrix elements of A and B are either binary or ternary. For binary values we use single-bit encoding \( x \rightarrow x^b : 1 \rightarrow 0, -1 \rightarrow 1 \). This way matrix multiplication \( z = xy \) can be computed using our representation as \( z^b = x^b \oplus y^b \) (where \( \oplus \) is an addition modulo 2 or XOR operation). Using this representation we can compute matrix multiplication using only XOR, bit-count and addition operation in the inner loop:

\[
c = \sum_{i=1}^{k} a_i b_i = \sum_{i=1}^{k} (1 - 2a_i^b \oplus b_i^b) = k - 2 \sum_{i=1}^{k} (a_i^b \oplus b_i^b). \tag{6}
\]

For ternary values we use 2-bit encoding \( x \rightarrow (x^+, x^-) \): 
1 \rightarrow (1, 0), 0 \rightarrow (0, 0), -1 \rightarrow (0, 1), and code (1, 1) is invalid. Using those operations we can compute ternary multiplication \( z = xy \) as

\[
(z^+, z^-) = ((x^+ \land y^+) \lor (x^- \land y^-), (x^+ \land y^-) \lor (x^- \land y^+))
\]

and ternary-binary multiplication as

\[
(z^+, z^-) = ((x^+ \lor y^+) \land (x^- \lor y^-), (x^+ \lor y^-) \land (x^- \lor y^+)),
\]

where \( \land, \lor, \text{and } \oplus \) denote logical AND, OR, and NOT. Truth tables for ternary and ternary-binary multiplication illustrating these equations are presented in Table I.

### Table I

| x | y | z | x^+ | x^- | y^+ | y^- | z^+ | z^- | u^+ | u^- |
|---|---|---|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 1 | 1 | 1   | 0   | 1   | 0   | 0   | 0   | 1   | 0   |
| 1 | -1| -1| 1   | 0   | 0   | 1   | 0   | 1   | 0   | 1   |
| 0 | 1 | 0 | 0   | 0   | 1   | 0   | 0   | 0   | 0   | 0   |
| 0 | 0 | 0 | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   |
| 0 | -1| -1| 0   | 0   | 1   | 1   | 0   | 0   | 0   | 0   |
| -1| 1 | 1 | 0   | 0   | 1   | 0   | 0   | 1   | 0   | 1   |
| -1| 0 | 0 | 0   | 1   | 0   | -   | 0   | 0   | -   | 0   |
| -1| -1| -1| 0   | 1   | 0   | 1   | 1   | 0   | 1   | 0   |

Assuming that \( a_i b_i = (c^+, c^-) \) is a ternary or ternary-binary multiplication of a couple of elements as shown above, we can compute dot product (and matrix multiplication) as:

\[
c = \sum_{i=1}^{k} a_i b_i = \sum_{i=1}^{k} ((a_i b_i)^+ - (a_i b_i)^-). \tag{7}
\]

B. Binary microkernel

Now that we have encoding and operation definitions for matrix multiplication based on binary-logic operations available in the ARM instruction set, we move to matrix multiplication microkernels. As we stated in Section II-A microkernel multiplies \( m_{nk} \) rows stored in buffer Ablock by \( n_{mk} \) cols stored in buffer Bblock. To describe a multiplication microkernel we need to specify its shape \( m_{nk} \times n_{mk} \), storage order in buffers Ablock and Bblock and operations used in the computation. All the microkernels we propose in this work have \( 16 \times 8 \) shape and use 16 128-bit SIMD registers \((C00, \ldots, C07, C10, \ldots, C17)\) to hold the corresponding block of matrix C as 16-bit integers. However, storage order and SIMD instructions are different for all multiplications (BNN, TNN and TBN). Let us start with binary matrix multiplication.

To pack values into Ablock we

1) take 16 rows of A matrix encoded as binary values and pack them into 8-bit values (each holding 8 consecutive bits from the corresponding row);
2) store this 8-bit matrix in column-major order (first go 8 bits from the 1st row, then 8 bits from the 2nd and so on until the 16th, after that bits 9...16 from the 1st row, then bits 9...16 from the 2nd and so on).

To pack values into Bblock we

1) take 8 columns of B matrix encoded as binary values and pack them into 8-bit values (each holding 8 consecutive bits from the corresponding column);
2) store this 8-bit matrix in row-major order (first 8 bits from the 1st column, then 8 bits from the 2nd and so on until the 8th, after that bits 9...16 from the 1st column, than bits 9...16 from the 2nd and so on).

In one iteration of the loop over depth dimension in the microkernel (shown in Fig. 1) we

1) load a column of 8-bit values from Ablock into two 128-bit registers \( a \);
2) load a row 8-bit values from Bblock into one 64-bit register \( b \);
3) for each 8-bit element of \( b \) compute XOR (EOR instruction in ARM) with register \( a \), count number of 1-bites in the “product” with CNT instruction and accumulate the result with SADDW instruction.

C. Ternary microkernel

As described in Section III-A we use 2-bit representation for ternary values. To pack them into Ablock we

1) consider that \( A^+ \) and \( A^- \) are stored as two separate matrices;
2) take 8 rows of \( A^+ \) matrix and pack them into 8-bit values (each holding 8 consecutive bits from the corresponding row);
3) do the same for $A^-;$
4) store the first 8 8-bit elements from the first column of
$A^{+}$ block, then store the first 8 8-bit elements from the
first column of $A^{-}$ block, then the last 8 elements from
the first columns from $A^{+}$ and $A^{-}$ blocks, then repeat
this for the $2^{nd}$, the $3^{rd}$ and all the remaining columns.

To pack values into $B^{block}$ we
1) consider tat $B^{+}$ and $B^{-}$ are stored as two separate
matrices;
2) take 8 columns of $B^{+}$ matrix and pack them into 8-
bit values (each holding 8 consecutive bits from the
 corresponding column);
3) do the same for $B^{-}$;
4) for the first row: store the $1^{st}$ element from $B^{+}$ block,
then store the $1^{st}$ element from $B^{-}$ block, then the $2^{nd}$
elements and so on; repeat that procedure for all rows.

On each iteration ternary microkernel loads a column from
the $A^{block}$ as two 128-bit registers ($a^{0}$ and $a^{1}$) and a row
from $B^{block}$ as a single 128-bit register $b$. For each pair of
elements in $b$ it computes the product with registers $a^{0}$ and $a^{1}$
using AND and OR operations, then applies bit-count CNT to
compute sums of “+” and “-” bits of the product, computes
difference with SSUBL and accumulates the result in the
 corresponding register with ADD. Fig 2 demonstrates a half
of this microkernel – 8 rows from $A^{block}$.

\[ \begin{array}{c|c|c}
\hline
& A^{block} & B^{block} \\
\hline
& a^{0} & b \\
\hline
& a^{1} & b_{0} & \ldots & b_{7} & b_{0} \\
\hline
\end{array} \]

\[ \begin{array}{c|c|c|c}
\hline
& a_{0} & a_{1} & C_{00} & C_{01} \\
\hline
& a_{2} & \ldots & C_{10} & C_{11} \\
\hline
& a_{7} & \ldots & C_{70} & C_{71} \\
\hline
\end{array} \]

Fig. 2. Ternary GeMM microkernel.

D. Ternary-binary microkernel

For ternary-binary multiplication we store values ternary
in $A^{block}$ in the same way as for ternary multiplication
and binary values in $B^{block}$ in the same way as for binary
multiplication.

This way multiplication this microkernel is almost the same
as ternary with only two differences:

- $B^{block}$ contains 8 column of 8-bit values, so we use
  64-bit register $b$ to load them;
- as we show in Section III-A, different instructions (OR,
  AND and ORN – OR with negation of the second
  operand) are used to compute the product.

IV. MATRIX MULTIPLICATION EVALUATION

In this section, we demonstrate the efficiency of the pro-
posed ternary (TNN), ternary-binary (TBN), and binary (BNN)
matrix multiplication on ARM Aarch64 CPUs and compare
them to known efficient algorithms: binary from daBNN
library [22] (daBNN), 8-bit from gemmlowp library [29] (U8),
4-bit from [20] with a microkernel upscaled to $24 \times 8$ size
(U4, the original size was $24 \times 4$ for ARMv7 architecture),
and our implementation of floating-point 32-bit baseline which
uses the same register layout as gemmlowp, but computes
operations in floating-point (F32).

A. Theoretical evaluation

In Table II we show a comparison of the microkernels for
multiplication algorithms under consideration. We compare
them by a number of columns in $A^{block}$ ($m$), a number
of rows in $B^{block}$ ($n$), a step over depth per iteration ($k$),
a number of computational instructions per iteration ($COM$
– FMLA for F32 algorithm, UMLAL/UMLAL2 for U8,
etc.), a number of loads of SIMD register per microkernel
instruction ($LD$), a number of other SIMD instructions per
iteration ($MOV$ – MOV, DUP, INS, etc.), and by a number
of SIMD instructions per microkernel element $INS = (COM +$
$LD + MOV)/nmk$). We also estimate a maximum depth of
multiplication ($k_{max}$) as (4) for U8 and U4 algorithms. In a
ternary and binary matrix multiplication $xy = z$, $|z| \leq 1$, so
$k_{max}$ equals to the maximum possible value that a register
can hold. TNN, TBN, and BNN use 16-bit signed registers,
and $k_{max} = 2^{15} - 1$. daBNN uses 32-bit floating point
registers (with 23-bit significand field) to store $C^{block}$, so
$k_{max} = 2^{23} - 1$.

A multiplication algorithm reaches maximal efficiency when
multiplication parameters height, width, and depth are multi-
plies of corresponding microkernel parameters ($m, n, k$). It lim-
its the applicability of the multiplication algorithm in CNNs.
If a convolution is computed using im2col transformation, the
height is the number of pixels in the input feature map; the
width is the number of filters (from only a few in upper layers
of small CNNs to hundreds and thousands in lower layers

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of big CNNs). \( k_{\text{max}} \) limits the number of input channels in the feature maps (5). Taking all the limitations into account, we can see that U4 algorithm is only suitable for small CNNs, daBNN, on the other hand, will show better results in large networks, and all the rest (including three proposed algorithms) will work fine in small, medium and large CNNs.

### B. Experimental Evaluation

Although the number of instructions (COM, LD, MOV, and INS in Table II) can give us general ideas on which algorithm should have better computational efficiency, in practice the efficiency also depends on cache misses (which in turn depends on the order of loads and stores in memory), the ability of CPU to use the instruction pipelining (that depends on the order in which instructions are fetched). Furthermore, the overall efficiency of the matrix multiplication is affected also by reordering operations that prepare matrix blocks for microkernel and by post-processing in algorithms U8 and U4, which is shown in (3). That is why we experimentally measure the efficiency of all the algorithms under consideration.

We implemented matrix multiplication algorithms F32, U4, TNN, TBN, TNN according to Algorithm 2. All the microkernels were written on ARMv8 assembly to optimize the usage of SIMD registers. We ran time measurements for different values of height \((H \in \{72, 120, 240, 360\})\), width \((W \in \{24, 48, 72, 96\})\) and depth \((D \in \{128, 256, 384, 512\})\). Those values are chosen to be multiples of the microkernel size for each algorithm, so that they all can show the maximum efficiency. They also are representative for matrix multiplications in small and medium CNNs, which can be used in real-life tasks on mobile CPUs.

We ran our experiment on the ARM Cortex-A73 CPU, a part of Odroid-N2 development board with Linux. For each value of parameters, we took the median of 5 measurements (to exclude random errors) and repeated the whole experiment 50 times, taking the average of the measurements to reach 0.8% empirical relative error of running time. We summarize them in Table III. Each cell compares algorithms \( A \) and \( B \) as \( \mathbb{E}_\theta(T_B(\theta)/T_A(\theta)) \), where \( T_A \) and \( T_B \) denote execution times of corresponding on test \( \theta \), \( \mathbb{E} \) is mathematical expectation.

According to Table III our TNN algorithm significantly outperforms matrix multiplication for types with greater bit-width: it is 3.6 faster than F32, 2.5 times faster than U8 and 1.4 times faster than U4. TBN is only slightly faster than TNN because of a simpler data flow in \( B_{\text{block}} \). BNN is almost 3 times faster than TNN (and 2.9 times faster than TBN. Moreover our implementation of binary multiplication turns out to be 1.15 times faster than that of daBNN library, due to a bigger microkernel and 16-bit representation of the result.

Proposed algorithms for ternary, ternary-binary, and binary matrix multiplication show significantly higher computational efficiency than algorithms with greater bit-width. They can be used for the inference of low-bit CNNs on mobile devices and do not pose strict constraints on the network architecture (although to achieve maximal efficiency, numbers of channels in feature maps and convolutional filters should be multiples of 8). It opens an opportunity to investigate the trade-off between recognition quality (which usually decreases along with the bit-width of QNN) and efficiency gain from low-bit quantization of several layers or whole CNNs. Note that in the pursuit of high computational efficiency, different libraries for network inference usually implement direct convolution algorithms for the most common shape of convolution kernels that do not rely on matrix multiplication. For example, daBNN library implements \( 3 \times 3 \) binary convolution directly. Our ideas of encoding and computation of ternary and binary dot products can be used in those algorithms as well.

### V. Conclusion

In this paper, we presented algorithms for matrix multiplication of ternary, ternary-binary, and binary matrices of ARM CPUs. Those algorithms are superior to existing CPU implementations of matrix multiplication. For example, ternary, ternary-binary, and binary multiplications are 3.6, 3.7, and 11 times faster, respectively, than floating-point multiplication. They have also shown good computational efficiency compared to 8-bit multiplication from Google’s gemmlowp library (ternary multiplication is 2.5 times faster) and binary multiplication from daBNN library (our binary algorithm is 1.15 faster).

Our algorithms can be used in the GeMM-based convolution implementations of CNNs over a wide range of parameters, which allows for computationally- and resource-efficient inference of low-bit CNNs on mobile devices.

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### Table II

| Algo | \( m \times n \times k \) | COM | LD | MOV | INS | \( k_{\text{max}} \) |
|------|----------------|-----|----|-----|-----|--------|
| F32  | \( 12 \times 8 \times 1 \) | 24  | 5  | 0   | 0.302| —      |
| U8   | \( 12 \times 8 \times 2 \) | 48  | 5  | 5   | 0.302| 66051 |
| U4   | \( 24 \times 8 \times 2 \) | 48  | 5  | 16  | 0.180| 291   |
| TNN  | \( 16 \times 8 \times 8 \) | 96  | 3  | 64  | 0.159| 32767 |
| TBN  | \( 16 \times 8 \times 8 \) | 96  | 3  | 56  | 0.151| 32767 |
| BNN  | \( 16 \times 8 \times 8 \) | 32  | 2  | 8   | 0.041| 32767 |
| daBNN| \( 8 \times 6 \times 128 \) | 156 | 12 | 36  | 0.033| 8388607|

### Table III

| B   | A     | F32 | U8 | U4 | TNN | TBN | BNN | daBNN |
|-----|-------|-----|----|----|-----|-----|-----|-------|
| F32 | 1.00  | 1.44| 2.52| 3.63| 3.75| 10.9| 9.60 |
| U8  | 0.69  | 1.00| 1.75| 2.51| 2.60| 7.52| 6.63 |
| U4  | 0.40  | 0.57| 1.00| 1.44| 1.49| 8.52| 5.81 |
| TNN | 0.28  | 0.40| 0.70| 1.00| 1.03| 2.99| 2.64 |
| TBN | 0.27  | 0.39| 0.67| 0.97| 1.00| 2.90| 2.55 |
| BNN | 0.093 | 0.13| 0.23| 0.34| 0.35| 1.00| 0.88 |
| daBNN| 0.11  | 0.15| 0.27| 0.39| 0.40| 1.15| 1.00 |
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