A Low Input Voltage Charge Pump for Energy Harvesting

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Abstract. This paper proposes a low input voltage charge pump using 0.18um CMOS process for energy harvesting. There are two main sections in the charge pump system: Low Voltage Charge Pump (LVCP) and High Voltage Charge Pump (HVCP). In the LVCP, a negative charge pump is utilized to improve the efficiency at low input voltage, Dynamic Body Bias (DBB) and switch-conductance enhancement techniques are applied to a unit stage of the two-stage charge pump. In the HVCP, the charge pump circuit utilizes charger transfer switches (CTS) with a complementary banch scheme to significantly reduce undesired charge transfer, and an optimized gate control strategy is applied to further decrease the power loss caused by undesired charge transfer. The simulation result demonstrates that the proposed circuit can achieve 97% voltage conversion and drive 800uA load current at 0.6V input voltage. In the region of 0.4V to 0.6V input voltage, the circuit performs well with the load resistance of 10K ohms.

1. Introduction
As the development of the process technology, more and more portable devices come into people's lives. The increasing need for System on Chips (SoCs) for Internet-of-Things (IoT) platforms demands a smaller form factor, low power, low cost, and minimum maintenance. Alongside reducing the power consumption, energy harvesting has been proposed as a possible solution to increase the lifetime, reducing maintenance, and cost especially for IoT. However, energy harvesting source cannot be used directly due to the fluctuation of the voltage and power levels, which is determined by the source availability. Hence, an efficient power management unit (PMU) is needed to manage the energy from the source, store it, and deliver it to the load. The low-voltage up-converter has two types of main elements that transfer energy from the input to the output: an inductive type and a capacitive type. Compared with traditional inductor-based buck-boost or transformer-based converters, charge pumps benefit from the significantly higher energy density of capacitors, making them especially suitable for chip-level power conversions [1,2].

A whole charge pump system with low input voltage is proposed in this paper using 0.18um CMOS process. The simplified block diagram of the designed topology is shown in Figure 1. The system includes two parts: Start up and Boost. In the first part, low input voltage charge pump (LVCP) utilizes a new threshold reduction technology for converting low input voltage to high voltage. In the second part, a complementary branch scheme and an optimized gate strategy are utilized in high input voltage charge pump (HVCP). The rest of the paper is structured as follow. Section 2 describes the structure and circuit of each part, and then analyses the principle of the threshold reduction technology in LVCP, reverse current suppression technology in HVCP. The simulation results are demonstrated in the section 3. Section 4 concludes this paper.
2. Circuits of Proposed Charge Pump and Analysis of Each Part

The block diagram of the proposed charge pump system is depicted in Figure 1. The Start-Up module consists of an oscillator, charge pump unit with DBB and conductance enhancer. There are an oscillator and charge pump with auxiliary transistors in the Boost module.

2.1. LVCP

In the system of energy harvesting, the output voltage of the energy harvester is usually 0.4V~0.6V, so a low voltage start-up circuit is needed to drive the post-stage circuit. In this design, threshold reduction technology, DBB, is used in the LVCP to turn the CTSs on and the conductance enhancement technology is also utilized to improve the power conversion efficiency (PCE). The block diagram of the LVCP is depicted in Figure 2. LVCP consists of two Unit CP, a clock generator without overlap and Gm_Enhancer.

A Unit CP consists of a voltage doubler, a dual-series PMOS switch, and four switches for DBB as shown in Figure 3. As detailed schematic shown, a voltage doubler, which includes a cross-coupled NMOS pair (MN1 and MN2) in a deep n-well and two pumping capacitors (CP1 and CP2), allows CT and CTB to swing between Vin and Vo. Vin is the input voltage and Vo is the output voltage of the unit CP, respectively. Vout is the output voltage of the LVCP which is the highest voltage to avoid PN junction of the PMOS for ward bias. The clock cannot be directly connected to the body of the cross-coupled NMOS pair because they are overlapped signals. Figure 4 shows the schematic of the clock without overlap and the control signals to drive the pumping capacitor and turn the CTSs on or off.

When CLK is low and CLKB is high, CT is about Vin and CTB is about 2Vin. So MN1 is turned on to charge the pumping capacitor CP1, and MN2 is turned off, and then the pumping capacitor CP2 deliver charge to the load through the MP2. At this time, the control signal E is high and EB is low to ensure MP1 is off and MP2 is on. Due to the low voltage Vin (0.4V-0.6V), it is hard to turn the NMOS
on completely. So DBB technology is used to lower the threshold of NMOS. When MN1 is on and MN2 is off, E is high and EB is low. Then MS1 and MS4 are turned on and MS2 and MS3 are turned off, the body of MN1 is connected to Vo and the body of MN2 is connected to ground. In the contrary, during the period that the CLK is high and CLKB is low, E is low and EB is high. At this half period, VCT is approximately 2Vin and VCTB is belike Vin. Now MN2 turns on and MN1 turns off, moreover, auxiliary transistor MS2 and MS3 are on, MS1 and MS4 are off. Due to the MS2 and MS3, the body of MN1 and MN2 is set to ground and Vo, respectively. It can be inferred from the above process that substrate of on-state CTS is connected to high level voltage, and substrate of off-state CTS is set to ground. For the high efficiency, and low leakage current, all CTS at on-state should be in the forward mode for high on-current, while CTS at off-state have to be in the reverse mode for low leakage current.

According to the formula of threshold voltage,

\[ V_{TH} = V_{TH0} + \gamma \sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F} \]  \hspace{1cm} (1)

we can find that the threshold of the MOSFET \( V_{TH} \) is proportional to the voltage difference between the source and substrate \( (V_{SB}) \). In the equation (1), \( V_{TH0} \) is the threshold voltage without considering the body effect, \( \gamma \) is the body effect coefficient, \( \Phi_F = (kT/q) \ln \left( \frac{N_{sub}}{n_i} \right) \). It’s easy to conclude that threshold voltage can be reduced when the source to substrate voltage is negative. Therefore, the CTS in LVCP can work in the condition of low input voltage to start the post-stage circuit. Combined with the formula of the equivalent resistance of MOSFET working in triode region,

\[ R_{on} = \frac{1}{\mu \cdot C_{ox} \cdot \frac{W}{L} (V_{GS} - V_{TH})} \] \hspace{1cm} (2)

As \( V_{TH} \) reduces, the equivalent resistance of MOSFET falls so that power consumption of the CTS decreases.

Figure 4 shows schematic of the dead-time circuit. The dead-time circuit consists of two cross-coupled latches. To minimize delay overhead, at low input voltage, the parasitic capacitor of inverters and wire routing within the dead-time circuit should be minimized. Figure 5 depicts the detailed schematic of Gm_Enhancer [3]. In fact, it’s a combination of a negative charge pump, two NMOS doublers and two switches. The two-phase negative charge pump used to boost \( V_{GS} \) of the series switches allows E and EB to be driven down to -Vin. Two auxiliary voltage doublers supplied by the control signals C1/C2 and L1/L2 allow E and EB to turn off the series PMOS switches completely. Above all, the output signal of Gm_Enhancer can swing between -Vin and Vout.
2.2. HVCP
The detailed schematic of HVCP is depicted in Figure 6. A complementary branch scheme is applied based on the CTS charge pump technology. Undesired charge transfer caused by simultaneous conduction of auxiliary transistors is eliminated with their gate control signals generated in both complementary branches [4]. As we can see from Figure 6, this charge pump circuit consists of two complementary branches. These two branches are identical circuits with complementary clocks and are connected in parallel between the supply voltage and output. PMOS transistors are used as CTSs except for the first stage, which has the advantage that the body effect can be easily eliminated by connecting the substrate to high voltage side. A simple two-phase clocking is applied, the clock signals \( \Phi_1 \) and \( \Phi_2 \) are both out-of-phase and have a voltage identical to VDD. The gate driving signal for each transistor is internally generated by both Branch A and Branch B. The detailed operation is explained as follow.

In the first stage, only one NMOS transistor is used for each branch. For the transistor MA1, when \( \Phi_1 \) is low and \( \Phi_2 \) is high, the voltage at node A1 (V\(_{A1}\)) is close to but less than VDD, while V\(_{B1}\), which is generated in Branch B, is about 2VDD. As a result, MA1 is turned on effectively by a gate-source voltage of VDD enabling charge to be pushed from the supply voltage to capacitor CA1. Instead of the threshold voltage drop of the NMOS-based Dickson charge pump, the voltage drop across MA1 is V\(_{DS}\), which is much less than the threshold voltage. During another half of period, V\(_{A1}\) goes up to 2VDD while V\(_{B1}\) drops to VDD, turning off MA1 to cut off the path from node A1 back to the power supply. On the other hand, transistor MB1 operates in an opposite and complementary way.

In the middle stage, during the time interval T1, both V\(_{B1}\) and V\(_{B2}\) are about 2VDD with V\(_{B1}\) slightly higher than V\(_{B2}\). V\(_{A1}\) and V\(_{A2}\), which are generated in Branch A, are approximately VDD and 3VDD, respectively. As a result, auxiliary pass transistor MNB2 is turned on with a gate-source voltage of VDD and MPA3 is turned off by the gate-source voltage of -VDD. The ON state of MNB2 leads to the gate terminal of MB2 connected to node B1 (V\(_{B1}\) is about VDD), which turns on MB2 with a gate drive voltage of VDD, allowing charge transfer from capacitor CA1 to capacitor CA3. During time interval T2, auxiliary pass transistor MPB2 is turned on while MNB2 is turned off. The MB2 is turned off since its gate and source terminals are connected together through MPB2, cutting off the path from node B2 to B1. On the other hand, Branch A operates in a complementary manner. Specifically, MA2 is turned on during the time interval T1, allowing charge transfer from node A1 to A2, and is turned off during the time interval T2 cutting off the path from node A2 to A1.

The output stage features a similar operating principle to the first stage. Instead of NMOS transistors, one PMOS transistor is utilized for each branch. CTS MAout is turned on and MBout is turned off in one phase, and MAout is turned off and MBout is turned on in another phase. The ON state of MAout enables charge transfer from capacitor CA2 to output capacitor Cout. Similarly, charge can be delivered from CB2 to Cout when MBout is on. In this way, charge is delivered to the output during both the charge and discharge phase, which effectively reduces output voltage ripples.

3. Simulation Results
The proposed charge pump is fabricated in 0.18um standard CMOS process. To compare with the performance of the traditional charge pump, the simulation of LVCP, HVCP and all circuits are performed as follow.

Figure 7 depicts the output voltage of LVCP and HVCP in different load with different input voltage. For the LVCP, in order to achieve the enough driving capability, the capacitance of the pumping capacitors CP1 and CP2 is chosen as 10 nF, and the capacitance of the pumping capacitor CN1 and CN2 in Gm_enhancer is 60pF for stronger capability to drive large CTS. What’s more, the frequency of the oscillator is about 1MHz for enough time to charge and discharge the pumping capacitor due to the low input voltage causing the MOSFET working in the subthreshold region. According to Figure 7. (a), the input voltage ranges from 0.4V to 0.6V and the load resistance varies from 500 ohms to 10K ohms. The output voltage reaches 1.196V and 1.79V with the load resistance of 10K ohms at 0.4V and 0.6V input.
Figure 7. Simulated output voltage versus input voltage (a) LVCP and (b) HVCP in different load voltage, respectively. With the decrease of load resistance, the output voltage is reduced because of the increased load current. At the load resistance of 1K ohms, the output voltage still remains over 1V (1.1V) with 0.48V input voltage. For the HVCP, the capacitance of the pumping capacitor is 1 nF and the frequency of the oscillator is about 2M due to the high input voltage which comes from LVCP. As depicted in Figure 7. (b), at the load resistance of 1K, the output voltage can still reach 3.84V with 1.8V input voltage. When the load resistance is 10K ohms, the HVCP works better to generate high output voltage (6.29V with 1.8V input voltage).

Figure 8. Simulated output voltage of the proposed circuit in different load with different input voltage

The relationship between the output voltage and input voltage under different load resistance varied from 2k to 50k is shown in Figure 8. The output voltage of the top circuit, at 0.4V input voltage, can reach 3.56V without load and the LVCP output voltage is 0.92V due to the power consumption of the oscillator of HVCP, and the voltage conversion is about 97%. According to the Figure 8, when the load resistance is 2K ohms and the output current is 400uA to 800uA, the system still can work in the region of 0.5V to 0.6V input voltage. What’s more, the output voltage reaches 6.052V and 2.611V at the 0.4V and 0.6V input voltage, respectively, with 50K ohms load resistance. The maximum output current that the system can drive is approximately 800uA at 0.6V input voltage with the load resistance of 2K ohms.

The comparison results of the proposed charge pump and Ref(5), Ref(6),Ref(7) are demonstrated in Table 1. According to the table, the proposed charge pump can supply higher voltage than Ref(5) and Ref(6) at input voltage lower than threshold voltage. The peak load current reaches up to 800uA higher than the Ref(5), and the input voltage gets down to 0.4V lower than Ref(7). Moreover, the voltage conversion is about 97% higher than Ref(5) and Ref(6) and lower than Ref(7).
Table 1 performance comparison

| Parameter              | [5]  | [6]  | [7]  | This work |
|------------------------|------|------|------|-----------|
| Year                   | 2013 | 2015 | 2018 | 2020      |
| Process (um)           | 0.35 | 0.18 | 0.18 | 0.18      |
| Clock Freq (Hz)        | 7M   | 12.8K| 10M  | 1M        |
| Input Voltage          | 0.9V-2.5V | 0.25V-0.6V | 1V-1.2V | 0.4V-0.6V |
| Vout @ Vin=0.9V        | 3.4V | 0.3V | 4V   | 3.56V     |
| @ Vin=0.25V            |      |      |      |           |
| Vout @ Vin=1V          |      |      |      |           |
| Voltage Conversion     | 76%  | 83%  | 99%  | 97%       |
| Peak Load Current      | 120μA| N    | N    | 800μA     |
| Pumping Capacitor      | 20pF | 10nF/1nF | 10pF | 10nF/1nF  |

4. Conclusion

A charge pump using 0.18um CMOS process for low input voltage energy harvesting is proposed in this paper. DBB and Gm_enhancement technologies are utilized in LVCP converting the low input voltage to high voltage above the threshold voltage of MOSFET. The HVCP circuit consists of a complementary branch scheme and an optimized gate control strategy. The simulation results demonstrate that the proposed charge pump can achieve the converting from 0.4V-0.6V input voltage into high voltages and the voltage conversion can reach up to 97%. What’s more, it can also drive up to 800μA load current.

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