Monotone Circuits

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Abstract— Maximal monotonicity is explored as a generalization of the linear theory of passivity, which allows for algorithmic system analysis of an important physical property. The theory is developed for nonlinear 1-port circuits, modelled as port interconnections of the four fundamental elements: resistors, capacitors, inductors and memristors. An algorithm for computing the steady state periodic behavior of such a circuit is presented.

I. INTRODUCTION

Passivity is the backbone of linear circuit theory. As a system theoretic concept, it provides a fundamental bridge between physics and computation, well beyond electrical circuits. Passive linear systems are those that can be realized as port interconnections of passive elements\cite{1}, and the KYP lemma provides an algorithmic framework for the analysis of passive circuits by convex optimization\cite{2}–\cite{4}. The circuit concept of passivity has generated amongst the most important developments of control theory over the several last decades, including dissipativity theory\cite{5}, \cite{6}, nonlinear passivity theory\cite{7}–\cite{9}, and passivity based control\cite{10}–\cite{13}.

This paper explores the concept of maximal monotonicity as a generalization of the LTI theory of passivity that retains the fundamental bridge between physics and computation beyond the world of linear, time-invariant systems.

This is a most classical proposal, as the very concept of maximal monotonicity emerged in the study of nonlinear resistors. The prototype of a maximally monotone circuit element was the quasi-linear resistor studied by Duffin\cite{14}; this was later generalized to maximally monotone relations by Minty\cite{15}–\cite{18} and Desoer and Wu\cite{19}, again in the study of networks of nonlinear resistors.

The research journeys of maximal monotonicity and nonlinear circuit theory have somewhat drifted apart over the last 40 years. Following the influential paper of Rockafellar\cite{20}, on the proximal algorithm for finding the zero of a maximal monotone relation, maximal monotonicity has become central to convex optimization\cite{21}–\cite{25}. This line of research exploits the algorithmic significance of maximal monotonicity, but has progressively become detached from its physical significance. On the other hand, recent years have witnessed a surge of interest in the physical significance of memristive nonlinear circuits\cite{26}–\cite{52}, but with little emphasis on algorithms and system analysis.

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The operator-theoretic property of maximal monotonicity can be interpreted, when defined on an appropriate space, as the incremental form of cyclo-passivity\cite{33}. It coincides with passivity only in the linear world. Like passivity, maximal monotonicity is retained through interconnection: port interconnections of monotone circuits are monotone. But maximal monotonicity is much more than passivity because, unlike passivity, it comes with a convex algorithmic theory, even in the nonlinear world. Maximal monotonicity has been a central property in the study of nonsmooth dynamical systems\cite{34}, and early connections between passive systems and maximal monotone operators appear in this work - in particular in the study of Lur’e systems with maximal monotone nonlinearities\cite{35}, \cite{36}. The algorithmic significance of maximal monotonicity has gained a lot of momentum in the recent years because of the renewed interest for first-order methods in large scale and nonsmooth convex optimization\cite{24}.

The main contribution of this paper is to reunite the algorithmic framework of maximal monotonicity with nonlinear circuit analysis. A preliminary version of this work has been submitted for presentation at ECC2021\cite{37}. We consider nonlinear circuits obtained as port interconnections of the four fundamental 1-port circuit elements: the resistor, the inductor, the capacitor, and the memristor. LTI circuits may be analysed efficiently by means of their transfer functions, and the harmonic response of such a system is readily computed. The corresponding problem for a nonlinear circuit can, in general, only be solved approximately. We propose a method for steady state periodic analysis of monotone nonlinear 1-ports using fixed point iterations. The approach firstly provides guaranteed convergence in signal space to the true solution at a given rate, and secondly provides a strong link between the algorithmic steps and the physical structure of the circuit. Existing solution methods fall into two classes: methods to perform a transient simulation, and wait for convergence to a periodic solution\cite{38}–\cite{40}, and harmonic analysis\cite{41}. The transient simulation method proposed by Heemels, Sessa, Vasca, \textit{et al.}\cite{42} makes use of maximal monotonicity in the context of passive, nonsmooth state space systems, rather than the input/output circuits considered here.

The remainder of this paper is organized as follows. In Section\ref{sec:2} we motivate our work with a simple example. In Section\ref{sec:3} we develop the circuit modelling methodology of this paper. In Section\ref{sec:4} we introduce the property of monotonicity, and several stronger properties. Section\ref{sec:5} develops a computational technique to compute the periodic output of a periodically driven monotone 1-port circuit, and gives several examples. In Section\ref{sec:6} we discuss the generalization of monotonicity from 1-port circuits to systems, and make
connections with passivity and cyclo-passivity. We conclude in Section VII with some open questions for future research.

II. Motivating Example

We begin with a simple example, which motivates the developments of this paper: the series interconnection of two resistors (see Figure 1).

![Series Interconnection of Two Resistors](image)

Consider first the linear, time invariant case, \( v_j = R_j i_j \). The series interconnection maps the applied current \( i \) to the port voltage \( v \) by the relation \( v = R_1 i + R_2 i \). The inverse relation maps voltage \( v \) to current \( i \) by \( i = v/(R_1 + R_2) \). A parallel connection is dual: voltage and current are exchanged, and resistance is replaced by its reciprocal, conductance.

The fundamentals of the circuit remain unchanged if the resistors are each replaced by a linear passive transfer function. Indeed, the series interconnection of two passive 1-ports remains passive, and the inverse of a passive transfer function is again passive.

If we replace the linear resistors by nonlinear, but passive resistors, however, several attractive properties of the resistors are lost. A passive resistor can have regions of negative slope in its \( i-v \) curve (Chua, Yu, and Yu [3] give a catalogue of physical examples). The inverse of such a resistor may not be well defined. If, however, we consider monotone nonlinear resistors, the fundamentals of the LTI case remain unchanged. Monotonicity of a resistor means its \( i-v \) curve is nondecreasing; most importantly, invertibility of the interconnection is retained. This is illustrated in Figure 2.

![i-v Curves of a Passive and Monotone Resistor](image)

III. Fundamental Elements and Their Interconnections

A. Relations

We begin by introducing some mathematical preliminaries.

**Definition 1.** A relation on a space \( X \) is a subset \( S \subseteq X \times X \).

For example, a resistor defines a relation on \( \mathbb{R} \):

\[
S_{\text{resistor}} = \{ (i, v) \in \mathbb{R} \times \mathbb{R} \mid v = R_i \}.
\]

In this case, the relation describes a linear function. In general, however, a relation may be set-valued. We write \( v \in S(i) \) to denote \( (i, v) \in S \). The domain and range of a relation \( S \) is denoted by \( \text{dom} S \). The interior of a set \( X \) is denoted by \( \text{int} X \).

The usual operations on functions can be extended to relations:

\[
S^{-1} = \{ (y, u) \mid y \in S(u) \}
\]

\[
S + R = \{ (x, y + z) \mid (x, y) \in S, (x, z) \in R \}
\]

\[
SR = \{ (x, z) \mid \exists y \text{ s.t. } (x, y) \in R, (y, z) \in S \}.
\]

B. 1-port Elements

A 1-port is an electrical device with two external terminals. Two variables may be measured across these terminals - the port voltage \( v \) and the magnetic flux linkage \( \phi \). Two variables may be measured through these terminals - the port current \( i \) and the charge \( q \). We assume each of these variables takes values in \( \mathbb{R} \).

\[\phi \text{ and } v \text{ are related by Faraday’s law of induction:} \]

\[
\frac{d}{dt} \phi = v,
\]

(1)

Similarly, \( i \) and \( q \) are related by

\[
\frac{d}{dt} q = i.
\]

(2)

A 1-port \( S \) is defined by a relation between port voltage and port current. For the purposes of modelling, we take \( v \) and \( i \) to belong to the space of continuously differentiable functions from the time axis \( \mathbb{R} \) to \( \mathbb{R} \), which we denote by \( C^1 \). The forward direction of the relation may be from voltage to current (voltage controlled), or from current to voltage (current controlled).

There are four fundamental elements: resistors (commonly denoted \( R \)), capacitors (\( C \)), inductors (\( L \)) and memristors (\( M \)). Each of these is defined by a relation on \( \mathbb{R} \) between one of \( i, q \) and one of \( v, \phi \), as shown in Figure 3. The relation may be defined in either direction. By applying this relation at each time \( t \), we obtain a relation on \( C^1 \). If \( \phi \) or \( q \) is involved, then the algebraic relationship is composed with one or both of the fundamental laws (1) and (2) to give a relation between \( i \) and \( v \).

![The Four Fundamental Elements](image)

Resistors, capacitors and inductors are familiar from basic circuit theory. The existence of the memristor (a contraction of “memory resistor”) was postulated by Chua [44], who argued...
by symmetry that there should be a fourth fundamental element relating charge and flux. The device is absent from linear theory, as in the linear case, a memristor is simply a resistor. The memristor remained hypothetical until 2008, when it was identified in a physical device by researchers at HP Labs [26]. The fundamental status of the memristor, however, has remained contentious [45]. Since the 2008 discovery, interest in the memristor has surged, primarily due to its potential in neuromorphic computers and analog neural networks [27], [29]–[32]. We note that the invention of the memristor by Chua [44] follows the first paper of monotone circuits [16] by a decade, but that, to the best of the authors’ knowledge, all the system-theoretic investigations of the memristor have focused on passivity rather than monotonicity, although Theorem 1 of Chua [44] can be interpreted as showing that monotonicity is equivalent to passivity for a memristor.

C. Series and parallel interconnections

The study of circuits modelled as 1-ports is classical, dating back to work by Bott and Duffin [11], Foster [46], and Brune [47], and others. In the spirit of this classical work, and of the “tearing, zooming and linking” modelling methodology advocated by Willems [48], we will model general 1-port networks by building them as series and parallel interconnections of the four fundamental elements.

Series and parallel interconnections are illustrated in Figure 4.

![Fig. 4. Series (left) and parallel (right) interconnections of two 1-ports.](image1)

For a parallel interconnection, the composition of Kirchhoff’s laws and the device laws of each 1-port create a natural forward relation from voltage to current, as follows.
1) KVL: \( v = v_1 = v_2 \)
2) Device: \((v_1, i_1) \in G_1, (v_2, i_2) \in G_2\)
3) KCL: \( i_1 + i_2 = i \).
This is illustrated in Figure 5.

For a series interconnection, the roles of current and voltage are reversed. The natural forward relation is from current to voltage, as follows.
1) KCL: \( i = i_1 = i_2 \)
2) Device: \((i_1, v_1) \in R_1, (i_2, v_2) \in R_2\)
3) KVL: \( v_1 + v_2 = v \).
This is illustrated in Figure 6.

![Fig. 5. Block diagram of parallel interconnection, illustrating parallel forward relation from current to voltage.](image2)

![Fig. 6. Block diagram of series interconnection, illustrating parallel forward relation from voltage to current.](image3)

Constructing 1-ports: The class of 1-ports we consider in this paper are those that may be constructed in the following way.

Take an ordered set of \( n \) fundamental elements, represented by the relations \( E_i, i \in \{1, \ldots, n\} \). Denote by \( d(E_i) \in \{i \to v, v \to i\} \) the direction of the relation \( E_i \), either current to voltage (current-controlled) or voltage to current (voltage controlled). We drop the superscript when the direction of the relation is immaterial. The construction has \( n \) steps. Let \( j \in \{1, \ldots, n\} \) denote the step number. In step \( j = 1 \), we initialise the relation \( M_1 \) to be \( E_1 \). For each of the steps \( j = 2, \ldots, n \), we perform the following.

\[
M_j \leftarrow \begin{cases} 
M_{j-1} + E_j, & d(E_{j-1}) = d(E_j) \\
M_{j-1} + E_j, & d(E_{j-1}) \neq d(E_j).
\end{cases}
\]

The final 1-port is \( M := M_n \). It’s forward direction is \( d(E_n) \).

In this construction, we use the direction of relation \( E_i \) to decide whether it is connected in series or parallel. If \( E_i \) maps current to voltage, it is connected in series. If it maps voltage to current, it is connected in parallel. Note that building a 1-port from the series and parallel interconnection of 1-port elements involves iteratively applying the operations of inversion and addition.

We make the following assumption on series and parallel interconnections.

**Assumption 1. Series:** any 1-port formed by the series interconnection of 1-ports with **current to voltage relations** \( R_1 \) and \( R_2 \) obeys
\[
\text{int dom } R_1 \cap \text{dom } R_2 \neq \emptyset
\]
or
\[
\text{int dom } R_2 \cap \text{dom } R_1 \neq \emptyset.
\]

**Parallel:** any 1-port formed by the series interconnection of 1-ports with **voltage to current relations** \( G_1 \) and \( G_2 \) obeys
\[
\text{int dom } G_1 \cap \text{dom } G_2 \neq \emptyset
\]
or
\[
\text{int dom } G_2 \cap \text{dom } G_1 \neq \emptyset.
\]
This assumption is sufficient (but not necessary) for the existence of solutions to the interconnection (that is, the resulting relation between \(i\) and \(v\) is nonempty).

IV. MONOTONE 1-PORTS

A. Monotonicity

The property of monotonicity connects the physical property of energy dissipation in a device to algorithmic analysis methods. Let \(H\) be a Hilbert space with inner product \(\langle \cdot, \cdot \rangle\) and norm \(\| \cdot \|\). Monotonicity on \(H\) is defined as follows.

Definition 2. A relation \(R \subseteq H \times H\) is called monotone if
\[
\langle u - v, y - w \rangle \geq 0
\]
for all \(y \in R(u)\) and \(w \in R(v)\).

Monotonicity is preserved under a number of operations. The proof of the following lemma may be found in [22].

Lemma 1. Consider monotone relations \(G\) and \(F\). Then
1) \(G^{-1}\) is monotone;
2) \(GF\) is monotone;
3) \(G + F\) is monotone;
4) \(\alpha G\) is monotone for \(\alpha > 0\);
5) \(C(x, y) = \{ (u, v) \mid u \in G(x), v \in F(y) \}\) is monotone.
6) If \(F\) is monotone on a space of dimension \(s\), and \(M \in \mathbb{R}^{s \times t}\), then the relation given by
\[
G(x) = M^\top F(Mx)
\]
is also monotone.

B. Monotone 1-ports

An element is monotone if it defines a monotone relation between \(i\) and \(v\) (or, equivalently, between \(v\) and \(i\)). In the remainder of this paper, we examine 1-port circuits built by interconnecting monotone fundamental elements in series and parallel. Such 1-ports are always monotone.

Theorem 1. Any 1-port formed by the parallel and series interconnection of monotone fundamental elements on a Hilbert space \(H\) of scalar signals is monotone on \(H\).

Proof. We show that Kirchoff’s laws preserve monotonicity. This follows from taking \(M = (1, 1)^\top\) in Lemma 1 property 6 and noting that the inverse of a monotone relation is monotone (Lemma 1 property 1). It follows that parallel and series interconnections of monotone relations between \(i\) and \(v\) are themselves monotone relations between \(i\) and \(v\).

Note that, since \(G^{-1}\) is monotone for monotone \(G\), a negative feedback interconnection of monotone components is monotone, as it can be represented as \((G^{-1} + K)^{-1}\). This can be viewed as a generalisation of the fundamental theorem of passivity.

We now turn our attention to periodic signals. A trajectory \(w\) is said to be \(T\)-periodic if \(w(t) = w(t + T)\), for all \(t\). We consider the Hilbert space of finite energy, \(T\)-periodic, continuous signals, restricted to a single period, with values in \(\mathbb{R}\). Let \(T > 0\) be arbitrary. Denote this space by \(L_{2,T}\), and note that for all \(w(t) \in L_{2,T}\), \(w(0) = w(T)\). Define the usual inner product \(\langle x, y \rangle := \int_0^T x(t)y(t) \, dt\) and norm \(\|x\|^2 := \langle x, x \rangle\). The following lemma shows that the monotonicity of a fundamental element on \(L_{2,T}\) is captured by the monotonicity of its device law, defined on \(\mathbb{R}\).

Lemma 2. A fundamental element is monotone on \(L_{2,T}\) if its device law is monotone on \(\mathbb{R}\).

Proof. The proof has two parts. First, we show that a memoryless relation on \(L_{2,T}\) (that is, a relation where \(y(t)\) depends only on \(u(t)\)) is monotone if it is monotone on \(\mathbb{R}\). Indeed, by monotonicity on \(\mathbb{R}\), we have
\[
\langle u_1(t) - u_2(t), y_1(t) - y_2(t) \rangle \geq 0 \quad \text{for all } t,
\]
from which it follows that
\[
\langle u_1 - u_2, y_1 - y_2 \rangle = \int_0^T \langle u_1(t) - u_2(t), y_1(t) - y_2(t) \rangle \, dt \geq 0.
\]

This proves the lemma for resistors, and proves that capacitors, inductors and memristors are monotone on \(L_{2,T}\) from \(q\) to \(v\), \(i\) to \(\phi\) and \(q\) to \(\phi\), respectively. It remains to show that the integral and derivative are monotone. It is well known that the integral and derivative are passive linear systems. Passivity implies operator positivity on \(L_{2,T}\) [49]. Linearity implies that this is equivalent to monotonicity (see §VI-A). The result then follow from Lemma 1 part 2.

C. Stronger properties

Strongly monotone and Lipschitz relations: Here we introduce some additional properties a relation may have. These properties are referred to in the next section, as requirements for convergence of some algorithms.

Definition 3. A relation \(S\) has a Lipschitz constant of \(L > 0\) if, for all \((u, w), (v, y) \in S\),
\[
\|u - v\| \leq L\|w - y\|.
\]
If \(L < 1\), \(S\) is called a contraction. If \(L = 1\), \(S\) is called nonexpansive.

Definition 4. A relation \(S\) on \(X\) is said to be averaged if there exists a \(\vartheta \in (0, 1)\) such that \(S = (1 - \vartheta)I + \vartheta G\), where \(I\) is the identity relation and \(G\) is some nonexpansive relation.

Definition 5. A relation \(S\) is \(\alpha\)-coercive or strongly monotone with parameter \(\beta > 0\) if, for all \((u, w), (v, y) \in S\),
\[
\langle u - v, w - y \rangle \geq \alpha\|u - v\|^2.
\]

Definition 6. A relation \(S\) is \(\alpha\)-cocoercive if, for all \((u, w), (v, y) \in S\),
\[
\langle u - v, w - y \rangle \geq \alpha\|w - y\|^2.
\]

It is seen immediately that \(F\) is \(\alpha\)-coercive if and only if \(F^{-1}\) is \(1/\alpha\)-cocoercive. It also follows from the Cauchy-Schwarz inequality that \(F\) has a Lipschitz constant of \(1/\alpha\) if \(F\) is \(\alpha\)-cocoercive. Finally, if \(A\) is \(\alpha\)-coercive (resp. \(\alpha\)-cocoercive) and \(B\) is monotone, \(A + B\) is is \(\alpha\)-coercive (resp. \(\alpha\)-cocoercive). For more details on these properties, we refer the reader to [22 §2.2].
Maximal monotone relations: An important property in computational applications is maximality. Maximality is required for convergence and well-posedness of many fixed point algorithms, including those introduced in the next section. This is the significance of the Minty surjectivity theorem [50].

Definition 7. A monotone relation $S$ is called maximal monotone if there is no monotone relation which properly contains it.

In general, maximality is not preserved when two relations are added (indeed, the graph of their sum may be empty). However, by [51] Thm. 1, it follows from Assumption 1 that maximality is preserved for the interconnections considered in this paper.

V. ALGORITHMIC STEADY-STATE ANALYSIS OF MONOTONE CIRCUITS

In this section, we demonstrate the algorithmic tractability of monotone 1-ports by considering the problem of computing the periodic output of a 1-port, given a periodic input. Precisely, the problem is as follows.

Problem statement
Consider a monotone 1-port circuit represented by a relation $R$. Assume, without loss of generality, that $R$ maps from $i$ to $v$. Suppose that $v$ is now an arbitrary periodic signal, $v^*$. Find a corresponding periodic input $i^*$ such that $(i^*, v^*) \in R$.

General solution method
Define the relation $\Delta R$ by $\Delta R(i) = R(i) - v^*$. Then any $i$ which solves $0 \in \Delta R(i)$ is a possible solution $i^*$. The problem $0 \in \Delta R(i)$ is solved using a fixed point iteration.

In the first part of this paper, we considered the modelling of circuits using monotone elements, which is most naturally treated using continuous signals. Here, we consider algorithmic questions, for which discrete signals are the natural domain. We restrict the variables $v, i, q$ and $\phi$ to be discrete, finite real valued signals $w = \ldots, w_0, w_1, \ldots$, where $w_k \in \mathbb{R}$, which are $N$-periodic: $w_k = w_{k+N}$ for all $k$. As the signal information is captured by a single period, we restrict the signals to a single period. We denote this space by $l_2, N$ (the discrete counterpart of $L_2, T$). This space may be identified with $\mathbb{R}^N$, with the additional constraint that, for all $w \in l_2, N$, $w_0 = w_{N-1}$.

We define the derivative on this space to be the backwards finite difference. Due to the periodicity of $q$ and $\phi$ signals, the backwards finite difference has the finite representation

$$ D = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & -1 \\ -1 & 1 & 0 & \cdots & 0 & 0 \\ 0 & -1 & 1 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & -1 & 1 \end{bmatrix}. $$

If a circuit also includes integrators (for example, capacitors mapping current to voltage), then, in order to have a finite dimensional representation of the integral, we must further restrict signals to $i$ and $v$ with zero mean,

$$ \sum_j v_j = 0, $$

$$ \sum_j i_j = 0, $$

and to zero offset $q$ and $\phi$: $q_{N-1} = 0$, $\phi_{N-1} = 0$.

Under these additional conditions, the derivative is given by the relation

$$ D = \left\{ (u, y) \mid y_T = ND_T u_T, \\ y_{N-1} = N \sum_{k=0}^{N-2} y_k = -Nu_{N-2}, u_{N-1} = 0 \right\}, $$

where $x_T$ denotes the truncation of the signal $x$ to the first $N-1$ components, $x_T = \{x_0, x_1, \ldots, x_{N-2}\}$, and $D_T$ is the $N-1 \times N-1$ matrix

$$ D_T = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 0 \\ -1 & 1 & 0 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & -1 & 1 \end{bmatrix}. $$

The inverse relation $J := D^{-1}$, which replaces the integral, is given by

$$ J = \left\{ (u, y) \mid y_T = \frac{1}{N} J_T u_T, u_{N-1} = N \sum_{k=0}^{N-2} u_k, y_{N-1} = 0 \right\}, $$

where $J_T$ is the $N-1 \times N-1$ Riemann sum:

$$ J_T = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 0 \\ 1 & 1 & 0 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 1 & 1 & 1 & \cdots & 0 & 1 \end{bmatrix}. $$

A. Fixed point algorithms

In this section, we briefly introduce the algorithms which will be used in the examples that follow. Rather than provide an exhaustive treatment of these methods, we provide only the necessary details, and refer the interested reader to the introductory papers [23], [24], [52], [53], and the textbooks [22], [54].

A fixed point of a relation $F$ is a point $x$ such that $x \in F(x)$. The fixed point, or Picard, iteration, is given by the update rule

$$ x^{j+1} = F(x^j), $$

where superscripts denote iterations of the entire signal $x$, as opposed to subscripts, which denote a particular time instant of the signal. For several classes of relations $F$, this iteration will converge to a fixed point of $F$. This includes contractions (this is the Banach fixed point theorem [55]) and averaged relations [22, 2.4.2].

There are a number of ways in which $0 \in S(x)$ can be solved by finding a fixed point of a relation related to $S$, and we describe several below. Note that solving $0 \in S(x)$ for monotone $S$ is equivalent to inverting the offset operator $u \mapsto S(u) + u^*$. Note also that because monotonicity and related properties are defined between pairs of trajectories, $S(u) + u^*$ has the same monotonicity properties as $S(u)$. The basic operation needed to solve a general monotone 1-port is inversion of a relation of the form $y = S_1(u) + S_2(u)$. This is precisely the problem for which base splitting schemes have been developed. These schemes separate computation for the components $S_1$ and $S_2$. 


Below, we describe the most basic fixed point algorithm, the forward step, and two base splitting schemes - the forward/backward splitting and the Douglas-Rachford splitting.

**Forward step**: The forward step is suitable for solving a relation corresponding to a single 1-port, of the form \( y = S(u) \). It can be viewed as a generalization of gradient descent.

\[
0 \in S(x) \\
\iff 0 \in -\alpha S(x) + x - x \\
\iff x \in (I - \alpha S)(x).
\]

The fixed point iteration \( x_{j+1} = x_j - \alpha S(x_j) \) converges geometrically to the unique fixed point of \( I - \alpha S \) when \( S \) is strongly monotone with parameter \( m \) and Lipschitz with parameter \( L \), and \( \alpha \in (0, 2m/L^2) \). The optimal contraction factor of \( 1 - m^2/L^2 \) is given by \( \alpha = m/L \). In this case, \( I - \alpha S \) is a contraction mapping; existence and uniqueness of a fixed point follow from the Banach fixed point theorem. If \( S \) is merely \( \beta \)-cocoercive, then the forward step is averaged, and converges to a solution if one exists [22, §2.4.3].

**Forward/backward splitting**: The simplest base splitting scheme is the forward/backward splitting \([56]-[58]\).

\[
0 \in S_1(x) + S_2(x) \\
\iff 0 \in x - \alpha S_1(x) - (x + \alpha S_2(x)) \\
\iff (I + \alpha S_2)x \geq (I - \alpha S_1)x \\
\iff x = (I + \alpha S_2)^{-1}(I - \alpha S_1)x.
\]

The relation \((I + \alpha S_2)^{-1}\) is called the resolvent of \( S_2 \), denoted \( \text{res}_{S_2} \). The fixed point iteration \( x_{j+1} = \text{res}_{S_2}(x_j - \alpha S_1(x_j)) \) converges whenever \( S_2 \) is monotone and under the same conditions on \( S_1 \) as the forward step [22, §2.7.1].

**Douglas-Rachford splitting**: The Douglas-Rachford splitting algorithm \([59], [60]\), is a more sophisticated splitting algorithm, which converges if \( A \) and \( B \) are monotone [61]. The iteration for this algorithm is as follows:

\[
x_j^{k+1/2} = \text{res}_A(i^k) \\
\Rightarrow_j^{k+1/2} = 2x_j^{k+1/2} - i^k \\
x_j^{k+1} = \text{res}_B(z_j^{k+1/2}) \\
i^{k+1} = i^k + x_j^{k+1} - x^{k+1/2}.
\]

The Douglas-Rachford algorithm forms the basis of the Alternating Direction Method of Multipliers (see [62] and references therein), and is one of the most successful fixed point methods.

**B. Fourier analysis**

It follows from Parseval’s theorem that monotonicity of a relation is preserved under the Fourier transform. LTI operators have a diagonal Fourier transform, meaning that a fixed point iteration of an LTI operator in the frequency domain can be computed separately - computation for each frequency component can be done in parallel.

**C. Existence of periodic solutions**

We have presented algorithms for finding periodic solutions of periodically driven circuits, without guaranteeing such solutions exist. Here, we collect a few basic results which show that such periodic solutions do exist for large classes of monotone 1-ports. We begin by noting that for the fundamental elements and purely series or parallel circuits, periodic inputs map to periodic outputs, regardless of monotonicity of the elements, provided that signals which are integrated have zero mean.

**Proposition 1.**

- Resistors map \( T \)-periodic currents to \( T \)-periodic voltages, and \( T \)-periodic voltages to \( T \)-periodic currents.
- Capacitors map zero mean \( T \)-periodic currents to \( T \)-periodic voltages, and \( T \)-periodic voltages to \( T \)-periodic currents.
- Inductors map \( T \)-periodic currents to \( T \)-periodic voltages, and zero mean \( T \)-periodic voltages to \( T \)-periodic currents.
- Memristors map zero mean \( T \)-periodic currents to \( T \)-periodic voltages, and zero mean \( T \)-periodic voltages to \( T \)-periodic currents.

**Proof.** The property is clearly true for a memoryless relation, that is, a relation between \( u \) and \( y \) such that \( y(t) \in f(u(t)) \). Indeed, \( y(t + T) \in f(u(t + T)) = f(u(t)) \Rightarrow y(t) \). This includes resistors viewed as relations between \( i \) and \( v \), capacitors as relations between \( q \) and \( v \), inductors as relations between \( \phi \) and \( i \), and memristors as relations between \( \phi \) and \( q \).

The property also holds for the derivative, and for the integral when the signal has zero mean over a period. Indeed,

\[
\frac{du(t)}{dt} = \lim_{h \to 0} \frac{u(t) + u(t + h)}{h} = \lim_{h \to 0} \frac{u(t + T) + u(t + T + h)}{h} = \frac{du(t + T)}{dt},
\]

and

\[
\int_{-\infty}^{t} u(t) \, dt = \int_{-\infty}^{t-t \mod T} u(t) \, dt + \int_{t-t \mod T}^{t} u(t) \, dt = \int_{t-t \mod T}^{t} u(t) \, dt + \int_{t-t \mod T}^{t+T} u(t) \, dt.
\]

**Proposition 2.** A series (resp. parallel) interconnection of \( n \) 1-ports which map \( T \)-periodic currents (voltages) to \( T \)-periodic voltages (currents) also maps \( T \)-periodic currents (voltages) to \( T \)-periodic voltages (currents).

**Proof.** Periodicity is preserved under summation of signals, and therefore preserved by Kirchoff’s laws. Indeed, if \( y_j(t) = u_j^1(t) + u_j^2(t) \), and \( u_j^1 \) and \( u_j^2 \) are both \( N \)-periodic, then \( y_j(t + T) = u_j^1(t + T) + u_j^2(t + T) = u_j^1(t) + u_j^2(t) = y_j(t) \).

Next, we show that monotone RLC 1-ports map periodic inputs to periodic outputs, provided that any 1-port which
must be inverted during the construction is both coercive and cocoercive. A 1-port is coercive and cocoercive if, for example, it includes a resistor which is coercive and cocoercive. This is a resistor with the property that \( i \to \pm \infty \iff v \to \pm \infty \).

Other classes of systems with this property include contractive state space systems [63] and approximately finite memory input/output maps [64].

**Theorem 2.** Let \( G \) be the relation on \( L_{2,T} \), from either \( v \) to \( i \) or \( i \) to \( v \), of a 1-port constructed from \( n \) fundamental elements with relations \( E_i \), such that the construction obeys the following conditions

1. \( E_i \) is monotone for all \( i \);
2. \( \text{dom } E_i = L_{2,T} \) for all \( i \);
3. capacitors are interconnected in parallel (meaning the relation for each capacitor is from voltage to current);
4. inductors are interconnected in series (meaning the relation for each inductor is from current to voltage);
5. any 1-port which must be inverted during the construction is coercive and cocoercive;
6. inductors and capacitors have continuous device laws.

Then \( G \) maps any input in \( L_{2,T} \) to a unique \( T \)-periodic output in \( L_{2,T} \).

**Proof.** We begin by observing that continuity of inductors and capacitors guarantees consistency of the backwards finite difference discretization. For a capacitor, it follows from Taylor’s theorem that \( \Delta q(t)/\Delta t \to dq(t)/dt \) as \( \Delta t \to 0 \). From continuity of the capacitance \( q = C(v) \), it follows that \( (i(t),v(t)) = (i(t),v(t)) \) as \( \Delta t \to 0 \), where \( (i(t),v(t)) \) is a solution to the discretized 1-port and \( (i(t),v(t)) \) is a solution to the continuous 1-port. Suppose now that \( (i(t),v(t)) = (i(t+T),v(t+T)) \) for every \( \Delta t \). Then \( (i(t),v(t)) = (i(t+T),v(t+T)) \). It remains to show that the discretized 1-port maps \( T \)-periodic inputs to \( T \)-periodic outputs.

It follows from Proposition 1 that each of the relations \( E_i \) maps \( T \)-periodic inputs to \( T \)-periodic outputs (we denote this property by PIPO for the remainder of this proof). We show that constructing a circuit under the given conditions preserves this property. We first note that restricting to \( T \)-periodic inputs allows the elements to be represented as relations on \( l_{2,T} \). This requires conditions 3 and 4 which ensure that inputs to capacitors and inductors are differentiated, not integrated.

The derivative has a finite representation on \( l_{2,T} \). Following the algorithmic method we have presented, we take, for a given periodic \( y^* \), the incremental relation \( \Delta y = F(u) - y^* \). As \( F \) is a relation on \( l_{2,T} \) and \( y^* \) is periodic, \( \Delta F \) is also a relation on \( l_{2,T} \). Convergence of the forward step algorithm when \( F \) is strongly monotone and Lipschitz guarantees the existence and uniqueness of a zero to the incremental relation, by the Banach fixed point theorem [22 §2.4.2], [55]. Note also that periodicity is preserved at every iteration of the forward step. This shows that \( F \) is invertible on \( l_{2,T} \). Invertibility on \( L_{2,T} \) then follows from consistency of the discretization.

Finally, we note that conditions 2 and 3 may be relaxed by restricting the set of input signals so that no element has an input outside its domain, and no integrator has an input which has non-zero mean. Memristors may also be included under this condition. A special case is given by [37, Thm. 2].

**D. Alternative techniques**

Several methods have been proposed in the literature to analyse the response of a nonlinear circuit to a periodic input. These include harmonic balance (see, for example, Feldmann, Melville, and Long [41]), the shooting Newton method [38] and traditional numerical time-integration techniques [40]. Maximal monotonicity is a central property in the extensive work by Brogliato and coauthors on time-stepping techniques for the simulation of nonsmooth dynamical systems (see, for example, the monograph [39] and the recent review [34]). Also of note are the two time-stepping algorithms proposed by Heemels, Sessa, Vasca, et al. [42], for the computation of the periodic response of a periodically driven Lur’e system with passive linear part and maximally monotone, set valued nonlinearity. These algorithms rely on the fact that such Lur’e systems have contractive state transition mappings. The primary advantages of the techniques we propose here are the availability of a rigorous complexity theory, which gives bounds on the convergence rate to the periodic output solution, the scalability and parallelizability of the algorithms used and the large class of systems to which the method applies.

**E. Examples**

**Example 1: envelope detector:** An envelope detector is a simple nonlinear circuit consisting of a diode in series with an LTI RC filter (Figure 7). It is used to demodulate AM radio signals.

![Fig. 7. An envelope detector, configured as a 1-port.](image)

We model the diode using the Shockley equation:

\[ v = nV_T \ln \left( \frac{\Delta i + i^*}{I_s} + 1 \right), \]

where \( I_s \) is the reverse bias saturation current, \( V_T \) is the thermal voltage and \( n \) is the ideality factor.

The outermost interconnection in this circuit is the series interconnection of the diode and filter, hence the forward relation maps current to voltage:

\[ v = R_{\text{diode}}(i) + R_{\text{RC}}(i), \]
where \( R_{\text{diode}} \) is the current to voltage relation of the diode, and \( R_{RC} \) is the current to voltage map of the RC filter.

The RC filter is itself a parallel interconnection of a resistor and capacitor, hence its forward relation maps voltage to current:

\[
R_{RC} = G_{RC}^{-1}
\]

\[
i_{RC} = G_{RC}(v_{RC}).
\]

**Current to voltage simulation**

Computing the voltage given a current input involves applying the forward relation of the outer series interconnection. The voltage response is the sum of the diode voltage and the filter voltage. The diode voltage may be computed immediately by applying the diode relation \( R_{\text{diode}} \). To compute the filter voltage, we have to compute the filter inverse relation. This is done using the forward step algorithm:

\[
v_{RC}^{i+1} = v_{RC}^i - \alpha \Delta G_{RC}(v_{RC}^i).
\]

where \( \Delta G_{RC} \) is the forward relation of the RC circuit offset by the input current:

\[
\Delta G_{RC}(v_{RC}) = G_{RC}(v_{RC}) - i^*.
\]

\( G \) is the forward relation of the RC circuit, which encompasses the following steps:

- **KVL:** \[
\begin{bmatrix} v_C \\ v_R \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \end{bmatrix} v
\]
- **Devices:** \[
\begin{bmatrix} q_C \\ i_R \end{bmatrix} = \begin{bmatrix} CV_C \\ \frac{1}{R} v_R \end{bmatrix}
\]
- **Physical law:** \( i_C = D q_C \)
- **KCL:** \[
i = \begin{bmatrix} 1 & 1 \end{bmatrix} \begin{bmatrix} i_C \\ i_R \end{bmatrix}.
\]

These steps can be collapsed to a single linear operator:

\[
G = \frac{C}{N} D + \frac{1}{R} I.
\]

As \( \Delta G \) is affine, it has a Lipschitz constant \( L \) equal to its largest singular value and is coercive with constant \( m = \lambda_{\min}((A + A^T)/2). \) Hence the forward step converges geometrically for any choice of \( \alpha \in (0, 2m/L^2). \)

Figure 8 shows the results of performing this scheme with an input of \( i^* = 1 + \sin(2\pi t) \) A, with \( R = 1 \Omega, C = 1 \text{F}, I_s = 1 \times 10^{-14} \text{A}, n = 1 \) and \( V_T = 0.02585 \text{V}. \) The number of time steps used is 500.

**Voltage to current simulation**

The voltage to current simulation involves computing the inverse relation of the outer series interconnection.

The properties of the diode limit the available algorithms that one may apply. It is maximal monotone, but it neither Lipschitz nor strongly monotone, and its range is not the full space \( \mathbb{R}. \) Furthermore, the resolvent of the diode cannot be computed analytically. The diode relation is however fully separable in time, meaning the resolvent value at each time point can be computed in parallel.

The incremental voltage \( \Delta v = v - v^* \) is given as a relation of \( i \) by

\[
\Delta v = R_{\text{diode}}(i) + R_{RC}(i) - v^*.
\]

The split nature of the relation into diode and RC circuit parts suggests the use of a splitting algorithm. Here we apply the Douglas-Rachford splitting algorithm. This involves applying both the resolvents \( \text{res}_{RC} \) and \( \text{res}_{\text{diode}}. \)

The resolvent \( \text{res}_{RC} \) is given by \( (I + \lambda G_{RC}^{-1})^{-1}. \) This is computed as follows:

\[
y = \text{res}_{RC}(u) = (I + \lambda G_{RC}^{-1})^{-1} u
\]

\( (G_{RC} + \lambda I)y = u \)

This last line is solved using a general purpose linear system solver.

The resolvent of the diode, \( \text{res}_{\text{diode}}, \) is given by \( \text{res}^{-1}_{\text{diode}}(x) = (I + \lambda R_{\text{diode}}(x) - \lambda v^*). \) There is no analytic expression for this operator. Rather, the resolvent is computed numerically. A guarded Newton algorithm [23] is used to compute this resolvent.

Figure 8 shows the results of performing this scheme with an input of \( v^* = \sin(2\pi t) \) A, with \( R = 1 \Omega, C = 1 \text{F}, I_s = 1 \times 10^{-14} \text{A}, n = 1 \) and \( V_T = 0.02585 \text{V}. \) The number of time steps used is 500.

**Example 2: memristor crossbar array:** Conventional computer architectures have computational devices and memory devices located in separate areas. As processors have become faster, the transport delay between computation and memory has become a significant bottleneck in computer speed - the so-called von Neumann bottleneck. The ability of a memristor to both remember and compute allows the von Neumann bottleneck to be circumvented. Recent studies have shown neural networks are able to be implemented on crossbar arrays of solid state memristors [30], [65]-[67]. A crossbar array consists of \( n \) input lines and \( m \) output lines. Each input line is connected to every output line by a switch. In the case of a memristor crossbar array, the switches are solid state memristors. The memristors used in these arrays are able to have their resistance modified by the application of...
a DC current, and are able to be read without modifying their resistance by the application of an AC current.

The physical memristor model that we simulate here is that proposed by HP Labs [26]. The device consists of a single layer of a semiconductor material between two contacts. The semiconductor is partially doped with a positive charge carrier. The resistance of the doped region of the semiconductor is $R_{on}$, and the resistance of the undoped region is $R_{off}$. Letting $w(t)$ denote the coordinate of the boundary between doped and undoped regions, and $D$ denote the width of the semiconductor film, the resistance of the device is

$$R(q(t)) = R_{on} \frac{w(t)}{D} + R_{off} \left(1 - \frac{w(t)}{D}\right)$$

for $0 \leq w(t) \leq D$. As a current flows through the device, the dopant drifts in the direction of current flow, and the boundary $w(t)$ between the doped and undoped regions moves according to

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{on}}{D} q(t),$$

where $\mu_v$ is the average ion mobility. Integrating with respect to time, and setting $w = D/2$ when the charge $q = 0$, we have

$$w(t) = \mu_v \frac{R_{on}}{D} q(t) + \frac{D}{2}.$$

For $w(t)$ outside the range $[0, D]$, we treat the memristor as a linear resistor, with resistance $R_{on}$ for $w(t) \leq 0$, and resistance $R_{off}$, for $w(t) \geq D$. This causes the device to “remember” all the charge that has flowed through it, rather than saturated $w(t)$ becoming unsaturated as soon as the current reverses direction. More realistic models have been proposed (see, for example, Strukov, Snider, Stewart, et al. [26] and Biolek, Biolek, and Biolková [68]), which take the form of a memristive system [69]. The flux-controlled, or memductance, form of this model is given by the following equations, where we drop time dependence for notational convenience.

$$q = M(\phi) = \begin{cases} \frac{1}{2\sigma} \phi - \frac{1}{R_{on}} C_1 & \phi \leq \phi_l \\ \frac{1}{2\sigma} (b + \sqrt{(b^2 - 4ac)}) & \phi_l < \phi < \phi_u \\ \frac{1}{2\sigma} \phi - \frac{1}{R_{on}} C_2 & \phi \geq \phi_u, \end{cases}$$

where

$$\phi_l = \frac{D^2}{\mu_v R_{on}} \left(\frac{3}{8} R_{off} - \frac{1}{8} R_{on}\right)$$

$$\phi_u = \frac{D^2}{\mu_v R_{on}} \left(\frac{1}{4} R_{off} + \frac{1}{8} R_{on}\right)$$

$$a = (R_{on} - R_{off}) \frac{\mu_v R_{on}}{2 D^2}$$

$$b = (R_{on} + R_{off})/2$$

$$c = -\phi.$$

Here, we simulate the simplified situation where we consider only a single output, and $n = 10$ inputs are interconnected to a single sinusoidal source. This gives a 1-port circuit which is the parallel interconnection of 10 memristors. The voltage to current relation of this parallel interconnection is given by

$$i = \sum_{j=1}^{n} \Delta M_j v,$$

where the $\Delta M_j$ are the incremental memductances of the $n$ memristors. Integrating, and setting $q = 0$ when $\phi = 0$, we have

$$q = \sum_{j=1}^{n} M_j(\phi).$$

The memristors have device values which are normally distributed with a standard deviation of 2% about the following nominal values:

$$\mu_v = 10 \times 10^{-14} \text{m}^2 \text{s}^{-1} \text{V}^{-1}$$

$$D = 10 \times 10^{-9} \text{m}$$

$$R_{on} = 100 \Omega$$

$$R_{off} = 600 \Omega.$$

When viewed as a relation between $\phi$ and $q$, this array is Lipschitz with constant $\sum_j 1/R_{on}$ and coercive with constant $\sum_j 1/R_{off}$. We can therefore compute the current to voltage response using a forward step iteration in the $\phi$–$q$ domain. The $i$–$v$ response is calculated by integrating $i$ to obtain the input $q$ before the iterative scheme is applied, and differentiating the $\phi$ computed using the fixed point iteration, to obtain $v$. The Lissajou figure generated by an input current of $i = 9 \times 10^{-6} \sin(2\pi t) \text{A}$ is shown in Figure 10. This matches the characteristic Lissajou figure of a memristor, shown for example by Strukov, Snider, Stewart, et al. [26] and Chua and Kang [69].

**VI. MONOTONICITY AS A SYSTEM PROPERTY**

**A. Monotonicity and cyclo-passivity**

Monotonicity on the space of $T$-periodic signals, as introduced for the algorithmic techniques of this paper, is closely related to the classical notion of cyclo-passivity. Cyclo-passivity is a generalisation of passivity to storages that are
not necessarily bounded, allowing the inference of instability theorems. Cyclo-passivity was first introduced by Willems [33], and later developed by Hill and Moylan [70]. For recent work on cyclo-dissipativity of multi-ports, see van der Schaft [71] and van der Schaft and Jeltsema [72]. To the best of the authors’ knowledge, the incremental version of this property has never been studied. We define incremental cyclo-passivity as follows:

**Definition 8.** A relation \( R \) on \( \mathcal{H} \) is said to be incrementally cyclo-passive if, for all \( T \), and all \( (u, y), (v, w) \in R \) with the property that \( u(-T) = u(T) \) and \( v(-T) = v(T) \) (respectively for \( y \) and \( w \)),

\[
\langle u - v | y - w \rangle \geq 0.
\]

This corresponds to monotonicity on the space of all periodic trajectories of any period. The property required for the methods described in Section V, monotonicity on periodic signals with a particular period, is a weaker notion.

Monotonicity also relates to the classical input/output notions of passivity and positivity. These notions are developed on general signal spaces, which we briefly introduce as follows.

Let \( \mathcal{H} \) be a Hilbert space with inner product \( \langle \cdot | \cdot \rangle_{\mathcal{H}} \). Let \( T \subseteq \mathbb{R} \) be a time interval. Form the space \( \mathcal{F} \) by taking all functions from \( T \to \mathcal{H} \), where the norm and inner product are inherited from \( \mathcal{H} \) as follows:

\[
\langle x | y \rangle = \int_T \langle x(t) | y(t) \rangle_{\mathcal{H}} \, dt \quad \text{(continuous case)}
\]

\[
\langle x | y \rangle = \sum_{n \in \mathcal{T}} \langle x_n | y_n \rangle_{\mathcal{H}} \quad \text{(discrete case)}
\]

\[
\| x \| = \langle x | x \rangle.
\]

Define the Hilbert space \( \mathcal{G} \subseteq \mathcal{F} \) by

\[
\mathcal{G} := \{ x \in \mathcal{F} \mid \| x \| < \infty \}.
\]

Desoer and Vidyasagar [49] define the notion of positivity of a relation as follows.

**Definition 9.** A relation \( R \) on \( \mathcal{G} \) is positive if

\[
\langle x | y \rangle \geq 0
\]

for all \( x \in \mathcal{G} \) and all \( y \in R(x) \).

Monotonicity on \( \mathcal{G} \) (in the sense of Definition 2) is the incremental version of this type of positivity. Desoer and Vidyasagar [49] note that, for causal operators, positivity and passivity (which is defined on an extended signal space) coincide. The same correspondence exists between monotonicity and incremental passivity, with the proof requiring very little modification. We refer the interested reader to [49, Chapter 6, lemma 9.2] for details.

Note that, for linear relations, positivity and monotonicity coincide. Indeed, if we restrict ourselves to linear relations \( \lambda \), then we can write \( Au - Av = A(u - v) \). By linearity of the signal space \( \mathcal{H} \), \( u - v \in \mathcal{H} \), and furthermore any \( x \in \mathcal{H} \) can be written as \( x - 0 \), with \( 0 \in \mathcal{H} \), which shows that \( \mathcal{H} - \mathcal{H} = \mathcal{H} \). The definition of monotonicity then reduces to

\[
\langle u | Au \rangle \geq 0,
\]

which is the definition of positivity.

In the linear, time invariant case, the physical property of passivity allows questions to be answered in a computationally tractable way, for example, a passive storage function can be found by solving an LMI [5]. For nonlinear passive systems, these computationally tractable methods no longer apply, in general. For nonlinear systems with incremental properties, however, tractable methods do exist. This is the fundamental result of contraction theory [73], is noted in the input/output context from Fromion and Scorletti [74], and more recently in dissipativity analysis by Verhoek, Koelewijn, and Tóth [75] and Forni, Sepulchre, and van der Schaft [76]. The approaches in these works differ from that of this paper, however, in their reliance on state-dependent linear matrix inequalities, rather than monotone operator methods.

Passivity of nonlinear input/output systems can be unintuitive. For example, there exist physical nonlinear resistors which are passive and have regions of negative differential resistance [43]. Their passivity is quickly verified by checking that the \( i \)-\( v \) curve lies entirely in the first and third quadrants. The inverse of such a device is set-valued, and not well-defined in the traditional theory of passive systems. Monotonicity precludes such systems.

### B. Monotonicity and order

Let \( \mathcal{H} \) be a Hilbert space, and define \( \mathcal{M}_H \) as the set of all monotone relations on \( \mathcal{H} \).

\( \mathcal{M}_H \) is closed under the operations of summation, scalar multiplication and inversion. Furthermore, it is a proper superset of the set of passive LTI relations studied by Cohen and Lewkowicz [77]. Hence \( \mathcal{M}_H \) may be viewed as a generalization of the convex, invertible cone of passive transfer functions, with the caveat that inversion is understood in the relational sense, and it may not be that \( R^{-1} = I \). We leave for future research the question of how stronger properties such as coercivity and cocoercivity generalize sub-cones of
the convex, invertible cone of passive transfer functions, such as the cone of strictly passive transfer functions.

The cone structure of $\mathcal{M}_R$ allows an ordering to be defined on monotone relations: for $A, B \in \mathcal{M}_R$, we write $A \preceq B$ if $B - A \in \mathcal{M}_R$, and $A < B$ if $A \preceq B$ and $A \not= B$. This generalizes the order of passive transfer functions [78].

C. Open synthesis problem

A central question of circuit theory is the network synthesis problem, that is, the realization of an input-output relation by a port interconnection of electrical elements. This question was first developed in the context of LTI inductors, capacitors and resistors, beginning in the work of Foster [46] and Cauer [47]. Brune [47] introduced the idea of a positive real transfer function, and showed that any such transfer function can be synthesized as the 1-port behavior of a series/parallel interconnection of LTI resistors, capacitors, inductors and transformers. Bott and Duffin [1] removed transformers from the construction.

We have shown that any series/parallel interconnection of monotone elements is monotone. We leave the converse question for future research.

**Question 1.** Given a monotone relation $S$ between current and voltage, construct a 1-port by interconnecting monotone resistors, inductors, capacitors and memristors in parallel and series, such that the 1-port relation is equal to $S$.

VII. CONCLUSIONS

We have shown that the input/output property of monotonicity is a generalization of the linear theory of passivity which retains algorithmic tractability for nonlinear circuits. Computational methods have been developed for the particular problem of steady state periodic analysis of 1-ports composed of monotone resistors, capacitors, inductors and memristors. Several questions are left open for future research. Among these are the extension to $n$ ports and to multi-input, multi-output systems. The treatment of monotone systems with the state property and, more generally, the connection of monotonicity to incremental passivity will be the topic of a subsequent article.

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