Gradient-Based Neuromorphic Learning on Dynamical RRAM Arrays

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Abstract—We present MEMprop, the adoption of gradient-based learning to train fully memristive spiking neural networks (MSNNs). Our approach harnesses intrinsic device dynamics to trigger naturally arising voltage spikes. These spikes emitted by memristive dynamics are analog in nature, and thus fully differentiable, which eliminates the need for surrogate gradient methods that are prevalent in the spiking neural network (SNN) literature. Memristive neural networks typically either integrate memristors as synapses that map offline-trained networks, or otherwise rely on associative learning mechanisms to train networks of memristive neurons. We instead apply the backpropagation through time (BPTT) training algorithm directly on analog SPICE models of memristive neurons and synapses. Our implementation is fully memristive, in that synaptic weights and spiking neurons are both integrated on resistive RAM (RRAM) arrays without the need for additional circuits to implement spiking dynamics, e.g., analog-to-digital converters (ADCs) or thresholded comparators. As a result, higher-order electrophysical effects are fully exploited to use the state-driven dynamics of memristive neurons at run time. By moving towards non-approximate gradient-based learning, we obtain highly competitive accuracy amongst previously reported lightweight dense fully MSNNs on several benchmarks.

Index Terms—Neuromorphic computing, memristor, spiking neural network, supervised learning, backpropagation.

I. INTRODUCTION

SPIKING Neural Networks (SNNs) impose neuroscience-inspired constraints to modern deep learning algorithms, and have accordingly demonstrated significant improvements in runtime efficiency. By moving from full precision and fixed precision activations of artificial neuron models over to temporally-encoded data representations captured by spiking neurons, neuromorphic hardware has shown significant savings in energy consumption and latency [1], [2], [3], [4], [5], [6].

The broad success of error backpropagation to train deep learning models has ushered in a plethora of related training algorithms adapted for SNNs, most of which are guided by surrogate gradient descent to overcome the non-differentiability of discrete spikes [7], [8]. This proliferation of SNN usage is complemented by the development of modular deep learning programming packages that have optimized autodifferentiation for CUDA acceleration [9], [10], [11], [12], [13].

In parallel to these advances in training SNNs, the past decade has seen huge strides in brain-inspired devices, circuits, and architectures that integrate neuronal dynamics to improve the hardware integration of SNNs and its constituent parts. Memristors and resistive RAM (RRAM) make up an immense part of such exploratory research in SNN implementation as they are a natural bridge between SNN algorithms and accelerators [14], [15]. They have been widely employed as both synapses and as spiking neurons.

At the ionic level, memristive synapses have been integrated into systems that naturally implement the spike-timing-dependent-plasticity (STDP) update rule using higher-order device dynamics [16], [17], [18]. An alternative use of ion-driven dynamics is when implementing the memristor as a neuron, where nonlinear conductance evolution gives rise to abrupt switching that can be used to emit sudden voltage spikes. This approach is typically coupled with capacitive integration, and has been referred to as a ‘neuristor’ [19], [20], [21], [22], and a ‘memristive integrate-and-fire’ (MIF) neuron [3], [23], [24]. Similarly, membrane leakage in biological neurons can be implemented using resistive dissipation as in neuristors, or via volatile ionic drifting dynamics observed in single devices [25] and also in nanowire networks [26], [27], [28].

Moving up to the architectural level, RRAM has been shown as a promising candidate for compute-in-memory (CIM) architectures due to their ability to parallelize matrix-vector multiplication independently of time complexity when integrated as large-scale, modular arrays [29], [30], [31], [32], [33]. Rather than neurons, memristive synapses map neural network weights to device conductances. In general, RRAM CIM architectures are intended to be trained offline with weights mapped on-chip for inference and deployment. As such, RRAM synapses should be stationary and only used for weight read-out. Higher-order dynamical behaviors of memristors are abstracted away, and treated as non-idealities.

An additional challenge with RRAM-based CIM is the cost of communicating analog current signals along lengthy bit-lines and conversion into the digital domain. These issues have spurred the use of binary activations in the form of spike-based CIM accelerators which have shown to alleviate the burdens of mixed-signal computation, by removing the need for large analog-to-digital (ADC) data converters [34].

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The majority of deep learning acceleration using memristors can be classified into one of the above cases: memristive neurons, memristive synapses that learn via associative learning, and CIM accelerators. A small set of designs have combined memristive neurons and memristive synapses together [35], [36]. Doing so is a commendable feat, as the natural switching dynamics of memristive systems are relied on to achieve data-driven tasks. The cost of allowing hardware behave naturally is that a designer can no longer rely on synchronous, clock-driven processing, and is subject to fault injections that are a result of nonlinear ionic dynamics. Letting the natural dynamics of memristive hardware to ‘teach itself’ exacerbates the challenges of training MSNNs. This challenge has limited the demonstration of fully memristive SNNs to unsupervised learning tasks that have shown to solve simple, low-dimensional pattern recognition via local learning rules (typically STDP) and associative learning. These include the classification of several characters and numbers (such as a subset of the MNIST dataset).

In this paper, we push beyond the classical limits of fully memristive SNNs, and demonstrate competitive performance on real-world datasets that go beyond static pattern recognition using a MSNN that includes both memristive synapses and memristive neurons. We achieve this by combining higher-order memristive dynamics with the gradient optimization process. While fault injections during weight update have been accounted for in the past, this is the first time nonlinear memristive dynamics are included within the computational graph used in the gradient calculation process, enabling more precise fine-tuning of network parameters.

The action potentials generated by memristive neurons are a result of nonlinear ion-driven dynamics, which are functionally equivalent to a chain of nonlinear operations in a computational graph. As each spike is a result of naturally arising physics-driven phenomena rather than discrete switching in digitally-composed SNNs, all functions are fully differentiable and the gradient is well-defined. Therefore, there is no need to resort to surrogate gradient approaches that have become ubiquitous when training SNNs. The voltage action potential is scaled by memristive synapses, and the resultant current drives downstream layers of memristive neurons.

An overview of our approach is shown in Fig. 1 and a summary of our contributions are provided below:

- We present a fully memristive SNN utilizing both memristive neurons and synapses, and is shown to achieve state-of-the-art accuracy for lightweight dense network architectures on real-world datasets. These datasets are more complex than what has been demonstrated in the past on MSNNs while using naturally arising physics-driven phenomena in RRAM;
- We propose MEMprop, the application of error backpropagation directly to SPICE circuit models of memristive neurons such that higher-order device dynamics are fully utilized in the learning process. Memristive dynamics are broken down into a series of composable, differentiable functions and used during gradient descent;
- SNNs are shown to be trainable without the need for gradient approximations around hard thresholds, such as with surrogate gradient descent; and
- The need for ADCs is amortized by relying entirely upon analog current injection at the input, and analog action potentials at the output.

In doing so, the rich dynamics of nonlinear devices can be fully leveraged in larger systems, in a way that moves far...
beyond applying fault injection and variation into the training process. We achieve state-of-the-art accuracy for lightweight dense network architectures on several static and neuromorphic datasets, which pushes the fringe of what previous MSNNs have shown to be capable of.

II. Memristive SNN Based Learning

There is an incredibly broad span of work that integrates memristors with brain-inspired architectures, from low-level analog action potential emulation [23], to discrete spiking dynamics [34], up to non-spiking CIM processors [29]. We focus our background on prior work that use nonlinear dynamics in memristive neurons together with memristive synapses, with associated demonstration of synaptic optimization to achieve a data-driven outcome.

A. Fully Memristive SNNs

Fully memristive SNNs refer to arrays that utilize nonlinear switching dynamics of memristors to trigger action potentials, and are coupled with memristive weights that are used as neural network parameters. The $8 \times 8$ crossbar array presented in [35] successfully integrates a fully memristive SNN, including memristive synapses and neurons. The synaptic array is trained using unsupervised STDP to classify four letters in a 24-pixel grid. While the task achieved is considerably simple, the fully memristive experimental demonstration sets the stage to build upon new training methods.

The work in [37] uses half-wave rectification interposed between crossbar arrays to process the ReLU activation in the analog domain. While not fully memristive, nor a ‘spiking’ network, it demonstrates a pivotal example of successively passing analog activations between RRAM crossbars without intermediate data conversion, in a manner akin to how our analog action potentials are transmitted between layers. The training process relies on gradient-based optimization where device non-idealities are injected during the forward pass. In doing so, a test set accuracy of 93.63% is obtained on the MNIST dataset.

In Refs. [38] and [39], convolutional SNNs with memristors are used, where both used pretrained on non-spiking networks that are mapped or converted into the spiking domain. Both networks obtained competitive accuracy on the MNIST dataset, though did not demonstrate performance on more complex, real-world data. This may potentially be due to the large differences between the networks that were trained and the MSNN that was implemented. In Ref. [40], a dense MSNN is adopted using a similar approach to what is used here, and as such, has minimal hardware requirements at run-time. The training process abstracts away the switching dynamics of the memristive neuron into a firing rate, and may be the reason why a relatively low accuracy of 83.2% was achieved on the MNIST dataset. A more detailed comparison is illustrated in Section V, subsection B.

Almost all of these works offer compelling demonstrations using in-house fabricated arrays, either with standalone crossbars or back-end-of-the-line (BEOL) integrated arrays with foundry-made chips. In contrast, we have aimed to make our work as device-agnostic as presently possible by using commercially available Knowm memristor and its corresponding model [41].

Although Knowm memristors are not known for their reliability, their metastable switching dynamics are accounted for within the gradient calculation step, as it forms part of the computational graph. In contrast, Kiani et al. use the memristors in the forward-pass only, as their devices are not intended to be reprogrammed during inference, and thus do not require switching to generate spiking dynamics. Gradients can therefore be deterministically calculated partially off-chip [37], whereas our approach harnesses memristive dynamics in the forward-pass computation in our network. As such, our MSNN approach can leverage the benefits of spike-based processing, such as sparse processing and lower data collision rates.

B. Memristive Learning Frameworks

To ease and emulate the training process of memristive networks, a variety of valuable frameworks have been developed that each address various niches. These include MemTorch [42], NeuroSim [43], and the IBM Analog Hardware Acceleration Kit [44], which implement non-spiking networks that adopt mixed-signal bit-line charge/current accumulation/summation processing. In these simulators, memristive dynamics are accounted for during weight updates, and are otherwise fixed during inference. To complement these tools, NeuroPack [45] specifically targets the simulation of spiking networks, where memristive dynamics are also factored in during the weight update process, and fixed during inference. Spiking dynamics are triggered by pulse-based input voltages.

The closest relation to our proposed work comes from Demirag et al. who offer a software implementation of a real-time recurrent learning variant [46], [47] using phase change device models to train a MSNN [48].

Much like these simulators, our approach MEMprop integrates SPICE-level memristor models into the training process. But distinct from these simulators and training methods, we utilize arrays of memristive integrate-and-fire (MIF) neuritors that trigger self-induced action potentials during the forward-pass computation. To emit spikes, the state of a memristor must evolve and ultimately switch to provide sudden discharge pathways which triggers spikes. Therefore, the dynamical characteristics of a memristor will alter the gradient itself, whereas all prior approaches account for dynamics in the weight update step when reprogramming memristive synapses.

Our approach applies the backpropagation algorithm directly to SPICE-level neuristor models that emit analog action potentials as a result of charge-accumulation and metastable threshold switching. That is to say, the memristive dynamics in SPICE models are not fixed during the forward-pass, but rather, they are dynamically extracted during the forward-pass to fire neuristor-induced spikes. The BPTT algorithm is applied directly to SPICE models, thus integrating memristive neurons as part of the gradient calculation step, rather than isolating their dynamics to synaptic weight updates as in prior implementations. This offers a dynamical and totally new way to train fully memristive networks that uses state-based dynamics as part of the gradient calculation step.

In terms of hardware implementation, the conventional use of RRAM in circuits often requires significant overhead to convert analog currents into digital voltages and consumes large amount of power [29]. In many instances, the power/area demands of the ADCs and Digital-to-Analog
Converters (DACs) far exceeds the overhead brought on by RRAM, offsetting the advantages of memristors. In contrast, our spike-based approach eliminates the need for ADCs and DACs such that the cost of peripheral circuits are substantially reduced.

C. Error Backpropagation Through SPICE Models

Our proposed approach enables us to scale up the complexity of learnable tasks in fully MSNNs by directly applying gradient descent to the nonlinear state evolution of memristive neurons and synapses. Both neurons and synapses in biological neural networks are modeled using memristors. The MIF neuron model is designed to achieve distinct depolarization, hyperpolarization, and repolarization voltage phases with a minimal set of circuit elements. Memristive synapses act as interconnects between layers of neurons.

To train the fully memristive network, we propose MEMprop, an application of error backpropagation to large-scale networks derived from SPICE circuit models. This enables dynamical, time-varying memristive neurons to learn and thus achieve much higher accuracy on data-driven tasks than has been previously reported with MSNNs. By relying on the analog spiking characteristics that naturally occur in the MIF neuron model, the non-differentiability of spike-based activations are completely avoided. This means MEMprop does not rely on surrogate gradient techniques that are commonly used to train SNNs, which calculates biased gradient estimators to circumvent the dead neuron problem [8].

To promote broad accessibility of our methods, we use SPICE models of commercially available, low-cost memristors and demonstrate the efficacy of MEMprop in a supervised deep learning framework.

III. DESIGN METHODS

A. Memristive Integrate-and-Fire Model

The neuron model adopted in our MSNN is the MIF neuron model depicted in Fig. 2(a) [23]. Qualitatively, given a positive current injection $I(t)$, the membrane potential $v(t)$ will charge up from the neuron’s resting potential $E_{\text{rest}}$. Once a sufficiently large electric field builds up across the memristor $M_2$, it switches on, effectively shorting the output to $E_{\text{rest}}$. The action potential waveform that the MIF triggers is shown in Fig. 2(b), and our prior work in Ref. [23] provides an experimental demonstration using a pair of Knowm memristors.

The memristor model used is based on the generalized metastable switch (MSS) model [41], which has been used to accurately describe a large range of possible devices. In this model, a MSS is an idealized element that switches with a given probability between two states as a function of its voltage and temperature. A memristor is modeled by a collection of MSSs, which determines the state-time dynamics that lead to non-volatile characteristics. $s$ characterizes the internal state as a variable normalized between 0 and 1, as determined by the switching states of all MSSs.

Formally, the governing dynamics of the MIF neuron are characterized by the system of differential equations in Table I. The membrane potential $v$ is dependent on $G_1$ and $G_2$, the device conductances of $M_1$ and $M_2$, the MIF capacitance $C$, and $E_{\text{rest}}$ and $E_{\text{reset}}$, which are voltage biases in the MIF circuit.

$G_1$ and $G_2$ are dependent on $x_1$ and $x_2$, a pair of variables governing the internal state of each device, where $R_{\text{on}}$ and $R_{\text{off}}$ are the on/off resistances.

The rates of change of $x_1$ and $x_2$ are dependent on the state evolution time constants $\tau_1$ and $\tau_2$, the thermal voltage $V_{\text{th}}$ at room temperature, and the volatility constant $k_v \in [0, 1]$ in the range of 0 to 1. As $k \to 0$, the more retentive the device is.

B. Neural Network Layout

When accounting for the hardware implementation of a fully memristive neural network, the voltage response of the MIF neuron must drive the memristive synapses, and is correspondingly weighted by the synaptic conductances. This can be fully integrated in a crossbar according to Eq. (1) below:

$$I = G \times V$$

where $I$ is the output current vector, $V$ is the input voltage vector, and $G$ is the conductance matrix of the crossbar. The output current vector is generated via bit-line current summation as shown in Eq. (2), and directly drives the input of the next MIF neuron layer. Resistive loading may attenuate the output current in subsequent stages, but this can be accounted for using a scaling factor, or otherwise buffered [23, 49, 50].

Fig. 3 shows a small-scale schematic of a fully memristive neural network with three MIF neurons and a $3 \times 2$ memristive crossbar, which receives three fan-in input currents $I_{\text{in}0} - I_{\text{in}2}$ and generates two fan-out output currents. $E_{\text{rest}}$ and $E_{\text{reset}}$ are the voltage sources in the MIF circuit. $C_{\text{BL}}$ is the bit-line parasitic capacitance generated by the metal line, or otherwise by the drain-bulk capacitance of select transistors, and is used as the membrane capacitance in the MIF circuit.

C. Forward-Mode Solution of MIF Model

In order to train a network of MIF neurons and synapses using gradient descent, the differential equations representing
TABLE I
MIF MODEL DIFFERENTIAL EQUATIONS VS NUMERICAL INTEGRATION

| Variable | Continuous Time Derivative | Discrete Time Solution |
|----------|-----------------------------|------------------------|
| $v$      | $\frac{dv}{dt} = \frac{I - G_1(v - E_{\text{rest}}) - G_2(v - E_{\text{rest}})}{C_{\text{m}}}$ | $v_{t+1} = \frac{I - G_1(v_t - E_{\text{rest}}) - G_2(v_t - E_{\text{rest}})}{C_{\text{m}}} + v_t$ |
| $G_1$    | $G_1 = \frac{x_1}{C_{\text{m}1}} + \frac{1}{R_{\text{eff}}} \frac{dx_1}{dt}$ | $G_{1_{t+1}} = \frac{x_{1_{t+1}}}{C_{\text{m}1}} + \frac{1}{R_{\text{eff}}} x_{1_{t+1}}$ |
| $G_2$    | $G_2 = \frac{x_2}{C_{\text{m}2}} + \frac{1}{R_{\text{eff}}} \frac{dx_2}{dt}$ | $G_{2_{t+1}} = \frac{x_{2_{t+1}}}{C_{\text{m}2}} + \frac{1}{R_{\text{eff}}} x_{2_{t+1}}$ |
| $x_1$    | $\frac{dx_1}{dt} = \frac{1}{\tau_1} \left( \frac{1 - x_1}{1 + \exp\left(\frac{v_t - E_{\text{reset}}}{\tau_{\text{syn}} \gamma_v}\right)} - 1 \right)$ | $x_{1_{t+1}} = \frac{1}{\tau_1} \left( \frac{1 - x_{1_{t+1}}}{1 + \exp\left(\frac{v_{t+1} - E_{\text{reset}}}{\tau_{\text{syn}} \gamma_v}\right)} - 1 \right) + \frac{x_1}{\tau_1}$ |
| $x_2$    | $\frac{dx_2}{dt} = \frac{1}{\tau_2} \left( \frac{1 - x_2}{1 + \exp\left(\frac{v_t - E_{\text{reset}}}{\tau_{\text{syn}} \gamma_v}\right)} - 1 \right)$ | $x_{2_{t+1}} = \frac{1}{\tau_2} \left( \frac{1 - x_{2_{t+1}}}{1 + \exp\left(\frac{v_{t+1} - E_{\text{reset}}}{\tau_{\text{syn}} \gamma_v}\right)} - 1 \right) + \frac{x_2}{\tau_2}$ |

Fig. 3. Schematic of a fully memristive neural network. The blue-shaded segment depicts memristive neurons, and the orange-shaded segment includes memristive synapses.

the MIF circuit dynamics (middle column, Table I) are recast into discrete-time form (left column, Table I). In doing so, the memristive dynamics can be captured in a computational graph that evolves over time, much like a recurrent neural network (RNN).

In practice, SPICE simulators use a variety of differential equation solvers, such as the backward Euler method, and the 4th-order Runge-Kutta method (RK4). For compatibility with the BPTT algorithm, we solve the differential equations using the forward Euler method, which provides an explicit representation of the next time step using present-time dynamics. The rich dynamics of the MIF neuronal network are now accounted for in the MSNN, unrolled in time such that gradient descent can be used to optimize the memristive synapses as a function of the MIF evolution.

Many neural coding studies represent spike trains as a summation of time-shifted Dirac delta pulses $\sum_n \delta(t - t^n_i)$. As such a model of spikes is an idealization, we use the spike train to modulate a time-continuous, alpha input current $I$ modeled by the equation in Table II to be compatible with real, physical systems. In this series of equations, $a$ is an internal state variable, $\tau_{\text{syn}}$ is a time constant that determines the shape of the alpha current, $W_i$ is the synaptic weight between a presynaptic neuron $i$ and its associated post-synaptic neuron. It is commonly regarded that such alpha waveforms correspond to the response from biological neurons in the sensory periphery that respond with graded potentials [51].

D. MIF Single Neuron Simulation

To verify the accuracy of the forward Euler method, we conduct a single neuron simulation using Python shown in Fig. 4 across 1,000 time steps, which provides ample time for the membrane potential $v$ to traverse from spiking $V_{th}$, to the reset potential $E_{\text{reset}}$, back to the resting potential $E_{\text{rest}}$. Each time step is of duration 0.01 ms over a total duration of 10 ms.

The parameters used in the simulation are listed in Table III. The resting potential, charge integration, thresholding, and reset dynamics are closely reproduced in a SPICE simulator that uses the RK4 solver, which verifies the solution generated by adopting the forward Euler method. Deep learning is known to be tolerant to fault injections [52], [53], and so the tradeoff between the numerical integration accuracy and the training complexity should be considered. We adopted Forward Euler method which is able to balance the two. Technically, our training method is expected to generalize to other numerical integration methods as well, but with added computational complexity.

E. BPTT in MSNNs

The discrete-time solution in Table I is illustrated as a directed, acyclic graph in Fig. 1, where time flows from left to right. The MIF circuit parameters are color-coded to show how each electrical characteristic impacts the others at the next time step. To train a network, a loss function is calculated using the membrane potential $v$ of the output layer at each step. Note that the adjoint method in [54] is not adopted here, as an intermediate state is required to calculate loss and guide training for each time step. We are concerned with the spiking output at all time steps, and not just the final state of the system which makes BPTT a more optimal choice. In our example network provided in Fig. 1 with 10 output neurons, the predicted MIF neuron is expected to spike most frequently by aiming to increase the membrane potential across time steps, while the incorrect target should be suppressed. As the membrane dynamics are continuous, a fully analog MSNN can be trained without surrogate gradients, as has become ubiquitous in deep SNNs trained via error backpropagation [8], [55].
TABLE II

| Variable | Continuous Time Derivative | Discrete Time Solution |
|----------|-----------------------------|------------------------|
| $I$      | $\tau_{\text{syn}} \frac{dI}{dt} = a - I$ | $I^{t+1} = \frac{I^t - I^{t+1}}{\tau_{\text{syn}}} + I^t$ |
| $a$      | $\tau_{\text{syn}} \frac{da}{dt} = -a + W_i \cdot \sum_{n} \delta(t - t_i^n)$ | $a^{t+1} = -a^t + W_i \cdot \sum_{n} \delta(t - t_i^n) + a^t$ |

The input layer consists of a number of input features (784 for the static datasets; 2,048 for a downsampled neuromorphic dataset). An alpha current generator with an amplitude weighted by the input pixel intensity (Table II), weighted by memristive synapses, inducing 100 MIF neurons to fire into another set of memristive synapses, terminated by the output layer of MIF neurons. To account for circuit loading effects, the current injected to each MIF layer is attenuated by a scaling factor defined in the hyperparameters.

B. Datasets

Three datasets of increasing difficulty are used to assess the MSNN: MNIST, FashionMNIST, and the DVS128 Gesture datasets. Despite being considered a ‘solved’ problem for quite some time now, it was often the case that the MNIST dataset was the most challenging problem that could be solved by previously reported MSNNs. In most cases, a subset or simplified alternative would be used to demonstrate pattern recognition. Here, we demonstrate for the first time that RRAM arrays that rely on internal dynamics are still capable of processing more challenging problems and real-world datasets, namely, FashionMNIST and neuromorphic data.

The MNIST [56] and the slightly more challenging FashionMNIST datasets [57] are used to test the performance of the MSNN on temporally static data. Both datasets consist of 60,000 28 × 28 greyscale images in the training set, and 10,000 images in the test set, with 10 output classes of handwritten digits (MNIST) and clothing items/accessories (FashionMNIST/FMNIST). During the training process, the alpha current inject is applied at every 100 steps to promote sparse network activity.

For a more challenging test case, the DVS128 Gesture dataset [58] is used a neuromorphic baseline to test the MSNN’s performance on event-driven data filmed with an event-based camera [59]. Each sample only processes sufficient changes in luminance, and consists of 11 different output classes of hand gestures, such as clapping, arm rotation, and air guitar. Each sample is downsampled to a resolution of 32 × 32 × 2, where the channel depth of 2 accounts for on and off spikes (positive and negative luminance changes). The training data is integrated to fit within 100 discrete time steps, and the testing data is integrated within 360 time steps, to account for GPU memory constraints.

C. Training Process

The forward Euler solution of each MIF neuron was defined in PyTorch v1.10.1 in Python 3.8, where the autodifferentiation framework was used to keep track of gradients of all forward-mode computations on-the-fly.

IV. EXPERIMENTAL RESULTS

A. Network Architecture

To validate the use of MIF neurons in a deep learning framework, we used a lightweight 3-layer dense SNN with 100 hidden MIF neurons (bottom-left of Fig. 1). Each MSNN is simulated for a duration of 10 ms over a span of 1,000 discrete time steps.

IV. EXPERIMENTAL RESULTS

A. Network Architecture

To validate the use of MIF neurons in a deep learning framework, we used a lightweight 3-layer dense SNN with 100 hidden MIF neurons (bottom-left of Fig. 1). Each MSNN is simulated for a duration of 10 ms over a span of 1,000 discrete time steps.
needs 10 RRAM tiles of 128 in size. Fig. 3, a total of 0.16M RRAM cells are required, which is linearized for the window of interest is $2.77 \times 10^{-3}\text{mm}^2$, and a complete array will occupy $2.77 \times 10^{-2}\text{mm}^2$ [61]. If a bit-line current summation approach was adopted for a dense ANN with 8-bit networks, a current-mode SAR ADC each occupies $3 \times 10^{-3}\text{mm}^2$, where 4 ADCs are shared across the column wires for each crossbar. In such a case, the improvement of our approach without converting and serializing activations by adopting a spike-based approach is a factor of $5.33 \times$.

The loss used is the negative log-likelihood of the membrane potential $v(t)$ (Fig. 1) of the output layer. The network objective is to increase voltage across the MIF neuron associated to the correct class. The total loss across time-steps is summed prior to backpropagating the error through the SPICE memristor model using the Adam optimizer [60]. The MSNNs are each trained for 50 epochs.

D. Results

The final test set accuracy is measured across 50 epochs over 5 trials for each dataset with early stopping applied, and the average result is shown in Fig. 5 with error bars.

The average accuracy on the MNIST dataset reaches 93.08%, which is very high among fully MSNN considering almost no required peripheral circuitry for hardware implementation and far exceeds other MSNN baselines that have been previously reported. Although it remains somewhat below non-memristive baselines which can obtain greater than 97% on the MNIST dataset using a similar architecture, such models are typically computed using fixed- and full-precision arithmetic rather than depending on naturally arising memristive dynamics.

Where our approach tends to shine is on real-world data that goes beyond the simplicity of handwritten digit recognition. Our fully MSNN performance holds for the FashionMNIST dataset, where we obtained an average of 84.77%, and also for the DVS128 Gesture dataset, with 82.63%. This provides the first successful demonstration of training a MSNN on a neuromorphic dataset by relying on naturally occurring device dynamics for spike emission.

V. Discussion and Conclusion

A. Area, Power, and Latency

With our fully MSNN approach, one of the main advantages is that we avoid the need for ADCs, and subsequently, we do not need to multiplex or serialize data. To quantify the potential improvement in terms of power, area, and latency, we assume a dense 3-layer architecture of 784-100-10 neurons. Such a network requires 110 MIF neurons and 79.4k memristive synapses. For each synaptic weight, a pair of devices are required to implement current subtraction to represent both positive and negative weights. Given the array structure in Fig. 3, a total of 0.16M RRAM cells are required, which needs 10 RRAM tiles of 128 × 128 in size.

To provide an area estimation at a 65-nm technology node, the size of each RRAM tile with 1T1R cells is $2.77 \times 10^{-3}\text{mm}^2$, and a complete array will occupy $2.77 \times 10^{-2}\text{mm}^2$ [61]. If a bit-line current summation approach was adopted for a dense ANN with 8-bit networks, a current-mode SAR ADC each occupies $3 \times 10^{-3}\text{mm}^2$, where 4 ADCs are shared across the column wires for each crossbar. In such a case, the improvement of our approach without converting and serializing activations by adopting a spike-based approach is a factor of $5.33 \times$.

Estimating the power consumption of asynchronous, spike-based workloads requires profiling the spiking activity in the network for a given dataset. Using the MNIST dataset, we found that an average of 2% of neurons are spiking at any given time in the network. This may be modulated to promote varying degrees of excitation in the network, for example, by applying a spike-dependent regularization term to the objective function. The average resistance in our network is close to the midpoint between the on/off resistances: $R_{\text{off}} = 100$ kΩ, $R_{\text{on}} = 1000$ Ω, average $R_{\text{ave}} = 50.5$ kΩ. The voltage across each device when emitting a spike follows a sharp peak of $v_{\text{on}} = 110$ mV, a refractory period where the potential drops down to $v_{\text{off}} = 5$ mV, and the average value assuming the spike is linearized for the window of interest is $v_{\text{ave}} = 57.5$ mV can give an estimate of the average power

$$P_{\text{ave}} = \frac{v_{\text{ave}}^2}{R_{\text{ave}}} \times N_{\text{cells}} \times 2\%,$$

which is then numerically evaluated for a single $128 \times 128$ tile to be 21.45 μW, and 0.21 mW when accounting for all 10 tiles. When accounting for data conversion overhead where each 8-bit ADC consumes $2 \times 10^{-4}$W, the total power consumption increases to 8.21 mW. Our approach can offer an improvement of $38.30 \times$.

We estimate latency by driving ADCs at an operating frequency of 40 MHz. With 4 ADCs converting 64 column currents (assuming 2 bit-lines per activation), 32 data-lines are grouped to share a driving DAC which generates an 8-bit serialized input operating across 8 distinct cycles, evaluating to input data latency of 6.4μs. At the output, 32 bit-lines each share an ADC where 16 column currents must be converted, increasing the latency by 0.4μs. Further assuming that data conversion dominates latency, this means that it takes 6.8μs per vector matrix multiplication (VMM). A 1,000 time step simulation, as used in our network, will extend this to a latency of 6.8 ms. Additionally, each input is fed as an alpha current signal with a measurable latency around 0.64 ms, giving the total latency for the conventional approach of 7.44 ms, as opposed to MEMprop which only requires the additional switching time of the memristors (on the order of 100s of nanoseconds added to the alpha current latency).

In our approach, currents and voltages are generated without the need for conversion or serialization, and so there is no additional switching time of the memristors (on the order of 100s of nanoseconds added to the alpha current latency).
TABLE V

COMPARISON AMONG FULLY MEMRISTIVE SPIKING NEURAL NETWORKS

| Method | Architecture | Neuron No. of elements | Refractory | Neuron feature | Training Method | MNIST | Complexity of Additional Control Logic |
|--------|--------------|------------------------|------------|----------------|-----------------|-------|---------------------------------------|
| [38]   | 1Mem-C-M-C-M-1024F-10F | 4(5)+33T | ✗ | Mixed-signal | LIF rate fit TDMA | 97.1% | high |
| [39]   | 784-C-M-C-M-10F | 5+2T | ✗ | Digital | Stochastic switch fit ANN converts SNN | ~96% | high |
| [40]   | 784-100F-10F | 3 | ✗ | Analog | LIF shape fit surrogate gradient | 83.2% | low |
| Our work | 784-100F-10F | 3(5) | ✓ | Analog | MIF direct train MEMprop | 93.2% | low |

1 T: transistor. 2 Mem: memristor. 3 C: convolutional layer. 4 M: max pooling layer. 5 F: fully connected layer.

TABLE VI

TEST SET ACCURACIES FOR THE MNIST, FASHION-MNIST, AND DVS128 GESTURE DATASETS

| Dataset  | Batch | LR      | Best | Avg. (n = 5) | σ    |
|-----------|-------|---------|------|--------------|------|
| MNIST     | 1e-4  | 93.18   | 93.08| 0.07         |      |
| FMNIST    | 1e-4  | 84.79   | 84.77| 0.13         |      |
| DVS-128   | 1e-4  | 83.21   | 82.63| 0.95         |      |

1 LR: learning rate \( \eta \). 2 \( \sigma \): standard deviation.

added ADC latency. The alpha current injection and response already account for RC delay through the memory array.

A summary of the above mentioned comparison is shown in Table IV.

B. Comparison

A comparative analysis against other memristive networks is provided in Table V. Where metrics are not provided in the original sources (e.g., chip area, power consumption, and inference latency), we have made an estimate where sufficient data has been provided to extrapolate these values. The closest MSNNs to our work are briefly described below.

In Ref. [38], a convolutional neural network with analog neurons and digital spiking at the input layer is adopted. Each analog neuron consists of four transmission gates, seven operational amplifiers, a comparator, and a memristor. While this is substantially more complex than the MIF neuron, the large overhead per neuron is offset by using time-division multiplexing access (TDMA) to treat a single physical neuron as multiple algorithmic neurons.

Wijesinghe et al. also adopt a convolutional SNN using stochastic switching to implement probabilistic firing, which is a natural fit for devices that switch based on random processes [39]. A non-spiking ANN is first trained and subsequently converted to an SNN. This approach is known to perform optimally for static datasets on reasonably deep SNNS, but it sets an upper-limit of performance such that the SNN accuracy will not surpass the accuracy of the ANN. Furthermore, ANN to SNN conversion is yet to show success on neuromorphic datasets [55]. The total area of the design is reported to be 3 mm², and the latency for a single spike is 0.21 \( \mu s \).

In Ref. [40], a 3 element neuron is constructed, consisting of a resistor, a memristor, and a capacitor, which is closest in spirit to our own approach here. The neuron is parameterized to fit to a leaky integrate-and-fire neuron model, which relies on hard-thresholded spike generation which is a non-differentiable function. The problem is circumvented by utilizing surrogate gradient descent, and results in a test set accuracy of 83.2%. This comparatively lower accuracy highlights the challenges of adopting neuristor-like dynamics, and the difficulty of mapping conventional training methods, both supervised (surrogate gradient descent) and unsupervised (STDP), to dynamical RRAM arrays. We expect the lack of a direct correspondence between thresholded leaky integrate-and-fire neurons and memristive neuron spiking is what resulted in the accuracy degradation, though it sets the stage for developing new training methods that account for dynamical, continuous-time switching into the computational graph of the network. In absence of power consumption metrics, we apply the same assumptions as in our MSNN architecture, namely, that 2% of the network is active at any given time, and estimate the total power consumption is 0.63 W.

No surrogate gradients or associated approximations are required due to the continuous-time nature of the spiking behavior in our experiments. The absence of ADCs/DACs in conventional full-precision/fixed-precision bit-line current summation approaches reduces the computational overhead. This is due to the use of MEMprop. More details of our experiments are listed in Table VI.

C. Concluding Remarks

To the best of our knowledge, this is the first work that has mapped low-level, analog SPICE dynamics directly into an acyclic computational graph that is compatible with the backpropagation algorithm. Directly mapping the behavior of dynamical RRAM arrays into an autodifferentiation framework has enabled us to achieve promising performance on real-world datasets on fully memristive SNNS, beyond simple pattern recognition and handwritten digit classification. By harnessing a blend of the intrinsic behaviors of memristors and the sparse network activity of SNNS, the power consumption and latency of our approach surpasses that of all other similar methods without compromising on accuracy.

We propose MEMprop with a lightweight dense neural network to validate this idea of applying backpropagation...
directly to SPICE circuit model. In the future, a deeper convolutional MSNN can be explored to further improve accuracy and to solve more complex tasks. In such a case, the benefits of MEMprop in terms of area, power, latency should still hold. Our approach can account for fault injections by incorporating device-to-device variability at the SPICE model level, which are then ported into gradient-based updates. This is important in the commercial memristors available, as learning heterogeneous device dynamics can improve the representational capacity of MSNNs. MEMprop should be able to offer a method by which these variations are accounted for during the training process. While variation is tolerable, neuristor-based firing relies on device switching which is a limiting factor in RRAM cells that exhibit limited cycle endurance. This motivates the development of devices that have a wide range of behaviors, but are resilient to consistent switching. Nonetheless, we successfully trained our network to be sparsely activated, which reduces the frequency of switching and relaxes this stringent demand on large device endurance.

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