A Reduced Single-Phase Switched-Diode Cascaded Multilevel Inverter

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Abstract—The cascaded multilevel inverters (MLIs) are suitable topologies when a high number of voltage levels are needed. Nonetheless, cascaded topologies possess the main drawback of a high number of power switches and gate drivers that make sophisticated control, reducing efficiency, and increasing cost. This article proposes a new fundamental switched-diode topology that is capable of generating five positive-voltage levels with only three power switches, three power diodes, and three dc voltage sources. Based on a combination of the \( n \) number of new fundamental topology, two cascaded topologies are proposed, which increases the number of voltage levels and decreases the number of power switches and voltage stress. The proposed cascaded topologies can operate in asymmetric dc sources, so different dc voltage source magnitudes are submitted to minimize the number of components. The main advantages of the proposed cascaded topologies are reducing the number of power switches, and gate drivers with reasonable dc voltage sources count in comparison with other state-of-the-art cascaded topologies. Furthermore, the proposed topologies reduce the cost in comparison with other recent MLI topologies. The power loss analysis and the recommended application for the proposed topologies are discussed. The simulation and experimental works are presented to verify the operation correctness of the proposed topologies.

Index Terms—Cascaded configurations, single-phase multilevel power converter, symmetrical and asymmetrical.

I. INTRODUCTION

MULTILEVEL power inverters create a higher number of voltage levels compared with the two-level inverters that are widely used in medium-voltage high-power applications. Multilevel inverters (MLIs) generate a staircase waveform at the output using a number of lower voltage dc links. The inverters are, therefore, capable of generating an output voltage waveform with low total harmonic distortions (THDs). In addition, the voltage rating of power semiconductor devices is lower than the overall output voltage because the topologies use many switches in cascade, meaning that the voltage is shared between many devices. Therefore, MLIs can be applied in medium-voltage applications and have some advantages compared with conventional two-level power inverters, particularly in some power system conditions, including static synchronous compensator (STATCOM), flexible alternating current transmission system (FACTS) devices, electrical vehicle (EV), ac motor drives, and renewable energy sources (RES) [1], [2]. The basic operation of MLIs can be found in three general topologies: neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) MLIs [3], [4]. Some disadvantages of FC and NPC inverters are the voltage magnitude of some of the devices, unbalanced dc-link conditions, and the high capacity capacitors. These drawbacks can be solved by using cascaded connections of the converter, such as the CHB topology, but they require more power semiconductor switching devices [5]. Therefore, researchers have been improving this type of topology based on proposing the new basic units or submodule topologies, replacing the H-bridge inverter in the cascaded connection [6]–[8]. Recently, a number of studies can be found about new multilevel power inverters topologies with a reduced number of power semiconductor devices and dc power supplies in [9]–[20]. Babaei et al. [9], [10] and Babaei and Laali [11] have developed three single-phase MLIs topologies. In all these topologies, a new topology is used, which is formed from two half-bridge inverters, for example, a back-to-back inverter with two additional power switches in the circuit. The first topology presented [9] has developed for cascaded MLI applications along with several dc power supplies implementation methods. A generalized topology of [9] is given in [10], and it has extended for additional voltage levels by expanding the basic structure. Babaei and Laali [11] have investigated a topology [9], [10] to increase the number of voltage levels by introducing an optimal arrangement. The resulting topology creates all the additional voltage levels without other circuits by changing the polarity of the output voltage, which is an advantage of these topologies. Still, they require a high number of dc power supplies to achieve a

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high number of voltage levels. A new single-phase basic unit for an MLI connected to an H-bridge inverter to change the polarity of the output voltage is suggested in [12]. This asymmetric configuration creates seven output voltage levels using three dc-links. The cascaded connection has been extended to generate a high number of voltage levels. The main limitation of this topology is the high value of total standing voltage (TSV) and the high number of power semiconductor devices, as well as dc power supplies. Samadeiet al. [13] introduced an Enveloped T-type (E-type) inverter using four dc-links and eight power switches that generate 13 levels in an asymmetric operation mode. The suggested topology in [14] is an improvement of the MLI topology presented in [13], which adds a bidirectional switch to boost the number of voltage levels from 13 to 17 levels. This topology is called Square T-Type (ST-Type), which generates 17 levels by four independent dc power supplies. The topology suggested in [15] is an advanced ST-Type topology called the K-Type module. This module uses two extra switches compared with the ST-Type module. It minimizes the number of dc power supplies to half by replacing just two capacitors, thereby producing 13 levels at the output. Alishah et al. [16]–[18] have suggested three different topologies based on H-bridge modules for general MLI topologies with a reduced number of power semiconductor devices. The recommended topology in [16] is an extensive topology that can operate in symmetric and asymmetric modes with a basic unit that can be extended to set up additional voltage levels. The suggested topology in [17] is a reconfiguration [16] with a different arrangement of the power semiconductor devices. The idea of the topology presented in [18] is the same with [16], but it requires only two dc power supplies. Other dc power supplies are replaced with capacitors, and some of the switching power devices are replaced with power diodes. In [19] and [20], two generalized MLIs have developed for symmetric and asymmetric MLIs. The presented topology in [19] uses a basic unit that has been developed for symmetric and cascaded configurations. This topology uses four unidirectional switches to reduce the standing voltage on the power switches and leads to reduce the power losses. The topology presented in [20] has the same form with [19] that developed for asymmetric MLIs. This topology generates 17 levels with the u-n shaped multicarrier-based pulsewidth modulation (PWM) modulation method.

Another configuration of MLIs is switched-capacitor-based MLIs (SC-MLIs) [21]. These groups of MLIs are introduced to minimizing the number of dc voltage sources because, usually, they use one or two dc power supplies in the input and other dc sources are replaced by capacitors that can charge in the desired voltages by suitable control strategies. SC-MLIs have some drawbacks; they require multiple sensors (voltage/current), costly controllers, signal processing circuits, and sophisticated control algorithms to deal with the voltage balancing of capacitors [22]. Hence, recently, researchers have been worked to develop SC-MLIs by introducing new configurations or advanced control strategies to balance the capacitor’s voltage and mitigate voltage ripples of capacitors [21]–[24]. Babaei and Gogwani [21] have introduced two cascaded SC-MLI configurations. Both presented cascaded MLIs comprised of two stages: the first stage builds up a basic unit that can be developed based on switched capacitors with one input dc voltage source, and the second part is an H-bridge inverter to create ac voltage. The used H-bridge in each basic unit is led to the number of switches increase. The majority of the SC-MLI uses an H-bridge inverter at the output that makes increases the number of power switches and the voltage stress on switches [21], [22].

A novel SC-MLI topology in [23] has been reported to overcome the aforementioned issues. This topology has removed the H-bridge inverter by a new arrangement of switches that can reduce the stress of voltage and also the number of switches. Recently, a new SC-MLI has been presented in [24] that does not need H-bridge inverter at the output to overcome interesting switch count when high levels are needed. This topology can be developed for more voltage levels by utilizing more switched capacitors easily. Also, the authors applied a hybrid PWM strategy to reduce the voltage ripples of capacitors that usually solved by considering larger capacitors. SC-MLIs usually operate in symmetrical dc source and cannot operate in the asymmetrical dc source, so the number of output voltage levels is less than MLIs that use multiple dc voltage sources. Hence, switched-diode MLIs require still a high number of power switches to generate a high number of levels.

Another type of MLIs is switched-diode-based MLIs. In this regard, a few switched-diode-based MLI topologies have been presented to mitigate the components count in the literature [25]–[30]. A general switched-diode MLI has been addressed in [25] and [26] with a different algorithm to determine dc source values. These topologies use a general basic topology along with an H-bridge at the output that can extend to a cascaded MLI. To produce a large number of levels, they still need a high number of switches and discrete diodes. The presented switched-diode MLI topology in [27] is a symmetric configuration that makes a limitation in the asymmetric operation in MLIs. Besides, this topology needs both types of bidirectional and unidirectional switches in its circuits that increase the number of insulated-gate bipolar transistors (IGBTs). A similar MLI topology has been investigated in [28] and [29] with two different objectives. Wang et al. [28] have removed the back-flow current by adding an extra power switch, and Kishore et al. [29] have mitigated THD value by PWM switching control. These topologies have not been investigated in the asymmetric and cascaded operation, so, to generate a large number of levels, they require a high number of power switches that make a restriction for medium- or high-power applications. A new topology for switched-diode-based MLI has been reported in [30]. The benefits of this topology are operating in asymmetric dc sources and use discrete diodes to reduce switches count. The disadvantage of this MLI is using a high number of dc voltage sources to make a high number of voltage levels. In addition, it still needs a large number of power switches to generate a high number of voltage levels. In addition to the discussed MLIs, the reduced MLI topologies to minimize devices’ count and the stress voltage of power switches are presented in [31]–[34].
The contribution of this article is introducing a switched-diodes cascaded MLI topology to decrease the number of power switches and gate drivers with some advantages over the recently published topologies. The rest of this article is organized as follows. First, a fundamental switched-diode-based topology is proposed. Then, the theoretical concepts of the proposed fundamental topology and its cascaded configurations are explained in detail. In Section II, a comparison study is made to show the variations among the number of devices, the variety of dc power sources, and TSV for the same number of levels for the proposed topology and other state-of-art MLI topologies. In Section IV, the power losses calculation is presented, and the medium-voltage-application of the proposed topology is investigated in Section V. The simulations and experimental results finally are analyzed for two case studies.

II. PROPOSED SWITCHED-DIODE MLI CONFIGURATION

The architecture of the proposed fundamental switched-diode MLI (SD-MLI) is shown in Fig. 1(a). The proposed SD-MLI comprises three dc power supplies, three switching semiconductor devices, and three diodes. The typical output voltage of the proposed SD-MLI is exhibited in Fig. 1(b). As can be seen in Fig. 1(b), the proposed inverter can generate five positive-voltage levels, \( V_1, V_2, (V_1 + V_2), (V_2 + V_3), (V_1 + V_2 + V_3) \), and a zero level. The switching states of the proposed basic SD-MLI are specified in Table I. In this table, “1” is the ON-state, and “0” is the OFF-state of the switching devices; “F” is forward bias, and “R” is the reverse bias of the diodes. All the valid operating modes of the proposed SD-MLI are shown in Fig. 1(c).

In the first mode, switch \( S_1 \) is ON, and switches \( S_2 \) and \( S_3 \) are OFF. Hence, diode \( D_3 \) is forward bias, and \( D_1 \) and \( D_2 \) are reverse biases. Therefore, the output voltage level is \( V_1 \). In the second operation mode, the voltage level \( V_2 \) is generated. For this mode, the switch \( S_2 \) is turned on, and the switches \( S_1 \) and \( S_3 \) are OFF. Hence, two diodes \( D_1 \) and \( D_2 \) are forward biases, and diode \( D_3 \) is in the reverse bias. In the third operation mode, two switches \( S_1, S_2 \) are ON, the switch \( S_3 \) is OFF, \( D_2 \) is forward bias, and two diodes \( D_1 \) and \( D_3 \) are reverse biases. Hence, in this mode, the voltage level of \( V_1 + V_2 \) is obtained. In the fourth mode, the voltage level of \( V_2 + V_3 \) is produced. For this mode, the switch \( S_3 \) is ON, the switches \( S_1 \) and \( S_2 \) are OFF, \( D_1 \) is forward bias, and two diodes \( D_2 \) and \( D_3 \) are reverse bias. In the fifth mode, the peak output voltage of \( V_1 + V_2 + V_3 \) is produced. In this mode, the switches \( S_1 \) and \( S_3 \) are ON, the switch \( S_2 \) is OFF, and all three diodes \( D_1, D_2, \) and \( D_3 \) are reversed bias. In the sixth mode, zero level is produced by turning off all three switches \( S_1, S_2, \) and \( S_3 \). Thus, two diodes \( D_1 \) and \( D_3 \) are forwarded biases, and \( D_2 \) is reverse bias.

As previously discussed, the proposed SD-MLI can only generate positive-voltage levels, so it requires an H-bridge inverter to change the polarity of the output voltage. Besides, the circuit can connect \( n \) number of SD-MLIs in series before the H-bridge to increase the number of output levels. The proposed cascaded MLI based on the \( n \) number of SD-MLI is displayed in Fig. 2(a). In this topology, each proposed SD-MLI can produce five different voltage levels and a zero level with output voltages of each unit being indicated by \( v_{o1}, v_{o2}, \ldots, v_{oN} \). Therefore, the total output voltage of the proposed SD-MLI can be calculated as follows:

\[
v_o(t) = v_{o1}(t) + v_{o2}(t) + \cdots + v_{oN}(t). \tag{1}
\]

Table II gives the general output voltage levels of the proposed cascaded MLI. As can be seen from this table, the proposed cascaded topology generates positive levels and requires an H-bridge inverter with four power switches (H1–H4) at the output.

Fig. 2(b) shows the proposed cascaded SD-MLI based on the proposed SD-MLI cell. In this topology, with two power switches \( H_1 \) and \( H_2 \), the positive-voltage level of \( V_L = +V_o \) is created, the negative-voltage level of \( V_L = -V_o \) is produced with two power switches \( H_3 \) and \( H_4 \), and the zero levels are provided by two pair switches of \( H_1, H_3 \) or \( H_2, H_4 \). In the proposed cascaded MLI, the number of power switches.

![Fig. 1. (a) Proposed SD-MLI topology. (b) Typical output voltage. (c) Operation modes.](image-url)
(or IGBTs) is $3n + 4$, and the number of power diodes is the same with the number of dc power supplies equal to $3n$, where $n$ is the number of basic SD-MLI.

An essential factor in reducing the cost of MLIs is the maximum TSV. The less TSV leads to the lower price of MLIs as the power electronics devices (IGBTs and diodes) will require a low TSV. However, the maximum TSV of the proposed SD-MLI is the sum of the standing voltages that each power switches and power diodes endure. Regarding Fig. 2(b), the value of TSV for the proposed cascaded MLI can be calculated as follows:

$$\text{TSV} = (V_{S1j} + V_{D1j} + V_{S2j} + V_{D2j} + V_{S3j} + V_{D3j}) + (V_{H1} + \cdots + V_{H4}).$$  

The magnitude of the maximum standing voltage on each semiconductor device is:

$$V_{S1j} = V_{D1j} = V_{1j} \tag{3}$$
$$V_{S2j} = V_{D2j} = V_{2j} \tag{4}$$
$$V_{S3j} = V_{D3j} = V_{2j} + V_{3j} \tag{5}$$
$$V_{Hj} = V_{H2} = V_{H3} = V_{H4} = V_{1j} + V_{2j} + V_{3j}. \tag{6}$$

Hence, the TSV on power switches and diodes $S_{1j}, D_{1j}, S_{2j}, D_{2j}, S_{3j}$, and $D_{3j}$ are as follows:

$$V_{\text{stand}j} = 2(V_{1j} + 2V_{2j} + V_{3j}). \tag{7}$$

The H-bridge inverter will see the full amplitude of the input voltage from the dc power supplies, so the amount of standing

**TABLE II**

**GENERATED OUTPUT VOLTAGE LEVELS BASED ON SWITCHING STATES OF THE PROPOSED CASCADED SD-MLI [SEE FIG. 2(a)]**

| No. | $V_o$ | First SD-MLI | Second SD-MLI | ... | $n^{th}$ SD-MLI |
|-----|------|--------------|--------------|-----|----------------|
| 1   | $V_{11}$ | 1 0 0 R R F 0 0 0 R R F | ... | 0 0 0 F R F |
| 2   | $V_{21}$ | 0 1 0 F F R 0 0 0 F R F | ... | 0 0 0 F R F |
| 3   | $V_{11} + V_{21}$ | 1 1 0 R F R 0 0 0 F R F | ... | 0 0 0 F R F |
| 4   | $V_{31} + V_{11}$ | 0 0 1 F R R 0 0 0 F R F | ... | 0 0 0 F R F |
| 5   | $V_{11} + V_{31} + V_{21}$ | 1 0 1 R R R 0 0 0 F R F | ... | 0 0 0 F R F |
| 6   | $V_{12}$ | 0 0 0 F R F 1 0 0 R R F | ... | 0 0 0 F R F |
| 7   | $V_{22}$ | 0 0 0 F R F 0 1 0 F R F | ... | 0 0 0 F R F |
| 8   | $V_{12} + V_{22}$ | 0 0 0 F R F 1 1 0 R R F | ... | 0 0 0 F R F |
| 9   | $V_{22} + V_{32}$ | 0 0 0 F R F 0 0 1 F R F | ... | 0 0 0 F R F |
| 10  | $V_{12} + V_{22} + V_{32}$ | 0 0 0 F R F 0 0 0 F R F | ... | 0 0 0 F R F |
| 11  | $V_{11} + V_{12}$ | 1 0 0 R R F 1 0 0 R R F | ... | 0 0 0 F R F |
| 12  | $V_{11} + V_{22}$ | 1 0 0 R R F 0 1 0 R R F | ... | 0 0 0 F R F |
| 13  | $V_{11} + V_{22} + V_{22}$ | 1 1 0 R R R 1 1 0 R R F | ... | 0 0 0 F R F |
| 14  | $V_{11} + V_{22} + V_{32}$ | 1 0 0 R R F 0 0 1 F R F | ... | 0 0 0 F R F |
| 15  | $V_{11} + V_{12} + V_{22} + V_{32}$ | 1 0 0 R R F 1 0 1 R R F | ... | 0 0 0 F R F |
| ...  |      | ...   | ...   | ... | ... |
| $6^n - 1 \sum_{j=1}^{n} V_{1j} + V_{2j} + V_{3j}$ | 1 0 0 R R F 1 0 0 R R F | ... | 1 0 0 R R F |

*R: Reverse, F: Forward*
The voltage seen by the power semiconductor devices is equal to

\[ V_{\text{stand}H} = 4(V_{1j} + V_{2j} + V_{3j}). \]

Therefore, the maximum standing voltage in the proposed topology is equal to

\[ TSV = \sum_{j=1}^{n} V_{\text{stand}j} + V_{\text{stand}H}. \]

As mentioned earlier, the H-bridge inverter shown in Fig. 2(b) suffers the peak of output voltage that leads to increase TSV value. Therefore, a recommended cascaded configuration to the reduction of TSV value is proposed in Fig. 2(c). This configuration uses \( n \) SD-MLI topology and \( n \) H-bridge inverter that leads to increasing the number of power switches with decreasing TSV magnitude.

The proposed extended MLI topology [shown in Fig. 2(b)] can generate different voltage levels at the output, which corresponds to the magnitudes of dc power supplies. Furthermore, the proposed extended MLI topology can operate in different modes: symmetric and asymmetric. In the proposed extended MLI topology, three different operation modes are introduced, the first proposed pattern (M1) is symmetrical, and two others (M2 and M3) are asymmetrical (given in Table III).

In the first mode (M1), all dc sources magnitudes in the proposed cascaded SD-MLI are equal with each other, which are equal to a per-unit voltage (\( V_{1j} = V_{2j} = V_{3j} = V_{dc} \)). For example, by assuming \( n = 2 \) in the proposed cascaded topology, namely, two of the proposed SD-MLIs are connected as a cascaded topology, the number of switching semiconductor devices is ten switches along with six dc sources. All dc sources magnitudes are the same with a value of \( V_{dc} \). Therefore, it can generate 13 voltage levels at the output, as shown in Table III.

Proposing symmetrical dc sources in MLIs can generate a low number of levels. Therefore, asymmetrical dc sources in MLIs are presented to create more voltage levels. Hence, two asymmetrical dc sources are presented for the proposed cascaded topology in the following. In the second proposed mode M2, in the first SD-MLI, the dc power supplies have the same voltage as the per-unit voltage \( V_{dc} \) and the other SD-MLIs have a magnitude \( 4^{-1} \), where \( j \) is the number of SD-MLIs. In this mode, assuming \( n = 2 \) (the number of used SD-MLIs), the number of semiconductor devices and dc power supplies are the same amounts with symmetric mode. This mode can create 31 voltage levels (see Table III), twice than the first mode.

In the third proposed mode (M3), the dc power supply voltages in the first SD-MLI are \( V_1 = V_{dc} \) and \( V_2 = V_{j} = 2V_{dc} \) and, for the other SD-MLIs, are \( V_1 = 6^{-1}V_{dc} \) and \( V_2 = 2V_{j} = 2(6^{-1}V_{dc}) \), where \( j \) is the number of SD-MLIs. Note that if the magnitudes of dc sources \( V_2 \neq V_3 \), the height/magnitude of steps in the output voltage waveform is not the same, so the created stepped voltage waveform by the proposed topology contains a high harmonic amplitude.

In the third mode, assuming \( n = 2 \), the number of semiconductor devices and dc power supplies are the same as the first and second modes, but this mode generates 71 voltage levels (see Table III). The main objective of the proposed modes is to keep the same number of semiconductor devices and dc power supplies to increase the number of voltage levels.

### III. Comparison of the Proposed Cascaded SD-MLI With Recent Cascaded MLIs

To demonstrate the advantages of the proposed cascaded SD-MLI, a comprehensive comparison is made among the proposed MLI topology, conventional MLIs, and well-known switched-diode-based MLIs. The comparative study is performed in terms of the number of IGBTs, power diodes, dc power supplies, variety of dc power supplies, peak switch voltage (PSV), and the magnitude of (TSV) to validate the new capabilities of the proposed topology compared to other MLI topologies, as shown in Table IV.

Fig. 3(a) shows that the proposed cascaded SD-MLI in symmetric and asymmetric modes (M1–M3) can create a large number of levels has a significant difference in the required number of switches than conventional MLIs and has a reasonable difference with presented switched-diode-based MLIs [25]–[30]. Fig. 3(b) reports the variation of the number of IGBTs to generate different levels for the proposed cascaded SD-MLI and other MLIs. As can be seen in Fig. 3(b), the proposed cascaded SD-MLI (M1–M3) requires a fewer number of IGBT than other conventional topologies and switched-diode-based MLIs. Also, the proposed SD-MLI is reduced the number of driver circuits due to reducing the number of IGBTs because each IGBT uses a gate driver.

Fig. 3(c) compares the required number of power diodes for the proposed SD-MLI topology and other MLIs. As highlighted in Fig. 3(c), the proposed cascaded SD-MLI reduces the number of diodes in comparison to other MLIs based on the suggested third method (M3), which has a low amount in comparison with other MLIs except (R14). Although the proposed topology utilizes discrete diodes instead of power switches, still, it requires a low number of diodes than other presented MLIs.

From Fig. 3(d), it is evident that the proposed SD-MLI topology in symmetrical dc sources (M1) to create the same voltage levels requires the same number of dc power supplies in comparison to other MLI topologies. For asymmetrical dc source, it reduces dc sources count than [9], [12], except for CHB (R4) and presented topologies in [15] and [25].

One of the factors that impact the cost of cascaded MLIs is the variety of dc power supplies. This factor has been introduced in [9] for the first time. \( N_{\text{variety}} \) is the variety of dc power supplies or the number of different voltage magnitudes of the used dc power supplies in cascaded MLIs. As can

### Table III

| Modes | DC Magnitudes | \( V_{\text{emax}} \) | \( N_j \) | TSV |
|-------|---------------|-----------------|--------|-----|
| M1    | \( V_{1j} = V_{2j} = V_{3j} = V_{dc} \) | \( 3nV_{dc} \) | \( 6n+1 \) | \( \frac{2n}{6}(N_N-1) \) |
| M2    | \( V_{1j} = 4^{-1}V_{dc} \) | \( 4^n-1) \) | \( 2V_{dc} \) | \( 2(4^n-1) \) | \( \frac{2n}{6}(N_N-1) \) |
| M3    | \( V_{2j} = 2V_{dc} \) | \( 6^n-1 \) | \( 2V_{dc} \) | \( 2(6^n-1) \) | \( \frac{2n}{6}(N_N-1) \) |
Fig. 3. Comparison studies. (a) Variation of $N_{\text{level}}$ against $N_{\text{switch}}$. (b) Variation of $N_{\text{level}}$ against $N_{\text{IGBT}}$. (c) Variation of $N_{\text{level}}$ against $N_{\text{diode}}$. (d) Variation of $N_{\text{level}}$ against $N_{\text{dc}}$. (e) Variation of $N_{\text{level}}$ against $N_{\text{variety}}$. (f) Variation of $N_{\text{level}}$ against PSV. (g) Variation of $N_{\text{level}}$ against TSV.

TABLE IV

All Required Parameters of Presented MLIs for Comparison Study Correspond to Their Magnitude DC Power Supplies

| Topologies | Methods | $N_{\text{m},A}$ | $N_{\text{IGBT}}$ | $N_{\text{diode}}$ | $N_{\text{dc}}$ | $N_{\text{variety}}$ | PSV | TSV (p.u.) |
|------------|---------|----------------|------------------|------------------|----------------|----------------|-----|----------|
| NPC       | R1      | 2(N$_{+1}$ - 1) | 2(N$_{+1}$ - 1) | 2(N$_{+1}$ - 1) | (N$_{+1}$ - 1)/2 | 1               | $V_d$ | (N$_{+1}$ - 1) |
|           | R2      | 2(N$_{+1}$ - 1) | 2(N$_{+1}$ - 1) | 2(N$_{+1}$ - 1) | (N$_{+1}$ - 1)/2 | 2               | $V_d$ | 2(N$_{+1}$ - 1) |
| CHB       | R3      | 6(N$_{+1}$/3 - 1)/5 + 3 | 6(N$_{+1}$/3 - 1)/5 + 3 | 6(N$_{+1}$/3 - 1)/5 + 3 | (N$_{+1}$/3 - 1)/2 | 1                           | $V_d$ | 2(N$_{+1}$/3 - 1)/2 |
|           | R4      | 5(log$^{(1/2)}$ - 1) - 9 | 5(log$^{(1/2)}$ - 1) - 9 | 5(log$^{(1/2)}$ - 1) - 9 | (log$^{(1/2)}$ - 1) - 8 | 1                           | $V_d$ | (log$^{(1/2)}$ - 1) - 8 |
| BUMLI     | R5      | 12(N$_{+1}$/6 - 1)/8 | 12(N$_{+1}$/6 - 1)/8 | 12(N$_{+1}$/6 - 1)/8 | (N$_{+1}$/6 - 1)/2 | 1                           | $V_d$ | 12(N$_{+1}$/6 - 1)/2 |
|           | R6      | 11(N$_{+1}$/6 - 1)/8 | 11(N$_{+1}$/6 - 1)/8 | 11(N$_{+1}$/6 - 1)/8 | (N$_{+1}$/6 - 1)/2 | 1                           | $V_d$ | 11(N$_{+1}$/6 - 1)/2 |
| DCMLI     | R7      | 9(N$_{+1}$/6 - 1)/2 | 9(N$_{+1}$/6 - 1)/2 | 9(N$_{+1}$/6 - 1)/2 | (N$_{+1}$/6 - 1)/2 | 2                           | $V_d$ | 9(N$_{+1}$/6 - 1)/2 |
|           | R8      | 6(N$_{+1}$/6 - 1)/2 | 6(N$_{+1}$/6 - 1)/2 | 6(N$_{+1}$/6 - 1)/2 | (N$_{+1}$/6 - 1)/2 | 2                           | $V_d$ | 6(N$_{+1}$/6 - 1)/2 |
|           | R9      | 7(N$_{+1}$/6 - 1)/2 | 7(N$_{+1}$/6 - 1)/2 | 7(N$_{+1}$/6 - 1)/2 | (N$_{+1}$/6 - 1)/2 | 2                           | $V_d$ | 7(N$_{+1}$/6 - 1)/2 |
|           | R10     | 7(N$_{+1}$/6 - 1)/2 | 7(N$_{+1}$/6 - 1)/2 | 7(N$_{+1}$/6 - 1)/2 | (N$_{+1}$/6 - 1)/2 | 2                           | $V_d$ | 7(N$_{+1}$/6 - 1)/2 |
|           | R11     | (N$_{+1}$/2) - 3 | (N$_{+1}$/2) - 3 | (N$_{+1}$/2) - 3 | (N$_{+1}$/2) - 3 | 1                           | $V_d$ | (N$_{+1}$/2) - 3 |
|           | R12     | 10(log$^{(1/2)}$ - 1) | 10(log$^{(1/2)}$ - 1) | 10(log$^{(1/2)}$ - 1) | 10(log$^{(1/2)}$ - 1) | 1                           | $V_d$ | 10(log$^{(1/2)}$ - 1) |
|           | R13     | 3(N$_{+1}$/3 + 16/4) | 3(N$_{+1}$/3 + 16/4) | 3(N$_{+1}$/3 + 16/4) | 3(N$_{+1}$/3 + 16/4) | 3                           | $V_d$ | 3(N$_{+1}$/3 + 16/4) |
| MLI       | R14     | (N$_{+1}$/3 + 16/4) | (N$_{+1}$/3 + 16/4) | (N$_{+1}$/3 + 16/4) | (N$_{+1}$/3 + 16/4) | 3                           | $V_d$ | (N$_{+1}$/3 + 16/4) |
|           | R15     | (N$_{+1}$/2) - 3 | (N$_{+1}$/2) - 3 | (N$_{+1}$/2) - 3 | (N$_{+1}$/2) - 3 | 3                           | $V_d$ | (N$_{+1}$/2) - 3 |
|           | R16     | (N$_{+1}$/2) - 3 | (N$_{+1}$/2) - 3 | (N$_{+1}$/2) - 3 | (N$_{+1}$/2) - 3 | 3                           | $V_d$ | (N$_{+1}$/2) - 3 |

see from Table IV and Fig. 3(e). $N_{\text{variety}}$ for all symmetrical cascaded MLIs is 1.0 because all used dc power supplies have the same magnitude. Asymmetrical cascaded MLIs require multiple dc power supplies with different voltage magnitudes, so these topologies have different variety of dc sources that are directly related to their amplitudes.

Fig. 3(f) shows the comparison of PSV of the proposed topology and other MLIs. As can see from this figure, the PSV’s value in the most of presented MLIs, such as the proposed SD-MLI (M1-M3) and (R5, R6, R11, R14–R16), is high because they use an H-bridge inverter in their circuits. Low PSV in symmetrical mode is for conventional topologies (NPC, FC, and CHB) and in symmetrical mode is for (R4) and (R10).

The comparison of TSV’s value in the proposed cascaded SD-MLI and all MLIs, as mentioned earlier, versus the number of levels is indicated in Fig. 3(g). The NPC, FC, CHB, and MLIs [9] have a low TSV’s value, the proposed topology (M2) [15], [25], [26] has an average quantity to generate a large number of levels, and other topologies have high TSV’s value.

Besides, a comparison is made among the proposed SD-MLI with other MLIs to create 11-level. The proposed 11-level SD-MLI consists of basic SD-MLI and an H-bridge with three dc sources with magnitudes of 1:2:2. Table V shows the comparison results of 11-level SD-MLI with other MLIs under the same condition. Note that some of the presented MLI topologies can generate 15 or 17 voltage levels, but, in this comparison, the magnitude of dc sources is set to create 11 levels. Also, some presented MLIs cannot make 11 levels accurately and generate 13 levels.

IV. Power Losses Analysis

The power losses are separated into two types: conduction and switching losses [13]–[20]. Conduction losses are determined by the ON-state of switches and diodes in the current...
TABLE V

| Topologies | N_{on} | N_{driver} | N_{IGBT} | N_{diode} | N_{dc} | N_{cap} | PSV | TSV |
|------------|--------|------------|----------|-----------|-------|---------|-----|-----|
| 2019 [22] | 11     | 17         | 17       | 1         | 1     | 5       | 3V_d | 33V_d |
| CHB       | 11     | 12         | 12       | -         | 3     | -       | 3V_d | 20V_d |
| 2019 [34] | 11     | 12         | 12       | -         | 1     | 4       | 2V_d | 33V_d |
| 2020 [31] | 11     | 9          | 9        | 4         | 3     | -       | 4V_d | 18V_d |
| 2019 [32] | 1      | 8          | 11       | -         | 2     | 4       | 1    | 6V_d  | 30V_d |
| SD-MLI    | 11     | 7          | 7        | 3         | 3     | -       | 5V_d | 34V_d |
| 2014 [10] | 13     | 12         | 12       | -         | 4     | 0       | 3V_d | 24V_d |
| 2015 [11] | 13     | 10         | 10       | -         | 4     | 0       | 6V_d | 20V_d |
| 2016 [13] | 13     | 8          | 10       | -         | 4     | 0       | 6V_d | 20V_d |
| 2017 [15] | 13     | 11         | 11       | -         | 2     | 2       | 2V_d | 35V_d |
| 2016 [16] | 13     | 10         | 12       | -         | 2     | 2       | 2V_d | 37V_d |
| 2017 [17] | 13     | 8          | 10       | -         | 4     | 0       | 6V_d | 18V_d |
| 2019 [18] | 13     | 10         | 10       | -         | 4     | 0       | 6V_d | 30V_d |
| 2019 [19] | 13     | 10         | 10       | -         | 2     | 2       | 2V_d | 27V_d |
| 2019 [20] | 13     | 10         | 10       | -         | 4     | 0       | 6V_d | 20V_d |
| 2019 [33] | 13     | 10         | 10       | -         | 2     | 2       | 2V_d | 20V_d |

Similarly, turn-off power losses $P_{sw,off}$ are

$$P_{sw,off,n} = \frac{v_{stand,n}I_{off}}{6}$$

where $v_{stand,n}$, $I$, $t_{on}$, and $t_{off}$ are the standing voltage of switches, the flowing current by the switch, and ON-state and OFF-state of switch, respectively. The sum of switching losses ($P_{sw,n}$) for each power switch is computed as follows:

$$P_{sw,n} = f_s(P_{sw,on,n} + P_{sw,off,n}) = \frac{v_{stand,n}I(t_{on} + t_{off})f_s}{6}$$

where $f_s$ is the switching frequency of power switches. Assuming $t_{on} = I_{off}$, (15) can be written as

$$P_{sw,n} = \frac{I_{on}}{3} \times f_s \times v_{stand,n}$$

By considering $I(t_{on})/3 = A$ as a constant, (16) can be written as

$$P_{sw,n} = A \times f_s \times v_{stand,n}$$

By using (7) and (8), the switching losses for 11-level SD-MLI $P_{sw,SD-MLI}$ can be calculated as

$$P_{sw,SD-MLI} = A \times (f_s(V_1 + 2V_2 + V_3 + 4f_f(V_1 + V_2 + V_3))$$

where $f_f$ is the fundamental frequency that is a low frequency. By considering $V_1 = V_{dc}$ and $V_2 = V_3 = 2V_{dc}$ to generate 11 levels at the output, (18) can be written as

$$P_{sw,SD-MLI} = A \times V_{dc} \times (f_s + 20f_f)$$

$$= 7 \times A \times V_{dc} \times \left(f_s + \frac{20}{7}f_f\right).$$

For the reason that $f_s \gg (20/7)f_f$, (19) can be written as

$$P_{sw,SD-MLI} = 20 \times A \times V_{dc} \times f_s.$$

Similarly, by using (17), the switching losses for an 11-level CHB-MLI $P_{sw,CHB}$ will be

$$P_{sw,CHB} = 40 \times A \times V_{dc} \times f_s.$$

Comparing (20) and (21), the switching losses of proposed 11-level SD-MLI are much lower than an 11-level CHB-MLI. Therefore, the total losses of the proposed cascaded SD-MLI considering (12) and (17) are obtained as follows:

$$P_{loss} = P_{sw,con} + P_{sw,n}.$$
configuration can be developed for the proposed cascaded SD-MLI by including more PV panels for other input dc source requirements.

In the proposed SD-MLI and cascaded SD-MLI topologies, such as the topologies presented in [12], [27], [28], [30], and [32], the H-Bridge converter at the end is used to change the output voltage polarity and create zero levels. The limitation of the proposed topology is requiring H-bridge inverter that their switches should endure peak output voltages. Hence, the proposed topology has any superiority in this regard.

As a result, the voltage rating of the used power switches in the proposed topologies should determine to clarify the superior advantages of the proposal. Assuming the highest standard commercial voltage of IGBT be $V_{\text{IGBT,cc}}$, the maximum operating voltage of the proposed MLI will be equal to $\sqrt{1.5} \times V_{\text{IGBT,cc}}/\gamma$, and $\gamma$ is a factor to ensure the safe operation of the IGBT that is typically assumed $\gamma = 1.7$. Therefore, by the determination of the maximum IGBT voltage, the operation voltage of the proposed topology is obtained. The determination of IGBTs voltage of the proposed topology is calculated for medium-voltage applications for 11-level SD-MLI and 31- and 71-level cascaded topologies. By assuming that the maximum IGBTs voltage in medium-voltage applications is 3.3 kV, the operation voltage of three-phase rms voltage will be 2.3 kV. For the single-phase system, the operation phase voltage rms will be 1328 V or a maximum voltage of 1878 V.

Note that, in industrial applications, usually, the number of voltage levels of MLIs is limited to 11 or 13 levels unless the specific applications need a high-quality waveform. Therefore, the component’s cost comparison is conducted among the proposed 11-level SD-MLI and other 11- or 13-level MLIs for medium-voltage applications.

Therefore, for such an rms voltage of 1328 V, the dc power supply magnitudes for 11-level SD-MLI will be $V_1 = 375.6$ V and $V_2 = V_3 = 751.2$ V. Thus, for the proposed topology, the voltage rating of IGBTs is calculated based on (3)–(6) and considering $V_{\text{IGBT,cc}}$ that are presented in Table VI. The costs of required IGBTs and driver circuits of single-phase proposed 11-level SD-MLI and recent 11- and 13-level MLIs [15], [22], [31], [34] are compared in Table VI. The commercial IGBT’s voltage with the nominal current of 400 A is made by MITSUBISHI company. The prices of IGBTs (single pack) and gate driver circuits (Semikron, dual pack) and the power diode (single pack, Mouser Electronics) are in USD as a role example [35]. Viewing this table, by comparing the cost of proposed 11-level topology with other 11- or 13-level MLIs, the cost of the proposed SD-MLI is less than the other recently presented MLIs.

The proposed cascaded topologies consist of two series of basic SD-MLIs [see Fig. 2(b)]: 31-level (see Table III, M2) and 71-level (see Table III, M3). Therefore, for the maximum voltage of 1878 V, the dc power supply magnitudes for 31-level cascaded topology are $V_{S_{1,1}} = 125.2$ V, $V_{S_{1,2}} = V_{S_{1,3}} = 250$ V, $V_{S_{2,1}} = V_{S_{2,2}} = 500.8$ V for the second SD-MLI. For 71-level proposed cascaded topology, the dc power supply magnitudes are $V_{S_{1,1}} = 1001.6$ V, $V_{S_{1,2}} = V_{S_{1,3}} = 1878$ V, $V_{S_{2,1}} = V_{S_{2,2}} = V_{S_{2,3}} = 3300$ V for the second SD-MLI. Therefore, based on the commercial voltage of IGBTs, the different rated voltages of IGBTs for 31- and 71-level SD-MLIs are illustrated in Table VII.
Both 31- and 71-level SD-MLIs require six IGBTs for two series SD-MLIs and four IGBTs for the H-bridge converter, which is in the output. According to Table VI, the maximum standing voltage is related to four switches ($H_1$–$H_4$). As mentioned earlier, the four power switches of H-bridge converter ($H_1$–$H_4$) operate in fundamental frequency and zero-state switching.

VI. SIMULATION AND EXPERIMENTAL VALIDATIONS

Simulation and experimental results are presented to validate the performance of the proposed topology, in two different case studies. In the first, the performance of 11-level SD-MLI is evaluated, and then, 31-level cascaded SD-MLI (consists of two SD-MLIs) is tested. The simulation results are performed in the MATLAB environment. Two prototypes of the proposed 11-level SD-MLI and 31-level cascaded SD-MLI are built using IGBTs as the switching devices. The experimental parameters are listed in Table VIII.

Basically, the conventional modulation techniques to commutate MLIs are based on PWM, fundamental frequency switching technique, or staircase modulation [36]. In this article, the staircase modulation technique is applied for the proposed SD-MLI and cascaded topology. The staircase strategy uses a sinusoidal stepped waveform with the fundamental frequency that illustrates in Fig. 6. In this method, by considering the desired total number of levels $N_L$ in the proposed topologies, the switching angels are calculated for

\[
0 < \alpha_j < \pi/2 \text{ as follows:}
\]

\[
\alpha_j = \sin^{-1}\left(\frac{j - 0.5}{N_L}\right) \quad \text{for } j = 1, 2, \ldots, \frac{N_L - 1}{2}.
\]

Then, the switching angles generate the switching pulses of the proposed MLI, which are determined separately based on the switching states in Table II. The step timing is chosen based on the output frequency, and it is calculated offline.

The 89C52 microcontroller by ATMEL Company is applied to implement this technique. The 11- and 31-level switching states are programmed in EPROM of the microcontroller. Then, the switching angles transfer to the microcontroller port. Finally, the switching pulses move to IGBTs of prototypes. HGTPI0N40CID IGBT power switches are used to switch dc power supplies to deliver the output voltage to 250-$\Omega$, 20-mH ac load.

A. Proposed 11-Level SD-MLI

The proposed 11-level SD-MLI consists of one basic SD-MLI and an H-bridge inverter. Therefore, it has seven IGBTs, three power diodes, and three dc power supplies. In the simulation and experimental results, the third proposed operation mode (M3) is applied. In this mode, considering $n = 1$, the values of dc power supplies are $V_1 = 10$ V and...
Fig. 7. Response of proposed 11-level SD-MLI to three different modulation index. (a) Zoomed-in view for \( M = 1.0 \) to \( M = 0.8 \). (b) Zoomed-in view for \( M = 0.8 \) to \( M = 0.7 \). (c) Zoomed-in view for \( M = 0.7 \) to \( M = 1.0 \).

Fig. 8. Dynamic response of proposed 11-level SD-MLI. (a) Output frequency changes from 50 to 100 Hz at \( t = 50 \) ms. (b) Operation under nonlinear loading at \( t = 50 \) ms. (c) Sudden load changes from pure \( R \) load to an \( RL \) load at \( t = 50 \) ms.

\[ V_2 = V_3 = 20 \text{ V.} \] Therefore, the proposed SD-MLI generates 11-level with a peak of 50 V at the output.

The simulation and experimental results of the 11-level SD-MLI are illustrated in Fig. 5. Fig. 5(a), (c), and (e)–(g) indicates the simulation results, and Fig. 5(b) and (d) shows the experimental results. Fig. 5(a) and (b) shows the generated output voltage waveform before H-bridge inverter by the proposed 11-level SD-MLI in the simulation and experimental tests, respectively. It is observed that the SD-MLI generates only five positive-voltage levels. Fig. 5(c) and (d) indicates the simulation and experimental tests for the load voltage and load current generated by the proposed 11-level SD-MLI for the ac load. The maximum output voltage for the experimental results is 49 V with a maximum current of 198 mA, which gives the voltage and current rms values of 35.2 V and 145 mA, respectively. The THD’s value of the load voltage and current for the simulation results of 11-level SD-MLI is 8.45% and 3.36%, and the experimental results are 9.55% and 4.48%, respectively. Furthermore, the simulation results of the current waveform for three used power diodes \( D_1, D_2, \) and \( D_3 \) are shown in Fig. 6(e)–(g), respectively.

The efficiency (\( \eta \)) of the MLIs are obtained based on the input power (\( P_{\text{in}} \)) and the output power (\( P_{\text{out}} \)) by measuring them \( \eta = \frac{P_{\text{out}}}{P_{\text{in}}} \). The input and output powers are measured, and the efficiency of 11-level SD-MLI is given in Table IX. The input power is a dc power that is obtained by the summing of three input dc power supplies (5.25 W) to produce 11 voltage levels by the proposed SD-MLI, as shown in Table IX. The applied staircase modulation technique has a low switching frequency, which leads to low power losses. Therefore, the efficiency of the proposed topology is 94.3%, which is a high efficiency for MLIs.

### B. Dynamic Test Scenarios

The dynamic response of the proposed 11-level SD-MLI is tested in different scenarios: modulation index changes, output frequency changes, operation under nonlinear loading, and sudden load change. The simulation results of modulation index changes are shown in Fig. 7. Fig. 7(a) shows the
output voltage and current waveform for modulation indexes, 1.0–0.8, with an \( RL \) load at \( t = 1 \) s. As can see from this figure, the output voltage levels are deduced from 11 levels to nine levels. Then, the modulation index is changed from 0.8 to 0.7 at \( t = 2 \) s, and voltage levels are reduced to seven from nine levels, as shown in Fig. 7(b). Finally, the modulation index changing is returned from 0.7 to 1.0 \( t = 3 \) s, and the changing output voltage and current for this case are depicted in Fig. 7(c). Simulations of the output frequency changes, operation under nonlinear loading, and sudden load change for the proposed topology are illustrated in Fig. 8. Note that the step changes occurred at \( t = 50 \) ms for these tests.

The simulation results of output frequency change are presented in Fig. 8(a). The output frequency changes from 50 to 100 Hz. The proposed topology can operate at 100-Hz frequency without any variation in the shape of the output voltage and current waveforms. Fig. 8(b) shows the operation of the proposed topology under nonlinear loading. The linear load is an \( RL \) load, and the nonlinear load is an H-bridge diode that is switched to the output of the inverter at \( t = 50 \) ms. As can see from this figure, the output voltage waveform is generated without any shape changes, but the quality of the output current is declined, which contains a high THD’s value. Fig. 8(c) shows the simulation results of sudden load change for the proposed topology. The value of the load changes from a pure resistance load of 250 \( \Omega \) to an \( RL \) load of 250 \( \Omega \) and 100 mH. It is clear that the proposed topology remains in the steady state, and each output level keeps unchanged.

The proposed topology cannot operate in low power factors like other presented MLIs [25]–[27], [30], due to using diodes in its structures. The solution is replacing switch rather than diodes. The simulation results are presented for proposed 11-level SD-MLI under different power factors, as shown in Fig. 9. As can see from this figure, the proposed topology can operate in a low power factor and handle the back-flow current.

C. Proposed 31-Level Cascaded SD-MLI

The performance of the proposed cascaded SD-MLI is evaluated by the simulation and experimental results for 31 levels. The proposed configuration consists of two proposed SD-MLIs and an H-bridge inverter at the output, which has ten IGBTs, six power diodes, and six dc power supplies. In the simulation and experimental evaluations, the second proposed operation mode (M2) is applied for generating 31 levels. Considering the operation mode (M2) with \( n = 2 \), the values of dc power supplies for the first and second SD-MLIs are given in Table VII. Consequently, the cascaded SD-MLI generates 31 levels with a peak of 300 V at the output.

Fig. 10 shows both simulation and experimental results of the 31-level cascaded SD-MLI. They correspond to the output voltage waveforms of the first SD-MLI (\( V_{o1} \)) [see Fig. 10(a) and (b)], the output voltage for the second SD-MLI (\( V_{o2} \)) [see Fig. 10(c) and (d)], the total voltage of the first and second SD-MLIs (\( V_{o} \)) [see Fig. 10(e) and (f)],
and the load voltage and current curves \((V_L)\) and \((I_L)\) [see Fig. 10(g) and (h)], respectively. It can see that the experimental results have a good agreement with the simulation results for the proposed cascaded 31-level topology. The maximum output voltage for the experimental results is 298.5 V, with a maximum current of 1.18 A, which gives the voltage and current rms values of 214.7 V and 0.85 A, respectively. The THD percentage of the load voltage and current for the simulation results of 31-level SD-MLI are 1.82% and 1.32%, and the experimental results are 2.1% and 1.46%, respectively.

Table X gives the efficiency of the proposed 31-level cascaded topology. The efficiency of the converter is 96.98%. The comparison of the efficiency in 11-level SD-MLI and 31-level cascaded SD-MLI shows that the 31-level cascaded topology has high efficiency. It means that the power losses in the 31-level cascaded topology are less than 11-level SD-MLI.

### VII. Discussion

The performance of the proposed topologies was validated through both simulation and experimental analysis. The proposed topologies can generate all levels based on presented theoretical concepts. The proposed cascaded topology can produce a large number of levels compared with other topologies because it requires a low number of power switches. Using lower power switches makes the proposed topology more efficient, highly reliable, and low cost.

The result findings of comparison studies indicate that the proposed topology can be applied to PV systems and replace the classical CHB inverter because the final cost has been reduced due to the reduced number of components so that the control of the proposed topology will be simpler.

The proposed topology like other presented switched-diode MLIs [25]–[27], [30] cannot operate in low power factors due to using the discrete diodes in its power circuits. The back-flow current capability is usually created when MLIs are connected to the grid. The grid-based MLI systems have a high power factor, and the need for back-flow current is rare. Replacing the switch rather than the diode is an alternative solution. Therefore, the proposed topology can run and handle the back-flow current to work in a low power factor.

### VIII. Conclusion

In this article, a reduced switched-diode-based MLI was proposed for cascaded configurations. The presented fundamental SD-MLI comprises three power switches, three dc sources, and three power diodes that generate five positive-voltage levels. The proposed fundamental topology was developed for cascaded MLIs to create a large number of levels while reducing the number of devices. Based on the presented comparison results of the proposal with other MLIs, the proposed SD-MLI requires fewer components to generate a high number of levels. Furthermore, this article has demonstrated that the proposed cascaded topologies have reduced TSV value than some presented MLIs in the literature. The proposed cascaded topologies like other reported cascaded MLIs possess some limitations; in particular, they still require a wider dc voltage source variety for the proposed asymmetric operation mode. However, the number of devices deducted, and the solution is using dc/dc converters for the regulation of input dc voltage sources.

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