An asynchronous dual switch envelope tracking supply modulator with 86% efficiency

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Abstract: An asynchronous dual-switch hybrid envelope tracking (ET) supply modulator is proposed in this paper. Two high-efficiency switching amplifiers (SA) working at different speed are adopted to reduce the current supplied by the linear amplifier (LA), which improves the efficiency of the supply modulator. A highly reliable control circuit is presented to make the SAs work asynchronously. Measured with 20 MHz LTE signal, the proposed supply modulator’s average efficiency reaches 86% when the output power is 29.7 dBm. The supply modulator is fabricated in 180 nm CMOS technology with 0.7 x 0.7 mm² die area.

Keywords: Envelope tracking, Power Amplifier, CMOS, Switch

Classification: Integrated circuits

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1 Introduction

In the high-speed wireless communication systems, the modulated radio frequency (RF) signals usually have a high peak to average power ratio (PAPR) [1]. The high PAPR signals make the power amplifiers mainly work at the power back-off level,
with a relatively low efficiency. For the upcoming 5G communication system, this problem is still serious. To enhance the efficiency of power amplifiers at the power back-off point, envelope tracking (ET) is an attractive technique. Compared with the Doherty power amplifier, the ET technique does not need λ/4 transmission lines, which makes the system compact. Therefore, it is suitable for the mobile equipment. Furthermore, the technique does not require the output voltage of the supply modulator to follow the signal’s envelope accurately, compared with the envelope elimination and restoration (EER) technique [2]. The supply modulator is the key block for the ET system as shown in Fig. 1 and the bandwidth and the efficiency are the key specifications. A hybrid structure for the supply modulator is proposed in [3]. A switching amplifier (SA) is used to provide current around DC with high efficiency while a linear amplifier (LA) is used to provide current with broad bandwidth. The LA, which is usually designed in Class-AB mode, has a lower efficiency than the SA. To minimize the current provided by the LA and enhance the efficiency of the supply modulator, a digitally assisted dual-switch structure is proposed in [4] and a two-phase switching structure is proposed in [5]. An improved dual-switch topology based on adaptive slew rate controller and multi-level comparators are used in [6, 7]. However, the complexity of the circuit increases as many comparators and control circuits are used. The reliability is significantly reduced when the voltage supply or process corner varies.

In this paper, an asynchronous dual-switch structure supply modulator is proposed. The proposed structure simplifies the cooperation of the two SAs and reduces the current supplied by the LA. The overall efficiency of the supply modulator is improved, and a better figure of merit (FoM) is achieved. The supply modulator is fabricated in a standard 180nm bulk CMOS technology. Measurement results show that the supply modulator has an average efficiency of 86% when the output power is 29.7 dBm, which is measured with a 20 MHz LTE signal. At a same output power level, the result increases by 8% compared with a single-switch hybrid supply modulator, which is fabricated by the same CMOS process.

The design principle of the asynchronous dual-switch supply modulator is
analyzed in Section 2. Section 3 introduces the implementation of the proposed supply modulator in detail. The measurement result is given in Section 4. Section 5 concludes the paper.

2 The Design Principles of the Asynchronous Dual-Switch ET Supply Modulator

![Block Diagram of the Single-Switch ET Supply Modulator](image)

The block diagram of the single-switch ET supply modulator.

The structure of the conventional hybrid single-switch ET supply modulator is shown in Fig. 2. The output current is provided by the SA and the LA. The efficiency of the SA is higher. However, the slew rate of it is lower. Oppositely, the LA has lower efficiency and higher slew rate. Therefore, the SA contributes the low-frequency part of the output current and the LA outputs the high-frequency part. The efficiency of the supply modulator ($\eta_{SM}$) can be expressed as

$$\eta_{SM} = \frac{1}{\alpha + \frac{1-\alpha}{\eta_{sw} \eta_{lin}}}$$

(1)

where the $\eta_{sw}$ and $\eta_{lin}$ represent the efficiency of SA and LA, respectively. The $\alpha$ represents the proportion of the high-efficiency current of the SA ($I_{sw}$) in the output current ($I_{out}$), while the proportion of LA’s current ($I_{lin}$) is $1-\alpha$. To improve the $\eta_{SM}$, $\alpha$ should be increased. However, the working bandwidth decreases if the size of the SA is increased directly. To overcome the problem, another SA with smaller size and higher speed can be used to enhance the portion of the high-efficiency current. The key problem is the cooperation of the two SAs.

In the time domain, the output current of the single-switch supply modulator is shown in Fig. 3 (a). The current delivered to the load is $I_{out}$, which is the black line. The current supplied by SA is $I_{sw}$, which is the yellow region. The LA delivers current at the red region, when the $I_{load}$ is larger than $I_{sw}$ and the envelope voltage rises faster than the slew rate of the SA. Meanwhile, it sinks current at the blue region when the $I_{load}$ is smaller than $I_{SW}$, as the $I_{SW}$ cannot be reduced suddenly. The
ISW contributes the main current of the low-frequency part, while the LA outputs the high-frequency current and maintains that the output voltage envelope follows the input voltage.

To reduce the low-efficiency current in the red region, another SA (SA₂) with faster speed can be controlled to deliver part of the high-frequency current, which is originally provided by LA as shown in Fig. 3(b). To achieve a higher slew rate, the SA₂ should have a smaller size. The SA₂ turns on and off faster and reduces the red region, which means the low-efficiency current. The asynchronous working mode is indispensable, as the two SAs work at the different regions in the frequency domain. The first slower SA (SA₁) contributes the low-frequency current around DC. Then, the faster SA₂ contributes the current in the middle-frequency band. Finally, the LA gives the highest frequency current.

The efficiency of the dual-switch supply modulator can be expressed as

\[
\eta_{SW} = \frac{1}{\eta_{sw} + \frac{1 - \alpha_{SA1} - \alpha_{SA2}}{\alpha_{SA1} + \alpha_{SA2}}} \tag{2}
\]

The \(\alpha_{SA1}\) represents the proportion of the current provided by the SA₁ and \(\alpha_{SA2}\) represents that provided by SA₂. The proportion of the current provided by LA is reduced, which means better \(\eta_{sw}\). Though the proportion of the LA’s current is reduced to a very small part, the LA is retained in the hybrid structure. The LA can further smooth the ripple of the SAs’ output current and enhance the working bandwidth compared with switch-only structure [8, 9].

3 The Design of the Proposed Asynchronous Dual-switch ET Supply Modulator

3.1 Principle of the System

A dual-switch ET supply modulator, which is based on the principle described in Section II, is implemented in 180nm CMOS technology. The schematic of the proposed ET supply modulator is shown in Fig. 4. The input envelope signal is amplified by an operation amplifier. The gain is determined by the feedback resistors \(R₁\) and \(R₂\). The transistors \(M₁ \sim M₂\) make up the Class AB LA and deliver the high bandwidth linear current. The transistors \(M₃ \sim M₄\) make up the current

\[\text{Fig. 3.} \quad \text{The output current of the supply modulator with (a) single switching amplifier and (b) dual switching amplifier.}\]
sense unit and control the $SA_1$. The $SA_1$ consists of a hysteresis comparator, drivers and a switching stage. The switching stage consists of transistors $M_7 \sim M_8$ and delivers current with low frequency. The $SA_2$ consists of a controller, a driver and a switching stage. The $SA_2$ is controlled by the $LA$’s output voltage ($V_{out}$) and the outputs voltage of hysteresis comparator in $SA_1$. The transistors’ size of the switching stage is smaller than that in $SA_1$, which enables a higher switching speed. The output currents of the $LA$ ($I_{lin}$), $SA_1$ ($I_{SA1}$) and $SA_2$ ($I_{SA2}$) make up the supply modulator’s output current. Instead of transistors, a diode is used in $SA_2$ to avoid the direct through current from $SA_1$ to $SA_2$.

**Fig. 4.** The schematic of the proposed dual-switch supply modulator.

**Fig. 5.** (a) The schematic of the control and (b) the operation region.

The operation of the $SA_2$ is shown in Fig. 5. The schematic of the controller is shown in Fig. 5(a). The output of the $LA$ is connected to a charge storage capacitor...
($C_{\text{charge}}$) through a resistor ($R_4$). When the $V_{\text{out}}$ rises up, the capacitor is charged and there is a positive voltage on the input of the hysteresis comparator. On the contrary, when the $V_{\text{out}}$ decreases, the input of the hysteresis comparator is negative. The output of the hysteresis comparator and the $V_{SA1}$ pass an AND gate. The output of the AND gate control the switching stage.

In region A of Fig. 5(b), the output voltage increases and the $C_{\text{charge}}$ is charged. The $V_{SA1}$ is high and it is the same with $V_{SA2}$. Both of the SAs are turned on and output current. In region B, the $V_{\text{out}}$ decreases and the $C_{\text{charge}}$ is discharged. The $SA2$ is turned off with the variation of the envelope. However, the $SA1$ with a slower speed is still on. In region C, the $V_{\text{out}}$ continues to decrease. Both of the $SA1$ and $SA2$ are turned off. The $LA$ sinks the extra current of the $SA1$. In region D, though the $V_{\text{out}}$ increases, the remnant current of $SA1$ is still more than the output current. The $SA1$ is off and there is no need to turn on the $SA2$. Therefore, through the operation of AND gate, the $SA2$ is also closed. The $SA2$ only outputs current in region A and B. Therefore, it reduces the current in the red region.

![Fig. 6. The voltage and current waveforms of each node in time domain.](image)

Voltage and current waveforms of each node in the time domain for an envelope signal are shown in Fig. 6. The switching time of the $V_{SA2}$ is faster than that of $V_{SA1}$. Therefore, the $I_{SA1}$ contributes the main current around DC and the $I_{SA2}$ contributes the peak current in high frequency.

From the above description, the proposed controller turns on the $SA2$ when the linear amplifier delivers current, and closes it before the $SA1$ closes when the envelope voltage decreases. Therefore, the $SA2$ is able to track the high-frequency envelope signal and reduce the current by the $LA$. The efficiency is enhanced as the proportion of current provided by the SAs is improved. The operation of the controller is charge-based and is independent with the variation of the technology or supply voltage. This makes the controller less sensitive to the temperature variation and the pulling of the power amplifier’s large output signal.
3.2 The linear amplifier

The LA consists of an input amplifier, a bias circuit and an output stage. The simplified schematic is shown in Fig. 7. To amplify the high-frequency signal and track the envelope, the operation amplifier adopts a source cross couple class AB differential amplifier as the first stage [10]. The source cross couple class AB amplifier has a low quiescent current when the high slew rate is required. The quiescent current is controlled by the $I_{bias}$. When input signal in the positive terminal is much larger than the minus terminal, half of the amplifier is cut off. The class AB amplifier provides much larger current than the class A amplifier [10]. The input amplifier only has 3.6 mA quiescent current. Due to the addition of $SA_2$, the output current of the LA decreases. Therefore, the size of the output stage is reduced and lower quiescent current is required with the same slew rate. Then the efficiency can be further improved. The bias stage gives a proper bias point to the output stage and makes the output stage work at class AB mode.

![Fig. 7. The simplified schematic of the LA.](image)

3.2 The hysteresis comparator

The hysteresis comparator consists of three stages as shown in the Fig. 8: the input stage, the judgement stage, the output stage. The input stage amplifies the input signal and improves the sensitivity of the judgement stage. The judgement stage is used to distinguish the relative magnitude of the differential input ports and give a judgement result. The transistors $M_6 \sim M_9$ forms a positive feedback to enhance the gain. If the transistors $M_6$ and $M_9$ have the same sizes, the comparator is an ideal comparator. On the other hand, if the transistors $M_7$ and $M_{10}$ have the different sizes, the comparator shows the hysteresis characteristic. The transistor $M_{11}$ shifts the output common mode voltage of the judgement stage’s to fit the output stage. The output stage converts the different judgement signal to a single-ended logic.
signal. It is made up by a different differential amplifier.

4 Measurement Result

The proposed supply modulator is fabricated in standard 180 nm CMOS technology. The die photo of it is shown in Fig. 9. The size of the chip is 0.7 x 0.7 mm\(^2\) including all pads. The supply modulator works with a 3.3 V supply. With a resistor load, the average efficiency of the supply modulator versus output power is shown in Fig. 10 and it achieves 86\% when the output signal is 29.7 dBm. Compared with the single-switch hybrid supply modulator, the efficiency increases by 8\%. As the LA is the Class AB mode amplifier, the efficiency of the LA drops when the output power decreases. Therefore, the efficiency of the whole supply modulator decreases at the low output power region. The decrease depends on the proportion of the LA’s output current in the modulator’s output current. Since we use two SAs to reduce the LA’s output current, the efficiency of the
proposed structure in the low power region shows obvious improvement compared with the single-switch structure. The efficiency is still more than 80% when the output power back off is 10 dB.

![Graph showing efficiency versus output power, with proposed dual-switch structure and single-switch hybrid structure compared.]

**Fig. 10**  The measured efficiency versus output power.

![Graph showing input and output voltage envelope waveform.]

**Fig. 11.**  The input and output voltage envelope waveform.

![Graph showing efficiency of power amplifier and ET system.]

**Fig. 12.**  The efficiency of the power amplifier and the ET system.
A commercial GaAs power amplifier (PA) is used to make up the ET system with the supply modulator. An envelope voltage signal of a 20 MHz LTE signal is used to test the envelope tracking capability. The input and output voltage waveforms are shown in Fig. 11. The amplification factor is set to one to give a better comparison, which is not the real situation. Measurement result shows that the ET supply modulator can track the 20 MHz LTE envelope signal accurately.

![Image](image1)

**Fig. 13.** The variation of ET system’s (a) AM-AM and (b) AM-PM.

![Image](image2)

**Fig. 14.** The measured AM-AM and AM-PM distortion.

| Reference    | Structure            | Bandwidth    | Pout (dBm) | Efficiency | Process  | FoM   |
|--------------|----------------------|--------------|------------|------------|----------|-------|
| PE2016 [8]   | Switch-only          | 10 MHz LTE   | 33.0 dBm    | 85.8%      | 0.18um CMOS | 28.31 |
| PE2016 [9]   | Dual-Switch          | 10 MHz LTE   | 31.8 dBm    | 86.5%      | 0.18um CMOS | 27.51 |
| ISSCC2015[11]| Hybrid with AC-coupling | 10 MHz LTE | 26.0 dBm    | 82%        | 0.13um CMOS | 21.32 |
| ISSCC2017[12]| Hybrid              | 40 MHz LTE   | 19.0 dBm    | 75%        | 28nm CMOS  | 22.83 |
| ISSCC2017[13]| Hybrid              | 20 MHz LTE   | 33.0 dBm    | 82%        | 0.5um CMOS  | 35.21 |
| ISSCC2017[14]| Hybrid with AC-coupling | 20 MHz LTE | 23.9 dBm    | 88.7%      | 65nm CMOS  | 27.58 |
| JSSC2017 [15]| Hybrid              | 13 MHz Sine  | 23.0 dBm    | 81%        | 0.13um CMOS | 20.75 |
| This work    | Hybrid with dual-switch | 20 MHz LTE | 29.7 dBm    | 86%        | 0.18um CMOS | 33.23 |
The maximum PAE of the GaAs PA is 56% with 27 dBm output power. The efficiency of the ET system increases the efficiency at the power back off region as shown in Fig. 12. At the 10 dB power back off point, the system’s efficiency is still more than 40%. Through the proper design, the supply modulator is also able to increases the linearity of the PA. The principle is shown in the Fig. 13. The measured AM-AM and AM-PM distortion of the ET system is shown in the Fig. 14.

The comparison with the state-of-the-art supply modulators is listed in the Table I. The proposed dual-switch ET supply modulator shows a good FoM. The FoM is calculated from

$$\text{FoM} = \eta \times P_{\text{out}}(\text{dBm}) \times \log_{10}(\text{Bandwidth(MHz)})$$

which includes the efficiency, output power and the working bandwidth.

## 5 Conclusion

A hybrid structure ET supply modulator with asynchronous dual SAs is presented. The proposed structure simplifies the cooperation of the two SAs and reduces the low-efficiency current provided by LA. The charge-based operation principle is robust and not associated with the process and temperature. Measured with 20 MHz LTE signal, the efficiency reaches 86% when it outputs 29.7 dBm power, which has a significant improvement than the single-switch structure.

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