Electrical isolation of dislocations in Ge layers on Si(001) substrates through CMOS-compatible suspended structures

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Abstract
Suspended crystalline Ge semiconductor structures are created on a Si(001) substrate by a combination of epitaxial growth and simple patterning from the front surface using anisotropic underetching. Geometric definition of the surface Ge layer gives access to a range of crystalline planes that have different etch resistance. The structures are aligned to avoid etch-resistant planes in making the suspended regions and to take advantage of these planes to retain the underlying Si to support the structures. The technique is demonstrated by forming suspended microwires, spiderwebs and van der Pauw cross structures. We finally report on the low-temperature electrical isolation of the undoped Ge layers. This novel isolation method increases the Ge resistivity to 280 $\Omega$ cm at 10 K, over two orders of magnitude above that of a bulk Ge on Si(001) layer, by removing material containing the underlying misfit dislocation network that otherwise provides the main source of electrical conduction.

Keywords: Ge, germanium, dislocation, conduction, etch, anisotropic, TMAH, RP-CVD

1. Introduction
The ambition of totally integrating all variations of micromechanical systems (MEMS) (sensors, actuators and structures) with electronics, optoelectronics and spintronics is well known and has generated considerable research effort. In working towards this goal, the simpler fabrication methods are easier to incorporate into mass fabrication. Suspended structures can be made thermally, electrically and/or structurally independent from their substrate and, when placed in vacuum, also independent of the ambient atmosphere. This decoupling of the suspended structure from its host can lead to a more rapid and higher sensitivity response in sensors and open the possibility to add new functionality to integrated systems. Examples of devices that benefit from being suspended include comb drive actuators [1, 2], resonant chemical sensors [3], high-$Q$ solenoids [4], micromirrors [1] and spiderweb bolometers [5].

Previously, the main method for producing suspended structures was bulk micromachining [6], where the bulk of the Si wafer is machined from the back side of a wafer to produce the features on the surface; the most basic structure fabricated in this manner is the freestanding membrane [7]. However, micromachining from the front surface is the favoured route to incorporate MEMS alongside CMOS, where the processing consists of defining the structural boundaries of the active layer and then removing the material from under the active layer. One method of fabricating suspended structures, largely independent of starting material used, is through dry etching where a combination of isotropic and anisotropic etch steps can release a defined structure [8]; however, this requires multiple expensive processing steps that often need high temperatures, e.g. oxide deposition. In utilizing cheap wet etchants, active layers are mainly made upon sacrificial layers, generally dielectrics, that can be selectively removed [6] due to their high etch selectivity.
in wet isotropic etchants [9]. Anisotropic etchants, such as potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH), have also been used to create suspended structures by a ‘brute-force’ etch against the etch-resistive \{111\} planes in Si(001) substrates [10, 11]. An alternative method has been to use a post-CMOS fabrication technique to create suspended micro-hotplates [12, 13], exploiting the underetching rates of a Si(001) substrate in TMAH [14–16]. This processing works on a Si(001) substrate by patterning the active layer, away from the surface \langle 110 \rangle directions, thus avoiding the \{111\} etch-resistive planes during the etching.

Germanium is extremely chemically resistive against KOH and TMAH [17], so is potentially an excellent material for this kind of micromachining. Germanium is also a logical supplement to enhance existing silicon semiconductor technologies, as its material behaviour is very similar to Si, and allows new functional devices that cannot be fabricated from Si alone [18]. High-quality crystalline Ge layers grown epitaxially on a Si(001) substrate can be fully relaxed, with sub-nm roughness and low defect densities [19]. Since the Ge is epitaxially grown on Si it has no adhesion issues, which sometimes can occur in metal mask layers [20], and can also be doped during epitaxy, thus avoiding additional implantation steps. In addition, Ge has been reported with spintronic [21], optical detection [22] and lasing [23] abilities and is an accommodating buffer for further SiGe layers [24, 25] and III–V materials on Si [26]. Epitaxial Ge on Si(001) is, however, plagued by electrical leakage due to conduction through the dislocation network still present in the layer [27–30]. Figure 1 shows the electrical circuit through which dislocations can potentially conduct. Within this network, two main components are present: (i) threading arms and (ii) the misfit interface. Generally, research efforts have focussed on reducing the threading dislocation density. However, we speculate that surface-to-surface conduction could also be prevented if the misfit interface was removed, as shown in figure 1(b). To our knowledge, limited research has been performed into suspended Ge structures fabricated from blanket epitaxially grown layers [31–33], and dislocation action has not been investigated in those works.

In this paper we show that if a Ge layer, chemically resistive to most alkaline anisotropic etches, is geometrically patterned completely away from the surface \langle 110 \rangle directions then the underetching mechanism can be used to intentionally create various suspended structures. These suspended structures could allow the Ge/Si interface to be removed, and with it the majority of the misfit dislocation network, thereby limiting the electrical leakage. Therefore, if Ge layers could be micromachined quickly and with ease, Ge could be the material of choice for a new generation of platform that enables complete integration of optoelectronic/spintronic/CMOS devices with the benefits of suspended MEMS technology. In particular, we suggest that if suspended Ge nanowire devices [34–36] could be fabricated and then coated with dielectric on all sides, for example by using gas deposition sources, a truly homogeneous all-round gate control of conduction through nanowires could be achieved.

2. Fabrication of suspended structures

We used low-resistivity (10–25Ω cm), 525μm thick 4" Si(001) wafers polished on one side. A germanium layer was epitaxially grown on the polished side of the wafer by reduced-pressure chemical vapour deposition (RP-CVD) in an ASM Epsilon 2000E system, using germane as a precursor. The details of growth are identical to those reported previously [19], using a 100-nm-thick low-temperature deposition ‘seed’ layer and a subsequent 900-nm-thick layer deposited at a high temperature, the complete structure being named a two-temperature Ge layer of overall thickness 1000 nm. The overall layer has sub-nm rms roughness and is slightly tensile-strained to remain flat [37]. Another two-temperature Ge bilayer was grown to demonstrate how the overall epitaxial heterostructure determines and limits the dimensions of the suspended structures. This bilayer consisted of a 100-nm-thick seed layer and a 100-nm-thick...
The process flow for the fabrication of the underetched structures: (a) the layer prior to any patterning, (b) the structure after lithography and dry etching with the critical orientations, and (c) the suspended structure after anisotropic underetching.

The process flow for the underetched structures is shown in figure 2. First, standard optical lithography was performed using a single layer of 1.3 µm S1813 photoresist and an MJB3 optical mask aligner. Then Ge mesa definition was performed by a Corial 200 IL reactive ion etching (RIE) system using a mix of O₂ and SF₆ plasma, 100 W RF power, total gas pressure of 20 mTorr and a total gas flow of 30 cm³ min⁻¹ at an etch rate of approximately 150 nm s⁻¹, with selectivity over the photoresist. This photoresist was then removed through an acetone wash which left a Ge mesa as depicted in figure 2(b). Finally, the sample was etched in a 25 wt% TMAH bath at 85 °C to suspend the structure, as shown in figure 2(c). Note that in the simple flow diagram surface-orientated ⟨100⟩ features are completely underetched and surface-orientated ⟨110⟩ features leave various etch resistive planes. It was found that the underetching rate along the surface ⟨100⟩ directions is approximately 0.6 µm min⁻¹.

We first demonstrate a spiderweb platform, utilizing the 1 µm Ge layer, of overall dimensions 800 µm × 800 µm with 5-µm-wide legs. Figure 3 shows a scanning electron microscopy (SEM) image of the Ge spiderweb mesa attached to the bulk substrate, and figure 4 shows a tilted SEM image of this Ge spiderweb partially suspended after TMAH etching. The SEM observations were performed with an accelerating voltage of 5 kV and a Zeiss Supra InLens backscattered electron detector. Partial suspension of the structure can be confirmed from the electron shadow of the beams as outlined in figure 4, observable due to the large tilt of the sample. Note also that the longest legs of the design are still anchored to the substrate. This is because these legs are patterned on the surface ⟨110⟩ directions, which reveal the {111} etch planes and resist the underetching process, whereas all other legs for the structure are patterned away from the surface ⟨110⟩ directions.

Next, we redesigned the spiderweb so that all features are rotated and patterned off the surface ⟨110⟩ directions and the frame is anchored to the substrate by patterning on the surface ⟨110⟩ axes. In addition, the dimensions of the spiderweb are reduced to demonstrate that the epitaxial design is the limiting thickness factor of these nano/microstructures. The suspended spiderweb structure, shown in figure 5, spans over an area of 200 µm × 200 µm and has 3-µm-wide legs and a Ge thickness of 200 nm. This structure was misaligned to the substrate surface ⟨110⟩ directions, allowing some underetching of the frame, which also reveals the contrast between the underetched Ge and bulk layers near the frame. SEM imaging was performed at the higher energy of 20 kV, instead of 5 kV which, in combination with reduction of the Ge thickness, allows electron transparency in the suspended sections. This enables us to determine suspension in a new
Figure 4. Tilted plan-view SEM image at 5 kV of the partially suspended spiderweb over an area of 800 µm with a leg width of 5 µm and a thickness of 1 µm. Green shows the Ge arms, both suspended and not, whilst purple shows the Si [111] planes which have resisted the etch. The outlined area shows a Ge beam and its electron shadow, one method of determining the suspension of the structure.

Figure 5. A tilted plan-view SEM image at 20 kV of a fully suspended Ge spiderweb of lateral dimensions over 200 µm × 200 µm, leg width 3 µm and thickness 200 nm. Green shows the Ge. The outlined area shows the advantage of using higher SEM accelerating voltages, where the electron transparency is obvious.

way by noting the reduced intensity of backscattered electrons from the suspended portion.

We finally tested the repeatability of the underetching process with a multiple Ge microwire design. The overall design is shown in figure 6(a) where the edges of the contact/anchor pads are patterned on the surface ⟨110⟩ directions, to avoid release, and the wires are patterned on the surface ⟨100⟩ direction to allow for underetching. One important observation for these structures is that the anchor size is limited due to the ⟨112⟩ equivalent planes revealed on the corners that allow for some local underetching. This can be seen to affect the last few wires at either end of the structure in figure 6(a) where wires are unsupported over this local underetching and flex towards the Si surface. However, where the anchor holds, the smallest lateral dimensions achieved (limited by the optical mask aligner used) are 2-µm-wide wires with a Ge thickness of 200 nm, over a length of 285 µm, shown in figure 6(b). These wires are extremely uniform and are clearly suspended without any signs of bowing or buckling, which is another advantage of the Ge layer being under slight tension. This tension arises during the epitaxial growth of Ge on Si, because although the Ge is fully relaxed at the growth temperatures, it acquires tension on cooling to room temperature due to the difference in thermal expansion coefficients of Si and Ge. The tension is retained after etching as, although the Ge is no longer held by the immediately underlying Si substrate, its dimensions are still constrained by the surrounding Si frame to which it is firmly bound by the continuous Ge layer. With higher resolution lithography, and retaining a similar aspect ratio, we believe that much finer wires could also be formed by this technique.

3. Hall measurements of suspended structures

The second part of this investigation demonstrates the intrinsic electrical properties of the bulk Ge and suspended Ge. Previously, it has been difficult to measure the properties of thin epitaxial layers because of the shunting effect of the attached substrate, but here we present a way to remove that. A pair of van der Pauw cross structures were fabricated using the same fabrication process flow, but where one sample was not underetched to act as a control and the other received the full processing, so that the cross is suspended and the bulk pads are anchored to the substrate, see figure 7(a). Contacts were made to the pads by indenting them with a diamond scribe, so that the Si substrate was also contacted and an InGa eutectic was applied with Cu needles. Note that the RP-CVD-grown Ge layer is nominally undoped, which in practice for this high-purity growth process means an impurity concentration of below 10¹⁷ cm⁻³. This was confirmed by SIMS analysis revealing no common impurities above this detection limit.
Resistivity measurements were performed from room temperature down to 10 K using currents in the order of 0.1–20 µA on a sample with 20-µm-wide Ge arms and a layer thickness of 1 µm, so that the threading dislocation density was as low as possible [19]. The active thickness of the intrinsic sample is assumed to be the entire thickness of 1 µm, and all the following results are calculated with this value shown in figures 7(b) and (c). From 300 K down to 150 K the conductivity of the Si(001) substrate dominates in both samples, meaning that the absolute values are incorrect, but allows a conduction calibration of both samples to confirm that our experimental analysis is valid. From 150 K to about 90 K the free carriers in the Si substrate can be seen to freeze out [38] and the resistivity increases. In the region from 90 K to 30 K the effect of suspension is observed as a resistivity shift of the two curves. We interpret this as conduction occurring within the Ge layer for both samples, but the additional conduction in the dislocation network due to carrier hopping between dislocation-localized states [28, 29] further reduces the resistance of the unsuspended sample. In the suspended sample the dislocation network has been partially etched away and no longer provides this conduction path. This observation is supported by the data from below 30 K, where carrier freeze out is expected to occur in the Ge [27, 39]. Only a minimal resistivity shift is observed in the bulk Ge on Si sample, since conduction is dominated by transport through the misfit dislocation network, whereas the suspended sample shows a 100-fold increase in resistivity as its major conduction path is closed. Within this low-temperature regime, below 20 K, the resistivity of the suspended Ge plateaus is increased from 2.5 Ω cm on the bulk sample by over two orders of magnitude to a maximum of 280 Ω cm in the suspended structure. Compared to a similar study in bulk Ge with induced dislocations by Hung and Gliessman and by Kozhukh [40, 41], these values suggest that our Ge layer is exhibiting the typical conduction and general trends with temperature observed when transport is dominated by impurities at a level of about $10^{16}$ cm$^{-3}$.

These observations are supported by Hall measurements in a field of 600 mT, which produce the results shown in figure 7(c). From 300 to 150 K the silicon mobility dominates, and then the Ge mobility dominates from below 90 K down to 30 K as free carriers freeze out in the Si. In both these regimes
the mobility in the suspended and bulk samples are roughly equal and within experimental uncertainty, demonstrating that the transport mechanism is the same and most likely determined by the bulk material. Compared to the work by Bebye and Conwell [42] it demonstrates that the mobility of $1 \times 10^4 \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ in Ge at 20 K arises from an intrinsic carrier concentration of approximately $10^{16} \text{cm}^{-3}$, confirming the doping level suggested by the resistivity measurements. Below 20 K we observe a dramatic difference between the two samples, which we believe indicates that at low temperature the main transport mechanism is conduction through the dislocation network. This drop of mobility, from $\sim 650 \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ in the bulk to only $\sim 10 \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ in the suspended structure, shows that the intrinsic carriers in the Ge have frozen out in both cases to leave very low mobility in the suspended structure, even lower than that of a very highly doped Ge layer [43]. In the bulk sample there is a significantly greater conductivity where the dislocation network remains and assists in transporting carriers thus increasing mobility.

We have performed similar measurements using a wafer with a degenerately doped top layer of Ge. This simplifies the interpretation of the results by removing the temperature dependence that arises from freeze out of intrinsic carriers and also eliminates any uncertainty arising from a depletion region influenced by charges trapped on the top surface. The overall thickness of the Ge on Si layer was kept as 1 $\mu$m, to retain the same dislocation density, but the topmost 350 nm was doped with phosphine (PH$_3$), see figure 8(a). The dopant concentration was measured by SIMS to be $3.3 \times 10^{19} \text{cm}^{-3}$ with a thickness of 350 nm, and the carrier concentration was confirmed by Hall measurements to be $3.0 \times 10^{19} \text{cm}^{-3}$ in both the suspended and bulk structures. This means the doped layer is degenerately doped and will be one of the main sources of conduction at higher temperatures. At low temperatures it will not freeze out, and so remain alongside the dislocation conduction. The results of resistivity and Hall measurements are shown in figures 8(b) and (c). Above 100 K the Si substrate still contributes to the mobility and resistivity. Below 100 K there is little temperature variation for either sample, as expected, but a difference in resistivity between the suspended and bulk samples is close to two orders of magnitude, which is similar to that seen in figure 7 at low temperatures where intrinsic conduction is frozen out. We identify the two main paths of conduction: the doped region and the dislocations at this point where suspending the sample removes most, if not all, of the dislocation conduction. The effect of removing most of the misfit dislocation network can thus be observed within the suspended sample by the increased resistivity as well as lowered carrier mobility, which we speculate to be low due to scattering from ionized impurities and dislocations. This shows that leakage paths through the dislocations have been isolated and the bulk material did not dominate the measurements.

4. Summary

We have fabricated Ge suspended structures and studied the role of dislocations within them. A range of fully suspended crystalline Ge structures, which are purity-compatible with the manufacture of integrated circuits (IC clean), have been demonstrated, including spiderwebs, microwires and crosses. The microwires were 200 nm thick, 2 $\mu$m wide and 285 $\mu$m long, and these dimensions could be reduced to feasibly fabricate suspended Ge nanowire devices [34–36]. The intrinsic electric resistivity of the suspended layer was studied by fabricating a suspended van der Pauw cross and measuring the resistivity as a function of temperature. Removal of the misfit dislocation network was shown to enhance the intrinsic electrical isolation by over two orders of magnitude at low temperature to a maximum resistivity of 280 $\Omega$ cm. With this knowledge, we suggest that Ge nanowire devices could be fabricated utilizing this suspension method.
with an all-round gate for ultimate transistor control by
gas source deposition, and that leakage of devices could be
eliminated as a major issue. Additionally, these suspended
wires could be processed similar to the work by Nam et al
[33] and Lauhon et al [34]. Those authors took advantage
of the free-standing nature of a Ge membrane by applying
a bilayer stressor method to achieve tensile strain, which
demonstrates efficient electroluminescence for Ge lasing
applications. Similar structures could be used to measure
other properties of the suspended layer, such as thermal
conductivity, or to create devices that are much more sensitive
to changes in their environment than their bulk counterparts.

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