A generic and efficient convolutional neural network accelerator using HLS for a system on chip design

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Abstract

This paper presents a generic convolutional neural network accelerator (CNNA) for a system on chip design (SoC). The goal was to accelerate inference of different deep learning networks on an embedded SoC platform. The presented CNNA has a scalable architecture which uses high level synthesis (HLS) and SystemC for the hardware accelerator. It is able to accelerate any CNN exported from Python and supports a combination of convolutional, max-pooling, and fully connected layers. A training method using fixed-point quantized weights is proposed and presented in the paper. The CNNA is template-based, enabling it to scale for different targets of the Xilinx ZYNQ platform. This approach enables design space exploration, which makes it possible to explore several configurations of the CNNA during C- and RTL-simulation, fitting it to the desired platform and model. The convolutional neural network VGG16 was used to test the solution on a Xilinx Ultra96 board. The result gave a high accuracy in training with an auto-scaled fixed-point Q2.14 format compared to a similar floating-point model. It was able to perform inference in 2.00 seconds, while having an average power consumption of 2.63 W, which corresponds to a power efficiency of 6.0 GOPS/W for the CNN accelerator.

Keywords: System On Chip, FPGA, High Level Synthesis, Convolutional Neural Network, PYNQ

1. Introduction

In recent years, deep learning with convolutional neural networks (CNN) has been applied in many different fields such as image classification [1],[2], object detection [3],[4] and recognition [5]. In most cases, state-of-the-art CNN models run on a server in the cloud. However, with the increase of Internet of Things (IoT), there is a demand for embedding the deep neural networks into mobile edge computing. This is especially true for computer vision systems, where the amount of collected data is high and analyses of images must be carried out in real-time.

As CNNs continue to be applied to increasingly complex problems, low throughput, latency and energy efficiency present challenges on embedded devices with central processing units (CPUs) or graphical processing units (GPUs). Due to several attractive features, field programming gate arrays (FPGA) present promising platforms for hardware (HW) acceleration of CNNs as reported in [6],[7],[8],[9]. CNNs optimized for fixed-point or using binary neural networks achieve even better performance [10],[11],[12],[13]. In general, FPGAs provide higher performance than CPUs and have a better energy efficiency than both CPUs and GPUs.

Historically, the long design time and need for HW experts have limited the use of FPGA. Here, the high level synthesis (HLS) tools have enabled automatic compilation from imperative high-level programs to low-level specifications in a hardware definition language (HDL) [14]. It is, however, still a challenge to accelerate large-scale CNNs [15] on a FPGA, since model parameters typically require far more memory than the on-chip capacity of the FPGAs. Another challenge is to find an optimal configuration for a given HW accelerator design due to the long design time.

The scope of our work is to develop a generic and flexible architecture, which can accelerate the inference of CNN networks on a multi-processor system.

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on chip design (MPSoC). It presents the design of the HW/SW architecture, i.e. the programmable logic that will reside in the FPGA fabric and the design of the software. The architecture is generic so that it can accept major CNNs such as AlexNet [16] and VGG16 [2], which can be exported from a deep learning framework such as Keras [17]. It is developed in the PYNQ [18] framework using Python and SystemC [19] in order to create a generic template based HW accelerator. To find the optimal design, a SystemC based simulation is used to explore the design space of the optimal configuration parameters of the CNN accelerator. The design model is translated to a HDL specification using HLS. Our paper discusses the precision, speed and power consumption of the accelerator as well as the fixed-point retraining of the CNN.

1.1. Related work

In this section, the current state-of-the-art hardware based CNN accelerators that inspired the architecture presented in this paper will be discussed.

The Microsoft model [20] is an architecture developed by Microsoft for accelerating CNN for a cloud server solution with several FPGA-cards. The architecture uses a top-level controller to control the data-flow with a PCI memory interface. It has multiple input buffers, one kernel weight buffer, a large array of processing element arrays (PEA) and lastly, a data redistribution block. It uses a direct memory access (DMA) channel to load data in from PC memory to the buffers. On the FPGA it uses PEA blocks to perform dot product calculations of the values in the input buffer and the weight buffer. The result of the dot product is saved into the next input buffer.

ZynqNet [21] is based on the architecture of the Microsoft model. However, it focuses on making it work for both training and inference. It is built for a SoC design instead of a server solution. The proposed solution seems promising, although it appears to have a few bottlenecks due to a purely C-based HLS implementation of the solution. It uses a circular line buffer (CLB) for input data handling and uses a memory-mapped master interface to get data from the main memory, e.g. weights and input data are transferred using the memory-mapped interface.

YodaNN: An Ultra-Low Power Convolutional Neural Network Accelerator Based On Binary Weights [22] is an accelerator designed for an ASCI instead of an FPGA. It is stated that FPGA is two orders of magnitude less energy efficient than ASCI. The architecture of the accelerator is built for accelerating an input of 32 channels with 32 kernels, which results in a 32 channel output. The accelerator only focuses on the convolution part of CNN and is locked to a specific type of CNN architecture.

FINN-R [11] is an end-to-end deep-learning framework for fast exploration of quantized neural networks (QNN). It is a framework built upon the FINN accelerator [23] which is a QNN built for FPGA. The FINN-R consists of a cascade of multiple layer accelerators that are optimized for a pipelined architecture. This design reduces the transferring of data between the main memory and the accelerators. The difficult part is to balance the layered accelerators in order to prevent bottlenecks or resource waste. However the framework, does not solve the problem of different throughput for each layer. FINN-R optimizes the generated HW using HLS, allowing fast exploration of QNN to create the perfect accelerator for a specific FPGA target.

NeuFlow [24] uses a so-called Runtime Reconfigurable Dataflow Architecture. It consists of processing tiles (PT), a DMA, and both global and local data lines, where each PT has a local data line with its four neighbours. It consists of a controller and bus, which allows configuration and grid wiring of all the PTs during runtime. In this way, the grid can be set up to run different types of operations, although the PTs are only fine-tuned for accelerating artificial neural networks (ANN).

Most of the different architecture build their architectures are built around a PEA with a buffer for handling input data, which could be a CLB or a row buffer. The output handling varies. Some designs, such as FINN-R, use the output to feed the next accelerator. Others have a large memory to cache layered outputs directly to the next input buffer so that data are ready for the next CNN layer. However, due to limited internal memory, this approach is not feasible for all FPGAs. Therefore, there is a need for reloading the input data from the main memory. An example of this is the Microsoft model. Other architectures use the main memory to cache the data between layers. FINN-R, for example, does this for each block of layers.

The CNN developed in this work has some elements in common with the papers presented above. It uses the main memory to store data between layers. In addition, the architecture is built around a PEA with two buffering systems: one for the
weights and one for input image data, the latter of which uses a CLB. The above architectures are very similar, but the major difference lies in the details of the CLB, which enables efficient pipelining and data alignment.

The CNN architecture in our work supports any input size and layer depth, stride, zero padding and windows size. It also supports so-called stitching, which allows the splitting of CNN layers into multiple iterations. This is explained in detail in section 3.2. It makes the accelerator more flexible and enables it to run nearly any CNN model that uses convolution, pooling and fully connected layers. Unlike FINN, which uses small building blocks, the accelerator developed in this work accelerates all parts inside a single IP core. This approach allows the hardware to reuse the efficient but expensive CLB in both convolution layers and pooling layers. It can be used with most CNN models during runtime without the need for re-compiling that is required for the Microsoft model. The accelerator is developed to work with PYNNQ [25],[18] and uses an application programming interface (API) similar to Keras [17]. The CNN model may need to be retrained if too much quantization is desired, i.e. a very small fixed-point format.

2. Design methods

In this section, we will briefly describe the design methods and concepts used as a basis in designing and implementing the architecture for the convolutional neural network accelerator (CNNA).

When working with FPGAs, there are different methods for developing an Intellectual Property Core (IP). A wide-used method is writing code at the behavioural level or RTL in HDL language such as Verilog or VHDL. These languages are normally time-consuming and require skilled HDL engineering.

Another possibility is to use HLS [26],[27] to develop the IP. HLS is a way of writing behavioural models of the hardware in a higher abstraction language, typically C or C++. This behavioural model can be mapped and scheduled to an RTL model using a synthesis tool such as Xilinx Vivado HLS [28],[29]. Developing IP using HLS can be very time efficient due to the higher abstraction level as well as the inherent design flow.

In our work, SystemC is used with the design flow described in [28, ch. 1],[30]. It is an efficient way in which an IP can be written and verified using HLS. SystemC is able to model the hardware structure and concurrency in a more optimal manner than pure C and C++. It is an IEEE standard (IEEEStd 1666-2011) [19], based on a C++ template library made for HW/SW co-design.

Productivity for ZYNQ (PYNNQ) [31] is an open-source framework for creating applications on a ZYNQ MPSoC. The system design in this work is based on PYNNQ for controlling the IP directly from Python. This framework is divided into three layers: application, software, and hardware.

The application layer, which hosts the user-code, is described in [31, ch. 22]. This is usually Python code in the form of a Jupyter notebook that runs on the ARM CPU inside the ZYNQ MPSoC. The authors of the present paper argue that the choice of Python increases productivity, since Python is a high-level interpreted language, which can be developed quickly and run piecewise, thus allowing for quick debugging.

The middle layer in the PYNNQ framework is the software layer. This layer contains the Python libraries and the interaction with the IP inside the FPGA through the OS drivers. Several drivers are provided through the PYNNQ libraries for interacting with the IP. The interface is called an overlay and is used to program the FPGA and manage the IP.

The last hardware layer in the PYNNQ framework is the bit-file programmed into the FPGA. The interaction between the software layer and the hardware layer is done using direct memory access (DMA) or memory-mapped interfaces.

3. System architecture

The SoC design consists of three main elements: the FPGA (i.e. the programming logic (PL)) the dual core CPU and memory (i.e. random access memory (RAM)). The goal is to run a CNN consisting of convolutional, max-pooling and fully connected layers computed in the same IP Core inside the FPGA logic. The responsibility of the CPU is to let the user control the hardware acceleration so that the IP Core is processing CNN layers in correct sequential order. Figure 1 shows that the system uses direct memory access (DMA) to transfer data and weights between the CPU and IP Core accelerator. The CPU controls the DMA data block transfer and converts the memory interface to the streaming interface of the IP Core.
The system interacts in different manners depending on which scenario it needs to execute. There are three main scenarios: preprocessing, initialization and inference.

Preprocessing. The first scenario preprocessing converts the weights to fixed-point and realigns and scales the weights so that they are ready for the system to use. Preprocessing also calculates parameters such as layer output size and layers to be split which can be done offline on any computer. The weights are transformed from floating-point to fixed-point representation in the chosen format, and aligned and rounded off correctly, as described later. Finally, the weights are saved in an h5-file, which is the standard format for storing weights in Keras [17], and can be transferred to the hardware target.

Initialization. The hardware target needs to be configured and initialized for a particular fixed-point resolution by using the synthesized bit-file of the optimized CNNA. The bit-file contains the CNNA IP Core and interconnection setup to the CPU for the specified hardware target. This is done using a specification of the model in the form of a JSON-file and an h5-file containing the weights, which are already realigned and quantized in the preprocessing. It starts by calculating the buffer size and getting the properties of the loaded CNNA. When this is done, the SW allocates the needed resources and readies the SW for inference by allocating the buffers for each layer in the CNN.

Inference. When using the system, predicting an image will be the most commonly used task. This task is shown in the sequence diagram in figure 2. Here, the user calls the method predict, which returns the predicted class of the image when the inference is done. The image, which is the parameter to the method predict, is stored internally in a contiguous array, i.e. an array which can be used by the PYNQ DMA library. Depending on the CNN, several layers are executed in the correct order, i.e. convolution, pooling or fully connected layer. All parameters controlling the CNN execution are sent at the start of the predict method.

The CPU initiates the convolution by starting several tasks, which happens in parallel. These tasks prepare the data transfers for the input control buffer CTRL, the input data buffer X, the output data buffer Y, the weight buffer W, and the stitching buffer Xbuf. The data transfers are handled by the DMA, which streams the data from RAM to the CNNA. If Xbuf is in use, it means that the convolutional layer has been split into several operations, because the buffer for the weights in the FPGA is too small. This is called stitching and essentially interleaves an old result with new results.

Figure 1: Block diagram of the system architecture covering CPU (ZYNQ Ultrascale+ MPSoC), memory (DDR RAM), hardware IP Core accelerator (CNNA), five DMAs for inputs (X), outputs (Y), weights (W), control (CTRL) and splits (XBUF).

Figure 2: Sequence diagram of the system of interaction between software control (PYNQ) and hardware accelerator (FPGA) during inference.
All configuration for the IP core is sent through the CTRL DMA so that it calculates the convolution correctly.

The convolution is done by the CPU initiating four different tasks in parallel. It sets up the data transfer for the input control data CTRL, the input data X, the output Y and Xbuf. Each of these data transfers are handled by the DMA, which streams the content of the buffer from RAM to the CNNA.

The input control data CTRL is for sending the configuration for the CNNA to do the computation correctly. The last supported layer is the fully connected layer. The fully connected layer is executed similarly to both pooling and convolution. It starts four different DMAs, one for each of the input data X, the weights W and the output Y and the configuration though the CTRL.

3.1. Interfaces

Two interfaces are used. The streaming interface used for the DMA is implemented with a functional deterministic guaranty so that no race condition can happen, which makes the whole IP very stable. The other AXI-lite [32] interface, which is a memory-map, interface is only used for reading status registers.

**Streaming interface.** The streaming interface, i.e. the AXI streaming interface, is used for transmitting the data between the CPU and IP. This interface can, in theory, be connected to any module supporting the interface. In this work, however, it is connected to a DMA interface. The main reason for choosing the streaming interface is that it enables transmission of data to the IP using the high performance (HP) buses which can accomplish speeds up to $128$ bit $/\text{clock}$ using standard DMA modules. The streaming interface also provides back-pressure which allows throughput balancing of the streaming ports.

**Status interface.** The status register is used for checking the properties for the current CNNA so the software knows how the data should be aligned, or for reading status registers and debugging. The interface is implemented as an AXI4-lite [33] memory-mapped interface and is used to interact with the IP as part of the CPU memory address space. This can remove some of the overhead that comes with using DMA and is only faster when transferring few data values.

3.2. Software control and stitching

Some convolutional layers are too large to be processed as a single CNNA iteration. This means that they are split up into several sub convolutions. However, the result is returned from the IP Core with the depth first and thus needs to be stitched together with the later result. This is done using the IP Core which has a DMA-channel (XBUF) for this purpose, as shown in figure 1. An example of stitching can be seen in figure 3. The shown example illustrates the output of two pixels, a and b, from a convolution that has a depth that needs to be split.

The stitching is done using two equally sized buffers, which both have a size equal to the expected output size. The size in this example is six. The first convolution only uses the first buffer as the output, where pixels a and b are both updated by the DMA. However, only the first third of the depth is calculated in the first convolution. The second convolution calculates the next third of the output. However, these outputs need to be stitched in between the previous outputs. This is done using the output of the first convolution as a stitch buffer. The IP Core is informed to use the first part of each pixel and appends the result to each pixel depth-wise. The result of this stitching is sent to the output buffer[1]. The third convolution takes two thirds from the stitch buffer and the last third from the output for each pixel. The output of the stitched convolution is in the buffer, which is the one used as output in the last stitching.

However, most fully connected layers are also too large to be processed at once, however, in which case the splits are handled differently. A fully con-
The connected layer generates a single value per output. The buffer will be filled with values from the first split when it runs the first time. The second time it runs it will get the next outputs, which need to be put after the first split in the buffer. This is solved by adding the number of bytes, which is produced by the first split, to the physical address, i.e. the pointer to the address in RAM.

All the splits need to have an adjusted number of bytes to receive so such that it only receives the right amount of data. When all the splits have been processed the result is in the same buffer, which is then ready for the next layer. This means that the fully connected layer only needs a single buffer, contrary to the convolution layers, which needs two.

### 3.3. CNN hardware accelerator

Figure 4 shows the architecture overview of the main elements of the CNNA. The CNNA works as an accelerator for a single layer at a time. This means that the accelerator needs to be reconfigured for each layer, which is done using the streaming interface CTRL.

Furthermore, the accelerator has four other streaming interfaces, which each of which has a specific use. The streaming interface $W$ is used to load the weights, which can consist of multiple kernels, and cache these in the weight buffer. This means they can be used multiple times. The streaming interface $X$ is used to stream in the input data, which can either be an image or the output from the previous layer. $X$ buf is an interface that is used when a convolutional layer is split into several splits, which need to be stitched together correctly. The last streaming interface is $Y$, which streams out the output values of the operation.

The accelerator is built for three different operations: convolution, pooling and fully connected layers. During convolution acceleration, it uses the weight buffer, the data buffer and the PEA. The pooling operation is done using only the data buffer and the pooling block. When executing the fully connected layers, the weight buffer and data buffer are simply set to forward the data directly to the PEA, thus generating a dot product of the two.

The CNNA is designed using the five blocks briefly described in the following sections.

**Weight buffer.** The weight buffer is used to cache the weights inside the FPGA. This cached data is transmitted to the PEA where the convolution is calculated.

**Data buffer.** The data buffer is used to handle the input data stream and create the windows on which the convolution or pooling is carried on. These windows are used for further calculations, which will be described later in this section.

**Processing elements array (PEA).** The PEA is used for handling the math acceleration in the CNNA, i.e. it is an array of dot product accelerators. Each of these PEAs are given a matching pair of input data and weights from the data buffer and the weight buffer, respectively. They then calculate the output. The PEAs also handles the activation function, which can be either linear or ReLU [34]. The output of these is passed on to the output handling element.

**Pooling.** The polling element is used to accelerate the pooling operation. It gets its input from the data buffer and sends the output to the output handling part, thus bypassing the PEA, which is not used in pooling.

**Output handler.** The output handling element plays a major role in getting the output of the CNNA into the right shape and alignment before streaming it out through interface $Y$. It merges the results from the PEA when it is used, and if the data needs to be stitched with $X$ buf, i.e. if a convolution operation has been split into more than one convolution and needs to have the old output
Figure 5: Weight buffer with alignment illustrates how kernel weight data are aligned so that a specific kernel gets in the right spot. The illustration shows how the weight data of kernel 0 are sent to stream buffer 1. The iteration interval (II) and bandwidth (BW) of the weight input package are changed by a factor of resize factor. The yellow part of the image cube shows which part of the kernel is sent.

interleaved into the new output. Splitting the convolution happens when too many kernels need to be stored in the weight buffer.

It also handles the output of a pooling operation, which simply means forwarding the output of the pooling element.

3.3.1. Weight buffer

The weight buffer is used for caching the weight kernels. This caching is necessary, because the convolution requires the kernels to be used once for each output pixel. For instance, if the first convolutional layer of VGG16 has an output of 224 × 224 = 50,176, i.e. the kernel is used 50176 times, it makes it worthwhile to store and not resend every kernel for each pixel.

An illustration of the weight buffer module can be seen in figure 5, which shows the modules inside of it. The iteration interval (II) and bandwidth (BW) of the weight input package are changed during resizing as illustrated in the figure. It shows how the resize module changes the BW from input BW, BW^{(in)} by a factor of resize factor. It also splits the raw package into smaller packages. The realign module splits the raw package into smaller packages. The splitter separates the data stream into \( N \) different stream buffers, each of which has the same BW as the resized BW, BW^{(resize)}. Each stream buffer sends the kernel to a PE \( X \) times.

The realignment in the weight buffer is complicated. This is firstly due to the bias value, which uses a complete package. Secondly, it is complicated because the kernels need to match the order in which the three-dimensional window comes from the data buffer, i.e. have the same positions and depths as the data buffer. In figure 5, the first package contains the bias values transferred to the weight buffer. It shows that this single value only uses a complete resized package. This is followed by \( N \) other bias packages. After all bias packages are sent the weight packages are sent. In this example, the weight packages contain a 3 × 3 × 4 window. The stream buffers contain a 3 × 3 × 4 window.

3.3.2. Data buffer

An image typically consists of three channels, RGB, which can be visualized as a three-dimensional cube. A three-dimensional image is illustrated in figure 6. The image is stored in raster order, i.e. firstly, pixel (0,0) channel 0, then channel 1 of the same pixel followed by the last channel. This is followed by the same three channels for the pixel one row down, which means that the Z-axis is processed first, then the Y-axis second and the X-axis last. Raster order is the order in which the image data is streamed to the CNNA.

The Circular Line Buffer (CLB) can be considered the brain of the CNNA, because it allows it to increase the BW and removes the need to realign the input data for each layer. However, before explaining the different parts of the CLB, we must explain the parameters that the actor can set through the control interface, must be explained. These parameters are:

- **Row size** The row size of the input image, i.e. the Y-axis length. It is assumed that the image is quadratic.
- **Depth** The depth is N-channels of the input image, i.e. the Z-axis of the image. This should be dividable by the bandwidth.
- **Stride** Stride is a convolution parameter.
- **Window size** The size of the window. If the window size is 3, the real window size would be 3 × 3 × depth. This is also a convolution parameter.
- **Zero pad** A convolution parameter setting the size of the zero padding around the image.
Figure 6: An illustration of the flow of data through the CLB. It consists of two parts: a line buffer for storing $N_{lines}$ previous lines and a shift buffer for storing $N_{pixels}$ previous pixel for each line. The leftmost image cube illustrates a single pixel 202, which is written for the line buffer. The middle cube illustrates which data is saved in which line buffer and how the new line replaces the first line. The rightmost cube illustrates what data is in the shift buffers. The missing part illustrates how much more data is needed from the line buffers before it has a complete window in the shift buffer. The read pointer on the shift buffers is used for getting the $N$ previous samples and is used for generating the output from the shift buffers.

- **Replay** How many times the CLB should resend a single window.

After setting up the CLB with the parameters through the control interface, the image data can flow into the CLB. The CLB consists of two parts: a line buffer for storing $N_{lines}$ previous lines and a shift buffer for storing $N_{pixels}$ previous pixel for each line. These parts are explained in detail below:

**Line buffers.** The first module in the CLB, where the image data is ordered and stored is the line buffer. This module streams one row of the image with all channels at the same time. The number of line buffers is equal to the maximum window size minus one, $N_{line\ buffer} = window_{size} - 1$. This is because only the $N$ previous lines are needed to construct a window. The illustration of the data flow of the line buffer in figure 6 shows that the $N - 1$ previous lines are stored inside the line buffer and sent out individually. This means that the bandwidth increases with a factor of $window_{size}$. It is also indicated that the buffer is stored circularly, i.e. the oldest value is overwritten by the newest when new data arrive. This is handled by the pointer, which can be seen in figure 6. This pointer will increase each time a new input is received, and after receiving a whole line, the line buffers will rotate, i.e. the first line will be moved to the back the second line will be pushed forward and the pointer will be reset. This is done by multiplexing logic in the implemented design.

**Shift buffers.** After the line buffers, the data reaches the shift buffers. These buffers are used for getting the $N$ previous pixels from each line, i.e. having all the pixels needed for a convolution window, as shown in figure 6. The shift buffers have another important function too. They replay the window for the convolution if there are not enough PEs to run all the dot products in the convolution operation at once. The shift buffers are RAM-based shift buffers and consist of two pointers. The write pointer is essentially controlled by counting up whenever data is written and moving it back to start of the shift buffer when the end has been reached. The read pointer, however, is controlled by logic, which tells the shift buffer that it needs the $N$ previous samples. This will be handled by the shift buffer, which also calculates its new posi-
3.3.3. Processing element array

The heart of the CNNA is the PEA. Each processing element (PE) performs hardware acceleration of a dot product with a small range of activation functions, i.e. linear or ReLU. The PE operation can be written as shown in equation 1, which is a dot product of the two equal length vectors $\vec{x}$ and $\vec{w}$.

$$PE(\vec{x}, \vec{w}) = f\left(\sum_{i=0}^{N-1} (x_i \cdot w_i)\right)$$

Each PE receives data frames in pairs from the weight buffer and the data buffer, i.e. one from each. The acceleration of the PE is done by running the multiplications in parallel and totaling the results afterward, as illustrated in figure 7. This data is dotted together and followed by the activation function.

The figure 7 shows how the PE has two inputs: $W$, the weight input, and $X$, the data input. When the PE has received a frame on both $W$ and $X$, the data frames are dotted together and the bias is added to the result. The result is forwarded to the next part, which is the PE summer. This part accumulates the result, which it has received from the PE dot product. It will keep on accumulating until it receives the last flag. When this happens, it will multiply the accumulated value by a factor set by the actor, i.e. the control interface, and apply the activation, which is also set by the actor through the control interface. Lastly, it is streamed out through the port $Y$, and the accumulated result is reset.

3.3.4. Pooling

Pooling is used in CNN to downsample an image. The reason for placing the pooling operator inside the CNNA is reuse of the CLB hardware. The pooling accelerator receives its input directly from the CLB, and the output from the pooling goes directly to the output.

When looking at figure 8, it can be seen that the pooling block consists of logic for handling the pooling operation, e.g. max-pooling, and RAM for buffering a single pixel. The pooling logic is controlled by the actor and is used for setting the depth of the current image and the size of the window, e.g. $2 \times 2 \times$ depth or $3 \times 3 \times$ depth. The last parameter controls what type of pooling operator should be run, i.e. max-, min- or average-pooling.

4. Training for fixed-point

To overcome the challenge of the CNNA using fixed-point values, an emulation of fixed-point needs to be made for the CNN to be trained and calculated correctly. This is mostly due to the large dynamic range of the weights.

This emulation is shown in equation 2, where $Q_{[I,F]}(x)$ is the fixed-point representation of $x$ in
the fixed-point format $Q[I,F]$ [35]. Here, $I$ is the number of integer bits and $F$ is the number of fractional bits. First, the number $x$ is scaled up by $2^F$ and then rounded off to resolve the limited resolution of fixed-point numbers. This is followed by what is essentially a saturation of the number to the range of the fixed-point number, i.e. between $-2^{l+F-1}$ and $2^{l+F-1} - 1$. Lastly, the number is scaled down by the same factor it was scaled up by. This results in a value that can be interpreted correctly by the CNNA.

$$Q[l,F](x) = \max\left(-2^{l+F-1}, \min(2^{l+F-1} - 1, \text{round}(x \cdot 2^F))\right) \cdot 2^{-F}$$

(2)

4.1. Quantized weights

The weights are quantized as a constraint to the optimizer, which executes the backpropagation [36]. This constraint is set to quantize all weights after each update using equation 2. This results in the stochastic gradient decent (SGD) update formula shown in equation 3, where $Q[l,F](x)$ is the quantization function shown in equation 2, $W^{(l,t-1)}$ is the previous weight, $W^{(l,t)}$ is the new weight, and $\alpha$ is the learning rate.

$$W^{(l,t)} = Q[l,F](W^{(l,t-1)} - \alpha \nabla W^{(l,t-1)})$$

(3)

However, this introduces a problem, that makes the training freeze. The cause of the problem is that the size of the update to the weights is too small to move from one quantized value to another. The effect of a too-small update change can be seen in the following example shown in equation 4. Its not possible to update a single weight in Q2.6 with a value smaller than the smallest quantized value, in this case $2^{-6} = 0.015625$. The example shows a weight with value 1.671875 being updated by a too-small value: 0.0015624. Updating the quantized weight value does not result in a change, which causes the training to freeze.

$$W^{(l)} = Q[2.6](1.671875 - 0.0015624) = 1.671875$$

(4)

To solve this issue, an extra copy of the weights $W$ is saved so that the forward pass, i.e. inference, is calculated using the quantized weights, and the SGD is calculated using unquantized weights. This means that the weights do not get stuck between quantization steps. This is also known as Lazy update SGD [37]. In this way, the weights $W$ are saved and the quantized weights $WQ$ are used for the forward pass, which can be seen in equations 5 and 6.

$$W^{(l),t=\tau} = (W^{(l),t=\tau-1} - \alpha \nabla W^{(l),t=\tau-1})$$

(5)

$$WQ^{(l),t=\tau} = Q[l,F](W^{(l),t=\tau})$$

(6)

By using these equations, the optimizer can train the CNN even though the changes are too small to be significant when quantized.

4.2. Dynamic range scaling

It has been found that the small kernels in the first convolutional layers of the CNN VGG16 have large weights, i.e. close to 1 or −1, but the fully connected layers have very small weights that only use the lowest bits, even in Q2.14. This means that the CNN needs more fractional bits. However, this is possible to solve by dynamically scaling the weights and the output. This is carried out with integers in [38]. The following will show how this can be carried out on fixed-point values as well. It has been found that the dynamic range of each kernel is almost the same for each layer. This knowledge can be used to add scaling to each layer in order to change the dynamic range of the weights. For example, based on the given weights

$$W = \begin{bmatrix}
0.11 & 0.024 & -0.30 \\
-0.05 & 0.002 & 0.1
\end{bmatrix}$$

and a fixed-point format $Q[l,F]$, which, for simplicity, is able to store a maximum value of 1, denoted $Q[l,F]^{MAX}$, a scaling can be found. To find the scaling needed for a better dynamic range, equation 7 can be used. This equation takes the absolute maximum absolute value of the weights and divides it by the maximum value of the fixed-point format.

$$\text{scale}^{(l)} = \frac{\max(|W^{(l)}|)}{Q[l,F]^{MAX}} = \frac{|-0.30|}{0.30} = 0.30$$

(7)

The scaled value of the weights can now be calculated as shown in equation 8, which divides the
weights by \( scale^{(l)} \). This shows that the maximal absolute value is now \(-1\).

\[
W_{\text{scale}}^{(l)} = \frac{W^{(l)}}{scale^{(l)}} = \begin{bmatrix} 0.367 & 0.08 & -1 \\ -0.167 & 0.00667 & 0.333 \end{bmatrix} \tag{8}
\]

Using this scale factor, the output of a layer is calculated as shown in equation 9, which has an added multiplication of the quantized value of the scale factor, where \( z_{\text{scale}}^{(l)} \) is the scaled output of layer \( l \), \( W_{\text{scale}}^{(l)} \) are the scaled weights, \( a^{(l-1)} \) is the output from the previous layer and \( scale^{(l)} \) is the scale factor of the layer \( l \).

\[
z_{\text{scale}}^{(l)} = Q[l,F](W_{\text{scale}}^{(l)}a^{(l-1)}) \cdot Q[l,\text{ceil}](scale^{(l)}) \tag{9}
\]

Because of the quantization, it cannot be guaranteed that the outputs are the same, but they should be very similar, i.e. \( z^{(l)} \approx z_{\text{scale}}^{(l)} \). The main difference between the scaled and unscaled version is that \( z_{\text{scale}}^{(l)} \) is better suited for the bit range of the fixed-point format than \( z^{(l)} \). More bits result in a better SNR, as shown in equation 10. This means that, for example shown earlier, the bits used have increased by \( \text{ceil}(\log_2((scale^{(l)})^{-1})) = 2 \), which corresponds to an increase in SNR of 12.04dB.

\[
\Delta SNR_{\text{DB}}(N_{\text{bits}}) = 20 \log_{10}(2^{N_{\text{bits}}}) \approx 6.02 \cdot N_{\text{bits}} \tag{10}
\]

5. Design space exploration

The template-based IP Core written in SystemC has a number of parameters that must be selected to achieve an optimal solution. When optimizing the IP Core for a FPGA, it can be an enormous task to generate a design and find the optimal design parameters. It takes approximately one hour to synthesize the HLS code to RTL code. If this was to be done for all possible combinations of parameters, it would take weeks, months or even years, since the developed architecture has such a large number of parameters, e.g. bandwidth (BW) between modules, FIFO-depth, the number of PEs, etc.

The design parameters are used for tuning the CNNA design in order to find a tradeoff between precision, speed and resources. The CNNA tuning parameters used are as follows:

- \( data_{\text{size}}^{(W)} \): The word-length of the fixed-point data format in bits, i.e. 1+F. Has an impact on precision.
- \( PE_{BW(x)} \): The internal BW with an element size of data_{\text{size}}^{(W)} used by the CNNA.
- \( PE_N \): The number of PEs and the PEA are limited by the size of FPGA fabrics.
- \( DB_{BW(x)}^{(output)} \): The output BW multiplier after the CLB. Normally this will be set at an equal value to \( CLB_{N}^{(rows)} \) but can be set to a lower number in order to allow the PE to run with lower BW and potentially have a bigger PEA. The internal BW in the PE will be \( DB_{BW(x)}^{(output)} \cdot PE_{BW(x)} \), with an element size of data_{\text{size}}^{(W)}. The BW used inside the weight buffer is also equal to \( DB_{BW(x)}^{(output)} \cdot PE_{BW(x)} \).
- \( kernels_{N}^{(2 \times 3 \times 512+1)} \). Used to calculate

\[
WB_{\text{size}}^{(buffer)} = \left( \frac{(3 \times 3 \times 512)}{DB_{BW(x)}^{(output)} \cdot PE_{BW(x)}} + \text{bias}_{\text{size}} \right) - \text{kerne}\]

\[
\text{To measure the performance of the different CNNA configurations, a simulation was made. It consisted of five different elements, two pooling operations, two convolution operations and a single fully connected operation, which was executed individually but evaluated together.}

When looking at the latency for the combined simulation test, i.e. the five simulations carried out consecutively after each other, the dominant candidates all have DB_{BW(x)}^{(output)} = 1 regardless of word length (see figure 9). The figure shows that the faster the accelerator is the higher the number of PEs.

Two models were created of each configuration, one of which was done using C-simulation, i.e. simulation using the SystemC HLS code directly. The
Figure 9: Results of the C-simulation of the combined test of all fixed-point candidates, showing the average resource usage of BRAM and DSP vs latency. The $PE_{BW}$ is set to 128 for all solutions. The plotted text for a candidate is in the format $PE_N, DB_{\text{output}}$ kernels$_N^{(3 \times 3 \times 512 + 1)}$. The candidates are split up in three groups of the word lengths (data size) 8 bit, 16 bit and 32 bit versions.

Other was a RTL-simulation, which used the RTL-code generated from the SystemC model. The latter was clock cycle accurate and the execution time was precise.

Several candidates were identified and shown in greater detail in table 1. The table shows the number of DSP and BRAM used, as well as the total latency for C- and RTL-simulation. Some candidates marked with a "-" uses more resources than is available on the tested target platform. Other candidates were synthesized and tested using RTL-simulation, which simulates the real HDL-code generated. This also gives a more precise resource usage, which is typically slightly lower than the one estimated using C-simulation. The execution time is also shown and is slightly higher than the estimated value.

Finding the optimal parameters was done using two different fixed-point formats (data size): Q2.14 and Q2.6, i.e. a word length of 16 bits and 8 bits, respectively. These were chosen because of area constraints of the FPGA on the Xilinx Ultra96 board [39]. However 32-bits would have been possible with a larger FPGA.

Finally, three different configurations of the CNNA were chosen for the final test of the system, one of which used 16-bit fixed-point format Q2.14 while two used 8 bit fixed-point format Q2.6.

6. Results and discussion

The dataset DETECT [40] was used to verify the system. This dataset consisted of 29 classes of micro-invertebrates suspended in alcohol. Only the first five classes were used in the first test, while the second test used all 29 classes. The training was carried out over the span of 100 epochs, which means that the complete dataset was repeated 100 times for training.

The CNN used was VGG16 [2]. Here the dense layers following all the CNN blocks is two fully connected layers with either 4096 or 1024 neurons. The last fully connected layer has either five or 29 neurons, depending on the number of classes. The training was performed on two fixed-point formats: Q2.14 and Q2.6, and tested on three configurations, which will be denoted CNNA$_{16}$, CNNA$_{18}$ and CNNA$_{28}$. CNNA$_{16}$ uses the tuning parameters $\vec{\beta} = [16, 128, 8, 3, 32]$, CNNA$_{18}$ uses $\vec{\beta} = [8, 128, 16, 1, 42]$ and CNNA$_{28}$ uses $\vec{\beta} = [8, 128, 8, 3, 42]$.

The accuracy and performance of the proposed system will be presented and discussed in this section. The inference time of an image will be evaluated, using the VGG16 trained in section 4. Execution time for each layer will be presented in order to give an indication of which layers take the longest time.

6.1. Accuracy

The CNN was trained using the small dataset in order to find suitable candidates faster, since it is easier to train for five classes than for 29 classes. If the accuracy of a fixed-point format is poor on five classes, it will likely be as poor, or worse, when training on 29 classes. In addition, training on five classes takes approximately two and a half hours on VGG16 with 4096 neurons in the fully connected layers, whereas it takes almost eight hours to train the network when using all 29 classes. Therefore, the first training is done on the small dataset.

Figure 10 shows that most of the trained models face some issues and obtain low accuracy when using fixed-point format. The only quantized version that obtains a high accuracy is the one using fixed-point format Q2.14. It is unknown why the training that uses fixed-point format Q2.14 and no auto-scaling makes a sudden dive after 10 epoch. However, it could be caused by the learning-rate being too high or too low, or too few neurons in the fully connected layers. It seems that the best results

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Table 1: Design space exploration of resource usage and latency of possible CNNA candidates using C- and RTL-simulation. A "÷" means RTL-simulation performed, but insufficient space on target platform (Ultra96). A "-" means RTL-simulation not performed.

| Parameters | resource average % | DSPs (RTL) | BRAMs (RTL) | latency [ms] (RTL) |
|------------|--------------------|------------|-------------|-------------------|
|            | 70                 | 384        | 359         | 144               | 249               | 4.60 | 6.66 |
| [8, 128, 8, 3, 42] | 34                 | 128        | 125         | 137               | 185               | 4.95 | 7.28 |
| [8, 128, 16, 3, 42] | 124                | 768        | -           | 152               | -                 | 4.26 | -    |
| [8, 128, 16, 1, 42] | 52                 | 256        | 245         | 139               | 193               | 4.03 | 6.66 |
| [16, 128, 8, 3, 32] | 54                 | 192        | 360         | 233               | 377               | 7.47 | 8.40 |
| [16, 128, 8, 1, 32] | 35                 | 64         | -           | 227               | -                 | 7.61 | -    |
| [16, 128, 16, 3, 32] | 81                 | 384        | -           | 239               | -                 | 6.98 | -    |
| [16, 128, 16, 1, 32] | 44                 | 128        | 293         | 229               | 349               | 6.27 | 8.52 |
| [32, 128, 8, 3, 20] | 94                 | 384        | -           | 355               | -                 | 13.19 | -    |
| [32, 128, 8, 1, 20] | 58                 | 128        | 165         | 351               | 336               | 12.92 | 14.53 |
| [32, 128, 16, 3, 20] | 148                | 768        | -           | 359               | -                 | 12.42 | -    |
| [32, 128, 16, 1, 20] | 76                 | 256        | 325         | 353               | 408               | 10.73 | 12.81 |

Figure 10: Fully connected layers have 1024 neurons. Gray: floating-point, orange: fixed-point Q2.14 with auto-scaling, blue: fixed-point Q2.14 without auto-scaling, red at the bottom: fixed-point Q2.6 with and without auto-scale. Figure 11: Fully connected layers have 4096 neurons. Orange: fixed-point Q2.14 with auto-scaling, blue: fixed-point Q2.14 without auto-scaling, red at the bottom: fixed-point Q2.6 with and without auto-scale.

are achieved using fixed-point format Q2.14 and auto-scaling, which converges towards an accuracy of almost 100%. Figure 11 shows that the fixed-point format Q2.14 with auto-scaling performs well on the CNN with 4096 neurons in the fully connected layers. The training that uses Q2.14 with no auto-scaling performs well and reaches approximately 84%. All fixed-point Q2.6 versions did not manage to be trained or achieve any useful results.

Table 2 shows the results of the training. It shows the type of fixed-point training, omitting the ones that did not achieve any useful results. The table shows the number of neurons in the fully connected layers, N_{neurons}, as well as the validation accuracy, where validation is performed on a dataset not used for training. Finally, it shows the accuracy on the training dataset.

The final test was performed on all 29 classes of DETECT, using the candidates that performed well in the previous test. The best candidates were the floating-point version for reference and the versions using fixed-point format Q2.14, both with and without auto-scaling. As is evident from figure figure 12, only the training using fixed-point format Q2.14 and auto-scaling achieved any promising results. It shows that it is much harder to train the CNNA when using quantization, because details are lost due to the limited range of the fixed point num-
Table 2: Training results for the training of VGG16 on 5 classes.

| Type    | auto-scale | N_{neurons} | validate | train  |
|---------|-----------|-------------|----------|--------|
| float   | n/a       | 1024        | 97.5     | 100.0  |
| Q2.14   | no        | 1024        | 24.3     | 23.6   |
| Q2.14   | yes       | 1024        | 94.2     | 98.8   |
| float   | n/a       | 4096        | 97.9     | 99.5   |
| Q2.14   | no        | 4096        | 83.2     | 83.6   |
| Q2.14   | yes       | 4096        | 91.7     | 97.6   |

Figure 12: Fully connected layers has 4096 neurons. Blue: floating-point, red: fixed-point Q2.14 with auto-scale, light blue: fixed-point Q2.14 without auto-scaling.

6.2. Performance

The Xilinx Ultra96 board [39] was used to evaluate the performance of the system using a hardware clock of 100 MHz and 172.22 MHz for the CNNA IP Core. The inference time was measured for the different configurations of the CNNA_{16}, CNNA_{1}^{16} and CNNA_{2}^{16} and the inference times are shown in table 4. The timing performance is measured on the Ultra96 board during inference of the quantized and trained VGG16 model with five classes. The mean time and variance is measured as an average over 30 measurements. The fastest model CNNA_{1}^{16} takes 1.22 sec per image, while the slowest, CNNA_{16} at 100 MHz, takes 2.20 sec per image.

Table 4: Average inference time and variance using VGG16 for five classes using four different IP Cores.

|                  | CNNA_{16} 100MHz | CNNA_{16} 173MHz | CNNA_{1}^{16} 173MHz | CNNA_{2}^{16} 173MHz |
|------------------|------------------|------------------|----------------------|----------------------|
| avg [sec]        | 2.20             | 1.96             | 1.22                 | 1.49                 |
| var [10^{-3}]    | 0.25             | 0.30             | 0.20                 | 0.11                 |

The different layers have different execution times, as shown in table 5. As expected, the execution time in convolutional layers depends on the number of bits in the fixed-point format. However, pooling takes approximately the same time for all tested IP, since pooling is independent of the fixed-point format. The table shows that the IP CNNA_{1}^{16} obtains the best performance due to the larger number of PEs (16). Note that CNNA_{2}^{16} is slightly faster than CNNA_{1}^{16} in the convolutional layers, even with fewer PEs, due to the higher bandwidth of the output multiplier. There is a large number of splits (512) in the dense_1 and dense_2 layers, and they consume more than half of the total execution time for all three CNNA configurations. A larger FPGA enabling more PEs and buffers could be a solution to lower the number of splits and optimize the system further.

6.3. Power consumption

The power consumption of the design with CNNA_{16}, CNNA_{1}^{16} and CNNA_{2}^{16} was measured on the Ultra96 board during inference of the trained VGG16 model with five classes. The measured voltage of the power supply to the board was multiplied with the measured current to compute the power consumption. The mean and maximum power during inference is calculated as a mean over 10 inferences. The power consumption of the IP Core is defined as the difference of the Ultra96 board idling and power during inference. The idle power consumption was measured over a five-minute period to be $P_{idle} = 3.055$ Watt:

$$P_{idle} = 3.055 \text{ Watt}$$
Table 5: Time of execution of each VGG16 layer in [ms] using four different IP Cores.

| layer | CNNA\textsubscript{16} 100MHz | CNNA\textsubscript{16} 172MHz | CNNA\textsubscript{1} 172MHz | CNNA\textsubscript{1} 172MHz |
|-------|-----------------|-----------------|-----------------|-----------------|
| l1\_conv1 | 19.3            | 17.0            | 19.9            | 21.4            |
| l1\_conv2 | 111             | 84.1            | 61.3            | 60.1            |
| l1\_pool | 18.1            | 13.7            | 12.9            | 17.1            |
| l2\_conv1 | 55.4            | 42.9            | 31.3            | 30.5            |
| l2\_conv2 | 108             | 81.3            | 60.2            | 56.3            |
| l2\_pool | 8.98            | 6.87            | 6.36            | 8.40            |
| l3\_conv1 | 56.0            | 4.35            | 33.1            | 29.9            |
| l3\_conv2 | 112             | 84.2            | 64.2            | 59.1            |
| l3\_conv3 | 110             | 85.5            | 63.0            | 57.8            |
| l3\_pool | 4.51            | 3.48            | 3.25            | 4.23            |
| l4\_conv1 | 64.6            | 51.5            | 37.9            | 35.3            |
| l4\_conv2 | 126             | 97.9            | 76.0            | 70.5            |
| l4\_conv3 | 123             | 102.0           | 73.5            | 67.8            |
| l4\_pool | 2.32            | 1.83            | 1.71            | 2.19            |
| l5\_conv1 | 46.6            | 41.0            | 30.7            | 29.3            |
| l5\_conv2 | 49.1            | 39.7            | 29.7            | 28.1            |
| l5\_conv3 | 45.8            | 39.5            | 29.6            | 27.8            |
| l5\_pool | 0.74            | 0.62            | 0.59            | 0.69            |
| dense\_1 | 767             | 737             | 364             | 509             |
| dense\_2 | 393             | 397             | 197             | 362             |
| dense\_3 | 1.55            | 1.62            | 1.18            | 1.50            |

Table 6: Average and peak power consumption of the Ultra96 board and the system and IP Core during inference.

|              | CNNA\textsubscript{16} 100MHz | CNNA\textsubscript{16} 172MHz | CNNA\textsubscript{1} 172MHz | CNNA\textsubscript{1} 172MHz |
|--------------|-----------------|-----------------|-----------------|-----------------|
| $P_{\text{avg}}$ [W] | 5.28            | 5.68            | 4.71            | 4.80            |
| $P_{\text{peak}}$ [W] | 6.60            | 7.14            | 5.76            | 6.35            |
| $P_{IP\_\text{avg}}$ [W] | 2.23            | 2.63            | 1.66            | 1.74            |
| $P_{IP\_\text{peak}}$ [W] | 3.55            | 4.09            | 2.71            | 3.30            |

Table 6 shows that the mean power consumption of the Ultra96 board is between 4.7 – 5.7 W for all tests from where the IP Core only consumes approximately 2 W. This means that running the IP does not affect the average power consumption. However, the fixed-point IPs with a low amount of bits use less energy per inference because they run for a shorter amount of time. The CNNA\textsubscript{16} using a 100 MHz clock is 0.24 sec slower but consumes less power than the version using a 172 MHz clock.

Table 6 shows that the peak power consumption is almost the same for all tested IPs in the range from 2.7 W to 4.1 W.

Figures 13, 14 and 15 show that the power consumption is largest in the beginning of the inference, i.e. in the convolution blocks of the CNN. The power consumption drops during execution of the fully connected layers. This indicates that most of the FPGA logic is in action during convolution, while less is used when computing the fully connected layers and pooling. Pooling activity corresponds to the big dips in power consumption in the first half of the inference.

7. Comparing to state-of-art CNNs

To compare the results of this work with current state-of-the-art CNNs, the same units of measurement are needed. Because of this, the throughput needs to be expressed in giga operations per second.
(GOPS) and the power efficiency in GOPS/W. This section will evaluate the CNNA in the present paper with the same units of measurements as in [41], and discuss whether the results are satisfactory.

**Throughput.** The throughput in GOPS is calculated as shown in equation 11, where $N_{\text{operations}}$ is the number of operations in the tested CNN. In the case of VGG16, this number is 30.76 GOP. $t_{\text{run}}$ is the time of inference using the CNN in seconds and $N_{\text{OPS}}$ is the number of operations per second in GOPS.

$$N_{\text{OPS}} = \frac{N_{\text{operations}}}{t_{\text{run}}} \quad (11)$$

The results are shown in table 7, which indicates that the GOPS are lower than the compared architectures. This can be due to different measurement methods, i.e. if only tested on convolutional layers, the number of GOPS is very large. However, if fully connected layers are taken into consideration, it will drop dramatically, which is the case for the tests carried out in this work. Furthermore, the Ultra96 target used in our evaluation is very small and low-cost compared to the ones used in the state-of-the-art examples. If a larger and more expensive target such as the Xilinx ZCU104 evaluation kit [42] was used, it would be possible to increase the number of PEs, thereby achieving a higher throughput and performance.

**Power efficiency.** The power efficiency is expressed as GOPS/W. It can be calculated as shown in equation 12, where $N_{\text{OPS}}$ is the number of operations per second, which we calculated earlier. $P_{\text{IP mean}}$ is the mean power consumption of the CNNA, which we measured earlier. $\frac{\text{GOPS}}{W}$ is the power efficiency.

$$\frac{\text{GOPS}}{W} = \frac{N_{\text{OPS}}}{P_{\text{IP mean}}} \quad (12)$$

Compared to many of the current state-of-the-art accelerators, the CNN accelerator in this work performs well in terms of power efficiency. When using 16-bit fixed-point weights, it is comparable to both NeuFlow and Microsoft. However, the results are very dependent on the method of measurement, as described above. It is not the most power-efficient solution, but, unlike FINN, it does not need recompiling, and unlike YodaNN it is reconfigurable. In terms of power efficiency, it is comparable to Microsoft, although Microsoft uses a much larger and more expensive FPGA, and thus achieves a considerably higher throughput.

8. Conclusion

In this paper, an architecture for a system on chip design was presented. This presented architecture implements the different operations necessary for a deep neural network to perform close to real-time inference. The architecture was implemented using Python and HLS for the IP Core and was able to run on the Ultra96 board using PYNQ. The interface for the system is similar to Keras and should be familiar to most engineers working in the field of machine learning.

The CNN is able to accelerate deep learning algorithms that uses uses any sequence of convolutional, max-pooling and fully connected layers. The layer operations can support many different parameters and will be able to perform inferences using most modern CNNs. The network weights can use any 8-, 16- or 32-bit fixed-point format when exported from Keras and the weights must be autoscaled correctly. A training method was proposed which achieved inference accuracies that were almost as high when using fixed-point weights as floating-point weights.

The system is able to accelerate the CNN operations in HW. However, it is not able to run in real-time for a computer vision system that demands a throughput of several frames per second. The VGG16 architecture chosen for testing in this paper was able to perform inference in 2.0 sec per image when using the fixed-point format Q2.14 and 1.2 sec when using fixed-point format Q2.6. The power
Table 7: A table with state-of-the-art CNN accelerators. ÷ = unsupported and ∼ = needs re-compiling.

| Technique       | Power Efficiency [GOPS/W] | GOPS  | DSP | BRAM | LUT | Format [bit] | Scalable input, conv pool, fc | SoC   |
|-----------------|---------------------------|-------|-----|------|-----|--------------|--------------------------------|-------|
| FINN [23]       | 210.7                     | 2465.5| N/A | 186  | 46253| 1-2          | ∼                              | ✓     |
| NeuFlow [24]    | 14.7                      | 147   | N/A | N/A  | 16  | ✓            | ✓                              | ✓     |
| YodaNN [22]     | 2756                      | 1510  | N/A | N/A  | 1   | ∼            | ∼                              | ∼     |
| Microsoft [20]  | 7.15                      | 1178  | N/A | N/A  | N/A | float        | ✓                              | ✓     |
| CNN1 [16-100MHz]| 6.278                     | 13.99 | 339 | 277  | 42490| 16           | ✓                              | ✓     |
| CNN1 [16-172MHz]| 5.989                     | 15.73 | 360 | 174  | 55626| 16           | ✓                              | ✓     |
| CNN2 [172MHz]   | 15.22                     | 25.23 | 245 | 132  | 57232| 8            | ✓                              | ✓     |
| CNN2 [172MHz]   | 11.83                     | 20.71 | 359 | 160  | 64998| 8            | ✓                              | ✓     |

consumption of the developed CNN (Q2.14) is less than 7.2 W peak power including the other components of the system and has an average power consumption below 5.7 W. The IP Core alone consumes a peak power of 4.1 W with a mean power between 1.5 – 2.7 W and has a power efficiency between 6.0 – 15.2 GOPS/W depending of the fixed-point format. The accuracy of the VGG16 network was acceptable when using fixed-point format Q2.14 with weights retrained for the specific format.

Acknowledgments

We would like to thank Freia Martensen for language and proof reading the article.

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