Remarkably High-Performance Nanosheet GeSn Thin-Film Transistor

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Abstract: High-performance p-type thin-film transistors (pTFTs) are crucial for realizing low-power display-on-panel and monolithic three-dimensional integrated circuits. Unfortunately, it is difficult to achieve a high hole mobility of greater than 10 cm²/V·s, even for SnO TFTs with a unique single-hole band and a small hole effective mass. In this paper, we demonstrate a high-performance GeSn pTFT with a high field-effect hole mobility (μFE), of 41.8 cm²/V·s; a sharp turn-on subthreshold slope (SS), of 311 mV/dec, for low-voltage operation; and a large on-current/off-current (I_On/I_Off) value, of 8.9 × 10⁶. This remarkably high I_On/I_Off is achieved using an ultra-thin nanosheet GeSn, with a thickness of only 7 nm. Although an even higher hole mobility (103.8 cm²/V·s) was obtained with a thicker GeSn channel, the I_Off increased rapidly and the poor I_On/I_Off (75) was unsuitable for transistor applications. The high mobility is due to the small hole effective mass of GeSn, which is supported by first-principles electronic structure calculations.

Keywords: GeSn; nanosheet TFT; monolithic 3D IC; 3D brain-mimicking ICs

1. Introduction

Thin-film transistors (TFTs) [1–29] have been investigated intensively in the past few decades [1–3] because of their ultra-low-energy-using process, usage of a small amount of material, and light transparency [4–7]. To realize system-on-panel (SoP) and monolithic three-dimensional (3D) integrated circuits (ICs) [8–11], high-performance n-type and p-type TFT devices (nTFT and pTFT, respectively) are required to form low-DC-power complementary TFTs (CTFTs) [12–15]. For oxide nTFTs, excellent device performance with a high field-effect mobility (μFE), of ~100 cm²/V·s; a sharp turn-on subthreshold swing (SS), of ~100 mV/dec; and a large on-current/off-current (I_On/I_Off) ratio, of >10⁶, has been achieved using a SnO₂ channel material [16–20]. However, because of the fundamental physical restrictions [30,31], the mobility of oxide pTFTs is generally less than 10 cm²/V·s [22–25], which remains a basic challenge for CTFTs. Although single-hole energy bands and small hole effective masses have been reported in metal-oxide SnO materials, the hole mobility of pTFTs is restrained by the requisite low-temperature process [22]. Alternatively, GeSn material also has a small hole effective mass and a direct energy bandgap [32–34]. In this paper, we report poly-GeSn pTFT with a high μFE (41.8 cm²/V·s), a sharp SS (311 mV/dec), and a large I_On/I_Off value (8.9 × 10⁶). Although an even larger hole mobility, of 103.8 cm²/V·s, is obtained in a thicker GeSn channel, there is a tradeoff with a poor I_Off, with an I_On/I_Off of only 75. The crucially large I_On/I_Off was achieved using an ultra-thin (7 nm) nanosheet GeSn. The I_Off leakage is the crucial issue for highly
scaled 3 and 2 nm node silicon (Si) transistors. To decrease the $I_{\text{OFF}}$, an ultra-thin (7 nm) channel layer is used for Si nanosheet FETs on 12-inch wafers. It is important to note that although many papers have reported the device performance using the monolayer two-dimensional (2D) materials, there is no manufacture solution for a 12-inch Si wafer till date. X-ray photoelectron spectroscopy (XPS) analysis revealed that the Ge/Sn ratio in the GeSn film was 7. First-principles electronic structure calculations show that the high mobility is due to the smaller hole effective mass of $\text{Ge}_{0.875}\text{Sn}_{0.125}$, which is lower than that of Ge. The low fabrication temperature (350 °C) and a high-performance nanosheet GeSn TFT are an enabling technology for SoP, monolithic 3D ICs, and 3D brain-mimicking ICs.

2. Materials and Methods

A 500 nm thick SiO$_2$ layer was formed on a p-type Si wafer to mimic a glass substrate. Subsequently, 50 nm of TaN was deposited by a reactive sputtering system and served as the gate electrode. Then, the gate insulator was deposited with a 40 nm thick high-dielectric constant (high-$\kappa$) HfO$_2$ layer and a 2 nm SiO$_2$ interfacial layer. The gate insulator was subjected to 350 °C post-deposition annealing in ambient O$_2$ for 30 min. Thereafter, GeSn layers with a thickness of 5, 7, or 9 nm were deposited by sputtering Ge and Sn targets at 80 and 10 W, respectively, under an Ar gas flow of 24 sccm. Next, the GeSn layer was annealed at 350 °C for 30 s by rapid thermal annealing in N$_2$ ambient. Finally, 30 nm of Ni was deposited and patterned as the source and drain electrodes to form the TFTs. The length and width of the bottom-gate GeSn pTFTs were 50 and 500 µm, respectively. The electrical characteristics were measured using an HP 4155B parameter analyzer and a probe station. All the devices were measured at 25 °C, the room temperature in a lab environment. The GeSn channel layer was analyzed by X-ray photoelectron spectroscopy (XPS, Thermo Nexsa, MA, USA). The device structure was examined using high-resolution transmission electron microscopy (TEM, FEI Talos F200X, OR, USA). The crystallinity of the GeSn layer was measured by X-ray diffraction (XRD) using a Bede D1 high-resolution XRD analyzer (Durham, England). First-principles electronic structure calculations were carried out using the Vienna ab initio simulation package (VASP) [35] and aimed to disclose the electronic structure of $\text{Ge}_{0.875}\text{Sn}_{0.125}$. The projector augmented wave (PAW) approach was applied to describe the interactions between the core electrons and nuclei [36,37]. The valence electrons explicitly treated were (4s$^2$, 4p$^2$) and (5s$^2$, 5p$^2$) for Ge and Sn, respectively. The exchange correlation of electrons was described using Heyd–Scuseria –Ernzerhof (HSE) hybrid functionals [38]. The self-consistent calculation converged at $10^{-6}$ eV. The structures were optimized using a conjugated-gradient algorithm until the ionic forces were smaller than 0.0001 eV/Å with a plane wave cutoff of 400 eV, and the corresponding k-point mesh of $5 \times 5 \times 5$ was applied to the optimized structure of the diamond cubic $\text{Ge}_{0.875}\text{Sn}_{0.125}$ model with a lattice constant of 5.763 Å, containing eight atoms (Figure S1). Density of state (DOS) calculations were performed using a denser k-point mesh, of $6 \times 6 \times 6$. The SUMO Python Package [39,40] and Vaspkit code [41] were employed to generate symmetry K-Path for the band structure calculation and for post processing of the effective mass extraction from the band.

3. Results

Figure 1a shows the drain-source current versus the gate-source voltage ($I_{\text{DS}}$–$V_{\text{GS}}$) characteristics of GeSn/SiO$_2$/HfO$_2$ pTFTs with GeSn thicknesses of 5, 7, or 9 nm. The device with a channel thickness of 7 nm exhibited the best performance, with an $I_{\text{ON}}$/$I_{\text{OFF}}$ value of $8.9 \times 10^6$. The gate-source current versus the gate-source voltage ($I_{\text{GS}}$–$V_{\text{GS}}$) of the TFT devices with different GeSn film thicknesses is displayed in Figure S2. Figure 1b displays the field-effect mobility versus the gate-source voltage ($\mu_{\text{FE}}$–$V_{\text{GS}}$) characteristics of the GeSn pTFTs, which were measured under a small $V_{\text{DS}}$ (−0.1 V). Here, the hole mobility values increase with the GeSn layer thickness, which is consistent with the increasing trend of $I_{\text{ON}}$. This is due to the decreased depletion width of GeSn by the gate and surface potential, which provides more carriers to transport from the source to the drain. The peak
mobilities of the GeSn TFTs with GeSn thicknesses of 5, 7, and 9 nm were 3.9, 41.8, and 103.8 cm²/V·s, respectively. Although the device with a GeSn thickness of 9 nm showed the highest mobility, the poor SS (1560 mV/dec) and an \( I_{\text{ON}}/I_{\text{OFF}} \) of only 75 make it unsuitable for device applications. The thin (5 nm) channel thickness exhibited 10 times lower mobility than the 7 nm GeSn device, which is attributed to the lack of carriers and strong interfacial scattering \([26,27]\). The 7 nm GeSn TFT device showed a large \( I_{\text{ON}}/I_{\text{OFF}} \), of \( 8.9 \times 10^6 \); a good SS value, of 311 mV/dec; and a high \( \mu_{\text{FE}} \), of 41.8 cm²/V·s, which is much better than those of traditional oxide pTFTs and shows the high potential for future SoP and monolithic brain-mimicking IC applications. In addition, such a high hole mobility is similar to that of the single-crystal Si used for standard ICs \([42]\). It is important to note that the nanosheet GeSn thickness of 7 nm is exactly the same as that of the single-crystal Si nanosheet FET used for 2 nm node technology manufacture.

![Figure 1](image-url)

**Figure 1.** The (a) \( I_{\text{DS}} \)-\( V_{\text{GS}} \) and (b) \( \mu_{\text{FE}} \)-\( V_{\text{GS}} \) characteristics of the GeSn/SiO₂/HfO₂ pTFTs with different channel thicknesses.

The drain-source current versus the drain-source voltage \( (I_{\text{DS}}-V_{\text{DS}}) \) characteristics of GeSn pTFT devices with GeSn thicknesses of 5, 7, or 9 nm are shown in Figure 2a–c, respectively. The saturation \( I_{\text{DS}} \) increases with increasing GeSn channel thickness, and a higher \( I_{\text{DS}} \) leads to a higher \( \mu_{\text{FE}} \), as shown in Figure 1b. The \( I_{\text{DS}}-V_{\text{DS}} \) curves for 5 and 7 nm thicknesses of GeSn display good \( I_{\text{DS}} \) saturation characteristics. In contrast, the 9 nm thick GeSn device shows poor saturation characteristics, which is due to excessive carrier conduction and poor channel pinch-off. In addition, the non-negligible \( I_{\text{DS}} \) at \( V_{\text{GS}} = 0 \) V will lead to high standby power.

![Figure 2](image-url)

**Figure 2.** The \( I_{\text{DS}} \)-\( V_{\text{DS}} \) characteristics of the GeSn/SiO₂/HfO₂ pTFTs with (a) 5 nm, (b) 7 nm, and (c) 9 nm channel thicknesses.
Figure 3a illustrates the schematic device structure diagram of the bottom-gate GeSn pTFT. High-work-function Ni was formed on GeSn and used as the drain and source electrodes. The HfO$_2$ and thin SiO$_2$ stack served as the gate dielectric, in which SiO$_2$ was used to minimize the remote phonon scattering effects from high-$\kappa$ HfO$_2$ [17,20,43–45]. In this study, a high-$\kappa$ gate dielectric was used to increase the gate capacitance and $I_{ON}$, which is widely used for Si metal-oxide-semiconductor (MOS) FET and TFT devices. The device structure was further verified using cross-sectional TEM. As depicted in Figure 3b, the thicknesses of the GeSn channel layer and the SiO$_2$ interfacial layer on high-$\kappa$ HfO$_2$ are 7 and 2 nm, respectively. Here, the crystal grains in the TEM image are marked with a yellow dashed line. Figure S3a and Figure S3b show the TEM images of the device with GeSn layers annealed at 300 and 350 °C, respectively. A 2 nm SiO$_2$ layer is added between HfO$_2$ and GeSn. Via an atomic force microscope (AFM), Figure S4 exhibits the surface roughness of the GeSn layer annealed at different temperatures. The surface roughness of the GeSn layer degrades with increasing annealing temperature. The device annealed at 300 °C displays the best surface smoothness and uniformity (Figure S4a); however, the hole $\mu_{FE}$ is only 3.71 cm$^2$/V·s, as depicted in Figure S5. The crystalline size depends on the GeSn thickness and annealing temperature. However, the increasing GeSn thickness increases the device $I_{OFF}$ leakage. The increasing annealing temperature degrades mobility by increasing surface roughness (Figure S4c). Therefore, there is a tradeoff between the channel layer surface roughness, uniformity, and carrier mobility. The 350 °C annealing is the best condition to increase $\mu_{FE}$ of the nanosheet FET. Further hole $\mu_{FE}$ and $I_{OFF}$ tradeoff may be possible by using a 6 nm GeSn layer.

![Figure 3](image-url)

**Figure 3.** (a) The schematic device diagram and (b) the cross-sectional TEM image of a bottom-gate GeSn pTFT.

XPS analysis was conducted to examine the composition of the GeSn layer. Through XPS measurements, as depicted in Figure S6, the ratio of Ge/Sn was determined to be 7. Figure 4a shows the Ge 3d and Sn 3d$_{5/2}$ core spectra. There is no oxide compound signal of GeO$_x$ or SnO$_x$ in the Ge 3d and Sn3d$_{5/2}$ spectra [46], which is one of the reasons for the high mobility. As depicted in Figure 4b, the XRD analysis reveals that the GeSn layer is polycrystalline after annealing at 350 °C. The diffraction peaks related to GeSn are crystal orientations GeSn (111), GeSn (220), and GeSn (311), corresponding to 2θ values of 27.0°, 45.0°, and 52.7°, respectively, which are similar to previously published data [29,47–49]. Additionally, at 2θ = 30.79° and 55.03°, diffraction peaks of $\beta$-Sn (200) and $\beta$-Sn (301) were observed [22,49,50], which could be the Sn precipitated during the rapid thermal annealing at 350 °C.
To thoroughly comprehend the fundamental physical properties related to the hole mobility of the GeSn pTFT, the electronic structure and hole effective mass were computed based on first principles. Figure 5a,b present the band structure and density of states (DOS) of Ge$_{0.875}$Sn$_{0.125}$, respectively, revealing a direct bandgap of 0.25 eV. Our calculated outcome is analogous to that of previous work, where the bandgap of GeSn is expected to turn directly when the Sn/Ge ratio is larger than 8% [33]. The contributions of each orbital in the valence band maximum (VBM) of Ge$_{0.875}$Sn$_{0.125}$ were further investigated using the total DOS, the orbital-decomposed DOS, the projected DOS of Sn, and the local DOS near the VBM, as shown in Figure 5b. These results lead to the following conclusions: (1) Both the valence band and the conduction band are primarily contributed by the Ge orbitals (Figure S7). (2) Figure 5b shows that the topmost valence band is predominantly contributed by both Ge 4p and Sn 5p orbitals, reinforcing the electron density in the vicinity of the VBM. (3) In contrast, for the region near and beyond the conduction band minimum (CBM), the major contribution is from all Ge orbitals (4s > 4p > 3d), but not the Sn orbitals, supporting the predominant contribution of Sn orbitals to the VBM. In addition, the calculated effective mass and the energy bandgap of Ge$_{0.875}$Sn$_{0.125}$ from Figure 5a are summarized in Table 1. The heavy-hole effective mass at the $\Gamma$ point ($m_{\text{hh}}^{\Gamma}$) is $-0.225 m_0$ (the unit of free electron mass), while the light-hole effective mass at the $\Gamma$ point ($m_{\text{lh}}^{\Gamma}$) is $-0.028 m_0$, indicating that the heavy-hole effective mass dominates the total transport mass. Table 1 also shows that the $m_{\text{hh}}^{\Gamma}$ of Ge$_{0.875}$Sn$_{0.125}$ is less than that (0.28 $m_0$) of Ge and half that of Si (0.49 $m_0$) [51]. This is the reason why GeSn has been proposed for pMOS or pTFT. However, the reported GeSn pTFTs in the literature suffered from poor $I_{\text{ON}}/I_{\text{OFF}}$ [26–29], which is due to the leakage current of the small energy bandgap.
Figure 5. (a) The band structure and (b) the total density of states (DOS), the orbital-decomposed DOS, the projected DOS of Sn, and the local DOS near the VBM (insert) of Ge_{0.875}Sn_{0.125}.

Table 1. Comparison of effective masses at gamma of heavy-hole (m_{\text{hh}}^\Gamma, in m_0) and light-hole (m_{\text{lh}}^\Gamma, in m_0) direct and indirect bandgaps (E_{g,\text{direct}} and E_{g,\text{indirect}} in eV) of Ge_{0.875}Sn_{0.125}, Ge [51], and Si [51].

| Reference | Material        | m_{\text{hh}}^\Gamma (m_0) | m_{\text{lh}}^\Gamma (m_0) | E_{g,\text{direct}} (eV) | E_{g,\text{indirect}} (eV) |
|-----------|----------------|-----------------------------|----------------------------|--------------------------|---------------------------|
| This work | Ge_{0.875}Sn_{0.125} | 0.225                       | 0.028                      | 0.25                     | –                         |
| 52 work   | Ge              | 0.28                        | 0.044                      | –                        | 0.66                      |
| 52        | Si              | 0.49                        | 0.16                       | –                        | 1.12                      |

Table 2 displays the crucial TFT device parameters of various poly-GeSn TFTs [26–29]. The remarkably high I_{ON}/I_{OFF} and relatively sharp SS are the advantages of this study. The excellent device performance is due to the ultra-thin nanosheet GeSn layer, with a thickness of only 7 nm. Although the mobility can reach higher than 100 cm²/V·s with a thickness of 9 nm, the SS and I_{ON}/I_{OFF} values are degraded and unfavorable for transistor applications. The low process temperature (350 °C) and high-performance nanosheet GeSn pTFT in this work are promising for SoP and monolithic 3D IC applications.

Table 2. Comparison of several important parameters among various poly-GeSn TFT devices.

| Reference | Poly-GeSn Thickness (nm) | Highest Process Temperature (°C) | \(\mu_{FE}\) (cm²/V·s) @V_{DS} (V) | SS (V/Decade) | I_{ON}/I_{OFF} |
|-----------|--------------------------|----------------------------------|----------------------------------|--------------|---------------|
| 26        | 10                       | 300                              | 54 @ – 0.5                       | –            | 1.2 \times 10^2 |
| 27        | (nanowire)               | 440                              | 14.54 @ – 0.2                    | 1.87         | 5.3 \times 10^3 |
| 28        | 12                       | 500                              | 39.3 @ – 0.05                    | –            | 1.7 \times 10^4 |
| 29        | 15                       | 500                              | 20 @ – 0.05                      | 1            | 1.1 \times 10^4 |
| This work | 9                        | 350                              | 103.8 @ – 0.1                    | 1.56         | 75            |
| This work | 7                        | 350                              | 41.8 @ – 0.1                     | 0.31         | 8.9 \times 10^6 |
4. Conclusions

In this study, a high-performance poly-GeSn pTFT was achieved with an excellent transistor performance (41.8 cm²/V s), a sharp SS (0.31 V/dec), and a large \( I_{ON}/I_{OFF} \) value (8.9 × 10⁶). This was achieved using an ultra-thin (7 nm) nanosheet GeSn layer that can be depleted by gate and surface potentials. The high hole mobility is related to its small heavy-hole effective mass, \( m_{hh} \approx 0.225m_0 \). The remarkably high performance and low thermal budget of the nanosheet GeSn pTFT are an enabling technology for CTFTs, SoP, monolithic 3D ICs, and 3D brain-mimicking ICs.

Supplementary Materials: The following are available online at https://www.mdpi.com/article/10.3390/nano12020261/s1, Figure S1: Optimized structure of the diamond cubic Ge\(_{0.875}\)Sn\(_{0.125}\) model with the lattice constant of 5.763 Å, containing eight atoms by first-principles calculations, Figure S2: The \( I_{DS} \) vs. \( V_{GS} \) characteristics of the GeSn/SiO\(_2\)/HfO\(_2\) pTFTs with different channel thickness, Figure S3: The cross-sectional TEM image of GeSn pTFT with GeSn annealed at (a) 300 and (b) 350 °C, Figure S4: The surface roughness of GeSn films annealed at (a) 300 °C, (b) 350 °C and (c) 400 °C measured by AFM, Figure S5: The \( I_{DS} \) vs. \( V_{GS} \) and \( \mu_{FE} \) vs. \( V_{GS} \) characteristics of the GeSn pTFTs with 7 nm channel thickness and annealed at 300 °C, Figure S6: The XPS spectrum of Ge\(_{0.875}\)Sn\(_{0.125}\), Figure S7: Total density of state (DOS) and projected DOS of Ge and Sn of Ge\(_{0.875}\)Sn\(_{0.125}\) by first-principles calculations.

Author Contributions: T.J.Y. did the experiments; A.C. is the principal investigator (PI) to monitor the project; W.K.C. and H.-Y.T.C. did the simulation; V.G. is the co-PI for this work. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the Ministry of Science and Technology of Taiwan, project no. 110-2221-E-A49-137-MY3 and 108-2112-M-007-023-MY3. The computing resource were supported by TAIWANIA in the National Center for High-Performance Computing (NCHC) in Taiwan.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data presented in this study are available on request from the corresponding author. The data are not publicly available due to privacy.

Acknowledgments: We would like to thank the National Yang Ming Chiao Tung University Nano Facility Center and the Taiwan Semiconductor Research Institute for providing the laboratory instruments. We would also like to thank C.C. Huang for assisting in the device fabrication during his master’s degree study.

Conflicts of Interest: The authors declare no conflict of interest.

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