LETTER

A Compact Model for Dual-Gate GaAs PHEMT and Application for Power Amplifier Design

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Abstract A compact model of the biased dual-gate GaAs pHEMT device is proposed. The biased dual-gate pHEMT is considered as one macro unit to simplify the model and facilitate simulation. We derive the model based on analytical formulation and represent it with a simplified circuit containing only eight elements. The extrinsic elements are extracted using improved open-short method with a larger frequency range than traditional method. The simulated S-parameters based on the proposed model agree with the measured results well up to 40 GHz for 0.25 \(\mu\)m dual-gate GaAs pHEMT devices. In addition, the large-signal model is constructed with a new empirical drain current model. A 2.4 GHz power amplifier (PA) is designed using the proposed model, and the measurement results agree well with the simulation.

key words: Dual-gate, GaAs PHEMT, device modeling

Classification: Electron devices, circuits and modules (silicon, compound semiconductor, organic and novel materials)

1. Introduction

With the rapid development of fifth-generation (5G) communication, the GaAs technology is attractive for RF tranceivers because of the requirements for high power, efficiency and linearity \([1]\). The cascode configuration provides an approach often employed in monolithic integrated circuits (MMIC) to obtain higher output resistance and reduce Miller effect \([2, 3, 4, 5]\). However, as the frequency spectrum of 5G communication allocated from below 6 GHz up to millimeter-wave range, the unwanted parasitic effects become a major issue that degrades performance. Thus the dual-gate device technology has been utilized in many RF circuits to minimize parasitics \([6, 7, 8, 9]\). Unfortunately, many foundries do not provide compact dual-gate GaAs pHEMT model to support accurate and efficient circuit design. Using two independent single-gate device models inevitably introduces extra parasitics that does not exist, and deteriorates design accuracy.

Compared with single-gate device modeling, only a few researches focus on dual-gate device modeling. Due to a large number of elements to be determined at different biases, it is hard to realize a compact and accurate small-signal model of a dual-gate device. The typical small-signal model contains two single-gate models in cascode configuration \([10, 11]\), which cannot be directly extracted even by using three-port measurement. A conventional resolution is to model the dual-gate device by assuming one gate at linear region as a resistor and modeling the other gate using single-gate model \([12, 13]\). However, it is hard to construct a large-signal model due to such complicated procedures and sophisticated small-signal models. Dual-gate device large-signal model has been proposed by \([14, 15, 16, 17]\). These methods are all based on stacking two similar single-gate devices. This approximation presents fairly complex optimization, because the drain (\(D_1\)) and source (\(S_2\)) of equivalent single-gate devices are merged, which makes the two equivalent single-gate devices different and the voltage of \(D_1/S_2\) immeasurable as shown in Fig. 1(a).

![Fig. 1](image)

Fig. 1 (a) Symbol of dual-gate device. (b) Symbol of biased dual-gate device.

In order to realize a compact dual-gate device model, the second gate \((G_2)\) is considered as an independently biased thyristor. Because microwave LNA and PA designs often use dual-gate devices with a biasing resistor and decoupling capacitor at the second gate \((G_2)\), as shown in Fig. 1(b). This technique is often applied to optimize amplifier’s isolation, stabilities and other performances with the second gate effectively attaching to a RF ground through the added capacitor \([18, 19, 20]\). Under this condition, the dual-gate GaAs pHEMT device can be simplified as a two-port device.

In this paper, we propose a simplified model based on biased dual-gate pHEMT. Device intrinsic elements can be extracted with only one set of S-parameter measurement under different biases. Compared with conventional dual-gate models, the proposed model contains only eight
2. Compact Model for Dual-Gate GaAs PHEMT

2.1 Intrinsic Elements Extraction

We simplify the parameter extraction by converting the two-port network into a Y-parameter network, as shown in Fig. 2. The two-port Y-matrix can be derived:

\[
Y = \begin{bmatrix}
Y_1 + Y_2 + Y_3 + Y_4 + k_3 g_{sd} e^{j\omega t} & -Y_6 \\
-Y_5 & Y_1 + Y_3 + Y_4 + k_3 g_{sd} e^{j\omega t}
\end{bmatrix}
\]

(1)

where Y₁, Y₂, Y₃, Y₄, Y₅ and Y₆ represent the Y-parameter of subcircuit shown in Fig.1(b), and M, k₁ and k₂ can be written as:

\[
M = Y_1 + Y_2 + Y_4 + Y_6 + k_3 g_{sd} e^{j\omega t},
\]

(2)

\[
k_1 = \frac{1}{1 + j\omega C_{gs} R_i},
\]

(3)

\[
k_2 = \frac{1}{1 + j\omega C_{gs} R_{ds}}.
\]

(4)

2.2 Extrinsic Elements Extraction

To measure the performance of the dual-gate device, interconnections and ground-signal-ground (GSG) pads are incorporated in the device under test. Thus, it is essential to remove the influence caused by these additional structures.
With the second gate effectively attaching to the RF ground, the parasitic network can also be treated as a two-port network. Traditional open-short method was often used to extract parasitic elements [21, 22, 23].

Since the traditional open-short method is valid below 10 GHz, an improved open-short de-embedding method is proposed that increases modeling accuracy with consideration of series inductance in open structure. All the required elements can be extracted using analytical formulas. The proposed equivalent circuit of parasitic elements is shown in Fig. 4(a). To simplify the extraction procedure, the equivalent circuit of open structure is transformed from a Δ structure to a T structure, which is shown in Fig. 4(b). The imaginary part of Z parameter can be expressed as

$$\omega \text{Im}(Z_{i}) = \omega \nu(L_{i} + L_{a}) \left( \frac{1}{C_{r}} + \frac{1}{C_{g}} \right)$$ (21)

$$\omega \text{Im}(Z_{sg}) = \omega \nu L_{is} - \frac{1}{C_{g}}$$ (22)

$$\omega \text{Im}(Z_{gd}) = \omega \nu(L_{i} + L_{a}) \left( \frac{1}{C_{r}} + \frac{1}{C_{g}} \right)$$ (23)

Inductance and capacitance can be calculated using a linear regression and the parasitic capacitance can be calculated as follows:

$$\frac{1}{C_{st}} = \frac{1}{C_{r}} + \frac{1}{C_{o}} + \frac{C_{s}}{C_{r}C_{o}}$$ (24)

$$\frac{1}{C_{sr}} = \frac{1}{C_{r}} + \frac{1}{C_{s}} + \frac{C_{r}}{C_{s}C_{r}}$$ (25)

$$\frac{1}{C_{so}} = \frac{1}{C_{o}} + \frac{1}{C_{s}} + \frac{C_{o}}{C_{s}C_{o}}$$ (26)

After removing the influence of parasitic elements of open structure, the parasitic elements of short structure can be extracted from measured Z-parameters.

3. Dual-gate Nonlinear Model

Drain current is the prime source of nonlinear device behavior. Most published models deal with the dual-gate device as a cascode connection of two current sources [16, 17]. However, this approximation can’t fit the measured data directly, which causes fitting error. On the other hand, a few neural models [24, 25] and empirical models [26, 27] deal with the dual-gate device as one current generator. Although neural models are able to characterize the anomalies in devices due to its dynamics, these models often result in a slow convergence in the simulation. Empirical models provide expressions which facilitate simulation. However, empirical models need large numbers of parameters to improve accuracy. Ibrahim [27] proposed the empirical drain current model that outperforms Jenner’s model [26], which simplify the model from 165 parameters to 49 parameters.

To further simplify the dual-gate drain current model, a new empirical model with 37 parameters is presented. The drain current of dual-gate GaAs pHEMT is fitted by the following model:

$$I_{d} = I_{d}(V_{G1}, V_{G2})I_{d}(V_{G1}, V_{G2}, V_{D})$$ (27)

$$I_{d}(V_{G1}, V_{G2}) = 1 + \tanh(\alpha V_{G1} - \Psi_{0}) + \alpha V_{G1} - \Psi_{0} + \alpha_{1}(V_{G1} - \Psi_{0})^{3}$$ (28)

$$\Psi_{0} = \alpha_{1} V_{G1} + \alpha_{2} V_{G1}^{2}$$ (29)

$$\alpha = \alpha_{1} + \alpha_{2} V_{G1} + \alpha_{3} V_{G1}^{2}(i = 0, 1, 2)$$ (30)

$$I_{d}(V_{G1}, V_{G2}) = 1 + \tanh(\beta V_{G1} - V_{ps}) + \beta V_{G1} - V_{ps} + \beta_{1}(V_{G1} - V_{ps})^{3}$$ (31)

$$\beta = b_{0} + b_{1} V_{D} + b_{2} V_{D}^{2}(i = 0, 1, 2)$$ (32)

$$I_{d}(V_{G1}, V_{G2}, V_{D}) = c_{0} \left[ 1 + K_{o} V_{D} \right] \tanh(K_{o} V_{D})$$ (33)

$$K_{o} = c_{2} \left[ 1 + (c_{1} + c_{2} V_{G1} + c_{3} V_{G1}^{2}) (c_{4} + c_{5} V_{G2} + c_{6} V_{G2}^{2}) \right](i = 0, 1, 2)$$ (34)

where $\Psi_{0}$ is the voltage of $G_{1}$ changing with the voltage of $G_{2}$ for maximum transconductance. $K_{o}$ controls the slope of drain current at saturation region. $K_{1}$, $\alpha$, and $\beta$ are the fitting parameters.

The other nonlinear elements are extracted from small-signal model by using muti-bias S-parameter measurements. The large-signal model is built from intrinsic elements varied with bias ($V_{G1}$, $V_{G2}$ and $V_{D}$) and the current source is modelled based on our proposed drain current model. Then, we summarize these nonlinear parameters into a large-signal model using verilogA language.

4. Experiment Results

To verify the proposed model, two-port S-parameters are measured under different bias conditions on dual-gate 0.25 μm GaAs pHEMTs with gates width 4 × 125 μm and 8 × 125 μm. The DC characteristics are measured by Keysight B2902A. S-parameters are measured using Keysight N5247A VNA. In Fig. 4(b), the procedure to determine the parasitic elements of open structure is illustrated. $L_{g1}$, $L_{d1}$ and $L_{st}$ can be determined from the slopes of three straight lines. $C_{gd}$, $C_{gs}$ and $C_{os}$ can be calculated from the intercepts of three straight lines. Then the extracted elements are de-embedded from short structures, $L_{g2}$, $L_{d2}$, $L_{s}$, $R_{p}$, $R_{d}$ and $R_{s}$ can be easily extracted from measured Z-parameters. Fig. 6
shows a comparison of S-parameters simulated by using the proposed method and the traditional open-short method respectively. It can be seen that the proposed model characterizes the performance of open structure and short structure more accurately up to 40 GHz.

Fig. 5 Measured data and linear regression to calculate parasitic elements of open dummy structure.

![Image](image1)

Fig. 6 Comparison among measured S parameters (red circle), simulated S parameters by using the proposed method (blue triangle) and traditional method (black cross) from 500 MHz to 40 GHz.

![Image](image2)

Fig. 7 (a) Measured (red square) and simulated (blue circle) two-port S-matrix of dual-gate pHEMT with $V_{D}=5$ V, $V_{G1}=0.6$ V, $V_{G2}=1$ V from 500 MHz to 40 GHz.

Subsequently, the influence of extrinsic elements is removed from the measured S-parameters of dual-gate device, and the intrinsic elements are derived by using the method mentioned above. The simulated S-parameters based upon the built small-signal model and the measured S-parameters are compared in Fig. 7(a) and Fig. 7(b).

To quantify model accuracy, an error function is defined by:

$$EF = \sqrt{\frac{1}{N} \sum_{i=1}^{N} \sum_{j=1}^{N} \frac{|S_{ij}^{(m)} - S_{ij}^{(c)}|^2}{|S_{ij}^{(c)}|^2}}$$

where $S_{ij}^{(m)}$ is the measured S-parameters, $S_{ij}^{(c)}$ is the calculated S-parameters, and $N$ is the number of frequencies. The EF represents the error between the measured and calculated S-parameters. As shown in Fig. 8, the EF of the proposed models with gates width $4 \times 125$ μm and $8 \times 125$ μm are presented. The average error of proposed model is about 6.4%, which proves that the proposed method gives an accurate result to the measured S-parameters. Tab. 1 summarizes the previously proposed dual-gate model. The presented dual-gate model demonstrates wide frequency range and good fitting error.

![Image](image3)

Fig. 8 Errors between simulated and measured S-parameters with the bias of $V_D=3$ V $- 5$ V, $V_{G1}=0.2$ V $- 0.6$ V when $V_{G2}=1$ V and $V_{G1}=0.8$ V $- 1$ V when $V_{G1}=0.5$ V.

![Image](image4)

Table 1. Comparison of dual-gate device model.

| Ref. | Process   | parameter | Freq. (GHz) | port | EF  |
|------|-----------|-----------|-------------|------|-----|
|      | This work | pHEMT     | 8           | 0.5-40 | 2   | 6.4 |
| [11] | MESFET    | 14        | 2-11        | 3    | 9.8 |
| [13] | MESFET    | 14        | 1.5-11      | 3    | <10 |
| [17] | CMOS      | 12        | 0.5-15      | 3    | N/A |

![Image](image5)

Fig. 9 Comparison of measured (symbols) and simulated (solid) 1-V characteristics of a $8 \times 125$ μm dual-gate pHEMT. (a) $V_{G2}=0.6$ V, $V_D=0$ V $- 5$ V with a step of 0.1 V and $V_{G1}=0.2$ V $- 0.65$ V with a step of 0.05 V. (b) $V_{G2}=1.0$ V, $V_D=0$ V $- 5$ V with a step of 0.1 V and $V_{G1}=0.2$ V $- 0.65$ V with a step of 0.05 V. After extracting small-signal model at different bias conditions, the large-signal model is constructed as proposed. The model prediction and the measured I-V characteristics are shown in Fig. 9, and the measured and
simulated transconductance are compared in Fig. 10. As can be observed, good agreement between model prediction and the measurement is obtained.

![Fig. 10](image)

Fig. 10 Comparison of measured (symbols) and simulated (solid) transconductance of a $8 \times 125 \mu m$ dual-gate pHEMT. (a) $g_{m1}$ at $V_{G1} = 0.6 ~ 1.0 V$ with a step of 0.1 V, and $V_{G2} = 0.2 V ~ 0.6 V$ with a step of 0.05 V. (b) $g_{m2}$ at $V_{G1} = 0.4 V ~ 0.7 V$ with a step of 0.05 V, and $V_{G2} = 0.5 ~ 1.4 V$ with a step of 0.1 V.

5. Power Amplifier design and Verification

To evaluate the large-signal model, a single-stage 2.4 GHz power amplifier is designed using the proposed dual-gate device model. The schematic is shown in Fig. 11. Two paralleled devices ($8 \times 125 \mu m$) are power combined to boost output power.

An adaptive bias circuit is used to bias the power amplifier, as shown in Fig. 11(a). A dual-pHEMT self-compensating current source is used to sense the changes in each of the devices. With the input power varying, the voltages at the gates of the power devices remain constant due to the compensation voltage change between the gate and source of pHEMT H3. Therefore, the bias circuit provides high linearity even with the variation of input power and temperature. With power devices adaptively biased, the power amplifier can operate in class-B mode to achieve both high output power and efficiency.

![Fig. 11](image)

Fig. 11 (a) Schematic of the bias circuit. (b) Schematic and photograph of the designed PA.

The total chip size is 0.38 mm by 0.6 mm. As shown in Fig. 11(b), the chip is mounted on a printed circuit board (PCB) by gold bonding wires. Input and output matching networks are designed off the chip to transform 50 ohm to the desired impedance on chip. The matching networks are carefully designed using lumped devices considering the parasitics of bonding wire, pads and transmission line. The designed power amplifier achieved flat gain in a broad frequency range.

Fig. 12(a) shows the measured and simulated S-parameter in the frequency range from 100 MHz to 4 GHz. The supply voltage $V_{CC}$ is 5 V, and the Gate2 voltage $V_{G2}$ is 1.5 V. The control voltage of bias circuit $V_{bias}$ is 1.5 V, and drain voltage of bias circuit $V_{ds}$ is 1.5 V as well. The measured small-signal gain achieves 20.5 dB with a fluctuation within $\pm 1$ dB from 0.9-2.4 GHz. The large-signal characteristic is measured at 2.4 GHz. Fig. 12(b) shows the simulated output power, power gain and power-added efficiency and the measured results. A 1 dB output compression point of 23.4 dBm is achieved. The power gain is about 18.5 dB at 2.4 GHz, and the PAE is approximately 39.9%. As shown in Fig. 12(a) and (b), the simulation results and measurement results agree with each other, validating that the proposed model can predict the small-signal and large-signal performance with good accuracy.

Tab. II summarizes the performance of this work compared with previously reported power amplifier using GaAs pHEMT technology. The presented power amplifier demonstrates good power gain with only one stage, and competitive PAE and P1dB are achieved.

![Tab. II](image)

Table II. Comparison of PA using GaAs pHEMT technology.

| Ref. | GaAs Process (um) | Freq. (GHz) | Gain (dB) | PAE (%) | P1dB (dBm) | Die size (mm²) |
|------|-------------------|-------------|-----------|----------|------------|---------------|
| This work | 0.25 | 0.9-2.4 | 20.5 | 39.9 | 23.4 | 0.228 |
| [28] | 0.15 | 2.4 | 7.51 | 31.7 | 14.01 | 0.84 |
| [29] | 0.15 | 2.6-5 | 25.5 | 51.5 | - | 9.62 |
| [30] | 0.25 | 3.5 | 16.1 | 22 | 23 | 3.2 |
| [31] | 0.15 | 0.5-7 | 14 | 24 | 29 | 7.5 |

6. Conclusion

A simplified dual-gate model has been proposed. The extrinsic elements are extracted using improved open-short method which performs good accuracy up to 40 GHz. All intrinsic elements are directly extracted from the measured
two-port S-parameters under different biases. With only one-step measurement and eight elements to be extracted, the proposed modeling procedure is significantly simplified. The average EF of the model is 6.4% from 500 MHz to 40 GHz without any optimization. Moreover, a large-signal model is constructed from multi-bias S-parameter measurement with a new empirical drain current model. A single-stage power amplifier is designed using the proposed model. The simulated results of the amplifier also agree with the measurements, indicating a good accuracy of the compact dual-gate pHEMT model.

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