A series of modeling of plasma etching and damage reduction: vertically integrated computer aided design for device processing

Toshiaki Makabe*, Jun Matsui, Kazunobu Maeshige

Department of Electronics and Electrical Engineering, Keio University, Yokohama 223-8522, Japan

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Abstract

The present stage of a series of numerical modelings of the plasma etching processes is overviewed. Physical, chemical and electrical linkage among modules describing low-temperature plasma structure/function in a reactor, the profile and local charging evolution in a hole/trench, and electrical device damage during etching will make it possible to prepare a technology computer aided design (TCAD) for the practical purpose of prediction and design of the etching process. This system will also help us to determine device arrangement and size in the system on a chip (SoC) in a closed integration system. Vertically integrated CAD for device processing (ViaAddress) has been recently proposed by the authors. ViaAddress will also provide a tool for discussing the etching processes between process engineers and device designers in the age of nanometer-scale device technology. © 2001 Published by Elsevier Science Ltd.

1. Introduction

Low pressure radio-frequency (rf) glow discharges, named low-temperature plasmas, have been widely used in microelectronic device fabrication and in the manufacture of new material. They differ from the dc glow discharge plasmas in that the plasma is maintained in an electrodeless chamber as well as between metallic and/or dielectric electrodes. They are used to produce chemically activated neutrals (radicals) and ions, responsible for surface reactions in plasma etching and plasma chemical vapor deposition.

The 1999 edition of the International Technology Roadmap for Semiconductors (ITRS) targeted the current needs in nanometer-scale-device manufacturing [1,2]. Circuit integration progresses from the present system on a chip (SoC) (ultralarge scale integrated circuit (ULSI)) with $10^7$ transistors to that with $10^9$ transistors with a 70 nm gate length, operating with a 10 GHz clock frequency at 1% activity level in 2008 [1,2]. It is considered that the functional throughput of SoC in 2008 may be compared with that of the human brain, which has $10^{15}$ synapses operating effectively with a 1 kHz clock frequency at 0.1% activity level [3]. The achievement of the SoC’s high speed operation arises from two developments. One is the further shrinkage of the device dimension, and the other is the use of a multi-interconnect from six to nine layers to reduce the signal delay in the interconnect. Therefore, future progress in the SoC development depends strongly on the manufacturing technology used to produce nanometer-scale devices by means of plasma etching, while miniaturization requires optimization of each of the processes involved in the technology.

Currently, there is no general rule for designing the plasma etching. Under these circumstances, the industry research laboratories have focused on the challenges posed by the plasma chemical issues, in development of next-generation plasma processing and tools [4]. We, however, believe that further optimization of the plasma structure should be achieved first, and plasma chemical kinetics should be optimized later as the changes in the former may strongly affect the latter. During the past 15 years, modeling of the plasma structure and its function in the etching reactor has been developed [5]. Microscopic profile evolution of a patterned wafer and microloading during etching have been simulated independent of macroscopic plasma modeling in reactors. Plasma damage to the device during etching has been experimentally studied.

In line with the roadmap, continuous improvement of tools and processing methods lead to the reduction in the size of the features of a chip. Parallel to the development of this hardware, the next decade will bring fabrication methodology into the field of process integration. One of the promising procedures for this purpose will be the prediction of the plasma structure and processing on the wafer with the aid of numerical modeling over the entire reactor.

* Corresponding author. Tel./fax: +81-45-566-1547.
E-mail address: makabe@mke.elec.keio.ac.jp (T. Makabe).

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### Governing Equation System in Plasma Reactor

| Data Base | Governing Equations | Source |
|-----------|---------------------|--------|
| **Collision/Reaction Processes** | Boltzmann Eq. | Voltage $V(t)$ |
| **Gas-phase** | Conservation of Particles | $\mathbf{E}$-field |
| $e + A \rightarrow A^+ + B^-$ | $n$-ions (radicals) |
| $A^+ + B^- \rightarrow A + A$ | Poisson's Eq. $n$-E field |
| $A + AB \rightarrow A$ | **Maxwell's Eq.** |
| **Interface (Surface)** | **Momentum Relaxation** | **Current** $I(t)$ |
| $\Phi_W$ | electrons | Feed Gas |
| **Solid-phase** | Energy Relaxation | |
| $\Phi_e \epsilon$ | |

**Navier-Stokes Eq.**

| Boundary Conditions (Reactor wall, wafer) |
| gas flow |

Fig. 1. Governing equation system in VicAddress.

System. This will be achieved by means of the database, regarding the fundamental collision and reaction processes, both in a gas phase and on the wafer surface (Fig. 1). That is, practical application of technology computer aided design (TCAD) will extend into the backend processes, especially in plasma etching, in addition to the frontend processes, in order to elaborate the optimum conditions between the device designer and the process engineer.

Fig. 2. Overview of a series of modelings (VicAddress) of plasma structures in a two-frequency capacitively coupled reactor, plasma etching, and related damage prediction.
In this paper, we propose a series of modelings of a low-temperature plasma structure and the function in a reactor of profile evolution and charging in a patterned wafer, and of device damage during plasma etching/deposition by using modules for each of the objectives. It is named ‘vertically integrated CAD for device processing (VicAddress)’ (Fig. 1). Prediction of plasma damages to a nanometer-scale-device structure during etching will be discussed, as an example, in a two-frequency capacitively coupled plasma (2f-CCP) reactor by using VicAddress.

2. Overview of proposed VicAddress system

The system proposed here (Fig. 2) for the purpose of backend process prediction, in particular, for plasma etching involves a gas phase module, surface phase module, and bulk device module. The gas phase module provides macroscopic plasma structure/function, and the feed gas flow and particle flow produced in the gas phase and on the wafer with microscopic structures in the plasma etcher (Fig. 3) by using an extended relaxation continuum (E-RCT) model [6] under the database of microscopic collision processes and external plasma conditions. It uses direct numerical procedure (DNP) of the phase space Boltzmann equation when at need, under the result of the plasma structure, to predict the velocity (or energy) distribution of ions, electrons, and high energy neutrals in front of the wafer [7–10]. The surface module works as a future profile predictor at etching and for predicting plasma damage. The bulk device module predicts the plasma damage and the critical size of the device element in SoC (or ULSI) by the aid of plasma parameters under the circumstances of the aspect ratio of a trench/ hole size and a geometrical antenna profile.

It aims at an optimum plasma design in a reactor and at the avoidance of plasma damage during etching/deposition by means of low-temperature plasma control or revision of the device arrangement and the size. The system VicAddress will provide a TCAD tool to align the backend etching/deposition processes between the process engineer and the device designer in the industry.

3. Plasma etching reactor design

The low-temperature plasma used in micro and nanoelectronic device manufacturing is maintained even in an electrodeless chamber as well as between metallic and/or dielectric electrodes. A compact apparatus with high-density plasma, exactly speaking, with flux and energy uniformly distributed on the wafer surface is required for the next generation of the etching reactor, which will have a high rate of surface treatment on a large-area wafer. High-density plasma is produced by using an ac power source in the range of high-, very high-, and ultrahigh-frequencies with or without the aid of external magnetic field. The dry etching reactor is classified into three types according to the coupling system between the external ac power source and the plasma. These are named capacitively coupled, inductively coupled, and antenna coupled plasmas (Fig. 3). The wafer to be processed in the reactor is usually biased by a low frequency (LF) voltage source in order to obtain anisotropic etching with high efficiency.

Plasma etching is applied to metal(Al), poly-Si, and dielectric(SiO2, low-k materials). Metal and poly-Si etching use a high-density plasma with low energy ions on the wafer, while the latter SiO2 etching is executed by ion-assisted processing using a few hundred eV or more.

3.1. Two-frequency capacitively coupled plasma structure and its function

The modern oxide etcher has to separate the function of plasma sustaining and biasing electrodes. In our previous paper, separation of the effects of rf sources used for biasing
ions hitting the wafer surface without perturbing the plasma.

2. The reduction in excessive dissociation of CF-radicals improves the selectivity of the etching in the CxFy/Ar system.

Reducing the device dimension, the high aspect ratio etching of the contact hole or trench is influenced by a local charge accumulation inside the structure. This is known as anomalous etching. Otherwise, charging on metal in a period of over-etching causes critical damage to the thin gate oxide, known as antenna effect [12,13]. The damages to the wafer with topographically different surface structure are intrinsic to high-density plasma etching. Fig. 5 describes the predicted axial number density distributions of the charged particles and the metastable argon in temporally averaged form in the VHF(100 MHz)–LF system, obtained by the RCT modeling. The plasma density with $10^{11} \text{cm}^{-3}$ spreads widely between both electrodes due to the influence of the spatial trapping of low energy electrons, as compared with that driven by the HF(13.56 MHz)–LF system. In order to overcome plasma damage occurring during the etching process, pulsed operation of a high-density plasma source was proposed in order to aim at the control of positive and negative charge flux to the surface during the on/off period [14]

3.2. Ion velocity distribution incident on wafer

SiO$_2$ etching requires a high energy ions incident on the patterned wafer. The energy is distributed between 200 and 1000 eV in order to obtain a sufficient etching yield of SiO$_2$ under the ion assisted mode in feed gases based on Ar and fluorocarbon mixture.

One of the physical issues in oxide etching is the prediction of the velocity distribution of ions incident on the wafer as a function of frequency and amplitude of the bias voltage, though a number of experimental distributions have been observed. As is well known, at high frequency, the ion has no sufficient time to cross the space between the electrodes during the half-period, the ion transport is characterized in a time-averaged fashion. Thus, the ion velocity distribution is estimated as a function of distance from the sheath–bulk plasma boundary. This means that a time-independent Boltzmann equation can predict with validity the distribution at high frequency and VHF ranges [7].

Since at frequencies an ion will temporally relax the energy to the instantaneous field, we have to consider the space and time characteristics of the ion velocity by using the time-dependent Boltzmann equation. At low frequency the ion can go across the sheath instantly in front of the wafer during the half-period of the bias voltage, and the ion velocity is numerically obtained from the time-independent Boltzmann equation under a local sheath field in each phase of the external wafer voltage. In Fig. 6, we show the typical example of the energy distribution of ions, Ar$^+$. 

Fig. 4. Example of the functional separation in oxide etcher in 2 frequency-CCP reactor, sustained at 100 MHz and 300 V, and biased at 1 MHz at 50 mTorr in CF$_x$Ar. (a) 2D electron number density at bias amplitude of 500 V, (b) normalized electron number density as a function of bias amplitude.
incident on the biased wafer at 1 MHz and 500 V at 50 mTorr in CF₄(5%)/Ar in 2f-CCP in two modes [10]. That is, Fig. 6(a) describes the time dependence, \( f_0(\varepsilon, r; r = 0) \) at the center of the wafer, \( r = 0 \). The radial characteristics, \( f_0(\varepsilon, r) \) are shown in Fig. 6(b) in a time-averaged form. Complete time modulation of the ion energy during the period at 1 MHz and the degree of radial uniformity are predicted from the gas-phase module in VicAddress.

### 3.3. Ejected nonvolatile particle transport

Ideal dry process will produce gas phase molecules of the surface materials after physical and chemical reactions during plasma etching. In a practical ion assisted etching, a nonvolatile as well as volatile particles are detected in the reactor. The nonvolatile particle, ejected nonuniformly from the wafer surface by the impact of energetic ions during etching, is transported from the surface through a high sheath field region with initial nonthermal high energy under the circumstances of the external feed gas flow in the reactor. A finite amount of the etched particles will be reabsorbed on the wafer surface by back diffusion, ionized mainly between the sheath and the bulk plasma, or deposited on the reactor wall. The nonvolatile particles may accumulate and coagulate with each other at specific points or regions in the reactor. Otherwise, they will be pumped out with a feed gas. The transport proper to the nonvolatile particles is numerically predicted.

Fig. 7 shows the 2D density distribution of the Si atom steadily ejected from the wafer of 140 mm in diameter in 1f-CCP driven at 100 MHz and an amplitude of 300 V at 50 mTorr in CF₄(5%)/Ar. The spatial distribution with the axial peak at 3 mm from the wafer is the result of the collisional energy relaxation of the ejected high energy neutral Si atom with the feed gas, and of the ionization by the electron impact since the ionization threshold of Si, 8.15 eV is much lower than that of the feed gases, Ar and CF₄, 15.6 and 16 eV. In fact, the effect of the ionization reduces the neutral Si density by 6%. It is reported that in a high-density plasma with \( 10^{12} \) cm⁻³ at low pressure, almost 50% of the ionization to sustain the plasma is supplied by way of the ejected metallic atom from the metal target. These will change the original plasma structure maintained purely in the feed gas.

The exhaustive path of nonvolatile particles ejected with an initial nonthermal energy at the wafer surface is
practically important for the reactor design as well as the feed gas flow. Flow design of the feed gas, supplied from the showerhead on the electrode, is a well-established technique obtained by the Navier–Stokes equation or direct simulation Monte Carlo (DSMC) [15,16]. In particular, DSMC suited for the problem of rarefied gas dynamics. At intermediate pressure, 25–50 mTorr, the momentum transfer theory can effectively estimate the transport of the nonvolatile particles as shown in the form of 2D flow velocity distribution in Fig. 8 (see Ref. [6]). It can be concluded from this typical example that the flow pattern of the nonvolatile particle is completely different from the feed gas flow in the oxide etcher.

4. Charging inside a microstructure

By increasing the device integration and shrinking the SoC’s, or ULSI’s size, topographical nonuniformity and/or potential localization on the microscopically patterned wafer will be provided during plasma etching for a high aspect ratio or large antenna ratio hole/trench. It will grow further in a multi-layer interconnect system with 9 or 10 layers. Under these circumstances, technological development in uniform etching without producing microloading (RIE-lag) and damage is an urgent issue in plasma processing.

4.1. Microtrench and etch stop

The influence of physical and electrical properties of plasma etching on the inside of a microtrench with/without surface conductivity is estimated by studying the growth of the local potential by using Monte Carlo simulation of ion and electron transport with the aid of surface-charge-continuity and Poisson’s equation under the information of the fluxes and energies incident on the wafer [17]. When the aspect ratio increases, the bottom is charged to the potential sufficient to prevent all the incident ions within the period of monolayer stripping under a practical set of conditions, and the etch stop occurs. Fig. 9 shows the temporally saturated potentials on the top part of the side wall and the trench bottom as a function of aspect ratio in the case of no surface conductivity [17]. In a practical RIE with a typical fluxes of $10^{16}$ cm$^{-2}$ s$^{-1}$ of electrons and ions, and an etch rate of 500 nm min$^{-1}$, a monolayer in SiO$_2$ is apparently stripped at intervals of hundreds of ms.

Under these circumstances, we will predict the relations of the time constant between the charging ($\tau_{\text{charge}}$) and the monolayer stripping ($\tau_{\text{Monetch}}$) at very high aspect ratio etching. $\tau_{\text{charge}} \approx \tau_{\text{Monetch}}$. The results show that charging may become the cause of etch stop and associated problems in oxide etching at high aspect ratios. It is still possible that both chemical and physical mechanisms may occur at the same time because the mechanism presently described is the limiting mechanism as it is dependent only on geometry and on the initial conditions. More complex plasma chemistry may lead to a different type of ion that provide different plasma potentials, or may allow conductive deposition at the side wall or a conductive thin layer at the bottom [3].

Fig. 7. Ejected Si atom from the wafer in a conventional RIE.

Fig. 8. 2D flow velocity distribution of the ejected Si atom. External conditions are the same as those shown in Fig. 7.

Fig. 9. Charging potential dependence on aspect ratio at the bottom and the top of the sidewall of SiO$_2$ trench in the system struck by beam-ions with 300 eV and thermal electrons of 3 eV (see Ref. [14]).
5. Conclusions

Anomalous etching (microloading) in metal, Poly-Si, and SiO₂, and gate oxide damage during plasma etching are experimentally observed through processes of the further integration and the shrinkage of the device. These are urgent issues in SoC manufacturing. These phenomena are caused by the local charging of positive ions and electrons inside micro and nanostructures and are considered as functions of aspect ratio and antenna ratio on patterned wafers exposed to plasma. These difficulties may further grow in those days of SoC having a multi-interconnect with 9 or 10 layers.

Locally distributed surface charging will be one of the interesting phenomena in future nanotechnologies using low-temperature plasma because the physical mechanism of the local charging inside the micro/nanostructure exposed to the plasma is based on two proper and general characteristics of plasma, i.e. the quasi-neutrality of charges and the incident flux equality under different ranges of energies on a surface.

Numerical modeling of a low-temperature plasma in a reactor, profile evolution, local charging in a hole or trench, and electrical device damage during plasma etching have been for the most part investigated independently of each other for the last 15 years in USA, Japan and Europe. Physical, chemical, and electrical linkage among these modules will make it possible to prepare a TCAD for the practical purposes of the prediction and design of the etching process, and of device arrangement and the size in SoC in a closed integration system. Here, we proposed a VicAddress. In addition, the present proposed VicAddress will provide a tool for the discussion of the etching processes between process engineers and device designers.

It will be finally stated that the practical success of the prediction and design of the etching process by using VicAddress will depend largely on the presence of the database regarding gas and surface phases. It must be strongly emphasized in order to avoid a database crisis in TCAD application that it is increasingly essential to study fundamental collision/reaction processes both in atomic/molecular and in surface physics and chemistry.

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