Room-temperature operation of Si spin MOSFET with high on/off spin signal ratio

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Received September 30, 2015; accepted October 6, 2015; published online October 22, 2015

We experimentally demonstrate a Si spin metal–oxide–semiconductor field-effect transistor (MOSFET) that exhibits a high on/off ratio of source–drain current and spin signals at room temperature. The spin channel is nondegenerate n-type Si, and an effective application of gate voltage in the back-gated structure allows the spin MOSFET operation. This achievement can pave the way for the practical use of the Si spin MOSFET. © 2015 The Japan Society of Applied Physics

Semiconductor spintronics has been intensively studied over the past several decades. GaAs was a central material in earlier semiconductor spin devices, such as the Dass-Datta-type spin transistor.¹ Recently, Si has also become pivotal in semiconductor spintronics, because Si is ubiquitous and nontoxic, and is a light element with lattice inversion symmetry. In particular, the lattice inversion symmetry and small atomic number of Si give rise to good spin coherence, enabling its use in novel spin devices such as the Sugahara–Tanaka-type spin metal–oxide–semiconductor field-effect transistor (MOSFET).² Si spin MOSFETs can be used to construct reconfigurable logic circuits, producing logic systems with ultralow power consumption. Hence, the room-temperature (RT) operation of Si spin MOSFETs has been a significant milestone in Si spintronics. The easiest way to realize this RT operation is through electrical spin injection into Si, which has been intensely studied. Various experimental methods have been used to obtain solid evidence of a successful electrical spin injection in Si, and it is now widely recognized that a combination of a nonlocal four-terminal method,³,⁴ local methods including the three-terminal magnetoresistance (3T-MR)³ and two-terminal (2T)⁶ methods, and measurements of the Hanle effect³,⁷ is indispensable for avoiding the detection of spurious signals in the conventional local three-terminal method.⁸–¹² The first reliable spin transport in Si at RT was reported in degenerate n-type Si,¹ in which the nonlocal four-terminal method was used for the propagation of pure spin current and the observation of the Hanle-type spin precession up to RT. However, the high doping concentration of the degenerate Si impeded an effective gate-voltage application, i.e., spin MOSFET operation. In 2014, the first experimental demonstration of the RT operation of a Si spin MOSFET was achieved by using nondegenerate n-type Si.¹³ Because the Si was not degenerated, the gate voltage application allowed the gate-induced modulation of a spin signal and the source–drain current \( I_d \) simultaneously. However, these spin MOSFETs still had a low on/off ratio in both the spin signal and the source–drain current \( I_{sd} \). In this paper, we report on Si spin MOSFET operation at RT with high on/off ratios. The electrical local 2T method is used for investigating the spin MOSFET characteristics, where the spin transport is corroborated by the 3T-MR method. The on/off ratios of the \( I_d \) and spin signals are greater than \( 10^3 \) in the same Si spin MOSFET. More significantly, the gate voltage dependence of the spin signals is consistent with that of \( I_d \). This achievement can pave the way for a practical application of Si spin MOSFETs.

Our Si spin MOSFET was fabricated on a silicon-on-insulator (SOI) substrate with a structure of Si (100 nm)/SiO₂ (200 nm)/bulk Si [see Fig. 1(a)]. The upper Si layer was phosphorous (P)-doped by ion implantation. Before depositing the ferromagnetic electrodes, the Si layer in these regions was heavily doped to a concentration of ca. \( 5 \times 10^{19} \) cm\(^{-3} \). Figure 1(b) shows the doping profile of the structure, measured by secondary ion mass spectroscopy. The profile is the same as that of the spin MOSFET in the literature,¹³ because we used the same batch of SOI substrates. After the natural oxide layer on the Si channel was removed using a HF solution, Pd (3 nm)/Fe (13 nm)/MgO (0.8 nm) was grown on the etched surface by molecular beam epitaxy. Then, we etched out the Pd (3 nm)/Fe (3 nm) layers, and Ta (3 nm) was grown on the remaining Fe. In order to realize an efficient gate voltage application, the Si channel was etched.
to a depth of more than 25 nm by ion milling. The device resistivity was 4300 Ωμm, which is much higher than that of an earlier spin MOSFET (160 Ωμm\textsuperscript{13}), indicating that the etching process effectively removed the highly doped region from the surface of the Si channel. The contacts had dimensions of 0.5 × 21 and 2 × 21 µm\textsuperscript{2}, respectively. The Si channel surface and sidewalls at the ferromagnetic contacts were buried by SiO\textsubscript{2}. The nonmagnetic electrodes, with dimensions of 21 × 21 µm\textsuperscript{2}, were made from Al and produced by ion milling. The gap between the FM electrodes was set to be 4.26 µm. The gate voltage was applied from the back side of the device. The conventional FET and spin MOSFET characteristics were investigated by using a probing station (Janis Research ST-500), a source meter (Keithley Instruments 2400 and 2401), and a digital multimeter (Keithley Instruments 2010). All measurements were performed at RT.

Figure 2 shows the principle of detecting spin signals in the 3T-MR and 2T methods used in this study. As reported in the literature,\textsuperscript{5} the 3T-MR method is another reliable method for realizing spin transport (not only spin accumulation), and resistance hysteresis due to spin transport can be observed, which is the central difference from the conventional local three-terminal method. The ferromagnetic electrode was set downstream of the spin flow, acting as a spin detector. Because the spin flow in the Si is affected by the spin drift effect caused by an electric field in the Si,\textsuperscript{14,15} the downstream side experiences efficient spin accumulation. Because the spin direction in two ferromagnetic electrodes is controlled by an external magnetic field parallel to the Si channel, the alignment of the spin direction of the detector electrode and the accumulated spin beneath the detector electrode (= the propagating spin in the Si) are controlled to be parallel or antiparallel, yielding the resistance hysteresis. A more quantitative and detailed discussion will be reported elsewhere.\textsuperscript{16} On the contrary, spin accumulation at both the spin injector and detector electrodes can be measured by using the local 2T method. Notably, anisotropic magneto-resistance and other spurious signals can superimpose on the signals detected using the local method, so experiments should be conducted with utmost care. We used both methods to corroborate spin transport in the Si spin MOSFET at RT.

Figure 3(a) shows the magnetoresistance, including the minor loop, observed with the 3T-MR method. At an electric current of 1 mA, the magnitude of the magnetoresistance was measured to be 0.38 Ω. The magnetic fields, where the hysteresis and the minor loop appeared, are consistent between the measurements, showing that the magnetoresistance is ascribed to a successful spin transport in the Si spin MOSFET at RT. The distance of the ferromagnetic electrodes was 4.26 µm and a spin transport of 4.26 µm was realized. Such a long spin transport was achieved by spin drift in addition to spin diffusion as discussed previously.\textsuperscript{13} When
we changed the measuring method to the local 2T method with the gate voltage application, a similar magnetoresistance was observed under an applied gate voltage of +50 V, as shown in Fig. 3(b) (note that the electric current instead of the device resistance is shown). As described in the literature, on- and off-states are generated by a gate voltage (electric on/off states) as in a conventional MOSFET, and in addition, the other on- and off-states are generated by the magnetization configuration (spin on/off states). We define the spin signal of the Si spin MOSFET as the difference in \( I_{sd} \) in the parallel and antiparallel magnetization configurations, that is, in the spin on/off states, as shown in Fig. 3(c). Under a gate voltage of +50 V, the magnitude of the spin signal measured was 0.68 \( \mu \)A.

Sweeping the gate voltage from −125 to +125 V at a source–drain voltage of 4 V modulated the \( I_{sd} \) of the spin MOSFET (see Fig. 4). Because the Si is of the n-type, a positive gate voltage increases \( I_{sd} \) and a negative gate voltage suppresses \( I_{sd} \). Thus, this device exhibited a conventional MOSFET operation. The switching voltage of the device is comparatively large; in other words, the transconductance of the device is not good enough. The minimum of \( I_{sd} \) and the magnitude of the spin signals were very consistent as functions of the gate voltage, and the on/off ratios for \( I_{sd} \) and the spin signals were both greater than 10\(^3\). Because the on/off ratio was much less than 10\(^4\) in a previous study, optimizing the device fabrication process effectively improved the spin MOSFET performance. This result directly shows that the Si spin MOSFET operated successfully at RT.

In summary, we demonstrated the RT operation of a Si spin MOSFET with a high on/off ratio of \( I_{sd} \) and the spin signals. The operation was enabled by spin transport in nondegenerate Si at RT and an effective application of the gate voltage. This success can pave the way for the practical use of Si spin MOSFETs.

Acknowledgment Part of this study performed by M.S. and Y.A. was supported by a Grant-in-Aid for Scientific Research (A) from the Japan Society for the Promotion of Science.

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