A Joint Implementation for Timing Synchronization and Matching Filtering Through the Frequency Domain

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Abstract. In order to reduce the computational complexity of the high-speed satellite communication system, the article proposes an architecture that combined the timing synchronization and the matching filtering without mixing. In the architecture, the filter module and the synchronization module are improved to ensure that the filter operation results could be used in the timing synchronization module. In other words, the architecture can complete signal filtering and synchronization processing through a Fast Fourier Transform. This method can not only reduces system complexity but also reduces the amount of computation. Theoretical analysis and simulation experiments show that the architecture has better estimation performance at low signal to noise ratio and high latency environment. At the same time, this architecture effectively reduces the amount of system calculations by reusing resources between modules. Compared with the Gardner algorithm, the scheme uses in this paper can reduce about 70% of the calculation, which is suitable for high-speed demodulation system.

1. Introduction

With the development of satellite technology and on-star payload technology, the amount of data needed to be transmitted by satellites has increased sharply, which makes ground receiving system develop into high-speed broad-band processing. However, the traditional serial processing technology can not meet the real-time processing of up to Gbps sampling rate data stream because of the limitation of stable working clock frequency of the commonly used digital processor (such as FPGA)[1], so it is necessary to adopt parallel implementation structures to overcome the limitation of the clock frequency and improve the symbol rate of the system.

Generally speaking, the common parallel demodulation architecture can be divided into time-domain implementation and frequency-domain implementation. Because of the low computation and simple realization, the frequency domain parallel structure is more suitable for high-speed communication, and generally used in it.[2] With the increase of the symbol rate of the system and the increment of parallel path, the traditional frequency parallel architecture cannot meet the requirement of real-time communication. The algorithm and the architecture of the system need to be improved. The paper[3] has proposed an improved interpolation structure with reference to the Gardner algorithm, which not only improves the accuracy, but also reduces the difficulty of implementation. So far, the research on the improvement of this algorithm is quite some, and is more and more mature. The further optimization is limited. The paper [4][5][6] start with the system architecture. They effectively reduce the complexity of system and the number of the hardware resource by adopting the simplification of the mixer-free and parallel filters. The advantage of this method is that it simplifies the implementation of the system.
without changing the performance by using the fast algorithm, but does not take into account the characteristics of the algorithms between the modules, and cannot fully reuse the public resources. Therefore, this paper has made further improvement on the reuse of the public resources between system modules, and the improved parallel architecture has lower computational capacity and more applicability.

2. The architecture based on mixer-free of the parallel demodulation through frequency domain
In order to avoid the instability of the NCO(Number-Control-Oscillation) module and reduce the complexity of the architecture implementation, paper[4] introduced the mixer-free structure to the traditional parallel demodulation architecture, and improved the matching filter module. The improved architecture is shown in the figure1.

2.1. The definition of the mixer-free architecture
Suppose that \( I(t) \) and \( Q(t) \) are the in-phase and quartered-phase values of the \( I \) and \( Q \) route, \( f_c \) is the frequency of IF signal, and \( f_s \) is the sample rate. The received baseband signal can be written as:

\[
s(t) = I(t)\cos(2\pi f_c t) - Q(t)\sin(2\pi f_c t)
\]

(1)

Assuming \( 4f_c = f_s \), we can get \( s(n) \) as follows:

\[
s(n) = [I(0),-Q(1),-I(2),Q(3),I(4),-Q(5),...]
\]

(2)

From this equation, we can see that through odd-even selecting, inserting zeros and partly signal inverting, we can get the baseband signal, \( I(n) = [I(0),0,I(2),0,...] \) and \( Q(n) = [0,Q(1),0,Q(3),...] \). After low-pass-filtering operations, we can get the in-phase and quartered-phase values of the baseband signal. We may define this special structure the Mixer-Free structure.

![Fig. 1. The flow chart of parallel demodulation architecture system](image)

3. A Joint Implementation for Timing synchronization and matching filtering
In order to solve the problems such as the low utilization of system resources and avoid feedback loops, this paper intends to start with the system structure, reduce the system complexity on one band and reduce the use of resources on the other. The key point of this paper is whether the matching filter can be simplified by multiplexing.

3.1. The proposed of Joint Implementation
Through the analysis of Figure 1, the system implements the matching filter before the synchronous estimation. In other words, both in time and resource use, the two modules are completely independent. And the matching filter and Timing synchronization module take full advantage of the frequency algorithm, and both of them are based on the frequency domain, and the implementations of both need to use the algorithm. So if we can make full use of the public resources of two modules during the process of operation, we can reduce the unnecessary calculation to some extent. Based on this idea, the article proposed an architecture that combined the timing synchronization and the matching filtering without mixing. The process of the demodulation is shown in the figure2.
As is shown in figure 2, the system uses the overlap retention method to send data into the DFT module, and then uses the time domain convolution characteristics of the signal to complete the filtering and timing synchronization of the I and Q channels respectively. With this special structure, the system not only realizes the multiplexing of resources between the DFT and the timing synchronization module, but also reduces the output data rate. Which provides an effective way for system hardware resource savings, complexity reduction, and computational reduction.

3.2. Implementation of joint structure

The key to the joint filter and timing synchronization module is the multiplexing of resources, that is, how to multiplex the operation results of the matched filter module into the timing synchronization module. [7] Based on this idea, this paper mainly improves the matched filter module and the synchronous algorithm module to ensure that the signal filtering and synchronization processing can be realized by one FFT.

3.2.1. Improvement of DFT module

In a conventional demodulation system, I and Q paths are processed separately, so the system requires two DFT/IDFT modules and two filter modules. However, in the mix-free demodulation architecture, the I and Q paths are mixed and alternated. Using this feature, this paper adjusts the data and then performs Fourier transform to obtain the frequency domain values of I and Q respectively through one transformation.

3.2.2. Selection and Implementation of Timing Synchronization Algorithm

Commonly used frequency domain timing synchronization algorithms mainly include SLN, AVN, FLN and LONG. Paper [8] pointed out that under the additive Gaussian white noise channel, all four algorithms can realize the timing parameter estimation under large frequency offset conditions. In particular, the SLN algorithm is widely used due to its insensitivity to roll-off and signal modulation. Based on the above analysis, this paper uses SLN algorithm as the timing synchronization estimation algorithm.

By approximating and simplifying, the delay $\tau$ in the SLN algorithm can be expressed as follows:

$$\tau = -\frac{T}{2\pi} \arg \left\{ \sum_{i=0}^{P-1} s(i)e^{j2\pi iP} \right\}$$  \hspace{1cm} (3)

Where $s(n)$ is the input no-mix signal, $T$ is the symbol rate, and $P$ is the number of samples in one symbol.

In order to satisfy the multiplexing of the frequency domain filtering results by the synchronization module, the article understands the formula (3) from the perspective of the frequency domain. This means that we can convert the delay solving problem into a frequency domain phase solving problem.

$$\|s(n)\|^2 = \|I(n)\|^2 + \|Q(n)\|^2$$  \hspace{1cm} (4)
From equation (4), we can get $|s(n)|^2$ by calculating $|I(n)|^2$ and $|Q(n)|^2$. Using the frequency domain cyclic convolution and linear properties of DFT, we can get:

$$DFT[s^2(n)] = \frac{1}{N} S(k) \otimes S(k)$$  \hspace{1cm} (5)

$$DFT[s^2(n)] = \frac{1}{N} [I(k) \otimes I(k) + Q(k) \otimes Q(k)]$$  \hspace{1cm} (6)

Based on equation (6), the physical meaning of equation (3) can be understood as the phase value of the Lth spectral line after solving the short-time Fourier transform of sequence x with length of LP.

Based on equation (6), the solution of the delay can be transformed into the phase value of the Lth line after solving the sequence $|I(n)|^2 + |Q(n)|^2$ for the LP point Fourier transform. It can also be regarded as an average statistic of L periods for the first line after performing a short-time Fourier transform of the P point on the sequence $|I(n)|^2 + |Q(n)|^2$. The implementation flow diagram is shown in Figure 3.

![Implementation Flow Diagram](image)

**Fig. 3.** SLN algorithm frequency domain parallel implementation structure

4. **Simulation and analysis**

The article uses QPSK signals for simulation. Assume that the signal symbol rate is 600Msps, the sampling rate is 2.4GHz, the intermediate frequency signal frequency is 600MHz, the sampling frequency is 4 sampling points, and the transmitting terminal and the receiving terminal adopt the 33-order root raised cosine filter with the roll-off coefficient of 0.35.

Figure 4 (a)-(d) shows the timing synchronization of the signal under different transmission delays with a signal-to-noise ratio of 25 dB. Figure 4(e)-(f) shows the timing synchronization of the signal with a transmission delay of 3T/8 under a condition of a signal-to-noise ratio of 15dB.

![Simulation Results](image)

(a) before \( (\tau = T/8, SNR = 25dB) \)  \hspace{1cm} (c) before \( (\tau = 3T/8, SNR = 25dB) \)  \hspace{1cm} (e) before \( (\tau = 3T/8, SNR = 15dB) \)
As it can be seen from Fig. 4(a)-7(d), in the large delay environment, the phase information of the received signal is substantially destroyed, and four reference phase points are completely invisible. However, after the delay is restored, the reference phase point can be clearly seen. That is to say, the article algorithm can accurately achieve delay recovery in a demodulation environment with better signal to noise. Moreover, it can be seen from Fig. 4(e)-(f) that the algorithm can still recover the delay signal accurately in a low SNR and large delay environment. So we can draw a conclusion that the algorithm is suitable for the low SNR communication environment.

5. Conclusion

The paper proposes an architecture for the application requirements of high-speed parallel demodulation, which is based on a combination of timing synchronization and matched filtering. In the way, the architecture effectively reduces the complexity of the system by multiplexing the resources between modules, and greatly reduces the use of system hardware resources. The simulation analysis shows that the scheme has better tracking performance under the condition of low SNR and large delay. Therefore the architecture has a good application prospect.

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