Simulations of the CNFETs using different high-\(k\) gate dielectrics

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ABSTRACT

In this paper we presented the analysis of carbon nanotube field effect transistors (CNFETs) using various high-\(k\) gate dielectric materials. The objective of this work was to choose the best possible material for gate dielectric. This paper also presented the study on the effect of thickness of gate dielectric on the performance of the device. For the analysis (19, 0) CNT was considered because the diameter of (19, 0) CNT is 1.49 nm and the CNFETs have been fabricated with the CNT diameter of ~1.5 nm. It has been observed that La\(_2\)O\(_3\) is the best gate dielectric material followed by HfO\(_2\) and ZrO\(_2\). It was also observed that as thickness of gate dielectric material reduces, drain current of CNFET increases very marginally. The outcomes of this study matches with the analytical results and hence confirm the results.

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1. INTRODUCTION

For many years, silicon (Si) has been used as a basic material in the fabrication of transistors. However, the problem associated with attempting to scale down traditional semiconductor devices (Si-MOSFET) have led researchers to look into other material devices such as carbon nanotube field effect transistors (CNFETs) as alternative. Carbon nanotubes (CNTs) have been the subject of a lot of scientific research in recent years, not only due to their small size but also because of their remarkable mechanical properties, electronic (high mobility, high transconductance and high current density) properties [1] and many potential applications [2, 3]. As shown in Figure 1, based on the chirality, CNTs can be classified into two types: chiral CNT and achiral CNT. Achiral CNT is further divided into Zigzag CNT and Armchair CNT. Figure 2 shows the schematic view of these CNTs. The diameter (\(d\)) and energy band gap (\(E_g\)) of CNT is calculated by following (1-2) [4]:

\[
d = 0.078 \times \sqrt{n^2 + m^2 + nm}
\]

\[
E_g = \frac{2a_{33t}}{d} \approx \frac{0.8}{d}
\]

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where (n, m) are chirality of CNT, $a_{cc}$ is nearest neighbor C-C bonding distance (~0.142 nm) and t is the tight binding energy (~3 eV). The diameter of the SWCNT ranges from 0.5 nm to 5 nm [5].

Figure 1. Classification of carbon nanotubes

![Figure 1](image1.png)

Figure 2. Schematic view of carbon nanotube, (a) Chiral (12, 9) (b) Armchair (9, 9) and (c) Zigzag (19, 0)

CNFETs are being studied for a wide variety of applications, including logic devices, memory devices, sensors etc. However, to predict the ultimate performances of these novel nano devices and to further offer guidance and cost reduction of the technological development, accurate and reliable simulation tools appear as key issues. The performance of CNFET depends on gate dielectric, source and drain materials. It is well established fact that reduction in device dimension leads to increase in leakage current. One way to reduce the possibility of leakage current is to use high-$k$ dielectric materials as gate. Commonly reported high-$k$ dielectrics include Hafnium oxide (HfO$_2$), Alumina (Al$_2$O$_3$), Hafnium Silicate (HfSiO$_4$), Zirconia (ZrO$_2$), Yttrium Oxide (Y$_2$O$_3$), Lanthanum oxide (La$_2$O$_3$), Silicon dioxide (SiO$_2$) and Silicon Nitride (Si$_3$N$_4$) [6-15]. Now the issue is that the material properties including relative dielectric constant ($\varepsilon_r$), energy band gap ($E_g$), conduction band offset (CBO) and coefficient of thermal expansion (CTE) affects the choice of dielectric material to be used. The analysis for the selection of the best gate dielectric materials can be done analytically and also by simulation. In our recent work [16, 17], it was found analytically that La$_2$O$_3$ and HfO$_2$ are the best gate dielectrics for CNFET. Analytical study was done using three material selection methodologies; Ashby’s Approach, TOPSIS method and VIKOR analysis [18]. According to Ashby’s approach, the best gate dielectric is La$_2$O$_3$. Table 1 shows the ranking of gate dielectrics obtained using TOPSIS and VIKOR analytical approaches. However, before going for fabrication of device it is important to develop the device in virtual environment. Therefore, simulation study helps in comparing the simulated results with analytical work reported earlier.

The performance of CNFET depends on the geometry of device (i.e. planar or gate-all-around structure) and the thickness of gate dielectric. Fabricated results for the planar structure [19-23] and gate-all-around (GAA) structure [24, 25] show that the performance of CNFET is affected by the various thickness of gate dielectric material [26, 27]. In planar structure, the performance of device is affected by fringing effect while the GAA structure is expected to be ideal geometry that maximizes the electrostatic gate control in FETs [28, 29]. The paper is organized as follows: Section 2 describes the design of CNFET.
and input parameters. Section 3 provides the simulation results for the selection of the best gate dielectric with the suitable thickness of dielectric and observations. The concluding remarks are given in Section 4.

Table 1. Ranking of gate dielectrics using analytical approach [16]

| Dielectric materials | TOPSIS | VIKOR |
|----------------------|--------|-------|
| SiO₂                 | 7      | 7     |
| Al₂O₃                | 5      | 3     |
| HfSiO₄               | 6      | 6     |
| ZrO₂                 | 3      | 4     |
| La₂O₃                | 1      | 1     |
| Y₂O₃                 | 4      | 5     |
| HfO₂                 | 2      | 2     |
| Si₃N₄                | 8      | 8     |

2. DEVICE STRUCTURE AND SIMULATION

In this work, we have simulated the cylindrical CNFET with different gate dielectric materials as shown in Table 2 and also studied the effect of thickness of dielectric layer (i.e. 3nm, 5nm, 7nm, 8nm, 10nm and 20nm) on the drain current (I_d). The schematic view of CNFET is shown in Figure 3. The electronic transport mechanism in the CNFET is ballistic. The diameter and energy band gap have been simulated by using QuantumWise Atomistic Tool Kit (ATK) software. The diameter and energy band gap of (19, 0) CNT comes out to be 1.490nm and 0.441079eV, as shown in Figures 4 and 5. Table 3 shows the input parameters of CNFET for the simulation.

Table 2. Relative dielectric permittivity of various high-k dielectric materials

| S. No. | Dielectric materials | Relative dielectric constant (ε_r) |
|--------|----------------------|----------------------------------|
| 1      | SiO₂                 | 3.9                              |
| 2      | Al₂O₃                | 9                                |
| 3      | HfSiO₄               | 11                               |
| 4      | ZrO₂                 | 25                               |
| 5      | La₂O₃                | 30                               |
| 6      | Y₂O₃                 | 15                               |
| 7      | HfO₂                 | 25                               |
| 8      | Si₃N₄                | 7                                |

Figure 3. Schematic view of carbon nanotube field effect transistor using nano-hub [30]

Figure 4. Diameter of (19, 0) CNT

Figure 5. Energy bandstructure for (19, 0) CNT
Table 3. Input parameters for the simulation of CNFET

| Input Parameters                      | Values           | Input Parameters                      | Values           |
|--------------------------------------|------------------|--------------------------------------|------------------|
| Gate dielectric thickness            | 3 nm             | Final drain voltage                  | 1 eV             |
| Insulator dielectric material       | La$_2$O$_3$($\varepsilon_r$=30) | Number of bias points (drain)        | 11               |
| temperature                          | 300 K            | Threshold voltage                    | 0.32             |
| Final gate value                     | 0 eV             | Gate control parameter               | 0.88             |
| Number of bias points (gate)         | 0.3eV            | Drain control parameter              | 0.035            |
| Initial drain voltage                | 3V               | Series resistance                    | 0 (ohms)         |
|                                      |                  | NT Diameter                          | 1.49 nm          |

3. RESULTS AND DISCUSSION

In order to get the best gate dielectric material for CNFET, transfer characteristics and output characteristics have been analyzed for different gate dielectric materials. Figure 6 shows the transfer characteristics of CNFET for different high-k gate dielectric materials. In this plot SiO$_2$ is also considered for the comparison purpose. The value of drain to source voltage ($V_{ds}$) is assumed as 0.3V. It has been observed from the plot that corresponding to each gate voltage ($V_{gs}$), La$_2$O$_3$ gives the highest value of drain current, followed by HfO$_2$ and ZrO$_2$. However, at low values of gate voltage this difference is negligible. The subthreshold swing and current on/off ratio for La$_2$O$_3$ are 65.41mV/dec and 1.8089x 10$^6$, respectively. The high current on/off ratio shows the figure of merit for having low leakage power and high performance for CNFET.

Figure 7 shows the output characteristics of CNFET for different high-k gate dielectrics materials. In this plot, the value of gate to source voltage ($V_{gs}$) is assumed as 0.3V. It has been observed from the plot that corresponding to each drain voltage ($V_{ds}$), drain current ($I_d$) increases with increase in relative dielectric constant ($\varepsilon_r$). It has been shown that La$_2$O$_3$ ($\varepsilon_r$=30) has the highest output drain current ($I_d$=1.19 µ Amp) followed by HfO$_2$ and ZrO$_2$ among all the possible gate dielectric materials.

![Figure 6. Transfer characteristics of CNFET with different gate dielectric](image)

![Figure 7. Output characteristics of CNFET with different gate dielectric](image)

Table 4 shows the output drain current ($I_d$) for different gate dielectric materials. In CNFET, the analysis of transfer characteristics and output characteristics with different high-k gate dielectric materials show that La$_2$O$_3$ is the best gate dielectric material among all possible gate dielectrics which is followed by HfO$_2$ and ZrO$_2$. The effect of thickness of gate dielectric layer in CNFET also studied with the best gate dielectric materials i.e. La$_2$O$_3$ and HfO$_2$. Table 5 contains the output results of the simulated device which has both La$_2$O$_3$ and HfO$_2$ results with the variation of the thickness of dielectric layer.

Table 4. Drain current in CNFET with the possible gate dielectrics

| S.No. | Dielectric Materials | Drain Current ($I_d$) (µ Amp.) |
|-------|----------------------|--------------------------------|
| 1     | SiO$_2$              | 0.605                          |
| 2     | Al$_2$O$_3$          | 0.865                          |
| 3     | HfSO$_4$             | 0.927                          |
| 4     | ZrO$_2$              | 1.15                           |
| 5     | La$_2$O$_3$          | 1.19                           |
| 6     | Y$_2$O$_3$           | 1.02                           |
| 7     | HfO$_2$              | 1.15                           |
| 8     | Si$_3$N$_4$          | 0.785                          |
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Table 5. Output drain current for CNFET with the two best dielectrics (i.e. La$_2$O$_3$ and HfO$_2$) by various thickness of gate dielectrics

| S.No. | $T_{ox}$ (nm) | $I_D$ ($\mu$Amp) for La$_2$O$_3$ | $I_D$ ($\mu$Amp) for HfO$_2$ |
|-------|---------------|----------------------------------|------------------------------|
| 1     | 3             | 1.27                             | 1.24                         |
| 2     | 5             | 1.23                             | 1.19                         |
| 3     | 7             | 1.2                              | 1.16                         |
| 4     | 8             | 1.19                             | 1.15                         |
| 5     | 10            | 1.17                             | 1.13                         |
| 6     | 20            | 1.12                             | 1.08                         |

The variation of $I_D$ with respect to $V_{gs}$ for various gate dielectric thickness ($T_{ox}$) (i.e. 3nm, 5nm, 7nm, 8nm, 10nm, 20nm) with gate dielectric material La$_2$O$_3$ and HfO$_2$ is shown in Figure 8 and Figure 9, respectively. It has been observed from the plots that the current on/off ratio increases with decreases the thickness of gate dielectric material. It has been shown that the highest on current ($I_{on}$) of CNFET with La$_2$O$_3$ and HfO$_2$ are 46.54 $\mu$Amp and 46.52 $\mu$Amp for the thickness of gate dielectric material of 3nm.

The variation of $I_D$ with respect to $V_{ds}$ for various gate dielectric thickness with gate dielectric material La$_2$O$_3$ and HfO$_2$ at $V_{gs}$ of 0.3V is shown in Figure 10 and Figure 11, respectively. It has been observed from the plots that the drain current of CNFET increases very marginally with decreases the thickness of gate dielectric layer. This shows that the resistivity of CNFET is proportional to the thickness of gate dielectric material. It has been shown that $I_D$ is the highest for the thickness of gate dielectric material of 3nm.
4. CONCLUSION

CNFET with various high-k gate dielectrics has been investigated. The analysis was done using simulations and results show that $\text{La}_2\text{O}_3$ shows the best result followed by $\text{HIO}_2$ as compared to other possible materials. Therefore, it is expected that using $\text{La}_2\text{O}_3$ as gate material into CNFET may be useful for producing high performance FETs. For the thickness of gate dielectric, the results show that as the thickness of dielectric decrease from 20 nm to 3 nm, output current and current on/off ratio increase which shows the low leakage current and better gate control in CNFET.

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