DANCE: Differentiable Accelerator/Network Co-Exploration

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Abstract

To cope with the ever-increasing computational demand of the DNN execution, recent neural architecture search (NAS) algorithms consider hardware cost metrics into account, such as GPU latency. To further pursue a fast, efficient execution, DNN-specialized hardware accelerators are being designed for multiple purposes, which far-exceeds the efficiency of the GPUs. However, those hardware-related metrics have been proven to exhibit non-linear relationships with the network architectures. Therefore it became a chicken-and-egg problem to optimize the network against the accelerator, or to optimize the accelerator against the network. In such circumstances, this work presents DANCE, a differentiable approach towards the co-exploration of the hardware accelerator and network architecture design. At the heart of DANCE is a differentiable evaluator network. By modeling the hardware evaluation software with a neural network, the relation between the accelerator architecture and the hardware metrics becomes differentiable, allowing the search to be performed with backpropagation. Compared to the naive existing approaches, our method performs co-exploration in a significantly shorter time, while achieving superior accuracy and hardware cost metrics.

1 Introduction

After decades of efforts from the researchers, DNNs now exhibit near- or over-human performance in various applications, such as image classification (Geirhos et al. 2017), playing board games (Silver et al. 2017), or driving fighter planes (Hambling 2020). However, the success comes at the cost of exploding compute intensity. The model size of DNNs is increasing at a rapid rate, and the same trend can be witnessed from number of required operations. In addition to the increased GPU hours for training such large models, one important issue is the related HW cost. For example, inference latency is already being perceived as an important factor in designing network architectures (Sandler et al. 2018), Howard et al. 2019, Iandola et al. 2016) to run on mobile devices or to meet real-time requirements.

Neural Architecture Search (NAS) is an approach that tries to solve such problems. Designing a network has traditionally been a hard task that requires a lot of human effort (He et al. 2016, Huang et al. 2017), and it becomes even harder with latency in consideration (Howard et al. 2017). To mitigate such issues, NAS automatically searches for network architecture, using evolutionary algorithms (Dai et al. 2019, Guo et al. 2019, Real et al. 2019), reinforcement learning (Tan et al. 2019, Tan and Le 2019, Howard et al. 2019, Pham et al. 2018), or backpropagation (Liu, Simonyan, and Yang 2018, Cai, Zhu, and Han 2018, Chen et al. 2019, Xu et al. 2019). Recent NAS algorithms also consider the latency of the network in many ways such as considering Flops penalty (Cai, Zhu, and Han 2018) or modeling latency as a ML model (Xu et al. 2020).

Another popular way to tackle the latency is through specialized hardwares (Often called `accelerator’s). In the remainder of this paper, we use words ‘hardware’ and ‘accelerator’ interchangeably. By utilizing an accelerator specialized for executing DNNs, it’s been shown that they could achieve superior latency and cost compared to widely-used CPUs or GPUs available on the market (Chen et al. 2014, 2016, Jouppi et al. 2017). For example, Google TPU (Jouppi et al. 2017) has been deployed to accelerate the processing of AlphaGo (Silver et al. 2017), datacenters and cloud services.

Designing dedicated accelerators opens up another large design space for optimizing not only the latency, but also other hardware cost metrics such as energy consumption and area. For example, one could attempt to increase the speed of the accelerator by naively placing more memory and computing resources into the accelerator, only to result in a design that has unrealistically large area and high energy consumption. The increase in the design area exponentially increases the price of the product, and considered as an important cost for HW accelerators. Also, high energy consumption would increase the device temperature and drain the battery which is ever more important for mobile devices. Therefore, it is necessary to efficiently design the accelerator for balancing between the cost metrics.

However, the network architectures and the accelerator are not independent, and blindly optimizing one side could often hurt another. For example, the commonly used separable convolution (Sandler et al. 2018, Tan and Le 2019) usually achieves superior latency due to its low computational requirements. However, some type of accelerators such as google’s TPU are designed to run faster when the number of channels on the network is large. Because of this, a separa-
ble convolution executed on TPU suffers from long latency compared to normal convolution operations despite the less number of computations (Gupta and Akin 2020). Similarly, optimizing only the network oblivious of the target accelerator or optimizing the accelerator without considering the network would often yield suboptimal solutions.

In such regard, co-exploration of both the hardware accelerator and network architectures (Jiang et al. 2020b,a; Hao et al. 2019; Lu et al. 2019; Yang et al. 2020; Abdelfattah et al. 2020) is critical in achieving the desired application performance (i.e., accuracy) and a reasonable cost (latency, area, and energy consumption). Existing co-exploration techniques typically achieve the goal using RL-based techniques. First, the network architecture and accelerator design are generated. The generated designs are evaluated by training the network for accuracy and the hardware cost metrics. Obtaining the cost metrics is often performed by accelerator evaluation software, which helps analyze the accelerator before producing the real hardware by simulating the behavior of the hardware in a low-level (Samajdar et al. 2018) or by relying on simplified analysis models (Parashar et al. 2019; Kwon et al. 2019; Wu, Emer, and Sze 2019). After the evaluation, a reward function is calculated and a new network architecture and accelerator design are generated based on the reward. The obvious problem of this procedure is that it requires a huge search time. As in other RL-based NAS techniques, the generated network needs to be fully trained in order to evaluate the accuracy. Also, the accelerator evaluation often takes non-negligible time and resources to complete. Hence, the search either demands excessive amount of time, or terminates with premature solutions (Jiang et al. 2020b; Abdelfattah et al. 2020).

This work presents DANCE (Differentiable Accelerator/Network Co-Exploration), which hugely reduces the search cost by adopting the idea of differentiable neural architecture search (Liu, Simonyan, and Yang 2018) into the co-exploration problem. Differentiable NAS reduces the search cost of the NAS problem by modeling the network architecture space as a continuous hyperspace. However, the search cannot be directly applied to accelerator/network co-exploration, as the relation between the accelerator design and the hardware metrics is complicated (Parashar et al. 2019; Kwon et al. 2019). Moreover, the design parameters of the hardware accelerators are discrete, and renders the relation non-differentiable.

At the heart of DANCE is the modeling of the accelerator evaluation software (which is non-differentiable) using a neural network. Since a neural network is differentiable, it can be used as a differentiable loss function and be enclosed within the frameworks of differentiable NAS. Using the evaluator network, we propose a method for exploring the neural architecture and accelerator designs.

DANCE can be applied to any differentiable NAS framework, using any evaluation software such as simulators (Samajdar et al. 2018) or schedulers (Parashar et al. 2019; Kwon et al. 2019). We demonstrate that DANCE can efficiently explore the search space within a short amount of time, and finds good design points among accuracy, latency, energy efficiency and area. Our contribution can be summarized as the following:

- We propose a differentiable co-exploration method for accelerators and network architectures to achieve fast search time and application performance at the same time. To the best of our knowledge, this is the first work that performs a differentiable approach to the problem.
- We provide a cost estimation network architecture for modeling the accelerator evaluation software which is differentiable and fast, but still provides a high accuracy.
- We provide a hardware generation network architecture that searches for the optimal accelerator design given a network design under search.
- We present a framework which puts the cost estimation network and the hardware generation network into differentiable NAS framework so that a high quality co-exploration can be done within a short amount of time.

2 Related Work

2.1 Neural Architecture Search

In reaction to cope with the increasing network size and the corresponding manual design effort, neural architecture search automates the design of DNN architectures. Early works usually adopted RL or EA to generate the network. (Tan et al. 2019; Tan and Le 2019; Howard et al. 2019; Pham et al. 2018) use RL and (Dai et al. 2019; Guo et al. 2019; Real et al. 2019) use EA as the main method to generate the new candidate networks.

However, the search cost required for those algorithms often becomes the drawback, ranging from hundreds to thousands of GPU-days. To perform a search, RL- or EA-based search algorithm requires evaluating many candidates, and evaluating each of them requires a full training of the network. Differentiable neural architecture search (Liu, Simonyan, and Yang 2018) is a way to mitigate such cost, which builds a supergraph and finds a path within it. It was able to find state-of-the-art performing networks within a few orders of magnitude shorter time, and many other works followed (Xu et al. 2019; Chen et al. 2019).

Recent works started employing hardware penalties to reduce latencies of the searched network architecture. SNAS (Xie et al. 2018) uses Flops, memory access and parameter size as regularizers to constrain the resource usage of the network. ProxylessNAS (Cai, Zhu, and Han 2018) and FBNet (Wu et al. 2019) add latency constraints accessible with lookup tables. LA-DARTs (Xu et al. 2020) and AOWS (Berman et al. 2020) adopt ML-based modeling for the network latency as the loss function to consider the latency in a further granularity. Finally, OFA (Cai et al. 2019) is a work worth mentioning, that searches a supernetwork that can be later cropped to adapt towards various cost requirements.

2.2 Hardware DNN Accelerators

Hardware accelerators for DNNs are often focused on executing many floating-point multiply operations (Flops) in parallel, as it is the most common operation in modern CNNs. For example, Google TPU (Jouppi et al. 2017) was
Figure 1: CNN execution dimensions and an example DNN accelerator. (a) and (b) shows the seven dimensions in a convolutional layer and its execution, and (c) shows an example DNN accelerator with multiple PEs (Processing Elements).

able to achieve $30 \times$ performance and $80 \times$ energy efficiency on DNNs than GPUs, and is deployed in datacenters and the cloud services. Also, (Nvidia 2018) is an open-source DNN accelerator that provides high performance for inference.

Figure 1c shows an example DNN accelerator. It comprises on-chip memory, many PEs (processing elements), and the interconnects between them. Even with a predetermined backbone accelerator design, many properties still remain as tunable parameters, in trade-off with metrics such as the execution latency, energy consumption, and the area. For example, as there are more PEs in an accelerator, the latency for executing a DNN will get shorter, but the energy consumption and the area will increase proportionally to the number of PEs. In each PE, there is a RF (register file) and a floating point arithmetic (multiply, add) unit. The RF acts as a fast, local memory to the PE. Therefore increasing the RF size also helps reduce latency but increases the energy/area.

Usually, a DNN layer includes multiple dimensions of computation. For example, a convolution layer has seven layers of computations as shown in Figure 1a three for input activations ($H, W, C$), three for weights ($R, S, K$), and one for batches ($N$). Thus, it is formulated as a seven-level nested loop (Figure 1b) and executing a DNN layer on an accelerator requires mapping and ordering those loops on the accelerator. This is often called the dataflow. Many accelerators (Chen et al. 2016; Du et al. 2015; Parashar et al. 2017) provide different dataflows that focus on keeping some of the weight parameters, input activation, or output activations in the local memory as long as possible.

To analyze how each choice in the accelerator design affects the DNN latency, some evaluation software frameworks are proposed. ScaleSim (Samajdar et al. 2018) is a simulator that divides the DNN execution into multiple phases, and counts how much time is required on each phase for a given accelerator configuration. Recently, some analytical evaluation tools were proposed (Parashar et al. 2019; Kwon et al. 2019). By composing a few mathematical models, they provide easier and faster latency and accelerator cost modeling than simulators. In this work, we utilize Timeloop (Parashar et al. 2019) combined with Accelergy (Wu, Emer, and Sze 2019), a state-of-the-art accelerator evaluation software, and train the evaluation network that is integrated into the DANCE algorithm.

### 2.3 Accelerator/Network Co-exploration

There are a few existing works on co-exploring the network architecture and accelerator design. To the best of our knowledge, all prior work on co-exploration utilize RL as their controller due to its relatively simpler way of formulating the problem. (Jiang et al. 2020b; Abdelfattah et al. 2020) propose such RL-based algorithms for co-exploring the accelerators and network architectures. (Yang et al. 2020) solves a similar problem for multi-task networks, and (Lu et al. 2019) optimizes for edge devices. However, they all inherit the same search-cost problem from the RL-based NAS algorithms. (Jiang et al. 2020a) proposed starting from a pre-trained network model and accelerator design, but it fails to explore a large design space. In contrast, this paper proposes adopting the idea of differentiable NAS on the co-exploration problem to significantly reduce the search cost, while still producing the state-of-the-art accuracy network and accelerator design.

### 3 Differentiable Accelerator/Network Co-Exploration

#### 3.1 Existing RL-Based Co-explorations

Figure 2 shows how RL-based co-explorations are performed. The black letters represent the components for ordinary NAS algorithms, and the blue letters represent components added for the co-exploration. First, the search space on the network architecture and hardware accelerator is provided to the controller. Then the controller generates candidate designs for the provided space (network and accelerator). The generated candidates are sent to the evaluator, which performs training on the network to get its accuracy,
and analyzes the cost metrics for the given hardware running the network. While it well-serves the purpose of co-exploration, it shares the same problem of RL-based NAS algorithms: the training cost. A costly training is required for each candidate being generated. Moreover, searching for the optimal hardware design also takes considerable time which is also performed for each candidate. As a result, the search suffers from exploding GPU-hours.

3.2 Proposed Differentiable Co-exploration

Figure 3 illustrates the proposed differentiable co-exploration method, named DANCE. The left part is the network search module similar to other differentiable NAS algorithms, where a path within the super-network is found using backpropagation to become the final searched network. On the right-hand side of Figure 3 is the differentiable evaluator, which takes the architecture parameters from the search module, searches for the optimal hardware accelerator design, and evaluates its cost metrics. It is a pre-trained neural network, which is frozen during search and used only to connect the architecture to the hardware cost metrics. The loss function considers both the accuracy and the cost metrics as below:

\[
\text{Loss} = \text{Loss}_{CE} + \lambda_1 \|w\| + \lambda_2 \text{Cost}_{HW}
\]  

(1)

Where \(\lambda_1\) and \(\lambda_2\) are hyperparameters that control the trade-off between the terms, \(\text{Loss}_{CE}\) is the cross-entropy loss, and \(\|w\|\) is the weight decay term following (Cai, Zhu, and Han 2018). Finally, \(\text{Cost}_{HW}\) is the cost function for hardware accelerators, calculated from the output values of the evaluator network. For example, it can be a linear combination of latency, area, and the energy consumption. We discuss various possible hardware cost functions in Section 3.5.

3.3 Evaluator Network

The original (non-differentiable) cost evaluation softwares are comprised of two different pieces of software: a hardware generation tool and a cost estimation tool. As briefly explained in Section 2.2, the hardware generation tool takes the network architecture as the input, and proposes a hardware accelerator design. In this paper, we choose the loop order (i.e. dataflow), number of processing units, and size of the register file as the search space of the hardware accelerator design (Refer to Section 3.5 for more details). Then, the cost estimation tool takes the hardware accelerator and network design to output the cost metrics. In general, the hardware generation tool is composed as an outer loop enclosing the cost estimation tool. By using exact algorithms such as exhaustive search or branch-and-bound algorithms, it outputs the optimal solution for the given network architecture, within the hardware search space \(\mathcal{H}\). In this work, we use Timeloop (Parashar et al. 2019) for latency and Accelergy (Wu, Emer, and Sze 2019) for energy/area, which is regarded as a state-of-the-art cost estimation toolchain. On top of those, we design our own hardware generation tool based on exhaustive search algorithm. We generate random networks within the network architecture space \(\mathcal{A}\) as inputs, and the output of the toolchain will become ground-truth for training the components for evaluator network.

Our design of the evaluator network is composed of two modules: Hardware generation network and cost estimation network. Figure 4 shows the evaluator network architecture. The hardware generation network models the exhaustive search algorithm as a classification problem. We model it with a five-layer perceptron, which uses ReLU as activation functions. To increase the accuracy of the cost estimation network and establish the gradient path towards the network under search, we adopt residual connections between the layers (He et al. 2016).

For the cost estimation, we model the network as a five-layer regression network with residual connections. It has ReLU as activation functions, and applies batch normalization every layer. It outputs the three cost metrics of our interest (latency, area, and energy consumption), based on the ground truth generated from the evaluation software (Timeloop + Accelergy) described above. We use MSRE (Mean Squared Relative Error) loss for training each evaluator network, which can be represented as the following:

\[
\text{Loss}_{MSRE} = \sum_i (\hat{y}_i/y_i)^2
\]  

(2)

where \(y_i\) is the hardware cost function (\(\text{Cost}_{HW}\)) for each metric generated from result of Timeloop+Accelergy and \(\hat{y}_i\) is the same cost function calculated using the network output. While we could use typical MSE loss, it has a prob-
lem of falsely heavy-weighing the metrics that have the high values. For example, the latency values outputted within our search space ranges from 8ns to over 100ns per each layer. If we use MSE loss, we regard the 10ns error out of 8ns cycles and 10ns error out of 100ns cycles as the same, giving unfair favor towards modeling the long-cycle situations more correct. Since our objective is to find accelerators with low latency, such behavior is undesirable.

In the evaluator architecture, the cost estimation network having to output the HW cost metrics means that it has to internally model two functions: Find the optimal hardware, and estimate the metrics. While the standalone network shows fairly high accuracy (Section 4), we can further improve the latency by adding a feature forwarding path from the output of the hardware generation network. We concatenate the result of the hardware generation network to the network architecture, and feed it to the cost estimation network. One problem is that the input of the cost estimation network is supposed to be discrete (e.g., number of multipliers in the hardware cannot be a fractional number), while the output of the hardware generation network is not. To mitigate the problem, we use Gumbel softmax (Jang, Gu, and Poole 2017) as the last layer of the hardware generation network, so that the intermediate value becomes as close as possible to the training values for the cost estimation network.

3.4 Hyperparameter Warm-up

Compared to optimizing for the application’s classification accuracy, optimizing for the cost metrics are relatively easier for the NAS algorithm. For instance, selecting most of the operations to be zero quickly optimizes all of the latency, area, and the energy consumption. Once the architecture falls into such a solution it is difficult to find heavier architectures even if those are needed for optimizing the best accuracy. To mitigate such effect, we use hyperparameter warm-up scheduling. We use small $\lambda_2$ from Eq. 1 for the first few epochs, and increase the $\lambda_2$ to the desired value later, after the network architecture reaches a certain stage for high accuracy.

3.5 Hardware Cost Functions

By default, we use a linear combination of the three hardware cost metrics as the cost function $Cost_{HW}$ of Eq. 1 as below:

$$Cost_{HW, linear} = \lambda_E Energy + \lambda_L Latency + \lambda_A Area$$  \hspace{1cm} (3)

By controlling $\lambda_E$, $\lambda_L$, and $\lambda_A$, we can set a constraint on how we weigh the balance between each cost metric. In addition, we use the product of all metrics,

$$Cost_{HW, EDAP} = Energy \cdot Latency \cdot Area$$  \hspace{1cm} (4)

where EDAP is a common metric used to evaluate hardwares (i.e. energy-delay-area product (Li et al. 2009)). It has the benefit of having no extra hyperparameter and is unitless. Refer to Section 4 for how setting those cost functions affect the searched solutions.

| Network                  | Objective | Accuracy |
|--------------------------|-----------|----------|
| Hardware Generation      | $PE_X$    | 98.9%    |
|                          | $PE_Y$    | 98.3%    |
|                          | RF_Size   | 98.3%    |
|                          | Dataflow  | 98.8%    |
| Cost Estimation (w/o feature forwarding) | Latency | 93.7%    |
|                          | Energy    | 96.3%    |
|                          | Area      | 92.8%    |
| Cost Estimation (w/ feature forwarding) | Latency | 99.6%    |
|                          | Energy    | 99.7%    |
|                          | Area      | 99.9%    |
| Overall Evaluator       | Latency   | 98.3%    |
|                          | Energy    | 98.3%    |
|                          | Area      | 99.2%    |

Table 1: Performance of the Evaluator Network

4 Experimental Results

We have conducted several experiments on DANCE using CIFAR-10 and ImageNet (ILSVRC2012) dataset. In this section, we first describe the results of the evaluator network, and then the co-exploration solution quality in comparison with the NAS works and existing RL-based co-exploration works. All algorithms are implemented on PyTorch (Paszke et al. 2017) and run on four RTX2080Ti GPUs.

4.1 Search Space

For $H$, the hardware accelerator search space, we use a state-of-the-art accelerator named Eyeriss (Chen et al. 2016) as the backbone. We choose number of PEs (Processing Elements), RF (Register File) size, and Dataflow (loop ordering) as the design parameters. Since the PEs are placed in a two-dimensional topology, we separately assign a variable per dimension: $PE_X$ and $PE_Y$, where each value can range from 8 to 24. In our settings, larger $PE_X$ favors the layers with more channels, and larger $PE_Y$ favors larger feature maps for parallelism. The RF size per PE could take values between 4 and 64. For Dataflow, we choose three dataflows from existing hardware accelerators: WS (Weight Stationary (Jouppi et al. 2017)), OS (Output Stationary (Du et al. 2015)), and RS (Row Stationary (Chen et al. 2016)). Within the evaluator network, each variable is formulated as one-hot vectors to simplify the cascaded connection between the hardware generation and the cost estimation networks.

For the network architecture search space $A$, we have adopted ProxylessNAS (Cai, Zhu, and Han 2018) as the backbone network architecture. The network has 13 layers, where the number of channels increase every 3 layers. Each of the 9 layers placed in the middle has 7 candidate operations in addition to a skip connection: MBConv3X3_expand3, MBConv3X3_expand6, MBConv5X5_expand3, MBConv5X5_expand6, MBConv7X7_expand3, MBConv7X7_expand6, and Zero. When Zero is chosen, only the skip connection remains and the layer effectively disappears from the network. The architecture parameters are trained using the binarized method (Courbariaux, Bengio, and David 2015).
Table 2: Performance of DANCE on CIFAR-10

| $HW_{Cost}$ | Cost Hyperparam. | Method | Acc. (\%) | Latency (ms) | Energy (mJ) | EDAP ($J \cdot sec \cdot m^2 \cdot 10^{-12}$) |
|-------------|------------------|--------|------------|--------------|-------------|------------------------------------------|
|             | $\lambda_L$ $\lambda_E$ $\lambda_A$ | Baseline (No penalty) + HW† | 94.5 13.5 5.0 | 133.1        |
|             |                  | Baseline (Flops penalty) + HW | 94.1 10.9 2.8 | 79.4         |
|             |                  | DANCE (w/o FF*) | 93.1 3.1 11.8 | 94.8         |
|             |                  | DANCE (w FF)-A | 94.4 2.8 10.2 | 74.0         |
|             |                  | DANCE (w FF)-B | 93.5 1.5 5.1 | 19.7         |
| $Cost_{HW, EDAP}$ | N/A N/A N/A | Baseline (No penalty) + HW | 94.5 3.7 13.5 | 162.2        |
|             |                  | Baseline (Flops penalty) + HW | 94.1 10.9 2.8 | 79.4         |
|             |                  | DANCE (w/o FF) | 93.4 3.0 3.7 | 21.8         |
|             |                  | DANCE (w FF)-A | 94.3 1.1 3.2 | 15.7         |
|             |                  | DANCE (w FF)-B | 93.4 1.0 3.9 | 13.2         |

| $Cost_{HW, linear}$ | 4.1 4.8 1.0 | Baseline (No penalty) + HW | 94.5 3.7 13.5 | 162.2        |
|                     |            | Baseline (Flops penalty) + HW | 94.1 10.9 2.8 | 79.4         |
|                     |            | DANCE (w/o FF) | 93.4 3.0 3.7 | 21.8         |
|                     |            | DANCE (w FF)-A | 94.3 1.1 3.2 | 15.7         |
|                     |            | DANCE (w FF)-B | 93.4 1.0 3.9 | 13.2         |

†HW: Hardware accelerator, designed using the hardware generation tool after the NAS. *FF: Feature Forwarding.

4.2 Evaluator Network Results

Cost Estimation Network Table 1 shows the experimental results for the components of the evaluator network. We separately train the cost estimation and the hardware generation network on the ground truth values and combine them.

Each layer of the cost estimation network has width of 256. The network is trained using Adam optimizer with learning rate of 0.0001 for 200 epochs. We have used batch size of 256. We have trained the cost estimation network on 1.8 million cases generated with Timeloop+Accelergy from the search space, and validated on 0.45 million cases. All three cost metrics show over 99% accuracy, showing that it is precise enough. Also, it is observed that feature forwarding improves the accuracy by 4.3% on average, allowing the cost estimation network to reach high enough accuracy for the co-exploration.

Hardware Generation Network For the hardware generation network, the layer widths are set to be 128. We use normal CE loss as the loss function of the hardware generation network, which we denote as $Loss_{CE, HW}$. The network has been trained using SGD with batchsize 128 for 200 epochs, where the learning rate starts with 0.001 and decreases by 0.1 every 50 epochs. We have generated 50K network cases from the search space explained in the previous section, and used 10K cases for validation. The ground truth was found by exhaustive search. On all of the hardware accelerator design parameters, the accuracy was nearly 99%, also showing that it is accurate enough. It is worth noting that not only the hardware generation network is accurate and differentiable, but it is also much faster than the original exhaustive search method. With the same functionality, the inference time for the hardware generation network takes about 0.5ms with a single GPU, while the exhaustive search takes about 112s using 48 threads from 24 cores of two Intel Xeon Silver-4214 CPUs.

End-to-end Evaluator Network Results Finally, we test the whole evaluator network as a combination of hardware generation and cost estimation network. Even though the intermediate values are not one-hot vectors, Gumbel softmax approximates them as the max function, and still maintains around 99% accuracy for the cost metrics.

4.3 Co-exploration Results

Experimental Results on CIFAR-10 Table 2 shows the performance of DANCE on CIFAR-10 dataset. For the baseline, we have performed search using ProxylessNAS (Cai, Zhu, and Han 2018) (w/ or w/o Flops penalty term), and conducted hardware generation on the searched network using the exhaustive-search tool in Section 3.3. It represents the typical separate design performed in practice. Following (Cai, Zhu, and Han 2018), the search was performed for 120 epochs with batch size of 256. SGD optimizer with Nesterov momentum was used for the search using cosine scheduling with learning rate of 0.025, weight decay 0.00004, label smoothing 0.1 and momentum 0.9. After the search, the final network was trained from scratch for 200 epochs. The hyperparameters for training are the same, except that the learning rate is 0.0125 and the weight decay factor is 0.001.

Using DANCE, we have performed co-exploration with the cost functions described in Section 3.5. All the hyperparameters were the same as the baseline. Similar to after-search training, a one-time exact hardware generation was performed after the search to obtain the optimal hardware accelerator design.

Overall, DANCE was able to obtain network-accelerator design superior to the baseline. For DANCE, we report two designs, one with high accuracy (-A) and the other towards efficient hardware design (-B). For the high accuracy design (-A), DANCE achieves almost the same accuracy of the baseline network architecture that was searched with-
DANCE achieves up to function within at most 1% accuracy drop. It shows that for the efficient hardware design (-B), we chose the design which shows the best cost line (w/ or w/o Flops penalty). For the efficient hardware tors, DANCE yields much better cost metrics than the base-

out any hardware cost penalty on the loss function. On the other hand, with the associated optimal hardware accelerators, DANCE yields much better cost metrics than the baseline (w/ or w/o Flops penalty). For the efficient hardware design (-B), we chose the design which shows the best cost function within at most 1% accuracy drop. It shows that DANCE achieves up to 4× better EDAP, or almost 4× better latency by performing an efficient co-exploration.

Some readers might become curious whether the results are just artifacts of tuning the hyperparameter \( \lambda_2 \) from Eq. 1. To address such concern, we show in Figure 5 that DANCE achieves dominating solutions compared to the baseline, not merely trading off accuracy with the hardware cost. The figure plots the EDAP-error relations of the designs found from the baseline and DANCE. In both of the axes, lower is better. In addition to the data points reported in Table 2, we have searched for with varying \( \lambda_2 \) from Eq. 1 to achieve different balance between accuracy and the Cost_{HW}. As shown in the plot, the baselines+HW do not optimize the cost metric well, even with the Flops penalty term. The baseline and DANCE are both able to reach similar accuracies with accuracy-oriented hyperparameter settings, but in those cases DANCE always exhibits significantly lower hardware cost metric. When the hyperparameters are tuned more towards the cost metric, DANCE shows a much better trade-off, and is able to gain superior cost metric than the baseline with Flops penalty.

Experimental Results on ImageNet Table 4 shows the performance of DANCE on ImageNet dataset. The baseline with the separate hardware search yields 70.6% accuracy but suffers from latency cost of 10.3ms, 43.0mJ energy consumption and EDAP of 1212.6. As in the case of experiments of Table 2, DANCE discovers a good tradeoff point, and results with significantly better cost metrics, with 8.1ms latency, 36.3mJ energy and EDAP of 808.3, while showing only a small accuracy drop.

4.4 Comparison of DANCE with Existing Co-exploration Algorithms

Table 3 compares DANCE with other accelerator/network co-exploration algorithms. Since the hardware environments are all different, direct comparison of the hardware cost metrics are not possible. Thus, we only report the achieved accuracy and the search cost from the published literature. All of the co-exploration algorithms utilize reinforcement learning except for (Hao et al. 2019) which still adopts a similar structure. Therefore they all suffer from having to train many candidates for evaluation during search. As a result, many of them only output sub-optimal network architectures with inferior accuracy compared to DANCE.

The search time also shows the advantage of DANCE. Compared to those where GPU-hours for search was available, DANCE is an order of magnitude faster. (Yang et al. 2020) shows a small difference, but this is due to the fact that its backbone architecture is based on a manually fine-tuned architecture (Hao 2019) where the model size is significantly small compared to other backbone architectures. The #candidates’ column is an attempt to provide a fair comparison of the search costs for considering such cases. It reports the number of candidates each algorithm has to train while searching for a solution. Each number is either directly reported in the original literature, or our best estimates based on available information. RL-based co-exploration algorithms require around hundreds to thousands of candidates to be trained, while DANCE requires only one, as it is based on backpropagation. Thus, when performed on an equal search space, one can envision that DANCE would be significantly faster than the others.

5 Conclusion

In this paper, we propose a novel differentiable method of co-exploring hardware accelerator and network architecture together targeting both high accuracy and low cost metrics. We adopt differentiable NAS algorithms into the co-exploration problem, to obtain efficient hardware design without compromising the accuracy at an extremely low search cost. We believe this work would bring much cost reduction to the co-exploration problem in many additional fields in the future, such as video or natural language processing.
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