ISM2: Optimizing Irregular-Shaped Matrix-Matrix Multiplication on GPUs

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Abstract—Linear algebra operations have been widely used in big data analytics and scientific computations. Many works have been done on optimizing linear algebra operations on GPUs with regular-shaped input. However, few works focus on fully utilizing GPU resources when the input is not regular-shaped. Current optimizations do not consider fully utilizing the memory bandwidth and computing power; therefore, they can only achieve sub-optimal performance. In this paper, we propose two efficient irregular-shaped matrix-matrix multiplication (GEMM) algorithms on GPUs—TSM2 and ISM2. Both of them focus on optimizing GEMMs with various input sizes where at least one of the matrices is tall-and-skinny. We implement our proposed algorithms and test on several modern Nvidia GPU micro-architectures. Experiments show that compared to state of the art, our TSM2 speeds up the computation by 1.1x~3x and improves the memory bandwidth utilization and computing power utilization by 8%~47.8% and 7%~37.3%, respectively, when the size of regular matrix is relatively large or medium. Moreover, our ISM2 speeds up the GEMM by 1.1x~3.5x and improve the memory bandwidth utilization by up to 55% when the size of regular matrix is relatively small.

Index Terms—Irregularly shaped; Matrix-matrix multiplication; GEMM; GPU; Optimization; CUDA.

1 INTRODUCTION

Matrix-matrix multiplication (GEMM) has been one of the most extensively used linear algebra operations in big data analytics and scientific computations. Due to many factors (such as algorithms, input data, etc.) the size or shape of input matrices for GEMM usually varies when it is used in different applications. For example, many modern highly scalable scientific simulation packages in the field of fluid dynamics, such as Finite Element Method (FEM) needs to compute many GEMM with small-sized input matrix. Artificial neural networks (ANN) involve using GEMM with small to medium input matrices. Matrix decompositions uses GEMM with large-sized input matrices [1], [2], [3], [4]. Thus, besides large-sized input, which has already been extensively optimized during the past decades, GEMM with small to medium sized input has also drawn much attention to recent researchers. For instance, Dong et al. [5] proposed MAGMA-Batched, which aims to batch small input matrices into larger ones in order to utilize the highly optimized implementations for large size on GPUs. Heinecke et al. [6] proposed to speed up GEMM with small input using architecture and instruction level optimization on modern CPU architectures.

Although previous works have focused on optimizing GEMM with different matrix sizes, most of them only assume that the input matrices are regular-shaped. In other words, the size mentioned in their works usually refers to both dimensions of the input matrix. For example, a small matrix means both of its width and height are small and their magnitudes are close to each other. When the dimensions of the input matrices have significant difference, we consider them as irregular-shaped inputs. In particular, many irregular-shaped inputs involve tall-and-skinny matrices, in which their widths are significantly smaller than their heights. Tall-and-skinny matrices are widely used in many applications. For instance, recent highly optimized K-means implementations [7], [8] use GEMM as their core computation, and the input size is mostly tall-and-skinny. This is because the number of centroids is usually far less than the number of input data points. Moreover, when GEMM is used for encoding checksums for many algorithm-based fault tolerance applications [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], the input would involve a tall-and-skinny checksum weight matrix.

However, previous efforts made for optimizing GEMM with regular-shaped input may not work for irregular-shaped inputs. For instance, Chen et al. [12] illustrates that calculating GEMM with tall-and-skinny matrices using vendor’s highly optimized linear algebra library (e.g., cuBLAS [20]) is slower than disassembling the tall-and-skinny input matrix into several vectors and then applying matrix-vector multiplications instead. However, it can be easily seen that this workaround is not efficient, since elements in input matrices are accessed by GPU more times than necessary.

To the best of our knowledge, GEMM with irregular-shaped input has not been fully studied and optimized. Our previous work [21] is the first work that focuses on irregular-shaped inputs on GPU. Specifically, it focuses on inputs that involve one large squared matrix and one tall-and-skinny matrix. In this paper, we aim to extend it to handle a boarder spectrum of irregular-shaped inputs for GEMM on GPUs.
The key insight of our work is that the computation characteristic of GEMM on modern computing systems is not always unchanged as we change the shape of input matrices. When the sizes of input matrices are regular-shaped (an $m \times k$ matrix multiplies an $k \times n$ matrix), the compute-to-load ratios of each element in the input matrices are $O(m)$ or $O(n)$. So, the regular-shaped GEMM operations are usually compute-bound especially for large matrices. However, when the input is irregular-shaped (e.g., $n$ is much smaller than $m$ and $k$), the average compute-to-load ratio is reduced to around $O(n) \approx O(1)$. Depending on $n$ and the performance characteristics of hardware (such as GPUs), the computation can be either compute-bound or memory-bound. As $n$ gets smaller, it moves toward memory-bound; otherwise, it moves toward compute-bound. To optimize GEMM with irregular-shaped input, it is critical to design a computation algorithm that considers both compute-bound and memory-bound cases.

The main contributions of this paper include:

- We study the limitation of current state-of-the-art GEMM implementation with irregular-shaped inputs. With benchmarking, we find that the under-utilization of GPU resources is the main reason that causes of performance degradation when the input is irregular-shaped.

- To handle a board spectrum of irregular-shaped inputs for GEMM on GPUs, we design two classes of algorithms focusing on different cases: (1) TSM2 is used to handle inputs with one tall-and-skinny matrix and one large-to-medium regular shaped matrix; (2) ISM2 is used to handle inputs with one tall-and-skinny matrix and one small regular shaped matrix.

- We present a performance model for TSM2 and compare our evaluation performance results that model. In addition, we examine the inadequacies of our original performance model and optimize ISM2 based on our observations and findings.

- Our experimental evaluation covers four generations of Nvidia GPUs: Kepler, Maxwell, Pascal, and Volta. Experiments show that our TSM2 and ISM2 can obtain 1.1x~3.0x and 1.1x~3.5x speedups, respectively, compared to state-of-the-art cuBLAS library.

2 BACKGROUND

2.1 Irregular Shaped Inputs for GEMM

In this work we restrict our scope to handle irregular shaped inputs that involve tall-and-skinny matrices. Tall-and-skinny matrix is typical class of matrices that can be found in irregular shaped inputs for GEMM. It is a kind of matrix in which its width is significantly smaller than its height. For example, input matrix A with size $20480 \times 20480$ and matrix B with size $20480 \times 2$ are considered as irregular shaped input in our work. We choose this input size and shape because we believe it can expose most of the challenges in irregular shaped input, so the design idea and optimization techniques introduced in this paper can be easily applied to other cases with slight modification.

2.2 cuBLAS

One of the most commonly used standard linear algebra libraries optimized for GPU is the cuBLAS library developed by Nvidia. The cuBLAS is the core computing library of many big data and scientific computing applications. For example, it is the GPU computing library for MAGMA heterogeneous linear algebra library [22], [23], [24], cuLA library [25], and cuDNN deep learning library [26]. With deep optimization by Nvidia, the cuBLAS library is able to provide state-of-the-art performance in many use cases.

For example, with inputs that involve tall-and-skinny matrices, the GEMM operation in current best implementation (cuBLAS 9.0 running on NVIDIA Tesla K40c GPU) only uses less than 10% of the theoretical peak memory bandwidth on average with $n = 2$ (Fig. 5 (a) - (b)). When $n = 16$, the same GEMM operation only uses less than 20% of the theoretical peak memory bandwidth on average (Fig. 5(g) - (h)). The resource utilization is even lower with larger input dimensions. By comparing the two input sizes, it can be seen for input with smaller $n$ values, the computation utilizes higher memory bandwidth (close to memory bound). On the other hand, for input with larger $n$ values, the computation utilizes higher computing power (close to compute bound). However, since we are unable to analyze the implementation of GEMM in none open-sourced cuBLAS library, it is hard to tell the exact characteristic of their computation.

3 Design of TSM2

To handle different kinds of irregular shaped GEMM on GPUs, we design two classes of algorithms: TSM2 and ISM2. TSM2 is used to handle inputs with one tall-and-skinny matrix and one large-to-medium regular shaped matrix. ISM2 is used to handle inputs with one tall-and-skinny matrix and one small regular shaped matrix. We start with the designing of TSM2.

3.1 Insight on Irregular Shaped Inputs

For regular shaped GEMM ($m \times k$ matrix multiplies $k \times n$ matrix), the input matrices size is $O(mk + kn)$, while the computing time complexity is $O(mk + kn)$, so each element in input matrices is used $O(mn)$ or $O(n)$ times within the entire computation process. Since loading data from GPU off-chip DRAM (i.e., global memory) to GPU is expensive and to avoid extensive data load operations, one common optimization for this kind of problem is minimizing the number of times each element needs to be loaded into the GPU by using fast on-chip memory (e.g., cache, registers) to enable data reuse. As the number of loads reduces, optimized GEMM tends to be compute-bound. For example, current GEMM implementation in cuBLAS library can reach near bare-metal performance on GPUs [27].

However, unlike regular-shaped GEMM, when one matrix is tall-and-skinny (e.g., $n \ll m, k$), each element in the input matrices is used $O(n)$ times on average:

$$\frac{(m \times k) \times n \times \text{times} + (k \times n) \times m \times \text{times}}{m \times k + k \times n} \approx O(n) \text{ times.}$$
Depending on the size of $n$ and target GPU peak computing power and memory throughput ratio, the computation can be either compute-bound or memory-bound. When $n$ gets smaller, the computation tends to be memory-bound. Otherwise, the problem tends to be compute-bound. In either case, the problem is always near the boundary between memory bound and compute bound, so it is critical to design an algorithm that is optimized for both two cases.

### 3.2 Algorithm Design

As the core of our optimization, algorithm design plays an important role. First, we need to consider how to fit the workload of our TSM2 into the programming model of CUDA (i.e., thread hierarchy). Although the workload can be easily decomposed into many independent smaller workloads, careful consideration on workload distribution is still necessary, since any unnecessary performance penalty can drastically cause GPU resource underutilization. Several factors are considered in our design:

1. Total number of global memory accesses;
2. Efficiency on global memory throughput;
3. Utilization on global memory throughput;
4. Parallelism of overall workload;
5. On-chip memory utilization;
6. Streaming Multiprocessor (SM) utilization;
7. Optimization for compute & memory-bound cases.

To achieve good performance, there must exist enough number of active threads in each SM of GPU to ensure proper instruction and memory access latency hiding. So, in our algorithm we divide the workload by assigning $n$ rows of matrix $A$ to $n$ different threads. Each vector-matrix multiplication is assigned to one thread (i.e., $(A[i, :] \times B)$). The benefit is three-fold: 1) this ensures high parallelism and high SM occupancy; 2) since the number of elements of matrix $A$ is much higher than matrix $B$, this kind of distribution ensures minimum number of memory accesses in favor of matrix $A$; 3) it also enables high memory access efficiency and throughput, since all memory accesses to matrix $A$ are naturally coalesced (assuming matrices are stored in column-major by convention).

As for the vector-matrix multiplication assigned to each thread, to further reduce the number of memory accesses to matrix $A$, we use outer-product style computation instead of the regular inner-product style computation. As shown in Alg. 4 if we use inner-product, each element of matrix $A$ is repeatedly referenced $n$ times. On the other hand, if we use outer-product as shown in Alg. 2 each element of matrix $A$ is referenced only once. (Please note, as we will discuss in later sections, when $n$ is larger than a certain threshold, elements in matrix $A$ still need to be referenced more than once due to the limited resources available for each thread, but it is still far lower than using inner-product). For large matrix $A$, the benefit is significant, since it greatly reduces the total number of global memory accesses during the entire GEMM computation. Also, the outer-product style does not bring any extra memory accesses to matrix $B$ compared to inner-product style. The only cost for outer-product is extra registers holding $n$ intermediate results. However, with proper tuning, they only bring little performance impact compared with extra memory accesses.

#### 3.3 Efficient Off-Chip Memory Access

One key factor of optimizing memory intensive applications is ensuring high off-chip memory access efficiency. Depending on the GPU model type or runtime configurations, global memory (off-chip) accesses of threads within the same warp can to coalesced into 128 byte- or 32 byte-transactions [28] if their addresses fall into the same 128 byte- or 32 byte-segments in global memory, which enables efficient use of memory bandwidth. Otherwise, the GPU still loads memory in 128 byte- or 32 byte-transactions, but it may contain unrequested data that are stored in neighbor addresses, which causes inefficient memory accesses.

Since each thread reads one row of matrix $A$ and the matrix is stored in column-major by convention, memory accesses are naturally coalesced when threads within the same warp access elements on different rows but on the same column. So, 100% memory access efficiency is achieved on matrix $A$. However, for matrix $B$, all threads access the same element at the same time, which results a single memory transaction containing one requested element and several unrequested neighbor elements. So, only $\frac{8 \text{ bytes}}{128 \text{ bytes}} = 6.25\%$ or $\frac{8 \text{ bytes}}{32 \text{ bytes}} = 25\%$ memory access efficiency is achieved for accessing 64-bit double floating point elements. Although the total number of elements in matrix $B$ is small, given that each element needs to be accessed $n$ times, this inefficient access pattern can still greatly impact the overall performance.

To improve the efficiency of memory accesses to matrix $B$, we utilize shared memory in GPU. Since it is located on-chip, shared memory gives us the speed of L1 cache and it is fully programmable. Threads within one thread block can use shared memory to share data. So, one key advantage of shared memory is that it eliminates the need for the consistency between patterns of data loading and data using pattern, which enables us to load global memory in the most efficient way and keep the way we use data as before.

#### Algorithm 1: Each thread’s workload with inner product.

```
Require: input matrix $A$ ($m \times k$) and $B$ ($k \times n$)
Require: output matrix $C$ ($m \times n$)
1: for $i = 1$ to $n$ do
2: for $j = 1$ to $k$ do
3: $C[thread_id, i] += A[thread_id, j] \times B[j, i]$
4: end for
5: end for
```

Algorithm 1: Each thread’s workload with inner product.

By using shared memory for accessing matrix $B$, we can reduce the total number of memory accesses and enable
coalesced memory access. As shown in Alg. 3 for each iteration, instead of letting threads request elements they need individually by themselves inefficiently, we now let a block of threads work together to fetch a tile of matrix B into the shared memory in a coalesce-compatible way (line 13-15). Then during computation, each thread references elements in matrix B through the shared memory instead of loading each one of them individually from global memory. This reduces the total number of accesses to matrix B from global memory (from $n$ to $n/t_1$ per element). Also, threads in a same thread block fetch elements of matrix B column by column, which enables coalesced memory access and greatly improves memory-access efficiency to 100%.

In Alg. 3, we also introduce three parameters: $t_1$, $t_2$, and $t_3$. These parameters are used for adjusting the performance and will be discussed in later sections.

Require: input matrix A ($m \times n$) and B ($k \times n$)
Require: output matrix C ($m \times n$)
1: $t_1 \leftarrow \text{tile}_B \times n$, $t_2 \leftarrow \text{tile}_A$, $t_3 \leftarrow \text{tile}_A$
2: Register: $A_1, A_2, ..., A_{t_1}$
3: Register: $C_1, C_2, ..., C_{t_3}$
4: Shared Memory: $\text{curr}B$ with size $t_1 \times t_2$
5: Threads per thread block $\leftarrow t_1$
6: Total thread blocks $\leftarrow m/t_1$
7: for $p = 1$ to $n$ with step size $= t_2$
8: \hspace{1cm} $C_1 \leftarrow C[\text{thread}_id, p]$
9: \hspace{1cm} $C_2 \leftarrow C[\text{thread}_id, p+1]$
\hspace{1cm} ...
10: \hspace{1cm} $C_{t_2} \leftarrow C[\text{thread}_id, p+t_2 - 1]$
11: for $j = 0$ to $k$ with step size $= t_3$
\hspace{1cm} $\text{Load a tile of B into shared memory}$
\hspace{1cm} $C[\text{thread}_id, p] \leftarrow B[j + \text{thread}_id, 0]$
\hspace{1cm} $C[\text{thread}_id, p] \leftarrow B[j + \text{thread}_id, 1]$
\hspace{1cm} $\text{Load a tile of A into registers}$
\hspace{1cm} $A_1 \leftarrow A[\text{thread}_id, 0]$
\hspace{1cm} $A_2 \leftarrow A[\text{thread}_id, 1 + 2]$
\hspace{1cm} ...
\hspace{1cm} $A_{t_1} \leftarrow A[\text{thread}_id, t_1 - 1]$
\hspace{1cm} $C_1 = A_1[0] \times \text{curr}B[\ldots, t_2 - 1]$
\hspace{1cm} $C_2 = A_1[1] \times \text{curr}B[\ldots, t_2 - 2]$
\hspace{1cm} $C_{t_2} = A_1[t_2 - 1] \times \text{curr}B[\ldots, t_2 - 1]$
17: for $l = j$ to $j + t_3$ with step size $= t_3$
\hspace{1cm} $\text{Add a tile of C into shared memory}$
18: \hspace{1cm} $A_1 \leftarrow A[\text{thread}_id, l + 2]$
\hspace{1cm} $A_2 \leftarrow A[\text{thread}_id, l + 3]$ 
\hspace{1cm} ...
\hspace{1cm} $A_{t_1} \leftarrow A[\text{thread}_id, l + t_3 - 1]$
\hspace{1cm} $C_1 = C_1 \times \text{curr}B[\ldots, l + t_2 - 1]$
\hspace{1cm} $C_2 = C_2 \times \text{curr}B[\ldots, l + t_3 - 2]$
\hspace{1cm} $C_{t_2} = C_{t_2} \times \text{curr}B[\ldots, l + t_3 - 1]$
19: end for
20: $C[\text{thread}_id, p] \leftarrow C_1$
21: $C[\text{thread}_id, p+1] \leftarrow C_2$
22: $C[\text{thread}_id, p+t_2] \leftarrow C_{t_2}$
23: end for

Algorithm 3: TSM2 with shared memory.

3.4 Optimizing Use of Shared Memory

Although fast, elements in shared memory still need to be loaded into registers before using [29]. Its accessing speed can affect the overall performance. Shared memory is divided into several same-sized memory banks for fast parallel accesses. Different threads accessing different memory banks can be done simultaneously. So, total $b$ memory banks can speedup overall shared memory throughput by $b$ times compared to the throughput of one single memory bank. However, if 4 threads in the same warp access different data from the same memory bank, $x$-way bank conflict would occur and each request is processed sequentially, which dramatically reduces the accessing throughput by a factor of $1/x$.

In our algorithm, threads in the same thread block load data from global memory into shared memory column by column to enable fast coalesced global memory access. Then threads access data from shared memory row by row during computation. How we store elements in shared memory will affect how these elements are accessed from memory banks, which affects the throughput of shared memory. We have two ways of storing a tile of matrix B in shared memory: column-major storage and row-major storage. To choose between the two ways, we need to analyze and compare which way brings the least overall bank conflict. We assume the size of one tile of matrix B is $t_1 \times t_2$ and $t_1$ is the multiply of total number of memory banks $b$ for simplicity.

For column-major storage, elements (32-bit words or 64-bit words) in the same column of one tile of matrix B are stored in successive memory banks. So, for shared memory with $b$ memory banks, every $t_1$ elements of one column are stored in $b$ different successive memory banks with each bank stores at most $t_2/b$ elements and is accessed by at most $warp size/b$ threads at the same time, which may potentially cause bank conflict if $warp size/b$ is greater than one.

For row-major storage, elements in the same row of matrix B are stored in successive memory banks. So, elements of the same column are stored in $b$ different banks with each bank stores at most $t_2$ elements from one column. Since each bank has $t_2$ times more elements from one column, totally each bank has at most $t_2$ times more thread accessing at the same time: $warp size/b \times t_2$, which may also potentially cause bank conflict.

On modern Nvidia GPUs, the warp size is fixed to 32 and total number of banks is also 32 [28], so column-major storage does not cause bank conflict, since each bank can only have up to one thread accessing. Row-major storage can cause up to 2-way bank conflict, which decreases overall shared memory throughput to $\frac{1}{2}$ of the peak throughput. As shown in Fig. 1, we load a 64 × 2 matrix tile into shared memory using column-major storage (left) and row-major storage (right). When using column-major storage, threads in one warp all access different banks, so no bank conflict occurs. But when using row-major storage, 32 elements are stored in 16 banks causing 2-way bank conflict.
column-major storage as it brings no bank conflict and potentially brings the highest shared memory throughput.

3.5 Overlapping Computation and Memory Access Latency

During execution, for each instruction issuing moment, each warp scheduler picks an eligible warp and send it to the corresponding component for execution. A warp becomes eligible only if all operands of its next instruction are ready. However, if a warp is loading data from global memory, it would take several hundred cycles before it can be ready for execution. To hide this long latency, we can either increase the number of threads reside in each SM to ensure there always exist eligible warps [30] or put independent instructions in between data loading and data consuming operations, so that warps are also eligible for execution during memory loading time. The first approach requires us to adjust the on-chip resource usage of each thread block.

We will leave that discussion in the next section. In this section, we will add independent instructions in between data loading and data consuming operations.

A shown in Alg. 3 line 13-15 and 18-20 load data from global memory and line 21-23 consume data once data is loaded. However, due to data dependency, there is no independent instruction in between, so once each warp issues global memory access requests, it must wait for the requested elements to be ready before it can proceed to computation.

So, to add independent instructions, we use data prefetching to mix the data loading and consuming between neighbor iterations. Specifically, instead of letting each iteration loads data that is going to be used for current iteration, we let the data needed for current iteration to be loaded by the previous iteration, so that its calculation will not be blocked by data loading (since the data are ready). When doing calculation, it also loads data that is going to be used for the next iteration. By overlapping data loading and computation, we can significantly improve memory bandwidth and SM utilization. We apply data prefetching to both matrix A and B.

As shown in Alg. 3 we design our TSM2 with data prefetching. In line 4 and 5, we allocate two sets of \( t_3 \) registers for storing current tile of elements of matrix A and next tile of element of matrix A for prefetching. In line 6 and 8, we allocate \( t_2 \) registers for data prefetching of elements in matrix B, and allocate \( t_1 \times t_2 \) for storing currently loaded tile of matrix B. Note that we cannot store current tile of matrix B in registers, because elements in matrix B need to be shared between threads during computation.

Before the core computation iteration (line 20-40), we pre-load current tile of matrix A and B into registers and shared memory (line 13-19), so that computation can start immediately as soon as we enter the computation loop without being blocked by any data dependency. The main computation resides in line 28-30. To overlap computation with memory accesses, we initiate loading for the next tile before the computation (line 21-23 for matrix B and line 25-27 for matrix A). We use two loops for loading matrix A and B, because we want to have the flexibility to adjust loading pace (tile size) differently for the two matrices. We

Require: input matrix A \((m \times k)\) and B \((k \times n)\)

Require: output matrix C \((m \times n)\)

1. \( t_1 \leftarrow \) tile size_A, \( t_2 \leftarrow \) tile size_B, \( t_3 \leftarrow \) tile size_C, \( t_3 \leftarrow \) tile size_A
2. Register: curr_A1, curr_A2, ..., curr_A3
3. Register: next_A1, next_A2, ..., next_A3
4. Register: next_B1, next_B2, ..., next_B3
5. Register: C1, C2, ..., C12
6. Shared Memory: curr_B with size \( t_1 \times t_2 \)
7. Threads per thread block \( \leftarrow t_1 \)
8. Total thread blocks \( \leftarrow m / t_1 \)
9. for \( p = 1 \) to \( n \) with step size \( t_2 \) do
10.  \( C_1 \leftarrow C[\text{thread}, p] \)
11.  \( C_2 \leftarrow C[\text{thread}, p + 1] \)
12.  \( \ldots \)
13.  \( \ldots \)
14.  \( \ldots \)
15.  \( \ldots \)
16.  \( \ldots \)
17.  \( \ldots \)
18.  \( \ldots \)
19.  \( \ldots \)
20.  ThreadsSyncromization()
21.  /*prefetch the next tile of B into registers*/
22.  if \( j + t_1 < n \) then
23.    next_B1 \leftarrow B[j + t_1 + \text{thread}_d, p]
24.  end if
25.  /*prefetch the next tile of A into registers*/
26.  if \( l + t_3 < n \) then
27.    next_A1 \leftarrow A[\text{thread}_d, l + t_3]
28.  end if
29.  /*prefetch the next tile of A into registers*/
30.  if \( l + t_3 < n \) then
31.    next_A1 \leftarrow A[\text{thread}_d, l + t_3]
32.  end if
33.  /*prefetch the next tile of B into registers*/
34.  if \( j + t_1 < n \) then
35.    next_B1 \leftarrow B[j + t_1 + \text{thread}_d, p]
36.  end if
37.  /*prefetch the next tile of B into registers*/
38.  if \( j + t_1 < n \) then
39.    next_B1 \leftarrow B[j + t_1 + \text{thread}_d, p]
40.  end if
41.  ThreadsSyncromization()
42.  curr_B[\text{thread}_d, 1] \leftarrow next_B1
43.  curr_B[\text{thread}_d, 2] \leftarrow next_B2
44.  curr_B[\text{thread}_d, 3] \leftarrow next_B3
45.  ThreadsSyncromization()
46.  curr_B[\text{thread}_d, 4] \leftarrow next_B4
47.  ThreadsSyncromization()

Algorithm 4: TSM2 with shared memory & data prefetching.

will discuss this in the next subsection. Fig. 2 and 3 show one iteration of our optimized TSM2 with data prefetching. LD C and ST C represent loading initial values from matrix C and storing final results back to matrix C. Each iteration we show three sub-iterations for loading matrix B. As we can see, we load pre-load the next tile of matrix B in concurrent with computation to improve memory bandwidth utilization. A threads synchronization is inserted in the end of each iteration. For the inner most iteration, we do the actual computation and pre-load elements from matrix A each time. Please note that the length of each rectangle does not accurately represent the exact execution time length and the ratio between number of LD nextA and LD nextB is not necessarily two in actual computation. Also, we show one thread block with four threads only for illustration proposes. As we will discuss in the next subsection that different parameter values can affect the length of each part and the ratio between number of LD nextA and LD
3.6 Parameters Definition

In Alg. 3 and Alg. 4, we introduced three adjustable parameters: $t_1$, $t_2$, and $t_3$. In this section, we first discuss how each parameter controls the computation of our TSM2. Then, we introduce our performance model that estimates how certain performance metrics change with these parameters. Finally, we explain our strategies of choosing values for these parameters in order to achieve high GPU resources utilization and optimized overall performance. Please note that the following discussions are all based on Alg. 4.

3.6.1 Behaviors of Parameters

First, we list the behaviors of each parameter as follows:

- $t_1$ specifies the number of rows of one tile of matrix B. To maximize use of available active threads and to avoid any inefficient thread execution caused by warp divergence, we let all threads in each thread block participating in fetching elements of matrix B. For fast coalesced global memory access, we let each thread fetch one row, so $t_1$ is also the total number of threads in each thread block. Also, since we let total $m$ threads working on the computation, the total number of thread blocks can be calculated as: $m/t_1$.

- $t_2$ specifies the number of elements in matrix C that each thread is working on at a time. It is used to divide the overall workload into several smaller workloads that are processed iteratively by each thread. Smaller workload makes each thread’s SM resource usage smaller, which allows us to keep higher SM occupancy. However, dividing the workload means we need to load matrix A repeatedly for each small workload. So, there is a trade-off. $t_2$ also affects the ratio between total number of memory fetches and computation operations in core part of our algorithm, which allows us to adjust the computation to be compute or memory-bound (will be discussed later in detail).

- $t_3$ specifies the number of elements in matrix A that each thread fetches at a time. Since elements fetched are independent to each other, they can be done without blocking each other, so $t_3$ can be used to adjust the memory loading concurrency.

3.6.2 Performance Metrics Estimation

In this section, we introduce our parameters based performance model that is used to estimate three important performance metrics: SM occupancy, memory bandwidth utilization and computing power utilization. These estimations will be used for optimizing the overall performance.

- **Max SM occupancy estimation**

  With these parameters we can calculate the max occupancy of each SM, which is defined as max number of active threads per SM. (Some works also use max number of warps, which is similar to ours. We found that using max thread is more consistent across our performance models. We also choose thread block size to be the dividend of this value to ensure expected number of threads are active.) This occupancy is mainly bound by the maximum hardware allowable number of threads ($HW_{MAX}$) and on-chip memory utilization per thread. We first calculate the total number of registers utilized per thread. Since register utilization can potentially be optimized by the nvcc compiler, we use maximum number of registers to estimate this value. First of all, there is a relatively fix amount of registers uses for CUDA initial setup, and we represent this amount as $C$. We get its amount through off-line profiling. Then, we need two sets of $t_2$ registers for storing elements of matrix B for both next tile fetching and current tile calculation. Please note that although the current tile of matrix B is stored in shared memory, it still needs to be transferred to registers for calculation. Next, we need $t_2$ registers for keeping intermediate results of matrix C. Finally, we need two sets of $t_3$ registers for storing elements of matrix A for both next tile fetching and current tile calculation. So, the total number of registers is:

  $$R_{thread} = (t_2 \times 3 + t_3 \times 2) \times \frac{\text{bytes per element}}{\text{bytes per register}} + C.$$

  As for shared memory, through shared memory is allocated per thread block, we calculate the average amount of shared memory that each thread uses for consistent calculation here. Since the size of allocated shared memory per thread block is $t_1 \times t_2$, and as we will discuss earlier that we set $t_1 = \text{threads per threadblock}$, the amount of shared memory allocated for each thread on average is:

  $$S_{thread} = t_2 \times \text{bytes per element}.$$
So, the max SM occupancy can be calculated as:

$$MaxOccup_{SM} = \min(HW_{MAX}, \frac{R_{SM}}{\text{thread}}, \frac{S_{SM}}{\text{thread}}).$$

In the above calculation, \(R_{SM}\) and \(S_{SM}\) stand for the max available registers and shared memory per SM.

- **Max memory bandwidth utilization estimation**
  Next, we estimate the max memory bandwidth utilization of our algorithm when the computation is memory-bound. In this case, loading elements of matrix A dominates the computation instead of floating point calculations in our algorithm. So, we can estimate max memory bandwidth utilization using the maximum number of concurrent global memory accesses per SM. It can be calculated as:

$$Concurrent_{mem} \approx MaxOccup_{SM} \times t_3.$$ 

Please note that, we only consider the memory accesses to matrix A here for simplicity. Since the majority memory accesses are for matrix A, this only brings minor inaccuracy. Then, similar to [30, 31] we calculate the least number of concurrent memory accesses per SM needed to achieve max memory bandwidth utilization using Little’s Law:

$$Throughput_{max_{mem}} = \frac{\text{Peak Band.}}{\text{# of SM x core clock}},$$

$$Concurrent_{max_{mem}} = \text{latency}_{mem} \times Throughput_{max_{mem}}.$$ 

The latency\(_{mem}\) is the average global memory access latency, which is considered as a constant in our model and is obtained through offline profiling. The estimated memory bandwidth utilization is:

$$Util_{mem} = \frac{Concurrent_{mem}}{Concurrent_{max_{mem}}}.$$ 

- **Max computing power utilization estimation**
  Next, we estimate the max computing power utilization of our algorithm when the computation is compute-bound. In this case, floating point calculation dominates the computation instead of memory accesses in our algorithm. So, we can estimate max computing power utilization using the maximum number of concurrent floating point operations per SM. It can be calculated as:

$$Concurrent_{comp} = MaxOccup_{SM} \times t_3 \times t_2.$$ 

Then, also similar to [30] we calculate the least number of concurrent floating point operations per SM needed to achieve max computing power utilization using Little’s Law:

$$Throughput_{max_{comp}} = \frac{\text{Peak Perf.}}{\text{# of SM x core clock}},$$

$$Concurrent_{max_{comp}} = \text{latency}_{comp} \times Throughput_{max_{comp}}.$$ 

The latency\(_{comp}\) is the average latency of floating point operations in our calculations, which is considered as a constant in our model and is obtained through offline profiling. So, the estimated computing power utilization is:

$$Util_{comp} = \frac{Concurrent_{comp}}{Concurrent_{max_{comp}}}.$$ 

- **Determine compute- or memory-bound**
  Given parameters and GPU specification, we can determine whether the current computation is memory or compute-bound. This is mainly determined by the inner most loop (line 24 - 34) of Alg. 4. The memory loading instructions (line 25-27) are overlapping with computation (line 28-30). Since line 31-33 depends on memory loading results, it serves as an implicit synchronization point for memory load and computation. The time takes for the two parts will determine whether the current computation is compute-bound or memory-bound. So, we first estimate the time takes for computation and memory access as follows:

$$time_{comp} = \frac{t_3 \times t_2}{\text{Peak Perf.} \times \text{# of SM} \times \text{Occupancy}_{SM}},$$

$$time_{mem} = \frac{t_2 \times \text{bytes per elem.}}{\text{Peak Band.} \times \text{# of SM} \times \text{Occupancy}_{SM}}.$$ 

Then, by comparing the two time costs, we can determine whether the current computation is compute-bound or memory-bound.

$$r = \frac{time_{comp}}{time_{mem}} = \frac{t_2}{\text{bytes per elem.}} \times \frac{\text{Peak Band.}}{\text{Peak Perf.}}.$$ 

As we can see, when \(r\) is greater than one, the computation is compute-bound. Otherwise, the computation is memory-bound. Also, since we divide the original workload into several smaller workloads using \(t_2\), this ratio is determined by \(t_2\). By adjusting \(t_2\), the actual computation can be shifted between compute and memory-bound. The boundary between the two cases can be calculated by setting the ratio \(r = 1\), so we get a threshold for \(t_2\):

$$t_2^{th} = \frac{\text{Peak Perf.}}{\text{Peak Band.}} \times \text{bytes per elem.}.$$ 

Similarly, we can also estimate computation characteristic of the original problem, in which the workload is not divided into smaller workloads. In this case, \(t_2\) is always fixed to \(k\). So, by comparing \(k\) with \(t_2^{th}\) we can estimate the computation characteristic. If \(k\) is greater than \(t_2^{th}\), the original problem is compute-bound; otherwise, it is memory-bound. It can be easily seen, depending on the value of \(t_2\) and \(k\), the computation characteristic of the current problem and original problem can be different, which can affect the overall performance. We discuss this in later part of this section.

3.6.3 Deciding Parameters

When choosing parameters, the first thing we should determine is whether we should optimize for computation or memory bandwidth. This is determined by whether the given TSM2 computation on the given GPU should be compute or memory-bound. In the last section, we proposed to estimate this characteristic by comparing \(n\) and \(t_2^{th}\), so that we can adjust parameters to optimize the computation in the right direction.

In the case where original problem is memory-bound \((n \leq t_2^{th})\), we need to keep the actual computation to be memory-bound also (let \(1 \leq t_2 \leq n\)) and optimize for memory bandwidth utilization. On the other hand, if the
original problem is compute-bound \((n > t_2^{threshold})\), we first try to keep the actual computation to be compute-bound too (let \(t_2^{threshold} < t_2 \leq n\)) and optimize of computing power utilization. However, in the case where \(t_2^{threshold}\) is too high on the given GPU, we also try to optimize it for memory-bound (let \(1 \leq t_2 \leq t_2^{threshold}\)) and output the result parameters that deliver better performance.

1. if \(n \leq t_2^{threshold}\) then
2. Total memory \(\approx m \times k \times \frac{n}{t_2} \times bytes\_per\_elem.\)
3. Bandwidth = PeakBand \(\times Util\_mem\)
4. Use Gradient Descent to Optimize \((t_2\) and \(t_3\)):
   \[Time = \frac{Total\_memory}{Bandwidth}\]
   with \(1 \leq t_2 \leq n\) and \(1 \leq t_3\)
5. Output: \(t_2\) and \(t_3\)
6. else
7. Total_flops = \(m \times k \times n \times 2\)
8. Compute\_power = Peak\_Perf. \(\times Util\_comp\)
9. Use Gradient Descent to Optimize \((t_2\) and \(t_3\)):
   \[Time_2 = \frac{Total\_flops}{Compute\_power}\]
   with \(t_2^{threshold} \leq t_2 \leq k\) and \(1 \leq t_3\)
10. Output: \(t_2\) and \(t_3\)

Algorithm 5: Parameter optimization for TSM2.

Alg. 5 shows the parameter optimization procedure for \(t_2\) and \(t_3\). We first determine the computation characteristic in line 1. If it is memory-bound, we optimize for total time cost to access needed elements from global memory (line 4). Otherwise, we optimize for either total computation time (line 9) or memory access time (line 14). Please note that we only count the total amount of memory accesses to matrix A for simplicity, since total accesses to matrix B is much less than matrix A, so this simplification only brings minor inaccuracy. Also, considering the total accesses to matrix B would bring one additional parameter \(t_1\), which can be hard to optimize since \(t_1\) is also related to threads organization that is hard for modeling-based estimation. The memory bandwidth utilization term \((Util\_mem)\) and computing power utilization term \((Util\_comp)\) is calculated using the equation mentioned before. Since we have two parameters \((t_2\) and \(t_3\)) in our optimization target, we use Gradient Descent (GD) to do the optimization. In GD, based on our experience, we set initial value of both \(t_2\) and \(t_3\) to be 1, and step size to be 0.1. The stop threshold is set to be 1e-4, since we do not need very accurate precision. The final \(t_2\) and \(t_3\) are rounded to the nearest integers.

To optimize \(t_1\), we found it only controls the number of threads in each thread block. Since the total number of threads is fixed to \(m\), \(t_1\) only determines how these threads are organized into thread blocks. There is trade-off: if \(t_1\) is large, the total number of accesses to elements of matrix B is reduced, however, large thread block means large number of threads need to participate in the same synchronization, which may have impact on performance. On the other hand, if \(t_1\) is small, the total number of accesses to elements of matrix B higher, but the smaller thread block makes scheduling more flexible and efficient. It is hard to determine the optimum value of \(t_1\) theoretically, so we use offline profiling to choose the best value. Specifically, once \(t_2\) and \(t_3\) are determined, we benchmark different \(t_1\) values that can divide MaxOccup\_SM as mentioned earlier and choose the \(t_1\) that deliver the best performance. Although \(t_1\) seems to have direct effect on shared memory allocation (or max SM occupancy), it actually has limited impact on it, since we fix the amount of shared memory per thread \((S\_thread = t_1 \times bytes\_per\_element)\).

4 Experimental Evaluation on TSM2

4.1 Experiments Setup

We evaluate our optimized TSM2 on our heterogeneous testbed cluster—Darwin. We run each test on a single GPU node with single GPU card. We conduct our tests on three different commonly used modern Nvidia GPUs with three different micro-architectures: Kepler, Maxwell, and Pascal. For Kepler GPU, we use Tesla K40c, which has 1430 GFLOPS peak double floating point performance and 288 GB/s memory bandwidth. For Maxwell GPU, we use Tesla M40, which has 213 GFLOPS peak double floating point performance and 288 GB/s memory bandwidth. For Pascal GPU, we use Tesla P100, which has 4600 GFLOPS peak double floating point performance and 720 GB/s memory bandwidth.

We implemented our TSM2 using CUDA C for both single and double floating point input. We disabled compiler auto unrolling for better control on register allocation. For comparison, we compare our TSM2 with GEMM in the current latest cuBLAS library and latest BLASX library [32]. Also, we try to compare our work with KBLAS [33], however since its GEMM kernel is based on cuBLAS, its performance is identical to cuBLAS, so we omitted its results. Each test is repeated multiple times to reduce noise and timed using CUDA Events API. We measure performance by calculating the performance of FAMD instructions. We also measure the global memory throughput using \(nvprof\) on the command line with \(-metrics\) \(gl\_throughput\) option. In addition, we use \(-metrics\) \(gl\_efficiency\) option to verify 100% global memory access efficiency is achieved in our optimization during development.

Our input matrix is initialized with random floating point numbers \((0\ to\ 1)\). We test the multiplication between a large square sized matrix multiplies a tall-and-skinny matrix. The size of the large input matrix is from 10240 \(\times 10240\) to 30720 \(\times 30720\). The tall-and-skinny input matrix has size ranges from 10240 \(\times n\) to 30730 \(\times n\) with \(n\) equals 2, 4, 8, 16.

4.2 Tests with Different Optimization Combinations

We use the GEMM in cuBLAS as comparison baseline. We apply different combinations of optimization in TSM2 and compare them with GEMM in cuBLAS and BLASX. We have totally four versions of TSM2:

- \(V_0\): the most straightforward inner product version as described in Alg. 1.
- \(V_1\): the outer production version as in Alg. 2. This version reduces the total number of global memory accesses from algorithm level;
Limited by the page space, we only show the result on K40c GPU. Our optimization behaves similar on other GPUs. To evaluate our optimization, we need to determine by which resource our program is bounded. Since, the threshold $t_2(k_{40c}) \approx 40$, the computation is always memory bound for the given $n$ values. The optimized parameters are: $t_2 = n$, $t_3 = 4$, and $t_1 = 128$. The parameters are only applied to the last to versions of TSM2. Fig. 4 shows the speedup of different versions in single and double precision. From the results, we can see that the TSM2-V0 suffers from really poor performance due to the requirement of much higher number of global memory accesses in the inner product version. The TSM2-V1, on the other hand, significantly improve the performance compared to TSM2-V0 (2.2x~4.7x faster), since it requires much lower number of global memory accesses. TSM2-V2 further improves the efficiency of global memory access to matrix B, which plays a vital role in the overall performance. In addition, the shared memory shares tiles of matrix B between threads within a thread block also reduced the total number of memory accesses to matrix B. This leads to additional 1.1x to 2.1x speedup. Finally, the data prefetch introduced in TSM2-V3 further mitigate the memory access bottleneck, which brings additional 1.3x~3.5x speedup.
In addition to Kepler micro-architecture, we also conduct test on newer Maxwell, Pascal, and Volta GPUs. Similar as with Kepler GPU, we get $t_{\text{threshold}} \approx 6$ and $t_{\text{threshold}} \approx 50$. Tesla M40 has slower computing power, so the computation with input with $n = 16$ is compute bound. Our parameter optimization procedure also output parameters in favor of computing optimization: $t_2 = 8$, $t_3 = 4$, and $t_1 = 256$. As shown in Fig. 6, our optimized implementation achieves 1.1x -1.9x (avg. 1.47x) speedup on Tesla M40 with 7% to 37.3% (avg. 20.5%) computing power utilization improvement compared to the GEMM function in cuBLAS 9.0. P100 has much stronger computing power, as we can see the computation with input with $n = 16$ is memory bound. Our parameter optimization procedure also output parameters in favor of memory optimization: $t_2 = 4$, $t_3 = 4$, and $t_1 = 128$. As shown in Fig. 7, our optimized implementation achieves 1.1x -3.0x (avg. 2.15x) speedup on Tesla P100 with 17% to 47.6% (avg. 34.7%) memory bandwidth utilization improvement compared to the GEMM function in cuBLAS.

We also test TSM2 on the Nvidia Tesla V100 GPU, with the Volta architecture. As shown in Fig. 8, speedsups of up to 1.35x are achieved on single precision, while speedsups of up to 3.2x are achieved on double precision. Note that the speedup for $n = 16$ on single precision is slower than cuBLAS. This is due to cuBLAS’s single-precision GEMM being optimized for $32 \times 32$ matrices; thus we no longer target this case. Finally, note that the V100 kernels achieve higher percent memory bandwidth usage than on other GPUs. This is partly attributed to the improvements of Volta architecture over previous architectures. More specifically, the Volta’s improved HBM2 memory allows many workloads to obtain up to 19% more memory bandwidth usage than Pascal GPUs, according to the Volta whitepaper [34].

### 4.5 Tests on Uneven Input

On the Tesla V100, we also evaluate uneven input. The input is formatted as follows: a rectangular matrix of size $m \times k$ and a tall-and-skinny matrix of size $k \times n$, where $k$ is smaller than $m$ by some small integer factor. Evaluating this case reveals very little performance impact, as demonstrated in Fig. 8. Although smaller than $m$, $k$ is still large enough to ensure the kernel follows our performance model. The kernel’s memory bandwidth usage remains similar to the case where $m = k$, and the kernel’s performance scales linearly with the size of the matrices.
To explain these results, we expand upon the performance model proposed in Section 3.6.2. This model assumes that the maximum theoretical occupancy is always achieved throughout the computation. However, since the algorithm loops $k \times n^2$ times, and $k$ is very small, each thread does not perform enough workload to hide latency and hence low occupancy. Consequently, the program issues fewer global memory reads, resulting in less efficient memory usage. TSM2 thus performs in latency-bound mode (neither compute-bound nor memory-bound) on this particular input case, as indicated in a prior study [30].

**5.2 Proposed Optimizations for ISM2**

Based on these observations, we further design two optimization approaches. Both optimization approaches intend to exchange warp latency for memory access latency by launching fewer threads. As a result, each thread performs more work, and the accumulated warp latency can be replaced by the memory access latency. Since we are launching fewer threads than the number of rows of matrix $A$, we must divide it into several horizontal tiles. Here we introduce a new parameter $tcf$ to represent the tile number of $A$ under our new case. We launch $\frac{n}{tcf}$ threads in the new kernel.

The first optimization involves dividing the multiplication into $tcf$ parts, where each part consists of multiplying
We thus have to determine an appropriate warp latency just as it does in the naive adaptation of TSM2. Performance would suffer. If the algorithm is launched with an insufficient number of threads, the parallelism becomes too low and hence the computation time increases and memory access bandwidth decreases. As a result, computation time is replaced with that of different kinds of latency such as memory bandwidth latency. As fewer threads are launched, the impact of warp latency increases and fewer threads are launched, the impact of warp latency decreases and memory access bandwidth increases in this case. Note that for this case the number of threads launched is replaced with the identifier thread replaced by the identifier r/7.

Algorithm 6: Proposed optimization 1 for ISM2.

The second optimization is interleaving the computation of each of the tiles, rapidly loading elements from different tiles of matrix A and loading and storing intermediate sums in matrix C. Once a t1 x t2 tile of matrix B is loaded, the intermediate results are loaded, computed, and stored for each tile of matrix A. The C register set is loaded with values from matrix C which contains the product accumulated so far. After the computation is finished, the values are stored to matrix A as the next tile of matrix A is prepared for computation. To quickly switch between tiles, values from matrix C are prefetched in addition to the prefetching already described in Alg. 4. A new set of registers, nextC[1...t2], is used to store the values of C associated with the next tile of A. The elements of A and B are accessed only \( \frac{n}{t2} \) times, though each element of C is accessed \( \frac{k}{t1} \times \frac{n}{t2} \) times. However, since we do not achieve either high occupancy or high memory bandwidth in this case, we are not as concerned about issuing more memory read instructions. The detail is described in Alg. 7.

Fig. 12 illustrates the effects of the two optimizations on both performance and memory bandwidth usage. As fewer and fewer threads are launched, the impact of warp latency is replaced with that of different kinds of latency such as memory bandwidth latency. As a result, computation time decreases and memory access bandwidth increases in this case. Note that for this case the number of threads launched must be reduced to at least \( \frac{m}{k} \) before a significant decline in speedup or memory bandwidth utilization occurs. This is attributed to that the kernel must manage so many threads that so little work when \( m = 10^7 \).

Therefore, we must choose an appropriate tcf, determining the number of threads to launch for each kernel. If the algorithm is launched with an insufficient number of threads, the parallelism becomes too low and hence the performance would suffer. If the algorithm is launched with too many threads, the performance would be impacted by warp latency just as it does in the naive adaptation of TSM2. We thus have to determine an appropriate tcf for each target system with offline profiling.
**References**

[1] “MAGMA.” [Online]. Available: icl.cs.utk.edu/magma

[2] J. Chen, L. Tan, P. Wu, D. Tao, H. Li, X. Liang, S. Li, R. Ge, L. Bhuyan, and Z. Chen, “GreenLA: green linear algebra software for gpu-accelerated heterogeneous computing,” in High Performance Computing, Networking, Storage and Analysis, SC16: International Conference for. IEEE, 2016, pp. 667–677.

[3] L. Tan, S. Kothapalli, L. Chen, O. Hussaini, R. Bissiri, and Z. Chen, “A survey of power and energy efficient techniques for high performance numerical linear algebra operations,” Parallel Computing, vol. 40, no. 10, pp. 559–573, 2014.

[4] L. Tan, S. L. Song, P. Wu, Z. Chen, R. Ge, and D. J. Kerbyson, “Investigating the interplay between energy efficiency and resilience in high performance computing,” in 2015 IEEE International Parallel and Distributed Processing Symposium. IEEE, 2015, pp. 786–796.

[5] T. Dong, A. Haidar, P. Luszczek, S. Tomov, A. Abdelfattah, and J. Dongarra, “Magma batched: A batched bias approach for small matrix factorizations and applications on gpus,” Technical report, Tech. Rep., 2016.

[6] A. Heinecke, G. Henry, M. Hutchinson, and H. Pabst, “Libxsmm: accelerating small matrix multiplications by runtime code generation,” in High Performance Computing, Networking, Storage and Analysis, SC16: International Conference for, 2016.

[7] I. S. Dhillon, Y. Guan, and B. Kulis, “Kernel k-means: spectral clustering and normalized cuts,” in Proceedings of the tenth ACM SIGKDD international conference on Knowledge discovery and data mining. ACM, 2004, pp. 551–556.

[8] “K-means by NVIDIA.” [Online]. Available: https://github.com/NVIDIA/kmeans

[9] J. Chen, X. Liang, and Z. Chen, “Online algorithm-based fault tolerance for cholesky decomposition on heterogeneous systems with gpus,” in Parallel and Distributed Processing Symposium, 2016 IEEE International, 2016.

[10] K.-H. Huang, I. Abraham et al., “Algorithm-based fault tolerance for matrix operations,” Computers, IEEE Transactions on, 1984.

[11] J. Chen, S. Li, and Z. Chen, “Gpu-abft: Optimizing algorithm-based fault tolerance for heterogeneous systems with gpus,” in Networking, Architecture and Storage (NAS), 2016 IEEE International Conference on.

[12] J. Chen, H. Li, S. Li, X. Liang, P. Wu, D. Tao, K. Ouyang, Y. Liu, K. Zhao, Q. Guan et al., “Fault tolerant one-sided matrix decompositions on heterogeneous systems with gpus,” in Proceedings of the International Conference for High Performance Computing, Networking, Storage, and Analysis. IEEE Press, 2018, p. 68.

[13] D. Tao, S. L. Song, S. Krishnamoorthy, P. Wu, X. Liang, E. Z. Zhang, D. Kerbyson, and Z. Chen, “New-sum: A novel online abft scheme for general iterative methods,” in Proceedings of the 25th ACM International Symposium on High-Performance Parallel and Distributed Computing, 2016.
[14] P. Wu, Q. Guan, N. DeBardeleben, S. Blanchard, D. Tao, X. Liang, J. Chen, and Z. Chen, “Towards practical algorithm based fault tolerance in dense linear algebra,” in Proceedings of the 25th ACM International Symposium on High-Performance Parallel and Distributed Computing, 2016.

[15] P. Wu, N. DeBardeleben, Q. Guan, S. Blanchard, J. Chen, D. Tao, X. Liang, K. Ouyang, and Z. Chen, “Silent data corruption resilient two-sided matrix factorizations,” in Proceedings of the 22nd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, 2017.

[16] X. Liang, J. Chen, D. Tao, S. Li, P. Wu, H. Li, K. Ouyang, Y. Liu, F. Song, and Z. Chen, “Correcting soft errors in fast online Fourier transform,” in Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis. ACM, 2017, p. 30.

[17] S. Tomov, J. Dongarra, and M. Baboulin, “Towards dense linear algebra for hybrid GPU accelerated manycore systems,” Parallel Computing, 2010.

[18] S. Tomov, R. Nath, H. Ltaief, and J. Dongarra, “Dense linear algebra solvers for multicore with GPU accelerators,” in Proc. of the IEEE IPDPS'10. Atlanta, GA: IEEE Computer Society, 2010.

[19] J. Dongarra, M. Gates, A. Haidar, J. Kurzak, P. Luszczek, and Z. Chen, “Fmm2: optimizing tall-and-skinny matrix-matrix multiplication on gpus,” in Proceedings of the ACM International Conference on Supercomputing, 2019, pp. 106–116.

[20] S. Tomov, J. Dongarra, and M. Baboulin, “Towards dense linear algebra for hybrid GPU accelerated manycore systems,” Parallel Computing, 2010.

[21] C. NVIDIA, “Basic linear algebra subroutines (cublas) library,” 2017.

[22] S. Tomov, R. Nath, H. Ltaief, and J. Dongarra, “Dense linear algebra solvers for multicore with GPU accelerators,” in Proc. of the IEEE IPDPS'10. Atlanta, GA: IEEE Computer Society, 2010.

[23] S. Tomov, R. Nath, H. Ltaief, and J. Dongarra, “Dense linear algebra solvers for multicore with GPU accelerators,” in Proc. of the IEEE IPDPS'10. Atlanta, GA: IEEE Computer Society, 2010.

[24] S. Tomov, R. Nath, H. Ltaief, and J. Dongarra, “Dense linear algebra solvers for multicore with GPU accelerators,” in Proc. of the IEEE IPDPS'10. Atlanta, GA: IEEE Computer Society, 2010.

[25] [“cudnn,” 2018. [Online]. Available: https://developer.nvidia.com/cudnn]

[26] [“cublas benchmark,” 2018. [Online]. Available: http://developer.download.nvidia.com/compute/cuda/compute-docs/cuda-performance-report.pdf]

[27] [“cudnn programming guide,” 2018. [Online]. Available: http://docs.nvidia.com/cuda/cuda-c- programming-guide/index.html#multi-processor-level]

[28] [“Pix programming guide,” 2018. [Online]. Available: http://docs.nvidia.com/cuda/parallel-thread-execution/index.html#data-movement-and-conversion-instructions-id]

[29] V. Volkov, “Understanding latency hiding on gpus,” Ph.D. dissertation, University of California, Berkeley, 2016.

[30] H. Wong, M.-M. Papadopoulos, M. Sadoghi-Alvandi, and A. Moshovos, “Demystifying gpu microarchitecture through microbenchmarking,” in Performance Analysis of Systems & Software (ISPASS), 2010 IEEE International Symposium on, 2010.

[31] L. Wang, W. Wu, Z. Xu, J. Xiao, and Y. Yang, “Blas: A high performance level-3 blas library for heterogeneous many-gpu computing,” in Proceedings of the 2016 International Conference on Supercomputing. ACM, 2016, p. 20.

[32] A. Abdelfattah, D. Keyes, and H. Ltaief, “Kblas: An optimized library for dense matrix-vector multiplication on gpu accelerators,” ACM Transactions on Mathematical Software (TOMS), vol. 42, no. 3, p. 18, 2016.

[33] “Nvidia Tesla V100 GPU Architecture,” 2017. [Online]. Available: https://images.nvidia.com/content/volta-architecture/pdf/volta-architecture-whitepaper.pdf

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