Subthreshold-swing physics of tunnel field-effect transistors

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Band-to-band tunnel field-effect-transistors (TFETs) are considered a possible replacement for the conventional metal-oxide-semiconductor field-effect transistors due to their ability to achieve subthreshold swing (SS) below 60 mV/decade. This letter reports a comprehensive study of the SS of TFETs by examining the effects of electrostatics and material parameters of TFETs on their SS through a physics based analytical model. Based on the analysis, an intrinsic SS degradation effect in TFETs is uncovered. Meanwhile, it is also shown that designing a strong onset condition, quantified by an introduced concept - “onset strength”, for TFETs can effectively overcome this degradation at the onset stage, and thereby achieve ultra-sharp switching characteristics. The uncovered physics provides theoretical support to recent experimental results, and forward looking insight into more advanced TFET design.

I. INTRODUCTION

Band-to-band tunnel FET is a promising candidate for next generation low-power digital applications, due to its low OFF-current and small subthreshold-swing compared to conventional metal-oxide-semiconductor field-effect transistors (MOSFETs). However, TFETs suffer from low ON-current mainly because of the large band-to-band tunneling (BTBT) barrier, especially for large band gap semiconductors including silicon, the material of choice for mainstream semiconductor technology. To overcome this shortcoming and further improve the subthreshold characteristics, many efforts have been focused on proposing new structures/materials for TFETs, among which several exhibit near perfect (step-like) switching characteristics, i.e., ultra-small SS. However, the hidden physics and design rules leading to such ideal subthreshold characteristics are still not apparent. As a result, certain degree of ambiguity prevails over the choice of structures and materials for achieving small SS, such as, which material system among Si, Ge and InGaAs has the greatest potential to reach the smallest SS. This work is aimed at exploring and understanding the physics behind these issues, based on which both theoretical and experimental results could be well explained, and more importantly, a general design rule for TFETs with small SS can be formulated.

II. ANALYTICAL MODEL FOR SS

Within the Landauer’s formalism, the current for one conduction mode in TFETs can be expressed as

\[ I_{ds} = \frac{2q}{h} \int_{E_{cc}}^{E_{ox}} T(E) [f_s(E) - f_d(E)] dE \]  

(1)

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FIG. 1. Device structure (top) and energy band diagram (bottom) along the channel surface. Fermi-Dirac distribution of electrons in the source region, $f_s(E)$, is schematically shown. $W_T$ is the minimum tunnel width. $E_vj$ is the valence band maxima at the source/channel junction. $\Delta E$ is the allowed tunnel window. $E_{f/d}$ is the source/drain Fermi level and $E_g$ is the band gap.

where $q$ is the electron charge, $h$ is the Planck’s constant, $T(E)$ is the BTBT probability, and $f_{f/d}(E)$ is the source/drain Fermi-Dirac distribution function. $E_{vs}$ and $E_{vc}$ (Fig. 1) are the valence band maxima in the source region and conduction band minima in the channel region, respectively. Fig. 1 shows the schematic illustration (top) of a double-gated n-TFET used as the sample device in this paper and the corresponding energy band diagram (bottom) along its channel surfaces. P-type source and n-type drain are highly doped, while the channel is left intrinsic. $W_T$ is the minimum tunnel width, $E_{vj}$ is the valence band maxima at the source/channel junction, $\Delta E$ is the allowed tunnel window contributing to transport, and $E_{f/d}$ is the source/drain Fermi level. Assuming $T(E)$ remains constant across $\Delta E$, it can be taken out of the integral in Eq. (1). This assumption is valid for BTBT in the range of small $\Delta E$ (within a few $kT$), which is the regime of essence for the SS physics of TFETs, as will be pointed out in the subsequent sections. In circuit applications, the drain voltage of an n-TFET is usually at least 0.1 V larger than the source voltage. This way, $f_d(E)$ is small enough to be neglected compared to $f_s(E)$. Thus, the source to channel tunneling current can be formulated as

$$I_{ds} = \frac{2q}{h} T(\Delta E) F_{\text{Integral}}$$

where

$$F_{\text{Integral}} = kT \ln \left( \frac{1 + \exp \left( \frac{(E_{fs} - E_{vs} + \Delta E)/kT}{1 + \exp \left( (E_{fs} - E_{vs})/kT \right)} \right)} \right)$$

$F_{\text{Integral}}$ is the integral of the Fermi function part in Eq. (1). Note that the Fermi-Dirac distribution of electrons (in the source region, which is the relevant region in this work) is truncated by the band gap of the source region at $E_{vs}$.

To obtain the expression of $T(\Delta E)$, we need to solve the 2D Poisson’s equation to obtain the channel potential. Simplifying 2D Poisson’s equation into a 1D form as expressed in Eq. (4) by using Yan’s parabolic approximation is an efficient approach in FET compact modeling.

$$\frac{d^2 \phi_s}{dx^2} + \frac{V_{gs} - V_{fb} - \phi_s}{\lambda^2} = \frac{\rho}{\varepsilon}$$

where $\phi_s$ is the surface potential; $\lambda$ is the natural length; $V_{fb}$ is the flat band voltage; $\rho$ is the charge density; and $\varepsilon$ is the material permittivity. Following this approach, Zhang et al. recently developed an analytical model that can accurately capture the electrostatic potential profile around the tunnel junction in double-gated TFETs. Employing their model, $E_{vj}$ can be expressed as:

$$E_{vj} = \sqrt{(E_{vs} - E_{fs})^2 + \gamma^2} + 2\gamma(\Delta E_{sc} + E_{vs} - E_{fs}) - (\Delta E_{sc} + E_{vs} - E_{fs} + \gamma)$$
where \( \Delta E_{sc} = \Delta E + \delta E + E_g, \delta E \) (fixed at 0.1 eV in this work) is the value of \( E_{cc} - E_{vs} \) at \( V_{gs} = 0 \), and

\[
\gamma = N_{a, eff} q^2 \lambda^2 / \varepsilon_{ch}, \quad N_{a, eff} = N_a - \frac{\varepsilon_{ox}(\Delta E_{sc} + E_{vs} - E_{fs})}{\pi q^2 T_{ox} T_{ch}}
\]

where \( N_a \) is the source doping level; \( \varepsilon_{ch/ox} \) and \( T_{ch/ox} \) are the permittivity and thickness of channel material/gate dielectric, respectively.

The minimum tunnel width can be written as\(^{15}\)

\[
W_T = L_1 + L_2 - \lambda \cosh^{-1} \left( \frac{\Delta E + \delta E - E_{fs} + E_{v, W_T}}{E_{vs} - E_{fs} + \delta E} \right)
\]

where \( \lambda = \sqrt{\varepsilon_{ch} T_{ox} T_{ch}/(2e_{ox})} \)

\[
L_1 = \sqrt{2\varepsilon_{ch}(E_{vs} - E_{v,j})/(q^2 N_{a, eff})}
\]

\[
L_2 = \lambda \cosh^{-1} \left( \frac{\Delta E_{sc} + E_{vs} - E_{fs} - (E_{vs} - E_{v,j})}{E_{vs} - E_{fs} + \delta E} \right)
\]

\[
E_{v, W_T} = \sqrt{(E_{vs} - E_{fs} + \delta E)^2 + \gamma^2 + 2\gamma(\Delta E + \delta E + (E_{vs} - E_{fs}))}
\]

\[
-(\Delta E + \delta E + E_{vs} - E_{fs} + \gamma)
\]

Tunneling probability is then calculated using the Wentzel–Kramers–Brillouin (WKB) approximation and the two-band dispersion relation,\(^{16}\)

\[
T(\Delta E) \approx \exp \left( -\frac{\pi \sqrt{2m_T E_g^3/2}}{4q \hbar F} \right)
\]

where \( m_T \) is the tunnel effective mass, and \( F \) is the junction electric field modeled as \( F = E_g / W_T \).

According to the definition, \( SS \) equals the gate voltage swing needed to change the drain current by one decade. Hence, combining Eq. (10) with Eq. (2), \( SS \) can be expressed as

\[
SS = \left( \frac{d \log_{10}(I_{ds})}{d(\Delta E/q)} \right)^{-1} = \frac{SS_T SS_{FD}}{SS_T + SS_{FD}}
\]

where \( SS_T = \left( \frac{d \log_{10}(T(\Delta E))}{d(\Delta E/q)} \right)^{-1} \), \( SS_{FD} = \left( \frac{d \log_{10}(E_{mean})}{d(\Delta E/q)} \right)^{-1} \)

Eq. (11) clearly shows the manner in which the tunneling probability variation and the truncated Fermi-Dirac distribution contribute to the total \( SS \) through \( SS_T \) and \( SS_{FD} \), respectively. \( SS_{FD} \) can be easily expressed as

\[
SS_{FD} = \frac{\ln(10) k T}{q} \left( 1 + \exp \left( \frac{E_{vs} - E_{fs} - \Delta E}{k T} \right) \right) \ln \left( 1 + \exp \left( (E_{fs} - E_{vs} + \Delta E)/k T \right) \right) \left( 1 + \exp \left( (E_{fs} - E_{vs})/k T \right) \right)
\]

The expression for \( SS_T \) can be written as,

\[
SS_T = \frac{2\sqrt{2} \ln(10) \hbar}{-q \pi \sqrt{m_T E_g d W_T} d(\Delta E)}
\]

where \( \hbar \) is the reduced Planck’s constant.

III. EFFECT OF FERMI-DIRAC TRUNCATION

Before delving into the \( SS \) physics through the developed model, the transfer characteristics and \( SS \) behavior of a conventional Si TFET and a high-performance graphene-nanoribbon (GNR) based...
TFET are comparatively shown in Fig. 2. The purpose of showing this comparison is simply to point out the differences between the I-V curves of these two devices, and thereby serve as the starting point for the discussion on the $SS$ behavior. The width and thickness of the GNR channel are 2.34 nm and 0.34 nm, respectively, while those of the Si channel are 1 μm and 10 nm, respectively. Other features of the two devices are kept identical. An in-house NEGF simulator and the Sentaurus device simulator are used to simulate the GNR and Si devices, respectively. Fig. 2 displays two main points that will be analyzed thereafter. Firstly, the $SS$ of GNR TFET (red squares) approaches zero at some $V_g$, while that of the Si TFET (red triangles) does not. Secondly, the $SS$ of GNR TFET increases much faster than that of Si TFET with $V_g$.

Fig. 3 shows the shapes of $SS$, $SS_T$, and $SS_{FD}$ versus $ΔE$ for a double-gated Si TFET, calculated with Eqs. (11)–(13). Relevant parameters are listed in the caption of Fig. 3. When $N_d$ is low enough so that $E_F$ is higher than $E_{vs}$, $SS_{FD}$ expressed by Eq. (12) reduces to $SS_{FD} = \frac{kT}{q} \left( 1 - \exp \left( \frac{-ΔE}{kT} \right) \right)$ (14) $SS_{FD}$ exponentially approaches zero with decreasing $ΔE$, which stems from the truncation of the Fermi-Dirac distribution by the band gap of the source region (will be abbreviated as Fermi-Dirac truncation in following text). Starting from $ΔE = 2kT$ to region II ($2kT < ΔE < E_{vs} - E_F$), $SS_{FD}$ initially stays at a constant value of 60 mV/dec, and then quickly increases, which mimics the thermionic emission dominated subthreshold behavior of a MOSFET. Note that Eq. (11) can’t describe the total $SS$ in region II and III as accurately as in region I (the onset stage), which is the focus of this work. Calculated results in region II and III only provide a qualitatively correct trend of $SS$, as confirmed by the extracted $SS$ shape in the numerical simulation in Fig. 2.

IV. EFFECT OF OFF-CURRENT

Based on Eq. (14) and Eq. (11), all TFETs should have a near-zero $SS$ within the onset stage due to their BTBT nature determined Fermi-Dirac truncation. The reason why a near-zero $SS$ in
FIG. 3. $SS_T$, $SS_{FD}$ and total $SS$ versus the tunnel window $\Delta E$. Parameters of the double-gated Si TFET used in the calculation are: $m_T = 0.65m_0$, $N_a = 3 \times 10^{20}$/cm$^3$, $T_{at} = 1$ nm, $T_{th} = 10$ nm, $E_g = 1.12$ eV, at room temperature.

FIG. 4. BTBT current at $\Delta E = 0.5kT$ ($I_{onset}$) and OFF-current $I_{off}$ (for homo-junction (homol) TFET) versus (a) source doping level $N_a$, (b) natural length $\lambda$, (c) energy band gap $E_g$ and (d) tunnel effective mass $m_T$. Blue dotted line in (c) schematically represents the shape and level of $I_{off}$ for hetero-junction (heterJ) TFET, for which $E_g$ is the band gap overlap between source and channel. The horizontal lines are schematically drawn to illustrate the independence or weak dependence of $I_{off}$ on relevant parameters.

Simulated Si TFET does not appear is due to the fact that the OFF-current “immerses” the relatively low but quite sharply changing BTBT current within the onset stage, as schematically denoted (by red dotted curve) on the transfer characteristics curve for Si TFET in Fig. 2.

For a well designed/fabricated TFET, thermionic component of OFF-current is dominant and can be modeled as,

$$I_{off} = \frac{2q}{h} \int_{E_fs}^{+\infty} f_s(E)dE \approx \frac{2qkT}{h} \exp\left(-\frac{E_g + E_{vs} - E_fs}{kT}\right)$$

(15)

To bring out the near-zero-$SS$ nature of TFET’s, the BTBT current at the onset stage should be higher than the OFF-current. To quantify this effect, $I_{onset}$ is defined as the BTBT current at $\Delta E = 0.5kT$ ($\sim 13$ meV). The concept of “onset strength” is proposed as the difference between $I_{onset}$ and $I_{off}$. It is well known that the source doping level $N_a$, natural length $\lambda$, band gap $E_g$ and tunnel effective mass $m_T$ are the four critical parameters for TFETs performance. The former two can be classified as electrostatic parameters, while the remaining two as material parameters. We make these four parameters as variables in our study to lump the effect of several promising technologies, such as low-dimensional materials/structures, strain technology, III-V compound, etc. Fig. 4 shows the dependence of $I_{onset}$ and $I_{off}$ on these four parameters. As shown in Fig. 4(a), $I_{onset}$ has a maximum value at a relatively high $N_a$. The initial increase of $I_{onset}$ with $N_a$ is due to the shrinkage of the tunnel width $W_T$ leading to higher tunneling probability. However, when $N_a$ increases too much, $E_g$ moves far below $E_{vs}$, leading to severely reduced occupation probability of states around the valence band.
FIG. 5. \( SS_T \) at \( \Delta E = 2kT \) (\( SS_{T@2kT} \)) and minimum \( SS \) (\( SS_{min} \)) versus (a) source doping level \( N_a \), (b) natural length \( \lambda \), (c) energy band gap \( E_g \) and (d) tunnel effective mass \( m_T \).

edge of the source region and thus to the reduction of \( I_{onset} \). \( I_{off} \) keeps decreasing with \( N_a \) because minority carrier density, which contributes to the OFF-current proportionally, decreases with \( N_a \). When any of \( \lambda \), \( E_g \) or \( m_T \) is reduced, \( I_{onset} \) is significantly enhanced as shown in Figs. 4(b)–4(d). The difference between the last three cases is that while \( I_{off} \) remains constant with \( \lambda \) and \( m_T \) variation, it keeps decreasing with increasing \( E_g \) (similar to \( I_{onset} \)). In other words, \( N_a \), \( \lambda \) and \( m_T \) are the explicit parameters to enhance the “onset strength” and thus “pull” the steepest part of BTBT current above the OFF-current, while \( E_g \) is not explicit, since its effect on the “onset strength” depends on the rate of change of both the OFF-current and the BTBT current w.r.t \( E_g \) (Fig. 4(c)). There is, however, an exceptional condition in which \( E_g \) also becomes explicit. That is the hetero-junction TFET in which \( E_g \), for \( I_{off} \) calculation, is the band gap of the source material, while for \( I_{onset} \) it is the band gap overlap between the source and the channel material. For this case, the red dashed line for \( I_{off} \) should be replaced by the blue horizontal dotted line (Fig. 4(c)).

It is worthwhile to note that the OFF-current of a not well designed/fabricated TFET should also include trap assisted tunnel leakage and gate leakage, which are not taken into account in Eq. (15). The trap assisted tunnel leakage may stem from interface states near the tunneling junction, defects at the tunneling junction (especially in hetero-junction TFETs), and high doping induced band edge states. These leakages will increase the OFF-current and somehow degrade the “onset strength” and prevent TFETs from exhibiting ultra-small \( SS \). This issue needs further investigation but is beyond the scope of this article.

V. INTRINSIC SS DEGRADATION IN TFET

In the TFET community, there exists an ambiguity about the minimum \( SS \) (\( SS_{min} \)) achievable for certain structure or material system. So far, it is clear that \( SS_{min} \) appears at the current level of \( I_{BTBT} = I_{off} \) (Fig. 2). For devices with strong “onset strength”, \( SS_{min} \) is apparently near-zero. However, strong “onset strength” usually requires stringent fabrication condition and thus is not easy to achieve. In this situation, to clarify the ambiguity, we need to extend the discussion from the contribution of Fermi-Dirac truncation to that of tunneling probability variation, i.e., \( SS_T \). \( SS_T \) very close to \( \Delta E = 0 \) does not play an important role, since the near-zero \( SS_{FD} \) there results in a near-zero \( SS \), as reflected by Eq. (11). Therefore, a figure of merit – \( SS_{T@2kT} \), which equals the value of \( SS_T \) at \( \Delta E = 2kT \) is defined as an indicator of \( SS_T \) behavior. Fig. 5 shows the dependence of \( SS_{T@2kT} \) and \( SS_{min} \) on \( N_a \), \( \lambda \), \( E_g \) and \( m_T \). When \( N_a \) increases, or \( \lambda \) (or \( m_T \) or \( E_g \)) decreases, \( SS_{T@2kT} \) becomes larger. At first glance, these results seem unexpected, since the tunneling efficiency, which is a more familiar performance parameter for TFET, is expected to improve with higher \( N_a \), or smaller \( \lambda \) (or \( m_T \) or \( E_g \)), i.e., “\( I_{on} \) improving condition”. Following analysis verifies that these results are physical. The two electrostatic parameters \( N_a \) and \( \lambda \), determine the depletion widths \( L_1 \) (Eq. (7)) in the source region, and \( L_2 \) (Eq. (8)) in the channel region, respectively. When \( N_a \) becomes higher and/or \( \lambda \) becomes smaller, \( L_1 \) and/or \( L_2 \) shrink leading to the reduction of \( W_T \) according to Eq. (6). With higher \( N_a \),
and/or smaller $\lambda$, $W_T$ is smaller as expected. The important point is that the rate of change of $W_T$ w.r.t. $\Delta E$ also becomes smaller. This is because stronger electrostatic screening effect for devices with smaller $W_T$ leads to slower rate of change of $W_T$, i.e., smaller $dW_T/d\Delta E$. Therefore, $SS_T$ becomes larger for higher $N_a$ or smaller $\lambda$ according to Eq. (13). The manner in which the material parameters $E_g$ and $m_T$ affect $SS_T$ is also clear from Eq. (13), but is governed by the nature of tunneling rather than the junction electrostatics, since Eq. (13) is directly derived from WKB approximation based tunneling probability expressed in Eq. (10). From the above analysis of $SS_T$, it can be deduced that these four parameters degrade (through $SS_T$ in Eq. (11)) the SS in a manner that can be regarded as intrinsic properties of TFETs, and hence, the corresponding degradation in SS can be termed as intrinsic SS degradation. This effect is usually overlooked in the TFET community, but it plays an important role in determining the achievable $SS_{min}$.

**VI. PATHWAYS TOWARD MINIMUM SS**

It can be observed from Fig. 5 that the effects of $N_a$, $\lambda$, and $m_T$ on $SS_{min}$ are opposite of that on $SS_{T@2kT}$, while the effect of $E_g$ displays the same behavior for both. The reason can be explained in a schematic manner as shown in Figs. 6(a) and 6(b). Compared to the reference condition (grey curves), both $I_{BTBT}$ and $SS$ in “$I_{on}$ improving condition” (black curves) increase over the entire range of $\Delta E$, due to the reduced tunnel barrier and intrinsic SS degradation, respectively. As analyzed above, the levels of $I_{off}$ are critical in determining $SS_{min}$, since $SS_{min}$ appears at $I_{BTBT} = I_{off}$. As shown in Fig. 4, $I_{off}$ decreases with $N_a$, and remains nearly constant with $\lambda$ (or $m_T$), while increases with $E_g$. Therefore, $I_{BTBT}$ and $I_{off}$ meet at much smaller $\Delta E$ (labeled as $\Delta E_0$) than the original $\Delta E$ that corresponds to the reference condition (labeled as $\Delta E_0$) for $N_a$, $\lambda$ and $m_T$ cases, while at relatively large $\Delta E$ (labeled as $\Delta E_i$) (may be larger than $\Delta E_0$) for the case of $E_g$. These trends lead to smaller $SS_{min}$ for higher $N_a$ or smaller $\lambda$ (or $m_T$), while larger $SS_{min}$ for smaller $E_g$, as shown in Fig. 6(b). In other words, the enhancement of “onset strength” with higher $N_a$ or smaller $\lambda$ (or $m_T$) overcomes the intrinsic SS degradation, leading to a reduction of $SS_{min}$, while that with smaller $E_g$ is not strong enough to reach the same result. Several representative experimental results ($I_{off}$ and $SS_{min}$) obtained recently on TFETs, are summarized in Fig. 6(c). The Si SOI device is set as the reference device, and improvements on specific parameters are denoted by corresponding arrows. It can be observed that using small-$E_g$ channel materials, such as Ge and III-V, does not improve SS, because increased $I_{off}$ degrades the “onset strength”, in agreement with the uncovered SS physics above. It is worthwhile to
mention that SS of III-V devices may also suffer from interface traps, which is expected to improve with more advanced interface engineering in the near future. To increase ON-current while retaining small SS, hetero-junction TFET (with large $E_g$ on source side for lowering leakage and small $E_g$ or the band gap overlap of source and channel, for enhanced tunneling) could be a solution, which has been experimentally achieved to some extent in Ref. 6. Excellent electrostatics, arising from using nanowire structure, or using atomically-thin emerging 2D semiconducting crystals$^{20-22}$ as channel materials, are also promising alternatives.

Thus far, the reasons for faster increase of SS of GNR TFET with $\Delta E$ compared to that for Si TFET, and the step-like transfer characteristics in many proposed TFETs$^{2-4}$ can be well explained. Strong “onset strength” in these devices make their ultra-sharply changing BTBT current visible, i.e., larger than $I_{off}$ at the onset stage, leading to ultra-small $SS_{min}$. At the same time, the intrinsic SS degradation of these devices is also strong, i.e., SS increases rapidly with gate bias (i.e., $\Delta E$), leading to quick flattening of the BTBT current, and thus to step-like transfer characteristics. From the application point of view, TFETs with strong “onset strength” should only be used for ultra-low power application in which supply voltages are ultra-low. The reason is that larger supply voltages result in larger regions (flattened part of BTBT current) degraded by intrinsic SS degradation. Thus the average SS over specific $I_d$ or $V_g$ (or supply voltage) interval will be increased, with reduced advantage of ultra-small $SS_{min}$ at the onset stage.

VII. SUMMARY

In summary, essential physics of the SS of TFETs is studied in this paper, from the perspectives of Fermi-Dirac distribution and tunneling probability variation. The novelty of this work can be attributed to the much improved insights gained into the SS characteristics of TFETs, wherein it is shown, by examining the effects of the four critical parameters for TFET performance - the source doping level, natural length, band gap and tunnel effective mass, that the truncation of the Fermi-Dirac distribution, OFF-current and the uncovered intrinsic SS degradation compete with each other and determine the minimum achievable SS. Detailed analysis suggests that small natural length, suitably high source doping level, and small tunnel effective mass, are preferred for homo-junction TFET design. On the other hand, for the hetero-junction TFET design, in addition to these three parameters, small band gap only at the tunnel junction (keeping band gap relatively large in the remaining areas to suppress OFF current) is preferred. The uncovered SS physics in this work is consistent with recent representative experimental results and offers the nanoscale device community deeper insight into TFET design.

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