Multipliers: comparison of Fourier transformation based method and Synopsys design technique for up to 32-bits inputs in regular and saturation arithmetics

Danila Gorodecky
United Institute of Informatics Problems of NAS of Belarus
University of Bologna
email: danila.gorodecky@gmail.com

Abstract

The technique for hardware multiplication based upon Fourier transformation has been introduced. The technique has the highest efficiency on multiplication units with up to 8 bit range. Each multiplication unit is realized on base of the minimized Boolean functions. Experimental data showed that this technique the multiplication process speed up to 20% higher for 2 – 8 bit range of input operands and up to 3% higher for 8 – 32 bit range of input operands than analogues designed by Synopsys technique.

1 Introduction

There is a variety of approaches to arithmetical operation of multiplication for hardware realization, but there is no universal approach for efficient hardware multiplication. The efficiency of each technique is limited by a number of conditions: bit ranges, number of multiplicands, area of implementation, special arithmetic (signed, unsigned, saturation arithmetic, residue number system, and etc.).

Our approach for designing $A \cdot B = R$ multiplier reminds of Lego constructing. Initially we develop a multiplication block (or blocks), and then build whole multiplier using these structural blocks, which we call monolithic multipliers.

Our technique is relevant to two known mathematical algorithms. First is called Karatsuba multiplication [1] and the second is Fourier transformation method (FTM) [2].

Karatsuba multiplication splits $A$ and $B$ into two vectors with the same length and then performs multiplication independently for each vector. But it works only for a big number of multiplication (for some hundreds bits numbers) [1].

A more similar technique is FTM. It is known that this approach is suitable for big numbers [2, 3] and implemented in arithmetic in modulo [3].

In this paper we focus on regular arithmetic and in saturation arithmetic multiplication. If in the regular arithmetic a result of multiplication $A \cdot B = R$ is $2n$-bits vector $R$, for $A$ and $B$ are $n$-bits vectors, then in saturation arithmetic a result has the same length as input operands. We consider multiplication from 2 to 32 bits of input operands.

This paper is organized as follows: in Section 2 we describe monolithic multipliers design technique and propose results of the synthesis; Section 3 dedicated to description of monolithic based multipliers in the regular arithmetic; Section 4 dedicated to description of monolithic based multipliers in the saturation arithmetic; in Section 5 we propose a technique of reducing of adders in hardware multiplication; Section 6 provides the results of the synthesis of monolithic based multipliers comparing with Synopsys analogues; the last section resumes our study.

All multipliers have been described on Verilog and synthesised (without place-and-routing) with Synopsys 2014 CAD on 28 nm technology in Synopsys standard synthetic library with compile ultra mode. We propose no-memory technique and it is dedicated to unsigned multiplication.
2 Design of Monolith Multipliers

The name of monolithic multiplier refers to a holistic structure. An idea of monolithic multipliers synthesis concludes in the generating of small range multipliers from the truth table of Boolean functions. Initially we find out more suitable monolithic multiplier in small bit range. Afterward it is repeatedly implemented to design a final structure of multiplier.

It is a well known fact that linear growing of number on variables of a Boolean function lead to exponential growing of the truth table. Thus minimization of disjunctive normal form (DNF) for a function on more than 10-15 variables with a standard minimization is unacceptable. So we study monolithic multipliers with no more than 16 inputs and 16 outputs.

Realization of the multiplication is based on Boolean functions implementation, those we used some types of minimizations of Boolean functions: Espresso in the version 2.3 [4] and the ELS minimizer [5].

We used two options of Espresso minimization: exact minimization and qm (QuineMcCluskey) algorithm of minimization. The exact minimization is more powerful, but for 10 inputs and 10 outputs, i.e., for $A \cdot B = R$, where $A$ and $B$ are 5-bits vectors, minimization with exact option is not suitable. For a bigger bit range multipliers we used qm option of minimization.

We implemented following ELS minimizer options: options, class, literals, Espresso with power consumption minimization. In some cases class and literals minimizations showed more preferable results than Espresso.

Table 1 shows number of disjunctions in full DNF and in minimized DNF for all monolithic multiplier in regular and in saturation arithmetics.

| Multiplier | Truth table | Minimized |
|------------|-------------|-----------|
| $2 \times 2 \rightarrow 4$ | 14 | 8 |
| $3 \times 3 \rightarrow 6$ | 111 | 40 |
| $4 \times 4 \rightarrow 8$ | 678 | 160 |
| $5 \times 5 \rightarrow 10$ | 3733 | 629 |
| $6 \times 6 \rightarrow 12$ | 18953 | 2435 |
| $7 \times 7 \rightarrow 14$ | 92334 | 9194 |
| $8 \times 8 \rightarrow 16$ | 434660 | 38957 |

| Multiplier | Truth table | Minimized |
|------------|-------------|-----------|
| $2 \times 2 \rightarrow 2$ | 2 | 10 |
| $3 \times 3 \rightarrow 3$ | 68 | 14 |
| $4 \times 4 \rightarrow 4$ | 4 | 92 | 44 |
| $5 \times 5 \rightarrow 5$ | 2064 | 143 |
| $6 \times 6 \rightarrow 6$ | 10272 | 511 |
| $7 \times 7 \rightarrow 7$ | 49216 | 1881 |
| $8 \times 8 \rightarrow 8$ | 229504 | 6916 |

We synthesized monolithic $2 \times 2$, $3 \times 3$, $4 \times 4$, $5 \times 5$, $6 \times 6$, $7 \times 7$, and $8 \times 8$ multipliers and compared the results in the speed with Synopsys analogues. The comparisons of the speed of computations for monolithic multipliers and Synopsys are represented for regular arithmetic on Figure 1 and for saturation arithmetic on Figure 2.

According to the comparison monolithic $3 \times 3$ is faster on 20%, $4 \times 4$ on 15%, and $5 \times 5$ on 21% than Synopsys. As monolithic blocks we propose to use $4 \times 4$ and $5 \times 5$ multipliers, so we will use them to constructing blocks for monolithic based multipliers.
3 Design of Monolithic Based Multipliers in Regular Arithmetic

An idea of the technique for design $A \cdot B = R$ multiplier reminds of Lego constructing. Initially we found out more suitable monolithic multiplier in a small bits range. Afterward we implement this monolithic block to $A \cdot B = R$ multiplier. It is known a similar approach for a regular multiplication which is a branch of Fourier transformation [2].

We represent a mathematical algorithm aimed to implement for hardware realization and based on FTM. The main idea of FTM consists in splitting the input vectors into $k$ groups with $m$ bits in every group. So it is suitable for $k \cdot m$ dimension vectors. In common $A \cdot B = R$ can be represented as follows:

$$A = \sum_{i=1}^{k} A_i \cdot 2^{m \cdot (i-1)} \text{ and } B = \sum_{j=1}^{k} B_j \cdot 2^{m \cdot (j-1)}, \text{ then } R = \sum_{i=1}^{k} \sum_{j=1}^{k} A_i \cdot B_j \cdot 2^{m \cdot (i+j-2)}. \quad (1)$$

According to Table 1 a) we take $m = 3, 4,$ and $5$.

Let’s consider multiplication $A \cdot B = R$, where $A, B$ are 14-bits and $R$ is 28 bits. So we split each input $A = \{a_{14}, a_{13},..., a_1\}$ and $B = \{b_{14}, b_{13},..., b_1\}$ into three 4-bits and into one 2-bits vectors: $A_1 = \{a_4, a_3, a_2, a_1\}, A_2 = \{a_8, a_7, a_6, a_5\}, A_3 = \{a_{12}, a_{11}, a_{10}, a_9\}, A_4 = \{a_{14}, a_{13}\}, B_1 = \{b_4, b_3, b_2, b_1\}, B_2 = \{b_8, b_7, b_6, b_5\}, B_3 = \{b_{12}, b_{11}, b_{10}, b_9\}, B_4 = \{b_{14}, b_{13}\}$, where $a_{14}$ and $b_{14}$ are the most significant bits. Thus $A = \{A_4, A_3, A_2, A_1\}$ and $B = \{B_4, B_3, B_2, B_1\}$. Referring to the conditions of the example formula (1) takes the following form:

$$R = A_1 \cdot B_1 + A_1 \cdot B_2 \cdot 2^4 + A_1 \cdot B_3 \cdot 2^8 + A_1 \cdot B_4 \cdot 2^{12} + A_2 \cdot B_1 \cdot 2^4 + A_2 \cdot B_2 \cdot 2^8 + A_2 \cdot B_3 \cdot 2^{12} + A_2 \cdot B_4 \cdot 2^{16} + A_3 \cdot B_1 \cdot 2^8 + A_3 \cdot B_2 \cdot 2^{12} + A_3 \cdot B_3 \cdot 2^{16} + A_3 \cdot B_4 \cdot 2^{20} + A_4 \cdot B_1 \cdot 2^{12} + A_4 \cdot B_2 \cdot 2^{16} + A_4 \cdot B_3 \cdot 2^{20} + A_4 \cdot B_4 \cdot 2^{24}. \quad (2)$$

According to (2) the final phase of computation consists of fifteen operations of adding. It means that implementing in hardware the last step of computation will consists of a 4-level tree of fifteen adders.

4 Design of Monolithic Based Multipliers in Saturation Arithmetic

The process of monolithic based multipliers in saturation arithmetic has a specific detail. In this type of arithmetic we are interested in the $n$ least significant bits of the result of multiplication, thus inputs and output vectors have the same length $n$.

We can use formula (1) for multiplication in saturation arithmetic. It is clear that for 14 by 14 bits multiplication with 4-bits of splitting of inputs in saturation arithmetic we have the next redundant operands: $A_2 \cdot B_4 \cdot 2^{16}, A_1 \cdot B_3 \cdot 2^{16}, A_3 \cdot B_4 \cdot 2^{20}, A_4 \cdot B_2 \cdot 2^{16}, A_4 \cdot B_3 \cdot 2^{20}, A_4 \cdot B_4 \cdot 2^{24}$. But what about $A_1 \cdot B_4 \cdot 2^{12}, A_2 \cdot B_3 \cdot 2^{12}, A_3 \cdot B_2 \cdot 2^{12}, A_4 \cdot B_1 \cdot 2^{12}$. Results of
these multiplications are 8-bits vectors, but we need only 4 least significant bits of them. In this case we use the multiplication modulo 4 and can represent a 14 by 14 multiplication as follows:

\[
R = A_1 \cdot B_1 + A_1 \cdot B_2 \cdot 2^4 + A_1 \cdot B_3 \cdot 2^8 (\text{mod} \ 2^6) + A_1 \cdot B_4 \cdot 2^{12} (\text{mod} \ 2^2) + \\
A_2 \cdot B_1 \cdot 2^4 + A_2 \cdot B_2 \cdot 2^8 (\text{mod} \ 2^6) + A_2 \cdot B_3 \cdot 2^{12} (\text{mod} \ 2^2) + \\
A_3 \cdot B_1 \cdot 2^8 (\text{mod} \ 2^6) + A_3 \cdot B_2 \cdot 2^{12} (\text{mod} \ 2^2) + \\
A_4 \cdot B_1 \cdot 2^{12} (\text{mod} \ 2^2).
\]

This manner of multiplication save \(\frac{k^2-k}{2} - 2\) adders comparing with (1), where \(k\) is a number of \(m\)-bits groups of subvectors of inputs. For example, in 14 by 14 bits multiplication with 4-bits splitting of the inputs we reduce number of adders from 15 to 9, and in 32 by 32 multiplication and the same splitting of inputs we save 26 adders.

5 Adder-tree Levels Reduction Technique

We proposed a technique to reduce the number of adding in the final step. The principle is to join in one vector as much as possible results of monolithic multiplications. According to the 14 \(\times\) 14 multiplication in regular arithmetic results of multiplications \(A_1 \cdot B_1 = R_1\) and \(A_1 \cdot B_3 \cdot 2^8 = R_3 \cdot 2^8\) will be represented as eight and sixteen bits vectors respectively, where \(R_3 \cdot 2^8\) includes eight zeros in the least significant bits. In this case \(R_1\) and \(R_3\) can be joint in one vector. Implementing this principle for (4) we reduced number of adders from 15 to 6, and the adder-tree has been reduced from 4 to 3 levels.

Thus after replacement of \(A_1 \cdot B_1 = R_1\), \(A_1 \cdot B_2 = R_2\), \(A_1 \cdot B_3 = R_3\), \(A_1 \cdot B_4 = R_4\), \(A_2 \cdot B_1 = R_5\), \(A_2 \cdot B_2 = R_6\), \(A_2 \cdot B_3 = R_7\), \(A_2 \cdot B_4 = R_8\), \(A_3 \cdot B_1 = R_9\), \(A_3 \cdot B_2 = R_{10}\), \(A_3 \cdot B_3 = R_{11}\), \(A_3 \cdot B_4 = R_{12}\), \(A_4 \cdot B_1 = R_{13}\), \(A_4 \cdot B_2 = R_{14}\), \(A_4 \cdot B_3 = R_{15}\), \(A_4 \cdot B_4 = R_{16}\) and implementing of joining technique the result of multiplication will be represented with the next formula:

\[
R = (R_{16}, R_{11}, R_3, R_1) + (R_{12}, R_7, R_2, 0000) + (R_{15}, R_{10}, R_5, 0000) + \\
+ (R_8, R_6, 00000000) + (R_{14}, R_9, 00000000) + (R_4 + R_{13}, 000000000000),
\]

where \(R_1, R_2, R_3, R_4, R_6, R_7, R_9, R_{10}, R_{11}\) are 8-bits vectors, \(R_4, R_8, R_{12}, R_{13}, R_{14}, R_{15}\) are 6-bits vectors, and \(R_{16}\) is 4-bits vector.

The logic scheme of the adders tree of \(A \cdot B = R\) multiplication, where \(A, B\) are 14 bits inputs and \(R\) is 28 output vector, is proposed on Figure 3.

![Adders tree for 14 by 14 bits multiplication](image)

Figure 3: Adders tree for 14 by 14 bits multiplication, where "&" means concatenations, i.e. joining of binary vectors

In the common case an adders tree consists of \(\lceil \log_2 M \rceil\) levels, where \(M = n \cdot k\). In Table 2 we compare number of adders in a common case and after final reduction for regular arithmetic a) and for saturation arithmetic b).
## Results and Discussion

We studied multiplication in regular and in saturation arithmetics: $8 \times 8$, $10 \times 10$, $12 \times 12$, $14 \times 14$, $16 \times 16$, $18 \times 18$, $20 \times 20$, $22 \times 22$, $24 \times 24$, $26 \times 26$, $28 \times 28$, $30 \times 30$, $32 \times 32$, where $10 \times 10$, $20 \times 20$, and $30 \times 30$ multiplications were realized with $5 \times 5$ monolithic multipliers utilizing and the rest based on $4 \times 4$ multiplication.

Figure 4 shows the results of the experiments in regular arithmetic.

### Figure 4: Synthesis of multipliers in regular arithmetic

![Synopsys and Monolithic Multiplication Frequencies](image)

The jittering of the frequency of calculation for proposed multipliers and Synopsys in the regular arithmetic is limited by: 8% for $5 \times 5$ based multipliers; 5% for $4 \times 4$ based multipliers; 21% for monolithic multipliers. The advantage of multipliers achieves: to 8% by Synopsys comparing with the proposed; 1% for $4 \times 4$ monolithic based multipliers comparing with Synopsys; 21% for monolithic multipliers comparing with Synopsys.

Figure 5 shows the result of the experiments in saturation arithmetic.

The jittering of the frequency of calculation for proposed multipliers and Synopsys in saturation arithmetic is limited by: 6% for $5 \times 5$ based multipliers; 3% for $4 \times 4$ based multipliers; 33% for monolithic multipliers. The advantage of multipliers achieves: to 4% by Synopsys comparing with the proposed; 3% for $4 \times 4$ monolithic based multipliers comparing with Synopsys; 33% for monolithic multipliers comparing with Synopsys.

The area of the proposed technique of monolithic based multipliers comparing with Synopsys jitters from 216% (for monolithic based on $4 \times 4$ multipliers) to 523% (for monolithic based on $5 \times 5$ multipliers) for both type of arithmetics.

Moreover we conducted experiments where Espresso multipliers have been changed by Synopsys $4 \times 4$ and $5 \times 5$ multiplication. In these cases area of the resulting multipliers oversized the Synopsys analogues in $5 - 10\%$, and in some cases even was smaller on $2 - 3\%$, but disadvantage

### Table 2: Comparison of the number of adders for the common case of multiplication and for the proposed technique in

| Multipliers        | Common case | Reducing technique |
|--------------------|-------------|--------------------|
| $8 \times 10 \rightarrow 16$ | 3 | 2 |
| $10 \times 10 \rightarrow 20$ | 3 | 2 |
| $12 \times 12 \rightarrow 24$ | 19 | 10 |
| $14 \times 14 \rightarrow 28$ | 15 | 6 |
| $16 \times 16 \rightarrow 32$ | 25 | 6 |
| $18 \times 18 \rightarrow 36$ | 25 | 8 |
| $20 \times 20 \rightarrow 40$ | 15 | 6 |
| $22 \times 22 \rightarrow 44$ | 35 | 10 |
| $24 \times 24 \rightarrow 48$ | 35 | 10 |
| $26 \times 26 \rightarrow 52$ | 48 | 12 |
| $28 \times 28 \rightarrow 56$ | 48 | 12 |
| $30 \times 30 \rightarrow 60$ | 35 | 10 |
| $32 \times 32 \rightarrow 64$ | 63 | 14 |

### Table 2: Comparison of the number of adders for the common case of multiplication and for the proposed technique in

| Multipliers        | Common case | Reducing technique |
|--------------------|-------------|--------------------|
| $8 \times 8$ | 2 | 2 |
| $10 \times 10 \rightarrow 10$ | 2 | 2 |
| $12 \times 12 \rightarrow 12$ | 5 | 4 |
| $14 \times 14 \rightarrow 14$ | 9 | 6 |
| $16 \times 16 \rightarrow 16$ | 10 | 6 |
| $18 \times 18 \rightarrow 18$ | 14 | 6 |
| $20 \times 20 \rightarrow 20$ | 9 | 6 |
| $22 \times 22 \rightarrow 22$ | 21 | 10 |
| $24 \times 24 \rightarrow 24$ | 21 | 10 |
| $26 \times 26 \rightarrow 26$ | 27 | 12 |
| $28 \times 28 \rightarrow 28$ | 28 | 12 |
| $30 \times 30 \rightarrow 30$ | 21 | 10 |
| $32 \times 32 \rightarrow 32$ | 35 | 21 |

...
in the speed was around 5 – 10%.

7 Conclusions and Further Work

We considered the approach of hardware multiplication. The approach concludes in the using of FTM relevant technique and in significant reducing of adders on the final step of multiplication. The propose technique leads up to 20% advantage in multiplication for monolithic blocks, and up to 3% for multiplication from 8 to 32 input operands comparing with Synopsys analogues.

The results proposed in this paper are limited with $32 \times 32 \rightarrow 64$ bit range. We have conjecture that implementation of the proposed multiplication technique will lead to more preferable difference for more wide bit ranges, i.e. $64 \times 64$, $128 \times 128$, and $256 \times 256$.

8 Acknowledgements

The research was supported by the European Commission Erasmus Mundus MID. The author is very grateful to Luca Benini and Micrel Lab for their help and support during the project. Thanks also to Paul Leonczyk and Petr Bibilo for cooperating in the conducted experiments.

References

[1] A. Karatsuba, Yu. Ofman: Multiplication of many-digital numbers by automatic computers, in Proceedings of the USSR Academy of Science, 1962, Vol. 145, No. 2, pp. 293-294, (in Russian).
[2] A. Schonhage, V. Strassen: Schnelle Multiplikation großer Zahlen, in: Computing 7 (1971), pp. 281-292.
[3] P. Gaudry, A. Kruppa, P. Zimmermann: A GMP-based Implementation of Schonhage-Strassens Large Integer Multiplication Algorithm, in: Proceedings of the 2007 International Symposium on Symbolic and Algebraic Computation (ISSAC07), Waterloo, Ontario, Canada, pp.167-174, (2007).
[4] https://embedded.eecs.berkeley.edu/pubs/downloads/espresso/index.htm
[5] P.Bibilo, L.Cheremisinova, S.Kardash, N.Kirienko, V.Romanov, D.Cheremisinov: Automatizations of the logic synthesis of CMOS circuits with low power consumption: Programmaia ingeniria, 2013, Vol.8, pp. 35-41, (in Russian).