Analog multiplier design with CMOS-memristor circuits

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Abstract—CMOS-transistors circuits have been used as a conventional approach for designing an analog multiplier in modern era of industrial electronics. However, previous studies have shown, that based on the working region of transistors, such as saturation or weak inversion regions, the circuit may face issues with output ranges and accuracy. One possible solution to that problem could be choosing CMOS-memristors as a basis for the circuit. Although memristor research is still a growing and promising field, one could argue that its implementation could bring many benefits such as increased circuit density and superior computation speeds, etc. Additionally, the era of Moore’s Law of downscaling the size of transistors is to eventually come to an end. No one knows whether the end of a scaling paradigm is to happen within the next five or twenty years. Hence, the research on this particular subject is quite important. This paper proposes an analog multiplier design with CMOS and memristive components. Mainly, the aim of the paper is to compare the power consumption and overall characteristic of the multiplier such as the accuracy and the output range to that of the conventional multiplier. The designed circuit is expected to be suitable for low power applications, and it is built using 18um CMOS technology. The circuit simulations will be conducted using SPICE software. Finally, the effects of channel modulation and temperature on the multiplier performance will be discussed.

Index Terms—Multiplier circuit; signal processing; modulation; CMOS memristors; low power.

I. INTRODUCTION

The analog multiplier is difficult to design due to the complexity of the multiplication circuits. Therefore, the analog multiplier tend to be large in terms of on-chip area and consume a large amount of power. We proposed to used memristive components to solve these issues, as memristors have been proven to be efficient for various architectures [11], [2], [3], [4], [5], [6], [7], [8], [9], [10].

In this paper, we test the performance of an analog multiplier with CMOS-memristive components. The original amplification circuit is designed using 0.18 um TSMC level 49 (BSIM3v3) CMOS technology. We will replace the transistors in saturation mode which are acting as resistors with memristors and analyze the performance. The simulation tests such as DC transfer characteristics and amplitude modulation tests are shown.

II. BACKGROUND

First of all, in order to proceed with the research paper, it is essential to understand what the topic is all about, i.e. what is the analog multiplier, and what are its applications. Therefore, I am providing a short literature review on this electronic device.

A. Analog multiplier

1) What is analog multiplier: Analog multiplier is essentially an electronic circuit which can take the product of two analog signals [11]. In addition, besides being able to produce the output for multiplication of two signals, it has a rich application variety such as analog divider, signal squaring and square root computation, frequency modulation (FM radio), etc [12].

Depending on the complexity of the multiplier circuit, its operating range may be restricted to two-quadrants. This type of multiplier is known as two-quadrant multiplier. However, since these limitations are severe for many analog signal processing applications, utilization of two-quadrant multipliers are rather unpractical [13].

Fortunately, we can also have four-quadrant multipliers which are evidently most practical in industrial electronics. The basis for most integrated circuit multiplier systems is the Gilbert multiplier cell (Fig. 1.) [14]. Which is apparently a minor modification of two-quadrant circuit [15].

2) Applications of analog multiplier: As it was briefly mentioned above, the device can have a variety of applications in analog signal processing and communication systems, because nonlinear operations on analog signals are vital in these fields of industrial electronics. For example, the list of applications of analog multipliers could be illustrated as shown below [16].

(a) Instrumentation
• Wattmeters
• Watt-hour meter
• Flowmeter

(b) Signal generators and filters
• Wien-bridge oscillator

Fig. 1: Gilbert multiplier cell.
• Low-distortion oscillator
• Voltage-controlled low-pass filter
(c) Multiplier applications
• Deviation
• Frequency doubling
• Bridge linearization

B. Memristor

1) How does it work: The term memristor was initially coined by circuit therapist Leon Chua in 1971. Chua has envisioned it as the missing fundamental circuit element which linked the electric charge with magnetic flux \[17\]. The conceptual symmetries of fundamental circuit elements that can be seen in Fig. 2, is often used in order to clearly illustrate why memristor is considered as the missing element.

Fig. 2: Symmetries of fundamental elements.

The main purpose of memristor is to be able to change the value of its resistance, hence act as a switch \[18\]. Through the years of research on this topic, some studies proposed that this property could be achieved by changing the dimensions of a memristor, thus changing its resistance in the order of thousands.

The reason why it is important is because memristors are very small in size, and can be effectively implemented in the digital memory circuits, such as crossbar arrays (see Fig. 3) \[19\].

2) Simulation of circuit with memristor: In this part of the report, the memristor model provided in the e-mail was simulated.

(a) Circuit schematics

The schematics of the simulation is shown in Fig. 4.

(b) Hysteresis loop

The hysteresis loop and the change in resistance value can be seen in the Fig. 5.

The hysteresis loop of -I(V1) vs V(n001) shown in Fig. 6, does not follow its path as the input voltage varies from -1.2 V to 1.2 V. Hence, the value of resistance of memristor can be changed by changing the input voltage V1. Also, another thing to note from the hysteresis loop, is that the device remembers its most recent value of resistance. In other words, it is indeed following the theoretical expectations and acting as memristor.

Fig. 3: Memristor crossbar array.

Fig. 4: Memristor simulation schematic.

Fig. 5: Hysteresis loop.

III. METHODOLOGY

The main principle of this circuit is that it works based on the square-difference identity as:

\[(x + y)^2 - (x - y)^2 = 4xy\]

Where x+y is input 1, and x-y is input 2. In other words, Vin1 = Vx+Vy and Vin2 = Vx-Vy.

The Gilbert cell is used in order to perform the squaring and canceling the extra terms.

IV. SIMULATION RESULTS

This paper includes the preliminary simulation results based on the already provided research papers (multiplier 4). The aim of these simulations is to be able to recreate the circuit provided in the paper by replacing CMOS transistors with 18um CMOS technology or memristors. After doing so, we will be able to determine the performance of the modified circuit in comparison to the original one. Based on the
performance of the new circuit, it will be decided whether it requires any further modifications in the foreseeable future.

All simulations are done using LTspice XVII software.

A. Performance with 0.18 µm CMOS technology

The simulations are performed by utilizing the 0.18 µm CMOS transistors in the circuit provided in the multiplier 4 paper. The width and length values were taken as .27 μm and .18 μm for all transistors. These values were taken from the TSMC level 49 (BSIM3v3) 0.18 μm CMOS technology. The redrawn version of the circuit can be seen below.

Fig. 6: Proposed four-quadrant multiplier circuit.

1) Amplitude modulation performance: From Fig. 6, it can be seen that two AC voltage sources are connected to each input. These input sources represent 500 kHz carrier sinusoid and 50 kHz modulating signal with 400 mV amplitude. Hence, by multiplying these two signals, the circuit should perform as an amplitude modulator. It can be seen that for each input there are two AC sources connected in series. These are Vin1 = Vx + Vy, and Vin2 = Vx - Vy, where Vx is carrier and Vy is the modulating signal. In addition, the supply voltage Vdd is set to 1.8 V as it was done in the paper, also the bias voltage for the P-channel transistors M17 and M18 is set -0.2 V, since their threshold voltage is equal to -0.54 V for their provided W/L ratio of 0.27/0.18.

Additionally, NMOS and PMOS transistors shown in the Fig. 6, are modeled using the TSMC level 49 (BSIM3v3) 0.18 um parameters, which contains the configurations of a real 0.18 µm CMOS technology. The same BSIM3v3 model was used in the original paper (multiplier4).

The simulation results for the case of an amplitude modulator are provided in Fig. 7.

![Fig. 7: Carrier sinusoid and modulating signal.](image)

2) DC transfer characteristics: DC transfer characteristics were obtained by keeping Vy constant, and sweeping Vx from -400 mV to 400 mV, and then observing the output.

As it can be seen from Fig. 8, the characteristics are not quite linear, hence the performance is not perfect.

![Fig. 8: DC transfer characteristics.](image)

3) THD Analysis: The total harmonic distortion analysis was performed by keeping Vx constant 100 mV, and Vy as a sinusoid with the frequency of 100 kHz and 1 MHz. In addition, for each frequency (100 kHz and 100 MHz) we need to vary the peak-to-peak value of a sinusoid, which is in this case chosen to be from 0.2 to 1.2 Volts. The value of THD in percentage was calculated by LTSpice with the code: "four 100kHz V(+vout,-vout)". To see the value of THD, we need to go to View -¿ SPICE Error Log. By default it takes 9 harmonics, which should be enough, but it can also be changed...
by specifying it in the code. The obtained result can be seen in Fig. 9.

4) Width and Length parameters: Initial W/L parameters for each transistor is given in Table 1 below. There are 3 standard W/L ratios for TSMC level 49 (BSIM3v3) 0.18u CMOS transistors. They are: minimum (.18/.27), wide (.18/.20), and large (50/50). As it can be seen from the table, values are taken as the standard W/L ratio for a minimum sized BSIM3v3 transistor.

| #  | Width | Length |
|----|-------|--------|
| M1 | 18u   | 27u    |
| M2 | 18u   | 27u    |
| M3 | 18u   | 27u    |
| M4 | 18u   | 27u    |
| M5 | 18u   | 27u    |
| M6 | 18u   | 27u    |
| M7 | 18u   | 27u    |
| M8 | 18u   | 27u    |
| M9 | 18u   | 27u    |
| M10| 18u   | 27u    |
| M11| 18u   | 27u    |
| M12| 18u   | 27u    |
| M13| 18u   | 27u    |
| M14| 18u   | 27u    |
| M15| 18u   | 27u    |
| M16| 18u   | 27u    |
| M17| 18u   | 27u    |
| M18| 18u   | 27u    |

5) Power Analysis: Figures below illustrate the power waveform of each transistor while the circuit is performing as an amplitude modulator.

By observing the mean and RMS values for each transistor, it was found that transistors M13 and M15 consume the most power within the given time interval. Mean values for M13 and M15 are 77.302W and 77.283W respectively.

Fig. 9: Total Harmonic Distortion of output.

![Fig. 9: Total Harmonic Distortion of output.](image)

Fig. 10: Power waveform of transistors M1-4.

Fig. 11: Power waveform of transistors M5-8.

Fig. 12: Power waveform of transistors M9-12.

Fig. 13: Power waveform of transistors M13-16.

B. Performance when replaced CMOS transistors that act as the resistors in the circuit with the memristors

Since both P-channel transistors M17 and M18 are biased and act as a resistors R, we can replace them with memristors. Fig.15 illustrated the circuit schematic with memristors.

1) Amplitude modulation: The performance as an amplitude modulator is illustrated in Fig.16.
Fig. 14: Power waveform of transistors M17-18.

Fig. 15: CMOS-memristive circuit.

Fig. 16: Amplitude modulation with memristors.

Fig. 17: DC transfer with memristors.

V. Discussion

It was found that the circuit with memristors performs worse in comparison to the original circuit with transistors. Both performance tests: amplitude modulation, and dc transfer characteristics lead to this conclusion.

Also, the dc transfer characteristics shown in Fig. 8 indicate that the output is not perfectly linear.

In addition, it was found that the output range of the circuit is about -25 to 25 mV, while the input range is -400 to 400 mV.

VI. Conclusion

In this paper we tested the analog multiplier circuit’s performance when replacing some transistors with memristors. Hence, by building a CMOS-memristive circuit. It was found that the performance abruptly degrades, since both tests such as amplitude modulation and dc transfer characteristics have shown poor results. On the other hand the original circuit with CMOS transistors performs well, but with the output range limitations of 24 mV. Changing the model for transistors or choosing a different W/L ratio might help to solve this problem.

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