Simulation and investigations on semiconductor materials and devices with surround gate geometry for high performance and low power nano scale applications

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Abstract. All The device with surround gate geometry provides a better way to scale down the dimensions and optimization of power and performance for nano scale applications. The superior gate control can be obtained by novel materials and innovative techniques for various regions of the nano scale device. The surround gate (SG) field effect transistor provides high gain, high trans-conductance, reduced short channel effects and conditions for scaling the technology to sub nano scale. The device has been modeled using SILCAVO Atlas3d and DevEdit3D module also used for creating the device structure with integration of multiple layers of different materials. In this paper, surround gate device input (I_D-V_GS) and output (I_D-V_DS) characteristics have been intensively studied and parameters including I_ON/I_OFF ratio, DIBL, sub threshold slope extracted and compared with the conventional devices. The silicon nanowire field effect transistor (SiNWFET) with surround gate geometry at 0.6 V applied between source and drain exhibits threshold voltage (V_TH) 0.204 V, drain induced barrier lowering (DIBL) 172 mV/V, sub-threshold swing (SS) 104.23 mV/dec, I_ON=440.1 µA, I_OFF=1.04 µA and I_ON/I_OFF ratio 4.24e+02. The results demonstrate improvement in device parameters for the SiNWFET device as compared to other conventional MOSFETs. The results obtained for SiNWFET are also compared with FinFET and CNTFET devices. This research also investigates the integration of alternate channel, dielectric and gate materials into novel GAA device structure.

Keywords: Surround gate, SiNWFET, SILVACO, Atlas3d, and DevEdit3D.

1. Introduction
The number of transistors is doubling every two years to keep Moore’s law alive for more than five decades. The most of the devices using conventional technology have reached its fundamental limit of scaling. So, it is the requirement of time to look for alternate techniques and novel materials for modern semiconductor industry for various applications [1].

1.1 Various challenges in scaling
In nano scale devices major scaling challenges are device dimensions, area and supply voltage for low power device applications. The various short channel effects like SS, DIBL, velocity saturation, gate tunnelling etc. degrades the device performance and are the brick wall in scaling the devices [2-3]. The non-planner FinFET devices at sub nano meter scale also have various problems associated with the controlling gate electrostatics which requires novel materials and device structures for optimum system performance.
1.2 Possible solutions to potentially tackle scaling challenges
The various scaling challenges can be targeted by introduction of novel materials, device geometry and other innovative techniques as discussed in later section.

1.2.1 Handling device gate and channel issues
In MOSFETs gate is the controlling terminal responsible for flow of charge carriers between source and drain terminals of the device [4]. The device performance and power can be optimized by reducing the contact resistance by introduction of novel materials, wrap all around gate and source/ drain contacts, reduced device parasitic. The novel devices such as Silicon nanowire field-effect transistors (SiNWFETs) and CNTFETs are getting attention for future semiconductor technology [5-6].

1.2.2 Interface properties and contact resistance
The electrical properties, good interface with gate oxides and it’s compatibility with silicon processing has made polysilicon better choice for the gate electrode for last three decades. Ideally, polysilicon as gate material with silicon substrate have zero work function difference gives advantage for conventional MOSFETs. However, at the sub nano scale level polysilicon have various problems including poly-depletion, poly diffusion and high leakage current which triggers to shift from polysilicon to other alternate materials as gate and contact materials [7].

The GAA CNTFET parasitic resistances are of two types: 1) contact resistance of CNT with metal ($R_c$) and 2) the resistance due to contact extensions (Source/Drain) ($R_{ext}$) resistance. The contact resistance can be given as [8]:

$$R_c = \frac{R_Q}{2} \left( 1 + \frac{4}{\lambda_c R_Q} \coth \left( \frac{L_c}{L_T} \right) - 1 \right)$$  \hspace{1cm} (1)

Where $R_Q$ is quantum resistance ($R_Q = h/4q^2$) which have typical value 6.5kΩ (approx.), $\lambda_c$ is mean free path (MFP) of carriers in the carbon nanotube, and $g_c$ is carbon nanotube and contact metal coupling conductance, $L_c$ is the contact length and $L_T$ is the length of current transfer.

The resistance associated with extension of contacts can be calculated as [9]:

$$R_{ext} = \frac{1}{S} - R_Q$$  \hspace{1cm} (2)

where $S$ is carbon nanotube conductance which also includes the resistance of contacts.

In modern semiconductor technology as the transistor density increases the number of contacts and hence the contact resistance also increases which may degrade the device performance and have to be optimize to meet the scaling targets [10].

1.2.3 Gate oxide thickness and EOT
The thickness of gate oxide plays a crucial role while determining the gate leakage current of device, and thinner oxides leads to more leakage due to gate tunneling [11]. Further, as the device scaling continues, the oxide thickness goes on decreasing and the conventionally used silicon dioxide ($SiO_2$) is not enough to handle the problem associated with the scaling, and we have to look for other dielectric materials to meet the device scaling requirement. The equivalent oxide thickness (EOT) is thus given as [12]:

$$EOT = \left( \frac{\kappa_{SiO_2}}{\kappa_{high,\kappa}} \right) \times t_{high,\kappa}$$  \hspace{1cm} (3)

where $\kappa_{SiO_2} = 3.9$ is dielectric constant of $SiO_2$, $\kappa_{high,\kappa}$ and $t_{high,\kappa}$ are dielectric constant and thickness of high-$\kappa$ material under consideration. A high-$\kappa$ material can be made many times thicker than silicon dioxide which helps to reduce the leakage of charge carriers across the dielectric, while maintaining the same capacitance.
The sub-threshold swing of a FET device can be defined as the amount of change in input voltage needed to change the sub-threshold output current by one decade which is given as [13]:

$$SS = \left( \frac{dV_{GS}}{d(\log_{10}I_D)} \right)$$  

(4)

Where $V_{GS}$ is gate-source voltage and $I_D$ is drain current. Further, increased in $SS$ indicates the poor gate control which may be due to various quantum phenomenon occurring at nano scale device dimensions [14].

Device Modeling and Simulation

The research investigates GAA-MOSFETs and Si-nanowire FETs and finally the comparison with FinFET and CNTFETs.

2. Investigations on different materials

In this research different materials have been used to model, simulate and then to investigate their combination and compatibility with other metallic, insulating and transistor forming materials for conventional MOSFETs and novel SiNWET structures for various applications.

The High_K gate dielectric materials have been to overcome gate tunnelling through the dielectric layer and to enhance the performance of SiNWETs [15]. The intensive investigation has been carried out on different material including polysilicon, aluminium (Al) and aluminium alloys for gate and source/drain contacts for nano scale device applications.
Table 1. Device gate and source/drain contact materials used in Nano scale device structures

| Materials       | Work Function | Melting point($\varphi_m$) | Density ($\rho$) |
|-----------------|---------------|---------------------------|-----------------|
| Poly-Silicon    | 4.15eV        | 1414°C                    | 2330kg/m$^3$    |
| Aluminium       | 4.26eV        | 660°C                     | 2710 kg/m$^3$   |

Table 2. Device gate dielectric materials used in Nano scale device structures

| Materials                             | Dielectric constant ($\kappa$) | Bandgap (Eg) | Melting point($\varphi_m$) |
|---------------------------------------|--------------------------------|--------------|---------------------------|
| Silicon dioxide ($\text{SiO}_2$)      | 3.9                            | 8.9eV        | 1710°C                    |
| Hafnium oxide ($\text{HfO}_2$)        | 25                             | 5.78eV       | 2758°C                    |
| Aluminium dioxide ($\text{Al}_2\text{O}_3$) | 9                             | 8.8eV        | 2072°C                    |

3. The MOSFET and Silicon nanowire FET (SiNWFET)

The MOSFETs have been the key element for the CMOS technology for three decades. Both the NMOS and PMOS used in CMOS are the voltage controlled devices with high gain and transconductance which better suited for the semiconductor industry [16-17]. Fig. 2 illustrates a gate all around metal oxide semiconductor field effect transistor modelled by Silvaco DevEdit 3D tool, which utilizes bulk silicon as a channel with complete encirclement using polysilicon gate, hafnium dioxide ($\text{HfO}_2$) as gate dielectric and aluminium as source and drain contacts. For MOSFETs we have created a structure using SILVACO DevEDIT3D module using various layers in which silicon as a channel, hafnium dioxide ($\text{HfO}_2$) as gate dielectric surround the channel, aluminium as source/drain contact and polysilicon as gate material as shown in Fig. 2.
Fig. 2 Square geometry GAA-MOSFET design using Silvaco TCAD DevEDIT 3D, with Silicon as channel, HfO$_2$ as gate dielectric material, Polysilicon for gate and aluminum for source/drain contacts, (a) GAA-MOSFET device geometry (b) various regions of the GAA device. The Si-nanowire FET use a thin wire of silicon between source and drain terminal which acts as a channel responsible for current conduction. The Silicon nanowire field effect transistors (SiNWFETs) can effectively suppress the off-leakage current and providing high on current with gate around geometry and has been good alternative device geometry for nano scale CMOS devices [18,19,28]. The conduction in silicon nanowire is high because many conduction sub-bands contribute to the conduction as the gate voltage increase [20,29]. The structure of SiNWFET is depicted in Fig. 3.

Fig. 3 Cylindrical ($\Theta=360^\circ$) GAA SiNWFET designed using Silvaco TCAD ATLAS 3D, Al$_2$O$_3$ as gate dielectric material, aluminum alloy as contact material and CNT as channel, (a) GAA SiNWFET device structure (b) Various regions of the GAA device.
4. Results analysis and discussion

This research investigates the different materials including polysilicon, aluminum (Al) and aluminum alloy for gate and source/drain contacts and high-k materials such as Al₂O₃ and HfO₂ for gate dielectrics and their combinations to be used in MOSFETs and SiNWFTs for nano scale applications.

4.1 The current-voltage characteristics of different devices

The modeled device using Silvaco TCAD has been investigated via I-V characteristics. The input (I_D-V_GS) and output (I_D-V_DS) curves of GAA-MOSFET device in Fig. 2, are depicted in Fig. 4. The device input (I-V) shows that there is almost negligible increase in drain current up to V_GS=0.45V and then there is increase in current with further increase in V_GS to maximum value i.e. V_DS=0.6V. The device operating at 0.6V gives drain current 1.4e-05A, shows better performance over conventional MOSFETs.

Fig.4 The current-voltage IN-OUT characteristics of GAA MOSFET device. (a) The device input(I-V) characteristics (I_D vs V_GS) at V_DS= 0.6 V (b) Output characteristics I_D versus V_DS at different gate voltages (V_GS); bs2108_1=0.2 V, bs2108_2=0.3V, bs2108_3=0.4V, bs2108_4=0.6V, V_DS= (0 – 0.6 V).

The input (I_D-V_GS) and output (I_D-V_DS) characteristics of gate all around Si-nanowire FET device are illustrated in Fig. 5. The device operating at 0.6V gives drain current 4.5e-04A, shows better performance over conventional MOSFETs. The comparative power and performance measures of the Si-nanowire device with different alternative materials are illustrated in Table 3. The device with aluminum oxide as gate dielectric shows the better device performance as compare to silicon dioxide as a gate dielectric material.
Fig. 5 The current-voltage IN-OUT of GAA SiNWFET device. (a) The device input (I-V) characteristics ($I_D$ vs $V_{GS}$) at $V_{DS}$= 0.6 V (b) Logrithmic: Input characteristics log $I_D$ versus $V_{GS}$ at $V_{DS}$= 0.6 V (c) The device output characteristics ($I_D$ vs $V_{DS}$) at different gate volates ($V_{GS}$): SiNW_1_1=0.2 V, SiNW_1_2=0.3V, SiNW_1_3=0.4V, SiNW_1_4=0.6V, $V_{DS}$= (0 – 0.6 V) (d) Logrithmic: log $I_D$ vs $V_{DS}$ Output characteristics ($I_D$-$V_{DS}$) at different gate volates ($V_{GS}$): SiNW_1_1=0.2 V, SiNW_1_2=0.3V, SiNW_1_3=0.4V, SiNW_1_4=0.6V, $V_{DS}$= (0 – 0.6 V).

Table 3. Results obtained in Silicon Nano wire Field Effect Transistor (SiNWFET) with different materials

| Parameters                              | SiO$_2$       | Al$_2$O$_3$     |
|-----------------------------------------|---------------|-----------------|
| Drain-Source voltage ($V_{DS}$)         | 0.6 V         | 0.6 V           |
| Threshold voltage ($V_{TH}$)            | 0.163 V       | 0.204 V         |
| Drain-induced-barrier-lowering (DIBL)   | 172mV/V       | 172mV/V         |
| Sub-threshold-Swing (SS)                | 204 mV/dec    | 104.23 mV/dec   |
| On-state current ($I_{ON}$)             | 116.5 µA      | 440.1 µA        |
| Off-state current ($I_{OFF}$)           | 2.955E-06 A   | 1.04 µA         |
| $I_{ON}/I_{OFF}$ ratio                  | 3.94e+01      | 4.24e+02        |
The various modelled and simulated devices and their performance parameters are summarized in Table 4. The results of this research has also been compared with the literature of modeling, simulation and fabrication. The different parameters point that the devices with GAA geometry are good alternative to meet various scaling, power and performance optimization targets of semiconductor industry.

Table 4. The results comparison of various parameters of Silicon nanowire FET, FinFET and CNTFET

| Device Parameters                  | GAA SiNW-FET [This work] | FinFET [Ref.] | GAA SiNW-FET [Ref.] | GAA CNTFET [Ref.] |
|-----------------------------------|--------------------------|---------------|---------------------|-------------------|
| Drain-Source voltage (V_{DS})     | 0.6 V                    | 0.75 V [26]   | 1.0 V [19]          | 0.75 V [26,29]    |
| Threshold voltage (V_{TH})        | 0.204 V                  | 0.27 V [26]   | 0.2 V [19]          | 0.25 V [27,29]    |
| Sub-threshold-Swing (SS)          | 104.23 mV/dec            | 79 mV/dec [26]| 65 mV/dec [19]      | 67 mV/dec [26,29], 95 mV/dec [27] |
| I_{ON}/I_{OFF} ratio              | 4.24e+02                 | 2.5e+03 [26], 4.24e+05 [25] | 1e+06 [19]          | 1.6e+04 [26], 2.27e+06 [25,29] |

5. Conclusion
In the gate all around (GAA) structures, the gate material completely surrounds the device channel region and give even better control than the FinFET devices. Among the high-k materials HfO2 and Al2O3 have been identified to be most appropriate for the surround gate MOSFETs and Silicon nanowire FETs due to their high dielectric constant and wide band gap which further reduces the subthreshold current and leakage to enhance the performance at low power. The semiconductor devices using these materials exhibit better I_{ON}/I_{OFF} ratio, increased threshold voltage and low Subthreshold-swing which enhance the device performance. The GAA-SiNW FET device at V_{DD} 0.6 V exhibits V_{TH} 0.204 V, SS 104.23 mV/dec, DIBL 172 mV/V and I_{ON}/I_{OFF} ratio 4.24e+02. The proposed Si-nanowire FET with surround gate geometry device better suited for high performance miniaturized applications.

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