High efficiency interleaved bi-directional ZVS DC-DC converter

M Zafarullah Khan¹, M Mohsin Naveed¹ and D M Akbar Hussain²
¹ Institute of Industrial Control Systems, P.O Box, 1398, Rawalpindi, Pakistan
² Department of Energy Technology Aalborg University, Denmark

E-mail: mohssinnaveed30@gmail.com

Abstract. A high efficiency interleaved bi-directional ZVS DC-DC converter is presented in this paper. This converter can be operated in both buck and boost mode. CoolMOS is used as a power device to achieve low conduction losses and fast turn off. The value of inductance is selected such that the CoolMOS drain-to-source voltage always falls to zero before it turns on and ZVS is achieved. Multiphase interleaved inductors are used to achieve high power and low ripple currents. Converter is operated at 50kHz and MATLAB Simulink simulation is performed. 6kW prototype converter is implemented in buck mode and simulation results are verified.

1. Introduction

Bi-directional dc-dc converter is being used in many power applications like hybrid electric vehicle (HEV)[1], satellite[2], UPS, renewable energy systems[3] etc. In UPS, a bi-directional dc-dc converter acts as a dc link between low voltage battery source and high voltage dc bus of an inverter. Bi-directional power flows from the high voltage dc bus to low voltage battery when the battery is being charged and from low voltage battery to high voltage dc bus when the battery is supplying power. In renewable energy systems, a bi-directional dc-dc converter is used as a voltage regulator when the power is being transferred to high voltage dc bus while charging the capacitive energy source when the power is being transferred from high voltage dc bus to low voltage side. In HEV, bi-directional power flows from low voltage battery to high voltage dc bus during acceleration and from high voltage dc bus to low voltage battery during regenerative braking. A non-isolated high efficiency interleaved bi-directional zero voltage switching (ZVS) DC-DC converter is shown in Figure 1. The main advantages of this converter are high power density, high efficiency, low switching losses due to ZVS, low conduction losses due to interleaving of phase-leg currents and CoolMOS utilization, and low output voltage ripple due to coupled inductor.
In this paper, design, simulation and implementation of a non-isolated high efficiency interleaved bi-directional ZVS DC-DC converter is realized. Simulation of the converter operation in buck mode is presented and then results obtained are verified experimentally.

2. Design of high efficiency interleaved bi-directional ZVS DC-DC converter

2.1 Power topology

The power topology of high efficiency interleaved bi-directional ZVS DC-DC converter utilizes CoolMOS as the power device. CoolMOS has distinct benefits over other power devices like MOSFET and IGBT [4]. There is no tail current in CoolMOS as compared to IGBT hence it has fast turn off time. Whereas high voltage MOSFET has a problem of high on state resistance resulting in increased conduction losses. CoolMOS has low on state resistance at high voltage compared to MOSFET resulting in low conduction losses in forward conduction period as well as reverse conduction period of synchronous rectification hence high efficiency. The inductors of phase A and B are coupled [5, 6] together and represented by \(L_{12}\). The inductors of phase C and D are also coupled together and represented by \(L_{34}\). \(C_{\text{low}}\) and \(C_{\text{high}}\) serve as the smoothing capacitors. Interleaved inductors are used to minimize the ripple current flowing through \(C_{\text{low}}\).

2.2 Complementary gating signals

Figure 2 shows the gating signals of all the power devices of high efficiency interleaved bi-directional ZVS DC-DC converter with duty cycle defined in buck mode. Phase B is 180° phase shifted with respect to phase A, phase C is 90° phase shifted with respect to phase A and phase D is 270° phase shifted with respect to phase A. Each phase connected to the same coupled inductor is 180° phase shifted. Complementary PWM is applied to the power devices of same half - bridge leg.
Figure 2. Gating signals of high efficiency interleaved bi-directional ZVS DC-DC converter with duty cycle defined in buck mode.

Figure 3 shows the gating signals with dead time of phase A power devices and current through the inductor connected to phase A. The inductor current varies from positive value to zero and further goes negative to achieve ZVS.
When the power device SW1 is turned on, power flows from the high voltage side to low voltage side and inductor current starts rising. During the dead time $t_d$, inductor current charges the drain to source capacitance ($C_{ds}$) of the SW1 and discharges the $C_{ds}$ of SW5. Then the current starts decaying through the DW5, integrated diode of SW5 and SW5 turns on in ZVS condition as the DW5 diode is freewheeling. When the current reaches zero, negative current flows through SW5 and DW5 is naturally turned off without reverse recovery loss. This negative current of SW5 charges the $C_{ds}$ of SW5 and discharges the $C_{ds}$ of SW1. After the complete discharge of $C_{ds}$ of SW1, the drain to source voltage $V_{ds}$ across the switch falls to zero and SW1 turns on in ZVS condition. ZVS operation of the devices results in zero turn on losses and high frequency converter can be easily implemented with reduced inductor size. When the power flows from low voltage side to high voltage side, the converter is operating in "boost mode". When power flows from high voltage side to low voltage side, the converter is operating in "buck mode".
2.3 Coupled inductor design to achieve ZVS

To minimize the output voltage and current ripples, the inductance need to be large enough but with large inductance converter operates in continuous conduction mode (CCM) and transient response is slow. To improve the transient response, small value of inductance should be used but this will increase the ripple content in output voltage and converter will operate in discontinuous conduction mode (DCM). It will impose stress on the output capacitor and large output capacitor will be required to filter out these ripples. In order to achieve ZVS, the converter should be operated further into synchronous conduction mode which requires the flow of negative current as shown in Figure 3. As in synchronous conduction mode, ripple current is further increased, multichannel interleaving is used to reduce this ripple current. Due to small value of inductance required in this converter, the size of the magnetic components is very small. Physical structure of two EE type magnetically coupled inductors is shown in Figure 4(a) and Figure 4(b). The coupling coefficient is close to 0 in Figure 4(a) and between 0 and 1 in Figure 4(b). Air gap is required in the coupled inductors of Figure 4(a) and Figure 4(b) to avoid saturation of the inductors.

![Figure 4. Physical structure of magnetically coupled inductors. (a) Non-coupling. (b) Loosely coupling.](image)

The type of inductor shown in Figure 4(a) has certain drawbacks compared to the inductor shown in Figure 4(b). The cores are in contact at center limb and there is gap in side limbs. Gap must be filled with non-magnetic material to ensure mechanical stability. As there is no gap in the center limb, the thickness of spacers used should be precise and equal to the gap length. Moreover, the gap cannot be adjusted to achieve different inductance values. These drawbacks introduce complications in the manufacturing of inductor.

The inductor shown in Figure 4(b) has gap in each limb. The thickness of the spacers required need not to be very precise. The gap can be easily adjusted and different values of inductance can be easily made. This structure is mechanically stable and provides ease in adjustment of required inductance.
The equivalent inductance required in Figure 4(b) is given by Eq (1)

\[ L_{eq} = \frac{L^2 - M^2}{L - \frac{D}{1-D} M} \quad \text{Eq (1)} \]

Where \( L \) is the self inductance of the coupled inductor, \( M \) is the mutual inductance and \( D \) is the duty cycle defined in buck mode.

As the inductor in Figure 4(b) has equal gap in each limb its mutual inductance is given by \( M = L/3 \). Putting this value of \( M \) and required value of \( D \) in Eq (1), the relationship between \( L \) and \( L_{eq} \) can be obtained i.e. for \( D = 0.4 \), \( L_{eq} = 1.14L \). The negative peak of the inductance current \( I_{pk} \) can be obtained by the energy balance between the inductor and \( C_{ds} \) of the power device. It is given in Eq (2)

\[ I_{pk-} = \sqrt{\frac{2C_{ds}V_{high}^2}{L_{eq}}} \quad \text{Eq (2)} \]

Where \( C_{ds} \) is the output capacitance of the CoolMOS, \( V_{high} \) is the high side voltage and \( L_{eq} \) is the equivalent inductance.

The half of the peak-to-peak current \( I_{pk-pk} \) through the inductor equals the average low voltage side current plus \( I_{pk} \), as shown in Eq(3)

\[ \frac{1}{2}I_{pk-pk} = \frac{1}{2}\frac{V_{high} - V_{low}}{L_{eq}}DT_s = \frac{P}{V_{low}} + I_{pk-} \quad \text{Eq(3)} \]

Here \( T_s \) is the switching period and \( P \) is low voltage side power in each phase.

This converter is normally operated at high frequency and it is important to know that at high frequency eddy current losses increases significantly which causes heating of wire. So Litz wire should be used at high frequency to fully utilize the capacity of wire.

2.4 MATLAB Simulink simulation

High efficiency interleaved bi-directional ZVS DC-DC converter has been simulated with Simulink. Self inductance of the coupled inductors is 13uH and switching frequency of the converter is 50kHz. High side voltage is 150V, low side voltage is 60V and low side current is 100A.

Figure 5 shows the drain to source voltage \( V_{ds} \) and gate to source voltage \( V_{gs} \) of SW5. It can be seen that \( V_{ds} \) drops to zero before \( V_{gs} \) goes high resulting in ZVS.
Figure 5. $V_{ds}$ and $V_{gs}$ of SW5 showing ZVS.

Figure 6 shows the individual four inductors currents $i_1$, $i_2$, $i_3$, $i_4$ and total peak-to-peak current $i_{\text{total},pk-pk}$ at point E. Individual phase inductor peak current $i_{pk}$ is 62A, negative peak current $i_{pk}$ is -10A, peak-to-peak current $i_{pk-pk}$ is 72A, total peak-to-peak current $i_{\text{total},pk-pk}$ is 7A and the average current $i_{\text{average}}$ is 96A.
Figure 6. Individual four inductors currents and total current.

Figure 7 shows the gate-to-source voltage $V_{gs}$, drain-to-source voltage $V_{ds}$ and drain-to-source current $I_{ds}$ of SW5. $V_{ds}$ is $150V$ and $I_{ds}$ is $72A_{pk-pk}$. 

$i_{pk} = 62A$

$i_{pk-pk} = 72A$

$i_{pk} = -10A$

$i_{total_{pk-pk}} = 7A$

$i_{average} = 96A$
Figure 7. $V_{gs}$, $V_{ds}$ and $I_{ds}$ of SW5.

Figure 8 shows the high side voltage $V_{high}$, low side voltage $V_{low}$ and output current $I_{dc}$. $V_{high}$ is 150V, $V_{low}$ is 60V and $I_{dc}$ is 100A.
2.5 Experimental verification

6kW prototype of high efficiency interleaved bi-directional ZVS DC-DC converter is implemented using CoolMOS as a power device. Coupled inductors are made using ferrite core with 13μH self inductance. Switching frequency of the converter is 50kHz. High side voltage is 150V, low side voltage is 60V and low side current is 100A. Figure 9 shows the drain to source voltage $V_{ds}$ and gate to source voltage $V_{gs}$ of SW5. It can be seen that $V_{ds}$ drops to zero before $V_{gs}$ goes high resulting in ZVS.
Figure 9. $V_{ds}$ in Ch1 and $V_{gs}$ in Ch2 showing ZVS of SW5.

Figure 10 shows the individual four inductors currents $i_1$, $i_2$, $i_3$, $i_4$ and total peak-to-peak current $i_{total,pk-pk}$ at point E. Individual phase inductor peak current $i_{pk}$ is 62A, negative peak current $i_{pk-}$ is -10A, peak-to-peak current $i_{pk-pk}$ is 72A, total peak-to-peak current $i_{total,pk-pk}$ is 7A and the average current $i_{average}$ is 94A.

Figure 10. Individual four inductors currents and total current.
Figure 11 shows the gate-to-source voltage $V_{gs}$, drain-to-source voltage $V_{ds}$ and drain-to-source current $I_{ds}$ of SW5. $V_{ds}$ is 150V, $I_{ds}$ is 72A pk-pk and $V_{gs}$ is +15V, -5V.

![Figure 11. $V_{gs}$, $V_{ds}$ and $I_{ds}$ of SW5.](image)

Figure 12 shows the high side voltage $V_{high}$, low side voltage $V_{low}$ and output current $I_{dc}$. $V_{high}$ is 150V, $V_{low}$ is 60V and $I_{dc}$ is 100A. Efficiency of the converter is measured to be 98%.

![Figure 12. $V_{high}$, $V_{low}$ and $I_{dc}$.](image)
From all the measurements shown above it can be observed that experimental results clearly verify the simulation results.

3. Conclusions
High efficiency interleaved bi-directional ZVS DC-DC converter is simulated and realized experimentally in this paper. Following distinct features of the converter are discussed.

1. CoolMOS is used as a power device resulting in low conduction losses compared to the MOSFET and fast turn off compared to IGBT mainly due to the absence of tail current.

2. Output capacitance of the CoolMOS is used to achieve ZVS resulting in almost zero turn on loss.

3. Coupled inductors are used to cancel out low voltage side ripples in the center limb resulting in small capacitance and low ripple contents in the output voltage.

4. Four phase interleaved operation is significant for dense power applications with less stress on power devices, low conduction losses and low ripple contents in the output current.

High efficiency interleaved bi-directional ZVS DC-DC converter is designed, simulated and implemented for a 6kW system. Experimental results verified the simulated results. Its efficiency is more than 98% at full load.

References

[1] Lai J S and Nelson D J 2007 Proc. IEEE, vol. 95 766
[2] Dan M Sable, Fred C Lee, and Bo H Cho 1992 Proc. IEEE APEC 614
[3] Khan M Z, Hussain M M, Naveed M M, and Akbar Hussain D M 2012 Proc. IMECS
[4] Zhang J, and Lai J S 2006 Proc. IEEE APEC 19
[5] Jamieson R S 1984 Negative coupled inductors for poly-phase choppers U.S. Patent 4 442 401
[6] Andersen R 1993 H-driver DC-to-DC converter utilizing mutual inductance U.S. Patent 5 204 809