The Reliability Design of Switch Chip Based on THENA Process Stimulation System

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Abstract. This paper mainly focuses on the 2CK6642 silicon switch diode chip, which is mainly used for the surface-mounted packaging device of CLCC-3 metal ceramic. Different from that of ordinary diode, the internal structure of 2CK6642 silicon switch diode has a high resistance region I in the middle of Type P and Type N silicon materials, forming a P-I-N structure. Silvaco TCAD interactive tools, i.e. ATHENA process stimulation system and ATLAS device stimulation system, are used to conduct the design and stimulation of 2CK6642 silicon switch diode chip, so that alternative plugging with external devices could be achieved finally.

1. Introduction

Diodes have many varieties, and are essential and common, just like buttons and zippers in clothing. Diodes have many branches, including DO series and TO series which are most common in dip diode, as well as SMA series, SMB series, SMC series, CD series, SOD series, SOT series, DFN series and QFN series, which are provided with surface-mounted packaging [1-3]. At present, comprehensively considering the price and production conditions, etc. of single wafer and epitaxial wafer, deep junction table surface process is mainly adopted in domestic production, with the less application of shallow junction plane process, which is opposite to that of foreign production. On account of that the front side of the surface-mounted packaging device chip of CLCC-3 metal ceramic must be made of aluminum, and that the reverse side must be made of silicon or gold [4], the structure must be plane process. On account of that such products and chips are still prohibited to be imported to China internationally, corresponding products were not replaced in China until 2010, resulting in that there are no reliable
devices available for domestic high-end equipment. The subject 2CK6642 silicon switch diode chip in this paper is used for surface-mounted packaging device of CLCC-3 metal ceramic.

2. Experiment

Different from that of ordinary diode, the internal structure of 2CK6642 silicon switch diode has a high resistance region I in the middle of Type P and Type N silicon materials, forming a P-I-N structure [5-8]. In this paper, the longitudinal parameter design and longitudinal parameter design theory of the classical plane chip are used for the theoretical calculation. Silvaco TCAD interactive tools, i.e. ATHENA process stimulation system and ATLAS device stimulation system, are used to conduct the design and stimulation of 2CK6642 silicon switch diode chip.

3. Results and discussion

In this study, the requirements of the detailed specification in US military standard MIL-PRF-19500/578K of 1N6642 was referred to for design, so that alternative plugging with external devices could be achieved finally. Main electrical parameters are shown in Table 1.

| Parameter | Conditions | Limits |
|-----------|------------|--------|
| Forward voltage ($V_{FM1}$) | $I_F=10mA$ | ≤0.8V |
| Forward voltage ($V_{FM2}$) | $I_F=100mA$ | ≤1.2V |
| Reverse current ($I_{R1}$) | $V_R=20V$ | ≤25mA |
| Reverse current ($I_{R2}$) | $V_R=75V$ | ≤500nA |
| Breakdown voltage ($V_{BR}$) | $I_R=100\mu A$ | ≥100V |
| Reverse current ($I_{R3}$) | $V_R=20V, T_A=150^\circ C$ | ≤50µA |
| Reverse current ($I_{R4}$) | $V_R=75V, T_A=150^\circ C$ | ≤100µA |
| Forward voltage ($V_{FM3}$) | $I_F=10mA, T_A=150^\circ C$ | ≤0.8V |
| Forward voltage ($V_{FM4}$) | $I_F=100mA, T_A=-55^\circ C$ | ≤1.2V |
| Capacitance ($C_{tot1}$) | $V_R=0V, f=1MHz$ | ≤5pF |
| Capacitance ($C_{tot2}$) | $I_R=1.5V, f=1MHz$ | ≤2.8pF |
| Reverse recovery time ($t_{rr}$) | $I_F=I_R=10mA$ | ≤5ns |

3.1. Longitudinal parameter design

3.1.1. Longitudinal parameter design. The chip is made of N--N+ type monocrystalline silicon material with a high resistance epitaxial layer, and it is developed with a N- high resistance epitaxial layer with certain thickness, with a low-resistance N-type monocrystalline silicon slice characterized by the classic $<111>$ crystal orientation and resistivity of $\Omega \cdot cm$ 0.006 - 0.008 as the substrate.

(a) Determination of epitaxial resistivity $\rho$

For the PN junction of the diffusion plane, abrupt junction approximation is adopted in calculation. According to the maximum breakdown voltage requirement of DC parameters, $V_{BR} \geq 100V$, considering the error between the theoretical value and the actual value, the epitaxial layer with doping concentration of $N_c = 1.7 \sim 1.8 \times 10^{15}$/cm$^3$ is selected.

(b) Selection of epitaxial layer thickness $W$

The epitaxial layer thickness $W$ must ensure that the space charge region of the collector region near the PN junction will not exceed the high-resistance epitaxial region under the maximum counter voltage of the collector junction. In addition, it shall consider anti-diffusion depth (about $X_{jc}$) to the epitaxial layer of diffused junction depth $X_c$ and highly-doped substrate and the thickness $d_a$ (about 1µm) of the epitaxial layer consumed by each generation of SiO$_2$ through oxidation, $W=10\mu m - 11\mu m$. 


3.1.2. Transverse parameter design. According to the requirements of electrical parameters: \( C_{ob} \leq 2.8 \text{pF} \). When calculation, the junction capacity shall be taken as the plate capacitance approximation. The capacitance: \( A \leq 8.3 \times 10^5 \text{µm}^2 \).

3.1.3. Design of the total diffusion perimeter. The minimum length \( L_e \) can be obtained based on the line current density \( I_0 \) along the diffusion perimeter. Through calculation: \( L_e \geq 0.06 \text{cm} \).

3.2. Chip manufacturing process simulation

The breakdown characteristic curve and the reverse recovery time curve are the main characteristic curves for measuring the DC performance of the device. The DC characteristic of devices is closely related to the process parameters, so the process simulation is very important. The design and stimulation conducted by Silvaco TCAD interactive tools, i.e. ATHENA process stimulation system and ATLAS device stimulation system, are adopted for 2CK6642UB chip manufacturing process. The system has efficient and stable multithreading algorithm, which greatly reduces the simulation time while maintaining the accuracy [9-11].

3.2.1. Chip process stimulation. According to the requirements of the process design and device parameters, the file card and program design were conducted in the THENA process simulation system, with the final structure diagram shown in Figure 1. As shown in Figure 1, the structure meets the design requirements of the PN junction depth of 3µm designed.

Activate the electrode, define the grid rules, refine the grid, and complete the transition from Process to Device. The grid is referred herein for the need of physical characteristics simulation of devices. We have set a dense grid in the key area of the device, with the final grid shown in Figure 2:

![Figure 1. Chip simulation structure diagram.](image-url)
3.2.2. Device-level stimulation of chips. The device-level simulation, also known as physical characteristic simulation, is to conduct characteristic-level design in the ATLAS device simulation system, with the final breakdown characteristic curve shown in Figure 3, and the reverse recovery time curve shown in Figure 4.
As shown in Figure 3, the reverse breakdown voltage of the device is 150V, and the reverse electric leakage of the device increases instantly after exceeding 150V. Under the reverse voltage test condition of 20V and 75V required in the specifications, the reverse electric leakage is under 10-12A. By default, the simulation result is the result at direction Y with the thickness of 1μm. The actual electric leakage of the device is less than 2×240×10-12A=4.8nA, meeting the maximum electric leakage of 25nA under 20V and the maximum electric leakage of 500nA under 75V required in the specifications. As shown in Figure 4, the reverse recovery time of the device is (2-0.5) ×10-9s=1.5ns, meeting the design requirement of 5ns.

### 3.3. Test and analysis of chip results

#### Table 2. Initial touch chip test results.

| Parameter | Conditions | Limits | 1   | 2   | 3   | 4   | 5   |
|-----------|------------|--------|-----|-----|-----|-----|-----|
| \(V_{FM1}\) | \(I_F=10mA\) | \(\leq 0.8V\) | 0.708 | 0.708 | 0.706 | 0.707 | 0.708 |
| \(V_{FM2}\) | \(I_F=100mA\) | \(\leq 1.2V\) | 0.894 | 0.894 | 0.891 | 0.892 | 0.892 |
| \(I_{R1}\) | \(V_R=20V\) | \(\leq 25nA\) | 10.61 | 12.11 | 11.54 | 10.85 | 10.92 |
| \(I_{R2}\) | \(V_R=75V\) | \(\leq 500nA\) | 15.41 | 18.32 | 16.03 | 16.07 | 17.03 |
| \(V_{BR}\) | \(I_R=100μA\) | \(\geq 100V\) | 139.5 | 139.0 | 138.8 | 140.2 | 139.0 |
| \(I_{R3}\) | \(V_R=20V,T_A=150℃\) | \(\leq 50μA\) | 22.20 | 19.62 | 20.93 | 22.01 | 21.52 |
| \(I_{R4}\) | \(V_R=75V,T_A=150℃\) | \(\leq 100μA\) | 32.01 | 32.11 | 33.42 | 32.14 | 31.73 |
| \(V_{FM3}\) | \(I_F=10mA,T_A=150℃\) | \(\leq 0.8V\) | 0.490 | 0.490 | 0.490 | 0.492 | 0.494 |
| \(V_{FM4}\) | \(I_F=100mA,T_A=-55℃\) | \(\leq 1.2V\) | 1.002 | 1.005 | 1.009 | 0.999 | 1.000 |
| \(C_{tot1}\) | \(V_R=0V,f=1MHz\) | \(\leq 5pF\) | 0.98 | 0.96 | 0.98 | 0.98 | 0.96 |
| \(C_{tot2}\) | \(V_R=1.5V,f=1MHz\) | \(\leq 2.8pF\) | 0.95 | 0.94 | 0.95 | 0.94 | 0.96 |
| \(t_{rr}\) | \(I_F=I_R=10mA\) | \(\leq 5ns\) | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 |
The chips for the product were manufactured according to the chip parameters and process design. After the test, the parameters and reliability of the product basically meet the requirements of parameter indexes in the agreement. After tested, the product parameters meet the requirements. The test data of 5 products randomly selected are shown in Table 2.

4. Conclusion
The 2CK6642 chips, characterized by epitaxial slice doping concentration of $1.7-1.8 \times 10^{15} \text{cm}^{-3}$, epitaxial layer thickness of $10 \mu\text{m}$-$11 \mu\text{m}$ and epitaxial slice type of N/N+, meet the design requirement. With 2CK6642 chip, the device can achieve the breakdown voltage of 150V, recovery time of 1.5ns and reverse electric leakage within 4.8nA, which meet the design requirements.

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