A C A S E  S T U D Y  O F  L L V M - B A S E D  A N A L Y S I S  F O R  O P T I M I Z I N G  S I M D  C O D E  G E N E R A T I O N

Joseph Huber
Oak Ridge National Laboratory
huberjn@ornl.gov

Weile Wei
Louisiana State University
wei@lsu.edu

Giorgis Georgakoudis
Lawrence Livermore National Laboratory
georgakoudis1@llnl.gov

Johannes Doerfert
Argonne National Laboratory
jdoerfert@anl.gov

Oscar Hernandez
Oak Ridge National Laboratory
oscar@ornl.gov

June 29, 2021

A B S T R A C T

This paper presents a methodology for using LLVM-based tools to tune the DCA++ (dynamical cluster approximation) application that targets the new ARM A64FX processor. The goal is to describe the changes required for the new architecture and generate efficient single instruction/multiple data (SIMD) instructions that target the new Scalable Vector Extension instruction set. During manual tuning, the authors used the LLVM tools to improve code parallelization by using OpenMP SIMD, refactored the code and applied transformation that enabled SIMD optimizations, and ensured that the correct libraries were used to achieve optimal performance. By applying these code changes, code speed was increased by $1.98 \times$ and 78 GFlops were achieved on the A64FX processor. The authors aim to automatize parts of the efforts in the OpenMP Advisor tool, which is built on top of existing and newly introduced LLVM tooling.

K e y w o r d s  O p e n M P  ·  S I M D  ·  c o m p i l e r s  ·  f e e d b a c k  ·  L L V M  ·  H P C  t o o l s

1 Introduction

Program analysis tools are important in helping users understand, improve, and port their applications to new platforms. This is crucial for applications that need tuning and significant code restructuring to exploit new types of hardware devices, such as single instruction/multiple data (SIMD) units and accelerators. Compiler-based tools are crucially important for identifying opportunities to improve application codes as the compiler generates code for different architectures. In particular, the LLVM compiler is an open-source compiler that provides a set of tools for the static analysis and feedback of application code. Static program analysis information can be combined with dynamic information (profile-based) to filter the large amount of information produced by the compiler so that users can focus on the most frequently executed regions of their code.

This paper presents a methodology for using LLVM-based tools to tune an application to generate efficient SIMD instructions that target the new ARM A64FX processor, as well as describes what is required to achieve good performance.

0This manuscript has been co-authored by UT-Battelle, LLC under Contract No. DE-AC05-00OR22725 with the U.S. Department of Energy. The United States Government retains and the publisher, by accepting the article for publication, acknowledges that the United States Government retains a non-exclusive, paid-up, irrevocable, world-wide license to publish or reproduce the published form of this manuscript, or allow others to do so, for United States Government purposes. The Department of Energy will provide public access to these results of federally sponsored research in accordance with the DOE Public Access Plan (http://energy.gov/downloads/doe-public-access-plan).
2 Case Study: Porting DCA++ to Wombat

This section describes the authors’ experiences in porting the DCA++ (dynamical cluster approximation) application to the Wombat cluster, an ARM-based heterogeneous cluster at Oak Ridge National Laboratory. This section presents a methodology for using LLVM-based tools to tune the DCA++ application targeting the ARM A64FX and ThunderX2 processors. The goal is to describe what changes are required for the new architecture and generate efficient SIMD instructions that target the new Scalable Vector Extension (SVE) instruction set available in the A64FX processors based on LLVM-based tools information.

2.1 Evaluation Environment

The case study used the Wombat test bed with 24 compute nodes. Sixteen compute nodes are based on the Fujitsu A64FX processor with SVE and a theoretical peak performance of 3.3792 TFlops. Each A64FX node has one processor socket with 32 GB of second-generation High-Bandwidth Memory (HBM2). The A64FX-equipped nodes do not have additional Double Data Rate (DDR) memory. Eight compute nodes have two ThunderX2 processors with NEON vector instructions and a theoretical peak performance of 560 GFlops. The ThunderX2 nodes have 256 GB of DDR4 RAM and a 480 GB solid-state drive for node-local storage. All nodes are connected with Enhanced Data Rate InfiniBand (100 Gbit/s). The compilers on the system are the ARM 20.3 compilers and the Clang upstream compiler, which is based on Clang 12. The scientific libraries available on Wombat are the ARM Performance Libraries (APL) version 20.3.

2.2 DCA++

Quantum Monte Carlo (QMC) solver applications are popular tools essential to the US Department of Energy-supported scientific software. This paper studies one cutting-edge QMC application called the DCA++ algorithm. DCA++ [1] implements quantum cluster algorithms to solve quantum many-body problems in condensed matter physics. DCA++ is a highly scalable and performant scientific software written in modern C++ and has been ported to various high-performance computing architectures, including IBM Power9, x86_64, ThunderX2, and ARM A64FX [2]. The DCA++ software currently integrates three different programming models—message passing interface (MPI), Compute Unified Device Architecture (CUDA), and High Performance ParalleX (HPX)/C++ threading—together with numerical libraries (e.g., Basic Linear Algebra Subprograms [BLAS], Linear Algebra Package [LAPACK], and MAGMA) to expose the parallel computation structure.

Wei et al. [2] reported that DCA++ with the HPX run time system [3] has produced a 20% run time speedup over the one with C++ standard threading support. The speedup is primarily due to the faster thread context switching and reduced scheduler synchronization overheads in the HPX run time. Moreover, Autonomic Performance Environment for Exascale (APEX) [4] is an in situ profiling and adaptive tuning framework to the HPX run time system that can capture operating system and hardware system performance data through various interfaces, such as Performance Application Programming Interface (PAPI) [5]. Because APEX is highly integrated into the HPX run time, for HPX-supported applications, users can easily capture PAPI counter information (e.g., level 2 data cache misses, vector/SIMD instructions, floating point instructions) through HPX function annotation. The overhead introduced by APEX profiling is as low as ~1% [6] compared with the overall application run time.

In DCA++, the QMC solver is the most computation-intensive unit that models strongly correlated electron systems [2]. Computation on the QMC solver is parallelized by using a multithreading scheme that comprises walker (i.e., producer) and accumulator (i.e., consumer) tasks. Each task runs on an independent thread. There are multiple walkers running concurrently. Each walker is responsible for a Monte Carlo (MC) update (sampling from the Markov chain), and then an accumulator is popped from the head of the accumulator waiting queue to compute an MC measurement from the walker. When each accumulator finishes its accumulation measurement, it is pushed back to the end of the queue. The walker-accumulator synchronization is managed by the synchronization primitives mutex and conditional_variable.

2.3 Baseline Performance

The following experiments compare DCA++‘s performance on Wombat by using its A64FX and ThunderX2 nodes. The performance is measured using 48 accumulators and 48 walkers and using 100,000 measurements, which is a representative scientific simulation case in production. On A64FX, DCA++ is built with two different configuration settings: SVE vectorization and SVE-disabled. The SVE vectorization version of DCA++ means that DCA++ is built with SVE compiler flags enabled and vectorized loops, and it uses the APL optimized for SVE (i.e., LAPACK, BLAS, AP...
|                     | vectorization | walltime (seconds) ± standard deviation | speedup | Gflop/s |
|---------------------|---------------|----------------------------------------|---------|---------|
|                     | no            | 488.42±3.09                            | -       | 17      |
|                    | yes           | 246.98±0.48                            | 1.98    | 78      |
| A64fx              | no            | 1336.61±178.09                         | -       | 14      |
|                    | yes           | 805.53±24.06                           | 1.66    | 27      |
| ThunderX2          | no            | 488.42±3.09                            | -       | 17      |
|                    | yes           | 246.98±0.48                            | 1.98    | 78      |

Figure 1: DCA++ execution time.

Fastest Fourier Transform in the West (FFTW)). The SVE compiler flags are set to “-DNDEBUG -fsimdmath -fopenmp -O3 -mcpu=a64fx” The SVE-disabled version means that DCA++ is built with original DCA++ code and open-source scientific libraries, including Netlib-LAPACK and FFTW. Similarly, on ThunderX2, DCA++ is built with two different configurations: with NEON and NEON disabled.

Figure 1 shows DCA++ execution time on A64FX and ThunderX2 architectures. On A64FX, the SVE vectorization version of DCA++ performs ~2× faster than the SVE-disabled version. On ThunderX2, the NEON version of DCA++ is observed to be ~1.66× faster than the NEON-disabled version. Noticeably, the SVE vectorization version of DCA++ on A64FX has ~3.3× speedup over the NEON version on ThunderX2. Meanwhile, the NEON version on ThunderX2 is measured to have ~27 GFlops, and the SVE vectorization version of DCA++ on A64FX reached ~78 GFlops (~2.8×).

These results show the performance gains of DCA++ due to the peak performance improvements of the A64FX processor (e.g., 500 GFlops for ThunderX2 vs. 2.5 TFlops for A64FX).

Figure 2 shows the breakdown of DCA++ execution time into four categories: application, scientific libraries, HPX run time, and other activities. Each category only considers functions that have more than 1% overhead shown in the final profiling report generated from perf, a Linux built-in performance profiling tool. The application category includes custom modules developed in the DCA++ source code. The HPX run time category represents necessary scheduling and coordination efforts in HPX threads manager. The scientific libraries category captures routines from external numerical libraries, such as BLAS, LAPACK, FFTW, and math routines. The other activities category summarizes all other functions that have less than 1% overhead in the final profiling report.

Several observations were made from the timing breakdown shown in Fig. 2.

1. With SVE vectorization or NEON optimization, the dominant percentage of the overall execution time is shifted from the external scientific libraries to the application source code. For example, on A64FX, the percentage of application time in the SVE-disabled vectorization version of DCA++ is 26%, whereas the percentage of application time in the SVE version is 57%. A similar percentage shift is also observed on ThunderX2 comparisons. In other words, with APL (SVE vectorization on A64FX or NEON optimization on ThunderX2), less time is spent on scientific libraries because APL are particularly optimized on targeting platforms.

2. The HPX run time library imposes minimal overhead to the overall program execution. The overhead is primarily due to a lack of sufficient parallelism from the application so that some HPX worker threads in the kernel level are spinning and waiting for user-level tasks.

Further investigation using hardware performance counters is shown in Fig. 3. Here, hpx::annotated_function() is used to wrap accumulator and walker tasks so that their activities (i.e., timing information and PAPI counters) can be distinguished in the final profiling report generated from the HPX-APEX profiling tool. Figure 3 shows that the total execution time of accumulator and walker takes the majority of the overall program execution time (~93.00% in the SVE-disabled version and ~91.25% in SVE vectorization version). Several observations were made from Fig. 3.

1. The SVE-disabled version of DCA++ on A64FX has nearly ~40× higher VEC_INC, 2× higher TOT_CYC, and 1.2× higher FP_INS than the SVE vectorization version, where VEC_INC is vector/SIMD instructions, TOT_CYC is total cycles, and FP_INS is floating point instructions. The authors noticed that by using the optimized libraries, the application uses less vector and floating point SVE instructions. Because SVE has wider 512 bit width, fewer vector instructions are needed in the computation than NEON, which has 128 bit width. Also, the SVE has a more powerful instruction set that uses fewer instructions for the same operation.

2. The L2_DCM (L2 data cache misses) does not change with the SVE optimized version because the SVE optimization does not impact overall memory access patterns. Access to HBM2 remained constant in both versions.
3. Using SVE vectorization on DCA++ shifts timing percentages between accumulator and walker in overall program execution. To perform efficient matrix-related operations, the implementation of walker extensively uses DGEMM routines, which are provided by the scientific libraries. The timing percentage of walker is 62.15% with the SVE-disabled version of DCA++ in overall program execution and is reduced to 40.14% with the SVE vectorization version. The percentage reduction of walker is similar to the percentage reduction of scientific libraries observed in Fig. 2.

The results show that to further improve the DCA++ application, the focus must be on tuning the application source code, particularly the accumulator code, to determine which loops need further optimization and which were successfully vectorized by the compiler. This requires significant interaction with the LLVM tools to understand the application hot spots and the opportunities for SVE optimizations.

3 An LLVM Tool Methodology to Generate Efficient Vectorization

A64FX performance is highly dependent on how well the source can be mapped to SVE instructions. It is important to determine which application loops are not being vectorized and their impact on the application’s overall performance. The ARM C/C++ compiler is based on the LLVM/Clang compiler, which is also the basis for the authors’ exploration and automation toward vectorizing the most important loops in an application.

Like most modern compilers, LLVM/Clang and its derivatives support profile guided optimization (PGO). The idea is that the compiler inserts profiling instructions into the target binary to collect information when the application is run. During application shutdown, profiling information is stored on the disk for later use. When the application is recompiled in the future, the collected profiling information is used to drive heuristics (e.g., to determine a suitable unroll count for loops). Such profiling also allows the compiler to approximate how much time was spent in a certain portion of code, also referred to as code hotness. The latter makes PGO especially interesting to filter optimization...
| Accumulator | % total | L2_DCM | VEC_INS | TOT_CYC | FP_INS  |
|-------------|---------|--------|---------|---------|---------|
| no SVE      | 30.86   | 9.29E+09 | 6.05E+11 | 1.29E+13 | 2.73E+12 |
| standard deviation | 0.30   | 4.27E+07 | 0.00E+00 | 2.24E+10 | 0.00E+00 |
| SVE vectorization | 51.11   | 9.88E+09 | 6.53E+10 | 1.09E+13 | 2.62E+12 |
| standard deviation | 0.17   | 3.59E+07 | 0.00E+00 | 0.00E+00 | 0.00E+00 |

| Walker | % total | L2_DCM | VEC_INS | TOT_CYC | FP_INS  |
|--------|---------|--------|---------|---------|---------|
| no SVE | 62.15   | 6.15E+10 | 3.99E+12 | 2.61E+13 | 8.37E+11 |
| standard deviation | 0.61   | 2.03E+08 | 0.00E+00 | 4.70E+10 | 0.00E+00 |
| SVE vectorization | 40.14   | 6.27E+10 | 5.05E+10 | 8.56E+12 | 3.45E+11 |
| standard deviation | 0.14   | 1.11E+08 | 0.00E+00 | 8.87E+09 | 0.00E+00 |

| Total (Acc. + Walker) | % total | L2_DCM | VEC_INS | TOT_CYC | FP_INS  |
|-----------------------|---------|--------|---------|---------|---------|
| no SVE                | 93.00   | 7.08E+10 | 4.60E+12 | 3.90E+13 | 3.57E+12 |
| standard deviation     | 0.90    | 2.46E+08 | 0.00E+00 | 6.94E+10 | 0.00E+00 |
| SVE vectorization      | 91.25   | 7.26E+10 | 1.16E+11 | 1.95E+13 | 2.97E+12 |
| standard deviation     | 0.31    | 1.46E+08 | 0.00E+00 | 8.87E+09 | 0.00E+00 |

Figure 3: PAPI counter for DCA++ runs on A64FX.

When optimizing any loops, the compiler’s vectorization pass must preserve the semantics of the original source code. This usually requires static analyses to verify that the transformation is legal. However, it is not uncommon for a transformation to be correct but unable to be statically verified by the compiler. Since OpenMP 4.0, OpenMP has added support for the SIMD directive, which provides a cross-platform method for statically asserting information about the program’s semantics to the compiler’s vectorization pass [7]. In DCA++, various loops require additional information to be successfully vectorized.

3.1 OpenMP SIMD

When optimizing any loops, the compiler’s vectorization pass must preserve the semantics of the original source code. Thus, with PGO, users can be guided toward the loops that would benefit the most from vectorization and avoid overloading them with a plethora of uninteresting remarks.

The authors manually analyzed several loops in the DCA++ application by using the aforementioned method described to determine what was hindering loop vectorization. Some loops required a simple change in vectorization flags, and others required user intervention (e.g., vectorization directives, such as OpenMP SIMD) to assist the compiler. The authors also identified loops that required transformations to make the vectorization more efficient. The following sections present a brief discussion for four hot loops that the compiler was unable to vectorize without user intervention.

In line 6 of Figure 5, there is a noncontinuous memory load—a gather. ARM’s SVE supports fast gathering operations; however, the compiler cannot vectorize this loop without manual intervention because the accessed arrays M_{ij}, M_{ij_left}, and M_{ij_right} might alias and hence overlap. In these situations, the compiler is often able to vectorize the loop and generate a vectorized variant guarded by a run time alias check to verify that the accessed ranges of the arrays do not overlap at run time. However, the support for such run time alias checks in LLVM/Clang is limited to the case in which the accessed bounds are known statically [8]. Because the index into the M array is based on the values loaded from the configuration arrays, the access range cannot be bound statically. The compiler remark shown below the loop nest summarizes this discussion in a way that is difficult or impossible for application developers to understand.
```c
#pragma omp simd reduction(-:x_val) aligned(x_val, G_ptr : 64)
for (int i = 0; i < j; i++)
x_val -= x_ptr[i] * G_ptr[i];
```

remark: loop not vectorized: cannot prove it is safe to reorder floating-point operations; allow reordering by specifying ”#pragma clang loop vectorize (enable)” before the loop or by providing the compiler option ”-ffast-math”

Figure 4: A loop performing a parallel reduction that is not vectorized automatically.

Using OpenMP SIMD effectively tells the compiler that there are no overlapping accesses, allowing the loop to be vectorized. Care must be taken to ensure that no aliasing actually occurs, otherwise this will result in incorrect results.

```c
for (int j = start_index_right_[orb_j]; j < end_index_right_[orb_j]; ++j) {
    const int out_j = j - start_index_right_[orb_j];
    #pragma omp simd
    for (int i = start_index_left_[orb_i]; i < end_index_left_[orb_i]; ++i) {
        const int out_i = i - start_index_left_[orb_i];
        M_ij_(out_i, out_j) = M(config_left_[i].idx, config_right_[j].idx);
    }
}
```

remark: loop not vectorized: Unknown array bounds

Figure 5: A loop performing a memory gather that requires OpenMP SIMD to be vectorized by the ARM compiler.

### 3.2 Using the Correct Compiler Flags

Some loops require additional compiler flags to be vectorized. The code shown in Figure 6 has two run time calls, line 5 and 6, which prevent the compiler from automatically vectorizing it. A function call usually requires an explicit vector version of the function and compiler support to allow vectorized execution. The ARM compiler provides an optimized math library that includes vector variants of common math functions. Users must explicitly enable such a vector library because it will disturb the precision of the result, similar to the floating point reordering. The ARM compiler provides the `fsimdmath` option to use its performance libraries, whereas standard Clang requires `fveclib` to be set to the desired vectorized library. `ffast-math` or `fno-math-errno` will allow the compiler to execute the loop out of order, but no vectorized math library is used. This means that the vector lanes are effectively unpacked before the call, and the math function is executed once per vector lane.

Another issue is that the application uses a custom matrix class that performs bounds checking by using assertions in the overloaded access operators. Although assertions are a good software engineering practice, their “complex” semantics must be preserved by the compiler. The problem is that no code is executed after a violated assertion. Thus, if assertions are enabled and present in a loop, the compiler must verify that the assertion cannot trigger to execute any side effects succeeding the assertion (e.g., from the next iteration). To disable assertions completely, `NDEBUG` can be defined during compilation; however this will cause a tension between “debug” and “release” builds that is often not desirable. For developers to identify issues that stem from assertions and other errors in handling code, the authors added a new remark to the LLVM vectorizer, which is shown below the code. For these experiments, the authors disabled assertions, provided a vectorized math library, and added OpenMP SIMD to allow vectorization, even in the presence of possibly aliasing accesses.

### 3.3 Loop Transformations

The loop in Fig. 7 contains gathers from memory at lines 11 and 18. More importantly, the code uses a column-major layout for all its matrices while this loop iterates across a row. This will require expensive scattering operations to distribute the stores to discontinuous memory addresses. This loop can be transformed to better exploit SIMD parallelism. Each iteration of this loop is independent, and the matrices are guaranteed to be square in the code, so this loop can safely be transposed to improve memory accesses. This transformation will also improve performance without vectorizing the loop.

This loop contains conditional expressions that must be transformed into masks to be vectorized. This requires calculating the result of each branch and conditionally moving it into the final register by using a mask. In this case, the
for (int j = 0; j < n_v; ++j) {
    #pragma omp simd
    for (int i = 0; i < n_w; ++i) {
        const ScalarType x = configuration[j].get_tau() * w_[i];
        T_[0](i, j) = std::cos(x);
        T_[1](i, j) = std::sin(x);
    }
}

remark: loop not vectorized: loop exit block contains control flow that does not return
remark: loop not vectorized: library call cannot be vectorized. Try compiling with -fno-math-errno, -ffast-math, or similar flags

Figure 6: A code block using the math library functions \textit{cos} and \textit{sin}.

for (int i = 0; i < Gamma.Rows(); i++) {
    for (int j = 0; j < Gamma.Cols(); j++) {
        int spin_idx_i = random_vertex_vector[i];
        int spin_idx_j = random_vertex_vector[j];
        if (spin_idx_j < vertex_index) {
            Real delta = (spin_idx_i == spin_idx_j) ? 1. : 0.;
            Real N_ij = N(spin_idx_i, spin_idx_j);
            Gamma(i, j) = (N_ij + exp_V[j] - delta) / (exp_V[j] - 1.);
        } else
            Gamma(i, j) = G_precomputed(spin_idx_i, spin_idx_j - vertex_index);
        Real gamma_k = exp_delta_V[j];
        Gamma(i, j) -= (gamma_k) / (gamma_k - 1.);
    }
}

remark: loop not vectorized: control flow cannot be substituted for a select
remark: loop not vectorized: cannot identify array bounds

Figure 7: A loop requiring a source transformation and OpenMP SIMD (left) and its transformed version (right).

true condition of the loop at line 6 is much more computationally expensive than the false condition. If the result was not needed, then this will be calculated at each iteration of the loop, only to be thrown away. This problem is even worse for the final update across the diagonal at line 17 which will only be needed once every iteration of the inner loop but calculated every iteration. This conditional update can be hoisted from the loop to improve performance significantly. Another issue is the division at line 14. This could cause a division-by-zero error that can block vectorization if regular error handling semantics are maintained. This can be disabled with fast math, but in some cases, the compiler is able to vectorize it by using masked division instructions. This would be a good application of the assume directive added in OpenMP 5.1 to assert to the compiler that the division will never cause an error.

3.4 Results

The overall impact of these transformations is shown in Fig. 8 which shows a significant speedup in most cases. The loop in Fig. 6 had the largest improvement when using ARM’s vector math support. The reduction loop in Fig. 4 yielded no improvement. Upon further investigation, this was because the loop’s trip count was very small in the average case, so the majority of the time was spent doing the final reduction, and work was rarely done in parallel. The other loops saw reasonable improvements, but their performance was limited by the gathering instructions required to vectorize them.
Figure 8: The loops in Figs. 6, 5, 7, and 4, respectively, before and after the barriers to SVE execution were remedied. Performance is measured as the total time spent by all the threads in a run using 24 accumulators/walker threads over 100,000 measurements.

4 Automating the Process: The OpenMP Advisor

It is unrealistic but unfortunately still common practice to optimize code and add support for new platforms and features by manually inspecting and modifying the application. Given the increasing complexity when it comes to hardware and the requirement to support multiple heterogeneous platforms simultaneously, the authors must rethink their software engineering practices to ensure that the code is not only correct but also performant and portable. To automate this manual process and boost programmers’ productivity, the authors began developing the OpenMP Advisor. Based on the portable OpenMP directive language, we hope to evolve the OpenMP Advisor over time into a valuable software engineering tool by using and extending LLVM capabilities. During the porting effort of the DCA++ application described here, the authors experienced various issues that require interpretation to derive actionable advice. Using their experience, the authors began automating the parts of the process and improving the compiler remarks that were missing or misleading. As a result, the OpenMP Advisor the authors develop as part of the LLVM compiler framework will use optimization remarks from multiple optimization passes to report the most performance-critical problems in the code based on the available profiling data.

5 Related Work

There are several other tools that analyze source code or provide support for parallelization but with limited support that automatically inserts SIMD directives in the code. These include: CAPO [9] for automatic OpenMP work-sharing directives generation, which supports Fortran 77 and some F90 extensions; Appentra’s Parallware [10], which focuses on parallelizing C/C++ applications by using OpenMP and OpenACC for multicores and accelerators; and Cray Reveal [11], which helps autoscope OpenMP variables and generate OpenMP work-sharing for Fortran and C/C++ for multicore and accelerators. Intel Inspector focuses on OpenMP semantic checking for data race detection. Foresys [12] and the Dragon Analysis tool [13] are legacy tools that supported the maintenance of Fortran code and help with parallelization with OpenMP.

6 Conclusion

Porting the DCA++ application to the A64FX processor requires the use of optimized scientific libraries and vectorizing the application hot spots. This process can be overwhelming to users, and tools are needed to automate this process. This work shows that by using LLVM tools, users can easily detect hot spots, determine why loops are not vectorized, and correct the issues by applying the correct compiler flags, transforming the code, or applying OpenMP directives.

Currently, authors are working an OpenMP Advisor tool that is built on top of existing and newly introduced LLVM tooling to automate this process. Ultimately, the authors want to enable application developers to navigate and handle compiler-generated information productively. Optimization reports should pinpoint important opportunities to tune the code (e.g., non-vectorized loops) and simultaneously provide sufficient information and suggestions to allow informed
decisions without elaborate studies of compiler and programming language theory. The authors believe that tools can recommend portable annotations, such as OpenMP SIMD directives, when they inform users about the requirements for correctness. Furthermore, compiler analysis and optimizations can directly target the recently proposed OpenMP assume directive to request user feedback. In other words, OpenMP assume directives and the authors’ implementation in the LLVM compiler will enable analyses and transformations to request high-level information from users naturally. The OpenMP Advisor will improve communication in the other direction to present users with important requests and remarks, together with information and examples that translate “compiler language” to “application language.”

Acknowledgment

The authors would like to thank Manuel Arenaz (Appentra Solutions), Hartmut Kaiser (Louisiana State University), and Kevin Huck (University of Oregon) for their guidance and feedback on this work.

This work was supported by the Scientific Discovery through Advanced Computing (SciDAC) program funded by US Department of Energy, Office of Science, Advanced Scientific Computing Research (ASCR) and Basic Energy Sciences (BES) Division of Materials Sciences and Engineering. This research was also supported by the Exascale Computing Project (17-SC-20-SC), a collaborative effort of the US Department of Energy Office of Science and the National Nuclear Security Administration, in particular its subproject on Scaling OpenMP with LLVM for Exascale performance and portability (SOLLVE).

Notice: This manuscript has been authored by UT-Battelle, LLC, under contract DE-AC05-00OR22725 with the US Department of Energy (DOE). The US government retains and the publisher, by accepting the article for publication, acknowledges that the US government retains a nonexclusive, paid-up, irrevocable, worldwide license to publish or reproduce the published form of this manuscript, or allow others to do so, for US government purposes. DOE will provide public access to these results of federally sponsored research in accordance with the DOE Public Access Plan (http://energy.gov/downloads/doe-public-access-plan).

This work was performed under the auspices of the U.S. Department of Energy by Lawrence Livermore National Laboratory under Contract DE-AC52-07NA27344 (LLNL-CONF-819815).

References

[1] Urs R Hähner, Gonzalo Alvarez, Thomas A Maier, Raffaele Solcà, Peter Staar, Michael S Summers, and Thomas C Schulthess. Dca++: A software framework to solve correlated electron problems with modern quantum cluster methods. Computer Physics Communications, 246:106709, 2020.
[2] Weile Wei, Arghya Chatterjee, Kevin Huck, Oscar Hernandez, and Hartmut Kaiser. Performance analysis of a quantum monte carlo application on multiple hardware architectures using the hpx runtime. In 2020 IEEE/ACM 11th Workshop on Latest Advances in Scalable Algorithms for Large-Scale Systems (ScalA), pages 77–84. IEEE, 2020.
[3] Hartmut Kaiser, Patrick Diehl, Adrian S. Lemoine, Bryce Adelstein Lelbach, Parsa Amini, Agustín Berge, John Biddiscombe, Steven R. Brandt, Nikunj Gupta, Thomas Heller, Kevin Huck, Zahra Khatami, Alireza Kheirkhahan, Auriane Reverdell, Shahrazad Shirzad, Mikael Simberg, Bibeck Wagle, Weile Wei, and Tianyi Zhang. Hpx - the c++ standard library for parallelism and concurrency. Journal of Open Source Software, 5(53):2352, 2020.
[4] Kevin A Huck, Allan Porterfield, Nick Chaimov, Hartmut Kaiser, Allen D Malony, Thomas Sterling, and Rob Fowler. An autonomic performance environment for exascale. Supercomputing frontiers and innovations, 2(3):49–66, 2015.
[5] Dan Terpstra, Heike Jagode, Haihang You, and Jack Dongarra. Collecting performance data with papi-c. In Tools for High Performance Computing 2009, pages 157–173. Springer, 2010.
[6] Patrick Diehl, Dominic Marcello, Parsa Armini, Hartmut Kaiser, Sagiv Shiber, Geoffrey C. Clayton, Juhan Frank, Gregor Daibl, Dirk Pfäflä, David Eder, Alice Koniges, and Kevin Huck. Performance measurements within asynchronous task-based runtime systems: A double white dwarf merger as an application, 2021.
[7] Joseph N. Huber, Oscar R. Hernandez, and Matthew Graham Lopez. Effective vectorization with openmp 4.5. 3 2017.
[8] Péricles Alves, Fabian Gruber, Johannes Doerfert, Alexandros Lamprinias, Tobias Grosser, Fabricio Rastello, and Fernando Magno Quintão Pereira. Runtime pointer disambiguation. In Proceedings of the 2015 ACM SIGPLAN International Conference on Object-Oriented Programming, Systems, Languages, and Applications, OOPSLA 2015, page 589–606, New York, NY, USA, 2015. Association for Computing Machinery.
[9] C.S. Ierotheou, H. Jin, G. Matthews, S.P. Johnson, and R. Hood. Generating openmp code using an interactive parallelization environment. *Parallel Computing*, 31(10):999–1012, 2005. OpenMP.

[10] Manuel Arenaz and Xavier Martorell. Parallelware tools: An experimental evaluation on power systems. In Michèle Weiland, Guido Juckeland, Sadaf Alam, and Heike Jagode, editors, *High Performance Computing*, pages 352–360, Cham, 2019. Springer International Publishing.

[11] Luiz DeRose, Heidi Poxon, James Beyer, and Alistair Hart. A high level programming environment for accelerator-based systems. *Procedia Computer Science*, 29:1480–1490, 2014. 2014 International Conference on Computational Science.

[12] Jean-Louis Pazat. *Tools for high performance fortran: A survey*, pages 134–158. Springer Berlin Heidelberg, Berlin, Heidelberg, 1996.

[13] B. Chapman, O. Hernandez, Lei Huang, Tien-hsiung Weng, Zhenying Liu, L. Adhianto, and Yi Wen. Dragon: an open64-based interactive program analysis tool for large applications. In *Proceedings of the Fourth International Conference on Parallel and Distributed Computing, Applications and Technologies*, pages 792–796, 2003.