A radiation-hardened optical receiver chip

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Abstract: High-speed optocoupler is widely used in aerospace field, it is required to have tolerance of radiation in the application environment. The key module of optocoupler is optical receiver chip. This paper introduces a kind of radiation-hardened optical receiver chip. A transimpedance amplifier with gain self-regulating circuit, a signal amplitude detector and adjustable inverter, a reference with DTMOS and enclosed gate layout are designed for radiation hardening. The proposed chip is fabricated in a standard 0.5 µm CMOS process. Experimental results indicate that the hardened chip can still work at the total dose of 400 Krad(Si).

Keywords: optical receiver, gain self-regulating circuit, narrow pulse amplitude detector and adjustable inverter, DTMOS reference, enclosed-gate NMOS, radiation harden

Classification: Integrated circuits

References

[1] M. Jutzi, \textit{et al.}: “2-gb/s CMOS optical integrated receiver with a spatially modulated photodetector,” IEEE Photonics Technol. Lett. \textbf{17} (2005) 1268 (DOI: 10.1109/LPT.2005.846563).
[2] S. Radovanovic, \textit{et al.}: “A 3-Gb/s photodetector in standard CMOS for 850-nm optical communication,” IEEE J. Solid-State Circuits \textbf{40} (2005) 1706 (DOI: 10.1109/JSSC.2005.852030).
[3] D. Lee, \textit{et al.}: “An 8.5 Gb/s CMOS OEIC with on-chip photodiode for short-distance optical communications,” IEEE ICCSS (2010) 362 (DOI: 10.1109/ISSCC.2010.5434720).
[4] T. F. Miyahira and A. H. Johnston: “Trends in optocoupler degradation,” IEEE Trans. Nucl. Sci. \textbf{49} (2002) 2868 (DOI: 10.1109/TNS.2002.805350).
[5] P. J. McMarr, \textit{et al.}: “14-MeV neutron and cobalt-60 gamma testing of a power MOSFET optocoupler,” IEEE Trans. Nucl. Sci. \textbf{50} (2003) 2030 (DOI: 10.1109/TNS.2003.821394).
[6] A. H. Johnston, \textit{et al.}: “Optocouplers: Fundamentals and hardness assurance for space applications,” IEEE Trans. Nucl. Sci. \textbf{56} (2009) 3310 (DOI: 10.1109/TNS.2009.2033685).
[7] R. A. Reed, \textit{et al.}: “Assessing the impact of the space radiation environment on parametric degradation and single-event transients in optocouplers,” IEEE Trans. Nucl. Sci. \textbf{48} (2001) 2202 (DOI: 10.1109/23.983196).
[8] H. L. Hughes and J. M. Benedetto: “Radiation effects and hardening of MOS technology: Devices and circuits,” IEEE Trans. Nucl. Sci. \textbf{50} (2003) 500 (DOI: 10.1109/TNS.2003.812928).
[9] J. R. Schwank, \textit{et al.}: “Radiation effects in MOS oxides,” IEEE Trans. Nucl.
1 Introduction

High-speed optocoupler consists of high-speed LED and optical receiver chip. The key module is the optical receiver chip whose performance directly determines the data transmission quality of optocoupler. Optocoupler can realize complete electrical isolation of input and output, and can transmit signals with high quality. The common optical receiver chips are mostly suitable for the hybrid integrated optical detection chip of optical fiber communication. However, there are few studies on optical receiver for optocoupler. Reference [1, 2, 3] introduce some optical receiver chips in different CMOS process, in which spatially modulated photodetector technology and equalizer technology are referred.

With the development of optical hybrid IC technology and the maturity of the semiconductor process, optocoupler becomes widely used in space environment. The application of optocoupler in space, has to consider all kinds of radiation effect, such as proton, neutron, electron and gamma rays, which will lead to the degradation or failure of devices [4, 5, 6]. Most of the circuit in optical receiver chip mainly consist of MOS, which is sensitive to proton, electron, gamma rays and heavy ions. Total ionizing dose (TID) effect will lead to threshold shift, leakage current and carrier mobility reduction, resulting in the degradation or failure of devices and circuits. The heavy ions can produce errors in highly integrated semiconductor devices, resulting in single-event effect [7], leading to error output of the circuits. Optical receiver with radiation hardening by design for high-speed optocoupler has great significance in space application.

In this paper, a radiation-hardened optical receiver chip is designed in a standard 0.5 µm CMOS process. Part 2 introduces the typical structure and principle of optocoupler. Part 3 describes the innovations for hardening design of the optical receiver chip. Part 4 shows TID experiment and test results for the chip. Finally, conclusion is summarized in part 5.

2 Structure and principle of optocoupler

The block diagram of a typical optical receiver chip is shown in Fig. 1. The optocoupler consists of a light emitting diode (LED) and an optical receiver. The optical receiver includes a photodetector, a reference, a transimpedance amplifier (TIA), a comparator, a signal amplitude detector, an adjustable inverter and a driver.
When the light signal emitted by the LED reaches the photodetector, it will convert into current signal. The current signal is not easy to be processed directly, so the TIA converts the current signal to a voltage signal and provide a certain gain. The comparator reshapes the signal to provide standard digital signals. The signal amplitude detector and adjustable inverter can cooperatively detect the strong and narrow pulse voltage signal caused by the single-event transient (SET) and adjust to prevent the error signal to transmit forward. An additional output driver is designed to ensure driving ability. The reference provides the accurate bias for each module of the circuit.

Because the optocoupler chip may work under radiation, the degradation of radiation should be taken into consideration. Radiation hardening by design is necessary for the sensitive devices and circuits.

3 Radiation hardening by design

Radiation effect is related to the feature size of the process. The thickness of the oxide decrease as the feature size decrease. When the thickness of the gate oxide is less than 10 nm, TID effect on gate oxide will disappear [8]. Chip in this paper is designed in a standard 0.5 µm CMOS process, in which the TID effect in thin gate oxide can be ignored. Meanwhile, TID effect on the poor quality thick field oxides will be more obvious. As the feature size goes down, the circuit becomes more and more sensitive to the single-event effect.

Radiation effect will reduce the carrier lifetime in the photodetector, which will gradually reduce the diffusion current and degenerate responsivity of photodetector [4]. Heavy ions may produce SET, resulting in transient change of voltage and current and make the chip to output error signal [7]. The radiation-induced positive charges in the edge of the thick field oxide will invert the silicon surface, forming an n-type region underneath the field oxide. The conducting paths in n-type region will greatly increase the leakage current for the n-channel transistor. [9].

A TIA with gain self-regulating circuit is proposed to keep a certain margin for photodetector degradation to avoid TID effect upon the chip. A signal amplitude detector and an adjustable inverter are designed to prevent the SET induced error signal to transmit forward and ensure normal output. The reference is hardened by
using DTMOS instead of BJT. Meanwhile, radiation-induced leakage current of MOSFET should also be controlled by applying the enclosed gate NMOS layout.

3.1 Hardening design for transimpedance amplifier

The schematic of the proposed TIA is designed as shown in Fig. 2. The first stage is a common source amplifier which provides high transconductance. The second stage is a current mirror, which is used to isolate the first and the third stages. The third stage is a common source amplifier and a local degenerative feedback composed of a resistor. The voltage amplifier in the TIA adds a local degenerative feedback \( R_{l,TIA} \) to reduce the input resistance of the third stage circuit. Thus, the open-loop low-frequency poles are pushed up. Finally, the bandwidth of the designed TIA is increased.

Assuming that the main pole is at the input side, the DC gain and bandwidth of the whole TIA circuit are as follows:

\[
|Z_{TIA,DC}| = R_{TIA}
\]  

\[
BW_{TIA} = \frac{A}{2 \pi R_{TIA}C_{in}}
\]  

where \( A \) is the voltage gain and \( C_{in} \) is the input capacitance of the three stage voltage amplifier in TIA. Based on two port network analysis, the accurate transfer functions are deduced as follows:

\[
Z_{l,TIA} = \frac{A_{l}R_{l,TIA} + r_{o}}{1 - A_{l} + s[R_{l,TIA}(C_{L,in} + r_{o}(C_{L,in} + C_{L})) + s^{2}R_{l,TIA}r_{o}C_{L,in}C_{L}]}
\]  

\[
\omega_{n} = \frac{1 - A_{l}}{R_{l,TIA}r_{o}C_{L,in}C_{L}}
\]  

\[
\zeta = \sqrt{\frac{[R_{l,TIA}C_{in} + r_{o}(C_{L,in} + C_{L})]^{2}}{4(1 - A_{l})R_{l,TIA}r_{o}C_{L,in}C_{L}}}
\]
where $A_I$ is the voltage gain of voltage amplifier, $r_o$ is the output resistance of voltage amplifier, $C_L$ is the sum of load capacitance and output capacitance, $C_{l,in}$ is the input capacitance.

From Eq. (3), it can be seen that the TIA is a two-stage system. According to Eq. (3)–(5), the expression of pole frequency can be approximately obtained:

$$f_{nd,1} = \frac{A_I}{(2\pi R_{1,TIA} C_{l,in})}$$

$$f_{nd,2} = \frac{1}{(2\pi r_o C_L)}$$

Eq. (6) shows that, compared with setting normal resistor as load, this circuit has pushed up the secondary pole by $A_I$ times and increase bandwidth of the system effectively.

In order to ensure the normal function of the circuit under radiation, the TIA should be designed to increase its dynamic input range. A gain self-regulating transistor is proposed to be added to TIA to increase its dynamic input range, which can improve the tolerance of radiation effect. The input photocurrent flows into MP$_3$ transistor via feedback resistor. As the input photocurrent increases, the output voltage of TIA increases. When the input photocurrent is larger than a certain value, MP$_3$ transistor will enter the linear region, and the circuit presents a nonlinear working state. In order to avoid bring nonlinear state into the circuit, MP$_4$ transistor is added to dynamically control the TIA gain.

When input photocurrent is large, the output voltage is also large, hence, the gain self-regulating MP$_4$ will be turned on, and the MP$_4$ is in the sub-threshold on-state. The equivalent feedback resistance $R_{TIA}$ is equal to $R_1$ add $R_{ds,MP4}$, in which the $R_{ds,MP4}$ is the equivalent resistance of MP$_4$. The equivalent feedback resistance is smaller when the output voltage is larger. That means, the equivalent transimpedance gain decreases and the output voltage is not easily saturated, which ensures that the circuit will not enter the saturated nonlinear state. When the TID effect degenerate responsivity of the photodetector, the input photocurrent decreases, and the output voltage decreases too, the MP$_4$ transistor is cut off, and the feedback resistance $R_{TIA}$ at this time is equal to $R_1$ add $R_2$. The equivalent feedback resistance is larger when the output voltage is smaller, that means the gain of the TIA becomes higher. So, the dynamic input range of TIA is widened and the TID tolerance is increased.

The frequency characteristics of the voltage amplifier are shown in the Voltage Amp curve in Fig. 3. The bandwidth of the voltage amplifier reaches 185 MHz, which is greater than $3BW_{TIA}$, and the low frequency gain is 45.6 dB, which meet the design requirements. While, the open-loop frequency characteristic of the whole TIA has 67 degrees phase margin and 11 dB gain margin. The bandwidth of the close-loop frequency characteristic of the TIA is 90 MHz, which is larger than the expected bandwidth. This is because the open-loop phase margin and gain margin are small. It makes the close-loop frequency characteristic to appear some resonance peak at the turning frequency, which makes the close-loop bandwidth seemingly high. But in fact, the phase lag is very serious, so the transient response delay is not very small.

Fig. 4 shows the transient response waveforms of a TIA with (W/) and without (W/O) gain self-regulating circuit respectively, when the input photocurrent is
large. As shown, the high-level output voltage has a long tail without automatic gain control. In contrast, the high-level output tail has a small effect with gain self-regulating circuit. So that the response speed is accelerated and the trail is eliminated, the bandwidth of the TIA meets the requirement.

3.2 Single-event transient detection and hardening

In radiation environment, the heavy ions may hit the photodetector and leads to ionization. These charges are transmitted and collected, resulting in transient fluctuations in voltage and current at the incident node. Finally, the optical receiver may respond to generate an error signal.

This paper proposes a SET hardened circuit, which includes a narrow pulse amplitude detector and a charging current adjustable inverter. Fig. 5 shows the structure of the detector and adjustable inverter. $V_{O1}$ is the output of the TIA. $I_{\text{charge}}$ is connected with the power supply of the adjustable inverter, which provides charging current for the establishment of the output signal of the inverter. $V_b$ is the bias voltage provided by the reference circuit.

The pulse current signal is transformed into a voltage signal with a large amplitude of narrow pulse by TIA, and will be detected by the detection circuit. The detection circuit adjusts the adjustable inverter by reducing its charging...
current, so that the pulse signal cannot be established normally in a narrow time. Different from ordinary inverters, the output terminal is connected with a load capacitor $C_1$. When the input of the inverter is low, the charging current of the load capacitor is regulated by the detection circuit. The logic of the narrow pulse output from the TIA must be correct when it is transmitted to the input of the adjustable inverter.

$MN_1$ is turned off during normal signal transmission, and $I_{charge}$ is the sum of the currents flow in $MP_2$ and $MP_3$, which ensures the adjustable inverter works properly. When the input of the detection circuit is a large narrow pulse signal, $MN_1$ will turn on, meanwhile $MN_2$ source voltage rise up to cut off itself, which means the current in $MP_2$ is zero. Compared with $MP_2$, $MP_3$ has a very small static current, so that $I_{charge}$ is much smaller than the normal signal transmission. Therefore, when the narrow pulse signal is transmitted to the input of the adjustable inverter, the output signal cannot be established, thus preventing the error signal from transmitting forward.

Fig. 6 shows the simulation waveforms of an optical receiver with the SET hardening circuit. $I_{pd}$ represents the current of the photodiode. In general, the photocurrent amplitude is 3 to 10 µA. SET can cause the instantaneous increase of the current in the optical receiver. In Fig. 6, the current signal with nanosecond pulse width and large amplitude is used to simulate the SET current. $V_{e1}$ is the output of a TIA, which converts the transient current signal into a large voltage.
signal. \( V_{o2} \) is the output of the comparator, and there is a false signal after the normal signal. \( V_{o3} \) is the output of an adjustable inverter and the output of the whole circuit.

Due to the SET hardening design of the circuit, the error signal of SET cannot be transmitted forward. Therefore, the tolerance of the circuit to the SET is enhanced to a certain degree by applying a narrow pulse amplitude detector and an adjustable inverter.

### 3.3 Radiation-hardened reference with DTMOS

In traditional reference structure, diode connected BJT transistor is used to generate proportional to absolute temperature (PTAT) current. In the non-radiation environment, the PN junction diode has normal performance.

However, under the radiation, the positive radiation-induced charges are generated and accumulated in the field oxides at the SiO\(_2\) side near the SiO\(_2\)-Si interface. At the same time, negative charges are induced at the Si interface, forming a parasitic PN\(^+\) junction. The induced electron concentration increases as the total dose accumulates, and changes the I-V characteristic of BJT transistor, which makes the output of reference shifting from the design value. So the degradation of BJT in radiation, has great influence on the reference output.

DTMOS is widely used in the radiation hardening for the reference [10]. DTMOS is a dynamic threshold MOS, which is in fact a PMOS transistor whose gate/drain/substrate are connected together. Its I-V characteristics are similar to PN junction. The structure of reference with DTMOS instead of BJT is shown in Fig. 7.

![Fig. 7. Reference with DTMOS](image)

The operational amplifiers consist of MN\(_1\), MN\(_2\), and MP\(_1\)–MP\(_4\). The output of operational amplifiers is connected to MN\(_3\), which constitutes a common source amplifier. The output current of MN\(_1\) transistor flows through two branches and then it is mirrored to R\(_1\) by a current mirror composed of MP\(_8\) and MP\(_9\). The feedback voltage is generated by R\(_1\) and applied to one end of the amplifier. The DTMOS generates reference voltage at the other end of the operational amplifier. MP\(_3\), MP\(_5\), MP\(_7\) and MN\(_6\) construct the starting circuit. When all the ratio of current mirrors in Fig. 7 are 1:1, the reference current becomes:
\[ I_{\text{bias}} = \frac{V_{S,\text{DTMOS}}}{R_1} \] (8)

\( V_{S,\text{DTMOS}} \) is the source voltage of DTMOS with negative temperature coefficient. \( R_1 \) is the resistance of the polysilicon resistor with negative temperature coefficient also. So, it has a certain degree of temperature compensation to the reference current.

### 3.4 Hardened layout design with enclosed gate NMOS

TID effect will greatly increase the leakage current for the NMOS. It has been proved that the edgeless structure of the enclosed gate layout can cut off that leakage current path. So the enclosed gate layout structure is widely used in radiation-hardened integrated circuit design [11]. All the NMOS used in the optical receiver chip are layout as the enclosed gate NMOS.

The layout of the enclosed gate MOS is various, and the corner-cut square gate structure is adopted in this design, as shown in Fig. 8. There is only small thickness gate oxide with good quality between source and drain, and there is no thick field oxide. In the radiation environment, the accumulated charges in the gate oxide layer is greatly reduced, and the leakage current between the source and the drain is effectively suppressed.

![Fig. 8. Corner-cut square structure for enclosed gate MOS](image)

However, due to its special geometry, it cannot be recognized by the standard CMOS process. Such as its parameters cannot be identified accurately, cannot be validated by LVS/PEX rules, cannot be applied to circuit design and simulation. In order to realize the circuit design and simulation with enclosed gate MOS, this paper build up the library for the enclosed gate MOS in the PDK.

According to conformal transformation, the irregular shape is equivalent to the parallel connection of the standard rectangular channel, and the equivalent \( \frac{W}{L} \) of the enclosed gate layout can be obtained. The equivalent \( \frac{W}{L} \) of the corner-cut rectangular gate layout is obtained as [12]:

\[ \frac{W}{L} = \frac{W_1}{L_1} + \frac{W_2}{L_2} + \cdots \]
$$\frac{W_{\text{eff}}}{L} = \frac{8\alpha}{\ln\left(\frac{d}{d' - 2aL_{\text{eff}}}\right)} + K \frac{1 - \alpha}{\frac{1}{2}\sqrt{\alpha^2 + 2\alpha} + 5\ln\frac{1}{\alpha}} + \frac{d - d'}{2L_{\text{eff}}}$$ \quad (9)

$$d' = d - \sqrt{2C}$$ \quad (10)

$$K = 8 - A/L$$ \quad (11)

$$L_{\text{eff}} = L - 2L_D$$ \quad (12)

In which, $L_D$ is the lateral diffusion length of the channel internal source drain, and $\alpha$ is the fitting parameter, which is used to characterize the boundary of the division of the conformal transformation.

With this equivalent calculation model, the equivalent $W/L$ of the MOS can be obtained. More importantly, the enclosed gate MOS cell library can be built up, such as Cadence library, Hspice simulation library, Calibre validation library, etc. Consequently, the enclosed gate MOS model can be used for simulation of the enclosed gate circuit.

This paper has taped out and tested the single NMOS transistor to verify the effectiveness of this method. As shown in Fig. 9, the $I_{\text{reg}}$ curve is the transfer characteristic curve of a normal 14 µm/2 µm NMOS and the $I_{\text{elt}}$ curve is the transfer characteristic curve of an enclosed gate NMOS which has equivalent $W/L$ of 14 µm/2 µm. It can be seen that the two curves are very similar.

4 Radiation experiment and analysis

The optical receiver chip was designed and fabricated in a standard 0.5 µm CMOS process. Experiment of irradiation and test was carried out. The test used the Co-60 gamma ray source to irradiate the packaged chips at dose rate of 50 rad/s, up to total dose of 400 Krad(Si) in several steps. The test samples are the radiation-hardened optical receiver chips designed in this paper. Layout of the designed chip is shown in Fig. 10. The light emitted from LED irradiate on photodetector in the middle. Pad VDD is the power supply, pad GND is the ground, pad VE is the enable port, and pad OUT is the output port. Importantly, pad VTRIM is designed to connect an extra resistor to adjust the flipping threshold of comparator. This can...
ensure the optical receiver to work properly, even when integrated to different LEDs with different parameters.

![Fig. 10. Layout of the hardened optical receiver chip](image)

The optical receiver chip was packaged together with an LED to compose an entire optocoupler. The input signal is added to input of the optocoupler, which is the input of the LED shown in Fig. 1. A 4 V input voltage is added on the LED and an input resistor in series connection. The power supply current of the chip is monitored in real time during the whole test. The input and output waveforms are characterized by the oscilloscope at the dose node to read the transmission delay time. The sample chips are put back within 30 minutes when each test finish. Table I shows the comparison of test data before and after irradiation throughout the test. The tPLH is establishment time from low to high and the tPHL is high to low.

| Number of chip | Hardened | Total dose irradiation (Krad(Si)) | Static current (mA) | Dynamic current (mA) | tPLH (ns) | tPHL (ns) |
|---------------|----------|----------------------------------|--------------------|----------------------|----------|----------|
| #1            | No       | before 4.679                      | 12.256             | 1160                 | 100      | failed   |
|               |          | 50 4.896                          | 5.283              | failed               | failed   | failed   |
| #2            | Yes      | before 5.519                      | 12.665             | 1040                 | 56       | 46       |
|               |          | 400 5.530                         | 12.910             | 1014                 | 46       | 46       |
| #3            | Yes      | before 5.372                      | 12.598             | 1180                 | 45       | 45       |
|               |          | 400 5.390                         | 12.710             | 1220                 | 48       | 48       |

The normal chip without hardening design fails at total dose of 50 Krad(Si). At total dose of 50 Krad(Si), the output of the unhardened chip nearly becomes constant high and the time turned down is very short, as shown in Fig. 11(a). It can be inferred that the static working point of TIA moves up after irradiation, resulting in the increase of TIA output, and the output of comparator becomes...
continuous high. And in the following test, with the increase of the total dose, the unhardened chip output can no longer flip, and completely fails out.

However, the hardened chips can still work normally at the total dose of 400 Krad(Si), as shown in Fig. 11(b). It is obvious that the radiation hardening for the optical receiver chip is very effective. By comparing the parameters of the chips before and after irradiation, the parameters change only a little, meeting the requirements for the radiation application.

5 Conclusion

This paper introduces the design of a radiation-hardened optical receiver chip. A TIA with gain self-regulating circuit is proposed to widen the dynamic input range and enhance the tolerance to TID effect. A signal amplitude detector and the adjustable inverter is proposed to detect and prevent the error signal transmitting and enhance the tolerance to SET. The reference is hardened by using DTMOS instead of BJT. The enclosed gate layout is applied to the chip by building up the design library for it. TID experiment and test are carried out for packaged chips, which are fabricated in a standard 0.5 µm CMOS process. The test results prove the radiation-hardened optical receiver chip can still work after TID irradiation at total dose of 400 Krad(Si) and the hardening design for the optical receiver chip is very effective.

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