A non-isolated DC-DC converter with low voltage stress and high step-down voltage conversion ratio

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Abstract
This work focuses on a new non-isolated interleaved DC-DC converter with very high step-down voltage conversion ratio. By employing the switched/series capacitor concept, along with the proper component interconnection, the converter features a high step-down voltage conversion ratio where, in the private case of equal duty ratios, it is six times higher than the conventional buck converter. This high step-down voltage conversion ratio is achieved with the lowest number of components compared to other similar topologies of the same conversion ratio. Also, due to the blocking/series capacitors, the voltage stress on the switches is reduced, improving the converter efficiency. One of the key features of the proposed converter is the inherent automatic current sharing between the interleaved phases, which in the case of equal duty ratios, is uniformly distributed. To add on, due to the use of only two interleaved phases, the converter has a wide output voltage range, since the duty cycle can be extended to 0.5. To validate the proposed converter operation, a 250 W wide-input/wide-output experimental prototype was built, achieving a peak efficiency of 94%.

1 INTRODUCTION

Nowadays, step-down DC-DC converters have gained and increased interest, due to their employment in various applications such as battery chargers, LED lamp drivers but more importantly, as power supplies in automotive industry, IoT devices, data centres and power-over-tether systems [1–10]. In hybrid and electric vehicles, where the battery pack voltage value is increasing due to the use of highly efficient permanent magnet synchronous motors (PMSM) motors [11, 12], the use of high step-down voltage ratio DC-DC converters is imperative for present and future applications [6]. In data centres applications, they can be used as separate conversion stages or to combined stages, i.e. combination of the first step-down stage from the high voltage DC bus to lower values (usually 48 V) and the pre-regulating module (PRM) stage, before the conversion to the isolated 12 V safe extra low voltage (SELV) levels [4, 8, 9, 13]. In power-over-tether applications, step-down converters are used to directly supply the unmanned aerial vehicles (UAVs) while operating, increasing the drone flight duration [10].

These applications require converters with high output current capabilities, tightly regulated output voltage, and high efficiency. Numerous isolated topologies could fulfill the previous characteristics. However, isolated topologies have drawbacks such as slower response in transients due to the transformer large inductances, high cost due to the customized transformer design, as well as high voltage stress on the devices during switching transitions, due to the transformer leakage inductance [14].

In cases where isolation is not mandatory, the conventional interleaved buck converter (IBC) could be introduced as a solution, due to its simplicity in design and control [15]. However, the major drawback of the IBC is the low efficiency at low duty cycle values, due to the high current stress on the semiconductor devices. Also, in the switch voltage stress is equivalent to the input voltage, transistors and diodes with high breakdown voltages are selected, leading to extended conduction losses due to the high on-resistance ($R_{DS(on)}$) of MOSFETs and high forward voltage of diodes, respectively. To achieve high step-down voltage conversion ratios combined with high efficiency and high
output current capabilities, several topologies and PWM techniques have been proposed [8, 14, 16–48].

To extend the duty cycle of the conventional IBC, the quadratic buck converter was firstly introduced in [16–18]. This topology is a two-stage converter where the step-down voltage conversion ratio is a function of the square of the duty cycle ($D^2$). The major drawback of this topology is the high voltage stress on the active switching device, which depends on the duty cycle and is always higher than the input voltage. Thus, the efficiency of this topology is affected by the high switching losses on the transistor. The same voltage conversion ratio ($D^2$) can be achieved in the conventional buck converter with the implementation of the dual PWM control, as introduced in [8]. The only drawback of the dual PWM control is that the high frequency carrier must be multiple times higher than the low frequency carrier, making the control difficult with conventional microcontrollers. The delayed quadratic buck converter, introduced in [19], employs an additional inductor, offering higher step-down voltage conversion ratio but the voltage stress on the main switch remains the same as in the conventional quadratic buck. By adding a switching-capacitor cell in the quadratic buck the step-down ratio is increased, but at the cost of even higher voltage stress on the main switching device than in the quadratic buck [20]. An improved version of the quadratic topology is the double quadratic buck [21], implemented by clamping the neutral point of the input voltage to another quadratic buck. The transistor voltage stress is halved but still depends on the duty cycle values, making the selection of devices with lower breakdown voltage difficult. Extreme quadratic based conversion ratios are, also, achieved by the fourth-order converter in [22] but at the cost of very high voltage stress on the main switch, depending on the duty cycle values.

Similar to the IBC is the series capacitor (SC) buck converter proposed and revised in [23] and [24] respectively, while its optimal steady-state and transient mode control is studied in [25]. Although the voltage conversion ratio is $D/2$, one transistor is stressed with the input voltage, leading to the selection of transistors with higher breakdown voltage and higher $R_{DSon}$. An alternative SC IBC converter with reduced switch voltage stress and continuous input current is presented in [26]. Although the continuous input current feature improves the power quality at the converter input, the step-down ratio is not as high as in the original SC IBC. The double series capacitor buck converter (DSCBC) in [27], offers improved voltage step-down ratio ($D/3$) with low component count. However, for equal duty ratios, one inductor has twice the current value of the other, leading to asymmetrical magnetic component design and higher output ripple than the conventional two-phase IBC.

Improved step-down voltage conversion ratios could, also, be achieved by employing the switched-capacitor concept [14, 28, 29]. This concept is either employed as a front-end cell of capacitors and diodes [14] or as a multilevel/multistage converter, such as the converters in [28, 29]. As multistage converters, the voltage gain depends exponentially [25] or is based on mathematical sequences [29] on the number of cascaded switched-capacitor structures. In both cases, however, the number of components needed for interleaved converters is very high, making the implementation of such converters impractical.

Great step-down conversion ratios can be also achieved with the hybrid high-ratio voltage step-down converters, by employing more than one of the concepts above. A hybrid of the quadratic and series capacitor concept, proposed in [30], offers a wide duty cycle range and improved efficiency due to lower voltage stress on the devices but at the cost of a significantly high number of components. However, the most renown hybrid case is the switched/series capacitor concept [31–37]. Based on this, an expandable four-phase interleaved voltage step-down converter with quadruple conversion ratio ($D/4$) and low switch voltage stress was presented in [31]. The main converter drawbacks are the narrow duty cycle range ($D_{max} = 0.25$) and the high number of magnetic components. The same conversion ratio is achieved by the converter in [32], when $D < 0.25$. Again, this converter has duty cycle limitations, as for higher values, the converter operation differs, and the step-down capability is degraded. Based on the [32] topology, the converter in [33] has a lower number of components and operates in two or three phase mode but the conversion ratio is only $D/3$. A four-phase converter with quadruplet conversion ratio and low capacitor count is reported in [34]. Contrary to the low number of capacitors is the high number of semiconductor switches needed for the converter implementation. This conversion ratio is, also, offered by the two-phase converter in [35], with only two output buck stages and wide duty ratio ($D_{max} = 0.5$), at the cost of higher output voltage ripple. An attempt to achieve greater conversion ratio ($D/6$) was made in [36] and [37], by expanding the converter presented in [35]. Yet, the number of diodes and magnetic components increases, whereas the duty cycle value is limited to 0.33.

To further increase the voltage step-down conversion ratio, the coupled techniques are introduced [38–48]. Some advantages of coupled inductors converters are the turns ratio dependent voltage conversion ratio, the ability to create single-input multiple-output converters (SIMO) and the possible creation of ZVS/ZCS conditions by carefully utilizing the leakage inductance. An SIMO converter with ZVS was proposed in [38]. Despite the high voltage stress on the transistors, the converter offers high conversion ratio. However, as in most SIMO cases, the converter lacks control of its secondary output voltage value, since it depends on several parameters besides the converter duty ratio, such as the output inductance value, the load etc.

In the category of single-output coupled inductor converters, the converter in [39] does not achieve high step-down ratio and the input switch must have higher breakdown voltage as it blocks the input voltage, affecting the converter efficiency, despite the ZVS condition. ZVS condition has, also, the converter in [40] but the blocking voltage of the input switch and diode equals to the input voltage as well, leading to selection of transistors with high breakdown voltage and high $R_{DSon}$. The converter in [41] and its improvement in [42], has very high conversion ratio, and the combination of
lower switch voltage stress with ZVS, improves the overall converter efficiency. However, the step-down conversion ratio is significantly affected by the coupling coefficient of the coupled inductors.

Other converters are offering ZCS conditions, taking advantage of the leakage inductance values [43–48]. Based on [35], the converter in [43] offers ZCS and increased conversion ratio. However, the switch blocking voltage remains high, similar to the converter in [35]. High step-down conversion ratio with ZCS characteristics has, also, the converter in [44]. The drawbacks of this topology are the high number of magnetic components and the very small duty cycle range ($D_{max} < 0.25$). Low component count and high conversion ratio, with ZCS condition, is achieved by [45]. The switch voltage stress, however, depends on the duty ratio and turns ratio, where for $n < 1$ values, becomes significantly greater than the input voltage. Despite the high step-down conversion ratio, the converter [46] has high switch voltage stress, which combined with the inherent converter gain sensitivity to the coupling factor, makes it not very suitable for high input voltage applications. The converter in [47] is based on the converter [27], offering higher conversion ratio values. Still, the asymmetry on the inductor currents remains an issue, causing higher output voltage ripple as the ripple of the inductor phased currents are not cancelling each other. Another converter with ZCS and a self-driver synchronous rectifier is the converter [48]. The step-down ratio, however, is not as high compared to other coupled inductor topologies.

In general, several coupled inductors topologies and configurations have been proposed, managing to extend the conversion ratio due to the dependence on coupled inductors turn ratio. However, the circuit and design complexity of coupled inductor converters are very high, due to the transformer construction and additional conduction states related to the leakage inductance. Leakage inductance is a double-edged sword: on the one hand offers ZVS and ZCS conditions but on the other hand affects the step-down conversion ratio and if not properly addressed, it can create voltage overshoots with devastating effects for the semiconductor switches [49].

In this paper, an interleaved high step-down voltage conversion ratio converter is presented, with six times higher voltage conversion ratio than the conventional IBC (D/6). The converter is a hybrid topology which combines the switched and series capacitor structures as the front-end and the interleaved buck converter concept as the back-end, and has the lowest number of components, compared to similar topologies of the same conversion ratio. What is more, the appropriate front-end switched/series capacitor structure allows for low switch voltage stress during steady-state, and with the appropriate PWM sequence, offers automatic current sharing to its only two output inductors as well as a wide output voltage range due to the extended duty ratio limit, up to 0.5.

The operating principles of the converter are described in detail in Section 2. In Section 3, the dc voltage gain is extracted, and the automatic current sharing mechanism is explained. A converter design guide is presented in Section 4 and a comparison with other topologies of the same voltage conversion ratio is conducted in Section 5, highlighting the pros and cons of the proposed topology. A more practical approach to the component selection, as well as the most significant experimental results and power loss distribution, are presented in Section 6. Finally, conclusions are presented in Section 7.

2 OPERATING PRINCIPLES OF THE CONVERTER

The topology under investigation, shown in Figure 1, consists of six transistors, six blocking capacitors but only two inductors with their corresponding freewheeling diodes. The converter uses the blocking and series capacitor concept; by series charging and parallel discharging, the capacitors manage to divide the input voltage $V_{in}$, automatically distribute the output current to the output inductors and increase the voltage conversion ratio.

Although the converter has a high number of switches, the operation is simple since only two PWM signals with $180^\circ$ phase-shift are needed. First, the group of transistors $Q_{1a}, Q_{1b}$ and $Q_{1c}$ is switched-on, and with $180^\circ$ phase-shift, the second group of transistors ($Q_{2a}, Q_{2b}$ and $Q_{2c}$) is switched-on. Due to the parallel discharging of capacitors, the maximum theoretical permitted duty ratio for each group is 0.5, since for higher duty ratios the converter will not operate in the intended mode. Nevertheless, compared to similar topologies, the converter has the highest duty ratio regulation limit, offering wider output voltage range.

To theoretically analyse the circuit operation, the following assumptions should be made: The converter operates in steady-state and in continuous conduction mode (CCM), the inductor values $L_1$ and $L_2$ are equal ($L_1 = L_2 = L$), all capacitors ($C_1, C_2, C_3, C_4,$ and $C_5$) are considered large enough so that their voltage values remain approximately constant within a switching period and, finally, all active and passive devices are considered ideal (zero conduction and switching losses, zero voltage drop). The different conduction states within a switching cycle are shown in Figure 2.

In State 1 ($t_0, t_1$), as shown in Figure 2(a), the group of $Q_{1a}, Q_{1b}$ and $Q_{1c}$ is switched-on, creating three separate and parallel current loops which charge the inductor $L_2$, whereas the current of inductor $L_1$ is freewheeling through diode $D_1$. For the first current path, stored energy in capacitor $C_1$, as well as energy from the input, is transferred to $L_2$ inductor through
$C_2$ and $C_{a2}$, while charging them. The path is closed back to $C_i$ through the load and $D_i$ and back to $V_{in}$ through the load, $D_i$ and $C_{a2}$, while charging it. Within the second current loop, $C_4$ is discharging, transferring its energy to $L_2$, while charging $C_b$. The second path is closed back to $C_4$ through the load and $Q_{2c}$. Finally, since $Q_{1h}$ is turned-on, a third current path is created, and energy from $C_a$ is transferred to $L_2$ through $Q_{1h}$ and $C_{a2}$ while charging $C_b$. The third loop is closed back to $C_a$ through the load and $D_i$.

In State II [$t_1$, $t_2$], all six transistors are switched-off. During this state, both inductors are discharging through their corresponding diodes, transferring the energy stored in them from the previous charging states to the load. In addition, the input capacitors $C_i$ and $C_2$ are charging from the input, correcting any deviation from their nominal voltage value. The circuit operation during this state is shown in Figure 2(b).

In State III [$t_2$, $t_4$], the operation is symmetrical to State I as the second group of transistors ($Q_{2a}$, $Q_{2b}$ and $Q_{2c}$) is switched-on, charging the inductor $L_1$ while $L_2$ current is freewheeling through $D_2$. As shown in Figure 2(c), the inductor $L_1$ is charging through three different current paths. Within the first current loop, the capacitor $C_2$ is connected in parallel with the input source and $C_i$, transferring their energy to $L_1$. The current loop is closed back to $C_2$ and $V_{in}$ through the load, $D_2$, $C_b$ by discharging it, $C_4$ by charging it and $Q_{2a}$. Regarding the second path, $C_3$ stored energy is transferred to $L_1$, through $Q_{2b}$ and $C_b$, while charging $C_a$. The second loop is closed back to $C_3$ through the load, $D_2$ and $C_{a2}$, while discharging it. Finally, for the third current path, $C_b$ is discharging, transferring a portion of its energy to inductor $L_1$, through $Q_{2c}$. The third path is closed back to $C_3$ through the load and $D_2$ once again.

In State IV [$t_3$, $t_4$], all transistors are switched-off, leading the inductor currents to freewheel through their corresponding diodes. State IV circuit operation is the same as in State II and can be described by Figure 2(b).

The key waveforms of the proposed converter are presented in Figure 3. The voltage stress on each transistor depends on the capacitors voltage and, as will be proven later, the maximum theoretical voltage stress is always equal to $V_{in}/3$, except for the transistor $Q_{1h}$, which is even lower (down to $V_{in}/6$). This will allow the selection of transistors with low breakdown voltage values, which may have improved characteristics such as low $R_{DSS}$, minimizing the conduction losses of the converter, which, as will be proven later, are not dominant to the total converter losses. The most important feature, however, is that during switch-on/switch-off transitions, the voltage across the transistors is lower than $V_{in}/3$ and, in case of equal duty ratios, equals to $V_{in}/6$, leading to reduced switching losses. On the other hand, the voltage across diodes $D_1$ and $D_2$ is lower than $V_{in}/3$, and for equal duty ratios is $V_{in}/6$, allowing the selection of diodes with low breakdown voltage, such as Schottky which offer low forward voltage and zero reverse recovery losses, and improving the converter efficiency even further.

## 3 STEADY STATE ANALYSIS

The dc voltage gain and the automatic current sharing of the proposed converter will be investigated only in CCM. Besides, for the same output power in discontinuous conduction mode (DCM), the peak and rms currents through the semiconductor devices would become extremely high, making the employment of the converter for high output current and high efficiency applications impractical.

### 3.1 DC voltage gain

During State I [$t_0$, $t_1$], the inductor $L_2$ is charged by three different current paths. Hence, the voltage across $L_2$ for each loop should be equal to:

$$u_{L_{2,t0}-t1} = V_{C1} - V_{C2} - V_o$$  \hspace{1cm} (1)

$$u_{L_{2,t0}-t1} = V_{C4} - V_{Cb} - V_o$$  \hspace{1cm} (2)

$$u_{L_{2,t0}-t1} = V_{Ca} - V_{Cb} - V_o$$  \hspace{1cm} (3)
Combining Equations (2) and (3), we conclude that $C_4$ and $C_a$ voltage values are equal:

$$V_{C4} = V_{Ca}$$  \hspace{1cm} (4)

since $V_{C4} = V_{Ca}$, Equations (2) and (3) are identical. Hence, by combination of Equations (1), (2) and (4), the $C_1$ capacitor voltage is:

$$V_{C1} = V_{C3} + V_{C4} = V_{C3} + V_{Ca}$$  \hspace{1cm} (5)

On the other hand, during State III [$t_2$, $t_3$], the inductor $L_1$ is charged by three different current loops. Once again, the voltage across the inductor $L_1$ must be equal to:

$$u_{L1,t_2-t_3} = V_{C2} - V_{C4} + V_{Cb} - V_o$$  \hspace{1cm} (6)

$$u_{L1,t_2-t_3} = V_{C3} - V_{Ca} + V_{Cb} - V_o$$  \hspace{1cm} (7)

$$u_{L1,t_2-t_3} = V_{Cb} - V_o$$  \hspace{1cm} (8)

The combination of Equations (6) and (8), as well as Equations (7) and (8), leads to Equations (9) and (10) respectively:

$$V_{C2} = V_{C4}$$  \hspace{1cm} (9)

$$V_{C3} = V_{Ca}$$  \hspace{1cm} (10)

Hence, combining Equations (4), (9) and (10), it is derived that the capacitors $C_2$, $C_3$, $C_4$ and $C_a$ have always the same voltage value:

$$V_{C2} = V_{C3} = V_{C4} = V_{Ca}$$  \hspace{1cm} (11)

Also, combining Equations (5) and (11), the $C_1$ capacitor voltage value is always equal to:

$$V_{C1} = 2V_{C2}$$  \hspace{1cm} (12)

Considering that the input voltage equals to the sum of the input capacitors $C_1$ and $C_2$ voltage:

$$V_{in} = V_{C1} + V_{C2}$$  \hspace{1cm} (13)

from Equations (11), (12) and (13), and after some manipulations, the voltage values of capacitors $C_1$, $C_2$, $C_3$, $C_4$ and $C_a$ are always given by Equations (14) and (15), regardless of their capacitance or the converter duty ratio:

$$V_{C1} = 2V_{in}/3$$  \hspace{1cm} (14)

$$V_{C2} = V_{C3} = V_{C4} = V_{Ca} = V_{in}/3$$  \hspace{1cm} (15)

On the other hand, the $C_b$ voltage value depends on the duty ratio of each state. In steady-state operation, $V_{Cb}$ can be calculated considering that the average voltage value of each inductor within a switching cycle equals to zero. Hence, for the inductor $L_2$:

$$\frac{1}{T_s} \int_{t_0}^{t_i} u_{L2}(t) dt = 0 \Rightarrow u_{L2,t_0-t_1}D_2 = V_o(1-D_2) \Rightarrow \left(\frac{V_{in}}{3} - V_{Cb} - V_o\right)D_2 = V_o(1-D_2) \Rightarrow \frac{V_{in}}{3}D_2 = V_{Cb}D_2 = V_o$$  \hspace{1cm} (16)
where \( D_a = \frac{t_{on,Q1}}{T_s} \) is the duty ratio of \( Q_1 \) group of transistors \((Q_{1a}, Q_{1b}, Q_{1c})\) and \( T_s \) is the switching period. Likewise, for the inductor \( L_1 \) we have:

\[
\frac{1}{T_s} \int_0^T u_{L1}(t) \, dt = 0 \Rightarrow u_{L1,t_2-t_1} = V_o (1 - D_b) \\
\Rightarrow (V_{Cb} - V_o) D_b = V_o (1 - D_b) \Rightarrow V_{Cb} D_b = V_o
\]

(17)

where \( D_b = \frac{t_{on,Q2}}{T_s} \) is the duty ratio of \( Q_2 \) group of transistors \((Q_{2a}, Q_{2b}, Q_{2c})\). The combination of Equations (16) and (17), reveals that \( V_{Cb} \) depends on both duty ratio values and equals to:

\[
V_{Cb} = \frac{V_o D_a}{3 (D_a + D_b)}
\]

(18)

The step-down voltage conversion ratio arises by substituting Equations (17) to (18), and after a few manipulations:

\[
\frac{V_o}{V_{in}} = \frac{D_a D_b}{3 (D_a + D_b)}
\]

(19)

From Equation (19), it is obvious that the dc voltage gain depends on the relation between \( D_a \) and \( D_b \). In the case of equal duty ratios, i.e. \( D_a = D_b = D \), the step-down voltage conversion ratio is six times higher than the IBC and is given by:

\[
\frac{V_o}{V_{in}} = \frac{D}{6}
\]

(20)

Also, for equal duty ratios, \( V_{Cb} \) is calculated equal to:

\[
V_{Cb} = \frac{V_o}{6}
\]

(21)

which confirms the theoretical waveforms presented in Figure 3.

### 3.2 Automatic current sharing

One of the major features of the proposed topology is the automatic uniform current sharing between the two output inductors. The balance between the average inductor currents \( I_{L1} \) and \( I_{L2} \), can be derived by analysing the charge balance of each capacitor within a switching cycle. For instance, in State I, the capacitor \( C_b \) is charged by the inductor \( L_2 \) current, since they are connected in series. The charge change of \( C_b \) is obtained by:

\[
\Delta Q_{Cb,Stat1} = \frac{D_a I_{L2}}{f_s}
\]

(22)

where \( f_s \) is the switching frequency. In contrast, during State III, \( C_b \) is discharging by \( I_{L1} \) current, transferring its stored energy to the inductor \( L_3 \). The change in \( C_b \) charge equals to:

\[
\Delta Q_{Cb,StatIII} = \frac{D_a I_{L3}}{f_s}
\]

(23)

Since the sum of the average inductor currents \( I_{L1} \) and \( I_{L2} \) is equal to the output current \( I_o \), and due to the fact that Equations (22) and (23) must be equal within a switching period, it is proven that the average output current is automatically distributed to each inductor according to the following relations:

\[
I_{L1} = \frac{D_a}{D_a + D_b} I_o
\]

(25)

\[
I_{L2} = \frac{D_b}{D_a + D_b} I_o
\]

(26)

Thus, in the case of equal duty ratios \( D_a = D_b = D \), the output current is uniformly distributed between the two inductors:

\[
I_{L1} = I_{L2} = \frac{I_o}{2}
\]

(27)

### 4 Key Design Parameters

#### GUIDANCE

As mentioned in the steady-state analysis, the converter operates in CCM and the capacitor voltage values are considered approximately constant. In practice however, a voltage ripple will appear on them due to the charging/discharging process within a switching period. What is more, not only the device voltage stress but the transistor and diode current stress should be quantified as well, to better understand their impact on the converter design. Therefore, to properly design the converter, these important features must be determined.

#### 4.1 Minimum inductance value and inductor current ripple

As shown in Figure 3, in the private case of equal duty ratios, the inductor currents have the same average value as well as the same waveform, only shifted 180° to each other. Hence, the current equation for each inductor within a switching period is given by:

\[
i_{L1,2}(t) = \begin{cases} 
\frac{L_2}{2} - \frac{V_o (1-D)}{2 L f_s} t, & 0 \leq t \leq DT_i \\
\frac{L_2}{2} + \frac{V_o (1-D)}{2 L f_s} (t - DT_i), & DT_i \leq t \leq T_i 
\end{cases}
\]

(28)
where the first two terms of the upper equation are the minimum inductor current $I_{L,\text{min}}$, and the first two of the second one equal to the maximum current $I_{L,\text{max}}$. Combining Equations (20) and (28), the current ripple of each inductor with respect to the input voltage is:

$$\Delta I_{L1} = \Delta I_{L2} = \Delta I_L = \frac{V_{in}(1 - D)D}{6L_{fs}}$$

(29)

Regarding the minimum inductance value, the converter inductors operate in CCM when their minimum current $I_{L,\text{min}}$ is equal or greater than zero. Therefore, the minimum inductance can be calculated combining Equations (20) and (28), and should satisfy the following inequality:

$$I_{\text{min}} \geq \frac{V_{in}(1 - D)D}{6I_{\text{min},fs}}$$

(30)

where $I_{\text{min}}$ is the minimum mean output current value in which the converter operates in CCM for a given value of ripple.

### 4.2 Transistor voltage and current stress

As mentioned earlier, the maximum theoretical voltage stress on every transistor is equal to one third of the input voltage ($V_{in}/3$) except for $Q_{b}$ where is one sixth ($V_{in}/6$), as shown in Figure 3. Regarding the transistor current stress, since in States I and III three parallel loops are created charging each inductor, the current flowing through every transistor equals to one third of the inductor current within $DT_s$. Thus, using Equation (28) and after some mathematical manipulations, the RMS current value on each transistor can be quantified as:

$$I_{\text{Q,RMS}} = \frac{1}{6} \sqrt{\left(\frac{V_{in}^2}{3} + \frac{V_{in}^2(1 - D)^2}{3L_{fs}^2D^2}\right)}$$

(31)

### 4.3 Diode voltage and current stress

As shown in Figure 3, the diode voltage stress depends on the $C_o$ voltage. In the private case of equal duty ratios, the maximum diode stress is equal to one sixth of the input voltage ($V_{in}/6$), allowing the selection of diodes with improved forward voltage and very low reverse recovery losses. In contrast, in this family of converters, the current stress is always high on the output diodes due to the low duty cycle values as well as the inherent nature of the converter where, during $D_oT_s$ and $D_oT_s$ intervals, the current paths charging the complementary inductor are closed through them. However, as shown in Figure 3, the diodes are not equally stressed. Although during $D_oT_s$ all three current loops are closed through $D_o$, during $D_oT_s$ only two current loops are closed through $D_1$. Therefore, the average current value for each diode ($I_{D1}$ and $I_{D2}$) is slightly different and can be calculated from Equation (28) equal to:

$$I_{D1} = \frac{I_o}{2} \left(1 - \frac{D}{3}\right)$$

(32)

$$I_{D2} = \frac{I_o}{2}$$

(33)

### 4.4 Capacitor voltage ripple

During the preceded ideal steady-state analysis, the capacitors were considered as ideal dc voltage sources with their voltage values unchanged within a switching cycle. However, when the transistors are switched-on, the current flowing through them creates a voltage ripple.

In the private case of equal duty ratios, the $C_b$ capacitor is charging and discharging in State I and III respectively, with the whole inductor current, since it is connected in series with both inductors during their charging state. Thus, the voltage ripple on $C_b$ after the end of each state can be obtained by:

$$\Delta V_{C_b} = \frac{\Delta Q}{C_b} = \frac{DI_{L1,2}}{C_b f_s} \Rightarrow \Delta V_{C_b} = \frac{DL}{2C_b f_s}$$

(34)

On the other hand, the capacitors $C_{3,4}$ are charging and discharging with a third of the inductor current each time. Hence, the voltage ripple on them after the end of each state is:

$$\Delta V_{C_{3,4,a,b}} = \frac{DI_{L1,2}}{3C_{3,4,a,b} f_s} \Rightarrow \Delta V_{C_{3,4,a,b}} = \frac{DL}{6C_{3,4,a,b} f_s}$$

(35)

The input capacitors $C_1$ and $C_2$, are charging and discharging with $I_{L1,2}/6$, since the voltage source of the first current path of States I and III consists of two parallel voltage sources, supplying half of the $I_{L1,2}/3$ current each. Therefore, the voltage ripple on them after $D_oT_s$ or $D_oT_s$ intervals, is obtained by:

$$\Delta V_{C_{1,2}} = \frac{DL_{1,2}}{6C_{1,2,a,b} f_s} \Rightarrow \Delta V_{C_{1,2}} = \frac{DL}{12C_{1,2,a,b} f_s}$$

(36)

Finally, the voltage ripple on the output capacitor $C_o$ is generated using the ac component of the output current only, before the capacitor. Since the output current equals to the sum of inductor currents, shifted by $180^\circ$, the output capacitor current ripple can be calculated from Equation (28), after some manipulations:

$$\Delta i_{C_o} = \frac{V_o(1 - 2D)}{L_{fs}}$$

(37)

The voltage ripple on $C_o$ can be calculated using the conventional relation [50]:

$$\Delta V_{C_o} = \frac{\Delta Q}{C_o} \Rightarrow \Delta V_{C_o} = \frac{\Delta i_{C_o}}{8C_o f_{out}}$$

(38)
where $f_{	ext{out}} = 2f_{s}$, since the $i_{L1} + i_{L2}$ ac component has twice the switching frequency, due to the interleaved nature of the converter. By combining of Equations (37) and (38), $C_o$ voltage ripple is equal to:

$$
\Delta V_{C_o} = \frac{V_o (1 - 2D)}{16 L C_o f_s^2}
$$

(39)

5.1 TOPOLOGY HIGHLIGHTS AND COMPARISON

One of the greatest merits of the proposed converter is the flexible step-down voltage conversion ratio, which completely depends on the relation between the duty ratios of each converter phase. Especially in the case of equal duty ratios ($D_a = D_b = D$), the converter has a very high step-down voltage conversion ratio ($D/6$) which along with the extended duty cycle upper regulation limit (0.5), offers a very low but wide output voltage range. Also, the maximum voltage stress on the transistors is significantly lower than the input voltage, i.e. $V_{in}/3$, regardless of the duty ratios relation, allowing the selection of devices with lower breakdown voltage, which might have lower $R_{DSon}$. On the other hand, during switch-on/switch-off transitions, the voltage across transistors and diodes depends on the relation between $D_a$ and $D_b$, but it is lower than $V_{in}/3$ and in case of equal duty ratios, it is six times lower than $V_{in}$, reducing the overall converter switching losses, as well as conduction losses due to the selection of low breakdown voltage diodes with low forward voltage. An additional merit of this converter is the inherent automatic current sharing to its interleaved phases without any additional circuitry or complex control methods since it only depends on the $D_a$ and $D_b$ relation. In the special case of equal duty ratios operation, the output current is uniformly distributed to the two inductors, offering very low output current ripple and, consequently, lower output voltage ripple, as well as simplifying the implementation process with the symmetrical design of the converter.

A comparison of the proposed converter with expanded versions of other recent topologies of the same voltage conversion ratio is presented in Table 1. The proposed converter has the same switch voltage stress as the other similar topologies, except for the coupled inductor converters, where the maximum voltage stress is, generally, higher for all transistors. More specifically, the transistor voltage stress in converter [41] is $V_{in}/2$ but it employs ZVS during switch-on transitions, which allows for high efficiency due to low switching losses, despite the high voltage switch stress. The maximum switch voltage stress of the converters presented in [43] and [44], is also $V_{in}/2$, and in some transistors depends on the coupled inductor turns ratio $n$. In the case of the same voltage conversion ratio ($s = 0.5$), the maximum voltage stress on these transistors is $V_{in}/3$. During switching transitions, however, the switch voltage stress is $V_{in}/4$ for these converters, leading to higher switching losses per transistor. Also, the diode voltage stress depends on the turns ratio $n$, where in the case of same voltage conversion ratio, the diodes are stressed equally to the proposed converter ($V_{in}/6$). Comparing the number of semiconductor components, the number of transistors is the same as in [31, 32, 35–37, 41] and the number of diodes is lower than the other topologies and same to the converter in [44]. Converter [41] does not have any diodes, as the MOSFETs are operating synchronously, substituting the freewheeling diodes. One of the highlights of the converter under investigation is the lowest number of magnetic components, since it only employs two output inductors, reducing the overall cost of the topology. In comparison with [41] and [44], the converter employs more capacitors, but it lacks customized magnetic components with difficult winding process such as coupled inductors/transformers, counterbalancing the overall cost. What is more, the ZVS condition of converter [41] is difficult to achieve at a wide operating range, as it depends on the load current and needs substantial leakage inductance values. High leakage inductance values, however, affects the voltage step-down conversion ratio and increases the converter losses since higher amounts of leakage energy need to be recycled. In terms of control and design complexity, the converter can easily be driven by two phase-shifted pulses, reducing the need of a high amount of independent PWM generators, and thus, a costly microcontroller. Concerning the control algorithm challenges of this converter family, the authors in [25] present the optimal steady-state and transient mode control of the series capacitor buck converter. Finally, since the converter features the highest permitted duty ratio, it can operate in a wider output voltage range, making it suitable for a wide range of applications.

The efficiency performance of the proposed converter compared to other topologies is evaluated using PSpice and is, also, presented in Table 1. The same Si power MOSFET model with low breakdown voltage (IXFH70N30Q3 from IXYS, $V_{DS(max)\text{=}800\text{~V}}$) was selected for all converters and the same diode model RB238NS150 ($V_{f\text{max} = 150\text{~V}}$) from ROHM semiconductor was used for every converter diode. To quantify the inductor copper losses, we assumed 0.2 m$\Omega$/uH, mostly based on measurements conducted in the experimental set-up inductors ($L_2$ = 70 uH). Also, a typical ESR value of 1.6 m$\Omega$ was used for every converter capacitance, selected according to the capacitor models used in the experimental prototype, which are shown later. Finally, it is worth mentioning that since the converters operate in CCM, the core losses are a small portion of the converter losses and are, therefore, neglected. The components used to simulate the converters in PSpice are summarized in Table 2.

The efficiency of each topology is calculated for two operating points: (a) $P_o = 250\text{~W}$, $V_{in} = 500\text{~V}$, $V_o = 12\text{~V}$ and (b) $P_o = 250\text{~W}$, $V_{in} = 500\text{~V}$, $V_o = 24\text{~V}$. As it is shown in Table 1, the proposed converter has higher efficiency compared to the coupled inductor converters [41, 43, 44], mostly due to the lower voltage stress on the transistors. On the other hand, compared to the topologies with higher number of output buck stages (inductor-diode) [31, 32, 35–37], it has slightly lower efficiency, since the RMS current values on the inductors and diodes are higher. It is worth noticing that the converters [31] and [44] cannot operate at $V_o = 24\text{~V}$ due to duty cycle limitations.
### TABLE 1  
Comparison of the proposed converter with similar topologies of the same voltage conversion ratio

| Parameters                              | [31] Expanded | [32] Expanded | [35] Expanded or [36], [37] | [41] \((\alpha = 2)\) | [43] \((\alpha = 0.5)\) | [44] \((\alpha = 0.5)\) | Proposed converter |
|----------------------------------------|---------------|---------------|-----------------------------|------------------------|------------------------|------------------------|-----------------|
| Voltage conversion ratio \((V_o/V_{in})\) | \(D/6\)       | \(D/6\)       | \(D/6\)                     | \(D/6\) \((2/1)^{1/2}\) | \(D/6\) \((4/1)^{1/2}\) | \(D/6\) \((4/1)^{1/2}\) | \(D/6\)         |
| Transistor number                      | 6             | 6             | 3                           | 6                      | 4                       | 4                      | 6               |
| Diode number                           | 6             | 6             | 7                           | 7                      | 5                       | 4                      | 7               |
| Capacitor number                       | 6             | 7             | 3                           | 3                      | 5                       | 4                      | 7               |
| Inductor number                        | 6             | 6             | 3                           | 2                      | 4                       | 2                      | 2               |
| Coupled inductors number               | –             | –             | –                           | 2                      | 1                       | 2                      | –               |
| Phase-shifted pulses                   | 6             | 6 or 3        | 3                           | 4                      | 4                       | 4                      | 2               |
| Maximum allowed duty ratio             | 0.167         | 0.167 or 0.33 | 0.33                        | <0.5                   | <0.5                    | <0.25                  | 0.5             |
| Maximum transistor voltage stress      | \(V_o/3\)     | \(V_o/3\)     | \(V_o/3\)                   | \(V_o/2\)              | \(V_o/2\)               | Two with: \(4/1^{1/2}\) | \(V_o/3\)       |
| with: \(V_o/6\)                        |               |               |                             |                        |                          |                        |                 |
| Transistor voltage stress during on/off transitions | \(V_o/6\) | \(V_o/6\) | \(V_o/6\)                   | \(V_o/4\)              | \(V_o/4\)               | \(V_o/6\)               |                 |
| Maximum diode/synchronous rectifiers voltage stress | \(V_o/6\) | \(V_o/6\) | \(V_o/6\)                   | –                      | \(V_o/4\)               | \(V_o/4\)               | \(V_o/6\)       |
| Efficiency: \(V_o = 12\ V\)          | 91.58%        | 91.72%        | 91.01%                      | 89.48%                 | 87.25%                 | 87.97%                 | 90.43%          |
| Efficiency: \(V_o = 24\ V\)          | N/A           | 95.85%        | 95.09%                      | 94.05%                 | N/A                    | 95.44%                 |                 |
| Input/output common ground            | Yes           | No            | No                          | Yes                    | No                     | Yes                    | No              |
| Cost                                   | High          | High          | Medium-high                 | High                   | Medium                 | High                   | Medium          |

**FIGURE 4  **Efficiency vs number of semiconductor devices per converter for the \(V_{in} = 500\ V, V_o = 12\ V\) and \(P_o = 250\ W\) case

In general, the greater the number of components is, the higher the converter efficiency is, which is illustrated in Figure 4. According to this figure, the proposed converter efficiency stands at the middle: just below of the converters with a higher number of components but significantly above of the converters with, generally, a lower number of semiconductor devices. Hence, the converter selection for each application depends on several factors such as the number of components, the duty ratio range etc., and not only the efficiency.

### 6 EXPERIMENTAL ANALYSIS

To validate the operation of the proposed converter, a 250 W, wide voltage input–wide voltage output range laboratory prototype operating in 100 kHz switching frequency was implemented and is shown in Figure 5. The appropriate PWM pulses to drive the MOSFETs were generated by a TMS320F28377S Development Board by Texas Instruments (TI).

#### 6.1 Converter parameters and practical component selection

The components used to build the prototype and the overall converter parameters are presented in Table 3. The com-
TABLE 2 Component parameters used in the simulation analysis

| Parameters | [31] Expanded | [32] Expanded | [35] Expanded or [36], [37] | [41] (α = 2) | [43] (α = 0.7) | [44] (α = 0.7) | Proposed converter |
|------------|---------------|---------------|--------------------------|-------------|--------------|--------------|-------------------|
| Si MOSFET model | IXYS | ROHM | RB238NS150 | ROHM | RB238NS150 | ROHM | RB238NS150 | ROHM | RB238NS150 |
| Diode model | ROHM | ROHM | ROHM | ROHM | – | ROHM | – | ROHM | – |
| Gate resistance |
| $R_G$ | 13 Ω | 13 Ω | 13 Ω | 13 Ω | 13 Ω | 13 Ω | 13 Ω | 13 Ω |
| Inductance value |
| $L_1$, $L_2$, $L_3$, $L_4$, $L_5$, $L_6$, $L_7$, $L_8$, $L_9$, $L_{10}$ | 70 μH | 70 μH | 70 μH | 70 μH | 70 μH | 70 μH | 70 μH |
| Inductor copper resistance | 14 mΩ | 14 mΩ | 14 mΩ | 14 mΩ | 14 mΩ | 14 mΩ |
| Coupled inductors ratio | – | – | – | $L_p = 200$ μH, $L_d = 50$ μH | $L_p = 50$ μH, $L_d = 200$ μH | $L_p = 50$ μH, $L_d = 200$ μH | – |
| Coefficient factor $k$ | – | – | – | 0.99 | 0.99 | 0.99 | – |
| Coupled inductors resistance | – | – | – | $R_p = 40$ mΩ | $R_p = 10$ mΩ | $R_p = 10$ mΩ | – |
| Capacitance values |
| $C_1$, $C_2$, $C_3$, $C_4$, $C_5$, $C_6$ | 6.6 μF | 6.6 μF | 6.6 μF | 6.6 μF | 6.6 μF | 6.6 μF | – |
| ESR capacitor resistance | 1.6 mΩ | 1.6 mΩ | 1.6 mΩ | 1.6 mΩ | 1.6 mΩ | 1.6 mΩ |
| Frequency | 100 kHz | 100 kHz | 100 kHz | 100 kHz | 100 kHz | 100 kHz |

FIGURE 5 Proposed converter laboratory-built prototype

Component selection was carried out with respect to the key design parameters guidance section (Section 4), as well as with the addition of some extra criteria, such as cost and high efficiency.

Regarding the transistor selection, the STW36N55M5 MOSFETs from STMicroelectronics were selected, which offer low $R_{DS(on)}$ combined with low parasitic capacitors ($C_{gs}$, $C_{ss}$) and, consequently, low current rise ($t_f$) and fall ($t_r$) times. This will allow the reduction of conduction and switching losses, improving the overall converter efficiency. The cost criterion also contributed to the final transistor selection.

Since the switches of the proposed converter are floating, the driving circuitry can be implemented in two ways: either by six (6) independent gate driver circuits with separate isolated power supplies, or by using the bootstrap driving technique in three (3) transistor pairs which are in half-bridge configuration and are switching in complementary fashion: $Q_{1a}$-$Q_{2b}$, $Q_{1b}$-$Q_{2a}$ and $Q_{1c}$-$Q_{2c}$, considerably reducing the isolated power supplies to only three (3). In our case, the first way was preferred and the MOSFET gate drivers ISO5451 by TI were selected, which offer isolation between the PWM microcontroller signals and the power circuit and can directly drive the MOSFETs of the prototype without any additional isolation or amplification stage. They, also, feature negative gate voltage during switch-off and active Miller clamp to avoid undesirable phenomena such as the self turn-on phenomenon, which is a common problem in converters with fast switching operation and floating switches, such as inverters, multilevel inverters etc. [51], [52]. In addition, six isolated dc/dc converters MEV1S1215SC by Murata were used as power supply of the high-side/output stage of the MOSFET drivers.

As proven in Section 4, the diodes are stressed with high current values, calculated from Equations (32) and (33), under the worst case scenario, which is the $V_i = 400$ V, $V_o = 12$ V and $P_d = 250$ W case, where the output current reaches its highest values, resulting to significant conduction losses. Thus, the diodes selected for this application are Schottky, which have low forward voltage and almost zero reverse recovery losses, reducing the transistors current stress due to the reverse recovery current and improving the converter efficiency.
The circuit capacitors were selected with the following criteria: low voltage ripple, low equivalent series resistance (ESR), high current capability and cost. The capacitance values are initially estimated using the relations Equations (34)–(36) and according to the specifications presented in Table 3 regarding the maximum voltage ripple, which is selected to be lower than 2.5% of the nominal value under the worst-case scenario. In our case, the maximum voltage ripple on the capacitors appears at $V_{in} = 300 V$, $V_o = 12 V$ and $P_o = 250 W$. Since currents of high values and frequency flow through the capacitors, MKP capacitors were selected which have very low ESR in a wide frequency range compared to electrolytic capacitors. What is more, to increase each capacitor current capability and reduce ESR even further, each circuit capacitor component consists of several parallel connected capacitors. The final capacitor choice, however, was made with the cost criterion, since they were less expensive than other choices which satisfied the above requirements, despite their high breakdown voltage.

Finally, the inductors were calculated according to the specifications presented in Table 3: The maximum current ripple appearing on the inductors should be $\approx 20\%$ of the output load current in the worst-case. For the inductors, the maximum current ripple appears at $V_{in} = 400 V$, $V_o = 24 V$ and $P_o = 250 W$.

6.2 | Steady-state, start-up and transient state waveforms

The key steady-state waveforms which validate the converter operation are presented in Figures 6–10. The converter operates close to its nominal operating point for equal duty ratios ($D_a = D_b \approx 0.18$), i.e. $P_o \approx 225 W$, $V_{in} = 400 V$ and $V_o = 12 V$. As shown in Figure 6, the inductor $L_2$ is charging when the transistor $Q_{1a}$ is switched-on. Also, the $L_1$ and $L_2$ currents are in $180^\circ$ phase to each other and their average current values are almost equal. Slight deviations to the current ripple might

### TABLE 3 Converter specification and components

| Specifications         | Value                      |
|------------------------|-----------------------------|
| Input voltage $V_{in}$ | 300 to 500 V                |
| Output voltage $V_o$   | 12 to 24 V                  |
| Output power $P_o$     | 250 W                       |
| Maximum inductor current ripple $\Delta I_L$ | 2.2 A (20%) |
| Maximum capacitor voltage ripple $\Delta V_C$ | 1.25 V (2.5%) |

### Parameters

| Parameter                  | Value |
|----------------------------|-------|
| Switching frequency $f_s$  | 100 kHz |

### Components

| MOSFETs $Q_{1a}, Q_{1b}, Q_{1c}, Q_{2a}, Q_{2b}$ and $Q_{2c}$ | STW36N55M5 (Si) |
| MOSFET drivers         | ISO5451 |
| Diodes $D_1$ and $D_2$ | DSSK60-02A |
| Capacitors $C_1$ and $C_2$ | ECW-FD2W225J 6.6 uF/450 V (3 x 2.2 uF) |
| Blocking capacitors $C_3$ and $C_4$ | ECW-FD2W225J 6.6 uF/450 V (3 x 2.2 uF) |
| Series capacitor $C_a$ | ECW-FD2W225J 6.6 uF/450 V (3 x 2.2 uF) |
| Series capacitor $C_b$ | ECW-FD2W225J 19.8 uF/450 V (9 x 2.2 uF) |
| Output capacitor $C_o$ | ECA-1HG331 990 uF/63 V (3 x 330 uF) |
| Inductors $L_1$ and $L_2$ | 70 uH |
| Core type               | RM14, N87 |
| Turns $N$               | 17 |
| Total gap $\Sigma g$   | 1.12 mm |
existing because of the inductance tolerance between $L_1$ and $L_2$. In Figure 7, the $Q_{\text{group}}$ voltage along with $D_2$ voltage waveforms are presented. It is confirmed that the maximum voltage stress on the transistors during steady-state operation equals to $V_{\text{in}}/3 \approx 133.3$ V except for $Q_{1b}$ transistor where is $V_{\text{in}}/6 \approx 66.7$ V. Also, the stress on the transistors during switch-on/switch-off transitions, as well as the diode voltage stress, are also equal to $V_{\text{in}}/6$ offering improved switching losses. The complementary $Q_{\text{2group}}$ and $D_1$, depicted in Figure 8, have the same voltage stress values as $Q_{\text{1group}}$ and $D_2$ respectively. The small voltage ringing appearing on the experimental waveforms is due to the circuit parasitic inductances as well as the very fast switching transitions of the power devices. This must be considered during the converter design process with the selection of devices with higher breakdown voltage.

Also, the capacitor voltage levels for all converter capacitors are presented in Figures 9 and 10. In Figure 9, $V_{C1}$, $V_{C2}$ and $V_{Cb}$ are approximately equal to the theoretical values calculated from Equations (14), (15) and (18) respectively. The other three capacitor voltage levels $V_{C3}$, $V_{C4}$ and $V_{Ca}$ are shown in Figure 10, and are equal to the theoretical ones calculated from Equation (15). A demonstration of the most significant converter voltage and current values for this operating point is presented in Table 4. The comparison between the theoretical and the measured experimental values validates the theoretical analysis of the converter. Some slight deviations from the theoretical values are due to several factors such as the capacitance tolerance, higher practical duty cycle value than the theoretical due to losses etc.

The most significant capacitor voltage levels during start-up are illustrated in Figure 11. Initially, the input voltage is equally shared between the two input capacitors ($V_{C1} = V_{C2} = V_{\text{in}}/2 = 200$ V) and the series capacitor $C_b$ is not yet charged. After the PWM sequence begins, the capacitors will reach their steady-state values without any additional control method or additional circuitry. However, it should be noted that since the input voltage is shared initially between the input capacitors while the other circuit capacitors are not yet charged, the transistors $Q_{1a}$ and $Q_{2a}$ will be stressed with $V_{\text{in}}/2$. Thus, the “practical” voltage stress on the transistors during start-up

### Table 4

| Parameter | Equation ref. | Value | Measured values |
|-----------|---------------|-------|-----------------|
| $V_{C1}$  | (14)          | 266.67 V | 267.32 V |
| $V_{C2}$  | (15)          | 133.33 V | 132.69 V |
| $V_{C3}$  | (15)          | 133.33 V | 132.47 V |
| $V_{C4}$  | (15)          | 133.33 V | 133.94 V |
| $V_{C5}$  | (15)          | 133.33 V | 131.69 V |
| $I_{L1}$  | (27)         | 9.38 A  | 9.21 A         |
| $I_{L2}$  | (27)         | 9.38 A  | 9.45 A         |
| $\Delta I_{L1}$ | (29) | 1.41 A | 1.52 A |
| $\Delta I_{L2}$ | (29) | 1.41 A | 1.52 A |
| $\Delta V_{Cb}$ | (34) | 0.85 V | 1.03 V |
| $\Delta V_{C3,C4,Ca}$ | (35) | 0.85 V | 0.98 V |
| $\Delta V_{C1,C2}$ | (36) | 0.43 V | 0.55 V |
process is $V_{in}/2$ and they should be selected for such breakdown voltage.

Regarding the control, the conventional PI control scheme was selected to regulate the output voltage, which is presented in Figure 12. The only limitation is the differential sensing of the converter output voltage due to the non-common ground feature of the converter. The transient response of the proposed converter for a step change of the input voltage is presented in Figure 13. The initial converter operating point is at $V_{in} = 400$ V, $V_o = 18$ V, and $P_i = 220$ W. Then, the input voltage drops by 100 V (new $V_{in} = 300$ V), leading to a voltage drop on the output voltage and current, but the PI controller acts and corrects the deviation from the reference voltage ($V_o = 18$ V). After, the transient time, a small increase on the pulsating input current is spotted, due to the increased duty cycle values. A more sophisticated approach regarding the optimal steady-state and transient mode control algorithms can be found in [25].

6.3 Efficiency and power loss distribution

Efficiency measurements for different input and output voltages, as well as a wider frequency range, were carried out using the precision power analyser LMG500 of ZES Zimmer manufacturer. The converter efficiency was measured in three different cases: wide output voltage range, unregulated input voltage and variable frequency.

The converter efficiency in the case of wide output voltage range is presented in Figure 14. The input voltage was set to 400 V and the maximum output power goal was set to 250 W. As expected, the efficiency is higher for higher output voltages, reaching 94% in the case of $V_o = 24$ V, due to the lower current stress on the output diodes, as well as because of the lower copper losses on the inductors, since in the case of $V_o = 12$ V, the average diode currents and the RMS current inductor currents are reaching values higher than 10.5 A. For comparison reasons, the efficiency curve for the worst case of operation, i.e. $V_{in} = 500$ V/$V_o = 12$ V is presented as well. Even though the efficiency is the lowest one, it is still higher than 81% at the low power range and up to 87% for the nominal load. More specific, comparing the efficiency with the $V_{in} = 400$ V/$V_o = 12$ V case, it is just 3% lower for small load values and only 1% for the full load operating point.

In the second case, presented in Figure 15, the output voltage was set to 18 V and the parameter was the input voltage. As it is depicted, for high power range the distance between the curves is almost negligible. On the other hand, in the low power range, the efficiency is up to 1% higher for lower input voltages, which signifies that the switching losses due to the higher input voltage are more dominant within this area.
The third case is presented in Figure 16. In this case, the efficiency was measured for three different switching frequencies: 100 and 150 kHz with the same inductors $L = 70 \mu H$ and for 50 kHz with twice the initial inductors ($L = 140 \mu H$). On the one hand, the increase in frequency without changing the inductors showed that the switching losses have linear effect to the converter efficiency, as the two curves are almost parallel to each other for the whole output power range. In contrast, the experiment at 50 kHz with $L = 140 \mu H$, indicated that in low power range, the converter performs better with lower frequency and bigger inductors. Hence, for high output current applications, the selection of a higher switching frequency might be of great merit for the converter efficiency.

The converter power loss distribution in the case of $V_{in} = 400 \text{ V}$, $V_o = 18 \text{ V}$ and $f_s = 100 \text{ kHz}$ is presented in Figure 17. Each type of losses is calculated from the converter losses equations (shown in the Appendix) and expressed as a percentage of the total converter losses for each output operating point. The voltage and current values, as well as other converter parameters used to calculate the losses are presented in Table 5. The calculations were made in MATLAB, where parameters like voltage fall ($\tau_{fu}$) and rise ($\tau_{ru}$) times were calculated using the capacitance variation diagram in STW36N55M5 datasheet, the driver voltage value, the external gate resistance etc. Other parameters like $t_i$, $t_f$, $V_{GSS}$, $V_{GS}$, $R_g$ were slightly readjusted and $R_{DSon}$ was selected at 40 $^\circ$C. The diodes forward voltage and resistance were selected at the same temperature as well.

As expected, the diode conduction losses are the most dominant losses within the whole output power range, due to the high current stress of the output diodes. As Schottky diodes were used, the reverse recovery losses are not taken into account. The transistor switching losses have a significant impact on the converter losses, especially in the low and middle power range, which shows that transistors with low switching times are preferred for this application. The transistor conduction losses percentage is increasing as the output power increases but still, it remains low, due to the low current stress on the transistors as well as the low $R_{DSon}$, such as in our case. Also, as the output power increases, the inductor copper losses become more dominant in the efficiency degradation. Finally, “other losses” represents a sum of all capacitor conduction losses due to their ESR, as well as the magnetic core losses. Within the low power-range, “other losses” are

| Operating point | $P_o$ (W) | $V_o$ (V) | $I_o$ (A) |
|-----------------|-----------|-----------|-----------|
| 1st (50W)       | 51.00     | 17.99     | 2.84      |
| 2nd (100W)      | 102.17    | 18.00     | 5.68      |
| 3rd (150W)      | 149.78    | 18.02     | 8.31      |
| 4th (200W)      | 203.94    | 18.03     | 11.31     |
| 5th (250W)      | 248.22    | 17.98     | 13.80     |
significant mostly due to the magnetic core losses, which however, remain almost constant for the whole power, as it can be seen from Equation (50). On the other hand, as output power increases, these losses are relatively small, due to the selection of capacitors with very low ESR values.

7 CONCLUSION

This work is focused on a new high step-down voltage conversion ratio topology. The converter offers a very high step-down ratio, which in the case of equal duty ratios is six times higher than the conventional buck \((D/6)\) and along with the extended duty cycle regulation limit \((D_{\text{max}} = 0.5)\), which is the highest compared to topologies of the same family and conversion ratio, it offers a wide output voltage range. Despite the use of six transistors, the converter can be driven by only two PWM pulses with \(180^\circ\) phase-shift offering simplicity to the overall control. Another major feature adding to simplicity, is the automatic current sharing between the two interleaved phases, which in case of equal duty ratios is also uniform. In terms of cost, the converter has the lowest number of magnetic components and the second lowest number of semiconductor components compared to familiar topologies of the same voltage conversion ratio.

By employing the switched/series capacitor concept along with the appropriate component interconnection, the voltage stress on the semiconductor devices during switching transitions is reduced, improving the overall converter efficiency by lowering the switching losses. As shown in the experimental analysis, the converter demonstrates exceptional efficiency for a wide input/wide output range of applications, making a perfect fit for high efficiency applications.

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APPENDIX A

The loss equations of each component of the proposed converter are extracted according to the theoretical waveforms presented in Figure 3 and the design guidance equations presented in Section IV. The switching losses calculation was conducted according to the application note [53], which also considers the parasitic capacitors of the transistors, as well as the driver voltage and the transistor gate resistance values. The inductor copper losses are mainly due to the dc resistance, since the inductor current ripple is relatively minor compared to the average current, as well as the use of Litz wire to neglect the skin effect. The core losses are calculated using the iGSE [54] and are proven to be of minor significance for high output power values. Hence, the losses of each component are given from the following equations:

1. Conduction losses per transistor:

\[
\begin{align*}
P_{\text{cond},Q} &= \frac{I_{Q,RMS}^2}{Q} \cdot R_{D\text{son}} \Rightarrow P_{\text{cond},Q} \\
&= \left( \frac{I_o^2}{36} + \frac{V_o^2}{108L^2 f_z} \right) D \cdot R_{D\text{son}} \quad (40)
\end{align*}
\]

2. Switching losses per transistor:

\[
\begin{align*}
P_{\text{sw},Q} &= P_{\text{ON},Q} + P_{\text{OFF},Q} \Rightarrow P_{\text{sw},Q} \\
&= \left( \frac{V_o}{12} \left( \frac{L}{Q} + \frac{V_o (1 - D)}{6d_f} \right) (\tau_h + \tau_f) \right) + \left( \frac{V_o}{Q} \right) \left( \frac{L}{6d_f} \right) (\tau_h + \tau_f) \quad (41)
\end{align*}
\]
where $t_\text{r}$ and $t_\text{f}$ are the current rise and fall times given from the device datasheet, and $t_\text{f}$ and $t_\text{r}$ are the voltage fall and rise times, calculated according to [53].

1. Conduction losses of $D_1$ and $D_2$ diodes:

$$P_{\text{cond,D1}} = I_{D1} \cdot V_{F1} + P_{2\text{D1,RMS}} \cdot R_{D1} \Rightarrow P_{\text{cond,D1}} = \frac{I}{2} \left(1 - \frac{D}{3}\right) V_{F1} + \left(\frac{I^2}{4} \left(1 + \frac{D}{3}\right) + \frac{V_{F1}^2}{12L^2 f_{\text{d}}^2} \left(\frac{D}{3} + \frac{7}{2} D^2 - \frac{23}{7} D + 1\right)\right) R_{D1} \quad (42)$$

$$P_{\text{cond,D2}} = I_{D2} \cdot V_{F2} + P_{2\text{D2,RMS}} \cdot R_{D2} \Rightarrow P_{\text{cond,D2}} = \frac{I}{2} V_{F2} + \left(\frac{I^2}{4} \left(1 + 2D\right) + \frac{V_{F2}^2}{12L^2 f_{\text{d}}^2} \left(2D^3 - D^2 - 2D + 1\right)\right) R_{D2} \quad (43)$$

where $V_{F1}$ and $V_{F2}$ are the forward voltages, and $R_{D1}$ and $R_{D2}$ are the resistances of $D_1$ and $D_2$ diodes, respectively.

1. Reverse recovery losses per diode:

$$P_{\text{reverse,D}} = \frac{V_{F1}}{12} s + \frac{I_{RM} f_{s}}{4} t_\text{r} \quad (44)$$

where $s$ is the diode softness factor, $t_\text{r}$ is the recovery time and $I_{RM}$ is the peak reverse current. These three parameters can be determined from the component datasheet, depending on the application specifications. In our case, these losses are neglected due to the use of Schottky diodes.

1. Losses per input capacitor ($C_1$ and $C_2$):

$$P_{C1,C2} = I_{C1,C2,\text{RMS}}^2 \cdot ESR_{C1,C2} \Rightarrow P_{C1,C2} = \frac{D}{72} \left(I^2 + \frac{V_{a}^2(1 - D)^2}{3L^2 f_{\text{d}}^2}\right) ESR_{C1,C2} \quad (45)$$

where $ESR_{C1,C2}$ is the Equivalent Series Resistance of $C_1$ and $C_2$ capacitors, given in the component datasheet.

1. Losses per blocking capacitor ($C_3$ and $C_4$) and of series capacitor $C_2$:

$$P_{C3,C4,Ca} = I_{C3,C4,Ca,\text{RMS}}^2 \cdot ESR_{C3,C4,Ca} \Rightarrow P_{C3,C4,Ca} = \frac{D}{9} \left(I^2 + \frac{V_{a}^2(1 - D)^2}{3L^2 f_{\text{d}}^2}\right) ESR_{C3,C4,Ca} \quad (46)$$

1. Series capacitor $C_b$ losses:

$$P_{C_b} = I_{C_b,\text{RMS}}^2 \cdot ESR_{C_b} \Rightarrow P_{C_b} = \frac{D}{9} \left(I^2 + \frac{V_{a}^2(1 - D)^2}{3L^2 f_{\text{d}}^2}\right) ESR_{C_b} \quad (47)$$

1. Output capacitor $C_a$ losses:

$$P_{C_a} = I_{C_a,\text{RMS}}^2 \cdot ESR_{C_a} \Rightarrow P_{C_a} = \frac{D}{9} \left(I^2 + \frac{V_{a}^2(1 - D)^2}{3L^2 f_{\text{d}}^2}\right) ESR_{C_a} \quad (48)$$

1. Inductor conduction losses (copper losses $P_{Cb}$):

$$P_{C_b,1,1,2} = I_{RMS,1,1,2}^2 R_{d,Cb} \Rightarrow P_{C_b,1,1,2} = \frac{1}{4} \left(I^2 + \frac{V_{a}^2(1 - D)^2}{3L^2 f_{\text{d}}^2}\right) R_{d,Cb} \quad (49)$$

where $R_{d,Cb}$ is the copper dc resistance.

1. Inductor magnetic losses (core losses):

$$P_{\text{cermalloy,1,1,2}} = V_{e} \left(\frac{1}{T_{c}} \int_{0}^{T_{c}} k_{i} \left[\frac{dB}{dt}\right]^{\alpha} \left[\Delta B \right]^{\beta} - d \right) \Rightarrow P_{\text{cermalloy,1,1,2}} = V_{e} k_{i} \left[\frac{V_{a}(1 - D)}{N A_{d}}\right]^{\beta} \left[\frac{1}{\alpha - \beta} \left(D^{1 - d} + (1 - D)^{1 - d}\right)\right] \quad (50)$$

where $V_{e}$ is the core volume in m$^3$, $N$ represents the number of turns, $A_{d}$ is the effective magnetic cross section in m$^2$, $\alpha$ and $\beta$ are material parameters and $k_{i}$ is calculated using $\alpha$ and $\beta$. 