

A New Perspective of Graph Data and A Generic and Efficient Method for Large Scale Graph Data Traversal

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Abstract — The BFS algorithm is a basic graph data processing algorithm and many other graph data processing algorithms have similar architectural features with BFS algorithm and can be built on the basis of BFS algorithm model. We analyze the differences between graph algorithms and traditional high-performance algorithms in detail, propose a new way of classifying algorithms into data independent algorithm and data correlation algorithm based on their run-time correlation with data, and use this new classification to explain the validity of the methods proposed in this paper. Through a deeper analysis of graph data, we propose a new fundamental perspective on understanding graph data, establishing a link between two basic data structures, graph and tree, and viewing graph data as consisting of smaller subgraphs and edge trees. Small degree vertices are found to be one of important cause of random memory access. Based on this, we propose a general, easy to implement, and efficient method for graph data processing, with the basic idea of treating low-degree vertices and core subgraphs separately, thus significantly reducing the size of random memory access and improving the efficiency of memory access. Finally, we evaluated the performance of the method on three major data center computing platforms (Intel, AMD, and ARM), and the experiments showed that it brought 19.7%, 31.8% and 17.9% performance improvement, respectively, with a performance-power ratio of 282.70 MTEPS/s on the ARM platform, ranking it among the Green graph500 in November 2019. World No. 1 on the big dataset list.

Index Terms — Parallel algorithms, Breadth first search, Graph algorithms, Graph and tree search strategies, Graph500

1 INTRODUCTION

Data can be divided into structured data and unstructured data. Unstructured data is more difficult for a computer to understand as compared to structured data. Graph data is a typical example of unstructured data. Graph is highly abstract and flexible, and can adequately express the connections and dependencies of things in nature. Many problems can be solved efficiently with graph-related algorithms supported by graph theory, such as graph coloring, network routing, and network flow. In addition, graph data processing allows mining and analysis of huge, sparse, and ultra-dimensional associations, and has been widely used in social networks, transportation networks, bioinformatic networks, knowledge graphs, GNN, etc. [1,2,3,4]. However, the scale of graph data increases exponentially, and the number of edges can reach billions, in addition, natural graphs often exhibit a very skewed power-law distribution [5], which brings a great challenge to computing systems at all levels, and how to handle large-scale graph data efficiently has become the focus of research in academia and industry.

The Breadth First Search (BFS) algorithm is a basic graph data processing algorithm, and many graph algorithms can be built based on the BFS algorithm, such as PageRank, Single-Source Shortest Path, Connected Component, Betweenness Centrality, etc. [6]. Many mainstream graph computing frameworks and programming models are now extended into generic forms based on the BFS algorithm model, such as ligra [6], ligra+ [7], Gemini [8], and Grazelle [9]. In addition, numerous other graph processing algorithms are essentially the same as BFS algorithms in terms of their architectural features. These algorithms have significantly different architectural characteristics from those of traditional algorithms for high-performance computational processing (matrix multiplication, FFT, convolution, etc.). Graph processing algorithms have typical characteristics such as poor data locality, low memory access efficiency, low parallelism and poor scalability, and the processing of graph data reflects significant inefficiencies on high-performance computers, with design challenges at all levels of the computer [10]. Top500 ranking is used internationally to measure the performance and power consumption of computers and clusters, profoundly affecting the development of computers at all levels. The benchmark Top500 used is the traditional vector and matrix multiplication and other high-performance numerical algorithms, but there are some drawbacks in using such algorithms to measure computer efficiency. Therefore, the Graph500 ranking was proposed internationally in 2010 to evaluate the performance and power consumption of computers and clusters [11], which uses the BFS algorithm as the benchmark. In summary, if a basic algorithm like BFS can be studied in depth, it will facilitate the research of general graph com-
puting frameworks, improve the performance of other graph processing algorithms, or indirectly provide new research ideas to the research of graph processing frameworks and graph algorithms. It will also promote the development of computers at all levels like Top500.

In this paper, the optimization technique of BFS algorithm under a single node will be systematically introduced. However, these methods treat all vertices uniformly and do not explore the specificity of low-degree vertices, resulting in low-degree vertices bringing a large number of random access to affect performance. We propose a new fundamental way to understand graph data and a fundamental BFS algorithm model to divide the low-degree vertices and core subgraphs to significantly reduce the random access size and improve the traversal efficiency of the graph processing problem. This optimization idea can be implemented both in a generic graph processing framework and on different platforms such as CPU/CPU cluster/GPU/ASIC. The main contributions of this paper are as follows:

- We propose a new algorithm classification approach by analyzing the differences between graph algorithms and high-performance numerical algorithms. And the effectiveness of the methods proposed in this paper is explained using this classification approach.

- We propose a new fundamental perspective of understanding graph data, which can be seen as smaller core subgraphs and edge trees.

- We find that small degree vertices are one of the most important reasons for the high random access of the BFS algorithm (degree 1, etc.), which are typically located on edge trees.

- We propose a new general, easy-to-implement, efficient and large graph data traversal method. The central idea of the method is to treat low-degree vertices and core subgraphs separately. The method improves the performance significantly while maintaining the generalization of the BFS algorithm pattern to build a graph processing framework.

- The method was fully performance evaluated on different computing platforms (Intel, AMD, ARM) and the results show that the method can significantly improve graph processing performance on different platforms. And it achieved the No.1 in the world in the Green graph500 large dataset list in November 2019.

The chapters of this paper are organized as follows. Chapter 2 systematically summarizes the common optimization methods of the BFS algorithm, which are also implemented in this paper. Chapter 3 introduces our proposed algorithm classification approach. Chapter 4 introduces a new fundamental perspective of understanding graph data. Chapter 5 introduces a strong and effective graph data traversal method. Chapter 6 presents the experimental results. Chapter 7 summarizes the full text.

2 RELATED WORK

2.1 Hybrid Optimized

The traditional BFS algorithm is a top-down traversal method that generates a large number of invalid detections later in the traversal. Beamer creatively proposed a Bottom-up algorithm to reduce invalid traversals [12]. As shown in Algorithm 1, the Bottom-up algorithm uses the exact opposite idea to Top-down. It checks whether there are any neighbor vertices in the unvisited vertices that are located in the current layer, and if so, it breaks out of the loop and ends the access to the remaining neighbor vertices, effectively reducing the redundant access overhead. However, the Bottom-up algorithm generates a large number of invalid detections in the previous layers. By combining Top-down and Bottom-up, using Top-down in the early part of the traversal, and switching to Bottom-up in the middle and late part of the traversal, the traversal efficiency can be significantly improved.

Algorithm 1 Direction-optimizing BFS
1: Input
2: \( G = (V,A^{OUT},A^{IN}) \) \( A^{OUT} \) represents the set of outgoing edges of the undirected graph, and \( A^{IN} \) represents the set of incoming edges of the undirected graph
3: vertex \( v \) start
4: Output
5: parent[\( v \)] \( \geq \) the parent info of every vertex
6: \( v \) set
7: parent[\( v \)] \( \leftarrow \) vertex \( v \)
8: \( V^S = \{v \} \) \( \geq \) store the visit state of all vertices
9: \( CQ = \{v \} \) \( \geq \) store the vertices in current level
10: \( NQ \leftarrow 0 \) \( \geq \) store the vertices in next level
11: while \( CQ \neq \emptyset \) do
12: if is top down direction(\( CQ \), \( NQ \), \( V^S \)) then
13: \( NQ \leftarrow \) TOP-DOWN(\( G \), \( CQ \), \( V^S \), parent)
14: else
15: \( NQ \leftarrow \) BOTTOM-UP(\( G \), \( CQ \), \( V^S \), parent)
16: end if
17: swap(\( CQ \), \( NQ \))
18: end while
19: return parent[\( v \)]
20: procedure TOP-DOWN(\( G \), \( CQ \), \( V^S \), parent)
21: \( NQ \leftarrow 0 \)
22: for \( v \in CQ \) in parallel do
23: if \( v \in A^{OUT}(v) \) do
24: \( \text{for } w \in V^S \text{ atomic then} \) \( \text{parent}[w] \leftarrow v \)
25: \( V^S \leftarrow V^S \cup \{w\} \)
26: \( NQ \leftarrow NQ \cup \{w\} \)
27: end if
28: end for
29: end for
30: return \( NQ \)
31: procedure BOTTOM-UP(\( G \), \( CQ \), \( V^S \), parent)
32: \( NQ \leftarrow 0 \)
33: for \( v \in V \setminus V^S \) in parallel do
34: if \( v \in A^{OUT}(v) \) do
35: \( \text{if } v \in CQ \text{ then} \) \( \text{parent}[w] \leftarrow v \)
36: \( V^S \leftarrow V^S \cup \{w\} \)
37: \( NQ \leftarrow NQ \cup \{w\} \)
38: break
39: end if
40: end for
41: end for
42: return \( NQ \)
43: end procedure

2.2 NUMA Optimized

With the increase of the number of cores in a processor, as well as the number of sockets, the single-chip memory interconnect architecture has become a bottleneck, so the NUMA architecture has developed into the dominant architecture. Yasui et al [13] proposed a NUMA graph partitioning method for this feature of the NUMA architecture, which preprocesses the NUMA data based on the features of the top-down and bottom-up algorithms, re-
spective. The method significantly improves the locality of NUMA access to graph data. Equation (1) denotes the set of vertices to which the kth NUMA is divided, where I denotes the number of numa nodes, n denotes the number of all vertices. Equation (2) denotes the adjacency list of out-edge neighborhood to which the kth NUMA is assigned in the top-down algorithm, and equation (3) denotes the adjacency list of in-edge neighbors to which the kth NUMA is assigned in the bottom-up algorithm. In order to improve the overall numa locality, the current layer vertex list, visit information VS, the next layer vertices NQ, and parent array are also numa data partitioned. Algorithm 2 to perform the above NUMA division, top-down and bottom-up algorithm. The method significantly improves the NUMA locality of the graph data.

\[ V_k = \{ V_j \in V \mid j \in I \cdot n, \frac{(k+1)}{I} \cdot n \} \]

\[ A^{OUT}_k(v) = \{ w \mid w \in V_k \cap A(v) \}, v \in V \]

\[ A^{IN}_k(w) = \{ v \mid v \in A(w) \}, w \in V_k \]

Algorithm 2 NUMA-optimized BFS

1. Input
2. \( k \in \{ 0, 1, ..., l - 1 \} \)
3. \( T = \{ T_k \} \)
4. \( G = (G_k) \)
5. \( CQ = (CQ_k) \)
6. \( VS = (VS_k) \)
7. parent = \{ parent_k \}
8. Output
9. \( NQ = \{ NQ_k \} \)
10. procedure NUMA-optimized-TOP-DOWN(G, CQ, VS, parent)
11. \( NQ_k = \emptyset \)
12. for \( w \in CQ_k \) in parallel (\( T_k \)) do
13. \( VS_k \leftarrow V \cup \{ w \} \)
14. \( NQ_k \leftarrow NQ_k \cup \{ w \} \)
15. end for
16. return \( NQ_k \)
17. end procedure
18. procedure NUMA-optimized-BOTTOM-UP(G, CQ, VS, parent)
19. \( NQ_k = \emptyset \)
20. for \( w \in VS_k \) in parallel (\( T_k \)) do
21. \( \\text{if } v \in A^{OUT}_k(w) \) do
22. \( \\text{if } v \in CQ_k \) then
23. \( \\text{parent}_k(w) \leftarrow v \)
24. \( V \leftarrow VS_k \cup \{ w \} \)
25. \( NQ_k \leftarrow NQ_k \cup \{ w \} \)
26. \( \text{break} \)
27. \( \text{end if} \)
28. \( \text{end for} \)
29. \( \text{return } NQ_k \)
30. end procedure

**2.3 Degree Aware Bottom Up**

The Bottom-up algorithm scans all the neighbor vertices that have not been visited in its traversal, and ends the traversal of the remaining neighbor vertices as soon as a neighbor vertex is found in the current layer. The earlier it is terminated, the more the number of neighbor checks can be reduced. Yasui et al [13] experimentally found a correlation between vertex degree and access frequency, the higher the degree of the vertex, the higher its access frequency. As shown in Algorithm 3, splitting the neighborhood adjacency list of each vertex into \( A^{IN}_k \) containing only the highest in-degree neighbor vertices and the remaining in-neighborhood list \( A^{OUT}_k \) arranged in descending order by degree, and splitting the Bottom up algorithm into the processing of both adjacency lists, a large number of vertices will not only be successfully detected in \( A^{IN}_k \), but also \( A^{OUT}_k \) is visited sequentially, lines 12-19 of the algorithm. This not only greatly reduces the traversal of redundant edges, but also improves the locality of data access.

**Algorithm 3 Degree-aware Bottom-up BFS**

1. Input
2. \( k \in \{ 0, 1, ..., l - 1 \} \)
3. \( T = \{ T_k \} \)
4. \( G = (G_k) \)
5. \( CQ = (CQ_k) \)
6. \( VS = (VS_k) \)
7. parent = \{ parent_k \}
8. Output
9. \( NQ = \{ NQ_k \} \)
10. procedure DEGREE-AWARE-BOTTOM-UP(G, CQ, VS, parent)
11. \( NQ_k = \emptyset \)
12. for \( w \in VS_k \) in parallel (\( T_k \)) do
13. \( v \leftarrow A^{OUT}_k(w) \)
14. \( \\text{if } v \in CQ_k \) then
15. \( \\text{parent}_k(w) \leftarrow v \)
16. \( V \leftarrow VS_k \cup \{ w \} \)
17. \( NQ_k \leftarrow NQ_k \cup \{ w \} \)
18. \( \text{break} \)
19. \( \text{end if} \)
20. \( \text{return } NQ_k \)
21. end procedure

**2.4 Static Round-Robin Shuffle**

The natural graph is a power-law graph with extremely unbalanced distribution of degrees and numbers of vertices, which leads to unbalanced multicore load and inefficient thread-level parallelism, and how to fully exploit the advantages of the multicore architecture becomes a fundamental problem. We propose a static round-robin shuffle optimization method that allocates vertices according to their degree by round robin[14]. As shown in Algorithm 4, the vertices are sorted in descending order of degree, and the vertices are assigned to different concurrent entities (node, numa, thread, etc.) by polling to ensure that the high degree vertices and low degree vertices are evenly assigned to each concurrent entities. In practice, if numa data partitioning is used, then consider numa-level static round-robin shuffle data partitioning first, followed by thread-level data partitioning. By the above method, on one hand, the data locality of vertex ordering is maintained. On the other hand, it improves the sequential memory access to vertices in each thread. The overhead caused by frequent dynamic scheduling of threads and the empirical parameter adjustment of block granularity in the dynamic allocation method are avoided. When optimizing for a problem, if it is found that data preprocessing leads to significant load imbalance between concurrent entities, then consider us-
ing the static round-robin shuffle to obtain easily accessible load balancing.

Algorithm 4 Static Round-Robin Shuffle
1: Input
2: row_old ▷ sorted row buffer
3: segmentNum ▷ The number of segments to shuffle
4: Output
5: row: new ▷ new row buffer after shuffle
6: new2old ▷ the map of new id to old id
7: procedure SRSS(old_array, segmentNum)
8: num ← vertexNums/segmentNum
9: for tid = 0; tid < segmentNum; tid + + do
10: for j = 0; j < num; j = j + 1 do
11: row_old[tid * num + j] ← row_old[tid * segmentNum * j]
12: new2old[tid * num + j] ← tid + segmentNum * j
13: end for
14: end for
15: return row: new, new2old
16: end procedure

2.5 Block Search Bottom Up

In the Bottom-up algorithm, each iteration is scanned sequentially through the visit bitmap to find unvisited vertices. After several Bottom-up iterations, the number of unvisited vertices will be drastically reduced and sparsely distributed. Sequential scanning of the visit bitmap is inefficient. We propose a block search based Bottom UP algorithm [15], as shown in Algorithm 5, where 64 vertices form a block and are loaded into a general register so that the binary processing algorithm can quickly find the unvisited vertices in the register. The method also skips access to already traversed vertices at block granularity, lines 27 of the algorithm. In addition, we find that we can compress the three bitmaps used by the Bottom UP algorithm into only two, lines 23-48 of the algorithm, and the entire algorithm kernel is optimized for register processing and read operations on cache, with the write operations on cache reduced to one, occurring after the overall processing is completed on a block-by-block basis, lines 25-46 of the algorithm. In addition, because processing in blocks increases the proportion of effective computations, we merged two separate sections of degree-aware code into one, lines 31-44 of the algorithm. The above optimizations reduce access to cache, improve branching efficiency, and significantly improve the efficiency of single-core computation.

In summary, the above optimizations have been performed from the perspectives of reducing redundant memory access, improving NUMA memory access locality, improving multi-core load balancing, and improving single-core caching and branching efficiency, but have not yet touched an important cause of the severe random memory access of graph applications, the high random memory access due to low degree vertices. We transformed some random memory access into sequential memory access by edge tree optimization, which significantly reduced the impact of random memory access on performance.

Algorithm 5 Block Search Bottom-up optimization
1: Input
2: G = (V, E) = (V, (A^{IN}, A^{OUT}))
3: vertex.start
4: Output
5: parent[N] ▷ the parent info of every vertex
6: procedure BLOCKSEARCHUNVISITEDVERTEX(block, no:visit, pos)
7: unvisited.bit: no:visit ← block: no:visit && (¬block: no:visit)
8: unvisited.mask: no:visit ← ¬bit: no:visit − 1
9: pos ← 1
10: block: no:visit ← block: no:visit ∧ ¬bit: no:visit
11: block: no:visit ← block: no:visit ∧ ¬bit: no:visit
12: return pos, block: no:visit
13: end procedure
14: procedure BSR-BFS(G, vertex.start)
15: visit[bit] ← 0, ∀e ∈ V
16: visit[vertex.start] ← 1
17: parent[vertex.start] ← vertex.start
18: flag ← 0
19: flag ← 1
20: flag ← 1
21: Block:Num ← vertex.num/BlockSize
22: Total vertices divided by block width.
23: while flag == 1 do
24: for i ← 0 to Block:Num in parallel do
25: The current layer is traversed, taking each block in turn.
26: Block:visit ← getBlock(visit, i).
27: Get the access status of the ith block and store it in the block: visit register.
28: Block: visit ← block: visit
29: while block: no:visit ∧ 0 do
30: Break vertex: visit = block: visit
31: The current block has untraversed and undetected vertices.
32: pos ← BLOCKSEARCHUNVISITEDVERTEX(block: no:visit)
33: w − i × Block:Size + pos
34: v ← A^{IN}(w)
35: if getBit(visit, v) then
36: block: visit ← block: visit || (l < pos)
37: parent:vis ← v
38: flag ← 1
39: flag ← 1
40: break
41: end if
42: end for
43: end if
44: end while
45: writeBlock(visit: new, block: visit)
46: Write the updated visit state of the ith block back to visit: new bitmap.
47: end for
48: read(visit: new)
49: end while
50: return parent[N]
51: end procedure

3 DATA RELEVANCE OF THE ALGORITHM

Graph algorithms (BFS, PageRank, etc.) and traditional high-performance numerical algorithms (matrix multiplication, FFT, convolution, etc.) have completely different architectural features, but there is no work yet to explain why this difference arises. The work on parallel tuning is prone to some optimization pitfalls. In the following, we propose a new classification of algorithms to explain the difference between these two classes, which is used later to illustrate the effectiveness of edge-tree graph traversal proposed in this paper.

3.1 Data Independent Algorithm (DIA)

Definition: The runtime memory access behavior of an algorithm does not depend on the specific value of any memory cell.

Memory ordering of data-independent algorithms is determined at compile time. The memory ordering does not change regardless of the data values stored in the
memory cell. This good property leads to the fact that such algorithms can be easily accelerated by the compiler or by manually adjusting the order of memory accesses to improve the regularity and locality of the accesses, and can be easily accelerated using hardware. Traditional high-performance numerical algorithms (matrix multiplication, FFT, convolution) fall into this category, which are well established. As shown in Algorithm 6, the common optimization methods are loop unroll, loop exchange, tile, SIMD, prefetching, and systolic array, etc.

Algorithm 6 Matrix Multiplication

1: for i = 0; i < N; i + +
2: for j = 0; j < N; j + +
3: for k = 0; k < N; k + +
4: c[i][j] ← c[i][j] + a[i][k] * b[k][j]
5: end for
6: end for
7: end for

3.2 Data Correlation Algorithm (DCA)

Definition: The runtime memory access behavior of an algorithm depends on the specific value of a certain storage unit.

The intrinsic feature of data correlation algorithms is that the runtime state depends on some stored value, which leads to the fact that optimization methods for data-independent algorithms are generally ineffective for data correlation algorithms. Optimization of data-correlation algorithms is more difficult than optimization of data-independent algorithms. A typical representative of this class of algorithms is the graph algorithm (BFS, SSSP, PageRank, etc.). In addition to graph algorithms falling into this category, a large number of applications in data centers also fall into this category, and data centers are generally more focused on high throughput, hence this paper uses the term high throughput computing (HTC) as a counterpart to high performance computing (HPC). There are two points to note, 1) Although a large number of data correlation algorithms have random access to memory features, data correlation algorithms do not always have random access features to memory. Depending on the contents of the storage unit, data correlation algorithms can exhibit both sequential and random memory access features. The first for loop in Algorithm 7, if the value of childld in edgelist is continuously increasing, then the parent is sequentially accessed, and vice versa. This is a very important difference between data correlation and data-independent algorithm. This means that if an algorithm is of the data correlation type, the same piece of code does not need to be changed at all, and the memory order in which the algorithm is accessed can be changed simply by changing the arrangement of the data, leading to different performance results. 2) Random access data correlation algorithms are not necessarily cache-unfriendly. If the range of random accesses is smaller than the capacity of the cache, these random accesses can also be hit in the cache. Such random accesses still have good cache locality. The second for loop in Algorithm 7, although the access to the bitmap is randomly accessed, still has good cache locality because the bitmap can be placed in the cache entirely.

Therefore, the cache friendliness of the data correlation algorithm is used here to further subdivide the algorithm, defined as cache-friendly and cache-unfriendly data correlation algorithms, respectively.

Cache Friendly Data Correlation Algorithm (CFDCA)

Cache-friendly data correlation algorithms still have good memory access locality and can be further divided into sequential access cache-friendly data correlation algorithms and random access cache-friendly data correlation algorithms. The nature of cache-friendly data correlation algorithms approximates data-independent algorithms, and the same optimization methods for data-independent algorithms generally apply to cache-friendly data correlation algorithms. However, compilers do not perform compiler-level automatic optimizations like data-independent algorithms, because current compilers can only perform conservative optimizations and are not able to recognize runtime memory access locality. For cache-friendly data correlation algorithms, programmers are generally required to manually specify compiler optimization strategies to improve performance.

Cache Unfriendly Data Correlation Algorithm (CUDCA)

Cache-unfriendly data correlation algorithms exhibit truly random accesses, with very fine granularity, such that the range of addresses for two adjacent accesses exceeds the capacity of the cache. The characteristic makes memory access behavior difficult to predict at compile and run time. Graph processing algorithms fall strictly into this category. Optimization methods for data-independent algorithms are generally based on the regularity of memory access, and the locality of memory access can be improved by simply changing the control flow, but these methods do not change the true random memory access properties of data correlation algorithms after they are used to cache-unfriendly data correlation algorithms. Thus, to obtain better memory access locality, cache-unfriendly data correlation algorithms generally rely heavily on data preprocessing. Most of the optimization methods used in the related work need to be implemented with the corresponding data preprocessing.

In summary, A detailed comparison of the above algorithms is shown in TABLE 1. From the above analysis, we can establish a clearer framework for algorithm optimization, avoid some optimization pitfalls. At the same time, we can also see that cache-friendly data correlation algorithm is a special class of data correlation algorithm, which is intrinsically data correlation algorithm, but are similar in nature to data-independent algorithm, and data-independent algorithm optimization tools can generally be used directly for cache-friendly data correlation algorithm. Cache-friendly data correlation algorithm appears to bridge the gap between cache-unfriendly data correlation algorithm and data-independent algorithm. This inspires us that if we are able to transform cache-unfriendly data correlation algorithm into cache-friendly data correlation algorithm, then we can make use of our familiar optimization methods and experience related to data-independent algorithm.
4.2 Edge Tree View of Graph

Our further analysis shows that the graph data has not only a large number of small degree vertices, but also a large number of low degree vertices. Several low degree vertices form a tree, and the graph data has a large number of such trees, which we define as edge tree (ET). As shown in Fig. 1, the left and right graphs are the same graph. The graph on the right simply adjusts the position of the lower vertices, the graph on the left looks very chaotic, and the graph on the right has structure. We define this kind of graph on the right as an edge tree view of the graph (ETVG). The original graph can be understood as consisting of core subgraphs and a large number of edge trees.

After defining the concept of edge tree, we mark the vertices in the graph, which can be divided into five categories:

- Core Internal Vertex (CI)
  Such vertices are located in the core graphs and are not connected to any edge trees. Such vertices are shown in white on the diagram.
- Core Edge Vertex (CE)
  Such vertices are located in the core graphs and are connected with some edge trees. Such vertices are shown in red on the diagram.
- Tree Internal Vertex (TI)
  Non-leaf vertices on the edge trees. Such vertices are shown in green in the diagram.
- Tree Leaf Vertex (TL)
  The leaf vertices on the edge trees. That is, vertices of degree 1 in the original graph. Such vertices are indicated in blue in the graph.
- Vertex Zero (VZ)
  Isolated vertices in the original graph. Such vertices are shown in black in the diagram.

4.3 Edge Tree Vertex Classification Algorithm

The goal of the edge tree vertex classification algorithm is to classify the vertices in the original graph, labeled as CORE_INTERNAL, CORE_EDGE, TREE_INTERNAL, TREE_LEAF, and VERTEX_ZERO, respectively. As shown in Algorithm 8, initially all vertices are of type CORE_INTERNAL by default, and then they are marked from the bottom up from the leaf vertices. Vertices of degree 1 and 0 are marked with TREE_LEAF and VERTEX_ZERO, respectively, and then the TREE_LEAF vertices and their neighbors are deleted from the graph. Then select a vertex of degree 1 or 0, mark it as a vertex of type TREE_INTERNAL. Then delete the vertices of type TREE_INTERNAL and their

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Algorithm 7 Traverse EdgeList Only Leaf Vertex[TEOLV]

1. Input
2. struct < src, dst > edgeList[M]
3. Output
4. parent[N] => the parent info of every vertex
5. 6. procedure TEOLV(edgeList, parent)
7. /*
8. for i = 0; i < M; i++ do
9. if (i != parent[i]) then
10. parent[i] = edgeList[i].src
11. else
12. parent[i] = edgeList[i].dst
13. end if
14. end for
15. */
16. return parent[0]

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| TABLE 1 The Comparison of Algorithm Type |
|------------------------------------------|
| Data Dependency | DIA | CFDC | CUDA |
| Cache Locality | High | High | Low |
| Random Access | Low | Low | High |
| Load Balancing | Easy | Easy | Hard |
| Compiler Optimization | Auto | Set Manually | Can’t |
| CPU Friendly | Yes | Yes | No |
| Tuning Difficulty | Easy | Easy | Hard |
| Typical Application | GEMM/FFT | BFS/PageRank |
| Computing Category | HPC | HTC/HTC |

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4. Edge Tree View of the Graph

4.1 Small Degree Vertices and Random Access

The optimization of data correlation algorithms is closely related to the properties of the data. A change in the data layout will change the memory access behavior of the algorithm. In many cases, a change in the data layout will result in a larger performance improvement than the optimization of the algorithm itself. Some related work has exploited the relevant properties of power-law graphs with large degree vertices [13],[14], but no related work has investigated the small degree vertices. We find that small degree vertices are also one of the important cause of the high random access to the graph processing. Nature graph conforms to skewed power-law degree distribution [5],[17]. Most vertices have relatively few neighbors while a few have many neighbors. The kronecker graph [18], a common power graph generator, is heavily used in the graph research field and the Graph500 uses it as an input graph as well. As shown in TABLE 2, the Kronecker graph (SCALE=26) has 63% of small vertices, with 51.1% of isolated vertices(VZs) and 12.4% of vertices with degree 1 (TLs). In the graph processing algorithm, if the neighbor vertices of a vertex contain small degree vertices, then obviously the memory access of two neighbor vertices adjacent to each other is probabilistically true random access. And this random memory access is fine-grained in terms of vertices. This problem will become more worse under the multi-core, NUMA architecture of the existing architecture, and the existing architecture faces severe challenges.
neighbor edges from the graph, and repeat the process until there are no vertices of type TREE_INTERNAL, and complete the marking of the vertex of type TREE_INTERNAL. Finally, by comparison with the original graph, if the degree of the vertex has changed, then the vertex is marked as a vertex of type CORE_EDGE. The remaining vertices are vertices of type CORE_INTERNAL, which are set initially and do not need to be processed. By controlling the height of the edge tree, different MH divisions are obtained. MH = 0 division, only vertices of type TREE_LEAF and VERTEX_ZERO are marked. There are no vertices of type TREE_INTERNAL in the edge tree view. We call this special case as edge leaf view of graph (ELVG). The algorithmic complexity of the preprocessing at this point is O(V).

Algorithm 8 Edge Tree Vertex Classification Algorithm

1: Input
2: G = (V,E)
3: if height of edge tree to be classified, default is 0 classify leaf nodes only-1 indicates a fully preprocessed classified edge tree of the original graph
4: Output
5: vertex_type[N] // array of storing the type of every vertex
6: procedure ETVCAG()
7: vertex_type[N] := CORE_INTERNAL
8: memmap(vertex.num,pre,G.vertex.num,N) // copy array of storing the number of neighbors
9: memmap(vertex.num,new,G.vertex.num,N) // copy array of storing the number of neighbors
10: flag = 0 // 0 indicates that there are no vertices in the current height in the edge tree
11: for i ∈ V do // classify TYPE.ZERO and TREE.LEAP
12: if vertex.num,pre[i] == 0 then
13: vertex.type[i] := TREE.ZERO
14: else if vertex.num,pre[i] == 1 then
15: vertex.type[i] := TREE.LEAP
16: if vertex.num,new[i] <= vertex.num,pre[i] then
17: vertex.type[i] := TREE.INTERNAL
18: for each v adjacent to w do
19: vertex.num,new[w] := vertex.num,new[w] + 1
20: end for
21: flag := 1
22: end if
23: for i ∈ V do
24: height.current := height.current + 1
25: while flag = 0 do // classify TREE.INTERNAL
26: flag := 1 // start processing vertices in edge tree of height, current
27: for i ∈ V do
28: if vertex.num,pre[i] == height.current then
29: vertex.type[i] := CORE_INTERNAL // (vertex.num,pre[i] == 0 ∨ vertex.num,new[i] <= vertex.num,pre[i]) then
30: vertex.type[i] := TREE.INTERNAL
31: for each v adjacent to w do
32: vertex.num,new[w] := vertex.num,new[w] + 1
33: end for
34: flag := 1
35: end if
36: end for
37: height.current := height.current + 1
38: end while
39: for i ∈ V do
40: if vertex.type[i] == CORE_INTERNAL // G.vertex.num[i] then
41: vertex.type[i] := CORE_EDGE
42: end if
43: end for
44: return vertex_type[N]
45: end procedure

4.4 Properties of The Edge Tree View

1. The two types of vertices, Core Internal Vertex and Core Edge Vertex, make up the core graph, which is a smaller subgraph of the same nature as the original graph and still has true random access properties.

2. Tree Internal Vertex and Tree Leaf Vertex make up the edge trees. These types of vertices, although contributing heavily to random access in the original graph, have the potential to be optimized for sequential memory access because the tree is a special data structure.

3. At most one Core Edge Vertex is connected to the root vertex of each edge tree. As shown in Fig. 1, each edge tree corresponds to a unique Core Edge Vertex (red vertex).

4. Vertices in each edge tree are not connected to any Core Internal Vertex type.

5. The edge tree has all the properties of a tree structure. The parent vertex of each vertex is unique.

4.5 The Height of Edge Tree

Given a graph G, if the fathers are sequentially partitioned into edge trees starting from the leaf vertices, the number of vertices in the core graph gradually decreases and the number of vertices in the edge tree gradually increases, and eventually the two sets converge to some fixed value. Define the maximum height of all edge trees at this point as the Peak Height(PH) of the edge tree of the graph. Note that the PH of the kronecker graph is very small, e.g. a kronecker graph with scale=26 has a PH of 2. For a given Max Height(MH, less than or equal to PH), divide the vertices in the graph as far as possible onto the edge tree, but ensure that the maximum height of all edge trees does not exceed MH, called the MH edge tree division of the graph. MH = 0 is a special case where only leaf vertices are divided onto the edge tree. For any graph, get the relevant parameters in its edge tree view and many optimization issues will become clear. For example, Fig. 2 are the all MH divisions of Fig. 1. TABLE 2 is the Kronecker graph with scale=26, edgefactor=16, and the number of vertices of each type under different MH divisions. We can see that the proportion of TL and VZ is very high, accounting for 63%, TI type accounting for 0.03%. Only 37% of the vertices in the core graph (CI and CE). TABLE 3, MH=2, scale=26 graph contains a total of 2484171 Core Edge Vertex connected edge trees, these edge trees contain a total of 8332878 vertices, on average each edge tree contains 3 vertices, the largest edge tree contains 9685 vertices, the smallest edge tree contains 1 vertex. This indicates that the edge tree is severely sparse and is an important cause of random access to the memory. This inspires the possibility of special treatment of these low-degree vertices in edge trees individually to improve performance.

| MH | CI  | CE  | TI  | VL | Total |
|----|-----|-----|-----|----|-------|
| 0  | 21970533 | 2502108 | 208 | 8332198 | 34304025 |
| 1  | 21966322 | 2484225 | 22094 | 8332198 | 34304025 |
| 2  | 21966312 | 2484171 | 22158 | 8332198 | 34304025 |

TABLE 3 The Distribution of the Number of Vertices Contained in All Edge Trees Connected by Core Edge Vertex in the Kronecker Graph with Scale=26,Edgefactor=16, MH=2

| Edge Tree Number | Ave | Max | Min | Total |
|------------------|-----|-----|-----|-------|
| 2484171          | 3   | 9685| 1   | 8332878 |
5 Edge Tree Traversal Algorithm

The original graph in the edge tree view is partitioned to consist of some core subgraphs and edge trees. Considering that the father of the leaf vertex can be determined before the algorithm run, the father information of the leaf vertex can be made into a lookup table in the data pre-processing stage, so that the algorithm only needs to process the core graphs and not the leaf vertices. Thus it improves the performance of the BFS algorithm. However, there are two key problems with this approach: 1) The leaf vertices are not re-visited during the run of the algorithm, losing the generality of the BFS algorithm as a basic pattern for graph processing algorithms. Some graph processing algorithms need to update the state of all vertices in each iteration, such as PageRank, etc. 2) The performance improvement brought by the above approach may come from this part of the removed access to the memory and that not an optimization of random memory access. Is there a method that simultaneously processes leaf vertices during graph algorithm traversal that guarantees both generality and high performance? We propose an edge tree breadth-first traversal method to solve this problem, which is a method that guarantees both generality of the BFS algorithm model and high performance.

5.1 Data Structure and Layout

5.1.1 Master Data Structure

The data structure of graph is stored in the well-known Compressed Sparse Row (CSR) format, adopted by most graph algorithms and graph processing systems. The CSR consists of two lists as shown in Fig. 3. The adjacency list stores the neighbor information and its size is bounded by the number of edges. In the row list, it stores the first neighbor’s pointer of each vertex. The CSR format allows streaming access of all neighbors for each vertex. The main data structure still uses the CSR. The vertices in the edge tree view can be divided into two categories, one is the vertices in the core subgraph, which is further subdivided into two types CORE_INTERNEL and CORE_EDGE. The other category is the vertices in the edge tree, further subdivided into the types TREE_INTERNEL, TREE_LEAF, and VERTEX_ZERO. The data layout in the CSR is as follows.

- **Row array.** Place the vertices in the core subgraph to the left of Row and the vertices in the edge tree and isolated vertices to the right of Row. As shown on the right side of Fig. 3, a, d, and e are the vertices in the core subgraph placed to the left, and b, f, and c are the vertices in the edge tree placed to the right.
- **Col array.** All neighbor vertices of each vertex are also separated by type, with vertices in the core subgraph placed on the left and vertices in the edge tree on the right. As shown on the right side of Fig. 3, d and e of the neighbors of vertex a are the vertices in the core subgraph to the left and b and f are the vertices in the edge tree to the right.

The above proposed is a layout idea, the BFS algorithm comes without further adjustment of the layout. Other algorithms can further adjust the layout according to the characteristics of the algorithm. This data structure and layout has the following advantages.

- Guaranteed generality and compatibility of data structures and graph algorithms. The data structure is still in the CSR format, just adjusting the layout of the data in the CSR, and the other graph algorithms and optimizations work with little to no change. Restoring the layout is also easy.
- The storage of vertices in all edge trees is continuously incremental and can be processed sequentially using the CFDCA algorithm. Previous CSR data layout in which vertices in the edge trees and vertices in the core graphs are stored together in a mixture, cannot process the vertices in the edge tree sequentially. In our proposed layout, all the vertices in the edge tree are on the right side of the CSR and their numbering is continuous, enabling sequential processing using the CFDCA algorithm to improve performance.
- There is little impact on the performance of different optimization methods. For example, the degree-aware optimization mentioned in the related work requires that the high-degree vertices in each neighborhood are on the left and the low-degree vertices are on the right, and the layout here also satisfies this condition, with the left core being the high-degree vertices in the core graph and the right side being the low-degree vertices in the edge tree.

- Low data pre-processing complexity and cost. Although graph applications do not generally require performance for data preprocessing, the data preprocessing of the edge tree algorithm proposed in this paper still has a low algorithmic complexity. The edge tree vertex classification algorithm has a low algorithmic complexity. The algorithmic complexity of adjusting the CSR layout is \(O(V+E)\) when the type of vertices is obtained.Moreover, these preprocessing algorithms are cache-friendly data correlation algorithms, easy to parallelize and easy to optimize.

5.1.2 Storage and Representation of Edge Trees

The main data structure and layout are designed with the idea of ensuring generality and compatibility. The edgelist data structure is used to store the edge tree. The edge trees are stored using the edgelist data structure. The edgelist represents the edges in the edge trees as arrays of elements (src,dst). The src and dst represent the starting...

Fig. 3 The Data Structure and Layout of Edge Tree View
5.2 Edge Tree BFS Algorithm (ET-BFS)

As shown in Algorithm 9, if the start vertex of the traversal is on the edge tree, the vertex is of type TREE_INTERNAL or TREE_LEAF; then it is necessary to first traverse the edge tree alone and return the corresponding CORE_EDGE vertex of the edge tree (this vertex is unique by property 3). For MH=0 division, only leaf vertices are marked, so this step can be omitted. Next, the core subgraphs and the edge trees are processed separately. The BFS_CORE indicates any BFS algorithm, except that the size of the processing graph data is changed from the original graph to the smaller core subgraph, and the vertices in the edge trees will no longer participate in the processing. Then, the processing of vertices in the edge trees can be completed by simply traversing the edge tree edgelist through sequential memory access. The core idea of the method is to treat vertices in the edge tree (vertices of low degree) and vertices in the core subgraphs differently, using the CSR data structure to process vertices in the core subgraph and using the edgelist data structure to process vertices in the edge tree. The previous approach did not deeply recognize the different nature of the vertices in the graph and treated all vertices uniformly, resulting in low-degree vertices bringing a large number of random memory access and not taking advantage of the potential for sequential memory access that exist in the low-degree vertices.

5.3 Edge Tree Processing Algorithm

As shown in Algorithm 10, the processing of edges in all edge trees is achieved by traversing the edgelist. Some edge trees will not be traversed during the traversal process because they are not located on the connected subgraph where the start vertex is located and belong to another connected subgraph. However, the graph500 requires that the vertex with a non-empty parent value must be on the traversal spanning tree of the starting vertex as the root vertex, so it needs to determine whether the edges exist in edgelist are on the traversal spanning tree edge of the starting vertex as the root vertex, only the vertices that can be traversed need to update their father information. The core_edge indicates the Core Edge Vertex of the edge tree where (src, dst) is located. If the core_edge has been visited, then it means that dst can be traversed and its father can be updated. A caveat here is that the dst in edgelist needs to be arranged in ascending order and the bitmap can be filled into the cache so that the algorithm can become a CFDCA type algorithm. The cache is localized well and easy to optimize. Our proposed CSR storage layout naturally makes dst ascending because the numbering of all vertices in the edge trees of a CSR data structure is incremented serially, and the vertex numbering in edgelist is the numbering of the CSR, so the dst values of the neighboring positions in edgelist are also incremented serially. This is a very important point, because if the dst of adjacent positions in the edgelist is not continuously incremented, then the accesses to the parent array will not be continuous, and Algorithm 10 will degenerate into a CUDCA type algorithm, still with a large number of random accesses, which experiments show will not lead to performance improvement. For the edge leaf view, MH=0, and only leaf vertices are extracted, then the algorithm can be judged directly using src instead of core_edge, as shown in Algorithm 7 TEOLV, which has a simpler form. According to the power-law rate nature of the natural graph, a large number of vertices in the edge trees are leaf vertices, such as TABLE 2 and TABLE 3. TEOLV algorithm form is not only simple, but also experimental results show that it has high performance at the same time.

Algorithm 9: Edge Tree BFS Algorithm

1. Input
2. $G=(V,E)\rightarrow$ (Core.Tree)
3. struct $<src,dst,...>\rightarrow$ edgelist[M]
4. vertex.start $\rightarrow$ the starting vertex of the traversal
5. Output
6. parent[N] $\rightarrow$ the parent info of every vertex
7. 8. procedure ET-BFS(G, edgelist, vertex.start)
9. if vertex.start $\rightarrow$ Tree then
10. (vertex.start, new, parent) $\rightarrow$ traverse.return/core.edge(G, vertex.start)
11. traverse the edge tree where the start vertex located and return the corresponding CORE.EDGE vertex of the edge tree.
12. vertex.start $\rightarrow$ vertex.start, new $\rightarrow$ update the vertex start
13. end if
14. BFS.CORE(G, vertex.start) $\rightarrow$ CUDCA algorithm. Just process core graph
15. TRAVERSE.EDGELIST(edgelist) $\rightarrow$ CFDCA algorithm. Just process edge trees
16. return parent[N]
17. end procedure

Algorithm 10: Traverse EdgList Edge Tree (TEET)

1. Input
2. struct $<src,dst,core.edge>\rightarrow$ edgelist[M]
3. Output
4. parent[N] $\rightarrow$ the parent info of every vertex
5. 6. procedure TEET(edgelist, parent)
7. for $i=0;i<M; i++$ do $\rightarrow$ CFDCA algorithm
8. parentId $\rightarrow$ edgelist[i].src
9. childId $\rightarrow$ edgelist[i].dst
10. core.edge $\rightarrow$ edgelist[i].core edge
11. if bitmap(core.edge) then $\rightarrow$ random memory access but cache
12. friendly
13. parent[childId] $\rightarrow$ parentId $\rightarrow$ sequential memory access, if the children are in ascending order
14. end if
15. end for
16. return parent[N]
17. end procedure
6 Experimental Evaluation

6.1 Experiment Setup

In order to evaluate the validity of the methodology, we used computing platforms provided by the three leading vendors of supercomputing and data center, Intel, AMD, and ARM. As shown in TABLE 4, for their specific configurations. The Intel E5-2683 is mainly used to evaluate the effectiveness of the method, the AMD EPYC 7452 is the latest processor for evaluating the maximum performance, and the ARM processor is used to evaluate the potential of the ARM architecture as an emerging server architecture. Unless otherwise noted, both Intel and AMD are compiled using the icc 19.0.0 compiler and ARM processors are compiled using gcc 8.3.0. The test dataset was generated using kronecker graph generator from the Graph500 benchmark with the parameters set to default values (A = 0.57, B = C = 0.19, D = 0.05). The kronecker graph generator can be adjusted by entering parameters such as scale and edgefactor, where the scale parameter indicate the scale of the vertices of the graph, and the edgefactor indicates the average degree of each vertex, where the default value of Graph500 is 16. The generated graph data satisfies the power-law distribution and contains the number of vertices in $2^{scale}$ and the total number of edges in $2^{scale*edgefactor}$. According to Graph500, the performance is represented by giga-traversed edges per seconds (GTEPS). 64 source vertices are randomly selected to execute the BFS algorithm, and then the average of the results from these 64 vertices is taken as the final performance.

| Platform | Intel | AMD | ARM |
|----------|-------|-----|-----|
| Operation System | CentOS7 | CentOS7 | CentOS7 |
| CPU | Xeon E5-2683 | EPYC 7452 | HTC Centriq |
| CPU speed | 2.00 GHz | 2.35 GHz | 2.30 GHz |
| Socket(s) | 2 | 2 | 1 |
| Cores per socket | 14 | 32 | 40 |
| L3 cache | 35 MB | 128 MB | 50 MB |
| Memory capacity | 384 GB | 256 GB | 384 GB |
| Memory type | DDR4 | DDR4 | DDR4 |
| TDP | 120 W | 155 W | 110 W |

TABLE 4 Configure information

6.2 Performance of Different MH Divisions

The machine used for the experiments in this section is the E5-2683, and this section uses all the optimization methods that is Hybrid+RmZero+RoundRobin+NumaAware+DegreeAware+BlockSearch+ET-BFS. The graph is set to scale=26, edgefactor=16 to study different MH divisions’ performance. As shown in Section 4.5, the higher the MH, the more vertices will be partitioned to the edge tree. The PH of the graph for SCALE=26 is 2. MH=0 is a special case and can also be used to process leaves using Algorithm 7 TEOVL, which is also used here as a comparison. The figure shows that the performance is almost identical under different MH divisions. This is due to the small percentage of TI vertices, which are basically leaf vertices. Considering the simplicity of the TEOVL algorithm, TEOVL is chosen as the object of study in the latter part of the paper.

6.3 Strong Efficiency

The trigger conditions for the validity of data-correlation algorithm and data-independent algorithm are also different. The optimization methods of a data-independent algorithm generally leads to performance improvements on top of other optimization methods, but some optimization methods of a data-correlation algorithm can only show an optimization effect when paired with a particular optimization method. A data correlation algorithm is said to be strongly effective if the optimization method of the algorithm can further improve performance on the basis of most other optimization methods. This section evaluates the two effectiveness of the edge tree algorithm by adding edge tree optimization to any optimization method. The machine used in this section is E5-2683. Kronecker graph with SCALE=26 and Edgefactor=16. As shown in Fig. 5, each element of the X-coordinate represents the added optimization relative to the previous one. The first column of each X-coordinate represents the previous performance. The second column represents the addition of the full edge tree optimization (BFS_CORE and TEOVL) to it, and the third column represents the addition of TEOVL to the first column of Hybrid optimization only, the second column indicates the use of Hybrid+BFS_CORE, and the third column indicates Hybrid+BFS_CORE. As for RoundRobin, the first column indicates the use of Hybrid+RmZero+RoundRobin optimization, and the second column indicates the use of Hybrid+RmZero+RoundRobin+BFS_CORE. The diagram contains a wealth of information to see that edge tree algorithm are strongly effective algorithms that can deliver performance improvements based on any optimization on methods.
6.4 Overall Performance Analysis

The machines used for the experiments in this section are E5-2683, HTC Centriq and EPYC-7452, and the performance under different scales such as Fig. 6 was tested using kroncker graph with edgefactor = 16, where PRE indicates previous optimization, Hybrid+RmZero+RoundRobin+NumaAware+DegreeAware+BlockSearch. The AMD EPYC 7452 performance values correspond to the right Y-axis, the rest of the platforms correspond to the left Y-axis.

![Fig. 6 Overall Performance](image)

**Big Graph Data Efficiency**

Many optimization methods are effective for smaller scale graphs, but are ineffective for processing large graphs, and algorithms that are effective for large graphs are more difficult to design. A major reason for this is that as the size of the graph changes, the space required to represent the bitmap of the vertices also becomes larger, exceeding the capacity of the cache. Our proposed EdgeTree optimization algorithm still shows acceleration for large graphs because it decomposes the large graph into smaller core graphs. As in Fig. 6, on all platforms, the 28, 29, and 30 graphs show performance improvements relative to PRE.

**Performance Upper Bound**

The edge tree processing algorithm is of CFDCA type and easy to optimize. Different graph processing algorithms can tune the edge tree processing algorithm according to their own memory access characteristics. The core graph determines the upper bound on the performance of the edge tree processing algorithm optimization. For example, the complete edge tree algorithm BFS_CORE+TEOLV of Fig. 6 has an average performance gap of 4 GTEPS relative to BFS_CORE, which still has room for optimization. It is worth mentioning that although the full edge tree algorithm brings about an 8% performance improvement over the previous optimization, TEOLV is still an initial version of the code implementation that has not been fine-grained yet, just to illustrate the effectiveness of the edge tree algorithm with minimal implementation cost.

**Platform Performance Comparison**

The BFS_CORE+TEOLV on the E5-2683, HTC-Centriq, and EPYC 7452 platforms improved all SCALE by an average of 8.0%, 8.7%, and 13.2%, respectively, relative to PRE. The BFS_CORE on the E5-2683, HTC-Centriq, and EPYC 7452 platforms improved all SCALE by an average of 19.7%, 17.9%, and 31.8%, respectively. The EPYC 7452 platform has the strongest performance due to the use of the most advanced manufacturing process, huge capacity LLC, and the largest number of physical cores. The HTC-Centriq is essentially the same configuration as the E5-2583. Since the E5-2683 uses an ICC compiler by default and has two NUMA nodes, it has been optimized with NumaAware compared to the HTC-Centriq platform. We also tested with GCC and without NumaAware on E5-2683 for increased comparability. As shown in Fig. 6, HTC-Centriq Platform performance is on average 57.9% higher than the E5-2683, providing a significant performance advantage.

6.5 Scalability Analysis

This section tests the thread scalability of the edge tree BFS algorithm under different edgefactor with SCALE=26. The HTC Centriq platform is used to illustrate this scalability, considering that it has more cores. For example, when the Fig. 7 average degree is 16, high concurrent processing under 40 threads improves the performance by a factor of 24.43 over single threads, and the performance scales approximately linearly with increasing number of threads. The higher the number of edgefactors, the higher the performance. This is due to the nature of the Kronecker-generated graphs, which become less sparse as the average degree increases. The average performance of the algorithm can reach 56.23 GTEPS at an average degree of 32, which is better than 35.67 GTEPS at an average degree of 16 and 21.41 GTEPS at an average degree of 8.

![Fig. 7 The scalability of ET-BFS under Different Edgefactors](image)

6.6 Cache Efficiency

The basic idea of the edge tree algorithm proposed in this paper is to decompose the random access data correlation algorithm into a smaller random access data correlation algorithm and a cache-friendly data correlation algorithm, which reduces the size of the random access data and improves the cache efficiency. This section uses Perf to obtain the LLC Cache Miss Rate in the multicore to
observe this efficiency improvement. As in Fig. 8, the LLC cache miss rate of TEOLV is only half of that of BFSCODE, and the LLC cache miss rate of the complete ET-BFS algorithm is also reduced. This fully demonstrates that the optimization approach in this paper effectively improves the cache locality and the memory access efficiency.

6.7 Performance and Power Consumption Comparison

As shown in TABLE 5, the performance and power consumption of the main platforms in the Green Graph500 ranking for this research area are listed for the same period. With the addition of the optimizations mentioned in this paper, the HTC Centriq platform has further improved its performance, ranking first on the 2019 Graph500 large dataset list. Compared to Tesla P100 GPU there is still a 1.59x performance power advantage. HTC Centriq, despite having only 1 numa node, still has 3.17 GTEPS higher performance than the previous representative work in the CPU space[13] (4-way machines) and even a 4.49x improvement in performance power consumption. Once again, the efficiency of the approach proposed in this paper is fully demonstrated.

TABLE 5 The Performance and Power Consumption Comparison of Different Platforms

| Reference [13] | Platform | Core | RAM (GB) | Scale | Edge Factor | GTEPS | MTEPS | GreenGraph500 |
|----------------|----------|------|----------|-------|-------------|-------|--------|---------------|
| This work      | 1-way    | 40   | 384      | 30    | 16          | 34.49 | 282.70 | Nov 2019     |
|                | HTC      |      |          |       |             |       |        |               |
|                | Centriq  |      |          |       |             |       |        |               |
| Other          |          | 66   | 30       | 16    | 41.7        | 177.45|        |               |
|                |          |      |          |       |             |       |        |               |
| Other          |          | 10   | 30       | 16    | 13.2        | 66.0  | Nov 2019|               |
|                |          |      |          |       |             |       |        |               |
| Other [13]     | 4-way    | 32   | 512      | 30    | 16          | 31.32 | 62.30  | Nov 2019     |
|                | Xeon E5 |      |          |       |             |       |        |               |
| This work      | 2-way    | 64   | 256      | 29    | 16          | 86.15 |        |               |
|                | EPYC 7452|      |          |       |             |       |        |               |

7 CONCLUSION

In this paper, we propose a new way of classifying algorithms into DIA, CFDCA, and CUDCA based on their runtime correlation and cache friendliness with data. The differences between data correlation algorithms and high performance numerical algorithms are expressed in depth, which can be useful for future data correlation algorithm optimization and architecture design. We find that small degree vertices are an important cause of high random memory access in graph processing, and propose a basic perspective of graph data understanding, which views graphs as consisting of core graphs and edge trees, and provides a basic analytical model for relevant research in the field of graph processing. Finally, we propose a general, easy-to-implement, and strongly effective breadth-first traversal algorithm for graph data, ET-BFS, which provides a new way of thinking for future optimization work in the field of supercomputing and graph processing. The experimental results show that it brings 19.7%, 17.9%, and 31.8% performance improvement on mainstream platforms such as E5-2683, HTC-Centriq, and EPYC 7452, respectively. The performance-power ratio on HTC-Centriq platform is 282.70 MTEPS/s, which is in the November 2019 Green Graph500 list ranked first in the world[19].

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