LETTER

Silicon neuron transistor based on CMOS negative differential resistance (NDR)

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Abstract Computer-science-oriented and neuroscience-oriented are two general approaches to developing Artificial General Intelligence (AGI). In this study, a silicon neuron transistor is developed using the neuroscience approach for AGI applications. Neuronal behavior (“weighted sum and threshold” function) is based on the complementary metal–oxide–semiconductor (CMOS) negative differential resistance (NDR) theory. The neuron transistor is implemented by the UMC 180-nm commercial standard CMOS process, which is beneficial to implement an entire neural network or integrate with other CMOS circuits on the same chip. The neuron transistor is composed of three inputs V₁, V₂, and V₃ and a control terminal, V₀. A load terminal, V₀(LOAD), and a driver terminal, V₀(DRIVER), respectively. The width of each input is 1.8 μm, and the inputs have 1, 2, and 4 fingers respectively, that is, the weight ratio is 1:2:4. V₀(LOAD) and V₀(DRIVER) enable a neuron transistor to function more closely resembles a real biological neuron, with improved sensitivity and less complexity compared to a traditional artificial neural network. The neuron MOS transistor was measured at the maximum frequency of 10 kHz. It had an extremely low power consumption of <10⁻⁴ µW and a miniscule footprint 30 × 15 μm². As the process feature size decreases, the chip’s operating frequency could be increased by one order of magnitude, while its power consumption and footprint will decrease.

Keywords: artificial general intelligence (AGI), CMOSFET circuits, artificial neural networks (ANNs), silicon neuron transistor, negative differential resistance (NDR)

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Artificial General Intelligence (AGI) chips have diverse application prospects in domains such as image classification [1], language processing [2], speech recognition [3], and other specific tasks [4, 5, 6, 7, 8]. Non-spiking Artificial Neural Networks (ANNs) inspired by the cortex in terms of spatial complexity are current research hotspots. ANNs are predominantly built using idealized computing units with continuous activation values and a set of weighted inputs. These units are commonly called “neurons” because of their biological inspiration [5, 9, 10, 11].

In 1992, Shibata first proposed the neuron metal–oxide–semiconductor (MOS) transistor (neuMOS or vMOS) [12, 13, 14, 15] based on a double-poly silicon CMOS process, which performed the weighted summation and threshold operations of biological neurons. In previous studies, a neuron transistor with a MoS₂ flake as the channel layer was developed, and its frequency range was 0.0125–14.60 Hz [16, 17, 18, 19, 20], which is extremely close to the response frequency of biological neurons. In the present research, the 180-nm United Microelectronics Corporation (UMC) standard CMOS process is used to implement the basic functions of neurons (weighted sum and threshold). Based on our literature review, these functions implemented using a commercial CMOS standard process based on Negative Differential Resistance (NDR) theory [21, 22, 23] for the first time and can be integrated with other circuitry structures on the same chip.

The NDR neuron transistor without a capacitance structure is measured at maximum frequency of 10 kHz, and the results indicate that it has an extremely low power consumption of <10⁻⁴ µW. As the process feature size [24, 25] decreases, the chip’s operating frequency will increase by one order of magnitude, and its power consumption and footprint will decrease [25].

The remainder of this paper is organized as follows: the CMOS NDR theory is discussed in Section 2, the measurement results of the developed neuron transistor are analyzed in Section 3, concluding remarks are given in Section 4.

2. CMOS NDR

The NDR concept has been researched for nearly 100 years [22, 23, 26, 27, 28]. An NDR device is characterized by the negative slope of I–V curve. An ideal A-type NDR I–V curve [29] and an ideal N-type NDR I–V curve [30] are shown in Fig. 1.

Fig. 1 (a) Ideal A-type NDR I–V curve, (b) ideal N-type NDR I–V curve.
higher than that when $V_b = 1.0$, $1.2$, $1.4$, $1.6$, and $1.8$ V from bottom to top.

Fig. 2(a) shows a $\Lambda$-type CMOS NDR circuit, which comprises three NMOS field effect transistors (NMOSFETs): MN1, MN2, and MN3. The three terminals of the NDR device are denoted as base (B), collector (C), and emitter (E), and the device symbol is shown in Fig. 2(b).

The emitter (E) of the NDR device and the substrate are grounded. When $V_b$ is a fixed value and $V_c = 0$ V, the gate voltage of MN2 is $0$ V which is below the threshold voltage $V_{TH}$ of MN2, so no current flows through the channel of MN2. Therefore, the sum of $V_{GS1}$ (the voltage between the gate and source of MN1) and $V_{GS3}$ of MN3 is $V_b$. The current of MN1 cannot pass through the gate of MN3 to the channel of MN2. Because $V_{GS2}$ of MN2 is less than the $V_{TH}$, the current of MN1 is zero. Therefore, $I_c$ is equal to the $I_{DS3}$ (drain-source current of MN3). According to the working principle of NMOSFET, the $I_{DS3}$ will be increasing as the $V_c$ rising. When $V_c$ gradually rises up to $V_{TH}$, both MN1 and MN2 are turned on, and the current flows toward the emitter (E) through MN2. Thus $V_{GS1}$ rises, $V_{GS3} = V_b - V_{GS1}$ drops, so $I_{DS3}$ decreases, until $V_{GS3}$ is less than $V_{TH}$. And $I_{DS3}$ decreases to zero, resulting in a $\Lambda$-type CMOS NDR.

Fig. 2(c) shows the simulated $\Lambda$-type $I$–$V$ curves [29] of the NDR device measured by modulating $V_b$ to $1.0$, $1.2$, $1.4$, $1.6$, and $1.8$ V. The gate length of NMOSFETs is $180$ nm. The gate widths of the NMOSFETs in the NDR device are $W_{MN1} = 240$ nm, $W_{MN2} = 1.8$ $\mu$m, and $W_{MN3} = 1.8$ $\mu$m, and the numbers of fingers are $1$, $2$, and $6$, respectively. When $V_b = 1.0$ V, the peak voltage and peak current are $\sim 0.16$ V and $3.1$ mA, respectively. As the $V_b$ increasing, the peak voltage and peak current increase simultaneously. When $V_b = 1.8$ V, the peak voltage and peak current are $\sim 0.37$ V and $15.1$ mA, respectively. The peak current is five times higher than that when $V_b = 1.0$ V.

Fig. 3(a) shows a N-type CMOS NDR circuit, which comprises four NMOSFETs: MN1, MN2, MN3, and MN4. The three terminals of the NDR device are denoted base (B), collector (C), and emitter (E). The peak current is five times the gate widths of the NMOSFETs in the NDR device are 1.6, and 1.8 V. The gate length of NMOSFETs is 180 nm. When $V_c$ rising, $I_c$ increases owing to MN4.

Fig. 3(b) shows the simulated $I$–$V$ curves of the N-type NDR measured by modulating $V_b$ to $1.0$, $1.2$, $1.4$, $1.6$, and $1.8$ V. The emitter (E) of the NDR device and the substrate are grounded. The gate length is $180$ nm, and the gate widths of the NMOSFETs in the NDR device are $W_{MN1} = 240$ nm, $W_{MN2} = 1.8$ $\mu$m, $W_{MN3} = 1.8$ $\mu$m, and $W_{MN4} = 1.8$ $\mu$m, and the numbers of fingers are $1$, $2$, $6$, and $20$, respectively. The N-type NDR device and the $\Lambda$-type CMOS NDR device work alike. When $V_c$ is small, the $V_{GS4}$ of MN4 is less than $V_{TH}$, and the circuit presents negative resistance. As $V_c$ rising, $I_c$ increases owing to MN4.

Compared to the N-type NDR [30] devices using four NMOSFETs, as shown in Fig. 3, the $\Lambda$-type NDR device has only three NMOSFETs, $\sim 40\%$ smaller footprint, and considerably lower power consumption.

### 3. Neuron transistor

A neuron transistor is a high-function multi-input logic device [31] that can be used to realize the same functions as neuron cells. The original neuron transistor was fabricated using a double-poly silicon CMOS process [12, 13, 14], but it is also realizable using the NDR devices of 180-nm UMC CMOS [32, 33] process as well.

The circuit shown in Fig. 4(a) is composed of an NDR-load and an NDR-driver in series. The gate widths of the NMOSFETs in the NDR-load and the NDR-driver are $W_{MN1} = 240$ nm, $W_{MN2} = 1.8$ $\mu$m, and $W_{MN3} = 1.8$ $\mu$m. The finger numbers of the NDR-load are 1, 2, and 6. The finger numbers of NDR-driver are 1, 2, and 30. The DC $I$–$V$ curve of the NDR-load and the NDR-driver are shown in Fig. 4(b), and $V_{b\text{(load)}}$ and $V_{b\text{(driver)}}$ are $1.4$ V and $1.0$ V, respectively. $V_c$ and $I_c$ denote the voltage and current at terminal C in the NDR-load and the NDR-driver. The stable
The operating point can be determined based on the intersection point of the two $I-V$ curves by performing load-line analysis, as shown in Fig. 4(b) [23, 34].

The operating point B for intersecting at the NDR region is unstable [22]. If the current of the NDR-load is greater than current of the NDR-driver, the excess current must charge the load capacitance at the circuit output, so the output voltage increases. According to the load-line in Fig. 4(b), the current of the NDR-load further increases, and the current of the NDR-driver decreases, leading to a further rise in the output voltage across the load capacitance. Therefore, the output voltage holds the stable high state C corresponding to ‘1’. Otherwise, the output voltage holds the stable low state A corresponding to ‘0’. To switch the state from A to C, a current of sufficient amplitude must be injected into the output node to bring the circuit beyond point B. To realize the transition from C to A, a suitable current level must be subtracted from the output node to decrease the output voltage down to point B.

$V_{CC}$ is a clock, and the two stable states are “erased” when $V_{CC}$ is zero. When $V_{CC}$ is reestablished, the circuit moves toward A or C depending on the external excitation.

The function of a neuron transistor is to mimic the neuronal cells by implementing the following functions

\[
S = \sum W_i x_i \quad (i = 1, 2, 3) \quad (1)
\]

\[
O = \mu(S - L_{th}) \quad (2)
\]

where $W_i$ and $x_i$ ($x_i = 0, 1$) are the input signal weights of the three input gates ($V_{g1}, i = 1, 2, 3$), $S$ is the weighted sum, $O$ is the output, and $L_{th}$ is the threshold value. $\mu(S - L_{th})$ is a step function that equals ‘0’ when $S - L_{th} < 0$ and ‘1’ when $S - L_{th} > 0$. The above signals are digitally processed forms of the actual signals and do not represent the actual voltages.

As shown in Fig. 5(c), a neuron transistor consists of a weighted sum circuit and a threshold logic circuit in series. Three NMOSFETs paralleling to the NDR-load act as the synapses (input gates) that connect to the neuron with the synaptic weights represented by the total NMOSFET width. Signals injected by $V_{g1}, V_{g2}$ and $V_{g3}$ are weighted and summed as the weighted sum $S$. According to Eq. (1), the $S$ is the sum of the product of the $W_i$ and the input gate voltage signal (‘0’ or ‘1’). When the $S$ exceeds the threshold value $L_{th}$ (controlled by the threshold voltage $V_{con}$, $L_{th}$ is the digital form of $V_{con}$). Therefore, $L_{th}$ can be controlled by $V_{con}$, the output $V_{out}$ is high (‘1’). Fig. 6 shows the operation of the three input gates and the corresponding output signals. The width of each gate is 1.8 $\mu$m, and the gates have 1, 2, and 4 fingers respectively, which means that the weight ratio is 1:2:4. The threshold voltage $V_{con}$ and the NDR-driver perform the threshold logic operation on $S$ [21]. For example, the neuron transistor is set at, $V_{b(load)} = 1.4$ V and $V_{b(driver)} = 1.0$ V respectively as shown in Fig. 6 and Table I. $L_{th}$ can be varied from −0.5 to 7.5 by changing the control voltage $V_{con}$. 

![Fig. 4](image-url) Operation mechanism. (a) Circuit diagram, (b) load-line analysis.

![Fig. 5](image-url) (a) Biological neuron, (b) artificial neuron transistor, and (c) circuit of neuron transistor.

![Fig. 6](image-url) Operation of three input gates and output signal.
The current of the weighted sum circuit and the current of the threshold logic circuit are controlled by the weighted voltage \( V_{G} \) and the threshold voltage \( V_{con} \), respectively. According to Fig. 4(b), when the output is open, the current of the weighted sum circuit and the threshold logic circuit should be equal, and the neuron transistor works in the unstable state B. When \( S - L_{th} > 0 \), the current of the weighted sum circuit is more than the current of the threshold logic circuit, the excess current charges the load capacitor. The output voltage is maintained at a stable high-level state C, which corresponds to the digital logic ‘1’. Because of the current in the pull-down NMOSFET controlled by \( V_{con} \), which necessarily flow through the NDR-load, the output voltage is 0.82–0.79 V, which is less than the clock voltage \( V_{CC} \), as shown in Fig. 6.

When the weighted voltages of three input gates (\( V_{G} \)) are determined which means that \( S \) is determined, the increase of \( V_{con} \) will lead to an increase of the current of the threshold logic circuit, but the increase of \( V_{con} \) will not charge the load, which is equivalent to an output disconnection. However, to ensure that the current of the weighted sum circuit is equal to the current of the threshold logic circuit, the current of the NDR-load must be increased (see Fig. 4(b)), causing the \( V_{con} \) drops to state A, corresponding to the digital logic ‘0’.

A conventional Resonant-Tunneling-Diode (RTD) neuron transistor does not include \( V_{G(\text{load})} \) and \( V_{G(\text{driver})} \), and the relationship between \( L_{th} \) and \( V_{con} \) is fixed. Therefore, it is incapable to scale the synapses. Synaptic scaling is defined as the differential modulation of the individual synaptic gains in a population of synapses. This process stabilizes a neuronal network [35]. However, a biological neuron is unstable and sensitive to the environment, and it can learn from the past. \( V_{G(\text{load})} \) and \( V_{G(\text{driver})} \) make a neuron transistor more like a biological neuron (see Table I). As shown in Fig. 5(a), the dendrites and axon terminals connect multiple neurons to form an ANN. The proposed neuron transistor in this study has \( V_{G(\text{load})} \) and \( V_{G(\text{driver})} \), which can improve the sensitivity and reduce the complicity of an ANN, thereby facilitating the construction of powerful AGI chips with synaptic scaling. In the previous work, synaptic scaling was implemented by adjusting the weight, and the threshold value remained unchanged \[12, 13, 14\]. In this study, the weights should be changeable, but the NMOS width of the \( V_{G} \) is always fixed (the weight cannot be changed). However, the threshold value \( L_{th} \) can be changed by \( V_{con} \). Therefore, synaptic scaling was realized by adjusting the threshold value \( L_{th} \).

Table I Relationship between \( L_{th} \) and \( V_{con} \) for different \( V_{G(\text{load})} \) and \( V_{G(\text{driver})} \)

| \( L_{th} \) | \( V_{con} \) (1.45V) | \( V_{con} \) (1.45V) | \( V_{con} \) (1.45V) | \( V_{con} \) (1.45V) |
|-----------|-----------------|-----------------|-----------------|-----------------|
| 0.5       | 1.37            | 0.72            | 1.65            | 0.99            |
| 1.5       | 1.39            | 0.74            | 1.66            | 1.00            |
| 2.5       | 1.41            | 0.76            | 1.68            | 1.02            |
| 3.5       | 1.43            | 0.78            | 1.70            | 1.04            |
| 4.5       | 1.45            | 0.80            | 1.72            | 1.06            |
| 5.5       | 1.47            | 0.82            | 1.73            | 1.08            |
| 6.5       | 1.49            | 0.825           | 1.735           | 1.10            |
| 7.5       | 1.50            | 0.83            | 1.738           | 1.12            |

Table I summarizes the relationship between \( L_{th} \) and \( V_{con} \) for different combinations of \( V_{G(\text{load})} \) and \( V_{G(\text{driver})} \). At a fixed \( V_{G(\text{load})} \), a higher \( V_{G(\text{driver})} \) causes the neuron transistor to operate at a lower \( V_{con} \). Conversely, at a fixed \( V_{G(\text{driver})} \), a higher \( V_{G(\text{load})} \) causes the neuron transistor to operate at a higher \( V_{con} \). Table I also reveals that \( V_{con} \) varies uniformly as \( L_{th} \) changes from 1.5 to 5.5. However, when \( L_{th} \) changes from 5.5 to 7.5, the variation in \( V_{con} \) is nonuniform. Fig. 6 and Table I confirm that all the \( S \) can be distinguished using the \( V_{con} \).

Fig. 7(a) shows a zoomed layout view of the neuron cell from the EDA tool, and Fig. 7(b) shows the top view of the neuron transistor. The chip size is \( 0.67 \times 0.60 \text{ mm}^2 \), and the transistor has 10 pads, including two GND pads, a \( V_{CC} \) pad, three \( V_{G} \) pads \((i = 1, 2, 3)\) pads, a \( V_{con} \) pad, and two \( V_{load} \) pads. All pads are designed to measure the neuron transistor. In fact, the footprint of the neuron transistor with 10 NMOSFETs is \( 30 \times 15 \text{ mm}^2 \).

Fig. 8 shows the circuit used to test the power consumption of the neuron transistor. The maximum internal resistance of the voltmeter is 10 M\( \Omega \), and the voltmeter is connected in series with the neuron transistor. The reading is still less than 1 mV, which estimates that the power consumption of the neuron transistor is less than \( 10^{-4} \text{ \mu W} \), which is about four orders of magnitude lower than other chips, as shown in Table II [36, 37]. At the same time, the frequency of the chip is three orders of magnitude higher and its area is the smallest. As the size of the process features decreases, the operating frequency of the chip will increase by an order of magnitude, and its power consumption and area will continue to decrease.
Table II Comparison of this work with conventional neuron transistor.

| Reference | Technology | Area (μm²) | Frequency (Hz) | Power consumption (μW) |
|-----------|------------|------------|----------------|------------------------|
| [12-15]   | double-polysilicon CMOS | -2400 | - | - |
| [11]      | RGZO (PECVD) | ~20000 | 0.01 | ~10² |
| [36, 37]  | ITO (PECVD) | ~80000 | -0.01-0.05 | -4 |
| [17]      | MoS₂ | 800 | 0.0125- 14.6 | -1 |
| **This work** | CMOS 180 nm | 450 | 10 k | <10⁴ |

4. Conclusion

MOS neurons remain the best choice for integration with analog/digital VLSI circuits. In this study, a new neuron MOS transistor comprising 10 NMOSFETs was designed and fabricated according to the CMOS NDR theory, which has not been done before based on our review of the literature. The neuron transistor was measured at the maximum frequency of 10 kHz. The result of power consumption test indicated that the developed transistor had an extremely low power consumption of <10⁻⁴ μW, and it occupied a very small footprint. The work done here provides a novel design methodology for potential researchers in this area to design their own neurons based on CMOS NDR design concept. The work also demonstrates an innovative design methodology based on CMOS NDR concept in the design and fabrication of AGI chips, breaking away from the conventional circuit design theory approach. As the process feature size decreases, the chip’s operating frequency could be increased by one or more orders of magnitude, while the chip’s power consumption and area will continue to decrease.

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