Low Thermal Budget Fabrication of III-V Quantum Nanostructures on Si Substrates

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Abstract. We show the possibility to integrate high quality III-V quantum nanostructures tunable in shape and emission energy on Si-Ge Virtual Substrate. Strong photoemission is observed, also at room temperature, from two different kind of GaAs quantum nanostructures fabricated on Silicon substrate. Due to the low thermal budget of the procedure used for the fabrication of the active layer, Droplet Epitaxy is to be considered an excellent candidate for implementation of optoelectronic devices on CMOS circuits.

The achievement of III-V self-assembled quantum nanostructures (QNs) integration on silicon substrates could allow the use of silicon infrastructure, based on complementary metal oxide semiconductor (CMOS) technology, as base for the fabrication of optoelectronic devices like nano emitters and inter-subband detector realized with III-V semiconductor materials [1].

The integration of III-V optoelectronic devices and structures on Si is far from optimized, notwithstanding its great technological relevance. Some important issues have to be overcome in order to obtain high quality III-V materials directly on Si. The first is the large lattice mismatch (about 4.1%) between Si and GaAs, which introduces misfit dislocation nucleation as soon as the GaAs epilayer thickness exceeds a critical value. A second issue is the antiphase disorder, that arises from different symmetry of the zincblend and diamond lattice. A last major issue is the strict thermal budget required during the growth of an epilayer to maintain the compatibility with the underlying CMOS circuit.

To avoid these issues we used a Ge virtual substrates (GeVS), that is a fully-relaxed, micron thick, Ge epitaxial buffer. GeVS can be used to accommodate the lattice mismatch between GaAs-based III-Vs and the Si substrate. GeVS growth technique is also compliant with front-end CMOS integration. Anti Phase Domains (APDs) can be effectively eliminated by using intentionally misoriented substrates [2,3].

For the growth of III-V nanostructures we selected an intrinsecally low thermal budget (LTB) technique, the droplet epitaxy (DE) [4,5]. Being performed at 200-350°C, DE is perfectly suited for the realization of growth procedures compatible with back-end integration of III-V nanostructures on CMOS that is, after the CMOS circuitry has been already realized. The fabrication of quantum nanostructures by DE is consistent with the strict constraints on thermal budget imposed by the compatibility with the underlying CMOS circuit. Moreover, the use of DE technique opens the possibility to fabricate a large variety of three dimensional nanostructures tunable in density, size and shape [6-8].

1. Experimental setup

For our experiments we used a silicon (001) substrate, 6° misoriented towards [110]. A fully-relaxed 2 μm layer of Ge buffer layer was deposited on the silicon substrate by Low-Energy Plasma-Enhanced Chemical Vapour Deposition (LEPECVD) [9,10] in order to form a Ge virtual substrate (GeVS). Just after deposition, the GeVS was cyclically annealed six times at 600 - 780°C to reduce the threading dislocation density to 2×10⁷ cm⁻² [11]. GeVS technology we adopted is reported to be used for the fabrication of ultra-low dark current Ge photodiodes and to be fully compliant with CMOS front-end technology [12].

The GeVS was then transferred to a Gen II MBE machine. In the growth chamber we started an MBE growth of 1 μm GaAs buffer keeping the temperature at 580°C. Confirmation of APD-free sample came from the clear (2x4) surface reconstruction of the RHEED pattern during GaAs growth. Our first task was then to test the self aggregation of QNs by DE on a GaAs/Ge/Si substrate. So for the first sample we
used standard high temperature MBE growth for the deposition of an high crystal quality Al$_{0.30}$Ga$_{0.70}$As buffer. A temperature range between 150 and 200$^\circ$C compatible with CMOS technology was maintained only for the fabrication of the quantum dots (QDs) by DE. Details for the growth procedure are reported in ref [13]. The sample was finally capped with 150 nm of Al$_{0.30}$Ga$_{0.70}$As by conventional MBE at 580$^\circ$C for PL measurements and with a GaAs capping layer. This sample was then submitted to an annealing step at 700$^\circ$C in As atmosphere for 30 min to improve barrier crystal quality [14].

We then fabricated a second sample with an active layer fully compliant with LTB requirements. For this purpose we reduced the thermal budget for the annealing procedure and for the creation of the Al$_{0.30}$Ga$_{0.70}$As barrier. Using migration enhanced epitaxy [15], temperature was kept constant at 350$^\circ$C during the creation of the whole active layer. Details for the growth procedure are reported in ref [16]. For this sample another 80 nm Al$_{0.30}$ Ga$_{0.70}$ As layer was deposited by MEE at 350$^\circ$C for photoluminescence measurements. The sample was finally submitted to a 4 minutes Rapid Thermal Annealing (RTA) procedure at 600$^\circ$C in nitrogen atmosphere to improve barrier crystal quality [17]. Also this step is compliant with LTB requirements for $>0.25\mu$m CMOS back-end technology [18].

Surface morphology was analyzed on uncapped samples by a Veeco-Innova Atomic Force Microscope (AFM). The photoluminescence (PL) spectra of the capped samples were measured at 14 K using a closed-cycle cold-finger cryostat. PL was excited with a neodymium doped yttrium aluminum garnet laser with $\lambda_{exc}=532$ nm and an excitation power density of $P_{exc}=6$ W/cm$^2$. The spectrum was measured by a grating monochromator operating with a Peltier-cooled charge-coupled device detector.

2. Results and discussion

Left panel of figure 1 shows the AFM image of the first uncapped sample. It demonstrates the QD formation on the surface of the first sample. The density is about $1 \times 10^{10}$ cm$^{-2}$, in good agreement with data reported for DE experiments on GaAs substrates [6]. An interesting point is to observe that the size and density of QDs is not constant across the surface of the sample, being smaller and with higher density in the substrate valleys. This behaviour could be associated qualitatively with the interaction of the gallium droplets with surface steps. Is known that surface steps are preferential nucleation sites for gallium droplets, as shown on (110) substrates [19]. The QD ensemble shows a mean height of $\approx 5$ nm and a base radius of $\approx 20$ nm with a size dispersion for both values around 25%. PL spectrum of QD capped sample (figure 1, right panel) shows an intense emission peak at 1.78 eV, in good agreement with the calculated value of $E_{gs}=1.75$ eV. This emission energy was predicted for a single randomly choosen single quantum dot, applying the method of effective mass approximation outlined in [21] and using material parameters reported in [22].

Left panel of figure 2 shows AFM image of the second uncapped sample. It demonstrates the formation of quantum nanostructures with a density of $6 \times 10^8$ cm$^{-2}$ characterized by a regular, nanometers high, flat disk with a diameter of hundreds of nanometers and a hole at the center of $\approx 80$ nm. The rim of the
Figure 2. Left panel: 2x2 μm AFM image for uncapped CRD sample. Inset shows profile of a typical nanostructure. Right panel: normalized photoluminescence spectra for CRD sample with excitation power density of 6 W/cm² (black line) and 0.6 W/cm² (red line).

inner hole is protruded over the disk surface by some nanometers. Because of their shape we call these nanostructures Coupled Ring-Disks (CRDs) [20].

PL measurements of the CRD sample show (figure 2, right panel) an intense emission peak at 1.55 eV, and a shoulder at 1.59 eV. The first value is in good agreement with the energy of the ground state \( E_{gs} = 1.56 \) eV obtained using effective mass approximation. The shoulder should be attributed to the excited state. This calculation shows also that electron and hole are confined in the inner ring, and that the excited state is extended along the external disk.

Comparing PL data makes clear that is possible to obtain efficient and high quality III-V QNs on Si substrate using a LTB procedure not only for the fabrication of the QNs, but also for the whole active layer. Measurements performed on the CRD sample shows a quantum efficiency of \( \eta = 3 \times 10^{-3} \) similar to the one obtained by DE on standard GaAs substrate [16]. Calculations were performed evaluating the number of incoming and emitted photons.

The PL emission is clearly detectable at room temperature, where PL intensity is reduced by a factor \( \approx 400 \) respect to the low temperature case.

3. Conclusions

We demonstrated the growth of high quality and high efficiency III-V QNs on Silicon substrate, using a LTB procedure. In particular, the fabrication procedure for the GeVS we proposed is compliant with front-end CMOS integration, while the growth procedure for the AlGaAs/GaAs active region is fully compliant with CMOS back-end integration. With small changes for the GaAs layer growth, the whole structure would be easily made fully compliant with the requirements of CMOS technology.

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