The SpiNNaker 2 Processing Element Architecture for Hybrid Digital Neuromorphic Computing

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Abstract — This paper introduces the processing element architecture of the second generation SpiNNaker chip, implemented in 22nm FDSOI. On circuit level, the chip features adaptive body biasing for near-threshold operation, and dynamic voltage-and-frequency scaling driven by spiking activity. On system level, processing is centered around an ARM M4 core, similar to the processor-centric architecture of the first generation SpiNNaker. To speed operation of subtasks, we have added accelerators for numerical operations of both spiking (SNN) and rate based (deep) neural networks (DNN). PEs communicate via a dedicated, custom-designed network-on-chip. We present three benchmarks showing operation of the whole processor element on SNN, DNN and hybrid SNN/DNN networks.

Index Terms — MPSoC, neuromorphic computing, SpiNNaker2, power management, DVFS, synfire chain

I. INTRODUCTION

Neuromorphic circuits try to mimic certain aspects of neural tissue [1]. The aim is to further our understanding of how the brain computes information, as well as derive novel types of computational hardware for e.g. artificial intelligence applications [2], [3]. This paper introduces the processing element (PE) architecture of the second generation SpiNNaker chip, a digital neuromorphic system. The “Spiking Neural Network Architecture” SpiNNaker is a processor platform optimized for the simulation of neural networks [4]. A large number of ARM processor cores is integrated in a system architecture optimized for communication and memory access. Specifically, to take advantage of the asynchronous, naturally parallel and independent sub-computations of biological neurons, each core simulates neurons independently and communicates via a lightweight, spike-optimized asynchronous communication protocol.

The second generation SpiNNaker2 scales down technology from 130nm CMOS to 22nm FDSOI CMOS [5], while also introducing a number of new features. Adaptive body biasing (ABB) in this 22nm FDSOI process node delivers cutting-edge power consumption [6]. With dynamic voltage and frequency scaling, the energy consumption of the PEs scales with the spiking activity computed on the cores [7], [8]. The Arm Cortex-M4 cores employed for SpiNNaker2 integrate a single-precision floating point unit, thus extending the fixed-point arithmetic of the first generation SpiNNaker. Computation-wise, SpiNNaker2 retains the processor-based flexibility of the first generation system [9], while adding additional numerical accelerators to speed up common operations [10]–[12]. In the current prototype described in this paper, another accelerator has been added, a 16 by 4 array of 8 bit multiply-accumulate units (MAC), enabling faster 2D convolution and matrix-matrix multiplication [13]. Efficient usage of these accelerators can extend the simulation capacity of SpiNNaker2 by a significant factor [14]. The PEs are arranged in groups of four to quad-processing-elements (QPEs) which are connected by a Network-on-Chip (NoC) to allow scaling towards a large neuromorphic System-on-Chip (SoC).

In the following, we introduce the processing element architecture of SpiNNaker2. Subsequently, we show results from the current prototype, specifically a side-by-side implementations of (1) a conventional spiking neural network using the numerical accelerators (2) a standard DNN layer using the MAC array and (3) a hybrid network, where we use the MAC in a spiking context.

II. HYBRID NEUROMORPHIC COMPUTATION APPROACH

We try to capture our approach to neuromorphic computing with the term “hybrid”. In a general sense, this means we aim to achieve a compromise between (a) the software/processor-based approach of Loihi [15] and the first generation SpiNNaker [16] and (b) the classical neuromorphic approaches with dedicated neuron and synapse circuits (in digital or analog) [17]–[20]. Thus, while we do not implement the full neuron and synapse functionality as dedicated circuits, we aim to achieve close to this kind of efficiency by numerically accelerating common operations such as exponentials, log or random functions. At the same time, classical neuromorphic approaches have always been hindered by their essential hard-coding of functionality, which we aim to avoid by keeping the processor cores at the center, employing them to tie the accelerator blocks together.
In an extension of the above definition, "hybrid" also means that we can realize both spiking and rate-based artificial neural networks (SNN/ANN) on SpiNNaker2, since we incorporated accelerators for both types of networks and the ARM processors and communication infrastructure (Network on chip, DMA, etc) are flexible enough to support both. Thus, hybrid networks at the boundary between SNNs and ANN can be realized that combine the best of both worlds, e.g. the numerical simplicity of ANNs with the sparsity and time-dynamic features of SNNs, for enhanced energy efficiency and novel computational paradigms. In a specific instantiation of this idea, the MAC array could be run not frame-based, but in an event-triggered fashion. To fully use the multipliers, this mode of operation needs a graded weight (usually given) and a graded activity-related input value (usually not given, if we assume single-bit axonal spikes). Biologically realistic versions of a graded input value (i.e. multi-bit spikes) for the multipliers in the MAC array could be (1) electrical synapses that generally transmit graded values, e.g. in a retina model. (2) Dendritic computation, i.e. where amplitudes inside a neuron are scalar and have some amplification factor (weight) when being transmitted to other parts of the neuron. Or (3) treating the neuron input as a scalar synaptic current (e.g. representing a pixel grayscale value). This approach is employed in our hybrid use case later in the paper. Non-biologically realistic versions would use the possibility of a 'spike with a payload' for e.g. more efficient coding by trading spike payload for spike frequency, achieving increased sparsity [21]. Another possibility could be more complex processing. That is, the payload could represent some dynamic characteristic of the neuron, e.g. the value of some adaptation process, or how fast the charging slope was, etc.

III. SpiNNaker 2 Many-Core Architecture

With the shrink of semiconductor technologies more processing elements (PEs) can be integrated on a single silicon die, which improves scalability toward multi-million core neuromorphic processors systems. However, the on-chip bus system (system NoC) from SpiNNaker [9] does not scale toward a larger number of on-chip PEs, since it is implemented with flat logic on the chip top-level. This approach is not feasible for a larger number of PEs since flat top-level routing and timing closure would not be feasible. Therefore a quad-processing element (QPE) architecture is employed here, as described in the following.

A. QPE and NoC Architecture

Fig. 1 shows the top-level floorplan architecture of SpiNNaker 2. Its main components are 38 QPEs with 152 PEs in total. The SpiNNaker 2 packet router (Sec. III-B) is responsible for spike communication. In total 6 chip-to-chip communication links allow to form the SpiNNaker multichip network [9]. A host interface allows to connect to an Ethernet infrastructure. Two LPDDR4 memory controllers and PHYs allow the connection of off-chip DRAM. A periphery block contains various low-speed interfaces (GPIO, JTAG, SPI) for configuration, debugging and other general purpose use cases.

A detailed view of the QPE is shown in Fig. 2. The QPE logically combines 4 PEs and a NoC router, with connections to the PEs and the four neighbor QPEs. It is implemented in a globally-asynchronous-locally-synchronous (GALS) clocking scheme, allowing the PEs to operate in the dynamic voltage and frequency scaling (DVFS) scheme from [8] independent from each other and the NoC router logic. Additionally, the...
GALS approach also decouple the QPEs from each other to prevent the need for a chip top-level synchronous clock distribution network. Therefore, the QPE further forms a place and route hard macro which can be seamlessly arranged in an array on chip top-level to build a the many-core SoC. All signal connections to neighbor QPEs are realized in a connect-by-place scheme with asynchronous FIFO clock domain crossings. Additionally of the NoC connections, only a small number of dedicated signals are routed between the QPEs, as for example clock, reset and a few physical interrupt signal lines. The NoC is the main communication resource that interconnects all on-chip components in a 2D-mesh structure. It consists of two independent but interconnected NoC meshes: the data NoC (DNoC) and configuration NoC (CNoC). For data transfers such as DMA or spike packets the DNoC is used. A simplified structure of the NoC router is shown in Fig. 3. It consists of wide asynchronous FIFOs for incoming packets to the router’s clock domain. The packet destination is determined by a X/Y-first routing logic. A following FIFO stage is shorten the internal critical timing path. The output port control arbitrates incoming routing requests in a round-robin fashion and controls the crossbar accordingly. DNoC flit size is 192bit hence an entire packet can transferred at once for high throughput. The router’s latency is 5 clock cycles per hop at a frequency of 400MHz. Besides the NoC a separated CNoC is implemented. It is operated using the reference clock signal and is thereby operational if no clock generator is switched on. And provides access to all registers in a boot-up and configuration step. During operation it allows for data transmission, even if the DNoC is blocked, e.g. by large DMAs. It has a flit width of 32bit and is operating in a worm-hole switching scheme. For interoperability DNoC and CNoC are using the identical packet format shown in 4. The 192bit NoC packet consists of a 15bit NoC header, 17bit packet header, 32bit address and 0 up-to 128bit payload data. Routing decisions of the NoC are made based on the X/Y destination coordinates of the NoC packet. Additionally there are four destination PE bits reserved to allow a multicast on QPE level for spike packet or data packets.

B. The SpiNNaker Router

The SpiNNaker2 packet router, based on [22], [23], is one of the key components of the chip. It is responsible for routing multicast, core-to-core and nearest neighbour packets. An overview of the SpiNNaker2 packet router architecture is shown in Fig. 5. The router incorporates a number of evolutions to support the increased communication throughput, such as parallel routing structure, larger multicast routing tables, improved packet-dropping mechanism, out-of-order issue buffer and a large optional packet payload. Error Correction Code (ECC) SRAMs are adopted and TCAM built-in self-test is designed to improve fault tolerance and test automation. Additionally, the router has fully payload pipeline control and a clock gating implementation for power-saving. The multicast packets are used for neural events and routed by a key provided at the source. The core-to-core packets are routed by a destination address to any core on any chip and intended for machine management. Last but not least, the nearest neighbour packets are routed by destination port(s) to the monitor processor(s) of the neighbouring chip(s), and they are intended for machine boot and debugging functions. The packet format is shown in Fig. 6.

C. Processing Element

As shown in Fig. 7, the processing Element (PE) consists of the Arm Cortex-M4F core, pseudo and true random number generators [12], a fixed-point exponential and logarithm
accelerator [10], [11], a MAC array, timers, SRAM memory array, AHB bus, DMA, and crossbar. DVFS [8] allows for switching between two VDD rails (PL1 and PL2 in Fig. 7) during operation of the PE.

The various computation and memory units of the PE are interconnected through the communication units AHB bus, DMA and crossbar. As shown in Fig. 7, the Arm core is master of three AHB buses, two for access to the memory, one for access to the accelerators, DMA and timers. In addition to the AHB buses for data and instruction for the Arm core of the same PE, the crossbar is also connected to neighboring PEs withing the same QPE, which allows low latency memory sharing between PEs in the same QPE. The crossbar is also connected to the DMA for high-speed communication with other PEs or the DRAM, and for the MAC array to read and write data independently of the the Arm core.

The different numerical accelerators are each connected as individual slave to an AHB multiplexer. Each accelerator has a specific range in the memory map of the PE that it uses for read and write. For details on specific numerical accelerators, please refer to the respective publications, [11] for the exp/log accelerator, [12] for the true random number generator.

To reduce the possibility of contention for SRAM, the crossbar is also connected to neighboring PEs withing the same QPE, which allows low latency memory sharing between PEs in the same QPE. The crossbar is also connected to the DMA for high-speed communication with other PEs or the DRAM, and for the MAC array to read and write data independently of the the Arm core.

While the Arm core forms the main computational resource of the PE, the additional accelerators like the random number generators and the MAC array can greatly increase the computational and power efficiency for certain applications [24] [14]. To reduce the possibility of contention for SRAM, the SRAM is divided into four addressable banks.

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With this testchip iteration the SpiNNaker2 system introduces a broadcast output-stationary MAC accelerator shown in Fig. 8, targeting core operations in popular Deep Neural Network models. The first revision provides 8bit unsigned 4x16 multiply-accumulate per clk cycle and two modes of operation, 2D convolution (CONV) or matrix multiplication (MM). These modes are realized by adapting the memory fetch pattern to the MAC array. To not get bottlenecked by the memory fetch, the accelerator almost fully utilizes the 128Bit/clk local connection to the SRAM within the same PE and writes out results via the same connection. The second operand is fetched from the NoC via a 128Bit/clk NoC interface, which is only partially utilized. The accelerator can be controlled over either the ARM core or per incoming configuration NoC packets. Once started, its execution is independent of the ARM core and from other processing elements. An interrupt is thrown if an operation has finished. For CONV operation, a shift register is included for input feature map reuse relaxing the continuous memory fetch to 4Byte/4clk. Furthermore the output channel dimension and the input feature map width dimension were chosen to fully utilize 1x1 kernels of bottleneck layers and exploit weight and input feature map reuse. The reduced size of the array was chosen due to area considerations. However, since each PE includes its own independent MAC array, the system supports highly distributed inference operations. For that, distribution strategies to optimize for time efficiency and data reuse were developed and simulated [13]. This also
enables row-stationary dataflow [25] and further data reuse due to weight and input feature map sharing between PEs. Further details on how the accelerator works in more detail can be seen in [26].

IV. 22FDX IMPLEMENTATION

A. Adaptive Body Biasing

Adaptive body biasing (ABB) is a technique for FDSOI technologies [5] for the compensation of device performance variations caused by process, voltage and temperature (PVT) variations by means of the adaptive control of the back-gate voltages [6]. In the 22nm FDSOI target technology [5], two body bias schemes, Forward-Body-Bias (FBB) and Reverse-Body-Bias (RBB), are available. In this work the FBB scheme with the flipped well approach (N-Well below NMOS, P-Well below PMOS) is used. Compared to the zero-bias approach where 0.0V is statically connected to the biased-wells, an up to 10X speed improvement at 0.50V operation can be achieved [6]. This enables the ultra-low-voltage (ULV) implementation of the PEs at reasonable clock frequencies of several 100MHz.

In this work the ABB IP platform [6] is used, which provides ABB-aware characterized libraries and dual-rail SRAM from 0.40V to 0.80V core supply voltages. Design implementation, sign-off and power analysis has been performed following the ABB-aware methodology from [27]. Fig. 9 shows the relative performance and leakage power of the nominal supply conditions from 0.40V to 0.60V, being considered for this work. It shows the target speed for ABB regulation, as performance indicator for the operating frequency, versus the worst-case leakage power of the Super-Low-Vt (SLVT) flavor with 28nm gate length at the fast-hot PVT condition. From 0.40V to 0.60V there is a performance gain by factor 5 with a worst case leakage increase by factor 2.

![Graph showing relative performance and leakage power of ABB biased designs.](image)

**Fig. 9.** Relative performance and leakage power of ABB biased designs. Y-axis shows worst case leakage of example cells (SLVT28) in ffg VDD+10% 125C corner. X-axis shows the target speed of the ABB regulation.

B. Design implementation Strategy

The main implementation constraint of the PE was to achieve minimum energy per operation at a reasonable clock frequency, similar to the first generation SpiNNaker chip [9] with a processor clock frequency of 180MHz. Therefore, a mixture of Super-Low-Vt (SLVT) and Low-Vt (LVT) standard cells from a 9-track 104nm CPP library is used [27] to achieve the speed target under ULV conditions. Trial implementations of the PE have been performed at 4 different nominal voltages and different target clock frequencies, as shown in Fig. 10. The designs have been implemented for timing closure at the worst speed PVT corner (ssg, VDD -10%, -40C) and power analysis has been performed in the worst case power corner (ffg, VDD+10%, 125C) with on-post-layout VCD based power analysis of the processor running a software task. Note that the absolute worst speed considered for sign-off does not scale similar to the nominal target speed as plotted in Fig. 9 since additional margins apply [27], which lead to significant additional performance degradation especially at the extreme low voltage conditions. Considering energy per operation metric, there exists a minimum energy point (MEP) at nominal 0.50V operation. At higher voltages, more energy per operation is spent due to higher switching energy. At lower voltages more energy per operation is accumulated due to leakage power over the longer clock period.

![Graph showing trial implementation result, relative energy consumption from design implementations at 4 different supply voltages and target clock frequencies.](image)

**Fig. 10.** Trial implementation result, relative energy consumption from design implementations at 4 different supply voltages and target clock frequencies, MEP Study result

As result, the target implementation point has been chose at 0.50V nominal and 200MHz. However, this does not denote a significant performance scaling compared to the first generation SpiNNaker processor [9]. Therefore, the DVFS technique from [7], [8] is applied here, with two performance levels (PLs). PL1 is the MEP operating point of (0.50V, 200MHz) and PL2 is defined as the higher performance level at (0.60V, 400MHz). This allows for DVFS operation between 200MHz and 400MHz. Fig. 11 summarized the implementation results statistics of the PE for cell distribution and component area and leakage distribution. By means of ABB the design could be implemented with relatively low SLVT cell-count (Fig. 11(a)) which still dominates the leakage power. The total PE cell area is dominated by the 128kB SRAM and the Arm Cortex-M4 MCU with floating point unit which in sum consume 75% of the PE area. The peripheral blocks like hardware accelerators, NoC and bus interfaces consume only 25% of the area (Fig. 11(b)), but 50% of the total leakage.

In Fig. 12 the layout of the QPE with 4PEs is shown. Because the QPE logic shows less toggle rate compared to the PE its energy efficiency is more sensitive to leakage and power analysis has been performed for timing closure at the worst speed PVT corner (ssg, VDD -10%, -40C) and power analysis has been performed in the worst case power corner (ffg, VDD+10%, 125C) with on-post-layout VCD based power analysis of the processor running a software task. Note that the absolute worst speed considered for sign-off does not scale similar to the nominal target speed as plotted in Fig. 9 since additional margins apply [27], which lead to significant additional performance degradation especially at the extreme low voltage conditions. Considering energy per operation metric, there exists a minimum energy point (MEP) at nominal 0.50V operation. At higher voltages, more energy per operation is spent due to higher switching energy. At lower voltages more energy per operation is accumulated due to leakage power over the longer clock period.

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Fig. 11. PE implementation results statistics

(a) standard cell distribution
(b) component distribution

Fig. 12. Chip photo and QPE layout

V. TESTCHIP

A test chip JIB has been implemented in GLOBAL-FOUNDRIES 22FDX technology [5] with a chip area of 8.76mm². The chip photo is shown in Fig. 12. It contains two QPEs with 8 PEs in total, a SpiNNaker router instance for Spike communication with two prototype chip-2-chip connection SerDes links. A SerDes host interface is integrated to allow for connection of an FPGA. The periphery block contains various standard interfaces (UART, SPI, I2C, JTAG) and the instance of the adaptive body bias generator [27]. The on chip clocks are generated using the clock generator from [28].

A lab evaluation PCB has been designed, as shown in Fig. 13. It contains 6 test chip sockets, which allows for prototyping of various system integration aspects of the SpiNNaker2 system. The board is equipped with automated power supply measurement devices, which allows for detailed characterization of the test chip energy efficiency.

VI. BENCHMARKS AND RESULTS

To show both, the energy efficiency of the Processing Element (PE) and the capability of hybrid digital neuromorphic of SpiNNaker2, we implement various benchmarks. This includes plain CoreMark and matrix multiplication cases and three diverse benchmark networks ranging from Synfire Chain representing the classical Spiking Neural Network (SNN) (section VI-B), through the Neural Engineering Framework (NEF) representing the combined SNN/DNN approach (section VI-C), to convolutional layers and fully connected layers as examples of Deep Neural Networks (DNN) (section VI-D).

A. PE metrics testchip results

Fig. 14 shows the measured PE processor efficiency when executing the CoreMark benchmark from local SRAM. At the two DVFS PLs efficiencies of 16.68μW/MHz (at 0.50V, 200MHz) and 20.16μW/MHz (at 0.60V, 400MHz) are achieved. Fig. 15 shows the measured energy efficiency when executing 8-bit matrix multiplications from local SRAM in the 16 × 4 MAC accelerator array. At the two DVFS PLs 1.47TOPS/W (at 0.50V, 200MHz) and 1.51TOPS/W (at 0.60V, 400MHz) are achieved, respectively. For this scenario we can achieve 1.75TOPS/W (at 0.50V, 320MHz). Due to a hardware bug in the data transfer the overall TOPs/W are reduced by a factor of roughly 1.56.

Fig. 13. Testchip PCB Setup

Fig. 14. Measured PE CoreMark benchmark energy efficiency
B. Spiking Neural Network

For the SNN benchmark we follow the approach of [8]: each PE simulates a number of neurons and their inbound synapses. A timer tick triggers each time step and guarantees real time operation. In each time step, after the neurons are simulated, the output spikes are sent to their target PEs, where they are stored in a FIFO and processed in the next time step. The Performance Level (PL) of the PE, which is a supply voltage and frequency pair ($V_{DD}, f$), is adjusted according to the number of spikes in the FIFO. In each time step, after the simulation is finished, the PE returns to PL1 for minimum energy consumption and switches to sleep mode, until the next timer tick wakes the PE up.

For the testchip 3 PLs are available: PL1 with 0.5 V 100 MHz for low power operation, PL2 with 0.5 V 200 MHz for normal operation, and PL3 with 0.6 V 400 MHz for peak performance operation. Similar to [8], an energy model is employed to estimate the energy consumed in a simulation cycle:

$$E_{cycle} = P_{BL,i} \cdot t_{sp} + P_{BL,1} \cdot (t_{sys} - t_{sp}) + e_{neur,i} \cdot n_{neur} + e_{syn,i} \cdot n_{syn}$$ (1)

where $P_{BL,i}$ is the baseline power at PL $i$, which means the power of a PE when it is switched on and wake-up is done by the timer ticks, but after wake-up immediately goes back to sleep, without doing any computation related to neuron or synapse. $t_{sys}$ is the length of the simulation cycle, normally 1 ms, $t_{sp}$ is the time within the simulation cycle, during which the actual simulation is done, $e_{neur,i}$ is the energy for updating one neuron at PL $i$, $n_{neur}$ is the number of neurons, $e_{syn,i}$ is the energy for processing one synaptic event at PL $i$, and $n_{syn}$ is the number of synaptic events.

To extract the parameters of the energy model, we simulate and measure the same locally connected network as in [8], and the parameters are shown in Table I.

Synfire chain [29] is chosen as the spiking neural network benchmark, with the same network parameters as in [8] and [7]. The network structure is shown in Fig. 16. On each PE, there is an excitatory and an inhibitory neuron population. Both populations receive excitatory inputs from the previous layer (PE), and the excitatory population additionally receives inhibitory inputs from the inhibitory population on the same PE. The excitatory population has 200 neurons, and the inhibitory population has 50 neurons. The neurons receive a normally distributed noise current. The synaptic delay from the inhibitory to the excitatory population is 8 ms, and the synaptic delay from the excitatory population to the next layer is 10 ms. The last PE is connected to the first PE to form a circle. Each neuron has 60 presynaptic connections from the excitatory population of the last layer. Each excitatory neuron has 25 presynaptic connections from the inhibitory population of the same layer. A stimulus pulse packet is provided to PE 0 at the beginning of the simulation to kick start the network activity. The network parameters are summarized in Table II. The threshold $I_{th}$ indicates the number of received spikes above which the performance level should be increased. These parameters were determined using the methods in [8].

![Image](image_url)

Fig. 15. Measured PE matrix multiplication energy efficiency

**Table I**

| Parameter       | PL1          | PL2          | PL3          |
|-----------------|--------------|--------------|--------------|
| $P_{BL}$ [mW]   | 22.38        | 29.72        | 66.44        |
| $e_{neur}$ [nJ] | 1.51         | 1.50         | 1.89         |
| $e_{syn}$ [nJ]  | 0.20         | 0.20         | 0.26         |

![Image](image_url)

Fig. 16. Synfire network [8]

**Table II**

| Parameter       | Value       |
|-----------------|-------------|
| Neurons per core| 250         |
| Synapses per core| 20000      |
| Avg. fan-out    | 80          |
| $I_{th,1}$      | 17          |
| $I_{th,2}$      | 59          |

The simulation and measurement show similar results as in [8] and [7]. As shown in Fig. 17, the PL is increased only when it is necessary, i.e. there is more spikes to process. Since the network activity is very sparse for most of the time, mostly PL 1 is used (Fig. 18). Without DVFS, the system would have to be operated at PL 3 all the time. Power measurement is done when the PEs simulate the synfire chain with and without DVFS. The results are summarized in Table III. With DVFS, the total power reduction is 60.4%, with a leakage power reduction of 63.4%.

C. Neural Engineering Framework

The Neural Engineering Framework (NEF) [30] is a hypothesis about using neurons to encode scalar values or vectors.
TABLE III
POWER MEASUREMENT RESULTS FOR SYNFIRE CHAIN SIMULATION (MW)

|                          | baseline power | neuron power | synapse power | total power |
|--------------------------|----------------|--------------|---------------|-------------|
| only PL 3 DVFS reduction | 66.4           | 24.3         | 63.4%         | 71.3        |
| neuron power             | 3.3            | 2.6          | 21.2%         | 66.4        |
| synapse power            | 1.6            | 1.3          | 18.7%         | 24.3        |

Computationally, it normally consists of 3 phases: encoding, neuron update and decoding. In the encoding process, a vector can be translated into neuron input currents. After the neuron update process, the neuron outputs are then translated back to a vector in the decoding process. The encoding process is a vector-matrix multiplication, similar to the fully-connected layer in a Deep Neural Network. In the neuron update process, in the case of a spiking neuron model, the computation is the same as in SNN. Due to this particular computational feature, NEF is chosen as an example of the combined SNN/DNN approach.

We follow the approach in [31] to implement encoding, neuron update and decoding in one PE to reduce communication and computation. Particularly, for the test chip, since the MAC array offloads the computation of matrix multiplication from the ARM core, the encoding process can be executed by the MAC array. For spiking neurons, the decoding process is event based, so it is done in the ARM core. The computation is summarized in Figure 19.

![Fig. 19. Computation flow of Neural Engineering Framework on test chip.](image)

To demonstrate the functionality of the implementation, we show the communication channel example, where the decoded output of a neuron population tries to resemble the input vector. Figure 20 shows the result of the simulation. The neuron population consists of 512 neurons and represents 1 dimension.

![Fig. 20. Communication channel with 512 neurons and 1 dimension. The decoded output of the neuron population tries to resemble the input.](image)
the neuromorphic literature. For the following calculations, we consider two neuron populations each with $N$ neurons and $D$ dimensions. To calculate the number of synaptic events, two approaches are considered. The first approach is the equivalent synaptic event similar to Braindrop [32]. Here, we consider the number of synaptic events it would be if the connection matrix were not factorized, i.e. $NN$ connections between two populations, and each spike causing $N$ synaptic operations. The second approach is to consider the hardware operations related to the synaptic events, i.e. the $ND$ MAC operations done by the MAC array and the $D$ ADD operations for each neuron that has spiked in a time step. Assuming $M$ neurons have spiked in a time step, the number of synaptic operations is $ND + MD$. The results of both approaches are shown in Fig. 21. In the first approach, the energy per equivalent synaptic operation is ca. 10 pJ, surpassing Loihi, which has reported 24 pJ per synaptic operation [15]. In the second approach, for higher dimensions, the energy per synaptic operation reaches 20 pJ, approaches and slightly surpasses Loihi.

Fig. 21. Dynamic power per core, population mean firing rate, energy per synaptic event and energy per equivalent synaptic event, with 512 neurons.

D. Deep Neural Network

Florian

For benchmarking the 2D cross-correlation and matrix multiplication accelerator we select individual layers from Lenet [33], VGG-16 [34], ResNet-50 [35] and MobileNetV2 [36] and compare the results with a comparable execution with ARMNN [37] on the ARM4F core. For a study of complete DNNs, please refer to the simulation study by [13]. We divide the layers to fit into the 128kByte SRAM per PE and optimize to utilize each MAC cell of the accelerator as much as possible. The data is send into each of the 8 PEs and then processed 100000 times in a loop. For time measurements we use the PE clock frequency and supply voltage we sweep over both.

![Image]

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hybrid neural networks, i.e. various crossovers between SNNs and DNNs, can benefit from the SpiNNaker2 architecture. Possibilities of combining MACs with spiking neurons: - as shown, for multi-bit synaptic current input to spiking neurons - Dynamically sparse DNNs, i.e. where information is transmitted only on some form of change, not on a frame-by-frame basis. - a learning-to-learn loop where the inner network is a spiking one and the outer network is a DNN optimizing some target function by modifying the inner spiking network - multi-scale modelling, DNNs realize rate-based or mesoscopic networks, interface with spiking networks go through metrics/results, compare to other hardware

state-of-the-art ML: - Sticker-T [38] achieves 50 TOPs/W 4-bit

Industry overview: [39] [40] Tianjic [41] reports 1278 GOPs/W DNN and 649 GSOPS/W (synaptic operations).

Other architectures to compare: - TrueNorth SNN + eventual Joule per inference for DNN tasks - Loihi - Brain-Drop for equivalent SynOp? - key-word spotting paper, which compares different approaches.

latest BrainScales-2 system has option for analog vector-matrix multiplication and HAGEN-mode HICANN-DLS [42], [43]. - 5-bit input, 6-bit weight, 8-bit neuron activation - 12 mJ per image (conv network) 3 mJ for smaller dense network - SNN: [44] 4uJ per image. Simple MLP, with latency code. They try spike sparsity by adding a term to the loss function

Interesting comparison of SNN and DNN by UC Waterloo for same network architecture: [45] They actually use a conv operation in the input layer.

Maybe add some paper from UNIBI: Christoph Ostrau [46], [47] benchmarking of SNN hardware + CPU + GPU

What actually matters: energy to solution. However no clear benchmarks defined [48] GPUs are also a candidate: see e.g.: [49]: down to 0.3 uJ / synaptic event on TX2. A draft comparison table can be found in file: "CompHybridNeuromorph.ods"

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