A body bias technique for low power full adder using XOR gate and pseudo NMOS transistor

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ABSTRACT

Power dissipation is a major issue in digital circuit design. As technology into developed into range, power and delay becomes vital nanometer parameters to ameliorate the performance of the circuit. To minimize the power consumption many low power techniques such as MTCMOS, stacking, body biasing techniques have been reported. In this paper, a new pseudo NMOS adder circuits have presented. It has designed using transmission gate and body bias technique. Simulation has been accomplished by using SPICE tool. The simulation result show the validity of the proposed techniques is reduces power dissipation from 0.367 mW to 0.267 mW and PDP reduced from 19.311pJ to 13.311pJ. Overall improvement of 29% in power consumption and 30% in PDP has obtained.

Keywords:
Body biasing
Full adder
Pass transmission logic
Pseudo NMOS
XOR gate

1. INTRODUCTION

In the present span, there is a constant advancement in VLSI technology which has caused fast decrease in size and geometries of the transistors and rise in densities of the transistor [1]. Due to this, the circuit consumes huge amount of power and many times it results to silicon failure in chips. High speed operation with low power utilization is becoming a momentous factor in the modern design of various electronics components [2]. The adder is the most critical component that’s extensively used in portable devices i.e. cellular phones, remote sensors, wearable electronics and devices where very low power consumption is needed. Adder has used in the many computational power efficient circuits [3]. The body biasing is a power reduction technique used in many VLSI circuits. The equation which shows how body bias effects the threshold voltage is:

\[ V_{th} = V_{th0} + \gamma(2\phi_B - V_{SB})^{1/2} - (2\phi_B)^{1/2} \]  

Where \( \phi_B \)  Fermi Potential  
\( \gamma \)  body effect coefficient  
\( V_{th0} \)  Threshold voltage with zero \( V_{SB} \)  substrate bias  
\( V_{SB} \)  source to body bias voltage  

The leakage current is the sources of power consumption in the sub threshold circuits; this increase the threshold voltage significantly decreases the sub threshold leakage current. In order to maintain the low threshold voltage \( (V_{th}) \)  in the static CMOS parameters, the body terminals of PMOS has connected to \( V_{DD} \)  and the NMOS body terminal connected to ground. A PMOS transistor are used as a load device and NMOS used as pseudo-NMOS logic. The merit of pseudo-NMOS logic are its high speed (large fan-in NOR gates)

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and low transistor count [4]. The disadvantage is the static power consumption of the pull-up transistor as well as the reduced output voltage and voltage gain, which makes the gate more liable to noise.

In this paper we have proposed a schematic approach to design full adder and this adder are useful in large circuits such as multipliers. In recent year’s different circuit technique have been described to improve the performance of XOR/XNOR gates, static CMOS transistor mainly contains pull-up PMOS and pull-down NMOS networks [5].

In this paper, a XOR circuit has designed using pseudo NMOS, this technique reduce power consumption and number of transistors. Adder has designed with XOR circuit and multiplexer. This proposed circuit has reduced supply voltage, less the power and small time delay reduction using sub threshold and different body biasing techniques [6]. Transmission gate have been also used in designing of carry block of proposed adder circuit. Four different circuits have been proposed in this to implement the full adder. Rest of paper organized as: Section II describes the proposed adder circuit, section III discusses simulation result about of the proposed adder, finally section VI conclude the above.

2. PROPOSED ADDER CIRCUIT

In circuit I, a full adder has been designed using XOR gates with the multiplexer block. XOR gate has designed using pseudo NMOS whereas multiplexer has designed using transmission gates. In circuit II, full adder has been designed using same circuit as circuit I with body biasing of PMOS substrate with \( V_{DD} \) and NMOS substrate with \( V_{SS} = GND \). Supply voltage \( V_{DD} \) had taken between 0.8 to 1.6V. Multiplexer has designed using one transmission gate; it reduced number of the transistors [7-9]. When the body of NMOS has biased with negative supply the channel region increase therefore rises in the threshold voltage. Full adder using XOR and MUX circuit a shown in Figure 1. Body connections in MOS devices a shown in Figure 2.

![Figure 1. Full adder using XOR and MUX circuit](image1)

![Figure 2. Body connections in MOS devices](image2)
the gate to switch faster and the output raise faster which has suppressed the sub threshold leakage current afterwards but only after that current has not required. In proposed technique, PMOS body biasing has done to gate output and NMOS body biasing to a voltage supply $V_{SS}$ ($V_{SS}<0.40V$). Figure 3 a shown in (a) DTPMOS technique (b) PMOS body biasing technique (c) The proposed technique. Shown in Adder using XOR and multiplexer (Circuit-I) a shown in. Adder using body biasing technique with NMOS substrate connected to ground (Circuit-II) a shown in Figure 5. Adder using body biasing and DTPMOS techniques (Circuit-IV) shown in Figure 7. Adder using body biasing with NMOS substrate connected to $V_{ss}$ (Circuit-III) a shown in Figure 6.

![Figure 3](image.png)

**Figure 3.** (a) DTPMOS technique (b) PMOS body biasing technique (c) The proposed technique

![Figure 4](image.png)

**Figure 4.** Adder using XOR and multiplexer (Circuit-I)
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3. RESULTS AND DISCUSSION

The simulations are performed in SPICE 180nm technology with supply voltage variation from [0.8-1.6]V. Substrate biasing has been used to control the leakage current and power consumption. With help of pseudo NMOS and transmission gates number of transistors and dynamic power dissipation had reduced. It has been observed that by using proposed body bias and DTPMOS techniques more than 29% saving in power and more than 1.5% savings in delay are achieved. To evaluate the performance of the proposed body bias scheme, the implemented full adder is simulated at different supply voltages (V_{DD}) from 0.8V to 1.6V and the performance parameters power, delay, PDP are compared. From the comparisons made it is observed that: Also the magnitude of percentage decrease in power is more with the increase in V_{DD}. Particularly delay of operation (V_{DD}=0.8V) the proposed scheme incurred a penalty of 0.8% increase in delay because of less output driving capability due to the increase in threshold voltage of the device. The proposed full adder circuit has achieved more than 30% power delay product saving than the standard CMOS configuration at the different supply voltage V_{DD} from 0.8V to 1.6V. Power dissipation and time delay with variation in VDD as shown in Table 1.

| VDD (V) | Adder with NMOS substrate to GND | Adder with NMOS substrate to V_{SS} | Adder with NMOS substrate to V_{SS} and PMOS Substrate to output |
|---------|---------------------------------|-----------------------------------|---------------------------------------------------------------|
|         | Power (mW) | Time Delay (ns) | PDP (pJ) | Power (mW) | Time Delay (ns) | PDP (pJ) | Power (mW) | Time Delay (ns) | PDP (pJ) |
| 0.8     | 0.045      | 50.670         | 2.280    | 0.034      | 50.957         | 1.732    | 0.027      | 51.090         | 1.379    |
| 0.9     | 0.088      | 50.703         | 4.461    | 0.044      | 50.632         | 2.227    | 0.038      | 50.938         | 1.935    |
| 1       | 0.146      | 50.715         | 7.404    | 0.088      | 50.645         | 4.456    | 0.073      | 50.691         | 3.700    |
| 1.1     | 0.222      | 50.634         | 11.240   | 0.204      | 50.650         | 10.331   | 0.120      | 50.654         | 6.078    |
| 1.2     | 0.316      | 50.612         | 15.993   | 0.305      | 50.643         | 15.446   | 0.181      | 50.642         | 9.166    |
| 1.3     | 0.430      | 50.789         | 21.839   | 0.419      | 50.634         | 21.215   | 0.265      | 50.629         | 13.416   |
| 1.4     | 0.564      | 50.648         | 28.565   | 0.553      | 50.621         | 27.993   | 0.382      | 50.612         | 19.333   |
| 1.5     | 0.720      | 50.637         | 36.458   | 0.708      | 50.596         | 35.821   | 0.532      | 50.603         | 26.920   |
| 1.6     | 0.898      | 50.737         | 45.561   | 0.884      | 50.598         | 44.728   | 0.790      | 50.040         | 39.531   |
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4. CONCLUSION

The full adder circuits using XOR and multiplexer block using body bias and DTPMOS technique have been proposed. Power and PDP is reduced to greater extent than existing method. The simulations are performed in SPICE 180nm technology. The simulation results show that the proposed adder circuit offers improved average power and average delay such as 0.267 mW and 50.601 ns. The circuit operates with more speed after applying biasing and DTPMOS technique. The proposed full adder circuit show less power consumption and PDP with reduced number of transistors. The adder designed shows minimum power dissipation of 0.267mW with PDP of 13.495 pJ at different supply voltage from $V_{DD}$=0.8V to 1.6V.

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