Comparative study on thermal robustness of GaN and AlGaN/GaN MOS devices with thin oxide interlayers

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Compared to traditional silicon-based field-effect transistors (FETs) with a conventional Schottky gate, GaN and AlGaN/GaN MOS devices have gained considerable attention as candidate materials for next-generation power devices.1–3 In addition, because of the high-electron field than SiC, which indicates that GaN-based MOS devices are discussed on the basis of these findings. © 2019 The Japan Society of Applied Physics

1. Introduction

Metal-oxide-semiconductor field-effect transistors (MOSFETs) are the most commonly used semiconductor switching devices, and the quality of gate dielectrics and dielectric/semiconductor interfaces is a determining factor in their performance and reliability. Like the state-of-the-art Si-based integrated circuits, normally off MOSFETs have a large advantage over normally on transistors in fail-safe operation of power devices. Currently, Si-based power devices such as insulated-gate bipolar transistors are widely used, but Si-based devices have physical limitations. Silicon carbide (SiC) and gallium nitride (GaN) have gained considerable attention as candidate materials for next-generation power devices.1–4 Although some problems remain in MOS interface quality,3–6 vertical-type SiC-MOSFETs have already been commercialized and implemented in railway cars and home electronics. GaN is a direct-bandgap semiconductor applicable to optoelectronic devices and also exhibits a wider energy bandgap and higher breakdown field than SiC, which indicates that GaN-based materials have great potential for power-device applications.1–3 In addition, because of the high-electron mobility of two-dimensional electron gas (2DEG) generated at the hetero-interface between GaN-based materials, planar-type AlGaN/GaN heterojunction field-effect transistors (HFETs) with a conventional Schottky gate have been used in advanced high-power wireless communication systems. However, a large gate-leakage current severely degrades device performance and increases the power consumption of the AlGaN/GaN HFETs, so MOS gate structures on the AlGaN surface have been intensively investigated as a potential solution of this problem.10–20 Recently, the higher dielectric breakdown field of GaN-based materials and remarkable progress in free-standing GaN substrates have inspired the development of vertical-type GaN-MOSFETs with ultrahigh blocking-voltage characteristics that surpass those of SiC-based devices. The creation of high-quality MOS structures on GaN and AlGaN surfaces has become a major challenge in the development of next-generation GaN-based power devices. Various insulating materials, such as SiO2, Al2O3, and their oxynitrides, have been investigated for GaN-based MOS applications. Among them, Al2O3 films are widely adopted in compound semiconductor devices. High-quality Al2O3 film can be formed with atomic layer deposition. However, a recent theoretical study revealed its intrinsic problem regarding electron trapping within the film, which is a crucial issue for the threshold-voltage stability of MOSFETs.40 We have successfully demonstrated the impact of nitrogen incorporation into Al2O (AlON) both for suppressing charge trapping and improving the stability of SiC- and GaN-based MOS devices but this approach has the drawback of reducing the energy bandgap of the oxynitride.41 Considering thermal stability and the need for a sufficiently wide energy bandgap, SiO2 is thought to be the most plausible gate dielectric material even for GaN MOS devices but only in cases in which the interface between SiO2 and GaN-based semiconductors is well-controlled. We have reported that an insertion of a thin Ga-oxide (GaOx) interlayer between the SiO2 insulator and GaN surface (SiO2/GaOx/GaN gate stack) is effective in fabricating high-quality GaN-MOS devices.42–44 The post-deposition oxidation (PDO) of the stacks typically at around 800 °C was found to be beneficial for further improving their interface quality. However, the PDO at 1000 °C degraded the interface quality, suggesting a harmful effect of excess thermal treatment on the GaN surface.45 In order to extend this method to AlGaN/GaN MOS-HFETs, we examined initial thermal oxidation of the AlGaN surface in dry oxygen ambient.46 However, the compatibility of the thin oxide interlayers with novel SiO2/GaOx/AlGaN gate stacks and their physical properties have not yet been investigated in detail. In this study, we first evaluated the electrical properties of the AlGaN/GaN MOS capacitors with SiO2/GaOx stacked gate dielectrics. We then conducted systematic physical
characterizations to understand similarities and differences between the oxide interlayers on AlGaN and GaN surfaces in the design of high-quality MOS devices.

2. Experimental methods

The samples used in this study were AlGaN/GaN epitaxial layers grown on Si(111) substrates and n-type GaN epitaxial layers grown on free-standing GaN(0001) substrates. The thickness and Al-content of the AlGaN layers were 50 nm and 20%, respectively. The doping concentration of Si for the n-type GaN epilayers was about $1 \times 10^{16}$ cm$^{-3}$. In fabricating AlGaN/GaN MOS capacitors, the AlGaN surface was wet-cleaned with a diluted hydrochloric (5% HCl) solution for 5 min. Then, 8 nm thick SiO$_2$ films were directly deposited using low-damage plasma-enhanced chemical vapor deposition (PECVD) with tetraethyl orthosilicate (TEOS) and an oxygen–gas mixture. The total gas pressure, TEOS/O$_2$ ratio, RF input power, and substrate temperature were 53 Pa, 1/500 (0.5/250 sccm), 20 W, and 370 °C, respectively. These conditions were the same as in our previous study on GaN-MOS devices. As we reported, PECVD was conducted in a radical oxygen ambient, so the GaN surface was oxidized at the initial stage of SiO$_2$ deposition, resulting in the formation of a thin GaO$_x$ interlayer (SiO$_2$/GaO$_x$/GaN stacked structure). The thickness of the GaO$_x$ layer, interface layer formed on the GaN surface under these conditions was estimated to be around 2 nm. Then, the stacked structures received post-deposition annealing in nitrogen ambient at temperatures ranging from 600 to 1000 °C for 3 min. Ohmic contact to the 2DEG was formed by sputter-deposited Al/Ti bilayers with subsequent contact annealing at 600 °C for 3 min. Finally, Ni gate electrodes were deposited on the gate dielectrics to fabricate AlGaN/GaN MOS capacitors. To characterize the interface quality of the gate stacks, bidirectional capacitance–voltage ($C$–$V$) measurements were conducted at frequencies ranging from 1 kHz to 1 MHz at room temperature.

We also evaluated the thermal stability and decomposition kinetics of the thin GaO$_x$ layers on GaN and AlGaN surfaces fabricated by in situ synchrotron radiation X-ray photoelectron spectroscopy (SR-XPS) and ex situ atomic force microscopy (AFM). For this purpose, after cleaning the GaN and AlGaN surfaces with 5% HCl solution for 5 min, 3 nm thick GaO$_x$ layers were sputter-deposited using a Ga$_2$O$_3$ target in Ar ambient (1.0 Pa, 10 sccm) with an input power of 100 W at room substrate temperature (GaO$_x$/AlGaN, GaO$_x$/GaN samples). To understand the thermal decomposition kinetics in detail, we also fabricated reference sample by depositing the 3 nm thick GaO$_x$ layer directly on a Si(001) substrate (GaO$_x$/Si) for comparison. The Si substrate was cleaned by a diluted hydrofluoric (0.5% HF) solution before GaO$_x$ deposition. SR-XPS analysis of these samples was conducted at the BL23SU beamline in SPring-8. The excitation energy and take-off angle were 1253.6 eV and 90°, respectively. In situ annealing of these thin GaO$_x$ layers grown on various substrates was conducted in an ultrahigh-vacuum analysis chamber. The reference core-level spectra were obtained at a substrate temperature of 400 °C. Then, each sample was subjected to vacuum annealing at target temperatures ranging from 500 to 1000 °C for 5 min in series. In situ SR-XPS spectra were acquired in between the vacuum annealing cycles after the sample was cooled to 400 °C. After the cyclic heating and spectrum acquisition up to 1000 °C, the resulting surface morphology was investigated using ex situ AFM in the air.

3. Results and discussion

3.1. Electrical property of AlGaN/GaN MOS capacitor with GaO$_x$ interface layer

Figure 1 gives the highlight of our previous research on GaN-MOS capacitors with SiO$_2$/GaO$_x$/GaN stacked gate dielectrics fabricated on GaN substrates using the same deposition procedure described in the previous section. As shown in Fig. 1(a), we reported very small hysteresis ($<5$ mV) and negligible frequency dispersion in the bidirectional $C$–$V$ curves taken from the GaN-MOS capacitor after post-annealing in O$_2$ ambient at 800 °C. This result indicates excellent interface properties achieved with the GaO$_x$ interlayer. The interface state density ($D_{it}$) value estimated by a conductance method was actually below the detection limit of our measurement system ($<10^{10}$ cm$^{-2}$ eV$^{-1}$). However, an excess post-annealing at 1000 °C resulted in a significant increase in clockwise $C$–$V$ hysteresis of over 300 mV [Fig. 1(b)], which suggests degradation of the interface quality of the SiO$_2$/GaO$_x$/GaN gate stacks.

In this study, the SiO$_2$ deposition and subsequent annealing procedures were applied to AlGaN surfaces to fabricate AlGaN/GaN MOS capacitors in the same manner as that used for GaN-MOS devices. Considering that initial oxidation of GaN surfaces in dry O$_2$ ambient is promoted by Al addition for AlGaN surfaces, a thin oxide layer composed mostly of GaO$_x$ should be formed between the PECVD-SiO$_2$ and AlGaN surface at the initial stage of SiO$_2$ deposition (SiO$_2$/GaO$_x$/AlGaN stack). Figure 2 shows bidirectional $C$–$V$ curves obtained from the AlGaN/GaN MOS capacitors post-annealed at various temperatures ranging from 600 to 1000 °C. A reasonable two-step response corresponding to 2DEG carriers at the AlGaN/GaN interface (in the negative gate-voltage region) and electron accumulation at the insulator/AlGaN interface (starting at around 0 V) was observed for all capacitors. Slight frequency dispersion in
maximum capacitance at around 4 V originated from the parasitic series resistance such as contact resistance and substrate resistance. Negligible frequency dispersion in the second response at around 0 V demonstrated excellent inter-face quality enabled by the GaO<sub>x</sub> interlayer, as is the case for the GaN substrate. In addition, C–V hysteresis estimated from the second C–V slope appeared to have improved with an increase in the post-annealing temperature. Consequently, extremely small hysteresis (<15 mV) was achieved even for the wide voltage sweep ranging from −10 to +4 V after annealing at 1000 °C [see Fig. 2(c)]. Comparing these results from the MOS capacitors with thin GaO<sub>x</sub> interlayers fabricated on GaN and AlGaN surfaces (Figs. 1 and 2), it can be concluded that the GaO<sub>x</sub> interlayer is beneficial even for the AlGaN surface and that the SiO<sub>2</sub>/GaO<sub>x</sub> stacked dielectric on the AlGaN surface exhibits superior thermal stability than that on the GaN surface.

3.2. Thermal decomposition of GaO<sub>x</sub> layers on GaN and AlGaN surfaces

To understand the physical origins of the superior thermal stability in the SiO<sub>2</sub>/GaO<sub>x</sub>/AlGaN stack over that of the SiO<sub>2</sub>/GaO<sub>x</sub>/GaN stack, thermal decomposition of sputter-deposited thin GaO<sub>x</sub> layers grown on the GaN and AlGaN surfaces was examined by in situ SR-XPS and ex situ AFM analyses. Figure 3 shows the changes in XPS core-level spectra caused by vacuum annealing at various temperatures. The binding energy (BE) and peak intensity of the spectra were calibrated and normalized by N 1s peaks originating from the GaN and AlGaN substrates. As shown in Figs. 3(a) and 3(d), the shape of the N 1s spectra were mostly identical regardless of the annealing. While there were no significant changes in the peak position of O 1s and Ga 3p spectra, the peak intensities markedly decreased with an increase in the annealing temperature. This indicates thermal decomposition of the thin GaO<sub>x</sub> layers from the GaN and AlGaN surfaces. Considering the decrease in both Ga and O content relative to the N signal and the absence of a metallic Ga component on the surfaces, thermal decomposition of the thin GaO<sub>x</sub> layers is thought to be mediated by the formation of volatile Ga<sub>2</sub>O<sub>3</sub> products and their desorption from the surfaces.46

Figure 4 summarizes thermal decomposition of the GaO<sub>x</sub> layers on GaN and AlGaN surfaces. As shown in Fig. 4(a),
decomposition of the thin oxide layers proceeded gradually up to 900 °C on these surfaces. In contrast with the case of the AlGaN surface, a drastic decrease in O 1s signal was observed at 1000 °C only on the GaN surface. The Ga 3p spectrum taken after annealing at 1000 °C was mostly identical to that of the reference GaN surface [see hatched peak in Fig. 3(c)]. This corresponds to the complete removal of the thin GaOx layer. As for the AlGaN surface, significant amount of oxygen and Ga content other than that from the GaN substrate remained even after the vacuum annealing at 1000 °C [Figs. 3(e), 3(f), 4(a)]. Furthermore, when comparing Al 2p core-level spectra obtained from the GaOx/AlGaN sample with the reference spectrum from a bare AlGaN surface, chemical shift components were identified at higher BE as indicated in Fig. 4(b). These findings for the GaOx/AlGaN sample demonstrate the formation of a thermally stable Al1-Ga2-O layer on the AlGaN surface.

The resulting surface morphology of the GaN and AlGaN substrates after the vacuum annealing at 1000 °C was also examined with ex situ AFM. As a result of the complete thermal decomposition of the thin GaOx layer, the GaN surface suffered significant roughening [Fig. 5(a)]. The root mean square (RMS) roughness of the GaN surface was 1.79 nm. Assuming the thermal oxygen transport from the GaOx layer to the GaN surface, highly volatile Ga2O products will be formed by both reduction of the GaOx layer and oxidation (consumption) of the GaN substrate, resulting in surface roughening at high temperatures, as illustrated in Fig. 5(a). Regarding the AlGaN surface, the newly formed thin Al1-Ga2-O layer with stable Al–O bonds will act as an oxygen diffusion barrier and prevent subsequent oxygen transport, as depicted in Fig. 5(b). Consequently, the smooth surface was preserved on the AlGaN surface even after the vacuum annealing at 1000 °C. On the basis of these models and discussions, the deteriorated electrical properties of the SiO2/GaOx/GaN stack after the post-annealing at 1000 °C [see Fig. 1(b)] can be explained as a result of the generation of electrical defects caused by GaOx decomposition and interface roughening. The contrasting improved thermal robustness of the SiO2/GaOx/AlGaN stack can be attributed to the suppressed oxygen transport at the interface due to the thin Al1-Ga2-O reaction layer.

3.3. Control of oxygen transport in thermal decomposition of GaOx

We examined the validity of the proposed model discussed above by intentionally controlling oxygen transport at the interfaces. We attempted to promote oxygen transport from the GaOx layer with a Si substrate that serves as an oxygen absorber. Figure 6 shows changes in Si 2s, O 1s, Ga 3p, and Si 2p core-level spectra induced by the in situ vacuum annealing at various temperatures. Like the GaOx/GaN stack
shown in Fig. 3, thermal decomposition of the GaO$_x$ layer during the vacuum annealing was observed from the gradual decrease in the O 1$s$ and Ga 3$p$ (105 eV) intensities as summarized in Fig. 7. Furthermore, apparent increases in Si–O chemical shift components at around 153.5 eV in Fig. 6(a) and at 102.5 eV in Fig. 6(c), together with the increased O–Si component at around 532 eV in Fig. 6(b), demonstrate successive SiO$_2$ growth on the Si surface mediated by oxygen transport from the GaO$_x$ layer. These findings support the validity of our proposed model that determines thermal robustness of GaN-based MOS gate stacks. We thus conclude that although the post-annealing at high temperatures leads to better SiO$_2$ bulk quality and defect passivation with the Ga–O bonds at the insulator/GaN interface, annealing temperature must be optimized in terms of thermal reactions mediated by oxygen transport at the interfaces. More specifically, insertion of the GaO$_x$ interlayers in GaN-MOS devices is the most effective way to achieve excellent electrical properties, but maximum post-treatment temperature is limited to around 800 °C on the pure GaN substrate. In contrast, the SiO$_2$/GaO$_x$ stack on the AlGaN substrate is advantageous for designing post-annealing treatment up to 1000 °C because of the superior thermal robustness of the interface.

4. Conclusion
Excellent electrical properties of SiO$_2$/GaO$_x$/AlGaN gate stacks were demonstrated with thin GaO$_x$ interlayers and high-temperature post-annealing of up to 1000 °C, in which extremely low $D_{it}$ and negligible $C–V$ hysteresis were achieved in AlGaN/GaN MOS capacitors. In situ SR-XPS analyses showed that thermal decomposition of thin GaO$_x$ layers, which causes electrical degradation of MOS structures, is mediated by oxygen transport at the interface. Additionally, thin Al$_2$Ga$_x$O$_y$ reaction layers with a stable Al–O oxygen diffusion barrier significantly improve the thermal robustness of the SiO$_2$/GaO$_x$ gate stacks fabricated on the AlGaN substrate.

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