Performance Analysis of DC-DC Buck Converter for Renewable Energy Application

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Abstract. This paper presents the analysis of DC-DC buck converter for renewable energy application. Renewable energy resources mostly produce DC voltages that are used DC-DC converter to convert the DC voltage from one level to another level according to different applications. This DC-DC buck converter is used to step down the high level DC voltage to low level DC voltage. By varying the duty cycle, the performance of buck converter in term of its output voltage can be obtained and analysed. Simulations have been performed using PSIM and validated with hardware implementation. All of the results are recorded and showed that very low voltage can be produced using this topology.

1. Introduction
Since most renewable energy produce DC voltage, power electronic circuit such as DC-DC converters are used to convert a DC voltage to a different DC voltage level [1]. Nowadays these converters are widely used with modern electronic application [1]. In photovoltaic (PV) application, maximum power point tracking (MPPT) with buck, boost, buck-boost, cuk, sepic and zeta converters are used commonly for peak power tracking [1][2]. In buck converter, the output voltage is always lower than the input voltage while in boost converter, the output voltage is always higher than input voltage [3]. For buck-boost converter, the output can be either lower than or higher than the input voltage depending on their duty cycle (D). If the duty cycle is higher than 0.5, the output voltage is greater than input and becoming boost converter. On the other hand, if the duty cycle is less than 0.5, the output voltage is lower than the input voltage and becoming buck converter. Figure 1 show the DC-DC converter in PV application with MPPT. Prior to transfer maximum power from the PV panel to the load, load matching must be achieved by varying the duty cycle of the DC-DC converter [4].

![Figure 1. PV system with DC-DC converter and MPPT](image)

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2. Topology of DC-DC buck converter

Basically a DC-DC buck converter consists of power switches such as MOSFET or BJT that will act as switches to control pulses. The circuit topology as shown in Figure 2 consists of MOSFET as power switch and this circuit will step down high level DC voltage to low level DC voltage. The output voltage for this circuit is always smaller than the input voltage [1]. The purpose of this circuit is to produce the output that is purely DC. So, the filter such as LC low pass filter was added in the basic circuit to produce the DC output voltage. When the switch is ON, the diode will become reverse bias and provide energy to the load and inductor. When the switch is OFF, diode will become forward bias and inductor current will flow through the diode. Some of its stored energy will be transferred to the load. This circuit topology can be connected to low load from high level voltage [3] and also can be used in high range step down converter [6].

![Figure 2. Buck converter topology][5]

3. Mathematical analysis of DC-DC buck converter

In this part, the relationship of input voltage, $V_i$, and duty cycle in producing low output voltage related with buck converter are observed. The value of output voltage, $V_o$ depends on the duty cycle. Equation (1) can be used in calculating the output voltage based on the duty cycle, $D$. Equation (2) and (3) are used to calculate the value of inductor while designing the buck converter. In calculating the value of inductor, it must be 25% greater than the minimum value of inductor, $L_{min}$ obtained in Equation (2) to make sure that the circuit will be operated continuously. Furthermore, the maximum inductor current, $I_{max}$ and minimum inductor current, $I_{min}$ can be calculated by using Equation (4), (5) and (6). The value of $I_{min}$ must be positive in order to sustain the continuous current. The value of capacitor, $C$ can be calculated by using Equation (7) with the output ripple voltage which can be defined as a fraction of the output voltage.

\[
D = \frac{V_o}{V_i} \quad (1)
\]

\[
L_{min} = \frac{(1-D)R}{2f} \quad (2)
\]

\[
L = 1.25L_{min} \quad (3)
\]

\[
I_L = \frac{V_o}{R} \quad (4)
\]

\[
I_{max} = I_L + \frac{\Delta I_L}{2} \quad (5)
\]

\[
I_{min} = I_L - \frac{\Delta I_L}{2} \quad (6)
\]
4. Methodology
DC-DC buck converter is designed to step down 5V DC voltage source to 2V and 3V DC output voltages. The selected switching frequency, \( f \) is 25 kHz which is more than 20 kHz to avoid audio noise with 10 ohm load resistance, \( R \) and 10uF capacitor, \( C \). The duty cycle, \( D \) of 0.4 and 0.6 are tested to produce 2 V and 3V DC voltage respectively. The circuit is simulated using PSIM software by using calculated parameters as shown in Equation (1) – (7) and the output waveforms will be analysed further. Low pass filter is included in this circuit to produce purely DC output voltage.

For the hardware implementation, components selection depend upon the maximum current and voltage that components can withstand according to their specification such as MOSFET, inductor, capacitor and resistor. Considering the power switches such as MOSFET, the designer should consider the maximum current and voltage stress during on and off condition that can be handled by the MOSFET and diode. Furthermore, the designer should also consider the maximum current that the inductor can support and the value of its operating frequency to avoid components break down.

The designed hardware is tested, analysed and measured using oscilloscope and digital multimeter. By differentiating the duty cycle of 0.4 and 0.6, the expected result of 2 V and 3 V DC voltages can be produced with this designed circuit of buck converter. MOSFET is triggered using gate driver to switch ON and OFF of the pulses. Similar parameters of inductor, capacitor and resistor which are 150uH, 10uF and 10Ω tested respectively for simulation and hardware testing.

5. Analysis of the simulated results and its hardware implementation.
An analysis of DC buck converter from the simulation results and hardware implementation will be presented. All of the data are recorded and tabulated for further discussion.

5.1. Simulation results
Figure 3 shows the circuit design for DC-DC buck converter that can convert high input of DC voltage to low output DC voltage that had been run in PSIM. Voltmeters that labeling with \( V_{\text{ind}} \), \( V_{\text{diode}} \), \( V_{\text{cap}} \) and \( V_{\text{out}} \) are used to measure the voltage drop across the inductor, diode, capacitor and load resistor respectively.

![Figure 3. The designed of DC buck converter.](image)

Figure 4 shows the output waveform when the duty cycle is 0.4 while Figure 5 shows the output waveform when the duty cycle is 0.6. The output voltage waveform is equal to 2 V for the duty cycle of 0.4 and 3 V for the duty cycle of 0.6. The comparison data was recorded in Table 1 for the duty
cycle of 0.4 and 0.6 respectively. Based on simulation results, the value of output voltage depends on the duty cycle proportionally. When the duty cycle is smaller, the output voltage produced will be lower.

![Figure 4. Output waveforms when the duty cycle is 0.4](image)

![Figure 5. Output waveforms when the duty cycle is 0.6](image)

5.2. Hardware prototype results.
For hardware prototype, the output waveforms and the reading of voltage across the components as well as the current flow through the components will be recorded for further analysis. Table 1 presented that the output voltage across the load is reduced to half as compared to the simulation and calculated value due to some losses from the high voltage drops across the diode and harmonic issues. This problem can be fixed by replacing the diode with second MOSFET that has low voltage drop and
reduce the losses. Figure 6 – 10 show the output waveform across the DC buck converter such as capacitor, diode, inductor, load resistor as well as the inductor current.

**Table 1.** Comparison of hardware results for different duty cycle.

| Parameters | Duty Cycle, D = 0.4 | Duty Cycle, D = 0.6 |
|------------|---------------------|---------------------|
| $V_{\text{out}}$ | 0.970 V | 1.760 V |
| $V_{\text{ind}}$ | 0.330 V | 0.250 V |
| $V_{\text{cap}}$ | 1.090 V | 1.810 V |
| $V_{\text{diode}}$ | 1.040 V | 1.910 V |
| $I_{\text{ind}}$ | 0.019 A | 0.035 A |

![Waveform Images](image1.png)  
(a) ![Waveform Images](image2.png)  
(b)

**Figure 6.** Load resistor output voltage at (a) duty cycle, D of 0.4 (b) duty cycle, D of 0.6.

![Waveform Images](image3.png)  
(a) ![Waveform Images](image4.png)  
(b)

**Figure 7.** Diode voltage at (a) duty cycle, D of 0.4 (b) duty cycle, D of 0.6.

![Waveform Images](image5.png)  
(a) ![Waveform Images](image6.png)  
(b)

**Figure 8.** Inductor voltage at (a) duty cycle, D of 0.4 (b) duty cycle, D of 0.6.
Figure 9. Capacitor voltage at (a) duty cycle, D of 0.4 (b) duty cycle, D of 0.6.

Figure 10. Inductor current (a) duty cycle, D of 0.4 (b) duty cycle, D of 0.6.

5.3. Comparison between simulation and hardware implementation results.
Table 2 shows the comparison between calculation, simulation and hardware prototype results with different duty cycle of the DC buck converter. The experiment varies the duty cycle to analyze the output voltages. The output voltage and current obtained from hardware prototype are different compared to calculation and simulation result by half due to some losses occur during high voltage drops across the diode and harmonic issues

Table 2. Summary results of the designed DC buck converter.

| Parameters | Duty Cycle, D = 0.4 | Duty Cycle, D = 0.6 |
|------------|---------------------|---------------------|
|            | Calculation | Simulation | Hardware | Calculation | Simulation | Hardware |
| $V_{out}$  | 2.0 V       | 2.0 V       | 0.965 V  | 3.0 V       | 3.0 V       | 1.760 V  |
| $I_{ind}$  | 0.2 A       | 0.2 A       | 0.019 A  | 0.3 A       | 0.3 A       | 0.035 A  |

6. Conclusion
This paper presents the analysis of DC buck converter that can be applied for renewable energy application that can be reduced or step down its input voltage to a lower level depending upon the load requirement. By varying the duty cycle of the DC buck converter, the output voltage can be varied proportionally. Even though the hardware implementation shows the output voltage is reduced by half from the simulation and calculated results, this problem can be solved with including a second MOSFET in replacing the diode to reduce the losses and lower voltage drop as compared to diode.

Acknowledgments
The author would like to acknowledge the support from the Fundamental Research Grant Scheme (FRGS) Project code: 9003-00559 from the Ministry of Higher Education Malaysia.
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