Study of spin transport and magnetoresistance effect in silicon-based lateral spin devices for spin-MOSFET applications

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In this paper, we introduce the current status of research and development on silicon-based spin metal-oxide-semiconductor field-effect transistors (Si spin-MOSFETs) in terms of electrical spin injection, spin transport, and spin detection in Si-based lateral spin-valve devices. First, it is important for understanding the spin transport in Si to obtain reliably large spin signals for analyses. By using n+-Si spin-transport layers with a small cross-sectional area of ~0.3 µm², we can observe 50-fold the magnitude of four-terminal nonlocal (NL) magnetoresistance signals and NL Hanle signals at room temperature in previous works. Next, by analyzing these spin signals, we can reliably estimate the spin diffusion length and spin relaxation time of n+-Si at room temperature. Also, we clarify that inter-valley spin-flip scattering is one of the dominant spin relaxation mechanisms in n+-Si at room temperature. Furthermore, we find the crystal orientation effect on spin injection/detection efficiency in n+-Si and discuss the possible origins. Finally, we demonstrate a room-temperature MR ratio of 0.06%, twice as large as that in the previous work.

Key-words: Si spin-MOSFETs, spin transport, spin relaxation, MR

1. Introduction

Spintronics devices typified by hard disc drive (HDD) heads and magnetic random access memories (MRAMs) contribute a lot to the storage and memory industry. From now on, spintronic technologies are expected to contribute to the future semiconductor industry. Silicon-based spin metal-oxide-semiconductor field-effect transistors (Si spin-MOSFETs)1,2 are one of the key spintronics devices for a new logic-in-memory architecture by employing the spin degree of freedom of electrons2,3

Fig. 1 shows the schematic diagram of a Si spin-MOSFET. This basic concept was proposed by Sugahara and Tanaka in 2004.1,3 The general structure of the Si spin-MOSFET consists of a Si-MOSFET and ferromagnetic source (SO) and drain (DR) electrodes. The most important technology is the electrical spin injection and detection at SO and DR electrodes, respectively, through the spin transport in a Si channel layer. When the magnetization direction between SO/DR electrodes forms the parallel state, the current-voltage characteristics of the standard MOSFETs can usually be observed. On the other hand, when the magnetization direction between SO/DR electrodes forms the antiparallel state, the electrical resistance can be changed by depending on the spin-dependent transport in the Si spin-transport channel. This mechanism is available to utilize the magnetization state of SO/DR electrode as an enabler for bit information.1-3 Namely, because of the integration of the two functionalities, nonvolatile memory and logic element, the Si spin-MOSFET is an innovative device for future semiconductor industry. It should be noted that, since the spin diffusion length of Si is relatively long (~2 µm),4 it is possible to combine the Si spin-MOSFETs with integrated circuits.

As one of the most effective possible applications of Si spin-MOSFETs, we focus on a reconfigurable logic device.5 A numerical benchmark for an island-style field programmable gate array (spin FPGA) using Si spin-MOSFETs has been reported by improving standard benchmark tools.5 If the room-temperature operation of the Si spin-MOSFET with a high magnetoresistance (MR) ratio of ~100% is realized, the chip area in the spin FPGA can be significantly reduced, leading to the high speed and low-power-consumption operation.2,5 Thus, it is important for the useful Si spin-MOSFETs to obtain a high MR ratio of ~100%.2,5 The value of the MR ratio can be expressed as

\[
\left( \frac{R_{AP} - R_{P}}{R_{P}} \right) \times 100 = \left( \frac{\Delta R}{R_{P}} \right) \times 100, \quad (1)
\]
where $R_{F}$ and $R_{D}$ are the resistances between SO and DR electrodes under the antiparallel and parallel states, respectively. From the one-dimensional diffusion model proposed by A. Fert et al.\(^6\) and F. J. Jedema et al.\(^7\), Eq. (1) in Si-based lateral spin-valve (LSV) devices can be modified as

$$
\frac{\Delta R}{R_{P}} \times 100 = \frac{2(\beta r_{FM} + P r_{b})^2}{A} \times 100,
$$

(2)

where $P$ is the interface spin polarization of the spin injector and detector contacts, $r_{b}$ is the interface resistances between the ferromagnetic electrodes and the used Si layer, $r_{FM}$ and $r_{Si}$ are the spin resistance of the ferromagnetic electrode and the used Si channel layer, respectively. $d$ is the distance between ferromagnetic electrodes, and $\beta$ is the bulk spin polarization of the ferromagnet. $\Delta R = (\beta r_{FM} + P r_{b}) d \lambda_{Si}$.

The spin diffusion constant and the spin lifetime, respectively) is influenced by several unknown parameters. If Si spin-MOSFETs with a MR ratio of ~100% were considered based on Eq. (2), we can understand that it is essential to decrease $d$, to enhance $P$, and to reduce $r_{b}$.

In this review, we introduce our recent progress of the research and development for Si spin-MOSFETs on the basis of electrical spin injection, spin transport, and spin detection in Si-based LSV devices. First, we show a reliable detection of room-temperature spin transport in Si by fabricating fine-pitch devices with a small cross-sectional area of ~0.3 μm. By analyzing the obtained data, reliable room-temperature spin diffusion length and spin lifetime in $n$-Si can be estimated. Next, considering the temperature dependence of the spin diffusion length and spin lifetime, we can also regard the spin relaxation mechanism in $n$-Si as a consequence of impurity- and phonon-induced inter-valley spin-flip scattering in the conduction band valleys. Furthermore, we find the crystal orientation effect on spin injection/detection efficiency in Si-based LSV devices. By combining these results, we can observe the highest MR ratio of 0.06% at room temperature.

Finally, as future prospects in Si spin-MOSFETs, we propose several plans to improve the MR ratio up to 100%.

### 2. Current status

#### 2.1 Spin injection and detection in Si

Since the observation of room-temperature spin accumulation signals in Si\(^8\), lots of studies of three-terminal and four-terminal NL Hanle measurements in Si-based devices have been reported.\(^9-32\) So far, the value of $P$ estimated from the simple models has been discussed for Si spin-MOSFETs. Recent studies on Ge-based LSV devices\(^33-34\) have reported that the value of $P$ is almost the same value as the spin injection/detection efficiency estimated from NL spin transport measurements. Thus, the spin injection/detection efficiency obtained by the previous three-terminal and four-terminal NL Hanle measurements can roughly be regarded as the value of $P$.

Fig. 2 shows the trend in the reported values of $P$ for Si-based devices.\(^22-31\) We find that relatively high $P$ values have been reported year by year by using ferromagnet/MgO tunnel barrier contacts. On the other hand, the reported MR ratios measured by local two-terminal measurements were quite small less than 0.01% at room temperature,\(^15, 22, 24, 30, 32\) largely inconsistent with the expected values from Eq. (2). This means that it is difficult to rationalize the improvement of reported $P$ values in Fig. 2. At this stage, the precise origin of the above discrepancy in Si-based devices is still unclear. To precisely discuss the value of $P$ as much as possible, we firstly use the small sized LSV devices for detecting reliable spin signals at room temperature.

Fig. 3 shows a typical structure of a schematic LSV device fabricated here. A channel layer consists of a Si (~70 nm) on insulator (SOI) for confining the spin transport region to the SOI layer. When the magnetization states of ferromagnetic electrodes (FM1 and FM2) can be modulated by applying external magnetic fields, the NL and local spin transport signals corresponding to the magnetization state can be observed. For this reason, the width of each FM electrode ($W_{FM1}$ or $W_{FM2}$) is generally designed to be much shorter than the length of channel width ($L_{CH}$). However, the long length of the FM electrode may cause the suppression of the

![Fig. 2](image-url) (Color online) Trend in reported spin injection/detection efficiency ($P$) for Si-based devices.
magnitude of spin signals due to the large variation of the spin transport length in the Si channel region. As a result, the analytical data may include relatively large errors compared to the actual values, as indicated in Fig. 2. Thus, as mentioned above, we fabricated fine LSV devices with a small cross-sectional area of $0.305 \mu m^2$ by employing a short length of $L_{CH}$ ($\sim 7.0 \mu m$) in the $n^+\text{-Si}$ layer. Here, we adopted CoFe and MgO as the ferromagnet and the tunnel barrier materials, respectively, because we have observed spin signals in $n^+\text{-Si}$ by using CoFe/MgO contacts in previous studies. In theory, Fert et al. have reported that thinned and fine-pitch channels in semiconductor-based LSV devices can enhance the spin signals due to the increase of the spin accumulation in semiconductors.

To obtain reliable values of spin signals, the use of the fine LSV devices is meaningful.

2.2 Spin diffusion length and spin lifetime in $n^+\text{-Si}$

In general, $|\Delta R_{NL}|$ can be expressed by the following equation:

$$|\Delta R_{NL}| = \frac{4 |P_{inj}| |P_{det}| r_h r_s b^2 \exp \left( \frac{-d}{\lambda_{Si}} \right)}{S_N \left( (2r_h + r_s)^2 - r_s^2 \exp \left( \frac{-2d}{\lambda_{Si}} \right) \right)}, \quad (3)$$

where $P_{inj}$ and $P_{det}$ are spin polarizations of the electrons in Si created by the spin injector and detector, respectively. $S_N$ is the cross-sectional area ($0.305 \mu m^2$) of the $n^+\text{-Si}$ layer. We examined the dependence of $|\Delta R_{NL}|$ on $d$ at 303 K in Fig. 5. Since $|\Delta R_{NL}|$ is much larger than that in previous work, we can observe spin signals for the LSV device with $d = 3.75 \mu m$ (see inset of Fig. 5) and an exponential decay of $|\Delta R_{NL}|$ with an increase in $d$ is seen. Using Eq. (3), we extract the room-temperature $\lambda_{Si}$ of $\sim 0.95 \mu m$. We also extracted $\lambda_{Si}$ ($= \sqrt{D\tau_{Si}}$) from the fitting of the NL Hanle-effect curves based on the one-dimensional spin drift diffusion model. The solid curves in the inset of Fig. 4(b) show representative results of the fitting to Eq. (2) in Ref. 7). As a result, the $\tau_{Si}$ and $D$ values at 303 K for the $n^+\text{-Si}$ layer are estimated to be 0.7 ns and 20 cm$^2$/ns, respectively, leading to a $\lambda_{Si}$ of 1.2 µm at 303 K, also consistent with the above framework.

Here, we summarize the reported values of $\lambda_{Si}$ and $r_{Si}$...
for $n^+$-Si with various carrier concentrations and measurement temperatures in Table 1. There are only four experimental reports for the $\lambda_{Si}$ and $\tau_{Si}$ values at room temperature. In general, to estimate the $\lambda_{Si}$ and $\tau_{Si}$ values by measuring four-terminal NL magnetoresistance signals, accurate micro-fabrication processes for LSV devices with various $d$ are necessary. If the fabricated LSV devices have some fluctuation of the contact size and electrical characteristics, they can cause the scattering of the values of $|\Delta R_{NL}|$ for large LSV devices. Our estimated $\lambda_{Si}$ values are relatively consistent with other reports in Table 1. However, we can find that the $\tau_{Si}$ values are largely different from those in Table 1. Therefore, it is important for discuss the spin relaxation mechanism in $n^+$-Si to use the small sized LSV devices showing large spin signals at room temperature.

### 2.3 Spin relaxation mechanism in $n^+$-Si

The spin relaxation in undoped Si has so far been discussed in terms of the Elliott-Yafet mechanism including the conduction-band valley anisotropy. Recently, Dery and co-workers reexamined the Elliott-Yafet mechanism in multivalley semiconductors. Consequently, they predicted the detailed spin relaxation due to electron-phonon interactions in the multivalley conduction band in Si. In addition, they also suggested donor-driven spin relaxation for doped Si. This means that the conduction band dominated by the multivalley nature causes short-range spin-flip scattering due to the central-cell potential of impurities doped in Si. In the following, we simply comment on the temperature dependence of $\tau_{Si}$ in terms of these theories.

For all the small sized LSV devices, we measured the dependence of $|\Delta R_{NL}|$ on $d$ at various temperatures, and then $\lambda_{Si}$ as a function of temperature was obtained. Using the relation, $\lambda_{Si} = \frac{D \tau_{Si}}{\mu}$, we can simply calculate the value of $\tau_{Si}$. Here, we measured temperature-dependent channel mobility ($\mu$) using the Hall-bar device of the used $n^+$-Si layer (the inset of Fig. 6) and estimated the $D$ values from the following equation:

$$D = 2 \left( \frac{k_B T}{|q|} \right) F_{1/2}(\xi) \left( \frac{1}{F_{1/2}(\xi)} \right), \quad (4)$$

![Fig. 5](Color online) $d$ dependence of $|\Delta R_{NL}|$ at 303 K. Dashed line shows results of fitting to Eq. (3). Inset is four-terminal NL magnetoresistance curve at 303 K for a device with $d = 3.75$ μm. Figure reprinted with permission from 35). Copyright (2016) by American Physical Society.

### Table 1

| Carrier density at R.T. ($/{\mathrm{cm}}^2$) | Tunnel barrier | FM | Method | Temperature (K) | $W_{CH}$ (μm) | $\lambda_{Si}$ (μm) | $\tau_{Si}$ (μsec) | Reference |
|-----------------------------------------|----------------|-----|--------|---------------|--------------|-----------------|------------------|----------|
| $8 \times 10^{19}$                      | MgO/Mg         | Fe  | 4TH    | 4             | 180          | 1.0 (fix)       | 2.0              | [17]     |
| $2.7 \times 10^{19}$                    | MgO            | Fe  | 4TH    | 10            | 40           | 2.2             | 18               | [18]     |
| $2.7 \times 10^{19}$                    | MgO            | Fe  | 4TH    | 300           | 40           | 1               | 2.5              | [18]     |
| $2 \times 10^{19}$                      | MgO            | CoFe| NL     | 77            | 100          | 1.6             | -                | [30]     |
| $1.5 \times 10^{19}$                    | MgO            | CoFe| 4TH    | 20            | 100          | 0.98            | 4.16             | [19]     |
| $1 \times 10^{19}$                      | MgO            | Fe  | 4TH    | 8             | 21           | 2.6             | 9.4              | [28]     |
| $1 \times 10^{19}$                      | MgO            | Fe  | NL     | 8             | 21           | 2.25            | -                | [20]     |
| $5 \times 10^{19}$                      | MgO            | Fe  | 4TH    | 8             | 21           | ~2.0            | 10               | [29]     |
| $1.8 \times 10^{19}$                    | MgO            | Fe  | 4TH    | 8             | 21           | 2.0             | 10               | [9]      |
| $1.8 \times 10^{19}$                    | MgO            | Fe  | 4TH    | 300           | 21           | ~0.6            | 0.6              | [9]      |
| $3 \times 10^{18}$                      | Al$_2$O$_3$     | Fe  | 4TH    | 10            | 100          | -               | 0.9              | [21]     |
| $2 \times 10^{19}$                      | MgO            | CoFe| NL     | 303           | 7            | 0.95            | 2.1              | [35]     |
| $2 \times 10^{19}$                      | MgO            | CoFe| 4TH    | 303           | 7            | 1.2             | 0.7              | [35]     |
where $k_B$ is Boltzmann’s constant, $T$ is the temperature, $q$ is electron’s charge, and $f_{\mu}(\xi)$ is the Fermi-Dirac integral $f_{\mu}(\xi) = \int_{0}^{\infty} \frac{x^\mu \exp(-x) + 1}{\exp(x) + 1} dx$. The obtained temperature dependence of $\tau_{Si}$ is shown as solid symbols in Fig. 6. It should be noted that $\tau_{Si}$ is ~16 ns at low temperatures and is largely suppressed to ~2.1 ns with increasing temperature, implying the presence of strong temperature dependence. By considering Eqs. (2)–(5) in Ref. 35, we can fit the experimental data (see gray dashed curve). From the theories proposed by Dery and co-workers 41-42,44, the spin relaxation mechanism in n+-Si is dominated by the impurity-induced spin scattering at low temperatures ($T < 50$ K) and the phonon-induced intervalley spin-flip scattering above 50 K,35 respectively. We note that the temperature dependence of $\mu$ shown in the inset of Fig. 6, also indicates the presence of the strong phonon-induced carrier scattering above 50 K. Therefore, we should regard the temperature-dependent $\mu$ for n+-Si as an important factor for understanding the spin relaxation mechanism in n+-Si.

2.4 Crystal orientation effect on spin injection/detection efficiency in n+-Si

The crystal orientation effect on the spin injection in semiconductors has been discovered in (Ga,Mn)As/GaAs LSV devices.46 That is, for epitaxial ferromagnetic (Ga,Mn)As electrodes, it is well known that there is the tunneling anisotropic spin polarization depending on the crystal orientation of GaAs.46 After that, using three-terminal Hanle-effect measurements, similar phenomena for various ferromagnetic metal electrodes have been observed in Si.47-48 According to the previous works on Si 47-48, the anisotropy of the tunneling spin polarization is attributed to the magnetization direction of ferromagnetic electrodes relative to the crystal orientation of Si.

Here, we also investigated the effect of crystal orientation on the pure spin current transport in Si-LSV devices with epitaxially grown CoFe/MgO tunnel electrodes. When the crystal orientation of the spin-transport channel in LSV devices is changed from <110>, which is a conventional cleavage direction, to <100>, the magnitude of the spin signals is always enhanced at various conditions, as shown in Fig. 7. From the analyses based on the one-dimensional spin diffusion model, we revealed that the spin-diffusion length and spin lifetime between Si<100> and Si<110> LSV devices are comparable, while the spin injection/detection efficiency in Si<100> LSV devices is evidently larger than that in Si<110> ones. This study clarified that it is important for Si-based spintronic applications to consider the crystal orientation effect.

We infer that there are two possible origins of the difference in the spin injection/detection efficiency between Si<100> and Si<110> LSV devices.49 One is the presence of the tunneling anisotropic spin polarization, being due to the magnetization direction of the ferromagnetic electrodes relative to the crystal orientation of semiconductors 46-48, discovered in (Ga,Mn)As/GaAs LSV devices.46 Although the origin of the presence of the tunneling anisotropic spin polarization has not been discussed in detail 46-48, the magnetization direction of ferromagnetic electrodes relative to the crystal axis in between Si<100> and Si<110> LSV devices should also be considered. The other is the crystallographic effect of the conduction band valleys in Si. Fig. 8(c) illustrates the conduction-band valley positions in the $k$-space in Si; six valleys are located close to the $X$ point along <100>. On the basis of the calculation with a full-orbital tight-binding model, similar to those in previous reports 50-51, we can roughly obtain the spin-resolved tunnel current $I_\uparrow$ and $I_\downarrow$ for a ferromagnet (FM)/MgO/Si junction.46 Figs. 8(a) and (b) show the momentum-resolved $I$ for spin-up ($\uparrow$) and spin-down ($\downarrow$), respectively. Not only the component of $I$ around the $Gamma$ point but also that around the $X$ point can be seen evidently in both spin states because the six conduction-band valleys are located close to the $X$ point along <100> in the $k$-space in Si. That is, the tunneling spin polarization (TSP) in the FM/MgO/Si junctions can
be affected by the $X$-point component in the electrical spin injection and detection. Fig. 8(d) presents the calculated TSP as a function of bias voltage applied to the CoFe/MgO/Si junction. Here the negative bias voltage means the condition of the spin injection from CoFe/MgO contacts into Si. The magnitude of TSP is governed by the $\Gamma$-point component in all the calculated bias conditions, but the bias-dependent behavior is evidently affected by the $X$-point one. From these considerations, we can expect that the conduction band valleys in Si contribute to the anisotropy of the electrical spin injection and detection through the FM/MgO/Si junctions. For enhancing the MR ratio in Si spin-MOSFETs, it is important to consider the magnetization direction of the ferromagnetic contacts relative to the Si crystal axis.

2.5 Magnetoresistance at room temperature in Si<100> devices

As described in Introduction, a large MR ratio of $\sim$100% is required for Si spin-MOSFET applications. Finally, we discuss the two-terminal local signals ($\Delta R_{\text{local}}$) for two kinds of LSV devices consisting of the Si<100> or Si<110> spin-transport channel with a small size (0.305 $\mu$m$^2$) cross section. Fig. 9 shows a room-temperature local spin signal for a Si<100> LSV device [a], together with that for a Si<110> one [b]. Relatively large values of $\Delta R_{\text{local}}$ can reproducibly be observed for Si<100> LSV devices compared to those for Si<110> ones. The maximum MR ratio is 0.06% at room temperature,$^{52}$ It should be noted that this value is twice as large as that in the previous work.$^{32}$ We suggest that, for Si spin-MOSFETs with the large MR ratio, it is important to consider the crystal orientation effect described in section 2.4.

3. Future prospects for Si spin-MOSFETs

Although we have improved the MR ratio in Si-based LSV devices up to 0.06% at room temperature, there is still an enormous gap between the target value (100%) and the current value (0.06%) unfortunately. As one of the reasons, we consider that the phonon-induced spin scattering in n+-Si influences, as discussed in section 2.3. Since the contribution of the phonon-induced intervalley spin-flip scattering was dominant as the spin relaxation in n+-Si, we should utilize a strained-Si, which can lift the valley degeneracy of the conduction band$^{53-54}$, as a spin-transport channel to suppress the phonon-induced intervalley spin-flip scattering at room temperature.

In our opinion, the enhancement of spin injection/detection efficiency of the spin injector and detector electrodes is the most important for obtaining large MR ratios. As mentioned in section 2.1, the values of $P$ have been scattered from device to device because of large sized LSV devices. In this study, we used small sized LSV devices and obtained values of $P < 0.2$, estimated from NL measurements. With respect to this, we will use highly ordered ferromagnetic Heusler alloys as ferromagnetic electrodes to obtain large spin polarization, as reported in previous works$^{55-56}$. Although we have so far fabricated Co$_2$FeSi/MgO/Si LSV devices and observed the spin signals even at room temperature,$^{19}$ the MR ratio has been still small less than 0.01%. Because of the large lattice mismatch between Co$_2$FeSi and MgO ($\sim$5%), the highly ordered
Based LSV devices ($d = 0.5$ μm). Here, $P$ is the spin injection/detection efficiency, $r_b$ and $r_{Si}$ are the spin resistance of the ferromagnet/MgO interface and the $n^+$-Si layer, respectively.

Co$_2$FeSi could not be formed for Si-based LSV devices. In future, we will select highly spin-polarized Heusler alloys having a small lattice mismatch for MgO.

Finally, we will comment on the importance of reducing the interface resistance between the ferromagnetic electrodes and Si. Fig. 10 shows the dependence of the interface resistance on MR ratio estimated from Eq. (2), together with the maximum data we presented. When the spin injection/detection efficiency $P$ is enhanced, one can clearly see the improvement of MR ratio. However, we have used a MgO tunnel barrier between a ferromagnet and Si. As a result, the interface resistance is so high, leading to the suppression of the MR ratio because of the large $R_b$ in the devices. For realizing the MR ratio of ~100%, it is also important to reduce the interface resistance in addition to the enhancement of the spin injection/detection efficiency, as shown in Fig. 10. Regarding this point, we will use ferromagnet/Si Schottky tunnel contacts without using MgO. Recently, Co-based Heusler alloy/Ge Schottky tunnel contacts with a low contact resistance of less than 0.5 kΩ µm were simultaneously demonstrated for Ge-based LSV devices.

In future, we should also explore Co-based Heusler alloy/Si Schottky tunnel contacts for high MR ratios in Si-based LSV devices.

After achieving the above three improvements, suppression of the room-temperature spin relaxation, enhancement in the spin injection/detection efficiency, and reduction in the interface resistance, a high MR ratio of 100% in Si-based LSV devices can be obtained for high-performance Si spin-MOSFETs. Therefore, we will further explore the developments of the optimum Si channel and spin injector/detector contacts in future.

4. Conclusion

Because of two functionalities, i.e., the nonvolatile memory and the logic element, Si spin-MOSFET with a MR ratio of 100% is one of the key spintronics devices for low-power-consumption Si LSI. This paper has introduced our recent progress of the development on Si spin-MOSFETs in terms of electrical spin injection, spin transport, and spin detection in Si-based LSV devices. First, by using $n^+$-Si spin-transport layers with a small cross-sectional area of ~0.3 μm², we observed 50-fold the magnitude of four-terminal NL magnetoresistance signals and NL Hanle signals at room temperature in the previous work. By analyzing these spin signals, we were able to estimate the reliable spin diffusion length and spin relaxation time of $n^+$-Si at room temperature. Next, we clarified that the inter-valley spin-flip scattering is the dominant spin relaxation mechanism in $n^+$-Si at room temperature. Furthermore, we found the crystal orientation effect on spin injection/detection efficiency in $n^+$-Si and discussed the possible origins. From these experiments, we demonstrated a room-temperature MR ratio of 0.06%, twice as large as that in the previous work. To obtain a high MR ratio of 100% in Si-based LSV devices for high-performance Si spin-MOSFETs, suppression of the room-temperature spin relaxation, enhancement in the spin injection/detection efficiency, and reduction in the interface resistance should be further explored.

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References

1) S. Sugahara and M. Tanaka: Appl. Phys. Lett., 84, 2307 (2004).
2) Y. Saito, T. Inokuchi, M. Ishikawa, H. Sugiyama, T. Marukame, and T. Tanamoto: J. Elec. Chem. Soc., 158, H1068 (2011).
3) M. Tanaka and S. Sugahara: IEEE Trans. Electron Devices, 54, 961 (2007).
4) S. M. Thompson, D. Pugh, D. Loraine, C. L. Dennis, J. F. Gregg, C. Shirsathikul, and W. Allen: Spintronic Materials and Technology, edited by Y. Xu and S. Thompson (CRC Press, USA), 249 (2008).
5) T. Tanamoto, H. Sugiyama, T. Inokuchi, T. Marukame, M. Ishikawa, K. Ikegami, and Y. Saito: J. Appl. Phys., 109, 07C312 (2011).
6) A. Fert and H. Jaffrè: Phys. Rev. B, 64, 184420 (2001).
7) F. J. Jedema, H. B. Heersche, A. T. Filip, J. J. A. Baselmans, and B. J. van Wees: Nature, 416, 713 (2002).
8) S. P. Dash, S. Sharma, R. S. Patel, M. P. Jong, and R. Jansen: Nature, 462, 491 (2007).
9) T. Suzuki, T. Sasaki, T. Okawa, M. Shiraishi, Y. Suzuki, and K. Noguchi: Appl. Phys. Express, 4, 023003 (2011).
10) C. H. Li, O. M. J. van’t Erve, and B. T. Jonker: Nature Commun., 2, 245 (2011).
11) Y. Ando, K. Kasahara, S. Yamada, Y. Maeda, K. Masaki, Y. Hoshi, K. Sawano, M. Miyao, and K. Hamaya: Phys. Rev. B, 86, 035320 (2012).
12) M. Ishikawa, H. Sugiyama, T. Inokuchi, K. Hamaya, and Y. Saito: *Appl. Phys. Lett.*, **100**, 232404 (2012).
13) R. Jansen, S. P. Dash, S. Sharma, and B. C. Min: *Semicond. Sci. Technol.*, **27**, 083001 (2012).
14) H. Sugiyama, M. Ishikawa, T. Inokuchi, T. Tanamoto, Y. Saito, and N. Tezuka: *Solid State Commun.*, **190**, 46 (2014).
15) Y. Saito, T. Tanamoto, M. Ishikawa, H. Sugiyama, T. Inokuchi, K. Hamaya, and N. Tezuka: *J. Appl. Phys.*, **115**, 17C514 (2014).
16) A. Spiesser, Y. Fujita, H. Saito, S. Yamada, K. Hamaya, S. Yuasa, and R. Jansen: *Appl. Phys. Lett.*, **114**, 242401 (2019).
17) S. Sato, R. Nakano, T. Hoda, and M. Tanaka: *Phys. Rev. B*, **96**, 235204 (2017).
18) A. Spiesser, H. Saito, Y. Fujita, S. Yamada, K. Hamaya, S. Yuasa, and R. Jansen: *Phys. Rev. Appl.*, **8**, 064023 (2017).
19) M. Ishikawa, H. Sugiyama, T. Inokuchi, K. Hamaya, and Y. Saito: *Appl. Phys. Lett.*, **107**, 092402 (2015).
20) T. Sasaki, T. Oikawa, T. Suzuki, M. Shiraishi, Y. Suzuki, and K. Tagami: *Appl. Phys. Express*, **2**, 053003 (2009).
21) O. M. J. van’t Erve, C. Awo-Affouda, A. T. Hanbicki, C. H. Li, P. E. Thompson, and B. T. Jonker: *IEEE Trans. Magn.*, **56**, 2343 (2009).
22) Y. Saito, M. Ishikawa, T. Inokuchi, H. Sugiyama, T. Tanamoto, K. Hamaya, and N. Tezuka: *IEEE Trans. Magn.*, **48**, 2739 (2012).
23) M. Ishikawa, H. Sugiyama, T. Inokuchi, T. Tanamoto, K. Hamaya, N. Tezuka, and Y. Saito: *J. Appl. Phys.*, **114**, 243904 (2013).
24) Y. Saito, T. Inokuchi, M. Ishikawa, T. Ajay, and H. Sugiyama: *AIP Adv.*, **7**, 055937 (2017).
25) R. Jansen, A. Spiesser, H. Saito, Y. Fujita, S. Yamada, K. Hamaya, and S. Yuasa: *Phys. Rev. Appl.*, **10**, 064050 (2018).
26) A. Spiesser, Y. Fujita, H. Saito, S. Yamada, K. Hamaya, W. Mizubayashi, K. Endo, S. Yuasa, and R. Jansen: *Phys. Rev. Appl.*, **11**, 044020 (2019).
27) A. Dankert, R. S. Dulul, and S. P. Dash: *Sci. Rep.*, **3**, 3196 (2013).
28) T. Sasaki, T. Oikawa, T. Suzuki, M. Shiraishi, Y. Suzuki, and K. Noguchi: *IEEE Trans. Magn.*, **46**, 1436 (2010).
29) M. Shiraishi, Y. Honda, E. Shihoko, Y. Suzuki, T. Shinjou, T. Sasaki, T. Oikawa, K. Noguchi, and T. Suzuki: *Phys. Rev. B*, **83**, 241204(R) (2011).
30) Y. Saito, M. Ishikawa, H. Sugiyama, T. Inokuchi, K. Hamaya, and N. Tezuka: *J. Appl. Phys.*, **117**, 17C707 (2015).
31) M. Kamenou, Y. Ando, E. Shiko, T. Shinjou, T. Sasaki, T. Oikawa, Y. Suzuki, T. Suzuki, and M. Shiraishi: *Appl. Phys. Lett.*, **101**, 122413 (2012).
32) T. Sasaki, T. Suzuki, Y. Ando, H. Koike, T. Oikawa, Y. Suzuki, and M. Shiraishi: *Appl. Phys. Lett.*, **104**, 052404 (2014).
33) M. Tsukahara, M. Yamada, T. Naito, S. Yamada, K. Sawano, V. K. Lazarov, and K. Haimaya: *Appl. Phys. Express*, **12**, 033002 (2019).
34) Y. Fujita, M. Yamada, M. Tsukahara, T. Naito, S. Yamada, K. Sawano, and K. Hamaya: *Phys. Rev. B*, **100**, 024431 (2019).
35) M. Ishikawa, T. Oka, Y. Fujita, H. Sugiyama, Y. Saito, and K. Hamaya: *Phys. Rev. B*, **95**, 115302 (2017).
36) A. Fort, J.-M. George, H. Jaffrès, and R. Mattana: *IEEE Trans. Electron Devices*, **54**, 921 (2007).
37) S. Takahashi and S. Maekawa: *Phys. Rev. B*, **67**, 052409 (2003).
38) H. Jaffrès, J.-M. George, and A. Fort: *Phys. Rev. B*, **82**, 140408(R) (2010).
39) I. Appelbaum, B. Huang, and D. J. Monisma: *Nature*, **447**, 295 (2007).
40) B. Huang, D. J. Monisma, and I. Appelbaum: *Phys. Rev. Lett.*, **99**, 177209 (2007).
41) P. Li and H. Dery: *Phys. Rev. Lett.*, **107**, 107203 (2011).
42) Y. Song and H. Dery: *Phys. Rev. B*, **86**, 085201 (2012).
43) J. L. Cheng, M. W. Wu, and J. Fabian, *Phys. Rev. Lett.*, **104**, 016601 (2010).
44) Y. Song, O. Chalaev, and H. Dery: *Phys. Rev. Lett.*, **113**, 167201 (2014).
45) M. E. Flatté and J. M. Byers: *Phys. Rev. Lett.*, **84**, 4220 (2000).
46) A. Einwanger, M. Ciorga, U. Wurstbauer, D. Schuh, W. Wegscheider, and D. Weiss: *Appl. Phys. Lett.*, **95**, 152101 (2009).
47) S. Sharma, S. P. Dash, H. Saito, S. Yuasa, B. J. van Wees, and R. Jansen: *Phys. Rev. B*, **86**, 165308 (2012).
48) S. Sharma, A. Spiesser, H. Saito, S. Yuasa, B. J. van Wees, and R. Jansen: *Phys. Rev. B*, **87**, 085307 (2013).
49) M. Ishikawa, M. Tsukahara, S. Honda, Y. Fujita, M. Yamada, Y. Saito, T. Kimura, H. Itoh, and K. Hamaya: *J. Phys. D: Appl. Phys.*, **52**, 085202 (2019).
50) S. Honda, H. Itoh, J. Inoue, H. Kurebayashi, T. Trypiniotis, C. H. W. Barnes, A. Hirohata, and J. A. C. Bland: *Phys. Rev. B*, **78**, 245316 (2008).
51) S. Honda, H. Itoh, and J. Inoue: *J. Phys. D: Appl. Phys.*, **43**, 135092 (2010).
52) M. Ishikawa, M. Tsukahara, M. Yamada, Y. Saito, and K. Hamaya: *IEEE Trans. Magn.*, **54**, 1400604 (2018).
53) O. Chalaev, Y. Song, and H. Dery: *Phys. Rev. B*, **95**, 035204 (2017).
54) S. Takagi, T. Mizuno, T. Tetsuka, N. Sugiyama, S. Nakaharai, T. Numata, J. Koga, and K. Uchida: *Solid-State Electron.*, **49**, 684 (2005).
55) T. Kimura, N. Hashimoto, S. Yamada, M. Miyao, and K. Hamaya: *NPG Asia Mater.*, **4**, e9 (2012).
56) K. Hamaya, Y. Fujita, M. Yamada, M. Kawano, S. Yamada, and K. Sawano: *J. Phys. D: Appl. Phys.*, **51**, 393001 (2018).

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