A Comparison of DC/AC and DC/DC Modular Multilevel Energy Conversion Processes

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Using strings of cascaded submodules for multilevel dc/ac conversion has attracted considerable attention owing to the widespread popularity of the modular multilevel converter (MMC). Recently, it has been shown that such conventional submodule strings can be adapted to achieve single-stage dc/dc conversion. Although the modular string configurations for dc/ac and dc/dc conversion are similar, the underlying power transfer mechanisms employed by each differ significantly. This paper compares the dc/ac and dc/dc energy conversion processes for series-cascaded submodules and highlights their key similarities and differences. In addition, converter operation and control requirements for dc/ac and dc/dc conversion are discussed and compared. A capacitor voltage regulation scheme for dc/dc conversion is proposed, whereby vars generation can be arbitrarily allocated between the converter arms in order to maximize conversion efficiency. It is shown that single-stage dc/dc conversion can reduce converter cost and operating losses by up to 50% as compared to conventional cascaded dc/ac stages, i.e. dc/ac-ac/dc conversion.

Keywords: DC/AC converter, DC/DC converter, HVDC, modular converter

1. Introduction

The well known modular multilevel converter (MMC)1–7 uses strings of cascaded submodules (SMs) to perform dc/ac conversion. These SMs constitute modular voltage cells (i.e. each SM contains a local energy storage capacitor) that can be individually switched “in” or “out” along the string to create a multilevel ac voltage waveform. By series-stacking the requisite number of SMs, any desired multilevel ac voltage can be synthesized. This modular string architecture has become the basic building block for many converter topologies8–17 and is particularly appealing for use in HVDC transmission18–20.

Although attractive for dc/ac conversion, using conventional strings of cascaded SMs (or hybrid SM strings18–21) to perform dc/dc conversion has, to date, required a front-to-front (i.e. dc/ac-ac/dc) converter configuration22–25. This implies the use of two dc/ac conversion stages and an intermediate ac transformer, all of which must be rated for the full input power. As each stage processes the same input power this results in: 1) poor utilization of installed SMs, and 2) reduced overall conversion efficiency. Consequently, the cascading of two complete dc/ac stages to form a dc/dc converter structure is a relatively costly option.

Recently, it has been shown that conventional strings of series-cascaded SMs for dc/ac conversion can be adapted for single-stage bidirectional dc/dc conversion14–15. Elimination of the traditional intermediate ac link is achieved by exploiting circulating ac currents to maintain power balance of the SM capacitors. This new power balancing mechanism enables replacement of two cascaded dc/ac converters with a single dc/dc architecture (termed the DC-MMC15), thus opening the door to a new class of energy conversion well suited for HVDC applications. Other recent works exploiting a similar power balancing mechanism for dc/dc conversion have also emerged16–18.

This paper compares and contrasts the new form of single-stage dc/dc conversion introduced in14–15 with the conventional MMC based dc/ac conversion process. Key similarities and differences between each are identified and discussed. In particular it is shown that three physical modifications enable a conventional string of series-cascaded SMs for dc/ac conversion to be adapted for single-stage dc/dc conversion. Although sharing similar modular structures, performing dc/dc versus dc/ac conversion utilizes significantly different power transfer mechanisms. Operation and control requirements for each form of energy conversion are thus discussed and contrasted. A comparison of total installed SM voltage requirements for dc/ac versus dc/dc conversion is also provided. Based on presented results, it is shown that single-stage dc/dc conversion enables up to a 50% reduction in cost and operating losses when compared to converter structures utilizing two cascaded dc/ac stages, i.e. dc/ac-ac/dc conversion.

This work focuses on cascaded SMs in a single string configuration, as this is the simplest modular structure enabling both dc/ac and dc/dc multilevel energy conversion. Additional converter structures can be realized by using multiple paralleled SM strings as illustrated in Sect. 2.3.

2. Modular Multilevel Architectures

2.1 Single-String: DC/AC Conversion

The conventional single-string architecture utilizing series-cascaded SMs for dc/ac conversion is shown in Fig. 1. This structure is
flux in the core. Filter capacitors magnetizing branch) to be realized while also eliminating dc permits a large fundamental frequency ac impedance (via the coupled inductors can be used, the implementation in Fig. 2 power transfer from dc to ac terminals, while interfacing to midpoint node “a” as shown. Connecting an ac load restricts full-bridge SMs can be exploited to improve ac voltage utilization and provide bidirectional fault blocking capability. Either a passive ac load or an ac source can be connected at midpoint node “a” as shown. Connecting an ac load restricts power transfer from dc to ac terminals, while interfacing to an ac source enables bidirectional power transfer capability. The string’s ideal (lossless) output-to-input voltage conversion ratio, $G_v$, and its complement, $G'_v$, are defined as

$$G_v = \frac{V_{dc,o}}{V_{dc,i}} \quad \text{(1)}$$

$$G'_v = 1 - G_v \quad \text{(2)}$$

In (14) (15) it is shown that step-up voltage conversion (i.e. $G_v > 1$) can be achieved by exploiting full-bridge SMs in the outer arms of Fig. 2 to inject a negative average voltage. However, to be consistent with conventional dc/ac conversion requiring only half-bridge SMs, this work focuses on step-down operation (i.e. $G_v < 1$).

Observe the single-string configurations in Fig. 1(a) and Fig. 2 share a similar modular structure. This similarity stems from the fact the dc/ac structure can be adapted for single-stage dc/dc conversion requiring three key modifications:

1. Each arm of n SMs is partitioned into a pair of arms: an inner arm of m SMs and an outer arm of k SMs;
2. A path, enabled by $L_f$ in this case, is created to allow the flow of circulating ac currents.
3. A filter network, comprised of passive elements $L_f$ and $C_f$ in this case, is added to prevent circulating current from propagating to the output.

### 2.3 Multi-String Converter Architectures

The architectures in Fig. 1(a) and Fig. 2 are the simplest modular structures enabling dc/ac and single-stage dc/dc multilevel energy conversion. Moreover, they simplify analysis as only $G_v$ replaces use of $D$ in (14) (15) to avoid confusion with average duty cycle of switch-mode dc/dc converters as $D$ is not necessarily equal to the average duty cycle of DC-MMC submodules.

![Fig. 1. Conventional string of series-cascaded SMs comprising two arms for dc/ac conversion: (a) modular converter structure, (b) standard switching cell types for $j$th SM of arm “x”, where variable “x” represents either an upper or lower arm](image1)

![Fig. 2. String of series-cascaded SMs comprising four arms for single-stage dc/dc conversion](image2)
one string needs to be studied. Although useful from an analytical perspective, these architectures cause fundamental frequency ac currents to flow into the dc line, e.g. \( I_{dc} \) in Fig. 1(a) has an ac component. In practice, dc/ac converters employ multiple strings\(^{(14)(15)}\) to prevent ac currents from having to enter the dc network.

Figure 3 illustrates example multi-string dc/ac and single-stage dc/dc\(^{(14)(15)}\) converter architectures. The multi-string architectures can eliminate ac current flow in the dc network\(^{(a)}\) by imposing appropriate phase shifts between ac quantities of the different strings, e.g. the 3-phase MMC uses a phase shift between strings of 120°. For consistency with established literature the dc/ac converters are referred to as being multi-phase. As previously highlighted, MMC based dc/dc conversion has traditionally required two dc/ac stages in a front-to-front arrangement. For example, two 2-phase dc/ac converters from Fig. 3(a), along with an intermediate ac transformer, can be arranged in a dc/ac/dc configuration\(^{(12)}\).

As shown in Fig. 3(b) the 2-string and 3-string dc/dc converters are formed by interleaving multiple SM strings. In general, an arbitrary number of strings can be interleaved. The 2-string exploits a coupled inductor at each output pole (due to the even number of strings) while the 3-string\(^7\) retains the filter arrangement of the 1-string architecture. Of notable interest in Fig. 3(b) is the 1-string dc/dc converter. Here only one SM string is needed, as ac currents are allowed to circulate within the converter structure by installing two series-stacked capacitors as shown\(^{(16)}\). This architecture, a minor modification of Fig. 2, is particularly interesting as neither input nor output dc terminals are adversely impacted by significant ac ripple content at the midpoint node. This is not the case for the single-phase dc/ac structure in Fig. 3(a) as the midpoint node is directly coupled to the ac output terminal.

3. **Ideal Energy Conversion Processes**

This section compares the ideal dc/ac and single-stage dc/dc energy conversion processes. Ideal energy conversion is characterized by the following assumptions:

1. A large number of SMs are employed in each arm and effective switching frequency is sufficiently high such that individual arms synthesize near sinusoidal ac voltages (as justified by \(^{(15)(19)}\)).

2. The ubiquitous SM capacitor voltage sort and selection algorithm\(^{(26)}\) ensures voltage balancing amongst individual capacitors within each arm.

3. Voltages and currents are assumed to consist of dc and fundamental frequency ac components, in order to focus on key power transfer mechanisms.

4. Resistance terms are neglected.

5. Ideal ac output filtering is assumed for the dc/dc architecture in Fig. 2 (as justified by \(^{(15)}\)).

For ease of notation, in Fig. 2(a) and Fig. 2: 1) average input current is denoted by \( I_{dc} \), and 2) average input voltage is denoted by \( V_{dc} \). Thus, for lossless energy conversion the total average power transfer between dc and ac terminals in Fig. 1(a) and the total average power transfer between dc terminals in Fig. 2 are both denoted by \( P_{dc} = V_{dc} I_{dc} \). Capital letters denote dc quantities. With reference to Fig. 1(a) and Fig. 2, the notation \( i \) represents the fundamental frequency component of \( i \), i.e. \( i(t) = I_0 + i(t) \) where \( i(t) = I \cos(w_{dc}t + \theta) \). \( I \) is the rms phasor for \( i \), i.e. \( I = \sqrt{\text{rms}} \).

3.1 **DC/AC Conversion**

Figure 4 shows the ideal dc/ac conversion process for Fig. 1(a). Observe the arms voltages and currents are separated into their dc and ac components. Table 1 lists these arms quantities and Table 2 summarizes the corresponding average and ripple powers. In Fig. 4, an inherent symmetry about the midpoint node is evident. Both arms carry one-half of the total ac output current while synthesizing complementary ac voltages (ref. Table 1). Thus, when coupled to a passive ac load with real and reactive parts, each arm delivers one-half of the average ac power transfer and either supplies (inductive load) or absorbs (capacitive load) one-half of the load vars. In the case of an external ac source, the arms may also absorb equal amounts of average ac power. Recalling that SMs employ capacitors for energy storage, and using the results of Table 1, the average power balance constraints for each arm are:

\[
\begin{align*}
    p_{pa}^0 &= 0 = \frac{V_{dc}}{2} I_{dc} + \frac{\tilde{V}}{2} \cos(\theta) & (3) \\
    p_{na}^0 &= 0 = \frac{V_{dc}}{2} I_{dc} + \frac{\tilde{V}}{2} \cos(\theta) & (4)
\end{align*}
\]
Comparison DC/AC and DC/DC Modular Multilevel Energy Conversion (Gregory J. Kish et al.)

Table 1. Arms voltages and currents for single-string DC/AC and DC/DC architectures

| Quantities * | DC/AC Structure in Fig. 4 | DC/DC Structure in Fig. 5 |
|--------------|----------------------------|----------------------------|
| Arms \( v_{\text{in}} = \frac{V_0}{2} + \hat{V} \cos(2 \pi f t) \) | \( v_{\text{in}} = G_1 \frac{V_0}{2} + \hat{V} \cos(2 \pi f t) \) | \( v_{\text{in}} = G_1 \frac{V_0}{2} + \hat{V} \cos(2 \pi f t) + M \hat{V} \cos(\omega_1 t + \Phi) \) |
| Voltages \( v_{\text{in}} = \frac{V_0}{2} - \hat{V} \cos(2 \pi f t) \) | \( v_{\text{in}} = G_2 \frac{V_0}{2} - \hat{V} \cos(2 \pi f t) \) | \( v_{\text{in}} = G_2 \frac{V_0}{2} - \hat{V} \cos(2 \pi f t) + M \hat{V} \cos(\omega_1 t + \Phi) \) |
| Arms \( i_{\text{in}} = I_{\text{dc}} + I \cos(\omega_1 t + \Phi) \) | \( i_{\text{in}} = I_{\text{dc}} + I \cos(\omega_1 t + \Phi) \) | \( i_{\text{in}} = (1 - \frac{1}{G_1}) I_{\text{dc}} + \cos(\omega_1 t + \Phi) \) |
| Currents \( i_{\text{in}} = I_{\text{dc}} - I \cos(\omega_1 t + \Phi) \) | \( i_{\text{in}} = I_{\text{dc}} - I \cos(\omega_1 t + \Phi) \) | \( i_{\text{in}} = (1 - \frac{1}{G_1}) I_{\text{dc}} - \cos(\omega_1 t + \Phi) \) |

* *Note: values of \( V \) and \( I \) for dc/ac versus dc/dc conversion are not necessarily equal.

Table 2. Average and ripple powers for individual arms in single-string DC/AC and DC/DC architectures

| Arms Power * | DC/AC structure in Fig. 4 ** | DC/DC structure in Fig. 5 ** |
|-------------|------------------------------|------------------------------|
| Average  \( p_{\text{av}} = \frac{V_0 I_0}{2} + \frac{\hat{V} I}{2} \cos(\theta) \) | \( p_{\text{av}} = G_1 \frac{V_0 I_0}{2} + \frac{\hat{V} I}{2} \cos(\theta) \) | \( p_{\text{av}} = G_2 \frac{V_0 I_0}{2} + \frac{\hat{V} I}{2} \cos(\theta) + M \hat{V} \cos(\omega_1 t + \Phi) \) |
| 1st harmonic (i.e. \( u_{\text{in}} \))  \( p_{1m} = \frac{V_0 I_0}{2} \cos(\omega_1 t + \Phi) + I_{\text{dc}} \hat{V} \cos(\omega_1 t) \) | \( p_{1m} = G_1 \frac{V_0 I_0}{2} \cos(\omega_1 t + \Phi) + I_{\text{dc}} \hat{V} \cos(\omega_1 t) \) | \( p_{1m} = G_2 \frac{V_0 I_0}{2} \cos(\omega_1 t + \Phi) + (1 - \frac{1}{G_1}) I_{\text{dc}} \hat{V} \cos(\omega_1 t + \Phi) \) |
| 2nd harmonic (i.e. \( 2u_{\text{in}} \))  \( p_{2m} = \frac{V_0 I_0}{2} \cos(\omega_1 t + \Phi) + I_{\text{dc}} \hat{V} \cos(2 \omega_1 t + \Phi) \) | \( p_{2m} = G_1 \frac{V_0 I_0}{2} \cos(\omega_1 t + \Phi) + I_{\text{dc}} \hat{V} \cos(2 \omega_1 t + \Phi) \) | \( p_{2m} = G_2 \frac{V_0 I_0}{2} \cos(\omega_1 t + \Phi) + (1 - \frac{1}{G_1}) I_{\text{dc}} \hat{V} \cos(2 \omega_1 t + \Phi) \) |

* Powers are defined as being into (i.e. absorbed by) each arm, e.g. \( p_{\text{av}} = v_{\text{in}} i_{\text{in}} = p_{1m} + p_{2m} + p_{\text{ra}} \).

** Due to symmetry only the upper arm in Fig. 4 and positive pole inner and outer arms in Fig. 5 are analyzed.

As expected, Eqs. (3)–(4) indicate each arm transfers an average ac power to the midpoint output node equal to \( P_{\text{dc}}/2 \). A similar symmetry exists for the reactive power injected by each arm. Thus, the upper and lower arms in Fig. 4 operate identically in that they equally share the real and reactive power requirements of the ac load/source. This implies each arm operates at the same ac power factor. The arms experience equal ac ripple powers as a consequence. Due to ac load/source requirements, the fundamental frequency of the ac arm voltages and currents is constrained to conventional 50/60 Hz.

To summarize, the key power flow related characteristics of Fig. 4 for conventional dc/ac conversion are:

1. Each upper and lower arm supplies an average ac power to the midpoint output node equal to 0.5\( P_{\text{dc}} \).
2. Fundamental frequency of ac voltages and currents is fixed to conventional 50/60 Hz due to ac load/source requirements.
3. vars demand of the ac load/source is split equally between upper and lower arms.
4. Both arms have equal ac ripple power.

3.2 Single-Stage DC/DC Conversion The ideal single-stage dc/dc energy conversion process, which is described in detail in [10], is illustrated in Fig. 5. Table 1 summarizes the dc and ac voltages and currents for each arm and Table 2 lists the corresponding average and ripple powers. By chosen convention, each inner arm ac voltage is scaled by \( M_{\text{dc}} \), relative to the adjacent outer arm. The outer arm voltage \( v_{\text{ik}} \) is assigned zero phase angle reference for consistency with dc/ac converter parameters. AC voltage parameter \( M \) is adopted for ease of converter analysis as it simplifies derivation of mathematical expressions, as seen in Table 2.

The composite reactive load formed by \( L_c \) (not shown in Fig. 5) and each \( L_a \) establishes circulating ac currents that follow the exchange of average ac power between each inner arm and the adjacent outer arm. To achieve the desired ac current for a given \( V \), parameters \( M \) and \( \Phi \) are appropriately assigned. This power transfer mechanism is exploited to maintain power balance of the SM capacitors, thereby eliminating the traditional (full-rated) intermediate ac link. Interestingly, while circulating ac currents are considered largely undesirable for cascaded SM based dc/ac conversion [10], they become the key enabling power balancing mechanism by
which single-stage dc/dc conversion can be realized.

Similar to the dc/ac converter, all arms in Fig. 5 see one-half of the total ac current leaving the midpoint node. This is due to conserved symmetry about the node “01”. However, as each arm in Fig. 4 is now partitioned into an inner arm and an adjacent outer arm, their ac voltage components do not necessarily have to be equal. This implies each inner arm and the adjacent outer arm do not have to operate at the same ac power factor. Moreover, as the circulating ac currents serve only to maintain power balance of the SM capacitors, the fundamental frequency is not constrained to conventional 50/60 Hz (unlike in Fig. 4 for grid-connected applications). In general, any type of modulation can be used.

To maintain power balance of SM capacitors, each inner arm and adjacent outer arm in Fig. 5 exchange an average ac power equal to 0.5\(G\text{\textunderscore}pa\text{\textunderscore}L\text{\textunderscore}dc\). This power balance criteria is easily derived using the results of Table 2:

\[
p_{\text{ik}}^0 = 0 = G\text{\textunderscore}v\text{\textunderscore}I_m + \frac{\hat{V}}{2} \cos(\theta) \quad \cdots \quad (5)
\]

\[
p_{\text{im}}^0 = 0 = -G\text{\textunderscore}v\text{\textunderscore}I_m + \frac{\hat{V}}{2} \cos(\Phi - \theta) \quad \cdots \quad (6)
\]

\[
p_{\text{im}}^0 = 0 = -G\text{\textunderscore}v\text{\textunderscore}I_m + \frac{\hat{V}}{2} \cos(\Phi - \theta) \quad \cdots \quad (7)
\]

\[
p_{\text{ik}}^0 = 0 = G\text{\textunderscore}v\text{\textunderscore}I_m + \frac{\hat{V}}{2} \cos(\theta) \quad \cdots \quad (8)
\]

In Fig. 5, the dc components of the arm voltages and currents are functions of \(G_v\). This is fundamentally different from the dc/ac converter in Fig. 4, where all arms carry the same amount of dc current and have the same dc voltage component. Consequently, this impacts the distribution of ac ripple power between arms, i.e. all arms are not necessarily subjected to the same ripple power. This asymmetry between inner and outer arms is easily visualized by examining the appropriate rows of Table 2. Specifically, parameters \(G_v\), \(\hat{V}\), \(M\) and \(\Phi\) all influence the active and reactive power injections of each arm. Note, the results in Tables 1 and 2 reveal that \(G_v = 0.5\) is a unique operating point where arms quantities for dc/dc and dc/ac conversion have strong symmetry. This symmetry will be illustrated in Sect. 5.

To summarize, the key power flow related characteristics of Fig. 5 for single-stage dc/dc conversion are:

1. Each pair of inner and outer arms exchange an average ac power equal to 0.5\(G\text{\textunderscore}v\text{\textunderscore}P\text{\textunderscore}dc\).
2. Fundamental frequency of ac voltages and currents is a free design parameter.
3. Allocation of vars support between inner and outer arms can be assigned arbitrarily.
4. AC ripple power can be unequally distributed between arms.
5. Arms modulation is not constrained to traditional sinusoidal ac.

### 3.3 Example Power Flows Visualization

Figure 6 shows example phasor diagrams that illustrate the power transfer mechanisms employed to maintain SM capacitor power balance for the energy conversion processes in Figs. 4 and 5. Here the inner and outer arm voltages for dc/dc conversion have equal magnitudes (\(M = 1\)) and thus vars generation is split equally between arms; however, as mentioned, this does not have to be the case. The ac power flows for each conversion process are easily visualized using phasor dot products. Observe the average ac power exchanged between arms increases as \(|\Phi|\) becomes larger. The \(M\) and \(\Phi\) required for SM capacitor power balance is the outcome of ac current control, as will be shown in Sect. 4.4. Bidirectional power flow (i.e. \(I_k < 0\)) is accommodated by appropriately adjusting the ac arms voltages. For dc/dc conversion, the voltage phasors are reflected about the imaginary axis.

It is important to stress that, as shown by Fig. 6, both the dc/ac and single-stage dc/dc conversion processes benefit from natural cancellation of ac voltages along the SM string. That is, \(v_{pa} + v_m = 0\) and \(v_{ik} + v_{im} + v_{lim} + v_k = 0\). For dc/dc conversion the inner arms ac voltages are also selected such that \(v_{im} + v_{lim} = 0\). Thus, the ac modulation strategy for dc/dc conversion benefits from ensuring that a net fundamental frequency ac voltage is not impressed across either the input or output dc terminals in Fig. 2.

### 4. Operation and Control Requirements

#### 4.1 Arm Current Stresses

Figure 7 compares arm current stresses for dc/ac and single-stage dc/dc conversion, normalized to \(I_{dc}\). These curves are derived by evaluating Eqs. (3)–(4) and Eqs. (5)–(8) at rated \(P_{dc}\). For ease of comparison: 1) converter fundamental frequency vars consumption is neglected, i.e. assume small \(L_m\) in Fig. 1(a) and small \(L_{dc}\), \(L_e\) in Fig. 2, 2) \(V\) is maximized for each dc/dc operating point, and 3) half-bridge SMs are employed, i.e. arms voltages cannot be negative valued. Note, in Fig. 7(a) the peak ac current, \(I\), has a minimum value of 2 \([\text{pu}]\) for a resistive load and increases with worsening load power factor, \(PF_{\text{load}}\). The “nominal operating point” is given by a modulation index, \(\frac{V}{(V_{dc}/2)}\), slightly less than 1 \([\text{pu}]\) to avoid converter over-modulation.

Figure 7 reveals arm current stresses for single-stage dc/dc conversion are comparable to those for conventional dc/ac conversion (near nominal operating point) when operating in the vicinity of \(G_v = 0.5\). Stresses increase substantially for smaller \(G_v\). However, inner arm current stresses are reduced as \(G_v\) increases from 0.5 to 1. Figure 7(b) clearly illustrates the dc/dc architecture in Fig. 2 is best suited for dc voltage ratios ranging from unity to somewhat less than 0.5.

In Fig. 7 the plots are drawn assuming negligible converter fundamental frequency vars consumption. Of course, accounting for non-zero \(L_{dc}\) and \(L_e\) will cause \(I\) in both diagrams...
to increase slightly. In Fig. 7(b), which is drawn for $M = 1$ (arms have same ac voltage magnitude), an increase in $\bar{I}$ implies a larger circulating ac current is needed to achieve rated $P_{dc}$. To counter this increase in $\bar{I}$, thereby reducing losses and increasing power transfer capability, the ac voltage ratio $M$ can be adjusted to improve the arms power factor as needed. This strategy is elaborated on in Sect. 4.2.

4.2 AC Modulation Strategy Table 3 outlines a proposed ac modulation strategy for single-stage dc/dc conversion to maximize conversion efficiency, based on the discussion in Sect. 4.1. This strategy is based on the premise of minimizing circulating ac currents for a given operating point. For values of $G_v$ around 0.5 (quantified by $G_v = 0.5 \pm \alpha$), all arms should operate at the same ac power factor since $G_v \approx G_v' \approx 0.5$. However, for larger (or smaller) values of $G_v$, the outer arms (or inner arms) should operate at unity power factor. This approach maximizes the available ac voltage, such that circulating ac currents needed for a given $P_{dc}$ are minimized. For large $G_v$, the maximum outer arm ac voltage is limited to $V/(V_{dc}/2)=G_v'$ where $G_v' << G_v$. In this case, the outer arms should operate at unity power factor to minimize the required $\bar{I}$. To achieve this objective the inner arms ac voltage must be larger than the outer arms, requiring $M > 1$.

The ac modulation strategy in Table 3 revolves around the principle of maximizing the ac arms voltages, subject to available voltage headroom. This strategy was motivated by the conventional ac modulation approach for the dc/ac converter, where ac arms voltages are intentionally maximized. This can be seen in Table 1 where complementary ac voltages $\tilde{v}_{pa}$ and $\tilde{v}_{na}$ have a maximum amplitude of $\tilde{V} = V_{dc}/2$ (for half-bridge SMs).

4.3 Total Installed SM Voltage Requirements Total installed SM voltage requirements for dc/dc conversion corresponding to the strategy in Table 3 are given in Fig. 8. Note that 2 [pu] installed SM voltage is inherently needed for the dc/ac converter, as the midpoint node voltage in Fig. 1(a) swings (ideally) from $+V_{dc}/2$ to $-V_{dc}/2$. In comparison, for the single-stage dc/dc converter the total installed SM voltage can be reduced below the conventional 2 [pu] threshold. This implies the ability to reduce the total number of installed semiconductor switches for single-stage dc/dc conversion. Although only half-bridge SMs are used in this analysis, it should be mentioned that full-bridge SMs can also be exploited in the outer arms to increase available ac voltage headroom (15). Such a strategy can prove advantageous for $G_v > 0.5$, particularly for values of $G_v$ approaching unity.

4.4 Control Requirements Figure 9 compares control schemes for the dc/ac converter and single-stage dc/dc converter. For the dc/ac converter, direct modulation is employed for fundamental frequency quantities while a
supplemental current control loop suppresses undesirable second harmonic circulating ac currents. Balancing of SM capacitor voltages in Fig. 9(a) is achieved via the ubiquitous SM capacitor voltage sort and selection algorithm (24).

The control scheme for single-stage dc/dc conversion, although sharing a similar control structure to Fig. 9(a), utilizes significantly different power transfer mechanisms. To balance SM capacitor voltages the sort and selection algorithm is alone insufficient (27); some form of regulation of average ac power exchange between arms is required. This is achieved via closed loop control of fundamental frequency circulating ac currents, which acts on the difference in SM capacitor voltages between adjacent arms as shown in Fig. 9(b). Scalar $k_q \in [0,1]$ allows arbitrary splitting of vars generation between arms, by appropriately allocating the common mode voltages produced by the proportional-resonant (PR) compensators. Key values include $k_q = 0$ (inner arms supply all vars), $k_q = 0.5$ (split vars equally between arms for case of $k = m$) and $k_q = 1$ (outer arms supply all vars). These correspond to $M > 1$, $M = 1$ and $M < 1$, respectively. The average duty cycle of each arm is fixed based on the desired ideal dc voltage ratio $G_v$, which is sufficient for operation at a constant $G_v$.

AC voltage parameter $M$, which as discussed earlier was adopted for ease of converter analysis, has been replaced by $k_q$ in Fig. 9(b) for practical control implementation. For the case of $k_q = 0.5$ and assuming a small net circuit inductance, the synthesized arms voltages have a fundamental frequency magnitude approximately equal to $\hat{V}$, e.g. $|V_{1m}| = |V_{im}| \approx \hat{V}$. This is visually confirmed in Fig. 6 when considering values of $|\Phi|$ approaching $180^\circ$ and recalling the use of differential ac voltages $\hat{V}_1 \cos(w_m t)$ and $\hat{V}_2 \cos(w_m t + 180^\circ)$ as shown in Fig. 9(b).

It should be highlighted that Fig. 9(b) is a generalized formulation of the SM capacitor voltage control first proposed in (15). Specifically, the control scheme in (15) corresponds to Fig. 9(b) where: 1) $k_q = 0$, 2) reference signals $v_{1m}^*, v_{2m}^*$ are generated solely by the PR compensators, 3) control feedback utilizes only outer arms current measurements, and 4) it is assumed $k = m$. It is also important to note that for the dc/ac converter, the presence of second harmonic circulating ac currents are undesirable and thus typically suppressed to reduce the rms value of the arms currents as well as reduce capacitor voltage ripple (24) (25). Utilizing fundamental frequency circulating ac currents as a secondary control means for equalization of SM capacitor voltages during transients is also possible (26). However, control of fundamental frequency circulating ac currents is the primary mechanism by which SM capacitor voltages are regulated to their nominal values for single-stage dc/dc conversion (15) (27).
Fig. 10. Simulation results demonstrating symmetry between waveforms for dc/ac and single-stage dc/dc conversion ($P_{dc} = 7$ MW): (a) dc/ac conversion, with $n = 8$ and resistive load, (b) single-stage dc/dc conversion, with $k = m = 4$, $G_r = 0.5$ and resistive load.

Table 4. PLECS simulation data

| General Parameters               | Value |
|---------------------------------|-------|
| Nominal DC input voltage, $V_{in,dc}$ | 17.6 kV |
| Average power transfer, $P_{dc}$ | 7 MW |
| SM capacitor, $C_{sm}$          | 14 μF |
| Nominal SM voltage, $V_{sm,dc}$ | 2.2 kV |
| Fundamental frequency, $f_{ac}$ | 377 rad/s |
| Carrier frequency, $f_c$        | 4.4 kHz |
| DC/AC Converter Parameters     |       |
| Arm choke, $L_a$                | 1 mH |
| SMs per arm, $n$                |       |
| AC voltage, $V$                 | $8.6kV_{ac}$ |
| DC/DC Converter Parameters     |       |
| Value                           |       |
| $G_r = 0.5$                     | $G_i = 0.75$ |
| SMs per arm, $k/m$              | 4/4   |
| AC voltage, $V$                 | $4.3kV_{ac}$ |
| Vars allocation, $k_a$          | 0.5   |
| Arm choke, $L_a$                | 0.3 mH |
| Midpoint string inductor, $L_i$ | 0.5 mH |
| Filter magnetizing inductance, $L_m$ | 900 mH |
| Filter capacitor, $C_f$         | 15 μF |

5. Case Study Simulations

Simulation results for switched models of Fig. 1(a) and Fig. 2 implemented in PLECS are presented. The control schemes in Fig. 9 are adopted. For each scenario, $V_{dc} = \pm 8.8$ kV and $P_{dc} = 7$ MW. A total of $2n = 16$ half-bridge SMs are used for the dc/ac converter. A total of $2(k+m) = 16$ half-bridge SMs are used for the single-stage dc/dc converter to achieve $G_r = 0.5$. To achieve $G_r = 0.75$, a total of $2(k+m) = 12$ half-bridge SMs are used. The chosen ac modulating frequency is 60 Hz. Simulation parameters are given in Table 4.

5.1 DC/AC and DC/DC Conversion Symmetry

The dc/ac conversion process is shown in Fig. 10(a). Here a resistive load draws 7 MW from the midpoint node at unity power factor. Observe the upper and lower arms waveforms are complementary as the ac load requirements are split equally between arms. Fig. 10(b) shows the single-stage dc/dc conversion process for $G_r = 0.5$ (8.8 kV/17.6 kV ratio). For $P_{dc} = 7$ MW, each pair of inner and outer arms exchange 1.75 MW of average ac power. $k_a$ is set to 0.5 such that all arms have equal ac voltage magnitudes as per Table 3.

5.2 DC/Conversion with $G_r > 0.5$

As anticipated, arms waveforms in Fig. 10(a) and Fig. 10(b) exhibit strong symmetry. This symmetry is a result of the unique dc/dc operating point $G_r = 0.5$, which coincides with the dc/ac converter where all arms have equal average voltages and carry equal amounts of dc current. It is important to stress Fig. 10 demonstrates the same power transfer, $P_{dc} = 7$ MW, can be achieved for the dc/ac converter and single-stage dc/dc converter (at $G_r = 0.5$), while: 1) utilizing the same capacitive energy storage, and 2) exhibiting equal arm current stresses and capacitor voltage ripple variation. This equivalence is verified by evaluating entries in Table 1 and Table 2 at $G_r = 0.5$. Table 5 summarizes the results of such a comparison for the upper half of each converter structure. Observe all arms have equal peak current stresses and $|p_{dc}| = |p_{ac1}| + |p_{ac2}|$. The impact of this outcome will be discussed in Sect. 5.3.

Table 5. Symmetry of arms quantities for ideal DC/AC conversion and DC/DC conversion at $G_r = 0.5$

| Arms | DC/AC Structure in Fig. 4 | DC/DC Structure in Fig. 5 |
|------|---------------------------|---------------------------|
| Voltages | $v_{in,ac} = \frac{V_{dc}}{2} [1 + \cos(w_{ac}t)]$ | $v_{in,dc} = \frac{V_{dc}}{2} [1 + \cos(w_{dc}t)]$ |
| Currents | $i_{a1} = I_{dc} [1 - 2 \cos(w_{ac}t)]$ | $i_{in,dc} = I_{dc} [1 - 2 \cos(w_{dc}t)]$ |
| | $i_{a2} = I_{dc} [1 - 2 \cos(w_{ac}t)]$ | $i_{in,dc} = I_{dc} [1 - 2 \cos(w_{dc}t)]$ |
| | $i_{p,dc} = \frac{P_{dc}}{V_{dc} [1 - \cos(2w_{ac}t)]}$ | $i_{p,dc} = \frac{P_{dc}}{V_{dc} [1 - \cos(2w_{dc}t)]}$ |
| | $i_{p,ac} = \frac{P_{dc}}{V_{dc} [1 - \cos(2w_{ac}t)]}$ | $i_{p,ac} = \frac{P_{dc}}{V_{dc} [1 - \cos(2w_{dc}t)]}$ |

For ease of comparison, neglecting fundamental frequency vars consumption of $L_a$ and $L_f$ enables use of parameter values $\bar{V} = V_{dc}/2$ (for dc/ac), $\bar{V} = 0.5 V_{dc}/2$ (for dc/dc), $M = 1$, $\Phi = \theta = 180^\circ$.

As anticipated, arms waveforms in Fig. 10(a) and Fig. 10(b) exhibit strong symmetry. This symmetry is a result of the unique dc/dc operating point $G_r = 0.5$, which coincides with the dc/ac converter where all arms have equal average voltages and carry equal amounts of dc current. It is important to stress Fig. 10 demonstrates the same power transfer, $P_{dc} = 7$ MW, can be achieved for the dc/ac converter and single-stage dc/dc converter (at $G_r = 0.5$), while: 1) utilizing the same capacitive energy storage, and 2) exhibiting equal arm current stresses and capacitor voltage ripple variation. This equivalence is verified by evaluating entries in Table 1 and Table 2 at $G_r = 0.5$. Table 5 summarizes the results of such a comparison for the upper half of each converter structure. Observe all arms have equal peak current stresses and $|p_{dc}| = |p_{ac1}| + |p_{ac2}|$. The impact of this outcome will be discussed in Sect. 5.3.

5.2 DC/Conversion with $G_r > 0.5$

To illustrate a dc/dc operating point with asymmetry between inner and outer arms, single-stage dc/dc conversion is shown in Fig. 11 for $G_r = 0.75$ (13.2 kV / 17.6 kV ratio). Each pair of inner and outer arms now exchange only 0.875 MW of average ac power for the same $P_{dc} = 7$ MW. $k_q$ is set to 0 to operate the outer arms at unity power factor as per Table 3. The impact of this outcome will be discussed in Sect. 5.3.
The average current carried by the inner and outer arms is now unequal, with the inner arms having reduced dc current. All arms still carry the same amount of fundamental frequency ac current. These results reflect the power flow analysis in Fig. 5 for $G_0$ larger than 0.5. Observe fewer total SMs can be used for $G_0 = 0.75$ $(k + m = 6)$ relative to $G_0 = 0.5$ $(k + m = 8)$, as anticipated from Table 8. Observe also the SM capacitor voltage ripple between inner and outer arms is now unequal, which stems from the analysis in Table 2.

**5.3 Single-Stage and Two-Stage DC/DC Conversion**

Conventional MMC based dc/dc conversion has, to date, required a front-to-front (i.e. dc/ac-ac/dc) configuration. For example, two 2-phase dc/ac converters from Fig. 3(a), along with an intermediate ac transformer, can be arranged in a dc/ac-ac/dc configuration (13). This two-stage dc/dc conversion process ultimately suffers from poor SM utilization, as 100% of the power throughput must be processed by both dc/ac stages and the ac transformer. Conversion efficiency is also hindered.

The comparison at $G_0 = 0.5$ in Sect. 5.1 reveals that single-stage dc/dc conversion enables a 50% reduction in both converter cost and conversion losses relative to state-of-the-art MMC based two-stage dc/dc conversion. This outcome is due to the fact that only a single dc/dc structure is needed in Fig. 10 to process rated $P_{dc}$, whereas two dc/ac structures from Fig. 10 are required in a cascaded dc/ac-ac/dc configuration. That is, the total number of switches and installed capacitive energy storage (and thus converter cost) is reduced by one-half, as so are the conversion losses. Of course, these savings do not take into account a comparison of the magnetics requirements between topologies — output filtering for single-stage dc/dc conversion and intermediate ac transformer for two-stage dc/dc conversion. A comparison at $G_0 = 0.5$ based on rms winding ratings (using analysis in (13)) indicates a coupled inductor solution as shown in Fig. 2 has a MVA rating of $S = 0.354P_{dc}$. In contrast, an intermediate ac transformer must be rated for full power with $S = P_{dc}$. A significant reduction in magnetics rating is therefore also realized.

The cost and losses comparison described above is for a voltage ratio of $G_0 = 0.5$. The strong symmetry in dc/ac and single-stage dc/dc waveforms at $G_0 = 0.5$ enabled relative ease in performing this analysis. However, carrying out a similar comparative analysis for $G_0 \neq 0.5$ is not as straightforward. This is because operational requirements of single-stage dc/dc conversion vary as a function of $G_0$, as detailed in Sects. 3.2 and 4. Furthermore, various converter design and operational considerations not explored in this work may be utilized. These include: 1) increasing the magnitude of ac arms voltages (using full-bridge SMs) to further reduce ac current stresses and SM capacitor voltage ripples, 2) exploiting higher modulating frequencies, and 3) utilizing unequal SM capacitances between inner and outer arms. The last strategy facilitates optimization of arms energy storage when a reduced number of SMs are employed for $G_0 > 0.5$.

A comprehensive study taking into account the above considerations and trade-offs is outside the scope of this paper. The key message here is that single-stage dc/dc conversion can enable substantial cost and efficiency savings relative to conventional MMC based two-stage dc/dc conversion.

### 6. Conclusion

A comparison is carried out between the established dc/ac and recently introduced single-stage dc/dc modular multilevel energy conversion processes. It is shown that three physical modifications allow the well known single-phase dc/ac MMC to be adapted for single-stage dc/dc conversion. The power transfer mechanisms employed for each energy conversion process, however, are significantly different. In the dc/ac converter, circulating ac currents are typically suppressed, or, even possibly utilized as a secondary control means for equalization of SM capacitor voltages during transients. In contrast, ac currents are intentionally circulated as the primary means to enable balancing of SM capacitor voltages for the single-stage dc/dc converter.

The dc voltage ratio $G_0 = 0.5$ is a unique operating point where strong symmetry exists between dc/ac and dc arms waveforms. Arm current stresses for conventional dc/ac and single-stage dc/dc conversion are comparable when operating in the vicinity of $G_0 = 0.5$. Current stresses are reduced as $G_0$ increases, demonstrating the dc/ac architecture is best suited for voltage conversion ratios ranging from 1 to 0.5. Conversion ratios below 0.5 may still prove advantageous when comparing the single-stage dc/dc structure with a conventional MMC based two-stage dc/dc converter, i.e. dc/ac/dc conversion, as the single-stage dc/dc structure utilizes fewer total SMs and incurs lower operating losses at $G_0 = 0.5$.

A comparison of the controls needed for dc/ac and single-stage dc/dc conversion reveal similar structures, although they utilize significantly different power transfer mechanisms. A capacitor voltage regulation scheme for dc/dc conversion is proposed whereby var allocation between converter arms can be assigned arbitrarily in order to maximize conversion efficiency. This scheme adopts closed-loop current control to ensure SM capacitor voltages are regulated to their nominal values in light of dc power transfer variations.

It is shown that single-stage dc/dc conversion can be achieved using less total installed SM voltage relative to conventional dc/ac conversion. In comparison to conventional MMC based two-stage dc/dc conversion, single-stage dc/dc conversion enables up to a 50% reduction in converter cost and operating losses. This signifies that the recently intro-
duced DC-MMC offers significant promise as a key enabling technology for future HVDC based grids.

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