Voltron: Understanding and Exploiting the Voltage–Latency–Reliability Trade-Offs in Modern DRAM Chips to Improve Energy Efficiency

Kevin K. Chang\textsuperscript{1,2} Abdullah Giray Yağlıkçı\textsuperscript{2} Saugata Ghose\textsuperscript{2} Aditya Agrawal\textsuperscript{3} Niladrish Chatterjee\textsuperscript{3} Abhijith Kashyap\textsuperscript{4,2} Donghyuk Lee\textsuperscript{3} Mike O’Connor\textsuperscript{3,5} Hasan Hassan\textsuperscript{6} Onur Mutlu\textsuperscript{6}

\textsuperscript{1}Facebook \hspace{1cm} \textsuperscript{2}Carnegie Mellon University \hspace{1cm} \textsuperscript{3}NVIDIA Research \hspace{1cm} \textsuperscript{4}NVIDIA \hspace{1cm} \textsuperscript{5}The University of Texas at Austin \hspace{1cm} \textsuperscript{6}ETH Zürich

This paper summarizes our work on experimental characterization and analysis of reduced-voltage operation in modern DRAM chips, which was published in SIGMETRICS 2017 [29], and examines the work’s significance and future potential. This work is motivated to reduce the energy consumption of DRAM, which is a critical concern in modern computing systems. Improvements in manufacturing process technology have allowed DRAM vendors to lower the DRAM supply voltage conservatively, which reduces some of the DRAM energy consumption. We would like to reduce the DRAM supply voltage more aggressively, to further reduce energy. Aggressive supply voltage reduction requires a thorough understanding of the effect voltage scaling has on DRAM access latency and DRAM reliability.

We take a comprehensive approach to understanding and exploiting the latency and reliability characteristics of modern DRAM when the supply voltage is lowered below the nominal voltage level specified by DRAM standards. Using an open-source FPGA-based testing platform based on SofMC [54], we perform an experimental study of 124 real DDR3L (low-voltage) DRAM chips manufactured recently by three major DRAM vendors. We find that reducing the supply voltage below a certain point introduces bit errors in the data, and we comprehensively characterize the behavior of these errors. We discover that these errors can be avoided by increasing the latency of three major DRAM operations (activation, restoration, and precharge). We perform detailed DRAM circuit simulations to validate and explain our experimental findings. We also characterize the various relationships between reduced supply voltage and error locations, stored data patterns, DRAM temperature, and data retention.

Based on our observations, we propose a new DRAM energy reduction mechanism, called Voltron. The key idea of Voltron is to use a performance model to determine by how much we can reduce the supply voltage without introducing errors and without exceeding a user-specified threshold for performance loss. Our evaluations show that Voltron reduces the average DRAM and system energy consumption by 10.5% and 7.3%, respectively, while limiting the average system performance loss to only 1.8%, for a variety of memory-intensive quad-core workloads. We also show that Voltron significantly outperforms prior dynamic voltage and frequency scaling mechanisms for DRAM. We believe our experimental characterization and findings can pave the way for new mechanisms that exploit DRAM voltage to improve power, performance, energy, and reliability.

1. Motivation

In a wide range of modern computing systems, spanning from warehouse-scale data centers to mobile platforms, energy consumption is a first-order concern [39, 56, 65, 105, 107]. In these systems, the energy consumed by the DRAM-based main memory system constitutes a significant fraction of the total energy. For example, experimental studies of production systems have shown that DRAM consumes 40% of the total energy in servers [56, 140] and 40% of the total power in graphics cards [115].

Improvements in manufacturing process technology have allowed DRAM vendors to lower the DRAM supply voltage conservatively, which reduces some of the DRAM energy consumption [59, 60, 61]. In this work, we would like to reduce DRAM energy by further reducing DRAM supply voltage. Vendors choose a conservatively high supply voltage, to provide a guardband that allows DRAM chips with worst-case process variation to operate without errors under the worst-case operating conditions [36]. The exact amount of supply voltage guardband varies across chips, and lowering the voltage below the guardband can result in erroneous or even undefined behavior [29]. Therefore, we need to understand how DRAM chips behave during reduced-voltage operation. To our knowledge, no previously published work examines the effect of using a wide range of different supply voltage values on the reliability, latency, and retention characteristics of DRAM chips.

Our goal in our SIGMETRICS 2017 paper [29] is to (i) characterize and understand the relationship between supply voltage reduction and various characteristics of DRAM, including DRAM reliability, latency, and data retention; and (ii) use the insights derived from this characterization and understanding to design a new mechanism that can aggressively lower the supply voltage to reduce DRAM energy consumption while keeping performance loss under a bound.
To this end, we build an FPGA-based testing platform based on SoftMC [54] that allows us to tune the DRAM supply voltage and change DRAM timing parameters (i.e., the amount of time the memory controller waits for a DRAM operation to complete). We perform an experimental study on 124 real 4Gb DDR3L (low-voltage) DRAM chips manufactured recently (between 2014 and 2016) by three major DRAM vendors. Our extensive experimental characterization yields four major observations on how DRAM latency, reliability, and data retention are affected by reduced voltage.

Based on our experimental observations, we propose a new low-cost DRAM energy reduction mechanism called Voltron. The key idea of Voltron is to use a performance model to determine by how much we can reduce the DRAM array voltage at runtime without introducing errors and without exceeding a user-specified threshold for acceptable performance loss.

2. Characterization of DRAM Under Reduced Supply Voltage

In this section, we briefly summarize our four major observations from our detailed experimental characterization of 31 commodity DRAM modules, also called DIMMs, from three vendors, when the DIMMs operate under reduced supply voltage (i.e., below the nominal voltage level of 1.35V). Each DIMM comprises 4 DDR3L DRAM chips, totaling to 124 chips for 31 DIMMs. Each chip has a 4Gb density. Thus, each of our DIMMs has a 2GB capacity. Table 1 describes the relevant information about the tested DIMMs. For a complete discussion on all of our observations and experimental methodology, we refer the reader to our SIGMETRICS 2017 paper [29].

| Vendor | Total Number of Chips | Timing (ns) | Assembly Year |
|--------|-----------------------|-------------|---------------|
| A (10 DIMMs) | 40 | 13.75/13.75/35 | 2015-16 |
| B (12 DIMMs) | 48 | 13.75/13.75/35 | 2014-15 |
| C (9 DIMMs) | 36 | 13.75/13.75/35 | 2015 |

Table 1: Main properties of the tested DIMMs. Reproduced from [29].

2.1. DRAM Reliability as Voltage Decreases

We first study the reliability of DRAM chips under low voltage, which was not studied by prior works on DRAM voltage scaling (e.g., [36]; see Section 4 for a detailed discussion of these works). Figure 1 shows the fraction of cache lines that experience at least 1 bit of error (i.e., 1 bit flip) in each DIMM (represented by each curve), categorized based on vendor.

We observe that we can reliably access data when DRAM supply voltage is lowered below the nominal voltage level, until a certain voltage value, $V_{\text{min}}$, which is the minimum voltage level at which no bit errors occur. Furthermore, we find that we can reduce the voltage below $V_{\text{min}}$ to attain further energy savings, but that errors start occurring in some of the data read from memory. However, not all cache lines exhibit errors for all supply voltage values below $V_{\text{min}}$. Instead, the number of erroneous cache lines for each DIMM increases as we reduce the voltage further below $V_{\text{min}}$. Specifically, Vendor A’s DIMMs experience a near-exponential increase in errors as the supply voltage reduces below $V_{\text{min}}$. This is mainly due to the manufacturing process [90] and architectural variation [87], which introduces strength and size variation across the different DRAM cells within a chip.

We make two major conclusions: (i) the variation of errors due to reduced-voltage operation across vendors is very significant; and (ii) in most cases, there is a significant margin in the voltage specification, i.e., $V_{\text{min}}$ for each chip is significantly lower than the manufacturer-specified supply voltage value.

2.2. Longer Access Latency Mitigates Voltage-Induced Errors

We observe that while reducing the voltage below $V_{\text{min}}$ introduces bit errors in the data, we can prevent these errors if we increase the timing parameters of three major DRAM operations, i.e., activation, restoration, and precharge [27, 29, 55, 87, 90]. When the supply voltage is reduced, the DRAM cell capacitor charge takes a longer time to change, thereby causing these DRAM operations to become slower to complete. Errors are introduced into the data when the memory controller does not account for this slowdown in the DRAM operations. We find that if the memory controller allocates extra time for these operations to finish when the supply voltage is below $V_{\text{min}}$, errors no longer occur. We validate, analyze, and explain this behavior using SPICE simulation of a detailed circuit-level model, which we have openly released online [124]. Sections 4.1 and 4.2 of our SIGMETRICS 2017 paper [29] provide our extensive circuit-level analyses, validated using data from real DRAM chips.

2.3. Spatial Locality of Errors

While reducing the supply voltage induces errors when the DRAM latency is not long enough, we also show that not
all DRAM locations experience errors at all supply voltage levels. To understand the locality of the errors induced by a low supply voltage, we show the probability of each DRAM row in a DIMM experiencing at least one bit of error across all experiments.

Figure 2 shows the probability of each row experiencing at least a one-bit error due to reduced voltage in the two representative DIMMs. For each DIMM, we choose the supply voltage at which errors start appearing (i.e., the voltage level one step below \( V_{\text{min}} \)), and we do not increase the DRAM access latency (i.e., keep it at 10ns for both tRCD and tRP, which are the activation and precharge timing parameters, respectively). The x-axis and y-axis indicate the bank number and row number (in thousands), respectively. Our tested DIMMs are divided into eight banks, and each bank consists of 32K rows of cells. Additional results showing the error locations at different voltage levels are in our SIGMETRICS 2017 paper [29].

2.4. Impact on Refresh Rate

Commodity DRAM chips guarantee that all cells can safely retain data for 64ms, after which the cells are refreshed to replenish charge that leaks out of the capacitors [26, 96, 97]. We observe that the effect of the supply voltage on retention times is not statistically significant. Even when we reduce the supply voltage from 1.35V to 1.15V (i.e., a 15% reduction), the rate at which charge leaks from the capacitors is so slow that no data is lost during the 64ms refresh interval at both 20°C and 70°C. Therefore, we conclude that using a reduced supply voltage does not require any changes to the standard refresh interval at 20°C and 70°C. Detailed results are in Section 4.6 of our SIGMETRICS 2017 paper [29].

2.5. Other Experimental Observations

We refer the reader to our SIGMETRICS 2017 paper [29] for more details on the other two key observations. First, we find that the most commonly-used ECC scheme, SECDED [66, 99, 132], is unlikely to alleviate errors induced by a low supply voltage. This is because lowering voltage increases the fraction of data that contains more than two bits of errors, exceeding the one-bit correction capability of SECDED (see Section 4.4 of our SIGMETRICS 2017 paper [29]). Second, temperature affects the reliable access latency at low supply voltage levels and the effect is very vendor-dependent (see Section 4.5 of our SIGMETRICS 2017 paper [29]). Out of the three major vendors whose DIMMs we evaluate, DIMMs from two vendors require longer activation and precharge latencies to operate reliably at high temperature under low supply voltage. The main reason is that DRAM chips become slower at higher temperature [24, 87, 90].

3. Exploiting Reduced-Voltage Behavior

Based on the extensive understanding we have developed on reduced-voltage operation of real DRAM chips, we propose a new mechanism called Voltron, which reduces DRAM energy without sacrificing memory throughput. Voltron exploits the fundamental observation that reducing the supply voltage to DRAM requires increasing the latency of the three DRAM operations in order to prevent errors. Using this observation, the key idea of Voltron is to use a performance model to determine by how much to reduce the DRAM supply voltage, without introducing errors and without exceeding a user-specified threshold for performance loss. Voltron consists of two main components: (i) array voltage scaling and (ii) performance-aware voltage control.

3.1. Components of Voltron

Array Voltage Scaling. Unlike prior works, Voltron does not reduce the voltage of the peripheral circuitry, which is responsible for transferring commands and data between the memory controller and the DRAM chip. If Voltron were to reduce the voltage of the peripheral circuitry, we would

---

2We believe this observation is due to both process and architectural variation across different regions in the DRAM chip.
have to also reduce the operating frequency of DRAM. A reduction in the operating frequency reduces the memory data throughput, which can significantly degrade the performance of applications that require high memory bandwidth. Instead, Voltron reduces the voltage supplied to only the DRAM array without changing the voltage supplied to the peripheral circuitry, thereby allowing the DRAM channel to maintain a high frequency while reducing the power consumption of the DRAM array. To prevent errors from occurring during reduced-voltage operation, Voltron increases the latency of the three DRAM operations (activation, restoration, and precharge) based our observation in Section 2.2.

Performance-Aware Voltage Control. Array voltage scaling provides system users with the ability to decrease DRAM array voltage ($V_{array}$) to reduce DRAM power. Employing a lower $V_{array}$ provides greater power savings, but at the cost of longer DRAM access latency, which leads to larger performance degradation. This trade-off varies widely across different applications, as each application has a different tolerance to the increased memory latency. This raises the question of how to pick a “suitable” array voltage level for different applications as a system user or designer. For our evaluations, we say that an array voltage level is suitable if it does not degrade system performance by more than a user-specified threshold. Our goal is to provide a simple technique that can automatically select a suitable $V_{array}$ value for different applications. To this end, we propose performance-aware voltage control, a power–performance management policy that selects a minimum $V_{array}$ which satisfies a desired performance constraint. The key observation is that an application’s performance loss (due to increased memory latency) scales linearly with the application’s memory demand (e.g., memory intensity). Based on this empirical observation we make, we build a performance loss predictor that leverages a linear model to predict an application’s performance loss based on its characteristics and the effect of different voltage level choices at runtime. Using the performance loss predictor, Voltron finds a value of $V_{array}$ that can keep the predicted performance within the user-specified target at runtime. We refer the reader to Section 5.2 of our SIGMETRICS 2017 paper [29] for more detail and for an evaluation of the performance model alone.

3.2. Evaluation

We evaluate the system-level energy and performance impact of Voltron using Ramulator [75, 124], integrated with McPAT [93] and DRAMPower [25] for modeling the energy consumption of both the processor and DRAM. Our workloads consist of 27 benchmarks from SPEC CPU2006 [134] and YCSB [34]. We evaluate Voltron with a target performance loss of 5%. Voltron executes the performance-aware voltage control mechanism once every four million cycles. We refer the reader to Section 6.1 of our SIGMETRICS 2017 paper [29] for more detail on the system configuration and workloads. We qualitatively and quantitatively compare Voltron to MemDVFS, a dynamic DRAM frequency and voltage scaling mechanism proposed by prior work [36].

Figure 3 shows the system energy savings and the system performance (i.e., weighted speedup [43, 131]) loss due to MemDVFS and Voltron, compared to a baseline DRAM with a supply voltage of 1.35V. The graph uses box plots to show the distribution among all workloads that are categorized as either non-memory-intensive or memory-intensive. The memory intensity is determined based on the commonly-used metric MPKI (last-level cache misses per kilo-instruction). We categorize an application as memory intensive when its MPKI is greater than or equal to 15. We make two observations.

First, Voltron is effective and saves more energy than MemDVFS. MemDVFS has almost zero effect on memory-intensive workloads. This is because MemDVFS avoids scaling DRAM frequency (and hence voltage) when an application’s memory bandwidth utilization is above a fixed threshold. Reducing the frequency can result in a large performance loss since the memory-intensive workloads require high memory throughput. As memory-intensive applications have high memory bandwidth consumption that easily exceeds the fixed threshold used by MemDVFS, MemDVFS cannot perform frequency and voltage scaling during most of the execution time. In contrast, Voltron reduces system energy by 7.0% on average for memory-intensive workloads. Thus, we demonstrate that Voltron is an effective mechanism that improves system energy efficiency not only on non-memory-intensive applications, but also (especially) on memory-intensive workloads where prior work was unable to do so.

Second, as shown in Figure 3 (right), Voltron consistently selects a $V_{array}$ value that satisfies the performance loss bound of 5% across all workloads. Voltron incurs an average (maximum) performance loss of 2.5% (4.4%) and 2.9% (4.1%) for non-memory-intensive and memory-intensive workloads, respectively. This demonstrates that our performance model enables Voltron to select a low voltage value that saves energy while bounding performance loss based on the user’s requirement.

Our SIGMETRICS 2017 paper contains extensive performance and energy analysis of the Voltron mechanism in Sections 6.2 to 6.8 [29]. In particular, we show that if we exploit spatial locality of errors (Section 2.3), we can improve the performance benefits of Voltron, reducing the average per-
formance loss for memory-intensive workloads to 1.8% (see Section 6.5 of our SIGMETRICS 2017 paper [29]). We refer the reader to these sections for a detailed evaluation of Voltron.

4. Related Work

To our knowledge, this is the first work to (i) experimentally characterize the reliability and performance of modern low-power DRAM chips under different supply voltages, and (ii) introduce a new mechanism that reduces DRAM energy while retaining high memory data throughput by adjusting the DRAM array voltage. We briefly discuss other prior work in DRAM energy reduction.

**DRAM Frequency and Voltage Scaling.** Many prior works propose to reduce DRAM energy by adjusting the memory channel frequency and/or the DRAM supply voltage dynamically. Deng et al. [39] propose MemScale, which scales the frequency of DRAM at runtime based on a performance predictor of an in-order processor. Other work focuses on developing management policies to improve system energy efficiency by coordinating DRAM DFS with DVFS on the CPU [12, 37, 38] or GPU [115]. In addition to frequency scaling, David et al. [36] propose to scale the DRAM supply voltage along with the memory channel frequency, based on the memory bandwidth utilization of applications.

In contrast to all these works, our work focuses on a detailed experimental characterization of real DRAM chips as the supply voltage varies. Our study provides fundamental observations for potential mechanisms that can mitigate DRAM and system energy consumption. Furthermore, frequency scaling hurts memory throughput, and thus significantly degrades the system performance of especially memory-intensive workloads (see Section 2.4 in our SIGMETRICS 2017 paper [29] for our quantitative analysis). We demonstrate the importance and benefits of exploiting our experimental observations by proposing Voltron, one new example mechanism that uses our observations to reduce DRAM and system energy without sacrificing memory throughput.

**Low-Power Modes for DRAM.** Modern DRAM chips support various low-power standby modes. Entering and exiting these modes incurs some amount of latency, which delays memory requests that must be serviced. To increase the opportunities to exploit these low-power modes, several prior works propose mechanisms that increase periods of memory idleness through data placement (e.g., [44, 83]) and memory traffic reshaping (e.g., [2, 9, 14, 40, 100]). Exploiting low-power modes is orthogonal to our work on studying the impact of reduced-voltage operation in DRAM. Furthermore, low-power modes have a smaller effect on memory-intensive workloads, which exhibit little idleness in memory accesses, whereas, as we show in Section 3.2, our mechanism is especially effective on memory-intensive workloads.

**Low-Power DDR DRAM Chips.** Low-power DDR (LPDDR) [59, 61, 112] is a specific type of DRAM that is optimized for low-power systems like mobile devices. To reduce power consumption, LPDDRx (currently in its 4th generation) employs a few major design changes that differ from conventional DDRx chips. First, LPDDRx uses a low-voltage swing I/O interface that consumes 40% less I/O power than DDR4 DRAM [33]. Second, it supports additional low-power modes with a lower supply voltage. Since the LPDDRx array design remains the same as DDRx, our observations on the correlation between access latency and array voltage are applicable to LPDDRx DRAM as well. Voltron, our proposal, can provide significant benefits in LPDDRx, since array energy consumption is significantly higher than the energy consumption of peripheral circuitry in LPDDRx chips [33]. We leave the detailed evaluation of LPDDRx chips for future work since our current experimental platform is not capable of evaluating them. Two recent experimental works [72, 112] examine the retention time behavior of LPDDRx chips and find it to be similar to DDRx chips.

**Low-Power DRAM Architectures.** Prior works (e.g., [31, 35, 135, 137]) propose to modify the DRAM chip architecture to reduce the ACTIVATE power by activating only a fraction of a row instead of the entire row. Another common technique, called sub-ranking or mini-ranks, reduces dynamic DRAM power by accessing data from a subset of chips from a DRAM module [139, 145, 152]. A couple of prior works [102, 144] propose DRAM module architectures that integrate many low-frequency LPDDR chips to enable DRAM power reduction. These proposed changes to DRAM chips or DIMMs are orthogonal to our work.

**Reducing Refresh Power.** In modern DRAM chips, although different DRAM cells have widely different retention times [74, 96, 112], memory controllers conservatively refresh all of the cells based on the retention time of a small fraction of weak cells, which have the longest retention time out of all of the cells. To reduce DRAM refresh power, many prior works (e.g., [3, 11, 13, 68, 69, 70, 71, 95, 96, 97, 106, 108, 110, 112, 119, 138]) propose mechanisms to reduce unnecessary refresh operations, and, thus, refresh power, by characterizing the retention time profile (i.e., the data retention behavior of each cell) within the DRAM chips. However, these techniques do not reduce the power of other DRAM operations, and these prior works do not provide an experimental characterization of the effect of reduced voltage levels on data retention time.

**Improving DRAM Energy Efficiency by Reducing Latency or Improving Parallelism.** Various prior works (e.g., [26, 28, 54, 55, 80, 87, 88, 89, 90, 91, 92, 107, 128, 129, 130]) improve DRAM energy efficiency by reducing the execution time through techniques that reduce the DRAM access latency or improve parallelism between memory requests. These mechanisms are orthogonal to ours, because they do not reduce the voltage level of DRAM.

**Improving Energy Efficiency by Processing in Memory.** Various prior works [4, 5, 6, 10, 16, 17, 28, 41, 45, 46, 48, 49, 50, 51, 53, 57, 58, 67, 73, 81, 101, 111, 113, 114, 118, 126, 127, 129, 130, 135, 136, 149] examine processing in memory to improve
energy efficiency. Our analyses and techniques can be combined with these works to enable low-voltage operation in processing-in-memory engines.

**Experimental Studies of DRAM Chips.** Recent works experimentally investigate various reliability, data retention, and latency characteristics of modern DRAM chips [24, 27, 54, 63, 64, 70, 71, 76, 77, 87, 89, 90, 96, 97, 104, 112, 125, 132, 133] usually using FPGA-based DRAM testing infrastructures, like SoftMC [54], or using large-scale data from the field. None of these works study these characteristics under reduced-voltage operation, which we do in this paper.

**Reduced-Voltage Operation in SRAM Caches.** Prior works propose different techniques to enable SRAM caches to operate under reduced voltage levels (e.g., [7, 8, 32, 123, 141, 142]). These works are orthogonal to our experimental study because we focus on understanding and enabling reduced-voltage operation in DRAM, which is a significantly different memory technology than SRAM.

5. **Significance**

Our SIGMETRICS 2017 paper [29] presents a new set of detailed experimental characterization and analyses on the voltage-latency-reliability trade-offs in modern DRAM chips. In this section, we describe the potential impact that our study can bring to the research community and industry.

5.1. **Potential Industry Impact**

We believe our experimental characterization results and proposed mechanism can have significant impact in fast-growing data centers as well as mobile systems, where DRAM power consumption is growing due to higher demand for memory capacity for certain types of service (e.g., memcached). To reduce the energy and power consumed by DRAM, DRAM manufacturers have been decreasing the supply voltage of DRAM chips with newer DRAM standards (e.g., DDR4) or low-voltage variants of DDR, such as LPDDR4 (Low-Power DDR4) and DDR3L (DDR3 Low-voltage). However, the supply voltage reduction has been conservative with each new DDR standard, which takes years to be adopted by the vendors and the market. For example, since the release of DDR3L (1.35V) in 2010, the supply voltage has reduced by only 11% with the latest DDR4 standard (1.2V) released in 2014. Furthermore, since the release of DDR4 in 2014, the supply voltage for most commodity DDR4 chips has remained at 1.2V. As a result, further reducing DRAM supply voltage below the standard voltage, as we do in our SIGMETRICS 2017 paper [29], can be a very effective way of reducing DRAM power consumption. However, to do so, we need to carefully and rigorously understand how DRAM chips behave under reduced-voltage operation.

To enable the development of new mechanisms that leverage reduced-voltage operation in DRAM, we provide the first set of comprehensive experimental results on the effect of using a wide range of different supply voltage values on the reliability, latency, and retention characteristics of DRAM chips. In this work, we demonstrate how we can use our experimental data to design a new mechanism, Voltron (Section 3), which reduces DRAM energy consumption through voltage reduction. Therefore, we believe that understanding and leveraging reduced-voltage operation will help industry improve the energy efficiency of memory subsystems.

5.2. **Potential Research Impact**

Our paper sheds new light on the feasibility of enabling reduced-voltage operation in manufactured DRAM chips. One important research question that our work raises is how do modern DRAM chips behave under a wide range of supply voltage levels? Existing systems are limited to a few DRAM power states, which prevent DRAM from serving memory accesses when it enters a low-power state. However, in our work, we show that it is possible to operate commodity DRAM chips under a wide range of supply voltage levels while still being able to serve memory accesses under a different set of trade-offs. To facilitate further research initiative to exploit reduced-voltage operation in DRAM chips, we have open-sourced our characterization results, FPGA-based testing platform [54], and DRAM SPICE circuit model (for validation) in our GitHub repository [124]. We believe that these tools can be extended for other research objectives besides studying voltage reduction in DRAM. One potential direction is to leverage our results to design mechanisms that reduce DRAM latency by operating DRAM at a higher supply voltage.

5.3. **Applicability to Other Memory Technologies**

We believe the high-level ideas of our work can be leveraged in the context of other memory technologies, such as NAND flash memory [19, 20, 21], PCM [84, 85, 86, 103, 120, 121, 146, 147], STT-MRAM [30, 52, 82, 103, 109], RAM [143], or hybrid memory systems [1, 15, 42, 47, 62, 94, 98, 103, 116, 117, 121, 122, 146, 148, 151]. A recent work on NAND flash memory, for example, proposes reducing the pass-through voltage [18, 19, 20, 21] to reduce read disturb errors, which in turn saves energy. We refer the reader to past works on NAND flash memory for a more detailed analysis of reliability-voltage trade-offs [18, 19, 20, 21, 22, 23]. We hope our work inspires characterization and understanding of reduced-voltage operation in other memory technologies, with the goal of enabling a more energy-efficient system design.

6. **Conclusion**

Our SIGMETRICS 2017 paper [29] provides the first experimental study that comprehensively characterizes and analyzes the behavior of DRAM chips when the supply voltage is reduced below its nominal value. We demonstrate, using 124 DDR3L DRAM chips, that the DRAM supply voltage can be reliably reduced to a certain level, beyond which errors arise within the data. We then experimentally demonstrate the relationship between the supply voltage and the
We hope that the experimental characterization, analysis, and performance, efficiency, and/or reliability. We also hope that our paper’s studies inspire new experimental studies to understand reduced-voltage operation in other memory technologies, such as NAND flash memory, PCM, and STT-MRAM.

Acknowledgments

We thank the anonymous reviewers of SIGMETRICS 2017 and SAFARI group members for their feedback. We acknowledge the support of Google, Intel, NVIDIA, Samsung, VMware, and the United States Department of Energy. This research was supported in part by the ISTC-CC, SRC, and NSF (grants 1212962 and 1320531). Kevin Chang was supported in part by an SRCEA/Intel Fellowship.

References

[1] N. Aggarwal and T. F. Wenisch, "Thermostat: Application-Transparent Page Management for Two-Tiered Main Memory," in ASPLOS, 2017.
[2] N. Aggarwal et al., "Power-Efficient DRAM Speculation," in HPCA, 2008.
[3] A. Aggarwal et al., "Mosaic: Exploiting the spatial locality of process variation to reduce refresh energy in on-chip eDRAM modules," in HPCA, 2014.
[4] J. Ahn et al., "A Scalable Processing-in-Memory Accelerator for Parallel Graph Processing," in ISCA, 2015.
[5] J. Ahn et al., "PM-Enabled Instructions: A Low-Overhead, Locality-Aware Processing-in-Memory Architecture," in ISCA, 2015.
[6] B. Akin et al., "Data Reorganization in Memory Using 3D-stacked DRAM," in ISCA, 2015.
[7] A. R. Alamaldeen et al., "Adaptive Cache Design to Enable Reliable Low-Voltage Operation," IEEE TC, 2011.
[8] A. R. Alamaldeen et al., "Energy-Efficient Cache Design Using Variable-Strength Error-Correcting Codes," in ISCA, 2011.
[9] A. M. Amin and Z. A. Chishti, "A Hardware Cache Replacement and Write Buffering to Improve DRAM Energy Efficiency," in ISLPED, 2010.
[10] O. O. Babarinsa and S. Idreos, "Jafar: Near-data processing for databases," in SIGMOD, 2015.
[11] S. Baek et al., "Refresh Now and Then," IEEE TC, vol. 63, no. 12, pp. 3114–3126, 2014.
[12] R. Begum et al., "Energy-Performance Trade-offs on Energy-Constrained Devices with Multi-component DVFS," in ISDW, 2015.
[13] J. Bhati et al., "Flexible Auto-refresh: Enabling Scalable and Energy-efficient DRAM Refresh Reductions," in ISCA, 2015.
[14] M. Bi et al., "Delay-Hiding Energy Management Mechanisms for DRAM," in HPCA, 2010.
[15] S. Bock et al., "Concurrent Migration of Multiple Pages in Software-Managed Hybrid Main Memory," in ICCD, 2016.
[16] A. Boroumand et al., "LaisyPIM: An Efficient Cache Coherence Protocol for Processing-in-Memory," CAL, 2016.
[17] A. Boroumand et al., "Google Workloads for Consumer Devices: Mitigating Data Movement Bottlenecks," in ASPLOS, 2018.
[18] Y. Cai et al., "Read Disturb Errors in TLC NAND Flash Memory: Characterization and Mitigation," in ISSN, 2015.
[19] Y. Cai et al., "Error Characterization, Mitigation, and Recovery in Flash-Memory-Based Solid-State Drives," Proceedings of the IEEE, 2017.
[20] Y. Cai et al., "Error Characterization, Mitigation, and Recovery in Flash Memory Based Solid-State Drives," arXiv:1706.08642 [cs.AR], 2017.
[21] Y. Cai et al., "Errors in Flash-Memory-Based Solid-State Drives: Analysis, Mitigation, and Recovery," arXiv:1711.11427 [cs.AR], 2017.
[22] Y. Cai et al., "Vulnerabilities in TLC NAND Flash Memory Programming: Experimental Analysis, Exploits, and Mitigation Techniques," in HPCA, 2017.
[23] Y. Cai et al., "Data Retention in TLC NAND Flash Memory: Characterization, Optimization, and Recovery," in HPCA, 2015.
[24] K. Chandrasekar et al., "Exploiting Expensive Process-Margins in DRAMs for Run-Time Performance Optimization," in DATE, 2014.
[25] K. Chandrasekar et al., "DRAMPOWER: Open-source DRAM Power & Energy Estimation Tool," http://www.drampower.info.
[26] K. K. Chang et al., "Improving DRAM Performance by Parallelizing Refreshes with Accesses," in HPCA, 2014.
[27] K. K. Chang et al., "Understanding Latency Variation in Modern DRAM Chips: Experimental Characterization, Analysis, and Optimization," in SIGMETRICS, 2016.
[28] K. K. Chang et al., "Low-Cost Inter-Linked Subarrays (LISA): Enabling Fast Inter-Subarray Data Movement in DRAM," in HPCA, 2016.
[29] K. K. Chang et al., "Understanding Reduced-Voltage Operation in Modern DRAM Devices: Experimental Characterization, Analysis, and Mechanisms," in SIGMETRICS, 2017.
[30] M. T. Chang et al., "Technology Comparison for Large Last-Level Caches (LLCs): Low-Leakage SRAM, Low Write-Energy STT-RAM, and Refresh-Optimized eDRAM," in HPCA, 2013.
[31] N. Chatterjee et al., "Architecting an Energy-Efficient DRAM System for GPUs," in HPCA, 2017.
[32] Z. Chishti et al., "Improving Cache Lifetime Reliability at Ultra-Low Voltages," in MICRO, 2009.
[33] J. Choi, "LPDDR4: Evolution for new Mobile World," in MEMCON, 2013. Available: http://www.memcon.com/pdfs/proceedings2013/track1/LPDDR4_Evolution_for_a_New_Mobile_World.pdf
[34] B. F. Cooper et al., "Benchmarking Cloud Serving Systems with YCSB," in SOCC, 2010.
[35] E. Cooper-Balis and B. Jacob, "Fine-Grained Activation for Power Reduction in DRAM," IEEE Micro, vol. 30, no. 3, pp. 34–47, 2010.
[36] H. David et al., "Memory Power Management via Dynamic Voltage/Frequency Scaling," in ICAC, 2011.
[37] Q. Deng et al., "CoScale: Coordinating CPU and Memory System DVFS in Server Systems," in MICRO, 2012.
[38] Q. Deng et al., "MultiScale: Memory System DVFS with Multiple Memory Controllers," in ASPLOS, 2012.
[39] Q. Deng et al., "MemScale: Active Low-power Modes for Main Memory," in ASPLOS, 2011.
[40] B. Diniz et al., "Limiting the Power Consumption of Main Memory," in ISCA, 2007.
[41] J. Draper et al., "The Architecture of the DIVA Processing-in-memory Chip," in ICS, 2002.
[42] S. R. Dullor et al., "Data Tiering in Heterogeneous Memory Systems," in EuroSys, 2016.
[43] S. Eyerman and L. Eeckhout, "System-Level Performance Metrics for Multiprogram Workloads," IEEE Micro, 2008.
[44] X. Fan et al., "Memory Controller Policies for DRAM Power Management," in ISLPED, 2001.
[45] A. Farmahini-Farahani et al., "NDA: Near-DRAM acceleration architecture leveraging commodity DRAM devices and standard memory modules," in HPCA, 2015.
[131] A. Snavely and D. Tullsen, "Symbiotic Job Scheduling for a Simultaneous Multi-threading Processor," in ASPLOS, 2000.

[132] V. Sridharan et al., "Memory Errors in Modern Systems: The Good, The Bad, and The Ugly," in ASPLOS, 2015.

[133] V. Sridharan and D. Liberty, "A Study of DRAM Failures in the Field," in SC, 2012.

[134] Standard Performance Evaluation Corp., "SPEC CPU2006 Benchmarks," http://www.spec.org/cpu2006.

[135] H. S. Stone, "A Logic-in-Memory Computer," IEEE TC, 1970.

[136] Z. Sura et al., "Data access optimization in a processing-in-memory system," in CF, 2015.

[137] A. N. Udipi et al., "Rethinking DRAM Design and Organization for Energy-Constrained Multi-Cores," in ISCA, 2010.

[138] R. Venkatesan et al., "Retention-Aware Placement in DRAM (RAPID): Software Methods for Quasi-Non-Volatile DRAM," in HPCA, 2006.

[139] F. A. Ware and C. Hampel, "Improving Power and Data Efficiency with Threaded Memory Modules," in ICCD, 2006.

[140] M. Ware et al., "Architecting for Power Management: The IBM® POWER™ Approach," in HPCA, 2010.

[141] C. Wilkerson et al., "Trading Off Cache Capacity for Reliability to Enable Low Voltage Operation," in ISCA, 2008.

[142] C. Wilkerson et al., "Trading Off Cache Capacity for Low-Voltage Operation," IEEE Micro, 2009.

[143] H.-S. P. Wong et al., "Metal-Oxide RRAM," Proc. IEEE, 2012.

[144] D. H. Yoon et al., "BOOM: Enabling Mobile Memory Based Low-power Server DIMMs," in ISCA, 2012.

[145] D. H. Yoon et al., "Adaptive Granularity Memory Systems: A Tradeoff Between Storage Efficiency and Throughput," in ISCA, 2011.

[146] H. Yoon et al., "Row Buffer Locality Aware Caching Policies for Hybrid Memories," in ICCD, 2012.

[147] H. Yoon et al., "Efficient Data Mapping and Buffering Techniques for Multilevel Cell Phase-Change Memories," TACO, vol. 11, no. 4, pp. 40:1–40:25, 2014.

[148] X. Yu et al., "Banshee: Bandwidth-Efficient DRAM Caching via Software/Hardware Cooperation," in MICRO, 2017.

[149] D. Zhang et al., "TOP-PIM: Throughput-Oriented Programmable Processing in Memory," in HPDC, 2014.

[150] T. Zhang et al., "Half-DRAM: A High-Bandwidth and Low-Power DRAM Architecture from the Rethinking of Fine-grained Activation," in ISCA, 2014.

[151] W. Zhang and T. Li, "Exploring Phase Change Memory and 3D Die-Stacking for Power/Thermal Friendly, Fast and Durable Memory Architectures," in PACT, Raleigh, NC, September 2009, pp. 101–112.

[152] H. Zheng et al., "Mini-rank: Adaptive DRAM Architecture for Improving Memory Power Efficiency," in MICRO, 2008.