Front-end ASIC for Spectroscopic Readout of Virtual Frisch-Grid CZT Bar Sensors

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Abstract

Compact multi-channel radiation detectors rely on low noise front-end application specific integrated circuits (ASICs) to achieve high spectral resolution. Here, a new ASIC developed to readout virtual Frisch-grid cadmium zinc telluride (VFG CZT) detectors for gamma ray spectroscopy is presented. Corresponding to each ionizing event in the detector, the ASIC measures the amplitude and timing at the anode, the cathode and four pad sense electrodes associated with each sensor in a detector array. The ASIC is comprised of 52 channels of which there are 4 cathode channels and 48 channels which can be configured as either anode channels with a baseline of 250 mV or pad sense channels to process induced signals with a baseline of 1.2 V. With a static

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power dissipation of 3 mW, each channel performs low-noise charge amplification, high-order shaping, peak and timing detection along with analog storage and multiplexing. The overall channel linearity was better than ± 1 % with timing resolution down to 700 ps for charges greater than 8 fC in the 3 MeV range. With a 4 x 4 array of 6 x 6 x 20 mm³ virtual Frisch-grid bar sensors connected and biased, an electronic resolution of ≈ 270 e⁻ rms for charges up to 100 fC in the 3.2 MeV range was measured. Spectral measurements obtained with the 3D correction technique demonstrated resolutions of 1.8 % FWHM at 238 keV and 0.9 % FWHM at 662 keV.

Keywords: Application Specific Integrated Circuit (ASIC), low noise front-end, mixed signal, Cadmium Zinc telluride (CdZnTe or CZT), thallium bromide (TlBr), mercuric iodide (HgI₂), virtual Frisch-grid, 3D, gamma ray, spectroscopy, radiation detection

1. Introduction

The demand for compact, high resolution and low power multi-channel radiation detection systems to explore the frontier of nuclear science brings together a group of stakeholders with application interest in security, medicine, industry, geology, space exploration and high energy physics (HEP). At the forefront of the technological innovation space are advances in material science and monolithic application specific integrated circuits (ASICs). We developed an ASIC prototype that was optimized for virtual Frisch-grid cadmium zinc telluride (VFG CZT) sensors. Given the interest in room temperature detectors, we instrumented additional circuitry on the chip to facilitate proof of concept designs with other materials such as Mercuric iodide (HgI₂)
and thallium bromide (TlBr) sensors.

Gas, liquid, scintillator, and semiconductor sensors have been successfully demonstrated for x- and γ-ray spectroscopy [1] with niche applications based on practical trade-offs between cost, detection efficiency and achievable resolution. High purity germanium (HPGe) has the best energy resolution for sources with closely spaced energy peaks and low energy photons but these sensors must be cooled to temperatures around 130-77 K to yield resolutions down to ≈ 0.3% at 662 keV [2, 3] which constrain their deployment as portable radiation detectors.

Wide bandgap semiconductors such as mercuric iodide (HgI$_2$), thallium bromide (TlBr), and cadmium zinc telluride (CZT) are three attractive room temperature sensor materials with low dark current and high photoelectric cross-section. Polarization and charge trapping degrade the spectral performance of HgI$_2$ [4], yet, detectors with single pixel resolution below 1% FWHM at 662 KeV were reported [5]. TlBr is attracting renewed interest for gamma ray spectroscopy [6, 7] as techniques are being developed to address polarization in biased sensors [8, 9, 10, 11, 12]. Single pixel resolution on the order of 1% FWHM at 662 keV was reported at 20 °C where the detector showed stable performance [13, 14]. CZT has become the choice material for room temperature gamma ray detection and spectroscopy [15, 16]. Improvements in growth and characterization techniques are trending towards better spectral performance [17, 18].

For high energy gamma ray spectroscopy, large volume premium CZT crystals are required to achieve good detection efficiency and resolution < 1 % FWHM at 662 keV. Since the yield on large volume premium crystals
is impacted by crystal defects, smaller standard crystals are an attractive cost-effective alternative. To improve the resolution of CZT detectors, a number of techniques have been developed [19]. The fraction of the signal contribution due to hole trapping can be measured electronically then subtracted using the coplanar grid (CPG) technique [20, 21]. Alternatively, electrostatic shielding using the small pixel effect 3D position sensing method [22, 23, 24, 25] or the Frisch-ring approach [26, 27, 28, 29, 30, 31] can make the crystal single polarity (e−) sensing for improved performance. In a compact multi-channel system that utilizes these capabilities, custom ASICs are required for low noise and low power signal processing. The Virtual Frisch-Grid (VFG) approach incorporated an optimization of the Frisch-ring technique [32, 33, 34, 35]. This economical approach to CZT spectroscopy allows for the development of commensurable large volume detectors by tiling unit bar sensors (up to 40 mm thick) made from standard grade material into large arrays [36].

To facilitate practical applications of the VFG sensors, an advanced virtual Frisch-grid (AVG) ASIC was developed to independently readout the six electrodes (anode, cathode and four sense pads) associated with each VFG CZT bar sensor as shown in Figure 1. Each channel in the ASIC performs charge preamplification, high order shaping with configurable baseline (including baseline stabilization), amplitude measurement with corresponding event time extraction, analog data storage and multiplexing. In section 2, the architecture of the ASIC is presented. This is followed by the experimental setup and results in sections 3 and 4. We close the paper with our conclusions and future work in section 5.
Figure 1: Simulated preamplifier output corresponding to charge collected on six electrodes (anode, cathode and four pads) of a Virtual Frisch-grid CZT bar sensor.

2. AVG ASIC Architecture

2.1. Chip Level Architecture

The first AVG ASIC prototype designed to readout a 3 x 3 array of VFG CZT sensors has 36 anode channels to readout negative charge and 9 cathode channels to readout positive charge with a fixed 250 mV baseline. This architecture is upgraded to the second AVG ASIC prototype illustrated in Figure 2 with changes to the channel configuration. To accommodate a 4
Figure 2: Block diagram of the second AVG ASIC prototype. The chip implements a global control logic, configuration registers, 52 programmable input channels, two test generators, a bias, DACs, global logic, analog multiplexers and a monitor for in-situ tracking of critical circuit blocks.

A global logic selects between three modes of operation referred to as write-in, signal acquisition and readout. During write-in, a pseudo serial array of VFG bar sensors, the ASIC implements a total of 52 channels. The modular design incorporates 4 cathode channels (one for each 2 x 2 unit array of sensors) while each of the remaining 48 channels has the option to be independently configured as either an anode channel with a baseline of $\approx 250$ mV or a pad sensing channel with a baseline of $\approx 1.2$ V.
peripheral interface (pSPI) is used to shift data into the configuration registers from an external data acquisition system (DAQ). The configuration bits set the initial condition for the bias, adjust the digital-to-analog converters (DACs), and program the 52 channels and the test generators. The global bias block establishes the bias voltages and currents while the DACs set the threshold voltages for pulse amplitude discrimination and the output voltage of two test generators. In signal acquisition mode, the embedded generators are used to inject charge into the front-end.

The analog signal from each critical ASIC block can be multiplexed and monitored on a dedicated auxiliary port while running diagnostics or evaluating the chip in-situ. All anode channels are optimized for 3.3 pF of input capacitance while the cathode channels are optimized for 6.3 pF of input capacitance [37]. The ASIC has four programmable gains from 120 mV/fC to 20 mV/fC covering the energy range from 530 KeV to 3.2 MeV in CZT. Eight programmable shaping times from 250 ns to 12 µs are implemented to add flexibility to the design. The digital interface is low voltage differential signaling (LVDS) with on-chip 100 Ω termination resistors. Whenever a sensor event goes above threshold, the ASIC releases a flag. Subsequent readout by the external DAQ is realized with a token passing scheme. That is, the token controls the switching of the analog multiplexers, so only the channel in which the token resides can put analog data on the respective amplitude and timing ports for analog-to-digital conversion. In addition, a temperature sensor is integrated and its analog data is multiplexed onto the tail of the data stream after the last channel is read.
2.2. Anode and Pad Sensing Channels

A representation of the configurable anode or pad channel is presented in Figure 3. The signal chain in each of the 48 channels is comprised of a charge preamplifier with pole-zero cancellation, a fifth order shaper with bandgap referenced baseline holder [38] and a pair of extractor (discriminator, peak detector and time-to-amplitude converter) [39, 40, 41]. In anode mode, the total channel gain is configured as 20 mV/fC, 40 mV/fC, 60 mV/fC or 120 mV/fC while in pad sensing mode, the selectable channel gains are 13.3 mV/fC, 26.6 mV/fC, 40 mV/fC and 80 mV/fC.

The input of the charge preamplifier implements a PMOS transistor that is optimized for 3.3 pF total capacitance at a drain bias current of 120 µA [37]. At the optimization point, a gate geometry (W/L) of 310 µm/0.36
µm with a corresponding gate capacitance \( (C_g) \) of approximately 816 fF and a transconductance \( (g_m) \) of about 2.2 mS is obtained. The transistor contributes 79 rms electrons to the ENC at 1 µs shaping time and dissipates \( \approx 300 \) µW. In addition, a current mirror continuous adaptive reset connected in the feedback loop establishes the amplifier bias point and provides continuous reset of the circuit after each measurement \[42, 43, 44\]. The pole introduced by the feedback loop is cancelled with a scaled replica of the mirror which created a zero at the output of the preamplifier. With this arrangement, the charge amplifier provides selectable charge gains of 48 or 96 \[45\].

Signal shaping is realized with a 5\(^{th}\) order complex conjugate semi-Gaussian shaper \[46\] with adjustable shaping times of 250 ns, 500 ns, 1 µs and 2 µs. Cognizant of the developments in wide bandgap sensors such as TlBr, additional circuitry is implemented for selectable shaping times of 3 µs, 6 µs and 12 µs to facilitate proof of concept designs with sensors characterized by longer drift times. The simulated shaper output in anode configuration and pad configuration is shown in Figures 4a and 4b respectively.

The first ASIC prototype implements 45 channels with fixed baselines of \( \approx 250 \) mV for shaper responses up to 2 V above baseline as shown by the blue trace in Figure 4a. When connected to a 3 x 3 array of VFG sensors, this ASIC can readout charge from 9 cathodes, 9 anodes and 27 pads. For the channels that are connected to the sensor pad electrodes, the shaped negative pulse response to an induced transient is clipped as shown by the red trace in Figure 4a since there is not enough headroom for the negative voltage swing.

In the second prototype, solving this problem by designing a dedicated
Figure 4: Simulation of a channel in: (a) anode configuration with a baseline of 250 mV for unipolar pulse shaping. If connected to a sensor pad electrode, the negative pulse response to induced pad transients are clipped (b) pad configuration with a baseline of 1.2 V added in the second prototype. Full amplitude response to induced transient from the pad electrode.

Figure 5: A $5^{th}$ order shaper with one real pole, two pairs of complex conjugate poles, a baseline holder and inverting stage with programmable bandgap references of 0.25 V and 1.2 V.

channel to process the transient pad signals would almost double the power and the silicon area. This issue is addressed in Figure 5 by adding an analog
inverting stage after the shaper and shifting the baseline to 1.2 V when a channel is configured to process pad induced signals with the response shown in Figure 4b. Forty eight of these configurable channels are implemented in the second prototype.

Pulse height discrimination and threshold equalization is realized by two low hysteresis discriminators with 5 bit trims per channel that compensates for baseline dispersions. A pair of peak detector and time-to-amplitude converters (TACs) extracts and store the bi-parametric amplitude and analog timing data corresponding to an event.

2.3. Cathode Channel

The chip is designed with four cathode channels that service a modular 4 x 4 array of sensors. Each of the four cathode channels independently processes positive charge from a cathode electrode that is common to a unit 2 x 2 sensor array. A block diagram of the cathode channel is illustrated in Figure 6. The channel implements a low noise charge preamplifier optimized for 6.3 pF input capacitance, a pulse or ramp test circuit and a feedback network that reset the circuit after each measurement.

The output of the preamplifier is split into two parallel signal processing chains. One signal path measures the event amplitude with selectable channel gain of 20 mV/fC or 60 mV/fC while the other signal path measures the event timing with selectable gain of 27 mV/fC and 162 mV/fC. The amplitude-processing branch was similar to the anode channel presented in section 2.2.

The event timing is realized as a fast 3rd order unipolar shaper which comprises one real pole and a pair of complex conjugate poles with adjustable peaking times of 100 ns, 200 ns, 400 ns, and 800 ns. A band-gap referenced
baseline holder prevents baseline drift while a threshold discriminator with 4-bit trimming triggers a programmable time-to-amplitude converter (TAC) for above threshold events. The trigger from the discriminator initiates a voltage ramp that is sampled by a reference signal from the external DAQ. The sampled voltage is stored on analog memory inside the TAC for readout.

2.4. ASIC Prototype

A micrograph of the second ASIC prototype is shown in Figure 7. On the left side of the die are 52 input channels that interface with the sensor electrodes. The channels are arranged in four groups of twelve anode/pad
Figure 7: A photograph of the second AVG ASIC prototype. There are 52 input channels arranged in four groups of 12 anodes and a cathode. At the back-end are bias, configuration, readout control and interface ciruity. The layout size is 7.6 mm x 10 mm.
channels plus a cathode channel. At the channel level, the functional blocks are linearly arranged with a preamplifier at the input followed by a shaper then two peak detectors, two time detectors and local control logic. The common circuits such as buffers, bias, DACs, configuration registers and global logic are at the back-end of the layout. Power and ground are supplied from the top and bottom of the chip while the back-end is reserved for bidirectional signal interfacing with the external DAQ. The chip was fabricated in a commercial 250 nm process with a silicon footprint of 7.6 mm x 10 mm and dissipates 177 mW of static power.

3. Experimental Setup

The first prototype of the ASIC was wirebonded to a custom 28 mm x 22 mm carrier board shown in Figure 8(a) with on board decoupling capacitors and discrete electrostatic discharge protection devices for the cathode channels. On the front of the carrier board were two electrically isolated connectors for digital (top) and analog (bottom) power and signal interface respectively. On the back (Figure 8(b)) of the board were two connectors that accommodated a detector board which housed a 3 x 3 array of VFG CZT sensors. Similarly, the 52 channel revised prototype was wirebonded to the front of a 45 mm x 45 mm interposer (Figure 8(c)). The detector was connected to the back of the board (Figure 8(d)) through a Z-ray connector [47].

A picture of the external DAQ is shown in Figure 8(e) with one of two analog motherboards plugged into the assembly. A first prototype carrier board was mounted on the front of an analog motherboard which provides
Figure 8: A 45 channel first ASIC prototype wirebonded to (a) the front of a 28 mm x 22 mm carrier board with (b) 2 connectors on the back to accommodate the sensor array. The second 52 channel ASIC prototype (c) mounted on the front of a 45 mm x 45 mm interposer while (d) the pads on the back interface with the detector module through a Z-ray connector. (e) An assembled external DAQ with the first ASIC carrier board mounted on an analog motherboard.

Low noise (< 20 µV rms) power and analog-to-digital conversion as depicted by the discrete components on the back of the second motherboard. In the fully assembled system, the two motherboards were read out by an Altera Arria GX FPGA board that supplied system power along with the option for optical fiber, Gigabit Ethernet or USB communication. The system required only two connections to operate. That is, one connection for main power and the other for communication with a computer. During measurements, the system was placed in a slotted aluminum enclosure with thinned walls that formed a Faraday cage around the ASICs and sensors.
Figure 9: Measured equivalent noise charge at low gain (solid symbols) and high gain (open symbols) for an anode channel (blue traces), a pad channel (green traces) and a cathode channels (red traces) as a function of shaping time. The solid lines are measurements without a sensor and the dashed lines are measurements with a 6 x 6 x 20 mm$^3$ VFG CZT sensor.

4. Experimental Results

Figure 9 shows the measured equivalent noise charge (ENC) as a function of shaping time for an anode channel (blue), a pad channel (green) and a cathode channel (red) with and without the sensor connected. The noise voltage at the buffered output of the shaper was measured with a Rhode
and Schwarz true RMS meter then referred to the input of the preamplifier. Without the sensor connected, at high gain covering the 530 keV energy window in CZT, the anode channel gave an ENC of \( \approx 60 \) e\(^-\) RMS at 1 \( \mu \)s shaping time for an effective dynamic range of \( \approx 760 \). Further, at low gain (3.2 MeV maximum photon energy) an ENC of 100 e\(^-\) corresponding to a dynamic range of \( \approx 2900 \) was attained. As designed, the difference is attributed to the noise contribution from the shaper. With a 6 mm x 6 mm x 20 mm VFG CZT sensor connected and biased between 2-3 kV, the dynamic range achieved was \( \approx 900 \) and \( \approx 200 \) for low gain and high gain respectively. The measured ENC without the sensor at each shaping time was less than that measured with the sensor. This can be explained as follows. Without the sensor connect, the dominant part of the interconnect capacitance (on the order of a few hundred femto-Farads) was already incorporated in the carrier board. With the sensor connected, each electrode capacitance (on the order of pico-Farads) substantially increases the contribution of the series noise (white and low-frequency). In addition, the sensor leakage current (bias voltage dependent) contributed quadratically to the total ENC.

The cathode which was optimized for a larger capacitance and smaller gains (20 mV/fC and 60 mV/fC) had an electronic noise contribution that was less than 300 e\(^-\) rms at all shaping times without the sensor. With the sensor connected and biased (dotted traces), the ENC for the cathode was below 450 e\(^-\) rms at 1 \( \mu \)s shaping time. For VFG CZT applications, the maximum shaping time did not exceed 2 \( \mu \)s. At longer shaping times, the parallel noise dominated due to increased integration time of the current from the adaptive reset and the sensor leakage current. Though less than optimal
for the ENC, we implemented the longer shaping times for prototyping and proof of concept designs with sensor material such as TlBr and HgI$_2$ that have long drift times.

The anode channel response to 16.7 fC of injected charge from the on-chip test generator at four shaping times (0.25 µs, 0.5 µs, 1 µs and 2 µs) and four gains (covering 0.53 MeV, 1.06 MeV, 1.6 MeV and 3.2 MeV in CZT) is shown in Figure 10. The anode had a baseline of 250 mV with a maximum voltage swing of $\approx 2$ above baseline.

Similarly, a plot of the same channel’s response to 25 fC of injected charge when configured as a pad sensing channel to process induced charge is shown in Figure 11. In this configuration, the baseline was held at 1.2 V and the measured shaper response to induced transients were bipolar pulses with amplitude swings up to $\pm 1$ V. This was an improvement to [45, 49] that was designed to readout pixelated sensors with 250 mV baseline and maximum pulse amplitude responses of $+2/-0.05$ V. During data acquisition, the
Figure 11: Measured sensing pad response to 25 fC of charge at four gains and four shaping times.

ASIC measured the peak amplitude along with the corresponding timing data from the positive and negative peaks. This data was combined with the independent bi-parametric measurements from the other channels to correct the photopeak for each event.

A plot of the best fit lines and the residuals for an anode and a cathode channel is shown in Figure 12. The anode had a linearity on the order of +0.9/-0.4% while the cathodes were measured in the range of +0.4/-0.2%. The cathode measurements were obtained by varying the amount of charge (up to 100 fC) injected into the front-end with the on-chip test generator and recording the corresponding amplitude. Regarding the anode on-chip test generator, a scaling factor in this circuit limited the maximum injected charge to 50 fC in the 3.2 MeV energy range. It should be noted that while this was a minor inconvenience for the evaluation of the chip, there was absolutely no impact on the designed charge measuring capabilities with a
sensor connected. Therefore, the attenuated output of a LeCroy 9210 pulse generator was capacitively coupled to the anode front-end for the injection of charge (up to 100 fC).

The timing response of the anode channel was measured with externally injected charge while that of the cathode was evaluated with charge injected from the integrated test generator. For each increment of input charge (from 0.08 fC to 100 fC), representative samples of the time-to-amplitude converter (TAC) output were taken by the external DAQ. The statistical mean of the TAC output was used to evaluate the timewalk while the standard deviations were used to determine the time resolution.

Figure 12: Measured anode and cathode linearity better than ± 1 % in the 3.2 MeV energy range for up to 100 fC of injected charge.
Figure 13: Measured anode time resolution at 20 mV/fC (solid symbols) and 120 mV/fC (open symbols) for injected charge up to 100 fC.

Figure 14: Measured anode time walk at 20 mV/fC (solid symbols) and 120 mV/fC (open symbols) for injected charge up to 100 fC.
Figure 13 shows the anode time resolution. For a TAC duration of 1 µs, a minimum time resolution of 700 ps rms was measured at high gain (120 mV/fC) and 0.25 µs shaping when charge greater than 8 fC was processed. The ASIC demonstrated the capability to resolve charge down to 0.09 fC with a resolution of 31 ns. For a TAC duration of 2 µs, low gain (20 mV/fC) and 12 µs shaping time shaping time, input charges ≥ 0.7 fC were resolved at 290 ns or better. The corresponding timewalk adjusted to the minimum was captured in Figure 14 with a lower limit of 1.6 ns at high gain and 0.25 µs shaping time to an upper limit of 330 ns at low gain and 12 µs shaping time.

The cathode timing response for the threshold crossing of a fast unipolar pulse was evaluated with similar procedures to the anode except for the injection of holes into the front with the on-chip test generator. It should be noted that the high gain in the cathode was 60 mV/fC while the low gain was 20 mV/fC. At high gain and 0.25 µs, charges as low as 0.8 fC were resolved at 5.4 ns with corresponding timewalk of 58 ns as shown in Figures 15 and 16 respectively. At low gain and 12 µs shaping time, the resolution achieved was 50 ns with a corresponding timewalk of 1.67 µs. This general trend was explained in [50]. At low shaping time, high gain, and large charge injection, the slope of the pulse is relatively high which is ideal for good threshold crossing. Conversely, as the shaping time increased, the gain decreased and the injected charge decreased, the slope of the pulse decreased accordingly and the timewalk increased.

The first AVG ASIC prototype (with 36 anode channels and 9 cathode channels) was used to acquire spectra with four groups of VFG CZT sensors
Figure 15: Measured cathode time resolution at 20 mV/fC (solid symbols) and 60 mV/fC (open symbols) for injected charge up to 100 fC.

Figure 16: Measured cathode time walk at 20 mV/fC (solid symbols) and 60 mV/fC (open) symbols for injected charge up to 100 fC.
with different geometries. Three of the sensors had a common cross-sectional area of 6 x 6 mm$^2$ but differ in thicknesses of 20 mm, 30 mm and 40 mm while the fourth had a cross-section of 5 x 5 mm$^2$ and was 50 mm thick. Depending on the thickness, the sensors were biased from the cathode side between 3 kV and 9 kV while the anode side was held at virtual ground by the ASIC front-end to set up the drift field inside the sensor. The measurements were taken inside an environmental chamber where the temperature was held between 17-18 °C. An uncollimated $^{137}$Cs was used to irradiate the sensors from $\approx$ 1 cm above the cathode side. Initially, the VFG pad sensing electrodes were connected to the ASIC anode channels for readout but it was observed that the channel’s negative amplitude response to induced transients was clipped as discussed in section 2.2. This issue was addressed by connecting the VFG pad electrodes to spare cathode channels for signal readout.

With this configuration, we measured between 3.2 keV to 3.5 keV for the total cathode channel noise contribution which corresponds to 0.5 % - 0.6 % FWHM at 662 keV. For each sensor, after 3D correction, we achieved 0.76 %, 1.06 %, 1.10 %, and 1.6 % FWHM at 662 keV for the 20 mm, 30 mm, 40 mm, and 50 mm thick VFG CZT bar detectors respectively. Further improvements were realized by mapping the non-uniformities of each sensor then correcting the spectra based on the uniform regions of the sensor. From this optimization, we reported improved resolutions ranging from 0.7 %, 0.83 %, 0.85 % and 1.5 % FWHM at 662 keV for the uniform regions of each sensor. The lower resolution in the 50 mm sensor was attributed to the weak electric field near the anode.

The spectroscopic performance of the second AVG ASIC prototype (48
channels configurable as either anode or pad sensing channels and 4 dedicated cathode channels) was evaluated with a 4 x 4 array of 6 x 6 x 20 mm$^3$ standard grade CZT crystals with VFG electrodes added. The sensor array was biased at 2.8 kV and irradiated at $\approx 3$ cm from the cathode side with uncollimated $^{232}$U and $^{137}$Cs sources in an environmental chamber maintained at 23 °C. Using the conventional 1D (cathode/anode) correction, we reported energy resolutions of 2.8 % at 238 keV and 2.5 % at 662 keV. By applying the 3D correction it was shown that the resolution improved to 1.8 % at 238 keV and 0.9 % at 662 keV [52, 47]. Even though the leakage current and crystal defects limited the resolution, the results are very encouraging for standard grade CZT crystals that can be tiled to form commensurable large volume radiation detection systems.

5. Conclusions and Future Work

We demonstrated an ASIC with an electronic noise contribution of less than 100 $e^-$ at 1 µs shaping time in the 3 MeV energy range of CZT. The bi-parametric measurement of amplitude and timing in each channel for above threshold incident photon events enabled the 3D correction of the spectra taken with VFG CZT board sensors. The ASIC demonstrated that resolution less than 1 % FWHM at 662 keV can be obtained from spectral measurements with VFG sensors up to 40 mm thick.

In the current design, the anode test pulse generator was only capable of injecting a maximum charge of 50 fC instead of the desired 100 fC into the anode front-end channels. This issue was attributed to a coarse scaling factor in the charge delivered by the test generator. During the evaluation
of the chip, this observation was reproduced in simulation and subsequently solved. The improved layout will be implemented and verified in the next ASIC fabrication.

Further, two other design related issues were observed. First, the anode channels and pad sensing channels shared the same threshold voltage for the respective positive pulse amplitude discriminator. During normal ASIC operation with the VFG sensors, some channels were configured as anodes while others were configured as pad sensing. In both arrangements, the positive pulse amplitude discriminators shared a common threshold DAC. This created an issue since the baselines for anode channels were \( \approx 250 \text{ mV} \) while that for the pad sensing channels were \( \approx 1.2 \text{ V} \). After careful investigations, it was observed that setting a threshold voltage (about 3\( \sigma \)) above the noise floor of the 250 mV baseline resulted in normal chip operation. Under this threshold setting, the pad channels operated as designed but their shaping time had to be greater than or equal to that of the anode shaping time. Likewise, the chip performed as intended as only an anode could trigger a readout.

Second, at threshold voltages about 1 V and higher, the readout was triggered by above threshold events related to the positive pad channel amplitudes but these data sets were identifiable by their timing signatures. It is worth mentioning that a threshold this high on the anode is not practical since low energy events would be completely rejected. To address these two issues, separate DACs will be implemented for anode and pad signal discrimination. In addition, a circuit has been developed to block the flag generated by the pad signal from triggering the readout of the chip. These
Improvements will be implemented to ensure the full independence of each channel on the ASIC.

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