A Method for Improving Bandwidth of Multimode Optical Fiber Network

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Abstract. A high-speed data exchange network based on multimode fiber and RapidIO technology is widely used in existing projects. It consists of a fiber switch and a high-speed interface module. The fiber switch is used as the data exchange core to complete protocol conversion. The high-speed interface module is connected to the universal device node and is responsible for access conversion of the RapidIO bus between the optical network. The hardware design utilizes the commercial shelf architecture, the software design adopts a multi-buffer and multi-thread data exchange method to increase the entire network bandwidth from 300MB/s to 800MB/S.

1. Introduction

With high-speed frequency hopping, spread spectrum and wideband/ultra-wideband new style signal has been widely used. Front-end sensor data is exploding, data transmission and processing is in a booming phase. As a core unit of data communication exchange, high-speed data exchange network is facing the common requirements of high bandwidth, high efficiency and low latency. Combining the Fibre Channel and RapidIO high-speed bus technology to build a high-speed data exchange network is an effective way to solve the current actual needs.

Fibre Channel over Ethernet technology which allows Fibre Channel to use 10Gb Ethernet network protocols to encapsulate Fibre Channel frames based on Ethernet network protocol packets. By supporting Fibre Channel packets over Ethernet, FibreChannel and Ethernet LANs can share the same single or integrated network infrastructure, solving the problems caused by the coexistence of different types of networks, and maintaining the loss of Fibre Channel data rates. The Fibre Channel over Ethernet technology has been widely used in the high-speed data storage field of data centers, enabling enterprises to maintain existing investments in Fibre Channel storage, reduce data center cost and complexity, and simplify network management, storage environment wiring and data management costs, etc.

RapidIO technology is a packet switching based crossbar interconnect technology, which with high bandwidth, low latency, high efficiency and high reliability. The main function is high speed data transmission communication between peripherals and high performance embedded microprocessor, DSP module and FPGA module. Currently, RapidIO provides a good solution for internal interconnect communication between chip-to-chip and board-to-board high-speed interconnects. As a new high-speed data exchange bus, RapidIO has experienced six versions of 1.1, 1.2, 1.3, 2.0, 2.1 and 2.2 since the release of the bus standard. Currently, the 2.x version supports 5GHz and 6.25GHz transmission rate. In recent years, the technology has been widely used in many high-tech electronic information products such as aerospace and ship field. The RapidIO plug-in backplane has become...
synonymous with standardized access equipment.

2. High Speed Network Design

2.1 FCoE protocol conversion and configuration

The high-speed interface module is implemented by a PowerPC processor and a 10G Ethernet controller. The processor integrates the RapidIO interface, configures the network port, debugs the serial port, and mounts the FCoE controller on the PCIe interface to implement the main conversion function. The high-speed interface module backplane the connectors VPX RP0, RP1, RP3, RP4, and pin definitions are implemented in accordance with VITA 46.0, 46.3, and 46.10 standards. The logical structure of the high-speed interface module is shown in Figure 1.

![Figure 1. High-speed interface module structure](image)

The high-speed interface module runs the Linux operating system. The software design of the interface module mainly includes three aspects: FCoE protocol, protocol conversion and dynamic configuration.

1) Ethernet Fibre Channel Protocol

The Ethernet Fibre Channel protocol mainly implements the FCoE Initialization Protocol (FIP) and the Fibre Channel Protocol (FCoE Protocol). The protocol hierarchy of the design is shown in Figure 2. The brown and gray parts are the implementation hierarchy of the existing Open-FCoE-SCSI protocol stack. The blue part is the part that needs to be developed and implemented for the FCoE communication protocol support. The entire protocol needs to be designed to implement a separate FC protocol raw frame (FC-RAW) interface, to achieve communication protocol support for extended link services (FC-ELS), to achieve FIP support.

![Figure 2. High-speed interface module software structure diagram](image)

The fiber-optic Ethernet data exchange protocol is implemented in a full-duplex, sequential transmission mode. In terms of data reliability transmission, the method uses a PFC (Priority-based Flow Control) and a transmission selection mechanism ETS (Enhanced TransmissionSelection) to enhance the network to avoid packet loss. In the case of multi-service data transmission in the same physical link, the PFC only stops the service data of the single-congested network, ensuring that other service data interactions are not affected; ETS is an optimal allocation of link bandwidth. Management mechanism to dynamically allocate the bandwidth of the service data transmission link according to the traffic flow.
2) High Speed Protocol Conversion

The high-speed protocol conversion software mainly implements the conversion of the RapidIO protocol to the FCoE protocol, which converts the large-scale communication and message door-to-door mechanism of RapidIO into FCoE message transmission. When the application layer sends and receives the RapidIO bus data packet, it needs to follow the user protocol for packing and unpacking. The single packet data includes the RIO header, the Payload field and the RIO tail. The Payload field is the user application data core field. The data link and the destination address used in the interaction are constrained, and the destination address includes the FCID and the RapidID number information.

The high-speed data interface module has set up 8 virtual links, 4 groups of sending channels and 4 groups of receiving channels, respectively, using DMA to establish a memory buffer, and the buffer address is mapped to the RapidIO bus address. The FCoE data packet process is when the main control thread arrives at the RapidIO bus data, acquires the Payload field data, and the data link data interacts with the thread pool according to the link selection field number. After the thread pool sub-thread acquires the data, it parses the FCID and RapidID numbers contained in the destination address, converts it into the destination address (MAC DA) in the FCoE frame format, and writes the entire Payload field to the FCoE data frame field to complete the data packet. The data unpacking process is relatively simple, data analysis can be performed on the protocol field FCoE data frame.

3) Dynamic exchange configuration

On the interface module of RapidIO conversion to FCoE, the FCoE data flow direction configuration is implemented through the configuration interface. on the interface module of FCoE conversion to RapidIO, Through the configuration interface, RapidIO can distribute the CPU data to the integrated information processor, and the module parameters and configuration information can be obtained through the configuration interface.

2.2 Data Exchange Software and Protocol

The standard access device communication interface supported by the high-speed data exchange network is mainly through SRL. The SRL nodes of different extension units (such as FPGA, DSP or PowerPC) can communicate with the high-speed interface module according to the agreed data format as long as they follow the RapidIO specification. And transparently distributing SRL data to a designated general information processing device node through a high speed interface module.

1) RapidIO initialization and ID assignment

The standard access device accesses the FCoE through the RapidIO interface. The initialization of
the RapidIO node can be completed by the standard access device or by the high-speed interface module. The ID modules of each RapidIO node need to be uniquely identified and distinguished from each other. A single high-speed interface module supports a maximum of 255 RapidIO nodes.

2) High speed switching multi-buffer setting

The high-speed switching module separately divides 128MB of DMA buffer space for fast data transmission interaction with standard access devices and general-purpose processing devices. The buffer setting is shown in Figure 6. The single buffer size is 1MB, and the buffer RapidIO address is calculated as the base address and the sum of offset addresses, when performing multiple SRIO data nodes for communication, use multi-thread for buffer maintenance.

![Figure 6. Buffer Settings for High Speed Interface Module](image)

3) RapidIO access and communication method

The RapidIO software interface of the high-speed interface module provides three communication modes: Nread and Nwrite, Message and Doorbell. The data transmission process is the same for the three communication methods. The communication flow of the three RapidIO nodes is shown in Figure 7.

The Nread and Nwrite communication modes are suitable for large-scale data communication, and the application layer large data blocks can be batch-sent to the designated RapidIO node, and the large-sized data can be received in batches for the user to process. When using NRead and Nwrite communication of RapidIO, the receiving endpoint notifies the sending endpoint of the local buffer address. The sending endpoint receives the address, sends the valid data part to the receiving endpoint by using the Nwrite method, and then the sending endpoint notifies the receiving endpoint by sending a Doorbell mechanism, and after receiving the data, the receiving end repeats the above work. Then the RapidIO communication between the sending endpoint and the receiving endpoint is completed after the loop processing.

Message communication mode is used for receiving and transmitting small block data. Its maximum receiving and transmitting length is 4 KB. Similar to UDP communication mode, its sending and receiving requires 4 parameters, namely localport, destid, buff and len. The high-speed interface module provides rioNread and rioNwrite functions.
3. High-speed Network Switching Bandwidth Test and Result

Based on the actual application requirements of shipborne intelligence reconnaissance, this paper builds application scenarios based on the characteristics of its universal access equipment and conducts test verification. There are two ways to access a high-speed data exchange network in a single universal access device, that is, a high-speed interface module connected with a single SRIO or multiple SRIO sending nodes. In order to fully test and verify the performance of the high-speed data exchange network, a single universal access device is used to implement three SRIO access modes, and data is distributed to two general-purpose processing device nodes. The specific connection relationship structure is shown in Figure 8.

Figure 8. Test connection block diagram

The test plan is shown in Table 1.

| Test Item | Test Conditions |
|-----------|-----------------|
| Single RapidIO | Packet size 1MB, Packet size 512KB, Packet size 256KB, Packet size 128KB |
| Two RapidIO  | Packet size 1MB, Packet size 512KB, Packet size 256KB, Packet size 128KB |
| Three RapidIO | Packet size 1MB, Packet size 512KB, Packet size 256KB, Packet size 128KB |

1) Single RapidIO Node test result
In the case of a single node, the test packet size is 1 MB, 512 KB, 256 KB, and 128 KB, the delay
and the number of transmissions are counted separately without packet loss. The test data is shown in Figure 9.

![Figure 9. Single RapidIO node test data](image)

2) Two RapidIONodes test Result
In the case of two nodes, the test packet size is 1 MB, 512 KB, 256 KB, and 128 KB, the delay and the number of transmissions are counted separately without packet loss. The test data is shown in Figure 10.

![Figure 10. two RapidIO nodes test data](image)

3) Three RapidIONodes test Result
In the case of three nodes, the test packet size is 1 MB, 512 KB, 128 KB, the delay and the number of transmissions are counted separately without packet loss. The test data is shown in Figure 11.

![Figure 11. three RapidIO nodes test data](image)

According to the usage flow of the high-speed data exchange network, the transmission delay and transmission rate indicators of the high-speed data exchange network are respectively tested for the actual use scenarios of the network, and the transmission capability of the high-speed data exchange network is evaluated and analyzed. The data transmission time of the first packet is defined as the transmission delay of the two consecutive data transmissions, and the transmission delay is sent. The transmission rate, that is, the data transmission bandwidth of the standard access device per unit time, which indicates the size of a single packet, the total number of packets, and the statistics time of transmission. The experimental results are shown in Table 2.2. Under the test scenario, the single RapidIO node can reach 829MB/S, the dual RapidIO node can reach 728MB/S, and the three RapidIO nodes can reach 628MB/S.
Table 2. Test results

| Test item       | sender/receiver | Packet size | Transmission delay(us) | Transmission rate(MB/s) | Transmission cnt(Times/s) |
|-----------------|-----------------|-------------|------------------------|------------------------|--------------------------|
| I               | Single RapidIO node experimental test data conclusion | 1           | node1/CPUA 1MB         | 1206                   | 829                      | 829                      |
|                 |                 | 2           | node1/CPUA 512KB       | 974                    | 513                      | 1026                     |
|                 |                 | 3           | node1/CPUA 256KB       | 892                    | 280                      | 1121                     |
|                 |                 | 4           | node11/CPUA 128KB      | 479                    | 261                      | 2087                     |
| II              | two RapidIO nodes experimental test data conclusion | 1           | node1/CPUA 1MB         | 2745                   | 364                      | 364                      |
|                 |                 | 2           | node1/CPUA 512KB       | 1426                   | 350                      | 700                      |
|                 |                 | 3           | node1/CPUA 256KB       | 1035                   | 241                      | 966                      |
|                 |                 | 4           | node1/CPUA 128KB       | 921                    | 135                      | 1085                     |
| III             | three RapidIO nodes experimental test data conclusion | 1           | node1/COMA 1MB         | 2764                   | 361                      | 361                      |
|                 |                 | 2           | node2/COMC 128KB       | 1477                   | 84                       | 677                      |

4. Conclusions

Based on FCoE and RapidIO bus technology, this paper adopts multi-buffer multi-thread data interaction transmission method to support multiple SRIO node data interaction scenarios of a single universal device. The entire network switching bandwidth is up to 800MB/S, and it has access standardization and interface universal. Advantages such as ease of use, low cost, and low cost. It has great application and promotion value.

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