Model Checking Software Programs with First Order Logic Specifications using AIG Solvers

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Abstract

Static verification techniques leverage Boolean formula satisfiability solvers such as SAT and SMT solvers that operate on conjunctive normal form and first order logic formulae, respectively, to validate programs. They force bounds on variable ranges and execution time and translate the program and its specifications into a Boolean formula. They are limited to programs of relatively low complexity for the following reasons. (1) A small increase in the bounds can cause a large increase in the size of the translated formula. (2) Boolean satisfiability solvers are restricted to using optimizations that apply at the level of the formula. Finally, (3) the Boolean formulae often need to be regenerated with higher bounds to ensure the correctness of the translation.

We present a method that uses sequential circuits, Boolean formulae with memory elements and hierarchical structure, and sequential circuit synthesis and verification frameworks to validate programs. (1) Sequential circuits are much more succinct than Boolean formulae with no memory elements and preserve the high-level structure of the program. (2) Encoding the problem as a sequential circuit enables the use of a number of powerful automated analysis techniques that have no counterparts for other Boolean formulae. Our method takes an imperative program with a first order logic specification consisting of a precondition and a postcondition pair, and a bound on the program variable ranges, and produces a sequential circuit with a designated output that is true when the program violates the specification. Our method uses sequential circuit synthesis reduction techniques to reduce the generated circuit, and then uses sequential circuit verification techniques to check the satisfiability of the designated output. The results show that our method can validate designs that are not possible with other state of the art techniques, and with bounds that are an order of magnitude larger.

Index Terms

Software verification, static analysis, Boolean satisfiability solvers, Hoare triplet
1 INTRODUCTION

The work in [1] takes a declarative formula $\phi$ in first order logic (FOL) with transitive closure and a bound on the universe of discourse and translates it to a sequential circuit expressed in VHDL. A sequential circuit is a Boolean netlist with memory elements and a hierarchical structure. It then passes the sequential circuit to SixthSense [2], an IBM internal sequential circuit verification framework, and decides the validity of $\phi$ within the bound. It scales to bounds larger than what is possible with Kodkod [3] which translates $\phi$ into a propositional Boolean formula in conjunctive normal form (CNF) and checks its validity using a Boolean satisfiability solver such as MiniSat [4].

The work in [5] translates an imperative C program, with an assertion statement therein, and a bound on the input size, into a sequential circuit expressed in VHDL. It then passes the sequential circuit to SixthSense [2] and decides the validity of the assertion within the bound. It scales to bounds larger than what is possible with CBMC [6]. CBMC unwinds loops and recursive functions up to the given bound, and translates the program into a CNF formula that asserts the properties. It then checks for correctness using a Boolean satisfiability solver.

In this work, we present our method that takes an imperative program $S$ with a specification, FOL precondition and postcondition pair $(P, Q)$, and checks whether $S$ satisfies the specification within a bound $b$ on the domain of the program and specification variables $(S \models (P, Q)|_b)$; i.e. when the bounded inputs of $S$ satisfy $P$, the outputs of $S$ satisfy $Q$. The program is written in $J$, a subset of C++/Java that includes integers, arrays, loops, and recursion. Our method translates the problem $S \models (P, Q)|_b$ into a sequential circuit with a designated output therein that is true iff the program violates the specification within the bounded domain. Our method uses sequential circuit synthesis reduction and abstraction techniques embedded in the open source ABC [7] framework to reduce the generated sequential circuit. Then it uses ABC verification techniques to decide the satisfiability of the designated output. ABC either (1) proves the validity of the program, (2) generates a counterexample illustrating that the program violates

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the specifications, or (3) reports an inconclusive result as it exhausts computational resources. Our method translates the counterexample back to the program domain and provides the user with a visual debugging tool (GTKWave [8]) to trace the violation.

Our method significantly extends the work of both [1], [5] in that

- it uses a program counter semantics to translate the program into an intermediary one loop program ($Olp$), where a program counter is an additional variable that encodes the control flow of the program. It encodes the data flow of the program into ternary conditional statements based on the value of the program counter. The work in [5] performs only a source to source translation to VHDL,
- it directly translates the $Olp$ program into bit level representation using And-Inverter-Graphs (AIG) sequential circuits while [1], [5] depend on the VHDL compiler and synthesis tools to do the translation to bit level,
- it supports imperative programs annotated with FOL specifications and also supports array boundary and overflow checks,
- it supports function calls including recursion,
- in case the original correctness check was not conclusive, it uses heuristics to guess a termination bound on the program execution time, it enables a termination guarantee check within the execution time bound, and it then uses the execution time bound with bounded model checking to decide correctness,
- it uses ABC [7], an open source sequential circuit synthesis and verification framework, instead of SixthSense [2] an IBM internal sequential circuit solver. ABC is a transformation-based verification (TBV) [7] framework that operates on sequential circuits and iteratively and synergistically calls numerous reduction and abstraction algorithms such as retiming [9], redundancy removal [10]–[13], logic rewriting [14], interpolation [15], and localization [16]. These algorithms simplify and decompose complex problems until they become tractable for ABC verification techniques such as symbolic model checking, bounded model checking, induction, interpolation, circuit SAT solving, and target enlargement [2], [17]–[20],
- our method is fully implemented as an open source tool ($\{P\}S\{Q\}$) available online

1. http://research-fadi.aub.edu.lb/dkwk/doku.php?id=sa
and compared our method to CBMC and other tools ranking top in the software verification competition [21]. \( P \) succeeded to find and report counterexamples for all defected programs. It found and reported defects that we were not aware of while developing the evaluation benchmarks. It scaled to verification bounds higher than those possible with the other tools, and proved specifications that were not possible by the other tools.

**Limitations of translation to Boolean formulae:** Recent advances in SAT enabled tools like Kodkod Alloy Analyzer [3], and CBMC [6] to check real programs. However, these programs often need to be partial, leaving out important functionality aspects, to enable the analysis to complete. Moreover, the analysis is typically bound to relatively small limits.

There are three limiting aspects of translating high-level programs to Boolean formulae.

**Disadvantage 1** The translation to Boolean formulae depends on the bounds; a small increase in the bound on variable ranges can cause a large increase in the size of the translated formula due to unwinding loop and recursion structures in programs, or eliminating quantifiers in declarative first order logic.

**Disadvantage 2** CNF SAT solvers are restricted to using optimizations, such as symmetry breaking [22] and observability don’t cares (ODC) [23], that apply at the level of CNF formulae. However these optimizations usually aim at increasing the speed of the solver and often result in larger formulae as they add literals and clauses to the CNF formula to encode symmetry and ODC optimizations [24]. Often times when the analyzer successfully generates a large CNF formula, the underlying solver requires intractable resources.

**Disadvantage 3** Often times the formula needs to be regenerated with higher bounds in case the unwinding bounds were not large enough for the loops to complete as is the case with CBMC and ESBMC.

To extend the applicability of static analysis to a wider class of programs as well as to check more sophisticated specifications and gain more confidence in the results, we need to scale the analysis to significantly larger bounds.

**Advantages of sequential circuits:** We formally define sequential circuits in Section 2.2; for now a sequential circuit can be viewed as a restricted C++ program, specifically a concurrent program in which all variables are either integers, whose range is statically bounded, or Boolean-valued, and dynamic allocation is forbidden [25]. There are two key advantages to compiling
programs into sequential circuits rather than Boolean formulae:

**Advantage 1** Sequential encodings are much more succinct than SMT or pure combinational SAT formulae. They are imperative and state-holding while CNF and SMT formulae are declarative and state-free. For example, they can naturally represent the execution of quantifiers and loops without the need for unrolling them. Moreover, they can store and reuse intermediate results in local variables. In cases, SAT and SMT encoding algorithms produce a data structure that uses several orders of magnitude more memory to represent.

**Advantage 2** Casting the decision problem for a program specification as an invariant check on a sequential circuit allows to leverage a number of powerful automated analysis techniques that we discuss in Section 2.3 and that have no counterpart in CNF or SMT analysis.

Other software verification techniques and tools exist that leverage predicate abstraction, interpolation, model checking, SMT, and other FOL and CNF solvers [26]–[32]. We discuss the tools and further compare our method to them in Section 7.

The rest of this paper is structured as follows. Section 2 reviews basic definitions and concepts related to Boolean formulae, and introduces the Jcore and J programs, sequential circuits, and the ABC framework. Section 3 provides an overview of the $P \{S \{Q\}$, introduces Olp programs, and illustrates the method with an array search example. Section 4 describes the translation of J programs into sequential circuits. Section 5 discusses the implementation. We discuss the results in Section 6, the related work in Section 7, and conclude with future work in Section 8.

# 2 BACKGROUND

In this section we define programs, sequential circuits, and introduce the ABC synthesis and verification framework. A reader well-versed in software verification may wish to skip this section, using it only as a reference.

## 2.1 J programs

The grammar on the left of Figure 1 defines Jcore, the core subset of J. A Jcore program is one or more declaration statements, followed by one or more statements. The directives a-un-op, a-bin-op, b-un-op, b-bin-op, and ba-bin-op denote arithmetic unary and binary operators, Boolean unary and binary operators, and Boolean arithmetic operators, respectively. The variables matching the var and array-var rules in a program $S$ form the sets of scalar variables $V = \{v_1, v_2, \ldots, v_m\}$ and array variables $A = \{a_1, a_2, \ldots, a_n\}$, respectively.
Definition 1 (terms): A target term is either a variable \( v \in V \), or an array access term of the form \( a[e] \) which denotes the \( e^{\text{th}} \) element of \( a \) where \( a \in A \) and \( e \) is an expression. A term is either a target term, or a constant \( c \in \mathbb{Z} \).

Definition 2 (expressions): An expression is a term, an arithmetic expression of the form \(-e, e_1 + e_2, e_1 - e_2, e_1 \ast e_2, e_1/e_2, e_1 \% e_2 \) where \( e, e_1, e_2 \) are expressions and \(-, +, \ast, /, \%\) denote subtraction, addition, multiplication, division and remainder, respectively.

Definition 3 (Boolean expressions): A Boolean expression is either (1) a constant from the set \( \mathbb{B} = \{ \text{true}, \text{false} \} \), (2) a binary Boolean arithmetic expression of the form \( e_1 < e_2, e_1 \leq e_2, e_1 > e_2, e_1 \geq e_2 \) where \( e_1, e_2 \) are expressions and \(<, \leq, >, \geq\), and \(==\) denote smaller, less than or equal, bigger than, bigger than or equal, and equal, respectively, (3) a binary Boolean expression of the form \( b \& \& b', b \mid b', b \rightarrow b', b == b' \) or (4) a unary Boolean expression of the form \( \neg b \) where \( b, b' \) are Boolean expressions and \&\&, \|, !, \rightarrow\), and \(==\) denote logical conjunction, disjunction, negation, implication, and equivalence, respectively.

Definition 4 (First order logic formula): A first order formula is either a Boolean expression, or
a quantified formula of the form $Qq.b(q)$, where $Q \in \{\forall, \exists\}$ is a universal or an existential quantifier, $q$ is a quantified variable, and $b(q)$ is a first order formula with $q$ as a free variable.

Definition 5 (Statement): A statement is (1) an assignment statement of the form $t = e$ where $t$ is a target term and $e$ is an expression, (2) a list of statements in a well defined order that could be empty, (3) a conditional statement if($b_1$) { then – block } else { else – block } where $b_1$ is a Boolean expression, and then – block, and else – block are lists of statements, (4) a while loop statement while($b_2$) { while – block } where $b_2$ is a Boolean expression and while – block is a list of statements, or (5) a declaration statement of the form type $v$; or type $a[constant]$; where type is either bool or int denoting the domain of the variable values, $v$ and $a$ denote the variables in sets $V$ and $A$, and constant denotes the size of the corresponding array.

The grammar of Figure 1 (right) extends Jcore to form J. Boolean expressions are extended with existential and universal quantifiers that quantify a Boolean expression over a range of variable values defined by a start and an end expression. Statements are extended with pre- and postconditions that share the same specification name (specname). Declaration statements are extended with function declarations that take an argument declaration list, and a body block including a return statement. Terms are extended with function calls with an argument call list.

J program semantics: The semantics of a program is defined in terms of traces of variable values across execution time. The assignment statements define the data flow of the program and their semantics is defined in terms of updating the value of the target term with the value of the expression of the assignment statement. The lists of statements, conditional statements, loop statements, function calls, and return statements define the control flow of the program. The program starts execution at the first statement in its list of statements. The list of statements defines the order of execution. An if/else conditional statement $s$ in a list of statements $\ell$ executes the then-block if the value of the Boolean expression $b$ is true, otherwise it executes the else-block. The last statement in the then-block and the else-block moves execution to the statement next to $s$ in $\ell$. A loop statement $s$ in a list of statements $\ell$ executes the first statement of the while-block if the value of the Boolean expression is true, otherwise it executes the statement next to $s$ in $\ell$. The last statement in the while-block moves execution back to the loop statement $s$.

A function call updates the values of the function argument declaration variables with the corresponding function call argument expressions and moves execution to the first statement of
the body-block. The return statement in a function declaration substitutes the corresponding
function call with the value of the return expression and moves execution back to the statement
that made the function call.

A specification \((P, Q)\) is a pair of first order formulae where \(P\) is the precondition specifying
constraints on the inputs of \(S\) and \(Q\) is a postcondition relating the outputs of \(S\) to its inputs.

### 2.2 AIG Sequential Circuit

**Definition 6 (Sequential circuit):** A sequential circuit is a tuple \(((U, E), G, O)\). The pair \((U, E)\)
is a directed graph on vertices \(U\) and edges \(E \subseteq U \times U\) where \(E\) is a totally ordered relation.
The function \(G : U \mapsto \text{types}\) maps vertices to \text{types}. There are three disjoint types: primary
inputs, bit-registers (which we often simply refer to as registers), and logical gates. Registers have
designated initial value, as well as next-state functions. Gates describe logical functions such as
the conjunction or disjunction of other vertices. A subset \(O\) of \(U\) specifies the primary outputs.
We denote the set of primary input variables by \(I\), and the set of bit-register variables by \(R\).

**Definition 7 (Fanins):** We define the direct fanins of a gate \(u\) to be \(\{v \mid (v, u) \in E\}\) the set of
source vertices connected to \(u\) in \(E\). We call the support of \(u\) \(\{v \mid (v \in I \lor v \in R) \land (v, u) \in \ast E\}\)
all source vertices in \(R\) or \(I\) that are connected to \(u\) with \(\ast E\), the transitive closure of \(E\).

For the sequential circuit to be syntactically well-formed, vertices in \(I\) should have no fanins,
vertices in \(R\) should have 2 fanins (the next-state function and the initial-value function of that
register), and every cycle in the sequential circuit should contain at least one vertex from \(R\).
The initial-value functions of \(R\) shall have no registers in their support. All sequential circuits
we consider will be well-formed.

The ABC analyzer reasons about AIG sequential circuits which are sequential circuits with only NAND
gates restricted to have 2 fanins. Since NAND is functionally complete, this is not a limitation.

**Semantics of sequential circuits:**

**Definition 8 (State):** A state is a Boolean valuation to vertices in \(R\).

**Definition 9 (Trace):** A trace is a mapping \(t : U \times \mathbb{N} \to \mathbb{B}\) that assigns a valuation to all vertices
in \(U\) across time steps denoted as indexes from \(\mathbb{N}\). The mapping must be consistent with \(E\) and
\(G\) as follows. Term \(u_j\) denotes the source vertex of the \(j\)-th incoming edge to \(v\), implying that
TABLE 1: Brief description of selected ABC synthesis and verification techniques.

| Technique   | Description                                                                 | Command |
|-------------|-----------------------------------------------------------------------------|---------|
| Balancing   | Logic balancing applies associativity transformation to reduce AIG levels.  | balance |
| Sweep       | Structural register sweep (SRS) reduces the number of registers in the circuit by eliminating stuck-at-constant registers [34]. | ssweep  |
| Correspondence | Signal correspondence (Scorr) computes a set of classes of sequentially-equivalent nodes using k-step induction [34]. | scl -l  |
| Rewriting   | AIG rewriting iteratively selects and replaces rooted subgraphs with smaller pre-computed subgraphs in order to reduce AIG size [35]. | rewrite |
| Refactoring | Refactoring is a variation of rewriting. It uses a heuristic to compute a large cut for selected AIG nodes, then replaces the sub-graph that corresponds to the cut with a refactored structure if an improvement is observed [36]. | refactor |
| Retiming    | Retiming manipulates register boundaries and count in a given logic network, while maintaining output functionality and logic structure [37]. | retime  |
| Induction   | Temporal induction uses circuit SAT and BDD solvers to carry simple and k-step induction proofs over the time steps of the AIG [38]. | ind     |
| Interpolation | Interpolation-based algorithms aim find interpolants and overapproximate the reachable states of the AIG with respect to the property [39]. | int     |
| Reachability | Property directed reachability (Pdr) tries to prove that there is no transition from an initial state of the AIG to a bad state [40]. | pdr     |

$$(u_j,v) \in E.$$ The value of gate $v$ at time $i$ in trace $t$ is denoted by $t(v,i)$.

\[
t(v,i) = \begin{cases} 
  s^i_v & : v \in I \text{ with sampled value } s^i_v \\
  t(u_1,0) & : v \in R, i = 0, u_1 := \text{initial-state of } v \\
  t(u_2,i-1) & : v \in R, i > 0, u_2 := \text{next-state of } v \\
  G_v(t(u_1,i),...,t(u_n,i)) & : v \text{ is a combinational gate with function } G_v 
\end{cases}
\]

The semantics of a sequential circuit are defined with respect to semantic traces. Given an input valuation sequence and an initial state, the resulting trace is a sequence of Boolean valuations to all vertices in $U$ which is consistent with the Boolean functions of the gates. We will refer to the transition from one valuation to the next as a step. A node in the circuit is satisfiable if there is an input sequence which when applied to an initial state will result in that node taking value $true$. A node in the circuit is valid if its negation is not satisfiable. We will refer to targets and invariants in the circuit; these are vertices whose satisfiability and validity is of interest, respectively. A sequential circuit can naturally be associated with a finite state machine (FSM), which is a graph on the states. However, the circuit is different from its FSM; among other differences, it is exponentially more succinct in almost all cases of interest [33].

### 2.3 ABC synthesis and verification framework

ABC is an open source synthesis and verification framework for sequential circuits. ABC operates on sequential circuits in AIG format and checks the satisfiability of a designated output gate.
Fig. 2: Overview of verifying J programs with AIG synthesis and verification techniques therein. ABC applies several reduction and abstraction techniques to simplify and decompose the problem into smaller problems. It then calls decision techniques to decide the simplified problems. Table 1 briefly summarizes some of the techniques supported by ABC.

3 OVERVIEW

Figure 2 illustrates our method. First, \( \{P\}S\{Q\} \) preprocesses program \( S \) with its FOL specification pair \( (P, Q) \) to resolve function calls, specifications, and quantifiers and produces an equivalent program \( S' \) in Jcore. It then translates \( S' \) into a one loop program where it encodes the control flow into an additional program counter variable and encodes the data flow into assignment statements with ternary conditional expressions that depend on the value of the program counter variable. Then \( \{P\}S\{Q\} \) translates the generated one loop program into an AIG circuit with bit vectors of fixed width that correspond to program variables. Array sizes are limited by the largest possible index and \( \{P\}S\{Q\} \) translates each array element into a vector of AIG registers. \( \{P\}S\{Q\} \) resolves array access operations to refer to the vectors of registers, it then instantiates equivalent logic circuits to the expressions and connects the circuits to the initial value and next state value functions of the registers. \( \{P\}S\{Q\} \) designates one output of the AIG circuit to be true when the program violates the specifications. Other AIG outputs signal out of bound array access and arithmetic overflow.

\( \{P\}S\{Q\} \) uses the ABC synthesis techniques to reduce the size and the complexity of the generated AIG circuit until it is amenable for verification. Once the AIG circuit is small enough, \( \{P\}S\{Q\} \) uses ABC verification algorithms to check the designated output. The verification technique may find a violation and return a counterexample, return a proof that the program is
correct within the bound, or return an inconclusive result after exhausting computational limits. When an ABC verification returns a counterexample, $\{P\}S\{Q\}$ translates the counterexample from the AIG circuit level to traces of variable values in the original program and provides the user with a visual debugging view using GTKWave [8].

We describe the termination guarantee bound technique, the $Ol p$ programs, relate them to AIG circuits, and then illustrate the translation to $Ol p$ using an array search example.

### 3.1 Termination guarantee bound

In case the ABC prove techniques do not reach a conclusive result, $\{P\}S\{Q\}$ uses heuristics to compute a termination upper bound $\theta$ in terms of execution time, and calls ABC twice. The first call is to verify that the program is guaranteed to terminate within the termination bound ($\psi \equiv time \geq \theta \rightarrow pc = \text{last}(S)$). The second call uses $\theta$ as a bound with the ABC bounded model checking technique to prove that the program does not violate the specification within the termination bound. Intuitively, checking $S |\equiv (P, \Psi)|_b$ is often easier than checking $S |\equiv (P, Q)|_b$, and once $\theta$ is confirmed as an upper bound for termination, bounded model checking is decidable.

### 3.2 One loop programs

The grammar in Figure 3 extends $Jcore$ with the primary and dotogether constructs to define one loop programs. The primary construct denotes a primary input variable declaration with non-deterministic values. The concurrent dotogether{together-block} denotes that all statements of the together-block list of statements execute simultaneously. An $Ol p$ starts with variable declarations. Then the init-list list of assignment statements concurrently initializes the $Ol p$ variables. After initialization, a loop keeps updating the values of the variables concurrently using the list of assignment statements next-list until the $Ol p$ is done as denoted by the notdone Boolean variable.

Intuitively, the structure of an $Ol p$ is similar to that of a sequential circuit where the variables
correspond to registers, the init-list and next-list correspond to the initial and next state value functions, respectively.

3.3 Array search example

The Array search program in Figure 4 takes as input an array \( a \), a start index \( s \), an end index \( e \), a data value \( d \), and the number of elements in the array \( n \). The precondition states that \( s \) and \( e \) are within array bounds and that \( n \) is within the bound of array sizes. The postcondition makes use of a variable \( rv \) denoting the return value. It states that if \( rv \) is valid between \( s \) and \( e \) inclusive, then \( a[rv] \) must be equal to \( d \), otherwise, \( rv \) must be invalid (-1) and all entries in \( a \) between \( s \) and \( e \) inclusive are not equal to \( d \). Figure 4 also shows a semantically equivalent Olp array search program in terms of the values of the common program variables at termination.

The equivalent program introduces Boolean variables \( \text{preas}, \text{postas}, \) and \( \text{notdone} \) to encode the precondition, postcondition, and termination state of the program, respectively. The equivalent program also introduces a program counter variable \( \text{pc} \) which encodes the control flow of the program as indicated in the comments of the original program. Variable \( \text{notdone} \) is initialized to \( \text{true} \), and \( \text{pc} \) is initialized to the first executable line of the program 3. Once \( \text{pc} \) reaches the last executable line of the program 13, the program terminates and thus \( \text{notdone} \) becomes \( \text{false} \). Assignment statements are grouped by target variables, and encoded into ternary conditional expressions that depend on the value of \( \text{pc} \). For example, the iterator \( i \) is assigned to \( s \) when \( \text{pc} \) is 3, incremented when \( \text{pc} \) is 8, and remains the same otherwise. Furthermore, the assignment statements on Lines 2 and 3 assign initial values to the target variables. The

```c
int ArraySearch(int[] a, int d, int s, int e, int n) {
    @pre as ( 0 <= s && s <= e && e < n && n <= MAXSIZE; }
    int i = s;       // pc = pc+1
    while ( i <= e ) { // pc = (i <= e) ? 5 : 10;
        if (a[i] == d) { // pc = (a[i] == d) ? 6 : 8;
            break;     // pc = 10;
        }
        else { // pc = 4;
            i = i+1;
        }
    return i;       // pc = 11; rv = i;
    @post as { // next-list with next state functions
        (s <= rv && rv <= e) -> a[rv] == d
    forall (int i)[s .. e]{
        a[i] != d -> (rv== -1) }
    } }
@endtogether ( // init-list for initial value0s
    @preas = 0 <= s && s <= e && e < n && n <= MAXSIZE;
    @postas = true; postas = true; }
    int pc = 0; notdone = true; postas = true; }
    while (notdone) { @dotogether {
        pc = (pc == 11) ? notdone : true;
        rv = (pc == 10) ? i : rv;
        pc = (pc == 0) ? 3: (pc == 3) ? 4 : rv;
        if (pc == 3) ? s : (pc == 8) ? i+1 : i;
        postas = (rv >= s && rv <= e) -> a[rv] == d &&
        @forall (int i)[s .. e]{a[i] != d -> (rv== -1);})))
```
assignment statements inside the while loop (Lines 5 to 15) compute the next state value of each of the target variables.

Our method translates the Olp program to an AIG sequential circuit where an iteration of the while loop is equivalent to a single time step in the AIG. For example, The pc variable ranges from 0 to 11 and is encoded with bit-vector of 4 registers with initial value functions set to 0 and next state functions set to gates representing the right hand side expression of the pc assignment statement. Section 4.4 discusses the translation from Olp to AIG.

Our method takes the resulting AIG and designates a gate therein that represents \(- (\text{preas} \land \text{done} \rightarrow \text{postas})\) as the output gate, passes the AIG to ABC, and checks for validity. The ABC solver returns the counterexample of Figure 13 with \(a = [15, 15, 15, 11], s = 3, e = 3, n = 4, d = 13, rv = 0\) where \(d\) is not in \(a\), and the return value is \(e + 1\), while the postcondition requires an invalid index \((-1)\). The provided counter example can be used to fix the program. A possible fix is to replace Line 6 with \(\text{return } i;\), and Line 10 with \(\text{return } -1;\). Our method takes the fixed program, translates it into a sequential circuit, and passes it to ABC which validates the correctness of the fixed program using symbolic model checking.

4 Transformation

In this section we present source to source transformation algorithms to translate a program \(S\) written in Jcore into a Olp program. We then present algorithms that preprocess a \(J\) program with functions and specifications and translates it into Jcore. Finally, we present algorithms for translating the generated Olp program into an AIG circuit. The algorithms follow the execution semantics of \(J\) and the correctness of the translation holds by construction. We first present helper functions and terms that are used in the algorithms.

4.1 Helper functions

Function \(\text{label}(s)\) takes a statement in \(S\) and returns a unique label in \(\mathbb{N}\). Function \(\text{next}(s)\) takes a statement \(s\) and returns the label of the next statement of \(s\) in a list of statements \(\ell\). If \(s\) is the last statement in \(\ell\), several cases arise.

1) \(\ell\) is a function declaration body-block, \(\text{next}\) returns the label of the return statement.
2) \(\ell\) is a while-block of a loop \(l\), \(\text{next}\) returns the label of the loop statement \(\text{label}(l)\).
3) \(\ell\) is a then-block or an else-block of a conditional \(s_1\), \(\text{next}\) returns the label of the statement next to \(s_1\) (\(\text{next}(s_1)\)).
4) Finally, \( \ell \) is the last statement in \( S \), \( \text{next} \) returns a special label \( \text{done} \).

Functions \( \text{first} \) and \( \text{last} \) return the first and the last statement in a list of statements, respectively, or \( \text{nil} \) if the list is empty. Functions \( \text{then} \), and \( \text{else} \) take a conditional statement \( s \) of the form \( \text{if} \ (b) \ \{ \text{then-block} \} \ \text{else} \ \{ \text{else-block} \} \). They return the labels of the first statement of the then and else blocks, \( \text{label}(\text{first}(\text{then-block})) \), and \( \text{label}(\text{first}(\text{else-block})) \), respectively. If the list of statements is empty, both functions return \( \text{next}(s) \).

Function \( \text{body} \) takes a loop statement or a function declaration. The loop statement is of the form \( \text{while} \ (b) \ \{ \text{while-block} \} \). The function declaration is of the form \( \text{type} \ \text{fname}(\text{arg-decl-list}) \ \{ \text{body-block} \} \) where \( \text{type} \), \( \text{fname} \), and \( \text{arg-decl-list} \) are the return type, name, and argument declaration list of the function, respectively, and \( \text{body-block} \) is a list of statements followed by a return statement. For a function declaration, \( \text{body} \) returns the label of the first statement in \( \text{body-block} \) (\( \text{label}(\text{first}(\text{body-block})) \)). For a loop, \( \text{body} \) returns the label of the first statement in \( \text{while-block} \). In case \( \text{while-block} \) is empty, it returns the label of the loop. Function \( \text{condition} \) takes a conditional or a loop statement and returns \( b \).

Functions \( \text{target} \) and \( \text{expr} \) take an assignment statement of the form \( \text{target-term} = \text{expression}; \) and return \( \text{target-term} \) and \( \text{expression} \), respectively. Function \( \text{base} \) and \( \text{index} \) take an array access term of the form \( a[e_1] \) or \( a[e_1][e_2] \) where \( a \) is an array variable, and \( e_1 \) and \( e_2 \) are expressions. Function \( \text{base} \) returns \( a \). When \( a \) is declared as \( \text{type} \ a[c_1] \), where \( c_1 \) is a constant, \( \text{index} \) returns \( e_1 \). When \( a \) is declared as \( \text{type} \ a[c_1][c_2] \), where \( c_2 \) is a constant, \( \text{index} \) returns \( e_1c_2 + e_2 \). Finally, function \( \text{typeof} \) takes a variable (or array variable) and returns its type.

4.2 \( \text{Jcore} \) programs to \( \text{Olp} \)

Algorithm \( \text{generateOneLoopProgram} \) of Figure 5 takes a program \( S \) written in \( \text{Jcore} \) and generates the \( \text{decl-list} \), \( \text{init-list} \), and \( \text{next-list} \) of an equivalent \( \text{Olp} \) program. Algorithm \( \text{generateDeclarationList} \) generates a declaration for each variable in \( S \), and also generates a primary input \( \text{vnondet} \) variable for each variable that is used before being initialized in \( S \). It also declares the program counter \( \text{pc} \) and the termination guard \( \text{notdone} \) variables. Algorithm \( \text{generateOneLoopProgram} \) calls \( \text{generateInitList} \) that generates \( \text{init-list} \) where all variables are initialized to 0 except those that are used before being assigned in \( S \), those are initialized with their corresponding non-deterministic primary input variables. The program counter \( \text{pc} \) and the termination guard \( \text{notdone} \) are initialized to the label of the first statement of the program, and to \( \text{true} \), respectively.
The generateOneLoopProgram Algorithm builds one assignment statement v-next-list for each variable v and appends it to next-list. If v is a regular variable, generateVarNextList iterates over each assignment s where v is the target and builds a nested ternary conditional expression v-expr that evaluates to expr(s) when pc points to the label of s. When pc does not point to a statement that assigns to v, v-expr evaluates to the original value of v which is denoted by appending v as the value of the last choice in in the nested ternary expression.
If \( v \) is an array variable, Algorithm `generateArrayNextList` from Figure 6 iterates over all statements \( s \) where \( v \) is target. It aggregates all expressions and index expressions into two nested ternary conditional expressions \( a\text{-index} \) and \( a\text{-expr} \) for the index expression and the right hand side expression of the \( v\text{-next-list} \) assignment statement. The ternary conditional expressions depend on the position of \( pc \) to return the corresponding expressions and index expressions. In case \( pc \) does not point to a statement with \( v \) as a target, then \( v\text{-next-list} \) makes sure that \( v[0] \) stays the same by appending 0 and \( v[0] \) as the last default choices in the ternary conditional expressions, respectively.

Finally, `generateOneLoopProgram` calls `generatePCNextList` from Figure 6 to encode the control flow of \( S \) into \( pc\text{-next-list} \) with a nested ternary conditional expression that defines the value of \( pc \). Algorithm `generatePCNextList` iterates over all statements and encodes their execution flow semantics. When \( s \) is at a conditional statement, \( pc \) moves to `then-block` if the Boolean condition evaluates to `true`, and to the `else-block` otherwise. When \( s \) is at a loop statement, then \( pc \) moves to the first statement of `body-block` if the Boolean condition evaluates to `true`, and to the statement next to the loop otherwise. When \( s \) is an assignment statement such that \( \text{target}(s) = pc \), then \( pc \) moves to the expression of \( s \); this is similar to a `goto` statement and may result from resolving function calls as discussed in Section 4.3. For other statements, \( pc \) points to the next statement.

### 4.3 Preprocessing \( J \) programs

\( \{P\}S\{Q\} \) resolves function declarations, return statements, functions calls, pre and post conditions, and quantifiers by translating \( S \) into \( S' \) that is restricted to \( Jcore \).

**Non recursive functions:** Algorithm `resolveNonRecursiveFunction` in Figure 7 considers the declaration and function calls of a function \( fname \). It declares two additional variables in the function. Variable \( return-pc \) is added to `arg-decl-list` and it holds the label that \( pc \) should return to after the function is done. Variable \( retvar \) is added to `func-decl-list` and it holds the value of the return expression when the function is done. The `func-return-statement` is then replaced by `func-return-list` that sets \( retvar \) and \( pc \) to \( \text{expr}(\text{func-return-statement}) \) and \( return-pc \), respectively.

For each statement \( s \) containing an \( fname \) function call, `resolveNonRecursiveFunction` constructs a list of assignment statements that marshal the arguments and set the \( return-pc \) to
**Fig. 7:** Resolve non-recursive function calls and declarations

the label of `fcall-ret-statement`. It then adds an explicit statement that sets `pc` to the label of the first statement in `fname`. The `fcall-ret-statement` reads the value of `retvar` into a unique function call return variable `fcall-retvar-i`. This is necessary to resolve multiple function calls in the same expression. Statement `s'` substitutes the function call by `fcall-retvar-i`. The argument marshaling, `fcall-ret-statement`, and `s'` form the list `func-call-list`. Finally, statement `s` is replaced by the list of statements `func-call-list`.

**Recursive functions:** Algorithm `resolveRecursiveFunctionDeclaration` of Figure 8 resolves a recursive function declaration `fname` into `Jcore` by emulating stack frames with depth `max-depth`. The argument and local variables of `fname` become arrays. References to them in the body of the function are replaced with the corresponding array variables indexed by an additional stack pointer `sp-i` that points to the current recursive depth of the function. The rest
of the translation follows similarly to Algorithm `resolveNonRecursiveFunction` of Figure 7 and declares additional variables to hold the return, and return program counter values.

Algorithm `resolveRecursiveFunctionCalls` of Figure 9 works similarly to resolving function calls in Figure 7 with additional attention to the stack pointer `sp`. Variable `sp` is used to appropriately marshal the arguments and the return program counter to the current frame of the recursive function.

Specifications and quantifiers: Algorithm `resolveQuantifier` of Figure 10 takes a quantifier expression `q` and the statement `s` that contains it. It declares a Boolean variable `q-i` in the scope of the quantifier to hold the value of the quantifier. It initializes `q-i` to `true` when `q` is a universal
Fig. 9: Resolve recursive function calls

quantifier, and to false when \( q \) is an existential quantifier. It translates the quantifier statement to a loop that iterates over the range of the quantified variable \( v \) and accumulates the value of the Boolean expression with a conjunction in case \( q \) was a universal quantifier, and a disjunction in case \( q \) was an existential quantifier. Algorithm \texttt{resolveQuantifier} substitutes for \( q \) in \( s \) by \( q\)-i to construct \( s' \). Finally, it replaces \( s \) with the constructed loop and \( s' \). Alternatively, if the Boolean expression in the quantifier does not include function calls, the quantifier can be unrolled into a sequence of conjunctions (disjunctions in case of an existential quantifier) of the Boolean expression for the range of \( v \). This allows for a smaller execution time.

Algorithm \texttt{resolvePrePost} of Figure 10 declares a Boolean variable \texttt{pre-specname} for each precondition statement \( s \) of the form \( \texttt{@pre specname \{boolean-expr\}} \). It then replaces the precondition statement with an assignment statement that updates \texttt{pre-specname} with the value of the corresponding Boolean expression \texttt{boolean-expr}. Algorithm \texttt{resolvePrePost} works similarly for the postcondition. Of special interest is the expression \( \texttt{pre-specname} \land \texttt{pc} = \texttt{label}(s) \rightarrow \texttt{post-specname} \) which expresses that the program satisfies the specification.
4.4 \textit{Olp} to AIG circuits

Algorithm \textit{variables} of Figure 11 instantiates vectors of AIG registers and primary inputs to translate the corresponding \textit{Olp} program variables and stores the translation in a lookup function \textit{vargates}. The width of a bit vector can be selected by the user, or set to match the default width of the declared type. Typically the default values for the bit width are 32 bits for an integer. Arrays are represented by a fixed number of array elements and each element is then treated as a regular variable. The number of array elements is either specified in the
program, bounded by the user, or fixed to a constant by \( \{P\}S\{Q\} \).

4.4.1 Assignment statements: \( \{P\}S\{Q\} \) considers each assignment statement \( s \) in \text{init-list}\ and \text{next-list} and traverses the right hand side expression of \( s \) with the recursive \text{traverse} Algorithm of Figure 11. If expression \( exp \) refers to a variable (base case), or an array access operator with a constant index, then \text{traverse} returns \( \text{vargates}(exp) \). If \( exp \) was an array access \( a[ie] \) where \( a \) is the array variable and \( ie \) is an index expression, then \text{resolveArrayAccess} of Figure 12 translates \( exp \) into a nested ternary expression where the conditions depend on the value of \( ie \) and the values are array access terms with constant indices between 0 and \( \text{size}(a) - 1 \). Algorithm \text{resolveArrayAccess} calls \text{traverse} again on the generated expression to produce the corresponding AIG.

If the expression is a logical, conditional, or arithmetic expression, then the \text{library} routine looks it up in a complete table of AIG circuits with the adequate bit width. For example, if the expression is a ternary conditional statement of the form \( b ? e_1 : e_2 \), then \text{library} instantiates a multiplexer, connects its two data fanins to the nodes corresponding to \( e_1 \) and \( e_2 \), connects its control fanins to the nodes corresponding to \( b \), and returns its fanouts. Alternatively, users have the choice to abstract multiplication, division, and remainder by non-constant factors with non-deterministic variables (uninterpreted functions).

4.4.2 Connections and array access target terms: For assignment statements with target terms that are regular variables, or array access with constant index expressions, \( \{P\}S\{Q\} \) connects the nodes corresponding to the right hand side expressions in \text{init-list} and \text{next-list} to the initial and next state value fanins of the corresponding register gates, respectively.

An assignment statement \( s \) of the form \( a[ie] = expr; \), where \( a \) is an array variable, \( ie \) is a non constant index expression, and \( expr \) is an expression, requires preprocessing before being translated to AIG. Algorithm \text{variables} instantiates \( \text{size}(a) - 1 \) register vectors corresponding to the elements of array variable \( a \), each requiring initial and next state value functions. Algorithm \text{resolveArrayTargetTerms} of Figure 12 takes as input an assignment statement \( s \) and replaces it with \( \text{size}(a) - 1 \) assignment statements of the form \( a[j] = (j == ie)?expr : a[j]; \) where \( j \) ranges from 0 to \( \text{size}(a) - 1 \) such that each array element \( a[j] \) evaluates to \( expr \) if \( ie \) evaluates to \( j \), otherwise, \( a[j] \) keeps its value.
Fig. 12: Resolve array access expressions and resolve array target terms

5 IMPLEMENTATION

We fully implemented \( \{P\}S\{Q\} \) using C++ and ANTLR [41] and integrated our implementation with the ABC synthesis and verification framework [7] and the GTKWave visualization tool [8]. The frontend supports the \( J \) syntax under C, C++, and Java. Figure 13 shows a trace that highlights the defect of the array search program of Figure 4 where \( d \) is not in \( a \) and \( rv \) is not \(-1\). \( \{P\}S\{Q\} \) provides a fully automated verification path of execution where it executes a well selected sequence of synthesis reduction and verification techniques that work well for software verification tasks. \( \{P\}S\{Q\} \) also supports an interactive shell with parser, synthesis, verification, and debugging commands where the user can save and use intermediary results, try different synthesis and verification strategies, and inspect counterexamples. Table 2 provides a short list of the \( \{P\}S\{Q\} \) commands. The commands allow the users to specify (1) the program, (2) bounds on variable data width, array size, recursion depth, and (3) optional automatically embedded checks on array out of bound access and arithmetic overflow. \( \{P\}S\{Q\} \) is available online as an open source tool with tutorial and documentation 2.

6 RESULTS

We evaluated \( \{P\}S\{Q\} \) by verifying software artifacts including library algorithms and data structures with complete sophisticated specifications from the Calculus of Computation book [42], an array based implementation of the red black balanced binary search tree (RBBST) with specifications formalized from [43], and a memory allocation model (MMAN) with complete specifications provided from the Frama-C ANSI C Specification Language (ACSL) [44]. Table 3 reports

2. http://research-fadi.aub.edu.lb/dkwk/doku.php?id=sa
TABLE 2: Summary of $\mathcal{P}\mathcal{S}\mathcal{Q}$ commands

| Command      | Description                                                                 |
|--------------|-----------------------------------------------------------------------------|
| read         | Parses a program and generates a parse graph.                              |
| print-time   | Prints the runtime time of the last command and the total run time.        |
| prove-scheme1| Performs a predefined scheme of sequential synthesis and proof strategies. |
| prove-scheme2| Performs a predefined scheme of sequential synthesis and proof strategies.  |
| abc cmd      | Performs the ABC techniques specified in cmd.                              |
| debug        | Generates a program counterexample from the AIG counterexample and allows the user to inspect the values in a textual format. |
| vdebug       | A visual version of debug that allows the user to view and interact with the traces using GTKWave. |
| start-sim    | Starts the simulator helper tool to help the user analyze the code and perform what-if analysis on variable values. |
| sim-variable | Runs the simulator helper tool to generate and display values for specific variables. |
| start-prove  | Configures the prove engine with parameters such as variable bit width, array size bounds, and recursion depth bounds, as well as overflow check, out of bound access check, and quantifier unrolling. |

The results with several bounds and compares against CBMC [6]. The results show that $\mathcal{P}\mathcal{S}\mathcal{Q}$ scales to bounds larger than CBMC by at least one order of magnitude.

We also evaluated $\mathcal{P}\mathcal{S}\mathcal{Q}$ with benchmark verification tasks from the 2014 software verification competition [21] each with memory safety, termination, and error label reachability checks. Some of the tasks are true where a proof is expected, and some are false where a counterexample is expected. We ran our experiments on a machine with similar settings to the server machine reported in [21] (3.4 GHz 64-bit Quad Core CPU, a 64 bit GNU/Linux operating system, and 32 GB of RAM). We compare our results to the leading tools in the competition. Table 4 reports the results where some of the leading tools in the competition (CBMC [6], ESBMC [45], BLAST [46], and CPAChecker [47]) successfully completed the verification task and compares against them in terms of running time. The results show that $\mathcal{P}\mathcal{S}\mathcal{Q}$ succeeded to verify all the tasks and ranked either first or second in terms of running time in comparison.
with the leading tools. Table 5 reports the results of verifying benchmarks from [21] where the leading tools reported a timeout and failed to complete the verification task. According to the wrapper scripts provided from [21], CBMC and ESBMC report a true result by default when they reach their timeout while the SAT or SMT solver are running, they report an unknown result when the timeout passes before they generate the first CNF or SMT instance to pass to the underlying solver. This is probably reasonable as CBMC and ESBMC consider the inability of the solvers to find counterexamples within the timeout period as an indication of the rarity or absence of such results. Thus we consider a true result with a timeout time from CBMC and ESBMC as a timeout result for comparison purposes. The results show that $\{P\}S\{Q\}$ succeeded to complete verification tasks that were not completed by the leading tools.

In the experiments, we used an automated script that ran reduction algorithms first with a timeout of 10 minutes with Table 4 and three minutes for Tables 4 and 5, followed by three instances of verification using the pdr, dprove, and ind ABC commands with proper timeout, number of frames, and BDD size configurations.

6.1 Algorithms and data structures

Table 3 shows that $\{P\}S\{Q\}$ was able to verify programs with sophisticated specifications faster than CBMC and for array sizes that CBMC could not verify. The table shows the number of memory elements (registers), gates, and logic levels before and after the ABC reductions. It also shows the total time taken and the time taken to verify the programs. The CBMC columns show the size of the generated CNF formulae in terms of the number of CNF variables and clauses. We developed the programs and the specifications and called $\{P\}S\{Q\}$ and CBMC to verify their correctness incrementally. Both $\{P\}S\{Q\}$ and CBMC returned counterexamples that we used to correct the programs and the specifications. For programs with array indirection where array elements are used as indexes of other arrays such as next, left, right, and parent in the linked list and red black balanced binary search tree (RBBBST), $\{P\}S\{Q\}$ and CBMC both succeeded in returning counterexamples for index out of bound violations. However, once we corrected those issues, CBMC mistakenly reported that the programs are correct while $\{P\}S\{Q\}$ correctly reported counterexamples related to the cardinality of the data structures after insertion or removal of elements. The rows highlighted in red report the time taken by CBMC to verify the defected code and return a wrong result versus the time taken by $\{P\}S\{Q\}$ to verify the correct code. Note that CBMC and other tools reportedly returned several wrong results for
## Table 3: Results of \( \{\mathcal{P}\} \mathcal{S}\{\mathcal{Q}\} \) and CBMC to verify array based algorithms and data structures with increasing array sizes. TO, MO, ERR, MISTAKE stand for timeout, memory out, runtime error, and verification mistake, respectively.

| Array size | \( \{\mathcal{P}\} \mathcal{S}\{\mathcal{Q}\} \) | CNF size | CBMC |
|------------|-------------------|--------|------|
| 3          | \n | 4                           | 4,612/4,508\n | 0.016 |
| 7          | \n | 4,612/4,508\n | 0.016 |
| 15         | \n | 16,332/8,928\n | TO |
| 31         | \n | 37,216/23,208\n | TO |
| 63         | \n | 75,856/69,616\n | TO |
| 256        | \n | TO/TO\n | TO |
| binary      | \n | 42,461/19,723\n | 38,493 |
| search      | \n | 100,379/42,410\n | 4,955,223 |
| bubble      | \n | 65,785/19,603\n | 7,298 |
| sort        | \n | 341,592/1,082,480\n | 455.5 |
| selection   | \n | 1,214,801/6,809,622\n | TO |
| sort        | \n | TO/TO\n | TO |
| array       | \n | 286,799/16,613\n | 2.3 |
| partition   | \n | 56,366/121,478\n | 25 |
| linked      | \n | 19,741/55,151\n | 0.37 |
| list        | \n | 315,305/11,297,841\n | TO |
| insert      | \n | 959,841/3,849,448\n | TO |
| linked      | \n | 3,269,941/14,350,256\n | TO |
| list        | \n | TO/TO\n | TO |
| remove      | \n | TO/TO\n | TO |
| RBBSS1      | \n | 15,763/6,364\n | 4,403,782 |
| insert      | \n | 52,993/28,622\n | 65,366 |
| remove      | \n | 40,794/29,281\n | 291,311 |
| memory      | \n | 140,841/66,558\n | 15,008 |
| manager     | \n | 4,454/1,387\n | 150 |
| average reductions | \n | 64.5\% | TO |

| Array size | Array size before/after reductions | \( \{\mathcal{P}\} \mathcal{S}\{\mathcal{Q}\} \) | CNF size | CBMC |
|------------|-----------------------------------|-------------------|--------|------|
| 3          | 86 / 41                           | \n | 4,612/4,508\n | 0.016 |
| 7          | \n | 4,612/4,508\n | 0.016 |
| 15         | \n | 16,332/8,928\n | TO |
| 31         | \n | 37,216/23,208\n | TO |
| 63         | \n | 75,856/69,616\n | TO |
| 256        | \n | TO/TO\n | TO |
| binary      | \n | 42,461/19,723\n | 38,493 |
| search      | \n | 100,379/42,410\n | 4,955,223 |
| bubble      | \n | 65,785/19,603\n | 7,298 |
| sort        | \n | 341,592/1,082,480\n | 455.5 |
| selection   | \n | 1,214,801/6,809,622\n | TO |
| sort        | \n | TO/TO\n | TO |
| array       | \n | 286,799/16,613\n | 2.3 |
| partition   | \n | 56,366/121,478\n | 25 |
| linked      | \n | 19,741/55,151\n | 0.37 |
| list        | \n | 315,305/11,297,841\n | TO |
| insert      | \n | 959,841/3,849,448\n | TO |
| linked      | \n | 3,269,941/14,350,256\n | TO |
| list        | \n | TO/TO\n | TO |
| remove      | \n | TO/TO\n | TO |
| RBBSS1      | \n | 15,763/6,364\n | 4,403,782 |
| insert      | \n | 52,993/28,622\n | 65,366 |
| remove      | \n | 40,794/29,281\n | 291,311 |
| memory      | \n | 140,841/66,558\n | 15,008 |
| manager     | \n | 4,454/1,387\n | 150 |
| average reductions | \n | 64.5\% | TO |

| Array size | Array size before/after reductions | \( \{\mathcal{P}\} \mathcal{S}\{\mathcal{Q}\} \) | CNF size | CBMC |
|------------|-----------------------------------|-------------------|--------|------|
| 3          | 94 / 56                           | \n | 6,503/24,533\n | 0.085 |
| 7          | \n | 16,172/68,130\n | 1.91 |
| 15         | \n | 42,461/19,723\n | 38,493 |
| 31         | \n | 100,379/42,410\n | 4,955,223 |
| 63         | \n | 65,785/19,603\n | 7,298 |
| 256        | \n | 341,592/1,082,480\n | 455.5 |
| binary      | \n | 1,214,801/6,809,622\n | TO |
| search      | \n | TO/TO\n | TO |
| bubble      | \n | TO/TO\n | TO |
| sort        | \n | TO/TO\n | TO |
| selection   | \n | TO/TO\n | TO |
| sort        | \n | TO/TO\n | TO |
| array       | \n | TO/TO\n | TO |
| partition   | \n | TO/TO\n | TO |
| linked      | \n | TO/TO\n | TO |
| list        | \n | TO/TO\n | TO |
| insert      | \n | TO/TO\n | TO |
| linked      | \n | TO/TO\n | TO |
| list        | \n | TO/TO\n | TO |
| remove      | \n | TO/TO\n | TO |
| RBBSS1      | \n | TO/TO\n | TO |
| insert      | \n | TO/TO\n | TO |
| remove      | \n | TO/TO\n | TO |
| memory      | \n | TO/TO\n | TO |
| manager     | \n | TO/TO\n | TO |
| average reductions | \n | 64.5\% | TO |
TABLE 4: Runtime results in seconds for verification tasks completed successfully by \{PSQ\} compared to the leading software verification competition tools. TO and ERR stand for timeout and error, respectively.

| Problem  | eca  | TO  | TO-T | 4.5 | 4.6 |
|----------|------|-----|-------|-----|-----|
| Problem01_00 true | 7.5  | TO  | TO-T  | 4.5 | 4.6 |
| Problem01_10 true | 9.06 | TO  | TO-T  | 4.6 | 4.4 |
| Problem01_20 true | 9.41 | TO  | TO-T  | 4.5 | 5.9 |
| Problem02_00 true | 10.68 | 460 | TO-T  | 4.3 | 6.3 |
| Problem02_10 true | 9.71  | 580 | TO-T  | 4.3 | 4.8 |
| Problem02_20 true | 10.14 | ERR | TO-T  | 4.3 | 4.8 |

- Most of the times where both \{PSQ\} and CBMC succeeded to verify the programs, \{PSQ\} took less time to complete the verification task.
- \{PSQ\} succeeded to verify the programs for bounds larger than what CBMC could verify.
TABLE 5: Results for verification tasks in seconds where \{P\}S\{Q\} terminated successfully while the leading tools either timed out or produced erroneous output. TO: timeout, TO-T: report true on timeout, TO-F report false on timeout, MISTAKE: report erroneous results, ERR: reported a runtime error, and UNKNOWN: report inconclusive result.

| Category                  | \{P\}S\{Q\} | BLAST | CBMC | CPAChecker | ESBMC |
|---------------------------|--------------|-------|------|------------|-------|
| Problem07_02_true         | ControlFlowInt/eca | 620   | TO   | TO-T       | TO    | UNKNOWN-TO |
| Problem09_02_true         | ControlFlowInt/eca | 433   | TO   | TO         | TO    | UNKNOWN-TO |
| Ackermann01_true          | Recursive    | 723   | N/A  | TO-T       | TO    | ERR-1.9     |
| Ackermann01_false         | Recursive    | 22    | N/A  | 0.73       | ERR-1.9 | TO-F       |
| Addition01_false          | Recursive    | 11.2  | N/A  | MISTAKE-TO | ERR-2  | TO-F       |
| EvenOdd01_true            | Recursive    | 0.68  | N/A  | 0.96       | ERR-1.9 | MISTAKE-0.4 |
| EvenOdd01_false           | Recursive    | 0.45  | N/A  | 0.2        | ERR-1.9 | 0.4        |
| insertion_sort_true       | loops        | 154   | MISS-6.6 | TO-T | TO    | UNKNOWN-TO |
| invert_string_false       | loops        | 0.22  | 1.8  | 0.47       | TO    | 0.6        |
| jain_3_true               | bitvector    | 1.44  | N/A  | 0.53       | TO    | 0.25       |
| linear_search_false       | loops        | 0.39  | 0.13 | 0.62       | ERR-2.6 | MISTAKE-0.3 |
| McCarthy91_false          | Recursive    | 1.2   | N/A  | 0.19       | ERR-1.9 | TO-F       |
| McCarthy91_true           | Recursive    | 567   | N/A  | TO-T       | ERR-1.9 | MISTAKE-TO |
| MultiCommutative_true     | Recursive    | 780   | N/A  | TO-T       | ERR-1.9 | MISTAKE-TO |
| s3_sshv_1_alt_true.BV     | bitvector    | TO    | N/A  | TO-T       | TO    | TO-T       |
| s3_sshv_1_true            | ssh-simplified | TO   | UNKNOWN-0.1 | 160 | 4.6 | 3.9 |
| s3_sshv_3_true            | ssh-simplified | TO   | 430   | 210  | 13  | 4   |
| s3_sshv_7_true            | ssh-simplified | TO   | 210   | 24   | 4.3 |
| Problem08_02_true         | ControlFlowInt/eca | TO   | TO   | UNKNOWN-TO | TO    | UNKNOWN-TO |

within the three hours seconds timeout.

- CBMC failed to generate the CNF formula for some programs with relatively larger array sizes while \{P\}S\{Q\} succeeded to verify some of them and generated AIG circuits but timed out while verifying the rest. This is significant since model checking typically returns counterexamples fast when they exist, and takes long time to report a proof for unsatisfiable (correct) claims. That is, \{P\}S\{Q\} succeeded to perform model checking for a significant time length, even when it timed out, as compared to CBMC that failed to generate the CNF formula, thus did not really test the program for correctness.

For the array search program, the precondition checks that the indexes are in range and the postcondition checks whether the return value is consistent. For the binary search program both the precondition and the postcondition specify the sortedness property for the array. For the bubble and selection sort programs, the precondition checks the sanity of the size of the array, and the postcondition specifies that the resulting array holds the same elements of the original array in order. For the array partition program, the precondition specifies the sanity of the indexes and the size of the array, and the postcondition specifies that the resulting array holds the same elements of the original array partitioned in order left and right of the cursor. The linked list insert and remove precondition specifies a non circular, in order, list of elements,
and the postconditions reassert the same specification with an additional cardinality condition. The RBBBST insert and remove precondition specifies the full characteristics of an RBBBST and that the index arrays involved all hold valid indexes. The postconditions reassert the same specification with an additional cardinality condition. The RBBBST insert also checks the sanity of the newly allocated node in the tree. The memory manager unit has several multidimensional arrays to bookkeep the use of memory chunks and the precondition and the postcondition assert the sanity of the arrays, and the consistency of the module. We made use of the assume statement __CPROVER_assume and loops to implement the preconditions and the quantifiers in CBMC.

The reduction algorithms used by \{P\}S\{Q\} were able to reduce the original problems on average to 64.5% of their memory elements, and to 51.2%, and 44.7% of their logic gate and level counts in often insignificant time. Without these reductions \{P\}S\{Q\} timed out on several benchmarks. These reductions have no counterparts in CBMC.

6.2 SV-COMP 2014 benchmarks

Tables 4 and 5 show the results of \{P\}S\{Q\} compared against the results reported in [21] for the leading participating software verification tools. We selected the benchmarks that required no or minor syntax modifications for the \{P\}S\{Q\} front end and compared the execution time of \{P\}S\{Q\} with the leading tools. The tables show the name of the benchmark, its category and the running time needed by the tools to complete verification with a timeout of 900 seconds as required by SVComp 2014 regulations.

\{P\}S\{Q\} succeeded to complete the verification tasks in Table 4 and ranked first or second in terms of running time. \{P\}S\{Q\} succeeded to complete the verification tasks in Table 5 where the leading tools either timed out, reported runtime errors, or reported a wrong result (produced a counterexample when the benchmark is correct, or produced a claim of correctness when the benchmark had a known defect).

For the last five verification tasks in Table 5 \{P\}S\{Q\} timed out without producing a conclusive result while some of the leading tools returned the correct result, reported a timeout, or reported an inconclusive result.

6.2.1 Interactive sessions: We inspected the results of the benchmarks where the automated \{P\}S\{Q\} script did not return a conclusive result. We were able to verify several of them
interactively via trying ABC synthesis reduction and verification commands and techniques with different configurations and settings. This is not possible with the tools we compared to.

7 RELATED WORK

ESBMC [45] uses SMT solvers to verify multi-threaded C programs by forcing bounds on the number of context switches, loop iterations, and recursive calls. It also uses an aligned memory model that resolves pointers. We differ in that we use AIG solvers, where we do not need to have bounds for loop iterations, and we plan in the future to extend our approach to concurrent programs by encoding each execution thread as a separate program counter and limiting the number of program counters.

VCC [28] is an industrial strength verification framework for concurrent low level C programs. It has a ghost type state system that tracks the validity of memory objects; i.e., references to memory objects do not overlap type states. It generates verification conditions that can be checked by Boogie; i.e. a high order logic analyzer. Boogie in turn uses the Z3 SMT solver [48] for automatic verification and Isabelle [49] for interactive verification. FranklinBIT [50] takes a bit-vector program with a verification condition and computes an unsound approximation (not over and not under) of the verification condition. Then it uses a logic solvers (SMT or propositional) to decide the original verification condition strengthened with the inductive unsound approximation.

LLBMC [51] is a bit precise bounded model checker for low level C programs that works on an intermediate assembly representation of the program using an SMT solver. Ultimate Automizer [52] computes appropriate abstractions of programs based on statements as alphabet atoms in an automata framework. The work in [53] is implemented within the CPAChecker [47] platform to verify event condition action (ECA) systems using BDDs. Our method allows the use of symbolic model checking through ABC that makes use of BDD without the need to restrict ourselves to ECA systems. The CPAChecker [47] framework passes a program $S$ and an invariant $\Psi$ to model checkers for verification. In case a model checker returns an inconclusive result, CPAChecker uses partial results to formulate a state predicate formula $\Phi$ where the invariant holds. This incrementally reduces the work of the next model checker to check $\neg \Phi$. In the future, we plan to extend the same idea to the ABC model checker. BLAST [46] is the predecessor of CPAChecker and it uses abstraction and refinement techniques to model check temporal properties of C programs. Similar to CPAChecker is UFO [54] that provides a
framework for exploring abstraction and interpolation techniques for software verification and uses SMT solvers as a backend.

CBMC [55] is a bounded model checker for ANSI-C programs that checks for properties such as pointer safety, array bounds and user assert statements. Given an ANSI-C program and a bound on the range of variables, CBMC produces a Boolean formula in CNF and checks the formula with SAT solvers. CBMC relies mostly on the power and speed of SAT solvers. SAT solvers often face an exponential blow up in the number of possible assignments to the atomic propositions. This problem, known as the state explosion, and the large number of variables and clauses used in the CNF encoding, limit the CBMC analysis to relatively small bounds.

The work in [26] uses an encoding similar to that of CBMC, but instead of producing a CNF formula it produces an SMT formula. The SMT formula allows for variables with no range bounds. The loops are still unrolled up to a finite bound and loop completion assertions fire in case the bound imposed on the number of loop iterations was small and the loop guard was still satisfiable. The higher level solver may now decide to reproduce a new SMT formula with bigger loop unrolling bounds and call the SMT solver on the new formula. We differ in that our encoding to AIG circuits requires no bounds on loop iterations. This allows for more succinct representation of programs than with SMT.

Java PathFinder [29] (JPF), is a popular explicit-state model checker for Java programs. It implements a customized Java virtual machine (JVM) that supports state backtracking and allows programs to check properties of a wide range of Java programs without the need to respecify the programs in specialized languages. JPF does not apply any program transformations. JPF also does not scale well in the presence of loops and branches with long running time. JPF operates at the word level, however, it does not make use of program specific properties and exhaustively searches the tree of possible executions. We differ in that we operate at the bit level and we apply reduction techniques that allow backtracking algorithms to run faster as they operate on a smaller state space.

The work of Xie et al [32] translates software artifacts into equivalent semantics that are model-checkable. It applies compositional rules to the translated system to build its formal semantics in the context of message passing systems. We differ in that we use a specific program counter based semantics with a finitization rule to translate the software artifacts to an AIG, a model checkable formalization, where reductions, including compositional ones, can be used.
8 CONCLUSION

We presented PS\{Q\} that takes a program and a pair of specifications, translates it into an AIG circuit, reduces the circuit using the ABC synthesis reduction techniques, and then check the circuit for correctness using the ABC verification techniques. PS\{Q\} scales to bounds larger than that possible with existing tools, and solves verification tasks from the software verification competition benchmarks that leading tools at the competition did not solve within the specified timeout. In the future, we plan to extend PS\{Q\} to verify concurrent programs using several program counters to represent multi-threaded executions. We also plan to integrate PS\{Q\} with existing frameworks that benefit from word level optimizations and techniques such as CPAChecker to leverage both word level and bit level techniques as well as cover an extended syntax set through existing front ends.

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