Stochastic Computing Implemented by Skyrmionic Logic Devices

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Abstract

Magnetic skyrmions, topologically non-trivial spin textures, have been considered as promising information carriers in future electronic devices because of their nanoscale size, low depinning current density and high motion velocity. Despite the broad interests in skyrmion racetrack memory, researchers have been recently exploiting logic functions enabled by using the particle-like behaviors of skyrmions. These functions can be applied to unconventional computing, such as stochastic computing (SC), which treats data as probabilities and is superior to binary computing due to its simplicity of logic operations. In this work, we demonstrate SC implemented by skyrmionic logic devices. We propose a skyrmionic AND-OR logic device as a multiplier in the stochastic domain and two skyrmionic multiplexers (MUXs) as stochastic adders. With the assistance of voltage controlled magnetic anisotropy (VCMA) effect, precise control of skyrmions collision is not required in the skyrmionic AND-OR logic device, thus high thermal stability can be achieved. In the two MUXs, skyrmions are driven by Zhang-Li torque or spin orbit torque (SOT). Particularly, we can flexibly regulate the
skyrmion motion by VCMA effect or voltage controlled Dzyaloshinskii-Moriya Interaction (VCDMI) effect in the SOT-driven case. In our design, an 8-bit stochastic multiplier and an adder are further verified by micromagnetic simulations, which are competitive in terms of time efficiency and energy cost in comparison with typical CMOS based stochastic circuits. Our work opens up a new route to implement SC using skyrmionic logic devices.

I. INTRODUCTION

Magnetic skyrmions are topologically stable chiral structures, which are generated at the B20-type bulk materials or ultra-thin ferromagnetic (FM) layers favored by Dzyaloshinskii-Moriya Interaction (DMI) [1-6]. Due to their small size, high motion velocity and low depinning current density, skyrmions have been considered as promising carriers to transfer information in future electronic devices [7-10]. Over the past years, much effort has been devoted in developing skyrmion based racetrack memory [11-16], which requires no mechanical parts and shows great potential in advanced high-density storage applications. Moreover, by exploiting the particle-like behaviors of skyrmions, logic device concepts with high operation speed and low power consumption have also been proposed.

One of the most essential application of skyrmionic logic device is to support stochastic computing (SC), which can be realized by AND and multiplexer (MUX) logic operations. SC is an unconventional computing method that treats data as probabilities [17-19]. A N-bit stochastic number (SN) bit-stream with X 1s denotes a probability of \( P = X/N \), indicating the probability of observing bit 1 at a bit-stream. SC has been applied in the massively parallel computing system for its good tolerance to soft errors as well as high operation speed [20]. Besides, SN and X are flexible, which brings great convenience to its applications. To date, SC has been typically implemented in CMOS based stochastic circuits, which suffers from the challenges of power consumption and area cost [21-22]. Skyrmionic logic devices emerge as a solution to these issues. However, the existing proposals of skyrmionic AND logic
devices encounter low room temperature stability due to the narrow width of the racetrack and the requirement to precisely control skyrmions collision to execute logic operations [8, 23]. In addition, no skyrmionic MUX has been proposed yet.

In this work, we propose a skyrmionic AND-OR logic device and two types of skyrmionic MUXs regarding the skyrmions motion manner to implement SC. In the skyrmionic AND-OR logic device, which acts as a stochastic multiplier [24] in SC, skyrmions are driven by spin orbit torque (SOT) [25-27] and guided by voltage controlled magnetic anisotropy (VCMA) effect [28-30]. Therefore, it is not necessary to accurately control skyrmions collision to execute logic operations and this device can tolerate the thermal diffusion under $T = 250 \text{ K}$. In the skyrmionic MUXs operating as a stochastic adder [24], skyrmions can be driven by Zhang-Li torque or SOT. VCMA effect or voltage controlled DMI (VCDMI) effect [31] is used to dynamically modify the energy landscape to regulate the skyrmion motion in such devices. Based on the above single-bit logic device, 8-bit SN stochastic multiplier and stochastic adder are further confirmed by micromagnetic simulations. Subsequently, the performance of the proposed skyrmionic logic devices is analyzed, which shows broad prospects on implementing SC compared to typical CMOS based stochastic circuits.

**II. Skyrmionic AND-OR Logic Device**

In the proposed structure shown in Fig. 1(a), the skyrmionic AND-OR device is mainly composed of three parts, including heavy metal (HM) layer, ferromagnetic (FM) layer and two electrode gates. The HM layer, which is beneath the FM layer (not shown in the figure), is used for the flow of driving current to drive skyrmion from the left side to the right side by the spin Hall effect [32]. We apply positive voltages on electrode gate 1 ($V_{g1}$) and 2 ($V_{g2}$) (see Fig.1(b)), increasing the potential energy of the FM layer beneath $V_{g1}$ and $V_{g2}$ to guide the skyrmion motion. The effect of a voltage $V$ on the perpendicular magnetic anisotropy (PMA) [33] can be calculated by the equation $K_g = K_u + \zeta \cdot V / (d \cdot h)$, where the VCMA coefficient $\zeta$ is set as $48 \text{ fJ} \cdot \text{V}^{-1} \cdot \text{m}^{-1}$ according to previous reports [29], $d$ denotes the thickness of the insulator layer between electrode gates and the FM layer, and $h$ is the thickness of the FM layer, which are both set as 1
nm in our simulations. Precisely, if a +2 V voltage is applied on one electrode gate, the PMA of the FM layer beneath it will increase from 0.8 MJ·m$^{-3}$ to 0.896 MJ·m$^{-3}$, creating an energy barrier blocking the skyrmions from crossing this region.

![Diagram](image)

**Fig. 1** Skyrmionic AND-OR logic device at $T = 0$ K. (a) Device structure with two input lanes and two output lanes. The two electrode gates ($V_{g1}$, $V_{g2}$) are designed to modulate the skyrmion motion through the VCMA effect. (b) Profile of the SOT current density ($J_{SOT}$) and applied positive voltages to achieve the device function. (c-e) Three cases of the inputs and their corresponding simulation processes and outputs. In the snapshots of micromagnetic simulations, red region represents spin up ($m_z = +1$), blue represents spin down ($m_z = -1$) and white represents spin that horizontal to the plane ($m_z = 0$).

Fig. 1(b) shows the profile of the SOT current density ($J_{SOT}$) and the electrode voltages to achieve the device function. A voltage of +2V is dynamically applied on $V_{g1}$ and $V_{g2}$ to guide the skyrmions motion. Fig.1(c-e) demonstrates the top-viewed
simulation snapshots under three different inputs. The data “1” or “0” is encoded by the presence or absence (in FM background) of a skyrmion. In the circumstance with only one skyrmion input, this skyrmion will enter OR lane and be blocked at a position near \( V_{g2} \) under the joint effect of VCMA, \( J_{SOT} = 6 \text{ MA} \cdot \text{cm}^{-2} \) for 3 ns and repulsion from the edge [34-35]. After the positive voltage on \( V_{g2} \) is removed, the skyrmion finally outputs from the OR lane. Therefore, the OR and AND lane generate an output of “1” and “0”, respectively. In the case with two skyrmion inputs, the first skyrmion (from \( \text{In}_0 \) ) stops near \( V_{g2} \), similar to the aforementioned behavior. The subsequent skyrmion (from \( \text{In}_1 \) ) is then blocked because of the repulsion from the first skyrmion and the energy potential caused by \( V_{g1} \). At \( t = 3 \text{ ns} \), the voltage on \( V_{g1} \) is set to 0 V and \( J_{SOT} \) increases to 10 MA \cdot cm^{-2}. Thus, the subsequent skyrmion will be driven to the AND lane by a combined effect of skyrmion Hall Effect [36-40], skyrmion-skyrmion repulsion and skyrmion-edge repulsion while the first skyrmion moves out from OR lane after the voltage on \( V_{g2} \) returns to 0. In this case, both OR and AND lane give rise to an output of data “1”. Obviously, AND-OR logic function is realized in our proposed device. Note that during these operations, it is not necessary to precisely control the skyrmion-skyrmion collision. However, in the previous proposals [8, 23], this is required to realize logic function, which will suffer from instability in the presence of thermal effect and pinning. We further verify the function of the proposed AND-OR Logic device at \( T = 250 \text{ K} \) (See Appendix B for details), indicating the higher thermal stability of our device.

Moreover, we designed an 8-bit stochastic multiplier, using the proposed single-bit skyrmionic logic AND-OR device as the stochastic multiplier cell. Fig. 2(a) shows the schematic of multiplication computation of \( 4/8 \times 6/8 \) implemented by an AND logic gate, which can be physically achieved with our proposed skyrmionic device, as exhibited in Fig. 2(b). The AND function is implemented using the above single-bit skyrmionic logic AND-OR device while the inputs and outputs can be stored in the corresponding elongated lanes. Notches at the lanes are used to synchronize the input and output skyrmions, and to divide each lane into 8 regions (yellow regions in Fig. 2(b)). Through periodically increasing the current to \( J_{SOT} = 20 \text{ MA} \cdot \text{cm}^{-2} \) for 0.6 ns, skyrmions can move to the region of the next data bit [23]. Otherwise, skyrmions will
be blocked in their original area. The operation timing diagram of a single-bit AND-OR logic operation in one cycle is shown in Fig. 2(c). Compared to the timing diagram in Fig. 1(b), an additional 0.6 ns wide high current pulse is provided every 19.6 ns to synchronize the skyrmions, which means that the whole operation time for 8-bit multiplication computing is about 156.8 ns. In our simulations, input skyrmions are initialized at the left racetracks. There are four and six skyrmions distributed in the two 8-bit input lanes, denoting two probabilities of $P_1 = 4/8$ and $P_0 = 6/8$, respectively. After eight cycles of single-bit operation, three skyrmions output from the AND lane, as shown in Fig. 2(d), illustrating an output probability of $P_{\text{out}} = 3/8$ and the capableness of our device to perform stochastic multiplication.

FIG. 2 Skyrmionic AND-OR logic device used as an 8-bit stochastic multiplier. (a) Schematic of an exact multiplication computation of $4/8 \times 6/8 = 3/8$. A logic AND gate is required during the operation. (b) Schematic of the proposed 8-bit skyrmionic stochastic multiplier. Notches are used to divide each lane into 8 regions and to synchronize the motion of skyrmions. (c) Profile of driving current density ($J_{\text{SOT}}$) and electrode voltages in a single-bit operation cycle. (d) Snapshots of the magnetization configuration of the 8-bit stochastic multiplier at selected times. At $t = 0$ ns, the skyrmions distributed in the two input lanes represent probabilities $P_1 = 4/8$ and $P_0 = 6/8$, respectively. After 168 ns, AND lane will output the binary sequence of “0, 0, 1, 0, 1, 0, 1”, i.e., a probability of $P_{\text{out}} = 3/8$, which denotes the multiplication result of two inputs.
III. Skyrmionic MUXs

Addition operation in SC can be performed by a MUX [24], where two input bit-streams (In₁, In₀) are selected by a select signal S with a probability of 0.5, thus the output bit-stream owns a probability that is half sum of the two inputs. Considering the feature of a MUX and the particle-like behaviors of skyrmions, we propose two types of skyrmionic MUXs regarding the skyrmion motion manner.

Fig. 3(a) shows the first scheme to implement the MUX logic, which is based on the deflection of skyrmions at an interface between regions with different DMI. The DMI constant $D_1$ of the left side is set as 3.5 mJ·m$^{-2}$ while $D_2$ of the right plane varies from 3.35 to 3.65 mJ·m$^{-2}$. The skyrmion deflection direction depends on the relative magnitude of $D_1$ and $D_2$. Specifically, in our settings, if $D_2 > D_1$, skyrmions will be deflected along $+y$ direction. Therefore, skyrmions from In₀ will enter the OUT lane while skyrmions from In₁ will output from the $C_1$ lane, which means data from In₀ is selected. In contrast, if $D_2 < D_1$, skyrmions from In₁ will enter the OUT lane, while skyrmion from In₀ will crush at the lower edge. By regulating $D_2$ through VCDMI effect according to a select signal S, MUX logic can be implemented in our device. Note that when skyrmions cross the interface where the DMI changes, the applied in-plane polarized current (CIP) $J_{\text{STT}}$ maintains $-15$ MA·cm$^{-2}$ (see Fig. 3(b)). If the current density is too high, skyrmions will quickly go through the interface, leading to a small displacement along $y$ direction, not enough to realize the function.
FIG. 3 Skyrmionic MUX driven by the Zhang-Li torque. (a) Schematic of the proposed device, where the DMIs in the left panel ($D_1$) and right panel ($D_2$) are different. There are two input lanes ($\text{In}_0$, $\text{In}_1$), one output lane (OUT) to export the selected data. Trajectories of skyrmions are indicated by the black and red symbols when $D_2 = 3.35$ or 3.65 mJ·m$^{-2}$ while $D_1$ is fixed as 3.5 mJ·m$^{-2}$. (b) Profile of the driving in-plane polarized current $J_{\text{STT}}$. Note that a damping constant $\alpha = 0.1$ is used in the simulations of (a) to obtain large enough skyrmion deflection.

However, this scheme has several shortcomings. First, the stability and the power efficiency of this device will be affected by the crush of skyrmions. Second, deflection toward $-y$ direction at the interface can only be achieved when skyrmions are driven by the Zhang-Li torque (See Appendix C for the simulation results of SOT-driven case and Discussion for explanation), which consumes more energy and time than the SOT-driven case. In addition, the skyrmion displacement along the $y$ direction is inversely proportional to the damping constant [41], which indicates that the damping constant should be relatively low ($\alpha = 0.1$ is used in this simulation) to enable an enough displacement. However, in the widely studied Pt/Co system, damping is usually larger than 0.1 [42].

Therefore, we propose another scheme of skyrmionic MUX where skyrmions are driven by SOT. There are two copy lanes ($C_1$, $C_0$) outputting the data that is not selected by S. As shown in Fig. 4(a), an oblique interface is introduced to guide the skyrmion motion. Three electrode gates ($V_{G1}$, $V_{G2}$, $V_{G3}$) are used to lower the DMI value of the FM layer beneath the electrode gates through the VCDMI effect [31]. $V_{G1}$ and $V_{G3}$ are always applied with the same voltage, which are used to select the input skyrmion from $\text{In}_1$. By contrast, a voltage different from $V_{G1}$ and $V_{G3}$ is applied on $V_{G2}$ to select skyrmion from $\text{In}_0$. The select signal S can be produced by a random number generator (RNG) [43-45], where the probability of “1” is 0.5. When the random number from S is 0, $D_2$ will decrease to 3.2 mJ·m$^{-2}$, creating a high energy barrier to guide skyrmions from $\text{In}_0$ to enter the OUT lane. In the meantime, $D_1$ and $D_3$ remain unchanged (default value $D = 3.5$ mJ·m$^{-2}$). Therefore, skyrmions from $\text{In}_1$ will output from $C_1$. When the random number is 1, only $V_{G1}$ and $V_{G3}$ are selected, lowering $D_1$ and $D_3$ to 3.2 mJ·m$^{-2}$ simultaneously. Therefore, skyrmions from $\text{In}_1$ eventually move to the OUT lane while
skyrmions from In₀ are guided by \( V_{G3} \) and enter the \( C₀ \) lane. The trajectories of skyrmions under different situations are explicitly shown in Fig. 4(a).

During the operation, the 0.3 mJ·m\(^{-2}\) difference of DMI can sustain a max current density of \( J_{SOT} = 6.1 \) MA·cm\(^{-2}\). If the current is higher, skyrmions from In₁ will go through the \( V_{G1} \) region and enter the \( C₁ \) lane, leading to the wrong logic output. Except for VCDMI, VCMA effect can also be used to change the local potential energy. Fig. 4(b) shows the schematic of a skyrmionic MUX using the VCMA effect. Like Fig. 4(a), three voltage gates are placed to modify the energy landscape in the device. In our simulations, we apply a +1 V voltage on the electrode gates to increase the local PMA energy density from 0.8 MJ·m\(^{-3}\) to 0.848 MJ·m\(^{-3}\). In this case, the max current density is \( J_{SOT} = 3.0 \) MA·cm\(^{-2}\), otherwise skyrmions will enter wrong lanes. Materials with higher VCMA coefficient or higher voltages can be used to improve the device speed.

Based on the single-bit MUX device using the VCMA effect, we further design an 8-bit stochastic adder. Fig. 5(a) is the schematic of an exact addition computation of \( 1/2 \cdot (7/8 + 3/8) \) performed by a MUX. The structure of the proposed 8-bit skyrmionic stochastic adder is shown in Fig. 5(b). Following the timing diagram in Fig. 5(c), the proposed skyrmionic MUX can select the skyrmion from In₁ or In₀ depending on the

![Fig. 4](image-url) - Skyrmionic MUXs driven by the SOT. Schematic of the proposed device, where the energy landscape is dynamically changed through (a) VCDMI effect (b) VCMA effect. Three electrode gates \( (V_{G1}, V_{G2}, V_{G3}) \) are introduced to guide the skyrmion motion. Trajectories of the skyrmions are indicated by the black and red lines when selecting data from different lanes. \( J_{SOT} \) applied in (a) and (b) is 6.1 MA·cm\(^{-2}\) and 4.0 MA·cm\(^{-2}\), respectively.
sequence $S$ produced by a RNG. Like the 8-bit stochastic multiplier, a high current $J_{\text{SOT}} = 10 \text{ MA} \cdot \text{cm}^{-2}$ for 2.2 ns is used every 17.2 ns to enable skyrmions cross the notches and to synchronize the skyrmions. Therefore, the whole duration to complete the 8-bit MUX logic operation is 137.6 ns. Fig. 5(d) shows the snapshots of the magnetization configuration at selected times. We can find that there are five skyrmions on the 8-bit OUT lane, denoting a probability of $P_{\text{out}} = 5/8$, which is exactly the half sum of the two input probabilities of $P_1 = 7/8$ and $P_0 = 3/8$.

**FIG. 5** Skyrmionic MUX used as an 8-bit stochastic adder. (a) Schematic of an exact addition computation of $1/2 \cdot (7/8 + 3/8) = 5/8$ implemented by a MUX. (b) Schematic of the proposed 8-bit stochastic adder. (c) Profile of the driving current density ($J_{\text{SOT}}$) and the applied voltages on three electrode gates ($V_{G1}$, $V_{G2}$, $V_{G3}$) in a single-bit operation cycle. (d) Snapshots of the magnetization configuration of the 8-bit stochastic multiplier at selected times. At $t = 0$ ns, the skyrmions distributed in the two input lanes represent probabilities $P_1 = 7/8$ and $P_0 = 3/8$, respectively. After 137 ns, the OUT lane will output the binary sequence of “1, 0, 1, 0, 0, 1, 1”, i.e., a probability of $P_{\text{out}} = 5/8$, which denotes the half sum result of two inputs.
IV. Discussion
A. Skyrmion dynamics at an interface where DMI changes

To understand the skyrmion dynamics in the two proposed MUXs, we investigate the trajectory of skyrmions driven by the Zhang-Li torque or SOT based on the Thiele equation which assumes that skyrmions are rigid during the steady motion.

We first analyze the skyrmion dynamics driven by the Zhang-Li torque. The Thiele equation for this case reads [46]:

\[ G \times (v - u) - \alpha D v + F_1 = 0 \]  

(1)

Here, \( G = (0, 0, G) \) is the gyromagnetic coupling vector, where \( G = \frac{M_s t_F}{\gamma} 4\pi Q \) with saturation magnetization \( M_s \), FM layer thickness \( t_F \), gyromagnetic ratio \( \gamma \), and skyrmion number \( Q = \frac{-1}{4\pi} \oint m \cdot (\frac{\partial m}{\partial x} \times \frac{\partial m}{\partial y}) \ dS \); \( v = (v_x, v_y, 0) \) is skyrmion motion velocity; \( u \) is a vector along the electron motion direction with amplitude \( u \); \( \alpha \) is the damping constant; \( D = \frac{M_s t_F}{\gamma} \oint (\frac{\partial m}{\partial x})^2 \ dS \) is the dissipative force; \( F_1 = -\nabla V(\mathbf{r}) \) is the force induced by the interface where DMI changes with \( V(\mathbf{r}) \) denoting the system energy when a skyrmion locates at position \( \mathbf{r} \). Assume that we apply an in-plane current along \(-x\) direction and the interface is exactly along \( y \) direction as shown in Fig. 3(a), the solution to Eq. (1) is given by:

\[
\begin{align*}
\nu_x &= \frac{\alpha D F_1 + G^2 u}{G^2 + (\alpha D)^2} \\
\nu_y &= \frac{G (F_1 - \alpha D u)}{G^2 + (\alpha D)^2}
\end{align*}
\]  

(2)

where \( F_1 \) denotes the magnitude of the force \( F_1 \).

If \( D_1 = D_2 \) or skyrmions are far away enough from the interface, we can set \( F_1 = 0 \) in Eq. (2). As a consequence, we obtain \( \nu_x = \frac{G^2 u}{G^2 + (\alpha D)^2} \) and \( \nu_y = -\frac{\alpha D G u}{G^2 + (\alpha D)^2} \). This illustrates that skyrmions will gain a velocity along \(+x\) direction in this case, which is the feature of the Zhang-Li torque driven domain wall motion dynamics. In contrast, whether skyrmions move toward \(+y\) or \(-y\) direction depends on the sign of skyrmion number \( Q \). In our simulations, we get \( Q = 1 \) because the magnetization of the background FM layer points along \(+z\) direction. Therefore, \( \nu_y \) is negative, which agrees
with the trajectories as shown in Fig. 3(a). Further, the skyrmion Hall angle $\theta_{sk}$, which describes the deviation of skyrmions from $x$ direction, is given by

$$\theta_{sk} = \tan \left( \frac{v_y}{v_x} \right) = -\tan \left( \frac{oD}{G} \right).$$

If the skyrmion radius $R$ is larger than the domain wall width $\Delta$, $\theta_{sk}$ can be well simplified to $-\tan \left( \frac{oR}{2\Delta} \right)$ [47]. Taking the parameters used in Fig. 3(a), $\theta_{sk}$ is estimated as $-16^\circ$, corresponding well to the simulation results. When $D_1 \neq D_2$ and skyrmions are near the interface, $F_i$ cannot be left out in Eq. (2). As illustrated in Fig. 7(c), $F_i$ is positive if $D_1 < D_2$ and vice versa. From the expression of $v_y$, we can see that the skyrmion deflection can be changed by varying the magnitude of $F_i$ and $\alpha Du$. Once $D_1 < D_2$ and $F_i > \alpha Du$, skyrmions will move toward $+y$ direction. Otherwise, skyrmions still bend over $-y$ direction. The first proposed MUX is exactly based on this property.

In contrast, the Thiele equation for the SOT-driven case reads [32]:

$$G \times v - \alpha Dv + F_{SHE} + F_i = 0 \quad (3)$$

where $F_{SHE} = F_{SHE}\hat{\sigma}$ is the force induced by the SOT with magnitude $F_{SHE}$, the sign of which depends on the spin polarization direction $\sigma$. By solving Eq. (3), we can find

$$\begin{align*}
v_x &= \frac{\alpha D(F_{SHE} + F_i)}{G^2 + (\alpha D)^2} \\
v_y &= \frac{G(F_{SHE} + F_i)}{G^2 + (\alpha D)^2} \quad (4)
\end{align*}$$

If $D_1 < D_2$, $F_{SHE}$ and $F_i$ are both positive, thus the skyrmion Hall angle $\theta_{sk} = \tan \left( \frac{v_y}{v_x} \right) = \tan \left( \frac{G}{\alpha D} \right)$, which means that skyrmions can only bend toward $+y$ direction when approaching the interface from In$_0$ or In$_1$. According to the expression of $\theta_{sk}$, the skyrmion Hall effect should be remarkable in the SOT-driven case, agreeing well with the trajectories in Fig. 4(a). If $D_1 \geq D_2$, $F_{SHE} + F_i = 0$ can be achieved when skyrmions gradually approach the interface. Thereafter skyrmions remain static, as indicated by Fig. 7(a). Therefore, in the MUX displayed in Fig. 3(a) where the interface is along $y$ direction, only Zhang-Li torque can be used to realize the MUX function.

If an oblique interface is introduced, as is the case in Fig. 4(a), $F_i$ can be expressed as $F_i = (F_{ix}, F_{iy}, 0)$. Therefore, the solution to Eq. (3) becomes:
\[
\begin{align*}
\nu_x &= \frac{\alpha D (F_{\text{SHE}} + F_{ix}) - GF_{iy}}{G^2 + (\alpha D)^2} \\
\nu_y &= \frac{G (F_{\text{SHE}} + F_{ix}) + \alpha DF_{iy}}{G^2 + (\alpha D)^2}
\end{align*}
\]

(5)

To guide skyrmions move along the interface, we have \(F_{\text{SHE}} > 0, F_{ix} < 0 \) and \(F_{iy} < 0\), i.e., \(D_1 > D_2\). Assume that the interface encloses angle \(\delta\) with the \(-y\) direction, we have

\[ k = \tan(\delta) = -\frac{\nu_x}{\nu_y} = \frac{F_{iy}}{F_{ix}}. \]

Subsequently, we can obtain:

\[ F_i = -\frac{\alpha D + kG}{\alpha D \sqrt{1 + \delta^2}} F_{\text{SHE}} \]  

(6)

Therefore, we can guide skyrmions motion along a designed interface when a proper SOT current is applied. Since \(F_i\) can also be generated at the interface where PMA changes, VCMA effect can be used to realize similar function, as shown in Fig. 4(b).

Note that if the applied SOT current is too high, \(F_i\) provided by the interface may fail to satisfy Eq. (6). Under this circumstance, skyrmions can go through the electrode gated regions, resulting in wrong outputs.

**B. Performance evaluation of SC implemented by skyrmionic logic devices**

As shown above, we have successfully implemented SC by the skyrmionic logic devices. Despite the non-volatile advantage of skyrmion based devices, it is also necessary to evaluate the performance in terms of energy consumption, delay and area.

For the 8-bit stochastic multiplier, the energy consumption is about 1.264 pJ at \(T = 0\) K (See Appendix D for energy calculation method), which is only about 5.5% of the CMOS based stochastic circuits [21]. In addition, the delay of our proposed skyrmionic stochastic multiplier is proportional to the SN, thus the whole delay of a \(N\)-bit SN stochastic multiplier is \(N \times 19.6\) ns. In contrast, the delay of the CMOS based stochastic circuits is nonlinear, growing exponentially as the SN increases [21]. Consequently, when \(SN > 12\), the delay of skyrmionic stochastic multiplier will become lower than that of CMOS based stochastic circuits, and the delay of skyrmionic stochastic multiplier will be extremely lower as the SN continually increases [21]. For example, when \(SN = 20\), the delay of skyrmionic stochastic multiplier will be only 0.37% of that of the CMOS based stochastic circuits. In the meantime, the 8-bit stochastic adder
consumes about 1.224 pJ for 8-bit addition operation in about 137.6 ns, occupying about 0.6 μm² for one device, which is competitive in terms of time efficiency and energy cost with typical CMOS based stochastic circuits. Considering also the higher thermal stability, the proposed skyrmionic logic devices demonstrate broad prospects as advanced alternatives to implement SC.

V. Conclusion

In this work, we propose a skyrmionic AND-OR logic device and two types of skyrmionic MUXs to implement SC. Thanks to the energy landscape designed by the VCMA effect or VCDMI effect, precise control of skyrmion-skyrmion collision is not required in our devices, thus enabling higher thermal stability. Based on the single-bit device, we further demonstrate an 8-bit stochastic multiplier and adder. Performance evaluation shows that our proposed skyrmionic logic devices outperform typical CMOS based circuits to execute SC in terms of energy consumption, time delay and area. Our work unfolds the great potential of skyrmionic logic devices to implement SC.
Appendix A: Simulation Methods

Micromagnetic simulations were performed by utilizing the GPU-accelerated simulation software mumax3 [48]. The dynamics at each site are depicted by the following Landau-Lifshitz-Gilbert (LLG) equation [4, 32]:

$$\frac{\partial \mathbf{m}}{\partial t} = -\gamma \mu_0 (\mathbf{m} \times \mathbf{H}_{\text{eff}}) + \alpha (\mathbf{m} \times \frac{\partial \mathbf{m}}{\partial t}) + \tau_{\text{SOT}} + \tau_{\text{CIP}}$$

where $H_{\text{eff}}$ is the effective field, including the contributions from the anisotropy field, exchange field, DMI field, demagnetization field and thermal field (when $T \neq 0$ K). $\mathbf{m} = \frac{M}{|M_s|}$ is the reduced magnetization with $M_s$ the saturation magnetization, $\alpha$ is the damping constant, $\gamma$ is the gyromagnetic ratio and $\mu_0$ is the vacuum magnetic permeability. $\tau_{\text{SOT}} = \gamma J_{\text{SOT}} \theta_{\text{SH}} \hbar \frac{e d}{2} M_s (\mathbf{m} \times \mathbf{\sigma} \times \mathbf{m})$ denotes the SOT exerted on the magnetization when applying a SOT current $J_{\text{SOT}}$ with spin polarization direction $\mathbf{\sigma}$, spin Hall angle $\theta_{\text{SH}}$, elementary charge $e$ and FM layer thickness $d$ and reduced Plank constant $\hbar$ [32, 49]. $\tau_{\text{CIP}} = u(\mathbf{m} \times \frac{\partial \mathbf{m}}{\partial x} \times \mathbf{m})$ is the exerted Zhang-Li torque when an in-plane polarized current is applied, where $u = \gamma J_{\text{STT}} \frac{P \hbar}{2e} M_s$ with current density $J_{\text{STT}}$ and spin polarization $P$ [32, 50].

Unless specified, the following material parameters are adopted in our simulations: exchange stiffness $A = 15$ pJ·m$^{-1}$, Gilbert damping $\alpha = 0.3$, saturation magnetization $M_s = 580$ kA·m$^{-1}$, spin polarization $P = 0.4$, spin Hall angle $\theta_{\text{SH}} = 0.4$, PMA constant of the FM layer $K_u = 0.8$ MJ·m$^{-3}$, DMI constant $D = 3.5$ mJ·m$^{-2}$ and VCMA coefficient $\xi = 48$ fJ·V$^{-1}$·m$^{-1}$ [7, 29, 49]. The simulation area is divided into a cubic grid of 2 nm × 2nm × 1nm.
Appendix B: Skyrmionic AND-OR functions performed at $T = 250$ K

FIG. 6 Skyrmionic AND-OR logic device performed at $T = 250$ K: (a) the device structure is larger than the device in Fig.1(a). (b) Profile of $J_{\text{SOT}}$ and electrode voltages. (c-e) Three cases of inputs and their corresponding simulation process and results.

We enlarge the area of the device and adjust timing diagram (see Fig. 6(a-b)) to enable the fluctuation of the skyrmions because of the high thermal stability of skyrmions in a wider racetrack [51]. Fig. 6(c-e) shows the simulation results with different inputs. The volume of skyrmion dramatically increases and fluctuating a lot at $T = 250$ K, which limits the current density applied in driving the skyrmions [52]. Basically, $J_{\text{SOT}} = 4.2 \text{ MA} \cdot \text{cm}^{-2}$ is applied to drive skyrmion motion but a lower current is used ($J_{\text{SOT}} = 2.9 \text{ MA} \cdot \text{cm}^{-2}$) when the second skyrmion moves to the AND lane. This is because the second skyrmion is more likely to crush at the edge while it fluctuates at $T = 250$ K compared to the situation at $T = 0$ K. The operation time becomes longer because of the larger size of the device as well as the lower driving current. But still, the AND-OR function can be achieved, indicating the high thermal stability of our device.
Appendix C: Simulation results of SOT-driven skyrmion motion at the interface where DMI changes

FIG. 7 (a-b) Trajectories of a SOT-driven skyrmion at different $D_2$ when an $y$-direction or oblique interface is introduced. $D_1 = 3.5 \text{ mJ}\cdot\text{m}^{-2}$ and $J_{\text{SOT}} = 4 \text{ MA}\cdot\text{cm}^2$. (c) Effect of DMI on the energy of a nanotrack system. DMI strength increases from 3.2 $\text{mJ}\cdot\text{m}^{-2}$ at the left side to 3.8 $\text{mJ}\cdot\text{m}^{-2}$ at the right side, generating a force to drive the skyrmion along $+x$ direction. At each position, the energy of the system is recorded.

We investigate SOT-driven skyrmion motion at different interfaces where DMI changes. A constant SOT current $J_{\text{SOT}} = 4 \text{ MA}\cdot\text{cm}^2$ is applied along $+x$ direction to drive skyrmion motion. As shown in Fig. 7(a) where the interface is exactly along $y$ direction, skyrmion deflection is along $+y$ direction when $D_1 \leq D_2$. However, skyrmions will stop at the interface when $D_1 > D_2$. In contrast, in Fig. 7(b), we find that an oblique interface can guide skyrmions along $-y$ direction, which can be utilized to perform the MUX function. We further evaluate the effect of different DMI on the potential energy. We initialize a skyrmion at the left side of the nanotrack shown in Fig. 7(c). Along this nanotrack, the DMI strength $D$ increases from 3.2 $\text{mJ}\cdot\text{m}^{-2}$ at the left side to 3.8 $\text{mJ}\cdot\text{m}^{-2}$ at the right side. Due to the DMI gradient, the skyrmion will move freely to the right side and the energy is measured at each position. We can see that the potential energy in the region with a lower DMI is higher, which can be used to guide the motion of skyrmions. Besides, the energy difference between two regions is nearly proportional to the DMI difference. By enlarging the DMI difference between two adjacent regions, we can regulate the skyrmion in a more stable manner, and a higher current can be used to drive the skyrmion.
Appendix D: Energy Consumption Evaluation Method

Energy consumed to operate an 8-bit stochastic multiplication is equal to 8 times of a single-bit AND operation according to the discussion above. For a single-bit AND operation, the energy consumption $W$ for a constant SOT current $J$ is calculated by

$$W = J^2 \cdot S_{HM} \cdot \rho \cdot l \cdot T,$$

where $J$ is the current density flowing in the HM layer, $S_{HM}$ is the $y$-$z$ cross area of HM layer, $\rho$ is the resistivity of the HM layer [53], $l$ is the length of the HM layer in $x$ direction and $T$ is the time duration. According to the time diagram shown in Fig. 2(c), different current density $J_i$ ($i = 1, 2, 3, 4$) is applied for different time duration $T_i$. The corresponding parameters are listed in the TABLE I.

Therefore, the energy consumed for a single-bit operation is about 158 fJ, which indicates the total energy consumed for 8-bit AND operation is $8 \times 158 = 1264 \text{ fJ} = 1.264 \text{ pJ}$. Similarly, the total power consumption for 8-bit MUX operation is calculated to be 1.224 pJ.

| $J_i$ (MA·cm$^{-2}$) | $S_{HM}$ (nm$^2$) | $\rho$ (Ω·m) | $l$ (nm) | $T_i$ (ns) |
|---------------------|------------------|---------------|---------|----------|
| i = 1               | 10               | 480           | 1.8×10$^{-6}$ | 2400     | 3        |
| i = 2               | 20               | 480           | 1.8×10$^{-6}$ | 2400     | 0.6      |
| i = 3               | 4.5              | 480           | 1.8×10$^{-6}$ | 2400     | 11       |
| i = 4               | 10               | 480           | 1.8×10$^{-6}$ | 2400     | 5        |
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