Tartan: Accelerating Fully-Connected and Convolutional Layers in Deep Learning Networks by Exploiting Numerical Precision Variability

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Abstract—Tartan (TRT), a hardware accelerator for inference with Deep Neural Networks (DNNs), is presented and evaluated on Convolutional Neural Networks. TRT exploits the variable per layer precision requirements of DNNs to deliver execution time that is proportional to the precision \( p \) in bits used per layer for convolutional and fully-connected layers. Prior art has demonstrated an accelerator with the same execution performance only for convolutional layers\cite{1}, \cite{2}. Experiments on image classification CNNs show that on average across all networks studied, TRT outperforms a state-of-the-art bit-parallel accelerator \cite{3} by \( 1.90 \times \) without any loss in accuracy while it is 1.17\times more energy efficient. TRT requires no network retraining while it enables trading off accuracy for additional improvements in execution performance and energy efficiency. For example, if a 1\% relative loss in accuracy is acceptable, TRT is on average 2.04\times faster and 1.25\times more energy efficient than a conventional bit-parallel accelerator. A Tartan configuration that processes 2-bits at time, requires less area than the 1-bit configuration, improves efficiency to 1.24\times over the bit-parallel baseline while being 73\% faster for convolutional layers and 60\% faster for fully-connected layers is also presented.

I. INTRODUCTION

It is only recently that commodity computing hardware in the form of graphics processors delivered the performance necessary for practical, large scale Deep Neural Network applications \cite{4}. At the same time, the end of Dennard Scaling in semiconductor technology \cite{5} makes it difficult to deliver further advances in hardware performance using existing general purpose designs. It seems that further advances in DNN sophistication would have to rely mostly on algorithmic and in general innovations at the software level which can be helped by innovations in hardware design. Accordingly, hardware DNN accelerators have emerged. The DianNao accelerator family was the first to use a wide single-instruction single-data (SISD) architecture to process up to 4K operations in parallel on a single chip \cite{6}, \cite{3} outperforming graphics processors by two orders of magnitude. Development in hardware accelerators has since proceeded in two directions: either toward more general purpose accelerators that can support more machine learning algorithms while keeping performance mostly on par with DaDianNao (DaDN) \cite{3}, or toward further specialization on specific layers or classes of DNNs with the goal of outperforming DaDN in execution time and/or energy efficiency, e.g., \cite{7}, \cite{8}, \cite{1}, \cite{9}, \cite{10}. This work is along the second direction. While an as general purpose as possible DNN accelerator is desirable further improving performance and energy efficiency for specific machine learning algorithms will provide us with the additional experience that is needed for developing the next generation of more general purpose machine learning accelerators. Section VI reviews several other accelerator designs.

While DaDN’s functional units process 16-bit fixed-point values, DNNs exhibit varying precision requirements across and within layers, e.g., \cite{11}. Accordingly, it is possible to use shorter, per layer representations for activations and/or weights. However, with existing bit-parallel functional units doing so does not translate into a performance nor an energy advantage as the values are expanded into the native hardware precision inside the unit. Some designs opt to hardwire the whole network on-chip by using tailored datapaths per layer, e.g., \cite{12}. Such hardwired implementations are of limited appeal for many modern DNNs whose footprint ranges several 10s or 100s of megabytes of weights and activations. Accordingly, this work targets accelerators that can translate any precision reduction into performance and that do not require that the precisions are hardwired at implementation time.

This work presents Tartan (TRT), a massively parallel hardware accelerator whose execution time for fully-connected (FCLs) and convolutional (CVLs) layers scales with the precision \( p \) used to represent the input values. TRT uses hybrid bit-serial/bit-parallel functional units and exploits the abundant parallelism of typical DNN layers with the following goals: 1) exceeding DaDN’s execution time performance and energy efficiency, 2) maintaining the same activation and weight memory interface and wire counts, 3) maintaining wide, highly efficient accesses to weight and activation memories. Ideally, Tartan improves execution time over DaDN by \( \frac{16}{17}^p \) where \( p \) is the precision used for the activations in CVLs and for the activations and weights in FCLs. Every single bit of precision that can be eliminated ideally reduces execution time and increases energy efficiency. For example, decreasing precision from 13 to 12 bits in an FCL can ideally boost the performance improvement over DaDN DaDN to 33\% from 23\% respectively. TRT builds upon the Stripes (STR) accelerator \cite{2}, \cite{1} which improves execution time and energy efficiency on CVLs only. While STR matches the performance
of a bit-parallel accelerator on FCLs its energy efficiency suffers considerably. TRT improves performance and energy efficiency over a bit-parallel accelerator for both CVLs and FCLs.

This work evaluates TRT on a set of convolutional neural networks (CNNs) for image classification. On average TRT reduces inference time by 1.61×, 1.91× and 1.90× over DaDN for the fully-connected, the convolutional, and all layers respectively. Energy efficiency compared to DaDN with TRT is 1.06×, 1.18× and 1.17× respectively. By comparison, efficiency with STR compared to DaDN is 0.73×, 1.21× and 1.14× respectively. Additionally, TRT enables trading off accuracy for improving execution time and energy efficiency. For example, on average on FCLs, accepting a 1% loss in relative accuracy improves performance to 1.73× and energy efficiency to 1.14× compared to DaDN.

In detail this work makes the following contributions:

- Extends the STR accelerator offering performance improvements on FCLs. Not only STR does not improve performance on FCLs, but its energy efficiency suffers compared to DaDN.
- TRT incorporates cascading multiple serial inner-product (SIP) units improving utilization when the number of filters or the dimensions of the filters is not a multiple of the datapath lane count.
- It uses the methodology of Judd et al. [11] to determine per layer weight and activation precisions for the fully-connected layers of several modern image classification CNNs.
- It evaluates a configuration of TRT which trades off some of the performance improvement for enhancing energy and area efficiency. The evaluated configuration processes two activation bits per cycle and requires half the parallelism and the SIPs than the bit-serial TRT configuration.
- Reports energy efficiency and area measurements derived from a layout of the TRT accelerator demonstrating its benefits over the previously proposed STR and DaDN accelerators.

The rest of this document is organized as follows: Section III motivates TRT. Section [11] illustrates the key concepts behind TRT via an example. Section IV reviews the DaDN architecture and presents an equivalent Tartan configuration. Section V presents the experimental results. Section VI reviews related work and discusses the limitations of this study and the potential challenges with TRT. Section VII concludes.

II. Motivation

This section motivates TRT by showing that: 1) the precisions needed for the FCLs of several modern image classification CNNs are far below the fixed 16-bit precision used by DaDN, and 2) the energy efficiency of STR is below that of DaDN for FCLs. Combined these results motivate TRT which improves performance and energy efficiency for both FCLs and CVLs compared to DaDN.

A. Numerical Representation Requirements Analysis

The experiments of this section corroborate past results that the precisions needed vary per layer for several modern image classification CNNs and during inference. The section also shows that there is significant potential to improve performance if it were possible to exploit per layer precisions even for the FCLs. The per layer precision profiles presented here were found via the methodology of Judd et al. [11]. Caffe [13] was used to measure how reducing the precision of each FCL affects the network’s overall top-1 prediction accuracy over 5000 images. The network definitions and pre-trained synaptic weights are taken from the Caffe Model Zoo [14]. The networks are used as-is without retraining. Further reductions in precisions may be possible with retraining. As Section III will explain, TRT’s performance on an FCL layer L is bound by the maximum of the weight (P_w^L) and activation (P_a^L) precisions. Accordingly, precision exploration was limited to cases where both P_w^L and P_a^L are equal. The search procedure is a gradient descent where a given layer’s precision is iteratively decremented one bit at a time, until the network’s accuracy drops. For weights, the fixed-point numbers are set to represent values between -1 and +1. For activations, the number of fractional bits is fixed to a previously-determined value known not to hurt accuracy, as per Judd et al. [11]. While both activations and weights use the same number of bits, their precisions and ranges differ. For CVLs only the activation precision is adjusted as with the TRT design there is no benefit in adjusting the weight precisions as well. Weights remain at 16-bits for CVLs. While, reducing the weight precision for CVLs can reduce their memory footprint [15], an option we do not explore further in this work.

Table III reports the resulting per layer precisions separately for FCLs and CVLs. The ideal speedup columns report the performance improvement that would be possible if execution time could be reduced proportionally with precision compared to a 16-bit bit-parallel baseline. For the FCLs, the precisions required range from 8 to 10 bits and the potential for performance improvement is 1.64× on average and ranges from 1.63× to 1.66×. If a 1% relative reduction in accuracy is acceptable then the performance improvement potential increases to 1.75× on average and ranges from 1.63× to as much as 1.85×. Given that the precision variability for FCLs is relatively low (ranges from 8 to 11 bits) one may be tempted to conclude that a bit-parallel architecture with 11 bits may be an appropriate compromise. However, note that the precision variability is much larger for the CVLs (range is 5 to 13 bits) and thus performance with a fixed precision datapath would be far below the ideal. For example, speedup with a 13-bit datapath would be just 1.23× vs. the 2× that is be possible with an 8-bit precision. A key motivation for TRT is that its incremental cost over STR that already supports variable per layer precisions for CVLs is well justified given the benefits. Section IV quantifies this cost and the resulting performance and energy benefits.
### Table I

| Network   | Per Layer Activation Precision in Bits | Ideal Speedup | Fully-Connected layers | Per Layer Activation and Weight Precision in Bits | Ideal Speedup |
|-----------|----------------------------------------|---------------|------------------------|-------------------------------------------------|---------------|
|           | 100% Accuracy                          |               |                        | 99% Accuracy                                    |               |
| AlexNet   | 9-8-5-5-7                              | 2.38          | 10-9-9                 | 1.66                                            |
| VGG_S     | 7-8-9-7-9                              | 2.04          | 9-8-8-8                | 1.64                                            |
| VGG_M     | 7-7-7-7-7                              | 2.23          | 10-8-8-8               | 1.64                                            |
| VGG_19    | 12-12-12-11-12-10-11-11-13-12-13-13-13 | 1.35          | 10-9-9                 | 1.63                                            |

| AlexNet   | 9-7-4-5-5-7                            | 2.58          | 9-8-8-8                | 1.85                                            |
| VGG_S     | 7-8-9-7-9                              | 2.04          | 9-8-8-8                | 1.79                                            |
| VGG_M     | 6-8-7-7-7                              | 2.74          | 9-8-8-8                | 1.80                                            |
| VGG_19    | 9-9-9-8-12-10-10-12-13-11-12-13-13-13 | 1.57          | 10-9-8-8               | 1.63                                            |

**B. Energy Efficiency with Stripes**

*Stripes (STR)* uses hybrid bit-serial/bit-parallel inner-product units for processing activations and weights respectively exploiting the per layer precision variability of modern CNNs [1]. However, STR exploits precision reductions only for CVLs as it relies on weight reuse across multiple windows to maintain the width of the weight memory the same as in DaDN (there is no weight reuse in FCLs). Figure 1 reports the energy efficiency of STR over that of DaDN for FCLs (Section V-A details the experimental methodology). While performance is virtually identical to DaDN, energy efficiency is on average 0.73× compared to DaDN. This result combined with the reduced precision requirements of FCLs serves as motivation for extending STR to improve performance and energy efficiency compared to DaDN on both CVLs and FCLs.

### C. Motivation Summary

This section showed that: 1) The per layer precisions for FCLs on several modern CNNs for image classification vary significantly and exploiting them has the potential to improve performance by 1.64× on average. 2) STR that exploits variable precision requirements only for CVLs achieves only 0.73× the energy efficiency of a bit-parallel baseline. Accordingly, an architecture that would exploit precisions for FCLs as well as CVLs is worth investigating in hope that it will eliminate this energy efficiency deficit resulting in an accelerator that is higher performing and more energy efficient for both layer types. Combined FCLs and CVLs account for more than 99% of the execution time in DaDN.

### III. Tartan: A Simplified Example

This section illustrates at a high-level the way TRT operates by showing how it would process two purposely trivial cases: 1) a fully-connected layer with a single input activation producing two output activations, and 2) a convolutional layer with two input activations and one single-weight filter producing two output activations. The per layer calculations are:

**Fully – Connected:**

\[ f_1 = w_1 \times a \]
\[ c_1 = w \times a_1 \]

**Convolutional:**

\[ f_2 = w_2 \times a \]
\[ c_2 = w \times a_2 \]

Where \( f_1, f_2, c_1 \) and \( c_2 \) are output activations, \( w_1, w_2 \), and \( w \) are weights, and \( a_1, a_2 \) and \( a \) are input activations. For clarity all values are assumed to be represented in 2 bits of precision.

### A. Conventional Bit-Parallel Processing

Figure 2 shows a bit-parallel processing engine representative of DaDN. Every cycle, the engine can calculate the product of two 2-bit inputs, \( i \) (weight) and \( v \) (activation) and accumulate or store it into the output register \( OR \). Parts (b) and (c) of the figure show how this unit can calculate the example CVL over two cycles. In part (b) and during cycle 1, the unit accepts along the \( v \) input bits 0 and 1 of \( a_1 \) (noted as \( a_{1_0} \) and \( a_{11} \) respectively on the figure), and along the \( i \) input bits 0 and 1 of \( w \) and produces both bits of output \( c_1 \). Similarly, during cycle 2 (part (c)), the unit processes \( a_2 \) and \( w \) to produce \( c_2 \). In total, over two cycles, the engine produced two \( 2b \times 2b \) products. Processing the example FCL also takes two cycles: In the first cycle, \( w_1 \) and \( a \) produce \( f_1 \), and in the
second cycle $w_2$ and $a$ produce $f_2$. This process is not shown in the interest of space.

B. Tartan’s Approach

Figure 3 shows how a TRT-like engine would process the example CVL. Figure 3a shows the engine’s structure which comprises two subunits. The two subunits accept each one bit of an activation per cycle through inputs $v_0$ and $v_1$ respectively and as before, there is a common 2-bit weight input $(i_1, i_0)$. In total, the number of input bits is 4, the same as in the bit-parallel engine.

Each subunit contains three 2-bit registers: a shift-register AR, a parallel load register BR, and an parallel load output register OR. Each cycle each subunit can calculate the product of its own bit $v_i$ with the BR which can be written or accumulated into its OR. There is no bit-parallel multiplier since the subunits process a single activation bit per cycle. Instead, two AND gates, a shift-and-add functional unit, and OR form a shift-and-add multiplier/accumulator. Each AR can load a single bit per cycle from one of the $i$ wires, and BR can be parallel-loaded from AR or from the $i$ wires.

**Convolutional Layer:** Figure 3b through Figure 3d show how TRT processes the CVL. The figures abstract away the unit details showing only the register contents. As Figure 3b shows, during cycle 1, the $w$ synapse is loaded in parallel to the BRs of both subunits via the $i_1$ and $i_0$ inputs. During cycle 2, bits 0 of $a_1$ and of $a_2$ are sent via the $v_0$ and $v_1$ inputs respectively to the first and second subunit. The subunits calculate concurrently $a_1/0 \times w$ and $a_2/0 \times w$ and accumulate these results into their ORs. Finally, in cycle 3, bit 1 of $a_1$ and $a_2$ appear respectively on $v_0$ and $v_1$. The subunits calculate respectively $a_1/1 \times w$ and $a_2/1 \times w$ accumulating the final output activations $c_1$ and $c_2$ into their ORs.

In total, it took 3 cycles to process the layer. However, at the end of the third cycle, another $w$ could have been loaded into the BRs (the $i$ inputs are idle) allowing a new set of outputs to commence computation during cycle 4. That is, loading a new weight can be hidden during the processing of the current output activation for all but the first time. In the steady state, when the input activations are represented in two bits, this engine will be producing two $2b \times 2b$ terms every two cycles thus matching the bandwidth of the bit-parallel engine.

If the activations $a_1$ and $a_2$ could be represented in just one bit, then this engine would be producing two output activations per cycle, twice the bandwidth of the bit-parallel engine. The latter is incapable of exploiting the reduced precision for reducing execution time. In general, if the bit-parallel hardware was using $P_{\text{BASE}}$ bits to represent the activations while only $P_a^L$ bits were enough, TRT would outperform the bit-parallel engine by $P_{\text{BASE}} / P_a^L$.

**Fully-Connected Layer:** Figure 4 shows how a TRT-like unit would process the example FCL. As Figure 4a shows, in cycle 1, bit 1 of $w_1$ and of $w_2$ appear respectively on lines $i_1$ and $i_0$. The left subunit’s AR is connected to $i_1$ while the right subunit’s AR is connected to $i_0$. The ARs shift in the corresponding bits into their least significant bit sign-extending to the vacant position (shown as a 0 bit on the example). During cycle 2, as Figure 4b shows, bits 0 of $w_1$ and of $w_2$ appear on the respective $i$ lines and the respective ARs shift them in. At the end of the cycle, the left subunit’s AR contains the full 2-bit $w_1$ and the right subunit’s AR the full 2-bit $w_2$. In cycle 3, Figure 4c shows that each subunit copies the contents of AR into its BR. From the next cycle, calculating the products can now proceed similarly to what was done for the CVL. In this case, however, each BR contains a different weight whereas when processing the CVL in the previous section, all BRs held the same $w$ value. The shift capability of the ARs coupled with having each subunit connect to a different $i$ wire allowed TRT to load a different weight bit-serially over two cycles. Figure 4d and Figure 4e show cycles 4 and 5 respectively. During cycle 4, bit 0 of $a_1$ appears on both $v$ inputs and is multiplied with the BR in each subunit. In cycle 5, bit 1 of $a_1$ appears on both $v$ inputs and the subunits complete the calculation of $f_1$ and $f_2$. It takes two cycles to produce the two $2b \times 2b$ products once the correct inputs appear into the BRs.

While in our example no additional inputs nor outputs are shown, it would have been possible to overlap the loading of a new set of $w$ inputs into the ARs while processing the current weights stored into the BRs. That is the loading into ARs, copying into BRs, and the bit-serial multiplication of the BRs with the activations is a 3-stage pipeline where each stage can take multiple cycles. In general, assuming that both activations and weights are represented using 2 bits, this engine would match the performance of the bit-parallel engine in the steady state. When both set of inputs $i$ and $v$ can be represented with fewer bits (1 in this example) the engine would produce two terms per cycle, twice the bandwidth of the bit-parallel engine of the previous section.

**Summary:** In general, if $P_{\text{BASE}}$ is the precision of the bit-parallel engine, and $P_a^L$ and $P_w^L$ the precisions that can be used respectively for activations and weights for layer $L$, a TRT engine can ideally outperform an equivalent bit parallel engine by $P_{\text{BASE}} / P_a^L$ for CVLs, and by $P_{\text{BASE}} / \max(P_w^L, P_a^L)$ for FCLs. This example used the simplest TRT engine configuration. Since typical layers exhibit massive parallelism, TRT can be configured with many more subunits while exploiting weight reuse for CVLs and activation reuse for FCLs. The next section describes the baseline state-of-the-art DNNs accelerator and presents an equivalent TRT configuration.

IV. Tartan Architecture

This work presents TRT as a modification of the state-of-the-art DaDianNao accelerator. Accordingly, Section IV-A reviews DaDianNao’s design and how it can process FCLs and CVLs. For clarity, in what follows the term brick refers to a set of 16 elements of a 3D activation or weight array input which are contiguous along the $i$ dimension, e.g., $a(x, y, i)\ldots a(x, y, i+15)$. Bricks will be denoted by their origin element with a $B$ subscript, e.g., $a_B(x, y, i)$. The size of a brick is a design parameter. Furthermore, an FCL can be thought of as a CVL where the input activation array has unit
Fig. 2. Bit-Parallel Engine processing the convolutional layer over two cycles: a) Structure, b) Cycle 1, and c) Cycle 2.

Fig. 3. Processing the example Convolutional Layer Using TRT’s Approach.

Fig. 4. Processing the example Fully-Connected Layer using TRT’s Approach.
x and y dimensions, and there are as many filters as output activations, and where the filter dimensions are identical to the input activation array.

A. Baseline System: DaDianNao

Figure 5a shows a DaDN tile which processes 16 filters concurrently calculating 16 activation and weight products per filter for a total of 256 products per cycle [3]. Each cycle the tile accepts 16 weights per filter for total of 256 weight and 16 input activations. The tile multiplies each weight with only one activation whereas each activation is multiplied with 16 weights, one per filter. The tile reduces the 16 products per filter into a single partial output activation, for a total of only one activation whereas each activation is multiplied with 16 input activations. The tile multiplies each weight with the tile accepts 16 weights per filter for total of 256 weight filters for a total of 256 products per cycle [3]. Each cycle concurrently calculates 16 activation and weight products per cycle. A. Baseline System: DaDianNao

B. Tartan

As Section III explained, TRT processes activations bit-serially multiplying a single activation bit with a full weight per cycle. Each DaDN tile multiplies 16 16-bit activations with 256 weights each cycle. To match DaDN’s computation bandwidth, TRT needs to multiply 256 1-bit activations with 256 weights per cycle. Figure 5b shows the TRT tile. It comprises 256 Serial Inner-Product Units (SIPs) organized in a 16 × 16 grid. Similar to DaDN each SIP multiplies 16 weights with 16 activations and reduces these products into a partial output activation. Unlike DaDN, each SIP accepts 16 single-bit activation inputs. Each SIP has two registers, each a vector of 16 16-bit subregisters: 1) the Serial Weight Register (SWR), and 2) the Weight Register (WR). These correspond to AR and BR of the example of Section III. NBout remains as in DaDN, however, it is distributed along the SIPs as shown.

Convolutional Layers: Processing starts by reading in parallel 256 weights from the SB as in DaDN, and loading the 16 per SIP row weights in parallel to all SWRs in the row. Over the next $P^L$ cycles, the weights are multiplied by the bits of an input activation brick per column. TRT exploits weight reuse across 16 windows sending a different input activation brick to each column. For example, for a CVL with a stride of 4 a TRT tile will processes 16 activation bricks $a_B(x, y, i)$, $a_B(x + 4, y, i)$ through $a_B(x + 63, y, i)$ in parallel a bit per cycle. Assuming that the tile processes filters $f_i$ through $f_{i+15}$, after $P^L_a$ cycles it would produce the following 256 partial output activations: $o_B(x/4, y/4, f_i)$, through $o_B(x/4 + 15, y/4, f_i)$, that is 16 contiguous on the $x$ dimension output activation bricks. Whereas DaDN would process 16 activations bricks over 16 cycles, TRT processes them concurrently but bit-serially over $P^L_a$ cycles. If $P^L_a$ is less than 16, TRT will outperform DaDN by $16/P^L_a$, and when $P^L_a$ is 16, TRT will match DaDN’s performance.

Fully-Connected Layers: Processing starts by loading bit-serially and in parallel over $P^L_w$ cycles, 4K weights into the 256 SWRs, 16 per SIP. Each SWR per row gets a different set of 16 weights as each subregister is connected to one out of the 256 wires of the SB output bus for the SIP row (is in DaDN there are 256 × 16 = 4K wires). Once the weights have been loaded, each SIP copies its SWR to its SW and multiplication with the input activations can then proceed bit-serially over $P^L_a$ cycles. Assuming that there are enough output activations so that a different output activation can be assigned to each SIP, the same input activation brick can be broadcast to all SIP columns. For example, for an FCL a TRT tile will process one activation brick $a_B(i)$ bit-serially to produce 16 output activation bricks $o_B(i)$ through $o_B(i × 16)$ one per SIP column. Loading the next set of weights can be done in parallel with processing the current set, thus execution time
is constrained by $P_{\text{max}}^L = \max(P_a^L, P_w^L)$. Thus, a TRT tile produces 256 partial output activations every $P_{\text{max}}^L$ cycles, a speedup of $16/P_{\text{max}}$ over DaDN since a DaDN tile always needs 16 cycles to do the same.

**Cascade Mode:** For TRT to be fully utilized an FCL must have at least 4K output activations. Some of the networks studied have a layer with as little as 2K output activations. To avoid underutilization, the SIPs along each row are cascaded into a daisy-chain, where the output of one can feed into an input of the next via a multiplexer. This way, the computation of an output activation can be sliced over the SIPs along the same row. In this case, each SIP processes only a portion of the input activations resulting into several partial output activations along the SIPs on the same row. Over the next $np$ cycles, where $np$ the number of slices used, the $np$ partial outputs can be reduced into the final output activation. The user can chose any number of slices up to 16, so that TRT can be fully utilized even with fully-connected layers of just 256 outputs. This cascade mode can be useful in other Deep Learning networks such as in NeuralTalk [16] where the smallest FCLs have at least 4K output activations. Some of the networks studied have a layer with as little as 2K output activations. To make full utilization of an FCL must have at least 4K output activations. Some of the networks such as in NeuralTalk [16] where the smallest FCLs can have 600 outputs or fewer.

**Other Layers:** TRT like DaDN can process the additional layers needed by the studied networks. For this purpose the tile includes additional hardware support for max pooling similar to DaDN. An activation function unit is present at the output of NBout in order to apply nonlinear activations before the output neurons are written back to NM.

**C. SIP and Other Components**

**SIP: Bit-Serial Inner-Product Units:** Figure 7 shows TRT’s Bit-Serial Inner-Product Unit (SIP). Each SIP multiplies 16 activation bits, one bit per activation, by 16 weights to produce an output activation. Each SIP has two registers, a Serial Weight Register (SWR) and a Weight Register (WR), each containing 16 16-bit subregisters. Each SWR subregister is a shift register with a single bit connection to one of the weight bus wires that is used to read weights bit-serially for FCLs. Each WR subregister can be parallel loaded from either the weight bus or the corresponding SWR subregister, to process CVLs or FCLs respectively. Each SIP includes 256 2-input AND gates that multiply the weights in the WR with the incoming activation bits, and a $16 \times 16b$ adder tree that sums the partial products. A final adder plus a shifter accumulate the adder tree results into the output register OR. In each SIP, a multiplexer at the first input of the adder tree implements the cascade mode supporting slicing the output activation computation along the SIPs of a single row. To support signed 2’s complement neurons, the SIP can subtract the weight corresponding to the most significant bit (MSB) from the partial sum when the MSB is 1. This is done with negation blocks for each weight before the adder tree. Each SIP also includes a comparator (max) to support max pooling layers.

**Dispatcher and Reducers:** Figure 8 shows an overview of the full TRT system. As in DaDN there is a central NM and 16 tiles. A Dispatcher unit is tasked with reading input activations from NM always performing eDRAM-friendly wide accesses. It transposes each activation and communicates each a bit at a time over the global interconnect. For CVLs the dispatcher has to maintain a pool of multiple activation bricks, each from
different window, which may require fetching multiple rows from NM. However, since a new set of windows is only needed every $P_o^L$ cycles, the dispatcher can keep up for the layers studied. For FCLs one activation brick is sufficient. A Reducer per title is tasked with collecting the output activations and writing them to NM. Since output activations take multiple cycles to produce, there is sufficient bandwidth to sustain all 16 tiles.

D. Processing Several Activation Bits at Once

In order to improve TRT’s area and power efficiency, the number of activation bits processed at once can be adjusted at design time. The chief advantage of these designs is that less SIPs are needed in order to achieve the same throughput – for example, processing two activation bits at once reduces the number of SIP columns from 16 to 8 and their total number to half. Although the total number of bus wires is similar, the distance they have to cover is significantly reduced. Likewise, the total number of adders required stays similar, but they are clustered closer together. A drawback of these configurations is they forgo some of the performance potential as they force the activation precisions to be multiple of the number of bits that they process per cycle. A designer can chose the configuration that best meets their area, energy efficiency and performance target.

In these configurations the weights are multiplied with several activation bits at once, and the multiplication results are partially shifted before they are inserted into their corresponding adder tree. In order to load the weights on time, the SWR subregister has to be modified so it can load several bits in parallel, and shift that number of positions every cycle. The negation block (for 2’s complement support) will operate only over the most significant product result.

V. Evaluation

This section evaluates TRT’s performance, energy and area compared to DaDN. It also explores the trade-off between accuracy and performance for TRT. Section V-A describes the experimental methodology. Section V-B reports the performance improvements with TRT. Section V-C reports energy efficiency and Section V-D reports TRT’s area overhead. Finally, Section V-E studies a TRT configuration that processes two activation bits per cycle.

A. Methodology

DaDN, STR and TRT were modeled using the same methodology for consistency. A custom cycle-accurate simulator models execution time. Computation was scheduled as described by [11] to maximize energy efficiency for DaDN.

The logic components of the both systems were synthesized with the Synopsys Design Compiler [17] for a TSMC 65nm library to report power and area. The circuit is clocked at 980 MHz. The NBin and NBout SRAM buffers were modelled using CACTI [18]. The eDRAM area and energy were modelled with Destiny [19]. Three design corners were considered as shown in Table II and the typical case was chosen for layout.

B. Execution Time

Table III reports TRT’s performance and energy efficiency relative to DaDN for the precision profiles in Table I separately for FCLs, CVLs, and the whole network. For the 100% profile, where no accuracy is lost, TRT yields, on average, a speedup of $1.61 \times$ over DaDN on FCLs. With the 99% profile, it improves to $1.73 \times$.

There are two main reasons the ideal speedup can’t be reached in practice: dispatch overhead and under-utilization. Dispatch overhead occurs on the initial $P_w^L$ cycles of execution, where the serial weight loading process prevents any useful products to be performed. In practice, this overhead is less than 2% for any given network, although it can be as high as 6% for the smallest layers. Underutilization can happen when the number of output neurons is not a power of two, or lower than 256. The last classifier layers of networks designed to perform recognition of ImageNet categories [20] all provide 1000 output neurons, which leads to 2.3% of the SIPs being idle.

Compared to STR, TRT matches its performance improvements on CVLs while offering performance improvements on FCLs. We do not report the detailed results for STR since they would have been identical to TRT for CVLs and within 1% of DaDN for FCLs.

We have also evaluated TRT on NeuralTalk LSTM [16] which uses long short-term memory to automatically generate image captions. Precision can be reduced down to 11 bits without affecting the accuracy of the predictions (measured as the BLEU score when compared to the ground truth) resulting in a ideal performance improvement of $1.45 \times$ translating into a $1.38 \times$ speedup with TRT. We do not include these results in Table III since we did not study the CVLs nor did we explore reducing precision further to obtain a 99% accuracy profile.

C. Energy Efficiency

This section compares the Energy Efficiency or simply efficiency of TRT and DaDN. Energy Efficiency is the inverse of the relative energy consumption of the two designs. As Table III reports, the average efficiency improvement with TRT across all networks and layers for the 100% profile is $1.17 \times$. In FCLs, TRT is more efficient than DaDN. Overall, efficiency primarily comes from the reduction in effective computation
following the use of reduced precision arithmetic for the inner product operations. Furthermore, the amount of data that has to be transmitted from the SB and the traffic between the central eDRAM and the SIPs is decreased proportionally with the chosen precision.

D. Area

Table [IV] reports the area breakdown of TRT and DaDN. Over the full chip, TRT needs $1.49 \times$ the area compared to DaDN while delivering on average a $1.90 \times$ improvement in speed. Generally, performance would scale sublinearly with area for DaDN due to underutilization. The 2-bit variant, which has a lower area overhead, is described in detail in the next section.

E. TRT$_{2b}$

This section evaluates the performance, energy efficiency and area for a multi-bit design as described in Section [IV-D] where 2 bits are processed every cycle in as half as many total SIPs. The precisions used are the same as indicated in Table I for the 100% accuracy profile rounded up to the next multiple of two. Table [V] reports the resulting performance. The 2-bit TRT always improves performance compared to DaDN as the “vs. DaDN” columns show. Compared to the 1-bit TRT performance is slightly lower however given that the area of the 2-bit TRT is much lower, this can be a good trade-off. Overall, there are two forces at work that shape performance relative to the 1-bit TRT. There is performance potential lost due to rounding all precisions to an even number, and there is performance benefit by requiring less parallelism. The time needed to serially load the first bundle of weights is also reduced. In VGG$_{19}$ the performance benefit due to the lower parallelism requirement outweighs the performance loss due to precision rounding. In all other cases, the reverse is true.

A hardware synthesis and layout of both DaDN and TRT’s 2-bit variant using TSMC’s 65nm typical case libraries shows that the total area overhead can be as low as $24.9\%$ (Table [IV]), with an improved energy efficiency in fully connected layers of $1.24 \times$ on average (Table [III]).

VI. RELATED WORK AND LIMITATIONS

The recent success of Deep Learning has led to several proposals for hardware acceleration of DNNs. This section reviews some of these recent efforts. However, specialized hardware designs for neural networks is a field with a relatively long history. Relevant to TRT, bit-serial processing hardware for neural networks has been proposed several decades ago, e.g., [21], [22]. While the performance of these designs scales with precision it would be lower than that of an equivalently configured bit-parallel engine. For example, Svensson et al., uses an interesting bit-serial multiplier which requires $O(4 \times p)$ cycles, where $p$ the precision in bits [21]. Furthermore, as semiconductor technology has progressed the number of resources that can be put on chip and the trade offs (e.g., relative speed of memory vs. transistors vs. wires) are today vastly different facilitating different designs. However, truly bit-serial processing such as that used in the aforementioned proposals needs to be revisited with today’s technology constraints due to its potentially high compute density (compute bandwidth delivered per area).

In general, hardware acceleration for DNNs has recently progressed in two directions: 1) considering more general purpose accelerators that can support additional machine learning algorithms, and 2) considering further improvements primarily for convolutional neural networks and the two most dominant in terms of execution time layer types: convolutional and fully-connected. In the first category there are accelerators such as Cambricon [23] and Cambricon-X [24]. While targeting support for more machine learning algorithms is desirable, work on further optimizing performance for specific algorithms such as TRT is valuable and needs to be pursued as it will affect future iterations of such general purpose accelerators.

TRT is closely related to Stripes [2], [1] whose execution time scales with precision but only for CVLs. STR does not improve performance for FCLs. TRT improves upon STR by enabling: 1) performance improvements for FCLs, and 2) slicing the activation computation across multiple SIPs thus preventing under-utilization for layers with fewer than 4K outputs. Pragmatic uses a similar in spirit organization to STR.
but its performance on CVLs depends only on the number of activation bits that are 1 [25]. It should be possible to apply the TRT extensions to Pragmatic, however, performance in FCLs will still be dictated by weight precision. The area and energy overheads would need to be amortized by a commensurate performance improvement necessitating a dedicated evaluation study.

The Efficient Inference Engine (EIE) uses synapse pruning, weight compression, zero activation elimination, and network retraining to drastically reduce the amount of computation and data communication when processing fully-connected layers [7]. An appropriately configured EIE will outperform TRT for FCLs, provided that the network is pruned and retrained. However, the two approaches attack a different component of FCL processing and there should be synergy between them. Specifically, EIE currently does not exploit the per layer precision variability of DNNs and relies on retraining the network. It would be interesting to study how EIE would benefit from a TRT-like compute engine where EIE’s data compression and pruning is used to create vectors of weights and activations to be processed in parallel. EIE uses single-lane units whereas TRT uses a coarser-grain lane arrangement and thus would be prone to more imbalance. A middle ground may be able to offer some performance improvement while compensating for cross-lane imbalance.

Eyeriss uses a systolic array like organization and gates off computations for zero activations [9] and targets primarily high-energy efficiency. An actual prototype has been built and is in full operation. Cnvlutin is a SIMD accelerator that skips on-the-fly ineffectual activations such as those that are zero or close to zero [8]. Minerva is a DNN hardware generator which also takes advantage of zero activations and that targets high-energy efficiency [10]. Layer fusion can further reduce off-chip communication and create additional parallelism [26]. As multiple layers are processed concurrently, a straightforward combination with TRT would use the maximum of the precisions when layers are fused.

Google’s Tensor Processing Unit uses quantization to represent values using 8 bits [27] to support TensorFlow [28]. As Table I shows, some layers can use lower than 8 bits of precision which suggests that even with quantization it may be possible to use fewer levels and to potentially benefit from an engine such as TRT.

A. Limitations

As in DaDN this work assumed that each layer fits on-chip. However, as networks evolve it is likely that they will increase in size thus requiring multiple TRT nodes as was suggested in DaDN. However, some newer networks tend to use more but smaller layers. Regardless, it would be desirable to reduce the area cost of TRT most of which is due to the eDRAM buffers. We have not explored this possibility in this work. Proteus [15] is directly compatible with TRT and can reduce memory footprint by about 60% for both convolutional and fully-connected layers. Ideally, compression, quantization and pruning similar in spirit to EIE [7] would be used to reduce computation, communication and footprint. General memory compression techniques offer additional opportunities for reducing footprint and communication.

We evaluated TRT only on CNNs for image classification. Other network architectures are important and the layer configurations and their relative importance varies. TRT enables performance improvements for two of the most dominant layer types. We have also provided some preliminary evidence that TRT works well for NeuralTalk LSTM [16]. Moreover, by enabling output activation computation slicing it can accommodate relatively small layers as well.

Applying some of the concepts that underlie the TRT design to other more general purpose accelerators such as Cambricon [23] or graphics processors would certainly be more preferable than a dedicated accelerator in most application scenarios. However, these techniques are best first investigated into specific designs and then can be generalized appropriately.
We have evaluated TRT only for inference only. Using an engine whose performance scales with precision would provide another degree of freedom for network training as well. However, TRT needs to be modified accordingly to support all the operations necessary during training and the training algorithms need to be modified to take advantage of precision adjustments.

This section commented only on related work on digital hardware accelerators for DNNs. Advances at the algorithmic level would impact TRT as well or may even render it obsolete. For example, work on using binary weights would obviate the need for an accelerator whose performance scales with weight precision. Investigating TRT’s interaction with other network types and architectures and other machine learning algorithms is left for future work.

VII. CONCLUSION

This work presented Tartan, an accelerator for inference with Convolutional Neural Networks whose performance scales inversely linearly with the number of bits used to represent values in fully-connected and convolutional layers. TRT also enables on-the-fly accuracy vs. performance and energy efficiency trade-offs and its benefits were demonstrated over a set of popular image classification networks. The new key ideas in TRT are: 1) Supporting both the bit-parallel and the bit-serial loading of weights into processing units to facilitate the processing of either convolutional or fully-connected layers, and 2) cascading theadder trees of various subunits to enable slicing the output computation thus reducing or eliminating cross-layer imbalance for relatively small layers.

TRT opens up a new direction for research in inference and training by enabling precision adjustments to translate into performance and energy savings. These precisions adjustments can be done statically prior to execution or dynamically during execution. While we demonstrated TRT for inference only, we believe that TRT, especially if combined with Pragmatic, opens up a new direction for research in training as well. For systems level research and development, TRT with its ability to trade off accuracy for performance and energy efficiency enables a new degree of adaptivity for operating systems and applications.

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