The Study of Transient Faults Propagation in Multithread Applications

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ABSTRACT
Whereas contemporary Error Correcting Codes (ECC) designs occupy a significant fraction of total die area in chip-multiprocessors (CMPs), approaches to deal with the vulnerability increase of CMP architecture against Single Event Upsets (SEUs) and Multi-Bit Upsets (MBUs) are sought. In this paper, we focus on reliability assessment of multithreaded applications running on CMPs to propose an adaptive application-relevant architecture design to accommodate the impact of both SEUs and MBUs in the entire CMP architecture.

This work concentrates on leveraging the intrinsic soft-error-immunity feature of Spin-Transfer Torque RAM (STT-RAM) as an alternative for SRAM-based storage and operation components. We target a specific portion of working set for reallocation to improve the reliability level of the CMP architecture design. A selected portion of instructions in multithreaded program which experience high rate of referencing with the lowest memory modification are ideal candidate to be stored and executed in STT-RAM based components. We argue about why we cannot use STT-RAM for the global storage and operation counterparts and describe the obtained resiliency compared to the baseline setup. In addition, a detail study of the impact of SEUs and MBUs on multithreaded programs will be presented in the Appendix.

Keywords
multi-threaded applications; on-line testing; soft error; single event upset; multiple bit upset; fault-tolerant systems; memory structure; emerging technology;

1. INTRODUCTION
In order to keep performance improvement rates within a given power budget, the ITRS technology roadmap recommends the movement toward employing many-core processors in devices offering reduced power consumption and execution time. To maximize the beneficial of using many-core processors, thread level parallelism has been introduced as an inevitable counterpart in multicore programming [5]. Meanwhile, the advances in CMOS technology have provided reduction in transistor size and voltage levels which results in significant increase of transient fault occurrence in the microprocessors. In particular, given roughly 50% of chip is occupied by memory structure, the existing memory module becomes highly susceptible to soft errors [13].

Soft errors also referred as Single Event Upsets (SEUs) induced by energetic particles penetrate the silicon substrate and generate electron-hole pairs along their tracks. If the generated electrons collected into cell junction is larger than critical charge (Qc), it can flip the cell state [7], [9]. The smaller device size and power supply reductions have severely increased the impact of SEU on deep-submicron technology, as they reduced aggressively the critical charge of memory cells [8], [6]. Thus, the memory cells have become more sensitive to atmospheric neutrons as well as to alpha particles which are created by unstable isotopes in the materials of a chip.

Furthermore, the technology scaling and high precision manufacturing techniques have also decreased the separation distance between two adjacent memory cells which results in a single particle strike passing through adjacent cells in a row flip more than one cell. This phenomenon is called Multiple-bit Upset (MBU) [4]. The main issue regarding the MBU handling is that the existing Error Correcting Codes (ECC) are not able to handle MBUs due to unpredictable behavior of the impact of soft errors when they flip more than one memory cell. To maintain acceptable reliability levels, the state-of-the-art MBU protection techniques have recently received significant attention to protect modern multicore architectures from the potential write and read failures introduced by soft errors.

One intuitive solution is to replace traditional vulnerable SRAM-based memory technology with soft-error-immune memory modules such as Spin-Transfer Torque Magnetic Random Access Memory (STT-RAM). The STT-RAM offers high density, low standby power, nonvolatility and soft error resiliency [14], [21]. Recent research shows that the intrinsic immunity of STT-RAM to soft errors cause this device gets influenced by several order lower soft errors compared to

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The authors of [15] proposed an architectural radiation-induced soft error resilient solution for L1 cache through using STT-RAM as alternative for traditional SRAM. However, this work only concentrates on the impact of soft errors in L1 cache while the lifetime of a L1 cacheline is extremely short which means the error caused by particle strikes may not have enough time to be either consumed by CPU or propagated to the lower level of memory hierarchy. On the other hand, the authors of [14] studied the impact of using 3D stacked STT-RAM caches on the reliability of the whole cache hierarchy. They proposed a set of configurations for cache hierarchy and compared the results in respect of performance, power consumption and reliability. The obtained results show that the replacing memories with a STT-RAM alternative can significantly mitigate soft errors while offering slight performance improvement.

In this work, we show that not every memory component in the processor core is required to be replaced by STT-RAM because the following reasons:

- The frequency of instruction call is not similar for every single instruction of the program. For example, a 95% of a program execution time may be spent on an iteration which implies that this portion of program is more susceptible to soft errors if the generated error be consumed by CPU before masking the error through a write operation.

- The instructions running on CPU show various sensitivity to soft errors. For example, if a bit cell in register file of a sensitive instruction flipped due to particle strike, the error is immediately propagated into the multithreaded program which may result in the rapid crash of the program.

- The STT-RAM suffers from long write latency and high write energy which impose extra overhead to run write-intensive workloads in terms of performance reduction and high dynamic energy consumption.

The ideal instructions to benefit from soft-error-immune STT-RAM memory component are those instructions which experience high rate of referencing with the lowest memory modification. Thus, a comprehensive study is required to recognize highly sensitive instruction to soft errors either to SEU or to MBU, and frequently called instructions with the lowest memory modification in the system. To protect aforementioned instruction typeset, we propose to use STT-RAM memory module to maintain the reliability levels of the system in an acceptable error margin. Accordingly, the trade-off among reliability, performance, and power consumption of the proposed technique compared to traditional methodologies will be explored.

The outline of the rest of the paper is as follows: we examine the runtime behavior of multithreaded programs in Section 2. The proposed execution model assumed in this paper will be presented in Section 3. The experimental results will be discussed in Section 4. Finally, we conclude the paper in Section 5.

2. THE RUNTIME PROGRAM BEHAVIOR

The runtime program behavior is required to be investigated to help us to determine which functions or instructions are ideal candidates to be mapped on soft error resilient STT-RAM components.

2.1 The Frequency Call of Instructions

In order to investigate the instruction references in multithreaded programs, we used Visual Studio 2013 Profiler Instrumentation with no special optimizations on Intel i7 with 8 GBs of RAM. The data values and ranges in the report are named "Elapsed Inclusive Time %", "Elapsed Exclusive Time %", "Avg. Elapsed Inclusive Time" and "Avg. Elapsed Exclusive Time" which are defined accordingly "The percentage of time spent executing a function and its child functions", "The percentage of time spent executing a function excluding its child functions", "The average time spent executing a function and its child functions" and "The average time spent executing a function excluding its child functions". Table 1 shows most used functions in each benchmark and the results gathered from instrumentation.

2.2 The Sensitivity Analysis of Instructions to Soft Errors

We define the application resilience to soft errors as its ability to tolerate hardware faults if they occur, without leading to an incorrect output. Incorrect outputs are also known as Silent Data Corruptions (SDCs). To recover this group of failures, there is no dedicated method to indicate that the application has malfunctioned (unlike a crash or a hang, where either an exception is raised or a timeout occurs). Since, we are primarily interested in evaluating the soft error immunity of applications, we only inject faults into the program's data or instructions that are visible at the assembly code or higher levels, rather than into the micro-architectural structures.

 Accordingly, we classify the outcome of activated faults based on the program's behavior to following categories:

- Crash: if the program is terminated by the OS due to an exception.
- Silent Data Corruption (SDC): if the output is incorrect due to lack of appropriate method to report the impact of the fault propagation.

Figure. 1 shows the impact of SEU on benchmarks suite which benefit from POSIX Pthreads standard for creating and handling threads. The most SEUs in the benchmarks are factorial benchmarks result in SDC in our system while other benchmarks often crash when a soft error occurs. Furthermore, Figure. 2 shows that the rate of crash or SDC significantly increase as the number of flipped bits increased. This results confirm our previous statement that MBUs are major reliability issue in current multi-core systems which demand a comprehensive solution for mitigating them.

To determine the most sensitive instructions to soft error, we target various type of instructions. We noticed that pthread related code fragments show high vulnerability to soft errors. This means pthread related code fragments are required to be mapped on soft-error-immune storage and operation components. For further information, please refer to Appendix A.

3. THE PROPOSED EXECUTION MODEL

To completely benefit from the intrinsic soft error resiliency characteristic of STT-RAM, we also need to thoroughly explore the other aspects of using STT-RAM instead of SRAM.
Table 1: The function reference computation using Visual Studio 2013 profiler instrumentation

| Benchmarks | Function Name | Number of Calls | Elapsed Inclusive | Elapsed Exclusive | Avg. Elapsed Inclusive (sec) | Avg. Elapsed Exclusive (sec) |
|------------|---------------|-----------------|-------------------|-------------------|-----------------------------|-----------------------------|
| blackscholes | mainCRTStartup | 1 | 100 | 34.41 | 162.89 | 56.05 |
|             | be_thread     | 1 | 34  | 162.89 | 56.05 | 55.38 |
| specrand   | printf        | 1,002 | 99.9  | 34.41 | 152.25 | 55.38 |
|            | mainCRTStartup | 1 | 99.9  | 34.41 | 152.25 | 55.38 |
| mm         | pthread_join  | 8  | 51.93 | 34.41 | 0.07  | 0.07  |
|            | pthread_create | 2 | 21.39 | 34.41 | 0.07  | 0.07  |
|            | printf        | 1 | 51.93 | 34.41 | 0.07  | 0.07  |
| qs         | pthread_join  | 5  | 24.74 | 34.41 | 0.14  | 0.14  |
|            | pthread_create | 2 | 17.12 | 34.41 | 0.14  | 0.14  |
|            | printf        | 1 | 34.41 | 34.41 | 0.14  | 0.14  |
| factorial  | CxxSetUnhandledExceptionFilter | 1 | 9.86  | 0.14  | 0.03  | 0.03  |
| circular_buffer | pthread_join | 2 | 35.41 | 0.14  | 0.03  | 0.03  |
|            | pthread_create | 2 | 35.41 | 0.14  | 0.03  | 0.03  |
| stack      | pthread_join  | 2 | 35.41 | 0.14  | 0.03  | 0.03  |
|            | pthread_create | 2 | 35.41 | 0.14  | 0.03  | 0.03  |

Figure 1: Aggregated single fault injection results with LLFI for all operation instructions

3.1 The Spin-Transfer Torque Magnetic Random Access Memory (STT-RAM)

As illustrated in Figure 1, the STT-RAM uses magnetic elements called magnetic tunneling junction (MTJ) to store data in which a thin insulating oxide layer, e.g. MgO, is sandwiched by two ferromagnetic layers. Moreover, the upper ferromagnetic layer usually aliased as free layer, its polarity of magnetic field can be flipped over during a write event; while, the lower ferromagnetic layer usually called as pinned layer is designed to have its magnetization pinned. Thus, MTJ has low (high) resistance distribution if the magnetization of the free layer and the pinned layer are aligned (anti-aligned). Accordingly, low (high) resistance distribution is stored in MTJ, instead of traditional electronic charge or current flow.

For a read operation, a small current is required to be driven from bit-line to source line. Unlike read operation, a successful write operation requires a current flow drive either from bit-line to source-line or vice versa, depending on the differential voltage between these two lines. Although STT-RAM does not suffer from write endurance, however the advent of long write latency and high energy consumption exacerbate the performance of STT-RAM. Figure 1 shows the write latency comparison for various cache module configurations among three well-known memory technologies including eDRAM, STT-RAM, and SRAM obtained from NVSim [3] for 45nm technology node. This comparison shows that the STT-RAM is not a good candidate for small size memory module due to its long write latency compared to other technologies. This means that the design of proposed architecture should carefully leverage the potential of STT-RAM for small size storage elements like register arrays in the processor’s pipeline.
is stored in reliable portions of the data cache. Note that
able space). When this reliable address is accessed, the data
data can be linked to a reserved virtual address space (reli-
based on regions of physical memory address. This can be
data stored in memory is distinguished from unreliable data
elements. To be specific, the reliable and unreliable registers
RAM offering high resiliency to soft errors while the tradi-
in the form of both reliable and unreliable storage compo-
components.

As illustrated in Figure. 3, the proposed storage is offered
in the form of both reliable and unreliable storage compo-
ments. The reliable storage components are made of STT-
RAM offering high resiliency to soft errors while the tradi-
tional SRAM cells are used for creating unreliable storage
elements. To be specific, the reliable and unreliable registers
are distinguished based on the register number. The reliable
instructions can use special functional units which
operations as well as reliable floating point operations. The
reliable instructions can use special functional units which
are made of STT-RAM offering soft error resiliency. Note
that even if a field which should be mapped into soft-error-
immune field ends up stored in an unreliable memory, it
will still be loaded into reliable registers and be subject to
reliable operations.

4. EXPERIMENTAL RESULTS

In order to evaluate the proposed technique, LLVM-based
fault injection tool called LLFI [20] has been used to inject
transient faults into the multithreaded programs in a multi-
core system (Intel(R) Core(TM) i7-4770 CPU @ 3.40GHz,
RAM=6GB, OS=Linux Ubuntu 14.04.3 LTS). LLFI works
at the LLVM compiler’s IR level, and allows fault-injections
to be performed at specific program points, and into par-
ticular instructions. LLFI supports various fault injection
customizations, and enables tracing the propagation of the
fault among instructions in the program.

The steps required to inject faults using LLFI are as fol-
following:

- In Step 1, LLFI takes the program IR as input, and ap-
plies custom fault injection instruction and operand(s)
selector to determine which instructions/operands are
fault injection candidates.
- In Step 2, LLFI instruments the fault injection instruc-
tions/operands with calls to fault injection functions.
The fault injection functions are designed to perturb
the specific instruction operand according to the spec-
fied fault type at runtime (e.g. flip one bit of the
operand for bit-flip faults).
- In Step 3, the compiled program is executed at run-
time, and LLFI randomly selects one runtime instance
of the instrumented instructions to trigger the fault in-
jection function and inject into the selected instruction
operand value.

Because hardware faults occur randomly at runtime, LLFI
picks a random instruction from the set of all dynamically
executed instructions at runtime to inject into.

The benchmarks suite we used in our experimental results
are as following:

- blackscholes: The blackscholes application is an Intel
RMS benchmark. It calculates the prices for a port-
folio of European options analytically with the Black-
Scholes partial differential equation. (PDE).
- specrand: The benchmark simply generates a sequence
of pseudorandom numbers starting with a known seed.
- Matrix Multiplication (mm): It is a simple matrix mul-
tiplication program in which the main thread makes
slave threads responsible to compute each elements of
the product separately and concurrently.
int main(void) 
{
    int x;
    nv_int y;
    int A[100];
    nv_int B[100];
    nv_pthread_t id1, id2;
    nv_pthread_mutex_init(&m, 0);
    nv_pthread_create(&id1, NULL, t1, &queue);
    ...
    return 0;
}

Figure 5: HW/SW model assumed in our system. The green areas are made of soft-error-resilient memory module.

- Quick Sort (qs): It is a simple quick sort program in which main thread first partitions the 100-elements array of integers into two parts, by performing one round of the quick sort algorithm, then assigns each sub-arrays to a slave thread in order to sort each part separately and simultaneously.
- factorial: It computes the product of all positive integers less than or equal to n.
- circular_buffer: It simulates a buffer using shared variables to synchronize receive and send operations.
- stack: It is a program simulating a data-stack structure.

Since we are interested in the study of the impact of MBUs in the existing CMP architectures, we injected 1000 multiple faults into the assumed hardware model in our system. The results show that the proposed architecture design is 30% on average more resilient to soft errors as shown in Figure. 6, 7, and 8. The obtained results show the efficiency of the proposed method to handle soft errors in the entire CMP architecture. For most of the benchmarks, the replacement of a portion of memory modules reduces the period during which the data in the storage component are exposed to particle strikes. In the cache hierarchy, the use of STT-RAM to maintain frequently read cachelines in the high-dense low-level caches significantly increase the reliability level of the system. The main reason for the high vulnerability of traditional low-level caches to soft error is the high potential of residing a data block in the last level cache for millions of cycles between two consecutive accesses [11].

In the pipeline stage, the replacement of a portion of unreliable registers and functional units with reliable elements eliminate a high portion of faults in operation components. However, the soft error in logic components still can be propagated in our proposed approach. Nonetheless, this portion of faults are relatively small compared to other faults which exclusively target storage and operation components.

5. CONCLUSIONS

In this paper, we focused on leveraging the intrinsic soft-error-immunity characteristic of STT-RAM as an alternative for SRAM-based storage and operation components. We

Figure 6: Aggregated results for multiple fault injection into all operation instructions of the proposed HW model.

Figure 7: Aggregated results for multiple fault injection into arithmetic operation instructions of the proposed HW model.
showed that a specific portion of working set in the multi-threaded programs are ideal candidate to be stored and executed in STT-RAM based components. Doing so, the proposed CMP architecture can achieve 30% on average more resilient to soft errors.

6. FUTURE WORK

We still look for a methodology to determine those instructions which experience high rate of references with the lowest memory modification. To attain this goal, we started to look into intel etune [12] which provides a rich set of performance insight into CPU performance, threading performance & scalability, bandwidth, caching and much more. We expect to better determine the candidates for using STT-RAM elements through obtaining the rate of memory modification by executing each instruction. In addition, another section in experimental results needs to be added which shows the amount of energy consumption and performance benefit achieved using the proposed method compared to traditional approach.

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8. APPENDIX A

A detail study of the impact of soft errors on multithreaded programs are shown in Figure. 9 and 10. The soft errors contribute the most SDCs in specrand and factorial benchmarks in both arithmetic and load/store instruction typesets while other benchmarks only crash depend on the sensitivity of their instructions to soft errors. For example, mm, qs and stack benchmarks show high sensitivity to soft errors while the circular_buffer workload does not readily get influenced by soft errors.