Quantitatively Enhanced Reliability and Uniformity of High-κ Dielectrics on Graphene Enabled by Self-Assembled Seeding Layers

Vinod K. Sangwan¹, Deep Jariwala¹, Stephen A. Filippone¹¹, Hunter J. Karmel¹, James E. Johns¹, Justice M. P. Alaboson¹, Tobin J. Marks¹,² *, Lincoln J. Lauhon¹ *, Mark C. Hersam¹,²,³ *

¹Department of Materials Science and Engineering, Northwestern University, Evanston, Illinois 60208
²Department of Chemistry, Northwestern University, Evanston, Illinois 60208
³Department of Medicine, Northwestern University, Evanston, Illinois 60208

ABSTRACT: The full potential of graphene in integrated circuits can only be realized with a reliable ultra-thin high-κ top-gate dielectric. Here, we report the first statistical analysis of the breakdown characteristics of dielectrics on graphene, which allows the simultaneous optimization of gate capacitance and the key parameters that describe large-area uniformity and dielectric strength. In particular, vertically heterogeneous and laterally homogenous Al₂O₃ and HfO₂ stacks grown *via* atomic-layer deposition and seeded by a molecularly thin perylene-3,4,9,10-tetracarboxylic dianhydride organic monolayer exhibit high uniformities (Weibull shape
parameter $\beta > 25$) and large breakdown strengths (Weibull scale parameter, $E_{BD} > 7$ MV/cm) that are comparable to control dielectrics grown on Si substrates.

KEYWORDS: epitaxial graphene, alumina, hafnia, Weibull analysis, dielectric breakdown, nanoelectronics

The success of Si in integrated circuits (ICs) can be attributed to the fortuitous combination of several desirable properties exhibited by the interface between crystalline Si and its native amorphous oxide. For example, the technical ease of integration, low interfacial trap charge density, high interfacial barrier height with Si, and high breakdown reliability of silicon dioxide have contributed to the dominance of Si in ICs despite the lower charge carrier mobility of Si compared to competing semiconductors such as Ge and GaAs.$^{1,2}$ Today, an emerging electronic material, graphene, is being seriously considered for radio frequency (RF) electronics due to its high carrier mobility ($\sim 200,000$ cm$^2$/Vs), high saturation velocity, and two-dimensional structure.$^{3-7}$ With these attributes, most of the applied research on top-gated graphene electronics has focused on achieving a high cut-off frequency, a high field-effect mobility, and current saturation.$^{8-20}$ However, in light of the aforementioned historical precedent set by Si, a reliable high-capacitance top-gate dielectric with wafer-scale uniformity will also be required for graphene to achieve the required scaling for high-frequency operation and seamless integration with existing technologies.$^{1,12,13,21}$ Towards this end, we report here the first extensive and systematic study of the breakdown characteristics of top-gated dielectrics deposited on graphene,
thereby enabling the identification of optimized dielectric growth conditions and structures for high reliability and large-area uniformity.

Atomic layer deposition (ALD) has emerged as a ubiquitous technology for dielectric deposition in the microelectronics industry due to several compelling advantages such as large-area pin-hole free conformal coating, atomic-level thickness control, low-temperature growth, and compatibility with a wide range of materials. However, the chemically inert nature of the graphene surface coupled with its hydrophobicity results in non-conformal ALD growth. Surface treatments of graphene to seed ALD via chemical functionalization with nitrogen dioxide, oxidized metals, or polymer coatings can degrade the properties of the underlying graphene or reduce the overall gate capacitance. While physical vapor deposition and oxidation of metal films on graphene can yield promising gate-dielectrics, these approach lack atomic level thickness control and suffer from the inherently rougher surfaces of evaporated metal films. Furthermore, efforts to seed ALD by ozone exposure demonstrated minimal perturbation to graphene at low growth temperatures but increased damage at higher temperatures. Recently, ALD oxide growth has been seeded on graphene by self-assembled molecular layers of perylene-3,4,9,10-tetracarboxylic-3,4,9,10-dianhydride (PTCDA), which circumvents these issues and results in low-leakage, high-capacitance gate-dielectrics. Here, we further demonstrate that PTCDA-seeded ALD growth provides a reliable pathway to vertically heterogeneous oxide stacks that simultaneously maximize gate capacitance, dielectric strength, and large-area homogeneity. In this manner, this work addresses the critical issues that underlie dielectric reliability and uniformity, thereby providing a pathway to wafer-scale graphene-based nanoelectronic circuits.
Dielectrics may break down due to intrinsic effects (e.g., Joule heating, impact ionization) or by extrinsic processing flaws (e.g., pin-holes, defects). Notwithstanding the underlying mechanism, dielectric breakdown is characterized by a “weakest-link failure” event where a single short-circuit can trigger thermal runaway, leading to irreversible damage. Thus, dielectric breakdown is a highly stochastic process, requiring statistical analysis of a large number of test structures (e.g., capacitors) to understand the underlying breakdown mechanisms and predict reliability. Weakest-link failure events are typically characterized by the Weibull distribution. Industry standards for predicting the lifetimes of electrical circuits are based on extreme value statistical analysis of time-dependent gate oxide breakdown (TDDB) measurements. Note that the voltage to breakdown ($V_{BD}$) distribution also follows a Weibull form for a constant voltage ramp-rate, which has been shown to be a robust predictor for TDDB. Therefore, for this first dielectric breakdown study on graphene, we conduct statistical analysis based on the $V_{BD}$ distribution. The 2-parameter Weibull cumulative distribution function (CDF) is given by:

$$F_{BD} = 1 - \exp \left( -\left(\frac{V_{BD}}{\alpha}\right)^\beta \right)$$

where $\alpha$ (the scale parameter) represents the voltage at which 63% of the devices fail, and $\beta$ (the shape parameter) characterizes the width of the distribution. Consequently, a large value of $\alpha$ signifies high electrical breakdown strength, while a large value of $\beta$ represents high uniformity. The Weibull CDF can be rearranged as:

$$\ln(-\ln(1 - F_{BD})) = \beta \ln(V_{BD}) - \beta \ln \alpha$$

which allows the Weibull parameters, $\alpha$ and $\beta$, to be extracted from the intercept and slope of a linear plot of $\ln(-\ln(1 - F_{BD}))$ versus $\ln(V_{BD})$ (i.e., the Weibull plot). In terms of reliability, $\beta <$
1 signifies “infant-mortality” and the rate of failure decreases with increasing voltage (or time). Such failures can be attributed to systematic defects caused by intrinsic flaws in the dielectric processing, and they result in “dead-on-arrival” products that are highly undesirable. Therefore, a $\beta > 1$ is one of the most important metrics for reliability where the failure rate increases with voltage (or time) due to common “wear-out.”

In this study, capacitors were fabricated on epitaxially grown graphene (mixture of single-layer and bilayer graphene, Supporting S1) on 9 mm x 4.5 mm n-type 4H-SiC (EG-SiC) substrates. Less than two monolayers (< 2 MLs) of PTCDA were grown in a thermal evaporator (Fig. 1a, Supporting S1), followed by ALD growth of $\text{Al}_2\text{O}_3$ and $\text{HfO}_2$ dielectrics (Supporting S1). Capacitors of three different areas (area-1 = 20 µm x 20 µm, area-2 = 50 µm x 50 µm, and area-3 = 80 µm x 80 µm, see Figs. 1b, d) were fabricated by evaporating 100 nm thick Au through shadow masks. A dielectric thickness of 10 nm was chosen based on well-behaved current-voltage (I-V) characteristics. Thinner dielectrics (8 nm and 5 nm) exhibited significantly larger pin-hole density as discussed in Supporting S4. To simultaneously optimize capacitance, large-area uniformity, and dielectric strength, the two most commonly studied high-$\kappa$ oxides, $\text{Al}_2\text{O}_3$ and $\text{HfO}_2$, were introduced in four different sample layering configurations. Fig. 1c shows the vertical structure of these four dielectric stacks: sample-1 (8 nm $\text{HfO}_2$ + 2 nm $\text{Al}_2\text{O}_3$ + PTCDA + EG-SiC); sample-2 (10 nm $\text{Al}_2\text{O}_3$ + PTCDA + EG-SiC); sample-3 (10 nm $\text{HfO}_2$ + PTCDA + EG-SiC); sample-4 (8 nm $\text{Al}_2\text{O}_3$ + PTCDA + EG-SiC). Capacitance-voltage (C-V) measurements on these samples (Fig. 1e) show the expected broad V-shape due to the quantum capacitance ($C_Q$) of graphene. The larger capacitance variation between devices in sample-3 is consistent with increased dielectric thickness variations from AFM images (Supporting S5). Flattening of the C-V plot on the left side ($V < 0$ V) can be attributed to the formation of a
depletion region in the n-doped SiC. Therefore, a C_Q model was fit to the right side of the curves to extract the capacitance of these dielectric stacks (Supporting S2). It should be noted that the C_Q model does not fully account for all experimental conditions including the presence of a mixture of single-layer and bilayer graphene, gate-induced modulation of the depletion region in the SiC substrate, and the frequency-dependent capacitance resulting from series resistance at the ground contact (Supporting S2). However, these secondary effects are minimized by conducting the measurements at low frequency (1 kHz) and fitting the C_Q model only for V_g > 0 V.

The capacitance of the four samples (sample-1 = 785 nF/cm², sample-2 = 545 nF/cm², sample-3 = 890 nF/cm², and sample-4 = 610 nF/cm²) implies dielectric constants of the constituent oxides Al₂O₃ (κ_{Al₂O₃} = 6.5) and HfO₂ (κ_{HfO₂} = 13) that are consistent with literature precedent (Supporting S2). The extracted dielectric constants of the oxides are also consistent with the C-V response of the same dielectric stack deposited on Si control substrates (control-1: 8 nm HfO₂ + 2 nm Al₂O₃ + 1.8 nm native oxide + Si, Fig. 2a), see Supporting S2. A parallel-plate capacitor model also yields a PTCDA thickness (assuming κ_{PTCDA} = 1.9, perpendicular to the molecular plane) of less than 0.5 nm in all the samples (Supporting Table S1). The extracted sub-2 ML thickness of PTCDA (1 ML thickness = 0.3 nm) from the C-V analysis is consistent with the absence of fluorescence in the Raman spectra for < 2 MLs PTCDA (Supporting S1).

Capacitor I-V measurements were conducted in vacuum (< 10⁻⁴ mbar) by biasing the Au electrode from 0-10 V at a ramp rate of 0.04 V/s. A positive voltage was chosen to minimize band-bending at the interface of the underlying substrates (n-SiC and n-Si). All samples showed leakage currents less than 10⁻⁸ A/cm² for biases < 2 V (Supporting S3). At larger biases, the current begins to increase reversibly in the soft-breakdown regime (soft-breakdown mechanisms such as Fowler-Nordheim tunneling and Poole-Frenkel emission are discussed in Supporting S3).
Eventually, the voltage becomes high enough that the current spikes by 2-3 orders of magnitude and reaches the compliance limit (10 µA) within 0.01 V, allowing for a clear definition of the breakdown voltage ($V_{BD}$). This catastrophic event is characteristic of irreversible damage to the dielectric (i.e., hard breakdown). Fig. 2b shows the current density ($J$) plotted versus electric field ($E$) for sample-1 and control-1. The solid $J$-$E$ curve corresponds to a capacitor with $V_{BD}$ in the middle of the Weibull distribution, while the dashed curves represent the two extreme values of $V_{BD}$, excluding low and high voltage tails. Thus, all of the capacitors measured for sample-1 and control-1 that follow the Weibull distribution show $J$-$E$ curves that fall between the two corresponding dashed curves (I-V characteristics of all 210 sample-1 capacitors are shown in Supporting S3).

We first discuss the $J$-$E$ curves in the soft-breakdown regime before proceeding to the statistical analysis of hard-breakdown characteristics. Both sample-1 and control-1 show indiscernible spreads in current density in Fig. 2b over the soft-breakdown regime (< 6 MV/cm) and a larger spread in the effective breakdown fields $E_{BD}$ ($E_{BD} = (V_{BD} - V_{Interface})/d$, $d =$ total dielectric thickness, $V_{Interface} =$ voltage drop across graphene-SiC interface). Sample-1 capacitors break down earlier and have a wider spread in $E_{BD}$ than the control-1 capacitors. The current density in sample-1 is approximately an order of magnitude lower than that in control-1. This lower leakage current in sample-1 arises from its unique band-offset. In particular, lower leakage currents in high-\(\kappa\) (small band-gap) dielectrics are commonly achieved by creating a large band-offset via incorporation of an ultra-thin interfacial layer of a low-\(\kappa\) (large band-gap) material.\textsuperscript{48} However, this mechanism fails to explain the characteristics of the present devices because the interfacial layer of SiO\(_2\) in control-1 has a larger band-offset than PTCDA or Al\(_2\)O\(_3\) in sample-1. Consequently, we attribute the lower current density in sample-1 to a Schottky
barrier at the interface between the epitaxial graphene and the n-type 4H-SiC.\textsuperscript{49} Previously, C-V measurements on EG-SiC have shown Fermi-level ($E_F$) pinning of graphene approximately 0.49 eV above the charge-neutrality point.\textsuperscript{49} Quantum capacitance model fits of C-V curves (Fig. 1e) also yield a charge density ($n$) of $\sim$5 x 10\textsuperscript{12}/cm\textsuperscript{2} (Supporting Table S1), resulting in a Fermi energy offset of 0.28 eV, calculated from $E_F = \hbar v_F \sqrt{\frac{n}{\pi}}$, where $\hbar$ is Planck’s constant divided by 2$\pi$ and $v_F$ ($\sim$10\textsuperscript{8} cm/s) is the Fermi velocity of graphene. The discrepancy in the derived Fermi level could be due to bilayer graphene regions in EG-SiC and/or additional doping introduced by the dielectric growth process. In either case, a Schottky barrier in addition to a triangular potential barrier in the dielectric can explain the reduced quantum mechanical tunneling probability and thus the lower current density. Note that this Schottky contact also reduces the overall voltage across the dielectrics by 0.28 V, which is then subtracted from the applied voltage to obtain the effective electric field (E) in the dielectrics for all samples except control-2 (consisting of same oxide stack as sample-1 (8 nm HfO\textsubscript{2} + 2 nm Al\textsubscript{2}O\textsubscript{3}) grown directly on EG-SiC without PTCDA, Fig. 3c) where 20% of the devices break at $V_{BD} < 0.28$ V due to excessive pin-holes (Supporting S5).

A Weibull plot of $V_{BD}$ distributions for sample-1 capacitors of different areas is shown in Fig. 3a (see $V_{BD}$ histograms in Supporting S3). A good linear fit ($r^2 > 0.95$) to the majority of the data (>85%, excluding low voltage tails that are visibly separated from the majority of the data) indicates that the $V_{BD}$ data are described well by a 2-parameter Weibull distribution. Weibull parameters and 95% confidence bounds were extracted using a previously reported methodology (Supporting Table S2).\textsuperscript{50, 51} Since Weibull fits assume a random distribution of breakdown locations within the dielectric, we confirm the validity of this assumption explicitly.
by scaling all capacitors to a common area of 1 mm$^2$. For randomly distributed defects, $V_{BD}$ data is expected to obey the following area (A) scaling law:\(^{42}\)

$$\ln(-\ln(1-F_1)) - \ln(-\ln(1-F_2)) = \ln\left(\frac{A_1}{A_2}\right).$$

Therefore, random defects should result in statistically identical $\beta$ values for different areas, whereas $\alpha$ should scale as $\frac{\alpha_1}{\alpha_2} = \left[\frac{A_2}{A_1}\right]^{1/\beta}.\(^{42}\) Since shadow masking results in up to 5% variation in the capacitor areas, the average area of each sample was directly confirmed by optical contrast imaging (Supporting S4 and Table S2). A Weibull plot of all 210 area-scaled sample-1 data also fits well to a straight line ($r^2 > 0.9$) as shown in Fig. 3b. However, area-1 capacitors show a larger $\beta$ (103) than area-2 (27.3) and area-3 (29) devices, possibly due to the spatial distribution of breakdown locations having a characteristic length scale. Also note that the $V_{BD}$ distribution of the area-1 capacitors has multiple values of $V_{BD}$ that are identical within experimental error (within 0.01 V), which results in an artifact of infinite slope and thus an overestimated $\beta$.

To quantify the positive effect of PTCDA seeding on reliability and dielectric strength, we also consider a control sample (control-2) consisting of the same oxide stack as sample-1 (8 nm HfO$\text{$_2$}$ + 2 nm Al$_2$O$_3$) grown directly on EG-SiC without PTCDA (Fig. 3c). The area-scaled Weibull plot (Fig. 3d) of $V_{BD}$ for control-2 shows that the $V_{BD}$ distribution does not scale with area. The extracted $\beta$ from the majority of the data ($>90\%$, excluding low-voltage tails) is 0.96 for area-1 and 0.98 for area-3, although $\beta = 1$ falls within the 95% confidence bounds (Supporting Table S2). Note that 10% of the control-2 capacitors still break down at an electric field greater than 4 MV/cm. Therefore, even though direct ALD growth on graphene can
produce isolated operational devices, a seeding layer is needed to achieve $\beta > 1$ (i.e., large-area uniformity) and large breakdown fields.

We also explored how PTCDA-seeded ALD dielectrics on graphene compare with ALD oxides on Si substrates. To address this issue, we conducted a breakdown study of capacitors (Fig. 2a) on Si substrates (control-1). Control-1 $V_{BD}$ data follow a Weibull distribution and scale well with area (Supporting S4). Area-scaled $E_{BD}$ distributions of all samples (sample-1, -2, -3) and controls (control-1, -2) are displayed together in the Weibull plot of Fig. 4a. The atomically thin PTCDA seeding layer shifts the $E_{BD}$ distributions of all three samples from control-2 close to control-1; i.e., the PTCDA seeding increases the dielectric strength by more than an order of magnitude ($\alpha(E_{BD}) = 0.45$ MV/cm for control-2, whereas $\alpha(E_{BD}) = 6.83 - 7.31$ MV/cm for the three PTCDA-seeded samples) and remains only 15% lower than control-1 ($\alpha(E_{BD}) = 8.17$ MV/cm). In addition, PTCDA contributes to a significant increase in large-area dielectric uniformity ($\beta > 25$ for sample-1, $\beta \leq 1$ for control-2).

For an overall assessment of dielectric quality, uniformity and dielectric strength should be analyzed concurrently with capacitance. Dielectric capacitance ($C$) and dielectric strength ($V_{BD}$) determine the largest reversible modulation of carrier concentration ($n$) in the semiconductor channel ($n = C(V_{BD} - V_{Interface})/e = \kappa\varepsilon_0 E_{BD}/e$; $e =$ electronic charge, $\varepsilon_0 =$ vacuum permittivity). Thus, the intrinsic dielectric property is the maximum displacement field (scale parameter $D_{max} = \kappa\varepsilon_0\alpha(E_{BD})$). Note that although capacitance can also be increased by thinning the dielectric, surface roughness and defects in the EG-SiC wafers limited the thickness to approximately 10 nm (Supporting S3), which is significantly thicker than the fundamental limits of quantum mechanical tunneling (~1 nm).
We now discuss the role of vertical heterogeneity in the oxide stack in relation to enhancing the dielectric performance metrics. Fig. 4b shows zoomed-in $E_{BD}$ distributions of area-3 capacitors on samples-1, -2, and -3 from Fig. 4a (see Supporting S4 for area-scaled Weibull plots of sample-2 and -3). Uniformity of sample-1 (95% confidence bounds of $\beta$: 23.8 – 35.3) is higher than both sample-2 ($\beta$: 17.0 – 25.5) and sample-3 ($\beta$: 9.5 – 16.5). Although the effective dielectric strength scale parameter ($\alpha(E_{BD})$) of sample-1 is only marginally greater than those of sample-2 and sample-3, the occurrences of “leaky capacitors” as soon as measurements were begun is significantly smaller in sample-1 (<1%) than sample-2 (>10%) and sample-3 (>17%) (Supporting S3 and Table S2). In addition, the sample-3 dielectric was found to be mechanically fragile and showed a tendency to peel off during probing. Therefore, we conclude that PTCDA seeds ALD growth of $\text{Al}_2\text{O}_3$ more effectively than $\text{HfO}_2$ on graphene, which was also suggested by microscopy analysis in a previous study.\textsuperscript{39} Owing to the 2x greater $\kappa$ value for $\text{HfO}_2$ versus $\text{Al}_2\text{O}_3$, sample-1 also shows a larger value of $D_{\text{max}}$ (6.02 $\mu\text{C/cm}^2$) than sample-2 (3.32 $\mu\text{C/cm}^2$), see Supporting Table S1. Note that the Schottky contact between the SiC substrate and the ground probe may introduce a uniform shift in the scale parameters of the samples, although the shape parameters are unaffected by a constant shift in $V_{BD}$.

Empirically, the dielectric constant and breakdown fields of oxide dielectrics are known to exhibit an inverse relationship.\textsuperscript{52} From that perspective, we highlight two surprising observations. First, in spite of higher effective $\kappa$, sample-1 shows higher uniformity ($\beta$), larger dielectric strength ($\alpha(E_{BD})$), and a significantly reduced fraction of “leaky capacitors” compared to sample-2. This observation suggests that a sequential ALD growth of two different oxides likely interferes with pin-hole formation, perhaps through misalignment of randomly distributed pin-holes in each of the two different layers. Therefore, the attractive attributes of sample-1 may
originately not only from advantageously tailored chemistry but also from the physical aspects of vertical heterogeneity. Second, in spite of the 13% smaller capacitance of sample-1 versus sample-3, $D_{\text{max}}$ of sample-1 is only 6% lower than that of sample-3. The greater $a(E_{\text{BD}})$ and $D_{\text{max}}$ values of sample-1 can be attributed to the interfacial $\text{Al}_2\text{O}_3$ layer in sample-1 that has a larger band-gap (8.8 eV), larger band-offset, and larger breakdown strength than $\text{HfO}_2$ in sample-3. These results are in agreement with experimental reports that have demonstrated improved characteristics in Si devices that utilize $\text{Al}_2\text{O}_3 + \text{HfO}_2$ oxide stacks in place of $\text{HfO}_2$ alone. The improved uniformity and breakdown strength of sample-1 is also consistent with surface morphology analysis of the samples via atomic force microscopy (Supporting S5).

In conclusion, we have addressed large-area reliability and breakdown limits of gate dielectrics grown on graphene. A molecularly thin organic seeding layer, PTCDA, leads to significant improvements in dielectric performance limits (e.g., increasing the Weibull scale parameter and shape parameter in the $E_{\text{BD}}$ distribution by more than an order of magnitude) for ALD-grown oxides on graphene. Furthermore, we find that vertically heterogeneous oxide stacks provide additional advantages from the perspectives of large-area homogeneity and maximum displacement field. In particular, a 2 nm thick interfacial $\text{Al}_2\text{O}_3$ layer is shown to enable robust ($\beta > 1$) growth of high-κ $\text{HfO}_2$, thus achieving a high breakdown field of $>7$ MV/cm at the highest capacitance (785 nF/cm$^2$) thus far reported on large area epitaxial graphene substrates. These results, coupled with the ability of PTCDA-seeded ALD top dielectrics to yield competitive graphene field-effect transistors (see Supporting S6), present clear future opportunities for graphene-based large-scale integrated circuits.
Figure 1. (a) High-resolution scanning tunneling microscopy (STM) image of a PTCDA monolayer on epitaxial graphene on SiC. (b) PTCDA molecular structure and the four different sample structures consisting of different combinations of Al₂O₃ and HfO₂ layers. Color codes for the materials (black box) and samples are retained throughout all figures. (c) Square capacitors of three different areas (area-1: 20 µm x 20 µm, area-2: 50 µm x 50 µm, and area-3: 80 µm x 80 µm) fabricated on each sample. (d) Schematic of an array of capacitors on a large area dielectric. (e) Capacitance-voltage curves of sample-1, sample-2, sample-3, and sample-4 at a frequency of 1 kHz. Data points are the average of 5 capacitors, and the error bars represent standard deviations. The black lines are fit to the quantum capacitance model (Supporting S2). The solid horizontal lines represent the extracted capacitances of the oxide stacks in each of the samples.
Figure 2. (a) Schematic of control-1 capacitors on an n-doped Si substrate. (b) Current density versus electric field (J-E) characteristics of sample-1 and control-1 capacitors. The solid and the dashed lines correspond to the capacitor in the middle and capacitors on the extremes of the Weibull distribution, respectively. (c) Schematic band-diagram of a control-1 capacitor when the Au electrode is biased to a positive voltage. (d) Schematic band-diagram of a sample-1 capacitor. Note that n-doped graphene on SiC forms a Schottky junction, which presents an additional tunnel barrier for the leakage current.
Figure 3. (a) Weibull plot of the breakdown voltage ($V_{BD}$) distribution for sample-1 capacitors. The number of data points for area-1, area-2, and area-3 are 74, 66, and 70, respectively. The dashed lines represent 95% confidence bounds. Linear fits (black lines) are performed on the majority of the data (excluding low-voltage tails) to extract Weibull parameters. (b) Weibull plot of the sample-1 $V_{BD}$ data after scaling to a common area of 1 mm$^2$. (c) Schematic of control-2 capacitors fabricated on EG-SiC without PTCDA. (d) Weibull plot of control-2 $V_{BD}$ data after scaling to a common area of 1 mm$^2$. Linear fits (solid lines) are performed on the majority of the data (excluding low-voltage tails) to extract Weibull parameters.
Figure 4. (a) Weibull plot of the breakdown fields $E_{BD}$ (V/cm) for the three samples and two controls. $E_{BD}$ data of area-3 capacitors on each sample were scaled to a common area of 1 mm$^2$. (b) The same Weibull plot is displayed over a narrower $E_{BD}$ range to compare the $E_{BD}$ distribution for sample-1, sample-2, and sample-3.
ASSOCIATED CONTENT

Supporting Information. Detailed description of graphitization of SiC; deposition of PTCDA; Raman analysis; atomic layer deposition of dielectrics; quantum capacitance modeling and capacitance-voltage analysis; dielectric breakdown measurements and reliability analysis of all samples and controls; two tables of Weibull parameters; atomic force microscopy analysis; top-gated graphene field-effect transistors. This material is available free of charge via the Internet at http://pubs.acs.org.

AUTHOR INFORMATION

Corresponding Authors

*Emails: t-marks@northwestern.edu; lauhon@northwestern.edu; m-hersam@northwestern.edu

Present Addresses

# Department of Materials Science and Engineering, Johns Hopkins University, Baltimore, MD, 21218

Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

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