Voltage-mode ultra-low power four quadrant multiplier using subthreshold PMOS

Xin Xin, Jueping Cai\textsuperscript{a)}, Ruilian Xie, and Peng Wang

State Key Laboratory of Wide Bandgap Semiconductor Technology Disciplines, Xidian University, Xi’an 710071, P.R. China
a) jpcai@mail.xidian.edu.cn

Abstract: A voltage-mode ultra low power four quadrant analog multiplier using subthreshold PMOS is presented in this paper. PMOS subtract cell and combiner cell operating in the subthreshold region are used to lower the voltage-mode multiplier power consumption. Simulation results of the multiplier demonstrate a linearity error of 0.8\%, a maximum THD of 4\%, a −3 dB bandwidth of 1.4 MHz, and a power consumption of 77 nW with 100 fF load capacitor at a supply voltage of 0.6 V using a TSMC 0.18 um CMOS process.

Keywords: voltage-mode multiplier, ultra-power, subthreshold

Classification: Integrated circuits

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1 Introduction

Commonly used in analog computational systems such as modulation, frequency doubling, rectification, and gain amplification, four quadrant multiplier especially focus on low power consumption performance [1, 2] for wireless sensor network chip. Driven by the early work of Gilbert which was implemented using BJT [3], many multipliers have been reported specially in CMOS technology based on the current mode and voltage mode topologies.

In current mode topologies, subthreshold analog multipliers [4, 5], based on the inherent log/anti-log cancellation technique, feature a larger dynamic range and a better linearity, but they requires five additional current sources, which make power consumption of them exceed nanowatt level. The class-AB four-quadrant current multiplier [6] has nanowatt power consumption in the condition of ultra low bandwidth. In voltage mode topologies, all transistors biased in saturated region [7] or part of the transistors biased in saturated region [8], the two multipliers can reduce supply voltage with a high bandwidth and a wide input range. But their power consumption is more than dozens of microwatt level. The subthreshold multiplier in [9] achieves several microwatt consumption if we accept using a large value for resistances, which will occupy a large area of the silicon. Meanwhile, a high precision current generation circuit is needed to reduce the bias current mismatch. The subthreshold analog multiplier in [10] suffers from poor total harmonic distortion (THD), and could not operate at high frequency with bulk-driven technique. The performance metrics for multipliers include linearity, input range, chip area cost, power consumption, bandwidth and noise. Depending upon applications, some of them can be more important than others. Also, it is not uncommon that some metrics need to be traded for others.

In this paper, we present a multiplier based on voltage mode topologies with emphasis on low power consumption, subthreshold PMOS is used to reduce 1/f noise and avoid bulk effect compared with NMOS. Different from common low voltage multiplier with square-law function circuit and linear transconductor in [11], subtractor cell and combiner cell are applied in the proposed voltage mode multiplier, and diode-connected PMOS is used to convert the output current to output voltage in the combiner cell, which can reduce chip area significantly. Because of only two transistors stacked in the supply voltage path, the proposed multiplier enables an operation at a low supply voltage. Simulation results show
that its power consumption is only 77 nW with 1.4 MHz bandwidth at 0.6 V supply voltage.

The rest of this paper is organized as follows: Section 2 presents the basic cells and the proposed multiplier with subthreshold PMOS. Section 3 describes the nonlinearity and mismatch analysis. In Section 4, simulation results are presented. Finally, Section 5 concludes this paper.

2 Circuit implementation

2.1 Basic cell

The drain current for a PMOS transistor in subthreshold region is given as [4]

\[
I_D = I_{D0} \exp \left( \frac{V_{SG} + (n - 1)V_{SB}}{nU_T} \right) \left( 1 - \exp \left( \frac{V_{SD}}{U_T} \right) \right)
\]

where \( I_{D0} = 2n\mu_C(W/L)VT^2 \) is the leakage current, \( n \) is the slope factor and \( U_T \) is the thermal voltage. For \( V_{DS} > 4U_T \), current \( I_D \) is almost independent of \( V_{SD} \).

Inspired by the subtractor cell and combiner cell operating in the saturation region [12], every PMOS transistor of these two cells shown in Fig. 1(a) and Fig. 1(b) is biased in the subthreshold region, whose bulk terminal is connected to its source terminal.

Consider the circuit in Fig. 1(a), the subtractor cell has two stacked PMOS whose source-drain current can be expressed as:

\[
I_{DX} = I_{D0} \exp \left( \frac{V_{DD} - V_X}{nU_T} \right)
\]

(2a)

\[
I_{DY} = I_{D0} \exp \left( \frac{V_Z - V_Y}{nU_T} \right)
\]

(2b)

Because PX transistor has the same source-drain current as PY transistor, \( V_Z \) can be achieved as (3) with an initial assumption of matched devices.

\[
V_Z = V_Y - V_X + V_{DD}
\]

(3)

Refer to Fig. 1(b), it can be seen that the drain and source terminals of P1 and P2 are connected to each other and the input voltages \( V_1 \) and \( V_2 \) control the drain currents which are summed in the diode-connected PMOS [2]. The output voltage of the combiner can be expressed as
\[
V_o = nU_T \ln \left( \exp \left( \frac{V_{DD} - V_1}{nU_T} \right) + \exp \left( \frac{V_{DD} - V_2}{nU_T} \right) \right)
\]

The advantage of using diode-connected subthreshold PMOS is to avoid using two large resistances which saves the chip area significantly.

### 2.2 The proposed multiplier

All PMOS transistors of the proposed multiplier, as shown in the Fig. 2, have the same size, and all of them are matched. The proposed multiplier comprises four subtractor cells and two combiner cells. Differential input voltages, defined by \( V_x = V_{x+} - V_{x-} \) and \( V_y = V_{y+} - V_{y-} \), are applied to input terminals of the four subtractor cells. Differential output voltages, defined by \( V_{out} = V_{o1} - V_{o2} \), are applied to output terminals of the two combiner cells.

Applying (4) to the circuit in Fig. 2, the two output voltages of the multiplier are

\[
V_{o1} = nU_T \ln \left( \exp \left( \frac{V_{DD} - V_{z1}}{nU_T} \right) + \exp \left( \frac{V_{DD} - V_{z2}}{nU_T} \right) \right) 
\]

\[
V_{o2} = nU_T \ln \left( \exp \left( \frac{V_{DD} - V_{z3}}{nU_T} \right) + \exp \left( \frac{V_{DD} - V_{z4}}{nU_T} \right) \right)
\]

Applying a Taylor series (retaining the first two terms only) to a general exponential function results in

\[
V_{o1} = nU_T \ln \left( 1 + \left( \frac{V_{DD} - V_{z1}}{nU_T} \right) + \frac{1}{2!} \left( \frac{V_{DD} - V_{z1}}{nU_T} \right)^2 \right) + 1
\]

\[
V_{o2} = nU_T \ln \left( 1 + \left( \frac{V_{DD} - V_{z3}}{nU_T} \right) + \frac{1}{2!} \left( \frac{V_{DD} - V_{z3}}{nU_T} \right)^2 \right) + 1
\]

if \( \frac{V_{DD} - V_{z1}}{nU_T} \ll 1 \), \( \frac{V_{DD} - V_{z2}}{nU_T} \ll 1 \), \( \frac{V_{DD} - V_{z3}}{nU_T} \ll 1 \) and \( \frac{V_{DD} - V_{z4}}{nU_T} \ll 1 \).

![Fig. 2. Proposed four quadrant multiplier.](image-url)
Similarly, applying a first order Taylor series to the function  \( \ln(1 + x_1 + x_2) \) results in

\[
V_{o1} = \left( \frac{V_{DD} - V_{z1}}{2} + \frac{(V_{DD} - V_{z1})^2}{4nU_T} + \frac{(V_{DD} - V_{z2})^2}{4nU_T} + \frac{(V_{DD} - V_{z2})^2}{2} \right) \cdot \ln 2
\]

(7a)

\[
V_{o2} = \left( \frac{V_{DD} - V_{z3}}{2} + \frac{(V_{DD} - V_{z3})^2}{4nU_T} + \frac{(V_{DD} - V_{z4})^2}{4nU_T} + \frac{(V_{DD} - V_{z4})^2}{2} \right) \cdot \ln 2
\]

(7b)

Subtracting (7a) into (7b), the differential output voltage of the multiplier arrives at

\[
V_{\text{out}} = V_{o1} - V_{o2} = -\frac{V_x V_y \ln 2}{2nU_T}
\]

(8)

Therefore, equation (8) implements a true four-quadrant voltage-mode multiplication function independent of device parameters. Since all PMOS transistors are biased in subthreshold, the power consumption can be ultra-low. Besides, there are only two transistors stacked in the supply voltage path, which enables an operation at low supply voltage.

### 3 Nonlinearity and mismatch analysis

The whole mismatch in the proposed multiplier can be analyzed by considering the higher order terms and variations due to the process parameters. Applying a Taylor series (retaining the first three terms) for the combiner cell results in

\[
V_{o1} = nU_T \ln \left( 1 + \frac{V_{DD} - V_{z1}}{nU_T} \right) + \frac{1}{2!} \left( \frac{V_{DD} - V_{z1}}{nU_T} \right)^2 + \frac{1}{3!} \left( \frac{V_{DD} - V_{z1}}{nU_T} \right)^3
\]

(9a)

\[
V_{o2} = nU_T \ln \left( 1 + \frac{V_{DD} - V_{z3}}{nU_T} \right) + \frac{1}{2!} \left( \frac{V_{DD} - V_{z3}}{nU_T} \right)^2 + \frac{1}{3!} \left( \frac{V_{DD} - V_{z3}}{nU_T} \right)^3
\]

(9b)

According to equation (9a) and equation (9b), equation (8) can be rewritten as

\[
V_{\text{out}} = -\frac{V_x V_y \ln 2}{2nU_T} - \frac{1}{3!} \frac{V_x V_y (V_{x_+} + V_{x_-} - V_{y_+} - V_{y_-})}{(nU_T)^2} \ln 2
\]

(10)

The third order and higher harmonics have a little effects on THD, since  \( V_{x_+} + V_{x_-} = 0 \) and  \( V_{y_+} + V_{y_-} = 0 \) for the differential input signals.

Besides the third order and higher harmonics, the leakage current  \( I_{D0} \) of the PMOS subthreshold region is proportional to the aspect ratio of PMOS transistors. If the aspect ratios of M1–M14 in Fig. 2 are mismatched due to the process variation, it would result in the leakage current  \( I_{D0} \) of M1–M14 to be not identical. The drain current of PX transistor and PY transistor shown in Fig. 1(a) can be expressed as
According to equation (13a) and equation (13b), and assume that

\[ \begin{align*}
I_{DX} &= I_{D0} \exp \left( \frac{V_{DD} - V_X}{nU_T} \right) \\
I_{DY} &= \delta_0 I_{D0} \exp \left( \frac{V_Z - V_Y}{nU_T} \right)
\end{align*} \]  

(11a)  

(11b)

\[ V_Z \] can be achieved by the following subtraction function

\[ V_Z = V_Y - V_X + V_{DD} - nU_T \ln \delta_0 \]  

(12)

Where \( \delta_0 \) is the mismatch factor between PX transistor and PY transistor. \( \delta_{0j} \) represents the mismatch factor between \( M_i \) and \( M_j \) transistor.

Assume that \( I_{D011} = \rho_1 \cdot I_{D09}, I_{D011} = \rho_2 \cdot I_{D010}, I_{D014} = \rho_3 \cdot I_{D012} \) and \( I_{D014} = \rho_4 \cdot I_{D013}, \) where \( \rho_1 \) and \( \rho_2 \) are the mismatch factors that the leakage current of \( M9 \) and \( M10 \) transistors is relative to \( M11 \) transistor’s respectively, while \( \rho_3 \) and \( \rho_4 \) are the mismatch factors that the leakage current of \( M12 \) and \( M13 \) transistors is relative to \( M14 \) transistor’s respectively. Then the two combiner cells shown in Fig. 1(b) can be expressed as:

\[ V_{o1} = nU_T \ln \left( \rho_1 \exp \left( \frac{V_{DD} - V_{z1}}{nU_T} + \ln \delta_{012} \right) + \rho_2 \exp \left( \frac{V_{DD} - V_{z2}}{nU_T} + \ln \delta_{034} \right) \right) \]  

(13a)

\[ V_{o2} = nU_T \ln \left( \rho_3 \exp \left( \frac{V_{DD} - V_{z3}}{nU_T} + \ln \delta_{056} \right) + \rho_4 \exp \left( \frac{V_{DD} - V_{z4}}{nU_T} + \ln \delta_{078} \right) \right) \]  

(13b)

According to equation (13a) and equation (13b), and assume that \( \rho_1 \approx \rho_2 \approx \rho_3 \approx \rho_4, \delta_{012} + \delta_{034} \approx \delta_{056} + \delta_{078}, \) and \( \rho_1 \delta_{012} + \rho_2 \delta_{034} \approx \rho_3 \delta_{056} + \rho_4 \delta_{078}. \) The output voltage of the proposed multiplier can be rewritten as

\[ V_{out} = V_{o1} - V_{o2} \approx - \frac{V_x V_y \ln(\rho_1 \delta_{012} + \rho_2 \delta_{034})}{nU_T (\delta_{012} + \delta_{034})} \]  

(14)

From Eq. 14, the mismatch in the devices will lead to the nonlinearity error. To avoid the nonlinearity error, careful layout consideration is necessary.

### 4 Simulation results and discussion

The proposed multiplier is simulated in Cadence using TSMC 0.18 um CMOS process \((V_{cp} = -437 \text{ mV})\). Input signals common-mode \(V_X = 0.3 \text{ V}, V_Y = 0 \text{ V}\) and a single supply voltage \(V_{DD} = 0.6 \text{ V}\) are set as design conditions. The devices are of equal size with \((W/L) 2.5 \text{ um}/0.18 \text{ um}\). The DC transfer characteristic is shown in Fig. 3(a) when the input voltage \(V_X\) varies from \(-50 \text{ mV}\) to \(50 \text{ mV}\) while the input voltage \(V_Y\) steps from \(-50 \text{ mV}\) to \(50 \text{ mV}\) by \(10 \text{ mV}\) step size. Similar characteristic for \(V_Y\) is obtained and is shown in Fig. 3(b). Multiplier is used as a balanced modulator, as shown in Fig. 4, where a \(100 \text{ mV}_{P-P}, 4 \text{ KHz}\) sinusoidal carrier signal \(V_x\) is multiplied by a \(100 \text{ mV}_{P-P}, 100 \text{ KHz}\) sinusoidal modulating \(V_y\). The dynamic nonlinearity is examined by THD with \(V_x\) as a \(100 \text{ KHz}\) sinusoidal signal and varying from \(10 \text{ mV}_{P-P}\) to \(100 \text{ mV}_{P-P}\), and \(V_y\) fixed at \(100 \text{ mV}_{P-P}\) or the anther case shown in Fig. 5 where the worst-case THD is less than \(4\%\).

Fig. 6(a) shows the corner case analysis of small signal response for the TT, SS and FF corners. This figure proves that the worst-case small signal bandwidth of the circuit is \(0.8 \text{ MHz}\) with \(100 \text{ fF}\) load capacitor. The multiplier works properly
even in the worst corners of technology. Fig. 6(b) shows the temperature is swept from $-20$ to $100\,\text{°C}$ when $V_x = 50\,\text{mV}_{\text{P-P}}$, and $V_y = 50\,\text{mV}_{\text{P-P}}$ and the reported deviation from the normalised output voltage is 0.12. As shown in Fig. 6(c), changing the supply voltage has negligible effect on the circuit. To test the robustness of the circuit under different process parameters deviation, Monte-Carlo analysis has been carried out for 200 samples. The nonlinearity error has been calculated by applying a DC voltage $V_x$ to $V_y$ and connecting an external gain stage with adjustable gain to the output, percentage of error obtain is 0.8%. The standard deviation found to be 0.92 MHz, 0.082% and 1.89% for $-3\,\text{dB}$ frequency, THD and linearity error shown in the Fig. 7 respectively. Moreover, the multiplier has advantage in power consumption and bandwidth as evident from Table I. The power consumption of the proposed multiplier is only 77 nW. Meanwhile, the proposed multiplier can be made to operate under a supply voltage of $V_{DD} = 0.6\,\text{V}$. 

![Fig. 3. The DC transfer characteristics.](image)

![Fig. 4. Transient response of the whole multiplier.](image)

![Fig. 5. Relation between THD, Vx and Vy](image)
A voltage-mode ultra low power four quadrant analog multiplier has been presented. Using PMOS substract cell and combiner cell in subthreshold, power consumption and complexity of the proposed multiplier can be reduced, meanwhile $-3$ dB bandwidth also can be widen, making it suitable for analogue VLSI circuits such as adaptive filters, phase locked loops and integrated fuzzy systems.

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**Table I.** Comparison of different multipliers

| Parameter | Technology | Supply | THD | Linearity error | Power | Bandwidth |
|-----------|------------|--------|-----|----------------|-------|-----------|
| [4]       | 0.18 um    | ±0.5 V | 1.22% | 3.5%            | 3 uW  | 4.5 MHz   |
| [5]       | 0.18 um    | ±0.6 V | 0.08% | 0.63%           | 1.16 uW | 1.5 MHz |
| [6]       | 0.13 um    | 0.65 V | 3.16% | -               | 12.4 nW  | <1 MHz   |
| [10]      | 0.18 um    | 0.5 V  | 5%   | 5.6%            | 714 nW  | 221 KHz  |
| This work | 0.18 um    | 0.6 V  | 4%   | 0.8%            | 77 nW   | 1.4 MHz  |

**Fig. 6.** Corner case analysis, temperature effect and supply voltage effect

**Fig. 7.** Monte Carlo process and mismatch analysis

a $-3$ dB frequency deviation
b THD deviation
c Non-linearity deviation

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**5 Conclusion**

A voltage-mode ultra low power four quadrant analog multiplier has been presented. Using PMOS substract cell and combiner cell in subthreshold, power consumption and complexity of the proposed multiplier can be reduced, meanwhile $-3$ dB bandwidth also can be widen, making it suitable for analogue VLSI circuits such as adaptive filters, phase locked loops and integrated fuzzy systems.