Parameter Conditions to Prevent Voltage Oscillations Caused by LTC-Inverter Hunting on Power Distribution Grids

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Abstract—As more distributed energy resources (DERs) are connected to the power grid, it becomes increasingly important to ensure safe and effective coordination between legacy voltage regulation devices and inverter-based DERs. In this work, we show how a distribution circuit model, composed of two LTCs and two inverter devices, can create voltage oscillations even with reasonable choices of control parameters. By modeling the four-device circuit as a switched affine hybrid system, we analyze the system's oscillatory behavior, both during normal operation and after a cyber-physical attack. Through the analysis we determine the specific region of the voltage state space where oscillations are possible and derive conditions on the control parameters to guarantee against the oscillations. Finally, we project the derived parameter conditions onto 2D spaces, and describe the application of our problem formulation to grids with many devices.

I. INTRODUCTION

The traditional voltage regulation problem is to design load-tap changer (LTC), voltage regulator, and capacitor bank control parameters such that, over a minutes-to-day duration, the distribution grid voltage is kept within 5\% of the nominal voltage (ANSI C84.1 standard) to avoid interrupting or damaging customer equipment. The addition of naively controlled DERs such as solar PV makes this voltage regulation problem harder [1] and can cause LTCs to actuate much more frequently, reducing their lifespan. Depending on the control logic and design parameters, connecting smart inverters can either alleviate [2] these voltage fluctuations or be a source of adverse interactions [3].

One type of adverse interaction is device hunting which we define as one or more devices actuating in a repeated sequence that results in periodic voltage oscillations. Hunting among LTCs has been observed by utilities since the 1980s [4], [5] and has been modeled as a hybrid system in the literature [5]. Inverter-based DERs may be able to solve these problems if their control parameters are set appropriately. However, current inverter standards [6] require inverter control parameters to be adjustable by a remote entity’s communication network, which introduces a potential vulnerability to cyberattacks [7]. Bad parameters sent to inverters on a circuit, whether deliberately or by mistake, can trigger adverse interactions [8]. This motivates our investigation into how a poor choice of device parameters can lead to hunting, as simulated in Fig. 1.

Related work: There are two common approaches when selecting distribution-grid device parameters for voltage control: an approach based on rules of thumb followed by simulation, and an optimization-based approach. For basic operation of LTCs and parameter rules of thumb we refer to the text [9, Chapter 9.3], and to papers [1], [10]. One limitation of this approach is the assumed timescale separation between the LTC and inverters, which may not hold when LTCs delays are shortened to handle increased voltage variability [11]. Moreover, the simulations in these papers are not sufficient to guarantee against the possibility of sustained voltage oscillations.

Meanwhile, optimization methods focus on addressing the non-convexity of the mixed-integer optimal power flow problem resulting from including both continuous (smart inverter) and discrete (LTC and voltage regulator) dynamics [12], [13]. However, the optimal parameter solution determines tap positions and power dispatch rather than the device parameters in the control law. As such, the optimal solution does not provide significant insights into the symbolic relationship between control parameters and adverse interactions.

Our goal of deriving symbolic parameter conditions for hybrid systems stability is a challenging task and remains relatively unexplored in control systems literature. The design of switching strategies for stabilization commonly assumes one can switch modes at any time, rather than switching according to parameterized conditions [14], [15]. Linear parameter variation (LPV) literature commonly assumes the parameters to be time-varying, but here our parameters are time-independent and we want to solve for them symbolically [16]. Therefore, our methodology leverages our...
familiarity with the specific system’s model dynamics.

**Paper contribution:** We seek to analyze how parameters of LTCs and inverters prevent or contribute to voltage oscillations created by device hunting. The results yield two distinct benefits: (i) the parameter conditions can provide intuition for improving the rules of thumb used to operate these devices in industry and (ii) the conditions can be directly checked on each device without simulations, enabling real-time checks on incoming parameter updates by remote entities.

**Paper Organization:** The remainder of the paper is organized as follows. In Sec. II, the system equations are presented and the parameter condition problem is solved for two subsystems. In Sec. III, the parameter condition problem is solved for the full system. In Sec. IV, the conditions on the full system conditions are illustrated. In Sec. V, we present conclusions and future work. We include proofs of the main theorem and lemmas in-line, and refer readers to the appendix for the minor proofs.

II. SYSTEM DYNAMICS AND SUBSYSTEM ANALYSIS

A. Notation

Let $\mathbb{R}^c$ be the c-dimensional vectors of real numbers. Given a time-varying vector $x$, we let $x[k]$ be its value at time $k$, and $x_i[k]$ be the value of the i-th element of $x$ at time $k$. Let $x^T$ be the transpose of vector $x$. Let $||.||_i$ denote the $\ell_i$ vector norm for $i = 1, 2, \infty$. We define the margin $M(S, d)$ as the set of points $x$ that are within distance $d$ from a set $S$. That is, $M(S, d) := \{ x \notin S : \exists s_j \in S : \| x - s_j \|_2 \leq d \}$. We define a partition of a set $S$ to be a collection of subsets $S_i$, $i = 1, \ldots, k$ such that $\bigcup_{i=1}^{k} S_i = S$ and $S_i \cap S_j = \emptyset$ for all $i \neq j$. We use $\rightarrow$ and $\rightarrow$ to indicate possible and impossible transitions between partitions, respectively. Let $S'$ denote the complement of set $S$, and $S \setminus Q$ be the part of the set $S$ that is not in $Q$.

B. Overview of Four-Device System

![Fig. 2: Distribution circuit with LTC and inverter devices](image)

We model four devices operating on the radial circuit shown in Fig. [2]. Suppose there are constant loads at all nodes shown. LTC1 and inverter1 regulate voltage $v_1$, while LTC2 (sometimes called a line voltage regulator) and inverter2 regulate voltage $v_2$. We let $v_{\text{diff}} := v_1 - v_2$. The LTCs estimate these voltages using line drop compensation, and the inverters measure these voltages with their internal sensors. All devices operate with fixed time delay logic; that is, they only respond when the voltage remains outside the deadband for a certain delay $d$. We denote the upper deadband boundary as $v^+ = v^{ref} + \varepsilon$, and lower deadband boundary as $v^- = v^{ref} - \varepsilon$. Then we define the deadband

$$D := \{(v_1, v_2) : v^- \leq v_1 \leq v^+, \; v^- \leq v_2 \leq v^+\}. \quad (1)$$

Because there are no active dynamics when both voltages are in the deadband, the set $D$ is invariant. When $v_i > v^+$ we say $v_i$ has an overvoltage, and when $v_i < v^-$ we say $v_i$ has an undervoltage. With the shorthand $v_i \in D$ or $v_i \notin D$, we refer to whether $v^- < v_i < v^+$ is satisfied or not.

Next, we define normal operating $W := (H \cap P)$ where

$$H := \{(v_1, v_2) : (v_1 > v^- \text{ and } v_2 > v^+) \text{ or } (v_1 < v^- \text{ and } v_2 < v^+)\}$$

$$P := \{(v_1, v_2) : \|v[k] - v^{ref}\|_\infty < 3\varepsilon\}. \quad (3)$$

The hourglass-shaped set $H$ disallows one voltage from being above $v^+$ when the other is below $v^-$. $P$ bounds the distance each voltage can be away from $v^{ref}$.

**Assumption 1. (normal operation) A given system $\Sigma$ operates in normal operating states $W$ defined by (2) and (3).**

We consider states outside $W$ to be abnormal operating conditions that should be addressed with the grid’s protection system rather than the system dynamics analyzed in this work. We are interested in the system behavior while $v \in W$, especially if the initial condition (IC) starts in $W$ and eventually leaves $W$.

The goal is to coordinate the device actions so that $v_1$ and $v_2$ land inside the deadband without device hunting. Table I summarizes the notation for the states, fixed parameters, and symbolic parameters we are interested in designing to guarantee against hunting. The table also assumes relationships from basic operation of power systems that are drawn from [9, Chapter 9.3] and [17]. In the table, all fixed and symbolic variables except for $g$ are taken to be positive and real valued due to their physical meaning.

| type | description | default | relationship |
|------|-------------|---------|--------------|
| $v^{ref}$ | voltage ref. (p.u.) | 1.0 | - |
| $\varepsilon$ | half of deadband width | 0.1 | - |
| $v^-$. $v^+$ | deadband boundary | 0.95, 1.05 | $v^- = v^{ref} - \varepsilon$, $v^+ = v^{ref} + \varepsilon$ |
| $\chi$ | line reactance to the substation (p.u.) | 0.1 | - |
| $\eta$ | impedance damping factor | 0.9 | $0 < \eta < 1$ |
| $v_{10}$ | state node 2 initial voltage (p.u.) | 1.04 | - |
| $v_{20}$ | state node 3 initial voltage (p.u.) | 0.94 | - |
| $d_{inv}$ | symbolic inverter 1 and 2 delay (s) | 4 | $d_{inv} < d_{L1}$ |
| $d_{L1}$ | symbolic LTC1 delay (s) | 30 | - |
| $d_{L2}$ | symbolic LTC2 delay (s) | 40 | $d_{L1} < d_{L2}$, $d_{L2} < 2d_{L1}$ |
| $v_{L}$ | symbolic tap voltage (p.u.) | 0.03 | $v_L < 2\varepsilon$ |
| $g$ | symbolic inverter 1 and 2 control gain | - | - |

C. Conditions for two-LTC System

Let the $\Sigma_1$ be the subsystem where LTC1 and LTC2 operate on the circuit in Fig. [2] normally (see Assumption 1). Both devices have the same deadband width $2\varepsilon$ that
is centered on the same voltage reference \( v^{ref} \). When the voltage is outside the deadband for \( d_{L1} \) (\( d_{L2} \)) seconds, LTC1 (LTC2) taps, which updates both voltages according to \( v[k+1] = v[k] \pm [\bar{v}_L, \bar{v}_L] \) where \( v = [v_1, v_2]^T \in \mathbb{R}^2 \). Because all tap actions shift both voltages by \( \bar{v}_L \) amount, tapping manifests as discrete jumps on the \((v_1, v_2)\) space with slope of \( \pm 1 \) between the initial and after-tap voltage.

**Lemma 1.** If \( \bar{v}_L > 2\varepsilon \), system \( \Sigma_1 \) will have marginally stable oscillations for all time when any \( v_1[0] \in M(D, c) \) or \( v_2[0] \in M(D, c) \) where \( c = \bar{v}_L - 2\varepsilon > 0 \).

Distribution engineers know not to set \( \bar{v}_L > 2\varepsilon \) when choosing LTC settings, so next we focus on how oscillations could occur when \( \bar{v}_L \leq 2\varepsilon \).

We partition \( W \) into four regions \( D, W_o, W_b, W_a \), based on the possible trajectories from starting the system in each region. We define \( W_o \) such that from there we only transition to the deadband or oscillate. For example, \( v_1 \) should satisfy \( v_1 - \bar{v}_L < v^+ \). Therefore we define the boundary of \( W_o \) in terms of the \( v_i^* \) that satisfies \( v_i^* - \bar{v}_L = v^+ \) for \( i = 1, 2 \). This gives the regions

\[
W_o = \{(v_1, v_2) \in W : (v_1 \in M(D, v_1^* - v^+) \text{ and } v_2 \in D), \text{ or } (v_2 \in M(D, v_2^* - v^+) \text{ and } v_1 \in D)\}
\]

(4a)

\[
W_b = \{(v_1, v_2) \in W : (v_1, v_2) > v^+ \text{ and } v_1 + v_2 \leq v^+ + \bar{v}_L), \text{ or } (v_1, v_2) < v^- \text{ and } v_1 + v_2 \geq v^- - \bar{v}_L)\}
\]

(4b)

and \( W_g \) is what remains of \( W \) \((W_g = W \setminus (D \cup W_o \cup W_b))\).

\[\]

**Lemma 2.** If \( \bar{v}_L \leq 2\varepsilon \), \( v[T] \in W_o \), and \( v^{diff} < 2\varepsilon - \bar{v}_L \), system \( \Sigma_1 \) will have marginally stable oscillations starting at time \( T \).

\[\]

A simulation of marginally stable oscillations due to Lemma 2 hunting is in Fig. 4.

\[\]

Fig. 4: Simulation of system \( \Sigma_1 \) when Lemma 2 holds. Parameters are the defaults listed in Table 1.

**D. Conditions for 2-Inverter System**

Let the \( \Sigma_2 \) be the subsystem where the two inverters operate on the circuit in Fig. 2 normally (see Assumption 1). For now we omit the deadband in the control logic. We employ a discrete integrator (also called incremental volt-var control in [17], [18]) for computing inverter reactive power set-points \( q^{inv} \) with

\[
q^{inv}[k+1] = q^{inv}[k] - G(v[k] - v^{ref}),
\]

where \( v^{ref} \in \mathbb{R}^n \) is the reference voltage, and \( G \) is a diagonal matrix containing controller gains. Because only a subset of the network nodes are controlled, \( v^{ref} \) can be assigned to the nominal vector of ones. \( G \) being diagonal enforces that each inverter is injecting power to regulate the voltage at its own node. For any radial circuit with \( n \) inverters at different nodes, \( v \in \mathbb{R}^n \) and \( q^{inv} \in \mathbb{R}^n \).

The algebraic power flow equations that map inverter power injections to voltages can be represented by

\[
v[k+1] = v[k] + X(q^{inv}[k+1] - q^{inv}[k])
\]

from [19, equation 8]. Matrix element \( X_{ij} \) is the common ancestor path reactance between node \( i \) and node \( j \) on the network. Next we substitute (5) into (6), giving

\[
v[k+1] = v[k] - XG(v[k] - v^{ref}).
\]

Finally, we subtract \( v^{ref} \) from both sides and define \( e[k] := v[k] - v^{ref} \), giving [19, equation 12]:

\[
e[k + 1] = (I - XG)e[k].
\]

Author [19] proves in their Theorem 3.1 that for the system \( v \to v^{ref} \) iff

\[
0 < G < 2X^{-1}.
\]

In the scalar case (one inverter acting on a single phase circuit), this condition is \( 0 < g < 2/\chi \). This implies that under normal operation, \( g \) should be positive but not too large to have the voltages converge. We are also interested in the possibility of \( g < 0 \), where the inverters push the voltage away from \( v^{ref} \), because that case is more dangerous.

**Lemma 3.** If \( G < 0 \), system \( \Sigma_2 \) given by (8) has \( v \to \pm \infty \).
When the deadband is introduced, inverters only operate according to (5) when their voltage is outside the deadband.

Because $v^{ref}$ is centered in the deadband, Lemma 3 holds in the same way as the no-deadband case, and the convergence condition (9) yields $v \to D$ instead of $v \to v^{ref}$.

For our system $\Sigma_2$, $G = \text{diag}([g \ g])$ and $q = [q_1 \ q_2]$. The dissipative nature of power grids due to line impedances causes the diagonal terms of $X$ to be larger than the off-diagonal terms. From the circuit in Fig. 2, system $\Sigma_2$ has

$$X = \begin{bmatrix} \chi & \eta \chi & \chi \end{bmatrix},$$

where the damping factor $\eta$ satisfies $0 < \eta < 1$. In general, if inverters have different reactances in the line path to the substation, $\eta_1 = X_{21}/X_{11}$ and $\eta_2 = X_{12}/X_{22}$. Because in this work we only use $\eta$ for its property of $0 < \eta < 1$, using $\eta = \eta_1 = \eta_2$ does not change the results.

### III. Full System Analysis

#### A. Modeling the Four Devices as a Hybrid System

Next we model all devices in Fig. 2 (except Assumption 1) as a discrete hybrid automaton, which is the interconnection of a finite state machine with a switched affine system. This system, $\Sigma_3$, has state vector $x = [z_1 \ z_2 \ z_3 \ v_1 \ v_2]^T$, where $z_1, z_2, z_3$ are the internal timers for LTC1, LTC2, and inverter1 and 2, respectively. The two inverters use the same timer $z_3$ because they have the same delay of $d_{inv}$. Let $T_s$ be the time step of the discrete model. Each mode has a label with the format $m \times 0$ where $* = 1, 2, ... 8$, and has affine dynamics of the form $x[k+1] = Ax[k] + c$ where $A \in \mathbb{R}^{5 \times 5}$ and $c \in \mathbb{R}^5$. To define the switching conditions, we define a function $f$ for whether a voltage is inside the deadband:

$$f_i := \max(v_i - v^+, 0) - \max(v^- - v_i, 0) \quad \text{for} \quad i = 1, 2, 3 \quad (11)$$

For $i = 1, 2$, if $v_i$ is an overvoltage then $f_i > 0$. If it is an undervoltage then $f_i < 0$, and if inside $D$ then $f_i = 0$. Inverter1 (LTC1) responds when $f_1 \neq 0$ for $d_{inv} (d_{L1})$ seconds, and Inverter2 (LTC2) responds when $f_2 \neq 0$ for $d_{inv} (d_{L2})$ seconds.

Now we introduce the hybrid model, where we make the symbolic variables bold:

- **m10**: tap LTC1 up
  
  Switch condition: $z_1 > d_{L1}$ and $(f_1 + f_2 < 0)$
  
  Dynamics:
  
  $$\begin{bmatrix} z_1 \\ z_2 \\ z_3 \\ v_1 \\ v_2 \end{bmatrix}_{k+1} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} z_1 \\ z_2 \\ z_3 \\ v_1 \end{bmatrix}_k + \begin{bmatrix} T_s \\ T_s \\ T_s \\ \bar{v}_L \end{bmatrix}$$

  m20 (tap LTC1 down) is the same as m10 except the condition has $(f_1 + f_2 < 0)$ and the affine term is $[T_s \ T_s \ T_s \ -\bar{v}_L \ -\bar{v}_L]^T$.

- **m30**: tap LTC2 up
  
  Switch condition: $z_2 > d_{L2}$ and $(f_1 + f_2 < 0)$
  
  Dynamics:
  
  $$\begin{bmatrix} z_1 \\ z_2 \\ z_3 \\ v_1 \\ v_2 \end{bmatrix}_{k+1} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} z_1 \\ z_2 \\ z_3 \\ v_1 \end{bmatrix}_k + \begin{bmatrix} T_s \\ T_s \ end{bmatrix}$$

  m40 (tap LTC2 down) is the same as m30 except the condition has $(f_1 + f_2 < 0)$ and the affine term is $[T_s \ T_s \ T_s \ -\bar{v}_L \ -\bar{v}_L]^T$.

- **m50**: inverter(s) respond to voltage issues
  
  Switch condition: $z_3 > d_{inv}$ and $(f_1 \neq 0 \ or \ f_2 \neq 0)$
  
  Dynamics:
  
  $$\begin{bmatrix} z_1 \\ z_2 \\ z_3 \\ v_1 \\ v_2 \end{bmatrix}_{k+1} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} z_1 \\ z_2 \\ z_3 \\ v_1 \end{bmatrix}_k + \begin{bmatrix} T_s \\ T_s \ \chi g v^{ref} + s \chi g v^{ref} + \chi g v^{ref} \end{bmatrix}$$

  m60: reset LTC2 and inverter timers
  
  Switch condition: $(m = m10 \ and \ (f_1 > 0 \ or \ f_2 > 0))$ or $(m = m20 \ and \ (f_1 < 0 \ or \ f_2 < 0))$
  
  Dynamics: $z_2[k+1] = T_s, \ z_3[k+1] = T_s, \ v[k+1] = v[k]$

- **m70**: reset LTC1 and inverter timers
  
  Switch condition: $(m = m30 \ and \ (f_1 > 0 \ or \ f_2 > 0))$ or $(m = m40 \ and \ (f_1 < 0 \ or \ f_2 < 0))$
  
  Dynamics: $z_1[k+1] = T_s, \ z_3[k+1] = T_s, \ v[k+1] = v[k]$

- **m80**: increment timers
  
  Switch condition: no other mode conditions hold
  
  Dynamics: $z_i[k+1] = z_i[k] + T_s \forall i = 1, 2, 3, \ v[k+1] = v[k]$

**Remark 1.** By the relationship $d_{inv} < d_{L1} < 2d_{L2}$ from Table 1, the inverters respond to voltage issues before LTC1. This relationship is a less conservative version of $d_{inv} < d_{L1}$, which is often made for power systems [1]. Therefore, an LTC will never tap twice before an inverter acts.

**B. Behavior when $g > 0$**

For positive values of the inverter gain $g$, our control action renders the voltage dynamics stable, as shown next.

**Proposition 1.** If system $\Sigma_3$ has $0 < g < \frac{2}{\chi},$ there exists $T > 0$ such that $v[k] \in D$ for all $k \geq T$.

**Proof.** We give an intuitive sketch of the proof through a Lyapunov function. We notice that when $g = 0$ circuit $\Sigma_3$ behaves equivalently to $\Sigma_1,$ Lemma 2 establishes that if $\bar{v}_L < 2\varepsilon,$ then the system exhibits marginally stable oscillations (recall Fig. 4). This implies that the energy of the system
$Y_k$ remains positive and bounded by fixed values $\bar{Y}_1$ and $\bar{Y}_2$, i.e., $0 < Y_1 < Y_k < Y_2 < \infty$, when $g = 0$.

Now if we consider a positive gain $0 < g < 2/\chi$ in $\Sigma_3$, equation (9) guarantees that the inverter acts as a stabilizing controller during mode m50, decreasing the system energy and driving $v$ closer to the deadband. Finally, from Remark[1] we know that because of the conditions on the timers, we will always return to m50 regularly, at least once between each LTC controller during mode m50, decreasing the system energy equation (9) guarantees that the inverter acts as a stabilizing controller during mode m50, decreasing the system energy and driving $v$ closer to the deadband. Finally, from Remark[1] we know that because of the conditions on the timers, we will always return to m50 regularly, at least once between each LTC tap. Therefore, the system $\Sigma_3$ has maximum energy of $\bar{Y}_2$ and will only lose energy until landing in the deadband.

The consequence of Lemma[1] is that for realistic values of the network with $g > 0$, the system exhibits damped oscillations which eventually reach the deadband. Thus, we focus the remainder of this paper on the more dangerous scenario where $g < 0$ renders the oscillations unstable.

C. Trajectory Walkthrough for $g < 0$

![Fig. 5: Simulation of system $\Sigma_3$ for $g < 0$ with parameters being the defaults in Table 1 System start time is at $k_0$.](image)

Here, we describe a scenario on system $\Sigma_3$ that can result in the beginning of unstable oscillations. Suppose an adversary gains access to and installs malware in the communication system that remotely sends parameters to the inverters. The malware logic could, for example, send a negated inverter controller gain $g$ when any of the inverter voltages suddenly change substantially $|v[k+1] - v[k]| > 0.6\varepsilon$, and the voltage lands far from $v^{ref}$ $|v[k+1] - v^{ref}| > 0.6\varepsilon$. Such an attack is dangerous because the trigger by external voltage event(s) conceals the time when the cyber breach occurred, which could be much earlier than the parameter negation.

Follow along with Fig. 5 Suppose shortly before time $k_0$ some external event(s), such as a fault or effect from the transmission grid, causes the voltages to shift abruptly. Suppose the voltage shifts increase $v^{diff}$, make $v_2$ an undervoltage, and triggers the negation of the inverter parameter $g$. See [20] for power flow examples of this voltage shift on realistic circuits. We are interested in what happens after the system $\Sigma_3$ start time of $k_0$. From $k_0$ to $k_1$: at $k_0$ we have $f_2 < 0$ while $f_1 = 0$, so inverter2 actuates several times, each time causing $v_2$ to get further from the deadband. For $k_1$ to $k_2$: the LTC2 delay is complete so LTC2 taps, fixing the $v_2$ undervoltage but making $v_1$ an overvoltage. For $k_2$ to $k_3$: the inverter1 actuates several times, each time causing $v_1$ to get further from the deadband. For $k_3$ to $k_4$: the LTC1 delay is complete so LTC1 taps, fixing the $v_1$ overvoltage but making $v_2$ an undervoltage again. At $k_4$ we have $f_2 < 0$ while $f_1 = 0$ which was the case for $k_0$, so we have completed one quasi-periodic oscillation. In future sections we show how these oscillations continue.

D. Single Inverter Action Preliminaries

In this section we present some properties of inverter actions between LTC taps to prepare for later proofs.

Suppose inverter $i$ is acting during a time interval $[k ... k+N]$. Define the change in $v_j \in \mathbb{R}^1$ due to the inverter’s action as $\Delta v^{inv}_i(X_{ij}, k + N, k, v_i[k]) := v_j[k + N] - v_j[k] \in \mathbb{R}^1$. $\Delta v^{inv}_i$ can be thought of as the projection of inverter’s actuation onto the $v_j$ axis of the $(v_i, v_j)$ space. Occasionally we omit some of the four parameters from $\Delta v^{inv}$ when they are not relevant.

Assumption 2. (Bounds on LTC and inverter action) $\bar{v}_L + \Delta v^{inv}_i(X_{ii}, k + N, k, v_i[k]) < 2\varepsilon$ for $v_i[k] \in W$, and $\forall k, N$.

This assumption implies that $\bar{v}_L < 2\varepsilon$ and $\Delta v^{inv}_i(X_{ii}, k + N, k, v_i[k]) < 2\varepsilon$ for $v_i[k] \in W$, and $\forall k, N$. The Assumption is reasonable because $\bar{v}_L$ is typically significantly less than $\varepsilon$, and $\Delta v^{inv}$ imparting a voltage change of close to $2\varepsilon$ would require unreasonably large combinations of circuit impedance and inverter capacity.

Recall the voltage update equation (7) $v[k+1] = v[k] - XG(v[k] - v^{ref})$. The inverter acts $N_1 := \text{floor}(d_{L1}/d_{inv})$ times if after the interval $[k ... k+N_1]$ the LTC1 taps, or

$N_2 := \text{floor}(d_{L2}/d_{inv})$ times if after $[k ... k + N_2]$, LTC2 taps. The $i^{th}$ row of (7) implies that node $i$’s voltage is

$$v[k+1] = v[k] + \chi(v[k] - v^{ref}) \in \mathbb{R}^1,$$

and each other voltage on the network is given by

$$v[k+1] = v[k] + \eta\chi(v[k] - v^{ref}) \in \mathbb{R}^1$$

from substituting (10) into (7). Now consider the accumulation of (7) for $N = N_1$ or $N = N_2$ timesteps:

$$v[N + k] = (I - XG)^N v[k] + \sum_{r=0}^{N-1} (1 - XG)^r (XGv^{ref})$$.

The $j^{th}$ row of (14) gives a parameterization of $\Delta v^{inv}_j$:

$$\Delta v^{inv}_j(X_{ij}, k + N, k, v_i[k], g) = v_j[N + k] - v_j[k]$$

$$= ((1 - \chi g)^N - 1)v[k] + \sum_{r=0}^{N-1} (1 - \chi g)^r (X_{ij}gv^{ref}).$$

Remark 2. (Remarks about $\Delta v^{inv}_i$ ∀ $i = 1, 2$)

1) Because $\Delta v^{inv}_i < 2\varepsilon$ from Assumption 2

2) If $g > 0$, $\text{sign}(\Delta v^{inv}_i(v[k])) = -\text{sign}(v_i[k] - v^{ref})$.

3) If $g < 0$, $\text{sign}(\Delta v^{inv}_i(v[k])) = \text{sign}(v_i[k] - v^{ref})$. 
The first item establishes that each inverter acts in the same direction between LTC taps. The second (third) items establish that when \( g > 0 \) (\( g < 0 \)), the inverters push the voltage toward (away) from the deadband.

**Lemma 4.** \((\Delta v^{inv}_i)\) is a homogeneous function) The coupling effect of a single inverter acting at node \( i \) on the voltage at node \( j \) is damped by a factor of \( \eta \). That is, \( \Delta v^{inv}_{ij}(X_{ij}, k+N, k, v_i[k]) = \eta \Delta v^{inv}_i(X_{ii}, k+N, k, v_i[k]) \).

**E. Partitioning \( W \) in State Space when \( g < 0 \)**

In this section we will partition \( W \) into \( D, W_g, W_b, W_o \), based on the possible trajectories from starting the system in each region. We use a similar process to Section [13]. The \( W_b \) region will be when both voltages are above or below the deadband. In that case, both inverters act between LTC taps, and from Assumption \( P \) oscillations cannot occur. Then \( W_o \) will be where only one inverter acts between taps, and is close enough to \( D \) for oscillations to occur. An oscillation would begin with an inverter pushing the voltages further from the deadband (Remark 2 #3) until an LTC tap towards the deadband and overshoots it. Therefore, the boundary of \( W_o \) comes from the states \( v \) where after inverter action(s) and an LTC tap the state is within the deadband edge:

\[
\begin{align*}
    v_1 + r_1 - \bar{v}_L &< v^+ & (16a) \\
    v_2 + r_2 - \bar{v}_L &< v^+ & (16b) \\
    v_1 + r_1 + \bar{v}_L &> v^- & (16c) \\
    v_2 + r_2 + \bar{v}_L &> v^- & (16d)
\end{align*}
\]

Function \( r \) is the inverters’ change in voltage before an LTC tap:

\[
\begin{align*}
    r_1 &:= \Delta v^{inv}_1(\chi, N, v_1) + \Delta v^{inv}_{12}(X_{12}, N_1, v_2) & (17a) \\
    r_2 &:= \Delta v^{inv}_{12}(X_{12}, N_1, v_1) + \Delta v^{inv}_2(\chi, N_1, v_2) & (17b)
\end{align*}
\]

Note that \( r \) depends on both \( v_1 \) and \( v_2 \), but when only one inverter acts, one term in each of (17a) and (17b) zero out, causing eqs. (16a) to (16d) to depend only on \( v_1 \) or \( v_2 \). We can now define the state space regions as

\[
\begin{align*}
    W_o &:= \{(v_1, v_2) \in W : (v_1 \in M(D, v_1^* - v^+) \text{ and } v_2 \in D) \}, & (18a) \\
    W_b &:= \{(v_1, v_2) \in W : (v_2 \in M(D, v_2^* - v^+) \text{ and } v_1 \in D) \}, \quad \text{and } W_g \quad \text{is what remains of } W \setminus (D \cup W_o \cup W_g).
\end{align*}
\]

The \( v_1^* \) and \( v_2^* \) in (18a) are the \( v_1 \) and \( v_2 \) when (16a) and (16c) are set to be equalities. The \( W_o \) region definition is the same as that of the 2-LTC system \( \Sigma_1 \) [13], with the distinction that equations (16) have the additional \( r \) term.

**Fig. 6** shows these state space regions as well as the possible transitions between regions. The trajectory of Fig. 5 is plotted on Fig. 6 with a blue square marker for the IC. Observe that the trajectory oscillates until eventually leaving

In addition to the possible transitions for system \( \Sigma_3 \) in Fig. 4, this system has: \( W_b \to W_g, W_o \to W_b, \) and \( W_o \to W_o \) since the inverter pushes voltages away from \( D \).

When the IC is in \( W_g \) or \( W_b \), there may exist a \( k_0 \) where the full state vector \( x[k_0] = [0, 0, 0, v_1[k_0], v_2[k_0]]^{\top} \). Because \( \Sigma_3 \) is time-invariant, the Fig. 6 regions apply to any \( x[k_0] \) where \( x[k_0] = [0, 0, 0, v_1[k_0], v_2[k_0]]^{\top} \). For example, the system IC could be in \( W_g \) then later have \( x[k_0] \in W_o \), after which point the behavior would be the same as if the system started in \( W_o \).

**F. Conditions for Oscillations to Begin when \( g < 0 \)**

In this section we consider trajectories where \( v[k_0] \in W_o \). As illustrated in Fig. 6, W_o is comprised of four disjoint regions. If hunting occurs in the lower region of \( W_o \) (\( f_1 = 0 \) while \( f_2 < 0 \)), the hybrid system mode sequence (MS) that creates one period of oscillation is \( \alpha_1 \) := \( \{m50, m10, m60, m50, m40, m70\} \) after omitting the increment mode (\( m80 \)) for brevity. Similarly, let \( \alpha_2, \alpha_3, \) and \( \alpha_4 \) be the oscillation sequences when the IC is in the upper, left, and right-hand regions of \( W_o \), respectively.

**Lemma 5.** Basis step for oscillations Consider system \( \Sigma_3 \) with \( g < 0 \). When \( f_1 = 0 \) while \( f_2 < 0 \), necessary and sufficient conditions for completing one oscillation period starting at time \( k_0 \) are

\[
\begin{align*}
    v_1[k_0] + \eta \Delta v^{inv}_2(\chi, k_0 + N_2, k_0, v_2[k_0]) &> v^- & (19a) \\
    v_1[T_1] + \eta \Delta v^{inv}_2(\chi, k_0 + N_1, k_0, v_2[T_1]) &< v^+ & (19b) \\
    v_1[T_2] + \Delta v^{inv}(\chi, k_0 + N_1, k_0, v_2[T_2]) &< v^+ & (19c) \\
    v_2[T_1] + \Delta v^{inv}_2(\chi, k_0 + N_2, k_0, v_2[T_1]) &< v^- & (19d)
\end{align*}
\]

where \( v[T_1] = v_2[k_0] + \Delta v^{inv}_2(\chi, k_0 + N_2, k_0, v_2[k_0]) + \bar{v}_L \), and \( v[T_2] = v_1[k_0] + \eta \Delta v^{inv}_2(\chi, k_0 + N_2, k_0, v_2[k_0]) + \bar{v}_L \).

**Proof.** Follow along with Fig. 5. We will express sequence \( \alpha_1 \) in terms of the system voltage trajectories. For the IC, \( v_2[k_0] \) is an undervoltage and \( v_1[k_0] \) in the deadband. Inverter2 responds to the \( v_2 \) undervoltage, but due to \( g < 0 \) it decreases both voltages. To prevent inverter2 from pushing both voltages below the deadband, we require that

\[
    v_1[k_0] + \Delta v^{inv}_1(\chi, k_0 + N_2, k_0, v_2[k_0]) > v^-.
\]

Next, with the persisting \( v_2 \) undervoltage, LTC2 taps which increases both voltages. To create overshoot so that \( v_1 \) has
an overvoltage, we require that
\[ v_2[k_0] + \Delta v_2^{inv}(X_{12}, k_0 + N_2, k_0, v_2[k_0]) + \bar{v}_L > v^p. \]
Inverter1 responds to the \( v_1 \) overvoltage, but due to \( g < 0 \) it increases both voltages. To prevent inverter1 from pushing both voltages above the deadband, we require that
\[ v[T_1] + \Delta v_1^{inv}(X_{12}, k_0 + N_1, k_0, v_1[T_2]) < v^p. \]
With the persisting \( v_1 \) overvoltage, LTC1 taps which decreases both voltages. To create overshoot so that \( v_2 \) becomes an undervoltage, we require that
\[ v[T_2] + \Delta v_1^{inv}(X_{11}, k_0 + N_1, k_0, v_1[T_2]) - \bar{v}_L < v^p. \]

Finally, we substitute equation (10) into all above equations and apply Lemma 4 to the first and fourth equation, giving the conditions in the lemma statement.

G. Showing Oscillations Continue and Grow when \( g < 0 \)

Next we show that once the MS \( \alpha_1 \) occurs, the next MS will be \( \alpha_1 \) while \( v \in W_0 \). The same process can be applied to the other MS \( \alpha_2, \alpha_3, \) and \( \alpha_4 \).

Define \( m[k]\) as the mode that system \( \Sigma_3 \) is in at time \( k \). Across each \( \alpha_1 \) MS, \( v^{\text{diff}} \) increases. We will prove that in the next section, but note that as a result the voltage that is outside \( D \) gets further from \( v^{rc} \) across each \( \alpha_1 \) MS. Next, consider the following condition:
\[ v_1^{inv}(k_5, k_4, v_1[k_4]) + \Delta v_1^{inv}(k_3, k_2, v_1[k_2]) > 0 \quad (20) \]

Lemma 6. (Induction step for oscillations) Consider system \( \Sigma_3 \) with \( g < 0 \). Assuming condition (20) and Assumption 7 holds, if the system completes MS \( \alpha_1 \), the MS \( \alpha_1 \) will repeat.

Proof. Use Fig. 5 to follow along. \( m[k_4] \): at \( k_0 \) inverter2 actuates and \( m[k_0] = m_50 \) so \( v_2[k_0] \notin D \). Because \( v_2 \) gets further from \( v^{rc} \), \( v_2[k_4] < v_2[k_0] \), so \( v_2[k_4] \notin D \) too. From Assumption 1, \( v_1[k_4] \) cannot be outside \( D \), so \( v_1[k_4] \in D \). Thus inverter2 actuates at \( k_4 \) and \( m[k_4] = m_50 \).

\( m[k_5]\): Because \( g < 0 \), inv2 actuating (\( m[k_4] = m_50 \)) will keep \( v_2 \notin D \). If the inverter’s coupling effect on \( v_1 \) is strong enough, even though \( v_1[k_4] \in D \), \( v_1 \) could go below the deadband by the time of \( k_5 \). By Assumption 2 the inverter actions summed with an LTC tap are not large enough for this. Thus at \( k_5 \), \( v_1 \) is still inside \( D \) and \( v_2 \) is still outside \( D \). So at \( k_5 \) LTC2 taps up and \( m[k_5] = m_30 \).

\( m[k_6]\): The LTC2 tap may not overshoot the deadband at \( k_6 \). If (20) does not hold, then \( v_1[k_6] \in D \), by Assumption 1, \( v_2[k_6] \in D \) too, and the system stays in the deadband. If (20) holds, inverter1 actuates and \( m[k_4] = m_50 \). \( m[k_7]\): Assumption 2 disallows \( v_2 \) from going above \( D \) (like how in \( m[k_5] \) it disallows \( v_1 \) from going below \( D \)). Thus at \( k_7 \), \( v_2 \) is still inside \( D \) and \( v_1 \) is still outside \( D \). So at \( k_7 \) LTC1 taps down and \( m[k_7] = m_20 \).

Lemma 7. (Oscillations grow) If system \( \Sigma_3 \) with \( g < 0 \) has oscillations, \( v^{\text{diff}} \) increases after each oscillation period.

Let \( s_1 \) be the set of \( (v_1[k_0], v_2[k_0]) \) where basis conditions (19) hold. The sets of conditions that correspond to sequences \( \alpha_2, \alpha_3, \) and \( \alpha_4 \) are derived with the same process as the Lemma 5 proof, and we call their corresponding sets \( s_2, s_3, \) and \( s_4 \). Then define \( S := (\bigcup_{i=1}^{s_4} s_i) \in W_0 \), which is the only voltage region where oscillations can begin. Note that with the \( \Delta v^{\text{inv}} \) parametrized form (15), \( S \) can be represented by purely the variables listed in Table 4.

Theorem 1. Define \( T_1 \) as the first instant where \( v[T_1] \in D \), and define \( T_2 \) as the first instant where \( v[T_2] \in W_1 \). When \( g < 0 \), \( v[k_0] \in S \) is necessary but not sufficient for system \( \Sigma_3 \) to exhibit growing oscillations starting at time \( k_0 \). These oscillations terminate either at time \( T_1 \) or \( T_2 \).

Proof. Lemma 5 (basis step) establishes that (19) are necessary for on period of oscillations to occur. By Lemma 6 (induction step), the system continues to oscillate after the first oscillation period. Lemma 7 establishes that the oscillations grow, so the system will eventually land in \( D \) or outside \( W_1 \).

Theorem 1 implies that when \( g < 0 \), the only way for \( \Sigma_3 \) to exhibit oscillations is when \( v[k_0] \in S \). To use this theorem, engineers would choose control parameters such that \( S = \emptyset \). Further, if each device has a copy of all control parameters, they can reject incoming parameter updates when \( S \neq \emptyset \).

IV. RESULTS AND SCALABILITY

A. Parameter Plots

In this section we use MATLAB’s MPT toolbox to plot set \( S \) in the \((v_1, v_2)\) space and examine its implications on the ratio of the device control delays. Recall that \( S \) is the only voltage region where oscillations can begin, and includes the projection of basis conditions (19) onto the \((v_1, v_2)\) space.

In Fig. 7, we plot \( S \) on the \((v_1, v_2)\) space, and validate that \( S \) in Fig. 7a is indeed a subset of \( W_0 \) from (18a), as both sets have width of 0.0095 pu. Observe that some corners of \( W_0 \) are not included in \( S \) because trajectories that start there leave \( W \) before completing an oscillation period. We also observe that in Fig. 7b, where oscillations can grow, the area of \( S \) is smaller compared to when oscillations are damped in Fig. 7a. It is relieving that the regions where dangerous oscillations could occur are narrow.

Next we examine the appropriate timescale separation between the inverters and LTC1 for system \( \Sigma_3 \) when \( g < 0 \). Because \( N_1 = \text{floor}(d_{L1}/d_{inv}) \) and \( N_1 \) enters \( \Delta v^{inv} \) as the exponent (see (15)), each fixed \( N_1 \) represents the slope of a line through the origin on the \((d_{L1}, d_{inv})\) space. As such, varying \( d_{L1} \) and \( d_{inv} \) such that \( N_1 \) is fixed will not change the \( S \) region on \((v_1, v_2)\). Therefore, rather than iterate over
the \((d_{L1}, d_{inv})\) in a meshgrid, we compare the area of set \(S\) for lines corresponding to different \(N_1\) values.

We set all variables except \((v_1[k_0] and v_2[k_0])\) to the defaults in Table I. Instead of \(d_{L1} = 30\) and \(d_{inv} = 40\), which have a ratio of \(\frac{30}{40} = \frac{3}{4}\). We vary \(N_1\) from 5 to 29. For each \(N_1\) value, if \(S = \emptyset\), then hunting oscillations are impossible for all \(v[k_0] \in W\), and we mark the line with slope \(N_1\) as light gray in Fig. 8. Conversely, if \(S \neq \emptyset\) then the \(N_1\) line is dark gray. The line \(d_{inv} = d_{L1}\) is also marked to only allow the \(d_{inv} < d_{L1}\) from Table I. We observe that \(N_1 = 17 = \text{floor}(d_{L1}/d_{inv})\) is the borderline case where hunting is impossible. For example, if the inverters have a 3-second delay, the substation LTC needs at least a 51-second delay to prevent hunting for all IC in \(W\).

B. Grids with More than Four Devices

Radial distribution grids are typically tree graph networks whose root is the substation. Each node has one or more branch(es), which is the tree network connected to that node’s edge(s). Suppose there is at most one LTC and at most two actively controlled inverters on each branch of the root node \(b\). Then each branch has a system comprised of the substation LTC, the LTC on the branch, and two inverters on the branch. One can characterize each system as \(\Sigma_3\) and setup conditions to prevent oscillations separately using the methodology of section III. The conditions across all branches must be jointly satisfied, but because the substation LTC is common to all subsystems, as \(b\) grows the number of symbolic variables grows by \(3b + 1\) instead of \(4b\).

V. CONCLUSION

We have presented a novel hybrid system model for LTCs with inverters on radial distribution circuits. Leveraging the system dynamics, we have derived conditions on the control parameters to guarantee against voltage oscillations created by device hunting. The conditions inform the design of appropriate parameters, such as the minimal timescale separation of control delays between LTCs and inverters. The conditions also pave the way for implementing on-board certificates that guard against malicious firmware updates of control parameters.

Future work will more formally investigate the types of events that widen the voltage difference enough for hunting to be possible. Additionally, the relationships between parameters captured by the conditions derived here will be examined in more detail. Finally, the behavior of the system in abnormal but not impossible operating states will be explored.

VI. APPENDIX

Lemma [1] If \(\bar{v}_L > 2\epsilon\), system \(\Sigma_1\) will have marginally stable oscillations for all time when any \(v_1[0] \in M(D, c)\) or \(v_2[0] \in M(D, c)\) where \(c = \bar{v}_L - 2\epsilon > 0\).

Proof. If \(v_1[0] \in M(D, c)\), LTC1 taps, causing \(\bar{v}_L\) to overshoot the deadband of width \(2\epsilon\) and land outside \(D\). After a delay \(d_{L1}\), LTC1 will tap in the opposite direction, landing at the system IC. Then these actions repeat, causing \(v_1\) and \(v_2\) to oscillate with constant amplitude for all time. When \(v_2[0] \in M(D, c)\) we get the same oscillatory behavior. \(\Box\)

Lemma [2] If \(\bar{v}_L \leq 2\epsilon\), \(v[T] \in W_o\), and \(v^{\text{diff}} < 2\epsilon - \bar{v}_L\), system \(\Sigma_1\) will have marginally stable oscillations starting at time \(T\).

Proof. First consider an IC in \(W_o\) (i.e. \(T = 0\)) where \(v_2[0]\) is an undervoltage. Overshooting the deadband with an LTC tap can be represented with

\[v_2[0] < v^-\text{ start with undervoltage}\]

\[v_1[0] + \bar{v}_L > v^+\]

Combining the above two equations gives \(v^{\text{diff}} > 2\epsilon - \bar{v}_L\). These conditions for \(v_2[0]\) being an overvoltage would yield the same \(v^{\text{diff}} > 2\epsilon - \bar{v}_L\). Now consider where our IC is not in \(W_o\) but at time \(T\) we land in \(W_o\). Because the system has no internal memory states, oscillations will begin after this nonzero \(T\) as if the zero-start time was at \(T\). \(\Box\)

Lemma [3] If \(G < 0\), system \(\Sigma_2\) given by (8) has \(v \to \pm\infty\).

Proof. Let \(F = -G\). Because \(G < 0\) and is diagonal, \(F\) is diagonal and positive definite. The proof of Theorem 3.1 in [19] shows that \(\text{eig}(XS) = \text{eig}(S^{\frac{1}{2}}XS^{\frac{1}{2}}) \in (0, 2)\) for symmetric \(X\) and diagonal positive definite \(S\). Thus \(\text{eig}(XF) = \text{eig}(F^{\frac{1}{2}}XFS^{\frac{1}{2}}) \in (0, 2)\). Then all \(\text{eig}(I - XG) = \text{eig}(I + XF) = 1 + \text{eig}(XF) > 1\). Thus the spectral radius of \((I - XG)\) is greater than 1, so \(e \to \infty\), and \(v \to \infty\) or \(v \to -\infty\). \(\Box\)

Lemma [4] The coupling effect of a single inverter actuating at node \(i\) on the voltage at node \(j\) is damped by a factor of \(\eta\). That is, \(\Delta v_i^{\text{inv}}(X_{ij}, k + N, k, v_i[k]) = \eta \Delta v_i^{\text{inv}}(X_{ij}, k + N, k, v_i[k])\).

Proof. From the update equations (12) and (13).

\[\Delta v_i^{\text{inv}}(X_{ii}, k + 1, k, v_i[k]) = -\chi(v_i[k] - v^{ref})\]

\[\Delta v_j^{\text{inv}}(X_{ij}, k + 1, k, v_i[k]) = -\eta(v_i[k] - v^{ref})\]

By Remark 2 the voltage change at each timestep over \([0, N]\) is additive in the same direction. If we consider a duration...
over two timesteps,
\[
\Delta v_{1}^{\text{inv}}(x_{1}, k+2, k, v_{i}[k]) = v[k+2] - v[k+1] + v[k+1] - v[k]
\]
\[
= \Delta v_{j}^{\text{inv}}(\chi, k+2, k+1, v_{i}[k+1]) + \Delta v_{j}^{\text{inv}}(\chi, k+1, k, v_{i}[k])
\]
\[
= -\eta \chi(v_{i}[k+1] - v_{e}(f)) - \eta \chi(v_{i}[k] - v_{e}(f))
\]
\[
= \eta \Delta v_{i}^{\text{inv}}(X_{i}, k+2, k, v_{i}[k])
\]
\]
\]
\]
\]
\]
\]
\]
\]
\]
\]
\]
\]
\]
\]

Lemma 7 If system $\Sigma_3$ with $g < 0$ has oscillations, $v_{\text{diff}}$ increases after each oscillation period.

Proof. We consider the case that the IC is below the deadband. We express the voltages after the first sequence of modes and compare $v_{\text{diff}}[k_0]$ to $v_{\text{diff}}[k_4]$

\[
v_1[k_4] = v_1[k_0] + \eta \Delta v_2^{\text{inv}}(k_0 + N_2, k_0, v_2[k_0]) + v_L
\]
\[
+ \Delta v_{1}^{\text{inv}}(k_0 + N_1, k_0, c) - v_L
\]
\[
v_2[k_4] = v_2[k_0] + \Delta v_2^{\text{inv}}(k_0 + N_2, k_0, v_2[k_0]) + v_L
\]
\[
+ \eta \Delta v_{1}^{\text{inv}}(k_0 + N_1, k_0, c) - v_L
\]

where $c := v_1[k_0] + \eta \Delta v_{1}^{\text{inv}}(k_0 + N_2, k_0, v_2[k_0]) - v_L$. Subtracting the above two equations, we have

\[
v_{\text{diff}}[k_4] = v_{\text{diff}}[k_0] + \eta \Delta v_{1}^{\text{inv}}(k_0 + N_2, k_0, v_2[k_0])
\]
\[
+ \Delta v_{1}^{\text{inv}}(k_0 + N_1, k_0, c) - \Delta v_{1}^{\text{inv}}(k_0 + N_2, k_0, v_2[k_0])
\]
\[
- \eta \Delta v_{1}^{\text{inv}}(k_0 + N_1, k_0, c) - v_L
\]

which simplifies to

\[
v_{\text{diff}}[k_4] - v_{\text{diff}}[k_0] = (\eta - 1) \Delta v_{1}^{\text{inv}}(v_2[0], N_2)
\]
\[
- \Delta v_{1}^{\text{inv}}(k_0 + N_1, k_0, c)
\]

(21)

The damping factor has $0 < \eta < 1$, so $(\eta - 1)$ is negative. $v_2[k_0]$ is below the deadband, so $\Delta v_2^{\text{inv}}(N_2, v_2[k_0]) < 0$, and $v_1[k_2]$ is above the deadband, so $\Delta v_{1}^{\text{inv}}(c, N_1)$ is positive. Together, (21) is always positive. Thus $v_{\text{diff}}[k_4] > v_{\text{diff}}[k_0].$

If we repeat this process for the case of the IC being an overvoltage, we get the same final equation (21).

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