Device Characteristics of AlGaN/GaN HEMTs with p-GaN Cap Layer

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In this study, AlGaN/GaN high-electron-mobility transistors with a 5-nm p-GaN cap layer were investigated to compare their performance under various activation conditions. Specifically, p-GaN cap layers were activated using rapid thermal annealing at 700 °C for 5, 10, and 15 min in an N2 environment before device fabrication. The gate leakage current reduced considerably when the p-GaN cap layer activation time was longer. The measured on/off current ratio was improved to 9 × 107 for a Schottky-gate device with 15-min annealing time. The breakdown voltage was increased using the activated p-GaN cap layer. In pulsed I–V measurements, the device with the p-GaN cap layer with a 15-min activation time exhibited less current dispersion.

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Figure 1. Schematic cross-sectional view of the AlGaN/GaN structure on a Si substrate.

Device Structure and Experimental

Figure 1 shows a schematic of the AlGaN/GaN HEMT structure under investigation. The epitaxial layers were grown on 4-in p-type Si substrates through MOCVD and were supplied by NTT-Advanced Technology Corporation. The epitaxial layers comprised a 300-nm GaN channel, a 1-nm AlN layer, a 20-nm Al0.25Ga0.75N layer, and a 5-nm GaN cap. The polarization-induced 2DEG density was formed with Mg at a doping concentration of 1 × 1019 cm−2. According to X-ray rocking curve measurements, the full width at half-maximum (FWHM) values of the epitaxial wafer were 563 and 732 arcsec for the symmetric (002) and asymmetric (102) peaks of GaN, respectively. Hall measurements revealed the 2DEG mobility and density to be 1970 cm2/V·s and 1.004 × 1012 cm−2, respectively. The sheet resistance was estimated at 314.8 Ω/sq before activation.

Samples with the Mg-doped GaN cap layer were activated using rapid thermal annealing at 700 °C for 5, 10, and 15 min in an N2 environment before device fabrication. Table I summarizes the FWHM

| Samples            | Directions | FWHM (arcsec) |
|--------------------|------------|---------------|
| Without activation | (002)/102  | 563/732       |
| With 700 °C 5-min   | (002)/102  | 555/731       |
| With 700 °C 15-min  | (002)/102  | 566/729       |

Table I. Summary of X-ray diffraction measurements.

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values derived from X-ray diffraction measurements for samples with and without thermal activation. After activation, the FWHM values were found to be similar, indicating the same crystal quality. Table II summarizes the 2DEG mobility and density with and without thermal activation, as determined from the Hall measurements. The sheet resistances from the TLM measurement were respectively 310, 273, and 277 kΩ/sq for the samples with the 5, 10, and 15-min annealing times; these resistances were similar to those derived from Hall measurements. Lower sheet resistance was obtained after annealing, possibly because of thermal annealing at 700 °C.

After thermal activation, all samples were fabricated using the same layout and process flow. Dry etching with BCl3 and Cl2 mixed gas was performed to obtain a mesa isolation of 390 nm. The ohmic contacts were formed by evaporating a Ni/Ti/Al/Ti/Au stack through E-beam evaporation. The Schottky gate metal was obtained by evaporating a Ni/Ti/Al/Ti/Au stack through E-beam evaporation. No field-plate design was used in this process. All the devices under testing had a gate-source distance of 4 μm, a gate length of 2 μm, a total gate width of 2 × 50 μm, and a gate–drain distance (LGD) of 8 μm. Devices with various LGD were fabricated simultaneously for a breakdown study. Finally, devices were passivated with a 200-nm SiN layer through inductively coupled plasma CVD at 200 °C.

Results and Discussion

DC I–V characteristics were measured using a Keysight B1505A semiconductor device parameter analyzer. Fig. 2 shows the output and transfer characteristics of the devices fabricated with a p-GaN cap layer activated under various conditions. The drain current (ID) was found to have increased from 530 to 586 mA/mm at VGS = 1 V and VDS = 10 V after 15 min of activation at 700 °C, which corresponds to a ~0.2-V shift in the threshold voltage. The increase in ID was because of the decreased sheet resistance. Fig. 3 shows the ID–VGS and IG–VGS characteristics in a semilog scale. The off-state current was dominated by the gate leakage current and found to decrease at longer annealing times. The gate leakage was effectively suppressed by the p-GaN cap layer after activation. The lowest ID was 6.5 × 10–6 mA/mm; a Schottky-gate device exhibits an on/off current ratio of 9 × 107.

The breakdown characteristics of the fabricated HEMTs with various LGD are shown in Fig. 4. The measured breakdown voltage was determined at ID = 1 mA/mm and VGS = –6 V with substrate floating. Because this study investigated the cap layer effect on device performance, substrate floating measurements were performed to alleviate the buffer/substrate effect on the breakdown voltage. For all of the fabricated devices, a linear increase in the breakdown voltage was observed as LGD was increased up to 10 μm. The devices fabricated under longer annealing times exhibited higher breakdown voltages. The inset in Fig. 4 shows the ID–VDS at off-state for devices with LGD of 20 μm. Lower off-state currents were observed in the devices fabricated under longer activation times, hence the higher breakdown voltages. The highest breakdown voltage was 1380 V, which was observed in the device with an LGD of 20 μm and activation time of 15 min. Because there was no field-plate design in the fabricated device, no field-plate design in the device with an LGD of 20 μm and activation time of 15 min. Because there was no field-plate design in the fabricated device, its performance was not affected by the activation time.
the highest electric-field was located near the drain-side gate edge. The 5-nm p-GaN cap layer was found to be crucial to reducing the leakage current and thus enhance the breakdown characteristics.

Pulsed I–V measurements were performed using a Keysight B1525A high-voltage semiconductor pulse generator unit with a pulse width of 5 μs and a period of 1 ms. Fig. 5 shows the pulsed I–V characteristics of the fabricated devices. The quiescent bias points of \( (V_{GS}, V_{DS}) \) were (0, 0), (−6, 10), (−6, 20), (−6, 30), and (−6, 40) V. This figure shows that lower current dispersion was observed in the device with the layer formed with a 15-min activation time. Moreover, the pulsed I–V curves show a less pronounced self-heating effect compared with those in Fig. 2a. Higher current and lower \( R_{ON} \) were obtained at room temperature. Because the highest electric field is located near the gate edge, surface states located near the gate edge can be charged while biasing into the off-state, causing current collapse. Fig. 5 shows that the devices with longer activation times exhibited less current dispersion, indicating that an effective suppression of electron injection into the trap states at the surface was achieved.

Different quiescent bias points were also used to investigate the effect of off-state bias on transient \( I_D \). Transient \( I_D \) was obtained at \( V_{DS} = 10 \) V and \( V_{GS} = 1 \) V from Fig. 5. Fig. 6 shows the normalized transient \( I_D \) at various off-state drain biases. The transient \( I_D \) decreased as the drain bias stress was increased from 10 to 40 V. However, improvement in the current drop was observed in the devices prepared under longer activation times.

Conclusions

AlGaN/GaN HEMTs with 5-nm p-GaN cap layers fabricated under various activation conditions were investigated. Three activation times were adopted for annealing at 700 °C (5, 10, and 15 min) in N\(_2\) ambient, which was performed before device fabrication. DC I–V and pulsed I–V characteristics of all devices showed significant improvement in the device with a 15-min activation time. The device with the highest on/off current ratio of \( 9 \times 10^7 \) showed a breakdown voltage of 1380 V. The electric field near the drain-side gate edge in AlGaN/GaN HEMTs is a critical factor related to the gate leakage current, off-state breakdown, and current collapse. In the present study, the p-GaN cap layer was found to be a viable alternative to i-GaN cap layers used in AlGaN/GaN HEMTs because it reduces the leakage current, improves the breakdown characteristics, and mitigates current collapse.

Acknowledgments

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