A Broadband High-speed Programmable Multi-modulus Divider Based on CMOS Process

Muzhen Hao¹, Xiaodong Liu¹*, Zhizhe Liu¹, Feng Ji¹, Di Sun¹, Hongjie Yin¹, Xingwang Li¹

¹ Beijing Institute of Remote Sensing Equipment, Beijing, China

*Corresponding author’s E-mail: xiaodongnanjing@163.com

Abstract. This paper introduces a design of a high-speed programmable multi-modulus divider (MMD) based on 65nm CMOS process. The design adopts the cascade structure of 7 level 2/3 frequency dividers, and expands the frequency division range by adjusting the number of cascade stages, so as to achieve a continuous frequency division ratio of 16 to 255. Among them, the first level 2/3 frequency divider adopts the D flip-flop design of CML (current mode logic) structure, the second level 2/3 frequency divider adopts the D flip-flop design of E-TSPC (extended true-single-phase-clock) structure. The whole circuit realizes the working frequency range of 13–18GHz high frequency and large bandwidth. This design has completed layout drawing and parasitic parameter extraction simulation. The simulation results show that the operating frequency range of the circuit can reach 13–18GHz. When the input signal is 18GHz and the frequency division ratio is 255, the phase noise is about -135dBc/Hz@1kHz. It has the advantages of high frequency, large bandwidth, and low phase noise.

1. Introduction

With the development of millimetre-wave detection and communication technology, the design and research of millimetre-wave integrated circuits has become a research hotspot in industry in recent years. As one of the core modules in the millimetre wave transceiver system, the millimetre wave frequency synthesizer provides stable and pure local oscillation signals for the system, and its performance indicators determine the working efficiency of the transceiver system. In the design of integrated millimetre wave frequency synthesizer, the design of a high-speed, wide-band, and low-noise programmable frequency divider is one of the difficulties. It can divide the oscillator high-frequency signal to a lower frequency at a specified multiple for comparison with the reference frequency. The frequency division accuracy and phase noise of the programmable frequency divider will have an important impact on the performance of the frequency synthesizer, while its working bandwidth and frequency division range affect the configurability and versatility of the entire frequency synthesizer at the same time.

In this article, a multi-modulus divider (MMD) which can be applied to high-performance broadband millimetre wave frequency synthesizers has been realized by adopting 65nm CMOS process. This MMD is realized based on CML (current mode logic) and E-TSPC (extended true-single-phase-clock) technology. Therefore, the programmable frequency division can be carried out on the input signals of 13~18 GHz, with a frequency division ratio ranging from 16 to 255. Firstly, this article presents the overall structure and circuit implementation of the MMD, and emphatically describes the design of the high-speed 2/3 frequency divider based on CML technology and the high-speed 2/3 frequency divider based on E-TSPC technology. Secondly, the layout and post-simulation of the overall circuit are...
introduced. The simulation results show that the broadband high-speed MMD proposed in this paper can achieve 16–255 continuous frequency division in the range of 13–18GHz. When the input signal is 18GHz and the frequency division ratio is 255, the phase noise is about -135dBc/Hz@1kHz. With the advantages of high frequency, large bandwidth, low phase noise, etc., MMD can meet the application requirements of high-performance millimeter wave phase-locked loop frequency synthesizers.

2. The design of MMD

2.1. The overall structure of MMD

Figure 1 is the scalable frequency division ratio MMD structure used in this article, which is improved on the basis of the basic n-level 2/3 frequency divider cascade structure[1]. By adding enable control to some post-stage frequency division units, the effective number of stages in the MMD can be changed, thereby realizing the downward expansion of the frequency division ratio.

The working principle of the n-level 2/3 frequency divider cascade structure MMD is as follows: When performing frequency division, the last-stage frequency division unit generates the feedback signal Do7 and transmits it to the previous stage, and the feedback signal is re-locked by each level unit in the entire link. When the Doi signal input from the i-th stage is high (enable), and if the control signal MCi is also high at this time, the 2/3 frequency divider divides frequency by 3, and thus an extra period of the input signal is added to the output signal period. Therefore, an n-stage 2/3 frequency dividing unit chain can generate an output signal with a period of [2]:

$$T_{out} = (2^n + 2^{n-1} \cdot MC_{n-1} + 2^{n-2} \cdot MC_{n-2} + \cdots + 2 \cdot MC_1 + MC_0) \times T_{in}$$

(1)

In the formula (1), $T_{in}$ is the period of the input signal $F_{in}$, and $MC_0 \cdots MC_{n-1}$ is the control word of the 2/3 frequency division of each stage unit. When $MC$ is high, the frequency is divided by 3, and when $MC$ is low, the frequency is divided by 2. It can be seen that the overall frequency division range of MMD is from $2^n$ (all MCs are low) to $2^{n-1} - 1$ (all MCs are high). It can be seen that the frequency division range of this structure is limited by the number of cascaded stages n. This design changes the effective number of stages in the MMD by adding switch control word $EN_i$s to the rear 3 levels of the 2/3 frequency divider, so as to achieve a frequency division range of 16 to 255.

2.2. The structure of 2/3 dual-modulus divider

The overall structure of the 2/3 dual-mode frequency divider in this article is shown in Figure 2. It consists of two D flip-flops and three logic gates. When DIN is high, the 2/3 divider is controlled by MC. If MC is high at this time, the 2/3 frequency divider is equivalent to the divide-by-3 frequency divider shown in Figure 3 (a). It is a sequential state machine with 3 states composed of two D flip-flops, and its state transition table is shown in Figure 3 (b). If MC is low, the divider is in divide-by-2 mode. When DIN is low, the 2/3 frequency divider is not controlled by MC and can only divide frequency of input signal by 2.

The working frequency of MMD is mainly limited by the D flip-flop in the 2/3 frequency divider. In order to make MMD work in a high frequency environment of 13–18GHz, the first level 2/3 frequency divider adopts CML structure D flip-flop, and the second level 2/3 frequency divider adopts E-TSPC structure D flip-flop. At the same time, the size of the transistor is optimized and the parasitic capacitance
is reduced. The following will emphatically introduce the D flip-flop design of the CML structure and E-TSPC structure used in this article[2].

![Figure 2. The structure of 2/3 dual-modulus divider](image)

2.3. The design of CML structure D flip-flop
The D latch is the basic unit that constitutes the dual-mode frequency divider. By cascading two identical D latches in a master-slave manner, a D flip-flop can be formed. Figure 4 (a) shows the schematic circuit diagram of the CML latch[3]. Compared with the rail-to-rail latch structure, the CML latch voltage swing is smaller, which can reduce the signal rise and fall time, thereby increasing the operating frequency. The load of the latch uses the variable resistor network shown in Figure 4 (b), and the size of the connected resistor is controlled by SEL1 and SEL0. It is ensured that the load resistance of the appropriate size can be selected under different process angles to realize the normal frequency division function, which has a certain engineering application value.

![Figure 4. (a) CML latch (b) Variable resistance network](image)
As shown in Figure 4 (a), the CML latch contains 3 sets of differential pairs of transistors, M1 and M2 are clock pairs, M3 and M4 are sampling pairs, and M5 and M6 are latch pairs. Here, a structure without tail current source is used to obtain a higher voltage margin and increase the operating frequency. The working principle of the CML latch is: when the input signal CLK is high, M1 is turned on, M2 is turned off, and the sampling pair transistors M3 and M4 work. At this time, the input signal is sampled and the differential signal is amplified. When the input signal CLK is low, M2 is turned on and M1 is turned off. At this time, M5 and M6 work to lock the sampled data, and the data will no longer change[4].

Besides the speed of the CML latch, the operating frequency of the 2/3 divider is also affected by the signal feedback delay. In order to reduce the parasitic capacitance, reduce the feedback delay, and increase the operating frequency, some of the logic gates in Figure 2 can be integrated into the D latch. Figure 5 shows the D latch of the CML structure integrating the AND gate and the OR gate.

2.4. The design of E-TSPC structure D flip-flop
True Single-Phase Clock (TSPC) D flip-flop is a dynamic logic structure with high-speed single-ended input[5]. It only needs a single-phase clock signal, and can avoid the influence of the deviation between multi-phase clocks. It has no static power consumption, and can reduce area, power consumption and design complexity. The structure of the traditional TSPC D flip-flop is shown in Figure 6 (a).

The E-TSPC structure is extended from the traditional TSPC structure, as shown in Figure 6 (b). Without the stacked transistors, all transistors are not affected by the back-gate effect, so the operating frequency is higher[6]. Its working principle is as follows: when CLK is high, MN1 and MN2 are both turned on. Since MP1 has a stronger driving ability than MN1, so the level of point X is determined by data D. At same time, MN2 has a stronger driving ability than MP2, so no matter what level the X point takes, the Y point will be discharged to low. Since the Y point is at a low level, MP3 and MN3 are not turned on, and the Q point maintains the original value, and the trigger is in the holding state at this time.

Figure 5. (a) CML latch with integrated AND gate. (b) CML latch with integrated OR gate.

Figure 6. (a) The structure of the traditional TSPC D flip-flop. (b) The structure of E-TSPC D flip-flop.
When CLK is low, MN1 is turned off and MP3 is turned on. At the beginning of CLK low level, the level of point X remains unchanged, and then D may charge point X to a high level. MN2 is turned off, and the level at point Y is $\overline{X}$. Since MN3 has a stronger driving ability than MP3, point Q gets the level of $\overline{Y}$ (a new value of D). At this time, the trigger is in the sampling state. It can be seen that this E-TSPC D flip-flop is triggered by the falling edge.

3. Layout design and simulation verification
This article adopts the 65nm CMOS process to design and layout the MMD according to the system structure shown in Figure 1. Figure 7 shows the MMD layout designed in this article, with an overall size of about 170um × 88um. The signal is input from the bottom and output from the right after passing through a 7-level 2/3 frequency divider.

In the article, the parasitic parameters of the layout are extracted, and the post-simulation verification has been carried out. Figure 8 (a) shows the post-simulation input and output waveforms when the input is 13GHz and the frequency is divided by 255. At this time, the MMD has the lowest frequency output. Figure 8 (b) shows the post-simulation input and output waveforms when the input is 18GHz and the frequency is divided by 16. At this time, the MMD has the highest frequency output.

Through frequency sweep verification, MMD can be divided normally in the frequency range of 13~18GHz. Figure 9 (a) shows the degradation of MMD to ideal signal phase noise when the input is 13GHz and the frequency division ratio is 255. At this time, the output frequency is about 50.98MHz, and the phase noise is about -137dBc/Hz@1kHz. Figure 9 (b) shows the degradation of phase noise.
when the input is 18GHz and the frequency division ratio is 255. At this time, the output frequency is about 70.59MHz, and the phase noise is about -135dBc/Hz@1kHz. When the working voltage is 1.2V, the current of the whole circuit is about 35mA.

4. Conclusion
This article introduces a 16~255 continuous programmable MMD with operating frequency of 13~18GHz, and analyzes the working principle of core circuits such as 2/3 frequency divider of CML structure and E-TSPC structure in detail. The MMD is formed by cascading 2/3 frequency dividers of a level 1 CML structure, a level 1 E-TSPC structure and a level 5 CMOS logic structure. The post-simulation results show that when the input signal is 18GHz and the frequency is divided by 255, the phase noise of the output signal is about -135dBc/Hz@1kHz. The overall circuit working current is about 35mA at 1.2V working voltage. The MMD has the advantages of high frequency, large bandwidth, low phase noise, versatility and strong match ability etc., and can meet the application requirements of high-performance millimeter wave phase-locked loop frequency synthesizers.

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