Cryogenic High-Frequency Readout and Control Platform for Spin Qubits

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We have developed a cryogenic platform for the control and readout of spin qubits that comprises a high density of dc and radio frequency sample interconnects based on a set of coupled printed circuit boards. The modular setup incorporates 24 filtered dc lines, 14 control and readout lines with bandwidth from dc to above 6 GHz, and 2 microwave connections for excitation to 40 GHz. We report the performance of this platform, including signal integrity and crosstalk measurements and discuss design criteria for constructing sample interconnect technology needed for multi-qubit devices.

I. INTRODUCTION

Nanoscale circuits that enable coherent manipulation and readout of single electron spin-states are of interest as platforms for constructing quantum information technology [1–3]. These qubit devices are operated at cryogenic temperatures by controlling electron energy levels using nanosecond voltage pulses applied to metal electrodes on the surface of a semiconductor heterostructure [4, 5]. At present an evolution is underway, from single-qubit architectures that have demonstrated state preparation, arbitrary superposition [4, 7], and single-shot readout [8–11], to multi-qubit devices needed to quantify entanglement and perform computation via the parallel operation of several quantum gates [12–14]. Scaling from single to few qubits, in addition to the major scientific challenges, also requires technical advances such as the development of new hardware and methods for enhancing readout, control, and noise mitigation in multi-qubit cryogenic setups.

Crosstalk between control signals presents a challenge for scale-up of spin qubit devices, increasing error rates for single qubits and opening new channels for decoherence in multi-qubit architectures. In particular, the broadband nature of control waveforms, which are typically large-amplitude rectangular ‘dc’ pulses with sub-nanosecond rise-times, resemble a mixed-signal environment in which digital logic circuits can interfere with sensitive analog systems [15]. Maintaining a high degree of readout and control signal fidelity under these conditions is necessary if spin-qubit architectures are to reach the low hardware error thresholds required for quantum error correction [16].

Many of these technical challenges are not unique to quantum devices and are common place in the context of commercial monolithic microwave integrated circuit (MMIC) implementation and packaging. In contrast however, interconnect solutions for spin-qubit device development require cryogenic and high magnetic field operation together with a flexibility that allows for the many iterations of a design, fabrication, and measurement cycle. For instance, interconnects are required to accommodate the regular changing of sample chips of different size and bonding configuration. Quantum coherent circuits are also different to typical MMIC architectures in that they can be sensitive to very broadband noise and interference (hertz to terahertz) which increases the device electron temperature and, when strong enough, can artificially drive transitions between qubit energy levels [17], lead to photon assisted tunnelling [18], or create bias currents from rectification [19]. For spin qubits, even small amplitude noise or crosstalk (of the order of nano-volts) reduces the fidelity of quantum gate operations by introducing uncontrolled fluctuations of the electron potential defined electrostatically using metallic surface electrodes. Error suppression methods that dynamically decouple environmental fluctuations can serve to mitigate noise on control lines, but these introduce an additional computational overhead and fail in the limit of white noise derived from thermal sources [20].

Here we report a low-noise readout and control platform that incorporates the high density of interconnects needed to operate multi-qubit devices at cryogenic temperatures. The modular platform makes use of a series of microwave printed circuit boards (PCBs) that connect together to enable ease of sample exchange. The main device-PCB is a 5-layer laminate that electrically partitions dc, radio-frequency (rf), and microwave signals using ground planes and a dense array of vias. Such partitioning is shown to strongly suppress high-frequency crosstalk in device architectures that require a high-density of signal interconnects. Characterizing our setup, we present signal fidelity measurements at cryogenic temperatures and compare these to EM circuit models and simulations. Although developed specifically for spin qubits, we anticipate that the results reported here are of general interest for experiments that involve high-frequency measurements of nanoscale devices at cryogenic temperatures.

II. COUPLED PRINTED CIRCUIT BOARDS

We first describe the setup of the circuit boards and their interconnects, including details of the cryostat wiring and filters used to suppress noise in our system. The 3 PCBs comprise a cryostat-PCB, in thermal contact with the mixing chamber of a dilution refrigerator, a 5-layer device-PCB that houses the wire bonded sample
FIG. 1: Modular PCB architecture incorporating a high density of interconnects needed for multi-qubit readout and control. (a) The cryostat-PCB is fixed to the cold finger at the mixing chamber of a dilution refrigerator. (b) Shows the high-frequency custom cables and feed-throughs entering the cold finger. (c) Top view and (d) bottom view cartoon of the coupled PCB set (rendered using Solidworks CAD software package). (e) The device-PCB, which houses the chip, connects to the cryostat-PCB with the use of MSMP connectors and bullets. The device-PCB has 31 filtered dc lines, matching circuits, and 2 microwave frequency connections together with 14 rf lines that are passed through from the cryostat-PCB. The ground-PCB pushes on to the device-PCB from the other side, allowing for ‘make-before-break’ connections. (f) Terraced bond pads and recess for housing the qubit chip.
chip, and a ground-PCB that allows ‘make-before-break’ connections of all high-frequency lines to protect the device from electrostatic discharge.

A. Cryostat-PCB and Wiring

Fast voltage pulses for spin qubit control are produced using room temperature waveform generators and transmitted to the sample chip using semi-rigid coaxial cables thermally anchored in the dilution refrigerator using attenuators. The chip is mounted inside a light-tight cold-finger attached to the mixing chamber stage of a ‘cryo-free’ dilution refrigerator with base temperature \(\sim 18\) mK \([22]\). Impedance-matched microwave filters \((Z_0 = 50\ \Omega)\), constructed using magnetically lossy epoxy \([23]\), further thermalize and limit the frequency bandwidth of coaxial connections. Multi-stage cryogenic \(RC\) filters are used on all low-frequency wiring, which are shielded between room temperature and the cold finger. Using Coulomb blockade thermometry we measure an electron temperature below \(40\) mK with this high-frequency setup.

Custom cryogenic cables connect MCX- and SMA-type coaxial connectors at the cold-finger feed-throughs [see Fig. 1(b)] to the cryostat-PCB shown in Fig. 1(a). These custom cables are non-magnetic, hand-formable, and consist of a semi-rigid copper inner conductor, followed by a teflon dielectric wrapped with a silvered copper foil and a silver braid that serves as the outer conductor. High-frequency connectors on the cryostat-PCB are MMCX-type.

The cryostat-PCB is in strong thermal contact with the gold-plated, high-purity copper cold finger and remains attached to the refrigerator. On-board bias tees constructed from surface mount resistors and capacitors add true-dc, or low-frequency signals to the high-frequency readout and control lines. A ‘nano-D’ connector \([24]\) [shown in Fig. 1(a)] is used to connect these dc lines to the bias tees on the cryostat-PCB.

The set of interconnecting PCBs is shown as a rendered cartoon in Fig. 1(c) and Fig. 1(d). The boards are connected to each other using mini-SMP connectors \([25]\) and interconnect coaxial ‘bullets’ that allow a radial misalignment of \(\sim 0.4\) mm and an axial misalignment of \(\sim 0.7\) mm. The grounding-PCB is mated with the device-PCB during sample bonding and transport and ties all high-frequency connections to a common ground via 500 kΩ resistors that dissipate high voltage spikes that can otherwise shock the device. To make connection with the cryostat wiring the device-PCB is first mated with the cryostat-PCB before removal of the ground-PCB. The force required to separate the bullets from their connectors is specified such that all bullets remain attached to the cryostat- and grounding-PCBs, rather than the device-PCB. In this way the device is connected to a high resistance ground throughout.

B. Device-PCB

The chip is mounted in a square recess created in the circuit board by the use of multiple framing layers of Rogers 3003 laminate bonded together to build up the device-PCB, shown as a photograph in Fig. 1(e) and schematically in Fig. 2. Bond pads for the high-frequency signals emerge close to the chip on the high-frequency layer of the device-PCB, with dc bond pads located further away, on the top dc-layer. This creates a terraced bond pad structure that reduces the bond-wire length for high-frequency connections [see Fig. 1(f)]. The Rogers laminate has a thermal expansion coefficient matched to copper and exhibits a small variation in dielectric constant with temperature \((+13\) ppm / degree), ensuring that the impedance of planar transmission lines does not change when cooling. The laminate also exhibits a low loss \(0.0013\) dissipation factor and relatively high thermal conductivity, making it well suited to microwave cryogenic applications. We note that we have performed many thermal cycles of this PCB without degradation.

Metallic features on the device-PCB are defined using electroless-nickel electroless-palladium immersion gold (ENEPIG) finish which ensures strong wire bond adhesion. The board remains essentially non-magnetic as only a trace amount nickel is used as a sticking layer during PCB metal deposition and all components are non-magnetic. Connecting the ground planes and signal layers are a large number of ‘plated through’ vias that are plugged with epoxy so as to not trap gas that may otherwise act as a virtual leak under vacuum. These vias also suppress any parallel-plate capacitor resonance modes produced by metallic layers in the PCB \([20, 27]\).

The low dielectric constant of Rogers 3003 \((\epsilon_r = 3)\) allows the design to minimize crosstalk despite the high density of planar transmission lines. Constrained by the minimum feature size compatible with PCB manufacture, a low dielectric constant allows an impedance of \(Z_0 \sim 50\ \Omega\) to be maintained by having the ground-plane positioned a close distance underneath the signal tracks relative to the distance between neighbouring tracks. In this way, electric field lines stemming from the signal lines mostly terminate on the ground-plane beneath the transmission lines rather than terminating on adjacent signal tracks which would otherwise increase coupling \([28]\).

The layout of the individual layers of the device-PCB are shown in Fig. 2(a). The dc layer (top surface) of the device-PCB has 24 low-frequency signal tracks that connect bond pads [see Fig. 1(f)] to a 31-pin ‘nano-D’ dc-connector, shown in Fig. 1(e). The remaining 7 wires on the connector provide additional connections for thermometry, active device power, or cold light-emitting diodes. Each low frequency line is first filtered at the mixing chamber using low-pass \(RC\) stages embedded in magnetically lossy epoxy \([29]\) and shielded before entering the light-tight cold finger housing. This combination provides more than -60 dB of noise suppression for frequencies from 700 Hz to above 50 GHz. We additionally
make use of 7-stage surface mount low-pass filters \(80\) MHz cutoff frequency \[24\] located on the PCB close to the device, to suppress high-frequency crosstalk from rf to the dc lines [see Fig. 1(e)]. We note that mounting chip capacitors in place of these filters (on the PCB) can introduce parasitic resonances in the frequency band of control signals.

High-frequency signals are fed to the chip via 14 separate coplanar waveguides embedded on distinct layers of the device-PCB. Contact to the high-frequency layer is made using mini-SMP connectors mounted on the top (and bottom) surface of the device-PCB. The central pin of these connectors is soldered to a via that makes contact to either the high-frequency layer or tank-circuit layer of the device-PCB [see Fig. 2(a)]. These ground-covered coplanar waveguides have low dispersion and are adiabatically tapered from the \(Z_0 = 50\) \(\Omega\) SMP connectors to \(\sim 83\) \(\Omega\) at the bond pads to minimise impedance mismatch with the bonding wire geometry. Ground-planes separate each signal layer together with a fencing-via technique [30, 31], that effectively terminates electric field lines from high-frequency signal tracks in order to suppress crosstalk (see discussion below).

Electron spin resonance (ESR) is a method needed for spin qubit manipulation and typically requires microwave frequencies for excitation. To enable ESR we make use of 2 edge-mounted 2.40 mm microwave launchers [32]. These connectors maintain good impedance matching and signal integrity to 40 GHz and are connected to the chip using coplanar waveguide structures (ESR 1 and ESR 2) on the high-frequency layer of the device-PCB [see Fig. 2(a)]. These waveguides are again well isolated from other signal lines using fencing-vias.

Finally, on the bottom side of the device-PCB is the tank-circuit layer which contains solder pads for incorporating surface mount components in series with coplanar waveguides. We typically mount chip inductors here to implement \(LC\) tank-circuits for the purpose of impedance matching to charge sensors needed in rf reflectometry [33] for spin readout [10]. The 8 solder pads differ in size to accommodate the range of surface mount gauges. The presence of metal structures proximal to the inductor mounts are minimized to reduce parasitic capacitance (measured to be \(\sim 0.2 - 0.3\) pF).
III. CROSSTALK AND SIGNAL FIDELITY MEASUREMENTS

Having described the layout of the cryostat- and device-PCB we now present low temperature measurements characterizing the crosstalk and transmitted signal fidelity of the coupled PCB architecture. Measurements are made with a calibrated vector network analyzer [34] at a temperature $T \sim 5$ K using a high-frequency cryogenic probe-station [35]. We have verified that microwave $S$-parameters do not change when the PCB is cooled further to milli-Kelvin temperatures.

Beginning with the edge-mounted microwave launchers used for ESR, Fig. 3(a) shows the crosstalk (red) and transmission performance (blue) of the device-PCB. Crosstalk from the two planar transmission lines is determined via a measurement of $S_{21}$ between the unconnected ports, ESR 1 and ESR 2. We find a maximum crosstalk of $\sim -40$ dB at frequencies above 10 GHz. The transmission performance [shown in Fig. 3(a)] is determined by connecting the bond pads with long bond wires where they terminate close to the chip cavity and again measuring $S_{21}$ between ports ESR 1 and ESR 2. The bond-wires are required to perform a transmission measurement but lead to addition loss and parasitic resonances from the bond wire partial inductance and stray capacitance. Without losses from the bond-wires, numerical simulations [36] indicate that transmission drops to $S_{21} \sim -3$ dB at $\sim 13$ GHz. We note that these coplanar waveguides have the shortest distance between them of all the signal lines on the PCB and exhibit the strongest crosstalk. The 14 transmission lines that use mini-SMP connectors to make contact with the high-frequency layer are designed for carrying control pulses with a bandwidth...
FIG. 4: We examine the effect of the fencing-via technique on the EM coupling and crosstalk between signal lines. (a) Layout of the high-frequency layer of the device-PCB showing zoom and electric field strength obtained using EM simulation software [36] [see scale bar in (c)]. An input voltage amplitude of 1 V is applied to the port SMP 1 at a frequency of 40 GHz. (b) Crosstalk between high-frequency ports SMP 1 and SMP 6 in a bandwidth 0 - 6 GHz. Simulation software is used to evaluate crosstalk when fencing-vias are used (red dashed line) and not used (blue dashed line). (c) Numerical simulation of the field strength in a cross-section of the high-frequency layer of the device-PCB, again at 40 GHz. The magnitude of the electric field is shown with (top) and without (bottom) fencing-vias. (d) Shows magnetic field strength comparing the coupling between ports, with and without fencing-vias for conditions as in (c). A reduction in the coupling strength of electric and magnetic field is seen when fencing-vias are implemented. A via diameter of 0.38 mm is used with a via centre-to-centre spacing of ~ 0.6 mm.

below ~ 6 GHz. The performance of these interconnects is shown in Fig. 3(b) for two neighbouring lines. A loss in transmission of $S_{21}$ ~ -1 dB is observed, again using bond-wires to connect signal tracks near the chip cavity to allow the transmission measurement. Crosstalk between adjacent lines remains below -40 dB for frequencies up to 6 GHz.

Readout interconnects on the tank-circuit layer are investigated via measurements with, and without, surface mount inductors soldered to nearest neighbour transmission line pads [see Fig. 3(c)]. In both cases, readout line crosstalk is larger relative to the performance of the lines on the high-frequency layer shown in Fig. 3(b). This is because, in the case of the tank-circuit layer, the signal tracks are on the back surface of the PCB and do not have a covering ground plane to enhance shielding. Tank-circuit resonators used for readout typically operate however, at frequencies below 3 GHz, where crosstalk remains less than -40 dB. The use of inductors to create tank-circuit resonators leads to an increase in crosstalk at the resonant frequency of the respective tank, likely because of the magnetic flux that threads the mutual inductance of the two surface mount components. Such crosstalk can be mitigated by separating tank-circuits that are close in resonant frequency or orienting inductors perpendicular to each other.

Finally, we evaluate the crosstalk between different layers of the device-PCB, with data shown in Fig. 3(d). Crosstalk is strongest for pairs of transmission lines that align or are proximal with each other, despite being on separate PCB layers. This is likely due to shared screening currents that flow in the common ground-plane. Additional coupling occurs at the end of the signal tracks where the ground layer has been removed to enable bonding to the chip.
IV. CROSSTALK MITIGATION

Traditional sample-chip mounting methods, widely used in nano-electronics experiments, do not make use of the multi-layer circuit board techniques described here. The high density of interconnects needed for control and readout of multi-qubit devices however, leads to a crowding of high-frequency planar transmission lines at the PCB layer and a significant increase in crosstalk. In an effort to mitigate crosstalk when requiring large numbers of interconnects, we make use of continuous fencing-vias to tie together the ground planes above and below high-frequency transmission lines. This method essentially creates a quasi-coaxial grounding geometry surrounding the central conductor, as illustrated in Fig. 4(a) for the case of the coplanar transmission lines implemented on the high-frequency layer of the device-PCB. Using numerical simulation [36], we evaluate the effect of these fencing-vias and find that they decrease crosstalk between closely aligned signal tracks by \( \sim 25 \text{ dB} \), as shown in Fig. 4(b).

The residual crosstalk is largely due to the presence of screening currents flowing in the common ground between signal lines. Figures 4(c) and 4(d) show the result of a numerical simulation [36] for the electric and magnetic field density in a cross-section of the high-frequency layer of the device-PCB. The presence of fencing-vias can be seen to mitigate crosstalk by strongly suppressing the electric field between the transmission lines. A weaker suppression is seen for coupling produced by the magnetic field component.

V. DISCUSSION AND CONCLUSION

The use of multi-layer ground-planes and the fencing-via method analysed here represent an approach to mitigating crosstalk in PCB architectures that require a high density of wide bandwidth interconnects. We have not addressed the significant crosstalk and signal degradation that can occur on chip, but note that there are many approaches to suppressing crosstalk at the device layer [37]. As capacitance and mutual inductance between two conductors is proportional to their length, the contribution to crosstalk by on-chip structures can be small in comparison to the longer interconnect features required at the PCB layer. On-chip crosstalk can also be minimized with the appropriate use of ground guards between signal-carrying transmission lines [15] [37]. For qubit structures however, this is challenging as device operation requires significant capacitive coupling between surface electrodes and the quantum dot structures used to confine electron spin qubits. This direct cross-coupling then sets a lower bound for the level of indirect crosstalk tolerable at the PCB layer: it should be much less than the unavoidable coupling at the device layer, which is typically of the order of a few percent (\( \sim -40 \text{ dB} \) for GHz voltage pulses). We note that we have measured high-frequency crosstalk to be as high as \( \sim -3 \text{ dB} \) for a range of commercially available chip-mount packages commonly used in nano-electronic and qubit experiments.

In conclusion, we have described a coupled-PCB platform designed to enhance the operation and testing of spin qubit devices in the regime where a high density of interconnects are needed. The platform is well suited to frequent re-bonding of device chips with different geometries and performs well at cryogenic temperatures and in the presence of magnetic fields. Crosstalk is strongly suppressed below \(-40 \text{ dB} \) (1% for voltage amplitudes) for all control and readout transmission lines by making use of a multi-layer device-PCB with alternating ground planes and fencing-vias.

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