Low Temperature SLID Bonding Approach in Fine Pitch Chip-stacking Structure with 30 μm-pitch Interconnections

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Abstract
In this study, a 160°C low-temperature bonding method was developed for fine pitch chip-stacking application by Solid-Liquid Inter-diffusion (SLID) bonding technology. The chip-to-wafer test was conducted by using Cu/Sn-Ag and Cu/Ni/In as the micro pillar bump structure for top chip and bottom wafer, respectively. Indium, with a low melting point of 157°C, was chosen to realize the SLID bonding mechanism in this study. A thin indium layer with a thickness of 1 μm was plated on nickel to induce low temperature bonding with tin. These 30 μm-pitch interconnects bonded at low temperature were well-bonded and exhibited excellent electrical continuity through 3,264 I/Os. Furthermore, the bonded samples were tested under reliability assessments to verify the thermal stability.

Keywords: Chip to Wafer Bonding, Indium, Indium-tin, 3D Integration, Reliability

1. Introduction
As the rapid development in hetero-integration, organic substrates have been widely used in 2.5D and 3D packages to achieve the high speed transmission. Therefore, in order to reduce the warpage effect and enhance the reliability performance of micro joints, minimizing the CTE mismatch as well as the residual stress between packages and organic substrates are crucial.[1] Thus, low-temperature bonding technologies have been widely studied to meet this growing demand.

Among many low-temperature bonding techniques, Solid-liquid interdiffusion (SLID) bonding is a potential bonding method because the joint materials can be bonded at low temperature and applied in a high temperature environment.[2] Indium has been considered as bonding materials used for hybrid pixel detector systems due to its low melting point, high ductility, good mechanical and electrical properties in a broad temperature range.[3]

In this work, a low-cost bonding process by electroplating indium with the thickness of 1 μm is introduced to achieve SLID bonding at 160°C, focusing on its electrical properties and reliability investigations. The daisy chain resistance of the bonded structures remained stable after reliability tests, showing an excellent potential in heterogeneous integration with low thermal budget.

2. Experimental Procedure
To realize SLID bonding, In/Sn system and Cu were chosen as low-temperature melting metal and high-melting-point component. The specifications of the chip-to-wafer test vehicle were listed in Table 1. and the process flow was shown in Fig. 1. The surface treatment process by Ar plasma mixed with 5% H2 was used to remove the surface oxide before bonding. The plasma treatment was carried out for 100 seconds at 350 W. The thermal compression bonding test was carried out by Toray FC-

| Table 1 Specifications of the test vehicle. |
|---------------------------------------------|
| Dimension (mm)                              |
| 5.1 × 5.1                                   |
| Bottom wafer                                |
| 200 × 200                                   |
| Thickness (μm)                              |
| 600                                         |
| 725                                         |
| Bump diameter (μm)                          |
| 18                                          |
| 18                                          |
| Bump pitch (μm)                             |
| 30                                          |
| 30                                          |
| Bump height (μm)                            |
| Cu/Sn-2.5Ag (5/8)                           |
| Cu/Ni/In (5/2/1)                            |

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3000WS bonder with an alignment accuracy of ± 2 μm. After chip-to-wafer test, scanning electron microscope (SEM), focused ion beam (FIB), and electron probe micro analysis (EPMA) were used to examine the microstructure and identify the chemical composition of the intermetallic compounds. Daisy chain circuits with 3,264 I/Os were designed to measure the electrical continuity of 30 μm-pitch interconnections after bonding process and reliability test. Afterward, temperature cycling test (TCT) based on the JESD22-A104B standard was performed under the temperature range of −55 to 150°C. High temperature storage test (HTS) was tested under 150°C for different time periods based on the JESD22-A103 standard. The failure criterion in TCT and HTS was considered as the variation of daisy chain resistance over 15%.

3. Results and Discussion

A well-bonded interface of the chip-on-wafer sample at 160°C for 1 minute was evaluated by SEM, FIB and EPMA, as shown in Fig. 2 and Fig. 3. In addition, according to the EPMA result, indium was apparently diffused to top die and consumed quickly to formed (Cu,Ni)_{6}(Sn,In)_{5} IMCs, transforming the joints into full intermetallic joints. The presence of (Cu,Ni)_{6}(Sn,In)_{5} IMCs with a high melting point of 500°C allowed applications at higher processing temperature.

As shown in Fig. 2, some kirkendall voids were formed at the Cu/solder interfaces after bonding process. The electrical measurement was conducted to verify whether the kirkendall voids would affect the reliability of micro joints. The daisy chain resistance of TCT samples was checked at different time intervals of 0, 250, 500, 750 and 1,000 cycles; while that of HTS samples was checked at different time intervals of 0, 100, 250, 500, 1,000 hours. As shown in Fig. 4 and Fig. 5, the variation of daisy chain resistance after temperature cycling test (TCT).
resistance was 4.27% and 4.16% without any electrical failure after temperature cycling test (TCT) 1,000 cycles and high temperature storage test (HTS) 1,000 hours, respectively. The result showed that the joints remained very good electrical property after TCT and HTS test. The electrical result was also consistent with the cross-sectional view in Fig. 6, showing a well-bonded interface without cracks after TCT 1,000 cycles. Therefore, the presence of kirkendall voids would not affect the reliability of micro joints.

4. Conclusions

In this work, a chip-to-wafer SLID bonding method by a thin indium layer has been proposed for low temperature bonding technology. Some important results are summarized in the following.

1. The bonding process was completed at 160°C for 1 min, realizing a low temperature and time-saving method for 3D integration application.

2. The electrical measurement results showed stable daisy chain resistance through 3,264 I/Os after TCT and HTS. The result proves the In/Sn-Cu bonded interconnections can withstand large temperature variation and survive in a high temperature environment for a long term.

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