Methods for designing electrical equipment for testing VLSI used in aviation digital information systems

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Abstract. Very-large-scale integrated circuits are widely and successfully used in the artificial intelligence systems and digital signal processing systems on board modern aircraft and space apparatuses through the implementation of complete digital systems on a chip. However, the level of integration of very-large-scale integrated circuits according to Moore's Law continues to double every 2 years, and today the test equipment for their functional control is working to the limit of its capabilities. Since the development of interface boards (the main unit of test electrical equipment) for testing microcircuits is currently carried out manually, the timing of the release of microcircuits is unacceptably increasing. This article presents the original methods for automating the design of an interface board circuit using the information contained in the test vectors. By eliminating the human factor from the development process of this board, time is significantly reduced and design errors are eliminated.

1. Introduction
The world fleet of aircraft and spacecraft for various purposes is constantly being updated. Flight safety and efficiency increase, flight weight decreases, functionality of modern liners increases, aircraft control becomes more comfortable. These improvements are achieved through the introduction of the powerful automated control systems on board the aircraft, which are implemented using the latest element base – very-large-scale integrated circuits (VLSI). For example, to ensure the proper safety of passengers and crew of aircraft, they can be equipped with an artificial intelligence system, implemented using a VLSI “system-on-chip”, “on board” of which there are up to a billion transistors [1,2]. The specified level of VLSI integration allows the implementation of the entire multicore processor on a single crystal. The installation of a powerful built-in computer system on board the aircraft based on the named processors will provide the ability to process service and scientific information in real time [3] with high reliability of transmission of the corresponding protocols [4,5]. In parallel, the weight and volume of the computer system will be sharply reduced. However, to achieve the above, it is necessary to increase the level of integration of modern VLSI at least 2-3 times. Currently, the existing test equipment on the market, even working at the limit of its capabilities, barely copes with testing modern VLSI. The fact is that a feature of modern production of VLSI with an integration level of 10⁹ is the use of the latest ultrapurpore materials and high-precision control equipment. In addition, the parallel reduction of technological standards for VLSI design to
16 nm leads to an increase in the influence of external factors on the operation of VLSI, an increase in the volume and complexity of test vectors [6], and a decreasing in the operational reliability of VLSI [7-9]. As a result, the effectiveness of the existing VLSI technical control methods becomes directly dependent on the quality of the feasibility study. Its most important part is the interface board, shown in figure 1, which implements the connection between the VLSI under test and the test equipment [10].

Typically, each new type of integrated circuit (IC) and/or each new piece of new equipment requires the design and manufacture of a new interface board. At the moment, there is no application or automated production complex that allows you to automate the stages of its design [11]. Therefore, engineers at IC manufacturing enterprises are engaged in the development of tooling in manual mode according to the scheme shown in figure 2 [12]. The only the program tool which currently accelerating the test electrical equipment (TEE) development process is the Microsoft Excel package. That package is notable for its ease of data processing. In terms of content of TEE design process, so today it is as follows [13,14].

![Image of TEE printed board on a metal frame.](image1)

**Figure 1.** The test electrical equipment printed board on a metal frame.

![Diagram of TEE interface board design stages.](image2)

**Figure 2.** Basic design stages of the interface board for TEE.

At the first stage, specialists study the documentation for new equipment and/or a new type of IC. The results of information processing at the second stage are: a standardized list of pins, sheets with IC configuration options and channel assignments, and a sheet with a description and visual representation of the IC pins. Here the scan pins are yellow; pins that require parallel connection to equipment through a relay to the channels used for polling in a queue format are green; ground and power pins are blue. The signal pins are colorless.
The third and fourth stages are the most time consuming, as here the engineer manually fills in a table of more than 1000 lines in Microsoft Excel program. And here the task is multiplied complicated if it is necessary to install two contacting devices on the board and, accordingly, two microcircuits, as it shown in figure 4 [15, 16]. This stage takes a lot of time and requires the utmost concentration of attention. To assign channels correctly, the designer must pay attention to the presence of scan-outputs in the group, and not to allow the presence of conductor intersections on the printed circuit board. The fifth stage involves checking the completed assignments. The engineer searches for repeating channels, intersections of future traces and the correct connection of the special group’s pins. The presence, for example, of only one repeating channel returns the developer to the previous stage and leads to the need to reassign all group of pins again (up to 64 pins).

The main point of the sixth stage - the stage of drawing up a technical task for the development of a printed circuit board for electrical equipment – is the preparation of a pin assignment table obtained when performing stages 4 and 5. This table is an important tool with which engineer can track errors. The seventh step is routing the printed wires on the printed circuit board. This stage is final if the tracing is 100% successful. Otherwise, the developer goes back to stage 3 or 4. Thus, the process of TEE designing is very time consuming, and requires an increased concentration of attention from the engineer throughout the entire development process.
The purpose of this article is to develop methods to significantly reduce the complexity of the design stage of the TEE interface board by automating it. Note that the authors did not find analogues of the methods developed here in the domestic and world literature.

2. Methods and methodology

In this work, in essence, the problem of generating a list of circuits and a list of elements for designing an interface board and assigning VLSI pins to the tester's channels is solved. Full automation of these two stages allows parallel automation of all "manual" stages of the interface board design shown in blocks 1 through 6 in figure 2, since in this case the subjective factor will be excluded from the development process.

2.1. Methods of generation the TEE board

Note that the automation of data preparation for the development of a schematic diagram at the stage of production testing of the IC allows, without further participation of the developer, also prepare a list of contacts for the further operation of assigning the tested pins of the IC onto the tester channels. This becomes possible, since all the information necessary for carrying out these stages is already contained in the test vectors prepared at the stage of describing tests for functional testing of VLSI. So at next step there is remaining to program the selection of this information from the test and bring it to the computer aided design (CAD) format of the enterprise. All computational experiments to solve that problem had done by the authors in the development environment the tests of functional control VLSI Functional Test Studio (FTStudio), developed by K K Smirnov [8].

Note also that the source functional control tests are prepared in the FTStudio system in the system language (STeeL) and contain not only the data necessary to generate the net list, but also the necessary links to the element base of the interface board being developed. If due to the limitations on the number of tester channels it is necessary to split the test in half, the program will automatically create circuits for two different boards under each test. Test vectors contain information about chip pin assignments to the information signals, about function blocks and switching circuits to be tested. Additionally, the test vectors contain variable test tables, digital signal processing algorithms, and procedures for generating the necessary signals based on the results of calculations performed using these algorithms.

The implementation of the procedure for generating an electrical circuit based on the information contained in the test vectors is performed using mechanisms for automatically setting channel numbers, duplicating and switching channels, as well as mechanisms for setting various test configurations. An example of the above is figure 5, which demonstrates the automatic creation of a test for equipment with fewer channels than of the signals of the tested VLSI.

![Microcircuit under test](image)

**Figure 5.** Splitting the test in case of lack of channels on the tester.

An alternative to dividing the test is to use the switching circuit of the output signals of the IC under test according to the circuit in figure 6, where the test algorithm is restarted several times. In that case control is carried out alternately for different groups of output signals. When forming the test vector, the multiple launch of the testing algorithm is taken into account with alternate monitoring of various output signal groups and setting the corresponding values on the switching signals [15, 17].
In addition, the STeeL language allows the configuration of the project according to the scheme in figure 7, allowing the testing algorithm to be described in such a way that the electrical equipment, the model of the tested product and the functional test itself are described as single project in one language.

2.2. Assignment of IC pins onto the tester channels
Modern integrated circuits implement simultaneous support for up to ten or more interfaces [18], some of which use differential signal pairs. This circumstance must be taken into account when solving the problem of assigning equipment channels to IC contacts in an automatic mode. This problem is a special case of the well-known transport problem [8] and its formal solution in the FTStudio system is performed using the Hungarian algorithm [13, 19] with helping the device under test board and tests socket components. The first component is responsible for connecting the channels of test equipment to the contacts of the IC, and the second for the seats of the contact devices installed on the printed circuit board [20]. The main difficulty in implementing the Hungarian algorithm here lies in choosing a suitable optimization criterion that is able to provide a “planar” assignment result, shown in figure 8a. For example, assignment based on the criterion of increasing the distance between pairs of contacts will lead to the situation shown in figure 8b. To explain the criterion by which the solution shown in figure 8a is obtained, consider the board topology in figure 9.

The section of the printed circuit board inside in circle contains a typical fragment of the desired topology in the form of a V-shaped branching of differential pairs, the intersection of which is unacceptable. Here the set \( \{T\} \) of contacts is connected to the set of contacts \( \{P + S\} \) by binary edges and it is required to find such a mapping:

\[
\{T\} \Rightarrow \{P + S\},
\]

in which the resulting set of binary edges has not the intersections.
Figure 8. The result of destination the differential pairs by the criterion: “minimum the intersections” (a) and “increasing distance” (b).

Figure 9. V-shape branching of differential pairs.

We will call this set the “optimal set” and show the procedure for generating it on a model problem in which the total number of vertices of the set \( \{T\} \) is 4. Let us will distribute the vertices over the sets as follows: \( \{T\} = \{A, B, C, D\} \); \( \{P\} = \{a, b\} \); \( \{S\} = \{c, d\} \) (figure 10a). It makes no sense to solve this NP-complete problem by the "brute force method", since the value of N can reach one and a half thousand, and the computational difficulties begin after a dozen matchings. The problem is solved by choosing the next criterion of cost: “the number of intersections of the next edge with the edges that model the all rest of the matchings”. The complete graph of these matchings is shown in figure 10b, and the corresponding cost matrix is shown in table 1. Here the following designations are introduced: Down Row (Up Row) – the tops in figure 10 of the lower (upper) row.

Figure 10. To the solution the task of minimizin of the ribs graph intersections.
So the problem posed is NP-complete. The variant of its solution, shown in figure 10a, using the method “connect each vertex to the vertex nearest to it”, as we see, does not eliminate intersections. The final solution the task of assignment, marked in table 2 by the asterisk symbols, shows that the resulting assignment, firstly, the only one, and, secondly, the corresponding to it graph of matching does not have intersections. The solution found in this way is shown by the "red" lines in figure 10b. When preparing target matrices, variable information regarding the net list of the new interface board is selected directly from the test vectors as well as from the CAD component descriptions. Further, this information is processed and combined with the permanent part in order to take into account the radio elements previously placed on the board, which the future routes must “bypass”.

| Table 1. The Initial matrix of cost. | Table 2. The resulting matrix of cost. |
|------------------------------------|---------------------------------------|
| **Down Row** | **Up Row** | **Down Row** | **Up Row** |
| **a** | **b** | **c** | **d** | **a** | **b** | **c** | **d** |
| A | 0 | 3 | 6 | 9 | A | 0* | 2 | 5 | 9 |
| B | 3 | 4 | 5 | 6 | B | 0 | 0* | 1 | 3 |
| C | 6 | 5 | 4 | 3 | C | 3 | 1 | 0* | 0 |
| D | 9 | 6 | 3 | 0 | D | 9 | 5 | 2 | 0* |

3. Results and discussion

3.1. Example of generation the TEE board

As we can see, the STeeL language allows lets us to form the project structure in the FTStudio environment in accordance with the diagram in figure 7 such, that the electrical equipment, the model of the tested product and the functional test itself are described as a single project. This opportunity are provided a component-oriented principle underlying the implementation of the STeeL language, which is understood as a set of tests and automatically generated technical data for the development of electrical equipment, including the electrical schematic diagram of the interface board. At the same time, the components can be described both in the STeeL language itself, and in other programming languages, or presented in the form of logical equations, tables, etc. Each such component is represented in the FTStudio system by a logical model of a digital device with inputs and outputs, through which it can be connected with other components, and the result of compiling a test project is the test solution itself.

If the project is compiled for a format with a small number of digital channels, the compiler automatically divides the test vector into several vectors that test individual blocks of the circuit. Thus, the prepared test vectors are used twice at the VLSI manufacturer. At the first stage, tests are run in the FTStudio environment to automatically obtain a configuration of electrical equipment for the enterprise's test equipment park. And only after the development of the interface board, which acts as a connecting link of the tested VLSI with the channels of the test equipment, the second stage is performed – the stage of testing the VLSI by running the same test vectors, using a same of hardware and software complex (FTStudio).

As mentioned above, the most time-consuming operation in the manufacture of an interface board, still performed manually, is the assignment of VLSI pins to the channels of the test equipment. Taking into account the growth rate of the level of integration of modern VLSI, one should expect in the next 4-5 years a corresponding increase in the number of its outputs (N) to several thousand. This circumstance can become a serious computational problem, since the complexity of its solution is proportional to the value of N^3 [19], which is confirmed by the graph obtained by the authors in figure 11 (Variant 1).
Below is an example of a description in STeeL language of an algorithm for developing a functional test and an interface board of the simplest combinational device for the AdvanTest V93000 logic analyzer:

```
// interface board schema generation
[COMPILER("GenerateShematic"), PACKAGE(P108), TESTSOCKET(UK108)]
#steel
// generation a test and a interface board schematic for the Advantest V93000 tester
config "V93000"
group "INsignal"
// tester channels for pins D0..D2, Q0..Q2, sel are automatically selected by the compiler
pin ["D [3]", "Q [3]", "sel"], IN, INsignal, AUTO
// the channel for F output is assigned by the algorithm designer
pin "F", OUT, 11316
// description of the model (schematic) of the device under test
wire ["Line1", "Line2", "Line3", "Line4"]
and D0, D1, D2, sel, Line1
and Q0, Q1, Q2, sel, Line2
or Line1, Q2, Line3
or Line2, D2, Line4
xor Line2, Line3, Line4, F
// supply of influences on the described model
// enumeration of all possible values of input signals D0..D2, Q0..Q2, sel
// ("INsignal" group) and calculating the output signal F on each test cycle
biegr "seq", "INsignal"
cycle (seq.Count)
    nextc seq
end
#end
```

Here there are declares the inputs D [3], Q [3], and sel, followed by the AUTO keyword to tell the compiler to automatically connect the output pin of F to channel 11316 of the tester. The following is a description of the model of the device under test, according to which the calculation of the logical value at its output will be performed. To speed up the enumeration of all signal values at the inputs in a random
order, the bijection algorithm of the set of input signal values $D$, $Q$, and sel is used. As a result of compiling the program, files with a test table, pin description files, files of timing and waveform and a file with a description of the electrical circuit of the interface board will be created. This circuit is shown in the figure 11.

3.2. Decreasing a time of solving the matchings problem

The interface board descriptions files are used to define locate the pads of the tester channels and the pads of the device under test on the board. The location of these pads is used further to calculate the minimum lengths of mutually non-intersecting lines between the leads of the tested product and the equipment channels. The algorithm for this calculation was described in section 2.1. Figure 12 shows a graph of the dependence of the time for solving the assignment problem on the number of matchings. The analysis of the execution time of individual operations in the general computation cycle showed that here the operation of calculating the presence of intersections of two segments turned out to be the longest computational procedure. As a result, as the graph in figure 12 shows, when the number of the IC contacts is more than 640, the solution time increasing sharply, and that additional research have required in terms of increasing the efficiency of solving this problem.

![Figure 12. Graph of time dependence for solving the assignment problem on the number of matchings.](image1.png)

The fact is that the number of pins of the tested microcircuits already today is about one and a half thousand and is constantly growing. To reduce the time for solving the assignment problem, a number of additional computational experiments were carried out, as a result of which this time was reduced by exactly 4 times. As a result, the task of assigning 2500 contacts to the tester's channels (see the variant 2 scale in figure 12) takes only an hour and a half of machine time, which is more than acceptable for practice. This effect was achieved by distributing the total number of hits across four sectors (A, B, C, and D), located as shown in figure 13. With this approach, matches from sectors B, C and D do not take part in the process of solving the assignment problem for sector A. Similarly, comparisons from sectors A, C and D do not take a participate in the process of solving the assignment problem for sector B comparisons, and so on. If the value of N will be doubled, it is necessary to use 8 sectors instead of the 4, shown in figure 13 in order to stay within an acceptable time frame for solving this problem.

4. Conclusion

The current state of designing of digital VLSI used in digital information processing systems on board modern aircraft and spacecraft is analyzed. The modern process of developing electrical equipment for the functional control of VLSI was described step by step and the problems of the VLSI test designing in connection with the growth of the integration of digital microcircuits are considered. An original technique for designing an interface board is proposed and implemented, which allows to automatically
generate its schematic diagram based on the information contained in the test vectors. It is noted that there are no analogues to this method in world practice.

A criterion for assigning (without intersections on the interface board) differential pairs to test equipment channels is proposed, which allows to drastically reduce the complexity of solving this problem by using the classic "Hungarian algorithm". An estimate is given of the time required to solve the problem of distributing differential pairs over the channels of test equipment, depending on the number of contacts of the tested VLSI, and an algorithm for reducing this time is described.

The methods proposed in the article are implemented within the FT-Studio hardware and software complex. Its use allows today to move on to solving the problems of interoperative analysis of test results, without which testing the next generation VLSI on modern test equipment will become simply impossible. In addition, the application of the developed methods within the FTStudio complex opens up prospects for solving in an automatic mode the problem of evaluating the suitability of crystals using neural networks.

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