Accelerating complex control schemes on a heterogeneous MPSoC platform for quantum computing

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ABSTRACT
Control and readout of superconducting quantum bits (qubits) require microwave pulses with gigahertz frequencies and nanosecond precision. To generate and analyze these microwave pulses, we developed a versatile FPGA-based electronics platform. While basic functionality is directly handled within the FPGA, guaranteeing highest accuracy on the nanosecond timescale, more complex control schemes render impractical to implement in hardware.

To provide deterministic timing and low latency with high flexibility, we developed the Taskrunner framework. It enables the execution of complex control schemes, so-called user tasks, on the real-time processing unit (RPU) of a heterogeneous Multiprocessor System-on-Chip (MPSoC). These user tasks are specified conveniently using standard C language and are compiled automatically by the MPSoC platform when loaded onto the RPU. We present the architecture of the Taskrunner framework as well as timing benchmarks and discuss applications in the field of quantum computing.

1. INTRODUCTION
Quantum bits (qubits) are the elementary building blocks of a quantum processor. While a variety of different qubit implementations exist [17, 21, 30], superconducting circuits represent a promising candidate that is actively used and investigated by many groups in the field [10, 16, 18]. In the last couple of years, the focus shifted from mostly physics-driven research focusing on qubit types and properties towards a more comprehensive, interdisciplinary system perspective [2, 11, 31]. In order to build a quantum computer, the full software and hardware stack [4, 12, 13] must be considered. One of the key requirements is a quantum-classical interface to control the quantum processor.

Systems based on superconducting qubits [10, 16, 18] require microwave pulses with gigahertz frequencies and nanosecond precision for readout and control [6, 19, 32]. A quantum-classical interface thus needs to be able to transform classical instructions into such microwave pulses that then interact with the qubits. Furthermore, the response of the setup needs to be monitored and analyzed in order to determine the qubit states. We developed a versatile electronics platform based on a field-programmable gate array (FPGA) that provides such an interface for superconducting qubits. The most important functionalities, like scheduling microwave pulses with nanosecond accuracy and evaluating readout responses, is directly implemented on the FPGA. Control schemes that require challenging parameter variations and advanced data evaluation are implemented in software. This combines the advantages of a versatile and fast software development process with the benefits of highly parallel data processing and nanosecond precision on the FPGA.

We utilize a heterogeneous system architecture based on the Xilinx Zynq UltraScale+ series which combines the FPGA with an ARM Cortex-A53 application processor (APU) and an ARM Cortex-R5 real-time co-processor (RPU). By providing a software running on the RPU called Taskrunner, the user can easily implement and load complex experiment schemes during run-time. This is complemented by on-the-fly compilation of the user task on the APU. The RPU is closely connected with the FPGA domain which enables it to quickly and deterministically access hardware registers. It also provides the ability to perform further data reductions in software.

In the following, we will give a brief introduction into the fundamentals of interfacing with superconducting qubits and related work in the field. This is complemented by an introduction into the used hardware, our platform architecture and the interaction between the components. In the main chapter of this work, we present the Taskrunner framework. After elaborating on the architecture, we give insights into different aspects of the Taskrunner. This ranges from the initialization process over loading and executing a user task up to the interface used to exchange information and data with the external client. Finally, we provide timing benchmarks for the most common use-cases and present selected applications in experiments with superconducting qubits.

2. FUNDAMENTALS

2.1 Interfacing superconducting qubits
Qubits are artificial atoms that can be interacted with by employing light-matter interaction [16, 20]. Therefore, microwave photons with frequencies of a few gigahertz are regularly used to manipulate and readout the state of superconducting qubits [6, 18, 32].

Qubits are operated fundamentally different than classical bits. While information of classical bits is represented as electrical voltages, quantum bits have a quantum mechanical state comprising two fundamental states called $|0\rangle$ and $|1\rangle$. In contrast to classical bits, arbitrary superpositions of these two states are possible and can be exploited for computations [3].
2.1.1 Qubit gate operations

For most qubit implementations, gates are also realized differently than on a classical computer. There, gates are stationary circuits built out of transistors through which the bits are passed through in form of electrical signals. In quantum computing, especially for superconducting qubits, the qubits themselves are stationary and gate operations are performed by applying microwave and/or current pulses to the qubit circuitry. With typical frequencies of multiple gigahertz and pulse durations of a few tens of nanosecond, high sampling quality and speed is necessary in order to achieve accurate qubit gates [7].

Quantum computing algorithms comprise a sequence of gate operations and thus microwave pulses. Timing of these pulses is critical and the phase jitter can easily compromise the calculations [5, 8].

2.1.2 Qubit state measurements

Qubit state measurements play a central role in every quantum algorithm, be it to obtain the result at the end of the calculation or to influence the algorithm through measurement back action [14]. In quantum computing, measuring qubits will influence their state after the measurement. While, during calculation, the qubit can be in any arbitrary superposition, the readout will result in either the $|0\rangle$ or $|1\rangle$ state. The probabilities of the two possible measurement outcomes are given by the superposition. After the measurement, the superposition is destroyed and the qubit is in the detected state. This is called a projective measurement and characteristic for experiments in quantum mechanics [23].

This also implies that, in order to obtain the probabilities, one cannot simply repeat the measurement operation numerous times. Instead, one needs to repeat the whole pulse sequence to end up with the same superposition prior to the projective measurement. For quantum computing, one therefore tries to formulate the algorithm in a way that, prior to the measurement of the final result, the qubit is in one of the two states $|0\rangle$ or $|1\rangle$.

2.1.3 Parameter variations and averaging

In research on superconducting qubits, on the other hand, the probabilities are of great interest. Therefore, many repetitions of the pulse sequences will be performed in order to obtain suitable statistics. This is often combined with parameter variations to investigate the qubit state dependency on these parameters. The order of averaging and parameter variations can have a large impact on the measurement result if low frequency noise is present in the system.

When first averaging for one parameter set, a currently present noise bias will be incorporated into the signal. For the next parameter configuration, the bias might have changed if the noise frequency is on the order of the parameter change rate. To give an example: A single pulse sequence takes 10 μs and we perform 1000 averages per parameter configuration. That implies a parameter change every 10 ms or a rate of 100 Hz. Thus, it makes the experiment outcome highly sensitive to noise on this time scale, like 50 Hz noise. It is therefore generally advisable to first change the parameters and average afterwards. While this is conceptually easy, depending on the experimental setup, it might be difficult to implement efficiently.

2.1.4 Qubit relaxation delay

In order to obtain reproducible results, it is furthermore important that the qubits are all in the same state before each pulse sequence starts. In the most simplest case, this is achieved by waiting a sufficiently large time interval after the last sequence. The qubit is very fragile and its state decays exponentially into the $|0\rangle$ state on a time scale $T_1$, called energy relaxation time. Typical $T_1$ times for superconducting qubits range from $1 - 100\,\mu s$ [16, 28]. Therefore, one typically waits on the order of five to ten times the $T_1$ time to ensure that the qubit is relaxed into $|0\rangle$ and one has comparable starting conditions.

2.1.5 Dispersive qubit readout

Returning to the measurement itself, this is normally performed as so-called dispersive readout [6]. In that case, the qubit is coupled to a microwave resonator leading to a slight shift of the resonator frequency depending on the qubit state. By probing the microwave resonator with a readout pulse, typically a few hundred nanoseconds long, one can extract the qubit state. It is encoded in the phase information of the reflected microwave pulse. By performing heterodyne IQ mixing and a digital down-conversion, the in-phase and quadrature components of the signal can be obtained, and thereby the phase information. In Fig. 3, the measurement result of an actual qubit experiment is shown.

2.2 Related work

Research institutions working with superconducting qubits widely use generic laboratory equipment to generate and analyze the necessary microwave pulses. This includes arbitrary waveform generators (AWGs), vector network analyzers (VNAs) and signal analyzers (SAs). They are suited for fast testing of circuits and performing experiments with simple pulse sequences. With increasing system complexity, utilizing these devices becomes unfeasible due to significant communication delays, bad scaling properties and high relative cost. Complex data processing like calculating correlations is also inefficient or even impossible to realize with such setups. Therefore, FPGA-based systems emerged in different research groups specifically designed for certain experiments to meet the high data processing and latency demands [1, 22, 29].

Recently, first commercial products appeared on the market specifically targeting the quantum computing sector for superconducting qubits. Noteworthy products are the OPX of Quantum Machines [27], the Quantum Computing Control System (QCCS) of Zurich Instruments [34], and the Quantum Engineering Toolkit (QET) of Keysight [15]. All offer the sequencing, generation and detection of base-band microwave pulses. The technical realization, however, differs among the different products.

Keysight’s QET comprises a modular system in a PXIe chassis with components to generate microwave signals, components to digitize and process microwave pulses, and components to realize the control of the other components. The AWG components each offer four 14-bit channel outputs with 1 GSPS or 16 bit outputs with 500 MSPS. The digitizer com-
ponents offer up to eight 14 bit input channels with 100 MSPS or four 14 bit channel with 500 MSPS. The modules are based on FPGAs of the Xilinx Kintex-7 series.

Similarly, Zurich Instruments’ QCCS builds on a combination of their HDAWG devices for manipulation pulse generation and a separate device to generate and process readout pulses, the UHFQA Quantum Analyzer. The HDAWG offers up to eight 16 bit channels with 2.4 GSPS. The UHFQA has a 14 bit dual-channel AWG and a 12 bit dual-channel input, both operating at 1.8 GSPS. They offer frequency-division multiplexing for up to ten qubit readout frequencies. In contrast to Keysight’s product, these are fully operational standalone devices. Multi-device synchronization is achieved by an additional device, the Programmable Quantum System Controller (PQSC). There, they use a Xilinx UltraScale+ XCZU15EG-2I FPGA [34] with heterogeneous MPSoC that can be customized by the user. It is not publicly known if the real-time processor is used and if a similar FPGA is present within UHFQA and HDAWG.

Quantum Machine’s OPX integrates pulse generation and qubit readout in a single device. It offers ten analog output channels and two analog input channels. To the best of our knowledge, it does not utilize a heterogeneous MPSoC processing system.

Besides the different quantum readout systems, there are theoretical concepts to describe future quantum computers with a higher level of abstraction. A quantum computing stack [4,12,13] describes the necessary layers to translate a high-level description of a quantum algorithm into physical operations on a quantum processor. The aforementioned hardware platforms provide the lowest layer above the quantum chip itself and act as quantum-classical interface. If their classical computation capabilities permit, they can also be utilized to implement a simple quantum computer micro-architecture.

3. PLATFORM ARCHITECTURE

Our electronics platform is based on the heterogeneous architecture provided by Xilinx Zynq UltraScale+ MPSoCs. After first using the ZCU102 evaluation board with externally attached FMC converter cards, we changed our focus to the ZCU111 board. It features the more integrated RFSoC comprising gigasample A/D and D/A converters directly integrated within the system-on-chip (SoC). An overview of our design architecture is visible in Fig. 1. To generate and digitize microwave pulses, we employ the integrated A/D and D/A converters operating at 4 GSPS and utilize decimation and interpolation filters to obtain a per-channel data rate of 1 GSPS within the FPGA. This allows the platform to handle base-band signals up to the Nyquist frequency of $f_s/2 = 500$ MHz. A separate RF electronics containing mixers and microwave sources is necessary to translate these base-band signals to and from the band-pass signal in the desired gigahertz frequency range of the superconducting circuits.

On the FPGA, different modules are implemented. Fig. 1 shows the modules needed to interact with a single qubit. Two pulse generators supply the DACs with samples containing digital pulses. Frequency, phase, and shape of these pulses can be defined during the experiment. One generator is used for manipulating the qubit state, the other to generate readout pulses. A recording module processes the experiment response from these pulses by performing a digital down-conversion of the signal obtained from the ADC. It also applies further filtering and processing to average over measurements and extract the state of the qubit. Both pulse generators and the recording module are triggered by a sequencer that enables the user to schedule pulses in 4 ns steps, as well as to start processing of incoming pulses. The recording module also reports the determined qubit states back to the sequencer which can then perform sequences conditioned on the outcome of a previous measurement. All modules are supplied by a single clock domain rigidly coupled to the converter clock. This guarantees highest reproducibility between multiple experiment repetitions.

All modules are addressable by a register-based AXI4Lite bus and mapped into the physical memory address range of the processing system. Therefore, RPU and APU can read out status and data from these modules, as well as configure them, by simple memory read and write operations. They also share a common external DDR4 memory which can be used to exchange data between both processors.

The APU hosts a Linux operating system on which programs are implemented to initialize the platform at boot time, provide means to communicate with external clients via Ethernet, as well as to perform further data post-processing online. We wrote a modular communication server running on the APU with services for all of our components. This includes FPGA components like the pulse generators, the sequencer and the recording module, but also more abstract components like the Taskrunner. The communication protocol is based on

![Architecture of our heterogeneous electronics platform.](image-url)
remote procedure calls (RPC) and employs the open source framework gRPC [9]. Thereby, it is possible to connect to the platform with any client written in a language that is supported by gRPC. As Python is widely used within the experimental physics community, this was our choice for the primary client.

4. TASKRUNNER FRAMEWORK

As detailed in Section 2.1, performing computational tasks and experiments with superconducting qubits requires the execution of a well-defined sequence of pulses and measurements. Typically, delays and pulse properties need to be adapted between individual executions to sweep a specified parameter range. Executions with fixed properties are directly handled by the sequencer within the FPGA for highest reproducibility with nanosecond precision. However, performing complex sequences and varying parameters between individual ones is impractical to implement in hardware. Implementing these variations in the Python client is easily possible but yields a high latency due to the communication overhead.

The main goal of our Taskrunner framework is to address this issue by utilizing the real-time co-processor (RPU) on the heterogeneous Zynq UltraScale+ architecture. This renders complex control schemes with deterministic timing and low latency possible without having to adapt the FPGA. The Taskrunner framework enables the user to execute arbitrary code, so-called user tasks, at run-time. Tasks can be transmitted in binary format or as source code. In the latter case, the source code will be compiled on the fly by a cross-compiler on the RPU and afterwards sent to the Taskrunner. The new task replaces a possibly pre-existing user task and can be started and stopped by the gRPC control service.

4.1 Architecture

The structure of the Taskrunner framework is depicted in Fig. 2. It comprises the APU and RPU, as well as the communication between both processors and the communication to an external client via Ethernet.

4.1.1 Real-time co-processor

On the RPU, our Taskrunner software is hosted by the real-time operating system FreeRTOS. It handles communication with the APU and controls the task execution and is loaded together with FreeRTOS upon initialization from the APU.

The Taskrunner consists of two threads that are scheduled by the FreeRTOS scheduler. One handles the communication with the control service on the APU. It is only scheduled when the control service is requesting information from or sending data to the Taskrunner. The other thread implements the execution of the user task, in the following called application thread. Unwanted context switches between both threads that would break deterministic execution in relevant sections of the user task can be inhibited by defining a critical section using the Taskrunner interface (see Section 4.5).

4.1.2 Application processor

Most of the functionality provided by the Taskrunner is directly wrapped by the control service on the APU and exposed to the user. The functionality also includes loading of new tasks during run-time which, if transmitted as source code, will first be compiled on the fly by a cross-compiler on the APU and afterwards sent to the Taskrunner. There, the new task replaces a possibly pre-existing user task and can be started and stopped by the gRPC control service.

4.1.3 Inter-processor communication

The connection between RPU and APU employs the shared DDR4 memory, as well as the Linux remoteproc framework and the RPMMsg messaging protocol [24]. On the RPU, the implementation is provided by the Open Asymmetric Multi Processing (OpenAMP) [25] framework. In our configuration, the APU acts as host, controlling the RPU slave via remoteproc. The communication between the Taskrunner on the RPU and the control service on the APU is handled by the RPMMsg protocol. RPMMsg is based on inter-processor interrupts and a shared memory (compare Fig. 1). The communication thread on the RPU is notified by an interrupt whenever a message is available. In the other direction, the control server on the APU is currently only polling status information on request.

Building on the RPMMsg protocol, the user payload is further structured. After a header to indicate message type and packet number with 1 byte each, the type-specific packet data follows. We implemented the following packet types: acknowledged, not acknowledged, status request, control operation like starting and stopping a user task, update parameter list size, obtain error messages in queue, get finished data boxes, mark data boxes as processed, set the Taskrunner firmware hash, as well as packets to transfer the user task and to init and close the connection.

4.2 Initialization

During boot of the Linux on the APU host, an init script initializes the RPU. It first ensures that the RPU is stopped. Then it copies the Taskrunner binary including FreeRTOS as firmware onto the RPU. Both Taskrunner firmware and user task are located inside the tightly-coupled memory (TCM) banks of the Zynq UltraScale+ series [33, p. 80 f.]. This ensures a low-latent, deterministic access and thus execution
```c
#include "task.h"
#include "recmodule.h"
#include "sequencer.h"

int task_entry()
{
    uint32_t *param_list = rtos_GetParameters();
    uint32_t param_count = rtos_GetParametersSize() / sizeof(uint32_t);
    if (param_count != 2)
    {
        rtos_PrintfError("Please provide exactly 2 parameters (%d given).", param_count);
        return -1;
    }
    uint32_t repetitions = param_list[0];
    uint32_t start_pc = param_list[1];
    iq_pair *data_iq = rtos_GetDataBox(repetitions * sizeof(iq_pair));
    // Ensure sequencer is ready for current task
    sequencer_wait_while_busy();
    for (uint32_t i = 0; i < repetitions; i++)
    {
        sequencer_wait_until_qubit_relaxed();
        sequencer_start_at(start_pc);
        // Wait until result available
        sequencer_wait_while_busy();
        recmodule_wait_while_busy();
        recmodule_get_iq_pair(0, data_iq + i);
        rtos_SetProgress(i + 1);
    }
    rtos_FinishDataBox(data_iq);
    return 0;
}
```

Listing 1: Basic user task showcasing how to implement a control flow with the Taskrunner framework. This task will perform a certain number of repetitions as defined in the parameter list and store every single in-phase and quadrature result in a data box. The obtained data can be used to generate a histogram as shown in Fig. 3.

of operations. The TCM banks are operated in lock-step mode, giving access to the full 256 kB memory capacity. To maximize performance, text sections are located inside the first TCM (ATCM) and data sections inside the second one (BTCM) [33, p. 89]. For the user task, a 50 kB region is reserved in both ATCM and BTCM. The remaining space is utilized by the firmware itself, which is occupying 123 kB of memory.

At the end, the RPU is started and it is checked that everything is running. If so, a Linux kernel module handling the communication with the RPU is loaded. Finally, a MD5 hash of the Taskrunner firmware is sent to the Taskrunner which can later be queried in order to verify that pre-compiled user tasks are linked against the correct Taskrunner version. Afterwards, the gRPC server is started and the control service initialized. The service establishes the RPMsg connection to the Taskrunner and queries the memory regions for data and parameter transfer.

### 4.3 User Task Programming

The user task is conveniently written in the C language. Thereby, a broad feature set of the C language and existing libraries can be utilized. A basic task triggering pulse sequences and collecting measurement results is shown in Listing 1. The entry function of the user task is called `task_entry()` and has no parameters. All interaction with the Taskrunner is handled by separate interface functions (see Section 4.5).

The source code is transmitted to the control service on the APU via the gRPC interface. There, a cross-compiler for the RPU is invoked. In our case, this is the bare-metal compiler of the GCC (arm-none-eabi). We also provide multiple C libraries to abstract from a pure register-based access when interacting with modules on the FPGA. This e.g. includes functions like `sequencer_wait_while_busy()`. They are already present on the platform and will be taken into account when the source file is compiled. Furthermore, in order to interact with the Taskrunner and provide standard libraries, the user task is also linked against the RPU firmware binary. It is noteworthy that the compilation is performed with the optimization flags `-O2 -mcpu=cortex-r5 -funroll-loops` which substantially speeds up the task execution. After compilation, the binary is stripped using the objcopy method of the compiler removing unused sections in the binary. A custom linker script, ensures that the entry function is at the beginning of the resulting binary file and the function symbol addresses are matched to the running FreeRTOS.

Finally, meta information is added to the end of the binary file, in particular a configurable name for the task as well as the MD5 hash of the RPU firmware binary. The latter is to guarantee compatibility in case the binary is kept and reused later. It will be checked by the logic loading the user task and results in a rejection if it does not match the running version. If an error occurs during the compilation process, the output streams of the compiler will be returned to the user. The user can also load a pre-compiled task via the gRPC interface which will then skip the compilation step. In both cases, the MD5 hash of the task and the running RPU firmware is compared to ensure compatibility before the binary is loaded onto the RPU using the RPMsg interface.

On the RPU, the communication thread will store the task in the TCM. Both the communication and the application thread of the Taskrunner use a mutex to guarantee that there is no conflicting access to the user task memory region. Direct access from the APU to the TCM is not intended. After loading the user task, the status flags are updated accordingly.

### 4.4 User Task Execution

Prior to starting the task execution, parameter values can be passed to the user task. Examples are a list of delays, the number of average repetitions to perform, or boolean information like if a separate calibration step should be included in the execution. The parameter list will be transferred via gRPC to the APU and copied into the respective region in the DRAM by the control service. In our implementation, the region currently offers 15 MB of space for parameter values. The control service also notifies the Taskrunner that the pa-
The parameter list has been updated and reports the new size of the list. This information can later be queried by the user task to know the valid parameter range inside the DRAM memory region. As the DRAM access is subject to fluctuations in execution time, the on-chip memory (OCM) [33, p. 35] could potentially also be used. With its size of 256 kB it should be still sufficient for most applications.

When the user starts the task execution, the command will be relayed via gRPC and RPMsg to the Taskrunner. The communication thread of the Taskrunner will ensure that no task is currently running and raise an error if it is the case. Then it will notify the application thread about the received start command. The application thread will try to lock the mutex of the user task memory region. It then verifies that a user task was loaded and a start command issued. Before starting the task, it invalidates the DRAM cache of the region where the parameter values are located. This is especially important if the values changed since the last execution to avoid obtaining outdated parameter values.

It then casts the address of the task memory region into a function pointer and calls the entry function of the user task in the context of the application thread. After the execution finished, the mutex is released again. Before and after the function call, also the status flags are updated accordingly so the communication thread reports the correct status of the Taskrunner.

### 4.5 Taskrunner Interface

The user task can utilize a provided function library to interact with the Taskrunner. The functions are part of the RPU firmware binary and will be linked against during compilation. A list of all available functions is given in Listing 2. This includes a print function to output text to the UART interface for debugging purposes and functions wrapping FreeRTOS functionality like defining critical sections and resetting and reading out the PMCCNTR counter for timing benchmarks. Error messages can be specified and will be appended to a queue that can be fetched by the control service on the APU. The Taskrunner also provides a function to query the parameter list that can be used to customize the task’s behaviour. One function allows the user task to specify a uint32_t progress value that can be polled by the user during execution to monitor the task progress. Finally, functions to operate with data boxes (see next section) are provided to exchange data with the user.

```c
void rtos_Printf(const char *format, ...);
void rtos_EnterCriticalSection(void);
void rtos_ExitCriticalSection(void);
void rtos_RestartTimer(void);
uint32_t rtos_GetCycleCountTimer(void);
uint32_t rtos_GetNsTimer(void);
void rtos_ReportError(const char *error_msg);
void rtos_PrintfError(const char *format, ...);
void *rtos_GetParameters(void);
uint32_t rtos_GetParametersSize(void);
uint32_t rtos_SetProgress(uint32_t progress);
void *rtos.GetDataBox(uint32_t size);
void rtos_FinishDataBox(void* databox);
void rtos_DiscardDataBox(void* databox);
```

Listing 2: A list of all functions available for the Taskrunner interface.

### 4.6 Data Transfer

Typical user tasks in experiments with superconducting qubits perform data collection, aggregation or post-processing. Therefore, the Taskrunner provides an interface to exchange collected data with the APU and the user. In our implementation, we employ so-called data boxes to store obtained or processed values from the user task. We define a 480 MB heap located in the DDR4 memory with custom functions to request, finish and discard data boxes of an individually settable size (see last section).

Finished data boxes of a running or completed user task can be requested by the user. The control service then fetches a list of the corresponding DDR4 memory addresses and sizes from the Taskrunner. After sending the data boxes to the user, the corresponding memory regions are freed and can be reused again. When discarding an acquired data box the allocated memory region is also freed. In this case no data is sent to the APU and user. Data boxes from a previous task execution which have not been discarded or fetched will be freed when a new task starts.

When transferring data between Taskrunner and user, two different operation schemes can be distinguished. For shorter experiments it is sufficient to collect the data when the user task completed. The data boxes are finished at the end of the user task and the Python driver checks if the task is done prior to fetching the data boxes. During task execution, only the progress value is exchanged between Taskrunner and client.

Longer experiments, on the contrary, might exceed data sizes that can be handled by the heap on the RPU. Furthermore, fast feedback by delivering first data to the user is beneficial as they might already judge from this if the task should continue or if some experimental parameters need to be adapted. Therefore, data boxes can also be finished during the user task execution and collected in parallel by the user. Afterwards, the memory is freed again on the RPU which solves the first issue. It also provides the means to directly visualize the evolving measurement results while the experiment progresses.

## 5. PERFORMANCE VALIDATION

In order to verify operation of the system, the following section presents characteristic timing benchmarks and elaborates on means for improvement. It also shows selected experimental applications and results to showcase operation scenarios in superconducting qubit experiments.

### 5.1 Timing benchmarks

During execution of the user task in the Taskrunner, each communication request causes a context switch between the two FreeRTOS threads and thus an interruption of the user task. Depending on the complexity of the request, the interruption can be shorter or longer. Requesting the Taskrunner status and obtaining the newest progress value, for example, causes an interruption of 16.2 µs. Querying error messages when none are present leads to a 14.3 µs interruption. Asking for available finished data boxes takes longer and causes an interruption of 42.7 µs. Therefore, it is advisable to query the task status not too often in order to not significantly slow down the user task execution. In our Python client, we typically wait 200 ms before checking again if the user task com-
Table 1: Comparison of timing performance for typical operations running within the Taskrunner and within the Python client. The AXI register memcpy was benchmarked with 1024 register values copied into the TCM. The array multiplication was performed with two 32 bit arrays, each with 1024 elements, also located in the TCM.

| Operation              | Taskrunner | Python client |
|------------------------|------------|---------------|
| AXI register read      | (306 ± 2) ns | (590 ± 40) µs |
| AXI register write     | (323 ± 2) ns | (620 ± 40) µs |
| Sequencer status poll  | (324 ± 2) ns | (580 ± 60) µs |
| AXI reg. memcpy        | (312401 ± 4) ns | (1500 ± 130) µs |
| Array multiplication   | 10270 ns    | (1.5 ± 0.8) µs |

Table 2: Durations to load different tasks onto the Taskrunner from the Python client. Three tasks are distinguished based on their complexity which is also reflected in the number of source code lines.

| Task     | Lines | Source code | Binary file |
|----------|-------|-------------|-------------|
| Empty    | 6     | (184.8 ± 0.5) ms | (1.25 ± 0.09) ms |
| Basic    | 39    | (260.3 ± 0.6) ms | (1.55 ± 0.10) ms |
| Complex  | 386   | (1107.2 ± 1.8) ms | (2.99 ± 0.10) ms |

Complexity of the task. While the empty and basic task both only consist of the entry function, the complex task also implements multiple separate functions to perform calculations like an FFT.

Finally, the speed to transfer data boxes to the Python client is an important benchmark. Requesting and transferring 10 KB data as int32_t values takes (4.3 ± 1.6) ms. With increasing data box size, the overhead decreases and thus the transfer speed increases. Transferring a 100 MB data box requires (2.32 ± 0.16) s corresponding to 43 MB s⁻¹.

5.2 Experimental applications

In the field of quantum computing, many applications exist where a low response time is critical but prototyping an FPGA design is unfeasible. While not being discussed in this paper, this can also comprise tasks like prototyping complex quantum error correction schemes or realizing part of a quantum processor micro-architecture. As these concepts are still at an early stage, in the following, we will instead focus on three fundamental use-cases in research with superconducting qubits.

5.2.1 Fast parameter changes

As outlined in Section 2.1, it is important to first change parameter values before averaging in order to avoid low frequency noise. For operation without the Taskrunner, this requires frequent communication between the FPGA and our external Python client. Let us assume a standard experiment with 42 parameter changes, a qubit relaxation delay of 100 µs and 10000 repetitions. This would roughly take 24h due to the significant communication overhead after each pulse sequence. In contrast, when first averaging on the sequencer and then changing the parameters using Python, this example experiment takes 51s but becomes susceptible to low frequency noise.

At the same time, an identical experiment can be easily implemented using the Taskrunner framework and executed in only 43s. In this case, a user task performs the necessary parameter changes, collects single measurement results and only afterwards averages them separately for each parameter configuration. This solves both the overhead issue and the susceptibility to slow fluctuating noise. The major contribution in both cases is the qubit relaxation delay corresponding to 10000 × 42 × 100 µs = 42 s. The difference is that, when executed by the Taskrunner, there is nearly no overhead left due to the low-latent interface towards the FPGA.

5.2.2 Single measurement statistics

Another important aspect is the necessity to perform further statistics of single measurements. Due to the latency, the Python client is clearly not suited to perform evaluations based on single measurements. The Taskrunner, on the other hand, can collect and aggregate single measurement results online and send the collected data independent of the FPGA execution to the user. This renders experiments like generating a histogram from one million single qubit measurements possible. The in-phase and quadrature response of the system can be visualized, corresponding to roughly 8 MB of collected data. An exemplary measurement result from our platform is shown in Fig. 3. Despite the noise, one can clearly
where the signals with the probability to end up in different states. For this component. The FPGA already reduced the ADC data rate to the convolution theorem implementation on the Taskrunner also allows us to exploit processing would take place outside of the platform. The tween single recordings but is still much faster than if the real-time processor leads to an increased dead-time being task which is typically implemented on the FPGA. In order to stay flexible for a variety of different experiments, we perform this calculation and averaging on the Taskrunner. This allows the user to quickly implement and adapt the experiment script to its needs without requiring knowledge in FPGA design. On the downside, the implementation on the real-time processor leads to an increased dead-time between single recordings but is still much faster than if the processing would take place outside of the platform. The implementation on the Taskrunner also allows us to exploit the convolution theorem $F\{f(t) * r(t)\} = F(f) \cdot R(f)$ and employ a fast Fourier transform (FFT) to speed up the calculation and further reduce the measurement dead-time.

As an example, let us assume a $g_2$ correlation measurement with 1024 samples for each $S_i$. Each sample consists out of two 16 bit values for the in-phase and quadrature components. The FPGA already reduced the ADC data rate to one value pair every 100 ns. This means that a measurement on the FPGA takes $1024 \times 100 \text{ns} = 102.4 \mu s$. Afterwards, the $g_2$ calculation is performed on the Taskrunner. To obtain sufficient statistics, we perform 100 000 averages. Without the FFT, it takes 1810 s to calculate and average $g_2(t)$ for the first 11 values of $t$, i.e. $t \in \{0, 100 \text{ns}, \ldots, 1000 \text{ns}\}$. The same experiment with FFT, in contrast, gives the full $g_2(t)$ with all 1024 possible $t$ values after only 169 s.

Still, the calculation overhead is dominant as the measurement time of 102.4 $\mu s$ per iteration and average is an order of magnitude smaller than the calculation time of 1.31 ns. This time is currently dominated by the FFT (530 $\mu s$) and the process of copying the signal data from the recording modules (627 $\mu s$). As the AXI4Lite register read access is a bottleneck here, other data transfer methods like direct memory access (DMA), the possibility of burst reads, and the utilization of a separate AXI interface better suited for the RPU will be addressed in our future work.

5.2.3 Calculation of correlation functions

Also more sophisticated scenarios render possible with the heterogeneous architecture. An example is the calculation of the second order correlation function $g_2$:

$$g_2(t) \approx \frac{1}{N} \sum_{i=1}^{N} S_{1,i}(t)S_{1,i}(t+\tau)S_{2,i}(t+\tau)S_{2,i}(t)\,d\tau \tag{1}$$

where the signals $S_1$ and $S_2$ of two signal paths are recorded and correlated. As the sum does not commute with the multiplication, single signals need to be processed and multiplied prior to the averaging taking place. This results in a demanding task which is typically implemented on the FPGA. In order to stay flexible for a variety of different experiments, we perform this calculation and averaging on the Taskrunner. This allows the user to quickly implement and adapt the experiment script to its needs without requiring knowledge in FPGA design. On the downside, the implementation on the real-time processor leads to an increased dead-time between single recordings but is still much faster than if the processing would take place outside of the platform. The implementation on the Taskrunner also allows us to exploit the convolution theorem $F\{f(t) * r(t)\} = F(f) \cdot R(f)$ and employ a fast Fourier transform (FFT) to speed up the calculation and further reduce the measurement dead-time.

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Figure 3: Histogram showing the in-phase and quadrature response $I$ and $Q$ of one million measurements of a physical Transmon qubit. Please be aware that the color scale is logarithmic. The data is collected by the user task shown in Listing 1.

6. CONCLUSION

We presented our Taskrunner framework for applications in quantum computing. It combines a real-time co-processor (RPU) and an application processor (APU) to provide low-latent access to the FPGA logic. Thereby, we leverage fast parallel processing on the FPGA with the flexibility of a software-based approach. Due to the usage of the C language, complex functionality and control sequences can be implemented and rapidly tested, with no FPGA design knowledge and testing required. The integration of the compiler on the APU furthermore leads to less dependencies for the user and enables on-the-fly compilation.

The Taskrunner framework has been characterized by timing benchmarks. We verified deterministic execution behavior and low-latent AXI register access to the FPGA logic on the order of 300 $\mu s$. This is three orders of magnitude faster than if the access to the FPGA logic accessed by an external control computer. We also motivated different experimental applications that are already utilized in research with superconducting qubits.

Improvements will further reduce the latency, extend the handling of experimental tasks and add automatic calibration features for superconducting qubit experiments.

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