New structure for an all-optical logic gate based on hybrid plasmonic square-shaped nanoring resonators and strips

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Abstract
Seven all-optical logic gates based on hybrid plasmonic squared-shaped nanoring resonators and strips are proposed, designed, and numerically analyzed using finite element method with COMSOL software package version 5.5. Constructive and destructive interferences between the input port(s) and the control port(s) are the main operating principles used to produce the proposed gates. The ratio of output optical power to the input power at a single port which is called the transmission threshold is selected to be 30% and the resonance wavelength is 1310 nm. All the hybrid plasmonic logic gates are performed in a single structure of 400 nm × 400 nm dimensions and the performance is measured according to the values of transmission at the output port versus a wavelength range from 800 to 2000 nm, contrast ratio, modulation depth, and insertion loss. The transmission exceeds 100% in five gates, 146% at NOT and NAND gates, 202.3% at OR, AND, and XNOR gates. The modulation depth scores are 99.75% at the XNOR gate, 98.5% at the NOR gate, 97.67% at OR, AND, NOT, and NAND gates, and 95.29% for the XOR gate.

Keywords Hybrid plasmonic waveguides · All-optical logic gates · Square-shaped nanoring resonators and strips

1 Introduction
Surface waves that are generated at the interface between a metal and a dielectric are known as surface plasmon polariton (SPP) (Barnes et al. 2003). They have a great view of interest for many reasons such as they break the limit of diffraction for the light wave in the waveguides, so by using SPP the light wave can flow in guides with dimensions smaller than or equal one-half the operating wavelength and the size of the devices can be reduced significantly (Maier 2006). SPP has many applications like biosensing (Homola 2003) and electronic circuits implementation (Liu et al. 2011; Pan et al. 2013; Wang et al. 2013; Bian and Gong 2014; Ooi et al. 2014; Maksymov 2011). The biggest challenge for the SPP is the propagation loss or propagation length, SPP can propagate only for a few distances
before the supporting power is decayed to a noticeable level, many efforts have been done
to make a trade-off between the propagation loss and the wave confinement so there are
new structures of waveguide appears such as nanoparticle waveguides (Maier et al. 2002),
channel waveguides (Lee et al. 2007) metal–insulator–metal (Gong et al. 2009), metal slot
(Guo et al. 2018), insulator–metal–insulator (Abdulnabi and Abbas 2019).

The pros and cons of the plasmonic waveguides (PW) and the dielectric waveguides
(DW) can be seen as one complete the other (Alwahib et al. 2021, 2020, 2213), for exam-
ple, DW can be regarded as lossless guides but there is a problem in the mode size, on
the other side PW can permit the light to flow under the diffraction limits but there is a
problem of high propagation loss. A great deal between confinement and propagation loss
can be achieved by using Hybrid Plasmonic Waveguide HPWG (Oulton et al. 2008), where
plasmon and dielectric guiding leads the guiding mechanism (Dai and He 2009; Fujii et al.
2009). As shown in Fig. 1 Alam et al. (2013), the low index medium (dielectric) separated
the metal layer from the high index medium (semiconductor), whereas d, is the height of
the dielectric layer 1, h and w is the Hight and width of the semiconductor layer 2 respec-
tively, the effect of changing these dimensions on the HPWG performance was illustrated
in Table 1. Transverse electric (TE) and transverse magnetic (TM) modes can support the
hybrid plasmonic waveguides, but SPP waveguides support only TM mode (Alam et al.
2007), so in this paper we take only TM modes into account. The method used to analyze
the hybrid plasmonic waveguide modes is known as the transfer matrix method (Breuke-
laar 2004), it offers prices and accurate solutions for these modes. Recently, several hybrid
plasmonic all-optical logic gates with various structures, resonance frequencies, materials,
and amount of transmission have been established (Maksymov 2011; Cui and Yu 2018;
Sharma and Kumar 2018; Peng et al. 2013a; Wang et al. 2016).

In this paper, the full number of hybrids plasmonic logic gates (seven gates) have
been designed, analyzed, and simulate for the same structure, resonance frequency, and

![Diagram of Hybrid Plasmonic Waveguide (HPWG)]
transmission threshold using square shaped nanoring resonators and strips made of [AlN-Al₂O₃ (Aluminum oxynitride, ALON)] which has a high hardness and good optical transparency in the wavelength range of 0.2–5.2 μm properties (Bandyopadhyay et al. 2002), by using the finite element method (FEM). Hybrid plasmonic waveguides (HPWGs) are the solution when PWs and DWs are combined (Alam 2012).

The organization of this paper is as follows: Sect. 2, demonstrates the theoretical principles and the system layout. In Sect. 3, the design of the proposed hybrid plasmonic logic gates are presented. In Sect. 4, a comparison between this paper and previous works has been accomplished and finally, the conclusion about the work and the results has been done in Sect. 5.

2 Mathematical description and system setup

Generally, the hybrid plasmonic waveguides it’s a multilayer system, in our design the system is consisted of silver (ε_Ag) as conducting metal, Teflon (ε_Teflon) for the dielectric layer, and Aluminum oxynitride, ALON (ε_ALON) as a high index medium, for theoretical analysis let us assume the structure in Fig. 1 with the materials we mentioned for propagation in the Z direction, the magnetic field for layers q = 1 and q = 2 is as follow Alam et al. (2013):

$$\vec{H}_q(y,z) = H_{xq}(y) \exp (j(\beta z - wt)) \hat{x}$$ (1)

where β is the complex propagation constant and equal to $k_0 (n_{eff} + j k_{eff})$, $k_0$ is the free space wavenumber and equal to $(2\pi/\lambda_0)$, $\lambda_0$ is the free space wavelength and $n_{eff}, k_{eff}$ its real and imaginary parts of the effective refractive index, the magnetic field for cover layer (Teflon) and base (Silver) layer are Alam et al. (2013):

$$\vec{H}_{cover}(y,z) = A_c \exp (-k_c(y-(d+h))) \exp (j(\beta z - wt)) \hat{x}$$ (2)

$$\vec{H}_{base}(y,z) = A_s \exp (k_b y) \exp (j(\beta z - wt)) \hat{x}$$ (3)

where $k_b$ and $k_c$ are the attenuation rate for base and cover and equal to:

$$K_{base} = \sqrt{\beta^2 - \varepsilon_{Ag} k_o^2}$$ (4)

$$K_{cover} = \sqrt{\beta^2 - \varepsilon_{Teflon} k_o^2}$$ (5)

Now, the dispersion relation for the HG in Fig. 1 with its layers is:

$$(k_{base}/\varepsilon_{Ag})m_{11} + (k_{cover}/\varepsilon_{Teflon})m_{22} - m_{21} - (k_{base}k_{cover}/\varepsilon_{Ag}\varepsilon_{Teflon})m_{12} = 0$$ (6)

where m equal to Alam et al. (2013):

$$\begin{bmatrix} m_{11} & m_{12} \\ m_{21} & m_{22} \end{bmatrix} = \begin{bmatrix} \cos(k_1d) & -\varepsilon_{Teflon} k_1 \sin(k_1d) \\ k_1 \sin(k_1d) & \cos(k_1d) \end{bmatrix} \times \begin{bmatrix} \cos(k_2h) & -\varepsilon_{ALON} k_2 \sin(k_2h) \\ k_2 \sin(k_2h) & \cos(k_2h) \end{bmatrix}. \quad (7)$$

here, $k_q$ is the transverse wave number for the qth layers (q = 1, 2) and is given by:
The suggested configuration to achieve all-optical logic gates by using HPWG is illustrated in Fig. 2, it consists of three strips and three rectangular for Silver, two square-shaped ring resonators, and two strips for the ALON material and residual for Teflon with dimensions depicted in Fig. 3 all in (nm).

As seen in Fig. 2, the total number of ports is four, an output port, input(s) port(s), and control(s) port(s), these ports have been distinguished according to the requirement of the hybrid plasmonic logic gate. By launching TM-polarized plane wave for the input(s) port(s) and control(s) port(s) surface waves are excited. Johnson and Christy (1972) data are handled to illustrate silver permittivity, Hartnett et al. (1997) data for the Aluminum oxynitride permittivity and the refractive index for Teflon material are 1.375 (French et al. 2009), the resonance condition for the square-shaped ring resonators calculated concerning (Peng et al. 2013b).

\[
k_1 = \sqrt{\varepsilon_{\text{Teflon}} k_0^2 - \beta^2}
\]

(8)

\[
k_2 = \sqrt{\varepsilon_{\text{ALON}} k_0^2 - \beta^2}
\]

(9)

where \( L \) is the total length of the square, \( m \) is the mode number and it’s an integer, \( N_{\text{eff}} \) is the total refractive index and \( \lambda_{\text{resonance}} \) is the resonance wavelength. The type of the materials and the structure dimensions are two important factors for selecting the resonance

Fig. 2 The proposed HPWG structure

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wavelength of the system, our system is operating at 1310 nm, it’s an important window for optical communication systems. Two-dimension Finite Element Method (2-D FEM) is used to make a numerical solution to the Maxwell equations, for the boundary condition of the aperture under calculations the convolutional perfectly matched layer (CPML) has been used.

To evaluate the performance of the seven all-optical logic gates four criteria had been used, the first is the ratio of output optical power to the input power at a single port (input or control port) which is called the transmission threshold versus wavelength, the value of the transmission threshold to distinguish between two states (logic 1 and logic 0) ON and OFF-state is selected to be 0.3 to achieve the seven logic gates in the same structure (Freeman and Moisen 2008). The second is the ratio of the minimum optical power for the ON state to the maximum optical power for the OFF state (extinction or contrast ratio) as depicted in Table 2, the fulfilment of the plasmonic gates would be better whenever the

| Contrast ratio (dB) | Description | Performance               |
|---------------------|-------------|---------------------------|
| Negative value      | Low         | Poor and inefficient      |
| Below than or equal 4 dB | Low     | Accepted                  |
| Greater than 4–8 dB  | Medium      | Moderate                  |
| Greater than 8–12 dB | Medium      | Good and efficient        |
| Greater than 12–16 dB | High      | Very good and efficient   |
| Greater than 16–20 dB | High       | Excellent and efficient   |
| Greater than 20 dB   | Very high   | Excellent and very efficient |
variance between this optical power is large. These two criteria are described by Eq. (11) Lin and Huang (2008) and Eq. (12) Dolatabady and Granpayeh (2017), respectively.

\[ T_{\text{threshold}} = \frac{\text{Output power}}{\text{Input power}} \]  

where \( T_{\text{threshold}} \) is the transmission threshold. Output power, is the output optical power of the output port in logic 1 state and logic 0 state. Input power, is the input optical power for single input port or single control port.

\[ \text{Contrast ratio} = 10 \times \log \left( \frac{P_{\text{out}|\text{ON}}}{P_{\text{out}|\text{OFF}}} \right) \text{ max} \]  

where \( P_{\text{out}|\text{OFF}} \) is the maximum output power of the output port for logic 0 state and \( P_{\text{out}|\text{ON}} \) is the minimum output power of the output port for logic 1 state.

The third criteria and at the same time the answer to the question, is the dimension of the suggested structure give the best result? As shown in Table 3 it’s called the modulation depth (MD) and it’s given by Yarahmadi et al. (2015); Rezaei et al. (2019):

\[ \text{MD} = (T_{\text{ON max}} - T_{\text{OFF min}})/T_{\text{ON max}} \]  

where \( T_{\text{ON max}} \) is the maximum transmission in the case of ON state and \( T_{\text{OFF min}} \) is the minimum transmission in the OFF state.

The fourth criteria are insertion loss (IL) in dB which is defined as the loss in signal power from the input port to the minimum transmission of the output port in the case of ON state and is illustrated by Johnson and Christy (1972):

\[ \text{IL} = 10 \times \log \left( \frac{P_{\text{out}|\text{ON}}}{P_{\text{in}}} \right) \text{ min} \]  

The optical power ratio at the output (Transmission) can be reduced or raised depending on two important factors (Christopoulos et al. 2016; Mossayebi et al. 2016), one of them is the port position the other is the polarization of the incoming field and its phase, on the other hand, the logic gates performance is calculated based on the fundamental of enhancement and destroying interferences between the input light signal(s) and control light signal(s) according to Alwahib et al. (2020), Alam et al. (2013), it is depending strongly as we mentioned on the port position and the phase of the incident field when the other parameters (size, shape, material, and dimensions of the configuration remain unchanged).

| Table 3 | Illustration for the values of the modulation depth Abdulnabi and Abbas (2022) |
|---------|---------------------------------------------------------------|
| Modulation depth | Description | Optimality in dimension |
| Below than 10% | Low | Poor and inefficient |
| 10% to < 20% | Low | Accepted |
| 20% to < 40% | Medium | Moderate |
| 40% to < 60% | Medium | Good and efficient |
| 60% to < 80% | High | Very good and efficient |
| 80% to < 90% | High | Excellent and efficient |
| Greater than 90% | Very high | Excellent and optimum |
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3 Proposed hybrid plasmonic logic gates

HPWG that used in the structure of Fig. 2 to perform the all-optical logic gate had been hit by a plane wave for the input port(s) in case of ON state and the control port(s) to perform the functionality of the logic gates in the same structure for a wavelength range 800 to 2000 nm. The trial–error method is used to make a good selection for which is the input port(s) and which is the control port(s) to make an optimum transmission.

3.1 Hybrid plasmonic NOT logic gate

A NOT logic gate or the inverter is used to achieve the complement concept, that is means the output of this gate is opposite to its input. To perform the NOT logic gate, port 1 and port 2 are chosen to be control ports, port 3 is the input port, and port 4 is an output port. control ports are continuously illuminated by a light wave with a wavelength of 1310 nm but with different phases according to the cases of inputs, thus when the input port (port 3) is OFF, then the phase of the waves in the control port is chosen to be 0° and that means a constructive interference would happen because the phase difference between the control ports is zero and then the output port (port 4) will be ON, the transmission at this case is 1.46 and it’s above the transmission threshold (0.3) so this is ON state and the complement concept achieved. Now for the case that the input port (port 3) is ON that is mean it’s lighted with 1310 nm wavelength but with a phase of 0°, a destructive interference happened due to a large phase shift between the input port and the control ports (control ports in this situation subjected with a light wave for a phase of 180°) and an OFF state is obtained at the output port (port 4) the transmission, in this case, is 0.034 and it is below the transmission threshold (0.3). The operation of the suggested hybrid plasmonic NOT logic gate is outlined in Tables 4 and 5. The transmission spectrum and the magnetic field (Z component) are shown in Figs. 4 and 5 respectively.

| Inputs | Input port 3 (phase) | Control port 1 (phase) | Control port 2 (phase) | Transmission | Output |
|--------|----------------------|------------------------|------------------------|--------------|--------|
| Logic 0 | OFF (0°)             | ON (0°)                | ON (0°)                | 1.460/0.3    | Logic 1|
| Logic 1 | ON (90°)             | ON (0°)                | ON (180°)              | 0.034/0.3    | Logic 0|

It is the (Transmission threshold value) which is the value that distinguishes between two states (logic 1 and logic 0) ON and OFF-state and it is selected to be 0.3 to achieve the seven logic gates in the same structure.

Table 4 The transmission values for the suggested hybrid NOT gate

Table 5 Computations of the Contrast ratio, modulation depth and insertion loss for the proposed hybrid NOT gate

| Output power (μW) | Contrast ratio | Modulation depth | Insertion loss |
|-------------------|----------------|------------------|----------------|
| \( P_{\text{Min,ON}} \) | 1.460          | 16.32 dB         | 97.67%         |
| \( P_{\text{Max,OFF}} \) | 0.034          |                  | 1.643 dB       |
3.2 Hybrid plasmonic OR, AND, XOR logic gates

These three hybrid plasmonic logic gates shared a common factor in our proposed design, they have the same assignment for the ports. Here, port 1, port 2 are the input ports and port 3 is the control port, for the output port, port 4 is assigned. For the case of the OR gate, the output produces logic 1 whenever there is an ON state in one of the inputs and this can be done without changing the phase difference among the ports as listed in Table 6.

The transmission in the OR gate exceeds 100% (2.023) also in the previous case for (NOT gate), this improvement and amplification is due to the constructive phenomena.
between the input signals and the control signal especially the phase difference between them is (0°).

The contrast ratio for the OR logic gate is good and efficient (Abbas and Abdulnabi 2020), the modulation depth is excellent and optimum (Yarahmadi et al. 2015), because the transmission exceeds 100% and the variance is large (the difference between \(P_{\text{Min}}|_{\text{ON}}\) and \(P_{\text{Max}}|_{\text{OFF}}\)) particularly when the input ports are in ON state. The transmission spectrum and the magnetic field (Z component) are shown in Figs. 4 and 5 respectively.

For the AND logic gate, an output of logic 1 appears only when the two inputs are logic 1, otherwise, the output is logic 0. The difference between this logic gate and the OR gate is in the case of opposite inputs, here in the AND logic gate a phase difference of (180°) between the input ports are set to make a destructive interference and that leads to a transmission value below the threshold (0.3) to achieve the logic 0, while the control port is still in ON state with a phase of (0°). Again, the transmission in the AND gate like the case of NOT and OR logic gates exceed 100% when the two inputs are logic 1 and that gives the structure its recognizable manner (Figs. 6, 7, Table 7).

### Table 6  The transmission values for the suggested hybrid OR gate

| Inputs | Input port 1 (phase) | Input port 2 (phase) | Control port 3 (phase) | Transmission | Output |
|--------|----------------------|----------------------|------------------------|--------------|--------|
| Logic 0 | Logic 0 | OFF (0°) | OFF (0°) | ON (0°) | 0.047/0.3 | Logic 0 |
| Logic 0 | Logic 1 | OFF (0°) | ON (0°) | ON (0°) | 0.620/0.3 | Logic 1 |
| Logic 1 | Logic 0 | ON (0°) | OFF (0°) | ON (0°) | 0.723/0.3 | Logic 1 |
| Logic 1 | Logic 1 | ON (0°) | ON (0°) | ON (0°) | 2.023/0.3 | Logic 1 |

**Fig. 6** The spectrum of the power ratio (transmission) of the suggested hybrid OR gate.
The function of the suggested hybrid plasmonic AND gate is listed in Tables 8 and 9. The transmission spectrum and the magnetic field (Z component) are shown in Figs. 8 and 9 respectively.

In XOR hybrid plasmonic logic gate, logic 1 is recognized when the input ports have a different logic level, logic 0 appears when the input ports have the same logic level, which can be expressed by a circuited plus sign (⊕) between inputs.
In this logic gate, destructive interference when the two inputs are in ON state is achieved by making a phase shift of 90° among the input ports and the control port, unlike the case of the OR logic gate, the maximum transmission has been noticed when the input ports are ON–OFF to be 0.723.

If there is a comparison had been made with the OR logic gate, we see that the contrast ratio is the same because the variance of the OR gate is equal to the variance of the XOR gate, but the modulation depth reduced by about 2.38% due to its dependence on the maximum transmission which is below that of the OR gate by 1.3 dB.

The function of the suggested hybrid XOR gate is listed in Tables 10 and 11. The transmission spectrum and the magnetic field (Z component) are shown in Figs. 10 and 11 respectively.

### 3.3 Hybrid plasmonic NAND, NOR, XNOR logic gates

Unlike the previous hybrid plasmonic logic gates, the arrangement of ports for the NAND, NOR, and XNOR logic gates in our structure as illustrated in Fig. 2, port 1 as input port 1, port 3 as input port 2, port 2 as control port, and port 4 as an output port.
In the NAND gate, a logic 0 is produced only when the input port states are ON-ON otherwise the output is logic 1. That represents a challenge especially in the case when the input ports are OFF-OFF, where logic 1 is produced depending on the control port (port 2). The reason behind selecting port 2 as a control port is that the strip length is sufficient to take effect on the square-shaped ring resonator and make use of the hybrid plasmonic waveguide concept. The point of view for the long propagation length to

![Fig. 9 Allocation of the magnetic field (Z component) of the presented structure for AND gate when input ports is OFF (a), input ports is OFF ON (b), input ports is ON OFF (c) and input ports is ON (d)](image)

| Table 10 | The transmission values for the suggested hybrid XOR gate |
|----------------|----------------------|
| Inputs | Input port 1 (phase) | Input port 2 (phase) | Control port 3 (phase) | Transmission | Output |
| Logic 0 | Logic 0 | OFF (0°) | OFF (0°) | ON (0°) | 0.047/0.3 | Logic 0 |
| Logic 0 | Logic 1 | OFF (0°) | ON (0°) | ON (0°) | 0.620/0.3 | Logic 1 |
| Logic 1 | Logic 0 | ON (0°) | OFF (0°) | ON (0°) | 0.723/0.3 | Logic 1 |
| Logic 1 | Logic 1 | ON (0°) | ON (180°) | ON (90°) | 0.034/0.3 | Logic 0 |

| Table 11 | Computations of the Contrast ratio, modulation depth and insertion loss for the presented hybrid XOR gate |
|----------------|----------------------|
| Output power (μW) | Contrast ratio | Modulation depth | Insertion loss |
| $P_{\text{Min}}$ | $P_{\text{Max}}$ | |
| 0.620 | 0.047 | 11.20 dB | 95.29% | – 2.076 dB |

In the NAND gate, a logic 0 is produced only when the input port states are ON-ON otherwise the output is logic 1. That represents a challenge especially in the case when the input ports are OFF-OFF, where logic 1 is produced depending on the control port (port 2). The reason behind selecting port 2 as a control port is that the strip length is sufficient to take effect on the square-shaped ring resonator and make use of the hybrid plasmonic waveguide concept. The point of view for the long propagation length to
Fig. 10  The spectrum of the power ratio (transmission) of the suggested hybrid XOR gate

Fig. 11  Allocation of the magnetic field (Z component) of the presented structure for XOR gate when input ports is OFF (a), input ports is OFF ON (b), input ports is ON OFF (c) and input ports is ON (d)
produce a logic 1 at the output port which is port 4 and as a result, the transmission, in this case, is 0.327 which is above the threshold value (0.3), and that represents logic 1.

When the input ports are in an ON-ON state, the proper phase shift among the input ports and the control port (which is always ON) is 90° to produce a logic 0 at the output port (port 4) due to the damaging interference. Now the case of input ports (ON–OFF), whereas the phase shift between the input port 1 and the control port is 0 to generate the enhancement interference and thus the transmission exceeds 100% (1.46), but when the input port states are opposite, the output port has also logic 1 under the condition of 0 phase shift between input port 2 and the control port but the transmission does not exceed the 100 percent (0.620) and the reason behind that is the asymmetry situation that happened in the structure for this case because the right side of the structure as shown in Fig. 2 is the side with powers while the left side of our proposed structure is without power because the case is the (OFF–ON) state.

The function of the suggested hybrid NAND gate is listed in Tables 12. and 13. The transmission spectrum and the magnetic field (Z component) are shown in Figs. 12 and 13 respectively.

For the NOR hybrid plasmonic logic gate, logic1 appears only in the case of the input ports are logic 0. For the case of opposite states at input ports (OFF–ON), a phase difference of 180° between the input port 2 and the control port had been set to guarantee a damaging interference, and that lead to a logic 0 at the output port with a transmission of 0.034 and that below the threshold point 0.3, while in (ON–OFF) states at the input ports also to produce a destructive interference a phase shift of 180 has taken into account and here give the minimum transmission at the output port of our structure for all situations of the hybrid logic gates and that is 0.0049 out of the 0.3 threshold value. the other cases of the input ports (OFF-OFF) and (ON-ON) are similar to the NAND hybrid plasmonic logic gate.

The function of the suggested hybrid NOR gate is listed in Tables 14 and 15. The transmission spectrum and the magnetic field (Z component) are shown in Figs. 14 and 15 respectively.

| Table 12 | The transmission values for the suggested hybrid NAND gate |
|----------|-----------------------------------------------------------|
| Inputs   | Input port 1 (phase) | Input port 3 (phase) | Control port 2 (phase) | Transmission | Output |
| Logic 0  | Logic 0            | OFF (0°)             | OFF (0°)             | 0.327/0.3   | Logic 1 |
| Logic 0  | Logic 1            | OFF (0°)             | ON (0°)             | 0.620/0.3   | Logic 1 |
| Logic 1  | Logic 0            | ON (0°)              | OFF (0°)             | 1.460/0.3   | Logic 1 |
| Logic 1  | Logic 1            | ON (0°)              | ON (90°)            | 0.034/0.3   | Logic 0 |

| Table 13 | Computations of the Contrast ratio, modulation depth and insertion loss for the presented hybrid NAND gate |
|----------|---------------------------------------------------------------------------------------------------|
| Output power (μW) | Contrast ratio | Modulation depth | Insertion loss |
| PMin | ON | 0.327 | 0.034 | 9.83 dB | 97.67% | − 4.854 dB |

The function of the suggested hybrid NAND gate is listed in Tables 12. and 13. The transmission spectrum and the magnetic field (Z component) are shown in Figs. 12 and 13 respectively.
Fig. 12  The spectrum of the power ratio (transmission) of the suggested hybrid NAND gate

Fig. 13  Allocation of the magnetic field (Z component) of the presented structure for NAND gate when input ports is OFF (a), input ports is OFF ON (b), input ports is ON OFF (c) and input ports is ON (d)
Now for the XNOR hybrid plasmonic logic gate, it can be noted that the only case to generate logic 1 at the output port (port4) is when the input ports have the same logic levels.

In the XNOR logic gate, the case of maximum transmission is also achieved when both input ports are in ON state because there is no phase shift among the inputs and the control port (phase shift = 0) lead to a constructive interference, that would affect the value of the modulation depth in XNOR and its equal to (99.75%) due to its dependence

| Table 14 | The transmission values for the suggested hybrid NOR gate |
|----------|----------------------------------------------------------|
| Inputs   | Input port 1 (phase) | Input port 3 (phase) | Control port 2 (phase) | Transmission | Output  |
| Logic 0  | Logic 0 OFF (0°)     | OFF (0°)              | ON (0°)                | 0.327/0.3    | Logic 1 |
| Logic 0  | Logic 1 OFF (0°)     | ON (0°)               | ON (180°)              | 0.071/0.3    | Logic 0 |
| Logic 1  | Logic 0 ON (0°)      | OFF (0°)              | ON (180°)              | 0.0049/0.3   | Logic 0 |
| Logic 1  | Logic 1 ON (0°)      | ON (90°)              | ON (180°)              | 0.034/0.3    | Logic 0 |

Table 15 | Computations of the Contrast ratio, modulation depth and insertion loss for the proposed hybrid NOR gate |
|----------|----------------------------------------------------------------------------------------------------------------|
| Output power (μW) | Contrast ratio | Modulation depth | Insertion loss |
| P_{Min} | ON 0.327 | 0.071 | 6.63 dB | 98.5% | −4.854 dB |

Fig. 14 The spectrum of the power ratio (transmission) of the suggested hybrid NOR gate
on the value of the maximum transmission and also the value of the minimum transmission, and that the difference from the case of the NOR logic gate. the value of the contrast ratio is the same for both NOR and XNOR equal to 6.63, the reason behind that they have the same value of variance.

The proposed hybrid XNOR gate function is listed in Tables 16 and 17. The transmission spectrum and the magnetic field (Z component) are shown in Figs. 16 and 17 respectively.

4 Proposed work versus previous works

A comparison has been made between the suggested work and some recent previous works as listed in Table 18.

| Inputs | Input port 1 (phase) | Input port 3 (phase) | Control port 2 (phase) | Transmission | Output |
|--------|----------------------|----------------------|------------------------|-------------|--------|
| Logic 0 Logic 0 | OFF (0°) | OFF (0°) | ON (0°) | 0.327/0.3 | Logic 1 |
| Logic 0 Logic 1 | OFF (0°) | ON (0°) | ON (180°) | 0.071/0.3 | Logic 0 |
| Logic 1 Logic 0 | ON (0°) | OFF (0°) | ON (180°) | 0.0049/0.3 | Logic 0 |
| Logic 1 Logic 1 | ON (0°) | ON (0°) | ON (0°) | 2.023/0.3 | Logic 1 |
In this work, a new hybrid plasmonic waveguide structure has been used to realize all-optical seven logic gates, these gates are NOT, OR AND, XOR, NAND, NOR, and XNOR. Based on the coupling theory and the nature of the material used, transmission at the output port can be achieved. By changing the phase of the incident light to the input port(s), the control port, and by optimally distributing positions of these ports, the magnitude of the transmission in the output port can be controlled, thus producing the hybrid plasmonic logic gates in the same structure and some of them with transmission amplification. A threshold value had been chosen for the transmission and it is (30%) to distinguish between logic 1 and logic 0 at output port leads to achieving the gates at 1310 nm. The realized gates represent the building block for the photonic integrated circuits.

### Table 17

| Output power (μW) | Contrast ratio | Modulation depth | Insertion loss |
|-------------------|----------------|------------------|----------------|
| P_{Min} ON        | P_{Max} OFF    |                  |                |
| 0.327             | 0.071          | 6.63 dB          | -4.854 dB      |

![Fig. 16](image_url)  

The spectrum of the power ratio (transmission) of the suggested hybrid XNOR gate

### 5 Conclusion

In this work, a new hybrid plasmonic waveguide structure has been used to realize all-optical seven logic gates, these gates are NOT, OR AND, XOR, NAND, NOR, and XNOR. Based on the coupling theory and the nature of the material used, transmission at the output port can be achieved. By changing the phase of the incident light to the input port(s), the control port, and by optimally distributing positions of these ports, the magnitude of the transmission in the output port can be controlled, thus producing the hybrid plasmonic logic gates in the same structure and some of them with transmission amplification. A threshold value had been chosen for the transmission and it is (30%) to distinguish between logic 1 and logic 0 at output port leads to achieving the gates at 1310 nm. The realized gates represent the building block for the photonic integrated circuits.
Fig. 17 Allocation of the magnetic field (Z component) of the presented structure for XNOR gate when input ports is OFF (a), input ports is OFF ON (b), input ports is ON OFF (c) and input ports is ON (d)
### Table 18: Comparison of the suggested work with previous works

| Criteria                                           | This paper                                    | Sharma and Kumar (2018) | Cui and Yu (2018)         |
|----------------------------------------------------|-----------------------------------------------|-------------------------|---------------------------|
| Software program used                              | FEM-2D                                        | FEM-2D                  | FDTD                      |
| Proposed structure                                 | Square-shaped nanoring hybrid plasmonic waveguides (HPWGs) | Hybrid metal insulator metal plasmonic Y-splitter | Multimode interference HPWGs |
| Number of proposed logic gates                      | 7 gates                                       | 3 gates                 | 4 gates                   |
| Proposed logic gates                                | NOT, OR, AND, XOR, NAND, NOR, and XNOR       | NOT, OR and XOR         | NOT, OR, AND and XOR      |
| Realization of proposed plasmonic logic gates       | All proposed hybrid plasmonic gates are admitted in a single structure | All proposed hybrid plasmonic gates are admitted in two configuration area | All proposed hybrid plasmonic gates are admitted in a single structure |
| Size                                               | 400 nm × 400 nm                              | 17.12 μm² and 19.6 μm² | 1000 nm × 3200 nm         |
| Operating wavelength(s)                            | 1310 nm                                      | 1550 nm                 | 1550 nm                   |
| Dielectric material used                           | Teflon                                        | SiO₂                    | SiO₂                      |
| Nobel metal used                                    | Silver                                        | Silver                  | Silver                    |
| Semiconductor used                                  | Aluminum oxynitride, ALON                     | Silicon                 | Silicon                   |
| Model of description the relative permittivity of the silver | Johnson and Christy data                     | –                       | –                         |
| Model of description the relative permittivity of the ALON | Hartnett et al. data                         | –                       | –                         |
| Performance measured                               | Transmission, contrast ratio, modulation depth and insertion loss | Transmission and contrast ratio | Transmission and contrast ratio |
| Transmission threshold between ON/OFF states        | 30%                                           | Less than 63%           | Variable                  |
|                                                    |                                               | 2% NOT                  | 20% NOT                   |
|                                                    |                                               | 20% OR                  | 20% AND                   |
|                                                    |                                               | 2% XOR                  | 2% XOR                    |
| Criteria                  | This paper            | Sharma and Kumar (2018) | Cui and Yu (2018) |
|--------------------------|-----------------------|-------------------------|-------------------|
| Maximum transmission %   | 146% at NOT gate       | 63.4% at NOT            | 14% at NOT        |
|                          | 202.3% at OR gate      | 131.6% at OR gate       | 96% at OR gate    |
|                          | 202.3% at AND gate     | 66.5% at XOR gate       | 40% at AND gate   |
|                          | 72.3% at XOR gate      |                         | 14% at XOR gate   |
|                          | 146% at NAND gate      |                         |                   |
|                          | 32.7% at NOR gate      |                         |                   |
|                          | 202.3% at XNOR gate    |                         |                   |
| Amplifying of transmission | NOT gate, OR gate, AND gate, NAND gate and XNOR gate | OR gate | Does not exist |
|                          |                       |                         |                   |
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**Declarations**

**Competing interests** The authors have not disclosed any competing interests.

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