Size-dependent Transport Study of In$_{0.53}$Ga$_{0.47}$As Gate-all-around Nanowire MOSFETs: Impact of Quantum Confinement and Volume Inversion

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Abstract—InGaAs gate-all-around nanowire MOSFETs with channel length down to 50nm have been experimentally demonstrated by top-down approach. The nanowire size-dependent transport properties have been systematically investigated. It is found that reducing nanowire dimension leads to higher on-state performance of InGaAs GAA nanowire MOSFETs. To our surprise, higher $I_{on}$ and intrinsic $g_m$ have been obtained on devices with smaller nanowire size. The low field mobility ($\mu_0$) is extracted using the Y-function method to further elucidate the transport performance of the nanowire devices [5], confirming the enhanced mobility for smaller nanowires. TCAD quantum mechanical simulation is employed to study the underlying physical mechanism [6]. It is shown that quantum confinement and volume inversion effects play an important role in the improved transport properties for the InGaAs GAA nanowire MOSFETs.

Index Terms—InGaAs, gate-all-around, nanowire.

I. INTRODUCTION

InGaAs MOSFETs have recently been considered as one of the promising candidates for beyond 14nm logic applications [1]. To meet the stringent demands of electrostatic control, non-planar 3D structures have been introduced to the fabrication of InGaAs MOSFETs, including InGaAs FinFETs [2], multi-gate InGaAs quantum wells FETs [3] and most recently, InGaAs gate-all-around (GAA) nanowire MOSFETs [4].

In particular, the InGaAs GAA nanowire MOSFETs have been shown to offer good scalability down to channel length ($L_{ch}$) of at least 50nm, thanks to the best electrostatic control of the GAA structure. High drive current ($I_{on}$) of 1.17mA/$\mu$m and peak transconductance ($g_m$) of 0.7mS/$\mu$m have also been achieved [4] despite the non-optimized source/drain resistance ($R_{S/D}$) and large equivalent oxide thickness (EOT), showing great promise of the InGaAs GAA technology. Moreover, a detailed scaling metrics study has also revealed that reducing the nanowire size leads to improvements in subthreshold swing (SS), drain induced barrier lowering (DIBL), and threshold voltage ($V_T$) roll off, due to the tighter gate control [4]. However, the impact of nanowire size on the transport properties of InGaAs GAA nanowire MOSFETs has not been studied and could lead to better understanding and design guidelines for next-generation InGaAs nanowire devices.

II. DEVICE FABRICATION

![Figure 1](image) Fig. 1. (a) Key fabrication process steps of InGaAs GAA nanowire MOSFETs by top-down approach. (b) Schematic diagram of an InGaAs GAA nanowire MOSFET and InGaAs nanowires with two different sizes under investigation (30nm×30nm and 50nm×30nm). Surface orientation (100) of the top surface and ideal side surface with vertical sidewall are illustrated. The nanowire patterning and current transport direction of [100] is depicted. A cross-sectional TEM image of an InGaAs GAA nanowire MOSFET with $W_{NW}$ of 30nm is also shown. The actual width and height of the nanowire is measured to be 26nm and 27nm with a ~25° angle between actual and ideal sidewall. Note that nanowires with vertical sidewall and designed $W_{NW}$ is assumed in the normalization and simulation in this letter.

In this letter, we systematically investigate the impact of nanowire size on the on-state performance of InGaAs GAA nanowire MOSFETs. The low field mobility ($\mu_0$) is extracted using the Y-function method to further elucidate the transport performance of the nanowire devices [5], confirming the enhanced mobility for smaller nanowires. TCAD quantum mechanical simulation is employed to study the underlying physical mechanism [6]. It is shown that quantum confinement and volume inversion effects play an important role in the improved transport properties for the InGaAs GAA nanowire MOSFETs.
with ammonia sulfide, 10nm Al<sub>2</sub>O<sub>3</sub> and 20nm WN were grown by atomic layer deposition (ALD) at temperature of 300°C and 385°C respectively. Due to the excellent conformal coating ability of ALD, the gate stack forms surrounding all facets of the nanowires. Gate etch using CF<sub>4</sub> based ICP etching was then carried out to define the gate pattern. Finally, ohmic contacts were formed by electron beam evaporation of Au/Ge/Ni and liftoff process. Details of the fabrication process can be found in [4].

The fabricated devices have nominal \( L_{ch} \) varying from 120nm down to 50nm. Two different nanowire width (\( W_{NW} \)) (50nm and 30nm) were defined by lithography with a fixed nanowire height (\( H_{NW} \)) of 30nm defined by the MBE channel thickness. Since the nanowires were aligned along [100] direction, both the top and side surfaces are (100) surfaces assuming vertical sidewalls. Due to the non-optimized fin etching process, the actual sidewall leans 10 to 30 degrees towards (110) surface, confirmed by the SEM images [4].

III. RESULTS AND DISCUSSION

Figure 3(a) shows the average \( I_{on} \) measured at \( V_{gs} - V_{T} = 2V \) and \( V_{ds} = 1V \) as a function of \( L_{ch} \). A gradual increase of \( I_{on} \) is observed when scaling down the channel length for both nanowire sizes. An average of 40% increase in \( I_{on} \) has been obtained on devices with \( W_{NW} \) of 30nm over the entire \( L_{ch} \) range. Devices with different \( W_{NW} \) show similar \( R_{SD} \), ranging from 950 to 1150Ω·μm. The intrinsic \( g_m \) of devices with smaller nanowire size is found to be 34% higher than those with larger nanowire size (not shown). To further characterize the transport in the nanowire devices, effective mobility was extracted using the Y-function method, which agrees reasonably well with the split-CV method and allows for the suppression of the series resistance effect [5]. Figure 3(b) shows the average \( \mu_0 \) versus \( L_{ch} \), demonstrating over 20% mobility enhancement for devices with smaller \( W_{NW} \). The apparent mobility reduction at shorter \( L_{ch} \) can be explained by Shur’s model using a Mathiessen-like relation considering the ballistic mobility [7]. It is also shown in Figure 3(b) that the extracted \( \mu_0 \) of the InGaAs GAA nanowire MOSFETs are 2-4 times higher than those from state-of-the-art Si nanowire devices [8], owing to the better transport properties of the III-V channel.

The increase in \( I_{on} \), \( g_m \), and \( \mu_0 \) has confirmed that improved transport has been obtained in smaller InGaAs nanowires. Normally for top-down nanowires, it is expected that reducing the nanowire size will degrade transport due to the relative increase in surface roughness scattering given the larger surface to volume ratio of the ultra-small nanowires. However, it has been reported on Si nanowire MOSFETs that the improved transport from high-mobility sidewall [9], oxidation induced strain inside the nanowire [10], and the volume inversion effect in nanowires with small cross sectional area [11] would result in enhanced transport properties with \( W_{NW} \) shrinkage. The InGaAs (111)A surface has been demonstrated to offer higher mobility than other crystal orientations due to the trap redistribution [12]. However, (111)A surface can not be the sidewall facet of InGaAs nanowires in this study, since previous FinFET work [2], indicating the suitability of GAA structure for logic applications.
the nanowires are aligned along [100] direction. Moreover, the thermal budget of the fabrication process after nanowire release in this letter is as low as 385°C, which is much lower than the thermal oxidation temperature (usually over 1000°C) of the Si nanowire MOSFET [10]. Therefore, strain-induced mobility enhancement can not play a significant role in the InGaAs nanowires under investigation. On the other hand, due to the much smaller effective mass and density of states of InGaAs, the inversion layer thickness can be 3.5 times larger than that of Si. As a result, inversion carriers can be pushed further away from the interfaces due to a stronger quantum confinement leading to the volume inversion effect in InGaAs nanowires at larger dimensions than Si.

To further clarify the underlying mechanism, TCAD simulation using Sentaurus Device [6] was carried out. The electron distribution inside the nanowire in the strong inversion regime is obtained using a coupled Poisson and quantum potential solver based on the density gradient model [6], [13], considering only Γ valley for InGaAs. It is found that both InGaAs GAA nanowire MOSFETs with $W_{NW}$ of 30nm and 50nm operate in the volume inversion regime, where the inversion charge density inside the entire nanowire is higher than the background p-type doping. The $W_{NW}$=30nm device show stronger confinement, resulting in the inversion layer being pushed 1~2nm further away from the surface and a higher inversion charge density at the center of nanowire compared to the $W_{NW}$=50nm case, as shown in Figure 4(a). This would lead to suppressed surface roughness scattering for the smaller nanowire. Furthermore, the volume inversion also results in the inversion layer centroid of the smaller nanowire being closer to the surface and therefore an increase in electrostatic capacitance with decreasing $W_{NW}$. It is also found that the two inversion layers inside InGaAs nanowire would merge into one peak at a dimension of ~10nm, twice as large as that in the Si case (~5nm) as shown in Figure 4(b). The inversion layer distributes further inside the InGaAs nanowire with a higher density at the center compared to the Si case with the same nanowire size. Further experimental efforts reducing InGaAs nanowire size are required to illuminate on the ultimate scaling limit of InGaAs GAA nanowire MOSFETs, which may require development of new nanowire thinning techniques. The volume inversion at a larger dimension and a stronger quantum confinement in the InGaAs GAA nanowire MOSFETs may relax the fabrication complexity and interface quality requirements for InGaAs nanowire devices.

IV. CONCLUSION

In this letter, we have fabricated and characterized InGaAs GAA nanowire MOSFETs with different nanowire size. Enhanced transport properties have been confirmed on InGaAs nanowires with a smaller dimension, due to a stronger quantum confinement and volume inversion effect. It is shown that distribution of inversion carriers moves further away from the surface and volume inversion occurs at a larger dimension on InGaAs nanowire than its Si counterpart, making InGaAs GAA MOSFETs favorable for future logic applications.

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Fig. 4. (a) Cross sectional distribution of electron density in the In0.53Ga0.47As nanowire with $W_{NW}$ of 30nm and 50nm at $V_{GS}−V_{T}=1.2$V. Dashed line shows the inversion layer centroid. (b) Normalized electron distribution at the middle of the nanowire ($y=0.5H_{NW}$) for square-square Si and In0.53Ga0.47As nanowires. Note that vertical sidewalls are assumed in the simulation. While the sidewalls in the experiments are not vertical, resulting in reduced gate control, the general scaling trend comparing nanowires with different sizes remains unchanged.