"Entirely protecting operating systems against transient errors in space environment"

Tokponnon, Mahoukpego Parfait ; Lobelle, Marc ; Eugene C. Ezin

ABSTRACT

In this article, we propose a mainly-software hardening technique to totally protect unmodified running operating systems on COTS hardware against transient errors in heavily radiation - flooded environment like high altitude space. The technique is currently being implemented in a hypervisor and allows to control the upper layers of the software stack (operating system and applications). The rest of the system, the hypervisor, will be protected by other means, thus resulting in a completely protected system against transient errors. The induced overhead turns around 200% but this is expected to decrease with future improvements.

CITE THIS VERSION

Tokponnon, Mahoukpego Parfait ; Lobelle, Marc ; Eugene C. Ezin. "Entirely protecting operating systems against transient errors in space environment." European Dependable Computing Conference (EDCC Fast abstract) 2017 (Geneve, Suisse, du 04/09/2017 au 08/09/2017). http://hdl.handle.net/2078.1/196062

Le dépôt institutionnel DIAL est destiné au dépôt et à la diffusion de documents scientifiques émanant des membres de l'UCLouvain. Toute utilisation de ce document à des fins lucratives ou commerciales est strictement interdite. L'utilisateur s'engage à respecter les droits d'auteur liés à ce document, principalement le droit à l'intégrité de l'œuvre et le droit à la paternité. La politique complète de copyright est disponible sur la page Copyright policy.

DIAL is an institutional repository for the deposit and dissemination of scientific documents from UCLouvain members. Usage of this document for profit or commercial purposes is strictly prohibited. User agrees to respect copyright about this document, mainly text integrity and source mention. Full content of copyright policy is available at Copyright policy.
Entirely protecting operating systems against transient errors in space environment

Mahoukpégo Parfait Tokponnon * †
mahoukpego.tokponnon@uclouvain.be

Marc Lobelle *
marc.lobelle@uclouvain.be

Eugene C. Ezin †
eugene.ezin@ifri.uac.bj

* Computing Science and Engineering Department
Université catholique de Louvain

† Institut de Formation et de Recherche en Informatique
Université d’Abomey-Calavi

Abstract—in this article, we propose a mainly-software hardening technique to totally protect unmodified running operating systems on COTS hardware against transient errors in heavily radiation-flooded environment like high altitude space. The technique is currently being implemented in a hypervisor and allows to control the upper layers of the software stack (operating system and applications). The rest of the system, the hypervisor, will be protected by other means, thus resulting in a completely protected system against transient errors. The induced overhead turns around 200% but this is expected to decrease with future improvements.

Index Terms—Transient errors, hypervisor, operating system, fault tolerance.

I. INTRODUCTION

A transient error is a change of state of a logical node in an electronic component (0 to 1 or 1 to 0) due to interaction between ionizing particles contained in cosmic rays and silicon atoms which generally compose integrated circuits. Although these errors do not damage the circuit, they may cause crashes, hangs and sometimes even erroneous results in Operating Systems (OS) and applications running on ordinary unprotected processors [1]. Therefore, for critical missions, ordinary equipment may not be used in an radiation-flooded environment without special care. Even though they are generally cheaper than hardware-hardened circuits because the latter are manufactured in little series for niche markets.

In this article, we present a technique, still under research, that combines software redundancy with usual functionalities of ordinary hardware (blended technique) in order to totally protect operating systems running on these COTS materials against transient errors. In the first part of this article, we present the technique in more detail, after specifying the objective of this work, then we will give some results we achieved so far.

II. BLENDED HARDENING CONCEPT

A. Objective

We propose to use some of the functionalities of ordinary hardware to detect and inhibit errors that occur in the circuit based on redundancy of execution. This is a Blended Hardening Technique (BHT) that allows to protect a full computing system at runtime with no need to access its source code.

B. Blended hardening technique : Background

Considering a running program which is a long stream of machine instructions, the BHT here consists of:

- splitting, during execution, each program to be hardened into small sets of subsequent instructions called Processing Elements (PE),
- running them twice,
- and comparing their execution traces to detect any occurring errors.

The Fig.1a gives a conceptual view of how each PE is processed. When errors are detected, the execution is simply rejected and the processing is resumed from the last correct execution point. The two execution have the same effect as the initial single execution. The PE is idempotent and its processing is atomic. For this to hold, the BHT sets two postulates:

- Firstly, zero or at most one transient error per treatment: Thus, if there is an error, it would be either during the first execution, or during the second execution, or during the verification/commit phase, but never two or all phases will be erroneous. The statistical study in [2] has shown that transient errors in an radiated environment follow the Poissons law. So, A maximum time interval, during which there can be no more than one transient error, can be deduced; no matter when the interval is taken.
- Secondly, a central memory, fully immune against transient errors, is necessary in order to preserve all data, coming from an error-free execution and saved in the main memory, from erroneous alteration. In this way one is sure to always start the processing of a PE from reliable data. The manner of obtaining such kind of memory from ordinary materials will not be discussed in this paper.

This model has been formally proven in [3]. In this article, such an interval had been calculated for a Leon processor (10µs) and a stand-alone program had been hardened by Lesage et al, using the BHT.

As the results were encouraging, the following step was to
bring this technique to a more complex environment such as multitasking OS. This work is undergoing research where the kernel of Minix is being modified to harden its user applications that run on top of it [4]. The hardening module being incorporated in the core, the OS itself remains thus unprotected. That’s why we are searching to completely protect the OS, using a hypervisor (Nova [5]) essentially because of its inherent ability to manipulate OS.

III. METHODOLOGY

A. Hypervisor based hardening

A hypervisor is software that runs directly on the hardware and can host one or more OS(s) in virtual machines. Thanks to the hypervisor, OSs run identically as if they were running on a bare machine (confer Fig. 1b). Above the hypervisor and in user mode is the program called VMM (Virtual Machine Monitor) which is actually a set of system programs. Its role is to control, and emulate the virtual machine on which the guest system believes it is running.

B. Approach

To achieve this, we have subdivided the work into three steps:

- Harden programs in the VMM
- Harden of OSs running on top of them
- Harden the hypervisors layer: but this last part is identical to the hardening of the standalone program Lesage had already achieved [3]. The hypervisor is also a standalone program that runs on the bare machine with the source code at disposal.

IV. MID-TERM RESULTS

The first part of the work is currently finished, with the actual hardening of all the system processes in the VMM completely done. This means that an error that occurs during the execution of any VMM process is automatically detected and inhibited. The overhead currently revolves around 2 times the normal execution in average. As shown in Fig 2a this overhead is more severe when the hardened program release itself the CPU (self-stop) than when we had to interrupt it by a timer(timer-stop); that is because the PE execution time is shorter in the first case.

V. RELATED WORKS

Other techniques have also been proposed in this field. Although Romain [6] ensures an overhead of 30% when all redundant threads are spread on available CPU cores (Fig 2b), it does not provide an entire protection against transient errors. We have not yet tested the BHT but this technique is designed to provide total protection for unmodified operating systems at runtime without needing to recompile them.

VI. FUTURE WORKS

The rest of the work will be devoted specifically to the hardening of the virtualized OS. We will focus on:

- privileged instructions management
- PE delimitation for guest OS and
- management of device drivers contained in guest OSs.

We will then test the system by both simulated transient errors and exposition to ionizing radiation in space environment to test it under real conditions.

VII. CONCLUSION

We have shown in this paper a mainly-software method to protect the execution of operating systems on ordinary hardware against transient errors in highly radiation-flooded environment.

We outlined the level reached and an overview of what remains to be done. Current level implementation gives a rather encouraging overhead and presages of acceptable overhead once the work will be finished.

REFERENCES

[1] H. Madeira, R. R. Some, F. Moreira, D. Costa, and D. Rennels, “Experimental evaluation of a cots system for space applications,” in Dependable Systems and Networks, 2002. DSN 2002. Proceedings. International Conference on. IEEE, 2002, pp. 325–330.

[2] T. Goka, S. Kuboyama, Y. Shimano, and T. Kawanishi, “The on-orbit measurements of single event phenomena by eta-v spacecraft,” IEEE transactions on nuclear science, vol. 38, no. 6, pp. 1693–1699, 1991.

[3] L. Lesage, B. Mejias, and M. Lobelle, “A software based approach to eliminate all SEU effects from mission critical programs,” in 12th European Conference on Radiation and Its Effects on Components and Systems (RADECS). IEEE, 2011, pp. 467–472.

[4] E. Assogba, “Etude de la tolérance aux fautes transitoires dans le système dexploitation minix 3,” 2011.

[5] U. Steinberg and B. Kauer, “Nova: a microhypervisor-based secure virtualization architecture,” in Proceedings of the 5th European conference on Computer systems. ACM, 2010, pp. 200–222.

[6] B. Doebel, “Operating system support for redundant multithreading,” october 2014. [Online]. Available: https://pdfs.semanticscholar.org/5b77/e0edbac8851701da.pdf