Exploiting Fine-Grain Ordered Parallelism in Dense Matrix Algorithms

Jian Weng, Vidushi Dadu, Tony Nowatzki

University of California, Los Angeles
{jian.weng, vidushi.dadu, tjn}@cs.ucla.edu

ABSTRACT
Dense linear algebra kernels are critical for wireless applications, and the oncoming proliferation of 5G only amplifies their importance. Many such matrix algorithms are inductive, and exhibit ample amounts of fine-grain ordered parallelism – when multiple computation flows with fine-grain producer/consumer dependences, and where the iteration domain is not easily tileable. Synchronization overheads make multi-core parallelism ineffective, and the non-tileable iterations make the vector-VLIW approach less effective, especially for the typically modest-sized matrices.

Because CPUs and DSPs lose order-of-magnitude performance/hardware utilization, costly and inflexible ASICs are often employed in signal processing pipelines. A programmable accelerator with similar performance/power/area would be highly desirable. We find that fine-grained ordered parallelism can be exploited by supporting: 1. fine-grained stream-based communication/synchronization; 2. inductive data-reuse and memory access patterns; 3. implicit vector-masking for partial vectors; 4. hardware specialization of dataflow criticality.

In this work, we propose, REVEL, as a next-generation DSP architecture. It supports the above features in its ISA and microarchitecture, and further uses a novel vector-stream control paradigm to reduce control overheads. Across a suite of linear algebra kernels, REVEL outperforms equally-provisioned DSPs by 4.6x-37x in latency, and achieves a performance per mm$^2$ of 8.3x. It is only 2.2x higher power to achieve the same performance as ideal ASICs, at about 55% of the combined area.

1. INTRODUCTION
Dense linear algebra kernels, like matrix factorization, multiplication, decomposition and FFT, have for decades been the computational workhorses of signal processing across standards, specifications, and device settings. The oncoming proliferation of 5G wireless is only further pushing the computational demands, both in performance and energy efficiency. Driven by needs of higher capacity and applications like augmented and virtual reality [1], new standards will require signal processing at more than an order-of-magnitude higher throughput and lower latency.

Despite their ubiquity, many important dense matrix operations are far from trivial to parallelize and compute at high hardware efficiency. As evidence, Figure 1 shows the hardware utilization (based on max. vector issue width), of a modern CPU and DSP running common DSP algorithms from native application suites (eg. MKL, and TI DSPLIB). For algorithms without fine-grain dependences (GEMM, FIR, and FFT), a reasonable utilization is achieved, usually between 30-80%. However, for factorization/decomposition (SVD, QR, Cholesky, Solver), the utilization is exceptionally poor, generally between 5%-20%. Even this measure is generous as we only consider the maximum throughput of a single core, yet there is enough raw parallelism to multithread. Empirically, however, MKL and TI libraries do not even invoke multiple threads at the commonly-small matrix sizes required, due to synchronization overheads. CPUs and DSPs leave untapped factors of performance/hardware utilization.

The challenge and opportunity comes from the dominant form of parallelism in these workloads, which we call fine-grained ordered parallelism (FGOP). FGOP consists of fine-grain producer/consumer relationships between otherwise parallel computations, where the rate of production-to-consumption, the rate of data reuse, and the memory access relation is an affine function of the induction variables. This results from the iterative and inductive nature of these algorithms, as they operate on relatively small matrix sizes.

To substantiate, consider the triangular solver in Figure 2(a). Its iteration space diagram, 2(b), reveals the many

Figure 1: Percent peak performance of CPU (Intel Xeon 4116) and DSP (TI C6678) on DSP kernels

Figure 2: FGOP Example: Triangular Linear Solver
fine-grain dependences that make profitable multithreading between regions impossible. Furthermore, the inner-loop trip count changes inductively, leading to many iterations that are difficult to vectorize. Nevertheless, an architecture can be designed to exploit FGOP; the potential is shown in Figure 2(c,d). If dependences between regions can be enforced at a fine-grain with low overhead, then overlap between regions becomes possible, increasing the parallelism. If the inductive memory access pattern (and its relationship to computation) can be expressed efficiently, then vectorization can reduce the total time of the inner-loop region.

ASICS can of-course be designed to exploit FGOP – hence why they are so commonly employed for these tasks. Unfortunately, they have significant drawbacks: design time and verification effort, extra on-chip area, lack of flexibility, and lengthened time-to-market; these are especially relevant for example domain of wireless, where standards are continually changing and infrastructure costs are high. A general and programmable architecture exploiting FGOP could prove to be a worthy, if not essential, replacement of traditional vector-VLIW DSP architectures.

**Goals:** Our goals are twofold: 1. developing abstractions and execution semantics to enable efficient expression of FGOP; and 2. applying these abstractions to create an efficient programmable accelerator instance for DSP algorithms, capable of accelerating both FGOP and non-FGOP workloads in this domain (eg. GEMM, filters).

**Approach:** Through an in-depth workload analysis, we find four essential architecture abstractions to express FGOP efficiently to hardware: 1. parallel dataflows with ordered communication channels. 2. to reduce control overhead, induction-variable dependent communication, memory access, and data-reuse. 3. for efficient vectorization, the implicit masking of non-vector-width-divisible iterations. 4. for high hardware utilization, the specialization of compute hardware for critical versus non-critical dataflows.

While in principle the above abstractions can be added to a conventional ISA, we choose a stream-dataflow ISA [2], as its dataflow-based computation and communication abstractions are simple to modify, and the resulting accelerator can be performance/power competitive with DSPs. For the hardware implementation, we start with a simple design for one lane: a scratchpad connected to a coarse grain reconfigurable fabric (eg. similar to some previous designs [3, 4, 5, 6]). We use multiple such “lanes” to scale up the design.

Our accelerator, REVEL: the Reconfigurable Vector Lane architecture (Figure 3), is constructed by adding support for each of the FGOP-exploiting abstractions: 1. We allow multiple parallel dataflows (similar to threads) which can communicate within/across lanes through FIFOs to support synchronization on fine-grain dependences. To simplify the ordering of commands, we centralize control into one control-core which coordinates all lanes. 2. We provide the ability to express inductive memory access, data-reuse and communication patterns by adding suitable state machines to FIFO communication structures. 3. We implement implicit vector masking by exploiting the relationship between computation-vector width and communication-stream length. 4. For high computation utilization, we develop a novel heterogeneous compute fabric, where different regions are specialized for critical and non-critical dataflows.

**Our contributions are:**
- Identification and characterization of fine-grain ordered parallelism (FGOP) as the main challenge for accelerating many dense linear algebra kernels.
- Architecture and execution model for expressing FGOP naturally to hardware.
- Novel architecture features (vector-stream control, inductive access/reuse, implicit vector-masking, and heterog. fabric), enabling ASIC-like power/area/performance.

**Results:** A single 1.25GHz REVEL unit can outperform a 2.1GHz OOO core running highly-optimized MKL code on DSP workloads by mean 9.6×, with an area normalized speedup of 1308×. Compared to a DSP, REVEL achieves between 4.6×-37× lower latency, with an area normalized speedup of 8.3×. Compared to a set of ideal ASICs with equivalent performance, it is about 2.2× higher power and .55× the area.

**Paper Organization:** We briefly motivate the kernels in Section 2, and analyze their challenges/potential in Section 3. The FGOP abstractions and ISA instance (REVEL) are in Sections 4 and 5. Section 6 and 8 describe the microarchitecture and compiler. Methodology and results are in Sections 9 and 10. We finally cover related work and conclude.

**2. WHY THESE WORKLOADS?**

We examine these DSP workloads as they represent a coherent and important set, and because exploiting FGOP is critical for their performance. To elaborate, Figure 4 shows the stages of a typical 4G/5G transmitter/receiver.

**Kernels we do not target:** Channel coding and modulation involve mostly bit-level arithmetic. RE mapping is a short resource allocation phase which is not computation intense.

**Kernels we target:** The Beamforming stage involves mostly GEMM, coming from spatial signal filtering [7]. Filters and FFT of several varieties are also common [8, 9, 10].
3. FINE-GRAIN ORDERED PARALLELISM

Here we first define FGOP properties with an example kernel, and explain why each is important either as a challenge or opportunity. Then we characterize their prevalence in our workloads and beyond. Finally, we perform a case study to answer why task-parallelism plus vectorization is insufficient.

3.1 Characteristic Properties of FGOP

We use Cholesky decomposition as a running example in Figure 5. Cholesky contains a point, a vector, and a matrix computation region. In general, regions correspond to computations either across subsequent loops, or from within the same imperfect loop but at different nesting levels.

**Property 1: Parallel Flows with Fine-grain Dependences:**
A central characteristic of FGOP is the presence of fine-grain dependences between regions. In Cholesky, the vector and matrix region are dependent on the point region (forward dep.), and the point region is dependent on the first element in the matrix region (loop carried dep.). For a small matrix, the granularity of these dependences is a few hundred instructions or less, and even lower as the algorithm progresses.

*Why is this important:* the presence of these fine-grain dependences is the key limiter to performance of multithreading the regions, due to high synchronization overhead.

**Property 2: Ordered Dependences:**
Dependences are often strictly-ordered from the perspective of their producing and consuming instructions. Figure 5(b) shows Cholesky’s iteration space and dependences. In Cholesky, across multiple iterations of the outer i loop, the point region is producing values (inv and sqrt) that are consumed by the matrix region. Similarly, the matrix region produces values consumed by subsequent iterations of the point region. An example of a non-ordered dependence is when an array is consumed in the backwards order of how it was produced.

*Why is this important:* the structure of ordered dependences makes fine-grain synchronization of these dependences natural, and therefore creates an opportunity to exploit efficiently in hardware.

**Property 3: Inductive Access/Data-Reuse:** An inductive algorithm iteratively builds on previous computations. In array codes, this often manifests as induction-variable dependent trip-counts. This is the case for both of Cholesky’s loops (but would not, for example, be true of a matrix multiply).

This has implications for dependences, in that their reuse pattern (the rate of production to consumption) would be induction-variable dependent. For example, how many times inv is consumed in the matrix region varies with k and j. Another example is that the matrix region only produces a value for the next point region on the first iteration of the inner loop (so depends on k).

Also, inductive loops cause patterns of computation/memory that are not easy to tile with vectorized loop iterations. Figure 5(b) also shows a vector-tiling pattern for Cholesky, with many leftover iterations. In a traditional vector architecture, these would require scalar iterations or masking/merging overhead.

*Why is this important:* inductive patterns cause overheads for coordination of vector computation, as well as the wide interface to memory.

**Property 4: Region Imbalance:**
Finally, regions often express imbalanced amounts of work. In Cholesky, the matrix region performs much more computation than the others, making it critical for performance. In the Figure 5(a), we highlight the critical region in red, and the sub-critical regions in purple. In DSP workloads, sub-critical regions often contain high-latency operations like agt and div.

*Why is this important:* for a high hardware utilization, execution resources should be allocated appropriately to regions. Furthermore, we will show how it is possible to specialize the computation substrate for criticality.

**Similar properties in QR, SVD:** Figure 6 shows that both have fine-grain ordered deps. between scalar/matrix regions (eg. tau and between inner loops (eg. v[j]). Inner loops are inductive and imbalanced compared to householder region.

**Prevalence of FGOP:** We characterize the prevalence of each FGOP property in our 7 DSP workloads (Cholesky, QR, SVD, Solver, FFT, GEMM, Filter), as well as a more general dense matrix benchmark suite, PolyBench [16]. We use LLVM [17] to instrument programs to track dynamic memory dependences. Figure 7 shows a cumulative density
function (CDF) for each property across three different matrix sizes (16, 32, 128).

- **Fine Granularity**: Figure 7(a) characterizes the distance between inter-region dependences in terms of arithmetic instructions. Most dependences (where the steepest part of the CDF curve is) are between about 75 to 1000 instructions, where larger data sizes are on the higher end. Intuitively, this is a range where an out-of-order (OOO) core's instruction window begins to be insufficient, but still where shared-memory based synchronization also significantly hurts performance (especially considering pipeline serialization during synchronization).

- **Ordered**: Figure 7(b) shows the prevalence of ordered dependences as a fraction of total dependences. All workloads contain at least 50% ordered dependences, and more than 80% of DSP workloads are completely ordered; this is quite high and promising for later exploitation.

- **Inductive**: DSP workloads have significant amounts of inductive access. 4/7 of the DSP workloads have more than 85% inductive accesses. PolyBench in general has much less inductive access, but still about 1/5 of those workloads are 60% inductive. Nevertheless, the inductive property is critical for our DSP workloads.

- **Imbalanced**: 4/7 DSP workloads have imbalanced regions, while 50% of PolyBench have imbalanced regions. Overall, FGOP properties are common across dense matrix workloads, especially for the relevant DSP workloads.

### 3.2 Why not task parallelism + vectorization?

We know from the data in Figure 1 (page 1) that exploiting FGOP is non-trivial for vector and VLIW cores. But why is this so, given that DSPs are designed for these workloads?

The traditional method of parallelizing workloads with FGOP is through task parallelism on a block of computations (e.g., a set of iterations). Each dependence, or set of dependences, is simply a condition under which to start a new task or synchronize existing tasks. Intuitively, this works well when dependences are coarse-grain (less overhead to start or synchronize), and when blocks are perfectly tile the iteration space. As we discussed earlier, this is not true for the DSP workloads we study.

**Case Study: Task-parallel Cholesky**: For practical analysis, we analyzed an established Cholesky kernel [18] which uses blocked task-parallel execution. Figure 8 shows the task-parallel speedup over the single-threaded industry-standard MKL for different matrix sizes (see Sec 9 for CPU and methodology). First, notice the its performance is similar to MKL for large matrices, which is possible because it underlies BLAS routines (doptf2, dtrsm, dsyrk) at a block-level. We suspect MKL's implementation uses a similar approach, but does not use task parallelism at small matrix sizes for performance reasons.

Considering the task-parallel code, the results indicate that exploiting FGOP is only **profitable** at all for larger matrices. Using more threads simply results in higher overhead of synchronization, far outweighing the benefits of parallelization. For the task-parallel version, speedups higher than 2× are only possible with matrices of 1024k size or larger, higher than we can make use of in our domain. Therefore, our goal is to create an architecture which can exploit FGOP better at all matrix sizes and enable speedup at small sizes.

### 4. ABSTRACTIONS TO EXPRESS FGOP

In this section we propose a set of architecture features which can express fine-grain ordered parallelism efficiently to hardware. The description here is architecture-neutral, and we later develop an architecture instance (an ISA).

**Feature 1: Concurrent Dataflows with Ordered Dependences**: The essential abstraction is that of concurrent dataflows (threads) with the ability to express ordered dependences between regions. Ordered dependences are distinguished from typical instruction dependences in that they have a non-uniform rate of production to consumption. A consumption rate higher than one indicates reuse of a
value along a dependence. This may occur because data is reused multiple times within a subsequent inner loop. A production rate higher than one means that several iterations occur before producing a value. For example, this could be because data is being reduced (accumulated) for several iterations. Figure 9 shows the solver kernel’s dataflows, annotated with the memory access it performs within each iteration of the outer j loop. Edges are labeled with their production:consumption rate, unless they are uniform (1:1).

**Importance of Control Overhead:** One important consideration is the control-to-computation ratio. Short-vector SIMD is one way to reduce control overhead; one SIMD instruction expresses multiple operations over a fixed number of data items. A generalization (used in a variety of prior architectures [19, 20, 2, 21, 22, 23, 24]) is the concept of streams, where a single control command describes an entire pattern of operations. The following features (2–4) are related to the use of streams to reduce control overhead.

**Feature 2: Inductive Production:Consumption Rate**

Data-reuse patterns may depend on induction variables, as seen in Figure 9. Here, the output of division is used multiple times within the inner loop, but the number of times is reduced by one each iteration. In general, we find that the pattern changes only by small constant parameters. We specify these as two “stretch” parameters: $s_p$ and $s_n$, the rate of change of production and consumption. Figure 11 contains an example encoding as a stream. Including these parameters is not necessary for correct enforcement of dependences, because multiple lower-dimension streams can be generated. However, the number of instructions increases by an order of magnitude (as shown in Figure 11).

**Feature 3: Inductive Memory Streams:** Similarly, all prior architectures that we are aware of use rectangular memory access streams: their iteration domains (without loss of generality) begin at 0 and end at a constant $n$ in each dimension (ie. a trip count), and their address functions are linear functions of $\vec{f}$. If we let $c_i$, $c_j$ etc. be the multipliers of $\vec{f}$ in the address function, rectangular streams can then be depicted intuitively as a loop nest — see Figure 10(a).

Inductive streams are more general; their iteration domains may be bounded polyhedra instead of strictly rectangular. Trip counts become a linear function of lexicographically previous iterators. We encode using stretch multipliers $s_j$, representing the multipliers of iterator $j$ in the trip count for dimension $i$. Figure 10(b) shows a 2D inductive stream pattern as a loop nest. Figure 11 shows how to specify the accesses in solver using either rectangular or inductive streams. Again, inductive access streams require O(n) fewer control insts.

Later evaluation uses a simple notation to describe capabilities: Letter “R” denotes a rectangular dimension, and “I” denotes inductive dimension, so “RI” would be a 2D capability.

(a) Solver Code

```
for (j=0; j<n; ++j)
  b[j] /= a[j,j]
for (i=j+1; i<n; ++i)
  b[i] -= b[j]*a[i,j]
```

(b) Iteration Space and Dependences

![Figure 9: Solver’s Dataflows and Ordered Dependences](image-url)

Figure 9: Solver’s Dataflows and Ordered Dependences

(a) Using 2D Rectangular Streams
(b) Using 2D Inductive Streams

(a) 2D Rectangular (RR) (b) 2D Inductive (RI)

Figure 10: Memory Address Stream Type Comparison

for $j=0$ to $n_j$
for $i=0$ to $n_i$
array $\{j+c_j+i*c_i\}$
array $\{j+c_j+i*c_i\}$

Figure 11: Stream Specification using Different Types

(a) Vectorized Critical-Region (b) Masked Lanes when $i+4>n_i$

Figure 12: Implicit Vector Masking

5. **REVEL: An FGOP-Enabled ISA**

Using the principles from the previous section, we construct an efficient and scalable ISA and execution model (REVEL ISA) to exploit FGOP and traditional parallelism in dense matrix algorithms. REVEL is an instance of a stream-dataflow ISA [2], which we chose because it is straightforward to enhance for FGOP, and it enables an efficient programmable accelerator. Section 7 discusses enhancing other architectures (OOO cores and Plasticine [4]). In this section, we discuss the control model, how the architecture incorporates FGOP features, and then its specific ISA instantiation.

**Background on stream-dataflow:** Stream-dataflow ISAs...
express computation as a dataflow graph, where its inputs and outputs are named ports. Communication is performed using streams, where the endpoints of streams are either the dataflow-graph ports or memory. A VonNeumann program embeds all stream commands, and streams with the same port number are guaranteed to be executed in program order. Memory requests can be ordered by explicit barriers.

**ISA Enhancements to support FGOP:**
- **Ordered Dependences between Dataflows**: Computation is expressed as multiple independently-triggered dataflow graphs, where streams describe their communication and re-use pattern.
- **Inductive Dependence/Access**: Stretch parameters ($s_p, s_c$) added to relevant streams.
- **Vector Masking**: Non-divisible iteration lengths causes predication of the corresponding dataflow.
- **Execution Rate**: Implementation is closely related to hardware, so we describe separately (Section 6.3).

**Example: Cholesky**: Figure 13 demonstrates REVEL’s abstractions by showing the transformation from source (a) to the abstract dataflow IR (b), and finally to dataflow configuration and stream-code running on the control core (c.d).

**Enabling Scalability with Lanes**: To enable scalability at low overhead, we chose to add multiple lanes of execution. Each lane is independent, in that it can concurrently execute multiple dataflows, each potentially communicating using inductive streams or through a global memory. Also, since each lane can be programmed separately, the architecture is flexible in terms of how computations are being parallelized.

**Vector-stream control**: There are two challenges with using multiple lanes: 1. Each lane needs coordination (control overhead), and 2. The dataflow-dependence streams between lanes must somehow be ordered.

Our solution is the vector-stream control model. Here, a single VonNeumann control program coordinates the execution of all lanes. Control commands are sent to all relevant lanes, specified by a bitmask (eg. load array from address 0 of local memory to dataflow 1). In addition, a lane’s index can be used to offset the address of a command, so a single command can allow each lane to read a different portion of an array. This is unique and more powerful than the control amortization offered by either vectorization or streaming alone, as it amortizes both in “space” across lanes, and in time through streaming commands. It is inspired by

| Pattern Parameters | Source Parameters | Dest. Parameters | Lane Bitmap (ALL) |
|--------------------|------------------|-----------------|-----------------|
| Shared_mem           | shared_addr local_addr        | local_addr shared_addr |              |
| Local_mem n0          | out_port           | local_addr          |              |
| Const                 | val1, val2         | in_port, $n_c$, $S_c$ |              |
| XFER                  | out_port           | local_addr          |              |
| Configure            | local_addr          |              |              |

Table 1: REVEL’s Vector-Stream Control Commands

Vector-threading [25, 26, 27] but with a stream-based ISA. In the example, Figure 13, we map all three dataflows (scalar, vector, matrix) to one lane to share its resources, and parallelize the outer k loop across lanes.

**REVEL Commands**: Table 1 contains the set of commands within the VonNeumann control program for stream coordination, including their pattern parameters, source, and destination. Shared_mem & St are for transfers between local and shared memory. Local_mem & St transfer between the local memory and the dataflow graph. XFER specifies inter-dataflow communication streams to support fine-grain dependences. Const can stream a pattern of val1, val2, eg. (0,0,0,1,0,1,0,1,0,1), which is useful for inductive control-flow within the dataflow graph. The Barrier command prevents concurrent scratchpad memory access, and Wait delays until a lane is no longer active. These are used for flexible double buffering. All commands take a lane bitmask as a parameter, to implement vector-stream control.

**6. REVEL MICROARCHITECTURE**

We describe REVEL’s microarchitecture by first giving a broad overview, then explaining the key innovations that enable efficient exploitation of FGOP. We discuss the heterogeneous compute fabric in detail, as it is a key novel component of the design, enabling low overhead execution of unbalanced FGOP regions.

**6.1 Hardware Overview**

The REVEL processor (Figure 14) is composed of a number of lanes, a low power VonNeumann control core, and a shared scratchpad. The control core can issue vector-stream commands to each lane. Each lane manages its stream and memory dependences, data access requests and computation

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firing. Dataflows on the same or separate lanes can communicate data through the XFER unit or shared scratchpad.

**High-level Operation:** REVEL’s high-level execution flow is as follows: First, the core will issue a config command, and configuration data is broadcast to each relevant lanes’ compute fabric and its ports. Asynchronously, the control core will begin to compute the parameters of any stream commands. When a command is ready, it will be broadcast relevant lanes’ command queues. Commands are then issued to either the private or shared scratchpad, provided the resources they depend on are free (eg. input or output compute-fabric ports). Streams execute locally until completion, until which point they notify the command queue that they are free. Independent dataflows may be mapped onto the compute fabric, where they are executed in pipelined fashion once enough data has arrived for an instance of the computation. Once the control core has completed issuing vector-stream commands, it will issue a wake command. This blocks the control program until all relevant lanes are no longer active, which is determined by the completion of all streams.

**The responsibilities of each component are:**
- **Command Queue** is the lane’s resource manager, and is responsible for maintaining data ordering. It maintains a queue of commands from the control core, and issues them to the scratchpad or XFER unit if no barrier commands or port dependencies prevent that. A scoreboard tracks ports in-use.
- **Stream Control** maintains the set of concurrent streams, where each stream tracks the state of its iterators \( (i, j) \) and length \( n_i \), (to support inductive access). It can generate addresses for one stream per cycle, along with a mask for any unused words of the scratchpad line. Streams are prioritized by minimum “cycles-to-stall,” which is the number of cycles before the corresponding port will run out of data (data-in-fifo / port-width).
- **Input/Output Ports** contain a set of FIFOs for holding intermediate results while waiting for (or produced from) the compute fabric. Input ports can receive data either from the scratchpad bus, or from the XFER unit if receiving data from a neighboring dataflow. Each port attaches to a unique location within the grid, so it is the compiler’s responsibility to choose optimal ports.
- **Compute Fabric** monitors the data ready in each input port FIFO to determine which dataflows can begin. Multiple can be fired in a single cycle. This heterogeneous fabric is divided into regions which specialize for either critical or non-critical computations (Section 6.3).
- **XFER Unit** is responsible for arbitrating the bus from output ports back to the local or remote input ports, which enables fine-grain dependences between dataflows, both within and across lanes.

### 6.2 Supporting FGOP Abstractions

Here we describe the essential hardware mechanisms for supporting FGOP within REVEL. Details on the heterogeneous compute are discussed subsequently.

**Concurrent Dataflows with Ordered Dependences:** To support multiple dataflows with different firing conditions, the data present in each dataflow’s ports are tracked separately by the data-firing logic, which can manage up to four independently-firing dataflows. The association between ports and dataflows is determined at configuration time.

One other challenge is maintaining data-ordering when there are fine-grain dependences between lanes – ie. a source lane should not transmit until all prior data items (in program order) for the destination lane’s port have arrived. This is accomplished by sending the destination lane a placeholder stream. The destination’s command queue informs the source’s when the placeholder is issued for the destination port, and the source’s command queue informs the destination’s when the placeholder can be removed.

**Inductive Memory Access:** To support inductive re-use streams, the scratchpad controller maintains the current iterator values and the current stream length. When \( n_i \) addresses are complete, the length is adjusted by the stretch \( s_{ij} \). Note that \( s_{ij} \) is a fixed-point number to support vectorization with induction patterns.

**Inductive Data Reuse:** While a stream without reuse would perform the usual destructive FIFO read on every cycle, a stream with reuse will only pop the data from the port at a longer interval. When the stream is issued from the command queue to the stream control unit, the reuse configuration \( (n_i \text{ and } s_{ij}) \) is sent to the port (maintained similarly to params for memory access). Besides enabling fine-grain dependences with inductive changes in re-use length, another benefit of the reuse within the configurable port is a large reduction in scratchpad bandwidth.

**Implicit Vector Masking:** As a stream is executing, the stream control unit compares the remaining iterations with the vector length of the destination port. If the iterations left are non-zero and less than the vector length, the stream control unit sends the data padded with zeroes for the unused lanes, along with additional meta-information which indicates that the those lanes should be predicated off. This information is buffered in a predication FIFO which tracks the data FIFO.

### 6.3 Heterogeneous Compute Fabric

Attaining high utilization in FGOP workloads requires balancing execution resources between critical and non-critical dataflows. This is especially challenging given that they prefer quite-different fabric microarchitectures.

There are two key types of fabrics with different trade-
offs. Dedicated fabrics are those that restrict each execution resource (tile) to execute only a single instruction, but pipelined at full throughput (e.g., FPCA [24], Q100 [21], Tartan [28], PipeRenCh [29], and DySER [6]). In contrast, temporal fabrics are those that may time-multiplex multiple different static instructions over the same resources (e.g., TRIPS [30], WaveScalar [31], Triggered Insts [32] and RAW [33]). While dedicated fabrics only need to wait for the arrival of data for dataflow execution, temporal fabrics require token matching, meaning more complex structures (and power/area overhead).

Because critical dataflows are often easily vectorizable by the compiler, they can be scaled to the size of the fabric, and be executed more efficiently on the more power/area efficient dedicated fabric. However, non-critical dataflows often have many instructions, and running them on a dedicated fabric would be a waste of resources (e.g., FP units) as they would attain poor utilization. Therefore, non-critical dataflows would be best run on a temporal fabric. It would also be inefficient to run critical dataflows on a smaller temporal fabric, as contention for resources would degrade the throughput. An over-provisioned temporal fabric can alleviate this, at the cost of significant power/area overhead.

Criticality-Specialization: Given the above, our approach is to make the fabric heterogeneous: provision most of the fabric’s resources to be a dedicated fabric to enable fast execution of the critical dataflows, and allocate a smaller portion to be a temporal fabric, which can execute non-critical regions efficiently. Figure 15 shows the lower corner of REVEL’s heterogeneous compute fabric, which embeds the temporal fabric’s network and compute into the dedicated fabric.

The physical network for both fabrics is a circuit-switched mesh with no flow control. The dedicated tiles simply select inputs, perform computations, and forward outputs in fully pipelined fashion according to the dataflow configured by the mesh. The dataflow compiler must equalize delays for each operand to ensure correct execution.

The temporal fabric is embedded within the circuit-switched mesh, using a pattern shown by blue arrows in Figure 15. This allows temporal units to communicate without interfering with the dedicated region (i.e., no horizontal/vertical links consumed). The temporal tile microarchitecture is based on Triggered Instructions [32], which performs operations based on the arrival of data to a queue at the input or output. A register file holds live-state of waiting instructions.

Note that dataflows communicate through ports (exiting and re-entering the fabric). The benefit of integration into the same network is that when there are no non-critical dataflows, the temporal region may be reclaimed for use by critical instructions. Section 8 details compilation concerns.

7. GENERALITY OF OUR APPROACH

Finally, we argue our approach is applicable to other architectures. Table 2 explains how to add FGOP capabilities to out-of-order (OOO) cores and Plastine [4], a reconfigurable dataflow fabric, programmed using parallel patterns. This table describes changes necessary in the software, ISA and hardware.

8. SOFTWARE STACK

A program is decomposed into two components: 1. C+intrinsic specifications including the Von Neumann control program, and 2. Dataflow specification which is mapped onto the compute fabric. A dataflow compiler (described in the next paragraph) is responsible for producing the hardware configuration bits for the temporal and dedicated portion of the fabric. These are finally compiled together to create the final RISC-V binary.

Dataflow Compiler: We implemented a spatial architecture compiler (e.g., [34, 35, 36, 37, 38]) which maps computation and communication of all dataflows together on the compute fabric. For the dedicated dataflows, all operand timing paths must be equalized, and there is no sharing of resources. For the temporal dataflows, the goal is to minimize resource contention. Usually instructions from a temporal/dedicated

| Ordered Dep. | Inductive Dep. | Inductive Mem. | Implicit Vector Mask | Crit. Specialization |
|--------------|----------------|----------------|----------------------|---------------------|
| OOO Core     | S/W | Thread-communication-aware OS sched | Streaming memory command interface | Add FIFO interf. b/t streams & vector instrs. |
|              | ISA | Stream-based producer/consumer instrs. | Add induction parameters to stream instrs. | Implicit mask register indicating predicated lanes. |
|              | H/W | Commun.-FIFOs b/t neighbor cores | Add inductive control to FIFOs | Vector store instruction ignores masked lanes. |

Table 2: Adding FGOP Abstractions to Existing Architectures

8
dataflow map to the corresponding region of the compute fabric. However, temporal instructions may map to the dedicated fabric to minimize utilization, and dedicated instructions may be mapped to the temporal fabric to minimize latency or network congestion, provided that there are enough resources either way. To balance these objectives, we take a simulated annealing approach similar to the Pathfinder algorithm [39] and prior stochastic schedulers [40], which allows resource over-provisioning to determine and then constrain heavily needed network and execution resources.

9. EVALUATION METHODOLOGY

REVEL Modeling: REVEL hardware parameters are in Table 3. For performance, all blocks are modeled at a cycle level within a modified gem5 [42][43]. We synthesized a single lane of REVEL (heterogeneous fabric, stream control, ports, command queue, XFER unit) using Synopsys DC, 28nm tech library. The design meets timing at 1.25GHz. An open source triggered instructions implementation was our reference for the temporal fabric [44]. Results from synthesis, with Cacti 7.0 [45] for SRAMs, are used to create an event-based power model and area model.

ASIC Analytical Models: These highly-optimistic models (Table 4) are based on the optimized algorithms, and are only limited by the algorithmic critical path and throughput constraints, with equivalent FUs to REVEL. ASIC area and power models only count FU and scratchpad power.

| Workload Data Size | Lane | Acc | Dep | Reuse | Het | Vec |
|--------------------|------|-----|-----|-------|-----|-----|
| SVD 12 16,24,32     | 1    | RI  | Y   | Y     | Y   | Y   |
| QR 12 16,24,32      | 8    | RI  | Y   | Y     | Y   | Y   |
| Cholesky 12 16,24,32| 8    | RI  | Y   | Y     | Y   | Y   |
| Solver 12 16,24,32  | 1    | RI  | Y   | Y     | Y   | Y   |
| FFT 64,128...1024   | 1    | RR  | N   | Y     | N   | N   |
| GEMM 12 24,48x16x64 | 8    | RR  | N   | Y     | N   | N   |
| FIR 12 16,24,32     | 8    | I   | Y   | N     | Y   | N   |

Table 5: Workload Params. and FGOP Features; small and large sizes bolded; Lane: #Lanes in latency ver., Acc: Access pat. Dep: Fine-grain deps; Reuse: stream-reuse, Het: Heterog. fabric, Vec: implicit vect. masking

• TI 6678 DSP (@1.25GHz) 8-core DSP, each core has 16-FP adders/multipliers, using DSPLIB_C66x_3.4.0.0.
• OOO Core: Intel Xeon 4116 (@2.1GHz) Conventional OOO processor using highly-optimized Intel MKL library. (8 cores used)
• REVEL-No-FGOP: REVEL without FGOP support (8 Lanes). To evaluate, we therefore also implement highly-optimized non-FGOP workload versions.

Workload Versions: We make comparisons in two different settings, high-throughput and low-latency. The throughput setting assumes there exist multiple data items to parallelize over, while the latency setting assumes only one. We implement both throughput and latency optimized REVEL workloads, where latency-optimized spreads work across multiple lanes. Throughput versions use each lane in data-parallel fashion. Note that we could not profitably parallelize any FGOP kernel across multiple DSP/OOO cores, even using native libraries, so their latency-optimized versions only use a single core. Table 5 describes data-sizes, and also how FGOP features were used by each workload.

10. EVALUATION

We broadly answer the question of whether fine-grain ordered parallelism is exploitable in DSP workloads, and if REVEL’s execution model, architecture, and microarchitecture is effective. What we find overall is that REVEL’s ability to exploit FGOP leads to order-of-magnitude speedup and area-normalized performance over traditional DSPs.

We first discuss the applicability of FGOP features and overall latency and throughput potential. We then explain how performance improvements were achieved by analyzing cycle-level bottleneck breakdowns, and incremental performance improvements. We also answer the question of sensitivity to temporal region size and address-generation capability. Finally, we analyze the area and power breakdowns, comparison of normalized performance, and compare to optimistic ASIC models.

Q1. Can workloads use REVEL’s FGOP features?: Table 5 shows the applicability of FGOP features. Matrix factorization/decomposition workloads (QR, SVD, Cholesky, Solver) use all FGOP features. Even non-FGOP workloads took advantage of streaming-reuse to reduce scratchpad bandwidth, and FIR had a short inductive access phase.

Q2. How much speedup do REVEL’s execution model and FGOP features provide?: The speedups over DSP for latency optimized codes are shown in Figure 16 for both small and large matrices. The DSP and CPU have similar mean performance. REVEL attains up to 37× speedup, with geomean
of 10× and 17× for small and large data sizes. Considering just workloads which exhibit FGOP, the speedup from FGOP specialization is 6.1× (large size). The benefit of REVEL’s dataflow/vector-stream model without FGOP provides 2.8× speedup over DSP. The DSP is only competitive on the small FFT, as REVEL here requires multiple-configurations.

Performance for throughput-optimized kernels (data parallelism across lanes), is shown in Figure 17. For small and large sizes, REVEL gets a speedup of 6.3× and 8.1× over the DSP and CPU. Again, considering just workloads which exhibit FGOP, the speedup from FGOP specialization is 4.4× (large size). REVEL’s dataflow/vector-stream model provides the other 2.6× speedup over the DSP. The performance trade-offs here are similar, except the advantage of parallelizing across lanes is diminished due to data-parallel execution.

The vector-stream control and FGOP-exploitation enables combined order-of-magnitude speedups.

Q3. Why does exploiting FGOP help REVEL?: Figure 18 overviews REVEL’s cycle-level behavior, normalized to non-FGOP hardware. Latency-optimized workloads are labeled as “multi”. To explain the categories, issue and multi-issue means that one or multiple dedicated dataflow fired, and temporal means only a temporal dataflow fired during that cycle. All other categories represent overhead, including the drain of the dedicated fabric, scr-b/w and scr-barrier for bandwidth and synchronization, stream-dpd for waiting on dependences, and ctrl-ovhd for waiting on the control core.

The clearest trend is that exploiting FGOP reduces the control overhead for both small and large matrix sizes. Also, exploiting FGOP enables parallelism between dataflows, which can be seen in the multi-issued category, especially prevalent for the larger matrix sizes of FGOP kernels.

Exploiting FGOP increases parallelism and reduces control overhead, enabling higher hardware utilization.

Q4. What is the impact of each mechanism?: Figure 19 shows the incremental speedup of each hardware/software feature (so 5 versions of each kernel). Latency-optimized versions have “lat” as a suffix.

The inductive benefit is small alone, as it reduces control but does not increase parallelism. Only FFT benefits greatly by using inductive reuse to reduce SAPD bandwidth. Most workloads were accelerated dramatically from exploiting fine-grain dependences. However, QR and SVD have complex sub-critical regions, so they only see the benefit after adding the heterogeneous fabric. Throughput-optimized QR suffers from local memory access because of the shrinking matrix sizes, but latency-optimized QR converts these to inter-lane data streams. Solver is also accelerated by the heterogeneous fabric because it is latency sensitive, and collapsing sub-critical instructions can reduce latency. Cholesky’s triangular access implies large gains from implicit vector masking.

REVEL’s mechanisms together enable high performance.

Q5. What is the biggest remaining overhead for REVEL?: As shown in Figure 18, this is the drain time on smaller workloads, often caused by reconfiguration. This is more of an issue for the smaller matrices and especially FFT, where the datapath should be reconfigured for each algorithm phase. REVEL’s reliance on deep pipelines causes config/serialization penalty on extremely short phases.

Q6. What are the sources of area and power?: Table 6 shows the breakdown; the largest source (especially power) comes mostly from the floating point units. At 28nm, REVEL is 1.79mm². Note that the control core is now only about one 50th of the overall area.

Q7. Does REVEL have better perf/mm²?: REVEL’s high speedup with only small area overhead (over the DSP) for the computation fabric’s networks results in a large performance/mm² advantage: 1308× over the OOO core and 8.3× over the DSP.

Q8. How sensitive is REVEL’s performance to the size of the temporal region?: Because temporal tiles cost more than 5× the area than dedicated tiles (dedicated tile: 2265μm², temporal tile: 12062μm²), it is important to
choose the correct temporal region size. Figure 20 shows REVEL’s performance sensitivity to this size, as well as the area tradeoff. SVD and QR have the largest regions, so are affected the most, but a $1 \times 1$ temporal region only has 13% overhead. We choose this size to minimize area penalty.

**Q9. Do we require a heterogeneous fabric?** To create a purely dedicated fabric, we would have had to support 52 additional dedicated tiles for our largest temporal region in SVD, costing about 2.75× fabric area. Similarly, for the entire design to be temporal, it would have cost around 2.5× fabric area. A heterogeneous fabric provides the best performance/area ratio.

**Q10. Would even more complex inductive streams have reduced control overhead?** Our analysis so far has shown that using 2D inductive streams can reduce control overhead and improve performance significantly. An interesting question is whether supporting higher dimension stream-access could have helped further.

To analyze stream capabilities analytically, we implement a static compiler analysis in LLVM [17], using scalar evolution analysis [46] for the closed-form representation of address patterns and loop termination with respect to induction variables. This analysis can determine the length of a given stream for each variable. Figure 21 shows the average length of a stream: the number of loop iterations the pattern describes. We also calculate the number of effective memory instructions per inner-loop iteration, “Mem. Insts/Iter”, which is a measure of the control overhead (Figure 22). We consider vector (V), 1D streams (R), 2D streams (RR and inductive RI) and 3D streams (RRR and inductive RII).

Regular workloads like GEMM require only a low dimension rectangular access pattern for a long length. However, FGOP workloads show much higher lengths only with inductive access capability (RI or RII capability). This benefit translates to fewer memory instructions per-iteration. A value of less than 1 in Figure 22 means that fewer than one control instructions would need to be issued per cycle. This helps to explain why vector instructions alone are insufficient for parallelism – because they require too much specification of work. Fortunately, the RI capability always either achieves a control overhead below 1 inst/iter or matches the least overhead capability.

The ability to reuse stream values as part of the stream definition can also reduce control overhead. The control overhead if this feature is disabled is shown by the stacked bar in Figure 22. This benefit is modest; the more important reason for stream-reuse is to reduce memory bandwidth.

2D Induction streams (RI) are necessary to reduce control overhead, and RII may provide only a small energy advantage, but is also more complex.

**Q11. How competitive is REVEL with custom ASICs?** Table 6 shows the performance-normalized power and area overhead, as compared to ASIC analytical models. REVEL is mean 2.2× power. This is mostly due to the control logic (vector ports, bus, and etc.) and reconfigurable networks. It is 0.55× the area of the combined ASIC. Note this is highly optimistic for ASICs, as the performance model assumes perfect pipelining, and the power model assumes no control.

![Figure 20: Temporal region sensitivity (width × height)](image)

![Figure 21: Stream-type Access Length Comparison](image)

![Figure 22: Control overhead of various Capabilities measured in control instructions per iteration. The stacked bar indicates additional control overhead if stream-reuse technique is disabled.](image)

### 11. RELATED WORK

**DSP Accelerators:** Many application/domain-specific reconfigurable designs have targeted DSP algorithms. Fasthuber et al. [47] outline the basic approaches. One representative example includes LAC [48], targeted at matrix factorization.

**Ordered Parallelism and Synchronization:** A conceptually similar work to ours from the GPGPU space is dMT-CGRA [49], which proposes inter-thread communication between SIMT threads [50, 51]. Prabhaker et al. [52] develops “nested-parallelism,” which enables coupling of datap-
aths with different nesting of parallel patterns. Swarm [53] also targets a form of ordered parallelism by building abstractions on top of a task-parallel model, targeting irregular data-dependent parallelism [54].

**Task-parallel Acceleration:** An alternative model to ours is task-based parallelism plus some form of acceleration to reduce the synchronization overhead (eg. TAPAS [55]). Task parallelism has the benefit of dynamic load balancing, but this does not appear to be necessary for our DSP workloads.

**Flexible Vectorization:** Our vector-stream control paradigm is inspired by prior techniques which marshal independent execution lanes to create a vector-like execution when useful. This includes Vector-Threading [26, 25], Vector-Lane Threading [27], and Loop-Task Accelerators [56]. REVEL also marshals lanes to reduce control and increase parallelism, but its lanes are autonomous once programmed with streams.

Some techniques apply vectorization with reconfigurability, eg. Libra [57] and DySER [6], which can create/reconfigure vector lanes. REVEL also amortizes control through time.

**Stream-based ISAs:** Several prior architectures have stream primitives. We list their address capability as compared to REVEL on the right. We believe REVEL is the only one to support inductive patterns.

| Address Gen Capability | Name | Type |
|------------------------|------|------|
| Imagine [19]           | R    |
| Q100 [21]              | R    |
| Accel DMA [58]         | R    |
| Softtrain [2]          | RR   |
| RSVP [20]              | RR   |
| CorAM++ [22]           | RR   |
| APMC [23]              | RRR  |
| REVEL                  | RI   |
| FPCA [24]              | RRR  |

12. DISCUSSION AND CONCLUSION

This paper identified fine-grain ordered parallelism as a common property across a variety of linear-algebra and DSP algorithms. It is extremely difficult to take advantage of using existing VonNeumann Vector and multi-threading architectures. This work identified a set of abstractions and developed an execution model and hardware implementation (REVEL) which could exploit this form of parallelism.

Our REVEL implementation was more than an order of magnitude lower latency (10×-17×), and its performance per mm² was 6.7× that of a DSP (up to 16×). Overall, REVEL’s design offers large advantages over existing architectures for important signal processing workloads, and is a promising alternative to existing DSPs and beyond.

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