I. INTRODUCTION

Recently, the demand for military or civilian drones and surveillance radars has been increasing. In radar transceivers, several forms of waves are used to determine object distance and velocity information, of which continuous wave (CW) and frequency modulated continuous wave (FMCW) are typically used [1]-[3]. If CW is used, the speed of the object can be determined but not the distance. When using FMCW, both the distance and speed of the object can be determined, but when there are multiple targets, a ghost target is created.

To solve this problem, FMCW and CW can be used together to verify the distance and speed information of multiple targets without a ghost target [2]. For CW, the Doppler frequency is added to the carrier frequency and received by the receiver, whereas for FMCW, the additional beat frequency, as well as the Doppler frequency, is received; therefore, for each case, the sampling rate required by the analog-to-digital converter (ADC) is different. If the sampling rate is high, it is advantageous that the switch size is large and the capacitor size is small. However, if the sampling rate is low, it is advantageous that the size of the capacitor is large, and the size of the switch is small, considering the charge injection and clock feed-through. Therefore, this work proposes a design that uses different sample-and-hold circuits when using FMCW and CW.

In ADC, the sample-and-hold circuit, and the capacitive digital-to-analog converter (CDAC) are mainly used together. That is, the CDAC acts as a capacitor for the sample and hold circuits. However, in the case of CDAC, the small design of unit capacitors will have a negative impact on performance because matching characteristics have a very large impact on linearity.

Eq. (1) represents the resistance of the switch when the switch
is designed as NMOS, as shown in Fig. 1, and Eq. (2) shows the error in the output of the sample-and-hold considering the charge injection.

\[
R_{ON} = \frac{1}{(\mu_n C_{ox} W / L)(V_{GS} - V_{TH})} 
\]

\[
\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_H} 
\]

Eq. (1) and Eq. (2) show that there is a trade-off relationship between \(R_{ON}\) and charge injection, depending on the size of the switch [4]. Fig. 2 shows the spurios free dynamic range (SFDR) according to the input frequency and size of the CMOS switch. The sampling rate is based on Nyquist sampling. If the sampling rate is high, the larger switch provides a higher signal-to-noise distortion ratio (SNDR), and if the sampling rate is low, the smaller switch provides a higher SNDR.

Therefore, in this work, when using FMCW, the switch’s clock was bootstrapped, and the sampling capacitor was used separately. When using CW, a small switch was used, and CDAC was designed to act as a capacitor for the sample-and-hold circuits.

Further, the DC offset of ADC, which causes errors in distance or speed, is eliminated primarily by signal processing in DSPs; however, in this work, we designed circuits that calibrate offset in analog-integrated circuits. In general, offset calibration in the comparator includes auto-zeroing [5], which is a method of sampling offset charge, or a method of compensating \(V_{th}\) mismatch by changing the body voltage on both sides of the input MOSFET through a charge pump and phase detector [6].

However, in the case of auto-zeroing, the SAR ADC requires a preamp with a high gain, which slows the ADC’s operating speed. The disadvantage of changing body voltage is that if the offset is too large, too much change in body voltage can lead to leakage from the body to the source or body to drain, and the addition of a switch used in offset calibration mode slows the capacitor down. To overcome these shortcomings, this paper calibrates offset using a method of changing \(V_{ref}\)

The remainder of this paper is organized as follows: Section II describes the structure of the proposed ADC and the description of each block, Section III describes the simulation results, and Section IV concludes this paper.

II. ARCHITECTURE AND CIRCUIT DESCRIPTION

Fig. 3 shows the block diagram of the SAR ADC. First, in the offset calibration phase, the SAR control logic does not work, and the offset of the comparator is calibrated. As shown in Eq. (3), the offset can be reduced if the input MOSFET is large [7].

\[
V_{offset} = \left(\frac{(V_{in} - V_{th})}{2} + \frac{W}{L} \left(\frac{\Delta V}{L_{th}}\right)\right)^2 + \left(\frac{(V_{in} - V_{th})}{2} + \frac{W}{L} \left(\frac{\Delta V}{L_{th}}\right)\right)^2 
\]

However, there are two disadvantages to designing an input MOSFET large. First, the kickback noise caused by the clock of the comparator increases. Second, the CDAC produces a gain error equal to \(C_S/(C_S + C_P)\). In particular, the size of the sampling capacitor used in the FMCW mode was smaller in this work, which is more fatal. Therefore, the size of the input MOSFET is designed to be calibrated instead of the small size of the input MOSFET designed to be calibrated.
In the A/D conversion phase, the offset calibration logic does not work, and the differential input signal enters two paths, and the magnitude of the output voltage at paths 1 and 2 determines the output of the comparator. In the FMCW mode, the input enters path 1, and the input switch in path 2 is designed to always be open. At this point, the sampled input in path 1 is output, and at path 2, the voltage that is feedback through the comparator, control logic, and CDAC is output. Conversely, in the CW mode, the input enters path 2, the input switch in path 1 is always open, and the output of path 1 is always designed to be common-mode voltage (V_{CM}). In path 2, the sampled input and the voltage from the CDAC are added to the output. In both paths 1 and 2, input is sampled using the bottom plate sampling technique, in CDAC in path 2, V_{CM} based switching is used to reduce area and energy consumption, and a bridge capacitor is used. Further, in path 1, the switch uses a bootstrap circuit to sample fast inputs, and in path 2, a transmission gate switch with a simpler structure and less power consumption than the bootstrap circuit is used because it does not sample fast inputs.

Fig. 4 shows a schematic of the bootstrap circuit. In the track-and-hold circuit, the sampling speed is determined by the value of the R_{on} of the MOSFET and the value of the sampling capacitor. If only a simple NMOS is used as a switch, it causes nonlinearity that changes V_{th} according to V_{in}. However, the use of bootstraps can prevent R_{on}'s value from changing as V_{in} changes by fixing the value of V_{gs} [8]. However, as shown in Eq. (4), the change in V_{th} caused by the body effect follows the change in V_{in}.

\[
V_{th} = V_{th0} + \gamma(\sqrt{2\Phi_{F}} + V_{sb} - \sqrt{2\Phi_{F}})
\] (4)

The change in V_{in} causes a change in R_{on} and a change in charge injection [9]. To prevent the V_{th} from changing due to the body effect, the body is connected to the V_{in} during the sampling phase. In the hold phase, the body is connected to the ground to prevent leakage from the body to the output.

Fig. 5 is a schematic of the comparator designed with 4 inputs based on a double tail current comparator [10]. The double-tail current comparator is more advantageous than the commonly used strong-arm latch in terms of current consumption, delay, and offset compared to the commonly used strong-arm latch.

Fig. 6 shows a circuit diagram of the CDAC. V_{CM}-based switching technique is used to reduce the area and switch energy consumption, and the total area is greatly reduced using bridge capacitors [11]. The size of the bridge capacitor is equal to that of the unit capacitor.

Fig. 7 shows a block diagram of the offset calibration. We propose a method for offset calibration by controlling the reference voltage according to the output result of the comparator in the offset calibration phase. If offset is present, the action is to bring the values of V_{refp} close to V_{refp} + V_{offset}, as shown in Fig. 8.

Fig. 9(a) shows a circuit diagram of the offset control logic, and Fig. 9(b) shows a circuit diagram of the reference voltage.
Fig. 7. Block diagram of offset calibration.

Fig. 8. Flowchart of offset calibration.

Fig. 9. (a) Offset control logic; (b) reference voltage with switch.

Fig. 10. Calibrated offset using \( V_{\text{ref}} \) change.

Fig. 11. Monte Carlo simulation results.

Before and after calibration, a Monte–Carlo simulation was carried out to check the offset of the capacitor. As shown in Fig. 11, the offset of the comparator before calibration was \(-46\) mV and \(50\) mV in the worst case. By contrast, after calibration, the offset was \(-4\) mV and \(4\) mV in the worst case. Table 1 compares offsets before and after calibration.

### Table 1. Offset statics without and with calibration.

|                  | Before calibration | After calibration |
|------------------|--------------------|-------------------|
| Mean of Absolute offset [mV] | 14.78              | 1.54              |
| Min offset [mV]  | -46                | -4                |
| Max offset [mV]  | 50                 | 4                 |

### III. SIMULATION RESULT

Fig. 12 shows the results of the fast Fourier transform (FFT) simulation of the designed ADC. This result is a pre-simulation result, but a capacitance of 5fF was applied to the intermediate node of each block in consideration of the value of parasitic capacitance that may occur during the layout. Fig. 12(a) is
obtained when the input enters path 1, and the input frequency is determined to be close to 10 MHz, considering coherent sampling. Fig. 12(b) shows that the input enters path 2, and the input frequency is similarly determined to be around 50 kHz, considering coherent sampling. Simulation results show that if the input enters path 1, it obtains an SFDR of 64.62 dB, an SNDR of 57.35 dB, and an effective number of bits (ENOB) of 9.23 bits. Power consumption is 0.3481 mW, and FOM is 28.9 fJ/Conv-Step. If the input enters path 2, it obtains an SFDR of 60.53 dB, an SNDR of 55.76 dB, and an ENOB of 8.97 bits. Power consumption is 1.72 μW and FOM is 34.2 fJ/Conv-Step.

Tables 2 and 3 compare performance with other works [12]-[17]. As shown in the tables, the ADC proposed in this work uses two different input paths according to the input frequencies, so it does not degrade the SNDR or SFDR compared to ADCs with different sampling rates.

**IV. CONCLUSION**

This paper shows the design results in the TSMC 65 nm process and uses a supply voltage of 1.2 V. We designed a suitable SAR ADC for multimode radar transceivers. In both modes, inputs are designed to fit in different paths, both with a resolution of 10 bits. The ADC was designed to operate at sampling rates of 20 MS/s and 100 KS/s, respectively, and when Nyquist sampling was performed, path 1 obtained an SFDR of 64.62 dB, an SNDR of 57.35 dB, and an ENOB of 9.23 bits. Power consumption was 0.3481 mW, and FOM was 28.9 fJ/Conv-Step. In the case of path 2, SFDR was 60.53 dB, SNDR was 55.76 dB, ENOB was 8.97 bits, power consumption was 1.72 μW and FOM was 34.2 fJ/Conv-Step. The design also configured a
circuit for offset calibration of the comparator to reduce the offset from -46 mV/+50 mV to -4/+4 mV in the worst case.

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