Research on a Novel DC Circuit Breaker Based on Artificial Current Zero-Crossing

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ABSTRACT Modular multilevel converter-based high voltage direct-current (MMC-HVDC) transmission has developed rapidly because of its flexibility, reliability and efficiency. DC circuit breaker (DCCB) is one of the key equipments to ensure the safe and stable operation of MMC-HVDC power grids. In this paper, we investigate a novel topology of DC circuit breaker based on artificial current zero-crossing. The proposed DC circuit breaker can effectively limit the magnitude and rise rate of fault current at the converter station side and reduce the impact of DC fault on the converter devices. The principle and operation sequence of this topology are described. Meanwhile, the breaking process of the DC fault is analyzed theoretically and the considerations for parameter design are presented. Finally, the system model of DC circuit breaker and a four-terminal MMC-HVDC test system are built in PSCAD/EMTDC. The simulation results show that the proposed DC circuit breaker is effective for quick breaking after fault.

INDEX TERMS DC circuit breaker, novel topology, artificial current zero-crossing, short circuit fault, bidirectional current breaking, MMC-HVDC.

I. INTRODUCTION

MMC-HVDC power transmission technology based on power electronics is widely used in power supply and grids and has become the focus of research. MMC-HVDC technology has great advantages in renewable energy grid-connected, distributed generation grid-connected, island power supply, urban distribution network power supply, etc. Especially in recent years, the number of MMC-HVDC transmission projects has been increasing, which has proved that MMC-HVDC transmission has its feasibility and superiority in technology and engineering [1]–[5].

However, the DC fault which leads to serious overcurrent is still a major challenge in HVDC grids realization and development [6]. Till now, only using DC circuit breakers can achieve the required fast and flexible fault isolation without voltage collapse, and maintain normal operations of non-fault areas in HVDC grids. The technology of DC circuit breaker has been extensively studied in academic and industrial fields at home and abroad [7], [8]. In the previous researches, DC circuit breakers can be categorized into three types: mechanical DCCBs (MCBs), solid-state DCCBs (SSCBs), and hybrid DCCBs (HCBs) [8]–[12]. Among them, the solid-state DCCBs use semiconductors with turn-off ability, such as Insulated-gate bipolar transistors (IGBTs) and Integrated gate commutated thyristors (IGCTs), and attain very fast operational speed [13]–[15]. Although SSCBs have the most satisfactory operational speed for interrupting currents, consisting of massive semiconductors causes high conduction losses and high cost. The MCBs do not have enough fast fault current interruption capability [8], [11].

The hybrid DCCBs combine the advantages of mechanical DCCBs and solid-state DCCBs, which makes HCBs be preferable [8], [13], [16]–[18]. ABB developed a structure of HCB that contains a main DC breaker (MB) and a bypass formed by an auxiliary DC breaker in series with a fast mechanical disconnector [13]. The MB is composed of many IGBTs to withstand the transient overvoltage and serious fault current. The State Grid Corporation of China also proposed a full-bridge based HCB, which is also an IGBT-based hybrid
DCCB and has been used in Zhangbei MMC-HVDC engineering project [19]–[21]. Recently, various topologies of hybrid DC circuit breakers have been proposed [22]–[30], and most of these topologies have common features: The fault current cannot be effectively limited, a large amount of fault energies will be dissipated by the surge arrester, and high cost of full-controlled semiconductors. In other words, these DCCB must have enough fault interruption capability, the converters near the fault must withstand serious overcurrent, and the design of surge arrester in DCCB becomes particularly critical.

Thyristors are superior to IGBTs or IGCTs in terms of cost, rating parameters, and reliability [25]. Therefore, to overcome these shortcomings mentioned above, a novel type of DC circuit breaker based on artificial current zero-crossing is proposed in this paper. The proposed DCCB is based on thyristors, and has the advantages of effectively limiting fault current, fast reclosing, without full-controlled semiconductors and no additional pre-charging power supply. It can be better applied in HVDC grids. Section II details the basic structure and working principle of the proposed DC circuit breaker. The working process and considerations for parameter design are analyzed mathematically in section III. By establishing the model of DC circuit breaker and a multi-terminal test system in section IV and V, the fault current breaking simulation is carried out to validate the feasibility and effectiveness of this topology.

![Figure 1. Topology of the novel DC circuit breaker based on artificial current zero-crossing.](image)

**II. TOPOLOGY STRUCTURE AND WORKING PRINCIPLE**

**A. TOPOLOGY STRUCTURE**

The proposed topology of DC circuit breaker are shown in Fig. 1, which is composed of ultrafast mechanical switch (K), anti-parallel thyristor strings (T_K), inductors (L_1, L_2, L_0), mechanical switches (K_1, K_2), diode strings (D_1, D_2), thyristor strings (T_1, T_2), mechanical switches (S_1, S_2), capacitors (C_1, C_2), and fast charging branches.

D_1 and T_1 are anti-parallel connected, and then in series with S_1 and C_1 to form a commutation branch; similarly, another commutation branch is composed of D_2, T_2, S_2, and C_2. The two fast charging branches consist of charging resistors (r_1, r_2) and charging thyristors (T_{r1}, T_{r2}). T_K is parallel connected with the ultrafast mechanical switch. Capacitors have individual paralleled surge arresters.

In Fig. 1, i_{dc}, i_K, i_{T_K}, i_f are the current of converter side, the current of ultrafast mechanical switch, the current of T_K, and the fault current of line side, respectively. I_u is the threshold of fault current detection; u_{C1}, i_{C1}, u_{C2}, i_{C2} are corresponding capacitors’ voltage and current; u_K is the voltage of K, the total voltage of K and L_0 (i.e., the difference value between u_{C1} and u_{C2}) is recorded as u.

**B. OPERATION PRINCIPLES**

The proposed DCCB has three basic operation modes: normal conduction mode, fault current interruption mode and breaker reclosing mode. Because of its symmetry, we take the current direction and the fault location shown in Fig.1 as an example to clarify the operation principle in this paper.

1. Normal conduction mode: When the whole HVDC system prepares to start up, the switch K_1 and K_2 should be closed. After turning on thyristors T_{r1} and T_{r2}, the system begins to pre-charge capacitors C_1 and C_2, the charging process can be done through charging resistors (r_1, r_2) upon energization of the DC bus side. After C_1 and C_2 are charged up to the system voltage level the charge current decreases gradually. The thyristors turn off naturally after the charge current falls below the holding current, and then close the mechanical switches S_1 and S_2. Considering the influence of charging current on DC system, the capacitors will be charged from zero to the system voltage in tens of milliseconds with parameters designed of charging resistors. In most of the working time of DCCB, the load current flows through the following path: K_1 - L_1 - K - L_0 - L_2 - K_2.

2. Fault current interruption mode: The proposed topology has bidirectional interruption capability. We take a fault location shown in Fig.1 as an example, the following paragraphs will describe how to clear the fault current.

Assume that the short circuit fault occurs at t_0, the fault current rises rapidly and reaches the threshold value I_u at t_1. Then, the control system sends the action command to the DCCB. The thyristor T_{r1} is triggered and K is controlled to open at the same time. The capacitor C_1 starts discharging to the fault line and feeds the fault point, which provides most of the fault current. Therefore, the amplitude and rise rate of the current at the converter side are limited, in addition, reducing the impact of the fault current on the converter station. After the short mechanical delay of K, the contacts begin to separate at t_2, resulting in arc immediately, and the distance between contacts increases gradually. After the preset arcing time, at t_3, the thyristor string in T_K whose direction is opposite to i_K is turned on and thyristor T_2 is triggered, C_2 starts to discharge. Under the resonance of C_2 and L_0, the resonant current injects into switch K branch, which makes i_K decrease immediately, meanwhile, C_1 is charged. At t_4, i_K becomes zero, the resonant current continues to...
flow through $T_K$, which provides enough time for $K$ to extinguish arc and ensure the recovery of dielectric insulation, therefore, the arc extinguishes and $K$ breaks completely. At $t_5$, the $T_K$ turns off while the direction of resonant current reverses, thus, the converter is isolated from the DC fault.

After $t_5$, the current $i_{dc}$ starts to charge $C_1$ through diode $D_1$; $C_2$ forms a continuous current loop with the fault point. The current $i_{dc}$ decreases gradually during the resonant process. At $t_6$, $i_{dc}$ drops to zero, $D_1$ and $T_1$ all turn off. At $t_6$, $C_2$ completes charge and $i_f$ drops to zero, $D_2$ and $T_2$ all turn off. When $i_{dc}$ and $i_f$ all become zero, which indicates that the DC fault current is completely cleared.

3. Breaker reclosing mode: After fault breaking, the fault transmission line needs de-ionization to restore insulation. The time interval of de-ionization is about 300 ms \[7\], \[31\], \[32\]. DC circuit breaker used in MMC-HVDC system should have the ability of reclosing and re-breaking after the first breaking interval of 300 ms. The prerequisite of fault current breaking is the capacitors pre-charged. When fault resistance is several-tens of ohms, or even several hundred ohms, the voltage of $C_2$ may be lower than $U_{dc}$ after fault breaking, so $C_2$ must be recharged quickly before reclosing operation (if the fault located on the left side of the DCCB, $C_1$ must be recharged). After the first break, $K_2$ and $S_2$ are controlled to open, closing $K$ and turning on $T_r2$ to charge $C_2$ up to the rated DC voltage level quickly through $r_2$. After $T_r2$ turns off naturally, $S_2$ is controlled to close. We can control the charging current and charging time by designing $r_2$, and the recharging process can be completed before reclosing.

In order to avoid reclosing dccb under fault situation, the proposed dccb has an additional function that we can choose to test the fault before reclosing. The strategy is as follows: first, triggering thyristor $T_2$. If $C_2$ is detected to have very small discharge current due to the characteristics of transmission line distribution parameters, the short circuit fault does not exist, then the reclosing operation can be carried out. If $C_2$ has a large discharge current, it shows that there is still a short circuit fault, stop reclosing and after a set time, triggering $T_2$ again for testing. If the fault still exists, we can judge the fault as a permanent fault and conduct repair.

III. THEORETICAL ANALYSIS AND DESIGN CONSIDERATIONS

This section will focus on analyzing the breaker’s equivalent process and parameter design considerations.

The overhead lines’ failure rate will be much higher than dc cables. In this paper, we take overhead lines as an example, and overhead lines can be represented to simplified R-L series models \[33\]–\[35\].

In the whole process of DCCB isolating faults, it is better that the breaker can avoid converter blocking to maintain the power transmission of the healthy area. we take the half-bridge MMC (HB-MMC) converter as an example, the analysis is carried out under the condition that the converter submodules (SMs) will not be blocked. HB-MMC can be equivalent to a discharge circuit consists of a capacitance $C_S$, a reactance $L_s$, and a resistance $R_s$ in series during the fault process \[36\]–\[38\]. And $C_s = 6 C_m/N$, $L_s = 2 L_m/3$, $R_s = 2R_m/3$, where $N$ is the number of SMs in each arm, $C_m$ is the SM capacitor, $L_m$ and $R_m$ are the inductance and resistance in each arm, respectively \[34\], \[39\], \[40\].

FIGURE 2. Equivalent circuits of different periods in the fault current breaking.

The equivalent circuits of short circuit fault breaking process are shown in Fig. 2. The fault occurs at $t_0$. $i_{dc}$ is the normal steady-state DC system current before fault. $U_{dc}$ is the...
initial steady-state voltage of 
\( C_s \), also represents the rated DC
 bus voltage. The following four stages describe the isolation
process of the line fault.

A. \( t_0 \sim t_1 \)

After fault occurs, inductors limit fault current immediately.
The fault current is fed by the DC system. As shown in Fig.
2(a), the circuit equation can be expressed as follows:

\[
(L_1' + L_2' + L_L) \frac{d^2u_{C_s}}{dt^2} + (R_s + R') \frac{du_{C_s}}{dt} + u_{C_s} = 0
\]

\[
 i_f(t_0) = i_{dc}(t_0) = I_{dc}, \quad u_{C_s}(t_0) = U_{dc}
\]

We can obtain the expression of fault current as follows:

\[
u_{C_s}(t) = \left[ -\frac{L_f}{C_s} - p_2U_{dc} \right] e^{p_1(t-t_0)}
\]

\[
\frac{p_1 - p_2}{1 - p_2} + \frac{L_f C_s + p_1 U_{dc}}{1 - p_2} e^{p_2(t-t_0)}
\]

where

\[
L_1' = L_1 + L_a, L_2' = L_2 + L_2', R' = R_L + R_f, p_1 \text{ and } p_2
\]

are

\[
\pm \sqrt{\left( \frac{R_s + R'}{2(L_1 + L_2 + L_L)} \right)^2 - \frac{1}{(L_1 + L_2 + L_L)C_s}}, R_L \text{ and } L_L \text{ are equivalent resistance and inductance of transmission line respectively, and } R_f \text{ is fault resistance.}
\]

B. \( t_1 \sim t_3 \)

The equivalent circuit is shown in Fig. 2(B), turning on \( T_1 \)
and open switch \( K \) at \( t_1 \), \( C_1 \) discharges to contribute most of
the fault current which can prevent the DC bus voltage from
collapsing.

According to laplace transform and node-voltage method, we can obtain:

\[
U_1(s) = \frac{u_{C_1}(t)}{s^3 + k_0 s^2 + k_1 s + k_2}
\]

where

\[
u_{C_1}(t) = U_{dc}, i_f(t) = I_a, L_2'' = L_2' + L_L,
\]

\[
k_0 = \frac{R_s}{L_1'} + \frac{R''}{L_2'}, k_1 = \frac{R_s R' + (R'' L_1' - R'' L_2')}{L_1' L_2''} i_f(t_1) + u_{C_1}(t_1) L_2'' + \frac{1}{L_1'C_s}, k_2 = \frac{R'' C_1}{L_1' L_2'' C_1 u_{C_1}(t_1)} + \frac{R'}{L_1' L_2'' C_1} i_f(t_1)
\]

\[
k_3 = \frac{R_s R'' + L_2'' + L_2'}{L_1' L_2'' C_1} + \frac{1}{L_1'C_s}, k_4 = \frac{R_s + R'}{L_1' L_2'' C_1} + \frac{R'}{L_1' L_2'' C_1}, k_5 = \frac{R_s}{L_1' L_2'' C_1}
\]

\[
U_1(s) = u_{C_1}(s), \text{ and then we can deduce the Laplacian expression of the current } i_K \text{ at this stage as follows:}
\]

\[
i_K(s) = i_f(s) = \frac{U_1(s)}{L_2'' + R'}
\]

The inverse Laplace transform of \( i_K(s), i_{dc}(s), u_{C_1}(s), u_{C_2}(s) \) can be solved by using MATLAB, so their corresponding

time domain solutions can be obtained.

C. \( t_3 \sim t_5 \)

As shown in Fig. 2(c), after the preset arcing time, the contacts
of \( K \) have reached a safe distance. At \( t_3 \), the discharge current of the capacitor \( C_2 \) injects into switch \( K \) in reverse
direction.

We know that the current expression of LC resonance is:

\[
i = U_C \left[ \frac{\sqrt{C_s}}{L} \sin\left( \frac{t}{\sqrt{LC}} \right) \right]
\]

where \( U_C \) is the initial voltage value of the capacitor.

In the equivalent circuit of this stage, the resonance of \( C_2-L_0-C_1 \)
is superimposed on \( K \). The value of \( L_0 \) is much smaller than \( L_1 \) and \( L_2 \). The resonant frequency of \( C_2-L_0 \)
is high and the amplitude of resonant current is very large, so the zero-crossing time of \( i_k \) is very short. In order to

simplify the analysis, the resonant current injected into \( K \) can be approximately given by:

\[
i_{C_2} = \Delta U_C \left[ \frac{\sqrt{C_s}}{L_0} \sin\left( \frac{t - t_3}{\sqrt{L_0 C_2}} \right) \right]
\]

where \( \Delta U_C \) is the differential voltage value between \( u_{C_2}(t_3) \) and \( u_{C_1}(t_3) \), and \( u_{C_2}(t_3) = U_{dc} \). From (8), the time of zero-crossing of \( i_k \) can be approximately obtained:

\[
\left\{ \begin{array}{c}
i_k(t) = i_{C_2}(t) \\
i_k\left( \frac{\pi}{2} \sqrt{L_0 C_2} + t_3 \right) = \Delta U_C \left[ \frac{\sqrt{C_s}}{L_0} \right]
\end{array} \right.
\]

According to Laplace transform and node-voltage method, we can obtain:

\[
u_{C_2}(s) = \frac{U_{dc}}{s^3 + \left( \frac{1}{L_0 C_2} + \frac{u_{C_1}(t_3)}{L_0 U_{dc}} \right)}
\]

So, \( u_{C_2}(t) \) and \( u_{C_1}(t) \) can be further derived.

D. AFTER \( t_5 \)

After \( t_5 \), \( K \) has opened and \( T_K \) has turned off, the current of
converter side charges \( C_1 \), meanwhile, \( C_2 \) discharges through
\( L_2 \) to the fault point. As shown in Fig. 2(d).

According to Laplace transform and loop current method for circuit of
converter side, the following equation can be gotten:

\[
i_1(s) = \frac{u_{C_2}(t_5) - u_{C_1}(t_5)}{L_1's^2 + R_s s + \frac{1}{C_1} + \frac{1}{C_1'}}
\]

Hence, we can obtain \( u_{C_1}(t), i_{dc}(t), u_{C_2}(t) \) and other variables.

Furthermore, \( u_2(t) \) can be given by:

\[
u_{C_2}(t) = \frac{\left( -\frac{i_0}{C_2} - p_4 u_0 \right) e^{p_3(t-t_5)}}{p_3 - p_4} + \frac{\left( \frac{i_0}{C_2} + p_4 u_0 \right) e^{p_3(t-t_5)}}{p_3 - p_4}
\]
where \( u_0' = u_{c2}(t_5), i_0' = i_{c2}(t_5), \) \( p_3 \) and \( p_4 \) are
\[
R \left( \frac{R}{2(L_2+L_4)} \right)^2 - \frac{1}{(L_2+L_4)C_2} \]

The voltage across the switch \( K \) can be approximately given by:
\[
u_K(t) = u_{C1}(t) - u_{C2}(t) \quad (12)
\]

After both \( i_{dc} \) and \( i_f \) become zero, the fault breaking process ends. The MOVs of capacitor are used for voltage limiting protection, and the impedance characteristic is nonlinear. This paper will not discuss it.

In MMC-HVDC system, there are relatively large bridge arm inductance, and line impedance between fault point and DC circuit breaker. Therefore, the actual inductance of fault equivalent circuit is much larger than the inductance in DC circuit breaker. The design of inductor \( (L_1, L_2) \) should consider the maximum current \( I_{max} \) that DC system and DCCB can withstand, and the maximum fault detection time \( \Delta t \) for the fault with 0 km distance. Therefore, we have:
\[
L_1 + L_2 \geq \frac{U_{dc}\Delta t}{I_{max} - I_{dc}} \quad (13)
\]

The reasonable values of \( C_1, C_2 \) and \( L_0 \) can be obtained based on the theoretical calculation above and following design considerations: the maximum amplitude and zero-crossing time of converter side current \( (i_{dc}) \) must be limited; in order to ensure \( i_K \) can achieve zero-crossing, the maximum amplitude of resonant current provided by \( C_2-L_0-C_1 \) should be 1.3-2 times the amplitude of \( i_K \), and the resonant frequency should be several hundred Hz to several kHz [41]; the capacitor value of \( C_1 \) should not be too large because of its cost.

\[\text{FIGURE 3. Simplified simulation system model.}\]

IV. SIMULATION ANALYSIS OF FAULT BREAKING
This section aims to detail the performance of fault breaking, the simplified simulation system is depicted in fig. 3, according to the analysis in section III, the designed parameters of simulation system are as follows: \( U_{dc} = 500 \text{kV}, I_{dc} = 3 \text{kA}, N = 312, C_m = 15 \text{mF}, L_m = 100 \text{mH}, R_m = 0.3 \Omega \).

Ultrafast mechanical switch adopts vacuum switches, under the current research and development situation, the time to achieve the safe distance between contacts of switch k is set to 2 ms [6], [42], and the mechanical delay is set to 0.3 ms [43], [44]. \( L_1 = L_2 = 100 \text{mH}, L_0 = 2 \text{mH}, C_1 = C_2 = 100 \mu F. \)

Resistors \( r_1 \) and \( r_2 \) are 200 \( \Omega \), which can effectively control charging current and charging time.

The low-impedance \( (R_F = 1 \text{m}\Omega) \) pole-to-ground fault occurs at the connection between the DCCB and the transmission line (fault distance from DCCB to fault point is 0 km), which is the most serious fault for DCCB. The threshold current value \( I_0 \) is set to 1.5\( I_{dc} \).

Fig. 4 shows the main voltage and current waveforms of dccb. the short circuit fault occurs at \( t_0 = 0.2 \text{s} \). The fault current \( i_f \) rises rapidly and reaches 4.5 kA at \( t_1 = 0.201 \text{s} \), then, \( K \) is controlled to open and triggering \( T_1 \). Upon \( T_1 \) is turned on, \( C_1 \) discharges and effectively restricting the growth of \( i_{dc} \). At \( t_3 = 0.203 \text{s} \), turning on \( T_2 \) to discharge \( C_2 \), the reverse current injects into \( K \). Fig. 4(a) show the current of switch \( K \) without breaking, which aims to illustrate that the topology can produce reliable current zero-crossing in \( K \). At \( t_4 = 0.20328 \text{s} \), \( i_K \) becomes zero, and at \( t_5 = 0.20383 \text{s} \), \( i_K \) becomes zero. We can obtain that the thyristor \( T_K \) provides a period of more than 500 \( \mu \text{s} \) (between \( t_4 \) and \( t_5 \)) for \( K \) to recover its insulation with low voltage stress. Current of converter side (\( i_{dc} \)) drops to zero at \( t_6 = 0.210 \text{s} \) and line side current fault (\( i_f \)) becomes zero at \( t_7 = 0.2205 \text{s} \). So, the whole process of fault breaking is completed at \( t_7 \). In other words, the converter can be isolated from the DC fault within about 10 ms. Moreover, the fault can be completely cleared within approximately 20 ms after it occurs.

In addition, it can be seen that the converter side current \( i_{dc} \) begins to decrease within 4 ms after the fault is detected, which means the breaking time of the proposed DCCB is 4 ms. And its maximum value is only 4.92 kA, which effectively reduces the impact of DC fault on the converter station. The capacitors \( C_1 \) and \( C_2 \) are restored to the initial voltage. The maximum current of \( K \) is 13.6 kA and the maximum voltage across it is 2.4 times as much as \( U_{dc} \), which requires a high insulation ability. Therefore, the multi-switch combination structure should be used.

The DCCB proposed by State Grid Corporation of China can break fault in 3 ms, which will be used in Zhangbei HVDC grid. But, it’s maximum value of the fault current reaches about 13 kA with current limiting reactor of 200 mH, therefore, taking a certain design margin into consideration, MMC converter for Zhangbei is designed to withstand transient current of 100 ms up to 32 kA [21], [45]. A large number of IGBT and many technologies for improving breaking capability of IGBT are used, which leads to high costs. However, the maximum fault current of the proposed DCCB is 4.92 kA, which is less than 2 times the rated DC current. Thus, the design margin of IGBT and other related technologies can be reduced by more than half, and further reduce the cost of MMC converter stations.

According to the preceding scheme, reclosing can begin at 0.52 s. The opening of \( K_2 \) and \( S_2 \) will take a few milliseconds, then the recharge process of \( C_2 \) will begin. The voltage of \( C_2 \) under different fault resistance is shown in Fig. 5. It can be seen that the topology can quickly charge \( C_2 \) before reclosing, and has the ability of reclosing and re-breaking.
Taking $R_f = 1$ mΩ as an example, and reclosing operation begins. In case of the transient fault, the HVDC system will quickly enter the steady-state operation mode, and the line current will be restored, as shown in Fig. 6(a). However, in the case of the permanent fault, the DCCB can break fault again immediately after reclosing, the process of re-breaking...
In order to better illustrate the current limiting effect of the proposed DCCB, we built the simulation model of the abb-dccb [13], and compared the two DCCBs. Under the condition that the parameters of the simulation system are the same, we obtain the fault current waveforms at the converter station side of the two schemes in the process of dc line fault, as shown in Fig. 7. After the fault is detected, the ABB-DCCB starts to transfer fault current to the MB, then turn off MB after several milliseconds of fast mechanical disconnector break time. During the process, the fault current continues to increase until the MOV starts. The peak value of fault current $i_{dc}$ is 8.24 kA. However, once the fault is detected, the proposed DCCB starts to limit the current by discharging the capacitors, the maximum value is 4.92 kA. Therefore, the fault current $i_{dc}$ of the proposed DCCB is limited more quickly and greatly. It is obvious that the proposed DCCB has an effective current limiting capability.

V. SIMULATION RESULTS IN MULTI-TERMINAL HVDC SYSTEM

A. TEST SYSTEM

To evaluate the basic operational performance of the proposed DCCB in HVDC system, a four-terminal MMC-HVDC test model with a DC system voltage of 500 kV is built in PSCAD/EMTDC, as shown in Fig. 8. The test model adopts HB-MMC and integrate the proposed circuit breaker.
All overhead lines are modelled with the frequency-dependent model, and their lengths are shown in Fig. 8. MMC1 operated in a constant DC voltage control mode, other MMCs operate in constant active power control mode. A current limiting inductance of 200 mH is set at both ends of each line, which is integrated in the DC circuit breaker (i.e. $L_1$ and $L_2$). Parameters of the DCCB are as the same as in section IV.

B. RESULTS

In Fig. 8, a pole-to-ground fault f is occurs on the Line1 side of CB12 (i.e. the fault location was 0 km away from CB12) at $t = 3$ s.

The detailed currents in the CB12 simulation results are shown in Fig. 9(a), which indicates that the overall fault clearing time of the DCCB is 20.05 ms. The initial steady current amplitude of CB12 ($i_{dcCB12}$) is 1kA, and the threshold current value is 1.5 times of $i_{dcCB12}$. After the fault, the peak current of converter side (i.e. $i_{dcCB12}$) is 2.26 kA, and becomes zero at 3.0118 s. The withstand voltage of switch $K$ in CB12 is 1140 kV, as shown in Fig. 9(b).
The currents of each line in test system are as shown in Fig. 10(a). After the fault, the currents of each converter station stabilize again after a short period of oscillation fluctuation.

As shown in Fig. 10(b), the normal DC bus voltage of the system is 500 kV, when the DC fault happens, the DC voltage decreases sharply. Only the DC bus voltage of MMC1 and MMC2 fluctuates to a certain extent. After the fault is cleared, the DC bus voltage quickly restores to the system voltage, which avoids the voltage collapse of the DC bus.

In practical engineering, in order to protect converter valves, the converter’s IGBTs will be blocked when arm current exceeds a maximum threshold [46], [47]. From Fig. 10(c), it can be seen that the bridge arm current fluctuation of MMC1 is small and restores to normal quickly, which can effectively reduce the blocking probability of converter and keep the continuous operation of the healthy part of multi-terminal HVDC system.

VI. CONCLUSION
In view of the shortcomings of existing DC circuit breakers and the demands of MMC-HVDC transmission system, a new type of DC circuit breaker topology based on artificial current zero-crossing is proposed.

The unique advantages of the proposed DC circuit breaker are as follow: it can quickly limit the fault current on the side of the converter station, significantly reduce the impact of dc fault on the converter, reduce the design capacity of converter valves to a certain extent, reduce the blocking probability of converter, and reduce the cost. The clamping effect of capacitors can avoid voltage collapse of DC bus when short circuit fault occurs. It realizes fast reclosing and has the ability of identifying whether the faults are cleared before reclosing, which can avoid the effect of fault on DC system again.

Firstly, the operation principle of the topology is detailed, and the theoretical analysis of the working process is presented. Then, aiming at the demands of MMC-HVDC grids, the basic operational performance of DCCB is simulated and verified by PSCAD/EMTDC.

The topology scheme in this paper provides a new idea for the research of DC circuit breaker and has positive significance for the construction of HVDC power system. Future work will analyze the application of the proposed DC circuit breaker in different MMC-HVDC system structures and different fault types. In addition, a cost-benefit analysis will be investigated in order to confirm the economic feasibility of its application in meshed MMC-HVDC grids.

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