Design of Dual-energy Signal Acquisition and Driving Circuit for Logistics Park Based on CPLD

Jiao Ren, Shaohua Zhang
Zhejiang University Kunshan Innovation Center, Jiangsu Kunshan 215300, China

Abstract. With the increase of security and defense, the security inspection of logistics park has put forward high requirements, and the perspective imaging technology of truck has become the most important. In this design, a high-speed parallel programmable logic device CPLD and Verilog HDL language are used to design the driving circuit of the perspective imaging signal acquisition part of truck, which can not only realize high-speed signal acquisition, but also have high integration, high accuracy and strong anti-interference ability, and other characteristics. The simulation and experimental results show that the driving circuit can satisfy the requirements of high efficiency, high reliability and fast imaging for the perspective imaging technology of freight cars.

1. Introduction
With the increase of railway, civil aviation, port, postal security and investment, the huge road network and the concealment of freight vehicles will become more and more forbidden goods and other transportation channels. Therefore, the entry of transport vehicles loaded with dangerous chemicals and contraband into the logistics park seriously endangers the logistics park and social security, and the state issued three policies in 2012, 2015 and 2016, all of which put forward requirements for the security inspection of the logistics park. However, the traditional logistics industry only relies on small chartered aircraft to check small cargo and express delivery, and to check large cargo vehicles with greater hidden dangers, without technical equipment. For example, each cargo in the car passes through chartered aircraft alone, which greatly affects the efficiency of logistics park.

Therefore, the perspective imaging technology for freight cars is put forward, which has the characteristics of fast inspection, high efficiency, high reliability and small occupation of land. The dual-energy signal acquisition module developed in this design is an important part of the perspective imaging technology of freight cars. The acquisition module can quickly and accurately collect perspective image signals and transmit them to PC for data processing and image display.

In order to ensure that the dual-energy signal acquisition module can collect perspective signals quickly and stably, CPLD and Verilog HDL [1] are selected to realize the driving circuits of the peripherals of the dual-energy signal acquisition module. The device has the characteristics of high integration, high speed, good reliability and easy programming.
2. The overall structure design of driving circuit

The driving circuit of the dual-energy signal acquisition module mainly includes driving reference clock generation circuit, AD sampling driving circuit, channel switching circuit and range switching circuit. The specific block diagram is shown in Figure 1.

![Figure 1. Structural block diagram of signal acquisition driving circuit](image)

2.1. Design of Driving Circuit for Clock Module

Clock module is the benchmark of other driving circuit design, which needs to generate 500KHZ clock. The flow chart is shown in Figure 2.

![Figure 2. Design flow chart of reference clock driver](image)

2.2. Design of Driving Circuit for Range Switching Module

The module is mainly used to adjust the sampling value when the signal is too strong or too weak. When switching range is needed, the range switching module receives instructions to receive and switch the latest range value. The specific flow chart is shown in Figure 3.
2.3. Design of Driving Circuit for Channel Switching Module
The module needs to switch 32 channels in a circular way. The flow chart is shown in Figure 4.
2.4. Design of driving circuit for AD sampling module

The driver module uses high-speed sampling chip AD9826 to collect signals[2]. Because it needs to collect high-energy and low-energy signals at the same time, the 2-channel SHA Mode mode is chosen when designing the driver circuit. The specific timing is shown in Fig. 5.

**Figure 5. AD Sampling Drive Sequence Diagram**

In order to ensure the accuracy and synchronization of data output, it is necessary to design the driver strictly in accordance with the timing requirements. The flow chart of driving circuit design is shown in Figure 6.

**Figure 6. Flow chart of AD sampling driver circuit**
3. Simulation and results

3.1. Simulation
The waveform simulation tool of Quartus II 9.1 is used for simulation. After the driver circuit is compiled successfully, the input and output are matched to each pin of the chip, and then a waveform file with the suffix of VWF is created in the project. The input and output nodes are added to the waveform file, and the clock source of 50MHz is given to the CPLD. The file is compiled successfully, and the driving signals of each module are simulated as the waveform shown in Figure 7.

![Figure 7. Simulated waveform](image)

3.2. Measured results
In order to further verify the function of the design, EPM570T144C5 chip of MAXII series of Altera Company is selected as the core controller, and 50MHz external clock signal is used as the reference signal of CPLD, and other timing signals are generated on this basis. Fig. 8 and Fig. 9 respectively measure the driving sequence of the linear array Clk_M and AD9826 generated by CPLD on the oscilloscope.

![Figure 8. Clk_M waveform](image)  
![Figure 9. AD9826 clk waveform](image)

Compared with the measured waveforms and timing requirements of driving sequence, the actual output driving pulse of CPLD can satisfy the driving requirements very well. The driving circuit has high precision, fast speed and good reliability, which verifies the feasibility and correctness of the scheme.
4. Conclusion
Combining CPLD technology with Verilog HDL language, the driving circuit of dual-energy signal acquisition is designed, including sampling timing of AD9826, channel switching and range switching. After design input, compilation, and simulation, the generated driving circuit files are burned into CPLD through JTAG loading cable, and the whole design of dual-energy signal acquisition driving circuit is completed. From the results of software simulation and oscilloscope measurement, it can be concluded that the output signal correlation and pulse width of the driving circuit meet the timing design requirements, and the waveform is good. The driving circuit has strong flexibility, good stability, fast speed, high reliability and simple structure. Compared with the traditional drive circuit, this scheme greatly simplifies the structure and design process of the drive circuit.

5. References
[1] Chen Zheng. Research on X-ray identification technology of contraband [J]. Journal of Gansu Police Vocational College, 2010, (03): 70.74
[2] Guo Jintao. Research on the theory and system of X-ray medium identification [D]. Xi’an Petroleum University, 2014.
[3] Wu Xiaoping, Chen Zhiqiang, Wang Xuewu. Application of Dual-energy X-ray Material Identification Technology in Large Container Detection System [J]. Nuclear Electronics and Detection Technology, 2005, (06): 216-218
[4] Alvarez RE, Macovski A. Energy-selective reconstructions in X-ray computerized tomography [J]. Physics in Medicine and Biology. 1976, 21 (5): 733-744
[5] Macovski, A., Alvarez, R.E., Chan, J.L.H. Energy dependent reconstruction in Xray computerized tomography [J]. Computers in Biology and Medicine. 1976, 6 (4): 325-336
[6] Chen Zhiqiang, Zhao Tiao, Li Liang. Summary of high-energy dual-energy X-ray DR imaging and material identification technology [J]. Theory and application of CT, 2014, 05:731.742
[7] Xia Yuwen. Verilog HDL Digital Design and Synthesis (Second Edition) [M]. Electronic Industry Press, 2004.
[8] AD9826 Datasheet[Z/OL].