Superconducting Through-Silicon Vias for Quantum Integrated Circuits

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We describe a microfabrication process for superconducting through-silicon vias appropriate for use in superconducting qubit quantum processors. With a sloped-wall via geometry, we can use non-conformal metal deposition methods such as electron-beam evaporation and sputtering, which reliably deposit high quality superconducting films. Via superconductivity is validated by demonstrating zero via-to-via resistance below the critical temperature of aluminum.

INTRODUCTION

Through-silicon vias (TSVs) have been widely used in semiconducting integrated devices in recent years, both as high-performance interconnects to create 3D circuits and to engineer isolation between components on chips [1, 2]. Superconducting qubit circuits, composed of microwave resonant structures that store and manipulate quantum information, will require similar technical solutions as the number of qubits grow. A truly scalable quantum integrated circuit architecture requires both 3D integration and careful engineering of the RF environment in which qubits operate.

The advantages of using TSVs in quantum integrated circuits are:

Signal delivery. Traditionally, signal delivery in superconducting qubit devices has been in the plane of the circuit through bond pads at the boundary of the chip. However, most proposals for large quantum circuits involve tiled 2D lattices in which interior qubits cannot be accessed from the perimeter [3]. Delivering signals perpendicular to the plane of the 2D circuit is therefore necessary for future scalability. Flip-chip processes using superconducting indium bumps have recently been used to bond a chip with qubits to another chip with readout and control signals demonstrating high qubit coherence (>20 µs) [4-6]. 3D integration using vias, on the other hand, enables delivering signals through the substrate. A simple schematic of such an architecture is shown in Fig. 1 in which high frequency signals travel from an interposer to the back side of the chip, through the vias, onto the top surface, and to the qubits.

Isolation. To achieve maximum coherence and minimal crosstalk, the resonant elements of a quantum integrated circuit should ideally be completely isolated from each other and from the environment, except for engineered couplings. This would also eliminate frequency-crowding concerns for large circuits. TSVs can partially accomplish this if arranged so as to surround resonant elements, locally confining electromagnetic modes in the substrate. A conductive cage above the plane of the chip would complete the creation of a 3D enclosure.

Suppressing substrate modes. Dielectric substrates host electromagnetic modes. A thin chip with dimensions \( x \times y \) has a fundamental mode with frequency \( (c/2\pi\sqrt{\varepsilon})\sqrt{\left(\pi/x\right)^2 + \left(\pi/y\right)^2} \), where \( c \) is the speed of light in free space and \( \varepsilon \) is the dielectric constant. For sufficiently large substrates, the mode falls in the operating range of a superconducting qubit device, typically 3-10 GHz, and provides a loss channel for otherwise high-quality resonators. In practice, this places an upper bound on circuit size and complexity one can build on a single chip. However, the presence of a large number of metal TSVs in the substrate enforces boundary conditions on substrate modes, effectively limiting the maximum wavelength to the TSV spacing. This can raise the lowest-lying mode frequency well above 10 GHz and eliminates its dependence on substrate size, allowing for arbitrarily large chips.

Enabling coupling between layers. Long-term scaling of quantum integrated circuits will require multi-layer structures. In such a geometry, the precision of the vertical distance between layers is usually set by the fabrication technology, making capacitative coupling between layers difficult to engineer. Rather, a galvanic connection using vias is preferable for delivering signals between different planes, and coupling capacitances could be designed within planes.
The state of the art of TSV manufacturing in the semiconductor industry typically includes the following process steps [2]:

**Via formation:** Deep reactive ion etching or laser drilling to define the via shape.

**Dielectric barrier deposition:** Thermal silicon oxide or nitride, or plasma-enhanced chemical vapor deposition (PECVD) of a thin film to form diffusion barrier between Cu and Si.

**Adhesion and seed layer deposition:** Physical vapor deposition (PVD) of Ti, followed by Cu.

**Cu electroplating:** Fill the via with conductive Cu. Alternative electroplating metals such as W and Sn are also used. Usually, it is followed by an annealing process to release stress.

**Chemical mechanical polishing (CMP):** Removal of Cu overburden.

**TSV reveal:** Mechanical and chemical grinding or polishing (hard reveal) or wet etching (soft reveal) of the wafer to reveal the vias.

This process, while manufacturable and widely used for CMOS circuits, could be incompatible with superconducting qubits for three reasons. First, the dielectric liner would be a site of microwave loss. Second, the normal metal fill will introduce ohmic heating and loss, whether due to signals or grounding currents. Third, poorly controlled CMP processes could lead to small levels of contamination and doping in otherwise insulating Si substrates. All three factors would reduce qubit lifetimes.

Furthermore, these problems cannot be resolved with simple materials substitutions. There is no well-established process for electroplating of superconducting metals such as Al. High-quality superconducting microwave structures are typically fabricated via physical deposition, but such methods deposit metal too slowly and with too much stress to fill deep holes. Even worse, the difference in thermal expansion properties between Si and a metal fill may prohibit cryogenic use of these structures.

### TSV MANUFACTURING IN QUANTUM INTEGRATED CIRCUITS

We propose a process for manufacturing superconducting TSVs which uses a superconducting metal as the via liner, a polymer for partial filling, and avoids the need for CMP by employing a temporary membrane to support the via liner.

**Support membrane.** Unlike industry processes in which thick wafers are etched and later polished to reveal the vias, we etch entirely through the Si wafer during via formation. First, however, we deposit a film on the back of the wafer which is highly selective to our silicon etch and therefore acts as stop. In subsequent steps it supports the deposition of liners and fills. At the end of the process it is easily etched away, revealing a pristine Si surface with exposed metal tops of vias, onto which the superconducting circuit can be fabricated.

**Etch geometry and deposition method.** In our process, via walls are etched to be slanted, which allows us to substitute electroplating for more directional deposition methods such as electron-beam evaporation, epitaxy, and sputtering. For a truly directional process, we can easily calculate the coverage on the sidewalls as a function of both via sidewall angle and deposition angle.

Fig. 2 shows the ratio of the sidewall deposition rate to the overall deposition rate on a normal surface as a function of the evaporation angle for different sidewall tapers. For evaporation angles smaller than the TSV angle, both sidewalls are coated, while at least a portion of the sidewalls is shadowed when the evaporation angle is larger than the TSV angle. In the former regime, a nonzero deposition angle reduces sidewall deposition. Hence, we primarily deposit onto our sloped walls at an angle normal to the plane of the wafer, with no substrate tilt relative to the deposition source.

The choice of the via sidewall angle depends on: 1) the minimum required thickness of the metal on the walls; 2) the maximum possible deposition thickness; and 3) the maximum allowed difference between the via diameter at each end (which depends on the minimum required via density and the maximum acceptable via volume).

Based on the above parameters, sidewall angles in the range of 10 to 20 degrees are small enough to allow acceptable difference between the opening on the sides of
the wafers (in our case, ∼150 µm) and at the same time large enough to allow sidewall coverage in the range of 20–30% of the amount deposited on a normal surface.

**Polymer fill.** It is still necessary to fill the via to provide permanent support for the thin metal liner once the membrane is removed. The criteria for the selection of fill materials are: 1) a straightforward deposition process that does not alter the thin membrane and liner film; 2) mechanical strength to provide permanent support to the via metal liner; 3) robustness to downstream chemical processing; 4) cryogenic compatibility, including thermal expansion properties similar to silicon. The microwave properties of the material are not relevant as long as the superconducting liner is thick enough to completely shield it from the circuit.

Thick polymers are one promising class of materials for this purpose, among which Parylene-C was chosen [11]. It has the desired mechanical and chemical properties, is inert to almost all wet process, and has a simple deposition process. Due to its conformal, pinhole-free, and easily controlled deposition process (even for ultra-thin coatings), it is commonly used to protect electronic components and compact packages as well as sensors, LEDs, and MEMS [12]. We have also tested the mechanical and cryogenic properties with no sign of degradation after repeated thermal cycles.

**SUPERCONDUCTING TSV PROCESS**

Here, we describe the process we have developed for fabricating grounded superconducting vias for isolation and for suppressing substrate modes. In this process all the vias are grounded through a blanket metal deposition on the back side side of the wafer. Future use for 3D signal delivery will require additional process steps to pattern the wafer backside. The process steps are as follows (Fig. 3):

**Starting substrate.** For superconducting microwave structures, we use 300 µm-thick high-resistivity (>15 kΩ-cm) silicon wafers. First, we deposit an etch stop for the via etch process. We perform PECVD of a silicon oxynitride SiO$_x$N$_y$ film with the thickness of 7-10 µm. The stoichiometry is tuned to minimize stress and wafer bow, reduce stress changes in the membrane upon etch stop removal, and be easily removed using wet etch chemistries. Since the etch is deep, a thick positive photoresist (> 10 µm) is used to pattern the vias on the non-oxynitride side of the wafer.

**Via formation.** The via formation process employs the method described in [7, 10] where a non-Bosch process in an SPTS inductively coupled plasma (ICP) tool is used to etch the desired via taper. The continuous plasma etching process uses a mixture of SF$_6$/O$_2$/Ar gases to etch vias with angles in the range of 10 to 20 degrees. The etch process is performed in two steps, which we refer to as the main via etch and the isotropic via etch. In the main etch, the sloped vias are formed with an overhang as a result of the etch undercut (Fig. 4-b). Next, in the isotropic etch step, we strip off the photoresist and perform a global etch to remove the overhang (Fig. 4-d).

Approximately 50 µm of the wafer thickness is etched away during the isotropic etch step, making the final wafer thickness ∼250 µm. Our target angle is 10-20 degrees, and is achieved with SF$_6$/O$_2$ flows of 135/70 sccm and 300/75 sccm for the main and iso etch steps, respectively. Also, since the etch stops at an isolating mem-
brane, to avoid footing (which is a common problem for dry silicon etching in ICP processes) we employ a low frequency pulsed power for the platen.

Superconducting liner deposition. In this step we coat the via walls with Al using electron-beam evaporation. For the film to effectively shield radiation it should be several times larger than the London penetration depth (∼50 nm). A 2.5 µm deposition guarantees minimum of 250 nm deposition on the sidewalls for angles above 10 degrees, based on the calculations represented in Fig. 2. This blanket deposition coats the walls of the vias as well as the entire backside of the wafer, and grounding all vias together.

Via fill. We deposit a 20 µm layer of Parylene-C film in a PVD process. It partially fills the vias on the sidewalls and the bottom, while leaving most of the via volume empty. Fig. 5 shows the cross-section image of the vias after Parylene deposition step.

Via reveal. Finally, the oxynitride film is etched using buffered HF acid. The via Al is revealed after this process (see Fig. 6 for a top view). The two concentric circles shown on the revealed side of the via are representative of the main and isotropic etch processes, which cause different surface roughnesses on the silicon and the oxynitride membrane. This roughness is transferred to the deposited Al film.

After the reveal step, the wafer is ready for the quantum circuit fabrication processes.

SUPERCONDUCTIVITY MEASUREMENT

To verify the superconductivity of the vias, we measured DC resistances between pairs of vias in a dilution refrigerator. Since all vias on a given wafer are connected through the back side, we can measure in a 4-terminal arrangement the voltage drop resulting from a current flowing from the front side, through one via, across the back plane, and returning to the front side through a second via (Fig. 7a-b).

To prepare the sample, we patterned contact pads, re-
moved the native oxide on the surface of the via Al with a 400 V, 20 mA argon ion mill etch, and deposited in situ a 160 nm Al film using electron-beam evaporation. After liftoff, the test structures appear as in Fig. 7c.

We measured the via-to-via resistance with a lock-in amplifier while cooling the sample to subkelvin temperatures (Fig. 8). As expected, the resistance drops to zero below the critical temperature of Al, around 1.2 K. Our instrumentation sets the lower bound of the critical current of this device to be 100 $\mu$A.

**CONCLUSIONS**

A microfabrication process for superconducting TSV with Al, sloped via walls and Parylene-C as the via fill was developed. The via geometry allows using non-conformal metal deposition methods such as e-beam evaporation. We demonstrated the superconductivity of vias by measuring the zero via pair resistance below the critical temperature of Al.

This establishes the viability of the process for making grounded superconducting vias. Future work is required to demonstrate compatibility with superconducting qubit fabrication and measurement, as well as the extra process steps required to use vias to deliver microwave signals.

[1] J. P. Gambino, S. A. Adderly, J. U. Knickerbocker, An overview of through-silicon-via technology and manufacturing challenges, Microelectronic Engineering; 135, 73 (2015)
[2] Lau, J. H., 2013, Through-Silicon Vias for 3D Integration, McGraw-Hill, New York.
[3] A. G. Fowler, M. Mariantoni, J. M. Martinis, and A. N. Cleland, Surface codes: towards practical large-scale quantum computation. Phys. Rev. A 86, 032324 (2012)
[4] D. Rosenberg, et. al., 3D integrated superconducting qubits, [arXiv:1706.04116](https://arxiv.org/abs/1706.04116)
[5] M. Mohseni, et. al., Commercialize quantum technologies in five years, Nature 543, 171, (2017)
[6] J. Mutus, et. al., H46.00006: 3D integration of superconducting qubits with bump bonds: Part 1, J. Kelly, et. al., H46.00007: 3D integration of superconducting qubits with bump bonds: Part 2, E. Lucero, et. al., H46.00008: 3D integration of superconducting qubits with bump bonds: Part 3, APS March Meeting 2017
[7] P. Dixit, et. al., Effect of process gases on fabricating tapered through-silicon vias by continuous SF6/O2/Ar plasma etching, ECS Journal of Solid State Science and Technology, 1 (3) 107 (2012)
[8] S. Heraud, et. al., Easy to fill sloped vias for interconnects applications improved control of silicon tapered etch profile, Electronic Components and Technology Conference, 59th (2009)
[9] R. F. Figueroa, et. al., Control of sidewall slope in silicon vias using SF6/O2 plasma etching in a conventional reactive ion etching tool, Journal of Vacuum Science and Technology B 23, 2226 (2005)
[10] R. Nagarajan, et. al., Development of a novel deep silicon tapered via etch process for through-silicon interconnection in 3-D integrated systems, Electronic Components and Technology Conference, May 30 - June 2, 2006, San Diego, CA, USA, IEEE, 383 (2006).
[11] A Kahouli, Structural and dielectric study of parylene C thin films, Appl. Phys. Lett. 94, 152901 (2009);
[12] URL: https://scscoatings.com/parylene-applications/electronic-coatings/