Supplementary Information

Highly Compact (4F^2) and Well Behaved Nano-Pillar Transistor Controlled Resistive Switching Cell for Neuromorphic System Application

Bing Chen¹,#, Xinpeng Wang²,##*, Bin Gao¹#, Jinfeng Kang¹,##*, Zheng Fang², Lifeng Liu¹, Xiaoyan Liu¹,*, Guo-Qiang Lo² and Dim-Lee Kwong²

¹Institute of Microelectronics, Peking University, Beijing 100871, China;

kangif@pku.edu.cn, xyliu@ime.pku.cn

²Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Singapore 117685;

wangxin@ime.a-star.edu.sg
**Supplementary Information**

**S1 Mechanism of the resistive switching device.**

Commonly, the resistive switching phenomenon in metal-oxide materials is due to formation and rupture of conductive filament (CF) which is constructed by oxygen vacancies ($V_O$). So the switching characteristics of metal-oxide based resistive switching devices are strongly correlated with generation and recombination of $V_O$ in the switching layer [1]. The physical origin of resistive switching phenomenon is schematically illustrated in Fig.S1. In the SET process, under the electrical field from inert electrode (IE) to active electrode (AE) the oxygen ion ($O^{2-}$) is generated and drift to the AE left VO in the oxide layer. This process will cause the formation of a CF connecting AE and IE, which results in the cell switching to the low resistance state (LRS). For the RESET process, the AE acts as $O^{2-}$ reservoir, when apply a field from AE to IE, a part of Vo in oxide layer will be positive charged due to electron deplete effect, and the $O^{2-}$ will be drifted from AE to switching layer and the recombine with positive charged $V_O$. then the CF will rupture and the resistive switching device will be switched to the high resistance state (HRS). Normally The electron transport is always metallic-like when $V_O$ concentration is high, but in low current resistive switching device it is dominated by electron hopping among the disperse $V_O$. Additionally, the thermal effect caused by high current density in filament play an important role in Vo generation and recombination.
Fig S1 Schematic physical process of resistive switching phenomenon, including the generation of oxygen vacancy, oxygen ion hopping, oxygen ion absorbed and released by the electrode, recombination of oxygen vacancy with oxygen ion, local temperature increase due to local current and electron transport.
**S2 Simulated oxygen vacancy distribution during resistive switching process**

To investigate the microscopic mechanism of CF generation and rapture process in resistive switching metal, which is important in its synaptic response to voltage pulse stimulate, we develop a stochastic method to simulate the oxygen vacancies distribution during this microscopic process [2].

Fig. S2 shows the evolution of the $V_O$ distribution and corresponding I-V curve obtains from the stochastic simulation during the resistive switching process. The results indicate that in SET process (A-D), the CF growing is corresponding to two stages, firstly connecting the tip of the CF and TE then gradually enlarging along the radius direction as the current increase. And CF rupture in the RESET operation (E-H) is corresponding to the whole filament disconnecting firstly at the TE then extending towards the interior gradually.

Fig. S2 simulated I-V curve of resistive switching process and the $V_O$ distribution in the switching layer at different point marked in the I-V curve.
S3 Reliability of the nano-pillar transistor controlled resistive switching Cell.

The endurance and retention characteristics of the nano-pillar transistor controlled resistive switching cell are shown in Fig.S3 [3]. The good reliability and low current switching of the cell is benefits its high density integration which is critical for the synaptic device in neuromorphic system.

**Fig. S3** (a) Endurance properties of the 1T-1R cell in bipolar switching mode using voltage pulses, without degradation after 105 cycles; (b) measure Retention characteristics of the 1T-1R cell @ 300k and with read-out voltage @ 2V.
S4 Synaptic response of the 1T1R cell under negative voltage pulse stimulate

The bipolar synaptic behavior of the synaptic devices is important for realizing some complex functions in electrical neuromorphic systems. Besides the gate controlled synaptic behavior of the 1T1R cell under positive voltage pulse stimulation, the cell also shows good synaptic response to negative voltage pulse stimulation, as illustrated in Fig.S4.

**Fig. S4** Measured synaptic response of the 1T1R cell under negative voltage pulse: at first the cell is switched to LRS, when apply a -1.5V/1µs pulse, its resistance gradually increase.
**S5 Characteristics of the gate-all-around nano-pillar transistor**

The feature-size scaling down in semiconductor technology has continued for nearly 50 years and face great challenge now. As a result, the gate-all-around structure is developed to enhance gate electrostatic control of channel potential and Fig. S5 is schematic view of a gate-all-around (GAA) nano-pillar transistor. A GAA Si nano-pillar transistor with 8 nm channel length and 31.4nm channel width (radius of Si nano-pillar is 5nm) is demonstrated [4]. In the GAA nano-pillar transistor, record-high drive currents density of 3740 μA/μm good sub-threshold slope of 75mV/Dec and large $I_{on}/I_{off} > 10^7$ is attain.

![Vertical gate-all-around Si Nano-pillar transistor](image)

**Fig. S5** schematic view of the structure of a gate-all-around (GAA) nano-pillar transistor
**S6 Superiority of the 1T1R cell in neuromorphic system application**

New training rules can be developed based on the developed 1T1R cell. For example, the demonstrated gate-controlled multi-level switching behaviors enable the realization of novel neuromorphic architecture. The feedback signal of the neuromorphic system based on the 1T1R synapse architecture can apply on the gate to process complex tasks. As a result the “winner-take-all” system architecture [5] as a critical neuromorphic system application can be easily realized by the array as shown in Figure.S6. Different from previous work [refs.18,19] whose feedback signal is always applied on the bottom electrode of synaptic ReRAM, in this work the feedback signal can be applied on the gate to promote activation or inhibition of the post-neurons. In this case the feedback signal can control the connection strength of the synaptic device more effectively.

**Figure.S6** Schematic view of using this 1T1R to realize a “winner-take-all” system architecture. At first all of the synapse connect pre-neuron and post-neuron is at same states that the gate voltage which controlling the pulse response of ReRAM. Then when a winner neuron fire, the 1T1R synapses connect to this neuron will be given a positive gate voltage to strengthen their connection. But other synapses connect to post-neurons will be given a negative gate voltage to inhibit them.
References:

1. Gao, B.; Kang, J. F.; Chen, Y. S.; Zhang, F. F.; Chen, B.; Huang, P.; Liu, L. F.; Liu, X. Y.; Wang, Y. Y.; Tran, X. A.; Wang, Z. R.; Yu, H. Y.; Chin, A., Oxide-Based RRAM: Unified Microscopic Principle for both Unipolar and Bipolar Switching. *IEEE Tech. Dig. IEDM 2011*, 2011 417-420.

2. Huang, P.; Gao, B.; Chen, B.; Zhang, F. F.; Liu, L. F.; Gang, D.; Kang, J. F.; Liu, X. Y., Stochastic Simulation of Forming, SET and RESET Process for Transition Metal Oxide-based Resistive Switching Memory. In *Simulation of Semiconductor Processes and Devices (SISPAD)* 312-315 (2012).

3. Wang, X. P.; Fang, Z.; X. Li; Chen, B.; Gao, B.; Kang, J. F.; Chen, Z. X.; Kamath, A.; Shen, N. S.; Singh, N.; Lo, G. Q.; Kwong, D. L., Highly Compact 1T-1R Architecture (4F² Footprint) Involving Fully CMOS Compatible Vertical GAA Nano-Pillar Transistors and Oxide-Based RRAM Cells Exhibiting Excellent NVM Properties and Ultra-Low Power Operation. *IEEE Tech. Dig. IEDM, 2012*, 493-496.

4. Jiang, Y.; Liow, T.Y.; Singh, N.; Tan, L.H.; Lo, G.Q.; Chan, D.S.H.; Kwong, D.L., Performance breakthrough in 8 nm gate length Gate-All-Around nanowire transistors using metallic nanowire contacts. *VLSI Technology Symposium, 2008*, 34-35.

5. K. Mehrotra, C. K. Mohan, S. Ranka, Elements of Artificial Neural Networks, MIT Press, 1996.