Abstract

Traditional processors use the von Neumann execution model, some other processors in the past have used the dataflow execution model. A combination of von Neumann model and dataflow model is also tried in the past and the resultant model is referred as hybrid dataflow execution model. We describe a hybrid dataflow model known as the microthreading. It provides constructs for creation, synchronization and communication between threads in an intermediate language. The microthreading model is an abstract programming and machine model for many-core architecture. A particular instance of this model is named as the microthreaded architecture or the Microgrid. This architecture implements all the concurrency constructs of the microthreading model in the hardware with the management of these constructs in the hardware.

Contents

1 Introduction 2
2 Latency tolerance 2
3 The microthreading model 3
4 The Microgrid 10
5 Programming the Microgrid 15
6 The microthreading model in the context of the Microgrid 17
7 I/O in the Microgrid 25
8 Conclusion 26
1 Introduction

Traditional processors are based on the von Neumann execution model. In this model a sequence of instructions is executed one-by-one and the state of the program is identified by a single program counter. However, performance can not be improved by executing instructions sequentially. In order to improve the performance, dataflow scheduling is used where instructions are executed based on the availability of data. Theoretically, dataflow models are parallel execution models, because instructions can be scheduled only with the availability of the data, and the scheduled instructions can be executed independently. Most of the out-of-order execution techniques are derived from dataflow scheduling. However, the execution of the program is still determined largely by the instruction sequence as dataflow scheduling is only applied to a few instructions in a small window over the sequential code. In contrast, Moonsoon [29] and Wavescalar [40] are based on dataflow models.

The von Neumann model is simple but sequential, the dataflow model is parallel and improves the efficiency of the execution of the program but with the cost of adding complexity in the hardware design, therefore a hybrid dataflow model [9] [17] was tried to combine the advantages of both. The issue with generalized dataflow model is the requirement of a matching store to detect which operations become ready to execute when its dependencies are satisfied. The efficient organization of the matching store is not so clear to the designers of the execution models. With a hybrid dataflow model, the ordering of instructions can be sequentialized to reduce the need for a big matching store. In hybrid dataflow models instructions are executed based on the von Neumann model within a thread but there is support for dynamic execution of threads based on the dataflow model. This model allowed multicore architectures to exploit parallelism in programs. P-RISC [33], Multiscalar [35] and DDM-CMP [39] are based on the hybrid dataflow model.

Modern many-core systems one way or other provide concurrency constructs to exploit parallelism. To quote Prof. Chris Jesshope By 2020 we could see up to $10^4$ cores and $10^6$ hardware threads on a single chip. The concurrency constructs introduced by the microthreading model are implemented in the instruction set of the microthreaded architecture which is also referred as the Microgrid. This architecture assumes a lot of concurrency in the applications and provides the concurrent architecture to exploit parallelism.

The rest of the paper is organized as follows. In Section 2 we define the latency tolerance feature in computer architecture. We explain the details of the microthreading model in Section 3 and the details of the architecture based on this model in Section 4. We describe the programming of the Microgrid in Section 5. We explain the microthreading model in the context of the Microgrid in Section 6. We present the I/O in the Microgrid in Section 7 and conclude the paper in Section 8.

2 Latency tolerance

In any program, a computation is preceded and followed by memory operation which takes a variable amount of time as it depends on the locality of the data i.e. the data is located in L1-, L2-,L3-caches or off-chip memory. In single-threaded programs the processor has to wait for memory operations to complete and then continue with the computation. In multi-threaded programs, when a memory operation is issued, the thread may be suspended and execution is switched to another available thread. Because of dataflow scheduling, the memory operation completes asynchronously and wakes up the suspended thread. The execution of program is tolerant to the long latency operations and is shown in fig. 1 assuming multiple instructions issued and executed in a single core.
Figure 1: Latency tolerance in multi-threaded programs assuming multiple instructions issued and executed in the core.

The use of multiple threads per core in order to hide latency has been understood for long time \[53\]. For instance, software time sharing is adequate to tolerate external I/O latencies but can not tolerate other long latency operations (e.g. memory access) because of the absence of fine-grained latency tolerance. Hardware multi-threading with dynamic scheduling is used to tolerate long latency operations e.g. MTA cores can switch on every miss operation but it requires a long pipeline flush. Niagara cores switch on the issue of a memory operation \[37\] and therefore tolerate long latency operations, but can not tolerate the latency in FPUs or other asynchronous operations (e.g. management of threads).

3 The microthreading model

The microthreading model \[18\] is based on a type of hybrid dataflow model and has evolved from DRISC \[4\] (Dynamically-scheduled RISC) which was proposed in 1996 with the goal of separating computation from communication. DRISC provides dataflow scheduling in RISC core, which executes instructions asynchronously and with multiple threads it can tolerate the latency of long latency operations. The innovation in this model is that instead of multiple threads, an ordered set of threads referred as families are used, which provide composability in programs. The operations to create families resemble the fork/join operations found in most parallel programming models. The microthreading model is actually a hybrid of von Neumann model, dataflow scheduling of threads.

The microthreading model has been refined over the decade from a single processor model to an abstract machine model for many-cores and can capture as much concurrency as possible using families of threads in a dynamically evolving concurrency tree. A family is comparable to loop or function call in traditional programming. Any thread can create further families (any heterogeneous combination is supported by the model) showing a hierarchy of threads. An example concurrency tree of the microthreading model is shown in fig. 2 where every family is composed of some number of threads and every thread can create another family.

As the overhead of creating and synchronizing threads in software is 10 to 100 thousands cycles on contemporary hardware \[49\]. The microthreading model shifts the perspective from software threads to hardware threads with concurrency management in hardware in order to reduce the
The number of cycles taken by an instruction depends on the dynamic state of the architecture, but because of asynchronous completion and fine-grained latency tolerance the model has the potential to achieve the goal of RISC i.e. *one cycle per instruction*. In the microthreading model the throughput of the program can potentially demonstrate that every instruction takes one cycle to complete, assuming single instruction issued and executed in the core.

### 3.1 Communication and synchronization

The microthreading model supports hybrid dataflow scheduling by using I-structures [4]. An I-structure is a data structure with the semantics of dataflow i.e. every element has a state of either *full* or *empty*. Any operation accessing an element with *empty* state is suspended. The state of the element is changed to *full* asynchronously, and the suspended operation is released to access the element. This process is termed as *split-phase* operation [54] which has two phases; requesting and consuming. A request to the desired data is issued, but if the data is not available, the request is suspended. The execution model can continue executing other computations while the request is in the progress. When the data arrives, the suspended operation is released and the instruction can consume the data.

The microthreading model uses I-structure as a set of channels; globals and shared to support communication between threads. These channels are actually registers address using the register names of the underlying ISA. But for the sake of generality these registers are referred as channels. These channels have blocking read and non-blocking writes. By blocking we mean that the operation is suspended because of the unavailability of the data, and by non-blocking we mean that the operation is performed and the writing of the data complete asynchronously. Global channels are mapped to all threads in the family and have read only access. Shared channels provide the mechanism for the communication only between adjacent threads uni-directionally in the ordered sequence of threads in the family. The sharing of synchronizers between threads enables fast
thread-to-thread synchronization, for example to implement dependencies in a loop. The creating thread communicate with the created threads using messages, which can access the synchronizing memory of a family remotely. The one-way communication is restricted but ensures a deadlock free communication [52]. The communication and synchronization between threads are shown in fig. 3 and more details can be found in [21, Sec. 4.3.3.3].

3.2 Memory consistency model

The microthreading model addresses consistency using two models for threads and families. A single thread is sequentially consistent, as all the instructions within a thread appear to execute in sequential order. A family is weakly consistent, as it follows the three properties of Weak Consistency:

- Any created thread can perform a read or write operation only after all the writes by the creating thread prior to the creation of the family.
- The family can be synchronized only when all previous write operations by the created threads are performed.
The creating thread can perform a read or write operation only after the created family is synchronized.

Memory consistency models [11, 28] have been defined for different programming and machine models. We present only two consistency models which are relevant to the microthreading model.

**Sequential Consistency (SC):**
A system is sequentially consistent if the result of the execution of instructions is the same as if instruction of all the cores were executed in some sequential order. In addition, the instructions of each individual core appear in the same sequence as specified by the program. SC has two cases:

1. A read operation by any processor/thread is allowed to perform only if all previous read and write accesses are performed globally.
2. A write operation by any processor/thread is allowed to perform only if all previous read and write accesses are performed globally.

**Weak Consistency (WC):**
A system is weakly consistent if the synchronizing operation is performed only if there is no pending ordinary (non-synchronizing) read or write operations, and any ordinary read or write operations can not be performed if there is a pending synchronizing operation. The weak consistency is defined in [11] but we are slightly modifying the terminology to match with the microthreading model. WC has three cases:

1. All previous synchronizing operations must be performed before an ordinary operation is performed.
2. All previous ordinary operations must be performed before the synchronizing variable.
3. Synchronizing operations are sequentially consistent with respect to one another.

### 3.3 The notion of resources in the microthreading model

The microthreading model is an abstract machine and programming model and therefore does not have physical resources, but it is designed with the notion of resources as the model addresses many-core architectures. A family of threads is allocated to a group of resources and are referred as place. These resources can be one or more cores, single or many threads etc. A family created on a place will execute there until synchronized and a thread allocated to a core will execute there until terminated.

In order to control the number of threads on a core per family, windowsize is introduced as a run-time parameter. A programmer can carefully use this parameter to use only the requested number of resources, leaving resources for other families (or may be more important families). More importantly this parameter is used to avoid deadlock from dependencies down the concurrency tree. It can wisely be used by the programmer or compiler to ensure that at least one leaf of the concurrency tree can continue execution by using the available resources and hence avoid deadlocks. The windowsize limits the number of threads executing in a family, similar to the concept as k-bounded loops in dataflow scheduling. The parameter ‘k’ is comparable to the windowsize in
the microthreading model. However, it should be noted that *windowsize* is per core and 'k' is per loop which may be distributed on many cores.

The microthreading model introduces *break* used by a thread to terminate the execution of the family. The *break* will let the already created threads of the family to complete and will stop the creation of any new threads in the family. It is comparable to the *exit* statement in loops or functions in traditional programming, and is useful when the synchronization of the family depends on some dynamic conditions.

3.4 Concurrency constructs

The microthreading model defines concurrency constructs to use the concurrency provided by the hardware. But these constructs need to be introduced in some intermediate language in order to write programs. In this section we explain some of the concurrency constructs of the microthreading model and show that these constructs are defined in an intermediate language referred as SL [21, 22]. In Section 5 we will show an example program that will demonstrate the use of concurrency constructs of the microthreading model in an application.

Allocation and deallocation of place

A group of cores i.e. *place* is required to be allocated before the creation of a family and released when the family is synchronized.

- *sep_alloc(<parameters>)* and *sep_free(<parameters>)*
  are used to allocate and de-allocate cores through a software API. The *<parameters>* are a list of parameters passed for allocation and de-allocation e.g. specifying the strategy of allocation or number of cores etc. and can be found in [19].

Creation and synchronization of family

A family of threads can be created by using *sl_create* constructs similar to a loop in traditional programming. The created family can be synchronized using *sl_sync* construct.

- *sl_create(fid, pid, start, limit, step, windowsize, options, thread[, <arguments>])*
  defines the creation of a parameterized family.

  - *fid* is the identifier of the family of type *sl_family_t*.
  
  - *pid* is the identifier of the *place* of type *sl_place_t*.

  - *start, limit* and *step* indicate the starting, ending and iteration step counter of threads (similar to the iterators in a loop).

  - *windowsize* determines the upper limit on the number of threads that can be created on a core.
• *option*
decides the way the family should be created an executed. e.g. sl_forceseq will force the
family to execute sequentially.

• *thread*
is the name of the thread which defines the code to be executed by created threads in the
family.

• *<argument>*
is a comma separated list of global and shared arguments passed to the thread.

• *sl_sync()*
is used for the synchronization of the family.

**Global and shared channels**
The global and shared channels introduced by the microthreading model are implemented as global
and shared variable in the intermediate language. They are used as parameters/arguments to the
creation of a family of thread.

• *sl_glarg(type, variable, value)* and *sl_sharg(type, variable, value)*
  indicates the global and shared variable of type with some value passed from the creating
  thread to the created thread.

• *sl_glparm(type, variable) and sl_shparm(type, variable)*
defines the global and shared variable of type received by the created thread from the creating
  thread.

• *sl_getp(variable)*
is used to read from global or shared variable.

• *sl_setp(variable, value)*
is used to write the shared variable with a modified value to be read by the next thread.

• *sl_seta(variable, value)*
is used by the creating thread to write a value to the shared variable to the first thread of
  the family.

• *sl_geta(variable)*
is used by the creating thread to read the shared variable from the last thread in the family.

**Starting and terminating threads**
Threads are implicitly created with the creation of a parameterized family and terminated when all
of their instructions are executed. But programmers need to define the starting and terminating of
a thread similar to the way functions are defined in traditional programming.

• *sl_def(type, < parameter >)*
is used to define a thread with return of type and < parameter > of a list of the global or
  shared variables used by the thread.
• \texttt{sl.enddef}
  defines the terminating of the thread.

• \texttt{sl.index(index)}
  can be used to retrieve the index of the ordered set of threads in the family.

**Breaking family**

Any thread in a family can use the break statement to stop creation of new threads in the family. The syntax is given below:

• \texttt{sl.break}
  is used to stop creating new threads in the family.

### 3.5 More about families

The microthreading model has evolved over the years and have introduced different types of families as per the requirements of the programs. All the families are created using \texttt{sl.create} construct (except detached family, see below). The family can be of any of the type (described in this section) based on the way the created threads are executing. However, some types of families are need to be explicitly defined by passing a parameter to the create construct. In this section we give a brief overview of the different types of families supported by the microthreading model with the aim that programmers can write a parallel program using different combination of threads and families. Families that are required to be explicitly defined at the time of creation are explicitly stated in their respective subsection.

**Independent family**

A family is called independent family when its created threads do not require any communication between threads. Embarrassingly parallel applications generally do not require communication between created threads and the microthreading model supports these types of applications by creating them as independent families.

**Dependent family**

Threads in dependent family communicate with each other. Fine-grained parallel applications require a lot of communication and coarse-grained parallel applications communicate a little between threads. The microthreading model supports these types of application by creating dependent families. These families communicate with each other through shared channels introduced earlier (c.f. Section 3.1). Dependent families are inherently sequential and therefore do not get any speedup by distributing the threads on many cores. But in the microthreading model these threads get benefit from latency tolerance and asynchronous completion as a dependent family can be executed along with other families.

**Homogeneous family**

All families are statically homogeneous but can be made dynamically heterogeneous if the programmer calls/creates different functions in a thread dependent on the index of the thread.
**Heterogeneous family**

A family can be composed of threads that are not identical to each other. The programmer need to explicitly write the code for different threads based on the index of the thread to perform different operations.

**Detached family**

A family is required to be synchronized before continuing further. But there may be situations when a family may not want to synchronize and is called detached family. For instance, creating a family that prints some characters on terminal may not require synchronization as all the created threads perform only read operations and do not modify any memory. The programmer has to explicitly specify the detached family by creating a family with `sl_detach(<parameters>)` instead of `sl_create(<parameters>)`, where `parameters` are defined in Section 3.4.

**Exclusive family**

To support mutual exclusion in the microthreading model, exclusive families are introduced. Exclusive families are treated differently to regular families because of the requirement of being mutually exclusive. More details about mutual exclusion in the microthreading model can be found in [21, Sec. 14.1]. To create an exclusive family the programmer have to explicitly use `sl-exclusive` in the place of `options` in the create construct. Generally exclusive families consist of a single thread.

**Sequentialized family**

A family can be forced to execute sequentially, to avoid using resources by creating many threads. The programmer has to explicitly use `sl-forceseq` at the place of `options` in the create construct. The sequentialized family will execute as regular code of the parent thread.

### 4 The Microgrid

Microgrid is actually a blueprint with parameters defined for the architecture. There are many Microgrids; with 1 core, 128 cores, 1000 cores, random bank memory, COMA etc. We use the term Microgrid to generalize all instances of the blueprint. At some time we talk about a particular instance, but then we explicitly give the details of the parameters. In the context of the Microgrid, a core is explicitly termed as microthreaded core to differentiate from traditional cores. In addition, a thread is termed as microthread to distinguish it from traditional threads.

The basic component of the Microgrid is the microthreaded core, and it is important that we understand the execution of instructions in the core in order to simulate the core at the high-level. The concurrency constructs of the microthreading model are implemented in the instruction set (ISA) of the core. The cores are designed to be simple; single issue, in-order, 6-stage pipeline [20] and based on RISC. Some components of the operating system are implemented in the silicon of the core [7] e.g. scheduler, resource allocation, mapping etc. Some energy inefficient features are removed from the design of the core e.g. speculation, out-of-order execution and cache prefetching.

The 6 stage pipeline of the core is shown in fig. 4, where we are not showing the scale of components, but mainly the layout of components. It is a classic RISC core with some modifications to existing components and adding some more components to support the concurrency constructs of
the microthreading model in the core. The instruction fetch (IF), instruction decode (ID), register read (RR), execute (EX), memory (MEM), write back (WB), I-cache, D-cache, Integer register file, Floating register file and shared FPU are existing components but slightly modified in order to support the ISA of the Microgrid. The scheduler, allocator, network, thread table and family table are the newly added components to support the concurrency constructs of the microthreading model. The thread table and family table are used to store the thread contexts and family contexts. Every core also has a single exclusive context for creating an exclusive family and thread. The shared channels in the microthreading model are implemented in the registers of the cores. These registers are synchronizing and provide two ports for synchronous and asynchronous completion e.g. D-cache and FPU operations are completed asynchronously and therefore connected to the asynchronous ports of the registers. The bus interface connects the L1-cache to the snoopy bus and the network interface connects the core to the network of other cores on the chip.

The threads in hardware are supported by the thread management unit through the instruction set of the core for creation and synchronization of threads. It has lowered the overhead of creation and synchronization of software threads from more than ten thousands of cycles to just few cycles. It also has extremely low overhead of context switching (zero cycle) and provides fine-grained interleaving i.e. interleaving at every cycle. However, this interleaving is not as strict as in traditional threads. Threads can execute multiple instructions from a single thread until a context switch is required. Interleaving can be bypassed to maximize pipeline usage if there is no other available thread. In single-threaded programs interleaving does not make sense anyway. To ensure fairness in the execution of threads, interleaving is enforced so that no thread can monopolize the execution time of the core.

The binary code of a program generated for the microthreaded core can be executed on any other core that supports the same instruction set as Microgrid. The other core may not support concurrent execution and the code will be executed as single threaded. The code can also be executed on different number of thread slots per core. This is called binary code compatibility i.e.
the binary code may not get the same performance but at least it will not fail, its performance will be gracefully degraded.

As Microgrid provides many cores on a single chip, we show a group of four cores in fig. 5 to demonstrate the interconnection of large number of cores. The delegation network is a Network-on-Chip (NoC) where all cores are addressable from all other cores. Currently it is implemented as a fully connected network in MGSim, but could be implemented as a mesh network in the hardware implementation. A core is connected to the previous and the next core by a distribution network. Two cores share an FPU, and every core has an L1-cache which are connected to L2-cache by a snoopy bus. L2-caches are connected with each other in the distributed cache network. In order to handle deadlock in memory network, every L2-cache has an incoming and outgoing message buffer. An example layout of the 128-core Microgrid in a single chip is shown in fig. 6.

4.1 The communication network

The Microgrid chip has two communication networks on the chip, in addition to the distributed memory network.

Delegation network

Every core is connected to every other core by a bi-directional fully connected network. This network is highly efficient because a message travels in 10 or even less cycles from source to destination. The current implementation of the Microgrid assumes a single cycle, node-to-node routing in a lightly loaded network, but in a loaded network it may take more cycles due to contention and buffering delays. Since delegation network is very efficient, it is used only for the concurrency management between cores that are not adjacent.

Distribution network

All the cores are connected in a single bi-directional daisy-chained network in a Moore curve. The curve can be chosen in a way to preserve locality in L1-caches and L2-caches. It takes two cycles to travel from one core to an adjacent core. The cycles taken by a return trip of a message from
Figure 6: The layout of 128 cores on the Microgrid chip.
a core to any other core on the distribution network is given in Eq: ??, where \( c \) is the number of cores.

\[
delay = 2 \times 2 \times c
\]  

The distribution network is used for the logical partitioning of the chip i.e. different parts of the program can be executed on different parts of the chip. It provides grouping of cores to be used for delegating a family, where the distribution network knows the starting core in the group and the size of the group.

4.2 Resource management in the hardware of the Microgrid

An integer value in the source program is used to identify a group of adjacent cores where a family can be delegated. We refer to the group of cores as \textit{place} and the integer value that identify the place as \textit{placeid}. The identifier can identify the starting core of the place and the size of the place. More details about places can be found in [24, 22] and [21, Chap. 11 & App. E].

A family can execute on the same core as the parent thread or the same place as the parent thread. The former is called \textit{local place} and the later is called \textit{default place} and are identified by place id as 0 and 1 respectively. The execution of a family on a place different than used by the parent thread is called \textit{delegation}. We can perform some arithmetic operations on \textit{placeid} to derive the starting core and the size in the place. The starting core can be calculated as given in Eq: ?? and the size of the place can be calculated as given in Eq: ??.

\[
\text{starting core} = (\text{placeid} \& (\text{placeid} - 1)) >> 1
\]  

\[
\text{size} = \text{placeid} \& -\text{placeid}
\]

4.3 Proposed software service to access resources in the Microgrid

A software layer for the allocation of resources is defined in a protocol referred as SEP [19, 27] which provides an easy to implement and efficient management of resources. In the initial research work, a single core on the Microgrid is reserved for the operations of SEP. It works in mutually exclusive manner, and can soon become a bottleneck when a lot of requests are coming to this single core. Some research is ongoing in avoiding bottleneck and making the management hierarchical.

SEP is implemented using the well-known binary buddy allocation [30] of the memory management. An example of buddy allocation used for cores in the Microgrid is shown in fig. 7.

14

- Divide 8 cores in half.
- Still bigger than required, divide 4 cores into half.
- Still bigger than required, divide 2 cores into half.
Figure 7: An example of the binary buddy allocation of cores by SEP.

- We found a single core as requested, allocate the single core.

A request for a given number of cores, will allocate the group of cores if available. In case the available group is larger than requested, divide the bigger group into smaller group until the group of requested cores is obtained. When the allocated cores are released, they are grouped into a larger group. In the given example when the last 4 cores are released it is grouped into larger group of 8 cores, bringing the system to the initial state.

A programmer can choose different numbers of cores in a place. Every time a place is requested, a group of cores which are not allocated to any other family is allocated. The allocated cores can be used by the family (and sub families if any) to which the place is allocated, and can not be allocated to any other family until explicitly de-allocated. SEP provides two API to programmers; `sep_alloc()` and `sep_free()` for allocation and de-allocation respectively similar to `malloc` and `free` in C. The allocation and de-allocation of SEP can be performed asynchronously, but in the current implementation these processes are not asynchronous. The moment the allocation or de-allocation is issued by a thread, the thread will wait until the operation is completed. The allocation of place depends on the policy given below:

- Minimum: Allocate at least the number of cores specified (may be more if available).
- Maximum: Allocate at most the number of cores specified (may be less if unavailable).
- Exact: Allocate the exact number of cores. The allocation will fail if the given number of cores can not be allocated.
- Any size: Any available size in the power of 2 will be allocated, starting from the lowest available size of the group.

5 Programming the Microgrid

In this section we show an example program i.e. Matrix Multiplication of equal sized matrices, to demonstrate the way programs are written for the Microgrid. The objective is to show that a
Listing 1: Sequential execution of Matrix Multiplication.

```c
#include <stdio.h>

int N = 1000;

int main()
*
{
    int *A = (int*) malloc(N * N * sizeof(int));
    int *B = (int*) malloc(N * N * sizeof(int));
    int *C = (int*) malloc(N * N * sizeof(int));

    int i, j, k;

    // Perform the multiplication
    // matmul
    for(i=0; i<N; i++)
    {
        // matmul_middle
        for(j=0; j<N; j++)
        {
            //matmul_inner
            for(k=0; k<N; k++)
            {
                C[i*N+j] += A[i*N+k] * B[k*N+j];
            }
        }
    }

    free(A), free(B), free(C);
    return 0;
}
```

A sequential C program can be transformed to a microthreaded program easily by high-level programming languages, a compiler or with little effort by the programmer. We also show the concurrency constructs in the generated assembly to demonstrate the way the concurrency constructs are supported in the ISA of the Microgrid.

### Sequential C program

The sequential C code for Matrix Multiplication of size 1000 × 1000 is shown in listing 1. We allocate three arrays; two for source matrices and one for the result matrix. Once the memory is allocated, we can fill these arrays with some numbers, but for saving space in the page, we assume the existing values present in those memory locations. To perform matrix multiplication we write three loops; outer loop, middle loop and inner loop. The inner loop is the one which multiplies the two elements of the source matrices and stores in the result matrix. After the multiplication is completed, we free the allocated memory.

### Microthreaded program

The microthreaded program for the Matrix Multiplication of size 1000 × 1000 written in SL is shown in listing 2. In the `t_main` function, we first allocate a group of 8 cores in the Microgrid. Then we allocate three arrays for source and result matrices. Then we replace the outer loop by creating a family of N threads. The threads in the outer family create further middle families and then each of those creates the inner family. The inner family perform the multiplication of
elements in source arrays and store the multiplication in the resultant array. The transformation from sequential program to microthreaded program involves the creation of families and shared and global parameters. Once all the families are synchronized, the allocated memory to arrays and allocated cores are released.

**Microthreaded assembly code**

The microthreaded assembly code is shown in listing 3. We can see the assembly instructions of concurrency constructs i.e. *allocate* for the allocation of family, *crei* for creation of family, *sync* for synchronization of family, *puts* writing a shared variable, *gets* reading from a shared variable etc. This is the innovation in the Microgrid, which avoids the mapping of software threads to hardware threads, which reduces the overhead from more than 10-100 thousands cycles of software threads to just few cycles in hardware threads. The ISA of program is scheduled by the microthreaded core with the hardware support for concurrency management.

**SL tool-chain**

The SL tool-chain is shown in fig. 8 and is built around SL [22] which is a C based language but is extended to express the concurrency constructs of the microthreading model. SL is an intermediate language intended for higher level programming languages (such as Single Assignment C or SAC [36, 13, 12, 13, 15], FastFlow [2, 11] etc.) and parallelizing C compiler [34, 35]. SAC is Matlab-like programming language, and it provides concurrency from a very high view. Programmer writes program using arrays and let the compiler decide to exploit concurrency in the programs.

A number of tools and simulators are added to the designer’s toolbox and used for the evaluation of the Microgrid from different perspective. The SL compiler can generate binary for different implementations of the Microgrid. We have software libraries that provide the run-time systems for the microthreading model on the shared memory SMP machines and referred as *sup-ctl* [51] and distributed memory for clusters/grids and are referred as Hydra [26] and *dsup-ctl* [50]. The SL compiler can generate binary for UTLEON3 [9, 10], MGSim [5, 32] and HLSim [34, 43, 47, 42, 41, 44].

Unless specified otherwise, the SL compiler generates two implementations for every family in the given SL program; concurrent and sequential. Either one is used as per the dynamic state of the chip. In case resources can not be allocated to a family, the sequential version can be used. The sequential version of the program is used to avoid deadlock and if the deadlock can be avoided by static analysis, then suspension on resource allocation is safe. The programmer can force the program to use the concurrent version all the time i.e. threads are suspended until resources become available.

6 The microthreading model in the context of the Microgrid

We gave details of the Microgrid, and would like to revisit the microthreading model in the context of the Microgrid. We need to understand all the details of the model and the architecture in order to simulate the architecture at a high level, as the high-level simulator have to exhibit the same behavior.
Listing 2: The microthreaded version of Matrix Multiplication.

```c
#include <svp/sep.h>
#include <stdio.h>

int N = 1000;

//matmul_inner
sl_def(matmul_inner, void,
    sl_shparm(long, sum), sl_glparm(void*, A),
    sl_glparm(void*, B), sl_glparm(size_t, i),
    sl_glparm(size_t, j)) { sl_index(k);
    int (*A)[N][N] = (int (*)[N][N])(void*)sl_getp(A);
    int (*B)[N][N] = (int (*)[N][N])(void*)sl_getp(B);
    int v = (*A)[sl_getp(i)][k] * (*B)[k][sl_getp(j)];
    sl_setp(sum, v + sl_getp(sum));}
}sl_enddef

//matmul_middle
sl_def(matmul_middle, void,
    sl_glparm(void*, A), sl_glparm(void*, B),
    sl_glparm(void*, C), sl_glparm(size_t, i)) { sl_index(j);
    sl_create(pid, 0, N, matmul_inner,
        sl_sharg(long, sum, 0), sl_glarv(void*, sl_getp(A)),
        sl_glarv(void*, sl_getp(B)), sl_glarv(size_t, sl_getp(i)),
        sl_glarv(size_t, j));
    sl_sync();
    int (*C)[N][N] = (int (*)[N][N])(void*)sl_getp(C);
    (*C)[sl_getp(i)][j] = sl_geta(sum);
}sl_enddef

//matmul_outer
sl_def(matmul_outer, void,
    sl_glparm(void*, A), sl_glparm(void*, B),
    sl_glparm(void*, C)) { sl_index(i);
    sl_create(pid, 0, N, matmul_middle,
        sl_glarv(void*, sl_getp(A)), sl_glarv(void*, sl_getp(B)),
        sl_glarv(void*, sl_getp(C)), sl_glarv(size_t, i));
    sl_sync();}
}sl_enddef

sl_def(t_main, void) {
    // Allocate a place using SEP
    int core = 8;
    sl_place_t pid;
    if (sep_alloc(root_sep, &pid, SAL_EXACT, core) == -1) {
        printf("cannot allocate a place.");
        exit(1);
    }

    // Allocate memory for matrices
    int *A = (int*)malloc(N * N * sizeof(int));
    int *B = (int*)malloc(N * N * sizeof(int));
    int *C = (int*)malloc(N * N * sizeof(int));

    // Perform the multiplication
    sl_create(pid, 0, N, matmul_outer,
        sl_glarv(void*, A), sl_glarv(void*, B), sl_glarv(void*, C));
    sl_sync();
    free(A); free(B); free(C); sep_free(root_sep, &pid);
}sl_enddef
```
Listing 3: A snipper of the assembly program generated from the microthreaded program of Matrix Multiplication for the Microgrid.

```
# Assembly code of thread matmul_inner
.ent matmul_inner
.registers 4 1 4 0 0 0
matmul_inner:
ldpc $l3
ldah $l3 , 0( $l3 )
lda $l3 , 0( $l3 )
$matmul_inner:ng:
ldah $l1 , N( $l3 )
ldl $l1 , N( $l1 )
mulq $l0 , $l1 , $l2
mulq $g2 , $l1 , $l1
addq $l2 , $g3 , $l2
addq $l1 , $l0 , $l0
s4addq $l2 , $g1 , $l2
s4addq $l0 , $g0 , $l0
ldl $l2 , 0( $l2 )
ldl $l0 , 0( $l0 )
mull $l2 , $l0 , $l0
addq $l0 , $d0 , $l0
mov $l0 , $s0
end
.end matmul_inner
```

# to show the concurrency constructs in the ISA
.ent t_main
... allocate/s $l0 , 0 , $10
setstart $l0 , 0
ldq $l1 , matmul_outer($117)
setlimit $l0 , $19
setstep $l0 , 1
setblock $l0 , 0
wmb
crei $l0 , 0($l1)
putg $l12 , $l0 , 0
putg $l11 , $l0 , 1
putg $l10 , $l0 , 2
sync $l0 , $l1
mov $l11 , $s11
release $l0
...
.end t_main
6.1 A concrete example

A concrete example of the microthreaded program in the microthreading model executing in a single core of the Microgrid is shown in fig. 9. All concurrency constructs are shown in the figure in the form of rectangles of different sizes/color. We also show the effect of concurrency constructs on the execution of threads. Every thread has an implicit start and end event. Threads are created at the rate of one thread per cycle. The creation process takes 4 cycles (with additional latency to load the cache-line from memory if not in the I-cache, also potential queueing delays if another family is being created). The instructions of a thread can be executed as soon as the thread is created which means the first instruction of the first thread can execute along with the creation of the other threads. The process of creation of threads is implemented sequential on a single core, and is decided based on the trade-off between simple design and efficient creation of family. In the figure we can see that two allocate events execute concurrently, but the create events are sequentialized on a single core.

We show a heterogeneous family of threads i.e. Threads 0 and 1 in Family 0 in the first level is different from each other. We show a dependent family where threads are waiting for the previous threads to write the shared variable/register. We also show that the sync event is waiting for all the threads to complete. We show a homogeneous independent family where the parent threads is executing along with the child threads and therefore the sync does not wait as the time the sync is issued where all the created threads are completed already.
6.2 Family’s Life cycle

A family passes through different stages in the Microgrid during the execution. In this section we consider an example when a parent thread is executing on a core and it delegates a family to a place of four cores shown in fig. 10. A detailed explanation of these stages is given in below section.

Allocation

It is implemented as try-to-allocate mechanism (see below for various options on allocate). In this process; family context, thread contexts and registers on all cores of the place are tried to be allocated. The parent thread sends a message on the delegation network to the first core. The first core checks the availability of at least one thread context, one family context and 31 registers. In case of success the message is passed to the next core of the place using distribution network. When all the cores succeed, the message comes back from the last to the first core on distribution network, and the contexts are asynchronously allocated. The first core then notifies the parent core using delegation network. The allocate protocol has three different modes:

- Normal (or default): The allocation fails immediately after the allocation fails on any core in the place.
- Suspend: The allocation waits for the availability of resources.
- Exclusive: The allocation allocates exclusive contexts and in case of unavailability, keeps waiting until resources are acquired.

The allocate protocol has four different strategies:
Figure 10: The life cycle of a family during the execution in the Microgrid.
- Normal (or default): It will try to allocate as many cores as requested, possibly down to one core (in power of 2).
- Exact: It will allocate the family on all the requested cores.
- Single: It will allocate the entire family to the first core in the place.
- Balanced: It will allocate the entire family to the least loaded core of the place, in terms of family contexts.

Configuration

Once the contexts are allocated on the cores, the next message is sent on the delegation network to the first core to store parameters in the allocated family table entry for the bulk creation. It consists of `setstart`, `setlimit`, `setstop`, `setblock` etc. which are derived from the create construct and defines the number of threads to be created per core. The configuration process is completed asynchronously and does not need any acknowledgement. Therefore as soon as the configuration message is issued, the next message can also be sent. In the current implementation, the delegation network preserves the order of messages i.e. configure messages will reach to the destination before create message.

Creation

The create message is sent from the parent core to the first core in the place via delegation network. As soon as the message is received by a core, thread creation is started asynchronously and the message is forwarded to the next core in the place. The first core will acknowledge the parent core when all the threads on the first core are created. The parent core may then write the global and/or shared registers to the first core through inter-context communication and can continue with its instructions (if any) or wait for the synchronization of the family.

When all the threads are created, the core can de-allocate the contexts that are not really required e.g. at the time of allocation 31 registers were allocated, but suppose a thread is created which only uses 15 registers therefore the core will de-allocate the extra 16 registers. All the threads continue their execution on the allocated core, and as the threads get terminated the context get de-allocated asynchronously. Every core shares the information when it completes executing the allocated threads of a given family with the next core. The last core has the information that all the threads in the family are completed.

Synchronization

When all threads in the family complete, the last core will send a message on the delegation network to the parent core. The parent thread is activated so that the family can be synchronized. All the modified state from the family becomes defined. In the case of a dependent family, the parent core will also read the value from the register updated by the last thread through inter-context communication.

Release

A message is sent from the parent core to the first core on delegation network to release the family. This process will complete asynchronously and the parent core can continue its execution.
6.3 Thread’s life cycle

A thread passes through different stages during the execution and is shown in fig. 11. A newly created thread is allocated thread context, registers and PC (Program counter) is configured to place the thread in ready queue. In case the thread gets an I-cache miss the thread waits until the instructions are loaded from cache. The thread then passes to the active queue. The context of the thread is moved from the active queue to running where the instructions actually execute in the execute stage of the pipeline. A thread can be suspended when it is active or running at the write back stage of the pipeline e.g. in case of dependency. The asynchronous completion of a thread moves the thread from the suspended stage to ready queue. At the termination of the thread the allocated entries are cleaned up which can be used by any newly created threads.

6.4 Distribution of threads

The distribution of threads to the cores in a place depends on the type of family i.e. dependent or independent. The threads in a dependent family are restricted to single core only, as no significant speedup can be obtained by distributing them on multiple cores. However instructions in the thread will get benefit from latency tolerance on asynchronous completion in loads, store and floating point operations.

Threads of an independent family are distributed by an equal distribution of threads per core. In fig. 12 we show an example of a family with 40 threads on 4 cores with window size of 5. Threads are distributed as 40/4 and every core can create 10 threads. But the window size is 5 and therefore only 5 threads can be activated at a time on a given core. As soon as a thread terminates, a new thread can use the context of the terminated thread. For instance on core x, threads 0,1 and 2 are terminated, threads 3-7 are executing and threads 8 and 9 are still waiting to be created.
6.5 Communication through registers

Every thread created in the Microgrid uses a set of registers in the register file. The channels of the microthreading model used for the communication and synchronization of the family introduced in Section 3.1 are implemented in registers of the Microgrid. The registers allocated to a thread are categorized as: globals, locals, shareds and dependents. The mapping of registers to threads and their communication through registers is shown in fig. 13. Some explanation of these registers are given as:

- Global registers implement global channels and are visible to all threads in the family. The parent thread writes to the global registers and all created threads in the family can read from them.
- Local registers are only visible to the individual thread only.
- Dependent registers implement shared channels and have read-only access to the shared registers from the previous threads.
- Shared registers implement shared channels and have the write access by the current threads, and carry the modified value to be read by the next thread.

7 I/O in the Microgrid

The Microgrid requires a decentralized approach where not every core is connected to I/O but some specialized microthreaded cores are used to support I/O and referred as I/O cores. I/O cores have limited/extended instruction set compared to the regular microthreaded core and has no floating point operations. The instruction set of the I/O core supports the I/O infrastructure and are connected to the delegation network of the Microgrid. We do not simulate I/O cores in the current implementation of HLSim, therefore we refer readers to [16, 21, 31] for the I/O management in the Microgrid.
8 Conclusion

The microthreading model is a hybrid dataflow model and provides the simplicity of von Neumann model and asynchronous completion of the dataflow execution model. It is an abstract machine model for many-cores architecture and shifts the perspective from software threads to hardware threads. Because of asynchronous completion and fine-grained latency tolerance the microthreading model can potentially achieve the goal of RISC i.e. one instruction per cycle in the throughput of the program assuming single issue width. The details of a particular type of future many-cores systems are given to demonstrate the complexity of the architecture.

Acknowledgement

The author would like to thank Dr. Raphael Poss, Dr. Michiel van Tol and Prof. dr. Chris Jesshope.

References

[1] Marco Aldinucci, Sonia Campa, Marco Danelutto, Peter Kilpatrick, and Massimo Torquati. Targeting distributed systems in fastflow. In Euro-Par 2012 Workshops, Proc. of the CoreGrid Workshop on Grids, Clouds and P2P Computing, LNCS. Springer, 2013.
[2] Marco Aldinucci, Marco Danelutto, Peter Kilpatrick, and Massimo Torquati. Fastflow: high-
level and efficient streaming on multi-core. In Programming Multi-core and Many-core
Computing Systems, ser. Parallel and Distributed Computing, S. Pllana, page 13, 2012.

[3] Arvind, Rishiyur S. Nikhil, and Keshav K. Pingali. I-structures: data structures for parallel
computing. ACM Trans. Program. Lang. Syst., 11:598–632, October 1989.

[4] A. Bolychevsky, C. R. Jesshope, and V. B. Muchnick. Dynamic scheduling in rise architectures.
In IEE Proceedings Computers and Digital Techniques, volume 143, pages 309–317, 1996.

[5] K. Bousias, L. Guang, C. R. Jesshope, and M. Lankamp. Implementation and evaluation of a
microthread architecture. J. Syst. Archit., 55:149–161, March 2009.

[6] Richard Buehrer and Kattamuri Ekanadham. Incorporating data flow ideas into von neumann
processors for parallel execution. Computers, IEEE Transactions on, C-36(12):1515 –1522,
dec. 1987.

[7] Sorin Cotofana and Stamatis Vassiliadis. On the design complexity of the issue logic of sup-
erscalar machines. In Proceedings of the 24th Conference on EUROMICRO - Volume 1,
EUROMICRO ’98, pages 10277–, Washington, DC, USA, 1998. IEEE Computer Society.

[8] D. E. Culler and Arvind. Resource requirements of dataflow programs. SIGARCH Comput.
Archit. News, 16(2):141–150, May 1988.

[9] M. Danek, L. Kafka, L. Kohout, and J. Sykora. Instruction set extensions for multi-threading
in leon3. In Design and Diagnostics of Electronic Circuits and Systems (DDECS), 2010 IEEE
13th International Symposium on, pages 237 –242, april 2010.

[10] M. Daněk, L. Kafka, L. Kohout, J. Sýkora, and R. Bartosinski. UTLEON3: Exploring Fine-
Grain Multi-Threading in FGPA\textregistered s. Circuits and Systems. Springer, November 2012.

[11] Kourosh Gharachorloo, Daniel Lenoski, James Laudon, Phillip Gibbons, Anoop Gupta, and
John Hennessy. Memory consistency and event ordering in scalable shared-memory multipro-
cessors. SIGARCH Comput. Archit. News, 18:15–26, May 1990.

[12] Clemens Grelck. Shared memory multiprocessor support for functional array processing in
SAC. Journal of Functional Programming, 15(3):353–401, 2005.

[13] Clemens Grelck, Stephan Herlutt, Chris Jesshope, Carl Joslin, Mike Lankamp, Sven-Bodo
Scholz, and Alex Shafarenko. Compiling the functional data-parallel language sac for microgrids
of self-adaptive virtual processors. In 14th Workshop on Compilers for Parallel Computing
(CPC’09), IBM Research Center, Zurich, Switzerland, 2009.

[14] Clemens Grelck and Sven-Bodo Scholz. SAC: A functional array language for efficient multi-
threaded execution. International Journal of Parallel Programming, 34(4):383–427, 2006.

[15] Clemens Grelck and Sven-Bodo Scholz. Sac: off-the-shelf support for data-parallelism on mul-
ticores. In Proceedings of the 2007 workshop on Declarative aspects of multicore programming,
DAMP ’07, pages 25–33, New York, NY, USA, 2007. ACM.
[16] Michael A. Hicks, Michiel W. van Tol, and Chris R. Jesshope. Towards Scalable I/O on a Many-core Architecture. In International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), pages 341–348. IEEE, July 2010.

[17] R. A. Iannucci. Toward a dataflow/von neumann hybrid architecture. SIGARCH Comput. Archit. News, 16:131–140, May 1988.

[18] Chris Jesshope and Bing Luo. Micro-threading: A new approach to future risc. In Proceedings of the 5th Australasian Computer Architecture Conference, pages 34–, Washington, DC, USA, 2000. IEEE Computer Society.

[19] Chris Jesshope, Jean-Marc Philippe, and Michiel van Tol. An Architecture and Protocol for the Management of Resources in Ubiquitous and Heterogeneous Systems Based on the SVP Model of Concurrency. In SAMOS '08: Proceedings of the 8th international workshop on Embedded Computer Systems, pages 218–228, Berlin, Heidelberg, 2008. Springer-Verlag.

[20] Chris R. Jesshope. Multi-threaded microprocessors - evolution or revolution. In Amos Omondi and Stanislav Sedukhin, editors, Advances in Computer Systems Architecture, 8th Asia-Pacific Conference, ACSAC 2003, Aizu-Wakamatsu, Japan, September 23-26, 2003, Proceedings, volume 2823 of Lecture Notes in Computer Science, pages 21–45. Springer, 2003.

[21] Raphael ‘kena’ Poss. On the realizability of hardware microthreading—Revisting the general-purpose processor interface: consequences and challenges. PhD thesis, University of Amsterdam, 2012.

[22] Raphael ‘kena’ Poss. SL—a “quick and dirty” but working intermediate language for SVP systems. Technical Report arXiv:1208.4572v1 [cs.PL], University of Amsterdam, August 2012.

[23] Mike Lankamp. Design and evaluation of a microthreaded many-cores architecture. PhD thesis, University of Amsterdam, 2012.

[24] Mike Lankamp and Raphael Poss. Microgrid places and work addressing.

[25] Mike Lankamp, Michiel W. van Tol, Chris Jesshope, and Raphael Poss. Hardware I/O interface on the Microgrid.

[26] Andrei Matei. Towards Adaptable Parallel Software - the Hydra Runtime for SVP Programs. November 2010.

[27] Raphael ‘kena’ Poss Mike Lankamp. Sl library: dynamic place allocation.

[28] David Mosberger. Memory consistency models. SIGOPS Oper. Syst. Rev., 27:18–26, January 1993.

[29] Gregory M. Papadopoulos and David E. Culler. Monsoon: an explicit token-store architecture. In 25 years of the international symposia on Computer architecture (selected papers), ISCA '98, pages 398–407, New York, NY, USA, 1998. ACM.

[30] James L. Peterson and Theodore A. Norman. Buddy systems. Commun. ACM, 20(6):421–431, June 1977.
[31] Raphael Poss, Mike Lankamp, Irfan Uddin, Jaroslav Sýkora, and Leoš Kafka. Heterogeneous integration to simplify many-core architecture simulations. In Proceedings of the 2012 Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools, RAPIDO ’12, pages 17–24, New York, NY, USA, 2012. ACM.

[32] Raphael Poss, Mike Lankamp, Qiang Yang, Jian Fu, Irfan Uddin, and Chris Jesshope. MGSim - A simulation environment for multi-core research education. SAMOS, 2013. (To appear).

[33] Rahul Razdan, Karl S. Brace, and Michael D. Smith. Prisc software acceleration techniques. In Proceedings of the 1994 IEEE International Conference on Computer Design: VLSI in Computer & Processors, ICCS ’94, pages 145–149, Washington, DC, USA, 1994. IEEE Computer Society.

[34] Dimitris Saougkos, Despina Evgenidou, and George Manis. Specifying loop transformations for C2uTC source-to-source compiler. In Proc. of 14th Workshop on Compilers for Parallel Computing (CPC’09), Zürich, Switzerland. IBM Research Center, January 2009.

[35] Dimitris Saougkos and George Manis. Run-time scheduling with the C2uTC parallelizing compiler. In 2nd Workshop on Parallel Programming and Run-Time Management Techniques for Many–Core Architectures, in Workshop Proceedings of the 24th Conference on Computing Systems (ARCS 2011), Lecture Notes in Computer Science, pages 151–157. Springer, 2011.

[36] Sven-Bodo Scholz, Stephan Herhut, Frank Penczek, and Clemens Grelck. Sac 1.0 – single assignment c – tutorial. 2010.

[37] J.L. Shin, K. Tam, D. Huang, B. Petrick, H. Pham, Changku Hwang, Hongping Li, A. Smith, T. Johnson, F. Schumacher, D. Greenhill, A.S. Leon, and A. Strong. A 40nm 16-core 128-thread cmt sparc soc processor. In Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International, pages 98 –99, 2010.

[38] Gurindar S. Sohi, Scott E. Breach, and T. N. Vijaykumar. Multiscalar processors. SIGARCH Comput. Archit. News, 23:414–425, May 1995.

[39] Kyriakos Stavrou, Paraskevas Evripidou, and Pedro Trancoso. Ddm-cmp: Data-driven multithreading on a chip multiprocessor. In SAMOS’05, pages 364–373, 2005.

[40] Steven Swanson, Andrew Schwerin, Martha Mercaldi, Andrew Petersen, Andrew Putnam, Ken Michelson, Mark Oskin, and Susan J. Eggers. The wavescalar architecture. ACM Trans. Comput. Syst., 25:4:1–4:54, May 2007.

[41] Irfan Uddin. High-level simulation of the Microgrid. Master’s thesis, University of Amsterdam, Amsterdam, the Netherlands, August 2009.

[42] Irfan Uddin, Chris R. Jesshope, Michiel W. van Tol, and Raphael Poss. Collecting signatures to model latency tolerance in high-level simulations of microthreaded cores. In Proceedings of the 2012 Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools, RAPIDO ’12, pages 1–8, New York, NY, USA, 2012. ACM.

[43] Irfan Uddin, Raphael Poss, and Chris Jesshope. Cache-based high-level simulation of microthreaded many-core architectures. Journal of System Architecture, 2013.
[44] Irfan Uddin, Raphael Poss, and Chris Jesshope. Multiple levels of abstraction in the simulation of microthreaded many-core architectures. *Simulation Modelling Practice and Theory*, 2013.

[45] Irfan Uddin, Raphael Poss, and Chris Jesshope. One-IPC high-level simulation of microthreaded many-core architectures. *Simulation Modelling Practice and Theory*, 2013.

[46] Irfan Uddin, Raphael Poss, and Chris Jesshope. Signature-based high-level simulation of microthreaded many-core architectures. *Microprocessors and Microsystems*, 2013. (Submitted, but not yet reviewed).

[47] Irfan Uddin, Raphael Poss, and Chris Jesshope. Analytical-based high-level simulation of microthreaded many-core architectures. In *PDP*, February 2014. (Submitted, but not yet reviewed).

[48] Irfan Uddin, Michiel W. van Tol, and Chris R. Jesshope. High-level simulation of SVP many-core systems. *Parallel Processing Letters*, 21(4):413–438, December 2011.

[49] Michiel W. van Tol. A characterization of the SPARC T3-4 system. *ArXiv e-prints*, abs/1106.2992, June 2011.

[50] Michiel W. van Tol and Juha Koivisto. Extending and implementing the self-adaptive virtual processor for distributed memory architectures. *ArXiv e-prints*, abs/1104.3876, April 2011.

[51] M.W. van Tol, C.R. Jesshope, M. Lankamp, and S. Polstra. An implementation of the sane virtual processor using posix threads. *Journal of Systems Architecture*, 55(3):162–169, 2009. Challenges in self-adaptive computing (Selected papers from the Aether-Morpheus 2007 workshop).

[52] Thuy Duong Vu and Chris Jesshope. Formalizing sane virtual processor in thread algebra. In *Proceedings of the formal engineering methods 9th international conference on Formal methods and software engineering*, ICFEM’07, pages 345–365, Berlin, Heidelberg, 2007. Springer-Verlag.

[53] W.-D. Weber and A. Gupta. Exploring the benefits of multiple hardware contexts in a multiprocessor architecture: preliminary results. *SIGARCH Comput. Archit. News*, 17(3):273–280, April 1989.

[54] Wen yen Lin and Jean luc Gaudiot. The design of i-structure software cache system. In *In Workshop on Multithreaded Execution, Architecture and Compilation*, 1998.