VMM3a, an ASIC for tracking detectors

George Iakovidis
Brookhaven National Laboratory, Upton NY 11973, U.S.A.
E-mail: giakovidis@bnl.gov

Abstract. The VMM3a is a System on Chip (SoC) custom Application Specific Integrated Circuit (ASIC)\(^1\). It is the production version which will be used as the front ASIC for both Micromegas and sTGC detectors of the ATLAS Muon New Small Wheels upgrade at CERN. Due to its highly configurable parameters it has been proposed for several tracking detectors and other experiments. It is fabricated in the 130 nm Global Foundries 8RF-DM process. The ASIC integrates 64 channels, each providing charge amplification, discrimination, neighbour logic, amplitude and timing measurements, analog-to-digital conversions, and either direct output for trigger or multiplexed readout within a data-driven readout system. The front-end amplifier can operate with a wide range of input capacitances, has adjustable polarity, gain and peaking time. The ASIC has been tested on resistive Micromegas and sTGC prototypes in test beam campaigns at CERN.

1. Introduction

The VMM is a custom Application Specific Integrated Circuit (ASIC). The development was initiated with the motivation to upgrade the forward system of the ATLAS muon spectrometer at CERN [1]. The New Small Wheels [2], which was established as an upgrade project in 2013, will be using two detector technologies, resistive Micromegas [3], and sTGC [4] detectors. The VMM was selected to employ the ∼2.4 M channel system, providing precision readout and fast trigger outputs. The first version of the ASIC, VMM1, was designed including only the analog frontend and a two-way analog and digital readout. The VMM2, second version of the chip, included a continuous digital readout while VMM3, the third revision, included the buffer required by ATLAS, being radiation tolerant. It also included several improvements and minor functionalities. The VMM3a implements fixes for all issues found on VMM3. The evolution of the ASIC is shown in Figure 1. The performance of the earlier versions of the ASIC [5] will not be addressed here. This note focuses on the VMM3a, the production version for the NSW upgrade.

2. Architecture

The VMM has been developed at Brookhaven National Laboratory, fabricated in the 130 nm Global Foundries 8RF-DM process (former IBM 8RF-DM). The device is packaged in a 20×20 Ball Grid Array with outline dimensions of 21×21 mm\(^2\). It is composed of 64 front-end channels. A block diagram of one of the identical channels is shown in Figure 2. Each channel integrates a low-noise three-stage charge amplifier with adaptive feedback, test capacitor and masking.

\(^1\) The ASIC is designed by Gianluigi de Geronimo. Circuitry related to the L0 selector is designed by Sorin Martoiu.
possibility. The input MOSFET is a p-channel and is configurable for adjustable polarity. The gain is adjustable in eight values (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC). The filter (shaper) is a third-order (one real pole and two complex conjugate poles) designed in delayed dissipative feedback (DDF) [6]. It has adjustable peaking time in four values (25, 50, 100, and 200 ns) and stabilized, band-gap referenced, baseline. The DDF architecture offers higher analog dynamic range, making possible a relatively high resolution at input capacitance much smaller than 200 pF. The VMM3a features as well an ion tail suppression mechanism in two stages (mild or strong) which ensures that it will recover from longer drift time signals.

Next to the shaper are the sub-hysteresis discriminators [7] with neighbor-enabling logic and individual threshold trimming, the peak detector, and the time detector. The threshold is adjusted by a global 10-bit Digital to Analog Converter (DAC) and an individual for each channel 5-bit trimming DAC. The neighbor-enabling logic forces the measurements of channels neighboring a triggered one, even those channels do not exceed the set threshold. The neighbor logic extends also to the two neighboring chips through bidirectional IO. The peak detector measures the peak amplitude and stores it in an analog memory. The time detector measures the timing using a time-to-amplitude converter (TAC), i.e., a voltage ramp that starts either at threshold crossing or at the time of the peak and stops at a clock cycle of the Bunch Crossing

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2 To process either positive or negative charge.
3 Full baseline return in less than 600 ns.
The ASIC includes global and acquisition resets. It features an adjustable pulse generator connected to the injection capacitor of each channel, adjustable with a global 10-bit DAC, and triggered by an external clock. A band-gap reference circuit and a temperature sensor complete the basic features of the VMM. Finally, it integrates analog monitor capability to directly measure the global DACs, the band-gap reference, the temperature sensor, the analog baseline, the analog pulse, and the channel threshold (after trimming).

3. Readout modes

The VMM has three modes of operation, a two-phase analog mode, a continuous simultaneous read/write mode and the so-called L0 mode.

3.1. Two-phase analog mode

In the two-phase mode data are registered while the VMM is in acquisition mode and then read out, after the system is switched to the readout mode. Acquisition is re-enabled after the readout phase is completed. The readout advances by injecting a token at the token input. The token is sparse, passed only among those channels with valid events. Once the readout is complete, the token is routed to the output for the readout of the next chip. This allows a daisy-chained readout with a single token input. In this mode, the internal ADCs are switched off and the signals are read out through analog buffers with external ADCs.

3.2. Continuous mode

In continuous mode the simultaneous read/write of data assures dead-timeless operation that can handle rates up to the maximum of 4 MHz per channel\(^4\). Higher rates can be achieved by interrupting the 10-bit ADC once the 6-bit ADC has finished. The peak and time detectors convert the voltages into currents that are routed to the 10-bit ADC and 8-bit ADC respectively. The channel is reset once both conversions are complete and the digital values are latched in digital memories. The channel self resets provide continuous and independent operation of all 64-channels. In this mode the ASIC provides 38-bit data stored in a 4-event deep de-randomizing FIFO per channel. The readout is achievable by two serial data-lines.

3.3. L0 mode

This mode was specifically designed to be compatible with the ATLAS readout scheme, but also giving the ability to buffer the data in deeper memory while enabling the chip to select the data based on an external trigger. The first FIFO is a 64-deep “latency” one where all hits can be buffered. Each channel has a selector circuit based on the arrival of the external trigger signal which finds events within the timing window configured (maximum size is eight clock cycles). Once there is a match, the data are copied to the channel FIFO and are ready to be readout in a round-robin manner, starting with the information of the bunch crossing clock. The data transfer from VMM is achieved via two serial lines running at 160 MHz with Double Data Rate (DDR) giving a total bandwidth of 640 Mb/s. The data are encoded using the 8b/10b protocol which leads to an effective bandwidth of 560 Mb/s. The overall buffer scheme is shown in Figure 3.

\(^4\) This is a result of the 250 ns internal ADCs conversion time.
3.3.1. Fast outputs The VMM has several fast serial outputs that can be used in different applications:

- The Address in Real Time (ART). This is the address of the first fired channel with signal above threshold transmitted serially providing an external 160 MHz clock. The address is sent on every clock cycle of the bunch-crossing clock.
- Direct Data Outputs (DDO) for all 64 channels in parallel in one of five configurable formats: time-over-threshold (ToT), threshold-to-peak (TtP), peak-to-threshold (PtT), or a 10 ns pulse occurring at peak (PtP). The readout is achievable providing an external 160 MHz clock.

4. ADC architecture and performance
The VMM3a integrates three ADCs per channel. The 6-bit ADC is a single-stage conversion which digitizes the peak amplitude found. This available to a serial direct output per channel. Digital latency from the peak found to the leading edge of the 6-bit word is \( \sim 4 \) ns while the conversion itself takes \( \sim 50 \) ns including the channel reset.

The 10-bit and 8-bit ADCs are current mode, two stage conversion digitisers. The 10-bit provides information of the amplitude while the 8-bit, information on the timing through the TAC conversion. They can be compared to a digital thermometer. For eg. the 10-bit ADC while converting is compared to 1024 current sources. The first stage quickly selects (compatible with the 6-bit conversion mentioned above) one of the 64 macro-cells thereby defining the 6 upper bits. In the second stage, one of the 16 micro-cells is identified defining the precision 4 lower bits. The two-stage ADCs have the ability to cross macro-cells in case of misidentification. The minimum deadtime is dominated by the 10-bit ADC and is \( \sim 250 \) ns including the channel reset. The conversion deadtime is configurable up to \( \sim 480 \) ns and can be interrupted if the data from the 6-bit ADC is only needed and hence, decrease the effective dead-time. The architecture of the 10-bit ADC is shown in Figure 4.

The performance of the ADCs is not ideal though. It was measured by looking on the channel response while injecting an external accurate amount of charge. The performance was then calculated with the Differential Non Linearity (DNL) and the Integrated Non Linearity (INL) technique[9]. It was found that the ADC’s equivalent number of bits (ENOB) is \( \sim 8 \) for the 10-bit ADC.
Figure 4. Architecture of the 10-bit ADC. The input current is compared at the first stage with one of the 64 macro-cells while on the second stage is compared with the 16 micro-cells in the identified macro-cell.

5. Radiation tolerance
In the VMM3a there are three types of storage elements that require Single Event Upset (SEU) protection, the configuration registers, the state machine control logic and the L0 logic. To mitigate for SEU two techniques are used:

- Dual Interlocked Cells (DICE) for the protection of the configuration registers
- Triple Modular Redundancy (TMR) for the state machines and the L0 state machine
- Single-bit faults on data FIFOs are flagged by a parity bit which is registered in the FIFOs and transmitted outside while the FIFO resets

The ASIC has been tested for both SEU and Total Ionization Dose (TID) and satisfies the requirement of the NSW upgrade.

6. Performance with detectors
The performance of the VMM3 and 3a has been tested through several testbeam campaigns at CERN. The detectors used were resistive Micromegas prototypes of $10 \times 10 \text{cm}^2$ active area used in older analysis [10].

6.1. Noise measurement
In order to achieve a good signal to noise ratio (SNR), low noise level must be achieved. This is something very essential for the resistive Micromegas detectors especially for tracks under an angle and the presence of the magnetic field where the drifting electrons are spread in more readout channels. The left plot in figure 5 shows the simulated[5] percentage of the strip signal loss as a function of the equivalent threshold set. The right plot of Figure 5 shows the equivalent noise charge (ENC) as a function of the electronics gain setting in VMM. The effect of the detector capacitance is visible.

6.2. Calibration
Following the noise, the next important configuration is equalizing the individual channel discriminator level. As described in Section 2, the VMM has a global threshold setting driven by a 10-bit DAC. This discriminating level though may vary from channel to channel. In order to achieve a discrimination at exactly the same amount of input charge, each channel has an individual 5-bit DAC which is used to account for channel discriminating fluctuations at a level

5 The detector gain in simulation was assumed to be $10^4$ which is a figure easily achievable with resistive Micromegas detectors of this size.
Figure 5. Left: The percentage of the simulated signal loss as a function of the discriminated equivalent charge from a random strip within a cluster. The simulation was performed for incident particles traversing the detector plane under 30° and detector gain of $\sim 10^4$. Right: Equivalent noise charge in electron units as a function of the electronics gain in mV/fC. The measurement is shown for the VMM channel floating and attached to the small Micromegas prototypes.

Figure 6. The 5-bit DAC range as a function of the VMM channels. A common discrimination level is found and indicated with red-dots.

To precisely measure the drift time of the ionizing electrons, the TAC must be calibrated. This operation is per channel allowing to transform the measured ADC counts in a meaningful time unit. To perform this type of calibration, an internal pulse is driven by a clock which has a fixed relation with the bunch crossing clock. By configuration, this relation varies in steps of 1 ns. By performing multiple steps and measuring the TAC, the ADC-ns relation is extracted. This method takes into account any time-walk introduced at peak finding. Figure 7 shows a diagram of the signals initiated during this calibration (left) as well as the TAC measured as a

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6 The TAC measures the peak or threshold crossing time with respect to the falling edge of the bunch crossing clock. The circuitry arms when a rising edge of the bunch crossing clock occurs.
function of channel. A good uniformity is shown. These calibration parameters are then used in the analysis of the data.

![Timing diagram of the TAC calibration with the injection of an internal to VMM charge circuit (pulser). Right: The TAC acquired value as a function of the channel in VMM. The TAC duration was set to 100 ns.](image)

**Figure 7.** Left: Timing diagram of the TAC calibration with the injection of an internal to VMM charge circuit (pulser). Right: The TAC acquired value as a function of the channel in VMM. The TAC duration was set to 100 ns.

6.3. Results

After careful calibration of the ASICs, the data analysis is performed. This is done using the charge centroid method for particles traversing the detector perpendicularly and using pattern recognition with the µTPC technique for particles traversing the detector plane under an angle [5]. The analysis was performed with two resistive Micromegas detector prototypes. On each detector, a space point is reconstructed depending on the angle conditions mentioned above. The residual distribution is shown in Figure 8 for both perpendicular tracks (left) and tracks under an angle of 30° (right) respectively. The distributions are fit with two Gaussian distributions of the same mean to account for the tails. The resolution is derived by dividing the result with $\sqrt{2}$ since the detectors are identical.

![Spatial resolution as acquired in the testbeam with small resistive Micromegas prototypes at CERN. The resolution for perpendicular tracks is shown on the left while the one obtained for tracks under 30° is shown on the right.](image)

**Figure 8.** The spatial resolution as acquired in the testbeam with small resistive Micromegas prototypes at CERN. The resolution for perpendicular tracks is shown on the left while the one obtained for tracks under 30° is shown on the right.
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References

[1] CERN (ATLAS Collaboration) (2008) JINST 3 S08003
[2] CERN (ATLAS Collaboration) (2013) New Small Wheel Technical Design Report CERN-LHCC-2013-006. ATLAS-TDR-020 (Geneva)
[3] Alexopoulos T et al. (2011) Nucl. Instrum. and Methods A 640 110 – 118 ISSN 0168-9002
[4] Abusleme A et al. (2016) Nucl. Instrum. and Methods A 817 85 – 92 ISSN 0168-9002
[5] Iakovidis G (2014) Research and Development in Micromegas Detector for the ATLAS Upgrade Ph.D. thesis Natl. Tech. U., Athens
[6] De Geronimo G and Li S (2011) IEEE Transactions on Nuclear Science 58 2382–2390
[7] De Geronimo G et al. (2013) IEEE Transactions on Nuclear Science 60 2314–2321
[8] De Geronimo G et al. (2007) IEEE Transactions on Nuclear Science 54 541–548
[9] (2011) IEEE Std 1241-2010 (Revision of IEEE Std 1241-2000) 1–139
[10] Alexopoulos T et al. (2019) Nucl. Instrum. and Methods A 937 125 – 140