A compact hybrid envelope tracking supply modulator with wide-band high-slew-rate linear amplifier

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Abstract This paper presents a compact implementation of a switch-linear hybrid envelope tracking supply modulator (HETSM). By combining transconductance-enhanced method and nonlinear current mirror technique in the operational transconductance amplifiers (OTAs), the proposed linear amplifier (LA) which utilizes the OTAs with class AB output stage achieves improved gain bandwidth and boosted slew-rate without increasing quiescent current. A good stability can also be attained without using any on-chip and off-chip compensation capacitors. The proposed LA facilitates the HETSM to achieve fast tracking with reduced chip area. An HETSM using the proposed LA in parallel with a hysteretic buck converter has been fabricated in 0.18-μm 1.8/5 V CMOS process with 1.24 mm\textsuperscript{2} die size. The measured results show that the HETSM is able to track a 10 MHz LTE signal accurately with less than 1.5% output error, achieving the maximum efficiency of 83% at 1W output power with 5 Ω resistive load. The HETSM can accommodate the variation of loading from 5 Ω to 20 Ω.

Keywords: linear amplifier (LA), operational transconductance amplifier (OTA), bandwidth, slew-rate, envelope tracking (ET), supply modulator

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

The envelope tracking supply modulator (ETSM) is widely used to track the envelope voltage of the RF signal and provide the supply voltage for power amplifiers (PAs)\cite{1, 2, 3, 4}. Conventionally, either linear regulators or switching regulators can be utilized as supply modulators. However, both types of regulators fail to simultaneously realize the large bandwidth and the high efficiency that are critical requirements for an ETSM\cite{5, 6, 7}. To balance the bandwidth and the efficiency effectively, the hybrid envelope tracking supply modulator (HETSM) combing the linear amplifier (LA) and the switching converter has been proposed, while various HETSMs have also been reported to enhance the envelope tracking (ET) PA system’s efficiency and linearity\cite{8, 9, 10, 11, 12, 13}.

In a HETSM, the linear amplifier should meet some requirements, such as a large bandwidth, a high slew-rate and a sufficient DC gain, to track the envelope voltage effectively\cite{14, 15, 16, 17}. Moreover, to drive the low equivalent resistance of PA and adapt to the load change from PA, a large driving capability and a good stability are also critical for a linear amplifier.

Usually, a linear amplifier is implemented by a folded-cascode structure with a class AB output stage to achieve the high DC gain and good driving capability\cite{18, 19}. But, more quiescent current (I\textsubscript{Q}) is often required to get the large bandwidth and high slew-rate, which unavoidably degrades the efficiency of the HETSM. Furthermore, a miller compensation network is generally used to stabilize the circuit to accommodate the load variation from PA\cite{19, 20}. However, the compensation capacitor has to consume large area to ensure stable operation. Recently, some LAs have been reported for HETSMs. In Ref.\cite{21}, OTA with the parallel combined class-AB output stage is applied in the LA to achieve large loop bandwidth. But, it may not improve the slew-rate of the LA. In Ref.\cite{22}, the LA utilizes OTA with parallel slew-rate enhancement (SRE) circuits to track wide-band signal. However, the class-AB bias adjustment circuit is needed to avoid the risk of distortion while the SRE circuit is turned on. This increases the design complexity.

In Ref.\cite{23}, adaptive biasing, gain enhanced current-mirror OTA is utilized in the LA. Although the bandwidth and slew-rate are increased, the quiescent current consumption needs to be further decreased. Therefore, most previously reported LA for the HETSM failed to achieve large bandwidth, high slew-rate, small I\textsubscript{Q}, small area and wide load range simultaneously.

Motivated by the above concerns, an enhanced LA is proposed in this paper. The implementation of HETSM utilizing the proposed LA in parallel with a hysteretic buck converter is also presented. The HETSM features compact design, good tracking performance, high efficiency and wide load range concurrently. This article is organized as follows: the circuit design considerations are given in Section 2, while the measurement results shown in Section 3 to verify the design. The conclusions are drawn in Section 4.

2. Circuits design consideration

2.1 Proposed linear amplifier

As shown in Fig. 1, in the HETSM, the wide-band LA behaves as a voltage source to provide a voltage output, which is an amplified replica of the input voltage, to ensure high accuracy of the output signal. In this paper, the LA with enhanced performance is constructed by two operational transconductance amplifiers (OTAs), a class AB output stage and two resistors R\textsubscript{1} and R\textsubscript{2}, as shown in Fig. 2 (a). The R\textsubscript{PA} and C\textsubscript{PA} are the equivalent resistance and capacitance of PA load for the LA.

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The DC gains of the OTA, the class AB stage, and the LA are defined as \( A_{V,\text{OTA}} \), \( A_{V,\text{ClassAB}} \), and \( A_{V,\text{LA}} \) respectively. The \( A_{V,\text{LA}} \) can be expressed as

\[
A_{V,\text{LA}} = A_{V,\text{OTA}} \cdot A_{V,\text{ClassAB}},
\]

and \( A_{V,\text{ClassAB}} \) is given by

\[
A_{V,\text{ClassAB}} = (g_{mp} + g_{mn})(R_{PA}/r_{op}/r_{on}) \\
\approx (g_{mp} + g_{mn})R_{PA}.
\]

Here, \( g_{mp} \) (\( g_{mn} \)) is the conductance of \( M_p \) (\( M_n \)), \( r_{op} \) (\( r_{on} \)) is the output resistance of \( M_p \) (\( M_n \)) which is much larger than \( R_{PA} \).

In the ET application, as the HETSM provides large biasing current to the PA, the size of power device \( M_{PN} \) is large, and the dominant pole existing at the gate of \( M_{PN} \) is expressed by

\[
\omega_p = \frac{1}{R_{\text{OUT,OTA}} \cdot C_{G_{MP,N}}} \\
\approx \frac{1}{R_{\text{OUT,OTA}} \cdot C_{G_{MD,PN}} \cdot A_{V,\text{ClassAB}}}
\]

where \( R_{\text{OUT,OTA}} \) is the output resistance of the OTA and \( C_{G_{MP,N}} \) is the equivalent capacitance at the gate of \( M_{PN} \). The second pole is the output pole and is given by

\[
\omega_{p1} = \frac{1}{R_{PA} \cdot C_{PA}}.
\]

In the case of small \( R_{PA} \), as the output pole is far away from the dominant pole, the stability is good. With the increase of \( R_{PA} \), the output pole is moved to a lower frequency, additional miller capacitance are usually needed to ensure the stability which occupies large area [24].

In the proposed LA, to accommodate the variation of \( R_{PA} \) from 5 \( \Omega \) to 20 \( \Omega \), \( R_1 \) and \( R_2 \) are included. First, \( R_2 \) is much larger than \( R_1 \), and the closed loop gain approximated to 1 is nearly not affected by the \( R_1 \) and \( R_2 \). Second, for a large \( R_{PA} \) (eg. 10 \( \Omega \) < \( R_{PA} \) < 20 \( \Omega \)), \( R_1 \) can be set to be a higher value, the current of \( M_p \) and \( M_n \) can be reduced to save the current consumption of LA. Third, with higher \( R_1/R_2 \), \( g_{mp} \) and \( g_{mn} \) are decreased due to the less current of \( M_p \) and \( M_n \). Then the \( A_{V,\text{classAB}} \) can be reduced to ensure the stability in the case of a large \( R_{PA} \), and the additional miller compensation capacitor at the gate of \( M_{PN} \) is not needed. By using the topology, the unity gain bandwidth (UGBW) of the LA is given by

\[
\text{UGBW}_{LA} \approx \frac{G_{m,\text{OTA}}}{C_{G_{MD,MP,N}}},
\]

where \( G_{m,\text{OTA}} \) represents the equivalent transconductance of the OTA. And the slew-rate (SR) of the LA is expressed as

\[
\text{SR}_{LA} \approx \frac{I_{O,\text{MAX}}}{C_{G_{MD,MP,N}}},
\]

where \( I_{O,\text{MAX}} \) is the maximum output current of the OTA. With unchanged \( C_{GD} \) of \( M_{PN} \), the \( A_{V,LA} \), UGBW\(_{LA} \), and SR\(_{LA} \) described in Eq. (1), Eq. (5), Eq. (6) can be improved by using enhanced OTAs.

Considering the design for OTA, Fig. 2 (b) and Fig. 2 (c) show a conventional current-mirror OTA and an enhanced flipped voltage follower (FVF) based current-mirror OTA with local positive feedback in the proposed design. \( K_1 \) and \( K_2 \) are the mirror factors. Suppose \( I_b \) is much smaller than \( I_{\text{BIAS,LA}} \) (Fig. 2 (c)), the total current of the two OTAs are almost the same.

By comparing the two structures, the differences and benefits of the enhanced current-mirror OTA (Fig. 2 (c)) are summarized as follows. First, local positive feedback constituted by two cross-coupling transistors M3b and M4b are utilized. The impedance at \( X_2(Y_2) \) is boosted, the effective transconductance \( G_{m,\text{OTA}} \) and the \( A_{V,\text{OTA}} \) are increased, improving the UGBW\(_{LA} \) and the \( A_{V,LA} \). Second, the maximum output current \( I_{O,\text{MAX}} \) is increased to about \( K_2I_{\text{BIAS,LA}} \) if the transistors M3a (M4a) are biased at the saturation region (case I), improving the SR\(_{LA} \). Third, the flipped voltage follower (FVF) [25, 26] based current mirror, which consists of the transistors M9 (M10), M3a (M4a) and M5 (M6), can be used as a nonlinear current mirror to further enhance the \( I_{O,\text{MAX}} \) of the OTA (case II). By adjusting the W/L of M9 (M10), transistor M3a (M4a) is biased at the
Table I Performance comparison between the two OTAs

|                  | The conventional current-mirror OTA (Fig. 2 (a)) | The enhanced current-mirror OTA (Fig. 2 (c)) |
|------------------|-------------------------------------------------|---------------------------------------------|
| $g_{m,OTA}$      | $K_1 \frac{K_2}{1+K_1 g_{m,2}}$                | $K_1 \frac{K_2}{1+K_1 g_{m,2}}$            |
| $A_{V,OTA}$      | $K_1 \frac{K_2}{1+K_1 g_{m,2}}$                | $K_1 \frac{K_2}{1+K_1 g_{m,2}}$            |
| $I_{O,MAX}$      | $\frac{K_1}{1+K_1} I_{Bias,LA}$                | $\frac{K_1}{1+K_1} \frac{I_{Bias,LA}}{2 I_{a,MAX}} V_{OUT,LA}$ (Case I) |
|                  |                                                 | $\frac{K_1}{1+K_1} \frac{I_{Bias,LA}}{2 I_{a,MAX}} V_{OUT,LA}$ (Case II) |

Fig. 3 Frequency responses of $V_{OUT}$ in LA [A] and LA [B] with 8 $\Omega$ $R_{PA}$.

Fig. 4 Step responses of $V_{OUT}$ in LA [A] and LA [B] with 8 $\Omega$ $R_{PA}$.

boundary of the triode region. While the slewing occurs, a large current $I_{BIAS,LA}$ is injected into transistor M3a (M4a), forcing it into triode region. At this time, $I_{O,MAX}$ has been largely increased, further enhancing the $SR_{LA}$.

Table I gives a summary of performance comparison between the two OTAs. In Table I, $g_m$, $r_o$ and $\beta$ are the transconductance, the output resistance and the process transconductance parameter of a transistor respectively. With the higher $K_1$, the boosting factor of UGBW and SR are increased while the phase margin (PM) is degraded. To balance the performance boosting and the system stability, $K_1$ is set to 1/4 and the transistors M3a (M4a) are biased near the triode region.

For comparison, two LAs (LA[A] and LA[B]) with the topology shown in Fig. 2 (a) are designed and simulated on the 0.18 $\mu$m CMOS process. Two conventional current mirror OTAs are used in LA[A], while the two enhanced OTAs are adopted in LA[B]. Fig. 3 and Fig. 4 show the simulated frequency responses and step responses of the two LAs with 150 pF $C_{PA}$. The results are summarized in Table II. In comparison with the LA[A], the UGBW and the SR in the proposed LA[B] have been increased by 1.7 times and 1.5 times respectively. The LA[A] and LA[B] consume the same amount of quiescent current which is 12 mA. The frequency response of the LA[B] with different values of $R_{PA}$ is given in Fig. 5. The results show that with 20 $\Omega$ $R_{PA}$, the PM of the LA is still larger than 50 degree. The proposed LA can accommodate the variation of $R_{PA}$ from 5 $\Omega$ to 20 $\Omega$.

Table III summarizes the comparison of simulated results between the proposed LA and some prior LAs utilized in different HETSMs. Compared with the LA in Ref. [23], the proposed LA achieves higher UGBW and SR with smaller current consumption. By consuming less AB bias current, the proposed LA also has a larger UGBW than the LA in Ref. [21]. Although the LA in Ref. [22] has a higher UGBW and SR, the $I_Q$ is not given. Besides, it uses 65 nm CMOS technology which is around a third of 180 nm CMOS technology used for our design. The smaller technology size makes it easier to get a larger UGBW and SR for the LA due to the smaller parasitic capacitance.

### 2.2 Switching buck converter

As shown in Fig. 1, in the HETSM, the switching buck converter behaves as a current-controlled current source to provide output current and handle the majority of the envelope power [27, 28]. By sensing the current flowing out...
Table IV Comparison with prior HETSMs

| Design       | Die Function | HETSM Topology         | Process (µm) | Max. VDD (V) | Signal Bandwidth (MHz) | PAPR (dB) | Max. Power(W) | Die Area(mm²) | Max. Efficiency (%) |
|--------------|--------------|------------------------|--------------|--------------|-------------------------|-----------|--------------|---------------|--------------------|
| [8] JSWC2016 | ET           | Hybrid with SCCI control | 0.13         | 1.2          | LTE 10 (Simulated)      | N/A       | 0.2          | 1.8           | 81                 |
| [13] ISSC2017| ET           | Hybrid with PED control | 0.5          | 4            | LTE 10                  | N/A       | 2            | 2.34 (core area) | 82                 |
| [21] MTT2017 | ET           | Hybrid with hysteretic control | 0.18         | 3.6          | LTE 10                  | 7.24      | 1            | 1.1 (core area)  | 83                 |
| [21] MTT2019 | ET and APT   | Combined Series-Parallel Hybrid with hysteretic control | 0.13         | 4.6          | LTE 1.4/5/10/20         | 5.8       | 0.8          | 5             | 88.2@1.4MHz, 81@5MHz, 80@10MHz, 78@20MHz |
| [22] MTT2019 | ET           | Hybrid with hysteretic control | 0.065        | 2.4          | LTE 40/60              | 7.84      | 1            | 2.72          | 95@40MHz, 91@20MHz |
| This work    | ET           | Hybrid with hysteretic control | 0.18         | 4.2          | LTE 10                  | 6         | 1            | 1.24, 0.78 (core area) | 83                 |

Fig. 6 (a) Simplified schematic of the hysteresis comparator, (b) simplified schematic of the switching driver and power transistors.

Fig. 7 (a) Die photo (1.55 × 0.8 mm²), (b) test board with off-chip inductor and resistive load.

The proposed HETSM was implemented in 0.18-µm 1.8/5 V CMOS process, and the die photo of the proposed HETSM is shown in Fig. 7 (a). Since the HETSM features simple implementation and does not require any area-consuming on-chip compensation capacitors, the die only occupies 1.55 × 0.8 mm² including all pads. The core area of the chip is around 0.78 mm². The HETSM test board with off-chip inductor is shown in Fig. 7 (b).

The 10 MHz LTE envelope signal with 6 dB PAPR is used as the input signal. Similar to other designs [8, 10, 21, 22] and [23], the modulator is characterized with resistive load resembling the supply node impedance of a PA. The measured input and output waveforms of the HETSM with RPA = 8 Ω is shown in Fig. 8. The output envelope voltage can follow the input envelope voltage accurately with high output voltage swing (3 V). The output ripple is less than few millivolts with 4.7 µH inductor. The HETSM is measured with different resistive loads from 5 Ω to 20 Ω. Fig. 9 shows the efficiency and output error versus output power. The maximum efficiency of the HETSM is 83% with 5 Ω resistive load at 1 W output power with VDD = 3.8 V. The maximum output error is only 1.5%.

Table IV summarizes the performance comparison between this work and references. Compared with de-
signs [8, 10, 22] and [23], the modulator in this paper provides the similar ET function with the smallest die size. The measurement results show that when tracking 10 MHz LTE signal, the presented HETSM achieves a high maximum efficiency of 83%. Although the HETSM in design [22] can track 80 MHz LTE signal with high efficiency, the three-level buck converter which provides a high percentage of power amplifier (PA) supply load current with lower ripple greatly improves the system efficiency of the modulator. The 65 nm technology with lower supply voltage also helps the HETSM in design [22] to get a faster tracking response.

4. Conclusion

In this work, a compact HETSM utilizing transconductance and slew-rate enhancement for the linear amplifier is presented. The proposed LA design achieves 1.7 times improvement in UGBW and 1.5 times enhancement in slew-rate. The design has been fabricated in a 0.18 μm 1.8/5 V CMOS process, while the experimental results show that the area-efficient HETSM with the proposed LA features wide bandwidth (10 MHz), high efficiency (max. 83%), high fidelity (<1.5% output error), wide load range (5 Ω to 20 Ω), and can potentially be used to improve the performance of ET PAs.

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References

[1] P. Asbeck and Z. Popovic: “ET comes of age: envelope tracking for higher efficiency power amplifiers,” IEEE Microw. Mag. 17 (2016) 16 (DOI: 10.1109/MMM.2015.2505699).
[2] D. Kimball, et al.: “High efficiency envelope tracking power amplifiers for wide modulation bandwidth signals (invited),” Asia-Pacific Microwave Conference (APMC) (2014) 103.
[3] B. Kim, et al.: “Push the envelope: design concepts for envelope tracking power amplifiers,” IEEE Microw. Mag. 14 (2013) 68 (DOI: 10.1109/MMM.2013.2340851).
[4] X. Liu, et al.: “A 2.4V 23.9dBm 35.7%-PAE 32.1dBc-ACLR LTE-20MHz envelope-shaping-and-tracking system with a multiloop-controlled AC-coupling supply modulator and a mode-switching PA,” ISSCC Dig. Tech. Papers (2017) 38 (DOI: 10.1109/ISSCC.2017.7870249).
[5] J. Sankman, et al.: “Switching-converter-only multipe phase envelope modulator with slew rate enhancer for LTE power amplifier applications,” IEEE Trans. Power Electron. 31 (2016) 817 (DOI: 10.1109/TPEL.2015.2460710).
[6] J. Kim, et al.: “Envelope tracking two-stage power amplifier with dual-mode supply modulator for LTE applications,” IEEE Trans. Microw. Theory Techn. 61 (2013) 543 (DOI: 10.1109/TMTT.2012.2225532).
[7] X. Ruan, et al.: “A review of envelope tracking power supply for mobile communication systems,” CPSS Trans. Power Electron. Appl. 2 (2017) 277 (DOI: 10.24295/CPSTPEA.2017.00026).
[8] M. Tan, et al.: “An efficiency-enhanced hybrid supply modulator with single-capacitor current-integration control,” IEEE-I Solid-State Circuits 51 (2016) 533 (DOI: 10.1109/ISSCC.2015.2490224).
[9] D. Chowdhury, et al.: “A fully integrated reconfigurable wideband envelope-tracking SoC for high-bandwidth WLAN applications in a 28nm CMOS technology,” ISSCC Dig. Tech. Papers (2017) 34 (DOI: 10.1109/ISSCC.2017.7870247).
[10] S. Yang, et al.: “A single-inductor dual-output converter with linear-amplifier-driven cross regulation for prioritized energy-distribution control of envelope-tracking supply modulator,” ISSCC Dig. Tech. Papers (2017) 36 (DOI: 10.1109/ISSCC.2017.7870248).
[11] S.C. Lee, et al.: “A hybrid supply modulator with 10dB ET operation dynamic range achieving a PAE of 42.6% at 27.0dbm PA output power,” ISSCC Dig. Tech. Papers (2015) 42 (DOI: 10.1109/ISSCC.2015.7062916).
[12] J. Kim, et al.: “Wideband envelope amplifier for envelope-tracking operation of handset power amplifier,” 2014 IEEE European Microwave Integrated Circuit Conference (EuMIC) (2014) 1532 (DOI: 10.1109/EmAccess.2014.6986695).
[13] P.Y. Wu and P.K.T. Mok: “A two-phase switching hybrid supply modulator for RF power amplifiers with 9% efficiency improvement,” IEEE J. Solid-State Circuits 45 (2010) 2543 (DOI: 10.1109/JSSC.2010.2076510).
[14] J. Kim, et al.: “Highly efficient RF transmitter over broad average power range using multilevel envelope-tracking power amplifier,” IEEE Trans. Circuits Syst. I, Reg. Papers 62 (2015) 1648 (DOI: 10.1109/TCSI.2015.2427711).
[15] J. Ham, et al.: “CMOS power amplifier integrated circuit with dual-mode supply modulator for mobile terminals,” IEEE Trans. Circuits Syst. I, Reg. Papers 63 (2016) 157 (DOI: 10.1109/TCSI.2015.2512703).
[16] M. Hassaan, et al.: “A combined series-parallel hybrid envelope amplifier for envelope tracking mobile terminal RF power amplifier applications,” IEEE J. Solid-State Circuits 47 (2012) 1185 (DOI: 10.1109/JSSC.2012.2184639).
[17] M. Hassan, et al.: “High efficiency envelope tracking power amplifier with very low quiescent power for 20 MHz LTE,” IEEE Radio Freq. Integr. Circuits (RFIC) Symp. (2011) 131 (DOI: 10.1109/RFIC.2011.5940618).
[18] R. Wu, et al.: “High efficiency silicon-based envelope-tracking power amplifier design with envelope shaping for broadband wireless appli-
cations,” IEEE J. Solid-State Circuits 48 (2013) 2030 (DOI: 10.1109/JSSC.2013.2265501).

[19] W. Chu, et al.: “A 10 MHz bandwidth, 2 mV ripple PA regulator for CDMA transmitters,” IEEE J. Solid-State Circuits 43 (2008) 2809 (DOI: 10.1109/JSSC.2008.2005743).

[20] R. Shrestha, et al.: “A wideband supply modulator for 20 MHz RF bandwidth polar PAs in 65 nm CMOS,” IEEE J. Solid-State Circuits 44 (2009) 1272 (DOI: 10.1109/JSSC.2009.2014730).

[21] J.-S. Paek, et al.: “Design of boosted supply modulator with reverse current protection for wide battery range in envelope tracking operation,” IEEE Trans. Microw. Theory Techn. 67 (2019) 183 (DOI: 10.1109/TMTT.2018.2879323).

[22] P. Mahmoodi-daryan, et al.: “Wideband hybrid envelope tracking modulator with hysteretic-controlled three-level switching converter and slew-rate enhanced linear amplifier,” IEEE J. Solid-State Circuits 54 (2019) 3336 (DOI: 10.1109/JSSC.2019.2941014).

[23] Y. Jing and B. Bakkaloglu: “A high slew-rate adaptive biasing hybrid envelope tracking supply modulator for LTE applications,” IEEE Trans. Microw. Theory Techn. 65 (2017) 3245 (DOI: 10.1109/TMTT.2017.2678476).

[24] J.N. Kitchen, et al.: “Combined linear and Δ-modulated switch-mode PA supply modulator for polar transmitters,” ISSCC Dig. Tech. Papers (2009) 82 (DOI: 10.1109/ISSCC.2007.373598).

[25] A.J. Lopez-Marin, et al.: “Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency,” IEEE J. Solid-State Circuits 40 (2005) 1068 (DOI: 10.1109/JSSC.2005.845977).

[26] Y. Kim and S. Lee: “Low power high-gain class-AB OTA with dynamic output current scaling,” IEICE Electron. Express 10 (2013) 20130042 (DOI: 10.1587/elex.10.20130042).

[27] D. Kim, et al.: “Highly efficient dual-switch hybrid switching supply modulator for envelope tracking power amplifier,” IEEE Microw. Wireless Compon. Lett. 22 (2012) 285 (DOI: 10.1109/LMWC.2012.2197382).

[28] D. Chen, et al.: “An asynchronous dual switch envelope tracking supply modulator with 86% efficiency,” IEICE Electron. Express 15 (2018) 20180206 (DOI: 10.1587/elex.15.20180206).

[29] R. Gregorian: “Comparators,” in Introduction to CMOS OP-AMPs and Comparators (Wiley, New York, 1999) 192.

[30] J. Choi, et al.: “A polar transmitter with CMOS programmable hysteretic-controlled hybrid switching supply modulator for multi-standard applications,” IEEE Trans. Microw. Theory Techn. 57 (2009) 1675 (DOI: 10.1109/TMTT.2009.2021880).