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A Low Power CMOS Phase Frequency Detector in High Frequency PLL System

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Abstract. The design of low power consumption for the different application and electronic product has become one of the challenges in high performance of Very Large Scale Integration (VLSI) design today. Therefore, many techniques have been introduced to minimize the power consumption and one of the technique is by using Multi-threshold Complementary Oxide Semiconductor (MTCMOS) power gating technique. This paper aimed to design a High Speed Phase Frequency Detector (HSPFD) using MTCMOS power gating technique implemented in 130 nm CMOS technology by using Cadence Virtuoso Tool. This design achieved a power consumption of 0.116 µW and frequency of 1.26 GHz. The result shows that the power consumption of HSPFD with MTCMOS power gating technique achieved about 67.14% smaller than conventional HSPFD while the frequency improved about 26%. The total area of the proposed HSPFD is 1423 µm² (61.100 µm x 23.290 µm). It can be conclude that, this design has better performance compared to previous work and it is suitable for applications like wireless communication system that need low power blocks to have long life battery.

1. Introduction

The rapid growth of electronic system has contributed to the use of Phase Locked Loops (PLL) as one of the inevitable necessities in modern days. It has been used as a part of digital system and communication system like wireless and wire-line [1]. PLL is widely used in many application such as clock generation and clock recovery in microprocessor, networking, communication system and frequency synthesizers. PLL basically consists of Phase Frequency Detector (PFD), Charge Pump (CP) and Loop Pass Filter (LPF) and Voltage Control Oscillator (VCO). Figure 1 shows the block diagram of PLL system where in the PFD, the phase of feedback signal from VCO with the input reference signal is compared and then it generate up or down output according to the phase difference. While for CP, it charges or discharges the capacitor of the low pass filter according to up or down signal from PFD and the VCO will increases or decreases the output frequency according to the control voltage that produced by the CP.
Complementary Metal Oxide Semiconductor (CMOS) technology offer a PFD design in smaller scale design with low power consumption and low area which able to perform in higher frequency with a lower power consumption. This paper focus on the Phase Frequency Detector (PFD) where it is one of the important block in PLL system. The PFD have two inputs that are clock reference (CLK\textsubscript{REF}) and clock from voltage control oscillator (CLK\textsubscript{VCO}) where the first input is from the reference clock and second input is from the feedback signal that coming from VCO. PFD also have two outputs known as UP and DOWN signal according to the phase and frequency difference of the input signals. The result of the PFD output were connected to the charge pump to generate the related control signal for VCO. Figure 2 shows a block diagram of PFD with its inputs and outputs.

This paper is divided into four sections and organized as follow. In Section 2, the HSPFD MTCMOS with power gating architecture is discussed. In Section 3, the simulation results and discussion for the findings is presented. Finally, the conclusion is in Section 4.
2. HSPFD MTCMOS with power gating architecture

The conventional HSPFD architecture consists of D Flip-flop, two inverter and NAND gate are used to reduce the power consumption and achieved the high speed by detecting the rising and falling edges of the input signals. The proposed HSPFD is using the MTCMOS power gating technique where two sleep transistors are applied between the supply voltage and ground line known as power gating. The MTCMOS technique provides a simple and effective power gating structure by utilizing high speed, low threshold voltage ($L_{Vt}$) transistors for logic cells and low leakage, high threshold voltage ($H_{Vt}$) devices as sleep transistors. Sleep transistors disconnect logic cells from the supply and/or ground to reduce the leakage in the standby mode [20]. This technique is based on disconnecting the $L_{Vt}$ logic gates from the power supply and the ground line via cut-off $H_{Vt}$ sleep transistor. The transistor that having low threshold voltage are used to isolate the low threshold voltage transistors from supply and ground during standby (sleep) mode to prevent leakage dissipation. While in the active mode, sleep transistor are turned on and the logic that consists of $L_{Vt}$ transistors can operate with high speed and low switching power dissipation. When the circuit is in sleep mode, the $H_{Vt}$ transistors are turned off causing isolation of $L_{Vt}$ transistors from supply voltage and ground and therefore it reduced the sub-threshold leakage currents [12]. Figure 3 shows the HSPFD MTCMOS with power gating technique.

![Figure 3. The proposed HSPFD MTCMOS with power gating technique.](image-url)
3. Result and Discussion

The simulation of HSPFD MTCMOS with power gating technique circuit was carried out in Cadence Virtuoso with supply voltage of 1.2 V and load capacitance of 1 pF.

The power consumption of the proposed HSPFD circuit is 0.116 µW with the frequency of 1.26 GHz. The peak-to-peak high and bottom peak were measured in these three condition that are in lock condition, when CLK leading condition and when CLKREF leading condition. In Figure 4(a), during lock condition, the value of peak-to-peak high and bottom peak measured are same that is 1.193 V. During CLKREF leading condition in Figure 4(b), the value of peak-to-peak high and bottom peak of UP output is slightly higher compared to DOWN output which is 1.229 V and 1.205 V while peak-to-peak high for DOWN output is 1.212 V. In CLK leading condition shown in Figure 4(c), the result of peak-to-peak high and bottom peak measured is vice versa from the CLKREF condition where the DOWN output has higher value of peak-to-peak high and bottom peak that is 1.229 V and 1.205 V while the UP output has the value peak-to-peak high measured is 1.212 V. This is happen due to the active and inactive mode of sleep transistor that has been explained in section 2. The layout of proposed circuit is 1423 µm² (61.1100 µm x 23.290 µm) is shown in Figure 5.

Table 1 tabulated the comparison of different low power technique together with the proposed design done that is HSPFD MTCMOS with power gating technique in this project. Based on the table, the proposed design measured the least power consumed in the HSPFD among other design. About 67.14% of power consumption of the HSPFD with MTCMOS using power gating technique is improved compared to the conventional HSPFD technique [17]. The frequency also improved about 26% compared to the conventional HSPFD technique [17] that achieved about 1 GHz only. This also proves that with smaller CMOS technology scale, lower power consumption can be achieved.

![Figure 4 (a). HSPFD MTCMOS with power gating waveform at lock condition.](image)
Figure 4 (b). HSPFD MTCMOS with power gating waveform at CLK\text{REF} leading condition.

Figure 4 (c). HSPFD MTCMOS with power gating waveform at CLK\text{VCO} leading condition.
Table 1. Summarization of proposed HSPFD with previous HSPFD technique.

| Authors | Techniques | Technology (nm) | Power (µW) | Frequency (GHz) |
|---------|------------|-----------------|------------|-----------------|
| [17]    | Conventional HSPFD | 0.13            | 0.353      | 1               |
| [16]    | HSPFD       | 0.18            | 8.513      | 1               |
| [18]    | Conventional HSPFD | 0.35            | 0.39       | 1               |
| [14]    | Conventional PFD | 0.18            | 33.5       | 0.5             |
| Proposed Design | HSPFD MTCMOS | 0.13            | 0.116      | 1.26            |

Figure 5. Layout of HSPFD MTCMOS with power gating technique.
4. Conclusion

Minimization of low power consumption is essential for high performance of VLSI systems. A HSPFD MTCMOS with power gating technique has been described in this paper where it is proven that the design was able to get low power consumption of 0.116 $\mu$W and high frequency of 1.26 GHz that implemented in 130nm CMOS technology. Therefore, this is proved that the MTCMOS with power gating technique was able to improve overall performance in PFD design.

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