FLOWER POLLINATION ALGORITHM BASED CAD APPROACH FOR SUPPLY NOISE REDUCTION IN SYSTEM-ON-CHIP

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Abstract

Designing an efficient power distribution network is a major challenge in modern day system-on-chip. During manufacturing, the signal integrity problems such as resistive voltage drop, inductive noise at pad locations and electro-migration may result silicon failures. This paper deals with the analysis of supply noise using multiple power supply and use of decoupling capacitors for reduction of supply noise. In this work flower pollination algorithm has been used for decap estimation so that the supply noise can be reduced significantly and various design parameters remains at its best. The purpose of this work is to reduce the supply noise with effecting the other design parameters of the chip. In this work the supply noise has been reduced upto 70.2% with reduction of 81.6% in power consumption and 17.07 % increment in delay parameters. This approach can be used for any system-on-chip.

Keyword: Decoupling capacitor, Flower Pollination Algorithm, Multiple Power Supply, Power Distribution Network, System-on-chip.

I. Introduction

Use of multiple VDD is an area interest of modern day VLSI designers. Previous research works has shown that the power performance of the chip improves
considerably with the use of multiple VDD though it has its own design constraints [VI], [X]. Multiple VDD design techniques generally used so that the supply voltage can be reduced. With decrease in supply voltage the dynamic power of chip decreases which improves the overall power performance. But with reduction in supply voltage reduces the threshold voltage due to which delay parameters of the chip increases. Also use of various multiple power supply (MPS) in system-on-chip (SoC) increases the overall design complexities. This design complexities are very challenging issues for modern day VLSI designers.

The popularity of digital circuits is largely due to associated noise immunity to physical noise sources such as flicker noise, thermal noise, shot noise and popcorn or burst noise. However, the high gains of digital circuits results in an alternate class of noise sources, having magnitude larger than the physical noise sources such as leakage noise, power supply noise, reflection noise and charge-sharing noise. These can be considered as “man-made” sources[IX]. Various types of pulse noise are supply noise, cross-talk noise and charge-sharing noise.

The wide acceptability of digital circuits is due to their associated noise immunity to such physical noise sources. Existing power distribution network (PDN) designs practice concerns like IR drop including crosstalk noise; they practically overlook the actual power loss in the network. The manufacturers are suffering the enduring trials of optimizing among power including performance, with high-performance mobile computing devices [VII], [VIII], [IX], [X].

Resonance is a component of supply noise that is gaining increasing importance in modern chips and is a noise source that must be factored into the voltage regulation specification of a chip.

As the on-chip capacitance, both inherent to the circuits and added decap, combine with the package inductance to form an LC-tank circuit. When excited by switching at the resonant frequency, this circuit can cause significant oscillations in the supply voltage. When insufficient resistance is present in the system to damp the oscillations, this noise can be persistent over multiple clock cycles and detrimental to the chip.

In this paper we have exploited the multiple VDD technique for various test circuits. Use of multiple VDD will improve the power performance but it can have an effect delay parameters. Simulation results shows that for multiple VDD there has been a considerable reduction in supply noise without having much effect on other design parameters i.e. propagation delay and power consumption.

Key contributions in this work are:
(i) Flower pollination algorithm (FPA) based computer aided design (CAD) implementation for noise suppression using decoupling capacitor (decap).

(ii) Analysis of reduction of supply noise, delay and power parameters with decap with multiple power supply.

The rest of the paper has been presented as follows. The various sources of supply noise has been briefly discussed in Section II. Decoupling capacitor estimation using FPA has been presented in section III. Simulation results and analysis has been presented in Section IV. In Section V the paper has been concluded.

II. Multiple VDD Based Power Distribution Network and Supply Noise-Aware

Multiple VDD based PDN topology is a challenging domain for the modern day VLSI designers. Reduction in operating voltage reduces the power performance as it decreases the dynamic power of the chip. But reduced VDD also reduces threshold voltage of the transistors which results in more gate delays. So it is important to balance between the power and the delay parameters.

Designing a multiple VDD based PDN is also a difficult task as the chip requires multiple VDDpins with much more power and ground line complexities. In this work we have used module wise VDD selection depending upon the packing density and also the current requirements. After estimating the power requirement of each module we have partitioned the chip into sub-modules and the VDD of that particular module has been estimated. The purpose is also to reduce the design complexities. More the number of VDD the more is the design complexity. Depending on the power requirements VDD parameter has been estimated with an aim to improve the power performance, to reduce the supply noise and also the delay parameters.

The primary sources of supply noise are the inductive and resistive elements present in the circuit. The inductive noise occurs in the pad locations and can be expressed by the expression [VIII]:

\[ \Delta V_L = L \cdot \frac{di(t)}{dt} \]  

(1)

The resistive noise generally occurs in the electrical wires and can be expressed as [VIII]:

\[ \Delta V_R = i(t) \cdot R \]  

(2)

The resistive, capacitive and inductive elements has a major effect on the functioning of SoC. The resistive component is mainly due the wiring length on the chip. With increase in length the IR drop increases which results in supply noise. Parasitic capacitance occurs between the power and ground lines and with the resistive
components it increases the overall delay and sometimes leads to failure of the chip. So implementing an efficient physical design has become a challenge for the modern day SoC designer [I], [II], [III], [V], [XII],[XIV],[XVI].

The signal integrity problems, such as IR-drop, ΔI noise, and electro-migration cause numbers of silicon failures. Circuits incorrect functioning and timing requirements mismatch are caused by IR-drop and ΔI noise while electro-migration may cause the damage circuit lifetime and logic failure of the chip.

III. Decap Estimation and Allocation

The focus of this work is the reduction of supply noise with a focus to keep the design parameters within acceptable limits. In this work we have used module-wise approach using multiple VDD to reduce the supply noise. Authors has shown the noise voltage swing can be kept within 50% by having a decap budget given by the formula [IV]:

$$C_{\text{decap}} = \frac{P}{VDD^2}$$  \hspace{1cm} (3)

where \(C_{\text{decap}}\) is the decap budget, \(P\) the total power consumption of the SoC, \(f\) the operating frequency and \(VDD\) the supply voltage.

The silicon area required for fabricating the decap can be estimated as [XIII]:

$$S_{\text{area}} = \frac{C_{\text{decap}}}{C_{\text{ox}}}$$  \hspace{1cm} (4)

\(C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}\), \(C_{\text{ox}}\) is MOS capacitance/ area, \(\epsilon_{\text{ox}}\) SiO\(_2\) permittivity and \(t_{\text{ox}}\) SiO\(_2\) thickness. Equation (3) and (4) gives the estimation and cost function of the decoupling capacitor.

In the previous research works to the best of our knowledge multiple power supply (MPS) have been used so that the supply voltage can further be reduced. This type of approach certainly improves the power performance of the chip but has an effect on delay and also increases the design and transistor complexities in the SoC[VI],[X]. To achieve more accurate results FPA has been used for decap estimation. Flower pollination algorithm works using global pollination and local pollination techniques as discussed in article[XI], [XV].

The concept of FPA can be summarized as [XV]:

\[\text{for } (i<n)\]

\[\text{global pollination: } x_i(t+1) = x_i(t) + L (x_i(t) - g),\]

where \(L=\) Levy's distribution and \(g=\)present best solution

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Partha Mitra et al
else

local pollination: \(x_i(t + 1) = x_i(t) + \epsilon \times (x_i(j) - x_i(k))\).

where \(x_i(j)\) and \(x_i(k)\) are pollens from different flower of same plant
and \(\epsilon\) = uniform distribution \([0,1]\).

Till termination continue iteration and accept the best set of solution.
end

Here, \(x(t) = \text{decap to be inserted and } g = \text{supply noise.}\)

Implementation of PDN for multiple VDD based integrated circuits is another
challenging task in the floorplan stage of the design. Modern day PDN in integrated
circuits uses 3-D structure for better implementation of physical design. In this work
modules with identical VDD has placed in the same metal layer.

The CAD approach in this work is described hereunder:
1. Verilog code to develop the SoC and functional verification
2. Multiple VDD allocated after partitioning of the SoC.
3. Netlist generated.
4. Modules are combined to form the SoC.
5. Reduction of supply noise, propagation delay and power consumption is estimated
   without allocation of decap.
6. Estimation and allocation of decap using expression [3] for individual modules.
7. Reduction of supply noise, propagation delay and power consumption is estimated
   for each module.
8. If results are satisfactory
9. Stop
10. else
11. for \((i<n)\)
12. global pollination: \(x_i(t+1) = x_i(t) + L \times (x_i(t) - g)\),
13. else
14. local pollination: \(x_i(t + 1) = x_i(t) + \epsilon \times (x_i(j) - x_i(k))\).
15. Till termination continue iteration and accept the best set of solution.
16. end

17. Estimation of supply noise, propagation delay and power consumption for the entire SoC.

IV. CAD Approach and Simulation Results

In this work we have considered 1-k point FFT core and International Test Conference 1999 (b14 and b17) as our test bench circuits. FFT core finds application in modern day digital communication systems. ITC99 (b14 and b17) are well defined test bench circuits and has been used in this work for experimental purpose. This work has been performed using both single VDD and multiple VDD.

The FFT core consists of input, memory blocks, address generator, twiddle factor, butterfly and control unit. Results of intermediate stages and twiddle factors are stored in memory block. Address generation block and control blocks are for overall operation on the processor.

Verilog Code is developed for implementation and functional verification in SYNOPSYS VCS platform for the test circuits. It is then imported into DESIGN COMPILER of SYNOPSYS platform to synthesize the design. Finally this design is implemented in CADENCE ENCOUNTER for the physical design stage. Then supply noise, propagation delay and power consumption without decap are estimated. Flower pollination algorithm has been used to estimate the decoupling capacitance and placed near each functional module. Next, reduction of supply noise, delay and power analysis are performed with decap allocation. For multiple VDD 1V, 0.8V and 0.5V operating voltage has been used for various functional modules depending on the current requirement with 1GHz switching frequency using TSMC 90nm technology. For single VDD 1V operating voltage with 1GHz switching frequency using TSMC 90nm technology has been used. The simulation results for single supply voltages and multiple supply voltages have been presented in the result tables.

Fig. 1: 1-K Point FFT core Architecture [IX]
Table 1: NOISE REDUCTION ANALYSIS USING MULTIPLE VDD

| Test Circuit | Noise without Decap (mV) | Noise With Decap (mV) | % Reduction Noise |
|--------------|--------------------------|-----------------------|-------------------|
| 1-k point FFT core | 0.45 | 0.16 | 64.4 |
| b14 | 0.47 | 0.14 | 70.2 |
| b17 | 0.63 | 0.19 | 69.8 |

Table 2: POWER ANALYSIS WITH DECAP

| Test Circuit | Single VDD (mW) | Multiple VDD (mW) | % Reduction Power |
|--------------|----------------|-------------------|-------------------|
| 1-k point FFT core | 203.1 | 46.3 | 77.2 |
| b14 | 228.4 | 42.3 | 81.6 |
| b17 | 833.8 | 212.5 | 74.5 |

| Reference [X] | ------- | ------- | 70 |
| Reference [VI] | ------- | ------- | 85.8 |

Table 3: DELAY ANALYSIS WITH DECAP

| Test Circuit | Single VDD (µsec) | Multiple VDD (µsec) | % Increment Delay |
|--------------|-------------------|---------------------|-------------------|
| 1-k point FFT core | 272.6 | 303.5 | 10.2 |
| b14 | 0.68 | 0.82 | 17.07 |
| b17 | 0.63 | 0.76 | 17.1 |

| Reference [X] | ---- | ---- | 22 |

From table I, supply noise has been reduced by 64.4%, 70.2% and 69.8% for 1-k point FFT core, b14 and b17 test circuits respectively. Table II shows that power consumption has been reduced by 77.2%, 81.6% and 74.5% for 1-k point FFT core, b14 and b17 respectively and has been compared with references [X] and [VI] where the power consumption has been reduced by 70% and 85.83%. Table III, shows that the increment in delay are 10.2%, 17.07% and 17.1% for 1-k point FFT core, b14 and b17 respectively. The increment in delay for reference [X] is 22%. 

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Partha Mitra et al
From the simulation results it has been observed that the supply noise has been reduced significantly. Also from the simulation results it is observed that delay performance of this work is much improved compared to previous research work. The power consumption in this work has also been reduced significantly. Overall the various design parameters of this work for all the test circuits are satisfactory.

V. Conclusion

The number of transistor count in modern day VLSI design has grown significantly. Propagation delay, power consumption and area are the major concerns for the VLSI designers. With very high packing density design and implementation of an efficient PDN is also becoming a challenging task. This leads to variation of voltages in the electrical nodes which results supply noise. Researches have developed various techniques for reduction of supply noise since this noise can lead to logic failures and malfunctioning of the chip.

In this work we have used multiple VDD technique and decaps are deployed to reduce the supply noise. With lowering of the supply voltages the power consumption decreases but increase the delay parameter. The focus of this work is to reduce the supply noise and the keep the various design parameters at its best. Experimental results show that noise and power consumption has been significantly, with a little increment in delay. The delay parameters in this work have improved significantly compared to previous research works.

Future work will focus on further analysis so that the noise and power consumption can further be reduced with having minimum effect on various design parameters.

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References

I. C. Tirumurti, S. Kundu, S. Sur-Kolay, Y. Chang, “A modeling approach for addressing power supply switching noise related failures of integrated circuits”, Proceedings of Design, Automation and Test in Europe Conference and Exhibition (DATE) pp.: 1078-1083, 2004.
II. J. A. Strak, H. Tenhunen, “Investigation of timing jitter in NAND and NOR gates induced by power- supply noise”, Proceedings 13th IEEE International Conference on Electronics, Circuits and Systems 2007.

III. K. Shah, “Power Grid Analysis in VLSI Designs”, Dissertation in Master of Science (Engineering), Super Computer Education and Research Centre, Indian Institute of Science Bangalore, 2007.

IV. K. Shimazaki, T. Okumura, “A Minimum Decap Allocation Technique Based on Simultaneous Switching for nano-scale SoC”. Proceedings of IEEE Custom Integrated Circuits Conference, 2009.

V. M. Khellah, D. Khalil, D. Somasekhar, Y. Ismail, T. Karnik, V. De, “Effect of power supply noise on SRAM dynamic stability”, Proceedings of Symposium on VLSI Circuits 2007.

VI. M. Musab, S. Yellampalli, “Study and Implementation of Multi-VDD Power Reduction Technique” Proceedings of IEEE International Conference on Computer Communication and Informatics (ICCCI), pp.: 1-4, 2015.

VII. M. Saint-Laurent, M. Swaminathan, “Impact of power-supply noise on timing in high frequency microprocessors”, IEEE Transactions on Advanced Packaging, Vol.:27, pp.: 135-144, 2004.

VIII. P. Mitra, J. Bhaumik, “Pre-Layout Decap Allocation for Noise suppression and Performance Analysis for 512-Point FFT core”, Proceedings of 2017 Devices for Integrated Circuits (DevIC), pp.: 341-345, 2017.

IX. P. Mitra, J. Bhaumik, “A CAD Approach for Suppression of Power Supply Noise And Performance Analysis of Some Multi-core Processors in Pre-layout Stage”, Microsystem Technologies, Springer, Vol.: 25, Issue: 5, pp.: 1977-1986, 2019.

X. S. A. Tawfik, V. Kursun, “Multi-Vth Conversion circuits For Multi-VDD Systems”, Proceedings of IEEE International Symposium on Circuits and Systems, pp.: 1397-1400, 2007.

XI. S. Ghosh., B. P. De, R. Kar, D. Mandal, A. K. Mal, “Optimal design of a 5.5GHz lowpower highgain CMOS LNA using the Flower Pollination Algorithm”. Journal of Computational Electronics, Springer 2019. DOI: 10.1007/s10825-019-01322-6
XII. S. Pant, “Design and analysis of Power Distribution Networks in VLSI Circuits”, Ph.D Dissertation, University of Michigan, 2008.

XIII. S. Zhao, K. Roy, C.K. Koh, “Decoupling Capacitance Allocation and Its Application to Power-Supply Noise-Aware Flooring”, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol.: 21, Issue: 1, pp.: 81-92, 2002.

XIV. T. Karim, “On-Chip Power Supply Noise: Scaling, Suppression and Detection”, Ph.D Dissertation, University of Waterloo, 2012.

XV. X.S. Yang, “Flower Pollination Algorithm for Global Optimization”, Lecture Notes In Computer Science, Springer, Vol. 7445, pp.: 240–249, 2012.

XVI. Y. Shi, J. Xiong, C. Liu, L. He, “Efficient Decoupling Capacitance Budgeting Considering Operation and Process Variations”, IEEE Trans. on CAD, Vol.: 27, Issue: 7, pp.: 1253-1263, 2008.