Radio Frequency Pulse Response of an In-Plane-Gate Field Effect Transistor

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Abstract. We report radio frequency responses of an in-plane-gate field effect transistor (IPGFET) using an electrical pulse and probe technique. A series of high frequency pulses with the frequency up to 3 GHz were superimposed on the DC gate bias, and the time-averaged drain current was measured. The frequency and amplitude dependence of the time-averaged current depended on both the intrinsic gate response time of the IPGFET and the charging/discharging time of the traps at the etched surface.

1. Introduction
There have been quite continuous efforts in the fabrication and characterization of in-plane-gate field effect transistors (IPGFETs) \cite{1-4}. One advantage of the IPGFET is simultaneous fabrication of an electron channel and in-plane gates by simply forming grooves on a HEMT wafer. Detailed DC characterization of IPGFETs have been done actively and new physics such as single electron transport \cite{4} and resonant tunneling \cite{5} have been found in quantum dot shaped IPGFETs. However, characterization of IPGFETs in radio-frequency (RF) regimes has rarely been reported except few works measuring S-parameters \cite{6}. This type of continuous wave measurement is not adequate for characterizing nano-sized devices since the change of the output signal due to those devices is usually much smaller than the background. To overcome such difficulties, electrical pulse and probe technique has been used recently \cite{7}.

This paper presents results of RF pulse measurements on an GaAs/AlGaAs IPGFET. Pulse signals with the frequency ($f$) up to 3 GHz and the amplitude ($V_{pp}$) reaching 3 V was superimposed on the DC gate bias and time-averaged drain current was measured. The measured spectrum as a function of the pulse $f$ and $V_{pp}$ was analyzed considering both the intrinsic gate response time and the dynamics of surface traps.

2. Measurement and result
Figure 1(a) shows a schematic experimental setup. The fabricated IPGFET was mounted on a microwave fixture with coplanar wave guides and the in-plane gates are wire-bonded to the coplanar waveguide. A series of RF pulse signals were superimposed on the DC gate bias ($V_{GS}$) using a bias tee and the time-averaged drain current ($I_{DS}^*$) was measured using a low noise preamplifier. The pulse $f$ ranged from 10 Hz to 3 GHz. Figure 1(b) shows the measured DC drain current ($I_{DS}$) as a function of $V_{GS}$, and the inset shows the transconductance. It shows a common FET characteristic with steep turn on/off. The maximum transconductance was 13.6 $\mu$S.

Figure 2 shows the measured $I_{DS}^*$ when RF pulses with $V_{pp} = 2$ V were applied on the IPGFET. The value of $V_{GS}$ was fixed at 0 V. Figure 2(a) shows the measured $I_{DS}^*$ in the range 10 Hz < $f$ < 40 MHz. The value of $I_{DS}^*$ increased as $f$ increased and then showed saturation at higher $f$. Figure 2(b) shows the measured $I_{DS}^*$ in the range 50 MHz < $f$ < 3 GHz. In this range, the value of $I_{DS}^*$ increased as $f$ increased and then showed a saturation to the DC value at higher $f$. Figure 2(c) shows the $I_{DS}^*$ as a function of $f$ in the whole range of $f$ and at the drain bias $V_{DS} = 2$ V. The dotted line denotes the value of $I_{DS}$. As $f$ increases, the $I_{DS}^*$ showed steep decrease when $f < 5$ kHz, saturation when several MHz < $f$ < 50 MHz, increase when 50MHz < $f$ < 1 GHz, and again saturation when $f > 1$ GHz.

When the gate perfectly responds to the pulse signal, the value of $I_{DS}^*$ is simply the average of the DC current value at pulse high ($V_{DS} + V_{pp}$) and pulse low ($V_{DS} - V_{pp}$).

$$I_{DS}^* = f \int_0^{1/f} I_D(V_{DS}(t))dt = \frac{1}{2}[I_D(V_{DS} + V_{pp}) + I_D(V_{DS} - V_{pp})]$$

The saturation of $I_{DS}^*$ to DC value at high frequency (> 1 GHz) occurs when the pulse period is shorter than the gate response time so that the gate bias remains at the DC value. The decrease and saturation of $I_{DS}^*$ at low $f$ is the dynamics of trap states at the etched surface.

Figure 2 (a) and (b) $I_{DS}^*$ at various values of the pulse $f$ ranging from 10 Hz to 40 MHz and from 50 MHz to 3 GHz, and (c) $I_{DS}^*$ as function of pulse $f$ at $V_{GS} = 0$ V, $V_{DS} = 2$ V and $V_{PP} = 2$ V.
Figure 3 shows schematic band diagrams of GaAs in the direction of the channel width at DC $V_{GS}$, right after the switching from pulse low to pulse high, and right after the switching from pulse high to pulse low. When the switching from pulse low to pulse high occurs, empty trap states move below the Fermi level ($E_F$). These states are occupied with electrons quickly since the electron channel is in the vicinity of traps. Then the current is the same as the DC current at the gate bias of pulse high. On the other hand, when the switching from pulse high to pulse low occurs, filled trap states move above $E_F$. It is difficult for the electrons in these states to relax back to the channel since the channel is far away. Therefore, the channel is narrower than when the same amount of DC bias is applied and the current is smaller.

![Figure 3 Schematic band diagrams at three different gate pulse conditions.](image)

According to our scenario of trap dynamics, $I_{DS}^*$ should be a strong function of $V_{pp}$. A larger $V_{pp}$ will move more trap states above $E_F$ and the decrease of the current will be larger. Figure 4 shows the measured $I_{DS}^*$ (red line), and calculated $I_{DS}^*$ (black line) using eq. (1), as a function of $V_{pp}$, at $V_{GS} = 0$ V and $V_{DS} = 2$ V. The frequency was fixed at 100 MHz much below the gate response time of the IPGFET. It shows a large decrease as $f$ increases, which is consistent with the scenario of Fig. 3.

![Figure 4 Measured $I_{DS}^*$ (red line), and calculated $I_{DS}^*$ (black line) using eq. (1), as a function of $V_{pp}$ when $f = 100$ MHz. The green line denotes the DC value.](image)

3. Conclusion
We report RF responses of our IPGFET using an electrical pulse and probe technique. A series of RF pulses with $f < 3$ GHz were superimposed on the DC gate bias, and the time-averaged drain current was measured. As $f$ increases, the $I_{DS}$ showed steep decrease when $f < 5$ kHz, saturation when several MHz $< f < 50$ MHz, increase when 50MHz $< f < 1$ GHz, and again saturation when $f > 1$ GHz. The behavior at high frequency is due to the intrinsic response time of the IPGFET. The behavior at low $f$ is consistent with the interpretation using charging/discharging of trap states at the etched surface.
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