A Non-Isolated High Step-Up Interleaved DC-DC Converter with Diode-Capacitor Multiplier Cells and Dual Coupled Inductors

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Abstract—In this paper, a non-isolated high step-up dc–dc converter is presented. The proposed converter is composed of an interleaved structure and diode-capacitor multiplier cells for interfacing low-voltage renewable energy sources to high-voltage distribution buses. The aforementioned topology can provide a very high voltage gain due to employing the coupled inductors and the diode-capacitor cells. The coupled inductors are connected to the diode-capacitor multiplier cells to achieve the interleaved energy storage in the output side. Furthermore, the proposed topology provides continuous input current with low voltage stress on the power devices. The reverse recovery problem of the diodes is reduced. This topology can be operated at a reduced duty cycle by adjusting the turn ratio of the coupled inductors. Moreover, the performance comparison between the proposed topology and other converters are introduced. The design considerations operation principle, steady-state analysis, simulation results, and experimental verifications are presented. Therefore, a 500-W hardware prototype with an input voltage of 30-V and an output voltage of 1000-V is built to verify the performance and the theoretical analysis.

Index Terms—Dual-coupled inductors, diode-capacitor cells, high step-up dc–dc converter, interleaved dc–dc converter, renewable energy systems.

I. INTRODUCTION

The environmental concerns, such as global warming, climate change and air pollution is becoming a critical public apprehension. Nowadays, renewable energy sources, such as photovoltaics (PVs) and fuel cell are promising alternative energy sources and extensively utilized in many applications. However, the output voltage of PV panels is low in the end stage and depends on the weather conditions, such as the change in temperature and solar irradiance. Power electronic converters play a vital role in power conversion of the distributed generation and the grid [1]. Thus, due to the aforementioned shortcoming, employing high step-up dc–dc converters plays a substantial role in increasing and regulating the low voltage of PV panels to high voltage [2], [3].

The conventional boost converter can be employed to boost the output voltage but that would require using extreme duty cycles and turns ratios. However, employing extreme duty cycles would eventually cause the voltage stresses on passive components and the conduction losses, and the voltage stress of the semiconductors is as excessive as the output voltage. The cascaded boost converter can be considered as a proper applicant for these high step-up gain converters. Nevertheless, applying cascaded boost converter will result in increasing the size of the converter and the cost and cause the electromagnetic interference problems. Moreover, it would reduce the reliability and efficiency and of the converter, and the output diode may experience a high voltage stress on the switches [4].

Many high voltage gain converters have been proposed with different voltage boost techniques to overcome the aforementioned shortcomings and enhance the voltage gain. In [5], a novel coupled inductor-based high step-up dc–dc converter has been proposed. In additions, the power density is increased due to high switching frequency, the voltage spike of the switch is clamped during the turn-off condition due to employing the clamped circuit, and zero voltage switching (ZVS) is given due the exittance of the energy in the leakage inductance. A high step-up interleaved dc–dc converter with asymmetric voltage multiplier and coupled inductors has been introduced in [6].

The aforementioned converter can be utilized to reduce the switching losses due to using the zero current switching (ZCS), lift the voltage gain and minimize the input current ripple, which would increase the lifetime of the input power. In [7], a group of cascaded high gain dc–dc converters with clamped circuits has been proposed to provide an ultra high voltage conversion with minimizing the passive components stresses. Several high step-up dc–dc topologies with ZVS turn-on capability are presented to achieve ultrahigh gain and mitigate and power devices losses in [8]-[13]. The losses in those topologies have been reduced due to the low resistance $r_{ds}$, and the reverse recovery problems have been alleviated due to the active clamp circuits [14]-[19]. Many high voltage gain dc–dc converters with coupled inductor and voltage multiplier techniques have been introduced [20]-[25]. Employing transformers can increase the output voltage level but cause result in decreasing the power density and cause the leakage inductance [26]-[31]. This paper introduces the operational principle of the proposed converter in section II, operating modes in part A of section II, voltage gain derivation in part B of section II, stress on power devices and performance comparison in section III, voltage stress and simulation results in part A of section III, experimental
verifications in part B of section III, and conclusion in section IV.

II. OPERATIONAL PRINCIPLE OF THE PROPOSED CONVERTER

This section primarily presents the operational principle of the proposed converter. In addition, the aforementioned converter comprises the interleaved boost converter with coupled inductors in the primary side, and the voltage multiplier cells with the secondary windings in the secondary side is as depicted in Fig. 1. Additionally, the current ripple and the losses can be reduced, and the voltage gain in the proposed structure can be extend further. The interleaved boost converter is mainly consisted of two coupled inductors, two magnetizing inductors \( L_{m1} \) and \( L_{m2} \), two leakage inductances \( L_{k1} \) and \( L_{k2} \) and two switches connected to the source. The voltage multiplier cells are connected with the secondary windings of the coupled inductors. The switching losses are reduced due to employing the zero current switching (ZCS). The input current ripple decreases as the phases of the interleaved converter increase. The phase shift between the switches is 180 degree, and the switching signals waveforms are depicted in Fig. 2 of the. As a result, in order to simplify the circuit, the following assumptions are considered:

1. The power devices are ideal, but the leakage inductances of the coupled inductors are modeled ideally with a magnetizing inductor a leakage inductor and an ideal transformer with a turns ratio of \( N = \frac{N_{1b}}{N_{1a}} = \frac{N_{2b}}{N_{2a}} \) (1)

2. All Capacitors are large enough to keep the voltage of the capacitors constant and make their voltages ripples free.

3. The current ripple in the inductors is negligible, and the inductors are large enough. The analysis of the proposed high voltage gain dc-dc converter is under the continuous conduction mode.

\[
\begin{align*}
\text{Mode 1:} & \quad S_1 \text{ is OFF and } S_2 \text{ is ON as depicted in Fig. 3. } N_{1b} \text{ and } N_{1a} \text{ store the energy, and the magnetizing inductors } L_{m1} \text{ and } L_{m2} \text{ store the energy, and the magnetizing inductor } L_{k1} \text{ and } L_{k2} \text{ are charged by the source. } L_{m2} \text{ and } L_{k2} \text{ are charged by the source. The magnetizing inductor currents are linearly increased. The diodes of voltage multiplier (VM) do not conduct, and they are reverse biased. Finally, the load energy is supplied by } C_1 \text{ and } C_2. \\
\text{Mode 2:} & \quad \text{In the second mode, } S_1 \text{ is OFF and } S_2 \text{ is ON as shown in Fig. 4. } D_2 \text{ and } D_3 \text{ do not conduct, and they are reverse biased. However, } D_1 \text{ and } D_4 \text{ are forward biased and conduct in this mode. The magnetizing inductance } L_{m1} \text{, the leakage inductance } L_{k1} \text{ and the source charge } C_2 \text{ and } C_4. \text{ } L_{m2} \text{ and } L_{k2} \text{ are charged by the source. Thus, } L_{m2} \text{ stores the energy, and } L_{m1} \text{ release the energy. }
\end{align*}
\]
B. Voltage Gain Derivation

This section introduces the derivation of the voltage gain. For the second mode, the steady state equations can be expressed as

\[ <V_{Lm1}> = <V_{Lm2}> = 0 \]  
\[ V_{in} = \frac{dV_{Lm1}}{dt} \]  
\[ V_{in} = \frac{dV_{Lm2}}{dt} \]  

The capacitor voltages for \( C_1 \) and \( C_2 \) are equal, the magnetizing voltages are identical and can be derived as

\[ V_{Lm1} = V_{Lm2} = V_{in} + Vc1 - Vc2 - Vc3 - Vc4 \]  
\[ V_{Lm1} = V_{Lm2} = V_{in} \]  

The volt-second balance principle, and the number of turns ratio is 1.5

\[ M = \frac{V_{out}}{V_{in}} = 2(N + 3) \times \frac{1}{(1-D)} \]  

For mode 3, the capacitor voltages can be written as

\[ V_{c1} = V_{in} \times \frac{1}{(1-D)} \]  
\[ V_{c2} = V_{in} \times \frac{2}{(1-D)} \]  
\[ V_{c3} = V_{in} \times \frac{3}{(1-D)} \]  
\[ V_{c4} = V_{in} \times \frac{4}{(1-D)} \]  

The voltage gain conversion can be written as

\[ V_{out} = V_{in} \times \frac{2}{(1-D)} \]  

III. STRESS ON POWER DEVICES AND PERFORMANCE COMPARISON

A. Voltage Stress and Simulation Results

This section discusses the voltage stress on components and comparison analysis. Hence, the voltage stress across the switches can be given as

\[ V_{s1} = V_{s2} = V_{in} \times \frac{1}{(1-D)} \]  

The magnetizing inductor currents and the output current can be derived as

\[ I_{Lm1(avg)} = I_{Lm2(avg)} = \frac{(N+2)I_{out}}{(1-D)} \]  
\[ I_{out} = \frac{V_{out}}{R} \]  

It can be observed from Fig. 6 and Fig. 7 that the voltage stress on the switches is reduced to 111.11 V, the magnetizing inductor currents are 20.20 A, the input voltage is 30 V and the output current is 1.21 A. Additionally, the voltage stress on diodes is reduced to 222.22 V, and the diode current are identical to the output current as depicted in Fig. 8. The voltage stress on diodes can be expressed as

\[ V_{pmax} = V_{D1} = V_{in} \times \frac{2}{(1-D)} \]  
\[ V_{D2} = V_{D3} = V_{D4} = V_{in} \times \frac{2}{(1-D)} \]  

The input current is the total of the two magnetizing inductor currents and can be calculated as

\[ I_{in} = \frac{2(N+2)I_{out}}{(1-D)} \]  

The input current is 40.40 A, the input voltage is 30 V, the voltage stress on \( C_1 \) is 111.11 V and the output voltage is lifted to 1000 V as illustrated in Fig. 9. The voltage stresses on \( C_2, C_3 \) and \( C_4 \) are 222.22 V, 333.33 V, 444.44 V as illustrated in Fig. 10.

Table I illustrates the performance between the proposed topology and other topologies in terms of voltage gain and voltage stress on switches, voltage stress on diodes, sharing ground connection, the input current and the total number of passive components and inductor cores. It can be noted that the voltage stress on switches and the total number of switches and capacitors in [5] and [6] are identical to the
The proposed converter. The total number of the inductor cores in [6] ground side for being floated and not shared is identical to the proposed topology. The voltage stress on the switches and diodes in [10] is high and could cause high conduction losses. The total number of power devices in [11] is equal to the proposed topology. TABLE II shows the selected components for the simulation part.

### TABLE II

| Component Parameters | Value |
|----------------------|-------|
| Input Voltage        | 30 V  |
| Output Voltage       | 1000 V|
| Duty Cycle           | 0.73  |
| Load Resistance      | 825 Ω |
| Magnetizing Inductors| 94 μH |
| Frequency (f_{sw})   | 118 KHz|
| Capacitors           | 10 μF |

B. Experimental Verifications

This section provides the experimental validation for the design and the theory. Additionally, a 500 W hardware prototype has been built to verify the simulation results and the design. The hardware prototype specifications are described in TABLE III. The topology is rated at 500 W with input voltage of 30 V and output voltage of 1000 V. The effective performance DPG20C300PN diodes are selected to achieve the voltage blocking on diodes, and the active switches are attained by employing MOSFETs IPA075N15N3GXKSA1. In addition, the capacitors are carefully chosen by utilizing MKP338 1 X1 to execute the existence high voltage blocking. The magnetizing inductor is done by using coupled inductors and magnetic core of EDT31 ferrite core, B66397 and N87 material. It can be observed that the parasitic resistance of the components could cause the conduction losses and can be written as

\[ P_{sw (cond loss)} = (I_{sw(rms)} \times I_{sw(rms)}) \times R_{DS(on)} \]  

The equivalent series resistance (ESR) of the capacitor may cause the capacitors losses and can be derived as

\[ P_{C (loss)} = (I_{C(rms)} \times I_{C(rms)}) \times ESR \]  

The diodes losses include the forward voltage and the average diode currents and can be given as

\[ P_D (loss) = I_{D(avg)} \times V_F \]  

### TABLE III

| Hardware Prototype Specifications |
|----------------------------------|
| MOSFETs                          | IPA075N15N3GXKS (S₁, S₂) |
| A (R_{ds(on)} = 7.5 mΩ, 150 V, 43 A) |
| Diodes                           | DPG20C300PN (D₃, D₄) |
| capacitors                       | MKP338 1 X1 (C₁ - C₄) |
| Capacitors                       | EDT31 ferrite core, B66397 |
| coupled inductor                 | (94 μH, N87 material) |

The experimental results of the voltage stress on the switches, input current, and the output voltage as depicted in Fig. 11. The voltage stress on the switches is 111.11 V, the input current is 40.40 A and the output voltage is 1000 V. The peak efficiency of the proposed converter is 96.9% at the output power of 500 W in different loads. Moreover, it can be observed that the maximum efficiency occurs at 500 W as shown in Fig. 12.
The power loss breakdown of the proposed converter is depicted in Fig. 13, and it can be noted that the coupled inductor loss are the dominant power losses, the diode loss, the capacitor loss and the switch loss. Thus, more coppers are highly recommended to enhance the efficiency of the proposed converter.

IV. CONCLUSION

A non-isolated high step-up dc-dc converter with diode-capacitor multiplier cells and dual coupled inductors has been introduced in this paper. Moreover, the input current of the proposed converter was continuous with small ripples due to the interleaved structure. The aforementioned topology has accomplished an ultra-voltage gain and power ability due to the coupled inductors and the voltage multiplier cell without an extreme duty cycle or a high turn ratio. The voltage gain, voltage stress on switches, voltage stress on diodes, sharing ground connection, the input current and the total number of passive components were compared between the proposed converter and other recent high step-up dc-dc converters. In addition, the voltage stress on power devices, the conduction losses and the cost were decreased. The reverse recovery problem of the diodes was alleviated, and the leakage energy was recycled. The theoretical analysis, operational principles, simulation results and experimental outcomes were designed. A hardware prototype was constructed to verify the design and the theory with improving the efficiency.

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