InAs-Al Hybrid Devices Passing the Topological Gap Protocol

Microsoft Quantum†
(Dated: February 15, 2024)

We present measurements and simulations of semiconductor-superconductor heterostructure devices that are consistent with the observation of topological superconductivity and Majorana zero modes. The devices are fabricated from high-mobility two-dimensional electron gases in which quasi-one-dimensional wires are defined by electrostatic gates. These devices enable measurements of local and non-local transport properties and have been optimized via extensive simulations to ensure robustness against non-uniformity and disorder. Our main result is that several devices, fabricated according to the design’s engineering specifications, have passed the topological gap protocol defined in Pikulin et al. [arXiv:2103.12217]. This protocol is a stringent test composed of a sequence of three-terminal local and non-local transport measurements performed while varying the magnetic field, semiconductor electron density, and junction transparencies. Passing the protocol indicates a high probability of detection of a topological phase hosting Majorana zero modes as determined by large-scale disorder simulations. Our experimental results are consistent with a quantum phase transition into a topological superconducting phase that extends over several hundred millitesla in magnetic field and several millivolts in gate voltage, corresponding to approximately one hundred micro-electron-volts in Zeeman energy and chemical potential in the semiconducting wire. These regions feature a closing and re-opening of the bulk gap, with simultaneous zero-bias conductance peaks at both ends of the devices that withstand changes in the junction transparencies. The extracted maximum topological gaps in our devices are 20-60 µeV. This demonstration is a prerequisite for experiments involving fusion and braiding of Majorana zero modes.

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1. INTRODUCTION

Topological quantum computation offers the promise of a high degree of intrinsic hardware-level fault-tolerance [1–6], potentially enabling a single-module quantum computing system that is capable of solving...
critical problems sufficiently rapidly to have societal impact [7]. This approach hinges on (a) reliably producing a stable topological phase of matter that supports non-Abelian quasiparticles or defects and (b) processing quantum information through protected operations, such as braiding. The former is challenging due to the material parameter and disorder requirements for topological phases of matter. In this paper, we report on three-terminal semiconductor-superconductor nanowire devices that pass the stringent topological gap protocol [8] and therefore satisfy these requirements. We further extract the gap associated with the topological superconducting phase in our devices [9–12].

Topological phases are a form of matter in which the ground state has long-range quantum entanglement and there is a gap to excited states [13]. Unlike phases of matter that can be distinguished completely by local measurements, topological phases are identified by the transformations of their low-energy states that result from fusing and braiding their quasiparticles and defects. Directly measuring these properties in experiments is rather subtle [14], hindering efforts to fully determine the topological order of candidate materials. In the fractional quantum Hall regime, for example, a quantized Hall conductance reveals the presence of a non-trivial topological phase, but many different topological phases can have the same Hall conductance. Consequently, different measurements are necessary to determine which topological phase is present in a given device [15–22].

In the case of quasi-one-dimensional superconducting wires without any symmetries enforced, there are only two phases — one trivial and one topological. The latter supports Majorana zero modes (MZMs) localized at the ends of the nanowire [9, 11, 12]. While MZMs can be directly detected through fusion and braiding, one of their auxiliary signatures are zero-bias peaks (ZBPs) in the differential tunneling conductance at the nanowire’s ends [23–28]. Indeed, most of the earlier experimental studies of candidate topological superconductors focused on ZBPs [29–42]. However, ZBPs can also be caused by disorder [43–45], smooth potential variations near the tunnel junction [46–51], unintentional quantum dots [52, 53], or a supercurrent [54]. These trivial ZBPs can persist over a fairly large range of system parameters [55–57].

A ZBP associated with an MZM must have a partner at the other end of the wire and should be stable to variations in the electric and magnetic fields in the device. The stability of MZMs with respect to such variations is determined by the bulk gap. However, if a device has a sufficiently large number of control parameters, it is likely that it can be tuned into a configuration in which it has trivial ZBPs at both ends. Meanwhile, the predicted range of stability of a topological phase depends strongly on device geometry, the full stack of materials, and disorder, rendering it difficult to distinguish “stable” ZBPs from “accidental” ones purely empirically. Analyzing the detailed shapes of tunneling conductance spectra leads to some loose qualitative patterns, but there is no sharp binary distinction between the local tunneling conductance spectra associated with MZMs and trivial ZBPs at non-zero temperature. In short, neither more extensive data sets of ZBPs nor more beautiful ZBPs can distinguish the topological and trivial phases. Therefore, it is crucial to develop a practical, reliable protocol that enables the detection of the topological superconducting phase of a nanowire, and it is clear that additional measurements beyond the tunneling conductance are necessary for such a protocol.

This challenge is addressed by the topological gap protocol (TGP) [8], which is designed to reliably identify the topological phase through a series of stringent experimental tests. At the heart of this protocol is the fact that there is necessarily a quantum phase transition between the trivial and topological phases [58]. The protocol detects a bulk phase transition between low-magnetic-field and high-magnetic-field phases via a bulk gap closing. It establishes that the high-field phase is topological through the stability of its ZBPs, in a manner that we specify below. The TGP requires three-terminal device geometries, which overcome the limitations of many earlier two-terminal devices. They allow ZBPs to be simultaneously observed at both ends and also allow for a measurement of the bulk transport gap through the non-local conductance. The protocol is passed when (a) ZBPs are observed in the local conductances measured at tunnel junctions at both ends of a wire, and they are stable to changes in the junction transparency; (b) these stable ZBPs persist over a range of magnetic fields and electron densities in the wire; (c) a closing and re-opening of the bulk transport gap is detected in the non-local conductances; (d) there is a region in the bulk phase diagram whose boundary is gapless and whose interior is gapped and has stable ZBPs; (e) the observed bulk transport gap throughout this region — the topological gap — exceeds the resolution of the measurement.

The hallmarks of most topological phases, including the one discussed here, are rather subtle: there is no signature as immediate as a quantized conductance or Meissner effect. Instead, the existence of a topological phase is imprinted on the measurable properties of the system in a manner that can only be identified through an elaborate measurement and analysis procedure such as the TGP or the even more elaborate procedures necessary for fusion and braiding. Thus, it is of paramount importance that the TGP has been validated by applying it to simulated transport data, especially since the tunneling spectroscopy and transport measurements comprising the TGP do not measure a topological invariant directly.

In simulated devices, we know whether there is a topological phase since we can compute a topological invariant. Hence, we tested the TGP on transport data from simulated devices by comparing its output to this topological invariant. We emphasize that we have not attempted to establish qualitative similarities between sim-
culated and measured conductance plots and this is not the purpose of these simulations. The goal is see if the TGP correctly distinguishes between regions with trivial and non-trivial topological invariant.

We simulated hundreds of devices with different disorder levels and concluded that if a device passes the TGP, then the probability that the candidate region in the phase diagram is not topological is $< 8\%$ at the 95\% confidence level. The TGP thereby distinguishes MZMs from trivial Andreev bound states and determines whether topological superconductivity is present in the parameter range scanned in a data set. Having thus confirmed the reliability of the TGP on simulated data, we formulate the central question of this paper: *can we fabricate and measure devices that pass the TGP?*

We answer this question in the affirmative by presenting data from four devices, named A, B, C, and D, that have passed this protocol with respective maximum topological gaps ranging between 20-60\,µeV. As we explain in more detail in Sec. 2, our devices are based on heterostructures combining indium arsenide (InAs) and aluminum (Al). The superconducting component is an Al strip, epitaxially-grown on the semiconductor so that it induces superconductivity via the proximity effect. The semiconducting portion is a shallow InAs quantum well hosting a two-dimensional electron gas (2DEG) that has been depleted by electrostatic gates, except for a narrow conducting wire that remains underneath the aluminum strip. Within this suite of components, we have used simulations to optimize the material stack and the device geometry with respect to the topological gap.

Disorder is the principal obstacle to realizing a topological phase supporting MZMs. We have used simulations to predict the (design-dependent) disorder level that the topological phase can tolerate. These simulations incorporate self-consistent electrostatics, the orbital effect of the magnetic field, and realistic semiconductor-superconductor coupling; see Refs. [41, 59, 60] for more details. Consequently, they show both qualitatively and quantitatively how device design can impact the effective disorder strength. Many of the resulting specifications are quite demanding, including: (1) higher mobility ($> 60,000\,\text{cm}^2/\text{Vs}$) than previously achieved in shallow InAs quantum wells and (2) gate-defined wires that are sufficiently narrow ($< 120\,\text{nm}$) as to enable tuning into the single sub-band regime.

Our simulations indicate that mesoscopic fluctuations are important. Even devices with the same average disorder level can have different TGP outcomes: some disorder realizations will pass while others fail. The disorder strength determines an expected yield for passing the TGP which is between 0\% and 100\% over a range of disorder levels. As expected from these simulation results, we have also measured devices that were similar to devices A-D but did not pass the TGP, and we report on data from two of them, which have been named devices E and F.

In summary, each of devices A-D has a high probability of being in the topological phase. To the best of our knowledge, these devices are the first to have passed as stringent a set of requirements as those encompassed by the TGP, namely (a) concurrent ZBPs that are stable both with respect to changes of the junction parameters and also with respect to changes of the bulk parameters that are larger (in appropriate units) than the bulk gap; and (b) a bulk gap closing and re-opening in response to an increasing magnetic field that is visible in the non-local conductance, indicating a quantum phase transition into a phase with correlated ZBPs.

2. **TOPOLOGICAL GAP DEVICE DESIGN AND REQUIREMENTS**

2.1. **Proximitized semiconductor nanowire model and its topological phase diagram**

In this section we briefly review the proximitized nanowire model [11, 12] which supports topological superconductivity over a range of densities and magnetic fields. The minimal model is comprised of a semiconductor nanowire with Rashba spin-orbit interaction coupled to a conventional (s-wave) superconductor. The effective
Hamiltonian for such a system is:

\[
H = H_{\text{SM}} + \Delta_{\text{ind}} O_{\text{SC}},
\]

\[
H_{\text{SM}} = \int_0^L dx \psi_\downarrow^\dagger(x) \left( -\frac{\partial^2}{2m^*} - \mu + i\alpha \sigma_y \partial_x + V_x \sigma_x \right) \psi_\downarrow(x),
\]

\[
O_{\text{SC}} = \int_0^L dx \left( \psi_\uparrow^\dagger(x) \psi_\downarrow^\dagger(x) + \text{h.c.} \right).
\]

Here, “SM” and “SC” are abbreviations for, respectively, semiconductor and superconductor, \(m^*\), \(\mu\) and \(\alpha\) are the effective mass, chemical potential, and Rashba spin-orbit coupling, respectively. \(V_x\) is the Zeeman splitting due to the applied magnetic field \(B\) along the nanowire: \(V_x = g_{\text{SM}} \mu_B B/2\), where \(g_{\text{SM}}\) and \(\mu_B\) are, respectively, the Landé \(g\)-factor and Bohr magneton. The proximity to the \(s\)-wave superconductor is effectively described by the pairing operator \(O_{\text{SC}}\), while \(\Delta_{\text{ind}}\) is the induced pairing potential.

The zero-temperature phase diagram of the proximitized nanowire Hamiltonian of Eq. (1) consists of a trivial (\(s\)-wave-like) phase and a topological phase, as shown in Fig. 1. The latter supports MZMs at the opposite ends of the nanowire and is in the same phase as a spinless \(p\)-wave superconductor [9]. The trivial and topological phases are separated by a quantum phase transition at \(V_x = \sqrt{\mu^2 + [\Delta_{\text{ind}}]^2}\) which is necessarily accompanied by the closing of the bulk gap. The stability of a topological phase is characterized by its bulk transport gap or, equivalently, the gap to extended states, which we call the topological gap \(\Delta_T\). In the idealized case of Eq. (1), this is simply the bulk gap. This phase has been proposed to occur in quasi-one-dimensional systems composed of chains of magnetic atoms on the surface of a superconductor [61–65] and in nanowires that are completely encircled by a superconducting shell in which the order parameter winds around the wire due to the orbital effect of the magnetic field [41, 66, 67].

The model discussed so far neglects many of the ingredients of real devices, such as additional sub-bands and the orbital effect of the magnetic field. To address this, we have developed realistic 3D simulations that take these effects into account. These simulations include self-consistent electrostatics, orbital magnetic field contributions, and realistic semiconductor-superconductor coupling [59, 60, 78–81]. We have validated these simulations through comparison with ARPES [82], THz spectroscopy [83], the Hall bar measurements reported in Appendix B, and transport through multiple types of previous devices involving proximitized semiconductor nanowires [41, 84–86]. We also take into account multiple disorder mechanisms such as charged disorder and variations of geometry and composition along the wire length, as discussed in Sec. 2.5. The superconductor’s degrees of freedom are integrated out, yielding a formulation in which it is encapsulated by self-energy boundary conditions [41, 85, 86]. Using this advanced simulation model, we optimized the design for gate-defined devices based on high-quality 2DEG heterostructures in order to minimize the effects of disorder, additional sub-bands, and the orbital effect of the magnetic field. This design is presented in the next subsection. In addition to performing transport simulations with this full model, we extract the parameters of a minimal model projected to the lowest sub-band in Appendix A.1. The parameters that define this effective single sub-band model are listed in Table I. After we have discussed the device design, we describe the general effects of disorder in mesoscopic topological wires, then quantify the effective disorder potential in our devices.

### 2.2. Gate-defined proximitized nanowire

Our devices are defined by an Al strip separated from an InAs quantum well by a barrier layer. There are two designs which are conceptually similar but have some practical differences. One has a single-layer gate (SLG) design while the other has a dual-layer gate (DLG) design, shown in Fig. 2 and Fig. 3, respectively. We will refer to both designs as “topological gap devices.” A cross-section of an SLG device is shown in Fig. 2(d), where the Al strip is light grey. The strip’s dimensions have been optimized using the simulations described above: length 10 \(\mu\)m, width < 120 nm, thickness < 10 nm.

The length is in the direction perpendicular to the cross-section in Fig. 2(d). The Al strip is covered by a several nm thick top oxide formed by controlled oxidation [not shown in Fig. 2(d) or Fig. 3(c)]. The Al strip features larger Al pads at each end of its 10 \(\mu\)m length, which can be seen at the right and left edges of the scanning electron micrograph (SEM) images in Fig. 2(b) and Fig. 3(b). The pads are contacted with Ti/Au or Ti/Al Ohmic leads, by which the Al strip is grounded. (Both types of contacts are normal in the typical operating regime.) We will denote the direction perpendicular to the surface of the quantum well as the \(z\)-direction, while the directions along and perpendicular to the Al strip are the \(x\)- and \(y\)-direction, respectively, as shown in Fig. 2(c,d).

There is a dielectric layer that separates the superconductor-semiconductor heterostructure from the electrostatic gates that are at the top of the cross-section in Fig. 2(d) and Fig. 3(c). The gates deplete the 2DEG except underneath the Al, which partially screens their electric fields, thereby creating a high-quality nanowire. The top view in Fig. 2(a) and the SEM image in Fig. 2(b) show that the split-gate structure of the SLG design is divided into three sections: three plunger gates and three
FIG. 2. (a) A schematic of the top view of the active area of a single-layer gate (SLG) topological gap device. All of the labelled gates serve to deplete the 2DEG in the InAs quantum well to define a high-quality one-dimensional conducting channel. The left, middle, and right plungers also tune the density in the corresponding sections of the device, while the left and right cutters also open and close the junctions. The two unlabelled gates are the “helper gates” which are used to control the electron density in the junctions and leads, the latter of which are connected to a measurement circuit as shown in this panel. (b) An SEM image of a topological gap device. The blue line indicates the active region depicted in (a). (c) Region of non-zero electron density (orange) in the InAs quantum well when the device is tuned to the operating regime: the middle section (underneath the middle cutter/plunger) is tuned to the topological regime while the outer sections (underneath the left/right cutter/plunger gates) are tuned to the trivial phase using the plunger gates. The blue curve shows the local density of states in the wire near zero energy, computed in the ideal disorder-free limit. (d) A schematic of the cross-section of an SLG topological gap device, in which the Al strip induces proximity superconductivity in the one-dimensional InAs nanowire that is defined by the gates shown in panel (a) and extends perpendicular to this cross-sectional view. The $x$-, $y$-, and $z$-directions are indicated in panels (c,d).

cutter gates. The three plunger gates serve to deplete the 2DEG on their side of the Al strip while the three cutter gates deplete the 2DEG on the other side. Once the 2DEG has been depleted, operating the plunger gates at even more negative voltages tunes the density underneath the Al via the fringe electric fields that remain after screening by the Al. The densities in the left, middle, and right sections can be controlled independently by the three plunger gates. We operate in the low-density limit in which only the lowest $z$-direction sub-band is occupied so, here and henceforth, will use the term “sub-band” for $y$-direction sub-bands. The left and right plungers control the densities underneath the corresponding sections of the Al, which are normally set for full depletion (no occupied sub-bands) underneath the Al. The width of the Al strip was chosen to enable this for moderate gate voltages $V_{\text{dep}} > -3$ V and also to minimize the orbital effects of a magnetic field in the $x$-direction.

There are two side tunnel junctions at the boundaries between the middle cutter gate and the left/right cutter gates, enabling the 3-terminal measurements [87–91] of the conductance matrix that are necessary for the TGP, as we discuss in Sec. 3. In addition to depleting the 2DEG on the opposite side of the Al strip from the plungers, the left and right cutter gate voltages $V_L$ and $V_R$ are also used to vary, respectively, the transparency of the left and right tunnel junctions. The split-gate geometry with plunger-cutter pairs ensures independent tuning of density and junction transparency for each section of the gate-defined nanowire. The two junctions are typically tuned into the tunneling regime in which the above-gap low-temperature differential tunneling conductance $G_N$ is $\lesssim e^2/h$, while the Al strip is grounded. The junctions are connected to Ohmic contacts via conducting paths in the 2DEG. There are two “helper” gates, which are the unlabelled gates at the bottom of Fig. 2(a); they extend from the junctions to the bottom edge of the SEM in Fig. 2(b).

The helper gates define these conducting paths by accumulating carrier density in the 2DEG underneath them and keeping it conducting. The orange region in Fig. 2(c) shows where the electron density is non-zero in the 2DEG in the device’s normal operating regime: underneath the middle section of the Al strip and underneath the helper gates.

In the DLG design, instead of a split-gate geometry, the plunger gates cover the Al strip completely, as il-
FIG. 3. (a) A schematic of the top view of the active area of a dual-layer gate (DLG) topological gap device. The plunger gates serve to deplete the 2DEG in the InAs quantum well to define a high-quality one-dimensional conducting channel and to tune the density in the corresponding sections of the device. The left and right cutters open and close the junctions. The two unlabelled gates are the “helper gates” which are used to increase the electron density in the junctions and leads, the latter of which are connected to a measurement circuit as shown in this panel. (b) An SEM image of a DLG topological gap device. The blue line indicates the active region depicted in (a). (c) A schematic of the cross-section of the middle section of a DLG topological gap device, in which the Al strip induces proximity superconductivity in the one-dimensional InAs nanowire that is defined by the gates shown in panel (a) and extends perpendicular to this cross-sectional view. The bulk of the wire doesn’t have a second gate layer, but the junctions have cutter gates in a second gate layer, and the 2nd dielectric layer separates them from the plunger gates in the first gate layer.

We will call the semiconductor underneath the middle section “the wire,” and the superconducting gap that is induced in the wire at $B = 0$ via the proximity effect the “induced gap” $\Delta_{\text{ind}}$. We denote the middle plunger gate voltage by $V_p$, which tunes the density in the wire. At the optimal operation point, the wire is tuned to the single-sub-band regime that occurs just before full depletion $V_p \gtrsim V_{\text{dep}}$. We will focus on the phase diagram of the wire as a function of the middle plunger gate voltage $V_p$ and the magnetic field $B$.

We comment briefly on the length of the wire here and discuss it in greater detail in Appendix A.3. To operate the device in the optimal regime, the nanowire should be much longer than the coherence length in the topological superconducting state, so that MZMs are well localized at the opposite ends of the nanowire [the situation depicted in Fig. 2(c)]. In this case, MZMs would lead to ZBPs that are stable with respect to local perturbations. When the coherence length is comparable to or larger than the nanowire length, a ZBP at one end of the wire may arise from an Andreev state extending from the opposite end [92]. In this case, however, we do not expect ZBPs to be stable with respect to local perturbations. Our simulations suggest that, for these designs and material stacks, the coherence length in the topological state would be around 300 nm in the absence of disorder. The wire is designed to be much longer than this. Disorder in the bulk of the nanowire suppresses the topological gap and increases the coherence length which, as we discuss in Appendix A.3, leads to a non-trivial requirement for the wire length which depends on the stack geometry/composition and disorder level. On the other hand, the wire cannot be too long since the visibility of gap closings will be strongly suppressed if the length of the wire is more than several times the normal-state localization length [87].

Assuming weak to moderate disorder, the optimal wire length in our devices is 3 $\mu$m. This length choice also ensures that when a transport gap closing is observed, there is a non-zero density of states in the bulk at zero energy which has non-vanishing matrix elements to both
leads so that non-local conductance is above the noise floor [89].

Finally, the outer sections (underneath the left/right cutter/plunger gates) must be significantly longer than the coherence length of the parent superconductor in order to prevent quasiparticle transport below the parent gap at full depletion.

2.3. Material stack

The material stack of the topological gap device is optimized to produce a large topological gap. To achieve a topological phase, the semiconductor stack needs to produce a large spin-orbit coupling and a large nominal $g$-factor in the confined 2DEG. In addition, the heterostructure should provide a low disorder environment, typically parameterized by high 2DEG mobility at low temperatures. Given the lack of suitable insulating and lattice-matched substrates, the active region is grown on an InP substrate employing a graded buffer layer to accommodate lattice mismatch.

The active region consists of the Al superconductor, an upper barrier, the InAs quantum well, and the buffer. The upper barrier layer plays a critical role in fine-tuning the coupling between the superconductor and the 2DEG residing in the quantum well. To drive the device into the topological phase, $B$ needs to be increased until the Zeeman energy $\mu_0 g^* \frac{B}{2}$ exceeds the induced gap $\Delta_{\text{ind}}$. Here, $g^*$ is the renormalized $g$-factor in the superconductor-semiconductor heterostructure, which is given by $g^* = g_{\text{SM}} \Delta_0 / (\Gamma + \Delta)$ if we neglect the $g$-factor of aluminum; a more general form of the renormalization factor is discussed in Appendix A.1. For strong coupling $\Gamma$ between the wire and the Al strip, $\Delta_{\text{ind}}$ would approach the gap in the Al strip $\Delta_\text{Al}$ and the electronic wavefunction of the single occupied sub-band of the wire would have large weight in the Al strip. In this case, $|g^*|$ would be renormalized to small values. In such a case, $\mu_0 g^* \frac{B}{2}$ would not approach $\Delta_{\text{ind}}$ until the magnetic field is very large (> 2.5 T), close to the critical in-plane field of the Al strip [27, 59, 93–95]. Conversely, if the coupling between the superconductor and semiconductor were too weak, the maximum attainable topological gap would be small, since it is bounded above by $\Delta_{\text{Al}}$. Hence, the material stack must satisfy $k_B T < \Delta_{\text{ind}} < \Delta_{\text{Al}}$.

As we shall see in Sec. 4, the parent gap in the Al strip is $\Delta_{\text{Al}} \approx 300 \text{ meV}$ (this is strongly dependent on the Al thickness). For an optimized heterostructure, according to our simulations of the device of Fig. 2(a), we expect $100 \mu\text{eV} < \Delta_{\text{ind}} < 200 \mu\text{eV}$, corresponding to an induced gap to parent gap ratio of $0.33 < \Delta_{\text{ind}} / \Delta_{\text{Al}} < 0.67$, and $4 < |g^*| < 7$.

Another function of the upper barrier layer is to separate the quantum well states from disorder on the dielectric-covered surface of the stack, thus enhancing the electron mobility. The quantum well thickness is chosen to minimize orbital effects from the magnetic field applied in the $x$-direction, to allow electrostatic tuning, and to retain the desirable properties of InAs, including optimally renormalized $g^*$.

Rashba spin-orbit coupling in the wire, characterized by the parameter $\alpha$, enables superconductivity to co-exist with the magnetic field $B$. Although $\alpha$ does not determine the critical field for the transition into the topological phase, it does contribute to the size of the topological gap and the extent of the topological phase in parameter space. The heterostructure has been engineered to have spin-orbit coupling in the range of 5 to 15 meV-nm.

In this paper, we present the results of measurements and simulations of devices based on four different material stacks satisfying the requirements given in this subsection. While they all feature an InAs quantum well, there are important differences in the quantum well width, barrier composition and thickness, and dielectric. In Table I, we give the effective parameters that encapsulate the effect of these materials changes, such as the effective mass, $g$-factor, and spin-orbit coupling. We will call these different materials stacks $\beta$, $\delta$, $\theta^*$, and $\epsilon$.

2.4. Phase diagram of ideal devices

For the SLG and DLG device designs described in Sec. 2.2 and the material stacks described in Sec. 2.3, we have computed the phase diagrams in the ideal disorder-free limit as a function of the actual control parameters of the device, $V_p$ and $B$. This is to be contrasted with Eq. (1) and Fig. 1, which contain the effective parameters $\mu$ and $V_x$. The bare spin-orbit coupling in the semiconductor is taken to be $\alpha_0 = 10 \text{ meV-nm}$ in both the SLG- and DLG-$\varepsilon$ designs. The color scheme in Fig. 4 is determined by the Pfaffian invariant [9, 97] (see Appendix A.4 for a brief description of this invariant). Darker red corresponds to larger topological gap and darker blue corresponds to larger trivial superconducting gap, as indicated by the color scale on the right-hand-side of the figure.

The red parabola in Fig. 1 has now become a sequence of red slivers in the ideal phase diagrams of an SLG device built on the $\beta$ stack in Fig. 4(a) and a DLG device built on the $\varepsilon$ stack in Fig. 4(b). The red slivers are topological phases with different numbers of occupied 1D sub-bands in the wire [27, 98]. When we zoom in on any one of these slivers, we see that it has the parabolic lobe-like shape $|g^*| \mu_0 B/2 > \sqrt{\mu^2 + \Delta_{\text{ind}}^2}$ that follows from Eq. (1). Here, the single-sub-band topological phase is at $V_p \approx -1.35 \text{ V}$, and it has a larger topological gap than when there are more occupied sub-bands. Recall that one of the design criteria was that the single-sub-band regime could be reached for moderate gate voltages; this figure confirms that it is satisfied by this design. As we increase $V_p$, thereby increasing the number of occupied sub-bands, the effective cross-sectional area of the gate-defined nanowire increases and, at some point, the orbital effect of the applied magnetic field becomes very important. In the second sub-band, an orbital-field-induced
The data and scripts required to reproduce this and other figures in this paper will similarly be in the (B, \( \delta \)) plane. This phase diagram is for a wire of infinite length. The maximum topological gap in the lowest sub-band is approximately 50 eV. It occurs at \( B \approx 3 \) T and \( V_p \approx -1.2 \) V. It is pushed to higher fields, as may be seen in Fig. 4.

Within the lowest sub-band, the effective mass \( m^* \), effective Rashba spin-orbit coupling \( \alpha^* \), effective \( g \)-factor \( g^* \), superconductor-semiconductor coupling \( \Gamma \), and lever arm \( d\mu/dV_p \) take the values given in Table I. As a result of the projection to the lowest sub-band, the bare Rashba spin-orbit coupling \( a_0 \) is replaced by the effective parameter \( \alpha \) given in the table. The precise definition of the effective single-band model governed by these parameters is given in Appendix A.1.

### 2.5. Disorder and uniformity requirements

We now discuss the level of imperfection that our device designs are expected to tolerate and still have a topological phase with coherence length \( \xi(0) \) shorter than the wire length \( L = 3 \) μm. See Appendix A.3 for a discussion of the coherence length \( \xi(0) \) and other important length scales.

In our devices, there are many different sources of disorder, including geometric and charged disorder [27, 38, 99]. Even small local variations in any of a number of device parameters can cause significant variations in the potential experienced by the electrons along the wire. As we discuss in Appendix A.1, we can extend the single-sub-band effective model Eq. (A1) parameterized by the couplings given in Table I to include disorder, leading to the Hamiltonian Eq. (A12). When the various disorder mechanisms are projected into this single-sub-band model, most of them can be characterized by the quenched Gaussian disorder model [100] in which disorder is represented by a random potential \( V(x) \) whose probability distribution is approximately described by the second-order cumulant defined in Eq. (A14). Both the strength of disorder \( \delta V \) and its correlation length \( \kappa \) depend on each disorder source in a manner that is highly dependent on the specific design and must be calculated in a full three-dimensional model, as we describe below. The designs in Fig. 2 and Fig. 3 have been optimized to be as forgiving as possible by requiring that the design minimize the projected disorder for fixed microscopic disorder.

In the regime of interest — the low-density regime with single sub-band occupancy — charged disorder domi-
nates \[101\]. From an analysis of the density-dependence of the mobility of Hall bars, we conclude that charged disorder is located primarily at the interface between the semiconductor surface and the gate dielectric. Hall bar measurements allow us to extract the average density of charged imperfections at the semiconductor-dielectric interface, denoted by \(n_{2D, \text{int}}\), and the lever arm \(dp/\partial V_t\). This is illustrated in Appendix B. Each chip studied in this paper has both topological gap devices and Hall bars, as shown in Fig. 5, enabling us to extract the average density of charged imperfections for each chip and to assess the impact on topological gap devices of chip-to-chip changes in the disorder level. Any impact that postgrowth fabrication has on the semiconductor-dielectric interface in a topological gap device will be present in its partner Hall bar as well since they are processed together on the same chip. If any fabrication processes increase the density of charged imperfections in a topological gap device, we will detect this in the corresponding Hall bar.

We have optimized the device geometry with respect to charged imperfections at the semiconductor-dielectric interface by choosing the Al width as wide as possible while still maintaining the ability to tune into the single sub-band regime. This keeps the active region in the InAs quantum well as far as possible from charged disorder at the interface between the semiconductor and the dielectric [see Fig. 2(d)]. (As we discussed in Sec. 2.3, the barrier layer plays a similar role in separating charged disorder as much as possible from the active region.) We use self-consistent electrostatics calculations \[59, 60\] to find the disorder potential underneath the Al. For realistic densities of charge defects \(n_{2D, \text{int}}\), we find that the variance of the projected disorder potential and correlation length to vary between \(\delta V \approx 0.5-1.5\) meV and \(\kappa \approx 75-125\) nm, respectively. In Fig. 22, we show how \(\delta V\) depends on \(n_{2D, \text{int}}\) for the SLG and DLG designs of, respectively, Fig. 2 and Fig. 3 in the \(\beta\), \(\delta\), or \(\varepsilon\) stacks.

From a transfer matrix calculation of \(\xi(0)\) for the model in Eq. (A12), we can obtain the disorder strength \(\delta V\) at which the minimum value of the coherence length \(\xi(0)\) begins to exceed our device length. Fig. 22 enables us to translate that value into a target \(n_{2D, \text{int}}\). In particular we obtain for SLG-\(\beta\) parameters that this occurs for \(n_{2D, \text{int}} > 3 \cdot 10^{12}/\text{cm}^2\). The \(\delta\) and \(\varepsilon\) stacks have slightly different requirements as a result of their stronger coupling to the superconductor, \(\Gamma\) (which is still within the required range of \(\Delta_{\text{ind}}/\Delta_{\text{Al}}\)). Hence, an initial target for dielectric quality is \(n_{2D, \text{int}} < 3 \cdot 10^{12}/\text{cm}^2\).

2.6. Topological phase diagram for a single disorder realization

Even when a device satisfies the requirements explained in the previous subsection and has a topological phase, disorder can cause the shape of the phase diagram to be rather complicated. To gain a better understanding, it is helpful to examine the phase diagram for a few representative disorder realizations. In this section, we diagonalize the Hamiltonian in Eq. (A12) and calculate the Pfaffian topological invariant \[9, 97\] for two independent disorder realizations. In any finite-sized system, the disorder-driven phase transition between the topological and trivial phases is rounded into a crossover. Consequently, a topological phase can be found in the phase diagram in some percentage of devices even for average disorder levels that exceed the critical value \(\delta V_c\) obtained in the thermodynamic limit. Conversely, some percentage of devices will not have a topological region of the phase diagram even for average disorder levels for which there would be a topological phase in the thermodynamic limit. Although disorder induces low-energy states —
FIG. 6. Phase diagrams for a single disorder realization at $\delta V = 0.3 \text{ meV}$ and $\delta V = 0.9 \text{ meV}$, as a function of the magnetic field $B$ and chemical potential $\mu$ for an $L = 3 \mu$m wire with the $\varepsilon$-stack single-band model parameters given in Table I. Blue represents the trivial phase and red is the topological phase, which is identified by the Pfaffian invariant $Q = \pm 1$. Compared to the ideal topological phase in Fig. 1 and relatively weak disorder effect in (a), the lobe in (b) moves to higher values of $\mu$ and splinters as a result of increasing disorder, consistent with Fig. 23b. A subset of the topological phase is highlighted in black, where the second lowest eigenvalue, representative of the gap, also has a high value. This more restrictive notion of topological region is even more “splintered” and prone to finite-size effects and mesoscopic fluctuations.

by creating domain walls between topological and non-topological regions, for instance — the density of such states may be low enough that an appreciable fraction of even reasonably long devices may not have any. Thus we can also characterize the phase diagram by the spectral gap in the $Q = -1$ region, taken as the second-lowest eigenvalue $E_2$ of $H$ (the lowest corresponds to the Majorana zero mode pair splitting).

In Fig. 6, we show the phase diagrams of two different simulated devices. Both have the DLG-$\varepsilon$ design, but with two different disorder realizations, one with $\delta V = 0.3 \text{ meV}$ (panel a) and one with $\delta V = 0.9 \text{ meV}$ (panel b). For weak disorder, the lobe structure of the topological phase is preserved, and the spectral gap remains high over a large region inside the lobe. For stronger disorder, mesoscopic fluctuations are important, as we discuss in Appendix A.3. The parabolic-shaped lobe of the topological phase of Fig. 1 — as identified by the Pfaffian topological invariant $Q = -1$ — is splintered into several disconnected regions of narrow range in $\mu$ and larger extent in $B$. This effect is even more dramatic if we additionally condition on a large spectral gap (black regions in Fig. 6). We will call these long, narrow regions of topological phase splinters of the single-sub-band lobe.

There precise shape of these splinters varies from one disorder realization to the next. We expect such mesoscopic fluctuations in our devices. In Appendices A.2 and A.3, we will discuss disorder-averaged parameters, such as the localization length $\xi(E)$.

2.7. Statement on confidential information

In summary, the principles behind the design of our devices and material stacks are that they should enable three-terminal transport and: (1) be based on a 2DEG residing in a low-defect quantum well; (2) have a charged defect density $n_{2D,in}$ at the semiconductor-dielectric interface that is less than $3 \cdot 10^{12}/\text{cm}^2$, as measured on a Hall bar on the same chip; (3) allow tuning to the lowest sub-band and full depletion of the wire; and (4) have an induced gap to parent gap ratio in the lowest sub-band that satisfies $0.33 < \Delta_{\text{ind}}/\Delta_{\text{Al}} < 0.67$.

The barrier thickness and composition, quantum well thickness, dielectric composition and deposition method, and Al strip width are critical factors that determine whether a device meets these prerequisites. The details of these design parameters and fabrication methods are Microsoft intellectual property that we cannot disclose. However, the principles listed above and described in this Section (particularly Secs. 2.2, 2.3 and 2.5) are sufficient to determine the key design and process parameters through a combination of simulation and experimentation. In particular, Hall bar measurements can be used to measure progress towards satisfying requirements (1) and (2); while zero-field transport measurements of topological gap devices (described in the next section) can be used to determine when (3) and (4) are satisfied. We present such measurements directly verifying that the $\beta$, $\delta$, $\delta'$, and $\varepsilon$ material stacks in either SLG or DLG designs fulfill them.

All of the key material and design parameters feed into the effective parameters given in Table I, together with $\delta V$ and $\kappa$. They define the projected single-sub-band model in Eq. (A12) from which our simulations can be reproduced. Any device that replicates our design and material stack will have similar effective parameters.
3. TOPOLOGICAL GAP PROTOCOL

The goal of the TGP is to identify whether there are regions in the experimental parameter space that show signatures consistent with a topological phase. The full source code of the TGP and raw data sets are available in Ref. [96]. The device’s outer sections are kept in the trivial superconducting phase by tuning their densities with the right and left plunger gates. In the topological phase of the wire, MZMs are localized at the boundaries between the topological and trivial sections, see Fig. 2(c). Provided that \( L \) is smaller than or, at least, not too much larger than the localization length \( \xi(\Delta_x) \), see Appendix A.3, there will also be an observed non-zero bulk transport gap. When this condition is satisfied, a non-zero above-gap non-local conductance is observable, enabling an identification of the gap, as we discuss further in Appendix A.3. In the TGP [8], the presence of MZMs and a bulk transport gap is detected by measuring the differential conductances

\[
\begin{pmatrix}
G_{LL} & G_{LR} \\
G_{RL} & G_{RR}
\end{pmatrix} = \begin{pmatrix}
dI_L/dV_L & dI_L/dV_R \\
dI_R/dV_L & dI_R/dV_R
\end{pmatrix}
\]  

(2)

as a function of \( V_p \) and \( B \) as well as the voltages \( V_{rc}, V_{le} \) controlling the tunnel junction transparencies, and the bias voltages \( V_b = V_R, V_L \), which can be increased in order to tunnel current into states of higher energies. The currents and voltages \( I_B, I_L, V_R, V_L \) are illustrated in Fig. 7. We use the cutter gates to open and close the junctions; when \( V_{rc} \) is more negative, the junction is more closed, and similarly with \( V_{le} \). We discard all devices in which one of the junctions cannot be completely closed at a pinch-off voltage \( > -3 \) V. Even among devices that pass this basic health check, there is considerable device-to-device variation in the pinch-off voltages and, more generally, in the relation between \( V_{rc}, V_{le} \) and the conductances through the junctions. This is, presumably, due to the different disorder configurations in the different junctions; these differences have a large effect because the junctions are depleted, leaving charged impurities unscreened, unlike in the bulk of the wire where the Al strip can suppress the effects of charged impurities via screening.

We want to vary the cutter gate voltages so that the local electrostatic environments at the two junctions change by enough to change the energy of bound states that are accidentally at zero energy for one cutter gate configuration. But since the cutter gate voltage change required to open or close a junction varies significantly from one junction to another as a result of disorder, we cannot simply choose the same sequence of \( V_{rc}, V_{le} \) values for each device. Instead, we use the above-gap conductance \( G_b \) at \( B = 0 \) and a bias voltage of 500 µV as a measure of the junction transparencies. In each device, we find sequences of cutter gate voltages \( V_{rc}, V_{le} \) for which \( G_b \) at both junctions take values between \( \approx 0.1 e^2/h \) and \( \approx 0.2 e^2/h \). They are slightly different in each device, but they always cover a substantial fraction of this range. When we say, as a shorthand, that we are varying the junction transparencies, we mean that we vary \( V_{rc}, V_{le} \) in this manner.

In the tunneling regime (i.e. for \( G_b < e^2/h \)), the current paths contributing to \( G_{RR}, G_{LL} \) are illustrated in Fig. 7(a). In this regime, \( G_{RR} \) and \( G_{LL} \) directly measure the local density of states in the wire at the boundaries between the middle and, respectively, the right and left sections. Hence, ZBPs in \( G_{RR} \) and \( G_{LL} \) in the tunneling regime indicate the presence of zero-energy states in the wire with sufficient tunneling matrix elements to the leads, consistent with MZMs but also with trivial zero-energy Andreev bound states. A zero-energy state (either MZM or trivial ABS) at the right junction will be manifested as a ZBP in \( G_{RR} \) and similarly for a zero-energy state at the left junction and a ZBP in \( G_{LL} \). Trivial ABS are not generically stable with respect to local perturbations whereas well-separated MZMs are. Therefore, the ZBP stability criterion, discussed below, allows one to better identify the region of interest.

The current path contributing to \( G_{LR} \) is illustrated in Fig. 7(b); \( G_{RL} \) is determined by the reverse path. For an intuitive understanding of \( G_{LR} \) and \( G_{RL} \), we first note that in the thermodynamic limit of the wire, the clean limit, and the tunneling limit of both junctions, a current injected at bias voltage above the Al parent gap will flow through the Al strip to ground via the contacts at the ends of the device unless it relaxes to energies between the induced gap and the parent gap. Hence, at bias voltages above the Al parent gap, \( G_{RL} \) and \( G_{LR} \) are strongly suppressed and are non-zero only as a result of these weak...
relaxation processes [87, 89, 102]. At zero-temperature, in the thermodynamic limit of the wire, the clean limit, and the tunneling limit of the junctions, current cannot be injected into the wire at bias voltages below the induced gap, except by Andreev processes, which inject supercurrent that also flows to the grounded contacts at the ends of the device. Now consider a finite-length disordered wire. At bias voltages at which the localization length $\xi(eV)$ is less than the length of the wire, $G_{RL}$ and $G_{LR}$ are strongly suppressed and are non-zero only as a result of non-zero temperature and finite ratio $L/\xi(eV)$.

(In an infinite wire, $G_{RL}$ and $G_{LR}$ would vanish at all bias voltages because all states are localized, except precisely at the transition. For a further discussion, see Appendix A.3.) Consequently, the highest bias voltage below which $G_{RL}$ and $G_{LR}$ are nearly vanishing (in a sense that we make more precise below) can be interpreted as the transport gap $\Delta_{tr}$ that we define in Appendix A.3. As we discuss in Appendix C.1, we perform this gap extraction with the parts of the non-local conductances that are antisymmetric in bias voltage, $A(G_{RL})$, $A(G_{LR})$:

$$A[(G_{RL}(V_b)] = [G_{RL}(V_b) - G_{RL}(-V_b)]/2$$  \hspace{1cm} (3)

and similarly for $G_{LR}$.

The high-dimensional nature of the parameter space that is explored by the TGP makes it prudent to narrow the measured parameter range. We explained above how the range of junction transparencies is limited. Meanwhile, the parameter range of $V_p$ is chosen to be close to the bottom of the first sub-band. When the chemical potential is below the first sub-band, the wire is fully depleted. The depletion point is identified by scanning the non-local conductance as a function of bias and $V_p$. This can be done at $B = 0$ or at non-zero $B$, with $B$ below the critical field of the superconductor, where the signal is generally larger. Recall that, as noted above, the non-local conductances are essentially zero outside the range of bias voltages between the induced and parent gaps, except for finite-size effects, thermal activation, and relaxation effects. Hence, full depletion of the wire causes the non-local conductance at bias voltages below the Al gap to drop below the noise floor. We use this depletion point to identify the single-sub-band regime.

In Fig. 8, we show the four elements of the experimentally-measured conductance matrix as a function of bias voltage $V_b$ and plunger gate voltage $V_p$ at zero magnetic field in one of our devices, which we label device A, to illustrate how the depletion point is identified. As may be seen from Fig. 8(c,d), the anti-symmetrized non-local conductances are large above the parent gap $\Delta_{Al} = 295 \pm 8 \mu eV$, which is indicated by horizontal dotted lines in Fig. 8(c,d). The anti-symmetrized non-local conductances are non-vanishing down to small bias for $V_p \approx -0.9 \mu eV$, which indicates that there is conduction through 2DEG regions not contacted by the Al for these plunger gate voltages. For $V_p$ more negative than $-0.9 \mu eV$, these 2DEG regions are depleted, and the induced gap opens up. As discussed previously, the anti-symmetrized non-local conductances are large between the induced and parent gaps, are suppressed above the parent Al gap, and are very strongly suppressed below the induced gap. As $V_p$ is decreased further, the induced gap increases, eventually reaching its maximum measured value of $\Delta_{ind} = 129 \pm 12 \mu eV$. At $V_p \approx -1.25 \mu eV$, the anti-symmetrized non-local signal drops sharply while local conductances remain large. For more negative $V_p$, the anti-symmetrized non-local signal is very small, and there is no longer a visible bias range between the induced and parent gaps. This is interpreted as full depletion of the semiconductor below the Al strip. The single-sub-band regime occurs just before wire depletion.

In summary, the TGP makes the parameter space of our devices manageable by by focusing on the most favorable region: $V_p$ near the bottom of the lowest sub-band;
$B$ from zero up to $2.5T$; and a range of junctions transparencies $G_\text{th}$ between $\approx 0.1e^2/h$ and $\approx e^2/h$.

The steps of the TGP are divided into two stages. 

**Stage 1:** (1) From an analysis of $G_{\text{th}}$ and $G_{\text{LL}}$, identify ZBPs at each end of the wire that are stable to variations of the junction transparencies and variations in local junction potential (which are controlled by $V_{\text{DC}}, V_{\text{DC}}$ in the manner discussed above). (2) Find clusters of points in the $B$-$V_p$ plane where there are stable ZBPs at both ends of the wire. These clusters and their surrounding neighborhoods define the regions of interest ROI$_1$ that are the focus of Stage 2. If there are no such clusters, the device fails Stage 1.

**Stage 2:** (3) Focusing on smaller $(B, V_p)$ ranges containing ROI$_1$s and restricting to cutter gate voltage pairs for which the junction transparency is approximately the same at both ends, confirm the existence of stable zero bias peaks in $G_{\text{th}}$ and $G_{\text{LL}}$, and recover the clusters of points in the $B$-$V_p$ plane where there are stable ZBPs at both ends of the wire. This step is important when there is a drift in $V_p$ between Stages 1 and 2. (4) Use $A(G_{\text{th}})$ and $A(G_{\text{LL}})$ to determine the bulk energy gap as a function of $(B, V_p)$ for each cutter gate pair. (5) For each cutter gate pair, find ZBP clusters identified in step 3 whose interiors are gapped and whose boundaries are gapless. We will denote them by $C_i^A$ where $i$ is a cutter gate pair index and $A$ is an index that distinguishes different gapped ZBP clusters with gapless boundaries that might occur for the same cutter gate pair. (6) Find the sets of clusters $T$ in the $B$-$V_p$ plane consisting of $C_i^A$ that overlap for different cutter gate settings. To be more precise, we define $T \equiv \{C_i^A \mid C_i^A \cap C_j^B \neq \emptyset \text{ for some } j \neq i \text{ and } \bigcup C_i^A \text{ connected}\}$. The device passes the TGP if there is a $T$ such that there is a $C_i^A \in T$ for a number of cutter gate settings $i$ that exceeds some threshold, as we make more precise in Appendix C.2. In this case we define the region of interest ROI$_2$ = $\bigcup_{C_i^A \in T} C_i^A$. Note that for a given device, there can be several $T$‘s and ROI$_{2\text{s}}$. We will call the clusters $C_i^A \in T$ “subregions of interest SOI$_2$ belonging to a region of interest ROI$_2$.”

There are a number of important measurement complexities that we discuss in Appendix C.1. The TGP is formulated with several thresholds which we explain in Appendix C.2: the minimum percentage of cutter gate settings for which a ZBP must be present in order to be considered stable, denoted by $(\text{ZBP\%})_{\text{th}}$; the minimum percentage of the boundary of a ZBP cluster that must be gapless in order for the whole boundary to be considered gapless, denoted by $(\text{GB\%})_{\text{th}}$; the conductance value below which we consider it to be effectively zero up to finite-size effects, denoted by $G_{\text{th}}$; and the minimum percentage of cutter gate settings for which an overlapping SOI$_2$ must be present in order to form an ROI$_2$, denoted by $(C_i\%)_\text{th}$.

The TGP captures the key physics of topological superconductivity because it requires a device to show stable ZBPs at both ends and also a bulk gap closing and reopening. However, we can make a much stronger quantitative statement about its reliability by testing it on simulated devices. We simulated 349 devices of different designs, material stacks, and disorder levels and applied the TGP to transport data from these devices. To test its reliability, we compared the ROI$_{2\text{s}}$ located by the TGP with the “scattering invariant” [103], a topological index that is defined for open systems (see Appendix A.4 for a brief description of this invariant). When the topological index is $-1$ in some region of the phase diagram, the region is topological; when it is $+1$, the region is trivial. However, trivial regions of the phase diagram can exhibit relatively stable ZBPs in their transport data, and the TGP was designed to avoid misidentifying such regions as topological.

We classify ROI$_{2\text{s}}$ as true positives (TP) if they contain any region with non-trivial topological index and as false positives (FP) otherwise. The false discovery rate (FDR) is the probability that an ROI$_2$ is trivial:

$$\text{FDR} \equiv P(\text{ROI}_2 \text{ is trivial}) = \lim_{N \to \infty} \frac{\text{FP}}{\text{FP} + \text{TP}},$$

where $N$ is the total number of devices. In essence, the FDR is the probability that if a device passes the TGP then the ROI$_2$ that it identifies has a completely trivial explanation, such as a trivial ABS. We estimate the FDR from the TP and FP numbers obtained from a large — but finite — number of simulated devices. As $N \to \infty$, the ratio $\text{FP}/(\text{FP} + \text{TP})$ approaches the FDR. For finite $N$, the best that we can do is estimate upper and lower bounds on the FDR. We use the Clopper-Pearson confidence interval at the 95% confidence level to estimate these bounds.

Our results are shown in Table II. Since we found no false positives, the confidence interval for the FDR is between zero and the upper bound that we list in the rightmost column. We find that if a device passes the TGP, there is a $< 8\%$ probability that the ROI$_2$ that it finds does not contain a topological phase. For the DLG-$\varepsilon$ design, the probability is $< 6\%$. We simulated several different disorder levels to investigate whether the TGP is more likely to give false positives when disorder is higher. Our results indicate that the TGP is reliable over the entire range $n_{\text{D,D,int}} = 0.1-4 \cdot 10^{12}/\text{cm}^2$, which is the range of charged disorder levels in the measured devices discussed in Sec. 4.1. Similarly, the differences between the SLG-$\beta$ and DLG-$\varepsilon$ stacks and designs have no effect on the accuracy of the TGP. The small dependence of our FDR estimates on disorder level and design that may be seen in Table II are entirely a consequence of the different numbers of ROI$_{2\text{s}}$ that were found at different disorder levels. Further details are given in Appendix D. As we

---

1 Note that the threshold $G_{\text{th}}$ depends on the level of disorder in the system and is taken differently at $0.1 - 10^{12}/\text{cm}^2$ charged disorder compared to the other cases. See Appendices D.2 and D.3 for details.
| Design, stack | $n_{2D,\text{int}}$ [10^{12}/cm^2] | TP | FP | FDR |
|--------------|-------------------------------|----|----|-----|
| SLG-β       | 1.0 244 0 < 1.5               |    |    |     |
|              | 2.7 46 0 < 7.7                |    |    |     |
|              | 4.0 45 0 < 7.9                |    |    |     |
| DLG-ε       | 0.1 125 0 < 2.9               |    |    |     |
|              | 1.0 97 0 < 3.7                |    |    |     |
|              | 2.7 67 0 < 5.4                |    |    |     |
|              | 4.0 66 0 < 5.4                |    |    |     |

TABLE II. Statistics of TGP results for simulated transport data from SLG-β and DLG-ε devices with 50 different disorder realizations for each of the average disorder strengths given in the first column. Devices with $n_{2D,\text{int}} \leq 10^{12}/\text{cm}^2$ typically have multiple distinct ROI$_2$s, so we have more total ROI$_2$s for low disorder. The listed range of FDR values is the confidence interval at the 95% confidence level.

discuss in Sec. 5, the statistical properties of the ROI$_2$s that we find in our simulations agree with the corresponding experimental values, thereby further validating the simulation model used estimate the FDR. This analysis addresses open questions regarding the reliability of the TGP [104].

4. EXPERIMENTAL DATA

4.1. Measurements of device A

In the remainder of this paper, we focus on measurements of devices such as the one shown in Fig. 2. In this section, we focus on data from device A, which is a 3 μm long SLG device built on a β-stack. We discuss three experimental measurements from this device. The raw data is available in Ref. 96. Measurement A1 was taken in one dilution refrigerator while measurements A2-A3 were taken in a different cooldown of device A in a different dilution refrigerator. The measured zero-field superconducting gap in the Al strip is $\Delta_{A1} = 295 \pm 8 \text{meV}$ and the maximum induced gap at zero $B$-field is $\Delta_{\text{ind}} = 129 \pm 12 \text{meV}$, which indicates that the induced gap to parent gap ratio $\Delta_{\text{ind}}/\Delta_{A1} = 0.44$ is well within the desired range. The effective charged impurity density at the interface with the dielectric is $n_{2D,\text{int}} = 2.7 \cdot 10^{12}/\text{cm}^2$, as is discussed in Appendix B. This value satisfies the specification explained in Sec. 2.5, which is based on the assumption that the average charged impurity density at the dielectric-semiconductor interface in the Hall bar is the same as at the dielectric-semiconductor interface in a topological gap device (the boundary between light blue and grey on either side of the Al strip in Fig. 2(d)) on the same chip. The critical field, $B_c$, for the thin Al strip is $> 4.5 \text{T}$ for magnetic fields in the direction of the strip. The single sub-band regime, as determined from the non-local conductance in the same manner as in Fig. 8, is reached at $V_p$ between $-1.2$ and $-1.4 \text{V}$ (depending on the cooldown). This is consistent with our simulations for device A; see Fig. 4. The base temperature in our measurements is $\sim 20 \text{mK}$ and, using NIS thermometry [105], we measured an electron temperature $T_e < 40 \text{mK}$.

4.1.1. TGP Stage 1

We begin by finding the single-sub-band regime, following the method discussed in Appendix C.1. The non-local signal below the Al parent gap vanishes for $V_p < -1.18 \text{V}$, which we interpret as the point at which the wire is fully depleted. We focus our Stage 1 scans on a $V_p$ range of 30 mV above this value.

In Fig. 9(a,b), we show the cutter gate fraction for ZBPs at, respectively, the left and right junctions as a function of $B$ and $V_p$. The black lines in Fig. 9(a,b) enclose the regions in which the cutter gate fraction for ZBPs at the left or right junction is greater than $> 70\%$. Finally, in Fig. 9(c), we show the fraction of junction transparencies at which there are ZBPs at both junctions, plotted as a function of $B$ and $V_p$. The black line indicates the part of the phase diagram where the cutter gate fraction for ZBPs at both junctions is $> 70\%$. Stage 1 data was taken for 5 different cutter gate voltages at each junction, or in total 25 $V_{lc}, V_{rc}$ settings. The cutter gate voltages were chosen so that $G_n$ of each junction is in the range $0.1-1.0 \text{e}^2/\text{h}$. In Stage 1, we find $(B, V_p)$ values at which there are ZBPs at both junctions for more than 17 out of 25 $(V_{lc}, V_{rc})$ pairs or, in other words, for which the cutter gate fraction for ZBPs at both junctions is $> 70\%$. Clusters of such points are the candidate regions of topological phase yielded by Stage 1 of the TGP, dubbed ROI$_1$ in Ref. 8.

There are several key features in Fig. 9 worth emphasizing. First, we expect that the topological phase in proximitized nanowires should have a lobe-like shape $|g|\mu_B B/2 > \sqrt{\mu^2 + \Delta_{\text{ind}}^2}$ in the absence of disorder. As a result of disorder, we expect the lobe to be splintered, as shown in the simulations in Fig. 6. In Stage 1 data from simulated device R1, this manifested as splintered regions in which there are stable ZBPs at both ends of the device, as may be seen in Fig. 27. The 30 mV field of view in Fig. 9 corresponds to a single lobe, which we identify as the lowest sub-band according to the method discussed in Appendix C.1. The structure that is visible in the phase space locations of stable ZBPs at the left and right junctions and, especially, in ROI$_1$ resembles the splintering of the lobe.

We have observed very similar ROI$_1$s in several devices (such as devices B, C, D, and E). In more disordered devices (such as device F, which is discussed in Sec. 4.2), ZBPs are scattered throughout phase space, and there is no structure, which suggests a non-topological phase of matter.

The data is reproducible between successive measurement runs on the same device, as we show in Sec. 4.1.3. The system is very stable, provided that $V_p$ is varied...
These cutter gate settings correspond to a range of bias voltages, which are the focus of Stage 2. As we will see when we compare measurements A2 and A3, focusing on this data. Qualitatively similar observations hold for the other two settings. In Fig. 10, there were 3 cutter gate pairs (rather than the 25 pairs of Stage 1). We use bias scans of the non-local conductances as a function of \( B \) and \( V_p \), which are the focus of Stage 2.

Next, we use bias scans of the non-local conductances \( A(G_{RL}) \), \( A(G_{LR}) \) to determine the bulk transport gap at each point in the phase diagram. We illustrate this in Fig. 10(e,f), where we show \( A(G_{RL}) \) and \( A(G_{LR}) \) as a function of \( B \) at the \( V_p = -1.17175 \) V horizontal line in Fig. 10(b). The black curves in Fig. 10(e,f) show the transport gap extracted from, respectively, \( G_{RL} \) or \( G_{LR} \) as a function of \( B \) for this \( V_p \) value. The black curves are determined according to the procedure explained in Appendix C.1. The transport gap is obtained by taking

\[
\Delta \approx \frac{1}{2} \sqrt{\Delta_{RL}^2 + \Delta_{LR}^2}
\]

where \( \Delta_{RL} \) and \( \Delta_{LR} \) are the transport gaps at the two junctions.
ing the minimum of the values extracted from \(A(G_{\text{RL}})\) and \(A(G_{\text{LR}})\). There is a clear bulk transport gap closing and re-opening visible in \(A(G_{\text{RL}})\) at \(B \approx 1.5\, \text{T}\). The gap remains open from \(B \approx 1.5\, \text{T}\) to \(B \approx 2.5\, \text{T}\).

We further illustrate the behavior of \(A(G_{\text{RL}}), A(G_{\text{LR}})\) by taking a vertical cut through the \(B-V_p\) plane. In Fig. 11, we show waterfall plots of local and non-local conductances as a function of \(V_p\) at fixed \(B = 1.66\, \text{T}\). The black dots in Fig. 11(c,d) indicate the bulk transport gaps extracted from \(G_{\text{RL}}\) and \(G_{\text{LR}}\). A gap closing and re-opening is clearly visible in these plots. We emphasize that these cuts through the phase diagram are a very small sample of the data comprising Stage 2 of measurement A1.

While these illustrative cuts are highly enlightening, they are not the primary goal of Stage 2 of the TGP, which is to derive an experimental phase diagram from the measured conductance matrix as a function of \(B, V_p, V_{\text{tc}}, V_{\text{rc}},\) and \(V_b\). The TGP yields the experimental phase diagrams in Fig. 10(a,b) for our representative cutter gate setting. All three cutter gate settings yield similar phase diagrams. The color scheme in Fig. 10(a,b) is the same as in the simulated phase diagrams in Fig. 28(a,b). The most salient feature of Fig. 28(a,b) is the presence of an SOI2. In this region, there are stable ZBPs at both ends of the device, and there is a non-zero bulk transport gap; 78\% of the boundary of this region in the \(B-V_p\) plane is gapless. Device A passed the TGP.

The crucial point of the TGP is to not rely on a single feature to identify a topological phase, but instead to rely on the totality of the data to provide evidence for the observation of a topological phase. Indeed, each pixel in Fig. 10(b) is determined by conductance data in a neighborhood of points around that pixel and for a range of cutter gate settings.

From \(A(G_{\text{RL}}), A(G_{\text{LR}})\), we infer a bulk gap closing and re-opening, which is a signature of a second-order phase transition. It is important to distinguish such behavior in the non-local conductances \(A(G_{\text{RL}}), A(G_{\text{LR}})\) from apparent gap closings/re-openings in the local conductances \(G_{\text{RR}}, G_{\text{LL}}\), which could easily be the motion of a local state towards zero energy, rather than a bulk phenomenon.

This phase transition line separates the high-field gapped phase from the gapped trivial superconducting phase that is present at low fields. It does not quite surround the high-field gapped phase: 78\% of the boundary shows a gap closing in \(A(G_{\text{RL}}), A(G_{\text{LR}})\). This surpasses \((\text{GB}\%)_\text{th}\); it is similar to the percentage of the boundary of the SOI2 that is gapless in the simulated data of Fig. 28 and is typical for simulations of this device design and disorder level. Consequently, we believe that the second order phase transition line that surrounds 78\% of our putative topological phase is, in fact, part of an unbroken transition line surrounding the entire phase. As noted in our discussion of \((\text{GB}\%)_{\text{th}}\) in Appendix C.2, one possibility is that the gap closing is not visible along 22\% of the boundary of the SOI2 due to a suppression of the signal by disorder/non-uniformity while another is that the topological region is larger than the SOI2. Indeed, for the cutter gate setting shown in Fig. 10, there are ZBPs at both junctions up to \(B = 2.5\, \text{T}\). However, at the other cutter gate settings, there is no visible ZBP at the left junction.

The high-field gapped phase is characterized by stable ZBPs at both ends of the wire, which is consistent with the topological phase. For some \(V_p\) values, the ZBPs appear before the gap re-opens, including at the \(V_p = -1.17175\, \text{V}\) horizontal line in Fig. 10(b). This is consistent with a scenario in which quasi-MZMs [46–51] are precursors to the transition into the topological phase, which is frequently seen in simulations.

The maximum topological gap is \(\Delta_{\text{topo}}^\text{max} = 23\mu\text{eV}\) for this cutter gate setting.\(^3\) Over the SOI2, which has an extent of \(\delta B \approx 500\, \text{mT}, \delta V_p \approx 1.5\, \text{mV}\), the extracted topological gap increases from zero to \(\Delta_{\text{topo}}^\text{max}\) in such a way that its median value over the region within the black line in Fig. 10(a,b) is 20\mu\text{eV}. From the phase diagram in Fig. 10(a,b), we see that the lowest field at which the gap closes near the SOI2 is \(\approx 0.8\, \text{T}\), which implies an effective \(g\)-factor of at least \(|g|_{\text{eff}} \approx 5.6\). Here, we define \(|g|_{\text{eff}} = 2\Delta_{\text{med}}/\mu_0 B_{\text{min}}\), where \(B_{\text{min}}\) is the lowest field at which the gap closes.\(^4\) This value of \(|g|_{\text{eff}}\) is close to the optimal value for this device design and material stack.

The induced gap (and all structure associated with its closing/re-opening) decreases rapidly when the magnetic field is rotated away from the direction of the wire, as expected. The transition to the topological phase should become more smeared as the temperature is increased, but it is difficult to study this systematically due to voltage drifts.

Comparing the experimental data in Fig. 10 to the simulated data in Fig. 28, we note both the qualitative and quantitative similarity between the phase diagrams. In both simulated and measured data, there are gap closings at similar \(V_p\)-dependent \(B\)-field values, and the extent of both the gapless regions and the SOI2s are of similar size in the \(B-V_p\) plane. However, we emphasize again that the main role of simulated data such as that shown in Fig. 28 is to test the TGP on (simulated) devices for which we know the phase diagram and not to reproduce the experimental phase diagram.

---

\(^2\) At the left junction, this ZBP is small, but above the measurement resolution, as may be seen in Fig. 10(c,g).

\(^3\) The extracted gap can depend on the cutter gate setting. Stability of the gap extraction with respect to cutter gate setting is not a requirement of the TGP.

\(^4\) Here we define the effective \(g\)-factor as the average slope of the extracted induced gap vs \(B\)-field. This is different from the conventional definition of the spin \(g\)-factor in terms of \(dE/dB\) at \(k = 0\). The former depends on spin-orbit coupling and orbital physics whereas the latter does not. However, in the single sub-band regime, where the lowest energy state has momentum close to \(k = 0\), both the orbital effect of the \(B\) field and spin-orbit coupling effects are small. In this case, \(|g|_{\text{eff}}\) is a good proxy for \(|g^z|\).
FIG. 10. (a) The experimental phase diagram of device A (measurement A1) in the color scheme shown at the left. The stability of ZBPs is determined by varying the cutter gates so that for both junctions $G_N$ takes the values 0.3, 0.5, 0.7$e^2/h$. The boundary of the SOI$_2$ is interpreted as a phase transition line, consistent with a visible gap closure along 78% of it. (b) The experimental phase diagram, showing trivial/topological phases, which the TGP identifies with the exterior/interior ($q = \pm 1$) of the SOI$_2$. The color scale shows the size of the trivial (positive sign) or topological (negative sign) gap. The protocol assigns a maximum topological gap $\Delta_{\text{max}}^{\text{topo}} = 23 \mu eV$. Measured local and anti-symmetrized non-local conductances along the horizontal line in panel b at $V_p = -1.17175 \text{ V}$: (c) $G_{LL}$, (d) $G_{RR}$, (e) $A(G_{RL})$, (f) $A(G_{LR})$. The SOI$_2$ lies between the vertical lines. Panels (g)-(j) are “waterfall” plots representing the same measured data. The data shown in (c)-(j) was obtained for $G_N \approx 0.3e^2/h$ for both sides. The black curves in panels (e) and (f) and the dots in panels (i) and (j) are not guides to the eye; they indicate where the non-local signal drops below a threshold value, as described in the text.
FIG. 11. “Waterfall” conductance plots of (a) $G_{LL}$, (b) $G_{RR}$, (c) $A(G_{RL})$, (d) $A(G_{LR})$ as a function of the corresponding bias and plunger gate voltage $V_p$ for device A (measurement A1). The data is the $B = 1.66$ T vertical line in Fig. 10(b). ZBPs and extracted gap points corresponding to SOI$_2$ are shown in black.

4.1.3. Reproducibility of the data: Measurements A2 and A3

We now present experimental data from a different cooldown in which measurements A2 and A3 were performed one week apart. These measurements produced similar data sets, both passing the TGP, indicating the reproducibility of our data and the device’s stability from one measurement run to another. Both of these data sets are consistent with measurement A1 shown in Sec. 4.1.

In our simulations, we saw that devices can pass the TGP for some disorder configurations but not others. Each cooldown typically leads to a somewhat different disorder configuration, resulting, for example, in a shift of the gate voltages at which we see the depletion of the lowest sub-band. As mentioned previously, when the device idles for a week, the disorder configuration can also drift slightly. Hence, we expect that the same device will pass the TGP in some measurements but not in other measurements occurring a week or more apart or in different cooldowns. This was the case with device A. It regularly passed the TGP, but also failed sometimes. In this subsection, we focus on measurements A2 and A3, in which device A passed the TGP with a topological phase that shifted in parameter space. For measurement A2, device A was warmed-up, removed from the dilution refrigerator in which A1 was performed, cooled down in a different dilution refrigerator, and re-measured. In accordance with the TGP, we performed Stage 1 measurements and identified an ROI$_1$ with stable ZBPs near $V_p = -1.4$ V. The results of the subsequent Stage 2 measurement are shown in Fig. 12.

The phase diagrams in Fig. 12(a,b) have the same basic features as those in Fig. 10(a,b). The primary differences are as follows. The lowest gap closing point in A2 is slightly lower in field than in A1, leading to an effective $g$-factor of $|g_{eff}| \approx 6.4$. The topological phase starts at lower fields, close to 0.8 T, which is closer to the lowest fields at which the gap closes than in A1, and it extends over a larger range of plunger gate voltages, $\delta V_p = 2.5$ mV but a similar magnetic field range $\delta B \approx 500$ mT. The maximum topological gap in measurement A2 is $\Delta_{\text{topo}}^{\text{max}} = 29$ µeV, see Fig. 12(b), which is the largest observed for device A, and the percentage of the boundary that is gapless is 80%. The local conductances are shown in Fig. 12(c,d). In addition to ZBPs, there is also a strong local resonance at the right junction which is evident in Fig. 12(d). However, this resonance moves away from zero bias as $B$ is increased. Furthermore, this resonance disappears in the subsequent measurement shown in Fig. 13(d), indicating that this is an accidental feature due to an impurity that moved between measurements A2 and A3. This trivial resonance partially obscures the stable ZBP, which has a smaller amplitude.

In Fig. 13, we show measurement A3 which was performed in the same cooldown as measurement A2 but one week later. The electrostatic environment of the system drifted by 2-3 mV during the week between the two measurement runs, as is typically the case in our devices.
FIG. 12. (a) The experimental phase diagram of device A (measurement A2) that results from combining the clusters of stable ZBPs at both junctions with the map of the locus of zero/non-zero gap. The stability of ZBPs is determined by varying the cutter gate settings so that for both junctions $G_N$ take the values 0.3, 0.5, 0.7, and 0.9e$^2$/h. The boundary of the SOI is interpreted as a phase transition line, consistent with a visible gap closure along 80% of it. (b) The experimental phase diagram, showing trivial/topological phases, which the TGP identifies with the exterior/interior ($q = \pm 1$) of the SOI. The color scale shows the size of the trivial (positive sign) or topological (negative sign) gap. The protocol assigns a maximum topological gap $\Delta_{\text{topo}}^{\text{max}} = 29 \mu$eV. Measured local and anti-symmetrized non-local conductances along the horizontal line in panel b at $V_p = -1.4045$ V: (c) $G_{LL}$, (d) $G_{RR}$, (e) $A(G_{RL})$, (f) $A(G_{LR})$. The SOI lies between the vertical lines. Panels (g-j) are “waterfall” plots representing the same measured data. The data shown in (c-j) was obtained for left (right) $G_N \approx 0.5$e$^2$/h ($\approx 0.8$e$^2$/h). The black curves in panels (e,f) and the dots in panels (i,j) indicate where the non-local signal drops below a threshold value, as described in the text.
FIG. 13. (a) The experimental phase diagram of device A (measurement A3) that results from combining the clusters of stable ZBPs at both junctions with the map of the locus of zero/non-zero gap. The stability of ZBPs is determined by varying the cutter gate settings so that for both junctions $G_N$ take four values between 0.3 and $0.8 e^2/h$ at $B = 0$. The boundary of the SOI is interpreted as a phase transition line, consistent with a visible gap closure along 90% of it. (b) The experimental phase diagram, showing trivial/topological phases, which the TGP identifies with the exterior/interior $(q = \pm 1)$ of the SOI. The color scale shows the size of the trivial (positive sign) or topological (negative sign) gap. The protocol assigns a maximum topological gap of $\Delta_{\text{max}}^{\text{topo}} = 22 \mu eV$. Measured local and anti-symmetrized non-local conductances along the horizontal line in panel b at $V_p = -1.4083$ V: (c) $G_{LL}$, (d) $G_{RR}$, (e) $A(G_{HL})$, (f) $A(G_{LR})$. The SOI lies between the vertical lines. Panels (g)-(j) are “waterfall” plots representing the same measured data. The data shown in (c)-(j) was obtained for left (right) $G_N \approx 0.6 e^2/h$ ($\approx 0.4 e^2/h$). The black curves in panels (e) and (f) and the dots in panels (i) and (j) indicate where the non-local signal drops below a threshold value, as described in the text.
However, the main qualitative features are reproduced from one run to the next: there is a topological phase with a comparable critical field and similar overall shape. The size of the maximum topological gap has decreased from its value in A2 to $\Delta_{\text{topo}}^{\text{max}} = 22\,\mu\text{eV}$, which is close to value found in measurement A1.

Finally, we discuss the stability of ZBPs with respect to local perturbations. In Fig. 13(c,d) one can see stable ZBPs at both junctions over a magnetic field range $\delta B \approx 0.5\,\text{T}$. They are similarly stable with respect to changes in $V_p$, as may be seen from the vertical extent of the orange region in Fig. 13(a). These peaks are also stable with respect to cutter changes modulating the transparency of the junctions, as we show in Fig. 14. There are ZBPs with height $O(\epsilon^2/h)$ that are present for 4 cutter gate settings. These changes in left cutter gate settings tune $G_n$ on both sides to vary over the range 0.1 and $1.0\epsilon^2/h$. Thus, while these cutter changes significantly modify the junction transparencies, the ZBPs remain stable with respect to these perturbations. In SOI$_2$, there are ZBPs exhibiting this type of stability at both junctions.

To conclude this subsection, we believe that the totality of the data from device A — passing the TGP in multiple cooldowns and re-measurements, qualitative and quantitative consistency with simulations, and the stability of the SOI$_2$ with respect to various perturbations — provides strong evidence for the observation of a stable topological superconducting phase supporting MZMs in this device. We now turn to the reproducibility of these results in other devices.

### 4.2. Experimental data from other devices

Since disorder can destroy the topological phase, and different devices will have different disorder realizations, we can expect quantitative and qualitative differences between devices. Indeed, we have measured devices in which we were not able to find a topological phase. However, devices that have a narrow Al strip, zero-field induced gap to parent gap ratio in the required range, and weak disorder often pass the TGP while devices not meeting these requirements have never passed TGP, as expected from simulations. For example, no devices with dielectric charge density above $3 \cdot 10^{12}/\text{cm}^2$, as extracted from a Hall bar on the same chip, have passed TGP.

In this section, we show data from devices B, C, and D, summarized in Figs. 15, 17 and 18, which also pass the TGP, thereby demonstrating that we can reproducibly fabricate devices passing the TGP. These three devices are DLG devices. Device B is built on the $\epsilon$-stack and has $\Delta_{\text{Al}} = 326 \pm 29\,\mu\text{eV}$ and $\Delta_{\text{ind}} = 169 \pm 11\,\mu\text{eV}$; hence, the ratio of the induced gap to the parent gap in device B is 0.52, which is slightly larger than in device A and very close to optimal. It has the largest topological gap reported in this paper: $\Delta_{\text{topo}}^{\text{max}} = 61\,\mu\text{eV}$. Device C is built on the $\delta$-stack and has $\Delta_{\text{Al}} = 292 \pm 8\,\mu\text{eV}$ and $\Delta_{\text{ind}} = 104 \pm 6\,\mu\text{eV}$; in device D, which is also built on the $\delta$-stack, the corresponding gaps are $\Delta_{\text{Al}} = 293 \pm 9\,\mu\text{eV}$ and $\Delta_{\text{ind}} = 117 \pm 20\,\mu\text{eV}$. The ratio of the induced gap to the parent gap in devices C and D, 0.35, and 0.4, respectively, is somewhat smaller than the nearly-optimal value of 0.52 that it takes in device B or even the value of 0.44 that it takes in device A. The effective charged impurity densities at the interface with the dielectric are $n_{2D,\text{int}} = 0.79 \cdot 10^{12}/\text{cm}^2$ in device B, $n_{2D,\text{int}} = 1.1 \cdot 10^{12}/\text{cm}^2$ in device C, and $n_{2D,\text{int}} = 1.0 \cdot 10^{12}/\text{cm}^2$ in device D, extracted by the procedure discussed in Appendix B.\(^5\) These values are smaller than in device A and satisfy the specification given in Sec. 2.5.

In addition, we show data from devices E and F that do not pass the TGP. They are DLG devices built on the $\delta'$ stack. As noted previously, we do not expect all

\(^5\) There is one subtlety here, which is that DLG devices have two different dielectric layers, one below the gate layer and one between the gate layers. The first dielectric layer is likely to control bulk properties of the wire while both dielectrics contribute to junction properties. The quoted $n_{2D,\text{int}}$ numbers are for Hall bars with both dielectric layers, but the difference with $n_{2D,\text{int}}$ extracted from sibling chips is small.
FIG. 15. (a) The experimental phase diagram of device B that results from combining the clusters of stable ZBPs at both junctions with the map of the locus of zero/non-zero gap. The stability of ZBPs is determined by varying the cutter gate settings so that for both junctions $G_N$ take the values 0.5, 0.41, 0.33, 0.24, and 0.15$e^2/h$ at $B = 1.4$ T. The boundary of the SOI$_2$ is interpreted as a phase transition line, consistent with a visible gap closure along 92% of it. (b) The experimental phase diagram, showing trivial/topological phases, which the TGP identifies with the exterior/interior ($q = \pm 1$) of the SOI$_2$. The color scale shows the size of the trivial (positive sign) or topological (negative sign) gap. The protocol assigns a maximum topological gap of $\Delta_{\text{topo}}^{\text{max}} = 61 \mu$eV. Measured local and anti-symmetrized non-local conductances along the horizontal line in panel (b) at $V_p = -1.15775$ V: (c) $G_{LL}$, (d) $G_{RR}$, (e) $A(G_{RL})$, (f) $A(G_{LR})$. The SOI$_2$ lies between the vertical lines. Panels (g)-(j) are “waterfall” plots representing the same measured data. The data shown in (c)-(j) was obtained for $G_N \approx 0.41e^2/h$ on both sides. The black curves in panels (e) and (f) and the dots in panels (i) and (j) indicate where the non-local signal drops below a threshold value, as described in the text.
devices to pass the TGP, even if they were to have the same gap ratio and disorder levels as device A. Hence, it is not surprising that some of our devices fail the TGP; indeed, it is required by consistency with our simulations. Moreover, devices E and F have lower induced gap to parent gap ratios, which suppresses their expected probabilities of passing the TGP. Device E has \( \Delta_{\text{AI}} = 415 \pm 13 \, \mu\text{eV} \) and \( \Delta_{\text{ind}} = 90 \pm 6 \, \mu\text{eV} \) (induced gap to parent gap ratio of 0.22); in device F, the corresponding gaps are \( \Delta_{\text{AI}} = 338 \pm 12 \, \mu\text{eV} \) and \( \Delta_{\text{ind}} = 92 \pm 14 \, \mu\text{eV} \) (induced gap to parent gap ratio of 0.27). The effective charged impurity densities at the interface with the dielectric is \( n_{2D,\text{int}} = 3.1 \times 10^{12} / \text{cm}^2 \) in device E and \( n_{2D,\text{int}} = 3.0 \times 10^{12} / \text{cm}^2 \) in device F, extracted by the procedure discussed in Appendix B. These values are larger than in devices A-D and, moreover, are large enough that do not satisfy the specification given in Sec. 2.5.

Device E exhibits clusters of points in \((B, V_p)\) space with stable ZBPs at both ends, thereby passing Stage 1 of the TGP. However, non-local conductance measurements in the region of interest yield zero gap. Device E is, thus, in a gapless phase and it fails Stage 2 of the TGP. Device F fails even Stage 1 because it does not have clusters of \((B, V_p)\) points with stable ZBPs at both ends.

Overall, the measurement data from devices A-F demonstrate the different qualitative phenomena observed in our devices.

### 4.2.1. Device B passing TGP

Since device B has a considerably larger zero-field induced gap than device A, a topological phase would have to occur at higher magnetic fields. The TGP finds an experimental phase diagram that is consistent with this expectation. There is a topological phase transition at \( B = 2 \, \text{T} \), as shown in Fig. 15(a,b). The TGP assigns this device a maximum topological gap \( \Delta_{\text{topo}} = 61 \, \mu\text{eV} \). The median value of the topological gap across the orange region in Fig. 15(a) is 47 \( \mu\text{eV} \). Device B has \( |g_{\text{eff}}| \approx 3.7 \), which is smaller than that of the other devices reported in this paper. This is consistent with device B’s large \( \Delta_{\text{ind}} / \Delta_{\text{AI}} \) ratio, which implies that electrons in the lowest occupied sub-band have a higher amplitude to be in the superconductor, thereby inheriting both a larger induced gap and a smaller \( |g_{\text{eff}}| \).

The extent of the SOI\(_2\) is \( \delta B = 0.2 \, \text{T} \). The measured extent in \( V_p \) is \( \delta V_p \approx 1 \, \text{mV} \), however, Stage 2 did not go to \( V_p \) lower than \( V_p = -1.1580 \, \text{V} \), where the SOI\(_2\) still appears to be quite robust, so it is possible that this underestimates the size of the SOI\(_2\). It is also possible that the blue region centered around \( B = 2.3 \, \text{T} \) and \( V_p = -1.573 \, \text{V} \) — which the TGP identifies as a gapped trivial region due to the absence of stable ZBPs — is actually topological but has MZMs that are poorly coupled to the leads. There are some sign changes in the non-local conductance, such as the one that occurs at \( B \approx 2 \, \text{T} \) in Fig. 15(e,f). Since \( G_{\text{LR}} \) and \( G_{\text{RL}} \) are suppressed at
FIG. 17. (a) The experimental phase diagram of device C that results from combining the clusters of stable ZBPs at both junctions with the map of the locus of zero/non-zero gap. The stability of ZBPs is determined by varying the cutter gate settings so that $G_N$ range from $0.6 \ e^2/h$ on the left and from $0.2 \ e^2/h$ on the right. The boundary of the SOI $2$ is interpreted as a phase transition line, consistent with a visible gap closure along $100\%$ of it. (b) The experimental phase diagram, showing the trivial/topological phases, which the TGP identifies with the exterior/interior ($q=\pm1$) of the SOI. The color scale shows the size of the trivial (blue) or topological (red) gap. The protocol assigns maximum topological gap of $19 \ \mu eV$. Measured local and anti-symmetrized non-local conductances along the horizontal line in panel (b) at $V_p = -2.3655 \ \text{V}$: (c) $G_{LL}$, (d) $G_{RR}$, (e) $A(G_{RL})$, (f) $A(G_{LR})$. The SOI $2$ lies between the vertical lines. Panels (g)-(j) are “waterfall” plots representing the same measured data. The data shown in (c)-(j) was obtained for left (right) $G_N$ of approximately $0.6e^2/h$ ($0.2e^2/h$). The black curves in panels (e) and (f) and the dots in panels (i) and (j) indicate where the non-local signal drops below a threshold value, as described in the text.
FIG. 18. Stage 2 data for device D. There are two $\text{SOI}_2$s in the phase diagram. (a) The experimental phase diagram of device D that results from combining the clusters of stable ZBPs at both junctions with the map of the locus of zero/non-zero gap. The boundary of the $\text{SOI}_2$s are interpreted as phase transition lines, consistent with visible gap closures along, respectively, 100% and 93% of them. (b) The experimental phase diagram, showing the trivial/topological phases, which the TGP identifies with the exterior/interior ($q = \pm 1$) of the $\text{SOI}_2$. The color scale shows the size of the trivial (blue) or topological (red) gap. The protocol assigns maximum topological gaps of $17 \mu\text{eV}$ and $21 \mu\text{eV}$ for the top and bottom clusters, respectively. Measured local and anti-symmetrized non-local conductances along the horizontal line in panel b at $V_p = -2.721 \text{V}$: (c) $G_{\text{LL}}$, (d) $G_{\text{RR}}$, (e) $A(G_{\text{RL}})$, (f) $A(G_{\text{LR}})$. The $\text{SOI}_2$ lies between the vertical lines. Panels (g)-(j) are “waterfall” plots representing the same measured data. All data shown in this figure were obtained for left/right $G_N$ of approximately $0.8e^2/h$. The black curves in panels (c) and (d) and the dots in panels (i) and (j) indicate where the non-local signal drops below a threshold value, as described in the text.
FIG. 19. Stage 2 data for device E. (a) The regions with stable ZBPs at both junctions. The stability of ZBPs is determined by varying the cutter gate settings so that the above gap conductances are 0.6 and 1.0e²/h on the left and 0.2 and 0.4e²/h on the right. (b) The gap as function of $B$, $V_p$. It vanishes in the region of interest, so this device fails the TGP. Measured local and anti-symmetrized non-local conductances along the horizontal line in panel b at $V_p = -1.3893$ V: (c) $G_{LL}$, (d) $G_{RR}$, (e) $A(G_{LL})$, (f) $A(G_{LR})$. The local conductances in panels c and d show ZBPs, but there is no gap re-opening visible in the anti-symmetrized non-local conductances in panels (e) and (f). The cut shown in (c)-(f) is at $G_N$ of approximately 0.6e²/h on the left and 0.2e²/h on the right.

these sign changes, they lead to large values of the extracted gap, which can bias $\Delta_{\text{topo}}^{\text{max}}$ towards larger values. However, even the median gap is 47µeV, and there is a clearly identifiable gap edge at $\approx 50$µeV in $G_{RL}$ at $B = 2.1$ T. “Waterfall” plots for local and non-local conductances at fixed plunger $V_p = -1.15775$ V are shown in Fig. 15(g,j)). Additionally, in Fig. 16 we show “waterfall” plots of conductances for fixed magnetic field $B = 2.12$ T corresponding to the vertical line in Fig. 15(b).

As noted above, device B has the largest $\Delta_{\text{ind}}$ value and the smallest $n_{2D,\text{ind}}$ value reported in this paper and, perhaps not surprisingly, the largest topological gap $\Delta_{\text{topo}}^{\text{max}}$ as well. The topological gap is actually equal, within error bars, to the largest topological gap that we would expect for a perfectly clean, infinitely-long DLG-$\epsilon$ device. This is not a contradiction. Finite-size effects can increase the gap. We measure a transport gap, which is the gap to extended states (for $L = 3 \mu$m), and it can be larger than the gap in the spectrum if states at the gap edge have short localization lengths.

4.2.2. Devices C and D passing TGP

The experimental phase diagram for device C is shown in Fig. 17. The TGP assigns this device a maximum topological gap $\Delta_{\text{topo}}^{\text{max}} = 19$ µeV, which is comparable to that of A1 and A3. The lowest $B$ field at which the gap closes is 0.7 T, corresponding to $|g_{\text{eff}}| \approx 4.4$, which is comparable to but smaller than that of device A. The extent of the topological phase is $\delta V_p \approx 1.5$ mV and $\delta B = 0.2$ T. On the other hand, device C’s ROI is at significantly lower plunger gate voltage $V_p \approx -2.3655$ V than device A’s. We attribute this to differences in the dielectric that are evident from Hall bar measurements. In addition, the gap closing in device C is more clearly visible in $A(G_{RL})$ than in $A(G_{LR})$, and the ZBP has much higher amplitude in $G_{LL}$ than in $G_{RR}$. The data is otherwise similar to that obtained from device A.

In Fig. 18, we show data from device D. There are two topological regions in the phase diagram. The TGP assigns maximum topological gaps of 17 µeV for the top and bottom regions, respectively. Even taken together, these regions occupy relatively small fraction of the phase diagram. The top cluster is detected at $B = 1.1$ T whereas
the bottom one appears at $B \gtrsim 1.8$ T. The latter is a relatively high field, but it is consistent with the broad distribution of fields that we find in simulations.

Our results on device D show that the TGP can even identify small ROI2s with small topological gaps.

### 4.2.3. Devices E and F not passing TGP

In Fig. 19, we show data from device E. This device has large regions with stable ZBPs at each end and thus shows a relatively large ROI1 in the Stage 1 of the TGP. However, in Stage 2 the system appears gapless throughout the region of interest: The induced gap closes and there are no signatures of gap re-opening in the non-local measurements. Since the system appears gapless in non-local conductances it is unclear if the correlated ZBPs correspond to a topological or trivial phase — either the topological gap is too small to be experimentally resolved or we observe a trivial state that couples to both sides because of the long coherence length that is expected in a system with very small gap. The fact that the ZBP is significantly brighter in $G_{RR}$ than in $G_{LL}$ as well as the similarity of finite-bias features in local measurements hints towards the second scenario. In both cases, such a phase would not be suitable for topological quantum computation. This example demonstrates the importance of Stage 2 of the TGP where non-local conductance is measured in order to identify false positives from Stage 1.

Meanwhile, device F does not have any regions with stable ZBPs at both ends, as may be seen in Fig. 20. The absence of correlations may be due to an inhomogeneous slowly-varying potential along the nanowire. The ZBPs that are seen at one end or the other are very similar to the ZBPs that are seen in devices passing the TGP. However, the ZBP that show up in more than 70% of cutter settings show no stable correlations between the two junctions. They may originate from a trivial Andreev bound states (ABS) crossing zero energy or stable ZBPs, dubbed quasi-MZMs, that appear due to a slowly-varying potential near the junction. Such states do not span over the whole length of the wire. The absence of a large enough cluster of correlated ZBPs causes this device to fail Stage 1 of the TGP.

### 5. SUMMARY AND DISCUSSION

In the previous sections, we have presented a summary of observed phenomena in gate-defined semiconductor nanowires coupled to a superconductor. We have demonstrated that, when devices A-D are tuned to the single sub-band regime, they yield data passing the TGP at magnetic fields in the range 1-2.5 T. We have observed topological gaps as high as $\Delta_{\text{topo}}^{\text{max}} \approx 60 \mu$eV. We emphasize that our results are reproducible within the same cooldown and between different cooldowns, as we have shown for device A. In short, our main empirical result is that multiple devices have passed the TGP.

These measurements represent strong evidence for the observation of a topological superconducting phase supporting MZMs. The TGP has been tested with extensive simulations, reliably identifying topological regions of the phase diagram of simulated devices and correctly distinguishing trivial Andreev bound states from Majorana zero modes. We found that, for a simulated device, there is > 90% probability that, when the TGP finds an ROI2, there is a topological phase in this region of its phase diagram.

In order to guide incremental progress towards passing the TGP, we relied on our estimates of the material and disorder requirements that gate-defined nanowires must satisfy. We developed designs and fabrication processes capable of meeting these requirements.

In the remainder of this section, we turn to the inter-
pretation of our results. The stability of the identified topological phase as a function of $B$ and $V_p$ is an important consistency check for our results. For the extracted effective $g_{\text{eff}}$-factor in measurement A1, $\delta B \approx 500$ mT corresponds to a Zeeman energy of $80 \mu$eV and, for the calculated lever arm of $\approx 85$ meV/V, $\delta V_p \approx 1.5$ mV corresponds to a chemical potential shift of $128 \mu$eV, see Eq. (1). In other words, the phase space extent in field is 3.5 times and the extent in gate voltage is 3.9 times the maximum topological gap of 23 meV. In measurement A2, we found that the topological region in Fig. 12 extends over a maximum $B$-field range $\delta B = 500$ mT and a maximum $\delta V_p = 2.5$ mV, corresponding, respectively, to energy scales of $80 \mu$eV and $213 \mu$eV. The other devices/measurements have similar stability in $B$ and $V_p$. Since the topological phase has an irregular shape, its area is smaller than the product of $B$ and $V_p$; it is listed in Table III, where the areas of the other measured topological regions is also listed. All of the devices have $\nu_{\text{SOI2}}$ in the range $0.1$-$0.5$ mV-T, and they have $\nu_{\text{SOI2}}$ values that are larger than $(\Delta_{\text{topo}}^\text{max})^2$ — in some cases, substantially larger — except device B. Note, however, that device B may have a larger SOI2 than what we can see in Fig. 15, extending below $V_p = -1.1580$ V. In other words, the observed candidate MZMs are stable with respect to parameter changes comparable to or larger than the maximum topological gap, which is an intrinsic energy scale of the problem that was determined from non-local conductance measurements.

The summary of the simulated data in the magnetic field range $B \leq 2.5$ T, which is comparable to experiment, is shown in Table IV. Here we present a brief summary; the raw data set is available [96]. The TGP yield and the average volume of SOI2 decreases with disorder strength (leaving aside the case of $n_{SOI,\text{int}} = 0.1 \cdot 10^{12}$/cm$^2$ which requires a different TGP calibration). The observed phase space of the topological phase is consistent with the results of simulations presented in Table IV, where we found that simulated SLG-$\beta$ and DLG-$\varepsilon$ devices had mean $\nu_{\text{SOI2}}$ in the range $0.1$-$0.2$ mV-T, but with a distribution that has long tails extending up to large volumes. Similarly, our simulated SLG-$\beta$ devices have $\Delta_{\text{topo}}^\text{max}$ values in the range $23$-$35$ $\mu$eV while our simulated DLG-$\varepsilon$ devices have $\Delta_{\text{topo}}^\text{max}$ values in the range $25$-$29$ $\mu$eV, both with long tails at large gaps. Device A would appear to be in the tail of the distribution, both with respect to $\Delta_{\text{topo}}^\text{max}$ and $\nu_{\text{SOI2}}$ while device B appears to be in the tail of the distribution with respect to $\Delta_{\text{topo}}^\text{max}$. In summary, the phase space for the topological phase is roughly as large as we would expect for a maximum topological gap of $20$-$60$ $\mu$eV and broadly consistent with our simulations. We note that this is a larger gap than in early measurements of the $\nu = 5/2$ fractional quantum Hall state [106, 107] and further note that the topological gap at $\nu = 5/2$ subsequently increased dramatically with material quality [108, 109].

The measured $\Delta_{\text{topo}}^\text{max}$, $\nu_{\text{SOI2}}$, $B_{\text{SOI2}}$ values in Table III are consistent with the simulated values in Table IV, which further validates the simulation model that was used to estimate the FDR. The primary outliers are $\nu_{\text{SOI2}}$ for measurements A1 and A2 and $\Delta_{\text{topo}}^\text{max}$ for device B; they are substantially larger than the mean values in simulations, but within the long tails of the non-Gaussian distributions found in simulations (see Appendix D for details). This consistency between simulated and measured values validates the model used to test the TGP, as suggested in Ref. 104.

We now consider other potential explanations of our results. According to our simulations, the probability that a device that passes the TGP does not have a topological phase overlapping the ROI2 is less than 10%, so any other explanation is extremely unlikely, though not impossible. For an intuitive understanding of why other explanations are unlikely, let us discuss trivial ZBPs. First, we observe that all of our devices have trivial ZBPs, even the ones that pass the TGP. Often, they occur at only one junction, but they sometimes occur at both junctions and they can even be stable to changes in junction transparency and also to changes in $B$ and $V_p$. For instance, there are stable ZBPs at both junctions in measurement A1 for $1$ T $< B < 2$ T and $V_p \approx -1.173$ V, as may be seen in Fig. 10. In device E, there are stable ZBPs at both

| Device, measurement | Design, stack | $\Delta_{\text{topo}}^\text{max}$ | $g_{\text{eff}}$ | $\nu_{\text{SOI2}}$ | $\nu_{\text{SOI2}}$ | $B_{\text{SOI2}}$ | GB |
|---------------------|--------------|----------------|-------------|-----------------|-----------------|------------|-----|
| A, A1               | SLG-$\beta$  | 23            | 5.6         | 0.5             | 12              | 1.7        | 78  |
| A, A2               | SLG-$\beta$  | 29            | 6.4         | 0.5             | 8.6             | 1.0        | 80  |
| A, A3               | SLG-$\beta$  | 22            | 6.4         | 0.2             | 5.7             | 1.0        | 90  |
| B                   | DLG-$\varepsilon$ | 61          | 3.7         | 0.2             | 0.3             | 2.1        | 92  |
| C                   | DLG-$\delta$ | 19            | 4.4         | 0.1             | 2.5             | 1.8        | 100 |
| D                   | DLG-$\delta$ | 17            | 4.5         | 0.1             | 1.4             | 1.1        | 93  |

TABLE III. For devices A-D passing the TGP, we list the the measured maximum topological gap $\Delta_{\text{topo}}^\text{max}$, the effective $g$-factor $g_{\text{eff}}$; the volume of the SOI2 shown in Sec. 4, in units of mV-T and $(\Delta_{\text{topo}}^\text{max})^2$; the “center-of-mass” magnetic field $B_{\text{SOI2}}$ of the SOI2; and the percentage of the boundary of the SOI2 that is gapless (GB%). Device D has two SOI2, and we list the values associated with both. From simulations, we estimate the lever arm as $d\mu/dV_p = 85$ meV/V for device A, 78 meV/V for device B, and 79 meV/V for devices C and D, see Table I.
TABLE IV. Statistics of ROI$_2$ and SOL$_2$ properties for simulated transport data from SLG and DLG devices for the average disorder strengths given in the first column. The third and fourth columns show the TGP yield as a fraction of devices that have at least one ROI$_2$. Its denominator indicates the total number of simulated devices; the numerator, the number of devices that pass the TGP. The TGP yield decreases with increasing disorder. All statistics in this table have been calculated with the magnetic field restricted to $B \leq 2.5$ T. The mean value of $\Delta_{\text{topo}}^\text{max}$ has weak dependence on the disorder strength, but the average phase space volume of an SOL$_2$, $V_{\text{SOI}2}$, decreases with increasing disorder, as may be seen in the forth column. For all disorder strengths simulated, $V_{\text{SOI}2} \sim O(0.1)$ mV·T. The last column lists $B_{\text{SOI}2}$, the average B field of an SOL$_2$, where the bar represents the statistical average over different disorder realizations. These regions occur at significantly higher magnetic field in the ε-stack, as expected since $\Delta_{\text{ind}}$ is larger and $g^*$ is smaller.

| Design, stack | $n_{2D,\text{int}}$ [$10^{12}$/cm$^2$] | Yield $\leq 2.5$ T | $\Delta_{\text{max}}^{\text{topo}}$ [μeV] | $V_{\text{SOI}2}$ [mV · T] | $B_{\text{SOI}2}$ [T] |
|---------------|--------------------------------------|--------------------|--------------------------------------|-----------------|----------------|
| SLG-β         | 1.0                                 | 47/50              | 23                                   | 0.2             | 1.9           |
|               | 2.7                                 | 23/50              | 34                                   | 0.1             | 1.5           |
|               | 4.0                                 | 24/49              | 34                                   | 0.1             | 1.5           |
| DLG-ε         | 0.1                                 | 24/50              | 35                                   | 0.2             | 2.2           |
|               | 1.0                                 | 28/50              | 29                                   | 0.2             | 2.3           |
|               | 2.7                                 | 13/50              | 30                                   | 0.2             | 2.2           |
|               | 4.0                                 | 16/50              | 30                                   | 0.1             | 2.2           |

A gap closing/re-opening could be caused by the orbital effects of the magnetic field. When half a flux quantum is threaded through the effective cross-sectional area of the device, the proximity effect is suppressed, and the gap closes. It re-opens when the flux increases still further, closing a second time when 3/2 flux quanta thread the active region. For device A, we expect a gap closing due to orbital effects at $B \geq 2.5$ T in higher sub-bands and even higher fields $>3$ T in the lowest sub-band. The observed gap closing is at much lower fields. Crucially, a gap closing due to orbital effects would be weakly-dependent on the gate voltage, as illustrated by the simulated phase diagrams of clean systems in Fig. 4, where the first closing due to orbital effects is a wide, nearly vertical white bar at $B \approx 2.5$ T that intersects the topological lobes at $V_p \approx -0.8$ V and $V_p \approx -1.0$ V (SLG-β) or $V_p \approx -0.95$ V (DLG-ε). We find similar behavior in the simulations that we used to test the TGP, which include disorder. On the other hand, as may be seen in Fig. 12, the gap closing that is observed in measurement A2 is strongly dependent on the gate voltage: at $V_p \approx -1.407$ V, the gap closes at $B \approx 0.6$ T, but at $V_p \approx -1.398$ V, it is still open at $B = 2$ T. Similarly, device C has a gap closing that occurs at $B \approx 0.7$ T at $V_p \approx -2.363$ but it is still open at $B = 1.3$ T at $V_p \approx -3.260$. Devices B and D have ROI$_2$s that occur at higher fields, but still below 2.5 T, and the gap closings are at, respectively, $B \approx 1.6$ T and $B \approx 1$ T. To determine the $V_p$ dependence of the gap closing in device B, we performed a large scale Stage 1 scan, which shows clear dependence, with a trivial gap that is still open at $B = 2$ T for some values of $V_p$. Hence, an explanation relying on the orbital effect of the magnetic field is not consistent with either the $B$ field value or the $V_p$-dependence of the observed gap closings/re-openings in devices A-D.

Of course, it is conceivable that the bulk gap closes and re-opens accidentally and that trivial ZBP also accidentally occur for the same $B$ and $V_p$. But to pass the TGP, the accidental closing would have to occur over an entire curve in the $B$-$V_p$ phase space and, moreover, the trivial ZBPs would have to persist over the enclosed region. Of course, we cannot rule this out completely. However, such coincidences do not require any physics that is not incorporated in our simulations. Hence, they could occur in our simulations, and we can quantitatively bound their probability. The false discovery rate (FDR) that we estimate from simulations is $\leq 8$% at a 95% confidence level for all of the device designs, material stacks, and disorder levels that we have simulated, which implies that there is a low probability that data from devices A-D can be explained by trivial ZBPs that occur coincidentally with an accidental gap closing/re-opening instead of a topological phase.
Trivial region
Trivial regions
MZM
Topological region
Quantum dot
Topological regions
MZM
Semiconductor

FIG. 21. (a) The linear tetron, a minimal device for performing fusion. The two outer regions must be tuned into the topological phase via the TGP, while the middle section must be in the trivial phase. This results in a device with four MZMs. (b) Two two-sided tetrons, with which measurement-based braiding can be performed. There are 5 topological sections. The middle (purple) one is a coherent link that is used for connecting the left and right of the two tetrons.

6. LOOKING AHEAD

A reliable process for tuning devices into the topological phase is an essential step on the journey to topological quantum computation, which relies on the fusion and braiding of anyons. Networks of such wires can be assembled into a many-qubit device, and this protocol can be used to tune each wire within a qubit into the topological phase. The linear tetron qubit [110, 111] is a minimal device for performing two non-commuting fusion operations; it is shown schematically in Fig. 21(a).

There are two outer topological sections, separated by a trivial section. Fusion outcomes for different pairs of MZMs are measured by coupling these MZMs to adjacent quantum dots. By measuring different sequences of pairs of MZMs, we can directly measure the fusion rules, a topological invariant of the state. The parameter space of such a device is simply too large to explore in the hope of finding a suitable operating point unless each of the outer sections of the nanowire is individually tuned into a topological phase, which can be achieved using the TGP.

Coherent manipulation of the encoded quantum state, for example through measurement-based implementations of braiding transformations [117, 118], requires an even more complex device, as shown in Fig. 21(b). This device consists of two superconducting islands, each comprised of two topological segments linked together by a short region of trivial superconductor, and thus contains two qubits. We refer to this configuration as a two-sided tetron because MZMs are on each side of the device. The additional topological wire between the qubit islands, shown in purple, is added to allow measurements between MZMs on opposite sides of the islands. In this device, unitary Clifford gates on one of the two qubits can be performed by using the other as an auxiliary qubit and performing a sequence of single- and two-qubit measurements [111]. Despite the even larger parameter space, these devices can be tuned using the TGP. Continued improvement in simulation, growth, fabrication, and measurement capabilities will be required to achieve the topological gap required for such coherent operations.

ACKNOWLEDGMENTS

We thank Greg Boebinger, Sankar Das Sarma, Michel Devoret, Klaus Ensslin, Leonid Glazman, Bert Halperin, Dale van Harlingen, Kam Moler, Krysta Svore, and Matthias Troyer for extensive discussions. We are grateful to Edward Lee and Todd Ingalls for their assistance with figures. We thank Leo Kouwenhoven for helpful comments on a previous version of this manuscript.

Correspondence and requests for materials should be addressed to Chetan Nayak (cnayak@microsoft.com).

†Morteza Aghaeae, Arun Akkala, Zulfi Alam, Rizwan Ali, Alejandro Alcaraz Ramirez, Mariusz Andrzejczuk, Andrey E. Antipov, Pavel Aseev, Mikhail Astafev, Bela Bauer, Jonathan Becker, Srini Bodapati, Frenk Boekhout, Jouri Bommer, Esben Bork Hansen, Tom Bosma, Leo Bourdet, Samuel Boutin, Philippe Caroff, Lucas Casparis, Maja Cassidy, Sohail Chatooor, Anna Wulf Christensen, Noah Clay, William S. Cole, Fabiano Corsetti, Ajuan Cui, Paschalis Dalampiras, Anand Dokania, Gijs de Lange, Michiel de Moor, Juan Carlos Estrada Saldaña, Saeed Fallahi, Zahra Heidarnia Fathabadi, John Gamble, Geoff Gardner, Deshan Govender, Flavio Griggio, Ruben Grigoryan, Sergei Grinon, Jan Guébelger, Sebastian Heedt, Jesús Herranz Zamorano, Samantha Ho, Ulrik Laurens Holgaard, William Hvidtfeldt Paldkær Nielsen, Henrik Ingerslev, Linda Johansson, Jeffrey Jones, Ray Kallagher, Farhad Karimi, Torsten Karzig, Evelyn King, Maren Elisabeth Kloster, Christina Knapp, Dariusz Kocan, Jonne Koski, Pasi Kostamo, Peter Krostrup, Mahesh Kumar, Tom Laeven, Thorvald Larsen, Kongyi Li, Tyler Lindemann, Julie
Appendix A: Effects of disorder

A.1. Projection to proximitized nanowire model

The disorder-free limit of the single-sub-band regime is well-represented by a Hamiltonian of the form of Eq. (1):

\[
H = Z'(H_{SM} - \tilde{\Gamma}_OFC)Z \tag{A1}
\]

In Eq. (A1), the effective mass, \( g \)-factor, and spin-orbit coupling in \( H_{SM} \) — obtained by projecting the full model for the device designs and material stacks described in Secs. 2.2 and 2.3 into the lowest sub-band — take the values given in Table I. The parameters in Table I are weakly density-dependent, so they were computed at \( \mu = 0.21 \text{ meV} \), which corresponds to a Fermi wavelength in range \( k_F \approx 30-80 \text{ nm} \). Compared to Eq. (1), there is a transformation \( Z \), described below, which is due to the renormalization of the electrons in the semiconductor by their coupling \( \Gamma \) to the Al, which has a superconducting gap \( \Delta_{Al} = 300 \text{ meV} \) and a Zeeman potential \( V_{x,sc} = g_{sc} \mu_B B/2 \) with a g-factor \( g_{sc} = 2 \).\(^7\) In the following we will neglect the orbital effect of the magnetic field on the superconductor, despite keeping the Zeeman splitting. The justification for this is that the SC thickness is \( d < 10 \text{ nm} \) and we estimate the disordered coherence length in the Al, \( \xi_{Al} \), to be around 40 nm. Orbital effects can be neglected when the depairing energy is small compared to the gap; this is justified \((\tilde{\Gamma} \ll \Delta_{Al} \ll V_{x,sc}^2)\). Additionally, the Zeeman potential experienced by the SM now includes an induced contribution from the Al, \( \tilde{V}_x \approx V_x + \Gamma V_{x,sc}/\sqrt{\Delta_{Al}^2 - V_{x,sc}^2} \).

In all three cases — SLG \( \beta \)-stack and DLG \( \alpha \)- and \( \delta \)-stacks — the transformation by \( Z \) as well as the induced Zeeman energy from the Al suppress the effective g-factor below \( g_{SM} \). Hence, as discussed in the previous section, the coupling between the semiconductor and the superconductor, \( \Gamma \), should not be too large or else the g-factor will be strongly suppressed and the topological phase will be pushed to high \( B \)-fields where the Al approaches the Clogston limit. On the other hand, \( \Gamma \) cannot be too small, either, or else the induced gap \( \Delta_{ind} \approx \Delta_{Al}/(\Gamma + \Delta_{Al}) \) will be small.

Here we turn to the renormalization factor \( Z \). The Green’s function of a hybrid SM-SC system is given, in general, by

\[
G(\omega) = [\omega - H_{SM} - \Sigma(\omega)]^{-1} \tag{A2}
\]

with a self-energy \( \Sigma(\omega) \) obtained by integrating out the SC degrees of freedom using the tunneling Hamiltonian model defined in Ref. 120,

\[
\Sigma(r, r', \omega) = -\int dx_1 dx_2 T^t(r, x_1)T(x_2, r') G_{sc}(x_1, x_2, \omega). \tag{A3}
\]

Here, the integrals are taken over the superconducting domain with \( x = (z, r) \) where \( z \) and \( r \) are out-of-plane and in the plane of the interface, respectively; the tunneling matrix elements read

\[
T(x_1, r) = \delta(r_1 - r)\delta(z_1)\partial_z \tag{A4}
\]

The delta function here corresponds to momentum conservation parallel to the interface whereas \( \partial_z \) enhances transmission for electrons in the superconductor that are incident with momentum normal to the interface. After some algebra [27], one finds that \( \Sigma(r, r', \omega) \propto \delta(r - r') \int d\epsilon G_{sc}(\omega, k) \) where \( \delta(r - r') \) represents the rapid decay of the self-energy on the scale of the Fermi wavelength in the metal.

We now derive the expression for the self-energy in the presence of disorder in Al which is crucial for understanding the proximity effect [27, 121–124]. Indeed, disorder removes momentum conservation constraints and effectively increases the tunneling rate \( \Gamma \). The disorder-averaged self-energy can be written as

\[
\langle \Sigma(r, r', \omega) \rangle = \tilde{\Gamma} g(\omega) \delta(r - r'), \tag{A5}
\]

where the Usadel Green’s function \( g(\omega) \) represents the diffusive limit of a spin-split s-wave superconductor. Here we neglect the orbital contribution of the magnetic field, as justified above. Analytic expressions for this Green’s function in this limit have been recently reported in Refs. [125, 126].

Now, we would like to obtain a frequency-independent effective Hamiltonian with eigenvalues that approximate the poles of \( G(\omega) \) (A2), but, in order to do so, it is insufficient to take the static limit by replacing \( \Sigma(\omega) \) by \( \Sigma_0 \equiv \Sigma(0) \). A better, widely used, approximation involves grouping the linear-in-frequency part of the self-energy, \( \Sigma_1 \equiv \partial_\omega \Sigma(\omega)|_{\omega=0} \), with the frequency of the Green’s function to define an overall renormalization of the energy scale before taking the static limit. Here we describe a generalization of that method.

Specializing the expressions in [125, 126] to the static and linear-in-frequency parts, we obtain

\[^7\] Note that this effective Hamiltonian is only valid provided \( \Delta_{Al} \) is not too small. In the more general case, integrating out the superconductor leads to an effective action that is non-local in time and has an energy-dependent renormalization.
Disorder strength, $V$, is where the disorder potential, projected into the lowest sub-band, is its sample-averaged autocorrelation:

$$\Sigma_0 = -\frac{\Gamma(-V_{x,SC}\sigma_x \tau_x + \Delta_{\text{AI}} \sigma_y \tau_y)}{\sqrt{\Delta_{\text{AI}}^2 - V_{x,SC}^2}},$$

(A6)

$$\Sigma_1 = -\frac{\Gamma(\Delta_{\text{AI}}^2 - V_{x,SC} \Delta_{\text{AI}} \sigma_x \tau_x)}{(\Delta_{\text{AI}}^2 - V_{x,SC}^2)^{3/2}},$$

(A7)

and the Green’s function in this linearized representation is

$$\tilde{G}(\omega) = [\omega(1 - \Sigma_1) - H_{\text{SM}} - \Sigma_0]^{-1}.$$  

(A8)

As a consistency check, we can consider the well-known $V_{x,SC} = 0$ limit, where $\Sigma_0 = -\Gamma \sigma_y \tau_y$ and $\Sigma_1 = -\Gamma/\Delta_{\text{AI}}$ and recover

$$\tilde{G}_{V_{x,SC}=0}(\omega) = \frac{\Delta_{\text{AI}}}{\Delta_{\text{AI}} + \Gamma} \left[\omega - \frac{\Delta_{\text{AI}}}{\Delta_{\text{AI}} + \Gamma}(H_{\text{SM}} - \Gamma_0 \sigma_y \tau_y)\right]^{-1},$$

(A9)

with poles at the eigenvalues of the renormalized effective Hamiltonian

$$H_{\text{eff}} = \frac{\Delta_{\text{AI}}}{\Delta_{\text{AI}} + \Gamma} (H_{\text{SM}} - \Gamma_0 \sigma_y \tau_y),$$

(A10)

recovering the previous results of Ref. [27]. In the more general case where $V_{x,SC} \neq 0$, $\Sigma_1$ is not proportional to the identity. Hence, we have to be careful in factoring out the coefficient of $\omega$. This is because we require a hermitian $H_{\text{eff}}$, and in general the matrix $(1 - \Sigma_1)^{-1}(H_{\text{SM}} + \Sigma_0)$ is not hermitian. To resolve this, we take a symmetric product, defining $Z = (1 - \Sigma_1)^{-1/2}$ and obtain the result

$$H_{\text{eff}} = Z^\dagger (H_{\text{SM}} + \Sigma_0) Z.$$  

(A11)

Finally, we now extend the model to include potential disorder in the semiconductor:

$$H = Z^\dagger (H_{\text{SM}} - \tilde{\Gamma}_0 \sigma_x \tau_x + H_{\text{Dis}}) Z,$$  

(A12)

where the disorder potential, projected into the lowest sub-band, is

$$H_{\text{Dis}} = \int_0^L dx V(x) \psi_{\sigma}^\dagger(x) \psi_{\sigma}(x).$$

(A13)

For the disorder mechanisms we have included, we find that the random potential can be approximately characterized by its sample-averaged autocorrelation:

$$\langle V(x)V(x') \rangle = \delta V^2 \exp(-|x - x'|/\kappa).$$

(A14)

The projected disorder parameters, variance $\delta V < 2$ meV and correlation length $\kappa = 80, 115$, and $120$ nm (for $\beta$, $\delta$, and $\varepsilon$-stacks, respectively), are obtained for the same design and materials stack as the uniform parameters given in Table 1. Here, the various sources of disorder and their strengths have been distilled to two numbers. These parameters’ relation to the underlying microscopic disorder depends on both the device geometry and the defect types and densities. We show the relation between $\delta V$ and $n_{2D,\text{int}}$ for SLG and DLG designs for the $\beta$, $\delta$, and $\varepsilon$ stacks in Fig. 22.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure.png}
\caption{The effective parameter $\delta V$ describing the disorder strength as a function of $n_{2D,\text{int}}$, the density of charged defects at the semiconductor-dielectric interface, for the SLG-$\beta$, DLG-$\delta$, and DLG-$\varepsilon$ design and material stacks.}
\end{figure}

A.2. Disorder-driven phase transition

In general, disorder suppresses the topological phase [127–137], causing important changes to the phase diagram of Fig. 1. For weak disorder, this leads to a decrease of the topological gap and an increase of the disorder-driven superconducting coherence length in the topological phase. As the disorder strength is increased, these variations can create small non-topological regions in an otherwise topological wire, thus nucleating additional subgap states at the domain walls between topological and non-topological regions. Eventually, these subgap states hybridize and lead to the breakdown of the topological phase through Griffiths’ effects [127]. In the limit in which the clean topological gap $\Delta_T$ is small compared to the Fermi energy, the stability condition for the topological phase is $\xi_c > \xi_T$ [130], where $\xi_c$ is the localization length in the normal state (which in one dimension and for short-ranged disorder is equal to twice the mean free path [138]) and $\xi_T$ is the coherence length in the clean topological superconductor. Equivalently, this can be rephrased in terms of energy scales as $\Delta_T = \hbar/2$, where $\tau$ is the elastic scattering time. In the effective model governed by $H = H_{\text{SM}} + \Delta_{\text{ind}} O_{\text{SC}} + H_{\text{Dis}}$, the scattering rate due to the random potential $V(x)$ can be evaluated to lowest order in $\delta V$:

$$\frac{\hbar}{\tau} = \frac{\delta V^2}{2E_F} \frac{2k_F\kappa}{1 + (2k_F\kappa)^2}.$$  

(A15)

Here, $E_F$ and $k_F$ are the Fermi energy and momentum. Thus, the transition at $\Delta_T = \hbar/2$ occurs at a critical value $\delta V^2_c$:

$$\delta V^2_c = 4E_F \Delta_T \left[1 + (2k_F\kappa)^2\right]/2k_F\kappa.$$  

(A16)

This expression for the critical disorder strength is valid in the regime of weak disorder and small gap, $\Delta_T \ll E_F$. However, the nanowire in the single subband regime has a small Fermi energy, so the latter requirement is difficult to satisfy. Moreover, disorder sources with correlation lengths $\kappa \lesssim k_F^{-1}$ cause stronger scattering than short-range disorder $\kappa k_F \ll 1$, as may be seen from Eq. (A15). For realistic disorder levels, it is necessary to go beyond lowest-order in $\delta V$. Consequently, the precise location of the disorder-driven phase transition is

\[...\]
more complicated than Eq. (A16) when the clean topological gap and disorder strength are comparable to the Fermi energy [101, 133]. Finally, there are important differences between the thermodynamic limit and finite-sized systems, where the phase transition is rounded into a crossover. In order to understand these additional complexities, we calculate the disordered coherence length numerically using the transfer matrix method, as we discuss in the next two subsections.

A.3. Length scales and topological phases in finite systems

Since we are concerned in this paper with topological phases in finite systems with disorder, we must pay attention to several important length scales. We will denote the superconducting coherence length in the wire by \( \xi(0) \). It is the distance that a zero-energy unpairoed electron can penetrate into the proximitized nanowire. In the topological phase, \( \xi(0) \) corresponds to the localization length of a Majorana zero mode. The coherence length \( \xi(0) \) diverges at the phase transition between the trivial and topological superconducting phases. In the topological phase, when disorder is very weak, \( \xi(0) \) approaches its clean value \( \xi_T \). Increased disorder elongates \( \xi(0) \) in the topological phase, while it shortens \( \xi(0) \) in the trivial phase.

In a perfectly clean system, there would be no states below the clean topological gap \( \Delta_T \), apart from the MZMs, and states above the gap would all be extended. However, even weak disorder localizes all states except the zero-energy state at the critical point, as noted in Sec. 2.1. It also causes localized states to appear below \( \Delta_T \). We will call the energy-dependent localization length, calculated for the Bogoliubov-de Gennes Hamiltonian (1), \( \xi(E) \). At low energy, \( \xi(E) \to \xi(0) \). When disorder is very weak, the density of states is very low for \( E < \Delta_T \), and these states have localization lengths that grow smoothly as a function of \( E \), increasing from \( \xi(0) \) to \( \xi(\Delta_T) \). At energies \( E \geq \Delta_T \), the localization length is proportional to the mean-free-path \( \ell \). If \( \xi(\Delta_T) > \ell \), then states above \( \Delta_T \) will appear to be extended and there will be an apparent transport gap \( \Delta_{tr} \lesssim \Delta_T \), which is the gap to “extended states,” namely the states whose localization lengths \( \xi(E) \) are larger than the system size. Turning now to the case of more general disorder strengths, we define \( \xi(\Delta) \) as the maximum value of \( \xi(E) \) for \( E < \Delta_{ind} \). Our devices are designed so that \( \xi(\Delta) \geq L \). When this holds, we can measure the transport gap \( \Delta_{tr} \), which is the minimum \( E \) for which \( L/\xi(E) \) is small enough that states at energy \( E \) are visible in bulk transport. We explain these measurements in Sec. 3 and Appendix C.1.

The decay of subgap states at small energies \( E \ll \Delta_T \) is controlled by \( \xi(0) \) while transport by excited states is controlled by \( \xi(\Delta) \). Hence, if we observe a ZBP at one junction, the amplitude to observe it at the other junction decays as \( e^{-L/\xi(0)} \), but if we observe an excited state of the bulk at one junction, the amplitude to observe the same state at the other junction decays at least as fast as \( e^{-L/\xi(\Delta)} \). Thus, depending on the disorder level and device length, there are three parameter regimes for the operation of a topological device. The first regime is when \( \xi(0) \ll \xi(\Delta) \ll L \). In this limit, the device is longer than any of the finite length scales that characterize the topological phase. Hence, there is no characteristic energy scale of the bulk topological phase that can be extracted from transport measurements.

In the second regime, \( \xi(0) \ll L \lesssim \xi(\Delta) \). In this regime, which we will call the asymptotic regime, the device is much longer than the localization length of a low-energy bound state. When ZBPs are observed at both junctions, we know that there are two distinct bound states, one at each junction. Since \( L \lesssim \xi(\Delta) \), there are excited states that are effectively extended, i.e., have localization lengths that are comparable to or longer than the system size. The transport gap is the energy gap to such states.

Finally, there is a third regime, in which \( \xi(0) \ll L \ll \xi(\Delta) \). This is a crossover regime in which the system is longer than the MZM localization length but it may not be so much longer that we are in the asymptotic limit. In this case, there may be some bulk transport at zero energy even when \( \Delta_{tr} > 0 \) because the \( e^{-L/\xi(0)} \) contribution is not negligible. Consequently, the system will be intermediate between the asymptotic regime and the critical regime that we define in the next paragraph. As \( \xi(0) \) is reduced, the system will move more firmly into the asymptotic topological regime. However, there isn’t a particular value of the ratio \( L/\xi(0) \) that separates the crossover regime from the asymptotic regime; the evolution from one to the other with increasing \( L/\xi(0) \) is smooth.

None of the three regimes mentioned above — thermodynamic, asymptotic, and crossover — is possible near the critical point, where \( \xi(0) = \infty \). When \( L \ll \xi(0) \), the system is in the critical regime, and we can’t distinguish it from a critical system. Even in a device of length \( L = 3 \mu m \), this is a fairly broad region. As we shall see, for intermediate disorder strengths, over much of the parameter range in which the system would be in the topological phase for \( L \to \infty \), the system is in the critical regime because the correlation length is long and \( L \ll \xi(0) \).

As an illustration of these various regimes, we calculate \( \xi(0) \) for the model Eq. (A12) using the transfer matrix method [139]. In Fig. 2 we plot the result for DLG, \( \delta \)-stack parameters from Table I and characteristic disorder strengths \( 5V = 0.3 \) and \( 0.9 \) meV. As \( \xi(0) \) is a function of the chemical potential and applied magnetic field, a finite wire can go from the critical to crossover to asymptotic regimes depending on these parameters. When the system is in the thermodynamic, asymptotic, or crossover regimes, it is deep in a \( \Delta_T > 0 \) phase. The devices discussed in this paper are in the asymptotic or crossover regimes. We discuss the implications for transport measurements when we described the topological gap protocol in Sec. 3 and Appendix C.1.

A.4. Finite-size behavior of topological invariants

We now consider the finite-size behavior of the invariants distinguishing the topological and trivial phases. We consider the “scattering invariant” [103] and the Pfaffian invariant [9, 97]). The scattering invariant is defined for an open system with a junction to a normal lead: \( SI = \text{sgn det} \tau \in [-1, 1] \), where \( \tau \) is the reflection matrix. When \( SI = -1 \), there is an MZM at the junction. The scattering matrix \( \tau \) depends on how open or closed the junction is. In a finite-sized system, an MZM at a junction will hybridize with the MZM at the other end of the wire with strength \( e^{-L/\xi(0)} \) (giving \( SI = +1 \)) unless it is coupled more strongly to the lead. If the MZM couples poorly to the leads, then we will erroneously find \( SI = +1 \). If the MZM couples more strongly
FIG. 23. The coherence length $\xi(0)$ evaluated numerically by the transfer matrix method for the model in Eq. (A12) with DLG, $\varepsilon$-stack parameters from Table I and characteristic disorder strengths (a) $\delta V = 0.3$ meV and (b) $\delta V = 0.9$ meV. The colorscale saturation highlights the divergence of $\xi(0)$, indicating the phase transition from the low-field trivial phase to the high-field topological phase. The solid and dashed lines mark contours of constant $\xi(0) = 1$ and 3 $\mu$m respectively. For our 3 $\mu$m simulations in Sec. 2.6, the region enclosed by dashed lines roughly represents the “critical” regime, while the area between dashed and solid lines is in the “crossover” regime where $L > \xi(0)$, but we still expect finite-size effects and mesoscopic fluctuations.

to the lead than to its partner at the other end, then we will have $\Sigma = -1$ in a finite-size system. Note, however, that we will also find $\Sigma = -1$ if the second MZM is much closer than distance $L$ but has small hybridization with the one at the junction, namely the “quasi-MZM” scenario [46–49, 51]. The Pfaffian invariant $Q$ is defined for a closed system as the relative sign of the ground state parity between periodic (PBC) and anti-periodic (APBC) boundary conditions. $Q = \text{sgn}[\text{Pf}(A_{\text{APBC}})]\text{sgn}[\text{Pf}(A_{\text{PBC}})]$ when the Bogoliubov-de Gennes Hamiltonian is written in terms of real fermionic operators $\gamma_{2i-1} = c_i + c_i^\dagger$, $\gamma_{2i-1} = -i(c_i - c_i^\dagger)$ so that it takes the form $H = (i/2)\sum_{i,j} A_{ij}\gamma_i\gamma_j$. In a finite system, we will have $Q = -1$ when the hybridization of the two MZMs is larger via the periodic boundary condition that connects the two ends than the $e^{-L/\xi(0)}$ hybridization that occurs through the bulk of the wire. In summary, both invariants rely on $e^{-L/\xi(0)}$ being smaller than the coupling to the lead or the boundary condition. This is the limit in which the topological phase can be defined; it becomes more clearly distinct from the trivial phase in a continuous fashion as $e^{-L/\xi(0)} \rightarrow 0$. In the next section, we will use the Pfaffian invariant to illustrate the combination of finite-size effects and disorder on the phase diagram. In Appendix D.3, we will use the scattering invariant to test the accuracy of the TGP because the scattering invariant can be calculated for the same device geometry and junction settings as used in transport simulations and measurements.

Appendix B: Electrostatic calibration from Hall bars

Each of the topological gap devices described in the main text is accompanied by a Hall bar device subject to the same growth and fabrication processes; this Hall bar enables a characterization of the bulk material quality. The full density dependence of the Hall mobility has been widely used previously to identify and quantify dominant scattering mechanisms in 2DEGs [137, 140–148]. In particular, across all samples, the low-density mobility rapidly increases with increasing density, consistent with the mobility being dominated there by scattering from the long-range Coulomb potential of remote impurities.

In our simulations, we calculate (i) the gate-voltage dependence of carrier density $n_e(V_g)$ for a 2DEG in our materials stack in a standard Schrödinger-Poisson framework; and (ii) the remote-impurity-limited mobility $\mu(V_g)$ in the Boltzmann-Born formalism. Both of these functions are parameterized by the density and location of impurities, and an effective composite dielectric permittivity. These parameters are used to simultaneously fit the model traces to experimental data. As mentioned in the main text, our best fits to density and mobility measurements over a variety of samples suggested a simplification in which an effective 2D impurity density $n_{2D,\text{int}}$ is placed in an “impurity layer” at the interface between the barrier and the gate dielectric. Small changes in the position or width of the impurity layer can be compensated by tuning the impurity density, but large changes modify the overall density dependence of the mobility and result in poor fits. Therefore, the values of charge impurity density that we quote here depend on the disorder model employed, with the goal of this model being to provide a consistent description of the impact of fixed charges on both the Hall mobility and TGP measurements.

Figure 24 shows a representative example measurement of mobility versus density for the Hall bar proximate to device A [note that the low-density upturn in $n_e(V_g)$ and non-single-valued $\mu(V_g)$ arise due to a measurement artifact and these points are excluded from the fitting]. The solid black lines represent our point estimate traces corresponding to the most-probable values of the effective impurity density, $n_{2D,\text{int}} = 2.7 \cdot 10^{12}/\text{cm}^2$, and effective dielectric permittivity.

Using similar analysis, we extracted the corresponding effective charged impurity densities at the interface with the dielectric for devices C-F yielding $1.1 \cdot 10^{12}/\text{cm}^2$, $10^{12}/\text{cm}^2$, $3.1 \cdot 10^{12}/\text{cm}^2$, and $3 \cdot 10^{12}/\text{cm}^2$, respectively.
First, to accelerate the search for ZBPs in Stage 1, rather than doing lengthy bias-voltage sweeps, we employ the third-harmonic (3ω) technique described in Ref. 149. This gives a direct measurement of $d^3I_R/dV_R^3$, which is the curvature of the local conductance $dI_R/dV_R$. When $d^3I_R/dV_R^3$ is negative and above the noise level, it indicates the presence of a ZBP. Using this technique, we are able to scan over a large area in phase space by varying four parameters: $B$, $V$, and the two cutter gate voltages $V_c$, $V_e$ that modulate the junction transparencies. We further facilitate this by restricting the cutter gate voltages so that $G_N$ at each junction is limited to the range 0.1-1 $e^2/h$ as a compromise between sufficient visibility and remaining in the tunneling regime. In Stage 2, we will also sweep $V_b$, but will restrict ($B$, $V_b$) to smaller ranges.

Second, $G_{LR}$ and $G_{RL}$ may receive contributions from line impedances in the measurement circuit, which we account for by taking the full impedance network into account [150]. In addition, we correct for finite frequency effects by calibrating the resistances and capacitances in the measurement circuit, as explained in Appendix E. Finally, we remove any remaining voltage divider corrections and improve SNR by focusing on the parts of the non-local conductances that are antisymmetric in bias voltage, $A(G_{RL})$, $A(G_{LR})$:

$$A(G_{RL}(V_b)) \equiv [G_{RL}(V_b) - G_{RL}(-V_b)]/2$$

and similarly for $G_{LR}$. A discussion of relevant multi-terminal conductance symmetry relations may be found in Ref. [151].

Third, the transport gap extracted from $A(G_{RL})$ will not, in general, be the same as that extracted from $A(G_{LR})$. The underlying transport gap is the same, but the two non-local conductances may not be the same due to the different ways in which local matrix elements enter $G_{LR}$ and $G_{RL}$. [We will see an example of this in simulated data in Fig. 26(b,c) in Appendix D.3.] This can obscure a gap narrowing or closing. Hence, for any given $V_e$ and $B$, we determine the induced gap as the lower of the gaps extracted from $A(G_{RL})$ and $A(G_{LR})$. Consequently, the observation of non-vanishing $A(G_{LR})$ or $A(G_{RL})$ at bias voltages approaching zero is a signature of a bulk gap closing. Note that the energy spectrum can be gapless due to the presence of disorder-induced localized states at low energies. The observed transport gap, extracted from $A(G_{LR})$ and $A(G_{RL})$, is the gap that we really care about since it is more predictive of qubit performance.

A fourth subtlety is that $A(G_{LR}(V_b)), A(G_{RL}(V_l))$ can be either positive or negative, depending on whether transport at that bias voltage is primarily due to electrons or holes. It can change sign as the matrix elements change as a function of $B$ or $V_p$, passing through zero when this occurs [102]. Such a sign change can appear as a very sharp increase in the induced gap, centered about some $B$ or $V_p$ value. In determining the zero-field induced gap, we simply avoid these points.

The situation is slightly more complicated for the topological gap, since it varies between zero at the phase transition and a maximum value that determines the stability of the topological phase. Hence, we will report both the median value of the gap over the SOI and also its maximum value. However, we will not extract the maximum from the single point at which it is largest. It is not uncommon to have a very small region over which the extracted topological gap is very large because one of the aforementioned sign changes occurs, suppressing the signal in $G_{LR}$ and $G_{RL}$. Hence, we define the “maximum topological gap” $\Delta_{\text{topo}}^{\text{max}}$ to be the upper quintile of measured gap values within SOI.

We add a note of caution here that the measured values of $\Delta_{\text{ind}}$ and $\Delta_{\text{topo}}^{\text{max}}$ are transport gaps, which are the lowest energy at which there is an excited state whose localization length is longer than the device length; they can be larger than the $\Delta_{\text{ind}}$ or $\Delta_{\text{topo}}^{\text{max}}$ expected for a clean system.

Fifth, we clarify the definition of the gapless boundary of an SOI. The boundary of the region is defined to consist of all points inside the SOI that neighbor the exterior of the SOI on the side or diagonally. Each such boundary point is then considered gapped if all of the neighboring points outside SOI are gapped. Otherwise the boundary point is considered gapless. Using this definition, we extract the fraction of the boundary points that are gapless.

### C.2. TGP parameters

The TGP is parametrized by thresholds that were fixed by an initial set of calibration simulations described in Appendix D.2 and then tested extensively by large-scale simulations for different disorder levels and device designs, as described in Appendix D.1. As a result, we have high confidence that ROI$_{28}$ overlap with the regions in parameter space where there is a topological phase, as we quantify in Appendix D.1.

In principle, this protocol is designed to detect any topological phase with a sizable gap. Finite experimental resolution and temperature, however, may obfuscate some of the topological signatures, giving rise to subtleties when interpreting the data that we discuss here.

A wire may have MZMs, but one or both of them may be slightly displaced from the end of the wire for some choices of junction transparency and, therefore, may not be visible. (Indeed, we see in Fig. 2(c) that the local density of states can...
be peaked a few hundred nanometers away from the junction in a simulation of an ideal disorder-free device.) For this reason, we do not insist that a ZBP be present for all junction configurations and, instead, consider a ZBP to be stable in Stage 1 if it is visible for at least 70%, of measured junction transparencies. We define the “cutter gate fraction” as the fraction of junction transparencies (or, equivalently, cutter gate settings) for which a ZBP is present. For instance, suppose we pick 5 cutter gate voltages \( V_{\text{c}} \) at the right junction such that \( G_{\text{c}}^{L} \) at the right junction takes the values 0.35, 0.49, 0.62, 0.76, 0.9\( e^2/h \) and similarly pick 5 cutter gate voltages \( V_{\text{b}} \) at the left junction so that \( G_{\text{b}}^{L} \) at the left junction ranges over the same five values. Then, a \((B, V_{b})\)-point will be said to exhibit stable ZBPs at both junctions if there are ZBPs at both junctions for > 70% of cutter gate pairs \((V_{\text{c}}, V_{\text{b}})\).

For Stage 2, we set a threshold percentage \((\text{ZBP})_{\text{th}}\) and define a stable ZBP as one that is visible for at least \((\text{ZBP})_{\text{th}}\) of junction transparencies. As we discuss further in Appendix D.2, we use calibration simulations to inform the choice \((\text{ZBP})_{\text{th}} = 60\%\) for the device parameters considered in this paper. For the junction transparencies given as an example in the previous paragraph, we would perform Stage 2 measurements for 5 different cutter gate pairs \((V_{\text{c}}, V_{\text{b}})\) such that \( G_{\text{c}}^{L} = G_{\text{b}}^{L} \approx 0.35, 0.49, 0.62, 0.76, 0.9\frac{e^2}{2h} \). A stable ZBP in Stage 2 would then need to be present for 3/5 cutter gate pairs.

A gap closing may not be visible even when it is present because \( A(G_{\text{c}}^{L}) \) and \( A(G_{\text{b}}^{L}) \) tend to be small at low bias voltage (due to their anti-symmetry in bias voltage) and will be suppressed even further by disorder and non-uniformity. Another reason why an SOI may be gapless along less than 100% of its boundary is that neighboring gapped regions may have been misidentified as non-topological (e.g. due to weak coupling of the MZMs to the leads or ZBP splitting due to a small topological gap). In case of such misidentification, such regions should actually be included in the SOI, which would be larger and gapless along its entire boundary. To account for both of these possibilities, we set a threshold percentage \((\text{GB})_{\text{th}}\). In order to qualify as an SOI, a cluster must be gapless along at least \((\text{GB})_{\text{th}}\) of its boundary. As we discuss in Appendix D.2, we use simulated transport data to inform the choice \((\text{GB})_{\text{th}} = 60\%\) for the device parameters discussed in this paper.

The non-local conductances \( A(G_{\text{RL}}^{L}) \) and \( A(G_{\text{LR}}^{L}) \) will never truly vanish at zero bias because there will at least be tunneling \( e^{-\Delta/L(\xi)} \) and thermally-activated \( e^{-\Delta/n/T} \) contributions.\(^8\) Hence, we need to give an operational definition for \( A(G_{\text{RL}}^{L}) \approx 0 \) and \( A(G_{\text{LR}}^{L}) \approx 0 \). To do this, we define a threshold value \( G_{\text{th}} \). Then, if \( A(G_{\text{RL}}^{L}(V_b)), A(G_{\text{RL}}^{L}(V_{\text{c}})) < G_{\text{th}} \), we interpret this as \( A(G_{\text{RL}}^{L}(V_b)), A(G_{\text{RL}}^{L}(V_{\text{c}})) \sim O(e^{-L/(\xi^2)} \cdot e^{-\Delta/n/T}) \). The extracted gap is obtained using the highest bias voltage \( V_b \) below which \( A(G_{\text{LR}}^{L}(V_b)) < G_{\text{th}} \) and \( A(G_{\text{LR}}^{L}(V_{\text{c}})) < G_{\text{th}} \). The choice of \( G_{\text{th}} \) should depend on \( \Delta/T \) and \( L/\xi(0) \) and also on the transparency of the junctions. For the disorder strengths expected in our devices, we take \( G_{\text{th}} \) equal to \( 0.05 \times \max(G_{\text{RL}}^{L}) \).

\(^8\) See also, Ref. 152 for additional considerations that are relevant to the non-local conductance.

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**Appendix D: Calibrating and testing the TGP with data from simulated devices**

In this section, we use simulations to quantify the reliability of the TGP. Our transport simulations begin with three-dimensional models of the devices in Figs. 2 and 3 that include the electrostatic environment defined by the set of gate voltages. We identify the \( V_{\text{c}} \) range for which the chemical potential is in the lowest sub-band and the cutter gate voltages for which the junction transparencies take the 5 values \( G_{\text{c}} = 0.35, 0.49, 0.62, 0.76, 0.9\frac{e^2}{2h} \). The resulting single sub-band parameters are given in Table 1 and Fig. 22. For this gate voltage set, we perform transport simulations and calculate the scattering matrix of the system. The local and non-local conductances \( G_{\text{LL}}, G_{\text{RR}}, G_{\text{LR}}, G_{\text{RL}} \) are then obtained by convolution with the derivative of the Fermi function at temperature \( T \). We analyze this data according to the TGP according to the same procedure that we will use in Sec. 4 to analyze experimental data.

**D.1. False discovery rate**

The basic question that we wish to answer is: suppose the TGP returns an ROI\(_2\) that passes; what is the probability that it does not have any overlap with the topological phase? The goal of TGP calibration is to set thresholds that minimize...
this probability. Once the TGP has been calibrated, we test it to assess whether this probability is low when the TGP is applied to a range of devices and parameters: different junction designs, different material parameters such as spin-orbit coupling, different disorder strength.

To compute this probability in simulations, we compare ROI28 with a topological index (the “scattering invariant” [103]). We classify ROI28 as follows: if an ROI2 has any overlap with a region of the simulated phase diagram with scattering invariant \(-1\), then we will call it a true positive; otherwise, it is a false positive. In Sec. 3 (see Eq. (4)), we defined the classification of regions as TP and FP, and derived the FDR from these numbers in order to quantitatively measure the reliability of the TGP.

Note that this is a classification of regions, rather than a classification of devices. Hence, if a device that does have a topological region were to pass the TGP but its ROI2 were completely disjoint from the topological region, then this ROI2 would be a false positive. We do not attempt to count negative regions: an arbitrary region is very likely to be negative, so the number of negative regions is not a useful statistic. Therefore, we do not compute the false positive rate (FPR), given by FP/(FP + TN), where TN is the number of true negatives. The FPR is less useful for the present discussion.

There is a further subtlety, which is that the scattering invariant depends on the junction transparencies. Since our device has two junctions, the scattering invariant can be defined at either one: \(\text{SI}_i = \text{sgn} \det r_i \in [-1, 1]\), where \(r_i\) is the reflection matrix and \(i = L, R\). When the junctions are completely closed, both SI are trivially equal to +1. When the junctions are opened, SI = −1 regions can appear, and they tend to grow as the junctions are opened further. Thus, we must decide how to assign a topological index to a finite system. We will define the topological region of the phase diagram as the union of the SI = −1 regions over \(i = L, R\) and the 5 different pairs of junction transparencies used in TGP Stage 2. We will call this union the “SI = −1 region.” Instead of taking the union of the SI = −1 regions, we could have taken the intersections. In our simulations, SI_L = −1 and SI_R = −1 regions overlap but not completely. For some cutter gate settings, only SI_R = −1 while for others SI_L = −1 because a zero-energy state can couple poorly to the lead at one junction or the other for different cutter gate settings. Our definition of the topological index is relatively insensitive to these details of the junctions. If we had wanted to use the Pfaffian invariant [9], we would have had to truncate the system to remove the junctions and then imposed periodic/anti-periodic boundary conditions. This would no longer be the same device as we would be probing in transport.

A final technical detail: the conductance matrix is temperature dependent, and the output of the TGP has a resulting temperature dependence. As we discuss in Sec. 4, the base temperature of our dilution refrigerators during these measurements is 20 mK, and the electron temperature is estimated to be \(\lesssim 40\) mK. We use transport data at 30 mK for our calibration simulations. We test the TGP using simulated data at 40 mK, and we used this simulated data in our estimates of the FDR and other statistical properties.

The main result of the subsections that follow is that we estimate that the FDR is \(\lesssim 8\%\) at a 95% confidence level for all device designs, material stacks, and disorder levels simulated. Thus, when a device passes the TGP, there is >92% probability that it has a non-zero gap and SI = −1. The details are in Table II.

### D.2. Setting the TGP thresholds

As discussed in Appendix C.2, there are three key thresholds which parametrize the TGP: \((ZBP\%)_{th}, (GB\%)_{th}, \text{ and } G_{th}\). We choose these parameters so that the TGP has a low FDR. If we were to make it very difficult to pass the TGP, then we would have very few false positives but also few true positives, and the FDR could be large. If we make it too easy to pass the TGP, then will have many more true positives but also more false positives. However, the right choices of \((ZBP\%)_{th}, (GB\%)_{th}, \text{ and } G_{th}\) lead to a TGP which is reliable because it has low FDR.

We performed an initial calibration of the TGP by analyzing simulated transport data at \(T = 30\) mK from 28 disorder realizations of an SLG-\(\beta\) device with an average charged defect density of \(n_{2D,int} = 2.4 \cdot 10^{12}/\text{cm}^2\) and spin-orbit interaction \(\alpha \approx 13\) meV·nm. We did not find any false positives: every ROI2 has at least some subset with SI = −1. However, the number of true positives and, hence, the FDR varies with the threshold values. We find that \((ZBP\%)_{th} = 60\%, (GB\%)_{th} = 60\%, \text{ and } G_{th} = 0.05 \max\{G_{NL}\}\) is close to optimal. There are 53 ROI28 spread across the 28 devices (all true positives) for these threshold settings. Hence, the FDR is \(\lesssim 6.7\%\) at the 95% confidence level. Had \((ZBP\%)_{th} \text{ and } (GB\%)_{th}\) been set lower, we would have found ROI28 that did not contain a region with SI = −1. For higher \((ZBP\%)_{th} \text{ and } (GB\%)_{th},\) we would have had fewer devices passing the TGP. If we had set \(G_{th}\) too low, then too much of the phase diagram would have been classified as gapless, thereby concealing gap re-openings. If we had set \(G_{th}\) too high, then too much of the phase diagram would have been classified as gapped, obscuring gap closings. Note that the two thresholds, \((GB\%)_{th}\) and \(G_{th}\) are correlated.

We show two realizations of simulated SLG, \(\beta\)-stack devices in Appendix D.5, one that passes the TGP and one that fails.

### D.3. Testing the TGP

With the TGP thus calibrated and validated, we turn to simulations estimating the FDR. Since we will be analyzing experimental data from devices with different designs, material stacks, and disorder levels, we apply the TGP to simulated SLG-\(\beta\) and DLG-\(\epsilon\) devices with several different charge disorder levels. For charge disorder given by \(n_{2D,int} \geq 10^{12}/\text{cm}^2\), we use the thresholds obtained in the calibration described above, whereas in the cleaner case of \(0.1 \cdot 10^{12}/\text{cm}^2\) we lower \(G_{th}\) from 0.05 to 0.01 while leaving the other thresholds unchanged. Although the optimal values of the thresholds in the TGP depend on the temperature, design, material stack, and disorder level, our goal here is to show that, for the thresholds chosen, the TGP remains reliable across a range of designs.
material stacks, and disorder levels, and at a slightly higher temperature. The motivation is that we would like to apply the TGP in cases in which neither the electron temperature nor the disorder level is known precisely. Note, however, that if either the disorder level or temperature were very different, then we would probably need to adjust \((ZBP\%)_{th}\), \((G B\%)_{th}\), and \(G_{th}\).

To estimate the FDR, we performed large-scale simulations involving 349 different disorder realizations, distributed across SLG-\(\beta\) and DLG-\(\varepsilon\) devices with intermediate to strong disorder levels defined by charge impurity densities of 0.1, 1, 2.7 and 4 in units of \(10^{12/cm^2}\), as shown in Table II. The Hall bar measurements described in Appendix B indicate that the devices experimentally measured in this paper have \(n_{2D,\text{int}}\) values in this range. The defect density \(n_{2D,\text{int}} = 2.7 \cdot 10^{12/cm^2}\) is the largest of any of the measured devices reported in this paper that has passed the TGP, while \(n_{2D,\text{int}} = 4 \cdot 10^{12/cm^2}\) is larger than in of any of the devices reported in this paper, including those that failed the TGP. Several of our measured devices have \(n_{2D,\text{int}}\) values at or below \(10^{12/cm^2}\).

We calculate the conductance matrix Eq. (2) for each simulated disorder realization at \(T = 40\, \text{mK}\) and analyze this data according to the TGP, as we would with experimental data. This analysis yields ROI\(_{2D}\); many disorder realizations, especially with stronger disorder, have none, while some disorder realizations, typically with weaker disorder, have multiple ROI\(_{2D}\). We compare these ROI\(_{2D}\) to the scattering invariant and classify each ROI\(_{2D}\) as a TP or FP depending on whether any subregion of the ROI\(_{2D}\) has \(SI = -1\). We find the statistics given in Table II. From the TP and FP values obtained from these simulations, we estimate the FDR by assuming a binomial distribution and use the Clopper-Pearson confidence interval at a 95% confidence level.

We do not have a single false positive in this data. This does not mean that the TGP perfectly identifies the topological region. Our results show that the TGP identifies an ROI\(_{2D}\) in some disorder realizations, especially with stronger disorder, have none, while some disorder realizations, typically with weaker disorder, have multiple ROI\(_{2D}\). We compare these ROI\(_{2D}\) to the scattering invariant and classify each ROI\(_{2D}\) as a TP or FP depending on whether any subregion of the ROI\(_{2D}\) has \(SI = -1\). We find the statistics given in Table II. From the TP and FP values obtained from these simulations, we estimate the FDR by assuming a binomial distribution and use the Clopper-Pearson confidence interval at a 95% confidence level.

Our analysis of the FDR indicates that TGP reliably identifies an SI = −1 region for different disorder levels and for different device designs. Indeed, as summarized in Table II, there are only small differences in the estimated FDR values for the above-mentioned parameters, and they are primarily due to the different numbers of ROI\(_{2D}\) for various disorder levels. Thus, the TGP at these threshold values can be applied to a large class of topological gap devices with intermediate disorder strength.

Our simulations also give us information about how the disorder level and device design affect the probability that a device will pass the TGP. We define the TGP yield as this probability:

\[ \text{TGP yield} \equiv P(\text{Device passes TGP}). \] (D1)

As may be seen from Table IV, the TGP yield depends strongly on \(n_{2D,\text{int}}\). More disordered devices are less likely to pass the TGP because they are less likely to have a topological phase.

We now consider the statistics of the SOI\(_{2D}\) that the TGP finds. Table IV shows these statistics when the magnetic field is restricted to \(B \leq 2.5\, \text{T}\), while \(B \leq 3\, \text{T}\) in Table V. We find that \(\Delta_{\text{SOI}}^{\text{max}}\) has mean value \(\Delta_{\text{SOI}}^{\text{max}}\) that varies between 25 and 35 \(\mu\text{eV}\) for different disorder strengths and has a non-Gaussian distribution with long tails towards larger gap. A smaller mean value is observed at the lowest disorder levels because there are significantly more SOI\(_{2D}\) at weak disorder, and many of them have small \(\Delta_{\text{SOI}}^{\text{topo}}\). The mean volume in the \(B-V_p\) parameter space of an SOI\(_{2D}\), denoted \(V_{\text{SOI}}\), is of the order 0.1 \(\text{mV}\cdot\text{T}\) and decreases with increasing disorder strength, see Table IV. As with \(\Delta_{\text{SOI}}^{\text{max}}\), the distribution of \(V_{\text{SOI}}\) is non-Gaussian with long tails. Finally, the average \(B\) field at which we observe SOI\(_{2D}\) ranges between 1.5T and 2.6T. As expected, \(\varepsilon\)-stack devices have SOI\(_{2D}\) that occur at higher magnetic fields > 2T since they have larger \(\Delta_{\text{ind}}\) and smaller \(g^*\).

### Table V.

| Design, stack | \(n_{2D,\text{int}}\) \([10^{12/cm^2}]\) | Yield \(\leq 3\, \text{T}\) | \(\Delta_{\text{SOI}}^{\text{max}}\) \([\mu\text{eV}]\) | \(V_{\text{SOI}}\) \([\text{mV}\cdot\text{T}]\) | \(B_{\text{SOI}}\) \([\text{T}]\) |
|---------------|---------------------------------|-----------------|-----------------|-----------------|-----------------|
| SLG-\(\beta\) | 1.0 | 48/50 | 23 | 0.2 | 2.1 |
|               | 2.7 | 24/50 | 34 | 0.1 | 1.5 |
|               | 4.0 | 26/49 | 36 | 0.1 | 1.5 |
| DLG-\(\varepsilon\) | 0.1 | 48/50 | 26 | 0.2 | 2.6 |
|               | 1.0 | 43/50 | 29 | 0.2 | 2.6 |
|               | 2.7 | 33/50 | 28 | 0.2 | 2.6 |
|               | 4.0 | 35/50 | 28 | 0.2 | 2.6 |

D.4. Example of the TGP applied to a single disorder realization

To illustrate the TGP, we now focus on a particular disorder realization in a narrow 3\(\mu\text{m}\) long device based on the DLG, \(\varepsilon\)-stack design. This is one of the devices that appears in Tables II and IV. We will call this simulated disorder realization DLG-\(\varepsilon\)-R1 for brevity. We have applied the TGP to \(T = 40\, \text{mK}\) transport data for this device, which we discuss in detail below, explaining the different stages of the TGP through this example. We also compare an SOI\(_{2D}\) identified by the TGP with the topological region determined by SI = −1. In Appendix D.5, we discuss simulated data from two other devices that we call realizations SLG-\(\beta\)-R1 and SLG-\(\beta\)-R2.

Stage 1: Stage 1 focuses on ZBPs in the local conductance. From the local conductances \(G_{\text{LR}}\) and \(G_{\text{LL}}\), we can map out the regions in \((B, V_p)\) space where there are stable ZBPs at the two junctions, where “stable” means that the ZBPs are present for a cutter gate fraction > 70%, as described in Appendix C.2. For simulated disorder realization DLG-\(\varepsilon\)-R1, the locations of stable ZBPs at the left junction are shown in
Fig. 25. The TGP applied to simulated transport data for DLG with \( n_{2D,int} = 10^{12}/\text{cm}^2 \) and 40 mK temperature broadening, highlighting regions of phase space with stable ZBPs in (a) \( G_{\text{LL}} \) and (b) \( G_{\text{RR}} \). (c) Regions of phase space with stable ZBPs in both \( G_{\text{LL}} \) and \( G_{\text{RR}} \). Simulated transport data such as this are used to test the TGP. Here, we show one particular disorder realization for illustrative purposes. Any possible visible resemblance to measured data is dependent on the disorder realization and does not play a role in our analysis.

Fig. 25(a) and at the right junction in Fig. 25(b). A topological phase should have stable ZBPs at both junctions at the same \( B \) and \( V_p \), so Fig. 25(c) shows the phase space locations where there are stable ZBPs at both junctions. This is the output of Stage 1 of the TGP. The entire gate voltage range shown here, \(-0.735 \text{ V} < V_p < -0.665 \text{ V}\), lies within the lowest sub-band. There is a trivial zero-energy state at the left junction over a region in the \( B-V_p \) plane that traces out a parabolic shape starting around \((B, V_p) = (1.2 \text{ T}, -0.69 \text{ V})\). However, this ZBP is unstable (i.e. fine-tuned) with respect to cutter changes and, therefore, is filtered out by the TGP. The ROI identified by the TGP is a smaller region at higher \( B \) and lower \( V_p \) where there are stable ZBPs at both junctions.

Stage 2: In Stage 2, we focus on the neighborhood of the ROI identified in Stage 1. Stage 2 analyzes local and non-local transport data over a range of bias voltages. In the simulated data, unlike in the experimental data discussed in Sec. 4, there is no drift of the plunger gate voltage \( V_p \), so the ROI is automatically recovered from local transport data. However, we do obtain the dependence of \( G_{\text{RR}} \) and \( G_{\text{LL}} \) on the bias voltage, as seen in Fig. 26(c,d). The more significant new ingredient in Stage 2 is the bias-dependence of the non-local conductances \( G_{\text{RL}} \) and \( G_{\text{LR}} \), from which we determine the transport gap as a function of \( B \) and \( V_p \). For simulated disorder realization DLG-\( \varepsilon \)-R1, the non-local conductances \( G_{\text{RL}} \), \( G_{\text{LR}} \) and the derived gap (indicated by black curves) as a function of \( B \) for \( V_p = -0.7205 \text{ V} \) are shown in Fig. 26(e,f). We give 5 significant digits after the decimal point for \( V_p \) so that these values can serve as indices in the relevant data files; this may be convenient for readers wishing to look directly at the data underlying the figures in this paper. Note that this cut passes through the topological phase transition and the topological phase; a gap closing and re-opening is seen in \( G_{\text{RL}} \) and \( G_{\text{LR}} \). Combining the local and non-local information, we can classify any point in phase space as gapped without stable ZBPs, gapped with stable ZBPs, gapless without stable ZBPs, or gapless with stable ZBPs. These are depicted in Fig. 26(a) as, respectively, blue, orange, white, or yellow. If an orange region is surrounded by white or yellow along more than 60% of its boundary, we identify it as an SOI\(_2\), and give it a black boundary in Fig. 26(a).

In addition to stable ZBPs, we also observe some zero-energy states that have a non-topological origin, as noted in our Stage 1 analysis. These trivial Andreev bound states (ABS) can be caused by resonances arising from the local electrostatic potential, local disorder, or a combination. We give some examples of their spectroscopy in Appendix D.5. While the presence of these ABSs can be limited by careful design of the junctions, they can never be fully suppressed. When running the TGP in experiments, we take care to tune away from pathological points in junction phase space as much as possible, while stepping between different junction configurations as we tune \( G_N \) to span from 0.1\( e^2/h \) to 1\( e^2/h \).

As we can see in Fig. 26(a,b), the TGP finds a region of topological phase [shown in orange in panel (a) and red in panel (b)] around \( B = 2.55 \text{ T}, V_p = -0.72 \text{ V} \) with a maximum topological gap \( \Delta_{\text{max}}^{\text{topo}} = 41 \mu\text{eV} \), which is the upper quintile of the gaps extracted in the SOI\(_2\).

The topological gap increases from zero at the phase transition to \( \Delta_{\text{max}}^{\text{topo}} \) in such a way that its median value over the red region within the black line in Fig. 26(b) is 26\( \mu\text{eV} \). The TGP phase diagram is compared with the scattering invariant. In Fig. 26(a), the region with SI = 1 is hatched. As may be seen in Fig. 26(a), the region identified by the TGP lies almost entirely within the region with negative topological index, i.e. the TGP is fairly conservative and identifies a subset of the topological phase. It is not a perfect match, of course, since the TGP is not directly calculating the scattering invariant and, moreover, the phase transition is rounded by finite temperature and finite-size corrections. Note the similarity between the hatched regions with negative topological index in Fig. 26(a) and the bright orange regions. The regions that pass the TGP are smaller pockets within these splinters.

Fig. 26(b) is another version of the phase diagram for this disorder realization: it shows the transport gap extracted from \( G_{\text{RL}} \) and \( G_{\text{LR}} \) multiplied by \( q = \pm 1 \), depending on whether that point lies outside or inside the SOI\(_2\). Note that \( q \) is not the same as the topological invariant \( Q \) that is used.
FIG. 26. (a) The simulated phase diagram for DLG, ε-stack with $n_{2D} = 10^{12}$ cm$^{-2}$ at $T = 40$ mK, combining the clusters of stable ZBPs at both junctions with the map of zero/non-zero gap. We identify gapped/gapless regions, with/without stable ZBPs, according to the color legend on the left. 67% of the boundary of the SOI is gapless. The hatched regions are where the topological invariant is negative. (b) The simulated phase diagram, showing trivial and topological phases, as identified by the TGP. $q = \pm 1$ in the trivial/topological phase, so the color scale shows the size of the trivial (blue) or topological (red) gap. The protocol assigns a maximum topological gap (defined as the top quintile of measured gaps within the SOI) of $\Delta_{\text{max}} = 41$ µeV. Simulated local and anti-symmetrized non-local conductances at $V_p = -0.7205$ V: (c) $G_{LL}$, (d) $G_{RR}$, (e) $A(G_{RL})$, (f) $A(G_{LR})$. The field range between the vertical lines is in the SOI. Panels (g)-(j) are “waterfall” plots representing the same simulated data. The black curves in panels (e) and (f) and the dots in panels (i) and (j) are not guides to the eye; they indicate where the non-local signal drops below a threshold value, as described in the text. The details of these plots are disorder-dependent, and any visible resemblance to measured data does not play a role in our analysis.
FIG. 27. The TGP applied to simulated transport data for a narrow 3 μm long wire with $n_{2D, \text{int}} = 2.4 \cdot 10^{12}/\text{cm}^2$, $\alpha \simeq 13\text{meV-nm}$ at $T = 30\text{mK}$, highlighting regions of phase space with stable ZBPs in (a) $G_{LL}$ and (b) $G_{RR}$. (c) Regions of phase space with stable ZBPs in both $G_{LL}$ and $G_{RR}$. Simulated transport data such as this are used to test the TGP. Here, we show one particular disorder realization for illustrative purposes. Any possible visible resemblance to measured data is dependent on the disorder realization and does not play a role in our analysis.

analogously in the color scale in Fig. 4 (where $Q$ is the Pfaffian invariant); rather, $q$ is the proxy for $Q$ that results from the TGP. The color scale of Fig. 26(b) can be viewed intuitively as the magnitude of the bulk gap multiplied by a proxy for the sign of the topological invariant. Darker red corresponds to larger topological gap.

As expected, there are some points along the boundary of the SOI where the closing is not visible in either $G_{RL}$ or $G_{LR}$. For this cutter gate pair in this particular disorder realization, 67% of the boundary of the SOI shows a gap closing in $G_{RL}$, $G_{LR}$, which is above (GB%)$_{th}$.

A comparison between the orange region in Fig. 26(a) and the hatched region lends credence to the idea that the part of the boundary that is gapped is not actually a boundary at all, and the true boundary is at higher $B$ and lower $V_p$. The blue region below and to the right of the orange region is hatched, indicating that it has been misclassified as non-topological. However, as may be seen in Fig. 26(b), this gapped (and ostensibly topological) region below and to the right of the SOI is light blue, indicating that it has a small gap. Hence, if it were topological, it would have a small topological gap and would not be useful for a topological qubit, in contrast to the darkest red regions within the SOI. The same observation applies to all of the hatched SI = −1 region that lies outside of the SOI: it may be topological, but it has a small transport gap. Moreover, since they do not have stable ZBPs in $G_{LL}$ and/or $G_{RR}$, it is unlikely that it would be possible to couple to these ZBPs in a qubit.

In this section, we discussed a disorder realization for a DLG-ε device that passed both Stages of the TGP and correctly found the topological phase. In Appendix D.5, we will show additional data from calibration simulations and discuss examples that fail the TGP.

D.5. Simulated disorder realizations used for the calibration of TGP

In this Appendix, we discuss two examples of simulated data that was used to calibrate the TGP. One example passes the TGP and one fails. The parameters of the simulation are equivalent to those of SLG-β devices with a larger spin-orbit coupling $\alpha \simeq 13\text{meV-nm}$.

The first realization, called SLG-β-R1, represents the 3 μm-long device with $n_{2D, \text{int}} = 2.4 \cdot 10^{12}/\text{cm}^2$. Here we assume $T = 30\text{mK}$, Stage 1 data is shown in Fig. 27. There are stable ZBP clusters in $G_{RR}$ and $G_{LL}$, as well as accidental ZBPs present for some cutter settings which correspond to disorder-induced subgap states at the junction. Due to the larger level of disorder in SLG-β-R1 than in DLG-ε-R1, there are more such accidental sub-gap states than in Fig. 25. The joint ZBP map is shown in Fig. 27(c).

The Stage 2 analysis of simulated device SLG-β-R1 is presented in Fig. 28. Simulated device SLG-β-R1 has an SOI around $(B, V_p) \approx (1.5\text{T}, -1.37275\text{V})$. 71% of the boundary of this SOI is gapless; the maximum and median topological gaps are 30μeV and 25μeV, respectively, for this cutter gate setting. Local and non-local conductances for $V_p = -1.37275\text{V}$ are shown in Fig. 28(c-f). There are stable ZBPs at both junctions over a range of $B$ fields of extent $\approx 1.3-1.7\text{T}$, and there is a clear gap closing and re-opening as a function of $B$. Also, note the similarity between the hatched regions with negative SI in Fig. 28(a) and the bright orange regions in the simulated Stage 1 data in Fig. 27.

For the sake of comparison, we also present trivial ZBPs seen at a different value of $V_p = -1.36575\text{V}$ in Fig. 28(g-j) [see upper dotted line in Fig. 28(b)]. However, the non-local conductance data in Fig. 28(i,j) clearly show that the system is gapless over the corresponding range of $B$ field values.

In Fig. 29, we present Stage 2 of TGP for another disorder realization, which we call SLG-β-R2. This is one of the realizations that passed Stage 1 but failed Stage 2. There are stable ZBPs at both junctions around $V_p = -1.36\text{V}$, as may be seen in Fig. 29(c,d). However, the non-local conductances...
in Fig. 29(e,f) yield zero gap. In fact, the system is gapless over most of the scanned region, so this simulated transport data does not pass Stage 2 of the TGP. This example once again reinforces the fact that local measurements alone cannot reliably detect a topological phase.

Appendix E: Three-terminal conductance measurements with several hundred Hz excitations

The conductance matrix is measured with a standard lock-in technique, applying simultaneous voltage excitations with amplitudes $dV_L^R(f_L)$ and $dV_R^L(f_R)$ to the inputs of the left and right terminals, respectively. They are at frequencies $f_L$ and $f_R$, respectively, and currents $dI_L^R(f_L)$ and $dI_R^L(f_R)$ are measured at the left terminal while $dI_R^L(f_L)$ and $dI_L^R(f_R)$...
are measured at the right terminal. However, due to the finite impedance network between the signal input and the measured sample, the voltages applied and the currents measured deviate from those at the sample inputs. At lock-in frequencies of several hundred Hz, the capacitances of the cryostat lines and filters (on the order of several nF) combined with the line and filter resistances have a non-negligible contribution to the measured currents. Furthermore, a finite resistance at the drain contact imposes an effective voltage modulation of the opposing contact as a voltage divider effect. As a result, the sample experiences voltage modulations \( dv_L(f_L) \) and \( dv_R(f_R) \) at the left and \( dV_R(f_L) \) and \( dV_R(f_R) \) at the right input. The currents at the left terminal are \( dI_L(f_L) \) and \( dI_L(f_R) \) while the currents at the right terminal are \( dI_R(f_L) \) and \( dI_R(f_R) \). Noting that \( dI_T(f) = G_{IJ} dV_J(f) \) where \( I, J = L, R \), the conductances are obtained from

\[
\begin{pmatrix}
G_{LL} & G_{LR} \\
G_{RL} & G_{RR}
\end{pmatrix}
= 
\begin{pmatrix}
dI_L(f_L) & dI_L(f_R) \\
dI_R(f_L) & dI_R(f_R)
\end{pmatrix}
\begin{pmatrix}
dV_L(f_L) & dV_L(f_R) \\
dV_R(f_L) & dV_R(f_R)
\end{pmatrix}^{-1}
\tag{E1}
\]

Note that we recover Eq. (2) if we take \( dV_L(f_L) = dV_R(f_L) = 0 \). To proceed, we need a map

\[
M = 
\begin{pmatrix}
M_{VV} & M_{V1} \\
M_{IV} & M_{II}
\end{pmatrix}
\tag{E2}
\]

between the voltages and currents at the sample, \( \mathbf{V} = (dV_L(f), dV_R(f))^T \) and \( \mathbf{I} = (dI_L(f), dI_R(f))^T \), and the voltages applied and the currents measured, \( \mathbf{V}_0 = (dV_{L,0}(f), dV_{R,0}(f))^T \) and \( \mathbf{I}_0 = (dI_{L,0}(f), dI_{R,0}(f))^T \):

\[
\begin{pmatrix}
\mathbf{V} \\
\mathbf{I}
\end{pmatrix}
= 
\begin{pmatrix}
M_{VV} & M_{V1} \\
M_{IV} & M_{II}
\end{pmatrix}
\begin{pmatrix}
\mathbf{V}_0 \\
\mathbf{I}_0
\end{pmatrix}
\tag{E3}
\]

The impedance network between the input ports and the measured sample consists of a sequence of stages, each of which has the general form illustrated in Fig. 30(a): every line has a capacitance to ground and to every other line in parallel and a resistance in series to the next stage. The drain of the measured device is also connected to ground at the input and is thus included in the circuit here and will be reduced from the final mapping later. By denoting the termi-
nals as \( k = \{L, R, D\} \) and \( l = \{L, R, D, G\} \) (where \( G \) denotes ground), the output voltages \( dV_k \) and currents \( dI_k \) are determined by the input voltages \( dV'_k \) and currents \( dI'_k \), as well as cross-currents \( dI_{kl} \) as

\[
dI_k = dI'_k - \sum_{l \neq k} dI_{lk} = dI'_k - \sum_{l \neq k} Y_{kl} (dV'_l - dV'_l) = - \left( \sum_{l \neq k} Y_{kl} \right) dV'_k + \sum_{l \neq k} Y_{kl} dI'_l + dI'_k, \quad \text{(E4)}
\]

This has the general form

\[
\begin{pmatrix} V \\ I \end{pmatrix} = \begin{pmatrix} M_{IV} & M_{II} \\ M_{IV} & M_{II} \end{pmatrix} \begin{pmatrix} V' \\ I' \end{pmatrix} = M \begin{pmatrix} V' \\ I' \end{pmatrix}. \quad \text{(E7)}
\]

With multiple stages in a sequence, the mapping from the input to the measured device

\[
\begin{pmatrix} V \\ I \end{pmatrix} = M^\text{tot} \begin{pmatrix} V^0 \\ I^0 \end{pmatrix}. \quad \text{(E8)}
\]

is given by matrix multiplication \( M^\text{tot} = \prod_k M^k \) where the matrices \( M^k \) are given by Eq. (E4). The \( 6 \times 6 \) map \( M^\text{tot} \) is further reduced to a more useful \( 4 \times 4 \) form by the following steps:

1. Imposing current conservation \( (dI_D = -dI_L - dI_R) \) at the sample, which then reduces the map to a \( 5 \times 5 \) matrix with \( k \in \{V_L, dV_R, dV_D, dI_L, dI_R\} \) and \( l \in \{dV'_L, dV'_R, dV'_D, dI'_L, dI'_R\} \) which now takes the form

\[
M_{kl}^\text{red} = M_{kl}^\text{tot} - (M_{dL}^\text{tot} dI'_D + M_{dR}^\text{tot} dI'_D + M_{dD}^\text{tot} dI'_D)^{-1} \left(M_{dL}^\text{tot} dI_L + M_{dR}^\text{tot} dI_R + M_{dD}^\text{tot} dI_D\right) M_{kd} dI'_D. \quad \text{(E9)}
\]

2. Defining \( dV_L \) and \( dV_R \) as potentials with respect to \( dV_D \) at the sample, as well as \( dV'_D = 0 \), which leads to the final \( 4 \times 4 \) matrix \( M \) with \( k \in \{dV_L, dV_R, dI_L, dI_R\} \) and \( l \in \{dV'_L, dV'_R, dI'_L, dI'_R\} \) that takes the form

\[
M_{V(L,R)} = M_{v(L,R)} - M_{VD},
M_{I(L,R)} = M_{I(L,R)}^\text{red} \quad \text{and} \quad M_{V(L,R)}^\text{red} = M_{V(L,R)} - M_{VDt}. \quad \text{(E10)}
\]

The effect on input voltages and measured currents of additional filtration from the measurement instruments should also be incorporated.

\[
dV_k = dV'_k - Z_k dI_k = \left(1 + Z_k \sum_{l \neq k} Y_{kl}\right) dV'_k - Z_k \sum_{l \neq k} Y_{kl} dI'_l - Z_k dI'_k, \quad \text{(E5)}
\]

where \( Z_k \) are the impedances (resistances for sufficiently low frequencies) of the lines, \( Y_{kl} = 2\pi i f C_{kl} \) are the parallel admittances via capacitors \( C_{kl} \) between \( k \) and \( l \), and \( V_G = 0 \). Equations (E4) and (E5) can be expressed in matrix form as

\[
\begin{pmatrix} V'_L \\ V'_R \\ V'_D \\ I'_L \\ I'_R \\ I'_D \end{pmatrix} = \begin{pmatrix} 1 + Z_L \sum_{D,L,G} Y_{Lk} & -Z_L Y_{LR} & -Z_L Y_{LD} & -Z_L Y_{LD} & -Z_L Y_{LD} & -Z_L Y_{LD} \\ -Z_R Y_{LR} & 1 + Z_R \sum_{D,L,G} Y_{Rk} & -Z_R Y_{RD} & -Z_R Y_{RD} & -Z_R Y_{RD} & -Z_R Y_{RD} \\ -Z_D Y_{LD} & -Z_D Y_{RD} & 1 + Z_D \sum_{L,R,G} Y_{Dk} & -Z_D Y_{RD} & -Z_D Y_{RD} & -Z_D Y_{RD} \\ -Y_{LR} & -Y_{RD} & -Y_{RD} & 1 & 0 & 0 \\ -\sum_{k=L,R,G} Y_{Dk} & -\sum_{k=L,R,G} Y_{Dk} & -\sum_{k=L,R,G} Y_{Dk} & -\sum_{k=L,R,G} Y_{Dk} & 1 & 0 \end{pmatrix} \begin{pmatrix} V'_L \\ V'_R \\ V'_D \\ I'_L \\ I'_R \\ I'_D \end{pmatrix}. \quad \text{(E6)}
\]

For our setup, the mapping \( M \) is comprised of four stages \( M^4 \) where the resistances are determined by the installed filters and, for the final stage, are the sample lead resistances which are extracted independently from the linear I-V response in DC measurements. To calibrate the capacitances in the setup, we measure \( dI'_D \) and \( dI'_R \) as a function of the excitation frequency \( f_L \) of a voltage modulation first applied to the left port, then as a function of frequency \( f_R \) of the modulation applied to the right port when the device is fully pinched off (i.e., the zero conductance limit). We then use capacitances between the lines and the ground as fit parameters relating the measured \( dI'_D \) to \( f_L \) and \( dI'_R \) to \( f_L \). Finally, the mutual capacitance between \( L \) and \( R \) is obtained as a fit parameter relating the measured \( dI'_D \) and \( dI'_R \) to \( f_L \) and \( f_L \), respectively. In the experiments described in the main text, the extracted capacitances of the fridges lines and filters, together with known cut-off frequencies of the voltage sources and current preamplifier outputs, are then used to calculate the sample conductances based on the measured \( dI'_D \) and \( dI'_R \). Full details on this calibration routine, including all extracted parameters that were used to process measured data, can be found in the accompanying data repository [96].

Note that a further effect of finite resistances on the stages of the measurement circuit is to rescale the applied DC bias voltages. As described in [150], the DC voltages at the sample \( V = (V_L, V_R)^T \) are related to the applied DC voltages \( V^0 = (V'_L, V'_R)^T \) and DC currents \( I^0 = (I'_L, I'_R)^T \) through the relationship:

\[
V = V^0 - R I^0. \quad \text{(E11)}
\]

where \( R \) is a matrix containing the total resistances on the left, right, and drain lines:

\[
R = \begin{pmatrix} R_L + R_D & R_D \\ R_D & R_R + R_D \end{pmatrix}. \quad \text{(E12)}
\]

For all the experimental datasets presented in this manuscript, the average magnitude of these corrections is 1%-6% of the applied bias voltages. For this reason, we do not apply these corrections and present the data as a function of the applied bias voltages, and not of the bias voltages at the sample.
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