Impact of high mobility III-V compound material of a short channel thin-film SiGe double gate junctionless MOSFET as a source

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Abstract
In recent years, technology has embraced the use of Junctionless Double Gate Metal-Oxide-Semiconductor Field-Effect Transistors (JL DGMOSFET) to reduce Short Channel Effects (SCEs). This research presents a novel JL DGMOSFET based on a highly doped N-type SiGe in which an III-V compound material is used at source regime. The III-V compound material GaSb with higher mobility and higher injection velocity is used as source material, whereas SiGe is considered for both channel and drain materials to produce a higher output current and low leakage current for the N channel JL DGMOSFET. In addition, high-k dielectric material HfO₂ is employed to improve the controllability of the gate at 20 nm channel length. Different parameters, such as \( I_d, SS, g_m, \text{ TGF, } I_{on}/I_{off} \) ratio, \( C_{gs} \), and \( f_T \) of a Symmetric JL DGMOSFET are studied and compared to existing works. The comparison shows that the proposed JL DGMOSFET outperforms the existing state of knowledge. The analysis is also being extended by including the trap charge for the symmetric JL DGMOSFET. Parametrically, the asymmetrical structure is finally studied. The proposed structure yields a higher \( I_d \) of 40 mA, \( SS \) of 60.25 mV/decade, \( g_m \) of 0.148 A/V, \( \text{TGF of 3.69 V}^{-1} \), \( I_{on}/I_{off} \) ratio of \( 3.41 \times 10^{13} \), \( C_{gs} \) of \( 3.78 \times 10^{-16} \) F and \( f_T \) of \( 1.19 \times 10^{13} \) Hz, hence indicating an improved RF and DC analysis.

KEYWORDS
asymmetric, cut-off frequency (\( f_T \)), donor traps, acceptor traps, gate drain capacitance (\( C_{gd} \)), gate source capacitance (\( C_{gs} \)), high-k dielectric, \( I_{on}/I_{off} \) ratio, junctionless double gate (JL DG) MOSFET, subthreshold swing, symmetric, transconductance (\( g_m \)), transconductance generation factor (TGF)

1 INTRODUCTION

In the modern era of digital and telecommunications technology, semiconductor devices play a pivotal role in integrated circuits, mobile devices, IOTs, defense application systems, wireless communication systems, and so on.¹ The sizing of a device becomes more difficult in terms of area, power, cost, and speed for a complex system. To overcome these challenges, device scaling is considered. The device (MOSFET) tends to generate more heat and consumes more power by
continuously shrinking dimensions, which indirectly enhances the functionality of the integrated circuit (IC) on a given silicon wafer. To minimize the effects of heat and power consumption, the supply voltage takes the back seat and reduced according to the scaling of the device. MOSFET’s scaling factor, however, boosts short channel effects (SCEs) and, unfortunately, decreases device performance as well as increases off-state leakage current, resulting in abnormal power consumption and less gate control over the channel. Loss of gate controllability over the channel causes large leakage current flow due to source-drain coupling, subthreshold conduction, drain induced barrier lowering (DIBL) and threshold voltage roll-off. Reducing the device dimension again helps to achieve higher packing density with lower power dissipation and enhanced circuit functionality, but causes severe SCEs. To reduce the SCEs and fit these devices for circuit applications, gate control is, therefore, the subject of research. The Multiple Gate FET (MUGFET) definition is, therefore, developed with proven superiority over the single gate devices. Some new architectures are being developed under the MUGFET, such as double gate (DG) MOSFET, gate all around (GAA) MOSFET, and quadruple gate (QG) MOSFET. In some modified structures such as dual material double gate (DMDG) MOSFET, triple material double gate (TMDG) MOSFET, etc., this purpose can also be observed. In the case of MUGFETs, there are several steep junctions such as p-n, n + − n, p + − p, p + − n, p + − n+, etc. and thermal energy increases due to these idealized junctions with an increase in temperature, thereby influencing the thermal budget. By definition, a thermal budget can be defined as the total amount of thermal energy transferred to the wafer when the temperature rises from a certain limit. This causes difficulties during the development of ultra-sharp source and drain junctions in the lithography process. This makes the thermal budget a challenging factor in the manufacture of devices. Junctionless double gate MOSFET (JL DGMOSFET) is a promising tool as a replacement for normal MOSFET to resolve the above parameters such as thermal budget, steep junction, doping concentration gradient, diffusion rules, mobility degradation, heat dissipation, leakage current, and ultra-scale minimization. Due to the absence of p−n junctions in the device manufacturing process, traps, and interface defects are reduced. Compared to conventional MOSFET, non-existence of p-n junction at source and drain in the proposed device offers less manufacturing complexity, cost, and thermal budget. The doping concentration of JL DGMOSFET is uniform throughout the device. This uniform doping helps the JL DGMOSFETs to eradicate the formation of source/channel and channel/drain junctions. The absence of gradient doping concentration offers high gn, drain current, minimal leakage current and ideal subthreshold slope. Many researchers have reviewed various models of JL DGMOSFET, suggesting that JL DGMOSFET turns-ON in the flat-band condition known as threshold voltage and turns-OFF in the sub-threshold region that occurs due to the complete depletion of the channel region within sub-nanometer technology. Channel region becomes fully depleted due to high doping dependency strong vertical electric field below VTH and the electric field becomes zero above the threshold condition. In terms of SCEs, the device plays supremacy over junction-based FETs. Because distance among the non-depleted source and drain regions become larger than the physical gate length of a JL DGMOSFET at a gate voltage less than VTH due to the electrostatic squeezing effect. This is a useful factor for reducing SCEs. Materials with high doping are generally used for JL DGMOSFET to improve conductivity. Increased on-current and reduced off-current will be accomplished at a lower supply voltage below the oxide thickness of less than or equal to 1.5 nm due to the use of heterostructure at source-channel junction and enhanced channel gate control. Decreasing the thickness of the oxide makes the parasitic capacitance and resistance value almost equal to or greater than the intrinsic capacitance and resistance. Thus the gate leakage current arises, which leads to the direct tunneling of free carriers and consequently to the undesirable dissipation of power. Materials with more permittivity than SiO2 are used to overcome these problems and these components are referred to as high dielectric or high-k materials. Some high-k materials like Ta2O5, TiO2, ZrO2, HfO2, and La2O3 are commonly used in MOSFETs to reduce gate leakage current. JL DGMOSFET is affected by speed and efficiency degradation due to the increase of SCEs with a scaling down to 15 nm or below channel length. But in an N-type JL DGMOSFET, the distance of the non-depleted source and drain regions becomes more than the physical gate length across the entire section of the device due to increment of negative gate voltage yielding parasitic series resistance and reduces SCEs. Some high electron mobility and lower bandgap compound materials in group III-V of the periodic table are used in JL DGMOSFETs to further overcome these shortcomings. Because of their low bandgap, light effective mass, high electron mobility, and high injection speed, these materials are used for logical application, resulting in high current even at low supply voltage. Thus in JL DGMOSFET, the formation of the narrow and thin semiconductor layer can be achieved by using a thin layer of dielectric material allowing the depletion carriers in the OFF state, which is advantageous for fabrication. Furthermore, the reduction of the body thickness of JL DGMOSFET enhances the volume depletion in nanowire architecture. Enhancing positive bias at both front and back gates provides a reduction of the depletion layer from the middle of the channel and uncovers an undepleted region at the center of the film thickness. A SiGe-based short channel N-type JL DGMOSFET with Gallium Antimonide (GaSb) as source is proposed using Gold, Hafnium Dioxide (HfO2), and Silicon Germanium...
TABLE 1 Comparative study between the proposed model and the earlier model

| Parameters          | Proposed structure | Earlier model | 1 |
|---------------------|--------------------|---------------|---|
| $I_d$(mA)           | 40                 | 0.7           |   |
| SS(mV/decade)       | 60.25              | 62.83         |   |
| $g_m$(A/V)          | $1.48 \times 10^{-3}$ | $2.91 \times 10^{-3}$ |   |
| TGF(V$^{-1}$)       | 3.69               | 40.03         |   |
| $I_{on}/I_{off}$    | $3.41 \times 10^{13}$ | $3.82 \times 10^{11}$ |   |
| $C_{gs}$(F)         | $3.78 \times 10^{-16}$ | $4.83 \times 10^{-16}$ |   |
| $C_{gd}$(F)         | $5.06 \times 10^{-17}$ | $3.46 \times 10^{-17}$ |   |
| $f_T$(Hz)           | $1.19 \times 10^{13}$ | $9.04 \times 10^{11}$ |   |

(SiGe) as front and back gates, front and back oxides, channel and drain materials respectively. This structure shows higher on current, lower off current$^{27-29}$ and lower SS than a normal Silicon-based JL DGMOSFET.$^1$ As SS is lower and suitable for switching, the system can be useful for logic applications. It also offers an improved $I_{on}/I_{off}$ ratio that again means a reduction in leakage current and is useful for low power logic development. Due to the presence of high-k dielectric material HfO$_2$ at both front and back gates, on-current increases and effect of fringing capacitance decreases. In this work, the simulation results show that response of GaSb-SiGe JL DGMOSFET is better than the earlier structure made of Si at 20 nm channel length.$^1$ The simulation work is calibrated and validated in comparison with the earlier model to obtain accurate results in Sentaurus T-CAD tool.$^1$ Table 1 shows a comparative analysis of $I_d$, SS, $g_m$, TGF, $I_{on}/I_{off}$, $C_{gs}$, $C_{gd}$, and $f_T$ between the structure proposed and the earlier model.$^1$ A fundamental research has also been conducted on interface traps such as donor and acceptor traps.

2 | DEVICE STRUCTURE AND OPERATION

Figure 1 demonstrates the schematic model of an n-type Symmetric JL DGMOSFET. The aforementioned structure is a 2D heavily doped n-channel JL DGMOSFET with a uniform Doping concentration $N_D$ of $1 \times 10^{19}$ cm$^{-3}$ in source, channel and drain regions. The different dimensions of the device are stipulated in Table 2. In Figure 1, high mobility and lower bandgap compound material, GaSb is used as a source whereas, high bandgap material SiGe is used both for channel and drain regions develops a heterostructure at the source-channel interface. HfO$_2$ is used as front and back oxide layers along with Gold as front and back gate metals. The schematic diagram of the JL DGMOSFET carried out in this work is shown in Figure 1 which is consisted of a channel length ($L_{ch}$) of 20 nm, source and drain extensions of 5 nm from the tip of the channel, body thickness ($T_{body}$) of 5 nm and gate oxide thickness ($T_{ox}$) of 1 nm with horizontally positioned metal contacts. The simulation is also extended at the front gate voltage of 1.2 V for the asymmetric JL DGMOSFET with 0.5 nm back gate oxide thickness ($T_{oxb}$).

An energy band diagram of symmetric JL DGMOSFET for the proposed structure is shown in Figure 4. The energy diagram is plotted at the center of the channel because JL DGMOSFET thin-film is completely dominant by off-state volume depletion method and the current conduction starts at the center of the channel with the increase of gate voltage. In Figure 4, valance and conduction bands are represented in off and on states by the blue and red lines. The bandgap of GaSb is less as compared to SiGe develops a band offset at source-channel interface. At a constant drain voltage of $V_d$ equal to 1 V, a positive gate voltage of 1.2 V greater than the threshold voltage is applied and a neutral region is created at

![Figure 1](image-url)  
Schematic diagram of an n-type SiGe-based JL DGMOSFET with GaSb as the source
| Parameter                        | Value     |
|---------------------------------|-----------|
| Gate work-function              | 4.8 eV    |
| Front gate oxide thickness ($T_{oxf}$) | 1 nm      |
| Back gate oxide thickness ($T_{oxb}$) | 1 nm      |
| Body thickness ($T_{body}$)      | 5 nm      |
| Channel length ($L_{ch}$)        | 20 nm     |
| Doping concentration ($N_D$)     | $1 \times 10^{19}$ cm$^{-3}$ |
| Drain voltage ($V_d$)            | 1 V       |
| Front gate voltage ($V_{gf}$)    | 1.2 V     |
| Back gate voltage ($V_{gb}$)     | 1.2 V     |

Table 2: Device specification of symmetric JL DGMOSFET

the center of the n-type channel. The source electrons find a low-resistive conduction path through the channel’s heavily doped neutral region and stream into the drain to serve as a closed switch. But in the off state, an applied gate voltage is lower than the flatband voltage that modulates the channel’s barrier height, thus providing a high-resistive path between source and drain as shown in Figure 4. It is therefore very difficult to move the electrons from source to drain through the channel, and JL DGMOSFET acts like an open switch.

3 | RESULT ANALYSIS

A comparative study is conducted between the three structures given in Figures 1-3 to distinguish drain current at low gate voltage. In addition Figures 5 and 6 show that drain current is higher for GaSb-SiGe than for SiGe and Si structures. As a result of this simulation, the drain current in GaSb-SiGe is 40 mA, in SiGe 7.6 mA and in Si 7.2 mA. Because of the high electron mobility and high injection velocity of the lower bandgap III-V GaSb compound material, high drain current flows throughout the GaSb-SiGe structure.

Various back gate voltages ($V_{gb}$) for asymmetric JL DGMOSFET are monitored and the result determined. The voltages of the back gate ($V_{gb}$) are tuned between −0.9 V to 0.9 V with a difference of 0.2 V with the voltage of the front gate ($V_{gf}$) maintained at 1.2 V. For the proposed device, Sentaurus T-CAD is used as a 2D simulation tool. To compare different drain current values, channel lengths are coordinated with a difference of 5 nm between 20 and 50 nm. The gate metal’s work-function remains through the manuscript at 4.8 eV. In this simulation different models like Inversion and Accumulation Layer Mobility Model (IALMob), Actual Mobility Model (High Field Saturation), Shockley-Read-Hall generation

![Figure 2](image.png)  
**Figure 2** Schematic diagram of an n-type SiGe-based JL DGMOSFET

![Figure 3](image.png)  
**Figure 3** Schematic diagram of an n-type Si-based JL DGMOSFET
**FIGURE 4**  Energy band diagram of symmetric junctionless transistor

**FIGURE 5**  Variation of $I_d$ as a function of $V_{gf}$ with different compound material for symmetric DG MOSFET

**FIGURE 6**  Variation of $I_d$ as a function of $V_d$ with different compound material for symmetric DG MOSFET
and recombination model. Doping Dependence Mobility model and BandGap Narrowing model are used to include the effect of scattering and screening effect of ionized impurities, electron mobility at room temperature, leakage current, carrier mobility degradation, and doping concentration. A JL DGMOSFET is a gated resistor where the gate modulates the mobile carrier density without PN, N + N or P + P junctions. It is a uniformly doped device for n-channel and p-channel MOSFETs with N+ and P+ semiconductor material nanowire films. Semiconductor material nanowires are used to make JL DGMOSFET with the same functionality as MOSFET and these are the devices where the carrier flow can be controlled by the gates and the control capability depends on the film thickness rather than the length of the gate and the thickness of the oxide. The flow of current is high during saturation mode because of high doping concentration and current at the surface by the accumulation layer. During the off state, the current flow is sealed for the depletion condition due to the metal and semiconductor work function difference of the proposed structure. Current increases as the concentration of doping increases. But it will be difficult to make the device off for high concentration of doping, henceforth the device’s cross-sectional area will be reduced to a minimum value. It is also known as capacitance operated device due to the dependence of the drain current on gate capacitance \( C = \varepsilon_0 KA/\tau_{ox} \), where \( \varepsilon_0 \) is the free space permittivity, \( K \) is the dielectric constant of gate oxide material, \( A \) is the cross-sectional area and \( \tau_{ox} \) is the oxide thickness. A JL DGMOSFET is a heavily doped donor and acceptor doping accumulation mode device for n-channel and p-channel transistors. It works same as a MOSFET with ease of fabrication but increases the current flow along the center of the channel due to high electron mobility.

With a higher gate potential the charge carriers gain excess kinetic energy and collide with each other results extra electrons and holes, this process is known as impact ionization. JL DGMOSFETs have revealed a steep SS of less than 60 mV/decade at room temperature due to high impact ionization. Some of the important performance parameters that can be achieved by a JL DGMOSFET are low leakage current, high ON current, low SS, higher \( I_{on}/I_{off} \) ratio and variability. Figure 7 displays the \( I_d\text{-}V_g \) characteristics of a symmetric n-type JL DGMOSFET in both standard and log scale. The device’s back gate voltage is tuned between −0.9 V and 0.9 V and the drain current increases and decreases as front gate voltages increase and decrease with constant drain bias and regulated back gate voltage. As we have already observed in Figure 4 that with the increase in gate voltages at a constant drain bias the barrier height decreases, the current begins to flow at the threshold voltage and rises for the positive gate biases. Reverse scenario happens for the gate voltages less than the threshold or flat band voltage which is visible in Figure 7 at a constant back gate and drain biases. Threshold voltage, as well as barrier height, also modulate with the change of back gate voltages from −0.9 V to 0.9 V with the difference of 0.2 V and device turn-ON at low front gate bias. In Figure 8A,B, \( I_d\text{-}V_g \) characteristics of the n-type symmetric and asymmetric JL DGMOSFET are shown with the variation of channel length.

Impact ionization plays a significant role in increasing the current in JL DGMOSFET. Due to the shrinking of channel length, the magnitude of the lateral electric field becomes extremely high and it enhances momentum as well as the kinetic energy of the channel electrons. These high energetic electrons collide with the atoms and exchange their momentum in order to generate electron-hole pairs. These generated electrons again gain sufficient energy from the lateral electric field to generate more electron-hole pairs. Thus current and device performance is improved in short channel JL DGMOSFET due to impact ionization.
**Figure 8** (A) Variation of $I_d$ as a function of $V_{gf}$ with a variation of channel length for symmetric DG MOSFET. (B) Variation of $I_d$ as a function of $V_{gf}$ with a variation of channel length for asymmetric DG MOSFET.

**Figure 9** (A) Variation of $I_d$ as a function of $V_d$ with different channel lengths for symmetric DG MOSFET. (B) Variation of $I_d$ as a function of $V_d$ with different channel lengths for asymmetric DG MOSFET.

Figure 9A,B show symmetric and asymmetric characteristics of $I_d$-$V_d$ with different channel length variations from 20 to 50 nm. As the lateral electric field is inversely proportional to the channel length, drain current increases for the diminishing of channel length from 50 to 20 nm both for symmetric and asymmetric structures. Drain current of symmetric JL DGMOSFET is comparatively more than the asymmetric one with $V_{gf}$ and $V_{gb}$ corresponding to about 1.2 and 0.5 V at 0.5 nm back oxide thickness.

The impact of oxide thickness variation for the symmetric and asymmetric structures is also analyzed in Figures 10A,B and 11A,B. For gate and drain voltage variations, it is observed in both structures that the magnitude of the current is inversely proportional to the oxide thickness variation and it reduces for lowering the oxide thickness from 2 to 0.5 nm which corresponds to gate tunneling through thin oxide thickness. In Figure 10A,B, variation of drain current with respect to front gate voltage at a constant back gate and drain voltages equal to 0.5 and 1 V are plotted considering high-$k$ dielectric material HfO$_2$ at front and back oxides instead of SiO$_2$. Oxide thickness less than 1.5 nm degrades the device performance due to gate tunneling through the thin oxide thickness.
By using high-k dielectric material, the effective oxide thickness of JL DGMOSFET is improved by the factor of $k_{HfO_2}/k_{SiO_2}$ to minimize gate tunneling. The drain current variation with respect to drain voltage is also analyzed in Figure 11A and lowering of drain current is also observed for the reduction of both front and back oxide thicknesses in case of symmetric Structure.

In Figure 11B, the change in the back oxide thickness is also performed, keeping the magnitude of the front oxide thickness constant. In Figure 12A,B, subthreshold swing with respect to gate voltages for symmetric and asymmetric structures are examined and minimum subthreshold swing, $SS_{min}$ is calculated.

For the symmetric JL DGMOSFET, $SS_{min}$ rises from 59.68 mV/dec to 60.25 mV/dec at 1.2 V due to SCE, reducing the channel length from 50 to 20 nm. This effect can also be observed for the asymmetric structure, and with the reduction of channel length, $SS_{min}$ also increases. However, a lower value of SS gives better control to the on-off currents, which are essential for switching applications. It is examined that the proposed structure has a better SS of 60.25 mV/dec than the earlier structure. Figure 13A,B depicts the $g_m$ and TGF with the variation of front gate voltage at constant drain bias for both symmetric and asymmetric structures. TGF can be defined as the transconductance achieved per unit ampere.
of output current and it is formulated as $\text{TGF} = g_m/I_d$. The parameter is considered as a figure of merit which signifies efficiency to translate current into $g_m$. Enhancement of $g_m$ and lowering of TGF are observed at a constant front gate bias for the shortening of channel length from 50 to 20 nm.

Less value of TGF is generally appreciable for microwave application and not unfavorable due to less power consumption in the subthreshold region. Variation of $I_{on}/I_{off}$ and SS with respect to $V_{TH}$ for Symmetric and Asymmetric JLDGMOSFETs are shown in Figure 14A,B. Here, the graphical result clearly shows that the ratio of on-current to off-current is quite high due to implementation of high mobility and high injection velocity III-V compound material at the source side. SS variation is also analyzed and it enhances with the SCEs. However, an improvement of SS compared to earlier model is observed in the proposed device structure.

Table 3 indicates the effect of channel length on digital and analog performance parameters and observed from the table that the performance of JLDGMOSFET degrades with the increase in channel length. Variations of gate to source capacitance, $C_{gs}$ and gate to drain capacitance, $C_{gd}$ with different gate voltages are plotted in Figure 15. Both the parasitic capacitances increase predominantly due to the decrement of depletion region lengths at source and drain sides. It is observed that the values of both $C_{gs}$ and $C_{gd}$ decrease with the reduction of channel length as both the fringing
TABLE 3 Performance parameters for different channel lengths of JL DGMOSFET MOSFET

| Parameters | 20 nm | 25 nm | 30 nm | 35 nm | 40 nm | 45 nm | 50 nm |
|------------|-------|-------|-------|-------|-------|-------|-------|
| $V_t$ (V)  | 0.92  | 0.93  | 0.94  | 0.95  | 0.96  | 0.964 | 0.968 |
| $I_d$ (mA) | 40    | 36    | 33    | 32    | 29    | 28    | 26    |
| SS(mV/decade) | 60.25 | 60    | 59.89 | 59.82 | 59.78 | 59.75 | 59.73 |
| $g_m$(A/V) | 0.148 | 0.139 | 0.131 | 0.128 | 0.127 | 0.121 | 0.116 |
| TGF(V$^{-1}$) at $V_{g}$ = 1.2 V | 3.69  | 3.85  | 3.96  | 4.15  | 4.25  | 4.33  | 4.41  |
| $I_{on}/I_{off}$ | $3.41 \times 10^{13}$ | $4.57 \times 10^{13}$ | $5.78 \times 10^{13}$ | $6.57 \times 10^{13}$ | $7.52 \times 10^{13}$ | $7.55 \times 10^{13}$ | $1.02 \times 10^{14}$ |
| $C_{gs}$ (F) | $3.78 \times 10^{-16}$ | $5.55 \times 10^{-16}$ | $7.40 \times 10^{-16}$ | $9.40 \times 10^{-16}$ | $1.16 \times 10^{-15}$ | $1.41 \times 10^{-15}$ | $1.68 \times 10^{-15}$ |
| $C_{gd}$ (F) | $5.06 \times 10^{-17}$ | $5.14 \times 10^{-17}$ | $5.24 \times 10^{-17}$ | $5.3 \times 10^{-17}$ | $5.35 \times 10^{-17}$ | $5.4 \times 10^{-17}$ | $5.45 \times 10^{-17}$ |
| $f_T$(Hz) | $1.19 \times 10^{13}$ | $7.78 \times 10^{12}$ | $5.46 \times 10^{12}$ | $3.97 \times 10^{12}$ | $3.03 \times 10^{12}$ | $2.38 \times 10^{12}$ | $1.92 \times 10^{12}$ |
capacitances are linearly dependent with the channel length, $L_{ch}$ and may be expressed by $C_{gs} = (\epsilon(W \cdot L_{ch})/t_{ox})$. Variation of $f_T$ with respect to gate voltage for different channel lengths with doping concentration $N_D$ at $10^{19}$ cm$^{-3}$ is shown in Figure 16. An improvement of $f_T$ happens due to the enhancement of $g_m$ and degradation of $C_{gs}$ and $C_{gd}$ for the shrunk JL DGMOSFETs. Generally, $f_T$ is defined by the expression $f_T = g_m/(2\pi(c_{gs} + c_{gd}))^{21}$ where it is inversely proportional to the $C_{gs}$ and $C_{gd}$ but directly proportional to the $g_m$. Increment of $g_m$ is comparatively more than $C_{gs}$ and $C_{gd}$ for the enhancement of gate voltage yields higher $f_T$. Figure 17 shows the variation of charge per unit area (Coulomb/meter$^2$) with respect to front gate voltage. From the above graphical interpretation, it is verified that charge builds up at the center of the channel of the JL DGMOSFET and directly depends on capacitance as well as gate voltage, $Q = C \times V$. Due to the advanced manufacturing technology of MOSFET, the possibility of existing interface traps at the Si-SiO$_2$ interface is approximately nil nowadays. However, the interface between high dielectric oxide material, HfO$_2$ and Si$_{1-x}$Ge$_x$ are not defect free. Nonstoichiometric Ge$_x$ formation and metallic Ge segregation in the interfacial layer of HfO$_2$ and Si$_{1-x}$Ge$_x$ play an important role in the degradation of the device performance.35 Numerous type of trap charges, which degrade the device performance are (a) interface-trapped charge, (b) fixed-oxide charge, (c) oxide trapped charge and (d) mobile ionic charge.36

To improve $I_d$, $SS$, and $g_m$, compound material Si$_{1-x}$Ge$_x$ is generally used instead of Si as a channel. The electrical properties of the device are further improved by implementing high dielectric material, HfO$_2$ as gate oxide. But complex interfacial reactions occur between the high-k film and the Si$_{1-x}$Ge$_x$ substrate which adversely interfere with the electrical performance of the films. In this manuscript, high electron mobility and high injection velocity III-V compound material GaSb is used as source for further improvement of electrical characteristics of the device under donor or acceptor trap charges. From Figure 18 it is evident that $I_d$ increases and decreases in the presence of donor-type and acceptor-type traps.

**Figure 16** Cut-off frequency with respect to front gate voltage for symmetric DG MOSFET

**Figure 17** Change in charge per unit area w.r.t. the $V_{gf}$
Under ionization, donor type traps are becoming positive charge ions yielding a screening layer between the depletion region and the heavily doped ground plane at the bottom of the device helps to enhance drain current. However, in opposite scenario acceptor traps become negatively charge ions under ionization and facilitate the depletion of the active device layer from the bottom reduces drain current.\(^{37}\)

## 4 | CONCLUSION

In this paper, the reliability of the device has been studied for different channel length from 50 to 20 nm considering GaSb as a source material for the SiGe JL DGMOSFET. The simulation results show that the device response of GaSb-SiGe JL DGMOSFET is better than the earlier structures made of Si or SiGe at 20 nm channel node. It is also verified from the simulation that the symmetric JL DGMOSFET performs better than the asymmetric one. In symmetric JL DGMOSFET, simulation focuses primarily on various short channel effects and how the use of compound III-V material and high-k dielectric material can minimize the degradation of these short channel effects. It is also found that this device is more viable at 20 nm channel length from the various parametric study with varying channel lengths.

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### CONFLICT OF INTEREST

The authors declare that there is no conflict of interest regarding the publication of this article.

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