Low Power Photo-Voltaic Harvesting Matrix Based Boost DC–DC Converter with Recycled and Synchro-Recycled Scheme

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Abstract: Photo-voltaic (PV) power harvest can have decent efficiency when dealing with high power. When operating with a DC–DC boost converter during the low-power harvest, its efficiency and output voltage are degraded due to excessive losses in the converter components. The objective of this paper is to present a systematic approach to designing an efficient low-power photo-voltaic harvesting topology with an improved efficiency and output voltage. The proposed topology uses a boost converter with an extra inductor in recycled and synchro-recycled techniques in continuous current mode (CCM). By exploiting the non-linearity of the PV cell, it reduces the power loss and using the current stored in the second inductor, it enhances the output voltage and output power simultaneously. Further, by utilizing the Metal Oxide Silicon Field Effect Transistor’s (MOSFET) body diode as a switch, it maintains a minimum hardware, and introduces a negligible impact on the reliability. The test results of the proposed boost converters show that it achieves a decent power and output voltage. Theoretical and experimental results of the proposed topologies with a tested prototype are presented along with a strategy to maximize power and voltage conversion efficiencies and output voltage.

Keywords: impedance matching; photo-voltaic; boost converter; reliability; low power harvest; synchronous rectifier; power loss reduction; energy recycling

1. Introduction

Energy harvesting provides a potential solution for “fit-and-forget” self-powered autonomous nodes used in wireless sensor networks (WSN)/Internet of Things (IoT) applications, making it unnecessary to replace the battery over the product’s lifetime [1]. The sensors require power, which, in many cases, is obtained from power harvesting. Among the clean sources is photo-voltaic (PV). The harvested energy from ambient light is the highest among Radio Frequency (RF), thermal and vibration energies [2,3], which makes it a good candidate for energy harvesting despite its challenges; such as impedance matching and non-linearity of this impedance. Improving the efficiency by increasing the output power, rather than reducing the power loss, does not seem to be a solution particularly in low power (LP) harvesting. Meanwhile, increasing the output voltage through cascading has a negative impact on the reliability, and it is not suitable for LP harvesting. Voltage multipliers using diodes suffer from excessive voltage loss and they are not applicable to the lower power harvest scheme. While it is important to improve both parameters without sacrificing one for another or imposing any negative impact on the reliability of the system, multiple topologies have been introduced when discussing the output voltage and efficiency. Typically, the output voltage of a single PV cell is very small (around 0.5 V) and should be boosted. Furthermore, the PV’s output impedance
is non-constant and changes in a non-linear pattern, introducing a challenge to match the load to the source for maximum power transfer. To ensure the PV operates in the Maximum Power Point Tracking (MPPT) mode, several methods have been proposed [4–6]. The work in [4] proposes a cascaded boost converter and sliding mode control for matching the PV impedance to the load, however, this will not be a favorable approach for the low-power harvesting due to the excessive loss, as a result of cascading. The authors in [5] demonstrate a MPPT for PV system using adaptive extremum seeking control and offer a state-space model using an averaging method. As mentioned, to make PV generation more competitive, it is important to maximize its power and output voltage. The work proposed in [6] discusses the PV internal resistance measurement using extremum-seeking control system.

The proposed work in [7] provides an overview of the recent development in circuit design for ultra-low power managements units (PMUs), and focuses mainly on the architecture and techniques required for energy harvesting from multiple sources. The work in [8] utilizes a complex control circuit and discusses harvesting up to 10 mW with good efficiency and voltage conversion ratio. The presented work in [9] examines ripple correlation and model reference adaptive controls to achieve MPPT with overall stability to maximize the power, the maximum voltage however, was not discussed. The paper referenced in [10] presents a Global MPPT for Flexible PV Modules and installation parameters effect of the aforementioned module; however, this is only applicable, to the flexible photo-voltaic module. In [11], a decent efficiency was reported, but it requires multiple switches and a complex control system.

The modeling and selection device for PV harvesting has been discussed in [12] with a decent theoretical efficiency, but the results are not supported with the actual test bench measurement. The work in reference [13] presents a general working principle and design procedures of an analog MPPT with Pulse Width Modulation, (PWM), multiplication for solar array. Berkovich and Axelrod [14] assert that increasing the output voltage using switched-capacitor is achieved; however, a switched capacitor can cause a high surge current. The proposed ultra gain step up converter in [15] and the proposed topology in [16] are not suitable for the LP harvesting due to an excessive number of components used.

The purpose of this research is to investigate and develop more efficient topologies for low-power PV harvesting. Through the application of a second inductor in a standard boost converter, this work will introduce an effective methodology to simultaneously increase the output power, power efficiency, and output voltage through the use of recycled energy. The proposed topologies further exploits the non-linearity of the PV cell to reduce the power loss.

This paper is organized as follows: in Section 2, a review of the output voltage, efficiency, and reliability issues in a boost converter using PV will be examined. In Section 3, a proposed topologies to improve the output voltage and efficiency concurrently, along with the circuit modeling and simulation will be presented; in Section 4, the experimental results and discussion will be provided and, finally, our conclusion will be presented in Section 5.

2. Maximum Power, Efficiency, Voltage, and Reliability Issues

2.1. PV Cell Characteristics Curve

A PV equivalent model is shown in Figure 1 [4–6].

![Figure 1. Single photo-voltaic (PV) cell equivalent circuit.](image-url)
Rs and Rp are the series and parallel resistances as a result of wire leads and PN junction, respectively [17]. The current equation of the PV is expressed as [18]:

$$I_{pv} = I_{sc} - I_o(e^{(V_{pv}+I_{pv}R_s)/nV_T} - 1) - \frac{(V_{pv} + I_{pv}R_s)}{R_p}, \tag{1}$$

where $I_{sc}$ is the short circuit current, $I_o$ is the reverse saturation current of the diode, $V_T$ is the thermal voltage, $V_{pv}$ is the output voltage of the cell and $n$ is the diode ideality factor.

In this paper, without loss of generality, a simplified model will be considered in which Rs and Rp are neglected. ($V_{pv} = V_p$, $I_{pv} = I_p$).

It is well known, that, the available power to the load will change as a result of shading. The MPPT algorithm is designed to ensure that the PV constantly operates in MPPT [5] where, $I_{mp}$, $V_{mp}$, and $P_{mpp}$ are the current, voltage, and power at the maximum power point, respectively.

$$P_{mpp} = I_{mp}V_{mp}. \tag{2}$$

The power loss and voltage drop in the boost converter are the two main obstacles to achieving higher efficiency and high voltage gain. In Figure 2, the IV and PV characteristic curves of a solar cell at five various irradiations, (G = W/m$^2$), have been simulated in MATLAB and are shown below. The constant current (CC) and constant voltage (CV) are the operating zones where PV exhibits such characteristic behaviour accordingly.

As shown, the solar cell current, voltage and power vary at various irradiations. The ratio of this voltage, $V_{pv}$, to the current $I_{pv}$ is defined as $R_{pv}$ or solar cell impedance [4]. This $R_{pv}$ is subject to a non-linear variation because of shading. Therefore, it is obvious that the maximum power cannot be transferred to load due to the violation of $R_{pv} = R_L$ condition, unless this impedance mismatch is corrected. A DC–DC boost converter is used as an interface between the load and solar cell as shown in Figure 3.
Figure 3. An impedance-matched PV boost converter.

The relationship between solar cell current and voltage using a boost converter in continuous current mode (CCM) is given as [4]:

\[
\frac{V_{pv}}{I_{pv}} = R_{pv} = R_L (1 - D)^2, \tag{3}
\]

where \(D\) is the duty cycle of the boost converter. The non-linear change of \(R_{pv}\) will cause an efficiency loss due to the impedance mismatch. For the regulation of efficiency, the following condition must be met [5]:

\[
R_{pv} = R_{in, boost} = R_L (1 - D)^2, \tag{4}
\]

where \(R_{in, boost}\) or \(R_{in}\), in short, stands for the input impedance seen from \(V_{pv}\) terminal Figure 3 (steady state mode). \(R_{in}\) can be tuned with the duty cycle so that \(R_{in} = R_{pv}\) for the maximum power transfer. The output voltage of the boost converter, neglecting voltage loss on the switches is given as [19]:

\[
V_o = \frac{V_{in}}{1 - D}. \tag{5}
\]

Voltage conversion efficiency, \(V_{CE}\), is defined as:

\[
V_{CE} = \frac{V_o}{V_{in}}, \tag{6}
\]

where \(V_{in}\) is the input voltage. The ideal matched efficiency is expressed as:

\[
\eta = \frac{R_{pv}}{R_L (1 - D)^2}. \tag{7}
\]

This method, ideally, is able to eliminate the efficiency loss as a result of mismatch by controlling the duty cycle. It is, however, unable to reduce the loss in the components, which are duty cycle-related. This issue will be addressed later in this section.

2.2. Output Voltage of a Conventional Boost Converter

The output voltage and efficiency calculation presented in previous section, using impedance matching for the efficiency regulation, are only valid for the ideal case. They cannot accurately predict the output voltage and efficiency for the LP harvesting scheme due to a considerable voltage drop and power loss in the diode and Metal Oxide Silicon Field Effect Transistor’s (MOSFET). For LP harvesting, \(V_o\) has to be accurately calculated in two phases:

**Phase 1:**

\[
0 < t < DT \quad t = t_{on}. \tag{8}
\]

In this period, the MOSFET switch is turned on. The circuit can be modeled as shown in Figure 4. (The DC resistance of the inductor is neglected). During this phase, the inductor current is building up linearly.
Figure 4. Boost converter when Metal Oxide Silicon Field Effect Transistor’s (MOSFET) switch is on.

The inductor voltage is calculated as [20]:

\[ V_L = V_{pv} - V_{sw} \]  
(9)

\[ I_L(t) = \left(\frac{V_{pv} - V_{sw}}{L}\right) t + I_{Lmin} \]  
(10)

\[ V_{sw} = D R_{DSon} I_{pv} \]  
(11)

where \(V_{sw}\) is the saturation voltage of the MOSFET and is negligible here due to a very small \(R_{DSon}\) and \(I_{pv}\). The inductor current during this period is:

\[ I_L(t) = I_{Lmax} \]  
(12)

The diode is off and output voltage is supplied from \(C_{out}\).

\[ \Delta I_L = I_{max} - I_{Lmin} = \left(\frac{V_{pv} - V_{sw}}{L}\right) DT \]  
(13)

where

\[ D = \frac{t_{on}}{T} \]  
(14)

Phase 2:

\[ t = t_{off} = T - DT. \]  
(15)

In this period, the MOSFET switch is off. The circuit can be modeled as in Figure 5. The diode is forward biased and ready to conduct. The MOSFET current is zero and the inductor depletes its energy to charge the output capacitor. The state equations can be written as:

Figure 5. Boost converter when MOSFET switch is off.

\[ V_L = -(V_o + V_F - V_{pv}) \]  
(16)

\[ I_L(t) = -\left(\frac{V_o + V_F - V_{pv}}{L}\right) (t) + I_{Lmax}, \]  
(17)

where:

\[ I_L(t = T - DT) = I_{Lmin}. \]  
(18)

Then:

\[ \Delta I_L = I_{max} - I_{Lmin} = \left(\frac{V_o + V_F - V_{pv}}{L}\right) (1 - D) T \]  
(19)
where $V_F$ is the diode forward voltage. By Equating (13) and (19), the output voltage is obtained:

$$V_o = \frac{V_{pv} - (1 - D) V_F}{1 - D}, \quad (20)$$

### 2.3. Power Consumption and Efficiency Analysis

To accurately predict the efficiency, the loss on each of the components in the boost converter has to be considered. Therefore, the total loss in the MOSFET which is the sum of switching, conduction, gate charge losses, and the loss in the diode and inductor, must be minimized as well. The ohmic switching loss of the MOSFET can be estimated from [21]:

$$P_{sw} = 0.25 I_p V_{p \max} (t_r + t_f)f, \quad (21)$$

where $t_r, t_f$ are the rise and fall time of the MOSFET, respectively, and $f$ is the switching frequency.

$P_c$ is the conduction loss in the MOSFET. With a MOSFET operating at a duty cycle $(D)$, in which $P_{cm}(t)$ is the instantaneous power loss over the switching cycle [22].

$$P_c = 1/T_{sw} \int_0^{T_{sw}} P_{cm}(t) \, dt = DR_{DS} I_{d\text{rms}}^2, \quad (22)$$

where $R_{DS}$ is the resistance between drain and source terminals. As shown in (20), increasing the duty cycle will increase the output voltage. However, increasing the duty cycle simultaneously increases conduction loss in the MOSFET as shown in (22).

The gate charge loss, $P_g$, can be estimated from [23] as:

$$P_g = V_{GS}fQ_g, \quad (23)$$

where $Q_g(nc)$ is the total charge of the MOSFET and $V_{GS}$ is the gate source voltage. The loss in the diode can be estimated from [24]:

$$P_{LD} = \frac{1}{T} \int_0^T (V_F + r_d i_D(t))i_D(t) \, dt = (1 - D)(V_F + r_d i_D(t))i_D(t). \quad (24)$$

As discussed earlier, to reduce the power loss as a result of mismatch, during shading, the duty cycle, $(D)$, has to be reduced. This however, increases the power loss in the diode based on (24). Consequently, although it reduces the power loss as a result of mismatched impedance, but it also introduces a duty cycle related power loss. Meanwhile, reducing the duty cycle reduces the output voltage. This highlights the shortcoming of an impedance-matched PV boost converter. An effective topology will be introduced in the next section.

The diode’s dynamic resistance $r_d$, its forward voltage, and the body diode voltage of the MOSFET have an impact on the efficiency, VCE and the output voltage. A comparison between MOSFET and Diode in terms of their body diode or forward voltages is given in Table 1.

A comparison between efficiency and output voltage of a Boost converter with single PV, using two different MOSFETs is presented in Table 2.

As shown, the efficiency with MOSFET CSD1657Q5B is reduced due to having larger $Q_g$ leading to a larger gate loss; however, the output voltage is larger due to its smaller body diode voltage. (For the efficiency calculation, the $Q_g$ was scaled down based on the operational gate source voltage).
Table 1. Comparison between various MOSFETS and DIODES.

| MOSFET        | Body Diode (V) |
|---------------|---------------|
| Csd16570q5b   | 1.00          |
| IRFz34        | 1.6           |
| IRF501        | 1.3           |
| RV1C002UN     | 1.2           |
| SI3900DV-T1-GE3 | 1.1         |

| Diode        | Forward Voltage (V) |
|--------------|---------------------|
| 1n4148       | 1 at 10 mA          |
| BYS10-25     | 1 at 1 A            |
| Bat54htig    | 0.5 at 10 mA        |
| S1 A/B       | 1.1 at 1 A          |
| NSR0520V2T1G | 0.48 at 500 mA      |

Table 2. A comparison between efficiency and output voltage of two different MOSFETs.

| MOSFET       | $R_{ds}$ (Ω) | $Q_g$ | $V_B$ (V) | $V_o$ (V) | $\eta$% |
|--------------|--------------|-------|-----------|-----------|---------|
| IRFZ34       | 0.05         | 46    | 1.6       | 1.09      | 69      |
| CSD1657Q5b   | 0.00068      | 124   | 1         | 1.34      | 58      |

2.4. Reliability

The reliability of systems is a good measure to compare their expected life-time [24]. In addition, material quality is positively correlated with the reliability of components [25]. A traditional boost converter consists simply of an inductor, a switch, and a diode [24]. The reliability of a circuit can be estimated by calculating the total failure rate of its components and it could be modeled based on the Military Handbook, Reliability Prediction of Electronics Equipment MIL-HDBK-217F [26].

To estimate the total failure of the boost converter, the sum of individual components failure rates must be calculated from [24]:

$$\lambda_{12} = \sum (\lambda_Q + \lambda_D + \lambda_L),$$

where $\lambda_{12}$ is the total failure rate of the components and $\lambda_Q$, $\lambda_D$, and $\lambda_L$ are failure rates (failure/hours) of the MOSFET, diode and inductor, respectively. The reliability function is expressed as [27]:

$$R = e^{-(\lambda_{12})t},$$

in which $t$ is the operational time. Meanwhile, the mean time to system failure is expressed as [28]:

$$MTTF = \int_{t=0}^{\infty} R (t).$$

Using [25] $\lambda_Q$ which is the failures/$10^6$ hours for a MOSFET is calculated as:

$$\lambda_Q = \prod \lambda_b \pi_T \pi_A \pi_E \pi_Q,$$

where $\lambda_b$ is the basic failure rate, $\pi_T$ is the temperature factor, $\pi_A$ is the application factor, $\pi_E$, is the environmental factor, and, finally $\pi_Q$ is the quality factor, accordingly. The thermal factor for the MOSFET is calculated from [24] as shown in Table 3.
Table 3. Temperature factor of components.

| Component   | Temperature Factor |
|-------------|--------------------|
| MOSFET      | $\pi_T = e^{-1925\left(\frac{1}{T_j + 273} - \frac{1}{298}\right)}$ |
| DIODE       | $\pi_T = e^{-3091\left(\frac{1}{T_j + 273} - \frac{1}{298}\right)}$ |
| Inductor    | $\pi_T = e^{0.11\times10^{-8.617}\left(\frac{1}{T_{HS} + 273} - \frac{1}{298}\right)}$ |

To calculate the junction temperature of MOSFET:

$$T_j = T_A + (R_{\theta JA} P_{LIFT}) = T_A + (R_{\theta JA}(P_c + P_g + P_{sw})),$$

(29)

in which $R_{\theta JA}$ and $T_A$ are the junction to air thermal resistance (${\degree}C/W$) and ambient temperature. Finally, the $\pi_T$ for the MOSFET can be calculated from (30) and Table 2.

$$\pi_T = e^{-1925\left(\frac{1}{T_A + 273 + (P_{sw} + P_g + P_c)R_{\theta JA}} - \frac{1}{298}\right)}.$$  (30)

The effect of duty cycle can be seen on the temperature factor of the MOSFET’s conduction loss through (22) and (30). The increase in the duty cycle would reduce the reliability according to (22), (25), (26) and (28)–(30). The heat is the ultimate factor affecting the reliability and can be further generated due to operating at a higher switching frequency and/or higher duty cycle, causing switching, gate charge, or conduction losses for each individual component, respectively.

In Table 4 the failure rate models for each component individually is shown [24]. To accurately calculate the reliability, the exact overcast profile is required, since the duty cycle varies according to this overcast. To circumvent this, the maximum duty cycle has been taken into consideration. Since, during the overcast, the duty cycle must be reduced, which reduces the power loss and heat accordingly. As a result, the calculated number for the reliability is representative of total minimum reliability, where (R%) shows the reliability percentage. The ideal reliability is 100%.

The impact of the output capacitor was not been taken into consideration due to the unavailability of equal series resistor, (ESR) of the capacitor in the data sheet. We conducted our estimation based on [24], however, the results are quite accurate. The overall minimum reliability of a boost converters, including MOSFET, diode, and inductor is plotted in Figure 6.

![Figure 6. Total minimum reliability at D = 0.8.](image)
Table 4. Failure rate models for the components.

| Component  | Failure Rate Model       |
|------------|--------------------------|
| MOSFET     | $\lambda_{MOSFET} = \lambda_b \times \pi_T \times \pi_A \times \pi_E \times \pi_Q$ |
| DIODE      | $\lambda_{Diode} = \lambda_b \times \pi_T \times \pi_S \times \pi_C \times \pi_Q \times \pi_E$ |
| INDUCTOR   | $\lambda_{Inductor} = \lambda_b \times \pi_T \times \pi_Q \times \pi_E$ |

3. Proposed Topologies

3.1. A Matrix Boost Architecture \([n \ m]\)

In this section, a general matrix boost architecture is proposed as \([n \ m]\), where \(n\) is the number of rows (PV cells put in a series) and \(m\) is the number of boost converters cascading as illustrated in Figure 7. (The bypass diode is shown in parallel with each PV cell). For a low-power harvest, a matrix with smaller \(m\) is recommended.

Figure 7. A matrix \([n \ m]\) of PV cells and boost converters.

3.2. Recycled Boost Converter Matrix \([1 \ 1]\)

Figure 8 shows the schematics of the proposed circuit. (Bypass diode is not shown). As shown, an extra inductor, \(L_2\), is placed between the source of \(Q_1\) and the ground terminal and a diode, \(D_2\), is then added. This inductor will assist to reduce the RMS input current and recycle its energy to charge the output capacitor, leading to the simultaneous improvement in both output voltage and efficiency. In the proposed topology, both inductors are charged in a series; however, during the discharge phase, the second inductor behaves as a current source in parallel with the inductor \(L_1\) to implement the current recycling using the body diode of the MOSFET. The operation principle of the proposed boost can be explained in two phases using Figures 8 and 9.

Figure 8. Proposed recycled boost converter, matrix \([1 \ 1]\).
Figure 9. Typical waveform of the proposed boost converter.

**Phase 1:**

Mode I

\[ t < t_0 \]  \hspace{1cm} (31)

Prior to \( t_0 \), the gate-to-source voltage \( V_{GS} \) of \( Q_1 \) is zero and its drain-to-source voltage \( V_{DS} \) is high. The output capacitor supplies the load.

Mode II \( t \in [t_0, t_1] \): In this period, the gate pulse arrives and turns \( Q_1 \) on. The drain current reaches \( I_d \), allowing the \( IL_1 \) and \( IL_2 \) inductors current build up linearly. There is no phase shift between two inductors current. (Ignoring \( R_{DS} \) and DC resistance of inductors, since \( X_L \) much greater than the sum of these resistances). During this interval, the source voltage of \( Q_1 \) also slightly rises due to the presence of \( L_2 \). This will be addressed in Section 4.

**Phase 2:**

Mode III \( t \in [t_1, t_2] \):

During this time interval, as the gate pulse reaches to zero, \( Q_1 \) turns off. The currents stored in \( L_1 \) returns it energy to the output capacitor via \( L_1-D_1-C_{out} \). Meanwhile, When \( Q_1 \) turns off, the energy stored in \( L_2 \) is released to the output capacitor via the \( D_3-D_1-C_{out} \). A negative voltage, will be generated on the source terminal when \( Q_1 \) turns off. Diode \( D_2 \) ensures that this negative voltage is limited by the \( V_F \) of the diode.

3.3. *Synchro-Recycled Boost Converter Matrix [3 1]*

The schematics of the proposed synchro-recycled boost converter matrix [3 1] is shown in Figure 10. (Bypass diode and the body diode of MOSFETs are not shown).

As shown, the synchronized MOSFET \( Q_2 \) replaced diode \( D_1 \) (see Figure 8) and the inductor \( L_2 \) and diode \( D_2 \) are added. The operation principle of this design is identical to the recycled boost except that \( Q_2 \) will be controlled by a complementary pulse emerging from the gate drive circuit. To avoid both MOSFETs turning on simultaneously, a delay (dead-time) was applied between gate pulses.

Figure 10. Proposed synchro-recycled boost converter, matrix [3 1].
3.4. Modeling of the Proposed Recycled Topology

By using the modelling method presented in [29–31] and neglecting the $V_{DS}$ voltage of the MOSFET and inductor’s DC resistance, the proposed recycled boost can be modeled as shown in Figure 11, where $r_D$, $r_B$, and $V_B$ are diodes, body diode dynamic resistors, and body diode voltage, respectively. The current of $I_{L2}$ is smaller than the current of $I_{L1}$, since $I_{L2}$ will be limited by two diode dynamic resistances.

![Figure 11. Averaged DC model of the recycled boost converter, matrix [1 1].](image)

For the proposed topology, using the volt-second balance principle, (neglecting the Diode’s dynamic resistances), the output voltage can be calculated:

$$V_o = \frac{V_{pxx}(1 + D)}{(1 - D)} - V_B - V_F. \quad (32)$$

where $V_{pxx}$ is the new solar cell voltage post $V_{mp}$, which is obtained using Omega-Wright function given below [18]:

$$\frac{V_{pxx}}{\omega(L_1 + L_2)} = I_{sc} - I_o(e^{(V_{pxx} + IpR_s)/nV_T} - 1) - \frac{(V_{pxx} + IpR_s)}{R_p}. \quad (33)$$

Meanwhile, the discharge current slope, ($m$) for the inductor $L_1$ in CCM is obtained from [30]:

$$m = \frac{-(V_o - V_{pxx})}{L}. \quad (34)$$

Since $V_{pxx}$ has increased, this slope is reduced leading to the larger average discharge current and higher output voltage, accordingly.

3.5. Simulation of the Recycled Topology

To validate the recycled topology, a simulation was also conducted in PSIM platform. The result of this simulation is shown in Table 5.

| Inductor Currents (RMS) | (mA) |
|------------------------|------|
| $I_{L1}$               | 4.58 |
| $I_{L2}$               | 3.22 |
| $I_{L_{Std}}$          | 7.06 |
| Diode Currents (Ave)   | (mA) |
| Standard               | 1.56 |
| Proposed              | 1.96 |
| Output Voltage         | (mV) |
| Standard               | 592  |
| Proposed              | 800  |
The simulation result shows that the output voltage of the recycled topology is greater than the standard boost, whereas its input current is smaller, which is attributed to reducing the loss. These results are consistent with Section 3.2, as expected and discussed.

4. Experimental Validation and Discussion

4.1. Prototype

To verify the validity of the proposed topology, a prototype was built. The tests were conducted on multiple matrix boost configurations. The matching duty cycles were chosen for each matrix to yield the maximum efficiency while the load was kept constant at $R_L = 490 \, \Omega$. The prototype implementation of a [1,1] synchro-recycled Matrix is shown in Figure 12.

![Figure 12. The prototype implementation of synchro-recycled matrix [2 1].](image)

As shown, it consist of, two inductors, two MOSFETs, a diode, an input/output capacitors, a PV cell, a load and a finaly a micro-controller port to program the gate pulse frequency and duty cycle. (To test the recycled topology, the second MOSFET was replaced with a diode). The components description used in the prototypes shown in Table 6.

| Component         | Description                                      |
|-------------------|--------------------------------------------------|
| MOSFET N Type     | IRFz34, IRF501, D2 Pack                          |
| Inductor          | SPR1210A-181MCT, 180 uH                           |
| Capacitor         | UKL1E101KPDANA 1000 uF                           |
| Diode Schottky    | MBR0520LT1, 1SS394TE85LFCT                       |
| PV cell           | KXOB22-12X1F                                     |
| PWM Pulser        | PIC Micro-Controller                             |

4.2. Test Result

The tests were conducted on multiple matrix boost configurations. To investigate the performance of the proposed topologies, two tests were conducted in which the matching duty cycles were chosen for each matrixes to yield the maximum efficiency with a constant load of $R_L = 490 \, \Omega$ and the second test, in which, the overcast was applied and the non-matched impedance remained uncorrected. Furthermore, the tests were conducted with various MOSFETS under various operating conditions with multiple matrix to investigate the degree of in-dependency of the proposed topologies. A performance comparison between a standard and recycled boost smaller matrix is shown in Table 7.

| Topology  | $V_o$ (V) | $\eta$ (%) | $V_{CE}$ | $P_{in}$ | $R$ (%) |
|-----------|-----------|------------|----------|----------|---------|
| Standard  | 1.295     | 38         | 2.3      | 9.98     | 0.9737  |
| Recycled  | 1.670     | 87.1       | 2.8      | 6.53     | 0.9680  |

As shown, compared to a standard boost converter, the output voltage and efficiency have been simultaneously increased in the proposed circuit, whereas the input power was reduced as a result of
$L_2$ inductor’s impedance limiting the current. The output voltage increases mainly due to the recycled current from $L_2$.

A performance comparison between standard and recycled boosts for a larger matrix is shown in Table 8.

**Table 8.** Performance comparison between standard and proposed recycled [3 1] matrix at $R_L = 490 \, \Omega$, non-matched, $f = 83.4$ KHz, $D = 0.549$ for the same Gate Loss, IRF501, $P_{LD}$ (mW).

| Topology   | $V_o$ (V) | $\eta$ (%) | $V_{CE}$ | $P_{LD}$ (mW) |
|------------|-----------|------------|----------|---------------|
| Standard   | 2.423     | 45.65      | 1.64     | 7.36          |
| Recycled   | 2.690     | 73.75      | 1.66     | 4.37          |

As shown, the power loss in the diode, $P_{LD}$, has been reduced drastically, while the output voltage, efficiency and $V_{CE}$, has been increased concurrently.

A performance comparison between standard and recycled boosts for a larger matrix with a matched impedance with a different MOSFET is shown in Table 9.

**Table 9.** Performance comparison between standard and recycled [3 1], $f = 80$ KHz, $R_L = 490 \, \Omega$, with $D = 0.57$ at strong overcast with a matched impedance.

| Operating Parameters       | Standard Boost | Recycled Boost |
|----------------------------|----------------|----------------|
| $V_o$ (V)                  | 2.00           | 2.4            |
| $P_o$ (mW)                 | 8.16           | 11.75          |
| Input Power (mW)           | $12.96 + 1.16 \,*$ | $12.39 + 1.16 \,*$ |
| Efficiency (%)             | 57.8           | 86.7           |
| $V_{CE}$                   | 1.85           | 1.71           |
| Reliability (%)            | 0.9716         | 0.9680         |

* Gate charge loss (mW).

In Table 10, a performance comparison between standard and synchro-recycled boost under non-matched impedance is shown.

**Table 10.** Performance comparison between standard and proposed synchro-recycled matrix [3 1], $f = 83.4$ KHz, Non-matched with $D = 0.58$ and MBR0520LT1, IRFZ34.

| Operating Parameters       | Standard | Synchro-Recycled |
|----------------------------|----------|------------------|
| $V_o$ (V)                  | 1.38     | 1.431            |
| $P_o$ (mW)                 | 3.886    | 4.179            |
| Efficiency (%)             | 33.47    | 33.70            |
| $V_{CE}$                   | 1.169    | 1.266            |
| Reliability (%)            | 0.9737   | 0.9558           |

As shown in Table 10, even for the case of non-matched impedance, with the same efficiency, the proposed synchro-recycled boost outperforms standard boost in terms of $V_{CE}$, output power, and output voltage concurrently.

Multiple tests were conducted at various operating conditions, components and overcast, to investigate the in-dependency of the proposed topologies, where the duty cycle, switching frequency and overcast level, were varied and the test results were recorded.

A comparison between all designs at various frequencies under two overcast is shown in Tables 11 and 12. (The overcast level was not measured, however, shading applied by re-positioning and attenuating the light source, and verifying the reduced power). The analysis of these results is provided in Section 4.7.2.
Table 11. Performance comparison between standard and proposed using Boost matrix [3 1], 
f = 83.4 KHz with D = 0.549, non-matched.

| Topology      | $V_o$ (V) | VCE (V) | $\eta$ (%) | $P_{in}$ * | $R$ (%) |
|---------------|-----------|---------|------------|------------|---------|
| Standard      | 2.66      | 1.48    | 24         | 28.64      | 0.9736  |
| Recycled      | 2.8       | 2.0     | 60         | 20.14      | 0.9696  |
| Synchro-Recycled | 2.78     | 1.43    | 50         | 21.755     | 0.9518  |

* Gate charge loss (mW) included.

Table 12. Performance comparison between standard and proposed Boost, matrix [3 1], f = 95.39 KHz, 
D = 0.53, non-matched, and MBR0520LT1, IRF501.

| Topology      | $V_o$ (V) | VCE (V) | $\eta$ (%) | $P_{in}$ | $R$ (%) |
|---------------|-----------|---------|------------|----------|---------|
| Standard      | 2.64      | 1.46    | 41         | 27.33    | 0.9736  |
| Recycled      | 2.7       | 1.40    | 60         | 17.88    | 0.9696  |
| Synchro-Recycled | 2.66     | 1.37    | 52         | 18.91    | 0.9518  |

4.3. The Boost Converter Experimental Characteristics Gain

To verify the voltage gain characteristics of a boost converter, the experimental voltage gain plot 
of the standard and recycled boost topologies vs. duty cycle with $R_L = 490 \Omega$ at constant irradiance at 
switching frequency, $f = 105.9$ KHz with 5% variations, is shown in Figure 13.

![Figure 13](image)

Figure 13. The voltage gain of the proposed recycled and standard boost converter vs. duty cycle, 
matrix [1 1].

As discussed, at strong overcast, the duty cycle has to be reduced to match the load to the PV 
cell. As shown, the proposed recycled topology is superior to the standard in a wide range of duty 
cycle. Although, as illustrated in Figure 13, the ratio of the voltage gain of the proposed topology to 
the standard boost, at smaller duty cycles, is much larger and it is being reduced as the duty cycle 
advances. This is due to (24), which substantial voltage drop and power loss, can be saved at smaller 
duty cycles, which further reiterates the effectiveness of this topology at strong overcast.

4.4. The Inductor Voltage and Current of the Recycled Boost Topology

For the proposed circuits, the value of both of the inductors are required to be equal. As mentioned, 
during Mode II, the source voltage slightly rises. When the inductor current is suddenly disrupted, 
a high voltage is generated on the MOSFET source terminal due to $di/dt$ effect. This transient spike 
can be absorbed by a snubber circuit. The sharp transient on the source terminal was measured 
maximum $\pm 1 V$.

To measure the inductor current in the proposed topology, a %1, 1 $\Omega$ resistor was added in series 
with the inductor and its voltage with respect to ground at different frequencies and duty cycles was 
measured through an oscilloscope. The current and voltage across inductor $L_2$, ($L_1$ was short-circuited),
is shown in Figure 14. This further corroborates the contribution of current from $L_2$. As expected, this current was found smaller than $I_{L_1}$.

![Figure 14. The current (top) and voltage waveform of $L_2$ for a matrix boost [1 1].](image)

4.5. Argument

The improvement reported in Tables 7–12 cannot simply be achieved by putting $L_1$ and $L_2$ in a series or increasing the inductance value of the inductor in a standard boost. By using two inductors in a series, in the absence of the gate pulse, the initial voltage on the output capacitor will be reduced due to the excessive impedance, while in the proposed circuit, this current is solely limited by single inductor’s impedance. To demonstrate the superiority of the recycled topology, it was tested and compared against standard boost (case A) and a boost with two inductors in a series (case C). The result are summarized in Table 13.

| Topology  | $P_{in} (V \times mA) + P_g$ | $P_o$ (mW) | $\eta$ (%) | $V_o$ (V) |
|-----------|-----------------------------|------------|------------|-----------|
| Case A    | 0.595 x 5.83 = 3.46         | 1.84       | 21         | 0.95      |
| Recycled  | 0.6 x 3.24 = 1.94           | 2.93       | 40.7       | 1.2       |
| Case C    | 0.587 x 6.46 = 3.79         | 2.41       | 26.5       | 1.087     |

As shown in Table 13, the recycled topology has a maximum output power and output voltage among all and it only requires a minimum input power. Multiple tests at various frequencies, duty cycles, and irradiance corroborated the consistent results and superiority of the proposed circuit.

4.6. A Performance Comparison with State of Art Power Harvest

A performance comparison with other state-of-the-arts solar power harvesters is listed in Table 14.

| $V_{in}$ | $P_o$ | $\eta$ (%) | $V_o$ | MPPT | Converter Architecture |
|----------|-------|------------|-------|------|------------------------|
| This work (Recycled) | 0.15–0.62 | 8.16 | 87.1 $^2$ | 0.8–2 | No Single stage Boost, single switch |
| Charger 2011 [8] | 0.5–2 | 5–10 | 80 | 0–5 | Yes Single stage Boost two switches |
| Charger 2018 [32] | 0.2–1 | 20 | 89 | 0.4–1.4 | Yes Single stage Buck Boost |
| Dual 2018 [33] | 0.4–0.8 | 84.4 | 1.2 | No Single stage Boost two switches |
| Dual 2016 [34] | 0.3–3.6 | 5.4 | 85 | 0 | No Single stage Boost two switches |
| Dual 2012 [35] | 0.15–0.75 | 5–10 | 83 | 1.8 | Yes Single stage Boost two switches |

$^1$ Maximum Power (mW); $^2$ At 125 KHz, $R_L = 490 \Omega$, 5.69 mW.

As shown, compared to the other works, the proposed topology, (recycled) is able to extract higher voltage, higher power, higher efficiency, and higher VCE, concurrently (during strong overcast) with a minimum input, from a single PV cell. Meanwhile by keeping the number of switches at minimum, (single), it has drastically reduced the control circuitry and programming features rendering...
an uncompromised reliability. Although, the output power is reduced during the overcast to 5.69 mW, the efficiency remained superior.

4.7. Discussion

4.7.1. Reliability

For the both proposed topologies, as reported in Tables 7–12, since the loss was reduced, the reliability has been improved; however, the negligible reduction has resulted in the introduction of two additional components according to (25) and (26).

4.7.2. Result Analysis

As result analysis demonstrated, the proposed topologies are substantially effective when PV cell operates post $V_{mp}$, where the cell behaves as a voltage source. In this zone, a substantial power loss can be saved by exploiting the non-linearity of the cell (see Figure 2).

As shown in Table 7, the recycled boost converter outperforms the standard boost in terms of efficiency, output voltage, and voltage conversion Efficiency (VCE), concurrently by exploiting the non-linearity characteristics of the solar cell in the CV area, (see Figure 2) and reducing the input current leading to the substantial improvement. By introducing the second inductor, the Root Mean Square (RMS) current supplied by the PV cell is reduced, which leads to a reduction in power loss, particularly in the diode (see Table 8). The current stored in this inductor contributes to the output voltage by discharging into the output capacitor.

Comparing the results shown in Tables 8 and 9, a higher efficiency can be achieved while impedance is matched to the load (in Table 8, the required duty cycle based on the overcast has been given to the converter, therefore, there are no losses as a result of reflection).

As shown in both tables, the superiority of the recycled topology compared to the standard boost is profound, despite operating conditions, overcast, impedance matched or non-matched, except with a negligible impact on the reliability.

As shown in Table 10, for the synchro-recycled boost, the test was conducted for the MOSFET replacing the diode and the insertion of the second inductor. In this test, the insertion of the second inductor has caused some current drop, (and slight drop in the input power). The MOSFET used in this test had a larger body diode voltage than Schottky diode’s forward voltage. This led to an increased voltage drop and power loss on the MOSFET; however, the current in the second inductor has increased the output voltage and the output power concurrently. Achieving comparable efficiency in both topologies originates from simultaneously increasing the loss and output power. However, the output voltage, power, and VCE have been improved compared to the standard boost.

A comparison between various designs at two different frequencies and overcast are shown in Tables 11 and 12. As a result of the second inductor, the input power decreased by diminishing the input current and by exploiting the non-linearity of the I–V. Meanwhile, the efficiency and output voltage have simultaneously increased, with a negligible impact on the reliability. Although the non-matched impedance resulted in lower efficiency in both cases, the proposed topologies were shown to be superior to the standard boost, despite of operating conditions and overcast. In Table 12, the VCE does not show much improvement, this is due to, mainly, a smaller D, which causes more power loss and voltage drop on the diode or body diode of the MOSFET (synchro-recycled case) according to (24). With a better understanding of a MOSFET’s body diode voltage, and carefull selection, the VCE can be further optimized.

The aim of these tests under various conditions was to demonstrate the superiority of proposed topologies and their degree of in-dependency regardless of components, overcast, and matched or non-matched conditions.
5. Conclusions

In this paper, two methodologies were proposed: (i) a recycled boost converter, and (ii) a synchro-recycled boost converter which serve to concurrently reduce power loss and improve efficiency, output voltage with minimum impact on the reliability. The proposed circuits, outperform the recent LP harvesting by exploiting the non-linearity of the PV cell. Compared to other methods, the advantages of the proposed topologies are concurrent improvements in output voltage, output power, and efficiency; a reduction in hardware (single MOSFET); a nearly intact reliability; and an ability to harvest power at strong overcast. (The synchro-recycled is utilizing single MOSFET, where the second MOSFET has only replaced the diode).

The results of the conducted tests at various operating conditions, overcast and components reveal the relative in-dependency of this topology from operating conditions.

The proposed recycled topology yield a decent efficiency of 87.1% and 60% non-matched from a single PV cell with an improved output power, and output voltage, concurrently. Finally it renders an uncompromised reliability, due to its reduced hardware size and circuitry.

Our future research, will focus on the improvement of PV battery charger performance at strong shading. This is a promising area of research and is yet to be explored.

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Abbreviations

The following Nomenclature are used in this manuscript:

- \( R_L \): Load Resistor
- \( P_{in} \): Input Power (mW)
- \( P_o \): Output Power (mW)
- \( P_{LFET} \): Total power dissipated in MOSFET
- \( I_{L_{std}} \): Inductor current, standard boost (mA)
- \( I_{L_1} \): Current in the first inductor (mA)
- \( I_{L_2} \): Current in the second inductor (mA)
- \( V_{CE} \): Voltage Conversion Efficiency
- \( V_F \): Diode forward voltage (V)
- \( V_B \): MOSFET Body Diode (V)
- \( V_{in} \): Input Voltage (V)
- \( D \): Duty Cycle
- \( \Delta D \): The error between set and actual
- \( \Delta DE \): Percentage of Error in \( \Delta D \)
- \( \omega \): Angular Velocity

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