ReS₂ based high-k dielectric stack charge-trapping and synaptic memory

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1. Introduction

With developments in the information age, data size in various media is explosive. A huge quantity of data requires more storage devices with higher performance and smaller size.\(^1\) Further miniaturization of traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) is reaching its limitation.\(^2\) Two-dimensional (2D) materials with atomic thickness are prospective semiconductors for future storage devices. 2D materials such as graphene and transition metal dichalcogenides (TMDs) have been widely explored and they have been demonstrated with excellent optical and electronic properties.\(^3-10\) Most widely researched 2D materials such as MoS₂ and WSe₂ have a symmetric lattice structure showing isotropic electronic properties, while anisotropic TMDs, due to a distorted lattice structure, have been rarely studied. Rhenium disulfide (ReS₂) is a typical anisotropic material with a distorted octahedral (1 T) crystal structure.\(^11,12\) Compared to the other TMDs that have a monolayer structure with a direct bandgap and a multilayer structure with an indirect bandgap, ReS₂ within ten layers are all considered to have direct bandgap.\(^12\) Therefore, the interlayer coupling energy is much weaker in ReS₂, which makes the monolayer exfoliation much easier and facilitates the fabrication of ReS₂ memory devices.

The explosive growth of data requires not only better data storage, but also smarter data processing. Computer performance in a von Neumann system is reaching its limits because the arithmetic unit and the memory are separated, and there is limited data transmission speed.\(^1,3-15\) However, the human brain, with about \(10^{11}\) neurons and \(10^{15}\) synapses, can compute and store information efficiently.\(^6,17\) Therefore, scientists have done lots of research to mimic the workings of the human brain,\(^8,19\) and devices with synaptic properties are the basis for realizing artificial intelligence.\(^20-22\)

In this work, we fabricated a high-k dielectric stack memory device using anisotropic 2D ReS₂ material, and we obtained a big memory window, fast P/E speed, excellent retention ability. When we applied it to synaptic emulation, we successfully simulated the short-term plasticity (STP), long-term potentiation (LTP), and long-term depression (LTD) behavior. This proves that our device has both a storage and synaptic capability. Compared with the previous abstract for SSDM 2019,\(^23\) this paper has added the following content: synaptic performance such as LTP, LTD have been shown to demonstrate the synaptic properties of our device. And the principle behind the device performance is explained in more detail. From the selection of two-dimensional materials (ReS₂) to the manufacture the device, further description has been added.

2. Experimental methods

Figure 1(a) shows the side and top views of the monolayer ReS₂ crystal structure, wherein adjacent Re (blue) atoms are bonded in the form of zigzag four-atom clusters on account of Peierls distortion. The a and b arrows, which are 61.03° or 118.97° apart are, respectively, the second-shortest axis and the shortest axis in the basal plane.\(^24\) Previous studies have testified that the maximum mobility of ReS₂ crystal is along the shortest b axis which corresponds to the Re–Re atomic chain direction.\(^25\) The atomic force microscopy (AFM) image of the ReS₂ film is shown in Fig. 1(c), and 1(d) shows that the thickness of the ReS₂ film is about 3.7 nm indicating a five-layer ReS₂ film (0.7 ~ 0.8 nm for a monolayer film). When manufacturing the ReS₂ memory device, direction b was selected as the direction of the channel current to best display memory properties. The schematic structure of our ReS₂ memory device is shown in Fig. 1(b), a highly p-type doped Si coated with a 200 nm SiO₂ was used as the substrate. After physical vapor deposition operation, the SiO₂/Si substrate was covered by a layer of 70 nm indium tin oxide (ITO) film, then annealing them in N₂ for 10 min at 400 °C. The sandwich type Al₂O₃/ZrO₂/Al₂O₃ structure with a 12/4/4 nm thickness was grown on ITO by atomic layer deposition (ALD). Then, a mechanically exfoliated five-layer ReS₂ film was deposited on the sandwich stack and carpeted with Ti/Au electrodes with a thickness of 10/70 nm. In our ReS₂ memory device, the ITO and Ti/Au layer act as back gate electrode, source and drain electrodes, respectively. Compared to the traditional top gate design which directly deposit the high-k dielectric on the channel materials and cause great damage to TMDs,\(^26\) the back gate structure well protects the properties of ReS₂, making sure our device...
has good performance. The 12 nm thick Al₂O₃ layer acts as a barrier layer, the ZrO₂ and 4 nm Al₂O₃ layer act as an electron capture layer, and a tunneling layer, respectively. Since the conduction band of ZrO₂ is lower than Al₂O₃ and the valence band is higher than Al₂O₃, this sandwich structure can effectively accomplish charge capture and storage. When testing synaptic performance, the ITO back gate acts as a presynapse neuron, and the Ti/Au electrodes act as the postsynapse neuron. A small and constant voltage is applied between the source and drain electrodes while the ITO back gate electrode is applied with pulses to modulate synaptic device performance.

3. Results and discussion

The output curve displays the drain-to-source current (I_{ds}) which first rises linearly and then becomes saturated when the drain-to-source voltage (V_{ds}) changes from 0 V to 1 V at a fixed back gate voltage, as shown in Fig. 2(a). The excellent saturation characteristics correspond to the strong channel regulation by the ITO back gate electrode. Figure 2(b) shows four clockwise hysteresis loops at different V_{bg} sweep ranges, the memory window increased from 1 V to 4 V when changing the sweep range from ±2 V to ±5 V, and the On/Off current ratio is over 10⁶ at a 5 V V_{bg} swing. These memory windows are symbolic of our device as memory, and provided a possibility for synaptic applications. When we scan the back gate voltage forward, carriers in the ReS₂ channel gained enough energy to move freely as the voltage reaches the threshold. A significant increase of carriers in the channel will lead to the increase of I_{ds}. In backward sweeping, fewer electrons move freely as the energy supplied becomes smaller, and the channel current gradually decreases. when the back gate voltage drops to a certain threshold, the channel current would be turned off. These characteristics indicate a typical n-type memory device. The energy band diagram of the device is shown in Fig. 2(c), where it can be seen when applying a positive voltage on the ITO back gate electrode, the energy bands bent in the direction of ITO, and the electrons gathered in the ReS₂ channel tunneled through the Al₂O₃ layer to the ZrO₂ layer. However, negative voltage excited the electrons to move from the ZrO₂ layer to the multilayer ReS₂, and the energy bands bent in the direction of the channel. To get a better sense of charge moving, the P/E operations were performed to demonstrate the capture and release of electrons between the ReS₂ channel and the charge-trapping layer. A clear right shift of the I_{ds}–V_{bg} curves can be observed when increasing the programming time. As shown in Fig. 3(a), a threshold voltage shift (ΔV_{th}) of 1 V was achieved after a 3 V, 1 s programming pulse. Figure 3(b) shows the erasing characteristics with different erasing time at fixed −3 V back gate pulses. Obviously, as the erasing time increases, the current curve shifts to the left. In the above test, the voltage applied between the source and drain was 100 mV, when increase that voltage, the channel current behaves differently. You can see from Fig. 3(c), at the same 3 V programming pulse but 500 mV drain-to-source voltage, the threshold voltage is smaller and the current value is larger. It indicates that channel electrons are more easier to be activated at high V_{ds} voltage. After P/E operations, the memory window can keep...
Fig. 2. (Color online) (a) Output characteristics ($I_{ds}$–$V_{ds}$) of the ReS$_2$ memory device at a fixed $V_{bg}$ changing from −2 V to 2 V with the step of 1 V. (b) $I_{ds}$–$V_{bg}$ hysteresis loops in different $V_{bg}$ sweep ranges of ±2 V, ±3 V, ±4 V, and ±5 V, respectively. (c) Energy band diagram of the ReS$_2$ memory devices with positive and negative ITO voltage, respectively.

Fig. 3. (Color online) (a) Programming operations with different pulse duration at a fixed 3 V pulse amplitude. (b) Erasing operations with different pulse duration at a fixed −3 V pulse amplitude. (c) Programming operations under 500 mV drain-to-source voltage. (d) Endurance characteristics of the ReS$_2$ memory device. The P/E operations were performed by applying 3 V, 1 s and −3 V, 1 s back gate voltage pulses, respectively.
steady for a long time [Fig. 3(d)], so our device has excellent retention properties.

The above results show good storage performance, and then we will do some synaptic stimulation to explore the synaptic properties of the device. A pair of negative pulses (−1 V, 10 ms with 2-s interval) was applied at the ITO back gate, and the typical excitatory postsynaptic current (EPSC) was detected. The current increment caused by two pulses are both 0.95 nA [Fig. 4(a)]. The increase in current is due to the number of electrons in ReS2 channel increasing. Because the negative voltage provides energy for electrons in ZrO2 to tunnel through the Al2O3 tunneling layer into the ReS2 channel. The changes in current caused by voltage pulses is similar to that of a biological synapse.27) The impulses emitted by presynaptic neurons are transmitted by synapses to postsynaptic neurons and then are converted into a postsynaptic current (PSC).28) Electron tunneling only happens when a pulse is stimulated. Since there is an Al2O3 layer between the ReS2 channel and the ZrO2 high-k layer, when the pulse is over, electrons cannot tunnel back, and would stay in the ReS2 channel. So the current increased and could be maintained for a long time. This process corresponds to the long-term potentiation (LTP) in the biological synapse.27) When positive voltage pulses are applied (2 V, 10 ms with 2-s interval), the inhibitory postsynaptic current (IPSC) was observed. As shown in Fig. 4(b), the channel current decreased after impulse stimulation, this phenomenon was called long-term depression (LTD). The decrease of current is 2.95 nA, 0.55 nA and 0.38 nA, respectively. When we increased the input pulse voltage, the postsynaptic current increased accordingly. As shown in Fig. 4(c), the EPSC increased over 20 times when changing the input pulse voltage from −1 V to −5 V. When we continuously applied the negative pulses (−5 V, 10 ms with 1 s interval), the continuous rising current was observed, as shown in Fig. 4(d). Different current values correspond to different conductance states. In this work, we obtained 50 conductance states with 50 continuous impulses. The conductance values are weights during a nerve signal transduction process,29,30) this suggests that our devices are have potential as synaptic devices. In our other studies, we further demonstrate the synaptic properties of the ReS2 device and describe in more detail how they are applied to artificial intelligence.31)

4. Conclusions
In this work, we fabricated a high-k dielectric stack memory device using anisotropic 2D ReS2 material. The operation voltage of our device with only a 20 nm distance between the ReS2 channel and the ITO electrode is below 5 V, promising fast P/E speed and excellent retention ability. Besides, our device demonstrates some fundamental synaptic behaviors such as long-term potentiation and long-term depression. These features could enable our device to be used as a next generation ultra-thin memory device in the future.

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