ScalaBFS: A Scalable BFS Accelerator on HBM-Enhanced FPGAs
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Abstract—High Bandwidth Memory (HBM) provides massive aggregated memory bandwidth by exposing multiple memory channels to the processing units. To achieve high performance, an accelerator built on top of an FPGA configured with HBM (i.e., FPGA-HBM platform) needs to scale its performance according to the available memory channels. In this paper, we propose an accelerator for BFS (Breadth-First Search) algorithm, named as ScalaBFS, that builds multiple processing elements to sufficiently exploit the high bandwidth of HBM to improve efficiency. We implement the prototype system of ScalaBFS and conduct BFS in both real-world and synthetic scale-free graphs on Xilinx Alveo U280 FPGA card (real hardware). The experimental results show that ScalaBFS scales its performance almost linearly according to the available memory pseudo channels (PCs) from the HBM2 subsystem of U280. By fully using the 32 PCs and building 64 processing elements (PEs) on U280, ScalaBFS achieves a performance up to 19.7 GTEPS (Giga Traversed Edges Per Second). When conducting BFS in sparse real-world graphs, ScalaBFS achieves equivalent GTEPS to Gunrock running on the state-of-art Nvidia V100 GPU that features 64-PC HBM2 (twice memory bandwidth than U280).

Index Terms—FPGA; Hardware Accelerators; Breadth-First Search; Graph Analytics

I. INTRODUCTION

BFS (Breadth-First Search) is one of the most fundamental algorithms of Graph theory and is widely used in application domains, such as navigation [1], social network [2], and many others. The computation of BFS, however, is famous for its irregular memory accesses and low computation-to-memory ratio [3]. To boost the performance of BFS, a computer system needs a large memory bandwidth, more specifically, a large memory bandwidth for random accesses. For such reason, BFS is chosen as one of the key benchmarks in Graph500 [4] to measure the capability of handling graph computing workloads of a computer system.

For the low cost and massive storage capacity, DRAMs (i.e., DDR RAMs) are widely used as the storage devices in most computer systems nowadays. But DRAMs yield much lower bandwidth when handling random accesses than sequential accesses, and their single-channel performance is limited (e.g., 19.2GB/s for DDR4). To improve the memory bandwidth, newly emerging memory techniques, such as HMC (Hyper Memory Cube) [5] and HBM (High Bandwidth Memory) [6], are proposed. HMC stacks multiple DRAM dies and logic dies into a single stack and connects with computing units (e.g., CPU/GPU/FPGA) with a serial link providing bandwidth up to 240GB/s. Similarly, the HBM technique stacks multiple DRAM dies and a logic die into a single stack, but exposes multiple memory channels to the computing units. By this, HBM can easily scale its bandwidth with more stacks (thus more memory channels). For example, two stacks of HBM2 (the second generation of HBM) provide up to 460GB/s aggregated bandwidth in Xilinx U280 [7], while four stacks of HBM2 provide up to 900GB/s aggregated bandwidth in Nvidia V100 GPU [8].

The unprecedented huge memory bandwidth, especially the scaling memory channels provided by HBM, makes it possible to build efficient accelerators for bandwidth-critical workloads like BFS. Since with multiple memory channels, HBM can compensate the weakness on random memory accessing of the underlying DRAM devices. However, it is still challenging to design an FPGA-based BFS accelerator that sufficiently exploits the increasing number of memory channels, since the accelerator itself needs to be scalable in design to match HBM’s massive memory bandwidth.

To investigate this research direction, we design a BFS accelerator, named as ScalaBFS, in this paper. By attaching each memory channel with configurable amounts of processing elements, ScalaBFS can efficiently exploit the memory bandwidth provided by an HBM to improve the performance of BFS. To the best of our knowledge, our work is the first system design that accelerates BFS on the FPGA-HBM platform.

Our paper makes the following contributions:

- proposes a design of BFS accelerator, that scales its performance according to the available memory channels of the FPGA-HBM platform;
- provides an open-source implementation that works on a real FPGA accelerator card (Xilinx Alveo U280) for data centers;
- extensively evaluates our prototype system and compares its performance with state-of-art FPGA approaches as well as those on GPUs.

The rest of paper is organized as follows: Section [II] presents the background knowledge required to understand this work. Section [III] motivates the building of ScalaBFS. Section [IV]
elaborates the design of our accelerator. We discuss the performance scaling issues of ScalaBFS in Section [V] and evaluate our prototype system in Section [VI]. Section [VII] concludes the paper and discusses the future works.

II. BACKGROUND AND RELATED WORKS

In this section, we will first introduce the background knowledge on the BFS algorithm and HBM technology, and then briefly discuss the related works to our paper.

A. BFS algorithm

A directed graph \( G = (V, E) \) consists of a set of a finite number of vertices \( V \), and an edge set \( E \) containing edges connecting two vertices from \( V \). The BFS algorithm computes the distances of vertices in \( V \) from a given root vertex \( r \).

Algorithm 1: BFS algorithm (push mode/pull mode).

\[\begin{align*}
\text{Input} & : \text{Directed graph } G, \text{ and root vertex } r. \\
\text{Output} & : \text{Array } Level[0..|V| - 1], \text{ distances of vertices from } r. \\
1 & \text{for } i \in [0, |V| - 1], \text{ distances of vertices from } r. \\
2 & \text{if } Level[i] = \infty; \\
3 & \text{Level}[r] \leftarrow 0; \text{ bfs_level} \leftarrow 0; \\
4 & \text{// push mode (beginning and ending iterations).} \\
5 & \text{while } \exists i \in V, \text{ such that } Level[i] = \text{bfs_level} \text{ do} \\
6 & \text{foreach vertex } i \text{ whose } Level[i] = \text{bfs_level} \text{ do} \\
7 & \text{foreach outgoing neighbor } v \text{ of } i \text{ do} \\
8 & \text{// push mode (beginning and ending iterations).} \\
9 & \text{while } \exists i \in V, \text{ such that } Level[i] = \infty \text{ do} \\
10 & \text{foreach vertex } i \text{ whose } Level[i] = \infty \text{ do} \\
11 & \text{foreach incoming neighbor } u \text{ of } i \text{ do} \\
12 & \text{// pull mode (mid-term iterations).} \\
13 & \text{while } \exists i \in V, \text{ such that } Level[i] = \text{bfs_level} \text{ do} \\
14 & \text{foreach vertex } i \text{ whose } Level[i] = \text{bfs_level} \text{ do} \\
15 & \text{bfs_level} \leftarrow \text{bfs_level} + 1; \\
\end{align*}\]

Our work considers the vertex-centric level synchronous implementation of BFS as listed in Algorithm 1. The computing is organized into multiple iterations, where each while-loop in line 4-9 or 10-15 in the listing is treated as one iteration. Regarding to the direction of message passing, there are two modes of processing: push mode and pull mode. By push mode (line 4-9), an iteration browses the level array to locate all the unvisited vertices (i.e., a vertex \( i \), whose \( Level[i] = \text{bfs_level} \) vertices, and then for each of them, visits their outgoing (child) neighbors to set their level value to the current level if they are not visited before (i.e., pushing messages to the children). In pull mode (line 10-15), an iteration browses the level array to locate all the unvisited vertices. Then for each of them, the algorithm visits their incoming (parent) neighbors, and sets its level value to the current level if one of its parents is active (i.e., pulling messages from the parents).

Generally, during the computation of the BFS algorithm, there will be small amounts of active vertices during the beginning and ending iterations, and large quantities of active vertices during the mid-term iterations. Therefore, choosing the push mode during the beginning and ending iterations, and switch to the pull mode during the mid-term iterations can help to reduce the number of memory access, and improve the performance of computation.

For a scale-free graph (degrees of vertices comply with the power-law containing millions of vertices, a push-mode (or pull-mode) iteration of BFS may contain hundreds of thousands of active (or unvisited) vertices. Although conflicts (e.g., different active vertices push level values to the same child vertex) exist, the algorithm logic of these active (or unvisited) vertices can be conducted in full parallel. The massively parallel nature of FPGAs makes them very suitable for the processing of the BFS algorithm. At the same time, the conflicts raised during computation can be comfortably solved using the on-chip memory resources (e.g., double pump BRAM used in our work) of the FPGAs. Consider the case that graph data are stored in the off-chip memory (e.g., HBM studied in this paper), which is regarded as the performance bottleneck of the system. The performance of BFS is then mainly decided by the time paid on reading the child (or parent) neighbors of the hundreds of thousands of active (or unvisited) vertices. With this regard, the throughput (not the latency) of the off-chip memory device plays a vital role in deciding the performance of BFS.

B. High Bandwidth Memory (HBM)

As a typical example, Figure 1 illustrates the HBM subsystem of Xilinx Alveo U280 [7]. The HBM subsystem contains two HBM stacks, each of which is divided into 16 pseudo channels (PCs). As each PC provides 2Gbit storage capacity, 32 HBM PCs provide 8GB (2×16×2/8) storage capacity totally.

Above the 32 PCs, there are 16 memory channels (MCs), each of which controls the accesses towards two adjacent PCs. The switch network consists of 8 4×4 mini-switches, each of which connects two adjacent MCs and exposes 4 AXI interfaces to the FPGA. Thus, the HBM subsystem of U280 exposes 32 AXI ports totally to the user logic built in the
FPGA. Every two adjacent mini-switches are connected with a bus to provide global addressing, such that a memory access towards an arbitrary PC can be issued from any AXI interface.

By conducting random (but regular memory) accessing workloads, Shuhai [11] measured the performance of the HBM subsystem of U280, and observed that: 1) A memory access to HBM suffers higher latency than that towards DDR4. 2) Although the bandwidth of a single HBM PC is smaller than DDR4, the aggregated bandwidth of HBM arrives at 425 GB/s when handling sequential accesses. As BFS is in-essence a throughput-critical workload, the aggregated bandwidth of HBM can greatly help on boosting its performance, despite its longer latency for individual memory accesses.

C. Graph data

We use Compressed Sparse Row (CSR) and its transpose, i.e., Compressed Sparse Column (CSC), to represent the graph data. The CSR consists of an offset array and an edge array, whereas the offset array stores the offsets of the outgoing (child) neighbor lists. The CSC has a similar structure as CSR, except that its edge array stores the incoming (parent) neighbor lists. The reason for ScalaBFS to use both CSR and CSC is that they facilitate the PEs to obtain both the outgoing and incoming neighbor lists of a selected vertex. Figure 2a gives an example graph and its CSR and CSC representations in Figure 2a.

D. Related Works

As an important algorithm, the computation of BFS is extensively studied in various platforms, including CPUs [12], [13], GPUs [14], [15], and FPGAs [16], [17], [18], [19], [20], [21], [8], [5], [22], [9], [23]. We briefly survey the relevant works in FPGA-based BFS accelerators below.

For a small graph that can be fully loaded in the on-chip memory of an FPGA, BFS can be conducted in it with very high performance using GraphStep [16]. However, for a large graph stored in the off-chip memory device (e.g., DRAM, HMC, or HBM studied in this paper), the key to improve the performance of BFS is to exploit the bandwidth provided by the off-chip memory devices, and at the same time, increase the parallelism of processing. With the advent of the big-data era, conducting BFS in the large graphs is of the research interest in most works.

Works in [17] and [21] use bitmaps stored in the on-chip memory devices (e.g., BRAM) of FPGAs to track the status changing of vertices, and issue writes to the level array directly to the DRAMs (according to Algorithm 1). By sufficiently using all memory channels and all logic resources of the 4 FPGAs, these two accelerators achieve the highest performance of 2.5 GTEPS on processing scale-free graphs.

The work in [3] proposes a hybrid BFS accelerator on the FPGA-CPU platform, where the CPU conducts the push-mode processing, and the FPGA executes the pull-mode processing. The work shows that choosing proper modes for different stages processing can effectively improve the performance of BFS. Recent work in [23] proposes an approach (named as Dr.BFS) that enhances the BFS performance by compressing the vertex data by using bitmaps. Dr.BFS can even achieve better performance than [3], with only push-mode processing. The methods on accelerating BFS on FPGA-HMC platform are studied in [5], [22] and [9], where the main focuses are accelerating bitmap operations conducted in BFS with HMC memory devices.

Besides the BFS accelerators studied in this paper, there are FPGA-based designs for general-purpose graph processing (i.e., supporting other graph algorithms, such as PageRank [25], besides BFS), such as ForeGraph [26] and the work in [27]. Aiming at supporting various graph algorithms, they generally adopt the edge-centric processing model to smooth the irregularity of graph processing workloads. The edge-centric processing model, however, limits their performances on BFS. For example, even after improvements on vertex caching [28], ForeGraph achieves only about 410 MTEPS on the soc-LiveJournal graph (parameters listed in Table I) according to the metrics of Graph500 by using a single DDR4 channel.

III. OPPORTUNITY AND CHALLENGE

In synchronous vertex-centric BFS algorithm [1-A], the vertices of the current level can be processed in parallel. However, the neighbor update of every vertex can have overlaps, thus need to be combined before written into level array or visited map. For example, the state-of-the-art implementation Dr. BFS [23] builds a status recombiner to combine those updates after every iteration. When the parallelism increases, the recombiner will need a longer time to process the updates due to limited external memory bandwidth, which becomes the performance bottleneck of the overall system [23]. The underlying reason is that previous FPGA boards always feature up to two DDR4 channels, providing up to 40GB/s memory bandwidth. Therefore, exploiting more computing parallelism fails to increase the overall performance and then the FPGA resources are underutilized even in a small FPGA [23]. For example, the BFS [23] utilizes 27% of the FPGA logic and Fabgraph [28] uses only 19%.

A. Opportunity from HBM-enhanced FPGAs

FPGA vendors such as Xilinx have already provided HBM-enhanced FPGA boards like U280 to provide up to 460GB/s memory bandwidth [11], which opens up new opportunity to accelerate graph processing in the context of FPGA. Therefore, HBM-enhanced FPGAs allow more computing parallelism to
fully leverage FPGA resources. However, it is not trivial to efficiently utilize HBM bandwidth in the context of BFS, which introduces random memory access.

B. Challenge when Leveraging HBM

Due to the random memory access property of BFS, we need a crossbar to globally access all the memory channels of HBM. There are two types of crossbar, which turns out to fail to satisfy the memory bandwidth requirement of our BFS engine.

A Full Xilinx AXI Interconnect. In our practice, the full Xilinx AXI Interconnect IP [29] only supports up to 16×16 AXI interconnect, which is unacceptable as U280 has 32 HBM PCs.

Xilinx’s Switch Network. We examine the effect of the built-in Xilinx’s switch network when memory accesses cross HBM channels. We employ Shuhai [11] to benchmark the performance of each AXI channel by reading data from neighboring HBM channels. Our data width is 256 bits, with the outstanding buffer size 256, and the burst length 64. Intuitively, the more number of HBM channels each AXI channel reads from, the higher pressure the switch network encounters. Figure 3 illustrates the throughput of each AXI channel that reads across 2^k neighboring HBM channels, where k = 0,1,...,5. For example, "4" in the figure legend indicates that the i^{th} (0 ≤ i ≤ 31) AXI channel in Shuhai visits 4 consecutive HBM PCs in the range of [(i/4)·4, (i/4)·4+3] in every 4 memory accesses.

We observe that reading across HBM channels significantly affects the achievable throughput of each AXI channel. For example, the case that crosses 32 HBM channels achieves less than 0.5GB/s, more than 20 times less than the case that does not cross any HBM channels. It means that globally random memory access leads to dramatically low throughput using Xilinx’s built-in switch network.

IV. SYSTEM DESIGN

In this section, we present the system design of ScalaBFS. We present the design methodology behind and the overall hardware architecture of ScalaBFS, followed by detailed hardware design of each hardware component.
In order to satisfy G1, we need to minimize 1) reference input graph from external memory M1, and 2) the on-chip memory overhead for intermediate states M2.

Satisfying M1. For an input graph, we separate its data into two types: vertex data and graph data. Vertex data refers to the level array, while graph data refers to the neighbor lists. We leverage precious on-chip memory resources (i.e., BRAMs and URAMs) to store all the vertex data, which is similar to [17] and [21]. The underlying reason behind this design choice is two-fold. First, Algorithm 1 illustrates that vertex data is frequently modified to track the status (i.e., active or visited) of vertices, and at the same time, store the result level values. On the contrary, graph data never change. Second, modern FPGAs now enjoy larger and larger on-chip memory capacity, in terms of BRAM and URAM, as FPGA technique advances. Larger on-chip memory capacity allows storing millions of vertices.

Satisfying M2. We present a new BFS algorithm to minimize intermediate state size, as listed in Algorithm 2. The key idea of the proposed algorithm is to employ three bitmaps, i.e., current frontier, next frontier and visited map, to track the statuses of vertex data during the execution of BFS. Each vertex occupies a single bit from each of these three bitmaps, which means that a vertex only consumes three bits. A bit in the current frontier indicates whether its corresponding vertex is active (1 for active, and 0 for inactive) in the current iteration. Similarly, a bit in the next frontier indicates whether its corresponding vertex will be activated in the next iteration. A bit in the visited map indicate whether the corresponding vertex is visited before (1 for visited, and 0 for un-visited). These three bitmaps are stored in double pump BRAMs, such that two operations can be conducted on them within a clock cycle.

In order to satisfy G2, ScalaBFS partitions the graph data into multiple subgraphs, and places each subgraph in an HBM PC to enforce locality of accessing (prevent the crossing shown in Figure 3). Figure 2 illustrates how to divide the vertex ID space of an example graph into two PEs: first, IDs are divided into two intervals, i.e., [0,2,4] and [1,3,5], due to the load-balancing reason. Then, the graph data are partitioned according to the partitioning results on the vertex ID space: neighbor lists of the vertices belonging to the same partition will be placed in the same subgraph as shown in Figure 2c. From the viewpoint of the adjacency matrix, our partitioning scheme partitions a graph horizontally, which is different from [23] where the input graph is partitioned vertically. The reason for this horizontal partition scheme is that it does not breakdown the neighbor lists, and longer neighbor lists mean more chances of sequential accesses towards the HBM, which helps on improving the memory bandwidth usage rates during processing.

Further, ScalaBFS employs multiple computing engines to provide massive computing parallelism, and the details are shown in the following hardware design.

Algorithm 2: BFS algorithm using three bitmaps

| Input | Directed graph G, and root vertex r. |
|-------|--------------------------------------|
| Output | Array Level[0...|V| − 1], distances of vertices from r. |

1. foreach \(i \in [0,|V| − 1]\) do
2. \(Level[i] \leftarrow \infty; \; \text{current\_frontier}[i] \leftarrow 0; \)
3. \(\text{next\_frontier}[i] \leftarrow 0; \; \text{visited\_map}[i] \leftarrow 0; \)
4. \(Level[r] \leftarrow 0; \; \text{bfs\_level} \leftarrow 0; \)
5. \(\text{current\_frontier}[r] \leftarrow 1; \; \text{visited\_map}[r] \leftarrow 1; \)

// push mode (beginning and ending iterations).

6. while \(\exists i \in V, \text{such that current\_frontier}[i] = 1\) do
7. foreach vertex \(i\) whose \(\text{current\_frontier}[i] = 1\) do
8. foreach outgoing neighbour \(v\) of \(i\) do
9. if \(\text{visited\_map}[v] == 0\) then
10. \(\text{next\_frontier}[v] \leftarrow 1; \)
11. \(\text{visited\_map}[v] \leftarrow 1; \)
12. \(\text{Level}[v] \leftarrow \text{bfs\_level} + 1; \)
13. \(\text{bfs\_level} \leftarrow \text{bfs\_level} + 1; \)
14. \(\text{swap}(\text{current\_frontier}, \text{next\_frontier}); \)

// pull mode (mid-term iterations).

15. while \(\exists i \in V, \text{such that visited\_map}[i] \neq 1\) do
16. foreach vertex \(i\) whose visited\_map\([i]\) \(\neq 1\) do
17. foreach incoming neighbour \(u\) of \(i\) do
18. if current\_frontier\([v]\) \(\neq 1\) then
19. \(\text{next\_frontier}[i] \leftarrow 1; \)
20. \(\text{visited\_map}[i] \leftarrow 1; \)
21. \(\text{Level}[i] \leftarrow \text{bfs\_level} + 1; \)
22. \(\text{bfs\_level} \leftarrow \text{bfs\_level} + 1; \)
23. \(\text{swap}(\text{current\_frontier}, \text{next\_frontier}); \)

Fig. 4: Architecture of ScalaBFS

B. Overall Hardware Architecture

According to Algorithm 2, we present the hardware architecture of ScalaBFS, which consists of multiple Processing Groups (PGs), a Scheduler, and a Vertex dispatcher. A PG consists of an HBM reader and one or more Processing Elements (PEs). The Scheduler in Figure 4 controls the processing mode (either pull or push model) of each PE, and informs its decisions to the PEs at the beginning of each iteration on the fly.

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*Discussing the case the size of vertex data is larger than the on-chip memory capacity is beyond the scope of this paper.*
Each PG is assigned exclusively to a single HBM pseudo channel (PC). The HBM reader is shared by all the PEs in a PG to issue memory requests to its corresponding HBM PC via AXI port to read the neighbor lists from HBM. Therefore, ScalaBFS has no more than 32 PGs on Xilinx Alveo U280, as its HBM subsystem has only 32 PCs (shown in Figure 1).

Each PE processes an interval of vertices of an input graph. In case of total $Q$ PEs, we divide the vertex ID space of an input graph into $Q$ non-overlapping intervals. In order to achieve load balancing between PEs, the vertex IDs are hashed before assigning to the intervals, such that the $i$-th PE is in charge of processing the vertex whose $VID$ satisfies $VID\%Q = i$. Moreover, each PE works in a hybrid (push-pull) processing mode according to the stages of BFS, to improve hardware utilization rate. The design details of a PE is shown in Subsection IV-C.

After HBM readers issue memory requests, the Vertex dispatcher gathers all responses of neighbor lists from all the PCs and then scatters the vertices in the neighbor lists to the destination PEs according to their vertex IDs (denoted as $VID$). We will present the details of these two modules in Subsection IV-D.

C. Hybrid-Mode PE

The goal of a hybrid-model PE is to allow both push and pull models within a PE. Intuitively, a PE works in the push mode in the beginning and ending iterations, and work in the pull mode during the mid-term iterations as listed in Algorithm 2. A hybrid-model PE consists of on-chip intermediate states and three execution components (i.e., stages).

Working Mechanism of Intermediate States. During a push-mode iteration, the current frontier is scanned to locate all the active vertices. And then for each active vertex, vertices in its outgoing (child) neighbor list will be checked. If a vertex in the list has not been visited before (by checking the visited map), the corresponding bit in the visited map and next frontier of the aforementioned unvisited vertex will be set, and its level value will be written back to the Level array stored in URAMs. Whereas during a pull-mode iteration, the visited map will be scanned to locate all unvisited vertices. And then for each unvisited vertex, vertices in its incoming (parent) neighbor list will be checked. If a parent vertex in the list is active (by checking the current frontier), the corresponding bits in the visited map and next frontier of the aforementioned unvisited vertex will be set, and its level value will be written back to URAMs.

Workload Preparing (P1). This stage prepares the workloads to be processed. When working in the push mode, the active vertices are first obtained from the current frontier, and then passed to the Read CSR module to read their outgoing neighbor lists from the CSR data. As the CSR data are stored in HBM, the module will pass its requests to the HBM reader. When working in the pull mode, the unvisited vertices are obtained from the visited map, and the remaining processes are the same as in the push mode except that the Read CSC module will read the CSC data for incoming neighbor lists from the HBM.

Neighbor Checking (P2). This stage accepts messages (i.e., the neighboring vertices) from the Vertex dispatcher. When working in the push mode, the messages will be the outgoing (child) neighbors of the active vertices prepared in P1. For each child vertex, the processing logic will proceed to check the visited map, and pass it to the next stage of processing (i.e., P3) if it is not visited before, or drop it if otherwise. When working in the pull mode, the messages will be the incoming (parent) neighbors of the unvisited vertices prepared by the stage of P1. For each parent vertex, the processing logic will then proceed to check the current frontier, and pass its child vertex (i.e., the unvisited vertex prepared by P1) to the next stage of processing (i.e., P3) if it (the parent vertex) is active, or drop it if otherwise.

Note that in the pull mode, the child vertex to be passed to P3 may not be in the same PE as that processing its parent, since the incoming neighbor lists in CSC contains vertices of other partitions as shown in Figure 2c. In such a case, the child vertex will be passed from one PE to another PE via a soft crossbar, which will be discussed in detail in the next subsection.

Result Writing (P3). This stage accepts result messages from P2 and conducts the modifications in the bitmaps according to Algorithm 2. In both processing modes, the results will be written to the next frontier and visited map. Besides, the results will also be written to the Level array stored in URAMs (not shown in Figure 5 for brevity).

Due to the similarities of the logic for these two processing modes, except for the soft crossbar used in P2 in the pull mode,
we use the same sets of circuits with parameters in registers to implement the similar modules, to save logic resources of the FPGA. Moreover, as the above processing stages are driven by signals (from the Scheduler) or data streams from other modules, the circuits work asynchronously in a pipelined fashion to maximize processing efficiency.

D. HBM Reader and Vertex Dispatcher

**HBM Reader.** The functionality of an HBM reader is to receive requests from the Read CSR or Read CSC, convert these requests into memory accessing AXI commands, and then issue them to its corresponding HBM PC. When PEs are now working in the push mode. A request (reading the outgoing neighbor list of an active vertex) is sent to an HBM reader, which will first assemble an AXI command to read the corresponding values in the offset array of CSR from HBM. After receiving the offset values, the HBM reader will then assemble another AXI command to read the outgoing neighbor list from the edge array. Procedures are similar in the pull mode, except that each PE will read the offsets in the CSC and incoming neighbor lists.

**Vertex Dispatcher.** The Vertex dispatcher intercepted read the neighbor lists read from the HBM. Particularly, the functionality of the Vertex dispatcher is to scrutinize the vertices in the input neighbor-list streams, classify them according to intervals that they belong to, and send them back to the corresponding PEs. The most straightforward approach that achieves such an objective is to use a full $N \times N$ crossbar where $N$ is the number of PEs (and accordingly, $N$ subgraphs). However, such a full crossbar requires $N^2$ FIFOs to implement [17], which are hard to fit within an FPGA when $N$ is sufficiently large. For example, when the length of FIFO is 16 and $N = 64$, the Vertex dispatch employs a full 64x64 crossbar that consumes more than half of the LUTs in the U280 FPGA card, leaving very limiting number of LUTs for PEs.

**Efficient Crossbar Design.** Inspired by the fact that the switching logic of our Vertex dispatcher is unidirectional (and thus simpler), we propose a multi-layer crossbar that requires much fewer FPGA resources to implement while keeping the same functionality. Our multi-layer crossbar design in ScalaBFS shares some similarities as the recent work of butterfly crossbar in [30]. The differences between our design and that in [30] are that: 1) our crossbar design supports general RTL (as ScalaBFS), while that in [30] mainly supports HLS (High Level Synthesis); 2) the focus of our crossbar design is to cope with random and irregular memory accesses, while that in [30] mainly addresses sequential memory accesses; 3) our crossbar design studies the trade-off between performance and on-chip resource consumption (explained in the following), while there is no such concern in [30].

To explain our multi-layer crossbar, we discuss a case that dispatches 16 neighbor-list streams to 16 PEs as shown in Figure 6. Figure 6a depicts the 16x16 full crossbar that contains 16 inputs and 16 output ports. The switching logic of this 16x16 full crossbar is to send a vertex to the $(VID\%16)^{th}$ port, where $VID$ denotes the vertex’s ID. Equivalently, we can convert the 16x16 full crossbar into a two-layer crossbar, which consists of two layers (input layer and output layer) and each layer consists of four 4x4 crossbar, as shown in Figure 6b. The switching logic of each 4x4 crossbar of the input layer is to send a vertex to its $(VID\%4)^{th}$ port, which connects to the $(VID\%4)^{th}$ 4x4 crossbar of the output layer. The $(i^{th})$ 4x4 crossbar of the output layer connects to the PEs such that $PE_ID\%4 = i$, where $PE_ID$ denotes the ID of a PE. By this for the output layer, the first $(0^{th})$ 4x4 crossbar connects to $PE_0$, $PE_4$, $PE_8$ and $PE_{12}$, while the second $(1^{th})$ 4x4 crossbar connects to $PE_1$, $PE_5$, $PE_9$ and $PE_{13}$, and so on. The switching logic of each 4x4 crossbar of the output layer is thus to send an incoming vertex to the $(VID\%16)^{th}$ PE (equals to the effectiveness of the 16x16 full crossbar).

To generalize our approach on converting an $N \times N$ full crossbar into a multi-layer crossbar: we need first decompose $N$ into multiple (say $k$) factors, such that $N = C_1 \times C_2 \times \ldots \times C_k$. The first (input) layer uses $N/C_1$ $C_1 \times C_1$ crossbars, and classifies the input vertices into $C_1$ groups according to $VID\%C_1$, where $VID$ denotes the ID of an input vertex. The second (relay) layer uses $N/C_2$ $C_2 \times C_2$ crossbars, and further classifies the input vertices into $C_1 \times C_2$ groups according to
VID(C1 × C2). Such a process continues till the vertices arrive at the last (output) layer, which uses N/Ck × Ck crossbars, and classifies the vertices into C1 × C2 ×...× Ck = N groups. The (N) vertex groups coming out of the last layer are finally sent to the (N) PEs, each of which is in charge of processing one vertex group (i.e., a vertex interval). Figure 6 merely illustrates a simple case where N = 16, k = 2, and C1 = C2 = 4.

We now compare these two approaches (full-crossbar vs. multi-layer crossbar) from the angles of resource consumption and efficiency. An N × N full crossbar consumes N^2 FIFOs, while the number of FIFOs required by its equivalent k-layer crossbar is (N/C1) × C1^2 + (N/C2) × C2^2 +...+ (N/Ck) × Ck^2. It is easy to prove that the number of FIFOs consumed by our k-layer crossbar is smaller than that of its equivalent N × N full crossbar, as N = C1 × C2 ×...× Ck. Consider the example in Figure 3, the 16×16 full crossbar consumes 16 × 16 = 256 FIFOs, while the two-layer crossbar consume only 2×4×4×4 = 128 FIFOs, meaning half resource consumption.

From the efficiency point of view, the N × N full-crossbar achieves 1-hop latency on message passing, while the equivalent k-layer crossbar approach requires k-hop latency for vertex dispatching. Obviously, the k-layer crossbar approach leads to higher latency than the full crossbar approach as k ≥ 2. Nevertheless, based on the observation that BFS is a throughput-critical workload as discussed in subsection II-A, it is appropriate for us to use multi-layer crossbars to trade latency for resource. In Section VI, we will use 3-layer 4×4 crossbars to replace the 64×64 full crossbar to help our accelerator to achieve the scale of 64 PEs on U280.

V. PERFORMANCE MODEL

ScalaBFS can scale its performance in two directions: 1) increasing the number of HBM PCs (thus PGs) with a fixed number of PEs in a PG, and 2) increasing the number of PEs in a PG with a fixed number of HBM PCs. The first direction of scaling is limited by the number of available HBM PCs of a given HBM subsystem, while scaling in the second direction may be limited by the amount of logic resources of an FPGA. If we regard the HBM as the slower device, and the processing circuits (PEs, HBM readers, and the Vertex dispatcher) of our accelerator works in a pipelined fashion, the performance of ScalaBFS should scale linearly along the first direction (i.e., increasing the number of HBM PCs). We study the scalability of our accelerator in the first direction empirically by experiments conducted in Section VI, and focus our discussions of this section in the second direction (i.e., increasing PEs). By a model-based study, we intend to investigate the answer to the following question: Given a fixed number of HBM PCs, how many PEs in a PG should we choose to achieve the optimal performance?

To simplify discussions, we consider a single HBM PC, on top of which a PG is constructed, and the number of PEs in the PG vary. We assume all processing units, i.e., PEs, the HBM reader, and the Vertex dispatcher, work in a pipelined fashion to mask delays in processing stages. As our PEs use double pump BRAMs as their local store on processing the bitmaps, each PE is capable of conducting two operations at each clock cycle. Therefore, when there are N_pe PEs, we configure the data width of AXI bus (denoted as DW) in Equation 1.

\[ DW = 2 \cdot N_{pe} \cdot S_v \]  \hspace{1cm} (1)

where S_v denotes the storage size of a vertex. As each neighbor list read from an HBM PC is treated as a stream of vertices, which are classified and then sent to all participating PEs by the Vertex dispatcher, assuming each PE receives the same number of vertices during processing (perfect load balancing), to feed more PEs, we need longer AXI buses.

Denote the PE’s frequency as F, the bandwidth of a single HBM PC (denoted as BW) can be computed according to Equation 2.

\[ BW = \begin{cases} \frac{DW \cdot F}{BW_{MAX}}, & DW \cdot F < BW_{MAX} \\ BW_{MAX}, & DW \cdot F \geq BW_{MAX} \end{cases} \]  \hspace{1cm} (2)

where BW_{MAX} denotes the maximum physical bandwidth of a single HBM PC. According to [11], BW_{MAX} is about 13.27GB/s. As HBM works in much higher frequency than PEs (e.g., the frequency of HBM in U280 is about 900 MHz, which is much higher than the FPGA circuits of ScalaBFS), we assume it produces a datum whose length is DW for each cycle, but at the same time, BW cannot exceed its physical limit of BW_{MAX}.

Now consider conducting a push-mode BFS iteration (pull-mode iterations exhibit similar patterns) in a given graph, a set of active vertices, each of which has a list of neighboring vertices stored in the edge array in Figure 2, is going to be processed. We assume that each active vertex has Len_{nl} neighboring vertices on average. Before retrieving the neighboring vertices, the HBM reader needs to read the offset values from the HBM. For each subgraph, assuming the length of data read from the offset array for each active vertex equals to the data width (i.e., DW), the percentage of HBM bandwidth paid on reading the neighbor lists P_{nl} can be computed using Equation 3.

\[ P_{nl} = \frac{Len_{nl} \cdot S_v}{DW + Len_{nl} \cdot S_v} \]  \hspace{1cm} (3)

Accordingly, the portion of bandwidth paid on reading the neighbor lists can be computed using Equation 4.

\[ BW_{nl} = BW \cdot P_{nl} = \begin{cases} \frac{DW \cdot F \cdot P_{nl}}{BW_{MAX} \cdot P_{nl}}, & DW \cdot F < BW_{MAX} \\ BW_{MAX} \cdot P_{nl}, & DW \cdot F \geq BW_{MAX} \end{cases} \]  \hspace{1cm} (4)

Regard each neighbor vertex as an edge connecting itself with a corresponding active vertex, by combining Equation 3 and 4, the theoretical performance of a single PG (denoted as Perf_{PG}, in number of traversed edges per second (TEPS)) can then be computed approximately in Equation 5.
Large and the performance gains are much higher for graphs with
the number of PEs can improve the performance of the accelerator,
the accelerator achieves better performance in graphs with
7, we can observe that: 1) with an equal number of PEs,
we compute and illustrate U280, our maximum number of PE is 64.

\[
\text{Perf} \approx \frac{\text{BW}_{nl}}{S_v} = \begin{cases} 
\frac{2N_{pe} \cdot F \cdot \text{Len}_{nl}}{2N_{pe} + \text{Len}_{nl}}, & 2N_{pe} \cdot S_v \cdot F < \text{BW}_{\text{MAX}} \\
\frac{2N_{pe} \cdot \text{Len}_{nl} \cdot N_{pc}}{2N_{pe} + \text{Len}_{nl}}, & 2N_{pe} \cdot S_v \cdot F \geq \text{BW}_{\text{MAX}}
\end{cases}
\]

Assuming that the vertex dispatcher is not the bottleneck
(which means adding PC/PGs can improve the performance
linearly, and our experiment can prove this), We can come up
with our overall performance Perf in Equation 6, where \(N_{pc}\)
the number of PC or PGs.

\[
\text{Perf} = \text{Perf}_{fg} \cdot N_{pc} = \begin{cases} 
\frac{2N_{pe} \cdot F \cdot \text{Len}_{nl} \cdot N_{pc}}{2N_{pe} + \text{Len}_{nl}}, & 2N_{pe} \cdot S_v \cdot F < \text{BW}_{\text{MAX}} \\
\frac{2N_{pe} \cdot \text{Len}_{nl} \cdot N_{pc}}{2N_{pe} + \text{Len}_{nl}}, & 2N_{pe} \cdot S_v \cdot F \geq \text{BW}_{\text{MAX}}
\end{cases}
\]

Also we can take the resource consumption into the consideration.
For simplicity, only LUT usage is considered. Assuming each FIFO in our \(k\) level vertex dispatcher costs \(R_{FIFO}\) LUTs, each PE costs \(R_{PE}\) LUTs, and the overall limit of LUTs is \(R_{\text{limit}}\). Then we have the constraints as inequality. Notice that \(N_{pe}\) must be power of 2 in our project.

\[
kN_{pe}^{\frac{1}{2} + 1} \cdot R_{FIFO} + N_{PE} \cdot R_{PE} < R_{\text{limit}}
\]

If we know \(R_{\text{limit}}\), then we can figure out the maximum number of PEs we can have. For example on Xilinx Alveo U280, our maximum number of PE is 64.

Let \(S_v = 32\) bits, \(F = 100MHz\) and \(\text{BW}_{\text{MAX}} = 13.27GB/s\), we compute and illustrate Perf in Figure 7. From Figure 7 we can observe that: 1) with an equal number of PEs, the accelerator achieves better performance in graphs with larger Len_{nl}, 2) for a given graph (fixed Len_{nl}), increasing the number of PEs can improve the performance of the accelerator, and the performance gains are much higher for graphs with larger Len_{nl}s. Nevertheless, there is a break-point (i.e., 16 PEs), after which the performance will degrade when the number of PEs increases.

The second observation is somewhat counter-intuitive since in the worst case, increasing the PEs should result in no detrimental effects on performance except for wasting logic resources. The underlying reason for such a phenomenon is that we configure the data width (i.e., \(DW\)) of the AXI bus according to the number of PEs. A larger number of PEs leads to larger \(DW\) according to Equation 1 which further leads to smaller \(P_{nl}\) in Equation 2 and consequently results in smaller \(BW_{nl}\) and Perf., if the HBM PC becomes saturated (i.e., the second conditions of Equation 4 and 5). Such an observation reveals the fact that when given a fixed number of HBM PCs, there exists a configuration regarding the number of PEs for ScalaBFS to achieve its upper-bound performance. We will further investigate this configuration by experiments in Section VI and verify the model of this section.

VI. System Evaluation

In this section, we will give the setups for our experiments in subsection VI-A present the resource consumption of ScalaBFS in subsection VI-B discuss hybrid-mode processing of the PEs in subsection VI-C address the scaling issues in subsection VI-D study the HBM bandwidth utilization in subsection VI-E and compare the performances of ScalaBFS with other state-of-art systems in subsection VI-F.

A. Experiment Setups

Hardware. We run our experiments in a COTS PC server, which features two Xeon Silver 4110 CPU running at 2.10GHz, and a Xilinx Alveo U280 accelerator card attached to the PC server via PCIe bus. The U280 card has an HBM subsystem (shown in Figure 1) of 8GB storage capacity. The HBM subsystem contains 32 pseudo channels, and provides a theoretical aggregated memory bandwidth up to 460GB/s. The Ultrascale+ FPGA in the U280 card contains 9.072MB BRAMs, 34.56MB URAMs and 1304K LUTs for implementing ScalaBFS. We implement ScalaBFS with Xilinx Vitis 2019.2. The host part of ScalaBFS is coded using OpenCL, and device part is programmed as an RTL kernel using Chisel language. Thanks to the productivity and flexibility (with which we can easily vary the number of PCs and PEs in ScalaBFS by simply changing the parameters) of Chisel language, the RTL kernel design of ScalaBFS consists of only about 1700 lines of Chisel code.

Workloads. We choose four real-world graphs taken from [32] and ten synthetic RMAT graphs created using the Kronecker Generator (with parameters: A=0.57, B=0.19, C=0.19) from Graph 500 [4] as listed in Table I to evaluate the performance of ScalaBFS. In the names of RMAT graphs, the first number stands for the scale (i.e., the number of vertices) of the graph, and the second number stands for the average degree (i.e., dividing number of edges by the number of vertices). For example, “RMAT18-8” represents a synthetic graph with \(2^{18} = 256K\) vertices and \(2^{18} \times 8 = 2M\) edges. For an undirected graph, we convert each of its edges (except for the loop
that connects the same vertex) into two directed edges with opposite directions.

On evaluating the performances, we use the notion of GTEPS (Giga Traversed Edges Per Second), which is computed by dividing the sum of outgoing or incoming neighbor list lengths of all visited vertices by the execution time of BFS. If an edge is “visited” more than once, it is counted only once.

### B. Resource Consumption

Table [II] lists the amounts of FPGA resources consumed by ScalaBFS in typical configurations (place and route results). When configured with 64 PEs and using all 32 PCs from HBM (i.e., the third configuration), the Vertex dispatcher of ScalaBFS uses a 3-layer crossbar, each layer of which consists of 16 4x4 crossbars. For other configurations, the Vertex dispatcher uses full crossbars.

Comparing the 16-PC/32-PE configuration with the 32-PC/32-PE configuration in Table [II] we can observe that the Vertex dispatcher of the former configuration even consumes more resources than the latter configuration. This is because the 3-layer 4x4 crossbars of the 32-PC/64-PE configuration consumes 3 (layer) × 16 (crossbars per layer) × 4 × 4 (FIFOs per crossbar) = 768 FIFOs, while the 32x32 full crossbar of the 32-PC/32-PE configuration consumes 32² = 1024 FIFOs. These numbers partially explain the differences in resource consumption of these two configurations.

From Table [II] we can observe that the PEs of ScalaBFS consume relatively small amounts of resources, even they are capable of hybrid (push-pull) mode processing. This is because the PEs reuse the circuits for push and pull modes, and the logic for memory accessing is decoupled from processing. Nevertheless, ScalaBFS stops at 64 PEs in the direction of scaling with more PEs in Table [II] since at our current stage of developing, higher numbers (e.g., 128) of PEs still lead to timing problems during the place and route phase. We will report performance results of ScalaBFS with more than 64 PEs in our future work.

### C. Hybrid-mode Processing

In this section, We leverage the 32-PC/64-PE configuration that yields the highest GTEPS to examine the effect of hybrid-model processing, compared with pull and push models, where two PEs are associated with a PC. Figure [VIII] illustrates the absolute throughput, in terms of GTEPS, of three models. We have two observations. First, the hybrid mode leads to 1.20x throughput improvement over the push (or pull) model. Second, ScalaBFS is able to achieve higher performance improvement when processing denser graphs, as the BFS processing in the hybrid mode effectively reduces the number of unnecessary memory accesses to the neighbor lists, coincident with previous works [33], [3] and [9]. For example, when processing the dense R MAT22-64 graph, ScalaBFS achieves its peak performance of 19.7 GTEPS. Therefore, we let PEs of ScalaBFS work in the hybrid mode in the following experiments.

---

### Table I: Graph datasets

| Graphs            | #Vertices (M) | #Edges (M) | Avg. Degree | Directed |
|-------------------|---------------|------------|-------------|----------|
| soc-Pokec (PK)    | 1.63          | 30.62      | 18.75       | Y        |
| soc-LiveJournal (LJ) | 4.85        | 68.99      | 14.23       | Y        |
| com-Orkut (OK)    | 3.07          | 254.37     | 76.28       | N        |
| hollywood-2009 (HO) | 1.14         | 113.89     | 99.91       | N        |

#### TABLE II: Resource Utilization of ScalaBFS with typical configurations on U280 (VD stands for Vertex dispatcher)

| #PC / #PE | \(f_{PE} / f_{BRAM}\) (MHz) | part | LUT | FF | BRAM |
|-----------|-----------------------------|------|-----|----|------|
| 16 / 32   | 90 / 180                    | total | 35.76% | 10.29% | 45.83% |
|           |                             | PGs  | 7.68%  | 0.76 %  | 35.71% |
|           |                             | VD   | 16.71% | 1.17%   | 0%    |
| 32 / 32   | 90 / 180                    | total | 39.93% | 13.22% | 46.33% |
|           |                             | PGs  | 8.97%  | 0.91%   | 35.71% |
|           |                             | VD   | 16.66% | 1.17%   | 0%    |
| 32 / 64   | 90 / 180                    | total | 42.08% | 13.52% | 48.21% |
|           |                             | PGs  | 14.31% | 1.50%   | 38.10% |
|           |                             | VD   | 13.40% | 1.39%   | 0%    |
D. Performance Scaling

For ScalaBFS, there are two scaling directions: increasing HBM PCs and increasing PEs. We first study the performance scaling of ScalaBFS by increasing the number of HBM PCs, and then study the performance scaling by increasing the number of PEs.

Effect of HBM PC. We examine the effect of HBM PC with the configuration of a single PE for each PG (thus on each HBM PC). Figure 9 illustrates the throughput improvement with a increasing number of HBM PCs. We observe that ScalaBFS achieves almost linear speedup with respect to the number of HBM PCs, indicating that more the decoupled design of ScaleBFS that allows decoupling memory accessing from processing leads to high efficiency and effectiveness when performing BFS.

Effect of PE. We examine the effect of PE within a PG (i.e., on a HBM PC). Since a single HBM PC provides only 2 Gbits storage capacity that limits the size of the graph data, we use small synthetic graphs with a scale of $2^{18}$ vertices, as illustrated in Figure 10. We observe that more PEs lead to higher performance of ScalaBFS, especially when the vertices of the input graph have higher average degrees.

However, the performance scaling stops at specific break-points. For example, the performances for the RMAT18-8 and RMAT18-16 graph stop at 4 PEs, that for the RMAT18-32 graph stops at 8PES. Comparing Figure 10 and Figure 7 we can observe that the trends are similar, except that the break-points show up earlier for graphs whose vertices have smaller numbers of neighboring vertices in real systems than in theory. This is because in the theoretical study in Section 7 we assume the load-balancing status is perfect, i.e., the Vertex dispatcher evenly distributes vertices among the PEs. Nevertheless, such an assumption may be compromised by the structure of the input graphs in real systems. Whereas, experimental results from Figure 10 still suggests that the optimal configuration on the number of PEs configured to each HBM PC in ScalaBFS is about 4 to 8 for sparse graphs, and it is about 8 to 16 for dense graphs. By this observation, our 32-PC/64-PE configuration listed in Table 7 has not fully exploited the HBM subsystem of U280, since each HBM PC is configured with only two PEs in such configuration. Deductively, we should configure about 128 (32x4) PEs or 512 (32x16) PEs for ScalaBFS to achieve the optimal performance in the sparse or dense graph respectively on U280.

Comparing Figure 10 with Figure 9 we can observe that the performance gain from increasing the number of PEs is much less than from increasing the number of HBM PCs. For example, increasing the number of PEs from one to two or one to four leads to about 1.68x or 2.48x speedup, even on the (dense) RMAT18-64 graph. Such an observation suggests that ScalaBFS should prioritize the scaling in the direction of using more HBM PCs, rather than increasing the number of PEs, especially when the amount of FPGA logic resources is limited. It is also the reason why the 32-PC/64-PE configuration of ScalaBFS can achieve the best performance so far on U280.

E. HBM Bandwidth Utilization

We measure the aggregated bandwidth (summation of bandwidths of 32 HBM PCs and 64 PEs) and baseline case. For ScalaBFS where the edge data of an input graph are partitioned (shown in Figure 2d) to evenly distributed to all HBM PCs, in the baseline case, the edge data are not partitioned (shown in Figure 2b), and placed in the HBM PCs sequentially (starting from PC0). For the data distribution, the HBM readers of the PGs in ScalaBFS only need to access its corresponding PC, while an HBM reader in the baseline case have to cross (possibly) multiple PCs to access the adjacency lists of the vertices assigned to its PG.
Figure [11] reports the aggregated bandwidths of HBM, as well as the performances of both ScalaBFS and the baseline case, when both systems are employed to process the same graphs. From Figure [11] we can observe that the baseline cases poorly use the HBM (small aggregated bandwidths) and consequently produce poor performances on BFS. The reasons for the small aggregated bandwidths in these baseline cases are that: 1) the PGS have to read the required edge data from remote PCs during computation, which places pressure on the switch network of HBM in Figure [1] and further leads to poor bandwidths as in Figure [3]. 2) the edge data of our chosen graphs are relatively small, and are thus stored in the PCs with small suffixes. During execution, such data placement scheme leads to unbalanced accesses and further limits the achievable bandwidths of HBM.

Compared with the baseline cases, ScalaBFS achieves much higher aggregated bandwidths by evenly distributing the edge data in HBM PCs, and at the same time, confining the PGS to access their corresponding PCs. From Figure [11] we can observe that the maximal achieved bandwidth is about 46GB/s. Since the RTL of ScalaBFS runs at 90MHz, the burst length is 128bits (2 PEs to each PC), the theoretical upper-bound aggregated bandwidth is about: 90MHz × 128/8 Byte × 32 PCs ≈ 46.08GB/s (i.e., the measured bandwidth is close to the upper-bound in theory). Nevertheless, such bandwidth is still much smaller than the theoretical bandwidth (up to 460GB/s) of HBM in U280. The reasons are that: 1) the access pattern of BFS is random and irregular, which limits the achievable bandwidths of each HBM PC using DRAM; 2) the relatively low clock frequency (i.e., 90MHz) limits the maximum achievable bandwidth as computed above.

F. Comparison with Other Existing Systems

Compared with Other FPGA-based Systems. In the existing works regarding FPGA-based BFS accelerators, [18] and [19] achieve 2.5 GTEPS by using 16xDDR2 on the Convey machines and Dr. BFS [23] that achieves about 470 MTEPS by using 2xDDR4, ScalaBFS achieves its peak performance of 19.7 GTEPS and yields about 7.9x over [18] and [19], since ScalaBFS exploits HBM’s high memory bandwidth and massive FPGA resources for PE-level parallelism. As different accelerators use different FPGA platforms with different numbers of DRAM channels, to be fair, Figure [12] compares the BFS performance of ScalaBFS and other similar systems using a single DRAM channel. From Figure [12] we can observe that ScalaBFS is much faster than existing systems even in the context of single memory channel performance, which further explains the high BFS performance speedups over existing systems.

Note that the performance of ScalaBFS on U280 is still far from the theoretical performance of 45.8 GTEPS [9] on bitmap operations (key operations of BFS) using the HMC device that supports the processing-in-memory (PIM) technology. Nevertheless, we should notice that the above experiments are conducted on the real FPGA board U280, which limits the performance of ScalaBFS with its fixed amount of physical resources, e.g., the number of HBM PCs and LUTs. We believe with the technology progresses, ScalaBFS will continuously achieve higher performance on future FPGA cards, that feature more HBM stacks and more logic resources, with its scalability.

Compared with GPU-based Systems. We further compare the performances of ScalaBFS on U280 with those of Gunrock [15], which is a popular accelerator for graph processing on GPUs, running on Nvidia V100 GPU (model SXM2, configured with 640 tensor cores and 5120 CUDA cores running at 1.53 GHz, 4 HBM2 stacks (totally 64 PCs, 16 GB storage space), consuming 300 watts [34]), when conducting BFS in real-world graphs in Table III. Gunrock also adopts the hybrid processing mode as in ScalaBFS when conducting BFS. We fine-tune the parameters of Gunrock during the experiments such that Gunrock achieves its best performance on V100.

From Table III we can observe that for sparse real-world graphs (i.e., PK and LJ) whose vertices have short neighbor lists, the performances of ScalaBFS are very close to those of Gunrock. This is because, when conducting BFS in these sparse graphs, the memory accesses towards the HBM are of smaller burst lengths, which makes the HBM to be the bottleneck of the system. ScalaBFS uses Algorithm 2 where the bitmaps stored in the BRAM absorb large amount of memory accesses to conduct BFS, and thus achieves equivalent performances by using only 32 HBM PCs to those achieved in Gunrock using 64 HBM PCs. Moreover, the power efficiencies of ScalaBFS on U280 are about 5.68 x 10.19x better than those of Gunrock on V100, due to the low power consumption of U280. We read the on-board power meter by using the Xilinx Board Utility (xbutil) [35], which reports 32 watts during the processing of all graphs in Table III.

From Table III we can also observe that for dense real-world graphs (i.e., OR and HO) whose vertices have long
neighbor lists, the performances of ScalaBFS are only about 0.13–0.22x of the performances of Gunrock. The reason is that the dense graphs lead to memory accesses with much larger burst lengths during processing, which makes the processing elements to be the real bottlenecks of the system. To this end, Gunrock enjoys the huge memory bandwidth provided by the 64 PCBs of the V100’s HBM and takes advantage of the large number of high-frequency hardware cores of the V100 to win the battle. Such a performance disadvantage of ScalaBFS also suggests that when conducting BFS in dense graphs, we need to build enough processing elements in an FPGA-based BFS accelerator to achieve comparable or even higher performance than GPUs.

VII. CONCLUSIONS AND FUTURE WORKS

In this paper, we propose ScalaBFS, an open-source BFS accelerator built on the FPGA-HBM platform. ScalaBFS features hybrid-mode processing elements that sufficiently exploit the memory bandwidth of HBM, and decoupled circuits for processing and memory accessing that scales its performance with the increasing HBM PCBs. By fully using the 32 HBM pseudo channels (PCs), the performance of ScalaBFS arrives at 19.7 GTEPS when conducting BFS in real-world and synthetic scale-free graphs on Xilinx Alveo U280 Data Center Accelerator card. The future works of ScalaBFS include further fine-tuning of the system, supporting more processing elements on U280, processing larger graphs, and extending itself to a general graph-processing framework that is capable of conducting other graph algorithms.