HEAM: High-Efficiency Approximate Multiplier Optimization for Deep Neural Networks

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Abstract—We propose an optimization method for the automatic design of approximate multipliers, which minimizes the average error according to the operand distributions. Our multiplier achieves up to 50.24% higher accuracy than the best reproduced approximate multiplier in DNNs, with 15.76% smaller area, 25.05% less power consumption, and 3.50% shorter delay. Compared with an exact multiplier, our multiplier reduces the area, power consumption, and delay by 44.94%, 47.63%, and 16.78%, respectively, with negligible accuracy losses. The tested DNN accelerator modules with our multiplier obtain up to 18.70% smaller area and 9.99% less power consumption than the original modules.

Index Terms—approximate computing, application-specific design, neural network accelerator

I. INTRODUCTION

Deep Neural Networks (DNNs) achieve tremendous success over recent years in artificial intelligence applications. Due to the large quantities of parameters, computing DNNs requires huge numbers of multiplication operations. In neural network accelerators, approximate multipliers are promising substitutes for exact multipliers, which can make a tradeoff between precision and hardware cost. To take advantage of this feature, we explore approximate multiplier design methodology to reduce the hardware costs of DNN accelerators.

Various works show that approximate multipliers can effectively reduce the area and power consumption with small precision loss. Most approximate multipliers are designed by adopting novel approximate blocks. In [1], the Karnaugh map of an exact $2 \times 2$ multiplier is modified to form a basic approximate block. Larger multipliers are constructed by stacking $2 \times 2$ blocks. Reference [2] designs an approximate multiplier by simplifying the partial product accumulation block with limited carry propagation. Mathematical approximation methods are used to design approximate multipliers as well. Mitchell approximation is adopted to design an iterative logarithmic multiplier [3]. In [4], an approximate hybrid radix encoding is proposed for the generation of approximate multipliers.

Recent studies have explored approximate computing for DNNs, such as [5], [6], and [7]. An approximate multiplier generated by Cartesian Genetic Programming (CGP) is applied to neural networks in [5]. Multiplier-less Artificial Neuron (MAN) [8] uses a novel Alphabet Set Multiplier which utilizes a pre-computer bank and an alphabet selection procedure to reduce the computational cost and accuracy loss in neural networks. Reference [7] designs an optimization scheme to build a floating-point approximate multiplier, which is optimal with the given bases.

The approximate multipliers for DNNs above rely on optimization procedures to ensure low accuracy loss. These optimization methods have an implicit assumption that the operands are uniformly distributed in the given space. Nevertheless, according to studies on the weight analysis of neural networks such as [9], the weight distributions are typically not uniform. Similarly, our experiment shows that the weights of quantized DNNs are concentrated around certain points. Reference [10] considers the weight distributions of DNNs and optimizes an approximate multiplier with CGP. However, the probability distributions of the activations are ignored, which leads to the biased estimation of the DNN computation. In the proposed method, the probability distributions of both operands are utilized to reduce the errors of multiplications on frequently-occurring operands. Furthermore, the CGP-based and MAN-multiplier-based methods require complicated DNN retraining to ensure low accuracy loss, while the proposed method does not need retraining. In addition, a precision controller is designed in [11] to obtain low accuracy loss. However, it limits the reduction of hardware cost.

We propose an application-specific optimization method which can generate a High-Efficiency Approximate Multiplier (HEAM). We design an approximate multiplier for DNNs with the proposed method, achieving small area, high power efficiency, short delay, and negligible accuracy loss.

The rest of this paper is organized as follows. In Section II, we describe our probability-based optimization method and the optimized approximate multiplier for DNNs. In Section III, we compare various multipliers in terms of hardware cost, evaluate the accuracies of the DNNs with the multipliers, and show the comparison of the DNN accelerator modules integrated with the multipliers. The last section is the conclusion.

II. APPROXIMATE MULTIPLIER OPTIMIZATION METHOD

A. Problem Formulation

An approximate multiplication can be decomposed into the weighted sum of the outputs of several basic operations. We...
use $\theta = [\theta_0, \theta_1, ..., \theta_{K-1}]$ to denote a weight vector with $K$ scalar elements. The approximate multiplication can be formulated as:

$$f(x, y|\theta) = \sum_{i=0}^{K-1} \theta_i L_i(x, y)$$  \hspace{1cm} (1)$$

where $L_i(x, y)$ is the output of a basic operation. We elaborate on the construction of $L_i(x, y)$ in Session II-B. For operands $x$ and $y$, we follow (7) to define the error of $f(x, y|\theta)$ as:

$$D(x, y|\theta) = (xy - f(x, y|\theta))^2$$  \hspace{1cm} (2)$$

In applications that are based on quantized numbers, $x$ and $y$ are discrete variables with finite values. Therefore, the average error of an integer approximate multiplier can be defined as:

$$E_d(X_d, Y_d, \theta) = \sum_{i=0}^{N-1} \sum_{j=0}^{M-1} D(x_i, y_j|\theta)p(x_i, y_j)$$  \hspace{1cm} (3)$$

where $x \in X_d$, $y \in Y_d$, $X_d = \{x_0, x_1, ..., x_{N-1}\}$, and $Y_d = \{y_0, y_1, ..., y_{M-1}\}$. The constants $N$ and $M$ are the numbers of possible values of $x$ and $y$, respectively. Notation $p(x_i, y_j)$ represents the probability that $x = x_i$ and $y = y_j$. $E_d(X_d, Y_d, \theta)$ is the expectation of errors in the applications where $x$ and $y$ are subject to $p(x, y)$. We can reduce the computational errors by minimizing $E_d(X_d, Y_d, \theta)$.

B. Optimization Method Details

The proposed method focuses on partial product reduction to obtain an approximate multiplier with low hardware cost. Based on this idea, we use logic operations to compress the partial products of a multiplier. Fig. 1 illustrates an example of how the partial products of an unsigned 4×4 multiplier are compressed by logic operations. In Fig. 1(a) each element in the shape of a square or circle represents a bit and each row of elements is a partial product. Each element with an operator symbol inside in Fig. 1(b) represents a compressed term generated by the corresponding logic operation on the bits represented by the same color and shape in Fig. 1(a). We use the symbols $\&$, $|$ and $\oplus$ to denote AND, OR, and XOR operations, respectively. The elements above the blue line constitute the partial product bit-matrix of the multiplier, where each row of the compressed terms forms a compressed partial product. The output of the 4×4 approximate multiplier is obtained by minimizing (5) with MATLAB Mixed Integer Genetic Algorithm.

\begin{equation}
\min_{\theta} \left( \sum_{i=0}^{N-1} \sum_{j=0}^{M-1} (x_i y_j - f(x_i, y_j|\theta))^2 p(x_i, y_j) + R(\theta) \right)
\end{equation}

In this paper, the approximate multipliers are obtained by minimizing (5) with MATLAB Mixed Integer Genetic Algorithm.

C. The Generated Multiplier for DNNs

We follow a widely-used quantization scheme [12] to train and evaluate DNNs with 8-bit integers in all experiments. The first four partial products of an 8×8 multiplier are compressed in the optimization procedure as shown in Fig. 2(a). To obtain an approximate multiplier for DNNs, we analyze a quantized LeNet [13] trained on MNIST dataset and get the probability distributions of the inputs and weights of all layers.
As examples of operand distributions, the histograms of the inputs and weights of its first fully-connected layer (FC1) are shown in Fig. 3(a) and Fig. 3(b) respectively. The inputs and weights are concentrated around 0 and 128, respectively.

The structure of the optimized multiplier is presented in Fig. 2(b). The size of the partial product bit-matrix is significantly reduced with negligible accuracy losses.

D. Evaluation Toolbox

We implement a toolbox named ApproxFlow to evaluate the DNN accuracy with approximate multiplication. In ApproxFlow, each approximate multiplier is described by a look-up table. A DNN is represented by a directional acyclic graph (DAG), where each vertex denotes a DNN layer and the edges indicate the data flow. When a vertex in the DAG is executed, its dependencies will be executed automatically. We decouple ApproxFlow from specific DNN toolboxes, unlike TFApprox [14] and ProxSim [15] which are based on Tensorflow [16].

III. EXPERIMENTS

A. Comparison of Approximate Multipliers

In this section, we compare our multiplier with several reproduced 8×8 approximate multipliers from recent works, including KMap [1], Configurable-Recovery (CR) [2], Approximate-Compressor (AC) [20], Optimal-Unbiased (OU) [7], and SDLC [21] multipliers. We reproduce two CR multipliers with 6-bit (C.6) and 7-bit (C.7) error recovery units. Two OU multipliers are implemented with level-1 (L.1) and level-3 (L.3) structures. Note that we implement OU multipliers by applying the optimization method in [7] to 8×8 integer multipliers to provide a fair comparison with others. In addition to the approximate multipliers, we use the standard multiplier synthesized by Synopsys Design Compiler (DC) 2016 as the exact multiplier for comparison. A Wallace Tree multiplier [22] is also implemented. The multipliers are evaluated with the following metrics: (1) The areas and power consumptions at fixed frequencies. (2) The minimum critical-path delays of the multipliers. (3) The LeNet accuracies on MNIST dataset.

To evaluate the multipliers, we implement them in Verilog, and synthesize the circuits in DC with Arizona State Predictive PDK (ASAP) 7nm process libraries [23]. The areas, power consumptions, and delays are obtained from DC. Fig. 4 presents the comparison of areas and power consumptions among the multipliers, where HEAM shows its competitive hardware efficiency. Some data are absent because the corresponding multipliers fail to meet the timing constraints. In Table I, we compare the hardware costs and DNN accuracies on MNIST dataset of the multipliers. The areas and power consumptions presented in Table I are obtained at 3GHz.

As shown in Table I, HEAM achieves the best accuracy among the approximate multipliers. Compared with KMap, HEAM has 15.76% smaller area, 25.05% less power consumption, 3.50% shorter delay, and 1.01% higher accuracy. Furthermore, HEAM attains 44.94% smaller area, 47.63% less power consumption, and 16.78% shorter delay than the exact multiplier with negligible accuracy loss. In terms of hardware cost, HEAM has slightly larger area than SDLC and higher power consumption than AC, but SDLC and AC suffer from nonnegligible accuracy loss. In conclusion, HEAM can achieve the highest accuracy among the tested approximate multipliers with small area and low power consumption.
TABLE I
COMPARISON OF THE HARDWARE COSTS AND ACCURACIES OF THE MULTIPLIERS ON MNIST DATASET

| Metric             | HEAM   | KMap   | CR (C.6) | CR (C.7) | AC    | OU (L.1) | OU (L.3) | SDLC   | Exact | Wallace |
|--------------------|--------|--------|----------|----------|-------|----------|----------|--------|-------|---------|
| Area@3GHz (µm²)   | 17.53  | 20.81  | 21.26    | 24.41    | 17.98 | 24.90    | -        | 16.13  | 31.84 | 42.98   |
| Power@3GHz (mW)   | 76.20  | 101.67 | 77.15    | 89.38    | 68.44 | 89.51    | -        | 86.55  | 145.49| 151.94  |
| Delay (ps)        | 247.94 | 256.94 | 226.98   | 239.88   | 227.90| 244.91   | 463.96   | 225.00 | 297.93| 278.99  |
| LeNet Accuracy (%)| 99.34  | 98.33  | 57.20    | 95.60    | 21.14 | 10.32    | 95.70    | 95.51  | 99.40 | 99.40   |

TABLE II
COMPARISON OF THE ACCURACIES ON FASHIONMNIST, CIFAR-10, AND CORA DATASET (%)

| Dataset          | HEAM   | KMap   | CR (C.6) | CR (C.7) | AC    | OU (L.1) | OU (L.3) | SDLC   | Exact | Wallace |
|------------------|--------|--------|----------|----------|-------|----------|----------|--------|-------|---------|
| FashionMNIST     | 91.01  | 81.66  | 20.88    | 78.34    | 17.53 | 15.16    | 49.95    | 75.89  | 91.26 | 91.26   |
| CIFAR-10         | 88.39  | 38.15  | 10.00    | 10.00    | 10.01 | 61.46    | 10.00    | 88.47  | 88.47 |         |
| CORA             | 80.24  | 79.58  | 76.4     | 79.39    | 70.94 | 15.44    | 30.21    | 78.80  | 80.24 | 80.24   |

TABLE III
COMPARISON OF DNN ACCELERATOR MODULES WITH THE APPROXIMATE MULTIPLIERS

| Module | Metric             | HEAM   | KMap   | CR (C.6) | CR (C.7) | AC    | OU (L.1) | OU (L.3) | SDLC   | Exact | Wallace |
|--------|--------------------|--------|--------|----------|----------|-------|----------|----------|--------|-------|---------|
| TASU   | Area@1.5GHz (µm²)  | 84726.74| 90209.57| 90568.82 | 91023.57 | 87283.42| 88737.03 | 86294.51| 90011.99| 98573.89|
|        | Power@1.5GHz (mW)  | 151.37 | 157.60 | 150.57   | 158.49   | 156.63 | 154.27   | 157.28   | 157.57 | 158.17 |         |
| SC     | Area@2.5GHz (µm²)  | 3462.40| 3709.50| 3698.00  | 3683.87  | 3581.05| 3546.40  | 3569.24  | 4258.61| 4831.81|
|        | Power@2.5GHz (mW)  | 17.06  | 17.84  | 17.89    | 17.76    | 17.60  | 16.76    | 17.75    | 18.57  | 18.26  |         |
| SA     | Area@2GHz (µm²)    | 25598.38| -      | 24473.36 | 24858.45| 22839.51| -        | 22105.41| 24926.97| -      |
|        | Power@2GHz (mW)    | 74.76  | -      | 82.38    | 82.50    | 81.52  | -        | 81.56    | 83.06  | -      |         |

B. Accuracy Comparison on Different Datasets

In addition to MNIST, we carry out an experiment on FashionMNIST [24] with LeNet structure and CIFAR-10 [25] with AlexNet [26] structure. Moreover, the multipliers are evaluated in a two-layer graph convolutional network (GCN) on CORA dataset [27]. We use the multiplier generated from the LeNet on MNIST dataset in this experiment rather than design a multiplier for each dataset.

Table I presents the accuracies of the neural networks with the multipliers. HEAM achieves the highest accuracies among the approximate multipliers, obtaining 9.35%, 50.24%, and 0.66% higher accuracies than KMap on FashionMNIST, CIFAR-10, and CORA datasets, respectively. KMap surpasses other approximate multipliers except HEAM on MNIST, FashionMNIST, and CORA datasets. Although OU (L.3) has better accuracy than KMap on CIFAR-10 dataset, it suffers from large hardware cost as shown in Fig. 4. Thus, KMap can be regarded as the best reproduced approximate multiplier. The experiment on these datasets further proves that the proposed optimization method can obtain negligible accuracy loss.

C. Comparison of DNN Accelerator Modules with Approximate Multipliers

In this experiment, we compare the multipliers by applying them to several DNN accelerator modules. TASU [17] is a DNN accelerator for DoReFa-Net [25]. We synthesize its processing block for the first convolution layer on DC to compare the multipliers. We also reproduce Systolic Cube (SC) [13], an efficient acceleration module for the convolution operations in DNNs. Systolic Array (SA) is a popular accelerator module adopted by Google Tensor Processing Unit (TPU) [19]. We implement a 16×16 SA in our experiment as well.

Table II presents the comparison of the accelerator modules with the multipliers on 7nm, showing their areas and power consumptions at fixed frequencies. Some results are not shown in the table because the corresponding modules fail to meet the timing constraints. Due to the space limit, we do not show the results of OU (L.3), whose hardware cost is obviously higher than others as shown in Fig. 4. HEAM attains the lowest areas and power consumptions in the TASUs and obtains competitive hardware costs in other modules. The modules with HEAM obtain up to 6.66% smaller area and 4.43% less power consumption than the modules with KMap. Moreover, the modules with HEAM achieve up to 18.70% area reduction and 9.99% power saving compared to the modules with the exact multiplier. This experiment indicates that HEAM can effectively reduce the hardware cost of DNN accelerators.

IV. Conclusion

We propose an optimization method to design a high-efficiency approximate multiplier, which minimizes the average error according to the probability distributions of operands in the target application. The generated approximate multiplier can achieve negligible accuracy loss with small area, low power consumption, and short delay. Our multiplier and ApproxFlow are available at https://github.com/FDU-ME-ARC/HEAM and https://github.com/FDU-ME-ARC/ApproxFlow.
REFERENCES

[1] P. Kulkarni, P. Gupta, and M. Ercegovac, “Trading accuracy for power with an underdesigned multiplier architecture,” in International Conference on Very Large Scale Integration (VLSI Design), 2011, pp. 346–351.

[2] C. Liu, J. Han, and F. Lombardi, “A low-power, high-performance approximate multiplier with configurable partial error recovery,” in Design, Automation and Test in Europe Conference (DATE), 2014, pp. 1–4.

[3] S. E. Ahmed, S. Kadam, and M. B. Srinivas, “An iterative logarithmic multiplier with improved precision,” in IEEE Symposium on Computer Arithmetic (ARITH), 2016, pp. 104–111.

[4] V. Leon, G. Zervakis, D. Soudris, and K. Pekmestzi, “Approximate hybrid high radix encoding for energy-efficient inexact multipliers,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 26, no. 3, pp. 421–430, 2018.

[5] V. Mrazek, S. S. Sarwar, L. Sekanina, Z. Vasiczek, and K. Roy, “Design of power-efficient approximate multipliers for approximate artificial neural networks,” in International Conference on Computer-Aided Design (ICCAD), 2016.

[6] V. Mrazek, Z. Vasiczek, L. Sekanina, M. A. Hanif, and M. Shafique, “ALWANN: Automatic layer-wise approximate deep neural network accelerators without retraining,” in International Conference on Computer-Aided Design (ICCAD), 2019, pp. 1–8.

[7] C. Chen, S. Yang, W. Qian, M. Imani, X. Yin, and C. Zhuo, “Optimaly approximated and unbiased floating-point multiplier with runtime configurability,” in International Conference on Computer-Aided Design (ICCAD), 2020, pp. 1–9.

[8] S. S. Sarwar, S. Venkataramani, A. Ankit, A. Raghunathan, and K. Roy, “Energy-efficient neural computing with approximate multipliers,” Journal on Emerging Technologies in Computing Systems, vol. 14, no. 2, Jul. 2018.

[9] I. Bellido and E. Fiesler, “Do backpropagation trained neural networks have normal weight distributions?” in International Conference on Artificial Neural Networks, 1993, pp. 772–775.

[10] Z. Vasiczek, V. Mrazek, and L. Sekanina, “Automated circuit method driven by data distribution,” in Design, Automation and Test in Europe Conference (DATE), 2019, pp. 96–101.

[11] I. Hammad, L. Li, K. El-Sankary, and W. M. Snelgrove, “CNN inference using a preprocessing precision controller and approximate multipliers with various precisions,” IEEE Access, vol. 9, pp. 7220–7232, 2021.

[12] B. Jacob, S. Kligys, B. Chen et al., “Quantization and training of neural networks for efficient integer-arithmetic-only inference,” in IEEE Conference on Computer Vision and Pattern Recognition (CVPR), June 2018.

[13] Y. Lecun, L. Bottou, Y. Bengio, and P. Haffner, “Gradient-based learning applied to document recognition,” Proceedings of IEEE, vol. 86, pp. 2278–2324, Dec. 1998.

[14] F. Vaverka, V. Mrazek, Z. Vasiczek, L. Sekanina, M. A. Hanif, and M. Shafique, “TFApprox: Towards a fast emulation of DNN approximate hardware accelerators on GPU,” in Design, Automation and Test in Europe Conference (DATE), 2020.

[15] C. De la Parra, A. Guntoro, and A. Kumar, “Proxim: Gpu-based simulation framework for cross-layer approximate DNN optimization,” in Design, Automation and Test in Europe Conference (DATE), 2020, pp. 1193–1198.

[16] M. Abadi, A. Agarwal, and P. B. et al., “TensorFlow: Large-scale machine learning on heterogeneous systems,” 2015, software available from tensorflow.org. [Online]. Available: https://www.tensorflow.org/

[17] L. Jiao, C. Luo, W. Cao, X. Zhou, and L. Wang, “Accelerating low bit-width convolutional neural networks with embedded FPGA,” in International Conference on Field Programmable Logic and Applications (FPL), 2017, pp. 1–4.

[18] Y. Wang, Y. Wang, H. Li, C. Shi, and X. Li, “Systolic cube: A spatial 3D CNN accelerator architecture for low power video analysis,” in Design Automation Conference (DAC), 2019, pp. 1–6.

[19] N. Jouppi, C. Young, N. Patil, and D. Patterson, “Motivation for and evaluation of the first tensor processing unit,” IEEE Micro, vol. 38, no. 3, pp. 10–19, 2018.

[20] A. Momeni, J. Han, P. Montuschi, and F. Lombardi, “Design and analysis of approximate compressors for multiplication,” IEEE Transactions on Computers, vol. 64, no. 4, pp. 984–994, 2015.