Spin switches for compact implementation of neuron and synapse

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Abstract:
Nanomagnets driven by spin currents provide a natural implementation for a neuron and a synapse: currents allow convenient summation of multiple inputs, while the magnet provides the threshold function. The objective of this paper is to explore the possibility of a hardware neural network (HNN) implementation using a spin switch (SS) as its basic building block. SS is a recently proposed device based on established technology with a transistor-like gain and input-output isolation. This allows neural networks to be constructed with purely passive interconnections without intervening clocks or amplifiers. The weights for the neural network are conveniently adjusted through analog voltages that can be stored in a non-volatile manner in an underlying CMOS layer using a floating gate low dropout voltage regulator. The operation of a multi-layer SS neural network designed for character recognition is demonstrated using a standard simulation model based on coupled Landau-Lifshitz-Gilbert (LLG) equations, one for each magnet in the network.

The standard building block\textsuperscript{1} for neural networks (Fig.1a) consists of 1) a synapse that multiplies a number of input signals $x_i$ with appropriate weights $w_i$ and 2) a neuron that sums all the weighted inputs together with a fixed bias $b$ to produce an output $y$ determined by some nonlinear function “$f$”

$$y = f\left(\sum w_i x_i + b\right) \quad (1)$$

It is well established that multilayer neural networks obtained by interconnecting building blocks of this form can be designed to implement useful functions and powerful algorithms have been developed for choosing the weights $w_i$ and the bias $b_i$ so as to implement a desired overall input-output functionality.

Most neural networks are usually implemented through software although it is recognized that hardware implementations could potentially\textsuperscript{2,3} lead to significant speed, power improvements and massively parallel computation \textsuperscript{4}. Different proposals based on spin torque devices, domain wall motions and memristors were previously proposed to implement neurons or/and synapses \textsuperscript{5-8}. The objective of this paper is to demonstrate the feasibility of implementing a hardware neural network (HNN) using a spin switch (SS)\textsuperscript{9} as the basic building block, by presenting a concrete implementation of a SS neural network for character recognition and establishing its operation through direct simulation using experimentally benchmarked models for SS devices. SS has a gain that gives it a transistor-like character allowing multiple units to be interconnected without intervening CMOS circuitry for clocks or amplifiers: one spin switch can directly drive the next one like ordinary transistors.

Fig. 1b shows a schematic representation and detailed structure of a building block implemented with a spin switch. It consists of a Write (W) unit and a Read (R) unit with free magnetic layers $x_i$, $x_i'$ or $(y, y')$ that are dipole coupled ensuring that the two are always anti-parallel $x_i = -x_i'$. This configuration allows information to propagate from the Write unit to the Read unit of a spin switch while maintaining their electrical isolation. As we will see, the Write unit functions as a neuron which performs the summation and threshold function.

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function $f$ while the Read unit functions as a synapse which provides the weighted output $w_i x_i$.

The Read unit consists of one MTJ whose conductance is $G_i = g_i / (1 + P_i \tilde{r} \tilde{h}) = g_i / (1 + P_i \tilde{h})$ where $P_i = (G_p - G_{AP}) / g_i$; $g_i = G_p + G_{AP}$; $\tilde{r}$ (or $\tilde{h}$) is the magnetization of fixed magnet and $\tilde{h}$ (or $\tilde{r}$) is the magnetization of free magnet.

The Write unit consists of a giant spin Hall effect (GSHE) metal like Ta$^{10}$ or tungsten$^{11}$ and a free magnet $\tilde{h}$ which generates a spin current $I_s$ when driven by a charge current $I_{in}$: $I_s = \beta I_{in}$, $\beta = \theta_{SH}(A_s/A)$ and $\theta_{SH}$ being the spin-Hall angle. $A_s$ and $A$ are the cross-sectional areas for the spin and charge currents respectively.

The Read unit functions as a synapse whose output current is weighted by $-V_i G_i$ while the Write unit functions as a neuron (see Fig. 1b): it sums weighted inputs from the R units of many spin switches labeled $1, \ldots, i, \ldots, n$ giving rise to a net current

$$I_{in} = \sum_i V_i G_i (\tilde{h}) + I_b,$$

where $G_{total} = \sum_i G_i$ \hfill (2)

($r$: resistance of the GSHE metal) and performs a hysteretic threshold function $f$ of the form sketched in the figure to produce the output:

$$y = f (I_{in}) = f \left( \sum_i \frac{V_i g_i}{2(1 + G_{total} r)} (1 - P_i \tilde{h}, \tilde{h}) + I_b \right) \hfill (3)$$

Comparison with Eq.(1) suggests that spin switches could provide a possible building block for HNN using $V_i$ to implement the desired weights $w_i = V_i g_i / (1 + G_{total} r)$. However, the details are not obvious especially since the function $f$ is hysteretic rather than the usual single-valued function.

In estimating the threshold current/voltage needed to drive the (next) Write unit, we note that a spin current of $2I_{sc}$ (critical spin current required to switch the magnet) will be needed to flip the Write magnet since it couples to the magnet of the Read unit. Hence:

$$I_{sc} \geq \frac{2I_{in}}{\beta} = \frac{2I_{in}}{\theta_{SH}(A_s/A)} \hfill (4)$$

As a result, the threshold voltage

$$V_{th} \geq \frac{2I_{th}}{g_i(1 - P)} (1 + G_i r) \hfill (5)$$

Using parameters described in Ref. 9, we have $I_{sc} = 160\mu A$. If $t_{gshe} = 2\text{nm}$ and the Hall angle reported experimentally $\theta_{SH} = 0.3$ for tungsten, the threshold current $I_{th} \approx 30\mu A$.

Also assuming TMR of 135% for the MTJ and resistance-area product of $A_s/G_p = 4.3\Omega \mu m^2$ \hfill (12), we have $P = 0.4$ and $g_i = (1.1k\Omega)^{-1}$ for $A_k = 80\text{nm} \times 30\text{nm}$. If we chose other GSHE material \hfill (13,14) with comparable spin hall angle but with low resistivity, then we can assume $G_i r \ll 1$. This will give us $V_{th} \approx 100\text{mV}$.

The power consumption of SS can be estimated as $P = I_{th} V_{th} \approx \text{few } \mu W$ along with the switching time of magnet as $\tau = 1\text{ns}$ results in energy consumption for the SS $E \approx \text{few } f J$ per switch. We should mention, however, that from the point of view of energy and delay, spin switches (or in general beyond-CMOS devices\hfill (15) based on established technology are inferior to a single CMOS transistor, but may still look attractive compared to CMOS based neurons\hfill (16), due to the compact multi-functionality provided by the SS (note that, the area of a SS is roughly the area of magnet in the Read or Write unit which is typically $\approx 100\text{nm}^2$). Moreover, the switching energy of a single SS neuron could be lowered significantly as new phenomena are discovered and developed (see for example\hfill (17-19)).

**Fan-out:** An important attribute of the SS is the possibility of large fan-out, whereby the output from one spin switch can be used to drive hundreds of other spin switches thus allowing large interconnectivity which is important for implementing neural network functions.

Fig.2 shows a SS neuron with multiple outputs where the voltage at each R unit represents the synaptic weight of this neuron in connection with the other neurons. Since each R unit has its own independent power supply, this neuron should be able to drive a large number of outputs. Note that the interconnections between neurons do not require GSHE material. They could be low resistance material (copper wires) with no increase in energy consumption. The only limitation arises from the threshold current/voltage needed to drive such a “big” neuron. Eq. (4) shows that the threshold current is proportional to the area $A$ of GSHE, but independent of its length. Of course the resistance ‘$r$’ of the GSHE increases with length but this has a minimal effect on the threshold voltage as long as the factor $(1 + G_i r)$ is not excessive. For example, if $L_{gshe}/L_{FM} = 100 \cdot W_{gshe}/W_{FM} = 2 \cdot \rho_{gshe} = 10^{-7} \Omega m$ we have $(1 + G_i r) \approx 3$.

![Synapse weights](image)

**FIG.2** A composite spin switch neuron with built-in synapses. The magnetization of any R unit represents the state of the neuron. The voltages at each R units represent the weight of synapses connecting to other neurons.
In designing a neural network (NN), we focus on the multi-layer feed-forward NN with training done off-line by smoothing the SS hysteresis function to make it differentiable and adapting the back-propagation method. Other techniques such as the weight perturbation method or the extreme learning machine might also be suitable especially for on-chip training. The key difference with standard neural network design is the hysteresis in the threshold function which makes the overall design more robust, but requires an extra condition during the training: the currents arriving at each neuron have to be above threshold.

To model SS devices, it’s notice that each SS with a W/R pair requires a pair of LLG equations for the magnet pair (see for more detail).

\[
\begin{align*}
I_{si} &= \beta \left( \sum_j V_j \frac{G_j(\hat{x}_j)}{1 + r_i G_{total}} + I_{bi} \right) \hat{z}; \quad I_{si} = -P_i V_j G_{ij} \hat{z} \\
\end{align*}
\]

where \(V_j\) are the voltages and \(I_{bi}\) are bias currents applied at preceding Read units.

Fig. 3 shows the input-output characteristic of a SS device. Note that at \(V = 0\), the switching currents are symmetric but there is a minor shift when \(V = V_{th}\). This is due to a (small) spin current \(I_s\) injected by the Read unit making it easier to switch from +1 to -1 than to switch from -1 to +1. This shift is relatively minor ensuring the key property of directionality: the state of the magnet (neuron) is largely determined by the input and not the output current.

Neural network for character recognition: Now we consider an example of a SS neural network designed for character recognition: it recognizes 8 letters A, B, C...H represented by \(7 \times 5\) matrices or vectors having 35 components (zero or one). Fig. 4a shows the layout of the SS neural network for this pattern recognition with 35 neurons in the input layer, 6 neurons in the hidden and 3 neurons in the output layer (labeling from 1 to 9). Hence each neuron in the input layer has six synapses while each neuron in the hidden has 3 synapses.

\[
\begin{align*}
\end{align*}
\]

FIG. 4 a) Implementation of spin switch neural network for character recognition: for simplicity the connections (copper wires) between layers are not shown. b) Matrices of interconnection weight voltages between input and hidden layers (35 × 6) and between hidden and output layers (6 × 3) shown by color scale.
FIG. 5 a) LLG simulations for the outputs layer of the SS neural network described in Fig. 5a in response to eight input characters: A, B, C...H. Here R7, R8 and R9 are the magnetizations of magnets in the R units of neuron 7, 8 and 9 respectively. b) The network still recognizes a letter that is not in the training set (a random defect). We assume all Read units have the same polarization and conductance: $p_i = 0.4, g_i = (1.1 \Omega)^{-1}$, $\beta = 12$

The voltages $V$ applied at Read units represent the weight of synapse in connecting with other neurons while the $I_P$ represents the bias current applied at each neuron. Both voltages and bias currents obtained through the training are shown in Fig. 4b in the form of $(35 \times 6)$, $(6 \times 3)$ matrices and $(1 \times 9)$ vector. They are all normalized to their threshold values.

Fig. 5a shows simulation results obtained from solving a set of 88 coupled LLG (70 for the input, 12 for the hidden and 6 for the output layer) equations whose solutions are the dynamics of the magnets. For a neuron with many synapses, we assume all the W/R units are identical so that the whole neuron can be modeled as a single W/R unit. Fig. 5a illustrates the character recognition function: If the input is A, the output is 000 which can be translated to $111$ for magnetizations of W magnets (note $\bar{1}$ means $m_2 = -1$). For magnets in the R units the result is 111. It is interesting to notice that, even there is a (random) defect in the letter, the network is still able to recognize it as shown in Fig. 5b.

It’s also notice that the layout for character recognition in Fig. 4a is quite robust to small variations of voltages and bias currents (see also XOR example in 23). Since currents arriving at neurons are always above threshold, the switching characteristics will not be affected by thermal noise.

Finally we would like to discuss a possible way of storing and adjusting the voltage applied at R units. The use of floating-gate(FG) transistors has been proposed as a mechanism to store tunable analog voltages which can be used for synapse weights 24, 25. Controlled amounts of charge can be injected and removed from the gate to create a spectrum of gate voltages which is important in the realm of neural networks.

Fig. 6 shows a possible means to store/adjust the voltages applied at the synapse Read unit MTJs using a FG low drop-out voltage regulator 26. As depicted, programmatic control of an individual FG charge can be accomplished through an addressable array that selectively controls $(V_{\text{tun},n}, V_{\text{Gn}})$ and $(V_{\text{tun},p}, V_{\text{Gp}})$. The tunneling voltage can be used to provide a global erase of stored values via Fowler-Nordheim tunneling while the respective gate voltages can be used to inject charge onto the FG with Channel Hot Electron Injection. This charge control in turn modulates the threshold voltage of the nFET/pFET and hence the regulated voltage. As a result, the nFET/pFET can be programmed to provide the desired synapse weights through an active learning process. Once programmed, these FG transistors will retain the voltage for an extended period of time due to their non-volatility.

In summary, we have demonstrated the possibility of a hardware neural network implementation using a spin switch (SS) as its basic building block. SS is a recently proposed
device based on established technology having a transistor-like gain and input-output isolation that allows large circuits to be constructed without intervening clocks or amplifiers. The SS neuron-synapse used in the present paper differs from the SS proposed in \cite{9} in the sense that there is only one MTJ stack at the Read unit. Among the three components comprising the SS, so far the GSH material and MTJ stack have been experimentally established. The dipolar coupling has also been well studied in the context of nano-magnet logic\cite{27}. But for SS applications, one needs to show the dipolar coupling between magnets having thicknesses $2 - 4$nm.

We have shown that a SS can be used to build neuron capable of performing summation, multiplication and an activation function which normally requires extra circuitry in other hardware implementations. The SS neurons occupy area much less than $\mu\text{m}^2$, consume femtojoules per switch and operate at room temperature. The weights for the neural network are conveniently adjusted through analog voltages that can be stored in a non-volatile manner in an underlying CMOS layer using a floating gate low dropout voltage regulator. The operation of a multi-layer SS neural network designed for character recognition is demonstrated using a standard simulation model based on coupled Landau-Lifshitz-Gilbert (LLG) equations, one for each magnet in the network.

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Appendix I. Training methods for hysteresis activation function by back propagation method

Since the back propagation (BP) method requires a differentiable activation function, we have to approximate the hysteresis activation of the magnet, for example, in the following way:

\[ y = f(x, x_0) = \begin{cases} \tanh(c \cdot (x - 1)) & \text{if } x \geq x_0 \\ \tanh(c \cdot (x + 1)) & \text{if } x \leq x_0 \end{cases} \]  

where \( x_0 \) is the “history” value of \( x \). For example, the red curve in fig. S1 is calculated with large negative \( x_0 \) while in the green curve, \( x_0 \) is a large positive number.

FIG. S1 An approximation of hysteresis function with \( c = 4 \) in Eq.1

To illustrate the concept, we focus on SS neural network having 3 layers: input, hidden and output as in Fig. S2 where each neuron is a W/R pair having opposite magnetization. The signals arrive at W units and come out at the R units. Given a set of input \( [x] \) (training set) and a desired output \( [d] \) vector, the BP method will find weight matrices \( [W_1], [W_2] \) and bias \( [b_1], [b_2] \) vectors such that the input produces the output.

From Eq. 3 in the main text, the output of a neuron is:

\[ y_i = f \left( \sum_j W_{ij} (1 \pm P_j x_j) + b_i \right) \]

where \( x_j \) is the magnetization of magnet in the W or R unit (they has opposite sign). Therefore, we can follow the BP method in literature \(^1\) with neuron states are represented by \( 1 + P x_j \) or \( 1 - P x_j \). Here are the steps used in finding the weights for a SS neural network:

For each training (epoch) {
    Randomly initialize values of \([W_1], [W_2], [b_1], [b_2]\) and states of neurons in the hidden and output layers.
    For each vector in the input set:
        Feed Forward, calculate updated functions and update the weight
    }

Evaluate the total mean squared error

The Feed Forward, update functions and weigh update are described in the following steps:

**Step 1:** Calculate the outputs of neurons in the hidden layer

\[ y = f([W_1](1 + P[x]) + [b_1]) \]

where \( f \) is the function in Eq. A1. Notice that those are the outputs of the Write units.

**Step 2:** Calculate the outputs of neurons in the output layer:

\[ [O] = f([W_2](1 - P[y]) + [b_2]) \]

Notice that the outputs of Read unit are opposite the outputs \([y]\) of Write unit in step 1.

**Step 3:** Calculate the update functions

\[ [\Phi_2] = [f'_\text{latent output}] \times ([d] - [O]) \]

\[ [\Phi_1] = [f'_\text{latent hidden}] \times [W_2]^T \Phi_2 \]

Where the derivatives of \( f \) are evaluated at output and hidden layer neurons for \( \Phi_2 \) and \( \Phi_1 \) respectively.

**Step 4:** Update the weight matrices and bias vectors

\[ [b_1] = [b_1] + \eta [\Phi_1] \]

\[ [b_2] = [b_2] - P \eta [\Phi_2] \]

\[ [W_1] = [W_1] - \eta P (1 + P[x])^T [\Phi_1] \]

\[ [W_2] = [W_2] + \eta (1 - P[y])^T [\Phi_2] \]

where \( \eta \) is the learning coefficient.

The total mean squared error function can be calculated as:

\[ E = 1/2 \| [d] - [O] \|^2 \]

If \( E \) is smaller than a selected criteria, we stop the algorithm, otherwise continue to train the network.
As mentioned in the main text, the hysteresis activation function requires one more condition: the total weighted sum arriving at neurons has to be above threshold. This will make sure that, the mapping from the input to the output is independent of the initial states of the hidden and output neurons. One way to accomplish this is to randomize the states of the neurons before entering for loop of input set in the above scheme.

It is also desirable to find weights that have low voltage values to avoid accidental switching of magnets in the Read units. The states of neurons should be determined by the signals arriving at the W units and not by the weights voltages at R units.

**Appendix II. Spin Switch neural network for Exclusive Or**

As a simple example of the SS-based implementation of a neural network, we show the layout for a non-linear exclusive or (XOR) gate in Fig. S3a. The voltages $V$ applied at Read units represent the weight of synapse connecting neuron $i$ and $j$ while the $I_b$ represents the bias currents applied at each neuron. Voltages and currents are obtained via training and their values are normalized to the threshold values.

Fig. S3b shows the simulation results of XOR obtained by solving a set of 30 coupled first-order differential equations (three components of the ten magnets, two per each neuron: A, B, 1, 2, 3) whose solutions are the dynamics of the magnets. For a neuron with many synapses, we assume all the W/R units are identical so that the whole neuron can be modeled as a single W/R unit. It is evident from Fig. B1b that the network behaves as an XOR gate when it responds to inputs A and B. For example, (A,B)=(1,1) and (-1,-1) have the same outputs and similarly for (A,B)=(1,-1) and (-1,1).

**Robustness of design:** The XOR layout in Fig. S3a is quite robust to small variations of voltages, bias currents and is not affected by thermal noise. This can be understood in the following way by defining the dimensionless weighted sum at the W units:

$$Z_w(j) = \sum_i V_o(1 + P_{mi}(i)) + I_{b}(j)$$

where $V_{ij}$ is the normalized voltage connecting neuron $i$ and $j$. $I_{b}(j)$ is the normalized bias current at neuron $j$. If $|Z_w(j)| > 1$, this implies that $|I_{w}(j)| > I_{th}$ and the magnet in W unit will be switched depend on the sign of $Z_w(j)$.

Table I shows the calculation of weighted sum $Z_w(j)$ at neurons $j$ in the hidden and output layers (labeled 1, 2 and 3) and its corresponding states (at Read unit) for every pair of inputs. As shown, they satisfy the condition $|Z_w(j)| > 1$ at every neuron for $P=0.4$ which means currents arriving at neurons are always above threshold. Because of this, the switching characteristics will not be affected by thermal noise.

The table also suggests that a small variation of voltages and currents will not affect the results making the design quite robust. For example, if we change $|V| = 3$ to $|V| = 3.2$ in the layout (keeping the sign), the network still functions as before.

$$D. \text{ Graupe, Principles of Artificial Neural Network (World Scientific, 2007).}$$