Current Threshold Elements of Cyclic Shift for Constructing Specialized IP-Memory Modules in Automation and Systems for Tolerance Control of Analog Signals

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Abstract. The current threshold elements of direct and reverse cyclic shift are developed. This logical elements are recommended as memory elements for the construction of relevant controllers and devices for tolerance control of analog signals, which used in diagnosis of complex electronic equipment. The mathematical apparatus used in the design is a linear algebra. The basic equations and results of computer modeling of the developed cyclic shift schemes are presented. Computer simulation was carried out in the Cadence environment on models of field-effect transistors XB06.

1. Introduction

The logical synthesis of the IP-modules for digital control and computing systems is based on the use of functionally complete bases of logical elements (LE). In the two-digit case, all such bases contain the inversion operation (as a separate operation) or associated (Schéffer stroke, Pierce arrow) [1-6]. The transition from classical binary logic to multi-valued logics provides a number of advantages and new functionality opportunities due to the emergence of multi-valued equivalents of two-digit operations of new properties that are absent in the two-digit case [7, 8]. For example, a generalization of the inversion operation for $k$-valued variables is the cyclic shift operation. Moreover, for $k > 2$, the direct cyclic shift operation (addition of 1 to mod $k$) and the reverse shift operation (subtraction of 1 by mod $k$) can be determined. As follows from the definition of shear operations, they both coincide with the inversion function for $k = 2$.

The linear algebra used as a mathematical apparatus for the logical synthesis of digital structures [7] allows one to obtain a logical, and on its basis, circuitry, implementation of linear analogs of the indicated logical functions [8]. At the same time, wide design possibilities are provided not only for classic Boolean elements, but also for logical devices for multi-valued signals. These circuitry solutions can then be used to build specialized current logic IP-modules and digital difficult functional blocks based on them, processors, which working with current logical variables, as well as means of tolerance control and diagnostics of complex electronic equipment [9-12].
The purpose and novelty of the article is to creation of current threshold circuits for the direct and reverse cyclic shift, which based on the mathematical apparatus of linear algebra.

2. The methodology of logical synthesis in linear algebra
To synthesize the logical functions of digital structures, regardless of significance, it is necessary:
1. Choose a basis that meets the technical, technological and operational requirements for the designed device;
2. Build an inverse matrix for it;
3. Multiply the vector of values of the projected function by the columns of the inverse matrix and obtain the vector of weights of the basis vectors in the representation of the function in this basis;
4. Write the representation of the implemented function in the form of the algebraic sum of weighted basis vectors.

Example. Perform a logical synthesis of forward and reverse cyclic shift operations in three-valued logic.
To demonstrate the capabilities of linear algebra, we choose two three-valued bases: one is a threshold
\[ A_1 = \begin{bmatrix} 1 & x \\ x > 1 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 0 & 1 & 2 \\ 0 & 0 & 1 \end{bmatrix} \]
\[ (A_1)^{-1} = \begin{bmatrix} 1 & -1 & 1 \\ 0 & 1 & -2 \\ 0 & 0 & 1 \end{bmatrix} \]

and the other is combined based on the operations of the truncated difference and the threshold function
\[ A_2 = \begin{bmatrix} 1 & x \div 1 \\ x < 1 \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 0 & 0 & 1 \\ 1 & 0 & 1 \end{bmatrix} \]
\[ (A_2)^{-1} = \begin{bmatrix} 0 & 0 & 1 \\ 1 & -1 & -1 \\ 0 & 1 & 0 \end{bmatrix} \]

The truth tables of the designed operations are of the form:

| \( x \) | 0 | 1 | 2 |
|---|---|---|---|
| \( \oplus (x) \) | 1 | 2 | 0 |
| \( \ominus (x) \) | 2 | 0 | 1 |

The first basis represents cyclic shift operations in the form
\[ \oplus (x) = 1 + x - 3(x > 1) ; \]
\[ \ominus (x) = 2 - 2x + 3(x < 1), \]
and the second in the form
\[ \oplus (x) = 2 - 2(x \div 1) - (x < 1) ; \]
\[ \ominus (x) = (x \div 1) + 2(x < 1). \]
As can be seen from the expressions obtained, their complexity in terms of logical synthesis and circuitry implementation is different, so the problem of optimal choice arises. Leave it for future research. Here, we choose for the logical synthesis of the expression:

\[ \Theta(x) = 1 + x - 3(x > 1); \]
\[ \Theta(x) = (x \div 1) + 2(x < 1). \]

3. The element of direct cyclic shift

As indicated earlier, the direct cyclic shift operation is defined as follows:

\[ y = x \oplus^k 1. \]

For \( k = 3 \), this expression corresponds to the truth table:

| x | 0 | 1 | 2 |
|---|---|---|---|
| y | 1 | 2 | 0 |

Signal conversion operations can be written as:

\[ y = x + 1 - 3((x + 1) > 2.5). \]  \( (1) \)

Figure 1 shows a diagram of the current threshold LE of direct cyclic shift on CMOS transistors [13], which implements expression (1).

![Figure 1. The CMOS circuit of a threshold current LE of direct cyclic shift.](image)

In accordance with the expression (1), the summation of the argument \( x \) with 1 is made by mounting the input of the LE input and the first reference current source \( I_0 \) at the input of the current mirror CM1. For comparison with the constant 2.5\( I_0 \), the current of the second reference current source is subtracted from the leaky current of the first output CM1. The differential current is supplied to the combined sources of the input transistors M1 and M2. The operating modes of these transistors are set by the voltage values of the bias voltage sources \( V_{off1} \) and \( V_{off2} \) and ensure that transistors of current mirrors are not saturated. When the sign of the difference in currents changes the transistors M3 and M4 of the differential stage (DS) switching. If the output current CM1 of the threshold level (2.5\( I_0 \)) is exceeded, the DC output current through the current mirror CM2 enters the output current generating
unit on transistors M5, M6 and is subtracted from the second output current CM1. The differential signal from the drain of the transistor M6 in the form of a leakage current signal is fed to CM3, where it is converted into an equal to the incoming current signal and fed to the output of the device [13].

4. The element of reverse cyclic shift
The inverse cyclic shift operation is defined as follows:

\[ y = x \ominus^k 1. \]

For \( k = 3 \), this expression corresponds to the truth table:

| x | 0 | 1 | 2 |
|---|---|---|---|
| y | 2 | 0 | 1 |

The threshold logic element of the inverse cyclic shift is described by the expression:

\[ y = x - 1 + 2(x < 0.5). \]  \hspace{1cm} (2)

Figure 2 shows a diagram of the current threshold LE of the reverse cyclic shift on CMOS transistors [14], constructed in accordance with expression (2).

![Diagram of the reverse cyclic shift LE on CMOS transistors](image)

**Figure 2.** The CMOS scheme of a threshold current LE of a reverse cyclic shift.

The implementation of the algebraic summation of the terms in expression (2) is carried out by assembling the leakage current of the second output CM1 and the flowing current of the third reference current source \( I_3 \), a comparison with the constant 0.5\( I_0 \) is provided by subtracting the current of the first reference current source \( I_1 \) from the current of the first output CM1 at the input of the threshold element containing transistors M1, M2 and DS on transistors M3, M4, a change in the sign of the difference in currents at the sources M1, M2 leads to switching transistors in DS. With a negative current difference at the input of the threshold element, the current of the reference current source \( I_2 \) enters through the transistor M4 and the current mirror CM2. From the combined signals at the input of CM3, the current of the reference current source \( I_3 \) is subtracted and converted through the CM3 to the input current signal, which is fed to the output of the device [14].

5. Results of computer simulation
In the circuits in figures 1, 2 resistor R1 is used to detect the presence of current quanta in the output at experimental studies.
The figure 3 shows a diagram of the ternary element of direct cyclic shift (figure 1) in the Cadence Virtuoso computer simulation environment on XB06 field-effect transistor models [13].

![Circuit Diagram](image)

**Figure 3.** The circuit of the direct cyclic shift LE of figure 1 in a Cadence environment.

On figure 4 shows the oscillograms of the input and output signals of the circuit of the current threshold LE of direct cyclic shift (figure 3) [13].

![Oscillograms](image)

**Figure 4.** The oscillograms of the input and output signals of the LE circuit of figure 3.

In figure 5 shows the reverse cyclic shift LE model (figure 2) in the Cadence computer simulation environment using XB06 field-effect transistor models [14].
Figure 5. The circuit of the reverse cyclic shift LE of figure 2 in a Cadence environment.

In figure 6 shows the oscillograms of the input and output signals of the circuit of the current threshold LE of the reverse cyclic shift (figure 5) [14].

Figure 6. The oscillograms of the input and output signals of the LE circuit of figure 5.

Shown on figures 4, 6 the results of computer simulations show the full compliance of the developed schemes with the algorithms of cyclic shift operations (figure 1, 2).

6. Conclusion
Thus, the developed circuit solutions of the threshold logic elements of the cyclic shift of the input ternary logical variable \( x \) are characterized by the multi-valued state of internal signals and signals at their current inputs and outputs. These logical elements, being the most important elements of functionally complete bases, can serve as the basis for computing and control devices using a multi-valued linear algebra, a particular case of which is Boolean algebra.
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