Low-Voltage, Printed, All-Polymer Integrated Circuits Employing a Low-Leakage and High-Yield Polymer Dielectric

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In the path toward the integration of organic field-effect transistors (OFETs) and logic circuits into low-cost and mass produced consumer products, all-organic devices based on printed semiconductors are one of the best options to meet stringent cost requirements. Within this framework, it is still challenging to achieve low voltage operation, as required by the use of thin film batteries and energy harvesters, for which a high capacitance and reliable organic dielectric is required. Here, the development of a parylene-C based dielectric bilayer compatible with top-gate architectures for low-voltage OFETs and logic circuits is presented. The polymer dielectric allows the high yield fabrication of all-polymer, bendable, transparent p- and n-type OFETs operating below 2 V, with low leakage, uniform performances, and high yield. Such a result is a key enabler for the reliable realization of complementary logic circuits that can operate already at a voltage bias of 2 V, such as well-balanced inverters, ring-oscillators and D-Flip-Flops.

1. Introduction

Organic field-effect transistors (OFETs) have been extensively studied in the last decades and are currently considered as the building block of the next generation of thin film electronics.[1–3] This technology allows for the development of large area, inexpensive, transparent electronic devices by means of cost-effective manufacturing techniques. Organic materials can be processed from solution, mostly by means of printing and coating techniques, which are low-temperature processes, enable mass production, and minimize the by-products.[4] Being these manufacturing techniques compatible with flexible, plastic and other low-cost substrates, there is a clear potential for the integration of additional electronic functionalities into mass-produced, consumer products.[5–7] In order to meet very stringent costs constraints, which do not allow integration of conventional electronic chips, all-organic circuits fabricated by means of scalable techniques are one of the best options.

One of the main limitations hindering the adoption of all-organic printed circuits in real applications is related to their operating voltage.[8] In order to grant their portability and easy integration, these circuits need in fact to be powered by thin film batteries[9,10] and/or energy harvesters, such as plastic solar cells,[11,12] thus requiring maximum operation voltages of a few volts and low power consumption, while keeping reasonably high values of accumulated charge density and of current flowing into the circuits. Efficient low voltage operation can be achieved by acting on the capacitance of the dielectric layer, which should be as high as possible and at the same time guarantee optimal charge accumulation and transport at the semiconductor–dielectric interface of both holes and electrons, in order to enable complementary architectures to drastically reduce power consumption.[13,14] Many efforts have been recently devoted to the development of suitable polymer materials for gate dielectric applications, aiming at the achievement of the highest possible gate capacitance.[15] Two main strategies may be followed, either increasing the dielectric constant of the employed material or decreasing its thickness. The integration of high-k materials as dielectrics is not straightforward, as the energetic disorder at the interface might interfere with charge transport inside the semiconductor layer.[15,16] Multilayer structures combining low-k and high-k materials have been therefore introduced.[17,18] However, high-k materials typically show dielectric relaxations occurring at low frequency,[19,20] possibly limiting the maximum operation frequency of OFETs. Such limit is particularly severe in electrolyte gated transistors,[21] where huge capacitances are achieved at the expense of the switching speed because of ions motion, even in recent solid-state electrolytes.[22]

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choice is to downscale a low-k dielectric polymer. However, this strategy typically leads to very high leakage currents or complete breakdown of devices. A possible solution to the latter is the adoption of poly(chloro-p-xylene)-C (Parylene-C), a low-k, semicrystalline, thermoplastic polymer, which is commonly deposited by means of chemical vapor deposition (CVD).[23] This is not a solution-based printing technique, but it has already been shown to be large-area compatible and industrially scalable, so it would not be a limiting factor during a possible upscale of the manufacturing. This dielectric grants a low energetic disorder at the semiconductor-dielectric interface[24] and presents some appealing characteristics, such as its chemical inertness, flexibility, and the ability to form conformal, pin-hole-free coatings.[24,25] For such reasons, parylene has been largely investigated as a dielectric for OFETs, although most of the reports deal with bottom-gated structures,[26–33] where the dielectric is deposited on an inert surface and not on the active material. Staggered, top-gate structures are however very important toward the development of logic circuits as they allow for optimal charge injection,[34] thanks to the possibility of reducing the contact resistance through gate to source/drain electrodes overlap.[35] Moreover, they allow for controlled interfaces between the semiconductor and the dielectric layer,[16,17] and for a partial self-encapsulation effect thanks to the upper gate dielectric and the gate electrode which improves environmental stability of devices.[38] In the context of OFETs based on a printed semiconductor, only one example of top-gated device employing parylene as dielectric has been reported, with opaque evaporated metallic contacts and operating voltages in the order of 30 V, thus not compatible with low voltage operation.[39]

Here we exploit a thin parylene layer for the development of a high capacitance polymer bilayer dielectric, comprising an ultrathin poly(methyl methacrylate) (PMMA), compatible with top-gate OFETs. Our bilayer dielectric achieves areal capacitances in the order of 20 nF cm\(^{-2}\) with leakage currents below 1 nA cm\(^{-2}\). It enables the robust fabrication of low-voltage, transparent, fully-polymeric, and complementary OFETs, where all the layers are inkjet printed but the parylene layer, based on poly[(N,N′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl)-alt-5,5′-(2,2′-bithiophene)] (PND12OD-T2) and poly[2,5-bis(7-decylnondenacyl)pyrrolo[3,4-c]pyrrole-1,4(2H,5H)-dione-(E)-1,2-di(2,2′-bithiophen-5-yl)ethene] (29-DPP-TV) as n- and p-type semiconductors, respectively. The ideal dielectric characteristics allow the transistors to operate with sub-10 V voltages and low leakage and to be fabricated with a 99% yield and good uniformity, as probed on a 100 transistors array for each OFET polarity. The reliable process was key to enable the integration of OFETs into logic circuits of different level of complexity operating down to 2 V, from well-balanced complementary inverters to seven-stages ring oscillators with stage delays as low as 1.14 ms, and D-Flip-Flops, fundamental building blocks of registers, counters and timers. Our results, exploiting scalable deposition processes, therefore offer a viable path for the cost-effective integration of electronic functionalities into consumer products.

2. Results and Discussion

For the realization of high capacitance all-polymer dielectrics, we opted for a bilayer dielectric combining a thin parylene film on top of an ultrathin solution-processed layer of PMMA, thus combining the excellent dielectric properties of parylene[40] and the optimal interface formed by PMMA with a broad range of polymer semiconductors. The PMMA layer is in fact important to achieve optimal n-type devices (Figure S1, Supporting Information), as it protects the electron transporting semiconductor from the degrading effect of chlorine present in the parylene.[39]

The overall dielectric properties of the bilayer dielectric have been investigated in order to find the best combination to be integrated into printed OFETs and circuits. For this analysis, a MIM (metal–insulator–metal) structure has been employed, as shown in Figure 1a, with the dielectric bilayer deposited between two metallic electrodes. The PMMA layer is 20 nm thick, while for the parylene layer we considered different thicknesses; for the analysis presented here, three different capacitors have been examined, with parylene layers that are 120, 200, and 310 nm thick. The capacitance as a function of frequency for the three above mentioned capacitors has been measured and is shown in Figure 1b. The areal capacitance at 1 kHz is 11.54 nF cm\(^{-2}\) for the 310 nm thick parylene layer, and it increases to 16.69 and 19.00 nF cm\(^{-2}\) for the 200 and 120 nm thick layers, respectively. The average leakage current at 10 V amounts to 10 nA cm\(^{-2}\) for the 120 nm thick parylene layer, while the 200 and 310 nm thick layers show average leakage currents of 4.6 and 2.25 nA cm\(^{-2}\), respectively (Figure 1c). Bilayers employing parylene layers thinner than ~120 nm, despite leading to an increase in capacitance, typically resulted in defective capacitors or short circuits. Following the capacitors characterization, we

![Figure 1](image-url)  
*Figure 1. a) Schematic diagram of the MIM structure. b) Capacitance as a function of the frequency and c) leakage current density of the capacitors. All the values shown here have been obtained as average over three identical devices.*
therefore decided to adopt bilayers with parylene films with thicknesses of about 100 nm for the printed transistors, so that a good compromise could be reached between low operating voltage, favored by the high capacitance value, and low leakages, together with a high yield and uniform performances.

The dielectric bilayer has been integrated into p- and n-type bottom-contact/top-gated OFETs (Figure 2a). These devices have been fabricated exclusively by means of additive processes, which are cost-effective and industrially scalable. First, poly(3,4-ethylenedioxythiophene):polystyrene sulphonate (PEDOT:PSS) source and drain contacts have been inkjet-printed (Figure 2b) onto 125 µm thick polyethylene naphthalene (PEN) substrates, defining a channel length (L) of 65 µm and width (W) of 1000 µm. Small pads of silver nanoparticle-based ink have been printed in correspondence of the points where electrical contacts are created during the characterization of transistors and circuits; it should be pointed out that these pads are only needed to facilitate external electrical probing of the devices, which can operate also without them, in a fully transparent configuration. Onto the contacts for the n-type transistors, a polyethylenimine (PEI)-based injection layer has been printed (Figure 2c), leading to enhanced electrons injection thanks to a reduced electrode work-function and interface doping.\[41,42\] P(NDI2OD-T2) has been inkjet printed for n-type devices, while 29-DPP-TVT for the p-type ones (Figure 2d,e). The dielectric stack has been subsequently deposited on top of the semiconductors: the 20 nm thick PMMA layer has been spin-coated, while parylene has been deposited by means of CVD, thus obtaining a dielectric stack with an overall thickness lower than 150 nm. Lastly, PEDOT:PSS gate electrodes have been inkjet printed on top of the dielectric (Figure 2f).

The electrical characterization of the resulting OFETs is presented in Figure 3. As it can be seen from the transfer curves (Figure 3a,d), both p- and n-type transistors show proper current modulation at voltages as low as 1 V. Output curves (Figure 3b,e) are rather ideal in the case of p-type devices, while a residual S-shaped characteristic is visible for n-type devices, likely owing to contact effects, though not precluding a correct low voltage operation of the devices.

The presented electrical data have been extracted from an array of 100 transistors for each polarity, in order to address both the performances and the uniformity of the printed OFETs. The average transfer curves with their standard deviation, for an applied source–drain voltage \(V_{DS}\) of 10 V, are shown in Figure 3c,f, while the raw data, both for linear and saturation regime, can be found in Figure S3 (Supporting Information). The average maximum current, which has been extracted from the 10 V transfer curves, amounts to 1.67 ± 0.29 µA for the n-type devices, while for the p-type devices it amounts to 4.02 ± 0.28 µA. This difference in the performance can be explained by considering the combined effect of their average field-effect mobilities and of their threshold voltages.

The average field-effect mobility of electrons (\(\mu_e\)) and holes (\(\mu_h\)), over 100 devices in both cases, was extracted from the slope of the transfer characteristic curves in the \(V_G\) range from 8 to 10 V, according to the gradual channel approximation.\[43\] The areal capacitance for the dielectric stack employed in these devices has been measured for frequencies down to 5 Hz (Figure S2c, Supporting Information), where we recorded a capacitance equal to 22.6 nF cm\(^{-2}\); this value has been used for the mobility extraction. For n-type devices, \(\mu_e = 0.08 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}\) in the linear regime \((V_{DS} = 2 \text{ V})\), and \(\mu_e = 0.12 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}\) in the saturation regime \((V_{DS} = 10 \text{ V})\), while for p-type devices \(\mu_h = 0.20 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}\) in the linear regime, and \(\mu_h = 0.21 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}\) in the saturation one. In the latter case, the mobility values do not show substantial gate voltage dependence in full accumulation (Figure S4b, Supporting Information), n-type OFETs, on the other hand, exhibit a slightly non-ideal behavior, given by a small gate dependence of the mobility curves (Figure S4a, Supporting Information). We extracted the measurement reliability factors (\(\eta\)), as recommended by Choi et al.,\[44\] and obtained in both cases high values: close to 100% for holes mobility in both linear (96%) and saturation (95%), and higher than 70% for electrons mobility (81% in linear and 73% in saturation regime). As a result, average effective mobilities \(\mu_{eff}\), which are more robust figure of merits to describe carriers field-effect mobility in thin-film transistors and are calculated as
µ_x × r and µ_y × r, are very close to µ_0 and µ_u: for p-type devices, μ_{eff,lin}=0.19 cm^2 V^{-1} s^{-1} and μ_{eff,sat}=0.20 cm^2 V^{-1} s^{-1}, and for n-type devices μ_{eff,lin}=0.06 cm^2 V^{-1} s^{-1} and μ_{eff,sat}=0.08 cm^2 V^{-1} s^{-1}. The lower r for n-type OFETs is due to the combined effect of a weak gate voltage dependence and a higher threshold voltage: P(NDI2OD-T2) devices present a threshold voltage of 1.35 ± 0.41 V and a turn-on voltage of 1 ± 0.22 V, while 29-DPP-TVT transistors show lower current onset values, with a threshold voltage of 0.49 ± 0.21 and 0.68 ± 0.3 V as turn-on voltage. The subthreshold slope (SS) is 148 ± 23 and 126 ± 25 mV dec^{-1} for p- and n-type OFETs, respectively. On-off ratios, defined as the maximum ratio of the drain current values in the “on” and “off” states, are relatively high, with average values of $5 \times 10^5$ for the p-type transistors and of $7 \times 10^6$ for the n-type ones.

The transfer curves for devices of both polarities present a small hysteresis. For what concerns p-type devices, during the backward sweep, the threshold voltage slightly shifts toward positive voltage and the SS is increased. The n-type OFETs, on the other hand, present a shift toward negative voltages and the same increase in SS. This feature can be explained with the presence of shallow traps at the dielectric interface, which are filled during the forward sweep and remain so during the backward one, which thus appears to be slightly more ideal. Being this hysteresis limited in size and reproducible, it does not affect the performances of our devices in a significant way and can be considered to be negligible.

Overall, of the 200 transistors fabricated for this electrical analysis, only two were not working, leading to a 99% yield. From a simple inspection with the optical microscope of the defective devices, we found that failure in the two devices was caused by particulate that landed onto the active channel (Figure S5a,b, Supporting Information). It is therefore reasonable to expect that in a more controlled environment, such as a classified cleanroom, the yield may approach 100%.

Gate leakage currents of our transistors are very low, with a flat curve and leakage current values below 100 pA (Figure 3a,d). More than 90% of the transistors are characterized by such low leakage, as shown in the raw data in Figure S3 (Supporting Information), while only about five devices for each polarity present an increased leakage current, while still working properly, with current and mobility values comparable with the ones of the very low leakage devices. For what concerns the transistor arrays presented here, the presence of the leakage current is to be related in
most of the cases to the accidental presence of small droplets of the silver nanoparticles ink into the transistors channel, as shown in Figure S5c (Supporting Information). Silver pads are needed uniquely for the characterization of transistors and circuits with external probes, but they are not needed for the actual operation of these devices; the main outcome of this work is in fact the development of fully transparent integrated circuits, in which the main cause of defective behavior here highlighted is eliminated.

The bendability of the printed transistors has been assessed, by means of bending tests with different applied bending radii, equal to 5.5, 8, and 13 mm, which lead to strain values equal to about 0.5%, 0.8%, and 1.1%. For each bending radius, the transfer curve of one transistor has been measured before the test and after 1, 10, 100, and 1000 bending cycles; the results of this analysis are presented in Figure 4. For what concerns the p-type devices, there is only a slight increase in the maximum current for increasing number of bending cycles, which is mirrored in the mobility values shown in Figure S6a (Supporting Information); overall, there is no significant change in performances after 1000 bending cycles. Considering n-type transistors, maximum current values stay almost constant up to 1000 bending cycles for applied strains below 1%, while for a 1.1% strain value the current and mobility values are unchanged up to 1000 bending cycles, while there is a small loss in performances after 1000 cycles, as it can be seen in Figure 4 and Figure S6b (Supporting Information).

The presented p- and n-type OFETs have been fabricated with the same techniques on the same substrates, employing identical electrodes and dielectrics. Therefore, their integration into complementary logic circuits is highly simplified. We started by fabricating a logic inverter, the simplest complementary circuit that can be realized, by integrating one p- and one n-type device. The inverter is fabricated by printing the two transistors with a shared drain contact and the same gate electrode, which act as output and input nodes, following the same fabrication steps presented for the transistor preparation (Figure 5a,b). Since the performances of the two different types of devices are not perfectly balanced, with the p-type transistors presenting slightly higher currents compared to the n-type ones, the channel width of the p-type devices ($W_p$) has been designed to be about one third of the n-type transistors' one ($W_n$), with $W_p = 300 \mu m$ and $W_n = 1000 \mu m$, while keeping the same channel length, $L_p = L_n = 65 \mu m$. The latter dimensions have been adopted for all complementary circuits in this work. First, a static characterization of the printed inverters has been performed. Voltage transfer curves (VTC) have been measured, sweeping the voltage input signal from a “0” logic state to a “1”; supply voltages ($V_D$) varying from 2 to 10 V have been used, and the so obtained VTC are plotted in Figure 5c as an average over the performances of five printed inverters.\textsuperscript{[45]} By finding the intersection point between the VTC and the bisector of the

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**Figure 4.** Bendability tests results. Transfer curves and maximum current values, recorded before bending and in flat configuration after 1, 10, 100, and 1000 bending cycles, for a,b) p-type and c,d) n-type devices. Transfer curves are presented for the case with an applied strain higher than 1%.
axes, an average inverting threshold voltage of 4.90 V has been obtained for devices operated at 10 V, with a standard deviation of 0.05 V. The inverters are functional down to a supply voltage of only 2 V, for which the average inverting threshold voltage amounts to 1.19 V, with a standard deviation of 0.07 V. The average gain values, obtained as the derivative of the VTC (Figure 5d), amount to about 14 for \( V_D = 10 \) V, with slightly higher values recorded for smaller input voltages. The maximum recorded gain is 17, and has been achieved with an input voltage of 2 V. The noise margins (NM), which give an estimation of the immunity of the printed inverters to noise on the input signal, have been calculated using the maximum equal criteria.\(^{[46]}\) NM lay in the range between 50% and 60% of \( V_D/2 \) for all supply voltages from 2 to 10 V, with the highest value obtained for \( V_D = 2 \) V, for which the average NM is equal to 0.62 V. The obtained figures of merit are ideal, indicating that low voltage complementary logic gates based on our printed transistors can be used in order to realize more complex integrated circuits.\(^{[45]}\)

The voltage transfer characteristics of these inverters show a small hysteresis, which can be related to the hysteresis shown by the single transistors and has already been addressed. This phenomenon is limited and reproducible, and thus doesn’t affect their correct operation.

In order to perform the dynamic characterization of these inverters, seven-stage ring oscillators (RO) have been fabricated (Figure 6a). An RO is a loop containing an odd number of inverters, where the output of an inverter is fed into the subsequent one, leading to its characteristic self-oscillation, whose frequency \( f_{\text{RO}} \) depends on the number of stages (\( N \)) and on the stage delay (SD), according to

\[
f_{\text{RO}} = \frac{1}{2N \cdot \text{SD}} \tag{1}
\]

The oscillating behavior of the circuit has been characterized, with supply voltages varying from 2 to 10 V, and results for three different supply voltages are presented in Figure 6c. The average oscillating frequency, evaluated on three different samples, goes from almost 6 Hz at 2 V to 57 Hz for a supply voltage of 10 V, leading to average stage delays of 13.1 ms and about 1.3 ms for supply voltages of 2 and 10 V, respectively (Figure 6b). The best performing circuit oscillates with a frequency of 62.5 Hz when a voltage supply of 10 V is applied, which leads a minimum stage delay achieved of 1.14 ms. At the best of our knowledge, this is the first demonstration of a printed, all-polymeric, transparent ring oscillator operating at low voltage.\(^{[8,47–50]}\)

We then proceeded to the fabrication of more complex logic circuitry, in particular we integrated the printed transistor in a D-Flip-Flop (DFF), one of the basic memory elements needed to build sequential logic circuits, counters and timers.\(^{[45,51–54]}\) This DFF has been implemented using a master-slave configuration, in which two D-latches (details in Supporting Information) are connected in series with opposite transparency phases. During its operation, this circuit retains the input data, and it adjusts the output according to the stored state only in correspondence of the falling edge of the clock signal; further details about the working mechanism can be found in the Supporting Information. For the circuit design we selected a pass-transistor based logic. This logic requires two main building blocks, the inverter, whose development and characterization has already been addressed, and the transmission gate. The latter is a logic
port acting as a switch, and in its typical design it is made of two complementary transistors with shared source and drain contacts, and with opposite signals driving the gate electrodes. In our design, aiming at a reduction of the number of transistors used in each circuit, we decided to use a single p-type transistor as transmission gate, instead of the complementary port, also because in this case there is no net gain in adopting the complementary pass gate.

As a consequence, our modified DFF design requires only 12 transistors. The schematic and the optical micrograph of our low-voltage transparent DFF are shown in Figure 7a,b. In Figure 7d,e the proper operational behavior of our devices is presented, for $V_D$ values equal to 10 V (d) and 2 V (e) (the operation of the D-latches sub-units is shown in Figure S8b,c, Supporting Information). One of the characteristic features of these devices is their transparency. We have thus evaluated the transmittance of the printed circuits by means of UV–vis spectroscopy in the visible range, and we have achieved a transmittance equal or higher than 90% for the overall system; in Figure S9 (Supporting Information) we show the spot on the circuit where this measurement has been performed. Taking into account the contribution of the PEN substrate, and normalizing the transmittance for the circuit alone, we can show that our printed circuits have a transpar-

cency equal or higher than 95% in the visible range, as it can be seen in Figure 7c. While previous low-voltage printed DFF has been presented in literature,\textsuperscript{(55–57)} this is the first example, to the best of our knowledge, of a low-voltage, all-polymer, transparent DFF, additionally obtained combining scalable processes.

We assessed the shelf-life stability of non-encapsulated printed circuits stored in nitrogen. After 4 months of storage the DFF are still perfectly operational (Figure 7f), thanks to the fact that characteristics of single transistors and inverters (Figure S7, Supporting Information) are negligibly altered.

3. Conclusions

We have demonstrated the integration of a parylene-based bilayer as top-gate dielectric for all-polymer, printed, transparent and low-voltage OFETs. Except for the dielectric, in which parylene was deposited through an already industrially scaled chemical vapor deposition method, all the functional layers were inkjet printed on a PEN substrate. We used P(NDI2OD-T2) and 29-DPP-TVT semiconducting co-polymers for n- and p-type transistors, respectively, and we have reported correct field-effect behavior down to 1 V. The printed OFETs achieve currents higher than 1 µA in both cases for operating voltages in the order of 10 V, with a high yield (99%) and uniform performances. The flexibility of these devices was assessed through bending tests, and it has been shown that they can sustain up to 1000 bending cycles with strains up to 1%.

We successfully demonstrated the integration of these transistors into complementary logic circuits. First, complementary inverters were fabricated, and well-balanced output characteristics were obtained, with NM equal or higher than 50% and an average gain of 14. Next, we demonstrated the first all-polymer, transparent, printed ring oscillators operating at voltages as low as 3 V, and achieving a maximum oscillation frequency of 62.5 Hz for a supply voltage of 10 V, thus showing a stage delay of 1.14 ms. Finally, we demonstrated all-polymer, transparent, printed D-Latches and D-Flip-Flops, correctly operating at voltages as low as 2 V. The transparency of these circuits is higher than 90% for the whole device has been obtained. Life-

shelf stability in nitrogen of non-encapsulated circuits exceeds 4 months after fabrication.

Our results show that it is possible to fabricate fundamental logic electronics blocks, as required in serialization circuits, timers and counters, through all-polymer, transparent OFETs on plastic capable of operating at voltages compatible with thin
film batteries or energy harvesters, paving the way to their integration into consumer products with low additional costs.

4. Experimental Section

Bottom-contact/top-gate organic field effect transistors, whose structure is presented in Figure 2a, were fabricated on a 125 μm-thick poly(ethylene 2,6-naphthalate) (PEN) substrate, purchased from Du Pont. Poly(3,4-ethylenedioxythiophene):polystyrene sulphonate (Clevios PJ700 formulation, purchased from Heraeus) source and drain contacts (Figure 2b) were inkjet-printed by means of a Fujifilm Dimatix DMP2831. This process allowed to fabricate transistors with a channel width of about 1000 μm and channel length in the order of 65 μm.

In order to facilitate the characterization of these devices, small pads of a silver nanoparticles-based ink were printed (Silverjet DGP-40LT-15C, purchased from Advanced Nano Products (ANP)) in correspondence of the points where electrical contacts with external probes were made during measurements. This was mainly related to the fact that these devices were transparent and it was thus quite difficult to characterize them without the help of clearly visible contact pads. All the devices presented in this work were fabricated with silver pads, but it was necessary to point out that they were not required for the actual operation of any of the circuits presented here.

For what concerns the n-type transistors, a PEI-based injection layer was printed on top of the contacts (Figure 2c). PEI (branched, purchased from Sigma Aldrich, average $M_w \approx 10\,000$), dissolved in water with a weight concentration of 0.2% (50 vol% of the final solution).

As semiconductors, P(NDI2OD-T2) (ActivInk N2200, Flexterra Corporation) was used for the n-type OFETs, and 29-DPP-TVT (synthesized according to Yu et al.[58]) for p-type devices. Both semiconductors were patterned by inkjet-printing (Figure 2d,e). P(NDI2OD-T2) was printed from a mesitylene-based solution, with a concentration of 7 mg mL$^{-1}$, while 1,2-dichlorobenzene was used as solvent for 29-DPP-TVT, to yield a concentration of 2.5 mg mL$^{-1}$. After printing, annealing in nitrogen atmosphere was performed; P(NDI2OD-T2) was annealed for 3 h at 120 °C, while 29-DPP-TVT for 5 min at 110 °C.

The bilayer dielectric stack was composed of a thin PMMA layer (purchased from Sigma Aldrich, average $M_w = 120\,000$), and a thicker parylene-C layer (dimer purchased from Specialty Coating Systems). The thickness of the PMMA layer was in the order of 20 nm, while the parylene-C layer was about 100 nm thick. The PMMA layer was spin-coated and annealed at 100 °C for 1 h in a nitrogen atmosphere, while parylene-C was deposited by means of chemical vapor deposition, using a SCS Labcoater 2—PDS2010 system. Parylene dimer underwent pyrolysis inside the furnace chamber at about 690 °C, while deposition was performed at room temperature, with a pressure in the chamber in the order of 15 mTorr. PEDOT:PSS gate contacts were inkjet printed on top of the dielectric layer (Figure 2f). For what concerns circuits, via-holes contacting different conductive layers were fabricated by either by laser or chemical drilling.
The characterization of the transistors and circuits was performed in an inert nitrogen atmosphere. The transfer and output curves for the transistors, together with the voltage transfer curves for the inverters, were measured using an Agilent B1500A Semiconductor Parameter Analyzer. The dynamic characterization of the integrated circuits was performed using the above-mentioned Semiconductor Parameter Analyzer for recording the output signals, while the input signals and the voltage supply were provided by an Agilent 81150A waveform generator and an Agilent B2912A source meter. For what concerns the dielectric characterization, an Agilent 4294A impedance analyzer was employed.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest
The authors declare no conflict of interest.

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