Performance Prediction for Coarse-Grained Locking

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A standard design pattern found in many concurrent data structures, such as hash tables or ordered containers, is an alternation of parallelizable sections that incur no data conflicts and critical sections that must run sequentially and are protected with locks. A lock can be viewed as a queue that arbitrates the order in which the critical sections are executed, and a natural question is whether we can use stochastic analysis to predict the resulting throughput. As a preliminary evidence to the affirmative, we describe a simple model that can be used to predict the throughput of coarse-grained lock-based algorithms. We show that our model works well for CLH lock, and we expect it to work for other popular lock designs such as TTAS, MCS, etc.

1 ABSTRACT COARSE-GRAINED SYNCHRONIZATION

Conventionally, the performance of a concurrent data structure is evaluated via experiments, and it is notoriously difficult to account for all significant experimental parameters so that the outcomes are meaningful. Our motivation here is to complement experimental evaluation with an analytical model that can be used to predict the performance rather than measure it. As a first step towards this goal, in this work, we attempt to predict the throughput of a class of algorithms that use coarse-grained synchronization.

Consider a concurrent system with \( N \) processes that obey the following simple uniform scheduler: at every time step, each process performs a step of computation. This scheduler, resembling the well-known PRAM model [5], appears to be a reasonable approximation of a real-life concurrent system. Suppose that the processes share a data structure exporting a single operation. If the operation induces a work of size \( P \) and incurs no synchronization, the resulting throughput is \( N \cdot \frac{\alpha}{P} \) operations in a unit of time: each process performs \( \frac{\alpha}{P} \) operations in a unit of time, where \( \alpha \) indicates the amount of work that can be performed by one process in a unit of time. One way to evaluate the constant \( \alpha \) experimentally is to count the total number \( F \) of operations, each of work \( P \), completed by \( N \) processes in time \( T \). Then we get \( \alpha = \frac{F}{NP} \). The longer is \( T \), the more accurate is the estimation of \( \alpha \).

Now suppose that, additionally, the operation performed by each process contains a critical section of size \( C \). In the operation, described in Figure 1, every process takes a global lock, performs the critical section of size \( C \), releases the lock and, finally, performs the parallel section of size \( P \).

Here, as a unit of work, we take the number of CPU cycles spent during one iteration of the loop in Lines 3-4 or 6-7. The iteration consists of a nop instruction, an increment of a local variable and a conditional jump, giving us, approximately, four CPU cycles in total.
operation():
    lock.lock()
    for i in 1..C:
        nop
    lock.unlock()
    for i in 1..P:
        nop

Fig. 1. The coarse-grained operation

2 MODEL ASSUMPTIONS

Below we list basic assumptions on the abstract machine used for our analytical throughput prediction.

First, we assume that coherence of caches is maintained by a variant of MESI protocol [7]. Each cache line can be in one of four states: Modified (M), Exclusive (E), Shared (S) and Invalid (I). MESI regulates transitions between states of a cache line and responses depending on the request (read or write) to the cache line by a process or on the request to the memory bus. The important transitions for us are: (1) upon reading, the state of the cache line changes from any state to S and, if the state was I, then a read request is sent to the bus; (2) upon writing, the state of the cache line becomes M, and, if the state was S or I, an invalidation request is sent to the bus.

We assume that the caches are symmetric: for each MESI state st, there exist two constants Rs and Ws such that any read from any cache line with status st takes Rs work and any write to a cache line with status st takes Ws work. David et al. [4] showed that for an Intel Xeon machine (similar to the one we use in our experimental validation below), given the relative location of a cache line with respect to the process (whether they are located on the same socket or not), the following hypotheses hold: (1) writes induce the same work, regardless of the state of the cache line; (2) swaps, not concurrent with other swaps, induce the same work as writes. Therefore, we assume that (1) W = W_M = W_E = W_S = W_I and (2) any contention-free swap induces a work of size W.

3 CLH LOCK

Multiple lock implementations have been previously proposed, from simple spinlocks and TTAS to more advanced MCS [6] and CLH [3]. For our analysis, we choose CLH, as the simplest lock among those considered to be efficient. In Figure 2, we inline lock and unlock calls to CLH lock in our abstract coarse-grained operation.

3.1 Cost of an operation

Let us zoom into what happens during the execution of the operation.

Note that at the beginning of an operation (unless it is the very first invocation), my_node.locked is loaded into the cache and the corresponding cache line is in state M, because of the set in Line 15 during the previous operation by the same process.

(1) The operation starts with swap (Line 9) that induces a work of size W, if not concurrent with other swaps, and a work of size at most X, otherwise.

(2) In Line 10, the algorithm loops on a field next.locked. During this loop one or two cache misses happens.

One cache miss can happen at the first iteration of the loop if the read of locked returns true. The last process that grabbed the lock already invalidated this cache line in Line 15 during its penultimate operation. MESI reloads the cache line and changes its state from I (or none if it was not loaded previously) to S.
class Node:
    bool locked

Node head = new Node() // global
Node my_node // per process
my_node.locked ← true

operation():
    Node next ← swap(&head, my_node) // W or X
    while (next.locked) {} // R1 or 2 · R1
    for i in 1..C: // C
        nop
    my_node.locked ← false // W
    my_node ← next
    my_node.locked ← true // W
    for i in 1..P: // P
        nop

Fig. 2. The coarse-grained operation with inlined lock and unlock functions

The other cache miss happens in every execution when the operation reads next.locked and
gets false. In this case, the cache line was invalidated in Line 13 during the last operation of the
last process that grabbed the lock. MESI reloads the cache line and changes its state from I (or
none) to S.

Each of the described cache misses induces the work of size $R_I$. Thus, the work induced in Line 10
is of size of $R_I$ (if only the second miss happens) or $2 · R_I$ (if both misses happen).

(3) In Lines 11-12, the critical section with work of size $C$ is performed.
(4) In Line 13, my_node.locked is set to false. There are two cases: if my_node.locked is not yet
loaded by any other process in Line 10 then the state remains $M$; otherwise, MESI changes the state
from $S$ to $M$ and sends a signal to invalidate this cache line. In both cases, the induced work is of
size $W$.

(5) In Line 14, the operation performs an assignment on local variables, without contributing to the
total work.

(6) In Line 15, my_node.locked is set to true. From the end of the while loop at Line 10 the
corresponding cache line is in state $S$. MESI changes the state to $M$ and sends a signal to invalidate
this cache line inducing work of size $W$.

(7) In Lines 16-17, the parallel work of size $P$ is performed.

3.2 Evaluating throughput

To evaluate the throughput of the resulting program under the uniform scheduler, take a closer
look on how $N$ processes continuously perform the operation from Figure 2.

Process 1 executes: its first swap (taking at most $X$ units); the critical section (blue, Lines 10-13):
acknowledges the ownership of the lock by reading false in Line 10 (takes $R_I$ units), performs
the work of size $C$ and releases the lock in Line 13 (takes $W$ units); the parallel section (red,
Lines 15-17 and 9): sets my_node.locked to true (takes $W$), performs the work of size $P$, performs
a non-contended swap (takes $W$) and, possibly, reads true in Line 10 (takes $R_I$). (Here, the swap
operation performed after the very first completed critical section is counted in the parallel work,
as it is executed in the absence of contention.) Every other process $i$ operates in the same way: it
swaps as early as possible (taking at most $X$), waits until process $i - 1$ releases the lock, and then
performs its critical (blue) and parallel (red) sections.

Depending on the parameters $N, C, P, W$, and $R_I$, two types of executions are possible.
In case 1 (Figure 3a), at the moment when process 1 finishes its parallel section, process N already finished its critical section, i.e., \( P + 2 \cdot W > (N - 1) \cdot (C + R_I + W) \). Therefore, in the steady case, at every moment of time, each process do not wait and execute either the parallel or critical section, and the read in Line 10 cannot return true because the lock is already released. Thus, the throughput, measured as the number of operations completed in a unit of time, equals to \( N \cdot \frac{\alpha}{(P + 2 \cdot W) + (C + R_I + W)} \).

In case 2 (Figure 3b), before proceeding to the next operation, process 1 has to wait until process N completes its critical section from the previous round of operations; process 2 waits for process 1, process 3 waits for process 2, etc. Thus, there is always some process in the critical section, giving the throughput of \( \frac{\alpha \cdot N}{C + R_I + W} \).

Therefore, given the number of processes \( N \), the sizes \( C \) and \( P \) of critical and parallel sections, the throughput can be calculated as follows:

\[
\begin{align*}
\text{if } P + 2 \cdot W &\leq (N - 1) \cdot (C + R_I + W) \\
\frac{\alpha}{C + R_I + W} &\quad \\
\frac{\alpha \cdot N}{(P + 2 \cdot W) + (C + R_I + W)} &\quad \text{otherwise}
\end{align*}
\]

4 EXPERIMENTS

For our measurements, we used a server with four 10-core Intel Xeon E7-4870 chips of 2.4 GHz (yielding 40 hardware processes in total), running Ubuntu Linux kernel v3.13.0-66-generic. We compiled the code with MinGW GCC 5.2.0 (with -O0 flag to avoid compiler optimizations, such as function inlining, that can screw up our benchmarking environment). The code is available at [https://github.com/Aksenov239/complexity-lock-with-libslock](https://github.com/Aksenov239/complexity-lock-with-libslock).

We considered the following experimental settings: the number of processes \( N \in \{5, 10, 20, 30, 39\} \); the size of the critical section \( C \in \{100, 500, 1000, 5000, 10000\} \); and the multiplier \( x \in [1, 150] \) (we
choose all integer values) that determined the size of the parallel section $P = x \cdot C$. For each setting, we measured the throughput for 10 seconds. Our experimental evaluation gives $a \approx 3.5 \cdot 10^5$, $W \approx 40$, and $R_I \approx 80$. The ratio between $W$ and $R_I$ correlates with the experimental results provided by David et al. [4].

In Figure 4 we show our experimental results for three settings with $N = 39$ and $C \in \{100, 500, 5000\}$ (blue curves) compared with our theoretical prediction (red curves). The two curves match very closely, except for the case of small $C$ and $P$ where our predicted throughput underestimates the real one. We relate this to the fact that we oversimplified the abstract machine: any write induces the work of constant size $W$, regardless of the relative location of the cache line with respect to the process. For small $C$ and $P$ two processes from the same socket are more likely to take the lock one after the other and, thus, on average, a write might induce less work than $W$, and, consequently, the throughput can be higher than predicted.

5 COMPARISON WITH PRIOR WORK

In this work, we proposed a very simple, not to say simplistic, analytical framework intended to predict the performance of a class of lock-based algorithms. A more involved analysis has been earlier proposed by Atalar et al. [1] for a similar class of lock-free concurrent data structures (Figure 5). There the concurrent processes alternate the constant size parallel work with constant-size critical work and synchronize critical operations on the shared data using read and compare&set operations on a dedicated access point.

By adapting the code to our notations, we get:

```plaintext
1 operation():
2   parallel_work()
3     while !success do
4       current ← read(AP)
5       new ← critical_work(current)
6       success ← compare&set(AP, current, new)
```

In order to have the critical work of size $C$ we had to have the critical loop of size $C - 1$, because in each iteration of the loop we increment the variable i and after the loop we increment the thread local variable it.

We argue that the two approaches, ours and by Atalar et al. [1] though seemingly quite similar, bear some important differences. In particular, these differences, do not allow us to treat our analytical framework as a special case of that in [1].

Note that we do not consider here the more general analysis in a later paper by Atalar [2] in which the amounts of parallel and critical work are treated as random variables obeying specific
distributions. The analysis in [2] is a probabilistic generalization of that in [1]. Therefore, it appears that, for the sake of comparison, we can focus on the deterministic framework of [1].

Two types of conflicts happen in the described lock-free algorithms:

- **logical conflicts** — the unsuccessful retry Lines 4-6, i.e., a “fast” process succeeds in updating the access point variable \( AP \), causing “slower” process to fail in their compare&set operations;
- **hardware conflicts** relates here to the serialization of concurrent reads at Line 4 and compare&set at Line 6 on \( AP \).

At the same time, our lock-based algorithms are subject only to hardware conflicts on head variable (Figure 2 Line 9).

At first, let us look on the two types of algorithms from the high-level point of view. Lock-based algorithms are *conservative* in the sense that the critical section is performed only when the lock is taken and the actions of the critical section always “take place”. In particular, this kind of algorithms is only subject to hardware conflicts.

In contrast, lock-free algorithms are *speculative*: a critical section can be performed several times before it succeeds and only the actions of the successful instance are effective. In analysing these algorithms, we should account for both logical and hardware conflicts.

Under high contention, speculative data structures perform worse than conservative ones due to the overwhelming number of retries critical sections. Intuitively, this suggests that we should use different analyses to reason about the throughput of these two classes of algorithms.

In what follows, we suppose that \( P \) and \( C \) exceed the cost of the swap operation. Such condition greatly simplifies the analysis for lock-based data structures since we do not have to deal with hardware conflicts.

Under high contention, i.e., when \( P \) is comparatively small, \( P < (n-1) \cdot C \), we use the special properties of the lock-based algorithms: with these parameters there is always some process in the critical section and, consequently, this allows us to easily evaluate the resulting throughput.

In contrast, the analysis of the performance of lock-free algorithms under high contention in [1] is considerably more involved, due to the intrinsic interleaving of hardware and logical conflicts.

When contention is small and conflicts are unlikely, the two analyses for fixed \( P \) and \( C \) should coincide. Both of them provide us with the throughput approximately equal to \( \frac{N^2}{P \cdot C} \) where \( \alpha \) is some constant and \( N \) is the number of threads.

To summarize, in the case of CLH Lock the analysis for lock-based algorithms coincide with the analysis for lock-free programs for the settings with small contention, while in other settings our analysis is much simpler due to the special properties of the lock-based algorithms.

Furthermore, we consider the MESI cache-coherence protocol [4]. Our analysis is further simplified by assuming that writes take the same time no matter in which state a cache line is: there are evidences that this is indeed the case for our machine. However, the situation might get more complicated for other machines in which, e.g., the write complexity depends on the cache state, which might result in a more complicated analysis.

If the CLH lock in conservative programs is replaced with a lock of another type, e.g., test&test&set, ticket, spin lock, MCS, etc., the analysis becomes somewhat more complicated but it still shares the part when \( P \geq (n-1) \cdot C \).

For example, suppose that we replace CLH lock with spin lock:

```plaintext
1 operation():
2     while !success:
3         success = compare&set(locked, 0, 1)
4     for i in 1..C:
5         nop
```

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locked = 0

for i in 1..P:
    nop

Here we have hardware conflicts not only on compare&set, but also on the write locked = 0. These conflicts are not considered by the analysis of lock-free programs and, thus, there should be a different analysis for the coarse-grained programs with spin lock.

To summarize, the two analyses, though designed using similar arguments, are distinct.

6 CONCLUSION

In this short note, we showed that a simple theoretical analysis may quite accurately predict the throughput of data structures implemented using coarse-grained synchronization. For the moment, our analysis is restricted to algorithms using CLH-based locking in systems obeying the uniform scheduler. In upcoming work, we intend extend the analysis to more realistic algorithm designs, lock implementations and architectures.

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