STAM: System level state-machine-based thermal behavior analysis for multicore processor

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Abstract: As the density of transistors is increased, the processor suffers from not only high power consumption but also high temperature. We presented the system level thermal behavior analysis model (STAM) which uses minimum physical characteristics and activities for components of the processor to obtain thermal behaviors. STAM employs the state-machine-based model for a thermal transient response. The results show that STAM is more than three orders of magnitude faster than the existing temperature estimation tool, with about a 6% average error to find hotspots.

Keywords: thermal analysis, system level design, state-based modeling

Classification: Electron devices, circuits, and systems

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1 Introduction

The power consumption per circuit area (e.g., power density), is increased, since the density of transistors in a die is increased. The temperature is directly
determined by the power density of the processor [1]. In addition, distributions of transistors in a die differ locally according to their functionalities. There are places called hotspots that have a high temperature than other places. These hotspots lead to various thermal problems, including increased power consumption, failures due to the different delays between components, and lifespan reduction due to thermal fatigue, etc. As a result, thermal analysis of the processor becomes a major challenge. HotSpot [1] is an architecture-level thermal simulator using power consumption values, thermal resistances and capacitances as parameters to estimate the temperature. These parameters are available at later design stages and the simulation time is about at least several milliseconds per sample time [1]. In addition, HotSpot requires a power consumption estimation method such as McPAT [2] for estimating changes in temperature. This is an overhead to slow the simulation speed. HotSpot can be used for worst-case thermal simulation that uses the peak power of the processor, but is not suitable for tracing thermal behaviors every short sampling period at the system level of abstraction. Other relevant studies on thermal analysis have focused on accurate thermal estimation to manage the temperature of the processor. These methods estimate the real temperature accurately, but their simulation time is slow and they require many physical characteristics as parameters and/or implemented thermal sensors to acquire the heat information of the die [3, 4]. Because it is difficult to obtain these low level parameters at early design stages, we need a system level analysis method to determine the thermal behavior of the processor. In this paper, we proposed the system level thermal behavior analysis model, STAM, using the thermal state machine (TSM) model. TSM is a state-machine-based model used to determine the thermal transient responses of components on the processor.

2 Framework of STAM

The thermal behavior of the component is determined from the physical characteristics related to heat generation and power consumption. The circuit area and power consumption determine the power densities that are directly affected by the temperature [1]. Generally, this information is not available at the early design stages such as system level design processes. It is easy to explore the design space at the system level to determine the thermally-optimized design by using thermal management algorithms. Also, a new metric is required that can evaluate the algorithms at early design stages. Therefore, we defined the system level metric

![State transitions of thermal state machine](https://example.com/state-machine-diagram.png)

**Fig. 1.** State transitions of thermal state machine
of the thermal degree, $T_B$, which is a counterpart of temperature. $T_B$ is a unitless value which is not directly comparable with the temperature degree such as Kelvin or Celsius. However, it can still be used to compare thermal degrees between components. To obtain $T_B$, we use TSM. TSM is a finite state machine model used to determine the thermal state based on the activity level of the component. The activity level is profiled data obtained from selected events in the component during certain time period. TSM has four states. Each state represents the four thermal states of the temperature transient model. Fig. 1 shows a diagram of TSM with each transition condition. The details of each state are as follows.

i) **IDLE**: no activity, no $T_B$ value. This state can only transit from the COOLING state and to the HEATING state.

ii) **HEATING**: activity is greater than a threshold value. The $T_B$ increases exponentially. This state can transit from all states and to OVERHEATING, COOLING, and to itself. Internal stages are increased at every recursive state transition.

iii) **OVERHEATING**: activity is kept high for a period. The $T_B$ has a maximum value. This state can only transit from HEATING state and to COOLING state.

iv) **COOLING**: activity is less than a threshold value. The $T_B$ decreases exponentially. This state can transit from HEATING and OVERHEATING states and to IDLE state only.

OVERHEATING state is a model of the positive feedback between the temperature and leakage current. However, this phenomenon is difficult to model at the system level due to the lack of information. Therefore, we use the constant value that indicates the final $T_B$ in our equation. State transition occurs due to the activity level during simulation and its status is sent to the TSM manager. The TSM manager is the separated system level module that manages all TSMs of the processor. Each component has one of the four thermal states for every sample time. The TSM manager calculates $T_B$ using previous and current states data with pre-defined parameters such as the heating/cooling table and ratio of the area. The heating/cooling table is a simplified model of the temperature transient response. Single stage lumped model for temperature transient response $T_i$ of component $i$ at time $t$ can be simplified as follows [5]:

$$T_i(t) = P_i(t) \cdot R_{th,i}(1 - e^{-t/\tau})$$

$$= P_i(t) \cdot \frac{d}{\kappa \cdot A_i} (1 - e^{-t/\tau})$$

$$= \frac{P_i(t)}{A_i} \cdot a(1 - e^{-t/\tau})$$

(1)

where, $R_{th,i}$ denotes the thermal resistance and $\kappa$ is the thermal conductivity of the component. $P_i$ and $A_i$ are the power consumption at time $t$ and the circuit area of the component, respectively. $d$ is the thickness of die and $\tau$ is the time constant. The power density is the power consumption divided by the circuit area, and it determines the final temperature of the component when sufficient time has lapsed. A time constant $\tau$ obstructs the temperature to reach the final value. This makes the temperature increases exponentially. A time constant $\tau$ is obtained by multiplying the thermal capacitance by the thermal resistance. As mentioned above, the
physical characteristics are usually not available at the system level. Thus, we assumed that the thermal conductivity $\kappa$ and the time constant $\tau$ are the same for all components under the same technology and the same materials. We replaced $d/\kappa$ with $\alpha$. The heating/cooling table provides rates of $T_B$ increment/decrement. The rates are calculated using $1 - e^{-t/\tau}$ in Eq. (1) with the pre-defined value of $\tau$. From these tables, the thermal behavior $T_B$ is increased and decreased exponentially similar to a thermal transient response when the component is in the HEATING/COOLING state. We considered the impacts of area for thermal behavior using the relative area ratio between components. The ratios of the area between components are defined in the TSM manager. These ratios determine the maximum $T_B$ for each component.

3 Thermal behavior analysis using STAM

The processes of STAM are as follows. Each component counts the activities during the time period. The activities level is determined by a performance counter or access signals such as transaction messages. After each time period, a state transition occurs according to the activity level of each TSM. The TSM manager collects the states of all components and calculates the $T_B$ for all components with the previous stored data. The formulas to calculate $T_B$ at each state are as follows:

$$T_{B,IDLE,i}(t) = 0$$

$$T_{B,HEATING,i}(t) = R_{Area,i} \cdot R_{Activity,i}(t) \cdot f_{HEATING}(n_{stage})$$

$$T_{B,OVERHEATING,i}(t) = R_{Area,i} \cdot R_{Activity,i}(t)$$

$$T_{B,COOLING,i}(t) = T_{B,COOLING,i} \cdot f_{COOLING}(n_{stage})$$

where, $R_{Area,i}$ is the ratio of the area of component $i$ to the reference component. $R_{Activity,i}$ denotes the activity level of the component $i$ during the unit time period. Function $f$ returns the rates of the $T_B$ increment/decrement from the heating/cooling table in the TSM manager when the state of the component is at the HEATING or COOLING state. The input of $f$ is a current stage number $n_{stage}$ of the state. $T_B$ is zero in the IDLE state. In the HEATING state, $T_B$ is the product of $R_{Area,i}$, $R_{Activity,i}$, and $f(n_{stage})$. $T_B$ increases exponentially to the maximum value according to the area and the activity level. When the state is in OVERHEATING, a $T_B$ has the maximum value. However, this maximum value still depends on the area and the activity level. Incidentally, the formulas of the COOLING state differ to those of other states. Under this state, heat generation does not occur in the component. The $T_B$ value falls to zero exponentially according to the heating/cooling table from the current value. Thus, the $T_B$ value should be stored in the TSM manager as a reference maximum value when the component transits to the COOLING state at that time. Fig. 2 illustrates the pseudo code of the TSM manager and the STAM used to obtain the $T_B$ during simulation. The TSM manager and TSMs are implemented in the gem5 simulator [6] to collect the statistics directly. The TSM manager calculates $T_B$ at each time period for all components. Fewer overheads are available for obtaining thermal behavior; thus, $T_B$ is calculated at the run-time during simulation. As $T_B$ is unitless, it is difficult to compare with the temperature directly. However, the relative comparison between components over
time can be compared with these two metrics. Using STAM, the designer can distinguish the hotspots for components over time during simulation. This approach is useful for resolving the temperature gradient problems.

4 Experiments

We compared the hotspots found using the existing open-source temperature simulator HotSpot with those found using STAM by using the architectural platform simulator, gem5. We built the homogeneous multicore system using ARMv7 architecture on the gem5 simulator with the PARSEC benchmark suite [7] for multicore systems. Since power consumption values cannot be obtained directly from the gem5 simulator, we use the statistics results of gem5 as an input to the McPAT power consumption model for the HotSpot simulator. For comparison, we set the threshold as a thermal constraint for both results. The thermal threshold is set at 70% of the maximum value. If temperatures or the TBs exceed the threshold, it is assumed that components become hotspots. Four cores have 17 components, with a total of 68 components. Table I illustrates periods of hotspots that exceed the thermal threshold during the simulation time for the instruction buffer (IB), instruction decoder (ID), instruction translation look-a-side buffer (ITLB), and data translation look-a-side buffer (DTLB) of two of the cores. The time overhead refers to the calculation time without the time spent for the gem5 simulation. Since the overheads for the power consumption estimation are iteratively added every sample time, HotSpot simulation is slower than STAM.

Table I. Periods of hotspots of sampled components that exceed thermal threshold during simulation time

| Component | HotSpot [ms] | STAM [ms] | Error [%] |
|-----------|--------------|-----------|-----------|
| IB1       | 5.13 × 10²   | 205.60    | 1.79      |
| IB2       | 5.13 × 10²   | 205.60    | 1.79      |
| IB3       | 5.13 × 10²   | 205.60    | 1.79      |
| ID1       | 205.44       | 205.44    | 0.00      |
| ID2       | 205.44       | 205.44    | 0.00      |
| ID3       | 205.44       | 205.44    | 0.00      |
| ITLB1     | 0.00         | 0.00      | 0.00      |
| ITLB2     | 0.00         | 0.00      | 0.00      |
| ITLB3     | 219.06       | 219.06    | 0.00      |
| DTLB1     | 218.56       | 218.56    | 0.00      |
| DTLB2     | 0.00         | 0.00      | 0.00      |
| DTLB3     | 39.84        | 39.84     | 0.00      |
However, STAM estimates thermal behaviors using activity levels without power consumption values. While excluding the gem5 run time, STAM gives the improved simulation speed of more than three orders of magnitude faster than the one of HotSpot analysis with McPAT traces. IBs and IDs exceed the thermal threshold for almost the entire total simulation time. The results for ITLB differ between HotSpot and STAM, with about 16 error rates. In HotSpot, while the temperatures of ITLBs are close to the thermal threshold, they do not exceed it. On the other hand, in STAM, the ITLBs exceed the thermal threshold. Figs. 3(a) and 3(b) show the simulation results using HotSpot and STAM with four selected components that have large spaces. Figs. 3(c) and 3(d) illustrate the average thermal map of HotSpot and STAM during simulation. The results of HotSpot and STAM concur for 57 components. The average error is 5.49% and the maximum error is about 17% for 11 components, except the matched components.

5 Conclusion

In this paper, we presented STAM, the thermal behavior analysis model, using TSM for system level design. We proposed TSM, a state-machine-based thermal behavior model, using ratios of the area and activity levels. The thermal behaviors of the processor cores are obtained from an early stage system design in order to manage thermal problems. Using STAM, the trends of the thermal behaviors are more than three orders of magnitude faster than the well-known thermal simulator. The average worst-case error is about 17% and the average error is 5.49%.