In-sensor time-domain classifiers using pseudo sigmoid activation functions

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ABSTRACT
This work presents an ultra-low-power classifier that can be integrated within energy-constrained bio-sensors to enable rapid analysis for continuous health monitoring. The in-sensor classifier saves significant transmission energy by extracting critical information locally to eliminate the need of transmitting raw data to centralized servers for remote signal processing. The convolutional-neural-network (CNN)-based classifier is built by using reconfigurable delay-locked loops (DLLs) to carry out classification algorithms with time-domain multiply-accumulate (MAC) operations. Pseudo sigmoid activation functions are realized by regenerative comparators that transform weighted timing to probabilities. The presented classifier achieves low-power consumption of 240.34 nW while performing up to 20 k operations per second. The proposed time-domain classifier reduces the energy to 36% of the previous works.

1. Introduction

To continuously monitor health conditions, distributed sensors are designed to capture and transmit psychological signals, such as electrocardiogram (ECG) or electroencephalogram (EEG), to the cloud for anomaly analysis, which is of great clinical importance. For example, hypertension accounts for about 25% of heart failure cases [1]. Real-time monitoring can be utilized to predict the emergency cases and diagnose the diseases before they become worse. That brings new challenges for pervasive edge sensors to enable the always-on feature for real-time tracking because transmitting raw data of the acquired signals to the aggregator burns a tremendous amount of energy. Comparing to full-waveform transmission, in-sensor computing or machine learning can be performed at edge sensors to extract critical features in situ and that further reduces volumes of transmission data [2–4]. In this way, only classified results will be sent to the aggregator, so transmission energy can be highly decreased to enable continuous monitoring.

Sensory interfaces to acquire EEG or ECG signals usually require more than 16-bit resolution [5]. High-performance analog-to-digital converters (ADCs) are often used to convert captured signals to digital data for digital signal processing (DSP). Automatic bio-signal analysis with statistical learning has been utilized for several years. Those digital architectures can be used as powerful accelerators [6–8]. However, machine learning operations are computationally expensive with modern computing systems for edge sensors. Moreover, they all require data converters, including ADCs and digital-to-analog converters (DACs) to interface with the sensors [9,10]. Recently, computational transformation can be embedded into ADCs to execute multiplying operations

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and to complete classification with backend processing [11–13]. To emulate biological sensory systems that are considered the most energy-efficient computers with analog signal processing [14], this paper utilizes CNN to enable direct classification in analog domain without sending data to or retrieving data from central processing units (CPUs) through data conversion to enhance data movement.

In order to decrease the energy consumption to its limits, lowering power supply voltages is an efficient approach. In this way, bio-sensors may use the energy harvested from the environment with the lowest maintenance [15]. As the CMOS technology is scaled down, the power supply is also scaled down to prevent the gate oxide from breakdown. While technology scaling with improved power and performance characteristics has brought tremendous benefits to digital circuits, the analog circuit design is becoming challenging due to the reduced intrinsic gain and limited headroom. Representing signals in time domain to achieve required resolution is beneficial because the unit delay of minimum-sized devices becomes finer with scaling. Hence, processing signals in time domain overcomes the difficulties of signal processing in voltage domain.

The presented approach focuses on signal processing in time domain to address low-headroom issues so that time-domain classification can be performed under low supply voltages to achieve better energy efficiency and benefit from technology scaling. Nevertheless, the greatest benefit along with the technology scaling is the increase of transit frequency and the decrease of propagation delay. Excellent timing accuracy is easily achieved when the transition time reaches the order of less than 10 ps? Meanwhile, smaller parasitic capacitance which comes from the smaller transistor size can decrease transition energy. Therefore, in order to get the most benefits from the progress of processes, digitizing more mixed-signal blocks to operate in time domain is an efficient method [16, 17].

2. Time-domain classifier

Extracting all of the features is very power consuming and impossible to be realized in the edge sensors. To achieve lower power consumption, mixed-signal classification structures with primary feature extraction
shown in Fig. 1 exploit time-domain multiplication and summation to perform the following inner-products

$$V_{out} = \sum_{i=1}^{N} (W_iX_i)$$  \hspace{1cm} (1)

Pseudo-sigmoid activation functions that are generated with regenerative comparators [18] calculate the likelihood for forward propagation of signals. A multi-layer neural network for classification with the proposed pseudo-sigmoid function is adopted in the paper. As the number of neurons grows to more than 200, the mean squared error increases significantly. Therefore, the structure with 100 neurons at each layer for 2 hidden layers is utilized with considering the accuracy and hardware overhead. Offline training to derive the weights is employed for further reduction of power consumption. Although rectified linear activation unit (ReLU) is popular in the CNN implementation recently because it is simple and can be easily implemented in the software-oriented classification. However, to implement it in the sensors in analog domain, it needs amplifiers with the closed-loop configuration to accomplish the linear part. The closed-loop amplifiers need large power consumption and supply headroom to achieve high linearity. It would lead to difficulties to integrate the classifiers into sensor front-end circuits, especially in advanced technology nodes. Therefore, the pseudo-sigmoid activation function is utilized in the proposed structure for better integration. The problem of vanishing gradients that nonlinear activation functions encounter in deep neural networks does not cause problems in this structure since the adopted structure only contain 2 hidden layers. The circuit designs to carry out classification algorithms are described below.

### 2.1. Multiplication

The circuit block and timing diagram of a time-difference amplifier are shown in Fig. 2. The time difference, \(\Delta t_m\), between the input signals \(V_{in1}\) and \(V_{in2}\) is amplified through the delay propagation. A delay-locked loop (DLL) is used to reduce the sensitivity over process, voltage, and temperature variations, so that the output signals with the precise \(N\) times of input time difference can be generated.

There are two delay lines in the circuit, and each delay line contains \(N + 1\) identical delay cells. The delays of cells in the constant delay line (CDL) are static during operation. However, the delays of cells in the voltage-controlled delay line (VCCL) are controlled by the \(V_{CTRL}\) signal generated by the feedback loop.

The input signals, \(V_{in1}\) and \(V_{in2}\), have the same clock periods, but with a time difference, \(\Delta t_0\). Output signals, \(V_{out1,0}\) and \(V_{out2,0}\), are connected to the phase/frequency detector (PFD), so the time difference between \(V_{out1,0}\) and \(V_{out2,0}\) are sensed by the PFD. UP/DN signals are generated according to the time difference and used in the charge pump (CP) to control currents for charging/discharging the loop filter. The resulted \(V_{CTRL}\) is used to modify the delay of VCDL to force \(V_{out1,0}\) to be in the same phase as \(V_{out2,0}\). As described above, the delay cell \(D_{V1}\) and \(D_{V0}\) are equally sized, so as \(D_{C1}\) and \(D_{C0}\). Therefore, the \(V_{out1,1}\) is one \(\Delta t_0\) ahead of \(V_{out2,1}\) instead of behind it. Then, \(V_{out1,2}\) is 2 times of \(\Delta t_0\) ahead of \(V_{out2,2}\), and \(V_{out1,N}\) is \(N\) times of \(\Delta t_0\) ahead of \(V_{out2,N}\).

To achieve higher resolution, the circuit is extended for more weight selections and a larger input range. \(M\) delay cells \((D_{A0} - D_{AM} \text{ and } D_{B0} - D_{BM})\) are integrated in the delay-locked loop as shown in Fig. 3. The fine delay cells are used to divide the input time difference \(\Delta t_m\) to \(\Delta t_0/M\) as a unit delay that extends the input range by \(M\) times. Connecting \(V_{out1,1-N}\) and \(V_{out2,1-N}\) with two N-to-1 MUXs, the weights of \(\Delta t_m\) can be reconfigured to accomplish the multiplication. Therefore, the output time difference can be expressed as

$$\Delta t_{out} = N \times \Delta t_0.$$  \hspace{1cm} (2)

Fig. 4 (a) illustrates the details of how the time difference between CLK1 and CLK2 is sensed through the PFD module. True-Single-Phase-Clock (TSPC)-based PFD is used for operating under low power supply.

![Fig. 4](image_url)
voltage [19]. While a rising edge on CLK 1 turns on M 5, the drain of M 5 is discharged so that DN goes high. In the same way, a rising edge on CLK 2 discharges the drain of M 11, so that UP goes high. Reset is triggered when both drain of M 5 and M 11 go low to discharge the drain of M 3 and M 9. It leads to forcing the drain of M 5 and M 11 to go high. Therefore, if CLK 1 is ahead of CLK 2, the PFD sends out UP signal. If CLK 1 is behind of CLK 2, the DN signal is sent out.

2.2. Summation

To perform the inner-product operations, it requires the summation of several weighted time differences. Fig. 5 shows the presented time-domain inner-product architecture. Two DLLs are cascaded to sum up the weighted Δt _in1_ and Δt _in2_, where Δt _in1_ is the initial time difference between _Vin_1_1_ and _Vin_1_2_, and Δt _in2_ is initial time difference between _Vin_2_1_ and _Vin_2_2_. In both configurations of Stage_1 and Stage_2, the transition edge of _Vout_1_1_ is equal to _Vout_1_2_ and the transition edge of _Vout_2_1_ is equal to _Vout_2_2_ because VCDL 1 and VCDL 2 are adjusted by VCTRL 1 and VCTRL 2 in the feedback loop.

In order to propagate the weighted time differences from Stage_1 to Stage_2, the inputs of the delay cells outside the loop in Stage_2 are routed to the outputs of Stage_1, so the start points of the delay line VCDL 2 and CDL 2 are characterized by previous outputs of Stage 1. Therefore, the weighted delays are accumulated from different stages through the cascaded delay lines to acquire the sum shown in different colors in the figure. For example, if the SEL 1 is 3 and SEL 2 is 4, the time...
difference between \( V_{O2,1} \) and \( V_{O2,2} \) is equal to \( (3 \times \Delta t_{i1} + 4 \times \Delta t_{i2}) \).

### 2.3. Pseudo-sigmoid activation function generator

The nonlinear activation functions are used in the hidden and output neurons to estimate the class probability for a given multiplication and accumulation result. A comparator shown in Fig. 6 has been designed as the pseudo-sigmoid activation function generator to transform the summation to probabilities. The summation of the weighted time differences controls charging time of the capacitors at the inputs of the regenerative comparator to perform logistic regression.

The regenerative sense amplifiers are usually used as comparators because the amplification is not required to be linear and achieves smaller delay time with positive feedback. The regenerative comparators can be simplified as the back-to-back inverter-based dynamic latch with its model shown in Fig. 7.

The output voltage can be calculated as

\[
V_{\text{out}}(t) = V_1(t) - V_2(t)
\]

where \( \tau = \sqrt{\frac{C_1 C_2}{G_{m1} G_{m2}}} \) and \( \alpha = \sqrt{\frac{C_1}{C_2} \frac{G_{m2}}{G_{m1}}} \). If the comparator is perfectly matched without any process variations, the output voltage of positive feedback characteristic of the dynamic latch can be expressed as

\[
V_{\text{out}}(t) = (V_{1,0} - V_{2,0}) \cdot e^{-\frac{t}{\tau}}
\]

The comparator output will regenerate more quickly with larger initial input difference as in Fig. 8. Therefore, the inverse of the exponential characteristic is utilized as the logistic sigmoid function

\[
f(x) = \frac{1}{1 + e^{-x}}
\]

### 3. Simulation results

The proposed circuits were simulated in a 65 nm CMOS process in Cadence and modeled as neuron cells for the system level simulation. Fig. 9 shows the simulation results of time-domain multiplication. The upper sub-figure shows that the delay between \( V_{\text{Out1}} \) and \( V_{\text{Out2}} \) is 0.100 \( \mu s \) when the initial input time difference is 0.1 \( \mu s \) and weighting of 1x is applied. The other 2 sub-figures show the weight setting of 4 and 8 and the corresponding time differences between the outputs. To compromise between speed and power consumption, the delay line is designed to carry out 16 times of delay multiplication. Fig. 10 shows the simulation results of 4-bit multiplication and accumulation that result in a summation of 5-bit matrix operation. The output time difference is changed linearly according to the weight values.

Fig. 11 shows the comparison of the normalized transfer curve of the presented activation function versus the standard sigmoid distribution. This pseudo-sigmoid logistic regression can be fitted as follows:

\[
f(x) = \frac{0.9915}{1 + e^{-1.037x}}
\]

The simulated transfer curve of the presented comparator demonstrated the s-shaped pseudo sigmoid function to transform inputs to probabilities. The resolution of the activation function is not limited by the digital levels because of its operation in time domain.

The system level demonstration was carried out in MATLAB for training and classification. Fig. 12 shows the training and testing setup. The time-domain classifier was trained with an off-chip engine. The system was evaluated by classifying the cardiac arrhythmia from the MIT-BIH arrhythmia database [20]. The ECG data that the experiments used is sampled at 360 Hz. Therefore, the classification results can be obtained with 20 k operations per second since the delay can be propagated to the next in the pipeline. The presented classifier achieves 90.5%
accuracy detection. Fig. 13 shows that power consumption scales with power supply voltages. Representing signals in time domain is not only beneficial from technology scaling, but also save significant power with lower power supply voltages. Unlike the conventional classification engines with data converters including ADCs and DACs to interface with the sensors, the time-domain operation can survive lower power supply voltages with lower operation speeds. The power supply can be even lowered to 0.4 V more complicated circuits/power consumption as shown in Ref. [21]. In this work the power supply of 0.9 V can be achieved without sacrificing operation speed to achieve best tradeoff between power consumption and operation speed. Since the calculated results are propagated to the next stage in the pipeline, the proposed architecture achieves 20 k operations per second per unit with power consumption of 240.34 nW. The estimated area for each neuron is less than 40 μm², which means less than 0.01 mm² is added for integration of the classifier into the sensor. Table 1 summarizes the performance and comparison with the other state-of-the-art works for in-sensor computing.

4. Conclusions

To eliminate the needs to continuously transmit complex signals to the aggregator for remote monitoring, a low-power time-domain in-sensor classifier that locally extracts critical features for rapid analysis is presented in this paper. The presented cascaded architecture utilizes DLLs to perform precise multiplication and accumulation. Through a pseudo-sigmoid activation function, the probability for the inner-product result is then estimated. Time-domain operations consume minimal energy under low supply voltages. Hence, the time-domain classifier can be
integrated with edge sensors to enable long-term continuous monitoring of biomedical signals.

Declaration of competing interests

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

CRediT authorship contribution statement

Ethan Chen: Conceptualization, Methodology, Investigation, Software, Data curation, Visualization, Writing - original draft. Vanessa Chen: Conceptualization, Methodology, Supervision, Writing - review & editing, Project administration, Funding acquisition.

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References

[1] W.B. Kannel, J. Cobb, Left ventricular hypertrophy and mortality - results from the Framingham Study, Cardiology vol. 81 (4-5) (1992) 291–298.
[2] Powell, H.C., Jr; Barth, A.T.; Lach, J., “Dynamics of Cardiovascular Disease Prevention”, Proceedings of the 4th International Conference on Body Area Networks, Los Angeles, CA, USA, 1-3 April 2009.
[3] F. Chen, A.P. Chandrakasan, V.M. Stojanovi, Design and analysis of a hardware-efficient compressed sensing architecture for data compression in wireless sensors, IEEE J. Solid State Circuit. 47 (3) (Mar. 2012) 744-756.
[4] K. Liu, M. Zhang, B. Subei, A.G. Richardson, T.H. Lucas, J. Van Der Spiegel, The PennBiH: design of a general purpose wireless brain-machine-brain interface system, IEEE Transactions on Biomedical Circuits and Systems vol. 9 (2) (Apr. 2015) 248–258.
[5] A.J. Cason, E. Rodriguez-Villegas, Considerations on Analogue to Digital Converter Architectures for EEG Acquisition in Augmented Cognition Applications, Human Factors and Ergonomics Society Annual Meeting, Proceedings, 2008, pp. 197–201.
[6] Y.H. Chen, T. Krishna, J. Emer, V. See, “EyeRIS, An Energy-Effective Reconfigurable Accelerator for Deep Convolutional Neural Networks”, IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, San Francisco, CA, Feb. 2016, pp. 262–263.
[7] V. See, Y.H. Chen, T.J. Yang, J. Emer, “Efficient processing of deep neural networks: a tutorial and survey”, Proc. IEEE 105 (12), 2295-2329.

Table 1

| Technology       | ISSCC 15° [11] | VLSI 16° [12] | This work       |
|------------------|----------------|----------------|-----------------|
| 130 nm CMOS      | 130 nm CMOS    | 65 nm CMOS     | 65 nm CMOS      |
| Operations       | 2 0.9-1.2 V    | 1.2 V          | –               |
| per Second       | 100 k          | 20 k           | 0.9 V           |
| Required Clock   | 2 kHz          | 20 kHz         | 2 kHz           |
| Frequency        | 100 MHz        | 20 kHz         | 243.7 µW        |
| Power Consumption| 28 nW          | 663.6 nW       | 240.34 nW       |
| Function         | Compressive Sensing | Matrix-Multiplying | Multiply-Multiplying & Activation Function |

[8] Sungpil Choi, Jinna Lee, Kyutoo Lee, “A 9 HoJ-Jun Yoo, 02mW CNN-stereo-based real-time 3D hand-gesture recognition processor for smart mobile devices”, IEEE Int. Solid-State Circ. Conf. (ISSCC) Digest Tech. Pap. (Feb. 2018) 220-222, San Francisco, CA.
[9] Vipan Kakkar, Comparative study on analog and digital neural networks, Int. J. Comput. Sci. Netw. Security (IJCSNS) VOL.9 (7) (July 2009).
[10] P. Chollet, R. Pallas, C. Lahuec, M. Arzel, F. Seguin, A sub-nJ CMOS ECG classifier for wireless smart sensor. 39th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, EMBC), 2017, pp. 3840–3843.
[11] J. Zhang, Z. Wang, N. Verma, A matrix-multiplying ADC implementing a machine-learning classifier directly with data conversion, IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (2015) 332-333.
[12] Fred N. Buhler, Adam E. Mendrela, Yong Lim, Jeffrey A. Fedenburg, Michael P. Flynn, A 16-channel noise-shaping machine learning analog-digital interface, in: Symposium on VLSI Circuits Digest of Technical Papers, June 2016, pp. C30-C31. Honolulu, HI, USA.
[13] F.N. Buhler, P. Brown, J. Li, T. Chen, Z. Zhang, M.P. Flynn, A 3.4TOPS/W 48.9pJ/ pixel 50.1x/classification 512 analog neuron sparse coding neural network with on-chip learning and classification in 40nm CMOS. Symposium on VLSI Circuits Digest of Technical Papers, Kyoto, Japan, 2017, pp. C30-C31. June.
[14] M.S. Madhav, S.A. Stamper, E.S. Fortune, N.J. Cowan, Closed-loop stabilization of the jamming avoidance response reveals its locally unstable and globally nonlinear dynamics, J. Exp. Biol. 216 (22) (Oct. 2013) 4272–4284.
[15] A. Klinefelter, N.E. Roberts, Y. Shakhshhire, P. Gonzalez, A. Shrivastava, A. Roy, K. Craig, M. Faisal, J. Foley, S. Oh, et al., 21.3 ± 6.45µW self-powered IoT SoC with integrated energy-gathering power management and ULP asymmetric radios. IEEE International Solid-State Circuits Conference, 2015, pp. 384–385.
[16] R.B. Staszewski, K. Muhammad, D. Leipold, C.-M. Hung, Y.-C. Ho, J.L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, L.V. Deng, V. Saric, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O.E. Elzeer, E. de-Ojaldo, P.T. Balsara, All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS, IEEE J. Solid State Circ. 39 (12) (Dec. 2004) 2278-2291.
[17] S. Henzler, S. Koepe, D. Lorenz, W. Kamp, R. Kuenemund, D. Schmitt-Landsiedel, A local passive time interopulation concept for variation-tolerant high-resolution time-to-digital conversion, IEEE J. Solid State Circ. 43 (7) (Jul. 2008) 1666–1676.
[18] H.J.M. Veendrick, The behavior of continuous-time to digital conversion, IEEE J. Solid State Circ. 15 (2) (Apr. 1980) 169-176.
[19] W.-H. Lee, J.-D. Cho, S.-D. Lee, A high speed and low power phase-frequency detector and charge-pump, in: Proceedings of the ASP-DAC '99 Asia and South Pacific Design Automation Conference, 1999, pp. 269-272.
[20] MIT-BIH arrhythmia database [Online]. Available: http://physionet.org/physiob ak/database/mitdb/.
[21] A. Amaravati, S.B. Naasir, J. Ting, I. Yoon, A. Raychowdhury, “A 55-nm, 1.0-0.4V, 1.25-pJ/MAC time-domain mixed-signal neuromorphic accelerator with stochastic synapses for reinforcement learning in autonomous mobile robots, IEEE J. Solid State Circ. 54 (1) (Jan. 2019) 75-87.
[22] D. Gangopadhyay, E.G. Allstot, A.M.R. Dixon, K. Natarajan, S. Gupta, D.J. Allstot, Compressed sensing analog front-end for bio-sensor applications, IEEE J. Solid State Circ. 49 (2) (Feb. 2014) 426-438.