Efficient Realization of Givens Rotation through Algorithm-Architecture Co-design for Acceleration of QR Factorization

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Abstract—We present efficient realization of Generalized Givens Rotation (GGR) based QR factorization that achieves 3-100x better performance in terms of GFlops/watt over state-of-the-art realizations on multicore, and General Purpose Graphics Processing Units (GPGPUs). GGR is an improvement over classical Givens Rotation (GR) operation that can annihilate multiple elements of rows and columns of an input matrix simultaneously. GGR takes 33% lesser multiplications compared to GR. For custom implementation of GGR, we identify macro operations in GGR and realize them on a Reconfigurable Data-path (RDP) tightly coupled to pipeline of a Processing Element (PE). In PE, GGR attains speed-up of 1.1x over Modified Householder Transform (MHT) presented in the literature. For parallel realization of GGR, we use REDEFINE, a scalable massively parallel Coarse-grained Reconfigurable Architecture, and show that the speed-up attained is commensurate with the hardware resources in REDEFINE. GGR also outperforms General Matrix Multiplication (gemm) by 10% in-terms of GFlops/watt which is counter-intuitive.

Index Terms—Parallel computing, orthogonal transforms, dense linear algebra, multiprocessor system-on-chip, instruction level parallelism

1 INTRODUCTION

QR factorization/decomposition (QRF/QRD) is a prevalent operation encountered in several engineering and scientific operations ranging from Kalman Filter (KF) to computational finance [1][2]. QR factorization of a non-singular matrix $A_{m \times n}$ of size $m \times n$ is given by

$$A = QR$$

where $Q_{m \times m}$ is an orthogonal and $R_{m \times n}$ is upper triangular matrix. There are mainly three methods to compute QR factorization, 1) Householder Transform (HT), 2) Givens Rotation (GR), and 3) Modified Gram-Schmidt (MGS). MGS is used in the embedded systems where numerical accuracy of the final solution is not critical, while HT is employed in High Performance Computing (HPC) applications since it is numerically stable operation. GR is applied in the application domains pertaining to embedded systems where numerical stability of the end solution is critical [3]. We sense here an opportunity in GR for applicability in domains beyond embedded systems. Specifically, we foresee opportunity in GR in generalization for annihilation of multiple elements of an input matrix simultaneously where annihilation regime spans over columns and rows. It is intended to expose higher parallelism in classical GR through generalization and also reduction in total number computations in GR. Such a generalization is possible by combining several Givens sequences and performing common computations required for updating trailing matrix beforehand. Surprisingly, such an approach is nowhere presented in the literature and that has reduced relevance of GR in several application domains. It has been emphasized in the literature that GR is more suitable for orthogonal decomposition of sparse matrices while for orthogonal decomposition of dense matrices, HT is more suitable over GR [4][5]. For implementations on multicore and General Purpose Graphics Processing Units (GPGPUs), a library based approach is followed for Dense Linear Algebra (DLA) computations where highly tuned packages based on specifications given in Basic Linear Algebra Subprograms (BLAS) and Linear Algebra Package (LAPACK) are developed [6]. Several realizations of QR factorization are discussed in section 2.3. Typically, block QR factorization routine (xgeqrf - where x indicates double/single precision) that is part of LAPACK is realized as a series of BLAS calls. dgeqrf2 and dgeqrf operations are shown in figure 1. In dgeqrf2, Double Precision Matrix-vector (dgemv) operation is dominant while in dgeqrf, Double Precision
Matrix Multiplication (dgemm) is dominant as depicted in the figure. dgemv can attain up to 10% of the theoretical peak in multicore platforms and 15-20% in GPGPUs while dgemm can attain up to 40-45% in multicore platforms and 55-60% in GPGPUs at ≈ 65W and ≈ 260W respectively [7]. Considering low performance of multicore and GPGPUs for critical DLA computations, it could be a prudent approach to move away from traditional BLAS/LAPACK based strategy in software and accelerate these computations on a customizable platform that can attain order of magnitude higher performance than state-of-the-art realizations of these software packages. A special care has to be taken in designing of an accelerator that is capable of attaining desired performance while maintaining generality of the accelerator in also supporting other operations in the domain of DLA computations. Coarse-grained Reconfigurable Architectures (CGRAs) are a good candidate for the domain of DLA computations since they are capable of attaining performance of Application Specific Integrated Circuits (ASICs) while flexibility of Field Programmable Gate Arrays (FPGAs) [3][9][10].

Recently, there have been several proposals in the literature in developing BLAS and LAPACK on customizable CGRA platforms through algorithm-architecture co-design where macro operations in the operations pertaining to DLA computations are identified and realized on a Reconfigurable Data-path (RDP) that is tightly coupled to the processor pipeline [11][12]. In this paper, we focus on acceleration of QR based factorization, where classical GR is generalized to achieve Generalized Givens Rotation (GGR) where GGR has 33% lesser multiplications compared to GR. Several macro operations in GGR are identified and realized on RDP to achieve superior performance compared to Modified Householder Transform (MHT) presented in [7]. Major contributions in this paper to achieve efficient realization of GR based QR factorization are as follows:

- We improvise over Column-wise Givens Rotation (CGR) presented in [13] and present GGR. While CGR is capable of simultaneous annihilation of multiple elements of a column in the input matrix, GGR can annihilate multiple elements of rows and columns simultaneously.
- Several macro operations in GGR are identified and implemented on an RDP that is tightly coupled to pipeline of a Processing Element (PE) resulting in 81% of the theoretical peak in PE. This implementation outperforms Modified Householder Transform (MHT) based QR factorization (dgeqr2ht) implementation presented in [7] by 10% in PE. GGR based QR factorization also outperforms dgemm in PE by 10% which is counter-intuitive.
- Arguably, moving away from BLAS for realization of GGR based QR factorization attains 10% higher performance than the classical way of implementation where Level-3 BLAS is used as a dominant operation in the state-of-the-art software packages for multicore and GPGPUs. This claim is validated by several case studies on multicore and GPGPUs where it is also shown that moving away from BLAS and LAPACK in these platforms does not yield performance improvement.
- For parallel realization in REDEFINE, we attach PE in REDEFINE framework where 10% higher performance is attained over dgeqr2ht implementation presented in [7]. We show that sequential realization in PE and parallel realization of GGR based QR factorization in REDEFINE are scalable. Furthermore, it is shown that the speed-up in parallel realization in REDEFINE over sequential realization in PE is commensurate with the hardware resources employed in REDEFINE and the speed-up asymptotically approaches theoretical peak of REDEFINE CGRA.

For our implementations in PE and REDEFINE, we have used double precision Floating Point Unit (FPU) presented in [14] with recommendations presented in [15]. Organization of the papers is as follows: In section 2, we discuss about GR, REDEFINE and some of the FPGA, multicore, and GPGPU based realizations of QR factorization. Case studies on dgemm, dgeqr2, dgeqr2ht, and dgeqr2ht are presented in section 3. GGR and implementation of GGR in multicore, GPGPU, and PE is discussed in 4. Parallel realization of GGR in REDEFINE CGRA is discussed in 5. We conclude our work in section 6.

### Abbreviations/Nomenclature:

| Abbreviation/Name | Expansion/Measuring |
|-------------------|---------------------|
| AVX               | Advanced Vector Extension |
| BLAS              | Basic Linear Algebra Subprograms |
| CE                | Compute Element |
| CFU               | Custom Function Unit |
| CGRA              | Coarse-grained Reconfigurable Architecture |
| CPI               | Cycles-per Instruction |
| CUDA              | Compute Unified Device Architecture |
| EREW-GRAM          | Exclusive-read/Exclusive-write Parallel Random Access Machine |
| DAG               | Directed Acyclic Graph |
| FPGA              | Field Programmable Gate Array |
| FPS               | Floating Point Sequencer |
| FPU               | Floating Point Unit |
| GPGPU             | General Purpose Graphics Processing Unit |
| GR                | Givens Rotation |
| GGR               | Generalized Givens Rotation |
| HHT               | Householder Transform |
| ICC               | Intel C Compiler |
| IFORT             | Intel Fortran Compiler |
| ILP               | Instruction Level Parallelism |
| KF                | Kalman Filter |
| LAPACK            | Linear Algebra Package |
| MAGMA             | Matrix Algebra on GPU and Multicores Architectures |
| MGS               | Modified Gram-Schmidt |
| MHT               | Modified Householder Transform |
| NoC               | Network-on-Chip |
| PE                | Processing Element |
| PLASMA            | Parallel Linear Algebra Software for Multicores Architectures |
| QUARK             | Queueing and Runtime for Kernels |
| RDP               | Reconfigurable Data-path |
| XGEMV/xgemv       | Single/Double Precision General Matrix-vector Multiplication |
| XGEMM/xgenn       | Single/Double Precision General Matrix Multiplication |
| XGEGQR2/dgeqr2    | Single/Double Precision QR Factorization based on Householder Transform (with XGEMV) |
| XGEGQRF/xgeqr     | Blocked Single/Double Precision QR Factorization based on Householder Transform (with XGEMM) |
| XGEGQR2HT/xgeqr2ht| Blocked Single/Double Precision QR Factorization based on Modified Householder Transform |
| XGEGQR2GGR/xgeqr2gg | Single/Double Precision QR Factorization based on Generalized Givens Rotation |
| XGEGR2FHT/xgeqfft | Blocked Single/Double Precision QR Factorization based on Modified Householder Transform (with XGEMM) |
| XGEGR2FFGR/xgeqfft | Blocked Single/Double Precision QR Factorization based on Generalized Givens Rotation (with XGEMM) |
| PACKAGE ROUTINE packageroutine | Naming convention followed for different routines pertaining to different packages. E.g., BLAS_DGEMM/blas_dgemm is a Double Precision General Matrix Multiplication Routine in BLAS |

### 2 BACKGROUND AND RELATED WORK
CGR presented in [13] is discussed in section 2.1 and REDEFINE CGRA is discussed in section 2.2. A detailed review of yeestyear realizations of QR factorization is presented in section 2.3.
2.1 Givens Rotation based QR Factorization

For a $4 \times 4$ matrix $X = x_{ij}$, applying 3 Givens sequences simultaneously yields to the matrix $GX$ shown in equation (2):

$$GX = \begin{bmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1 \\
\end{bmatrix}
$$

Corresponding Directed Acyclic Graphs (DAGs) for GGR for annihilation of $x_{41}, x_{31},$ and $x_{21}$ and update of the second column of the matrix $X$ are shown in figure 1. For an input matrix of size $n \times n$ classical GR takes $n(n-1)/2$ sequences while CGR takes $n-1$ sequences. Furthermore, if the number of multiplications in GR is $GR_M$ and number of multiplications in CGR is $CGR_M$ then

$$CGR_M = \frac{2n^3 + 3n^2 - 5n}{2}$$

$$GR_M = \frac{4n^3 - 4n}{3}$$

Taking ratio of equation (3) and (4)

$$\alpha = \frac{CGR_M}{GR_M} = \frac{3(2n + 5)}{8(n + 1)}$$

From equation 5 as $n \to \infty$, $\alpha \to \frac{3}{4}$. As we increase the size of the matrix, the number of multiplications in CGR asymptotically approaches $\frac{3}{4}$ times the number of multiplications in GR. Implementation details of CGR on systolic array and in REDEFINE can be found in [13].

2.2 REDEFINE CGRA

REDEFINE CGRA is a customizable massively parallel Multiprocessor System on Chip (MPSoC) where several Tiles are connected through Network-on-Chip (NoC) [16]. Each Tile consists of a Compute Element (CE) and a Router. CEs in REDEFINE can be enhanced to support several applications domains like signal processing and Dense Linear Algebra (DLA) computations by attaching domain specific Custom Function Units (CFUs) to the CEs [17]. REDEFINE framework is shown in figure 3. A Reconfigurable Data-path is tightly coupled to a Processing Element (PE) that is CPU for REDEFINE as shown in the figure 3. Performance of PE in dgemm and MHT based QR factorization (dgeqr2ht) is shown in figure 4(a) [7]. Performance of PE over several Architectural Enhancements (AEs) is shown in figure 4(b). It can be observed in the figure 4(a) that PE attains 3-100x better performance in dgemm and dgeqr2ht while PE with tightly coupled RDP is capable of attaining 74% of the theoretical peak performance of PE in dgemm as shown in figure 4(b). Performance in dgemm an dgeqr2ht is attained through algorithm-architecture co-design where macro operations in dgemm and dgeqr2ht are identified and realized on RDP. We apply similar technique in this exposition for GR where we first present GGR and identify macro operations in GGR that are realized on RDP. GGR implementation (dgeqr2ggr) outperforms dgeqr2ht and dgemm. Further details of dgemm and dgeqr2ht realizations can be found in [17], [18], [19], and [7].

2.3 Related Work

Due to wide range of applications in the embedded systems domain, GR has been studied extensively in the literature specifically for implementation purpose since it was first proposed in [20]. An alternate ordering of Givens sequences was presented in [21]. According to the scheme presented in [21], the alternate ordering is amenable to parallel implementation of GR while it does not focus on fusing several Givens sequences to annihilate multiple elements. For an input matrix of $n \times n$, the alternate ordering presented in [21] can annihilate maximum $\frac{n}{2}$ elements in parallel by executing disjoint Givens sequences simultaneously. Pipeline Givens sequences for computing QR decomposition is presented in [22] where its is proposed to execute Givens sequences in pipeline fashion to update the pair of rows partially updated by the previous Givens sequences. Analysis of this strategy is presented for Exclusive-read Exclusive-write Parallel Random Access Machine (EREW-PRAM) that shows that the pipeline strategy is twice as fast compared to the classical GR. Greedy Givens algorithm is presented in [23] that executes compound disjoiing Givens sequences in parallel assuming unlimited parallelism case. A high speed tournament GR and VLSI implementation of tournament GR is presented in [3] where a significant improvement is reported in ASIC over triangular systolic array. The scheduling scheme presented in [3] is similar to the one presented in [21] where disjoint Givens sequences are applied to compute QR decomposition. FPGA implementation of GR is presented in [24] while ASIC implementation of square-root free GR is presented in [25]. A novel technique to avoid underflow/overflow in computation of QR decomposition using classical GR is presented in [26] that results in numerical stable realization of GR in LAPACK. A two-dimensional systolic array implementation of GR is presented in [27] where classical GR is implemented on two-dimensional systolic array with diagonal elements of the array performs complex operations like square root and division while the rest of the array performs matrix update. Restructuring of tridiagonal and bidiagonal algorithms for QR decomposition is presented in [28]. The restructruing strategy presented in [28] has several advantages like it is capable of exploiting vector instructions in the modern architectures, reduces memory operations, and the matrix updates are in the form of Level-3 BLAS thus capable of exploiting cache architecture through reuse of data compared to classical GR where it is Level-2 BLAS. Although, the scheme presented in [28] re-arranges memory bound operations like Level-2 BLAS in classical GR to compute bound operations like Level-3 BLAS, the scheme does not reduce computations unlike GGR. In general, works related to GR in the literature focus on different scheduling schemes for parallelism and exploitation of architectural features for the targeted platform. In case of GGR, total work is reduced compared to the classical GR while also being architecture platform friendly. For implementation of GR, there has been no work in the literature where macro operations in the routine are identified and realized carefully for performance.

3 Case Studies

For our experiments on multicore and GPGPUs we use highly tuned software packages PLASMA and MAGMA. Software
3.1 dgemm

dgemm is a Level-3 BLAS routine that has three loops and time complexity of $O(n^3)$ for a matrix of size $n \times n$. Performance of dgemm in LAPACK in-terms of theoretical peak of underlying platform is shown in figure 6(a) and in-terms of Gflops/watt in MAGMA is shown in figure 6(b). It can be observed in the figure 6(a) that the performance attained by dgemm in Intel Core i7 and Nvidia Tesla C2050 is hardly 25% and 57% respectively. In-terms of Gflops/watt it is 1.22 in Nvidia Tesla C2050. Due to trivial nature of dgemm algorithm, we do not reproduce dgemm algorithm here while standard dgemm algorithm can be found in [2].

3.2 dgeqr2

Pseudo code of dgeqr2 is described in algorithm [1]. It can be observed in the pseudo code in the algorithm [1] that, it contains three steps, 1) computation of a householder vector for each column 2) computation of householder matrix $P$, and 3) update of trailing matrix using $P = I - 2vv^T$ where $I$ is an identity matrix.
matrix. For our experiments, we use Intel C Compiler (ICC) and Intel Fortran Compiler (IFORT). We also use different compiler switches to improve the performance of dgeqr2 in LAPACK on Intel micro-architectures. In Intel Core i7 4th Gen machine which is a Haswell micro-architecture, CPI attained saturates at 1.1 [7].

In case when compiler switch —mavx is used that enables use of Advanced Vector Extensions (AVX) instructions, the Cycles-Per-Instruction (CPI) attained is increased. This behavior is due to AVX instructions that use Fused Multiply Add (FMA). Due to this fact, the CPI reported by VTune™can not be considered as a measure of performance for the algorithms and hence we accordingly double the instruction count reported by Intel VTune™.

In case of GPGPUs, dgeqr2 in MAGMA is able to achieve up to 16 Gflops in Tesla C2050 which is 3.1% of the theoretical peak performance of Tesla C2050 while performance in terms of Gflops/watt is as low as 0.04 Gflops/watt.

3.3 dgeqrf

Algorithm 2 dgeqrf (Pseudo Code)

1: Allocate memories for input/output matrices
2: for $i = 1$ to $n$ do
3:    Compute Householder vectors for block column $m \times k$
4:    Compute $P$ matrix where $P$ is Computed using Householder vectors
5:    Update trailing matrix using dgemm
6: end for

Pseudo code for dgeqrf routine is shown in algorithm [3]. In terms of computations, there is no difference between algorithms [1] and [2]. In a single core implementation, dgeqrf is observed to be 2-3x faster than dgeqr2. The major source of efficiency in dgeqrf is efficient exploitation of processor memory hierarchy and dgemm routine which is a compute bound operation [30, 31]. In Nvidia Tesla C2050, dgeqrf in MAGMA is able to achieve up to 265 Gflops which is 51.4% of theoretical peak performance of Tesla C2050 as shown in the figure 6(a) which is 90.5% of the performance attained by dgemm. In dgeqr2 in MAGMA, performance attained in terms of Gflops/watt is as low as 0.05 Gflops/watt while for dgemm and dgeqrf it is 1.23 Gflops/watt and 1.09 Gflops/watt respectively in Nvidia Tesla C2050 as shown in figure 6(b). In case of dgeqr2 in PLASMA, the performance attained is 0.39 Gflops/watt while running dgeqr2 in four cores.

3.4 dgeqr2ht

Pseudo code for dgeqr2ht is shown in algorithm [3]. A clear difference between dgeqr2 in the algorithm [1] dgeqrf in the algorithm [2] and dgeqr2ht in the algorithm [3] is in updating of trailing matrix. dgeqr2 uses dgemv operation which is a memory bound operation, and dgeqrf uses dgemm operation which is compute bound operation while dgeqr2ht uses an operation that is more dense in-terms of computations resulting in lower $\theta$ where $\theta$ is a rough quantification of parallelism through DAG based analysis of routines dgeqr2, dgeqrf, and dgeqr2ht. In case of no-change in the computations in the improved routine after re-arrangement of computations (in this case fusing of the loops), $\theta$ translates into ratio of number of levels in the DAG of improved routine to number of levels in the DAG of classical routine. Implementation of dgeqr2ht clearly outperforms implementation of dgeqrf in PE as shown in figure 7(a). In the figure 7(a) the performance is shown in-terms of percentage of theoretical peak performance of PE and also in-terms of percentage of theoretical peak performance normalized to the performance attained by dgemm in the PE. It can be observed in the figure 7(a) that the performance attained by dgeqr2ht is 99.3% of the performance attained by dgemm in the PE. Furthermore, it can be observed in figure 7(b) that the performance achieved in-terms of Gflops/watt in the PE is 35 Gflops/watt compared to performance attained by dgeqrf which is 25 Gflops/watt. In multicore and GPGPUs, such a fusing does not translate into improvement due to limitations of the platform. Further details of dgeqr2ht implementation can be found in [7]. Based on case studies on dgemm, dgeqr2, dgeqrf, and dgeqr2ht, we make following observations:

- dgeqrf in highly tuned software packages like PLASMA and MAGMA attains 16% and 51% respectively. This leaves a further scope for improvement in these routines through careful analysis
- Typically, dgeqrf routine that has compute bound operation like dgemm achieves 80-85% of the theoretical peak performance attained by dgemm in multicore and GPGPUs
- dgeqr2ht attains similar performance as dgeqrf in multicore and GPGPUs while it clearly outperforms dgeqrf in PE

We further propose generalization in CGR presented in [13] and derive GGR that can outperform dgeqr2ht in PE and in REDEFINE.

4 GENERALIZED GIVENS ROTATION AND IMPLEMENTATION

From equation [1] matrix $A_{n \times n}$, annihilation of element in the last row and first column which is $(n,1)$ would require application of one Givens sequence

$$G_{n,1}A = \begin{bmatrix} R^{(1)}_1 \\ 0 \end{bmatrix}$$

where matrix $R^{(k)}$ is a matrix with $k$ zero elements in the lower triangle of the matrix and has undergone k-updates. In general Givens matrix is given by equation [7]

$$G_{i,j} = \text{diag}(I_{i-2}, \tilde{G}_{i,j}, I_{m-i})$$

$$\tilde{G} = \begin{bmatrix} c & s \\ -s & c \end{bmatrix}$$

$$G_{i,j} = \text{diag}(I_{i-2}, \tilde{G}_{i,j}, I_{m-i})$$

$$\tilde{G} = \begin{bmatrix} c & s \\ -s & c \end{bmatrix}$$

$$G_{i,j} = \text{diag}(I_{i-2}, \tilde{G}_{i,j}, I_{m-i})$$

$$\tilde{G} = \begin{bmatrix} c & s \\ -s & c \end{bmatrix}$$

Algorithm 3 dgeqr2ht (Pseudo Code)

1: Allocate memories for input/output matrices
2: for $i = 1$ to $n$ do
3:    Compute Householder vectors for block column $m \times k$
4:    Compute $PA$ where $PA = A - 2vv^T A$
5: end for

$$G_{i,j} = \text{diag}(I_{i-2}, \tilde{G}_{i,j}, I_{m-i})$$

$$\tilde{G} = \begin{bmatrix} c & s \\ -s & c \end{bmatrix}$$

$$G_{i,j} = \text{diag}(I_{i-2}, \tilde{G}_{i,j}, I_{m-i})$$

$$\tilde{G} = \begin{bmatrix} c & s \\ -s & c \end{bmatrix}$$

$$G_{i,j} = \text{diag}(I_{i-2}, \tilde{G}_{i,j}, I_{m-i})$$

$$\tilde{G} = \begin{bmatrix} c & s \\ -s & c \end{bmatrix}$$
where \( c = \frac{A_{i,j}}{A_{1,j}} \), \( s = \frac{A_{1,j}}{A_{i,j}} \) and \( t = \frac{A_{2,j}^{2} - A_{1,j}^{2}}{A_{2,j}} \). It takes \( n - 1 \) Givens sequences to annihilate \( n - 1 \) elements in the matrix \( A \). There is a possibility to apply multiple Givens sequences to annihilate multiple elements in a column of a matrix. Thus, extending equation \( \text{(6)} \) to annihilate 2-elements in the first column of the matrix \( A \)

\[
G_{n-1,1}A = \begin{bmatrix} R^{(2)}_{1} \\ 0 \end{bmatrix}
\]

where \( (G_{n-1,1}A)^{T}(G_{n-1,1}A) = (G_{n-1,1}A)(G_{n-1,1}A)^{T} = I \). Extending further equation \( \text{(6)} \) to annihilate \( n - 1 \) elements of the first column of the input matrix \( A \)

\[
G_{2,1}G_{3,1}...G_{n-1,1}A = \begin{bmatrix} R^{(n-1)}_{1} \\ 0 \end{bmatrix}
\]

where \( (G_{2,1}G_{3,1}...G_{n-1,1}A)^{T}(G_{2,1}G_{3,1}...G_{n-1,1}A) = (G_{2,1}G_{3,1}...G_{n-1,1}A)(G_{2,1}G_{3,1}...G_{n-1,1}A)^{T} = I \). Formulation in equation \( \text{(8)} \) can annihilate \( n - 1 \) elements in the first column of the input matrix \( A \). Further annihilating \( n - 1 \) elements to \( (n-1) + (n-2) \) elements that results in matrix \( R^{(n-1)+(n-2)} \) where \( n - 1 \) elements in the first column and \( n - 2 \) elements in the second column of matrix \( R \) are zero as given by equation \( \text{(9)} \)

\[
(G_{3,2}G_{4,2}...G_{n-1,2}A)G_{2,1}G_{3,1}...G_{n-1,1}A = \begin{bmatrix} R^{(n-1)+(n-2)}_{1} \\ 0 \end{bmatrix}
\]

where \( ((G_{3,2}G_{4,2}...G_{n-1,2}A)(G_{2,1}G_{3,1}...G_{n-1,1}A))^{T} = (((G_{3,2}G_{4,2}...G_{n-1,2}A)(G_{2,1}G_{3,1}...G_{n-1,1}A))^{T} = (((G_{3,2}G_{4,2}...G_{n-1,2}A)(G_{2,1}G_{3,1}...G_{n-1,1}A))^{T} = I \). To annihilate \( \frac{n(n-1)}{2} \) elements in the lower triangle of the input matrix \( A \), it takes \( n - 1 \) sequences and the Givens matrix shrinks by one row and one column with each column annihilation. Further generalizing equation \( \text{(10)} \)

\[
(G_{n,n-1})G_{n-1,1}G_{n-2,1}...G_{3,2}G_{n-1,2}G_{n-1,2}A = \begin{bmatrix} R^{(n-1)+(n-2)}_{1} \\ 0 \end{bmatrix}
\]

A pictorial view for \( 8 \times 8 \) matrix that compares CGR with GGR is shown in figure \( \text{(5)} \) and GGR pseudo code is given in algorithm \( \text{(4)} \) it can be observed in the figure \( \text{(8)} \) that CGR operates column-wise and takes total 7 iterations to upper triangularize the matrix of size \( 8 \times 8 \) while GGR operates column-wise as well as row-wise and can upper triangularize matrix in a single iteration. It can be observed in the algorithm \( \text{(4)} \) that the update of the first row and the rest of the rows can be executed in parallel. Furthermore, there also exist parallelism across the out loop iterations in GGR. Theoretically, classical GR takes \( \frac{n(n-1)}{2} \) iterations to upper triangularize an input matrix of size \( n \times n \), and CGR takes \( n - 1 \) iterations to upper triangularize an input matrix of size \( n \times n \) while GGR can upper triangularize a matrix of size \( n \times n \) in 1 iteration.
However, in practical scenario, it is not possible to accommodate large matrices in the registers or Level 1 (L1) cache memory. Hence, a sophisticated matrix partitioning schemes are required to efficiently exploit the memory hierarchy in multicore and GPGPUs.

4.1 GGR in Multicore and GPGPU

For multicores realization of GGR, we use PLASMA framework and for GPGPU realization, we use MAGMA framework depicted in figure 5.

4.1.1 GGR in PLASMA

To implement GGR in multicore architectures, we first implement dgeqr2ggr routine in LAPACK and we use that routine in PLASMA. GGR implementation in LAPACK is shown in algorithm 5 as a pseudo code. It can be observed in the algorithm 5 that the most computationally intensive part in GGR is update function. In our implementation, update function becomes part of BLAS while in LAPACK, we implement dgeqr2ggr function that is wrapper function of update function that calls update function $n$ times for input matrix of size $n \times n$ as shown in algorithm 5

Algorithm 5 lapack_dgeqr2ggr (GGR in LAPACK) (Pseudo code)

Allocate memory for input/output matrices and vectors
for $i = 1$ to $n$ do
    update(L, A(i,i), A, LDA, I, N, M, Tau(i), Beta)
end for

Update()  
Initialize $k$, $l$, and $s$ vectors to 0  
Calculate $2$-norm of the column vector  
Calculate $k$, $l$, and $s$ vectors  
Update row $i$ of the matrix  
Update row $i + 1$ to $n$ using $k$, $l$, and $s$ vectors

Performance comparison of dgeqr2ggr, dgeqrfggr, dgeqr2, dgeqr, dgeqr2ht, and dgeqrht in LAPACK and PLASMA is shown in figure 9. It can be observed in the figure 9 that despite more computations in dgeqr2ggr, the performance of dgeqr2ggr is comparable to dgeqr2, and performance of dgeqrfggr is comparable to dgeqr in LAPACK and PLASMA. We compare run-time of the different routines normalized to dgemm performance in respective software packages since total number of computations in HT, MHT, and GGR are different. Furthermore, in our implementation of GGR in PLASMA, we use dgemm for updating trailing matrix.

4.1.2 GGR in MAGMA

For implementation of magma_dgeqr2ggr, we insert routines in MAGMA_BLAS. Pseudo code for the inserted routine is shown in algorithm 6. The implementation consists of 3 functions, dnrn2 that computes $2$-norm of the column vector, computation of $k$, and $l$ vectors by function klvec and update of trailing matrix by dtmup function. It can be observed in the algorithm 6 that the most computationally intensive part in the routine is dtmup function. There are two routines implemented, 1) dgeqr2ggr where trailing matrix is updated using method shown in equation 2, 2) dgeqrfggr where trailing matrix is updated using dgemm. Performance of dgeqr2ggr and dgeqrfggr is shown in figure 9. It can be observed in the figure 9 that the performance of dgeqr2ggr is similar to performance of dgeqr2 in MAGMA while performance of dgeqrfggr is similar to the performance of dgeqr in magma. Despite abundant parallelism available in dgeqr2ggr, GPGPUs are not capable of exploiting this parallelism due to serialization of the routine while in dgeqrfggr, GPGPUs perform similar to dgeqr due to dominance of dgemm in the routine.

Algorithm 6 magma_dgeqr2ggr (GGR in MAGMA) (Pseudo code)

\[
\begin{align*}
\text{dnrn2} &<\langle grid, threads, 0, queue \rangle \rightarrow \text{cuda \_stream()} \\
\text{klvec} &<\langle grid, threads, 0, queue \rangle \rightarrow \text{cuda \_stream()} \\
\text{dtmup} &<\langle n, threads, 0, queue \rangle \rightarrow \text{cuda \_stream()} \\
\text{dnrn2} &()
\end{align*}
\]

for $k = 1$ to $m$ do
    for $j = 0$ to BLOCK_SIZE do
        $w = A[llda*(row) + (m-1-j-k)] \ast V\_shared[j]$
        if $row == 0$ then
            $dot[llda \ast (row) + (m - 1 - k - j)] = -
copysign(sqrt(w), \text{vector})$
            else if $row == 0$ then
                $dot[llda \ast (row) + (m - 1 - k - j)] = w$
            end if
        end for
    end for
end for
klvec()
if $row == 0$ then
    $dl[row] = 0$
    $dk[row] = 1/dot[0]$
else if $row == m - 1$ then
    $dl[row] = dv[row] / \text{dot[row - 1]}
    $dk[row] = dv[row - 1] / \text{dot[row - 1]}
else if $(row > 0) \& \& (row < (m - 1))$ then
    $dl[row] = \text{dot[row] / dot[row - 1]}
    $dk[row] = \text{dv[row - 1] / (dot[row] * \text{dot[row - 1]})}$
end if
dtmup()
\[
\begin{align*}
\text{tc}[\text{m - 1}] & = (dC[m - 1] \ast dC[m - 1]) - (\text{dl}[m - 1] \ast dC[m - 2]) \\
\text{for } j = m - 2 - \text{tx} \text{ to } 1 \text{ do} \\
\text{dC}[j] & = (dk[j] \ast \text{dot[j]}) - (\text{dl}[j] \ast dC[j - 1]) \\
\text{end for} \\
\text{dC}[0] & = dk[0] \ast \text{dot[0]}
\end{align*}
\]

of dgeqrfggr is similar to the performance of dgeqr in magma. Despite abundant parallelism available in dgeqr2ggr, GPGPUs are not capable of exploiting this parallelism due to serialization of the routine while in dgeqrfggr, GPGPUs perform similar to dgeqr due to dominance of dgemm in the routine.

4.2 GGR in PE

For implementation of dgeqr2ggr, and dgeqrfggr in PE, we use similar method as presented in [7]. We perform DAG based analysis of GGR and identify macro operations in the DAGs. These macro operations are then realized on RDP that is tightly coupled to PE as shown in figure 10. PE consists of two modules, 1) Floating Point Sequencer (FPS), and 2) Load-Store CFU.

FPS performs double precision floating point computations while Load-Store CFU is responsible for loading and storing of data in registers, and Local Memory (LM) to/from the Global Memory (GM). Operation in the PE can be defined by following steps:
Send a load request to GM for input matrix and store input matrix elements in LM
• Move input matrix elements to registers in the FPS
• Write results back to GM if the computed elements are the final output or if they are not to be used immediately

Up to 90% of overlap in computation and communication is attained in the PE for dgemm as presented in [17]. To identify macro operations, considering example of $4 \times 4$ matrix shown in the figure [2] and equation [2]. It can be observed in the figure [2] that computing Givens Generation (GG) is an square root of inner product while computing update of the first row is similar to inner product. Furthermore, computing rows 2, 3, and 4 is determinant of $2 \times 2$ matrix. We map these row updates on RDP as shown in figure [12] It can be observed in the figure [12] that the RDP can be re-morphed to perform scalar multiplication (MUL/DOT1), inner product of 2-element vectors (DOT2), inner product of 3-element vectors, determinant of $2 \times 2$ matrix (DET2), and inner product of 4-element vectors (DOT4) operations. In our implementation we ensure that the reconfiguration of RDP is minimal to improve energy efficiency of the PE. We introduce custom instructions like DOT4, DOT3, DOT2, DOT1, and DET2 instructions in PE to implement these macro operations in RDP along with instruction that can reconfigure RDP. Different routines are realized using these instructions as shown in figure [11] In the figure [11] it can be observed that irrespective of routine for QR factorization implemented in PE, the communication pattern remains consistent across the routines. In our implementation of dgeqr2ggr, we ensure that RDP is configured to perform two DET2 instructions in parallel that maximizes resource utilization of RDP. In our implementation of dgeqr2ggr, instructions in the two function UPDATE_ROW1 and UPDATE are merged such that the pipeline stalls in the RDP are minimized. Such an approach is not possible in implementation of dgeqrfggr or dgeqrft that since trailing matrix is updated using dgemm routine and until the matrix required to update the trailing matrix update is not computed, trailing matrix update can not be processed.

Speed-up in dgeqr2ggr over different routines is shown in figure [13(a)] It can be observed in the figure [13(a)] that the speed-up attained in dgeqr2ggr over other routines range between 1.1 to 2.25x. Performance in-terms of the percentage of peak performance normalized to the performance attained by dgemm for different routines for QR factorization is shown in figure [13(b)] A counter-intuitive observation that can be made here is that dgeqr2ggr can achieve performance that is higher than the performance attained by dgemm in the PE while dgeqr2ht performance reported in [2] is same as performance attained by dgemm. dgeqr2ggr can achieve performance that is up to 82% of the theoretical peak of PE. dgeqr2ggr attains 10% higher Gflops/watt over dgeqr2ht which is the best performing routine as reported in [2] and [19]. Furthermore, improvement in dgeqr2ggr over other platforms is shown in figure [13(d)]. It can be observed in the figure [13(d)] that the performance improvement in PE for dgeqr2ggr over dgeqr2ggr in off-the-shelf platforms is ranging from 3-100x.

5 PARALLEL IMPLEMENTATION OF GGR IN REDEFINE

An experimental setup for implementation of dgeqrfggr and dgeqr2ggr is shown in figure [14] where PE that outperforms other off-the-shelf platforms for DLA computations is attached as a CPU to the Routers in REDEFINE CE.

For implementation of dgeqrfggr and dgeqr2ggr in REDEFINE, it requires an efficient partitioning and mapping scheme that can sustain computation to communication ratio that is commensurate with the hardware resources of the platform, and also ensures scalability. We follow similar strategy presented in [2] for realization of dgeqrfggr and dgeqr2ggr in DEFINE and propose a general scheme that is applicable for the input matrix of any size. For our experiments, we consider 3 different configurations in REDEFINE consisting of $2 \times 2$, $3 \times 3$, and $4 \times 4$ Tile arrays. Assuming that input matrix is of the size $N \times N$ and REDEFINE Tile array is of size $K \times K$, the input matrix can be partitioned into the blocks of $N/K \times N/K$ sub-matrices. Since, objective of our experiment is to show scalability of our solution, we choose $N$ and $K$ such that $N \% K = 0$. Matrix partitioning and REDEFINE mapping is depicted in figure [15] As shown in the figure [15] for Tile array of size $2 \times 2$, we follow scheme 1 where input matrix is partitioned in to sub-matrices of $2 \times 2$. For Tile array of size $3 \times 3$ the input matrix is partitioned in to sub-matrices of size $3 \times 3$ as and the input matrix, the scheme 1 is used to sustain computation to communication ratio. In implementation of dgeqrfggr, we update trailing matrix using dgemm while in implementation of dgeqr2ggr, the trailing matrix is updated using DET2 instructions. Attained speed-up over sequential realization in different Tile array sizes and matrix sizes is shown in figure [15].

Speed-up in dgeqr2ggr, dgeqr2, dgeqrf, dgeqrft, and dgeqr2ht over sequential realizations of these routines. It can be observed in the figure [16(a)] that the speed-up attained in dgeqr2ggr is commensurate with the Tile array size in REDEFINE. For a Tile array size of $K \times K$, speed-up asymptotically approaches $K \times K$ as depicted in the figure [16(a)] Performance of dgeqr2ggr, dgeqrfggr, dgeqr2, dgeqrf, dgeqrft, and dgeqr2ht in-terms of theoretical peak performance of Tile array size is shown in figure [16(b)]. It can be observed in the figure [16(b)] that dgeqr2ggr can attain up to 78% of the theoretical peak performance in REDEFINE for different Tile array sizes.

6 CONCLUSION

Generalization of Givens Rotation was presented that resulted in lower multiplication count compared to classical Givens Rotation
operation. Generalized Givens Rotation was implemented on multicore and General Purpose Graphics Processing Units where the performance was limited due to inability of these platforms in exploiting available parallelism in the routine. It was proposed to move away from traditional software packages based approach to architectural customizations for Dense Linear Algebra computations. Several macro operations were identified in Generalized Givens Rotation and realized on a Reconfigurable Data-path that is tightly coupled to pipeline of a Processing Element. Generalized Givens Rotation outperformed Modified Householder Transform presented in the literature by 10% in Processing Element where Modified Householder Transform is implemented with similar approach of algorithm-architecture co-design. For parallel realization, the Processing Element was attached to REDEFINE Coarse-grained Reconfigurable Architecture as a Custom Function Unit and scalability of the solution was shown where speed-up in parallel realization asymptotically approaches Tile array size in REDEFINE.

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(b) Performance of dgeqr2ggr, dgeqrfgr, dgeqr2, dgeqrf, dgeqrfht, and dgeqrf2ht in PE In-terms of Theoretical Peak Performance Normalized to Performance of dgemm in the PE

(c) Performance of dgeqr2ggr, dgeqr2, dgeqrf, dgeqrfh, and dgeqrf2ht in PE In-terms of Gflops/watt

(d) Performance Improvement of dgeqr2ggr, dgeqr2, dgeqrf, dgeqrfht, and dgeqrf2ht in PE over Different Platforms

Fig. 13: Performance of dgeqr2ggr in PE

Fig. 14: Experimental Setup in REDEFINE with PE as a CFU
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(a) Speed-up in dgeqr2ggr, dgeqrfggr, dgeqr2, dgeqrf, dgeqrf2ht, dgeqrfht Routines in REDEFINE over Their Sequential Realization in PE

(b) Performance of dgeqr2ggr, dgeqrfggr, dgeqr2, dgeqrf, dgeqrfht, and dgeqrf2ht in REDEFINE In-terms of Theoretical Peak Performance of REDEFINE

Fig. 16: Performance of dgeqr2ggr in PE

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