Anisotropic plasma etching of Silicon in gas chopping process by alternating steps of oxidation and etching

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Abstract. In the present work a two-stage process for deep anisotropic etching of Silicon based on alternating steps of etching in SF₆ plasma and passivation of Silicon surface by oxidation in O₂ plasma is proposed. This developed Ox-Etch process has advantages of being free from deposited polymers on sidewalls and does not use cryogenic equipment. Etched structures show anisotropic profile with vertical scalloped walls similar to Bosch and STiGer processes. Selectivity of Silicon etch process with respect to SiO₂ mask is up to 120:1. The investigations of etching results depending on process parameters are presented. Main control parameters for Ox-Etch process defining the etch rate and degree of anisotropy are the durations of etch and oxidation steps.

1. Introduction

Anisotropic deep etching of Silicon by chemically active low temperature plasma is widely used for manufacturing in microelectronics and Si-based micromachining. Typical pattern size of etched features is from tens nanometers to 1 µm, and etch depth is from tens to hundred micrometers. Such microstructures are used in DRAM capacitors, TSV in interposers for 3D integration, MEMS sensors (gyro, accelerometers, actuators, microfluidics etc.).

The highest rate of etching is achieved in Fluorine-based plasma of SF₆ gas because of Fluorine atoms are easily detached from SF₆ molecules, and anisotropic reaction with Silicon is accelerated by ions flow normal to surface. The main problem is spontaneous lateral etching of structure sidewalls due to high reactivity of fluorine radicals. To suppress parasitic lateral etching and to get appropriate etch profile, a passivation of sidewalls by specific films is used. This passivation films should be produced in the same continuous process or in step-wise process.

Most often passivation films is a polymers coming from polymerizing plasma of gases C₄F₈, C₃F₈ or CHF₃ [1]. This process is consisted of the cyclic isotropic Silicon etching and fluorocarbon-based protection film deposition on sidewalls by fast gas switching (chopping). The SF₆ plasma steps etches the Silicon, and the C₄F₈ plasma steps deposits protection layer. After completing of microstructure etching the polymer layer should be removed from sidewalls by additional plasma stripping and wet chemistry operations. These operations are quite difficult for microstructures with deep blind holes and trenches.

There exists more clean cryogenic deep silicon etching processes. First version is continues regime with SF₆+O₂ plasma [2] and the second is gas chopping process SiF₄+O₂/SF₆ which is patented as STiGer etch process [3]. Both processes require cooling the Silicon wafer up to -100°C and utilize the Si₃F₆O₂ passivation layer stable only at cryogenic temperature. This layer completely evaporates at room temperature after cryo-process.

Obviously, the temperature stability of Si₃F₆O₂ film depends on content of fluorine, and without fluorination the SiO₂ film is remarkably stable at room temperature and higher temperatures.
2. Experimental details

In the present work a three-step cyclic process for deep etching of Silicon based on alternating steps of Silicon oxidation in O\textsubscript{2} plasma, the breakthrough of bottom oxide by Ar\textsuperscript{+} or SF\textsubscript{6}\textsuperscript{+} ions, and Silicon etching in SF\textsubscript{6} plasma is proposed (Figure 1). This developed Ox-Etch process has advantages of being free from deposited polymers and does not use cryogenic equipment.

![Proposed process and schematic of etching](image)

**Figure 1.** Proposed process and schematic of etching. The black line denotes a SiO\textsubscript{2} mask, and red line is SiO\textsubscript{x} passivation film recoverable at each passivation step, respectively.

Processes were carried out at room temperature in plasma etchers with high density ICP plasma source (RF frequency of 13.56 MHz and 2 MHz was used, RF power 800 – 1750 W) at chamber pressures of 5-20 mTorr. Wafer bias was in range of 30 – 50 V during etching step, and 0-30 V during oxidation step. Plasma discharge had a continuous mode to avoid effects of low reproducibility of ignition time. In order to check that Fluorine or Oxygen particles completely purged from reactor during the next step, OES monitoring of intensity for O\textsuperscript{*} (777.4 nm) and F\textsuperscript{*} (685.6 nm) lines were performed during the etch process (Figure 2). The graph shows that the process of gas exchange in the chamber takes time about 2 s which imposes a physical limit on the minimal duration of each step in a used equipment.
Experiments were carried out on Silicon wafers (100) (n-type, 10-20 Ohm·cm). Hard mask of SiO$_2$ layer of 1-2 µm was made by lithography with patterns of cylindrical holes with diameters of 2-75 µm and lines sized at 8-16 µm. Silicon oxidation by O$_2$ plasma was studied by in situ spectral ellipsometry on bare wafer surface during oxidation step of process. It was shown that without wafer biasing the oxide film grows up to 5 nm within time of 3-5 s. Under bias of 30-60 V oxide thickness saturates at 5-7 nm where growth of SiO$_x$ stops due to balance between oxidation and ion sputtering rates.

In situ measurements of plasma oxidation of Silicon by spectral ellipsometry
The spectral ellipsometer Woollam M-2000X was used (246-998 nm spectral range, 73.2° incidence angle) used for in situ measurements was attached on ellipsometric ports of plasma chamber. Data acquisition takes about 0.5 s with pause between measurements of 0.5 s. Data were processed after end of plasma oxidation experiments using an optical model for native oxide and known dependency of optic constants from temperature for Silicon which allows simultaneous measurements of oxide thickness and wafer temperature in plasma process.

In all plasma oxidation experiments Silicon temperature didn’t exceed 100°C, which indicates that reaction of surface oxidation has a non-thermal nature of activation, but occurs solely through the action of excited Oxygen radicals and accelerated ions flow.

Figure 3 depicts growth of SiO$_2$ thickness during plasma oxidation without bias applied to wafer. In the range 0-2 s the oxidation is too fast to be measured by applied in situ technique with available temporal resolution, but then growth rate become 0.01-0.1 nm/s and steadily decrease with thickness. Such kinetics couldn’t be described by Deal-Grove model for thermal oxidation of Silicon. Under experimental conditions the oxide thickness after 10 s of process is in 1.4 - 2.4 nm range. This should be the case on sidewalls of the trench (or hole), since they are not subject to significant bombardment of ions accelerated by electrical bias of wafer.
Figure 3. Spectral ellipsometry measurements of Silicon oxide growth during plasma oxidation in ICP etcher without wafer biasing.

Figure 4 shows growth of oxide thickness during plasma oxidation with wafer bias applied. It is seen that initial stage of oxidation is much faster than in the previous case, forming 2.5-3 nm of oxide within 2 s. If the bias potential does not exceed 40 V threshold the oxidation continues with gradual lowering rate. When the bias is higher than 40 V the oxide thickness saturates at some value at which rate of oxidation is equal to the rate of sputtering surface of oxide by accelerated ions.

Figure 4. Process of Silicon oxide growth measured by spectral ellipsometry in situ during plasma oxidation with wafer bias applied (chamber pressure is 6 mTorr).

4. Experimental results on anisotropic Silicon etching

Figure 5 shows example of etched structure in optimized process (etching and oxidation times are 10 s, \( W_{\text{ICP}}=1750 \) W, \( P=10 \) mTorr, 200 cycles). It can be seen that etch depth depends on lateral feature size and feature type (trench or cylindrical hole). Results on etch depth for different microstructures from same sample are summarized in the graph (Figure 6). The ARDE (aspect ratio dependent etching) effect...
was clearly observed, the dependence of the anisotropic etch rate on the ratio of the depth of the hole/trench to its diameter/width was quite pronounced. The physical mechanism of this effect consists in limiting the isotropic flux of active particles from the plasma to the bottom of microstructure through the input aperture of mask. Obviously, the effect is more pronounced for the holes than for the trenches, since in the case of a trench there is no restriction on the motion of the particles along it.

Figure 7 shows roughness of sidewall in the optimized process which could be estimated as low as 50 nm which is comparable to optimized Bosch process.

![Figure 5. Example of optimised process results](image)

![Figure 6. Etched depth in adjusted recipe of plasma etching depending on lateral feature size](image)

![Figure 7. Sidewall profile of trench etched in Silicon by Ox-Etch process.](image)
The process could be optimized by choice of durations of etching and oxidation steps. Taking the process with $t_{\text{ox}}=t_{\text{etch}}=10\text{ s}$ as a starting point, the variation of this parameter gives different results (Figure 8). It can be seen that moderate decrease of oxidation time to $t_{\text{ox}}=8\text{ s}$ does not increase anisotropic etch rate, but removes scallops on etch profile and increase undercut under mask (Figure 8b). Increasing etching step duration leads to damage the passivation layer which is unable to save the sidewalls during etching. Defects are formed with partial destruction of passivation film at upper part of microstructure where ion bombardment of sidewalls is most intensive. This part is also poorly protected in subsequent long etch steps and continues to deteriorate. Effect takes place only at the top of the hole, since in the lower ratio of the passivation rate and etch rate it is evidently changing in favour of the latter.

![Figure 8](image)

**Figure 8.** Oxidation and etching step duration optimisation: a) $t_{\text{ox}}=t_{\text{etch}}=10\text{ s}$, b) $t_{\text{ox}}=8\text{ s}$, $t_{\text{etch}}=10\text{ s}$, c) $t_{\text{ox}}=10\text{ s}$, $t_{\text{etch}}=13\text{ s}$.

The gas pressure in chamber during the process also affects the shape of the etched structures. Figure 9 compares the etching processes carried out in a pressure range of 5 - 20 mTorr under otherwise equal conditions. Table 1 shows the quantitative results of SEM measurements from these samples. It is seen that as the pressure increases, the ratio of the rates of passivation and etching on the sidewall increases, resulting in structures with a smaller undercutting. On the other hand, the vertical etching rate increases, which could be explained by the increase in fluorine radical density in plasma with pressure. An important result is a decrease in the rate of degradation of SiO$_2$ mask with increasing pressure, which gains the selectivity of etch process.

![Figure 9](image)

**Figure 9.** Gas pressure effect on the Ox-Etch process.

In chamber pressure: a) $p=5\text{ mTorr}$, b) $p=10\text{ mTorr}$, c) $p=15\text{ mTorr}$, d) $p=20\text{ mTorr}$
Table 1. Pressure effect on the etch depth, undercut and selectivity.

| Pressure, mTorr | Depth, µm | Undercut, nm | Selectivity |
|----------------|-----------|--------------|-------------|
| 5              | 12.27     | 690          | 39          |
| 10             | 14.34     | 420          | 55          |
| 15             | 16.23     | 300          | 116         |
| 20             | 17.39     | 150          | 102         |

5. Conclusion
The room temperature three-step polymer free oxidation-etching process is developed for anisotropic etching of Silicon in HDP-plasma (Ox-Etch process). The mandatory condition for success of Ox-Etch gas chopping process implies that reduction in sidewall oxide thickness during the etching step should be compensated during following oxidation step. Typical duration of passivation and etching steps do not exceed 10 s, and the mean anisotropic etch rates of Silicon up to 3 µm/min are achievable without noticeable undercut. Etched microstructures show anisotropic profile with vertical scalloped walls similar to Bosch and STiGer processes. Selectivity of Silicon etching with respect to silicon oxide mask is up to 120:1. Main control parameters for Ox-Etch process which determines the etch rate and degree of anisotropy are the duration of each step and gas pressure in plasma chamber. Developed Ox-Etch process could be put into practice for applications where contamination of Silicon microstructures sidewalls after etching could be a critical obstacle. After Ox-Etch process the chemical content of passivation layer on microstructures is close to native SiO₂.

6. Acknowledgements
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7. References
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