Self-timed Reinforcement Learning using Tsetlin Machine

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Abstract—We present a hardware design for the learning datapath of the Tsetlin machine algorithm, along with a latency analysis of the inference datapath. In order to generate a low energy hardware which is suitable for pervasive artificial intelligence applications, we use a mixture of asynchronous design techniques—including Petri nets, signal transition graphs, dual-rail and bundled-data. The work builds on previous design of the inference hardware, and includes an in-depth breakdown of the automaton feedback, probability generation and Tsetlin automata. Results illustrate the advantages of asynchronous design in applications such as personalized healthcare and battery-powered internet of things devices, where energy is limited and latency is an important figure of merit. Challenges of static timing analysis in asynchronous circuits are also addressed.

I. INTRODUCTION

We present a comprehensive design and analysis for an asynchronous learning datapath based on the Tsetlin machine (TM) algorithm. When coupled with asynchronous inference hardware [1], a complete asynchronous TM capable of online learning is formed. We also analyze the latency of the inference datapath, showing its evolution during training.

The TM [2] algorithm is effective in many large classification problems [3, 4, 5]. In addition, the TM’s reinforcement learning and logic-based inference make it a good candidate for energy efficient hardware [6]. We design an energy-frugal TM hardware with a view of use cases in pervasive artificial intelligence; e.g. in personal healthcare, accessibility, environmental monitoring and predictive maintenance. We give a brief introduction to the TM algorithm in Section II.

We wish to implement the TM using asynchronous circuits as they can be beneficial for low energy sensing systems [7], when tightly coupled with analog blocks [8], and when power delivery is unstable or unpredictable [9]. These features are often present in the aforementioned applications [10].

The architecture of the hardware is designed using a hybrid Petri net model in Section III. The model incorporates inference and learning components.

TMs use groups of reinforcement automata, called Tsetlin automata (TAs), to create an ensemble learning effect. We decompose the automata reinforcement feedback into three stages to aid the hardware design in Section IV.

The reinforcement process of the TM involves random choice with defined probabilities—some fixed and some varying at runtime. These probabilistic choices enable diversity of learning in the TAs. We design a quasi delay insensitive (QDI) pseudorandom bit generator (PRBG) for this use in the TM in Section V and motivate its use in other low power applications.

Considering the implementation of the state-holding TAs, we compare QDI and bundled-data (BD) design styles suitable for the low energy applications in Section VI. The comparison will show the limitations of the two asynchronous design methods in terms of area, energy and scalability. We use the WORKCRAFT framework [11] for specification and synthesis of the QDI implementation using signal transition graphs (STGs), as well as verification of the STG properties required for a functional and robust design. For BD, we are inspired by the desynchronization workflow of Cortadella et al. [12] in using a commercial synthesis tool designed for synchronous design. BD circuits are readily-implementable with industrial-quality tools, in contrast with QDI circuits.

Main contributions of this work:

- Visualization of an asynchronous TM hardware architecture using Petri nets (Section III).
- Latency analysis of the asynchronous TM inference datapath from III and its evolution during training (Section III).
- A detailed decomposition of TA reinforcement feedback into three stages (Section IV).
- Design of a QDI PRBG for probabilistic choice in the TM and other low power applications (Section V).
- Comparison of QDI and BD implementations of the TA for low energy hardware (Section VI).

II. Tsetlin Machines in Brief

TMs learn patterns in binary data using propositional logic. The main inference component of the TM is the clause that composes an AND expression of the input features and their...
complements. The TM comprises many clauses, each producing a vote. The composition of each clause is controlled by a vector of exclude bits (see Figure 1). These bits are parameters that are learned by teams of TAs.

Each clause can produce a vote for its class. The algorithm states that half of the clauses vote positively, while the other half of the clauses vote negatively (we will denote this by the boolean $c_{neg}$). The inclusion of inhibition in the voting system enables non-linear decision boundaries in the inference process. A majority vote gives an indication of class confidence. This confidence is used to classify the input data and influence future decisions of the automata through the feedback mechanism [2]. In this work we consider only the single class TM for simplicity.

The TA is a class of finite reinforcement automaton [13]. It produces an exclude output for states below the midpoint, and include for states above the midpoint as illustrated in Figure 2. The TA receives a penalty or reward from the feedback mechanism based on the current state of the TM. Continued rewards in the end states cause the TA to saturate. A penalty in one of the midstates ($n$ or $n + 1$) causes the TA to transition across the decision boundary—inverting its output from exclude to include, or vice versa. The feedback mechanism is described in more detail in Section IV.

### III. ASYNCHRONOUS TSETLIN MACHINE

Figure 3 is an architectural diagram for the asynchronous implementation of the TM shown in Figure 1 demonstrating the scalability of the design. The diagram can be composed with the Petri-net-like tiles in Figure 4 to form a visualization of the complete system. In these diagrams, rectangles represent transitions or computations, and circles represent places as in classical Petri nets. When abutting these tiles, adjoining places are reduced to a single place. This representation of the system is not a formalism.

The main structure is a $3 \times 3$ grid constructed with feature inputs in rows and clauses in columns. The small size facilitates the explanation of the system, but the architecture can be easily extended by appending clause columns to the right side, or feature rows below $f_3$.

The clause tile is detailed in Figure 4a and comprises a partial clause (PC) computation for the feature input and its complement (as introduced in Section IV); a partial feedback calculation for stage three feedback (FB3); and two TAs. The feedback stages will be discussed later in Section V.

The clause sum is computed in the sum tile at the bottom of each clause column. Figure 4b details the sum tile. Stage two feedback (FB2) for the clause is computed at this stage using the clause sum.

The diagrams capture the potential for both concurrency and serialization in the design. As presented, the system operates in a serialized manner where the feature inputs are passed through each clause in series. By contracting the places in the highlighted regions of Figure 4a, tokens are passed to the right without waiting for PC calc and FB3 calc, this allowing clauses to compute in parallel.

The majority of the system is implemented in a dual-rail (DR) style using a reduced completion detection (RCD) scheme [7]. However, the TAs are implemented in a single-rail (SR) style (as indicated in Figure 4a) which will be motivated and discussed in Section VII.

The RCD scheme is a simplified scheme which completion detects only the outputs of a block. This brings benefits of early propagation and drastically reduced area and power overheads versus traditional full completion detection. The trade-off is an added timing assumption on the return-to-idle phase of the DR signals. Full details of the RCD scheme are
In the following sections we will explore the inference circuit delays and analyze the inference latency of the asynchronous datapath with differing input operands. For synthesis we use a commercial, off-the-shelf technology library: UMC 65 nm LOW-LEAKAGE, herein referred to as UMC65LL.

**B. Delay Analysis**

Since we use an RCD scheme which enables early propagation [11], the delays of the circuits can vary based on the input operands. We analyze the delay distributions of the inference circuits using uniformly-distributed random inputs to gain an understanding of this phenomenon. We will use this to explain the evolution of latency during training in the next section.

**Clause:** In the worst-case delay no literals are excluded (\( e = 0 \)), all feature inputs are logic-1 (\( f = 1 \)); therefore the delay is bounded by the slowest input and the delay arc is through the positive rail. In the best-case delay, all but one literal is excluded and the literal is logic-0; therefore the delay is bounded by signal propagation through the OR tree in the negative rail. Since the clause is a large AND tree, there is a high probability of \( c = 0 \), so the delay distribution is mostly clustered at the lower end as Figure 6 shows. A much smaller portion is seen towards the circuit’s maximum delay and is associated with \( c = 1 \).

**Population Count:** The delay of the circuit is bounded by the carry chain formed by \( \text{HA}_8, FA_0 \) and \( FA_1 \). In the best case there are no carries and the circuit latency is governed by the longest logic path which comprises the first two layers of \( \text{HA}_8 \) (which have roughly equal paths), through the OR gates and finally \( FA_0 \) to the \( y_1 \) output. In the worst case, output \( y_3 \) must wait for the aforementioned best-case path as well as the carry through \( FA_1 \). This leads to the log-normal-like delay distribution seen in Figure 6.

**Magnitude Comparator:** For uniform random inputs and a normalized worst-case delay of 1, the comparator achieves a mean delay of 0.05. This is attributed to early propagation and the evaluation of single-bit comparisons from MSB to LSB. The delay of the circuit increases as the absolute difference between operands decreases, because more of the MSBs are equal. This circuit is therefore fastest during inference and the later stages of training. The operand space halves for each single-bit comparison leading to the negative exponential delay distribution in Figure 6.

**C. Operand-dependent Inference Latency**

We investigate the evolution of inference latency during training by plotting the spacer → codeword latency at different stages. We use a binarized version of the IRIS Flower dataset¹ to provide feature inputs (f). Exclude inputs (e) are retrieved from a TM pre-trained on the same dataset after the specified number of epochs. Figure 7 shows the distributions for the untrained TM, and the trained TM after 4 epochs and 50 epochs. The plots show the trend of the mean towards greater circuit delay as the TM is trained and therefore more clauses become

Inference Circuits

The inference datapath comprises the clauses, majority voting and classification introduced in Figure 1. Clauses are separated into partial clause calculations as discussed earlier in this section and can be implemented by the schematics in Figures 5a and 5b. Feature inputs occur in DR encoding along with exclude signals \( e_0 \) and \( e_1 \). The outputs of the partial clause are combined using a DR AND tree.

Majority voting calculated the sum of the clause votes \( (c_{\text{sum}}) \) and is implemented using DR population count. The schematic in Figure 5c shows the implementation based on DR half- and full-adders. The OR gates and wires in this circuit are also implicitly DR encoded. Two spacer inverters (spinv) are required to ensure uniform spacer polarity at the outputs.

For this single class TM example, the output is classified using a threshold function in the form of a magnitude comparator. The magnitude comparator lends itself to low energy implementation in DR and saves energy by evaluating single-bit comparisons from most significant bit to least significant bit only if needed, all within the period of one cycle [11]. To expand the example to two classes or more, an argmax function would take the place of thresholding.

1Available: https://github.com/cair/TsetlinMachine
activated during the computation of each datapoint ($c = 1$). In this case we see more examples from the right side of the clause delay distribution in Figure 6. This is the main contributor to the increase in mean latency as the system becomes more trained. The magnitude comparator offers a net decrease in mean latency as training progresses since the difference between input operands will increase, meaning we shift towards the left of the distribution in Figure 7. However this shift is somewhat smaller than that of the clauses, and it therefore has a lesser effect on the inference datapath. The distribution of the population count is much more uniform than that of the other circuits, and therefore has a negligible effect during training.

IV. DECOMPOSITION OF FEEDBACK

During learning, feedback is given to each TA to influence its future action, and therefore control pattern detection in the TM as a whole. The feedback is based on a carefully-designed payoff matrix [2, p. 10] and is split into two categories: Type I and Type II. Type I feedback reinforces good decisions and penalizes false negative outputs. Type II feedback combats false positives by penalizing TAs that exclude when $c = 1$.

We decompose the feedback logic into three stages based on scope: FB1 at TM level, FB2 at clause level, and FB3 at TA level. FB1 and FB2 are assigned types: none, T1 or T2; these are based on the Type I and Type II concepts introduced previously. FB3 assigns an action to a single TA: penalty, reward or inaction; and is based on the outcomes of the payoff matrix. Each feedback stage’s output is input to the next, until finally the output of FB3 is input to the corresponding TA. The following sections discuss each feedback stage in detail. Finally we will discuss the synthesis of the feedback circuits in the DR style in Section IV-D.

A. FB1: TM-level Feedback

Inputs: learn, $y_{\text{exp}}$

Output: Feedback type (none, T1 or T2)

The first stage broadly enables feedback for the entire TM if learn is asserted. The feedback type is chosen according to $y_{\text{exp}}$—the expected class as provided by the labeled data—as follows:

$$FB1 = \begin{cases} 
\text{none, for learn} = 0 \\
T1, \text{ for learn} = 1, y_{\text{exp}} = 1 \\
T2, \text{ for learn} = 1, y_{\text{exp}} = 0 
\end{cases}$$

B. FB2: Clause-level Feedback

Inputs: FB1, $c_{\text{neg}}, p_r$

Output: Feedback type (none, T1 or T2)

The second stage swaps the feedback type from T1 to T2, or vice versa if the associated clause is negated ($c_{\text{neg}} = 1$, discussed in Section II). Additionally, feedback is stopped (inaction given) if the number of activated clauses (those producing a logic-1 at the output) meets the threshold, $T$. This is determined by probabilistic choice, $p_r$, which is discussed at the end of this section. If there is no feedback from the previous stage (FB1 = none), then none will be generated (FB2 = none). Parameter $c_{\text{neg}}$ is determined at design time, therefore the logic for FB1 can be separated and depends only on FB1 and $p_r$. This will be demonstrated in Section IV-D.

Clause-level feedback can be summarized as follows:

$$FB2 = \begin{cases} 
\text{none, for } FB1 = \text{none} \\
\text{none, for } FB1 = T1, p_r = 0 \\
\text{none, for } FB1 = T2, p_r = 1 \\
T1, \text{ for } c_{\text{neg}} = 1, FB1 = T2, p_r = 0 \\
T2, \text{ for } c_{\text{neg}} = 1, FB1 = T1, p_r = 1 \\
T1, \text{ for } c_{\text{neg}} = 0, FB1 = T1, p_r = 1 \\
T2, \text{ for } c_{\text{neg}} = 0, FB1 = T2, p_r = 0 
\end{cases}$$

We do not consider boosting of true positive feedback, which is an option in the original algorithm.

Figure 6. Latency distributions of the Tsetlin machine inference datapath and its components for uniformly-distributed random inputs. Post-synthesis results using the UMC 65 nm LOW-LEAKAGE library.

Figure 7. Latency distribution of the Tsetlin machine inference datapath for the IRIS dataset.
Table I

TRUTH TABLE FOR FB3. x = DON’T CARE.

| FB2 | inc c | x | p_s | FB3 |
|-----|-------|---|-----|-----|
| none | x | x | x | x | inaction |
| T1 | 1 | 0 | 0 | 0 | inaction |
| T1 | 1 | 0 | 1 | 1 | inaction |
| T1 | 1 | 1 | 0 | 1 | reward |
| T1 | 1 | 1 | 1 | 0 | penalty |
| T1 | 0 | 0 | 0 | 1 | reward |
| T1 | 1 | 0 | 0 | 0 | inaction |
| T1 | 0 | 1 | 0 | 0 | inaction |
| T1 | 0 | 1 | 1 | 1 | penalty |
| T1 | 0 | 0 | 1 | 1 | inaction |

The TM algorithm describes probabilities of generating T1 and T2 [2, p. 10]. In this work we refer to them as \( P(T1) \) and \( P(T2) \) which are based on \( c_{\text{sum}} \) and T as follows:

\[
P(T1) = \frac{T - \text{clamp}(c_{\text{sum}})}{2T}, \quad P(T2) = \frac{T + \text{clamp}(c_{\text{sum}})}{2T},
\]

where the clamp function restricts its argument to \([-T,T]\) such that the probabilities lie in the range \([0,1]\). As the number of activated clauses (those producing \( c = 1 \)) approaches \( T \), the probability of the TA's in that clause receiving feedback decreases. In order to generate a randomized choice based on these probabilities, we could assign booleans as follows:

\[
q_1 = \text{rand} < P(T1), \quad q_2 = \text{rand} < P(T2)
\]

where \( \text{rand} \) is a real number in the range \([0,1]\). Since \( P(T1) \) and \( P(T2) \) are complementary in the range \([0,1]\), \( q_1 \) and \( q_2 \) are also complementary in the binary domain and therefore \( q_3 = q_1 \). We therefore introduce a single new signal for FB2, \( p_s \), which takes the place of the preceding probabilities. The generation of this signal will be discussed in Section V.

C. FB3: TA-level Feedback

**Inputs:** FB2, inc, c, x, p_s

**Output:** TA action (inaction, penalty or reward)

The third and final feedback stage translates the feedback type from FB2 into a TA action for the specified TA based on: the TA's current action, encoded as \( \text{include} \) in signal inc; the current clause output, c; the feature of complemented feature (f or t) associated with the TA, x; and a probabilistic choice component, \( p_s \).

The FB3 output is chosen according to Table I where \( p_s = 1 \) denotes that the higher probability \( (s - 1)/s \) option is chosen from the payoff matrix. \( p_s = 0 \) denotes that the lower probability \( 1/s \) is chosen. The generation of signal \( p_s \) will be discussed in Section V.

D. Synthesis of Feedback Circuits

Using one-hot encoding in the feedback circuits maintains direct compatibility with the inference datapath and ensures speed independence, which is important for hazard-freeness. Signals inc, c, x are already one-hot encoded (dual-rail) for the inference circuits in Section III so these encodings are reused here in the learning circuits. Furthermore, we encode FB1 as follows, and FB2 similarly: FB1 = \{FB1^T2, FB1^T1, FB1^none\}, FB3 describes TA actions and is encoded as: FB3 = \{FB3^r, FB3^p, FB3^i\}, for reward, penalty, inaction respectively. Note that rail orders do not matter as we refer to the rails by name. In this way, to indicate T2 feedback on FB1, we would set \( FB1^T2 = 1, FB1^T1 = 0, FB1^\text{none} = 0 \).

Using the previously defined logic, we can generate circuits for the feedback. The implementation of stage two feedback depends on the clause polarity—it being either negated (\( c_{\text{neg}} = 1 \)) or non-negated (\( c_{\text{neg}} = 0 \)). Note that the stage one circuit is instantiated \textit{once per TM}, the stage two circuit \textit{once per clause}, and the stage three circuit \textit{once per TA}.

In stage three, the FB2 signal is shared throughout the TAs within the same clause. For this reason, we carefully design the logic so that FB2 signals are injected as close to the outputs as possible, making the propagation path the shortest. Therefore when FB2 = 0, the computation on the corresponding FB3 rails will conclude rapidly, and for all TAs in the clause.

V. Generation of Random Bits \( p_r, p_s \)

We introduced two distinct probabilistic choice mechanisms in Section IV. In Section IV-B we introduced the signal \( p_r \): a probabilistic boolean chosen at the clause level which may force FB2 = none. This boolean is dependent on \( T \) and \( c_{\text{sum}} \). The probability of \( p_r = 1 \) varies at runtime according to \( c_{\text{sum}} \). In Section IV-C we introduced the signal \( p_s \), which is a random boolean generated for each TA. It is required under certain circumstances to choose between two TA actions. This boolean is dependent on \( s \) and is fixed during runtime.

From these requirements, we must be able to generate \textit{biased} random bits: bits where \( P(1) \neq 0.5 \) (unbiased random bits have \( P(1) = 0.5 \), such as those generated by a linear feedback shift register (LFSR)). In addition, we must be able to vary \( P(1) \) at runtime for \( p_r \). Probabilistic choices are used in the TM to ensure diversity of learning. A pseudorandom generator is sufficient to satisfy these needs, and benefits from higher energy efficiency than a \textit{true} random generator.

Due to the requirement of PRBGs for each TA, and additionally for each clause, their area and energy consumption are of utmost importance. We chose to implement a PRBG based on the principles of irregular sampling of a regular waveform, as this allows us to minimize the overheads and take advantage of the asynchronous nature of the rest of the system.

A. Asynchronous Sampling of Clock with Variable Duty Cycle

We take advantage of the asynchronous inference logic by using asynchronous handshakes to sample a regular clock waveform. A clock with \( 50\% \) duty cycle will generate unbiased random bits. A clock can be generated using a ring oscillator (RO). To ensure random sampling, the clock and handshake must be \textit{uncorrelated}. ROs can be gated by adding a \texttt{NAND} or \texttt{NOR} gate into the ring. However this technique will disadvantage us in this case as the RO will always start up in the same phase, therefore the clock and sampling signals may become correlated.

We take advantage of the properties of a purely inverter-based RO. The RO can be power gated using header/footer transistor when entropy generation is not required. Such an RO
will start up in a non-deterministic phase according to thermal noise and other effects in the inverters.

To generate biased bits for $p_r$ and $p_s$, we need to vary the duty cycle of the clock. Agustin and Lopez-Vallejo [14] show how to construct an RO such that each tap has a unique duty cycle. This is achieved by using inverters with asynchronous rise/fall times. For example, odd inverters have fast rise and slow fall times, and even inverters vice versa. This can be done via transistor sizing (ie. in the silicon library), or altering supply voltage to the inverters (ie. at implementation stage). Using this RO setup, we can multiplex between taps to obtain different clock duty cycles, and therefore alter our PRBG probability at runtime.

We have introduced a clock into our asynchronous circuit, and this may seem counterintuitive, however the load on this clock (and therefore its energy consumption) will be low compared with fully synchronous designs where the clock drives large numbers of flip-flops. In Section V-B we will investigate the optimal number of PRBGs required. By taking this distributed PRBG approach, we can vastly reduce the circuit area compared with a naive approach using one LFSR per TA.

Figure 8 shows the circuit used to sample the asynchronous req input. The mutex ensures $\text{ack}^p$ and $\text{ack}^n$ outputs are mutually exclusive. These outputs represent the random output bit with a dual-rail encoding. That is for $\{\text{ack}^p, \text{ack}^n\}$: $\{0, 1\}$ represents logic-0, and $\{1, 0\}$ logic-1. $\{0, 0\}$ is the spacer or null state used to separate valid output values temporally.

When the clk and req signals are both low, the output will be in the spacer state. If a request is made (by asserting req) during the low period of the clock, the output of the set-dominant latch is reset, and req wins the mutex, resulting in $\text{ack}^n$ asserting. If clk rises now, the output of the latch rises, however the mutex is still held by req. A following deassertion of req will result in clk gaining the mutex, however $\text{ack}^p$ will be masked by the AND gate.

If a request is made during the high period of clk, the output of the latch will already be high and clk will have won the mutex. On the rise of req the AND gate will unmask $\text{ack}^p$. If clk falls now, the output of the latch remains high since the R input is inactive, and therefore $\text{ack}^p$ also remains high.

The circuit is synthesized for the UMC65LL cell library and the results are summarized in Table I. The asynchronous handshake shows almost $10\times$ saving in area compared to an 8-bit LFSR. Power and energy are also drastically decreased. The asynchronous handshake is well suited to energy-conscious, pervasive applications.

### B. Optimal Number of PRBGs

The original TM algorithm takes a probabilistic choice for every TA update involving $s$. However Abeyrathna et al. [15] show that randomizing every $d$th TA update can save energy with a minimal drop in test accuracy. With $d = 1000$, an accuracy within 2% of $d = 1$ was maintained for three of the four datasets tested.

### VI. ASYNCHRONOUS TSERLIN AUTOMATON

In a TM, the TAs consume most of the hardware resources [6]. The number of TAs is given by $N_{TA} = 2N_{Classes}N_{Clauses}N_{Inputs}$. Therefore the goal is to create a lightweight TA implementation with a focus on area and energy. The TA hardware must implement the finite state automaton described by the state diagram in Figure 2.

This section explores two methods for the design of a TA. Firstly a QDI approach starting from an STG specification; and secondly a BD approach starting from a traditional synchronous specification, using matched delays to time the design. The designs will be compared with a synchronous implementation.

#### A. Quasi Delay Insensitive Approach

The STG in Figure 3 represents a one-hot finite state machine (FSM) for a two action, six-state TA (for the definition of STGs, see [16]). The inputs $p$ and $r$ come from the FB3 rails $FB^3p$ and $FB^3r$ which were introduced in Section IV-D. The $FB^3r$ rail denotes inaction and is only used for completion detection.

State bits are encoded in the $x_{s0}$ and $x_{s1}$ places at the top of the graph. States $x_{s0}$ ($x_{s1}$) are the action 1 (action 2) states—in these states the automaton is indicating the action to exclude (include) the feature or feature complement from the clause composition. The $x_{s1}$ ($x_{s3}$) states are the closest to (furthest from) the action decision boundary. As an example, when $x_{s1}$ holds a token, the automaton is indicating action 1 (exclude) strongly.

A token at $p_0$ denotes the idle state for the automaton. It offers a choice between penalty and reward represented by

![Figure 8. Handshake circuit for the asynchronous pseudorandom bit generator with dual-rail output.](image)

| PRBGs Synthesized for UMC 65 nm Low-Leakage Silicon Library. |
|-----------------|-------|-------|-------|-------|
| Implementation  | Area  | Cycle Time [ns] | Power [µW] | Energy [fJ] |
| LFSR8           | 92.2  | 0.38            | 6.41       | 2.44     |
| Handshake       | 9.72  | 0.23            | 0.621      | 0.143    |

Following on, we could hypothesize an optimal number of PRBGs to fulfill the needs of a given TM. If every 100th TA update is randomized, we will need to produce at most $N_{TA}/100$ probabilistic choices per learning phase.

This could result in a $100\times$ reduction in PRBGs for an LFSR-based design, in exchange for arbitration overhead to share one PRBG between multiple TAs. Similar could be said for the asynchronous handshake design, although the already small size of the design means that arbitration overhead would almost certainly result in a larger area than instantiating an asynchronous handshake PRBG for every TA.
signal transitions $p_+$ and $r_+$ respectively. Each subsequent branch from $p_+$, $r_-$ enables a transition in one of the action output signals $a_1, a_2$. Depending on the current action and the previous state, a state transition may also occur. The correct branch is chosen based on read arcs from the $x_{s+1}$ places. For example in the 2nd left-most branch of $r_-$, we transition from state $x_{12}$ to $x_{13}$. This happens by firstly giving the token from place $x_{13.0}$ to $x_{13.1}$, and secondly giving token $x_{12.1}$ to $x_{12.0}$.

After state transitions and action output have occurred, the acknowledge output, $ack$, makes a positive transition. Finally, the previously given input and action signals return low, followed by $ack$ and the token returns to $p_0$. The automaton is now ready for the next penalty or reward input.

The internal transitions $x_{s+}$ encode some information about the states in the STG. However, this is not enough to satisfy complete state coding (CSC) required for synthesis of the STG to logic gates [16]. In the previous example where we transition from $x_{12}$ to $x_{13}$, there is a point where tokens are held by both $x_{13.1}$ and $x_{12.1}$. The STG reaches this same state when transitioning in the opposite direction, from $x_{12}$ to $x_{13}$.

In order to achieve CSC, we introduce internal signals to encode the direction of travel of the state: $x_{sL+}, x_{sR+}$ for left and right. We insert these signals into every branch to maintain uniformity in the STG. Although not all these internal signals are strictly required, they ease scalability of the STG and help the synthesis tool to minimize and share logic efficiently.

The STG in Figure 9 passes all verification tasks required for synthesis of a correct and hazard-free circuit in the backend did not produce a result in a reasonable amount of time).

In order to read the state of the TA without giving penalty or reward (during inference for example), we add a latch to the output to store one of the $p$ or $r$ signals. The latch is controlled by the $ack$ handshake.

The STG state space expands exponentially as more signal transitions are added. This makes it difficult for the synthesis tool to handle TAs with more than three action states. Additionally there is a high possibility for human error when copying and editing branches of the STG. And as the number of TA action states increases, the graph becomes large and unwieldy to navigate. For these reasons we explore a BD approach to asynchronous TA design.

### B. Bundled-Data Approach

A synchronous one-hot FSM can be constructed using flip-flops as storage elements. The next state logic can be derived using the adjacent states and $p$, $r$ inputs as follows:

\[
\begin{align*}
  x_{13} &= x_{13} \cdot r + x_{12} \cdot r \\
  x_{12} &= x_{11} \cdot r + x_{13} \cdot p \\
  x_{11} &= x_{12} \cdot p + x_{21} \cdot p \\
  x_{21} &= x_{22} \cdot p + x_{11} \cdot p \\
  x_{22} &= x_{21} \cdot r + x_{23} \cdot p \\
  x_{23} &= x_{22} + x_{23} \cdot r + x_{22} \cdot r
\end{align*}
\]

This synchronous circuit is converted into a self-timed one through the process of desynchronization [12], by decomposing the flip-flops into master/slave latches and replacing the clock with handshake controllers and delays matched to the combinational logic paths. The timing of the resultant BD design is not as robust as the QDI approach in Section VI-A since the matched delays are fixed at design time and are subject to process, variation and temperature variations.

To reduce the overhead of the handshake controllers, we group the TAs into an array and use one handshake controller for many latches. Depending on the overall size of TM for the target application, the TAs could be grouped in different ways. A monolithic array will minimize controller overhead, however there comes a limit where buffers must be introduced into the latch enable signals to maintain integrity. At this point, it may become desirable to group the TAs by clause.

The specification of the BD design is easily scaled due to the use of parameterizable Verilog code. The workflow takes advantage of mature synchronous tools for synthesis.

### C. Synthesis Results

Timing and power analyses of asynchronous circuits need special consideration. In conventional synchronous static timing analysis, delay through logic gates is calculated using the input slew and output load capacitance. Power estimations also rely on these parameters. Synchronous tools cut combinational loops arbitrarily, therefore may be optimistic about slew, gate delays and internal power in asynchronous circuits which contain such loops.

To obtain results for the QDI design we use a specialized asynchronous static timing analysis tool [17] which takes into account the combinational loops in the timing calculation. The tool operates on the gate-level netlist and propagates slews iteratively through circuits with loops, therefore avoiding optimism in the slews and gate delays. In the case there are multiple paths in the circuit which begin and end at the same input/output combination, the tool uses the worst-case path to determine the cycle time.

Since the UMC65LL library does not contain C-elements, the QDI circuit is combinational with feedback loops. Table III shows a results summary of the TA implementations. All results are synthesis estimations and no layout is performed. In this case, the QDI circuit trades increased cycle time and energy for increased robustness to process, variation and temperature variations. The BD design strikes a good trade-off between performance, area and elastic timing to integrate with the rest of the system. The layout process will introduce more power.

| Implementation | Area $[\mu m^2]$ | Cycle Time $[ns]$ | Leakage $[nW]$ | Power $[\mu W]$ | Energy $[fJ]$ |
|----------------|-----------------|-----------------|--------------|----------------|-------------|
| Synchronous    | 87.8            | 0.35            | 3.08         | 4.58           | 1.60        |
| Bundled-data$^4$| 86.0            | 0.41            | 2.89         | 5.19           | 2.13        |
| QDI            | 123             | 3.35            | 3.42         | 1.58           | 5.29        |

$^4$Averaged over the array.
and latency into the synchronous and BD designs due to their clock trees, which the QDI design will not suffer from.

VII. CONCLUSION

Our Petri net visualization of the TM architecture enables flexible hardware implementations by encapsulating both concurrency and serialization. By decoupling the TA storage elements from the clauses, e.g. in a standalone array, the TM could be serialized further by reusing clause and sum hardware across multiple cycles, trading off throughput for reduced logic area (and leakage power).

Early propagation enabled by the rcd scheme used in the DR circuits can be leveraged to trigger fine-grained power gating in the system to further reduce energy consumption.

Distributed generation of probabilistic choices maximizes concurrency and decreases energy overheads compared to a centralized approach. A simple PRBG implementation is sufficient and most suitable for our applications. Features of a clock source undesirable in synchronous circuits (jitter, etc.) can be leveraged for stochasticity. Further study of PRBG properties and their effects on TM learning are a subject for future work.

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