A Near-Sensor Processing Accelerator for Approximate Local Binary Pattern Networks

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Abstract—In this work, a high-speed and energy-efficient comparator-based Near-Sensor Local Binary Pattern accelerator architecture (NS-LBP) is proposed to execute a novel local binary pattern deep neural network. First, inspired by recent LBP networks, we design an approximate, hardware-oriented, and multiply-accumulate (MAC)-free network named Ap-LBP for efficient feature extraction, further reducing the computation complexity. Then, we develop NS-LBP as a processing-in-SRAM unit and a parallel in-memory LBP algorithm to process images near the sensor in a cache, remarkably reducing the power consumption of data transmission to an off-chip processor. Our circuit-to-application co-simulation results on MNIST and SVHN datasets demonstrate minor accuracy degradation compared to baseline CNN and LBP-network models, and NS-LBP achieves 1.25 GHz and an energy-efficiency of 37.4 TOPS/W. NS-LBP reduces energy consumption by 2.2× and execution time by a factor of 4× compared to the best recent LBP-based networks.

Index Terms—Processing-in-memory, accelerator, near-sensor processing, SRAM.

I. INTRODUCTION

INTERNET of things’ (IoT) nodes consist of sensory systems, which enable massive data collection from the environment and people to process with on-/off-chip processors (10¹⁸ bytes/s or flops). In most cases, large portions of the captured sensory data are redundant and unstructured. Data conversion and transmission of large raw data to a back-end processor imposes high energy consumption, high latency, and low-speed feature extraction on the edge [1]. To overcome these issues, computing architectures will need to shift from a cloud-centric approach to a thing-centric (data-centric) approach, where the IoT node processes the sensed data. This paves the way for a new smart sensor processing architecture [2], [3], in which the pixel’s digital output is accelerated near the sensor leveraging an on-chip processor. Unless a Processing-in-Memory (PIM) mechanism is exploited [4], [5], [6] in this method, the von-Neumann computing model with separate memory and processing blocks connecting via buses imposes long memory access latency, limited memory bandwidth, and energy-hungry data transfer restricting the edge device’s efficiency and working hours [1]. The main idea of PIM is to incorporate logic computation within memory units to process data internally.

From the computation perspective, numerous artificial intelligence applications require intensive multiply-accumulate (MAC) operations, which contribute to over 90% of various deep Convolutional Neural Networks (CNN) operations [5], [7]. Various processing-in-SRAM platforms have been developed in recent literature [5], [8], [9], [10]. Compute cache [8] supports simple bit-parallel operations (logical and copy) that do not require interaction between bit-lines. Neural Cache [5] presents an 8 T transposable SRAM bit-cell and supports bit-serial in-cache MAC operation. Nevertheless, this design imposes a very slow clock frequency and a large cell and Sense Amplifier (SA) area overhead. In [11], a new approach to improve the performance of the Neural Cache has been presented based on 6 T SRAM, enabling faster multiplication and addition with a large SA overhead. While the presented designs show acceptable performance over various image datasets by reducing the number of operations, i.e., MACs, using shallower models, quantization, pruning, etc., they are essentially developed to execute the existing CNN algorithms that lead to a gap between meets and needs. We believe such a discrepancy can be avoided by developing an intrinsically-low computation network and an efficient PIM platform on the sensor side. Regarding the model reduction of CNNs, Local Binary Pattern (LBP)-based implementations have attained worldwide attention for edge devices, resulting in a similar output inference accuracy [12], [13], [14]. More interestingly, the amount of convolution operations is drastically reduced owing to the sparsity of kernels and conversion to simpler operations such as addition/subtraction [12] and comparison [15].

In this work, inspired by recent LBP networks, (1) we first develop a novel approximate, hardware-oriented, and MAC-free neural network named Ap-LBP in Section III to reduce computation complexity and memory access by disregarding the least significant pixels to perform efficient feature extraction. The Ap-LBP is leveraged on the sensor side to simplify LBP layers before even mapping the data into a near-sensor memory; (2) NS-LBP is designed as a comparator-based processing-in-SRAM...
architecture, in conjunction with the LBP parallel in-memory algorithm in Section IV, which remarkably reduce the power consumption as well as the latency of data transmission to a back-end processor; (3) In Section V, we propose a correlated data partitioning and hardware mapping methodology to process the network locally; and (4) We extensively evaluate NS-LBP performance, energy efficiency, and inference accuracy trade-off compared to recent designs with a bottom-up evaluation framework in Section VI.

II. BACKGROUND & MOTIVATION

A. Near-Sensor & In-Sensor Processing

Systematic integration of computing and sensor arrays has been widely studied to eliminate off-chip data transmission and reduce Analog-to-Digital Converters (ADC) bandwidth by combining CMOS image sensor and processors in one chip as known as Processing-Near-Sensor (PNS) [2], [3], [16], [17], [18], or even integrating pixels and computation unit so-called Processing-In-Sensor (PIS) [19], [20], [21], [22], [23], [24], [25]. However, since enhancing the throughput and increasing the computation load on the resource-limited IoT devices is followed by a growth in the temperature and power consumption as well as noise that lead to accuracy degradation [19], [26], the computational capabilities of PNS/PIS platforms have been limited to less complex applications [1], [27]. This includes particular feature extraction tasks, e.g., Haar-like image filtering [27] and blurring [3].

Various powerful processing-in-SRAM (in-cache computing) accelerators have been developed in recent literature that can be employed as a PNS unit [5], [8], [9], [10], [11], [28], [29], [30], [31]. XNOR-SRAM [10] accelerates ternary-XNOR- and-accumulate operations in binary/ternary Deep Neural Networks (DNNs) without row-by-row data access. CS3RAM [9] leverages capacitive-coupling computing to perform XNOR- and-accumulate operations for binary DNNs. However, both XNOR-SRAM and CS3RAM impose huge overhead over the traditional SRAM array by directly modifying the bit-cells. In [11], a new approach to improve the performance of the Neural Cache has been presented based on 6 T SRAM, enabling faster multiplication and addition with a large SA overhead. In the PIS domain, a CMOS image sensor with dual-mode delta-sigma ADCs is designed in [32] to process 1st-convolutional layer of Binarized-Weight Neural Networks (BWNNs). RedEye [33] executes the convolution operation using charge-sharing tunable capacitors. This design reduces energy consumption compared to a CPU/GPU by sacrificing accuracy. However, to achieve high-accuracy computation, the required energy per frame increases dramatically by 100×. The presented in-SRAM computing macro in [34] has been fabricated in 28 nm process technology and works based on approximate arithmetic hardware that negatively affects CNN accuracy (25.2% on CIFAR-10). To improve the accuracy, the authors use approximation-aware training and a new number format called multi-bit XNOR. Macsen [19] processes the 1st-convolutional layer of BWNNs with the correlated double sampling procedure achieving 1000fps speed in computation mode. However, it suffers from humongous area-overhead and power consumption.

There are three main bottlenecks in IoT imaging systems that this paper aims to solve: (1) The data access and movement consume most of the power (> 90%) [19], [28] in conventional image sensors; (2) the computation imposes a large area-overhead and power consumption in more recent PNS/PIS units and requires extra memory for intermediate data storage; and (3) the system is hardwired so their performance is intrinsically limited to one specific type of algorithm or application domain, which means that such accelerators cannot keep pace with rapidly evolving software algorithms.

B. LBP-Based Networks

An LBP kernel is a computationally efficient feature descriptor that scans through the entire image like that of a convolutional layer in a CNN. The LBP descriptor is formed by comparing the intensity of surrounding pixels serially with the central pixel, referred to as Pivot, in the selected image patch. Neighbors with higher (lower) intensities are assigned with a binary value of ’1’(’0’) and finally, the bit stream is sequentially read and mapped to a decimal number as the feature value assigned to the central pixel, as shown in Fig. 1(a). The LBP encoding operation of central pixel \( C(x_n, y_n) \) and its reformulated expression can be mathematically described as \( LBP(C) = \sum_{i_n=0}^{d-2} cmp(i_n, i_c) \times 2^n \) [12], where \( d \) is the dimension of the LBP, \( i_n \) and \( i_c \) represent the intensity of \( n^{th} \) neighboring- and central-pixel, respectively; thus, \( cmp(i_n, i_c) = 1 \) when \( i_n \geq i_c \), otherwise outputs 0. Simulating LBP is accomplished using a ReLU layer and the difference between pixel values.

The Local Binary Pattern Network (LBPNet) [14] and Local Binary Convolutional Neural Network (LBCNN) [12] are two recent LBP networks where the convolutions are approximated by local binary additions/subtractions and local binary comparisons, respectively. It should be noted that LBPNet and LBCNN are quite different, despite their similarity in their names, as illustrated in Fig. 2. In the LBCNN, batch norm layers are still heavily utilized, which are completed in floating-point numbers for the linear transform. Moreover, since the size and computation of 2D batch norm layers are linear in the size of the feature maps, model complexity increases dramatically. Therefore, the use of LBCNNs for resource-constrained edge devices, such as sensors, is still challenging and impractical. LBPNetworks, on the other hand, learn directly about the sparse and discrete LBP kernels, which are typically as small as a few KBytes. By using
LBPNet, the computation of dot products and sliding windows for convolution can be avoided. Rather, the input is sampled, compared, and then the results of the comparisons are stored in determined locations. A local binary comparison and random projection are used instead of conventional convolutions. An output channel is selected from intermediate channels using the random projection layer as a dimension-reducing process. Therefore, in LBPNet, only trained patterns of sampling locations are held, and no MAC operations (convolution-free) are performed, making it a hardware-friendly and suitable model for edge computing.

III. AP-LBP NETWORK

The Ap-LBP network is trained similarly to the LBPNet, which learns a set of local binary patterns. The Ap-LBP structure, visualized in Fig. 1(b), consists of multiple LBP layers followed by an average pooling, two Multi-Layer Perceptron blocks (MLP), and one batch normalization layer. A standard convolutional layer is replaced with a layer using LBPs, which means neither multiplication nor addition is required, and MAC operations are performed via memory access and comparison. An LBP layer, including an LBP Block and a Joint operation, is leveraged to extract feature maps. Each LBP block consists of an LBP Encoding step that can be readily implemented by a comparator\(^1\) to generate new feature maps connected to an approximate mapping and shifted-ReLU blocks to increase nonlinearity. The output of the LBP blocks is cascaded with the input feature maps (ifmaps) using joint blocks. Fig. 3 illustrates a portion of the LBP block’s operation. In the Ap-LBP, the size of the output feature maps (ofmaps) remains identical to the size of the ifmaps. To do so, the zero-padding approach might be utilized and the degree of zero insertions is calculated by

\[
\text{pad} = \left\lfloor s \times (\text{out} - 1) - \text{in} + f \right\rfloor / 2,
\]

where \(s\) is the stride window’s size, \(f\) is the size of the LBP kernel. This expression works for square matrices. For example, as shown in Fig. 3(a) with \(s=1, in=5\) and \(f=3\), to produce an ofmap with \(\text{out}=5\), zero-padding approach with a degree of one should be utilized.

The learned sets of LBPs from the training step are used in the encoding part to denote the sampling points in ifmaps’ positions that are to be compared with a pivot. After the training phase, pre-defined locations in encoding matrices and bit arrays are determined and remain fixed during the inference phase, e.g., LBP

\[\begin{align*}
\text{OP}_{\text{LBPNet}} &= \left[ \left\lfloor e \times ch + m \right\rfloor \right] + \left[ (e - 1) \times ch \right] \\
&\quad + \left[ (e - 1) \times ch + m \right] \\
&\quad \#\text{read} \quad \#\text{comparison} \quad \#\text{write}
\end{align*}\]

\(^1\)In the backward propagation, binary comparisons are replaced by a modified hyperbolic tangent (tanh) function and shifted to become differentiable.

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Fig. 4. Energy consumption versus accuracy regarding the number of approximated bits on MNIST dataset.

TABLE I

| Network | Computational cost | Memory cost |
|---------|--------------------|-------------|
| CNN     | p·q·ch·r·s          | p·q·r·s     |
| Ap-LBP  | ch·p·q·(e·apx)      | p·q·(e·apx) |
|         | (m·apx)             | (m·apx)     |
| Ap-LBP  | 0                   | r·s         |
|         | (e·apx)             | p·q·r·s     |

\[ OP_{Ap-LBP} = \begin{cases} 
(e - apx) \times ch + m - apx & \#read \\
(e - apx - 1) \times ch & \#comparison \\
(e - apx - 1) \times ch + m - apx & \#write 
\end{cases} \]

where \( e \) is the number of LBP kernels’ elements (number of samplings), \( ch \) is the number of channels, \( m \) is the number of mapping tables’ elements, and \( apx \) is the number of approximated bits. Increasing \( apx \) results in higher speed and energy efficiency on the cost of accuracy degradation. Fig. 4 illustrates the accuracy results for Ap-LBP on MNIST with respect to the number of approximated bits and energy consumption of the LBP layers. This figure shows trade-offs between energy consumption and accuracy with respect to the number of bits in our design. The results are achieved based on the framework setup that will be introduced in Section VI-A. The left axis (blue) contains hardware implementation results for the Ap-LBP processing of the MNIST dataset and the right axis (red) is achieved by our software-layer analysis based on the Pytorch model. As can be seen, the optimal condition occurs when 2 of 4 mapping tables’ bits are approximated, which leads to relatively high energy savings (42%) despite a small reduction in accuracy (1.3%). In addition, the computational and memory costs for the convolution layer of both conventional CNNs and Ap-LBP networks are presented in Table I. As shown, in the convolutional layer, the dimension of filters (ifmaps) is 4-D, \( K \times ch \times r \times s \) \((M \times ch \times h \times w)\), where \( K \) and \( M \) are the number of filters and ifmap, respectively, \( ch \) is the number of channels, \( r \times s \) is the spatial dimension of filters and \( h \times w \) is the dimension of 2-D ifmaps. So the generated ofmaps’ dimensions are \( M \times K \times p \times q \), where \( p \times q \) is ofmap’s 2-D dimensions. To simplify matters, a single kernel \((K = 1)\) and a single ifmap \((M = 1)\) are considered. Since the difference between the number of samplings in an LBP pattern, \( e \), and the number of approximated bits, \( apx \), is relatively smaller than the spatial dimensions of kernels, that Ap-LBP, with MAC-free LBP layers, significantly reduces the hardware cost, both computation, and memory.

IV. PROPOSED NS-LBP

A. Architecture

We propose NS-LBP as a cache-based near-sensor architecture to accelerate the Ap-LBP network with a parallel in-memory LBP algorithm. NS-LBP is mainly developed to process Ap-LBP’s key operations. LBP layers are accelerated through an efficient comparison implemented with data-parallel X(N)OR bit-wise operations and the MLP layers are executed near-sensor through data-parallel AND-bit count operations as explained below. However, NS-LBP can be used to accelerate 2- and 3-input bulk bit-wise operations in various applications such as data encryption, graph processing, etc. NS-LBP’s geometry of a single 2.5 MB cache connected to an image sensor is shown in Fig. 5(a). A rolling-shutter CMOS image sensor is composed of \( m \times n \) photodiode-based pixels, which utilize the Correlated Double Sampling (CDS) mechanism [19]. CDS measures the photodiode’s voltage drop before and after an image light exposure and utilizes an ADC to convert it to a digital value. However, a significant amount of power is consumed by ADC conversion of raw images and high-throughput transmission [1], [3], [19].

To reduce the power consumption imposed by ADC and data transmission to the memory, we first modify the sensor controller and peripheral circuitry so that Ap-LBP’s approximation can be applied on the sensor side by simply avoiding pixel conversion for less significant bits. This is explained in Section III. By using this mechanism, the NS-LBP is assured of receiving only compute pixels and pivots. Cache slices within NS-LBPs are designed to have 80 memory banks, of 32 KB each organized in 20 distinct ways. Each bank contains two 16 KB memory matrices-mat (see Fig. 5(a)). The centralized control unit (Ctrl) manages the internal memory data transfer, intra-bank computation, and a digital processing unit (DPU) common to all memory banks. The main computational cores of NS-LBP are 8 KB computational sub-arrays as depicted in Fig. 5(b)–(c).

According to our observations of existing sub-array-level processing-in-SRAM platforms, they face various challenges, such as multi-cycle in-memory operations, word-line underdrives, high-latency, read disturbances, etc. [11], [29], [31], when it comes to comparison and addition operations required by the proposed Ap-LBP. The proposed NS-LBP’s sub-array (Fig. 5(c)) leverages the voltage discharging profile of the read-write-decoupled 8 T SRAM cell (Fig. 5(d)) on Read-BL (RBL) used for the standard read operation and elevates it to implement Boolean logic between operands located in different memory rows in a single SRAM read cycle. In this way, we develop a processing-in-SRAM sub-array through a three-row activation mechanism by modifying the memory row decoder, SA, and Ctrl. It is important to note that the key idea comes from the observation that certain discharge rates on the precharged RBL...
can be expected based on selected memory bits. For instance, by activating three memory rows via Read Word-Lines (RWL), e.g., RWL0-RWL2 shown in Fig. 5(c), if $S_{0,0}, S_{1,0}$, and $S_{2,0}$ memory cells hold binary “1”, then the read access transistors (T8 in Fig. 5(d)) remain OFF, and the RBL precharged voltage doesn’t degrade. However, if all cells hold binary “0”, the RBL voltage is rapidly discharged through T8s. Accordingly, we propose a new reconfigurable SA as shown in Fig. 5(e) consisting of three sub-SAs, each dedicated to computing a particular function.

With a proper selection of a reference voltage ($R_1 < R_2 < R_3$), each sub-SA performs a neat voltage comparison with RBL voltage and generates (N)OR3, (MAJ)MIN, and (N)AND3 logic functions simultaneously. The XOR-based comparison is then achieved through an observation in which the three input majority function of OR3, MIN, and AND3 is able to generate XOR3 logic. The Boolean logic of in-memory XOR3 can be given as $XOR3/(Sum) = MAJ((A + B + C) + (AB + AC + BC) + (ABC))$. This unit is implemented with a low overhead capacitive voltage divider as shown in Fig. 5(g).

The implementation of 2-input bit-wise operations is straightforward by initializing one row to “0”/“1”. We choose an 8 T SRAM cell as a fast and compact design considering that the proposed in-memory computing mechanism operates based on BL discharging. Nevertheless, the mechanism presented here can be applied to various read-write decouple SRAM designs.

From a programmer’s perspective, NS-LBP is interfaced as a bus-facing accelerator that can be connected directly to the memory bus or through PCI-Express lanes rather than a memory unit. Therefore, a virtual machine and ISA for general-purpose parallel thread execution need to be defined. We designed instruction sets that could optimally leverage highly parallel NS-LBP’s operations discussed and developed a compilation framework on top of that. Accordingly, the programs will be translated at install time to the NS-LBP’s hardware ISA tabulated in Table II.

### B. In-Memory LBP Algorithm

By converting a conventional software-based sequential comparison operation into a parallel bit-wise XOR operation, we propose an NS-LBP hardware-oriented LBP algorithm that fully utilizes the sub-array parallelism of the NS-LBP. A key objective in developing such an algorithm is to enable a parallel bit-position-aware comparison between pivot (C) and surrounding pixels (P) and generate an LBP bit-stream in fewer cycles, eliminating unnecessary power-hungry bulk bit-wise operations.

For every LBP kernel, starting from the Most Significant Bit (MSB), Algorithm 1 issues the NS-LBP’s comparison command (NS-LBP\_XOR) in a loop to pivot and pixels in parallel and update the Result\_array (line-7). The result of $i^{th}$ bit comparison ($C_i \oplus P_{j,i}$) is leveraged as a determining factor for NS-LBP to take the next step. As indicated in the algorithm, when the XOR result is “1”, i.e., two unequal bits are identified (line-8), $C_i$ is read (NS-LBP\_Mem). Now, if $C_i$ equals “0”, the corresponding LBP\_array position is set by “1”, indicating $C_i < P_{j,i}$ and vice versa (lines-9-12). However, if equality is noticed, the next less significant bit in pixels and pivot is selected for comparison.
and this process stops when the XOR result is “1” (inequality). Such a parallel comparison operation could rapidly detect the mismatch between all pixels and pivot from MSB to LSB. Our algorithm has a constant search time that is determined by the bit length of numbers. As shown, NS-LBP_XOR is iteratively used in a nested “for” loop in the algorithm, and the NS-LBP architecture is mainly designed to accelerate this operation.

V. CORRELATED HARDWARE MAPPING

A. LBP Layer

To maximize Ap-LBP computation throughput and fully leverage NS-LBP’s parallelism, we propose partitioning data as shown in Fig. 6. Given an LBP layer, the accessed memory region of pixels and pivots could be easily predicted, and the LBP bit-stream could be locally computed if we could store such correlated regions into the same memory sub-array. Thus, we propose a novel, correlated data partitioning, and mapping methodology as shown in Fig. 6(a) to locally store correlated regions of pixel and pivot vectors in the same memory sub-array and enable entirely local computation (i.e., NS-LBP_XOR and NS-LBP_Mem completely within the same sub-array without inter-bank/chip communication). The NS-LBP’s compute sub-array (256 rows x 256 columns) is split into five key regions, i.e., Pixel-P (64 rows), Pivot-C (64 rows), Reserved (64 rows), Weight-W (32 rows), and Input-I (32 rows). We use P-, C-, and Resv. regions to process the LBP layer.

The selected input pixels in Ap-LBP are initially transposed in a 1D-Array (C[]), LBP _ array, and all-zero. Fig. 6(b) gives an intuitive example of LBP-layer computation with the in-memory LBP algorithm, where four pixels (P3 to P7) are selected. After data mapping, NS-LBP’s Ctrl activates three RWLs simultaneously, corresponding to pixels’ and pivot’s MSB and all-zero row. The NS-LBP sub-array then performs the parallel XOR2 operation in a single cycle based on the mechanism discussed in Section IV, and the result “1001” is stored in the Result_array row (step 3). Now, the Ctrl readily recognizes the potential mismatch in C7 = 0 value. As there are two matches (P2, C7, and P1, C7), the Ctrl selects the next MSBs in pixels and pivot to find the next potential mismatch. The final LBP_array value (“1001”) is returned in step 4 for the next step. It is worth pointing out that other configurations of SRAM-based cache memory can be readily adopted and used. The only constraint is to assure the converted sensor data can be properly stored to support the NS-LBP correlated data partitioning and mapping scheme.

B. MLP Layer

Besides the LBP layer, there are MLP layers in Ap-LBP as shown in Fig. 1(b) that can be accelerated close to the sensor without sending the activated LBP feature maps to an off-chip processor. Note that MLP can be equivalently implemented by convolution operations using 1 x 1 kernels [35]. W- and I-regions in every NS-LBP sub-array (Fig. 6(a)) are dedicated to performing such an operation locally. Fig. 7 gives an overview of the MLP bit-wise acceleration steps. In the first step, the processed input activation from NS-LBP’s LBP layers is quantized by DPU and mapped into I-region, where the MLP layer weights are located. In the second step, parallel computational sub-arrays perform bulk bit-wise operations between tensors and generate the output. Then, the output is activated by DPU’s Activation unit and saved back into the Resv. region. From a computation

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perspective, every MLP layer can be equivalently implemented by exploiting NS-LBP_AND, bitcount, and bitshift as parallelizable operations [35].

Assume \( I \) is a sequence of \( M \)-bit input integers, e.g., 3-bit in Fig. 7 located in ifmap covered by a sliding kernel of \( W \), such that \( I_i \in I \) is an \( M \)-bit vector representing a fixed-point integer. We index the bits of each \( I_i \) element from LSB to MSB, where \( m = 0 \) and \( m = M - 1 \) are corresponding to LSB and MSB, respectively. Accordingly, we represent a second sequence denoted as \( C_m(I) \) including the combination of \( m \)-th bit of all \( I_i \) elements (shown by colored elliptic). For instance, \( C_0(I) \) vector consists of LSBs of all \( I_i \) elements “0110”. Considering \( W \) as a sequence of \( N \)-bit weight integers (3-bit, herein) located in a sliding kernel with an index of \( n = 0, N - 1 \). The second sequence can be similarly generated as \( C_n(W) \). Considering the set of all \( M \)-th value sequences, the \( I \) can be represented like \( I = \sum_{m=0}^{M-1} 2^m c_m(I) \). Likewise, \( W \) is represented like \( W = \sum_{n=0}^{N-1} 2^n c_n(W) \). Thus, the convolution between \( I \) and \( W \) is defined as \( \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} 2^{m+n} \text{bitcount}(\text{and}(C_m(W), C_n(I))) \) [35]. In the data mapping step of Fig. 7, \( C_2(W) \cdot C_0(I) \) and \( C_2(I) \cdot C_0(I) \) are consequently mapped into an NS-LBP’s sub-array. Now, a parallel bit-wise AND operation (NS-LBP_AND) of \( C_n(W) \) and \( C_m(I) \) is performed. The results will be then processed using a bit-counter counting the number of “1”s in each vector and then a shifter unit, e.g., here left-shifted by 3-bit (\( \times 2^{2+1} \)) to “1000”. Eventually, the shifter unit’s outputs are added up to produce ofmaps for every layer.

VI. EVALUATION RESULTS

A. Setup

To estimate the performance of NS-LBP along with Ap-LBP, a bottom-up evaluation framework is developed as shown in Fig. 8. At the circuit level, NS-LBP is fully implemented with TSMC 65nm-GP with a supply voltage of 0.9V-1.1 V in Cadence, and the post-layout results are reported. However, NS-LBP is not taped out. The NS-LBP platform can be readily implemented in lower technology nodes to achieve lower power consumption and higher TOPS/W. At the architecture level, we fully implemented NS-LBP’s ISA using gem5 [36]. The compiler is then developed on top of the PIMSim’s full-system mode [37] taking array parameters (latency and energy consumption for individual operations) and the binary of the application as input and exporting the memory statistics and performance evaluation results. The results are then fed into a behavioral NS-LBP’s in-house optimizer tool, also taking the circuit-level data to model the timing, energy, and area. This tool will offer the same flexibility in memory configuration regarding bank/mat/sub-array organization and peripheral circuit design as Cacti [38] while supporting SRAM-level configurations. The architecture simulator can alter the configuration files with different array organizations. At the application level, we trained a PyTorch implementation of Ap-LBP inspired by LBPNet, with the difference that our design approximates pre-trained LBP kernel parameters. The Ap-LBP’s statistics are then leveraged in the behavioral NS-LBP model to compute the latency and energy of the whole system. Besides, to model the data loading time for all layers, we followed the approach in [5] by developing a micro-benchmark that sequentially accesses the sets in a way that requires data loading. In fact, the Ap-LBP network is the result of two sets of experiments. First, a software (PyTorch) implementation was accomplished to analyze the final network accuracy with various approximation methods including the PAC method. This experiment clearly showed us the expected accuracy degradation. Second, the Ap-LBP is fully implemented in our digital in-memory accelerator to achieve the expected accuracy.

B. Functionality Analysis

Fig. 9 shows the post-layout transient simulation results of an NS-LBP sub-array. To verify the functionality of all possible input combinations (“000”, “001”, “011”, and “111”), three WWLs are activated consecutively (first waveform) and by assigning proper voltages to WBL and WBLB, the SRAM cells are loaded with the operands. In the computation mode, we simultaneously activate the corresponding RWL of three cells to discharge RBL from the precharged voltage (1.1 V) w.r.t. the memory value. To compromise three-row activation stability by lowering the RWL voltage that leads to read latency, we reduced the RWL voltage to 790 mV to achieve the industry standard 6-sigma margin. For the evaluation, by activating the Sense
Amplifier Enable (SAE) signal, a voltage comparison between the RBL voltage and references is made. As shown in Fig. 9, $V_{R1}=360 \text{ mV}$, $V_{R2}=550 \text{ mV}$, and $V_{R3}=850 \text{ mV}$ are set as the reference voltages.

In the case of “000”, T8s (see Fig. 5(d)) of all three cells are ON pulling down the RBL voltage from 1.1 V to 280 mV. This can be easily detected by SA generating “0” as the XOR3 output ($V_{R3} > V_{R2} > V_{R1} > 280 \text{ mV}$). The total processing time from enabling the SA to get the result is ~400 ps in the same range given by the standard foundry memory compiler. In the case of “001”, T8s of two out of three cells are ON pulling down the RBL voltage from 1.1 V to 495 mV. This can be easily detected by SA generating “0” as the XOR3 output ($V_{R2} > V_{R3} > V_{R1} > 495 \text{ mV}$). With “011”, T8 of only one cell is ON pulling down the RBL voltage from 1.1 V to 735 mV generating “0” as the XOR3 output ($V_{R3} > 735 \text{ mV} > V_{R2} > V_{R1}$). Eventually, with “111” as inputs, all T8s are OFF taking the RBL voltage at 950 mV outputting “1” (950 mV $> V_{R3} > V_{R2} > V_{R1}$).

For the SA reference voltage ($V_{R}$) analysis, the RBL sense margins are first tested through post-layout Monte Carlo simulations in Cadence Spectre, as shown in Fig. 10, where the sensing margin is reported considering both process (inter-die) and mismatch variations (intra-die) for core VDD (1.1 V) at 1.25 GHz. To conduct the $V_{R}$ variation analysis, we tested all 256 bit-lines within each NS-LBP’s sub-array, 200 times, for all possible bit value combinations in memory. It is found that at lower voltages the maximum operating frequency is limited by the reduction of $V_{R}$ ranges. A higher VDD also yields a larger sensing margin. As we observe there is ~92 mV margin (the smallest voltage margin observed between “111” and “011” cases) between every two combinations bringing high in-memory computing reliability for the NS-LBP design.

### C. Energy Consumption & Performance

Fig. 11(a) shows the energy consumption breakdown of NS-LBP running Ap-LBP and LBPNet compared to a baseline 8-bit quantized CNN and LBCNN implemented by [29] running SVHN dataset. We meticulously report the energy consumed by MAC and CMP operations in various networks. We observe that (i) the NS-LBP running Ap-LBP demonstrates up to $2.2 \times$ and $5.2 \times$ higher energy efficiency compared to the LBPNet and CNN counterparts, respectively. Converting power-hungry MAC to bit-wise comparison operation in an approximate fashion has yielded such a striking improvement; (ii) leveraging Ap-LBP can bring up to $4 \times$ energy-efficiency when compared with the LBCNN. It is worth mentioning that LBCNN still relies on power-hungry MAC operations. Fig. 11(b) compares inference delay per input image in four under-test designs. We observe that the NS-LBP leveraging Ap-LBP achieves $4 \times$ and $2.3 \times$ speed-up compared to LBPNet and LBCNN designs, respectively. Besides, it can be seen that $6.2 \times$ speed-up is achieved when compared with the CNN baseline. Fig. 11(c) further clarifies that Ap-LBP doesn’t remarkably reduce the memory storage relative to LBP-Net; however, it requires $3.4 \times$ smaller memory to store the parameters than LBCNN.

### D. Comparison

Since several processing-in-SRAM platforms have been developed to accelerate various deep neural networks in literature, performing a fair comparison is a difficult task. Nevertheless, Table III lists seven recent designs for a comparison. We compared our digital approximate LBP accelerator with conventional analog/digital MAC-based neural network accelerators supporting bit-truncation (quantization) as a well-known method in neural network approximation. As can be seen, various designs are implemented with different bit-cell structures and SA designs. Here we report our main observations. (1) The NS-LBP and the designs in [29], [30] are the only in-SRAM platforms that can support XOR-based LBP computation. We observe that NS-LBP...
shows a fairly smaller SA area overhead (3.4 ×) compared to these designs to support in-memory computation. (2) It can be seen that the designs presented in [11], [30] show the highest frequency at 1 V, where NS-LBP stands as the third-fastest design. (3) The NS-LBP achieves 37.4 TOPS/W standing as the fourth most efficient design compared to all counterparts, whereas the design in [9] with 671 TOPS/W stands as the most efficient design. To assess the impact of the technology node on the overall performance, we implemented the NS-LBP with 22 nm Predictive Technology Model (PTM) library [40] and extracted the pre-layout results. Based on our observations, a higher performance (87.3 TOPS/W) and lower power consumption can be achieved.

Overall, NS-LBP offers 1) A dual-mode computational SRAM platform with no sacrifice of memory capacity that directly process data within the memory array to eliminate off-chip data communication; 2) A complete set of Boolean operations (both 2- and 3-input), majority, and full adder in only one single memory cycle, demonstrating one of the most efficient PNS systems to date; 3) Highly parallel low-bit-width convolution operation; and 4) Light modification of existing memory cell to achieve low in-memory logic area overhead.

E. Accuracy

To perform a fair comparison between Ap-LBP and five other neural network models, CNN (as a baseline) [41], Binarized Neural Network (BNN) [42], BinaryConnect [43], LBCCNN [12], and LBPNet [14], with identical hyper-parameters such as number of basic blocks, number of hidden neurons, etc. are selected. We conduct experiments on five datasets, i.e., MNIST, FashionMNIST, SVHN, CIFAR-10, and CIFAR-100 to evaluate the performance of both algorithm accuracy and hardware implementation. PyTorch implementation of Ap-LBP inspired by LBPNnet, with the difference that our design approximates pre-trained LBP kernel parameters, is developed. The number of basic blocks for MNIST and SVHN is set to 5 (3 LBP layers and 2 FC layers) and 10 (8 LBP layers and 2 FC layers) layers, respectively, with 512 hidden neurons. As for CIFAR-10 and CIFAR-100 datasets, the number of basic blocks is respectively set to 7 (5 LBP layers and 2 FC layers) and 17 (14 LBP layers and 3 FC layers) layers, respectively, with 512 hidden neurons. The simulation is performed with two GPUs (Nvidia RTX 3090) configurations. The comparison of classification accuracy is summarized in Table IV.

This paper first presented an approximate and multiply–accumulate-free deep neural network model named Ap-LBP for efficient feature extraction. We then developed a comparator-based near-sensor processing local binary pattern accelerator (NS-LBP) and a parallel in-memory LBP algorithm to process images near the sensor based on the Ap-LBP. The results on MNIST and SVHN datasets demonstrate minor accuracy degradation compared to baseline CNN and LBP-network models, while NS-LBP achieves 1.25-GHz and an energy-efficiency of 37.4 TOPS/W. NS-LBP reduces energy consumption and execution time by a factor of 2.2 × and 4 × compared to a recent LBP-based network.

VII. Conclusion

This paper first presented an approximate and multiply–accumulate-free deep neural network model named Ap-LBP for efficient feature extraction. We then developed a comparator-based near-sensor processing local binary pattern accelerator (NS-LBP) and a parallel in-memory LBP algorithm to process images near the sensor based on the Ap-LBP. The results on MNIST and SVHN datasets demonstrate minor accuracy degradation compared to baseline CNN and LBP-network models, while NS-LBP achieves 1.25-GHz and an energy-efficiency of 37.4 TOPS/W. NS-LBP reduces energy consumption and execution time by a factor of 2.2 × and 4 × compared to a recent LBP-based network.

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