How to report and benchmark emerging field-effect transistors

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The use of organic, oxide and low-dimensional materials in field-effect transistors has now been studied for decades. However, properly reporting and comparing device performance remains challenging due to the interdependency of multiple device parameters. The interdisciplinarity of this research community has also led to a lack of consistent reporting and benchmarking guidelines. Here we propose guidelines for reporting and benchmarking key field-effect transistor parameters and performance metrics. We provide an example of this reporting and benchmarking process using a two-dimensional semiconductor field-effect transistor. Our guidelines should help promote an improved approach for assessing device performance in emerging field-effect transistors, helping the field to progress in a more consistent and meaningful way.

Research into field-effect transistors (FETs) based on emerging nanomaterials—including carbon nanotubes1,2, graphene,3 phosphorene4, silicene5, tellurene6, transition metal dichalcogenides7–9, organic semiconductors10,11 and ultrathin metal oxides12—is thriving. Such studies allow the fundamental properties of the materials to be explored, and may lead to the development of various commercial applications. However, effectively and uniformly assessing the performance of emergent FETs is difficult due to the dependence of performance metrics on unique aspects of the device structure (Fig. 1a)13.

The structural parameters that influence device performance include channel length (L), contact length (Lc), gate insulator thickness (t), permittivity (ε), contact metal types, the thickness of the channel material (t) and the gating scheme (for example, top, bottom, gate-all-around, multi-channel). Performance metrics include on current (I), off current (I), the I/I ratio, contact resistance (R), transconductance (g), subthreshold swing (SS), channel mobilities and drain-induced barrier lowering (DIBL). Although the different studies reported in the literature often include some of these benchmarking figures, they struggle to capture the myriad variables, making comparisons inaccurate or even biased at times. In addition, the emerging device community consists of researchers from disparate disciplines—including electrical engineering, chemistry, materials science and physics—which also makes consistent reporting and benchmarking challenging. In this perspective we examine the challenges involved in assessing the operation and performance of FETs based on emerging materials, and provide guidelines on how to report and benchmark the devices.

Field-effect transistor structure and key parameters

In a FET, the structural parameters determine the electric fields and the eventual device performance (Fig. 1a). The subthreshold, transfer and output characteristics presented in Fig. 1b–d are the most common I–V (current–voltage) curves to capture device performance. Plotting the log of the drain current (I) as a function of gate–source voltage (Vgs) highlights the subthreshold (that is, off state) device behaviour. In contrast, transfer characteristics plot I versus Vgs on a linear scale and emphasize the device behaviour after Vgs exceeds the threshold voltage (Vth), where the device is in the on state. Ideally, the gate leakage current (Ig) versus Vgs should be plotted on the subthreshold plot as well.

The I–V sweeps in Fig. 1bc should be conducted at both ‘small’ and ‘high’ drain–source voltage (Vds) values to characterize device operation in both the linear and saturation regimes. We note that the small Vgs value should be sufficiently small to ensure linear-regime operation, but greater than ~2kBT (where kB is the Boltzmann constant and T is the absolute temperature, that is, ~50 mV at room temperature) to ensure that the subthreshold behaviour (here, in particular, DIBL, dVth/dVgs) is not misinterpreted due to thermal injection of carriers from the drain. These curves enable easy extraction of DIBL to demonstrate how Vth impacts Vgs. The transfer characteristics should be acquired with forwards and backwards sweeps, checking for the presence of any hysteresis due to charge trapping14. When comparing the hysteresis from different devices, precise measurement conditions such as sweep rates, hold times and maximum bias voltages should be listed, as these parameters influence hysteresis. If hysteresis exists, it
In the output characteristics (Fig. 1d), three main operation regimes are highlighted. The linear regime is characterized by the linear increase of $I_{DS}$ with both $V_{GS}$ and $V_{DS}$. After $V_{DS}$ surpasses the overdrive voltage ($V_{DD} = V_{GS} - V_{TH}$ for n-channel FETs), $I_{DS}$ starts to saturate to $I_{SAT}$, which could (based on the classical FET model) increase quadratically with $V_{GS}$ in the pinch-off region and linearly with $V_{DS}$ in the velocity saturation regime. Note that the linear regime may present as nonlinear (often exponential) in the event of poor carrier injection at the contacts, such as from large Schottky barriers.

Multiple performance parameters can be extracted from the $I-V$ curves in Fig. 1b–d. The most important performance metrics are the currents, which must be reported normalized by the channel width, $W_{ch}$ (for example, in units of $\mu A/\mu m^2$). For one-dimensional (1D) or quasi-1D devices, it is common to first report the current per carbon nanotube (CNT)/nanowire/nanosheet stack. The current can then be normalized to units of $\mu A/\mu m^2$ by considering the expected channel density and pitch of the channel material (for example, 10 $\mu A$ per CNT with 50 CNTs $\mu m^{-1}$, giving 500 $\mu A/\mu m^{-1}$), because the aerial footprint of the device is a critical aspect of performance. When extracting $I_{on}$ and $I_{off}$ from these $I-V$ curves, in a simplified scenario, $I_{on}$ is the $I_{DS}$ measured at $V_{GS} = 0$ and $V_{DS} = V_{DD}$, whereas $I_{off}$ is the $I_{DS}$ measured at $V_{GS} = V_{DD}$. Here, $V_{DD}$ is the voltage that would be supplied to operate the transistors. (For mainstream silicon technology, $V_{DD}$ dropped to 1 V near 2010 and to 0.7 V in recent years.) For modern technologies, the exact value of $V_{DD}$ depends on the application. For example, if the emergent transistor is used as an access transistor in a dynamic random-access memory (DRAM), then its $V_{DD}$ will be a small value to ensure linear-regime operation in the on state. Reported emergent devices often do not have threshold voltages tuned such that $V_{TH} = 0$ is a sensible off-state; additionally, there is often not a well-defined $V_{DD}$ value due to the wide variety of device structural parameters. We hence suggest extracting the maximum and minimum $I_{DS}$ ($I_{on}$ and $I_{off}$) from a typical subthreshold curve and reporting the $I_{on}/I_{off}$ ratios when $V_{DD}$ is biased in both the linear and saturation regimes. A more detailed description on reporting and benchmarking $I_{on}/I_{off}$ is provided in Supplementary Note 1.

When reporting the $I_{on}$ of a device, it is necessary to note the carrier density $n$ at which the $I_{on}$ is extracted. Ideally, the Hall effect is used to measure the carrier density for the channel material, but for most researchers in the FET community, more accessible approaches are needed that do not require specially designed test structures. In the linear regime, the average carrier density can be estimated as $n \approx C_{in} (V_{GS} - V_{TH})/q$, where $C_{in}$ is the gate insulator capacitance and $q$ is the elementary charge; however, in the saturation regime, the depletion region in the channel complicates the estimation. The carrier density near the source side is the same for both the linear and saturation regimes. For convenience and simplicity, we recommend clearly labelling the carrier density near the source as $n_s = C_{in} V_{GS}/q$ and using this value for both operation regimes. To determine $V_{GS}$, $V_{TH}$ is usually estimated using extrapolation in the linear portion of the transfer curve, as listed in Table 1. Other methods, such as constant-current, Y-function
methods\(^{19,20}\) and four-probe measurements\(^{21}\), can be used to cross-check the linear extraction of \(V_T\) and reduce the variation when estimating \(n_D\). More discussion regarding \(V_T\) extraction is given in Supplementary Note 2.

In addition to \(I_{DSS}, R_S\) is also essential to represent device performance. The transfer length method (TLM) is the most commonly used approach for extracting \(R_S\) along with the sheet resistance, \(R_{\text{sh}}\), of the channel (in units of \(\Omega \square^{-1}\)). The TLM approach requires a series of FETs with different channel lengths and consistent contact and gating configurations. It entails plotting the total resistance of each device versus \(L_{\text{ch}}\) at a given \(n_D\), allowing \(R_S\) to be extracted as the extrapolated y-axis intercept from a linear fit to the data points. Typically, the \(V_{DSS}\) for calculating the total resistance is the small \(V_{DSS}\) used in Fig. 1b to ensure linear-regime operation. The channel lengths in the TLM should range from short (where the total resistance is dominated by \(R_S\)) to long (dominated by channel resistance \(R_{\text{ch}}=R_{\text{sh}}-2R_S\) or \(R_{\text{sh}}L_{\text{ch}}\)) where the actual short and long channel lengths will depend on the relationship between the channel resistance and the contact resistance. A more detailed discussion on extracting \(R_S\) and other considerations using TLM data is provided in Supplementary Note 3.

Another frequently reported parameter is the carrier mobility of the channel material. Among various forms of mobility, the field-effect mobility \(\mu_{FE}=L_{\text{ch}}g_m/(W_{\text{ch}}C_{\text{ox}}V_{DSS})\) is often used. However, \(\mu_{FE}\) can be underestimated\(^{19,20}\) or overestimated\(^{21,24,25}\) relative to the drift mobility of the channel material depending on the details of \(V_{DSS}, V_{GSS}, R_S, L_{\text{sh}}\) and gate capacitance. In particular, gated contact effects can significantly affect mobility extraction. Although different approaches\(^{26,27}\) have been proposed to make \(\mu_{FE}\) less dependent on various factors, such as \(R_S\) and \(L_{\text{sh}}\), none of them is sufficiently general enough to be widely adopted. Conductivity mobility (\(\mu_{\text{con}}\)) has the advantage of strictly reflecting the channel material properties and the quality of the channel–dielectric interface\(^{22,26}\). In a FET, \(\mu_{\text{con}}\) (ref. 22) can be estimated from the sheet resistance of the semiconductor channel and the carrier density, \(n_D\) (Table 1); thus, it does not involve the contact resistance or the device structure. High mobility is often a goal for research FETs; when such reports are made, it is critical to clearly state how the values are determined, and ideally multiple approaches (such as \(\mu_{FE}\) and four-probe measurements\(^{21}\)) are taken to cross-validate the claims. It is worth noting that the usefulness of channel mobility as an indicator of performance in aggressively scaled FETs is debatable, as devices with channel lengths <30nm are going to be strongly limited by contact resistance (including carrier injection efficiency), with minimal dependence on transport in the channel\(^{27,28}\).

The most representative FET parameters are listed in Table 1 as a suggested reporting checklist. Additional parameters are briefly discussed in Supplementary Note 4.

Beyond the parameters in Table 1, showing statistics and variation is strongly encouraged to obtain comprehensive coverage of the device performance. The variation can be shown as error bars, box plots, coefficient of variation or cumulative distribution function (see Supplementary Note 5 for a demonstration). Due to the many non-idealities associated with emerging materials or unconventional device geometries, it is almost unavoidable that there could be considerable uncertainties in many extracted parameters, including \(R_S, n_D\) and mobilities. These parameters are often interdependent. Reducing device variation is a major research theme for the eventual application of emergent FETs. Whatever measurements and specific analysis approaches are taken to determine these

**Table 1 | Checklist of suggested device parameters to report**

| Name | Characteristics | Additional details |
|------|----------------|--------------------|
| Structural parameters | Contact length, \(L_{\text{ch}}\) | Specify contact and gating geometry/materials; include high-resolution electron microscopy evidence when reporting sub-20-nm dimensions (especially for \(L_{\text{ch}}\) and \(L_{\text{sh}}\)) |
| Insulator capacitance, \(C_{\text{ox}}\) | Capacitance-voltage or capacitance-frequency | Measured \(C_{\text{ox}}\) is more accurate than estimating \(e_{\text{ox}}\) especially when a high-k insulator is used |
| Threshold voltage, \(V_{T}\) and hysteresis, \(\Delta V_T\) | Extrapolation in the linear portion of the transfer curve\(^9\) | \(I_{DSS}-V_{GSS}\) should have forwards and backwards sweeps |
| | | Consider \(V_T\) uncertainty due to hysteresis (charge trapping), the dependence of \(V_{GSS}\) and \(I-V\) sweeps (Supplementary Note 2) |
| Drain current in saturation regime, \(I_{\text{sat}}\) | \(I_{\text{sat}}-V_{GSS}\) (saturation regime) | \(I_{\text{sat}}-V_{GSS}\) to the saturation regime |
| | | Specify carrier density where \(I_{\text{sat}}\) is extracted |
| | | Normalized by channel width |
| Contact resistance, \(R_S\) | Transfer length method (TLM)\(^{22}\) (Supplementary Note 3) | Linear regime (small \(V_{GSS}\)) |
| | | Specify carrier density \(n_D\) or plot \(R_{\text{sh}}\) versus \(n_D\) |
| | | TLM should have at least four channels and include at least one each of contact and channel resistance-dominated devices |
| Conductivity mobility, \(\mu_{\text{con}}\) | \(1/\sigma_{\text{con}}\) | \(R_S\) is extracted from the slope of TLM plots or from four-probe measurements\(^{21}\) (units: \(\Omega \square^{-1}\)) |
| | | Carrier density near the source: \(n_D \approx C_{\text{ox}}V_{GSS}/q\) |
| | | Mobility from \(R_{\text{sh}} = (q\sigma_{\text{con}})^{-1}\) |
| | | Plot mobility versus \(n_D\) to show field dependence |
| Transconductance, \(g_m\) | Transfer or output curves \(g_m = \frac{dI}{dV_{\text{GS}}\text{at}}\) certain \(V_{\text{GS}}\) | Specify \(g_m\) (linear) or \(g_m\) (saturation) |
| Subthreshold swing (SS) | Subthreshold curves (inverse slope in mV dec\(^{-1}\) below \(V_T\)) | SS depends on \(C_{\text{ox}}\) and interface trap capacitance \(C_s\) |
| | | Plot SS versus log\(_2\)(\(I_{\text{th}}\)) |
| \(I_{\text{sat}}/I_{\text{sh}}\) | Subthreshold curves at saturation regime, \(V_{\text{GSS}}=V_{GSS}\) (sat) | Report \(I_{\text{sat}}/I_{\text{sh}}\) as an alternative along with the \(n_D\) range |
| | | Plot \(I_{\text{sh}}\) versus \(V_{GSS}\) to show leakage current |
| DIBL | \(\Delta V_T/\Delta V_{DSS}\) from transfer curves | Key for short-channel devices |
parameters, the details should be clearly and explicitly reported, and our recommended approaches are demonstrated herein.

Once an emerging FET has been systematically parameterized, benchmarking tables and plots are extremely useful for comparing devices from different reports. Because the electric fields are the driving forces within FETs, benchmarking performance metrics based on electric fields is natural. However, special care is needed in considering electric fields in devices, because they are spatially non-uniform and depend on many other factors, such as fringing fields and quantum capacitance $C_{\text{q}}$. Thus, the electric fields in nanoscale FETs are more complicated than the simple definition of an applied voltage divided by a physically defined length. For example, it is a reasonable assumption that the channel electric field ($E_{\text{ch}}$) increases linearly from source to drain in the linear region of operation, but $E_{\text{ch}}$ peaks sharply at the drain end of the channel in classical pinch-off (saturation) regime. To account for this, the average $E_{\text{ch}}$ can be approximated as $(V_{\text{DS}} - 2 I_{\text{ds}} R_{t})/L_{\text{ch}}$ in the linear regime, accounting for voltage dropped at the contacts.

The vertical electric field at the source end, $E_{\text{sat}}$, can be estimated as $V_{\text{GS}}/t_{\text{ox}}$, if a planar gate is used. In turn, $E_{\text{gate}}$ and the gate insulator permittivity determine the carrier density in the channel. However, both $E_{\text{sat}}$ and the gate insulator permittivity are rather challenging to measure accurately. One more word of caution is justified: because many low-dimensional materials exhibit a low density of states, $C_{\text{ox}}$ needs to be replaced by $C_{\text{ox}}/t_{\text{ox}}$ ($C_{\text{ox}} + C_{\text{q}}$), where quantum capacitance ($C_{\text{q}}$) can be approximated as $q^2D_{\text{OS}}$ (density of states)$^{\text{34,35}}$. Only for $C_{\text{ox}} \ll t_{\text{ox}}$ does this expression become equivalent to $C_{\text{ox}}$. Because multiple parameters in Table 1 depend on $n_{S}$, benchmarking these versus $n_{S}$ is recommended to evaluate devices from different studies. A suggested list of benchmarking plots to evaluate device parameters and performance metrics is provided in Table 2.

Drain current is the key output of a FET and is also frequently benchmarked and compared. However, many comparisons are over-simplified and not fairly conducted as the drain current depends on many parameters. As mentioned in Table 2, we recommend benchmarking $I_{D}$ versus $L_{\text{ch}}$ at certain $V_{\text{GS}}$ and $n_{S}$ values, enabling fair comparison between devices having different channel lengths. On the other hand, if a record $I_{D}$ is claimed, we recommend benchmarking the maximum $I_{D}$ versus $n_{S}$, because it is a much closer indicator for the eventual drive current and ultimately sets the operating delay of a circuit stage (delay $\tau \propto CV_{\text{DS}}/I_{\text{DS}}$). As mentioned previously, assuming limited short-channel effects, $I_{\text{sat}}$ mainly depends on $n_{S}$ and not on $E_{\text{ox}}$. Usually, one performance metric depends on multiple parameters; hence, key parameters should be annotated on the benchmarking plot (Table 2).

### Reporting and benchmarking example

To demonstrate reporting and benchmarking based on the principles proposed above, MoS$_2$ is chosen as the example emerging channel material because it is among the most studied semiconducting nanomaterials in recent years and represents a family of 2D materials that holds promise for future transistor applications. Figure 2a shows an example transistor based on monolayer (1L) MoS$_2$ grown by chemical vapour deposition. The device is top-contacted and back-gated, which is the most common and convenient FET structure used to explore emergent channel materials. The approach is as follows:

**Step 1.** The structural parameters of the device are determined and labelled (Fig. 2a). In this example, the gate insulator is AlO$_x$, which is grown by atomic layer deposition with the oxide capacitance ($C_{\text{ox}} \approx 280\, \text{nF/cm}^2$) evaluated from a capacitance–voltage measurement of a large-area test capacitor. The thickness of the oxide ($t_{\text{ox}} \approx 20\, \text{nm}$) is further confirmed by cross-sectional transmission electron microscope (TEM) imaging. From the thickness and capacitance, the dielectric constant of the oxide is estimated to be $\varepsilon_{\text{ox}} \approx 6$. Other dimensions, such as $L_{\text{ch}}$, $W_{\text{ch}}$, and $L_{\text{ch}}$, are confirmed by scanning electron microscopy (SEM) after electrical characterization.

**Step 2.** $I_{D}$–$V_{\text{DS}}$ and $I_{D}$–$V_{\text{GS}}$ characterizations are performed, making sure that $V_{\text{GS}}$ and $V_{\text{DS}}$ are swept high enough for the device to reach saturation, and the $V_{\text{GS}}$ sweep range is sufficient to observe $I_{\text{sat}}$ in both the linear ($I_{\text{DS}}$) and saturation (high $V_{\text{DS}}$) operation regions. An $I_{\text{sat}}/I_{\text{DS}}$ of $\sqrt{4\times10^7}$ at $V_{\text{DS}} \approx 4\, \text{V}$ can be extracted from the subthreshold curve in Fig. 2b. $I_{\text{sat}}$ is extracted at $n_{S} \approx 1.4 \times 10^{13}\, \text{cm}^{-2}$. $I_{\text{sat}}$ is extracted under subthreshold conditions, where $V_{\text{GS}} < V_{\text{T}}$ yielding a negative $V_{\text{T}}$, and $n_{S} \approx 0$. The larger hysteresis for $V_{\text{DS}} = 4\, \text{V}$ in Fig. 2b,c highlights the impact of the larger source–drain field on the interface charges in the channel. Due to hot-carrier stress from the high $V_{\text{DS}}$ (explained later), $I_{\text{sat}}$ increases for high $V_{\text{DS}}$, resulting in an extracted DIBL of $-274$ to $-436\, \text{mV}\, \text{dec}^{-1}$, considering the effect of hysteresis. Also, from the transfer curves in Fig. 2c, the maximum $g_{me}^{\text{sat}}$ (sat) and $g_{me}^{\text{lin}}$ (lin) are estimated to be $\approx 59\, \mu\text{S}\, \mu\text{m}^{-1}$ and $\approx 1.7\, \mu\text{S}\, \mu\text{m}^{-1}$, respectively. In Fig. 2d, approximate current saturation is observed, with $I_{\text{sat}}$ around $325\, \mu\text{A}\, \mu\text{m}^{-1}$ obtained at $n_{S} \approx 1.3 \times 10^{13}\, \text{cm}^{-2}$ at $V_{\text{DS}} = 4\, \text{V}$. The blue and red points show the linear and saturation regions, approximately. The $I_{D}$–$V_{\text{DS}}$ spacing is sublinear at the highest $V_{\text{DS}}$, which is a sign of possible self-heating.

Figure 2a–d is used for primary characterization of one device, and more derived plots are shown in Fig. 2e–h, providing a more complete picture of the device characteristics. The device spread and parameter variations based on ten similar TLM structures are shown in Supplementary Fig. 5. The full range of $S$ and $I_{D}$ is plotted in Fig. 2d, with a minimum $S$ of $280\, \text{mV}\, \text{dec}^{-1}$ extracted in the subthreshold regime. Additionally, because $V_{\text{T}}$ depends on $V_{\text{DS}}$, it is key to extract $V_{\text{T}}$ at the associated $V_{\text{DS}}$ (as noted in Table 1). $R_{\text{t}}$ and $R_{\text{d}}$ and subsequently $\mu_{\text{ox}}$ are extracted by using a TLM
structure as shown in Fig. 2f–h. The $R_\text{s}$ is estimated to be ~2.1 kΩµm, which is comparable to the $R_\text{sh}$ of 2.8 kΩµm for the device with channel length of 280 nm. The relation between $n_s$ and extracted $R_\text{s}$ is plotted in Fig. 2g to show the effect of the overall back-gate on the contact resistance (that is, contact gating\textsuperscript{32–34}). Figure 2h shows that $\mu_\text{sat}$ decreases from 59 to 40 cm$^2$ V$^{-1}$ s$^{-1}$ with increasing $n_s$, probably due to the increased electron scattering with the oxide surface roughness.

Step 3. As a simplified example, we benchmark key device performance parameters in Fig. 3 (a limited number of reports are included). Currently, most papers do not report $I_\text{D}-V_\text{GS}$ at $V_\text{DS}$ (sat) or close to $V_\text{DD}$, as recommended above. Hence, plotting $I_\text{max}$ versus $n_s$ at certain $V_\text{GS}$ (for example, $V_\text{GS} = 1$ V) while annotating $I_\text{sh}$ is an acceptable approach (Fig. 3a). The upper limit of the carrier density is set at $n_s = 10^{19}$ cm$^{-2}$, ensuring a fair comparison of $I_\text{max}$. The $I_\text{max}/I_\text{sh}$ ratio annotated on the right axis is also shown in the dashed lines in Fig. 3a. Owing to better electrostatic control from the gate, devices with a larger $L_\text{ch}/$EOT ratio tend to yield higher $I_\text{max}/I_\text{sh}$ (where EOT is the equivalent oxide thickness). Other parameters also play a role, such as the leakage currents through the gate insulator or from source to drain. Large channel width can also produce a more accurate width-normalized $I_\text{max}$, especially when $I_\text{sh}$ is below the instrument noise floor. For example, a relatively high $I_\text{max}/I_\text{sh}$ ratio has been demonstrated in ref. \textsuperscript{35} in devices with 20-µm channel width. Further study is still needed to investigate how to achieve high $I_\text{max}$ and small $I_\text{sh}$ in aggressively scaled devices (small $I_\text{sh}$, $L_\text{ch}$ and EOT).

As mentioned previously, a high drain current in the saturation regime is a key performance metric. In Fig. 3b, $I_\text{sh}$ is plotted versus $n_s$ from representative studies of FETs based on MoS\textsubscript{2} as the channel material. We note that $I_\text{sh}$ is extracted at different $V_\text{DS}$ values, because different devices have different channel lengths, as annotated in Fig. 3b. We caution against plotting $I_\text{sh}$ versus $n_s$ because it implies that $I_\text{sh}$ is the main limiting factor for $I_\text{sh}$, which is not necessarily true, especially for scaled devices where contact resistance typically dominates $I_\text{sh}$ performance. Importantly, it is clear that $I_\text{sh}$ needs to be further improved to meet the high-performance target of the most recent technology guidelines (at $V_\text{DD} = 0.65$ V near 2030)\textsuperscript{36}. Many reports have already used high $n_s$, but fell short regarding $I_\text{sh}$ even with channel lengths down to ~10 nm (ref. \textsuperscript{37}), being strongly limited by their contacts.

Recently, semimetal contacts such as bismuth have been shown to produce high-quality contacts\textsuperscript{38}. It is nevertheless noteworthy that the two Bi-1L MoS\textsubscript{2} devices have a wide range of $I_\text{sh}$ performance, encompassing all the other devices in Fig. 3b, yet the channel length difference between the two devices is only 115 nm. Interestingly, one of the Bi-contacted devices ($L_\text{ch} = 150$ nm) actually underperforms other Au-contacted devices with longer channel lengths. Hence, although some approaches show potential to achieve the International Roadmap for Devices and Systems (IRDS) high-performance goal of $I_\text{sh}$ for the post-2030 era\textsuperscript{39}, further investigation is still needed to reliably and reproducibly realize high $I_\text{sh}$ from a monolayer channel. In next-generation FETs, $I_\text{sh}$ could also be increased by shifting to nanosheet device designs, which stack...
multiple channels vertically to improve current density in the same device footprint.

In some reports, a proper saturation current is not given. Also, because different devices use different channel lengths, $I_C$ is often extracted at different $V_{DS}$. To highlight the impact of channel length, we recommend benchmarking $I_D$ versus $L_{ch}$ at $V_{DS} = 1$ V and $n_s = 10^{13}$ cm$^{-2}$. This plot enables a direct comparison of devices with similar $L_{ch}$. In Fig. 3c, with channel length decreasing from 200 nm to 38 nm, devices contacted by both Bi$^{35}$ and Sn$^{40}$ yield relatively large increases in drain current. We note that the Bi-contacted devices are based on different MoS$_2$ films. The different quality of the MoS$_2$ may partially contribute to the large increase of $I_D$ with a relatively small change in $L_{ch}$. Nevertheless, Fig. 3c,d presents the potential of atomically thin materials for producing high drain current, especially for scaled devices.

In Fig. 3d, $R_s$ is plotted against $n_s$. Considering most devices have gated contacts (that is, the back-gate modulates the channel and contacts$^{23–34}$). Although some reported $R_s$ values reach below 500$\Omega$um, their TLM extractions are all based on channel resistance-dominated devices, which can lead to questionable validity in their claimed $R_s$ (an artificially small or even a negative $R_s$ can be extracted, see Supplementary Note 3 for details). We advocate that, if a record $R_s$ is claimed from TLM, $R_{sh}$ should be cross-examined by using other methods such as four-probe measurements, which can provide a relatively accurate estimation of $R_{sh}$ versus $n_s$ (Supplementary Note 3). With $R_{sh}$ versus $n_s$ from four-probe measurements, $R_s$ versus $n_s$ can be derived by deducting the $R_{sh}$ from the $R_{tot}$ to confirm the TLM extracted value. Showing extraction of $R_s$ from many TLM structures can also increase confidence in the data by providing an average value of the $R_s$ rather than just the minimal value from a single TLM$^{10,42}$. Furthermore, $R_s$ is heavily impacted by contact gating, as is evident from the similar trends of $R_s$ versus $n_s$ observed in different studies. Accordingly, further research is needed to obtain a small $R_s$ without gating the contacts.

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**Fig. 3** | Example benchmarking device performance of monolayer MoS$_2$ FETs. **a**, Benchmarking $I_{max}$ versus $L_{ch}$. The $I_{max}$ is extracted at $n_s = 10^{13}$ cm$^{-2}$. For simplicity, $I_{min}$ values of the data points are extracted at their respective smallest current. More rigorous benchmarking of $I_{max}$ versus $L_{ch}$ is described in Supplementary Note 1. **b**, Benchmarking $I_{max}$ versus $n_s$, where the channel length (in nm) is labelled next to the contact metals used in the devices. $I_{max}$ values are extracted at different $V_{DS}$ (listed in Supplementary Table 1). These devices do not have the same $V_{DS}$(sat) as devices with different channel lengths and saturated at different $V_{DS}$. The IRS high performance (HP) is shown in a range of $n_s$ to represent uncertainties of the carrier density in future generation technologies. **c**, Benchmarking $I_D$ versus $L_{ch}$ at $V_{DS} = 1$ V and $n_s = 10^{13}$ cm$^{-2}$. Reference$^{16}$ uses a top-gate, whereas other reports use a back-gate. **d**, Benchmarking $R_s$ versus $n_s$ in a few representative reports. The shaded regions represent uncertainties reported in the respective studies (Ag$^{26}$, AlO$_x$ doped/Au$^{38}$, In/Au$^{55}$, Sn/Au$^{56}$, and Au use standard error from the linear regression of TLM). The $R_s$ versus $n_s$ of Sb$^{57}$ is obtained using the Y-function method. The filled and open symbols show that the shortest channel device in the TLM structure is 2$\Omega$ and $R_s$ dominated, respectively. If $R_{sh}$ dominates or the $R_s$ is over an order of magnitude smaller than $R_{sh}$ for the smallest device in TLM, the extracted $R_s$ is of questionable validity; that is, the filled symbol data are more reliable (according to Supplementary Note 3). Different colours are assigned to different reported devices. The purple Au data denote devices described in Fig. 2. Most of the data are extracted from published reports: Ag$^{26}$, AlO$_x$ doped/Au$^{38}$, In/Au$^{55}$, Sn/Au$^{56}$, Sb$^{57}$, In$^{58}$, Sn$^{40}$. In **a** and **c**, reference numbers are added for Au-contacted devices to better differentiate their performance. A few studies are plotted as dotted lines to highlight the trends and to improve the clarity of the plots.
Looking forward, many opportunities remain to develop transistors that simultaneously have small contact resistance, high \( I_{\text{on}}/I_{\text{off}} \) ratio and minimal short-channel effects by using emergent nanomaterials. To achieve this technological goal, interface engineering at the contacts and gate dielectric needs to be further investigated\(^\text{43-45}\), along with progress in material synthesis\(^\text{46}\) and integration\(^\text{47}\). Moreover, it is important to focus on channel thicknesses below ~3 nm, where low-dimensional nanomaterials can excel compared to Si, which suffers from poor carrier transport properties and a widened bandgap in this thickness regime\(^\text{6}\).

In addition to the example benchmarking plots in Fig. 3, other benchmarks can also be used to compare different devices, for example, as included in Table 2, plotting \( I_{\text{on}}/I_{\text{min}} \) versus \( t_{\text{ox}} \) or \( I_{\text{off}}/I_{\text{on}} \) versus \( L_{\text{sat}}/EOT \) to compare the off-state device performance. Plotting \( SS \) versus \( C_{\text{on}} \) or \( SS \) versus \( \log_{10}(I_{\text{on}}) \) (ref. \(^\text{49}\)) can be used to evaluate subthreshold behaviour and trends across different devices. Finally, to show the quality of the channel materials, the channel sheet resistance or conductivity mobility can be plotted versus carrier densities, as in Fig. 2h. Representative reports with relatively large \( I_{\text{on}} \) are listed in Supplementary Table 1, including results for FETs with both monolayer and multilayer MoS\(_2\) channels (example benchmarking plots are provided in Supplementary Note 6). In the literature, notable benchmarking examples can be found in refs. \(^\text{38,50}\), which highlight different channel materials, and in ref. \(^\text{31}\), which focuses on device performance in integrated circuits (speed, gain, density, power consumption, fan-out capabilities, and so on).

Conclusions

Our guidelines should help put key performance metrics in a proper context and enable researchers to effectively report and benchmark emergent transistors based on various emergent nanomaterials. Although each of the listed metrics is important, it is not necessary—nor always possible—to extract and present all of them. As such, it is essential to completely describe the device geometry, to collect and report appropriate current–voltage characteristics, and to describe in detail the procedures followed in the experiments. The approaches used to analyse data and extract benchmarking metrics should also be described in detail. Depending on the context and need, we recommend three sets of parameters to report and benchmark. The first includes maximum saturation current, on/off current ratio, transconductance and subthreshold swing. These values can be directly obtained from the measured \( I-V \) characteristics that cover both linear and saturation regimes. These values are mainly determined by the intrinsic material properties, gate stack configuration and contact quality. The second includes the derived parameters such as mobilities and contact resistance, where uncertainty and statistical spread on these derived parameters should be shown. The third set of parameters are those specific to certain transistor demonstrations based on the target application\(^\text{2,3}\). For example, DBL is essential when reporting and evaluating ultra-scale FETs. It is important—whenever possible—to benchmark against other novel materials and also the state of the art in mature technological\(^\text{19,20}\). By using these guidelines, it should be possible to comprehensively and consistently reveal, highlight, discuss, compare and evaluate device performance, thus helping to identify advances and opportunities in the search for improved transistors.

Data availability

The data used in this paper are available from the corresponding authors upon reasonable request.

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Author contributions
All authors contributed to the preparation of the manuscript.

Competing interests
The authors declare no competing interests.

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