Improved Analysis of Current-Steering DACs Using Equivalent Timing Errors

Daniel Beauchamp*† and Keith M. Chugg†
*Jariet Technologies, 103 W Torrance Blvd, Redondo Beach, CA 90277
†Ming Hsieh Department of Electrical Engineering, University of Southern California, Los Angeles, California 90089
{dbeaucha, chugg}@usc.edu

Abstract—Current-steering (CS) digital-to-analog converters (DACs) generate analog signals by combining weighted current sources. Ideally, the current sources are combined at each switching instant simultaneously. However, this is not true in practice due to timing mismatch, resulting in nonlinear distortion. This work uses the equivalent timing error model, introduced by previous work, to analyze the signal-to-distortion ratio (SDR) resulting from these timing errors. Using a behavioral simulation model we demonstrate that our analysis is significantly more accurate than the previous methods. We also use our simulation model to investigate the effect of timing mismatch in partially-segmented CS-DACs, i.e., those comprised of both equally-weighted and binary-weighted current sources.

I. INTRODUCTION

Current-steering DACs are considered to be the de facto solution for transmitters in modern high-speed applications [1], including cellular communication, electronic warfare, and automotive radar. The CS-DAC generates an analog signal from a digital input sequence by combining current sources, as shown in Fig. 1. We refer to this as a fully-segmented CS-DAC, since each current source is equally weighted. In contrast, partially-segmented CS-DACs are hybrid architectures that are comprised of both equally-weighted and binary-weighted current sources. Regardless of the architecture, the ideal output is a perfect zero-order-hold (or staircase-like) representation of the digital input sequence. However, this is not true in practice due to nonlinear distortion caused by various errors.

Typically, errors in CS-DACs are classified as either static [2]. Static errors, which are time-invariant and memoryless, are mainly caused by current source mismatch and are treatable by various calibration techniques [3], [4], [5]. Dynamic errors, on the other hand, are more difficult to calibrate because they only appear during switching instants and last for a small fraction of the sample period. Hence, this necessitates calibration circuitry with fine resolution in both amplitude and time [6], [7]. Timing-related mismatch, for example, causes the current cells to fire at different times [8]; nominally, they all fire simultaneously at each switching instant.

Dynamic errors, such as timing-related mismatch, limit the high-frequency performance of the DAC [6], which makes their analysis critical. Previous research on this topic is presented in [8] and [9], where it was proposed that timing errors for each current cell can be lumped into an equivalent timing error for each switching instant. This is a key contribution that simplifies the analysis considerably. Under this framework, the DAC error is comprised of narrow pulses with amplitudes that are proportional to the difference between consecutive input codes. The signal-to-distortion ratio (SDR) is then derived as a function of the timing error spread, which is assumed to be the same for each current cell.

In this work, we utilize the equivalent timing error introduced in [8] and provide a more accurate analysis of the resulting model. The key difference in the analyses is that the approach in [8] implicitly assumed that the timing errors are present during the entire sample period. While this assumption leads to an accurate SDR for the Nyquist band, it is not as accurate for the wideband SDR, i.e., where all frequency components of the error are considered. In this work we make no such assumption, resulting in a significantly more accurate expression for the wideband SDR (as we confirm with behavioral simulations). The limitations of the equivalent timing error model are stated after characterizing the SDR over frequency. In addition, we use the behavioral model to explore the SDR for partially-segmented architectures.

The rest of the paper is organized as follows. In Section II, we provide background information on fully-segmented CS-DACs and the problem of timing-related mismatch. In Section III, we carry out the SDR analysis using the equivalent timing error model and compare it to that in [8]. In Section IV, we validate our analysis using a behavioral model, state its limitations, and simulate the SDR for partially-segmented architectures. Finally, we conclude the paper in Section V.

II. BACKGROUND

A. Fully-Segmented Current Steering DAC

A block diagram of an M-bit fully-segmented CS-DAC is shown in Fig. 1. It is modeled as an array of \( C = 2^M - 1 \) current cells, each weighted by \( I_a/2 \) with complementary switching. A binary-to-thermometer decoder is used to map the binary input code \( b_{M-1} \cdots b_0 \) to a thermometer code \( t_{C-1} \cdots t_0 \). The number of ones in the decoder output is equal to the decimal representation of its binary input, e.g., for a 2-bit DAC, \( 00 \rightarrow 000, 01 \rightarrow 001, 10 \rightarrow 011, \) and \( 11 \rightarrow 111 \). Each current cell is steered to either the positive or negative output, depending on the input code. In the absence of nonidealities,
the DAC output is
\[ y_{\text{ideal}}(t) = u(t) * \sum_{n=-\infty}^{\infty} I_u \Delta x_n \delta(t-nT_s) \] (1)
for a digital input sequence \( x_n \in \{0, \ldots, 2^M-1\} \), where \( \Delta x_n = x_n - x_{n-1} \), \( u(t) \) is the unit step function, and * denotes convolution.

**B. Equivalent Timing Error Model**

In (1), it is assumed that the current cells fire simultaneously at each switching instant, i.e., the DAC output changes abruptly at time \( nT_s \) when \( \Delta x_n \neq 0 \). In practice, the \( m \)th current cell fires at \( nT_s + \tau_m \), where \( \tau_m \) is the timing error for that cell, \( m \in \{0, \ldots, C-1\} \). As in [8], we model \( \tau_m \) as independently drawn from a mean-zero, normal distribution with variance \( \sigma^2 \) (i.e., \( \tau_m \sim N(0, \sigma^2) \)). The authors in [8] begin the analysis by considering the net charge error introduced by the code transition \( x_{n-1} \rightarrow x_n \). Next, they formulate an equivalent timing error for this transition, \( T_e(n) \), which allows the DAC output to be written as
\[ y(t) = u(t) * \sum_{n=-\infty}^{\infty} I_u \Delta x_n \delta(t-nT_s-T_e(n)) \] (2)
where
\[ T_e(n) = \begin{cases} \frac{1}{|\Delta x_n|} \sum_{m=\min(x_n,x_{n-1})}^{\max(x_n,x_{n-1})-1} \tau_m & \Delta x_n \neq 0 \\ 0 & \Delta x_n = 0 \end{cases} \] (3)

Note from (3) that timing errors only occur when the input code changes, i.e., \( \Delta x_n \neq 0 \). In this case, the equivalent timing error is the average of the timing errors for each current cell that switches for the \( x_{n-1} \rightarrow x_n \) code transition.\(^1\)

The error based on the equivalent timing error model is
\[ e(t) = y(t) - y_{\text{ideal}}(t) \]
and an example is illustrated in Fig. 2. Note that \( e(t) \) is comprised of narrow pulses with magnitudes \( I_u|\Delta x_n| \) and durations \( |T_e(n)| \). The magnitude of the net charge error introduced by the \( x_{n-1} \rightarrow x_n \) transition is \( Q_e(n) = I_u|\Delta x_n T_e(n)| \), i.e., the area under the error pulses.

\(^1\)A derivation of the equivalent timing error, \( T_e(n) \), is presented in [8].

\[ E[Q_{\text{previous}}(n)] = \mathbb{E} \left[ \left( \frac{Q_e(n)}{T_e(n)} \right)^2 \right] \] (4a)
\[ = \mathbb{E} \left[ \left( \frac{T_e(n)}{T_s} \right)^2 \Delta x_n^2 t_u^2 \right] 
\] (4b)
\[ = \frac{\sigma^2}{T_s^2} \mathbb{E}[|\Delta x_n|] \] (4c)
where \( \mathbb{E} \) denotes discrete time averaging. We use (4c) to define the wideband SDR as
\[ \text{SDR} = \frac{P_{\text{sig}}}{\frac{\sigma^2}{T_s^2} \mathbb{E}[|\Delta x_n|]} \] (5)
since the denominator is comprised of the total error power. Note that in (4a) it is implicitly assumed that the charge error occurs over the entire sample period, \( T_s \). However, the charge error actually occurs over a small fraction of \( T_s \), as illustrated in Fig. 2. In Section III, we carry out the analysis accordingly, resulting in a more accurate expression for the wideband SDR. Lastly, the authors in [8] specialize (5) for low-frequency sinusoidal inputs with the error power limited to the first Nyquist band, resulting in an SDR of
\[ \text{SDR}_{\text{Nyquist}} = \frac{A_1}{8 f_s f_s \sigma^2} \] (6)
where \( f_s \) is the input frequency and \( A_1 = \frac{1}{2} (2^M - 1) \) is the input amplitude.\(^2\)

**III. ANALYSIS**

The error shown in Fig. 2 may be written as the sum of non-overlapping pulses \( e_n(t) \), i.e.,
\[ e(t) = \sum_{n=-\infty}^{\infty} e_n(t) \]
where
\[ e_n(t) = -\text{sgn}(T_e(n)) I_u \Delta x_n \text{rect} \left( \frac{t-(nT_s+T_e(n)/2)}{|T_e(n)|} \right) \] (7)
\(^2\)A more detailed derivation of (6) is presented in [9].
and \( \text{rect}(t) = 1 \) if \( |t| \leq 1/2 \) and 0 if \( |t| > 1/2 \). Note that \( e(t) \) is a random process, where the randomness comes from the equivalent timing errors, \( T_e(n) \). The expected error power is

\[
E[P_e] = E \left[ \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{T/2} e^2(t) dt \right] = \lim_{N \to \infty} \frac{1}{2N+1} \sum_{n=-N}^{N} \left( \int_{-(2N+1)T_e/2}^{(2N+1)T_e/2} e_n^2(t) dt \right) = \lim_{N \to \infty} \frac{1}{2N+1} \sum_{n=-N}^{N} E[A_n] = \langle E[A_n] \rangle \tag{8}
\]

where \( A_n \) is a random variable defined by

\[
A_n = \frac{1}{T_s} \int_{-(2N+1)T_e/2}^{(2N+1)T_e/2} e_n^2(t) dt, \quad |n| \leq N \tag{9}
\]

Taking the expected value of (9) and then averaging yields

\[
E[P_e] = \left\langle E \left[ \frac{T_e(n)}{T_s} \Delta x_n^2 n^2 \right] \right\rangle \tag{10}
\]

Note from (3) that \( T_e(n) \sim N(0, \sigma^2/\Delta x_n) \), \( \Delta x_n \neq 0 \). Therefore, \( [T_e(n)] \) has a folded normal distribution \([10]\) with mean

\[
E[|T_e(n)|] = \frac{\sigma}{|\Delta x_n|^{1/2}} \sqrt{\frac{2}{\pi}} \quad \text{which we substitute into (10), yielding}
\]

\[
E[P_e] = \frac{1}{T_n} \sqrt{\frac{2}{\pi}} \sigma I_u^2 \langle |\Delta x_n|^{3/2} \rangle \tag{11}
\]

At this point, we can compare our analysis to that in [8]. Specifically, we observe that (10) and (4b) differ by a factor of \( |T_e(n)|/T_s \) inside the expectation, i.e., the duty factor of the error pulses. In practice, \( 0 < |T_e(n)|/T_s \ll 1 \), which means that this difference is nontrivial. The difference arises because the analysis in [8] implicitly assumes that the charge error is distributed over the entire sample period. In our analysis, we do not make this assumption. Using our analysis, the SDR based on a sinusoidal input at full scale is

\[
\text{SDR} = 10 \log_{10} \left( \frac{P_{\text{sig}}}{E[P_e]} \right) = 10 \log_{10} \left( \frac{(2^M - 1)^2}{8f_s \sqrt{\frac{2}{\pi}} \langle |\Delta x_n|^{3/2} \rangle} \right) - 10 \log_{10} \sigma \tag{12}
\]

where \( P_{\text{sig}} = \frac{(2/(2^M - 1))^2}{2} \) and \( E[P_e] \) comes from (11).

IV. SIMULATIONS

In this section, we simulate CS-DACs using a behavioral model with an oversampling ratio (OSR) of 4096, i.e., one sample period, \( T_s \), is represented by 4096 samples. The large OSR is so that we can capture timing errors that are a very small fraction of the sample period, e.g., we are interested in \( \sigma/T_s \) down to \( 10^{-3} \). Note that using an OSR = 4096 is memory intensive, so we ran the simulations on a modern workstation with 128GB of RAM. In Fig. 3, we plot simulated and analytical results of the SDR versus \( \sigma/T_s \) for \( M \)-bit DACs (\( M = 3, 5, 7, 8 \)). Note that the analysis in this work accurately captures the wideband SDR, i.e., with no filter at the DAC output. In contrast, the analysis in [8] accurately captures the Nyquist band SDR, i.e., where there is brick wall filter at the DAC output with a cutoff frequency of \( f_s/2 \). Hence, the Nyquist band SDR is substantially higher since it ignores the spectral content of the error beyond \( f_s/2 \). It is worth mentioning how the SDR is extracted from the simulations. First, the behavioral model is run with zero timing errors to generate the ideal output, \( y_{\text{ideal}}(n) \). Then, it is run with timing errors to generate the nonideal output, \( y(n) \), resulting in an error of \( e(n) = y(n) - y_{\text{ideal}}(n) \). For the wideband SDR, the power of the sequence \( e(n) \) is used. For the Nyquist band SDR, the power spectral density of \( e(n) \) is computed, and only the frequency components from DC to \( f_s/2 \) are included in the error power.

In Fig. 4, we plot the wideband SDR from simulation (blue) and compare it with two different analyses over frequency. The red markers are from (12) (this work), and the purple markers are derived from the analysis in [8], i.e., using (5) as the SDR. Note that our analysis, in contrast to that in [8], is in closer agreement with the simulations. This is because for practical values of \( \sigma/T_s \), i.e., \( 0 < \sigma/T_s \ll 1 \), the assumption in (4a) that the charge error is distributed over the entire sample period becomes less accurate. Since we do not make this assumption, there is a considerable difference between the two analyses for the small \( \sigma/T_s \) considered in Fig. 4.
Referring again to Fig. 4, note that our analysis diverges from the simulation as the number of bits, $M$, is increased (by up to 6.3dB for $M = 8$ and $f_0/f_s \approx 0.5$). This divergence is caused by the breakdown of the equivalent timing error model for larger values of $M$ at high frequencies. This is qualitatively shown in Fig. 6(a) and Fig. 6(b), where we illustrate the squared error for various code transitions for 3-bit and 6-bit DACs, respectively. Note that the squared errors in the 3-bit cases closely resemble rectangular pulses, i.e., they are well-suited for approximation via equivalent timing errors. In contrast, the squared errors for the 6-bit cases change gradually in the vicinity of the switching instant.

We also used the behavioral model to investigate partially-segmented DACs. We considered $M$-bit DACs with the first $T$ bits (MSBs) thermometer-decoded into $2^T - 1$ unit elements and binary weights for the remaining $M - T$ bits (LSBs). In Fig. 5, we plot simulations of the wideband SDR versus $T$ for $M$-bit partially-segmented DACs ($M = 8, 10, 12$). For $T < 6$, the SDR increases by approximately 3dB/bit. However, the SDR eventually saturates, i.e., the improvement gets smaller for each bit added when $T \geq 6$. For example, going from $T = 8$ to $T = 9$ yields only a 1dB increase in SDR. Lastly, it should be noted that if $M$ is sufficiently large, e.g., $M \geq 8$, then increasing it further does not improve the SDR, i.e., the impact of quantization on the timing errors becomes negligible.

V. CONCLUSION

In this work, we presented analysis of the wideband SDR due to timing errors in fully-segmented CS-DACs, which was validated using a behavioral model and proven to be significantly more accurate than the previous analysis. In addition, we used the model to characterize the SDR for partially-segmented architectures. Thus, this work provides a method for accurately specifying error tolerance in the circuit design to achieve a given SDR. A useful extension would be to improve the model accuracy for high-resolution DACs at high-frequency operation. This may be done by substituting the equivalent timing error model with one that more accurately captures the error pulse characteristics.

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