In this paper, a novel Asymmetrical Multi-Level Inverter (AMLI) is suggested to solve the voltage quality problem. The suggested AMLI has been constructed based on series connection of sub-AMLIs to create a high-step quasi-sinusoidal voltage with considering few semiconductor switches. The ladder capacitors of sub-AMLI have been clamped to the H-bridge structure via several bi-directional switches. Based on an innovative geometric progression for DC power supplies of AMLI, it can operate as so-called odd-nary AMLI. It has effectively created a quasi-sinusoidal with high steps i.e., low Total Harmonic Distortion (THD) with respect to low number of switches. The performance of suggested AMLI has been thoroughly compared with other inventive asymmetrical and symmetrical multilevel inverters. Following that, scission-style harmonic elimination based on Pulse Width Modulation (PWM) is introduced to enhance voltage quality of AMLI. Three prominent criterions related to voltage quality i.e., desired fundamental component, elimination of third harmonic and reduction of THD have been assigned as objective functions of optimization problem. Considering the multi-objective nature of the optimization problem, non-dominated sorting Multi-Objective Grey Wolf Optimizer (MOGWO) has been implemented to solve the optimization problem, and then compared with Non-dominated Sorting Genetic Algorithm II (NSGA-II). To sum up, the relevant analytical studies along with both the simulation and experimental results have transparently validated the performance of suggested AMLI. Also, the voltage quality problem using MOGWO-based scission-style harmonic elimination strategy has been well approved.

1. Introduction

Multilevel inverters have generally functioned as an AC voltage synthesizer to create a quasi-sinusoidal voltage i.e., rough sinusoidal waveform with desired steps using several DC power supplies [1]. Hence, high number of switching components has let the multilevel inverter to render a quasi-sinusoidal voltage with high quality [2]. The first multilevel inverter prototype has been constructed and analyzed by Nabae et al. [3]. Since that time, these structures have been captivating more industrial and academic consideration in the various medium voltages that such these multilevel structures have investigated in several literatures to elucidate the rating problem related to voltage and current of switching components [4, 5, 6, 7, 8].

One of the strongpoints of these structures other than creating a pertinent quasi-sinusoidal waveform is their feasibility to occupy them in transmission and sub-transmission levels for such these reasons: reduction of SPL, PIV, dV/dt and EMI [9, 10, 11]. One more special strongpoint of these structures is their capability in harmonic alleviation, avoiding the high frequency of semiconductors’ switching either reduction of the inverter’s output power [12, 13, 14].

Multilevel inverter is known as one of the most advanced and prominent power electronic structures. They have been widely applied in manifold compensators and energy conversion systems e.g., HVDC, FACTS, PV, UPS and Industrial drive systems. The conventional multilevel inverters have been essentially divided into three categories that are CHB, NPC, FC [15, 16, 17]. It is worth mentioning that, the conventional multilevel inverters have borne high switching elements such as: switches, capacitors, diodes and the suchlike toward producing high step number. Over the past several years, many different structures and technologies based on IGBT and MOSFET semiconductors with have been introduced [18, 19, 20, 21].

Apart from the beneficial advantages of multilevel inverters, existence of a large number of semiconductor switches is their most important disadvantage that consequently will bring such detriments: complexity of the circuit and control strategy, increase of the structure's cost-price, decrease of the reliability, and maintenance of the structure.

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Therefore, it is essential that the number of switching components to be decreased. Across the world, the scholars are attempting and venturing to improve and introduce high performance multilevel inverters with reduced components so that the aforementioned problems related to the conventional multilevel inverters to be obviated e.g.: [22, 23, 24, 25, 26]. Such the reduced multilevel topologies have generally competed with each other over the: low THD, and number of switching components as well as high-step of quasi-sinusoidal voltage, in which case, an inventive AMLI has been designed and introduced in this paper so that not only low number of components to be applied, but also high-step quasi-sinusoidal voltage to be attained. The proposed sub-AMLI has been designed based on the ladder capacitor clamped to H-bridge by means of the bi-directional switches. Based on an innovative geometric progression for DC power supplies of AMLI, it can operate as so-called odd-nary AMLI. In recent years, the power electronics experts have been endeavoring to enhance the conventional multilevel inverter structures and voltage quality. Therefore, undesirable voltage harmonics of multilevel inverters with DC power supplies can be reduced by the advantageous modulation strategies such as PWM and SVPWM [27, 28].

It should be considered, these strategies cannot accurately reduce the relevant harmonic components. Another strategy has been functioned in accordance with selection of the triggering angles to reduce the lower order harmonics viz. third, fifth, seventh from the quasi-sinusoidal voltage which is recognized by SHE [29, 30, 31]. A principal problem

Figure 1. (a). Proposed cascaded multilevel inverter. (b). Prototype's photograph of suggested AMLI.
as regards of such these strategies is acquiring the arithmetic solution of nonlinear transcendental equations which include the trigonometric clauses. These relationships can be also solved by iterative methods including Newton–Raphson [32]. Unfortunately, its dependency on the initial estimation points may cause trapping in local optima. Therefore, this approach can’t be considered to unravel the SHE problem with various triggering angles whereas have no initial estimation points. One more strategy has been operated via converting the transcendental equations into the polynomial equations [33, 34]. If the step number of voltage to be increased, the computational burden is highly intensified. As for the capability of heuristic algorithms in solving the complex objective functions, they have been widely used to figure out the optimal triggering angles.

Toward this subject, PWM-based scission-style harmonic elimination has been designed and implemented to enhance voltage quality of AMLI. Hence, three prominent criterions related voltage quality i.e., desired fundamental component, elimination of third harmonic and Reduction of THD have been assigned as objective functions of optimization problem. Considering the multi-objective nature of the optimization problem, non-dominated sorting MOGWO has been implemented to solve the optimization problem, and then compared with NSGA-II. To sum up, the relevant analytical studies along with both the simulation and experimental results have transparently validated the performance of suggested AMLI. Also, the voltage quality problem using MOGWO-based scission-style harmonic elimination strategy has been well approved.

2. Suggested odd-nary multilevel inverter

A new AMLI structure is proposed aimed to provide high-step quasi-sinusoidal with respect to few switch numbers. Suggested AMLI can feasibly act as both the symmetric and statuses. According to the Figure 1, sub-AMLI is composed using DC power supplies, capacitors along with unidirectional and bidirectional semiconductor switches. By cascading of these sub-multilevel inverters the overall construction of the

| ON Switches | \( V_{\text{out,symmetric}} \) | ON Switches | \( V_{\text{out,symmetric}} \) |
|-------------|-----------------|-------------|-----------------|
| \( H_1, S_1, H_1, H_2 \) | 1 | \( S_1, H_1, H_2, (H_1, H_1, H_2, S_1) \) | -1 |
| \( H_1, H_1, H_2, H_2 \) | 2 | \( H_1, H_1, H_2, (S_1, H_2, S_1) \) | -2 |
| \( H_1, H_1, S_1, H_2 \) | 3 | \( H_1, H_1, S_1, (H_1, H_2, H_2) \) | -3 |
| \( H_1, H_1, H_2 \) | 4 | \( H_1, H_1, H_2, H_2 \) | -4 |
| \( H_1, H_1, H_2, H_2 \) | 0 | \( H_1, H_1, H_2, H_2 \) | 0 |

Figure 2. (a). quasi-sinusoidal voltage in symmetrical operation with respect to \( k = 2 \) and \( n = 2 \). b. Experimental results of quasi-sinusoidal voltage in symmetrical operation with respect to \( k = 2 \) and \( n = 2 \).

Table 1. Relevant triggering mode of suggested multilevel inverter as symmetrical operation.
proposed AMLI is revealed. The relevant components utilized in suggested AMLI are given as follows:

\[ N_{\text{uni-directional}} = 4N_{\text{Source}} \]  
(1)

\[ N_{\text{bi-directional}} = (k-1)N_{\text{Source}} \]  
(2)

\[ N_{\text{Switch}} = N_{\text{uni-directional}} + 2N_{\text{bi-directional}} = 2(k+1)N_{\text{Source}} \]  
(3)

\[ N_{\text{capacitor}} = kN_{\text{Source}} \]  
(4)

Having said that, based on an innovative geometric progression for DC power supplies with different ratios a pertinent sinusoidal voltage with uniform step has been provided. Both symmetric and asymmetric operations of suggested structure have been explained in detail in as follows.

To confirm the suggested AMLI concept, 25-level quasi-sinusoidal of Figure 1 (a) has been constructed and analyzed. Todd-nary AMLI can provide staircase sinusoidal voltage with maximum of 120 V on the output. For this case, a single-phase resistive-inductive load is considered able. In the asymmetric structure, the values of DC power supplies are non-equal which are increased in accordance with the particular geometric progression assumed. In general, such these structures are engaged as an alternative approach to minimize the output voltages THD with available electric power components. If each module has k capacitors, DC power supplies' values in terms of capacitors value can be written by:

\[ M_{\text{Level}} = \frac{2(kV_{\text{max}}/N_{\text{Source}})}{V_{\text{dc}} + 1} \]  
(8)

Here, \( M_{\text{Level}}/N_{\text{Source}} \) is introduced to accurately inspect the utilization performance of Switches and DC Sources to create the step level. It can be given as follows:

\[ \frac{M_{\text{Level}}}{N_{\text{Source}}} = 2\left(1 + \frac{k+1}{N_{\text{Switch}}}\right) \]  
(9)

2.2. Multilevel asymmetrical status

For providing a high-step quasi-sinusoidal voltage without adding any components, occupation of asymmetrical multilevel inverters isn’t avoidable. In the asymmetric structure, the values of DC power supplies are unequal which are increased in accordance with the particular geometric progression assumed. In general, such these structures are engaged as an alternative approach to minimize the output voltages THD with available electric power components. If each module has k capacitors, DC power supplies' values in terms of capacitors value can be written by:

\[ V_{\text{in,sub-asymmetric}} = \sum_{j=1}^{N_{\text{Source}}} V_{i,j} \]  
(10)

where, \( V_{c,1}, V_{c,2}, ..., V_{c,k} = V_{c,\text{Vin}} \). Thus:

\[ V_{\text{in,sub-asymmetric}} = kV_{c,\text{Vin}} = V_{\text{dc}} \]  
(11)

Also, DC power supply value of the each module is determined by:

\[ V_{\text{in,sub-asymmetric}} = \frac{2}{N_{\text{Switch}}}(k + (k+1)\frac{N_{\text{Source}}}{N_{\text{Switch}}}) \]  
(12)

where, \( j = 2, 3, ..., k \) and \( i = 1, 2, ..., n \).

Summing the modules' outputs, the maximum voltage of multilevel inverter is attained:

\[ V_{\text{max,asymmetric}} = \sum_{j=1}^{N_{\text{Source}}} V_{\text{in,sub-asymmetric}} = \left(\frac{(2k+1)N_{\text{Source}}}{2} - 1\right) \]  
(13)

Also, voltage step number can be presented by:

\[ M_{\text{Level,asymmetric}} = \frac{2V_{\text{max,asymmetric}}}{V_{\text{dc}}} + 1 \]  
(14)

\[ \frac{M_{\text{Level,asymmetric}}}{N_{\text{Source}}} \]  
for asymmetric status can be given as follows:

\[ \frac{M_{\text{Level,asymmetric}}}{N_{\text{Source}}} = 2/(k+1) \]  
(15)

The advantage of proposed AMLI is its high ability to act the same as “Quinary” with respect to one bidirectional switch along with two capacitors (k = 2), “Septenary” with respect to two bidirectional switches along with three capacitors (k = 3), “Nonary” with respect to three bidirectional switches along with four capacitors (k = 4), “Undenary” with respect to four bidirectional switches along with five capacitors (k = 5), and also in the same way the suggested Odd-nary AMLI has been attained. To have better understanding of aforementioned explanations, the triggering mode of switches considering: two capacitors for each module and two sub-structure modules i.e. \( k = 2 \) and \( n = 2 \) are tabulated in Table 1. Furthermore, the output voltage of each sub-multilevel inverter accompanied by overall output voltage of AMLI is presented in Figure 2 (a). Furthermore, the relevant experimental results are presented in Figure 3 (b).

2.3. Comparison of proposed multilevel inverter with other conventional multilevel inverters

The capability of proposed multilevel inverter has been compared with other conventional multilevel inverters. To validate its capability, it
Table 2. Relevant triggering mode of suggested multilevel inverter as asymmetrical operation.

| ON Switches | \( V_{\text{out, symmetric}} \) | ON Switches | \( V_{\text{out, symmetric}} \) |
|-------------|----------------------------------|-------------|----------------------------------|
| \( S_1, H_1, H_2, H_3 \) | 1                                | \( S_1, H_2, H_1, H_2 \) | -1 |
| \( H_1, H_2, H_1, H_2 \) | 2                                | \( H_3, H_1, H_2, H_3 \) | -2 |
| \( H_3, H_2, S_1, H_3 \) | 3                                | \( H_3, H_2, S_1, H_3 \) | -3 |
| \( S_1, H_2, S_1, H_2 \) | 4                                | \( S_1, H_2, S_1, H_2 \) | -4 |
| \( H_1, H_2, S_1, H_3 \) | 5                                | \( H_2, H_1, S_1, H_2 \) | -5 |
| \( S_1, H_1, S_1, H_2 \) | 6                                | \( S_1, H_2, S_1, H_2 \) | -6 |
| \( H_1, H_2, S_1, H_2 \) | 7                                | \( H_1, H_2, S_1, H_2 \) | -7 |
| \( H_1, H_2, H_1, H_2 \) | 8                                | \( H_1, H_2, H_1, H_2 \) | -8 |
| \( S_1, H_2, H_1, H_2 \) | 9                                | \( S_1, H_2, H_1, H_2 \) | -9 |
| \( H_1, H_2, H_1, H_2 \) | 10                               | \( H_2, H_1, H_1, H_2 \) | -10 |
| \( S_1, H_2, H_1, H_2 \) | 11                               | \( S_1, H_2, H_1, H_2 \) | -11 |
| \( H_1, H_2, H_1, H_2 \) | 12                               | \( H_2, H_1, H_1, H_2 \) | -12 |
| \( H_1, H_2, H_1, H_2 \) | 0                                | \( H_2, H_1, H_1, H_2 \) | 0 |

Figure 3. (a). quasi-sinusoidal voltage in Asymmetrical operation with respect to \( k = 2 \) and \( n = 2 \). (b). Experimental results quasi-sinusoidal voltage in symmetrical operation with respect to \( k = 2 \) and \( n = 2 \).
has been evaluated under both the symmetric and asymmetric operation and compared with the conventional and recently introduced symmetric and asymmetric structures. The relationships between switch numbers in CHB structure, proposed structure in [35, 36, 37]: and [38], and MLevel/NSource benchmark in symmetric status can be respectively given as follows:

\[
\frac{M_{\text{Level}}}{N_{\text{Source}}} | \text{CHB} = 2 + \frac{1}{4N_{\text{switch}}} \quad (16)
\]

\[
\frac{M_{\text{Level}}}{N_{\text{Source}}} | \text{[35]} = 2 \left(1 + \frac{1}{(N_{\text{switch}} - 2)}\right) \quad (17)
\]

\[
\frac{M_{\text{Level}}}{N_{\text{Source}}} | \text{[36]} = 2 \left(1 + \frac{1}{(N_{\text{switch}} - 4)}\right) \quad (18)
\]

\[
\frac{M_{\text{Level}}}{N_{\text{Source}}} | \text{[37]} = \frac{1}{3} + \frac{2}{N_{\text{switch}}} \quad (19)
\]

\[
\frac{M_{\text{Level}}}{N_{\text{Source}}} | \text{[38]} = 2 \left(1 + \frac{3}{(N_{\text{switch}} - 4)}\right) \quad (20)
\]

Also, the relationships between switch numbers in binary and trinary structures [37, 38, 39]: and [40], and MLevel/NSource benchmark in asymmetric status can be respectively given as follows:

\[
\frac{M_{\text{Level, asymmetric}}}{N_{\text{Source}} | \text{[Binary]} = \left(\frac{4}{N_{\text{Switch}}}\right) \left(\frac{N_{\text{switch}}}{2} + 1\right) + 1 \quad (21)
\]

\[
\frac{M_{\text{Level, asymmetric}}}{N_{\text{Source}} | \text{[Trinary]} = \left(\frac{4}{N_{\text{Switch}}}\right) \left(\frac{N_{\text{switch}}}{3} + 1\right) \quad (22)
\]

\[
\frac{M_{\text{Level, asymmetric}}}{N_{\text{Source}} | \text{[37]} = \left(\frac{2}{N_{\text{Switch}}}\right) \left(\frac{N_{\text{switch}}}{5} + 1\right) \quad (23)
\]

\[
\frac{M_{\text{Level, asymmetric}}}{N_{\text{Source}} | \text{[38]} = 3 + \frac{2}{N_{\text{switch}} - 4} \quad (24)
\]

\[
\frac{M_{\text{Level, asymmetric}}}{N_{\text{Source}} | \text{[39]} = \left(\frac{2}{N_{\text{Switch}}}\right) \left(\frac{N_{\text{switch}}}{2} - 3\right) - 1 \quad (25)
\]

\[
\frac{M_{\text{Level, asymmetric}}}{N_{\text{Source}} | \text{[40]} = \left(\frac{3n - 1}{N(N_{\text{Switch}} - 4)}\right) \left(2(n + 1) - \frac{2n - 4}{N_{\text{Switch}} - 4}\right) - 1 \quad (26)
\]

The variation of MLevel/NSource benchmark versus switch number varieties of suggested structure and others for symmetrical and asymmetrical statuses are depicted in Figure 4 (a) and (b).
The portrayed curves in Figure 4 (a) and (b) validate the high capability of suggested multilevel inverter aimed to create high-step quasi-sinusoidal voltage against the low embedded switches and DC power supplies. Furthermore, the number of required components for suggested multilevel inverter and others are presented in Table 3. As consequence, the significant problems related to multilevel inverters such as voltage quality, low THD, structure’s cost price have been attained.

3. Voltage quality improvement scheme based on harmonic elimination Pulse Width Modulation

3.1. Harmonic elimination principle

Increase of switches to unravel the voltage quality problem becomes paler because the multilevel inverter provides a quasi-sinusoidal voltage waveform with trivial THD. Toward this subject, voltage quality of the proposed structure has been improved taking into account of ten switches to earn three prominent criterions related voltage quality i.e., desired fundamental component, elimination of third harmonic and Reduction of THD. Hence, nine levels symmetric status of the suggested structure has been considered to better exhibit elimination and reduction of harmonic components.

As well, the created quasi-sinusoidal voltage waveform can be extended in Fourier series:

$$u_{out}(\alpha) = A_0 + \sum_{n=1}^{\infty} A_n \cos(n\alpha) + B_n \sin(n\alpha)$$ (27)

where,

$$A_0 = (2\pi)^{-1} \int_0^{2\pi} u_{out}(\alpha) \, d\alpha$$

$$A_n = (\pi)^{-1} \int_0^{2\pi} u_{out}(\alpha) \cos(n\alpha) \, d\alpha$$

$$B_n = (\pi)^{-1} \int_0^{2\pi} u_{out}(\alpha) \sin(n\alpha) \, d\alpha$$ (28)

Due to absence of the average value or DC component created by multilevel inverter $A_0 = 0$. According to the general quasi-sinusoidal waveform of multilevel inverter presented in Figure 5.a, due to being odd function along with quarter-wave symmetry, only sinusoidal part of Fourier series with presence of odd harmonics can be appeared:

$$u_{out}(\alpha) = \sum_{n=1,3,5,...} B_n \sin(n\alpha)$$ (29)

![Figure 5. (a). General quasi-sinusoidal voltage of cascaded multilevel inverter. (b). General scission-style harmonic elimination in quarter cycle waveform of cascaded multilevel inverter.](image-url)
3.2. PWM-based harmonic elimination strategy

Harmonic elimination strategies have been designed and formulated to
eliminate destructive harmonics from the quasi-sinusoidal voltage which is
recognized as a contractual approach among the scholars and scientists. It
has been essentially employed to decrease the THD from the output of inverter [41, 42]. Conventional HEPWM method i.e. non-scission HEPWM
triggering has some prominent disadvantages. The first, to eliminate or
reduce all the harmonics, a number of voltage levels must be produced by
multilevel inverter which required more switches. The second, as the
suggested symmetric inverter module has been triggered just twice in each
quarter cycle, the perfect performance of these switches (high frequency
switches) couldn’t be used. Toward this subject, the scission-style harmonic
elimination based on PWM that can modulate a number of angles within
specific level provides quasi-sinusoidal voltage waveform with several
scissions in each level as shown in Figure 5 (a). The significant feature of
“this strategy is eliminating further harmonics of low-step quasi-sinusoidal
voltage i.e. low switch numbers. Thus, scission-style harmonic elimination
owing to more triggering of switches in each quarter cycle, their performance
reach to fullest potential. Moreover, unequal DC power supplies can more
augment the performance of this approach aimed to reduce lower order harmonics. Anyhow, the optimization problem has been
formulated with various values of: DC power supplies, pulses width of
quasi-sinusoidal waveform and triggering angles in each level which can
be perceived with envisaging the Figure 5 (b).

Fourier series of steps quasi-sinusoidal voltage with non-equal dc
sources can be presented by (28):

Where, s is the number of DC power supplies, and the VsVsDC is amount of
the kth DC power supply. If all of DC power supplies have the equal
value therefore VsVs = ... = Vs = 1. Also, α1 ... αm are the triggering
transitions in the first level, αm1 ... αm2 are the triggering transitions in
the second level, and the same αm1−m2 ... +1 ... + αm1−m2+ms are the
triggering transitions in the last level. The solution set will be attained
by precisely extract the triggering angles of IGBTs’ gates toward enhance the
voltage quality of multilevel inverter. To apprise and con

4. Description of non-dominated sorting multi objective grey
wolf optimization & non-dominated Sorting Genetic Algorithm II

Due to multi-objective nature of the harmonic elimination strategy, the optimization problem has been formulated based on MOGWO to
precisely extract the triggering angles of IGBTs gates toward enhance the
voltage quality of multilevel inverter. To apprise and confirm this optimization
scheme, it has been compared with NSGA-II. Both the MOGWO and
NSGA-II have been described in following subsections.

4.1. Non-dominated sorting multi objective grey wolf optimization

4.1.1. Grey wolf optimization review

GWO is a novel and advanced swarm based optimization algorithm
inspired by imitating the headship hierarchy and hunting strategy of grey
wolves. The performance of GWO is demonstrated more suitable than
other prevalent optimization algorithm such as genetic algorithm and
particle swarm optimization [43]. Moreover, GWO is a high performance
optimization technique with respect to its fast convergence (due to its
search mechanism) and perceptible mathematical structure [44]. Better
and more precise, all wolves are divided into four groups according to
their fitness. GWO search mechanism has been conducted by the best
three wolves in any iteration. This mechanism upgrades the exploration
so that all engaged wolves to be attracted, then the best three wolves, as
a result of that the fast convergence will be obtained.

4.1.2. Multi-objective optimization

Multi-objective optimization is functionally constructed for solution of
a multi-dimensional problem. The optimization problem formulation
as a multi-objective minimization problem can be given by [45, 46]:
Minimize $F(\bar{x}) = f_1(\bar{x}), f_2(\bar{x}), \ldots, f_k(\bar{x})$ \hspace{1cm} (42)

Subject to:

\begin{align*}
g_i(\bar{x}) & \leq 0, \quad i = 1, 2, \ldots, m \\
I_i(\bar{x}) & = 0, \quad i = 1, 2, \ldots, p \\
L_i & \leq x_i \leq U_i, \quad i = 1, 2, \ldots, n
\end{align*} \hspace{1cm} (43)

Where $n$, $m$, $p$, and $N$ are respectively the number of variables, inequality constraints, equality constraints, and objective functions. $g_i$ and $I_i$ are respectively $i$-th inequality and equality constraints, and $[L_i U_i]$ indicates the $i$-th variable boundaries. Optimized single-objective results can simply be compared because of the unique objective function. Whereas, the extracted results from a multi-objective space may not be compared according to the relational operators because of multi-criteria objective functions. Hence, multi-objective problem has been unravelled compared according to the relational operators because of multi-criteria objective functions. Where $n$, $m$, $p$, and $N$ are respectively the number of variables, inequality constraints, equality constraints, and objective functions.

A set including the relevant objective contents in Pareto optimal set is named Pareto optimal front (surfaces) \cite{47}.

Statement 1. Pareto Dominance:
Assume the existence of two vectors such as: $\bar{x} = (x_1, x_2, \ldots, x_k)$ and $\bar{y} = (y_1, y_2, \ldots, y_k)$.

Vector $x$ dominates vector $y$ i.e., $x \succ y$ if:

\begin{align*}
&\forall i \in \{1, 2, \ldots, k\}; [f(x_i) \geq f(y_i) \land \exists \bar{y} \in [0,1]^k : f(x_i) = \bar{y}] \\
\text{Pareto front (surface) is stated by} \ [48]:
\end{align*} \hspace{1cm} (44)

Statement 2. Pareto Optimality:
A solution $\bar{x} \in \mathbf{X}$ is named Pareto optimal if:

\begin{align*}
\exists \bar{y} \in \mathbf{X} & | F(\bar{y}) > F(\bar{x}) \\
\text{The non-dominated solutions set is named Pareto optimal set which is stated by:}
\end{align*} \hspace{1cm} (45)

Statement 3. Pareto optimal set:
A Pareto-optimal solution set is named Pareto set by:

\begin{align*}
P_* = \{x, y \in \mathbf{X} | \exists \bar{y} \in \mathbf{X} : F(y) > F(x)\} \\
\text{A set including the relevant objective contents in Pareto optimal set is named Pareto optimal front (surface) which is stated by:}
\end{align*} \hspace{1cm} (46)

\begin{align*}
\text{Statement 4. Pareto optimal front (surface):}
\end{align*} \hspace{1cm} (47)

4.1.3. Grey wolf optimization

This algorithm is inspired by the gregarious headship and hunting strategy of grey wolves. The social hierarchy of wolves is mathematically designed with consideration of the best solution as $\alpha$ wolf. Also, the second and third appropriate solutions are respectively considered as $\beta$ and $\delta$ wolves. Wolves that have are considered as $\omega$ wolves. Based on GWO, hunting or optimization has been carried out using $\alpha$, $\beta$, and $\delta$, within the $\omega$ wolves have optimally pursued these three wolves.

As for the Figure 6, the siege strategy of grey wolves during the hunting can be presented by:

\begin{align*}
\vec{D} = |\vec{C} \cdot \bar{X}_p(t) - \bar{X}(t)| \\
\bar{X}(t+1) = \bar{X}_p(t) - \vec{A} \cdot \vec{D}
\end{align*} \hspace{1cm} (48, 49)

where, $t$, $\bar{X}_p$ and $\bar{X}$ are respectively the current generation, the hunt situation vector, and the grey wolf situation vector. $\vec{A}$ and $\vec{C}$ are coefficient vectors.

\begin{align*}
\vec{A} = 2 \vec{\alpha} r_1 - \vec{\alpha} \\
\vec{C} = 2 \vec{\beta} r_2
\end{align*} \hspace{1cm} (50, 51)

where, $\vec{\alpha}$ is linearly subsided from 2 to 0 through the increase of iterations and $r_1$ and $r_2$ indicate the random vectors in $[0,1]$. The first three best solutions are preserved which are attained yet, then other search operators considering the omegas are compelled to improve their situation according to them. The following equations have been continually performed for each search operator during the optimi-
The finding process is approved using $A^+$ with random values upper than 1 or lower than -1 that compels the search operator to split from the hunt. $C^+$ as accelerating factors in finding operations is randomly created in $[0, 2]$, where in random weights has been created for prey to stochastically strengthen ($C > 1$) or weaken ($C < 1$) to determine the distance using hunt quality. The $C$ parameter is being essentially created a random value to strengthen the finding mechanism through the iterations. It is important factor to avoid getting involved in the local optima minima, particularly in the latest iterations. $|A| < 1$ means that the optimization exploitation initiates, whereas $A^-$ is randomly created in $[-1, 1]$. Individuals are diverged from the hunt as $|A^-| > 1$ and converged towards the hunt as $|A^-| < 1$. The following situation is located in any situation between its current situation and the hunt situation that boost the search procedure to converge to figured situation of hunt generated by $\alpha$, $\beta$, and $\delta$ solutions. The situation and $\alpha$ solution are come back so that the best solutions to be attained and the satisfied end state to delivered. Finally, the concise computational sages for MOGWO, as flowchart form can be comprehended in Figure 7.

![Flowchart of multi-objective grey wolf optimization](image)

Figure 7. Flowchart of multi-objective grey wolf optimization.

4.2. Non-dominated Sorting Genetic Algorithm-II [49]

### 4.2.1. Non-dominated sorting

- For each individual (p) in main population perform:
  > Initialize $S_p = \emptyset$. This set encompasses all the individuals which are dominated by p.
  > Initialize $n_p = 0$. This is the number of individuals which dominate p.
  > for each individual q in P
    ✓ if p dominated q then:
      • add q to the $S_p$ i.e. $S_p = S_p \cup \{g\}$
      ✓ else if q dominates p then
      • increase the domination counter for p i.e. $n_p = n_p + 1$
    ✓ if $n_p = 0$ i.e. no individuals dominate p therefore p belonging to the first front; adjust the rank of individual p to one i.e $r_{\text{rank}} = 1$. Improve the first front set via addition of p to front one i.e $F_1 = F_1 \cup \{p\}$
  ❖ This is performed for all individuals in the main population.
  ❖ Initialize the front counter to one. $i = 1$
  ❖ Subsequent is performed when the $i$th front is non-blank i.e. $F_i = \emptyset$;
  > $Q = \emptyset$; the set of storing the individuals for $(i+1)$ th front.
  > for each individual $p$ in front $F_i$
    ✓ for each individual q in $S_p$ ($S_p$ is the set of individuals dominated by p)
      • $n_q = n_q + 1$, decrease the domination counter for individual q.
      • If $n_q = 0$ subsequently there is no individuals in the following fronts would dominate q. Therefore, set $r_{\text{rank}} = r_{\text{rank}} + 1$. Update the set Q with individual q i.e. $Q = Q \cup q$.
    ✓ Increase the front counter by one.
    > Now the set Q is the next front and subsequently $F_i = Q$.

4.2.2. Crowding distance

- For each front $F_i$, $n$ is the number of individuals.
  > For all the individuals, the initialized distance is zero i.e. $d_j = 0$, where $j$ correlates to the $j$th individual in front $F_i$.
  > for each objective function $m$
    ✓ Sort the individuals in front $F_i$ according to objective $m$ i.e. $I = \text{sort} (F_i, m)$.
    ✓ The boundary values for each individual is defined infinite $F_i$ i.e. $I(d_j) = \infty$ and $I(d_j) = \infty$
    ✓ for $k = 2$ to $(n-1)$:
    $I(d_j) = I(d_j) + \frac{I(k+1)m - I(k-1)m}{d_{m+1} - d_{m-1}}$ (59)

- $I(k), m$ is the value of the $m$th objective function related to the $k$th individual in I.

4.2.3. Genetic operators

4.2.3.1. Simulated binary crossover. Simulated binary crossover method is chosen which is presented as follows:

$$c_{i,k} = \frac{1}{2} [(1 - \beta_k)p_{i,k} + (1 + \beta_k)p_{i,k}]$$ (60)
where, $c_{i,k}$ is the $i$th child with $k$th part, $p_{i,k}$ is the chosen parent, and $\beta_k$ ($\geq 0$) is randomly created.

$$p(\beta) = \frac{1}{2} (\eta + 1) \beta^k, \quad 0 \leq \beta \leq 1$$

$$p(\beta) = \frac{1}{2} (\eta + 1)^{1/\beta} \beta^{k - 1}, \quad 1 < \beta$$

The distribution index $\eta_k$ can be acquired using a uniform sampled random number $u$ between (0, 1).

$$\beta(u) = (2u)^{1/(\eta + 1)}$$

$$\beta(u) = \frac{1}{2(1 - u)^{1/(\eta + 1)}}$$

**4.2.3.2. Polynomial mutation.** The polynomial mutation is used which is identified as follows:

$$c_i = p_i + (p_{i}^p - p_{i}^f) \delta_i$$

where, $p_i$ and $p_{i}^f$ are child and parent, respectively, also $p_{i}^p$ and $p_{i}^p$ are the lower and upper bounds on the parent components, respectively. $\delta_i$ is the small deviation which is defined as follows:

$$\delta_i = (2u)^{1/(\eta + 1)} - 1, \quad \text{if } r_i < 0.5$$

$$\delta_i = 1 - (2(1 - u)^{1/(\eta + 1)}), \quad \text{if } r_i \geq 0.5$$

where, $\eta_i$ is randomly chosen between (0, 1) and $\eta_{max}$ is mutation distribution index.

**4.2.4. Trade-off solution**

Choosing an appropriate trade-off solution from all non-inferior options depends on problem and determiner's distinction. Therefore, the ultimate solution will be revealed based on both the procedures of optimization and decision. For this study, a Fuzzy-based method is applied to choose the best tradeoff solution from the acquired Pareto set. The $j$th objective function of a solution in a Pareto set $f_j$ is defined by a membership function $\mu_j$:

$$\mu_j(x) = \begin{cases} 
1 & f_j \leq f_{j,max}^i \\
\frac{f_{j,max}^i - f_j}{f_{j,max}^i - f_{j,min}^i} & f_{j,min}^i \leq f_j \leq f_{j,max}^i \\
0 & f_j \geq f_{j,max}^i 
\end{cases}$$

where, $f_{j,min}^i$ and $f_{j,max}^i$ indicate the minimum and maximum values of the $j$th objective function, respectively. For each solution $i$, the membership function $\mu$ can be presented by:

$$\mu = \sum_{j=1}^{n} \mu_j$$

5. Scission-style harmonic elimination analysis and results

This approach has been designed to enhance the quality voltage of odd-nary AMLI. Owing to three prominent voltage quality criterions i.e., desired fundamental component, elimination of third harmonic and reduction of THD, the problem formulation has been constructed based on multi-objective algorithm. Toward this subject, MOGWO method is employed so that both the mentioned targets (minimum value of (36)–(38)) to be acquired. It is worth mentioning that, MOGWO based Harmonic Elimination not only figures out the triggering angles of scission points in each level, but also incorporates the non-equality of DC power supplies’ magnitude and also different pulse-widths. Hereof, the flexibility of this strategy has been heightened using three salient criterions aimed to more acquisition of voltage quality improvement. The quasi-sinusoidal voltage waveform and reference-carriers waveforms that are created according to the scission-style harmonic elimination scheme are presented in Figure 6(a) and (b), respectively. However, this strategy has been solved in accordance with three following schemes:

Due to heavy computational burden of this approach, aforesaid schemes have been severally carried out.

5.1. Scission-style harmonic elimination scheme considering different scissions

According to the relevant sequencing presented in (39), the search space of MOGWO is constricted for pre-defined area. Moreover, for scission-style harmonic elimination the angles should be accurately located between these levels. As can be seen in Figure 5(b) $m_1$, $m_2$ and $m_3$ indicate the number of angles which are available in the first, the second and the latest level, respectively. The angle propagation index has been set as triggering angles to define a set angle in each step of quasi-sinusoidal voltage. This index is presented by $m_1/m_2/.../m_3$ for example for angle propagation proportion of $6/4/7/5$, it has indicated that first, second, third and fourth levels encompass 6, 4, 7 and 5 angles, respectively.

Computational burden of scission-style harmonic elimination with presence of the angle propagation index and sequencing has been highly heightened. Also, the number of scission in each step acts as critical function to define the performance of this computation, and accordingly value of THD. Meantime, as the number of scissions (in each level) to be
increased, subsequently the value of fundamental component will decrease, and reversely. Thus, the maintenance of fundamental component is one of the prominent issues in this field. Due to destructive effects of third harmonic on normal operation of system, it must be considered as another function. That’s why MOGWO is engaged to obtain three aforementioned objective functions. The optimization problem has unravelled twenty four angles in each quarter cycle of quasi-sinusoidal waveform of proposed multilevel inverter. Also, the propagation proportion is taken to be 3/5/9/11 along with the modulation index (2.68 < M < 3.03). Following that the optimization processes, the Pareto solution surfaces of the optimization problem performed by MOGWO and NSGA-II are portrayed in Figure 9(a), and the trajectory curve of twenty eight triggering angle are depicted in and 9 (b). As can be seen, the optimization scheme based on MOGWO has provided more accurate and optimum result than NSGA-II. Also, the quasi-sinusoidal voltage and the relevant harmonic spectrum are presented in Figures 10 (a) and (b). As consequence, the performance of scission-style harmonic elimination aimed at reduction of the THD, elimination of third harmonic and maintenance of fundamental component (1.7p.u.) is proved.

5.2. Scission-style harmonic elimination scheme considering non-equal DC power supplies

In accordance with the sequence of (40), the constraint of non-equality of DC power supplies is assigned. Same the previous section, the MOGWO has optimized the magnitude of DC power supplies in order to minimize three defined objective functions. Excluding the effects of triggering angle to carry out the Harmonic Elimination, variety of the DC power sources' magnitude can be considered as an important criterion for optimization problem. The quasi-sinusoidal voltage and its harmonic spectrum related to the optimum solution are presented in Figure 11 (a) and (b), respectively. Furthermore, their relevant experimental results are presented in Figure 11 (c) and (d). These figure have clearly shown that third objective-functions have been well-reduced and also fundamental component is held on pre-defined value1.9 p.u.

5.3. Scission-style harmonic elimination scheme considering different pulse-width values

In this part, the width of all pulses of quasi-sinusoidal waveform is optimized by MOGWO so that three objective functions to be minimized.
Figure 11. (a). Simulation result of quasi-sinusoidal voltage. (b). Simulation FFT of quasi-sinusoidal voltage. (c). Experimental result of quasi-sinusoidal voltage. (d). Experimental FFT of quasi-sinusoidal voltage.

Figure 12. (a). Simulation result of quasi-sinusoidal voltage. (b). Simulation FFT of quasi-sinusoidal voltage. (c). Experimental result of quasi-sinusoidal voltage. (d). Experimental FFT of quasi-sinusoidal voltage.
The performance of this item in the form of output voltage of inverter and harmonic spectrum are respectively shown in Figure 12 (a) and (b). Furthermore, their relevant experimental results are presented in in Figure 12 (c) and (d). These figures have confirmed that, what accuracy of acquired results from two previous parts is also repeated for this analysis. The difference here is that: the magnitude of fundamental component in considered to be 1.8 dB.

6. Conclusion

An innovational cascaded AMLI has been designed and analyzed so that a high-step quasi-sinusoidal voltage with low harmonic components to be acquired. To validate the suggested AMLI capability, it has been thoroughly evaluated and compared with the conventional and recently introduced symmetric and asymmetric multilevel inverters. Sub-AMLK has been designed using the ladder capacitors of clamped to the H-bridge by several bi-directional switches. A creative geometric progression has been designed using the ladder capacitors of clamped to the H-bridge by several bi-directional switches. A creative geometric progression has been designed using

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Additional information

No additional information is available for this paper.

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