On Detecting Delay Faults Using Time-to-Digital Converter Embedded in Boundary Scan

Hiroyuki YOTSUYANAGI†, Member, Hiroyuki MAKIMOTO†∗, Nonmember, Takanobu NIMIYA†, Student Member, and Masaki HASHIZUME†, Member

SUMMARY This paper proposes a method for testing delay faults using a boundary scan circuit in which a time-to-digital converter (TDC) is embedded. The incoming transitions from the other cores or chips are captured at the boundary scan circuit. The TDC circuit is modified to set the initial value for a delay line through which the transition is propagated. The condition for measuring timing slacks of two or more paths is also investigated since the overlap of the signals may occur in the delay line of the TDC in our boundary scan circuit. An experimental IC with the TDC and boundary scan is fabricated and is measured to estimate the delay of some paths measured by the TDC embedded in boundary scan cells. The simulation results for a benchmark circuit with the boundary scan circuit are also shown for the case that timing slacks of multiple paths can be observed even if the signals overlap in the TDC.

key words: delay testing, time-to-digital converter, boundary scan, design for testability

1. Introduction

Testing delay faults caused by defects like opens and shorts is more important to ensure test quality in recent deep sub-micron (DSM) designs. Especially small delay defects are hard to be detected since they cannot be detected unless the fault is propagated through a critical path [1], [2]. Test pattern must be generated such that the fault effects can be propagated through the path as long as possible. However, it is difficult to make such test patterns for every target faults. Small delay defects may escape if the critical path is not used in test pattern generation.

Faster-than-at-speed testing has also been used for detecting small delay defects [3]–[7]. In these methods, circuits are tested using multiple clock frequencies that are higher than the normal clock. Some other methods have been proposed to use the embedded sensors for measuring the circuit delay [8], [9]. Time-to-digital converters are also utilized for measuring the circuit delay or clock jitter [10]–[13].

We have proposed the boundary scan circuit in which a time-to-digital converter can be embedded for estimating the delay of an incoming transition [14], [15]. In our method, incoming transitions from the other cores or chips is delayed by some gates. Then the delayed transition is captured at the boundary scan cells. Using an embedded TDC, how fast the transition signal reaches to the observed output can be estimated without applying variable test clock frequency. Even if test clock is not so fast, the method can observe a transition signal at several different timing delayed by delay gates hence we can obtain the same results as faster-than-at-speed testing. In this paper, the modified TDC in the boundary scan circuit is proposed. A control signal is added for two purposes: One is to provide the initial logic value for a delay line. The other is to measure the delay of XOR gates in the delay line.

We also evaluate the capability of testing delay in multiple paths using our boundary scan design. When two or more transitions are measured using the boundary scan circuit, there may occur overlap between the signals. First we show the results of measuring the transitions obtained for the experimental chips to estimate the variability of the delay among ICs. The conditions for selecting multiple paths to be propagated into the delay line in the TDC are considered based on the expected timing slacks for each path.

The rest of this paper is organized as follows: In Sect. 2, a circuit for detecting delay between cores using a time-to-digital converter is presented. Section 3 describes the proposed boundary scan architecture in which a time-to-digital converter is embedded. Section 4 shows some results obtained for experimental chips. The condition to select two or more paths for testing delay faults is discussed in Sect. 5. Section 6 shows some simulation results for testing multiple paths using TDCBS. Section 7 concludes the paper.

2. Delay Detection Using Scan Cells with Time-to-Digital Converter

A time-to-digital converter has been used for measuring delay and clock jitter [10]–[13]. We have designed a boundary scan cell that has a capability to test the delay of incoming transitions from another core or chip [14]. The boundary scan cells can form a time-to-digital converter that is utilized for detecting delay.

Figure 1 shows new TDC circuit used in our design for detecting delay from outside of a core.

THRSWSCOT block consists of a shift register to provides control signal CONT[i] for selecting a transition at i-th input to be observed. The selected input signal is propagated into the delay line that consists of XOR and AND gates. The incoming transitions are delayed by these gates and captured at the flip-flops.

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This TDC circuit is modified from that of [14], [15]. In the previous design, the initial logic value at the output of each XOR gate can be set only to 0. When observing a rising transition, it is easy to find which input is observed from the captured responses since the captured value at the flip-flop \( FF_i \) differs from \( FF_{i-1} \), (i.e. \( FF_i = 1 \) and \( FF_{i-1} = 0 \)). Although which input is targeted to be observed is obvious, it is easier to make the difference between the captured value at \( FF_i \) and \( FF_{i-1} \). In the new design, CNTHL signal is added for providing an initial logic value for the delay line before observing an incoming transition. By setting all CONT\[i\] to 0 and LOOPCNT = 1, the logic value at the outputs of all XOR gates on the delay line can be set to CNTHL. When a transition from H to L is fed from Core A, CNTHL is set to H. If the captured value of a flip-flop differs from the initial value, the transition reached at the flip-flop before the clock cycle.

The delay in the incoming transition can be detected by the following procedure.

1. Initial logic value for the delay line is provided from CNTHL by setting LOOPCNT = 1 and all CONT\[i\] = 0.
2. Control signals are provided from THRUSWCONT block to select the target input and to configure a ring delay line.
3. Test pattern for making a transition is applied for Core A.
4. The delayed responses are captured at flip-flops. After that, SCANEN is set to 1 to make a scan chain.
5. The captured responses are observed through the scan chain by scan shift operation.

If two pattern tests are provided to Core A using scan-based approach widely used in at-speed testing, no extra test application time is required for our method when one transition is observed for each two pattern test by the TDC circuit. We can apply the initial logic value for the delay line and selection signal for THRUSWCONT at Step 1 and 2 in the above procedure during the scan shift required for providing the initial pattern of the two pattern test for Core A.

Figure 2 shows an timing diagram for measuring timing slack using the TDC circuit. The captured responses can be observed through the SCANOUT terminal. This example assumes a case that a transition from L to H through OUTA[1] in Fig. 1 is observed by setting CONT[1] = 1 and CONT[j] = 0 (\( j \neq 1 \)). The logic waveform at OUTA[1] can be observed through the scan chain. If there exists some glitches, logic value observed at SCANOUT may frequently changes as shown in the period between \( N_{U} \) and \( S_{in} \). The stable output is captured in the period between \( S_{in} \) and \( S_{out} \). The value observed at time \( S_{in} \) is the captured value of the flip-flop \( FF_i \) for which the incoming transition is connected. \( N_{max} \) is the number of XOR gates such that the delay of the XOR chain with \( N_{max} \) gates is same as the clock cycle.

The timing slack can be estimated by counting the number of scan shifts between time \( S_{in} \) and \( S_{out} \) shown in the figure. The transition from L to H is captured at the flip-flop corresponding to \( S_{t} \). Since an incoming signal may contain glitches, the captured value from \( N_{U} \) to \( S_{t} \) is not used for testing. The flip-flops between \( S_{t} \) and \( S_{in} \) capture the signal after the transition finished. The timing slack \( T_{slack} \) can be estimated as follows:

\[
T_{slack} = N_{slack} \times t_d
\]

where \( N_{slack} \) is the number of clocks between time \( S_{t} \) and \( S_{in} \), and \( t_d \) is the delay of an XOR gate in the delay line.

In the new design in Fig. 1, we can estimate \( t_d \) by observing \( N_{max} \) using CNTHL signal. \( N_{max} \) can be obtained by applying a clock pulse from CNTHL with setting CONT = 0 and LOOPCNT = 1, and by counting how much XOR gates output 1 or 0 when capturing the pulse by the TDC. The delay of a gate is estimated by \( t_g = T_{clock}/N_{max} \).

3. Modified Boundary Scan Cell to Embed a Time-to-Digital Converter

In our testable design, a boundary scan cell is modified such
that the cells can form a TDC that is utilized for detecting delay [14], [15].

Figure 3 shows a basic boundary scan cell [16]. In our testable design, the first flip-flop (capture register [16]) in a boundary scan cell is also utilized to form a TDC. Figure 4 shows new boundary scan cell called TDCBS cell. By setting TDCMode = 0, the TDCBS cell can be used as the boundary scan cell shown in Fig. 3. By setting TDCMode = 1, TDCBS cells can form a TDC shown in Fig. 1. We can embed a TDC into boundary scan design by adding an AND gate, an XOR gate, and MUX to the basic boundary scan cell.

To implement a TDC using TDCBS cells, THRUOUT and THRUIN terminals of neighboring cells are connected as shown in Fig. 5. To give additional delay enough to detect a transition even if an input is connected to the last stage of the delay line, the delay line is designed to be able to make a loop.

In this example, extra delay cells are added in a delay line. When the number of boundary scan cells for the original circuit is small, it is easier to observe the transition by adding extra delay cells to avoid the incoming transition to propagate around the ring delay line [15]. Since extra delay cells are used only for detecting delay, it consists of an XOR gate and a scan flip-flop only. It is also possible to avoid the transition to propagate around the ring delay line by replacing XOR gates in a delay line with gates that have larger gate delay. The number of XOR gates required for a delay line is estimated by dividing timing slack of the targeted paths by the gate delay of an XOR gate.

The area overhead of the testable design with TDCBS cells compared to the conventional boundary scan method is estimated by the following. For each boundary scan cell, an AND gate, a MUX gate and an XOR gate are added in our method. The controller block THRUSWCONT is also needed to select incoming signals to be observed. In this paper, we use a shift register as THRUSWCONT that requires k flip-flops. A decoder can also be utilized for the THRUSWCONT block.

4. Preliminary Experiment

To estimate the feasibility of our TDCBS cells for delay testing, an experimental chip including the circuit shown in Fig. 6 was designed and fabricated in 0.18 µm CMOS technology. Since this design is based on our previous TDCBS circuit in [14], CNTTHL signal is not included. The part of the chip layout is shown in Fig. 7.

The cs208 circuit, which is the combinational part of ISCAS89 benchmark circuit s208, is used as CUT#1 in Core A. Any two pattern inputs can be provided to CUT#1 by scan input part in Core A that contains a scan chain. Core B consists of TDCBS cells and THRUSWCONT block. We use a shift register as the THRUSWCONT block. The delay at an XOR gate used in a TDCBS cell is about 0.1 nsec. To observe the output waveform from CUT#1, extra delay cells are added after the scan chain in the TDCBS cells to form a long delay line. CUT#2 is designed for verifying the outputs of the TDCBS cells in Core B. It consists of scan...
flip-flops that captures the output of TDCBS cells (output OUT in Fig. 4).

In our preliminary experiment, the input transitions from the first and from the fifth input of Core B are measured using a TDC configured by TDCBS cells. Figure 8 shows the results obtained by both simulation and by measuring the experimental chips. First, control signals CONTCLK, CONTEN, CONTIN are applied to the THRUSWCONT block to select which input of Core B is measured. EN1 and IN1 are input signals for Core A and are used for providing rising transition for Core B. The signal from Core A to Core B through the selected TDCBS cell is propagated into the delay line by applying CONTEN = 1 and then is captured at the flip-flops. The captured response can be observed through the scan chain by applying Shift_DR = 1.

The captured responses obtained by the circuit simulation and by measuring 10 experimental chips are shown in the figure. Figure 8(a) and 8(b) show the results when the incoming transitions are observed through the first input and the fifth input, respectively.

The difference of \( N_{\text{slack}} \) between the results obtained for the first input and the fifth input, denoted as \( \Delta N_{\text{slack1}} \), is shown for each chip in the right side of Fig. 8(b). Although the number of scan shifts until the transition is detected differs from the chips, the difference between the delay observed for first and fifth inputs are almost the same for all chips. Since the difference in delay is only four to five scan shifts for every chips. If a delay fault that exceeds much more than \( 5 \times t_d \) is excited for one of the test pattern, it can be detected using the TDC. Although this experimental chip does not include CNTHL signal, the CNTHL signal in the new design can be utilized as the reference to calculate the difference in delay measurement. As described in Sect. 2, the gate delay occurred in a TDCBS cell can be estimated using CNTHL in the new design when comparing the gate delay in the different chips.

5. Delay Estimation of Multiple Paths

Here we describe the conditions of paths that can be tested at the same test pattern.

To estimate timing slack of the signal, the two timing \( S_{\text{in}} \) and \( S_t \) shown in Fig. 2 must be identified by observing scan output. The former can be easily identified by which incoming transition is selected using THRUSWCONT. However, the latter may not be identified when two or more incoming transitions are provided into the delay line. For example, the two rising transition signals from input \( I_1 \) and \( I_2 \) are propagated into the delay line. Let assume that input \( I_1 \) is connected to the input side of the delay line and \( N_{12} \) TDCBS cells exists between these inputs.

When these signals overlap in the delay line before capturing the response to the flip-flops, the transition from \( I_1 \) is flipped at an XOR gate in the TDCBS cell connected to \( I_2 \).

Figure 9 shows the timing diagrams for the cases that (a) the transitions propagated in the delay line do not interefere each other, (b) the transitions overlap in the delay line but timing slack can be estimated for both transitions, and (c) the transitions overlap in the delay line and timing slack cannot be observed due to unstable part of the transitions caused by glitches.

\( N_{\text{max}} \) is the number of flip-flops required for observing the whole transition during a clock period. \( N_{\text{max}} \) can be calculated by \( N_{\text{max}} = T_{\text{clk}}/t_d \). \( N_{\text{slack1}}, N_{\text{slack2}} \) are the number of XOR gates through which the incoming signal propagates within the timing slack of the transition from \( I_1 \) and from \( I_2 \), respectively.

If \( N_{12} > N_{\text{max}} \) holds, the capture clock reaches before the signals overlap in the delay line. Hence the observed output pattern is like in Fig. 9(a). In this case, time \( S_{\text{in1}} \) can be detected by observing the first transition after \( S_{\text{in1}} \). Time \( S_{\text{in2}} \) can also be detected by observing the first transi-
tion after $S_{in2}$. Since time $S_{in1}$ and $S_{in2}$ can be observed, both $N_{slack1}$ and $N_{slack2}$ can be measured using TDCBS. A circuit is identified as faulty when measured slack is less than the given limit for the target path.

If $N_{slack2} < N_{max} - N_{12}$, whether the timing slack can be measured or not depends on an expected timing slack $N_{slack2}$. Figure 9 (b) shows the case that the timing slack can be measured. Figure 9 (b-1) and (b-2) show the timing diagrams of the scan outputs for the case that only one of the inputs $I_1$ or $I_2$ is connected to the delay line and is observed separately. If these two inputs are connected to a delay line at the same time, the transition signals overlap during the period between $S_{in2}$ and $(S_{in1} + N_{max})$. The signal from $I_2$ is inverted by the XOR gate in the TDCBS cell connected to $I_1$ since $I_1$ is the side input of the XOR gate and is set to H. If $N_{slack2} > (N_{max} - N_{12})$, the expected value between $N_{in2}$ and $S_{in1}$, which is 0 in this case, can be calculated since both signal from $I_1$ and $I_2$ should be stable if no delay fault exist. Hence time $S_{in1}$ can be detected by observing the first transition after $S_{in2}$. Time $S_{in2}$ can also be detected by observing the first transition after $S_{in1} + N_{max}$. Since $S_{in1}, S_{in2}, N_{max}$ is known, we can measure the timing slack although the signal is inverted at the overlapping period.

Figure 9 (c) shows a timing diagram of the scan output when $N_{slack2} < (N_{max} - N_{12})$. Figure 9 (c-1) and (c-2)
show timing diagrams of the scan output when $I_1$ and $I_2$ are observed separately. In this case, since $S_{t1}$ overlaps the unstable transition period in (c-2), the timing slack for the signal from $I_1$ cannot be measured if $I_1$ and $I_2$ are observed through a delay line at the same time. Although $N_{slack1}$ cannot be measured in this case, a delay fault may be detected if it causes delay such that the last transition in (c-1) or (c-2) appears in the period between $S_{in1}$ and $S_{in2}$. In this case, $I_1$ and $I_2$ should be observed separately by applying the test pattern twice.

In case that the observed transitions include both rising and falling transitions, it should be noted that the difference between the rising delay and the falling delay at the output of a delay gate may affect the condition of detecting delay in multiple paths. Since $N_{max}$ is given by $T_{clk}/t_d$, $N_{max}$ depends on the delay of the XOR gate used in the TDC. The falling delay at an XOR gate is about 20% faster than the rising delay in the delay parameters given in the library used in our Verilog simulation. However, there is not so much difference in the actual gate delay when we measured the rising delay and the falling delay at XOR gates in the other experimental chips.

6. Simulation Results

To estimate the conditions of testing multiple paths using our TDCBS cells, we applied simulation for an example circuit in Fig. 10. In this simulation, the combinational part of ISCAS89 benchmark circuit s5378 (denoted as cs5378) is used as CUT#1 in Core A in Fig. 6 that has 228 outputs. Since there exists enough number of TDCBS cells, a delay additional part is not included in Core B.

We synthesize the circuit using Synopsys Design Compiler with Rohm 0.18 µm CMOS library. The gate delay of an XOR gate is about 0.08 nsec. The clock period is set to 8 nsec. Therefore, $N_{max} = 100$.

Figure 11 shows an example timing diagram obtained when two outputs of cs5378 are propagated into the delay

![Fig. 11](image_url)

The simulation results for testing two paths using condition (a).

![Fig. 12](image_url)

The simulation results for testing four paths using condition (b).
line at the same time. The two inputs were selected such that condition (a) in Sect. 5 is satisfied (N_{12} = 114). The rising transition at both inputs can be observed through scan chain in TDCBS cells. One of the transitions was propagated through the delay loop and was observed at the first and the last parts of the scan output.

Figure 12 shows an example timing diagram obtained when four outputs satisfy the condition (b) in Sect. 5 and are propagated into the delay line at the same time (N_{12} = N_{23} = N_{34} = 57). The four timing diagrams for each input are also shown in Fig. 12. Please note that the rising transitions from I_1 and I_4 are propagated through the loop in the delay line. The results of the timing slack for each transition observed at the SCANOUT output are N_{slack k1} = 79, N_{slack k2} = 80, N_{slack k3} = N_{slack k4} = N_{slack k5} = 81, N_{slack k6} = N_{slack k7} + N_{slack k8} = 81.

The measured timing slack is slightly different from that obtained when the transition is measured separately since the propagation delay in XOR gates used in our simulation differs between rising and falling transitions. The threshold of timing slack used in delay testing should be set in consideration of delay elements.

7. Conclusion

In this paper, delay testing using the boundary scan cells that can form a time-to-digital converter is discussed. From circuit simulation and the results obtained for experimental chips, the conditions to measure timing slacks for two or more paths are shown. The simulation results are also shown for each condition to prove the feasibility of testing multiple paths using our TDCBS circuit. It is expected that even if a critical path is hard to be tested, its partial path can be tested when the other critical path is tested if the pattern satisfies the condition discussed in Sec. 5. The test pattern generation for detecting delay faults for hard-to-detect paths using the TDCBS design is left as the future work.

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References

[1] Y. Sato, S. Hamada, T. Maeda, A. Takatori, Y. Nozuyama, and S. Kajihara, “Invisible delay quality - SDQM model lights up what could not be seen,” Test Conference, International, Paper 47.1, 2005.
[2] P.J. Chen, W.L. Hsu, J.C.M. Li, N.H. Tseng, K.Y. Chen, W.P. Changchien, and C.C. Liu, “An accurate timing-aware diagnosis algorithm for multiple small delay defects,” Asian Test Symposium, pp.291–296, 2011.
[3] H. Yan and A.D. Singh, “A delay test to differentiate resistive interconnect faults from weak transistor defects,” International Conference on VLSI Design, pp.47–52, 2005.
[4] N. Ahmed and M. Tehranipoor, “A novel faster-than-at-speed transition-delay test method considering IR-drop effects,” IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol.28, no.10, pp.1573–1582, Oct. 2009.
[5] B. Kruseman, A.K. Majhi, G. Gronthoud, and S. Eichenberger, “On hazard-free patterns for fine-delay fault testing,” Test Conference, International, pp.213–222, 2004.
[6] H. Yan and A. Singh, “On the effectiveness of detecting small delay defects in the slack interval,” Current and Defect Based Testing, 2004. DBT 2004. Proceedings. 2004 IEEE International Workshop on, pp.49–53, April 2004.
[7] N. Ahmed, M. Tehranipoor, and V. Jayaram, “A novel framework for faster-than-at-speed delay test considering IR-drop effects,” International Conference on Computer-Aided Design, pp.198–203, 2006.
[8] S. Ghosh, S. Bhunia, A. Raychowdhury, and K. Roy, “A novel delay fault testing methodology using low-overhead built-in delay sensor,” IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol.25, no.12, pp.2934–2943, Dec. 2006.
[9] X. Wang, M. Tehranipoor, and R. Datta, “A novel architecture for on-chip path delay measurement,” Proc. International Test Conf., 2009.
[10] J. Yu and F.F. Dai, “On-chip jitter measurement using vernier ring-time to-digital converter,” Asian Test Symposium, pp.167–170, 2010.
[11] K. Katoh, K. Namba, and H. Ito, “A low area on-chip delay measurement system using embedded delay measurement circuit,” Asian Test Symposium, pp.343–348, 2010.
[12] M.C. Tsai, C.H. Cheng, and C.M. Yang, “An all-digital highprecision built-in delay time measurement circuit,” Asian Test Symposium, pp.249–254, 2008.
[13] R. Datta, A. Sebastine, A. Raghunathan, G. Carpenter, K. Nowka, and J. Abraham, “On-chip delay measurement based response analysis for timing characterization,” J. Electronic Testing, vol.26, pp.599–619, 2010.
[14] H. Yotsuyanagi, H. Makimoto, and M. Hashizume, “A boundary scan circuit with time-to-digital converter for delay testing,” Asian Test Symposium, pp.539–544, 2011.
[15] H. Makimoto, H. Yotsuyanagi, and M. Hashizume, “On measuring timing slack using boundary scan with time-to-digital converter for detecting delay faults,” Proc. 2012 RISP International Workshop on Nonlinear Circuits, Communications and Signal Processing, pp.445–448, 2012.
[16] K.P. Parker, The Boundary Scan Handbook, Kluwer Academic Publishers, 2003.

Hiroyuki Yotsuyanagi received his B.E., M.E. and Ph.D. degrees from Osaka University, in 1993, 1995 and 1998, respectively. He is currently an Associate Professor of the Department of Information Solution, Institute of Technology and Science, the University of Tokushima. His research interest includes defect based testing of CMOS ICs and DFT for sequential circuits. He is a member of the IEEE.
Hiroyuki Makimoto received his B.E. and M.E. degrees in electrical engineering from the Univ. of Tokushima, in 2011 and 2013, respectively. He is currently with ROHM Co., Ltd. His research interests include delay fault testing.

Takanobu Nimiya received his B.E. degree in electrical engineering from the Univ. of Tokushima, in 2012. He is currently working towards his M.E. degree. His research interests include design for testability.

Masaki Hashizume received his B.E. and M.E. degrees in electrical engineering from the Univ. of Tokushima and Dr.E. degree from Kyoto Univ., in 1978, 1980 and 1993, respectively. He is currently a Professor of the Department of Information Solution, Institute of Technology and Science, the University of Tokushima. His research interests include supply current testing of logic circuits.