**FPGA Applied in Hardware Computer Aided Design of Gigabit Ethernet Data Acquisition System**

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**Abstract.** With the increasing popularity of the network, Ethernet has been widely used because of its wide distribution and convenient access. At the same time, due to the continuous innovation of Ethernet technology and the continuous development of new functions, it has gradually become the most popular network technology in the world. Gigabit Ethernet is a technology based on the Ethernet standard, and has become the mainstream because of its high efficiency, high speed and high performance Network technology. This paper presents a hardware design scheme of Gigabit Ethernet data acquisition system based on FPGA, including power module, clock module, FPGA main controller module, 88e1111 Ethernet module, which realizes data acquisition and transmission. The system is miniaturized, low-cost and portable.

**Keywords:** Gigabit Ethernet, data acquisition, miniaturization, low cost

1. **Introduction**

As a basic LAN technology, Ethernet brings great convenience to people's life. With the rapid development of computer and network, the demand of application is also increasing. The traditional Ethernet technology has been unable to meet people's needs, so along with various needs, Ethernet (10mbit/s) or fast Ethernet (100mbit/s) or Gigabit Ethernet (1000mbit/s) or 10 Gigabit Ethernet have appeared successively [1] [2]. Ethernet is out of many network technologies because of its own technical advantages [3] [4]. It has become the most promising network technology. Gigabit Ethernet is a technology based on the Ethernet standard. It is fully compatible with the widely used Ethernet and fast Ethernet [5]. With its high efficiency, high speed and high performance, it is widely used in finance, commerce, education, government agencies, factories and mining enterprises, and has become the mainstream network technology.

2. **All system**

The provide a hardware architecture that based FPGA and 88E1111 Ethernet module with fast real-time performance, more quickly processing speed, little size and small power consumption.

This hardware architecture of the structure is given in Figure 1, which collects and sends data through Gigabit Ethernet.
The external data source transmits the data to the FPGA main control module through RS422 interface. The RS422 interface selects the synchronous 422 interface ds26lv32 of TI Company to receive the data. The IC of DS26LV32A is a fast quickly quad differential CMOS receiver that cater the need of both TIA/EIA-422-B and ITU-T V.11. The CMOS ds26lv31 functions typical only static ICC of 9mA which makes it perfect for battery powered and supply for conscious applications. Select ds26lv31 to send data.

This hardware architecture of the important control module consists of an controller (FPGA), the power change module and a clock produce module. The controller of FPGA main uses Xilinx company artix-7 series xc7a200t-2fbg484i as the first processor chip; other 128MB nor flash, using configuring it to SPI mode, the use of logic circuit can be written in the NOR flash and when the system begin to wore, the software start from NOR flash.

This hardware architecture of Gigabit Ethernet includes PHY chip, which is implemented by 88e1111 chip of Marvell Company. 88e1111 is an integrated 10/100/1000mbit / s Ethernet transceiver. There are four physical layer interface standards: GMII (Gigabit media independent interface), RGMII (reduced gmii), TBI (ten bit interface) and RTBI (reduced TBI). GMII is a standard Gigabit Ethernet interface, which is located between MAC layer and physical layer; for TBI interface, the function of PCs sub layer will be realized by MAC layer chip, which reduces the complexity of phy chip and has less control lines than gmii interface. Both rmgii and rtbi can double the transmission rate of each data line and reduce the number of data lines by half.

3. System hardware design

3.1. RS422 interface
The RS422 interface of receiving data adopts ds26lv32 chip of Ti, and the circuit design is shown in Figure 2, which is higher than 400Mbps conversion rate.
3.2. Main control module
The FPGA of Xilinx series xc7a200t-2fbg484i FPGA is making the important processor chip, including 215360 logic cells, block ram, blocks13, FPGA is used for data acquisition, transmission and Gigabit Ethernet data control; FPGA as processor is connected with 128MB nor flash. Through SPI mode, the application logic circuit can be written in NOR flash to realize automatic startup from NOR flash when power on;

3.3. Power module
FPGA and its peripheral circuits need voltage of 3.3V or 2.5V or 1.8V or 1.2V. In order to fully test the power consumption of the platform and improve the efficiency of the power conversion unit, the
FPGA power supply is implemented by ltm4644 of Lingte Company. The input voltage range of ltm4644 is 4V~14V, and the output voltage range is 0.6 ~ 5.5V. The ltm4644 has four outputs, each of which has a current of up to 4A and a peak value of 5A. The rated working temperature of ltm4644 is -40℃~125℃. The 3.3V, 2.5V, 1.8V and 1.2V are all produced by LT Company DC-DC power chip LTM4644. The power conversion design is shown in Figure 4.

**Figure 4.** System power supply design.

### 3.4. Gigabit Ethernet Hardware Interface Design

PHY chip is implemented by 88E1111 chip. The RGMII interface between PHY chip and FPGA is designed to realize data communication, which will reduce the number of PCB wires on the circuit board and facilitate the development of the circuit board.

**Figure 5.** Interface relationship between FPGA and Phy.

It can be seen from Figure 5 that FPGA and 88e1111 communicate with each other through the rgmii interface. At the same time, during the power on initialization stage, FPGA will actively generate reset signal to reset 88e1111.
The design circuit diagram of Gigabit Ethernet Hardware is shown in Figure 6:

Figure 6. Gigabit Ethernet Hardware design circuit.

Figure 7. RJ45 interface circuit design
4. Experimental results

The network of OmniPeek packet capture software is used in the experimental test, as shown in Figure 8. The hardware system of Gigabit Ethernet data acquisition system based on FPGA is tested and the loss rate of packet and repetition rate of Gigabit Ethernet are tested.

The data size of each packet is 1088 bytes, containing frame header of 60 byte, 1024 byte real data and 4-byte CRC check bit. The figure 9 shows the data content of each packet. ① is the 4-byte packet count, which can count the loss rate of packet. ② is the channel number. If two packets of data with the same count of packet and number of channel are received, they are duplicate packets. After the repeatability test, the loss rate of packet is 0%, and the rate of repetition is 0%. It shows that this hardware design has stability and reliability.
5. Conclusions

The hardware design of Gigabit Ethernet data acquisition system based on FPGA takes FPGA as this main control module of this system and 88e1111 as this receiving and sending module of Ethernet port. It is miniaturized, low-cost and portable. OmniPeek network packet capture tool test, data transmission with stability and reliability.

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