Design of SEC-DED and SEC-DED-DAEC Codes of different lengths

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Abstract. Reliability is an important requirement for both communication and storage systems. Due to continuous scale down of technology multiple adjacent bits error probability increases. The data may be corrupted due to soft errors. Error correction codes are used to detect and correct the errors. In this paper, design of single error correction-double error detection (SEC-DED) and single error correction-double error detection-double adjacent error correction (SEC-DED-DAEC) codes of different data lengths have been proposed. Proposed SEC-DED and SEC-DED-DAEC codes require lower delay and power compared to existing coding schemes. Area complexity in terms of logic gates of proposed and existing codes have been presented. ASIC-based synthesis results show a notable reduction compared to existing SEC-DED codes. All the codec architectures are synthesized on ASIC platform. Performances of different SEC-DED-DAEC codes are tabulated in terms of area, power and delay.

keywords: Error correction codes (ECC), Soft errors, SEC-DED, SEC-DED-DAEC, ASIC

1 Introduction

Nowadays, consumer demand for more functionalities, low power consumption and compact systems. Memory is an important part of many electronics gadgets. The major concern for memories is soft errors which are caused by radiation [1], [2]. These soft errors corrupt the digital data and multiple bit upsets (MBUs) have occurred. So to impart more reliability to these systems, errors must be detected and corrected. Several error detecting and correcting codes are already available. Many adjacent error correcting codes [3], [4], [5] and CA-based error detecting and correcting codes [6], [7], [8] have already been introduced to detect and correct adjacent errors in communication and storage systems. Alternatively, Bose-Chaudhuri-Hocquenghem (BCH) code [9] and Reed Solomon (RS) code [10], [11] can protect MBUs.

Cha and Yoon proposed a technique to design an ECC processing circuits for SEC-DED code in memories. The area complexity of the ECC processing circuits have been minimized in [12]. Adalid et al. presented a SEC-DED code for
short data words which can detect the double bit errors and correct single error \cite{13, 14}. Alabady et al. proposed a coding technique to detect and correct single and multiple bit errors in \cite{15, 16, 17}. The algorithms, flowchart, error patterns and its syndrome values are presented in \cite{15, 16, 17}. Alabady et al. codes are unable to satisfy single error correction and double error detection functionality in some cases. Beside this limitation, there are some mistakes in flowchart, tables and figure which are rectified in \cite{18}. Ming et al. proposed a SEC-DED-DAEC code to diminish noise source in memories \cite{19}. These existing codes require more area, power and delay.

To mitigate these problems, this paper aims to develop new channel coding techniques. This work proposes a modified SEC-DED-DAEC code for memories. Also, this paper identifies the mistakes in proposed $H$-matrix construction procedures, the formation of equation 6 and one table of ref. \cite{20}. These typos do not affect the main contributions and results of the paper in \cite{20}. Here we have corrected these mistakes in \cite{20}. The main contributions are as follows:

\begin{itemize}
  \item[i)] New method to construct the parity check matrices ($H$) for SEC-DED-DAEC code has been proposed.
  \item[ii)] SEC-DED-DAEC codes with different message length have been designed and implemented in ASIC platform and
  \item[iii)] proposed codes are fast and power efficient compared to existing designs.
\end{itemize}

The rest of this paper is organized as follows. Section II provides design of proposed SEC-DED-DAEC codes. Section III presents estimation of logic gates for different designs. Section IV contains synthesis results and Section V presents the conclusion.

\section{Design of Proposed SEC-DED-DAEC Codes}

Proposed $(n-k)$ error correction code is a linear block code with parity check matrix ($H$) which consists of $(n-k)$ number of rows and $n$ number of columns. There are some mistakes in the construction procedure of (14, 8) proposed ($H$) matrix in ref. \cite{20}. In this section the corrected construction procedure of proposed ($H$) matrices for both SEC-DED and SEC-DED-DAEC codes with different message lengths has been described.

\subsection{$H$-matrix construction procedures}

The procedure to generate the (14, 8) proposed $H$-matrix for both SEC-DED and SEC-DED-DAEC codes is as follows:

\begin{itemize}
  \item[\textbf{Step 1}]: The $H$-matrix consists of $(n-k)$ number of rows and $(n)$ numbers of columns with $k$ numbers of data columns and $(n-k)$ numbers of parity columns having identity property.
  \item[\textbf{Step 2}]: Last data column ($d_8$) has been selected to satisfy the weight 3 as well as modulo-2 sum of $d_8$ and parity column ($p_1$) will generate ‘1’ in positions 1, 3, 4 and 6.
  \item[\textbf{Step 3}]: Data column ($d_7$) is selected to satisfy the weight 3 as well as modulo-2 sum of $d_7$ and data column ($d_8$) will generate ‘1’ in positions 1, 2, 4 and 6.
\end{itemize}
**Step 4:** Process is continued up to the first data column \((d_1)\) using following 
\(Q\)-matrix with target to reduce delay and power consumption without violating 
\(H\)-matrix construction rules.

The \(H\)-matrix of \((14, 8)\) SEC-DED and SEC-DED-DAEC codes are obtained by

\[
Q = \begin{bmatrix} 
11131211 \\
23442323 \\
45553444 \\
56664666 
\end{bmatrix}
\]

**Fig. 1.** \(Q\)-matrix of \((14, 8)\) proposed SEC-DED and SEC-DED-DAEC codes employing the proposed \(H\)-matrix construction methodology and it is shown in Fig. 1. This \(H\)-matrix consists of 8 data columns and 6 parity columns as shown in Fig. 2. Similarly the other \(H\)-matrices are constructed employing proposed

\[
H = \begin{bmatrix} 
10100110100000 \\
01110100100000 \\
11001100100000 \\
10010100100000 \\
01010000000010 \\
00101101000001 
\end{bmatrix}
\]

**Fig. 2.** \(H\)-matrix of \((14, 8)\) proposed SEC-DED and SEC-DED-DAEC codes

construction procedures. The \(H\)-matrix of \((8, 3)\) SEC-DED-DAEC code is pro-

\[
H = \begin{bmatrix} 
11010000 \\
01001000 \\
01100100 \\
10100010 \\
10100001 
\end{bmatrix}
\]

**Fig. 3.** \(H\)-matrix of proposed \((8, 3)\) SEC-DED and SEC-DED-DAEC codes

vided in Fig. 3. This matrix contains \(d_1\) to \(d_3\) data columns and \(c_1\) to \(c_5\) parity columns. The \(H\)-matrix of \((9, 4)\) SEC-DED-DAEC code is provided in Fig. 4.

In this matrix consists of 4 data columns and 5 parity columns. The \(H\)-matrix
Fig. 4. $H$-matrix of proposed (9, 4) SEC-DED and SEC-DED-DAEC codes

\[
H = \begin{bmatrix}
011010000 \\
101001000 \\
010100100 \\
110100010 \\
101100001
\end{bmatrix}
\]

Fig. 5. $H$-matrix of proposed (11, 5) SEC-DED and SEC-DED-DAEC codes

\[
H = \begin{bmatrix}
00110100000 \\
11010010000 \\
01011001000 \\
10101000100 \\
10000000010 \\
01101000001
\end{bmatrix}
\]

of (11, 5) SEC-DED-DAEC code is provided in Fig. 5 which consists of 5 data columns and 6 parity columns. The $H$-matrix of (13, 7) SEC-DED-DAEC code

\[
H = \begin{bmatrix}
0100110100000 \\
0011010010000 \\
1101011001000 \\
0110101000100 \\
101000000010 \\
1001101000001
\end{bmatrix}
\]

Fig. 6. $H$-matrix of proposed (13, 7) SEC-DED and SEC-DED-DAEC codes

is provided in Fig. 6 where $d_1$-$d_7$ are data columns and $c_1$-$c_6$ are parity columns. The $H$-matrix of (24, 16) SEC-DED-DAEC code is provided in Fig. 7. It has 16 data columns and 8 numbers of parity columns.

2.2 Encoding and Decoding Techniques

In this section, encoding and decoding processes of proposed (8, 3) SEC-DED and SEC-DED-DAEC code has been described.

2.2.1 Encoding Process
\[
H = \begin{bmatrix}
1010001010101101101000000 \\
0100000110010110010000000 \\
0001110001010110110010000 \\
0000000111101001000100000 \\
1001110110000000000001000 \\
011101100001010000000001000 \\
00101011110000000000001000 \\
110101001000110100100001000
\end{bmatrix}
\]

Fig. 7. H-matrix of proposed (24, 16) SEC-DED and SEC-DED-DAEC codes

The parity bits are collaborated with the data bits and form the codeword in the encoding process. The equations to generate check-bits of proposed (8, 3) SEC-DED and SEC-DED-DAEC code are in the following.

\[
c_1 = d_1 \oplus d_2 \\
c_2 = d_2 \\
c_3 = d_2 \oplus d_3 \\
c_4 = d_1 \oplus d_3 \\
c_5 = d_1 \oplus d_3
\]

(1)

2.2.2 Decoding Process

Decoding technique has two parts-a) syndrome computation and b) error correction logic. In the first part, error detection can be done by calculating the syndrome value. No error in received codeword is indicated if the syndrome value is zero (SY = 0) else there are some bit-errors. There are some typo errors in Error correction logic subsection in ref. [20]. It is rectified here and the modified error correction logic has been described in the following.

The error can be corrected by using the error correction block. For single error in one of the data bits the syndrome corresponds to one of the data column. In case of double adjacent errors in \(n^{th}\) and \((n + 1)^{th}\) bits the corresponding syndrome is modulo-2 sum of \(n^{th}\) and \((n + 1)^{th}\) columns of \(H\)-matrix. Finally, the error pattern block compares the double adjacent error syndromes and single error syndrome using 2-input OR (OR2) gates to confirm the occurrence of error in \(n^{th}\) bit. If error occurs in the \(n^{th}\) bit, then output of OR2 gate is 1 and error correction is done by 2-input XOR (XOR2) logic, which takes \(n^{th}\) bit and output of OR2 gate as inputs to produce corrected version of data stored in \(n^{th}\) position of codeword.
2.3 Calculation of parity-bits

The main aim of the proposed codes is to minimize the number of 1’s in each row and column of the $H$-matrix. The improvement in delay is occurred by minimizing the number of ones in the row of the matrix. The equation (2) in ref. [20] has been corrected in this section. For weight, $w=3$, the minimum number of parity bits $(n - k)$ are calculated by considering approximate value from the equation (2).

\[
(n - k) \geq (\sqrt{1 + 2.5k + 1.90})
\]  

The equation (2) is applicable for SEC-DED-DAEC codes but there is a limitation. This proposed equation is suitable up to 8-bit SEC-DED-DAEC codes. The number of parity bits required for a specific number of data bits are presented in Table 1.

Table 1. Parity bits required

| Codec | Data bit ($k$) | Number of parity bit ($P$) |
|-------|----------------|---------------------------|
| (8, 3) | 3              | 5                         |
| (9, 4) | 4              | 5                         |
| (11, 5) | 5              | 6                         |
| (12, 6) | 6              | 6                         |
| (13, 7) | 7              | 6                         |
| (14, 8) | 8              | 6                         |

3 Logic gate estimation of complexity analysis

This section presents the logic gate estimation of complexity analysis which consists of area complexity and critical path delay.

3.1 Area complexity

Area complexity in terms of logic gates of proposed and existing SEC-DED and SEC-DED-DAEC codes are presented in Table 2. Proposed codes require lesser number logic gates compared to other existing codes. Also the area complexity comparison of existing and proposed codes has been presented in terms of 2-input NAND (NAND2) gates.

3.2 Critical path delay

Critical path delay of proposed and existing SEC-DED and SEC-DED-DAEC codes are provided in Table 3. It has been observed that the performance of
**Table 2. Area complexity comparison of proposed codes and existing codes**

| Codec       | Schemes                  | XOR2 | AND2 | OR2 | NOT | Equivalent NAND2 |
|-------------|--------------------------|------|------|-----|-----|------------------|
| **Existing** |                          |      |      |     |     |                  |
| SEC-DED     | Alabady (9, 4) [15, 16]  | 31   | 16   | -   | 4   | 160              |
|             | Alabady (9, 4) [17]      | 15   | 16   | -   | 12  | 104              |
|             | Adalid (8, 4) [13, 14]   | 27   | 17   | 3   | 5   | 156              |
|             | Hsiao (13, 8) [4]        | 51   | 32   | -   | 16  | 284              |
|             | Hamming (13, 8) [3]      | 59   | 32   | -   | 14  | 314              |
|             | Cha, Yoon (13, 8) [12]   | 58   | 32   | -   | 13  | 309              |
|             | Adalid (16, 8) [13, 14]  | 55   | 25   | 7   | 1   | 292              |
| **Proposed** |                          |      |      |     |     |                  |
| SEC-DED     | Proposed (8, 3)           | 16   | 6    | -   | -   | 76               |
|             | Proposed (9, 4)           | 23   | 8    | -   | -   | 108              |
|             | Proposed (11, 5)         | 29   | 10   | -   | -   | 136              |
|             | Proposed (13, 7)         | 43   | 14   | -   | -   | 200              |
|             | Proposed (14, 8)         | 50   | 16   | -   | -   | 232              |
|             | Proposed (24, 16)        | 120  | 32   | -   | -   | 544              |
| **Existing** |                          |      |      |     |     |                  |
| SEC-DED-DAEC | Ming (22, 16) [19]       | 112  | 235  | 31  | 120 | 1131             |
|             | Dutta (22, 16) [5]       | 106  | 235  | 31  | 126 | 1113             |
| **Proposed** |                          |      |      |     |     |                  |
| SEC-DED-DAEC | Proposed (8, 3)          | 20   | 24   | 5   | -   | 143              |
|             | Proposed (9, 4)          | 27   | 33   | 7   | -   | 195              |
|             | Proposed (11, 5)        | 34   | 42   | 9   | -   | 247              |
|             | Proposed (13, 7)        | 48   | 60   | 13  | -   | 351              |
|             | Proposed (14, 8)        | 55   | 69   | 15  | -   | 403              |
|             | Proposed (24, 16)       | 127  | 141  | 31  | -   | 883              |

**Table 3. Critical path delay comparison of proposed codes and existing codes**

| Codec       | Schemes                  | XOR2 | AND2 | OR2 | NOT | Equivalent NAND2 |
|-------------|--------------------------|------|------|-----|-----|------------------|
| **Existing** |                          |      |      |     |     |                  |
| SEC-DED     | Alabady (9, 4) [15, 16]  | 8    | 4    | -   | 1   | 41               |
|             | Alabady (9, 4) [17]      | 4    | 4    | -   | 2   | 26               |
|             | Adalid (8, 4) [13, 14]   | 9    | 4    | -   | 2   | 46               |
|             | Hsiao (13, 8) [4]        | 10   | 4    | -   | 1   | 49               |
|             | Hamming (13, 8) [3]      | 20   | 4    | -   | 1   | 89               |
|             | Cha, Yoon (13, 8) [12]   | 18   | 4    | -   | 1   | 81               |
|             | Adalid (16, 8) [13, 14]  | 10   | 3    | 7   | 1   | 68               |
| **Proposed** |                          |      |      |     |     |                  |
| SEC-DED     | Proposed (8, 3)           | 4    | 2    | -   | -   | 20               |
|             | Proposed (9, 4)           | 6    | 2    | -   | -   | 28               |
|             | Proposed (11, 5)         | 6    | 2    | -   | -   | 28               |
|             | Proposed (13, 7)         | 10   | 2    | -   | -   | 44               |
|             | Proposed (14, 8)         | 10   | 2    | -   | -   | 44               |
|             | Proposed (24, 16)        | 16   | 2    | -   | -   | 68               |
| **Existing** |                          |      |      |     |     |                  |
| SEC-DED-DAEC | Ming (22, 16) [19]       | 22   | 5    | 2   | 1   | 105              |
|             | Dutta (22, 16) [5]       | 18   | 5    | 2   | 1   | 89               |
| **Proposed** |                          |      |      |     |     |                  |
| SEC-DED-DAEC | Proposed (8, 3)          | 8    | 3    | 2   | -   | 44               |
|             | Proposed (9, 4)          | 10   | 3    | 2   | -   | 52               |
|             | Proposed (11, 5)        | 11   | 3    | 2   | -   | 56               |
|             | Proposed (13, 7)        | 15   | 3    | 2   | -   | 72               |
|             | Proposed (14, 8)        | 15   | 3    | 2   | -   | 72               |
|             | Proposed (24, 16)       | 23   | 3    | 2   | -   | 104              |
proposed codes is better than related existing SEC-DED and SEC-DED-DAEC codes. The critical path delays of proposed codes are compared to the Alabady et al. code [17], Adalid et al. code [13], Hsiao code [4], Hamming code [3], Cha-Yoon code [12] and Ming et al. code [19].

4 Synthesis results

The proposed SEC-DED and SEC-DED-DAEC codes have been represented in Verilog hardware description language (HDL). All codes have been simulated and synthesized in ASIC platform using Cadence based Genus synthesis solution (TSMC18) tool. The ASIC-based synthesis results in terms of area, power, delay, power delay product (PDP), power area product (PAP) and cost (product of area, power and delay) of proposed and existing SEC-DED and SEC-DED-DAEC codes have been presented in Table 4.

| Codec        | Schemes       | Area   | Power  | Delay  | PDP    | PAP    | Cost   |
|--------------|---------------|--------|--------|--------|--------|--------|--------|
| Existing SEC-DED |               |        |        |        |        |        |        |
| Alabady (9, 4) | [15]          | 592.11 | 59.36  | 365.3  | 21.69  | 0.04   | 0.013  |
| Alabady (9, 4) | [17]          | 475.66 | 38.84  | 282.4  | 10.97  | 0.02   | 0.005  |
| Adalid (8, 4) | [13]          | 708.54 | 70.67  | 465.3  | 25.82  | 0.05   | 0.018  |
| Hsiao (13, 8) | [4]           | 1284.96| 155.94 | 602.9  | 47.24  | 0.20   | 0.061  |
| Hamming (13, 8) | [3]        | 1204.17| 145.41 | 328.9  | 47.83  | 0.18   | 0.058  |
| Cha, Yoon (13, 8) | [12]        | 1208.45| 159.58 | 365.3  | 55.55  | 0.19   | 0.070  |
| Adalid (16, 8) | [13]          | 1380.45| 180.83 | 423.5  | 76.58  | 0.25   | 0.106  |
| Proposed SEC-DED |               |        |        |        |        |        |        |
| Proposed (8, 3)   |               | 382.55 | 34.16  | 362.4  | 12.37  | 0.01   | 0.005  |
| Proposed (9, 4)   |               | 542.22 | 56.92  | 365.3  | 20.80  | 0.03   | 0.011  |
| Proposed (11, 5)  |               | 708.52 | 69.73  | 341.9  | 23.84  | 0.05   | 0.017  |
| Proposed (13, 7)  |               | 997.93 | 110.38 | 337.5  | 37.25  | 0.11   | 0.037  |
| Proposed (14, 8)  |               | 1109.95| 138.02 | 292.7  | 40.40  | 0.16   | 0.046  |
| Proposed (24, 16) |               | 2318.51| 344.57 | 308.4  | 106.27 | 0.80   | 0.246  |
| Existing SEC-DED-DAEC |         |        |        |        |        |        |        |
| Ming (22, 16) | [19]          | 2877.34| 486.99 | 467.4  | 227.62 | 1.40   | 0.655  |
| Dutta (22, 16) | [5]           | 2920.58| 461.16 | 429.3  | 197.98 | 1.35   | 0.578  |
| Proposed SEC-DED-DAEC |          |        |        |        |        |        |        |
| Proposed (8, 3)  |               | 555.52 | 61.18  | 273.6  | 16.74  | 0.03   | 0.009  |
| Proposed (9, 4)  |               | 751.77 | 87.33  | 289.7  | 25.30  | 0.07   | 0.019  |
| Proposed (11, 5) |               | 908.12 | 115.75 | 502.8  | 58.20  | 0.11   | 0.055  |
| Proposed (13, 7) |               | 1343.87| 177.40 | 482.7  | 85.63  | 0.24   | 0.115  |
| Proposed (14, 8) |               | 1543.44| 238.85 | 433.8  | 103.61 | 0.37   | 0.160  |
| Proposed (24, 16) |              | 2826.59| 619.47 | 434.4  | 269.10 | 1.75   | 0.761  |

5 Conclusion

In this paper, SEC-DED and SEC-DED-DAEC codes have been proposed for different message lengths. These SEC-DED and SEC-DED-DAEC codes have
been designed and implemented based on ASIC platform. Performance of our
design has been analyzed in terms of area, power, delay, PDP, PAP and cost. The
estimation of logic gates for proposed and existing SEC-DED and SEC-DED-
DAEC codes are provided. Our proposed design is faster and power efficient than
other related designs.

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