Crosstalk Analysis and Suppression of Single Chip SiC MOSFET Half-Bridge Circuit

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Abstract. For the hard-switch applications of the half-bridge circuit based on SiC MOSFET, the crosstalk generation mechanism of the half-bridge circuit in the switching on and off process is analysed. The influence of the driving resistance and stray inductance of driving circuit on the crosstalk is simulated and analysed. In the single-chip half-bridge circuit, the Miller clamp method with BJT + diode is used. By increasing the driving resistance and reducing the clamp circuit inductance, the crosstalk suppression effect can greatly improve. It is an effective way to optimize the clamping circuit and reduce the clamp circuit inductance without affecting the switch speed.

1. Introduction

The half-bridge circuit is one of the basic circuit topologies widely used in synchronous rectification, full-bridge circuits, inverters and other power applications. The application of wide-bandgap power electronic devices represented by SiC MOSFET has further improved the performance of the half-bridge circuit [1,2]. Compared with the traditional Si IGBT as the core device, the half-bridge circuit based on the SiC MOSFET has lower switching loss and conduction loss at the same rated current. Thanks to the body diode structure of SiC MOSFET, the external anti-parallel diode is no longer needed, which means that the half-bridge circuit based on SiC MOSFET has higher efficiency and higher power density [3-5]. However, there is always the problem of crosstalk between upper and lower switches in hard-switch half-bridge circuits. SiC MOSFET devices with faster switching speeds will produce larger \( \frac{dv}{dt} \) during switching process, which makes the problem more serious [6,7]. Due to processing problems of the gate of SiC MOSFET, the threshold voltage and negative safety voltage are small. The positive and negative voltage spikes caused by crosstalk can easily lead to unexpected turning on of the device and even lead to gate breakdown and damage to the device [8-10]. Therefore, it is necessary to analyse the mechanism of crosstalk and suppress it to improve the reliability of the circuit.

This paper introduces the crosstalk generation mechanism and influencing factors of the half-bridge circuit based on SiC MOSFET and proposes the method of Miller clamp crosstalk suppression. The crosstalk suppression of the single-chip SiC MOSFET parallel half-bridge circuit is analysed.

2. Crosstalk Generation Mechanism of Half-Bridge Circuit

A typical half-bridge circuit and its driving are shown in Figure 1. The upper and lower switches (M₁, M₂) share the bus voltage \( V_{bus} \) in series. Therefore, when the drain-source voltage of one SiC MOSFET
(which marked $V_{ds}$) changes, the other device's $V_{ds}$ will also change. For the convenience of discussion, this paper assumes that $M_1$ is the switch actively switching on and off and $M_2$ does not perform active switching behaviours. In general applications, in order to avoid through failures, there is a dead time between the upper and lower switching signals of the half-bridge circuit. When the upper switch turns on and off, the lower switch is always in the off-state. Therefore, in the following discussion, the lower switch can always be set to the off-state. Because the half-bridge circuit is usually used in the symmetrical working state of the upper and lower switches, the device parameters and driving parameters of the upper and lower switches are set the same.

![Figure 1. Typical half-bridge circuit and its driving circuit diagram.](image)

2.1. Crosstalk during Turn-on

The turn-on process of $M_1$ can divide into two stages. In the first stage, the channel current of $M_1$ rises and the current rise rate is marked as $\frac{di_{d1}}{dt}$. The changing current generates a forward voltage drop $V_L$ on the line stray inductance $L_{loop}$. In the second stage, $V_{ds1}$ begins to fall and $V_{gs1}$ enters the Miller platform. During the drop of $V_{ds1}$, the voltage across the Miller capacitor $C_{gd}$ drops and a discharge current generate on $C_{gd}$. The magnitude of the discharge current are determined by the driving resistance, the driving positive voltage $V_{cc}$ and the Miller platform voltage $V_{gsm}$. Assuming that $V_{gsm}$ does not change during this process, the rate of changing of $V_{ds1}$ can be expressed by formula (1):

$$\frac{dV_{ds1}}{dt} = -\frac{V_{cc} - V_{gsm}}{R_g C_{gd1}}$$

(1)

The junction capacitance $C_{gd1}$ represents the $C_{gd}$ value when the drain-source voltage is $V_{ds1}$.

The $V_{ds2}$ of $M_2$ is divided into two stages accordingly. In the first stage, the $M_2$ body diode (or anti-parallel diode) is turned on, $V_{ds2} = 0V$; in the second stage, the minority carrier recombination of the diode ends. The junction capacitance of $M_2$ begins to charge and $V_{ds2}$ rises. $V_{ds2} = V_{bus} - V_L - V_{ds1}$, where $V_{bus}$ is the DC voltage between the positive and negative buses in the half-bridge circuit.

At the beginning of the second stage, $V_{ds2}$ is very low and the junction capacitance $C_{gd2}$ of $M_2$ is relatively large. The variation of $V_{ds2}$ is mainly composed of $V_{gd2}$ and $V_{gs2}$. But this period is very short and $V_{gs2}$ is far from reaching the peak value. So the time period with lower $V_{ds2}$ is not introduced and analysed and only the situation when $V_{ds2}$ is higher is considered. When $V_{ds2}$ is high, $C_{gd2}$ is very small relative to $C_{gs2}$ and the change of $V_{ds2}$ mainly lies in $V_{gd2}$. The changing rate of $V_L$ is negligible. Therefore, the changing rate of the drain-gate voltage of $M_2$ can be expressed as:

$$\frac{dV_{gd2}}{dt} \approx \frac{dV_{ds2}}{dt} = -\frac{dV_{ds1}}{dt} = -\frac{V_{cc} - V_{gsm}}{R_g C_{gd1}}$$

(2)

As the $V_{gd2}$ of $M_2$ increases, a charging current is generated on $C_{gs2}$. Part of the current flows to $C_{gs2}$ and charges it causing the gate-source voltage of $M_2$ to rise, while another part of the current flows to the loop where $R_g$ is located. The charging current of $C_{gd2}$ is marked as $i_m$. The charging current of $C_{gs2}$
is marked as $i_{g}$. The current flowing through $R_{g}$ is marked as $i_{g}$, which is assumed to be unchanged. According to the circuit principle, the current relations (3)-(5) can be obtained as follows:

$$i_{m} = C_{gd2} \frac{dV_{gd2}}{dt} \frac{C_{gd}(V_{ds2})}{V_{cc} - V_{gsm}}$$

(3)

$$\int_{0}^{t} i_{gs} dt = \int_{0}^{t} (i_{m} - i_{g}) dt = C_{gs2} V_{gs2}.$$  

(4)

$$R_{g} i_{g} + L_{g} \frac{di_{g}}{dt} = V_{gs2}.$$  

(5)

**Figure 2.** Schematic diagram of crosstalk waveforms during switching of half-bridge circuit.

Figure 2 shows the waveform diagram of crosstalk during the switching of the half-bridge circuit. It can be seen from the figure that at time $t_{0}$, $V_{ds 2}$ starts to rise and $V_{ds 1}$ falls accordingly. At this moment, the value of $C_{gd 2}/C_{gd 1}$ is the largest. From (3), we can see that $i_{m}$ is also the maximum at this moment. After that, the value of $C_{gd 2}/C_{gd 1}$ decreases rapidly and at the same time $i_{m}$ continues to fall. From $t_{0}$ to $t_{2}$, the junction capacitance $C_{gs 2}$ changes as $i_{gs}$ and $V_{gs 2}$ rises. Meanwhile, $i_{g}$ rises and $i_{gs}$ falls. At $t_{2}$, $i_{gs}$ drops to zero and $V_{gs 2}$ reaches the positive maximum value ($V_{gpm}$). If $V_{gpm}$ is less than the threshold voltage $V_{th}$, $M_{2}$ will not turn on, then the positive effect of crosstalk on the $V_{gs}$ of $M_{2}$ can ignore; if $V_{gpm}$ exceeds $V_{th}$, the phase where $V_{gs 2}$ exceeds $V_{th}$ is marked as $t_{1}$ to $t_{3}$. Then in the time from $t_{1}$ to $t_{3}$ ($t_{2}$ to $t_{4}$ in Figure 2), $M_{2}$ is turned on and the current $i_{d 2}$ is superimposed on the current $i_{d 1}$ of $M_{1}$ to produce a higher turn-on current spike. After $t_{2}$, $i_{m}$ is not enough to support the $V_{gs 2}$ and $C_{gs 2}$ starts to discharge. $V_{gs 2}$ drops until both $V_{gs 2}$ and $i_{m}$ drop to zero at $t_{4}$. The crosstalk activation process ends.

### 2.2. Crosstalk during Turn-off

As shown in Figure 2, the crosstalk of the turn-off process starts at $t_{5}$. $V_{ds 1}$ rises and $V_{ds 2}$ falls. The Miller capacitor $C_{gd 2}$ of $M_{2}$ flows through the discharge current and the direction is opposite to the positive direction defined by $i_{m}$ in Figure 1. As $V_{ds 1}$ rises, $C_{gd 1}$ falls and $C_{gd 2}$ rises, so $C_{gd 2}/C_{gd 1}$ increases and $i_{m}$ also rises. At $t_{6}$, $V_{ds 1}$ reaches its maximum value (without considering the influence of $L_{loop}$) and $i_{m}$ reaches its peak value. Almost at the same time, $V_{gs 2}$ reaches a negative peak, which is marked as $V_{gpm}$. Then the change of $V_{ds 2}$ ends and $C_{gs}$ starts to discharge. $V_{gs 2}$ falls and $i_{m}$ rapidly drops from the peak value to a part of the $C_{gs}$ discharge current and continues to fall. At $t_{8}$, $V_{gs 2}$ and $i_{m}$ drops to zero and then the turn-off crosstalk process ends.
From $t_5$ to $t_6$, the relevant voltage and current still satisfy the equations (3)-(5). However, the $V_{gm}$ of the turn-off crosstalk must consider the entire turn-off process. Therefore, the relationship between $C_{gd}$ and $V_{ds}$ is very complicated.

3. Single-chip Half-bridge Miller Clamp Circuit

The main influences on crosstalk are as follows: driving resistance $R_g$, junction capacitance $C_{gs}$ and $C_{gd}$, driving loop stray inductance $L_g$, load current $I_{load}$, and driving voltage $V_{cc}$. The junction capacitance by the selected MOSFET. The load current and driving voltage are usually not changeable for specific applications. Therefore, the only thing that can be optimized are the driving resistance and the stray inductance of the driving loop.

We chose the Miller clamp method based on BJT + Diode to analyse the performance of crosstalk suppression in hard-switch half-bridge circuits. The half-bridge circuit based on SiC MOSFET Miller clamp is shown in Figure 3. The selected SiC MOSFET is Rohm’s SCT3022KL. The selected BJT is Infineon’s BCW68G and diode is ST Microelectronics’ BAR42. The bus voltage is 800V. In order to better suppress the positive fluctuation of $V_{gs}$, a stabilizing capacitor connected to an external 1.8V auxiliary power supply add to the driving circuit so that $V_{gs}$ is at -1.8V when the switch is off.

![Figure 3. The SiC MOSFET half-bridge circuit diagram with BJT + diode clamp.](image)

3.1. The Influence of Driving Resistance on Crosstalk in Actual Circuit

The driving resistance $R_g$ is composed of the gate resistance $R_{gout}$ and the internal driving resistance of the device. Different driving resistance means different switching speed. The amplitude of $V_{gs}$ crosstalk fluctuation is also different. After the Miller clamp circuit is connected in parallel between the gate and source of the switch, the driving current basically does not flow through the clamp circuit. The switching speed still determines by the loop composed of the driving resistance $R_g$ and the driving loop stray inductance $L_g$.

The crosstalk process under different driving resistances is tested (the load current is 68A). The test circuit includes the simple driving half-bridge circuit without Miller clamp in Figure 1 and the clamp driving half-bridge circuit with BJT+Diode clamp in Figure 3. Since the real $V_{gs}$ inside the device cannot be detected directly, the drain-source current is detected to reflect the crosstalk and suppression. In order to improve the measurement accuracy, the current is measured through a high-precision shunt resistance (shunt). The test results are shown in Figure 4 and Figure 5.
**Figure 4.** The gate source voltage and current waveforms of hard switch in half-bridge circuit without clamp driving. (a) Turn-on (b) Turn-off.

**Figure 5.** The gate source voltage and current waveforms of hard switch in half-bridge circuit with BJT + Diode clamp driving. (a) Turn-on (b) Turn-off.

**Figure 6.** Comparison of switch-on loss with or without clamp driving.

Comparing Figure 4 and Figure 5, it can be seen that with the increase of the driving resistance, the overshoot of the turn-on current of the two test circuits is decreasing. The decrease in the overshoot of the turn-on current means that $V_{gpm}$ decreases. This result is consistent with the simulation result in Figure 3. Comparing the current and voltage waveforms between the drain and source of the switch without a clamp circuit under the same driving resistance, it can be found that the changing rate of the voltage of the two is not much different, which shows that the switching speed of the two is the same; The overshoot of the turn-on current is quite different because of the Miller clamp. Figure 6 shows the turn-on loss of the SiC MOSFET with or without Miller clamp. It also can be seen from the two figures that the current overshoot amplitude of the switch with Miller clamp driving is lower and the overshoot time is shorter. So its turn-on loss is smaller, and as the driving resistance increases, the difference between the two will increase.
3.2. The Effect of Clamp Loop Stray Inductance Crosstalk in Actual Circuit

The $V_{gs}$ forward crosstalk fluctuation of the half-bridge circuit with Miller clamp driving is difficult to be completely suppressed. Therefore, the clamping loop needs to optimize as much as possible to reduce stray inductance without affecting the switching speed.

**Figure 7.** The measurement circuit of the influence of stray inductance of different clamping circuit on crosstalk.

In order to understand the influence of the stray inductance $L_{g\text{clamp}}$ on the crosstalk effect, simulation and actual measurement of the BJT clamp driving half-bridge circuit under different $L_{g\text{clamp}}$ are carried out. The actual measurement circuit built according to the principal circuit is shown in Figure 7. The DUT is a switch that is always in the off-state. Each bridge arm has three SiC MOSFETs connected in parallel. The dashed box A/B/C corresponds to the clamping circuits. The stray inductance values extracted by the Q3 software between each clamp circuit and the corresponding switch are about 6 nH, 10 nH and 14 nH respectively. The bus voltage is 800 V, the driving resistance is 10 Ω and the load current is 30 A.

**Figure 8.** The current simulation results on the crosstalk MOSFET corresponding to the different clamp circuit inductance.
Figure 9. Measured waveforms on the crosstalk MOSFET corresponding to the different clamp circuit inductance; (a) $V_{gs}$ (b) $I_d$.

Figure 8 is the simulation result of the current on the crosstalk switch under different clamp loop inductance $L_{gclamp}$. It can be seen that with the increase of $L_{gclamp}$, the peak value of the unexpected turning on current in the crosstalk switch and the unexpected turning on time both increases.

Figure 9 shows the actual measured $V_{gs}$ voltage waveform and drain-source current waveform on the crosstalk switch with different clamp loop inductances. It can be seen from the results that as $L_{gclamp}$ increases, the forward fluctuation amplitude of $V_{gs}$ of the crosstalk switch, the peak value of the unexpected turning on current and the unexpected turning on time all increase, which are consistent with the simulation results. In addition, as the increase of $L_{gclamp}$, the oscillation peak value after $V_{gs}$ drops and crosses zero also increases. This test result verifies the previous simulation analysis result.

4. Conclusions
This paper focuses on hard-switch applications of the half-bridge circuit based on SiC MOSFET and analyses the crosstalk generation mechanism during switching on and off process. The influence of driving resistance and driving loop stray inductance on the effect of crosstalk is analysed and simulated. In the single-chip half-bridge circuit, the Miller clamp method with BJT + Diode is adopted and the suppression effect of crosstalk improve by increasing the driving resistance and reducing the inductance of the clamp loop. This shows that optimizing the clamp loop and reducing the inductance of the clamp loop are methods that are more effective without affecting the switching speed.

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