Abstract—A digital finite impulse response (FIR) filter design is fully synthesizable, thanks to the mature CAD support of digital circuitry. On the contrary, analog mixed-signal (AMS) filter design is mostly a manual process, including architecture selection, schematic design, and layout. This work presents a systematic design methodology to automate AMS FIR filter design using a time approximation architecture without any tunable passive component, such as switched capacitor or resistor. It not only enhances the flexibility of the filter but also facilitates design automation with reduced analog complexity. The proposed design flow features a hybrid approximation scheme that automatically optimize the filter’s impulse response in light of time quantization effects, which shows significant performance improvement with minimum designer’s efforts in the loop. Additionally, a layout-aware regression model based on an artificial neural network (ANN), in combination with gradient-based search algorithm, is used to automate and expedite the filter design. With the proposed framework, we demonstrate rapid synthesis of AMS FIR filters in 65nm process from specification to layout.

I. INTRODUCTION

High-performance filtering is increasingly demanded by wireless communication systems for supporting multi-band and multi-mode operations. Traditionally, bulky off-chip SAW filters or tuned LC filters are used at the transmitter and receiver front-ends to achieve the required selectivity. As a more scaling-friendly alternative of these conventional analog filter, an analog mixed-signal (AMS) finite impulse response (FIR) filter is gaining growing popularity in direct radio frequency (RF) transmitters [1], [2]. However, the reconfiguration of such filter is typically achieved by tuning the analog components, i.e., resistor, capacitor or current source. This leads to limited flexibility, makes the system vulnerable to process, voltage and temperature (PVT) variations, and imposes challenges for a complete design automation.

Recently, a time-approximation filter (TAF) technique is proposed to tackle the issue by approximating the amplitude-varying impulse response of an AMS FIR filter with a constant-amplitude but time-duration-varying (i.e. digital-like) waveform [3]. Thanks to the mostly digital operations, TAF is highly flexible, scalable, implementation-friendly, and less prone to PVT variations. As a tradeoff of using time approximation, the finest achievable time resolution of TAF is constrained by the system clock rate, which degrades the filter performance and hence necessitates an effective searching algorithm to fine tune the filter’s impulse response. Additionally, like most AMS circuit blocks, AMS filter design is mostly a manual process compared to a digital FIR filter. Although there are prior arts exploring digital architectures [4]–[6] or using digital gates to approximate the function of an analog block [7], [8], most of the works lack efficient modeling and optimization techniques for the sizing and biasing of the circuits, which still require significant amounts of handcrafted design efforts and time from experienced analog designers.

To address the existing design automation challenges for AMS filters, we propose a design automation flow, hereafter referred to as TAF, with the following objectives: 1) apply time approximation technique to the AMS FIR filter and derive an optimum impulse response for the filter with minimum human intervention, and 2) automate the design of high-performance AMS filters within a short time frame. The primary features of TAF are summarized below.

- The proposed hybrid approximation scheme for filter’s impulse response significantly reduces time approximation errors of TAF over a wide range of specifications.
- A mostly-digital capacitor digital-to-analog converter (DAC) structure with a counter-based TAF waveform generation is proposed for filter implementation which favors the technology scaling and digital design flow.
- A layout-aware regression model combined with advanced search algorithms is used to expedite the synthesis of the filter by orders of magnitude during both schematic and layout design stages.

II. TIME-APPROXIMATION FILTER

A. Time Approximation of an Arbitrary AMS FIR Filter

The concept of time approximation scheme is shown in Fig. 1. The N-level impulse response of an arbitrary AMS FIR filter is encoded into a two-level time-modulated waveform, such that these two waveforms have similar frequency...
responses for filtering. Conventionally, AMS FIR filter implements the filter coefficients by scaling the size of DACs. The mismatch between the DACs inevitably degrades the filter performance. In contrast, TAF only requires a single DAC to express all of the filter coefficients by multiplying the digital-like TAF pattern with the input digital signal. Therefore, there is no mismatch between the filter taps. The multiplication can be achieved via MUXs or NAND gates for a single-bit pattern with minimum extra implementation overhead. In addition, TAF allows changing the filter coefficient digitally with a wide tuning range, which makes it more flexible than the conventional AMS FIR filter.

B. Time Approximation Errors

There are mainly two types of time approximation errors for a TAF: 1) the intrinsic error of approximating an amplitude-varying response in time with a constant amplitude and 2) the time quantization error set by minimum achievable time resolution. To the first order, the intrinsic approximation error $G_{err}$ is estimated as a function of the frequency $f$,

$$G_{err} = 20 \log_{10} \frac{\text{sinc}(a_{\text{min}} T_{\text{tap}} f)}{\text{sinc}(T_{\text{tap}} f)},$$

where $a_{\text{min}}$ is the smallest filter coefficient and $T_{\text{tap}}$ is the time interval between the adjacent filter taps.

In reality, the resolution of time approximation is determined by the period of the fastest clock, which cannot be infinitely small. Therefore, the time quantization error due to finite time resolution degrades the TAF performance. With the presence of circuit non-idealities, TAF’s response will further deviate from the original FIR filter response in terms of the locations and depth of filter notches and the in-band flatness.

III. PROPOSED FILTER AUTOMATION FLOW

Figure 2 shows the proposed AMS filter design flow. Based on the filter specifications, a hybrid TAF pattern (impulse response) generator is used to optimize the TAF pattern and minimize the time approximation errors given certain time quantization resolution. In addition, the simulated output transient waveforms of the circuit (schematic and post-layout netlists) are fed back to the TAF pattern generator for further pattern optimization considering the circuit non-idealities. To expedite the AMS filter design, we combine advanced search algorithm with a layout-aware regression model to rapidly search for the design parameters, such as device sizing and biasing. The regression model is based on an artificial neural network (ANN), which is first trained and validated using a schematic-level dataset generated from a parameterized circuit netlist and SPICE simulations.

To incorporate the layout parasitic information, a linear transfer learning (LTL) technique is applied to the ANN model trained using the schematic dataset. The layouts are generated using the proposed mixed-signal layout automation flow, which includes the standard digital design flow and a custom place and route (P&R) engine for analog components and top-level integration. After the layout-aware model is obtained, the design parameters are determined using a gradient based search algorithm. This layout-aware parameter search method leverages the fast speed of ANN inference and the reduced post-layout simulation overhead thanks to LTL, thus enabling efficient and low-cost optimization.

A. Hybrid TAF Pattern Generation

The proposed hybrid TAF pattern generation is depicted in Fig. 3. To avoid inefficient search in an enormous space of TAF pattern, a discrete-time (DT) FIR filter response is first designed based on the filter specifications ($h_{\text{FIR}}[n]$), and then converted into continuous-time (CT) response via zero-order hold (ZOH) interpolation ($h_{\text{FIR}}[t]$). To create TAF response ($h_{\text{TAF}}[t]$) from the CT FIR response, a time approximation on the filter coefficients is performed via pulse width ($a_n$) and position ($p_n$) modulations, such that the area and the position of each pulse is the same as that in $h_{\text{FIR}}[t]$. Pulse width and position are then quantized by the finite time resolution. The quantized time-approximated filter response ($h_{q}[t]$) is typically not optimal at this stage due to the time approximation errors and circuit non-linearity. An optimization loop based on coordinate descent is employed to fine tune the pulse width ($a^*_n$) and position ($p^*_n$) of each filter coefficient, so that TAF performance is maintained or improved in the presence of the aforementioned non-idealities.
Figure 4 presents the proposed fine tune scheme. The TAF response obtained from the knowledge-based approximation steps \((h_q^n)\) is used as the initial point of the optimization loop. Based on the loss incurred in taking a step toward a certain direction, the optimization engine decides whether to stay at the current location or move toward that direction. The updated TAF response at the \(i\)th iteration is annotated as \(h_q^i\), and is used to calculate the loss in the next decision. In order to be flexible, different loss functions can be applied for different applications. If the goal is to design a TAF response that mimics the response of the target CT FIR filter within the whole Nyquist band (DC to \(B\)) as closely as possible, the loss function is designed as:

\[
L(B) = \frac{1}{B} \int_0^B \left( |H_{FIR}(f)| - |H_q^n(f)| \right) df. \tag{2}
\]

The function utilizes the normalized magnitude difference between the frequency responses of the target FIR filter and the associated TAF. On the other hand, for applications that require extremely low noise at a specific band of interest, the loss function is designed as

\[
L(B_1, B_2, f_0) = \int_0^{B_1} \frac{|H_q^n(f)|}{B_1} df - \int_{f_0}^{f_0 + B_2} \frac{|H_q^n(f)|}{B_2} df, \tag{3}
\]

which uses the difference between the integrated energy within the signal band (DC to \(B_1\)) and the integrated energy of the specific band of interest \((f_0 \text{ to } f_0 + B_2)\). Given the fixed in-band energy, lower loss leads to deeper noise suppression at the specific band. Note that other potential loss functions can be applied for different optimization objectives under the same framework.

Figure 5 shows two examples of TAF response optimizations with different loss functions. In Fig. 5(a), loss function 2 is used for approximating an 8-tap FIR filter. A TAF response closer to the target FIR filter response is achieved via the proposed fine-tuning scheme. In Fig. 5(b), a 4-tap FIR filter is first designed and approximated in time with the knowledge-based approach. Then, loss function 3 is applied to tweak the TAF response so deeper attenuation at \(B_2\) can be achieved.

B. Layout-Aware Circuit Parameter Search

The proposed layout-aware circuit parameter search is shown in Fig. 6. First, we generate an ANN model representing the schematic-level parameter-to-metric (P2M) function (step 1 in Fig. 6). We select a large number of parameter combinations using random sampling from a predefined range of the circuit parameters and find the corresponding performance metrics via schematic-level SPICE simulations.

Next, layout parasitic information is incorporated in the ANN model (step 2 in Fig. 6). Obtaining training dataset (parameters-metrics pairs) in layout design stage is extremely inefficient compared to the schematic stage due to the long SPICE simulation time needed for post-layout designs. To reduce the number of required training samples for the layout model, we reuse the schematic-level ANN model and add a linear layer at its input and output. The weights and biases of the original ANN remain fixed, and only the added linear layers are trained using the post-layout simulation data.

Even though the cost of training the ANN model is not low, we only need to go through steps 1 and 2 once for a specific circuit as a tool developer. After obtaining the layout-aware ANN model, as a tool user, we search for the circuit parameters (step 3 in Fig. 6) which satisfy the desired specifications. Thanks to the quick evaluation using the ANN model, TAFA can rapidly determine the circuit parameters for diverse specifications. At each search iteration, the gradient-based algorithm changes the design parameters in a direction which minimizes a loss defined by the difference between ANN predicted metrics and the target specs. A parallel Monte Carlo optimization is also adopted to enable a fast and optimum parameter search 9. By utilizing multiple random initial parameters, the search process can avoid getting trapped in a local minimum of the loss function. Using this technique, we can generate multiple design candidates which can satisfy the given specifications within a short time frame.

C. Mixed-Signal Layout Automation Flow

The mixed-signal layout generation is a hybrid flow that utilizes both standard digital design tools and a custom
synthesis engine, as shown in Fig. 7. Critical analog blocks including the DAC drivers and capacitors need to be carefully designed and laid out to guarantee the filter performance. Therefore, we developed a custom P&R engine based on an open-source Python framework, taking insights from analog circuit designers. Considering the symmetry requirement for P&R and dummy cells for load balancing, layout templates are encoded in the P&R scripts. Similar to [13] and [14], the layout templates are parameterized for different device sizes. The libraries of devices, including custom MOSFETs and capacitors, are prepared and used by the custom P&R for different designs. Note that these analog blocks can also be laid out using other state-of-the-art P&R tools, which leverage the advanced algorithms to generate the layouts without providing the detailed layout template by the designers, as seen in [15], [16]. Those alternatives can be seamlessly integrated into the TAF flow. To leverage the well-developed digital design flow, we herein propose a capacitor DAC structure and a counter-based TAF waveform generator, which are more digitally-intensive implementations than the design in [3]. As a result, most of the circuits become less sensitive to mismatch and symmetry requirements and can be generated by the digital synthesis tools using a digital standard cell library. Behavioral Verilog files and timing constraints are prepared for digital synthesis and P&R. In the end, the custom P&R integrates the digital-synthesized layouts with the custom layouts for a single channel of the TAF. To generate the whole TAF, the system-level P&R in the flow can integrate eight time-interleaved channels symmetrically considering the power, signal, and clock routing. Such hierarchical layout generation is another feature of the proposed flow.

IV. Experimental Results

A. Embodiment of Filter Implementation

The block diagram of the TAF implementation is shown in Fig. 8 and is used to demonstrate the proposed TAF flow. To extend the impulse response of the TAF, an eight-way time-interleaved (TI) structure is used. Each TI channel consists of a capacitor DAC and a counter-based TAF waveform generator. The clock signal (clk) used for the TAF waveform generation is divided eight times via the feedback flops and further divided into eight slower clocks with shifted phases for TI operation. The shifted phases are generated by a ring counter, as shown in Fig. 8. The TAF pattern is synthesized with the proposed hybrid flow and stored as static digital signals. The TAF waveform generator uses a MUX and a counter to serialize these static signals into a 1-bit data stream, which is then used to modulate the DAC input signal for the TAF. In the circuit example, the TAF pattern contains 64 bits. A DFF is inserted at the output of the MUX to avoid glitches of the MUXed signal and to simultaneously force the timing
resolution of the TAF to be one period of the clk signal, which guarantees zero timing skew between taps of the TAF. The TAF waveform generator is able to synthesize both lowpass and bandpass filter responses by passing or chopping the MUXed signal, respectively.

B. Preliminaries and Circuit Synthesis

The AMS filter uses 10 different circuit parameters and two performance metrics which are power and SFDR. The associated ANN model has 3 hidden fully-connected layers with 128, 256 and 128 neurons, respectively. In principle, the hyper-parameters (ANN structure, training epoch etc.) are chosen to minimize the testing loss and prevent over-fitting. We randomly sample the parameter space to generate the training dataset for the ANN. As shown in Fig. 9, the surrogate model can accurately predict the circuit performance when sufficient training samples are guaranteed. In this example, we use 5,500 training samples from schematic simulations.

Next, LTL is applied to generate the post-layout P2M model of the circuit. We generate designs via random sampling, employ the proposed mixed-signal layout flow to obtain the corresponding layouts, and use the post-layout simulation results as metrics to train the layout-aware ANN model. With a less number of training samples (i.e. 800 samples from post-layout simulations), LTL achieves a much lower testing error compared to an ANN that is trained from scratch, as shown in Fig. 10. Note that the ANN model is only prepared once and then used for designing various AMS filters.

Based on this layout-aware ANN model, the circuit sizing is automated using the gradient-based search algorithm in combination with parallel Monte Carlo. For 10 different target specifications, this experiment takes less than 34 seconds to finish the parameter search with a six-core 2.60GHz CPU and a 32GB RAM. Given the design parameter, the proposed layout generator takes around 30s to generate the layout of the single-channel TAF, and around 10s to finish the P&R for the eight-way TI TAF.

C. SPICE Validation of the Synthesized AMS Filter

The performance of two representative TAF designs in 65nm CMOS process with different specifications is summarized in Table I. Each design is selected from 10 candidates that meet the design specifications. The circuits are designed and laid out automatically via the aforementioned automation techniques. The results are obtained via post-layout simulations with the SPICE model. With the proposed mixed-signal layout flow, the TAF waveform generator is able to operate faster than 2.4GHz (F_TAF). Decent DAC linearity and stopband attenuation are also achieved given the power and area budgets.

Fig. 11(a)-(b) show the generated layout for the two designs. The simulated filter transfer functions are shown in Fig. 11(c)-(d). The filter herein aims to suppress the noise at a specific band of interest (target band) with a deep attenuation. A target CT FIR filter response is first designed based on the filter specification, and then loss function (5) is applied to maximize the difference of integrated energy between the signal band and the target band. The TAF performance comparison between the knowledge-based [3] and the proposed hybrid

---

**TABLE I: Performance Summary**

| Design | DAC Res. (bits) | F_s (MHz) | BW (MHz) | F_max (GHz) | Corner Freq. (GHz) | Attenu. (dB) | Power [uW] | Area [mm²] |
|--------|----------------|-----------|----------|-------------|-------------------|-------------|------------|-----------|
| Design 1 | 6 | 300 | 20 | 2.4 | 49 | 21 | 20 | 6.9 | 0.044 |
| Design 2 | 8 | 200 | 10 | 1.6 | 51 | 14 | 18 | 5.2 | 0.089 |

* Corner frequency of the TAF's frequency response.
** Stop-band attenuation of the TAF.

---

**TABLE II: Performance Comparison**

| Design | Design 1 | Design 2 |
|--------|----------|----------|
| **KB** | Hybrid Appr. | KB** | Hybrid Appr. |
| Attenuation (dB) | 21.3 | 28.8 | 21.7 | 31 |
| BW with >20dB attenuation (MHz) | 24.1 | 63.5 | 19.7 | 42.7 |
| BW with >20dB attenuation (MHz) | 12 | 46.58 | 7.62 | 32.7 |

* Average attenuation of the TAF at the target band.
** Knowledge-based time approximation scheme proposed in [3].
time-approximation schemes is summarized in TABLE II. The proposed technique shows more than 7.5dB improvement on noise attenuation and 2.2X to 4.3X bandwidth enhancement given the attenuation specifications. To prove the flexibility of the proposed AMS filter, we use TAF to synthesize another filter response with lower corner frequency and wider stopband attenuation. The simulated transfer functions of the filter are shown in Fig.12. The filter’s impulse responses are designed to generally filter the out-of-band noise with decent attenuation. In this case, loss function (2) is used to reduce the magnitude difference between the frequency responses of the target AMS filter and the TAF. To validate the bandpass mode or mixing mode of the filter in the context of a wireless transmitter, we applied a 10-MHz modulated signal at 256 QAM as the input of the filter. The simulated spectra of the modulated signal at the baseband and RF band are shown in Fig.13. Deep noise reduction at the desired bands is achieved via lowpass and bandpass filtering, thus proving the dual-mode operation capability of the filter. Different carrier frequencies are swept around 2.4GHz, which shows the flexibility of the system thanks to the mostly digital architecture.

V. CONCLUSION

To address the increasing demand of AMS filter and its design challenges, this paper presented a new way of designing AMS FIR filter, featuring a time approximation architecture with associated hybrid optimization scheme for filter’s impulse response and an AMS circuit design automation flow that combines a layout-aware ANN model and a gradient-based search algorithm. The fully synthesized AMS filters achieved high stopband attenuation and the proposed framework demonstrated flexibility with various filter specifications.

ACKNOWLEDGMENT

The work is supported in part by DARPA ERI POSH program under Grant FA8650-18-2-7853 and in part by GlobalFoundries. The authors would like to thank Prof. Anthony F. J. Levi and Prof. Sandeep K. Gupta from the University of Southern California for technical discussions.

REFERENCES

[1] R. Bhat, J. Zhou, and H. Krishnaswamy, “Wideband mixed-domain multi-tap finite-impulse response filtering of out-of-band noise floor in watt-class digital transmitters,” IEEE Journal of Solid-State Circuits, vol. 52, no. 12, pp. 3405–3420, 2017.
[2] W. M. Gaber, P. Wambacq, J. Craninckx, and M. Ingels, “A CMOS IQ direct digital RF modulator with embedded RF FIR-based quantization noise filter,” in 2011 Proceedings of the ESSCIRC (ESSCIRC). IEEE, 2011, pp. 139–142.
[3] S. Su and M. S.-W. Chen, “A time-approximation filter for direct RF transmitter,” IEEE Journal of Solid-State Circuits, pp. 1–1, 2020.
[4] B. Xu, S. Li, N. Sun, and D. Z. Pan, “A scaling compatible, synthesis friendly VCO-based delta-sigma ADC design and synthesis methodology,” in 2017 54th ACM/EDAC/IEEE Design Automation Conference (DAC). IEEE, 2017, pp. 1–6.
[5] W. Deng, D. Yang, T. Ueno, T. Siriburana, S. Kondo, K. Okada, and A. Matsuzawa, “A fully synthesizable all-digital PLL with interpolative phase coupled oscillator, current-output DAC, and fine-resolution digital varactor using gated edge injection technique,” IEEE Journal of Solid-State Circuits, vol. 50, no. 1, pp. 68–80, 2014.
[6] Q. Zhang, S. Su, C.-R. Ho, and M. S.-W. Chen, “A fractional-N digital PLL, with background two-point DTC calibration achieving 66dBc fractional spur,” in 2021 IEEE International Solid-State Circuits Conference (ISSCC), vol. 64, 2021, pp. 410–412.
[7] Z. Chen, H. Zhou, and J. Gu, “Digital compatible synthesis, placement and implementation of mixed-signal time-domain computing,” in 2019 56th ACM/IEEE Design Automation Conference (DAC). IEEE, 2019, pp. 1–6.
[8] J. Liu, A. Fahmy, T. Kim, and N. Maghari, “A fully synthesized 0.4V 77dB SFDR reprogrammable SRMC filter using digital standard cells,” in 2015 IEEE Custom Integrated Circuits Conference (CICC). IEEE, 2015, pp. 1–4.
[9] M. Hassanpourghadi, R. A. Rasul, and M. S.-W. Chen, “A module-linking graph assisted hybrid optimization framework for custom analog and mixed-signal circuit parameter synthesis,” ACM Transactions on Design Automation of Electronic Systems (TODAES), vol. 26, no. 5, pp. 1–22, 2021.
[10] Y. Li, Y. Wang, Y. Li, R. Zhou, and Z. Lin, “An artificial neural network assisted optimization system for analog design space exploration,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 39, no. 10, pp. 2640–2653, 2020.
[11] Q. Zhang, S. Su, J. Liu, and M. S.-W. Chen, “CEPA: CNN-based early performance assertion scheme for analog and mixed-signal circuit simulation,” in 2020 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). ACM, 2020.
[12] J. Liu, M. Hassanpourghadi, Q. Zhang, S. Su, and M. S.-W. Chen, “Transfer learning with bayesian optimization-aided sampling for efficient ans circuit modeling,” in 2020 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). ACM, 2020.
[13] J. Crossley, A. Puggelli, H.-P. Le, B. Yang, R. Nancollas, K. Jung, L. Kong, N. Narevsky, Y. Lu, N. Sutardja et al., “BAG: A designer-oriented integrated framework for the development of AMS circuit generators,” in 2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). IEEE, 2015, pp. 74–81.
[14] M. Ding, G. Chen, P. Harpe, B. Busze, Y.-H. Liu, C. Bachmann, K. Philips, and A. van Roermund, “A circuit-design-driven tool with a hybrid automation approach for SAR ADCs in IoT,” in 2018 Design, Automation & Test in Europe Conference & Exhibition (DATE). IEEE, 2018, pp. 672–675.
[15] B. Xu, K. Zhu, M. Liu, Y. Lin, S. Li, X. Tang, N. Sun, and D. Z. Pan, “Magical: Toward fully automated analog ic layout leveraging human and machine intelligence,” in 2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). IEEE, 2019, pp. 1–8.
[16] K. Kunal, M. Madhusudan, A. K. Sharma, W. Xu, S. M. Burns, R. Harjani, J. Hu, D. A. Kirkpatrick, and S. Sapatnekar, “ALIGN: Open-source analog layout automation from the ground up,” in Proceedings of the 56th Annual Design Automation Conference 2019, 2019, pp. 1–4.