Soft-switching modulation of the multilevel cascaded H-bridge inverter under DC source fault

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Abstract
Cascaded H-bridge inverter (CHBI) is widely used in the industry application for its outstanding features. However, CHBI needs a large number of isolated DC sources. If some of the DC sources are out of work, the DC voltage cannot maintain the desired value and even decreases to zero, thus degrading the quality of the output voltage of the CHBI. Thus, a soft-switching modulation strategy based on the carrier phase shift SPWM is proposed in this paper to cope with the DC source failure. The strategy is proposed to achieve two goals: 1) one is to adjust the DC voltage of faulty cells back to the normal; 2) the other one is to make the pulse width modulation (PWM) pulses of each cell change without cell voltage level-skip. The correction and efficiency are verified by a prototype of three-cell CHBI built in the laboratory.

1 | INTRODUCTION

Multilevel converters have been widely applied in the industry because they can provide a cost-effective solution in the medium/high-voltage energy management systems [1–5]. There are four typical multilevel converter topologies which are neutral-point clamped converter (NPC), flying capacitor converter (FCC), cascaded topologies (Cascaded Half-Bridge: MMC; Cascaded H-Bridge: CHB) and hybrid multilevel converter (HMC). For NPC and FCC structures, a large number of additional clamping diodes and flying capacitors are needed because of the increasing requirement of the output voltage level. These clamping diodes and flying capacitors not only increase the total cost but also the packaging issue [6]. HMC, composed of two of the NPC, FCC or CHB, has attracted the attention in some applications such as the active NPC [7], nest NPC and three-level T-type converter [8], etc. The HMC possesses some good performances, but some demerits, such as unequal usage of switches and flying capacitors, unequal blocking voltage of switches and not suitable for high-voltage range, have limited its application. So, compared with the NPC, FC and HMC, the CHB converter (CHBC) has been implemented more widely with its advantages such as lowest devices count, modularity, low total harmonic distortion (THD), reduced voltage stress on the switches, fault-tolerant operation and better electromagnetic compatibility.

In the early time, CHBC was mainly applied in the field of pump, fans, conveyors, kneaders, compressors, mixers, crushers, extruders in the medium-voltage range [9]. In recent years, CHBC has played an important role in high voltage, high power applications like renewable energy system (photovoltaic (PV)/wind power-conversion) [10], power electronic traction transformer [11–12] or solid-state transformer [13], advanced traction power supply system [14] and active filter and reactive power compensation applications [15]. With the rapid development of the electric vehicle technology, CHBC can be applied in the electric vehicle industry because it is a competitive and promising topology [16], [17]. In these applications, the CHBC is selected as the rectifier or the inverter, and this paper focuses on the CHB inverter (CHBI) topology. The CHBI appeared first in 1988 [18]. It was well developed during the 1990s and attracted more interest after 1997 [19], [20]. During the past decades, scholars and engineers have carried out many meaningful studies about CHBI which can be concluded as the following three aspects: 1) improving the harmonic performance [21–23]; 2) solving the computational burden to improve the dynamic response [24–26]; 3) balancing the DC voltage and developing fault-tolerant control (detection, isolation and reconfiguration) to improve system reliability, maintainability and survivability [27–36]. Especially for the third aspect, the hardware redundancy and software redundancy [37] are the two efficient and main stream solutions. Specifically, in [27], a neural
network is employed to detect an open-circuit fault, identify the fault location and reconfigure the output voltage of the single-phase three-level NPC cascaded inverter after the fault module is bypassed. In [28], a novel auxiliary hardware circuit system is proposed to balance the DC voltage in a multilevel converter. The converter can maintain its function when one DC module is faulty. However, the additional hardware not only increases the volume of system, but also decreases the transmission efficiency, which is not suitable for industry applications. In [29], a voltage-balancing method for modular multilevel converters is proposed to balance the capacitor voltage in each cell. However, the method is not suitable for CHBC due to its special structure. In [30], a modified control strategy based on a CHB rectifier is proposed to solve the unbalanced DC voltage. The cost function and mathematical model are established in the control strategy. When the CHB rectifier works, the controller will process the complex calculations. However, the complexity of mathematical operation is much greater than that of digital operation. Thus, a compromise must be made between the cell numbers and dynamic response. In [31], an alternative 3-D modulation-based solution is proposed for CHBC. The calculation burden of the controller is avoided and the fault-tolerant capability is maintained. However, it is not suitable for any number of the cascaded modules of CHB. In [32], a modulation-based strategy with opposite vectors is proposed. This solution provides great fault-tolerant capability but also produces voltage-level-skip. In order to ensure the smooth change of voltage level, a fault-tolerant strategy with fixed and smooth switching states is proposed in [33]. However, this strategy increases the calculation burden under the situation of a great number of cascaded cells. In [34], the flywheels are connected to the DC side of the inverter powered by the wind generator and the control strategy is mainly to regulate the DC voltage fluctuation. In [35], the parallel interleaved voltage source converters (VSCs) share one common DC voltage and make effort to solve the circulating current. In [36], the optimal control strategy for the grid-side inverter in wind energy conversion systems is proposed to improve the dynamic response, suppress the harmonics and enhance the robustness to grid filter parameters.

As can be seen from the above analysis of voltage balance and fault-tolerant control, the published papers mainly dealt with the small voltage fluctuation between per cell or per phase and the open-circuits or short-circuits of the components which includes the electrolytic capacitors, switching devices (IGBTs, MOSFETs) because they are the most fragile and critical part of the CHBC. However, the CHBI has another special issue because it is composed of \( n \) power cells in series connection and each cell has a separated DC source. Specifically, the DC source can be obtained by: 1) a three-phase (or single-phase) diode-based or pulse width modulation (PWM)-based rectifier [38]; 2) PV solar panels with isolated DC-DC converters [39]; 3) power electronic transformer with separated dc-link topology [12]; 4) batteries or fuel cells. Some of these DC sources could possibly fail in work on many occasions. For example, diode/PWM-based rectifiers are prone to breakdown because of the complication in their structure and operating conditions, as well as their high electrical stress [40]; the solar radiation on one PV panel is near to zero caused by the uncertain meteorological conditions, so the corresponding dc voltage decreases to zero [41], [42]. Once the DC source is in failure, the DC voltage of the capacitor cannot maintain the stable voltage and even decreases to zero. The DC source failure can extremely burden the filter and degrade the output AC voltage with high distortion and imbalance.

Therefore, the fault-tolerant control of the CHBI under DC source failure needs to be studied urgently. However, to the best of our knowledge no work has been done to solve the DC sources failure issue. Thus, in this paper, a soft-switching modulation strategy (SSMS) is proposed for CHBI, to keep the DC voltage balance while the DC-source is faulty and avoid the voltage level-skip. The structure of the article is as the followings. In Section 2, the system configuration and control strategy are introduced. In Section 3, the DC source fault and operation mode are analysed. In addition, the optimal modulation strategy and the balanced boundary are calculated in this section. In Section 4, the simulation and the low power experimental test are established to verify the correctness and effectiveness of the proposed strategy. Finally, the conclusions of this paper are summarised in Section 5.

## 2 SYSTEM CONFIGURATION

### 2.1 Topology

The topology of the n-cell CHBI is shown in Figure 1. As an inverter topology, each inverter cell is powered by an individual DC source with the same value \( V_{dc1} = \ldots = V_{dcn}, \) \( n \) is the total number of the cells. \( C_i \) is the DC-link capacitor, \( L_i \) is the filter inductor and \( R \) is the load; \( u_i \) is the output voltage of each cell and can be one of \( V_{dc}, \) \( V_{dc} \) \( \pm, -V_{dc} \); \( u \) is the total output voltage described as equation (1)

\[
\begin{align*}
\frac{du}{dt} &= i \cdot R + \sum_{j=1}^{n} \frac{du_j}{dt} \\
\frac{du_j}{dt} &= \sum_{j=1}^{n} S_{ij} \cdot V_{dc} \\
u_i &= S_{ij} \cdot V_{dc}
\end{align*}
\]  

(1)

where \( S_{ij} \) is the switch state of cell \( i \). As is shown in Figure 2 and taking the cell \( i \) in Figure 1 as an example, based on the
different switch state of the four IGBTs, $S_i$, can be concluded as equation (2)

$$S_i = \begin{cases} 
1, & [S_{i1} \text{ and } S_{i4} \text{ on}; S_{i2} \text{ and } S_{i3} \text{ off}] \\
0, & [S_{i1} \text{ and } S_{i3} \text{ on}; S_{i2} \text{ and } S_{i4} \text{ off}] \text{ or} \\
[S_{i2} \text{ and } S_{i4} \text{ on}; S_{i1} \text{ and } S_{i3} \text{ off}] \\
-1, & [S_{i2} \text{ and } S_{i3} \text{ on}; S_{i1} \text{ and } S_{i4} \text{ off}] 
\end{cases}$$

where ‘1’ and ‘−1’ represent the ‘on’ state of the cell with output voltage $+V_{dc}$ (Figure 2(a)) and $-V_{dc}$ (Figure 2(d)), respectively; ‘0’ represents the ‘off’ state of the cell with output voltage 0 (Figure 2(b) and (c)).

2.2 The control strategy and the modulation algorithm

The control strategy and the modulation algorithm are shown in the yellow block and purple block in Figure 3, respectively. In order to ensure that the CHBI generates the desired output voltage and fast response to the load change, voltage and current double closed-loop control strategies are adopted. First, the root-mean-square value $U_{\text{rms}}$ of $i$ is compared with the reference voltage $U_{\text{ref}}$. Second, the error of the $U_{\text{rms}}$ and $U_{\text{ref}}$ is sent to the PI controller to generate the reference current $i_s^\ast$. Third, the reference current $i_s^\ast$ is compared with the output current $i_s$ to get the error signal $\Delta i_s$. Finally, the modulation signal $u_{\text{ref}}$ is the value obtained by multiplying $K_{ip}$ and $\Delta i_s$.

The carrier phase-shifted SPWM (CPS-SPWM) is used as the modulation algorithm. The highlighted advantage of CPS-SPWM is that it can provide an even power distribution among the cells, and the phase of each carrier is shifted by this modulation at a proper angle to reduce the harmonics in the output voltage. In the traditional modulation algorithm, once the modulation signal is obtained, the PWM switch signals are calculated through the CPS-SPWM which are depicted in the green-dashed block in Figure 3 as PWM1', PWM2', …, PWM $n'$. These PWM pulses are sent to trigger the corresponding IGBTs.

With such a control strategy and traditional modulation algorithm, the CHBI can provide stable output voltage if there are no faulty DC sources. In this paper, the SSMS is proposed as is shown in the red-dashed block in Figure 3. The proposed SSMS is adopted to enhance the performance of the CHBI when some of the DC sources are at fault. This optimal method will be analysed in the next part.

3 DC SOURCE FAULT ANALYSIS

3.1 The topology of the DC source

Figure 4 depicts some typical DC source topologies in the industry application. Figure 4(a) shows the PWM-based rectifier, of which the main advantages are bidirectional power flow and full controllability. Figure 4(b) illustrates the diode-based rectifier. This type is easy to put into implementation and less expensive. Figure 4(c) shows a typical DC source used in the CHBI grid-tied PV systems. Here, $n$ DC–DC converters share one common DC bus and the DC bus is connected to PV multi-string with individual maximum power point tracking DC–DC converter. Figure 4(d) introduces the battery arrays. In fact, the batteries are usually charged by the rectifiers or the DC–DC converters. Figure 4(e) and (f) depicts two practical applications in the advanced co-phase traction power supply system [14] and
the power electronic transformer [12], respectively. So, the DC sources are generally based on the power electronic devices which are prone to unexpected failure owing to their complex structure and operation conditions, as well as their high electrical stress. The failure will lead to abnormal operation and direct shut down of the DC sources. If one of the DC sources is out of work, the capacitor voltage of the corresponding cell cannot maintain a normal value, thus deteriorating the power quality of the output voltage of the CHBI. This section will analyse the DC source fault and an SSMS will be proposed to cope with the DC source fault and enhance the reliability of the CHBI.

### 3.2 Analysis of the DC source fault

Without loss of generality, assuming the DC source $i$ in Figure 1 is at fault that cannot maintain the corresponding capacitor voltage. The output power of cell $i$, supplying to the load and other cells, is defined as $P_i$:

$$P_i = S_i \cdot V_{dc} \cdot i_c.$$  

The positive, negative, or zero of $P_i$ is decided by the value of $S_i$ and $i_c$ since $V_{dc}$ is positive.

Figure 2(a)-(d) shows the four different current flow paths of cell $i$ and the detailed analysis will be given as the followings:

1. Figure 2(a) shows the state $S_i = 1 (1001)$. In this state, $P_i > 0$, the capacitor $C_i$ will be discharged when $i_c > 0$, and the capacitor voltage $u_{dc1}$ will decrease; when $i_c < 0$, $P_i < 0$, the capacitor voltage $u_{dc1}$ will increase.

2. Figure 2(b) and (c) shows the state $S_i = 0 (1010)$ and $S_i = 0 (0101)$, respectively. In these two states, the current will not pass through $C_i$, so the capacitor will neither be discharged nor charged. But considering the parasitic resistance and inductance of the capacitor $C_i$, the capacitor will lose its power slowly and the capacitor voltage will decrease slowly.

3. Figure 2(d) shows the state $S_i = -1 (0110)$. In this state, $P_i < 0$, the capacitor $C_i$ will be charged when $i_c > 0$, and the capacitor voltage $u_{dc1}$ will increase; when $i_c < 0$, $P_i > 0$, the capacitor voltage $u_{dc1}$ will decrease.

From the above analysis, obviously, the switch states $S_i = 1$ (1001) and $S_i = -1$ (0110) can change the capacitor voltage sharply. But for the switch states $S_i = 0$ (1010 or 0101), it cannot change the capacitor voltage. Based on the different four states, one can adjust the PWM signals of each cell to control the DC voltage of each capacitor which will be analysed in the next section.

### 3.3 The proposed optimal modulation strategy

Once the DC voltage $V_{dc1}, V_{dc2}, ..., V_{dcn}$ are sampled, a novel idea is to sort these DC voltages in ascending order. The cell with a lower DC voltage will receive a smaller rank number while the higher one will get the bigger rank number.

In order to get the enhanced and rapid voltage balance capability, the low voltage cells should be charged, meanwhile the high voltage cells should be discharged in a certain range. Thus, keeping the total output voltage the same, the cell with a smaller rank number should be arranged the switch state ‘1’ or ‘0’ if $i_c > 0$ and the cell with a bigger rank number should be arranged the switch state ‘1’ or ‘0’ if $i_c < 0$. Taking the three-cell CHBI as an example, the PWM signals are shown in Table 1. The DC voltages are ranked as $V_{dc1} > V_{dc2} > V_{dc3}$. In this way, the DC voltage of the faulty cell can be adjusted to the normal value; the cell with high DC voltage can be pulled back to the normal value. Hence, the DC voltage in each cell can keep balanced.

Table 2 shows the relationship between the switch state change and switch times. It is clear that the switch state change from ‘1’ to ‘0’ (‘0’ to ‘1’) has the maximum switch times. The unexpected cell port voltage level-skip will increase the switching frequency of the CHBI and the potential risk of misconduct of the switching devices. So, in order to avoid the unsmooth voltage level change, the soft switching modulation is necessary.

Based on the above analyses, a switching pair $S_{total}$ is defined to describe the switch state change of the CHBI

$$S_{total} = [S_1, S_2, S_3]$$
The balanced boundary of optimal modulation strategy

To find the boundary of DC voltage balance, the balance ability of SSMS needs to be calculated quantitatively which is important to evaluate the performance of the SSMS.

First, the unbalanced degree of the DC voltage is defined as $\Delta u_{dc}$ in (5). When CHBI is balanced, $\Delta u_{dc} = 0$

$$\Delta u_{dc} = u \cdot (u_{dc\text{-max}} - u_{dc\text{-min}}) \Big/ \sum_{i=1}^{n} u_{dcj} \quad (5)$$

when one cell of the CHBI is faulty, $\Delta u_{dc} = 1$; when several cells of the CHBI are faulty, $\Delta u_{dc}$ is in the range of 0 to 1. Thus, the most serious situation is described when one of the cells is faulty.

Second, the relationship between $\Delta u_{dc}$ and the unbalanced energy flow is built in (6), where $\Delta V_{dc}$ is the voltage difference of the faulty cell and the normal cell; $V_{dc}$ is the average value of the DC voltage; $\Delta W$ and $\Delta E$ are unbalanced power and energy of the faulty cell while the $W$ and $E$ are average power and energy of all cells

$$\Delta u_{dc} = \Delta V_{dc} / V_{dc} = \Delta W / W = \Delta E / E. \quad (6)$$

Third, $\Delta u_{dc}$ can be expressed to (7) by calculating the $\Delta W$ and $\Delta E$, respectively. In (7), the relationship between $\Delta u_{dc}$ and the modulation degree $m$ is established. $S_{\text{fault}}(t, m)$ is the voltage level of the faulty cell at the moment of $t$

$$\Delta u_{dc} = \Delta V_{dc} / V_{dc} = \Delta W / W = \int_{0}^{2\pi} V_{dc} \cdot S_{\text{fault}}(t, m) \, dt \Big/ \int_{0}^{2\pi} V_{dc} \cdot i \cdot \sin(\omega t) \, dt. \quad (7)$$

Finally, equation (7) can be calculated through the mathematical software and the relationship is illustrated in Figure 7. The simulation point and experimental point are marked in Figure 7. When $m < 0.81$, the most serious situation can be solved in CHBI, thus $\Delta u_{dc}$ can always remain zero and the CHBI is in a balanced region. However, when $m > 0.81$, the ability of DC voltage balance is decreased and the CHBI is in the unbalanced region. So, $m = 0.81$ is the critically balanced point.

Thus, the proposed SSMS aims to achieve two goals: one is to adjust the DC voltage of faulty cells back to the normal; the other one is to make the PWM pulses of every cell change smoothly without cell voltage level-skip (‘1’ to ‘−1’).

The optimal path of the proposed SSMS is shown in Figure 6(a)–(d), which represents the different total voltage level and energy flow direction. Figure 6(a) and (b) represents the opposite energy flow when the total voltage level is greater than zero while Figure 6(c) and (d) represents the different total voltage level when the total voltage level is lower than zero. As is clearly shown in Figure 6(a), three planes with different colours represent total voltage levels ‘0’, ‘1’, ‘2’, respectively. Once the total voltage level changes, the optimal and direct path will be selected and the voltage level-skip will be avoided. For example, the switching pair changes from (0, 1, 0) to (0, 0, 0), the change path is uniquely determined.

3.4 The balanced boundary of optimal modulation strategy

where each $S_{i}$ ($i = 1,2,3$) has three levels and the switching pair $S_{\text{total}}$ has altogether 27 possible combinations for three-cell CHBI. In this paper, a cube structure of voltage level for three-cell CHBI is designed as Figure 5. Each vertex stands for one switch pair. The dotted line represents the dynamic path between different switch pairs and the path change between any two vertexes can represent the voltage level change. For example, the red path means that the switching pair changes from (0, 1, 0) to (0, 0, 0), the change path is uniquely determined.

The optimal path of the proposed modulation strategy (a) $u > 0$, $u_{i} > 0$, (b) $u > 0$, $u_{i} < 0$, (c) $u < 0$, $u_{i} > 0$, (d) $u < 0$, $u_{i} < 0$

$\Delta u_{dc}$ can always remain zero and the CHBI is in a balanced region. However, when $m > 0.81$, the ability of DC voltage balance is decreased and the CHBI is in the unbalanced region. So, $m = 0.81$ is the critically balanced point.

Through setting the modulation degree as 0.78, 0.81 and 0.85, respectively, the boundary of the voltage balance is clearly described in Figure 7. If the modulation depth of control strategy
exceeds the limitation, the DC voltage of CHBI will be out of control.

4 SIMULATION TEST

A three-cell two-level neutral point clamped cascaded inverter system has been established by Matlab/Simulink. In this section, cell 3 is simulated with different DC source conditions and different modulation depths. In this way, the optimal modulation strategy is validated. Considering the balanced boundary of the proposed strategy, the modulation depth change from 0.78, 0.81 to 0.85 as three typical values, the corresponding system is balanced, critically balanced, and unbalanced, respectively. The simulation parameters are shown in Table 3.

### Table 3 The parameters of the simulation

| Parameter name     | Parameter value |
|--------------------|-----------------|
| Number of cells    | 3               |
| Input power source | 48 V            |
| DC-link capacitor  | 470 µF          |
| Inductance of LC filter | 5 mL         |
| Capacitance of LC filter | 10 µF      |
| Load R             | 50 Ω            |
| Switching frequency| 2 kHz           |

4.1 The start-up with cell 3 suffering from the DC source fault

The seamless start-up is an important requirement for the CHBI under DC source fault condition, hence, it is necessary to evaluate the system’s behaviour at the start period.

In this test, cell 3 starts with no input power source while the other two cells start with a 48-V power source. Figure 8 shows the DC voltages of each cell and AC current waveforms during the start-up and stable period.

In Figure 8(a), the modulation depth $m$ is 0.78 and the system is in the balanced boundary. In the start-up period, due to the application of SSMS, $V_{dc3}$ converges rapidly with $V_{dc1}$ and $V_{dc2}$ from 0 to 48 V with a small ripple. The system enters the stable period at 0.27 s, and it is a remarkable fact that the DC voltages of all three cells are at 48 V during the stable period. This result indicates that if the modulation depth $m$ is in the balanced region, the optimal modulation strategy can effectively adjust and hold the DC voltage of the fault cell at normal value with a very small deviation.

In Figure 8(b), $m = 0.81$ and the system is in a critically balanced region. Although three DC voltages stick together at a stable period, the system takes a longer time to enter the stable period. Besides, the dynamic response of $V_{dc3}$ gets worse and its value deviates to 47 V. In Figure 8(c), $m = 0.85$ and the system is in an unbalanced region. It takes a much longer time for the system to enter a stable period. More importantly, the DC voltage of cell 3 deviates seriously to 42 V. From these two tests, one can know that an unsuitable value of modulation depth $m$ can excite unstable voltage deviation and deteriorate the performance of CHBI in the start-up and stable period.

Comparing the differences in Figure 8(a)-(c), the theoretical analysis of the balanced boundary is strongly proved and
the SSMS features good fault-tolerant ability in the balance region. The AC current approximates the sine wave in all three figures.

4.2 The output voltage with different modulation depths

In order to look insight into the modulation procedure, this test will focus on the output voltage of each cell and the total output voltage under different modulation depths as is shown in Figure 9. Cell 3 is the faulty cell without the input DC source.

First, as can be seen from Figure 9(a)-(c), although the output voltages of each cell are no longer standard staircase-waveforms, a normal seven-step-waveform output voltage $u$ is promised, which indicates that the SSMS can make the output voltage synthesise normally even in a faulty condition. Second, taking the first positive half-cycle (red-dashed block) in Figure 9(a) as an example, the total output voltage $u$ is decided by the reference signal from the SSMS. Since the DC voltage of cell 1 and 2 is bigger than that of cell 3 and under the constraint that the output voltage of cell 1, 2 and 3 must synthesise the total output voltage, the SSMS tries to arrange switch state ‘1’ to cell 1 and 2, and switch state ‘−1’ and ‘0’ to cell 3. Further, comparing Figure 9(a)-(c), with the increase of modulation depth $m$, cell 1 and cell 2 produce a growing number of switch state ‘1’, while cell 3 produces a growing number of switch states ‘−1’ and ‘0’ in the positive half-cycle, vice versa. This is because switch states ‘−1’ could apply the stronger voltage recovery ability and ‘0’ could stop the power loss of the capacitor according to the analysis in 3.2. The output voltage of cell 3 adjusts quickly to synthesise different voltage levels of the total output voltage. Third, from Figure 9(a)-(c), one can know that there is no voltage level-skip in the output voltage of cell 1, 2 and 3. The above analysis, strongly proves that the SSMS can pull back the voltage of fault cell without any voltage level-skip.
FIGURE 11  The prototype of three-cell single-phase CHBI. CHBI, Cascaded H-bridge inverter

TABLE 4  The parameters of the experimental test

| Parameter name          | Parameter value | Numbers |
|------------------------|-----------------|---------|
| DC-link voltage        | 48 V            | 3       |
| IGBT                   | IHW20N120R      | 12      |
| FPGA                   | EP3C55F484C8    | 1       |
| Voltage sensor         | LV-25-P         | 4       |
| Current sensor         | LA-25-NP        | 1       |
| Carrier wave frequency | 2000 Hz         | –       |
| DC-link capacitor      | 470 µF          | 3       |
| Inductance of LC       | 5 mH            | 1       |
| Capacitance of LC      | 10 µF           | 1       |
| Load R                 | 50 Ω            | 1       |
| Number of modules      | 3               | –       |

4.3  DC source fault during steady-state operation

In the field application, usually, the DC sources tend to lose their power suddenly, therefore, verifying the dynamic response of the CHBI under the sudden change of DC sources is important. As shown in Figure 10, the DC voltages present different steady-state characteristics due to different modulation depths. From Figure 10(a)-(c), the input power source of cell 3 presents a sudden change at 0.4 s from the balanced input power source ($V_{dc3} = 48$ V) to no input power source ($V_{dc3} = 0$).

As illustrated in Figure 10(a), the DC voltages hardly have any disturbance at the sudden change. Since the system is in the balanced boundary, $V_{dc3}$ follows the track of $V_{dc1}$ and $V_{dc2}$ and oscillates only 0.3 V after the sudden change. In Figure 10(b), $V_{dc3}$ is parallel to the other two waveforms after the sudden change and oscillates approximately 1.1 V, which indicates that the system is critically balanced. In Figure 10(c), the modulation depth increases to 0.85 and the system is out of the balanced boundary, $V_{dc3}$ diverges away from the other two waveforms after the sudden change. Besides, along with the increase of modulation depth, the fluctuation of voltage gradually gets bigger. In this way, the voltage balanced boundary is, again, validated. Within the balanced region, the SSMS can maintain the DC voltage of the fault cell when a sudden DC power loss happens during normal operation. The AC current approximates the sine wave in all three figures.

5  LOW POWER EXPERIMENTAL TEST

To further validate the proposed SSMS, a prototype of three-cell CHBI is built in the laboratory. The hardware picture and circuit configuration of the experimental platform are shown in Figure 11. Three AC–DC rectifiers are applied as the DC source of the three cells, respectively. The control and modulation strategy are implemented into the EP3C55F484C8 FPGA chip. The waveforms are recorded by the digital storage oscilloscope (TEKTRONIX TPS2014B). The rest experiment parameters are listed in Table 4.

The first experimental test is carried out to evaluate the steady-state performance without any faults as is illustrated in Figure 12. The output voltage waveform of each cell has three levels and the output current is sinusoidal. More importantly, as can be seen from the red-dashed block, there is no voltage level-skip. Between the switch state ‘0’ and ‘−1’, the optimal modulation strategy can provide a short state of ‘0’, thereby ensuring
that the output voltage changes smoothly. So, with the proposed SSMS, CHBI operates well in a steady state and reaches the goal of smoothing the PWM switching pulses.

Next, a dedicated experimental start-up test is designed to show the start-up characteristics of the real CHBI and the modulation depth is 0.8. Compared with the simulated start-up test, in the experimental test, considering the worst case, the DC source of cells 1, 2 and 3 are all turned off before start-up. So the voltage of the three capacitors is 0. When the test starts, only DC source of cell 2 and 3 are turned on and that of cell 1 keeps the previous state to simulate the fault operation mode. Figure 13(a) shows the adjustment of the three DC voltages: $u_{dc1}$, $u_{dc2}$, $u_{dc3}$ in the post-fault reconfiguration mode. Obviously, the capacitors of cell 2 and cell 3 are charged quickly. After about 0.03 s, the DC voltage of cell 2 and cell 3 reaches and maintains at 48 V. However, for cell 1, it takes a longer time (0.22 s) to reach the normal value with very small fluctuation. Figure 13(b) illustrates the further comparison of the DC voltage with the same reference line. It can be seen that the DC voltage of the faulty cell and the other two normal cells is almost the same. This result proves that the SSMS can effectively adjust the serious unbalanced voltage (DC voltage of cell 1 is 0) to the normal value. Figure 13(c) demonstrates the output voltage of cell 1, 2 and 3. Because of the slow adjustment of the DC voltage of the cell 1, its output voltage increases gradually to the same value as cells 2 and 3. It is worth to note that the switching times increase in the faulty cell 1 to maintain the DC voltage because of the proposed SSMS. Moreover, there is no voltage level-skip in all the output voltage especially for the faulty cell. Figure 13(d) depicts the DC voltage of faulty cell 1, the output voltage of faulty cell 1 and total output voltage of CHBI. With the same increase trend, the total output voltage of the CHBI increases gradually to the steady state. From Figure 13(c)-(d), one can know that though the switch states of the three cells are rearranged, the total output voltage of CHBI keeps unchanged in steady state. In addition, the output current remains sinusoidal all the time.

Then, to explore the dynamic performance of the CHBI experimentally, a dedicated test is set up. This test is similar to the simulation test in 4.3 while the DC voltage of cell 1 is set higher than cells 2 and 3 intentionally to clearly observe the dynamic rearrangement of the output voltage of each cell. As is shown in Figure 14(a), before turning off the DC source of cell 1, the output voltage of cell 2 and 3 adjust quickly in order to maintain the same DC voltage as cell 1. Once the DC source of cell 1 is turned off, oppositely, the switching times of cell 1 increases sharply to hold the DC voltage. In Figure 14(b), when the DC source of cell 1 is turned off, its DC voltage decreases but soon maintains at the normal value with small fluctuation. The total output voltage of CHBI keeps unchanged and the output current remains sinusoidal all the time. The practical dynamic test reveals that the proposed SSMS is robust to the power loss of the DC source, suggesting that CHBI using SSMS can adapt to complex operation conditions.

Using the THD as the criterion, the last experiment test is dedicated to verify the harmonics suppression ability under faulty conditions. The THD of total output voltage in the normal operation mode, fault operation mode and post-fault reconfiguration mode is measured in Figure 15(a)-(c), respectively. The THD of normal operation mode is 16.7%, while the THD increases to 35.9% in the fault operation mode. When the SSMS is adopted in the post-fault reconfiguration mode, the THD decreases to 17.3% from 35.9%, which considerably alleviates the harmonic distortion. It is worth to note that the proposed SSMS fails to suppress the THD to the normal value but it is acceptable because the main purpose of the proposed SSMS is to make the system continuously operates during the fault until the faulty DC sources are repaired, thus ensuring the continuous and reliable power supply.

6 Conclusion

In this paper, a soft switching modulation strategy applied in CHBI is proposed, which can successfully solve the problem of
seriously unbalanced voltage between cells. The superiorities of the proposed strategy are as follows.

(1) When modulation degree is smaller than 0.81 (calculated by the simulation and experimental parameters in this paper), the voltage balance can be definitely maintained even if one of the DC sources is faulty. When modulation degree is over 0.81, the boundary of voltage balance is accurately calculated and intuitively represented, which promises the strong ability of voltage balance.

(2) The cube structure of the voltage level is proposed which establishes a novel perspective to observe the state of voltage balance. Through choosing the optimal path to change the voltage level, voltage level-skip is forbidden while the strong ability of voltage balance is obtained.

(3) According to the simulation and experimental results, the outstanding dynamic performance of the proposed strategy is obtained. When the system starts from the DC source faulty condition, the DC voltage of each cell returns to balance after only 0.22 s. When one cell is faulty and cut off, the power quality of the output current is smooth without any obvious distortion.

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