Integration of Indium Phosphide Thin Film Structures on Silicon Substrates by Direct Wafer Bonding

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Abstract. Wafer bonding or wafer fusion is a method of combining two same or dissimilar materials, either atomically or by means of adhesive. In this paper we report a new process to bond thin film Indium Phosphide (InP) to oxidized Silicon (100) substrates at low temperatures (>250°C). The treatment of InP epitaxial structures to oxygen plasma and the Si substrate to chemical treatment aids the substrates in contact bonding at room temperature. A thermal treatment at 220°C, completes the wafer fusion, with uniform bonding occurring along the length and breadth of the sample. The InP substrate is removed, resulting in a thin film of two micron InP bonded to oxidized Si. The InP thin film was studied for its structural and optical quality by high-resolution scanning electron microscopy, micro-PL and micro-Raman. The thin-film exhibited excellent quality and was patterned and released to form cantilever structures, showing the process capability of integrating free-standing III-V thin-films on Si platform.

Keywords: wafer-bonding; oxygen plasma; III-V; cantilevers;

1. Introduction
Wafer bonding has attracted much attention recently because of the important application in “micro-electrical-mechanical systems (MEMS)" and “silicon-on-insulator (SOI) technology 3,4”. Wafer bonding usually requires high-temperature annealing above 1000°C for Si systems and 650°C for III-V systems to achieve strong bonding between the wafers. Wafer bonding is an alternate for heteroepitaxy. When dissimilar materials are grown, the interface is resided with defects and dislocations, due to the different thermal and lattice expansion coefficients of the materials. Under such circumstances wafer bonding is very useful to produce good quality epitaxial layers on dissimilar substrates. Though there are many techniques to perform wafer bonding, temperature is a major issue. Successful wafer bonding of “III-V’s with Si takes place between 500 to 650°C5,6”. But this high temperature range and long annealing time has detrimental effects at the interface, in terms of electrical conductivity and subsequent device fabrication. Also such process may not be well suited for MEMS applications. Another method of wafer bonding is adhesive wafer bonding, in which the materials to be joined together are “bonded using polymers such as BCB etc.,7”. Though the bonding temperature is low, difficulties arise when the bonded material are subjected to dry or wet etching,
during MEMS structuring, leading to debonding of the interface. Therefore, it is mandatory to find a
direct low temperature bonding process that result in robust bonding at temperature below 300°C.

There are many new low temperature wafer bonding processes of which plasma-assisted bonding,
is gaining much attention because of the high yield in reproducibility and relatively “high bond
strength at low temperatures”. The use of plasma treatment of wafers before bonding results in high
surface energies. There are published results on wafer bonding experiments using plasma
pretreatments in a variety of plasma systems. For instance, reports are available on the use of barrel
reactors, reactive ion etchers (RIE), and RIE with inductively coupled plasmas (ICP-RIE). Some
authors report surface energies above 1 J m⁻² after storage at room temperature, while other authors
report the need for a low temperature annealing to increase the surface energy. Though plasma assisted
bonding results in enhanced bond strength, the effects of plasma activation are not fully clarified yet.
Identification of the actual bonding mechanism will require improved knowledge of the properties of
the oxygen plasma treated surfaces. It was recently proposed that the dramatically enhanced dynamics
of the strong bond formation at room temperature could be explained by the formation of a “porous
surface layer during the plasma exposure of the wafer”.

In this paper we report on a process to bond thin films of InP to oxidized silicon, in which the oxide
along with Si substrate later serves as sacrificial layers for etching to realize cantilever structures of
InP. During the process, the thin film of InP were characterized by high resolution scanning electron
microscopy (FESEM), photoluminscence (PL) and micro-Raman to reveal its structural and optical
quality.

2. Experimental

In the experiments, <100> oriented p-type Czochralski grown silicon wafers with 12mm x12mm and
InP epitaxial structure of dimensions 8mm x 8mm were used. All samples were cleaned in organic
solvents and oxide stripped in 5%HF for one minute (step 1). An oxide layer with a thickness of
200nm was grown on Si by wet chemical mixture (H₂SO₄:H₂O₂) (5:2) for ten minutes at 100°C.
Simultaneously InP epilayer structure was exposed to O₂ plasma in a reactive ion etcher for 30 secs.
(step 2) During the plasma exposure the chamber pressure was 90mTorr, with the gas flow set at
100sccm, with a bias voltage of 495V. Following this, Si samples were placed in H₂O₂ and InP in H₂O
for ten minutes respectively (step 3). The samples were removed and blow dried using N₂ gas. When
InP samples were placed on Si, it immediately contact bonded by the formation of covalent bonds. The
wafer bonding was done at 220°C for 45 minutes with a force of 80N inside a Karl Suss wafer bonder
(step 4). The entire process is shown in figure 1. To remove the InP bulk substrate, InP was lapped to
75μm and then removed by wet chemical etching HCl:H₂O (1:1) (step 5).
This stops at the InGaAs layer, which is later removed by etching in FeCl₃ (step 6), to have two micron of InP bonded to Si. The cantilever patterns were structured on InP using lithography, followed by dry-etching in HBr chemistry.

3. Results and Discussions
This method has a remarkable feature that bonding can be obtained at room temperature. The advantages of this method are low thermal damage, low residual stress and simplicity of the bonding process, which are expected for the packaging and assembly of micro-electro-mechanical systems (MEMS). The main driving force for this development is to realize InPOI materials, similar to SOI concept, but with the added advantages of III-V material on Si substrates. Figure 2a and b shows the cross-sectional SEM and surface morphology of the InP thin film layer bonded to oxidized Si (100) substrate. The measured oxide thickness is about 200nm which acts an interlayer with reliable bonding strength across the interface.
Fig. 2. (a) SEM cross-section of the 2μ InP film bonded to Si substrate with an thin oxide layer (200nm) and (b) smooth surface morphology of the thin InP film

The thickness of the interlayer depends strongly on the applied pressure during bonding. Large bond strength can be obtained when the interlayer is thin. After annealing the wafer at 220°C for 45 minutes under pressure, the bonding strength is so large that forced separation did not happen at the oxide-oxide bonding interface. In our previous study we have observed that a very “thin oxide layer forms on InP when subjected to oxygen plasma”⁸. Thus the SEM image depicts a total thickness of both InP based oxide with Si formed oxide. The interlayer constitution is basically a native oxide of silicon. A number of recent reports suggest that “this interlayer plays a very important role for the characteristics of oxide bonding”¹⁰. The surface morphology shown in figure 2b, exhibits a smooth surface which is very much essential when cantilever structures are to be developed.

The optical quality of the thin film was assessed by PL and micro-Raman measurements. For the PL an excitation source of 514nm Ar-ion laser was used and Raman spectra were recorded using JY-T64000 micro-Raman system. The InP thin film bonded to oxide/Si substrate was investigated by room temperature photoluminescence studies. The PL spectrum obtained from the bonded structures is shown in figure 3a. The photoluminescence is a measure of the optical quality of the epilayer bonded onto another substrate. The figure clearly indicates the optical signature corresponding to InP at 920nm. The PL measurements were done on a two micron bonded samples. No changes in PL intensities were observed before and after the bonding process. In addition, no peak wavelength shift was observed in the bonded samples, which suggests no interface stress is developed during the bonding, as the temperature is kept below 250°C in the bonding experiments.

Fig. 3. (a) Room temperature PL signature of InP bonded at 220°C to oxide defined Si substrate and (b) micro-Raman spectrum of the 2μthin film bonded to Si substrate
The quality of the bonded layers was also analyzed by micro-Raman spectroscopy. As shown in figure 3b, Raman spectrum recorded from thin InP bonded to oxide defined Si substrate film show strong InP-related transverse-optic (TO) and longitudinal-optic (LO) phonons. The TO phonon located near 300 cm$^{-1}$ is much stronger in this recording geometry from (100) oriented InP layer. After InGaAs etching, no phonon peaks related to InGaAs were detected in the Raman spectra. This confirms that InGaAs film has been completely etched away by the processing step. Etching induced disorder could lead to the disorder-activated Raman peaks defined as DA modes in the spectra.

The formation of MEMS patterns such as cantilevers as described in figure 4, were achieved using a combination of lithography, dry and wet etching techniques.

![SEM micrograph of 50µm long InP cantilever suspended on Si substrate, by selectively etching Si substrate in KOH:H$_2$O (30%).](image)

Suitable mask patterns were transferred onto InP by standard lithography and latter by etching in HBr chemistry using ICP etching system. The sample was etched to a depth of approximately 2.5µm. This was done to ensure Si substrate was exposed to facilitate the release of InP micromechanical structures. The InP cantilevers were released by etching the Si substrate in KOH:H$_2$O (30%) for a cyclic period of 15 minutes under room temperature.

The process developed to release InP free standing micromechanical structures is more robust, since KOH is very selective and does not etch InP membranes. Though the release of “InP does follow standard processes such as sublimation drying techniques”\textsuperscript{11}, in this process by etching away the underlying Si and followed by DI water rinse, results in the release of InP thin film cantilevers.

**Conclusions**

In this paper we have discussed an approach to transplant InP thin films on Si platform. The InP films exhibited excellent quality in terms of optical and surface characteristics indicating no development of stress in the films. The release of InP cantilevers by selectively etching Si in KOH solution is successfully demonstrated. This simple technique of releasing InP cantilevers on Si substrates is a suitable approach for integrating III-V materials on Si platform and can be potentially studied for device applications.

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