Computational Associative Memory with Amorphous InGaZnO Channel 3D NAND-Compatible FG Transistors

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Abstract

3D NAND enables continuous NAND density and cost scaling beyond conventional 2D NAND. However, its poly-Si channel suffers from low mobility, large device variations, and instability caused by grain boundaries. Here, we overcome these drawbacks by introducing an amorphous indium-gallium-zinc-oxide (a-IGZO) channel, which has the advantages of ultra-low OFF current, back-end-of-line compatibility, higher mobility and better uniformity than poly-Si, and free of grain boundaries due to the amorphous nature. Ultra-scaled floating-gate (FG) transistors with a channel length of 60 nm are reported, achieving the highest ON current of 127 μA/μm among all reported a-IGZO-based flash devices for high-density, low-power, and high-performance 3D NAND applications. Furthermore, a non-volatile and area-efficient ternary content-addressable memory (TCAM) with only two a-IGZO FG transistors is experimentally demonstrated. Array-level simulations using experimentally calibrated models show that this design achieves at least 240× array-size scalability and 2.7-fold reduction in search energy than 16T-CMOS, 2T2R, and 2FeFET TCAMs.
**Introduction**

Flash memories, which utilize the electron storage mechanisms either on a floating-gate (FG) or charge-trap (CT) layer, have been widely used in massive data storage due to the cost-effectiveness\(^1\)–\(^4\). They also show great potential for many emerging applications, such as in-memory edge computing\(^5\)–\(^6\). Vertically stacked NAND flash memories, or 3D NAND\(^7\)–\(^9\), has replaced planar NAND flash memories by overcoming many issues faced by 2D NAND when scaling beyond 20 nm technology node, including the requirement of the advanced lithography technique, increased cell to cell interference due to proximity effect, and more severe threshold voltage \((V_{TH})\) shift per electron injection caused by the random telegraphic noise\(^10\)–\(^12\). 3D NAND provides a scalable path for continual density improvement by stacking more and more layers for higher memory density while also increasing the number of bits stored in a single cell. Highly promising as it is, 3D NAND also faces challenges during the z-direction scaling (i.e., stacking more layers), especially with the poly-Si channel. Firstly, the mobility of the poly-Si in the flash memories is typically less than 10 cm\(^2\)/V∙s due to the disordered structure\(^13\), resulting in a low cell current and insufficient sense margin, especially after stacking hundreds of layers\(^14\),\(^15\). Secondly, the existence of grain boundaries in poly-Si degrades \(V_{TH}\) distribution and causes time-dependent \(V_{TH}\) instability because of charge trapping at the grain boundaries\(^16\)–\(^18\). Thirdly, the grain boundaries would also introduce large device-to-device variation in electrical characteristics at ultra-scaled channel length \((L_{CH})\), constraining the number of layers stacked due to extremely challenging etching of high-aspect-ratio holes for the NAND string. Therefore, for sustainable 3D NAND scaling, alternative channel materials that can solve these challenges while being compatible with existing processes are highly desired.
Amorphous indium-gallium-zinc-oxide (a-IGZO), a metal-oxide semiconductor\textsuperscript{19–21}, has emerged as one of the promising channel alternatives to poly-Si in 3D NAND owing to its high mobility, free of grain boundaries due to the amorphous nature, wafer-size thin film formation with high uniformity\textsuperscript{22,23}. Thin-film transistors (TFTs) with a-IGZO as the channel have been applied in displays, sensors, logic devices, and neuromorphic computing\textsuperscript{24–29}. Moreover, a-IGZO that can be processed within the back-end-of-line (BEOL) thermal budget could enable ultra-high density monolithic 3D integration by vertically stacking multiple tiers of functional layers of devices and circuits\textsuperscript{30–33}. In addition, our previous study for ultra-scaled a-IGZO TFT discovered that there was no noticeable degradation of mobility as the thickness of a-IGZO reduces from 6 to 3.6 nm\textsuperscript{34}, which is different from Si suffering from the dramatic reduction in mobility when the thickness is reduced to less than 5 nm\textsuperscript{35}. By suppressing the short channel effects (SCEs), a thinner channel could enable more aggressive channel length scaling to even less than 10 nm\textsuperscript{36,37}. Therefore, there is tremendous potential for realizing high-performance and ultra-scaled flash memories (FG or CT transistors) based on an a-IGZO channel. Although there have been several reports on a-IGZO-based flash transistors\textsuperscript{38–40}, the performance of the devices needs significant improvement, especially for lowering the operating voltage and scaling the channel length to tens of nanometers for high-density and high-performance 3D NAND applications.

In addition to its application as NAND memory storage, FG transistors also find emerging applications for in-memory computing with ternary content addressable memory (TCAM) as an important example\textsuperscript{41,42}. TCAMs, as associative memories, can perform pattern matching in a massive parallel manner, which is highly desirable for IP packets forwarding in networking routers, database engines, as well as recently investigated compute-in-memory applications\textsuperscript{42–44}. 


Various memory technologies can be harnessed for the TCAM design. The conventional TCAM cell is based on complementary metal-oxide-semiconductor (CMOS) technology and consists of 16 transistors (16T-CMOS), suffering from low area efficiency and high dynamical leakage power due to its volatility. Research studies employing emerging non-volatile memories (NVMs) for TCAM design have also been presented, such as resistive random access memory (ReRAM)\textsuperscript{45,46} and ferroelectric field-effect-transistors (FeFETs)\textsuperscript{47,48}. However, for these NVM-based TCAMs, a high thermal budget due to the high process temperature of Si technology and complex peripheral circuits to work with the low ON/OFF current ratio ($I_{ON}/I_{OFF}$) are necessary. Moreover, the large OFF current ($I_{OFF}$) of emerging NVMs limits the scalability of the NVM-based TCAM arrays. The scalability of a TCAM array is predominately determined by the $I_{OFF}$ of the transistors. As the TCAM word size increases, i.e., more transistors are connected in parallel on the same match line, the total $I_{OFF}$ in the TCAM word increases. This could discharge the match line even at a matching case, leading to a reduction of sense margin to distinguish between the match and mismatch scenarios and therefore causing possible function failure. The $I_{OFF}$ of transistors depends strongly on the thermionic leakage current and the tunneling current at the channel/drain junction\textsuperscript{49}. Both current components have a negative exponential relationship with the energy barrier height $\Phi$, while the tunneling current is additionally influenced by the tunneling barrier width\textsuperscript{50,51}. The wide bandgap (3.2 eV) of $a$-IGZO leads to a much greater built-in potential and a larger tunneling barrier height and width than Si, resulting in an ultra-low $I_{OFF}$\textsuperscript{52}. Thus, TCAM based on FG transistors with an $a$-IGZO channel can overcome the aforementioned disadvantages of 16T-CMOS and NVM-based TCAMs. Firstly, it has a lower thermal budget and simplified peripheral circuits due to much larger $I_{ON}/I_{OFF}$ as compared with Si counterparts. Secondly, the ultra-low $I_{OFF}$ of $a$-IGZO transistors and 2T configuration in an $a$-
IGZO FG transistor-based TCAM cell could achieve much lower search energy than 16T-CMOS and NVM-based TCAM designs. Thirdly, with the extremely low $I_{OFF}$ of $\alpha$-IGZO FG transistors, a much larger scale of the TCAM array can be realized, enabling applications that require a large array size, such as hyperdimensional (HD) computing$^{53,54}$.

In this work, we report the realization of $\alpha$-IGZO FG transistors with outstanding electrical characteristics, including a low $I_{OFF}$ of less than $10^{-7}$ $\mu$A/$\mu$m, a large $I_{ON}/I_{OFF}$ of $1 \times 10^8$, a low subthreshold swing (SS) of $\sim$80 mV/decade, and a high mobility of 32.6 cm$^2$/V·s. Our $\alpha$-IGZO FG transistors show a large memory window (MW) of 1.8 V at a low operating voltage with a retention time of more than 10 years, indicating the floating-gate-engineered nonvolatility. The endurance measurement of 1000 cycles of switching slightly reduces the MW from 1.8 to 1.6 V.

From the evaluation of temperature-dependent operations, $\alpha$-IGZO FG transistors still offer an MW of 1.4 V even at a high temperature of 80 °C. By scaling the $L_{CH}$ to 60 nm, record-high ON current ($I_{ON}$) of 127 $\mu$A/$\mu$m was realized and is much higher than reported flash transistors using an $\alpha$-IGZO channel, while maintaining the MW larger than 1.5 V. Furthermore, an area-efficient TCAM cell with only two parallel-connected $\alpha$-IGZO FG transistors was also demonstrated using a low thermal budget of 300 °C and functionalities of writing and searching are realized.

Using the experimentally calibrated device parameters, we further performed array-level simulations to benchmark the scalability, search energy, and search delay of our $\alpha$-IGZO FG transistor-based TCAM array with those TCAM arrays based on 16T-CMOS cell, two-transistor-two-ReRAM (2T2R), and 2FeFET. The results highlight that, compared with 16T-CMOS, 2T2R, and 2FeFET TCAM technologies, the TCAM array using $\alpha$-IGZO FG transistors exhibits at least a 240× improvement in array-size scalability and a 2.7-fold reduction in search energy.
Results

Device structure and electrical characteristics of a-IGZO FG transistors

Figure 1a shows the schematic illustration of the fabricated a-IGZO FG transistor, and the corresponding scanning electron microscope (SEM) image is shown in Supplementary Fig. 1. The bottom-gate structure with top-contacted source/drain was used, where the gap between the source and drain is defined as the $L_{CH}$. Figure 1b shows the cross-sectional view of the device. High-quality a-IGZO with a thickness of ~8 nm and a small root-mean-square (RMS) roughness of ~0.55 nm was employed (roughness is shown in Supplementary Fig. 2). The gate stack consists of 6-nm HfO$_2$/20-nm TiN/10-nm HfO$_2$/30-nm TiN from top to bottom, where the inserted 20-nm TiN is an FG and can be used to trap charges. The thicknesses of each layer in the channel region (A-A in Fig. 1b) were confirmed by the high-resolution transmission electron microscopy (HRTEM) image (Fig. 1c). The smooth and sharp a-IGZO/HfO$_2$ interface and the amorphous nature of the IGZO layer were also demonstrated. Figure 1d-j illustrate the energy-dispersive X-ray (EDX) mapping profiles in the layer stack of the drain region (B-B in Fig. 1b). The distribution of Hf, Ti, N, In, Ga, Zn, and O elements are exhibited. It is noted that nitrogen (Fig. 1f) and oxygen (Fig. 1j) are present in all layers, suggesting the possible interlayer diffusion of N and O during the thermal annealing process.

Figure 2a shows the width-normalized $I_{DS}$-$V_{GS}$ curves of the fabricated a-IGZO FG transistor ($L_{CH} = 5 \, \mu\text{m}$) at a low $V_{DS}$ of 0.1 V and a high $V_{DS}$ of 1 V. The transfer characteristics in the programmed state, which means the logic state ‘1’, were measured by the direct-current (DC) method after applying a program pulse (6.5 V, 1 ms). Similarly, the transfer characteristics in the erased state, which indicates the logic ‘0’, were measured after applying an erase pulse (-5 V, 1 ms). The electrons trapped at the FG shift the $V_{TH}$ of the transistor, which can be tuned by
applied pulses because of the electron tunneling effect. To further illustrate the tunneling mechanism, the energy band diagram along the direction perpendicular to the channel was obtained by simulating an a-IGZO FG transistor with the same structure of our fabricated device using technology computer-aided design (TCAD). The simulated device structure is shown in Supplementary Fig. 3a. During programming, electrons in the a-IGZO channel tunnel into the FG through the tunneling oxide after applying a positive voltage on the control gate (Supplementary Fig. 3b). On the other hand, electrons tunnel back from the FG to the IGZO channel after performing a pulse with a negative voltage during erasing (Supplementary Fig. 3c).

From the $I_{DS}$-$V_{GS}$ curves, the MW defined as the difference in $V_{TH}$ between the two states is $\sim$1.8 V, achieving excellent memory characteristics in a low operating voltage. It should be noted that the $I_{OFF}$ of $\sim$10$^{-7}$ $\mu$A/$\mu$m ($\sim$1 pA without normalization to the width of the device) is due to the detection limit of the measurement tool. The actual $I_{OFF}$ should be less than 1 pA for both programmed and erased states because of the wide bandgap of a-IGZO ($\sim$3.2 eV) and the low gate leakage current.$^{52,55}$ A large $I_{ON}/I_{OFF}$ of $\sim$1×10$^8$ is achieved at $V_{DS}$ of 1 V, and it can be further boosted by scaling the device $L_{CH}$ to improve $I_{ON}$.

$SS$ values extracted from the $I_{DS}$-$V_{GS}$ curves are shown in Fig. 2b as a function of $I_{DS}$ for the programmed state and the erased state at low and high $V_{DS}$. All the $SS$ values remain less than 100 mV/decade over more than 2 orders of $I_{DS}$ with the smallest value of $\sim$80 mV/decade, indicating the excellent gate stack quality. In Fig. 2c, the plot of transconductance ($G_m$) at $V_{DS}$ = 1 V as a function of $V_{GS}$ exhibits a peak value of $\sim$3.5 $\mu$S/$\mu$m for the programmed state and 3.2 $\mu$S/$\mu$m for the erased state. It also shows a noticeable window between the two states. The capacitance-voltage (C-V) curves were measured using the measurement configuration described
in Fig. 2d and were utilized to extract the effective mobility ($\mu_{\text{eff}}$) of $a$-IGZO FG transistors using the equation (1):

$$\mu_{\text{eff}} = \frac{L_{\text{CH}} \times I_{\text{DS}}}{W_{\text{CH}} \times Q \times V_{\text{DS}}}.$$  \hspace{1cm} (1)

Here $Q$ is the carrier charge density and $W_{\text{CH}}$ is the channel width. This is a widely used method in the CMOS device community. Figure 2e plots the $C$-$V$ results at various frequencies ranging from 100 Hz to 1000 kHz. The carrier charge density was obtained by integrating the $C$-$V$ curve. The extracted $\mu_{\text{eff}}$ as a function of carrier density ($N_{\text{carrier}}$) is shown in Fig. 2f. $\mu_{\text{eff}}$ of 32.6 cm$^2$/V·s, which is higher than poly-Si in 3D NAND$^{13}$, and relatively high for oxide semiconductor materials, is achieved at $N_{\text{carrier}}$ of $\sim$3.8×10$^{12}$ cm$^{-2}$.

**Impact of channel length down-scaling**

The continuous improvement in the areal density of memory devices lies in the scaling of a single transistor, especially the channel length of the transistor. In order to investigate the impact of $L_{\text{CH}}$ down-scaling on device performance, transistors with various $L_{\text{CH}}$ were fabricated. The shortest $L_{\text{CH}}$ is 60 nm, which was confirmed by the SEM image (Supplementary Fig. 4). Figure 3a shows the transfer characteristics of the ultra-scaled transistor ($L_{\text{CH}}$ = 60 nm) with a $V_{\text{DS}}$ of 0.1 V and 1 V, where the $I_{\text{ON}}$ is significantly improved compared with that of the long-channel device ($L_{\text{CH}}$ = 5 $\mu$m) while keeping the $I_{\text{OFF}}$ below 1 pA. The MW is larger than 1.5 V. The extracted $G_m$ is plotted in Fig. 3b, showing a peak value of 22.3 $\mu$S/$\mu$m and 23.4 $\mu$S/$\mu$m for the programmed state and erased state, respectively. Figure 3c gives the output characteristics of the same device with an $L_{\text{CH}}$ of 60 nm, yielding a high current of $\sim$127 $\mu$A/$\mu$m at $V_{\text{DS}}$ of 3 V and gate overdrive ($V_{\text{GS}}$ - $V_{\text{TH}}$) of 4 V.
The transfer characteristics of devices with $L_{CH}$ of 100 nm, 200 nm, and 500 nm are shown in Supplementary Fig. 5. Figure 3d summarizes the extracted $SS$ as a function of $L_{CH}$ from the $I_{DS}$-$V_{GS}$ curves. The average $SS$ of the programmed state and erased state remains less than 100 mV/decade until $L_{CH}$ is scaled down to 200 nm. The ultra-scaled device with an $L_{CH}$ of 60 nm exhibits the $SS$ value of $\sim$105 mV/decade, indicating excellent control of the SCEs. Summarized $I_{ON}$ can be observed in Fig. 3e, where $I_{ON}$ is obtained at an overdrive voltage of 3 V and a $V_{DS}$ of 3 V from the output characteristics (Supplementary Fig. 6). As the $L_{CH}$ scales down, the resistance in the channel region is reduced. However, the source/drain series resistance ($R_{SD}$) remains unchanged, and the $R_{SD}$ dominates the output current, which is the reason for the saturation of $I_{ON}$ at sub-500 nm of $L_{CH}$. By further reducing the $R_{SD}$ through advanced source/drain engineering, a significant $I_{ON}$ enhancement is expected$^{56,57}$. Figure 3f shows the relationship between the MW and $L_{CH}$. It is noteworthy that the MW remains larger than 1.5 V with $L_{CH}$ down to 60 nm, demonstrating the promise of our $a$-IGZO FG transistors to be used in ultra-high density 3D NAND at advanced technology nodes.

**Pulse response and reliability of $a$-IGZO FG transistors**

The pulse response of a single $a$-IGZO FG transistor was studied by applying pulses with different amplitudes and widths. For the positive $V_{TH}$ shift by applying a program pulse, the device was initially set to an erased state using a pulse with an amplitude of -5 V and a width of 1 ms. After that, a positive pulse was applied to switch the device to the programmed state. The value of $V_{TH}$ was obtained by DC measurement after each pulse. For the case of erasing, a positive program pulse (6.5 V, 1 ms) and a negative erase pulse were employed, which was opposite to the programming case. Figure 4a and Figure 4b illustrate the 2D contour of the $V_{TH}$
shift as a function of pulse amplitude and pulse width for the program pulse and the erase pulse, respectively. The absolute value of the $V_{TH}$ shift increases with the increase of pulse amplitude and pulse width, and a pulse with 1 ms pulse width is sufficient to obtain a saturated $V_{TH}$ shift. Notably, the $a$-IGZO FG transistor requires a low operating voltage of 6 V, which is beneficial for power consumption reduction.

The endurance of the $a$-IGZO FG transistor was evaluated by 1000 cycles of continual switching between programmed and erased states with a $V_{DS}$ of 0.1 V, as depicted in Fig. 5a. Each transfer curve was measured after the program or erase pulse. The device has a width of 10 $\mu$m. Figure 5b summarizes the extracted voltage for all the curves from Fig. 5a at the current level of $10^{-5}$ $\mu$A/$\mu$m. It shows that both the programmed and erased $I_{DS}$-$V_{GS}$ curves are positively shifted, with the MW slightly reducing from 1.8 to 1.6 V after 1000 cycles. The shift of the curves may be caused by the asymmetry of the program pulse and erase pulse, where the electrons were not completely depleted from the FG by the erase pulse and accumulated after cycling. Figure 5c shows the retention characteristics of the device after applying a program pulse (6.5 V, 1 ms) and an erase pulse (-5 V, 1 ms). Extrapolation of the data indicates that the programmed state and erased state can still be identified after 10 years with an MW of 0.9 V, demonstrating a retention time longer than 10 years. The change of $V_{TH}$ in the programmed state is slightly faster than that of the erased state. It could be caused by the local trap-assisted tunneling, which stimulates electrons to tunnel from FG back to the channel$^{58}$.

Temperature-dependent operations of $a$-IGZO FG transistors were also investigated. The transfer characteristics at various temperatures from -40 to 80 °C with a step of 20 °C are described in Supplementary Fig. 7. $SS$ increases monotonically as the temperature increases and reaches around 100 mV/decade at 80 °C, as depicted in Fig. 5d. The current obtained at $V_{GS}$ of 3
V and \( V_{DS} \) of 0.1 V at various temperatures is shown in Fig. 5e. Improved current at higher temperatures could be explained by the increase of carrier concentration. This is an advantage for operations at higher temperatures over Si-based devices, where a reduction of current at higher temperatures was typically observed because of the mobility degradation caused by phonon scattering\(^{59,60}\). Figure 5f plots the extracted voltage and MW as a function of the operating temperature. The \( I_{DS}-V_{GS} \) curves exhibit a slight positive shift when the operating temperature increases from -40 °C to 20 °C. However, further increasing the operating temperature from 20 to 80 °C causes the curves to shift negatively, which could be dominated by the increased carrier concentration in the IGZO channel at high temperatures. It was observed that MW degrades slightly at high temperatures but still offers a value of \( \sim 1.4 \) V at 80 °C.

The performance benchmarking of our devices with reported flash memories based on an a-IGZO channel was summarized in Supplementary Table 1. The devices studied in this work have the shortest \( L_{CH} \) of 60 nm with the best control of SCEs, achieving the highest \( I_{ON} \) of 127 \( \mu \)A/\( \mu \)m and the lowest operating voltage among all the a-IGZO-based flash devices.

**Fully functional TCAM based on a-IGZO FG transistors**

The conventional CMOS-based TCAM cell is composed of 2 static random-access memory (SRAM) cells and 4 comparison transistors (Fig. 6a). The logic state of the TCAM cell is indicated by the states of SRAM cells, logically taking one of the three states: 0, 1, or X (don’t care). The search operations are performed by 2 search lines (SL and \( \overline{SL} \)) while the write operations are performed by the bit lines and the write line. The output of the match line (ML) is determined by the XNOR result of the TCAM state and the search bit (Supplementary Table 2). It is clear that CMOS-based TCAM has complicated connection lines and occupies a large area.
Alternatively, the a-IGZO FG transistor-based TCAM is much more area-efficient due to its reduced connection lines, where the bit line and search line are merged into a single search line, as shown in Fig. 6b. This area-efficient schematic utilizes the nonvolatility and intrinsic transistor nature of the a-IGZO FG device, where the $V_{TH}$ can be tuned by pulses to indicate different logic states.

The SEM image in Supplementary Fig. 8 shows the fabricated TCAM cell with two parallel-connected a-IGZO FG transistors ($L_{CH} = 5 \mu m$). The source terminals and drain terminals of the transistors are connected and defined as ML and ground, respectively, while the gate terminals are designed as the search lines. The transistor $T_0$ and $T_1$ in the TCAM cell can be set to logic states ‘1’ or ‘0’ after writing pulses (1, high $V_{TH}$ and 0, low $V_{TH}$), as summarized in Fig. 6c. The ‘don’t care’ state can be realized by setting both transistors to high $V_{TH}$ states. For search operations, the pulse width is 0.2 ms with a low search voltage ($V_{SL\_L}$) of 0 V or a high search voltage ($V_{SL\_H}$) of 0.9 V. It should be noted that the negative erase pulse (-4.2 V, 1 ms) only partially shifts the $V_{TH}$ of the transistor in order to obtain a high current ratio between the search voltage of 0.9 V and 0 V ($I_{DS}$-$V_{GS}$ curves after pulses shown in Supplementary Fig. 9). This is because when the transistor is entirely erased, it can be switched on even at the search voltage of 0 V, or another method is to apply a lower $V_{SL\_L}$, such as -1 V$^{41}$. Note that the search operation is simply a transistor read, therefore its speed reported here is by no means the limit of the a-IGZO flash transistors, but rather limited by the measurement setup. Figure 6b describes the measurement setup of the TCAM cell with a $V_{DD}$ of 1.2 V and a load resistor of 3 MΩ. More details of the measurement scheme are described in Supplementary Fig. 10. During cell operation, logic states are first written into $T_0$ and $T_1$, and if the search state matches the stored data, the ML keeps high; otherwise, the ML discharges and switches to low.
Figure 6d shows the operation scheme of writing ‘1’ of the TCAM cell, where T0 is set to ‘1’ with a high V_{TH} after applying a positive pulse, and T1 is set to ‘0’ with a low V_{TH}. After that, search schemes of searching ‘1’ and searching ‘0’ are performed, as depicted in Fig. 6e and Fig. 6f, respectively. In Fig. 6e, a search pulse with an amplitude of V_{SL_H} is applied to T0, and another search pulse with an amplitude of V_{SL_L} is applied to T1. T0 with a high V_{TH} is cut off when the search voltage is 0.9 V, and T1 with a low V_{TH} is also cut off when the search voltage is 0 V. Therefore, the ML remains high, meaning that the search data matches with the data in the cell. On the other hand, a mismatch occurs when operating a search ‘0’ scheme. T0 with a high V_{TH} is still off under the search voltage of 0 V, but T1 with a low V_{TH} is switched on under the search voltage of 0.9 V, which discharges the ML, as observed in Fig. 6f. Other cases of writing ‘0’ and ‘X’ and corresponding search schemes are shown in Supplementary Fig. 11. Thus, a fully functional TCAM cell is demonstrated.

The ultra-low I_{OFF} of a-IGZO FG transistors (less than 10^{-7} \mu A/\mu m for a-IGZO FG transistors, while ~10^{-4} \mu A/\mu m for Si transistors^{61,62}) also provides the opportunity to make a TCAM array with a large array size, which can be used for hyperdimensional computing. To compare the performance of a-IGZO FG transistor-based TCAM with various TCAM designs (16T-CMOS, 2T2R, and 2FeFET), array-level simulations were carried out using the framework shown in Fig. 7a^{63,64}. TCAM cell for simulation is well-calibrated with the experimental data of our fabricated a-IGZO FG transistor with an L_{CH} of 60 nm, as shown in Supplementary Fig. 12. V_{SL_L} is set to -2 V while the V_{SL_H} is set to vary from 0 to 1 V to study the impact of I_{OFF} on the array size. During simulations, the ML of each row is precharged to a high voltage level, and the search lines are driven with input data. The sense amplifier senses the ML state of the associated word. When at least one cell does not match the input data, the ML could be discharged and drop to a
low level. Only when all cells match with the input data, the ML remains high. However, as the array size expands, the total $I_{OFF}$ increases because more TCAM cells are located at a single row. The ML could be discharged even at the matching case, making the matching case unable to be maintained for a long time. Figure 7b plots the simulation results of the matching case (storing 0 and searching 0) for $a$-IGZO FG transistor-based TCAM rows with various sizes ($V_{SL,L} = -2$ V, $V_{SL,H} = 0$ V). The actual search delay should be at the level of ns. However, to illustrate the ML dropping clearly, the search time is extended to 100 $\mu$s here. Obviously, the voltage of the ML for the 1×64 array drops faster than that of the 1×1 array because of the increased total $I_{OFF}$.

Time to drop $V_{DD}/2$ at the matching case, which is utilized to evaluate the scalability, is summarized in Fig. 7c for various TCAM designs based on a 1×64 TCAM array. TCAM array using $a$-IGZO FG transistors ($V_{SL,L} = -2$ V, $V_{SL,H} = 0$ V) shows at least a 240× improvement in time to drop to $V_{DD}/2$ as compared with 16T-CMOS, 2T2R, and 2FeFET TCAMs, indicating excellent scalability and the potential to be used in an enormous TCAM array which is essential for many emerging applications. It is important to mention that the $I_{OFF}$ of $a$-IGZO FG transistors of ~1 pA was obtained from the experimental measurement and limited by the detection accuracy of the measurement tool. The actual $I_{OFF}$ should be much lower so that the time to drop to $V_{DD}/2$ of the $a$-IGZO FG transistor-based TCAM array can be much longer. Additionally, the search energy and search delay of a 64×64 TCAM array are also simulated, as depicted in Fig. 7d. The $a$-IGZO FG transistor-based TCAM ($V_{SL,L} = -2$ V, $V_{SL,H} = 0$ V) array shows at least a 2.7-fold reduction in search energy due to the low $I_{OFF}$ and simple cell structure. The search delay defined as the time to drop to $V_{DD}/2$ of the ML under the mismatching case is mainly determined by the turn-on current of the transistor with a low $V_{TH}$ state under $V_{SL,H}$ (Supplementary Fig. 12). Higher current discharges the ML faster and results in a lower search
delay. By increasing the $V_{SL_H}$, the discharging current can be enhanced, and the search delay can be reduced while keeping the search energy almost unchanged (Fig. 7d). However, there is a trade-off between the search delay and the scalability (Fig. 7c). The time to drop to $V_{DD}/2$ at the matching case is reduced because the $I_{OFF}$ increases with the increase of $V_{SL_H}$, leading to degraded scalability. This can be optimized in future work by lowering the $R_{SD}$ of transistors to boost the discharging current and to remain the $V_{SL_H}$ at 0 V.

**Conclusion**

In summary, 3D NAND compatible high-performance $a$-IGZO FG transistors and an area-efficient TCAM cell based on two $a$-IGZO FG transistors are fabricated and investigated in this paper with both experiments and simulations. Our $a$-IGZO FG transistors have the benefits of low process temperature, low operating voltage, less than $10^{-7}$ µA/µm $I_{OFF}$, large $I_{ON}/I_{OFF}$ of more than $1 \times 10^8$, low $SS$ of about 80 mV/decade, high effective mobility of 32.6 cm²/V·s, large MW of ~1.8 V (1.4 V at 80 °C), and good endurance and retention. Ultra-scaled $a$-IGZO FG transistor with an $L_{CH}$ of 60 nm offers a boosted $I_{ON}$ of 127 µA/µm while remaining the MW larger than 1.5 V. Attributing the low $I_{OFF}$ of $a$-IGZO FG transistor and the simple TCAM structure, the TCAM array based on $a$-IGZO FG transistors shows much better scalability and lower search energy as compared with TCAM arrays based on 16T-CMOS, 2T2R, and 2FeFET. This work paves the way for the applications of $a$-IGZO FG transistors in 3D NAND and TCAM and projects the potential to significantly expand the size of the TCAM array.

**Methods**

Device fabrication.
The device fabrication process (Supplementary Fig. 13) started with the deposition of 30 nm TiN on the SiO₂/Si substrate using e-beam evaporation followed by an etching process. 10 nm HfO₂ film was deposited by ALD at 250 °C. Hf[N(C₂H₅)CH₃]₄ (TEMAHf) and ozone were used as the Hf precursor and oxygen source, respectively. After the patterning and etching of HfO₂, another 20 nm TiN was deposited and patterned as the floating gate. Then, 6 nm HfO₂ deposited by ALD was performed as the tunneling layer. After etching the tunneling layer, a layer of 8-nm a-IGZO was deposited by radio frequency (RF) sputtering at room temperature. Device isolation was then performed by wet etching of IGZO using HCl solution. Source/drain regions were defined using electron beam lithography (EBL), and Ti/Pt electrodes were deposited by e-beam evaporation followed by the lift-off process. Finally, fabricated devices were annealed at 300 °C for 20 minutes. The TCAM cell was formed during source/drain patterning by connecting the source and drain terminals of two transistors, respectively.

**Device characterization.**

Temperature-dependent operations of a-IGZO FG transistors were measured under vacuum conditions at various temperatures, and other characteristics of devices were measured under air conditions and room temperature. The surface roughness was measured by atomic force microscopy (AFM) (NX20, Park). The electrical characteristics of a-IGZO FG transistors were measured by a semiconductor parameter analyzer (4200a-SCS, KEITHLEY), and pulse measurements were performed by the pulse measurement unit (4225-PMU, KEITHLEY). The write and search functions of the TCAM cell were carried out by the analyzer, oscilloscope (MDO3104, Tektronix), and DC power supply (E3630A, Agilent). The schematic of the measurement setup is provided in Supplementary Fig. 10. The ML of the TCAM cell was
connected to an external resistor (3 MΩ). The other terminal of the resistor was connected to the power supply with a $V_{DD}$ of 1.2 V. Input pulses for writing and searching were generated by the PMU. The amplitude of the program pulse and erase pulse were set to 6.0 V and -4.2 V, respectively, with the pulse width of 1 ms. 200 μs search pulses with amplitudes of 0.9 V and 0 V were used for searching operations. The waveforms of the search lines and the ML were plotted by the oscilloscope.

**Author contributions**

This project was supervised and directed by X. Gong. C. Sun and X. Gong conceived and designed the experiments. C. Sun performed device fabrication and electrical measurements. C. Li, K. Ni, and X. Yin carried out the array-level simulation. All authors contributed to the discussion and data analysis. C. Sun, K. Ni, and X. Gong wrote the manuscript.

**Competing interests**

The authors declare no competing interests.
**Fig. 1 Device structure of the a-IGZO FG transistor.**

(a) Schematic illustration of the a-IGZO FG transistor. $L_{CH}$ is defined as the gap between the source and drain. (b) Cross-sectional view of the device, employing a gate stack of HfO$_2$/TiN (FG)/HfO$_2$/TiN from top to bottom. (c) HRTEM image of the device in the channel region, confirming the thickness of each layer. (d-j) EDX mapping profiles in the drain region, showing the distribution of Hf, Ti, N, In, Ga, Zn, and O elements.
Fig. 2 Electrical characterization of the a-IGZO FG transistor with an $L_{\text{CH}}$ of 5 $\mu$m. a $I_{DS}$-$V_{GS}$ of the device measured after applying pulses, achieving a large MW of 1.8 V. $I_{\text{OFF}}$ is lower than the detection limit of the measurement tool. Programmed state means ‘1’, and erased state means ‘0’. b Extracted $SS$ from $I_{DS}$-$V_{GS}$ curves. All the $SS$ values remain less than 100 mV/decade over more than 2 orders, with the smallest value of $\sim$ 80 mV/decade. c Extracted $G_m$ from $I_{DS}$-$V_{GS}$ curves at $V_{DS}$ of 1 V, showing a noticeable window between the two states. d Configuration for $C$-$V$ measurements. The source and the drain of the devices are connected. e $C$-$V$ measurements of the device for mobility extraction. f Extracted mobility of the device using the inserted equation, achieving high mobility of 32.6 cm$^2$/V$\cdot$s.
Fig. 3 Impact of $L_{\text{CH}}$ scaling and characterization for $a$-IGZO FG transistors. (a) $I_{DS}$-$V_{GS}$ of the ultra-scaled device with an $L_{\text{CH}}$ of 60 nm, showing a boosted $I_{\text{ON}}$ while keeping the $I_{\text{OFF}}$ below 1 pA. The MW is larger than 1.5 V for both $V_{DS}$ of 0.1 V and 1 V. (b) $G_m$ extracted from the $I_{DS}$-$V_{GS}$ curves with a peak value of 22.3 $\mu$S/μm for the programmed state and 23.4 $\mu$S/μm for the erased state. (c) $I_{DS}$-$V_{DS}$ curves of the device ($L_{\text{CH}}$ = 60 nm). A high current of $\sim$127 $\mu$A/μm is obtained at $V_{DS}$ = 3 V and $V_{GS}$ - $V_{\text{TH}}$ = 4 V. (d) Impact of $L_{\text{CH}}$ on SS. SS slightly increases as the scaling of $L_{\text{CH}}$ with a value of $\sim$105 mV/decade for $L_{\text{CH}}$ of 60 nm, indicating a good control of SCEs. (e) Summary of $I_{ON}$ at an overdrive voltage of 3 V and $V_{DS}$ of 3 V. (f) MW as a function of $L_{\text{CH}}$. MW maintains stable as the $L_{\text{CH}}$ reduces.
Fig. 4 $V_{TH}$ tuning of a-IGZO FG transistors by pulses. a $V_{TH}$ shifts positively by applying program pulses. The device was initially set to an erased state. The $V_{TH}$ was obtained by DC measurement after each pulse. Pulse with an amplitude of 6 V (1 ms) is sufficient to program the device entirely. b $V_{TH}$ shifts negatively by applying erase pulses. The device was initially set to a programmed state.
Fig. 5 Reliability characteristics of a-IGZO FG transistors. a Endurance measurement performed by 1000 cycles of continual switching between the programmed state and erased state. Each curve was obtained by DC measurement after applying the pulses. b Extracted voltage level at $I_{DS} = 10^{-5} \mu A/\mu m$ and the corresponding MW from endurance measurement. The positive shift of the voltage level could be caused by the asymmetry of the program pulse and erase pulse, resulting in the accumulation of electrons at the FG after 1000 cycles. The MW slightly drops to 1.6 V from 1.8 V after 1000 cycles. c Retention measurement of the device. $V_{TH}$ shows a positive shift after erasing and a negative shift after programming. Extrapolation of the points indicates that the device has a retention time longer than 10 years. d The relationship between SS and the operating temperature of the device. SS increases monotonically as the temperature increases. e Current at $V_{GS} = 3$ V and $V_{DS} = 0.1$ V increases monotonically as the temperature increases for programmed and erased states. f Extracted voltage level at $I_{DS} = 10^{-5} \mu A/\mu m$ from $I_{DS}$-$V_{GS}$ for various temperatures. The device is able to maintain an MW of $\sim$1.4 V at 80 °C.
Fig. 6 Fully functional TCAM cell using a-IGZO FG transistors. a Schematic of a conventional CMOS-based TCAM cell, which is composed of 2 SRAM cells and 4 comparison transistors. b Schematic of the area-efficient TCAM cell based on a-IGZO FG transistors. SL and SL̅ are employed for writing and searching. The load resistor (3 MΩ) is externally connected for measuring the voltage of ML. c Summary of write and search operations. The state of the TCAM cell is indicated by the states of T_0 and T_1. Pulses with amplitudes of 0.9 V and 0 V and a width of 0.2 ms are applied for searching. d Operation scheme of writing ‘1’ into the TCAM cell by setting T_0 to ‘1’ and T_1 to ‘0’. e Operation scheme of searching ‘1’ after writing ‘1’. T_0 with high V_{TH} is cut off when the search pulse is 0.9 V, while T_1 with low V_{TH} is also cut off when the search pulse is 0 V, indicating a matching case and keeping the ML at a high voltage level. f Operation scheme of searching ‘0’ after writing ‘1’. T_0 with high V_{TH} is cut off when the search pulse is 0 V, but T_1 with low V_{TH} is switched on when the search pulse is 0.9 V, indicating a mismatching case and discharging the ML.
Fig. 7 Array-level simulations for TCAMs. a Simulation framework. The ML is precharged before data input. ML remains high only when all the cells match with the input data. b Waveforms of ML at the matching case. The ML is discharged by the total $I_{OFF}$ even all the transistors are cut off. Here the search time is extended to 100 $\mu$s to illustrate the ML dropping clearly. c Time to drop to $V_{DD}/2$ of the ML for TCAM arrays using various designs. TCAM array based on $a$-IGZO FG transistors shows at least a 240× improvement in the time compared with 16T-CMOS, 2T2R, and 2FeFET TCAMs ($V_{SL,L} = -2$ V, $V_{SL,H} = 0$ V). d Benchmarking of the search energy and search delay for TCAM arrays. TCAM array based on $a$-IGZO FG transistors achieves at least a 2.7-fold reduction in search energy. The search delay can be reduced by increasing the $V_{SL,H}$ while keeping low search energy.
Supplementary Information

Supplementary Fig. 1 Top-view SEM image of the FG a-IGZO TFT. The gap between the source and drain is defined as the channel length ($L_{CH}$). Channel width ($W_{CH}$) is 10 $\mu$m, and $L_{CH}$ is 5 $\mu$m here.

Supplementary Fig. 2 AFM image of the a-IGZO layer. a-IGZO with a thickness of ~8 nm shows a smooth surface with root-mean-square (RMS) roughness of 0.55 nm, which is confirmed by the AFM image with a scan area of 5 $\mu$m $\times$ 5 $\mu$m.
Supplementary Fig. 3 Simulation of FG a-IGZO TFTs to illustrate the tunneling mechanism. 

**a** Structure of the device. The source/drain metal is not drawn and replaced by the contact. Energy band diagrams are extracted along the direction perpendicular to the channel. 

**b** Energy band diagram of the device under a positive $V_{GS}$. Electrons in the a-IGZO channel tunnel into the FG through the tunneling oxide. 

**c** Energy band diagram of the device under a negative $V_{GS}$. Electrons tunnel back after applying a negative voltage on the control gate.
Supplementary Fig. 4 Top-view SEM image of the ultra-scaled device channel. The $L_{CH}$ of 60 nm is confirmed by the SEM image.

Supplementary Fig. 5 Transfer characteristics of devices with different $L_{CH}$s. Transfer characteristics of the device with $L_{CH}$ of (a) 100 nm, (b) 200 nm, and (c) 500 nm at $V_{DS}$ of 0.1 V and 1 V are obtained by DC measurement after applying program pulse or erase pulse.
Supplementary Fig. 6 Output characteristics of devices with different $L_{CHs}$. The $I_{DS}-V_{DS}$ curves of devices with $L_{CH}$ of (a) 100 nm, (b) 200 nm, (c) 500 nm, and (d) 5000 nm are measured at the programmed state. $I_{ON}$ obtained at an overdrive voltage of 3 V and a $V_{DS}$ of 3 V saturates when $L_{CH}$ is below 500 nm.
Supplementary Fig. 7 Transfer characteristics of the FG a-IGZO TFT at different temperatures. Device characteristics at temperature of (a) -40 °C, (b) -20 °C, (c) 0 °C, (d) 20 °C, (e) 40 °C, (f) 60 °C, and (g) 80 °C are measured under vacuum conditions.
| This work | $W_{CH}/L_{CH}$ (μm) | $I_{ON}$ (a) ($V_{OV},V_{DS}$) (μA/μm) | $I_{ON}/I_{OFF}$ | Mobility (cm²/V·s) | $SS$ (mV/dec.) | MW (V) | Operate voltage (V) | Cycle | Retention (s) |
|-----------|---------------------|-------------------------------------|-----------------|------------------|------------------|--------|---------------------|--------|---------------|
| 2021 Jeong | 300/100             | 0.1 (6,0.3)                         | ~10^3           | -                | ~750             | 10     | 20                  | >1000  | >10^8         |
| 2021 Bae  | 20/0.14             | 0.2 (20,0.1)                        | ~10^3           | 42               | 380              | 3.14   | 18                  | >1000  | >10^8         |
| 2021 Naq  | 30 μA (b) (20,1)   | ~10^6                               | -               | ~750             | 10               | 20     | >3000               | >10^4  | >10^4         |
| 2020 Ryoo | 100/50              | 0.02 (20,0.1)                       | ~10^3           | -                | ~1200            | ~17    | 20 (c)               | -      | >10^3         |
| 2020 Kim  | 0.05 (15,0.1)       | ~10^6                               | 6.57            | ~1000            | 15               | 20     | >10^4               | >10^4  | >10^4         |
| 2020 Ma   | 10/10               | 1.1 (3,4)                           | >10^8           | 10.96            | 8                | 20     | -                   | >10^7  | >10^7         |
| 2020 Liu  | 60/10               | 0.1 (6,0.1)                         | ~10^6           | -                | 1000             | 8      | 13                  | >10^4  | >10^5         |
| 2020 He   | 1000/80             | 0.01 (6,2)                          | ~10^4           | 500              | 7.3              | 6      | 6 (c)               | >10^6  | >10^6         |
| 2019 Yang | 40/40               | 0.01 (12,1)                         | ~10^6           | -                | 1110             | 20     | 20 (c)              | -      | >6000         |
| 2019 Yoon | 0.03 (12,0.1)       | ~10^7                               | 6               | 200              | 25.6             | 20     | >8000               | >10^4  | >10^4         |
| 2019 Kim  | 0.075 (15,0.1)      | ~10^3                               | -               | ~200             | 15.2             | 15     | >1000               | >10^4  | >10^4         |
| 2019 Son  | 40/20               | 0.05 (12,0.1)                       | ~10^6           | -                | ~200             | 13.8   | 20 (c)              | >1000  | >10^3         |
| 2019 Naq  | 0.25 (15,0.5)       | ~10^7                               | ~200            | 25               | 20 (c)           | -      | >10^4               | >10^4  | >10^4         |
| 2018 Zhang| 80/10               | 0.5 (3,5)                           | 10^6-10^9       | 6.1              | 198              | 5.74   | 16                  | -      | >10^8         |
| 2018 Yang | 1 μA (b) (12,0.1)   | ~10^6                               | ~1000           | 19.8             | 20 (c)           | -      | -                   | -      | -             |
| 2018 Hwang| 20/5                | 0.5 (8,5,1)                         | ~10^6           | 19.3             | 182              | ~2     | 20                  | >10^4  | >10^8         |
| 2018 Koo  | 1000/100            | 0.01 (2,1.5)                        | ~10^4           | -                | ~300             | 0.88   | 9                   | >30    | >10^4         |
| 2017 Ji   | 30/20               | 0.3 (8,-)                           | ~10^3           | -                | ~1300            | 3.7    | 13                  | >400   | >10^8         |
| 2017 Seo  | 0.05 (15,0.1)       | ~10^6                               | -               | ~400             | 8.03             | 18     | -                   | >10^5  | >10^5         |
| 2017 Qian | 0.04 (6,0.1)        | ~10^6                               | 7.1             | 700              | 4.7              | 18     | -                   | >10^8  | >10^8         |
| 2017 Park | ~3 μA (b) (12,0.1)  | ~10^7                               | ~500            | 8                | 20 (c)           | -      | -                   | -      | -             |
| 2016 Ahn  | 10-Oct              | 0.8 (15,1)                          | 10^5-10^6       | 200              | 11.1             | 14     | >10^4               | >10^8  | >10^8         |
| 2016 Yun  | 40/40               | ~0.05 (12,0.1)                      | ~10^7           | 8.71             | 230              | 6.2    | 20                  | -      | >10^4         |
| 2016 Hanh | 80/40               | 0.05 (6,1)                          | ~10^6           | 16.3             | 1150             | 2.12   | 11                  | -      | >10^8         |
| 2016 Pan  | 100/10              | 3 (8,5)                             | ~10^7           | -                | 196              | 4.1    | 20                  | >10^5  | >10^8         |
| 2016 Kim  | 40/20               | 2.5 (10,5,5)                        | ~10^7           | 6                | 250              | 25.6   | 25 (c)              | >8000  | >10^4         |
| 2015 Qian | 0.7 (4,1)           | ~10^8                               | 14.6            | 440              | 4.67             | 19     | >1000               | >10^5  | >10^5         |
| 2015 Kim  | 0.1 (15,0.1)        | ~10^8                               | -               | 320              | 25.8             | 30 (c) | -                   | >10^4  | >10^4         |
| 2015 Zhang| 50/10               | 0.1 (2,1)                           | ~10^6           | 2                | 840              | 4.68   | 15                  | >100   | >10^5         |
| 2015 Bak  | 0.05 (15,0.1)       | ~10^7                               | 0.13            | 0.8              | 19.4             | 20 (c) | >10^4               | >10^5  | >10^5         |
| 2015 Li   | 0.01 (12,0.1)       | ~10^5                               | 6.2             | 240              | 14.4             | 20     | -                   | >10^5  | >10^5         |
| 2015 Her  | 0.4 (6,1)           | ~10^6                               | -               | 0.51             | 410              | 7.7    | 20                  | -      | >10^8         |
| 2014 Bak  | 0.05 (20,0.1)       | ~10^7                               | -               | ~400             | 17.1             | 20     | >10^4               | >10^4  | >10^4         |
| 2014 Bak  | 0.05 (20,0.1)       | ~10^7                               | -               | ~400             | 17.1             | 20     | >10^4               | >10^4  | >10^4         |
| Year  | Authors | Width | Overdrive | Overdrive (μA/μm) | Drain | Subthreshold  | Ion | Ioff | Ion/Ioff |
|-------|---------|-------|-----------|-------------------|-------|---------------|-----|------|----------|
| 2014  | Chen    | 100/35| 0.002 (3.0,1) | ~10⁴ | 2.28 | 665 | 1.99 | 12 | - | >10⁴ |
| 2013  | Cui     | 50/5  | 0.07 (2.5) | ~10⁶ | 8.4 | 390 | 6.15 | 10 | (c) | >100 >10⁸ |
| 2013  | Chen    | 100/25| 0.0025 (2.5,8) | ~10⁴ | - | ~600 | 6.38 | 15 | - | >10⁴ |
| 2012  | Nguyen  | 80/12 | 0.05 (5,1) | ~10⁷ | - | ~200 | 3 | 10 | - | >10⁸ |
| 2012  | Jung    | 20/5 | - | - | - | ~8 | 20 | - | - | >10⁵ |
| 2011  | Jang    | 50/10 | 0.1 (15,0.1) | ~10⁷ | - | 1200 | 4.7 | 35 | >1050 |
| 2011  | Nguyen  | 64/32 | 0.1 (3,1)) | ~10⁷ | 4.18 | 130 | 3.19 | 14 | - | - |
| 2010  | Park    | 50/5 | 0.0003 (30,20) | ~10³ | - | 8000 | 15 | 50 | >200 | >10⁸ |
| 2010  | Su      | 500/50| 0.015 | ~10⁶ | - | 128 | 1.6 | 12 | >5000 | >10⁷ |
| 2009  | Suresh  | 400/100| 0.25 (10,10) | ~10⁷ | 14 | 200 | 5.1 | 10 | (c) | - | >10⁵ |
| 2008  | Yin     | 50/4 | 0.5 (4,1.1) | ~10⁸ | 10.3 | 220 | 3.5 | 11 | - | >10⁴ |
| 2008  | Yin     | 50/4 | 0.52 (4,1.1) | ~10⁸ | 10.3 | 207 | 3.8 | 12 | >1000 | >10⁴ |

- **a**: Overdrive voltage: \( V_{OV} = V_{GS} - V_{TH} \)
- **b**: Not normalized to the channel width.
- **c**: Obtained by DC sweep, not by applying pulses

**Supplementary Table 1** Performance benchmark table for flash memories using the *a*-IGZO channel. Devices reported in this work show the shortest \( L_{CH} \) with the best control of short-channel effects (\( SS = \sim 105 \text{ mV/dec. for } L_{CH} = 60 \text{ nm} \)), achieving the highest \( I_{ON} \) of 127 µA/µm \((V_{OV} = 4 \text{ V}, V_{DS} = 3 \text{ V})\) and the lowest operating voltage of 6 V among all the flash memories based on an *a*-IGZO channel. The high \( I_{ON} \) and ultra-low \( I_{OFF} \) also result in the high \( I_{ON}/I_{OFF} \) of more than 8 orders.

| TCAM state | Search bit (SL, SL) | ML | Condition |
|------------|---------------------|----|-----------|
| Logic (D₀, D₁) | (0, 1) | 0 (0, 1) | 1 | Match |
|             | 1 (1, 0) | 0 | Mismatch |
|             | 0 (0, 1) | 0 | Mismatch |
|             | 1 (1, 0) | 1 | Match |
|             | 1 (1, 1) | 0 or 1 | 1 | Match |

\( ML = \text{XNOR (TCAM state, Search bit)} \)

**Supplementary Table 2** Operation schemes of conventional 16T-CMOS TCAM cell. The logic state \((0, 1, X)\) of the TCAM cell is indicated by the states of SRAM. The logic state of the
search bit is indicated by the states of search lines (SL and $\overline{SL}$). The output of the ML is determined by the XNOR result of the stored TCAM state and the search bit.

Supplementary Fig. 8 Top-view SEM image of the TCAM cell. The TCAM cell consists of two parallel-connected FG $a$-IGZO TFTs.

Supplementary Fig. 9 $I_{DS}-V_{GS}$ curves after applying pulses during TCAM measurement. The negative erase pulse (-4.2 V, 1 ms) only partially shifts the $V_{TH}$ of the transistor. If the transistor is entirely erased, it can be switched on even at the search voltage of 0 V (Another method is to apply a lower $V_{SL,L}$).
Supplementary Fig. 10 Schematic of the measurement setup of TCAM cell. The ML of the TCAM cell is connected to an external resistor (3 MΩ). The other terminal of the resistor is connected to the power supply with a $V_{DD}$ of 1.2 V. Input pulses for writing and searching are generated by the two-channel pulse measurement unit (PMU). The waveforms of the search lines and the ML are plotted by the oscilloscope.
Supplementary Fig. 11 Writing ‘0’ and ‘X’ and corresponding search schemes. a. Operation of writing ‘0’ and corresponding search (b) ‘1’, and (c) ‘0’ schemes. d. Operation of writing ‘X’ and corresponding search (e) ‘1’, and (f) ‘0’ schemes. The ML keeps high for both searching ‘1’ and ‘0’ after writing ‘X’.

Supplementary Fig. 12 Modeling and fitting of FG a-IGZO TFT ($L_{CH} = 60$ nm) for array-level simulation. The model used for simulations is well-calibrated according to the experimental data. $V_{SL,L}$ is set to -2 V, while $V_{SL,H}$ is set to vary from 0 V to 1 V.
Supplementary Fig. 13 Key process steps of the FG a-IGZO TFT and TCAM. The TCAM cell can be formed during source/drain patterning by connecting the source and drain terminals of two TFTs, respectively.
References

1. Jayanti, S., Xiangyu Yang, Suri, R. & Misra, V. Ultimate scalability of TaN metal floating gate with incorporation of high-K blocking dielectrics for Flash memory applications. in 2010 International Electron Devices Meeting 5.3.1-5.3.4 (2010).

2. Wang, J. & Wang, M. Separation of the geometric current in charge pumping measurement of polycrystalline Si thin-film transistors. IEEE Trans. Electron Devices 61, 4113–4119 (2014).

3. Zhao, C., Zhao, C. Z., Taylor, S. & Chalker, P. R. Review on Non-Volatile Memory with High-k Dielectrics: Flash for Generation Beyond 32 nm. Materials 7, 5117–5145 (2014).

4. Pavan, P., Bez, R., Olivo, P. & Zanoni, E. Flash memory cells—an overview. Proc. IEEE 85, 1248–1271 (1997).

5. Lue, H.-T. et al. Optimal design methods to transform 3D NAND flash into a high-density, high-bandwidth and low-power nonvolatile computing in memory (nvCIM) accelerator for deep-learning neural networks (DNN). in 2019 IEEE International Electron Devices Meeting (IEDM) 38.1.1-38.1.4 (2019).

6. Wang, P. et al. Three-dimensional NAND flash for vector–matrix multiplication. IEEE Trans. Very Large Scale Integr. VLSI Syst. 27, 988–991 (2019).

7. Goda, A. 3-D NAND technology achievements and future scaling perspectives. IEEE Trans. Electron Devices 67, 1373–1381 (2020).

8. Jeong, M.-K. et al. Analysis of random telegraph noise and low frequency noise properties in 3-D stacked NAND flash memory with tube-type poly-Si channel structure. in 2012 Symposium on VLSI Technology (VLSIT) 55–56 (2012).
9. Wu, J. *et al.* Comprehensive investigations on charge diffusion physics in SiN-based 3D NAND flash memory through systematical Ab initio calculations. in *2017 IEEE International Electron Devices Meeting (IEDM)* 4.5.1-4.5.4 (2017).

10. Miyagawa, H. *et al.* Metal-assisted solid-phase crystallization process for vertical monocrystalline Si channel in 3D flash memory. in *2019 IEEE International Electron Devices Meeting (IEDM)* 28.3.1-28.3.4 (2019).

11. Delhougne, R. *et al.* First demonstration of monocrystalline silicon macaroni channel for 3-D NAND memory devices. in *2018 IEEE Symposium on VLSI Technology* 203–204 (2018).

12. Monzio Compagnoni, C. & Spinelli, A. S. Reliability of NAND flash arrays: A review of what the 2-D–to–3-D transition meant. *IEEE Trans. Electron Devices* **66**, 4504–4516 (2019).

13. Park, J. K. *et al.* Surface-controlled ultrathin (2 nm) poly-Si channel junctionless FET towards 3D NAND flash memory applications. in *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers* 1–2 (2014).

14. Kim, B. *et al.* Investigation of ultra thin polycrystalline silicon channel for vertical NAND flash. in *2011 International Reliability Physics Symposium* 2E.4.1-2E.4.4 (2011).

15. Lue, H.-T. *et al.* Advantage of extremely-thin body (Tsi~3nm) device to boost the memory window for 3D NAND flash. in *2019 Symposium on VLSI Technology* T210–T211 (2019).

16. Wang, B., Gao, B., Wu, H. & Qian, H. A drain leakage phenomenon in poly silicon channel 3D NAND flash caused by conductive paths along grain boundaries. *Microelectron. Eng.* **192**, 66–69 (2018).

17. Wong, M., Chow, T., Wong, C. C. & Zhang, D. A quasi two-dimensional conduction model for polycrystalline silicon thin-film transistor based on discrete grains. *IEEE Trans. Electron Devices* **55**, 2148–2156 (2008).
18. Resnati, D. et al. Temperature effects in NAND flash memories: A comparison between 2-D and 3-D arrays. *IEEE Electron Device Lett.* **38**, 461–464 (2017).

19. Nomura, K. et al. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **432**, 488–492 (2004).

20. Lee, S. & Nathan, A. Subthreshold Schottky-barrier thin-film transistors with ultralow power and high intrinsic gain. *Science* **354**, 302–304 (2016).

21. Si, M. et al. Indium-tin-oxide transistors with one nanometer thick channel and ferroelectric gating. *ACS Nano* **14**, 11542–11547 (2020).

22. Venkatesan, S. & Aoulaiche, M. Overview of 3D NAND technologies and outlook. in *2018 Non-Volatile Memory Technology Symposium (NVMTS)* 1–5 (2018).

23. Chen, H., Cao, Y., Zhang, J. & Zhou, C. Large-scale complementary macroelectronics using hybrid integration of carbon nanotubes and IGZO thin-film transistors. *Nat. Commun.* **5**, 4097 (2014).

24. Sun, C. et al. First demonstration of BEOL-compatible ferroelectric TCAM featuring a-IGZO Fe-TFTs with large memory window of 2.9 V, scaled channel length of 40 nm, and high endurance of $10^8$ cycles. in *2021 Symposium on VLSI Technology* 1–2 (2021).

25. He, Y. et al. Dual-functional long-term plasticity emulated in IGZO-based photoelectric neuromorphic transistors. *IEEE Electron Device Lett.* **40**, 818–821 (2019).

26. Han, K. et al. First demonstration of oxide semiconductor nanowire transistors: A novel digital etch technique, IGZO channel, nanowire width down to ~20 nm, and $I_{on}$ exceeding 1300 $\mu$A/$\mu$m. in *Symposium on VLSI Technology Digest of Technical Papers* 2 (2021).

27. Ozer, E. et al. A hardwired machine learning processing engine fabricated with submicron metal-oxide thin-film transistors on a flexible substrate. *Nat. Electron.* **3**, 419–425 (2020).
28. Myny, K. The development of flexible integrated circuits based on thin-film transistors. *Nat. Electron.* **1**, 30–39 (2018).

29. Kim, Y.-H. *et al.* Flexible metal-oxide devices made by room-temperature photochemical activation of sol–gel films. *Nature* **489**, 128–132 (2012).

30. Mallik, A. *et al.* The impact of sequential-3D integration on semiconductor scaling roadmap. In *2017 IEEE International Electron Devices Meeting (IEDM)* 32.1.1–31.1.4 (2017).

31. Kwon, J. *et al.* Three-dimensional monolithic integration in flexible printed organic transistors. *Nat. Commun.* **10**, 54 (2019).

32. Liu, Y., Zhang, J. & Peng, L.-M. Three-dimensional integration of plasmonics and nanoelectronics. *Nat. Electron.* **1**, 644–651 (2018).

33. Salahuddin, S., Ni, K. & Datta, S. The era of hyper-scaling in electronics. *Nat. Electron.* **1**, 442–450 (2018).

34. Samanta, S. *et al.* Amorphous IGZO TFTs featuring extremely-scaled channel thickness and 38 nm channel length: Achieving record high Gm,max of 125 μS/μm at VDS of 1 V and ION of 350 μA/μm. In *2020 IEEE Symposium on VLSI Technology* 1–2 (2020).

35. Uchida, K. *et al.* Experimental study on carrier transport mechanism in ultrathin-body SOI n- and p-MOSFETs with SOI thickness less than 5 nm. In *Digest. International Electron Devices Meeting*, 47–50 (2002).

36. Li, S. *et al.* Nanometre-thin indium tin oxide for advanced high-performance electronics. *Nat. Mater.* **18**, 1091–1097 (2019).

37. Subhechha, S. *et al.* First demonstration of sub-12 nm Lg gate last IGZO-TFTs with oxygen tunnel architecture for front gate devices. *Symp. VLSI Technol. Dig. Tech. Pap.* 2 (2021).
38. Ji, H., Wei, Y., Zhang, X. & Jiang, R. Homogeneous-oxide stack in IGZO thin-film transistors for multi-level-cell NAND memory application. *Appl. Phys. Lett.* **111**, 202102 (2017).

39. Qian, S., Zhang, W., Liu, W. & Ding, S. Electrically programmable-erasable In-Ga-Zn-O thin-film transistor memory with atomic-layer-deposited Al$_2$O$_3$/Pt nanocrystals/Al$_2$O$_3$ gate stack. *AIP Adv.* **5**, 127203 (2015).

40. Zhang, W. *et al.* Demonstration of α-InGaZnO TFT nonvolatile memory using TiAlO charge trapping layer. *IEEE Trans. Nanotechnol.* **17**, 1089–1093 (2018).

41. Fedorov, V. V., Abusultan, M. & Khatri, S. P. An area-efficient ternary CAM design using floating gate transistors. in *2014 IEEE 32nd International Conference on Computer Design (ICCD)* 55–60 (2014).

42. Ni, K. *et al.* Ferroelectric ternary content-addressable memory for one-shot learning. *Nat. Electron.* **2**, 521–529 (2019).

43. Nii, K. *et al.* A 28nm 400MHz 4-parallel 1.6Gsearch/s 80Mb ternary CAM. in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)* 240–241 (2014).

44. Yang, R. *et al.* Ternary content-addressable memory with MoS$_2$ transistors for massively parallel data search. *Nat. Electron.* **2**, 108–114 (2019).

45. Li, J., Montoye, R. K., Ishii, M. & Chang, L. 1 Mb 0.41 µm$^2$ 2T-2R cell nonvolatile TCAM with two-bit encoding and clocked self-referenced sensing. *IEEE J. Solid-State Circuits* **49**, 896–907 (2014).
46. Lin, C.-C. et al. A 256b-wordlength ReRAM-based TCAM with 1ns search-time and $14\times$ improvement in wordlength-energy-efficiency-density product using 2.5T1R cell. in 2016 IEEE International Solid-State Circuits Conference (ISSCC) 136–137 (2016).

47. Yin, X. et al. An ultra-dense 2FeFET TCAM design based on a multi-domain FeFET model. IEEE Trans. Circuits Syst. II Express Briefs 66, 1577–1581 (2019).

48. Yin, X. et al. FeCAM: A universal compact digital and analog content addressable memory using ferroelectric. IEEE Trans. Electron Devices 67, 2785–2792 (2020).

49. Sze, S. M., Li, Y. & Ng, K. K. Physics of Semiconductor Devices. (2021).

50. Auth, C. P. & Plummer, J. D. Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET’s. IEEE Electron Device Lett. 18, 74–76 (1997).

51. Yan, R.-H., Ourmazd, A. & Lee, K. F. Scaling the Si MOSFET: from bulk to SOI to bulk. IEEE Trans. Electron Devices 39, 1704–1710 (1992).

52. Kato, K. et al. Evaluation of off-state current characteristics of transistor using oxide semiconductor material, indium–gallium–zinc oxide. Jpn. J. Appl. Phys. 51, 021201 (2012).

53. Imani, M. et al. SearcHD: A memory-centric hyperdimensional computing with stochastic training. IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. 39, 2422–2433 (2020).

54. Ge, L. & Parhi, K. K. Classification using hyperdimensional computing: A review. IEEE Circuits Syst. Mag. 20, 30–47 (2020).

55. Kunitake, H. et al. High thermal tolerance of 25-nm c-axis aligned crystalline In-Ga-Zn oxide FET. in 2018 IEEE International Electron Devices Meeting (IEDM) 13.6.1-13.6.4 (2018).

56. Ng, K. K. & Lynch, W. T. The impact of intrinsic series resistance on MOSFET scaling. IEEE Trans. Electron Devices 34, 503–511 (1987).
57. Yang, S.-H. et al. Low resistance ohmic contacts to amorphous IGZO thin films by hydrogen plasma treatment. *Surf. Coat. Technol.* **206**, 5067–5071 (2012).

58. Cao, W., Kang, J., Bertolazzi, S., Kis, A. & Banerjee, K. Can 2D-nanocrystals extend the lifetime of floating-gate transistor based nonvolatile memory? *IEEE Trans. Electron Devices* **61**, 3456–3464 (2014).

59. Kim, S. et al. Comparison of temperature dependent carrier transport in FinFET and gate-all-around nanowire FET. *Appl. Sci.* **10**, 2979 (2020).

60. Chain, K., Huang, J., Duster, J., Ko, P. K. & Hu, C. A MOSFET electron mobility model of wide temperature range (77 - 400 K) for IC simulation. *Semicond. Sci. Technol.* **12**, 355–358 (1997).

61. International roadmap for devices and systems (IRDS), http://irds.ieee.org/.

62. Auth, C. et al. A 10nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, Self-Aligned Quad Patterning, contact over active gate and cobalt local interconnects. in *2017 IEEE International Electron Devices Meeting (IEDM)* 29.1.1-29.1.4 (2017).

63. Yang, H. Z. et al. A novel high-density and low-power ternary content addressable memory design based on 3D NAND flash. in *2020 IEEE Silicon Nanoelectronics Workshop (SNW)* 29–30 (2020).

64. Sun, C. et al. Highly scaled InGaZnO ferroelectric field-effect transistors and ternary content-addressable memory. *IEEE Trans. Electron Devices* **69**, 5262–5269 (2022).

65. Jeong, S., Jang, S., Han, H., Kim, H. & Choi, C. C-axis aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO) and high-k charge trapping film for flash memory application. *J. Alloys Compd.* **888**, 161440 (2021).
66. Bae, S.-H. *et al.* Characterization of nanoscale vertical-channel charge-trap memory thin film transistors using oxide semiconducting active and trap layers. *J. Vac. Sci. Technol. B* **39**, 043202 (2021).

67. Naqi, M. *et al.* High-Performance Non-Volatile InGaZnO Based Flash Memory Device Embedded with a Monolayer Au Nanoparticles. *Nanomaterials* **11**, 1101 (2021).

68. Ryoo, H.-J. & Yoon, S.-M. Channel conductance modulation of dual-gate charge-trap oxide synapse TFT using In-Ga-Zn-O channel and ZnO trap layers. *IEEE Electron Device Lett.* **41**, 1661–1664 (2020).

69. Kim, H.-R. *et al.* Comparative studies on vertical-channel charge-trap memory thin-film transistors using In-Ga-Zn-O active channels deposited by sputtering and atomic layer depositions. *Nanotechnology* **31**, 435702 (2020).

70. Ma, P. *et al.* Charge-trapping memory based on tri-layer alumina gate stack and InGaZnO channel. *Semicond. Sci. Technol.* **35**, 055032 (2020).

71. Liu, D.-D. *et al.* Multilevel memory and synaptic characteristics of a-IGZO thin-film transistor with atomic layer–deposited Al₂O₃/ZnO/Al₂O₃ stack layers. *J. Mater. Res.* **35**, 732–737 (2020).

72. He, Y. *et al.* IGZO-based floating-gate synaptic transistors for neuromorphic computing. *Appl Phys* **7** (2020).

73. Yang, J., Kim, D., Yoon, M., Kim, G. & Yoon, S. Mechanically robust and highly flexible nonvolatile charge-trap memory transistors using conducting-polymer electrodes and oxide semiconductors on ultrathin polyimide film substrates. *Adv. Mater. Technol.* **4**, 1900348 (2019).
74. Yoon, S.-M. et al. Charge-trap-assisted flexible nonvolatile memory applications using oxide-semiconductor thin-film transistors. *Jpn. J. Appl. Phys.* **58**, 090601 (2019).

75. Kim, H.-R., Kang, C.-S., Kim, S.-K., Byun, C.-W. & Yoon, S.-M. Characterization on the operation stability of mechanically flexible memory thin-film transistors using engineered ZnO charge-trap layers. *J. Phys. Appl. Phys.* **52**, 325106 (2019).

76. Son, M.-T., Kim, S.-J. & Yoon, S.-M. Impacts of bottom-gate bias control for low-voltage memory operations of charge-trap memory thin film transistors using oxide semiconductors. *J. Semicond. Technol. Sci.* **19**, 69–78 (2019).

77. Na, S.-Y. & Yoon, S.-M. Impacts of HfO₂/ZnO stack-structured charge-trap layers controlled by atomic layer deposition on nonvolatile memory characteristics of In-Ga-Zn-O channel charge-trap memory thin-film transistors. *IEEE J. Electron Devices Soc.* **7**, 453–461 (2019).

78. Yang, J.-H., Kim, G.-H. & Yoon, S.-M. Investigation of mechanical-stress-induced electrical failure of oxide-based flexible charge-trap memory thin-film transistors fabricated on plastic substrates. in *2018 25th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD)* 1–4 (2018).

79. Hwang, E. S. et al. In₂Ga₂ZnO₇ oxide semiconductor based charge trap device for NAND flash memory. *Nanotechnology* **29**, 155203 (2018).

80. Koo, J. et al. Nonvolatile electric double-layer transistor memory devices embedded with Au nanoparticles. *ACS Appl. Mater. Interfaces* **10**, 9563–9570 (2018).

81. Seo, G. H., Yun, D. J., Lee, W. H. & Yoon, S. M. Atomic-layer-deposition-assisted ZnO nanoparticles for oxide charge-trap memory thin-film transistors. *Nanotechnology* **28**, 075202 (2017).
82. Qian, S.-B., Wang, Y.-P., Shao, Y., Liu, W.-J. & Ding, S.-J. Plasma-assisted atomic layer deposition of high-density Ni nanoparticles for amorphous In-Ga-Zn-O thin film transistor memory. *Nanoscale Res. Lett.* **12**, 138 (2017).

83. Qian, S.-B., Shao, Y., Liu, W.-J., Zhang, D. W. & Ding, S.-J. Erasing-modes dependent performance of a-IGZO TFT memory with atomic-layer-deposited Ni nanocrystal charge storage layer. *IEEE Trans. ELECTRON DEVICES* **64**, 5 (2017).

84. Park, M.-J. *et al*. Preparation of mono-layered Ag nanoparticles for charge-trap sites of memory thin-film transistors using In-Ga-Zn-O channel. *ECS J. Solid State Sci. Technol.* **6**, Q18–Q22 (2017).

85. Ahn, M.-J. & Cho, W.-J. Transparent multi-level-cell nonvolatile memory with dual-gate amorphous indium-gallium-zinc oxide thin-film transistors. *Appl. Phys. Lett.* **109**, 252106 (2016).

86. Yun, D.-J., Kang, H.-B. & Yoon, S.-M. Process optimization and device characterization of nonvolatile charge trap memory transistors using In–Ga–ZnO thin films as both charge Trap and active channel layers. *IEEE Trans. Electron Devices* **63**, 3128–3134 (2016).

87. Hanh, N. H., Jang, K. & Yi, J. Fabrication of InGaZnO nonvolatile memory devices at low temperature of 150 °C for applications in flexible memory displays and transparency coating on plastic substrates. *J. Nanosci. Nanotechnol.* **16**, 4860–4863 (2016).

88. Pan, T.-M., Chen, C.-H., Hu, Y.-H. & Her, J.-L. Effect of Ti content on the structural and electrical characteristics of ErTi_xO_y charge storage layer in InGaZnO thin-film transistor nonvolatile memories. *IEEE Trans. Electron Devices* **63**, 1539–1544 (2016).
89. Pan, T.-M., Chen, C.-H., Hu, Y.-H., Wang, H.-C. & Her, J.-L. Comparison of structural and electrical properties of Er$_2$O$_3$ and ErTi$_x$O$_y$ charge-trapping layers for InGaZnO thin-film transistor nonvolatile memory devices. *IEEE Electron Device Lett.* **37**, 179–181 (2016).

90. Kim, S.-J. *et al.* High performance and stable flexible memory thin-film transistors using In–Ga–Zn–O channel and ZnO charge-trap layers on poly(ethylene naphthalate) substrate. *IEEE Trans. Electron Devices* **63**, 1557–1564 (2016).

91. Kim, S. J., Lee, W. H., Byun, C. W., Hwang, C. S. & Yoon, S. M. Photo-stable transparent nonvolatile memory thin-film transistors using In–Ga–Zn–O channel and ZnO charge-trap layers. *IEEE Electron Device Lett.* **36**, 1153–1156 (2015).

92. Zhang, W.-P., Qian, S.-B., Liu, W.-J., Ding, S.-J. & Zhang, D. W. Novel multi-level cell TFT memory with an In–Ga–Zn–O charge storage layer and channel. *IEEE Electron Device Lett.* **36**, 1021–1023 (2015).

93. Bak, J. Y. *et al.* Effects of thickness and geometric variations in the oxide gate stack on the nonvolatile memory behaviors of charge-trap memory thin-film transistors. *Solid-State Electron.* **111**, 153–160 (2015).

94. Ya Li *et al.* Charge trapping memory characteristics of amorphous-indium–gallium–zinc oxide thin-film transistors with defect-engineered alumina dielectric. *IEEE Trans. Electron Devices* **62**, 1184–1188 (2015).

95. Her, J.-L., Chen, F.-H., Chen, C.-H. & Pan, T.-M. Electrical characteristics of gallium–indium–zinc oxide thin-film transistor non-volatile memory with Sm$_2$O$_3$ and SmTiO$_3$ charge trapping layers. *RSC Adv.* **5**, 8566–8570 (2015).
96. Bak, J. Y. & Yoon, S. M. High-performance transparent, all-oxide nonvolatile charge trap memory transistor using In-Ga-Zn-O channel and ZnO trap layer. *J. Vac. Sci. Technol. B Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.* **32**, 060604 (2014).

97. Bak, J. Y., Ryu, M.-K., Park, S. H. K., Hwang, C.-S. & Yoon, S. M. Impact of charge-trap layer conductivity control on device performances of top-gate memory thin-film transistors using IGZO channel and ZnO charge-trap layer. *IEEE Trans. Electron Devices* **61**, 2404–2411 (2014).

98. Bak, J. Y., Ryu, M.-K., Park, S. H. K., Hwang, C. S. & Yoon, S. M. Nonvolatile charge-trap memory transistors with top-gate structure using In–Ga–Zn–O active channel and ZnO charge-trap layer. *IEEE Electron Device Lett.* **35**, 357–359 (2014).

99. Chen, S. et al. Monochromatic light-assisted erasing effects of In-Ga-Zn-O thin film transistor memory with Al2O3/Zn-doped Al2O3/Al2O3 stacks. *Appl. Phys. Lett.* **104**, 103504 (2014).

100. Cui, X.-M. et al. Unique UV-erasable In-Ga-Zn-O TFT memory with self-assembled Pt nanocrystals. *IEEE Electron Device Lett.* **34**, 1011–1013 (2013).

101. Chen, S. et al. Novel Zn-doped Al2O3 charge storage medium for light-erasable In–Ga–Zn–O TFT memory. *IEEE Electron Device Lett.* **34**, 1008–1010 (2013).

102. Nguyen, H. H. et al. Investigation of charge storage and retention characteristics of silicon nitride in NVM based on InGaZnO channels for system-on-panel applications. *Microelectron. Eng.* **98**, 34–40 (2012).

103. Sim Jung, J. et al. The charge trapping characteristics of Si3N4 and Al2O3 layers on amorphous-indium-gallium-zinc oxide thin films for memory application. *Appl. Phys. Lett.* **100**, 183503 (2012).
104. Jang, J. et al. Endurance characteristics of amorphous-InGaZnO transparent flash memory with gold nanocrystal storage layer. *IEEE Trans. Electron Devices* **58**, 3940–3947 (2011).

105. Nguyen, H. H. et al. Fabrication of SiO$_2$/SiO$_x$/SiO$_x$N$_y$ non-volatile memory with transparent amorphous indium gallium zinc oxide channels. *J. Electrochem. Soc.* **158**, H1077 (2011).

106. Park, Y.-S., Lee, S. Y. & Lee, J.-S. Nanofloating gate memory devices based on controlled metallic nanoparticle-embedded InGaZnO TFTs. *IEEE Electron Device Lett.* **31**, 1134–1136 (2010).

107. Su, N.-C., Wang, S. J. & Chin, A. A nonvolatile InGaZnO charge-trapping-engineered flash memory with good retention characteristics. *IEEE Electron Device Lett.* **31**, 201–203 (2010).

108. Suresh, A., Novak, S., Wellenius, P., Misra, V. & Muth, J. F. Transparent indium gallium zinc oxide transistor based floating gate memory with platinum nanoparticles in the gate dielectric. *Appl. Phys. Lett.* **94**, 123501 (2009).

109. Yin, H. et al. Fully transparent nonvolatile memory employing amorphous oxides as charge trap and transistor’s channel layer. *Appl. Phys. Lett.* **93**, 172109 (2008).

110. Yin, H. et al. Program/erase characteristics of amorphous gallium indium zinc oxide nonvolatile memory. *IEEE Trans. Electron Devices* **55**, 2071–2077 (2008).