Abstract—This study proposes a new method to measure the polarization charge of ferroelectric field-effect transistors (FeFETs) using a pulse generator and source measurement unit (SMU) and exploiting the charge pumping (CP) principle, which is widely followed to measure the interface trap charge density ($D_{it}$) of MOSFETs. Although the pulse waveforms applied to the gate electrode were equal to that of conventional polarization charge measurement methods, the response current was measured using the SMU similar to that in CP. As the proposed method measured the average dc current on the well or source/drain terminal, it provided a reliable quantification of polarization charges with low noises even at lower applied voltages. This measurement is possible because the ferroelectric (FE) dipole-induced charge is immovable, similar to an interface charge that is not moved by an interface trap until it recombines with a movable opposite carrier. This method conveniently measured the switching charge even for $<50$ ns of rising/falling time of the applied pulse. Moreover, as the read current resolution of the SMU is $<5 \times 10^{-12}$ A, the switching charge can be measured with a device area $<1$ $\mu$m$^2$. Thus, the proposed CP-based method proved to be a highly effective method of polarization charge measurement for three- or four-terminal devices, such as FeFETs, unless the measurement requires the hysteresis curve along with polarization charges.

Index Terms—Charge pumping (CP), ferroelectric (FE), ferroelectric field-effect transistor (FeFET), HfO$_2$, HfZrO$_2$ (HZO), polarization charge.

I. INTRODUCTION

SINCE the first report in 2011 describing the ferroelectric (FE) properties of HfO$_2$-based thin films, these films have been extensively investigated as materials for nonvolatile memory applications, such as in FE field-effect transistors (FeFETs), FE random access memory devices, and FE tunneling junction devices [1]–[7]. In addition, they have drawn interest for applications in low-power semiconductor devices, such as negative capacitance field-effect transistors (NCFETs) [8], [9]. This is because HfO$_2$-based FEs are compatible with the mass production process of commercial high-$k$/metal gate CMOS and can maintain spontaneous polarization in 3-D structures or ultrathin films (thickness $<10$ nm) [3]. Generally, the electrical properties of FEs feature the remanent polarization and the consequent hysteresis in the polarization–voltage ($P–V$) curve, which is characterized by typically applying triangular or positive-up negative-down (PUND) pulses to a device [1]. In particular, the information such as the remanent polarization ($P_r$) or the coercive voltage ($V_c$) from FE devices can be obtained from the $P–V$ hysteresis curves that are typically measured from two-terminal structures, e.g., metal–FE–metal or metal–FE–Si (high-dose) capacitors. In metal–FE–Si (low-dose) (MFS) structures, however, the external voltage is divided into two FE and depletion layers of the Si channel in FeFETs or NCFETs, which results in failure in polarization switching of the FE layer in the depletion mode. Recently, Toprasetpong et al. [10] reported that spontaneous polarization in an MFS structure can be measured by adding a source or drain terminal in a three-terminal structure.

In this study, we suggest a simpler and more reliable method of measuring the $P_r$ of FeFETs based on the charge pumping (CP) method, which has been traditionally employed to measure interface trap charges in MOSFETs [17]. The reliability and stability are naturally enhanced because the CP method measures the steady-state dc current from the source/drain (S/D) or well by applying voltage pulses to the gate node. This study proposes a novel measurement method by combining the existing $P–V$ and CP measurement methods. Although the shape of the pulses applied to the gate node is identical to those in the conventional method, the current measurement uses the same source measurement units (SMUs) as the CP method. The SMU displays a higher resolution than that of an oscilloscope (OSC) and is easier to use. Therefore, this is a simpler and more reliable method of measuring $P_r$ compared to the traditional method of directly measuring the response current using an OSC.

The rest of this article is organized as follows. In Section II, the test devices and the details of the test instruments are introduced. In Section III-A, measuring the capacitance–voltage ($C–V$) and CP in FeFET results in different charge trap densities ($D_{it}$) and CP curve slopes. The evaluation of the
rising time \((t_r)\) and the falling time \((t_f)\) in CP measurements showed that these differences were not due to interface traps. In Section III-B, if the waveform of the voltage pulse applied to a gate electrode has the same in CP and \(P–V\) measurements, the current measured is the same. Therefore, the \(P_r\) value could be measured using the CP method. In Section III-C, the origin of the current measured by the CP and \(P–V\) method has been described. Finally, Section IV concludes this article.

II. EXPERIMENT

This experiment used an n-type MOS planar transistor that was fabricated following the gate last process. On the p-type Si substrate, poly Si was used as a dummy gate and removed after activation annealing of n+ S/D at 1050 °C. After precleaning with HF and the formation of SC1 interface oxide, HfO\(_2\) and HfZrO\(_2\) (HZO) films were deposited using atomic layer deposition at 300 °C, wherein HfCl\(_4\), ZrCl\(_4\), and H\(_2\)O were utilized as sources and oxidant. After HfO\(_2\) deposition, postdeposition annealing (PDA) at 850 °C was conducted prior to forming the TiN upper electrode. However, the TiN top electrode of the HZO FE was deposited without PDA. Instead, postmetal annealing (PMA) was conducted at 450 °C to induce the FE characteristics. The Zr content in the HZO film measured using X-ray photoelectron spectroscopy was 20%. Moreover, the thickness of the oxide films was measured using ellipsometry prior to the deposition of the top electrode. In particular, the thickness of HfO\(_2\) was 4.2 nm, and we prepared HZO films with two distinct thicknesses (4 and 5 nm). The voltage pulse for measuring the conventional \(P–V\) hysteresis curve was provided by the commercial measurement tool Waveform Generator/Fast Measurement Unit (WGFMU, B1500A-A30, Keysight Technologies), which has recently been used for measuring the \(P–V\) hysteresis of FE devices [10]. The WGFMU comprises a pulse generator (PG) and a current measurement unit that acts as an OSC. The new measurement method proposed in this article was derived using the Semiconductor Pulse Generator Unit (SPGU, B1525A, Keysight Technologies) and B1500 (Keysight Technologies). The gate length and width of a single transistor were 100 nm and 20 µm, and the total active area of the measurement transistor array was 800 µm\(^2\).

III. RESULTS AND DISCUSSION

A. Results of Charge Density

The typical measurement structure, voltage pulse waveforms, and \(P–V\) curves in FeFETs are illustrated in Fig. 1, wherein the device schematic of FE and dielectric (DE) stack used in this experiment are presented in Fig. 1(a); the pulse shapes for triangular and PUND voltage pulses are depicted in Fig. 1(b) and (c), respectively; and the \(P–V\) hysteresis curves extracted from the current responses of the triangular and PUND pulses are plotted in Fig. 1(d). In case the gate contained an FE and DE series stack, as depicted in Fig. 1(a), the \(P–V\) hysteresis under a triangular pulse represented the total polarization of the FE and DE stack, whereas the hysteresis under the PUND pulse represented only the FE layer polarization as it used the leakage difference between the first and second pulses for charge extraction. Therefore, the \(2P_r\) values obtained using both methods at 0 V represent the identical parameter because the DE charge is zero. The current measured during the voltage swing can be converted into charges and polarization values using (1) and (2), respectively, \[ Q = \int i \, dt \] \[ P_r = \frac{Q}{A} \] where \(Q\) denotes the number of charges, \(i\) denotes the measured current during the voltage swing, \(t\) represents the time, \(P_r\) indicates the polarization charge, and \(A\) represents the gate area. In this study, we demonstrate that the \(P_r\) value measured using this conventional method equal to that obtained by the CP measurement if the applied voltage waveforms are identical.

First, the interface charge density \((D_{it})\) obtained from the C–V curve using the conductance and the CP methods...
are comparatively presented in Fig. 2. In addition, \( D_{it} \) was extracted from the C–V curve and the CP method using (3) and (4)–(6), respectively [12], [17]

\[
D_{it} = \frac{2.5}{qA} \cdot \frac{G_p}{w} \quad (3)
\]

\[
N_{it} = \frac{I_{CP}}{qAf} \quad (4)
\]

\[
I_{CP} = 2qD_{it}f \cdot A \cdot kT \cdot \ln(\sqrt{t_r \cdot t_f}) \quad (5)
\]

\[
D_{it} = \frac{2qf \cdot A \cdot kT \cdot \ln(\sqrt{t_r \cdot t_f})}{C_{it}} \quad (6)
\]

where \( q \) denotes the charge of an electron, \( G_p \) indicates the equivalent parallel conductance, \( w \) denotes the angular frequency, \( I_{CP} \) represents the CP current, \( f \) denotes the measurement frequency, \( k \) represents Boltzmann's constant, \( T \) denotes the temperature in Kelvin, and \( t_r \) and \( t_f \) denote the rising and falling times of the voltage pulse.

The C–V curves presented in Fig. 2(a) were measured under a 10-kHz frequency, 50 mV of small-signal swing, and 0.02 V of voltage sweep step. The dissipation factors with voltage swing are presented in Fig. 2(b), and the maximum peak values in the depletion regions were used to extract \( D_{it} \) using the conductance method (\( G_p/w \) method) as in (3). The CP curves in Fig. 2(c) considered a base level voltage (\( V_{base} \)) of \(-1.0\) V, the measurement frequency of 500 kHz, the duty cycle of 50%, the rising/falling times (\( t_r/t_f \)) of 100 ns, and the maximum peak voltage (\( V_{peak} \)) of 1.0 V. Specifically, the charge numbers presented in Fig. 2(c) were evaluated using (4), and these measurement conditions were typically used for C–V and CP measurements of MOSFETs.

In Fig. 2(d), the \( D_{it} \) values obtained from the conductance method using (3) were compared with those obtained from the CP current using (6). Moreover, \( D_{it} \) of CP was derived from the peak voltage of 0.5 V in Fig. 2(c).

Upon comparing the \( D_{it} \) trend in Fig. 2(d), all samples measured using the conductance method exhibited \( D_{it} \) values in the range of 4.3–6.2 \( \times 10^{11} \) cm\(^{-2}\)eV\(^{-1}\) with slight deviations among the samples. In addition, \( D_{it} \) measured using CP yielded a value of 5.8 \( \times 10^{11} \) cm\(^{-2}\)eV\(^{-1}\) for 4.2-nm HfO\(_2\), 5.1 \( \times 10^{12} \) cm\(^{-2}\)eV\(^{-1}\) for 5-nm HZO, and 6.6 \( \times 10^{12} \) cm\(^{-2}\)eV\(^{-1}\) for 4-nm HZO. As obtained from the CP method, \( D_{it} \) values of the HfO\(_2\) film were 8.8–11.3 times larger than those of the HfO\(_2\) film. Moreover, as depicted in Fig. 2(c), the number of charges by CP in HfO\(_2\) saturated with increasing \( V_{peak} \), but the number of charges in HZO continued to increase, as exemplified in Fig. 3. \( N_{it} \) of 4.2-nm HfO\(_2\) and 4-nm HZO samples is comparatively presented in, Fig. 3(a) and (b) at a fixed rising/falling slope of 10-mV/ns pulse voltage (black squares) and \( t_r/t_f \) at 100 ns (red circles). As indicated by the black squares, \( V_{base} \) and rising/falling sweep rate of the CP measurements were set at \(-1.0\) V and 10 mV/ns, respectively. Consequently, \( t_r/t_f \) increased from 20 to 200 ns as \( V_{peak} \) was swept from \(-0.8\) to 1.0 V. As denoted by the red circles, \( t_r/t_f \) was set at 100 ns, which varied the rising/falling slope from 2 to 20 mV/ns at the same \( V_{peak} \) sweep. As portrayed in Fig. 3(a) and (b), \( V_{peak} \) increased in both HfO\(_2\) and HZO samples, and the set \( t_r/t_f \) slightly increased the number of charges over the fixed rising/falling voltage sweep slope
condition, but the difference was insignificant. The number of charges in HfO$_2$ and HZO are comparatively presented in Fig. 3(c) and (d) according to $t_f/t_i$. As observed, $N_t$ decreased as $t_f/t_i$ increased from 50 to 400 ns; however, the carrier variations of HZO were less than those in $N_t$, resulting from $V_{peak}$ [see Fig. 2(c)]. Therefore, the increasing $N_t$ slope in the measurement of the HZO gate oxide [see Fig. 2(c)] was not caused by the variations in the $t_f/t_i$ or slope of the applied pulse.

B. Comparison of Measurement Methods

Before comparing the FE charges using CP and conventional $P$–$V$ hysteresis methods, we measured the conventional $P$–$V$ hysteresis using the WGF MU. The 2$P_r$ values measured based on the triangular pulse and PUND pulse for HfO$_2$ and HZO samples are summarized in Fig. 4(a) and (b), respectively. In addition, the applied pulse shapes are presented in Fig. 1(b) and (c). The current values of the well and S/D terminal were separately measured and converted into polarization charge [10]. The 2$P_r$ value of the triangular pulse [see Fig. 4(a)] was used to calibrate the oxide leakage at 5 and 10 ms following a two-frequency method [13]. Moreover, the PUND pulse [see Fig. 4(b)] was corrected by subtracting the second pulse leakage from the first pulse leakage. As depicted in Fig. 1(d), the $P$–$V$ hysteresis curve of triangular pulse transformed into an open loop as the peak voltage increased (only $V_{peak}$ of 2.0 V is shown here), which can be attributed to the effect of electron charging in the bulk traps within the HZO thin film at the inversion operation mode. This implied that the gate current in the upward sweep voltage was larger than the downward sweep in the positive voltage swing, thereby resulting in the accumulation of a net charge in the inversion region, which generated the open-loop hysteresis. On the contrary, the PUND pulse in Fig. 1(d) depicts a closed $P$–$V$ hysteresis loop, even at a high peak voltage of 2.0 V, because the gate oxide leakage and trap charge were equal in the first and second pulses during the leakage correction of the PUND pulse. For the data shown in Fig. 4(a) and (b), similar 2$Pr$ values were observed at 0 V in the hysteresis curves, as shown in Fig. 1(d), owing to the zero DE charge, as discussed in Fig. 1(d). In addition, for the HfO$_2$ thin film in Fig. 4(a) and (b), the triangular pulse and PUND pulse were both approximately 1 $\mu$C/cm$^2$ of 2$P_r$ in the case of peak voltage > 1.5 V, which was potentially caused by the slight inclusion of the orthorhombic phase (O-phase) in pure HfO$_2$ [15]. Furthermore, the 2$P_r$ values of HZO increased with the peak voltage for film thicknesses of both 4 and 5 nm. In addition, the 2$P_r$ value of 4-nm-thick HZO was higher than that of the 5-nm-thick HZO. Generally, the trap charges in the low-frequency CP measurement increase with HfO$_2$ thickness owing to the bulk trap effect [24], [25]. Therefore, the higher charges of 4-nm-thick HZO over 5-nm-thick HZO did not originate from the bulk trap and presumably; this difference was caused by the higher in-film O-phase portion in the 4-nm film [1]. The O-phase portion of HZO depends on the thickness, Zr concentration, upper electrode, PMA, and so on. In the current HZO films with 20% Zr, the 2$P_r$ value was higher for the 4-nm-thick film, presumably because of the higher O-phase ratio relative to the 5-nm-thick film [11], [14], [16].

To compare the conventional $P$–$V$ measurement method with the CP, the pattern of the CP voltage pulse must be adjusted, as depicted in Fig. 5, because, typically, the CP employs $V_{base}$ approximate to the flat band voltage. The applied CP voltage pulse with the base voltage maintained proximity to the flat band voltage is illustrated in Fig. 5(a), wherein $V_{base}$ is $-1.0$ V (SPGU-1) represents a typical pulse form of the CP for $D_A$ measurement in MOSFETs. Upon maintaining the base voltage proximate to the flat band voltage and raising the pulse peak height, the CP current ($I_{CP}$) was measured after the peak voltage attained the threshold voltage.

In addition, the $I_{CP}$ saturated when the peak voltage surpassed the threshold voltage. The variations in the pulse voltage of the CP from a trapezoidal pulse to a triangular pulse (SPGU-2) are plotted in Fig. 5(b). The variations in the duty cycle of the pulse from 0.5 to 1.0 (SPGU-3) are displayed in Fig. 5(c). However, the application of a higher $|V_{base}|$, such as $-2.0$ V, was impossible because the gate oxide breaks down before reaching this voltage. In the CP measurements, $V_{base}$ was applied to the gate oxide for the majority of the period, except during the pulse application. Therefore, as the value of $V_{base}$ increased, the gate oxide was damaged by a relatively long applied period of the $V_{base}$. This is the reason for setting the base level voltage of CP at 0 V and increasing the peak voltage in both directions, as portrayed in Fig. 5(d) (SPGU-4). Consequently, the pulse displayed in Fig. 5(d) corresponded to the same waveform as the conventional $P$–$V$ hysteresis measurement method in Fig. 1(b).

The numbers of charges measured by these four voltage pulse waveforms for the 4.2-nm HfO$_2$ and 4-nm HZO samples based on (4) are depicted in Fig. 6(a) and (b), respectively. The variations in the number of charges measured from SPGU-1 to SPGU-4 converge to the same trend in the case of both HfO$_2$ and HZO. The numbers of charges by SPGU-1 were higher than that of other waveforms in both HfO$_2$ and HZO because SPG-1 measured fewer bulk traps using the trapezoidal waveform [18]. Compared to other waveforms, SPGU-4 exhibited a larger takeoff voltage, which can be attributed to the variations in $V_{base}$, because, for $V_{base}$ being 0 V, the charges were measured as $V_{peak}$ attained the threshold voltage, but, for $V_{base}$ being 0 V, the charges were measured only in case the $V_{peak}$ voltage acquired the flat band voltage and the threshold together. Moreover, this can be validated by the flat band voltage and the
threshold voltage displayed in the C–V curve [see Fig. 2(a)]. As displayed in Fig. 6(a) and (b), the pulses of SPGU-2, SPGU-3, and SPGU-4 portray the results of measuring the same number of traps at $V_{\text{peak}}$ of 1.0 V, where the peak–peak voltage was the same. Therefore, the application of the CP pulse in the manner presented in Fig. 5(d) can increase $V_{\text{peak}}$ while avoiding the breakdown of the gate oxide. Notably, the pulse shape in Fig. 5(d) for SPGU-4 was the same as that of the conventional triangular pulse used in the measurement presented in Figs. 1(b) and 4(a). Thus, these two results can be reasonably compared.

In Fig. 7(a), the $2P_r$ values measured by the conventional pulse [see Fig. 4(a) and (b)] are compared to the charges measured by CP in the linear scale [see Fig. 5(d)], which indicated the extremely small variations in $2P_r$ between the two methods for HfO$_2$ and HZO thin films at $V_{\text{peak}} \geq 2.0$ V, and these variations were within the standard chip-to-chip variations. For 4-nm thick HZO, at $V_{\text{peak}} < 2.0$ V, the difference between the values measured using the two methods became larger, which was caused by the noise current level measured using the conventional pulse method. In this experiment, the transistor active area was 800 $\mu$m$^2$ for both methods. However, as portrayed in Fig. 7(b) and (c), the currents measured during the application of the voltage to the gate electrode varied in the two methods. The current measured in case a pulse is applied using the conventional method (PUND pulse) according to $V_{\text{peak}}$ is presented in Fig. 7(b). The switching charge was extracted using (1), (7), and (8), which utilized the current variations between P and U, as well as that between N and D pulses. In this experiment, $t_r/t_f$ of the pulse used in this experiment was 5 $\mu$s, and the current measurement resolution of WGFMU was $1-10$ $\mu$A [19]. In Fig. 7(b), the current noise dominated for $V_{\text{peak}} \leq 1.8$ V, specifically, in the region D, so the $2P_r$ value extracted in this case is substantially affected by the current noise. To reduce the noise effect, the measured current magnitude must be increased, and to this end, the active area of the device should be increased, or $t_r/t_f$ should be reduced according to (7) and (8). However, in most cases, the area of the actual device was less than 1 $\mu$m$^2$, and it is disadvantageous owing to the strengthening influence of the series resistance as $t_r/t_f$ decreases. The current measured during the application of the voltage using the CP method is displayed in Fig. 7(c), which indicates that the measured current level was approximately one order less than that displayed in Fig. 7(b), and it could be clearly measured without noise even at a lower $V_{\text{peak}}$ because the current resolution of SMU was higher than that of the WGFMU. The SMU current resolution in the data sheet was 10 fA, whereas the resolution in the present experiment was 10 pA [low current limit indicated in Fig. 6(a) and (b)], probably because of chuck and cable noise [20].

\[
i = \frac{dQ}{dt} \quad (7)
\]

\[
N_{\text{conv}} = \frac{\int i \, dt}{qA} \quad (8)
\]

\[
N_{\text{CP}} = \frac{I_{\text{CP}} \ast t}{qA} \quad (9)
\]
where $N_{\text{conv}}$ and $N_{\text{CP}}$ denote the number of charges measured using the conventional method and the CP method, respectively.

As displayed in Fig. 7(b), at a low $V_{\text{peak}}$, the current measured using the conventional $P-V$ method is extremely sensitive to the noises pertaining to low current limits. In this experiment, the conventional method apparently required $V_{\text{peak}}$ of at least 2.0 V to sufficiently reduce the noise caused by the low current resolution of the measuring components. On the contrary, the CP measurement detected the recombination current of electrons and holes for the given dc current in the SMU with superior high current resolution. Therefore, the CP method can stably measure better than conventional $P-V$ measurements. In addition, the trends of both 5-nm-thick HZO and 4-nm-thick HZO were similar, as portrayed in Fig. 7(a). In the case of HfO$_2$, both methods increased by $2Pr$ at $V_{\text{peak}} \sim 1.5$ V, potentially because the polarization started at this voltage. Moreover, the HfO$_2$ acted as a DE at low $V_{\text{peak}}$, but it displayed inferior ferroelectricity at high $V_{\text{peak}}$. Based on the stated results, the CP method can measure the lower switching current more accurately than the conventional $P-V$ measurement method.

### C. Origin of Polarization Charge and Discussion

Subsequently, we investigated the origin of the current measured by CP and conventional methods. The number of charges obtained from $I_{\text{CP}}$ and $I_{\text{SD}}$ using (9) is presented in Fig. 8(a). These current components were simultaneously measured during the CP measurements, $I_{\text{CP}}$ denotes the current measured at the well terminal, and $I_{\text{SD}}$ represents the current measured at the tied S/D terminal. According to the CP measurement mechanism, $I_{\text{CP}}$ denotes the hole current supplied by the well when the holes recombine with the electrons trapped in the interface, and $I_{\text{SD}}$ represents the electron current supplied by S/D at the instant electrons recombined with the holes trapped at the interface [17]. Thereafter, $I_{\text{CP}}$ and $I_{\text{SD}}$ in the 4-nm-thick HZO sample with FE characteristics were identical, as displayed in Fig. 8(a). As the interface trap density of a well-controlled MOSFET does not exceed $5 \times 10^{12}$ cm$^{-2}$·eV$^{-1}$, the measured charge can be estimated using the components other than the additionally included interface traps [22], [23]. The calculated numbers of gate charges ($N_{\text{gate}}$), S/D charges ($N_{\text{SD}}$), and well charges ($N_{\text{well}}$) from the current components measured under the conventional triangular pulse are illustrated in Fig. 8(b), wherein $N_{\text{gate}}$ was extracted from the current after removing the parasitic components. As the charges measured at the gate terminal were equal to the sum of the S/D and well charges, which is consistent with the results reported by Toprasetpong et al. [10], it is suggested that the origin of the $N_{\text{SD}}$ measured during the application of a voltage pulse to the gate involves charges caused by the response of the S/D electrons, and the origin of the $N_{\text{well}}$ involves charges caused by the response of well holes. Therefore, $N_{\text{CP}}$ and $N_{\text{SD}}$ [see Fig. 8(a)] originated from the same source as $I_{\text{CP}}$ and $I_{\text{SD}}$ [see Fig. 8(b)]. As the gate oxide is composed of a FE material, the CP and conventional $P-V$ measurements record the switching polarization charge of the ferroelectricity in the same manner.

In Fig. 8(a), the number of charges decreased as $t_r/t_f$ decreased from 5 $\mu$s to 100 ns. According to the CP model expressed in (6), as $t_r/t_f$ decreased, the measured interface trap charges must increase because electron/hole emission in the Si bandgap decreases with $t_r/t_f$, which increases the electron/hole recombination and the interface traps, as portrayed in Fig. 3. Surprisingly, the number of measured charges decreased as $t_r/t_f$ decreased from 5 $\mu$s to 100 ns [see Fig. 8(a)], which further implies that the measured charges do not originate from the interface trap. The reduction in the number of charges can be attributed to the fewer FE switching charges at $t_r/t_f$ of 100 ns. According to Fig. 3, the number of charges measured in the $t_r/t_f$ range of 50–400 ns did not vary significantly. However, the number of charges measured at $t_r/t_f$ of 5 $\mu$s increased significantly owing to the presence of several FE switching charges, as observed in Fig. 8(a). This implied that the switching dynamics of FE dipoles are nonlinearly proportional to the switching time, which is consistent with the results of Liu et al. [21]. In this experiment, distinct results were obtained even at $t_r/t_f$ of 50 ns using the CP method. Therefore, this proposed method can aid the study of FE switching dynamics in the range of tens of nanoseconds to tens of microseconds.
Current components measured during CP in the FeFET are modeled in Fig. 9(a) and (b). As depicted in Fig. 9(a), the ferroelectricity is polarized in the downward direction during the inversion state of the FeFET. Thus, surface-induced electron charges owing to FE polarizing dipoles and trapped charges caused by interface traps exist simultaneously with the inversion electrons in the channel. As observed from Fig. 9(b), the electrons in the inversion region are transported to the S/D in case the gate voltage varied from the inversion state to the accumulation state. However, the electrons set by the FE polarized dipole and the interface trap could not move to the S/D. Thereafter, these FE-induced and interface electrons recombined with the hole supplied from the well terminal. A similar scenario occurs when the FeFET operation is changed from accumulation to inversion. Thus, the hole current supplied from the well and the electron current supplied from the S/D were proportional to the number of interface traps and dipoles of ferroelectricity, i.e., the current measured by the CP included both charges resulting from the interface traps and the charges caused by the polarization of ferroelectricity. In the 4-nm-thick HZO sample [see Fig. 7(a)], the 2Pr value at Vpeak of 2.4 V was 13 μC/cm², and the corresponding number of charges was 8.2 × 10¹³ cm⁻², as calculated in Fig. 9(c). Therefore, the charges measured by CP in the HZO samples with 5- and 4-nm-thick films could be attributed to the polarization of the ferroelectricity.

The typical Pr measurement method and the proposed CP method are presented in Table I, wherein the major difference between the two methods was the tool used for the current reading. The conventional method used a PG to apply voltage pulses to the gate terminal and measured the current using an OSC. The charges were obtained by integrating this current over time as in (1). Although the pulse was applied in the CP method following the same approach, the time-independent dc was measured using an SMU during the current reading, which was converted into charges using (4). Therefore, the stable current was measured at a lower peak voltage because reading the dc is more reliable with the SMU, as it offers a higher resolution than the OSC. An additional advantage of the CP method is that Pr can be measured with a small device area. In general, the switching characteristics of the FE dipoles vary with the device area because the switching characteristics are determined by the size and distribution of grains [14]. Therefore, the characteristics of FE switching ought to be clarified in a small device area. In the case of using the CP method proposed in this article, Pr of the device with an active area ≤1 μm² can be directly measured. The CP current measured at the area of 800 μm² and Vpeak of 2.4V in Fig. 7(c) was ~1 × 10⁻⁵ A, whereas 2Pr was approximately 13 μC/cm². If measured in a 1-μm² area, the current measured using (9) will be ~1.2 × 10⁻⁸ A, and thus, the area of 1 μm² can be adequately measured using this method as it offers a higher current resolution than the present SMU (100 pA). Moreover, an area of up to 100 nm × 100 nm can be measured by reducing the chuck leakage and increasing the measurement frequency.

Eventually, the possibility of NCFET measurement arises in the case of capacitance boosting. According to Hoffmann et al. [9], if the pulse is applied for ≤500 ns, the gate leakage effect decreases to enable the measurement of the capacitance boosting by ferroelectricity in the FE/DE stack [9]. In principle, the rising/falling time of the pulse in their experiment was 200 ns, so this method can be easily measured under this condition, as depicted in Fig. 3. However, as displayed in Figs. 8 and 9, the current measured using this CP method is basically an immovable charge by the FE dipoles. Therefore, the ideal NC cannot be measured using this method because it must be reversible with the applied voltage and contribute toward the drain current.

### IV. Conclusion

This study proposed a simple and reliable measurement method to analyze the FE properties with hafnium-based gate oxides. Based on a CP measurement, the interface trap charges were measured in an HfO₂ MOSFET, and the interface trap charges and FE switching charges were measured in an HZO FeFET. The CP measurement results of the HZO FeFET exhibited the same results as that of the conventional Pr measurement method. The CP measurement of FeFET switching charges was less vulnerable to noise than the conventional Pr measurement method. Therefore, the polarization could be stably measured at a lower measurement voltage, and the FE switching charge can be measured at a device area of 1 μm² or less with a time of 50 ns or less, facilitated by high current resolution and average current measurement of the SMU. Therefore, the CP method was established as an extremely effective approach to measuring polarization charge for three- or four-terminal devices, such as FeFETs, unless the measurement requires the hysteresis curve in conjunction with the polarization charges.
REFERENCES

[1] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, “Ferroelectricity in hafnium oxide thin films,” Appl. Phys. Lett., vol. 99, no. 10, Sep. 2011, Art. no. 102903, doi: 10.1063/1.3634052.

[2] H. Mulaosmanovic et al., “Evidence of single domain switching in hafnium oxide based FeFETs: Enabler for multi-level FeFET memory cells,” in IEDM Tech. Dig., Dec. 2015, pp. 26.8.1–26.8.4, doi: 10.1109/IEDM.2015.7490777.

[3] K. Florent et al., “Vertical ferroelectric HfO2 FET based on 3-D NAND architecture: Towards dense low-power memory,” in IEDM Tech. Dig., Dec. 2018, pp. 2.5.1–2.5.4, doi: 10.1109/IEDM.2018.8614710.

[4] S. Mueller et al., “From MFM capacitors toward ferroelectric transistors: Endurance and disturb characteristics of HfO2-based FeFET devices,” IEEE Trans. Electron Devices, vol. 60, no. 12, pp. 4199–4205, Dec. 2013, doi: 10.1109/TED.2013.2283465.

[5] Y. D. Lin et al., “3D scalable, wake-up free, and highly reliable FRAM technology with stress-engineered HfZrOx,” in IEDM Tech. Dig., Dec. 2019, pp. 15.3.1–15.3.4, doi: 10.1109/IEDM19573.2019.8993504.

[6] T. Schenk, M. Pesic, S. Slesazeck, U. Schroeder, and T. Mikolajick, “Memory technology—A primer for material scientists,” Rep. Prog. Phys., vol. 83, no. 8, Jun. 2020, Art. no. 086501, doi: 10.1088/1361-6633/ab8886.

[7] S. Fujii, Y. Kamimuta, T. Ino, Y. Nakasaki, R. Takaichi, and M. Saitoh, “First demonstration and performance improvement of ferroelectric HfO2-based resistive switch with low operation current and intrinsic diode property,” in Proc. IEEE VLSI Technol., Jun. 2016, pp. 1–2, doi: 10.1109/VLST.2016.7573413.

[8] S. Salahuddin and S. Datta, “Use of negative capacitance to provide voltage amplification for low power nanoscale devices,” Nano Lett., vol. 8, no. 2, pp. 405–410, 2008, doi: 10.1021/NL071804g.

[9] M. Hoffmann et al., “Unveiling the double-well energy landscape in a ferroelectric layer,” Nature, vol. 565, pp. 464–467, Jan. 2019, doi: 10.1038/s41586-018-0854-z.

[10] K. Toprasertpong et al., “Improved ferroelectric/semiconductor interface properties in HfO2-ZrO2-O2 ferroelectric FETs by low-temperature annealing,” IEEE Electron Device Lett., vol. 41, no. 10, pp. 1588–1591, Oct. 2020, doi: 10.1109/LED.2020.3019265.

[11] Y. T. Tang et al., “A comprehensive study of polymorphic phase distribution of ferroelectric-dielectrics and interfacial layer effects on negative capacitance FETs for sub-5 nm node,” in Proc. IEEE VLSI Technol., Jun. 2018, pp. 45–46, doi: 10.1109/VLST.2018.8510696.

[12] D. K. Schroder, Semiconductor Material and Device Characterization, 3rd ed. Hoboken, NJ, USA: Wiley, 2015, ch. 6, pp. 347–350, doi: 10.1002/0471749095.

[13] R. Meyer, R. Waser, K. Prune, T. Schmitz, and S. Tiedke, “Dynamic leakage current compensation in ferroelectric thin-film capacitor structures,” Appl. Phys. Lett., vol. 86, no. 14, Apr. 2005, Art. no. 142907, doi: 10.1063/1.1897425.

[14] H. J. Kim et al., “Grain size engineering for ferroelectric Hf52Zr48O52 films by an insertion of Al2O3 interlayer,” Appl. Phys. Lett., vol. 105, no. 19, Nov. 2014, Art. no. 192903, doi: 10.1063/1.4902072.

[15] A. Toriumi et al., “Material perspectives of HfO2-based ferroelectric films for device applications,” in IEDM Tech. Dig., Dec. 2019, pp. 15.1.1–15.1.4, doi: 10.1109/IEDM19573.2019.8993464.

[16] S. Shibayama, T. Nishimura, S. Migita, and A. Toriumi, “Thermo-dynamic control of ferroelectric-phase formation in Hf,Zr1−xOx and ZrO2,” J. Appl. Phys., vol. 124, no. 18, Nov. 2018, Art. no. 184101, doi: 10.1103/1.5028181.

[17] G. Groeseneken, H. E. Maes, N. Beltran, and R. F. De Keersmaecker, “A reliable approach to charge-pumping measurements in MOS transistors,” IEEE Trans. Electron Devices, vol. ED-31, no. 1, pp. 42–53, Jan. 1984, doi: 10.1109/T-ED.1984.21472.

[18] M. B. Zahid, R. Degraeve, L. Pantisano, J. F. Zhang, and G. Groeseneken, “Defects generation in SiO2/HfO2 studied with variable tcharge-tdischarge charge pumping (VT2CP),” in Proc. Int. Rel. Phys. Symp., Apr. 2007, pp. 55–60, doi: 10.1109/RELPHY.2007.369868.

[19] Pulse/Waveform Generation With Integrated Measurement Capability, B1500A’s Waveform Generator/First Measurement Unit, Keysight Technol., Santa Rosa, CA, USA, Dec. 2017, p. 7. [Online]. Available: https://www.keysight.com/kkr/ko/assets/7018-02288/technical-overviews/5990-4567.pdf

[20] B1500A Semiconductor Device Analyzer; Data Sheet, Keysight Technol., Santa Rosa, CA, USA, Dec. 2019, p. 11. [Online]. Available: https://www.keysight.com/kkr/ko/assets/7018-01289/data-sheets/5989-2785.pdf

[21] X. Lyu, M. Si, P. R. Shrestha, K. P. Cheung, and P. D. Ye, “First direct measurement of sub-nanosecond polarization switching in ferroelectric hafnium zirconium oxide,” in IEDM Tech. Dig., Dec. 2019, pp. 15.2.1–15.2.4, doi: 10.1109/IEDM19573.2019.8993509.

[22] D. E. H. Nicollian and J. R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology, 1st ed. New York, NY, USA: Murray Hill, pp. 317. [Online]. Available: https://www.wiley.com/en-us/MOS+Metal+Oxide+Semiconductor+Physics+and+Technology-p%3F7980471430707%23description-section

[23] D. G. Borse, S. J. Vaidya, and A. N. Chandorkar, “Study of SILC and interface trap generation due to high field stressing and its operating temperature dependence in 2.2 nm gate dielectrics,” IEEE Trans. Electron Devices, vol. 49, no. 4, pp. 699–701, Apr. 2002, doi: 10.1109/16.992883.

[24] A. Kerber and E. A. Cartier, “Reliability challenges for CMOS technology qualifications with hafnium oxide/titanium nitride gate stacks,” IEEE Trans. Device Mat. Rel., vol. 9, no. 2, pp. 147–164, Jun. 2009, doi: 10.1109/TDMR.2009.2016954.

[25] M. Rafik, G. Ribes, and G. Ghibaudo, “Contributions and limits of charge pumping measurement for addressing trap generation in high-k/SiO2 dielectric stacks,” in Proc. IEEE Int. Rel. Phys. Symp., May 2008, pp. 34.1–34.6, doi: 10.1109/RELPHY.2008.4558909.