Progressive and Stable Synaptic Plasticity with Femtojoule Energy Consumption by the Interface Engineering of a Metal/Ferroelectric/Semiconductor

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In the era of “big data,” the cognitive system of the human brain is being mimicked through hardware implementation of highly accurate neuromorphic computing by progressive weight update in synaptic electronics. Low-energy synaptic operation requires both low reading current and short operation time to be applicable to large-scale neuromorphic computing systems. In this study, an energy-efficient synaptic device is implemented comprising a Ni/Pb(Zr0.52Ti0.48)O3 (PZT)/0.5 wt.% Nb-doped SrTiO3 (Nb:STO) heterojunction with a low reading current of 10 nA and short operation time of 20–100 ns. Ultralow femtojoule operation below 9 fJ at a synaptic event, which is comparable to the energy required for synaptic events in the human brain (10 fJ), is achieved by adjusting the Schottky barrier between the top electrode and ferroelectric film. Moreover, progressive domain switching in ferroelectric PZT successfully induces both low nonlinearity/asymmetry and good stability of the weight update. The synaptic device developed here can facilitate the development of large-scale neuromorphic arrays for artificial neural networks with low energy consumption and high accuracy.

1. Introduction

The hardware implementation of neuromorphic computing requires the emulation of biological synapses whose plasticity provides the physiological substrate for a variety of neuromorphic computing and learning.[1] The energy-efficient and parallel execution of learning and inference in a large crossbar array over 1000 × 1000 synapses are desirable for an ideal neuromorphic system.[1] Further, low energy consumption and high dot-product computing accuracy require a reading current lower than 10 nA during weight updates.[2,3] The energy-efficient storage and processing of massive amounts of information require a short operation time in the range of nanoseconds and low operation voltage.[4–6] Symmetrically/linearly programmable conductance states under voltage training are also necessary for increasing the recognition accuracy in large-scale neuromorphic arrays.[1,7]

Two-terminal memristors have attracted considerable attention in implementing synaptic devices owing to their structural and functional similarity with biological synapses and easy integration with the crossbar array.[5,8] Among the various two-terminal memristors, metal/ferroelectric/semiconductor (MFS) memristors utilizing Nb-doped SrTiO3 as a semiconducting substrate have exhibited high performance in resistive switching behaviors owing to the modulation of the ferroelectric barrier and depletion region in Nb-doped SrTiO3 semiconductors by ferroelectric polarization reversal.[9–15] Progressive polarization reversal of the ferroelectric domain in MFS
can improve the electrical modulation of the band profile between the high resistance state (HRS) and low resistance state (LRS), which can lead to high linearity/symmetry of the synaptic weight update when using a smart programming pulse.\cite{9-13,16} However, parameter enhancement in weight update (linearity, symmetry, and variation) caused by interface engineering between the ferroelectric material and top electrode has not been addressed in MFS memristors reported earlier.\cite{4,8,11,14,15} Moreover, high reading currents of the order of μA during synaptic operation pose a major challenge in implementing energy-efficient large-scale synaptic arrays based on MFS devices, although ultrafast synaptic operation with low energy consumption has been achieved.\cite{2-4,8,11,14,15}

In this study, we fabricated a high-performance single synaptic device based on a Ni/Pb(Zr_{0.52}Ti_{0.48})O_3 (PZT)/0.5 wt.% Nb-doped SrTiO_3 (Nb:STO) MFS structure to develop an energy-efficient and accurate neuromorphic array. Engineering the interface barrier between the top electrode and PZT results in an ultralow reading current below 10 nA and a short operation time in the range of nanoseconds (20–100 ns). This lowers the minimum energy consumption in our device up to a few femtojoules or less at a pulse duration of 20 ns, which is significantly lower than those of biological synapses (10 fJ). In addition, the gradual electrical modulation and high stability owing to a ferroelectric layer in the Ni/PZT/Nb:STO device provide linear (nonlinearity factor of 0.01 for potentiation and 2.9 for depression) and symmetric (asymmetric ratio of 0.18) synaptic plasticity with a low relative standard deviation (0.9% for 300 cycles). Our synaptic device, characterized by femtoujoule energy consumption and high linearity/symmetry, can be considered an essential building block of highly energy-efficient, reliable, and accurate neuromorphic computing systems.

2. Results and Discussion

2.1. Structural and Ferroelectric Characterizations of PZT/Nb:STO

Ferroelectric PZT films were grown on a single-crystal Nb:STO substrate with a TiO_2-terminated step-terrace surface using pulsed laser deposition (see Experimental Section). Nb:STO was selected as the substrate material because of its small lattice mismatch with PZT and excellent conductivity.\cite{17} Figure 1a shows a cross-sectional transmission electron microscopy (TEM) image and schematic diagram of the interface structure of the PZT/Nb:STO heterostructure with a 6 nm-thick PZT layer.

The X-ray diffraction (XRD) data of the Nb:STO substrate and PZT/Nb:STO structure in Figure 1b shows the Bragg peaks for...
both the Nb:STO substrate and PZT film. The XRD pattern shows only PZT (00l) peaks, implying the preferential growth of the PZT film along the c-axis normal to the substrate.

Figure 1c displays the hysteretic behaviors of the out-of-plane piezo-response force microscopy (PFM) phase and amplitude, which are obtained at a specific point on bare PZT surface by sweeping the voltage from 3.0 V to −3.0 V (see Experimental Section). The coercive voltages, at which the phase changes abruptly, are determined as +1 V and −2 V. The ferroelectric behaviors of PZT films were also investigated by patterning ferroelectric domains on them with external voltages, as shown in Figure 1d. The out-of-plane PFM phase and amplitude images obtained after poling are shown in Figure 1e,f, respectively (see Experimental Section). The out-of-plane PFM phase image shows a 180° phase contrast and distinguishable domain boundary between the inversely poled areas. Furthermore, the ferroelectric domains with switchable remnant polarizations possess nearly the same amplitude, which indicates that antiparallel ferroelectric domains can be written in the PZT layer. The PFM images and hysteresis loops confirm the ferroelectric properties of the PZT film grown on the Nb:STO substrate.

2.2. Effect of the Top Electrode on Synaptic Behaviors

To implement large-scale synaptic arrays with high neuromorphic accuracy and low energy consumption, low reading current under 10 nA, and nanosecond-range operation time, even at a small external bias, should be simultaneously obtained by adjusting the barrier height at the metal/ferroelectric interface. Considering the fixed electron affinity of Nb:STO ($\chi_{\text{Nb:STO}} = 3.9$ eV), the Schottky barrier height ($\Phi_B$) in metal/PZT/Nb:STO (Figure S1, Supporting Information) can be controlled by the work function ($\Phi_{\text{metal}}$) of the metal top electrode according to $\Phi_B \sim \Phi_{\text{metal}} - \chi_{\text{Nb:STO}}$ in semiconductor theory because the band bending at the PZT/Nb:STO interface is the function of $\Phi_{\text{metal}}$ and $\chi_{\text{Nb:STO}}$, as shown in Figure 2a. Thus, a suitable top electrode on the PZT film is essential for obtaining the optimum $\Phi_B$ in a metal/PZT/Nb:STO structure.

$\Phi_B$ and the ideality factor ($n$) can be extracted from the equation of thermionic emission theory at a low forward bias:

$$I(V) = S A^* T^2 \exp\left(-\frac{q\Phi_B}{k_B T}\right) \left(\exp\left(-\frac{qV}{n k_B T}\right) - 1\right)$$

where $S$ is the junction area, $A^*$ the Richardson constant, $T$ the temperature, $k_B$ the Boltzmann constant, and $q$ the electron charge. Typical current–voltage ($I$–$V$) sweep data for metal/PZT/Nb:STO with different Cr, Ni, and Pt top electrodes were obtained by applying an external voltage (Figure S2, Supporting Information). The HRS currents at low forward bias
(≤0.5 V) were well fitted by equation (1), suggesting the dominant role of the Schottky barrier in the carrier transport.[19] The junction parameters \( n \) and \( \Phi_b \) of the HRS were estimated from the slope and intercept of the current axis in the \( \ln(I)–V \) curve, respectively. \( n \) (Cr: 6.1, Ni: 3.6, Pt: 1.6) decreases while \( \Phi_b \) (Cr: 0.41 eV, Ni: 0.56 eV, Pt: 0.79 eV) increases with increasing \( \Phi_{metal} \) (Figure 2b).

Figure 2c shows the resistance (R)-pulse voltage (\( V_p \)) loops of the metal/PZT/Nb:STO devices with Cr, Ni, and Pt electrodes, which are obtained using pulses of 10 μs duration. \( R \) was measured at −0.1 V. A low operation voltage is sufficient for flipping the ferroelectric domains in the Cr/PZT/Nb:STO device with small \( \Phi_b \). However, the large \( \Phi_b \) in Pt/PZT/Nb:STO requires a large operation voltage to flip the ferroelectric domains. Because the total external voltage is partially applied to the PZT and Schottky barrier, a larger \( \Phi_b \) decreases the partial voltage applied to the PZT layer.[4] Therefore, a lower operation voltage at a given pulse duration is possible in the device with a smaller \( \Phi_b \), resulting from a smaller \( \Phi_{metal} \), which facilitates lower energy consumption.

A smart programming pulse scheme (64 multi-states with amplitudes from 0.1 V to 6.4 V for potentiation with a step of 0.1 V; 64 multi-states with amplitudes from −0.1 V to −6.4 V with a step of −0.1 V for depression; 10 ms duration and −0.1 V amplitude for read) was used to compare the characteristics of synaptic weight updates depending on the top electrode, as shown in Figure 2d. The maximum reading current (\( I_{reading} \)) and operation time (\( t_d \)) during synaptic modulation in the devices with various top electrodes are shown in Figure 2f. A small \( \Phi_b \) in the Cr/PZT/Nb:STO device enables the flipping of ferroelectric polarization at a short \( t_d \) of 20 ns, which causes gradual synaptic weight update.[4] However, a high \( I_{reading} \) of over 1 μA, caused by its small \( \Phi_b \), may lead to high energy consumption in large-scale synaptic arrays. In contrast, the large \( \Phi_b \) in the Pt/PZT/Nb:STO device considerably reduces \( I_{reading} \) to under 10 nA, while it increases \( t_d \) up to 500 ns which is required for polarization reversal and synaptic weight update.[4] Most importantly, Ni/PZT/Nb:STO with medium \( \Phi_b \) shows a low \( I_{reading} \) under 10 nA and short \( t_d \) of 20 ns. Thus, the problem of high \( I_{reading} \) previously reported in MFS devices can be overcome by our Ni/PZT/Nb:STO device while maintaining a short operation time in the nanosecond range.[8,11,14,15]

### 2.3. Effect of the Ferroelectric Film on Electrical Properties

We assume that carrier transport in metal/PZT/Nb:STO is governed by charge trapping/detrapping, as previously reported for metal/Nb:STO devices, which can be affected by barrier modulation at the PZT/Nb:STO interface by external voltage.[20,26] The electrical characteristics based on charge trapping/detrapping in the Nb:STO substrate can be improved by inserting a ferroelectric film between the metal and Nb:STO substrate. The optimized Ni/PZT/Nb:STO synaptic device was employed to gain insight into the direct impact of the ferroelectric layer on synaptic performance. The basic electrical characteristics of the Ni/PZT/Nb:STO and Ni/Nb:STO devices were measured at room temperature. Bipolar resistive switching curves (counterclockwise) in both devices were repeatedly observed 500 times by sweeping the external voltage between −7.5 V and 2.5 V, while they exhibited different distributions of the HRS resistance, LRS resistance, and set voltage (Figure S3, Supporting Information). The HRS and LRS resistances of the Ni/PZT/Nb:STO device were more uniform than those of the Ni/Nb:STO device. Moreover, the Ni/PZT/Nb:STO device exhibited a narrow distribution of the set voltage (1.9%), which is comparable to those of single-crystalline SiGe epitaxial random access memory (1%) and alloyed memristor for neuromorphic computing (3.3%).[7,27] The improved stability in the Ni/PZT/Nb:STO device is more suitable for the practical implementation of reliable and highly accurate neuromorphic computing systems.[28] Device-to-device variation of set voltage for 50 Ni/PZT/Nb:STO devices was extracted with same voltage sweep, which shows small variation of ≈3% (Figure S4, Supporting Information).

Figure 3a shows the current level (reading at 0.1 V) of the LRS as a function of the DC sweep voltage in the Ni/PZT/Nb:STO and Ni/Nb:STO devices, which are extracted from Figure S5 (Supporting Information). Different \( I–V \) curves were obtained under different DC sweep voltages while maintaining the same reset process. The LRS current was controlled by tuning the DC sweep voltage. In the Ni/PZT/Nb:STO, it increases gradually from 2.5 × 10^−9 A to 3.2 × 10^−5 A as the DC sweep voltage increases from 1.1 to 2.0 V in steps of 0.1 V. However, the LRS current in the Ni/Nb:STO device changes abruptly from 2.4 × 10^−9 A to 5.9 × 10^−4 A as the DC sweep voltage increases from 0.25 to 2.00 V in steps of 0.25 V. The gradual current modulation in the Ni/PZT/Nb:STO device benefits on-chip training that relies on precise synaptic weight updates for rapid convergence.[29] Furthermore, it can also provide a linear behavior of current update by pulse training, which determines the training accuracy in neuromorphic computing.[30]

Figure 3b shows the \( n \) value of the LRS as a function of the DC sweep voltage in Ni/PZT/Nb:STO and Ni/Nb:STO devices. It was estimated from the slope of the linear region of the \( \ln(f_j)–V \) curve by using equation (1), where \( f_j \) represents the forward-bias current density (Figure S6, Supporting Information). The \( n \) of the LRS increases with the amplitude of the DC sweep voltage in both devices. The \( n \) of LRS in the Ni/PZT/Nb:STO device increases gradually from 2.55 to 3.96 with increasing DC sweep voltage from 1.1 to 2.0 V in steps of 0.1 V. However, the \( n \) of LRS in the Ni/Nb:STO device changes more abruptly from 2.02 to 4.49 with increasing DC sweep voltage from 0.25 to 2.00 V in steps of 0.25 V.

In an MFS junction, the interfacial ferroelectric layer has a capacitance \( C_f \) and it can partition the applied voltage \( V \) with \( V = V(n − 1)/n \). Consequently, the voltage drop across the depletion region is thus reduced to \( V_d = V/n \). Here, \( n \) can be expressed as[19,20]:

\[
n = 1 + \frac{C_d}{C_i} = 1 + \frac{d}{W_d} \cdot \frac{\varepsilon_i}{\varepsilon_f}
\]

where \( C_d \) and \( C_i \) are the high-frequency capacitances of the depletion region in the semiconductor and the insulator layer, respectively, \( \varepsilon_f \) and \( \varepsilon_i \) are their respective relative dielectric constants, \( W_d \) is the depletion region width, and \( d \) is the thickness of the insulator. Here, \( \varepsilon_f \) of Nb:STO was estimated to be 290 at room temperature.[19,31] An inversely proportional relationship
Figure 3. Gradual resistive switching based on progressive ferroelectric domain switching in Ni/PZT/Nb:STO. a–c) Current value (a), ideality factor (n) (b), built-in potential ($V_{bi}$), and depletion region width ($W_d$) (c) of LRSs obtained by applying DC sweep voltages with different amplitudes to the Ni/PZT/Nb:STO and Ni/PZT/Nb:STO devices while maintaining the identical reset process. d) PFM phase images and domain distributions of various regions (A, B, C, and D) on PZT/Nb:STO, which are acquired after applying different positive DC voltages (0.5, 1.0, 2.0, and 3.0 V), respectively. e) Evolution of downward domain (bright color) as a function of the number of pulses with amplitude and duration of +7 V and 100 ns, respectively, which are applied at a fixed tip. f–i) Band profiles of Ni/PZT/Nb:STO devices at HRS (f) and LRSs obtained by applying different positive voltages (g–i). The black arrow and red circle denote the polarization direction and electron captured at the trap site, respectively.

between $n$ and $W_d$ indicates a gradual increase in $n$ caused by a gradual decrease in $W_d$, for a fixed thickness of the insulator layer. $W_d$ was determined experimentally using the built-in potential ($V_{bi}$) value estimated from the $C_d^{-2}$–$V_d$ curve (Figure S7, Supporting Information). The values of $V_{bi}$ and $W_d$, which depend on the DC sweep voltage, are presented in Figure 3c. The $V_{bi}$ and $W_d$ of the Ni/PZT/Nb:STO device decrease from 5.18 to 2.77 V and from 76 to 44 nm, respectively, when the DC sweep voltage increases from 1.1 to 2.0 V in steps of 0.1 V. In the Ni/Nb:STO device, $V_{bi}$ and $W_d$ decrease from 2.78 to 1.70 V and from 46 to 24 nm, respectively, when the DC sweep voltage increases from 0.25 to 2.00 V in steps of 0.25 V. The data in Figure 3a–c suggest...
that the gradual control of the current in the Ni/PZT/Nb:STO device is correlated with the progressive control of $n$, $V_{hi}$, and $W_d$, owing to the gradual change in the ferroelectric domain configuration and the resultant charge trapping/detrapping. However, the Ni/Nb:STO shows abrupt changes in $n$, $V_{hi}$, and $W_d$ due to abrupt charge trapping/detrapping, which is induced by only external voltage without ferroelectric bound charges of PZT.

The PFM data in Figure 3d,e confirms the progressive modulation of the ferroelectric domain configuration by external bias. In Figure 3d, we first scanned a $6 \times 6 \, \mu m^2$ area with a DC bias of $-10.5 \, V$ applied to the cantilever tip to orient the polarization in the upward direction. Then, we reversed the polarization direction by applying DC bias of 0.5, 1.0, 2.0, and 3.0 $V$ to each $4 \times 1 \, \mu m^2$ area of A, B, C, and D, respectively (see Experimental Section). Figure 3d also reveals the distribution of the downward domain after scanning. The number of pixels with downward domains increases with applied voltage. The percentages of downward domains for A, B, C, and D are 14.6%, 58.3%, 85.5%, and 94.3%, respectively.

Because synaptic weight was generally updated using a pulsed signal, we monitored the evolution of the out-of-plane PFM phase image by applying voltage pulses with a duration of 100 $ns$ (Figure 3e).[4,32] We first scanned the $1 \times 1 \, \mu m^2$ area on the PZT film by applying a DC bias of $-9.0 \, V$ to the tip to create an upward ferroelectric domain. Then, we applied several positive pulses, whose amplitude and duration were 7.0 $V$ and 100 $ns$, respectively, to a fixed tip on the PZT film to partially change the domain distribution. The percentage of the downward domain in the $1 \times 1 \, \mu m^2$ area gradually increases with the number of pulses: 1.1%, 4.3%, 8.6%, 26.3%, and 41.1% for 70, 90, 110, 130, and 150 pulses, respectively. The evolution of the domain configuration in Figure 3d,e confirms the progressive reversal of the polarization from upward to downward, depending on the amplitude of the DC bias and number of voltage pulses.

Figure 3f–i shows the band profiles of the metal/PZT/Nb:STO device for HRS and LRS, which are determined by different ferroelectric domain distributions. When a large reverse (negative) bias is applied to the top electrode (Figure 3f), the negative bound charge in the PZT (upward polarization) increases the barrier at the PZT/Nb:STO interface. Electrons can be captured by the empty positively charged trap sites at the PZT/Nb:STO interface under reverse bias.[31] The trapped charges increase both $V_{hi}$ and $W_d$ in Nb:STO, leading to HRS.[29] After eliminating external bias, the trap sites can remain occupied owing to the large interface barrier caused by the upward remnant polarization in PZT. When a forward (positive) bias is applied to the top electrode (Figure 3g–i), the positive bound charge in PZT lowers the barrier at the PZT/Nb:STO interface. Trapped electrons are discharged from the trap states under forward bias.[31] The detrapped states decrease both $V_{hi}$ and $W_d$ in Nb:STO, leading to LRS. Consequently, the gradual change in the distribution of trapped/detrapped states, which are induced by the domain evolution of ferroelectric remnant polarization, can progressively modulate the band profile, as shown in Figure 3f–i. The gradual multi-domain configurations in a ferroelectric layer are expected to gradually change the band profiles at the PZT/Nb:STO interface and then induce more gradual multi-level current than the device without PZT.

2.4. Effect of the Ferroelectric Film on Synaptic Performance

Synaptic devices with high linearity/symmetry are suitable for high-accuracy neuromorphic computing systems and can constitute a transistor-less memristor array with high scalability and stackability.[6,34] The linearity/symmetry of weight updates for high-performance synaptic devices can be improved by applying a smart programming scheme.[16] As shown in Figure 4a, our smart programming scheme was applied to the Ni/PZT/Nb:STO device and Ni/Nb:STO. During 18 potentiation-depression cycles, the Ni/PZT/Nb:STO device shows more linear/symmetric and stable analog weight updates than the Ni/Nb:STO device. We obtained temporal statistics of the nonlinearity factor and asymmetric ratio (AR) for 18 cycles for a more quantitative analysis (see Experimental Section and Figure S8, Supporting Information). The potentiation and depression curves were simulated using NeuroSim to determine the nonlinearity factor.[35] Further, the relative standard deviation (RSD) in cyclic endurance tests, which is the ratio of the standard deviation ($\sigma$) to the mean ($\mu$), was also estimated owing to the negative impact of device variability on the training and recognition process.[16] Figure 4b shows that the average value and RSD for the nonlinearity factor of the Ni/PZT/Nb:STO device are 0.01 and $\sigma/\mu_p = 0\%$ for potentiation and 2.90 and $\sigma/\mu_d = 0\%$ for depression, respectively, whereas those of the Ni/Nb:STO device are 4.80 and $\sigma/\mu_p = 17\%$ for potentiation and 7.06 and $\sigma/\mu_d = 9\%$ for depression, respectively. The average value and RSD for AR of the Ni/PZT/Nb:STO device are 0.18 and $\sigma/\mu = 0.83\%$, whereas those of the Ni/Nb:STO device are 0.82 and $\sigma/\mu = 3.6\%$, respectively, as shown in Figure 4c. The linear and symmetric analog update with the incremental pulse scheme in the Ni/PZT/Nb:STO device is considered to originate from the multi-domain response of PZT, where individual ferroelectric domains possess different coercive voltages and react differently by train of pulses.[32,34]

High endurance is an important criterion for reliable crossbar arrays in neuromorphic computing.[28] In particular, the endurance of conductance tuning is an important concern for high accuracy in situ training in array-level implementation.[9,10,37] In situ learning requires a network to continuously adapt and update its knowledge as more training data become available, which significantly improves accuracy.[10] Figure 4d shows that the Ni/PZT/Nb:STO device retains similar potentiation/depression behaviors during 300 cycles (38 400 pulse trainings) with a pulse duration of 100 $ns$. This indicates good endurance without drastic changes in conductance states. Figure 4e shows the average RSD for each conductance state of potentiation/depression during 300 cycles (Figure 4d) and the weight update cycle-to-cycle variation (CCV) for the last cycle in our Ni/PZT/Nb:STO device (Figure S9, Supporting Information). CCV is distinct from RSD and is the variation in conductance change at every programming pulse, which influences the number of multi-states and nonlinearity.[35,38] The CCV of synaptic modulation was studied using the NeuroSim simulator in our device.[35] Our Ni/PZT/Nb:STO device displays an ultralow average RSD of 0.9% for 300 cycles. Recently, Pt/SnS/Pt and carrageenan/Ag nanocomposite devices showed small RSDs of 6.27% and 2.41% for 100 cycles, respectively, during smart programming.[36,39] An ultralow weight update CCV (<0.5%) in our Ni/PZT/Nb:STO...
Figure 4. Linear and symmetric synaptic plasticity of Ni/PZT/Nb:STO a) Analog synaptic behaviors (18 potentiation/depression cycles) obtained using a smart programming scheme, with a pulse duration of 100 ns and 64 multi-states, for Ni/PZT/Nb:STO and Ni/Nb:STO devices. b,c) Distribution of the nonlinearity factor of potentiation ($\alpha_p$) (b) and asymmetric ratio (AR) (c) for Ni/PZT/Nb:STO and Ni/Nb:STO devices. The inset of (b) shows the distribution of nonlinearity factor of depression ($\alpha_d$). d) Potentiation/depression behaviors of the Ni/PZT/Nb:STO during 300 cycles (38400 pulses) under smart programming with 100 ns duration. The inset shows the potentiation/depression curves during the 50, 150, and 250th cycles. e) Relative standard deviation (RSD) of current values for the 300 cycles and CCV for the last cycle.

Our Ni/PZT/Nb:STO device satisfies the targeted value of CCV (<2%) for high learning accuracy. Thus, the small RSD and CCV values imply the good stability of the synaptic behaviors of the Ni/PZT/Nb:STO device, which has the potential for reliable large-scale synaptic arrays in neuromorphic computing.[40] Analog synaptic behaviors obtained using an identical programming scheme are also measured for Ni/PZT/Nb:STO and Ni/Nb:STO devices, which also shows more enhanced properties of nonlinearity factor and RSD in Ni/PZT/Nb:STO device (Figure S10, Supporting Information). In addition, we measured the I–t curves for confirming the long-term memory properties of multi-states, which are obtained by pulse train with varying the pulse number in Ni/PZT/Nb:STO device (Figure S11, Supporting Information).

In biological systems, the energy consumption per synaptic event is $\approx 10$ fJ on average.[5] Therefore, electronic synapses with low energy consumption ($E = V_{write} \times I_{write} \times t$) similar to that of biological operation are required for brain-like neuromorphic computing.[41] Repeated smart programming schemes over $3 \times 10^7$ pulses with a duration of 20 ns were applied to the Ni/PZT/Nb:STO device, as shown in Figure 5a. We achieved an extremely low energy consumption of below 9 fJ/bit for operation during the stimulations and good endurance over $3 \times 10^7$ pulses. Our Ni/PZT/Nb:STO device exhibits an ultra-low energy consumption below 9 fJ during weight updates, which is lower than that of biological synapses (<10 fJ) because of the 20 ns pulse duration and low reading current under 10 nA (Figure S12, Supporting Information). Figure 5b displays the statistical results of the energy consumption in two-terminal synaptic devices modulated by ferroelectric domain switching over the last five years.[8,15,42–47] Notably, our Ni/PZT/Nb:STO device consumes the lowest energy during synaptic weight update among all the ferroelectric-based two-terminal synaptic devices. An appropriate top electrode is critical for reducing the operation time and reading current simultaneously, which are essential for low-energy synaptic operation. The ultralow energy consumption (on the order of fJ) with high endurance in our Ni/PZT/Nb:STO device can extend neuromorphic computing to low-power environments such as edge computing (e.g., mobile and wearable devices) or support adaptive neural networking.[2]

3. Conclusion

In conclusion, we implemented progressive and stable synaptic plasticity with femt joule energy consumption in a synaptic device based on a MFS structure. Interface engineering between metals and ferroelectrics reduced the operation time and reading current required for ultralow energy consumption during synaptic weight updates. Ferroelectric thin films with multi-domain configurations can enable progressive and stable changes in the distribution of trapped/detrapped states, which ensures linear/symmetric synaptic weight updates with small variability. Therefore, our Ni/PZT/Nb:STO device is a potential building block for reliable large-scale synaptic arrays for high-accuracy neuromorphic computing systems.
Figure 5. Femt joule energy consumption with high endurance in Ni/PZT/Nb:STO. a) Demonstration of stable synaptic weight update with ultralow energy consumption below 9 fJ during over 3 × 10^9 pulses. b) Statistical results of the reported two-terminal synaptic memristors based on ferroelectric domain reversal in the recent five years. [8,15,42–47]

4. Experimental Section

Device Fabrication: PZT films with a thickness of 6 nm were epitaxially grown on (001) single-crystalline Nb:STO substrates (Figure S13, Supporting Information) by pulsed laser deposition using a KrF excimer laser (Coherent, COMPexPro 205F). Before deposition, the Nb:STO substrates were etched by NH4F buffered-HF solution and annealed at 1000 °C for 1 h in air to form a TiO2-terminated step-terrace surface. The PZT films were deposited by using a laser energy density of 0.69 J cm\(^{-2}\) at a repetition rate of 1 Hz, maintaining the substrate temperature and O2 pressure at 550 °C and 200 mTorr, respectively. Au/Cr (thickness of 25/30 nm), Au/Ni (thickness of 25/30 nm), and Pt (thickness of 50 nm) top electrodes with 20 × 20 μm\(^2\) in size were deposited and patterned on the surfaces of PZT/Nb:STO heterostructures by using e-beam evaporation and lift-off processes.

Structural Characteristics: Cross-sectional TEM images were obtained using a 300 kV field-emission TEM (TecnaII G2 F30 super-twin). The thicknesses of the films were calibrated and their structural characteristics were measured using TEM images.

Ferroelectric Characterization: PFM images of the PZT/Nb:STO heterostructure were obtained using a Pt/Ir-coated tip as the top electrode in a commercial atomic force microscope (Park systems, XE-100). The local hysteresis loops and ferroelectric domain evolution were measured using a diamond-coated conductive tip. A lock-in amplifier (Stanford Research Systems, SR830) was used to apply an AC bias (f = 17 kHz) with an amplitude of 1.0 V (peak to peak) in the PFM mode.

Electrical Measurements: The I–V characteristics in DC mode and gradual current modulation in pulse mode were measured using a probe station equipped with a semiconductor characterization system (Keithley, 4200-SCS). The shortest pulse generated by the ultrafast module had a duration of 20 ns. The C–V characteristics were measured using an impedance analyzer (Agilent, 4294A) at room temperature with a frequency of 1 MHz and an oscillation level of 50 mV. All electrical measurements were performed at room temperature in air with 2 μm W probes (MS TECH, M1.5BT).

Analysis of Analog Weight Updates: To analyze the impact of nonlinear weight updates on learning, the conductance change of potentiation (G\(_P\)) and depression (G\(_D\)) with the number of pulses (P) were described by the following equations:

\[ G_P = B \left( 1 - e^{\left( \frac{P}{P_{max}} \right)} \right) + G_{min} \]  \hspace{1cm} (3)

\[ G_D = -B \left( 1 - e^{\left( \frac{P}{P_{max}} \right)} \right) + G_{max} \] \hspace{1cm} (4)

where G\(_{max}\), G\(_{min}\), and P\(_{max}\), which are directly extracted from the experimental data, represent the maximum conductance, minimum conductance, and maximum number of pulses required to switch the device between the minimum and maximum conductance states, respectively. [49] The parameter A controls the nonlinear behavior of the weight update, while B is simply a function of A that fits the functions within the range of G\(_{max}\), G\(_{min}\), and P\(_{max}\). A and B may be different in Equations (3) and (4).

Asymmetry indicates the degree of difference in the change of a certain conductance level between the potentiation and depression stages. [28] It is also an important factor in high-accuracy neuromorphic computing. The asymmetric ratio (AR) is defined as

\[ AR = \frac{\max|G_P(n) - G_D(n_{max} - n)|}{G_P(n_{max}) - G_D(n_{max})} \] \hspace{1cm} (5)

where G\(_P(n_{max})\) and G\(_D(n_{max})\) are the channel conductance values obtained after applying the last potentiation and depression pulses, respectively, while G\(_P(n)\) and G\(_D(n_{max} - n)\) are the channel conductance values obtained after applying the n-th potentiation and (n\(_{max}\) - n)-th depression pulses, respectively. For the ideal symmetric case, AR is zero. [49]

Supporting Information: The device conductance was calculated by the equation: G = I/V. The Origin software was used for data processing and analysis. Data variation such as CCV, RSD, and set voltage distribution was performed by Origin software and Excel software for the data processing and analysis.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.
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Conflict of Interest
The authors declare no conflict of interest.

Data Availability Statement
The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords
energy efficiency, linearity, low reading current, short operation time, symmetry

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