Analyzing the performance of Cascaded H-Bridge Multilevel Inverter with three phase multiwinding transformer and single phase supply

P.Kathirvel¹, V.Karpagam², K.Vijayakumar³, A.Venkatesh⁴
¹,⁴ Assistant Professor, Department of EIE, Dr.Mahalingam College of Engineering & Technology, Pollachi, Tamilnadu.
² Assistant Professor(SS), Department of EIE, Dr.Mahalingam College of Engineering & Technology, Pollachi, Tamilnadu.
³ Associate Professor, Department of EIE, Dr.Mahalingam College of Engineering & Technology, Pollachi, Tamilnadu.
*Email: kathir178@drmcet.ac.in

Abstract. A multi-level inverter type cascaded H-bridge design with a different harmonic reduction technique is provided. The proposed design includes the DC source, hybrid cascaded multilevel inverter, transformer and load circuit. For a hybrid, multi-level inverter, the 7-level stepped form of the wave is achieved similar to the sinus wave. The transformer supplies the seven-tier hybrid inverter with cascading into the load. The 5th and 7th harmonics were efficiently extracted with the algorithm from the line current. The simulation and research was carried out to show how the system proposed works. The observed harmonic detail results, the THD are approximately 12.27% only. The 3rd level harmonics magnitude is 5.2% and 5th level harmonics is only 8.2%. Simulation results from SIMULINK/MATLAB software and hardware experimental results are tabulated. The results are explained with graphically.

Index Terms - Multilevel inverter, Single phase DC link, Total Harmonic distortion (THD), Flying capacitors, Linear load.

1. Introduction
A broad rule has been developed in several applications for the multilevel converter. This multi-grade converter can be used on both sides of energy supply, as an electrical connection between wind, solar power, biomaterial, waste & bagasse, high power photovoltaic modules. Cascaded H-Bridge multi-level inverter is one of the commonest multi-level topologies. In both 1 and 3 stages, the transformation is probable. You are using the H-Bridge button and diode. A multi-level inverter needs at least three voltage levels. The converters are supplied with a number of voltage sources for switches and condensers. The unit produces steady output voltages with fewer harmonic fluctuations when the MOSFET switch is triggered and deactivated. Multi-level inverters are used as one of the latest power converter zones in production plant and public electricity boards because the disadvantages of standard pulse width modulators [6] can be managed [11]. Three different H-bridge cell types, such as diode clamped or floating condensers, with a separate dc source can be described [7].
1.1 Inverter Type Clamped Diode
The diode-clamped inverter is used for the diodes and supplies condensers in series connected by several voltage levels through different phase values. Send diodes to lower the load on other power supplies with the set voltage frequency. The input DC’s average stress is 50%. The switches, diodes and circuit condensers solve this problem. The dc-Link tension of the condenser terminals is regulated on three levels because of condenser safety problems [1, 8].

1.2 Flying type Capacitor Inverter
A number of condenser-connected switching diodes exist. The condensers relay the small voltage to the water. The conditions are similar to those of the diode-clamped inverter. In this type of multi-level inverter, clamping diodes are not required. The voltage is half the voltage of the DC signal.

1.3 H-Bridge Cascaded Cells with different DC Sources
Each H-Bridge module includes a separate dc-link voltage [1, 7] and a new multicolored H-bridge cascade inverter form. — The inverter form is different and calls for fewer components – steps, including condensers and mouse switches. The same dc relation voltage is to be used separately [4] in that H-bridge network. There’s some pain. The new goods have been equipped with reduced reactors and condensers, substituted with separate data sources which need at least three independent sources. The two-way switch approach was taken to identify the difference in input and output; while the source of input is adequate, it contributes to the complex configuration of the circuit with the implementation of two-way switches.

2. Multilevel Inverter with Cascaded H-Bridge
A one dc power supply and three separate 3 phase Low Frequency transformers are available on the Cascaded H-bridge multilateral inverter. Compared to conventional three-phase multi-level transformers, the latest design will that a number of transformers. This makes the installation of a simple, powerful inverter. The Newto Raphson process, based on each switch’s operation, calculates every relay corner for each switch. The linearization technique can be used in each area for all relay angles. Through this process, low-harmonic tension components are removed [3].

The Cascaded multi-level inverter promises high-powered electrical energy topology [2] due to its low EMI and low frequency control methods [6]. The current stage includes a 2n + 1 level of n-DC sources for a cascading multi-level inverter. The use of this inverter will avoid the use of too many different DC sources in many applications. In the Cascading H-bridges inverter known as the HC-bridge multilevel inverter (H-bridge) [4], a first source may be used with other (n-1)-DC sources to eliminate the need for DC sources to be linked to a separate engine drive. HCMLI can be used for a specific motor powertrain.

Fig. 1 demonstrates a design circuit with four separate H-bridges for inverter devices H-bridge [9]. This has a nine-level output voltage. The voltage is low, with H-bridge cells linked by series.

2.1 Working principle of Hybrid Cascaded Multilevel Inverter (HCMLI)
Condensers can be used to operate a Cascaded Multi-Level Inverter with one DC source as a DC source for all but the first source [3]. Build a two H-bridge inverter as shown in the Fig.1. A battery or fuel cell with a Vdc voltage is DC source for start of the H Bridge while the dc source is a Vc condenser for the next H bridge. The ultimate voltage of the H start is V1 and the corresponding H-bridge is V2.

\[ v(tf) = v1 (ts) + v2 (tn) \] (1)
The Next Bridge output voltage can be set to 0, -Vdc, Vdc and next output voltage from −Vc, 0, or Vc is adjusted by switching off and on by activating and disabling the starting bridge switches. The reverser voltage also can be set to nine end-rate values −Vdc+Vc, Vdc, −Vc, Vdc and Vc. In other situations the reverser voltage can also be set at 9 final-rate values. The inverter tension is then available at the end of the device. All possible voltage levels should be used in the condenser voltage control scheme. A Regular Vdc/2, -3Vdc/2, Vdc, −vdc, − vdc/2, Vdc/2, 3Vdc/2 can be used. If the VC with a Vdc/2 voltage capacitor is made, Fig. 4 displays the final values as shown in Table 1. and Fig. 2.

The Fig. 4 displays 01 ≤ θ < 02 power for the v1 = Vdc and v2 = −Vdc/2 and waveform voltage of H-bridge voltages. When 01 ≤ θ < 02 is used, Fig. 3 will be produced when V1 = Vdc and V2 = Vdc/2 are selected.
Table 1. Seven-level inverter output voltages

| θ   | V1 | V2 | V = V1 + V2 |
|-----|----|----|-------------|
| 0 ≤ θ < θ1 | 0  | 0  | 0           |
| θ1 ≤ θ < θ2 | 0  | Vdc/2 | Vdc/2      |
| θ2 ≤ θ < θ3 | Vdc/2 | -Vdc/2 | Vdc/2      |
| θ3 ≤ θ ≤ θ2 | Vdc/2 | Vdc/2 | Vdc/2      |

3. Modulation Control

For multi-level inverter modulation control, PWM control and space vector methods are used. The more losses are caused by the high-frequency procedures [8]. This makes it possible to monitor HCMLI using methods like selective harmonic removal procedure, simple frequency switches or active harmonic removal methods. We use the basic frequency approach from the proposed work [5].

3.1 Voltage switching control with 7 level equal step output

The expansion of the 7-stage corresponding voltage waveform from the Fourier series shown in the Fig. 3

\[
V(t) = \sum_{n=1,3,5}^{\infty} \frac{2V_{dc}}{n\pi} (\cos(n\theta_1 + \cos(n\theta_2 + \cos(n\theta_3))) \sin(nwt) \quad (2)
\]

Where n is the multi-level inverter's harmonic output voltage number [6]. Likewise, with V1 as the ideal fundamental voltage, the angles of switch θ1, θ2, and θ3 will be set in such a way as to remove the V(ωt) = V1 sin(ωt) and higher V(nωt) harmonics. The goal of this project is to accomplish the fundamental and remove the 5th and 7th harmonics. The solution for the following equations can be formulated by (2):

\[
\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) = 3 \quad (3)
\]
\[
\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0 \quad (4)
\]
\[
\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) = 0 \quad (5)
\]
The model suggested by three unknown inspired equations $\theta_1$, $\theta_2$, and $\theta_3$.

### 3.2 Hybrid Cascaded Multilevel Inverter Features

The core features are as follows:

- Cascaded inverters need to be converted into DC Power contact sources to one dc of electrical AC. PWM (SHEPWM) technologies will be the only choice for selective harmonic elimination. New dc sources, including fuel cells and biomass, must be produced for various renewable energy sources.

- In the consequent mode it is not possible to link the DC connection sources and converters as a short circuit between the synchronization can be installed.

### 3.3 Hybrid Cascaded Multilevel Inverter- Advantages

Cascaded inverter's key advantages are:

- Less parts are needed to achieve the same output voltage than diode clamped and flying power inverters.
- There are no other clamping diodes or voltage balance condensers needed for each stage.
- The architecture and functionality of all the circuits are perfect.
- In order to reduce system voltage decreases and stress, different soft switching strategies are necessary.

### 4. Proposed Cascaded H-Bridge Multi-Level Inverter with Multi-Winding Transformer

The topology of multi-wind transformers can be called a multi-source topology type. A four-cell multi-coiling inverter is shown in the Fig. 5

![Figure 5. Symbol of multi-winding transformer](image)

#### 4.1 Circuit configuration

Fig. 6 displays the new multi-level network inverter supply configuration [2]. A rising source dc and many low frequency transformers are available. For three-stage transformers, the number of necessary parts and system volume can be reduced. The main side is linked to the VDC, zero and VDC supply bridges. The transformer’s secondary side is linked to the production stage of the show. The three-phase terminal is connected to a delta to limit the third harmonic portion of the device. The Figs appears in 6 and 7 display transformers in three stages. The VAS voltage is connected serially with three terminal outputs. The multilevel inverter can be transmitted as a multi-level cascading inverter for H-bridge in this particular configuration. In the Fig. 6 The ultimate H-bridge inverter voltages associated with the Kth transformer are Vak, Vbk, and Vck voltages. The final voltages for each of the three phase values therefore belong to VAk, VBk and Vck[9].
5. Harmonic Reduction Technique
The LOH angles are used by four different equations, especially the fifth and seventh or 11th voltages. Equation 2.2 adjusts the required RMS voltage simultaneously. For fifth, seventh and eleventh grade harmonics, the remaining equations are employed. The THD is absolutely popular.
The four equations are

\[ \cos \alpha_1 + \cos \alpha_2 + \cos \alpha_3 + \cos \alpha_4 = 3 \pi m \]  
\[ \cos 5 \alpha_1 + \cos 5 \alpha_2 + \cos 5 \alpha_3 + \cos 5 \alpha_4 = 0 \]  
\[ \cos 7 \alpha_1 + \cos 7 \alpha_2 + \cos 7 \alpha_3 + \cos 7 \alpha_4 = 0 \]  
\[ \cos 11 \alpha_1 + \cos 11 \alpha_2 + \cos 11 \alpha_3 + \cos 11 \alpha_4 = 0 \]  

The MathCAD software has found the angles of control and complies with the above
\[ \alpha_1 = 12.844^\circ; \quad \alpha_2 = 29.918^\circ; \quad \alpha_3 = 50.983^\circ; \quad \alpha_4 = 64.239^\circ; \]

The total harmonic distortion is defined as

\[ \text{THD} = \sqrt{V_3^2 + V_5^2 + V_7^2 + \ldots \ldots + V_{31}^2} \]  

The transcended equations are converted into polynomials first. The four equations are then rendered by the variables. Consider \( \cos \theta_i = x_i; \)

\[ \cos(5\theta) = 5\cos \theta - 20\cos^3 \theta + 16\cos^5 \theta \]  
\[ \cos(7\theta) = -7\cos \theta + 56 \cos^3 \theta - 112 \cos^5 \theta + 64 \cos^7 \theta \]  
\[ \cos(11\theta) = -11\cos \theta + 220 \cos^3 \theta - 1232 \cos^5 \theta + 2816 \cos^7 \theta - 1024 \cos^{11} \theta \]  

The polynomials are formed by

\[ P_1(X) = X_1 + X_2 + X_3 + X_4 - m \]  
\[ P_2(X) = \sum_{i=1,3,5,7} (5X_i + 20X_i^3 + 16X_i^5) \]  
\[ P_3(X) = \sum_{i=1,3,5,7} (-11X_i + 220X_i^3 - 1232X_i^5 + 2816X_i^7 + 1024X_i^{11}) \]  

There are four unknown equations. Consequently, all measurements must be made. It led to a series of polynomial equations rather than trigonometric. There is a well-known theory that many polynomial equations can be solved, but the grade is very high. The resulting theory is used to solve this sequence of equations. \( \alpha_1, \alpha_2, \alpha_3, \alpha_4 \) which increases the overall harmonic voltage following the MathCAD phase, is the final solution.

6. Simulink model of CMLI

Figs 8 and 9 displays simulation proposed the 3ø CMLI specification. Three separate subsystems make up this architecture. A subsystem frame including it is specified in each subsystem block. Each subsystem builds into a group to reduce the complexity of design. Growing subsystem has a CMLI level of 7. To measure the increased voltage values of the circuit, a voltage measurement unit is used.
**Figure 8.** Proposed simulation design of 3ø- CMLI

6.1 Subsystem Model of CMLI

**Figure 9.** Subsystem model of CMLI

6.2 Output Voltage

Fig. 10 displays the final voltage of the 110V input voltage with the CMLI tri-phase simulation. The final tension of every block is 110 V and the total tension is 330 V.
6.3 Harmonic Profile

Fig. 11 displays the harmonic rates of the 7 stadium cascaded MLI. Cumulative harmonic distortion (CHD) is shown to be 9.55%. The 3rd order is about 2.0%, and the harmonics are around 2.3%.

7. Hardware Results and Discussion

MOSFETs to test the HCMLI proposal using the H-Bridge Multi-stage inverter with seven switching system equivalent voltages. A single DC supply is used to power the inverter. MOSFET feed is the door signals. The MOSFET pulses of the first H-bridge are aligned with the H-bridge positive leg pair pulse. This is shown in Fig. 12. A standard PIC 16F877A microcontroller performs the control algorithm and generates the PWM waveforms for the MOSFET drive inverter. By using Microcontroller, the control gate
signals are giving to the each pair of MOSFET unit and the corresponding gate pulse trigger to the particular pair of MOSFET unit will conducting. Finally we are connecting positive leg pairs of MOSFET and negative leg pairs of MOSFET through a three phase transformer. We are getting a seven level output voltage wave form which is shown in Fig. 13

7. Conclusion
A multi-level waterfall inverter is the first cascaded hybrid inverter. For a hybrid multi-tiered converter, the 7-level wave shape is similar to the sinus wave. The seven-story cascading multi-level inverter created at the price was used to demonstrate the effects of simulations. Seven phases of cascading hybrid inverter load and voltage are given in the hardware implementation compared to the voltage of the output simulation. Regularly and in more harmonic intervals the various modern electronics are developed. Such frequencies are referred to and used to check their original elements, often without legislative power. Normal monitoring systems are also possible to detect the consequences of their variable control distortions in a certain way. The HCMI generates the desired waveforms with a single power source for each operation. Time is indifferent and the phase waveform had minimum total harmonic distortion for this experiment. The ratio of frequencies is indifferent. The harmonics in the fifth and seventh order are based on harmonic removal procedures. There is no algorithm for the fifth and seventh harmonics of this section. The
simulation and testing were carried out to see how the program was operating. The studies show that only about 14.27 per cent of the THD is estimated. The third order is just 5.2% and the fourth order is 8.2%.

8. References

[1] J. N. Chiasson, B. Ozpineci, and L. M. Tolbert, "A five-level three-phase hybrid cascade multilevel inverter using a single DC source for a PM synchronous motor drive," in Proc. IEEE APEC, 2007, pp. 1504-1507.
[2] J. Vassallo, Nov. 2–6, 2003 “A power-equalized harmonic elimination scheme for utility-connected cascaded H-bridge multilevel converters”, in Proc. IEEE Ind. Electron. Soc. Annu. Conf, pp. 1185–1190.
[3] J. R Wells., Jan. 2007 “Modulation-based harmonic elimination”, IEEE Trans. Power Electron., vol. 22, no. 1, pp. 336–340.
[4] J. Rodriguez, P. W. Hammond, J. Pontt, R. Musalem, P. Lezana, and M. J. Escobar, "Operation of a medium-voltage drive under faulty conditions," IEEE Trans. Ind.Electron., vol. 52, no. 4, pp. 1080-1085, Aug. 2005.
[5] J. Rodriguez, “ Multilevel voltage-source-converter topologies for industrial medium voltage drives”, IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec.2007.
[6] F. Z. Peng, L. Chen, and F. Zhang, “Simple topologies of PWM ac-ac converters,” IEEE Power Electron. Letters, vol. 1, no. 1, pp. 10–13, Mar. 2003.
[7] Z. Du, L. M. Tolbert, J. N. Chiasson, B. Ozpineci, "A cascade multilevel inverter using a single fuel cell DC source", Proc. IEEE APEC; vol. 1, pp. 426-430, Mar. 2006
[8] J. Rodriguez, B. Wu, S. Bernet, J. Pontt, and S. Kouro, “Multilevel voltage source-converter topologies for industrial mediumvoltage drives,” IEEE Trans. Ind.Electron., vol. 54, no. 6, pp. 2930–2945, Dec. 2014.
[9] Xu, R.; Yu, Y.; Yang, R.; Wang, G.; Xu, D.; Li, B.; Sui, S. “A Novel Control Method for Transformerless H-Bridge Cascaded STATCOM with Star Configuration”. IEEE Trans. Power Electron. 2015, 30, 1189–1202.
[10] Rahman, M.A.; Islam, M.R. “Modified High Frequency Phase Disposition Pulse Width Modulation for Modular Cascaded H-bridge Multilevel Converters”. In Proceeding of the 2017 3rd International Conference on Electrical Information and Communication Technology (EICT 2017), Khulna, Bangladesh, 7–9 December 2017; pp. 1–5.
[11] Gadalla, A.S.; Yan, X.; Altahir, S.Y.; Hasabelrasul, H. “Evaluating the capacity of power and energy balance for cascaded H-bridge multilevel inverter using different PWM techniques”. IET J. Eng. 2017, 1713–1718.