Landside capacitor efficacy among multi-chip-module using Si-interposer

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Abstract  Power delivery network (PDN) impedance reduction is strongly required for recent high-performance graphical-processing-unit, and mobile electronics that requires massive data transfer among logic and memory dice. To improve PDN characteristics, low equivalent series inductance and resistance (ESL and ESR) are required for capacitor, as well as powerline routing including placement of the capacitor. In this paper, we focus on Si-interposer as a method to enable ultra-high bit rate as well as fan-out wafer level packaging. A Si-interposer with transmission lines is manufactured, and CMOS test vehicle and low ESL Si-capacitors are mounted on the Si-interposer to evaluate chip-to-chip communication performance on multi-chip-module (MCM), through evaluating powerline noise. Experimental results of in-place waveform with physically different capacitor types and placements on Si-interposer, by on-chip waveform monitoring (OCM) technology. PDN analysis clarified the efficacy of low profile Si-capacitors and placement strategy to minimize series parasitic components, captured waveform shows stabilized drain power voltage (VDD) waveshape through 12-channels low-voltage differential signaling (LVDS) transceivers operation.

Keywords: Si-interposer, capacitor, PDN, on-chip evaluation

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Recent high-performance graphical-processing-units (GPUs) and small footprint processing unit in mobile electronics requires extremely high bit rate between memory and processor, which requires stable PDN for multi-channel, high-speed, and low-power data transfer [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13]. For such a communication among logic and memory, MCM integration including 3D-stacked ICs, Si-interposer, and redistribution layer (RDL) based fan-out modules are required to minimize distance of transmission path [14, 15, 16, 17, 18].

Powerline design is also important for better signaling, to manage current consumption of enormous interface circuitry with minimizing simultaneous switching noise and IR drop. Improvement of the PDN characteristics demands lower parasitic inductance and resistance on the path between circuitry and capacitor, hence many studies focus on PI/SI analysis and improvement idea, including capacitance in Si-interposer and in-place voltage regulator [19, 20, 21, 22, 23, 24, 25, 26, 27].

In this study, we focus on PI in MCM employing Si-interposer with capacitors on the interposer. A couple of CMOS test chips are manufactured and mounted on the Si-interposer, to excite powerline noise by chip-to-chip data transaction and capture the noise using on-chip waveform capturer [28, 29]. Impedance between communication circuitry and capacitor is analyzed as well as total PDN and compared with measurement to discuss efficacy of capacitor performance and placement on Si-interposer.

2. Test vehicle overviews

Fig. 1 shows overview of the test vehicle in this study. Two CMOS test chips are mounted on Si-interposer to construct MCM with chip-to-chip communication functionality. The stacked module is mounted on a motherboard with solder balls after mounting landside capacitors (LSCs) on the motherboard side of the interposer.

The motherboard has a trench area for LSCs, for a case LSC height is larger than the gap between Si-interposer and motherboard. Motherboard capacitors (MBCs) are also mounted at just below the LVDS circuitry of the CMOS, on the solder side of the motherboard.

Figs. 2(a) and (b) show photos of CMOS side and motherboard side of the Si-interposer, and Fig. 2(c) shows cross-sectional structure. The Si-interposer is designed and manufactured with total 3 layer of 5 μm L/S pattern and 10 μm of diameter and 100 μm of depth TSVs. On the CMOS side, 162.5 μm pitch micro-bumps are formed to connect CMOS test chips and interposer, and on the motherboard side, Au electroplated lands are arrayed with 300 μm pitch to connect the Si-interposer and the motherboard with solder balls. As for capacitors on Si-interposer, lands compatible with 0603 size capacitor are prepared for both sides, the pads on the motherboard side is for LSCs, and another side is for die side capacitors (DSCs).

Figs. 3(a) and (b) show top-view photo and cross-sectional diagram of the assembled test vehicle, respectively. The CMOS test chip is manufactured with 0.18 μm CMOS process. 12 pairs of LVDS transmitter (Tx) and receiver (Rx) circuits are embedded in a single die, to enable chip-to-chip communication. A controller circuitry is also included to generate data for LVDS Tx and check error for LVDS Rx. An on-chip waveform capturer [29] is employed for PI/SI evaluation, which can acquire transient waveforms of

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powerline and a signal pair voltage of LVDS.

3. Measurement and analysis

Fig. 4 shows measured transient waveforms of LVDS Rx VDD during 3 cycles of 16-bit transmission, and each frequency components are also plotted. The waveforms in Fig. 4(a) and (b) are captured with the test vehicles with 2 and 12 multi-layer ceramic capacitors (MLCCs) as LSC, respectively. In a case of Fig. 4(c), 12 low profile and low ESL Si-capacitors [30] are used. From measured waveforms and frequency components, we can see larger capacitance and lower ESL of 157 pH of Si-capacitors improve PI of the LVDS, in comparison with ESL of 275 pH of standard MLCCs.

PDN impedance of each case is analyzed and shown in Fig. 5. From the impedance plot, not only large capacitance but also low ESL affects to the impedance curve, especially
Fig. 4 Measured transient waveform and frequency component plot with (a) 2 MLCCs, (b) 12 MLCCs, and (c) 12 Si-capacitors.

Fig. 5 Simulated PDN impedance of the test vehicle.

Fig. 6 (a) Considerable placement of capacitor, (b) impedance of the path between capacitance and LVDS VDD and (c) 10 nF Si-capacitance with (b).

in high-frequency area which covering 750 MHz to 1.5 GHz.

From the frequency component difference between Fig. 4(b) to (c) and PDN impedance curve in Fig. 5, we can say low ESL Si-capacitors as LSC effectively improve the PI/SI of chip-to-chip communication system in MCM.

Fig. 6 analyzes the impedance among the capacitors dif-
ferently positioned on the Si-interposer with respect to the VDD terminal of LVDS transceiver circuits. From the analytical result, LSC efficacy by comparison of MBC and LSC, and dependency of horizontal distance by comparison among two LSC cases and DSC. Although MBC placement shows inductance of 446 pH that almost 3 times large as Si-capacitor’s ESL of 157 pH, the best case of LSC placement shows inductance of 44.9 pH that can utilize lower ESL characteristic of Si-capacitor and show clear improvement from standard MLCC. On the other hand, large dependency of the horizontal distance is considered to be from fine but thin metal layer of Si-interposer, because of the process restriction, including limitation of plane size for damascene process. These results suggest that Si-interposer requires more strategical design to keep impedance low in comparison to fan-out interposer [27] with thick metal. On the other hand, Si-interposer has relatively fine L/S, hence a greater number of channels are enabled to raise bitrate or improve energy efficiency by slowing frequency.

As for capacitor types, Si-capacitor is suitable for dense integration like MCMs, due to its 85 μm of height enough lower than 121 μm of the gap between Si-interposer and motherboard. This easiness of assembly will allow cost reduction and motherboard wiring resource flexibility.

4. Conclusion

PI and SI will affect performance of logic-memory transaction among densely integrated ICs in MCM. Smaller component size and advanced packaging technologies enable various methodologies to improve PDN characteristics by flex and dense placement of capacitors.

In this study, we presented in-place measured waveforms on power delivery with physically different capacitor types and placements within multi-chip integration on Si-interposer. Measured powerline noise of LVDS transaction is well suppressed by employing low ESL capacitor as LSC on the Si-interposer. Analytical consideration shows LSC has far lower parasitic inductance in comparison with MBC and suggests that nearby LSC on Si-interposer can utilize low ESL characteristics of Si-capacitor. The dependency of the capacitor placement of Si-interposer is also shown, due to relatively higher resistive metal for fine L/S. From these results, low profile Si-capacitors are suitable for densely integrated modules, by system requirement of higher capacity and placement flexibility.

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