Current-induced control of the polarization state in a polar metal based heterostructure SnSe/WTe$_2$

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The concept of a polar metal proposes new approach of current-induced polarization control for ferroelectrics. We fabricate SnSe/WTe$_2$ heterostructure to experimentally investigate charge transport between two ferroelectric van der Waals materials with different polarization directions. WTe$_2$ is a polar metal with out-of-plane ferroelectric polarization, while SnSe ferroelectric semiconductor is polarized in-plane, so one should expect complicated polarization structure at the SnSe/WTe$_2$ interface. We study $dI/dV(V)$ curves, which demonstrate sharp symmetric drop to zero $dI/dV$ differential conductance at some threshold bias voltages $\pm V_{th}$, which are nearly symmetric in respect to the bias sign. While the gate electric field is too small to noticeably affect the carrier concentration, the positive and negative threshold positions are sensitive to the gate voltage. Also, SnSe/WTe$_2$ heterostructure shows re-entrant transition to the low-conductive $dI/dV = 0$ state for abrupt change of the bias voltage even below the threshold values. This behavior can not be observed for single SnSe or WTe$_2$ flakes, so we interpret it as a result of the SnSe/WTe$_2$ interface coupling. In this case, some threshold value of the electric field at the SnSe/WTe$_2$ interface is enough to drive $90^\circ$ change of the initial SnSe in-plane polarization in the overlap region. The polarization mismatch leads to the significant interface resistance contribution, analogously to the scattering of the charge carriers on the domain walls. Thus, we demonstrate polarization state control by electron transport through the SnSe/WTe$_2$ interface.

INTRODUCTION

Recently, ferroelectric van der Waals materials attract significant interest both for the fundamental physics and for promising applications in quantum sensors, new memory devices, and for the ferroelectric field-effect transistors [1–4]. For the fundamental research, some of these materials represent a novel concept of the intrinsic polar metal [5–9]. The latter can be regarded as a ferroelectric in metals, it is characterized by intrinsic conduction and inversion symmetry breaking [5].

Due to the finite conductance in polar metals, they propose new approaches to control ferroelectric polarization. For example, it is possible to control polarization by charge current or, vice versa, to control charge transport by the ferroelectric polarization. Out-of-plane polarization can be affected or even switched in well conducting semimetals MoTe$_2$ and WTe$_2$ by piezoresponse force microscopy (PFM) [10, 11]. Also, the initial in-plane polarization can be managed in SnSe and SnTe semiconductors using scanning tunneling microscope (STM) technique [12, 13]. Manipulation of charge transport by ferroelectric polarization is important for ferroelectric field-effect transistors (FeFET), as it has been demonstrated for In$_2$Se$_3$-based structures [2]. Ferroelectric polarization can be controlled also by the in-plane current-induced electric field in WTe$_2$ and SnSe thin films [14, 16]. Van der Waals materials also offer strain control of ferroelectric polarization [17].

In the sense of the ferroelectric polarization control, it is quite natural to consider also van der Waals heterostructures with one or several ferroelectric materials and (possibly) some other layers. For example, MoS$_2$/h-BN/graphene/CuInP$_2$S$_6$ heterostructure has been proposed for long-retention memory [18], while GeSe/MoS$_2$ heterojunction represents novel FeFET realization [19]. For the heterostructures with polar metals, theory predicts [3] realization of multiple states with different relative directions of polar displacements due to the interface coupling effects. If both the ferroelectric materials are conducting, like for WTe$_2$ and SnSe, the interface coupling, and, therefore, the polarization state, could be supposed to be controlled directly by electron transport through the heterostructure.

Here, we fabricate SnSe/WTe$_2$ heterostructure to experimentally investigate charge transport between two ferroelectric van der Waals materials with different polarization directions. WTe$_2$ is a polar metal with out-of-plane ferroelectric polarization, while SnSe ferroelectric semiconductor is polarized in-plane, so one should expect complicated polarization structure at the SnSe/WTe$_2$ interface. We study $dI/dV(V)$ curves, which demonstrate sharp symmetric drop to zero $dI/dV$ differential conductance at some threshold bias voltages $\pm V_{th}$, which are nearly symmetric in respect to the bias sign. While the gate electric field is too small to noticeably affect the carrier concentration, the positive and negative threshold positions are sensitive to the gate voltage. Also, SnSe/WTe$_2$ heterostructure shows re-entrant transition to the low-conductive $dI/dV = 0$ state for abrupt change of the bias voltage even below the threshold values. This behavior can not be observed for single SnSe or WTe$_2$ flakes, so we interpret it as a result of the SnSe/WTe$_2$
SnSe layered single crystal was grown by vertical zone melting in silica crucibles under argon pressure. WTe₂ compound was synthesized from elements by reaction of metal with tellurium vapor in the sealed silica ampule. The WTe₂ crystals were grown by the two-stage iodine transport [20]. Ultra-thin SnSe and WTe₂ flakes (about 100-200 nm) are obtained by regular mechanical exfoliation from the initial layered ingot. Thin single-crystal flakes of these materials have been well characterized in transport investigations [11, 16, 27, 28].

We assemble SnSe/WTe₂ heterostructure on the pre-defined Au leads pattern to avoid chemical or thermal treatment of the initial materials, similarly to single-flake samples [15, 16, 27–29]. 5 μm separated leads are formed on the standard SiO₂ substrate by lift-off technique after thermal evaporation of 100 nm Au. To obtain separate contacts to the individual layers, thin SnSe and WTe₂ flakes are placed on two independent contact groups (the left and the right ones in Fig. 1), so Au-SnSe or Au-WTe₂ junctions are formed at the bottom surfaces of the individual flakes. This procedure provides electrically stable contacts with highly transparent metal-semiconductor interfaces, which has been verified for the individual flakes [15, 16, 27–29]. SnSe/WTe₂ heterostructure appears as a small (40 μm×20μm) overlap of the flakes at the center of the structure in Fig. 1. Despite the apparent simplicity of the heterostructure fabrication, the samples are stable even for long-period measurements, the observed behavior can be well reproduced for different samples, as it is demonstrated below. Also, SiO₂ substrate protects the flakes from any oxidation/contamination [29], so all measurements are taken at room temperature under ambient conditions.

The prepared heterostructure allows to measure electron transport across SnSe/WTe₂ interface. In the case of high resistance samples, one have to use two-point technique with direct application of the voltage bias V to one of the left contacts in Fig. 1 in respect to one of the right contacts. We analyze differential conductance dI/dV behavior in dependence on the dc voltage bias. To obtain dI/dV(V) curves, the applied dc bias V is additionally modulated by a small (10 mV) ac component at about 1 kHz frequency. The ac current component is measured by lock-in, being proportional to differential conductance dI/dV at a given dc bias value. We verify that the obtained dI/dV(V) curves are independent of the modulation frequency in the range 1 kHz–10 kHz, which is determined by applied filters. Also, standard oxidized silicon substrate allows to apply the gate voltage Vg to the p-doped silicon across the 100 nm oxide layer. Even for relatively thick (100-200 nm) flakes, ferroelectric polarization is sensitive to the gate electric field [14], since the relevant (bottom) flake surfaces are adjoined to the SiO₂ surface.

**SAMPLES AND TECHNIQUES**

WTe₂ is usually considered as a Weyl semimetal [20, 21], while now it is also an example of a polar metal with out-of-plane ferroelectric polarization [11]. The polarization is observed even for three-dimensional crystal due to broken inversion symmetry for Td crystal structure [22, 23]. SnSe is a semiconductor, the in-plane ferroelectric polarization appears [24] due to the distortion of centrosymmetric Pnma orthorhombic structure at low thicknesses [12]. The critical thickness can be estimated [25] as 300 nm for SnSe.

For the present experiment, SnSe compound was synthesized by reaction of selenium vapors with the melt of high-purity tin in evacuated silica ampules. The SnSe layered single crystal was grown by vertical zone melting in silica crucibles under argon pressure. WTe₂ compound was synthesized from elements by reaction of metal with tellurium vapor in the sealed silica ampule. The WTe₂ crystals were grown by the two-stage iodine transport [20]. Ultra-thin SnSe and WTe₂ flakes (about 100-200 nm) are obtained by regular mechanical exfoliation from the initial layered ingot. Thin single-crystal flakes of these materials have been well characterized in transport investigations [11, 16, 27, 28].

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Experimental Results

$dI/dV(V)$ behavior is shown in Fig. 2 (a) for two dc bias $V$ sweep directions for one of the SnSe/WTe$_2$ heterostructures. At low biases (below $\pm 1.2$ V), $dI/dV(V)$ behavior is nonlinear with small hysteresis around the zero bias. This low-bias region is enlarged in the inset to Fig. 2 (a), both the hysteresis and $dI/dV(V)$ behavior are known to originate from ferroelectric polarization for the individual WTe$_2$ and SnSe flakes [14,16]. In Fig. 2 (a), $dI/dV(V)$ curves demonstrate a drop to zero conductance at $V_{th} \approx \pm 1.2$ V bias values. This $dI/dV$ conductance drop shows practically no hysteresis, so $dI/dV$ is abruptly changed at the same threshold voltage value $V_{th}$, irrespectively to the voltage sweep direction. Also, $V_{th}$ value is well reproducible in different voltage sweeps, it is unique for a particular sample: $V_{th}$ value is inversely proportional to the zero-bias conductance (see below the description of Fig. 4).

The threshold position can be affected by the gate voltage, see Figs. 2 (b) and (c). Negative gate voltages decrease the $V_{th}$ value for positive biases and simultaneously increase it for the negative one, so the $dI/dV(V)$ curve is shifted monotonously to negative biases. The effect is well-noticeable, it is about 4% of the $V_{th}$ value. In contrast, the gate electric field does not change the $dI/dV$ conductance below the threshold, so the carrier concentration is constant for the applied gate voltages. We check, that there is no gate leakage in the present gate voltage range.

For a single SnSe or WTe$_2$ flake, the low-bias hysteresis reflects slow relaxation processes due to the additional polarization current in conductive ferroelectrics [14,16]. Fig. 3 shows this behavior for the individual WTe$_2$ layer. Even well-conducting WTe$_2$ single crystals demonstrate ferroelectricity at room temperature, which has been shown by direct visualization of ferroelectric domains [11]. In our setup, there are two possible directions of the external electric fields in the WTe$_2$ layer, the result is depicted in Fig. 3 (a) the source-drain field $E_{sd} = \rho_j$, which is connected with the flowing current, $E_{sd}$ is parallel to the WTe$_2$ surface; (b) The gate field, $E_{gate} = V_g/d$, where $d = 300$ nm is the SiO$_2$ oxide thickness, $E_{sd}$ is directed normally to the WTe$_2$ surface. Any variation of electric fields leads to the additional polarization current.

In the latter case we observe a standard Sawyer-Tower ferroelectric polarization loop [30,31], similarly to the polarization change by high external electric field in Ref. [11]. The loop center is slightly shifted in Fig. 3 (b) due to the band bending at the gate dielectric interface. In the former case, source-drain field variation leads to the hysteresis of the same magnitude in Fig. 3 (a). Similar results can be obtained for the individual SnSe layer [12,16].

We also confirm the hysteresis sweep-rate dependence for low biases in Fig. 4 (a), but the threshold values $V_{th} \approx \pm 1.2$ V are well stable for different rates, low hysteresis can be seen around $V_{th} \approx \pm 1.2$ V position only for the highest sweep rate in the inset to Fig. 4 (a).

Qualitatively, similar $dI/dV(V)$ behavior can be demonstrated for SnSe/WTe$_2$ heterostructures with strongly different initial conductance, see Fig. 4 (b) and (c). The threshold $V_{th}$ positions are also symmetric, while the $V_{th}$ values are different in the figure: $V_{th}$ is inversely proportional to the zero-bias conductance for all three samples in Fig. 4 which implies constant threshold source-drain electric field, see the discussion below.

To our surprise, SnSe/WTe$_2$ heterostructure shows re-entrant transition to zero-conductance state even at low biases $V < V_{th}$, by abrupt change of the bias value $\Delta V$, as it is shown in Fig. 5. Let us start from $V = 0$, as depicted in the main field of Fig. 5. For low $\Delta V < 0.2$ V, $dI/dV$ is monotonously increased in exact correspondence with the $dI/dV(V)$ curve from Fig. 2 (a), the slow relaxation is insignificant for the scales in Fig. 5. For $\Delta V > 0.3$ V, this increase goes through the initial
abrupt change of the bias voltage as it is demonstrated in the inset to Fig. 5. Thus, the prominent hysteresis of the transition point [16, 33], at a wide temperature range at ambient pressure [22, 23].

The differential conductance goes through the \( \frac{dI}{dV} \) drop. The drop value grows with \( \Delta V \), so differential conductance goes through the \( \frac{dI}{dV} = 0 \) region for \( \Delta V > 0.5 \) V. This behavior does not depend on the initial bias \( V < V_{th} \) or the sign of the bias change \( \Delta V \), as it is demonstrated in the inset to Fig. 5. Thus, the abrupt change of the bias voltage \( V \) leads to re-entrant switching to zero conductance at low biases \( V < V_{th} \), while the zero-conductive state \( dI/dV \) state is stable at high biases \( V > V_{th} \).

**DISCUSSION**

As a result, SnSe/WTe\(_2\) heterostructure demonstrates sharp symmetric drop to zero \( dI/dV \) differential conductance at some threshold bias voltage \( V_{th} \), which is sensitive to the gate voltage. Moreover, SnSe/WTe\(_2\) heterostructure shows re-entrant transition to the low-conductive state for abrupt change of the bias voltage even below the threshold. This behavior is well reproducible for different SnSe/WTe\(_2\) samples, while it can not be observed for single SnSe or WTe\(_2\) flakes [14, 16].

First of all, we should exclude sample overheating by the flowing current as the origin of the observed effects. WTe\(_2\) crystal structure (T\(_d\)) is known to be stable in a wide temperature range at ambient pressure [22, 23]. The martensitic phase transition is known [32] for SnSe at \( \approx 480-530^\circ C \), but it is necessarily accompanied by the prominent hysteresis of the transition point [16, 33], which is just opposite to the \( dI/dV \) behavior in Figs. 2 and 4. Also, temperature-induced phase transition is inconsistent with the re-entrant transition to the low-conductive state in Fig. 5.

Also, any band bending/reconstruction effects at the interface should be strongly asymmetric in respect to the bias sign, while experimental \( dI/dV \) curves are highly symmetric in Figs. 2 and 5, so any possible influence of the band bending/reconstruction effects is within the small difference between the positive and negative thresholds in Fig. 2 (b) and (c). It can be estimated as about 0.05 V, the gate voltage effect is of the same value. We can not expect significant band bending for the well-conducting WTe2 and SnSe materials.

It is important, that low-bias \( dV/dI(I) \) behavior reflects polarization dynamics in conductive ferroelectrics [14, 16] in Figs. 2 and 4. Thus, it is quite reasonable to ascribe the observed high-bias behavior to the interface coupling of the ferroelectric polarizations at the SnSe/WTe\(_2\) interface, as it was predicted in Ref. [5]. WTe\(_2\) is characterized by semimetal spectrum [20, 21] with out-of-plane ferroelectric polarization [11], so it is a good representation of the polar metal concept [5]. SnSe thin flake is a ferroelectric semiconductor with in-plane polarization, while the SnSe conductivity is significant at room temperature [22]. Thus, SnSe/WTe\(_2\) bilayer can be considered as a heterostructure between two conducting ferroelectrics with different polarization.
of the bias change connected resistances of the SnSe/WT e between C3 and C6 in Fig. 1) consists of the in-series measurements. In our samples, the total resistance (e.g., about 40 \( \mu \)m \( \times \) 20 \( \mu \)m) with strong polarization mismatch. The latter leads to the significant interface resistance contribution, which we observe as the strong conductivity drop.

To understand the high-bias switching, it is important that current-induced electric field \( E_{sd} \) is oriented normally to the SnSe/WT\(_2\) interface due to the high WT\(_2\) in-plane conductance. It enhances the out-of-plane polarization in the WT\(_2\) layer, and, due to the interface coupling \([3]\), it should secondly switch the polarization out-of-plane also in the adjacent SnSe region at some threshold \( E_{sd} \) field. The planar contact (about 40 \( \mu \)m \( \times \) 20 \( \mu \)m) with zero polarization is transformed into the side junction (\( \approx 40 \mu \)m \( \times \) 100 nm) with strong polarization mismatch. The latter leads to the significant interface resistance contribution, which we observe as the strong conductivity drop.

This effect is not sensitive to the bias sign, since both \( E_{sd} \) directions at the interface can drive 90\(^\circ\) change of the initial SnSe in-plane polarization \([3]\). Similarly to
$E_{sd}$, the gate electric field $E_g$ is directed normally to the SnSe/WTe$_2$ interface. Thus, it increases the interface field for one $E_{sd}$ direction and decreases it for the opposite one, as we observe in Fig. 2(b,c). The proposed model is also confirmed by the excellent stability of the threshold regions in the experimental curves, see Figs. 2 and 4. Any contact or scattering effects should demonstrate random fluctuations from sample to sample. In contrast, $V_{th}$ is inversely proportional to the zero-bias conductance at different threshold values in Fig. 5. At constant bias $V$ the SnSe/WTe$_2$ flakes are nearly equipotential because of low resistivity $\rho_{WTe_2} \ll \rho_{SnSe}$. Thus, the abrupt change in the bias $\Delta V$ is applied initially at the SnSe/WTe$_2$ interface, while it is redistributed afterwards over the resistive SnSe flake. It, therefore, temporary forces the transition to the low-conducting state, which can not be preserved after the field redistribution at $V < V_{th}$. In Fig. 5 re-entrant transition indeed depends on the $\Delta V$ value, so the time-dependent behavior confirms our interpretation of the SnSe/WTe$_2$ polarization state control by electron transport through the interface.

CONCLUSION

As a conclusion, we fabricate SnSe/WTe$_2$ heterostructure to experimentally investigate charge transport between two ferroelectric van der Waals materials with different polarization directions. WTe$_2$ is a polar metal with out-of-plane ferroelectric polarization, while SnSe ferroelectric semiconductor is polarized in-plane, so one should expect complicated polarization structure at the SnSe/WTe$_2$ interface. We study $dI/dV$ curves, which demonstrate sharp symmetric drop to zero $dI/dV$ differential conductance at some threshold bias voltages $\pm V_{th}$, which are nearly symmetric in respect to the bias sign. While the gate electric field is too small to noticeably affect the carrier concentration, the positive and negative threshold positions are sensitive to the gate voltage. Also, SnSe/WTe$_2$ heterostructure shows re-entrant transition to the low-conductive $dI/dV = 0$ state for abrupt change of the bias voltage even below the threshold values. This behavior can not be observed for single SnSe or WTe$_2$ flakes, so we interpret it as a result of the SnSe/WTe$_2$ interface coupling. In this case, some threshold value of the electric field at the SnSe/WTe$_2$ interface is enough to drive $90^\circ$ change of the initial SnSe in-plane polarization in the overlap region. The polarization mismatch leads to the significant interface resistance contribution, analogously to the scattering of the charge carriers on the domain walls. Thus, we demonstrate polarization state control by electron transport through the SnSe/WTe$_2$ interface.

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