The Promise of Dataflow Architectures in the Design of Processing Systems for Autonomous Machines

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Abstract

The commercialization of autonomous machines is a thriving sector, and likely to be the next major computing demand driver, after PC, cloud computing, and mobile computing. Nevertheless, a suitable computer architecture for autonomous machines is missing, and many companies are forced to develop ad hoc computing solutions that are neither scalable nor extensible. In this article, we analyze the demands of autonomous machine computing, and argue for the promise of dataflow architectures in autonomous machines.

1 Rise of the Autonomous Machines

The commercialization of autonomous machines is a thriving sector, with projected average compound annual growth rate (CAGR) of 26%, and by 2030 this sector will have a market size of $1 trillion [1]. Hence, this sector is likely to be the next major computing demand driver, after personal computers, cloud computing, and mobile computing.

Autonomous machines exist in multiple forms, e.g., cars, aerial drones, service robots, industrial robots. Different kinds of autonomous machines are quite diverse in size, shape, mission, goals, location, propulsion, etc. [2] Generally, completely independent teams have approached the design, resulting in a bevy of solutions, some replications but certainly no standardization. A better understanding of the underlying issues, a formalization of the common problems, and a certain unification of the solutions would all yield a more efficient approach to the design process.

The core of autonomous machines obviously resides in their computing systems, and encompasses both the hardware and the software level, entailing algorithms, systems software, compilers, as well as computer architectures. Despite the recent advancements in autonomous machine systems design of such major industrial organizations as Google [3], Tesla [4], Mobileye [5], Nvidia [6], the architecture of autonomous machine systems still largely remains an open research question since existing solutions are often made on an ad hoc basis, and not only the development process takes a long time, but the design itself is neither scalable nor extensible [7].

In this article, we first review the advantages of dataflow architectures and their implementation difficulties. Then we summarize the observations of autonomous machine computing, and delve into the details of why dataflow architectures may be extremely well adapted for autonomous machine computing.

2 Dataflow Architectures

Before delving into the details of autonomous machines computing, let us first review the benefits of dataflow architectures and their implementation roadblocks.
Dataflow concepts originated in the 1970s and 1980s, with pioneering work by Jack Dennis and Arvind, and several others [8,9]. The central idea of dataflow architectures was to replace the classic control flow, or von Neumann, architectures. In a von Neumann architecture, the processor follows an explicit control flow, executing instructions one after another. In a dataflow architecture, execution is event-driven such that an instruction is ready to execute as soon as all its inputs, or “tokens,” are available, rather than when the control flow gets to it. To bridge the gap between traditional architectures and the dataflow computing model, Gao et al. have developed the codelet execution model that incorporates the advantages of macro-dataflow and von Neumann model [10,11]. The codelet execution model can be used to describe programs in massive parallel systems. Specifically, the observations of autonomous machine computing, as we summarize in section 3, reveal that when the programming model renders the appropriate level of abstraction, a hybrid dataflow and domain-specific accelerator (DSA) architecture is extremely well adapted for autonomous machine applications.

Classic dataflow architecture, by representing a program as a dataflow graph, can naturally explore the instruction-level parallelism in a program by firing instructions as soon as their operands are ready, hence minimizing the control overheads. Despite the implementation difficulties of the pure dataflow concepts, such as the cost/benefit problem [12], the merit of dataflow graph representation and data driven execution has led to the emergence of superscalar architectures (using restricted dataflow graph to exploit instruction level parallelism), and multiple grid architectures (hybrids of control-flow and dataflow) [13,14], which map dataflow graphs onto grid processors and execute operations in a dataflow fashion to enable concurrent execution. In addition to the general purpose processors, the dataflow architecture’s properties of decentralized control and data-driven execution have been successfully used to synthesize power efficient application specific hardware [15].

In more detail, the original dataflow architecture proposals specify that dataflow machines are fine-grain parallel computers, where the processes are about the size of a single instruction in a conventional computer. Instructions are known as nodes, and the data passed between different nodes are called tokens. A producing node is connected to a consuming node by an arc, and the point where an arc enters a node is called an input port. The execution of an instruction is called the firing of a node. Execution of a node only occurs if the node is enabled when each input port contains a token. Under the dataflow execution model, there is no such thing as control flow and the problem of synchronizing data and control flow has disappeared, making dataflow programs well suited for parallel processing. In a dataflow graph, the arcs between the instructions directly reflect the partial ordering imposed by their data dependencies [16].

The dataflow execution model is remarkably powerful and, in recent years, has been widely used in cloud and distributed computing [17]. Hardware architectures based on the dataflow execution model, however, have not had equal amount of success, primarily for four reasons:

- **Insufficient Amount of Parallelism**: At the instruction level, many conventional programs do not have enough intrinsic parallelisms to utilize a realistic dataflow hardware except when processing large arrays. The lack of ILP in conventional programs begs the question: is instruction the right level of abstraction for dataflow architectures?

- **Explosion of Parallelism**: Conversely, the very lack of central control, so central to allowing parallelism may lead to an uncontrolled (and uncontrollable) demand for parallel resources, leading to deadlocks.

- **Producer-Consumer Speed Mismatch**: When the speed between the producer and consumer nodes are mismatched, either the producer (or consumer) will have to stall, leading to...
hardware under-utilization, or a large buffer is required to absorb the communication data volume, increasing the memory storage requirement.

The speed mismatch issue is exacerbated when a node has a high fan-out, in which case the classic dataflow architectures call for separate copies of each value to be sent from the producer to each consumer. Such copying could lead to a large, instantaneous, data volume that, again, either stalls the hardware awaiting memory buffers to be available, or requires excessive storage [18, 19].

Traditional dataflow architectures use hardware throttle mechanisms to mitigate the speed mismatch and cushion instantaneous spikes in data communication, defeating the performance gains promised by dataflow architectures [16].

- **Reentrancy**: Function reentrancy is critical to many concurrent and parallel programs. Supporting reentrancy on dataflow architectures [20], however, usually leads to drastic performance degradation. Static dataflow machines utilize hardware lock or acknowledgement methods, which often lead to under utilization of processing power. Dynamic dataflow machines employ copying or tagged tokens methods, which may lead to excessive storage needs. For instance, a loop is dynamically unfolded at run-time by creating multiple instances of the loop body and allowing the execution of the instances concurrently, but also requiring a large number of matching tokens [21].

3 Why dataflow Architecture is a Good Fit for Autonomous Machines

Traditional dataflow machines are fine-grain parallel computers, in that each node in the DFG represents a single instruction. Although it has been successfully applied to applications such as digital signal processing [22], this level of abstraction also imposes inherent implementation difficulties that prevented dataflow architectures from becoming mainstream. Worse, autonomous machine software is very complicated; using the conventional instruction-level abstractions is unscaleable. We must rethink the level of abstraction in applying dataflow architectures to autonomous machines.

Fortunately, the autonomous machine software stack, while complex, can be cleanly and succinctly expressed as a **macro dataflow graph**, where each node represents a high-level task such as motion planning. Taking this macro abstraction leads to a natural way of designing hardware, where each node is executed on a dedicated hardware accelerator, and different hardware accelerators are integrated to form a chip. This view allows us to think about hardware design at the top-level while allowing for innovations in individual tasks. This design philosophy also matches the trend in hardware chip design, where different vendors design their own IP blocks, which are reusable and can be integrated into a full SoC.

Figure 1 shows two M-DFGs for a Level-4 self-driving car and a home robot. While they differ in details, they share the same flow of data [23, 24, 25]. We will focus on the self-driving car case but the same principles apply to the simpler home robot. We summarize four key observations of the autonomous machine workloads which show how autonomous machines are naturally not subject to the pitfalls that conventional “general purpose” dataflow architectures encounter.

**Continuous Inputs Provide Abundant Parallelisms**  Autonomous machine workloads provide abundant parallelisms, and thus will not starve the hardware. In particular, the input to autonomous machines is continuous: as an autonomous machine operates, the sensing data continuously rushes in and exercises the various sensor processing nodes, which in turn generate continuous outputs that further exercise later nodes. As a result, with ideal load balance all the
Flexible Dependencies  Autonomous machine workloads have flexible dependencies in that a consumer node, while dependent on a producer node, does not have to consume every single piece of producer’s output.

The reason autonomous machine workloads exhibit flexible dependencies is fundamentally due to the soft real-time nature of the workload. Autonomous machines must operate in real time; thus, each node in the DFG has a strictly-defined output frequency. For instance, the image perception node processes images at 30 FPS; the LiDAR perception node processes point clouds at 10 FPS. Figure 1 annotates each node with a firing frequency. As a result, engineers intentionally design algorithms such that nodes do not block if the firing time of a node is reached. For instance, the planning algorithm fetches the latest produced data, essentially dropping previously produced data; the localization algorithms consumes a sequence of frames such that missing one frame of data is not catastrophic.

In dataflow parlance, autonomous machine workloads, instead of consuming every token, can afford to drop tokens and fetch the latest token from producers. As a result, producer-consumer speed mismatch does not require stalling the hardware components.

Deterministic Data Communication  The data communication volume across nodes is largely deterministic, because each node has a fixed output size (e.g., a 1080p image) and a fixed output frequency (e.g., 30 FPS of the perception node). Therefore, one could statically analyze the data communication patterns and estimate the storage requirement for the run-time data communication. This trait in combination with the flexible dependencies above allows autonomous machines to address the producer-consumer speed mismatch issue.

No Loops  Autonomous machine computing graphs are DAGs and the nodes within the DAGs are stateless. The DFG nodes are thus naturally non-reentrant, eliminating the difficulty to deal with reentrancy in conventional dataflow architectures.
4 Timing-Safe Dataflow Programming for Autonomous Machines

While we believe dataflow architectures are ready to implement efficient processing in autonomous machines, we must be able to program such machines. We see event-driven programming as a natural fit, but it must be made timing-safe to be widely used for autonomous machines.

Event-driven Programming for Dataflow Architectures. An event-driven architecture requires an event-driven programming model. A natural fit is functional programming [26], which is event-driven in nature and has long been used in programming dataflow architectures. While developing the MIT Tagged-Token Dataflow project, Arvind et al. demonstrated the natural match between functional programming and dataflow architectures, as every unit in a dataflow machine is a pure function whose outputs depend only on its inputs [27]. Gaudiot et al. argued that the functional model of computation allows the extraction of available parallelism and demonstrated the effectiveness of a functional language, Sisal, on dataflow architectures [28]. A modern example of applying event-driven programming to autonomous machines is the widely popular Robot Operation System (ROS), which uses the classic “publish-subscribe” model, essentially an event-driven programming interface [29].

The Problem. A key challenge in applying classic event-driven programming to autonomous machines is that they do not provide real-time and safety guarantees. In ROS, for instance, while each DFG node is annotated with an expected firing frequency, the latency of each node is unmanaged. As a result, we routinely see violations to the firing frequency. For instance, in an early mobile robot deployment, while the localization frequency was expected to be 30 FPS, the achieved frame rate was on average only 20 FPS and could vary by as much as a factor of 5 [30].

Timing violation primarily come from two sources. First, the environment in which an autonomous machine operates changes and, thus, the workload changes. Taking visual inertial odometry (VIO) for autonomous machines as an example, Fig. 2 demonstrates that the latency of VIO’s building blocks, such as Kalman filter and marginalization, strongly correlates with the visual feature points detected in the environment and exhibits a wide range of distribution [31].

Second, there are often resource contention problem when executing autonomous machine workloads on existing computing systems, leading to timing violation.

The de facto strategy in industry to meet the timing deadlines is a laborious, empirical, and case-by-case tuning of the system. For instance, to reduce timing variations due to contention, the
A last-generation computing system of our logistic robotics makes an executive call, based on the empirical observations, to assign sensing tasks to a DSP, perception tasks to the GPU, and planning and control tasks to the CPUs [32]. This empirically worked well for one generation of the software stack. When a new sensor-computing co-designed localization module and a new object detection algorithm was added to the software stack for autonomous driving applications, the original design fell apart: the GPUs are not capable of dealing with the new perception module, and the DSP is an overkill for sensing. As a result, a new mapping was again manually devised to fit the new software stack [33], this time with a powerful GPU for the perception task and an dedicated, specialized accelerator on an embedded FPGA for sensing.

This “whack-a-mole” approach is clearly unsustainable as the software stack of autonomous machine is constantly evolving: new algorithmic components emerge on a daily basis, and our software stack is updated virtually on a daily basis.

**A Potential Solution.** Providing timing-safe event-driven programming requires two components to come together. First, the hardware must provide clean behavioral specifications, describing clearly its guarantees in terms of timing. Second, the compiler and run-time systems must be able to use the specifications to reason about timing behaviors, generating timing-compatible execution policies and preventing unacceptable program runs.

First, to reason about timing behavior at the software level, we envision that each IP block in the SoC will provide a performance specification, describing things like the worst-case and average-case latency, etc. The performance of traditional general-purpose processors is notoriously hard to model; it is, however, much easier to do so for accelerators due to the simpler (e.g., shallower, software-managed memory hierarchy) and more specialized design.

In fact, we could generate accelerators with a specific timing specification in mind. For instance, the Archytas framework analyzes the basic building blocks of the localization algorithm to identify a set of key knobs, and builds an analytical latency and power model [34]. Using the model, hardware generation becomes a principled constraint optimization problem. A concrete, Pareto-optimal localization accelerator (in the form of synthesizable Verilog code) can be generated in just a few seconds (compared to months or even years if the design space is to be exhaustively searched) given a timing specification and power/energy constraints. Figure 3 shows the measured power-vs.-time of the Pareto-optimal accelerators generated by our constraint optimization (squares), which do indeed Pareto-dominate other designs (circles), suggesting the feasibility of generating accelerators with precise timing (and power) guarantees.

With the performance specifications from the accelerators, it is the function of the compiler and the run-time system to guarantee timing at the application level. The compiler could reject timing-
unsafe programs by checking the timing requirement from the programmers against the timing specifications from the IP blocks. A similar approach is a type system for constant-time cryptographic programming [35]. The compiler should also transform/generate code that guarantees overall timing. For instance, autonomous machine pipeline exhibits a "funnel-like" communication pattern, where the inter-node communication volume is increasingly smaller as the data flow progresses toward the final output. The sensing module ships about 100 MB/s of data to the perception module but the output to the vehicle is only about 5 KB/s, comprised of simple actuation commands. The compiler could leverage this pattern to allocate just enough buffer space to avoid timing violations (excessive stalls).

Alternatively, the compiler might generate code and specification that provides only an average-case guarantee, while leaving to the run-time system to adapt to the run-time dynamism to meet the worst-case requirement. For instance, the Archytas framework, along with generating an accelerator, also generates a run-time system that dynamically scales the hardware configuration (e.g., clock gating) to adapt to the workload at run time. The goal is to dynamically scale down the hardware provision when the workload decreases has little accuracy/latency impact [34].

Algorithm 1 \(\lambda\)-calculus expression of the computation graph shown in Fig. 1b.)

\[
\begin{align*}
\text{Require:} & \quad IR(frequency > 50\text{Hz}) \quad & \triangleright \text{infrared sensor} \\
\text{Require:} & \quad Camera(resolution = 320\times240; frequency > 30\text{Hz}) \\
\text{Require:} & \quad IMU(frequency > 100\text{Hz}) \\
\text{Require:} & \quad WO(frequency > 50\text{Hz}) \quad & \triangleright \text{wheel odometry sensor} \\
\text{Require:} & \quad 2DPerception(frequency > 50\text{Hz}) \\
\text{Require:} & \quad Localization(frequency > 50\text{Hz}) \\
\text{Require:} & \quad Control(frequency > 50\text{Hz}) \\
1: & \quad \text{perc} \leftarrow \lambda(IR)\lambda(Camera)\lambda(2DPerception)[2DPerception(IR, Camera)] \\
2: & \quad \text{loc} \leftarrow \lambda(Camera)\lambda(IMU)\lambda(WO)\lambda(Localization)[Localization(Camera, IMU, WO)] \\
3: & \quad \text{cmd} \leftarrow \lambda(\text{perc})\lambda(\text{loc})\lambda(Control)[Control(\text{perc}, \text{loc})]
\end{align*}
\]

With hardware providing time specifications that are satisfied by constructions and the compiler/run-time guaranteeing the timing behaviors, safe programming for autonomous machines becomes much easier. A concrete example is shown in Algorithm 1 which is a \(\lambda\)-calculus expression describing the cleaning robot computation graphs shown in Fig. 1. The first few lines of 'Require' statements specify the configurations (e.g. image resolution) and the performance specifications for each DSA, the compiler goes through these statements and ensures that these performance requirements can be met. Then the next few lines of code specify the computation graph and the compiler will allocate just enough buffer space to facilitate communications between the nodes to avoid timing violations caused by excessive stalls. Note that with this approach, complex autonomous machine applications can be expressed in simply a few lines of code using functional, event-driven programming.

5 Conclusion

The core of autonomous machines resides in their computing systems, and encompasses both the hardware and the software level, entailing algorithms, systems software, compilers, as well as computer architectures. Unfortunately, the architecture of autonomous machine computing systems still largely remains an open research question, as existing autonomous machine computing solutions are often made on an ad hoc basis, not only the development process takes a long time, and the design itself is neither scalable nor extensible. In this article, we have argued for the
promise of dataflow architectures in autonomous machines. We started by reviewing the advantages of dataflow architectures and their implementation difficulties. Then we summarized the observations of autonomous machine computing, and explained why dataflow architectures may be extremely fitting for autonomous machine computing. Based on these observations, we have proposed timing-safe dataflow architecture and programming model for autonomous machines, in which the hardware provides clean behavioral specifications to guarantee performance under different operation scenarios, and the compiler and run-time systems utilize the specifications to reason about timing behaviors, generating timing-compatible execution policies and preventing unacceptable program runs. As a next step, we will apply the Parallel Turing Machine (PTM) model [36] to autonomous machine computing, as the PTM model, along with the codelet abstract machine, provides a generic program execution and architecture model to reason about the complex interactions between modules within an autonomous machine.

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