Light turning mirrors for hybrid integration of SiON-based optical waveguides and photo-detectors

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Abstract: For hybrid integration of an optical chip with an electronic chip containing photo-diodes and processing electronics, light must be coupled from the optical to the electronic chip. This paper presents a method to fabricate quasi-total-internal-reflecting mirrors on an optical chip, placed at an angle of 45° with the chip surface, that enable 90° out-of-plane light coupling between flip-chip bonded chips. The fabrication method utilizes a metal-free, parallel process and is fully compatible with conventional fabrication of optical chips. The mirrors are created using anisotropic etching of 45° facets in a Si substrate, followed by fabrication of the optical structures. After removal of the mirror-defining Si structures by isotropic etching, the obtained interfaces between optical structure and air direct the output from optical waveguides to out-of-plane photo-detectors on the electronic chip, which is aimed to be flip-chip mounted on the optical chip. For transverse-electric (transverse-magnetic) polarization simulations predict a functional loss of 7% (15%), while 7% (18%) is measured.

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References and links

1. B. Chmielak, M. Waldow, C. Mattheisen, C. Ripperda, J. Bolten, T. Wahlbrink, M. Nagel, F. Merget, and H. Kurz, “Pockels effect based fully integrated, strained silicon electro-optic modulator,” Opt. Express 19(18), 17212–17219 (2011).
2. S. V. Pham, M. Dijkstra, A. J. F. Hollink, L. J. Kauppinen, R. M. de Ridder, M. Pollnau, P. V. Lambeck, and H. J. W. M. Hoekstra, “On-chip bulk index concentration and direct label-free protein sensing utilizing an optical grating-waveguide cavity,” Sens. Actuator B 174, 602–608 (2012).
3. B. I. Akca, L. Chang, G. Sengo, K. Wörhoff, R. M. de Ridder, and M. Pollnau, “Polarization independent enhanced-resolution arrayed waveguide grating used in spectral domain optical low coherence reflectometry,” IEEE Photon. Technol. Lett. 24, 848–850 (2012).
4. T. Suhara and H. Nishihara, “Integrated optics components and devices using periodic structures,” IEEE J. Quantum Electron. 22(6), 845–867 (1986).
5. K. Watanabe and J. Schrauwen, A. Leinse, D. Van Thourhout, R. Heideman, and R. Baets, “Total reflection mirrors fabricated on silica waveguides with focused ion beam,” Electron. Lett. 45(17), 883–884 (2009).
6. M. V. Bazylenko, M. Gross, E. Gauja, and P. L. Chu, “Fabrication of light-turning mirrors in buried-channel silica waveguides for monolithic and hybrid integration,” J. Lightwave Technol. 15(1), 148–153 (1997).
7. F. Civitci, A. Driessen, and H. J. Hoekstra, “Light turning mirrors for hybrid integration of optical waveguides in SiON technology and CMOS based photo-detectors,” in Proceedings of The European Conference on Lasers and Electro-Optics, (European Physical Society, Mulhouse, 2011), paper: C8_2.
8. F. Civitci, G. Sengo, M. Pollnau, A. Driessen, and W. Hoekstra, “Light Turning Mirrors in SiON Optical Waveguides for Hybrid Integration with CMOS Photo-detectors,” in Proceedings of the Annual Symposium of
In recent years, waveguide (WG) based integrated optical devices have been used in many applications, such as telecommunication, optical spectroscopy, biological sensing, and signal processing in medical imaging [1–3]. Usually the WG output signals are measured using photo-diodes (PDs) that may be dedicated to certain applications, such as time gating in spectroscopic research or in diagnostics. In particular, for (high-resolution) spectroscopy the photo-diodes (PDs) that may be dedicated to certain applications, such as time gating in spectroscopic research or in diagnostics. In particular, for (high-resolution) spectroscopy the signals from a large number of different channels must be measured simultaneously, which can be done most conveniently with 2D arrays of PDs. Monolithic integration of the latter to the Si substrate of an optical chip has several disadvantages: (i) the PDs and their electronic processing circuitry must be fabricated first, implying that the temperature budget to fabricate the optical structures is limited to about 400 °C, whereas higher-temperature process steps are often needed, such as low-pressure chemical vapor deposition (LPCVD) and reflow of deposited layers; (ii) fabrication of PDs and their electronic processing circuitry on each optical chip would be far more expensive than processing a CMOS chip that includes densely packed PDs and electronics which could be flip-chip mounted on an optical die due to the large area occupied by the optical chip compared to the CMOS chip.

A number of techniques have been reported to provide a connection between optical WGs and electronic PDs on two individual, flip-chip mounted chips. One of these techniques uses a focusing grating coupler on top of a WG to focus the light onto the PD that is placed above the WG [4]. However, this device can only work for a limited wavelength range, which is defined by the grating period. In addition, high-volume production of such a grating could be expensive owing to its relatively small period. Another technique uses focused ion beam (FIB) milling for fabricating total-internal-reflection (TIR) mirrors at the end of silica WGs [5]. This technique is also not suitable for high-volume production due to the relatively low speed of FIB milling and the associated high cost. A third technique is based on a metal mirror, at which the desired mirror angle is defined by use of a superficial layer in the wet etching process of the buffer layer [6]. Although the efficiency of these mirrors is very high (up to 95%), the acceptable thermal budget of the fabrication process is low, because the melting temperature of the metal layer used as the mirror is only ~650 °C. Nevertheless, to enable efficient optical coupling between an optical die and a flip-chip mounted electronic die, low-cost high-efficiency 45° out-of-plane mirrors in optical chips would be favorable.

This paper describes a method to fabricate 45° mirrors in optical chips that enable highly efficient 90° out-of-plane light coupling to a flip-chip mounted electronic chip holding 2D PD arrays with corresponding processing electronics [7–9]. The fabrication process for these mirrors is suitable for batch production and has a thermal budget of 900 °C. The mirror is...
defined by anisotropic etching of a 45° facet in the Si substrate. After WG fabrication the mirror is formed by locally removing the Si facet at the interface between the truncated optical WG and air. In the next section, the envisioned device is introduced and the mirror performance estimated by simulations. Then the fabrication process steps toward realizing the mirror are explained. Finally, the results of structural device characterization and experimental performance of the fabricated devices are presented.

2. Device design and calculated performance

This section introduces the composition and principle of the proposed device and discusses the choices related to the configuration of the device. Simulation results to estimate the mirror performance are presented.

Figure 1 displays the cross section of the 45° mirror structure. The device is composed of a single-mode SiON channel WG, which is embedded in BPSG and continues, at the mirror side of the structure, on a 45°-angled thin Si$_3$N$_4$ layer, which has an interface with air at the opposite side of the SiON layer. This thin Si$_3$N$_4$ layer prevents the exchange of molecules at the interface between the buffer layer and the Si substrate, which otherwise might cause an ill-defined Si surface. Furthermore, calculations show that, with an optimized thickness of 100 nm, it leads to a decrease of the functional loss of the mirror by about 3%, thanks to the increased refractive-index contrast between the optical structure and air. Here, functional loss is defined as the loss in reflectance due to the fact that the mirror is ideally not fully reflecting (quasi-TIR). The device can also be configured such that the WG is truncated before it reaches the mirror interface, but calculations show that the functional loss would be increased. The working principle of this device is as follows. Owing to the abrupt directional change of the WG (45°) the light carried by the SiON WG is no longer confined and is reflected upwards via the nitride layer and its interface with air, where quasi-TIR takes place. This behavior is confirmed by 2D finite-difference time-domain (FDTD) calculations.

These mirrors are designed to be used in SiON WG technology in an application [10] using a central wavelength of $\lambda_c = 850$ nm. In principle, also a ridge WG geometry can be used; however, it is not possible to use ridge WGs in combination with a BPSG buffer layer, because outgassing in the subsequent high-temperature annealing step would lead to damage to the BPSG layer if fully covered with a SiON layer.

![Fig. 1. Cross-sectional view of the proposed device.](image-url)

The WGs are designed to be single-mode at $\lambda_c$, since single modality is required by most of the potential applications. The total height ($h_1 + h_2$) of the pyramidal mirror structures is of
critical concern in the WG design: the next section explains that this height should be as small as possible to ease the fabrication process. On the other hand, there is a lower limit to the buffer-layer height ($h_1$) because of radiation losses to the substrate, which can be minimized by increasing the vertical confinement of the WG mode.

We choose the WG width to be 1 µm, which is the minimum width that can be achieved with our fabrication process. Selecting the minimum width allows for a maximum WG height which, in turn, maximizes the vertical confinement. The refractive index and thickness of the SiON layer are selected to be 1.585 and 600 nm, respectively, for achieving a single-mode WG at $\lambda_c$. The BPSG buffer height $h_1$ is set to 3.5 µm, which ensures less than $10^{-4}$ dB/cm radiation losses to the substrate, according to mode-solver calculations based on the finite-element method. This estimated loss is much smaller than propagation losses of slab SiON layers, which is 0.2 dB/cm for visible light [8]. The vertical distance between the buffer layer and uppermost point of the mirror ($h_2$) is selected to be 1.5 µm, which provides a proper overlap between WG mode and mirror surface. Consequently, the total height of the pyramids is about 5 µm.

The application of thermally grown SiO$_2$, which is normally used as a buffer material [11], would lead to deformation of the Si micro-structures. Therefore, we selected BPSG (instead of undoped SiO$_2$) as the buffer and cladding material, as it does not lead to deformation of the Si micro-structures and can be reflowed at a temperature of 900 °C for removal of as-deposited defects. This reflow is required for the removal of voids or slits which arise during plasma-enhanced chemical vapor deposition (PECVD) near elevated micro-structures [12]; it defines the thermal budget of the device.

Performance of the proposed mirrors is estimated from the somewhat simplified structure in Fig. 2(a) by calculating the field profile after reflection of the Fourier components corresponding to the channel WG mode from the SiON-SiN-air structure. The simplification consists of the assumption that the 45° angled wall is fully covered with a 600 nm thick SiON layer, i.e., it is assumed that the modal power is incident from the SiON layer onto the mirror. The resulting calculated far-field-intensity distribution for transverse-electric (TE) polarization is displayed in Fig. 2(b), indicating that the intensity profile is not symmetric along the vertical direction. This asymmetrical behavior occurs, because Fourier components corresponding to downward-travelling beams have a (slightly) different angle of incidence upon the reflecting layer than more upwardly directed beams and, hence, a lower reflection coefficient. Although most of the Fourier components undergo TIR, some of them are not totally reflected, which leads to a decrease in efficiency. The calculated functional loss of the mirror is 7% for TE polarization and 10% for transverse-magnetic (TM) polarization.

![Fig. 2. (a) Cross-section of the simplified mirror structure used in the simulation and (b) calculated intensity profile at the far field for TE polarization.](image-url)
3. Fabrication process

The wafer cross-sections after different steps in the fabrication process flow are shown in Figs. 3(a)–3(j). Each step is briefly discussed below.

a. The fabrication process starts with the growth of 200 nm thick thermal silicon oxide to be used as an anisotropic Si etching mask. Subsequently, the oxide is patterned by buffered HF (BHF) etching.

b. 5 µm \((= h_1 + h_2)\) deep anisotropic etching of the (100) Si wafer is performed by use of a solution of TMAH and Triton-x-100. When applying this etchant, the \(\{110\}\) plane is etched slower than the \(\{100\}\) plane, resulting in an etch stop at the \(\{110\}\) planes, if the edges in the oxide mask are aligned parallel to \(\{110\}\) planes [13]. The desired wall angle of \(45^\circ\) is achieved with this etch stop, because the angle between the wafer surface and \(\{110\}\) planes is \(45^\circ\). Concentration and temperature of the etchant are optimized in order to minimize the roughness of etched \(\{110\}\) surfaces. In this study, 75 ppm of Triton-x-100 is added to a 25% TMAH solution and the etching process is carried out at 80 °C. Figure 4 shows the SEM pictures of Si structures that are etched with the optimized process. As can be seen from Fig. 4(b), the etched \(\{110\}\) surfaces are not perfectly smooth. The effect of this roughness is investigated by performing an experiment in which a laser beam at 632 nm wavelength is focused onto the etched Si surface and the light reflected from this surface is compared with the light reflected from a bare Si wafer surface. The measurements show that the roughness diminishes the reflectance of the beam by the Si surface by only 4%.
c. The fabrication process is continued by removal of the thermal oxide in BHF. Then a 100 nm thick SiN layer is deposited by LPCVD.

d. Hereafter, a thick boron-phosphorous-doped silica glass (BPSG) film is grown using PECVD, to serve as the buffer layer. The thickness of this layer should be at least 5 µm, which is equal to the etch depth defined in the anisotropic Si etch step, to obtain a flat surface using a chemical-mechanical polishing (CMP) step. Since as-deposited BPSG layers grown by this method contain slits at the corners of pre-patterned layers (elevated Si structures in our case), post-deposition annealing at 900 °C during 16 hours right after deposition of the BPSG layer is required to overcome this problem.

e. The surface topology, resulting after the anisotropic Si etch step, is maintained after the BPSG deposition. To obtain a flat surface, CMP is performed after annealing the BPSG layer, because non-annealed BPSG would be attacked by the cleaning solution (RCA-2) used after the CMP process. Additional elevated Si dummy structures were processed to improve uniformity of the removal rate of this polishing process over the full wafer [14]. These dummy structures had the same dimensions as the mirrors and were distributed over the full wafer, except for the area occupied by the WGs.

f. Subsequently, the BPSG is thinned in a BHF solution, such that a 3.5 µm thick buffer layer remains between guiding SiON layer and Si substrate.

g. This step is followed by deposition and patterning of the core SiON layer which has a refractive index of 1.585.

h. Next, the cladding BPSG layer is deposited, annealed, and polished by CMP under the same process conditions as applied to the buffer BPSG.

i. Then isotropic Si etching holes are introduced on top of the elevated Si structures.

j. Finally, through these holes the isotropic Si etching is performed. In this step, gas-phase XeF$_2$ etching is used to selectively remove Si. The selectivity to Si$_3$N$_4$ and annealed BPSG layers should be high in order not to diminish the surface quality of the TIR mirrors. It is known that XeF$_2$ etching of Si$_3$N$_4$ is at least 25 times slower than that of Si [15]. Our experimental results show that XeF$_2$ etching of Si is 1500 times faster than that of annealed BPSG.

![Fig. 4. (a) SEM cross section and (b) top view of Si structures etched by the optimized Si anisotropic etchant.](image)
4. Characterization

This section discusses the structural features of the fabricated device and experimental results related to device performance.

4.1 Structural characterization

Figure 5(a) shows a SEM picture of a cross section of the wafer through one of the pyramidal structures, which is obtained by dicing the sample through the center of the elevated Si structure and then etching the sample in XeF$_2$ to remove the Si from the edge of the chip. After XeF$_2$ treatment, the part of the BPSG layer at the edge of the chip is suspended in air. The bright particles in the image are an artifact of the dicing process. The angle between the mirror and the wafer surface is measured from this figure to be 45°, as expected. Figure 5(b) displays a top-view photograph of a device that is composed of four mirrors with corresponding WGs. Circular openings in the four mirror pyramids can be identified. These pyramids are surrounded by elevated Si dummy structures. The circular features around the four mirror pyramids correspond to the area etched during the XeF$_2$ treatment. Also visible in Fig. 5(b) at the transition between the buffer BPSG and cladding BPSG is a step that is formed because of the unwanted etching (approximately 30 nm in total) of the SiN layer in two different steps of the fabrication process: (i) BHF thinning of the buffer BPSG layer (Fig. 3(f)) and (ii) SiON patterning (Fig. 3(g)). Such a transition between BPSG layers is not visible at those pyramids that are not etched in XeF$_2$, which is attributed to the insufficient image contrast in those areas. Considering the relatively low measured functional loss (see below), apparently this undesired defect hardly reduces the mirror performance. Nevertheless, the step can be avoided by modifying the fabrication process as follows: (i) TEOS oxide which does not interact with the substrate can be used instead of BPSG as the buffer layer, making the thin SiN layer between buffer layer and substrate unnecessary, thereby eliminating the unwanted etching issue in the BHF thinning step; (ii) ridge WGs can be used instead of channel WGs to prevent over-etching in the SiON patterning step.

![Fig. 5. (a) SEM cross section obtained by dicing the sample through the center of an elevated Si structure and (b) top view photograph of part of the fabricated chip showing four mirrors with corresponding WGs as well as dummy pyramids.](image)

4.2 Optical characterization

Figure 6 shows a schematic of the optical setup used for estimating the mirror performance. Laser light at a wavelength of 850 nm is coupled into a single-mode optical fiber. Light at the output of this fiber is collimated by a thin lens, polarized by a polarization beam splitter (PBS) and a λ/2-plate, and coupled to the WG by a microscope objective lens. The light propagating in the WG is reflected from the mirror, illuminates a diffusive screen 1 cm away from it, and the resulting image is captured by a camera connected to a computer. Figures 7(a) and 7(b) show the measured far-field intensity patterns of TE- and TM-polarized light,
respectively. The graphs in Figs. 7(c) and 7(d) show the calculated, measured, and ideal (corresponding to 100% reflection from an ideal mirror) curves of the irradiance, integrated over \( y \), along the \( x \)-axis for both polarizations. The graphs show that the measured intensity profile for TE polarization is narrower than the simulated one although they are similar in shape. For TM polarization, the steep intensity decrease in the left half of the calculated graph is less pronounced in the experimental curve. This discrepancy can be attributed to the simplifications made in the calculation.

![Fig. 6. Schematic of the optical setup used for measuring the mirror performance](image)

![Fig. 7. Measured far-field beam profiles for (a) TE- and (b) TM-polarized light. The graphs show the calculated, measured, and ideal irradiance integrated over \( y \), along the \( x \)-axis for (c) TE and (d) TM polarizations.](image)

Two methods are applied to measure the functional loss of the mirror. In the first method, we compare the mirror output corresponding to a specific WG with that of the same WG after
the mirror has been removed by dicing. Differences in the excitation efficiencies of the WG during the measurements with and without mirror are accounted for by monitoring the light in the same part of the WG with a camera and determining the optical power propagating in the WG. This process is repeated a number of times to correct for statistical fluctuations, resulting in a functional loss of the fabricated mirror for TE polarization of 5% with 4% RMS deviation, which agrees well with the calculated value of 7%, and for TM polarization of 4% with 4% RMS deviation, which is considerably lower than the value of 15% obtained from calculations. This discrepancy is mainly due to simplifications made in the calculations and the possible roughness at the output of the WG after dicing, which could decrease the power coupling to the detector from the WG.

In the second method, which appears to be more reliable, the functional loss is determined from the measured far-field irradiance. Figures 7(c) and 7(d) show that the right-hand sides of the calculated and ideal irradiance curves exactly overlap. This implies that the reflectance of the plane waves corresponding to the right-hand side of the calculated curves is unity. Assuming unity reflectance for the measured curves, we fit the right-hand side (plus a small fraction of the left-hand side such that $R^2$, which is defined as the ratio of the sum of squares of the regression (SSR) and the total sum of squares (SST), is maximized, see Fig. 8) of these curves to the Gaussian function

$$I = Ae^{-\frac{(x-x_c)^2}{w^2}}. \quad (1)$$

where $A$, $x_c$, and $w$ are peak value, position of the peak, and width of the Gaussian function, respectively. The used data range for fitting corresponds to the Fourier components of the far field of the beam reflected according to TIR from the mirror. Figure 8 shows the experimental and fitted curves for the irradiance, as well as the part of the experimental data used for fitting and the resulting fit. The efficiency is calculated by dividing the area below the measured curve by the area below the fitted curve. The results show that the functional loss of the fabricated mirror for TE polarization is 6.2%, while for TM polarization it is 17.8%, which agrees well with the calculated values of 7% and 15% for TE and TM polarization, respectively.

![Figure 8](image)

Fig. 8. Measured and fitted irradiance, integrated over $y$, along the $x$-axis for (a) TE and (b) TM polarization

5. Conclusions

Quasi-TIR-based 90° out-of-plane light-turning mirrors with high efficiency for hybrid flip-chip integration of SiON WGs and CMOS-based photodiodes have been fabricated by use of a newly designed technology flow. Experimental results obtained from the fabricated device
show that the experimental functional loss of the mirrors are 6.2% for TE and 17.8% for TM polarization, reasonably close to the values obtained from approximate calculations being 7% and 15%, respectively.

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