A wideband current-reuse-RGC TIA circuit with low-power consumption

Akira Hida, Yusuke Nakane, Shunta Mizuno, Makoto Nakamura, Daisuke Ito, Shinsuke Nakano, and Hideyuki Nosaka

Abstract This paper presents a new Gain-Adder (GA) circuit for Current-Reuse (CR)-RGC TIA. The proposed GA circuit employs one transistor alone to enhance bandwidth and decrease power consumption. The proposed CR-RGC TIA circuit is designed in a 65-nm CMOS technology. The simulation results confirmed that the proposed CR-RGC TIA circuit improves bandwidth by 83% and decreases the power consumption by 34% in comparison with the conventional one.

key words: transimpedance amplifier, current-reuse, regulated-cascode

Classification: Integrated circuits

1. Introduction

The increase of network traffic requires more high-speed and large-capacity communications for optical networks [1, 2]. Accordingly, data traffic in a data center is explosively growing [3, 4], and the power consumption is also increasing due to a large number of pieces of communication equipment [5, 6, 7]. In the optical communication systems, a transimpedance amplifier (TIA) [8], which converts currents of a photodiode to voltage signals and amplifies it to drive following circuits, is the most essential circuit for the frequency bandwidth of the optical receiver [9, 10, 11], but to achieve high-performance transimpedance, TIA requires large power consumption [12]. A low-power TIA is also being actively investigated [13, 14].

This paper proposes a new circuit topology for bandwidth enhancement with low-power consumption based on a current-reuse regulated-cascode (CR-RGC) TIA. The conventional CR-RGC TIA [15, 16, 17, 18] has the gain-adder (GA) circuit consisting of two inverters and a load resistor for the first stage amplifier. The proposed GA circuit is simplified with a transistor alone to reduce the power consumption without bandwidth degradation. We designed the proposed TIA in a 65-nm CMOS technology. The simulation results confirmed that the proposed circuit increases the bandwidth by 83% and decreases the power consumption by 34% in comparison with the conventional CR-RGC TIA.

2. Conventional CR-RGC TIA circuit

In the receivers of high-speed optical communication systems, a photodiode connects with the input port of the TIA [19], and the TIA converts the photocurrent signals to the voltage signals. Its frequency bandwidth is determined by the dominant pole generated by capacitors and resistances including photodiode junction and input impedance of TIAs [20]. Therefore, the bandwidth can be improved by lowering the input impedance of TIAs [21]. Consequently, a regulated-cascode (RGC) circuit [22, 23, 24, 25] is widely used for a wideband TIA because it has a low-input impedance characteristic, and various modified RGC circuits are investigated [26, 27].

For more reducing the input impedance, a CR-RGC TIA using a current-reuse (CR) technique [28] based on the RGC TIA has been proposed [16]. Figure 1 shows the circuit diagram of the conventional CR-RGC TIA. It is configured with series connected NMOS and PMOS common gate circuits and the regulated feedback path to the gate port of them. This configuration boosts the transconductance of first stage to \( g_{mN} + g_{mP} \approx 2g_m \), which is about twice in the conventional RGC TIA. Accordingly, the input impedance \( Z_{in}' \) of the CR-RGC TIA circuit is written as follows:

\[
Z_{in}' = \frac{1}{(g_{mN} + g_{mP})(1 + A)} \approx \frac{1}{2g_m(1 + A)} \tag{1}
\]

where \( A \) is the amplification of the feedback path in the RGC circuit.

On the other hand, the transimpedance gain \( Z_i(s) \) is written as,

\[
Z_i(s) = \frac{Z_0}{(1 + s/s_1)(1 + s/s_2)} \tag{2}
\]

where \( s_1 \) and \( s_2 \) are the first and second poles of the CR-RGC TIA, respectively [29]. The low-frequency transimpedance gain \( Z_0 \) is expressed as Eq. (3).

\[
Z_0 = g_mR_0R, \quad R := R_N = R_P \tag{3}
\]
where \( g_{mi} \) is a transconductance of inverters, and \( R_D \) is a load resistor. The poles \( s_1 \) and \( s_2 \) are written as follows:

\[
s_1 = \frac{1}{R_1 C_1} = \frac{1}{Z_{in} C_{in}},
\]

\[
s_2 = \frac{1}{R_2 C_2} = \frac{1}{R (C_N + C_{ins}(1 + g_{mi}R_D))},
\]

where \( C_{in} (= C_{PD} + C_{TIA}) \) is an input capacitance, \( C_{inv} (= C_{gd;N} + C_{gd;P}) \) is a gate-drain capacitance in the GA circuit, and \( C_N \) is a parasitic capacitance at the drain of the NMOS \( M_N \). In Eq. (5), \( C_{inv}(1 + g_{mi}R_D) \) is the Miller capacitance [30] as shown in Fig. 2. In the conventional circuit, the GA circuit uses two inverters which have the large gain \( g_{mi}R_D \), and it makes \( s_2 \) to close to \( s_1 \). That means the frequency bandwidth depends on not only \( s_1 \) but also \( s_2 \). Furthermore, the GA circuit requires bias circuits for the two inverters, and a through current flows by them, it causes to increase power consumption.

3. Proposed CR-RGC TIA

To overcome these problems, we propose a new CR-RGC TIA topology that can extend the frequency bandwidth with low-power consumption, as shown in Fig. 3. It employs the simple GA circuit consists of one transistor \( M_f \) alone instead of two inverters.

Figure 4 shows the operational principle of the proposed GA circuit. The current \( i_{MP} \) that is a part of the signal current \( i_M \) flows to \( R_N \), and it joins \( i_{MN} \) generated by \( M_N \). As a result, the output voltage \( v_N \) is generated by a total current of two RGC circuits. This GA circuit topology can reduce power consumption because it can prevent through current since no inverters.

Let us consider a frequency characteristic of the proposed topology. The first pole \( s_1 \) is equal to the conventional TIA as written Eq. (5). The capacitance \( C_2 \) making second pole \( s_2 \) is given by \( C_N + C_{gs} \) as shown in Fig. 5. It is confirmed that the Miller effect of the \( C_{gs} \) is smaller than the conventional one because the gain of the source follower is small. The second pole of the proposed circuit is expressed as

\[
s_2 = \frac{1}{R_2 C_2} = \frac{1}{R (C_N + C_{gs})}.
\]

Consequently, the second pole of the proposed TIA is higher than the conventional one from Eq. (5) and (6). As a result, the frequency bandwidth of the proposed TIA can be expanded.

The low-frequency transimpedance gain \( Z_t(0) \) of the proposed CR-RGC TIA is given as Eq. (7)

\[
Z'_t(0) = \frac{1}{2} \left( 1 + \frac{g_{mf}}{g_m} \right) R_s \quad R_s = R_N = R_P,
\]

here, \( g_m \) is the transconductance of \( M_N \) and \( M_P \), \( g_{mf} \) is transconductance of \( M_f \), and the gain of the source follower is assumed to be 1. It is confirmed that the gain of proposed topology decreases compared with Eq. (3). However, its influence is smaller than the expansion of frequency bandwidth, and the proposed topology has advantage regarding a gain-bandwidth (GB) product. The proposed circuit has an asymmetrical GA circuit using the transistor \( M_f \). However, the delay time of the \( M_f \) is very small and thus will almost not worsen waveforms.

4. Simulation results

The proposed CR-RGC TIA is designed in a 65-nm CMOS technology with the 1.8 V supply. Figure 6 shows the cir-
circuit configuration of the proposed CR-RGC TIA. Common-source amplifiers are employed as the local-feedback and output buffer. The buffer is connected from the output of the source follower and boosts the transimpedance gain to arrange the total gain of the proposed TIA in the previous one for the comparison of specifications.

The simulated results of frequency responses for the conventional and proposed TIAs are shown in Fig. 7. The frequency bandwidth $f_{-3\text{dB}}$ and the transimpedance gain $Z_{t0}$ of our circuit are 10.3 GHz and 65.8 dBΩ, respectively. In comparison with the conventional TIA, the bandwidth of the proposed TIA improves by 83% with the same $Z_{t0}$ condition.

Figure 8 shows the GB products and power consumptions for various load resistances $R_{N, P}$. When the load resistances $R (=R_N = R_P)$ increase, the GB products of both circuits become large. The GB products of the conventional circuit are saturated over the load resistance 500 Ω. In the proposed circuit, in contrast to the previous one, it grows over 500 Ω because the second pole locates at a more higher-frequency than the conventional circuit. If we use large load resistances, the electrical currents of $M_{N, P}$ become small, therefore the bias currents of the GA circuits play a dominant role in TIAs. As mentioned earlier, the bias current of the proposed GA circuit is smaller than the conventional one. As a result, the power consumption of the proposed circuit becomes small.

Figure 9 shows the eye diagrams with 10 Gbit/s data rate in the conventional and proposed CR-RGC TIA circuits, where $T_r$ and $T_f$ are a rise and fall time from 10% to 90% of the amplitude. Note that, the amplitudes of them are almost the same; however the offset voltage of the proposed circuit is higher than the conventional one because they have different output stages. These results confirm that $T_r$ and $T_f$ are about 29 picoseconds shorter, and that the eye-opening is clear than the conventional TIA. These results reflect the bandwidth enhancement of the proposed circuit.

Table I summarizes the performance of the proposed and
conventional circuits. The figure-of-merit (FOM) is defined as the GB product per power consumption. This table confirms that the FOM value of the proposed circuit was larger than the conventional one. It means wide-bandwidth and low-power consumption.

| Table I. Performance summary and comparison. |
|---------------------------------------------|
| Power (mW) | Proposal | Conventional |
| 4.34       | 6.52     |               |
| Gain (dB)  | 65.8     | 65.6          |
| $f_{3dB}$ (GHz) | 10.3 | 5.6          |
| FOM (Ω · GHz/mW) | 4,628 | 1,636         |

* simulated results

In optical communication systems, a photodiode which has a large stray capacitance is connected to the input port of the TIA, hence the dominant pole locates at the input port. The influence of the pole associated with a layout is smaller than the dominant pole, therefore we seem that the proposed circuit can achieve the good performance to the conventional one even on a circuit experiment.

5. Conclusion

We proposed a new circuit topology for bandwidth enhancement with low-power consumption based on a CR-RGC TIA. The simple GA circuit that has one transistor alone instead of two inverters enables to lower the power consumption without degradation of bandwidth. The proposed CR-RGC TIA was designed with a 65-nm CMOS technology and simulated. The simulated results confirmed that the proposed circuit technique enables to improve bandwidth by 83% and to decrease the power consumption by 34% in comparison with the conventional one. It will contribute to low-power consumption and high-speed optical interconnection systems.

References

[1] Cisco, “Visual Networking Index: Forecast and Trends, 2017–2022 White Pap,” (2018).
[2] Cisco, “Global Cloud Index: Forecast and Methodology, 2016–2021,” (2018).
[3] Richard L. Sawyer, “Calculating Total Power Requirements for Data Centers,” APC white paper, 3, 1, (2011).
[4] Y. Takahashi et al., “Separating Predictable and Unpredictable Flows via Dynamic Flow Mining for Effective Traffic Engineering,” IEICE Trans. Commun., E101B, 2 (2017), 538–547.
[5] J. G. Koomen, “Worldwide electricity used in data centers,” Environ. Res. Lett., 3, 3 (2008), 3408.
[6] M. Averinou, P. Bertoldi, and L. Castellazzi, “Trends in Data Centre Energy Consumption under the European Code of Conduct for Data Centre Energy Efficiency,” Energies, 10, 10 (2017).
[7] Wayne M. Adams, “Power consumption in data centers is a global problem,” Data Centre Dynamics Ltd., (2018).
[8] M. H. Taghavi, L. Belostotski, and J. W. Haslett, “A bandwidth enhancement technique for CMOS TIAs driven by large photodiodes,” in 10th IEEE International NEWCAS Conference (2012), 433–436.
[9] S. Huang, W. Chen, Y. Chang, and Y. Huang, “A 10-Gb/s OEIC with Meshed Spatially-Modulated Photo Detector in 0.18-μm CMOS Technology,” IEEE J. Solid-State Circuits, 46, 5 (2011), 1158–1169.
[10] T. Takemoto, H. Yamashita, T. Yazaki, N. Chujo, Y. Lee, and Y. Matsuoka, “A 25–to-28 Gb/s High-Sensitivity (∼9.7 dBm) 65 nm CMOS Optical Receiver for Board-to-Board Interconnects,” IEEE J. Solid-State Circuits, 49, 10 (2014), 2259–2276.
[11] S. Ray and M. M. Hella, “A 53 dB 7-GHz Inductorless Transimpedance Amplifier and a 1-THz+ GBP Limiting Amplifier in 0.13-μm CMOS,” IEEE Trans. Circuits Syst. I Regul. Pap., 65, 8 (2018), 2365–2377.
[12] Saeedi, and A. Emami, “A 250Gb/s 170-pW/Gb/s optical receiver in 28nm CMOS for chip-to-chip optical communication,” in 2014 IEEE Radio Frequency Integrated Circuits Symposium (2014), 283–286.
[13] C. Li and S. Palermo, “A Low-Power 26-GHz Transformer-Based Regulated Cascade SiGe BiCMOS Transimpedance Amplifier,” IEEE J. Solid-State Circuits, 48, 5 (2013), 1264–1275.
[14] A. M. Z. Khaki, M. Omooni, and E. Borzabadi, “An ultra-low-power TIA plus limiting amplifier in 90nm CMOS technology for 2.5 Gb/s optical receiver,” 24th Iran. Conf. Electr. Eng. (2016), 1055–1059.
[15] A. H. M. Shirazi, and S. Mirabbsi, “An ultra-low-voltage ultra-low-power CMOS active mixer,” Analog Integr. Circuits Signal Process., 77, 3 (2013), 513–528.
[16] A. H. M. Shirazi, et al., “A Low-Power DC-to-27-GHz Transimpedance Amplifier in 0.13 μm CMOS Using Inductive-Peaking and Current-Reuse Techniques,” IEEE MWSCAS (2014), 961 (DOI: 10.1109/MWSCAS.2014.6908576).
[17] D. Abdi-Ebrahim, M. Atef, M. Abbas, and M. Abdelgawad, “Current-reuse transimpedance amplifier with active inductor,” ISSCS 2015, Int. Symp. Signals, Circuits Syst. (2015), 1–4.
[18] R. Costanzo and S. M. Bowers, “A Current Reuse Regulated Cascode CMOS Transimpedance Amplifier With 11-GHz Bandwidth,” IEEE Microw. Wirel. Components Lett., 28, 9 (2018), 816–818.
[19] B. Razavi, “Design of Integrated Circuits for Optical Communications,” (Wiley, 2012).
[20] C. Li and S. Palermo, “A Low-Power 26-GHz Transformer-Based Regulated Cascade SiGe BiCMOS Transimpedance Amplifier,” IEEE J. Solid-State Circuits 48 (2013), 1264 (DOI: 10.1109/JSSC.2013.2245059).
[21] R. G. Meyer and R. A. Blauschild, “A wide-band low-noise monolithic transimpedance amplifier,” IEEE J. Solid-State Circuits, 21, 4 (1986), 530–533.
[22] S. M. Park and H. Jun, “1.25-Gb/s Regulated Cascode CMOS Transimpedance Amplifier for Gigabit Ethernet Applications,” IEEE J. Solid-State Circuits 39 (2004), 112 (DOI: 10.1109/JSSC.2003.820884).
[23] S. M. Park, et al., “1-Gb/s 80-dBΩ Fully Differential CMOS Transimpedance Amplifier in Multichip on Oxide Technology for Optical Interconnects,” IEEE J. Solid-State Circuits 39 (2004), 971 (DOI: 10.1109/JSSC.2004.827795).
[24] Z. Lu, et al., “Broad-Band Design Techniques for Transimpedance Amplifiers,” IEEE Trans. Circuits Syst. I 54 (2007), 590 (DOI: 10.1109/TCSI.2006.887610).
[25] X. Hui, et al., “A 3.125-Gb/s inductorless transimpedance amplifier for optical communication in 0.35 μm CMOS,” J. Semiconductors 32 (2011), 105003 (DOI: 10.1088/1674-4926/32/10/105003).
[26] S. Bashiri, et al., “A 40 Gb/s transimpedence amplifier in 65 nm CMOS,” IEEE ISSCAS (2010), 757 (DOI: 10.1109/ISSCAS.2010.5537465).
[27] D. Li, et al.: “A 25Gb/s 3D-integrated silicon photonics receiver in 65nm CMOS and PIC25G for 100 GbE optical links,” IEEE ISCAS (2016), 2334 (DOI: 10.1109/ISCAS.2016.7539052).

[28] N. Kim, et al.: “A Resistively Degenerated Wide-Band Passive Mixer with Low Noise Figure and +60dBm IIP2 in 0.18 µm CMOS,” IEEE RFIC (2008), 185 (DOI: 10.1109/RFIC.2008.4561414).

[29] B. Razavi: Design of Analog CMOS Integrated Circuits (McGraw, New York, 2001).

[30] John M. Miller, “Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit,” Scientific Papers of the Bureau of Standards, 15, 351 (1920), 367–385.