Improved Space Vector Modulation for Neutral-Point Balancing Control in Hybrid-Switch-Based T-Type Neutral-Point-Clamped Inverters With Loss and Common-Mode Voltage Reduction

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Abstract—This paper compares different space vector modulation (SVM) strategies for neutral-point voltage balancing (NPVB) control in three-level (3-L) T-type neutral-point-clamped (TNPC) inverters, and proposes an improved SVM trimmed for NPVB control in hybrid-switch-based 3-L TNPC inverter with the features of loss and common-mode voltage (CMV) reduction. The proposed SVM strategy uses a new principle of small vector selection and vector sequence, and thus, it can balance the neutral point (NP) potential and achieve soft-switching of clamping leg simultaneously. The paper includes detailed analysis for circuit commutation mode, loss breakdown, and common-mode voltage patterns under different operation conditions. The circuit simulations and experiments are carried out in the last part of this paper to validate the proposed SVM strategy.

Index Terms—Electromagnetic interference (EMI), neutral-point (NP) voltage balance, Si-SiC hybrid switch, space vector modulation (SVM), T-type neutral-point-clamped (TNPC) inverter, wide bandgap (WBG) devices.

I. INTRODUCTION

THREE-LEVEL T-type neutral-point-clamped (3-L TNPC) inverter has higher efficiency and lower total harmonic distortion (THD) compared to two-level inverter, and it has become popular in high-speed motor drives and all-electric aircraft applications [1]–[5]. Emerging silicon carbide (SiC) MOSFET has lower losses and high switching speed compared to Si IGBT and enables higher efficiency and power density in power converters [6]–[11]. SiC MOSFET is becoming a major competitor and replacement for Si IGBT in power electronics systems.

However, the state-of-the-art die size limit and the high cost of SiC MOSFET are the bottlenecks for its high-current commercial applications. Therefore, [13] proposed a hybrid switch concept, as shown in Fig. 1. By adjusting the switching sequence of the two switches, the T-type inverter with the hybrid switch (hybrid structure 1) [14]–[16], which is shown in Fig. 2, can have low switching loss from SiC MOSFET switching, and low conduction loss from IGBT conduction. However, due to the long discharging time of the carriers inside the IGBT, the Si-SiC hybrid switch operation mode have a minimum duty cycle limitation [17], which deteriorates the output total harmonic distortion performance. Furthermore, the hybrid-switch-based 3-L TNPC increases the system complexity in terms of the gate driver and power loop design [18]–[20]. Because of more paralleled semiconductors, more gate drivers and more gating signals are required. [12] mentioned that the Si-SiC hybrid switch structure should ensure the safe operation area (SOA) of the SiC MOSFET. Table I illustrates the current dependent operation in [12].

To reduce the system complexity as well as improve the output THD performance, M1, M4, Q2, Q3, D2, and D3 in hybrid structure 1 are selected to operate, and the new structure is shown in Fig. 3 [21]. The hybrid structure 2 utilizes Si IGBT and SiC Schottky diode as clamping leg switches and SiC

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Fig. 1. Structure of the hybrid switch.
Table I
CURRENT DEPENDENT OPERATION OF THE HYBRID-SWITCH-BASED INVERTER [12]

| Condition                                      | Operation                                      |
|------------------------------------------------|------------------------------------------------|
| SiC MOSFET voltage drop is lower than Si IGBT threshold | Only SiC MOSFET is turned on                   |
| Load current is within SOA of SiC MOSFET        | Hybrid switch operation                        |
| Load current exceed SOA of SiC MOSFET           | Only IGBT is turned on                         |

Fig. 2. T-type inverter with hybrid switch structure 1 [13].

Fig. 3. T-type inverter with hybrid switch structure 2 [21].

MOSFET for half-bridge switch positions. With SPWM, the clamping switches are soft-switching under the unity power factor, and thus, the utilization of Si IGBTs does not increase the switching loss. Therefore, the total semiconductor cost of this hybrid switch combination 3-L TNPC is lower than that of the all-SiC 3-L TNPC inverter. While the cost is low, the efficiency is higher than that of the all-SiC 3-L TNPC inverter.

Although hybrid structure 2 possesses the merits of low complexity and high efficiency, it has not been fully validated in the 3-phase 3-L TNPC system yet. One of the main challenges is to design a proper space vector modulation (SVM) scheme, which needs to consider the soft switching feature of the clamping leg, neutral point balancing (NPB) [22]-[25] and the common-mode voltage (CMV) performance. This paper provides a criterion to choose the appropriate SVM for T-type inverter with hybrid structure 2 under different conditions. Firstly, this paper obtains the switching energy of T-type inverter with hybrid structure 2 by experimental double pulse test (DPT) result, then 3 different SVM schemes are discussed in terms of switching loss, NPB, and output CMV voltage performance.

The organization of the paper is as follows. Section II summarizes the soft-switching conditions for 3-L TNPC with hybrid structure 2, then loss analysis, neutral point balancing capability and common-mode noise voltage comparison of 3 different SVM schemes are discussed. In Section III, a 20 kVA hardware is built, the DPT is firstly performed to obtain exact switching loss, and followed by the analysis and comparison of semiconductor loss breakdown, EMI spectrum and neutral point voltage ripple for three SVMs. Section IV presents the conclusion of the preferred modulation scheme.

II. ANALYSIS OF DIFFERENT MODULATION ON HYBRID SWITCH BASED 3-PHASE 3-L TNPC

For switching loss reduction [21] and NPB [22]-[25] in 3 phase 3-L TNPC inverter with hybrid switch combination, SVM 1 with NPB [23], SVM 2 with NPB [24], and improved SVM 2 with NPB are compared, and 1st sector of the space vector modulation hexagon is given as an example. The nearest three space vector (NTSV) [26] and discontinuous pulse width modulation (DPWM) [27] are adopted to track the reference vector and further reduce the switching loss.

In this chapter, switching loss and soft-switching condition of clamping leg is discussed first in 3-L TNPC with the hybrid switch combination. Then three different SVM schemes are compared in terms of switching losses, neutral point balancing capability, and CMV performance, which gives guidance for hardware design and PWM modulation choice.

A. Preferred Switch Pairs in Terms of Switching Loss Reduction

Since switching loss of Si IGBT is much higher than SiC MOSFET, hard switching of Si IGBT on clamping leg in 3-L TNPC inverter with hybrid switch combination should be avoided or minimized. As shown in Fig. 4(a), when the phase current is positive, and the phase output voltage is transitioning from positive to neutral, $T_1$ is hard switching off, and then $T_2$ and $D_3$ are soft switched on. From Fig. 4(b) we can know that when phase current is positive, and the phase output voltage is transitioning from neutral to positive, clamping leg devices are soft switched off, and $T_3$ is hard switched on. Moreover, when the phase current is negative, and phase output is transitioning from neutral to positive, $T_2$ is hard switching off, and then $T_3$ is hard switched on and hard switched off.

In summary, when phase current is positive, switch pair 1...
Different switching transitions when the phase output is positive or neutral. (a) Switch transition 1 (positive phase current), (b) Switch transition 2 (positive phase current), (c) Switch transition 3 (negative phase current), (d) Switch transition 4 (negative phase current).

and 0 is preferred since the clamping leg is soft-switching, as shown in Fig. 4(a) and (b). Switch pair 0 and −1 should be avoided since clamping leg switch \( T_2 \) is hard switching. Symmetrically when phase current is negative, switch pair 0 and −1 is preferred to obtain the soft-switching character of clamping leg and switch pair 1 and 0 should be avoided or minimized to reduce the switching loss of Si IGBT, as shown in Fig. 4(c) and (d). Based on the aforementioned analysis, different SVMs can be compared in terms of switching loss, more detailed information will be given in the later section.

**B. Common-Mode Voltage of 3-L TNPC Inverter**

Assuming that only heatsink is grounded, the equivalent model of 3 phase 3-L TNPC [28]–[33] is drawn in Fig. 5, with the consideration of all the semiconductor’s junction to heatsink and output to ground capacitance. Also, a simplified model is given in Fig. 6, which indicates that the CMV noise can be modeled through (1).

\[
V_{CM} = \left( V_{AO} + V_{BO} + V_{CO} \right) / 3
\]

**C. Switching Loss Reduction, NPB and CM Voltage Analysis for Different SVM Schemes**

Firstly, space vectors of sector 1 are marked out in Fig. 7 and small vectors’ influence on neutral point potential are stated in Table III. For simplicity, the regions 3 and 2 are analyzed and compared for three kinds of SVM schemes, choices of small vectors and alignment in the regions 1 and 4 are similar to the
SVM schemes can get.

Fig. 5. Three-phase 3-L TNPC model with the parasitic capacitor.

| CMV of Space Vectors |
|-----------------------|
| Space vector | $V_1$ | $V_2$ | $V_3$ | $V_4$ |
| CMV | $-1/3V_{dc}$ | $-1/6V_{dc}$ | 0 | $1/6V_{dc}$ |

| Small Vector’s Influence on NP Potential |
|------------------------------------------|
| Small Vector Angle | Discharge NP | Charge NP |
|---------------------|--------------|-----------|
| $0^\circ$ | $V_4$ | $V_1$ |
| $60^\circ$ | $V_5$ | $V_2$ |

| SVM | $V_{s3}$ | $V_{s2}$ | $V_{s1}$ | $V_{s4}$ | $V_{s5}$ | $V_{s6}$ |
|-----|----------|----------|----------|----------|----------|----------|
| SVM 1 | $V_3$ | $V_2$ | $V_1$ | $V_4$ | $V_5$ | $V_6$ |
| SVM 2 & $0^\circ$ to $30^\circ$ | $V_3$ | $V_2$ | $V_1$ | $V_4$ | $V_5$ | $V_6$ |
| SVM 2 & $30^\circ$ to $60^\circ$ | $V_4$ | $V_5$ | $V_6$ | $V_3$ | $V_2$ | $V_1$ |
| Improved SVM 2 & $I_b < 0$ | $V_4$ | $V_5$ | $V_6$ | $V_3$ | $V_2$ | $V_1$ |
| Improved SVM 2 & $I_b > 0$ | $V_4$ | $V_5$ | $V_6$ | $V_3$ | $V_2$ | $V_1$ |

1) The Region 3 of Sector 1

The space vector choice and alignment for SVM 1, SVM 2, and improved SVM 2 are shown in Table IV. For SVM 1 scheme, both of the small vectors $V_1$ and $V_2$ are used for balancing the neutral point potential, and B phase switching state changes between 1 and 0 plus 0 and $-1$. Since SVM 1 does not consider the B phase current direction, B phase has hard switching operations on the clamping leg. For SVM 2 scheme, the region 3 is divided into the region 3.1 and the region 3.2 according to B phase voltage polarity. In the region 3.1, only $V_1$ and $V_4$ small vectors are used for balancing the neutral point potential. In the region 3.2, only $V_2$ and $V_4$ small vectors are used for balancing the neutral point potential. B phase clamping leg is always soft-switching under unity PF. Improved SVM 2 scheme is proposed to reduce the switching loss under the wider power factor range. When the B phase current is negative, $V_1$ and $V_4$ small vectors are used for balancing the neutral point potential. $V_1$ and $V_4$ small vectors are used when the B phase current is positive. Improved SVM 2 scheme is basically the same as SVM 2 scheme under the unity power factor, and since it considers the phase current direction for choosing the small vector, and thus, it has lower losses on clamping leg under the non-unity power factor case.

2) The Region 2 of Sector 1

For region 2, modulation strategies of SVM 1, SVM 2, and improved SVM 2 are the same, which is shown in Table V.
TABLE V
SPACE VECTOR CHOICE AND ALIGNMENT IN SECTOR 2

| The region 2 of Sector 1 | Discharge NP | Charge NP |
|--------------------------|--------------|-----------|
| SVM 1 \( V_1, V_6, V_1, V_6, V_1 \) | \( V_6, V_3, V_4, V_5 \) |
| SVM 2 \( V_1, V_6, V_1, V_6, V_1 \) | \( V_6, V_3, V_4, V_5 \) |
| Improved SVM 2 \( V_1, V_6, V_1, V_6, V_1 \) | \( V_6, V_3, V_4, V_5 \) |

TABLE VI
DEVICE PARAMETERS

| Device | Voltage (V) | Current (A) |
|--------|-------------|-------------|
| SiC MOSFET (Wolfspeed-C3M0075120K) | 1200 | 30 |
| Si IGBT (ROHM-RGCL60T502D) | 600 | 30 |
| SiC Schottky diode (Wolfspeed-C3M0075120K) | 650 | 20 |

\( V_1 \) and \( V_4 \) are chosen to discharge and charge the neutral point voltage, and alignments are \( V_1, V_4, V_4, V_1 \) and \( V_1, V_4, V_4, V_1 \) when the neutral point voltage is lower and higher than half of the DC-link voltage. Soft switching can be achieved on the clamping leg of B phase under the unity power factor.

3) Summary of Different SVM Schemes

In general, the improved SVM 2 scheme has the lowest switching loss on clamping leg. Moreover, under the non-unity power factor condition, SVM 1 has better neutral point balancing ability than SVM 2 and improved SVM 2. According to Table II, \( V_1 \) and \( V_4 \) have the highest CM voltage. Since SVM 2 and improved SVM 2 exclude \( V_1 \) or \( V_4 \) for reducing the switching loss, and SVM 1 employs both of the \( V_1 \) and \( V_4 \) for NPB, SVM 2 and improved SVM 2 have relatively lower CMV than that of SVM 1.

III. EXPERIMENTAL TEST AND LOSS BREAKDOWN

A 6 kVA 3-phase 3-L TNPC prototype is built to evaluate the efficiency and CM voltage noise spectrum with different SVM, upper and lower DC-link capacitors are 150 \( \mu \)F each. As shown in Table VI, we have chosen 1200 V/30 A SiC MOSFET, C3M0075120K from Wolfspeed, and 600 V/30 A Si-IGBT IKZ50N65EH5 from ROHM, and FFS1665A SiC Schottky diode, for experiment validation. Top leg and bottom leg switches are rated for 1.2 kV, and DC-link voltage is set to be 800 V to remain some safety margin. Output RMS voltage is set to 208 V to meet one of the grid standards. Switching frequency is set to be 70 kHz to reduce the passive components’ volume. The prototype is composed of three 2kVA single-phase 3-L TNPC, as shown in Fig. 8.

A. Switching Energy Evaluation of the Three-Level Inverter

Switching energy calculation based on the devices’ voltage and devices’ current waveform is comprehensively evaluated in [34]–[36]. DPT is firstly performed to obtain the switching transitions of both SiC MOSFET and IGBT devices. As mentioned in [37], switching energy in 3-L phase leg is different from 2L half-bridge due to the device’s junction capacitance, so the double pulse test in this paper is performed based on the single-phase 3-L TNPC platform. In this way, loss analysis using switching energy data from the double pulse test on the 3-L TNPC platform gives more accurate results. The accurate switching energy information for SiC MOSFETs and Si IGBT switch is shown in Fig. 9.

B. Semiconductor Loss Breakdown and EMI Performance Evaluation

Switching energy from DPT and device conduction performance in the component datasheet are used, and a detailed semiconductor loss breakdown can be obtained in simulation. While the total power level is 6 kVA, and the switching frequency is 70 kHz.

For the near unity PF case, the loss breakdown for different modulation schemes is listed in Fig. 10(a), and total semiconductor loss using SVM 1, SVM 2, and improved SVM 2 are respectively 17.1 W, 16 W, and 16 W. As shown in the diagram, under the unity power factor case, total loss of the SVM 2 and the improved SVM 2 are 6.4% lower than using SVM 1. All of the SVMs have the same neutral point voltage ripple, which is around 2 V due to the hysteresis control algorithm at half of the switching frequency and switching actions at switching frequency.

However, for PF = 0.8 (lead or lag) case, loss breakdown for different modulation schemes are listed in Fig. 10(c), and total semiconductor loss using SVM 1, SVM 2 and improved SVM 2 are respectively 22.7 W, 18.9 W, and 17.9 W. It can be seen that by adopting SVM 1, clamping leg devices have excessive switching loss. In this condition, SVM 2 and improved SVM 2 have respectively 4.2 times and 5.3 times lower clamping leg devices’ switching loss than that of SVM 1. Neutral point ripple voltage using SVM 1, SVM 2, and improved SVM 2 are respectively 2.3 V, 8.5 V, and 15 V.
The difference of SVM schemes is the switching transitions and soft-switching conditions of the clamping leg switches under different conditions, the average duty ratio for each switch does not change a lot for different SVM schemes. So even the conduction loss of different modulations have some difference, this difference in conduction loss is not as much as...
in switching loss, and its not obvious in the figures.

In summary, with the power factor decreasing from 1 to 0.7, SVM 1 has a much higher loss on clamping leg devices than SVM 2 and improved SVM 2, which may result in device overheat issue. And it can be seen in Fig. 10 that under different power factor cases, SVM 2 and improved SVM 2 have more equal loss distribution among switching devices, so SVM 2 and improved SVM 2 are preferred in terms of semiconductor loss reduction and the semiconductor loss distribution point of view.

The neutral point voltage ripple versus power factor relationship is shown in Fig. 11. We can know that when the power factor is in the region of 0.85 to 1 (lead or lag), the SVM 1 and improved SVM 2 have higher neutral point voltage than SVM 2. When the power factor is high enough, SVM 2 also has as good clamping leg loss reduction capability as improved SVM 2. So when the power factor is between 0.85 and 1, it is better to use the SVM 2 modulation scheme for both clamping leg loss reduction as well as NPB purpose.

When the power factor is in the region of 0.7 to 0.85 (lead or lag), the SVM 1 still possesses the best NPB capability, and in the meantime, the improved SVM 2 has better NPB performance than the SVM 2. Moreover, when the power factor is relatively lower, improved SVM 2 has better clamping leg loss reduction capability than the SVM 2. When the power factor is between 0.85 and 1, the improved SVM 2 serves better for both clamping leg loss reduction and NPB purpose.

As shown in Fig. 12, comparison is made for evaluating the trade-off between NPB and loss performance using the improved SVM 2. Hysteresis width for neutral point balancing algorithm is controlled for obtaining different neutral point voltage ripple. It can be seen from Fig. 12 that, when neutral point ripple is increasing within a certain range, the total loss is decreasing due to less number of changing space vector alignment actions. However, when neutral point voltage ripple increases, the commutation voltage of the device is higher due to the unbalanced neutral point, which deteriorates the loss performance. It is recommended that the hysteresis width should be kept within 30 V for a neutral point balancing control algorithm.

MATLAB simulation has been conducted to compare EMI performance of different SVM schemes. In this simulation, $V_{out}$ represents the output phase voltage switching waveform, $I_{ph}$ represents the phase current, $V_{np}$ is the NP voltage, and $V_{cm}$ shows the common-mode voltage. As shown in Fig. 13, when PF = 0.8, SVM 1 has a higher CM voltage ripple than SVM 2, and improved SVM 2. Under PF = 1 and PF = 0.8 cases, CM voltage and phase leg output voltage spectrum are shown in Fig. 14. As shown in Fig. 14(a) and (c), from 10 to 100 kHz range which is of great significance in EMI filter design, SVM 2 and improved SVM 2 have lower CM noise than SVM 1, especially at relatively low power factor case. It is shown in Fig. 14(b) and (d), since SVM 2, and improved SVM 2 have higher neutral point unbalanced voltage under non-unity power factor, their phase leg voltage has slightly larger harmonics (300 Hz, 420 Hz, etc.) than SVM 1. In terms of common-mode filter and output filter design, SVM 2 and improved SVM 2 are preferred due to their lower better common-mode voltage harmonics as well as comparable phase output voltage spectrum.

In summary, SVM 2 and improved SVM 2 have better performance regarding semiconductor loss and common-mode voltage reduction than SVM 1, but SVM 1 has the best neutral point balancing capability. When the power factor is between 0.85 and 1, SVM 2 is adopted for better overall performance.
Fig. 13. Phase leg output voltage, phase current, NP voltage, and CM voltage waveform when PF = 0.8. (a) Waveform for the SVM 1. (b) Waveform for the SVM 2. (c) Waveform for improved SVM 2.

Fig. 14. CMV and phase voltage spectrum at different power factors. (a) CMV when PF = 1. (b) Phase voltage spectrum when PF = 1. (c) CMV when PF = 0.8. (d) Phase voltage spectrum when PF = 0.8.
and when the power factor is between 0.7 to 0.85, improved SVM 2 can be utilized for its’ overall better loss reduction as well as neutral point balancing performance.

IV. CONCLUSION

In this paper, semiconductor losses of different commutation loops in hybrid switch combination TNPC are analyzed and compared. Based on different switching loss of commutation loops, SVM 1 and SVM 2 themes are utilized and compared in this topology comprehensively in terms of their influences on switching loss, NPB and EMI spectrum, and then improved SVM 2 is proposed to further push the converter to higher efficiency at relatively low power factor.

Comparing to SVM 1, SVM 2, and improved SVM 2 schemes have better loss performance and CM noise performance, while improved SVM 2 scheme has the lowest power loss and lowest CM noise. As for neutral point balancing capability, SVM 1 is better than SVM 2 and improved SVM 2 under non-unity power factor, and their neutral point balancing capabilities are the same under the unity power factor.

Hybrid-switch-based 3 phase 3-L TNPC is comprehensively studied in this paper, and it gives guidance for hybrid switch topology design consideration and the choice of SVM strategy.

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