Auto-Generation of Pipelined Hardware Designs for Polar Encoder

Zhiwei Zhong\textsuperscript{1,2}, Xiaohu You\textsuperscript{2}, and Chuan Zhang\textsuperscript{1,2,*}

\textsuperscript{1}Lab of Efficient Architectures for Digital-communication and Signal-processing (LEADS)
\textsuperscript{2}National Mobile Communications Research Laboratory, Southeast University, Nanjing, China
Email: \{zwzhong, xhyu, chzhang\}@seu.edu.cn

Abstract—This paper presents a general framework for automatic generation of pipelined polar encoder architectures. The proposed framework could be well represented by a general formula. Given arbitrary code length $N$ and the level of parallelism $M$, the formula could specify the corresponding hardware architecture. We have written a compiler which could read the formula and then automatically generate its register-transfer level (RTL) description suitable for FPGA or ASIC implementation. With this hardware generation system, one could explore the design space and make a trade-off between cost and performance. Our experimental results have demonstrated the efficiency of this auto-generator for polar encoder architectures.

Index Terms—Polar encoder, pipelined architecture, hardware auto-generation, high-level synthesis.

I. INTRODUCTION

Polar code [1], the first channel code which can provably achieve the capacity of the binary-input discrete memoryless channels (BDMCs), has been considered as the recent breakthrough of coding theory. Recently, polar code has been adopted by the enhanced mobile broadband (eMBB) control channels for the 5G NR interface. As pointed out by [1], to achieve a good error-correcting performance of polar code, the code length is expected to be sufficiently long. However, as for polar code, the hardware complexity of fully parallel encoder will be high as the code length increases. Therefore, pipelined architecture should be introduced to reduce the hardware cost. Using folding transformation [2], [3] has proposed both feed-forward and feed-back polar encoder with 2-parallel processing; [4] has proposed pipelined polar encoder architecture with 4-parallel processing. Although [4] has claimed that the folding transformation could derive polar encoder with any level of parallelism, the detailed framework is not given.

In synthesizing hardware architectures for an $N$-bit polar encoder, different level of parallelism leads to different latency, throughput, silicon area and memory cost. Intuitively, the level of parallelism $M$ suitable for an $N$-bit polar encoder should be $2 \leq M \leq N/2$, where $M$ is a power of two. Thus, as the code length increases, there will be more choices of $M$ and the design space will be wider. Therefore, it will be exhausting to choose the optimal values of $N$ and $M$ under different hardware constraints.

In order to fulfill the requirements of different applications, a auto-generator which can conveniently output polar encoder architecture with given code length $N$ and parallelism $M$ is highly expected. Also, this auto-generator can free the hardware designers from the laborious case designs, bypass the hardware details, and give the design space in a more convenient way. Inspired by a fast Fourier transform (FFT) generator [5] which could automatically generate FFT hardware architecture with arbitrary parallelism and figure out hardware cost, this paper proposes an auto-generation system which could produce polar encoder hardware architecture with arbitrary code length and arbitrary level of parallelism.

The remainder of this paper is organized as follows. In Section III the brief description of polar encoding is introduced. In Section IV we propose the generation system of polar encoder and an exemplary 32-bit polar encoder with 8-parallel processing. In Section V the analysis of the performance of the generation system is given. In Section VI we conclude and remark on the entire paper.

II. PRELIMINARIES

A. Polar Encoder

In polar code encoding, $u_0^{N-1}$ is regarded as the source word and $x_0^{N-1}$ as the codeword. The encoding scheme can be defined by Eq. (1), where $G_N$ and $B_N$ are the generation matrix and the bit-reversal permutation matrix respectively, and $F^{\otimes n}$ is the Kronecker power of $n$ with $n = \log_2 N$ and $F = \begin{bmatrix} 1 & 0 \end{bmatrix}$.

\begin{equation}
x_0^{N-1} = u_0^{N-1}G_N = u_0^{N-1}B_NF^{\otimes n}.
\end{equation}

As proved by [6], the data-flow graph (DFG) of polar encoder could be derived from the DFG of FFT processors by replacing all the butterfly modules with XOR-and-PASS modules, and all the twiddle factors with 1’s. Therefore, the proposed framework for polar encoder has the potential for implementing the pipelined hardware architecture for FFT by reversing the replacement. An exemplary DFG of an 8-bit polar encoder is shown in Fig. 1. Note that this DFG is similar to the that of an 8-point radix-2 decimation-in-frequency (DIF) FFT processor in the way mentioned above.

III. HARDWARE GENERATION

In this section, we introduce the general pipelined framework for polar encoder with arbitrary code length $N$ and arbitrary level of parallelism $M$. The general framework could be easily denoted by a general formula $F(N,M)$. Then we
show how to use an algorithm to derive a specific formula \( f_{N,M} \) from \( F(N,M) \) based on the values of \( N \) and \( M \). Finally, a compiler is employed to translate \( f_{N,M} \) into RTL description. The hardware generation system is illustrated in Fig. 2.

A. From General Framework to Formula

Consider that the general framework is expected to implement polar encoder with arbitrary code length and arbitrary level of parallelism, the framework should be scalable, i.e., the number of stages and the number of hardware modules in each stage should change with the values of \( N \) and \( M \). Such a scalable framework could be represented by formula \( F(N,M) \) shown in Eq. (2). Here the parameters \( N \) and \( M \) are powers of 2, and \( 4 \leq M \leq N/2 \). Before we go into details of \( F(N,M) \), we introduce all the symbols that might be used in \( F(N,M) \) and \( f_{N,M} \), as well as the symbols’ corresponding hardware modules. Note that the final hardware implementation of \( f_{N,M} \) is the serial connection of the individual modules of different symbols. Fig. 3 illustrates all the exemplary modules, as well as symbols, that might be used in our design, all of which take \( u_0^{N-1} \) as input and \( s_0^{N-1} \) as output.

Symbol \( XP \) represents an XOR-and-PASS module that achieves: \( x_0 = u_0 + u_1 \) (in GF(2)) and \( x_1 = u_1 \). The number of inputs of \( XP \) is fixed and equals to 2 in our design.

Symbol \( S_K \) (\( K \) is a power of 2, \( K > 1 \)) represents a switch with \( k/2 \) delay elements (denoted by \( D \)) on each side. A \( \log_2 K \)-bit counter is needed to control the switch: the value 0 of the most significant bit of the counter infers direct data transfer, and the value 1 infers cross data transfer. The number of inputs of \( S_K \) is fixed and equals to 2.

Symbol \( P_N \) (\( N \) is a power of 2, \( N > 2 \)) denotes the permutation on an \( N \)-dimensional vector. The detail function of \( P_N \) is illustrated in Algorithm 1. Intuitively, \( P_N \) is the duplication of \( P_{N/2} \). For example, \( P_8 \) could be viewed as partial overlap of two \( P_4 \) modules with red wires and black wires respectively.

Symbol \( (I_K \otimes A) \) (\( K \) is a power of 2, \( K > 0 \)) is a Kronecker product representing \( K \) parallel instances of module \( A \), where \( A \) is an abstract module and \( A \) could be replaced by \( XP \), \( S_K \) or \( P_N \). Note that when \( K = 1 \), \( (I_K \otimes A) \) equals to \( A \). Suppose that \( A \) has \( X \) inputs, the number of inputs of \( (I_K \otimes A) \) equals \( K \times X \).

The general formula \( F(N,M) \) is composed of symbols mentioned above, except that the \( W \) in Eq. (2) is a variable module. When deriving \( f_{N,M} \) from \( F(N,M) \), symbol \( W \) should be replaced by \( P_N \) or \( S_K \) according to its subscript. In Algorithm 2 as the code length and the level of parallelism are given, all the subscripts of each symbol in \( F(N,M) \) will be figure out. Then the module \( (I \otimes W) \) is replaced by \( (I \otimes P) \) or \( (I \otimes S) \) based on the value of the subscript of \( W \). Finally, the formula \( f_{N,M} \) is determined.

B. Compiler

We have built a compiler in Python that takes \( f_{N,M} \) as input and automatically connects all the basic modules in \( f_{N,M} \) in left-to-right order. Specifically, as we input \( N \) and \( M \) into \( F(N,M) \), the \( f_{N,M} \) will be determined and transformed into the register-transfer level (RTL) Verilog by the compiler. The detail of the compiler is beyond the scope of this paper; we only provide a brief introduction here.
\[
(I_{M/2} \otimes XP)(I_{M/4} \otimes P_3) \left\{ \Pi_{i=0}^{\log_2 N-3} [(I_{M/2} \otimes W_{N/(2^i M)})(I_{M/2} \otimes XP)] \right\} (I_{M/4} \otimes P_4)(I_{M/2} \otimes S_{N/M})(I_{M/2} \otimes XP) \tag{2}
\]
\[
(I_4 \otimes XP)(I_2 \otimes P_4) \{(I_4 \otimes W_4)(I_4 \otimes XP)(I_4 \otimes W_2)(I_4 \otimes XP)W_1(I_4 \otimes XP)\} (I_2 \otimes P_3)(I_4 \otimes S_4)(I_4 \otimes XP) \tag{5}
\]
\[
(I_4 \otimes XP)(I_2 \otimes P_4) \{(I_4 \otimes S_4)(I_4 \otimes XP)(I_4 \otimes S_2)(I_4 \otimes XP)P_8(I_4 \otimes XP)\} (I_2 \otimes P_3)(I_4 \otimes S_4)(I_4 \otimes XP) \tag{6}
\]

There are totally three types of basic modules in the formula \( f_{N,M} \): the XOR-and-PASS module \( XP \), the switch module \( S_K \), and the permutation module \( P_N \). There are two ways to expand these modules. The first one is to employ the symbol \( I_K \otimes \) to layout the duplication of one module in a parallel way. The other one is to change the symbols’ subscripts. Therefore, the compiler needs to read each symbol of \( f_{N,M} \) from left to right, and recognizes \( I_K \otimes \) as well as each symbol’s subscript. Then the compiler could determine the specific hardware architecture and print the Verilog files.

C. Input and Output Orders

The input and output data of this framework are in regular order. Suppose the input data of \( f_{N,M} \) is \( u_0^{N-1} \), since \( f_{N,M} \) represents a pipelined architecture, \( u_0^{N-1} \) will be divided into \( N/M \) \( M \)-dimensional vectors \( V_{in(i)} \) illustrated in Eq. (3), where \( i = 0, 1, \ldots, (N/M) - 1 \). All the data in \( V_{in(i)} \) will be entered into the encoder in parallel, and \( i \) indicates the sequence of the input vector, i.e., \( V_{in(0)} \) is the first set of the input data and the \( V_{in(N/M-1)} \) is the last set of the input data. The output data are in bit-reversal order. Specifically, suppose \( x_0^{N-1} \) is the theoretical codeword and \( y_0^{N-1} \) is in the bit-reversal form of \( x_0^{N-1} \). Then the \( i \)-th output vector \( V_{out(i)} \) equals to \( y_{M \times i + (M-1)}^{(M \times i + (M-1))} \), where \( i = 0, 1, \ldots, (N/M) - 1 \). \[
V_{in(i)} = \begin{bmatrix}
    u_{(M/2)\times i} \\
    u_{(M/2)\times i + (N/2)} \\
    u_{(M/2)\times i + 1} \\
    u_{(M/2)\times i + 1 + (N/2)} \\
    u_{(M/2\times i + 2)\times i + 2} \\
    \vdots \\
    u_{(M/2\times i + (M/2)\times i + (M/2)-1)} \\
    u_{(M/2\times i + (M/2)-1 + (N/2))}
\end{bmatrix} \tag{3}
\]

For the general framework, the processing latency (clock cycles) is \( T_{\text{latency}} = (3N/2M) - 1 \). The number of XOR gates and delay elements are:
\[
\#\text{XOR} = (M/2) \times \log_2 N; \\
\#\text{MEM} = (3N/2) - M. \tag{4}
\]

D. A 32-Bit 8-Parallel Polar Encoder

According to Algorithm 2 given \( N = 32 \) and \( M = 8 \), formulas \( F(32,8) \) and \( f_{32,8} \) are obtained in Eq. (5) and Eq. (6), respectively. The hardware architecture is illustrated in Fig. 4 which consists of 20 XOR gates and 40 delay elements in accordance with Eq. (4). The architecture could be split in 11 columns, each of which has its relevant symbol under the column. Note that Eq. (6) is actually composed of all the symbols at the bottom of Fig. 4. The order of the input data \( u \) \((k = 0, 1, 2, 3)\) at the leftmost part of Fig. 4 conforms to the order mentioned above. The output data \( x \) is in the bit-reversal order.

IV. PERFORMANCE AND COMPLEXITY

Some of the hardware designs derived from the auto-generation system were implemented on the Xilinx Virtex-7 VC709 FPGA platform with Virtex-7 XC7VX690T. All the design examples are of the same code length \( N = 1024 \), but with different level of parallelism. The synthesis results are illustrated in Table I. From the table, it can be observed that the throughput (T/P) and the number of Slice LUTs and Slice Registers increase as the value of \( M \) increases. In an extreme case, the polar encoder with \( M = 512 \) consumes more Slice
LUTs than the polar encoder with $M = 4$ by 5167% but achieves higher throughput by 8710%.

As mentioned in Section III, the value of $M$ conforms to $4 \leq M \leq N/2$. Then, given the code length $N$, the generation system could implement $(\log_2 N) - 2$ designs with different $M$, covering a wide cost/performance trade-off space. Therefore, one could choose the most suitable polar encoder in the design space to fit the application.

![Fig. 4. The hardware architecture of polar encoder with $N = 32$, $M = 8$.](image)

### Table I

| $N$   | $M$ | Slice LUTs | Slice Registers | Max freq (MHz) | T/P (Gbps) |
|-------|-----|------------|-----------------|---------------|------------|
| 1024  | 4   | 148        | 82              | 519.535       | 2.01       |
| 1024  | 32  | 467        | 312             | 407.05        | 13.02      |
| 1024  | 128 | 1278       | 845             | 340.518       | 43.58      |
| 1024  | 256 | 1704       | 1194            | 348.712       | 89.27      |
| 1024  | 512 | 2628       | 1025            | 356.223       | 182.38     |

### V. Conclusion

This paper proposes an auto-generation system for the hardware architecture of polar encoder. The system could offer users a wide range of design space so that the users could make a trade-off between cost and performance to best fit their applications. The essence of the generation system lies in the formula-based expression of the general framework for polar encoder that could achieve encoding with arbitrary code length and arbitrary parallelism. This auto-generation can help designers to conveniently design polar encoder without touching hardware details. The derivation of design space can further help us to identify the required design.

In this paper, we also introduce the scalable hardware modules associated with the formula, as well as the compiler that could transform the formula into RTL Verilog files. Synthesis results on FPGA have demonstrated the efficiency and the large trade-off space of the auto-generated circuits.

Future work will be directed toward the auto-generation of successive cancellation polar decoder and belief prorogation decoder based on our previous works [3–8], and the design optimization based on the design space.

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