Design and implementation of a digital mixer with digital logic

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Abstract. A mixer is a device whose output frequency is a sum or a difference of input frequencies. With \( f_1 \) and \( f_2 \) as input frequencies, the output frequency is \( f_1 + f_2 \) or \( |f_1 - f_2| \). The mixer is generally an analogue device. In this work, we suggest a digital mixer, designed and implanted using digital logic. A phase locked loop is added at the output of the mixer acting as a pass band filter. The input and output digital nature implies that there is no conversion loss and the isolation between output port and input ports was no less than 45 dB. The mixer can be used for downconversion of the signal to be measured in spectrum analyzer.

1. Introduction
Frequency mixers are widely used in communications systems for signals up conversion or down conversion. Usually they are analogue devices. Digital mixers have been also proposed in the literature. In [1] EXOR gates were used for multiplication of the input signals and some of the intermodulation spurs were cancelled through multi-phasing of input signals [2]. However multiple phases (up to 7-phase in the example given in the paper) were necessary to obtain satisfactory results. In [3] a nonlinear Digital-to-analog conversion was used in addition to multi-phasing. This nonlinear DAC add more complexity to the method. An FPGA implementation of a frequency mixer was also proposed in [4], in which VLSI (Very large Scale Integration) is used for frequency conversion. The last method appears to be too complex, in view of to the hardware involved. We suggest a simple digital mixer whose operation theory is based on trigonometric identity (1). The novelties of the method are:

- The use of the model of trigonometric identity for intermodulation cancelation of half of intermodulations spurs,
- The use digital logic for the operation of “ADDITION” of two square wave signals as shown in paragraph 2.2.
- Obtaining square wave at the output of the frequency mixer. The method used in [2] and [3] lead to obtaining sinusoidal signal.
- The suggested mixer does not need any calculation as in [2] and [3] and therefore can be used for high frequencies.

The limitation of proposed method is the presence of spurs which could not be removed by the filter as they are near the fundamentals and the harmonics of the square wave. The proposed mixer is digital in the sense that digital logic gates and digital signals are used instead of analogue components and analogue signals. We begin with design methodology which is based on mathematical trigonometric identity. The simulation and hardware implementation will follow. From the simulation, the hardware implementation and the measurements that have been made, it will be shown, that a pass band filter at the output is necessary for the attenuation of spurious components.
2. Design methodology
The functional diagram of the suggested digital mixer is shown on figure 1.

![Functional diagram of the suggested mixer](image)

The block 1 represents a digital multiplier whose role is to generate the difference of the input frequencies and the block 2 is a pass band filter added at the output of the digital mixer. The digital mixer operation theory is elaborated based on trigonometric identity (1). Square wave signals are used as digital inputs and ADDITION and MULTIPLICATION are replaced by digital logic. Simulation is done using Simulink and hardware implementation is achieved using High speed CMOS logic gates.

2.1. The theory of the suggested mixer
We will focus on digital mixer with the difference frequency at the output. However, the proposed methodology can be equally applied to get the sum frequency at the output. An ideal analogue mixer with the difference frequency at the output can be expressed by the following trigonometric identity:

\[ \cos(\omega_1 t) \cdot \cos(\omega_2 t) + \sin(\omega_1 t) \cdot \sin(\omega_2 t) = \cos((\omega_1 - \omega_2) t), \]

where \( \omega_1 \) and \( \omega_2 \) are the input signals pulsations.

\[ \cos(\omega_1 t) \cdot \cos(\omega_2 t) + \cos(\omega_1 t - \frac{\pi}{2}) \cdot \cos(\omega_2 t - \frac{\pi}{2}) = \cos((\omega_1 - \omega_2) t) \]  \( \text{(1)} \)

A simple multiplication of two cos would have given:

\[ \cos(\omega_1 t) \cdot \cos(\omega_2 t) = \frac{1}{2} \left[ \cos((\omega_1 - \omega_2) t) + \cos((\omega_1 + \omega_2) t) \right] \]  \( \text{(2)} \)

Equation (1) contains only difference of frequencies while equation (2) contains both the sum and the difference of input signals. In case of square wave signals, this method allow cancellation of the intermodulation of the frequencies \( n\omega_1 + m\omega_2 \) with \( n \) and \( m \) integers. We will use the model (1) for the digital mixer, with the difference that the signals at the input are digital square waves now and that the ADDITION and MULTIPLICATION in the analogue domain are replaced by their equivalent in the digital domain. It is well known that MULTIPLICATION in that case is equivalent to XOR [1].

In this paragraph, we explain how the ADDITION is implemented. Let A and B be the inputs to the digital mixer and let 1 and -1 be the low and high signal level respectively. The “ADDITION A+B” is shown on figure 2.

A and B are 2-level square wave signals while A+B is a 3-level signal. Based on figure 2, A+B can be implemented using digital logic. The first row in the figure 2 will be transformed in the low level, while the last row will be transformed into the high level. The first row is “NEITHER A nor B (logic NOR)” and it will reset the RS trigger while the last row “A and B (AND)” will set the RS trigger. The figure 3 shows the digital mixer based on the above mentioned principle. Therefore, equation (1) can be implemented by the digital circuit represented on figure 3 provided the shift \( \frac{\pi}{2} \) is done before the signal is fed to XOR gate.
### 2.2. Simulation

The figure 4 shows the simulation model using Simulink. The digital mixer is fed with two clock signals with frequencies f₁ and f₂. The gate NOT shifts the input signal by 180° and each D flip flop divides by 2 the frequency of the signal at his input. This results in a 90° shift between the signals at the output of “D flip flop” and “D flip flop1”. The same 90° shift exists between the “D flip flop2” and “D flip flop3” outputs. Due to the division by 2 when using D flip flops, the output of mixer is |f₁-f₂|/2. Simulation showed that whenever one of the frequencies is a multiple of the other, the mixer works perfectly while spurious components appear whenever this is not the case (figure 5 and figure 6). An output filter is therefore necessary as early mentioned.
2.3. Hardware implementation and measurements

For the bloc 1 on figure 1, the hardware implementation is straightforward from simulation functional diagram by replacing different blocs with corresponding logic gates. The following integrated circuits were used: D flip flop CD74HC74E, NOT gate CD74HC04E, XOR gate CD74HC86E, NOR gate CD74HC02E and AND gate CD74HC08E4. The RS flip flop was implemented using two NOR gate as shown on the figure 7.

![RS flip flop implementation from NOR gates.](image)

For the bloc 2 on figure 1, a passband frequency filter was implanted using PLL (phase locked loop). The chip CD74HC4046AE was used for this purpose. For the illustration of the mixer operation 2 para of frequencies where used. The figure 8 shows the output power spectral density with and without the output filter when $f_1=56464$ Hz, $f_2=37918$ Hz and $f_{\text{out}}=9273$ Hz. The effect of the PLL based pass band filter is also shown on figure 8. Figure 9 shows the output power spectral density when $f_1=9536$ Hz, $f_2=25893$ Hz and $f_{\text{out}}=8178.5$ Hz. Isolation of output from input is shown on figure 10 and figure 11, where the output power spectral density is measured at input frequencies.
3. Results and discussion
Both the simulation and hardware implementation show that the suggested method for digital frequency mixer can be implemented. It is simplicity is attractive, if we compare it to the methods described section 1. However, the measurement show that more effort is needed for spurs attenuation. It’s main advantage, compared to its analogue equivalent, is that there is no conversion loss and that good isolation of the output from inputs is assured.

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