Everything You Always Wanted to Know About Quantum Circuits

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I. INTRODUCTION

The development of circuits for quantum computing has been motivated by the proliferation of quantum algorithms which promise up to a superpolynomial factor speedup over classical equivalents. The quantum algorithms developed have the potential to impact fields such as number theory, encryption, scientific computation, and in quantum circuit design automation. The design of quantum algorithms remains an active area of research and new algorithms continue to appear in the literature. For instance, quantum circuits are composed of quantum gate networks. Quantum machines developed from entities such as IBM or Honeywell support gate based quantum computation. Gate based quantum circuit design has applications in fault tolerant quantum computation and in quantum circuit design automation. Each quantum gate represents a quantum mechanical operation. As a result, the designer working with quantum circuits shall have to contend with novel properties and challenges. In this work, quantum circuits are one-to-one and all information is preserved.

The design of quantum circuits for the implementation of quantum algorithms has caught the attention of researchers. Circuits for elementary functions such as basic arithmetic functions (such as addition or division) have been proposed such as \[30\] \[31\] \[32\] \[33\] \[34\] \[35\] \[36\] \[37\]. These basic circuits are used as building blocks for more complex datapath systems such as higher level mathematical functions for applications in scientific computing, image processing or machine learning \[38\] \[39\] \[40\] \[41\] \[42\] \[43\]. These functions in turn perform the computations called for in quantum algorithms. As a result, dedicated libraries of basic quantum arithmetic functions are included in quantum programming languages such as Quipper \[44\] and LIQUi\textsuperscript{\textregistered} \[45\] and researchers continue to invest efforts in the design of increasingly more resource efficient quantum circuits. In this work, we illustrate how elementary quantum circuits could be used to implement a quantum circuit for the image rotation operation. The image rotation operation is a higher level mathematical function that can be used for quantum realizations of image processing applications such as those shown in \[46\] \[47\] \[48\] \[39\].

In this work, we provide an overview of circuits for quantum computing. In Section II we introduce gates used in quantum computation and present resource cost measurements used to evaluate circuits made from these gates shown. We then illustrate how the gates shown are then combined into quantum circuits for basic arithmetic functions in Section III. In Section IV, we demonstrate how to calculate the resource costs of quantum circuits. We conclude this overview with Section V by illustrating an application of the elementary quantum circuits shown in Section III.

II. OVERVIEW OF QUANTUM CIRCUITS

Quantum circuits based on gates represent sequences of controlled quantum mechanical operations. These operations act on information stored in one or more quantum bits or qubits. The physical implementation of the qubit shall depend on the underlying technology. For instance, qubits are realized with Josephson junctions in superconducting quantum machines or qubits are individual ions in the case of a trapped ion quantum machine \[22\] \[51\] \[18\] \[21\]. Implementation differences aside, the quantum machine allows us to utilize the properties of quantum mechanics to perform useful work. Such useful properties include superposition and entanglement. Superposition is a consequence of the probabilistic nature of quantum machines and entanglement allows us to create dependencies between two or more qubits. Figure I introduces these properties. Thanks to superposition and entanglement it is possible for an \(n\) qubit quantum circuit to operate on \(2^n\) values simultaneously. This is because, pursuant to superposition, we are operating not on fixed binary values but on probability distributions (see Figure I). As a result every value is present with an associated probability \(p\). The ability to make codependent qubits through entanglement is a powerful tool that allows us to, among other tasks, create fault tolerant quantum gate implementations \[52\] \[24\].
A qubit is probabilistic in nature. Thus, a qubit is 1 with a probability $\alpha$ and 0 with a probability $\beta$. Thus, a qubit can assume an infinite range of values (any point on the surface of the sphere shown in the illustration above). With gates we can adjust the probability values of a qubit.

**Entanglement:** Two or more qubits can become interdependent. Thus, information about one of the entangled qubits can allow us to glean information on the others.

**Unitarity:** For given quantum operation $U$, there exists a $U^\dagger$ which undoes the computation. As a result, quantum computation is reversible in nature.

**Measurement:** The result of computation of a quantum circuit is read via measurement. Consequently, qubits in superposition are either set to values $|0\rangle$ and $|1\rangle$. Which of these computational basis states (or eigenstates) appears on the measured qubit shall depend on the associated state probabilities.

A consequence of working with quantum mechanical operations (or gates) is that they are unitary. The unitary principal means that for a given quantum operation $U$, there exists a $U^\dagger$ such that the following expression is true:

$$UU^\dagger = I \quad (1)$$

where $U$ is a quantum mechanical operation and $U^\dagger$ is the complex conjugate transpose of $U$.

Thus, there exists an operation which undoes the work accomplished by a previous quantum mechanical operation. Or, more specifically, for a given network of gates, there exists a gate network which shall undo the results of computation. This means that quantum gates and quantum circuits are reversible in nature. As a result (i) information is not destroyed and (ii) the mapping between circuit inputs and outputs is one-to-one. As a result the quantum circuit designer works exclusively with reversible gates and shall have to take into account new measures when evaluating the resource cost of a quantum circuit. Section II-A introduces many of these gates and Section II-B introduces the resource cost measures.

To determine the result of computation, a contents of a quantum register needs to be measured. Measurement is also used when the result of computation of a quantum circuit needs to be provided as input to a classical circuit. To illustrate measurement we need a way to present quantum states. We can represent a quantum state using vectors and matrices. Consider a qubit (a two level quantum state) $X$. The observable states of a qubit are 0 and 1 which we can represent in vector form as:

$$|0\rangle = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \quad |1\rangle = \begin{bmatrix} 0 \\ 1 \end{bmatrix} \quad (2)$$

So we can represent $X$ when in a superposition as follows:

$$|X\rangle = \alpha \cdot |0\rangle + \beta \cdot |1\rangle \equiv \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \quad (3)$$

The symbol around $X$ which appears in equation (3) is a “ket”. It is a shorthand notation for the vectors presented in the equations. If we were to take a complex conjugate of any of these vectors we can represent it using a “bra”. So $X^\dagger$ can be presented with a “bra” as follows: $\langle X |$. Collectively, this notation is called “bra-ket” notation and is widely used when describing quantum computing and the underlying physics.

So now that we know how one can present mathematically quantum states such as qubits, we now turn our attention to measurement. The quantum measurement task represents a projective quantum mechanical operation $\{A_i\}$. In a projective operation, a qubit in superposition shall be set to one of a set of observable states (also called eigenstates) at the end of computation. So, for the case of a qubit in superposition such as $|X\rangle = \alpha \cdot |0\rangle + \beta \cdot |1\rangle$, the observable states are $|0\rangle$ and $|1\rangle$.

So, at the end of computation $|X\rangle$ shall be projected to $|0\rangle$ or $|1\rangle$. The likelihood of seeing $|0\rangle$ and $|1\rangle$ shall depend on the associated probabilities $\alpha$ and $\beta$. More generally given a quantum state $|A\rangle$ given as:

$$|A\rangle = \sum_i c_i |m_i\rangle \equiv \sum_i |m_i\rangle \langle m_i |A \rangle \quad (4)$$

where $m_i \in M$ is the $i$th observable state and $c_i$ is the associated probability. In measurement, at the end of computation, $|A\rangle$ shall be projected to the observable $m_i$ (where $m_i \in M$) that enjoys the largest probability $c_i$. 

**Unique Quantum Computer Properties**

- **Superposition:**

  \[ |1\rangle = |\alpha\rangle + |\beta\rangle \]

  A qubit is probabilistic in nature. Thus, a qubit is 1 with a probability $\alpha$ and 0 with a probability $\beta$. Thus, a qubit can assume an infinite range of values (any point on the surface of the sphere shown in the illustration above). With gates we can adjust the probability values of a qubit.

- **Entanglement:** Two or more qubits can become interdependent. Thus, information about one of the entangled qubits can allow us to glean information on the others.

- **Unitarity:** For given quantum operation $U$, there exists a $U^\dagger$ which undoes the computation. As a result, quantum computation is reversible in nature.

- **Measurement:** The result of computation of a quantum circuit is read via measurement. Consequently, qubits in superposition are either set to values $|0\rangle$ and $|1\rangle$. Which of these computational basis states (or eigenstates) appears on the measured qubit shall depend on the associated state probabilities.

Fig. 1: Properties of quantum computer. For more details, the reader is encouraged to see \[49\] \[50\] \[22\].
Clifford+T gate set because it is (i) an approximately universal set and (ii) these can be made fault tolerant with existing quantum error correcting codes [27] [26] [54] [55] [56] [24].

Gates such as the Hadamard gate or T gate are examples of gates which produce a superposition state at the end of computation. Access to gates with produce superpositions enables the quantum circuit designer to execute a richer set of possible computations. For example, with a quantum computer, one can directly calculate the quantum Fourier transform shown below:

$$|x\rangle = \frac{1}{\sqrt{N}} \sum_{y=0}^{N-1} e^{2\pi \frac{xy}{N}} |y\rangle \quad (5)$$

Equation [5] is analogous to the discrete Fourier transform and is used in the implementation of algorithms such as those shown for integer factoring (see [2]), the hidden linear structure problem ([57]) or link invariant problems (see [58]).

Gates such as the Hadamard and T gate are called one qubit gates and the CNOT gate is an example of a two qubit gate. The CNOT gate (or Controlled NOT gate) is a two input operation where one input is referred to as the control qubit (qubit $|A\rangle$) in Figure [4] and the second input is the target qubit (qubit $|B\rangle$) in Figure [4]. As shown in Figure [4] the value of the control qubit shall determine the result of computation seen on the target qubit. Referring to the Figure, when $|A \equiv 1\rangle$, $|B\rangle$ shall have the value $1 \oplus B \equiv \overline{B}$. When $|A \equiv 0\rangle$, $|B\rangle$ shall be unchanged at the end of computation. The CNOT gate is an example of a controlled gate because the action of the gate (the NOT operation) is controlled (in this case by the value of qubit $|A\rangle$). The CNOT gate is also referred to as a Feynman gate in the literature.

Figure [4] shows how to read the quantum circuits shown in this work. Quantum circuits are read left to right. Each "line" shown in Figure [4] represents a qubit. Quantum gates are laid out as needed on the diagram to illustrate the computation tasks to be performed. The quantum circuit diagram provides a temporal representation of the computations taking place on quantum machines. Thus, in a quantum circuit diagram (such as the one shown in Figure [2]) one is seeing how quantum mechanical operations are applied as a function of time to complete a given operation.

Clifford+T gates can be combined to implement higher level logic gates. Figure [3] illustrates examples of how the Clifford+T gates are used to implement higher level logic gates (specifically the Toffoli gate and the Fredkin gate). These higher level gates have the functionality shown in Figure [5] Schematic images also are shown for the Toffoli gate and Fredkin gate.

We focus on the Toffoli and Fredkin gates (see Figure [5]) in this article because they are basic building blocks routinely used in the design of reversible logic systems such as those shown in [33] [59] [60] [61]. These gates are used to construct the quantum circuits presented in this article.

Like the Clifford+T gates, the Toffoli gate and Fredkin gate represent unitary operations and are reversible. The Toffoli gate takes 3 inputs $A, B, C$ and returns 3 outputs $A, B, A \cdot B \oplus C$. The Toffoli gate is another example of a controlled gate. Unlike the CNOT gate, the Toffoli gate has two control

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**Clifford+T Quantum Gates**

| Gate       | Matrix                                                                 |
|------------|------------------------------------------------------------------------|
| Hadamard   | $H = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$ |
| T Gate     | $T = \begin{bmatrix} 1 & 0 \\ 0 & e^{i\pi/2} \end{bmatrix}$        |
| Hermitian of T Gate | $T^\dagger = \begin{bmatrix} 1 & 0 \\ 0 & e^{-i\pi/2} \end{bmatrix}$ |
| Phase Gate | $S = \begin{bmatrix} 1 & 0 \\ 0 & i \end{bmatrix}$                |
| Hermitian of Phase Gate | $S^\dagger = \begin{bmatrix} 1 & 0 \\ 0 & -i \end{bmatrix}$ |
| NOT Gate   | $\lnot = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$ |
| Feynman (CNOT) Gate | $\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$ |

**Controlled Gate Example**

$|A\rangle \quad |A\rangle \quad |B\rangle = \begin{cases} |B\rangle & \text{if } |A\rangle = 0 \\ \overline{B} & \text{if } |A\rangle = 1 \end{cases}$

Fig. 2: This marked up example of a quantum circuit diagram illustrates how to read a quantum circuit diagram.

Fig. 3: The quantum gate set used in this work.

Fig. 4: The CNOT gate is an example of a controlled gate. Schematic diagram and mathematical description of operation are shown.
The Toffoli and the Fredkin Gate

| A | A |
|---|---|
| B | B |
| C | A \cdot B \oplus C |

(a) The Toffoli gate

| A |
|---|
| B |
| C |

(b) The Fredkin gate.

| A |
|---|
| B |
| C |

(c) Clifford+T implementation of the Toffoli gate. Source [23].

| A |
|---|
| B |
| C |

(d) Clifford+T implementation of the Fredkin gate. Source [23].

Fig. 5: The Clifford+T quantum gate implementation of reversible logic gates.

Sources of Overhead in Quantum Circuit

- **Garbage Output**: Garbage outputs are any outputs of a quantum circuit that is not a primary input or a useful output.
- **Ancillae**: Ancillae are additional qubits (often set to a constant value such as 0) required by a quantum circuit to hold computations.
- **Qubit Cost**: The total number of qubits required by a quantum circuit.
- **Depth**: The total number of gate layers in a circuit. A layer consists of quantum gates operating in parallel.
- **Gate count**: The total number of gates in a quantum circuit.

Fig. 6: Cost metrics used in quantum computation.

Procedure to Remove Garbage Output

| A | A |
|---|---|
| B | B |
| 0 | 0 |
| f(A, B) | f(A, B) |

(a) After Step 1

| A | A |
|---|---|
| B | B |
| 0 | 0 |

(b) After Step 2

| A | A |
|---|---|
| B | B |
| 0 | 0 |

(c) After Step 3

Fig. 7: General procedure to eliminate garbage outputs produced by a quantum circuit. $U$ refers to a generic quantum circuit. To probe further see [60].

B. Quantum Circuit Resource Cost Measurements

To determine items such as (i) the suitability of a given quantum circuit design for a given quantum machine or (ii) whether a newly proposed design improves upon the state of the art, we evaluate the resource costs of quantum circuits. Like in classical computing, we assess a circuit in terms of various resource measures. Figure 6 illustrates sources of resource overhead in a quantum circuit. Depth (number of gate layers) and total gate count should be familiar as similar measures exist in classical computing (such as critical path delay or transistor count). Qubit cost refers to the total number of qubits required by a quantum circuit. Because quantum computation is reversible, ancillae and garbage output are resource overheads which must be considered in quantum circuit design. Because information cannot be destroyed, there is a need for additional scratch qubits (or ancillae) to hold intermediate steps of computation. These intermediate steps of computation can end up becoming garbage outputs. In general, any output that is not part of the original input or a desired output is garbage. Garbage outputs must be removed via reverse computation before the occupied qubits can be used for subsequent computations. The general procedure for the removal of garbage outputs is shown in Figure 7 and outlined in [60].

As illustrated in Figure 7 a three step procedure is outlined where in Step 1 the circuit performs its computation, Step 2 desired outputs are copied to ancillae. Then, in Step 3, the computations in Step 1 are undone. The result is that qubits holding garbage outputs are now restored to their initial values and can be used for subsequent circuits. The associated qubits and gates required to clear garbage output add to the overall...
circuit cost. The resource cost values reported for a quantum circuit with garbage outputs may not take into account the associated costs of removing garbage outputs. As a result, resource cost values for a reported for a given circuit may be lower than what is encountered when the circuit is used in computational work. Thus, the designer should take into account the costs of removing garbage outputs when assessing the suitability of a particular quantum circuit.

These resource costs measured (gate count, depth, ancillae, garbage output) have been further refined by quantum circuit designers for (i) fault tolerant quantum machines (or FTQ machines) and (ii) near-term (or noisy intermediate scale quantum NISQ machines). For the remainder of this Section, we shall examine the resource cost measures for both types of machines.

### Sources of Faults in Quantum Computers

- **Gate Error**: Implementing each quantum gate has a probability of incorrect operation.
- **Energy Relaxation**: A qubit in state \(|1\rangle\) decays to state \(|0\rangle\) over time.
- **Dephasing**: A qubit in superposition loses the superposition state information over time.
- **State Preparation and Measurement (SPAM) Error**: Qubit initialization and qubit measurement have probabilities of error. These are reported together since the only way to determine if a qubit was initialized correctly is to measure it.

Fig. 8: Sources of error in quantum machines. Source [51] [18] [61] [62] [63]

#### 1) Resource Cost measures for NISQ machines: The existing quantum machines from IBM, Honeywell, IonQ and others are NISQ machines (see [21] [51] [18]). These quantum machines are large enough to support interesting computations but too small for proposed quantum error correcting codes. Thus, the choice of resource measures to evaluate NISQ quantum circuits is motivated, in part, by the many sources of error that occur in NISQ machines. Figure 8 summarizes some of the reasons why a computation can fail on a NISQ machine. In addition to non-ideal outcomes from operations such as measurement, qubits sitting idle can lose their information over time. This is due to the property of coherence. While on paper, we can assume fully isolated qubits which can hold state information indefinitely, in practice the information on a qubit shall be disturbed by the environment [63] [61] [62]. Thus, an analogy can be drawn between the qubit and the DRAM cell due to the fact that they both lose their state information over time.

Figure 9 illustrates the measures used to evaluate the resource costs of a quantum circuit implemented on a NISQ machine. The CNOT gate (see Figure 3) has been emphasized because gates that act on two qubits have a higher error rate than one qubit gates [18] [51] [20]. A NISQ circuit with many CNOT gates shall face a higher risk of computation failure than a circuit with a reduced CNOT gate count. Therefore CNOT-count and CNOT-depth are cost measures that are used to evaluate quantum circuit performance [66]. The \(KQ\) measure is included as it is used in the estimation of the fidelity of a computation on a given quantum circuit [65] [66]. The probability of success of a given quantum circuit can be estimated by the following computation:

\[
\frac{1}{K \cdot Q} = A
\]

where \(Q\) is the qubit cost and \(K\) is the circuit depth.

A first order estimation of the likelihood of a correct computation of a circuit running on a quantum machine can be achieved by comparing \(A\) to the worst case (or largest) failure rate (\(\epsilon\)) reported for the quantum machine [65]. If \(A < \epsilon\) then a given circuit can deliver correct computations on the NISQ machine. Conversely, if \(A \geq \epsilon\) then the proposed circuit shall require quantum error correcting codes. \(KQ_{CNOT}\) is like the \(KQ\) measure in that it is used to estimate fidelity. However, we only consider the depth of CNOT gates when computing \(KQ_{CNOT}\).

#### 2) Resource Cost measures for FTQ machines: In fault tolerant quantum computation, quantum error correcting codes and fault tolerant gate implementations are used to mitigate the risk of noise errors. While a physical quantum machine that can handle quantum error correcting codes does not exist, researchers have worked to develop fault tolerant gates and circuits [56] [23] [26] [56] [68]. The Clifford+T gate set (see Figure 3) has been frequently used in fault tolerant quantum circuit design because it can be made fault tolerant with existing quantum error correcting codes [69] [24] [26] [70] [71] [72]. There are trade offs to using this gate family namely (i) high resource overhead of the fault tolerant implementation of the T gate and (ii) it is approximately universal [27] [54] [73].
In a fault tolerant T gate, ancillae set to the following superposition states $|A\rangle$ and $|Y\rangle$ (where $|Y\rangle = \frac{1}{\sqrt{2}}(|0\rangle + e^{i\frac{\pi}{2}}|1\rangle)$ and $|A\rangle = \frac{1}{\sqrt{2}}(|0\rangle + e^{i\frac{\pi}{4}}|1\rangle)$) are created. To ensure ancillae are set to $|A\rangle$ and $|Y\rangle$ with sufficient fidelity, a process called state distillation is used. The state distillation process adds to the overall overhead of the fault tolerant T gate in terms of gate cost, qubit cost and depth [54] [27]. The overhead from state distillation results in the T gate overwhelming the other Clifford gates in terms of resource costs [67]. As a result, the number of T gates (T-count) and number of T gate layers (T-depth) are used to assess quantum circuit performance. $K_{QT}$ is like the $K_Q$ measure in that it is used to estimate fidelity. However, we only consider the depth of T gates when computing $K_{QT}$.

The “approximately universal” nature of the Clifford+T gate means that certain types of gates and circuits shall incur prohibitively high T-count and T-depth costs [73]. This plagues circuits based on gates which perform the following operation:

\[
\begin{bmatrix}
1 & 0 \\
0 & e^{i\pi/4}
\end{bmatrix}
\]

where $n = 2^m$ (7)

where $m \in \mathbb{Z}$ and $m \geq 3$.

The high cost of this class of gates is because they cannot be exactly implemented by the Clifford+T gates [55] [73]. To improve the approximation accuracy, more gates are required [55]. This is in stark contrast to the Toffoli and Fredkin gates shown in Figure 5 because their associated Clifford+T gate implementations are functionally correct implementations. Circuit implementations for the quantum Fourier transform and inverse quantum Fourier transform are two examples of quantum circuits based on gates that perform operations shown in equation (7) where $m \geq 3$. Due to the importance of these circuits in quantum algorithms (see [2] [73] [75] [10] [76]), the search for implementations with reduced T-depth and T-count is an active area of research. Thus, the impact of the approximate universality of the Clifford+T gate set is an important consideration the quantum circuit designer should keep in mind.

III. QUANTUM CIRCUITS FOR BASIC OPERATIONS

Quantum circuits for elementary functions such as arithmetic functions are used as building blocks in implementations of quantum algorithms. In this Section we present examples of quantum circuits used for basic arithmetic which are used as building blocks in larger quantum datapath circuits such as those presented in [6] [42] [40] [44] [77] [12]. As a result, the design of quantum circuits for arithmetic functions is an active area of research and quantum programming languages such as Quipper [44] and LIQUi/i [35] include libraries of quantum arithmetic circuits.

This Section shall present circuits for several basic arithmetic functions. The circuits shown in Sections III-A III-B III-C and III-D are examples of quantum circuits which accept input that are either (i) a single boolean value or (ii) multiple boolean values in superposition. These circuits perform computations analogous to classical arithmetic circuits and return results of computation that are (i) a single boolean value or (ii) multiple boolean values in superposition. As we have learned, quantum gates can return superposition states. Thus, it is possible to represent computations in terms of superposition state manipulations. For these circuits, at the end of computation, the result shall appear as a modification to the original superposition state of the input. An example is the quantum Fourier transform which was presented earlier (see equation 5). To acquaint you with this class of circuit, Section III-E illustrates an example of the quantum circuit implementation of the quantum Fourier transform.

A. Addition

Figure 11 illustrates an example of a quantum circuit for addition that was first presented in [78]. As opposed to alternative architectures such as those shown in [38], this style of addition circuit enjoys no garbage outputs.

Consider the conditional addition of two $n$-bit numbers $a$ and $b$ which are stored in quantum registers $|A\rangle$ and $|B\rangle$. A quantum register is an $n$ bit array of qubits. Two ancillae are used (see Figure 11). One if set to $|0\rangle$ and shall have the most significant bit of the sum $s_n$. The second ancillae can be set to $|0\rangle$ or hold a carry in bit $c_0$. At the end of computation, quantum register $|B\rangle$ shall contain the sum bits $s_0$ through $s_{n-1}$. Quantum register $|A\rangle$ shall have the value $a$ and the ancillae originally set to $|0\rangle$ or $c_0$ shall be restored to its original value.

This circuit cleverly exploits the Bennett’s garbage removal method presented in [60] and shown in Figure 7 to eliminate garbage output. Each carry bit is generated first. This is accomplished by the array of Majority (MAJ) circuit blocks (the construction of a MAJ block in terms of reversible logic gates is shown in Figure 11). The most significant carry bit $c_n$ is then copied to an ancillae because $c_n = s_n$. Hence the CNOT gate which takes the qubit with the value $c_n$ and an ancillae as inputs appears in Figure 11. Then the computation of the carries is reversed in a manner such that the remaining sum bits are produced and any intermediate computations are removed. This uncomputation is the work performed by the array of Unmajority and Add (UMA) circuit blocks (the
construction of a UMA block in terms of reversible logic gates is shown in Figure 11. Note that the UMA blocks are applied in reverse order of the MAJ blocks. This is intentional and is because we need to uncompute the carry bits by first starting with the most significant bit \( c_n \) and working backward toward the least significant carry bit \( c_0 \).

The design of addition circuit continues and alternative designs free of garbage outputs have been proposed such as \[66\] \[79\] \[34\] \[80\] \[33\] that offer reductions in cost measures such as T-count or qubit costs. Useful variants such as conditional adders (adders whose functionality can be disabled via additional control signals) are being developed as well \[79\] \[30\] \[31\].

B. Subtraction

In classical computation, subtraction can be accomplished with arrays of full subtraction blocks or by modifying an addition circuit so that it performs subtraction. In this article, we shall focus on the latter approach. Figure 12 shows an implementation of an adder proposed in \[37\] that has been modified to perform subtraction. The adder used is the same.
design as the one shown in Figure 11. Figure 13 shows how a generic addition circuit can be made to perform subtraction.

Consider the subtraction of two $n$-bit numbers $a$ and $b$ which are stored in quantum registers $|A\rangle$ and $|B\rangle$. The subtraction circuit calculates $|B\rangle - |A\rangle$ which simplifies to $|B\rangle + |\overline{A}\rangle$. At the end of computation, $|A\rangle$ has the input value $a$ and $|B\rangle$ contains the difference $d$. As shown in Figure 13 by adding arrays of NOT gates to the before and after the quantum addition circuit, the whole circuit performs subtraction. The functionality of the quantum adder used is not impacted by the additional hardware.

The cost of this particular circuit is a function of the underlying addition circuit used. Thus, as researchers present more resource efficient addition circuits, the cost of subtraction circuits shall also stand to benefit.

C. Multiplication

![Quantum Multiplication Circuit](image)

Fig. 14: Quantum circuit for the multiplication of two 5 bit values. The blocks labeled “Conditional Add” are conditional addition circuits and block labeled “TGA” is an array of Toffoli gates. Adapted from the design shown in [31].

Figure 14 shows an example of a quantum multiplication circuit. The circuit is composed of (i) conditional addition circuits and (ii) arrays of Toffoli gates.

As multiplication is a fundamental operation in computation, researchers have developed many circuits to implement several algorithms for the tasks of multiplication such as shift add, and Karatsuba’s algorithm [81] [31]. However, for quantum computing, only a subset of these algorithms can be used. Specifically, we cannot use algorithms that result in circuit implementations that depend on feedback or fan out paths. The multiplication circuit shown in Figure 14 is based on the shift and add multiplication algorithm and can be viewed as a quantum circuit equivalent to array multipliers such as those presented in [82] [83]. More formally, the circuit shown in Figure 14 performs the multiplication of two $n$ bit values $a$ and $b$ by computing the following expression:

$$P = \sum_{i=0}^{N-1} a \cdot b_i \cdot 2^i \quad (8)$$

where $P$ is the product.

The circuit shown in Figure 14 takes two $n$ bit inputs $a$ and $b$ (located in quantum registers $|A\rangle$ and $|B\rangle$). The product $P$ shall appear on $2 \cdot n$ ancillae at the end of computation. The content in registers $|A\rangle$ and $|B\rangle$ are returned to their original values ($a$ and $b$, respectively) at the end of computation. As shown in Figure 14 an additional ancilla is required by the multiplication circuit for a total of $2 \cdot n + 1$ ancillae. The remaining ancillae is restored to its initial value at the end of computation.
To calculation of each term of Equation 8 is done by either (i) Toffoli gate arrays or (ii) conditional adders. A conditional adder shall function if the control signal is asserted. For the example shown in Figure 15 if |Ctrl⟩ = 1, the circuit shall compute |X⟩ + |Y⟩, else |X⟩ and |Y⟩ pass through the circuit unchanged. Therefore, the circuit in Figure 15 calculates |X⟩ + |Ctrl⟩ · |Y⟩. Thus, conditional adders can be used to (i) implement each a · b term in equation 8 and (ii) perform the summation of these terms indicated in equation 8. The shifting by 2^i (see equation 8) can be accomplished with arrays of CNOT gates (see [79]) or via appropriate layout of the conditional adders as is the case in Figure 14 and works such as [31].

By using conditional adders that do not produce garbage outputs (such as the one shown in Figure 15), a multiplication circuit free of garbage outputs can be obtained. The multiplication circuit shown in Figure 14 produces no garbage output. The resource cost of this multiplication circuit depends on the resource usage of its building blocks. Therefore, by using conditional adders that enjoy low resource costs (such as low T-count), the multiplication circuit as a whole shall benefit.

### D. Division

#### Algorithm: Non-Restoring Division Algorithm

| Function Non-Restoring(a, b) |
|---|
| Requirements: a and b are 2’s complement positive values. |
| // Takes a and b as two n bit inputs. |
| // Returns a n bit quotient Q and |
| // a n − 1 bit remainder R. |
| 1 R = 0; |
| 2 Q = a_n−1; // a_{n−1} ∈ {0, 1}. |
| 3 // a_{n−1} is the most significant bit of a. |
| 4 Q = Q − b |
| 5 |
| 6 For i = 1 to n − 1 |
| 7 Q_{n−i} = Q_{n−i+1} |
| 8 Concatenate Q_{n−i+1} · · · Q_0 and R_{n−2} · · · |
| ⋯ R_{n−1−i} then store result in Y |
| 9 // Q_{n−i−1} is the most significant bit of Y. |
| 10 If (Q_{n−i} = 0) |
| 11 Y = Y + b |
| 12 Else |
| 13 Y = Y − b |
| 14 End |
| 15 End |
| 16 |
| 17 If (R < 0) |
| 18 R = R + b |
| 19 End |
| 20 Q_0 = Q_0 |
| 21 Return Q, R |

Fig. 16: Pseudo-code outline of the non-restoring division algorithm.

Figure 17 shows an example of a quantum division circuit. The circuit is composed of (i) a conditional adder, (ii) a subtraction circuit and (iii) a conditional addition and subtraction circuit. This circuit implements the non-restoring division algorithm. The non-restoring division algorithm (and its counterpart the non-restoring division algorithm) are well suited to be implemented on a quantum machine. Other algorithms (such as SRT division or serial implementations) are not suitable for quantum computation due to significant cost overhead. The building blocks of the division circuit shall be discussed before the operation of the entire division circuit is outlined.

Quantum conditional adders and quantum subtraction circuit were discussed in Section III-B and Section III-A. A quantum conditional addition and subtraction circuit executes addition or subtraction depending on a control signal. Figure 15 presents a generic example of a quantum addition and subtraction circuit. This example accepts two inputs stored in quantum registers |A⟩ and |B⟩. The result of computation Y shall appear on register |B⟩ at the end of computation. An additional qubit (|Ctrl⟩) contains the control signal. By placing arrays of CNOT gates (which operate on qubit |Ctrl⟩ and the register |B⟩) before and after a quantum addition circuit. The following computation takes place:

\[
Y = \begin{cases} 
|A⟩ + |B⟩ & \text{if } |Ctrl⟩ = 0 \\
|A⟩ - |B⟩ & \text{if } |Ctrl⟩ = 1 
\end{cases}
\] (9)

Thus, a quantum addition circuit (such as the one shown in Section III-A) can be made to perform either addition or subtraction.

The division circuit shown in Figure 17 takes two n bit numbers a and b that are 2’s complement positive binary numbers. a and b and n − 1 ancilla are applied as inputs to the circuit. At the end of computation, the quotient of \( \frac{a}{b} \) and the input a appear
E. Quantum Fourier Transform

Figure 18 shows a two qubit implementation of the quantum Fourier transform. The gate schematic and matrix representation are shown. The quantum Fourier transform equation shown in (11) is rewritten as follows:

$$|x⟩ = \frac{1}{\sqrt{2}} \sum_{y=0}^{3} α_y \cdot e^{\frac{2\pi i x y}{4}} |y⟩$$  

(10)

where $N = 4$ because two qubits can represent 4 states and $α_y$ is the probability of the quantum register being in state $y$. To generalize, for a register of $Z$ qubits, $N = 2^Z$ in Equation (10). We can calculate the final superposition state for the quantum register $|X⟩$ by evaluating Equation (10) for each state value $x$. At the end of computation, the state probabilities $(λ_0, λ_1, λ_2, λ_3)$ for the four possible states of $|X⟩ (|00⟩, |01⟩, |10⟩$ and $|11⟩)$ are given as:

$$
λ_0|00⟩ = \frac{1}{2} \cdot (α_0 + α_1 + α_2 + α_3) \\
λ_1|01⟩ = \frac{1}{2} \cdot (α_0 + 2α_1 \cdot e^{\frac{\pi i}{2}} + 2α_2 \cdot e^{\frac{3\pi i}{2}} + α_3 \cdot e^{\frac{3π i}{2}}) \\
λ_2|10⟩ = \frac{1}{2} \cdot (α_0 + α_1 \cdot e^{\frac{3π i}{2}} + α_2 \cdot e^{\frac{π i}{2}} + α_3 \cdot e^{\frac{π i}{2}}) \\
λ_3|11⟩ = \frac{1}{2} \cdot (α_0 + 2α_1 \cdot e^{\frac{3π i}{2}} + 2α_2 \cdot e^{\frac{π i}{2}} + α_3 \cdot e^{\frac{π i}{2}})
$$

(11)

Which can be cleaned up into the following:

$$
λ_0|00⟩ = \frac{1}{2} \cdot (α_0 + α_1 + α_2 + α_3) \\
λ_1|01⟩ = \frac{1}{2} \cdot (α_0 + j α_1 + α_2 + j α_3) \\
λ_2|10⟩ = \frac{1}{2} \cdot (α_0 - α_1 + α_2 - α_3) \\
λ_3|11⟩ = \frac{1}{2} \cdot (α_0 - j α_1 + α_2 - j α_3)
$$

(12)

As can be seen the calculation has manipulated the superposition state of the quantum register applied to the circuit. The transformation shown in equations (11) can be represented in matrix form and is shown in Figure 18. The matrix transformation can be implemented in terms of quantum gates and the schematic is shown in Figure 18. The circuit is based on the Hadamard gate and a controlled version of the phase gate. This controlled phase gate is like the CNOT gate in that if the control qubit is one, then the phase gate operation $

\begin{bmatrix} 1 & 0 \\ 0 & i \end{bmatrix}

$ is performed on the target qubit. For additional details on the quantum Fourier transform and additional circuits which operate on quantum registers containing transform domain values, the reader is encouraged to see [39, 83, 86].
A. Resource Cost Calculations for a Circuit for a Fault Tolerant Quantum Computer

For this example, we shall seek to calculate the T-count, T-depth, garbage output, qubit cost and \(KQ_T\) for the quantum addition circuit presented in Section III-A and shown in Figure 11. The measures T-count, T-depth, qubit cost and \(KQ_T\) have been introduced in Section II-B. The quantum adder is composed of functional blocks (called Unmajority and Add (\(UMA\)) and Majority (\(MAJ\))) which in turn are constructed of Toffoli and CNOT gates (see Figure 11). Once a quantum circuit has been decomposed in terms of logic gates (i.e. Toffoli and CNOT gates), we can proceed to determine the cost measures. The CNOT gate is already a member of the Clifford+T gate family (see Figure 3) while the Toffoli gate needs to be decomposed into a Clifford+T gate implementation. We shall use the implementation shown in Figure 5c and presented in [23]. Having decomposed the circuit from a top level description to its Clifford+T gate circuitry, we can follow the procedure below to compute the T-depth and T-count.

### Procedure to calculate T-Count and T-Depth

- **Step 1:** Decompose the top-level circuit to its equivalent Clifford+T gate networks. As needed decompose circuit to submodules or logic gates to simplify the decomposition.
- **Step 2:** Calculate the T-count and T-depth for any submodules or logic gates from Step 1.
- **Step 3:** Calculate the T-count and T-depth for the whole circuit using results from Step 2.

Thus, we shall now calculate the T-count and T-depth of the Toffoli gate. The Clifford+T gate implementation of the Toffoli gate is repeated in Figure 5c.

### T-Depth of the Toffoli Gate

![Three T gate layers: T-Depth 3](image)

Fig. 19: Clifford+T gate implementation of the Toffoli gate illustrating the T-depth (and the corresponding gate layers). Implementation presented in [23].

To calculate T-count, we count the number of T gates in the Toffoli gate circuit. As shown in Figure 19, the T-count is 7. To calculate T-depth, we shall follow the procedure presented in [87] [23] [88]. In [87] [23] [88], the circuit is viewed as a series of gate layers (where a gate layer consists of quantum gates that run in parallel). Thus, the T-depth is the number of gate layers which contain 1 or more T gates. For the Toffoli gate in Figure 19, the T-depth is 3.

We can now consider the costs of the \(MAJ\) and \(UMA\) functional blocks (see Figure 11). As shown in Figure 11 both of these functional units contain 1 Toffoli gate apiece and the remaining gates are CNOT gates. For both the \(MAJ\) and \(UMA\) functional blocks, the T-count is 7 and the T-depth is 3. Now we can turn our attention to the adder itself. As shown in Figure 11 the quantum adder consists of \(n\) \(MAJ\) units in series (on a diagonal), a CNOT gate and finally \(n\) \(UMA\) units in series (again on a diagonal). The T-count is given as the total of \(MAJ\) and \(UMA\) functional blocks multiplied by the T-count per functional block. The mathematical computation is as follows:

\[
7 \cdot (2 \cdot n) = 14 \cdot n. \quad (13)
\]

Since the \(MAJ\) and \(UMA\) functional blocks are in series, these modules form \(2 \cdot n\) layers. Each layer contains a Toffoli gate with an associated T-depth of 3. Therefore, for this circuit the T-depth is given as the total of \(MAJ\) and \(UMA\) functional blocks multiplied by the T-depth per functional block. The mathematical computation is as follows:

\[
3 \cdot (2 \cdot n) = 6 \cdot n. \quad (14)
\]

We still need to compute the garbage output cost, qubit cost and \(KQ_T\) metrics for the quantum circuit. We shall calculate qubit cost first because with the qubit cost, we shall be equipped to calculate the remaining measures. Since the number of qubits required by a quantum circuit remains constant, we have two methods at our disposal to compute the qubit cost:

### Methods to Calculate Qubit Count

- **Method 1:** Qubit cost = ancillae + primary inputs
- **Method 2:** Qubit cost = garbage output + circuit outputs (where circuit outputs include primary inputs and restored ancillae)

We shall use Method 1. The quantum adder takes two \(n\) bit inputs and requires two ancillae (see Figure 11 and Section III-A). Hence the qubit cost is given as:

\[
2 \cdot n + 2 \quad (15)
\]

Now we can turn our attention to the garbage output cost. At the end of computation, the quantum adder produced a \(n + 1\) sum value, the remaining ancilla is restored to 0 and one of the \(n\) bit inputs is restored (see Section III-A). To determine the garbage output, we solve the Method 2 expression of qubit cost for the garbage output term. As a result, we obtain the following calculation:

\[
(2 \cdot n + 2) - (n + 1) - n - 1 \rightarrow 0 \quad (16)
\]
As shown in Equation 15, the addition circuit is free of garbage output. The $KQ_T$ measure is calculated as the product of the T-depth ($K$) and qubit cost ($Q$). The qubit cost is in Equation 15 and T-depth is in Equation 14. Thus the $KQ_T$ measure is given as:

\[(6 \cdot n) \cdot (2 \cdot n + 2) = 12 \cdot n^2 + 12 \cdot n \quad (17)\]

B. Resource Cost Calculations for a Circuit for Noisy Intermediate Scale Quantum Computers

For this example, we now consider the cost measures for quantum circuits that shall run on NISQ machines. Thus, we shall illustrate the calculation of the CNOT-count, CNOT-depth, qubit cost, garbage output and $KQ_{CNOT}$. These measures were presented in Section II-B and in Figure 9. We shall consider the conditional adder presented in Figure 15 in Section III-C for our computations. We begin by decomposing the circuit. The conditional addition circuit is composed of fundamental building blocks (labeled CUMA and CMAJ). These functional blocks in turn can be decomposed to Toffoli and CNOT gates. We note that the CNOT gate is already a Clifford+T gate and we shall use the Clifford+T gate implementation of the Toffoli gate shown in Figure 5c and presented in [23]. We are now in a position to calculate CNOT-count and CNOT-depth and shall use a procedure to calculate these measures with is identical to the example for fault tolerant quantum machines:

\[
\begin{align*}
\text{CNOT-Depth of the Toffoli gate} \\
\text{Seven CNOT gate layers : CNOT-Depth 7}
\end{align*}
\]

\[
\text{Fig. 20: Illustration of the Clifford+T implementation of the Toffoli gate. The gate layers with CNOT gates are shown.}
\]

We shall begin with the Toffoli gate implementation shown in Figure 20. To determine CNOT-count, we count up the CNOT gates used in the circuit. For the example shown in Figure 20, the CNOT-count is 7. To calculate CNOT-depth, we again view the circuit as a series of gate layers. As shown in Figure 20, we see that seven gate layers contain CNOT gates. Thus, CNOT-depth is 7. With the CNOT-count and CNOT-depth of the Toffoli gate found, we can now proceed to larger building blocks. The conditional adder is composed of Controlled Majority (CMAJ) and Controlled Unmajority and Add (CUMA) functional blocks (see Figure 15). The CMAJ building block consists of 2 Toffoli gates and a CNOT gate. The logic gates are in series. Thus, the CNOT-count is $7 \cdot 2 + 1 = 15$ and the CNOT-depth is $7 \cdot 2 + 1 = 15$. Likewise, the CUMA also is constructed from 2 Toffoli gates and a CNOT gate. These are also in series. As a result the CNOT-count is 15 and the CNOT-depth is 15.

Now we can turn our attention to the quantum conditional adder itself. The quantum conditional adder consists of $n$ CMAJ units in series (on a diagonal), a Toffoli gate, then $n$ CUMA units in series (again on a diagonal). All gates are in series meaning each building block listed forms a gate layer. Thus, the CNOT-count is given as the total of the Toffoli gate, CMAJ and CUMA functional blocks multiplied by the CNOT-count per functional block. Each CUMA and CMAJ module has a CNOT-count of 15 each and the Toffoli gate has a CNOT-count of 7. The computation is as follows:

\[
15 \cdot n + 15 \cdot n + 7 \rightarrow 30 \cdot n + 7 \quad (18)
\]

To calculate CNOT-depth, note that the CMAJ blocks, Toffoli gate and CUMA blocks are in series. Thus, the total CNOT-depth is the sum total of the CNOT-depths of these functional blocks. Each CUMA and CMAJ module has a CNOT-depth of 15 each and the Toffoli gate has a CNOT-depth of 7. The computation of total CNOT-depth is as follows:

\[
15 \cdot n + 15 \cdot n + 7 \rightarrow 30 \cdot n + 7 \quad (19)
\]

Now we can turn our attention to the qubit cost, garbage output cost and $KQ_{CNOT}$ measures. We shall first calculate the qubit cost. We calculate the qubit cost by finding the sum of the two $n$ bit inputs and three ancillae. Thus, we shall use Method 1 (Qubit cost = ancillae + primary inputs). The expression for the qubit cost is given as:

\[
2 \cdot n + 3 \quad (20)
\]

To calculate garbage output, we take the total qubit cost and subtract $n + 1$ qubits occupied by the output, $n$ qubits holding one of the original operands, the qubit $|\text{Ctrl}|$ and all ancillae that are restored to their initial values. Thus, the garbage output is calculated as:

\[
(6 \cdot n) \cdot (2 \cdot n + 2) = 12 \cdot n^2 + 12 \cdot n
\]
V. APPLICATION OF QUANTUM ARITHMETIC CIRCUITS IN QUANTUM ALGORITHMS

The arithmetic units presented in this work can be combined into more complex functional blocks for use in quantum algorithms. We present an example where quantum circuits for addition and multiplication are arranged into a functional block that performs image rotation. The design presented in [39] is shown. We present a quantum implementation of image rotation because quantum computing for image processing applications has caught the attention of researchers. The availability of quantum circuits for image processing applications can benefit because quantum computing for image processing applications

Equation 21 indicates that the conditional adder produces no garbage output. The $KQ_{\text{CNOT}}$ measure is the product of qubit cost $Q$ and the CNOT-depth $K$. Having already calculated qubit cost and CNOT-depth we can present the $KQ_{\text{CNOT}}$ as:

$$ (2 \cdot n + 3) - (n + 1) - (n + 1) - 1 \rightarrow 0 \quad (21) $$

$$ (30 \cdot n + 7) \cdot (2 \cdot n + 3) = 60 \cdot n^2 + 104 \cdot n + 21 \quad (22) $$

V. APPLICATION OF QUANTUM ARITHMETIC CIRCUITS IN QUANTUM ALGORITHMS

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In this Section, we present a quantum circuit for the computation of image rotation that is presented in [39]. The circuit is designed to operate on image information encoded on qubits using the Novel Enhanced Quantum Representation (NEQR) [93]. Details on NEQR can be seen in [93]. The rotation operation only works with the pixel location information of the image. In NEQR, the image location information is stored in two quantum registers (see [39]). The presented circuit uses quantum circuits for addition, subtraction and multiplication (such as those presented in this work) as building blocks.

Given an image pixel with coordinates $x_0, y_0$, the quantum image rotation circuit performs the following computations:

$$ y_t = \cos(\theta) \cdot y_0 + \sin(\theta) \cdot x_0 $$
$$ x_t = -\sin(\theta) \cdot y_0 + \cos(\theta) \cdot x_0 \quad (23) $$

where $\theta$ is the rotation angle and the sign indicates the direction of rotation (− counter-clockwise and + clockwise) [39]. Equation 24 can be presented in terms of matrices as:

$$ \begin{bmatrix} y_t \\ x_t \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \cdot \begin{bmatrix} y_0 \\ x_0 \end{bmatrix} \quad (24) $$

The design methodology used in [39] to implement equation 24 splits the rotation task into three separate shearing operations. Figure 21 shows a top level implementation of the rotation circuit where $x_s, y_s$ are the final image pixel location coordinates. Also, $\tan(\theta) = \alpha, \sin(\theta) = \beta, X_{\text{ref}}$ and $Y_{\text{ref}}$ are constants which corresponds to the center of rotation. By splitting the rotation into three shearing operations, equation 24 can be rewritten in terms of three shearing operations as now shown:

$$ \begin{bmatrix} y_t \\ x_t \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \tan(\theta/2) & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & -\sin(\theta) \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ \tan(\theta/2) & 1 \end{bmatrix} \cdot \begin{bmatrix} y_0 \\ x_0 \end{bmatrix} \quad (25) $$

where $\theta$ is the rotation angle. The transformation matrix $\begin{bmatrix} 1 & 0 \\ \tan(\theta/2) & 1 \end{bmatrix}$ represents the following horizontal shear translation:

$$ (x, y) = (x + y \cdot \tan(\theta/2), y) \quad (26) $$

The transformation matrix $\begin{bmatrix} 1 & -\sin(\theta) \\ 0 & 1 \end{bmatrix}$ represents the following vertical shear translation:

$$ (x, y) = (x, y - x \cdot \sin(\theta/2)) \quad (27) $$

The choice of the centroid of rotation $X_{\text{ref}}$ or $Y_{\text{ref}}$ is a design choice. In [39], the centroid corresponds to the center
pixel location values of the image. For the case of image centroids ($X_{ref}$ or $Y_{ref}$) within the range of pixel location values, the final image shearing in the vertical direction becomes:

$$ (x, y) = \begin{cases} 
(x, y + (X_{ref} - x) \cdot \sin(\theta)) & \text{if } y \in [y_0, y_k] \\
(x, y - (x - X_{ref}) \cdot \sin(\theta)) & \text{if } y \in [y_{i+1}, y_{n-1}] 
\end{cases} $$

(28)

The final image shearing in the horizontal direction becomes:

$$ (x, y) = \begin{cases} 
(x - (Y_{ref} - y) \cdot \tan \left(\frac{\theta}{2}\right), y) & \text{if } x \in [x_0, x_i] \\
(x + (y - Y_{ref}) \cdot \tan \left(\frac{\theta}{2}\right), y) & \text{if } x \in [x_{i+1}, x_{n-1}] 
\end{cases} $$

(29)

We require quantum arithmetic circuits for multiplication addition and subtraction. For each expression shown in Equations 28 and 29 an independent circuit is created.
A. Quantum Circuits for Horizontal and Vertical Shear Operations

Figures 23 illustrates the circuit to implement the horizontal shear for the case of images pixels located at values greater then the centroid value $X_{ref}$. The circuit shown calculates equation (26) where $\alpha = \tan \left( \frac{\theta}{2} \right)$. Figure 23 illustrates the circuits to implement the vertical shear for the case of images pixels located at values greater then the centroid value $Y_{ref}$. The circuit shown calculates equation (27) and $\beta = \sin(\theta)$. The circuits take as input the pixel location values $(x, y)$. The sinusoidal terms $\alpha = \tan \left( \frac{\theta}{2} \right)$ for the horizontal shear and $\sin(\theta) = \beta$ for the vertical shear are provided as inputs to the circuit. The purpose of the interpolation module (labeled IP in the Figures) is to round any fractional results from multiplication to the nearest whole number. An interpolation circuit such as those shown in [40] [94] can be used to implement this functional block.

The horizontal shear circuit shown in Figure 24 computes Equation 29 with four steps which are as follows. Figure 24 shows the quantum circuitry for the case of $x > X_{ref}$ where $X_{ref}$ is the centroid of rotation.

- **Step 1:** If $x \leq X_{ref}$, use a quantum subtraction circuit compute $Y_{ref} - y$. If $x > X_{ref}$, use a quantum subtraction circuit compute $y - Y_{ref}$.
- **Step 2:** With a quantum controlled multiplication circuit, multiply the result of Step 1 by $\tan \left( \frac{\theta}{2} \right)$.
- **Step 3:** With a quantum circuit implementation of the interpolation operation, round the result of Step 2 to the nearest integer
- **Step 4:** If $x \leq X_{ref}$, use a quantum subtraction circuit to subtract $x$ by the result of Step 3. If $x > X_{ref}$, use a quantum addition circuit to add $x$ by the result of Step 3.

Similarly, the vertical shear circuit shown in Figure 25 computes Equation 28 with four steps which are as follows. Figure 25 shows the quantum circuitry for the case of $y > Y_{ref}$ where $Y_{ref}$ is the centroid of rotation.

- **Step 1:** If $y \leq Y_{ref}$, use a quantum subtraction circuit compute $X_{ref} - x$. If $y > Y_{ref}$, use a quantum subtraction circuit compute $x - X_{ref}$.
- **Step 2:** With a quantum controlled multiplication circuit, multiply the result of Step 2 by $\sin \left( \frac{\theta}{2} \right)$
- **Step 3:** With a quantum circuit implementation of the interpolation operation, round the result of Step 2 to the nearest integer
- **Step 4:** If $y \leq Y_{ref}$, use a quantum subtraction circuit to subtract $y$ by the result of Step 3. If $y > Y_{ref}$, use a quantum addition circuit to add $y$ by the result of Step 3.

VI. Conclusion

This work introduces the design and evaluation of quantum circuits which can, in turn, be used to implement quantum algorithms. We start with a brief introduction to quantum computation illustrating, at a high level, fundamental properties of quantum computers (superposition, entanglement, measurement and unitarity). Then, our discussion introduces quantum operations (or gates) used to implement the quantum circuits shown in this work. We focus on the Clifford+T

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**Fig. 24:** Quantum circuit for the horizontal shear of images for pixel located at values greater then the centroid value. Adapted from [39].

**Fig. 25:** Quantum circuit for the vertical shear of images for pixel located at values greater then the centroid value. Adapted from [39].
gate set as there exists fault tolerant implementations for all these gates. Our discussion of gates also illustrates how we can combine the Clifford+T gates to synthesize higher level logic gates. After gates are introduced, the measures we use to evaluate the resource usage of quantum circuits is presented. Fault tolerant quantum computation and circuits for NISQ machines have differing sets of measures and we introduce them. Having seen examples of basic logic gates used in quantum computation, we now turn our attention to the design of quantum circuits for basic operations. Arithmetic functions (addition, subtraction, multiplication and division) are chosen because many quantum algorithms make use of at least one of these arithmetic functions (see [8] [10] [12]). For each circuit, we show the high level architecture and summarize how the logic gates shown previously are combined to form these arithmetic circuits. We also describe how the arithmetic units perform their functions. Afterward, we turn our attention to how we calculate the resource costs of quantum circuits such as quantum circuits for arithmetic. We show the calculations of the resource cost measures for both NISQ and fault tolerant computers using quantum arithmetic circuits as examples. We conclude by illustrating how building blocks (such as quantum arithmetic circuits) can be used to implement data paths for quantum algorithms. We present the quantum circuit implementation of the image rotation operation. The image rotation operation is a fundamental step for higher level image processing algorithms.

The design of quantum computers is at an exciting stage. The development of new algorithms is an active area of research and shall continue to be so in the near future. There already exist quantum computers of sufficient size to begin implementing quantum algorithms and circuits (albeit at a small scale). Work continues to enlarge the size of the available quantum machines and improve the underlying technology. New platforms (such as quantum dots or anyons [25] [96]) are being examined for their potential use in the development of quantum machines. To be able to realize the performance gains promised by proposed quantum algorithms, quantum circuits and quantum data paths must be developed. This article presents an introduction to the design and resource cost assessment of quantum circuits. This article also presents an end-to-end implementation of a larger quantum data path system from basic gates to complete system. We conclude that this article can provide a road map for scholars who wish to contribute to the field of quantum circuit design.

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