Limit of Field Effect Mobility on Pentacene Single Crystal

V.Y. Butko*, X. Chi, D. V. Lang and A. P. Ramirez
Los Alamos National Laboratory, Los Alamos, New Mexico, USA

We report on fabrication and characterization of field effect transistors (FETs) on single-crystal pentacene. These FETs exhibit hole conductivity with room temperature effective mobility, $\mu_{\text{eff}}$, up to 0.30 cm$^2$/Vs and on/off ratios up to $5 \times 10^6$. A negative gate voltage of $-50$V significantly decreases the activation energy ($E_a$) down to 0.143 eV near room temperature. Assuming thermal equilibrium between trapped and free carriers, from $E_a = 0.143$eV, we find the number of free carriers is only 0.4% of the total number of injected carriers. Along with $\mu_{\text{eff}} \sim 0.3$ cm$^2$/Vs this gives the intrinsic free carrier mobility of $\sim 75$ cm$^2$/Vs.

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The Field Effect Transistor (FET), based on controlled injection of free carriers into semiconductors, is probably the most prominent constituent of modern microelectronics\textsuperscript{1}. Semiconducting organic materials have received increased attention in the last several years because they promise bulk processing of flexible, large-area devices at low cost\textsuperscript{2-5}. FETs also provide a powerful method of investigating two-dimensional physical properties of these materials. However, the flexibility of organic materials is also related to the difficulties encountered in reproducing the well-known results obtained in inorganic semiconductors. Unlike inorganic materials, organics possess intrinsic inter- and intra-molecular vibrational modes that have the potential to scatter charge carriers, and reduce mobility, $\mu$, more effectively than usual phonons. Assessing the fundamental limits on free carrier mobility in organic systems is one of the major problems of the physics of organic solids.

Among the most interesting of organic systems are the polyacenes, with pentacene as the most prominent member\textsuperscript{2}. Pentacene has the smallest bandgap among the linear polyacenes, and the highest effective mobility in polycrystalline organic thin film FETs, $\mu_{\text{eff}} = 0.3-1.5 \text{ cm}^2/\text{Vs}$\textsuperscript{5-7}. This value is comparable to that of amorphous Si devices. It is known that $\mu_{\text{eff}}$ increases with increasing crystallinity in such thin film transistor (TFT) devices\textsuperscript{4,6-8}. This result and tremendous improvement of $\mu$ in inorganic crystals compare to disorder systems motivates the need for results on FETs fabricated from organic single crystals.

In this work we fabricate and study FETs formed on the surface of high-quality pentacene single crystals. These crystals were grown by horizontal physical vapor transport in a stream of ultra high purity argon. The crystal growth apparatus was a modified version of the one reported by Laudise et. al.\textsuperscript{9} with two glass tubes of different diameters. The outer one was wrapped with two rope-heaters which define the source zone and crystal growth zone, respectively. A glass
tube of smaller diameter serves as the reactor tube. The source temperature was 285 C, and the 
flow rate was 19 ml /min. The source material was purchased from Aldrich and was twice re-
crystallized in argon for purification before used for crystal growth. Typical crystal dimensions 
are 1-2 mm length, 0.2 – 1 mm width and 0.05 – 0.5 mm thickness. In this work we use two 
types of source/drain contact configurations: colloidal graphite/colloidal graphite and colloidal 
graphite/silver paste. Both of these configurations have been painted on the smooth, untreated 
single crystal surface. The separation between contacts is ~100 µm. The width of the contact 
pads is ~0.3 mm. Similar to the approach used in\textsuperscript{10} on rubrene, the organic parylene was used as 
gate insulator (400-500 nm thick). Parylene was deposited on the top of the crystal in a home- 
made reactor. The thickness of the parylene layer is estimated from the capacitance of planar 
devices fabricated simultaneously with the pentacene devices. In the final step of FET 
fabrication, a silver paste gate contact electrode was painted on the top of the parylene over the 
region between the source and drain. No devices have been annealed. The current and voltage 
were measured with two Keithley 6517A electrometers. The electrical measurements were made 
in darkness in a Quantum Design cryostat at fixed temperature in a vacuum ~ 10\textsuperscript{-5} Torr. For these 
measurements, a 1-20 Volt step and a 5-60 second delay between each measurement was typical. 
Leakage gate current at the low voltages was ~10\textsuperscript{-14}-10\textsuperscript{-13} A, and at the highest voltages applied, 
ever exceeded 3×10\textsuperscript{-12} A.

Typical transistor characteristics of devices at room temperature are shown in fig.1-2. The 
drain current (I\textsubscript{sd}) exhibits a linear dependence on source-drain voltage (V\textsubscript{sd}) at fixed gate 
voltages (V\textsubscript{g}) (Fig.1) when V\textsubscript{sd} < V\textsubscript{g}. For V\textsubscript{sd} ≥ V\textsubscript{g} the current saturates at a near-constant value. 
This is standard behavior of a semiconductor FET\textsuperscript{11}. In the right hand side of fig. 2, is shown I\textsubscript{sd}- 
V\textsubscript{g} characteristics at fixed V\textsubscript{sd}. One can see that the on-off ratio reaches 5×10\textsuperscript{6} at low V\textsubscript{sd}. From
the left-hand side of Fig.2, which shows the dependence of \((-I_{sd})^{1/2}\) on \(V_g\), we extract an effective mobility \(\mu_{eff} \sim 0.30 \text{ cm}^2/(\text{Vs})\) at \(V_{sd} = -50 \text{ V}\) and threshold voltage \(V_t \sim 5\text{ V}\). Our measurements on a sample with colloidal graphite/silver paste contacts also demonstrate FET action with a few times less mobility.

In Fig. 3 are shown results of a variable-temperature study of a pentacene single crystal FET at different values of \(V_g\). We fit these data to the form \(R = R_0\exp(-E_a/T)\), where \(E_a\) is an activation energy, and also plot \(E_a\) as a function of \(V_g\) in fig. 4. We see that for slightly positive \(V_g\), in room temperature range \(E_{a0} \sim 0.57 \text{ eV}\), a value approximately 30% of the optical activation energy of \(2 \text{ eV}\). This is most likely due to an asymmetric distribution of traps which pin the Fermi level toward the valence band. For large negative \(V_g\) (-50V), \(E_a\) decreases to a significantly lower value, but still a thermally activated transport (\(E_{a1} = 0.143 \text{ eV}\)) is observed. This behavior appears to be different from both the TFT results which exclude thermally activated hopping as the fundamental transport mechanism in pentacene thin films and the low temperature results of photoinduced carrier time-of flight (TOF) technique on naphthalene crystals, described by a band model. However, it is very likely that carrier trapping masks the intrinsic transport behavior in our crystals. To reveal the fundamental free carrier crystal mobility, the following analysis can be applied. The observed behavior is well described in terms of a standard semiconductor model assuming that holes injected from the contacts become trapped at and below the Fermi energy level \((E_F)\) inside the band gap. In this picture \(E_a \sim E_F - E_V\) and the dependence of \(E_a\) on \(V_g\) corresponds to a gradual shift of the hole Fermi energy toward the valence band as more empty shallow traps become filled due to FET hole injection. Therefore the number of injected carriers per unit area

\[
C_s V_g \approx \int_{E_{F1}}^{E_{F0}} \text{d}E N_i(E)
\]

(1)
where $N_t(E)$ is energy distribution function of traps (trapped carriers) per unit area. $E_{F0}$ and $E_{F1}$ are Fermi energy levels without and with $V_g$ on, correspondently. We assume that, at any injection rate, thermal equilibrium is established between free and trapped carriers\textsuperscript{14,16}. The number of thermally excited free carriers is given by

$$p_f = \int_{E_{F1}}^{E_c} dE N_t(E) \exp((-E_{F1} - E) / k_B T).$$

Due to an exponential decrease of the thermal excitation term from the deep trapped carriers, the $E_c$ (conduction band energy) integral limit can be changed to $E_{F0}$ without a significant error at room-temperature. Obtained expression can be overestimated by the following

$$p_f = \exp((-E_{F1} - E_{F1}) / k_B T) \int_{E_{F1}}^{E_{F0}} dE N_t(E) \approx \exp(-E_{a1} / k_B T) C_s V_g.$$

From this equation and $E_{a1} = 0.143$ eV at $V_g = -50$ V, we find that at room temperature the number of free carriers is about or less than 0.4% of the total number of injected carriers. This fact along with $\mu_{\text{eff}} \sim 0.3$ cm$^2$/Vs gives a free carrier mobility $\mu \sim 75$ cm$^2$/Vs. We note that $\mu_{\text{eff}}$ has been studied in the FET configuration in rubrene crystals\textsuperscript{10} and $\mu$ by the TOF technique on other crystals\textsuperscript{13,18,19}. The FET results on rubrene, $\mu_{\text{eff}} \sim 0.1 - 1$ cm$^2$/Vs, are not inconsistent with our present results. The TOF results demonstrate a significant increase of intrinsic mobility above values of $\mu_{\text{eff}}$ reported for TFTs. However, a direct confrontation of FET and TOF results for the same material (and same batch) have yet to be made.

As mentioned above, the crystals we studied have a large density of traps. It is conceivable that some of these traps are introduced in the process of FET fabrication, which has not been optimized. Of course, decreasing the number of traps would significantly improve the device characteristics, which remains the ultimate goal of single-crystal device project. On the
other hand, this work presents the first fabrication and study of pentacene single crystal FETs
and the first experimental indication that room temperature intrinsic pentacene mobility can be as
high as 75 cm$^2$/Vs.

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* On leave from Ioffe Physical Technical Institute, Russian Academy of Science, Russia

1 G. Horowitz, Advanced Materials 10, 365-377 (1998).
2 A. R. Volkel, R. A. Street, and D. Knipp, Physical Review B 66, 195336-1-195336-8
   (2002).
3 S. Forrest, P. Burrows, and M. Thompson, IEEE Spectrum 37, 29-34 (2000).
4 I. H. Campbell and D. L. Smith, Solid State Physics 55, 1-117 (2001).
5 Y. S. Yang, S. H. Kim, J. Lee, H. Y. Chu, L. M. Do, H. Lee, J. Oh, and T. Zyung,
   Applied physics letters 80, 1595-1597 (2002).
6 S. F. Nelson, Y. Y. Lin, D. J. Gundlach, and T. N. Jackson, Applied physics letters 72,
   1854-1856 (1998).
7 H. Klauck, D. J. Gundlach, J. A. Nichols, and T. N. Jackson, IEEE Transaction on electron
devices 46, 1258-1263 (1999).
8 D. J. Gundlach, Y. Y. Lin, T. N. Jackson, S. F. Nelson, and D. G. Schlom, IEEE Electron
   Device Letters 18, 87-89 (1997).
9 K. C. Laudise R.A., Simpkins P.G., Siegrist T., Journal of crystal growth 187, 449-454
   (1998).
10 V. Podzorov, V. M. Pudalov, and M. E. Gershenson, Applied physics letters 82, 1739-
   1741 (2003).
11 S. M. Sze, Physics of semiconductor devices, Vol. New York, Chichester, Brisbane,
   Toronto, Singapore, 2 ed. ( John Wiley & sons, Inc., 1981).
12 M. Pope and C. E. Swenberg, Electronic processes in organic crystals and polymers.,
   Vol. 56, second ed. (Oxford University Press, New York, Oxford, 1999).
13 W. Warta and N. Karl, Physical Review B 32, 1172-1182 (1985).
14 D. P. Horowitz G., Journal of Applied Physics 70, 469-475 (1991).
15 G. Horowitz, M. E. Hajlaoui, and R. Hajlaoui, Journal of Applied Physics 87, 4456-4461
   (2000).
16 S. J. Nespurek S., Phys. Stat. sol. (a) 41, 619 (1977).
17 H. W. Kao K.C., Electrical transport in solids, Vol. 14, 1 ed. (Pergamon press, Oxford,
   New York, Toronto, Sydney, Paris, Frankfurt, 1981).
18 N. Karl, Mol. Cryst. Liq. Crystl. 171, 157-177 (1989).
19 N. Karl, Journal of crystal growth 99, 1009-1016 (1990).
Pentacene #45, T = 300 K, graphite-graphite contacts

FIG. 1.

$I_{sd} (V_{sd})$ FET characteristics at different $V_g$. 
Pentacene #45, T = 300 K, graphite-graphite contacts

FIG. 2.

Right hand side: $-I_{sd}(V_g)$ FET characteristics at different $V_{sd}$. Left hand side: $(\frac{-I_{sd}}{2})^{1/2}(V_g)$ FET characteristic at $V_{sd}=-50\,\text{V}$.

$\mu_{\text{eff}} = 0.30 \, \text{cm}^2/(V\cdot\text{s})$
FIG. 3.

Main Part: Dependence of \(-I_{sd}(V_g)\) on 1/Temperature at \(V_{sd} = -40\) V

Inset: Dependence of \(E_a\) on \(V_g\) in 200K-300K temperature range.

Pentacene #45, 
\(V_{sd} = -40\) V, 
graphite-graphite contacts