Novel channel edge doping for hump reduction in LTPS TFTs

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ABSTRACT
We proposed a new channel edge doping (CED) technique for hump reduction in n-type low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) and validated it through experiments and technology computer-aided design (TCAD) simulations. The TCAD simulations indicate that the hump effect in LTPS TFTs is due to the high electron ($e^-$) concentration ($\sim 10^{16}$ cm$^{-3}$) induced by an enhanced electric field (e-field) at the channel edge region along the width direction. In order to reduce the hump effect, we focused on decreasing the $e^-$ concentration at the channel edge. The CED process led to the selective control of the $e^-$ concentration at the channel edge. The decrease in the maximum $e^-$ concentration from $3.4 \times 10^{16}$ to $2.9 \times 10^{14}$ cm$^{-3}$ at the channel edge using CED led to an effective reduction in the hump characteristic of LTPS TFTs. Furthermore, the CED process does not require any additional masks and is highly effective in hump reduction, rendering it beneficial for manufacturing active-matrix organic light-emitting diode displays.

1. Introduction
Low-temperature polycrystalline silicon (LTPS) has attracted great interest as a backplane material for high-performance thin-film transistors (TFTs) that are used in the active-matrix organic light-emitting diode (AMOLED) display industry, owing to their excellent device performance and stability [1–3]. However, there are still some important issues with LTPS TFTs, one of which is the 'hump' characteristic that causes an abnormal increase in current in the sub-threshold regime of transfer curves [4–7]. In AMOLED displays, non-uniform brightness at low grayscale is caused by the deviation of anomalous electrical characteristics, such as the hump phenomenon, which occurs significantly at low current levels in the sub-threshold region of the Dr-TFT [8,9]. Therefore, it is especially important to eliminate the hump characteristics of LTPS TFTs for the high image quality of OLED products. Previous studies have reported that the primary cause of the hump phenomenon is the channel edge effect [10–12]. Channel edge effect occurs when the electric field (e-field) is intensely enhanced at the corner of the channel edge in the width direction, which is called the taper region. In the enhanced e-field region, electrons flow and form redundant additional channels in the LTPS TFTs. In order to eliminate the channel edge effect, previous research has mostly focused on structural engineering, thereby forming a specific shape to decrease the e-field in the taper region by the etch step active (ESA) structure and the rounded profile [10,11]. However, the process for controlling the shape of the taper complicates the conventional manufacturing process of the LTPS TFTs, and it is difficult to fabricate the taper structure uniformly over the entire panel area.

In this study, we propose a channel edge doping (CED) process for the LTPS TFTs to overcome the aforementioned limitations of the structural approaches in order to eliminate the hump issue. The CED technique does not require any additional masks, and facilitates the uniform modulation of the LTPS channel over the entire panel area. We have successfully demonstrated that by employing the CED process, the hump characteristic of the LTPS TFTs can be reduced. We have analyzed the mechanism of hump removal by using three-dimensional (3D) technology computer-aided design (TCAD) simulation and suitably designed experiments in order to validate the CED process in the LTPS TFTs with a taper angle of approximately 45° [10].
2. Experiments

Figure 1(a) illustrates the schematic of the top-gate coplanar n-type LTPS TFT structure used in the experiments, as well as in the 3D TCAD simulation, in order to analyze the hump effect. Figure 1(b) shows the top view, whereas Figure 1(c) and (d) illustrate the cross-sectional views along the length and width directions, respectively. The taper region is indicated in Figure 1(d). The LTPS TFT devices have channel widths and lengths of 3.5 and 20 µm, respectively, and were fabricated by using the conventional LTPS process [13]. In order to analyze the mechanism of the hump phenomenon of the LTPS TFTs and to verify our CED process, TCAD simulation was performed by using Silvaco 3D TCAD process and device simulation tools. Fabrication processes, such as deposition, etching, and ion implantation for the coplanar structure of the LTPS TFTs were defined by using process simulation. The doping process conditions applied in the simulation were the same as those in the experiments presented in Table 1.

The comparison between the conventional channel doping and CED processes is shown in Figure 2. In the conventional channel doping process, ion implantation with boron is usually performed after the removal of the photoresist, as illustrated in Figure 2(a). In addition to the steps followed in the conventional channel doping process, the CED process involves an additional channel doping step, which is defined as taper doping (Figure 2(b)). In the CED process, the first boron implantation is performed before the photoresist is removed, followed by a second boron implantation step after its removal. Consequently, the CED process results in a higher level of doping in the taper region than in the main channel region, while the conventional channel doping results in equal concentration of boron in the entire channel region. The conditions for the CED process are presented in Table 1.

The transfer curves of the LTPS TFTs fabricated by the conventional channel doping and the CED process were measured in the dark at room temperature using a B1500A semiconductor device parameter analyzer. During the measurements, the gate voltage (VGS) was swept from −5 to +10 V, while the drain voltage (VDS) was fixed at 0.1 and 10 V, and the source electrode was grounded.

3. Results and discussion

3.1. Measured hump characteristic

Figure 3(a) illustrates the transfer characteristics with the threshold voltage (VTH) of 2.2 V measured at VDS = 0.1 and 10 V in LTPS TFTs with the conventional channel doping process. The hump phenomenon, which

| Table 1. Conditions for CED Process in LTPS TFTs |
|-----------------------------------------------|
| Doping Process | Impurity | Dosage [cm⁻²] | Energy [eV] |
|----------------|----------|---------------|-------------|
| Taper Doping   | Boron    | 4 x 10¹²      | 10k         |
| Channel Doping | Boron    | 1 x 10¹²      | 40k         |
| n⁺ Doping      | Phosphorus| 1 x 10¹⁵      | 85k         |
| n⁻ Doping      | Phosphorus| 6 x 10¹²      | 90k         |

Figure 1. Schematic diagram of the experimental device structure of n-type LTPS TFTs with channel width and length of 3.5 and 20 µm, respectively: (a) 3D structure, (b) top view, and cross-sectional views along the (c) length and (d) width directions.
leads to anomalous current, was observed in the sub-threshold regime at $V_{GS} = 0–2$ V of the transfer curve. As mentioned above, previous studies have explained that the hump characteristic is caused by the hump channel in the taper region, as indicated in Figure 3 (b) [10–12]. When the $V_{TH}$ of the additional hump channel is lower than that of the main channel, the current starts to flow through the hump channel earlier than the main channel as the gate voltage increases, and later flows through the main channel, eventually resulting in hump-shaped current curves. In this respect, the measured results can be explained by the transfer curve at $V_{DS} = 0.1$ V consisting of two current paths: the main channel with a $V_{TH}$ of 2.2 V denoted by a blue solid line, and the hump channel with a $V_{TH}$ of 0.7 V denoted by a red dotted line. In order to reduce the hump phenomenon, it is recommended that a CED technique is used to eliminate the hump channel, which is the main cause of the hump phenomenon.

3.2. Numerical analysis of hump phenomena

In order to analyze the hump mechanism, physical parameters, such as the e-field and electron ($e^-$) concentration distribution, were investigated from the cross-sectional view in the width direction along a one-dimensional (1D) cut-line (A’ to B’) from the results of the TCAD simulation, as shown in Figure 4.2. The e-field was enhanced at the channel edge region at $V_{GS} = 1$ V in the sub-threshold regime with hump characteristics (Figure 4[b]). Thus, electrons were crowded into the channel edge region much more than the main channel (Figure 4[c]). In contrast, at $V_{GS} = 3$ V, which is higher than $V_{TH}$ (~ 2.2 V), the electron concentration of the main channel increased from $\sim 10^{10}$ cm$^{-3}$ to $\sim 10^{16}$ cm$^{-3}$ (Figure 4[d]) [14]. This indicates that the hump characteristics are attributed to the hump channel generated from the crowded electrons by a strong e-field at the channel edge at low $V_{GS}$ in the sub-threshold regime before the main channel turns on. Figure 5 shows the variation in electron concentration at the hump channel with taper angles of 20°, 45°, and 70° in the sub-threshold regime at $V_{GS} = 0.5$ V and $V_{DS} = 0.1$ V. The electron concentration in the hump channel decreases as the taper angle increases. Meanwhile, the electron concentration in the main channel is not affected by the taper angle. This result indicates that the hump characteristics are extremely sensitive to the shape of the channel edge of the LTPS TFTs. However, the hump characteristics have been improved by changing the specific shape of the tapered region in the previous studies [10,11]. These hump-reduction methods may cause the non-uniform luminance issue over the entire panel area due to the variation in the shape at the taper region caused by the complex fabrication process. Therefore, to improve the hump characteristics, it is necessary to either reduce the e-field or control the electron concentration at the channel edge region. We focused on controlling the electron concentration selectively at the channel edge region by using a channel doping process. Our CED process is a technique for controlling electron concentration only at the channel edge region.
Figure 3. (a) Measured transfer curve with hump characteristics at $V_{DS} = 0.1$ and $10 \text{V}$ in LTPS TFTs with the conventional channel doping process, and (b) schematic illustration of the hump channel and main channel in the sub-threshold regime at $V_{GS} < V_{TH}$.

Figure 4. Simulated physical properties along a 1D cut-line (A' to B') of (a) the 3D simulation structure for LTPS TFTs at $V_{DS} = 0.1 \text{ V}$, (b) the e-field distribution at $V_{GS} = 1$, and the electron concentration distribution within the active layer at $V_{GS} = (c) 1 \text{ V}$ and (d) $3 \text{ V}$.
3.3. Channel edge doping (CED) effect for hump reduction

Figure 6 displays the comparison between the simulation results obtained for the conventional channel doping and CED processes at $V_{GS} = 1$ V and $V_{DS} = 0.1$ V in sub-threshold regime. When the CED is performed, a higher level of doping is observed in the taper region as compared to the conventional channel doping process (Figures 6[a] and 6[b]). In the n-type LTPS TFTs, boron acted as an acceptor and decreased carrier concentration [15]. The simulation results indicate that heavily doped boron at the taper region reduces the number of electron carriers, thus resulting in a decrease in the $e^{-\text{max}}$ from $3.4 \times 10^{16}$ to $2.9 \times 10^{14}$ cm$^{-3}$ compared to the conventional channel doping (Figures 6[c] and 6[d]).

Based on the simulation results, we conclude that the channel edge effect can be effectively eliminated by employing the CED technique. In order to verify whether this is the case, we fabricated LTPS TFTs by using the CED process with the doping conditions used in the simulation. Figure 7 demonstrates the results of our measurements of the LTPS TFTs fabricated by the conventional doping and CED process. The hump phenomenon is not observed in the transfer curve of the samples fabricated by the CED process, while the hump-shaped transfer curves are observed in the samples where the conventional doping process was employed. Consequently, we conclude that the CED process leads to an effective reduction in the hump characteristics, given the excellent agreement between the simulation and experimental results.
4. Conclusion

In this study, we proposed that the CED process can be used to reduce the hump characteristics that limit the performance of the n-type LTPS TFTs. Through the CED process, robust LTPS TFTs were fabricated and their transfer curves do not exhibit the hump phenomenon. Additional boron is doped selectively at the taper region during the CED process, thus enabling control over the carrier concentration in the taper area. Comparative analysis of the devices fabricated by the conventional channel doping and the CED processes was performed via TCAD simulation and experimental measurements. The CED technique does not require the use of additional masks and is easy to implement as compared to the conventional solutions for hump issues, such as changing the taper shapes. The results obtained from our study would be extremely useful for fabricating high-performance LTPS TFTs for AMOLED displays.

Disclosure statement

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