Reliability of Buried InGaAs Channel n-MOSFETs With an InP Barrier Layer and Al₂O₃ Dielectric Under Positive Bias Temperature Instability Stress

Haiou Li¹, Kangchun Qu¹, Xi Gao¹, Yue Li¹, Yonghe Chen¹, Zhiping Zhou¹, Lei Ma¹, Fabi Zhang¹, Xiaowen Zhang¹, Tao Fu¹, Xingpeng Liu¹, Yingbo Liu¹, Tangyou Sun*¹ and Honggang Liu*²

¹Guangxi Key Laboratory of Precision Navigation Technology and Application, Guilin University of Electronic Technology, Guilin, China, ²Microwave Device and IC Department, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China

The positive bias temperature instability (PBTI) reliability of buried InGaAs channel n-MOSFETs with an InP barrier layer and Al₂O₃ gate dielectric under medium field (2.7 MV/cm) and high field (5.0 MV/cm) are investigated in this paper. The Al₂O₃/InP interface of the insertion of an InP barrier layer has fewer interface and border traps compared to that of the Al₂O₃/InGaAs interface. The subthreshold slope, transconductance, and shift of V₉ are studied by using the direct-current I_d-V_g measurements under the PBTI stress. The experimental results show that the degradation of positive ΔV₉ under the medium field stress is mainly caused by the acceptor trap, while the donor trap under the high field stress become dominant in the subthreshold region, which leads to the negative shift in V₉. The medium field stress-induced acceptor traps are attributed by the InP barrier layer in the subthreshold region, resulting that the low leakage current can be achieved in the buried InGaAs channel n-MOSFETs with an InP barrier layer compared to the surface InGaAs channel n-MOSFETs.

Keywords: PBTI, Al₂O₃/InP interface, InGaAs MOSFET, border trap, buried channel

INTRODUCTION

InGaAs was considered for use as the n-type high-mobility channel material because it has higher electron mobility and smaller electron effective mass than that of silicon [1–3]. The complementary metal oxide semiconductor (CMOS) structure can be realized by integrating III-V n-MOSFETs and Ge p-MOSFETs on a Si CMOS platform [4–6]. However, one of the most critical problems that must be solved to realize III-V MOSFETs is the formation of a stable MOS interface with low trap density [7]. Compared with the SiO₂/Si system, the III-V native oxides negatively affect fermi-level pinning and current drift [8–10]. The atomic layer deposited (ALD) Al₂O₃ dielectric in surface InGaAs channel MOSFETs can achieve a thermally stable interface and large band offsets, as confirmed by the previous research on the dielectric layer of InGaAs MOSFETs [11–13]. However, Al₂O₃/InGaAs interface traps and border traps in the dielectric layer remain high, which reduces the effective channel mobility and results in reliability instability in InGaAs MOSFETs [14–16]. Based on the poor interface quality of InGaAs and Al₂O₃, the introduction of a barrier layer between the Al₂O₃ dielectric and InGaAs channel considerably improves channel electron mobility, transconductance,
and drive current [17–19]. Although the InGaAs channel and Al₂O₃ dielectric are separated by the barrier layer, high interface traps and border traps considerably affect device reliability under bias temperature instability (BTI) stress [20–22]. To reduce interface defect density, the interface passivation techniques of N passivation treatment [23–25] and sulfur passivation treatment [26–28] have been investigated to improve the interface properties and reliability.

Bias temperature instability stress directly leads to the degradation of threshold voltage, subthreshold slope, and on-state current. The interface trap and border trap induced by bias temperature instability stress are also considered to be the causes of the degradation of III-V MOSFET performance. Li et al. investigated the surface InGaAs channel n-MOSFETs under positive bias temperature instability (PBTI) stress and recovery [29]. They explained that high defect density exists at the InGaAs and Al₂O₃ interface, which includes both interface traps and border traps, and the PBTI stress induces mainly border traps. However, few studies have reported the buried channel InGaAs MOSFETs with a barrier layer under PBTI stress.

In this paper, we experimentally studied the mechanisms of the buried InGaAs channel n-MOSFETs with an InP barrier layer under PBTI stress and recovery. The interface and border traps are estimated in the Al₂O₃/InP and Al₂O₃/InGaAs interfaces. The degradation of \( I_d-V_g \) during the PBTI test shows a shift in \( V_g \) under a medium field (2.7 MV/cm), which is the opposite of that observed under a high field (5.0 MV/cm) in buried InGaAs channel n-MOSFETs. The effects of PBTI stress in the buried InGaAs channel n-MOSFETs with an Al₂O₃/InP interface were investigated by performing the subthreshold slope, transconductance, and \( V_g \) shift. The specific border traps are quantified to analyze the reliability of the device under the PBTI stress.

**EXPERIMENTAL**

**Fabrication Process**

The main structure of Si-based buried In₀.₂₅Ga₀.₇₅As channel n-MOSFETs used in this paper is illustrated in **Figure 1**. The layer structure was grown on InP substrate by metal–organic chemical vapor deposition (MOCVD) and consisted of a 20 nm In₀.₅₂Al₀.₄₈As buffer layer, a 2 nm In₀.₆Al₀.₄As doping layer with Be doping concentration of \( 3 \times 10^{18} \) cm\(^{-3} \), a 5 nm In₀.₅₂Al₀.₄₈As barrier layer, a 5 nm In₀.₂₅Ga₀.₇₅As channel layer, a 3 nm InP barrier layer, and a 40 nm In₀.₅₃Ga₀.₄₇As cap layer with N-type doping concentration of \( 2 \times 10^{19} \) cm\(^{-3} \). During the device fabrication process, benzocyclobutene (BCB) is used to bond the InP wafer to the Si wafer, and the two-step surface cleaning process was carried out. First, a 10% w/t HCl solution was applied for 3 min to remove the native oxide layer, and 20% w/t NH₄OH solution was applied for 6 min. Second, 20% (NH₄)₂S solution was applied to passivate the interface of the InP barrier layer for 15 min at room temperature [26, 27]. Then, 8 nm of Al₂O₃ (i.e., gate dielectric) was deposited by Beneq TFS-200 atomic layer deposition (ALD) system at the substrate temperature of 300°C. A postdeposition anneal (PDA) was carried out at 400°C for 30 s in N₂ atmosphere. Ti/Au gate metal was evaporated by an electron beam system. The post metal anneals (PMA) at 300°C for 30 s in N₂ was carried out in the rapid thermal annealing system. Source and drain electrodes (Ni/Ge/Au) were deposited by electron beam evaporation and annealing at 270°C for 3 min. The transistors have a 400-μm channel width and a 4-μm channel length (L).

**Measurement Methods**

DC current-voltage (\( I-V \)) characterization was achieved using an Agilent B1500A semiconductor device analyzer. In the \( I-V \) measurements [30], the drain voltage (\( V_d \)) was set to 50 mV and the source and substrate were grounded. During the PBTI stress phase, two different gate voltages were selected during the PBTI stress phase, and the gate field strengths were calculated to be \( E = 2.7 \) and \( E = 5.0 \) MV/cm, respectively, based on the simulation, while \( V_g\) = \( V_d\) = \( V_b\) = 0 V. All DC \( I_d\)-\( V_g\) tests were carried out at room temperature (300 K). The PBTI test contains a 500 s stress phase and a 500 s recovery phase, as shown in **Figure 2**. During the stress phase, PBTI stress is set to 2.7 MV/cm and to 5 MV/cm for Al₂O₃ for a duration of 500 s. Before applying the stress, we first measured the initial \( I_d\)-\( V_g\) curve by using a fresh sample (\( I\)-line). After a 500-s PBTI stress, the S line was measured; the R lines were the \( I_d\)-\( V_g\) curves obtained from the sample during the 500 s recovery.

**RESULTS AND DISCUSSION**

**Interface Characteristics**

The distribution curves of interface trap density (\( D_{it} \)) are extracted from the multifrequency (1 MHz to 1 KHz) \( C-V \)
Direct-Current $I_d$-$V_g$ Measurements

Unlike the Si MOSFET under positive bias temperature instability stress, the oxide traps of the InP/Al$_2$O$_3$ are generated during the stress phase. An uninterrupted cycle test on the same device can determine whether the test stress contributes to the $I_d$-$V_g$ curve drift. The $I_d$-$V_g$ curves of the buried InGaAs n-MOSFETs are shown in Figure 4. Compared with a fresh line, there is no distinct shift in $I_d$-$V_g$ curves for either the subthreshold or the on-state region, and there is no clear change in current after the first cycle test. In the second cycle measurement curve, the $I_d$-$V_g$ curves still do not show any shift. The subthreshold slope (SS) and on-state current remain the same compared with the fresh line, which indicates that neither negative nor positive charges were created under the measuring stresses.

According to the simulation results by Varghese et al. [33], the recoverable donor traps impact negative $\Delta V_g$ in the subthreshold region. Acceptor traps are essential for inducing a positive $I_d$-$V_g$ curve drift. The $I_d$-$V_g$ curves measured for the fresh device before stress (I line) and under PBTI stress ($S$ line) ($E_g = 2.7$ and $E = 5.0 \text{ MV/cm}$) after 500 s as well as the recovery (R line) after 500 s. Compared with the I, S, and R lines in the medium and high fields (2.7 MV/cm and 5.0 MV/cm), there are two cases in the subthreshold region and in the on-state region. (1) In a medium field ($E_g=2.7 \text{ MV/cm}$), the $V_g$ shift $\Delta V_g$ at a constant drain current is positive both in the subthreshold and on-state regions, which indicates that negative charges were created after the PBTI stress. The $I_d$-$V_g$ curve of the R line still demonstrates a negative shift in the on-state region compared with that of the S line. It is clear that acceptor traps, which are induced by the medium field strength stress, are recoverable. The stress-induced recoverable acceptor traps exist in the on-state region. However, the drain current of the R line coincides with that of the S line in the subthreshold region, indicating the medium field strength stress-induced recoverable traps are not shown in the subthreshold region. (2) In a high field ($E_g=5.0 \text{ MV/cm}$), the $V_g$...
shift $\Delta V_g$ is negative in the subthreshold region, indicating donor traps are created after the PBTI stress of 5.0 MV/cm. The $V_g$ shift $\Delta V_g$ is positive in the on-state region, demonstrating acceptor traps are created after the PBTI stress. The two crossing points, which mean a balance between acceptor trap and donor trap, are found in 500 s of PBTI and 500 s of recovery with initial curve. The results show that donor traps induce negative $V_g$ shift of $I_d-V_g$ curves, larger shift with lower $I_d$ current level. The acceptor traps induce positive shift of $I_d-V_g$ curves, larger shift with higher $I_d$ current level. The high field stress induced donor traps have a large density in distribution of energy gap, and their distribution extends to the conduction band, just opposite to the distribution trend of acceptor traps in the energy gap, which are consistent with that of the surface channel InGaAs n-MOSFETs [29, 33]. By comparing the $S$ line with initial curve under the high field strength stress, the shift of crossing point is found to be negative in the $R$ line with initial curve, indicating the donor traps are almost recoverable. Compared with the $S$ line, the $R$ line demonstrates a negative shift in the on-state region, indicating there are fewer recoverable donor traps than recoverable acceptor traps in the on-state region.

In surface channel InGaAs n-MOSFETs [29], stress-induced donor traps produce a negative shift in threshold voltage under the 2.7 MV/cm stress. However, stress-induced acceptor traps produce a positive shift in threshold voltage under the 2.7 MV/cm stress in buried channel InGaAs n-MOSFETs. Meanwhile, the $I_d-V_g$ curves of the $S$ and $R$ lines do not have an offset in the subthreshold region. The results indicate that no donor traps are induced under medium field for the buried channel device. The Al$_2$O$_3$/InP interface has a lower interface trap density than that of the Al$_2$O$_3$/InGaAs interface in the distribution of energy gap, especially the downtrend of $D_{th}$ distribution of the Al$_2$O$_3$/InP interface near the mid-gap, which is opposite of the $D_{th}$ distribution of the Al$_2$O$_3$/InGaAs interface near the mid-gap shown in Figure 3A. The effect of low defect density is not serious in the recovery curve of the buried channel InGaAs n-MOSFETs in the subthreshold region under medium field strength, so buried channel InGaAs n-MOSFETs with Al$_2$O$_3$/InP interface show a completely different trend than that of surface channel InGaAs n-MOSFETs in the recovery phase.

Time-dependence of $\Delta V_g$ in the on-state and subthreshold regions is shown in Figures 6A, B respectively. The value of $\Delta V_g$ shifts to positive direction in the on-state region under medium and high field strengths. From 500 to 1,000 s of recovery, $\Delta V_g$ of the two recovery curves continues the downward trend in the on-state region. The result shows recoverable acceptor traps have been proved to be recoverable in the on-state region under the field stress. The degradation of negative $\Delta V_g$ under high field stress is clearly smaller than the degradation of positive $\Delta V_g$ under medium field stress, indicating donor traps are induced under high field stress in the subthreshold region. Because stress-induced donor traps are fully recovered in the subthreshold region, $V_g$ is totally recovered in the subthreshold region. The degradation of the subthreshold slope ($SS$) and transconductance ($G_m$) are reflected by the stress-induced border traps under medium and high fields, as shown in Figures 7A, B. The downtrends of $\Delta S$ and $\Delta G_m$ are clear during the recovery process from 500 to 1,000 s, revealing that stress-induced recoverable traps were released in the recovery process. When high field stress-induced recoverable donor traps become dominant in the subthreshold region, the degradation of $\Delta S$ and $\Delta G_m$ are more pronounced compared with that of medium field stress. This finding illustrates that the degradation of the subthreshold slope and the transconductance are mainly caused by the donor traps under the high field stress.

Extracts of Trap Energy Densities

According to the similar explanation given by Li et al. [29], the distribution curves of border traps were investigated under the stress from $\Delta V_g$ among the $I$, $S$, and $R$ lines. Specifically, (1) donor and acceptor traps are induced at the end of the 500 s stress. (2) Stress-induced donor traps fully recover, while acceptor traps are partially recoverable and partially permanent at the end of 500-s recovery. Although stress-induced acceptor traps are dominant, donor traps may also exist. To distinguish between donor traps and acceptor traps, $\Delta N^T_{ox}(I_d)$ represents the density...
of negatively charged permanent acceptor traps, and $\Delta N^{\text{DR}}_{\text{ox}}(I_d)$ represents recoverable donor traps. $\Delta N^{\text{AP}}_{\text{ox}}(I_d)+\Delta N^{\text{AR}}_{\text{ox}}(I_d)$ or $\Delta N^{\text{AP}}_{\text{ox}}(I_d)+\Delta N^{\text{DR}}_{\text{ox}}(I_d)$ is the total trap, which represents the density difference of negatively charged acceptor traps or positively charged donor traps. $\Delta N^{\text{AR}}_{\text{ox}}(I_d)-\Delta N^{\text{DR}}_{\text{ox}}(I_d)$ is the density of negatively charged recoverable acceptor traps. These parameters can be obtained from:

$$\Delta N^{\text{AP}}_{\text{ox}}(I_d) = \left( \frac{C_{\text{ox}}}{q} \right) \Delta V_g^{\text{IS}}(I_d)$$ (1)

$$\Delta N^{\text{AP}}_{\text{ox}}(I_d) + \Delta N^{\text{AR}}_{\text{ox}}(I_d) = \left( \frac{C_{\text{ox}}}{q} \right) \Delta V_g^{\text{IS}}(I_d)$$ (2)

$$\Delta N^{\text{DR}}_{\text{ox}}(I_d)-\Delta N^{\text{AR}}_{\text{ox}}(I_d) = \left( \frac{C_{\text{ox}}}{q} \right) \Delta V_g^{\text{IS}}(I_d)-\left( \frac{C_{\text{ox}}}{q} \right) \Delta V_g^{\text{IR}}(I_d)$$ (3)

where $C_{\text{ox}}$ is the gate oxide capacitor per unit area and $q$ is the electron charge. We obtain $\Delta N^{\text{AP}}_{\text{ox}}(V_g)$, $\Delta N^{\text{DR}}_{\text{ox}}(I_d)$, $\Delta N^{\text{AP}}_{\text{ox}}(I_d)$, and $\Delta N^{\text{AR}}_{\text{ox}}(V_g)+\Delta N^{\text{DR}}_{\text{ox}}(V_g)$ as functions of gate bias $V_g$, as shown in Figures 8A, B. For buried channel InGaAs MOSFETs, the magnitude of total traps is averagely $1.5 \times 10^{12}$ cm$^{-2}$ and $1.6 \times 10^{12}$ cm$^{-2}$ under medium and high field strengths, respectively, indicating more traps are induced by high field stress than the medium field stress. The medium field stress-induced permanent acceptor trap is calculated to be $1.1 \times 10^{12}$ cm$^{-2}$, which is larger than recoverable acceptor trap with the average density of $3.8 \times 10^{11}$ cm$^{-2}$. By comparison of the surface channel InGaAs MOSFETs, donor trap is not induced by the medium field stress in the buried InGaAs channel MOSFETs. However, the recoverable acceptor trap and recoverable donor trap are generated by the high field stress with a common density of $8.7 \times 10^{11}$ cm$^{-2}$, and the permanent acceptor trap is averagely $7.7 \times 10^{11}$ cm$^{-2}$. The results indicate that recoverable trap is easily induced by high field stress. Meanwhile, the medium field stress-induced permanent acceptor trap is larger than the high field stress-induced permanent acceptor trap in the subthreshold region, indicating the permanent acceptor trap and recoverable acceptor trap have been neutralized by recoverable donor trap in the high field stress.

Compared to the surface channel InGaAs n-MOSFETs by considering the experimental results of Li et al. [29], the impacts of PBTI stress on buried InGaAs channel n-MOSFETs are summarized as follows: (1) The $D_{it}$ and $N_{bt}$ distribution of the Al$_2$O$_3$/InP interface is smaller than that of Al$_2$O$_3$/InGaAs.
interface through the sulfur passivation treatment, indicating the interface reliability of buried InGaAs channel n-MOSFETs are improved by the Al$_2$O$_3$/InP interface. (2) In the surface channel InGaAs n-MOSFETs with the Al$_2$O$_3$/InGaAs interface donor traps become the dominant under the medium field stress. In contrast, the medium field stress-induced the permanent acceptor trap and recoverable acceptor trap are attributed by the degradation of $\Delta V_g$ and $\Delta S$ in the buried InGaAs channel n-MOSFETs with the Al$_2$O$_3$/InP interface, which indicates that the generation of acceptor trap are attributed by the insertion of the InP barrier layer. (3) Compared to the surface InGaAs channel n-MOSFETs under the medium field stress, the acceptor trap become dominant in the subthreshold region for the buried channel one. The buried channel InGaAs MOSFETs is better to maintain the low off-state current developing III-V MOSFETs technology for low-power application.

CONCLUSIONS

In summary, the degradation of the buried InGaAs channel n-MOSFETs with an InP barrier layer under PBTI stress and recovery were investigated. The Al$_2$O$_3$/InP interface helps achieve low interface and border traps compared to the Al$_2$O$_3$/InGaAs interface through the sulfur passivation treatment. Contrary to the shift direction of $V_g$ under the medium field stress in the surface InGaAs channel n-MOSFETs, the permanent acceptor trap of $1.1 \times 10^{12}$ cm$^{-2}$ and recoverable acceptor trap of $3.8 \times 10^{11}$ cm$^{-2}$ become the dominant to produce a positive shift in $V_g$ in the buried InGaAs channel n-MOSFETs. The high field stress-induced recoverable donor trap of $8.7 \times 10^{11}$ cm$^{-2}$ cause degradation of $S$ and $G_m$ in the subthreshold region, whereas the degradation of $I_d-V_g$ is contributed by the recoverable acceptor trap and permanent acceptor trap in the on-state region. Compared to the surface

InGaAs channel n-MOSFETs under medium field stress, the low leakage current can be achieved in the buried InGaAs channel n-MOSFETs with an InP barrier layer.

DATA AVAILABILITY STATEMENT

All datasets generated for this study are included in the article/supplementary material.

AUTHOR CONTRIBUTIONS

HLi was the leader of the work and responsible for the main of experiment and paper writing. KQ, XG, YLi, YC, ZZ, and LM were responsible for single step of the fabrication process. FZ and XZ were responsible for device testing. TF, XL, YLIu, TS, and HLiu were mainly engaged in picture editing and related data processing. TS and HLiu contributed to the modification and suggestion in this paper.

FUNDING

This work was supported by National Natural Science Foundation of China (Nos. 11965009, 61874036, 61805053, and 61764001), Guangxi Innovation Research Team Project (No. 2018GXNSFGA281004), Guangxi Science and Technology Planning Project (Nos. AD18281030, AD18281084, AD18281034, and AD18281037), Guangxi Natural Science Foundation (Nos. 2016GXNSFDA380021, 2017GXNSFAA198164, 2018GXNSFAA050052, 2018GXNSFAA281152, and 2018GXNSFAA281201), Guangxi Key Laboratory of Precision Navigation Technology and Application (Nos. DH201801, DH201808, DH201702, and DH201701), and Innovation Project of GUET Graduate Education (No. 2018YJCB15).

REFERENCES

1. Alamo D, Jesus A. Nanometre-scale electronics with III-V compound semiconductors. Nature. (2011) 479:217–23. doi: 10.1038/nature10677
2. Kulbachinskii VA, Yuzeeva NA, Galiev GB, Klimov EA, Vas’evskii IS, Khalibullin RA, et al. Electron effective masses in an InGaAs quantum well with InAs and GaAs inserts. Semicon Sci Technol. (2012) 27:035021. doi: 10.1088/0268-1242/27/3/035021
3. Selmi L, Caruso E, Carapezzi M, Gnani E, Zagni N, et al. Modelling nanoscale n-MOSFETs with III-V compound semiconductor channels: from advanced models for band structures, electrostatics and transport to TCAD. In: IEEE International Electron Devices Meeting (IEDM), San Francisco, CA (2017).
4. Wu H, Ye PD. Fully depleted Ge CMOS devices and logic circuits on Si. IEEE Electron Device Lett. (2016) 36:3028–35. doi: 10.1109/TED.2016.2581120
5. Tewari S, Biswas A, Mallik A. Investigation on high-performance CMOS with p-Ge and n-InGaAs MOSFETs for logic applications. IEEE Trans Nano. (2015) 14:275–81. doi: 10.1109/TNANO.2015.2590295
6. Takagi S, Zhang R, Suh J, Kim SH, Yokoyama M, Nishi K, et al. Investigation on high-performance CMOS with p-Ge and n-InGaAs MOSFETs for logic applications. IEEE Trans Nano. (2015) 14:275–81. doi: 10.1109/TNANO.2015.2590295
7. Guo Y, Li H, Robertson J. AlN and Al oxy-nitride gate dielectrics for reliable gate stacks on Ge and InGaAs channels. J Appl Phys. (2015) 119:204101. doi: 10.1063/1.4951004
8. Franco J, Putcha V, Vais A, Sionckie S, Waldron N, Zhou D, et al. Characterization of oxide defects in ingaas mos gate stacks for high-mobility n-Channel MOSFETs. In: IEEE International Electron Device Meeting (IEDM), San Francisco, CA (2017).
9. Bouzid A, Pasquarello A. Electron trap states at InGaAs/oxide interfaces under inversion through constant Fermi-level abinitio molecular dynamics. J Phys. (2017) 29:055702. doi: 10.1088/1361-648X/aa9a09
10. Mo J, Lind E, Roll G, Wernersson LE. Reduction of off-state drain leakage in InGaAs-based metal-oxide semiconductor field-effect transistors. Appl Phys Lett. (2017) 105:033516. doi: 10.1063/1.4891569
11. He G, Zhu LQ, Sun ZQ, Wan Q, Zhang L. Integrations and challenges of novel high-k gate stacks in advanced CMOS technology. Prog Mater Sci. (2011) 56:475–572. doi: 10.1016/j.pmatsci.2011.01.012
12. Tang K, Droopad R, McIntyre PC. Bias temperature stress induced hydrogen degassing from Al$_2$O$_3$/InGaAs interface defects. J Appl Phys. (2018) 123:025708. doi: 10.1063/1.4994393
13. Tang K, Winters R, Zhang LL, Droopad R, Eizenberg M, McIntyre PC. Border trap reduction in Al$_2$O$_3$/InGaAs gate stacks. Appl Phys Lett. (2015) 107:202102. doi: 10.1063/1.4936100
14. Misheok C, Anderson J, Walle CGVD. Native point defects and dangling bonds in $\alpha$-Al$_2$O$_3$. J Appl Phys. (2013) 113:044501. doi: 10.1063/1.47 84114
15. Kwon HM, Kim DH, Kim TW. Relationship between effective mobility and border traps associated with charge trapping in In$_{0.5}$Ga$_{0.3}$As
MOSFETs with various high-K stacks. Appl Phys Express. (2018) 11:034101. doi: 10.7567/APEXP.11.034101

16. Vais A, Franco J, Martens K, Lin D, Sioncke S, Putcha V, et al. A new quality metric for III-V/High-k MOS gate stacks based on the frequency dispersion of accumulation capacitance and the CET. IEEE Electron Device Lett. (2017) 38:318–21. doi: 10.1109/LED.2017.2677994

17. Chang HD, Sun B, Xue BQ, Liu GM, Zhao W, Wang SK, et al. Effect of the Si-doped In$_{0.65}$Ga$_{0.35}$P barrier layer on the device performance of In$_{0.4}$Ga$_{0.6}$As MOSFETs grown on semi-insulating GaAs substrates. Chin Phys B. (2013) 22:077306. doi: 10.1088/1674-1056/22/7/077306

18. Xue F, Zhao H, Chen YH, Wang Y, Wang Y, Zhou F, et al. High-k InGaAs metal-oxide-semiconductor field-effect-transistors with various barrier layer materials. Appl Phys Lett. (2011) 99:033507. doi: 10.1063/1.3611502

19. Tewari S, Biswas A, Mallik A. Impact of different barrier layers and indium content of the channel on the analog performance of InGaAs MOSFETs. IEEE Trans Electron Dev. (2013) 60:1584–89. doi: 10.1109/TED.2013.2249071

20. Krylov I, Ritter D, Eizenberg M. The role of the substrate on the dispersion in accumulation in III-V compound semiconductor-based metal-oxide-semiconductor gate stacks. Appl Phys Lett. (2015) 107:103503. doi: 10.1063/1.4930202

21. Benbakhti B, Ayubi-Moak JS, Kalna K, Lin D, Hellings G, Brammertz G, et al. Impact of interface state trap density on the performance characteristics of different III-V MOSFET architectures. Microelectron Reliab. (2010) 50:360–64. doi: 10.1016/j.microrel.2009.11.017

22. Doera S, Berouker G, Loh WY, Vekasler D, Matthews K, Kim TW, et al. Positive bias instability and recovery in InGaAs channel nMOSFETs. IEEE Trans Device Mater Reliab. (2013) 13:507–14. doi: 10.1109/TDMR.2013.2284376

23. Wang SK, Sun B, Cao MM, Chang HD, Su YY, Li HO, et al. Modification of Al$_2$O$_3$/InP interfaces using sulfur and nitrogen passivations. J Appl Phys. (2017) 121:184104. doi: 10.1063/1.4982904

24. Haimoto T, Hoshii T, Nakagawa S, Takenaka M, Takagi S. Fabrication and characterization of metal-insulator-semiconductor structures by direct nitridation of InP surfaces. Appl Phys Lett. (2010) 96:012107. doi: 10.1063/1.3269906

25. Hoshii T, Yokoyama M, Yamada H, Hata M, Yasuda T, Takenaka M, et al. Impact of InGaAs surface nitridation on interface properties of InGaAs metal-oxide-semiconductor capacitors using electron cyclotron resonance plasma sputtering SiO$_2$. Appl Phys Lett. (2010) 97:132102. doi: 10.1063/1.3464170

Conflict of Interest: The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Copyright © 2020 Li, Qu, Gao, Li, Chen, Zhou, Ma, Zhang, Zhang, Fu, Liu, Liu, Sun and Liu. This is an open-access article distributed under the terms of the Creative Commons Attribution License (CC BY). The use, distribution or reproduction in other forums is permitted, provided the original author(s) and the copyright owner(s) are credited and that the original publication in this journal is cited, in accordance with accepted academic practice. No use, distribution or reproduction is permitted which does not comply with these terms.