High-Gain 200 ns Photodetectors from Self-Aligned CdS–CdSe Core–Shell Nanowalls

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1D core–shell heterojunction nanostructures have great potential for high-performance, compact optoelectronic devices owing to their high interface area to volume ratio, yet their bottom-up assembly toward scalable fabrication remains a challenge. Here the site-controlled growth of aligned CdS–CdSe core–shell nanowalls is reported by a combination of surface-guided vapor–liquid–solid horizontal growth and selective-area vapor–solid epitaxial growth, and their integration into photodetectors at wafer-scale without postgrowth transfer, alignment, or selective shell-etching steps. The photocurrent response of these nanowalls is reduced to 200 ns with a gain of up to $3.8 \times 10^3$ and a photoresponsivity of $1.2 \times 10^3$ A W$^{-1}$, the fastest response at such a high gain ever reported for photodetectors based on compound semiconductor nanostructures. The simultaneous achievement of sub-microsecond response and high-gain photocurrent is attributed to the virtues of both the epitaxial CdS–CdSe heterojunction and the enhanced charge-separation efficiency of the core–shell nanowall geometry. Surface-guided nanostructures are promising templates for wafer-scale fabrication of self-aligned core–shell nanostructures toward scalable fabrication of high-performance compact photodetectors from the bottom-up.

1D core–shell nanostructures are a promising alternative to thin film for compact optoelectronics owing to their high interface to volume ratio between two extended phases.[1–6] Depending on the bandgaps and relative position of electronic energy levels of the involved semiconductors, core–shell nanostructures are divided into different types, dominated type-I, type-II, and reverse type-I band alignments (or classified as p–n, n–n, and p–p junctions).[1,7,8] The different band alignments deliver different functions for practical applications. For instance, Zhang et al.[9] suggested that the photogenerated carriers in core–shell nanowires with a type-II band alignment are efficiently separated between the core and the shell, which extend both along the nanowire.[3,10] Charge separation in these heterostructures is enhanced by shortening the diffusion length of minority carriers,[5,6] and accordingly their photocurrent response. In type-I n–n core–shell nanowires,[1,8] the shell is often used to passivate the surface of the core, aiming to improve the optical properties of nanowires. Realizing the substantial potential of core–shell nanostructures, however, requires predictable control over their composition, interface, direction, and shell-to-core alignment from the bottom-up.[1–4] In particular, horizontal arrays are highly desirable toward scalable fabrication of nanodevices. However, deterministic assembly of freestanding core–shell nanostructures into horizontal arrays with controlled sites and shells remains a challenge. To date, although nanodevices based on core–shell nanostructures have been extensively studied, most of them were investigated at the single-nanowire level[2,3,10,11] or vertical arrays.[12,13]

One possible option to have ordered core–shell nanostructures is to follow the postgrowth assembly that has been proposed for assembly of compositional-homogenous nanowires by aid of external forces.[14–16] However, the alignment of postgrowth assembly is subject to thermal and dynamic fluctuations.[14–16] Moreover, most postgrowth assembly approaches are incapable of controlling the shell length and location. Besides, selective shell etching is usually involved after nanowire growth in order to have electrode contact with the core region, which is another hurdle toward scalable fabrication. Although the postgrowth selective shell etching based on a combination of lithography and wet chemical etching has been developed to expose the core in a lithographically defined region,[10] this scheme exhibited disadvantages such as tricky control over etched shell thickness, damage on core surface, introduction of contamination, and so on.

In contrast to the postgrowth assembly, surface-guided horizontal growth offers a facile method to prepare aligned core–shell nanostructures with predictable aligned shells from the bottom-up, as we have recently reported.[17] Horizontal growth was first observed during the growth of composition-homogeneous nanowires on atomic-flat single-crystal surfaces.[18–26]
Later, horizontal growth was also achieved on faceted substrates with periodic nanosteps or nanogrooves via the so-called “graphoepitaxy” (growth along relief features larger than lattice parameters).[27–29] Since the first graphoepitaxial growth of horizontal GaN nanowires,[29] a growing list of semiconductors has been succeeded in graphoepitaxy growth of nanowires, such as ZnO,[30] ZnSe,[31] ZnTe,[32] CdSe,[33] and CdS.[34] In the case of CdS, we found that a nanowall geometry has significant advantages over the nanowire geometry, enabling faster photodetectors and more efficient field-effect transistors owing to their 3D trigate configuration. Would it be possible to combine the advantages of a core–shell 1D heterostructure[17] with those of a nanowall geometry[34] in a single self-aligned nanostructure exploiting the phenomenon of graphoepitaxy?

Here we present a scheme that enables a site- and alignment-controlled growth of CdS–CdSe core–shell nanowalls on spontaneously nanofaceted sapphire surfaces. This scheme also offers a predictable control over shell length, site, and alignment. Taking advantage of the self-aligned nanowalls and the site-controlled shells, their scalable integration into photodetectors is demonstrated, without postgrowth dispersion, transfer, alignment, and selective shell-etching steps. The photocurrent of these core–shell nanowalls exhibits simultaneously a submicrosecond, high-gain response and high photoresponsivity owing to the virtues of both the epitaxial CdS–CdSe heterojunction and the enhanced charge-separation efficiency of the core–shell nanowire structure.

M-plane sapphire, i.e., α-Al2O3(1010), is thermodynamically unstable and forms periodic V-shaped nanogrooves upon annealing at elevated temperature.[29] The slopes of the V-shaped nanogrooves are composed of R(1102) and S(1101) facets at an angle of 130° (Figure 1a). Figure 1b shows the schematic drawing of typical experimental steps for the growth of CdS–CdSe core–shell nanowalls (see details in the Supporting Information). As-received M(1010) sapphire is first annealed at 1600 °C for 10 h to spontaneously form the desired nanogrooves. Gold nanoparticles are then deposited selectively on the annealed M(1010) sapphire surfaces to serve as catalysts for the site-controlled growth. Aligned CdS nanowalls are grown by physical vapor deposition (PVD) using CdS powder as precursor. Thereafter, the sample is covered with a thin layer of polycrystalline Al2O3 by atomic layer deposition (ALD), followed by defining the area to be etched via photolithography, etching in a buffered oxide etch (BOE) solvent, and liftoff the remained photoresist with acetone. Next, the sample with selective-etched area is used to perform another PVD growth, this time using CdSe powder as precursor. Only the exposed nanowall surfaces are coated with CdSe layers via a surface-epitaxial growth owing to the selective protection of the Al2O3 layer. Lastly, the remained Al2O3 layer is removed by another etching in the BOE solvent.

Scanning electron microscopy (SEM) revealed that the nanogrooves on annealed M(1010) sapphire surfaces have widths ranging from tens of nanometers (Figure S1, Supporting Information) to a few hundred nanometers (Figure 1c). Atomic force microscope (AFM) (Figure 1d,e) showed that these nanogrooves have heights of tens of nanometers. No aligned CdS nanostructures were observed on as-received M(1010) sapphire surfaces without nanogrooves (Figure S2, Supporting Information), whereas well-aligned high-density CdS nanowalls were obtained on the annealed M(1010) sapphire surfaces with nanogrooves (Figure S3, Supporting Information). These phenomena suggest that the nanogrooves on sapphire surfaces play the key role for the alignment of nanowalls.

Figure 1. Surface-guided CdS–CdSe core–shell nanowalls. a) Atomic model of M(1010) sapphire before (left) and after (right) annealing. Red and cyan balls are oxygen and aluminum, respectively. b) Schematic drawing of experimental steps. c) SEM, d) AFM, and e) height of the nanogrooves self-formed on annealed M(1010) sapphire surface. f) 45° titled SEM of CdS–CdSe core–shell nanowalls. g) 3D AFM image of CdS–CdSe nanowalls. h) Representative height across the CdS-only and CdS–CdSe core–shell region.
As-fabricated CdS–CdSe core–shell nanowalls are self-aligned along the nanogrooves with \( \{11 \bar{2} 0\}_\perp \) directions (Figure 1f). The lengths of these nanowalls are \( \approx 50 \mu m \) for a 30 min CdS-growth and the CdSe-shell lengths are 10 \( \mu m \) (Figure S4, Supporting Information). AFM image (Figure 1g,h) reveals that the heights of CdS-only regions are usually less than 100 nm, while the heights of the core–shell regions exceed 200 nm. In general, the CdSe-shell thickness can be tuned from a few ten nanometers (Figure S5, Supporting Information) to a few hundreds of nanometers by adjusting the CdSe-growth conditions (i.e., growth time or substrate temperature). It is worth emphasizing that this scheme also enables a predictable control over shell length and site from the bottom-up, in addition to the excellent alignment of nanowalls. For example, the length and site (\( \approx 15 \mu m \) away from the gold pad) of the CdSe shells shown in Figure 1f were defined by a photolithography process before the CdSe-shell epitaxy (Figure S4, Supporting Information). Consequently, electrode contact can be laid down deterministically onto the cores and shells without postgrowth-selective shell etching, which is a crucial step toward scalable fabrication of nanodevices.

Two samples with different CdSe-growth times (different CdSe thicknesses) were examined by grazing incidence X-ray diffraction (XRD). The diffraction peaks in each XRD pattern (Figure 2a) were indexed into a combination of hexagonal wurtzite CdS (purple, ICDD (International Center for Diffraction Data) No. 00-006-0314) and CdSe (orange, ICDD No. 01-070-2554) (Figure S6, Supporting Information). The relative intensity of CdSe peaks to CdS peaks in Sample I is much smaller than that in Sample II, indicating that the increase of CdSe growth time indeed resulted in an increase of CdSe-shell thickness. Compared with their ICDD peaks (purple and orange in Figure 2a), the shifts of CdS peaks from both samples were negligible, indicating that the CdS-lattice distortion is very small after the CdSe-shell growth. The CdSe peaks, however, shifted notably toward higher angles, and the CdSe peaks from Sample I with thinner CdSe shells shifted more significantly than those of Sample II. These observations suggested
that the CdSe-lattice distortion was gradually relaxed with the increase of shell thickness. The lattice spacing (d) was extracted from the XRD (see calculation details and Table S1 in the Supporting Information) and compared with their ICDD data. The comparison yields a positive and negative Δd for CdS and CdSe (Table S1, Supporting Information), respectively, indicating that CdS lattices underwent expansion whereas CdSe lattices undergone compression when they were brought together to form the core–shell nanowalls.

Cross-sectional transmission electron microscope (TEM) image (Figure 2b) shows that the angles of V-shaped nanogrooves are around 128°, very close to the 130° angle predicted by the atomic model (Figure 1a), hence the nanogroove surfaces are indeed composed of R[1012] and S[1011] lattice planes. The nanostucture standing on the nanogrooves shows a well-defined nanowall geometry. Ten nanowalls were checked and they have heights of 130–410 nm and widths of 50–90 nm. EDS spectra collected from different locations (top left in Figure 2c) and the in situ electron energy loss spectrum (EELS) mapping (Figure 2c) revealed that Cd was uniformly dispersed throughout the nanowall cross section, whereas S was concentrated in the lower core region and Se stayed near the nanowall surface (see more EELS mapping in Figure S7 in the Supporting Information), confirming the formation of CdS–CdSe core–shell heterostructure, as schematically shown in Figure 2d. In addition, more Se was detected on the nanowall top surface than that on the nanowall side surfaces, indicating CdSe had undergone a facet-selective growth.[35,36] Possible reasons will be discussed later. Fast Fourier transformation (FFT) pattern (Figure 2e) revealed that these nanowalls have a wurtzite structure and a growth axis along the [1120]_CdS || [1120]_CdSe direction. Besides, the CdS-FFT pattern is overlapped with the CdSe-FFT pattern, indicating their crystal lattice alignment is matched each other. High-resolution TEM (HRTEM) (Figure 2f,h) revealed that both the sapphire substrate and nanowalls possessed a single-crystalline quality after the growth, in agreement with the XRD results. Different from the atomic-sharp V-shaped CdS–sapphire interface, the CdS–CdSe interface is atomically continuous because of very small lattice mismatch between CdS and CdSe hexagonal phases. With the known crystallographic data and atomic models, the transversal and horizontal lattice planes of this nanowall are {1120} and {1012} planes, in parallel with [0001]_Al2O3 and [1100]_Al2O3 planes, respectively. Since the surface energy of top {1012} surface is higher than that of lateral {1120} surfaces,[37] surface-adsorbed atoms from the CdSe vapor would diffuse preferentially to the more chemically active {1012} surfaces,[35] leading to the faster CdSe growth along the top surface than that along the sides, which explains the Se distribution in Figure 2c. Different from vertically aligned nanowires grown by lattice-match epitaxy,[38] where the lattice match of nanowire with substrate existed along the nanowire height directions, the smallest lattice mismatch of horizontal nanowalls with sapphire was observed across the nanowall width with [1120]_CdS || [0006]_Al2O3 directions (Figure 2e). This observation is consistent with other works,[35] demonstrating that the nanogroove-guided growth is promising to hold a large tolerance for lattice mismatch between nanostructures and substrates.[29,32,33] In Figure 2g, the selected inverse-FFT image shows that many misfit dislocations exist at the CdS–sapphire interfaces, which is reasonable considering the facts that CdS and sapphire are different crystal structures and the lattice mismatch along [1120]_CdS || [0006]_Al2O3 directions is up to ~4.5%. The lattice fringes across the CdS–CdSe interface, however, are smooth and continuous (Figure 2i) because CdS and CdSe are the same hexagonal crystals with small lattice mismatch, and their crystal lattice alignment is matched each other (Figure 2e). Therefore, heterointerfaces with few misfit dislocations were obtained, which is essential for reducing interface states and carrier-trapping centers, and thus increasing the recombination rate of free carriers as well as the photon-induced current.[39,40]

Under 405 nm laser excitation, red emission was observed from the core–shell region of these nanowalls, whereas only green emission from the CdS-only region (Figure 3a). Spatially resolved photoluminescence (PL) revealed that the PL spectrum from the green (red) emission region has a single peak at 503 nm (708 nm) (Figure 3b). The emission peak energies (2.46 and 1.74 eV) are close to the room-temperature bandgaps of CdS and CdSe, respectively, therein they originate from the band-edge transitions of CdS and CdSe, respectively.[41] The PL spectrum collected at the green–red junction exhibits two peaks, coming from the emission of CdS core and CdSe shell simultaneously. All nanowalls exhibit clean band-edge emission with no obvious trap-level emission observed across the entire nanowall, indicating the high quality of the nanowalls and few defects.[42] 2D PL-intensity mapping images (Figure 3c) revealed that only the CdSe 708 nm peak was detected from the core–shell region, although it is composed of CdS and CdSe compounds. The absence of CdS-green emission from the core–shell region is a result of the reconstructed bandgap diagram.[43–46] We assume that the CdS and CdSe in these nanowalls are an n-type semiconductor due to background impurities/defects and the conductance band offset (ΔE_c) between them is quite small (<0.2 eV) since the synthesis approach is similar to the method reported in most of the experimental results,[43,44,47,48] although some theoretical results suggested that ΔE_c may larger than 0.2 eV.[49] Therefore, although bulk n–n-type CdS–CdSe system suggests a type-I band alignment, they can form a quasi-type-II band alignment through Fermi-level alignment owing to the small ΔE_c and the low effective mass of electrons.[43–48] Consequently, photogenerated electrons are commonly assumed to extend along the entire nanostructure, whereas holes are predicted to be strongly confined in the valence band of the CdSe shell due to the large valence band offset (ΔE_v > 0.5 eV) and high effective mass of holes.[48]

The above characterizations confirmed that self-aligned CdS–CdSe core–shell nanowalls with controlled site, microscale length, high density, and predictable shells were obtained on insulating sapphire surfaces. Consequently, photodetectors can be fabricated in a scalable manner (Figure S8, Supporting Information) without postgrowth transfer, shell-to-core alignment, or selective shell-etching steps, and that devices can be made of aligned arrays of many nanowalls. Figure 4a shows the SEM image of a representative photodetector made of 13 CdS–CdSe core–shell nanowalls, in which electrodes were deposited selectively onto the cores and shells to form Ohmic contacts. Figure 4b plots the current–voltage (I–V) curves under dark condition and illumination of 405 nm light with different
intensities as the bias voltage was applied onto the CdS cores. All curves showed a well-expressed rectification action due to the heterojunction barriers, demonstrating that these CdS–CdSe heterojunctions behave as well-defined diodes. The on/off current ratio is on the order of $10^2$ (Figure S9, Supporting Information) when the bias swept from 5 to $-5$ V. Figure 4c further reveals that these diodes have a very poor photovoltaic response to the 405 nm light, with small open-circuit voltages ($V_{oc}$) and short-circuit currents ($I_{sc}$). As expected, $V_{oc}$ and $I_{sc}$ depend logarithmically and linearly on the light intensity, respectively, on the light intensity ($I_{0}$),

$$\ln(I_{sc}) = qV_{oc}/NkT + \ln(I_{0}),$$

where $q$ is the electronic charge, $N$ is the diode ideality factor, $k$ is the Boltzmann constant, and $I_{0}$ is the reverse saturation current. Linear fitting of a plot of $\ln(I_{sc})$ versus $V_{oc}$ (Figure S10, Supporting Information) yields an $N$ and $I_{0}$ of 1.29 and 561 pA, respectively. The $N$ value is close to the value of an ideal Schottky junction ($N = 1$), indicating the high quality of the CdS–CdSe heterojunctions.

High response speed and high photocurrent gain play key roles for the development of high-performance photodetectors. Unfortunately, a large gain often reduces the response speed, or vice versa, as a result of the exciton recombination at the surface and bulk of nanostructures. The photocurrent of these detectors follows the square change of incident light intensity at the sub-millisecond level (Figure 4d), suggesting a sub-microsecond photocurrent response. The on-current and off-current in each cycle were stable at an order of $10^{-5}$ and $10^{-7}$ A, respectively, resulting in a $10^2$ on/off current ratio, demonstrating the excellent repeatability of the photodetectors, although the off-current and on/off current ratio is still not perfect. In order to determine the rise and fall times accurately, the photocurrent-record time interval was reduced to 35 ns (Figure 4e) from 105 ns (Figure 4d). The rise and fall edges of the photocurrent were fitted by a single-exponential function (Figure 4e), respectively, with time constants of ≈200 ns for both the rise ($\tau_r$) and decay ($\tau_d$) stages. The observation of only one decay time constant for both rise and decay stages indicates...
that the fast recombination of free carriers, instead of the slow recombination of trapped carriers, dominates the photocurrent decay.[33,59–61] Statistical of 10 devices gives $\tau_r = 170–250$ ns and $\tau_d = 160–330$ ns, respectively (Table S2, Supporting Information). The 3 dB bandwidth (half power point, $f_{3dB} = 0.35/\tau_d$[62]) of these photodetectors are 1.4–2.1 MHz, suggesting that these photodetectors could follow the changes of optical signals with on/off frequencies approaching 2 MHz. For example, Figure 4f shows that the relative balance of photocurrent ($I_{on} - I_{off}/I_{on} \times 100\%$) is always larger than 95% as the frequency of the modulated light approaches 500 kHz. Compared with bias voltage, light intensity has a more significant contribution to the submicrosecond response. For example, the photocurrent remains a submicrosecond response when bias voltage was reduced to 1 V (Figure S11, Supporting Information). In contrast, both the rise and fall times reduced rapidly from $\approx 2\mu s$ to $\approx 300$ ns.

Figure 4. Optoelectronic properties of surface-guided CdS–CdSe core–shell nanowalls. a) SEM image of photodetector, and false color was added onto one nanowall to show the CdS-only region (cyan) and CdS–CdSe core–shell region (pink). b) I–V curves under dark condition (black) and 405 nm light illumination with different intensities. c) Zoom-in view of (b) in the range of ±0.2 V, and the inset shows the plot of $V_{oc}$ and $I_{sc}$ as a function of light intensity. d,e) Photocurrent response under illumination of 405 nm light at 10 V bias. The on/off frequency of the light is 10 kHz, and intensity is 740 mW cm$^{-2}$. The time interval for the current acquisition is d) 105 ns and e) 35 ns, respectively. The orange and pink lines in (e) are the exponential fitting for the rise and decay edges, respectively. f) Frequency-dependent balance of photocurrent at 10 V bias and 740 mW cm$^{-2}$. g) Light intensity dependence of rise and fall time at 10 V bias. h) Light intensity dependence of photoresponsivity (pink) and gain factor (cyan) at 10 V bias. i) Model showing the continuous distribution of discrete states. Increased rate of excitation adds more states to the ground states and thereby leads to the shorter lifetime of free carriers. The light yellow and orange regions represent the shallow trapping states for electrons and holes, respectively. The cyan region corresponds to the ground states. The red and green arrows represent the thermal equilibrium process of trapped carriers and recombination of free carriers, respectively. Adapted with permission from ref.[59].
as the light intensity raised to \( \approx 100 \text{ mW cm}^{-2} \), thereafter they approach very slowly to a plateau at \( \approx 200 \text{ ns} \) (Figure 4g).

The gain factor \( \eta \) denotes the number of detected electrons per incident photon and is determined by \( \eta = \frac{R h c (n, \lambda)}{\epsilon I_0} \), where \( R \) is the photoresponsivity, \( h \) is the Planck’s constant, \( c \) is the velocity of light, \( \epsilon \) is the elementary charge, and \( \lambda \) is the laser wavelength. \( R \) is determined by \( R = \frac{I_{ph}}{P S} \), where \( I_{ph} \) is the net current, \( P \) is the light intensity, and \( S \) is the effective illuminated area. Figure 4h plots the light-intensity-dependent \( R \) and \( \eta \) at 10 V bias. It is clear that both \( R \) and \( \eta \) decrease with increasing \( P \) and reach maximum values of \( R = 3.6 \times 10^4 \text{ A W}^{-1} \), \( \eta = 1.1 \times 10^4 \) at the lowest \( P = 54 \text{ mW cm}^{-2} \). A quantitative fitting of \( R \) yields a power-law decrease, \( R \propto P^{-3} \), with the fitting parameter \( \alpha = 0.64 \), which is close to the reported values (\( \alpha = 0.71–0.79 \)).\(^{39,40,64} \) indicating an enhanced scattering or recombination rate of hot carriers as their density increases at higher light intensity.\(^{39,40,64} \) It is worth emphasizing that \( R \) and \( \eta \) are still as high as 1.3\( \times \)10\(^4 \text{ A W}^{-1} \) and 4.4\( \times \)10\(^3 \), respectively, at the highest light intensity we performed, where the shortest response time of 200 ns was achieved. Averaging over 10 devices (Table S2, Supporting Information) yields \( R = 1.2 \times 10^4 \text{ A W}^{-1} \) and \( \eta = 3.8 \times 10^3 \), respectively, at \( P = 740 \text{ mW cm}^{-2} \) and 10 V bias.

As listed in Table 1, the sub-microsecond response of these core-shell nanowalls is similar to the response of the guided CdS nanowalls, being the fastest results ever reported for photodetectors based on bottom-up compound semiconductor nanostructures.\(^{31,65–67} \) The photoresponsivity and gain of the core-shell nanowalls, however, are one order of magnitude higher than those of pure CdS nanowalls. The main reasons for the simultaneous realization of sub-microsecond response and high-gain photocurrent (efficiency) include the improved carrier separation enabled by the quasi-type-II band alignment (Figure 3d) and the abrupt epilayer interfaces are expected to enhance the carrier separation efficiency; consequently, raising the number of free electrons (\( n_f \)). The suppressed \( n_f \) and increased \( n \) eventually result in the ultrafast light response at room temperature. The light intensity dependent response time also has an explanation with the Rose model. With the increase of light intensity, the demarcation lines between shallow trapping and ground states for electrons and holes shift toward the conduction and valence bands, respectively.\(^{60,61} \) The shift of demarcation lines will bring new centers into the role of ground states, leading to an increased \( n_f \) and \( n \). Consequently, \( \tau \) and \( \tau_f \) become shorter at greater light intensity. The photoresponsivity and gain are also expressed as \( R = \frac{[\sigma \tau_L / \hbar c] \tau_f / \tau} {\tau_f / \tau} \) and \( \eta = [\sigma \tau_L / \hbar c] \tau_f / \tau \), respectively, in terms of the absorption coefficient (\( \alpha \)), the nanowall height (\( \tau \)), and the ratio of the lifetime of minority carriers (\( \tau_f \)) to the transit time of majority carriers (\( \tau_r \)). Considering that \( \tau = L^2 / \mu V \), where \( L \) is the electrode spacing, \( \mu \) is the electron mobility, \( V \) is the bias, the photoresponsivity and gain increase linearly with increasing applied bias voltage. As light intensity increases, Auger recombination processes will be introduced and carriers scattering will be enhanced.\(^{39,40} \) The Auger recombination processes lead to reduced \( \tau_f \) while the enhanced carriers scattering results in an increased \( \tau_r \).\(^{39,40} \) which explains the reduced photoresponsivity at higher light intensity in Figure 4h.

### Table 1. Photoconductivity performance based on different semiconductor nanostructures.

| Light [nm] | Intensity [mW cm\(^{-2}\)] | Bias [V] | \( I_{ph} \) [A] | \( I_{cm} \) [A] | \( \tau \) [\( \mu \text{s} \)] | \( \tau_f \) [\( \mu \text{s} \)] | \( R \) [A W\(^{-1}\)] | Gain | Ref. |
|------------|-----------------|-----------|----------------|----------------|----------------|----------------|----------------|--------|------|
| CdS NW\(^{a}\) | 400 | 2.0 | <2 pA | 100 nA | 15 | 15 | | 36–911 | [56] |
| CdSe NW\(^{a}\) | 473 | 1500 | 2.0 | 10\(^{-2}\) A | 3.5 \( \mu \text{A} \) | 2–3 | 2–3 | | | |
| ZnSe NB\(^{a}\) | 405 | 13 | 30.0 | 10 \( \mu \text{A} \) | 10.7 \( \mu \text{A} \) | 70 ms | 0.2 s | | | [31] |
| ZnO NW\(^{a}\) | 370 | – | 5.0 | 29 \( \mu \text{A} \) | 34 \( \mu \text{A} \) | 100 \( \mu \text{A} \) | 360 \( \mu \text{A} \) | | | [66] |
| ZnS NB\(^{a}\) | 320 | – | 5.0 | 10\(^{-14}\) A | 0.6 \( \mu \text{A} \) | 2.57 ms | 1.99 ms | | | [68] |
| GaSb/GaSb Sb NW\(^{a}\) | 1550 | – | 1 | – | <0.5 \( \mu \text{A} \) | 2 ms | 3.7 ms | | 8.5 \( \times \)10\(^{4}\) | [67] |
| CdS–CdSe axial NW\(^{a}\) | 515 | 3.5 | 4.0 | \( \mu \text{A} \) | 1 \( \mu \text{A} \) | 30 ms | 90 ms | | 10\(^{4}\) | [57] |
| CdS–CdSe axial NW\(^{a}\) | 480–640 | 2.86 | 1.0 | 10\(^{-12}\) A | 10\(^{-9}\) A | 68 \( \mu \text{s} \) | 137 \( \mu \text{s} \) | 118 | 3.1 \( \times \)10\(^{2}\) | [58] |
| Guided CdS NW\(^{a}\) | 405 | 2000 | 10.0 | 10\(^{-8}\) A | 10\(^{-4}\) A | <300 ns | <400 ns | 50–171 | 154–525 | [34] |
| This work | 405 | 740 | 10.0 | 10\(^{-2}\) A | 10\(^{-5}\) A | <250 ns | <330 ns | 1.2 \( \times \)10\(^{4}\) | 3.8 \( \times \)10\(^{4}\) | |

\(^{a}\)NW is Nanowire; \(^{b}\)NB is nanobelt; \(^{c}\)NW is nanowall; \(^{d}\)These values are an average over 10 photodetectors.
In summary, a facile approach is presented for site-controlled growth of aligned CdS–CdSe core–shell nanowalls based on the combination of graphoepitaxially guided vapor–liquid–solid growth and selective-area vapor–solid epitaxial growth. This approach offers not only a self-alignment of nanowall themselves, but also a site- and length-controlled shells from the bottom-up, which paves the way to scalable fabrication of nanodevices. As an example, photodetectors were fabricated in a scalable manner without postgrowth alignment, transfer, or shell selective-etching steps. A sub-microsecond response and high-gain photocurrent as well as high photoreponsivity were achieved simultaneously from these photodetectors. Lastly, the proposed approach is not limited to the CdS–CdSe system. In principle, different core–shell heterojunctions can be obtained by changing the core or the shell composition. Therefore, this work indicates that surface-guided growth can be extended to produce horizontally aligned core–shell heterostructures for scalable fabrication of high-performance devices from the bottom-up.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest
The authors declare no conflict of interest.

Keywords
CdS, CdSe, core–shell structures, nanostructures, photodetectors

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