Electron tunneling across a tunable potential barrier

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Abstract. We present an experiment where the elementary quantum electron tunneling process should be affected by an independent gate voltage parameter. We have realized nanotransistors where the source and drain electrodes are created by electromigration inducing a nanometer sized gap acting as a tunnel barrier. The barrier potential shape is in first approximation considered trapezoidal. The application of a voltage to the gate electrode close to the barrier region can in principle affect the barrier shape. Simulations of the source drain tunnel current as a function of the gate voltage predict modulations as large as one hundred percent. The difficulty of observing the predicted behaviour in our samples might be due to the peculiar geometry of the realized tunnel junction.

1. Introduction
Electron tunneling across a thin insulating barrier embedded between two metallic electrodes is a basic example of quantum phenomenon. This pure quantum effect found a spectacular application in the scanning tunneling microscope. Thanks to electron tunneling, atomic resolution was obtained only two years after its invention [1]. Furthermore electron tunneling remains one of the best probes to explore the density of states in bulk materials. Tunneling current depends also on the potential barrier shape in the whole system. Usually the potential profile is determined by the bias voltage and by the spacing between the two electrodes of the tunnel junction. In the following, we present an experimental set-up in which we could modify the potential barrier shape by a third gate electrode. We present simulations showing that the barrier modification should affect the tunnel current voltage characteristics and we compare these predictions with a first experimental test.

2. Sample preparation
The samples were made by conventional nanofabrication technique combined with electromigration [2]. E-beam lithography of a 1 µm wide wire is performed. A 40 nm thick layer of aluminum is deposited in a e-gun evaporator while cooling down the sample at nitrogen temperature. After warming up the sample, a thermal oxidation is performed during ten minutes. This results in an oxidised Al electrode which acts as a local gate. The sample is then processed in air for a second e-beam lithography step defining a suspended mask presenting a 50 nm wide and 100 nm long bridge. A double-angle evaporation technique is adopted to obtain a continuous gold nanowire with a 40 nm large and 20 nm thick constriction in the middle which directly lays on the Al2O3 local gate (see figure 1 a)). In the same step, a large 6 µm pad is designed to obtain a standard Al-Al2O3-Au junction, its transport characteristic allows us to determine the oxide properties.
Source and drain electrodes are obtained by breaking the nanowire by controlled electromigration. Electromigration is the result of a momentum transfer from the electrons to the atoms of the lattice [3]. This happens when a large current density flows through the nanowire and gold atoms start to move under the effect of a wind force due to collisions with electrons. The electromigration is also assisted by temperature and field effect. A 10 mV s\(^{-1}\) voltage ramp is applied to the constriction in series with a resistance (\(R_S = 150 \, \Omega\)) while monitoring the current (see figure 1 b)). The process is realized at room temperature under vacuum (\(P = 10^{-6} \, \text{mb}\)) and is similar to the one used in [4] (see figure 1 c)). As soon as electromigration begins, the voltage ramp is stopped within microsecond time scale to avoid the complete failure of the wire. The highest current density, localized at the constriction, induces atoms displacement. Repeated voltage ramps reduce the constriction size [5] and decreases its conductance to a few \(G_0\), where \(G_0 = \frac{2e^2}{h}\) is the conductance quantum for degenerated spins. The process is stopped as soon as the conductance reaches a value smaller than \(0.1G_0\), which corresponds to low transmitted barriers. For the sample of figure 1c), we obtain a resistance of 140 G\(\Omega\) at 4 K, corresponding to a nanometer size gap.

3. Nanotransistors characterization

Electron transport through a thin insulating barrier is a basic problem of quantum mechanics. The current density is inferred from the electron transmission probability across the potential barrier in the insulator. In the simplest case, the height of the potential barrier at the metal interface is the work function of the metal, respectively \(\Phi_S\) and \(\Phi_D\). In between, neglecting charge accumulation in the insulator, the potential \(\Phi(x)\) interpolates to a line with a slope proportional to the voltage \(V\) on a distance \(L\) (see figure 2 a)) leading to \(\Phi(x) = \Phi_S + eV + (\Phi_D - \Phi_S - eV)\frac{x}{L}\). Neglecting charge accumulation is equivalent to neglect image force. When the voltage is smaller than the work functions of the electrodes, to a good approximation, only electrons at the Fermi level of the injecting electrode contribute significantly to the current. Using a WKB approximation to calculate transmission probability, current voltage relation can be written following the Stratton model as [6]:

\[
I(V) = A \frac{e^2}{\hbar \pi} \frac{e^{-b_1}}{c_1} (1 - e^{-c_1 V})
\]  

Figure 1. a) Optic and SEM images of the sample before the electromigration procedure. b) Schematic of the electronic circuit used for electromigration and electronic transport measurements. c) Current voltage dependence during progressive thinning of the constriction. From top to down, ten successive voltage ramps are performed until the wire conductance reaches a few \(G_0\). In the last ramp, total breaking occurs around a bias voltage of 0.52 V.
with \( b_1 = \alpha \int_0^L \sqrt{\Phi(x)} dx \), \( c_1 = \alpha/2 \int_0^L 1/\sqrt{\Phi(x)} dx \), \( \alpha = 2\sqrt{2m e}/\hbar \). The area of the tunnel junction is noted \( A \), \(-e\) is the electron charge, \( \hbar = \frac{\hbar}{2\pi} \) the reduced Planck constant and \( m \) the effective mass in the insulating part.

\[ \Phi(x) = \frac{2\alpha}{L} \left( \sqrt{\Phi(x)} \right) \]

The current voltage characteristic of the reference tunnel junction shown on figure 2 is also fit to equation 1 using the free parameters \( \Phi_{Au} = 3.0 \) eV, \( \Phi_{Al} = 1.7 \) eV and \( t = 2.0 \) nm and the fixed parameters \( m = 10^{-30} \) kg and \( A = 6 \mu m^2 \) as determined by the SEM image. The determined work functions are close to the bulk ones corrected by the electroaffinity of \( Al_2O_3 \). Note the small thickness of the insulator barrier, \( t \), which should assure a good coupling between the gate electrode and the tunnel barrier.

### 4. Influence of the potential shape

The fundamental ingredient in the Stratton equation 1 is the potential shape \( \Phi(x) \) in the insulating layer. The potential profile can be modified in the case of a local gate strongly coupled to the barrier region. In order to estimate the effect of the gate voltage, we used the geometrical and physical properties as determined in part 3 (see figure 3a)). Simulations of the local gate effect on the barrier shape have been performed using a steepest descent method to solve Poisson’s equation inside the gap. The calculations, no charge accumulation is assumed in the insulator. The potential variation is presented in figure 3b) as a function of the \( z \)-direction and as a function of the gate voltage. As expected, the gate effect is screened by the bulk electrode but the expected modulation of the tunnel current remains as large as 100% for the
highest gate and source drain voltages (see figure 3c)). In our sample, no significant gate effect

![Figure 3.](image)

Figure 3. (Color online) a) Geometry used in the gate effect simulations. The value $L = 2.6$ nm is the source drain distance and $t = 2$ nm is the oxide thickness. b) Top : Influence of the distance to the oxide interface on the potential shape $\Phi$ in the middle of the gap region for $V_G = 0.4$ V: from down to top, $z$ varies between 0 and 4 nm. Bottom : Influence of the gate voltage on the potential shape $\Phi$ in the middle of the gap region at the oxide interface : $V_G$ varies between $-0.4$ V and $0.4$ V by step of $0.2$ V from top to down. c) Corresponding current voltage characteristics calculated with equation 1 by integrating on the area $A$.

was observed on the current voltage characteristics when varying $V_G$ between $-2$ V and 2 V. According to our simulation, this could happen if electronic transport between source and drain takes place through a surface smaller than the estimated $A$ junction area in a region where the gate effect is completely screened. Furthermore, taking into account leaking effect to the gate electrode would only modify the tunnel current by a factor of 1 % for the largest $V$ and $V_G$ considered.

5. Conclusion
Using electromigration and e-beam lithography, we have realized nanotransistors with a nanometer size source drain distance. Simulations of the current voltage characteristics as a function of the gate voltage predict large modulations. The effect has not yet been observed experimentally. Further improvements of the geometry are under investigation to probe the expected behaviour.

Aknowledgement
We thank D. Esteve and all the Quantronics group (SPEC-CEA Saclay) for their support. We thank the Laboratoire Pierre Aigrain in the ENS, Paris and Marco Aprili (LPS Orsay).

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