A steep-slope transistor based on abrupt electronic phase transition

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Collective interactions in functional materials can enable novel macroscopic properties like insulator-to-metal transitions. While implementing such materials into field-effect-transistor technology can potentially augment current state-of-the-art devices by providing unique routes to overcome their conventional limits, attempts to harness the insulator-to-metal transition for high-performance transistors have experienced little success. Here, we demonstrate a pathway for harnessing the abrupt resistivity transformation across the insulator-to-metal transition in vanadium dioxide (VO2), to design a hybrid-phase-transition field-effect transistor that exhibits gate controlled steep (‘sub-kT/q’) and reversible switching at room temperature. The transistor design, wherein VO2 is implemented in series with the field-effect transistor’s source rather than into the channel, exploits negative differential resistance induced across the VO2 to create an internal amplifier that facilitates enhanced performance over a conventional field-effect transistor. Our approach enables low-voltage complementary n-type and p-type transistor operation as demonstrated here, and is applicable to other insulator-to-metal transition materials, offering tantalizing possibilities for energy-efficient logic and memory applications.
Metal-oxide-semiconductor field-effect transistors (MOSFETs) have been the workhorse of digital computation. In a conventional MOSFET (Fig. 1a), a change in the drain-to-source current \( (I_{DS}) \) can be induced by the application of a transverse electric field across the gate dielectric by means of the third gate terminal. This field lowers the potential energy barrier separating the source and the channel, exponentially increasing the number of carriers traversing the channel. At room temperature, a minimum change of 60 mV in the gate bias \( (V_{GS}) \) is required to effectuate a decade change in \( I_{DS} \), setting up the so-called ‘60 mV per decade’ limit, also known as the ‘Boltzmann limit’ (Fig. 1a). Stemming from the statistical distribution of free and independent carriers in conventional semiconductors and determined by the thermal voltage \( kT/q \) \((k: \text{Boltzmann constant}; T: \text{temperature}; q: \text{electron charge})\), this fundamental limit restricts transistor performance, particularly at low-operating voltages \(^{1,2} \), and has motivated the exploration of FETs that harness collective carrier responses \(^{3-13} \). Such collective behaviour—wherein a small external perturbation can trigger an aggregated change in the ground state of the system—can produce internal amplification; and provide a pathway to overcome the Boltzmann limit to enable FET’s with sub-\( kT/q \) \((kT/q; \eta > 1)\) switching slope and superior performance at low voltages. Particularly, in insulator-to-metal transition (IMT) materials \(^{14} \) that exhibit strong correlation, like \( \text{VO}_2 \) \((\text{refs} \ 15-18) \), the collective response to external perturbation \( (\text{temperature}^{19,20}\ \text{pressure}^{21,22}\ \text{and electrical stimulus}^{23-28}) \) can be the ‘melting’ of carriers, marking an electronic phase transformation where the electrons localized at atomic sites change to an itinerant state (Fig. 1b). This phase transformation amplifies the free-carrier concentration \(^{29} \), and in the case of \( \text{VO}_2 \), manifests itself as a sharp change in resistivity up to five orders in magnitude \(^{30} \) at \( \sim 340 \text{K} \). However, attempts to realize IMT-based three-terminal transistor devices with a solid-state gate dielectric to induce the phase transition directly in the channel material have experienced only limited success \(^{31-33} \). Further, the alternate approach of using an ionic liquid as the gate dielectric, which is the focus of current research \(^{34-39} \), is typically slow \(^{40-42} \) and susceptible to electrochemical effects \(^{43} \). These constraints have restricted the utilization of this collective phenomenon in FETs for advanced high-performance electronic applications.

Here, we explore a novel transistor architecture that harnesses the abrupt free-carrier amplification across the phase transition in \( \text{VO}_2 \) using a conventional MOSFET. By electrically coupling the \( \text{VO}_2 \) in series with the source of a conventional MOSFET (Fig. 1b), we design a hybrid-phase-transition-FET (hyper-FET) wherein, for a given drain-to-source voltage \( (V_{DS}) \), the gate bias \( V_{GS} \) modifies the current \( I_{DS} \) flowing through the MOSFET channel and the \( \text{VO}_2 \) in series, triggering an abrupt phase transformation in \( \text{VO}_2 \). The proposed hyper-FET not only exhibits steep-slope characteristics but also circumvents the need for a direct field-induced phase transition in \( \text{VO}_2 \) with a solid-state gate dielectric. Further, the abrupt resistivity switching of \( \text{VO}_2 \) in the hyper-FET configuration, which is the origin of the steep-slope characteristics, induces a negative differential resistance (NDR) across \( \text{VO}_2 \) that results in internal voltage amplification which consequently enhances the hyper-FET’s performance beyond that of a conventional MOSFET.

**Results**

**Experimental demonstration and operation principle.** Figure 2a illustrates the schematic of an experimental hyper-FET consisting of a two-terminal \( \text{VO}_2 \) device in series with the channel of a conventional Si n-MOSFET \((\text{individual device characteristics are shown in Supplementary Fig. 1 and discussed in Supplementary Note 1)} \). All measurements in this work are performed at room temperature.
differential resistance NDR (red) across the phase transition in VO₂. The current–voltage dynamics through a feedback and inducing a negative channel resistance of the MOSFET acts as a series resistor, modifying the MOSFET in series, illustrating the electrically triggered abrupt IMT. The gate-source voltage \( V_{GS} \) proportion to their respective resistances; and the current \( I_{DS} \) reveals the steep-slope (4 V/4 mV) of the hyper-FET during the forward transition \( V_{DS} \) as a function of the temperature \( T=300 \text{K} \). The abrupt turn-ON and turn-OFF of the IMT/MIT in VO₂ results in steep-slope (40 mV per decade) characteristics, both during the forward and the reverse \( V_{GS} \) sweep. We emphasize that the current change \( \Delta I_{DS} \) is abrupt and the extracted value of \( S \) is limited by the voltage resolution (1 mV). The corresponding output characteristics \( (I_{DS}−V_{DS}) \) of the hyper-FET (Fig. 2d) show excellent \( I_{DS} \) saturation behaviour, which is paramount for small signal amplification. This is in contrast to the traditional IMT-based transistor design where the IMT occurs in the channel material. Such a transistor is unlikely to demonstrate current saturation since the design envisages the IMT channel to have a metallic character in the transistor’s ON-state which fundamentally cannot sustain a drain side depletion region.

Internal amplification in the hyper-FET. To elucidate the internal amplification, we analyze the current–voltage dynamics across VO₂ in the hyper-FET configuration (Fig. 2e). In this series combination, the abrupt IMT results in an NDR across the VO₂. Such an NDR is induced because when the VO₂ resistance decreases abruptly, it results in (a) an increase in \( I_{DS} \) \( (\Delta I_{DS}) \) of the VO₂ device and the MOSFET channel in series; (b) a reduction in the voltage across the VO₂ device \( V_{VO₂} \) \( (−\Delta V_{NDR}) \) (see Supplementary Fig. 2 and Supplementary Note 2 for discussion on the NDR in VO₂). The effective gate-to-source voltage across the MOSFET \( (V_{GS}: \text{internal node in Fig. 2a}) \) when VO₂ is in the insulating state (hyper-FET OFF-state) is \( V_{GS} = V_{GS} − V_{VO₂} \). It can be observed that the voltage across the insulating VO₂ results in an additional voltage drop \( (−V_{VO₂}) \) in the effective gate-to-source voltage \( V_{GS} \). Across the IMT in VO₂ which induces the NDR, this voltage drop \( (−V_{VO₂}) \) reduces by \( \Delta V_{NDR} \) (therefore increasing \( V_{GS} \) by \( \Delta V_{NDR} \) Fig. 2a). Thus, the additional voltage drop \( (−V_{VO₂}) \) in \( V_{GS} \) when VO₂ is in the insulating state results in a drastic reduction in the OFF-state current \( (I_{DS,OFF}) \) of the hyper-FET in comparison to the stand-alone MOSFET, whereas the reduction in ON-state current \( (I_{DS,ON}) \) is much less significant since the voltage drop across the metallic VO₂ is small; this results in an overall enhanced current change that is, a higher \( I_{DS,ON}/I_{DS,OFF} \) ratio (see Supplementary Fig. 3 and Supplementary Note 3 for additional details and simulations). We model the MOSFET with VO₂ combination as an equivalent common-source transistor circuit (Fig. 2a) where:

\[
\frac{\Delta I_{DS}}{\Delta V_{GS}} = \frac{g_m}{1 + g_m R_{VO₂}} \tag{1}
\]

Here, \( g_m \) is the transconductance of the stand-alone MOSFET. Across the IMT, the VO₂ exhibits an NDR \( (R_{VO₂} = −\Delta V_{NDR}/\Delta I_{DS}) \), and therefore equation (1) evolves to:

\[
\frac{\Delta I_{DS}}{\Delta V_{GS}} |_{\text{hyper-FET}} = \frac{g_m}{1 − g_m \left( \frac{\Delta V_{NDR}}{\Delta I_{DS}} \right)_{\text{IMT}}} = \beta g_m \tag{2}
\]

where \( \beta = \frac{1}{1 − g_m \left( \frac{\Delta V_{NDR}}{\Delta I_{DS}} \right)_{\text{IMT}}} > 1 \)

Figure 2 | Experimental demonstration of a VO₂-based hyper-FET. (a) Schematic of a hyper-FET consisting of a two-terminal VO₂ device (\( L_{VO₂} = 4 \mu m; W_{VO₂} = 2 \mu m \)) in series with the channel of a conventional Si n-MOSFET (\( L = 100 \mu m; W = 100 \mu m \)). \( V_{VO₂} \), is the voltage across the VO₂ device and \( V_{GS} \) is the effective gate-to-source voltage across the MOSFET. (b) \( I_{DS}−V_{GS} \) transfer characteristics of the hyper-FET exhibiting abrupt and reversible modulation of the channel current \( I_{DS} \) as a function of the gate-source voltage \( V_{GS} \). The abrupt turn-ON and turn-OFF of the hyper-FET corresponds to the IMT and MIT in VO₂, respectively. (c) Switching slope \( (S) \) as a function of \( I_{DS} \) revealing the steep-slope characteristics (\( S \approx 60 \text{mV per decade} \)) of the hyper-FET during the forward and reverse gate bias sweep. (d) Output characteristics (\( I_{DS}−V_{DS} \)) of the hyper-FET with excellent current saturation. (e) Current versus voltage characteristics of the VO₂ device with (red) and without (blue) the MOSFET in series, illustrating the electrically triggered abrupt IMT. The channel resistance of the MOSFET acts as a series resistor, modifying the current–voltage dynamics through a feedback and inducing a negative differential resistance NDR (red) across the phase transition in VO₂. The NDR reduces the voltage across the VO₂ by \( \Delta V_{NDR} \). The current has been normalized to the width of the Si n-MOSFET to show that the abrupt IMT in VO₂ triggers the abrupt turn-ON of the hyper-FET shown in b.
Equation (2) indicates that in a particular gate-voltage window, the amplified differential transconductance ($\beta g_m > 1$) of the hyper-FET facilitates a larger change in current compared with the stand-alone MOSFET. The VO$_2$, therefore, sets up an internal feedback loop that allows the hyper-FET to exhibit a $\sim 20\%$ higher ON-state current ($I_{DS,ON}$) compared with the stand-alone MOSFET over a gate-voltage window of 0.8 V at matched OFF-state current.

**Low-voltage n-type and p-type hyper-FET operation.** Next, we focus on the MOSFET component of the hyper-FET. The gate-bias triggers the phase transition in VO$_2$ by enabling the MOSFET to source the same currents at low $V_{GS}$ and $V_{DS}$. This motivates the integration of scaled, high-$g_m$-advanced transistor architectures like FinFETs fabricated on channel materials having mobilities higher than that of silicon to design a low-voltage hyper-FET (Figs 3 and 4).

Figure 3a illustrates a scaled hyper-FET consisting of a scaled In$_{0.7}$Ga$_{0.3}$As quantum-well multi-channel FinFET ($L_g = 500$ nm) (see Supplementary Fig. 4 and Supplementary Note 4 for fabrication method) in series with VO$_2$ ($L_{VO2} = 200$ nm; $W_{VO2} = 1$ $\mu$m). Figure 3b shows the transfer characteristics of the hyper-FET and its constituent FinFET, shown in Fig. 3d, also reflect the $I_{DS}$ enhancement.

We also demonstrate a p-type hyper-FET since complementary operation, similar to the complementary metal-oxide-semiconductor (CMOS) logic family, is imperative for low standby-power digital applications. Two-terminal VO$_2$ devices exhibit reversible switching in both positive and negative voltage polarities (Supplementary Fig. 1) which allows for electrical integration with a p-channel FinFET to enable p-type hyper-FET operation. Figure 4a shows the schematic of a p-type hyper-FET constructed using a p-channel Ge quantum-well multi-channel FinFET (see Supplementary Fig. 4 and Supplementary Note 4 for fabrication method) in series with VO$_2$ ($L_{VO2} = 200$ nm; $W_{VO2} = 1$ $\mu$m). Figure 4b,d shows the transfer characteristics and the corresponding output characteristics of the p-type hyper-FET and its constituent FinFET, respectively.

The p-type hyper-FET also exhibits an enhanced $I_{SD,ON}/I_{SD,OFF}$ ratio over a $V_{GS}$ range of $-0.5$ V, and thus a $\sim 60\%$ enhancement in $I_{SD,ON}$ at matched $I_{SD,OFF}$ (Fig. 4c).
The hyper-FET is a device concept that harnesses the phase transition in the IMT material, VO₂, to enable room temperature, steep-slope, n-type and p-type transistor operation with enhanced performance. These experimental results motivate the realization of a scaled, monolithic hyper-FET design entailing heterointegration of the IMT material with the conventional MOSFET, which can adversely affect its ON-state current (and therefore that of the hyper-FET), and that of the VO₂, which may possibly affect the magnitude of abrupt current change across the IMT. Further, scaling and optimizing the VO₂ and the MOSFET properties to enable a scaled hyper-FET device with low OFF-state leakage current relevant to low-power circuit applications would be key factors in realizing a hyper-FET-based hardware platform that can augment current state-of-the-art technology.

The hyper-FET, demonstrated here, is a manifestation of a design methodology that consolidates the unique properties of phase transition materials like abrupt and reversible resistivity switching, arising from collective carrier dynamics and usually inaccessible in a conventional semiconductor, with the robust field-induced switching dynamics of a conventional MOSFET. Our approach harnesses the abrupt IMT in VO₂ in the much-desired three-terminal transistor configuration, circumventing the need for direct electric field-induced phase transition. Furthermore, the generality of the hyper-FET design also facilitates this transistor architecture to be extended to other insulator–metal transition systems thus opening the doors to using electronic phase transition materials in digital applications.

References
1. Ionescu, A. M. & Riel, H. Tunnel field-effect transistors as energy-efficient electronic switches. Nature 479, 329–337 (2011).
2. Zhirnov, V. V. & Cavin, R. K. Nanoelectronics: negative capacitance to the rescue? Nat. Nanotechnol. 3, 77–78 (2008).
3. Markov, I. L. Limits on fundamental limits to computation. Nature 512, 147–154 (2014).
4. Cavin, R. K., Lugli, P. & Zhirnov, V. V. Science and engineering beyond Moore’s law. Proc. IEEE 100, 1720–1749 (2012).
5. Mannhart, J. & Haensch, W. Put the pedal to the metal. Nature 487, 436–437 (2012).
6. Reich, E. S. Metal oxide chips show promise. Nature 495, 17 (2013).
7. Zhou, Y. & Ramanathan, S. Correlated electron materials and field effect transistors for logic: a review. Crit. Rev. Solid State Mater. Sci. 38, 286–317 (2013).
8. Inoue, I. H. & Rozenberg, M. J. Taming the Mott transition for a novel Mott transistor. Adv. Funct. Mater. 18, 2289–2292 (2008).
9. Newns, D. M. et al. Mott transition field effect transistor. Appl. Phys. Lett. 73, 780–782 (1998).
10. Bernstein, K., Cavin, R. K., Porod, W., Seabaugh, A. C. & Welser, J. Device and architectures outlook for beyond CMOS switches. Proc. IEEE 98, 2169–2184 (2010).
11. Inoue, I. H. Electrostatic carrier doping to perovskite transition-metal oxides. Semicond. Sci. Technol. 20, S112–S120 (2005).
12. Ahn, C. H., Triscone, J.-M. & Mannhart, J. Electric field effect in correlated oxide systems. Nature 424, 1015–1018 (2003).
13. Chakhalian, J., Millis, A. J. & Rondinelli, J. Whither the oxide interface. Nat. Mater. 11, 92–94 (2012).
14. Imada, M., Fujimori, A. & Tokura, Y. Metal-insulator transitions. Rev. Mod. Phys. 70, 1039–1263 (1998).
15. Moriya, I. Collective excitations which show a metal-to-insulator transition at the Neel temperature. Phys. Rev. Lett. 3, 34–36 (1959).
16. Berglund, C. N. & Guggenheim, H. J. Electronic properties of VO₂ near the semiconductor-metal transition. Phys. Rev. 185, 1022–1033 (1969).
17. Wentzcovitch, R. M., Schulz, W. W. & Allen, P. B. VO₂: Peierls or Mott-Hubbard? A view from band theory. Phys. Rev. Lett. 72, 3389–3392 (1994).
18. Rice, T. M., Launois, H. & Pouget, J. P. Comment on 'VO₂: Peierls or Mott-Hubbard? A view from band theory'. Phys. Rev. Lett. 73, 3042 (1994).
19. Qazilbash, M. M. et al. Mott transition in VO₂ revealed by infrared spectroscopy and nano-imaging. Science 318, 1750–1753 (2007).
20. Zhang, S., Chou, J. Y. & Lauhon, L. J. Direct correlation of structural domain formation with the metal insulator transition in a VO₂ nanobeam. Nano Lett. 9, 4527–4532 (2009).
21. Cao, J. et al. Strain engineering and one-dimensional organization of metal-insulator domains in single-crystal vanadium dioxide beams. Nat. Nanotechnol. 4, 732–737 (2009).
22. Park, J. H. et al. Measurement of a solid-state triple point at the metal-insulator transition in VO₂. Nature 500, 431–434 (2013).
23. Kim, H.-T. et al. Mechanism and observation of Mott transition in VO₂ -based two- and three-terminal devices. New J. Phys. 6, 052 (2004).
24. Kim, B.-J. et al. Micrometer X-ray diffraction study of VO₂ films: separation between metal-insulator transition and structural phase transition. Phys. Rev. B 77, 235401 (2008).
25. Cao, J. et al. Constant threshold resistivity in the metal–insulator transition of VO₂. Phys. Rev. B 82, 241101 (2010).
26. Zimmers, A. et al. Role of thermal heating on the voltage induced insulator-metal transition in VO₂. Phys. Rev. Lett. 110, 056601 (2013).
27. Freeman, E. et al. Nanoscale structural evolution of electrically driven insulator to metal transition in vanadium dioxide. Appl. Phys. Lett. 103, 263109 (2013).
28. Stefanovich, G., Bergman, A. & Stefanovich, D. Electrical switching and Mott transition in VO₂. J. Phys. Condens. Matter 12, 8837–8845 (2000).
29. Ruzmetov, D., Heiman, D., Claflin, B., Narayanamurti, V. & Ramanathan, S. Hall carrier density and magnetoresistance measurements in thin-film vanadium dioxide across the metal-insulator transition. Phys. Rev. B 79, 153107 (2009).
30. Ladd, L. A. & Paul, W. Optical and transport properties of high quality crystals of V₂O₅ near the metallic transition temperature. Solid State Commun. 7, 425–428 (1969).
31. Ruzmetov, D., Gopalakrishnan, G., Ko, C., Narayanamurti, V. & Ramanathan, S. Three-terminal field effect devices utilizing thin film vanadium oxide as the channel layer. J. Appl. Phys. 107, 114516 (2010).
32. Borisov, P. P., Velichko, A. A., Bergman, A. L., Stefanovich, G. B. & Stefanovich, D. G. The effect of electric field on metal-insulator phase transition in vanadium dioxide. Tech. Phys. Lett. 28, 406–408 (2002).
33. Sengupta, S. et al. Field-effect modulation of conductance in VO₂ nanobeam transisitors with HfO₂ as the gate dielectric. Appl. Phys. Lett. 99, 062114 (2011).
34. Nakano, M. et al. Collective bulk carrier delocalization driven by electrostatic surface charge accumulation. Nature 487, 459–462 (2012).
35. Liu, K. et al. Dense electron system from gate-controlled surface metal-insulator transition. Nano Lett. 12, 6272–6277 (2012).
36. Shi, J., Ha, S. D., Zhou, Y., Schoofs, F. & Ramanathan, S. A correlated nickelate synaptic transistor. Nat. Commun. 4, 2676 (2013).
37. Shi, J., Zhou, Y. & Ramanathan, S. Colossal resistance switching and band gap modulation in a perovskite nickelate by electron doping. Nat. Commun. 5, 4860 (2014).
38. Hashimoto, T. et al. Gate control of electronic phases in a quarter-filled manganese. Sci. Rep. 3, 2904 (2013).
39. Scherwitzl, R. et al. Electric-field control of the metal-insulator transition in ultrathin NdNiO₃ films. Adv. Mater. 22, 5517–5520 (2010).
40. Zhou, Y. & Ramanathan, S. Relaxation dynamics of ionic liquid—VO₂ interfaces and influence in electric double-layer transistors. J. Appl. Phys. 111, 084508 (2012).