Stochastic Gradient Descent on Highly-Parallel Architectures

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Abstract

There is an increased interest in building data analytics frameworks with advanced algebraic capabilities both in industry and academia. Many of these frameworks, e.g., TensorFlow and BIDMach, implement their compute-intensive primitives in two flavors—as multi-thread routines for multi-core CPUs and as highly-parallel kernels executed on GPU. Stochastic gradient descent (SGD) is the most popular optimization method for model training implemented extensively on modern data analytics platforms. While the data-intensive properties of SGD are well-known, there is an intense debate on which of the many SGD variants is better in practice. In this paper, we perform a comprehensive study of parallel SGD for training generalized linear models. We consider the impact of three factors—computing architecture (multi-core CPU or GPU), synchronous or asynchronous model updates, and data sparsity—on three measures—hardware efficiency, statistical efficiency, and time to convergence. In the process, we design an optimized asynchronous SGD algorithm for GPU that leverages warp shuffling and cache coalescing for data and model access. We draw several interesting findings from our extensive experiments with logistic regression (LR) and support vector machines (SVM) on five real datasets. For synchronous SGD, GPU always outperforms parallel CPU—they both outperform a sequential CPU solution by more than 400X. For asynchronous SGD, parallel CPU is the safest choice while GPU with data replication is better in certain situations. The choice between synchronous GPU and asynchronous CPU depends on the task and the characteristics of the data. As a reference, our best implementation outperforms TensorFlow and BIDMach consistently. We hope that our insights provide a useful guide for applying parallel SGD to generalized linear models.

1 INTRODUCTION

Stochastic gradient descent (SGD) is the most popular optimization method to train analytics models, e.g., the back-propagation algorithm for deep neural networks [4], in a wide variety of application domains ranging from image [16] and speech [18] recognition to finance [10]. SGD is implemented in a form or another by every modern analytics system, including Google’s Brain [9], Microsoft’s Project Adam [6] and Vowpal Wabbit [2], IBM’s SystemML [13], Pivotal’s MADlib [17], and Spark’s MLlib [34]. Since these billion-dollar enterprises depend on processes which rely on SGD, it is important to understand its optimal behavior and limitations on modern computing architectures.

Motivation. Over the past decade, CPU design has been moving towards highly-parallel architectures with tens of cores on a die. The culmination of this trend is best exemplified by the current Graphics Processing Units (GPU) having thousands of cores. GPUs are assumed to be the ideal platform for analytics model training due to the compute-intensive nature of the task. This is exemplified by the extensive GPU support across many analytics frameworks, e.g., Caffe [2], TensorFlow [3], MXNet [4], BIDMach [5], SINGA [35], Theano [6] and Torch [7]. Published results that compare CPU
and GPU implementations, however, do not support the assumption that GPU is always superior [23, 9, 1]. Quite the opposite, it is often the case that the CPU optimizer outperforms the GPU implementation, even though the degree of parallelism is much lower. A possible reason is the choice of the SGD algorithm. The asynchronous Hogwild-family of algorithms [25, 12, 39, 32, 8, 30] are the preferred SGD implementation on multi-core CPUs due to their simplicity – the parallel code is identical to the serial one, without any synchronization primitives – and near-linear scaling across a variety of analytics tasks [31, 24, 11]. The SGD solutions on GPU resort to a synchronous implementation in which only the highly-optimized linear algebra kernels are offloaded to the GPU. The reasons behind this strategy are the original role GPUs had as accelerators for certain classes of computations and the intricate data access pattern incurred by asynchronous execution. The algorithmic difference in model update strategy – which is an open debate both in theoretical circles [5, 40] and practice [1] – makes a direct comparison between SGD on CPU and GPU challenging.

As far as we know, there is no work that performs an in-depth comparison across architectures and SGD algorithms. Given its central role in analytics training, we believe it is imperative to identify which SGD algorithm performs better on which architecture and what type of data.

**Problem.** We briefly present the setup for model training using SGD. The input data is a matrix in $\mathbb{R}^{N \times d}$ containing $N \cdot d$-dimensional training examples. The goal is to find a $d$-dimensional vector that minimizes the (convex) loss function over the examples specific to each model. SGD makes several complete passes over the input data and updates the model one or several times in each pass. SGD performance is measured by the time it takes to reach the loss function minimum. This depends both on the number of passes over the data and the time per pass. In parallel SGD, the input data is partitioned across threads which share a single common model. While this reduces the time per pass, it has the potential to increase the number of passes. The overall effect depends on several factors—including parallelization strategy, model update, data characteristics, and loss function type.

**Contributions.** In this paper, we perform the first comprehensive study of parallel SGD for training generalized linear models that investigates the combined impact of three axes – computing architecture, model update strategy, and data sparsity – on three measures—hardware efficiency, statistical efficiency, and overall time to convergence. We allocate a significant part of the study to the design of a novel asynchronous SGD algorithm on GPU – a missing topic in the existing literature – that explores exhaustively possible data organization, access, and replication alternatives. To this end, we introduce an optimized asynchronous SGD algorithm for GPU that leverages architectural characteristics such as warp shuffling and cache coalescing for data and model access.

![Figure 1: Exploratory axes.](image1)

**Figure 1: Exploratory axes.**

**Figure 2: Performance axes.**

**Exploratory axes.** Figure[1] depicts the space of the three axes studied in this work. On the computing architecture axis, we consider multi-core CPUs with Non-Uniform Memory Access (NUMA) and many-core GPUs with wide Single Instruction Multiple Data (SIMD) processing units. The specific representatives of the two architectures we use in our work are a dual-socket machine with two 14-core 28-thread Intel Xeon E5-2660 v4 CPUs (56 threads overall, 256 GB memory) and an NVIDIA Tesla K80 GPU with 2496 cores, a 32-wide SIMD unit, and 24 GB memory. Both of them are top-of-the-line representatives in their architectural class. The model update strategies we consider are synchronous and asynchronous. Synchronous updates follow a transactional semantics and allow a single thread to
update the model. While this strategy limits the range of parallel execution inside the SGD algorithm, it is suitable for batch-oriented high-throughput GPU processing. In the asynchronous strategy, multiple threads update the model concurrently. Our focus is on the Hogwild algorithm which ignores any synchronization to the shared model. Data sparsity represents the third axis. At one extreme, we have dense data in which there is a non-zero entry for each feature in every training example. This allows for a complete dense 2-D matrix representation. When the model is large, it is often the case that the examples have only a few non-zero features. A sparse matrix format, e.g., Compressed Sparse Row (CSR), is the only alternative that fits in memory in this case.

Out of the eight possible combinations, a limited set is implemented in practice—the full circles in Figure 1. The majority of the GPU solutions implement synchronous model updates over dense data, while the CPU implementations use asynchronous Hogwild which is suited for sparse data—the darker circles in the figure. In this paper, we explore the complete space and map the remaining combinations. We design an efficient Hogwild algorithm for GPU that is carefully tuned to the underlying hardware architecture, the SIMD execution model, and the deep GPU memory hierarchy. The considerably larger number of threads available on the GPU and their complex memory access pattern pose significant data management challenges in achieving an efficient implementation with optimal convergence. The Hogwild GPU kernel considers data access path and replication strategies for data and the model to identify the optimal configuration for a given task-dataset input. Moreover, we introduce specific optimizations to enhance the coalesced memory access for SIMD processing. Synchronous SGD on CPU turns out to be a simplification of the GPU solution. Instead of executing the linear algebra kernels on the GPU, invoke functions on the CPU. This is easily achieved by using computational libraries with dual CPU and GPU support, e.g., ViennaCL. Since the CPU functions do not require data transfer, they have the potential to outperform a sequence of GPU kernels that are not cross-optimized. The massive number of powerful threads in our testbed CPU provides an additional boost in performance.

Performance axes. Figure 2 depicts the three axes across which we measure the performance of the SGD algorithms. The hardware efficiency measures the average time to do a complete pass — or iteration — over the training examples. Ideally, the larger the number of physical threads, the shorter an iteration takes since each thread has less data to work on — thus, higher hardware efficiency. In practice, though, this holds only when there is no interaction between threads — even then, the size and location of data can be limiting factors. In asynchronous SGD, however, the model is shared by all (or a group of) the threads. This poses a difficult challenge both in the CPU and GPU case. For CPU, the implicit cache coherency mechanism across cores can decrease the hardware efficiency dramatically. Non-coalesced memory accesses inside a SIMD unit have the same effect on GPU. The statistical efficiency measures the number of passes over the data until a certain value of the loss function is achieved, e.g., within 1% of the minimum. This number is architecture-independent for synchronous model updates which are executed at the end of each pass. In the case of asynchronous model updates during a data pass, however, the number and order of updates may have a negative impact on the statistical efficiency. The third performance axis is represented by the time to convergence. This is, essentially, the product between the hardware and statistical efficiency. The reason we include it as an independent axis is because there are situations when two algorithms have reversed hardware and statistical efficiency — algorithm A has better hardware efficiency than algorithm B and worse statistical efficiency — and only the time to convergence allows for a full comparison. Such a case is common for synchronous and asynchronous updates and for CPU and GPU execution, respectively.

Summary of results. We organize the results based on the components of the exploratory axes. In the following, we present only the main findings, while we discuss the details in the experimental evaluation (Section 6):

- For synchronous SGD, GPU is always faster than parallel CPU in time per iteration and, thus, in time to convergence. The gap between GPU and parallel CPU is more than 5X on sparse data, while super-linear speedup of more than 400X is achieved over sequential CPU on cached data.
- The optimized asynchronous Hogwild algorithm we design for GPU uses different data access path + model replication + data replication configurations for different tasks and datasets — identifying the optimal configuration is highly-dependent on all these properties. However, even with these optimizations, asynchronous GPU outperforms (parallel) CPU in time to convergence only in a limited number of situations despite better hardware efficiency — the reason is poor statistical efficiency due to heavy model update conflicts.
- While GPU is the optimal architecture for synchronous SGD and CPU is optimal for asynchronous SGD, choosing the better of synchronous GPU and asynchronous CPU is task- and dataset-dependent.
Our SGD implementations always outperform the synchronous solutions from TensorFlow and BIDMach in time per iteration, number of iterations to convergence, and time to convergence.

Outline. In Section 2 we introduce SGD and classify it according to the exploratory axes. The parallel architecture of multi-core CPUs and modern GPUs is presented in Section 3. The SGD implementation and its optimizations are discussed in Section 4—synchronous—and Section 5—asynchronous. Section 6 presents the experimental results. Related work is discussed in Section 7 while Section 8 concludes the paper.

2 STOCHASTIC GRADIENT DESCENT

Consider the following model training problem with a linearly separable objective function:

\[ \Lambda(\vec{w}) = \min_{\vec{w} \in \mathbb{R}^d} \sum_{i=1}^{N} f(\vec{w}; \vec{x}_i, y_i) \]  \hspace{1cm} (1)

in which a \(d\)-dimensional vector \(\vec{w}\), \(d \geq 1\), i.e., the model, has to be found such that the objective function is minimized. The constants \(\vec{x}_i\) and \(y_i\), \(1 \leq i \leq N\), correspond to the feature vector of the \(i^{th}\) data example and its scalar label, while \(f\) is the loss. For example, the loss corresponding to binary classification with logistic regression (LR) and support vector machines (SVM) is \(f_{LR}(\vec{w}) = \log(1 + e^{-y_i \vec{x}_i \cdot \vec{w}})\) and \(f_{SVM}(\vec{w}) = \max(0, 1 - y_i \vec{x}_i \cdot \vec{w})\), respectively.

SGD is an iterative optimization algorithm for solving this class of model training problems. It starts from an arbitrary model which is updated iteratively based on a batch of \(B\) random training examples \(\vec{X}_k\) and their corresponding scalar labels \(\vec{Y}_k\). The updated model is computed by moving along the opposite direction of the loss function gradient \(\nabla \Lambda(\vec{w})\). For example, the gradients for LR and SVM are defined as:

\[ \frac{\partial f_{LR}(\vec{w})}{\partial w_j} = x_{ij} \left( \frac{y_i e^{-y_i \vec{x}_i \cdot \vec{w}}}{1 + e^{-y_i \vec{x}_i \cdot \vec{w}}} \right) \]

\[ \frac{\partial f_{SVM}(\vec{w})}{\partial w_j} = \begin{cases} -y_i x_{ij}, & \text{if } y_i \vec{x}_i \cdot \vec{w} < 1 \\ 0, & \text{otherwise} \end{cases} \]

2.1 Batch and Incremental SGD

The step size \(\alpha\), the batch size \(B\), and the number of iterations or epochs \(t\) are parameters specific to SGD. They are known as hyper-parameters of the model training problem, wherein the dimensions of \(\vec{w}\) are typically called the parameters of the model. Depending on the value of \(B\), SGD can be classified into incremental (\(B = 1\)), mini-batch (\(1 < B < N\)), and batch (\(B = N\)). While mini-batch is standard SGD, incremental and batch correspond to extreme cases of \(B\) which allow for an essential data access optimization. Random access to the training examples is replaced by sequential access which is orders of magnitude more efficient—especially for massive data that do not fit in the primary storage. Moreover, they discard the batch size hyper-parameter, thus, simplifying the optimization algorithm.

Algorithm 1 Stochastic Gradient Descent (SGD)

Require:

- Training examples \(\vec{X} \in \mathbb{R}^{N \times d}\) and their labels \(\vec{Y} \in \mathbb{R}^{N}\)
- Loss function \(f\) and its gradient \(\nabla \Lambda\)
- Initial model \(\vec{w} \in \mathbb{R}^d\) and step size \(\alpha \in \mathbb{R}\)
- Number of epochs \(t\) and batch size \(B\)

1. for \(k = 1\) to \(t\) do

   **OPTIMIZATION EPOCH**

2. Select a random subset \(\vec{X}_k = \{\vec{x}_{i1}, \ldots, \vec{x}_{iB}\}\) of \(B\) examples and their labels \(\vec{Y}_k = \{y_{i1}, \ldots, y_{iB}\}\)
3. Compute gradient estimate: \(\vec{g} \leftarrow \sum_{k} \vec{X}_k \cdot \vec{Y}_k \cdot \nabla \Lambda(\vec{w})\)
4. Update model: \(\vec{w} \leftarrow \vec{w} - \alpha \vec{g}\)
5. end for
6. return \(\vec{w}\)

The optimization epoch in the SGD algorithm becomes a linear scan over the training dataset in which the gradient is incrementally computed (batch SGD) and the model updated (incremental SGD). The differences between the two
algorithms are in how the gradient is computed (estimated) and how many times the model is updated. In batch SGD, the gradient is computed exactly using all the \( N \) examples in the training dataset and the model is updated only once per epoch. Incremental SGD is at the other extreme. The gradient is approximated using a single example and the model is also updated for every example—\( N \) times per epoch. While identical from a computational perspective, the two algorithms are significantly different in terms of convergence. It is a well-known fact that incremental SGD has a convergence rate as much as \( N \) times faster than batch SGD for large \( N \), when far from the minimum \[3\]. However, when close to the minimum, incremental SGD requires diminishing step sizes in order to converge. This translates into an additional hyper-parameter, i.e., the learning rate.

Algorithm 2 Batch SGD Optimization Epoch
1. Compute gradient:
   \[ \text{for } i = 1 \text{ to } N \text{ do } \tilde{g} \leftarrow \tilde{g} + \nabla \tilde{f}(\tilde{w}, \tilde{x}_i, \tilde{y}_i) \]
2. Update model:
   \[ \tilde{w} \leftarrow \tilde{w} - \alpha \tilde{g} \]

Algorithm 3 Incremental SGD Optimization Epoch
1. \( \text{for } i = 1 \text{ to } N \text{ do } \)
2. Compute gradient estimate:
   \[ \hat{g} \leftarrow \nabla \hat{f} (\hat{w}, \hat{x}_i, \hat{y}_i) \]
3. Update model:
   \[ \hat{w} \leftarrow \hat{w} - \alpha \hat{g} \]
4. \( \text{end for} \)

2.2 Synchronous Parallel SGD

Parallelizing SGD seems rather impossible because of a chain dependency on model updates across epochs (batch) and even inside an epoch (incremental), where the current gradient relies on the previous model. As a result, in order to preserve the theoretical soundness of the algorithm, concurrency is limited to within each stage—gradient computation and model update, respectively—while synchronization has to be strictly enforced between them. Of the two stages, gradient computation entails significantly more work and is, thus, the main candidate for parallelization. This is achieved by expressing the gradient as a linear algebra formula over the training data and the model. As a concrete example, we give the linear algebra expression for the LR gradient:

\[ \tilde{g} = X_k^T \odot \left( \begin{array}{c} -Y_k \cdot e^{-Y_k \cdot w} \\ \frac{e^{-Y_k \cdot X_k \odot w}}{1 + e^{-Y_k \cdot X_k \odot w}} \end{array} \right) \] (2)

The algebraic operators involving vectors and matrices are element-wise when written in standard notation and have the linear algebra meaning, otherwise. For example, \( \cdot \) corresponds to element-wise vector multiplication, while \( \odot \) stands for vector dot-product or matrix-vector multiplication. This expression replaces the loop corresponding to gradient computation in Batch SGD Optimization Epoch. Efficient parallel implementations from highly-optimized linear algebra libraries are then used to speed-up the computation.

2.3 Asynchronous Parallel SGD

In asynchronous parallel SGD, multiple model updates are executed concurrently—without synchronization primitives, e.g., mutexes or locks. Moreover, access to the model in gradient computation can also interfere with the update—or a stale model is used. Hogwild \[25, 12, 32, 38, 30\] is the most representative algorithm in this category. It is the exact Incremental SGD Optimization Epoch with the loop executed in parallel:

\[ \text{for } i = 1 \text{ to } N \text{ do in parallel} \]

This makes the parallel implementation of Hogwild very simple—a single directive has to be added in OpenMP\[http://www.openmp.org/\]. Although not satisfying the specification of SGD, it has been theoretically proven that the resulting non-determinism in Hogwild enhances randomness and guarantees convergence for sparse models \[25\]. However, due to parallelism, the overall time to convergence can be orders of magnitude faster than the sequential solution. The approach taken in synchronous SGD is more conservative—preserve the convergence of batch SGD exactly. “Which of the two alternatives is better?” is an open question that extends upon the debate between batch and incremental SGD—synchronous corresponds to batch, while asynchronous to incremental.
3 COMPUTING ARCHITECTURES

We present the two computing architectures considered in this work—multi-core NUMA CPU and GPU.

NUMA CPU. The architecture of a NUMA machine is depicted in Figure 3. It consists of several nodes which contain multiple cores and processor caches. The L1 and L2 caches are associated with each core, while the L3 cache is shared across all the cores in a node. Each node is directly connected to a region of the DRAM memory. NUMA nodes are connected to each other by high-bandwidth interconnects on the main board. To access DRAM regions of other nodes, data is transferred over these interconnects. However, this is slower than accessing the locally-associated memory. Cache-coherency is implicit on NUMA machines and is implemented in hardware. In the worst case, the coherency protocol requires transfer across nodes which can generate congestion on the interconnect and, thus, significantly reduce the speedup of parallel solutions.

![Figure 3: NUMA CPU architecture.](image)

GPU. As illustrated in Figure 4, a GPU contains multiple streaming multiprocessors (MP). Each MP consists of a large number of specialized cores targeted at a limited subset of instructions. In the CUDA programming model, work is issued to the GPU in the form of a function, referred to as the kernel. A logical instance of the kernel is called a thread. The kernel code is parametrized by a logical thread identifier that allows each thread to operate on a different partition of the input data. Since thousands of threads can be executed concurrently across MP, global thread synchronization is not available. Nonetheless, synchronization can be enforced at thread block level. A thread block (or block) is a logical group of the threads executed for a kernel and imposes an upper limit on the number of threads, e.g., at most 1024 threads can be part of a block. The programmer has to specify both the number of blocks and the number of threads in a block when launching a kernel. Physically, all the threads in a block must reside on the same MP, as shown in Figure 4. In order to highly utilize the GPU parallelism, the number of blocks has to be at least equal to the number of MP. To manage thousands of concurrent threads running on different parts of the data, the MP employs SIMT (single-instruction, multiple-thread) or SIMD (single-instruction, multiple-data) parallelism by grouping consecutive threads of a block into a warp. The MP issues instructions at warp level in vector-like fashion for all the threads in the warp at a time. The number of threads in a block should be a multiple of the warp size in order to achieve full warp utilization. Moreover, in order to fully utilize all the cores, there should be a sufficiently large number of warps that contain sufficiently long sequences of independent instructions.

Threads can access the various units of the deep memory hierarchy in Figure 4 explicitly—in the code—during execution. This is quite different from the CPU memory management which is completely hidden from the programmer. While more flexible, it also makes GPU programming harder. Global memory (or device RAM memory) is persistent over multiple kernel invocations and can be accessed from all the threads across MP. While the largest in size, global memory has the highest latency and lowest bandwidth. Shared memory is a low-latency high-bandwidth memory available to all the threads within a thread block. It is the only mechanism that allows synchronization between threads—only within a thread block, though. The read-only constant texture memory (or scratchpad memory) is a read-only cache populated from global memory. It is accessible by all the threads on an MP. Placement on the shared and scratchpad memory has to be implemented explicitly by the programmer. The two levels of cache L1 and L2 are used to improve the latency to the global memory. L1 cache handles only local thread memory and does
not cache global memory loads. As a result, there is no cache coherency implemented across MPs. When a global memory address is requested by a thread of a warp, aligned successive addresses are converted into a single memory transaction which is called memory coalescing. To move data efficiently from global memory, the threads in a warp have to access consecutive global memory addresses. If the requested addresses of the warp are sparse or unaligned, several memory transactions are required to support the warp computations. Until all the requested data are cached in L2, the warp cannot be scheduled for computation.

Table 1 gives the hardware specifications of the NUMA machine and the NVIDIA Tesla K80 GPU used in this paper. While the number of cores and threads is much larger for the GPU, the numbers for the NUMA machine are quite high compared to previous CPU generations, e.g., 56 independent threads can run concurrently on a single machine. Although the amount of memory available on the CPU is 20X larger than on the GPU, the L2 cache on the GPU is 6X larger. This reflects the throughput emphasis of the GPU memory hierarchy as opposed to the latency optimization for CPU.

|                | NUMA       | GPU       |
|----------------|------------|-----------|
| CPU/MP         | 2          | 13        |
| cores          | 14 per CPU | 192 per MP|
| blocks         | -          | 16 per MP |
| threads        | 28 per CPU | 2048 per MP|
| L1 cache       | 32+32 KB   | 48 KB     |
| L2 cache       | 256 KB     | 1.5 MB    |
| L3/shared      | 35 MB      | 48 KB     |
| RAM/global     | 256 GB     | 12 GB     |

Table 1: Hardware specification.

4 SYNCHRONOUS SGD IMPLEMENTATION

The implementation of synchronous SGD consists of a sequence of primitive linear algebra function invocations for gradient computation and model update. In the case of the LR gradient (Eq. 2), the function sequence is:

\[
\begin{align*}
\text{vector } a & = \text{matrix-vector-product(data, model)} \\
\text{a} & = \text{vector-vector-element-product(label, a)} \\
\text{a} & = \text{vector-element-exponent(a)} \\
\text{vector } b & = \text{vector-element-sum(1, a)} \\
\text{a} & = \text{vector-vector-element-division(a, b)} \\
\text{a} & = \text{vector-vector-element-product(a, -label)} \\
\text{gradient} & = \text{matrix-vector-product(transpose(data), a)}
\end{align*}
\]

Each of these functions is blocking, i.e., the next function in the sequence is invoked only after the previous finishes execution. This introduces a clear boundary between gradient computation and model update, essentially synchronizing access to the model. Parallelism is confined exclusively to intra-function processing. This allows for a variety of implementations, as long as the function API is preserved. ML frameworks, e.g., TensorFlow and BIDMach, capitalize on this abstraction and implement the linear algebra primitives for a unified API for both CPUs and GPUs. For example, function \text{matrix-vector-product} has an implementation for multi-thread CPU and one as a GPU kernel. Moreover, separate implementations are provided for dense and sparse data because of the different set of optimizations they require—this is not the case for TensorFlow and other deep learning frameworks which support only dense matrix representations and cannot, thus, handle high-dimensional models. The benefit of this approach is that switching between architectures does not require any code modification.

Our synchronous SGD implementation follows the common API approach. We use the ViennaCL library which implements the linear algebra primitives used in LR and SVM—we extend the library with several functions. ViennaCL has support for multi-thread CPU and GPU, and for dense and sparse data. Since the ViennaCL implementations use all the specific architectural optimizations and are among the fastest available, we do not have to apply further intra-primitive optimizations. For a specific configuration, e.g., CPU or GPU, all the primitives are executed on that device—no cross-device execution. We do not apply cross-primitive optimizations such as pipelining, fusion, and on-GPU intermediate result caching because this requires a holistic view of the program.

The benefit of highly-optimized linear algebra primitives is reflected in the hardware efficiency of parallel synchronous SGD. Figure 5 and 6 show that up to two orders of magnitude reduction is achieved over the sequential SGD.
for LR both by a multi-thread CPU and a GPU solution. These results also confirm that choosing the optimal kernel is highly-dependent on the data characteristics and the model. For dense data (Figure 5), the GPU kernel and parallel CPU are indistinguishable, while for sparse data (Figure 6), the GPU is faster by an order of magnitude. The complete details of the datasets and the models are given in Section 6. Since the exact semantics of sequential SGD is preserved, the statistical efficiency is the same for multi-thread CPU and GPU (Figure 5 and 6). This property is important because the convergence analysis for sequential SGD can be immediately extended to the parallel synchronous SGD. Moreover, the time to convergence is determined entirely by the hardware efficiency. Figure 5 and 6 confirm this linear dependency—the time to convergence is the number of epochs multiplied with the time of an epoch. As a result, GPU has faster convergence for sparse data, while on dense data, CPU and GPU are almost the same. Deciding the architecture on which to execute parallel synchronous SGD is not a straightforward decision, even though these results suggest that GPU is better. The convergence time is conditioned by the size and sparsity of the data, and the model. There is no simple rule on how to undoubtedly choose between CPU and GPU in ViennaCL—the same conclusion is supported by experiments with TensorFlow and BIDMach.

5 ASYNCHRONOUS SGD IMPLEMENTATION

Compared to the non-intrusive synchronous approach which composes a series of architecture-optimized linear algebra functions, the asynchronous solution consists of a single function that implements the Incremental SGD Optimization Epoch. For each training example, this function first computes the gradient and immediately applies it to a model update. Parallelism is achieved by executing several instances of the function, i.e., threads, concurrently over partitions of the examples. Asynchronous execution is the result of unprotected access to the shared state, i.e., the model, across concurrent threads. This approach to incremental SGD—the Hogwild algorithm \cite{25}—prioritizes hardware over statistical efficiency and better time to convergence is often obtained. However, a naive implementation is not sufficient \cite{32}. Rather, architectural optimizations of the hardware have to be carefully considered.
5.1 Hogwild on NUMA CPU

In DimmWitted [39], Zhang and Re give a Hogwild implementation optimized for NUMA CPU architectures. They investigate the impact of three factors – access method, model replication, and data replication – on the efficiency of Hogwild. For each factor, multiple alternatives are independently evaluated in terms of statistical and hardware efficiency and the optimal configuration is selected for every dataset/model combination—while the goal of DimmWitted is to do this automatically with a cost-based optimizer, unfortunately, it is not possible. Given the exhaustive nature of the DimmWitted study, our asynchronous SGD NUMA CPU implementation follows their solution. According to Figure 14 in [39], fully-replicated row-wise data access to a model replicated at NUMA node granularity is the optimal configuration for LR and SVM tasks. In our experimental setting, this corresponds to having two copies of the data and the model—one for each NUMA node. Essentially, we execute two independent Hogwild instances—one for each NUMA node. Due to the non-deterministic assignment of examples to threads and the model update order, these two instance are not identical copies—they provide non-redundant statistical information which improves the statistical efficiency. A second layer asynchronous Hogwild is executed between the NUMA node models in order to reduce their divergence. Periodically, a separate thread reads these two models, merges them, and updates each replica. Since all the threads scheduled on a NUMA node access only the corresponding model replica, no cache coherence overhead is incurred. This is reflected in higher hardware efficiency. For the remainder of the paper, all the references to asynchronous SGD on NUMA CPU correspond to this implementation.

5.2 Hogwild on GPU

In this paper, we provide the first in-depth study of Hogwild on GPU. While several GPU extensions to asynchronous SGD have been proposed in the literature [26, 19, 37], they either target a single application, e.g., low-rank matrix factorization, or restrict themselves to a specific data/model configuration, e.g., sparse round-robin partitioned data with a single shared model. Moreover, none of these solutions is completely asynchronous in a Hogwild sense. We take an exhaustive approach in which we organize the Hogwild design space into three dimensions and consider several strategies for each dimension. Given a training dataset, a model specification, and a GPU configuration of threads and blocks, our goal is to determine an execution plan for the asynchronous Hogwild. The execution plan has to specify the assignment of data and model to GPU threads and the access path to the assigned data and model—inside the thread. Table 2 summarizes the components of the execution plan – the dimensions of the design space – and their corresponding strategies.

Although derived from the NUMA CPU factors proposed in DimmWitted [39], the GPU optimizations are quite different because of the layered parallelism consisting of blocks and threads, the SIMD execution within a warp, and the distinct memory hierarchy optimized for throughput rather than latency. While our initial goal has been to build an analytical model that identifies the optimal execution plan for any data/model configuration automatically, we have found experimentally that this choice is highly-dependent on data and model characteristics. Thus, we limit ourselves to providing practical rules of thumb to guide the optimal choice.

5.2.1 Data Access Path

The training examples $\mathbf{x}_i$ form a 2-D matrix which can be organized in memory in row-major (row) – by example – or column-major (col) – by feature – format. These are extended to sparse data by the corresponding Compressed

| Dimension         | Strategies                            |
|-------------------|---------------------------------------|
| Data access path  | row-major round-robin (row-rr)        |
|                   | row-major chunking (row-ch)           |
|                   | column-major round-robin (col-rr)     |
|                   | column-major chunking (col-ch)        |
| Model replication | kernel                                 |
|                   | block                                  |
|                   | thread                                 |
|                   | example                                |
| Data replication  | no replication (no-rep)                |
|                   | k-wise replication (rep-2, rep-5, rep-10) |

Table 2: Design space for Hogwild on GPU.

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Sparse Row (CSR) and Compressed Sparse Column (CSC) format which store only the non-zero entries using three 1-D arrays. There are two arrays for the non-zero values and their column (or row) index – each of size the number of non-zero entries – and a third array with size the number of rows (or columns) that stores the index in the first two arrays where each column (or row) starts. The assignment of examples to threads – data partitioning – is a second factor that has to be carefully considered when accessing the training data. The two standard approaches that do not require preprocessing and dynamic scheduling are round-robin (rr) and chunking (ch)—horizontal partitioning. The combination of data format and partitioning results in four configurations—row-rr, row-ch, col-rr, and col-ch. Existing NUMA CPU implementations consider only row-ch since asynchronous SGD accesses a complete example to compute the gradient and chunking allows for exclusive access to the local memory. SIMD execution coupled with memory access coalescing inside a thread block/warp pose new challenges for GPU. If the number of examples assigned to the threads of a block is not identical, the threads having fewer examples are stalled until the others finish. For dense data, all the threads in a block access the same model feature simultaneously which results in non-coalescing. This also happens for sparse data, however, the reason is the random access pattern to the model features. In both cases, the number of memory transactions necessary to execute a SIMD instruction is a bottleneck for the NUMA CPU row-ch configuration. Thus, investigating the other alternatives is essential.

Figure 7 depicts a graphical representation of the four data access path configurations considered for the execution on GPU: row-rr, row-ch, col-rr, and col-ch. The dashed lines link the features accessed from the dataset and updated in the model. In the dense dataset, the hatched cells indicate the optimization method we apply to reduce the data conflicts on the model updates. The hatched cells in the sparse dataset are the padded zero features used to convert the sparse dataset into a dense representation.

**row-rr.** The training examples are stored in succession and they are accessed by consecutive threads in a block/warp. For dense data, the threads of a warp read the same feature from their example when computing the gradient and modify exactly the same feature of the shared model for every update. Therefore, only a single thread successfully updates the shared model which impacts statistical efficiency negatively. Moreover, the access pattern to examples and the model is not coalesced—consecutive threads do not access consecutive memory addresses. To reduce conflicts to the shared model, each thread starts the model update process from a different index, as shown by the hatched cells in Figure 7. The starting index is assigned circularly based on the thread id. As a result, when the model size is at least half of the warp size, no update conflicts exist. This optimization also provides coalesced access to the model, thus reducing the number of memory transactions. For sparse data, the number of features across examples varies and the feature indexes are discontinuous. When threads request the features at the same position, their index is likely different, leading to independent updates.

![Figure 7: Data access path configurations on GPU.](image-url)
In addition to the model, every thread has a local gradient which is stored by default in the local memory. Since local memory is mapped to L1 cache, each feature occupies a 128-byte cache line. A thread has to fetch aligned data – including nearby unrequested features – which wastes most of the space in a cache line for loading a single feature. The warp also jumps to non-coalesced addresses multiple times to combine the separate requested features. With half-a-warp, i.e., 16 threads, every feature requests 16 cache lines which are 2048 bytes. We consider the alternative of storing the gradients in the global memory. In this case, a feature occupies a 32-byte segment in L2 cache; then 16 features request 16 cache segments which take only 512 bytes. While each feature still caches nearby unrequested indexes, the size of memory transactions to global memory is 4 times lower than to local memory. This reduction improves hardware efficiency.

**row-ch.** The training examples are stored consecutively and a thread also processes consecutive examples (Figure 7). Examples that are chunk size apart are processed concurrently by threads in a warp. Since these are minor differences compared to row-rr, the same optimizations apply. Nonetheless, depending on the chunk size and the number of threads, the performance can be quite different (Figure 9).

**col-rr.** To implement the column-major representation, we transpose the training examples. This coalesces features across examples in global memory (Figure 7) and the data accessed by a warp covers full segments. On average, each feature takes only a quarter of a memory transaction to be cached. In order to avoid update conflicts, threads access the model in circular order—similar to row-rr. The CSR sparse format is, however, not adequate for column-major access because we have to traverse the 1-D array which records the row indices of non-zero features to locate all the features of an example. Therefore, we map sparse data into a dense padded format that stores all the examples at the same width—equal to the maximum number of non-zero features. When the threads of a warp request features from the same position, accesses are coalesced. Moreover, the shared model is updated without conflict.

**col-ch.** As in the case of row-major, the main difference between col-ch and col-rr is the width between examples processed concurrently in a warp. This impacts the number of memory transactions directly. When the chunk size is small – due to a large number of threads – the average memory transaction can be much smaller than 1 since features share a cache segment. For sparse data, the number of features is the other crucial factor impacting memory transactions. If the number of features differs greatly across the threads in a warp, the average number of memory transactions is closer to the maximum of 1.

![Figure 8: Access path selection for dense data (covtype).](image)

**Hardware efficiency.** Figure 8 and 9 depict the performance of the data access strategies for LR. For dense data, col-rr exhibits the highest hardware efficiency, taking minimum average time per iteration. Since the gradient is stored in the global memory, the number of memory transactions is mostly determined by the number of L2 cache segments accessed. col-rr takes full advantage of cache access coalescing. For sparse data, row-rr is slightly better than col-rr due to extra access to padded zero features. Moreover, the non-zero features at the same position in the CSR format are more likely to be in the same cache segment. Although round-robin access tends to perform better than chunking, this cannot be generalized since row-ch has better hardware efficiency than row-rr on dense data.

**Statistical efficiency.** The strategy with the highest hardware efficiency has the lowest statistical efficiency in Figure 8 and 9. We find that the behavior of cache coalescing has a negative effect on model update conflicts. When data requests are coalesced, the warps are not frequently stalled for memory transactions. We can have at most 52
concurrent warps – 1664 threads in total – scheduled by the warp schedulers for computation. Such a large number of threads updating the model concurrently increases the conflicts to the single shared model. As a result, fewer updates survive which results in reduced statistical efficiency and more iterations to converge.

**Figure 9:** Access path selection for sparse data (news).

**Time to convergence.** Unlike synchronous SGD, both hardware and statistical efficiency have to be considered for analyzing time to convergence. As shown in the figures, these are inversely correlated which makes reasoning more difficult. On dense data, the reduction in time per iteration obtained by col-rr is sufficient to outperform the larger number of iterations and result in faster time to convergence. On sparse data, however, the excessive number of model update conflicts introduced by higher hardware efficiency prohibits optimal convergence. The round-robin strategies – although converging faster to 2% error – cannot converge to 1% error. Overall, the rule of thumb is col-rr data access with circular model updates is the optimal strategy—with the caveat that optimal convergence on sparse data is harder to achieve.

### 5.2.2 Model Replication

As the shared model is accessed by multiple threads simultaneously, this can lead to degradation in statistical efficiency. In the case of GPU, this problem is triggered by the SIMD execution inside a warp – the threads in a warp read/write the model exactly at the same time – not by a cache coherency mechanism. Among all the threads in a warp which update the model simultaneously, only a single value is arbitrarily picked for each feature, while the other updates are discarded. Moreover, a warp may execute with a stale model – due to stalling and rescheduling caused by cache misses – since other warps keep modifying the model in the shared L2 cache. Given the inefficiencies incurred by a shared model per kernel, we consider several alternatives that reduce sharing by exploiting the deep GPU memory hierarchy.

Figure 10 shows the memory layout of the model replication configurations on GPU: kernel, block, thread, and example. In our design, the examples of the dataset are transferred into the GPU global memory while the model replicas are stored in different levels of the memory. We allocate space in DRAM for kernel, thread, and example and compare the difference between the performance of the allocations from global and local memory. As we analyze for gradient storage in Section 5.2.1, although the data in local memory are cached to on-chip L1 with 128-byte lines, most of the non-coalesced data are not requested for computation. The kernel strategy has a single model shared by all the threads on the multiprocessors. In the thread strategy, the sizes of the model replicas are not identical since we materialize only the features accessed by every thread. While the example strategy maintains the model replicas with the same features for every example, the size of the model replicas are also different. The model replicas of the block strategy are stored in shared memory. If the model size is larger than the size of shared memory per thread-block, the model replicas are spilled to global memory.

**block.** There is a model replica for each block which is initialized before each iteration and merged into the global model at the end of the iteration—CUDA supports block-level synchronization. If the model is small enough, it is allocated in the shared memory—sliced into a number of 64-bit wide banks. Bank conflicts are avoided since each feature is accessed independently by a thread. Otherwise, threads incurring a bank conflict have to execute serially. Moreover, if a warp accesses the same feature while updating and copying the model replica, conflicts can be avoided.

| Hardware efficiency | Statistical efficiency | Time to convergence |
|---------------------|------------------------|---------------------|
| row-rr              | row-ch                 | col-rr              |
| 0.00                | 0.04                   | 0.08                |
| 0.12                | 0.16                   | avg time per iter [sec] |
| 1%                  | 2%                     | 5%                  |
| 10%                 | 20%                    | # iterations to 2% error |
| 0                   | 50                     | 100                 |
| 150                 |                         |                     |
| time [sec]          |                         |                     |
| 0                   | 5                      | 10                  |
| 20                  |                         |                     |

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altogether because of broadcasting of features in the same bank. Large models are replicated in the global memory—one per block. Initializing and merging model replicas incur additional overhead.

**thread.** There is a model replica which resides in local memory for each thread. For small models, this is mapped into the registers and provides fast access. Otherwise, it is mapped into the global memory. There are no model update conflicts since each thread has its own replica. Nonetheless, merging the replicas incurs significant overhead due to the large number of models.

**example.** To avoid merging sparse models in CSR format, we introduce example replication in which every example has its own model replica in global memory. An example replica contains the same features as the example. After a thread finishes processing the assigned examples, it copies the model replicas to the shared model. Example replication avoids conflicts between threads almost entirely at the expense of memory usage.

![Model replication configurations on GPU.](image)

**Hardware efficiency.** Figure 11 and 12 plot the results with the col-rr access path for dense data—example replication applies only to sparse data. On dense data, block replication has the highest hardware efficiency because access to shared memory is faster than to global memory. thread has higher hardware efficiency than kernel, even though it incurs overhead to merge the local model. The reason is that the local models are cached in L1 which resides on MP, while in kernel the model is cached in L2 which resides off-chip. On sparse data, all the strategies utilize global memory to maintain the local and global models. kernel replication has the highest hardware efficiency, while block has the lowest—by a factor of 10. The synchronization required in block replication delays the threads with fewer non-zero features until the largest example is processed. example replication has no synchronization and caches models in L1, rather than L2—the case for thread and kernel.

![Model replication effect on dense data (covtype).](image)
**Statistical efficiency.** Kernel replication displays the highest statistical efficiency both for dense and sparse data. Thread replication is two orders of magnitude lower. Intuitively, the more replicas, the lower the statistical efficiency. Model replicas – whether stored on-chip or off-chip – record only partial information. When update conflicts occur, features in the model replicas are discarded which leads to the shared model fetching limited information. In addition, the dot-product computed with the local replica generates an unreliable gradient—especially for sparse data.

![Figure 12](image-url) Model replication effect on sparse data (news).

**Time to convergence.** On dense data, kernel and block have similar time to convergence, while thread is completely outperformed because of its low statistical efficiency. On sparse data, kernel converges the fastest—by two orders of magnitude. Block fails to converge to 1% error in an acceptable amount of time. Although in this case example is second, for different access path configurations, example outperforms kernel in time to convergence. Overall, the rule of thumb is to choose kernel model replication. However, if the model fits in the shared memory, block replication may be a better choice.

### 5.2.3 Data Replication

Standard data partitioning does not replicate examples across threads because generating the correct query result requires adequate post-processing which increases execution time. We adopt this no replication (no-rep) strategy in the data access path methods. Model training, however, is approximate and using more data has the potential to improve statistical efficiency. In order to explore this tradeoff between hardware and statistical efficiency, we investigate k-wise replication in which the example partitions assigned to threads overlap at the boundaries. For example, 2-wise replication (rep-2) assigns two additional examples to every thread. The reason behind replication at the boundary is to preserve coalesced memory access. k-wise replication interacts minimally with model replication. The only difference is that the number of examples assigned to a thread is larger by k.

![Figure 13](image-url) Data replication configurations on GPU.

Figure 13 plots the data replication configurations with two horizontal partitioning strategies: no replication (no-rep) and k-wise replication (rep-2). Without replication, the examples are sliced by the round-robin access path where threads take turn to process the examples one by one. With the chunking access path, the fixed-size chunks are...
assigned to the threads sequentially. In the k-wise replication strategy, the thread fetches several examples after the originally-assigned ones with no-rep, as Figure 13 shows. Therefore, the examples are accessed several times by different threads.

Figure 14: Data replication effect on dense data (covtype).

Figure 15: Data replication effect on sparse data (news).

Figure 14 and 15 depict the impact of k-wise replication on hardware and statistical efficiency for k equal to 2, 5, and 10, respectively. The trend is identical both on dense and sparse data. The larger k is, **hardware efficiency** drops almost linearly. This is somewhat unexpected because we expect coalesced memory access to be more resilient when the range increases only slightly. The configurations used in the figures are *col-rr+kernel* (dense) and *col-rr+example* (sparse). We observe similar trends for the other combinations. **Statistical efficiency** increases linearly with k since more information is extracted from the data for gradient computation and model update. When these opposing measures get combined in **time to convergence**, the reduction in number of iterations dominates the increase in time per iteration and we obtain faster convergence when the degree of replication is higher. The improvement diminishes beyond rep-10. Overall, the rule of thumb is to adopt a limited degree of data replication because it enhances statistical convergence linearly while also decreasing time to convergence by a significant margin.

6 EXPERIMENTAL EVALUATION

We perform an extended empirical study across the exploratory axes defined in Figure 1 with respect to the performance axes introduced in Figure 2. The goal is to fully characterize the relationship between the considered configurations and understand the relevance of each performance measure. We validate our results by comparing against two representative analytics frameworks that have support both for CPU and GPU—TensorFlow and BIDMach. We emphasize that the main objective of the comparison is to add other reference points on the performance axes beyond our implementation, while the direct comparison between frameworks is secondary. Specifically, our experiments target the following questions:
What is role of the computing architecture, i.e., CPU/GPU, on the performance of synchronous SGD?
What is role of the computing architecture, i.e., CPU/GPU, on the performance of asynchronous SGD?
What is the optimal configuration for asynchronous SGD on GPU?
How do synchronous and asynchronous SGD compare against each other on CPU and GPU separately, and across computing platforms?
Are our implementations efficient with respect to Tensorflow and BIDMach?
How do the proposed algorithms scale with the number of training examples and the dimensionality of the feature vector, respectively?

6.1 Setup

Implementation. We implement all the 8 configurations in Figure 1 following the best practices for Intel multi-core CPUs and for NVIDIA GPUs, respectively. We use OpenMP for multi-thread programming on the CPU and CUDA 8.0 on the GPU. Synchronous SGD is implemented using the ViennaCL (1.7.1) linear algebra library which provides optimized primitives with the same API for CPU and GPU. This allows us to have identical implementations—only compiled with different flags. We have separate implementations for dense and sparse data that use optimized data structures. All the code is written in C++. For the implementations in TensorFlow (0.12.0) and BIDMach (2.0.1), we write only the driver programs which define the objective function corresponding to the analytic model. We then invoke the synchronous SGD optimizer which calls the linear algebra kernels necessary in the gradient computation. While the driver is written in python for TensorFlow and scala for BIDMach, the linear algebra kernels are coded in C++/CUDA and are highly-optimized.

| dataset | #examples | #features | nnz/example (avg) | sparse size | dense size |
|---------|-----------|-----------|------------------|-------------|------------|
| covtype | 581,012   | 54        | 54 (54)          | 485 MB      | 485 MB     |
| w8a     | 64,700    | 300       | 1 to 114 (11.65)| 4.4 MB      | 155 MB     |
| real-sim| 72,309    | 20,958    | 1 to 3,484 (51.30)| 87 MB      | 12.1 GB    |
| rcv1    | 677,399   | 47,236    | 4 to 1,224 (73.16)| 1.2 GB     | 256 GB     |
| news    | 19,996    | 1,355,191 | 1 to 16,423 (454.99)| 134 MB    | 217 GB     |

Table 3: Experimental datasets. nnz is number of non-zero.

System. The properties of the computing architectures used in the experiments are presented in Figure 1. They are mounted in the same physical machine running Ubuntu 16.04 SMP with Linux kernel 4.4.0-77 and CUDA 8.0. Out of the two cards inside the Tesla K80 GPU, only one is used in the experiments. The two cards are seen as two independent GPUs by the operating system and have to be programmed independently. This is the default setting in both TensorFlow and BIDMach which require the programmer to specify the GPU on which the SGD optimizer executes. We plan to perform an evaluation with multiple – possibly distributed – GPUs in the future.

Methodology. We perform all the experiments at least 3 times and report the average value as the result. Each task is run for at least 10 iterations and the hardware efficiency is measured as the average execution time over the total number of iterations. The time to evaluate the loss is not included in the iteration time. All configurations/systems are initialized with the same model which gives the same initial loss. The SGD step size is chosen by gridding its range in powers of 10, e.g., \(10^{-6}, 10^{-5}, \ldots, 10^2\), and selecting the value that generates the fastest time to convergence. The optimal step size varies across configurations. For end-to-end performance, we measure the wall-clock time it takes for each configuration to converge to a loss that is within 10\%, 5\%, 2\%, and 1\% of the optimal loss. Following prior work [39], we obtain the optimal loss by running all configurations for one hour and choosing the lowest. The time to load the data and output the result is not included. Moreover, in the case of GPU, the time to transfer the data and the model to/from the GPU global memory is also not included—we measure only the kernel execution time. For Hogwild on GPU, we report only the result corresponding to the configuration that achieves 1% convergence error the earliest. As discussed in the results, this configuration is different across datasets.

Datasets and tasks. Rather than considering only two datasets – dense and sparse – we include five real datasets (Table 3) that exhibit large variety in size, dimensionality, and sparsity. The number of dimensions varies from tens
to more than 1 million, while the number of non-zero entries per example is as small as 1 for most of the datasets. In terms of physical size, the sparse representation is as small as 4.4 MB for w8a – it can be cached (almost) completely both on CPU and GPU – and as large as 1.2 GB for rcv1. In dense format, only covtype and w8a fit on the GPU, while rcv1 and news cannot be processed even on the CPU. covtype is the representative dense dataset throughout the paper since it is complete, while news has the highest sparsity ratio of $3 \times 10^{-4}$. These datasets have been used previously to evaluate the performance of parallel SGD on NUMA CPU [39] and GPU [32]—more details can be found therein. We use a dense format for w8a in order to allow TensorFlow to execute. As a result, synchronous SGD becomes batch gradient descent since it uses the complete dataset to compute the exact gradient. Even if we reduce the batch size and have several model updates per data pass, the time to convergence does not improve. With five datasets and four points on the exploratory axes, we obtain 20 configurations per model. Since we consider two tasks – LR and SVM – we have 40 configurations overall. We do not include any regularization in the objective function in order to measure only the time spent in the actual computation.

### 6.2 Results

We project the results on a subset of dimensions in the exploratory axes to facilitate a direct comparison between configurations. For synchronous and asynchronous updates taken separately, we compare the CPU and GPU implementations. Then we perform a direct comparison between the best synchronous and asynchronous configurations. For each computing architecture, we compare synchronous and asynchronous SGD, and the synchronous solutions in TensorFlow and BIDMach, respectively. Lastly, we study the effect of the number of examples and features on hardware efficiency for CPU and GPU separately.

| task | dataset | time to convergence (sec) | time per iteration (msec) | # iterations |
|------|---------|--------------------------|--------------------------|--------------|
|      |         | gpu | cpu-seq | cpu-par | gpu | cpu-seq | cpu-par |              |
| LR   | covtype | 1.05| 145.11  | 1.29    | 15 | 2,073  | 18.42   | 70           |
|      | w8a     | 0.37| 148.88  | 0.46    | 4.87 | 1,959  | 6.05    | 76           |
|      | real-sim| 3.10| 1,537.90| 7.67    | 4.43 | 2,197  | 10.96   | 700          |
|      | rcv1    | 31.69| 2,227.05| 48.06   | 44.82| 3,150  | 67.98   | 707          |
|      | news    | 0.65| 240.21  | 3.68    | 6.37 | 2,355  | 36.08   | 102          |
| SVM  | covtype | 10.22| 1,344.65| 13.50   | 14.27| 1,878  | 18.85   | 716          |
|      | w8a     | 0.78| 342.85  | 0.80    | 4.13 | 1,814  | 4.23    | 189          |
|      | real-sim| 0.23| 75.59   | 0.46    | 6.22 | 2,043  | 12.43   | 37           |
|      | rcv1    | 1.13| 111.61  | 2.61    | 29.74| 2,937  | 68.69   | 38           |
|      | news    | 0.30| 98.42   | 1.69    | 6.67 | 2,187  | 37.56   | 45           |

Table 4: Synchronous SGD performance to 1% convergence error. The best values for each dataset are underlined.

#### 6.2.1 Synchronous SGD

Table 4 contains the time to convergence, and hardware and statistical efficiency results for synchronous SGD implemented with the ViennaCL library. In order to show the improvement over a sequential solution, we also include results for a single-thread CPU implementation which achieves convergence in less than 5 minutes only for 6 out of the 10 dataset/task pairs. Since the parallel implementations always achieve convergence in less than 1 minute – sometimes even in less than a second – it is clear that parallelism helps. When comparing the multi-core CPU and GPU solutions, there is a clear trend—GPU is always faster than parallel CPU in time to convergence. Since the statistical efficiency is identical in synchronous SGD independent of the computing platform, this also translates into faster GPU time per iteration, i.e., better hardware efficiency. Given that ViennaCL defines its internal representation for dense and sparse data and implements optimized kernels for CPU and GPU independently, the difference is due exclusively to the computational power of the two architectures—the GPU has more FLOPS than the CPU. The gap between the two architectures – reflected by the speedup (Table 5) – increases with the sparsity of the data. The GPU
is faster by a small margin – 32% or less – on the dense datasets covtype and w8a. This confirms that having powerful CPUs with tens of cores provides extensive parallelism that has the potential to close the gap on the GPU. In fact, we find that computing the transpose of a dense matrix on the GPU is a serious bottleneck in ViennaCL. When the transpose is computed in-place, the GPU performance becomes worse than the CPU—in these results, the transpose is materialized and passed as a second matrix to the kernels. The gap between GPU and CPU increases on sparse data to more than 5X on news. Parallelizing linear algebra operations on sparse data is known to be a difficult task because of the irregular memory access [36]. This turns out to be more acute for the CPU memory hierarchy. At a close inspection, we find that ViennaCL takes advantage of the programmability of the GPU memory and exploits it to optimize coalesced access to sparse data. Moreover, the linear algebra kernels invoked depend on data sparsity—a different kernel is called on news compared to real-sim and rcv1. The high variance in statistical efficiency across dataset/task combinations is due to different hyper-parameters. It confirms that convergence rate is a property of both the task and the dataset and is independent of sparsity. When comparing the time per iteration across LR and SVM, however, we observe very similar results on GPU and CPU although their gradients are quite different. The reason for this is matrix batch processing and vectorization which hide the higher latency incurred by individual element-wise operations—both LR and SVM have exactly the same number of matrix-matrix and matrix-vector operations.

Table 5 contains the speedup in time per iteration generated by parallel CPU over sequential CPU and GPU over parallel CPU, respectively. For synchronous SGD, this also represents the speedup in time to convergence. Given that parallel CPU uses 56 threads, we expect a speedup in the range of 56 over sequential CPU. This is the case for news. The speedup for rcv1 is slightly below 56—due to the large size of the dataset which does not allow for efficient caching even in L3. We obtain super-linear speedup on covtype, w8a, and real-sim—on w8a the speedup is more than 400X for SVM. The reason for this is the improved cache behavior when all the cores are in use. w8a can be entirely cached in L1 due to its small size, while real-sim and covtype are cached in L2 and L3, respectively. None of these datasets can be cached on a single core when executing the sequential code. GPU improves further over parallel CPU by a factor of 1 to 5X.

Table 5: Speedup of synchronous SGD time per iteration. cpu-seq/cpu-par measures the speedup of the parallel CPU implementation over the sequential CPU. cpu-par/gpu corresponds to the speedup of GPU over parallel CPU.

6.2.2 Asynchronous SGD

Based on the three dimensions of the design space and related strategies for Hogwild on GPU, we list the optimal configuration for all the datasets used in the experiments (Table 6). The optimal configurations are determined by the fastest time to convergence for every dataset/task pair. Although w8a is a sparse dataset, we can afford to use a dense representation because of its relatively small dimensionality. In fact, we perform experiments with both representations and choose the better one—sparse representation turns to be better for both LR and SVM.

As expected, covtype benefits from coalesced col-rr data access with circular model updates on the model replicas in the shared memory—w8a in dense format has the same configuration. Moreover, replication is not beneficial. For the sparse datasets, the row-major format is better since it does not include zero padded features. Compared to column-major format, row-major format trades-off memory transactions by thread stalls, improving hardware efficiency considerably. Assigning examples to threads at round-robin- or chunk-level is a property of the dataset and computation due to the length of memory jumps incurred and the number of accesses per example. Due to the large model size, kernel model replication is the optimal choice for sparse datasets due to the limited size of shared memory—thread model replication degenerates into kernel with additional overhead. k-wise data replication is almost...
always beneficial and in larger sizes. However, the difference in time to convergence compared to no replication is small. Overall, these results confirm the importance of our study in characterizing the design and prove that applying the same configuration in all scenarios is suboptimal.

Table 7 depicts the time to convergence to 1% error, and hardware and statistical efficiency for asynchronous SGD. The parallel implementation on NUMA CPU is based on DimmWitted [39] (Section 5.1). The GPU results are based on the configurations in Table 6 corresponding to each dataset/task pair.

When comparing the CPU and GPU solutions, there is a clear trend—(parallel) CPU is faster than GPU in time to convergence. Specifically, on dense and low-dimensional data, the sequential CPU solution is faster, while on sparse data, parallel CPU dominates. The reason behind this Hogwild behavior on CPU is well-known [39, 32]—concurrent updates to the same features of the model generate cache-coherency conflicts that slow down execution and convergence. Essentially, parallelism is beneficial only on sparse data and models. Since there is no cache coherency mechanism on the GPU, one may expect the GPU solution to be considerably faster due to the higher degree of parallelism.

However, the GPU bottleneck turns out to be vectorized execution inside a warp which generates a significant number of model update conflicts. While the warp shuffling optimization reduces the number of conflicts inside a warp, the number of concurrent warps is a lower bound that cannot be overcome. In the case of sparse data, however, update conflicts are not an issue. The problem is the irregular access to the model across the examples inside a warp. First, there is a high variance in the number of non-zero entries—several orders of magnitude. This forces threads to stall while longer examples finish. Second, all accessed model indexes have to be cached before a vectorized instruction can be executed. This incurs a large number of slow memory transactions per instruction. In order to address these issues, data and model partitioning techniques similar to the ones proposed for out-of-core processing [27, 30] have to devised for GPU. We plan to look into this topic in future work.

Table 6: Optimal configurations for Hogwild on GPU.

| task | dataset | time to convergence (sec) | time per iteration (msec) | # iterations |
|------|---------|--------------------------|---------------------------|--------------|
|      |         | gpu | cpu-seq | cpu-par | gpu | cpu-seq | cpu-par | gpu | cpu-seq | cpu-par |
| LR   | covtype | 1.97 | 0.60  | 1.31    | 15  | 150     | 251     | 135 | 4       | 6       |
|      | w8a     | 0.20 | 0.27  | 0.18    | 21  | 2.8     | 5.9     | 8   | (80)    | 18  27   |
|      | real-sim| 2.46 | 1.35  | 0.52    | 271 | 27      | 8.1     | 9   | (92)    | 54  61   |
|      | rcv1    | 18.29| 20.37 | 4.64    | 226 | 345     | 71      | 81  | 59      | 65      |
|      | news    | 7.35 | 5.47  | 1      | 615 | 65      | 8.7     | 12  | (∞)     | 103     |
| SVM  | covtype | 0.96 | 0.16  | 0.35    | 15  | 53      | 77      | 63  | 3       | 4       |
|      | w8a     | 6.29 | 0.54  | 1.89    | 25  | (2.6)   | 5.6     | 247 | (∞)     | 239     | 333     |
|      | real-sim| 1.04 | 1.82  | 1.28    | 136 | 14      | 7.6     | 7   | (247)   | 164     | 166     |
|      | rcv1    | 8.56 | 22.71 | 7.57    | 955 | 94      | 68      | 9   | (109)   | 105     | 111     |
|      | news    | 8.75 | 20.01 | 1.79    | 454 | 50      | 8.4     | 19  | (∞)     | 425     | 211     |

Table 7: Asynchronous SGD performance to 1% convergence error. For the GPU configurations that use replication, we also include the values without replication, e.g., 21 (2.8) time per iteration for LR on w8a corresponds to 21 msec with rep-10 and 2.8 msec with no-rep, respectively. The best values for each dataset are underlined. ∞ stands for lack of convergence in 300 seconds and an unknown number of iterations, e.g., cpu-par for LR on news does not converge to 1% error within 300 seconds, thus the number of iterations to convergence is unknown.
Several entries in Table 7 require discussion. Parallel CPU does not converge for LR on news—also the case for GPU without replication. This proves the benefits of accessing an example multiple times during an iteration despite the increase in hardware efficiency. Nonetheless, the decision is particular to each dataset/task pair separately—parallel CPU converges without replication in all the other configurations, while GPU does not for SVM on w8a and news. Sequential CPU is the fastest for SVM on w8a because of several reasons. In sparse representation, w8a is small enough to be fully cached in L3, thus, memory latency is minimal. As discussed previously, parallelism triggers the cache coherency mechanism which incurs delays. Since w8a has only 300 features, the rate of update conflicts is high. Although this behavior is also present on LR, the results are different. This has to do with the much simpler form of the SVM gradient which can be evaluated with a simple bit flip operation—the label is +1 or -1. The LR gradient requires exponentiation which is considerably more expensive. GPU is the fastest for SVM on real-sim—the only case for asynchronous SGD across all our experiments. The reason is the very small number of iterations to convergence which are executed relatively fast. This is the perfect example for data replication. Nonetheless, the gap to CPU execution is minimal. The number of iterations sequential CPU requires to convergence for SVM on news is much larger than parallel CPU, e.g., 425 compared to 211. This is contrary to all the other results and unexpected. We found that sequential CPU gets stuck on a plateau for 220 iterations before the loss starts to decrease again. This is due to a too large step size that does not decrease fast enough. All our tries to find a better step size have failed—this is the best time to convergence we managed to achieve.

We report the time per iteration, i.e., hardware efficiency, and the number of iterations to convergence, i.e., statistical efficiency, for GPU with and without replication. This clearly shows the impact of replication—higher time per iteration and smaller number of iterations to convergence. While the ratio of the values follows closely the replication factor, the time to convergence is entirely determined by the actual value. Nonetheless, the times to convergence with and without replication are very close.

In general, the best time per iteration follows closely the optimal time to convergence. Parallel CPU is the fastest on sparse data for the same reasons mentioned previously. With the exception of SVM on w8a, GPU has the fastest time per iteration on dense data. This proves that with the optimal data layout—the superior FLOPS on the GPU lead to better performance. Identifying the optimal layout, however, requires the in-depth analysis performed in this work. The higher computational complexity of LR is reflected in the higher time per iteration across all the configurations. Table 8 summarizes the speedup in time per iteration corresponding to these values. In the best case, parallel CPU achieves a speedup of 6X over sequential CPU on news which is consistent with results published in the literature [32, 38]. The best speedup of GPU over parallel CPU is at most 5X on covtype.

| task | dataset | cpu-seq/cpu-par | cpu-par/gpu |
|------|---------|-----------------|-------------|
| LR   | covtype | 0.60            | 5.80        |
|      | w8a     | 2.54            | 2.11        |
|      | real-sim| 3.09            | 0.30        |
|      | rcv1    | 4.86            | 0.31        |
|      | news    | 6.09            | 0.13        |
| SVM  | covtype | 0.69            | 5.13        |
|      | w8a     | 0.39            | 2.15        |
|      | real-sim| 1.45            | 0.54        |
|      | rcv1    | 3.18            | 0.72        |
|      | news    | 5.60            | 0.17        |

Table 8: Speedup of asynchronous SGD time per iteration. cpu-seq/cpu-par measures the speedup of the parallel CPU implementation over the sequential CPU. cpu-par/gpu corresponds to the speedup of GPU over parallel CPU.

The reason it does not translate into better time to convergence is the much larger number of iterations—a factor of 15 or more. As expected, sequential CPU achieves convergence in the smallest number of iterations without data replication because it avoids update conflicts altogether. Intuitively, k-wise replication is equivalent to executing k passes over the data in a single iteration, i.e., k iterations. Asynchronous parallel processing always introduces additional iterations—correlated to the degree of parallelism.

6.2.3 CPU vs. GPU

We group all the results—hardware efficiency, statistical efficiency, and time to convergence—across all the datasets in Figure 16 for LR and Figure 19 for SVM, respectively. We also include in the figures the synchronous SGD implemented in TensorFlow (tf) and BIDMach (bid)—on parallel CPU and GPU. Since TensorFlow supports
only dense data, we have results only for \textit{covtype} and \textit{w8a}. The stacked bars for asynchronous SGD on GPU correspond to the configurations with and without replication—hardware efficiency is smaller without replication, while statistical efficiency is smaller with replication. The side-by-side depiction of the results allows for immediate comparison between CPU and GPU across four different implementations. It also allows us to compare our ViennaCL synchronous SGD with the ones implemented in TensorFlow and BIDMach.

![Figure 16: LR hardware efficiency comparison.](image)

![Figure 17: LR statistical efficiency comparison.](image)

![Figure 18: LR time to convergence comparison.](image)

For our parallel implementations – synch and asynch – the hardware efficiency results in Figures 16 and 19 are another representation of the time per iteration results from Table 4 and 7. As discussed previously, our synchronous GPU always outperforms synchronous CPU because of the higher degree of parallelism. We observe the same pattern for synchronous SGD in BIDMach—maybe with a smaller gap on sparse data. The TensorFlow results, while limited to dense data, are somehow different. Parallel CPU is almost identical and even better than GPU—on \textit{covtype}. We found matrix transpose computation to be the bottleneck on the GPU—the same problem as in ViennaCL. The hardware efficiency of asynchronous SGD is more sensitive to the task and dataset. Nonetheless, the trend in these figures suggests that GPU is better on dense data, while parallel CPU is better for sparse data. The reasons are discussed in Section 6.2.2. In terms of statistical efficiency, all the synchronous SGD implementations – including TensorFlow and BIDMach – require exactly the same number of iterations to converge to a given loss accuracy both on CPU and GPU. While the results confirm this, they also show that statistical efficiency is sensitive to the task and dataset. The statistical efficiency of asynchronous SGD on CPU is always better than on GPU – without replication – because of the reduced number of model update conflicts generated by a smaller number of threads. The gap between the two is especially high on dense data and small models.

The time to convergence for synchronous SGD is a scaled-up image of the time per iteration since the number of iterations is identical on CPU and GPU. Thus, with the exception of TensorFlow, synchronous GPU always converges faster than CPU. In addition to the matrix transpose inefficiency, the GPU kernels in TensorFlow are optimized for
dense matrices appearing in deep nets convolutions. These operations are more compute-intensive than the matrix-vector multiplications in LR and SVM. Since BIDMach is not exclusively targeted at deep learning, it optimizes these kernels better, while our implementation is focused on generalized linear models. The time to convergence for asynchronous SGD is a direct rendering of the results in Table 7. For the reasons discussed in that context, we observe that the CPU implementation always outperforms GPU, even though GPU has better hardware efficiency on dense data. However, this is not sufficient to compensate for the much higher number of iterations to converge.

6.2.4 Synchronous vs. asynchronous

Figure 16–18 and Figure 19–21 also provide a comparison between synchronous and asynchronous SGD for CPU and GPU, respectively. Since these are different algorithms initialized with different hyper-parameters, the only comparison that makes sense is in terms of hardware efficiency—the statistical efficiency and, thus, the time to convergence, are properties of the task and dataset. On the GPU, the hardware efficiency of synchronous SGD is generally better than that of asynchronous SGD. On the CPU, the hardware efficiency of synchronous SGD is better only for low-dimensional models, while for sparse high-dimensional data asynchronous is slightly better. To understand these results, we have to discuss first the two implementations. Synchronous SGD consists of a series of simple kernels – one for each linear algebra primitive – that process the complete input data. The result of each kernel is fully-materialized in memory. Essentially, synchronous SGD has a materialization execution strategy. Asynchronous SGD – on the other hand – consists of a single kernel that fuses all the gradient operations. Moreover, it also updates the model for each example, thus, executes more operations. In view of these, materialization is preferred on the GPU – as long as it does not incur memory overflow – because of simpler memory access patterns. The complete elimination of model updates – equal to the number of examples – is also an important factor. On the CPU, materialization is bounded by the size of the caches, not the complete memory—the smaller the intermediate results the better. Since none of the
datasets generates small-enough intermediates that can be cached in the upper layers of the hierarchy, a large number of cache misses that degrade performance is incurred. While operator fusion – or compilation – improves cache access, the cache coherency mechanism triggered by concurrent model updates continues to be an important deterrent for performance. On low-dimensional models, fusion cannot overcome the large number of model update conflicts per example. On sparse high-dimensional models with large intermediates, however, the number of conflicts is minor. Thus, asynchronous SGD outperforms synchronous SGD in hardware efficiency.

![Figure 22: Comparison in time to convergence between synchronous GPU and asynchronous CPU on LR.](image)

![Figure 23: Comparison in time to convergence between synchronous GPU and asynchronous CPU on SVM.](image)

We perform a direct comparison in time to convergence only between synchronous GPU and asynchronous CPU—the optimal configurations identified for each model update strategy. We measure the loss as a function of time for exactly the same hyper-parameters and the same initialization conditions. This allows us to isolate the effect of the update strategy while using the optimal computing architecture. The results are depicted in Figure 22 for LR and Figure 23 for SVM, respectively. Synchronous GPU achieves better convergence for certain dataset/task pairs, while asynchronous CPU is better for others. Specifically, synchronous GPU dominates on LR, while asynchronous CPU dominates on SVM. Given that this is essentially a comparison between batch gradient descent – which corresponds to synchronous GPU – and stochastic gradient descent – which corresponds to asynchronous CPU – we do not expect a single winner all the time. As shown previously in the literature [20], the best optimization strategy is particular to the task and the dataset. Our results confirm this finding for parallel optimizers with different model update strategies—a new scenario that has not been studied before. To summarize, while GPU is the optimal architecture for synchronous SGD and CPU is optimal for asynchronous SGD, choosing the better of synchronous GPU and asynchronous CPU is task- and dataset-dependent.

### 6.2.5 Comparison with TensorFlow and BIDMach

We compare our synchronous SGD implementation in ViennaCL with the solutions in TensorFlow and BIDMach based on the results in Figure 16–18 and Figure 19–21. The main point of this comparison is only to verify that our implementation is efficient. We observe that our synchronous SGD outperforms both TensorFlow and BIDMach in time per iteration and time to convergence for all the datasets and all the tasks—both on CPU and GPU. We emphasize that we measure only the time spent in critical processing across all the solutions. The performance of TensorFlow and BIDMach on dense data is comparable. TensorFlow is slightly better on the CPU because of the Java/Scala overhead incurred by BIDMach—which is better on GPU. As previously discussed, TensorFlow has an inefficient matrix transpose on GPU. In terms of statistical efficiency, there are cases where our synchronous SGD requires more iterations to converge. Nonetheless, they are rare and when they occur, the statistical efficiency of our synchronous
SGD is better than that of TensorFlow and BIDMach. The reason there are differences between the synchronous implementations despite them being algorithmically identical is different linear algebra kernels and different model update protocols. In summary, our SGD implementations always outperform TensorFlow and BIDMach in time per iteration, number of iterations to convergence, and time to convergence.

6.2.6 Scalability with the number of examples

In order to study the effect of the number of examples in the training dataset – or the size of the dataset – on the hardware efficiency of our algorithms, we generate three different instances of the covtype and news datasets with increasing number of examples. The size of these datasets is 100 MB, 500 MB, and 1 GB, respectively. We execute all the algorithms on these datasets and measure the time per iteration. The results are depicted in Figure 24. As expected, the time per iteration increases almost linearly with the increase of the dataset size. More importantly, the relative ordering of the algorithms is almost always preserved. Inversions happen on the sparse news dataset and they are minor. Specifically, asynchronous GPU becomes slightly faster than synchronous CPU, while asynchronous CPU becomes slightly faster than synchronous GPU. To put it differently, the synchronous solutions on sparse data are impacted negatively by larger training datasets. The reason is the increase in size of the intermediate results which deteriorate cache efficiency on CPU and memory usage on GPU, respectively. The rate of model update conflicts on dense data is too high for this behavior to be observed. We point out that we cannot study the effect of dataset size on convergence because the value of the loss function changes with the number of examples.

6.2.7 Scalability with the number of features

We take the three lowest-dimensional datasets – covtype, w6a, and real-sim – and materialize them in dense format while keeping the number of examples identical. The largest generated dataset, i.e., real-sim, is 2.15 GB in size. In order to generate data in sparse format, we extract the same number of examples from the three highest-dimensional datasets—real-sim, rcv1, and news. With this number of examples, news has the largest size—approximately 2 GB. We execute all the proposed algorithms on all the datasets for LR and SVM. Figure 25 depicts hardware efficiency as a function of the number of features. On data in dense format – as expected – the time per iteration increases with the increase in dimensionality. Unlike the increase with the number of examples, in this case...
we have a slightly sub-linear increase that impacts all the configurations equally—the relative order of the algorithms is preserved with the increase in dimensionality. For synchronous algorithms, the increase is due entirely to handling larger matrices. In the case of asynchronous algorithms, the examples become complete through “densification”, thus, they access the entire model—the semantics of “zero” is unknown during execution. As a result, the time per iteration is proportional to the number of features. The results on sparse data are more intriguing. First, we observe that going from real-sim to rcv1 – doubling the number of features – reduces the time per iteration for the synchronous algorithms. The increase in dimensionality, however, comes with a relatively small increase in the average number of non-zero dimensions per example. Moreover, the examples in rcv1 display less variance in the number of non-zeros compared to real-sim—rcv1 is more homogeneous than real-sim. We observe that ViennaCL handles the more uniform rcv1 matrix more efficiently with respect to cache and memory access, thus, the reduced time per iteration. The other phenomenon we observe on sparse data is that the relative performance of asynchronous CPU and synchronous GPU switches with the increase in dimensionality. This is similar to the behavior in Figure 24 and the reasons are the same—

asynchronous CPU outperforms synchronous GPU on highly-dimensional models trained over a sufficiently large number of examples.

6.3 Summary

Based on the extensive experiments we perform, we are in the position to provide answers to the questions identified at the beginning of the section. We repeat the questions – this time with the corresponding answers – in the following:

- What is role of the computing architecture, i.e., CPU/GPU, on the performance of synchronous SGD? GPU always outperforms parallel CPU in hardware efficiency and, consequently, in time to convergence. The difference is minimal for small low-dimensional datasets and increases with dimensionality and sparsity—for a maximum speedup of 5.66X.

- What is role of the computing architecture, i.e., CPU/GPU, on the performance of asynchronous SGD? Although parallel CPU outperforms GPU in general, it is more difficult to identify the optimal computing architecture for asynchronous SGD. The main reason is the complex interaction between hardware and statistical efficiency.

- What is the optimal configuration for asynchronous SGD on GPU? The optimal data access path + model replication + data replication configuration depends on the task and the training dataset. Limiting any implementation to a single configuration results in sub-optimal – and sometimes no – convergence.

- How do synchronous and asynchronous SGD compare against each other on CPU and GPU separately, and across computing platforms? Synchronous SGD is the optimal choice on GPU and asynchronous SGD is the safe choice on CPU. The better choice between these two depends on the task and the training dataset since they mirror the comparison between BGD and SGD.

- Are our implementations efficient with respect to TensorFlow and BIDMach? Our synchronous SGD – which is the equivalent of the TensorFlow and BIDMach implementations – is always faster in time to convergence both on CPU and GPU.

- How do the proposed algorithms scale with the number of training examples and the dimensionality of the feature vector, respectively? On dense data, the increase in time per iteration is proportional to the increase in data size for the algorithms. On sparse data, the distribution of the non-zero entries impact scalability to a similar degree as model dimensionality—in certain cases even more.

7 RELATED WORK

SGD on CPU. SGD is the most popular optimization method to train analytics models. Bismarck [12] and GLADE [28] present methods to implement SGD inside a database engine. DimmWitted [39] provides a study on how to implement parallel SGD on NUMA architectures. While similar exploratory axes and measure terminology are introduced, the focus on GPU is what distinguishes our paper from DimmWitted. Hogwild [25] performs model updates concurrently and asynchronously without locks. Due to this simplicity – and the near-linear speedup – Hogwild is widely used in many analytics tasks [31, 12, 24, 11, 9, 6]. Hogbatch [32] is an extension to Hogwild that is more scalable to cache-coherent architectures, while Cyclades [38] reduces model update conflicts using graph partitioning. Hogwild extensions to big models based on model partitioning are introduced in [27, 30]. Buckwild [8] is a low-precision
variant of Hogwild that represents the data and model with fewer bits. Model averaging [41] is an alternative method to parallelize SGD that is adequate in distributed settings. A detailed experimental comparison of Hogwild and averaging is provided in [29]. The integration of relational join with gradient computation has been studied in [21, 22, 33]. These solutions work only for batch gradient descent (BGD), not SGD. A cost-based optimizer that selects between sequential BGD and SGD is proposed in [20].

**SGD on GPU.** SGD is supported by all the major deep learning frameworks, including Caffe, TensorFlow, MXNet, BIDMach, SINGA, Theano, and Torch. These frameworks implement optimized kernels for GPU processing. As far as we can tell, all these kernels are for synchronous SGD—there is no Hogwild GPU kernel. As pointed out in [14], since convolutions are the most expensive operation in deep learning, they are the main candidate for offloading on GPU. GeePS [7] implements a distributed parameter server for training across multiple GPUs. Omnivore [15] is an optimizer for deep learning on CPU and GPU that achieves better SGD performance because of careful data partitioning and placement. The asynchronous SGD supported in Omnivore is cross-device, not within the GPU—the case in our work. GPUs are effectively used for querying deep neural networks in NoScope [37]. The work outside deep learning is targeting low-rank matrix factorization for recommender systems. In [19], dynamic scheduling strategies for low-rank matrix factorization on GPU are explored. The problem is modeled as a graph and scheduling is executed for independent subgraphs which do not have update conflicts. cuMF_SGD [37] extends dynamic scheduling with optimized SGD kernels that leverage the GPU cache, warp-shuffle instructions, and low-precision arithmetic. This is the only Hogwild GPU kernel we found in the literature. However, the design space is not explored at all.

## 8 CONCLUSIONS AND FUTURE WORK

In this paper, we perform a comprehensive study of parallel SGD for generalized linear models over NUMA CPU and GPU architectures. We measure hardware efficiency, statistical efficiency, and time to convergence as a function of the objective function, model updates, and data sparsity. Overall, our study shows that the optimal SGD solution for a given architecture is highly-dependent on all of these factors. Thus, the main value of this work is to map the overall solution space and provide a useful guide for applying parallel SGD in practice. In the process, we also design several optimizations for asynchronous SGD on GPU which have their stand-alone value. We draw several interesting insights from our extensive experimental study on five real datasets. For synchronous SGD, GPU always outperforms parallel CPU—they both outperform a sequential CPU solution by more than 400X. For asynchronous SGD, parallel CPU is the safest choice while GPU with data replication is better in certain situations. The choice between synchronous GPU and asynchronous CPU depends on the task and the characteristics of the data. While LR and SVM are wide-spread ML tasks, it is intriguing to see how the results extend to other types of models, such as low-rank matrix factorization and deep neural nets. This is a topic we will pursue in future work. We point out that in low-rank matrix factorization the structure of the problem imposes limitations that are not SGD-specific, but rather method-specific. Similarly, in convolution deep nets, computing the convolution kernels is the most time-consuming operation. By focusing on simpler tasks such as LR and SVM, we are able to quantify the exclusive performance of the SGD algorithms. In the future, we also plan to consider low-precision formats in data representation and study heterogeneous solutions that integrate concurrent processing across the CPU and GPU. We also intend to explore optimization strategies that select between synchronous GPU and asynchronous CPU dynamically.

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