Thickness Considerations of Two-Dimensional Layered Semiconductors for Transistor Applications

Youwei Zhang1,2, Hui Li1, Haomin Wang3, Hong Xie2, Ran Liu1, Shi-Li Zhang3 & Zhi-Jun Qiu1

Layered two-dimensional semiconductors have attracted tremendous attention owing to their demonstrated excellent transistor switching characteristics with a large ratio of on-state to off-state current, $I_{on}/I_{off}$. However, the depletion-mode nature of the transistors sets a limit on the thickness of the layered semiconductor films primarily determined by a given $I_{on}/I_{off}$ as an acceptable specification. Identifying the optimum thickness range is of significance for material synthesis and device fabrication. Here, we systematically investigate the thickness-dependent switching behavior of transistors with a wide thickness range of multilayer-MoS$_2$ films. A difference in $I_{on}/I_{off}$ by several orders of magnitude is observed when the film thickness, $t$, approaches a critical depletion width. The decrease in $I_{on}/I_{off}$ is exponential for $t$ between 20 nm and 100 nm, by a factor of 10 for each additional 10 nm. For $t$ larger than 100 nm, $I_{on}/I_{off}$ approaches unity. Simulation using technical computer-aided tools established for silicon technology faithfully reproduces the experimentally determined scaling behavior of $I_{on}/I_{off}$ with $t$. This excellent agreement confirms that multilayer-MoS$_2$ films can be approximated as a homogeneous semiconductor with high surface conductivity that tends to deteriorate $I_{on}/I_{off}$. Our findings are helpful in guiding material synthesis and designing advanced field-effect transistors based on the layered semiconductors.

The first successful demonstration of field-effect transistors (FETs) based on monolayer molybdenum disulfide (MoS$_2$) with appealing performance$^{1,2}$ has stimulated intensive research on two-dimensional (2D) transition metal dichalcogenides (TMDs). The planar nature of these 2D semiconductor materials could potentially lead complementary metal-oxide-semiconductor (CMOS) technology to the ultimate size scaling envisioned by Moore’s law and beyond$^{3–5}$. MoS$_2$, a representative layered TMD, has a satisfactory bandgap in the range of 1.3 to 1.8 eV$^{6,7}$, which is advantageous over the well-studied gapless graphene with respect to the standby leakage current of its FETs$^8$. The bandgap of MoS$_2$ is thickness-dependent and it is 1.6 eV for monolayers. As a result, transistors of both single- and multilayer-MoS$_2$ films have exhibited high ratio of on-state to off-state current ($I_{on}/I_{off} > 10^6$) with reasonable electron mobility$^{1,9–11}$. All this makes the layered TMDs promising in fields of low-power switches/circuits$^{11,12}$, nonvolatile memory devices$^{13,14}$, ultrasensitive photodetectors$^{15,16}$, etc.

In FET applications, multilayer MoS$_2$ with a smaller bandgap is of greater potential than the monolayer counterpart$^{17}$. First, multilayer MoS$_2$ has a 3-fold higher density of states and conducts current along multiple channels, which can be translated to a considerably high drive current$^{11,13}$. Second, the interlayer screening effect leads to a higher carrier mobility$^{19,20}$ and better noise immunity$^{21}$ in multilayer MoS$_2$. Compared to the direct-bandgap monolayer MoS$_2$, requiring a strict thickness control, the electronic properties of multilayer MoS$_2$ manifested by an indirect bandgap are relatively insensitive to layer thickness. Hence, multilayer MoS$_2$ is better suited for large-area and/or high-density electronics$^{12,22–32}$. However, multilayer MoS$_2$ and other TMD semiconductors have so far gained limited attention for their use in electronics, compared to their monolayer counterparts.

1State Key Laboratory of ASIC and System, School of Information Science and Technology, Fudan University, Shanghai 200433, China. 2State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem & Information Technology, Chinese Academy of Sciences, Changning Road 865, Shanghai 200050, China. 3Solid-State Electronics, The Ångström Laboratory, Uppsala University, Uppsala Box 534, SE-751 21, Sweden. Correspondence and requests for materials should be addressed to S.-L.Z. (email: shili.zhang@angstrom.uu.se) or Z.-J.Q. (email: zjqiu@fudan.edu.cn)
a 5 nm thick Ti adhesion layer. The Ti adhesion layer that is in intimate contact with MoS2 has a work function of (Supplementary Fig. S2).

whereas a typical top view photomicrograph of a fabricated device is given in Fig. 1b. Isolated MoS2 flakes on of more than 80 devices in a wide thickness range. Differences in digital logic applications, thickness range is of significance for material synthesis and practical device application of the 2D TMDs. For

unintentional chastic nature of the MoS2 exfoliation process. The source and drain metal used in our devices is 50 nm Au with channel width that is determined by the width of the flakes varies in the range of 2–60 flakes,

the SiO2/Si substrate were exfoliated from a bulk MoS2 crystal using a conventional mechanical exfoliation technique32. The sample preparation and device fabrication are detailed in Methods. The thickness of different flakes, \( t \), was measured by means of atomic force microscopy (AFM), as illustrated in Fig. 2. Only one channel length of 10\( \mu \)m is used for all devices and it is defined by the spacing of a Cu grid shadow mask. However, the channel width that is determined by the width of the flakes varies in the range of 2–60\( \mu \)m as a result of the stochastic nature of the MoS2 exfoliation process. The source and drain metal used in our devices is 50 nm Au with a 5 nm thick Ti adhesion layer. The Ti adhesion layer that is in intimate contact with MoS2 has a work function of \( \sim 4.3 \) eV, which is very close to the conduction band edge of thin-layer MoS2.8,31. Furthermore, Ti is a transition metal with its d-electron orbitals mixing favorably with the 4\( d \) states of Mo and resulting in an increase in the density of states at the Fermi level and a strong Fermi level pinning at the contact9,34,35. Therefore, this favorable interface geometry is expected to facilitate a good chemical bonding and allow for a maximized electron injection at the source/drain contacts with an increased overlap between the states at the interface.

The transfer characteristics of a back-gate multilayer-MoS2 FET shows a typical \( n \)-type unipolar carrier transport behavior (Fig. 3a). This confirms a rather small \( (<0.1 \) eV), if not negligible, Schottky barrier height (SBH) for electrons at the Au/Ti-MoS2 contacts (Supplementary Fig. S1). The SBH for holes is, thus, high \( (>1.2 \) eV) since the sum of electron SBH and hole SBH should approximately be equal to the energy bandgap (1.3 eV) of MoS2 (inset in Fig. 3a). Tunneling through the Schottky barrier at the metal/MoS2 contacts not only limits the charge injection in the device at its on-state but also plays a critical role when evaluating the device off-state in the subthreshold region of the transistor. The small electron SBH facilitates the injection of accumulated electrons at positive gate voltage, \( V_g \), while the large hole SBH suppresses the injection of inverted holes at negative \( V_g \). This results in the \( n \)-type unipolar behavior with a high \( I_{on}/I_{off} \) and is in stark contrast to the ambipolar conduction behavior in graphene FETs with a low \( I_{on}/I_{off} \). The FET with a 30-nm-thick multilayer MoS2 in Fig. 3a operates as a depletion-mode FET with a large negative threshold voltage, \( V \), and a high \( I_{on}/I_{off} \) of \( 10^3 \). All the FETs fabricated in this work exhibit the same \( n \)-type characteristics, regardless of the thickness of the MoS2 film in channel (Supplementary Fig. S2).

Results

A schematic representation of a back-gate multilayer-MoS2 transistor used in our work is shown in Fig. 1a, whereas a typical top view photomicrograph of a fabricated device is given in Fig. 1b. Isolated MoS2 flakes on the SiO2/Si substrate were exfoliated from a bulk MoS2 crystal using a conventional mechanical exfoliation technique32. The source and drain metal used in our devices is 50 nm Au with a 5 nm thick Ti adhesion layer. The Ti adhesion layer that is in intimate contact with MoS2 has a work function of \( \sim 4.3 \) eV, which is very close to the conduction band edge of thin-layer MoS2.8,31. Furthermore, Ti is a transition metal with its d-electron orbitals mixing favorably with the 4\( d \) states of Mo and resulting in an increase in the density of states at the Fermi level and a strong Fermi level pinning at the contact9,34,35. Therefore, this favorable interface geometry is expected to facilitate a good chemical bonding and allow for a maximized electron injection at the source/drain contacts with an increased overlap between the states at the interface.

The transfer characteristics of a back-gate multilayer-MoS2 FET shows a typical \( n \)-type unipolar carrier transport behavior (Fig. 3a). This confirms a rather small \( (<0.1 \) eV), if not negligible, Schottky barrier height (SBH) for electrons at the Au/Ti-MoS2 contacts (Supplementary Fig. S1). The SBH for holes is, thus, high \( (>1.2 \) eV) since the sum of electron SBH and hole SBH should approximately be equal to the energy bandgap (1.3 eV) of MoS2 (inset in Fig. 3a). Tunneling through the Schottky barrier at the metal/MoS2 contacts not only limits the charge injection in the device at its on-state but also plays a critical role when evaluating the device off-state in the subthreshold region of the transistor. The small electron SBH facilitates the injection of accumulated electrons at positive gate voltage, \( V_g \), while the large hole SBH suppresses the injection of inverted holes at negative \( V_g \). This results in the \( n \)-type unipolar behavior with a high \( I_{on}/I_{off} \) and is in stark contrast to the ambipolar conduction behavior in graphene FETs with a low \( I_{on}/I_{off} \). The FET with a 30-nm-thick multilayer MoS2 in Fig. 3a operates as a depletion-mode FET with a large negative threshold voltage, \( V \), and a high \( I_{on}/I_{off} \) of \( 10^3 \). All the FETs fabricated in this work exhibit the same \( n \)-type characteristics, regardless of the thickness of the MoS2 film in channel (Supplementary Fig. S2).
The depletion-mode nature of the transistors will set a limit on the thickness of the multilayer MoS$_2$ films primarily determined by the preset $I_{on}/I_{off} = 10^3$ as an acceptable specification. Over 80 multilayer-MoS$_2$ FETs were fabricated and characterized. Their $I_{on}$ and $I_{off}$ versus $t$ ranging from 6 nm to 225 nm are plotted in Fig. 3b. The minimum $I_{off}$ occurring for the smallest $t$ is limited by the noise level in the devices. A clear trend is observed for $I_{off}$; it increases rapidly with increasing $t$ below 100 nm. Beyond $t = 100$ nm, $I_{off}$ becomes comparable with $I_{on}$ and is almost independent of layer thickness. The stochastic variation of the flake widths makes the variation of $I_{on}$ with $t$ unspecific. However, $I_{on}/I_{off}$ is unaffected by the width variation due to the same width-dependence of $I_{on}$ and $I_{off}$. In the first 20–30 nm, $I_{on}/I_{off}$ exhibits a gradual decrease with increasing $t$, see Fig. 3c, likely caused by the $I_{off}$ variation. This is followed by an exponential decrease in $I_{on}/I_{off}$ with $t$ until it approaches unity for $t > 100$ nm. This is better seen in the inset of Fig. 3c where the best linear fit to the logarithmic $I_{on}/I_{off}$ versus $t$ in the range of 20–100 nm gives

$$
\log_{10} \left( \frac{I_{on}}{I_{off}} \right) = 8.24 - 0.087t
$$

It is well known that in the monolayer 2D materials, the charge carriers are confined in the 2D planes. This confinement can result in some unique characteristics not common in 3D materials, e.g. Si. When the layer thickness is increased, the carriers can hop freely between neighboring layers and move in the whole 2D layered

---

**Figure 2.** (a–d) AFM images of 9, 27, 60 and 103-nm thick MoS$_2$ films on SiO$_2$/Si substrate. The height profiles are measured along the dashed lines in the images.
material. As a result, the carriers distribute fairly uniformly in the 2D material. In this aspect, multilayer-MoS2 films can be approximated as a homogeneous semiconductor and simulated with traditional device simulators. We have therefore used a commercial simulation tool SILVACO TCAD to numerically solve the coupled Poisson and continuity equations for the multilayer-MoS2 FETs. Our focus here is on charge and current distributions in MoS2. For simplicity, the electron SBH is set to 0.1 eV and the unintentional n-doping concentration, N_d, in MoS2 is assumed to be $3.5 \times 10^{17}$ cm$^{-3}$, in order to attain identical $V_t$ between the simulation and experiments. The doping concentration in MoS2 is found to vary from $10^{16}$ to $10^{19}$ cm$^{-3}$. The other material parameters used in the simulation are shown in Supplementary Table S1. The simulated transfer characteristics of multilayer-MoS2 FETs for various channel thicknesses (Fig. 4a) and the variation of $I_{on}/I_{off}$ with $t$ (Fig. 4b) are in good agreement with the experimental results. In particular, the simulated $I_{on}/I_{off}$ shows a steep decrease with $t$ around ~50 nm, matching very well with the data in Fig. 3c. This critical thickness is strongly correlated with $W_{max}$ that is related to $N_d$ by the following formula:

$$W_{max} = \frac{4kT_\varepsilon_0}{q^2} \ln \frac{N_v}{n_i}$$

where, $k$ is the Boltzmann constant, $T$ is absolute temperature, $q$ is elementary charge, $\varepsilon_0$ is the relative dielectric constant of multilayer MoS2 (~11), $\varepsilon_0$ is the vacuum permittivity, and $n_i = 1.6 \times 10^5$ cm$^{-3}$ is the intrinsic carrier concentration in MoS2 due to thermal interband excitation. The calculated $W_{max}$ with the given $N_d$ is ~60 nm. The spatial distribution of charge carriers is inhomogeneous, due to charge screening, along the depth of the薄膜.
multilayer MoS$_2$ film. Specifically, the charge carriers in the MoS$_2$ layers close to the SiO$_2$ interface are effectively controlled by $V_g$. The electrostatic gate control of the carriers are weakened gradually, or even completely lost, in the MoS$_2$ layers further away from the SiO$_2$ interface on the account of charge screening.

As the device switching behavior is mainly determined by $I_{on}/I_{off}$, the carrier distribution at negative $V_g$ is shown, respectively, in Fig. 5a,b for $t < W_{max}$ and $t > W_{max}$. At a negative $V_g$, electrons are repelled from while holes are attracted to the MoS$_2$/SiO$_2$ interface. For $t < W_{max}$, electrons are depleted in the whole MoS$_2$ film at $V_g < -25$ V. Simultaneously, an inversion layer populated with holes is formed at the MoS$_2$/SiO$_2$ interface. However, when $t > W_{max}$, the carrier concentration close to the sample surface (away from the MoS$_2$/SiO$_2$ interface) remains constant independent of $V_g$. This is a result of charge screening effect that results in a poor electrostatic control of the electrons in the excess part of the MoS$_2$ film. This high and uncontrolled electron concentration in this excess
MoS₂ close to the sample surface, shown in Fig. 5c, contributes to I\text{off}. Although a hole inversion layer is formed under large negative V\text{g}, the hole conduction current can be neglected due to a large SBH at the contact interfaces (see Fig. 5d).

It is established now that W\text{max} is an important parameter determining the switching behavior of multilayer-MoS₂ FETs. When t ≪ W\text{max} the electrons can be fully depleted from the entire channel region under negative V\text{g} and an excellent switching behavior with a very low leakage current prevails. Under such circumstances, I\text{on}/I\text{off} is rather insensitive to t, as manifested by the slowly descending I\text{on}/I\text{off} with t shown in Figs 3c and 4b. When t around W\text{max}, the electrons in the excess part of the MoS₂ film cannot be fully depleted easily. An exponential decrease in I\text{on}/I\text{off} by about 4 orders of magnitude with t changing from 30 to 65 nm. Moreover, W\text{max} depends on doping concentration. The stochastic doping concentration in the MoS₂ flakes can induce a variation in W\text{max} which in its turn results in a large spread in the switching property at ~60 nm (indicated by a circle in the inset of Fig. 3c).

Discussion

In view of its significance in device physics, design and fabrication, quantifying the transistor switching behavior as a function of the layer thickness of the 2D semiconductor materials is of vital importance. A critical parameter W\text{max} is discussed when characterizing layered TMD semiconductors such as MoS₂ as the channel material in FETs. Both experimental and theoretical studies show W\text{max} = 50–60 nm for the multilayer-MoS₂ FETs. At this thickness, the FETs are characterized by an acceptable I\text{on}/I\text{off} around 10^6. If the multilayer-MoS₂ film is thinner than this W\text{max}, an excellent switching behavior with a low leakage current and a much higher I\text{on}/I\text{off} (than 10^6) will prevail. If the multilayer-MoS₂ film is substantially thicker than this W\text{max}, a large leakage current will persist and the switching behavior becomes inferior. An exponential decrease in I\text{on}/I\text{off} is found in the 20–100 nm thickness range, by a factor of 10 for each additional 10 nm. The findings in this work are useful in guiding material synthesis and designing advanced FETs with layered TMD semiconductors. It appears that the device physics established for traditional semiconductors such as Si is applicable for the layered TMD semiconductors, as it should be.

Methods

Thin MoS₂ flakes were peeled off from bulk MoS₂ (SPI supplies) by mechanical exfoliation. They were subsequently transferred to a heavily doped p-type Si substrate with a 300-nm-thick thermally grown SiO₂. The SiO₂/Si substrate was pre-cleaned by sonication in acetone, isopropyl alcohol, and deionized water. The transferred MoS₂ flakes were identified using an optical microscope (Keyence digital microscope VHX-600). The thickness of the MoS₂ flakes was measured using AFM (Dimension 3100 with Nanoscope IIIa controller, Veeco) operated in tapping mode under ambient conditions. In order to avoid contamination from photolithography or electron-beam lithography, a 10-μm spacing copper grid was placed on top of the thin MoS₂ flakes as a shadow mask for the electrode fabrication. A bilayer stack Ti/Au of 5/50 nm thickness was then deposited by means of electron-beam evaporation as the source and drain electrodes. The heavily doped Si substrate was used as the common back gate for the fabricated MoS₂ FETs. Electrical characterization of the devices was carried out in a shielded probe station with Keithley 4200 semiconductor characterization system in ambient environments.

References

1. Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V. & Kis, A. Single-layer MoS₂ transistors. Nature Nanotechnol. 6, 147–150 (2011).
2. Wang, Q. H., Kalantar-Zadeh, K., Kis, A., Coleman, J. N. & Strano, M. S. Electronics and optoelectronics of two-dimensional transition metal dichalcogenides. Nature Nanotechnol. 7, 699–712 (2012).
3. Liu, L., Kumar, S. B., Ouyang, Y. & Guo, J. Performance limits of monolayer transition metal dichalcogenide transistors. IEEE Trans. Electron Devices 58, 3042–3047 (2011).
4. Yoon, Y., Ganapathi, K. & Salahuddin, S. How good can monolayer MoS₂ transistors be? Nano Lett. 11, 3768–3773 (2011).
5. Alam, K. & Lake, R. K. Monolayer MoS₂ transistors beyond the technology road map. IEEE Trans. Electron Devices 59, 3250–3254 (2012).
6. Mak, K. F., Lee, C., Hone, J., Shan, J. & Heinz, T. F. Atomically thin MoS₂: a new direct-gap semiconductor. Phys. Rev. Lett. 105, 136805 (2010).
7. Splendiani, A. et al. Emerging photoluminescence in monolayer MoS₂. Nano Lett. 10, 1271–1275 (2010).
8. Schwierz, F. Graphene transistors. Nature Nanotechnol. 5, 487–496 (2010).
9. Das, S., Chen, H.-Y., Penunurtha, A. V. & Appenzeller, J. High performance multilayer MoS₂ transistors with scandium contacts. Nano Lett. 13, 100–105 (2013).
10. Liu, H., Neal, A. T. & Ye, P. D. Channel length scaling of MoS₂ MOSFETs. ACS Nano 6, 8563–8569 (2012).
11. Kim, S. et al. High-mobility and low-power thin-film transistors based on multilayer MoS₂ crystals. Nature Commun. 3, 1011 (2012).
12. Chang, H.-Y. et al. High-performance, highly bendable MoS₂ transistors with high-K dielectrics for flexible low-power systems. ACS Nano 7, 5446–5452 (2013).
13. Bertolazzi, S., Krasnozhon, D. & Kis, A. Nonvolatile memory cells based on MoS₂/graphene heterostructures. ACS Nano 7, 3246–3252 (2013).
14. Lee, H. et al. MoS₂ Nanosheets for top-gate nonvolatile memory transistor channel. Small 8, 3111–3115 (2012).
15. Lopez-Sanchez, O., Lembke, D., Kaya, M., Radenovic, A. & Kis, A. Ultrathin metal-oxide-semiconductor field-effect transistors based on monolayer MoS₂, Nature Nanotechnol. 8, 497–501 (2013).
16. Choi, W. et al. High-defectivity multilayer MoS₂ phototransistors with spectral response from ultraviolet to infrared. Adv. Mater. 24, 5832–5836 (2012).
17. Ganatra, R. & Zhang, Q. Few-layer MoS₂: A promising layered semiconductor. ACS Nano 8, 4074–4099 (2014).
18. Kaasbjerg, K., Thygesen, K. S. & Jacobsen, K. W. Phonon-limited mobility in n-type single-layer MoS₂ from first principles. Phys. Rev. B 85, 115317 (2012).
19. Castellanos-Gomez, A. et al. Electric-field screening in atomically thin layers of MoS₂: the role of interlayer coupling. Adv. Mater. 25, 899–903 (2013).
20. Li, S.-L. et al. Thickness-dependent interfacial coulomb scattering in atomically thin field-effect transistors. Nano Lett. 13, 3546–3552 (2013).
21. Kwon, H.-J., Kang, H., Jang, J., Kim, S. & Grigorenko, A. Analysis of flicker noise in two-dimensional multilayer MoS₂ transistors. Appl. Phys. Lett. 104, 083110 (2014).
22. Liu, K.-K. et al. Growth of large-area and highly crystalline MoS₂ thin layers on insulating substrates. Nano Lett. 12, 1538–1544 (2012).
23. Laskar, M. R. et al. Large area single crystal (0001) oriented MoS₂. Appl. Phys. Lett. 102, 252108 (2013).
24. Tarasov, A. et al. Highly uniform trilayer molybdenum disulfide for wafer-scale device fabrication. Adv. Funct. Mater. 24, 6389–6400 (2014).
25. Qu, H. et al. Hopping transport through defect-induced localized states in molybdenum disulphide. Nature Commun. 4, 2642 (2013).
26. Zhou, W. et al. Intrinsic structural defects in monolayer molybdenum disulfide. Nano Lett. 13, 2615–2622 (2013).
27. Najmaei, S., Yuan, J., Zhang, J., Ajayan, P. & Lou, J. Synthesis and defect investigation of two-dimensional molybdenum disulfide atomic layers. Acc. Chem. Res. 48, 31–40 (2015).
28. Radisavljevic, B. & Kis, A. Mobility engineering and a metal-insulator transition in monolayer MoS₂, Nature Mater. 12, 815–820 (2013).
29. Zou, X. et al. Interface engineering for high-performance top-gated MoS₂ field-effect transistors. Adv. Mater. 26, 6255–6261 (2014).
30. Zhang, Y., Ye, J., Matsushita, Y. & Iwasa, Y. Ambipolar MoS₂ thin flake transistors. Nano Lett. 12, 1136–1140 (2012).
31. Jariwala, D., Sangwan, V. K., Lauhon, L. J., Marks, T. J. & Hersam, M. C. Emerging device applications for semiconducting two-dimensional transition metal dichalcogenides. ACS Nano 8, 1102–1120 (2014).
32. Novoselov, K. S. et al. Electric field effect in atomically thin carbon films. Science 306, 666–669 (2004).
33. Hughes, H. P. & Starnberg, H. I. Electron Spectroscopies Applied to Low-Dimensional Structures. Kluwer Academic Publishers: Dordrecht, the Netherlands, 2000).
34. Popov, I., Seifert, G. & Tománek, D. Designing electrical contacts to MoS₂ monolayers: a computational study. Phys. Rev. Lett. 108, 156802 (2012).
35. Gong, C., Colombo, L., Wallace, R. M. & Cho, K. The unusual mechanism of partial Fermi level pinning at metal-MoS₂ interfaces. Nano Lett. 14, 1714–1720 (2014).
36. Taur, Y. & Ning, T. H. Fundamentals of Modern VLSI Devices, (Cambridge University Press: Cambridge, UK 1998).
37. Zhang, Y. et al. On Valence-band splitting in layered MoS₂, ACS Nano 9, 8514–8519 (2015).
38. SILVACO. ATLAS User’s Manual. SILVACO Inc., Santa Clara, CA 95054, 2008.
39. Howell, S. L. et al. Investigation of band-offsets at monolayer-multilayer MoS₂ junctions by scanning photocurrent microscopy. Nano Lett. 15, 2278–2284 (2015).
40. Chetwanchamnangij, T. & Lambrecht, W. R. L. Quasiparticle band structure calculation of monolayer-bilayer MoS₂ junctions. ACS Nano 8, 2642 (2014).
41. Zhang, C., Wang, H., Chan, W., Manolatou, C. & Rana, F. Absorption of light by excitons and trions in monolayers of metal dichalcogenide MoS₂: experiments and theory. Phys. Rev. B 89, 205436 (2014).

Acknowledgements
This work is supported partially by the National Natural Science Foundation of China (Nos 61204090 and 61171010), Fundamental Research Project of young teachers to enhance research capacity, Fudan University (No. 20520133248), State Key Laboratory of ASIC & System, Fudan University (No. 2015MS005), the Swedish Research Council (No. 2014-5591) and the Knut & Alice Wallenberg Foundation (No. 2011.0082).

Author Contributions
Z.-J.Q. conceived the research and analyzed the results. Y.Z., H.W. and H.X. carried out MoS₂ device fabrication. Y.Z. performed AFM analysis and electrical characterization. H.L. performed TCAD simulation. Z.-J.Q., S.-L.Z. and R.L. wrote the manuscript. All authors discussed the results and commented the manuscript.

Additional Information
Supplementary information accompanies this paper at http://www.nature.com/srep

Competing financial interests: The authors declare no competing financial interests.

How to cite this article: Zhang, Y. et al. Thickness Considerations of Two-Dimensional Layered Semiconductors for Transistor Applications. Sci. Rep. 6, 29615; doi: 10.1038/srep29615 (2016).

This work is licensed under a Creative Commons Attribution 4.0 International License. The images or other third party material in this article are included in the article’s Creative Commons license, unless indicated otherwise in the credit line; if the material is not included under the Creative Commons license, users will need to obtain permission from the license holder to reproduce the material. To view a copy of this license, visit http://creativecommons.org/licenses/by/4.0/