Research on Grid High Voltage Harmonic Detection Based on Ubiquitous Power Wireless Network

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Abstract. The intelligent optimized operation of the power grid depends on the ubiquitous perception of the system and complete and correct data support, which is also the most basic requirement that the ubiquitous power Internet of Things perception layer must meet. In the application of ubiquitous power Internet of Things, obtaining complete and correct measurement data is the basis for managing power quality problems. However, in the entire link of the actual grid collection and transmission, data defects will inevitably occur. Based on the background of the ubiquitous power Internet of Things wireless network, the paper adopts the idea of modular programming and divides it into three modules: frequency measurement sampling, waveform display and harmonic display according to the performance indicators of the harmonic analyser. It can measure the frequency of the input AC voltage, perform AC synchronous sampling of the input voltage according to the measured frequency, and display the waveform of the input voltage; and then calculate the harmonics of each order through the FFT algorithm. The simulation found that the proposed control strategy significantly improved the harmonic current content than the traditional d-q positive and negative sequence decoupling control.

Key words. Ubiquitous Power Internet of Things, Power Wireless Network, High Voltage Harmonic Detection, Smart Grid.

1. Introduction

In recent years, the rapid growth of installed capacity and large-scale grid connection of distributed renewable energy (DRE) such as wind power and photovoltaics has greatly increased the peak-to-valley difference of power. Traditional peak-shaving methods can no longer fully adapt to the new situation. Development of DRE, represented by photovoltaics and wind power, has problems such as scattered geographical location and intermittent output. It is difficult for the grid dispatching center to accurately cover and dispatch it. Therefore, it is traditionally considered that it is not suitable to undertake auxiliary power services such as peak shaving [1]. Based on the ubiquitous power Internet of Things, VPP can aggregate many DRE, energy storage equipment, and demand-side resources, providing the possibility for DRE to connect to the grid on a large scale and participate in system peak shaving.
In the power system, the harmonics generated by various harmonic sources cause pollution to the power system environment and affect the electrical environment of the entire power system, including the power system itself and the majority of users. Preliminary summed up, the main performance is that due to the high-order harmonic current flowing, the electrical equipment is overheated due to additional power consumption, or magnetic induction obstacles occur; the distortion rate due to the high-order harmonics is very important for the use of voltage harmonic control. The equipment may cause malfunction or loss of control; due to the existence of high-order harmonics, the communication line will have noise and dangerous induced electromotive force. In summary, it can be seen that no matter from the perspective of ensuring the safe and economic operation of the power system and the power supply system or ensuring the safety of equipment and people, it is urgent to regularly detect and limit the harmful effects of harmonic pollution.

2. Concept analysis

2.1. Development trend and network structure of ubiquitous power Internet of Things
State Grid Corporation puts forward the concept of ubiquitous power Internet of Things, centering on all aspects of the power system, fully applying modern communication technologies and information technologies such as mobile communications, the Internet, and artificial intelligence to realize the perception, interconnection, interaction, information processing, and Smart services and other functions provide sufficient and effective information services and data support for planning and construction, production operation, operation management, comprehensive services, development of new business models, and construction of corporate ecological environment [2]. The ubiquitous power Internet of Things includes a four-layer structure of perception layer, network layer, platform layer, and application layer, as follows:

a) The perception layer is used for the collection and processing of information and data, mainly including sensors, field collection equipment, smart business terminals, edge IoT agents and other equipment. b) The network layer is used to transmit the information and data of the perception layer to the corresponding platform for processing, and is used to transmit data and instructions. It mainly includes several networks such as access network, data network, transmission network, and satellite network. The key problem to be solved at the network layer is to promote the construction of electric power wireless private network and terminal communication, improve network coverage, enhance network bandwidth, achieve wide coverage, deep coverage and thick coverage, improve network resource allocation capabilities, and meet the needs of emerging business development. c) The platform layer mainly processes and analyzes the information and data collected by the perception layer, and provides the processing results to the perception layer. The goal of the platform layer is to achieve a large platform, multi-scenario architecture, and build a unified platform. Through the "cloud and fog collaboration" architecture, data sharing and high-speed and accurate processing can be realized, and the combination and construction of different types of applications can be supported. d) At the application level, according to different application requirements, corresponding analysis and processing of data are carried out to realize different functions [3]. The purpose is to better support core business operations more intelligently, serve the energy Internet ecosystem, improve management levels, and expand business scope.

2.2. Harmonic suppression
When evaluating the power supply quality of a power system, it is generally only required that the amplitude and frequency of the grid voltage remain stable. Therefore, in the National Electrical Code, the standards for voltage amplitude and power supply frequency are mainly compared with other indicators. These indicators more importantly determine the operating frequency of electrical equipment and the technical and economic indicators of the power grid. In recent decades, due to the emergence of harmonic problems, the scope and extent of harm caused by harmonics in some cases is comparable to the harm caused by unqualified main quality indicators of electric energy. The
experience and forecast of developed countries show that with the development of science and technology, the types, quantity and power consumption of non-linear load power equipment will also increase rapidly [4]. It is recognized internationally that harmonic pollution is a public hazard to the power grid and measures must be taken to limit it. Since 1984, the International Conference on Power System Harmonics has been held every two years, providing a direct channel for international exchanges in this field and promoting the development of harmonic research.

Since the actual measurement of the interference of the harmonics of the power grid has become one of the necessary measures to ensure the safe and economic operation of the power grid and high-quality power supply, countries around the world have developed and developed a series of harmonic measurement and analysis devices and instruments. The history of harmonic measurement and analysis has developed with the rapid development of integrated circuits, microprocessors and computers, and a series of harmonic analysers based on fast Fourier transform have been produced. The measured signal is maintained, A/D conversion, Fourier calculation output results, the test operation is simple and convenient, and the computer results are fast and accurate [5]. A new generation of multifunctional, digital, automated and intelligent harmonic measurement analysers has become the main direction of development.

3. Introduction to Harmonic Analysis Algorithm

Harmonic analysis of power system usually adopts fast Fourier transform (FFT); wavelet transform is also widely used in the field of harmonic analysis due to its good time-frequency analysis characteristics; this design adopts fast Fourier transform. Fast Fourier Transform (FFT) is the most widely used harmonic detection method in today’s harmonic detection. It can easily calculate and analyse the signal. Fast Fourier Transform is a fast algorithm of Discrete Fourier Transform (DFT). The FFT algorithm continuously decomposes the DFT of a long sequence into several DFTs of short sequences, and uses the periodicity and symmetry of the butterfly factor to reduce the number of operations. Using this method to measure harmonics has high accuracy and is easy to use. Therefore, when performing harmonic analysis, FFT analysis must be performed first. The simplest and most commonly used algorithm is radix-2FFT. The definition of DFT is shown in (1):

\[ X(k) = \sum_{n=0}^{N-1} x(n)W_n^kR_n(k) \]  

In the formula, \( W_n^k \) is called butterfly factor. If you directly calculate DFT according to this, the calculation amount is \( N^2 \) complex multiplications and \( N(N+1) \) complex additions. When \( N \) is large, the amount of calculation is quite large, for which fast Fourier transform is used. FFT algorithms can generally be divided into two categories: time decimation FFT and frequency decimation. The time decimation FFT algorithm divides the input sequence of \( N \) points in the time domain into odd and even sequences according to odd and even numbers in each stage of processing; while the frequency decimation FFT is to decompose the sequence into odd and even sequences in the frequency domain. Form to calculate. In order to decompose the DFT of the large number of points into the DFT of the small number of points for calculation, the length of the sequence \( N \) is required to be a composite number, and the most commonly used is the case of \( N = 2^M \) (\( M \) is a positive integer). First divide the sequence \( x(n) \) into two groups according to the parity items:

\[
\begin{align*}
    x(2r) &= x_1(r) \\
    x(2r+1) &= x_2(r)
\end{align*}
\]

Then, divide the DFT operation into two groups accordingly...
Among them, $X_1(k)$, $X_2(k)$ and B are the N/2 point DFT of $x_1(n), x_2(n)$ respectively:

$$X_1(k) = \sum_{r=0}^{N/2-1} x_1(r)W_{N/2}^{rk} = \sum_{r=0}^{N/2-1} x(2r)W_{N/2}^{rk}, 0 \leq k \leq \frac{N}{2}-1$$  \hspace{1cm} (4)

$$X_2(k) = \sum_{r=0}^{N/2-1} x_2(r)W_{N/2}^{rk} = \sum_{r=0}^{N/2-1} x(2r+1)W_{N/2}^{rk}, 0 \leq k \leq \frac{N}{2}-1$$  \hspace{1cm} (5)

So far, an N-point DFT is decomposed into two N/2-point DFTs. From formula $X(k) = X_1(k) + W_N^kX_2(k)$, we can get:

$$X(k + \frac{N}{2}) = X_1(k) - W_N^kX_2(k)$$  \hspace{1cm} (6)

In this way, the N-point DFT can all be determined by the following formula:

$$\begin{align*}
X(k) &= X_1(k) + W_N^kX_2(k) \\
X(k + \frac{N}{2}) &= X_1(k) - W_N^kX_2(k)
\end{align*}$$  \hspace{1cm} (7)

The above formula can be represented by a special dish-shaped symbol. The symbol shown in Figure 1 corresponds to one complex multiplication and two complex addition operations.
After this decomposition, each N/2-point DFT only requires \( (\frac{N}{2})^2 = \frac{N^2}{4} \) complex multiplications, and two N/2-point DFTs require \( 2(\frac{N}{2})^2 = \frac{N^2}{2} \) complex multiplications, plus the two N/2-point DFTs are combined into N points. In DFT, there are N/2 multiplications by the W factor, and a total of \( \frac{N^2}{2} + \frac{N}{2} \approx \frac{N^2}{2} \) multiplications are required. It can be seen that after only one decomposition, the calculation amount is reduced by nearly half. By analogy, after M decompositions, the N-point DFT is finally decomposed into N 1-point DFTs and M-level butterfly operations, and the 1-point DFT is the time domain sequence itself.

4. Harmonic suppression system and simulation

4.1. System design

The harmonic analyser system is based on the MSP430F5529 single-chip microcomputer, and its peripheral module circuits include: voltage sampling circuit, filter circuit, shaping circuit, unipolar conversion circuit, button circuit and liquid crystal display circuit. The system block diagram is shown in Figure 2.

![Figure 2. System composition block diagram](image)

The input 220V AC voltage is stepped down through the voltage sampling circuit, filtered through a low-pass filter after the step down, and the filtered voltage signal is input to the unipolar conversion circuit and the shaping circuit respectively. The unipolar conversion circuit generates a DC voltage through the MC1403 chip, and the DC voltage is superimposed on the input AC voltage through the operational amplifier to complete the unipolar conversion. The voltage shaping circuit is composed of a hysteresis comparator, and the filtered sinusoidal voltage can be shaped into a square wave through the module. Input the square wave to MSP430 single-chip computer system to be able to carry on the frequency measurement, can calculate the time interval of AC voltage sampling through the measured frequency [6]. The AC voltage after unipolar conversion is input to the single-chip system, and the 64-point AC synchronous sampling is performed according to the sampling interval time calculated by the
frequency measurement. After sampling, the coordinates of each point are calculated according to the sampled data, and then the voltage waveform is displayed on the LCD screen. Perform FFT operation to calculate the amplitude of each harmonic and display each harmonic on the LCD screen by pressing the button.

4.2. Simulation analysis

Use timer A1 to measure frequency, set timer A1 to capture mode, when the rising edge of the square wave arrives, record the value of the current timer counter, and calculate the measured frequency by the difference between two consecutive counts [7].

First, select the clock and the timer counting mode. These are determined by the TA1CTL register. The register selects TASSEL_2, that is, the clock selects the subsystem clock SMCLK and ID_3, which means that the clock is divided by eight. The subsystem clock is multiplied by 25M and divided by eight to 3.125M, that is, the clock of timer A1 is 3.125M; select MC_2, set the counting mode to continuous counting mode, and clear the initial count value [8]. Observe the output waveform of the hardware circuit with an oscilloscope. The waveform after unipolar conversion is shown in Figure 3:

![Figure 3. Unipolar conversion effect diagram](image)

5. Conclusion

This paper studies the feasibility and economy of DRE participating in peak shaving in the form of VPP under the background of building ubiquitous power Internet of Things. The simulation shows that the proposed scheme greatly reduces the harmonic current content than the traditional d-q positive and negative sequence decoupling control, and the algorithm workload is greatly reduced compared with the control scheme of extracting specific sub-harmonic currents alone, which has development potential.

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