Quantum error correction and fault-tolerance make it possible to perform quantum computations in the presence of imprecision and imperfections of realistic devices. An important question is to find the noise rate at which errors can be arbitrarily suppressed. By concatenating the 7-qubit Steane and 15-qubit Reed-Muller codes, the 105-qubit code enables a universal set of fault-tolerant gates despite not all of them being transversal. Importantly, the CNOT gate remains transversal in both codes, and as such has increased error protection relative to the other single qubit logical gates. We show that while the level-1 pseudo-threshold for the concatenated scheme is limited by the logical Hadamard, the error suppression of the logical CNOT gates allows for the asymptotic threshold to increase by orders of magnitude at higher levels. We establish a lower bound of $1.28 \times 10^{-3}$ for the asymptotic threshold of this code which is competitive with known concatenated models and does not rely on ancillary magic state preparation for universal computation.

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I. INTRODUCTION

Quantum computers have the potential to greatly enhance the efficiency of certain computational problems. However, they rely on the storage and manipulation of many quantum systems in superposition, and it is this careful juxtaposition of storage and manipulation of the quantum states that renders their development to be so difficult. Namely, by making individual quantum systems easily accessible to control often leads to increased external noise. Suppressing noise in a scalable manner is thus a necessary requirement for any quantum computing architecture, promoting the need for quantum error correction and fault-tolerance.

Quantum error correcting codes come in many different forms, yet the key to any error correcting scheme is the establishment of a fault-tolerance threshold [1–4]. Concatenated codes have played a key role in determining these threshold rates due to their ability to iteratively suppress errors by increasing levels of concatenation. Along these lines, Aliferis, Gottesman, and Preskill established a rigorous lower bound for the fault-tolerance threshold of concatenated codes by introducing a technique called malignant set counting [5]. Paetznick and Reichardt used this method to establish a circuit level noise threshold for the 23-qubit Golay code under physical depolarizing noise, obtaining a threshold error rate of $1.32 \times 10^{-3}$.

One of the most prominent methods for implementing a logical fault-tolerant gate is by implementing the gate transversally, that is by applying individual physical gates to each of the qubits composing the logical qubit. However, as shown by Eastin and Knill, the set of transversal gates for a given code generates a finite group, and therefore cannot be universal for quantum computation [6]. In order to circumvent this fundamental restriction and potentially reduce the qubit overhead seen in magic state distillation [7], many recent fault-tolerant proposals for universal logical quantum computation have focused on code conversion and gauge fixing [8–13]. In this work, we study a parallel construction for universal fault-tolerant quantum computation through the concatenation of two error correcting codes [14]. The idea behind this scheme is to protect the gate that is not transversal for one code through its implementation using transversal gates in the other code. The concatenation scheme provides a dual protection for the purposes of universal fault-tolerant quantum logic.

In this work, we establish a lower bound on the fault-tolerant threshold for the 105-qubit universal concatenated code under depolarizing noise. We show that the dual protection coming from the concatenation of two different error correcting codes provides more than just minimal fault-tolerant protection, it serves as a means for logical error suppression at the second level of concatenation (and above). We believe that this provides new insights in the development of quantum error correcting codes, and emphasizes an important principle: to logically protect the quantum gates that are most present in the fault-tolerant architecture.

II. CONCATENATED 105-QUBIT SCHEME

We begin by briefly reviewing the 105-qubit concatenated scheme for universal fault-tolerant logical gates [14]. The logical information is encoded through the concatenation of an outer and inner quantum code, that is each logical qubit of the outer code is in turn en-
code as errors can be spread between codeblocks, the un-
verted logical Hadamard to each of the encoded qubits. In the 105-qubit code is implemented fault-tolerantly by applying each non-fault-tolerant logical Hadamard gate in parallel. (b) Extended rectangle consisting of leading and trailing error correcting circuits implementing the desired logical gate \( G \).

III. FAULT-TOLERANCE THRESHOLD THEOREM

The key property of fault-tolerant architectures is the presence of an asymptotic threshold. For concatenated coding schemes, the asymptotic threshold is the physical error rate \( p_{th} \) such that for physical error rates \( p < p_{th} \) the logical error rate can be made arbitrarily small for sufficiently large number of concatenation levels and the overall time/space resource overhead scales as \( O(poly(\log(A/\epsilon)).A) \), where \( A \) would be the required resources for a noiseless circuit.

All currently known fault-tolerant schemes for quantum logic require active error correction between logical gates. Error correction steps are interleaved between the implementation of various fault-tolerant gates. In this study, fault-tolerant syndrome measurement and error correction is implemented using Steane’s method \[16]\.

At a given concatenation level, each component of the logical circuit (gates and error detection/measurement) will be themselves composed of many operations from the previous level of concatenation. These components include state preparation and measurement, logical gates and memory locations. We consider a depolarizing model for each physical location (level-0) in the circuit. Depolarizing noise is modeled in a similar manner to that of Paetznick and Reichardt in their study of the 23-qubit Golay code \[17\]. Each single qubit gate (including resting qubits) undergoes Pauli noise with probability \( p/4 \) for each Pauli operation, and each two qubit gate undergoes two-qubit Pauli noise with probability \( p/16 \) for each non-trivial two-qubit Pauli. Under this noise, state preparation in the stabilizer \( Z(X) \) basis is flipped from \(|0\rangle \) to \(|+\rangle \) with probability \( p/4 \). Similarly, measurement in the stabilizer \( Z(X) \) basis is flipped with probability \( p/4 \).

As first proposed by Aliferis et al. \[5\] we analyze logical gates by considering the whole as an extended rectangle (exRec), that is the logical gate itself along with its leading (LEC) and trailing (TEC) error correction circuits (see Figure 1(b)). In order to characterize the rate at which logical errors occur, we define malignant error events. Let \( |\psi_1\rangle \) be a single or two-qubit logical state obtained by applying ideal decoders immediately after the LEC circuit and \( |\psi_2\rangle \) the state obtained by applying ideal decoders immediately after the TEC. We define the event \( \text{mal}_E \) as \( |\psi_2\rangle = EU|\psi_1\rangle \) where \( E \) is a single or two-qubit logical Pauli error and \( U \) is the desired gate. We denote the malignant logical error \( E \) present at the output of the circuit by \( \text{mal}_E \). In what follows we will be interested in obtaining estimates of the probability that...
the event $\text{mal}_E$ occurs for the CNOT, Hadamard and $T$ gate.

We use Monte-Carlo sampling in order to determine the probability of each malignant event given an underlying physical depolarizing model. Given $N$ simulations of the logical gate $G$ at a physical error rate $p$, we track the number of malignant faults $a_E(e)$ of each error type $E$, and estimate the probability of a given logical fault as $\Pr[\text{mal}_E(G, p)] = a_E/N$. The estimate of $\Pr[\text{mal}_E|G, p]$ improves as the number of iterations $N$ increases by reducing the standard deviation. Using a least-squares fitting to determine the error probability as a function of input depolarizing error rate, we can determine the pseudo-threshold for each of the logical operations for our error-correcting code. For a level-1 exRec encoding the logical gate $G$, we define the pseudo-threshold as the crossing point $p = p^{(1)}_G(p)$, where $p^{(1)}_G(p) = \sum_{E_i} \Pr[\text{mal}_E(G, p)]$ for all possible logical Pauli errors $E_i$ for a given logical gate $G$. Intuitively, the pseudo-threshold corresponds to the error rate below which the logical error rate at level-1 is guaranteed to be lower than the physical error rate. In all previously studied error correction codes, the pseudo-threshold was conjectured to be an upper bound on the asymptotic threshold [17, 18]. In this work we show that this intuitive bound does not necessarily have to hold and that the asymptotic threshold can be much larger than the pseudo-threshold. To our knowledge this is the first exhibition of this type of logical error behaviour and is fundamentally related to the structure of the underlying 105-qubit error correcting code.

At each location of the level-one exRec, errors are introduced following the depolarizing noise model with noise strength $p$. Since the logical gates in question are fault-tolerant, a logical fault can only occur if a sequence of failures occur at the physical level. Namely, we can upper bound the failure probability for each logical fault $E$ as follows:

\[
\Pr[\text{mal}_E^{(1)}|G, p] \leq \sum_{k=0}^{L_G} c(k)p^k =: \Gamma^{(1)}_G, \tag{1}
\]

where the coefficients $c(k)$ are positive integers that parametrize the number of possible weight-$k$ errors that can lead to a logical fault, $L_G$ is the total number of circuit locations in the logical gate $G$, and $d^*$ characterizes the minimal distance of a given logical gate (that is $\lceil d^*/2 \rceil$ is the minimum weight error that must occur to produce a logical fault). For example in the 105-qubit code, the logical CNOT gate has $d^* = 9$, while the Hadamard and $T$ logical gates have $d^* = 3$ since they sacrifice some of the distance of the code due to the fact that they are not globally transversal. As was shown in [17], the polynomial $\Gamma^{(1)}_G(p)$ is monotone non-decreasing making its construction straightforward with the role of upper bounding the logical error probabilities of all the logical operations $G$ at level-1.

We can then generalize this notion to the level $l$ concatenation level, where each of the physical locations are replaced by logical exRec locations of the $(l - 1)$ level. Taking the worst case error rate for the $(l - 1)$ logical components, the error rate of logical gates at the $l$-th concatenation level can be bounded as follows:

\[
\Pr[\text{mal}_E^{(l)}|G, p] \leq \sum_{k=0}^{L_G} c(k) \left(\Gamma^{(l-1)}_G\right)^k =: \Gamma^{(l)}_G, \tag{2}
\]

where the polynomials given by the coefficients $c(k)$ remain the same as the logical gate is composed of the same operations, just replacing physical locations with logical exRecs from the previous concatenation level.

Finally, we generalize a claim of Ref. [17] required to show the suppression of errors for level-2 and higher concatenation levels when below the fault-tolerance threshold $p_{th}$. Importantly, there exists a $p_{th}$ such that the upper bound on the level-2 logical error probability will be lower than that of level-1, that is $\Gamma^{(2)}_G \leq \epsilon \Gamma^{(1)}_G$, and the following will hold for all concatenation levels $m \geq 2$:

\[
\Pr[\text{mal}_E^{(m)}|G, p] \leq \Gamma^{(m)}_G \leq \epsilon^{\lceil d^*/2 \rceil m - 2 + 1}\Gamma^{(1)}_G, \tag{3}
\]

that is the error rate is exponentially suppressed below the crossing point of $\Gamma^{(1)}_G$ and $\Gamma^{(2)}_G$, thus providing a lower bound for the asymptotic threshold for the logical gate $G$. The proof in full generality is presented in Supplementary Material B.

**IV. CONCATENATED 105-QUBIT THRESHOLDS**

At the level-1 encoding, the logical gate exhibiting the lowest pseudo-threshold is the Hadamard gate $H$. Due to the complexity of the individual logical Hadamard gates arising on each of the 15-qubit codeblocks, many errors propagating from the different individual gate locations could lead to logical faults on that codeblock. The predominant error occurs when two codeblocks contain a logical fault. The logical error that occurs with the highest probability $\Pr[\text{mal}_E|H, p]$ is a logical $X$. This can be understood from the sensitivity of the circuit encoding the Hadamard gate to input $Z$ errors from the LEC which have a high probability of leading to a logical error. If any of the input $Z$ errors land on the target qubit of the CNOT gates in the Hadamard encoding circuit, they will propagate to the physical Hadamard gate on the fourth qubit (see Figure 1(a)) resulting in a logical $X$ error.

Unlike the logical Hadamard, the leading level-1 logical error for both CNOT and $T$ arise from logical $Z$ errors rather than $X$ errors. This stems from the asymmetry in stabilizer generators of the 15-qubit code resulting in an increased protection against $X$ errors. Due to the transversality of the logical CNOT gate in both codes and since there are fewer ways for errors to propagate in
the implementation of the logical $T$, these gates have a better pseudo-threshold relative to logical $H$.

In order to lower bound the level-1 pseudo-threshold, the probability of all logical error types are summed for each of the logical gates and bounded as in Eq. 1. The resulting polynomials are compared to the input physical error rate and their crossing point determines the pseudo-threshold (see Fig. S5 in the Supplementary Material). The resulting values are presented in Table I.

It is important to observe that the CNOT pseudo-threshold is nearly two orders of magnitude larger than the Hadamard pseudo-threshold. Furthermore, all other operations in our circuits (resting qubits, measurement in the $X$ and $Z$ basis and state preparations) are upper bounded by level one polynomials that have larger pseudo-thresholds than CNOT. The dominant set of errors leading to logical faults in the level-1 Hadamard gate is a result of input errors from the LEC as well as failures in the CNOT gates within the 15-qubit Hadamard codeblocks. These components are composed of only memory, CNOT, $X$ and $Z$ basis state preparation and measurement locations. Since the level-1 logical error probability of these gates will be much smaller in the level-2 Hadamard exRec, detrimental faults will be much less likely to occur. Hence, there will be error rates $p$ above the pseudo-threshold $p_{1,H}$ such that the level-2 error polynomials characterizing the logical error rate will be below the level-1 bounding polynomial,

$$\Gamma^{(2)}(p) \leq \Gamma^{(1)}(p), \forall p \leq p_{2,H},$$

where $p_{2,H} > p_{1,H}$. The error rate $p_{2,H}$ is the threshold rate below which all level-2 logical gates have a lower error rate compared to the level-1 logical error rate. As shown in Ref. [17] and argued in the previous section, the value $p_{2,H}$ serves as a lower bound for the asymptotic threshold $p_{th}$.

In previous studies of asymptotic thresholds for the Golay and 7-qubit CSS codes, the CNOT exRec provided a lower bound on the threshold value since it contained the largest amount of locations relative to all the

| Gate          | Pseudo-Threshold | Asymptotic threshold |
|---------------|------------------|----------------------|
| CNOT gate     | $(2.11 \pm 0.02) \times 10^{-3}$ | $(1.95 \pm 0.01) \times 10^{-3}$ |
| $T$ gate      | $(4.89 \pm 0.11) \times 10^{-4}$ | $(1.58 \pm 0.02) \times 10^{-3}$ |
| Hadamard gate | $(4.47 \pm 0.29) \times 10^{-5}$ | $(1.28 \pm 0.02) \times 10^{-3}$ |
| 105-qubit     | $(4.47 \pm 0.29) \times 10^{-5}$ | $(1.28 \pm 0.02) \times 10^{-3}$ |
| 23-qubit Golay| $(1.73) \times 10^{-3}$ | $(1.32) \times 10^{-3}$ |

TABLE I: Lower bounds for the pseudo and asymptotic threshold results for the Hadamard, $T$ gate and CNOT gates. The Hadamard asymptotic-threshold is larger than its pseudo-threshold resulting from the double protection of the CNOT gates as seen by the high CNOT pseudo-threshold. In bold, the overall thresholds for the 105-qubit and 23-qubit codes are compared.

other gates in the universal gate set [5, 17, 19]. Since the CNOT exRec is itself composed entirely of gates that are transversal, as the error rate approaches the pseudo-threshold value, certain malignant events (for example, the probability of getting a logical $ZI$ error at the output of the CNOT circuit, as can be seen in Fig. S3(d)) become more likely to occur than the level-zero probabilities determined from the depolarizing noise model. Recall that the pseudo-threshold was conjectured to be an upper bound on the asymptotic threshold value. However, it is the CNOT locations that are the leading contributors to logical errors. Consequently, the pseudo-threshold of the CNOT gate, as opposed to the $H$ and $T$ gates, will be the limiting factor to the asymptotic threshold. As argued above, this will give rise to reduced logical error rates of the $H$ and $T$ gates at the second level of concatenation, and using Eq. 3, a lower bound for the asymptotic threshold $p_{th}$ can be determined. The plots in Fig. 3 illustrate the level-1 and level-2 polynomials upper bounding the logical error rates at the first and second level for the Hadamard and CNOT gate circuits (see Fig. S5 for the corresponding $T$ gate plots). As expected, the CNOT exRec contains a lower asymptotic thresh-

FIG. 3: Probability of logical error as function of physical error rate for the level-1 and level-2 logical (a) Hadamard and (b) CNOT. The crossing point of the fitted curve allows for the determination of a lower bound for the asymptotic threshold for each of the logical gates. The CNOT gate exhibits a much lower logical error rate than the Hadamard at the first level.
old value given by $(1.95 \pm 0.01) \times 10^{-3}$. The Hadamard exRec limits the threshold value of the 105-qubit code to be $(1.28 \pm 0.02) \times 10^{-3}$. Interestingly, the level-two polynomials satisfy Eq. 3 for error rates nearly 30 times larger than their corresponding level-one polynomials. This is a distinctive feature of the 105-qubit concatenated scheme and clearly demonstrates the impact of having an exRec primarily composed of gates which are transversal in both codes with much larger pseudo-threshold rates. The asymptotic threshold derived for the 105-qubit code compares favourably to the $[[23,1,7]]$ Golay code studied under the same depolarizing error model and metric for gate failures under malignant set counting [17]. This scheme does not require magic state distillation in order to achieve fault-tolerance and may lead to reduced overhead [20]. Determining the resource overhead remains an interesting open problem.

V. CONCLUSION

In this work, we established the first rigorous lower bound on the asymptotic threshold for the concatenated 105-qubit code. We show that the pseudo-threshold value of $(4.47 \pm 0.29) \times 10^{-5}$ arising from the $H$ gate is significantly improved at higher levels of concatenation yielding a lower bound on the asymptotic threshold value of $(1.28 \pm 0.02) \times 10^{-3}$. The increase in asymptotic threshold is primarily due to the relatively high threshold of the logical CNOT gate. We believe that this non-traditional behaviour of logical error probabilities at higher concatenation levels is an interesting property of the studied scheme and points to an interesting direction for future error correction research. Due to the high concentration of CNOT gates for the purposes of error detection, we believe that tailoring codes to correct for logical errors in encoded CNOT gates at the expense of perhaps noisy single qubit gates would allow for higher asymptotic thresholds for concatenated codes.

VI. ACKNOWLEDGEMENTS

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Supplementary Material A: Error type and detailed threshold analysis

In this section we provide a more detailed threshold analysis for the CNOT, $H$ and $T$ gates. Furthermore, we provide details on the contributions from different error types.

![Logical T gate circuit for the 105-qubit concatenated code. The T gate is applied transversally on the 15-qubit codeblocks. A single error at any location in the above circuit can result in a single error on multiple codeblocks which will be corrected at the 15-qubit level. Consequently, the logical T gate circuit is fault-tolerant at the 105-qubit level.](Image)

Fig. S1: Logical $T$ gate circuit for the 105-qubit concatenated code. The $T$ gate is applied transversally on the 15-qubit codeblocks. A single error at any location in the above circuit can result in a single error on multiple codeblocks which will be corrected at the 15-qubit level. Consequently, the logical $T$ gate circuit is fault-tolerant at the 105-qubit level.

Fig. S2: An example of shared EC’s between two consecutive level-one exReCs

1. Error type analysis

In computing the probability of obtaining a logical error $E$ at the second level of concatenation for an error rate $p$ and gate $G$ ($\Pr[\text{mal}_{E}^{(2)} | G, p]$), each level-one exRecs in the level-two circuit was treated as a physical independent location with a redefined noise model given by the polynomials $\Gamma_{G,E}^{(l)}$. For example, a level-one CNOT gate in a level-two simulation would be treated as a physical CNOT gate. A two-qubit Pauli error would be inserted with a probability upper bounded by the polynomials obtained in Eq. 2 with $l = 2$ instead of the probability arising from the depolarizing noise model. To be consistent with Eq. 4, the notation is chosen such that $\Gamma_{G}^{(l)}$ is the upper bounding polynomial at level-$l$ for all error types $E$ whereas $\Gamma_{G,E}^{(l)}$ is the upper bounding polynomial for the particular error type $E$.

As can be seen in Fig. S2, a level-two simulation will typically contain many level-one exReCs with overlapping ECs and so it is not entirely correct to treat them independently. If two level-one exReCs share ECs, then the rectangle that precedes the other one is replaced with a faulty gate only if it is still incorrect after the shared ECs have been removed. As was shown in Ref. [17], we must calculate $S_1$ for both complete and incomplete exReCs where one or more TECs have been removed and take the polynomial that bounds all cases. See Fig. S3(c) for an example. We would also like to point out that for single qubit gates, exRec’s without a TEC always had a lower probability of obtaining a logical fault (for any error type) compared to the case where the TEC was kept. This can be understood from the fact that the TEC adds more locations and hence more ways for errors to be introduced at the output of the circuit.

The polynomials in Fig. S3(d) upper bound the probability of obtaining a logical error at the first level of concatenation of the CNOT exRec. Each curve corresponds to a different error type (error types that are not displayed occur with a probability less than $10^{-7}$ for all sampled physical error rates). Note that the upper bounds on logical $Z$ malignant events are significantly higher than their $X$ counterpart. As mentioned in the
FIG. S3: (c) Polynomials upper bounding the event mal$_Z$ for either the full level-one CNOT exRec or the level-one CNOT exRec with one or both TEC’s removed. The polynomial upper bounding the event mal$_Z$ will upper bound all the curves in the above figure. (d) Polynomials upper bounding the level-one CNOT exRec for the different logical error types.

main text, this is primarily due to the fact that the 15-qubit Reed-Muller code offers better protection against X errors.

The polynomials of Fig. S4(a) upper bound the probability of obtaining a logical X, Z or Y error for the level-one Hadamard exRec. As was explained in section II of the main text, the circuit encoding the logical H on the 15-qubit codeblocks is very sensitive to input Z errors. Any Z error propagating through the target qubit of the CNOT gates (prior to the application of the physical H on qubit 4, see Fig. 1(a)) will result in a logical X error on the 15-qubit codeblock. The latter is the main reason for a larger upper bound on the event mal$_X$ compared to the event mal$_Z$ even though the 15-qubit Reed-Muller code provides better protection against X errors.

2. Threshold analysis

The pseudo-threshold values for a gate G given in Table I were obtained from the crossing point between the physical error rate $p$ and the curves $p^{(1)}_{G}(p) = \sum_{E_i} \Pr[\text{mal}^{E_i}_{G}, p]$ for all possible logical Pauli errors $E_i$. The plots on the left column of Fig. S5 illustrates the crossing point for the logical CNOT, Hadamard and T gate. The CNOT gate has the largest pseudo-threshold value of $(2.11 \pm 0.02) \times 10^{-3}$ due to the double protection from the CSS 7-qubit Steane code and the 15-qubit Reed-Muller code. On the other hand, the Hadamard gate has the lowest pseudo-threshold value of $(4.47 \pm 0.29) \times 10^{-5}$ due to the sensitivity of the encoding circuit on the 15-qubit codeblocks to input Z errors.

Following Eq. 4, a lower bound for the asymptotic threshold value for a particular gate G is given by the intersection between the polynomials upper bounding the probability of obtaining a logical error $E$ at the first and second level of concatenation ($\Gamma^{(1)}_{G,E}$ and $\Gamma^{(2)}_{G,E}$). Note that the error type $E$ in the asymptotic threshold calculation is chosen such that the intersection between $\Gamma^{(1)}_{G,E}$ and $\Gamma^{(2)}_{G,E}$ occurs at the smallest physical error rate.
For the CNOT gate (Fig. S5(b)) this is given by $E = ZI$, for the Hadamard gate (Fig. S5(d)) it is $E = X$ and for the $T$ gate (Fig. S5(f)) it is $E = Z$.

An interesting feature can be observed from the plots on the right column of Fig. S5. Notice that the polynomial upper bounding the logical error rates for higher concatenation levels, the level-two CNOT exRecs in the level-three simulation are more likely to fail than at the previous level (since $\frac{1.95 \pm 0.01}{10^{-3}}$). The reason is that for higher error rates than the asymptotic threshold value, the level-two CNOT exRecs will be noisy enough such that the probability of obtaining a logical fault at the output becomes less likely to fail than the level-one CNOT exRecs (in the level two simulation). Consequently, there is a higher probability of obtaining a logical fault at the output of the CNOT exRec. However, for the logical $H$ and $T$ gate exRecs, $\Gamma_{G,E}^{(3)}(p)$ intersects $\Gamma_{CNOT,ZI}^{(1)}(p)$ at the asymptotic threshold value $(1.95 \pm 0.01) \times 10^{-3}$. The reason is that for higher error rates than the asymptotic threshold value, the level-two CNOT exRecs in the level-three simulation are more likely to fail than the level-one CNOT exRecs (in the level two simulation). Consequently, there is a higher probability of obtaining a logical fault at the output of the CNOT exRec. However, for the logical $H$ and $T$ gate exRecs, $\Gamma_{G,E}^{(3)}(p)$ intersects $\Gamma_{G,H,X}^{(1)}(p)$ at an error rate which is larger than the asymptotic threshold value for these particular gates ($\frac{1.28 \pm 0.02}{10^{-3}}$ for $H$ and $\frac{1.58 \pm 0.01}{10^{-3}}$ for $T$). Consider the logical Hadamard gate (the following argument applies equally well to the $T$ gate). For error rates $p$ that are between the $H$ and CNOT asymptotic threshold values, $\frac{1.28 \pm 0.02}{10^{-3}} \leq p \leq (1.95 \pm 0.01) \times 10^{-3}$, the level-two Hadamard exRecs in the level-three simulation will be more likely to fail than at the previous level of concatenation. However, this will be compensated by all of the level-two CNOT exRecs in the level-three simulation which will be less likely to fail than at the previous level (since $p$ is below the CNOT asymptotic threshold value). Above the error rate where $\Gamma_{H,X}^{(3)}(p)$ intersects $\Gamma_{H,X}^{(1)}(p)$ ($p = 1.44 \times 10^{-3}$), the level-two Hadamard exRecs will be noisy enough such that the probability of obtaining a logical $X$ error will be larger than at the previous level. Therefore, by considering the crossing points of the logical error rates for higher concatenation levels, a lower lower-bound for the asymptotic threshold can be established. However, in order to fairly compare the performance of the concatenated scheme with the Golay code [17], we emphasized the lower bound obtained from the crossing point of the first and second concatenation levels.

**Supplementary Material B: Lower bound on asymptotic threshold**

We review how we arrived at Eq. 3 and how this result leads to a lower bound on the asymptotic threshold for the code in question. We prove a more general result for the exponential suppression of error rates as a function of concatenation levels given the presence of a crossing point of the upper bounding polynomials of the error rate at consecutive concatenation levels.

**Lemma 1.** Suppose the error rate of a logical gate $G$ at the $l$-th concatenation level can be upper bounded as follows:

$$Pr[\text{fail}]_E \leq \Gamma_G^{(l)} = \sum_{k=\lceil \frac{d^*}{2} \rceil}^{L_G} c(k) \left( \Gamma_G^{(l-1)} \right)^k.$$ (S2)

If the upper bounding error polynomial satisfies the following $\Gamma^{(l)} \leq \epsilon \Gamma^{(l-1)}$ for $0 \leq \epsilon \leq 1$, then the following holds:

$$Pr[\text{fail}]_E \leq \epsilon \Gamma^{(m)} \leq \sum_{r=0}^{m_0-\left\lceil \frac{d^*}{2} \right\rceil} \epsilon^{r} \Gamma^{(l-1)}_G,$$ (S3)

where $m > l$, and $d^*$ is the minimal distance of the encoded state throughout the logical application of the gate $G$.

**Proof.** We shall show this result by induction. Therefore, consider first the case of $m = l + 1$. By definition $Pr[\text{fail}]_E^{(l+1)} \leq \Gamma^{(l+1)}_G$, for all logical errors $E$. In order to show the right side of the inequality given in Eq. S3 consider the expansion of $\Gamma^{(l+1)}_G$ as a sum over failures of the gates at the $(l)$-th level, and use the claim that $\Gamma^{(l)}_G \leq \epsilon \Gamma^{(l-1)}_G$.

$$\Gamma^{(l+1)}_G = \sum_{k} c(k) \left( \Gamma_G^{(l)} \right)^k \leq \sum_{k} c(k) \left( \epsilon \Gamma_G^{(l-1)} \right)^k = \epsilon^{\lceil \frac{d^*}{2} \rceil} \sum_{k} c(k) \left( \epsilon \Gamma_G^{(l-1)} \right)^k \leq \epsilon^{\lceil \frac{d^*}{2} \rceil} \sum_{k} c(k) \left( \Gamma_G^{(l-1)} \right)^k = \epsilon^{\lceil \frac{d^*}{2} \rceil} \Gamma_G^{(l)} \leq \epsilon^{\lceil \frac{d^*}{2} \rceil} \Gamma_G^{(l-1)}.$$ (S3)

We used the fact that all of the $c(k)$ coefficients in the expansion are positive due to the fault-tolerance of the logical gates, errors of order smaller than $\lceil \frac{d^*}{2} \rceil$ are correctable and therefore $c(k) = 0 \forall k < \lceil \frac{d^*}{2} \rceil$.

To complete the proof, we assume the induction hypothesis for level $m$ and show for level $(m + 1)$:

$$\Gamma^{(m+1)}_G = \sum_{k} c(k) \left( \Gamma_G^{(m)} \right)^k \leq \sum_{k} c(k) \left( \epsilon^{m_0-\left\lceil \frac{d^*}{2} \right\rceil \Gamma_G^{(l-1)} \right)^k \leq \epsilon^{m_0-\left\lceil \frac{d^*}{2} \right\rceil} \sum_{k} c(k) \left( \Gamma_G^{(l-1)} \right)^k = \epsilon^{m_0-\left\lceil \frac{d^*}{2} \right\rceil} \sum_{k} c(k) \left( \Gamma_G^{(l-1)} \right)^k = \epsilon^{m_0-\left\lceil \frac{d^*}{2} \right\rceil} \Gamma_G^{(l)} \leq \epsilon^{m_0-\left\lceil \frac{d^*}{2} \right\rceil} \Gamma_G^{(l-1)},$$ (S3)

thus completing the induction proof. \(\square\)
It should be noted that the shift in the crossing point for different concatenation levels in the logical $H$ and $T$ gate (Figs. S5(d) and S5(f)) may at first glance violate the assumption that the polynomial coefficients $c(k)$ are the same at all levels. However, one of the assumptions of the polynomials were that the logical error rate of all locations at the previous level have the same error rate, and thus contribute equally in a potential error chain.

The fact that CNOT is in fact less noisy than other gates in the regime between the $H$ (and $T$) pseudo-threshold and asymptotic CNOT threshold means that certain error chains are further suppressed and as such the logical error rate is lower than the worst case bound set by the polynomials. The CNOT crossing points (Fig. S5(b)) are uniform across all levels, indicating that the true logical error rate is very close to the worst-case bound.
FIG. S5: The plots on the left column illustrate the probability of logical error as function of physical error rate for logical (a) CNOT, (c) Hadamard and (e) $T$ gate. The crossing point of the fitted curve allows for the determination of the level-1 pseudo-threshold for each of the logical gates. The CNOT pseudo-threshold is the largest among all three gates due to the double protection of the 7-qubit and 15-qubit code. The plots on the right column illustrate the polynomials upper bounding the probability of obtaining a logical error $E$ for the first, second and third level of concatenation. The crossing point between the level-one and level-two polynomials determine the asymptotic threshold for the gate under consideration. For the logical CNOT gate (b), it is the event $\text{mal}_Z$ which limits the threshold value. For the logical gate $H$ (d), $\text{mal}_X$ limits the threshold value. Lastly, for the logical $T$ gate (f), $\text{mal}_Z$ limits the threshold value.