PIRM: Processing In Racetrack Memories

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Abstract—The growth in data needs of modern applications has created significant challenges for modern systems leading a “memory wall.” Spintronic Domain-Wall Memory (DWM), related to Spin-Transfer Torque Memory (STT-MRAM), provides near-SRAM read/write performance, energy savings and non-volatility, potential for extremely high storage density, and does not have significant endurance limitations. However, DWM’s benefits cannot address data access latency and throughput limitations of memory bus bandwidth. We propose PIRM, a DWM-based in-memory computing solution that leverages the properties of DWM nanowires and allows them to serve as polymorphic gates. While normally DWM is accessed by applying spin polarized currents orthogonal to the nanowire at access points to read individual bits, transverse access along the DWM nanowire allows the differentiation of the aggregate resistance of multiple bits in the nanowire, akin to a multi-level cell. PIRM leverages this transverse reading to directly provide bulk-bitwise logic of multiple adjacent operands in the nanowire, simultaneously. Based on this in-memory logic, PIRM provides a technique to conduct multi-operand addition and two operand multiplication using transverse access. PIRM provides a 1.6× speedup compared to the leading DRAM PIM technique for query applications that leverage bulk bitwise operations. Compared to the leading PIM technique for DWM, PIRM improves performance by 6.9×, 2.3× and energy by 5.5×, 3.4× for 8-bit addition and multiplication, respectively. For arithmetic heavy benchmarks, PIRM reduces access latency by 2.1×, while decreasing energy consumption by 25.2× for a reasonable 10% area overhead versus non-PIM DWM.

I. INTRODUCTION

The growth in data needs of modern applications in the “big data” era has created significant challenges for modern systems. While considerable effort has been undertaken to improve memory storage density and energy consumption—through deeply scaled memories and tiered memories that include non-volatile memory—the fundamental data access latency and throughput have not kept pace with application needs. This is commonly referred to as the “memory wall” [1], [2], as it limits potential performance of memory bound applications due to the limited bandwidth of the bus between memory and processor. Additionally, moving data on this bus has been proven to consume a disproportionately large amount of energy, especially for programs which require large working sets. For example, adding two 32-bit words in the Intel Xeon X5670 consumes 11× less energy than transferring a single byte from the memory to the processor [3].

Processing-in-memory (PIM) [4]–[8] and near data processing (NDP) [9], [10] solutions promise to reduce the demands on the memory bus and can be a solution to efficiently realizing the benefit of increasingly dense memory from deep scaling and tiered memory solutions. However, leading solutions for bulk-bitwise PIM in DRAM [4], [5] are limited to two operand operations. Multi-operand bulk-bitwise PIM [6] has been proposed for Phase Change Memory (PCM), a leading commercial candidate in the tiered memory space. However, its endurance challenges (circa 10^8 writes [11]) and relatively high write energy (up to 29.7pJ per bit [12]) raise concerns about its effectiveness when used for PIM. It is also popular to use the analog characteristics of, particularly memristor-based, crossbar arrays to accelerate neural networks [13], [14] but these techniques can also lead to endurance as well as fidelity concerns. Spin-transfer torque magnetic random-access memory (STT-MRAM) has been proposed for caches due to its SRAM-class access latency, non-volatility, favorable energy, and no appreciable endurance limitation. STT-MRAM has also been proposed for PIM [15]. Unfortunately, STT-MRAM suffers from insufficient density to be competitive for main memories.

Spintronic Domain-Wall Memory (DWM), often referred to as Racetrack Memory [16], leverages the positive proprieties of STT-MRAM while dramatically improving the density by converting individual bits into multi-bit nanowires making it an appropriate choice for both main-memory integration and PIM. Two existing techniques propose using DWM for PIM with a goal of accelerating Convolutional Neural Network (CNN) applications. The first, abbreviated DW-NN for Domain-Wall Neural Network, leverages “giant magnetoresistance” to join a domain of adjacent nanowires through a shared fixed layer. This creates a shared access port that can be used to implement two operand XOR logic. They also include a special sensing circuit between three nanowires used to compute a carry in order to create a ripple carry adder [7]. Another, combines DWM with skyrmion logic to implement PIM, particularly addition and multiplication [8], which we refer to as SPIM.

Our paper proposes PIRM, or Processing In Racetrack Memories. PIRM achieves multi-operand bulk-bitwise and addition PIM operations that can far outperform current DWM architectures for DRAM, PCM, and DWM. Our approach treats the DWM nanowire as a polymorphic gate using a transverse read [7] (TR), a method to access the nanowire and count the number of ones across multiple domains. Using this one counts we can directly implement Racetracks that are optimized for computing arbitrary logic functions, sum, and carry logic output. Presuming a sensing circuit that can distinguish data among seven domains. PIRM is able to directly compute seven operand bulk-bitwise operations and five-operand addition. Multi-operand addition is particularly important to efficiently implement multiplication. PIRM uses this building block to create specialized PIM-enabled domain-block clusters (DBCs). These DBCs are interleaved throughout memory tiles to create the facility for massively parallel PIM in the PIRM main memory. We show that the combined
speedup of our multiplication procedure and the ability to process multiple operands significantly mitigates the memory wall and enables more sophisticated general PIM than prior work. Specifically, the contributions of this paper are:

- We present a novel technique to utilize a segment of DWM nanowire as a polymorphic gate, including the required sensing and logic circuitry.
- We present the first technique, to our knowledge, to perform multi-operand logic and addition operations in DWM using this polymorphic gate. We further extend this with shifting to implement efficient multiplication.
- We describe a PIM-enabled domain-block cluster architecture built from the PIM-enabled DWM.
- We propose a technique called Transverse Write (TW) to write and shift a segment of the nanowire in a single operation.
- We provide a detailed analysis of PIRM compared to state-of-the-art approaches in terms of energy, performance, and area.

PIRM is effective for myriad applications such as database searching that requires multi-operand bulk bitwise computation and convolution-based machine learning that leverages arithmetic operations.

The remainder of this paper is organized as follows. In Section II, we present the necessary background on Racetrack memory, its architecture, previous PIM techniques and TR. Next, Section III presents the basic concepts of PIRM, alongside our modified SA and supporting circuitry. Furthermore, this section presents several approaches to perform smart multiplication with a concrete example. In Section IV, we present the setup of our experiments to compare with state-of-the-art approaches in terms of energy, performance, and area.

II. BACKGROUND AND RELATED WORK

In this section, we first introduce the fundamentals of DWM, how it functions, and our assumed memory architecture based on prior work. We then discuss previous PIM work for both DWM and other memories. Finally, we describe details of TR and how it enables our PIM approach.

A. Domain-wall Memory Fundamentals

![Fig. 1: Anatomy of a DWM nanowire.](image)

DWM is a spintronic non-volatile memory made of ferromagnetic nanowires. DWM nanowires consist of many magnetic domains separated by domain walls (DWs) as shown in Fig. 1. Each domain has its own magnetization direction based on either in-plane (+X/-X) or perpendicular (+Z/-Z) magnetic anisotropy (IMA/PMA). Binary values are represented by the magnetization direction of each domain, either parallel/antiparallel to a fixed reference. For a planar nanowire, several domains share one/few access point(s) for read and write operations [18]. DW motion is controlled by applying a short current pulse laterally along the nanowire governed by SL. Since storage elements and access devices do not have a one-to-one correspondence, a random access requires two steps to complete: (1) shift the target domain and align it to an access port and (2) apply an appropriate voltage/current like in STT-MRAM to read or write the target bit.

The blue domains are dedicated for the actual data stored in memory. The grey domains are extra-domains used to prevent data loss while shifting data into the nanowire towards the extremities. The dark blue elements are the read or read/write ports. Fig. 1 contains a read-only port that has a fixed magnetic layer, indicated in dark blue, which can be read using RWL. The read/write port is shown using shift-based writing [19] where WWL is opened and the direction of current flows between BL and BL, and reading conducted from BL through the fin and up through RWL to GND.

To align a domain with an access port, a current needs to be sent from one extremity of the nanowire, shifting each domain. This inherent behavior of DWM can be imprecise, generating what is known as a “shifting fault” in the literature. Several solutions have been proposed to mitigate this fault mode [20–22].

B. Memory Designs with DWM

To employ DWM as main memory, we propose to use a similar architecture that has been previously proposed in the literature for emerging technologies (including DWM). This architecture maintains the same I/O interface as a traditional DRAM memory hierarchy to simplify adoption of a new technology. Thus, this architecture preserves the bank and subarray organization as shown in Fig. 2(a) and the tile size [23] as shown in Fig. 2(b). This also allows for data movement within the memory such as inter-bank copying that is described in previous work [24]. Fig. 2(c) shows a DWM subarray broken down into tiles, which share the same global wordlines. To facilitate DWM integration we divide tiles into domain block clusters. Each DBC shares the same local sensing circuitry and write driver as described for other main memory architectures using non-volatile memory [25].

Each DBC, expanded and turned 90° so that the nanowires are shown horizontally in Fig. 2(d) consists of X parallel racetracks composed of Y data domains. Thus, X represents the number of bits that can be accessed simultaneously. We show a typical example where X = 512. Y represents the distinct row addresses contained within the DBC. Y is limited as the necessary current required for successful shifting increases with the number of domains. Moreover, larger values of Y introduce increasingly large access delay due to the longer average travel distance. We show a typical example of
This architecture allows $32 \leq Y \leq 512$, which allows sufficient scaling for longer nanowires.

While, a single access point is necessary for each nanowire in the DBC, adding heads can reduce the delay by reducing the shift distance between accesses [26]. We show two heads in the example, which would traditionally divide the nanowire length into equal sections to minimize shift latency and reduce the number of overhead domains required. In addition, a second access port can also enable the polymorphic gate capability of the nanowire if placed sufficiently close to allow transverse access. We discuss this further in Section II-D. However, first we review prior work in PIM in the next section.

C. Processing in Memory

In this sub-section, we first present the state of the art bulk-bitwise operations in DRAM, followed by related works proposed for PIM in DWM.

1) PIM with bulk-bitwise operations in DRAM and PCM:

There have been two major proposals to conduct bulk-bitwise processing directly in DRAM. Bulk-bitwise logic combines two rows “bitwise” with the same logic operation such that $c_i = a_i \oplus b_i$. Ambit proposed to open three DRAM rows simultaneously and compare the combined voltage to the sensing threshold, i.e., $\frac{V_{DD}}{2}$. A majority of ‘1’s results in $\geq \frac{V_{DD}}{2}$ which would drive the senseamp (SA) to $V_{DD}$.

A minority of ‘1’s results in $\leq \frac{V_{DD}}{2}$ driving the SA to $V_{CC}$. Thus, to compute an \text{AND} the third row is used as a control row set to ‘0’ so that both data rows must contain ‘1’s for the result to be ‘1.’ \text{OR} is computed setting the control row to ‘1’ requiring only one data row to be ‘1.’ This process is destructive, as all three rows now contain the result of the logical operation.

Ambit uses a technique called RowClone [24] which essentially opens the source row, waits for the SA to refresh the row and then opens the destination row which is overridden by the SA just as happens in a write. Thus, operands are duplicated in a safe location to conduct the logic operation without destroying the orginal data. To create a complete logic set a dual-contact cell (DCC) concept is employed allowing a cell to be read as the inverted value through \text{EL}. A DCC row requires the same overhead as two regular rows. To execute $A \oplus B$ they leverage these DCC rows to first compute $k = A$ \text{AND} $B$, followed by $k' = A$ \text{AND} $B$, and finally $k \lor k'$.

ELP\textsuperscript{IM} improves on Ambit by directly performing logic operations without moving the data. Instead, the technique changes the pseudo-precharge state of the SA to replace the control row [4]. The process requires multiple comparisons to ultimately determine the final logic value, but avoids the need for cloning rows. They demonstrate a 3.2× performance improvement over Ambit as well as recent near-data processing approaches [9] for bitmap and table scan applications.
Pinatubo is a PIM technique for PCM that resembles aspects of Ambit and ELP\textsuperscript{2}IM. Like Ambit, it opens the two rows for comparison simultaneously, and like ELP\textsuperscript{2}IM it adjusts the sensing circuitry to conduct different operations \cite{7}. For example, changing the $V_{TH}$ to $< V_{TH}/2$ allows an OR operation and $> V_{TH}/2$ allows an AND operation.

Ambit, ELP\textsuperscript{2}IM, and Pinatubo insomuch as they are complete logic sets are capable of computing more complex arithmetic operations. More complex logic requires sequential steps to determine the result similar to the XOR example described for Ambit. Next we discuss PIM for DWM.

2) PIM in DWM: DW-NN creates a PIM processing element with dedicated circuitry to support current passing through two stacked domains at once. This allows measurement of the aggregate giant magnetoresistance (GMR) across the stacked domains \cite{7}. This computes XOR which is ‘0’ if the data is parallel and ‘1’ if the data is anti-parallel. To conduct addition, operand bits are stored in consecutive bits within a single nanowire. The XOR operation is used in combination with a pre-charge sensing amplifier (PCSA) that can compute a function of data from three nanowires’ access port—sum $S$ is the result of the two consecutive XORS, and $C_{OUT}$ is the result of the comparison of PCSA($A, B, C_{IN}$) $>$ PCSA($\bar{A}, \bar{B}, C_{IN}$). Both operations are bitwise serial since they must be shifted into alignment with the GMR/MTJs. Because operands are stored within a single nanowire, multiplication is possible using addition of shifted versions of one operand. Compared to accessing data and using a general purpose processor for computation, DW-NN claims an energy improvement of 92$\times$ and a throughput improvement of 11.6$\times$ for an image processing application.

SPIM extends DWM storage with dedicated skyrmion-based computing units \cite{8}. Within these units, custom ferromagnetic domains are physically linked together with channels that support OR and AND operations. By permanently merging many such domains and channels, full adder circuits are formed to perform addition and multiplication. SPIM demonstrates 8-bit addition and multiplication and reports being two times faster, while decreasing energy and area by 42% and 17%, respectively compared to DW-NN. Savings are achieved by parallel bulk-bitwise ops not possible in DW-NN and reduced area compared to a similar ALU/MTJ with CMOS.

DW-NN is capable of XOR addition, and multiplication, but is bit-serial and cannot compute other logic functions. SPIM improves on DW-NN with skyrmion logic units, but with more complex dedicated hardware and a more restrictive set of operations. SPIM provides a new method to do PIM in DWM that can achieve a superset of all the instructions proposed among these various methods while increasing the parallelism and efficiency. To accomplish this, SPIM leverages the transverse read operation discussed next.

D. Transverse read

TR was recently proposed \cite{17} and leveraged to improve reliability via detection and correction of over/under-shifting faults \cite{20}. TR is akin to using a portion of a DWM nanowire as a multi-level STT-MRAM cell. Specifically, the idea is to read an aggregate function of several domains at once along the nanowire. The output of a TR provides the number of ones stored between two heads or one head and an extremity, but without information about their positions. As the number of domains in the TR increases, the minimum sense margin decreases which creates a limit on the number of domains that can be included in a TR. We refer to this as the maximum TR distance or simply TRD.

Fig. 3 presents a segmented TR that can be used to query the full nanowire in the case that distance from the extremity to the access point is larger than the TRD. Each colored arrow represents the path taken by the current used to perform the TR. For instance, to perform a TR on the middle four domains (purple arrow), the transistors M1, M2 and M4 are open and M3 is closed, thus when a current is sent from SL1, it has to go through the four middle domains and exit through M3.

The two red and blue arrows indicate TR over regions with the same color can occur simultaneously. For the red arrows, M2, M3 and SLB transistors are open while M1 and M4 are closed. The current sent from SL and BL2 will flow to M1 and M4, respectively, reading two and one ‘1’s as output, respectively. Due to the larger nanowire resistivity between BL0 and BL2, the leakage current is small enough that the TR can safely be parallelized.

In the next section, we present how the TR can be used to perform logical and arithmetic operations, forming the foundation of PIRM.

III. PIRM

In this section, we discuss the PIRM architecture; this includes (i) modifications to the sensing circuit leveraging TR to realize multi-operand PIM, and (ii) the algorithms to achieve multi-operand addition and two-operand multiplication.

A. PIRM Architecture

We propose to add PIM capability to a portion of the DBCs in the memory architecture, see Fig. 2(c). The number of PIM enabled DBCs can be tuned based on the overhead and the desired PIM parallelism. The detailed DBC shown in Fig. 2(d) shows two access points. In PIRM, these access points are spaced according to the TRD. While TR has been demonstrated for a conservative TRD = 4 \cite{17}, our experiments using the LLG magnetic simulator \cite{28} and the resulting resistance levels indicate that TR can be scaled to a TRD = 7 by increasing the sensing current. This yields eight resistance levels which can be encoded by three bits. We will see how TRD = 7 is particularly effective for addition.
TRD = 7, while optimistic, is significantly more realistic than the presumed TRD = 32 assumed in prior work [20].

Assuming the distinct row addresses contained within the DBC $Y = 32$ as discussed in Section II-B and with a single access point, this nanowire would require 63 domains ($2Y - 1$) to permit shifting data at the extremities to the access point. Normally, adding a second access point would place ports at positions 9 and 25, reducing the number of overhead domains from 31 to 16. To enable TR with a TRD = 7, the ports would move to positions 14 and 20 and the overhead domains would only reduce from 31 to 25. Adding ports in this way provides some reduction of average shift distance while allowing for the TR operation. For two ports to remain at their optimal shift reduction position would not realistically allow a TR between them, because their distance would be 14 domains. Our experiments did not support a such a TRD = 14 at this time to be feasible.

For a tile with the additional access port to conduct TR, we modify the sensing circuitry as shown in Fig. 4(a) where the tan blocks show the added elements. To ensure performing TR requires each SA$_i$ to output seven level bit values such that SA$_i$(j) is ‘1’ if there are ≥ j ‘1’s in the TR and j ∈ 1..7. The extension with additional sensing circuitry is represented by a hashed tan block. These SA outputs become the seven inputs for the PIM unit described in Fig. 4(b). The PIM logic output is selected from a multiplexer. Note, the $i$th multiplexer selects some values provided by the local PIM block and some that come from $(i-1)$st and $(i-2)$nd PIM blocks. We will explain the purpose for the color coding and these connections in the following sections.

There is a direct read from the SA shown in orange that bypasses the PIM logic and the selector to a single two-way mux that feeds the read port. Thus, each direct read or result of PIM logic can be directly forwarded via a hierarchical row-buffer structure to the memory controller and returned to the processor. The capability is also added that PIM output can be written back to the memory block so an additional selector multiplexes the PIM logic with the write port input. As in previous work [5], [6], [24], given the hierarchical row buffer in the memory, the shared row buffer in the subarray or across subarrays can be used to move data from non-PIM DBCs to PIM-enabled DBCs.

C. PIRM Multi-Operand Addition

Based on the bulk-bitwise operations from the previous section, we show an example addition operation for five operands in Fig. 6. In step ①, referencing Fig. 4(a) a TR of $dwm_0$ (first nanowire) is conducted, evaluating $bit_0$ of all operands. $S_0$, which is XOR of $a_0...a_0$, computed by the PIM block and is among the five blue bits. Simultaneously, carry, $C_0$, is computed and sent to the right to the driver for $dwm_1$ shown in red and super carry, $C'_0$, is sent to the driver for $dwm_2$, shown in green in Fig. 4(a) and computed using the logic functions shown in Fig. 4(b). $S_0, C_0, C'_0$ are written into the left access port (port$L$) of $dwm_0$, the right access port (port$R$) of $dwm_1$, and port$L$ of $dwm_2$ simultaneously. In step ②, a similar set of steps occurs except the operations include $C_0$ in addition to $a_1...a_1$. Then, in step ③ TR is conducted over $C'_0, a_2...a_2, C_1$, seven total elements. In the general case, for step $k + 1$ (i.e., $dwm_k$), TR is conducted over $C'_{k-2}, a_k...a_k, C_{k-1}$ with $S_k$ written to port$L$ of $dwm_k, C_k$ written to port$R$ of $dwm_{k+1}$ and $C'_{k}$ written to port$L$ of $dwm_{k+2}$. The control for this operation is a simple counter circuit that provides selectors values for a window of three nanowires and activates the bit lines for $k...k + 2$.

Because the carry chain requires keeping the port$L$ and port$R$ clear to write $C, C'$, for a TRD = 7 we can compute a maximum of five-operand addition. While it may be possible in the future to increase TRD ≥ 8, we explore a technique to efficiently add more than five operands in the context of PIRM multiplication, which we discuss in detail next.
D. PIRM Multiplication

The capability to compute addition in memory, as described in the previous section, provides the foundation for multiple ways to conduct multiplication. A particularly naïve method to compute \( A \times B \) is to add \( A \times B \) times. For example, \( 3A \) can be computed as \( A + A + A \). Thus, we can perform a multiplication by doing several additions. This method can quickly exceed the capacity of a single multi-operand add. Consider \( 9A \), this can be computed by computing \( 5A \) in one step, and then computing \( 5A + A + A + A \). While this method could be improved by generating \( 5A \) in one addition step, then replicating \( 5A \) to generate \( 25A \), and so on, this method is clearly inefficient. One method to accelerate this process is to shift the copies of \( A \) to more quickly achieve the precise partial products that, when summed, produce the desired product.

In Fig. 4(a) we show how data read from bit \( i \) is forwarded to bit \( i+1 \) using the brown lines. These lines originate from the same place as the orange lines from \( i \) but are shown coming from the opposite side of the SA for reduced clutter in the figure. This connection allows a logical left shift which is equivalent to a multiply by 2 or \( A' \). To logically shift by more than one position, we first write \( A' \) and then shift and write \( A'' \) or \( A \ll 2 \). It is important to distinguish between these logical shifts being discussed, which move bits between nanowires and DW shifts, which shift the nanowires to access different data locations. Looking at Fig. 6 logical shifts occur in the Y direction and require the multiplexing logic from Fig. 4(a) and DW shifts move in the X direction. So, to write \( A \ll k \) requires \( k \) shifted read (brown arrows) and write operations. However to write \( A \ll k \) next to \( A \ll k+1 \) requires \( k \) shifted read and followed write steps, an additional shifted read, a DW shift, followed by a write. Thus, to write \( y \) shifted copies with a max logical distance of \( x \) requires \( x-1 \) shifted read/write operations and \( y \) DW shifts. Based on the logical shifting capabilities we describe techniques to leverage PIRM to conduct efficient multiplication in different situations.

1) Constant Multiplication: When one of the operands of the multiplication operation is known, there are sev-
eral ways to efficiently take advantage of PIRM to complete multiplication leveraging shifting. At compilation time, a method based on Booth multiplication is possible [29], [30] where numbers can be represented using 0, N, and \( \mathcal{P} \), which represent 0, -1, and 1, respectively. For example, consider a constant multiplier 20061 → “100111001011101,” this can be encoded as \( \text{POPOPOPOPOONOP} \). It can be decomposed using the pattern \( \text{POOOOOOPOOOOONONOP} \), which corresponds to 515, in positive and negative forms shifted by different amounts: \( \text{POOOOOOPOOOOONONOP} = \text{POPOPOPOPOONOP} \).

Thus, 20061 times \( A \) can be computed in two addition steps: ① \( A \ll 9 + A \ll 1 + A \rightarrow 512A + 2A + A = 515A \), ② \( 515A \ll 5 - 515A + A \ll 12 \rightarrow 16480A - 515A + 4096A = 20061A \). Note \( 515A \) can be computed by generating \( 515A + 1 \) making the last step \( 515A \ll 5 + 515A + 1 + A \ll 12 \) which is still one addition step. This is a significant improvement over adding 20061 copies of \( A \).

2) Arbitrary Multiplication: A more generic method that can also work for arbitrary multiplications is to use the ‘1’s in the multiplier to denote which shifted copies of the multiplier to be summed to create the product. In the 20061 example, there are 9 ‘1’s in the binary form of 20061. Thus, the method to directly compute the product is logically shift \( A \) \( n \) times where \( n \) is the bit-width of the multiplier \( B \). When \( b_i = ‘1’ \) then we also shift the nanowire to retain that “partial product.” When five partial products have been retained, we generate the sum. In this example in step ① \( T = A + A \ll 2 + A \ll 3 + A \ll 4 + A \ll 6 \), and in step ② product \( P = T + A \ll 9 + A \ll 10 + A \ll 11 + A \ll 14 \). Again, this takes only two addition steps. In the worst case, this takes \( \frac{n}{\text{TRD}} \) \( n \) steps or \( O(n^2) \) complexity where \( n \) is the bit-width of the operands.

3) Optimized Multiplication: In the prior methods, we required several addition steps to generate the final result and each addition is still performed sequentially. Using the partial products methodology the complexity remains \( O(n^2) \) in the bit-width. To improve on this we can borrow from Carry Save Adders (CSAs). A CSA leverages the three inputs of a full adder \( A, B, C_{IN} \) to be used for three operands \( X, Y, Z \) instead of two. This creates an entirely parallel process to reduce three operands to two in the form of \( S^\dagger, C^\dagger \). Then a traditional addition using a ripple carry adder can add \( S^\dagger + C^\dagger \rightarrow S \). We can leverage our polymorphic gates in the same way but with more input operands where seven partial products can be reduced to a \( S, C, C' \) in parallel yielding a 7 \( \rightarrow 3 \) operand reduction function.

This method accomplishes two things. The need for the sequential carry logic of addition is not required for the reduction step and the technique can directly be performed on TRD instead of TRD \( \rightarrow 2 \) operands. Furthermore, the 7 \( \rightarrow 3 \) reduction operation can be repeated on data, including prior output of this reduction function in a previous step. These reductions are continued until there are \( \leq \text{TRD} - 2 \) operands remaining. The final result can then be computed with a single addition operation, where one output is generated by TRD-2 inputs. For 32-bit multiplication in the worst case this would require \( n - 1 \) logical shifts, seven \( 7 \rightarrow 3 \) transformations, and one add that requires \( n \) steps. This makes multiply an \( O(n) \) operation.

The power of this approach is that the number and latency of \( 7 \rightarrow 3 \) transformations is much less than the latency of the add operation. Thus, given the width of the data stored in the DBC as 512, we can pack 32-bit multiply operations into the row width and gain parallelism while retaining simple control that allows the multiply to execute while only blocking a single subarray, allowing other subarrays to proceed in parallel. This general multiplication leveraging CSA inspired 7 \( \rightarrow 3 \) reduction of multiple packed \( w \)-bit words per \( n \)-bit row is specified in Algorithm 1. Note, as multiplication increases a \( 2w \)-bit wide product, we pack \( w \)-bit wide words with \( w \)-bit wide gaps to store for the full product.

First, one operand is copied across banks to a processing tile as described in prior work [2]. Once \( A \) is in the 0th position of a DBC, the first loop shifts and writes the row \( w \) times in adjacent domains. Then we precharge the write driver to “0..0” and bring the B row into the rowbuffer. Next, we shift back along the DBC and zero out the \( ith \) shifted version of \( A \) if that bit of \( B \) is ‘0’. We do this for each of the packed words in the row independently. This is the only portion of the control that differs based on the different words and it functions like predicated execution. We have now returned to the origin and start to use PIM to compute \( S, C, C' \) over the

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**Algorithm 1: Parallel Multiplication**

**Data:** Two rows \( A \) and \( B \) of size \( n \) with word of size \( w \)

**Result:** \( S = A \times B \)

```
begin
    Inter-bank-copy(A) \rightarrow 0th position of target DBC
    for \( i \in 0..w - 1 \) do
        Read-shifted
        Write
        DW Shift right
    \end

    Precharge write driver to “0..0”
    Inter-bank-copy(B) \rightarrow local-row-buffer
    for \( i \in w - 1..0 \) do
        for \( j \in 0..n/2w - 1 \) do
            if \( b_j \rightarrow 2w + i = 0 \) then
                write \( b_j \rightarrow 2w + i \rightarrow (j+1)2w - 1 \)
            end
        \end
        DW Shift left
    \end

    for \( i \in w - 1..0, i+ = \text{TRD} \) do
        Compute \( S, C \) and \( C' \)
        Shift DBC + TRD
        Write \( S, C, C' \) in DBC'
        Shift DBC' + 3
    \end

    Compute \( S, C, C' \) from DBC' \rightarrow DBC
    Continue until \( \leq \text{TRD - 2} \) elements
    Add to compute final result
end
```
TRD and write this into another DBC or DBC’. The remaining partial products from DBC are converted into $S, C, C'$ in DBC'. Then DBC’ is traversed writing the newly computed $S, C, C'$ back to the original DBC. This continues until there are $\leq$ TRD – 2 elements, which triggers an add to compute the final result. There are a few minor optimizations to this flow that can minimize cycles and steps, such as interleaving shifted versions of A across two DBCs in groups of size TRD which can overlap shifting and computing. Also for fixed size $w, n, TRD$, the exact steps can be optimized.

Another possible optimization for large addition is to increase TRD, consequently the number of operands per operation. For $8 \leq$ TRD $\leq$ 15, in addition to $S, C, C'$, PIRM could generate $C''$ that would impact the bitline+3.

IV. CASE STUDY: IMPLEMENTING A CNN

To demonstrate the potential of PIRM we explore the process of computing a convolutional neural network (CNN) using PIM. The CNN approach is composed of 3 main types of layers: convolution layers, pooling layers and fully connected layers, each of which can be complete in PIRM.

A. Convolution

The convolution layer is the process of taking a small kernel (or weight) matrix $K$, and combining it in “windows” with a larger matrix $I$ representing input features, at each step multiplying the overlapping positions and summing the results. As an example, for $I$ and $K$ of size $NxN$ and $3x3$, respectively, the convolution operation is:

$$\text{Conv}(I, K)(m, p) = \sum_{j=0}^{2} \sum_{t=0}^{2} K_{j,t} * I_{m+j-1,p+t-1}$$  \hspace{1cm} (1)$$

Using PIRM, we show the convolution flow in Fig. 7. First the multiplications are completed by operating in parallel with multiple copies of the weight window and executed on multiple items packed into rows in parallel. The multiplication approach in Section III-D3 generates $S, C, C'$ in parallel and summed with the 5-operand add as described in Section III-C. This generates the pointwise multiplication results. These results are then reduced over summation first across the columns, then those results are summed across the rows by shifting them into alignment to generate the output features. For larger kernels, PIRM performs $7 \rightarrow 3$ reductions as needed.

B. Pooling

During pooling, the dimensionality of an input matrix is reduced by taking the average or maximum of all values in submatrices of a predefined size to generate the output matrix values. Using PIRM, the max function can be realized via TR across all the candidates evaluating MSB to LSB sequentially. Each step compares the binary weight of the same bit position in each word, and the TR result determines the subsequent action via predicted execution with local information. This allows PIM instructions issued by the memory controller to work in parallel across many subarrays in parallel. First, the values upon which to compute the max are stored in adjacent positions between the access points. Then a TR is performed across the MSBs; If TR$>0$ the value under the right head is read and stored in the rowbuffer. If the MSB is ‘0’ the rowbuffer is reset. This eliminates a value that is lower than the other values. Then the DBC is shifted right and the value of the rowbuffer is written to the left head.

All five words are processed in this manner. If TR$=0$, then each word is read from the right and re-written to the left access point, while shifting in between. Essentially, the data remains unchanged. This is necessary because if all values are ‘0’ in this position, it does not eliminate any values from being the maximum. From a PIM instruction execution perspective, the memory controller issued instructions are identical for all participating subarrays by making the rowbuffer reset command predicated on the TR and tested bit. We can use a DWM AND function in another DBC of the same tile/subarray to store and compute the logic value governing the predicated execution of the row-buffer reset.

The process is repeated for each bit position and the value is read using TR$>0$, so the max vector is read, regardless of its location between the heads and if $>1$ vectors equal the max value the TR value it is still accessed correctly. Fig. 8 depicts a concrete example of the state of four words A, B, C, and D as they are processed by the maximum subroutine, in chronological order from left to right with a different color representing the values after a bit is processed. At the MSB pass starting with blue, TR$>0$. Words A and D have ‘0’ in their MSB, so they are overwritten by the zero vector and B and C are written back unchanged. The result after the first step is shown in white. For MSB-1, TR $=0$. Thus all words are read and written back unchanged as shown in red. For MSB-2, TR $>0$. Words A, C, and D all have ‘0’ in that bit position, so they are overwritten by the zero vector and only B is written back unchanged as shown in green. Now the maximum value has been determined, and will be maintained as all the bits are traversed through the LS}.
writing [19] approach and transverse access techniques [17] previously proposed. We illustrate this new concept in Fig. 8. Two write/read heads are represented in dark blue separated by data domains in light blue (four domains are shown instead of seven to simplify the explanation). To perform a classic shift-based write under the left head, WWL1 and RWL0 are closed, thus the current flows from BLB to a fixed layer, to the domain, shifting the dark red upward orientation of the fixed layer to replace the pink downward orientation in the nanowire. This operation can be modified to shift the pink orientation along the nanowire rather than to ground. This TW operation closes WWL1 and RWL1. Thus, the current flows from BLB through the fixed layer and the four domains before exiting through the right head as indicated by the green arrow. By doing so, the fixed layer orientation at WWL1 is written under the left head, and the pink orientation and those which follow it advance along the nanowire, forcing the yellow arrow to GND.

Applying this to the majority function, in the context of Fig. 9 if TR > 0, PIRM reads from the right head (yellow arrow). The predicated rowbuffer reset command is executed. Then the value of the word is written via TW from the left head to the right head. Thus, by reading from the right and conducting TW from the left the segmented shift ensures each updated operand is returned to its original position along the nanowires and the remaining locations are not disturbed.

C. Fully Connected

The fully connected layer executes the following function:

\[
ReLU(Wx + b)
\]  

where \(W\) is the weight matrix, \(x\) is the input vector and \(b\) is the bias vector. The \(ReLU\) function returns zero if \(\sum_{i=0}^{m} W_{ij} x_i + b_j \leq 0\) and \(\sum_{i=0}^{m} W_{ij} x_i + b_j\) otherwise. This function is implemented by computing \(\sum_{i=0}^{m} W_{ij} x_i + b_j\) using PIRM addition and multiplication operations. Using a predicated row refresh based on the MSB, which is ‘1’ for values \(< 0\) and writing the value back the resulting value from the \(ReLU\) function to the array, repeating \(\forall j\).

V. Experimental Results

We present four experiments to demonstrate the effectiveness of PIRM. First, we compare PIRM addition and multiplication characteristics against other computing units based on DWM. Second, we demonstrate the benefit of PIRM PIM on addition/multiplication oriented benchmarks from polybench [31]. Third, we compare bitmap indices [32], a common component of database queries, against Ambit and ELP2IM to show the benefit over state-of-the-art DRAM PIM. Finally, we implement two CNN applications, Lenet5 and Alexnet, using the method in Section IV and compare PIRM to SPIM, Ambit, and ELP2IM.

A. Comparison with DWM PIM technique

Based on the device level information provided in [7], [17], [33], [34], we calculated the timing and energy of read, write and TR operations for DWM. We have designed PIRM’s sense circuits for TR and synthesized the PIM logic from Fig. 4(b) in 45nm technology using FreePDK45 [35] and the Cadence Encounter flow. We then scaled the design by normalizing \(F^2\) to 32nm as described in prior work [33], [36] to compare with the 32nm results reported in DW-NN [7]. To calculate the energy we used a modified version of NVSIM to report the DWM energy at 32nm and modified the SA energy using our custom sensing circuit designed in LTSPICE and scaled energy reported from ASIC synthesis for the PIM logic gates. Latency is obtained by calculating the number of operations needed to perform an 8-bit add or multiply operation presuming a 1ns cycle speed, consistent with values reported by NVSIM. PIRM 8-bit addition shifts and writes the words between the two heads (10 cycles) and then writes after each TR (16 cycles) which yields to a total of 26 cycles. Table 1 reports the speed, energy, and area of PIRM, DW-NN and SPIM for two operand addition (2op add), five operand addition optimized for area by conducting multiple additions in series (5op add area), five operand addition optimized for latency by replicating addition units (5op add latency), and two operand multiplication (2op mult). PIRM is 1.9×, 9.4×, 6.9× and 2.3× faster and 2.2×, 5.5×, 5.5× and 3.4× less energy than SPIM, the state-of-the-art technique, for 2op add, 5op add area optimized, 5op add latency optimized, and 2op multiplication, respectively. PIRM is comparable to DW-NN and requires some area increase over SPIM for addition, but reduces the multiplication area by 3.7× and 3.3× compared to DW-NN and SPIM, respectively, while
TABLE I: Operation Comparison

| Scheme | PIRM | DW-NN | SPIM |
|--------|------|-------|------|
| Unit   | 2op Add (TR = 4) | 5op Add (TR = 7) | Mult (TR = 7) | 2op Add | 5op Add | 5op Add | 2op Mult. |
| Speed (cycles) | 28 | 26 | 64 | 54 | 264 | 194 | 163 |
| Energy (pl) | 12.54 | 22.14 | 57.39 | 40 | 169.6 | 169.6 | 308 |
| Area (µm²) | 2.16 | 4.94 | 5.07 | 2.6 | 2.6 | 5.2 | 18.9 |

TABLE II: DWM parameters

| Memory size | 8GB |
| Number of Bank | 32 |
| Subarrays per Bank | 64 |
| Tile per Subarray | 16 |
| DBC per Tile | 16 |

also providing additional processing capabilities such as bulk-bitwise operations.

B. Improvement to Memory Wall Versus Non-PIM DWM

We tested our scheme on the standard polyhedral polybench using a modified version of RTSIM [37]. The Polybench consists of 29 applications from different domains including linear algebra, data mining, and stencil kernels. From these 29 applications we selected the benchmarks most heavily focused on matrix addition and multiplication, from 2mm, which is two matrix multiplication, to gemm which is governed by $C = \alpha AB + \beta C$. We provide energy and queue latency improvement and the area overhead of PIRM at the main memory granularity. For this simulation we used the parameters of Table II [3].

1) Queue Latency: In these experiments, we extract the traces using a pintool, then we examine the accesses and determine which accesses correspond to additions and multiplications and we determine if there is an available PIRM PIM-enabled tile to perform the operations in memory instead of sending it to the processing unit. In order to efficiently use our PIM, we issue multiple parallel arithmetic instructions from the memory controller to different PIM tiles, which allows single instruction multiple data (SIMD) operation. Over the benchmarks shown in Fig. 10 we demonstrate an average improvement over the memory latency of 2.1×.

2) Area overhead: Fig. 11 shows the area overhead for adding some PIM capability to one tile in each subarray of the memory. There is a 10% overhead for including our full PIM

3) Energy consumption: To perform an energy analysis we compare the energy to send the data from DWM to the CPU and back plus the energy required to perform a CPU operation to the energy that PIRM needs to perform the same operation. The data transfer and operation costs are listed in Table II [4]. While the energy to perform the operation is the same order of magnitude in the CPU and in PIRM, the price to send the data is extremely high, more than 30× the operation cost. Leveraging these savings, Fig. 12 reports the energy improvement over the polybench benchmarks when leveraging PIM as much as possible, which decreases the energy consumption by more than 25.2×, on average.


### TABLE III: CNN application comparison

| Scheme            | Alexnet | Lenet5  |
|-------------------|---------|---------|
| SPIM (FPS)        | 22.5    | 53.2    |
| Ambit-NID (FPS)   | 84.8    | 7697.4  |
| ELP2IM-NID (FPS)  | 96.4    | 8329.5  |
| PIRM (FPS)        | 5217.9  | 130393.4|
| Improvement       | 54×     | 15×     |

---

C. Bitmap Indices

While PIRM has significant benefits over SPIM and DW-NN, neither of these schemes can perform bulk-bitwise logic. Thus, we compare the bulk-bitwise capabilities of PIRM to the state-of-the-art technique for bulk-bitwise operation in DRAM, ELP2IM and Ambit. We make this comparison on a classic PIM application as an indication of what PIRM could achieve against a scheme similar to a currently deployed memory technology.

We repeated the bitmap indices database query [32] experiment from prior DRAM PIM work [4]. A query from 16 million users’ data requested how many male users were active in the past $w$ weeks, where $w \in \{2...4\}$. Fig. [13] shows the latency improvement of Ambit, ELP2IM and PIRM normalized to the latency of a standard DRAM CPU system. For three, four, and five search criteria, i.e., male users for last two, three, and four weeks, PIRM provides a $1.6 \times$, $2.2 \times$, and $3.4 \times$ query speedup, respectively over the state-of-the-art ELP2IM. The speedup achieved when including more search criteria demonstrates the benefit of PIRM given its multi-operand bulk bitwise operations compared to two operand limits of previous work.

D. CNN

We implemented two CNN benchmarks: CNN Lenet-5 [38] and Alexnet [39], commonly used for image processing, machine learning training on handwritten digits and on RGB images. We used the parameters of Table I with a clock frequency of 1GHz. First, we demonstrate the benefit of PIRM over DW-NN and SPIM for convolution (Fig. [7]). Input features and weights can be packed into memory rows and combined with point-wise multiplication. We assume similar packing is possible in SPIM and DW-NN. Where PIRM really shines is in the addition reduction operations. By leveraging multi-operand addition, logical shifting, and a second multi-operand reduction, PIRM can reduce up to a 5x5 convolution window, common in both algorithms, in two addition steps. Presuming the same memory configuration from Table [11] for all schemes, PIRM is capable of executing convolution at 26 Tera Ops Per Second (TOPS), while DW-NN and SPIM achieve 2.88 and 2.92 TOPS, respectively, for the same number of functional units. PIRM is also capable of 108 Giga Ops Per Joule (GOPJ) while DW-NN and SPIM achieve 17 and 25 GOPJ, respectively. For context, a dedicated FPGA CNN accelerator was able to achieve 0.34 TOPS with 12.5 GOPJ [40].

We implemented the full CNNs, including the pooling and fully connected layers, as described in Section V-D. Table [III] shows PIRM improvement over the state-of-the-art PIM techniques in DWM, SPIM, and in DRAM, Ambit and ELP2IM applied to NID [41]. PIRM executes $54 \times$ and $15 \times$ more Frames Per Second (FPS) compared to ELP2IM which was already $1.22 \times$ faster than Ambit.

VI. Conclusion

PIRM is a significant step forward for PIM in the promising DWM technology. Our technique takes advantage of the intrinsic proximity of bits in DWM nanowires and the advantages of TR to build a polymorphic gate that can support myriad PIM operations. PIRM can perform bulk-bitwise or addition on multiple operands simultaneously, limited only by the TRD between access ports on DWM. Using carry-select adder inspired techniques these multi-operand operations can be used to efficiently implement multiplication with minimal additional logic. Our results show that PIRM improves over the state-of-the-art DWM-based PIM by $6.9 \times$ and $2.3 \times$ in terms of energy for five operand addition (optimized for latency) and multiplication, respectively. Thus, in terms of a convolution application, PIRM can perform $8.9 \times$ and $4.3 \times$ more GOPS and GOPJ, respectively. Compared to a standard DWM memory without PIM, PIRM improves memory latency by $2.1 \times$, decreases energy by $25.2 \times$ versus sending the data to the CPU. PIRM incurs an area overhead of 10% when PIM enabling one tile per subarray. PIRM bulk-bitwise capabilities are $\geq 1.6 \times$ faster than the state-of-the-art DRAM approach, ELP2IM. Moreover, PIRM provides a superset of the existing PIM techniques in a single memory technology.

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