Proposal for an All-Spin Artificial Neural Network: Emulating Neural and Synaptic Functionalities Through Domain Wall Motion in Ferromagnets

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Abstract—Non-Boolean computing based on emerging post-CMOS technologies can potentially pave the way for low-power neural computing platforms. However, existing work on such emerging neuromorphic architectures have either focused on solely mimicking the neuron, or the synapse functionality. While memristive devices have been proposed to emulate biological synapses, spintronic devices have proved to be efficient at performing the thresholding operation of the neuron at ultra-low currents. In this work, we propose an All-Spin Artificial Neural Network where a single spintronic device acts as the basic building block of the system. The device offers a direct mapping to synapse and neuron functionalities in the brain while inter-layer network communication is accomplished via CMOS transistors. To the best of our knowledge, this is the first demonstration of a neural architecture where a single nanoelectronic device is able to mimic both neurons and synapses. The ultra-low voltage operation of low resistance magneto-metallic neurons enables the low-voltage operation of the array of spintronic synapses, thereby leading to ultra-low power neural architectures. Device-level simulations, calibrated to experimental results, was used to drive the circuit and system level simulations of the neural network for a standard pattern recognition problem. Simulation studies indicate energy savings by $\sim 100\times$ in comparison to a corresponding digital/ analog CMOS neuron implementation.

Index Terms—Neuromorphic Computing, Artificial Neural Networks, Spintronics, Spin-Orbit Torque, Domain Wall.

I. INTRODUCTION

The basic computing element in an Artificial Neural Network (ANN) involves weighted summation of neuron inputs followed by a thresholding operation. For instance, if the neuron’s inputs are represented by $I_i$ and the corresponding synaptic weights are represented by $w_i$, then the neuron’s output is represented by $y = f(\sum w_i I_i)$. Here, $f$ represents the transfer function of the neuron, which could be a step, linear or sigmoid function of the resultant neuron input. Complex deep learning architectures used for pattern recognition tasks consists of interconnected layers of these basic computing blocks [1]. However, implementation of such algorithms on general-purpose computers are extremely area and energy inefficient since the sequential von-Neumann computing model is a complete contrast to the parallel, event-driven processing in the brain. Even custom analog/digital CMOS implementations have proved to be several orders of magnitude higher power and area consuming since they do not offer a direct mapping to the weighted summation and thresholding operations involved in neural computation. While analog designs are power-hungry, digital designs tend to be area expensive.

As a result, significant research efforts are being directed to develop neural architectures based on emerging post-CMOS technologies like Phase Change Memories (PCM) [2], [3], Ag-Si memristors [4], etc. Inspired by the fact that synapses are the main seat of learning and that synapses outnumber the neurons by several orders of magnitude, researchers have demonstrated how such nanoelectronic devices can directly mimic synaptic functionalities [2], [3], [4], [5], [6], [7]. However, since these synapses are required to drive analog CMOS neurons, power consumption of these neuromorphic systems are still orders of magnitude higher in comparison to that involved in the brain [8].

Recent discoveries in spintronics have brought forward a set of physical phenomena that offer a direct mapping to the thresholding operation of neurons. Researchers have proposed Lateral Spin Valve (LSV) structures [9], domain wall based devices [8] and spin-Hall effect based structures [10] that can be operated at ultra-low voltages and can be switched by ultra-low currents. Resistive crossbar array of programmable synapses based on memristors or PCMs can be interfaced with these spintronic neurons to perform ultra-low power non-Boolean computation [8]. However, a basic limitation of such computing platforms was that these spin-neurons could only emulate the step transfer function in ANNs (corresponding to the switching of a nanomagnet between its two stable states by an input synaptic current) whereas, non-step (linear or sigmoid) transfer function is more attractive for complex pattern recognition tasks since more information can be encoded in the neuron’s output in the latter case. In this paper, we explore the possibility of an All-Spin neuromorphic architecture where the core element is a spintronic device based on a ferromagnet (FM)-heavy metal (HM) multilayer structure, to realize an ultra-low power neural computing platform. The ferromagnet consists of a domain wall separating two oppositely polarized magnetic domains and is programmed by spin-orbit torque (SOT) generated by the heavy metal underlayer. We demonstrate the mapping of
this single device to neuron and synapse functionalities and illustrate how spintronic synapses interfaced with spintronic neurons can communicate via CMOS axon transistors to form a neural network. Further, the device can provide a non-step transfer function and thereby has the potential to be utilized for complex pattern recognition problems. The paper is organized into the following sections. Section II provides a brief description of the underlying device physics in the spintronic device. Section III illustrates the functionality of the proposed device as a neuron and a synapse. Section IV explains the All-Spin neuro-morphic architecture in details. Section V describes the simulation framework along with simulation results.

II. SPINTRONIC DEVICE STRUCTURE: PRINCIPLE OF OPERATION

Let us first provide a brief discussion on the underlying device physics and principle of operation of the three terminal device structure (Fig.1(a)) that serves as the basic building block for the All-Spin ANN. The device is a Magnetic Tunnel Junction (MTJ) where the “free layer” (ferromagnet whose magnetization can be manipulate) is separated from the “pinned layer” (ferromagnet whose magnetization is fixed) by a tunneling oxide barrier (MgO). The “free layer” consists of a ferromagnet where a domain wall separates two oppositely polarized magnetic regions.

The domain wall in the ferromagnet (FM) can be displaced by SOT exerted by a charge current flowing through a heavy metal (HM) underlayer. Current flow through an underlying HM in FM-HM heterostructures has recently become a promising mechanism to achieve deterministic domain wall displacement in FMNs [11], [12], [13], [14], [15]. This is mainly due to the fact that the same domain wall displacement can be achieved by current density magnitudes that are ~100× lower in comparison to conventional spin-transfer torque driven domain wall motion. Further, the input charge current flows mainly through the HM underlayer whose resistance is generally an order of magnitude lower than that of the FM. It is worth noting here that no external magnetic field is required for the displacement of the domain wall. Spin-orbit coupling at the interface of such magnetic multilayers (with Perpendicular Magnetic Anisotropy) leads to Dzyaloshinskii-Moriya exchange interaction (DMI) which results in the stabilization of a chiral Néel domain wall [11], [12], [13], [14], [15]. Assuming spin-Hall effect [11], [12], [13], [14], [15] to be the dominant underlying physical phenomena, an in-plane charge current through the HM underlayer results in the generation of a transverse spin current due to deflection of opposite spin polarizations at the top and bottom surfaces of the HM. For magnetic multilayers with left-handed chirality (see Fig.2), input charge current flow through the HM underlayer results in domain wall movement in the same direction and vice-versa.

Fig.2 illustrates the underlying physical phenomena responsible for domain wall motion in magnetic heterostructures with perpendicular magnetic anisotropy (PMA) due to the flow of an in-plane charge current through a heavy metal underlayer. The magnetization dynamics of the ferromagnet can be described by solving Landau-Lifshitz-Gilbert equation with additional term to account for the spin-orbit torque generated by spin-Hall effect (SHE) at the FM-HM interface [12], [16].

$$\frac{d\mathbf{m}}{dt} = -\gamma(\mathbf{m} \times \mathbf{H}_{eff}) + \alpha(\mathbf{m} \times \frac{d\mathbf{m}}{dt}) + \beta(\mathbf{m} \times \mathbf{m}_P \times \mathbf{m})$$  (1)

where $\mathbf{m}$ is the unit vector of FM magnetization at each grid point, $\gamma = \frac{2\mu_B}{h}$ is the gyromagnetic ratio for electron, $\alpha$ is Gilbert’s damping ratio, $\mathbf{H}_{eff}$ is the effective magnetic field, $\beta = \frac{\hbar J}{2\mu_0 e M_s}$ ( $\hbar$ is Planck’s constant, $J$ is input charge current density, $\theta$ is spin-Hall angle [12], $\mu_0$ is permeability of vacuum, $e$ is electronic charge, $t$ is FL thickness and $M_s$ is saturation magnetization) and $\mathbf{m}_P$ is direction of input spin current. The effective field $\mathbf{H}_{eff}$ also includes the field due to
DMI [12] and is given by,

$$\mathbf{H}_{DMI} = -\frac{2D}{\mu_0 M_s} \left[ \frac{\partial m_z}{\partial x} \hat{x} + \frac{\partial m_z}{\partial y} \hat{y} - \left( \frac{\partial m_x}{\partial x} + \frac{\partial m_y}{\partial y} \right) \hat{z} \right]$$

(2)

Here, $D$ represents the effective DMI constant and determines the strength of DMI field in such multilayer structures. A positive sign of $D$ implies right-handed chirality and vice versa. In the presence of DMI, the boundary conditions at the edges of the sample is given by,

$$\frac{\partial \mathbf{m}}{\partial n} = \frac{D}{2A} \mathbf{m} \times (\hat{n} \times \hat{z})$$

(3)

where, $A$ is the exchange correlation constant and $\hat{n}$ represents the unit vector normal to the surface of the FM. Current density was estimated by assuming that the current flow is mainly through the FM-HM layers in the stack structure [12].

Based on this physical phenomena, we propose a three terminal device structure, as shown in Fig.1, with decoupled “write” and “read” current paths. The “write” current, $I_{write}$, flows through the HM underlayer (between terminals WRITE and GND) and its magnitude determines the position of the domain wall in the MTJ “free layer”. The “pinned layer”s on either side of the “free layer” serve to stabilize the domain wall at either side of the “free layer” for large magnitudes of the input current. On the other hand, the “read” current, $I_{read}$, flows through the MTJ structure (between terminals READ and GND). The magnitude of the “read” current is modulated by the device conductance, which in turn, is a function of the domain wall position in the “free layer” of the MTJ. The domain wall position can be programmed by an appropriate charge current, $I_{write}$, between terminals WRITE and GND. The “read” current magnitude has to be maintained lower than the minimum current required for domain wall depinning. It is worth mentioning here, that deterministic domain wall movement have been experimentally demonstrated in such magnetic multilayer structures [11], [12], [13], [14], [15]. However, MTJs have been traditionally used to “read” the “free layer” magnetization state at the two extreme resistance states, namely the parallel (P) or the anti-parallel (AP) state. In this proposal, we exploit the analog resistance variation of the MTJ with change in domain wall position to realize neuron and synapse functionalities in such spintronic devices. We believe that this proposal for an All-Spin ANN will stimulate proof-of-concept experiments to develop such non-Von Neumann device structures suitable for low-power neural processing.

In order to simulate the variation of the MTJ resistance with applied voltage and oxide thickness, Non-Equilibrium Green’s Function (NEGF) based transport simulation framework [12] was utilized. Considering that the FM has a uniform magnetization direction, the MTJ resistance ($R$) is a function of the spacer (MgO) thickness ($t_{MgO}$), relative angle between the magnetizations of the FM and the pinned layer ($\theta$), and the voltage across the MTJ ($V_{MTJ}$). The variation is described by the following equations,

$$R \propto \left( e^{a_m t_{MgO}} + b_0 + \sum_{m=1}^c \left( (-1)^{m-1} V_{MTJ}^2 e^{a_m t_{MgO} + b_m} \right) \right)^{-d}$$

(4)

$$R(\theta) = \left( \frac{1}{R_P} \left( \cos \left( \frac{\theta}{2} \right) \right)^2 + \frac{1}{R_{AP}} \left( \sin \left( \frac{\theta}{2} \right) \right)^2 \right)^{-1}$$

(5)

Here, $R_P$ and $R_{AP}$ represent the parallel ($\theta = 0$) and anti-parallel resistance ($\theta = \pi$) of the MTJ respectively. The fitting parameters $a_m, b_m, c, \text{ and } d$ are determined by calibrating the simulation framework with experimental data reported in [18], [19]. For an extensive description of the NEGF based simulation framework, readers are referred to Ref. [17].
III. NEURON AND SYNAPSE FUNCTIONALITIES OF THE PROPOSED DEVICE

A. Synapse Functionality

The synapse functions as the memory element in neuromorphic architectures. Synapses are junctions (characterized by weights) between neurons and transmit weighted signals from the transmitting to the receiving neuron. The operation of the spintronic device as a synapse is explained in Fig 1. For a fixed applied voltage at the READ terminal, the resistance of the device between the READ and GND terminals is mainly given by the parallel combination of the AP and P domains along with a small region where the “free layer” magnetization is along the horizontal axis (corresponding to the domain wall region). The heavy-metal resistance in the path of \( I_{\text{read}} \) is negligible in comparison to the tunneling oxide resistance. Let us denote the device conductance when the entire “free layer” magnetization is P (AP) to the “pinned layer” by \( G_{P,\text{max}}(G_{AP,\text{max}}) \). Thus, for an intermediate position \( x \) of the domain wall from the left-edge of the MTJ, the equivalent conductance will be given by,

\[
G_S(x) = G_{P,\text{max}} \left( \frac{x}{L} \right) + G_{AP,\text{max}} \left( \frac{1-x}{L} \right) + G_{DW}.
\]  

Here, \( G_{DW} \) denotes the conductance of the domain wall region and \( L \) represents the length of the MTJ (excluding the domain wall width). For a fixed voltage applied between READ and GND terminals, \( G_{P,\text{max}}, G_{AP,\text{max}} \) and \( G_{DW} \) are constants. Hence, \( G_S \) is a linear function of \( x \) and therefore, the conductance in the path of the read current can be appropriately set by programming the domain wall position (by passing “write” current through the heavy metal). Hence, when a voltage \( V_S \) is applied across the spintronic synapse, the current, \( I_S = G_S \cdot V_S \), flowing through the device gets modulated by the MTJ equivalent conductance (which encodes the synaptic weight). It is worth noting here, that the resistance range of the spintronic synapses can be varied by varying the oxide thickness. Additionally, the critical current responsible for domain wall depinning for a particular time duration scales linearly with the device width. Hence, the width of the spintronic synapses can be appropriately designed such that the “read” current through the MTJ (which flows through some portion of the heavy metal) does not cause any domain wall motion. Although there is some injected spin current due to “read” current flowing through the PL, its magnitude is much smaller in comparison to that due to SOT.

The ratio of the maximum to minimum synaptic weight encoded in the MTJ conductances will be determined by the Tunneling Magnetoresistance Ratio (TMR) values of the devices. MTJ TMR values of \( \sim 600\% \) [20] have been fabricated resulting in a maximum to minimum weight ratio of \( \sim 7 \). TMR values \( > 1,000\% \) are expected within a time period of ten years [21].

B. Neuron Functionality

The neuron serves as the computing element in ANNs. It is characterized by a transfer function, i.e. it produces an output signal in accordance to the magnitude of its resultant synaptic input signal. The neuron’s output signal is transmitted via the axon as an input to its fan-out neurons. Fig 2 demonstrates the operation of the proposed spintronic device as a neuron. The neuron operation takes place in three stages, namely the “write”, “read” and “reset” stages. During the “write” stage, the neuron (denoted by “Neuron MTJ”) receives the resultant synaptic input current (flowing between terminals IN and GND) and its magnitude determines the domain wall position. Higher the magnitude of the synapse current, higher is the domain wall displacement and hence lower is the device resistance. During the “read” cycle, the IN terminal is deactivated and the “axon” circuit is activated. The “Reference MTJ” (whose orientation is fixed in the AP state) serves to produce a resistive divider network such that the gate voltage \( V_G \) of the PMOS transistor decreases (due to decrease in resistance of the pull-down network) with increase in the magnitude of the synaptic input current. Hence, the output current, \( I_{OUT} \), provided by the PMOS transistor increases with increase in the magnitude of the input current, \( I_{IN} \) (due to increase in magnitude of \( V_{GS} \) of the PMOS transistor). The neuron transfer function is characterized by the relationship between \( I_{OUT} \) and \( I_{IN} \) and the output transistor mimics the axon functionality of biological neurons by propagating the neuron output signal to fan-out neurons in the next stage. Finally, during the “reset” phase the domain wall is initialized to the left edge of the “free layer” of the MTJ neuron for the next operation cycle.

C. Correspondence to Biological Neural Network

Fig 3 demonstrates the close correspondence between the biological neural network and the proposed All-Spin neural network and thereby illustrates the direct mapping of synapse and neuron functionalities to nanoelectronic spin-devices. The biological neuron receives synaptic inputs from synapses and generates an output that is a function of the resultant input. The neuron’s output is transmitted via the axon to fan-out neurons. Similarly, the spintronic neuron receives a resultant synaptic current which is the weighted summation of its inputs. This resultant current input flowing through the heavy metal of the spintronic neuron generates an output which is transmitted via the CMOS transistor, acting as the axon, to the next stage.

IV. ALL-SPIN NEUROMORPHIC ARCHITECTURE

Next, let us consider the hardware mapping of a feed-forward ANN comprising of a hidden layer of neurons connected in an all-to-all fashion to an output layer (Fig 4). Let us first discuss the operation of the hidden layer. The hidden layer can be represented by a resistive crossbar network, as shown in Fig 5 where the input voltages (corresponding to pixel intensities) are applied along the horizontal rows. The vertical columns are connected to the spintronic neurons. Spintronic synapses are present at each cross-point of the array and the domain wall position in the device encodes the value of the corresponding synaptic weight or conductance. Let us denote the synaptic device conductance connecting the \( i \)-th input to the \( j \)-th neuron as \( G_{ij} \) and the neuron resistance lying in
domain wall position gets programmed in the “hidden layer” spintronic neurons. During the operation of the “hidden layer”, the “read” circuit of the “hidden” layer neurons is activated. The output axon PMOS transistor generates an output current which provides the input to the next layer. Considering the voltage drop across the spin-neurons for the next layer to be negligible, each PMOS transistor drives an equivalent conductance \( G_{eq} \), which is the sum of the synaptic conductances for a particular row. The input voltage provided to each row of the “output” layer crossbar array will be given by the product of the transistor output current and \( G_{eq} \). In order to ensure that the input voltage does not vary with varying \( G_{eq} \) for the different rows, a dummy column was considered in the crossbar array, where the conductance in a particular row of the dummy column is set such that the value of \( G_{eq} \) is equal for all rows of the array. As explained earlier, the “output” layer neurons receive currents proportional to the weighted summation of the inputs and produces a corresponding output.

It is worth mentioning here that the synaptic weights in an ANN can be positive or negative. In order to implement this functionality, the crossbar array for a particular layer can be split up into two separate “positive” and “negative” arrays. In case a particular synaptic weight is positive (negative), then the corresponding conductance in the “positive” (“negative”) array is set in accordance to the weight, else it is set to a very high OFF resistive state. The neuron “write” operation is then split up into two cycles where the “positive” crossbar array provides input current to the neuron in one direction during the first cycle and the “negative” array provides input current in the opposite direction during the next cycle.

Scalability of the proposed architecture can be determined by the driving capability of the neurons and synapses. Higher the number of synaptic inputs to the neuron, higher will be the magnitude of \( \sum_i G_{ij} \). However, the resistance range of the synapses can be appropriately tuned such that the ratio \( \gamma \ll 1 \). The number of neurons in the succeeding layer that can be connected to a particular neuron of the previous layer via the axon transistor is limited by the current driving capability, i.e., size of the transistor. However, this can be overcome by distributing large synaptic arrays into smaller crossbar arrays.

V. SIMULATION FRAMEWORK AND RESULTS

In order to assess the functionality and power consumption of the proposed All-Spin neural network, a hybrid device-circuit-algorithm co-simulation framework was used. The synergistic simulation framework, consisting of a “top-down” and “bottom-up” perspective, is described next.

A. Top-Down Perspective

As proof of concept, a small-scale ANN with 20 hidden layer neurons and 26 output layer neurons was used to recognize characters A-Z from the Chars74K dataset [22]. The input images were downscaled to size 16x16 and were applied as a 1-D vector to the input layer. The neuron transfer function was taken to be linearly increasing with the input, ultimately saturating at a maximum value. The choice of the transfer
function was obtained from device and circuit level simulations and will be described later. Standard backpropagation algorithm was used to generate a set of weights and biases of the network (for mapping to synapse conductance values). The accuracy of the network over a set of 260 images from the dataset was evaluated to be $\sim 80\%$.

B. Bottom-Up Perspective

The bottom-up simulation framework involves the investigation of the device physics of current induced spin-orbit torque in ferromagnets and the development of behavioral models for system level simulations of the All-Spin neural network. The simulation parameters (given in Table I) were obtained experimentally from magnetometric measurements of Ta(3nm)/Pt(3nm)/CoFe(0.6nm)/MgO(1.8nm)/Ta(2nm) nanostrips [11], [12]. The graphs are in good agreement with [12].

Fig. 6. (a) Domain wall displacement as a function of time for a CoFe strip of cross-section $120\times 30\, nm$ due to the application of a charge current density, $J = 0.1 \times 10^{12} A/m^2$. (b) Domain wall velocity as a function of current density. The domain wall displacement increases linearly with the magnitude of the charge current density and ultimately saturates to a maximum value. The simulation parameters (given in Table I) were obtained experimentally from magnetometric measurements of Ta(3nm)/Pt(3nm)/CoFe(0.6nm)/MgO(1.8nm)/Ta(2nm) nanostrips [11], [12]. The graphs are in good agreement with [12].

The velocity increases linearly with the current density and ultimately reaches a saturation velocity. The graphs are in good agreement with results illustrated in [12] for the same multilayer structure described in this section.

It is worth noting here that for a given duration of the current through the heavy metal, the domain wall displacement is directly proportional to the magnitude of the current (considering input current range to be less than the saturation regime). The simulations were performed in MuMax3, a GPU accelerated micromagnetic simulation framework [23]. Fig. 7 shows the temporal motion of the DMI stabilized domain wall in the device due to a programming current flowing through the HM for a duration of $1ns$. For a device with “free layer” dimensions of $120\times 20\, nm$, a maximum current of $\sim 25\, \mu A$ is required to displace the domain wall from one edge of the FM to the other edge.

Fig. 7. Domain wall motion in the device due to programming current of $25\, \mu A$ flowing through the HM underlayer for a duration of $1ns$. The FM was taken to be $120\, nm$ in length surrounded by pinned layers of length $20\, nm$ on either side. The domain wall is displaced entirely from one edge of the FM to the other edge.

The NEGF based transport simulation framework was calibrated to experimental results illustrated in [18], [19]. (a) Device resistance increases with increase in oxide thickness. (b) The AP MTJ resistance decreases with increase in the applied voltage across the MTJ. However, for sufficiently low values of applied voltage ($< 100\, mV$), the AP resistance variation is extremely small.

![Image](image_url)

Fig. 8. The NEGF based transport simulation framework was calibrated to experimental results illustrated in [18], [19]. (a) Device resistance increases with increase in oxide thickness. (b) The AP MTJ resistance decreases with increase in the applied voltage across the MTJ. However, for sufficiently low values of applied voltage ($< 100\, mV$), the AP resistance variation is extremely small.

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In order to simulate the variation of the MTJ resistance with domain wall position, Non-Equilibrium Green’s Func-
tion (NEGF) based transport simulation framework [17] was utilized. The simulation framework was calibrated to experimental results illustrated in [18]. [19]. For determining the MTJ resistance for a FM with a domain wall separating two oppositely polarized magnetized domains, the NEGF based simulator [17] was modified by considering the parallel connection of three MTJs. The magnetization direction of the FL of the three MTJs were considered parallel, anti-parallel and perpendicular (domain wall) to the pinned layer magnetization. The length of the first two MTJs was varied according to the position of the domain wall while the width of the third MTJ was taken to be equal to the domain wall width. Additionally, as shown in Fig. 8 the resistance range of the device can be varied by varying the oxide thickness.

C. System Level Simulations

The accuracy of the neural network over the image set was evaluated by varying the bit discretization level in the neurons and synapses. It was observed that there was insignificant degradation in accuracy with 15 (4 bit) intermediate levels and 3 (2-bit) intermediate levels between the maximum and minimum values of the synapse weights and neuron outputs respectively. Assuming that domain wall displacement over a distance of 10 nm can be sensed and considering a domain wall width of ~ 10 nm (approximately), the length of the “free layers” of the neurons and synapses were chosen to be 50 nm and 170 nm respectively.

Let us first discuss the simulation results for the spintronic neuron. Since the neuron is the computing element in the network, the device can be aggressively scaled down. Hence the area of the neuron “free layer” was taken to be 50 nm × 20 nm, corresponding to an MTJ “pinned layer” area of 30 nm × 20 nm. The critical current required to displace the domain wall from one edge of the “free layer” to the other was observed to be ~ 5 µA for a switching time of 2 ns. The synaptic crossbar array was split up into “positive” and “negative” arrays as mentioned in the previous section (corresponding to positive and negative synaptic weights). System level simulations yielded a maximum synaptic current of ~ 50 µA as input to the neuron. The resistance lying in the path of the input synaptic current was estimated to be ~ 140 Ω (for the above mentioned device dimensions) resulting in a maximum voltage drop of ~ 7 mV across the spintronic neurons.

Such ultra-low voltage operation of the spintronic neurons help in reducing the overall power consumption of the All-Spin neural network since the crossbar arrays can be operated at a much lower voltage. In our simulations, we considered a maximum input voltage of 100 mV across each horizontal row of the crossbar array. The minimum resistance (corresponding to a synaptic weight “1”) in the crossbar array was evaluated to be 20 KΩ (to ensure the critical current requirement of 5 µA to move the domain wall from one edge of the “free layer” to the opposite edge). Based on the crossbar resistance values, the maximum value of γ in the network was determined to be ~ 0.07 << 1, thereby validating the assumption that the voltage drop across the spin-neurons is negligible. Further, it is also apparent from Fig. 8 that variation in AP or P resistance of MTJ is extremely small for applied voltages < 100 mV. Hence, variation in synaptic conductance with applied voltage was considered to be insignificant. The maximum current flows through the synapse when 100 mV is applied across the minimum synaptic resistance (20 KΩ), which is ~ 5 µA. In order to ensure that the “read” current flowing through the synapse does not cause any domain wall displacement, the width of the synapse was scaled up to 200 nm. For the above device dimensions, the heavy metal resistance lying in the path of the synaptic current was ~ 50 Ω which is much lower than the range of synaptic resistances in the crossbar array.

Fig. 9 illustrates the variation of the output current provided by the axon transistor with input current to the neuron. As the magnitude of input current flowing through the heavy metal underlayer of the neuron increases, the gate voltage, V_G, of the axon transistor decreases as the pull-down resistance of the resistive divider network decreases. The supply voltage of the PMOS axon transistor was taken to be 650 mV. The supply voltage of the resistive divider network (0.9 V) was optimized such that the corresponding swing in the gate voltage resulted in maximum swing of the output current. The maximum current to be supplied by the axon transistor

![Fig. 9. (a) Gate voltage of axon transistor decreases with increase in magnitude of neuron input current, (b) Output current provided by axon transistor reduces with increase in the gate voltage, (c) Output current provided by the axon transistor increases almost linearly with the input current to the neuron. Hence, the neuron transfer function was taken to be linearly increasing with the input, ultimately saturating at a maximum value.](image)
was determined by the value of $G_{eq}$, such that the maximum voltage across the crossbar array was $\sim 100 mV$. As shown in Fig. 9(c), the output current provided by the axon transistor increases almost linearly with the input current to the neuron.

Another important point of consideration is the degradation of classification accuracy due to device mismatches and variability in the spintronic devices. Although there can be variation in the programming of domain wall position in the spintronic neurons/synapses, deterministic domain wall motion has been observed in such magnetic multilayer structures by several research groups \[11, 15, 24\]. Further, notches can be also utilized to pin the domain wall at specific locations along the length of the magnet to achieve necessary bit discretization \[25\]. Further, impact of resistance variation of the devices on the classification accuracy was evaluated by running 100 stochastic simulations of the network. Negligible degradation ($< 4\%$) in classification accuracy was observed even with $20\%$ variation in the resistances of the spintronic devices. This can be attributed to the error resilient nature of such brain-inspired computing systems. Further, recent efforts in the implementation of on-chip or chip-in-the-loop learning may be utilized to alleviate such issues and implement variation immune neuromorphic systems \[26\].

Let us now discuss the energy consumption involved in the spintronic neuron. It has three components, namely, the “write” power, the “read” power, and the “reset” power. The All-Spin neural network was simulated over the entire set of 260 images and the magnitude of the average current flowing through each neuron was estimated to be $\sim 17.5 \mu A$ through the entire time window of $4 ns$ for the “positive” crossbar array and $2 ns$ for the “negative” array. This results in an average “write” energy consumption of $0.17 fJ (\sim I^2 R t$ energy consumption). For the “read” circuit, the average current from the voltage supply ($0.9 V$) was maintained to sufficiently low values ($\sim 80 nA$) by an appropriate MTJ oxide thickness of $\sim 2 nm$. Lower read current helps in ensuring that there is no domain wall displacement during the “read” cycle and additionally helps in reducing the overall neuron power consumption. Since the “read” circuit for the hidden layer has to provide the input current to the “positive” and “negative” crossbar arrays for the output layer, each for a duration of $2 ns$, the overall “read” energy consumption involved is $0.15 fJ (V I t$ energy consumption). Considering that a current of $\sim 5 \mu A$ can “reset” the neuron in a duration of $2 ns$, the $I^2 R t$ “reset” energy consumption is $\sim 0.007 fJ$. As a result, the average overall energy consumption of the spintronic neuron is $\sim 0.32 fJ$ which is almost two orders of magnitude lower in comparison to a corresponding analog ($\sim 700 fJ$) and digital ($\sim 832.6 fJ$) CMOS neuron design in $45 nm$ technology. Additionally, for a given range of synaptic resistances, the crossbar array can be operated at ultra-low voltages of $\sim 100 mV$. In contrast, the crossbar arrays have to be operated at a much higher voltage $\sim 500 mV (V_{dd}/2)$ for running analog CMOS neurons. This results in power savings by a factor $\sim 25 \times$ per synapse ($V^2 / R$ power consumption) and thereby helps in reducing the overall power consumption of the neuromorphic system.

In conclusion, we have provided a vision for an All-Spin neural architecture where a single nanoelectronic device is able to mimic neuron and synapse functionalities in such systems. We provided extensive results for a standard image recognition problem based on an experimentally benchmarked device simulation framework to illustrate the functionality and energy-efficiency. Such All-Spin ANN architectures can potentially pave the way for ultra-low power deep learning neural systems.

References

[1] J. Schmidhuber, “Deep learning in neural networks: An overview,” Neural Networks, vol. 61, pp. 85–117, 2015.
[2] B. L. Jackson, B. Rajendran, G. S. Corrado, M. Breitwisch, G. W. Barr, R. Cheek, K. Gopalakrishnan, S. Raoux, C. T. Retten, A. Padilla et al., “Nanoscale electronic synapses using phase change devices,” ACM Journal on Emerging Technologies in Computing Systems (JETC), vol. 9, no. 2, p. 12, 2013.
[3] D. Kuzum, R. G. Jeyasingh, B. Lee, and H.-S. P. Wong, “Nanoscale programmable synapses based on phase change materials for brain-inspired computing,” Nano letters, vol. 12, no. 5, pp. 2179–2186, 2011.
[4] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, “Nanoscale memristor device as synapse in neuromorphic systems,” Nano letters, vol. 10, no. 4, pp. 1297–1301, 2010.
[5] B. Rajendran, Y. Liu, J.-s. Lee, K. Gopalakrishnan, L. Chang, D. J. Friedman, and M. B. Ritter, “Specifications of nanoscale devices and circuits for neuromorphic computational systems,” Electron Devices, IEEE Transactions on, vol. 60, no. 1, pp. 246–253, 2013.
[6] S. Ramakrishnan, P. E. Hasler, and C. Gordon, “Floating gate synapses with spike-time-dependent plasticity,” Biomedical Circuits and Systems, IEEE Transactions on, vol. 5, no. 3, pp. 244–252, 2011.
[7] A. Sengupta, Z. Al Azim, X. Fong, and K. Roy, “Spin-orbit torque induced spike-timing dependent plasticity,” Applied Physics Letters, vol. 106, no. 9, p. 093704, 2015.
[8] M. Sharad, D. Fan, and K. Roy, “Spin-neurons: A possible path to energy-efficient neuromorphic computers,” Journal of Applied Physics, vol. 114, no. 23, p. 234906, 2013.
[9] M. Sharad, C. Augustine, G. Panagopoulos, and K. Roy, “Spin-based neuron model with domain-wall magnets as synapse,” Nanotechnology, IEEE Transactions on, vol. 11, no. 4, pp. 843–853, 2012.
[10] A. Sengupta, S. H. Choday, Y. Kim, and K. Roy, “Spin orbit torque based electronic neuron,” Applied Physics Letters, vol. 106, no. 14, p. 143701, 2015.
[11] S. Emori, U. Bauer, S.-M. Ahn, E. Martinez, and G. S. Beach, “Current-driven dynamics of chiral ferromagnetic domain walls,” Nature materials, vol. 12, no. 7, pp. 611–616, 2013.
[12] E. Martinez, S. Emori, N. Perez, L. Torres, and G. S. Beach, “Current-driven dynamics of Dzyaloshinskii domain walls in the presence of in-plane fields: Full micromagnetic and one-dimensional analysis,” Journal of Applied Physics, vol. 115, no. 21, p. 213909, 2014.
[13] S. Emori, E. Martinez, K.-J. Lee, H.-W. Lee, U. Bauer, S.-M. Ahn, P. Agrawal, D. C. Bono, and G. S. Beach, “Spin Hall torque magnetometry of Dzyaloshinskii domain walls,” Physical Review B, vol. 90, no. 18, p. 184427, 2014.
[14] K.-S. Ryu, S.-H. Yang, L. Thomas, and S. S. Parkin, “Chiral spin torque arising from proximity-induced magnetization,” Nature communications, vol. 5, 2014.
[15] K.-S. Ryu, L. Thomas, S.-H. Yang, and S. Parkin, “Chiral spin torque at magnetic domain walls,” Nature nanotechnology, vol. 8, no. 7, pp. 527–533, 2013.
[16] J. C. Słomczewski, “Conductance and exchange coupling of two ferromagnets separated by a tunneling barrier,” Physical Review B, vol. 39, no. 10, p. 6995, 1989.
[17] X. Fong, S. K. Gupta, N. N. Mojumder, S. H. Choday, C. Augustine, and K. Roy, “KNACK: A hybrid spin-charge mixed-mode simulator for evaluating different genres of spin-transfer torque MRAM bit-cells,” in Simulation of Semiconductor Processes and Devices (SISPAD), 2011 International Conference on. IEEE, 2011, pp. 51–54.
[18] S. Yuasa, T. Nagahama, A. Fukushima, Y. Suzuki, and K. Ando, “Giant room-temperature magnetoresistance in single-crystal Fe/MgOFe magnetic tunnel junctions,” Nature materials, vol. 3, no. 12, pp. 868–871, 2004.
[19] C. Lin, S. Kang, Y. Wang, K. Lee, X. Zhu, W. Chen, X. Li, W. Hsu, Y. Kao, M. Liu et al., “45nm low power CMOS logic compatible embedded STT MRAM utilizing a reverse-connection IT/1MTJ cell,” in Electron Devices Meeting (IEDM), 2009 IEEE International. IEEE, 2009, pp. 1–4.

[20] S. Ikeda, J. Hayakawa, Y. Ashizawa, Y. Lee, K. Miura, H. Hasegawa, M. Tsunoda, F. Matsukura, and H. Ohno, “Tunnel magnetoresistance of 604% at 300 K by suppression of Ta diffusion in CoFeB/MgO/CoFeB pseudo-spin-valves annealed at high temperature,” Applied Physics Letters, vol. 93, no. 8, p. 2508, 2008.

[21] A. Hirohata, H. Sugetawa, H. Yanagishara, I. Zutic, T. Seki, S. Mizukami, and R. Swaminathan, “Roadmap for emerging materials for spintronic device applications,” Magnetics, IEEE Transactions on, vol. 51, no. 10, pp. 1–11, 2015.

[22] T. E. de Campos, B. R. Babu, and M. Varma, “Character recognition in natural images,” in VISAPP (2), 2009, pp. 273–280.

[23] A. Vansteenkiste, J. Leliaert, M. Dvornik, M. Helsen, F. Garcia-Sanchez, and B. Van Waeyenberge, “The design and verification of mumax3,” AIP Advances, vol. 4, no. 10, p. 107133, 2014.

[24] D. Bhowmik, M. E. Nowakowski, L. You, O. Lee, D. Keating, M. Wong, J. Bokor, and S. Salakhuddin, “Deterministic domain wall motion orthogonal to current flow due to spin orbit torque,” arXiv preprint arXiv:1407.6137 2014.

[25] D. Lacour, J. Katine, L. Folks, T. Block, J. Childress, M. Carey, and D. B. Strukov, “Training and operation of an integrated neuromorphic network based on metal-oxide memristors,” Nature, vol. 521, no. 7550, pp. 61–64, 2015.

[26] S. G. Ramasubramanian, R. Venkatesan, M. Sharad, K. Roy, and A. Vansteenkiste, J. Leliaert, M. Dvornik, M. Helsen, F. Garcia-Sanchez, and B. Van Waeyenberge, “The design and verification of mumax3,” AIP Advances, vol. 4, no. 10, p. 107133, 2014.

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