Electrically Reconfigurable Organic Logic Gates: A Promising Perspective on a Dual-Gate Antiambipolar Transistor

Ryoma Hayakawa, Kosuke Honma, Shu Nakaharai, Kaname Kanai, and Yutaka Wakayama*

Electrically reconfigurable organic logic circuits are promising candidates for realizing new computation architectures, such as artificial intelligence and neuromorphic devices. In this study, multiple logic gate operations are attained based on a dual-gate organic antiambipolar transistor (DG-OAAT). The transistor exhibits a \( \Lambda \)-shaped transfer curve, namely, a negative differential transconductance at room temperature. It is important to note that the peak voltage of the drain current is precisely tuned by three input signals: bottom-gate, top-gate, and drain voltages. This distinctive feature enables multiple logic gate operations with “only a single DG-OAAT,” which are not obtainable in conventional transistors. Five logic gate operations, which correspond to AND, OR, NAND, NOR, and XOR, are demonstrated by adjusting the bottom-gate and top-gate voltages. Moreover, varying the drain voltage makes it possible to reversibly switch two logic gates, e.g., NAND/NOR and OR/XOR. In addition, the DG-OAATs show a high degree of stability and reliability. The logic gate operations are observed even months later. The hysteresis in the transfer curves is also negligible. Thus, the device concept is promising for realizing multifunctional logic circuits with a simple transistor configuration. Hence, these findings are expected to surpass the current limitations in complementary metal–oxide–semiconductor devices.

1. Introduction

State-of-the-art computing systems, including artificial intelligence systems and neuromorphic computers, are highly required for the forthcoming Internet of Things society due to the growing demand for high-throughput data processing and low power consumption.[1–6] Organic integrated circuits hold promise for such cutting-edge computers.[7–10] This is because their unique features, such as mechanical flexibility, light weight, and low cost production, offer new device architectures such as printable and wearable brain-like logic circuits that cannot be obtained by the current Si-based electronics.[10–13] However, organic devices suffer from difficulties with regard to minimizing the use of electronic components due to their incompatibility with conventional lithography techniques. Therefore, logic circuits still have low integration density and poor data processing capability.[14,15]

Reconfigurable logic circuits, as represented by field-programmable gate arrays (FPGAs), have the potential to provide a paradigm shift from the von Neumann-type computer architecture.[16–20] The reason is that reconfigurability, which is the most attractive characteristic in these devices, is expected to enable parallel and high-speed data processing, low power consumption, and the large-scale integration of electronic components by taking advantage of the diverse and flexible circuit designs in individual hardware levels. These are the required features for the upcoming “big data era.”

So far, several types of emerging reconfigurable devices have been proposed, such as multiple gate transistors, ambipolar transistors, optically controllable transistors, and non-volatile memory devices, which include resistive memory-based FPGAs and ferroelectric gate transistors.[21–27] However, in most cases, these devices are basically constructed with the current complementary metal-oxide-semiconductor (CMOS) architecture.[16,26,27] Thus, the device configurations make these logic circuits complex. For instance, four transistors are required to produce NAND logic gates and eight transistors are necessary for the reconfigurable switching of NAND and NOR gates.[16,24,27] As a result, developing a simplified device structure to integrate multiple logic functions into a single device is a key strategy for attaining high-performance reconfigurable logic circuits. Gaspar et al. demonstrated two logic gate operations, NOR and NAND, with a simple dual-gate transistor in this regard.[28] The two logic gate operations were electrically switched in this study.
by adjusting the drain voltages. Additionally, Martins et al. implemented OR and AND logic gates by selecting the proper input voltages in the same transistor configuration.\[29\] However, the drain current of these transistors increases in a monotonic manner. As a result, the reconfigurable logic gate operations have been limited to OR/AND, AND/NAND, or NOR/NAND combinations.\[28–31\]

In this study, we propose a new reconfigurable logic circuit based on a single dual-gate organic antiambipolar transistor (DG-OAAT). An antiambipolar transistor (AAT) is a type of heterojunction transistor and is an essential component in the proposed circuit.\[32–38\] The transistor has a partially overlapped region of p-type and n-type semiconductors (pn junction) in the transistor channel. Therefore, it can induce a negative differential transconductance (NDT) even at room temperature. Namely, a sharp increase and then decrease in the drain current (that is, Λ-shaped drain current) can be visible despite the increase in the gate voltage. Due to this attractive feature, multivalued logic circuits (MVLs), such as ternary and quaternary inverters, have recently been realized, and their development is another significant strategy for improving the data processing capability of the currently used logic circuits.\[39–45\]

In contrast to the abovementioned efforts on MVLs, our approach is to apply AATs to electrically reconfigurable logic circuits. A dual-gate configuration enables the control of the used Λ-shaped drain current by three input signals: bottom-gate, top-gate, and drain voltages. Using this distinctive feature, multiple logic gate operations could be achieved using only a single transistor. First, we exhibited five logic gate operations—AND, OR, NAND, NOR, and XOR—by adjusting the bottom-gate and top-gate voltages. Moreover, the drain voltage induced electrical switching between two logic gates, e.g., NAND/NOR and OR/ XOR.

Such logic gate operations are not obtainable in conventional transistors due to the monotonic increase in drain currents, which is a unique feature of our proposed DG-OAAT circuit. Therefore, we believe that our concept provides a promising perspective for attaining large-scale integrated organic electronic circuits.

2. Results and Discussion

2.1. Single-Gate Operations with a Dual-Gate Organic Antiambipolar Transistor

Figure 1a,b shows the device structure and an optical microscopy image of the DG-OAAT. A highly doped p-type Si (100) substrate (<0.01 Ω cm) was used as the common bottom-gate (BG) electrode. A patterned Au film was used as the top-gate (TG) electrode. In addition, hafnium oxide and fluoropolymer (CYTOP) were used as the standard BG- and TG-insulators, respectively. The Experimental Section describes the formation process in detail. For the transistor channels, α-sexithiophene (α-6T) and N,N-diocyl-t,4,3,4,10-perylenedicarboximide (PTCDI-C8) were employed as p-type and n-type semiconductors, respectively. The film thicknesses were optimized to be 15 and 8 nm for the α-6T and PTCDI-C8 films, respectively, so as to enhance the tunability of TG and BG electrodes for both channel layers. Atomic force microscopy measurements were performed; the results confirmed that both channels and the partially overlapped (PN stacked) region have smooth surface morphologies, as shown in Figure S1 in the Supporting Information. The channel width of the DG-OAAT was 360 ± 20 μm. The typical channel length of the DG-OAAT was 150 μm (100 and 120 μm for the α-6T and PTCDI-C8 channels, respectively, including the overlapped area).

First, we evaluated the basic single-gate operations of the DG-OAAT under BG or TG voltages. All the measurements were performed at room temperature under atmospheric conditions. Figure 1c shows a typical drain current (\(I_D\))-BG voltage (\(V_{G,\text{bottom}}\)) curve and the differential transconductance curve of the transistor in the case of p-type operation. The drain voltage \(V_D\) was fixed at −10 V, and the TG electrode was electrically floated. The BG transistor exhibited a Λ-shaped \(I_D\). Namely, \(I_D\) rapidly increased at \(V_{G,\text{bottom}} = V_{\text{on}} = −3.2\) V and then decreased with increasing \(V_{G,\text{bottom}}\). Consequently, \(I_D\) was completely suppressed at \(V_{G,\text{bottom}} = V_{\text{off}} = −5.7\) V. The peak drain current \(I_{\text{peak:bottom}}\) reached −21.5 nA at a peak voltage \(V_{\text{peak:bottom}}\) of −4.6 V. The peak width (ΔV) was defined as ΔV = \(V_{\text{on}}−V_{\text{off}}\), which was estimated to be 2.5 V. The corresponding NDT was visible, and the maximum value of NDT, \(g_{\text{max}}\), was obtained as −41.3 nS at \(V_{G,\text{bottom}} = −4.7\) V. In addition, the hysteresis in both curves was negligible in 77% devices (Figure S2, Supporting Information), which reveals that carrier trapping sites located at the interfaces of the BG insulating layer and the organic channels were marginal owing to CYTOP coating.

Surprisingly, similar \(I_D\) and NDT behaviors appeared even in the case of TG operation, although a broadening in the peak width (ΔV = 8.9 V) of \(I_D\) was observed (Figure 1d). Moreover, in this case, the hysteresis was marginal in both curves, even though the observation yield of the hysteresis-free transfer curves (17%) was lower than that in BG operation (77%) (Figure S3, Supporting Information). In addition, the same peak current \(I_{\text{peak:top}}\) (−21.9 nA) was obtained at \(V_{\text{peak:top}} = −4.3\) V, and \(g_{\text{max}}\) was calculated to be −12.5 nS at \(V_{G,\text{top}} = −4.9\) V. These parameters are comparable with those obtained in the case of BG operation, which is assumed to be because of the smooth surface morphologies of the α-6T and PTCDI-C8 channels (Figure S1, Supporting Information).

Notably, the transfer curves obtained during the BG and TG operations were stable; no change in \(I_{\text{peak}}\) values was observed even after 3 months. These results show the high stability of the DG-OAATs (Figure S4, Supporting Information).

Based on our previous studies and the other recent works,\[35–37,45–47\] the Λ-shaped \(I_D\) is interpreted by a similar analogy to that of the shoot-through current in a CMOS inverter. The equivalent circuits are depicted in Figure 1e. The DG-AAT can be regarded as a series circuit of p-type and n-type transistors, where the BG or TG works as a common gate electrode. Namely, the Λ-shaped \(I_D\) can be explained as the overlapped current of the two transfer curves of the α-6T and PTCDI-C8 transistors using the following equations:\[47\]

\[
I_{D,p} = -\frac{W}{2L_p} \mu_{p,\text{C}} (V_C - V_{\text{sh,p}})^2
\]

\[
I_{D,n} = -\frac{W}{2L_n} \mu_{n,\text{C}} (V_0 - V_C + V_{\text{sh,n}})^2
\]
where \( L_p \) and \( L_n \) are the channel lengths of the \( \alpha \)-6T and PTCDI-C8 films, respectively, \( W \) is the common channel width, and \( C_i \) is the capacitance of the insulator per unit area (125 and 64 nFcm\(^{-2} \) for the BG- and TG-insulators, respectively). \( \mu_p \) and \( V_{th,p} \) are the hole carrier mobility and the threshold voltage of the \( \alpha \)-6T transistor, respectively. \( \mu_n \) and \( V_{th,n} \) represent the electron carrier mobility and the threshold voltage of the PTCDI-C8 transistor, respectively. Importantly, \( V_{on} \) in the AATs corresponds to the threshold voltage \( V_{th,p} \) of the \( \alpha \)-6T transistor. Meanwhile, \( V_{off} \) is related to \( V_{th,n} \) of the PTCDI-C8 transistor \( (V_D + V_{th,n}) \).

We estimated the carrier mobilities \( \mu_p \) and \( \mu_n \) and threshold voltages \( V_{th,p} \) and \( V_{th,n} \) of the OAATs (13 devices formed on the same substrate) and compared them to those obtained from \( \alpha \)-6T and PTCDI-C8 transistors. The representative \( I_{D}-V_{G} \) curves of \( \alpha \)-6T and PTCDI-C8 transistors (Figure S5, Supporting Information). The extracted parameters are summarized in Table 1. The carrier mobilities \( \mu_p \) and \( \mu_n \) and the threshold voltages \( V_{th,p} \) and \( V_{th,n} \) of OAATs in BG operations closely coincide with those of the \( \alpha \)-6T and PTCDI-C8 transistors. The result provides clear evidence that the \( \Lambda \)-shaped \( I_D \) in OAATs is explained as the overlapped current of the two transfer curves of the \( \alpha \)-6T and PTCDI-C8 transistors with enhancement modes. However, the transistor parameters estimated for TG operation were not quantitatively consistent with those found in the constituent transistors. The hole and
electron mobilities ($\mu_p$ and $\mu_n$) of OAATs were lower than those of $\alpha$-6T and PTCDI-C8 transistors. In contrast, the threshold voltages ($V_{th,p}$ and $V_{th,n}$) of OAATs were reduced compared with those of both transistors. These discrepancies between TG and BG operations are caused by the complicated channel structure of OAATs. The staggered PN region would hinder carrier transport in TG operations for both carriers. In addition, the structure could induce inhomogeneous gate electric fields, resulting in variations of threshold voltages.

Based on the above discussion, we briefly discuss the conductive mechanism of the transistor. When $V_G$ is below $V_{on}$ (Figure 1e-i), the PTCDI-C8 channel is on state, while the $\alpha$-6T channel is off state. As a result, the total $I_D$ does not flow in the transistor. In the middle range ($V_{on} < V_C < V_{off}$) (Figure 1e-ii), the total $I_D$ flows because both transistors are active. For the further increment of $V_C$ ($V_{off} < V_C$) (Figure 1e-iii), $I_D$ is suppressed again because the PTCDI-C8 channel becomes off state, even though the $\alpha$-6T transistor is active. As a result, the appropriate energy-level offset of p- and n-type materials is required to induce the $\Lambda$-shaped transfer curve. In this regard, the material combination of $\alpha$-6T and PTCDI-C8 films is promising.

### 2.2. Dual-Gate Operations with a Dual-Gate Organic Antiambipolar Transistor

We then exhibited the dual-gate (DG) controllability of the drain currents in DG-OAATs. Figure 2a shows a comparison of the values of $I_D$ in the case of BG operation at two TG voltages ($V_{G:top} = 0$ and $-10$ V), where $V_D$ was fixed at $-10$ V. The $\Lambda$-shaped $I_D$ was clearly shifted by applying a $V_{G:top}$ of $-10$ V. As a result, $V_{peak:bottom}$ varied from $-5.4$ V (blue solid line) to $-4.4$ V (red solid line). Note that $V_{peak:bottom}$ differs from that in Figure 1c because TG was grounded in this measurement.

In the case of BG operation, $V_{on}$ and $V_{off}$ were plotted as a function of $V_{G:top}$ to clarify whether the shifted $V_{peak:bottom}$ originates from the variation in the $V_{th}$ values in the individual transistor channels. $V_{on}$ was changed from $-4.1$ to $-2.9$ V, where

|                | $\mu_p$ [cm$^2$ V$^{-1}$ S$^{-1}$] | $V_{th,p}$ [V] | $\mu_n$ [cm$^2$ V$^{-1}$ S$^{-1}$] | $V_{th,n}$ [V] |
|----------------|----------------------------------|----------------|----------------------------------|----------------|
| OAAT (bottom)  | $4.6 \pm 2.1 \times 10^{-2}$     | $-3.1 \pm 0.4$ | $1.3 \pm 0.7 \times 10^{-3}$     | $4.2 \pm 0.9$  |
| $\alpha$-6T (bottom) | $2.9 \pm 0.4 \times 10^{-2}$     | $-4.0 \pm 0.3$ | N/A                              | N/A            |
| PTCDI-C8 (bottom) | N/A                              | N/A            | $1.7 \pm 0.5 \times 10^{-1}$     | $5.5 \pm 0.7$  |
| OAAT (top)     | $1.0 \pm 0.5 \times 10^{-2}$     | $0.0 \pm 0.8$  | $2.9 \pm 1.8 \times 10^{-2}$     | $1.6 \pm 1.3$  |
| $\alpha$-6T (top) | $3.6 \pm 0.4 \times 10^{-2}$     | $-3.9 \pm 1.1$ | N/A                              | N/A            |
| PTCDI-C8 (top) | N/A                              | N/A            | $2.1 \pm 0.7 \times 10^{-1}$     | $5.3 \pm 1.0$  |

Figure 2. a) $I_D$–$V_{C:bottom}$ curves obtained at $V_{G:top} = 0$ and $-10$ V, where $V_D$ was fixed at $-10$ V. b) $V_{C:top}$ dependence of $V_{on}$ and $V_{off}$ in the DG-OAAT. c) 3D- and d) 2D-$I_D$ mappings as functions of $V_{C:bottom}$ and $V_{C:top}$. 

Table 1. The estimated carrier mobilities and threshold voltages of OAAT, $\alpha$-6T, and PTCDI-C8 transistors.
V_{G,top} was applied ranging from 1 to −11 V. Meanwhile, V_{off} was linearly varied from −6.6 to −5.1 V in the same voltage range. These variations of V_{on} and V_{off} well agree with those of the V_{th} of the respective channels (V_{th:bottom,6G} and V_{th:bottom,PtCDI:6G}) (Figure S6, Supporting Information). These results indicate that the shift in V_{peak:bottom} was caused by the changes in V_{on} and V_{off} in the case of V_{G,top}.

The 3D and 2D I_{D} mappings were demonstrated as functions of V_{G:bottom} and V_{G;top} respectively, as shown in Figure 2c,d, to evaluate the detailed variations in V_{peak:bottom} and I_{peak:bottom}. The Λ-shaped I_{D} was found to be obviously shifted by V_{G;top} (Figure 2c). In addition, V_{peak:bottom} linearly changed from −5.7 to −4.2 V in the V_{G;top} range of 1 to −11 V (Figure 2d). The maximum I_{peak:bottom} was found to be −33.8 nA at V_{G:bottom} = −4.9 V and V_{G;top} = −4.8 V. In addition, the change in I_{peak:bottom} was less than 30% under 10-cycles V_{G:top} sweep from 0 to −10 V (Figure S7, Supporting Information).

These results clarify that the transistor parameters in the case of BG operation, V_{peak:bottom}, V_{on}, V_{off}, and I_{peak:bottom} can be tuned by V_{G;top}.

2.3. Multiple Two-Input Logic Gate Operations based on a Dual-Gate Organic Antiambipolar Transistor

Based on the DG operation in the DG-OAAT, we demonstrated five two-input logic gate operations—AND, OR, NAND, NOR, and XOR—using only a single transistor. Here, V_{G:bottom} and V_{G;top} were used as two-input signals in the logic gates, which are denoted as V_{IN1} and V_{IN2}. The obtained I_{D} was monitored as an output signal (I_{out}).

**Figure 3** shows 2D-I_{D} mappings as functions of V_{IN1} and V_{IN2} for the five logic gates. The I_{D} mappings are exhibited in two colors (white and purple), which correspond to I_{out} = 0 (low state) or 1 (high state) with a critical current of 7.5 nA. When I_{out} is within the range of 0 nA < I_{D} < 7.5 nA, I_{D} is represented in white, i.e., I_{out} = 0 in the logic gate, whereas the purple color coincides with I_{out} = 1 (7.5 nA < I_{D} < 35.0 nA). The 2D-I_{D} mappings show that five logic gate operations are possible by just adjusting V_{IN1} and V_{IN2}.

Figure 3f–j shows actual logic gate operations for the two-input signals, V_{IN1} and V_{IN2}. All the logic gate operations are obviously demonstrated. For example, for the AND gate operation, a high state, “1,” was output in I_{out} only at (V_{IN1}, V_{IN2}) = (1, 1). However, I_{out} showed a low state, “0,” for the other combinations of input signals. In this manner, OR, NAND, NOR, and XOR were exhibited (Figure 3g–j). These results indicate that five logic gate operations, namely AND, OR, NAND, NOR, and XOR, can be achieved in only one transistor by adjusting V_{IN1} and V_{IN2}, which is in contrast to the current CMOS-based logic gates (e.g., 4 and 12 transistors are necessary for the NAND and XOR gates, respectively). Our finding is thus expected to attain multifunctional logic circuits by the integration of multiple logic gate functions into a single transistor.

---

**Figure 3.** a–e) 2D-I_{D} mappings as functions of two-input voltages, namely, V_{IN1} ( = V_{G:bottom}) and V_{IN2} ( = V_{G:top}), for the AND (a), OR (b), NAND (c), NOR (d), and XOR (e) logic gates. Here, V_{IN1} and V_{IN2} are defined as follows: {((V_{IN1} = 0, V_{IN2} = 0), (V_{IN1} = 0, V_{IN2} = 1), (V_{IN1} = 1, V_{IN2} = 0), (V_{IN1} = 1, V_{IN2} = 1))} for AND, {((-4.2, −5.2 V), (0, −6.0 V))} for OR, {((-4.7, −5.4 V), (−2.0, −9.0 V))} for NAND, {((-5.5, −6.4 V), (0, −10.0 V))} for NOR, and {((-4.3, −5.5 V), (0, −10.0 V))} for XOR. In addition, the current mappings are shown in two distinct colors (white and purple) with a threshold of 7.5 nA. f)–j) Five logic gate operations correspond to the 2D-I_{D} mappings in (a)–(e), where the output signal, “1” or “0,” is defined by an I_{D} value of above or below 7.5 nA.
Similar logic gate operations have been achieved using single-electron transistors (SET) with multigate configurations. In these cases, the A-shaped $I_D$ was obtained by the Coulomb oscillation in accordance with the gate voltage. Maeda et al. exhibited six logic gate operations using a DG-SET. In addition to the abovementioned five logic gates, the XNOR gate operation was realized by making active use of periodic peak $I_D$. Takahashi et al. reported an XOR gate by a multigate SET in the same manner. However, these device operations have been limited in cryogenic temperatures ($\approx 40$ K) because of the nature of Coulomb blockade behaviors. In contrast, our transistor enables multiple logic gate operations at room temperature, which is a large benefit with regard to using AATs for reconfigurable logic gates.

2.4. $V_D$-Induced Switching of Two Logic Gates

In organic AATs, the A-shaped $I_D$ is interpreted by the same mechanism as that of the shoot-through current of CMOS inverters. This means that the peak width ($\Delta V$) can be systematically tuned by $V_D$, even though the $V_{th}$ values in the constituent transistors are identical for the $V_D$ changes. We made use of this feature for the electrical switching of two logic gates, leading to the integration of additional reconfigurable logic functions.

Figure 4a shows $I_D-V_{G_{bottom}}$ curves with different $V_D$, where $V_{G_{top}}$ was fixed at 0 V. $V_{on}$ was found to be $-3.4$ V, and this value is completely constant, irrespective of $V_D$. This is because $V_{on}$ is equal to the $V_{th}$ of $\alpha$-6T ($V_{th_{\alpha-6T}}$) (Figure S8a, Supporting Information). In contrast, $V_{off}$ clearly shifted from $-6.5$ to $-8.2$ V in the $V_D$ range from $-10$ to $-12$ V, even though the $V_{th}$ of PTCDDI-C8 ($V_{thPTCDI-C8}$) is constant and independent on $V_D$ (Figure S8b, Supporting Information). The reason is that $V_{off}$ agrees with the difference of $V_D$ and $V_{th}$ of PTCDDI-C8, i.e., $V_{D}+\Delta V_{PTCDI-C8}$. Accordingly, $V_{off}$ and $\Delta V$ can be controlled by $V_D$, even though no changes were observed in $V_{th}$ in both the channel layers.

By taking advantage of the $V_D$ tunability of $\Delta V$, we demonstrated the electrical switching of two logic gates by only changing $V_D$. Figure 4b,c shows the 2D-$I_D$ mappings obtained at $V_D = -10.0$ and $-10.8$ V, respectively. The mappings were markedly changed by only a difference of 0.8 V (8%) in $V_D$. The slight difference in $V_D$ attained two logic gate switching: NOR ($V_D = -10.0$ V) and NAND ($V_D = -10.8$ V). The corresponding logic gate operations are represented in Figure 4d ({{$V_{IN1}$, $V_{IN2}$}} 1), {{$V_{IN1}$ 0, $V_{IN2}$ 1}} = {{-5.5, -6.4 V}}, (0, -10.0 V). At $V_D = -10.0$ V, $I_{out}$ only shows the “1” state in the case of ($V_{IN1}$, $V_{IN2}$) = (0, 0), which is NOR gate operation. In contrast, at $V_D = -10.8$ V, the “0” state is output in $I_{out}$ only at ($V_{IN1}$, $V_{IN2}$) = (1, 1), i.e., the NAND gate operation.

This finding can be applied to various types of electrical switching for logic gates by selecting suitable $V_{IN1}$, $V_{IN2}$, and $V_D$. Figure 5 indicates another example of $V_D$-induced logic gate switching. Here, the XOR and OR logic gates were electrically switched (Figure 5a,b) by changing the input voltages: ({{$V_{IN1}$ 0, $V_{IN1}$ 1}}), ({$V_{IN1}$ 0, $V_{IN2}$ 1}) = {{-4.3, -5.5 V}}, (0, -10.0 V). The $V_D$ of $-10.0$ V achieved XOR gate operation. Namely, “1” state was output in $I_{out}$ at the combinations of ($V_{IN1}$, $V_{IN2}$) = (0, 1) and (1, 0) (Figure 5c). Meanwhile, $V_D = -10.8$ V induced OR gate operation, where $I_{out}$ only showed the “0” state at ($V_{IN1}$, $V_{IN2}$) = (0, 0). Notably, all of these logic gate operations can be achieved even after 5 months, which shows the extremely high stability and reliability of our devices (Figure S9, Supporting Information).

3. Conclusion

We have achieved reconfigurable logic gate operations using a single DG-OAAT by controlling the following three input parameters: $V_{IN1}$, $V_{IN2}$, and $V_D$. By selecting suitable $V_{IN1}$ and $V_{IN2}$, it was possible to demonstrate five logic gate operations: AND, OR, NAND, NOR, and XOR. Moreover, the slight variation (8%) in $V_D$ made it possible to electrically switch two logic gates, such as NAND/NOR and OR/XOR. Such logic gate operations are not possible with conventional transistors with a monotonic increase in the drain currents, which is a unique feature of our logic circuits based on DG-OAATs. Additionally, all of these logic gate operations were achieved even after 5
months, showing the high stability of our devices. Therefore, we consider that the multifunctional logic circuits based on DG-AATs contribute to the drastic reduction of the number of transistors in current integrated circuits and that they can improve the capability of data processing. Thus, our device concept provides a promising way for realizing multifunctional logic circuits with a simple circuit design.

4. Experimental Section

**Formation of DG-AATs:** DG-AATs with α-6T and PTCDI-C8 layers were produced using vacuum-deposition techniques. A highly doped p-type Si (100) substrate (<0.01 Ω cm), which was employed as a common BG electrode in all the transistors, was chemically cleaned using Shiraki’s method, followed by the removal of a native oxide in a 5% HF solution. Subsequently, using an atomic layer deposition (ALD) system, a 30 nm-thick HfO2 film was deposited on the Si substrate as a BG insulating layer at a temperature of 175 °C, where tetrais(dimethylamino)hafnium (TDMAHf) and water were used as hafnium and oxygen sources. Then, a 15 nm-thick fluorocarbon polymer (CYTOP) (AGC chemical, CTL-809M and SOLV-180) was spin-coated to passivate the carrier trap sites on the HfO2 surface and facilitate the charge transport of the organic channels. Afterward, α-6T (15 nm) and PTCDI-C8 (8 nm) films were grown as p- and n-type organic channels using a thermal vacuum deposition technique at a background pressure of 10−7 Pa. It is worth noting that the two organic layers were partially overlapped in the transistor channel to form a heterointerface, which is the origin of A shapes in AATs. For the source and drain electrodes, 30 nm-thick Au films were then deposited using a thermal vacuum deposition system.

For the TG configuration, a CYTOP (20–30 nm) film was spin-coated on the top of the organic channels, followed by the deposition of an HfO2 (40 nm) layer as a TG insulator using the ALD method. It should be noted that the deposition temperature of the HfO2 layer was reduced to 120 °C to hinder the aggregation of the organic layers during the ALD process. Consequently, an Au TG electrode was patterned for each transistor via thermal vacuum deposition to complete DG-AAT.

The typical width and length of DG-AATs were 360 ± 20 and 150 µm, respectively.

**Transistor Measurements:** The transistor measurements of DG-AATs and the logic gate operations were performed using source measurement units (Keysight Technologies, B2912A and B2912B). For the capacitance–voltage measurements, a semiconductor device analyzer (Agilent, B1500A) was used to evaluate the capacitances of the TG and BG insulators. All the measurements were performed using a 4-probe system at room temperature under atmospheric conditions.

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

**Conflict of Interest**

The authors declare no conflict of interest.

**Data Availability Statement**

Research data are not shared.

**Keywords**

antiambipolar transistor, dual-gate organic transistor, negative differential transconductance, reconfigurable logic gate

Received: November 22, 2021
Revised: January 26, 2022
Published online: February 27, 2022

[1] J. Pei, L. Deng, S. Song, M. Zhao, Y. Zhang, S. Wu, G. Wang, Z. Zou, Z. Wu, W. He, F. Chen, N. Deng, S. Wu, Y. Wang, Y. Wu, Z. Yang, C. Ma, G. Li, W. Han, H. Li, H. Wu, R. Zhao, Y. Xie, L. Shi, *Nature* 2019, 572, 106.
[2] A. Sebastian, M. L. Gallo, R. Khaddam-Aljameh, E. Eleftheriou, *Nat. Nanotechnol.* 2020, 15, 529.
[3] D. Markovic, A. Mizrahi, D. Querlioz, J. Grollier, *Nat. Rev. Phys.* 2020, 2, 499.
[4] T. F. Schranghamer, A. Oberoi, S. Das, *Nat. Commun.* 2020, 11, 5474.
[5] C. Liu, H. Chen, S. Wang, Q. Liu, Y. G. Jiang, D. W. Zhang, M. Liu, P. Zhou, *Nat. Nanotechnol.* 2020, 15, 545.
[6] V. K. Sangwan, M. C. Hersam, *Nat. Nanotechnol.* 2020, 15, 517.
[7] P. A. Ersman, R. Lassnig, J. Strandberg, D. Tu, V. Keshmiri, R. Forchheimer, S. Fabiano, G. Gustafsson, M. Berggren, *Nat. Commun.* 2019, 10, 5053.
[8] H. Yoo, H. Park, S. Yoo, S. On, H. Seong, S. G. Im, J. J. Kim, *Nat. Commun.* 2019, 10, 2424.
