Research on Synchronous Rectification Driver Technology of High-Frequency DC-DC Resonant Converter Based on GaN Devices

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This work was supported in part by the Natural Science Foundation of Fujian Province under grant 2018J01756, and in part by the Scientific research project of Jinjiang Fuda science and Education Park scientific research project under grant 2019-JJFDKY-45.

ABSTRACT With the increase of switching frequency to tens of MHz, the synchronous rectification faces many new challenges, among which a significant one is the design of the driver circuit for the synchronous rectification with wide bandgap gallium nitride (GaN) devices. According to the self-resonant driving theory, this paper proposes an in-phase feedback synchronous rectification driver circuit (SRDC) based on GaN devices and the driver chip. In this SRDC, the nonlinear parasitic capacitors are replaced with external capacitors, and the synchronous driving signal is in-phase with the excitation source. The new scheme can provide precise driving timing, stable driving amplitude and flexible phase-shifting characteristics for the synchronous rectification of a high-frequency DC-DC resonant converter (HFDRC) based on GaN devices. In this paper, a detailed parameter design method is introduced by analyzing the characteristics of the feedback network. The feasibility and effectiveness of the proposed SRDC are verified on a 20 MHz prototype with 18 V input and 5 V / 2 A output.

INDEX TERMS external capacitor, gallium nitride (GaN), high frequency, synchronous rectification driver circuit (SRDC).

I. INTRODUCTION Increasing switching frequency of converters can significantly reduce the volume and weight of passive components, increase the power density and the dynamic response [1]-[4]. Recently, the application of wide bandgap devices [5], [6] has enabled the operating frequency of DC-DC power converters to tens of MHz. Among them, the high-frequency DC-DC resonant converter (HFDRC) has received much attention.

The HFDRC generally includes three parts: the inverter, the matching link, and the rectifier. At present, diodes are usually utilized in the rectifier of the HFDRC at dozens of MHz, causing significant power loss [7]. To solve this problem, synchronous rectification technology can be utilized.

The biggest challenge to introduce synchronous rectification technology into the HFDRC is the driving control of the synchronous rectifier (QSR). When synchronous rectification based on Si MOSFET is adopted, the driving modes mainly include square wave driving mode and resonant driving mode [8]. The loss of square wave driving mode is directly proportional to the operating frequency. As the operating frequency increases to tens of MHz, the loss of driver circuit will rises rapidly, making it difficult to apply in such a high frequency region. To reduce the driving loss, the QSR can be driven by a resonant driver circuit. There are two main types of resonant driver circuits: external resonant driver circuit and self-resonant driver circuit. Reference [9] introduced a two-way complementary external resonant driving mode for push-pull circuit. In a resonant converter operating at tens of MHz, the timing relationship between the main switch (Qmain) and QSR is not necessarily complementary; and it depends on the circuit parameters. Therefore, the resonant driving mode mentioned in [9] is not appropriate for synchronous rectification at high-frequency region.

To overcome the difficulty of controlling the timing between the Qmain and QSR, some scholars have proposed two self-resonant SRDC schemes for Si MOSFET. Reference [10] mentioned a self-resonant SRDC, whose excitation source is from the auxiliary winding of transformer. The auxiliary
winding can realize electrical isolation and achieve a satisfactory driving effect. Nevertheless, this method requires additional auxiliary winding, increasing the volume and design difficulty. Reference [11] illustrated a self-resonant SRDC in which the excitation source is the drain-source voltage of \( Q_{SR} \). The parasitic capacitor of \( Q_{SR} \) is applied to transmit the signal, whereas the amplitude and phase of the driving signal is adjusted by changing the parameters of other components in the feedback network. Due to the non-linearity of the parasitic capacitor of \( Q_{SR} \), the driving signal is unstable. If the gate source or drain source of \( Q_{SR} \) was paralleled with capacitors to obtain a stable driving signal, the working state of \( Q_{SR} \) would be affected. Thus, this self-resonant SRDC greatly limits the stability of the driving signal and the freedom in the feedback network design.

All the aforementioned researches mainly focus on the SRDC with Si MOSFET. Compared with Si MOSFET, GaN devices possess the advantages of low on-resistance, small gate charge, excellent switching performance, high current density, and high power density [12], [13]. Therefore, GaN devices are suitable for high-frequency applications at ten MHz and above [14]-[16].

As for power converters based on GaN devices, a reliable GaN driver is critical for maintaining stable operation [17], [18]. In recent years, many scholars have proposed new ideas or designs in response to the challenges of GaN devices, such as the stringent gate-source voltage limit, fast \( dv/dt \) behavior and high voltage drop during reverse conducting. Reference [19] introduced a synchronous gate driver with an adaptive detection function to ensure that the circuit achieves ZVS. Reference [20] proposed a high-voltage-level shifter with differential-mode noise blanking scheme, which can effectively improve the driving reliability of the converter in high-voltage and high-frequency occasions. Besides, reference [21] introduced a bipolar and a three-level gate drive voltage scheme, achieving a robust switching as well as low power losses during reverse conduction of the GaN device.

Currently, GaN devices are rarely used in MHz-level synchronous rectification circuits. However, with the advancement of wide bandgap devices and the increase in frequency and capacity, research in this area is urgently needed. Literature [22] reported an SRDC that combines the driver chip LM5114 with the second-order RC filter feedback network. A special phase shift is required in the feedback network to compensate for the long delays in the driver chip (typically 14 ns) and the comparator (9 ns). Nevertheless, this not only limits the switching frequency, but also increases the design complexity and reduces the flexibility of the feedback network design.

This paper proposes an in-phase feedback synchronous rectification driver circuit (SRDC) with external capacitors for GaN devices. Compared with the previous work, the proposed SRDC shows several advantages. Firstly, the sampling capacitors are separated from \( Q_{SR} \), so that driving performance of the rectifier stage will not be affected when adjusting the amplitude-frequency characteristics of the feedback network. Secondly, the SRDC keeps the excitation source signal and the synchronous driving signal, \( v_S \), in-phase, which greatly improves the flexibility of the feedback network design to adjust the amplitude-frequency characteristics of \( v_S \). Thirdly, the SRDC drives GaN devices efficiently and makes the on-resistance low. According to the data sheet of the GaN device we use, the gate-source voltage needs to be controlled between 4.5 V and 5.5 V during the on-time to ensure extremely low on-resistance [23]. While the proposed SRDC can output a square wave signal stabilized above 4.5 V by comparing \( v_S \) with the threshold voltage.

This paper is structured as follows. In Section II, the control method of the HFDRC and the applied rectifier are introduced; and the traditional SRDC is presented. The proposed SRDC is detailed in Section III. Section IV shows the experimental results based on the SRDC. Finally, the conclusion is presented in Section V.

II. HFDRC

A. CONTROL MODE OF HFDRC

For general power converters, the closed-loop control of the system is usually realized through pulse width modulation (PWM) [24] or pulse frequency modulation (PFM) [25], but neither of them is suitable for the HFDRC working at tens of MHz. The soft-switching characteristic of the HFDRC is achieved with a certain duty cycle. Under the PWM control method, the duty cycle of the switch is variable, causing the deterioration of the soft-switching characteristic and greatly increasing the switching loss. For the PFM control method, the frequency change of the system at high frequency requires an extremely fast response of the control system, which can be hardly fulfilled. Therefore, these two control methods are not suitable for HFDRCs.

The common control method for the HFDRC is hysteresis (ON-OFF) control [26], [27], which controls the enablement of the high-frequency driving signal through a low-frequency signal. Fig. 1 illustrates the operating principle block diagram of the HFDRC used in this paper, and Fig. 2 shows the main waveforms of ON-OFF control.
Its operating principle can be described as follows: the voltage dividing network samples the output voltage $V_O$, and then compares $V_O$ with the reference voltage $V_{ref}$ with the high-speed comparator. When $V_O$ reaches the upper limit voltage $V_{OH}$ set by ON-OFF control, the control signal $v_{ctrl}$ output by the comparator flips from high to low. On the one hand, $v_{ctrl}$ can control the driver chip of $Q_{main}$ with the high-speed optocoupler to prohibit the inverter from working. On the other hand, $v_{ctrl}$ makes $Q_{SR}$ turn off synchronously by controlling the SRDC. When $V_O$ decreases to the lower limit voltage $V_{OL}$, $v_{ctrl}$ changes from low to high. Then, the inverter and rectifier are re-enabled to work normally at 20 MHz and at the optimal working point to ensure that the converter works in the optimal resonant state, which is the prominent advantage of the ON-OFF control.

B. RECTIFIER OF HFDRC

In the HFDRC, the rectifier is designed to work in a resonant state to achieve zero-voltage-switching (ZVS) conditions for $Q_{SR}$. The rectifier in this paper adopts the current-source Class E rectifier [28], as shown in Fig. 3. Here, $I_{ac}$ is the input current source; $L_R$ is the resonant inductor; $C_R$ is the resonant capacitor, which absorbs the parasitic capacitor of $Q_{SR}$; $C_O$ is the output capacitor; and $R_L$ is the load resistor.

The operating mode of the rectifier can be divided into two different parts. When $Q_{SR}$ is on, all other components in the rectifier stage can be treated as short-circuited, so the equivalent impedance of the rectifier stage ($Z_{eq}$) can be seen as zero. When $Q_{SR}$ is off, the load and the filter capacitor are regarded as a constant voltage source, which can be regarded as short-circuited when analyzing $Z_{eq}$. At this time, $Z_{eq}$ can be considered as a branch that $L_R$ and $C_R$ connected in parallel [29].
For Si MOSFET operating at MHz level, the gate-drain capacitance $C_{gd}$ is usually not large. For example, $Q_{SR}$ SI7454DP used in [30] holds $C_{gd} = 72$ pF. If paralleling capacitor is added to the gate drain of $Q_{SR}$ to improve the driving capability, the gate-drain impedance will be reduced. Thus, the risk of coupling $V_{ds}$ to $V_{gs}$ will increase when $Q_{SR}$ turns on, resulting in a large loss in the driver circuit, unstable $V_{gs}$, and decreased switching speed. In addition, $C_{gd}$ and $C_{gs}$ vary non-linearly with the change of $V_{gs}$. As $V_{ds}$ resonates, the unstable $C_{gd}$ and $C_{gs}$ will bring instability to the feedback network. Therefore, the best choice would be adjusting the gain and phase shift of the feedback network by changing $L_g$. Nevertheless, a small difference of $L_g$ will lead to a drastic change in the amplitude and phase of $V_{gs}$ before the resonant point. To obtain the required phase of $V_{gs}$ by adjusting $L_g$ will likely cause drastic changes in the amplitude of the $V_{gs}$, which is not allowed for GaN devices. Moreover, driving GaN with a sinusoidal signal will not only increase the risk of breakdown, but also fail to keep the device in a low on-resistance state during the on-time.

III. ANALYSIS ON PROPOSED SRDC

In the HFDRC, the switching timing of $Q_{SR}$ needs to be strictly matched with the resonant state of the rectifier to achieve ZVS. The accurate switching timing of $Q_{SR}$ is obtained through careful design of the feedback network.

A. OPERATING PRINCIPLE OF PROPOSED SRDC

Aiming at the problem that the design flexibility of the feedback network in the traditional SRDC is limited by the parasitic parameters of $Q_{SR}$, this paper proposes an in-phase feedback SRDC with external capacitors. The circuit structure is demonstrated in Fig. 7. It consists of a driver chip LMG1020 and a feedback network that is composed of external capacitors $C_{S1}$ and $C_{S2}$, inductor $L_S$, resistor $R_S$, and DC bias source $V_{bias}$, where no additional comparator is required. Fig. 8 presents the time-domain relationship among the drain-source voltage of $Q_{SR}$ ($V_{ds,SR}$), $V_S$, and the gate-source voltage of $Q_{SR}$ ($V_{gs,SR}$). Among them, $t_{on, delay}$ and $t_{off, delay}$ represent the turn-on delay and turn-off delay of the driver chip (typical 2.5 ns), respectively; and $V_L$ and $V_H$ are the low-level threshold and high-level threshold of the driver chip, respectively.

The operating principle of the proposed SRDC is described as follows: the excitation source $V_{ds,SR}$ generates $V_S$ through the function of the feedback network. And $V_S$ goes to the inverting input of the driver chip, making $V_S$ in-phase with $V_{ds,SR}$, so that the operating frequency band is located after the resonant point. Meanwhile, the non-inverting input of the driver chip is enabled by the control signal $v_{ctrl}$ of the ON-OFF control system. The driving timing of $Q_{SR}$ is determined by $V_S$. As $V_S$ decreases from high to $V_L$, $Q_{SR}$ turns on after $t_{on, delay}$; and as $V_S$ rises from low to $V_H$, $Q_{SR}$ turns off after $t_{off, delay}$. The driver chip’s output, $V_{gs,SR}$ is close to a square wave, which ensures the low on-resistance of the GaN devices during the on-time.

In this work, $V_{bias}$ is generated by the voltage regulator chip LP3878MR-ADJ, which provides DC bias for $V_S$ to realize a flexible duty-cycle adjustment. The part-to-part variation of the driver chip can be compensated via fine-tuning $V_{bias}$. It is important that the amplitude of the $V_{bias}$ must be higher than $V_L$. Otherwise, $V_S$ will always be lower than $V_L$, making $Q_{SR}$ straight on.

B. FEEDBACK NETWORK OF PROPOSED SRDC
The feedback network controls the switching timing and duty cycle of \( Q_{SR} \) by adjusting the amplitude and phase of \( v_S \). \( v_S(t) \) includes the DC component, \( V_{bias} \) and the AC component, \( v_{S_{\text{ac}}}(t) \), as shown in (2):

\[
v_S(t) = V_{bias} + v_{S_{\text{ac}}}(t) \tag{2}
\]

To get the transfer function of \( v_{ds_{SR}} \) and \( v_S \), \( V_{bias} \) is set to zero in Fig. 7 to get the AC signal feedback network shown in Fig. 9.

The transfer function of \( v_{ds_{SR}} \) and \( v_S \) in Fig 9 can be derived as:

\[
\frac{v_S}{v_{ds_{SR}}} = \frac{s^2L_S C_{S1}}{s^2L_S (C_{S1} + C_{S2}) + s R_S (C_{S1} + C_{S2}) + 1} \tag{3}
\]

The phase of the transfer function given in (3) can be expressed as:

\[
\theta = \pi - \arctan \left[ \frac{\omega R_S (C_{S1} + C_{S2})}{1 - \omega^2 L_S (C_{S1} + C_{S2})} \right] \tag{4}
\]

It can be seen from (3) and (4) that \( L_S, C_{S1}, C_{S2}, \) and \( R_S \) influence the characteristics of the feedback network. The following is the analysis of the detailed effect of these parameters.

Fig. 10 shows the bode diagram of the feedback network with different \( L_S \). \( v_{ds_{SR}} \) and \( v_S \) have an in-phase feedback relationship. The operating frequency band locates after the resonant point. And the advantage is that the amplitude of \( v_S \) is not oversensitive to the changes in \( L_S \). As can be seen from Fig. 10, \( v_S \) can maintain a high and steady amplitude, whereas the phase shift becomes obvious as \( L_S \) changes in a relatively large range. By adjusting \( L_S \), the phase of \( v_S \) can be flexibly adjusted without causing drastic changes in amplitude.

Fig. 11 presents the bode diagram of the feedback network with different \( C_{S1} \). It can be found that the amplitude of \( v_S \) increases with the growth of \( C_{S1} \), but the phase is almost unchanged. Therefore, we can fine-tune \( C_{S1} \) to adjust the amplitude of \( v_S \) in a small range without changing the phase shift.

Fig. 12 provides the bode diagram of the feedback network with different \( C_{S2} \). Obviously, \( C_{S2} \) has a vital impact on the amplitude of \( v_S \). The larger the \( C_{S2} \), the lower the amplitude and the smaller the phase shift.
FIGURE 12. Bode diagram of feedback network with different $C_{S2}$.

FIGURE 13. Bode diagram of feedback network with different $R_S$.

Theoretically, the proper phase can be obtained by adjusting $R_S$. But the growth of $R_S$ also increases the driving loss. Hence, $R_S$ in series should not be too large.

From the above analysis, it can be seen that compared with the traditional SRDC, the sensitivity of $V_S$ to the components of the feedback network is greatly reduced. Proper amplitude and phase of $V_S$ can be realized by adjusting $L_S$, $C_{S1}$, $C_{S2}$, and $R_S$. This makes circuit calibration so much easier.

C. PARAMETER DESIGN METHOD

The transmission gain of the feedback network can be obtained by substituting $s = j\omega$ into (3):

$$
\frac{V_S}{V_{ds}} = \frac{-\omega^2 L_S C_{S3}}{1 - \omega^2 L_S (C_{S1} + C_{S2}) + j\omega R_S (C_{S1} + C_{S2})}
$$

(5)

By sorting out (4), the identity can be derived as follows:

$$
\omega R_S (C_{S1} + C_{S2}) = \left[1 - \omega^2 L_S (C_{S1} + C_{S2})\right] \tan(\pi - \theta)
$$

(6)

The expression of $L_S$ can be derived by substituting (6) into (5):

$$
L_S = \frac{K}{\omega^2 \left[ K (C_{S1} + C_{S2}) - C_{S1} \right]}
$$

(7)

where

$$
K = \frac{V_S}{V_{ds}} \sqrt{1 + \tan^2(\pi - \theta)}
$$

(8)

Combining (6) and (7), the expression of $R_S$ becomes as follows:

$$
R_S = -\frac{C_{S1} \tan(\pi - \theta)}{\omega (C_{S1} + C_{S2}) \left[ K (C_{S1} + C_{S2}) - C_{S1} \right]}
$$

(9)

From (6) and (7), it becomes obvious that for the determined gain and phase shift, $L_S$ and $R_S$ can be calculated when $C_{S1}$ and $C_{S2}$ are given.

At tens of MHz frequency, the capacitance and inductance are as low as pF and nH level, respectively. The parasitic parameters of traces and devices are in the same or close orders of magnitude. Therefore, it is important to minimize the loop area of the gate driver and pay attention to the grounding in PCB layout. For this reason, circuit debugging requires precise theoretical design guidance.

In addition, the chip used in the design has extremely low latency; and the comparator is eliminated. As the result, the converter can operate at very high frequency, while the chip delay can be compensated by fine-tuning the component parameters, which ensures the flexibility and convenience of the design.

IV. EXPERIMENTS

To verify the theoretical analysis, a 20 MHz prototype with 18 V input and 5 V / 2 A output is built. As shown in Fig. 14, the converter topology [31] contains an isolated Class Φ2 inverter and a current-source Class E rectifier, where GaN devices are used at both $Q_{main}$ and $Q_{SR}$. The air-core planar transformer [32] and the air-core inductor are also introduced. $Q_{main}$ chooses the external driving mode, and $Q_{SR}$ adopts the in-phase feedback SRDC with external capacitors. The experimental prototype is shown in Fig. 15.
The parameters of the SRDC are calculated with the proposed method in Section III C. The result is presented in Table 1. Table 2 exhibits the part numbers of $Q_{\text{main}}$ and $Q_{\text{SR}}$. And the values of the main circuit components are shown in Table 3. Among them, $L_{11}$, $L_{22}$, and $k$ are equivalent T-model parameters of the transformer, which are obtained by finite element simulation. $C_{ds}$ is the parasitic capacitor of $Q_{\text{main}}$.

**TABLE 1. Parameters of proposed SRDC.**

| Parameter | Value |
|-----------|-------|
| $C_{S1}$ | 227pF |
| $C_{S2}$ | 1047pF |
| $L_S$ | 82nH |
| $R_S$ | 3Ω |

**TABLE 2. Part numbers of $Q_{\text{main}}$ and $Q_{\text{SR}}$.**

| Component | Part number |
|-----------|-------------|
| $Q_{\text{main}}$ | GS61008T |
| $Q_{\text{SR}}$ | EPC2015C |

The non-inverting input of the driver chip is enabled by $v_{\text{ctrl}}$. When $v_{\text{ctrl}}$ is low, the driver chip no longer drives $Q_{\text{SR}}$ and the converter turns off. Meanwhile, $v_{\text{ds}, \text{SR}}$ gradually reaches the output voltage (5V). When $v_{\text{ctrl}}$ is high, the driver chip is re-enabled and $Q_{\text{SR}}$ continues to work at 20 MHz. Then, the converter turns on and quickly enters a steady state.
Fig. 18 shows $v_{ds\_SR}$, $v_{gs\_SR}$, and $v_S$ within switching cycle. It can be seen that the delay of the driver chip is compensated by the feedback network. $v_S$ is well-matched with the phase of $v_{ds\_SR}$ to control the driving timing, making $Q_{SR}$ turn on and turn off accurately and maintain its soft-switching characteristics.

The switching of $Q_{SR}$ under ON-OFF control requires fast dynamic response to establish a normal driving timing of soft switching. Fig. 19 and 20 show the waveforms of $v_{ds\_SR}$, $v_{gs\_SR}$, and $v_S$ when the converter is at start-up and shut-down, respectively.

It can be seen that the time from the resonant working state to the steady-state working state is about 100 ns during the start-up process of the converter. When the converter shuts down, the whole process takes about 350 ns. After entering the steady state, the driving timing sequence is accurate to keep an efficient and reliable operation of the rectifier.

In the construction of an isolated power converter operating at MHz, the design of the inverter is based on the feasibility of the rectifier. Only when the rectifier and its driver circuit are reasonable and effective, the inverter and the whole prototype can work normally. Fig. 21 shows the output voltage waveform of the prototype at full load. The output voltage of the prototype is stable at 5 V. The ripple peak-to-peak is approximately 300 mV. The prototype can work steadily under ON-OFF control.

Table 4 depicts the property comparisons of some typical high frequency topologies. It can be seen that the proposed converter has the lowest switch drain-source voltage stress. Even working at such a high frequency and at such a large input-to-output voltage ratio, the converter still possesses a satisfactory efficiency.
V. CONCLUSION

Due to the shortcomings of oversensitive parameter adjustment and unstable feedback network, the traditional SRDC is not suitable for synchronous rectification based on GaN devices at tens of MHz. This paper proposes a novel in-phase feedback SRDC with external capacitors which is suitable for GaN devices. The SRDC uses the external capacitors to sample the excitation source, and provides a stable and reliable driving signal by combining the self-resonant feedback network with the driver chip. Meanwhile, the operating frequency band is set behind the resonant point, which gives the feedback network plenty of gain margin and phase margin.

This paper thoroughly analyzes the operating principle and characteristics of the feedback network, and provides the detailed parameter design method. The experiment is carried out on a 20 MHz prototype with 18 V input, and 5 V/2 A output. The experimental result demonstrates that the proposed scheme can provide reliable and stable driving signal for synchronous rectification based on GaN at 20 MHz; and the prototype can work stably, which verifies the feasibility and effectiveness of the designed SRDC.

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### TABLE 4. Properties comparisons of some typical high frequency topologies.

| Topology      | $f_s$ | Input/output voltage | Output power | Isolation | Voltage stress | Efficiency |
|---------------|-------|-----------------------|--------------|-----------|----------------|------------|
| Proposed      | 20MHz | 18V/5V                | 10W          | Yes       | 2.3            | 78.4%      |
| Synchronous   | 10MHz | 12V/5V                | 10W          | No        | 3              | 79.5%      |
| Class $\Phi_2$|       |                       |              |           |                |            |
| Isolated      | 20MHz | 12V/5V                | 10W          | Yes       | 2.6            | 80%        |
| Class E [33]  | 20MHz | 36-54V/12V            | 24W          | Yes       | 2.8            | 77.5%      |
| Push-Pull     | 30MHz | 30-36V/24V            | 50W          | Yes       | 2.8            | 73.3%      |
| SEPIC [34]    | 30MHz | 15V/28V               | 25W          | No        | 3.5            | 82.5%      |
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