Inductance of superconductor integrated circuit features with sizes down to 120 nm

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Received 31 January 2021, revised 20 April 2021
Accepted for publication 25 May 2021
Published 23 June 2021

Abstract

Data are presented on the inductance of various features used in superconductor digital integrated circuits: microstrip and stripline inductors with linewidths down to 120 nm and different combinations of ground plane layers, effect of perforations of various sizes in the ground planes and their distance to the inductors on inductance, inductance of vias of various sizes between adjacent layers, inductance of composite vias between distant superconducting layers. Test circuits used for the measurements were fabricated in a new 150 nm node of a fully planarized process with eight niobium layers developed at MIT Lincoln Laboratory for superconductor electronics as well as in our standard SFQ5ee and SC1 fabrication processes with 250 nm minimum feature size. The new SC2 process utilizes 193 nm photolithography in combination with plasma etching and chemical mechanical planarization of interlayer dielectrics to define inductors with linewidth down to about 100 nm on critical layers. The standard processes use 248 nm photolithography. The measured data are compared with the results of inductance extraction using software packages InductEx and wxLC. Variations of circuit inductors caused by the fabrication processes are discussed. Magnetic flux trapping in ground plane moats and its coupling to nearby inductors are discussed for circuit cooling in a residual field of several configurations.

Keywords: superconductor electronics, superconductor integrated circuits, SFQ circuits, superconducting inductors, kinetic inductance, flux trapping

(Some figures may appear in color only in the online journal)

1. Introduction

Recent advances in fabrication technology have enabled reliable fabrication of superconductor integrated circuits with feature sizes down to 250 nm [1–6] and increased the scale of integration from about $10^6$ Josephson junctions (JJs) per square centimeter [5] to about $10^7$ JJs per square centimeter [6, 7]. Reduction of feature size allows for increasing the scale of integration, but introduces new design challenges: closely spaced superconducting wires become mutually coupled and can no longer be modeled as isolated circuit inductors. While strong mutual coupling is required in some cases, e.g. for compact transformers, it is usually undesirable and should be accounted for or mitigated. Accurate knowledge of inductances and coupling of various features comprising logic and memory cells is critical for designing superconductor very large scale integrated (VLSI) circuits, especially in the advanced processes.

The need for superconductor electronics (SCE) design automation (EDA) tools has stimulated development of numerical methods and inductance simulation software, initially for two-dimensional (2D) and later for 3D structures; see [8–17] and references therein. More recently, a more advanced 3D inductance extractor, InductEx has been developed and
became widely available [18, 19]. InductEx is based on the original FastHenry approach [11, 20] and uses a finite element method for solving the Maxwell’s and London equations for magnetic field and electric current distributions in a superconducting circuit. Recently, this approach based originally on rectangular filaments (rectangular mesh) was extended to tetrahedral volume elements (triangular mesh) [21]. A different approach was developed by Khapaev [13–17], which is based on minimization of the total energy functional and solving the London equations written for the so-called stream functions instead of electric current. Using direct boundary element method, it allows for numerical extraction of inductance, capacitance, and wave impedance of conductors which are uniform in one direction but of arbitrary cross section [13]. The corresponding modeling programs are known as wxLL for inductance and wxLC for inductance, capacitance, wave impedance, and propagation speed extraction.

A large amount of work has been done recently to characterize inductance of various structures typically encountered in integrated circuits fabricated by various fabrication processes and to compare the results with 3D inductance extraction [22–25], usually obtaining a satisfactory agreement. However, the size of the superconducting features studied was relatively large, about 1 µm and larger, due to limitations of the fabrication processes used. Therefore, they do not capture and represent the peculiarities of the very dense VLSI circuits using deep sub-micrometer feature sizes and spacing.

Previously, we reported on inductance and mutual inductance of Nb thin-film circuit inductors with linewidth down to 250 nm [26, 27] fabricated in the SCE fabrication process titled SFQ5ee developed at MIT Lincoln Laboratory (MIT LL) [28, 29]. We obtained a good agreement, within about 5% for the whole range of linewidths, between the measured self-inductances of straight line microstrip and stripline inductors and the extraction results using inductance extractor wxLL [13] with no fitting parameters. The agreement was somewhat worse with InductEx extraction using rectangular meshing. Agreement between the measured and extracted mutual inductances was noticeably worse in all studied cases [27].

More recently, agreement between InductEx extraction results and self-inductance measurements on microstrip and stripline inductors fabricated in the SFQ4ee [28] and SFQ5ee [29] processes was improved by calibrating InductEx [30], i.e. by adjusting the software model settings for each circuit layer, e.g. the number and size of filaments, the value of magnetic field penetration depth, \( \lambda \), interlayer dielectric thickness, \( d \), etc., to obtain the best overall agreement with the measurements [31]. The measurements were done on 12 structures involving 12 combinations of the eight niobium layers available in the SFQ5ee process stack, and with 1.2 µm linewidth, a much larger feature size than used in [26, 27]. Although an overall agreement for structures with this particular linewidth was improved to about 1% according to [31], the calibration procedure involved dozens of free fitting parameters, e.g. values of \( \lambda \) and dielectric thicknesses which, unfortunately, were not constrained by independent physical measurements.

In this work, we present self-inductance measurements of inductors with linewidths from 4 µm down to 100 nm, especially concentrating on the 120–250 nm linewidth range which is intended for the use in advanced fabrication process nodes described in [5] and section 2.1. In order to remove any ambiguity, the thicknesses of all metal and dielectric layers used in test structures and their linewidths were measured, and these actual thicknesses were used in the software layer definition file (LDF) for inductance extraction. Section 2 describes circuit fabrication, test structures used, and the method of measurements as well as effects of the fabrication process parameter variations on inductance. In sections 3 and 4, we present inductance data for various structures, effect of perforations in the ground planes—long moats of various width—on inductance, and characterize inductor–moat coupling at various distances. Results of measurements are compared with inductance extraction software wxLL and wxLC [13], and InductEx [19].

In section 5, we present measurements of inductance of interlayer vias for sub-micrometer dimensions, an essential feature of integrated circuits in modern fabrication processes [5]. In section 6 we briefly discuss the inductance of thin-film resistors used for resistive shunting of JJs. Section 7 discusses magnetic flux trapping in ground plane moats and its coupling to adjacent inductors for various protocols of field cooling of superconductor circuits.

Mutual inductance of various features used in superconductor integrated circuits is a subject of a separate work and will be presented elsewhere.

2. Fabrication process, circuits, and measurements

2.1. Description of fabrication processes

Fabrication processes SFQ5ee and SC1 developed at MIT LL for SCE were described in [5, 28, 29]. They are based on patterning niobium layers, labeled hereafter Mi (\( i = 0, 1, \ldots \)), with 248 nm photolithography and high density plasma (HDP) etching, with subsequent planarization of each layer. Planarization involves depositing a thick SiO2 layer and its chemical–mechanical polishing to obtain a smooth planar surface and the desired thickness of the interlayer dielectric labeled as \( I_i \).

After etching contact holes in the dielectric layer \( I_i \), the next Nb layer, \( M_i + 1 \), is deposited, filling the etched contact holes, to form superconducting vias between layers \( M_i \) and \( M_i + 1 \). These vias are also labeled \( I_i \).

The difference between the SC1 and the SFQ5ee processes is in the location of the JJ layer, J5 in the process stack—it is the fifth Nb layer in the SFQ5ee and the second in the SC1 process. For design compatibility, we preserved the same layer notations in both processes, starting Nb layer count from M0 in the SFQ5ee and from M4 in the SC1. We use the same notations for the dielectric layers, e.g. I4, and for the features patterned in these layers, e.g. I4 vias formed after etched contact holes in I4 dielectric are filled with Nb of the next metal layer, M5.
The minimum linewidth and spacing achievable in the SFQ5ee and SC1 process are limited by multiple processes to 250 nm. Without using expensive advanced processing techniques such as optical proximity correction, multiple exposure, phase-shifting masks, etc, 248 nm photolithography restricts the accurate definition of smaller features. Additionally, uniformly filling spaces between etched metal features with SiO₂ dielectric becomes increasingly challenging at s below ∼250 nm due to limitation of the low-temperature plasma-enhanced chemical vapor deposition (PECVD) of SiO₂.

To alleviate resolution limitations, the SC1 process has been recently modified to include a 193 nm photolithography using an ASML PAS5500-1100 scanner [32] to pattern a layer of JJs, J5, and critical layers of inductors, whereas keeping the rest of the fabrication process identical to the SC1. This resulted in a new node, titled SC2, with 150 nm minimum linewidth for critical inductors and 500 nm minimum diameter of JJs in circuits. For further development, the minimum linewidth in inductor designs used in this work was 120 nm, and the minimum pitch (linewidth plus spacing) for dense inductors was 370 nm.

Transitioning from 248 nm lithography to 193 nm photolithography enables the fabrication of smaller features, but introduces new fabrication challenges. The etch rate of photoresists used for 193 nm photolithography is higher, and selectivity to Nb is lower, than that of 248 nm photoresists. This necessitates the use of a hard mask process [32], shown schematically in figure 1. Changing multiple critical fabrication processes required reevaluation and calibration of circuit structures, including inductors. Target (nominal) thicknesses of all layers in the SFQ5ee and the SC1/SC2 processes used in this work are given in table 1.

![Figure 1](image1.png)

**Figure 1.** Hard etch mask process used for definition of the critical Nb layers in the SC2 process employed in this work. The image formed in the photoresist was initially transferred onto a thin, about 70 nm, SiO₂ layer deposited over the Nb layer. Thus formed trilayer mask comprised SiO₂ layer, bottom antireflection coating, and photoresist was then used as an etch mask capable to withstand etching of 200 nm thick niobium features.

![Figure 2](image2.png)

**Figure 2.** Circuit diagram (left) and layout (right) of one unit of inductance measurement circuit, after [26]. The circuit comprises N such units, N SQUIDs, each formed by identical JJs J₁ and J₂, biased from a common bias rail I_bias via bias resistors R. SQUID output voltage, V_out, is measured as a function of magnetic bias current I_mag which is fed into both arms of each SQUID via identical resistors, R dividing the current equally between 2N inductors. The period ΔI_mag of SQUID voltage modulation V_out(I_mag) is used to calculate the difference of the inductances of the right L_right and left L_left arms of the SQUID from equation (1). If the arms, e.g. stripline inductors, differ only by the length, this differential method eliminates parasitic contributions, L_p associated with the inductors’ connections to the ground and to the junctions J₁ and J₂. The distance between L_left and L_right is 20 μm. The vertical size of the structure and the length of L_right were increased in order to increase the linewidth of the inductors. Vertical stripes on the sides of the inductors are metal fill structures assisting planarity in chemical mechanical planarization (CMP). The closest fill structures are 4 μm away. Their presence was explicitly accounted for in the simulations and found to have no effect at these distances on any of the measured and simulated self-inductances.

### 2.2. Self- and mutual inductance measurements

Inductance and mutual inductance measurements of various features were done using a superconducting quantum interference device (SQUID) method [33] and an integrated circuit developed in [26] for a parasitic-free extraction of self- and mutual inductances using a differential method. The typical circuit diagram and a fragment of the circuit layout are shown in figure 2. Two inductors, L_left and L_right, of the type under test form two arms of a dc SQUID. Equal currents were fed into the both arms from the common magnetic bias rail, I_mag, using two identical thin-film resistors, R, 10 μm long and 20 μm wide. Large dimensions of the resistors in comparison with the fabrication process spread of the resistor width with standard deviation σ ≤ 50 nm were used to guarantee equality of their values with better than 1% accuracy. Inductors L_left and L_right were placed 20 μm apart so their mutual coupling could be completely neglected. They differed only by the length, being identical in all other respects.

From the period of SQUID modulation, ΔI_mag, we extracted the difference of inductances of the SQUIDs arms:

\[
L = 2N\Phi_0/\Delta I_{mag}, \tag{1}
\]
where $L = |L_{\text{right}} - L_{\text{left}}|$ and $N$ is the number of SQUIDs connected to the common magnetic bias $I_{\text{mag}}$. This differential method allowed us to eliminate parasitic inductance, $L_p$ associated with connection of the inductors under test to the bare SQUID on one end and to the ground plane(s) on the other end. If $\Delta I_{\text{mag}}$ is measured with 1% accuracy and the resistors are identical within 1%, the accuracy of this method can be estimated as 1.4%.

Similarly, a mutual inductor, $L_M$ was placed parallel to the inductor $L_{\text{right}}$, and a modulation current $I_{\text{mod}}$ was fed into it from a separate current source, figure 2. Mutual inductance, $M$ of the two inductors determines the period of the SQUID modulation, $\Delta I_{\text{mod}}$. The circuits contained 24 dc-SQUID-based test structures per chip, grouped with $N = 6$, and allowed to extract self-inductances of 24 inductors and mutual inductances of 24 pairs of inductors.

In all cases, the differential length, $l$ of the individual inductors and the mutual running length of the parallel signal conductors in coupled inductors, $l_M$ was made much larger than the inductor width, $w$, and the spacing, $s$, between the coupled inductors, typically $l \sim 100w$, 100s. For instance, for all inductors with linewidth $w \leq 0.25 \mu m$, we used $l = l_M = 30 \mu m$, and longer (up to 100 $\mu m$) for larger linewidths. This allowed us to neglect the edge effects of narrow, 0.25 $\mu m$, perpendicular wires feeding current into $L_M$. It is convenient to characterize long and uniform inductors by the self- and mutual inductance per unit length, $\ell = L/l$ and $m = M/l_M$, and use simulations based on an infinite line approximation, e.g. wxLL or wxLC [13], for comparing the results. For comparison with InductEx, which is a full 3D inductance extractor, the actual layout of inductors in GDSII format was used. To characterize agreement between the simulated and measured data spanning a very large range of values, we used the mean absolute deviation (MAD) defined as $\chi = 100 \% \times n^{-1} \sum_i |1 - y_i/x_i|$, where $x_i$ and $y_i$ are the measured and simulated values, respectively, and $n$ is number of data points.

Hereafter, we use notations M#aM#, e.g. M6aM4, for microstrips, where the first M# indicates the signal conductor layer, M6, placed above the ground plane indicated by the second M#, M4. Inverted microstrips are labeled as M#bM#, e.g. M6bM7 indicates the signal conductor on layer M6 placed below M7 ground (sky) plane. Similarly, various striplines are referred to by indicating firstly the signal conductor and then the two ground planes, e.g. M6aM4bM7 refers to a stripline with signal conductor formed on the layer M6, which is placed above M4 and below M7 ground planes. In all stripline cases, these two ground planes were connected together around their edges far away from the two inductors in figure 2 and at their grounded ends, using superconducting vias. This created a box-like shielding configuration.

### 2.3. Variations of process parameters and inductance

All actual process parameters such as dielectric, $d$, and metal, $t$, thicknesses, and inductor linewidth, $w$, may deviate somewhat from the process targets (nominal parameters), varying within some ranges, $\pm \Delta w_{\text{max}}, \pm \Delta d_{\text{max}}, \pm \Delta t_{\text{max}}$. These process deviations cause deviations of inductances from their nominal (designed) values and variations across chip, chip-to-chip, and wafer-to-wafer, affecting circuit margins and circuit yield.

### Table 1. Target thicknesses of process layers.

| Layer   | SFQ5ee (nm) | SC1/SC2 (nm) | Comments                  |
|---------|-------------|--------------|---------------------------|
| M0–M3  | 200         | n/a          | Not used in SC1/SC2       |
| I0–I3  | 200         | n/a          | Not used in SC1/SC2       |
| M4     | 200         | 200          | Bottom ground plane       |
| R4     | n/a         | 40           | Planarized resistor in SC2|
| I4     | 200         | 260          | Between M4 and M5         |
| M5     | 135         | 135          | JJ bottom electrode       |
| J5     | 250         | 200          | JJ top electrode          |
| I5     | 280         | 260          | Between M5 and M6a        |
| R5     | 40          | n/a          | Not planarized resistor   |
| M6     | 200         | 200          | Critical layer in SC2     |
| I6     | 200         | 200          | Between M6 and M7         |
| M7     | 200         | 200          | Top ground plane in SFQ5ee|
| I7     | 200         | 200          | Chip passivation in SFQ5ee|
| M8     | 250         | 200          | Pt/Au pad metallization in|
| I8     | n/a         | 200          | Between M8 and M9         |
| M9     | n/a         | 200          | Nb layer in SC1 and SC2   |
| J9     | n/a         | 200          | Was used as passivation   |
| M10–M11| n/a         | 200          | Not used in this work     |
| PAD    | n/a         | 250          | Pt/Au pad metallization   |

a Thickness of Nb metal remaining after anodization of the Nb/Al bilayer.
b Total thickness from metal to metal, including anodized surface of M5.
These effects can be simulated [34] and taken into account in circuit design and margin optimization, similar to how this is done in semiconductor industry EDA tools.

It is important to distinguish between the effects of shifts in the parameter mean values, which usually have some reproducible distribution across the wafer (global variation), e.g. reflecting film deposition or CMP uniformity, and the effects of random statistical variations around the mean values. The former can be easily modeled whereas modeling the latter requires knowledge of statistical distributions of the parameters. Due to the nature of many processing tools and various process controlling feedbacks employed in the wafer fabrication, these distributions do not have to be Gaussian, and their extraction requires extensive measurements. Alternatively, it may be easier to measure the resultant inductance statistic and use it in EDA tools.

We consider here the effect of global shifts of the process parameters and discuss inductance statistics in III. As an example, let us consider a symmetric stripline M1aM0bM2 which is often used as a passive transmission line (PTL) for Data and Clock signals in SFQ circuits usually requires ferritic waves, $v_{\text{ph}}$ in wide transmission lines of these types is $c/\sqrt{3}$, where $c$ is the speed of light in vacuum. Transferring Data and Clock signals in SFQ circuits usually requires PTL with $Z = 8.0 \, \Omega$ in order to match the typical impedance of resistively shunted JJs in PTL drivers and receivers in the SFQ5ee process. For symmetric M1aM0bM2 striplines, this value is obtained at $w = 2.82 \, \mu m$, giving $v_{\text{ph}} = 0.324 c$.

3. Inductance results for the SFQ5ee process

3.1. Inductance of isolated microstrips and striplines

Inductance of M1aM0bM2 striplines and M1aM0 microstrips is shown in figure 4 as a function of linewidth of the signal conductor, for a randomly selected run of the SFQ5ee process, SFQ523181, wafer #5 (w5). The data are shown for nine locations corresponding to the locations of process control monitor (PCM) chips with inductance test structures on 200 mm wafers. These locations are marked on a $7 \times 7$ stepper exposure grid ($A, B, \ldots G; 1, 2, \ldots 7$). The inductance per unit length, $L/I$ extracted using wxLC [13] software is shown by the solid red and blue curves, corresponding to $\lambda = 90$ nm. Also shown by solid black lines is the extracted capacitance $C/I$ per unit length, linearly increasing with $w$. The wave impedance $Z = (L/C)^{1/2}$ for both types of the transmission lines is shown by dash–dot curves. For capacitance extraction, we used a relative dielectric permittivity $\varepsilon = 4.6$ for the PECVD SiO$_2$ interlayer dielectric in the SFQ5ee process, which was obtained from resonance frequency measurements of microstrip and stripline resonators [36].

With these parameters, the value of $Z$ (in ohms) for the microstrips and striplines with $w > 0.4 \, \mu m$ is approximately equal to their linear inductance (in pH/um) multiplied by 97. This means that the propagation speed of electromagnetic waves, $v_{\text{ph}}$ in wide transmission lines of these types is $c/\sqrt{9.7} = 0.32 c$, where $c$ is the speed of light in vacuum. Transferring Data and Clock signals in SFQ circuits usually requires PTL with $Z = 8.0 \, \Omega$ in order to match the typical impedance of resistively shunted JJs in PTL drivers and receivers in the SFQ5ee process. For symmetric M1aM0bM2 striplines, this value is obtained at $w = 2.82 \, \mu m$, giving $v_{\text{ph}} = 0.324 c$. 

![Figure 3. Effect of process parameter deviations, $\Delta w$, $\Delta d$, and $\Delta t$ on the inductance of a M1aM0bM2 stripline with parameters: width $w = 250 \pm 25 \, \mu m$, dielectric thickness $d = 200 \pm 30 \, \mu m$, Nb film thickness $t = 200 \pm 10 \, \mu m$. The numbers on the cube surface show the percent change in inductance per unit length ($L/I$) at $L_0$, the location for the nominal (unperturbed) parameters. Critical corners corresponding to the largest inductance deviation in the space of process parameter deviations are marked. The simulations were done using a very accurate inductance extractor wxLL [13] and $\lambda = 90$ nm.](image-url)
The overall agreement between the measured inductance and the simulations using $\lambda = 90$ nm and the nominal thickness of the layers is very good, the cumulative MAD is $\chi = 3.3\%$ and $5.9\%$ for all microstrip and stripline inductors measured on the wafer, respectively. However, location D4 corresponding to the center of the wafer has systematically larger inductance values than the simulated ones both for M1aM0 microstrips and M1aM0bM2 striplines. For example, $\chi \approx 11\%$ for the microstrips at D4, almost three times as large as at any other location. Also, inductance at D4 is systematically larger than at the other locations. This is especially clear from the wafermaps in figure 5 showing inductance of M1aM0bM2 striplines with $w = 0.35$ $\mu$m, the minimum linewidth allowed by the Design Rules of the SFQ5ee process, and with $w = 1.0$ $\mu$m. The wafermaps for all other linewidths are very similar and we do not present them to save space. In figure 5, inductance of microstrips and striplines near the center of the wafer is, respectively, about $8\%$ and $13\%$ higher than at other locations of the PCM chips. Since this increase is nearly independent of the linewidth, it reflects changes in the effective ‘magnetic thickness’ $d + 2\lambda$ because the relative effect of linewidth deviations on inductance diminishes as approximately $-\Delta w / \Delta w$ at large $w$ and should be negligible for $w > 0.7$ $\mu$m.

The effect of $d$ and $\lambda$ deviations on wide microstrip inductors is about $\Delta L / L = (\Delta d + 2\Delta \lambda)/(d + 2\lambda)$. So, an $8\%$ elevation of the inductance of M1aM0 microstrips in the central part of the wafer indicates a value of effective ‘magnetic thickness’ $d + 2\lambda \sim 410$ nm instead of the nominal value of 380 nm. However, dielectric thickness measurements do not show elevated values in the central part of the wafer or a radial variation of $d$. Therefore, we are left to suggest that $\lambda$ is larger in the
central part of the wafer than at other locations. We can minimize MAD at location D4 by increasing $\lambda$ to 96–98 nm; see dash curves in figure 4. This results in $\chi \approx 4\%$ and $\approx 2\%$, respectively, for the microstrips and striplines at D4, a factor of three reduction in comparison to the simulations with $\lambda = 90$ nm, but significantly increases $\chi$ at all other locations.

A center-to-edge radial dependence and rotational symmetry of various thin film properties are typical for many fabrication processes using thin film deposition and etching tools. For instance, sheet resistance of Nb films, residual stress, tunnel barrier resistance of Nb/Al–AlO$_x$/Nb junctions, Josephson critical current density, all show similar wafermaps with nearly rotational symmetry and a radial dependence [5]. Similarly, $\lambda$ appears to be larger in the central part of the wafer where residual stress in the Nb films was found to be close to zero or slightly tensile [5]. Penetration depth appears to be smaller outside of the central part, in the region where the residual stress was found to be strongly compressive [5]. From the microscopic theory [38], $\lambda$ is expected to decrease with increasing electron scattering, e.g. caused by lattice compression, and to increase with increasing electron scattering rate, i.e. with increasing the film resistivity. The observed changes in $\lambda$, as reflected by wafermaps in figure 5, agree with these trends. Direct measurements of $\lambda$ dependence on residual stress in Nb films would be required to confirm this explanation. CMP processes may skew rotational symmetry of the deposited dielectric and contribute somewhat to the skew in inductance wafermaps in figure 5.

Keeping inductance of various structures on target in a broad range of linewidths and for inductors formed on multiple superconducting layers is a challenging task because of the dependence on many fabrication parameters. However, this is important for providing high yield and preserving operating margins of superconductor VLSI circuits because of their high sensitivity to global and local variations of inductors. Figure 6 shows results of inductance tracking for M1aM0bM2 striplines on wafers fabricated in the SFQ5ee process since September 2017 and includes data on 32 tested wafers. By solid lines are shown the process target values for striplines on six different widths, corresponding to the simulated values shown in figure 4. The averaged data for each wafer are shown. Due to the described above systematic inductance elevation on the central die D4, this die was excluded from the wafer averages.

If we characterize wafer yield based on the stripline inductance falling within a $\pm 10\%$ band centered on the target values, shown by dashed lines in figure 6, the yield is: 100% for $w = 2 \mu$m; 97% for $w = 1 \mu$m; 91% for $w = 0.7 \mu$m and $w = 0.5 \mu$m; and falls to 84% for $w = 0.35 \mu$m. This is why the minimum recommended linewidth for inductors on the M1 layer was set to be $0.5 \mu$m in the Design Guide for MIT LL fabrication process SFQ5ee_v.1.3 [39], which we maintain for a number of users and for IARPA SuperTools program focused on the development of EDA tools for SCE [40]. This minimum recommended linewidth for inductors in integrated circuits is much larger that the physical resolution of the process, which for isolated wires is about 150 nm. Nevertheless, by carefully adjusting and controlling the photolithography process, much smaller linewidths than the minimum recommended can be defined and studied as described in the next section.

3.2. 200 nm microstrips: effect of dielectric thickness

Linear microstrips with $w = 200$ nm were formed on a single Nb layer, layer M6, which is typically used for critical inductors in the SFQ5ee process. Superconducting layers below M6 were used as various ground planes to create microstrips M6aM0, M6aM1, M6aM2, etc, differing by the dielectric thickness between the ground plane and the signal conductor, according to the SFQ5ee process. The obtained dependence of the M6 microstrip inductance on the dielectric thickness, $d$ above the ground plane is shown in figure 7.

A simulated, using wxLL software [13] and $\lambda = 90$ nm for all Nb layers, dependence of the $L/d$ on $d$ is shown in figure 7 by a solid line. It provides a perfect description of the measured data for microstrips M6aM5, M6aM4, M6aM3, and M6aM2. However, the difference between the simulated and measured data increases progressively with increasing $d$ in the row of M6aM2, M6aM1, and M6aM0 microstrips, reaching about 7% for the M6aM0 microstrips.

An often-used analytical expression for microstrip inductance derived by Chang [8, 9]:

$$L/l = \mu_r \mu_0 (d + 2\lambda)/wK(w, d, t)$$

is valid only for $w/d \gtrsim 1$ or $d \lesssim 0.2 \mu$m in our case. It is not applicable to the studied here range of thicknesses and narrow linewidths important for integrated circuits and corresponding to $0.7\gtrsim w/d \gtrsim 0.09$ in figure 7. Here $\lambda = \lambda_0 \coth(t/\lambda_0)$ is the thin film penetration depth, $\lambda_0$ the magnetic field penetration depth in bulk niobium, $\mu_r$ the relative magnetic permeability ($\mu_r = 1$ is used hereafter), $\mu_0$ magnetic permeability.
of vacuum, and $K(w,d,t)$ is a fringe factor strongly depending on the microstrip aspect ratios $w/d$ and $t/d$ [8, 9]. Expression (2) is plotted in figure 7 by a dash–dot curve. It agrees with the numerical simulations in a narrow range $0.1 \mu m \leq d \leq 0.2 \mu m$, corresponding to $2 \geq w/d \geq 1$, and significantly overestimates inductance (underestimates fringing) as $d \to 0$ because of $t/d \to \infty$.

For a comparison, we developed a simple analytical expression for the inductance of the studied microstrips, approximating their nominally square cross section with $w = t = 2\lambda$ by a circular wire of the same area, radius $r = (w t / \pi)^{1/2} = 0.113 \mu m$. Then, assuming a uniform current distribution in the wire and integrating magnetic flux density, we obtained [41]:

$$L/t = \mu_{0}(2\pi)^{-1} \ln [2(d + r + \lambda)/r] + \mu_{0}(8\pi)^{-1} + \mu_{0}\lambda_{t}^{2}/(tw)$$  \hspace{1cm} (3)$$

The best agreement with the numerically extracted inductance is achieved if we take their sum to be $0.29 \mu H/\mu m$ instead of $0.3045 \mu H/\mu m$ calculated above.

The fabrication process of M6aM2, M6aM1, and M6aM0 microstrips requires etching away of, respectively, three, four, and five Nb layers in the stack above the ground plane and filling the volume of each removed layer with a planarized SiO$_2$ dielectric. Hence, a possible explanation of the observed deviations in their inductance would be that the actual dielectric thickness is lower than the nominal thickness $d$ used in simulations, e.g. due a dishing of the SiO$_2$ interlayer dielectric during CMP in areas with removed metal layers. This assumed thickness difference should be quite significant because of a weak, logarithmic, dependence of inductance on $d$, see equation (3). For instance, matching the measured and simulated data for M6aM0 microstrips would require the $d$ to be about $1.65 \mu m$ instead of $2.215 \mu m$ nominal thickness. However, scanning electron microscope (SEM) measurements on cross sections of the inductors, made by a focused ion beam (FIB), did not show any significant deviations in the dielectric thickness. The measured $d$ between the M6 strip and M0 ground plane was 2.33 $\mu m$, very close to the nominal value. Hence, the cause of the difference between the measured and simulated data at large $d$ in figure 7 remains unclear.

For microstrips with dielectric filling in of $m$ etched away Nb layers $d = mt + (m + 1)d_{0}$, where $d_{0}$ is the nominal thickness of a single layer of interlayer dielectric between two adjacent metal layers; $d_{0} = 200$ nm for all pairs except between M5 and M6 where it is 280 nm. The maximum expected total dielectric thickness deviation is

$$\Delta d_{\text{max}} = \pm [m \Delta d_{\text{max}} + (m + 1)\Delta d_{0}]^{1/2},$$

assuming that variations of the thickness of the individual layers are statistically independent. Hence, inductance variations caused by potential variations of the dielectric thickness on a chip or across the wafer should significantly decrease with increasing the dielectric thickness. For example, for M6aM4 microstrip inductors $\Delta d_{\text{max}} \approx 44$ nm at $d = 615$ nm. If we maintain the linewidth within $\pm 10\%$ of the target value $w = 200$ nm, the maximum range of inductance variations is expected to be from $-8.8\%$ to $11.0\%$ of the nominal value, corresponding to the process corners $[+\Delta w_{\text{max}}, -\Delta w_{\text{max}}, +\Delta d_{\text{max}}, -\Delta d_{\text{max}}]$ and $[+\Delta w_{\text{max}}, -\Delta w_{\text{max}}, +\Delta d_{\text{max}}, -\Delta d_{\text{max}}]$, respectively. The largest contribution comes from the linewidth variations. For M6aM0 inductors $m = 5$ and $\Delta d_{\text{max}} = \pm 77$ nm, and the total variation range of inductance is from $-6.6\%$ to $8.3\%$, corresponding to the same corners of the process cube as in figure 3. The observed inductance variations between different chips and wafers shown in figure 7 are actually much smaller that this estimate because of a low probability of the extreme deviations of all three parameters in the same fabrication run.

4. Inductance results for SC1 and SC2 processes

4.1. Inductance in a wide range of linewidths

The SC1 process also uses 248 nm photolithography, which was centered to print 250 nm features instead of 350 and 500 nm features used in the SFQ5ee. The SC2 process uses

![Figure 7. Linear inductance of isolated M6 microstrips placed above various ground planes in the SFQ5ee process, progressively increasing the distance between the strip and the ground plane from 0.280 $\mu m$ in M6aM5 to 2.215 $\mu m$ in M6aM0 according to table 1. Solid curve is the simulated dependence, using wxLL software [13] and $\lambda = 90$ nm. Dash curve is equation (3) with $\lambda = \lambda_{t} = 90$ nm. Equation (2) at $w = t = 200$ nm and $\lambda = 90$ nm is plotted by a dash–dot blue curve.](image-url)
193 nm photolithography for the critical layers of inductors, only layer M6 in this particular case, which allowed us to study inductors with linewidth down to 120 nm.

Dependences of the linear inductance of various microstrip and striplines involving layer M6 defined by 193 nm photolithography and M5 defined on the same wafers by 248 nm photolithography are shown in figure 8. Simulation results using wxLL are shown by solid and dash lines, and using InducEx by dash–dot lines. With nominal process parameters from table 1 and $\lambda = 90$ nm, both simulation tools overestimate inductance for all $w$ larger than 0.25 $\mu$m, InducEx more so than wxLL. Reducing the penetration depth to $\lambda = 85$ nm certainly improves the agreement, indicating that the effective ‘magnetic thickness’ is smaller than the nominal. In principle, all thicknesses can be quite accurately extracted by fitting the simulations to the data in figure 8.

The actual linewidth on wafers, $w_w$, metal and dielectric thicknesses of inductors were measured using FIB cross sections. Multiples structures were cross sectioned to get chip-scale averages. The actual values can then be used in the LDFs of the inductance simulators. Multiple inductor types are required for comparison to remove any ambiguity. The average data are shown in table 2 for wafer #1 in figure 8. We can see that the actual thickness of dielectric I4 between the M4 ground plane and the signal conductor on M5 layer, $d_1$, is lower than the nominal thickness by 8%. Also, the actual thickness of the dielectric I6 between the M6 and M7 layers is lower by 10%, whereas all other thicknesses are very much on target. These lower dielectric thicknesses of I4 and I7 layers can fully explain the lower inductances of all inductors in figure 8 without the need to invoke a lower value of $\lambda$. Also of note is that M6 linewidth has a more significant positive bias, $+35$ nm, than M5 linewidth, $+10$ nm, which is the results of using SiO$_2$ hard etch mask in M6 processing. We will discuss the effect of linewidth bias on the narrow lines below.

4.2. Stripline inductors with linewidths down to 120 nm

Wafermaps of inductance of M6aM4bM7 stripline inductors with linewidth from 200 nm down to 120 nm are shown in figure 9. Stripline inductors with $w \geq 180$ nm linewidth have less than 1% inductance standard deviation on 5 mm chips. Wafermaps show the larger inductance values in the central part of the wafer with center-to-edge variation of ~9%, similar to figure 5, but with different locations of the PCM chips in the SC2 process than in SFQ5ee process. 150 nm stripline inductors have less than 3% on-chip spreads of inductance, which is acceptable for the use in VLSI integrated circuits. On-chip inductance variation of 120 nm inductors is relatively big and its cause needs further investigation.

Another important test for application of narrow-line inductors in VLSI circuits is to verify that there is no difference between horizontally and vertically oriented inductors because they are randomly mixed in superconductor integrated circuits. A difference between parameters of vertically and horizontally oriented devices, e.g. resistors and inductors, may indicate astigmatism of the projection optics, causing

![Figure 8. Linear inductance of various isolated stripline and microstrip inductors in a wide range of linewidths in the SC2 process. M6 and M5 signal wires with linewidths, respectively, from 0.12 and 0.22 $\mu$m to 4 $\mu$m were patterned using, respectively, 193 and 248 nm photolithography in the same process. Solid and dash lines show simulations using wxLL with, respectively, $\lambda = 90$ and $85$ nm, and nominal layer thicknesses from table 1 for the SC2 process. Dash–dot lines in (a) show simulations using InducEx with the LDF modified for the thicknesses in the SC2 process and $\lambda = 90$ nm for all layers. Data are shown for two wafers, w1 and w6, which only differ by the etch process used for etching niobium layer M6.](https://example.com/figure8.png)
linewidth difference, or/and texture in the film growth (e.g. for thin-film resistors). Figure 10 presents data for the horizontal and vertical inductors marked, respectively, as \( _{h} \) and \( _{v} \) for seven different locations of the test chip on the wafer, which do not show statistical difference. For instance, for \( w = 180 \text{ nm} \) striplines, the difference between the mean values for vertical and horizontal inductors on-chip is within ±1.4%; a ten-chip wafer average of this difference is −0.27%.

These data are consistent with the linewidth measurements of the inductors, using SEM imaging of their cross sections done by FIB, shown in figure 11. The linewidth measurements also show no difference between the vertical and horizontal inductors. However, the data show a systematic difference between linewidths of isolated and dense inductors. The term ‘dense’ here applies to multiple, typically five, lines at the minimum spacing allowed in the process, 250 nm in this case. The middle inductor in the group, the third in figure 11(a) (left panel), was the inductor tested electrically. Isolated, single, inductors do not have any neighbors within a few micrometers from them. This so-called iso-dense bias is a very well-known lithographic phenomenon [42]. It can also be created by a faster etch rate in the dense areas of the photoresist mask than in the sparse areas caused by various plasma microloading and resist charging effects; see, e.g. [43, 44]. For \( w < 200 \text{ nm} \), the iso-dense difference is about 20 nm, i.e. the single lines are wider than the dense ones by about 20 nm, as shown by the dash–dot line in figure 11(b). The difference diminishes with increasing spacing above 300 nm.

Inductance of the dense and single, both vertical and horizontal, inductors marked, respectively, \( d_{y}, d_{h}, s_{v}, \) and \( s_{h} \) is compared in figure 12 for several linewidths. It is clear that dense inductors have substantially larger inductance values, for all linewidth studied. For example, inductance of the dense 120 nm lines on \( w_1 \) and \( w_6 \), is larger by, respectively, 25% and 11% than inductance of the single lines. The difference can result from a smaller actual linewidth of the dense lines than of the isolated ones, see figure 11(b), and potentially larger contamination of niobium in dense structures, causing an increase in the penetration depth. The difference between \( w_1 \) and \( w_6 \) is caused by the difference in the etching process used, resulting in the overall smaller linewidth on \( w_1 \) than on \( w_6 \).

In figure 13 we plotted inductance of the single and dense inductors, both vertical and horizontal, as a function of their actual line width, \( w_1 \), measured using FIB cross sections. In this representation, a clear separation between single and dense lines goes away and all inductors align more or less along the same curve shown by a red dash line. For comparison, by black solid line we show inductance simulations, using \( w_{\text{LL}} \), with the actual metal and dielectric thicknesses measured on this wafer.

It is clear from figure 13 that using the actual linewidth for wide inductors with design \( w > 250 \text{ nm} \) improves agreement between the measured and the simulated values, making it better than 1% for all the widths up to 4 \( \mu \text{m} \). However, the linear inductance values for the physical linewidths smaller than about 250 nm are noticeably larger than those following from numerical simulations for these physical linewidths, shown by the solid line in figure 13. This difference can be explained by growing, with decreasing the linewidth to below the film thickness, magnetic penetration depth in Nb, from 90 nm in wide strips to ∼105–110 nm in the narrowest ones. Such an increase is known to occur in planar Nb film with decreasing their thickness and caused by decreasing electron mean free path [37]. Another causes could be Nb surface oxidation or hydrogen contamination in processing; see [45, 46], and references therein. Since Nb contamination mainly occurs through the sidewalls of the etched lines, the degree of contamination grows with decreasing the linewidth because the strip surface to volume ratio increases as 1/\( w \). Hence, at the same processing conditions, narrower lines will always absorb more impurities and have shorter electron mean free path than wider lines.

The presence of hydrogen contamination can be detected using electromigration, similar to [46], to drive hydrogen out of the inductor and into niobium ground plane, and then observe electromigration-induced changes in the stripline inductance. We leave these experiments for a different publication.

It is interesting to note that, if we plot inductance of single (isolated) striplines as a function of their design width \( w_1 \), as shown in figure 13 by black symbols, the measured values fall perfectly on the simulated dependence, which uses the actual dielectric and metal thicknesses, the design linewidth, and the

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**Table 2.** Actual thicknesses of process layers from FIB cross sections.

| Metal/thickness, linewidth | Nominal (nm) | Actual (nm) | \( w_1 \), nominal (nm) | \( w_1 \), actual (nm) |
|---------------------------|-------------|------------|------------------------|-----------------------|
| \( M_5aM_4bM_7 \)         | 260         | 239 (−8%)  | 660                    | 668                   |
| \( M_6aM_4bM_7 \)         | 655         | 664 (+1%)  | 200                    | 180                   |

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\( ^a \) Dielectric thickness between the \( M_4 \) ground plane and the signal layer.

\( ^b \) Dielectric thickness between the signal layer and the \( M_7 \) top ground plane.

\( ^c \) Percent deviation from the nominal value.
Figure 9. Wafermaps of the linear inductance of isolated striplines M6aM4bM7 with design linewidth, $w$ from 120 to 200 nm. The data are for w1. Triangle at the bottom indicate position of the wafer notch orienting wafers in processing tools. For $w \geq 150$ nm, the standard deviation of inductance on chip is less than 3%, which is acceptable for superconductor VLSI circuits. Center-to-edge inductance variation is similar to that in figure 5, although the SC2 uses different locations of the PCM chips than the SFQ5ee process.

Figure 10. Linear inductance of vertical, $v$, and horizontal, $h$, isolated stripline inductors with design linewidth $w = 180$ nm on two chips, ch2 and ch3, at various locations A3, C3, etc, on the wafer. The height of the statistic boxes indicates the standard deviation, $1\sigma$. Also indicated are the mean and the average values as well as the full range of data variation. The data show that there is no statistical difference between vertical and horizontal inductors.

standard value of $\lambda = 90$ nm. This suggests that the real superconducting width of narrow Nb striplines is smaller than their physical width measured in SEM by some amount $w_0$, which can be estimated from figure 13 as 35 to 36 nm. The value of $w_0$ corresponds to a shift between the black solid curve and the red dash curve in figure 13.

The presence of a thin nonsuperconducting layer on the sidewalls of Nb lines can be a result of the surface oxidation or contamination by hydrogen known to suppress superconductivity of Nb. The thickness of this nonsuperconducting or weakly superconducting sheath is $w_0/2 \sim 18$ nm on each sidewall of narrow Nb lines. For $w = 120$ nm isolated striplines on wafer 1, which measured $w_0 = 114$ nm in SEM, the superconducting width, $w_s = w_0 - w_0$, in this model would be only 78 nm. The simulated linear inductance of a 78 nm M6aM4bM stripline is 1.066 pH/µm, and 1.061 pH/µm if $w_0 = 80$ nm. The measured inductance on this chip is $1.049 \pm 0.049$ pH/µm, see figure 9, agreeing with this model with <1.6% difference.

It is known that both oxidation and hydrogen absorption lead to Nb swelling due to increase in the unit cell volume. For example, oxidation converts 1 nm of Nb into about 2.5 nm of Nb$_2$O$_5$ oxide. So, formation of an 18 nm oxide layer on the sidewalls, e.g. during wafer treatment in oxygen plasma, would require oxidation of only 7 nm of Nb. Since Nb lines are clamped to the substrate, their width at the interface with the underlying SiO$_2$ cannot change during the oxidation or hydrogen absorption but the linewidth can increase on the free surfaces. As a result, the narrow lines should acquire a noticeable negative profile, having a larger linewidth at the top of
Figure 11. (a) SEM images of the cross sections of the measured dense (left) and isolated (right) inductors with 120 nm design linewidth. (b) The actual linewidth of Nb striplines, $w_A$, measured using SEM vs their design linewidth, $w$. The data are shown for dense lines spaced by 250 nm and single, isolated, lines, both vertical and horizontal. Solid line shows constant positive process bias of 35 nm. Dash line shows a roll down of the actual linewidth. Note a difference between the linewidth of the dense and isolated lines. Also, the process bias for $w_1$ is smaller, and slightly negative, than for $w_6$ due to an intentional difference in the etch process. Dash–dot line indicates a larger process bias for isolated (single) inductors than for dense inductors at $w < 200$ nm.

Figure 12. Linear inductance of single (isolated) and dense stripline inductors M6aM4bM7 with different design linewidth, $w$, and two orientations: vertical and horizontal. Lines connecting data points are to guide the eye. A larger inductance of dense lines can result from a smaller physical linewidth, $w_p$, of the dense lines than of the single lines at the same design linewidth, $w$.

Figure 13. Linear inductance of single (isolated) and dense stripline inductors M6aM4bM7 with different design linewidth, $w$, and two orientations replotted as a function of their physical linewidth, $w_p$. The same data for the single inductors are also shown as the function of their design width. Arrows show the shift of the data points when the design linewidth is replaced by the actual linewidth. Black solid line shows the simulated inductance using $w_{LL}$ with the actual dielectric and metal thicknesses measured on this wafer. Red dash line corresponds to a 35 nm shift of the origin of the $x$-axis for the simulated curve. A good agreement with the data in this case suggests that an electric (superconducting) width of the wires is about 35 nm smaller than the physical width, e.g. due to the presence of a thin nonsuperconducting sheath on the sidewalls of the etched Nb lines.
In a practical range of the moats widths $W \leq 2 \, \mu m$, inductance can be increased up to $\sim 35\%$ with respect to unperforated ground planes. Much wider perforations are impractical for dense circuits because the growth of the inductance slows down, inductance doubles only at $W \approx 10 \, \mu m$, whereas the circuit density suffers dramatically. The relative increase in inductance of the microstrips with $W$ is significantly smaller due to a larger distance to the nearest ground plane and a significant contribution of the space above the signal conductor to magnetic inductance.

Sometimes narrow bridges across long moats need to be placed for signal routing, transforming the long slit into a series of rectangular perforations. These bridged moats have a slightly smaller effect on inductance. For instance, for $w = 0.25 \, \mu m$ striplines and $W = 2 \, \mu m$ moats with length $30 \, \mu m$, the average increase in inductance $L/L(0) = 1.33$ (figure 14), where $L(0) = L(\infty)$ is the inductance without the moat or at infinite distance from it. If instead of this long moat we use ten square perforations $2 \, \mu m \times 2 \, \mu m$ spaced at $1 \, \mu m$, the average increase in inductance of the striplines is 1.28. At a given moat width, the relative change in inductance $L/L(0)$ increases with increasing width $w$ of the signal conductor because narrower inductors have larger fringing fields which are less altered by the moat. For instance, in the previous case of ten square perforation, $L/L(0) = 1.33$ if $w = 0.35 \, \mu m$.

Ground plane perforations alter the return path of the superconducting current, forcing it to flow around the perforation instead of directly under the signal conductor. This can be modeled by inductance matrix containing self-inductances of the perforations and of the current paths along the signal conductor, returning along the perforations in the bottom and top ground planes, and mutual inductances between them [14]. Fortunately, inductance simulations using wxLL or wxLC, shown in figure 14, agree very well with the measurements, which simplifies the design procedure.

In the presence of the moats, inductance can be presented as:

$$L(W) = L(0) + M(W),$$  

(4)

where $M(W)$ is the aiding mutual inductance dependent on the moat width. Hence, the data in figure 14 correspond to $M(W)/L(0) + 1$. For the most practical moat width $W = 1 \, \mu m$, the mutual inductance between the M6 stripe centered over (under) the congruent moats in M4 and M7 ground planes is $M \approx 0.15 L(0) \approx 0.0855 \, \mu H/\mu m$.

In superconductor digital circuits, congruent moats in the ground planes are widely used to collect magnetic flux from active areas of circuits and prevent trapping of Abrikosov vortices in superconducting films where they easily spoil performance of logic cells; see, e.g. [50], and references therein. Although absolutely necessary, these flux trapping moats unavoidably reduce circuit density and may also affect inductances of the nearby inductors due to mutual coupling of inductor to moats. To avoid this coupling, circuit designers place inductors quite far from the moats that decreases circuit density even further.

4.3. Effect of ground plane perforations on inductance

Adding perforations in the ground plane(s) below or/and above the signal conductor of microstrips and striplines is a well-known method of adjusting their inductance, capacitance, and impedance in microwave engineering; see, e.g., [47–49], and numerous references therein. It is also used in superconductor circuits for inductance adjustments; see e.g. [6, 13, 22]. The prior work considered very wide inductors and ground plane perforations which cannot be applied to modern circuits for inductance adjustments; see e.g. [47-49], and numerous references therein. Although absolutely necessary, these flux trapping moats unavoidably reduce circuit density and may also affect inductances of the nearby inductors due to mutual coupling of inductor to moats. To avoid this coupling, circuit designers place inductors quite far from the moats that decreases circuit density even further.

In a practical range of the moats widths $W \leq 2 \, \mu m$, inductance can be increased up to $\sim 35\%$ with respect to unperforated ground planes. Much wider perforations are impractical for dense circuits because the growth of the inductance slows down, inductance doubles only at $W \approx 10 \, \mu m$, whereas the circuit density suffers dramatically. The relative increase in inductance of the microstrips with $W$ is significantly smaller due to a larger distance to the nearest ground plane and a significant contribution of the space above the signal conductor to magnetic inductance.

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Ground plane perforations alter the return path of the superconducting current, forcing it to flow around the perforation instead of directly under the signal conductor. This can be modeled by inductance matrix containing self-inductances of the perforations and of the current paths along the signal conductor, returning along the perforations in the bottom and top ground planes, and mutual inductances between them [14]. Fortunately, inductance simulations using wxLL or wxLC, shown in figure 14, agree very well with the measurements, which simplifies the design procedure.

In the presence of the moats, inductance can be presented as:

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where $M(W)$ is the aiding mutual inductance dependent on the moat width. Hence, the data in figure 14 correspond to $M(W)/L(0) + 1$. For the most practical moat width $W = 1 \, \mu m$, the mutual inductance between the M6 stripe centered over (under) the congruent moats in M4 and M7 ground planes is $M \approx 0.15 L(0) \approx 0.0855 \, \mu H/\mu m$.

In superconductor digital circuits, congruent moats in the ground planes are widely used to collect magnetic flux from active areas of circuits and prevent trapping of Abrikosov vortices in superconducting films where they easily spoil performance of logic cells; see, e.g. [50], and references therein. Although absolutely necessary, these flux trapping moats unavoidably reduce circuit density and may also affect inductances of the nearby inductors due to mutual coupling of inductor to moats. To avoid this coupling, circuit designers place inductors quite far from the moats that decreases circuit density even further.
To study the effect of moats on inductors, we measured the relative change of stripline inductance as a function of distance $s$ from the edge of congruent moats in M4 and M7 ground planes to the signal conductor edge, using dimensions typical for VLSI circuits. A sketch of the inductor cross section, showing mutual positions of the moats and the inductor is shown in figure 15. The results are shown in figure 15 as well. Negative values of $s$ correspond to the inductor moving into the moat; $s = -(W + w)/2$, where $W$ is the width of the moats, corresponds to a symmetrical position of the stripline along the middle of the moat, as in figure 14. We can see from figure 15 that the effect of moats on the inductance of nearby inductors is quite small. Even for inductors with zero distance to the moats, $s = 0$, the increase in the stripline inductance with respect to the stripline without moats is less than 6% for $W = 1.0 \, \mu m$, and smaller for narrower moats.

The simulated linear inductance $L(s)$ has a symmetric bell-shaped dependence with the apex at $s_0 = -(W + w)/2$, corresponding to the symmetrical position of the signal conductor in the moats. Within and near the moat, this bell shape can be approximated, e.g. by a Gaussian as shown in figure 15 by red $\pm$ symbols,

$$L(s) = \Delta L \cdot \exp \left[ - (s + s_0)^2 / (2d_{\text{eff}}^2) \right] + L(\infty), \quad (5)$$

where $\Delta L = L(s_0) - L(\infty)$ is the maximal moat-induced change of the inductance. The effective length $d_{\text{eff}}$, as well as $\Delta L$, depends on the moat width: $d_{\text{eff}} = 0.41$ and $0.31 \, \mu m$, respectively, for $W = 1.0 \, \mu m$ and $W = 0.5 \, \mu m$ moats.

The data in figure 15 indicate that the moat influence on inductors diminishes very quickly with moving inductor away from the moat. This is easy to understand. The return currents in the ground planes flow mainly right under and above the signal conductor, spreading very little and decaying with distance from the conductor edge with a typical decay distance of about $(d_1 d_2)^{1/2} \sim 0.36 \, \mu m$, where $d_1$ and $d_2$ are the bottom- and top dielectric thicknesses in the asymmetrical stripline [51]. So, moats in the ground planes placed farther away than this distance cannot significantly change the distribution of the return currents and, thus, should have negligible effect on stripline inductance and negligible moat to inductor coupling. Our measurements and simulation results demonstrate that spacing inductors from the moats by $\geq 0.25 \, \mu m$ is sufficient to keep the moat effect on inductance $M(W)/L(0)$ below 3% for all practical moat widths $W \leq 2 \, \mu m$ in the SFQ5ee and SC1/SC2 processes. Within the accuracy of the measurements, we were not able to detect any effect of the moats on stripline inductance at $s > 0.75 \, \mu m$. The simulation and the measurement accuracy was also not sufficient to distinguish between a simple exponential decay and equation (5) at $s > 0$.

The data points in figure 15 show some scattering, especially for inductors designed with $s = 0$, i.e. with coincident edges of the inductor and the moats. We think that this small variation is likely caused by misalignment of the fabricated inductors and the moat edges in the M4 and M7 ground planes. Misalignment between M6 and M7 has the largest effect because M7 is closer to the M6 inductor than M4. Assuming that M6 and M4 are perfectly aligned and that M7 moat is shifted by $+0.1 \, \mu m$, the simulated inductance is shown in figure 15 by a dash–dot bell curve for $W = 1 \, \mu m$ moats. It demonstrates a few percent increase in inductance with respect to the perfectly aligned layers. Therefore, misalignment between circuit layers may be an additional source of small inductance variations for inductors in a close proximity to moats in ground planes.

To conclude this section, our inductance data indicate that coupling of inductors to distant, $s \geq 0.75 \, \mu m$, moats is extremely small. For $W = 1.0 \, \mu m$ and $s = 0.25 \, \mu m$, mutual inductance with $w = 0.25 \, \mu m$ stripline M6aM4bM7 was measured to be $M \approx 0.02 \cdot L$ or about 0.01 pH/$\mu m$. If this moat traps one flux quantum $\Phi_0$, magnetic flux induced in stripline inductors at $s = 0.25 \, \mu m$ should be only 0.02$\Phi_0$ and much smaller for larger distances to the moats. This coupling should have negligible effect on the critical current of JJs in logic cells and the cells performance.

5. Inductance of vias between layers

5.1. Via structure and measurements

Superconducting vias are an essential component of all superconductor integrated circuits, providing connections between
chains of vias containing from 20 to 64 vias and placed them current direction and as the via has dimensions by some amount, is shown in figure typical SEM image of I5 via cross section with sidewall is about 75◦. The opening in the interlayer dielectric, I5 in this case, filled by niobium of the next layer, M6 in this case. The slope of the linear fit gives inductance per via, L_{via} shown in table 3. Inset shows inductance per via as a function of the via length b along the current direction for I7(M4 + M9) and I5(M4 + M7) vias with a = 500 nm. Solid lines are linear fits to L_{via} = L_0 + L_1 b, giving the averaged values L_0 = 0.248 ± 0.01 pH and 0.229 ± 0.01 pH, respectively, for I7(M4 + M9) and I5(M4 + M7) vias, and L_1 = 0.208 ± 0.01 pH/µm and 0.163 ± 0.01 pH/µm, respectively, for the same types of vias.

Figure 16. Schematic cross section of a chain of four I5 vias between M4 and M7 ground planes, showing direction of electric current alternating between M6 and M5 layers. The current is returned to the ground planes through staggered vias I6, I5, and I4 connecting M7 and M4 layers. A via presents an opening in the interlayer dielectric, with dimensions a and b at the bottom, filled by the next Nb layer as shown in the SEM image of the cross section. The opening must be surrounded by the top and bottom Nb by s and r on all sides for via reliability in case of misalignment. Top view shows dimensions a, b, s, r, and w. In the chain, adjacent vias are spaced by s and interconnected by short pieces of wires with width w in alternating layers to form a meandering current path. Much longer chains containing from 20 to 60 vias were used in inductance measurements to increase the accuracy. The contribution of the ground connection on the right, by vias I6, I5, and I4, was deducted using the differential method. The contribution of metal wires connecting the vias in M5 and M6 layers was also deducted to find inductance per single via; see text.

Figure 17. Inductance of chains of square vias I5 with different number of vias in the chain, and for different via sizes, a.
Inductance of interconnecting wires M5 and M6 was subtracted from the total inductance of the chain using differential measurements or independently measured inductance per unit length of M5 and M6 wires with w = 1 µm between M4 and M7 ground planes. The slope of the linear fit gives inductance per via, L_{via} shown in table 3. Inset shows inductance per via as a function of the via length b along the current direction for I7(M4 + M9) and I5(M4 + M7) vias with a = 500 nm. Solid lines are linear fits to L_{via} = L_0 + L_1 b, giving the averaged values L_0 = 0.248 ± 0.01 pH and 0.229 ± 0.01 pH, respectively, for I7(M4 + M9) and I5(M4 + M7) vias, and L_1 = 0.208 ± 0.01 pH/µm and 0.163 ± 0.01 pH/µm, respectively, for the same types of vias.

components located on different layers and closing superconducting loops forming circuit inductors. Reduction of the size of vias is a much more difficult task than reduction of the linewidth of inductors and is a subject of considerable technological efforts needed to increase the integration scale of SCE [52, 53]. Contribution of vias, especially of submicron sizes, to the inductance of superconducting loops formed in integrated circuits is largely unknown. Below we present experimental data for many configurations of vias in the SFQ5ee [29] and SC1/SC2 processes [5].

Vias I5 connecting layers M5 (JJ base electrode) and M6 are used very frequently because they are required to form resistively shunted junctions in the SFQ5ee and SC1/SC2 processes and inductors on M6 layer. Any via presents typically a rectangular opening in the interlayer dielectric, I5 in this case, filled by niobium of the next layer, M6 in this case. The slope of the sidewall is about 75◦. Bottom dimensions of the opening are a and b in the perpendicular and parallel to the current directions, respectively; square vias are used most frequently. The typical SEM image of I5 via cross section with a = b = 700 nm is shown in figure 16. The opening in the dielectric is surrounded by Nb of the bottom and top layers by some amount, s, in order to increase via reliability if there is a misalignment between the layers. The combined object which we refer to as the via has dimensions a + 2 - s, r perpendicular to the current direction and b + 2 - s, r along the current direction.

To increase the accuracy of the measurements, we used chains of vias containing from 20 to 64 vias and placed them in a stripline configuration, e.g. with M4 and M7 ground planes most often used in circuits, as shown in figure 16. Parasitic inductance of the ground connection at the chain end, using three staggered vias I6, I5, and I4 shown in figure 16, was deducted using the differential scheme described in section 2.2.

A chain containing an even number n of I5 vias has n/2 − 1 pieces of M6 wires and n/2 pieces of M5 wires each of length s, connecting vias in the chain. To find the inductance per single via, L_{via} we deducted the contribution of connecting wires from the total measured inductance, using two methods: (a) by deducting inductances of the stripline M6aM4bM7 with length s(n/2 − 1) and width w = a + 2 - s, r, and of the stripline M5aM4bM7 with length s(n/2) and the same width w, calculated using the stripline inductance data measured on the same chip and given in table 3; (b) by including these two striplines and two I5 vias as the left inductor in the differential measurements scheme in figure 2. Then, by plotting the resultant bare inductance versus the number of vias and using the linear fit L_{chain} = nL_{via} + L_0, as shown in figure 17, we determined the inductance per via, L_{via}. In all cases, we observed that the residual term L_0 was negligibly small in comparison with the measured inductance, indicating that the differential method of removing parasitic contributions worked very well. A similar procedure was used for all other types of vias.
Table 3. Inductance of vias of various types and dimensions.

| Via or Wire | Ground planes | a (nm) | b (nm) | sr (nm) | \( L_{\text{via}, \text{w6}} \) (pH) | \( L_{\text{via}, \text{w8}} \) (pH) |
|------------|---------------|--------|--------|---------|-----------------|-----------------|
| I5         | M4 + M7       | 700    | 700    | 350     | 0.245           | 0.245           |
| I5         | M4 + M7       | 700    | 700    | 150     | 0.287           | 0.281           |
| I5         | M4 + M7       | 500    | 500    | 250     | 0.318           | 0.325           |
| I5         | M4 + M7       | 400    | 400    | 300     | 0.362           | 0.362           |
| I5a        | M4 + M7       | 500    | 500    | 250     | 0.303           | 0.317           |
| I5b        | M4 + M7       | 1000   | 1000   | 250     | 0.389           | 0.394           |
| C5         | M4 + M7       | 500b   | 500b   | 200     | 0.473b          | —               |
| I6         | M4 + M9       | 500    | 500    | 250     | 0.394           | —               |
| I6         | M4 + M9       | 400    | 400    | 200     | 0.455           | —               |
| I6         | M4 + M9       | 400c   | 400c   | 200     | 0.473c          | —               |
| I6         | M4 + M9       | 350d   | 350d   | 175     | 0.484           | —               |
| I7         | M4 + M9       | 500    | 500    | 250     | 0.393           | —               |
| I6         | M4           | 500    | 500    | 250     | —               | 0.705           |
| I6         | M4           | 400    | 400    | 200     | —               | 0.876           |
| I7         | M4 + M9       | 500    | 500    | 250     | 0.393           | —               |
| I6         | M4           | 400    | 400    | 200     | —               | 0.876           |
| I6         | M4           | 400    | 500    | 250     | 0.393           | —               |
| I6         | M4           | 400    | 500    | 250     | 0.393           | —               |
| I5I6I7     | M4 + M9       | 500    | 500    | 250     | 1.249e          | —               |
| M5         | M4 + M7       | —      | —      | —       | 0.3094f         | 0.3006f         |
| M6         | M4 + M7       | —      | —      | —       | 0.2596f         | 0.2569f         |
| M6         | M4           | —      | —      | —       | 0.6405f         | 0.6405f         |
| M6         | M4 + M9       | —      | —      | —       | 0.3846f         | —               |
| M7         | M4           | —      | —      | —       | 0.7338f         | —               |
| M7         | M4 + M9       | —      | —      | —       | 0.3969f         | —               |
| M8         | M4 + M9       | —      | —      | —       | 0.3163f         | —               |

Wafers w3 and w4 are from a different fabrication run of the SFQ5ee process [29].

Diameter of a circular via to JJ on layer J5.

Circular via diameter; width of connecting wires \( w = a + 2 \cdot sr = 800 \) nm.

Width of connecting wires \( w = a + 2 \cdot sr = 700 \) nm.

Via comprised staggered vias I5, I6, and I7, connecting layers M5 and M8.

Inductance per unit length in pH/µm of wires with width \( w = 1 \) µm and the specified ground planes, measured on the same chip and used in the calculations of via inductance; see text.

Wafers w3 and w4 are from a different fabrication run of the SFQ5ee process [29].

I6 and I7 vias are spaced at 250 nm in the direction of current.

I6 and I7 vias are spaced at zero distance in the direction of current.

5.2. Inductance of vias between superconducting layers

The obtained results are summarized in table 3. We present a subset of data for two wafers, w6 and w8, fabricated in the same run of the SC1 process and two wafers, w3 and w4, fabricated in a different run in order to characterize the cumulative repeatability of the fabrication process and the measurements. The data should be also valid for the SFQ5ee process due to a close similarity in the layer thicknesses, and we included in table 3 some data obtained on wafers made in SFQ5ee process for comparison.

Via inductance crucially depends on the current return path, i.e. the type and number of ground planes, because inductance is electromagnetic property of a loop. So, the data in table 3 should only be used in this context. For instance, if two inductors M6aM4bM7 and M5aM4bM7 are connected by an I5 via it is appropriate to add \( L_{\text{via}} \) from table 3 to the total loop inductance. In asymmetrical inductors like these, a larger return current flows in the closest to the signal conductor ground plane than in the more distant one, and magnetic field is higher between the signal conductor and the closest ground plane. The closest ground plane is different for different inductors, e.g. it is M7 for M6 inductors and M4 for M5 inductors. When M6 and M5 inductors are connected, the return currents and magnetic field need to redistribute in the region of the via, contributing to the total inductance of the via.

Although vias are three-dimensional objects, we can gain some insight into their inductive properties from the properties of individual films and the data in table 3. We see that,
at a constant size $a$ and width $w$, via inductance linearly depends on its length in the direction of applied current, $b$, $L_{\text{via}} = L_0 + L_1 b$; see inset in figure 17. By inspecting the via cross section in figure 16, the current path in the via, from left to right, consists of a flat piece of M6 wire with length $sr$ in front of the opening in the dielectric, followed by a front wall of the via where most of the current flows down, similar to a waterfall, and a piece of wire with length $b$ and width $a$ at the bottom of the via, and then M5 wire with width $w$ and length $sr$. Inductance of the via can be estimated as the sum of these three components:

$$L_{\text{via}} = (\ell_{\text{M5}} + \ell_{\text{M6}}) \cdot (w - a)/2 + L_{\text{wall}} + b \cdot \ell_{\text{M5M6}},$$  \hspace{1cm} (6)

where we used that $sr = (w - a)/2$. In equation (6), parameters $\ell_{\text{M5}}$ and $\ell_{\text{M6}}$ are linear inductances of, respectively, M5 and M6 wires with width $w$, given in table 3; $\ell_{\text{M5M6}}$ is linear inductance of the via bottom layer, and $L_{\text{wall}}$ is inductance associated with the current dropping to the bottom of the via. There can be other terms related, e.g., to current crowding near the front wall and at the exit from thick bottom into the thinner M5, but we will neglect them for simplicity.

The metal thickness at the bottom of large vias is $\ell_{\text{M5M6}} = \ell_{\text{M5}} + \ell_{\text{M6}}$, the sum of M5 and M6 thicknesses given in table 1. It is slightly less in small vias due to shading effects during the top metal deposition into the opening. We will neglect this difference. Then, we simulated the linear inductance $\ell_{\text{M5M6}}$ for different linewidths $a$, using $wxLL$. Using the simple model equation (6), we calculated dependence of via inductance on via cross section $a$ for square $a = b$ vias, shown in figure 18 by a dash–dot line for $L_{\text{wall}} = 0$, along with the measured data from table 3.

From via cross sections, we determined that Nb thickness on via sidewall, $t_w$, is about 40% of the layer thickness on flat surfaces, about 80 nm for I5 vias, which is less than $\lambda$. The height of the drop is about the difference between the inter-layer dielectric thickness and the top metal layer thickness, $d_{\text{M5M6}} = t_{\text{M6}} \approx 60$ nm for I5 vias. Then, the contribution of the front wall drop to the inductance can be estimated assuming that this inductance is mainly kinetic, giving:

$$L_{\text{wall}} = \mu_0 \left(\lambda^2/\ell_w\right) \cdot (d_{\text{M5M6}} - t_{\text{M6}})/a,$$  \hspace{1cm} (7)

where $\mu_0 \lambda^2/\ell_w$ is kinetic inductance per square and $(d_{\text{M5M6}} - t_{\text{M6}})/a$ is the number of squares of Nb film on the front wall of the via. Including equations (7) into (6) results in the dependence of via inductance on via size shown by solid curve in figure 18, which nicely agrees with the data, especially at sizes $a \geq 0.5 \mu m$.

The via cross section in figure 16 and the described simple model cannot be applied to vias smaller than about 400 nm for two reasons. Firstly, openings in the dielectric with sizes comparable to the dielectric thickness cannot be filled by metal sputtering because of clogging near top of the opening. Secondly, the opening shape becomes very rounded, rather circular than square. For making high aspect ratio vias, completely different approaches need to be used, for instance, a stud-via process described in [50] where cylindrical metal pillars (studs) are etched and then interlayer dielectric is deposited over them and planarized by CMP. Another one is a damascene process filling the openings by a metal chemical vapor deposition to form cylindrical pillars and then removing the metal deposited on the flat surface by a metal CMP.

In any of these advanced processes, via would present a superconducting rod with diameter $a$ connecting two superconducting wires on different layers. For deep submicron via diameters, which are the main focus of these advanced processes, the rod inductance can be estimated using a formula similar to equation (5) where kinetic inductance of the rod $L_k = (4\lambda^2/\pi a^2) d$ will dominate; $d$ is the rod height equal to the dielectric thickness. In this asymptotic case, the via inductance becomes:

$$L_{\text{via}} = (\ell_{\text{M5}} + \ell_{\text{M6}}) \cdot (w - a)/2 + \left(4\mu_0 \lambda^2/\pi a^2\right) d$$  \hspace{1cm} (8)

This dependence is shown in figure 18 by a dash curve. A full dependence of $L_{\text{via}}$ on via size should provide a smooth transition from the dash–dot curve equations (6) and (7) for relatively large vias with $a > 0.4 \mu m$ to the dotted curve equation (8) for $a < 2\lambda$. To summarize this discussion, we developed a simple description of via inductance based on inductive properties of superconducting films comprising vias and obtained a good agreement with the available data.
Because vias are truly three dimensional objects, we also attempted to simulate inductance of I5 via chains using 3D inductance extractor InductEx [19]. We used a LDF corresponding to the fabrication process and circuit layouts corresponding to the differential measurements described above. These layouts have \( n = 24 \) via chains in the right arm of the SQUID in figure 2. In its left arm the SQUID has an I5 via to a 6 \( \mu \text{m} \)-long M5 wire, length \( sr = n/2 \), followed by another I5 via connecting a 5.5 \( \mu \text{m} \)-long M6 wire, length \( sr = (n - 1)/2 \), thus allowing to automatically deduct contributions of via interconnecting wires in the right arm and all ground connections. The differential number of vias in the layouts is 22. The version of InductEx used in simulations assumes a vertical slope of via sidewalls.

For the linear inductance of 1 \( \mu \text{m} \)-wide M5aM4bM7 and M6aM4bM7 striplines, InductEx gives 0.3041 and 0.2576 \( \text{pH/} \mu \text{m} \), respectively, which closely, within 0.3%, matches the average of values for the two wafers of 0.305 and 0.258 \( \text{pH/} \mu \text{m} \) in table 3, passing the first check. The simulated inductance per I5 via is shown in figure 18 by black squares for various sizes of square I5 vias at the fixed width of wires \( w = 1 \mu \text{m} \). The agreement with the measurements is not as good as it appears that the experimental dependence and the simulated one are different and simply intersect at one point at \( a \sim 0.4 \mu \text{m} \). Surprisingly, InductEx cannot find a solution if \( a = w \), a completely legitimate case from mathematical standpoint and often encountered in semiconductor electronics manufacturing. In this case all the current flows down the front sidewall of the first via and up the front sidewall of the second via, and so on, in chains of vias. The asymptotic behavior at \( a \rightarrow w \) indicates a value of 0.32 \( \text{pH per via} \), which is significantly larger than the inductance of a 1 \( \mu \text{m} \) long piece of wire with thickness \( t_{M5} + t_{M6} \), above M4 and below M7 ground planes. The dotted black curve in figure 18 is our approximation of the InductEx simulated values by a simple dependence in order to guide the eye. More work is required to understand the source of these differences, improve the software, and develop models for small vias.

5.3. Inductance of staggered and stacked-staggered vias

Composite vias comprising several individual vias placed at the minimum allowed spacing are used to connect distant layers, e.g. via I45I6 connecting M4 and M7 ground planes is sketched in figure 16. Vias between adjacent pairs of metal layers, I1 and I1+1, are offset (staggered) to make contact on the planar surface of metals M1 and M1+1. The next level via I1+2 can be either also offset in a staircase fashion or stacked on top of I1 in order to minimize the total area. A cross section of two stacked-staggered vias I112I3I4I5 connecting layers M1 and M6 is shown in figure 19 as an example. Usually, the offset between vias is equal 2\( sr \), allowing to assemble composite vias from individual parametric via cells.

In double vias, like I5I6 or I6I7, the transport current always flows in the same direction in both vias. Therefore, our simple model presented in section 3.2 should apply, and inductance of the double via should be equal to the sum of inductances of the individual vias. The data in table 3 more or less support this. Similarly, for a staircase arrangement of \( n \) vias, e.g. I1I2I3..., inductance of the composite via should be approximately equal to the sum of inductances of individual vias. In stacked-staggered vias, electric current in adjacent layers flows in the opposite directions in a meandering fashion, as shown by arrows in figure 19. This creates a negative mutual inductance between the layers and forces the current to flow near only one wall of the vias without spreading out along the bottom of the vias. In this case, we could expect the total inductance to be a bit lower than the sum of individual inductances.

We measured inductance of the stacked-staggered vias shown in figure 19 in order to provide data for circuit design and model building. Test circuits containing chains of stacked-staggered vias were fabricated in SFQ5ee process [29], and we used the approach described in V.B to infer inductance per composite via. The data for stacked-staggered vias comprised \( n = 4 \), for I112I3I4 via, and \( n = 5 \), for I112I3I4I5, individual square vias are shown in table 4. First of all, we note that inductance of these composite vias is quite substantial. A typical inductor in logic cells of superconductor integrated circuits has a loop inductance on the order of 10 \( \text{pH} \), and two vias are required to form a loop between different layers. So the inductance of two composite vias can reach up to 20%–30% of the typical loop inductance and, hence, needs to be accounted for quite accurately. Similarly, if M1 layer is used in a PTL to transmit data between logic cells, inductance of the M1–M6 path, i.e. of via I112I3I4I5, needs to be taken into account.

Individual vias are connected in series in the composite via. So, we can estimate a contribution of the top I5 via by subtracting inductance of I112I3I4 via from inductance of I112I3I4I5 via. The result is given in the third row of table 4; it does not differ significantly from the I5 via inductance in table 3, obtained using chains of individual I5 vias. We separated I5 vias because they slightly differ from all other vias in the stack because I5 dielectric thickness is 280 nm in the SFQ5ee process whereas thickness of all other dielectric layers

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**Figure 19.** Cross section of a chain of composite stacked-staggered vias I112I3I4I5 connecting layers M1 and M6, over M0 ground plane, fabricated in the SFQ5ee process. Vias I1 connecting neighboring layers M1 and M1+1 are offset by 2\( sr \) from vias I1+1 on the next level connecting M1+1 and M1+2. Individual vias are square with \( a = 700 \text{ nm} \), surround \( sr = 350 \text{ nm} \), and spacing between adjacent vias I1 and I1+1 and between the stacks is 500 nm.
is 200 nm; see table 1. We can simply characterize the average contribution of individual vias by dividing the total inductance into the number \( n \) of individual vias, as shown in table 4. The difference between \( n = 4 \) and \( n = 5 \) cases is within the error of the measurements and the wafer-to-wafer variation. Therefore, we recommend to use in circuit design the following average inductance values for 700 nm square vias in the SFQ5ee process: 0.28 pH per via for \( n = 4 \) and \( n = 5 \), and 0.29 pH per via for \( n = 5 \). Similarly, for 500 nm square vias, we suggest values of 0.32 pH for \( n = 5 \) and 0.31 pH per via for all other vias. The difference between inductance of vias with \( a = 0.5 \) and 0.7 \( \mu \)m is not that significant.

6. Inductance of thin film resistors

Thin-film resistors are used to shunt JJs in order to damp Josephson oscillations and control JJ switching dynamics. Shunt resistors operate with ac currents of very high frequencies up to about 1 THz, contrary to bias resistors which are used to simply set dc bias current through JJs. Inductance of shunt resistors can strongly affect JJ dynamics because it can resonate with junction capacitance and cause many nonlinear effects [54–56]. Hence, knowledge of this inductance and ability to control it is important for integrated circuit design and fabrication process development.

Geometrical inductance of thin-film resistors can be simulated using inductance extraction software like FastHenry [11] and InductEx [19], and is usually relatively small due to the presence of superconducting layers, ground planes, below and above the resistors. In [57], a relatively large inductance associated with thin-film shunt resistors was found and ascribed to the imaginary part of the complex conductivity and the associated kinetic inductance of thin-normal-metal films at frequencies larger than electron scattering frequency. This interpretation may require an additional re-examination which is beyond the scope of this paper and will be done separately.

Inductor extractors [19, 20] do not account for the kinetic inductance of resistors because they use only the real part of the complex conductivity of thin films at finite frequencies in their computational engines. In Whiteley’s [20] adaptation of the FastHenry [11] to superconductors, the complex conductivity is used to treat Meissner effect in superconductors; see, e.g. [58, 59]. Hence, extending this approach to thin-film resistors in the normal state should be straightforward.

7. Discussion

7.1. Flux trapping and coupling to moats

Recent flux trapping experiments, using M6aM4 microstrip inductors and circuits fabricated in the SFQ5ee process at MIT LL, found a much stronger coupling between microstrips and moats than what we measured in this work; see [60] and references therein. This is partly expected because, due to the large distance \( d_1 = 0.615 \mu \)m between M4 and M6 layers, see table 1, the return current spreads to much larger distances in these microstrips than in the striplines with two ground planes where \( d_2 = 0.2 \mu \)m mainly determines the current spreading around the moats. However, in [60] a coupling was observed to moats located at distances much farther away than would be consistent with the results of our measurements showing a very fast, nearly exponential decay of coupling with distance to long and narrow moats. We suggest that coupling to distant moats observed in [60] is an artifact of the experimental procedure used as well as a result of a difference between microstrip configuration used in [60] and stripline configuration used in this work.

To explain these differences, consider a simplistic circuit containing a piece of ground plane with two moats and a microstrip as sketched in figure 20(a). In a typical experiment with superconductor integrated circuits, a circuit is cooled down in a weak, but unfortunately unavoidable, residual magnetic field \( B_r \), whose source is far away from the chip. The source can be the Earth field or not completely demagnetized mu-metal shields [61, 62], and is represented in figure 20(a) by the \( N \) and \( S \) poles. Above the superconducting critical temperature, \( T_c \) the field distribution in the ground plane represents the field source pattern and is typically more or less uniform. All the field lines start and end on the magnet poles, and the field does not change direction within the circuit.

The purpose of the moats is to attract all Abrikosov vortices which can form in the ground plane upon field cooling or make their formation energetically unfavorable by reducing the effective width of the ground plane strips between long moats below the critical width \( w_c = (2\Phi_0/\pi B_r)^1/2 \); see [50] and references therein. Cooling through the \( T_c \) should be very slow.
If these cooling conditions fulfilled, below the $T_c$, magnetic flux is completely expelled from the ground plane to outside of the chip and into the moats as shown schematically in figure 20(b). Superconducting screening currents are induced around edges of the moats and around the periphery of the ground plane. These currents exponentially decay in films with thickness $t > 2\lambda$. Therefore, a microstrip placed a few $\lambda$ away from the moat edges is screened from the flux trapped in the moats; magnetic flux induced by the current in the microstrip does not couple to the flux trapped in the moats. This situation basically corresponds to the experimental conditions used in this work, except that we used striplines.

Now consider what happens if the external magnetic field is switched off, as was a part of the experimental procedure in [60]. Magnetic flux outside of the chip and the screening current on the periphery of the ground plane vanish. However, the flux cannot disappear from the moats in the superconductor (or from the vortices trapped in the film), because this would require destruction of superconductivity of the ground plane. Magnetic field lines must be closed according to the Maxwell equations. Therefore, magnetic field lines must rearrange to form closed loops, closing around the ground plane and through the moats, as shown schematically in figure 20(c). This completely changes configuration of the magnetic field around the circuit and distribution of currents in the ground plane. Now, the field lines and the superconducting screening currents need to spread out over the ground plane and appear also on its bottom side to keep magnetic field parallel to the superconducting ground plane. This spreading out increases coupling between microstrips on both sides of the ground plane to the nearest moats and induces coupling to distant moats. Apparently, this artificially induced coupling is what was observed in [60].

A much more adverse situation takes place if a circuit field cooling is done in a nonuniform, sign-changing field of a local source, e.g. a wire with current $I_{mag}$, placed near the chip surface, as was used in [60] and depicted schematically in figure 21. Above $T_c$, the closed-loop field lines produced by $I_{mag}$ penetrate the ground plane at various angles. The field decays inversely proportional to the distance from the wire and changes direction on its opposite sides, figure 21(a). Below $T_c$, the flux lines become expelled into the moats in such a way that moats on opposite sides of the wire have opposite directions of magnetic flux and superconducting currents are induced around and between the moats linked to the microstrip inductor M4aM4.

![Figure 20. A sketch (not to scale) of an inductor M6 with ports P1 and P2 on a planarized SiO$_2$ dielectric above M4 ground plane with just two flux trapping moats (perforations). In general, there may be many more moats and inductors at various distances to each other. (a) Cooling in a weak magnetic field created by a distant source. Magnetic flux is being expelled towards periphery of the ground plane and into the moats in the directions suggested by red arrows. The field lines start and end on the source of the residual field, e.g. Earth magnetic poles. (b) Below $T_c$, Meissner screening currents are flowing around the moats with trapped flux and around the periphery of the ground plane. The currents are confined to distances on the order of magnetic field penetration depth $\lambda(T)$. (c) After the field is switched off. The field lines must form closed loops, closing through moats and around the ground plane, as shown schematically. The trapped flux in the moats remains unchanged but the field and screening current distributions need to change substantially, causing coupling between inductor M6 and the moats. Superconducting currents are now induced everywhere in the ground plane, both on the top and bottom surfaces of the ground plane. Magnetic flux lines closing through the moats become linked to the microstrip inductor M6aM4.](image-url)
Figure 21. The same experiment as shown in figure 20 but now done using a local field sources, e.g. a wire with current $I_{\text{mag}}$ or a coil placed near the circuit. (a) The field direction changes sign within the circuit, pointing down to the right from the wire and pointing up to the left from the wire. In the normal state, all field lines are closed loops going through or around the ground plane. (b) Below $T_c$, magnetic flux is expelled out of the ground plane and a part of it is trapped into the moats, forming fluxons of the opposite polarity with screening currents circulating around the moats in the opposite directions. Screening current is also induced between the moats on both sides of the ground plane. Because magnetic field of the wire decays slowly (inversely) with the distance, it induces flux into and creates long-range interaction between very distant moats, thus creating a much stronger coupling to the inductor $M_6$ than in the case shown in figure 20. (c) After the field source (current $I_{\text{mag}}$) is switched off, the field lines closing around the ground plane vanish along with the screening currents. However, the flux trapped in the moats and linking the moats remains unchanged. The field and screening current distributions need to adjust. In this case, coupling of nearby inductors (on both sides of the ground plane) to the distant moats is the result of an artificially created bi-polar distribution of the local magnetic field that changes directions within the circuit, on opposite sides of the field source.

Figure 22. Schematic cross section of a stripline $M_6aM_4bM_7$ with flux trapping moats and distribution of magnetic field lines corresponding to the experimental conditions used in this work. The $M_4$ and $M_7$ ground planes are connected using superconducting vias placed on the periphery of the ground planes and between the moats, forming closed superconducting loops around the stripline. The effect of the nearest moat on the left was studied. This moat is not separated by vias connecting $M_4$ and $M_7$, whereas a more distant moat on the right is. (a) After field cooling in a weak residual field of the mu-metal shields, magnetic flux is expelled and trapped in the moats. The field is constant. All bias currents to the test circuit were applied and removed while the circuit was in the superconducting state, which cannot change flux distribution in the moats of the circuit. (b) If the field is switched off, a redistribution of flux and currents must happen to form closed $B$-field lines. However, in this case, the currents are mainly induced on the top surface of the top ground plane $M_7$ and the bottom surface of the bottom ground plane $M_4$. The stripline coupling to the flux in the moats remains weak and unchanged from (a). Coupling to the moat on the right is negligibly small due to superconducting vias connecting the ground planes.

7.2. Moats and flux trapping: striplines vs microstrips

Another major difference between the measurements in this work and in [60] is that we used stripline inductors with two connected ground planes, which provide a much better shielding than a single ground plane, even in the worst case considered above. Indeed, upon a slow cooling of the chip, the flux is expected to be trapped in the congruent moats as shown schematically in the cross sections in figure 22(a). If the field is somehow switched off, the flux lines need to rearrange into closed loops. However, in this case they can only close outside of the top ground plane $M_7$ due to the presence of superconducting vias connecting the top and bottom ground planes; see figure 22(b). Now, the screening currents will appear on the bottom surface of the bottom ground plane $M_4$ and on the top surface of the top ground plane $M_7$. However, the possibility of the field lines slipping under the $M_7$ and affecting the inductor $M_6$ is very small.

If the field was initially parallel to the ground planes, the flux may remain frozen in superconducting loops formed between vias connecting $M_4$ and $M_4$, and may still affect cell inductors and junctions between $M_4$ and $M_7$.

This discussion summarizes why configurations with two and more ground planes enabled by modern fabrication processes are more preferable for the use in advanced superconductor integrated circuits, providing much better circuit...
shielding and protection against flux trapping and parasitic coupling to moats.

8. Conclusion

In conclusion, we presented self-inductance data for many features commonly encountered in modern superconductor integrated circuits such as straight line inductors in microstrip (one ground plane) and stripline (sandwiched between two ground planes) configurations, vias between the adjacent layers and composite vias connecting distant layers in the stack, chains of vias, etc. We also studied the effect of moats—long and narrow slits in the ground planes—on inductance of overlapping or adjacent microstrips and striplines. The presented set of data should be sufficient for designing circuits into fabrication processes for SCE developed at MIT LL such as SFQSee and SC1/SC2 processes. We especially focused on inductors with deep submicron dimensions, down to 120 nm, in order to provide input for circuit design into the most advanced process nodes, in particular, the newest 150 nm node of the SC2 process.

In the majority of cases we observed a very good agreement between the existing inductance extractors, wxLL (or wxLC) and InductEx, and the measured values without using any fitting parameters if the actually measured linewidth and dielectric thicknesses are used in the LDFs of the software. However, agreement for more complex 3D objects such as vias is not so good and more development is required, especially to describe vias of very small sizes and stacked-staggered vias possessing a very significant inductance.

For transmission line type structures uniform in one direction, wxLC very accurately calculates the full inductance, capacitance, and impedance matrices for structures with arbitrary cross sections of the conductors, e.g. trapezoidal instead of rectangular. The former shape is frequently encountered because of particulars of niobium etching processes. However, wxLC is not applicable for simulating truly 3D structures. Therefore, for all complex structures encountered in integrated circuits, e.g. involving inductor bends, changes in width, connections of inductors, transitions between layers, vias, etc. InductEx is an absolutely indispensable tool which provides high-accuracy inductance extraction from circuit layouts.

Moats in ground planes are essential components of integrated circuits, allowing to trap and keep magnetic flux outside of flux-bias-sensitive parts of integrated circuits. Strong coupling between circuit inductors and magnetic flux trapped in the moats can occur if circuits are cooled in a nonuniform magnetic field changing sign (direction) within the circuits. Similar coupling can be induced upon magnetic field cooling if the field is switched off in the superconducting state.

At small linewidths of and spacings between inductors, which are required for increasing integration scale of SCE, mutual inductance becomes significant and may induce unwanted, parasitic, coupling. On the other hand, knowledge of mutual inductance is important for designing meandered inductors and superconducting transformers. The latter are the critical and most difficult to scale down component of superconductor digital circuits and memories, especially those using ac powering. Mutual inductance will be covered in a separate work.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

Acknowledgments

We are grateful to Vasili Semenov for numerous discussions of inductance measurements and extraction as well as of flux trapping in superconductor integrated circuits. S K Tolpygo would like to thank Mikhail M Khapaev for the access to inductance extraction software wxLL and wxLC, and to Coenrad J Fourie for the access to and help with InductEx. The authors are grateful to Alex Wynn for developing and maintaining a database of inductance measurements, to Ravi Rastogi and Scott Zarr for their help with wafer fabrication, and to the entire MIT LL fabrication team. We would like to thank Leonard Johnson, Mark Gouker, Scott Holmes, and Mark Heiligman for their interest in and support of this work.

This research was based upon work supported by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA), via Air Force Contract FA8702-15-D-0001. The views and conclusions contained in this publication are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of the ODNI, IARPA, or the US Government. The US Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright annotation thereon.

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