Measuring Dynamic On Resistance in GaN Transistors at MHz Frequencies

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Abstract—Gallium nitride (GaN) transistors are desirable for use in power electronics because of their low resistance and capacitance as compared to silicon devices. However, when switched at high frequencies, GaN transistors experience high dynamic on resistance which is both detrimental and difficult to measure. We propose a technique to measure dynamic on resistance of GaN transistors while exposing them to voltage and current waveforms that are similar to those seen in high-frequency (HF) power converters. The technique can be performed at high frequency while disambiguating loss in the output capacitance ($R_{oss}$) and can be applied across frequency, temperature, and off-state voltage. The result is a lumped $R_{on}$ value which is easily incorporated into device models to provide a more accurate basis for design, analysis, and simulation of HF converters. We apply this technique to evaluate commercial GaN transistors at 3 MHz and find that dynamic $R_{on}$ is roughly 4-6 times the room-temperature static $R_{on}$ values usually quoted in datasheets, with device-dependent temperature and off-state voltage dependence.

I. INTRODUCTION

Gallium Nitride (GaN) transistors have attracted great attention due to their ability to operate well at higher frequencies than silicon devices. Nevertheless, GaN transistors experience increased effective on-state resistance when switched at high voltage and frequency due to charge trapping in the device [1]–[3]. This increased resistance (often more than 2x with respect to dc) is variously known as current collapse, dynamic on-state resistance, or dynamic $R_{on}$. Dynamic $R_{on}$ is not commonly reported in datasheets, and how it varies with operating parameters is not well characterized. In addition, characterization techniques for dynamic $R_{on}$ have not been sufficiently developed or agreed upon. Therefore, better measurements of dynamic $R_{on}$ will greatly benefit the design of power electronics incorporating GaN devices and aid in the improvement of the devices.

Some previous efforts have measured dynamic on-state resistance [4]–[10]. The most common approach is to measure both switch current and voltage waveforms during the on state. Since on-state voltage is small and the off-state voltage is large, a voltage clamp must be placed on the switch node to allow for accurate low-voltage measurements. However, some setups suffer from the clamp’s RC time constant which limits operation speed [9]. Although this approach can be useful to determine the instantaneous dynamic $R_{on}$ during a switching event and may provide useful insights into GaN device physics, it is difficult to convert the data into a lumped $R_{on}$ parameter for modeling and simulation. Furthermore, this method is often measured under hard-switching conditions at low frequencies - an inauthentic environment for GaN switches in high-frequency power converters.

Another approach uses thermal data from a soft-switched high-frequency converter to determine dynamic $R_{on}$ [11], [12]. While this approach provides an authentic high-frequency environment, the power converter may limit reconfigurability for different operating conditions and the reliance on thermal measurements is slow and subject to errors which may be difficult to assess. Moreover, as this technique relies on temperature rise as the measurement signal, it is difficult to determine the temperature dependence of both dynamic $R_{on}$ and the off-state losses $P_{oss}$.

We propose an approach that is able to measure dynamic $R_{on}$ at megahertz frequencies, using commonly-encountered HF voltage and current waveforms, while varying frequency, off-state voltage, and temperature. This is done by accurately measuring dc power into an unloaded resonant switching circuit operating under zero-voltage switching (ZVS). The measured input power is entirely attributable to losses, which can be designed to be dominated by conduction loss in the transistor. By subtracting the (small) estimated extraneous losses, one can compute an equivalent lumped dynamic $R_{on}$ for a given operating condition.

The remaining sections of the paper include a detailed description of the proposed technique (II), estimation of non-conduction losses (III), and validation of the technique (IV). We then present experimental dynamic $R_{on}$ data for 3 MHz operation across temperature and voltage for GaN Systems, Navitas, and Panasonic devices (V).

II. MEASUREMENT TECHNIQUE

A simplified schematic of the proposed measurement circuit is shown in Fig. 1, with operating waveforms in Fig. 2. When the switch is on, the inductor current ramps up linearly. When
the switch turns off, \( L_r \) resonates with the capacitor \( C_r \) (in parallel with the device capacitance, \( C_{oss} \)), delivering a half-sine pulse of voltage \( v_{sw} \) across the device. As the switch voltage returns to zero, the switch is turned back on with ZVS. The magnitude and frequency of the currents and voltage pulses can be designed by the choice of \( L_r, C_r, \) the dc input voltage, and the on-time of the FET. It is noteworthy that the on- and off-state waveforms are closely matched to those of some high-frequency converters (e.g. [13]–[17]) and reasonably match a wide variety of soft-switching circuits. Since the variation of dynamic \( R_{on} \) across operating conditions is largely unknown, testing in an authentic environment may provide more useful results for circuit designers.

**Overall Measurement Strategy:**

1) Adjust \( t_{on} \) and \( V_{in} \) to impose off-state voltage pulses at the desired voltage and frequency.
2) Measure the dc power \( P_{in} \) at the input port of the circuit. This can be done accurately with multimeters.
3) Estimate losses not attributable to conduction in the transistor \( P_{other} \) and subtract them from \( P_{in} \).
4) Measure or infer the switch current \( I_{sw.rms} \), and solve for dynamic \( R_{on} = (P_{in} - P_{loss.other})/I_{sw.rms}^2 \).

Though these tasks can be summarized briefly, the challenge lies in making the measurements and estimations in steps 2-4 as accurately as possible.

**Switching Control:** The circuit is controlled by detecting ZVS each cycle to turn the FET on and using a ramp timer to determine the on-time and hence control turn-off (Fig. 3). This is similar to ZVS switching controls used in other applications [18]–[20]. The switch node voltage \( v_{sw} \) is stepped-down and compared to a threshold voltage \( V_{ZVS} \) producing a digital signal \( Z \). When \( v_{sw} \) gets close enough to zero, \( Z \) transitions to low, which turns the DUT on. At the same time, when \( Z \) goes low, the switch \( S_{ramp} \) turns off and thus activates an \( RC \)-timed voltage ramp \( v_{ramp} \). When \( v_{ramp} \) exceeds the threshold \( V_{tmr} \), the digital signal \( TMR \) goes high and the circuit turns the DUT off. Turning the device off causes \( v_{sw} \) to pulse again, and the process repeats.

By manually adjusting \( V_{tmr} \), the on-time can be varied. By varying \( t_{on} \) and \( V_{in} \), the desired pulse voltage \( V_{pk} \) and overall frequency can be achieved. For any operating condition, \( V_{ZVS} \) can be adjusted to achieve ZVS.

**Hardware Setup:** To facilitate testing of multiple devices, we divide the test setup into two components. First, a main board contains the filters\(^1\), input power measurement ports, and a microcontroller and DACs that set signals \( V_{tmr} \) and \( V_{2vs} \). Second, the transistor board contains the DUT and the HF control circuit (Fig. 3). The main board (Fig. 4) connects to the transistor board (Fig. 5) through a cable. This division allows the transistor board to be easily exchanged to test devices.

\(^1\)Since input current \( I_{in} \) demand is low but the input voltage \( V_{in} \) is high (\( \sim 100 \) V), some voltage sources may operate in a light-load mode in which bursts of current are supplied at low frequency (\( \sim 10 \) kHz). A lower frequency filter may be required between the source and the measurement point to prevent source noise from affecting the measurement of \( P_{in} \).
different devices, and it facilitates mounting the transistor board to a hot plate for temperature control. Only dc signals are sent from the main board to the transistor board, including input voltage, logic supply $V_{cc}$, and control reference voltages. Analog voltages are filtered at the comparator inputs to prevent interference. All high frequency signals (e.g. $v_{gs}$ or stepped-down switch voltage $v_{sw,step}$) are contained on the transistor board and are run through short traces.

**Temperature Control:** We control device junction temperature $T_j$ in order to determine the effects of temperature on dynamic $R_{on}$. This is done by heat-sinking the device to a hot plate through a low thermal resistance path as shown in Figures 6-7. Using an aluminum hot plate with high thermal conductivity, and with typical dissipation values in our system, we can assume that the case temperature of the device is very close to that of the hot plate. The temperature at the device junction is then the hot plate temperature $T_h$ plus a small $\Delta T_{jc}$ owing to the non-zero thermal resistance from the junction to the case (Table I). With an appropriately-designed via farm to an exposed copper pad on the reverse side of the PCB, this thermal resistance can be made sufficiently small to be neglected.

To validate this approach, we model the junction-to-case thermal resistance according to the datasheet values, which are about 1–2 °C/W. We model a single via having $R_{via} = 37.4°C/W$ [21]. Assuming 100 vias in parallel, we obtain an effective case-to-hot plate resistance of

![Fig. 6: Side view of thermal control setup. The FET’s source pad is via-farmed to the bottom layer of the PCB which makes thermal contact with the hot plate through an aluminum pedestal (machined flat, with thermal grease applied at each junction). A clamp is also screwed on top of the FET, through the PCB, and into the hot plate to provide even pressure.](image)

![Fig. 7: Thermal model of the thermal control setup. The hot plate temperature $T_h$ is controlled, and heavy via-farming ensures a low thermal resistance connection from the hot plate to the device case ($T_c$) and junction ($T_j$). In the prototype system, the thermal resistance from device case to hotplate is kept below ~1 °C/W.](image)

| Device | $R_{jc}$ | $P_{fet}$ | $\Delta T_{jc}$ | % Error ($\frac{\Delta T_{jc}}{\Delta T_{T_h}}$) |
|--------|---------|-----------|----------------|-----------------------------------------------|
| PGA26E19BA | 1.9 °C/W | 2.35 W | 4.46 °C | 5.56 % |
| NV6131 | 2.2 °C/W | 2.21 W | 4.86 °C | 6.08 % |
| GS66504B | 1.0 °C/W | 2.20 W | 2.20 °C | 2.75 % |

TABLE I: Breakdown of expected errors between junction temperature and case temperature $T_c$, taken from measurements at $T_c = 80°C$ and $V_{pk} = 400 V$. It can be seen that there are small discrepancies between $T_j$ and $T_c$; case temperature control is effectively junction temperature control for purposes of testing across a wide range of temperatures.
$R_{ch} = 0.37^\circ\text{C/W}$, for a total junction-to-plate thermal resistance of approximately $2.5^\circ\text{C/W}$. With $2\,\text{W}$ of loss in the FET (for example), the expected temperature difference from the junction to the hot plate is a negligible $5^\circ\text{C}$.

### III. Other Loss Attribution

Given the simplicity of the circuit, the total losses $P_{\text{in}}$ can be ideally attributed to only a few sources, namely conduction loss in the FET $P_{\text{cond}}$ and other losses including losses in the resonant inductor $P_{\text{lr}}$, in the FET output capacitance’s $P_{\text{oss}}$ [11] [12], in the filter inductors $P_{\text{filter}}$, and in the ZVS detector voltage divider $P_{\text{zvs}}$. By design, the non-conduction losses $P_{\text{other}}$ should be as small as possible; nevertheless, their actual losses can be estimated and subtracted from $P_{\text{in}}$ before computing dynamic $R_{\text{on}}$. Most losses are amenable to accurate estimation; we expound on the major contributors of the loss below, in order of decreasing significance. In doing so, we note that a limitation of the proposed technique is that all unidentified loss sources (or under-represented losses) are construed as additional conduction loss owing to dynamic $R_{\text{ds}}$-on. Thus, it is important to account for other loss sources as accurately as possible. In particular, the design or selection of the passive components in the system, especially $L_r$, is crucial to obtaining precise measurements of dynamic $R_{\text{on}}$. See Appendix A.

![Fig. 8: Typical breakdown of estimated losses’ contribution to total loss (%) based on measurements under 400V $V_{pk}$ at 3 MHz on a Panasonic FET (PGA26E19BA). It is important that $P_{\text{cond}}$ represent a large fraction of the overall loss to prevent errors in estimating $P_{\text{other}}$ from impacting the results.](image)

$\text{C}_{\text{oss}}$ Losses ($P_{\text{oss}}$): The loss associated with the output capacitor of the DUT ($P_{\text{oss}}$) can be high since the transistor terminals experience high-voltage pulses at high frequency; this loss mechanism is known to be significant at high frequencies in GaN devices and some Si devices. In some cases, these losses are ohmic in nature, while in others the losses are hysteretic or have even more complex relationships [11], [12]. This loss can be difficult to disambiguate from conduction loss since both occur within the FET. Nevertheless, one means to disambiguate $P_{\text{oss}}$ from conduction loss is by connecting a second always-off transistor $S_2$ in parallel to the DUT and using the additional loss imposed by the second device as an estimate of $P_{\text{oss}}$, similar to [11], [12].

Because $S_2$ is always off, the operating waveforms shown in Figure 2 are not significantly changed (recall that $C_r$ dominates the switch node capacitance by design, so the added $C_{\text{oss}}$ of the second device does not significantly affect the operating waveforms; if it does, then the resonant capacitance can be slightly adjusted to compensate for this). $P_{\text{oss}}$ can be estimated by performing power output measurements twice: once without $S_2$ in place, and once with $S_2$. The difference in FET loss in the two cases is attributed to $P_{\text{oss}}$. Note that this estimation technique assumes that $P_{\text{oss}}$ of an always-off device is the same as that of a device that switches at high frequency.

**Resonant Inductor Loss:** The resonant inductor $L_r$ accretes loss $P_{lr}$ as current flows through its equivalent ac resistance $R_{lr}$. $P_{lr}$ is estimated from the measured rms inductor current $I_{lr,rms}$ and the equivalent resistance of the inductor at the operating frequency $R_{lr}$. $^2$The inductor current is captured on an oscilloscope and the measured inductor current is used to obtain $I_{lr,rms}$. The resonant inductor loss can then be calculated as $P_{lr} = I_{lr,rms}^2 R_{lr}$. It is important to estimate $P_{lr}$ as accurately as possible since $P_{lr}$ is expected to be one of the most significant contributors to $P_{\text{other}}$. We use a large air-core structure to achieve a high-Q inductor with linear resistance, which keeps $P_{lr}$ both low and predictable. For more details on designing $L_r$, see Appendix A.

**Voltage-Divider Loss:** The switch voltage is monitored in order to obtain ZVS (see Fig. 3). This is done by stepping down the voltage through a voltage divider, which accrues loss. This loss is calculated straightforwardly as $P_{\text{zvs}} = V_{\text{sw},rms} R_{\text{step}}$, where $R_{\text{step}}$ is the total resistance of the divider. $V_{\text{sw},rms}$ may be calculated from the switch voltage as measured on an oscilloscope.

**Turn-on and Turn-off (Transition) Loss:** The loop containing the resonant capacitor and the FET contains some parasitic inductance $L_p$. During every turn-on/turn-off period, $L_p$ is magnetized/demagnetized and dissipates loss in the process.

$^2$To avoid accidentally including probe losses, which can be significant at high frequency, measurement of input power should only be taken with no voltage/current probes attached to the system. Probes are then attached to measure e.g. $I_p$ and $V_{\text{sw}}$. 

![Fig. 9: Method for extracting $P_{\text{oss}}$ loss by adding a second always-off transistor (filters not shown). For the same experiment with this setup, the additional loss is wholly attributable to $P_{\text{oss}}$.](image)
The turn-on and turn-off losses are calculated equivalently as 
\[ P_{\text{on}} = P_{\text{off}} = \frac{1}{2} L_p I_{\text{tran}}^2, \]
where \( I_{\text{tran}} \) is the instantaneous current through the device during a transition event. We infer \( I_{\text{tran}} \) from the measurement of the resonant inductor current. Assuming \( L_p = 1 \) nH, calculations at 3 MHz show that transition losses account for a small portion (0.47\%) of total losses (Figure 8). In many cases, it could be ignored.

We need not consider any turn-on overlap or capacitive discharge loss since the circuit achieves ZVS. Overlap turn-off loss can also be ignored due to the strong snubbing effect of \( C_{\text{oss}} \) and \( C_r \).

IV. Validation

To validate the proposed approach, we performed FET loss measurements across various voltages and verified them as plausible against thermal measurements. For example, we performed thermal resistance measurements on a Panasonic device (PGA26E19BA) by setting \( v_{gs} \) to zero and passing dc current from the source to the drain without heat-sinking the transistor board. Measurements of \( I_{\text{sd}}, V_{\text{sd}}, \) and \( \Delta T \) showed a measured thermal resistance of 35°C/W (case \( \Delta T \) for given dissipation).

We then performed a dynamic \( R_{\text{on}} \) test at (3 MHz and 400 V\text{pk}), again without heat-sinking the device. The experiment produced a calculated FET loss (\( P_{\text{cond}} + P_{\text{oss}} \)) of 1.6 W during operation. We simultaneously recorded the temperature of the FET case with a thermal camera, which was \( \approx 86 \)°C. Letting ambient temperature \( T_A = 25 \)°C, we expect the temperature of the FET to be: \( T_A + 35 °C/W \cdot 1.6W = 81 °C \) which is reasonably close to the measured value of 86°C. We performed several of these tests across various voltages and achieved very similar results. This verifies the accuracy of our loss modeling and adds confidence to our FET loss calculations.

V. Results

In this section, we report experimental results of dynamic on-state resistance of commercial GaN FETs from GaN Systems, Navitas, and Panasonic. For each device, data was recorded at 3 MHz overall frequency, for two different peak off-state voltages (\( V_{pk} = 200 \) V and 400 V), at several temperatures (room temperature, 80°C, and 120°C) as explained in Sec. II. As measurements were performed at the same frequency for similar devices, the same resonant inductor was used while the resonant capacitor value was adjusted slightly.

Results from each device are shown in Figs. 10–12, with dynamic \( R_{\text{on}} \) normalized to the datasheet value at 25°C. The most striking feature of the results is the high overall value for dynamic \( R_{\text{on}} \), roughly 4-6 times the room-temperature static \( R_{\text{on}} \) value on the datasheets. This result is consistent with findings by other research groups [11] that reported FET conduction loss multipliers ranging from 2-3 over their datasheet values at elevated temperatures.\(^3\) The switching environment between this work and that of [11] are somewhat similar (soft-switched at MHz frequencies) and any discrepancy between the findings may be attributable to differences in \( v_{sw} \) voltage and \( i_{sw} \) current waveforms. Nevertheless, the results agree that the dynamic \( R_{\text{on}} \) values are substantially higher than static \( R_{\text{on}} \), even when temperature is taken into account.

In general, dynamic \( R_{\text{on}} \) increases with peak switch voltage as seen in Figs. 10–12. This result is consistent with previous findings [5], [6], [22]. This is most likely due to high electric fields in the channel forcing electrons into trap states, causing dynamic \( R_{\text{on}} \) to increase.

The results in Figs. 10–12 also allow us to see how dynamic \( R_{\text{on}} \) varies with operating temperature. In particular, the results suggest that dynamic \( R_{\text{on}} \) is not a strong function of temperature for these devices. This may be the result of two conflicting phenomena: 1) as temperature increases, electrons in trap states are energized and more readily escape the traps, decreasing dynamic \( R_{\text{on}} \), and 2) as temperature increases, ohmic resistance increases which increases the apparent \( R_{\text{on}} \). The relative strength between these two competing effects may vary across devices, voltages, and temperature ranges.

\(^3\) [11] does not report operating temperatures, but reasonable elevated temperatures can cause dc resistance to increase by 1.5-2 times.
Fig. 11: Thermal sweep across 20 and 80 Celsius show that dynamic $R_{on}$ isn’t a strong function of temperature. Attempts at measuring at 120 Celsius caused the FET to fail. Measurements were done at 3 MHz on a Navitas FET with static $R_{on} = 135 \, m\Omega$ at 200V and 400V $V_{pk}$.

Fig. 12: Thermal sweep across 20, 80, and 120 Celsius show that dynamic $R_{on}$ increases with temperature with decreasing margin. Measurements were done at 3 MHz on a GaN Systems FET with static $R_{on} = 100 \, m\Omega$ at 200V and 400V $V_{pk}$.

Given the importance of accurate loss predictions for design, simulation, and modeling - along with the difficulty of measuring dynamic $R_{on}$, the proposed technique offers a solution to characterizing these significant discrepancies.

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APPENDIX A

IMPLEMENTATION DETAILS

The final component design and selection are summarized in Table II. The choice of resonant components is particular to 3 MHz operation. The filter and IC component selection is not strongly a function of operating conditions; these components are found on the “main board” which is used in common across multiple devices and operating points.

Design of Resonant Components: In this approach, passive component design and selection are crucial to obtain high precision dynamic $R_{on}$ measurements.

The resonant components $L_r$ and $C_r$ in Fig. 1 form a resonant tank. The component values must be chosen to satisfy a variety of constraints, including providing red pulse voltage peak and duration (or, equivalently, resonant frequency). They must also be chosen or designed such that the required current to generate the voltage pulse does not violate switch ratings but provides sufficient conduction loss to make $P_{sw}$ the majority of the loss. An additional constraint is ensuring that $C_r$ is large enough to be the dominant capacitance at the switch node (i.e. $C_r \gg C_{oss}$).

While the resonant component values influence the above metrics, the inductor quality factor $Q$ (i.e. the specifics of its design) matters as well. Inductor loss as a fraction of total loss depends both on the required current (determined by the $L_r$, $C_r$ values) and the inductor’s equivalent resistance (determined by its $Q$). The achievable quality factor is itself a function (albeit not analytically defined) of the inductor value, and this coupling makes optimization difficult.

To aid in design, we wrote a program to check various $L_r$ and $C_r$ pairs (for given inductor quality factor) and to highlight those combinations that satisfy all the constraints. The program output is a color map in the $L_r$, $C_r$ plane, with acceptable and unacceptable regions (e.g. Fig. 13). A generalized control-flow diagram of the program is provided in Fig. 14.

For a given $L_r$ and $C_r$, we calculate the required on-time and input voltage to achieve the desired pulse voltage and overall frequency. To achieve the correct overall period, the on-time is chosen to be

$$t_{on} = \frac{1}{2} \left( T - \frac{\pi}{\omega_r} \right) + \sqrt{\left( \frac{\pi}{\omega_r} - T \right)^2 - \frac{16}{\omega_r}} \tag{1}$$

4The resonant capacitor quality factor $Q_C$ may be important in principle; nevertheless, low-loss NP0/C0G ceramic, porcelain, and mica capacitors in the 500–5000 pF range are readily available with quality factors above 1000.
With $t_{on}$ determined, the dc input voltage required to generate the desired $V_{pk}$ is

$$V_{in} = \frac{V_{pk}}{1 + t_{on} \omega_r} \quad (2)$$

We then analytically compute the inductor and switch rms currents. The rms inductor current is found to be

$$I_{l,rms} = \sqrt{\frac{V_{in}^2 t_{on}^2}{12TL_r} + \frac{V_{in}^2 t_{on}^2}{16L_r^2}} \quad (3)$$

The rms switch current is also found to be

$$I_{sw,rms} = \sqrt{\frac{V_{in}^2 3 t_{on}^3}{12TL_r^2}} \quad (4)$$

We then estimate the losses in the FET based on a hypothesis of its dynamic $R_{on}$ and the losses in the inductor based on a hypothesis of its $Q$; these hypotheses are subject to error, so the results of the program are understood to be estimates only. Nevertheless, although $R_{on}$ is not known exactly and the achievable $Q$ may not be known a priori, multiple plots can be generated for several values of $R_{on}$ and $Q$ to explore the design space.

The color regions are mapped as:

- Green $\rightarrow$ Acceptable - Passes all constraints
- Red $\rightarrow$ Device is expected to overheat
- Blue $\rightarrow$ switch loss $P_{sw}$ does not represent the majority of total loss
- Purple $\rightarrow$ Intersection of Red and Blue case (i.e. device overheats and $P_{sw}$ not majority of loss)

For a given device and frequency, an $(L_r, C_r)$ point is chosen from the acceptable region, sufficiently far from any failure region as the region boundaries are calculated with a hypothesis for dynamic $R_{on}$. Nevertheless, $L_r$ and $C_r$ can be tuned afterwards to account for assumption errors.

After the $L_r$ and $C_r$ values are chosen for a given assumption about the inductor quality factor, it is important that $L_r$ be implemented to achieve at least that quality factor. Since the inductor losses are likely to be substantial, it is also important that its quality factor be well characterized so its losses can be accurately accounted for.

To achieve these features, the resonant inductor is implemented as a large air-core solenoid (Fig. 4) for two reasons. First, air-core solenoids for the 1–10 MHz frequency range can achieve quality factors well above 500. Second, air-core inductors have linear resistance and accurate resistance measurements with an impedance analyzer can be appropriately extrapolated to large-signal conditions.

The design of high-$Q$ air-core solenoids is well understood [23], [24]. A design obtained analytically (e.g. in [24]) can be verified with FEA tools or with available calculators which take into account a number of empirically-determined relationships for air-core solenoids (e.g. [25]). Using this approach, we obtained an inductor with $Q = 680$ at 3 MHz.

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