Programmable Photoelectric Memristor Gates for In Situ Image Compression

Dan Berco,* Diing Shenp Ang,* and Pranav Sairam Kalaga

Solid-state devices that emulate biologic neurons were demonstrated as far back as the early 1990s over floating-gate metal-oxide-semiconductor structures. [1, 2] Alternatively, the study of memristors [3, 4] as artificial synapses has been gaining momentum since the rediscovery of the reversible resistive switching effect. [5–8] Such devices demonstrated complex analog behavior, beyond a nonvolatile on–off operation, like alternating current rectification. [9, 10] Memristors have also been integrated with complementary metal–oxide–silicon (CMOS) logic gates to perform computations either as configurable switches, [11] logic elements, [12–14] or material implication (IMPLY) gates. [15, 16]

Other combinations of logic constructions were proposed as well. In particular, one class of memristor-based architecture was founded on the notation that the high- and low-resistance states of the memory device correspond to a logic level of one and zero, respectively. [17] In this manner, the devices are treated as computational elements and as outputs to latch and store the result. These paradigms are especially suitable for crossbar architectures and fuzzy-logic operations. [18]

More recently, memristive devices have been reported to produce a response to both electric and light stimulations. [19–24] In this context, Tan et al. [25] proposed a hardware-reconfigurable logic gate based on a single light-gated memristor and demonstrated both logical disjunction (OR) and conjunction (AND) operations. However, these gates lack an inherent logical negation (NOT) function, an essential part of the spanning set for a complete logic vector space. Performing this operation mandated a somewhat complex multistep process involving negative voltages. A Boolean OR gate implemented with an optoelectronic switching memristor was also shown by Zhao et al. [26] This emerging research field presents an opportunity for the development of intelligent, bioinspired visual perception apparatuses. Such systems could replace both bionic prostheses [27–29] and robotic eyes, [30] combining image sensors with artificial intelligent image processing [31, 32] into a single platform. [22]

Brain-inspired computing in the post-von-Neumann era should aim to imitate the functionality of biologic neural networks as closely as possible. In this work, we present an approach that combines electric and light inputs to perform fuzzy-logic computations based on optoelectronic memristive gates. These devices are considered to have promising potential for the implementation of high-density, hardware-based artificial intelligent visual sensing platforms, especially when configured in a crossbar paradigm. [33–35] In addition, the presented architecture allows for the implementation of logic functions with minimal components. First, a generic fuzzy photoelectric gate architecture is proposed. Elementary material nonimplication (NIMPLY) and logical true (TRUE) operations are then shown. This is followed by a demonstration of a more complex, three-input NIMPLY-AND gate, constructed of only two memristors and a single pull-down resistor. These gates are then used as building blocks for the design of a configurable matrix multiplication unit that effectively implements in situ image compression. Finally, a hybrid

Solid-state devices that emulate biologic neurons were demonstrated as far back as the early 1990s over floating-gate metal-oxide-semiconductor structures. [1, 2] Alternatively, the study of memristors [3, 4] as artificial synapses has been gaining momentum since the rediscovery of the reversible resistive switching effect. [5–8] Such devices demonstrated complex analog behavior, beyond a nonvolatile on–off operation, like alternating current rectification. [9, 10] Memristors have also been integrated with complementary metal–oxide–silicon (CMOS) logic gates to perform computations either as configurable switches, [11] logic elements, [12–14] or material implication (IMPLY) gates. [15, 16]
computation scheme composed of memristive fuzzy-logic driving defuzzifying CMOS gates is discussed.

1. Results and Discussion

1.1. Photoelectric Fuzzy-Logic Operation

Figure 1a shows a 3D visualization of an optoelectronic memristor-based, fuzzy-logic gate architecture. The image shows double-layer memristors, consisting of a bilayer dielectric (MgO/HfO2). Both materials are sandwiched between two conductive films (indium–tin–oxide [ITO]) acting as top and bottom electrodes (TE and BE, respectively). A MgO layer was added to improve the repeatability of device characteristics and reduce the forming voltage. The improvement in operational characteristics is believed to be associated with the incorporation of Mg species into the hafnia. It may be achieved through either diffusion of dopants from a layered structure or directly added to a sputtering process. In addition, charge localization in the MgO/hafnia interface may play a role by reducing the barrier for Frenkel pairs generation in HfO2. The memristive device was fabricated over a transparent glass substrate that allows visible radiation (light input) to reach the dielectric layer to affect defect stoichiometry. The TE takes the role of the electric input, whereas the common BEs are connected to a pull-down resistor and serve as the gate’s output.

A schematic depiction for a generic material nonimplication (NIMPLY) architecture, implemented by two memristors $S_1$ and $S_2$ connected to a single pull-down passive resistor $R$, is shown in Figure 1b. In this architecture, electric inputs $A_1$ and $A_2$ non-implies their corresponding light-inputs $B_1$ and $B_2$ to a common “wired-OR” output ($Out$). The matching logic table in Figure 1c details both the output logic levels and analog voltages $Vo$. It indicates that the operation of the gate is done in steps. The initial state (or step “0”) is an electrically setting of the memristors from a high-resistive state (HRS) to a low-resistive state (LRS), and as a result the output to a high logic level (TRUE). It is followed by a computation step where either none (step “1”) or only one (step “2”) or both (step “3”) memristors are exposed to illumination. The electrical states transitions of $S_1$ and $S_2$ resulting from such processes would be discussed in detail in the following sections. Note that step “3” may be reached immediately after...
step “1” if both $S_1$ and $S_2$ are illuminated simultaneously or going through step “2” where they are illuminated consecutively.

The table indicates that the output would assume a relatively high level only if at least one electric input is high and its corresponding light input is low. As essentially the output level is the outcome of a voltage divider, it would assume an analog level set between the common ground $Gnd$ and the supply voltage $Vdd$. The ratios of this voltage level are marked as $\alpha = R/(R + R_{LRS})$ and $\beta = R/(R + R_{HRS})$ where $R_{LRS} \ll R_{HRS}$ are the memristor’s LRS and HRS resistances. Because the pull-down value is chosen as $R_{LRS} < R \ll R_{HRS}$, $\alpha$ and $\beta$ would approach logic high and low, respectively. In step “2” where only $S_2$ is supplied with high-voltage and without illumination ($B_1, B_2 = 0$), the output level would be at $\mu Vdd$ with $\mu = 1/(2 + R_{LRS}/R)$. Choosing a relatively large pull-down compared with the LRS resistances yields approximately $\frac{1}{2}Vdd$. In step “3,” where both electric inputs are high, two additional analog intermediate levels are possible as the states of $S_1$ and $S_2$ are permuted. These ratios are marked as $\gamma = R/(R + \frac{1}{2}R_{LRS})$ and $\delta = R/(R + \frac{1}{2}R_{HRS})$. The indicated output ratios in Figure 1c were calculated as an example for $R \geq 3R_{LRS}$ and $R_{HRS} \geq 10R$.

The logic combinations given in the table go through the “$S_2$ follows $S_1$” sequence only. The complementary sequence is identical due to symmetry considerations. Furthermore, the schematic illustration in Figure 1b is intended to highlight the versatility of this architecture. In fact, other configurations using more memristors to implement complex functions are also possible. This work will present both elementary and complex logic operations using this architecture.

1.2. Electric Set and Photonic Reset

An optoelectronic memristive device forms the basis for the hybrid gate functionality discussed in the previous part. This section will present the characterization of such a device. A schematic illustration of the device-under-test along with the measurement setup is given in the inset in Figure 2a. The inset shows how the current $I(v)$ is recorded as a function of the sweep voltage $V_r$, while the output voltage $V(t)$ is recorded as a function of time. The memristors are set from an initial HRS to an LRS. It is achieved by electrically stressing the oxide to generate defect states leading to a reversible soft-breakdown.[38,39] As one of the devices was operated, the other was floated by keeping the corresponding contact in a state of high impedance.

Figure 2a shows the current as a function of the ramp-up voltage applied to the TE of $S_1$. The plots clearly show a transition from a HRS (blue) to a LRS (black and cyan). An initial sweep (“1”) shows the state of a virgin device. First, an electrical set and reset operations were performed to validate the integrity of the device. Once validated, the electrical set and photonic reset functionalities were tested. A first forming sweep (“2”) exhibits current jumps that may be associated with trap formation and annihilation events, whereas the second forming sweep (“3”)
shows a more abrupt soft-breakdown. The soft-breakdown event in the third sweep occurred at about 2.5 V when compared with 2 V in the second because the current compliance setting was increased from 1 to 10 mA. It was done to facilitate a more robust LRS. Sweep (“4”) indicates that the device was indeed formed into a LRS. Figure 2b shows the current as a function of the ramp-up voltage applied to the TE of $S_2$. A transition from a HRS (blue) to a LRS (red and black) occurred in this case as well. The photoreponsivity of the devices was tested through illumination of white light with irradiation power density of 20 mW cm$^{-2}$. The results are shown in Figure 2c,d for $S_1$ and $S_2$, respectively. The figures show the $I$–$V$ sweeps done after forming and after illumination, and as a result the conductance change due to exposure to visible light. It can be seen that irradiation led to reversal of the soft-breakdown, possibly due to light-induced recombination of metastable Frenkel pairs.$^{[40,41]}$

The sweeps in Figure 2a,b shows that generation and combination of traps are not exactly similar for both devices. This may be due to two main reasons. The first is based on the statistical nature of defect formation and annihilation in hafnia. These random events lead to parametric nonuniformities. The second is the relative large size of devices used in this work. A large electrode area can lead to multifilament formation. As more conductive filaments come into play, the statistical distribution is increased. In this case, the behavior may be related to the creation and destruction of multiple filaments during set. This hypothesis is supported by the $I$–$V$ curve provided in the supplementary information that depicts a two-stage formation event.

1.3. TRUE Operation

The purpose of a TRUE operation is to set the output of the gate to a high logic level. It is the mathematical equivalent of assigning a constant value to a function. Here, a single memristor $S$ was connected to a pull-down $R$ and set from an initial HRS to an LRS. The pull-down value ($R = 750 \Omega$) is chosen to be larger than the resistance of the memristor in the LRS and yet much smaller than that of the HRS. Figure 3a shows the memristor current as a function of the ramp-up voltage applied to the TE along with the experimental setup in the inset. The plots show a transition from a HRS (blue) to a LRS (black). An initial sweep (“1”) exhibits trap formation and annihilation events (marked by dashed arrows), whereas the second sweep (“2”) shows a more abrupt soft-breakdown. Once the memristor has transitioned to an LRS, its resistance was lower than $R$, which resulted in a high output voltage level as shown in Figure 3b. The soft-breakdown event in the second sweep occurred at about 6 V when compared with 4 V in the first because the current compliance setting was increased from 10 $\mu$A to 1 mA. In addition, the voltage drop across $R$ came into play as $S$ transitioned to a LRS. This additional forming was done to facilitate a more robust LRS.

The sweep rate is automatically determined on-the-fly by the system as a function of data averaging. The rate would thus be slower at the low currents and faster as the signal-to-noise ratio reduces. The second sweep was thus quicker because the memristor was already partially formed. It led to faster data acquisition convergence by the measurement system for a given $V_r$. This is the reason for the red curve in Figure 3b preceding the blue curve on the timeline, whereas on Figure 3a the blue curve is initiated first. The dashed arrows in the figure correspond to the generation-recombination events marked by a black dashed arrow. Inset: Schematic illustration of the gate along with the measurement setup. b) Superimposed temporal output voltage behaviors indicating that the gate output was indeed set to a high logic level as the device transitioned to a LRS.

Figure 3 thus shows the output level flipping as $S$ transitions from a LRS to a HRS. The reader should keep in mind that Figure 3a shows the voltage supplied to the gate ($V_r$), whereas Figure 3b shows the output level $V(t)$. During this experiment, both current and voltage compliances were operated simultaneously by the measurement systems. Current spiking consecutive events, shown in the blue sweep (“1”) of Figure 3a, manifested...
in a small bump in $V(t)$, as marked by magenta-headed arrows. These were followed by partial filament formation (green-headed arrows) and an output level hitting the compliance since $V_r > 4V$. Prior to this point, the output was almost zero because $S$ was in a HRS which is orders of magnitude larger than $R$. Once the second sweep (‘2’) was executed, the output level began to increase along with the current (gray-headed arrows). It was followed by robust forming (black-headed arrows) and an output spiking up to the compliance. As $S$ transformed to a LRS, most of the supply voltage dropped over $R$. The final sweep (‘3”) confirmed this state.

1.4. NIMPLY Gate

Material nonimplication (NIMPLY) is a logic operation used in generic circuits and Boolean algebra. Along with the TRUE operation, it can be used as a spanning set for the vector space of logic computations. Figure 4 shows the experimental results for a NIMPLY gate, implemented by a single memristor connected to different pull-downs and using various irradiation pulse characteristics (light inputs). The first implementation is shown in Figure 4a along with the corresponding logic table in the inset. In this construction, an electric input $A$ non-implies the light input $B$ to the output $Out$. The table indicates that only the case where the electric input is high and no illumination exists would result in a high level output. As essentially the output level is the outcome of a voltage divider, it would assume an analog level set between the common ground $Gnd$ and the supply voltage $Vdd$. The ratios of this voltage level are marked as $\alpha = \frac{R}{R + R_{LRS}}$ and $\beta = \frac{R}{R + R_{HRS}}$, where $R_{LRS}$ and $R_{HRS}$ are the LRS and HRS resistances, respectively. Because the pull-down value is chosen as $R_{LRS} < R < R_{HRS}$, $\alpha$ and $\beta$ would approach $Vdd$ and $Gnd$, respectively.

A TRUE operation was initially performed to set the state of the memristor $S$ to a LRS and the output high. At that point, both the output voltage $Vo$ and input current $I$ were recorded as a function of time. $Vo$ is given in Figure 4a for $R = 1k\Omega$. The figure shows that the output level started as $\alpha \cdot Vdd$. After a first white-light illumination pulse of 1 s with an irradiation power density of 10 mW cm$^{-2}$, it was reduced to an intermediate fuzzy level, indicating that $S$ transitioned to an intermediate resistive state. The second light pulse caused the output to drop to the bottom level of $\beta \cdot Vdd$ because $S$ completely switched to a HRS. Both the initial and final resistances are given in the current plot of Figure 4b.

The output behavior for a second implementation, using $R = 5k\Omega$, is shown in Figure 4c. Here, a low power density of

![Figure 4. A NIMPLY B (Out = A \rightarrow B) operation; a two-input, fuzzy-logic gate implemented using a single memristor $S$ and a pull-down resistor $R$. a) Fuzzy output voltage levels resulting from the application of 1 s white-light pulses (roughly at the 60 and 75 s points as marked by red arrows and dashed vertical lines) with an irradiation power density of 10 mW cm$^{-2}$. Inset: Logic table with matching analog fuzzy voltage levels. b) Corresponding time-dependent current flowing through the memristor ($S$) indicating a preillumination LRS resistance of $\approx 300 \Omega$ and a postillumination HRS resistance of $\approx 1M\Omega$. Note: A difference of about 10 s exists between the voltage and current timelines (i.e., voltage recording is initiated prior to the current). c) Fuzzy output voltage levels resulting from the application of five, 10 s white-light pulses with a low irradiation power density of 5 mW cm$^{-2}$ and a 5 k$\Omega$ pull-down resistor. d) Corresponding time-dependent current indicating a preillumination LRS resistance of $\approx 750 \Omega$ and a postillumination HRS resistance of $\approx 10M\Omega$.](image-url)
5 mW cm\(^{-2}\) and 10 s long irradiation pulses were used. As a result, the memristor was incrementally reset into a HRS in subtle steps and the output level transitioned through four fuzzy-logic levels before reaching its lowest level. A total of five illumination pulses were thus used to reach this state, as shown in Figure 4c. The corresponding time-dependent current, preillumination LRS, and postillumination HRS resistances are shown in Figure 4d. It can be seen that the input current was reduced as expected with every illumination pulse, as the memristor was stepped toward a HRS. The current reduction steps were nonlinear probably due to the random nature of trap annihilation in HfO\(_2\).\(^{38,39}\)

1.5. NIMPLY-AND Gate

Figure 5 shows the implementation of a more complex logic function. In this case, a nonimplication of an AND operation is demonstrated. This gate uses a common electric input \(A\) (i.e., \(A_1\) and \(A_2\) from Figure 1b were shorted together) to non-implies two light-inputs \(B_1\) AND \(B_2\). The architecture was investigated using two memristors connected to a single pull-down \(R\) with different resistive values. A first implementation is given in Figure 5a with the corresponding logic table in the inset. Initially, both \(S_1\) and \(S_2\) were independently set to a LRS. \(V_o\) is given in Figure 5a for a gate with \(R = 5\ \text{k}\Omega\) and \(V_{dd} = 0.2\ \text{V}\). The figure shows that the output level started as \(\gamma V_{dd}\). After a first visible-light illumination pulse (1 s with an irradiation power density of 20 mW cm\(^{-2}\)) over \(S_1\) (equivalent to a logic input setting of \(B_1 = 1\)), it was reduced to \(\alpha V_{dd}\). This drop indicates that \(S_1\) transitioned to a HRS since \(R_{HRS,1} \gg R_{LRS,1}\). The second pulse over \(S_2\) \((B_2 = 1)\) caused the output to drop to \(\delta V_{dd}\) because at this point both memristors were in a HRS. The time-dependent gate current plot is shown in Figure 5b. It shows an expected step-like drop in the overall current as each memristor is being reset by illumination. The LRS resistances were measured to be \(\approx 3\ \text{k}\Omega\) each.

The output voltage for a second implementation, with \(R = 2.5\ \text{k}\Omega\), is shown in Figure 5c. In this case, both \(S_1\) and \(S_2\) were simultaneously illuminated (equivalent to a logic input setting of \(B_1, B_2 = 1\)). As a result, both memristors were reset into a HRS at the same time and the output dropped to its lowest level almost instantly. As in this case \(R\) was chosen to be approximately equivalent to \(R_{LRS,1}\) in parallel to \(R_{LRS,2}\) (\(\approx 4\ \text{k}\Omega\) each), the output level started as \(\mu V_{dd}\) once the supply was turned on. The current \(I\) flowing through \(R\) is shown in Figure 5d. The overall current was reduced considerably after the illumination pulse.

Process variations affect all semiconductor devices and lead to functional distributions. As the optoelectronic memristive device stands at the core of the photoelectric gate implementation, any

![Figure 5](https://www.advintellsyst.com)
distributions related to gate operation are directly correlated to those of the device. A recently published work shows that the device functions in quite a reliable fashion considering cycle-to-cycle variations.\textsuperscript{[42]} Moreover, as the functional mode of the device in the gate scheme is binary in nature (on/off), it should be less susceptible to such distributions when compared with memristors intended to operate in an analog manner (e.g., implementing an adjustable synaptic weight value) especially because the off state resistance of the device is orders of magnitudes larger than $R$.

As evident from plots, the computation time and current consumption are relatively high. This is probably due to the use of large devices under a probe station environment with pull-down resistors. However, one should keep in mind that the current work aims to present proof-of-concept architecture for photoelectric memristor gates. These may be used as building blocks in fully programmable arrays that implement in situ computations related to visual information acquisition and processing. Such an application is demonstrated in the next section.

1.6. FUZIFFY Member Function

Crisp logic levels may be mapped to fuzzy ones by a FUZZIFY member function, as shown in Figure 6. In this case, the electrical input $A$ was only connected to memristor $S_2$, whereas $S_1$ was grounded, as shown in Figure 6a. Once the state of the gate was set by a TRUE operation, $V_0$ and $I$ (the pull-down current in this case) were recorded. Only $S_1$ was exposed to a series of 1 s white-light illumination pulses at a power density of 5 mW cm$^{-2}$ giving low-exposure doses. The figure shows that the output level started at $\mu \cdot V_{dd}$ where ideally $\mu = 1/(2 + R_{LRS}/R)$. Choosing a relatively large pull-down ($R = 10 \, \text{k}\Omega$) compared with the LRS resistances ($R_{LRS,1} \approx 2 \, \text{k}\Omega$ and $R_{LRS,2} \approx 3 \, \text{k}\Omega$) would yield approximately a $\frac{1}{3}V_{dd}$ level, as shown in Figure 6a.

After the first illumination pulse the output level increased slightly to about $\frac{2}{3}V_{dd}$, indicating that the combined parallel resistance of $R$ and $S_1$ increased to $\approx 3 \, \text{k}\Omega$. The application of three additional pulses resulted in the output voltage level reaching $\alpha \cdot V_{dd}$ and $S_1$ transitioned to a HRS. As $R_{HRS,1} \gg R$, this situation is very similar to that of the NIMPLY gate and $\alpha$ is approximately the same. The pull-down resistor current is shown in Figure 6b. The current rose gradually with every illumination pulse because more of the gate current flowed through $R$, as $S_1$ transitioned to a HRS. The concept of fuzzy computation with signal restoration is shown in Figure 6c. It shows a memristive-based fuzzy computational layer on top of a conventional CMOS logic layer. Electrical inputs are driven from the CMOS layer along with external light stimulations to the fuzzy layer. Once the fuzzy computation is performed, the outputs are defuzzified and the signals restored to explicit logic levels by CMOS gates (as illustrated by the Spice simulation in Figure 6d for an inverter’s output $V_L$).

![Figure 6. FUZZIFY member function; incremental setting of fuzzy voltage levels at the output as a function of successive low-dose irradiation pulses.](image-url)
1.7. In Situ Image Acquisition and Compression

The gate architecture presented herein may serve to construct building blocks for advanced visual systems, integrating sensory and logic computing into an artificial cognitive retina. An array of NIMPLY-AND gates can be used to capture image bitmaps as an imprint of visual information directly onto the crossbar structure, by altering the bitwise conductance values (i.e., LRS to HRS). In this manner, an image is imprinted directly into a processing element, thus avoiding the need to communicate information between a processor and an image sensor as in conventional machine vision apparatuses.[22] This concept is depicted in the schematic diagram of Figure 7a. It illustrates how a set of NIMPLY-AND gates are arranged in an array to capture visual information as a bitwise imprint. Each element is accessed by selection of a word line (WL) and bit-line (BL). Device sizes and separations in artificial retina applications should naturally be engineered to achieve good resolutions when capturing visual information. The parasitic resistance of the “wired-OR” connections is therefore much smaller than the HRS and LRS ones.

Each logic element in the array shown in Figure 7a holds information related to two consecutive pixels of an input image. The NIMPLY-AND gate discussed in this work can thus hold two bits of information. This information can be simply a 2-bit resolution representation regarding this pixel, or more advanced data like red–green–blue (RGB) for gate constructions made of wavelength responsive memristors (e.g., wavelength responsive dielectric layer). The image imprint process may be mathematically represented by an $m \times n$ tensor $M_{ij}$, where $m$ is the number of rows, $n$ is the number of columns, and each element is a $2^{p-1}$ sized vector with $p$ being the number of light inputs ($p = 2$ in this work). Image compression is done by multiplication of $M$ by each of the transposed eigenvectors $\hat{e}_j$. In this manner, the $m \cdot n \cdot 2^{p-1}$ binary tensor is reduced to an $m \cdot n$ analog matrix $Q$ according to

$$q_j = \hat{e}_j^T \cdot \gamma \sum_{k=1}^{p} M_{ij}^k \cdot t_k$$

were $q_j$ are the elements of the row vectors of $Q$, $t_1 = \alpha/\gamma$ and $(t_1 + t_2) = \delta/\gamma$.

Crossbar architectures are considered as promising candidates for achieving ultrahigh densities ($\approx 10^{15}$ bits cm$^{-2}$) similar to the human cerebral cortex ($\approx 10^{15}$ synapses) for futuristic hardware-based artificial intelligent platforms. In this light, the gate structure presented in this work may seem to suffer from a significant drawback. The need for a pull-down resistor can decimate this high-density potential. However, the operational scheme can be engineered to overcome this issue, as shown in the schematic diagram of Figure 7b. The figure depicts the use of a demultiplexer that activates a single WL based on an input address $(addr)$, whereas all the other WLs are kept in a state of high-impedance (high-z). In this manner, only a single pull-down resistor is required per column, as incorporated into the “read” circuitry placed under the array and connected to the

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**Figure 7.** In situ acquisition and compression of visual information using Matlab simulation. a) Schematic illustration of NIMPLY-AND gates arranged in an array to capture visual information as a bitwise image imprint. b) Schematic illustration of a proposed physical crossbar array implementation and read circuitry. c) Initial 50 kbyte image used as an input to the simulation. d) Intermediate image representing fuzzy logic levels processing. e) Final 25 kbyte image after mapping back into a binary bitmap.
BLs. Image information may be evaluated and latched on a row-by-row basis. The main disadvantage is computational time complexity increase from $O(1)$ (for vector matrix dot operations) to $O(n)$. Setting of individual cells in a row to a LRS could be done using a similar approach by floating other BLs, whereas only the required BL is grounded through $R$ (e.g., by using a simple low resistance selector between $R$ and $Gnd$). Image acquisition is performed by first setting all the gates in the array to TRUE. This may be done on a row-by-row basis or over the entire structure, using an appropriate driver able to clamp all the cells to a level of 3–5 V. This step is followed by a bitwise imprint of the image over the array by light-induced resetting of individual devices. Finally, compression and latching can be done via the read circuitry. In this manner, image acquisition speed is constrained over the array by light-induced resetting of individual devices.

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The concepts discussed in this section were demonstrated using a behavioral model based on Matlab code, and the simulation results are shown in Figure 7c–e. For more details regarding the pseudocodes, the reader may refer to the supplementary information. A binary bitmap image of $384 \times 1026$ pixels, shown in Figure 7c, was input into the simulation. This image was processed and reduced to a $384 \times 513$ pixels grayscale, where each analog pixel was represented by an 8-bit unsigned integer, as shown in Figure 7d. Each pixel in this revised image stands for an analog level in the fuzzy computation scheme as the NIMPLY-AND gate output. Once the data are assimilated into the fuzzy logic, it can go through further processing depending on the application. For example, cognitive retinas would be able to perform rudimentary pattern recognition by successive layers of similar crossbar logic structures. Finally, the image was translated back into a simple bitmap again, as shown in Figure 7e. This last stage represents a defuzzifying process that maps analog levels back to distinct zeros and ones. The final image size was exactly half of the original because two memristors were used per gate. It can be seen by comparing Figure 7c,e that the main features were maintained and this process should satisfy the basic requirements from most pattern recognition algorithms.

Therefore, image acquisition and compression may be done in situ by imprinting visual information directly onto the array, thus bypassing the need to communicate between separate image sensor and processor. Considering the nonvolatile nature of the device, the array should be rewritten prior to the next image acquisition. This refreshing operation costs time and energy but should not be immediately labeled as a deal-breaker. Applications that rely on passive devices and require constant refreshing are ubiquitous (e.g., dynamic memories). In addition, the fact that the device may go through a light-induced reset under very low supply voltages ($\approx 0.2$ V) is a non-negligible advantage, considering the energy and time effort needed to communicate information in robotic vision systems. Obtaining a higher compression ratio is also possible by using more memristors per gate, in a similar manner to software algorithms averaging localized pixel information.

**Figure 8.** A CMOS inverter may be used to defuzzify and map fuzzy voltages back to explicit logic levels. Fuzzy voltage levels are represented by a linear ramp-up function supplied as an input signal in a Spice simulation. The inverter output flips in response to different voltages depending on different settings of the inverter’s trip-point. Inset: Illustration of a hybrid computation scheme composed of a memristive-fuzzy-logic gate connected to a defuzzifying CMOS gate.

### 1.8. Fuzzy to Strict Logic-Level Conversion

Opposed to classical logic, founded on the strict notations of true and false, a memristive-based architecture allows for various degrees of truth. Such “gray” definitions present degrees of freedom for more intuitive computations in artificial intelligence fields such as natural language processing or image recognition. However, any fuzzy-logic-based platform would eventually need to interact with conventional logic at some point along the data path. For this purpose, fuzzy levels may be mapped into definitive values by conventional CMOS inverters or buffers. The trip-point of such buffers may be set to a predetermined level by changing the threshold voltage of the n-type device with relation to the p-type one. Thus, a re-mapping threshold may be defined.

**Figure 8** shows the results of a Spice simulation for a CMOS inverter in response to a time-dependent, linear ramp-up input voltage. The trip-point of different inverters was set in three different simulations to about 40, 100, and 155 mV, all with a supply of 0.2 V. The input signal to each inverter represents a fuzzy-logic level. It can be seen that the output voltage in each case initially assumes a high logic level. Once the fuzzy level surpasses the trip-point, the output flips to a low logic level (about 20, 55, and 80 s marks). The concept of fuzzy computation with signal restoration is also illustrated in the inset of the figure. It shows a memristive-based fuzzy gate connected to conventional logic. Once the fuzzy computation is performed, the outputs are defuzzified and the signals restored to explicit logic levels by CMOS gates.
2. Conclusions

In summary, this work presented a memristive, fuzzy-logic architecture for combined photoelectric computations. The architecture is based on resistive memory devices capable of state transitions in response to both electric and light stimulations. Optoelectronic memristive gates with inherent fuzzy functionality hold a promising potential for the implementation of high-density, hardware-based artificial intelligent visual perception platforms, especially when configured in a crossbar paradigm. The functionalities of TRUE and fuzzy NIMPLY, that serve as a spanning base for a logic space, were first presented. It was followed by a demonstration of a more complex logic operation (NIMPLY-AND) over a two-memristor-one-resistor structure. These gates were then used as building blocks in the design and simulation of a configurable matrix multiplication unit that effectively implements in situ image compression. Finally, it was discussed how conventional CMOS may be integrated with a FUZIFYF member function to translate strict logic levels to fuzzy ones and vice versa. The concepts presented in this work could help pave the way toward implementation of light-responsive gate arrays for futuristic bioinspired, intelligent vision platforms.

3. Experimental Section

The electrical measurements were performed at 300 °K using a Keithley SCS4200 semiconductor parameter analyzer and probe station. I–V sweeps were performed in quiet mode to minimize environmental noise. The devices were fabricated on a commercial glass/ITO substrate which was first rinsed in acetone, isopropyl alcohol (IPA), and deionized (DI) water. The substrate was then coated with a 7 nm layer of HfO₂ followed by a 3 nm MgO layer using atomic layer deposition (ALD). Both layers were deposited at a temperature of 200 °C with a nitrogen flow rate of 20 sccm. The HfO₂ was deposited using a tetrakis (ethylmethylamino) hafnium precursor and the MgO with a bis(cyclopentadienyl) magnesium precursor and H₂O as the oxidizing agent. The top ITO electrode was then sputtered onto the sample through a shadow mask with an electrode diameter of 150 μm. The sputtering was done in an ambient pressure of 5 mTorr with an Ar flow rate of 50 sccm and O₂ flow rate of 0.5 sccm using a radio frequency (RF) power of 100 W. Finally, an additional 10 nm Au layer was sputtered through the same shadow mask using a chamber pressure of 2 mTorr, 50 sccm Ar flow rate, and 150 W direct current (DC) power.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors acknowledge the partial funding support by Singapore Ministry of Education under grants MOE2016-T2-1-102 and MOE2016-T2-2-102.

Conflict of Interest

The authors declare no conflict of interest.
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