A sigma-delta modulator with residual offset suppression

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Abstract This Letter presents a low-residual-offset second-order sigma-delta modulator. By inserting a chopper working at low frequency to the mirrored integrator at the first stage of the modulator, the original residual offset is transferred to a high frequency, which can be removed by the filter. Besides, by applying the second-order fractal sequence as the timing of the new added chopper, the residual offset accumulation problem due to the integration at the second stage can be avoided. To evaluate the effect of residual offset suppression conveniently, a programmable timing is integrated to the design to control the state of the added chopper. The presented modulator is fabricated in a 0.18 μm CMOS technology, the core area of which is 0.38 mm2. Based on the measurement results, the DC offset of the sigma-delta modulator with the proposed method is reduced by 85.6 μV. The modulator realizes 64.8 dB dynamic range with 1 MHz sampling rate, which consumes 0.96 mW from a 3.3 V supply.

Keywords: sigma-delta modulator, chopper-stabilization, switched capacitor, low-residual-offset

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

The sigma-delta analog-to-digital converters (ADCs) have been used in many applications, such as audio systems, smart temperature sensors and readout integrated circuits (ROIC) [1, 2, 3, 4, 5, 6, 7, 8]. Such applications often process low level signals with low frequencies, which are easily affected by DC offset and noise when converting to digital domain. Hence, as an essential component of the sigma-delta ADCs, the sigma-delta modulator (SDM) with low offset and low frequency noise is needed.

In order to improve the low frequency performance, chopper-stabilization technique has been widely used in the design of operational amplifiers [9, 10, 11, 12, 13], SDMs [14, 15, 16, 17, 18, 19], etc. The basic concept of the chopper-stabilization is that the input signal is in low frequency domain, while the offset of the operational amplifier is modulated up to the chopping frequency which can be easily filtered out. However, due to the charge injection and clock feed-through at the chopper switches, residual offset is generated, which increases the total offset [20, 21]. For the case with high frequency input, mirrored integrator is introduced to form a high-pass SDM [22, 23, 24, 25], which is inherently immune to the DC offset. The high-pass SDM will also generate the residual offset, which is similar to the SDM with chopper-stabilization. An amplifier sharing technique has been proposed to reduce the residual offset in the SDM, however, the timing of the SDM is complicated [26].

In this Letter, a second-order switched-capacitor SDM with a low-residual-offset mirrored integrator is proposed. For the first stage of the SDM, by modulating the dominant chopper close to the input of the operational amplifier with an additional chopper working at a low frequency, the residual offset generated from the dominant chopper is modulated away from the operational frequency band, which can be filtered out by the following filter. Moreover, by applying a second-order fractal sequence as the timing of the new added chopper, the residual offset accumulation problem at the second stage of the SDM can be avoided. The proposed residual offset suppression technique has been validated by measurement results. A programmable timing is also introduced to the proposed SDM circuit for verification.

This Letter is organized as follows. The proposed low-residual-offset mirrored integrator is analyzed in Section 2, while the design of the total circuit of the proposed SDM is described in Section 3. Section 4 presents measurement results of the proposed SDM. Section 5 draws the conclusions.

2. Residual offset suppression technique

Fig. 1(a) shows a conventional mirrored integrator structure. In order to allow low frequency signal input, chopper CH1 and CH4 are added. The input signal $V_{in}$ is first modulated by chopper CH1 with the clock signal CLKC which works at the chopping frequency $f_{c}$, where $f_{c}$ is the sampling frequency, and finally demodulated back to the baseband by chopper CH4. The DC offset and $1/f$ noise of the operational amplifier are modulated to the chopping frequency by CH4, thus can be eliminated by the following low-pass filter.

As shown in Fig. 1(a), C1 and C2 are the parasitic capacitors of CH1 between the clock path and signal path, while C3 and C4 are the parasitic capacitors corresponding to CH2. Ideally, the capacitance of C1 and C2 are identical, and the same with C3 and C4. Therefore there will be no residual offset since no differential-mode spikes occur. However, due to the process variation, the capacitance of C1 and C2, C3 and C4 may have deviations. Because of the mismatch of the parasitic capacitors, spikes are generated with the chopping frequency at every clock transition, as shown in Fig. 1(b) [27, 28]. After demodulation by CH4, the residual offset will appear at the output of the integrator, which may not be distinguished from the input signal. The chopper CH3 and CH4 will generate the similar problems just as CH1 and CH2. However, the residual offset caused...
by the spikes corresponding to CH3 will be suppressed by the gain of the amplifier, while the spikes resulting from the mismatch of C7 and C8 are in chopping frequency which can be filtered out. Thus, the residual offset caused by CH3 and CH4 can be ignored.

To suppress the residual offset caused by CH1 and CH2 shown in Fig. 1, a residual offset suppression method is proposed. Fig. 2 illustrates the proposed low-residual-offset-integrator (LROI) and the corresponding clock waveforms. Firstly, CH1 used in Fig. 1(a) is removed, and then one side of the two switches controlled by Φ2 are connected to the capacitor Ci1 and Ci2 respectively, instead of the input terminals of the operational amplifier, as shown in Fig. 2(a). The proposed circuit structure does not change the functionality, while the residual offset caused by CH1 is removed.

Secondly, a chopper CHL is inserted for chopping CH2 with the clock signal CLKL as shown in Fig. 2(a). To reduce the residual offset caused by CHL itself, CHL works at a much lower frequency compared with CLKC. To keep the circuit function unchanged, the CLKM, as the clock signal of CH2, is set to vary with the voltage level of CLKL, as shown in Fig. 2(b). When CLKL is in high level, the timing of CLKM is identical to the timing of CLKC, while there is a 180 degree phase shift between CLKM and CLKC when CLKL is in low level. Hence, the spikes generated from CH2 are modulated to the frequency of CLKL, resulting in a zero average residual offset at the output of the LROI theoretically.

For first-order SDMs, the above up-modulated residual offset can be easily removed by a low-pass filter. However, for second-order SDMs, the residual offset generated from the first stage will be accumulated at the second integrator, similarly with the accumulation of the offset generated from the operational amplifier in the first stage [29].

For the convenience of illustration, we assume that the frequency of CLKL is half that of CLKC. Hence, there will be two positive spikes and two negative spikes in one CLKL period. Table I shows the output of the first and the second integrator respectively when assuming the input of the SDM is zero, and the initial value of the two integrators are both zero. \( V_{res} \) represents the equivalent contribution of the offset error for one spike, and T represents the period of CLKL. Although the output of the first integrator turns back to zero after one period T, the output of the second integrator keeps increasing, and the value can be given by

\[
V_{out,2nd} = \frac{1}{2} N^2 - \frac{3}{2} N + 1 + 4(T - 1) \cdot V_{res}
\]  

where N takes 1, 2, 3 and 4, and T is a positive integer.

To solve the similar accumulation problem caused by the offset of the operational amplifier in the second-order SDM, a fractal sequence is applied to the chopping timing [30]. Therefore, we modify the timing of CLKL according to the second-order fractal sequence, and the resulted waveform of CLKL is shown in Fig. 3. The symbol (+) represents the high level state of CLKL, while the symbol (−) represents the low level state, thus the second-order fractal sequence can be represented by the symbol ((+−)(−+)). As shown in Table I, when applying the fractal sequence to the CHL, the residual offset will return to zero theoretically for the second integrator after every two periods of CLKL, resulting in a second-order SDM with less residual offset.
Table I  The accumulation of the residual offset

| T | N | Residual offset | Output of the 1st integrator | Output of the 2nd integrator | Residual offset | Output of the 1st integrator | Output of the 2nd integrator |
|---|---|-----------------|-----------------------------|-----------------------------|-----------------|-----------------------------|-----------------------------|
| 1 | 1 | V_res | 0 | 0 | V_res | 0 | 0 |
|   | 2 | -V_res | V_res | 0 | V_res | V_res | 0 |
| 3 | 4 | -V_res | 2V_res | V_res | -V_res | 2V_res | V_res |
| 4 | 3 | V_res | 3V_res | V_res | -V_res | V_res | 3V_res |

Fig. 4  System diagram of the proposed SDM.

3. Circuit architecture and implementation

To obtain an SDM with low harmonic distortion, a second-order single-loop 1-bit full feed-forward SDM is chosen as the topology of the proposed low-residual-offset SDM. Fig. 4 shows the proposed SDM at the system level. Due to the mismatch of the input sampling paths and the feedback DAC paths for the fully-differential switched capacitor topology, there will be an additional low frequency offset, represented by $V_{path}$. In order to reduce the effect of $V_{path}$ to the total residual offset of the SDM, the chopper-stabilization technique is also executed to $V_{path}$ by adding three choppers CH5, CH6 and CH7. $V_{path}$ is up-modulated by CH6, which can be suppressed at the first stage integrator. The input signal is up-modulated by the chopper CH5 and demodulated by CH6. CH7 is placed in the DAC feedback loop for making the SDM work correctly. The chopping frequency of CH5, CH6 and CH7 is much lower compared with the frequency of CH3 and CH4 so as to reduce the contribution to the total residual offset error. Because the first stage integrator dominates the performance of the SDM, the LROI is applied to the first stage only.

The schematic diagram of the second-order SDM is shown in Fig. 5 with the LROI as the first stage integrator. To obtain a better linearity, non-overlapped clock signals are used to reduce the clock feedthrough and charge injection from the switches.

4. Implementation and measurement results

The proposed low-residual-offset SDM was fabricated in 0.18 um 1P4M CMOS technology. Fig. 6 shows the microphotograph of the designed SDM. The chip core area is 1.4 mm × 0.27 mm. Measurements were taken with a 3.3 V supply voltage, resulting in a power dissipation of 0.96 mW.

The timing of the SDM has been made programmable in order to switch between the on/off state of the chopper CHL. When CHL is in the on state, it works normally with the fractal sequence as described above. However, CHL becomes transparent for the signal when it is in the off state, and the timing of CLKM is modified to be identical with CLKC. Fig. 7 shows the measured output spectral with a $-4$ dBFS ($V_{FS} = 2.56V_{pp}$), 1 KHz input sinusoidal signal when CLKL is in the on and off state, respectively. The first frequency point in the FFT can be considered as the offset voltage of the SDM. As shown in Fig. 7, the normalized offset of the SDM is $-89.6$ dB when CHL is in the on state, and the equivalent absolute voltage is 42.4 $\mu$V. When CHL is in the off state, the normalized offset is $-80$ dB which corresponds to the voltage of 128 $\mu$V. Hence, 85.6 $\mu$V DC offset reduction is obtained with the proposed technique. Generally, the residual offset will increase with the sampling frequency. Thus, for high-speed applications, the effect of the proposed residual offset suppression will be
Fig. 8 shows the measured signal to noise ratio (SNR) and signal to noise distortion ratio (SNDR) versus the input amplitude with the frequency of 1 KHz. The oversampling ratio is 64.

It can be seen that the maximum SNR and SNDR are 64.1 dB and 62.6 dB, respectively. Besides, the proposed low-residual-offset SDM reaches the dynamic range (DR) around 64.8 dB.

Table II summarizes and compares the designed SDM with earlier publications [32, 33, 34]. The equation of the figure-of-merit (FoM) is defined as

\[
    \text{FoM} = \frac{\text{SNDR}}{10 \log_{10} \frac{\text{Bandwidth}}{\text{Power}}} \quad (2)
\]

5. Conclusion

This Letter presents a low-residual-offset second-order 1-bit switched capacitor SDM. Firstly, a LROI is proposed. The residual offset is suppressed by modulating the dominated chopper with another chopper, thus the spikes generated from the dominated chopper are up-modulated to the high frequency, which can be removed by the low-pass filter. Secondly, by applying the second-order fractal sequence to the added chopper, the problem of the residual offset accumulation at the second stage can be resolved. Finally, the chopper-stabilization is used to suppress the offset from the mismatch of the input sampling paths and feedback DAC paths. By means of integrating the programmable timing in the designed SDM, the state of the added chopper can be controlled. The proposed technique reduces the offset by 85.6 \text{V}. The measurement results show that the proposed low-residual-offset SDM achieves 64.8 dB DR, and 62.6 dB SNDR with 0.96 mW power consumption.
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