**vlang**: Mapping Verilog Netlists to Modern Technologies

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**Abstract**—Portability of hardware designs between Programmable Logic Devices (PLD) can be accomplished through the use of device-agnostic hardware description languages (HDL) such as Verilog or VHDL. Hardware designers can use HDLs to migrate hardware designs between devices and explore performance, area and power tradeoffs, as well as, port designs to an alternative device. However, if design files are corrupt or missing, the portability of the design is lost. While reverse engineering efforts may be able to recover an HDL-netlist of the original design, HDL-netlists use device-specific primitives, restricting portability. Additionally, the recovered design may benefit from other computational technologies (e.g., µP, GPGPUs), but is restricted to the domain of PLDs. In this work, we provide a new framework, vlang, which automatically maps Verilog-netlists into LLVM’s intermediate representation (IR). The remapped design can use the LLVM-framework to target many device technologies such as: x86-64 assembly, RISC-V, ARM or to other PLDs with a modern high-level synthesis tool. Our framework is able to preserve the exact functionality of the original design within the software executable. The vlang-produced software executable can be used with other software programs, or to verify the functionality and correctness of the remapped design. We evaluate our work with a suite of hardware designs from OpenCores. We compare our framework against state-of-the-art simulators, thereby outlining our framework’s ability to produce a fully-functional, cycle accurate software-executable. We also explore the usage of vlang as a front-end for high-level synthesis tools.

**Index Terms**—Verilog-to-C Compiler, High-Level Synthesis, Design Portability, Graph Algorithms

I. INTRODUCTION

Programmable logic devices (PLDs) are rapidly evolving: many new devices technologies and programming models are being delivered to the market to meet the computing needs of today [11–15]. However, maintaining portability of designs between past, current or future PLD-technologies is crucial [6, 7]: either for continued product use, or for broad adoption of upcoming technologies.

Traditionally, the portability of hardware designs is generally handled with a portable design medium such as a hardware-description language (HDL) or with specialized design files (i.e., bitstream files). However, if these design mediums are lost or damaged, preserving the design on a programmable device is difficult. If a PLD is still configured with the design’s bitstream, it may be possible to recover the design through *bitstream readback* [3–11]. Additionally, the original PLD model may be deprecated (i.e., the PLD model is no longer manufactured), rendering the recovered bitstream as useless since it cannot be applied to any other PLD. Therefore, the bitstream will need to undergo reverse engineering efforts [10].

Typically, the recovered design will be in the form of primitives native to the device (e.g., device-specific LUTs, DSPs, BRAMs, etc.) and represented with a HDL, which is referred to as a HDL netlist [3, 10]. The primitives used in the HDL netlist may not exist on the desired replacement device. Therefore, additional methods must be applied to remap deprecated-device primitives in the HDL netlist to the fabric of a user-selected modern device. Once this design has been remapped to the new-device’s primitives, it will undergo the corresponding vendor’s compilation flow.

It is not clear if the recovered-design will retain similar performance, power and area characteristics on alternative PLD technologies. Additionally, the recovered hardware design may benefit from other computational technologies (e.g., a µProcessor, GPGPU, CGRA). However, the reverse engineering process restricts portability of the recovered design to only programmable-hardware platforms. This is due the structural encoding of the recovered design: the low-level representation of an algorithm or hardware design limits the possibility to explore design optimizations or modifications during the recovery process (i.e. security patches, performance improvements, power reduction techniques) or to gain an understanding of an application’s intentions.

To address the issue of hardware-design portability with HDL-netlists, we present a framework, vlang. Our framework is a new LLVM [12] front-end which compiles Verilog-HDL netlists into LLVM’s intermediate representation (IR), permitting portability of designs across a variety of computational devices (e.g., x86, RISC-V, ARM, etc.). vlang’s LLVM-IR is high-level synthesis (HLS) compatible, allowing designs to be remapped to alternative PLD technologies supported by modern HLS tools. Additionally, vlang produces LLVM-IR code which is cycle-accurate and functionally
equivalent and to a hardware circuit, and can be used for simulation. We demonstrate that we can compile vlang’s LLVM-IR into a software executable which can be linked into C/C++ programs.

### A. LLVM

The LLVM compilation framework \cite{12} provides a set of toolchains to enable compilation between any supported source-language to any supported target language. Source-languages are compiled into LLVM’s-IR, a strongly-typed RISC instruction-set. The IR is agnostic to the source and target languages. RISC instructions are simple operations such as `add`, `or`, `xor`, `store`, `load`, etc. Instructions may have: (a) 0 or more inputs and (b) 0 or 1 outputs. LLVM encodes the IR using single static assignment \cite{13}. Control flow in the LLVM-IR is handled with the use of basic blocks and control flow graphs. A basic-block requires an entry to the block, a set of control-flow-independent instructions, and an termination point. Termination points can either be branch (br) or return (ret) instructions. Connections between basic-blocks are made if a branch exists to some other basic-block or itself. Connections between basic blocks can be represented graphically, which we refer to as a control flow graph (CFG). CFGs represent conditional flow of a program.

### B. Verilog Netlist

A Verilog-netlist encodes a hardware-design (e.g., an n-bit Adder, a registered and-gate) in terms of a device’s available programmable logic resources (e.g., DSPs, LUTs, etc.). We will refer to a device’s available programmable logic resources as device-specific primitives. In our work, we consider PLD netlist extraction processes which recover designs and represent them as a Verilog-netlist. We provide an example in Fig. 2. In Fig. 2(a) a registered-AND-gate is behaviourally described with Verilog. The same design is presented in Fig. 2(b); however, it has been encoded in terms of device-specific primitives.

### III. VLANG APPROACH

We present vlang, a LLVM-frontend to compile a Verilog netlist into LLVM’s IR. vlang’s compilation process for a Verilog netlist is outlined in Fig. 1. In this process, a Verilog netlist is first parsed into a software model. The software-model holds information regarding the primitives (e.g., LUTs, AND-Gates, Flip-Flops, etc.) in the supplied design, as well as the connections between primitives. During compilation, vlang replaces each primitive in the software-model with an LLVM-function. Replacement LLVM-functions are behavioural descriptions of the device-specific primitives. Once all primitives have been replaced with LLVM-functions, vlang determines the order-of-execution for all of the LLVM-functions through a scheduling algorithm; the explicit parallel structures in hardware need to be mapped into sequentially executed code. After scheduling has completed, vlang will connect LLVM-functions by assembling a set of temporary registers in the LLVM-IR to act as the wiring between modules. Lastly, vlang will produce a C-header file which outlines the calling-convention for this compiled design. The following subsections provide further detail on vlang’s compilation process.

#### A. Mapping Primitive Modules to LLVM

Typical PLD-fabric consists of programmable elements such as look-up tables (LUTs), flip-flops (FFs), digital-signal processing blocks (DSPs) and on-chip memories (RAMs). Routing resources are required to route information to-and-from these hardware-blocks. A Verilog netlist describes the hardware design (which has been configured on the PLD) by structurally representing programmable-hardware resources (i.e., primitives) as Verilog modules. Connections between primitives are explicitly made through the use of wires \cite{14}. For each primitive in the design, vlang will construct an LLVM-function, which we describe below.

\footnote{vlang does not attempt to create multi-threaded programs; this is left as future work.}
B. Inputs and Outputs

vlang remaps a primitive’s inputs into LLVM-software datatypes (e.g., i1, i32, i43) which match the bit-widths of the input. Since a Verilog module may have more than one output bus/net, vlang remaps output nets to pointers (sized to match the datatype-width of the net) as this provides the ability to obtain more than one output from a software function. Fig. 3 demonstrates this remapping, where Fig. 3(a) provides the original Verilog module and Fig. 3(b) provides the LLVM-function declaration generated by vlang.

C. Primitives

Primitives on PLD fabric can either be combinational or clock triggered. We map both classes of primitives to LLVM-functions.

1) Combinational Primitives: Combinational primitives such as {AND, XOR, OR, ...} gates or LUTs, can be mapped directly to LLVM instructions (e.g., an AND gate is replaced with the and instruction). However, replacing the LUT combinational primitive is not as trivial. To map a LUT into an LLVM-function, the following information must be provided: (a) the size of the LUT (i.e., the number of inputs to the LUT) and (b) the LUT-mask. Using the LUT-mask, the sum-of-products formula is constructed, therefore, a sequence of and and or LLVM-instructions can be used to construct the behaviour of the LUT.

2) Flip-Flops: Flip-flops are clock-triggered primitives which provide storage capabilities. Replacement LLVM-functions must be able emulate a flip-flop. Consider the circuit in Fig. 4 where two D-Flip Flops are chained together. At the next clock edge, data at the D inputs of the flip-flops will be stored and displayed at the output: DFF1 will display Q1 at it’s output, and DFF0 will output P1. However, if we were to sequentially update the flips flops from left-to-right (i.e., DFF0 is updated, then DFF1), DFF1 would improperly update to output P1. Unfortunately, a naive replacement LLVM-function would lead to the above error, since vlang produces sequentially executed LLVM-IR. Therefore, the replacement LLVM-function must preserve the parallel-functionality of the flip-flop. We detail how to update LLVM-described flip-flops. The function signature of the replacement LLVM-function for a flip-flop is depicted in Fig. 5.

Each flip-flop replacement must have two global variables, GV1 and GV2. GV1 holds the state of an incoming changes. GV2 holds the current state of the flip-flop, which will then be returned at the end of the function and then updated with the contents of GV1. Additionally, the flip-flop should only change state on a clock-edge. However, LLVM lacks the notion of edge-triggered logic. To capture a clock-edge, the function must be able to recall the previous state of the clock, and then use this memory as a reference against the current clock-signal. XOR-ing the recalled and current clock-signal will dictate if there was a change in the clock. Then, inspecting the current clock level will dictate if this was a positive edge, or negative edge shown in Fig. 6. Other flip-flop types (e.g., asynchronous reset, clock-enabled) can also be constructed as an LLVM function, by modifying this base-design.

3) Other Primitives: We currently do not support DSP and RAM blocks due the large number of configuration possibilities. Instead, if DSPs or RAM blocks are used in the original hardware, we map these to LUT and Flip-Flop elements. Adding support for these primitives is left as future work. We summarize the mapping between Verilog primitives and LLVM Datatypes in Table. I.

D. Module Execution Schedule

All primitives mapped into LLVM functions may only be executed sequentially and must preserve the functionality of the original hardware design. However, Verilog-netlists are a form of dataflow-graphs (DFGs) which expose explicit parallelism between operators. An example of this encoding is pictured in Fig. 7 where the logic equation:

\[ (a \land (\neg (a \oplus b))) \lor c \]  

is encoded as a DFG. Additionally, Verilog-netlists may contain feedback (e.g., a linear-shift feedback register). vlang must determine an ordering of the nodes in the dataflow graph which preserves the data flow between nodes (or synonymously, primitives). Typically, a topological ordering would suffice if the DFG was guaranteed to be acyclic [15]. Since Verilog-netlist DFGs may contain feedback paths, a topological ordering cannot be computed unless feedback paths in the graph can be handled.

Feedback loops in Verilog netlists can be divided into two classes: (a) sequential feedback and (b) combinational feedback. If a feedback edge passes through a clock-triggered element which saves state (i.e., a flip-flop), then this will be
| Verilog | LLVM |
|------------------|------------------|
| **Primitive Declaration** | **Function Declaration** |
| **Inputs and Wires** | **Variables** |
| **Outputs** | **Pointers** |
| **Logic Gates** | **Logic Instructions** |
| **Other Primitives** | **LLVM Functions** |

**Fig. 4:** Motivating example illustrating the need for two global-variables for the LLVM-function equivalent.

```cpp
define void @dff(i1 %d, i1 %clk, i1+ %q) {
    ; Translated Verilog module here..
    ret void
}
```

**Fig. 5:** The LLVM-function signature of a D-flip-flop.

```cpp
define i32 @dff(i1 %d, i1 %clk, i1+ %q) {
    %load.clk = load i32* @out_1.clk_reg
    %clkstate = xor i32 %clk, %load.clk
    %clkstatel = and i32 %clk, %clkstate
    %clk_hi = icmp eq i32 %clkstatel, 1
    ;... if hi, save d.
    ; Remember the state of the clock
    store i1 %clk, i1+ @dff clk_reg
    ;...
}
```

**Fig. 6:** Clock edge detection logic in LLVM.

E. Breaking Sequential Feedback Loops

First, `vlang` must identify if there are cycles in the provided DFG. Recall, the DFG is a directed graph. `vlang` employs Tarjan’s Strongly-Connected Components algorithm \[16\] to the DFG, to discover any strongly-connected components (SCC), thereby discovering cycles. The vertices in each discovered SCC are inspected to `ensure` there exists at-least one flip-flop (as this permits valid feedback paths). If there are no flip-flops in any of the strongly-connected components, `vlang` will abort compilation. Otherwise, the flip-flops within the SCC must be modified to `break` the cycle/SCC (providing an acyclic graph). Our procedure for flip-flop modification is outlined in Algorithm 1. For each flip-flop within an SCC, the modules which provide input (i.e., drivers) to the flip flop are inspected to see if the module is within the SCC. If a flip-flop’s driver is within the vertex set of the SCC, the edge (i.e., wire) connecting them is cut. The flip-flop driver pair is noted down in \( R \), a key-value data structure, as these modules will need to be reconnected after scheduling has occurred.

F. ASAP Scheduling

Once Algorithm 1 has completed, `vlang` generates an ILP formulation for an LP solver to serialize the data-flow graph. We used the system of difference constraints ILP formulation from \[17\], which will provide a solution for an as-soon-as-
Algorithm 1 Cycle Removal Algorithm

1: function CYCLEREMOVAL(G)  
2: \( C \leftarrow \text{TarjanSCC}(G) \) \( \triangleright \) List of SCCs  
3: \( R \leftarrow \text{newKeyValueTable}() \)  
4: if HasCombinationalSCC(C) then  
5: \( \text{abort}() \)  
6: for \( c \in C \) do  
7: for \( v \in c \) do  
8: if IsaFlipFlop(v) then  
9: for \( U \in v.\text{getModulesCon2In()} \) do  
10: if \( U \in c \) then  
11: \( R[v].\text{append}(U) \)  
12: v.\text{removeInput}(U)  
13: return \( R \)

possible (ASAP) execution schedule. We used the LP solver, lp_solve [18], to compute the schedule. As an example, if we serialized the DFG-encoding of Equation 1 using the ILP, the order of execution would be: \((\text{xor, inv, and, or})\). Optimizations to the serialization process could be made by adjusting the SDC-constraint formulation; we have left this as future work.

However, with Algorithm 1 flip-flops will be scheduled to be connected to what it drives. For example, if a flip-flop drives an and gate, the flip-flop will be scheduled to execute just before the and gate. However, the execution schedule of the modified flip-flops are not guaranteed to have the correct data driving it’s inputs. Therefore, modifications to the schedule must be made to allow for the flip-flops to (a) propagate data to the necessary consumers and (b) permit the updating of the flip-flops by reattaching their original drivers. We outline this procedure in Algorithm 2. For each modified flip-flop, we make a copy of the flip flop and set the clock to zero (thereby disabling the flip-flop). This allows the consumers of the affected flip-flops to obtain the data at the correct time. However, the affected flip-flops also need to be updated at the correct time. Recall, vlglang had stored the cut drivers from the flip-flops in a key-value data structure, \( R \). To restore updates to the flip-flops, the original copy of the flip-flop is inserted into the schedule. The insertion point is just-after the latest start-time of all of it’s original inputs. This restores updates to the flip-flop and guarantees the driver’s data to be arriving at the flip-flop at the correct time.

Once the schedule has been generated and modified, the original DFG has been serialized. vlglang will iterate through the schedule, and begin inserting call instructions to the the corresponding primitive-modules. Connections between modules are made with local variables, which are known as alloca instructions in LLVM. vlglang uses the connection-information collected during it’s parsing stage to determine how may temporary registers (in the LLVM-IR sense) should be instantiated to simulate data-transfer using wires. If a subsection of a bus is set or read, vlglang will use and/or logic to set or read from the sub-selected bus.

Algorithm 2 vlglang’s ASAP Scheduling

1: function SCHEDULE  
2: \( G_{\text{circuit}}(E, V) \) \( \triangleright \) This is the DFG of the circuit  
3: \( R \leftarrow \text{CYCLEREMOVAL}(G) \) \( \triangleright \) From Alg. 1  
4: \( S \leftarrow \text{ASAP}(G) \) \( \triangleright \) Computed Serialized Schedule  
5: for \( v \in S \) do  
6: if \( v \in R \) then  
7: \( v_{\text{copy}} \leftarrow v.\text{MakeCopy}() \)  
8: \( v_{\text{copy}}.\text{disableClock}() \)  
9: \( S.\text{replace}(v, v_{\text{copy}}) \)  
10: for \( \{v, (U_0, U_1, \ldots)\} \in R \) do  
11: \( D \leftarrow v.\text{getInputs()} \)  
12: \( T \leftarrow \text{GetLatestStart}(D_0, D_1, \ldots, U_0, U_1, \ldots) \)  
13: \( S.\text{insertAfter}(v, T) \)  
14: return \( S \)

A. OpenCore Benchmarks

OpenCore is an online repository of hardware-designs represented in Verilog or VHDL. A number of designs from OpenCores have been selected to evaluate vlglang’s ability to handle: (a) combinational-logic circuits, and (b) sequential-logic circuit with the possibility of feedback.

1) Combinational Logic Circuits:

adder: is a ripple-carry adder which has (a) three inputs, two 16-bit numbers and a 1-bit carry-in and (b) two outputs, one 16-bit sum, and a 1-bit carry-out.

bcdadder: implements the addition of two 4-bit numbers and a 1-bit carry-in, and produces a 4-bit sum as a binary-coded-decimal with a 1-bit carry-out.

divide: performs the division of two 32-bit inputs, and outputs a 32-bit quotient.
**mod3**: calculates a 3-bit remainder of an 8-bit input in modulo-3 space.

**popcount32**: determines the number of one’s in a 32-bit input and is output onto a 5-bit bus.

2) **Benchmarks with Clock-Triggered Elements**:

- **addertree**: implements an adder tree for five 16-bit inputs, where each pair of inputs are added and registered. The last registered stage is output to a 16-bit bus.
- **andreg**: computes the logical-and between two single-bit inputs, registers and then returns the result.
- **gcd**: calculates the greatest-common-divisor (GCD) between two 32-bit numbers, storing the result in a 32-bit register. This benchmark has feedback.

We selected these benchmarks to provide a variety of tests with respect to: (a) complexity of the design, (b) clock-triggered behaviour with and without feedback, and (c) a variety of applications. However, these benchmarks are described *behaviourally*: vlang can only compile a Verilog-netlist into LLVM-IR. To simulate this environment, we assume that it is possible to retrieve designs from Xilinx's Kintex-7 FPGAs in the form of Verilog netlists. Using `xst` from Xilinx's ISE design suite [23], and targeting a Kintex-7 device (`xc7k70t-1fbg484`), we use `xst` to synthesize a behavioural design from our OpenCores benchmark suite into the Kintex-7's FPGA-fabric, thereby producing a device-specific netlist. The device-specific netlist can be represented as Verilog-netlist using Xilinx's `netgen`.

**B. Results: Functional Correctness and Simulation Comparison**

Recall that `vlang` produces an LLVM-IR program which reproduces the functionality of a Verilog-netlist, and thereby, the original design. Simultaneously, `vlang` also produces a C-header file to permit other programs to reference and use this program. The `vlang` produced LLVM-IR can be linked into a C program using the LLVM framework [24]. Once linked, the corresponding LLVM-IR can either be executed just-in-time [25] or compiled to a binary. To evaluate `vlang`, we compile the test-bench and `vlang`-produced LLVM-IR to a binary using `llc` and `gcc` [26]. Each C test-bench tests a large subset of all possible test-cases, providing an avenue to validate correctness. The number of unique test-cases issued for each OpenCore benchmark is detailed in Table I. We also compare `vlang`'s simulation results and times against two open-source tools, Icarus Verilog [20] and Verilator [19] and a commercial simulation tool, Modelsim. All simulators were provided with the same test-cases. For all of the OpenCore benchmarks, Icarus Verilog, Modelsim and `vlang` produced the correct results. However, Verilator is unable to produce correct results for the `addertree` and `gcd` benchmarks. This is due to a software-bug in Verilator, where certain feedback paths in the Verilog netlist are not handled correctly.

Additionally, we compare the execution time for each testbench with all three simulators. The results are outlined in Fig. 8. This figure does not include results for `bcdadder`, `mod3` and `andreg`, as simulation times were on the order of $10^{-3}$ seconds. For a majority of the benchmarks, `vlang` is able to achieve a faster simulation time, compared to Icarus Verilog, Verilator and Modelsim. This is expected, as `vlang` is a compiled simulator [27]; these styles of simulators are known to provide faster execution time compared to event-driven simulators (Icarus Verilog, Verilator and Modelsim are event driven simulators) [28]. Overall `vlang` is $\sim 37.3\times$ faster than Icarus Verilog, $\sim 3.5\times$ faster than Verilator and $\sim 12.3\times$ faster than Modelsim. Although the focus of this paper is not on simulation, we were able to present `vlang`'s ability to: (a) produce an executable which reproduces the functionality of a Verilog-netlist with an LLVM-IR program and (b) be used a simulation tool, which is competitive in terms of simulation time and is cycle accurate.

**C. Results: Porting between PLDs**

We evaluate `vlang`'s portability by supplying `vlang`-produced LLVM-IR to LegUp, an open-source high-level synthesis tool from the University of Toronto [29]. Using LegUp, we compile the `vlang`-produced LLVM-IR to a Verilog design file, and target two devices, a Xilinx Kintex-7 device (`xc7k70t-1fbg484`) and an Intel Stratix V device (`5SGXEA7N2F45C2`), to study if the functionality of these designs are portable. With the Xilinx device, we also measure performance and area differences: the original design files (i.e., not the Verilog-netlists) are compiled with Xilinx's ISE v14.7 and targeted for the Kintex-7 device. For Xilinx devices, area
is gauged in terms of slices and number of LUTs and performance is measure in terms of $F_{\text{max}}$. For the combinational circuits in our OpenCore Benchmark suite, we used the worst-case estimated logic delay as our measure of $F_{\text{max}}$. The post place-and-route (PnR) area-and-performance metrics for the original design files are outlined in Table III.

### TABLE III: ISE’s Post PnR Kintex-7 Performance and Area metrics for OpenCore benchmarks.

| Benchmark | Slices | LUTs | Flip-Flops | $F_{\text{max}}$ (MHz) |
|-----------|--------|------|------------|------------------------|
| adder     | 4      | 16   | -          | 136.44                 |
| bcdadder  | 4      | 12   | -          | 143.32                 |
| divide    | 477    | 1347 | -          | 11.86                  |
| mod3      | 2      | 3    | -          | 164.10                 |
| popcount32| 19     | 53   | -          | 103.61                 |
| addertree | 16     | 64   | 64         | 671.14                 |
| andreg    | 2      | 4    | 1          | 709.723                |
| gcd       | 41     | 135  | 93         | 429.73                 |

To compare the HLS-generated circuits (from vlang’s LLVM-IR) to the original design files, we compiled the design’s Verilog-netlists with vlang. The vlang-produced IR was then supplied to LegUp. LegUp was set to target a 1 ns clock-period. The HLS-generated circuit then underwent ISE’s compilation flow, again targeting the Kintex-7 device, with a 1 ns clock-period. The results are tabulated in Table IV. Using our C-test-benches along with vlang-produced IR, we confirmed the functionality of the Verilog-netlist from the Kintex-7 was successfully ported back to the same device using LegUp’s test-bench generation flow [29]. However, supplying vlang’s LLVM-IR to an HLS tool may affect the overall area of HLS-generated design as shown in Table IV. This is demonstrated for all benchmarks, where the number of Slices and LUTs increase. As a general trend, the increase in LUTs follows the complexity of the original design: for example, the gcd benchmark uses 135 Slice-LUTs in the original design and the vlang-mapped design uses 5952 LUTs, whereas the adder benchmark uses 16 LUTs in the original design and vlang-mapped design uses 370. Additionally, the divide benchmark is not route-able on the Kintex-7 device (the design uses 97% of the available slices on this particular device). The increase in area is primarily attributed to the HLS-tool’s ability to produce hardware designs from vlang’s LLVM-Functions. The LLVM-function replicates the behaviour of a low-level device-primitive; there is no guarantee that the HLS tool will remap these LLVM-functions into these same primitive. Instead, the HLS tool may proceed to use additional logic resources to implement the LLVM-function. Additionally, extra logic from: (a) the HLS-compiler will be introduced to the original design (e.g., introducing an FSM-controller to enable switching between functions), thereby adding additional area costs and (b) from duplicateds flip-flops on feedback paths. Another notable difference: the combinational circuits have transformed into sequential circuits. This is expected since HLS-tools will infer a clock-signal (which is propagated throughout the entire design). This allows HLS tools to insert register stages into the design, to improve of upon the performance (i.e., breaking-up the critical path, pipe-lining, etc.). This can be desirable, especially if the combinational circuit need not be combinational with the new device. In our case all combinational benchmarks had a significant improvement in $F_{\text{max}}$. If cycle-latency is a sensitive parameter for design portability, the current flow will not be suitable: the additional register stages may affect the circuit’s cycle-latency. LegUp (or any LLVM-based HLS tool) could be modified to reflect the original design’s clock usage (or lack thereof) in vlang’s IR, but this is left as future work. Introducing register stages into combinational logic also prevents Quartus from inferring the entire logic function into a LUT: several LUTS and register would need to be used to infer the behaviour of this function.

### TABLE IV: ISE’s Post PnR Kintex-7 Performance and Area metrics for OpenCore benchmarks (files regenerated with LegUp HLS from vlang). X indicates the design was un-routable.

| Benchmark | Slices | LUTs | Flip-Flops | $F_{\text{max}}$ (MHz) |
|-----------|--------|------|------------|------------------------|
| adder     | 214    | 370  | 389        | 709.72                 |
| bcdadder  | 178    | 318  | 280        | 709.72                 |
| divide    | 9841   | 37189| 36627      | X                      |
| mod3      | 90     | 200  | 151        | 709.72                 |
| popcount32| 319    | 636  | 583        | 709.72                 |
| addertree | 1334   | 2289 | 2175       | 594.88                 |
| andreg    | 11     | 29   | 18         | 709.72                 |
| gcd       | 3625   | 5952 | 8908       | 472.14                 |

Lastly, we confirm the portability of vlang’s LLVM-IR by using LegUp HLS and targeting a Stratix V device. LegUp was set to target a 1 ns clock-period. The LegUp produced hardware design was then compiled with Quartus Prime 18.0
We note on the performance and area characteristics on the HLS-generated circuits for both Xilinx and Intel devices. Although there is no direct area comparison between Intel and Xilinx devices, we compare the number of LUTs used in Xilinx device (from Table III) to the number of ALUTs used in the Intel device. As before, we observe an increase in area: this is primarily attributed to the HLS-tool’s inability to recognize the device-specific primitives as LLVM-functions. Lastly, the achieved $F_{\text{max}}$ for the combinational benchmarks when using vlnc with LegUp HLS improve upon the baseline. Again, this is due to the HLS tool’s ability to (a) insert a clock signal to the design, and (b) insert register stages to break-up the critical path. Referring to Table V and Table VI there is a performance difference between the designs on the Intel device versus the Xilinx device. From our investigation, we discovered that Quartus had purposed many LUTs as routethroughs introducing additional logic delay, thereby affecting the $F_{\text{max}}$. This differs from Xilinx’s ISE, where the majority of designs utilized routing tracks versus LUTs as route-throughs, thereby providing a higher $F_{\text{max}}$ overall. From our experiments, vlnc’s IR was able to port designs originally intended for a Kintex-7 Xilinx FPGA to an alternative device technology, an Intel Stratix V device. We also demonstrated vlnc’s LLVM-IR can be used as a software executable and can be integrated with other software-ecosystems.

V. RELATED WORK

We present a list of works related to: (a) Verilog-to-C compilation procedures, (b) a (c) high-level synthesis technologies

A. Verilog-to-C/C++ Compilers

1) Verilog to C/C++ Compilers for Hardware Simulation:
   - Open-source tools v2c [30], icarus [20] and verilator [19] compile hardware description languages (i.e., Verilog and VHDL) to C/C++ for verification purposes. However, these tools do not present HLS-synthesizable C/C++ code.

2) Mapping Verilog to C++ for High-Level Synthesis:
   - Bomberi et al. explored raising the level of abstraction of hardware designs for: (1) generating and exploring designs with an HLS compiler [31], and (2) using RTL cores as standalone system software [32]. This work was able to recover the IP block specification for system-level design, and enable the derivation of more optimized implementations through HLS.

   - Mahapatra and Schafer identify a similar issue: older designs intended for a target architecture may suffer when porting HDL [33]. Additionally, their may be a need to optimize and port RTL cores [31], [33]. The authors provide a tool, veriIntel2c, to compile a subset of Verilog to a synthesizable set of C [33]. The compiled code is then explored for pareto-optimal designs by applying different code modifications to the C program. The authors built on this work in [34], where they optimize their Verilog to C process.

   - In these works, only either (a) a small subset of Verilog can be retargeted to C/C++ programs [33] or (b) an event scheduler-kernel is required to simulate a circuit in software [31], [32]. Our work is able to produce a software executable that is scheduled at compile time, while handling all gate-level representations in HDL.

B. LLVM-Based High-Level Synthesis Tools

High-level synthesis is a compilation flow which compiles a high-level language (e.g., C/C++) to a hardware description language (e.g., Verilog, VHDL) [35]. A number of algorithmic processes are required to map a high-level language to a hardware description language. The program will undergo a number of static and dynamic program analyses to either restructure the program to expose parallelism and make the program amenable for hardware. The restructured program will then undergo allocation, scheduling and binding. Generally, HLS tools take advantage of pre-existing compilation frameworks, such as LLVM or GCC [29], [36]. Our work produced LLVM-IR, to be suitable for usage with HLS compilers built within LLVM frameworks.

VI. CONCLUSION

This paper proposes a compilation method which transforms Verilog netlists into LLVM-IR to allow portability of these designs across a variety of computer architectures (e.g., $\mu$Processors, FPGAs, etc) by harnessing the LLVM framework [12]. Our method was implemented as an LLVM-frontend, which compiles the Verilog netlist to LLVM’s IR. Our frontend, vlnc, is able to produce an LLVM-IR program which preserves the functionality of the Verilog-netlist and is cycle accurate. Due to this ability, vlnc can be used a verification tool. Lastly, vlnc’s LLVM-IR is HLS-friendly. A number of experiments were performed with
vlang. First, vlang's LLVM-IR was validated by using brute-force comparisons against the original Verilog design. This simultaneously demonstrated vlang's ability to function as a Gate-level simulator and its ability to retain the exact functionality and cycle accuracy of a hardware design as a software executable. Lastly, we evaluated vlang's LLVM-IR for its usage in HLS processes. We demonstrated designs originally on a Xilinx device were successfully migrated to (a) the original Xilinx device and (b) an Intel FPGA. We commented on the HLS-generated hardware design's performance and area metrics against (a) the original design's performance and area metrics on the original device and (b) against the original design compiled to the Intel device.

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