Modern Distributed Data-Parallel Large-Scale Pre-training Strategies For NLP models

Hao Bai
haob2@illinois.edu
University of Illinois Urbana-Champaign
Champaign, Illinois, USA

ABSTRACT
Distributed deep learning is becoming increasingly popular due to the expanding demand for computing resources for deep learning models with a larger amount of parameters. Different from traditional training approaches, data-parallel training allows multiple compute nodes to train large deep learning models simultaneously in order to boost the training efficiency. In this paper, we present and compare six strategies for data-parallel training using PyTorch on the language model GPT-2 with 100M parameters using a qualitative approach. These strategies are Single GPU, Single Parameter Server, Distributed Parameter Server, Horovod, Distributed Parameter Server with Apex mixed-precision strategy, and Horovod with Apex mixed-precision strategy. We also analyze the quantitative experiment results from each strategy. In the end, we draw the conclusion that the Distributed Parameter Server with Apex mixed-precision strategy has the best performance on single node training, while Horovod with Apex is the most robust approach to use when we have single or multiple nodes.

CCS CONCEPTS
• Computing methodologies → Distributed computing methodologies; Machine learning; Parallel computing methodologies.

KEYWORDS
High-Performance Computing, Data Parallelism, PyTorch, Distributed Deep Learning, Natural Language Processing, GPT-2

ACM Reference Format:
Hao Bai. 2022. Modern Distributed Data-Parallel Large-Scale Pre-training Strategies For NLP models. In Proceedings of Inproceedings (HP3C). ACM, New York, NY, USA, 18 pages.

1 INTRODUCTION
Distributed deep learning is continuously gaining popularity due to its performance improvements on very-large-scale (VLS) deep learning models, including Computer Vision and Natural Language Processing [6]. This paper analyzes the state-of-the-art (SOTA) distributed deep learning strategies using conceptual abstractions and underlying mathematical principles, aiming to help researchers and engineers implement the strategies and accelerate the training process.

Since the proposal of the distributed deep learning idea, the two largest deep learning framework, PyTorch [14] and TensorFlow [2], have been working on practical ways to implement the theories concluded by researches proposing this idea [1, 13], with the goal to minimize the changes to the code already written.

Research has been done to test the experimental results of the practical performance of the theories. However, research concerning experimental results and a comprehensive comparison using the most recent tools by PyTorch using NVIDIA Graphical Processing Units (GPUs) is rare. This forces researchers to guess when choosing which strategy to use, especially for those who tackle with VLS models. In our research, we implemented the six most popular strategies in PyTorch to utilize data parallelization for distributed large-scale deep learning using GPT-2 model [16], and showed the first-hand experimental results of all strategies with reasoning and analysis.

Modern distributed VLS deep learning is divided mainly into two categories: data parallelization and model parallelization [8]. As implied by their names, data parallelization is used to distribute data on different devices for parallelization, while model parallelization is to distribute parts of the model on different devices. In other words, they both apportion parts of information to multiple devices. Each type of parallelization has its own intent. Data parallelization can accelerate the training process and increase the batch size to an approximately linear extent because the data is apportioned onto different devices, while model parallelization is invented to reduce the memory usage on one device. The usage and mathematical insight of them can be found in Appendix D.2 and D.8. In our research, we mainly focus on data parallelization, with model parallelization to be addressed in later research.

2 RELATED WORK
In this part, we present the prerequisites for understanding our work. First, we explain why we selected the six data-parallel strategies by surveying the SOTA distributed frameworks and their support for distributed deep learning. Second, as this research is conducted on the HAL mini-super-computer at the National Center for Supercomputing Applications (NCSA) [11], the experimental results are highly related to the architecture and performance of this machine, which we’re going to analyze in Section 3. We also analyze the language model we’re using in this study.
2.1 State-of-the-art Data Parallel Frameworks

Here we provide a brief survey on the SOTA data-parallel frameworks and how they support PyTorch and Tensorflow. The frameworks include PyTorch, Tensorflow, Spark, Horovod, Ray, Hadoop, and Kubernetes, as shown in Table 1.

| Framework      | Distribution Support |
|----------------|----------------------|
| PyTorch         | Official             |
| Tensorflow*     | None                 |
| Horovod*        | Official             |
| Ray             | Official             |
| Kubernetes      | TorchElastic         |
| Spark           | SparkTorch           |
| Hadoop          | None                 |
|                 | TensorFlow on Spark  |

Table 1: Data-parallel strategies on SOTA distributed systems and their relative complexity. ***: frameworks designed for deep learning. "None": no reliable support.

Among all the SOTA frameworks, PyTorch and Tensorflow are designed to be deep learning frameworks, and all of them offer original support for distributed deep learning tasks. Horovod is specifically designed to enable distributed deep learning using PyTorch or Tensorflow. Ray is a framework to scale compute-intensive workloads, but still officially supports distributed PyTorch and Tensorflow. All the three frameworks mentioned above offer reliable official support to distributed PyTorch and Tensorflow.

Kubernetes is a framework mostly for managing containerized applications, but also supports distributed deep learning with successful projects like Kubeflow and TorchElastic. Spark and Hadoop are two frameworks proposed based on the MapReduce algorithm and have the least to do with deep learning, so their support for PyTorch and Tensorflow is even worse.

2.2 High-Performance Computing and HAL

High-Performance Computing (HPC) relies on supercomputers to solve computationally demanding tasks. In the terminology of HPC, a computer with multiple CPU cores and GPUs is called a worker node and a group of these computers is called a cluster, which will be frequently used in this paper. HPC is crucial in distributed deep learning because we need a hardwore backbone for multi-worker training.

HPC systems have multiple computing nodes as they are the essential part of computing resources. For example, HAL is such a mini supercomputer consisting of shared storage, one login node, 16 computing nodes, each consisting of four GPUs and two 20-core CPUs. This research is conducted using HAL.

HAL is constructed using PowerPC CPUs and Tesla V100 GPUs, and it uses SLURM to manage the task queue. HAL uses conda instead of pip for package management. Pip is still available and we can use it as well, typically when the package is not available through conda and local compilation.

2.3 The GPT Language Models

Proposed by OpenAI, the Generative Pre-trained Transformer (GPT) models have been very successful in Natural Language Generation (NLG) tasks [4, 16]. Different from traditional language models, the GPT language models are designed to be stackable - the model can be constructed by stacking multi-head decoder layers proposed by the transformer architecture.

The transformer is one of the most famous encoder-decoder architectures proposed by Google, which aims to train a very deep model using attention layers. Both encoder and decoder in the transformer architecture are stacks of multi-head attention layers, as illustrated in Figure 1. Some insights into the multi-head attention layer are elaborated in Appendix B.

3 DATA PARALLELIZATION VARIANCES

As researchers have found that deep learning models with more parameters can store more information and improve model performance [7], models with more and more parameters are being proposed, especially for language models [18]. For example, the Google T5 language model reached 220 million parameters in 2019 [17], the GPT-3 model consisted of 175 billion parameters in 2020 [4], and the Google Switch Transformer language model rose up to 1.6 trillion parameters in 2021. Every year, the sizes of the language models are expanding at a thousand-fold speed, leading to an urgent upgrade of the distributed systems to train them.

As mentioned in Section 1, the data-parallel strategies are used to increase the training throughput and shorten the time needed for training. However, the workers (GPUs) need a communication interface to synchronize the training data and updated model parameters, which leads to the introduction of the parameter server architecture.

---

1Local compiling means downloading the source code from the official site, then compiling and install it locally.
2Stackability enables the model to be enlarged or shrunk without changing the model input/output, but simply hyper-parameters.
3.1 Parameter Server Architectures

The parameter server architecture is composed of the parameter server nodes and the worker (client) nodes [12]. The clients are in charge of learning the parameters according to the data scattered to them and updating the model parameters using the learning results, while the parameter servers store the updated parameters and manage synchronization. The abstract model of the parameter server architecture is shown in Figure 2.

![Diagram of the parameter server architecture](image)

Figure 2: Abstract model of the parameter server architecture.

According to the number of parameter servers, the data-parallel strategies are split into two main categories: Single Parameter Server (SPS) and Distributed Parameter Server (DPS) strategies. The SPS strategy utilizes one centralized server to authorize the synchronized parameters, while the DPS strategy sets up multiple parameter servers with well-defined typologies to minimize data transmission overhead. In the context of this paper, we denote DPS as a fully distributed one, i.e., each client is itself a parameter server and synchronizes a global copy of parameters.

3.2 Single Parameter Server

The Single Parameter Server strategy is the most naive parameter-server-based strategy for deep learning, with every GPU acting as a client and one worker GPU in charge of not only working but also synchronizing the parameters. In PyTorch and Tensorflow, this strategy is also the easiest to implement, which only requires tiny modifications of the original Python code, usually within less than 5 lines.

Before looking into the actual implementations, it’s necessary to go through the abstract algorithm of SPS under the context of deep learning, which is shown in Algorithm 1. The essence of this algorithm is to use one GPU as both the parameter server and worker, and all other GPUs as mere workers.\(^5\) In other words, only one GPU is used to store and synchronize the gradient needed for carrying on the training process. We represent the parameter server GPU:0 as \(G_0\) in the algorithm below. Note that this algorithm is batch-wise, which means that each time a data batch comes, this algorithm is repeated.

The conceptual illustration of the algorithm from a higher level is shown in Figure 3. Each time the CPU sends an epoch of data to the parameter server GPU:0, the parameter server splits the epoch of data into batches, scatters each batch into pieces, and delivers each batch into a worker GPU for calculation. After synchronization of all GPUs, it aggregates the results and calculates the updated weight and loss. The system then repeats this process. After all the batches are processed, the result is delivered back to the CPU and begins calculating the next epoch.

The implementation of SPS is simple, consisting of selecting the parameter server, transferring the model to the parameter server, and wrapping the model up. The pseudo-code is shown below.

---

\(^5\)We can also interpret the other GPUs as clients that read and write data to the server.
Note that the new batch size in the code should be multiplied by the number of GPUs used, as the parameter server will split the batch into equivalent pieces for each GPU worker. Also, note that SPS does not support multi-node training, as data transfer among nodes is too slow if there is only one parameter server globally.\(^6\)

There is one variant implementation of SPS, and achievable in PyTorch. After profiling the performance, it has been found that the backward propagation process on the parameter server caused much overhead, because all the losses were concatenated on the parameter server. The solution is to leave this work to each client, and the parameter server should gather all the gradients (instead of losses) after each client finishes the gradient calculation.

Although this implementation helps to improve the overall performance, this approach does not balance the load on each GPU either because each input batch is still scattered by the parameter server, which wastes time - the inequality of the GPUs always causes an unfair workload apportionment. To address this issue, the DPS strategy was proposed.

### 3.3 Distributed Parameter Server

In the DPS strategy, each GPU holds the whole bunch of input batches, instead of waiting for the parameter server to scatter them. When a GPU finishes calculating the loss and gradient, it broadcasts them to all other GPU workers, as a result of all GPUs being parameter servers to this GPU.\(^7\) Also, as the data sizes of loss and gradient are fairly small, the transmission overhead is greatly reduced. The algorithm is shown in Algorithm 2.

In DPS, there are multiple CPU processes, each in charge of one GPU worker. Each process should be notified of how many total processes there are, which is called “world size”, in order to make correct decisions. Each of them should also be notified of their order in the system, which is called “rank”, to determine the synchronization order. If there are multiple nodes, the “local rank” is introduced to describe the rank of the process (or GPU) in the node it belongs to. As the system is now fully decentralized, there is no authorized arbitration for the scattering algorithm anymore. Thus, a protocol \(P\) is required for all the processes to follow, which is predefined by PyTorch in its implementation.

Before the calculation for each batch begins, each GPU has one model that’s already synchronized with all other GPUs. When the algorithm begins, all processes are delivered the same data batch, so each process firstly scatters the data batch using a pre-defined protocol, and gets its scattered data, which should be different from all others. Then each process stores the scattered data into the assigned GPU. When the GPU gets the data, it launches the training task immediately, calculating both the loss \(j_i\) and gradient \(w_i\). After this, the GPU transfers the intermediate results to its corresponding CPU immediately. Then the system waits for all the GPUs to finish the calculations, to achieve synchronization. When synchronized, one master process \(C_m\) will gather all the loss and gradient pieces to calculate the final loss and gradient.

The approach that the processes communicate with each other to calculate the final results is called all-reduce. This approach requires one master GPU to gather the intermediate result and calculate the final result. The final results will be broadcasted to all the other GPUs to update their model, so that each model remains synchronized \([15]\).

Algorithm 2: DPS Data Parallel (for each batch)

\[
\text{Data: model } M, \text{ input tensor of size } [x, y, z], \text{ batch size } b, \text{ GPUs } G_i \text{ and CPUs } C_i \text{ where } i \in [0,n] \wedge N, \text{ scattering protocol } P. \\
\text{Result: Result of gradient } W \text{ and loss } J \text{ after this batch.} \\
\]

\[
\text{// The model } M \text{ is stored on each GPU} \\
\text{for } i \in [0,n] \text{ do} \\
\quad \text{\(d_i = \text{scatter}(b, x, y, z, P, C_i)\);} \\
\quad \text{\(\text{store}(d_i, G_i);\)} \\
\quad \text{\(j_i = \text{forward}(d_i, G_i);\)} \\
\quad \text{\(w_i = \text{backward}(j_i, G_i);\)} \\
\quad \text{\(\text{store}(j_i, w_i, C_i);\)} \\
\quad \text{\(\text{sync}(G_0 \rightarrow G_n);\)} \\
\quad \text{\(W, J = \text{allreduce}(w_i, j_i, C_m);\)} \\
\text{end} \\
\text{return } J, W; \\
\]

The conceptual architecture of the DPS strategy is shown in Figure 4. After the CPU launches a master process \(p_0\), the master process automatically spawns enough processes, so that each process will be in charge of one GPU. Each process gets the same copy of data, but they scatter the data differently, according to the pre-defined protocol. Then each CPU is in charge of one GPU to process the learning process, and use the allreduce functionality to synchronize the parameters.

Different from the simplicity when applying SPS, implementing DPS is more complex. For launching multiple processes, the multiprocessing library should be imported. For the initialization part, if the process is going to run on multiple nodes, we should launch the training script on all of the nodes. Moreover, we need
Figure 4: Conceptual architecture of Distributed Parameter Server parallelization approach.

to tell all the processes which one is the top process that launches other processes. The detailed Python script is shown below.

```python
arg.world_size = arg.gpus * arg.nodes
os.environ['MASTER_ADDR'] = '...
os.environ['MASTER_PORT'] = '...
mp.spawn(train, nprocs=arg.gpus,
    args=(args,))
```

We also need to modify the training function to fit the code into the DPS strategy. In the training function train(gpu, args), before wrapping the model, we need to calculate the rank number of each process and initialize the process group. Then we need to notify all processes in the process group where to find the global settings like world_size, using init_method. What’s more, we need to use the distributed scatterer to split each batch of data into pieces with a protocol, so that their scattered data pieces don’t overlap. The pseudo-code is shown below.

```python
rank = args.nr * args.gpus + gpu
dist.init_process_group()
model = construct_training_model()
model = DistrDataParal(model, ..)
train_dataset = construct_dataset()
train_sampler = DistrSampler()
train_loader = DL()
```

In order to make the new version work to fit the code into the DPS strategy. In the training function train(gpu, args), before wrapping the model, we need to calculate the rank number of each process and initialize the process group. Then we need to notify all processes in the process group where to find the global settings like world_size, using init_method. What’s more, we need to use the distributed scatterer to split each batch of data into pieces with a protocol, so that their scattered data pieces don’t overlap. The pseudo-code is shown below.

```python
python main.py -n 4 -g 8 -nr i
```

In this command, n is the total number of the computation nodes, $g$ is the total number of GPUs, and $i$ is the node rank, where $i \in \{0, 1, 2, 3\}$. Note that batch size after applying the DPS strategy is the world size multiplied by batch_size shown in the code above, as each GPU is designated for the same amount of batch_size. This is different from the batch_size in the SPS strategy, where it means the total batch size for the whole system.

If only one node is required for data-parallelization, the launch script torch.launch provided by Python can be a shortcut.\(^9\) To lunch the simplified script, it’s required to add some more arguments when executing. For example, when the program uses 4 GPUs on the node, the following command should be executed.

```bash
python -m torch.distributed.launch
--nproc_per_node=4 main.py
```

The `train_sampler`, `train_loader`, and model wrapping parts should be the same as the multiple nodes multiple GPUs approaches. There are also some other minor fix when using the launch script, which has been gathered on the GitHub repo.\(^9\)

There are also multiple implementations of this strategy. For example, the allreduce algorithm still needs a master process to calculate the final loss and gradient, which cannot be applied to large-scale tasks, because the calculation linearly expands when the number of workers increases. Thus, some DPS strategies replace the allreduce algorithm with the ring allreduce algorithm, which will be illustrated in Section 3.4. Other variants also try to synchronize the losses and gradients directly through the GPUs instead of going through CPUs, thus saving time due to storing the data back to the CPUs.

Although DPS is a very powerful approach to use on one node, for multiple nodes, it’s far from convenient because it requires each node to execute a script. What’s more, PyTorch implements the allreduce algorithm version of the DPS strategy, which is not scalable, as mentioned in the last paragraph. Thus, a bit later than the invention of DPS, the Horovod framework was invented to utilize the MPI backend for inter-node communication, which saves time to modify, and minimizes the data transmission overhead.

### 3.4 The Horovod Framework For DPS

Horovod is a very popular distributed deep learning framework supporting Tensorflow, Keras, PyTorch, and lots of other deep learning frameworks [19]. Different from the original DPS algorithm, Horovod utilizes the ring allreduce algorithm for communication among workers.

The Ring Allreduce algorithm groups all GPUs into a ring topology, with each GPU abstracted as a node [10], which is illustrated in Figure 5. If there are $n$ processes in total, then when synchronizing the parameters, each process will divide its gradient into $n$ blocks, then sends this piece of gradient to the next GPU in the ring for synthesizing. The details of the algorithm are illustrated in the paper proposing Horovod [10], where this algorithm is also proved to be a bandwidth-optimized algorithm.

```plaintext
p0 p1 p2 p3
```

Figure 5: The conceptual schema of the Ring Allreduce algorithm.

Different from the DPS approach in PyTorch, Horovod uses the external backend `openmpi` for communication among the nodes.

\(^9\)Note that this approach is only valid when we are running on one node. On multiple nodes, it’s still required to use the approach mentioned above.

\(^9\)The repository locates at https://github.com/BiEchi/DistributedTrainingGPT2/tree/main/GPT2-Chinese-Parallel-Distributed.
in the network, so before using Horovod, it’s required to install MPI on each computing node. After installing MPI, the node that launches Horovod will be able to communicate with all other nodes requested to run Horovod using the openmpi toolkit. The Python implementation of Horovod is basically the same as DPS except for minor fixes, which is shown below.

```python
hvd.init()
local_rank = hvd.local_rank()
torch.cuda.set_device(local_rank)
train_sampler = DistributedSampler()
train_loader = DataLoader()
optimizer = optim.SGD()
optimizer = hvd.DistributedOptimizer()
hvd.broadcast_parameters()
hvd.broadcast_optimizer_state()
device = torch.device()
```

To run Horovod on one node, simply use the command `horovordrun -np 4 -H localhost:4 python train.py` if there are 4 GPUs on the node. To run Horovod on multiple nodes, it’s required to explicitly list the node name in the launch command. For example, `horovordrun -np 8 -H nodename1:4,nodename2:4 python train.py` will launch a task with 8 processes, and `nodename(n)` is the name of the node in the cluster network, like `hal08`.

### 3.5 Apex Half Precision

Strictly speaking, the Apex half-precision training is not a distributed deep learning strategy per se, but a crucial tool to accelerate deep learning. The half-precision training can work without distributed deep learning, but can be integrated into the DPS and Horovod frameworks after minor changes to code, which accelerates the learning rate to an even higher extent. Thus, this research also takes Apex half-precision training into consideration.

The half-precision (fp16) training is often mixed with single precision (fp32) training. With the introduction of the half-precision floating numbers, GPUs take less storage\(^{10}\) and time to process the data so the batch size can be incremented. Half precision is also capable of utilizing NVIDIA Tensor Cores to further accelerate computing efficiency.

However, only GPUs supporting mixed precision calculations can make use of this strategy. To integrate fp16 into any framework, the first change is to use the backward function provided by Apex amp library. For either SPS or DPS based on the PyTorch framework, the modifications are shown below:

```python
model, optimizer = amp.initialize()
model = DDP(model)
with amp.scale_loss() as scaled_loss:
scaled_loss.backward()
```

Horovod does not officially support amp, but a solution provided by the community is available, with the modification shown below.

```python
with amp.scale_loss() as scaled_loss:
scaled_loss.backward()
```

\(^{10}\)For a more detailed effect of half-precision numbers on memory usage, please turn to Appendix D.1.

### 4 EXPERIMENTS

In this part, we show the experimental results of all the strategies mentioned in Section 3. The developed code is available on GitHub Repository [https://github.com/BiEchi/DistributedTrainingGPT2](https://github.com/BiEchi/DistributedTrainingGPT2).

In our experiments, we utilized the GPT2-Chinese model taken from GitHub Repo [https://github.com/Morizeyao/GPT2-Chinese](https://github.com/Morizeyao/GPT2-Chinese) as the starting point. The hyperparameters are listed in Table 4,\(^{11}\) and the dataset is simply a list of sentences extracted from a novel.

#### 4.1 Qualitative Results

In this part, we use Table 2 to show the arguments of each data-parallel strategy after experiments and the framework support (PyTorch and Tensorflow) for the strategies.

From the table, we see that all the data parallel types are officially supported by both PyTorch and Tensorflow. The baseline model has no parameter servers, the SPS strategy utilizes only one parameter server, and the DPS and Horovod strategies support multiple parameter servers. If the strategy is parameter-server-based, the number of processes should be the same as the number of parameter servers, because each parameter server requires an individual process to launch. More insights into other columns in this table will be introduced after Section 4.2.

#### 4.2 Quantitative Results

In this part, we analyze the GPU utilization and time consumption for each data-parallel strategy.

The GPU utilization for each strategy is shown in Table 3. Note that Horovod with multiple nodes has much higher GPU usage because we sum up the usage in two nodes. From the table, we conclude that under the limitation of 1 node, DPS has the overall best performance, and Horovod is only a little below it, while SPS performs much worse than them, with the GPU utility even worse than the baseline.

We then run the data parallelization on GPT-2 with a parameter amount of 10274200 (10M, similar to GPT2-mini) and 106310400 (100M, similar to GPT2-small), respectively. The time taken by different strategies is shown in Table 5. Note that we don’t run

---

\(^{11}\)The hyperparameters are also available directly in code at [https://github.com/BiEchi/DistributedTrainingGPT2/blob/main/GPT2-Chinese-Parallel/config/model_config.json](https://github.com/BiEchi/DistributedTrainingGPT2/blob/main/GPT2-Chinese-Parallel/config/model_config.json)
We then move on to train with the same arguments using the DPS strategy and the Horovod strategy. The results of SPS, DPS, and Horovod under a total batch size of 16 are shown in Figure 7b. During our training process, we unexpectedly found that DPS runs out of memory under the batch size of 4*4 (4 GPUs, each with batch size 4), while Horovod works well. The reason is related to the difference between the implementation of DPS and Horovod, more on this in Appendix D.7. Therefore, we decreased the batch size to 2 for both DPS and Horovod to get the training process to work. The results are shown in Figure 6b. It’s discovered that it costs slightly more time for Horovod to train on a batch size of 4 than that of 2. Based on this, we estimated the loss function of DPS under a batch size of 4 to be a bit higher than that of 2, as illustrated in the figure. For a detailed analysis of the cause of CUDA OOM errors, please turn to Appendix C and D.

This issue implies the scalability of Horovod. As mentioned in Section 3.4, Horovod uses the ring-allreduce strategy for communication among the workers, which totally gets rid of the inequality of the GPU workers. It’s also discovered that Horovod includes built-in functionalities like cleaning memory caches and balancing the workload on each GPU.

According to the results, it takes approximately half more time for Horovod to finish the training task, probably due to the framework overhead of Horovod, including the memory cleaner mentioned. However, the power of Horovod should not be underestimated: according to Figure 7a, after we implemented the garbage cleaner code for DPS, the training efficiency with respect to time decreased by a factor of 3. Although the codes added are simply del loss and empty_cache(), it causes a huge overhead for memory cleaning, which shows the value of Horovod. For the analysis of the effect of the garbage cleaning on the training performance, refer to Appendix D.4.

Based on these observations, it can be pointed out that DPS takes the first place due to its extremely high performance on one node, while it does not deal with memory cleaning and workload balancing and may cause the code to run out of memory. However, both DPS and Horovod significantly outperform SPS.

We also tested the performance of DPS with Apex and Horovod with Apex. We did not take SPS into consideration because it’s ten-fold slower. We first implemented Apex on DPS using 4 GPUs and a batch size of 4*4 to probe whether the overall mechanism works.

## Table 4: Selected hyper-parameters and their values.

| Hyper-Parameter          | Marker | Size   |
|-------------------------|--------|--------|
| # embedded layers       | n_embd | 768    |
| # heads per attention layer | n_head | 12     |
| # layers                | n_layer| 12     |
| vocabulary size         | vocab_size | 26679 |

## Table 5: Efficiency of different parallel patterns. Horovod-Multi means multi-node Horovod strategy, and Horovod-MA means Multi-node Horovod with Apex mix precision training.

| Parallel Type | PrmSrv | 10M (mini) | 100M (small) |
|---------------|--------|------------|--------------|
| Baseline      | 0      | > 24h      | > 24h        |
| SPS           | 1      | 186m       | > 24h        |
| DPS-Est       | 4      | 26m        | 228m         |
| DPS-Apex      | 4      | 14m        | 133m         |
| Horovod       | 4      | 42m        | 451m         |
| Horovod-Apex  | 4      | 22m        | 198m         |
| Horovod-Multi | 8      | 28m        | 292m         |
| Horovod-MA    | 8      | 18m        | 162m         |

We use the hooks provided by PyTorch to record the loss curve of each strategy with respect to the time or steps during training.

The loss curve of the SPS strategy (4 GPUs, total batch size 4) and benchmark (1 GPU, batch size 4) with respect to training time is shown in Figure 6a. Recall that if the batch size of the SPS solution is 4, each GPU will be assigned only 1 batch. According to the result, under the same batch size, the performance of SPS with 4 GPUs is even worse than the benchmark with only 1 GPU.

Referring back to Section 3.2, the probable cause is that the back propagation on the parameter server takes too much time. As shown in Algorithm 1, the workers can not go on with the next batch of input until the parameter server finishes the back propagation process. This can be further proved when we refer to Table 3: the GPU utilization of SPS is extremely low, and we see some phases when only the parameter server is in use.

We then move on to train with the same arguments using the DPS strategy and the Horovod strategy. The results of SPS, DPS, and Horovod under a total batch size of 16 are shown in Figure 7b. During our training process, we unexpectedly found that DPS runs out of memory under the batch size of 4*4 (4 GPUs, each with batch size 4), while Horovod works well. The reason is related to the difference between the implementation of DPS and Horovod, more on this in Appendix D.7. Therefore, we decreased the batch size to 2 for both DPS and Horovod to get the training process to work. The results are shown in Figure 6b. It’s discovered that it costs slightly more time for Horovod to train on a batch size of 4 than that of 2. Based on this, we estimated the loss function of DPS under a batch size of 4 to be a bit higher than that of 2, as illustrated in the figure. For a detailed analysis of the cause of CUDA OOM errors, please turn to Appendix C and D.

This issue implies the scalability of Horovod. As mentioned in Section 3.4, Horovod uses the ring-allreduce strategy for communication among the workers, which totally gets rid of the inequality of the GPU workers. It’s also discovered that Horovod includes built-in functionalities like cleaning memory caches and balancing the workload on each GPU.

According to the results, it takes approximately half more time for Horovod to finish the training task, probably due to the framework overhead of Horovod, including the memory cleaner mentioned. However, the power of Horovod should not be underestimated: according to Figure 7a, after we implemented the garbage cleaner code for DPS, the training efficiency with respect to time decreased by a factor of 3. Although the codes added are simply del loss and empty_cache(), it causes a huge overhead for memory cleaning, which shows the value of Horovod. For the analysis of the effect of the garbage cleaning on the training performance, refer to Appendix D.4.

Based on these observations, it can be pointed out that DPS takes the first place due to its extremely high performance on one node, while it does not deal with memory cleaning and workload balancing and may cause the code to run out of memory. However, both DPS and Horovod significantly outperform SPS.

We also tested the performance of DPS with Apex and Horovod with Apex. We did not take SPS into consideration because it’s ten-fold slower. We first implemented Apex on DPS using 4 GPUs and a batch size of 4*4 to probe whether the overall mechanism works.
As discussed in Section 3, unlike communication of GPUs, communication of nodes costs much more time because of the network protocol. The communication payload increases because the reduction of the batch size on one GPU requires a more frequent synchronization. As the data length of the gradient does not change for each synchronization, the total communication workload is fully balanced for each GPU worker.

This conclusion can be well supported considering the performance of Horovod-Apex under the batch size of 4/8. As illustrated, different from the relationship in Figure 6b, the training process under a larger batch size is accelerated, making it faster than both batch sizes of 4/4 and 2/8 on Horovod-Apex, which is probably because the performance increase in GPU is greater than the performance decrease due to inter-node communication. However, we still see the performance increase is much lower than the expected value (double) as the inter-node communication forms a bottleneck in the network, as illustrated in Figure 9.

The aggregation of the results is illustrated in Figure 8b for reference. According to the results, it is clear that Horovod-Apex, DPS, and DPS-Apex outperform other methods by a large margin when only one node is reachable, and DPS-Apex is performing the best on one node.

5 CONCLUSION

In conclusion, in the context of PyTorch, under the limitation of one node, it’s recommended to use DPS-Apex to gain the best performance. However, DPS requires a higher GPU memory and is prone to out-of-memory errors. On the contrary, it is more robust for Horovod with the same batch size because of its memory cleaning and workload balancing capabilities. Although Horovod is a bit slower, its robustness provides a very good experience for the training process. With the help of Apex fp16, the performance of Horovod can be lifted up to merely slightly lower than DPS-Apex.

Under the condition of multiple nodes, the operating difficulty of DPS is much larger than Horovod, as it requires running the command on every node concerned. DPS is also not scalable on multiple nodes, because it still requires one master GPU for the AllReduce process. Horovod is feasible for multiple nodes because it can be launched using a single command horovodrun and every node will automatically call mpirun to conduct the task on their GPUs, and it uses the Ring AllReduce for synchronization, which is fully balanced for each GPU worker.

---

The red line (Horovod-Apex) is cut off in the end because it experiences a gradient overflow issue from time to time after that point. But according to official explanations, it does not influence performance.
6 FUTURE WORK

The future work of this research will be focused on two topics:

- Quantitative Results for Data Parallelism on Tensorflow. Although we’ve completed data parallelization on PyTorch and analyzed the qualitative expectations of this on Tensorflow, we have not implemented the model on Tensorflow, so we lack a comparison between PyTorch and Tensorflow.
- Quantitative Results for Model Parallelism on PyTorch. We’ve completed the work to do data parallelism, but we still lack first-hand evidence to show the power of model parallelism.

We’re going to work on this topic so as to achieve these two future goals.

ACKNOWLEDGMENTS

I would like to sincerely thank Prof. Volodymyr Kindratenko for guiding this research and Nuohan Yang for reviewing this manuscript, and Dr. Dawei Mu for providing technical support with the HAL system. This work utilizes resources supported by the National Science Foundation’s Major Research Instrumentation program, grant #1725729, as well as the University of Illinois at Urbana-Champaign.

REFERENCES

[1] Martin Abadi, Ashish Agarwal, Paul Barham, Eugene Brevdo, Zhifeng Chen, Craig Citro, Greg S Corrado, Andy Davis, Jeffrey Dean, Matthieu Devin, et al. 2016. Tensorflow: Large-scale machine learning on heterogeneous distributed systems. arXiv preprint arXiv:1603.04467 (2016).

[2] Martin Abadi, Paul Barham, Jianmin Chen, Zhifeng Chen, Andy Davis, Jeffrey Dean, Matthieu Devin, Sanjay Ghemawat, Geoffrey Irving, Michael Isard, et al. 2016. {TensorFlow}: A System for {Large-Scale} Machine Learning. In 12th USENIX symposium on operating systems design and implementation. OSDI 16. 265–283.
Figure 8: The experimental results of single/multiple node training using Horovod-Apex (a), and a comprehensive comparison of all the optimizations concerned (b).

Figure 9: Gradient communication routine in 2-node configuration Horovod (Ring-Allreduce) architecture. Blue line indicates inter-GPU communication, blue line indicates GPU-CPU communication, and red line indicates inter-node communication, which becomes a performance bottle-neck.

[3] Ali Bakhoda, George L. Yuan, Wilson WL Fung, Henry Wong, and Tor M Aamodt. 2009. Analyzing CUDA workloads using a detailed GPU simulator. In 2009 IEEE international symposium on performance analysis of systems and software. IEEE, 163–174.

[4] Tom Brown, Benjamin Mann, Nick Ryder, Melanie Subbiah, Jared D Kaplan, Prafulla Dhariwal, Arvind Neelakantan, Pranav Shyam, Girish Sastry, Amanda Askell, et al. 2020. Language models are few-shot learners. Advances in neural information processing systems 33 (2020), 1877–1901.

[5] Cristian Buscău, Rich Caruana, and Alexandru Niculescu-Mizil. 2006. Model compression. In Proceedings of the 12th ACM SIGKDD international conference on Knowledge discovery and data mining. 535–541.

[6] Karanbir Singh Chahal, Manraj Singh Grover, Kuntal Dey, and Rajiv Ratn Shah. 2020. A hitchhiker’s guide on distributed training of deep neural networks. J. Parallel and Distrib. Comput. 157 (2020), 65–76.

[7] Jeff Dean. 2015. Large scale deep learning. In Keynote GPU Technical Conference, Vol. 3. 2015.

[8] Jeffrey Dean, Greg Corrado, Rajat Monga, Kai Chen, Matthieu Devin, Mark Mao, Marc V愈加reno Ranzato, Andrew Senior, Paul Tucker, Ke Yang, et al. 2012. Large scale distributed deep networks. Advances in neural information processing systems 25 (2012).

[9] Yanjie Gao, Yu Liu, Hongyu Zhang, Zhengxuan Li, Yonghao Zhu, Haoxiang Lin, and Mao Yang. 2020. Estimating GPU memory consumption of deep learning models. In Proceedings of the 28th ACM Joint Meeting on European Software Engineering Conference and Symposium on the Foundations of Software Engineering. 1342–1352.

[10] W Daniel Hallis and Guy L Steele Jr. 1986. Data parallel algorithms. Commun. ACM 29, 12 (1986), 1170–1183.

[11] Volodymyr Kindratenko, Dawei Mu, Yan Zhan, John Maloney, Sayed Hashemi, Benjamin Rabe, Ke Xu, Roy Campbell, Juan Peng, and William Gropp. 2020. Hal: Computer system for scalable deep learning. In Practice and Experience in Advanced Research Computing. 41–48.

[12] Mu Li, Li Zhou, Zichao Yang, Aaron Li, Fei Xia, David G Andersen, and Alexander Smola. 2013. Parameter server for distributed machine learning. In Big learning NIPS workshop, Vol. 6. 2.

[13] Shen Li, Yanli Zhao, Rohan Varma, Omkar Salpekar, Pieter Noordhuis, Teng Li, Adam Paszke, Jeff Smith, Brian Vaughan, Pritam Damania, et al. 2020. Pytorch distributed: Experiences on accelerating data parallel training. arXiv preprint arXiv:2006.15704 (2020).

[14] Adam Paszke, Sam Gross, Francisco Massa, Adam Lerer, James Bradbury, Gregory Chanan, Trevor Killeen, Zeming Lin, Natalia Gimelshein, Luca Antiga, et al. 2019. Pytorch: An imperative style, high-performance deep learning library. Advances in neural information processing systems 32 (2019).

[15] Pitch Patarasuk and Xin Yuan. 2009. Bandwidth optimal all-reduce algorithms for clusters of workstations. J. Parallel and Distrib. Comput. 69, 2 (2009), 117–124.

[16] Alec Radford, Jeffrey Wu, Rewon Child, David Luan, Dario Amodei, Ilya Sutskever, et al. 2019. Language models are few-shot learners. OpenAI Blog 1, 8 (2019), 9.

[17] Colin Raffel, Noam Shazeer, Adam Roberts, Katherine Lee, Sharan Narang, Michael Matena, Yanqi Zhou, Wei Li, and Peter J Liu. 2019. Exploring the limits of transfer learning with a unified text-to-text transformer. arXiv preprint arXiv:1910.10683 (2019).

[18] Adam Roberts, Colin Raffel, and Noam Shazeer. 2020. How much knowledge can you pack into the parameters of a language model? arXiv preprint arXiv:2002.08930 (2020).

[19] Alexander Sergeyev and Mike Del Balso. 2018. Horovod: fast and easy distributed deep learning in TensorFlow. arXiv preprint arXiv:1802.05799 (2018).

[20] Lao Song. 2021. What should I do when GPU memory runs out? https://zhuanlan.zhihu.com/p/85002487

[21] Xi Xiaoyao. 2021. What should I do when I encounter GPU OOM when during training a deep learning model? https://www.zhihu.com/question/461813359/answer/1916267649

[22] Andy B Yoo, Morris A Jette, and Mark Grondona. 2003. Slurm: Simple linux utility for resource management. In Workshop on job scheduling strategies for parallel processing. Springer, 44–60.
[23] Chen Yun. 2018. GPU and GPU Memory Analysis in Deep Learning. https://zhuanlan.zhihu.com/p/31558973
A THE SLURM QUEUEING SYSTEM

Proposed in 2003, the SLURM (Simple Linux Utility for Resource Management) task manager is a framework for multi-user hierarchical control [22], which is now widely accepted by companies and academia. As super-computers are often used by multiple users in an organization, Linux needs to know how to schedule all the tasks received and make a relatively rule for each user to share computational resources.

When the code and data are in place, the user is required to write a script to launch the task, including which nodes to use, how many GPUs are needed, and the maximum time for executing the script. The script is called by `sbatch <script>`, so it becomes the entry point of the whole program. Essentially, it’s just a bash script indicating resources required of the task, and what the task does. The script will be executed in a blocking way, so the second command in the script must wait until the first command is completed and returned.

As SLURM assigns the user tasks randomly, it’s hard for the user to know which node he is allocating before he launches the script. This problem can be solved by requesting a reservation on SLURM.

B MULTI-HEAD ATTENTION LAYER

The multi-head attention layer is the crucial concept proposed by the transformer architecture to parallelize temporal data modeling. As this layer is crucial in the GPT-2 model, we give a mathematical introduction here for readers to refer to.

B.1 Variances Of Recurrent Neural Network

Before the transformer was proposed, the most popular sequential models were all done by the Recurrent Neural Network (RNN). The basic ideology of each RNN layer is to input a sequence of vectors (words) and output a sequence of vectors with the same position and length. In other words, each RNN layer turns a sentence into another sentence with the same length. Because RNN cannot get future information, bidirectional RNN is proposed, as shown in Figure 10.

As indicated by its name, the communication among the neurons is bidirectional, which means a neuron can get information from both sides of a word in the sentence. However, RNN cannot be parallelized. For example, to get the result $b_3$, we have to first calculate $b_1$ to $b_2$. To solve this problem, the idea of Convolutional RNN is proposed: CNN be used to replace RNN, as shown in Figure 11.

B.2 The Self-Attention Layer

To solve this problem completely, the idea of the self-attention layer was introduced. The task of the self-attention layer is exactly the same as RNN - it takes a sentence as input, and outputs a sentence of the same size. The difference is that all the words are calculated and output at the same time, so they can be paralleled and easier for GPUs to process. Simply put, the self-attention layer is a paralleled RNN.

An example of the architecture of the self-attention layer is shown in Figure 13. The input is three words labeled $x_i$, and each of them goes through an embedding function to get its word vector $a_i$. Then the model defines 3 matrices, which are called the attention heads: the Q matrix for query, the K matrix for key, and the V matrix...
for weighted word vector. Practically, the query is used to match all keys to produce the attention vector $a_{ij}$, which is represented as "at" in the figure. We can represent the calculations in Formula 1.

$$a_{ij} = \frac{q_{i} \cdot k_{j}}{\sqrt{d}}$$

(1)

$$q_{i} = Qa_{i}$$

(2)

$$k_{i} = Ka_{i}$$

(3)

$$v_{i} = Va_{i}$$

(4)

The $a_{i}$ attention vectors are then normalized by passing through the soft-max layer and become the standardized attention vectors $s_{i}$. This vector does a dot-product with the weighted word vector $v_{j}$ and gains the weight vector $w_{j}$ for this word. This is why $v_{i}$ is called the weighted word vector - it is directly extracted from the embedded word and be summed up with the other vector, thus gaining the weight of this word. The word vector can represent the information stored in the word very well.

At last, we sum up the three weight vectors and get the final result $b_{1}$. Repeating this process 3 times, we can get the corresponding output vector $b_{2}, b_{3}$ for $a_{2}, a_{3}$ too, and thus outputting exactly the same form of data like RNN - one $b_{i}$ for each $a_{i}$.

Figure 13: The architecture of a self-attention layer.

Looking back at the gained vector $b_{1}$, we surprisingly find that it has already taken all information in the input sentence $A$. Consider the case we have a sentence of length $l > 3$, the parallization will be much more apparent and thus $b_{1}$ has a larger receptive field with a longer sentence.

However, for the naive model shown above, it’s still not obvious how everything can be parallelized. For example, we have to get $s_{11}$ to get $w_{11}$. In Section B.3, we discuss how to parallelize the calculation using linear algebra (matrix).

B.3 Parallization Of The Self-Attention Layer

Firstly, we notice that the transformer matrices $Q, K, V$ (we now represent them as $W^{Q}, W^{K}, W^{V}$ as they’re essentially weights) for each word are the same. Thus, we can use one matrix to calculate all the results in one-shot using the formula $[q_{1}q_{2}q_{3}q_{4}] = W^{Q}[a_{1}a_{2}a_{3}a_{4}]$, where $[q_{1}q_{2}q_{3}q_{4}]$ is the matrix constructed by stacking the four query vectors. We apply the same strategy to $W^{K}$ and $W^{V}$ for parallelization.

$$Q = W^{Q}A, K = W^{K}A, V = W^{V}A$$

(5)

$$Q = [q_{1}]^{T}, K = [k_{1}]^{T}, V = [v_{1}]^{T}$$

(6)

$$A = [a_{1}]^{T}$$

(7)

Secondly, we observe that the calculation of the attention vectors $a_{i}$ can be parallelized because they’re all using the same query vector $q_{i}$. Thus, we construct the attention matrix $\mathcal{A}$ as shown below.

$$[\alpha_{11} \alpha_{12} \alpha_{13}] = [k_{1}] \cdot q_{1}$$

(8)

We can apply the same process to $q_{2}$ and $q_{3}$, and we find that the $Q$ matrix can be used to solve the whole problem.

$$[\alpha_{11} \alpha_{21} \alpha_{31}] = [k_{1}] \cdot [q_{1} q_{2} q_{3}]$$

(9)

If we generalize the matrix, we get

$$\mathcal{A} = (k_{1})^{T} \cdot [q_{1}]^{T} = k^{T}Q$$

(10)

Then we apply the softmax function and get

$$\hat{\mathcal{A}} = Sm(\mathcal{A})$$

(11)

At last, we can parallelize the last step as well. Taking our example as the starting point, we have

$$b_{1} = [v_{1}v_{2}v_{3}]$$

(12)

$$b_{1}b_{2}b_{3} = [v_{1}v_{2}v_{3}]$$

(13)

To put in matrix, we have the simplified form

$$B = V \cdot \hat{\mathcal{A}}$$

(14)
matrix and the standardized attention matrix to get the output matrix \( B \). The whole process is shown below.

\[
Q = W^Q A, K = W^K A, V = W^V A \\
\mathcal{A} = k^T Q \\
\hat{\mathcal{A}} = Sm(\mathcal{A}) \\
B = V\hat{\mathcal{A}}
\]

(15) (16) (17) (18)

B.4 Multi-head Attention

The multi-head attention splits the attention head up to multiple smaller heads, and the architecture is shown in Figure 14. Using the multi-head attention layer, the dimension of the features is further expanded to a factor of the number of attention heads.

The multi-head attention takes all information in the sentence to train one word. Thus, this word has no information about where the words it’s learning from are in the sentence. This can become a serious problem, as failure to locate words makes the transformer lose the ability that RNN has. To overcome it, the Positional Encoding technique is introduced, which adds a position vector \( e_i \) to the embedded word \( a_i \).

This process has a prototype of concatenation. Suppose we have a one-hot positional vector \( p_i \), in which the only number 1 indicates the position of the word in a sentence, then we have the formula:

\[
\left[ W_A, W_P \right] x_i = W_A \cdot x_i + W_P \cdot p_i = a_i + e_i
\]

(21)

C.1 The CUDA GPU Memory

GPU memory is different from CPU memory because GPU memory is exclusively used by the GPU streaming multiprocessors on the card, while CPU memory (which is often called the general memory or simply "memory") is used by a series of devices including the CPU itself. The bandwidth of GPU memory (GDDR6) is 3 times faster than the general memory (GDDR4) due to a great requirement of high-performance computing, and thus it’s not recommended to train a deep neural network on a CPU instead of a GPU.

However, as CPU memory is commercialized and can be installed by the user himself, the size of CPU memory is often much larger than the GPU memory. Thus, under extreme circumstances, it’s still a valid way to change GPU memory to CPU memory to get the OOM issue solved, as will be discussed in Appendix D.5.

C.2 Estimating the Memory Use of Models

Before solving the OOM issue, we need to first estimate which part of the model causes the usage of CUDA memory [23]. Basically, it’s divided into three parts: parameters of the model, parameters of the optimizer for the model, and I/O for each layer in the model.

C.2.1 Parameters of the Layer (\( p_l \)). The number of parameters of the model is simply the sum of the weight and bias in all layers in the model, and doesn’t depend on the size of input data. In detail, the model is loaded after the command \( \texttt{model} = \text{MyGreatModel}() \), \( \texttt{cuda}() \) or \( \texttt{model.to(cuda:1)} \), and can be examined using the command \( \texttt{model.parameters()} \). It should also be noted that only some layers have weights (like CNN layer, RNN layer, FCN layer, BatchNorm layer, and Embedding Layer), while the others do not

13Extreme circumstances mean cases where no multi-GPU solution is possible, a large amount of memory is required to start the training (more than one GPU can satisfy), and cannot solve by reducing the model size.
(like activation layer, dropout layer, and pooling layer) [9]. Table 6 is a summary of the layers with their layer weights amount.

| Layer         | Layer Input | Layer Output | Weights Amount $p_l$ |
|---------------|-------------|--------------|----------------------|
| Linear        | $m$         | $n$          | $m \cdot n$          |
| Conv2d        | $c_i, k$    | $c_o$        | $c_i \cdot c_o \cdot k^2$ |
| BatchNorm2d   | $n, c, h, w$| $n, c, h, w$| $2 \cdot n$          |
| Embedding     | $n, w$      | $n, w, h$    | $n \cdot w$          |

Table 6: Parameter number in memory for one layer after PyTorch, originally proposed by [21].

Note that the number of parameters is not the same as the memory usage in memory, as each parameter has a data size. For example, float32 will multiply the number argument by 4 to get the memory usage, double will multiply it by 8, and so on.

C.2.2 Parameters of the Layer After Optimization ($p_l$). The parameter of the optimizer is the parameter generalized when back-propagating in the optimization state. In other words, the parameter of the optimizer is the gradient (AF(w)) and momentum (o).

As different optimizers utilize different optimization technologies, the actual amount of the parameters of the optimizer is also variable. For SGD, it takes approximately the same parameters as the model, which means that the parameter amount will be doubled after this optimizer. For Adam, it takes approximately 3 times as much as the model parameter, including the size of SGD, and double the size of momentum information, which means that the total parameters will be 4-fold after optimization. For reference, the memory storage of the optimizers is shown in Table 7 [3].

| Layer Optimizer | Layer Gradient | Momentum | Result $p_l$ | Factor n |
|-----------------|----------------|----------|--------------|----------|
| SGD             | $p_l$          | $p_l$    | $2p_l$       | 2        |
| SGD-Momentum    | $p_l$          | $p_l$    | $3p_l$       | 3        |
| Adam            | $p_l$          | $p_l$    | $4p_l$       | 4        |

Table 7: Parameter number in memory for one layer after applying the optimizer in PyTorch, originally proposed by [23].

In PyTorch, the optimizer is not layer-specific, as each optimizer applies to all layers in a model. Thus, we first calculate the model parameter without the optimizer and then multiply it by the optimizer factor. If we represent $p^i_l$ as the parameter in layer $i$, $l_i$ as the layer number, and $p_m$ as the parameter in the whole model, then the parameter number in the whole model can be calculated by Formula 22, as shown below.

$$p_m = \sum_{i=0}^{n} p^i_l \cdot n$$

C.3 Layer Output and Model Input

Except for memory for each layer, we also need memory for data produced by each layer. Thus, if we represent $p^i_o$ as the sum of all the outputs of layer $i$, the total memory usage for storing all the parameters for each layer output can be calculated by Formula 23. This formula holds because the output of each layer is the input of the next layer - we don’t need to add the layer inputs in the formula.

$$p_o = \sum_{i=0}^{n} p^i_o$$

(23)

The size of input data for the model can usually be omitted, because we always use an iterator to split the data into batches - a 5-GB large dataset can be split up into a large amount of 1-MB data, which is handled by the data loader. The illustration of the layer output and model input contributing to memory storage is in Figure 15.

![Figure 15: The illustration of storage of output of each layer $p_o$ (the read lines) and the storage of input of the model $p_b$ (the dashed green line). The latter one is usually ignored because we typically don’t calculate it’s gradient, and it’s usually split into pieces so it does not occupy too much storage.](image)

For the question about $p_o$ in the case that the input data is large: although the input data of the model $p_b$ is also multiplied by a large number, causing a large memory usage, it is still relatively small than $p_o$.

C.4 Concluded Formula

Taking all 3 ingredients into consideration, we have the CUDA memory calculation Formula 24, as shown below.

$$M = p_m \cdot n + b \cdot p_o + p_b$$

(24)

$$p_m \cdot n = \sum_{i=0}^{n} p^i_o$$

(25)

Here $M$ is the CUDA memory usage, $p_m$ is the parameter of the model, $p_o$ is the sum of parameters of the output for each layer, $p_b$ is the size of the input data for the whole model, $b$ is the batch size, and $n$ is an integer usually between 2 and 6, which is subjective to the type of optimizers, like 2 for SGD and 4 for Adam. Note that the last item ($p_b$) can usually be ignored as discussed in Section C.3.
D REDUCING GPU MEMORY USAGE

In this appendix, we illustrated the practical ways to reduce memory usage and the reason for the unexpected OOM issues in our experiments, as illustrated in Section 4.2. In this part, we frequently refer to Formula 24 so it’s recommended to go through Appendix C first.

D.1 Change Data Length using Apex

The most efficient strategy, also the easiest one, is to shift the processed data to another type with a shorter length. For example, if the data is now floating-point-32, consider shifting it to floating-point-16 for all data, including the model and the input data. This approach decreases a bit of the precision, but it decreases the usage of the memory to approximately a half [20].

This can be proved by Formula 24. Because all the parameter sizes ($p_m, p_o, p_b$) are decreased by a factor of 2, the whole usage $M$ is also decreased by a factor of 2.

However, changing data types manually is time-consuming and bug-prone, and can also decrease the precision non-trivially. Thus, PyTorch developed a very powerful library utilizing NVIDIA Tensor Core called Apex. The Apex library takes floating-point-32 as original code but utilizes in-library optimizations to the data using a mixed distribution of floating-point-16 and floating-point-32 to decrease the usage of data to a factor of approximately 2. This strategy is proved to lose only a trivial precision when training and requires adding only a few lines into the original code with floating-point-32 data.

However, mixed-precision training using fp16 (half precision) is now only available for GPUs supporting NVIDIA Tensor Core. Fortunately, the HAL system is built using V100 GPUs based on the Volta architecture, which has the built-in Tensor Core, so it’s safe to use in our experiments.

The detailed code snippet for utilizing the Apex library can be found on the official website at https://github.com/NVIDIA/apex.

D.2 Minimize Batch Size

Minimizing batch size is another crucial method to reduce $M$. According to Formula 24, when $b$ is halved, the second item is halved. Thus, when the first item is small, this is very useful for reducing the memory usage. Note that reducing both development batch size and testing batch size can contribute to a smaller $M$ [21].

However, small batch size is very likely to exert a performance loss of the convergence of the loss curve. For example, in our GPT-2 training process, if the batch size becomes 1 or 2, the model will not be sufficiently fed for each step and thus create a tendency of divergence in the loss curve. We’ve done several experiments, with the results shown in Figure 16. The results show that a smaller batch size tends to make the loss curve not as smooth and prone to diverge. Even if we observe a normal loss curve, a small batch size may also lead to results that are not meaningful.

Thus, researchers should double-check the influence of reducing batch size in the model they’re investigating, as the conclusion varies from model to model.

D.3 Reduce Input Sequence Length

Reducing the input sequence length is another popular way to tackle the OOM issue. Note that this method is more likely to be used in a sequential model that is order-sensitive, such as data used in RNN models. In these kinds of training, the sequence length of the data is linear to $p_o$, thus a halved sequence length has the same effect as halved batch size $b$, leading to approximately the same memory saving as discussed in Section D.2.

D.4 Free Unnecessary Variables

Compared to other strategies, this strategy is more engineering-based and has nothing to do with Formula 24. If we represent the real memory usage as $M_r$, and the marginal cost by the code itself as $M_c$, we have $M_r = M + M_c$.

The marginal cost of unnecessary variables in research code is very common, as precise allocation and deallocation of data pointers in the Python code need a great command of the Python Language. A common problem is that few researchers notice to free the variables in each step and epoch. We take the code snippet below for an example.

```python
for epoch in range(epochs):
    for step in range(len_ // batch_size):
        batch = ..
        out = model.forward()
        loss, logits = out[:2]
        loss.backward()
        optimizer.step()
```

The problem with this code is the variables allocated are still in the memory after each step ends. Note that these variables are in the CUDA memory instead of CPU memory because it would take too long for data to be transferred back and forth between GPU and CPU. Thus, the allocated CUDA memory cannot be freed. After each step, the GPU program not only recalculates the variables and replaces the original one, but also caches the original value in case of future use, leading to a serious memory expansion.
To solve this problem, an examination of what variables are safe to be deleted should be conducted, and then the researcher should delete the structures and free the GPU cache. After that, it’s recommended to use `del` followed by the `empty_cache()` command. For example, the correct fix for the code above is adding these lines at the end of each step:

```python
# epoch:
# step:
    del out, loss, logits
torch.cuda.empty_cache()
```

The `empty_cache()` command explicitly tells the CUDA compiler (`nvcc`) to clear the cache in memory. This command cannot be used without deleting the variable, because the run-time program is not able to find what cache to clear - both lines should be inserted at the same time.

As shown in Figure 17a, this approach has a drawback: the loss-time curve loses non-trivial performance for multi-GPU training. From the comparison of the experimental results, we see that clearing the memory in multi-GPU training takes lots of time. This is because flushing the cache will force the program to call a cleaner handler each time.

Conclusively, it’s still recommended to use this strategy only for small models. For a more detailed explanation to multiple-GPU programming, you can refer to Section D.7 and Section D.8.

### D.6 Minimize Model

Minimizing the model is one of the most difficult strategies for reducing $M$. It’s hard to conduct because the model varies from one to another, leading to uncertainty [20]. In fact, this approach has even branched a subject itself, called model compression [5].

The basic strategies include changing two-level LSTM to one-level, replacing LSTM with GRU, reducing the number of convolution cores, and using as few Linear layers as possible [23].

### D.7 Multi-GPU Data Parallel

Data parallelization focuses on using multiple GPU workers to distribute the data to reduce $M$. If we represent the number of GPUs working together as $k$, the memory usage $M_i$ for each GPU worker $i$ now becomes the formula below.

$$M_i = p_m \cdot n + \frac{b \cdot p_o}{k} + \frac{p_b}{k}$$

As we see, for output-dense training (large $p_o$), this multi-GPU approach decreases $M$ by a factor of approximately $k$. However, also note that $\frac{b}{k}$ must be an integer larger than one. If the batch size is 4 for 1 GPU, and 8 GPUs are available, then at most 4 GPUs can be used to apportion batch size, and the left 4 will get no data.

Here is another guess of the OOM error observed in Section 4.2. In the experiment on DPS with each GPU apportioned batch size of 4, we found that the training process ran into an OOM error, but the benchmark with 1 GPU apportioned batch size of 4 did not.

According to Formula 26, together with the condition that we have the batch size on each GPU the same as the benchmark (4), the deducted memory usage on each GPU should be as described in Formula 27, which is exactly the same as Formula 24, indicating the same memory usage with the benchmark.

For those models with a relatively small $p_o$, the effect may be decreased but still worth a try.
\[ M_i = p_m \cdot n + \frac{b \cdot p_o}{4} \cdot 4 + \frac{p_b}{4} \cdot 4 \] 

(27)

Except for the reason that the AllReduce algorithm still requires a master GPU to communicate, we suspect that \( p_o \) (sum of output data for each layer) is not averagely distributed, as described in Formula 28. We also take consideration of the marginal memory cost due to the engineering issue discussed in Appendix D.4.

\[ M'_i = p_m \cdot n + \frac{b \cdot (p_o + \Delta p)}{4} \cdot 4 + \frac{p_b}{4} \cdot 4 + M_e \] 

(28)

In the formula, \( \Delta p_i \) is the sum of the difference of the output data for each layer in the model on each node, and \( M_e \) is the memory usage caused by engineering work like no memory deallocation and cache deletion (which was illustrated in Appendix D.4).

### D.8 Multi-GPU Model Parallel

The second type of multi-GPU strategy is the model parallel strategy. Different from the data-parallel strategy, it stores different parts of a model in different GPUs, with similar approaches like dispatching some data to the CPU for parallelization, as illustrated in Section D.5. It’s pretty important for the researcher to figure out which part of the model causes the OOM issue and then apportion that part to another GPU for storage and computation.