Interleaved Multistage Step-Up Topologies with Voltage Multiplier Cells

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Abstract: This paper proposes a family of high-voltage-gain step-up dc-dc converters for photovoltaic integration application. The proposed converters are capable of converting the low voltage from input sources to a dc bus. The proposed family is constructed of interleaved single-switch multistage boost converters and voltage multiplier cells (VMC). The proposed converters feature low voltage stress across the components, equal current sharing among all phases, and a smooth input current. Moreover, the proposed family of converters has a modular structure in both the VMC and the boost stage. That is, the VMC can have N number of cells, and the boost stage can have k number of stages. The k can be different in each phase, allowing the designers to integrate two independent renewable energy sources with different output voltages. An example converter was explained, analyzed, and simulated. An 80 W hardware prototype was implemented to confirm the converter’s operation and validate the analysis.

Keywords: DC-DC; interleaving; high-voltage-gain; multistage; PV; voltage multiplier cells

1. Introduction

The high-voltage-gain dc-dc step-up converters have become more prevalent in recent years due to the progress in power and energy fields and the development of technologies, such as smart grids, dc microgrids, and dc distribution systems [1–5]. The dc distribution system was found to be an upgrade alternative to the ac distribution system because of the reduced number of conversion units, the capability to protect against grounding faults, superior power quality, and cost-effectiveness. Besides, the dc distribution is desirable for renewable energy sources and battery incorporation to the grid [6–12]. However, most of the renewable energy sources have low output voltage, which needs to be boosted by about 15–25 times. The most common topology used for stepping up the voltage is the conventional boost converter, which has a simple structure and a low number of components. However, the conventional boost converter’s voltage gain can only be high at extreme duty cycles [13–15]. Operating at very high duty cycles increases the voltage stress across the components and requires a large inductance to make the converter draw a continuous input current. With consideration of the conduction and the switching loss, the voltage gain is significantly reduced. Such drawbacks sparked the research for a topology with a high-voltage-gain conversion ratio.

One way to increase the voltage gain is by cascading multiple conventional boost converters, where the output voltage is increased exponentially. Cascading two conventional boost converters allows both stages to operate at a low duty cycle [16–18]. Therefore, the voltage stress on the first stage
components is low. However, the stress on the second stage output diode still has to block the output voltage. The quadratic converter can be simplified by using only a single MOSFET. The output diode of such a converter suffers from high voltage stress, and the input current has high current ripples [19–21].

The voltage stress across components is reduced in the three-level boost converter, and the converter’s size is decreased due to the increase of the effective frequency across the inductor. The three-level boost has the same gain as the boost converter, which is not sufficient for renewable energy applications [22,23]. Switched capacitor circuits are capable of increasing the voltage gain by increasing the number of switching cells. Several advantages can be obtained: high power density, low EMI, the capability of being fabricated into integrated circuit chips. The drawbacks are the inherent losses, a high number of transistors that require isolation circuitry, and gate drivers. Moreover, the output voltage is fixed and cannot be regulated.

Several topologies utilize the transformer or a coupled inductors’ turns ratio to increase the voltage gain as in References [24–29]. Using the transformer can meet the requirement of isolation and safety and can provide multiple outputs. However, the power density is significantly reduced, and the weight of the converter is increased. Also, the stress on the MOSFETs caused by the parasitic leakage inductance can damage the switches unless an extra auxiliary circuit is implemented to recycle the energy. Similar to using a transformer, using an integrated coupled inductor improves the voltage gain without providing isolation, such as a hybrid flyback-boost, interleaved with coupled inductors, or quadratic boost converter with coupled inductors. Such topologies suffer from leakage inductance and require extra circuits for circulating the energy and reducing the voltage stress across the switches [30–33].

This paper introduces an interleaved single-switch multistage boost converter with voltage multiplier cells. The converter features low voltage stress on components and high voltage gain, allows the user to get the most ripple cancellation that interleaving offers, has the capability to integrate different voltage sources, and can match a wide range of loads. Each phase of the interleaved multistage can have either the same or a different number of boost stages than the other phases. This can be very useful for integrating sources with a significant difference in their output voltage. The voltage multiplier cells (VMC) stage uses a bi-fold Dickson that has a symmetrical structure and low voltage stress across the components. Incorporating two symmetrical phases with the same duty cycle yields equal current sharing between the phases and a very smooth input current.

The rest of this paper is structured as follows. First, the theory of operation and steady-state analysis of each mode is presented in Section 2. The components selection and design procedure are presented in Section 3, and the implementation of the hardware prototype and experimental results are explained in Section 4. Finally, conclusions and future work are presented in Section 5.

2. Theory of Operation and Steady-State Analysis

The general structure of the proposed converter is shown in Figure 1. The converter consists of two single-switched multistage boost converter cells. These cells are 180° out of phase, and they are independent of each other, which means each cell can have a different number of the boost stages, as shown in Figure 1b,d. Two independent voltage sources can feed the proposed converter instead of one, which is essential to interface multiple renewable energy sources. The single switch multistage boost converter allows the converter to achieve higher converter gain with no need to add extra MOSFETs and can come in different topologies, as shown in Figure 2. The second stage of the converter consists of voltage multiplier cells to increase the voltage and reduce the voltage stress across the diodes. Numerous VMCs can be used with this converter as in References [34–36]. Example converters of the proposed family are shown in Figure 3. In this paper, Bi-fold Dickson VMC is used for the proposed converter, which features lower stress across the diodes and capacitors. Therefore, the voltage gain can be increased in three ways: by increasing the number of VMC cells, by increasing the duty cycle, or by increasing the number of
boost stages. The Figure 4 shows the proposed converter with $k$ boost stages and $N$ number of VMC cells. The converter can replace all diodes with MOSFETs to improve efficiency in the case of very high power applications, as shown in Figure 5. The following analysis and experimentation are based on the converter with $k = 2$ and $N = 2$, as shown in Figure 6.

The analysis of the proposed converter was performed on several assumptions: (1) All components are ideal (2) All capacitors are large so that the voltage is constant (3) The duty cycles $d_1$ and $d_2$ are equal ($d_1 = d_2 = d$), and they are out of phase. (4) The converter operates in the steady-state. The switching pattern of the proposed converter can be seen in Figure 7. The converter has three modes of operations, and the sequence of the mode is that the mode 1 always comes between mode 2 and 3.

2.1. Mode 1: Both MOSFETs Are ON

In this mode, diodes $D_{a1}$ and $D_{a3}$ are forward-biased, and they are ON, which allows the voltage source to charge the inductors $L_1$ and $L_3$, respectively. Diodes $D_{a2}$ and $D_{a4}$ are reversed biased, and they are OFF. Inductors $L_2$ and $L_4$ are being charged by capacitors $C_{a1}$ and $C_{a2}$, respectively. All diodes in the VMC stage are reversed biased, and they are OFF. The load is separated from the source, and it is fed by capacitors $C_{2A}$ and $C_{2B}$. the equivalent circuit for this mode is illustrated in Figure 7a. The inductor voltages are given by

$$L_1 \frac{di_{L_1}}{dt} = V_{in} \quad (1)$$

$$L_2 \frac{di_{L_2}}{dt} = V_{C_{a1}} \quad (2)$$

$$L_3 \frac{di_{L_3}}{dt} = V_{in} \quad (3)$$

$$L_4 \frac{di_{L_4}}{dt} = V_{C_{a2}} \quad (4)$$

and the output voltage is given by

$$V_o = V_{C_{2A}} + V_{C_{2B}}. \quad (5)$$

2.2. Mode 2: $Q_1$ Is ON and $Q_2$ Is OFF

In this mode, inductor $L_1$ is still being charged by the input source, while $L_2$ is being charged by $C_{a1}$. Inductors $L_3$ and $L_4$ are discharging to the VMC stage. Diodes $D_{1A}$ and $D_{2B}$ are reversed biased, and diodes $D_{1B}$ and $D_{2A}$ are forward biased. The energy in capacitors $C_{1A}$ and $C_{2B}$ is being discharged, and capacitors $C_{1B}$ and $C_{2A}$ are being charged. The equivalent circuit of this mode is shown in Figure 7b. The state equations are given by

$$L_1 \frac{di_{L_1}}{dt} = V_{in} \quad (6)$$

$$L_2 \frac{di_{L_2}}{dt} = V_{C_{a1}} \quad (7)$$

$$L_3 \frac{di_{L_3}}{dt} = V_{in} - V_{C_{a2}} \quad (8)$$
\[ L_4 \frac{d i_{L_4}}{d t} = V_{C_a2} - V_{C_18} = V_{C_a2} + V_{C_{1A}} - V_{C_{2A}}. \] (9)

Figure 1. The general structure of the proposed converter (a) both phases have a multistage boost converter and fed by a single source (b) phases have different numbers of stages and are fed by a single source (c) both phases have the same number of cascaded boost stages, but they are fed by two independent sources (d) each phase has a different number of stages and two independent voltage sources feed them.

Figure 2. Multistage boost converters (a) Quadratic cell with a grounded capacitor, (b) Cubic cell with grounded capacitors, (c) Quadratic cell with a floating capacitor, and (d) Cubic cell with floating capacitors.
Figure 3. Different variations of the proposed converter (a) Schematic of the proposed converter with 3 stages (cubic) and no voltage multiplier cell (VMC), (b) another interleaved cubic boost converter with one stage of cross capacitor VMC, and (c) interleaved cubic boost converter with one Cockcroft-Walton cell.
2.3. Mode 3: $Q_1$ is OFF and $Q_2$ is ON

In this mode, $L_1$ and $L_2$ are being discharged to the VMC stage. Diodes $D_{1B}$ and $D_{2A}$ are reversed biased. Diodes $D_{1A}$ and $D_{2B}$ are also reversed biased, and they are OFF. Opposite from mode 2, capacitors $C_{1B}$ and $C_{2A}$ are being discharged, while $C_{1A}$ and $C_{2B}$ are being charged. The equivalent circuit to this mode is shown in Figure 7c. The voltage across the inductors is given by

$$L_1 \frac{di_{i1}}{dt} = V_{in} - V_{C_{a1}}$$

(10)

$$L_2 \frac{di_{i2}}{dt} = V_{C_{a1}} - V_{C_{1A}} = V_{C_{a1}} + V_{C_{1B}} - V_{C_{2B}}$$

(11)

$$L_3 \frac{di_{i3}}{dt} = V_{in}$$

(12)

$$L_4 \frac{di_{i4}}{dt} = V_{C_{a2}}.$$  

(13)

![Schematic of the proposed converter with $k$ boost stages and $N$ voltage mutliplier cells.](image)

**Figure 4.** Schematic of the proposed converter with $k$ boost stages and $N$ voltage mutliplier cells. The voltage gain is $\frac{2N}{(1-d)^2}$.

2.4. Steady-State Analysis and Static Voltage Gain

By applying voltage-second balance to the inductors (using Equations (1)–(4) and (6)–(13)), the voltage across the capacitors and the output voltage, as well as the voltage gain of the converter, can be obtained. The average voltage of the inductors is given by

$$\begin{align*}
< v_{L_1} >& = d(V_{in}) + (1 - d)(V_{in} - V_{C_{a1}}) = 0 \\
< v_{L_2} >& = d(V_{C_{a1}}) + (1 - d)(V_{C_{a1}} - V_{C_{1A}}) = 0 \\
< v_{L_3} >& = d(V_{in}) + (1 - d)(V_{in} - V_{C_{a2}}) = 0 \\
< v_{L_4} >& = d(V_{C_{a2}}) + (1 - d)(V_{C_{a2}} - V_{C_{1B}}) = 0
\end{align*}$$

(14)

By solving Equation (14), the voltages of the first stage capacitors can be found, which are given by

$$V_{C_{a1}} = V_{C_{a1}} = \frac{V_{in}}{1 - d}.$$  

(15)
Similarly, the voltage across capacitors $C_{1A}$ and $C_{1B}$ is similar to the output capacitor voltage in the quadratic boost converter, which are calculated by

$$V_{C_{1A}} = V_{C_{1B}} = \frac{V_{in}}{(1-d)^2}. \quad (16)$$

The voltage across capacitors $C_{2A}$ and $C_{2B}$ is twice the voltage across capacitors $C_{1A}$ and $C_{1B}$, which is calculated by

$$V_{C_{2A}} = V_{C_{2B}} = \frac{2V_{in}}{(1-d)^2} \quad (17)$$

and the output voltage is calculated by

$$V_o = \frac{4V_{in}}{(1-d)^2}. \quad (18)$$

The voltage gain ($M$) of the proposed converter with 2 boost stages and 2 VMC cells is

$$M = \frac{4}{(1-d)^2} \quad (19)$$

The proposed converter can have more boost stages and VMC cells, as shown in Figure 4. The voltage gain of the proposed converter with $k$ boost converter stages and $N$ VMC cells is given by

$$M = \frac{2N}{(1-d)^k} \quad (20)$$

Figure 5. Schematic of the proposed converter with 3 stages (cubic) and 3 voltage multiplier cells (tripler) and implemented using MOSFETs instead of diodes to reduce the conduction loss.
Figure 6. Schematic of the proposed converter with $k = 2$ and $N = 2$.

Figure 8 shows the voltage gain versus the duty cycles at different numbers of voltage multiplier cells and boost stages. The converter can be fed by two independent voltage sources, and each phase can operate at a different duty cycle. Table 1 shows the output voltage for these cases.

Table 1. Output voltage at different cases when the number of stages are even.

| Case                        | The Output Voltage                                                                 |
|-----------------------------|-----------------------------------------------------------------------------------|
| $d_1 \neq d_2$ and $V_{in1} \neq V_{in2}$ | $N \frac{1}{(1-d_1)^2} V_{in1} + N \frac{1}{(1-d_2)^2} V_{in2}$                |
| $d_1 \neq d_2$ and $V_{in1} = V_{in2}$    | $N V_{in} \left( \frac{1}{(1-d_1)^2} + \frac{1}{(1-d_2)^2} \right)$             |
| $d_1 = d_2$ and $V_{in1} \neq V_{in2}$    | $N \frac{1}{(1-d_1)^2} (V_{in1} + V_{in2})$                                     |
| $d_1 = d_2$ and $V_{in1} = V_{in2}$       | $2N \frac{1}{(1-d_1)^2} V_{in}$                                                  |

The proposed converter is compared to other topologies in terms of the voltage gain and number of components, as shown in Table 2.

Table 2. Comparison between different topologies.

| Topology                                      | Quadratic Cascaded Boost Converter [37] | Cascaded Three-Level Boost Converter (Two Stages) [38] | Interleaved Boost with the Dickson VMC with $N = 5$ [39] | Interleaved Quadratic Boost Converter [39] | Proposed Converter with $N = 2, k = 2$ |
|----------------------------------------------|-----------------------------------------|-------------------------------------------------------|--------------------------------------------------------|----------------------------------------|---------------------------------------|
| Static voltage gain                          | $\frac{1}{(1-d)^2}$                     | $\frac{1}{(1-d)^2}$                                   | $\frac{1}{(1-d)^2}$                                   | $\frac{1}{(1-d)^2}$                   | $\frac{1}{(1-d)^2}$                   |
| Maximum stress on switches or diodes         | $V_o$                                   | $\frac{V_o}{2}$                                      | $\frac{V_o}{2}$                                      | $V_o$                                 | $\frac{V_o}{2}$                       |
| Maximum voltage on capacitors                | $V_o$                                   | $\frac{V_o}{2}$                                      | $V_o$                                                 | $V_o$                                 | $\frac{V_o}{2}$                       |
| Number of capacitors                         | 2                                      | 4                                                     | 6                                                     | 3                                      | 6                                     |
| Number of diodes                             | 2                                      | 4                                                     | 6                                                     | 6                                      | 8                                     |
| Number of inductors                          | 1                                      | 2                                                     | 2                                                     | 4                                      | 4                                     |
| Number of floating MOSFETs                   | –                                      | 2                                                     | –                                                     | –                                      | –                                     |
| Number of grounded MOSFETs                   | 2                                      | 2                                                     | 2                                                     | 2                                      | 2                                     |
Figure 7. Equivalent circuits to (a) mode 1: both MOSFETs are ON, (b) mode 2: Q₁ is ON and Q₂ is OFF, and (c) mode 3: Q₁ is OFF and Q₂ is ON.
3. Components Selection and Efficiency Analysis

3.1. Active Switches

The voltage stress across the MOSFETs are given by

\[ V_{Q_1} = V_{Q_2} = V_{in} \frac{1}{(1-d)^2} = \frac{V_o}{2N} \]  

(21)

and the maximum current passing through the MOSFETs is given by

\[ I_{Q_1, pk} = \frac{NV_o}{R} \frac{3 - 2d}{(1-d)^2} - \frac{V_{in}}{2f_s} \left( \frac{1-d}{L_1} + \frac{1}{L_2} - \frac{d}{(1-d)L_4} \right) \]  

(22)

\[ I_{Q_2, pk} = \frac{NV_o}{R} \frac{3 - 2d}{(1-d)^2} - \frac{V_{in}}{2f_s} \left( \frac{1-d}{L_3} + \frac{1}{L_4} - \frac{d}{(1-d)L_2} \right) \]  

(23)

where \( f_s \) is the switching frequency. The rms currents can be approximated by

\[ I_{Q_1, rms} = I_{Q_2, rms} = \frac{NV_o}{R} \sqrt{\frac{4}{(1-d)^2} + \frac{1}{(1-d)^4}}. \]  

(24)

3.2. Diodes

The maximum voltage stress across the diodes is given by

\[ V_{D_{a1}} = V_{D_{a3}} = V_{in} \frac{d}{(1-d)^2} \]  

(25)

\[ V_{D_{a2}} = V_{D_{a4}} = V_{in} \frac{1}{1-d} \]  

(26)

\[ V_{D_{1A}} = V_{D_{2A}} = V_{D_{1B}} = V_{D_{2B}} = 2V_{in} \frac{1}{(1-d)^2}. \]  

(27)

The average current and the RMS current passing through the diodes are shown in Table 3.
Table 3. Diode average and RMS currents.

| Current          | Average | RMS     |
|------------------|---------|---------|
| $I_{D_{all}}$    | $\frac{V_o}{R}$ | $\frac{V_o}{R} \sqrt{1 - d}$ |
| $I_{D_{a}}$, $I_{D_{b}}$, $I_{D_{2a}}$, $I_{D_{2b}}$ | $\frac{dN}{(1-d)^2}$ | $\frac{V_o N}{(1-d)^2} \sqrt{d}$ |
| $I_{D_{3}}$, $I_{D_{4}}$ | $\frac{V_o (N)}{(1-d)}$ | $\frac{V_o N}{(1-d)^2} \sqrt{1 - d}$ |

3.3. Inductors

Inductor selection is based on the required inductance to keep the converter operating safely in the continuous conduction mode (CCM). The input current is given by

$$I_{in} = \frac{V_o}{R} \frac{2N}{(1 - d)^2}$$  \hspace{1cm} (28)

The average current passing through inductors $L_1$ and $L_3$ is given by

$$I_{L_1} = I_{L_3} = \frac{V_o}{R} \frac{N}{(1 - d)^2}$$  \hspace{1cm} (29)

and the average current passing through inductors $L_2$ and $L_4$ is given by

$$I_{L_2} = I_{L_4} = \frac{V_o}{R} \frac{N}{1 - d}.$$  \hspace{1cm} (30)

The operation of the proposed converter in the CCM requires minimum inductance. The minimum inductance for $L_1$–$L_4$ can be calculated using

$$L_{1,\text{crit}} = L_{3,\text{crit}} = \frac{V_{in} d (1 - d)^2}{2 N I_o f_s}$$  \hspace{1cm} (31)

$$L_{2,\text{crit}} = L_{4,\text{crit}} = \frac{V_{in} d (1 - d)}{2 N I_o f_s}.$$  \hspace{1cm} (32)

The peak and rms currents of all inductors are listed in Table 4.

Table 4. Inductor peak and RMS currents.

| Current          | Peak                  | RMS                  |
|------------------|-----------------------|----------------------|
| $I_{L_1}$        | $\frac{V_o}{R} \frac{N}{(1-d)^2} + \frac{V_{in} d}{2 I_o f_s}$ | $\sqrt{\left( \frac{V_o}{R} \frac{N}{(1-d)^2} \right)^2 + \left( \frac{V_{in} d}{2 \sqrt{3} I_o f_s} \right)^2}$ |
| $I_{L_2}$        | $\frac{V_o}{R} \frac{N}{1 - d} + \frac{V_{in} d}{2(1-d)L_2 f_s}$ | $\sqrt{\left( \frac{V_o}{R} \frac{N}{(1-d)^2} \right)^2 + \left( \frac{V_{in} d}{2 \sqrt{3} L_2 f_s} \right)^2}$ |
| $I_{L_3}$        | $\frac{V_o}{R} \frac{N}{(1-d)^2} + \frac{V_{in} d}{2 I_o f_s}$ | $\sqrt{\left( \frac{V_o}{R} \frac{N}{(1-d)^2} \right)^2 + \left( \frac{V_{in} d}{2 \sqrt{3} I_o f_s} \right)^2}$ |
| $I_{L_4}$        | $\frac{V_o}{R} \frac{N}{1 - d} + \frac{V_{in} d}{2(1-d)L_4 f_s}$ | $\sqrt{\left( \frac{V_o}{R} \frac{N}{(1-d)^2} \right)^2 + \left( \frac{V_{in} d}{2 \sqrt{3} L_4 f_s} \right)^2}$ |
3.4. Capacitors

The voltage across the capacitors is already calculated in. The capacitor values are chosen based on the allowed voltage ripples $\Delta V_C$ of the capacitor voltage. The output capacitance is calculated by

$$C = \frac{V_o (1 - d)}{R f_s \Delta V_C}. \quad (33)$$

The RMS current of the output, and the first stage capacitors are given, respectively, by

$$I_{C2,\text{rms}} = I_{C2B,\text{rms}} = I_o \sqrt{\frac{d}{1 - d}} \quad (34)$$

$$I_{C1,\text{rms}} = I_{C1B,\text{rms}} = I_o \left(1 + \sqrt{\frac{d}{1 - d}}\right). \quad (35)$$

3.5. Efficiency Analysis

The efficiency of the proposed converter is mainly affected by the diodes, inductors and MOSFETs. Table 5 lists all the equations used for calculating the losses of the converter. The simulated efficiency is compared to the experimental in Section 4.

| Components | Equation | Variables |
|------------|----------|-----------|
| Inductors  | $I_{\text{rms}}^2 \times R_L$ | $R_L$ is the dc resistance of the inductor |
| Inductors  | $a(\Delta B)^b f_s^c$ | $a, b, c$ obtained using curve fitting from material datasheet |
| MOSFETs   | $I_{\text{rms}}^2 C_{\text{oss}} \times V_S^2$ | $C_{\text{oss}}$ is mosfet output capacitor |
| MOSFETs   | $f_s \times \frac{N V_S}{R (1 - d)^2} \times (t_{\text{OFF}} + t_{\text{ON}})$ | $f_s$ is switching frequency $T_{\text{ON}}$ and $T_{\text{OFF}}$ are the ON and OFF time of the MOSFET |
| Diode     | $I_{\text{D}}^2 \times V_f$ | $V_f$ is the forward voltage of the diode |
| Capacitor | $I_{\text{rms}}^2 \times ESR$ | $ESR$ is the equivalent series resistance of the capacitor |

4. Experimental Implementation and Results

An 80 W hardware prototype was implemented and tested in the laboratory to verify the operation and the analysis of the converter. Figure 9 shows the hardware prototype, which was implemented using the components listed in Table 6. The N5700 was used to supply power at 10 V to the prototype, and the output load was implemented using a mix of ceramic resistors. The duty cycle was set to be around 0.6, and that made the output equal to 250 V. The measurements and waveforms were taken at 80 V. Figure 10 shows the voltage waveforms across the switches. The MOSFETs have maximum voltage stress of 62 V. The maximum voltage stress across the diodes in the interleaved single-switch multistage is about 38 V for $D_a$ and $D_3$ and about 63 V for $D_2$ and $D_4$. The maximum voltage stress across the VMC diodes is 125 V. The voltage across the capacitors, depicted in Figure 11, is 25 V for $C_1$ and $C_2$, 63 V for $C_{1A}$ and $C_{1B}$ and 125 V for $C_{2A}$ and $C_{2B}$. The output voltage is about 250 V with ac components of less than 2%.
Other waveforms, such as the current of the switches and passive components, are shown in Figure 12 and Figure 13. The converter’s efficiency was simulated and experimentally measured, as shown in Figure 14. The experimental efficiency differs from simulation efficiency by a maximum of 1.5%. The difference is normal, and it is due to many factors, such as instrument errors and parasitic and conduction losses in the wires and the PCB. The efficiency is about 94% for a load ranges from 20–60 W. The increase of the drawn current from the input source increases the conduction loss of the switching elements and decreases the overall efficiency by 1% at the full load. As mentioned before, the efficiency can be further increased by selecting efficient diodes with low forward voltage for the interleaved boost stage or by replacing the diodes with efficient ones or MOSFETs.

Figure 9. Hardware prototype.

Figure 10. Voltage waveforms of the MOSFETs and the diodes.
Table 6. Component Listing for the Hardware Prototype.

| Item    | Designation | Rating               | Part No.   |
|---------|-------------|----------------------|------------|
| Inductor| L₁–L₄       | 100 µH, DCR = 25 mΩ, | 60B104C    |
|         |             |                      |            |
| Capacitor| C₁₂A, C₂₂A | 10 µF                | EXH2E106HRPT |
| Capacitor| C₁₂₁, C₁₂₂ | 10 µF                | B32674D3106K |
| MOSFET  | Q₁, Q₂      | 150 V, 37 A, R_{ds(on)} = 10.525 mΩ | IPA105N15N3 |
| Diode   | D₁₂A, D₂₂A  | 250 V, 40 A, V_{F} = 0.86 V, t_{rr} = 35 ns | MBR40250G   |
|         | D₁₂₁, D₂₂₂  |                      |            |

Figure 11. Voltage waveforms of the capacitors, the output load and the ac components of the output voltage.

Figure 12. Current passing through the MOSFETs, inductors and diodes D₁A–D₆A.
5. Conclusions

This paper presents a non-isolated interleaved multistage boost converter with VMC. The converter has high voltage and low voltage stresses across the components. Converting a 10 V to a 250 V can be achieved by the quadratic boost stage and a 2-cell VMC when operating at a 0.6 duty ratio. The converter is capable of converting power from a single source or two independent sources. The input is shared among the two phases equally, and since the converter operates at 0.6, the current ripple cancellation is higher than the other interleaved boost converters. The analysis of this converter was explained and validated by simulation and experimental prototype. The converter is very suitable for integrating PV panels to higher-voltage DC buses.

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Abbreviations
The following abbreviations are used in this manuscript:

- VMC: Voltage multiplier cells
- RMS: Directory of open access journals
- PCB: Printed circuit board
- DC: Direct current
- CCM: Continuous conduction mode

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