1. Introduction

Packaging technologies have been steadily evolving since the early 2000s together with semiconductor technologies according to Moore’s law. However, such technology trends have gradually been changing in the last decade. For example, the operating frequency of microprocessors, and the capacity of dynamic random-access memories (DRAMs) have become saturated against that predicted by Moore’s law. This change suggests the actual requirements of the electronics market have not been seen as a continuation of simple miniaturization.[1] Therefore, packaging technologies have become increasingly important to improve system performance. Therefore, we focused on a novel heterogeneous packaging technology as a means to achieve the diverse functionalities. The target of our study was the interconnection between logic and memory. This is a core technology to achieve high performance and there are continuous demands for it even now. For example, the display resolution of current mobile terminals is quad full high definition (QFHD: 3840 × 2160) even though it was mainly quarter video graphics array (QVGA: 320 × 240) a decade ago. Large and high-speed data communication with a data transfer rate of approximately 20 Gbps is required to display such high-resolution content. This means that a high-performance logic processor, large capacity memories, and wide-bus logic-memory interconnections are required, even in mobile appliances. The Joint Electron Device Engineering Council (JEDEC) has managed to provide two standards for next generation mobile memories to address this rapid change in the market.
The first is the Wide I/O DRAM published in 2011,[2] and the second is the Low Power Double Data Rate 3 synchronous dynamic random access memory (SDRAM) (LPDDR3) published in 2012.[3] These standards accomplish similar electrical performance. The main difference from the viewpoint of packaging technology is in the stacking structure of logic and memory chips. Wide I/O supports chip stacking with Through-Si-Vias (TSVs), while LPDDR3 as well as LPDDR2 support the PoP structure. Consequently, the total package height of Wide I/O is shorter than that of LPDDR3 because of the micro-bumps used in die stacking.

Even though the application of TSVs to interconnections between stacked chips is a promising solution, it will take time to be extensively implemented in practical use. The PoP structure has been used in mobile products in contrast to TSV technologies, and it has been thought to be more practical to expand PoP technologies for use in next generation mobile appliances.

A typical PoP structure is composed of a memory chip package at the top, and a logic chip package at the bottom, as seen in Fig. 1(a). Because the gap between the top and bottom packages has to be larger than the logic chip height, the total height of the PoP structure is generally higher than 1.5 mm and the interconnect pin count is limited.[4] Embedding the logic chip into the bottom package substrate, as shown in Fig. 1(b), effectively[5] solves these issues. PoP structures with embedded-LSI packages can lead to progress with further miniaturization, as shown in Figs. 1(c) and 1(d). However, the logic chip usually has to be customized to embed organic substrates from the electrical design constraint point of view. This results in cost increases and a long turnaround time in fabrication. This paper describes a methodology of electrical design to embed an existing logic chip into the bottom package of a PoP structure and reports a demonstration of the electrical performance of PoP structures based on the proposed design concepts.

2. Fabricated PoP Structure

A commercial LSI was employed to confirm the design methodology we developed. The package substrate for the embedded-LSI package was also redesigned by using LSI. Figure 2 is photographs of the developed embedded-LSI package. The conventional non-embedded-type package was also fabricated as a reference.

Table 1 summarizes the specifications for the developed and reference packages. The logic LSI was 7.5 mm square and had approximately 400 pads that were peripherally configured. The package was 13 mm square. The developed package employed a core-less substrate, which consisted of seven metal layers including the two reinforced layers and an alignment layer shown in Fig. 3 and Table 4. The metal layer count for routing signals is the same as the reference package. In addition to the reinforced layers, the combination of resin was optimized to decrease warp-
age. The vias formed in the resin layer including the embedded-LSI are called Silicon Side Vias (SSVs) in this paper. Table 2 lists the ball grid array (BGA) pad count assigned to the power supply and ground on the main-board side of the bottom package substrate.

Though RDL and additional metal layers with SSVs cause a cost escalation as compared to the conventional non-embedded-type package, it is thought that utilizing existing LSI and eliminating Au bonding wires limit the cost increases.

### Table 1 Specifications of developed and reference packages.

| Logic LSI | Developed package | Reference package |
|-----------|-------------------|-------------------|
| Size      | 7.5 mm sq.        | ←                 |
| Pad count | Approx. 400       | ←                 |
| Pad pitch | 350 μm grid-array | 70 μm peripheral  |
| Highest signal clock | 312 MHz | ←                 |

| Memory | Bus clock | 266 MHz LPDDR | ← |
|        | Capacity  | 32 MB        | ← |

| Substrate | Size     | 13 mm sq. ← |
|           | Pad count at top | Approx. 140 ← |
|           | Pad count at bottom | Approx. 470 ← |
|           | Metal layer count | 7 4 |

![Fig. 3 Cross-sectional structure of developed package.](image)

3. Chip-Package Co-Design

The LSI chip was originally designed to be mounted face up on the bottom package substrate to enable wire bonding, as outlined in Fig. 1(a). When this chip was embedded into the bottom package substrate, the traces connected between both sides of the substrate were interrupted by the embedded chip. Therefore, a “Chip-Package Co-Design” was crucial to designing the embedded LSI package. We found the following design concepts made the package design flexible:

The first was the grid-type layout to arrange the SSVs. The embedded LSI was an obstacle for the traces connecting both sides of the package substrate. This was a disadvantage compared to TSV-type chip stacking.

Because the grid-type arrangement is the same as that for the fine-pitch solder interconnections on the common bottom package of the PoP structure, package designers can easily design traces. The approximate SSV count was obtained as

$$n = \frac{S}{g},$$  \hspace{1cm} (1)

where \(n\) is the SSV count, \(g\) is the pad pitch, and \(S\) is the maximum space shown in Fig. 4. The practical SSV count was almost the same for both grid and staggered SSV layouts. The pitch of the SSVs was 500 μm and their diameter was 320 μm by taking production yield into consideration.

As a result, there were approximately 440 SSVs for a 13 mm square package, as shown in Fig. 5.

All traces connected with the bottom BGA pads passed through the SSVs on their way to the logic chip pads in routing the wires. The number of SSVs, therefore, needed

![Fig. 4 SSV layout area and layout patterns. Hatched area means SSV formable area: S.](image)

### Table 2 BGA pad count for each function at mainboard side of bottom package substrate.

| Function | Voltage [V] | Pad count | Used in |
|----------|-------------|-----------|---------|
| Power 1  | 1.85        | Approx. 30 | Logic   |
| Power 2  | 1.2         | Approx. 20 | Logic   |
| Power 3  | 1.85        | Approx. 20 | Memory  |
| Power 4  | 1.85        | Approx. 10 | Memory  |
| Ground   | 0           | Approx. 85 | Logic and memory |
| Signal   | –           | Approx. 355| Logic and memory |
be about the same as that of the BGA pads. In this case, the number of SSVs of approximately 440 is almost comparable to the number of BGA pads of approximately 470, as listed in Table 1. This was because some traces for the power supply and ground had multiple pads to reduce power distribution network impedance and current density. Since the SSVs were large and thick, they could be substituted for multiple normal vias, particularly in terms of reducing current density. The developed package was not suitable when there were far fewer SSVs than the signal pads of BGA pads.

The second most important task was re-arranging the embedded LSI pad layout with RDL. The chips for normal PoP structures are usually designed to be connected to the substrate by wire bonding or flip-chip bonding. Thus, the pad layout of the chip is not always suitable for embedded LSI packages. The LSI used in this work had a peripheral layout with a 70-μm pitch. Actually, that used in the previous work had a staggered layout with a 160-μm-pitch. This pitch is too fine for embedding an LSI into the package substrate by using printed-wiring-board-based technology. The pad layout was configured in a 20 × 20 area array with a 350-μm-pitch by using RDL with a line/space (L/S) value of 5 μm/5 μm. This L/S value was capable of treating the LSI used in this work. Two RDL layers were formed on the embedded LSI, as shown in Fig. 6.

The routing traces in the package could be categorized into three groups prior to designing the pad re-arrangement and RDL, as shown in Fig. 7 and Table 3:

- Group A: Mainboard-logic-memory
- Group B: Mainboard-logic
- Group C: Mainboard-memory

The designed package had design constraints considering its metal layer count, as listed in Table 4. The third metal layer was used to align the embedded LSI and the package substrate. The fourth and fifth metal layers were used to stiffen the package substrate as the power supply and ground plane. We had to optimize the “signal-centered” pad layout on RDL to complete the layout for approximately 400 traces with only two metal layers that were 7.5 mm square, as described below.

When the L/S on the second RDL layer was 20 μm/20 μm, four traces were formed between the pads. As a result, five rows on the periphery of the chip could be fanned out on the same metal layer, as shown in Fig. 8. Peripheral pads are conventionally assigned as signals in such flip-
chip packages because the total number of vias on a trace should be as small as possible, from the point of signal integrity (SI). Although the pad count of five rows on the periphery of the chip was 256, approximately 335 signals were necessary, as listed in Table 2. Therefore, some of the signal traces had to be assigned to the center portion of the chip. The total number of vias for each signal trace increased by one for Group-A and by two for Group-B for the signal traces assigned to the center portion of the chip, as seen in Fig. 9. We decided to assign Group-A to the center portion of the chip and Group-B to the five rows on the periphery to reduce the total number of vias for Groups-A and -B. This signal-centered layout also had the following advantage: When the package substrate needs to be miniaturized to the same size as the LSI chip, package designers generally need to thoroughly re-arrange it because the wiring layout is optimized for the original size. However, they can make the most of some of the wiring layouts located in the center portion of the chip without making substantial modifications in this signal-centered case. A comparison of the wiring layouts for the two package sizes in Fig. 10 (a) and (b) for 13 mm square packages are actually similar to (c) and (d) for 10 mm square packages, explained in detail below, particularly on the embedded LSI illustrated dashed frame in the Figures.

The resulting designed patterns for each layer are shown in Fig. 10 and Fig. 11. Figure 10 shows the patterns for each metal layer on the coreless substrate. A 10 mm square package was also designed to confirm that the proposed design methodology was suitable to miniaturize packages. In the 10 mm square package, L/S was 10 μm/10 μm and the pitch of the SSVs was approximately 320 μm and their diameter was 80 μm. The traces highlighted in red refer to the power supply and those in blue refer to the ground. The designed packages have a larger power/ground area than the reference, which is expected to be an advantage in reducing power distribution network (PDN) impedance despite the decreasing number of SSVs assigned to the power supply and ground. The first metal layer is the connection layer to the upper package substrate. Some of the signal traces of Group-A fan out from the center portion of the chip. The second layer is the connection layer to the embedded LSI. The third layer through to the fifth layer are reinforced layers. The sixth layer is the routing layer. The seventh layer is the connection layer to the mainboard. Figure 11 shows the patterns for each RDL layer on the embedded LSI. The fine patterns with the L/S value of 5 μm/5 μm enable the pad lay-
4. Evaluation of Electrical Performance

We evaluated electrical characteristics by calculating insertion loss for signal integrity (SI) and PDN impedance for power integrity (PI) to estimate practical operation by 2.5D electromagnetic simulation. The fabricated PoP structures were also tested. 

Fig. 10 Routing patterns of each metal layer of coreless substrate. Areas highlighted in red indicate power and those in blue indicate ground. Dashed flames indicate the embedded LSI.

(a) First metal layer for 13 mm sq. package.  (b) Second metal layer for 13 mm sq. package.

(c) First metal layer for 10 mm sq. package.  (d) The second metal layer for 10 mm sq. package.

Fig. 11 RDL layers of embedded LSI. Areas highlighted in red indicate power and those in blue indicate ground.

(a) First RDL layer.  (b) Second RDL layer.

(a) Signal Integrity (SI) Characteristics

Signal integrity was evaluated by using the insertion loss ($S_{21}$) of some of the higher data rate signal traces. Figure 12 outlines the set-up to calculate Groups-A and -B. Port-1 is on the LSI side for both groups, and Port-2 is on the upper package side for Group-A and on the mainboard side for Group-B.

Figure 13 plots the simulated insertion loss for develop-
oped and reference packages. The insertion loss does not depend on the package structure and are within ~3 dB up to approximately 2 GHz for all signals. The insertion loss is thought not to cause malfunction such as bit errors because the memory base clock frequency and the highest signal clock frequency of the logic LSI were 133 MHz and 312 MHz, respectively. The results suggest that the signal integrity of the designed embedded-LSI package is similar to the reference package.

(b) Power Integrity (PI) Characteristics

The LSI and memory used in this study mainly had the four kinds of power supply listed in Table 2. PDN impedance values of the developed and reference packages were simulated and compared for all power supplies as brief evaluation. PDN impedance from the LSI side and the upper package side were calculated by the same simulator as SI. Figure 14 outlines the port configuration used for calculating PDN impedance, and Fig. 15 presents the results obtained from calculating impedance for all powers. The computed impedance values of the developed embedded-LSI packages are almost the same as that of the reference package up to approximately 2 GHz, which is higher frequency than the fifth-order harmonics of the highest speed in the package, 312 MHz. Though practical PDN impedance have to be designed with decoupling capacitors and their configuration, the results suggest that
the developed embedded-LSI package can be successfully designed to have the same impedance as the reference package.

(c) Measurement Results

These simulation results suggest that the PoP structure with the embedded-LSI packages had been correctly designed. We then examined the operation and electrical performance of the fabricated PoP structures with the embedded LSI package by using an LSI tester. The developed PoP structures passed all the functional tests. The results of the tests can be graphed as a Shmoo plot. The Shmoo plot consists of two relevant parameters such as operating frequency and voltage of an LSI chip, and helps us understand visually how much margin the LSI has.[10]

Figures 16(a) and 16(b) are the examples of the obtained Shmoo plots. Figure 16(a) is a comparison of the operating voltage for the memory controller between ten developed packages and a reference package. The typical operating voltage is 1.8 ± 0.1 V. All tested samples passed the test at higher voltage than 1.5 V. The measured Shmoo plot reveals that the operating voltage margin of the developed package is equivalent to that of the reference package.

Figure 16(b) shows margin of the operating voltage and frequency of an RF function for a developed package. The typical operating voltage and frequency are 1.2 ± 0.1 V and 63 MHz, respectively. The operating frequency at the test was lower than the practical operation frequency because the test is not performed at speed. As can be seen from Fig. 16(b), the measured Shmoo plot also reveal sufficient operating margin. The SI and PI characteristics of the 10 mm square embedded-LSI package are comparable to those of the examined 13 mm square package. The design methodology will contribute to the miniaturization trend as
shown in Fig. 1.

Considering application to next generation mobile products working in a GHz range, further study will be necessary to optimize high-speed signaling because the low operating frequency of the logic and memory chips used in this study did not require wiring design with special care for GHz operation. One of the advantages of the developed package structure for high frequency operation is the two reinforcement metal layers, which can be used as power and ground planes for improving crosstalk, undesired radiation, and current density.[6, 11]

We confirmed from these results that the design methodology we developed was valid and practical. This methodology can easily be applied to such embedded-LSI packages, and is suitable for miniaturizing package sizes. Consequently, this would help package designers create low-cost, competitive, and unique PoP structures that meet various customer needs.

5. Conclusions

We developed a chip-package co-design methodology for an embedded-LSI package as the bottom package of a PoP structure with an existing LSI chip to achieve a practical thin and high-performance PoP. The embedded-LSI package we developed was 370-μm thick, which was 60% thickness of the 630-μm-thick reference package with a molded LSI. The fabricated PoP structure with the embedded-LSI bottom package designed with the proposed methodology worked effectively, and its electrical performance was equivalent to that of conventional PoP structures. The methodology we developed provided PoP structural design with flexible interconnections between the logic chip and memories. This means that packaging technologies can play a more important role in device performance because logic-memory interconnections represent a core component in electronic systems. This design flexibility meets diverse functionalities for small, inexpensive, and dependable packages ranging from consumer use to social infrastructure use.

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