A low-power fast-lock DCC with a digital duty-cycle adjuster for LPDDR3 and LPDDR4 DRAMs

Jongsun Kim\textsuperscript{a)} and SW Han

Electronic and Electrical Engineering, Hongik University,
94 Wausan-ro, Mapo-gu, Seoul 121–791, Korea
\textsuperscript{a)} js.kim@hongik.ac.kr

Abstract: A new low-power, fast-lock duty-cycle corrector (DCC) circuit with a digital duty-cycle adjuster (DCA) for mobile LPDDR3/LPDDR4 DRAMs is presented. The proposed DCC utilizes a digital feedback delay element (DFDE) to achieve wide duty-cycle correction and operating frequency ranges with low power consumption and fast lock capability. To obtain fast locking time and high duty-cycle correction accuracy, a 6-bit successive approximation register (SAR) controller utilizing a hybrid search algorithm is adopted. The measured duty-cycle error is less than ±0.85% over a 30–70% input duty-cycle range at 0.2–1.5 GHz. The DCC, which is fabricated in a 0.13-µm CMOS process, dissipates only 1.9 mW at 1 GHz and occupies an area of 0.036 mm².

Keywords: duty-cycle corrector, LPDDR3, LPDDR4, SDRAM, memory, DRAM

Classification: Integrated circuits

References

[1] Low power double data rate 3 SDRAM (LPDDR3): JESD209-3C (2015)
https://www.jedec.org/standards-documents/docs/jesd209-3c.
[2] Low power double data rate 4 SDRAM (LPDDR4): JESD209-4B (2017)
https://www.jedec.org/standards-documents/docs/jesd209-4b.
[3] C. Portmann, et al.: “A multiple vendor 2.5-V DLL for 1.6-GB/s RDRAMs,”
Symp. on VLSI Circuits, Digest of Papers (1999) 153 (DOI: 10.1109/VLSIC.1999.797268).
[4] B. Kim, et al.: “A 500 MHz DLL with second order duty cycle corrector for low jitter,”
IEEE Custom Integrated Circuits Conference (2005) 325 (DOI: 10.1109/CICC.2005.1568671).
[5] J. C. Ha, et al.: “Unified all-digital duty-cycle and phase correction circuit for QDR I/O interface,”
Electron. Lett. 44 (2008) 1300 (DOI: 10.1049/el.20080798).
[6] S. Kao, et al.: “All-digital fast-locked synchronous duty-cycle corrector,”
IEEE Trans. Circuits Syst. II, Exp. Briefs 53 (2006) 1363 (DOI: 10.1109/TCSII.2006.885396).
[7] Y. Min, et al.: “A 0.31–1 GHz fast-corrected duty-cycle corrector with successive approximation register for DDR DRAM applications,”
IEEE Trans.
1 Introduction

Following the mobile display and application processor (AP), DRAM memory is the largest power consumer in mobile devices such as smart phones. Low power double data rate 3 (LPDDR3) and LPDDR4 are the DRAM of choice for most of the latest smartphones [1, 2]. The latest LPDDR4 supports bandwidth of up to 4266 Mbits/s and incorporates a number of power-saving features. In order to reduce power consumption, LPDDR3 and LPDDR4 do not require a delay-locked loop (DLL) [9, 10] or phase-locked loop (PLL). However, LPDDR3 and LPDDR4 still require a duty-cycle corrector (DCC) since duty-cycle distortion (DCD) becomes worse as the data rate in mobile DRAM interface exceeds GHz range.

Therefore, one of the main challenges in the design of LPDDR3/LPDDR4 SDRAMs is the implementation of low-power DCCs that can provide a wide frequency range while maintaining high-resolution and fast lock capability. Although traditional analog DCCs [3, 4] are suitable over a wide operating frequency range, these are not able to support a fast wake-up from a power-down mode due to their analog nature. Thus, DCCs for mobile LPDDR3/LPDDR4 DRAMs must be designed using digital or hybrid approaches, since mobile DRAM interfaces require frequent power-mode transition. However, conventional digital DCCs [5, 6] have disadvantages including large areas, low-resolution and narrow duty-cycle correction ranges, limited operating frequency ranges, and large power consumption. Although hybrid DCCs [7, 8] are preferred for low power and wide frequency range operation, [7] was able to attain only a narrow operating frequency range of 0.3125–1.0 GHz owing to the limited capability of the complicated edge-generator based DCA. [8] achieved wide frequency and duty-cycle correction ranges; however, the DCC consumed large amounts of power as its DCA was based on analog differential pairs that required large static current. In this Letter, a new low-power, high-resolution, fast-lock hybrid DCC with a digital DCA for LPDDR3/LPDDR4 DRAMs is proposed. The proposed DCC utilizes a novel digital feedback delay element (DFDE) as its DCA in order to achieve low-power consumption as well as wide duty-cycle correction and operating frequency ranges. The DCC also adopts a 6-bit successive approximation register (SAR) controller to enable a hybrid (binary + sequential) search mode for fast locking.
2 Circuit design

Fig. 1 illustrates the proposed hybrid DCC, consisting of a digital DCA, a duty-cycle detector, and a SAR control block. The digital DCA with two cascaded 4-bit DFDEs receives an external input clock signal (INCLK) that may have duty-cycle distortions.

Based on the digital control signals A[7:0] and B[7:0], the DCA provides a single-ended full-swing output clock signal that has a 50% duty cycle. The duty-cycle detector consists of a charge pump and a comparator. The charge pump detects error in the duty-cycle of the output clock signal OUTCLK, while the comparator generates the up/down signal in response to the output signal, V/Vb, of the charge pump. The SAR control block consists of a 6-bit SAR, a 6-to-16 bit decoder, and a 1/8 divider. The duty-cycle detector and the SAR control block implement a feedback loop that senses error in the duty-cycle of the output clock and feeds back the control to the digital DCA in order to correct the duty-cycle error. The digital output Q[5:0] of the 6-bit SAR is input to the 6-to-16 decoder which generates DCA control signals A[7:0] and B[7:0].

In order to provide a sufficient timing margin for charge pump operation at high frequencies above 1 GHz and thus to minimize integrated errors in the duty-cycle, the SAR control block has an operating clock frequency that is 1/8 of the input clock frequency.

By transforming the binary search SAR into a sequential search counter after initial DCC lock-in, the proposed DCC retains closed-loop characteristics and is able to track variations in process, voltage, and temperature (PVT). This mixed (binary + sequential) search algorithm thus allows for higher operating frequency and duty-cycle correction accuracy without increasing the DCC locking time. At a SAR operating frequency that is 1/8 of the INCLK, the locking time of an N = 6-bit DCC would be \(8 \times N = 48\) INCLK cycles.

Fig. 2(a) shows the schematic of the proposed 1-bit DFDE, which consists of two inverters (INV1, INV2) and a 1-bit positive feedback control unit (PF CU). The PFCU consists of a tri-state inverter that has the input (OUT) and output (Z) signals. The gates of the two feedback transistors NF0 and PF0 are connected to the OUT node in order to establish positive feedback, while the gates of the two
switching transistors, N\textsubscript{S0} and P\textsubscript{S0}, receive the control signals A[0] and B[0], respectively, in order to enable or disable feedback. As shown in Fig. 2(b), when the PFCU is turned off (A[0] = '0' and B[0] = '1'), the output signal (OUT) of the DFDE has no change in the duty-cycle ratio.

If the pull-down network and the pull-up network of the PFCU are separately controlled by using the switching control signals A[0] and B[0], the duty cycle ratio of the OUT node can be adjusted. Fig. 2(c) shows how to increase the duty-cycle ratio when the input clock signal (IN) changes from High to Low with A[0] = '1' and B[0] = '1'. When the input node IN is logic HIGH, the intermediate node Z will be logic LOW, and the output node OUT will be logic HIGH; in this state, the pull-down network is turned on, causing the voltage transfer characteristics of the DFDE to shift. When the voltage at input node IN begins to transition from logic HIGH to LOW, the pull-down feedback path delays the rise of node Z to logic HIGH, which in turn delays transition of the output node OUT from logic HIGH to LOW. This leads to an increase in the duty-cycle ratio. In summary, enabling the pull-down network of the DFDE increases the duty-cycle ratio, and enabling the pull-up network reduces the duty-cycle ratio.

Fig. 2(d) shows how to decrease the duty-cycle ratio when IN changes from Low to High with A[0] = '0' and B[0] = '0'. In this case, the pull-up network is only turned on so that the falling slope of the Z node is slowed down, so only the rising edge of the OUT node is delayed, resulting in the decrease in the duty cycle ratio.
Fig. 3(a) shows the proposed 4-bit DFDE. The gates of transistors $N_{F0}$-$N_{F3}$ and $P_{F0}$-$P_{F3}$ are connected to the OUT node, while the gates of transistors $N_{S0}$-$N_{S3}$ and $P_{S0}$-$P_{S3}$ receive the control signals $A[3:0]$ and $B[3:0]$, respectively. Transistors $N_{F0}$-$N_{F3}$ and $P_{F0}$-$P_{F3}$ function as pull-down and pull-up networks, respectively. By providing a binary weighted parallel feedback path, the programmable hysteresis voltage characteristic of the 4-bit DFDE can be used to control the duty cycle ratio.

Fig. 3(b) shows the simulated 4-bit DFDE operation with an input clock duty cycle ratio of 40%. It shows how to increase the duty cycle ratio by activating the pull-down network with control bits of $A[3:0]$. Selectively turning on transistors $N_{S0}$-$N_{S3}$ enables the pull-down network of the positive feedback loop, while keeping the pull-up network disabled. There is no duty-cycle ratio change when $A[3:0] = 0000$. However, if $A[3:0] = 1111$ is applied, the duty-cycle ratio of the OUT node is increased by $+10\%$ and finally becomes 50%. As shown in Fig. 1, the duty-cycle correction range can be doubled by connecting two 4-bit DFDEs in series.

Fig. 4 shows the flow chart that illustrates the duty-cycle correction algorithm of the proposed fast-lock DCC. Initially, $Q[5:0]$ of the 6-bit SAR is set to [100000] and the DFDE control bits are set to $A[7:0] = 00000000$ and $B[7:0] = 11111111$, respectively. When the DCC starts to operate, the binary search node is first performed for $8 \times N = 48$ $IN_{CLK}$ cycles (where $N = 6$) to achieve fast...
locking. At the beginning of the operation, if Comp = ‘1’, this means that the output duty-cycle ratio is less than 50%. In this case, the value of Q[5:0], which is the output of the 6-bit SAR, is changed to [110000]. Thus, A[3:0] becomes [1111] and turns on the pull-down network of the 1st DFDE to increase the output duty-cycle ratio. Since A[7:4] remains unchanged to [0000] in this first cycle, all 2nd DFDEs are turned-off. If Comp = ‘1’ is still maintained in the next cycle, this still means the output duty-cycle ratio is less than 50%. Therefore, in order to further increase the duty-cycle ratio, the pull-down network of the 2nd DFDE needs to be additionally turned on, so the value of A[7:4] is changed to [1000]. When the binary search mode is completed in this way, the DCC starts the sequential search mode and maintains the locking status.

Fig. 5 shows a simulated locking operation of the proposed DCC with an input clock duty-cycle ratio of 40% at 1 GHz. In this case, because the input duty cycle is less than 50%, the DFDE’s pull-down network must be enabled to increase the output duty-cycle ratio. Since the input duty-cycle error is only 10%, the pull-down network of the 1st DFDE is only enabled while the 2nd DFDE is fully disabled (A[7:4] = [0000] and B[7:4] = [1111]). Therefore, if we look at the change of A[3:0], which is the control signal of the 1st DFDE, we can confirm the locking process of the DCC. It is shown that the DCC is locked at 48 ns.

The proposed mixed (binary + sequential) search algorithm achieves fast lock with higher duty-cycle correction accuracy. The DCC first performs a binary search, achieving a 50% duty-cycle OUTCLK in 48 clock cycles (= 8 × N = 48 INCLK cycles, where N = 6). After the binary search mode, the SAR is transformed into a sequential counter and the DCC performs sequential search mode to keep the locking status.
3 Measurement results

The proposed DCC was fabricated in a 0.13-µm, 1.2 V CMOS process. Fig. 6(a) shows the layout and silicon die of the proposed DCC, which has an active area of only 0.036 mm². Fig. 6(b) shows the test chip-on-board (CoB) assembly of the proposed DCC.

Fig. 7 shows the measured input and output clocks of the DCC at 1.0 GHz, when the input clock duty-cycle changes from 30% to 70%. For an input duty-cycle range of 30–70% over a frequency range of 0.2–1.5 GHz, the DCC achieved a maximum duty-cycle error of ±0.85%, dissipating only 1.9 mW of power at 1 GHz. As shown in Fig. 8, the measured peak-to-peak (p-p) jitter of the output clock is 8.75 ps at 1.5 GHz with a p-p input clock jitter of 7.5 ps. Therefore, the effective p-p jitter of the proposed DCC is only 1.25 ps.

A performance comparison between the proposed hybrid DCC and other state-of-the-art DCCs is given in Table I. The proposed DCC consumes the least power among the state-of-the-art DCCs and provides wider operating frequency range and smaller effective jitter.
Fig. 7. Measured input and output clocks of the proposed DCC at 1.0 GHz.

Fig. 8. Measured peak-to-peak jitter at 1.5 GHz.

Table I. Performance summary and comparison with state-of-the-art DCCs

|                        | [6]            | [7]            | [8]            | This Work       |
|------------------------|----------------|----------------|----------------|-----------------|
| Architecture           | Digital/Non-feedback | Hybrid/Feedback | Hybrid/Feedback | Hybrid/Feedback |
| Process & Supply       | 0.18 µm/1.8 V    | 0.13 µm/1.2 V   | 0.18 µm/1.8 V  | 0.13 µm/1.2 V   |
| Frequency range (GHz)  | 0.8–1.2         | 0.312–1.0       | 0.5–2.0        | 0.2–1.5         |
| Max. Correction Range  | ±10%            | ±10%            | ±30%           | ±20%            |
| Max. Duty Cycle Error  | ±1.5%           | ±1%             | ±1.49%         | ±0.85%          |
| p-p jitter (pS)        | 12.9 @1 GHz      | 15.5 @1 GHz     | -              | 1.25* @1.5 GHz  |
| Power (mW)             | 15 @1 GHz        | 3.2 @1 GHz      | 3.6 @1 GHz     | 1.9 @1 GHz      |
| Chip Area              | 0.23 mm²         | 0.048 mm²       | 0.043 mm²      | 0.036 mm²       |

*measured p-p jitter (8.75 ps) – input clock’s p-p jitter (7.5 ps)
4 Conclusion

We propose a low-power fast-lock DCC with a new digital DCA for use in mobile DRAM applications. Based on the functioning of its DFDE-based digital DCA, the proposed DCC was able to achieve higher duty-cycle correction accuracy and lower power consumption with smaller area than conventional DCCs; these results indicate that it should be well suited for use in low-power I/O and clocking circuits used in mobile LPDDR3/LPDDR4 DRAMs and mobile system-on-chip (SoC) applications.

Acknowledgments

This work was supported by the KIAT grant funded by the Korean government (MOTIE: Ministry of Trade, Industry & Energy, HRD Program for Software-SoC convergence. No. N0001883). The EDA tools were provided by IDEC, Korea.