Understanding of Polarization-Induced Threshold Voltage Shift in Ferroelectric-Gated Field Effect Transistor for Neuromorphic Applications

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Abstract: A ferroelectric-gated fin-shaped field effect transistor (Fe-FinFET) is fabricated by connecting a Pb(Zr_{0.2}Ti_{0.8})O_3-based ferroelectric capacitor into the gate electrode of FinFET. The ferroelectric capacitor shows coercive voltages of approximately −1.5 V and 2.25 V. The polarization-induced threshold voltage shift in the Fe-FinFET is investigated by regulating the gate voltage sweep range. When the maximum positive gate to source voltage is varied from 4 V to 2 V with a fixed starting negative gate to source voltage, the threshold voltage during the backward sweep is increased from approximately −0.60 V to 1.04 V. In the case of starting negative gate to source voltage variation from −4 V to −0.5 V with a fixed maximum positive gate to source voltage of 4 V, the threshold voltage during the forward sweep is decreased from 1.66 V to 0.87 V. Those results can be elucidated with polarization domain states. Lastly, it is observed that the threshold voltage is mostly increased/decreased when the positive/negative gate voltage sweep range is smaller/larger than the positive/negative coercive voltage, respectively.

Keywords: ferroelectric-gated field-effect-transistor (FeFET); ferroelectric capacitor; polarization; hysteresis; threshold voltage

1. Introduction

Following Moore’s law, the footprint of a transistor in as integrated circuit has been aggressively scaled down, resulting in improved performance/power consumption/integrity of integrated chips (ICs). In order to keep the Moore’s law alive, various steep switching devices featuring sub-60 mV/decade subthreshold slope (SS) have been proposed, resulting in overcoming the lower limit of SS (i.e., 60 mV/decade at 300 K), a.k.a., Boltzmann tyranny: tunnel field-effect transistor (TFET) [1], phase-transition FET [2,3], feedback FET [4,5], and negative capacitance FET (NCFET) [6]. Despite these advancements in transistors (especially for low-power applications), semiconductor societies have difficulties in realizing the Internet of Things (IoT) owing to the processing of enormous amounts of data [7,8]. Conventionally, von-Neumann-architecture-based computing systems have been used for processing large quantities of data, but such architectures encounter limitations in the realm of big data [9]. In recent years, the mimicking of biological brain synapses for neuromorphic systems has been widely investigated with the idea that these systems can process tremendous amounts of data at a faster transfer rate [10–13]. Non-volatile memory devices have been researched as synapse devices for the neuromorphic system, such as phase-change memory [14,15], resistive random-access memory [16], conductive-bridge random-access memory [17], and ferroelectric-gated FET (FeFET) [18]. Among these candidates, FeFET has been highlighted because FeFET can be fabricated by simply inserting a ferroelectric layer into the gate stack of a conventional MOSFET [19–21]. Having the same footprint as the conventional FETs, the FeFET can have non-volatile...
memory characteristics. FeFETs can mimic biological synapse characteristics as the ferroelectric domains are gradually switched by continuously applying a voltage, which leads to the threshold voltage shift and manipulation of the conductivity of FeFET [22–24].

Recently, ways to take advantage of hysteresis of FeFET for neuromorphic systems have been demonstrated (i.e. FeFET-based spiking neural networks (SNNs) [25,26] and oscillators [27]). Moreover, thanks to the CMOS-compatible device structure, an integrated ferroelectric-gated fin-shaped FET for neuromorphic applications has been introduced [28]. It has been also demonstrated that FeFETs can be utilized as multi-bit synapse devices by adjusting the number of ferroelectric domains [29]. From this point of view, the impact of domain switching on the operation of FeFET needs to be investigated to comprehend more deeply the operation of FeFET-based synapse devices. However, the experimental results have placed emphasis on the characteristics of neuromorphic synapse devices. Investigations on the polarization-induced threshold voltage shift are still lacking. Specifically, the effect of polarization switching from individual domains needed to be revealed. Therefore, in this study, the impacts of polarization behavior on the characteristics of a ferroelectric-gated fin-shaped FET (Fe-FinFET) are experimentally investigated by means of analyzing the input transfer characteristics. The Fe-FinFET used in this experiment was fabricated by connecting a Pb(Zr_{0.2}Ti_{0.8})O_3 (PZT)-based ferroelectric capacitor to the gate region of a baseline FinFET. The threshold voltage in the backward sweep ($V_{\text{th, backward}}$) of the Fe-FinFET increases from $-0.60 \text{ V}$ to $1.04 \text{ V}$, when the maximum positive gate-to-source voltage ($V_{\text{GS, positive}}$) with a negative gate-to-source voltage ($V_{\text{GS, negative}}$) of $-4\text{ V}$ is decreased from $4 \text{ V}$ to $1 \text{ V}$. On the other hand, when $V_{\text{GS, negative}}$ is varied from $-4 \text{ V}$ to $0 \text{ V}$ with a fixed $V_{\text{GS, positive}}$ of $4 \text{ V}$, the threshold voltage in the forward sweep ($V_{\text{th, forward}}$) decreases from $1.67 \text{ V}$ to $0.87 \text{ V}$. Those results are elucidated with polarization switching and coercive voltage in ferroelectric material.

2. Fabrication and Measurement

In this work, n-type enhancement mode FinFET is utilized as a baseline FET. The schematics of the Fe-FinFET are illustrated in Figure 1. The baseline FinFET has 80 nm, 30 nm, 40 nm, 5, 200 nm, and 1.4 nm channel length, fin width, fin height, number of fins, fin pitch, and equivalent oxide thickness, respectively. The fabrication process of the PZT ferroelectric capacitor used in this work is as follows: (i) a NdScO_3 substrate was prepared and (ii) a 20 nm-thick La_{0.7}Sr_{0.3}MnO_3 was deposited as the bottom electrode. Subsequently, (iii) a 60nm-thick Pb(Zr_{0.2}Ti_{0.8})O_3 (PZT) ferroelectric film was deposited using a pulsed laser deposition technique. Lastly, (iv) 60 nm-thick Au/Ti/Au top electrodes were deposited and patterned. The flow of the aforementioned fabrication process is illustrated in Figure 2b. The Fe-FinFET was implemented by physically linking the PZT-based ferroelectric capacitor to the gate region of baseline FinFET with gold wire. Each measurement was done using the Keithley 4200A-SCS semiconductor parameter analyzer at 300 K. For the input transfer curve measurement, forward and backward gate voltage sweep are done in sequence.

In the measurement, the gate-to-source voltage is applied to the device from $V_{\text{GS, negative}}$ to $V_{\text{GS, positive}}$ (i.e., forward sweep), then the gate-to-source voltage is applied to the device from $V_{\text{GS, positive}}$ to $V_{\text{GS, negative}}$ (i.e., backward sweep). In this work, the ranges of the gate voltage sweep are varied in two opposite ways: (1) $V_{\text{GS, positive}}$ decreases from $4 \text{ V}$ to $1 \text{ V}$ with the fixed $V_{\text{GS, negative}}$ of $-4 \text{ V}$. (2) $V_{\text{GS, negative}}$ increases from $-4 \text{ V}$ to $0 \text{ V}$ with the fixed $V_{\text{GS, positive}}$ of $4 \text{ V}$. Note that $V_{\text{th, forward}}$ and $V_{\text{th, backward}}$ were extracted using the constant current method at $1.375 \times 10^{-7} \text{ A}$ (i.e., $10^{-7} \text{ A} \times (2H_{\text{fin}} + W_{\text{fin}})/L_{\text{fin}}$). The hysteresis width was calculated by subtracting $V_{\text{th, backward}}$ from $V_{\text{th, forward}}$. 
Although it casts doubt on the ferroelectricity, this device still shows the properties of a ferroelectric layer. Each domain in the ferroelectric layer has its own coercive voltage because it has more or less doping concentration and grain size than the other domains. As a result, an externally applied voltage can switch the polarization direction of only those domains which have a lower coercive voltage than the applied voltage [31–35]. This partial polarization switching can gradually change the conductivity of FeFETs for neuromorphic applications [36]. In order to investigate the partial polarization switching, we have fabricated a ferroelectric capacitor, and its measured capacitance (C)–voltage (V) is drawn in Figure 2a. The positive and negative coercive voltage of the ferroelectric capacitor are ~2.25 and ~−1.5 V, respectively. Compared with previous results which show one sharp peak [22], the two peaks at the negative coercive voltage would have originated from aging effect. Although it casts doubt on the ferroelectricity, this device still shows the properties of a ferroelectric layer [see Figure S1 in Supplementary Information]. Figure 3 illustrates the measured input transfer curves of FeFET for various VGS_positive with the same VGS_negative. For all cases [i.e., (i), (ii), and (iii)], the VGS_negative (which is higher than the negative coercive voltage of ferroelectric capacitor for the FeFET) is identical, so that the initial polarization state is identical (i.e., the initial state is aligned upward). As a result, the Vth_forward of the three cases are almost identical. In the case of (i), the VGS_positive induces complete polarization switching, and, thereby, all the domains in the ferroelectric layer are
switched to the downward direction. This should result in the $V_{th,\text{backward}}$ being lower than the $V_{th,\text{forward}}$. The reason for this observation comes from the fact that the downward polarization (in addition to the vertical electrical field from the gate electrode) contributes to the accumulation of electrons when forming a channel. However, in the case of (ii) and (iii), the $V_{GS,\text{positive}}$ is not high enough to switch every domain, which results in partial polarization switching (i.e., partially downward). Therefore, the $V_{th,\text{backward}}$ for case (ii) and (iii) is higher than the value for case (i).

In order to analyze the impact of partial polarization switching on the operation of synapse devices, a FeFET was fabricated and then measured with different gate voltages (i.e., from 3 V or 4 V) for a fixed $V_{GS,\text{negative}}$ (i.e., $-4$ V) [see Figure 4a]. For 3–4 V of the $V_{GS,\text{positive}}$, the situations are corresponding to the case of (i) shown in Figure 3 (i.e., complete polarization switching). Although the $V_{GS,\text{positive}}$ values are different (i.e., 3 V or 4 V), the $V_{th,\text{backward}}$ values are similar to each other. In reality, the $V_{th,\text{backward}}$ values for the positive gate voltages of 4, 3.5, and 3 V are approximately $-0.60$, $-0.54$, and $-0.49$ V, respectively. These measurement results indicate that there are few domains which have coercive voltages between 3 and 4 V in the ferroelectric layer. Conversely, for the case of the $V_{GS,\text{positive}}$ from 2.5 V to 2 V (which is comparable to the positive coercive voltage of $-2.25$ V), the $V_{th,\text{backward}}$ increases from approximately $-0.02$ to $1.04$ V. This situation corresponds to either case (ii) or (iii), as shown in Figure 3. This represents the partial polarization switching occurring in the ferroelectric layer, resulting in the threshold voltage shift. In the case of $V_{GS,\text{positive}}$ from 2 V to 1 V, the Fe-FinFET is not turned on due to the lack of gate voltage sweep range. Regardless of the $V_{GS,\text{positive}}$ in all the measurements, the $V_{th,\text{forward}}$ values are almost identical when the device is turned on, because the initial polarization states are the same as described above. The $V_{th,\text{forward}}$ and $V_{th,\text{backward}}$ variation is characterized as a function of $V_{GS,\text{positive}}$ [see Figure 4c]. Figure 4b shows the hysteresis and subthreshold slope during backward voltage sweep ($SS_{avg,\text{backward}}$ vs. gate voltage. As the hysteresis is decreased from $-2.51$ to $-0.82$ V due to the $V_{th,\text{backward}}$ shift, the $SS_{avg,\text{backward}}$ increases from $-80$ to $-462$ mV/decade. This can be understood and explained using SS and load-line

![Figure 3. Drain current versus gate voltage with a decreasing upper limit of positive gate voltage. The inset indicates the initial polarization status of a ferroelectric PZT capacitor for a given negative gate voltage (i.e., sufficiently lower than the negative coercive voltage of the PZT capacitor). (i), (ii), and (iii) illustrate the polarization status for a few different upper limits of positive gate voltage.](image-url)
analysis in FeFETs [6,37–39]. A detailed analysis is described in the Supplementary Information (see the Figure S2 in the Supplementary Materials).

![Figure 4.](image)

Figure 4. (a) Measured drain current versus gate voltage for various $V_{GS, positive}$ (i.e., from 4 to 1 V) with the fixed $V_{GS, negative}$ of −4 V. (b) Hysteresis (left-axis) and $SS_{avg, backward}$ (right-axis) versus gate voltage sweep range of the Fe-FinFET. (c) $V_{th, forward}$ (left-axis) and $V_{th, backward}$ (right-axis) versus gate voltage sweep range of the Fe-FinFET.

Figure 5a shows the measured input transfer curves for various $V_{GS, negative}$ (i.e., from −4 to 0 V) with a fixed $V_{GS, positive}$ of 4 V. Contrary to the previous measurements adjusting $V_{GS, positive}$, the $V_{th, negative}$ is maintained regardless of the gate voltage sweep range. The reason for the observation shown in Figure 5 is that the polarization states during the backward sweeps are identical owing to the complete polarization switching from the fixed $V_{GS, positive}$ whereas the $V_{th, forward}$ decreases as the $V_{GS, negative}$ increases from −4 to 0 V. When the $V_{GS, negative}$ is changed from −4 to −1.5 V, the $V_{th, forward}$ is almost unvaried within the range of −1.82 to −1.67 V [see Figure 5c]. This situation corresponds to the case of manipulating $V_{GS, positive}$ from 4 to 3 V. The unvaried $V_{th, forward}$ means that there are few domains having a negative coercive voltage that is smaller than −3 V. The $V_{th, forward}$ starts to further decrease as the $V_{GS, negative}$ becomes larger than −1.5 V (i.e., a similar value to the positive coercive voltage of approximately −1.5 V). The $V_{th, forward}$ for the $V_{GS, negative}$ of −1 and −0.5 V are −1.43 and −0.87 V, respectively. The decrease in $V_{th, forward}$ originates from the polarization state after the measurement immediately before (i.e., the case of $V_{GS, negative}$ of −1.5 V). After this measurement,
the polarization states are not fully arranged to the upward direction due to some domains which have a negative coercive voltage smaller than ~1.5 V. As a result, electrons can be assembled to form a channel at a gate voltage lower than the previously measured one. Similarly, in the case of \( V_{\text{GS\_negative}} \) of 0 V, the \( V_{\text{th\_forward}} \) is decreased, but the current level becomes so high that the exact \( V_{\text{th\_forward}} \) cannot be extracted using the constant current method at \( 1.375 \times 10^{-7} \) A. These \( V_{\text{th\_forward}} \) and \( V_{\text{th\_backward}} \) variations are plotted in Figure 5c. Figure 5b shows the well-known relationship between the hysteresis (from ~2.26 to ~1.32 V) and \( SS_{\text{avg}} \) (from ~101 to ~161 mV/decade).

![Figure 5](image-url)

**Figure 5.** (a) Measured drain current versus gate voltage for various \( V_{\text{GS\_negative}} \) (i.e. from ~4 to 0 V) with the fixed \( V_{\text{GS\_positive}} \) (i.e., 4 V). (b) Hysteresis (left-axis) and \( SS_{\text{avg\_forward}} \) (right-axis) versus gate voltage sweep range plots of the Fe-FinFET. (c) \( V_{\text{th\_forward}} \) (left-axis) and \( V_{\text{th\_backward}} \) (right-axis) versus gate voltage sweep range plots of the Fe-FinFET.

From all the measurement data shown above, various parameters and characteristics for neuromorphic applications (e.g., pulse amplitude used for the function of “firing”) can be acquired. This is because \( V_{\text{GS\_positive}} \) and \( V_{\text{GS\_negative}} \) are equivalent to the amplitude of pulse measurement, in terms of electrical effects, which is the usual method for investigating the characteristics of neuromorphic applications. To be specific, it can be deduced that, if this device is used as a synapse device, the maximum pulse amplitude should not exceed 3 V because it will not affect any polarization state [see Figure 4a]. It can also be found that the threshold voltage shift is originated from the ferroelectricity. This means that if the device shows the characteristics of FeFET (even though the fabrication process or materials are changed), the contents (i.e., the trend shown in Figures 4 and 5) in this work should be applicable. Furthermore, this externally connected device structure is useful when various properties of capacitors need to be investigated, because the capacitor can be simply
replaced with other ones. For example, in an externally connected device structure, a sufficiently scaled-down ferroelectric capacitor, which has a few domains, can be used for investigating multi-bit neuromorphic systems without scaling down the baseline FET. On the other hand, in an integrated FeFET structure, the ferroelectric capacitor and baseline FET must be scaled down together to realize a few domains [23,24]. Likewise, using the externally connected device structure, we expect that the polarization-induced threshold voltage shift in FeFET will facilitate decisions about various parameters in neuromorphic applications.

4. Conclusions

The threshold voltage shift characteristics of the Fe-FinFET with a PZT-based ferroelectric capacitor were studied to understand the impact of polarization state on the device operation. The PZT-based ferroelectric capacitor had approximately 2.25 V and −1.5 V of the positive coercive voltage and negative coercive voltage, respectively. The Fe-FinFET was measured with various gate-to-source voltage sweep ranges. Because of the partial polarization switching (i.e., partially downward), the $V_{\text{th, backward}}$ was increased from ~0.60 to 1.04 V when the $V_{\text{GS, positive}}$ was decreased from 4 to 2 V for the same $V_{\text{GS,negative}}$ of ~4 V. When the $V_{\text{GS, positive}}$ was adjusted to a value similar to the positive coercive voltage (i.e., 2.5 and 2 V), the $V_{\text{th, backward}}$ was increased to ~0.02 and 1.04 V, respectively. When the $V_{\text{GS,negative}}$ was regulated from 4 to ~−0.5 V for the same $V_{\text{GS, positive}}$ of 4 V, the $V_{\text{th, forward}}$ was decreased from ~1.67 to ~−0.87 V. Similarly, the $V_{\text{th, forward}}$ was decreased to ~1.43 and ~−0.87 V when the $V_{\text{GS,negative}}$ was changed to a value similar to the negative coercive voltage (i.e., ~−1 and ~−0.5 V), respectively. From this research, it was proposed that the externally connected FeFET can contribute to the understanding of the operation of FeFET-based synapse devices in a different way, with the investigation of integrated FeFET-based synapse devices. For multi-bit neuromorphic applications, investigation of the synaptic characteristics of FeFET with sufficiently tiny ferroelectric capacitors needs to be implemented.

Supplementary Materials: The following are available online at http://www.mdpi.com/2079-9292/9/5/704/s1, Figure S1: The charge vs. voltage plot of the Pb(Zr$_{0.5}$Ti$_{0.5}$)O$_3$-based ferroelectric capacitor, Figure S2: (a) Capacitive network of ferroelectric-gated FET; (b) load-line analysis of ferroelectric-gated FET.

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