Electronic circuit implementation of chaos synchronization

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In this paper, an electronic circuit implementation of a robustly chaotic two-dimensional map is presented. Two such electronic circuits are realized. One of the circuits is configured as the driver and the other circuit is configured as the driven system. Synchronization of chaos between the driver and the driven system is demonstrated.

I. INTRODUCTION

Chaotic systems are sensitive to initial conditions and diverge exponentially. Even if there is an infinitesimally small difference in initial conditions, two identical chaotic systems spiral out along completely different paths. Synchronization of chaotic dynamics is a phenomenon wherein two or more chaotic systems, in the presence of a drive signal, adjust some property of their dynamics to bear a mathematical relationship. According to Pecora and Carroll, chaotic flows or iterated maps can be synchronized, in such a way that their states are almost identical, if they are coupled with a drive signal[1].

Robustness of chaos implies that in some neighborhood of the parameter space, the chaotic dynamics is free of any windows of periodicity. The absence of any windows of periodicity ensures that small changes in the parameter do not destroy chaos. Such structural stability of chaos is valuable, especially in engineering applications[2].

In[1] synchronization was achieved between electronic circuit realization of two flows. The flows were modified versions of an RC op-amp chaos generator. Few electronic circuit realizations of iterative chaotic maps have been reported in[3] and[4]. In this paper, an analog electronic circuit realization of a robustly chaotic iterative two-dimensional map is presented. Then, synchronization between two such electronic circuits is demonstrated.

II. THE MAP AND THE COUPLING SCHEME

The implemented map is a two-dimensional chaotic system that reduces to the Hénon and Lozi systems at its extremes[5]. The map is defined as

\[ (x_{k+1}, y_{k+1})^T = U(x_k, y_k), \]

where,

\[ U(x, y) = \left( 1 - 1.4f_{\alpha_b}(x) + y \right), \]

and \((x_k, y_k)\) is the state of the system. Here, \(\alpha_b\) is the bifurcation parameter and

\[ f_{\alpha_b}(x) = \alpha_b |x| + (1 - \alpha_b) x^2. \]

For \(\alpha_b = 1\) and \(\alpha_b = 0\), (2) reduces to the Lozi map and the Hénon map, respectively. The map is robustly chaotic for \(0 \leq \alpha \leq 1\). The implementation scheme is shown in figure[1].

In this paper, the drive signal \(x_k\) of the driver system is unidirectionally coupled to the driven system. The driver system can be written as,

\[ (x_{k+1}^r, y_{k+1}^r)^T = U(x_k^r, y_k^r), \]

where, \((x_k^r, y_k^r)\) denotes the state of the driver system at time \(k\). The driven system can be written as,

\[ (x_{k+1}^n, y_{k+1}^n)^T = U(\alpha_c x_k^r + (1 - \alpha_c) x_k^n, y_k^n), \]

where, \((x_k^n, y_k^n)\) denotes the state of driven system at time \(k\). \(0 \leq \alpha_c \leq 1\) is the coupling factor between the two systems. The coupling scheme is illustrated in figure[2].

III. CIRCUIT REALIZATION

A block diagram representation of the electronic circuit realization is shown in figure[3] Here, the bifurcation factor, \(\alpha_b\)
is chosen to be 0.4. The upper block of figure 3 implements $U(x, y)$ and computes the next state of the system, given the present state at its input. The lower block of figure 3 is a pair of sample-and-hold blocks, that remember the state of system for the duration of one clock cycle.

A. The circuit

The complete circuit used to realize the blocks of figure 3 is shown in figure 4. In the reported circuit realization, for computing $|x|$, for multiplying with a constant, and for a weighted sum, operational amplifiers are used. The operational amplifiers used were the integrated circuit LM324. The function $x^2$ is implemented by an analog multiplier, MPY634 [6]. Each sample-and-hold circuit is implemented using one LF398 integrated circuit [7]. The LF398 is a level-triggered circuit. Therefore, to obtain the necessary discrete-time nature of the map, each time-delay block is implemented in the form of two sample-and-hold circuits. The two circuits are driven by clock-waveforms that are $180\degree$ out-of-phase.

B. Synchronization

The synchronization scheme used is the same as that shown in figure 4. Here the state variable $x_k$ of driver circuit, is fed to the driven circuit, through a coupling factor.

The coupling circuit is just a weighted sum circuit, followed by a voltage follower stage, as shown in figure 5. The output of coupling circuit is $\alpha_c x_k^o + (1 - \alpha_c) x_k^n$. For $\alpha_c = 0.5$, $R_f = 5K\Omega$, $R_n = 10K\Omega$ and $R_r = 10K\Omega$. To obtain the value of $5K\Omega$ two $10K\Omega$ resistors were connected in parallel. For $\alpha_c = 0.4$; $R_f = 3.3K\Omega$, $R_n = 8K\Omega$ and $R_r = 5.5K\Omega$.

IV. RESULTS

The driver and driven voltages pertaining to $x_k^o$ and $x_k^n$ were captured on a digital storage oscilloscope and displayed as trace C1 and C2, respectively. The error voltage pertaining to these, was also computed and displayed on the oscilloscope as trace F1. Such oscilloscope trace, pertaining to an un-coupled pair of maps ($\alpha_c = 0$) is shown in figure 6. The lack of synchronization is evident. Oscilloscope trace for $\alpha_c = 0.4$ is shown in figure 7. It can be seen that the maps synchronize with a small error voltage. Oscilloscope trace for $\alpha_c = 0.5$ is
shown in figure 8. It can be seen that the maps synchronize with an error voltage of almost zero.

V. POTENTIAL APPLICATIONS

One potential application of such electronic circuit realization of synchronized robustly chaotic maps is in cryptography. Another potential application is in secure wireless communication.

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