A 16-bit 8-MS/s SAR ADC with a foreground calibration and hybrid-charge-supply power structure

Zhenwei Zhang\textsuperscript{1,2}, Lei Qiu\textsuperscript{3}, Yi Shan\textsuperscript{1}, and Yemin Dong\textsuperscript{1,4a)

Abstract In this paper, a 16-bit 8-MS/s successive approximation register analog-to-digital converter (SAR ADC) with a foreground calibration technique is proposed. A nonbinary searching algorithm is adopted to speed up the conversion rate and overcome the incomplete settling of the reference voltage. A foreground calibration method with low-cost circuitry is implemented to detect the mismatch of the capacitor digital-to-analog converter in calibration mode and compensate for the output code in conversion mode. The simulation results show that the peak signal-to-noise and distortion (SNDR) and spurious free dynamic range (SFDR) are improved from 69.98 dB to 91.39 dB and 73.94 dB to 99.41 dB, respectively. Moreover, the proposed ADC uses a hybrid-charge-supply power structure. The sampling circuit operates at 3.3 V to maintain a wide dynamic range, the logic circuit operates at 1.2 V to decrease the conversion time and power consumption, and the total power consumption is 45 mW at 8 MS/s.

key words: analog-to-digital converter, nonbinary, foreground calibration, SAR ADC

Classification: Integrated circuits

1. Introduction

The rapid development of the Internet of Things (IoT) is driving the world into a ubiquitous sensing environment with an emphasis on edge computing, which results in stringent requirements for both high-resolution (>10b) and lower-power analog-to-digital converters (ADCs). The successive approximation register (SAR) ADC has gained considerable interest in high-resolution implementations over the past several years due to its excellent power efficiency [1]-[10]. However, there is a trade-off between resolution and sampling rate. To achieve a high sampling rate, this paper adopts the nonbinary capacitor digital-to-analog converter (DAC) [11]-[13] to reduce the conversion time. For a high-resolution SAR ADC, the capacitor mismatch of the DAC is a critical problem [14]-[21]. To calibrate the mismatch, this paper proposes a new foreground calibration technique that requires less silicon area and power consumption. When the ADC works in calibration mode, the calibration circuit detects the mismatch of the capacitor and stores the calibration codes in the memory cell. When the ADC works in conversion mode, the calibration circuit fetches the calibration codes in memory and compensates for the output code of the ADC. Apart from the DAC mismatch, noise is another factor that limits the performance of a high-resolution SAR ADC. With a reduction of power supply, the noise becomes larger than the LSB level of the ADC. To degrade the noise level, several techniques have been proposed. References [2] and [22] decreased the noise by oversampling the comparator. However, these approaches sacrifice speed due to the additional cycle. A noise-tunable comparator was designed in [23] to tune the noise level such that the input-referred noise (IRN) level of the comparator could always be tuned below the LSB of the ADC. A low-noise pre-amplifier is adopted to suppress the noise of comparator. Moreover, this paper proposes a hybrid-charge-supply power structure. The sampling circuit built by IO transistor operates at 3.3 V to accommodate a 3 Vp-p input swing. The rest circuit built by core devices operates at 1.2 V to decrease the conversion time and power consumption. The wider dynamic range means a larger LSB, which reduces the impact of noise on the ADC performance.

2. ADC architecture and implementation

Fig. 1 shows the overall ADC system architecture, which mainly consists of bootstrap switch, clock generator, 18-bit main D/A conversion circuit (MDAC), 7-bit calibration D/A conversion circuit (CAL_DAC), comparator and SAR logic. The ADC sampling network and part of the DAC buffer are built by IO transistor and operate at 3.3 V to accommodate a 3 Vp-p input signal, and the rest of the logic circuits all operate at 1.2 V. The
ADC is implemented with a nonbinary weight DAC. A total of 18 cycles are used to perform a 16 bits conversion with 2 redundant cycles, and the weight of each capacitor, except for the low 4-bit capacitors are designed with redundancy. By increasing the redundant range of the MSB capacitors, the incomplete settling error of the DAC can be covered while simultaneously reducing the total conversion time. Benefiting from the foreground calibration circuit, the actual weights of the DAC after fabrication can be acquired. Then, the 16-bit outputs are calculated from the 18 raw bits by a digital adder according to the actual weights. A comparator with a pre-amplifier is employed to reduce the comparator noise and amplify the LSB level in this design. The output offset storage (OOS) technique [24] is used to eliminate the offset of the pre-amplifier.

2.1 Nonbinary capacitor DAC
Traditionally, SAR ADC uses binary searching algorithm. However, this paper adopts a nonbinary searching algorithm to reduce the conversion time. To better design the redundancy ratio of each capacitor, the relationship between the redundancy ratio and the DAC settling time was studied. For a binary SAR ADC, to ensure that the DAC can converge to one LSB in the last, the settling error \( \epsilon_i \) must satisfy

\[
\epsilon_i < \frac{1}{2} \text{LSB}. \tag{1}
\]

When the DAC buffer charges the capacitor, the voltage on the capacitor can be calculated as

\[
V_{\text{cap}} = V_{\text{ref}} (1 - e^{-\frac{t}{\tau}}). \tag{2}
\]

\( \tau = R_{\text{ON}} \cdot C \) is the time constant. \( R_{\text{ON}} \) is the turn-on resistance of DAC buffer. Based on equations (1) and (2), the settling time can be derived as

\[
t > (N \cdot \ln 2) \cdot \tau. \tag{3}
\]

\( N \) is the resolution of the SAR ADC. That the settling time is proportional to the resolution \( N \) can be obtained from equation (3).

By adopting a nonbinary searching algorithm, the settling accuracy requirement can be relaxed. Suppose that the redundant ratio of the \( L^o \) comparator is \( \epsilon_{i} \), as long as the settling error satisfies

\[
\epsilon_{i} < \epsilon_{i} \cdot V_{\text{ref}} \tag{4}
\]

there is no conversion error. Based on equations (2) and (4), the settling time can be derived as

\[
t > \ln(\frac{1}{\epsilon_{i}}) \cdot \tau \tag{5}
\]

The relationship between the settling time and redundant ratio is shown in Fig. 2, which illustrates that the redundancy can reduce the settling time. For instance, a 16-bit SAR ADC only needs 3.2 times \( \tau \) for a 4% redundant ratio but needs 11.09 times \( \tau \) without redundancy. The relationship between the redundant ratio and reduced time is also shown in Fig. 2.

Taking into account the incomplete settling of the reference voltage [25], the weights of the capacitors in the DAC array are designed and optimized. Table I shows the weights and redundant ratio for each capacitor in the DAC array. This redundant design only needs 75.36 times \( \tau \) for the DAC capacitor to complete the settling. However, the design takes 177.44 times \( \tau \) without redundancy.

![Fig. 2. Relationships between the redundant ratio and required/reduced settling time](image)

![Fig. 1. ADC architecture](image)

| Capacitor | Bit weight | Redundant range (LSB) | Redundant ratio (%) |
|-----------|------------|-----------------------|---------------------|
| C0        | 1          | 0                     | 0.00%               |
| C1        | 2          | 0                     | 0.00%               |
| C2        | 4          | 0                     | 0.00%               |
| C3        | 7          | 0                     | 0.00%               |
| C4        | 13         | 1                     | 7.69%               |
| C5        | 26         | 2                     | 7.69%               |
| C6        | 50         | 2                     | 4.00%               |
| C7        | 90         | 4                     | 4.44%               |
| C8        | 162        | 14                    | 8.64%               |
| C9        | 292        | 32                    | 10.96%              |
| C10       | 520        | 64                    | 12.31%              |
| C11       | 912        | 128                   | 14.04%              |
| C12       | 1568       | 256                   | 16.33%              |
| C13       | 2624       | 512                   | 19.51%              |
| C14       | 4224       | 1024                  | 24.24%              |
| C15       | 6400       | 2048                  | 32.00%              |
| C16       | 15872      | 4096                  | 25.81%              |
| -         | 32768      | 1024                  | 3.15%               |
2.2 Calibration design

Metal-oxide-metal (MOM) capacitors exhibit mismatch after fabrication because of the parasitism and variation in the process, especially in an advanced process due to metal space shrinkage. Thus, the actual value of \( i^{th} \) capacitor is

\[
C_i = \text{weight} \cdot C_0 + \Delta C_i.
\]  

(6)

\( C_0 \) is the unit capacitor, \( \Delta C_i \) is the variation between the ideal capacitance and the actual capacitance of the \( i^{th} \) capacitor. Under ideal circumstances, the calibrated capacitor \( C_i \) and the corresponding LSB capacitors \( C_{LSBS} \) satisfy

\[
C_i = \sum C_{LSBS}.
\]  

(7)

However, due to the mismatch. Equation (7) is no longer valid. Two cases are shown in equation (8).

\[
\begin{align*}
&\begin{cases}
C_i + \Delta C_i > \sum C_{LSBS} \quad \Delta C_i > 0, \\
C_i + \Delta C_i < \sum C_{LSBS} \quad \Delta C_i < 0.
\end{cases}
\end{align*}
\]  

(8)

To detect the variation \( \Delta C_i \), calibration capacitors are added to the smaller side of equation (8) to equate the right side and the left side. Equation (8) becomes

\[
\begin{align*}
&\begin{cases}
C_i + \Delta C_i = \sum C_{LSBS} + C_{CAL} \quad \Delta C_i > 0, \\
C_i + \Delta C_i = \sum C_{LSBS} + C_{CAL} \quad \Delta C_i < 0.
\end{cases}
\end{align*}
\]  

(9)

According to equation (9),

\[
\Delta C_i = C_{CAL}
\]  

(10)

can be obtained. Equation (10) is the fundamental equation for the DAC array calibration. Every capacitor in the DAC array can use this method to perform the calibration.

---

**Fig. 3. Calibration system for the SAR ADC**

The proposed foreground calibration technique can reduce the adverse effects of the mismatch of the DAC capacitor at a low cost of silicon area and power consumption. The calibration system is shown in Fig. 3. First, the calibration circuit sends control signals to the mismatch detection circuit. The output of the comparator will change when the calibration is complete. Then, the correct weight of the calibrated capacitor will be written to the memory unit, waiting to be fetched during the conversion.

Noting that when implementing the calibration circuit, due to the redundancy, the LSB capacitors that participating in the calibration need to satisfy equation (7), and the remaining capacitors do not participate in the calibration. The schematic of calibration circuit is shown in Fig. 4. First, the bottom plate of \( C_i \) and the corresponding LSB capacitors connect to \( V_{refp} \) and \( V_{refn} \), respectively. The remaining capacitors not participating in the calibration connect to the ground (GND), and the top plate of all capacitors connected to \( V_{cm} \), as shown in Fig. 4(a). Then, the top plate of the capacitor is disconnected from \( V_{cm} \) and the voltages connected by \( C_i \) and \( C_{LSBS} \) are exchanged, as shown in Fig. 4(b). Because the charge at the top plate in phase 1 and phase 2 keep constant, equation (11) can be derived.

\[
V_p - V_N = \frac{C_i \cdot (C_{LSBS} + C_{CAL} + V_{refp} - V_{refn})}{C_i - C_{LSBS}} + V_{OS}
\]  

(11)

\( V_{OS} \) is the offset of comparator. Letting \( C_{mis} = C_i - C_{LSBS} \),

\[
V_p - V_N = -C_{mis} \cdot Isb + V_{OS}
\]  

(12)

Phase 3 and phase 4 are shown in Fig. 4(c) and Fig. 4(d), respectively. The capacitors connect in the opposite way compared with the connections in phase 1 and phase 2. Therefore, a similar equation can be obtained

\[
V_p - V_N = C_{mis} \cdot Isb + V_{OS}
\]  

(13)

The principle of the calibration is to make \( V_p - V_N = 0 \), which can be realized by adding some calibration capacitors \( C_{cal} \) in parallel with \( C_i \) or \( C_{LSBS} \). As shown in Fig. 4(e), when trim_sign=1, \( C_{cal} \) is in phase with \( C_{LSBS} \). Otherwise, \( C_{cal} \) is in phase with \( C_i \). Trim_sign can be tuned according to the polarity of cal_out.

The calibration timing diagram is shown in Fig. 5. First, set chop=1, and the calibration circuit works in
phase 1 and phase 2. If Cal_out=0, assign trim_sign=1; otherwise, assign trim_sign=0, and tune trim_bit<6:0> step by step until Cal_out changes. Then, set chop=0, and repeat the same procedures used when chop=1. The flowchart of the calibration steps is presented in Fig. 6. After \( C_i \) is calibrated, according to equations (12) and (13), \( C_{mis} \) and \( V_{os} \) can be acquired as

\[
\begin{align*}
V_{oss} &= \frac{C_{cal1} + C_{cal0}}{2} \\
C_{mis} &= \frac{C_{cal1} - C_{cal0}}{2}
\end{align*}
\]  

(14)

Note that the polarity of \( \text{Ccal0} \) and \( \text{Ccal1} \) is critical when calculating \( C_{mis} \) and \( V_{os} \). Every capacitor in the MDAC can be calibrated in a similar way. After all the mismatches are acquired, the actual weight of each capacitor in the MDAC can be calculated from

\[
C_i = \sum C_{mis} + \sum C_{lsb}
\]  

(15)

Finally, all the weights will be stored in the memory unit, which can be fetched during the conversions to compensate for the output codes by an off-chip calibration circuit.

To ensure that the calibration circuit can completely cover the capacitor mismatch, the range of mismatch needs to estimate. The proposed MOM capacitor is shown in Fig. 7. The unit capacitor consists of metal1 to metal6, and the bottom-plate encloses the top-plate, which reduces the parasitic capacitance of the top plate. The capacitance of the unit cell is about 0.65 fF. The variation in a MOM capacitor might not be reported in the technology document provided by the wafer foundry, however, according to [26], the standard deviation \( \sigma_u \) of a finger capacitor is around 0.009 when the capacitance is 0.65 fF. The capacitor matching might be worse than that of the finger capacitor due to the floor-plan layout and wire routing. Assuming that \( \sigma_u \) is 0.03 in this work, the three standard deviation capacitance mismatch of the MSB capacitor is

\[
C_{mis, MSB} = 3 \times 3\sqrt{1744 \times 0.03} \times C_u = 16C_u
\]  

(16)

From equation (16), that the largest mismatch of the capacitors is 16\( C_u \) can be obtained. Taking into account the offset of the comparator, the CAL_DAC is designed as 64\( C_u \) to ensure it can fully cover the mismatch. The detail information of CAL_DAC is shown in TABLE II.

| Capacitor | Range (C\( u \)) |
|-----------|-----------------|
| \( C_{cal0} \) | 1/2 \( C_u \) |
| \( C_{cal1} \) | 2 \( C_u \) |
| \( C_{cal2} \) | 8 \( C_u \) |
| \( C_{cal3} \) | 32 \( C_{cal} \) |

2.3 Hybrid-charge-supply power structure

To achieve a wide input range and reduce the effects of noise while maintaining a high speed and low power consumption, a hybrid-charge-supply power structure is presented. The sampling circuit and DAC array buffer which are built by IO transistors operate at 3.3 V to accommodate a 6 \( V_{pp,diff} \) input swing, while the comparator and other logic circuits built by the core device operate at 1.2 V to improve the speed and decrease the power consumption. The pre-amplifier is a critical circuit to realize the connection between the 3.3 V power domain and the 1.2 V power domain safely. As shown in Fig. 8, the pre-amplifier consists of 4-stage amplifiers which are realized by a common source with resistor load amplifier. The first-stage amplifier is built by the IO transistor and operates with 2 V power supply, while the rest three-stage amplifiers are built by core device and operate at 1.2 V power supply. Two capacitors are connected in series between the adjacent stages. The waveforms in Fig. 9 show the maximum voltage of the input and output of the 1\(^{st}\) and 2\(^{nd}\) stage can achieve. It is worth noting that the maximum voltage that can couple to the input of 2\(^{nd}\) stage from the output of 1\(^{st}\) stage is 0.5 V, namely the maximum voltage of the 2\(^{nd}\) stage input is 1.2 V. So, the 2\(^{nd}\) stage can work...
3. Layout and simulation results

The proposed SAR ADC is designed in 1P7M 130-nm silicon-on-insulator (SOI) CMOS technology. The layout of the proposed SAR ADC is shown in Fig. 11. The core area is 0.72 mm²*0.9 mm. To verify the performance of the calibration circuit and to make the simulation results more realistic, some mismatches with a standard deviation of 0.03 were added to the MDAC by changing the capacitance of capacitors in the MDAC. The post-simulation results without and with the proposed calibration technique are shown in Fig. 12. The foreground calibration increases the peak signal-to-noise and distortion (SNDR) and spurious free dynamic range (SFDR) by 21.41 dB and 25.47 dB, respectively. The calibration circuit only requires an area of 0.015 mm².

![Fig. 11. Layout of the proposed ADC](image)

![Fig. 12. Simulation output spectrum with a 3.8 MS/s input (a) without calibration and (b) with calibration](image)

### Table IV. Comparison of recent high-resolution ADCs

|                        | [27] | [29] | [30] | This work* |
|------------------------|------|------|------|------------|
| Technology (nm)        | 180  | 180  | 40   | 130        |
| Supply (V)             | 3    | 3    | 1.8  | 3.3/1.2    |
| Sample rate (MS/s)     | 1    | 1    | 0.02 | 8          |
| Resolution             | 16   | 16   | 15   | 16         |
| SFDR (dB)              | 107.9| 94.33| 95.1 | 99.41      |
| SNDR (dB)              | 92.3 | 86.16| 74.12| 91.39      |
| Area (mm²)             | 5.61 | 2.52 | 0.315| 0.88       |
| Power (mW)             | 40   | 6.75 | 0.0017| 45         |
| FOM (pJ/step)          | 1.19 | 0.41 | 0.014| 0.18       |

*post-simulation results

The performance of the proposed ADC compared with other high-resolution designs in recent years is listed in Table IV.

4. Conclusion

In this study, a 16-bit 8-MS/s SAR ADC with a hybrid-charge-supply power structure is proposed and designed in 130-nm SOI CMOS technology. A nonbinary searching algorithm is used to speed up the conversion
rate. A foreground calibration technique is proposed to calibrate the mismatch of the capacitor DAC. In addition, to further reduce the power consumption and conversion time while maintaining a wide dynamic range, a hybrid-charge-supply power structure is implemented. According to the simulation results, the SNDR and SFDR of the proposed ADC can achieve 91.39 dB and 99.41 dB, respectively. In addition, the proposed SAR ADC consumes 45 mW when operating at an 8 MS/s sampling rate.

Acknowledgments

This work is supported by Research Foundation of Strategic Priority Research Program of Chinese Academy of Sciences (XDA18030100).

References

[1] Y. Chung, et al.: “A 102dB-SFDR 16-bit Calibration-Free SAR ADC in 180-nm CMOS,” IEEE A-PCAS (2019) 5 (DOI: 10.1109/A-PCAS.2019.8753163).
[2] C. Rhee, et al.: “8.4-to-16-bit resolution, 1-to-16 kHz bandwidth ADC with programmable-gain functionality for multi-sensor applications,” Electronics Letters 55 (2019) 982 (DOI: 10.1109/MWSCAS.2019.8884954).
[3] S. Li, et al.: “A 13-ENOB second-order noise-shaping SAR ADC realizing optimized NTF zeros using the error-feedback structure,” IEEE J. Solid-State Circuits 53 (2018) 3484 (DOI: 10.1109/JSSC.2018.2871081).
[4] A. Bannor, et al.: “An 18 b 5 MS/s SAR ADC with 100.2 dB dynamic range,” IEEE Symp. VLSI Circuits Dig. Tech. Papers (2014) 33 (DOI: 10.1109/VLSIC.2014.6858371).
[5] D. Hummerston, et al.: “An 18-bit 2MS/s pipelined SAR ADC utilizing a sampling distortion cancellation circuit with -107 dB THD at 100 kHz,” IEEE Symp. VLSI Circuits Dig. Tech. Papers (2017) 280 (DOI: 10.2939/VLSIC.2017.8000508).
[6] M. Ding, et al.: “A 46 pW 13 b 6.4 MS/s SAR ADC with background mismatch and offset calibration,” IEEE J. Solid-State Circuits 52 (2017) 423 (DOI: 10.1109/JSSC.2016.2609949).
[7] M. Maddox, et al.: “A 16 bit linear passive-charge-sharing SAR ADC in 55nm CMOS,” IEEE A-SSCC Dig. Tech. Papers (2016) 153 (DOI: 10.1109/A-SSCC.2016.7844158).
[8] C.P. Hurrell, et al.: “An 18 b 12.5 MS/s ADC With 93 dB SNR,” IEEE J. of Solid-State Circuits 45 (2010) 2647 (DOI: 10.1109/JSSC.2010.2075310).
[9] Y. Chi, et al.: “A 16-bit 1MS/s 44mW successive approximation register analog-to-digital converter achieving signal-to-noise-and-distortion-ratio of 94.3dB,” IEEE EDSSC (2013) 1 (DOI: 10.1109/EDSSC.2013.6628134).
[10] X. Huang, et al.: “A 16-bit, 250ksp/s successive approximation register ADC based on the charge-redistribution technique,” IEEE EDSSC (2011) 1 (DOI: 10.1109/EDSSC.2011.617627).
[11] C.C. Liu, et al.: “A 10 bit 320 MS/s Low-Cost SAR ADC for IEEE 802.11ac Applications in 20 nm CMOS,” IEEE J. of Solid-State Circuits 50 (2015) 2645 (DOI: 10.1109/JSSC.2015.2466475).
[12] J.H. Tsai, et al.: “A 0.003 mm2 10 b 240 MS/s 0.7 mW SAR ADC in 28 nm CMOS With Digital Error Correction and Correlated-Reversed Switching,” IEEE J. of Solid-State Circuits 50 (2015) 1382 (DOI: 10.1109/JSSC.2015.2413850).
[13] D. Zhang, et al.: “Analysis and Calibration of Nonbinary-Weighted Capacitive DAC for High-Resolution SAR ADCs,” IEEE Transactions on Circuits and Systems 61 (2014) 666 (DOI: 10.1109/TCSII.2014.2331111).
[14] C.-Y. Liou, et al.: “A 2.4-to-5.2 Gs/s SAR ADC with charge-average switching DAC in 90 nm CMOS,” IEEE ISSCC Dig. Tech. Papers (2013) 280 (DOI: 10.1109/ISSCC.2013.6487735).
[15] S. Thirunakkarasu, et al.: “Built-in self-calibration and digital-trim technique for 14-Bit SAR ADCs achieving ±1 LSB INL,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems 23 (2015) 916 (DOI: 10.1109/TVLSI.2014.2321761).
[16] J. McNeill, et al.: “Split ADC: architecture for deterministic digital background calibration of a 16-bit 1-MS/s ADC,” IEEE J. Solid-State Circuits 40 (2005) 2437 (DOI: 10.1109/JSSC.2005.856291).
[17] K. Obata, et al.: “A 97.99 dB SNDR, 2 kHz BW, 37.1 μW noise-shaping SAR ADC with dynamic element matching and modulation dither effect,” IEEE Symposium on VLSI Circuits (2016) 1 (DOI: 10.1109/VLSIC.2016.7573463).
[18] M. Zeloufi, et al.: “A 12 bit 40 MS/s SAR ADC with a redundancy algorithm and digital calibration for the ATLAS LAr calorimeter readout,” Journal of Instrumentation 11 (2016) C01030 (DOI: 10.1088/1748-0221/11/01/C01030).
[19] D. Xu, et al.: “A 10-bit 1.2 Gs/s 45 mW time-interleaved SAR ADC with background calibration,” IEICE Electron. Express 15 (2018) 20171235 (DOI: 10.1587/elex.15.20171235).
[20] X. Zhu, et al.: “A 6 mW 325 MS/s 8 bit SAR ADC with background offset calibration,” IEICE Electron. Express 14 (2017) 20170329 (DOI: 10.1587/elex.14.20170329).
[21] W. Liu, et al.: “A 12-bit, 45-MS/s, 3-mW Redundant Successive-Approximation-Register Analog-to-Digital Converter With Digital Calibration,” IEEE J. of Solid-State Circuits 46 (2011) 2661 (DOI: 10.1109/JSSC.2011.2163556).
[22] S. Choi, et al.: “An 84.6-dB-SNR and 98.2-dB-SFDR residue-integrated SAR ADC for low-power sensor applications,” IEEE J. Solid-State Circuits 53 (2018) 404 (DOI: 10.1109/JSSC.2017.2774287).
[23] T. Ito, et al.: “A 40-kS/s 16-bit non-binary SAR ADC in 0.18 μm CMOS with noise-tunable comparator,” IEEE International Conference on Electronics, Circuits and Systems, Papers (2017) 1 (DOI: 10.1109/ICECS.2017.8292000).
[24] B. Razavi, et al.: “Design techniques for high-speed, high-resolution comparators,” IEEE J. Solid-State Circuits 27 (1992) 1916 (DOI: 10.1109/68.173122).
[25] L. Qiu, et al.: “A flexible-weighted non binary searching technique for high-speed SAR-ADCs,” IEEE Trans. on Very Large Scale Integration (VLSI) Systems, 24 (2016) 2808 (DOI: 10.1109/TVLSI.2016.2532605).
[26] T. Vaibhav, et al.: “Mismatch Characterization of Small Metal Fringe Capacitors,” IEEE Trans. Circuits Syst. I, 61 (2014) 2236 (DOI: 10.1109/TCSI.2014.2332264).
[27] P. Zhang, et al.: “A 16-Bit 1-MS/s Pseudo-Differential SAR ADC With Digital Calibration and DNL Enhancement Achieving 92 dB SNDR,” IEEE Access 7 (2019) 119166 (DOI: 10.1109/ACCESS.2019.2937384).
[28] L. Qiu, et al.: “A 10-bit 300 MS/s 5.8 mW SAR ADC With Two-Stage Interpolation for PET Imaging,” IEEE Sensor Journal 18 (2018) 2006 (DOI: 10.1109/JSEN.2018.2790581).
[29] H. Li, et al.: “16-bit 1-MS/s SAR ADC with foreground digital-domain calibration,” IEEE ISSCC Dig. Tech. Papers (2017) 242 (DOI: 10.1109/ISSCC.2018.8310274).
[30] S. Misseob, et al.: “Edge-pursuit comparator: an energy scalable oscillator collapse-based comparator with application in a 74.1 dB SNDR and 20 kS/s 15 b SAR ADC,” IEEE J. Solid-State Circuits 52 (2017) 1077 (DOI: 10.1109/JSSC.2016.2631299).