Research on the Application of Big Data Ecology in College Physical Education and Training

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Abstract: As the demand for lightweight products in electronic products continues to increase, the demand for increased integration of products is becoming more and more urgent. Systematic package SiP refers to a package module system that combines multiple active electronic components with passive components to achieve a certain function. Through the effective packaging technology, the mechanical properties and thermal properties of the chip are greatly improved. According to the specific connection mode of the chip and the substrate, the packaging process can be mainly divided into wire bonding package and flip chip soldering, and 75% to 80% of the product package types are wire bonding packages. Although wire bonding packages have cost and reliability advantages, they still have I/O problems for IC packages, and wire bonding tools are still evolving. Flip-chip soldering has a shorter interconnect line, which results in a higher density of chip mounting. At the same time, the tools in these two technologies are constantly being updated, which makes the integration of chips more and more high.

1. Introduction

As product integration becomes more and more high, users are increasingly demanding the compactness and convenience of electronic products. With the continuous development of integrated circuit packaging technology and the gradual improvement of component performance, the overall effect of the product will inevitably be greatly improved. Under the trend of the encapsulation technology of integrated circuits, technology can be divided into two major trends, one is system single-chip SoC, and the other is system-packaged SiP. The quality of the packaging technology directly affects the mechanical properties and thermal properties of the final chip, and ultimately becomes the key to the success of the system.

The packaging technology implements three basic functions: protection, interconnection, and cooling. The protection function refers to the packaging technology of the integrated circuit, including SoC and SiP technology, which can effectively protect the chip from the external environment. The interconnection function is in the process of supplying power from the power supply to the chip. Through the power supply process from the power supply to the chip, various signals between the systems can be interconnected in time. The final heat dissipation function means that the chip can dissipate the heat generated by the chip to the outside world, thereby improving the performance of the chip during use. Therefore, packaging technology is crucial to the development of products. Reasonable packaging technology can greatly improve the performance of the product, and will also make the user experience more comfortable.

In recent years, the development trend of SIP has become more diversified, complicated and intensive. The complexity refers to the increasing integration of SiP in the development process, the
more types of components are integrated, and the performance is more and more complicated. The corresponding functions that can be achieved are also becoming more comprehensive. At the same time, for the packaging technology, copper pillars are now used instead of the original solder balls, so that the ball pitch is getting smaller and smaller. With the advancement and maturity of technology, the cost of forming boards is also decreasing. In 2013, the global SiP production value was 4,310 million US dollars. By 2016 alone, the global SiP production value has risen to 6,944 million US dollars, and has been gradually increasing.

2. System single-chip SoC and systemized package SiP

Systematic package SiP refers to a single standard package that combines a number of different functional active electronic components with freely selectable passive components to achieve a certain function, ultimately forming a system or subsystem.

The system single-chip SoC is similar to the system-packaged SiP, and both integrate a system containing logic components, memory components, and passive components into one unit. SoC is designed from the perspective of integrating the components required by the system on a single chip. SIP is a combination of packaging methods that side-by-side or superimposed different chips from the standpoint of packaging.

The differences in composition, material, size, development cycle, and development direction of SoC and SiP are shown in Table 1:

Table 1. Specific methods in each step of data cleaning

|          | SoC                        | SiP                        |
|----------|----------------------------|----------------------------|
| A chip is a system | Integrated system of each chip and passive devices |
| Limited by materials and different processes | Assemble on the substrate |
| Higher density, A high speed | Components that can be integrated with various processes, such as rf devices |
| Die size is larger | Complex test |
| High development costs | Lower development costs |
| Long development cycle and low yield | Shorter development cycle, higher yield |
| Moore’s law | Beyond Moore’s law |

The specific reasons for the selection of SiP can be clearly seen from Table 1. Considering the degree of integration of the circuit, the degree of integration of SiP is relatively high. It can be said that SiP is a combination of system single-chip SoC and DDR. In addition, with the continuous emergence of SoC in the development process, various obstacles at the technical level have made SiP more and more important in the process of using.

3. SiP process analysis

The integrated circuit system-level packaging process SiP requires assembly and interconnection between components on the substrate, and the pre- and post-installation sequence between components must be required. There are various details in the SiP packaging process to install different packaging fabrication processes, but the various parts of the process that are generally required for these methods are shown in Figure 2.
Figure 1. Packaging Process Flow Chart

It can be seen from Fig. 1 that the flow chart of the SiP package is roughly divided into 20 steps. In addition, according to the specific connection mode of the chip and the substrate, the packaging process can be mainly divided into two types: wire bonding package and flip chip bonding.

3.1 Wire bonding packaging process
The wire bonding packaging process performs some screening on the basis of the process in Fig. 1, and the main process steps are as follows:

Wafer→wafer thinning→wafer cutting→chip bonding→wire bonding→plasma cleaning→liquid encapsulant potting→assembly solder ball→reflow soldering→surface marking→separation→final inspection→test→packaging.

• Thin film thinning

The specific degree of thinning of the wafer in the wafer thinning process is mainly considered from two aspects. On the one hand, if the thickness of the wafer is too thin, in the later series of processing, the deformation, cracking, etc. of the wafer will inevitably occur, the mechanical strength
is greatly reduced, and the success rate in the production process is greatly increased. The impact will also increase production costs. On the other hand, if the wafer is only from the perspective of ensuring the quality of its production, the thickness of the wafer is too thick, and the overall quality of the final product is too heavy, which is related to the thinning and simple promotion advocated in the product renewal. Contradictions. Therefore, it is very important to select the wafer thickness of the most suitable product in order to carry out the thinning process of the wafer from the whole before packaging. The manufacturing process commonly used in wafer thinning is to thin the wafer to the desired thickness by mechanical grinding.

**Disc cutting**

The next step after the wafer is thinned after the wafer is cut is to achieve effective dicing of the thinned wafer. There are two main ways of dicing, including traditional dicing methods and automated dicing methods. Most of the traditional dicing methods are done by manual manual operation. However, in the context of the development of industrial processes, in the actual wafer cutting process, most of them use automated tools such as saw blades to complete this process. The edge of the wafer obtained after automated cutting is more regular than the conventional dicing method.

**Chip bonding**

In the bonding process of the chip, it is necessary to reasonably consider the size of the chip and the size of the pad. The size of the chip that has been cut cannot be changed, but the size of the pad can be reasonably selected. If the pad is too small, the chip may be squeezed during the bonding process, resulting in a poor final bond. Conversely, if the pad is too large, the chips need to be interconnected by wires during the bonding process. If the pad is too large, the lead will be too large, and the lead may be bent or damaged, which is different from the expected effect. In addition, after selecting a reasonable pad, it is necessary to solder the chip to the substrate with various materials such as soft solder and Au-Si eutectic alloy.

**Plasma cleaning**

Through the chip after the above operation, it is also necessary to continue to increase the adhesion of the film. Only the adhesion of the membrane continues to increase, and the overall performance of the system can continue to be improved. Now, an effective measure to improve film adhesion is plasma cleaning technology. At the same time, the substrate treated by the plasma treatment technology needs to be cleaned in the next step to remove the adverse effects left by the plasma treatment. The surface of the substrate treated by the plasma technology produces a fluoride-containing gray material which can be removed by washing with a solution. The surface of the substrate after the plasma cleaning technique has good wettability and adhesion.

**Liquid sealant potting**

The technique commonly used in liquid encapsulant encapsulation is the "tin paste" + "tin ball" ball placement method. This method is mainly divided into two parts. The first is to print the solder paste onto the pad to be operated. Then in the second step, you need to use the solder ball. You need to add the solder ball to the pad after the solder paste is finished. Because the solder ball is extremely easy to drop on the pad, it needs to be fixed with solder paste, and when heated, the solder ball is heated faster and more uniformly with the help of the solder paste. Another way to encapsulate liquid sealants is “welding paste” + “tin balls”.

**Surface marking**

As the name suggests, surface marking is to mark the module's package module with the characteristics of the module. These tags are used to indicate the location of the module, the code number of each device, and so on. These tags facilitate tracking and feedback during use, as well as for later device rework.

### 3.2 Flip chip bonding process

The process of flip-chip bonding is:
wafer → pad redistribution → wafer thinning, bump formation → wafer cutting → flip-bond bonding, underfill → encapsulation → assembly solder ball → reflow soldering → surface marking → Separation → Final inspection → Test → Packaging.

- Pad redistribution

  This step was introduced to address the need for lead pitch in the flip chip process. In order to increase the pitch of the leads, only adjusting the individual leads may not be completed, so that the overall redistribution adjustment of the pads is required.

- Making bumps

  On the pad after the pad redistribution process, it is also necessary to add bumps to it. The techniques for making bumps mainly include the following: (1) Bump production using a high melting point. This step is usually done using a metal with a higher melting point, such as a metal such as gold or copper. (2) The fabrication of bumps is done by solder. It mainly includes a variety of methods such as the use of traditional tin shots and the commonly used spray method. (3) Hybrid bump fabrication refers to the technique of combining high-melting-point bump fabrication with solder bump technology. In the specific application process, it is necessary to add a layer of solder to the high melting point metal. Through this operation, the reliability of bump production can be effectively guaranteed.

  Through the modification of the packaging process, the flip-chip bonding process has many advantages not found in the wire bonding process. First of all, the problem of the pad center distance limit in the wire bonding packaging process is solved by the flip chip bonding process. Secondly, the flip-chip soldering process has more advantages in the distribution of the power supply and the ground than the wire bonding packaging process, which can bring convenience to the designer. Finally, the performance of all aspects of the flip-chip soldering process is also high, and the heat dissipation is also good, which in turn makes the product performance stable and reliable.

4. Advantages of SiP

The SiP packaging technology enables multiple chips to be packaged together, and the variety of chips is increasing, and the overall size of the chip is continuously reduced, thereby greatly improving the overall packaging efficiency. The nature of SiP that can aggregate multiple materials also means that SiP is more compatible. At the same time, SiP reduces the layout-level routing steps in the design process compared to the SoC, which greatly reduces the time taken for the design as a whole. The reduction in design time also means that the time and cost involved are less, that is, the production system cost of the product is reduced, making the final product more competitive in the market. The application field of SiP package is also very extensive, not only dealing with digital systems, but also for communication systems, sensor systems and other fields.

  At the same time, the packaging industry chain is also constantly upgrading and improving, from the traditional single-line production process to the current multiple departments and multiple links to help each other. As shown in Figure 2, the terminal manufacturer can also directly contact the packaging and testing plant, making the entire processing and production environment more advantageous.
5. Conclusion
Through the analysis and research of system-in-package SiP, it can be clearly seen that SiP will represent the final development direction of the chip industry. System-in-package SiP has great advantages in the production process of the product due to its low power consumption and low cost. At the same time, SiP is constantly upgrading and transforming towards a more market-oriented direction. The application technology in each part of the SiP is also undergoing technical updates, and is continuously improving towards more stable and reliable standards.

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