A System-on-Chip for Series Arc Fault Acquisition in Smart Grid Based on two Configurable Sampling Rate SAR ADCs

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Abstract Arc faults in power systems may cause significant damage to equipment and even lead to electrical fires and hazard for personnel if they are not detected and isolated promptly. The series arc fault in a distribution system can be more dangerous compared to the parallel arc fault, because its low fault current will hinder the circuit breakers from responding in a timely manner. Therefore, it is necessary to properly detect the series arc fault. In this paper, a system-on-chip (SoC) for series AC arc fault acquisition is presented, which is based on two channels of configurable sampling rate successive approximation register (SAR) analog-to-digital-converters (ADCs). As the arc faults with different loads have different characteristics and may need a higher sampling rate under some circumstances, the adjustable sampling rate can meet varying needs. The system is implemented using a 55 nm CMOS process with a die area of 4.683 mm\(^2\) and power dissipation of 75.9 mW. The proposed SAR ADC design can achieve a good Schreier figure-of-merit (FoM) of 161 dB at 1 MS/s sampling rate. With this ADC design, the SoC can complete arc faults acquisition with high precision and configurable sampling rate at a low cost. Meanwhile, the system can sample voltage and current signals from the smart grid respectively to initially locate the arc fault.

key words: Smart grid, arc fault acquisition, SoC, SAR ADC, sampling rate, switching scheme

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Arc faults can occur in the presence of a long time overload operation state, wire connection damage or improper operation of equipment in the distribution system [1]. An arc fault may release strong light and huge energy, which will seriously impact the stable operation of the power system, and even cause electrical fires, casualties and huge property losses [2, 3, 4]. Therefore, achieving rapid detection of arc fault and timely disconnection of the line plays an extremely important role in the distribution system.

An arc fault can be divided into parallel arc fault and series arc fault. The former is usually caused by the short-circuit fault in the path. When the fault occurs, it will produce a large current and, therefore, these arcs can be detected and protected by the general circuit breaker [5]. The common cause of series arc faults is mainly loose connectors or terminals. The series arcs will increase the equivalent resistance of the load that means a decrease in the current flowing through the circuit. As a result, the circuit breaker cannot effectively detect this kind of arc faults [6, 7].

When arc faults arise, the spectrum of the arc can be taken advantage of to distinguish arc properties compared to luminescence, exothermic and odor phenomena [8]. Therefore, various methods using digital signal processing schemes, such as Discrete Fourier Transform (DFT) and Discrete Wavelet Transform (DWT), are developed to detect the arc fault, different arc fault detection schemes have been proposed based on the signatures of arc signals\cite{5, 7, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19}. Almost all of these schemes are based on software algorithms and are combined with microcontroller unit (MCU) or hosts. There has been a limited discussion on the experimental acquisition of arc signals. Meanwhile, development of smart grid and very large-scale integrated circuits (VLSI) make it important to design a low cost and effective power system-on-chip (SoC) for arc fault detection. A smart SoC for arc-fault detection called ZNRG2061 is offered by Integrated Device Technology, Inc. (IDT) in 2017 \cite{20}. The SoC is used to detect photovoltaic (PV) DC arc fault in solar power systems. Its trainable algorithm continuously monitors the photovoltaic DC current by the acquisition circuit on chip and observes any current fluctuation, ultimately performing a Fast Fourier Transform (FFT) analysis. However, it is not adaptable for detecting AC arc fault in the distribution system and can not locate the arc fault. Meanwhile, the FFT algorithms can not deal with non-stationary signal and acquire time domain and frequency domain information simultaneously, and wavelet analysis can produce more easily recognized detection results than the traditional Fourier transform approach \cite{21}. Due to the complexity of grid environment, both high-frequency and low-frequency current signals should be considered when designing the arc detection circuits \cite{3}. Consequently, the sampling circuit analog-to-digital converter (ADC) should be designed to be reconfigurable with flexible speed and power to meet multiple requirements \cite{22}. Therefore, this study focuses...
on designing a SoC dedicated for series AC arc faults acquisition with configurable sampling circuits, the ability of locating the arc fault and on-chip DWT algorithm to obtain the time domain and frequency domain information simultaneously.

The successive approximation register (SAR) ADC has low power consumption and a highly digital nature [23]. Therefore, integration of a SAR ADC in the SoC design for arc signal acquisition is a very attractive solution. In this paper, we present a SoC based on two channels of configurable sampling rate SAR ADCs. The proposed system can acquire voltage and current arc signals simultaneously from a power system to initially locate the arc fault. The arc faults characterized by different features due to different loads can be effectively acquired, benefiting from the configurable sampling rate of the arc fault acquisition circuit. Furthermore, both high frequency and low frequency signals can be dealt with to detect the occurrence of an arc in the grid.

The remainder of this brief is organized as follows. Section II presents the architecture of the proposed arc acquisition SoC. Section III describes the design of the front-end acquisition circuit on chip. The implementation and system-level experimental results are provided in Section IV. The paper is concluded in Section V.

2. System Framework

The presented SoC is based on a 32-bit Xuantie-803 (or CK803) CPU featured with low cost and low power dissipation from Alibaba T-Head division [24]. The advanced microcontroller bus architecture (AMBA) introduced by ARM Ltd is widely used as the on-chip bus system in SoC designs. The advanced high performance bus (AHB) and advanced peripheral bus (APB) two-level bus interconnection structure rather than the advanced extensible interface (AXI) bus architecture is adopted to meet the low power requirements. The operating clock frequency is up to 125 MHz, that can be generated by the all-digital phase locked loop (ADPLL) on chip. Figure 1 shows the system architecture.

![Fig. 1. Architecture of the proposed system](image)

The on-chip memory includes two 32 KB SRAMs and a 128 KB Flash. An application program can be directly downloaded into one of the two SRAMs through the JTAG debugger, and the other SRAM and Flash can be used to store application data. Once the SoC has been powered off, the program needs to be rewritten through the JTAG interface when the system is powered on again. Application programs can also be written to the on-chip Flash in a binary form through the JTAG debugger, which is for the normal usage. This approach does not require any reprogramming. The system also includes a few general peripheral components such as UART and SPI, which can be used to communicate with computers or other communication devices.

The SoC integrates many important analog intellectual-properties (IPs). The low-dropout voltage regulators (LDOs) consist of several parallel LDOs for powering the analog and digital parts with different voltage domains. The integrated temperature sensor is connected to the sigma-delta ADC, and is used to monitor the temperature variation of the chip when it is functioning. The ADPLL and clock dividers provide the main clock of this system and the working clocks of different modules. The two SAR ADC components form the core module for series arc faults acquisition.

3. On-Chip Front-end Acquisition Circuit Design

3.1 Front-End Acquisition Circuit Architecture

With different loads, two situations can occur: 1) Either the arc faults may lead to the shoulder phenomenon (zero values of the current), 2) or a few current pulses in the time domain will need a high sampling rate. Therefore, it is necessary for the sampling frequency to be adjustable in different situations. For example, in the former situation, there is no need for a very high sampling rate. Thus, it can be implemented with low power consumption by decreasing the sampling rate. While in the second situation, a high sampling rate is necessary for detecting the arc signals effectively. Meanwhile, due to the grid complexity, both high frequency and low frequency signals need to be dealt with.

The front-end acquisition circuit architecture on chip is shown in Fig. 2. The instrument amplifiers (IAs) are necessary in the presence of a weak signal. A clock divider assisted with on-chip ADPLL can implement configurable sampling rate for these two ADCs. Based on the flexible sampling frequency, the power is relatively flexible. The sampling rate can be set by configuring the registers through the AHB slave bus. The two ADCs can either sample signals simultaneously or separately, which can be controlled by the enable signal of the two ADCs. The sampled data will be transmitted to the AHB master bus. Then the data can be stored in the SRAM and processed by the arc fault detection algorithm that uses the DWT [25] on chip to rapidly detect arc faults and respond in time. Voltage and current signals from the power grid are sampled by the two channels of SAR ADC respectively. The arc fault can be initially located by observing any abnormal phenomena in the voltage and current signals. If an abnormal phenomenon is observed only in the
current field, the arc fault is located inside the load. If this phenomenon is observed in both voltage and current fields, the arc fault is located outside the load.

Fig. 2. Architecture design of the front-end acquisition circuit on chip

3.2 Configurable SAR ADC Implementation

The designed SAR ADC adopts synchronous sampling architecture in order to meet the requirement of adjustable sampling rate. The width of the sampling phase is extendible to ensure a correctly sampled value and fine tuning of the sampling rate. A reference voltage of 2.5 V is used to ensure sufficient range for sampling the arc signals. Several techniques are exploited in this design to improve the power, speed, area and precision efficiency. Top-plate-sampling structure [26] is used to significantly reduce the switching power consumption during the conversion process. With the top-plate-sampling operation, the total number of unit capacitance can be reduced to half compared to that with the original bottom-plate-sampling operation. A four-segment capacitor array structure with coupling capacitors is used in the design in order to further reduce the number of unit capacitors in the capacitor digital-to-analog (CDAC) array and decrease the difficulty of layout routing. The integration of ADC into the system can be accelerated and the takeout time can be further shortened based on the simplified capacitor array structure. The redundancy technique without using any redundant capacitors can not only provide a wide error tolerance range but also avoid the need to consider overflow by the design of the digital error correction (DEC) [27]. In addition, a DAC switching technique known as capacitor swapping [28] in the last three arrays and the dynamic element matching (DEM) [29] technique in most significant bit (MSB) array are used to suppress the non-linearity due to capacitor mismatch. The Schreier figure-of-merit (FoM) ($FoM_S$) [30] is defined as

$$FoM_S = SNDR + 10 \log \left( \frac{F_S}{2 \times Power} \right)$$ (1)

Where $F_S$ is the sampling rate. Adopting all aforementioned techniques, this design reports a FoM of 161 dB and an area of 0.13 mm² without any calibration in place.

The proposed segmented split capacitor and capacitor swapping with addition-only DEC (SSCCS-ADEC) differential SAR ADC architecture is shown in Fig. 3. The original MSB capacitor of each segment in the CDAC structure is split into two sub-capacitors with a ratio of seven to one. The splitting design can tolerate dynamic errors, and reduce the variation range of the input common-mode voltage of the comparator, thereby reducing the comparator design difficulty. The comparator in this ADC architecture adopts three stages of pre-amplifiers and a latch. With this structure, the bandwidth and gain can be balanced effectively. Figure 4 shows the DEC arithmetic table that converts raw 20 bit output codes to error-corrected 16 bit codes, based on the splitting structure of the capacitor array. Although the d0, d4, d8 and d12 bit weight columns in Fig. 4 contain three “1”’s, a full adder (FA) can be used here because they are the last bit in their segment without carry. The hardware for DEC is thus simple to implement and only 12 FAs are needed in this design, as shown in Fig. 3.

Fig. 3. The proposed differential SAR ADC with the SSCCS-ADEC technique

Fig. 4. DEC arithmetic table

The weight of MSB array is increased to eight in order to decrease the requirement of capacitor mismatch in this segmented CDAC structure, as shown in Fig. 3. Meanwhile, the
temperature code and DEM technique [29] are adopted in the MSB array to further reduce the influence of the capacitor mismatch ratio. The capacitor swapping [28] technique is used in the second significant bit (SSB) array, third significant bit (TSB) array and last significant bit (LSB) array of the CDAC structure instead of the DEM technique in order to reduce the difficulty of routing. Figure 5 illustrates the operations in the first two bit-cycles of the SSB array in the CDAC structure. Based on the aforementioned splitting design, each MSB capacitor in the last three segments such as C1-a in Fig. 5 is equal to the sum of C2, C3 and C4. The principle behind capacitor swapping is to average the error by reusing the prior switched capacitors. Therefore, C1-a in the SSB array is split into C1-a1, C1-a2 and C1-a3, and C1-a1 = C2, C1-a2 = C3, C1-a3 = C4 (TSB and LSB arrays are the same). As Fig. 5 shows, the bottom plates of C1-a (equals C1-a1, C1-a2 and C1-a3) on the lower voltage potential side is switched to VDD after B1 is decided. During the second bit-cycle, if B2 = B1, C2 is switched as shown in the left part of the third comparison. When B2 ≠ B1, as C1-a1 and C2 can transfer the same amount of charge, C1-a1 is switched but C2 is not switched. Similarly, C2, C3 and C4 can be swapped with the previously switched capacitors decomposed by the MSB capacitor.

4. System-Level experimental results

The proposed SoC for series AC arc faults acquisition is implemented and fabricated using a 55 nm CMOS technology.
this system could acquire arc signals with a flexible sampling rate at a low cost. The proposed ADC design was energy- and area-efficient with a configurable sampling rate.

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