Abstract—Recent advancements in deep learning have led to the widespread adoption of artificial intelligence (AI) in applications such as computer vision and natural language processing. As neural networks become deeper and larger, AI modeling demands outstrip the capabilities of conventional chip architectures. Memory bandwidth falls behind processing power. Energy consumption comes to dominate the total cost of ownership. Currently, memory capacity is insufficient to support the most advanced NLP models. In this work, we present a 3D AI chip, called Sunrise, with near-memory computing architecture to address these three challenges. This distributed, near-memory computing architecture allows us to tear down the performance-limiting memory wall with an abundance of data bandwidth. We achieve the same level of energy efficiency on 40nm technology as competing chips on 7nm technology. By moving to similar technologies as other AI chips, we project to achieve more than ten times the performance of the current state-of-the-art chips, and twenty times of memory capacity as compared with the best chip in each benchmark.

Index Terms—Artificial intelligence, heterogeneous integration, near-memory computing, system-on-chip

I. INTRODUCTION

AI is now used widely in a diverse set of tasks, ranging from face recognition to real-time speech processing to autonomous transportation. Among these applications, deep neural networks have been responsible for the most recent AI breakthroughs, like DeepMinds AlphaGos stunning defeat of the Go world champion. Google has developed a high-quality deep neural machine translation system between 17 languages [4]. Since then, natural language processing models have only grown more powerful and are now capable of programming, writing stories, and even composing poems. These powerful AI models require deeper and larger nets. In 2019, Nvidia published natural language model Megatron with 8.5 billion parameters. This year, Microsoft introduced the next generation Turing-NLG with 17 billion parameters. Recently, OpenAI released an even larger model and current state-of-the-art, GTP-3 [24]. With 174 billion parameters, GPT-3 takes 350GB memory and $12 million to train [25].

It is clear that newer AI models require more parameters, more memory, and larger training sets. They will only continue to grow in size and training cost. To address these future demands, we propose a new architecture for AI chip. In this paper, we discuss two key components of this new architecture: heterogenous chip integration technology and single-form memory.

Our results demonstrate the potential of this new architecture. This chip, fabricated on a 40nm process, achieves performances comparable with current-state-of-the-art chips, which use generations more advanced fabrication processes than the 40nm. We further extrapolate the performances of our chip to current fabrication processes. Our chip is projected to be able to hold 12 billion parameters on a single chip, while current best on the market only holds 8 billion on a whole wafer.

II. BACKGROUND

Neural networks consist of layers of nodes and the connections between them. Each node stores a value. During inference, the first layer contains the input values. The values of the nodes in subsequent layers are calculated from the values in the previous layer’s nodes. The last layer is the output of the neural network. Figure [1] shows connections...
between two layers. A neural neural network may be deep (i.e. a large number of layers). It may also be wide—each layer may have large number of nodes. Large amounts of computing power and training data are generally regarded as the drivers of modern breakthroughs in artificial intelligence. To sustain the momentum in the field, we need to address the three challenges for AI chips: the memory wall, energy efficiency, and on-chip memory capacity.

Computational power has increased 60% every year since the 80’s, as IC fabrication technology advances with Moores law. Yet memory performance, namely DRAM, has increased only 7% every year during the same time [5] [6]. The gap between processor and memory speed has been widening for more than two decades. As a result, data bandwidth cannot match the processing speed. This is the well-known memory wall. The memory wall has been a challenge for CPUs for decades. As AI computations consume much more data than most other applications, the memory wall is especially relevant in AI chip design.

There are two main existing approaches to addressing the memory wall problem. One is increasing the data transfer clock rate. The other is widening transfer data width. The first approach appears in high-bandwidth memory, such as high-performance DDR memory and HBM memory. Currently, the peak performance of such memory is around 256GB/s [26]. An example of the second approach is in Interposer, where the number of connections is in the 1000s [9].

The second challenge for AI chips is power consumption. Training an AI model emits more than five times the lifetime emissions of an average car [11]. Generally, power consumption comes mainly from computing units or data transfer units. AI chips must handle not only computationally intensive but also data transfer-intensive tasks. In addition to algorithm optimization, common approaches to reducing power consumption include using more advanced IC fabrication technology and reducing capacitance load on data transfer paths. To lower the power consumption of data transfer between DRAM [9] and AI chips, high-bandwidth memory (HBM) [10] and package substrate routing, like Interposer, are used. Yet even with these advanced technologies, data transfer power consumption is still over 0.5mW/Gbps. [16]

The third challenge for AI chips is fast memory capacity [13]. Fast memory is referred to as on-chip or near-chip memory, which provides data quickly without throttling the processing units. Fast memory is generally in the form of on-chip SRAM. SRAM has the advantage of fast access time, but its size limits memory capacity. As AI is applied to more complex problems, the number of parameters of neural network models grows exponentially. The largest NLP model to date has 170 billion parameters. It is crucial to keep as much parameters as possible in fast memory to avoid performance degradation. Currently, no AI chip can hold that many parameters. Most AI chips on the market typically have a memory capacity of just 50 MB, which leaves a large gap between current memory capabilities and memory demands. The insufficiency of fast memory capacity will only continue to get worse if nothing is done to address this problem.

The main goal of our approach is to overcome memory bandwidth limitations, to reduce power, and increase memory capacity. We achieve this by optimizing integration, architecture, and memory choice. The component technologies for our Sunrise chip include Heterogeneous Integration Technology on Chip (HITOC), single form memory (UNIMEM), and architecture specifically optimized for HITOC and UNIMEM.

III. HITOC

All AI chips are currently fabricated on a single wafer. Sunrise chip is partitioned into separately fabricated logic and memory wafers. These two wafers are bonded face-to-face with a hybrid bonding process [7] [14] using Cu damascene-patterned surfaces, as shown in Figure 2. External IOs are brought out to the backside of CMOS wafer with TSV (Through-Silicon Via) for bonding. Circuits on different wafers operate together and communicated through wires running between two wafers. We call this approach Heterogeneous Integration Technology on Chip (HITOC).

By fabricating logic and memory wafers separately, both the logic process and memory process are optimized indepen-
In the logic process, the transistor threshold voltage is low, and the number of metal layers is large. The opposite is true in the memory process. The physical structure of basic elements in the logic process and the memory process differ. Integrating logic and memory processes thus results in a design that favors one over the other, so we choose to separate the two. Furthermore, with logic and memory on separate wafers, there are more compute elements and memory elements in the same area when compared to a single wafer. By separating logic and memory, we achieve better electrical characteristics and overall chip characteristics as well as higher computational performance and memory capacity. HITOC is one form of 3D IC. There are other forms of 3D IC that are widely used. One is Interposer. Interposer is to connect two chips through metal lines on the substrate, as in Figure 3. Interposer connections are much denser compared to connections between different package of chips or bonding wire connections between chips in the same package.

Another approach is Through-Silicon Via. TSV is a direct vertical connection between different levels of a chip. It consists of a conducting via which passes through the silicon substrate and connects the two sides of the wafer [Fig. 4]. Typically, the interplane via is etched and filled with metal, such as tungsten (W) or copper (Cu). Connections between chips with are denser compared to Interposer connections between different package of chips or bonding wire connections between chips in the same package.

In that table, we conservatively assume the clock frequencies for data transfer are the same for comparison purposes. But clock frequency runs faster at HITOC and TSV. Data paths are shorter in HITOC than in Interposer and TSV. Shorter data paths have smaller capacitance loading. As a result, power consumption is only 0.02pJ/b for HITOC while 2.17 pJ/b and 0.55 pJ/b for Interposer and TSV respectively. With smaller capacitance loading, data transfer runs at higher frequency, and power consumption is lower.

With shorter and denser connection, HITOC delivers, among the three approaches, higher data transfer rate and lower power consumption.

**IV. UNIMEM: A SINGLE MEMORY SOLUTION**

To simplify the system and circumvent the need for conventional CPU-cache-memory architecture, Sunrise chip uses only the DRAM without SRAM cache. We call this approach UniMem, as we use only a single form of memory for the whole chip. We choose to use DRAM over SRAM, since DRAM has a higher density with a cell size of 6-12 \( F^2 \) compared to SRAMs cell size of 140 \( F^2 \). However, DRAM has a read/write latency that is around 50-90 times slower than SRAMs.

To counteract DRAMs slow latency, multiple localized DRAM units are pooled together to supply data to logic units. Memory access load is shared amongst DRAM arrays in the pool.
The computation sequence is rearranged such that parameters are reused. We adopted weight stationary data flow [3]. Operations on the same weights are grouped so that access to weight data from memory is minimized.

Data is broadcast and shared: in our weight-stationary systolic architecture, feature data and results move. Input feature data is broadcast to all Vector Processing Units (VPU). Each VPU computes and generates output channels independently from other cores. The results are sent back to a central memory pool. Then, the VPU performs all the operations necessary to generate a result. All intermediate data are localized in VPU’s, and no exchange of such data occurs with any other units.

With localized DRAM array pooling, and maximizing data movement, Sunrise chip overcomes slow DRAM latency and deliver high computation performance.

V. CHIP ARCHITECTURE

With HITOC, we have two wafers, logic wafer, and memory wafer, bonded together [Fig. 6]. On the logic wafer, we have pools of processing units. Underneath the logic pool on the other wafer are pools of DRAM arrays.

Logic wafer consists of mainly logic units, and control units that include processor and unified control engine (UCE) [Fig. 7].

There are two types of logic units: data serving unit (DSU) and vector processing unit (VPU). VPU’s perform computation on data. DSU’s serve data to VPU. Each DSU and VPU has their own multiple DRAM arrays directly bonded below the units from the DRAM wafer. All VPU’s and DSU’s form their respective pool. The overall bandwidth between DSU/VPU pool and DRAM pool is 1.8TB/s.

Feature data are stored in the DRAM of the DSU pool and are sent to the VPU pool for computation. The results are sent back to the DSU pool. The data bandwidth between the DSU pool and the VPU pool is 13 TB/s. This high bandwidth ensures that data transfer between DSU and VPU is not a bottleneck.

Because memory bandwidth is abundant in Sunrise chip, we choose to use vectors instead of tensors as the basic computational data unit. This allows us to optimize for better computational performance on sparse tensors.

With extremely high data bandwidth on Sunrise chip, synchronization of all modules is challenging. On this chip, all data flow and module operations are centrally controlled by a single unit called the Unified Control Engine (UCE). It consists of modules such as a Direct Memory Access controller (DMA), data path multiplexer controllers, and function selector. All modules are fully configurable to implement different neural networks.

There is a proprietary 13-bit processor on Sunrise chip. It mainly controls high-level tasks such as data batch movement and UCE configuration.

To minimize yield loss due to defects in memory, our DRAM PHY is capable of DRAM repair. Before shipment, DRAM is tested, and defects are recorded in non-volatile memory (NVM). During chip power-up, the defect information is retrieved, and repairs are applied to DRAM arrays.

There are two chip interfaces. One is a standard SPI interface, and the other is a proprietary high-speed-port (HSP) interface. SPI is for the host to transfer commands to the chip. The HSP interface is for data transfer with a transfer rate of 200MB/s.

Sunrise chip has three implementation layers: logic blocks, unified data flow control configuration, and firmware [Fig. 8]. Logic blocks consist of primitive functional blocks and configurable modules. The unified data flow control configu-
ration dictates how the configurable module functions. It also initiates predetermined sequences of operations. The top tier is the firmware. Firmware mainly modifies operation register values, changes configurations, or calls out configurations. The firmware also initiates large operations whose sequence is controlled by configuration. It is also responsible for host and chip communication. With this three-tier architecture, Sunrise chip implements a wide range of neural networks through a combination of firmware and configuration.

![Diagram of implementation layers]

Fig. 8. Implementation layers

VI. RESULTS

We fabricated Sunrise chip with a 40nm CMOS process and 38nm DRAM process. The chip consists of one die from logic wafer and one die from memory wafer [Fig. 9]. There are 32,768 MAC on the chip, with a die size of 110 mm² (12.4 mm × 8.8 mm) The chip has a high speed data interface with a transfer rate of 200MB/s and an SPI command interface. It has a peak performance of 25 TOPS. It performances inference of 1500 images per second with ResNet50 model. Internal memory bandwidth is 1.8TB/s. Internal memory capacity is 4.5Gb. The typical power consumption is 12W. Its temperature operating range is between -40 °C and 85 °C.

![Image of dies that make up a chip]

Fig. 9. Dies that make up a chip

We compare Sunrise chip with three other leading AI chips, whose information is publicly available. Table II contains key metrics and specifications for Sunrise as well as the other chips, referred to as Chip A [17], B [18], and C [19].

| Process | Sunrise | Chip A | Chip B | Chip C |
|---------|---------|--------|--------|--------|
| Die Size (mm²) | 40nm | 38nm | 456 | 512 |
| Peak Performance (TOPS) | 25 | 122 | 125 | 512 |
| Memory Capacity (MB) | 560 | 300 | 190 | 32 |
| Power Consumption (W) | 12 | 120 | 280 | 350 |
| Memory Bandwidth (TB/s) | 1.8 | 45 | no data | 3 |

*Measured in TOPS/mm². b Measured in MB/s/mm². c Measured in MB/mm². d Measured in TOPS/W.

Sunrise chip outperforms on two of the four metrics, memory capacity and energy efficiency [Tab. III]. Its peak performance is below chip C’s. This is understandable considering that Sunrise is fabricated on 40nm process, a process four generations behind that of chip C.

Sunrise memory bandwidth is below chip A’s. Chip A has large amount of fast SRAM on chip. SRAM enables high memory bandwidth. However, SRAM memory bit units are large and take up a large portion of the die area. This reduces memory capacity and leaves smaller die area for computation units. As a result, chip A lags behind Sunrise in both memory capacity and performance.

Sunrise takes a different approach to balance trade-offs between memory and performance. Replacing SRAM with DRAM leads to large memory capacity and leaves more die area for computation units. With HITOC and UNIMEM technology, this architecture not only overcomes slow DRAM latency but also has sufficient memory bandwidth to support high performance. HITOC cuts down data transfer energy consumption. UNIMEM removes SRAM cache, and thus the energy consumption associated with it. Both factors make Sunrise the most energy efficient amongst the other chips in the table.
In Table IV, we compare non-recurrence expense (NRE) and die costs. NRE mainly consists of process mask cost. Although the exact die cost of the other chips is not published, we estimate their die cost based on die size, wafer cost from major foundries, and expected yields. We also include the cost for delivering the same performance. It is expected that 40nm process delivers the lowest cost. Normally, a more advanced process delivers better cost-to-performance ratio. However, our chip delivers the best cost-to-performance ratio even with 40nm process. This is directly due to our chip architecture.

Combining all the discussed metrics, our Sunrise chip overall outperforms other leading AI chips despite its less advanced fabrication process. The HITOC and UNIMEM technology incorporated in this chip allows us move to a new and more optimal architecture. The key benefit is being able to achieve and surpass the performance of more advanced fabrication processes with less expensive fabrication.

VII. Projection

The AI chips in comparisons are fabricated with different processes. To compare the architecture effectively, we normalize each chip to a 7nm CMOS process and a 1y DRAM process, based on factors such as density, transistor performance, and power reduction. The factors are derived from the parameters of the CMOS process (Table V) [20][21] and the DRAM process (Table VI) [22] of leading foundries.

### Table IV

| Chip              | NRE      | Die Cost | Cost per TOPS |
|-------------------|----------|----------|---------------|
| SUNRISE (40nm)    | 2.2 × 10^{10} | 11        | 0.43          |
| Chip A (16nm)     | 7.2 × 10^{10} | 617       | 2.47          |
| Chip B (12nm)     | 15 × 10^{6}   | 296       | 1.19          |
| Chip C (7nm)      | 24 × 10^{6}   | 336       | 0.66          |

As seen in Table V, density is improved with each generation of process. More transistor computing units can be packed into the same die area. This not only improves device performance but also increases power consumption by the same factor. With more advanced process generation, one can choose high performance process to get performance gains, or choose lower power process to get better power efficiency. When we project the parameters of each chip in our normalization calculations, we use performance improvement parameters under the condition that power consumption is within the common range as seen in ASIC chips. Otherwise, we use power reduction parameters.

With all the chips normalized to 7nm, Sunrise chip architectures surpass all other three chips in all benchmarks (Table VII).

### Table VII

| Benchmark Comparisons Normalized to 7nm process |
|------------------------------------------------|
| Peak Performance | Memory Bandwidth | Memory Capacity | Energy Efficiency |
| SUNRISE          | 7.58          | 216            | 30.3            | 50.10          |
| Chip A           | 0.86          | 122            | 1.50            | 5.38           |
| Chip B           | 0.19          | no data        | 0.90            | 0.83           |
| Chip C           | 1.12          | 6.6            | 0.07            | 1.46           |

Although Sunrise chip is on a 40nm process, its performance per unit area exceeds that of two competing chips at 12nm and 16nm. It exceeds all three chips after normalized by process node. With the architecture of Sunrise, one can choose to either use a less expensive process to achieve the same performance as other chips or use current processes to get better performance then other chips.

As shown in Table III, the Sunrise chip has the highest memory bandwidth. We designed just enough bandwidth as needed for chip performance. Table IV shows that HITOC technology enables extremely high memory bandwidth. Even so, bandwidth after normalization exceeds that of all comparable devices.

Sunrise chips memory capacity is 20 times that of other chips at the 40nm node. When we normalized it to 7nm CMOS and 1Ynm DRAM process, it would reach 20 times the memory capacities of other chips. The gain in memory capacity is mostly a result of replacing all SRAM with DRAM, which has a density of more than 14 times higher than SRAM [12]. On a 800 mm² die, our architecture could reach a storage capacity as high as 24GB. The largest memory capacity on AI chip ever made is 18GB [15], which requires a whole wafer. With our architecture, the current memory capacity of an AI wafer can fit onto a single chip.

Sunrise chip is more energy-efficient than all other three chips, even though it is on a less advanced process. Our high energy efficiency is due to the removal of SRAM cache and the close proximity between memory and compute units.

Overall, Sunrise chip meets or exceeds benchmarks of AI chips in the market. The Sunrise architecture is projected to well exceed all benchmarks if fabricated with an advanced process.
VIII. CONCLUSION

We fabricated an AI chip, Sunrise, with our HITOC and UNIMEM technology. We developed a special architecture to overcome slow DRAM latency and completely replace SRAM with high-capacity DRAM. Sunrise chip, despite being fabricated on a 40nm process node, matches or exceeds other AI chips with more advanced process technology on the metrics of performance, memory bandwidth, memory capacity, energy efficiency, and cost. Based on the data of current silicon, we project that the same architecture is 7 to 20 times better on all major benchmarks. This architecture breaks the memory wall for AI applications. While our designs are motivated by the demands required by deep neural network training and inference, we believe that these technologies are applicable to chips used in other applications, such as high performance computing and big data processing.

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