Spike-time-dependent plasticity rule in memristor models for circuit design

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Received: 24 January 2021 / Accepted: 25 April 2022 / Published online: 18 May 2022
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Abstract
Spike-time-dependent plasticity (STDP) represents an essential learning rule found in biological synapses and is recommended for replication in neuromorphic electronic systems. This rule is defined as a process of updating synaptic weight that depends on the time difference between the pre- and post-synaptic spikes. It is well known that pre-synaptic activity preceding post-synaptic activity may induce long-term potentiation (LTP), whereas the reverse case induces long-term depression (LTD). Memristors, which are two-terminal memory devices, are excellent candidates to implement such a mechanism due to their distinctive characteristics. In this article, we analyze the fundamental characteristics of three of the most known memristor models, and then, we simulate them in order to mimic the plasticity rule of biological synapses. The tested models are the linear ion drift model (HP), the Voltage ThrEshold Adaptive Memristor (VTEAM) model, and the Enhanced Generalized Memristor (EGM) model. We compare the $I$–$V$ characteristics of these models with an experimental memristive device based on Ta$_2$O$_5$. We simulate and validate the STDP Hebbian learning algorithm proving the capability of each model to reproduce the conductance change for the LTP and LTD functions. Thus, our simulation results explore the most suitable model to operate as a synapse component for neuromorphic circuits.

Keywords LTP · LTD · Memristor models · Neuromorphic systems · Plasticity · Synapse · STDP

1 Introduction
Recently, neuromorphic technology has revealed that brain-based computer systems are capable of processing large amounts of data by using low-power operations [1]. However, they consist basically of similar structures like the human brain, composed of neurons linked by multiple synapses. These systems are able to follow a basic weight update rule across synapses, just like humans remember information. This rule was called spike-timing-dependent plasticity (STDP) [2]. It demonstrates how the strength of synaptic connections is modulated [2, 3]. Thus, the synaptic connection is strengthened when the pre-synaptic neuron fires before the post-synaptic neuron, which is known as long-term potentiation (LTP), and the connection is weakened when the firing order is reversed, which is called long-term depression (LTD).

Since the discovery of the STDP rule in biological synapses, researchers have been attracted to the concept of modifying synaptic weight using this rule in bio-inspired electronic synapses.

However, the circuit-oriented approach is complex in that the variable “synaptic weight” generally must be stored as an electric charge in a capacitor or even numerically in a neuromorphic integrated circuit. This adds complexity to the circuit and increases energy and power consumption. Consequently, non-volatile resistive memories, namely memristors, are currently employed in neuromorphic computation systems in order to reproduce the synaptic weight update by suitably changing their internal state [4–9].

In particular, the memristor has been widely studied and developed to mimic synaptic functions such as LTP, LTD, and STDP [4, 10–12]. Several complex tasks have been effectively performed using the memristor-based STDP learning rule, such as unsupervised learning [12], data classification [13], and pattern recognition [14].

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The memristor is the fourth circuit component that was originally introduced by Chua [15], which completes the link between the fundamental passive circuit elements alongside with resistor, capacitor, and inductor. Currently, memristors are widely used as synaptic devices due to their tunable resistance [16, 17], low-power operation, nano-scale physical structure, and high-density integration [18, 19].

In the literature, several research teams have fabricated memristive devices to emulate synaptic functions using a variety of materials [20–24]. The large variety of the memristor devices structure and materials has led to the development of various memristor modeling techniques [18, 20, 25–29]. The existence of multiple models makes it possible to choose an acceptable compromise between precision and simplicity.

From the available models, we will focus on three different models: the linear ion drift model (HP) [20], the Voltage ThrEshold Adaptive Memristor (VTEAM) model [29], and the Enhanced Generalized Memristor (EGM) model [18]. We simulated the \( I-V \) curve of these models in order to fit the experimental data of the \( \text{Ta}_2\text{O}_5 \)-RRAM device [23]. Next, we implement each model to determine both LTP and LTD functions, and then, we validate the STDP learning algorithm. We present a detailed comparison of these models, in order to explore the most promising memristor model to be used as a synapse component.

This article consists of the following sections: Sect. 2 provides a brief discussion of the memristor switching characteristics. Section 3 introduces the memristor fundamentals, including mathematical definition and working principle of the HP model, the VTEAM model, and the EGM model. Then, we present the \( I-V \) curves of these models compared to the experimental data. Section 4 discusses our simulation results obtained from the conductance change in order to validate LTP, LTD and the STDP learning algorithm. Section 5 contains discussion of our results. Finally, Sect. 6 concludes this article.

2 An overview of the memristor switching device

From 1976, the existence of memristive devices had remained theoretical [15], with no experimental evidence of their existence until 2008, when a team from HP Labs made their first experiment of a \( \text{TiO}_2 \)-based memristive device [20]. Since then, the memristor has been developed and made in several and varied approaches [30].

The memristor model that was practically realized at HP Labs is a solid-state device, which consists of a doped region with \( \text{TiO}_{2-x} \) oxygen gaps and an undoped region of \( \text{TiO}_2 \). These two regions are sandwiched together across two platinum electrodes, as depicted in Fig. 1a. The resistance change is induced by migration of the oxygen holes in the \( \text{TiO}_{2-x} \) region, produced by the application of a voltage across the memristor. Therefore, the oxygen holes migration depends on the sign of the applied voltage [20].

Applying a positive voltage to the top electrode of the device switches the resistance states from high resistance state (HRS) to low resistance state (LRS), and this switching is referred as SET state. Alternatively, when a negative voltage is applied, it switches from the LRS state to the HRS state, and this is referred as RESET state. Because of the poor oxygen mobility of the vacancies, they may be able to stand for a long time after switching off the power supply to the device. This means that if no power is provided to the device, then the memristors’ dynamic resistance will remain constant. This shows that the memristor device has the ability to operate as a non-volatile memory. Moreover, there is a major property that sets memristor devices apart from all other electronic devices, namely the \( I-V \) characteristic known as the pinched hysteresis loop, which is illustrated in Fig. 1b [31]. This distinctive shape arises from the nonlinear relationship between the voltage and the current passing across the memristor device. Besides, both negative and positive voltage pulses can affect the conductance of the device. This is similar to a biological synapse whose synaptic plasticity increases or decreases according to the applied action potential.

3 Memristor models

We provide in Table 1 a comparative study of three memristor models: HP, VTEAM and EGM, including their mathematical characteristics and their implemented parameters, which will be implemented and tested in the next section. We adopted a modeling approach used in our previous work [18]. This method is based on parametric analysis of the internal models parameters.

We simulate the studied models in Virtuoso® Custom IC Design using the Spectre simulator to fit the \( I-V \) results of an experimental \( \text{Ta}_2\text{O}_5 \)-RRAM memristor device and then to validate their capabilities to emulate synaptic functions.
| Memristor models | Linear ion drift model [20] | VTEAM model [29] | EGM model [18] |
|------------------|-----------------------------|------------------|----------------|
| Threshold voltage exists | No                          | Yes              | Yes            |
| State variable | 0 ≤ v < 1                   | Not explained physically | Yes           |
| Doped region width | 0 ≤ w ≤ D                 | 0 ≤ w ≤ 1       | 0 ≤ w ≤ 1     |
| Undoped region width | x_{on} ≤ x ≤ x_{off} | Not explained physically | Yes           |
| Current-voltage relationship | v(t) = \frac{R_{on}}{D} w(t) + \frac{R_{off}}{1 - w(t)} x(t) | v(t) = \frac{R_{on}}{D} w(t) + \frac{R_{off}}{1 - w(t)} x(t) | v(t) = \frac{R_{on}}{D} w(t) + \frac{R_{off}}{1 - w(t)} x(t) |
| State variable derivative | \frac{dw}{dt} = \frac{1}{D} v R_{on} i(t) | \frac{dw}{dt} = \frac{1}{D} v R_{on} i(t) | \frac{dw}{dt} = \frac{1}{D} v R_{on} i(t) |

Simulation parameters:
- R_{on} = 140 kΩ; R_{off} = 1 kΩ; \eta = 10^4; \alpha_p = 0.1; \alpha_n = 0.3; \eta_p = 0.1; \eta_n = 1
- V_{on} = 36 kΩ;
- V_{off} = 0.02 V;
- k_{on} = 100 ms^{-1}; k_{off} = 1 ms^{-1};
- \eta_{i,p} = 10^{14} m^2 s^{-1} v^{-1}.

Table 1: Comparative analysis of the memristor models

| Memristor models | Linear ion drift model [20] | VTEAM model [29] | EGM model [18] |
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| Doped region width | 0 ≤ w ≤ D                 | 0 ≤ w ≤ 1       | 0 ≤ w ≤ 1     |
| Undoped region width | x_{on} ≤ x ≤ x_{off} | Not explained physically | Yes           |
| Current-voltage relationship | v(t) = \frac{R_{on}}{D} w(t) + \frac{R_{off}}{1 - w(t)} x(t) | v(t) = \frac{R_{on}}{D} w(t) + \frac{R_{off}}{1 - w(t)} x(t) | v(t) = \frac{R_{on}}{D} w(t) + \frac{R_{off}}{1 - w(t)} x(t) |
| State variable derivative | \frac{dw}{dt} = \frac{1}{D} v R_{on} i(t) | \frac{dw}{dt} = \frac{1}{D} v R_{on} i(t) | \frac{dw}{dt} = \frac{1}{D} v R_{on} i(t) |

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- V_{off} = 0.02 V;
- k_{on} = 100 ms^{-1}; k_{off} = 1 ms^{-1};
- \eta_{i,p} = 10^{14} m^2 s^{-1} v^{-1}.
The linear ion drift model has been developed based on the first fabricated HP’s structure of the memristor device [20]. The above memristor behavior is mathematically described using equations in Table 1. The voltage $V$ and current $I$ curves of the HP model are shown in Fig. 2a, where we applied a sinusoidal voltage of 2 V with a frequency of 1 kHz. Figure 2b gives a comparative analysis between the experimental data of the Ta2O5-RRAM device [23] and the simulated results of the linear ion drift model.

The VTEAM model has been proposed by Kvatinsky et al. [29]. It is an extension of the TEAM model which is based on current threshold [28]. VTEAM is a voltage threshold-type model developed to fit different experimental results. Figure 3a gives the current $I$ and voltage $V$ curves of the simulated VTEAM model. Figure 3b shows the $I$–$V$ characteristics of the VTEAM model compared with the Ta2O5-RRAM memristor device [23].
Simulation of the enhanced generalized memristor model

The Enhanced Generalized Memristor model has been proposed in [27] and then explored in [18]. A sub-circuit of the memristor model is implemented as a simple netlist, which consists of multiple elements in SPICE [27]. Then, the EGM model undergoes some modifications in order to be implemented in Verilog-A [18]. The model was correlated with several memristor devices [5]. Figure 4a shows the current $I$ and voltage $V$ curves of the EGM model. Figure 4b

Fig. 5 Curves of the conductance change with voltage sweeping. Potentiations and depressions: a, b for the HP model, c, d for the VTEAM model and e, f for the EGM model
shows both the experimental $I$–$V$ curve of the Ta$_2$O$_5$-RRAM device [23] and the simulated results of the EGM model.

We can notice that the $I$–$V$ curves of the HP model and the VTEAM model indicate almost linear characteristics everywhere except the boundary, with a symmetric switching behavior for the HP model and an asymmetric behavior for the VTEAM model. Thus, the HP and VTEAM models cannot correlate well the behavior of the physical device. While the obtained $I$–$V$ characteristics of the EGM model with a symmetric curve agree well with the experimental data of the Ta$_2$O$_5$-RRAM memristor model [23].

4 Synapse function mimicking

4.1 Long-term potentiation/depression

In neural networks, the synaptic connection weight can be modulated through learning protocols, LTP, LTD and STDP. LTP indicates that certain patterns of synaptic activity can cause a lasting increase in synaptic strength, while other patterns of synaptic activity can cause a continuous decrease in synaptic strength, LTD.

To test LTP and LTD mechanisms, we applied a hundred consecutive pulses for different amplitudes values and a fixed pulses duration of 1 µs. Figure 5 explores the conductance change curves for the three memristor models showing the LTP and LTD cases when we applied different voltage amplitudes.

We specified two amplitude ranges for each model, the first one is used to maintain LTP and the second one is used to maintain LTD case.

- The pulse amplitude for the HP model is variated between $\{-1\, \text{V}, -4\, \text{V}\}$ for LTD and $\{1\, \text{V}, 4\, \text{V}\}$ for LTP. Figure 5a and b shows a gradual conductance decrease and increase for the HP model according to the input voltage bias.
- For the VTEAM model, the pulse amplitude is variated between $\{-1.5\, \text{V}, -3.5\, \text{V}\}$ for the LTP case and $\{1.5\, \text{V}, 3.5\, \text{V}\}$ for the LTD case. Figure 5c and d shows a gradual conductance decrease when applying positive voltage and no conductance increase for negative input voltage for the VTEAM model.
- For the EGM model, we choose a pulse amplitude variated between $\{-1.5\, \text{V}, -2.2\, \text{V}\}$ for LTD and $\{1.8\, \text{V}, 3\, \text{V}\}$ for LTP. Figure 5e and f shows a gradual conductance decrease and increase according to the input voltage bias for the EGM model.

The previous results of the $I$–$V$ characteristic and the conductance gradual change can prove that the EGM is the most effective and suitable model to be used as a synapse component. To further demonstrate this, we test the capacity of each model to validate the STDP mechanism.
4.2 Validation of the spike-time-dependent plasticity

The STDP is a learning mechanism based on mammalian brain synapses [32]. Several experimental investigations of this mechanism have been studied in synapses-based memristors architectures [10, 21–24]. The STDP adjusts the synaptic weight depending on the activities of the pre-synaptic and post-synaptic neurons [4]. The pre-neuron and post-neuron spikes reach the synapse in opposite directions. In this case, the change in synaptic weight is a function of the relative timing between the two neuron spikes, labeled \( \Delta t (\Delta t = t_{\text{post}} - t_{\text{pre}}) \), where \( t_{\text{pre}} \) and \( t_{\text{post}} \) are the arrival timing of pre- and post-spikes, respectively.

- When \( \Delta t > 0 \), the synapse exhibits long-term potentiation (LTP).
- When \( \Delta t < 0 \), the synapse exhibits a long-term depression (LTD).

The combination of the synaptic functions, LTP and LTD, subsequently confirms the STDP learning method.

In order to test and validate the STDP function using the memristor models detailed in our work, we employ a spike pair protocol [33, 34] in which the lower and upper memristor electrodes are assigned to the pre-synaptic and post-synaptic inputs, respectively, as shown in Fig. 6.

We considered the same voltage pulses for the three simulated memristor models. In this case, the voltage applied to their terminals was set to 2 V, which could be higher than their threshold voltages to change the resistance state. In the STDP demonstration, we consider the device conductance as the synaptic weight. Then, its variability corresponds to a change in the synaptic weight. The evolution of memristance for each memristor model during the application of positive and negative \( \Delta t \) is given in Fig. 7.

For the HP model, as shown in Fig. 7a when \( \Delta t > 0 \), the memristance decreases from 18.2 to 17.6 kΩ, and thus, the conductance exhibits LTP. And if \( \Delta t < 0 \), the memristance increases from 17.6 to 18.2 kΩ in order to display the conductance LTD.

For the VTEAM model, the memristance change is given in Fig. 7b. If \( \Delta t > 0 \), the memristance remains unchanged at 6.5 kΩ. And if \( \Delta t < 0 \), the memristance increases from 6.5 to 9.9 kΩ, and thus, the conductance demonstrates the LTD.

For the EGM model, the memristance change is given in Fig. 7c. If \( \Delta t > 0 \), the memristance decreases from 36.6 to 17.3 kΩ, and thereby, an LTP is shown. Then, if \( \Delta t < 0 \), the memristance increases from 17.3 to 36.6 kΩ; in turn, an LTD is exhibited by the conductance.

In addition, in order to implement the STDP learning rule, we apply the function \( \Delta w(\Delta t) \) described by Eq. 1, which is defined as a modification of the synaptic weight for an isolated pair of spikes [35, 36]. As given in Fig. 7, the amount of potentiation and depression will be determined as a function of the time difference between pre-synaptic and post-synaptic spikes.

\[
\Delta w(\Delta t) = \begin{cases} 
  w^+ e^{-\Delta t/\tau^+} & \text{for } \Delta t > 0 \\
  -w^- e^{\Delta t/\tau^-} & \text{for } \Delta t < 0
\end{cases}
\]

where \( w^- \) and \( w^+ \) indicate the minimum and maximum modifications of the synaptic weight with respect to the initial state during potentiation and depression functions, respectively. \( \tau^- \) and \( \tau^+ \) are the time windows parameters that define the synaptic weight update rate for LTD and LTP cases, respectively.

Moreover, we employ the results illustrated in Fig. 7 as found in our analysis to determine the change in the \( \Delta w \) function for each model. Figure 8 shows the simulation results of the STDP characteristics based on the three memristor models.

![Fig. 8](image-url)  
Fig. 8 STDP curve obtained using Eq. (1) for: a HP model, b VTEAM model, and c EGM model.
Using our previous results when testing the ability of the three simulated models to mimic the LTP and LTD, we can conclude that the conductance programmability of the HP model and the EGM model can demonstrate both LTP and LTD functions, which validate the STDP learning rule, as shown in Fig. 8a and c. Hence, these results are similar to biological synaptic systems [2]. Instead, the VTEAM model can only support LTD. Then, its STDP curve can show conformity with biological systems only when $\Delta t < 0$, as shown in Fig. 8b. So, we can conclude that we cannot apply the VTEAM model to implement neuromorphic circuit using the STDP learning method.

5 Discussion

To design neuromorphic circuits based on memristors, the implemented models must be sufficiently effective as compared to the behavior of physical devices, and they should support LTP and LTD functions to validate STDP learning mechanism. Also, it is desirable for the memristor model to be simple, flexible and general, so it can be adjusted to fit different physical memristive devices.

In this work, we have studied the most popular memristor models, the HP model [20], the VTEAM model [29] and the EGM model [18], in order to explore which of them would be the most suitable to operate as a synapse component for neuromorphic systems. Table 1 gives a comparison of these models, we note that the first model [20] has very limited parameters and does not include threshold voltage. It contains only five parameters, which make it less flexible to be tuned and to fit multiple memristor devices.

Its $I-V$ curve shows that the HP model does not correctly account for nonlinear behavior of the experimental memristor device.

However, our simulation results prove that this model can support both LTP and LTD functions and we successfully validate the STDP mechanism.

The VTEAM model [29] is a voltage-controlled model, and it is a general model, which can fit different memristor devices, but the application of a positive voltage allows the decrease of its conductance, whereas when applying a negative voltage, the conductance of the VTEAM model remains stable, and hence, there is no LTD in this case.

This affects the capability of the VTEAM model to validate the biological STDP rule, as illustrated in our results in Fig. 8b.

The EGM model [18] is flexible, it is a voltage-controlled model, and in general, it can fit various memristive devices. The simulated $I-V$ characteristics of this model with a symmetric curve correspond well with the experimental data of the $\text{Ta}_2\text{O}_5$-RRAM memristor device. Furthermore, the gradual conductance decrease and increase of the EGM model show that this model can exhibit the two synaptic functions LTP and LTD. This proves that we can implement and validate the STDP learning rule.

Figure 9 shows the relative variation curves of the STDP of the three implemented memristor models.

We prove that the first model can validate the biological STDP mechanism, but it has a convergence problem and it is less flexible. The second model is general and flexible, but using the implemented experimental data chosen in this work, the VTEAM model cannot support the LTP function. Hence, according to our results, the VTEAM model cannot implement the STDP rule like the biological synapses while applying the experimental data reported in this paper. The EGM model exhibits several characteristics that make it a good candidate for mimicking the function of a synaptic component. As shown in Fig. 9, we prove that this model can implement the STDP function in a similar way to biological synaptic systems [2]. These characteristics make the EGM model the most effective and acceptable model that can be used to validate the synaptic functions and then to successfully simulate neuromorphic circuits.

6 Conclusion

The memristive synapses play a key role in performing neuromorphic circuits. Their plasticity is obtained by a variation in memristance values based on the temporal coincidences of the pre- and post-synaptic points. In order to implement such systems, an effective memristor model is needed. In this article, we analyze the fundamental characteristics of three of the most known memristor models, the linear ion drift model (HP), the Voltage ThrEshold Adaptive Memristor (VTEAM) model and the Enhanced Generalized
Memristor (EGM) model. We tested their capability to imitate synaptic functions. We compared their $I-V$ characteristics to an experimental result. Then, we examined their gradual conductance modulation to prove the LTP and LTD functions which was achieved by modulating the polarity and amplitude of the applied pulse. Based on the conductance modulation of each model, we validate the STDP learning rule. From our simulation results, we find that the $I-V$ characteristics obtained from the EGM model match well with the experimental data of the Ta$_2$O$_5$-RRAM memristor device. Moreover, it is capable of demonstrating the LTP and LTD functions, which in turn would lead to the validation of the STDP learning rule. Consequently, the EGM model provides the most appropriate model to mimic the synaptic functions, and then, it can be employed in the neuromorphic circuits.

Enquiries about data availability should be directed to the authors.

**Funding** The authors have not disclosed any funding.

**Declarations**

**Conflict of interest** The authors have not disclosed any competing interests.

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