Quantifying the Efficacy of Logic Locking Methods

Joseph Sweeney, Deepali Garg, Lawrence Pileggi
Dept. of Electrical and Computer Engineering
Carnegie Mellon University, Pittsburgh, Pennsylvania
{joesweeney, deepalig, pileggi}@cmu.edu

Abstract—The outsourced manufacturing of integrated circuits has increased the risk of intellectual property theft. In response, logic locking techniques have been developed for protecting designs by adding programmable elements to the circuit. These techniques differ significantly in both overhead and resistance to various attacks, leaving designers unable to discern their efficacy. To overcome this critical impediment for the adoption of logic locking, we propose two metrics, key corruption and minimum corruption, that capture the goals of locking under different attack scenarios. We develop a flow for approximating these metrics on generic locked circuits and evaluate several locking techniques.

Index Terms—hardware security, logic locking, metrics

I. INTRODUCTION

Due to prohibitively high research and development costs, only a few foundries are manufacturing integrated circuits (ICs) in advanced technology nodes. Consequently, many IC companies tend to operate fabless, relying on untrusted foundries to manufacture their designs. Once a circuit is sent for fabrication, the foundry gains full visibility of the foundries to manufacture their designs. Since a circuit is

II. BACKGROUND

A. Attack Models

The vast majority of locking procedures can be described by the following model. A circuit is defined as a Boolean function, $C : X \rightarrow Y$, mapping an input space $X = \{0, 1\}^n$ to an output space $Y = \{0, 1\}^m$. The circuit is locked via a transformation that adds key inputs to the circuit, $L : C \rightarrow C_l$, where $C_l : X \times K \rightarrow Y$ and $K = \{0, 1\}^k$. When the correct key, $k_c$, is applied, the locked circuit produces the same input-output behavior as the original circuit, $\forall x, C_l(x, k_c) = C(x)$. Ideally, under other keys, the locked circuit behaves incorrectly to the extent that it is unusable.

The most rigorous definition of a successful attack is finding a functionally equivalent key. Here, the problem solved by the attacker is one of finding an exact key, $k_e$, for which the locked circuit produces the same function as the original, $k_e : \forall x C(x, k_e) = C(x)$. A relaxed version of the exact recovery success criteria is approximate recovery. Here, the attacker finds an approximate key, $k_a$, under which functionality of the locked circuit differs from the correct functionality with at most some probability $\epsilon$. Formally, $k_a : P_{x \in X} [C_l(x, k_a) \neq C_l(x, k_c)] < \epsilon$.

There are generally three attack scenarios considered in locking a circuit, differing in access to artifacts and abilities. 

1) Netlist: Adversarial access to the design data is a basic assumption of logic locking. Analyzing this data can produce a netlist containing the design's standard cells and interconnections. Along with the netlist, an adversary may have...
knowledge of transistor and interconnect models, allowing detailed physical simulation and analysis.

2) Oracle: A more powerful attack model assumes access to a functioning version of the unlocked design. The unlocked circuit has the correct key set in its tamper-proof memory, affording the attacker black-box access, commonly referred to as an oracle. Obtaining an oracle may be trivial if the IC is available on the open market, but also could be the result of compromised physical security. In this paper and commonly in the field, it is assumed that the adversary has access to the unlocked design’s scan chains. This allows an adversary to consider the circuit with only a combinatorial model.

3) Probe: The use of probing techniques may provide means to directly reveal key bits from the oracle. Foundries commonly use probing to aid the development of manufacturing processes and circuit failure analysis. Key values have been probed in nodes as small as 28nm [3]. However, as feature sizes continue to scale, this probing becomes more difficult, limited by spatial resolution [2]. Most work in logic locking has not directly considered this threat, relying on the validity of the tamper-proof memory assumption.

B. Insertion Locks
The earliest logic locking techniques insert parity gates (XOR/XNOR) into the circuit structure to invert nets depending on a key input [4]. The parity gates, termed key gates, are spliced into nets selected randomly or with heuristics maximizing corruption [5]. The circuit is subsequently resynthesized. These manipulations create a large amount of corruption within the circuit as the parity gate’s entire upstream function is inverted. Similar techniques utilize multiplexers (MUXs) and lookup tables (LUTs) in lieu of parity gates [6], [7]. Importantly, these techniques exhibit low overhead as few additional gates are added. These methods were originally developed targeting an oracle attack model. Unfortunately, within this context, these methods have been largely broken using a miter-based satisfiability (SAT) attack, detailed in section II-C.

C. Miter-Based SAT Attack
First proposed in [8], this attack uses a SAT solver, the locked netlist and an unlocked circuit to iteratively produce input-output (IO) relationships. These relationships are used to rule out all keys that do not produce the same behavior, narrowing the space of possible circuit functionalities. The IO relationships are efficiently learned through a three-step procedure: 1. First, a miter circuit, $M_0 \equiv C_i(x, k_0) \neq C_i(x, k_1)$, is encoded into a SAT solver to determine an input that produces different behavior for two different keys. 2. Next, the produced input, $x$, is applied to the unlocked circuit to determine the output, forming an input-output (IO) pair, $(x_0, y_0) \equiv (x, C_i(x, k_0))$, which the correct key must respect. 3. The IO pair is added as a constraint to the miter circuit for the next iteration, $M_i \equiv M_{i-1} \land (C_i(x_{i-1}, k_0) = y_{i-1}) \land (C_i(x_{i-1}, k_1) = y_{i-1})$. Now, any keys that satisfy the miter circuit will also satisfy the learned IO relationship, ruling out at least one of the keys from step 1. These steps repeat, adding more constraints until the miter circuit is unsatisfiable. At this point, any key that respects all learned IO relationships will be functionally correct.

D. Point Function-Based and Densely-Interconnected Locks
Following the miter-based SAT attack, the authors in [8] discuss a point function-like structure formed from an AND-tree locked with parity gates, $\bigwedge_{i=1}^{n} x_i \oplus k_i$, where $x_i$ is the $i$th bit of $x$. The structure requires an exponential number of iterations under their algorithm. This observation led to a series of locking schemes that incorporate close relatives of this structure to resist the miter-based SAT attacks. To further resist removal attacks based on analysis of properties such as signal probability [9] and Boolean sensitivity [10], many versions of this locking scheme have been proposed. While the exact scaling of the SAT-resistance depends on the specific technique, the class shows the greatest miter-based SAT attack resistance when the number of incorrect input values is minimal. Thus, there is an inherent trade-off between attack resistance and the corruption of the circuit.

Another approach to resisting the miter-based SAT attack is adding densely-interconnected instances into the circuit, overwhelming the SAT solver [11]–[13]. These instances typically have many interdependent keys. A prototypical example is LUTs combined with configurable routing, the resulting lock resembling a field-programmable gate array (FPGA) embedded into the circuit. The various locking methods vary on the specific insertion methods, density, and mixing with original logic.

III. LOCKING METRICS
A pervasive problem in the logic locking community is the lack of metrics that adequately capture the intended notions of security. Additionally, the metrics that do exist are only evaluated on trivially small circuits or rely on closed-form equations that correspond to simple structured locking schemes. In this section, we describe the limitations of existing metrics. We then define two metrics that capture intuitive definitions of security for the netlist and oracle attack models and subsequently relate the metric evaluation problem to the well-established field of model counting.

A. Existing Security Metrics
The run-time of the miter-based SAT attack has been a ubiquitous metric since the attack’s debut. The typical demonstration sweeps the number of key bits and produces a (hopeful) exponentially scaling attack time. While resistance to this attack is essential if the oracle attack model is considered, this run-time may give an over-optimistic notion of security. Importantly, while running the attack to completion may be infeasible, the intermediate results may produce keys that are functionally close to the original design. In this case, the adversary need not complete the attack, but rather run until the keys produced exhibit low enough error rates.

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A previously proposed metric for assessing a lock quality in terms of error rates is corruptibility [14], defined as

\[ \text{Cor}(C, C_l) \equiv P_{x \in X, k \in K}[C(x) \neq C_l(x, k)] \]

This metric captures the likelihood across all keys and inputs that a locked circuit is incorrect, essentially the total amount of inaccuracy in a locked circuit. However, it gives no notion of the distribution of incorrect values. An example of why this is important is depicted in Fig. 1. Here, a circuit is locked with two different schemes that produce locked circuits \( C_{l0} \) and \( C_{l1} \). The resulting miter truth tables, \( C \neq C_{l0} \) and \( C \neq C_{l1} \), are shown. Both locked circuits exhibit the same corruptibility, however, the quality of the locking schemes is clearly different. For half of the possible keys, \( C_{l0} \) is completely correct whereas \( C_{l1} \) has incorrect values for every key other than the correct one. This motivates the development of a metric that can capture this disparity.

### B. Key Corruption

Our first metric, key corruption, is meant to capture a more precise notion of resistance to oracle-based attacks beyond run-time. Key corruption is the portion of the input space that is mapped to incorrect outputs for a given key. Specifically, it is defined as

\[ \text{KeyCor}(C, C_l, k) \equiv P_{x \in X}[C(x) \neq C_l(x, k)] \]

This metric directly corresponds to the approximate key recovery outlined in section II-A. This is useful to the designer in assessing the accuracy of intermediate keys produced by an attack and also as a kernel in computing more complex metrics.

To evaluate the key corruption, we build a miter circuit, \( M \equiv C(x) \neq C_l(x, k_{\text{attack}}) \). Counting the number of input values that satisfy this miter and normalizing by the size of the circuit’s input space will determine the key corruption. Typical circuits can have input widths upwards of 64 bits, thus it is necessary to utilize approximation techniques as outlined in section III-D. The error of the estimated count of satisfying solutions can be tied to the bounds of the approximate solver.

Depending on the circuit’s application, the targeted key corruption definition can be adapted. The above definition counts an input value as incorrect if it has at least one output bit incorrect. Some applications may require several output bits to be incorrect. In this case key corruption could be defined as

\[ P_{x \in X}[\sum_{i=1}^{n} C(x)^{i} \neq C_l(x, k)^{i}] \geq t \],

where \( t \) is the required number of incorrect bits. Other definitions could weight certain bits more heavily, potentially useful in ensuring significant error in arithmetic operations.

### C. Minimum Corruption

While key corruption can assess the progress of oracle-based attacks, under a netlist attack model, a more useful metric to a designer is the probability that a sampled key meets a certain corruption threshold, \( \epsilon \in [0, 1] \). This threshold can be determined by the application. For example, disabling a cryptographic function may only require a small portion of the inputs to be corrupted whereas a neural network accelerator may need significantly more. We capture this notion using minimum corruption, defined as

\[ \text{MinCor}(C, C_l, k, \epsilon) \equiv \text{KeyCor}(k) \geq \epsilon \]

We then can define a probability of selecting a key that meets this minimum corruption value, \( p_{\text{mc}} \).

\[ p_{\text{mc}}(C, C_l, \epsilon) \equiv P_{k \in K}[\text{MinCor}(C, C_l, k, \epsilon)] \]

For a given key, minimum corruption discounts the corruption beyond the threshold. Again considering Fig. 1, we see that \( p_{\text{mc}} \) captures the difference between the two locking scenarios. The designer can determine a suitable threshold, then can scale the amount of locking until the probability of meeting the corruption threshold is acceptable.

The techniques discussed in section III-D can be used to efficiently approximate this metric. To obtain a \( p_{\text{mc}} \) estimate, we take a set of uniform random samples from the key space. For each of these sampled keys, we estimate the key corruption and compare it to the threshold to determine if it meets the minimum corruption. The fraction of key samples for which key corruption is greater than the threshold computes \( p_{\text{mc}} \).

### D. Estimating Metrics

In general, the metrics we propose will be used to evaluate the amount of discrepancy between the original and locked circuits under various scenarios. Calculation of these metrics directly maps to model counting (#SAT). The evaluation of metrics can be encoded as a Boolean formula wherein the number of satisfying solutions over the total space gives the value. Due to the high dimensionality of the problem, exact solutions can only be obtained for a limited key and input width. To understand how locks scale, we resort to approximation methods. Luckily, approximate model counting is a widely studied area with many efficient, open-source solvers.

We use the solver ApproxMC [15] as a kernel in estimating our proposed metrics. This solver uses hash functions to split a circuit’s input space into small, countable partitions of roughly equal size. By counting a single partition and multiplying by the number of partitions, the tool can give an estimation of the number of solutions to a formula. Repeating this process allows increased confidence in the estimation. Conveniently,

![Fig. 1. Miter truth-tables & corresponding metrics for two locked circuits.](image-url)
ApproxMC has a rigorous formulation of probably approximately correct (PAC) bounds. The relation between the real count, \( N \), and the estimated count, \( N_{\text{est}} \), is parameterized by \( \delta \in (0, 1] \) and \( \epsilon_a > 0 \). Specifically, the relationship is
\[
P[N/(1 + \epsilon_a) \leq N_{\text{est}} \leq N(1 + \epsilon_a)] \geq 1 - \delta.
\]

### IV. APPLICATION OF METRICS

The metrics proposed in the previous section can be used to evaluate the efficacy of locking techniques under the netlist and oracle attack models. We demonstrate this process using representative locks from the classes described in section II. We implement the locks using the open-source python library circuitgraph, which allows for easy manipulation of netlists. To allow for reproducibility, we share our lock and metric implementations in our repository that will be made available to the community upon acceptance. From the insertion-based lock types, we implement XOR, LUT, and MUX locking [4, 6, 7]. From the point-function based locks, we implement SFLL-Flex [16]. Finally, from the densely-interconnected locks, we implement Full-Lock [11] and LEBL [13]. Our miter-based attack implementation uses the SAT solver CaDiCal [17]. For the locking techniques that produce cyclic circuits, we use CycSAT [18] to form acyclic key conditions so that the attack terminates correctly. Each of these techniques is used to lock circuits from the ISCAS 85 combinational benchmark set [19].

#### A. Minimum Corruption under Netlist Attack Model

As discussed in section III-C, the probability of meeting minimum corruption provides the designer with a good understanding of how likely it is for an adversary to select a key that functions close to the correct design. In Fig. 2, we show an experimental run to determine an appropriate number of key samples to use for the estimation. As seen from the trend for our set of locked circuits, the value tends to converge around 1000 samples. We use this value for the remainder of our \( p_{\text{mc}} \) estimates.

Assuming that the adversary has no a priori knowledge of the key bits, we can evaluate \( p_{\text{mc}} \) for the selected locking techniques. We lock four circuits from our benchmark set with roughly 128 bits of locking. (The widths are not exact as the densely-interconnected techniques scale in unequal increments.) Using our estimation process, we uniformly sample keys and evaluate \( p_{\text{mc}} \), showing the results in Fig. 3. Several interesting conclusions can be drawn from this data. First, we see that XOR-locking shows the highest \( p_{\text{mc}} \) value. At this key width, all keys sampled are corrupted for all inputs on at least one output. This shows the significant amount of corruption obtained from the inversion of random nets in the circuit. Considering the other techniques, we see that they all, except SFLL-Flex, have a high probability of meeting a 0.2 \( \epsilon \) value. Generally, these probabilities decrease with \( \epsilon \) at rates depending on the circuit and lock type.

We can integrate more complex attacks into this analysis. For example, as discussed in [20], an adversary can analyze the local structure of a circuit locked with XOR-locking and determine a likely key with reported accuracy up to 95%. The effect of this bias in the key space can be assessed with our minimum corruption metric. We assume that the designer requires at least 10% of the input space to be corrupted. As the analysis of each locked gate is local, we assume that each key bit is independently drawn from a Bernoulli distribution with the probability parameter, \( p \), set to the accuracy of the model, \( P[k^i = k^i] \sim \text{Bernoulli}(p) \). We sweep \( p \) from 0.5 (i.e., no information) to 0.95, the highest reported accuracy of the models. For each accuracy level, we determine the minimum corruption for a set of circuits with varying amounts of XOR-locking. As seen from the results in Fig. 4, even at \( p = 0.95 \) and 96 bits of locking, the value of \( p_{\text{mc}} \) is very high. This shows that, while the local-structure analysis for likely key can significantly narrow the distribution of the correct keys, it does not necessarily translate into a circuit that is functionally close to the original; largely due to the high corruption of parity gates. If the attacker’s goal is to produce a functionally
The metric evaluated for oracle-based attacks is \( 448 \). The attacks are run with a timeout of 1 hour, indicated by the dashed red line. The zero value of key corruption is mapped to \( 10^{-14} \).

### B. Incremental Key Corruption of Oracle Attack Model

The *de facto* metric evaluated for oracle-based attacks is attack termination time. In this dimension, both the point function-based and densely-interconnected techniques exhibit very strong attack resistance. However, these attack times mean little if unaccompanied by a notion of corruption for the remaining keys.

Typically, when executing oracle-based attacks, a plausible key is produced in each iteration. Solving for additional keys is costly, likely motivating the attacker to simply use this incremental key. Evaluating the key corruption of the key from the attack can be used to indicate the progress of the attack.

In Fig. 5 we demonstrate the use of this metric to augment the miter-based SAT attack for our selected locking techniques. We lock the circuits with roughly 448 key bits and run the attack with a timeout of 1 hour, evaluating the corruption at each iteration. The results show several interesting insights. First, we see that in most cases XOR and LUT-locking terminate in under 100 seconds. At such large key widths, it is clear that these techniques do not hold up under this attack model. MUX-locking takes about an order of magnitude longer to terminate. As expected, we see no termination in the SFLL results; however, the key corruption remains too low to likely have a significant effect. The densely-interconnected techniques Full-Lock and LEBL generally show the best results, with the highest corruption levels at the timeout. We do see one run terminating under an hour for Full-lock. The trend in the key corruption for LEBL reveals an interesting pattern undetectable by just considering the attack termination time. Several of the ~ 100 intermediate results for circuits c2670 and c7552 are functionally correct keys, a major security vulnerability. An astute attacker could thoroughly test the intermediate key results and confirm that these keys have arbitrarily low corruption with the oracle.

### C. Overhead-Security Trade-Offs

Overhead in the typical VLSI metrics, delay, area, and power is a critical concern of logic locking. The application of the IC may enforce limitations on the acceptable overhead. Even if this is not the case, too much overhead may motivate the use of commercial solutions such as FPGAs or microprocessors, rather than design an ASIC. We analyze our selected locking techniques across these metrics to show their scaling with the number of key bits.

Using Cadence Genus along with a commercial standard cell library in a 28nm process, we obtain overheads as follows. The maximum frequency of the design is found via iterative logic synthesis runs. This result serves as the baseline implementation to which various amounts of locking are applied and to which the results are normalized. Each design is locked with the different techniques, varying key widths such that they produce roughly the same overhead range. We combine power, area, and delay into a single overhead value using, \( \text{Overhead} \equiv (\text{power}_{\text{locked}}/\text{power}_{\text{orig}}) \times (\text{delay}_{\text{locked}}/\text{delay}_{\text{orig}}) \times (\text{area}_{\text{locked}}/\text{area}_{\text{orig}}) - 1 \). Coupling this data with an attack model and corresponding security metric, we can visualize the overhead-corruption trade-off.

Fig. 6 displays the trade-off under the netlist attack model. We use \( p_{\text{mc}} \) at \( \epsilon = 0.5 \) plotted against the overhead. For each locking scheme, we draw the Pareto front. By a significant margin, the best performing locking scheme under these criteria is XOR-locking. With overhead less than 20\%, it shows a \( p_{\text{mc}}(0.5) \approx 1 \).

The oracle attack model results are plotted in Fig. 7. To handle the oscillations, we use the average \( \text{KeyCor} \) of the
keys produced in the last 100 seconds of the attack. Full-Lock shows the best result, closely followed by MUX-locking and LEBL. The other techniques appear as vertical lines since they terminated for all runs. Even though in Fig. 5, MUX-Locking has a lower per-bit key corruption, its low overhead makes it comparable to Full-Lock and LEBL.

V. DISCUSSION AND FUTURE WORK

Our proposed metrics offer a more nuanced evaluation of locking schemes compared to previous methods. Tailoring these metrics to specific scenarios enhances our understanding of potential adversary achievements and associated overhead costs. The framework also facilitates detailed attack comparisons, exemplified in our XOR-locking analysis under a structural attack.

Our results highlight a significant contrast between netlist and oracle attack models. While netlist attacks predict substantial key corruption, access to an oracle drastically reduces corruption values, even with increased overhead allowances. This underscores the critical importance of preventing oracle access in logic locking.

Future work can explore evaluating these metrics in a sequential setting as locking techniques evolve. Unrolling circuits, akin to sequential ATPG methods, can extend the applicability of our metrics. In the oracle attack model, estimating the time required to achieve a key corruption value and analyzing trends over attack time could yield valuable insights. Additionally, understanding the limitations of our approximation techniques in circuits with thousands of gates, within the logic cone sizes of industrial circuits, is a pertinent avenue for exploration.

VI. CONCLUSION

In this work, we have proposed two metrics for logic locking that capture notions of security for commonly considered attack models. We have shown how to estimate these metrics utilizing approximate model counting techniques. In evaluating the metrics on three families of locking techniques, we have shown previously unknown overhead-security trade-offs and vulnerabilities. Not only are these metrics critical information in the application of logic locking, but they can also be used to set quantitative goals for future locking schemes.

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