Built-in jitter measurement circuit for PLL based on variable vernier delay line

Zhikuang Cai\textsuperscript{1,2}, Haobo Xu\textsuperscript{2}, Shanwen Hu\textsuperscript{1}, and Jun Yang\textsuperscript{2a)}

\textsuperscript{1} College of Electronic Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing 210023, China

\textsuperscript{2} National ASIC System Engineering Research Center, Southeast University, Nanjing 210096, China

\textsuperscript{a)} dragon@seu.edu.cn

Abstract: In this paper, a novel built-in jitter measurement circuit (BIJM) for Phase-Locked Loops (PLL) based on a variable vernier delay line (VVDL) is proposed. Resolutions of the two-level VDLs can be designed flexibly and their lengths optimally according to the signal under test (SUT). A digitally controlled delay element (DCDE) using varactors acts as the basic delay element in VVDL. Instead of counters, thermometer-to-binary encoders are adopted in the design. An improved phase detector (PD) is also introduced. The circuit has been designed using an all-digital design methodology and verified with the TSMC 130 nm CMOS process. 800 MHz clock frequency is chosen, and the circuit occupies a total silicon area of 0.043 mm\textsuperscript{2}, which is reduced by 60% compared to the traditional VDL. Simulation results indicate coarse timing resolution of 15.4 ps and fine resolution of 2.1 ps, and measurement error is within 2.11%.

Keywords: phase-locked loops (PLL), built-in jitter measurement (BIJM), variable vernier delay line (VVDL), digitally controlled delay element (DCDE)

Classification: Integrated circuits

References

[1] S. Sunter and A. Roy: “BIST for phase-locked loops in digital applications,” IEEE Int. Test Conf. (1999) 532 (DOI: 10.1109/TEST.1999.805777).

[2] A. H. Chan and G. W. Roberts: “A jitter characterization system using a component-invariant vernier delay line,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 12 (2004) 79 (DOI: 10.1109/TVLSI.2003.820531).

[3] M. Ishida, et al.: “A programmable on-chip picosecond jitter-measurement circuit without a reference-clock input,” IEEE Int. Solid-State Circuits Conf. Dig. (2005) 512 (DOI: 10.1109/ISSCC.2005.1494094).

[4] G. H. Li and H. P. Chou: “A high resolution time-to-digital converter using two-level vernier delay line technique,” IEEE Nuclear Science Symposium Conference Record (2007) 276 (DOI: 10.1109/NSSMIC.2007.4436330).

[5] K. A. Jenkins, et al.: “On-chip circuit for measuring period jitter and skew of clock distribution networks,” IEEE Custom Integr. Circuits Conf. (2007) 157 (DOI: 10.1109/CICC.2007.4405703).
1 Introduction

Built-in jitter measurement (BIJM) is an effective solution focusing on measuring jitters of the Phase-Locked Loops (PLL) [1]. Generally, methods of BIJM for PLL are mainly based on vernier delay line (VDL), vernier oscillator (VRO), sampling techniques, and so on. A component-invariant VDL is proposed in [2], aimed at eliminating the component mismatches of the original VDL design. To avoid the dependence on reference clock, a significant enhancement to on-chip testing by eliminating the requirement for a reference clock is presented in [3]. In literature [4], a two-level vernier delay line technique is proposed to reduce the hardware overhead and expand the measurement range. A circuit for on-chip measurement of period jitter and skew of clock distribution is described in paper [5]. By using two delay lines differing by one clock period, and a single latch, the circuit measures the cumulative probability distribution due to jitter. Paper [6] combines a self-referenced clock and a cascaded time difference amplifier (TDA) with duty-cycle compensation, which results in reference-free, high-resolution timing jitter measurement without sacrificing operational speed.
The drawbacks of BIJM based on original VDL technique are also evident. First, the resolution of this method is highly dependent on the match of the delay elements, which is susceptible to process, voltage and temperature (PVT) impact. Although elaborate layout can alleviate this problem, it can never be eliminated. Second, as sub-gate resolution is achieved, the delay line must be extended to guarantee the expected dynamic range, resulting in long conversion time and large area overhead. Third, considerable phase detectors and counters are required to obtain the measurement results, leading to larger area, higher power consumption and aggravating the mismatch problem at the same time. Forth, reference clock is required during the measurement, which increases the measurement cost and introduces additional noise. In addition, the thermometer code read-out circuit used in this technique makes it difficult for successive measurement.

Aimed at these problems, a variable vernier delay line (VVDL) structure is proposed to shorten conversion time, reduce the required number of phase detectors, avoid using counters and alleviate the mismatch problem, thus dramatically reducing the area overhead and power dissipation, of course satisfying the measuring requirements for dynamic range and resolution at the same time.

The paper is organized as follows. Section 2 describes the fundamental principles of a PLL jitter measurement and some of its related analysis. Section 3 presents the details of the proposed circuit. Section 4 gives simulation results of the circuit which has been implemented with a TSMC cell library of 130 nm technology. Finally, Section V concludes this work.

2 Fundamental principles

A basic PLL is a negative feedback system that consists of a phase detector, a low pass loop filter, a voltage controlled oscillator (VCO) and a frequency divider. The proposed VVDL BIJM circuit is added in to the PLL, as shown in Fig. 1 [7].

The feedback signal $S_{\text{div}}$ is produced by frequency divider, whose frequency is only $1/N$ of $S_{\text{VCO}}$’s. By comparing its period with that of the jitter free reference signal $S_{\text{ref}}$, period jitter in $S_{\text{div}}$, i.e. $J_{\text{div}}$, can be obtained.

Due to the frequency divider, only one rising or falling edge in $S_{\text{div}}$ can be generated after $N$ cycles of $S_{\text{VCO}}$ [8]. Suppose there is a jitter free golden signal $S_n$, which has the same frequency as $S_{\text{VCO}}$. If there is no jitter in $S_{\text{VCO}}$, $S_{\text{div}}$’s frequency should equal that of $S_n$’s, which is $1/N$ of $S_n$. Namely,
\[ T_{\text{ref}} = T_n \times N \]  

where \( T_n \) is the period of \( S_n \). Then,

\[ J_{\text{div}} = T_{\text{div}} - T_{\text{ref}} = N \times T_n + \sum_{i=1}^{N} J_{\text{VCO}}(i) - T_{\text{ref}} \]

\[ = \sum_{i=1}^{N} J_{\text{VCO}}(i) \]

From the above description, it’s concluded that \( J_{\text{div}} \) is actually an accumulated jitter, which equals the sum of \( N \) cycles jitter in \( S_{\text{VCO}} \). This jitter is also called the long-term jitter. From this long-term jitter, \( S_{\text{VCO}} \)'s average period jitter can be obtained by dividing long-term jitter by \( N \), i.e.

\[ J_{\text{VCO}} = \frac{J_{\text{div}}}{N} \]

On the other hand, timing jitter of \( S_{\text{div}} \) equals that of \( S_{\text{VCO}} \), though some timing jitter information of \( S_{\text{VCO}} \) is missing.

VVDL BIJM circuit shares reference clock with the PLL, and takes the output signal of the frequency divider as the signal under test (SUT), which reflects the jitter information in PLL as explained above.

### 3 Circuit descriptions

The VVDL structure consists of a predict circuit, a coarse VDL, a fine VDL, an interface circuit and two thermometer-to-binary encoders as shown in Fig. 2.

In contrast to the traditional vernier delay line, VVDL contains two VDLs, i.e. coarse VDL and fine VDL, each of which has a different resolution, namely coarse resolution and fine resolution, defined as \( \tau_{\text{coarse}} \) and \( \tau_{\text{fine}} \) respectively.

VVDL has three modes, i.e. BP_Mode, Cali_Mode and Meas_Mode, and its effective mode is determined by the mode selection unit. In the BP_Mode, the
function of VVDL circuit is bypassed from PLL. In the Cali. mode, calibration circuit adjusts control words of delay elements in VVDL against PVT variations. In the Meas. Mode, input signals, namely the reference clock and the SUT, are firstly applied to predict circuit before they are fed into VVDL. The predict circuit guarantees that the upper signal is slower than the lower one. Next, input signals are measured by coarse VDL, and more accurately measured by fine VDL. For each VDL, phase detectors are used to detect the phase of the output signals of every stage, and the stage number where the rising edges of both signals coincide is fed into a thermometer-to-binary encoder.

The block diagram of DCDE is illustrated in Fig. 3. The propagation delay is controlled by control word C[3:0] in order to coordinate with the Cali. Mode, where C[3:0] is adjusted against PVT variations.

DCDE is basically composed by varactors as described in [9]. A simplified architecture of a varactor is also shown in Fig. 3.

When the control voltage $V_{ctrl} = V_{DD}$, the total capacitance is $C_{high}$, while the total capacitance is $C_{low}$ when $V_{ctrl} = 0$. Total capacitance difference $\Delta C$, induced by the control voltage difference, can be represented as

$$\Delta C = C_{high} - C_{low} \tag{4}$$

Capacitance difference means delay difference in VDL. Thus, a varactor pair is applied to create slight time difference for VDL. By elaborate width to length ratio design, delay of coarse VDL and the fine one can be digitally controlled, and the $i_{th}$ control bit can change the delay of DCDE by $2^{-i}$ times of $\Delta t$, which is the timing resolution of VDL.

Phase detector is another key circuit in VVDL. The schematic of ordinary phase detector (PD) is shown in Fig. 4 [10]. However, VVDL requires a highly symmetrical PD structure, and generally ordinary PD is not because of OR gate. For this reason, signal crossing occurred in simulation, as shown in the upper left corner in Fig. 4. Thus, some improvements have been made on the OR gate of ordinary PD to make it highly symmetrical as shown in the upper right corner in Fig. 4. And simulation result shows that the signal crossing problem is properly resolved.
Instead of using a large number of counters, thermometer-to-binary encoder is utilized in the proposed circuit, resulting in large area reduction and considerable power consumption decrease. Workflow of thermometer-to-binary encoder is illustrated in Fig. 5.

The output of VVDL is thermometer code, and it’s inconvenient to calculate the actual jitter. Therefore, a thermometer-to-binary encoder is proposed to convert two thermometer codes into two binary codes. Finally, subtraction is needed to get the final results:

$$J = \tau_{\text{coarse}} \times (Y)_D - \tau_{\text{fine}} \times (YY)_D$$  \hspace{1cm} (5)

where $(Y)_D$ and $(YY)_D$ are decimal values of $Y[3:0]$ and $YY[3:0]$ respectively.
4 Layout and simulation results

The circuit has been designed using an all-digital design methodology, including digital backend design steps such as Synthesis, STA, PnR, DRC/LVS and so on. As DCDE is a kernel module of the proposed circuit, its layout is elaborately designed and then extracted into FramView, which can be identified by Synopsys ICC tool and will be repeatedly instantiated in the design. To keep highly symmetrical, interconnection lines are designed as consistent as possible. Moreover, supply voltage VDD and VSS are also designed to be symmetrical in order to guarantee the supply balance of every cell. The circuit has been verified with the TSMC 130 nm CMOS process. Fig. 6 is the VVDL layout diagram. Coarse timing resolution of 15.4 ps and fine resolution of 2.1 ps are obtained in post-layout simulation.

![Layout diagram](image)

**Fig. 6.** Layout diagram

The circuit was simulated to verify its performance. Fig. 7 shows the statistical results of successive simulation.

![Histograms](image)

**Fig. 7.** (a) The histogram of the injected jitter, and (b) The histogram of the simulated measured jitter
The RMS value of the injected and the measured jitter in simulation are given in Table I. According to the post simulation data, the time that VVDL needed to complete 1000 groups’ signals is about 5 ms. For comparative analysis, this paper designs a traditional VDL circuit, whose delay chain length is 40 levels and the value of delay equals VVDL fine delay. The time that VDL needed to complete 1000 groups’ signals is about 12 ms in the same simulation environment.

Table I. Comparison between the injected and measured jitter

| Unit          | RMS Value |
|---------------|-----------|
| Injected jitter | 10.9 ps   |
| Measured jitter | 10.67 ps  |

To verify the circuit stability characteristics, simulations are performed in different process corners. Measurement results are shown in Fig. 8, which shows the injected jitter and measured jitter for fast-fast, slow-slow and typical-typical corner situations, indicating that the process variations have little impact on the measurement results.

Fig. 8. Injected jitter and measured jitter of the VVDL for fast-fast, slow-slow and typical-typical process corners.

Table II shows the performance comparisons of the proposed BIJM circuit with conventional BIJM designs [11, 12, 13, 14].

Table II. Comparison between the proposed BIJM circuit and conventional BIJM designs

| Methodology | [11] (simulation) | [12] (measurement) | [13] (measurement) | [14] (measurement) | This Work | Unit |
|-------------|-------------------|--------------------|--------------------|--------------------|-----------|------|
| Process     | 180               | 180                | 90                 | 90                 | 130       | nm   |
| Voltage     | 1.8               | 1.85               | 1.2                | 1.0                | 1.2       | V    |
| Frequency   | 100               | 1250               | 1000               | 3000               | 800       | MHz  |
| Jitter (RMS)| 42.7              | 5.45               | 0.73               | 4.15               | 10.9      | ps   |
| Resolution  | 18.5              | 1.17               | 0.88               | 1.8                | 2.1       | ps   |
| Area        | 0.004             | 0.03               | 0.45               | 0.038              | 0.043     | mm²  |
| Error       | 46.8              | 14.6               | 15.9               | 8.9                | 2.11      | %    |
It can be concluded from Table II that the VVDL structure is compact, accurate and has a high resolution.

5 Conclusion

In this paper, a high-resolution PLL jitter measurement circuit which is based on VVDL is proposed. Compared to traditional VDL, VVDL shortens conversion time, reduces the required number of phase detectors, avoids using counters and alleviates the mismatch problem, thus dramatically reducing the area overhead and power dissipation.

Acknowledgments

This work was supported by the National Natural Science Foundation of China (No. 61504065, No. 61501261), the Natural Science Foundation of Jiangsu Province (No. BK20150848), and Nanjing University of Posts and Telecommunications Scientific Foundation (No. NY214157).