Analysis, design and performance characterisation of transistor clamped dual active bridge DC–DC converter in wide voltage range

Dharmendra Yadeo | Pradyumn Chaturvedi | H. M. Suryawanshi | Dipesh Atkar | Sai Krishna Saketi

Department of Electrical Engineering, Visvesvaraya National Institute of Technology, Nagpur, Maharashtra, India

Correspondence
Dharmendra Yadeo, Department of Electrical Engineering, Visvesvaraya National Institute of Technology, Nagpur, Maharashtra, India. Email: dharmendra.yadeo@gmail.com

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Abstract
In order to control dual active bridge conventionally, control scheme such as single phase shift is used which reduces the system efficiency particularly when voltage conversion ratio differs from unity. This causes more circulating power and high current stress in switches. Moreover, voltage obtained at primary side of high frequency transformer is of two-level only, which increases voltage stress across it. Furthermore, it has only one degree of freedom which confines its ability to regulate power flow. In this paper, a transistor clamped dual active bridge dc–dc converter is proposed with three degrees of freedom which improves its ability to regulate power flow, and because of incorporation of five-level voltage on primary side of high frequency transformer, current stress in switches and voltage stress across high frequency transformer reduces. Mathematical modelling for the proposed converter is done for obtaining power flow equation. In addition to the phase shift control, proposed converter has two more control parameter which enhances the power flow controllability of the converter. Comparative analysis with conventional dual active bridge shows that the proposed converter is having more efficiency. Performance of the proposed converter is verified via simulation and hardware implementation.

1 | INTRODUCTION

For long distance power transmission, high voltage direct current (HVDC) has proven its innumerable advantages over high voltage AC (HVAC) transmission system such as reduced right of way (ROW), no reactive power demand, no skin effect, increase in power flow capability, less infrastructure, reduced losses, good power flow controllability, high flexibility, high power density and efficiency [1–10]. Many researches have emphasised that if generation and distribution is carried out at DC level, it will be very beneficial. In order to integrate power generated by various renewable sources (RES) such as wind and photovoltaic (PV), DC collector grid can be more effective as inverter and filter, required for interconnection to AC grid for elimination of harmonics to meet the grid code, will not be needed. Due to intermittent nature of RES, it becomes indispensable to integrate energy storage technique for improvement in reliability and flexibility in operation. Moreover, interconnection of high density batteries, fuel system and energy recovery system to a DC bus is easy [11]. It leads to increased efficiency and high reliability of DC system. At distribution level, DC system has many applications such as telecommunication, shipboard system, traction loads, LED based lighting, electric vehicle charging, variable speed heat pumps, computer and many more consumer electronics [10, 12]. The medium voltage DC (MVDC) system can be served as a link between low or medium voltage generation/distribution and high voltage transmission. They can strengthen the existing power distribution system effectively [13–15].

In all above power conversion system to achieve galvanic isolation and voltage matching, conventional low frequency transformers (LFT) are used. But these LFT are bulky, noisy and
heavy, making it difficult to achieve high power density. In order to improve the power density, high frequency transformers (HFT) are considered most influential because of its light weight, low volume and low cost. It can also avoid the current and voltage waveform distortion due to core saturation as in low frequency transformers. In the research of high frequency link power conversion system, isolated bidirectional DC–DC converters serve as the key component. The comparison of dual active bridge (DAB) with several other DC–DC converters reveals that DAB is an interesting alternative for high power applications [16, 17, 21]. DAB was earlier introduced in [18, 19] and plays a vital role to integrate two DC buses operating at same or different voltages because of its inherent features of bidirectionality, galvanic isolation and high power density. Figure 1 shows general block diagram of DC grid employing DAB for regulation of power flow between two DC buses, and acting as prerequisite for maintaining constant voltage at either bus. DC Bus 1 is connected to medium voltage AC grid (MVAC) through inverter/rectifier and various renewable energy sources (RES) through DC–DC converter and energy storage system (ESS) through bidirectional DC–DC converter. DC Bus 2 is connected to low voltage AC (LVAC) bus through inverter/rectifier along with various DC loads.

Conventionally, DAB is controlled by single phase shift (SPS) technique. In SPS, two H-bridges of DAB are controlled by phase shift angle, making one bridge to operate at leading phase with respect to other. Power flows from leading end to the lagging end. At unity voltage conversion ratio and full load, its operation is more efficient due to inherent zero voltage switching (ZVS). However, at light load and when voltage conversion ratio differ from unity, its efficiency decreases because of hard switching. At high voltage conversion ratio, its circulating power increases, which leads to rise in current stress [17, 20]. Moreover, it has one degree of freedom, which limits its power flow controllability.

At voltage conversion ratio other than unity and at lighter load, to reduce current stress, extended phase shift (EPS) technique is presented [22]. In EPS, driving pulses for one bridge are pulse width modulated, so voltage across that bridge becomes three-level, while other bridge is operated with 50% duty cycle [23]. Further, two bridges are operated with mutual phase difference, also called as outer phase shift. It has two degrees of freedom for power regulation.

Furthermore, in order to decrease circulating current and to minimise the current stress, dual phase shift (DPS) control technique is introduced in [24]. It has only two power flow control parameters, that is, inner phase shift ratio and outer phase shift ratio. Inner phase shift ratio determines the phase shift between two legs of H-bridges, whereas outer phase shift ratio regulates the phase shift between H-bridges of primary and secondary side of HFT. Inner phase shift ratio is highly sensitive to any change in outer phase shift ratio for the given amount of power flow and involve complex computation to obtain specific value of outer phase shift with corresponding inner phase shift [25]. Moreover, voltages across primary and secondary side of HFT is of three-level only.

Triple phase shift (TPS) control has three degrees of freedom which is obtained by independently controlling inner phase shift ratio of both the two H-bridges of DAB and outer phase shift ratio. SPS, EPS, DPS can be regarded as the special cases of TPS control. When DAB is controlled by TPS, a complicated algorithm, to compute desired value of inner phase shift ratio for the primary and secondary side legs of H-bridges, is required. Any slight variation in sensed data will drastically affect the performance of DAB which will degrade the efficiency of the system [26].
In [27], three-level DAB converter, composed of neutral point clamped inverter at both the sides of HFT for high voltage application is introduced. Power flow equations for different conditions were obtained. However, number of switches are more and no data or result regarding the current stress and efficiency is provided.

Taking into account five-level inverter, employing five switches which was initially proposed in [28], transistor clamped dual active bridge (DAB) converter is proposed in this paper. Proposed converter has three degrees of freedom as compared to conventional two-level DAB, which has only one degree of freedom to regulate power flow when controlled with SPS technique. It improves its ability to regulate power flow and because of incorporation of five-level voltage at primary side of HFT, current stress in switches decreases significantly at different voltage conversion ratio and it also leads to reduction in voltage stress across HFT. Modelling for the proposed converter is done for obtaining power flow equation. In addition to the phase shift control, proposed converter has two more control parameter which enhances the power flow controllability of the converter. Comparative analysis with conventional DAB shows that the proposed converter is having more efficiency. Section 2 presents the overview of conventional DAB under SPS control. Section 3 focuses on proposed transistor clamped DAB topology and its operation. Section 4 deals with mathematical modelling and switching control analysis in different modes. Section 5 deals with soft switching analysis, selection of electrical parameters and performance comparison between conventional DAB and proposed converter. Section 6 discusses validation of proposed topology by experimental analysis followed by conclusion in Section 7.

2 CONVENTIONAL TWO-LEVEL DAB DC–DC CONVERTER OPERATION

Schematic of conventional two-level dual active bridge consisting of two H-bridges on both the sides of HFT is shown in Figure 2. \( V'_{DC1} \) and \( V'_{DC2} \) are the input and output DC voltages, respectively. \( L \) is a leakage inductance of HFT. \( n \) is the transformer turns ratio from primary to the secondary side. \( V'_p \) and \( V'_s \) are the input and output AC voltages of HFT, respectively. In DAB only series connected leakage inductance is taken into account, as magnetic inductance connected in parallel assumes to have higher inductance value as compared to leakage inductance and so it can be considered as open circuit. Conventionally, DAB is controlled by SPS control technique [18]. Power flow direction from \( V'_p \) to \( V'_s \) for analysing operation of SPS is considered. Operating waveform when DAB operating with SPS control is as shown in Figure 3. In this technique, power flow is controlled by varying phase shift angle \( \delta \).

According to the inductor balance principle, average current through transformer under steady state is zero. Using assumption \( i'_{\theta_1} = -i'_{\theta_2} \), current equations are derived which gives maximum instantaneous current as

\[
|i'_{\theta}|_{max} = |i(\theta'_2)| = \frac{nV'_{DC2}}{2\omega L} [\pi(k-1) + 2\delta], \quad (1)
\]

where \( k = \frac{V'_{DC1}}{nV'_{DC2}} \) is the voltage conversion ratio and \( f \) is the switching frequency. Here, \( k > 1 \) as the converter is assumed to be operated in buck mode.

Average transmission power \( P_T \) for the conventional DAB can be obtained as,

\[
P_T = \frac{1}{\pi} \int_{\theta}^{\pi} V'_p V'_s(\theta) d\theta. \quad (2)
\]

After simplification power equation will be

\[
P_T = \frac{nV'_{DC1}V'_{DC2}}{\omega L} \delta \left(1 - \frac{\delta}{\pi}\right) \quad \text{for} \quad 0 < \delta < \pi. \quad (3)
\]

Maximum power for DAB when operating with SPS technique is obtained at \( \delta = \frac{\pi}{2} \) and it is called as unified power \( (P_N) \).
FIGURE 4  Schematic of transistor clamped dual active bridge dc–dc converter

which is given as,

\[ P_N = \frac{\pi n V_{DC1} V_{DC2}}{4\omega L}. \]  

(4)

For comparative analysis, normalised transmission power \((p_T)\) for SPS technique is obtained as,

\[ p_T = \frac{P_T}{P_N} = \frac{4}{\pi^2} \delta (\pi - \delta). \]  

(5)

In terms of load resistance \(R\), \(V_{DC2}\) is derived as,

\[ V_{DC2} = \frac{nV_{DC1} R}{\omega L} \delta \left(1 - \frac{\delta}{\pi}\right). \]  

(6)

Now unified current stress \(G_T\) for SPS will be given as,

\[ G_T = \frac{\left| i_L \right|_{\text{max}}}{i_N} = \frac{2}{\pi} [\pi (k - 1) + 2\delta], \]  

(7)

where normalised current \(i_N\) will be given as,

\[ i_N = \frac{P_N}{V_{DC1}} = \frac{\pi n V_{DC2}}{4\omega L}. \]  

(8)

If conventional DAB is controlled with traditional phase shift scheme, current stress is lesser at unity voltage conversion ratio and it increases if voltage conversion ratio \(k\) increases beyond unity. So conventional DAB is not suitable for operation when \(k\) is different from unity. Moreover, it has only one control parameter, that is, \(\delta\), if controlled with SPS control, through which only power flow control is possible and current stress controlling is not feasible.

3 | PROPOSED TRANSISTOR CLAMPED DUAL ACTIVE BRIDGE DC–DC CONVERTER

The schematic of transistor clamped dual active bridge dc–dc converter as shown in Figure 4. Primary side consists of H-bridge which is composed of four switches \((S_2, S_3, S_4, S_5)\) and one auxiliary switch \((S_1)\) with \(G_2, G_3, G_4, G_5\) and \(G_1\) as their switching pulses, respectively. \(L\) is the leakage inductance of HFT which provides galvanic isolation for DAB.

\(V_{DC1}\) and \(V_{DC2}\) are the input and output side voltages, respectively. Secondary side consist of simple H-bridge in which four switches \((S_6, S_7, S_8, S_9)\) are employed, having switching pulses \(G_6, G_7, G_8, G_9\), respectively. Input capacitor \(C_1\), and output capacitor \(C_0\) are relatively big to reduce any ripple in DC link voltage. HFT has turns ratio of \(n\) from primary to secondary side. \(V_p\) and \(V_s\) are the input and output voltages of HFT. Primary side voltage will be of five-level whereas secondary side voltage will be of two-level. Current through HFT will be due to voltage difference between \(V_p\) and \(V_s\).

Due to auxiliary circuit consisting of one switch \(S_1\) and four diodes, along with H-bridge, five-level voltage is obtained at primary side of HFT. It reduces the rate of change of voltage in comparison with conventional two-level DAB. The switching state and output voltage level obtained are given in Table 1.

Switching pulses for different switches of proposed converter can be generated as shown in Figure 5. If \(S_1\) is ON it gives
The voltage and current waveform for transistor clamped dual active bridge dc–dc converter in case 1 when $0 < \delta < \varphi_1$ is shown in Figure 6.

On the secondary side of HFT, voltage will be either $V_{DC_2}$ or $-V_{DC_2}$ depending on switching state of switches. Detail modes and switching state is discussed in Section 4. $\varphi_1$ and $\varphi_2$ are the switching angle for primary voltage as shown in Figure 6 where $0 < \varphi_1 < \varphi_2 < \pi/2$. Power flow and nature of primary voltage can be easily controlled by control parameters $\varphi_1$ and $\varphi_2$. Because of the five-level primary voltage, rate of change of current is lesser in proposed converter as compared to conventional two-level DAB when operated with SPS technique. It will ensure lesser current stress even if $k > 1$. Power flow equation for proposed converter can be obtained as given in subsequent section.

### 4 | MODELLING AND SWITCHING CONTROL ANALYSIS IN DIFFERENT MODES

Depending on the instantaneous voltages at primary and secondary side of HFT, inductor current is determined. If there is any change in voltage magnitude, current changes its slope. Full cycle of the current waveform can be divided into 10 different modes, depending on the instantaneous magnitude of primary and secondary voltages. Figure 6, shows various modes of operation of the proposed converter. Phase shift angle $\delta$ can be varied as per power flow requirement. Based on the phase shift angle $\delta$, three cases may arise:

- Case 1: $0 < \delta \leq \varphi_1$
- Case 2: $\varphi_1 < \delta \leq \varphi_2$
- Case 3: $\varphi_2 < \delta \leq \pi/2$

For analysis purpose only Case 1 is considered in this paper where phase shift $\delta$ is lesser than $\varphi_1$. However, analysis for the other two cases can be done in similar manner. Figure 6 shows the voltage and current waveform of proposed converter under Case 1. Instantaneous switching angle in one complete full cycle of waveform are given as $\theta_0$ to $\theta_{10}$. As the current waveform is having half wave symmetry so current equations in half cycle are obtained. $\theta_a$ to $\theta_e$ are the switching angle duration in different modes in half cycle. Mode $M_1$ to Mode $M_5$ form the half cycle. Steady state equation in different modes can be given as:

**Stage 1 $[\theta_0, \theta_1]$** Figure 7: Prior to $\theta_0$, $S_3$, $S_4$ are ON, on the primary side and other switches are OFF state. Current through primary winding is negative and it flows through $S_3$ and $S_4$. Secondary winding current flows through antiparallel diodes of $S_7$ and $S_8$.

At $\theta_0$, $S_3$ is turned OFF and $S_1$ is turned ON, inductor current $i_L$ flows through $S_1$ and $S_4$. Primary side bridge voltage is $-V_{DC_1}/2$ and secondary side bridge voltage is $-nV_{DC_2}$. Current $i_L$ decreases to a negative peak value and in this stage current is expressed as

$$i_L(\theta) = i_L(\theta_0) + \left(\frac{-V_{DC_1}}{2} + nV_{DC_2}\right)\omega L \theta_a$$  \hspace{1cm} (9)

**Stage 2 $[\theta_1, \theta_3]$** Figure 7: At $\theta_1$, $S_1$ is turned OFF and inductor current flows through $S_4$ and antiparallel diode of $S_2$ on the primary side. Secondary winding current continues to flow through antiparallel diode of $S_7$ and $S_8$. The primary bridge voltage becomes zero. Current $i_L$ starts to increase and in this
Stage 3 [θ₂, θ₃] Figure 8: At θ₂, S₄ is turned OFF and S₃ is turned ON. Primary winding current flows through S₃ and antiparallel diode of S₅. The primary bridge voltage stays to zero. Current \( i_L \) continues to increase.

Stage 4 [θ₃, θ₄] Figure 8: At θ₃, in the secondary side, switches S₆ and S₉ are turned ON and secondary winding current flows through S₆ and Sₙ. Secondary bridge voltage becomes \( V_{DC2} \). The inductor current \( i_L \) starts decreasing again. Current \( i_L \) in this stage can be expressed as

\[
i_L(\theta) = i_L(\theta_3) + \left( \frac{V_{DC2}}{2} \right) (\theta_4 - \theta_3).
\]

Stage 5 [θ₄, θ₅] Figure 8: At θ₄, in the primary side, switch S₃ is turned OFF and switch S₁ is turned ON. Primary winding current flows through the S₁ and antiparallel diode of S₅. Primary bridge voltage becomes \( \frac{V_{DC1}}{2} \). In the secondary side secondary winding current continues to flow through S₆ and Sₙ. The inductor \( i_L \) current starts increasing. Current \( i_L \) in this stage can be expressed as

\[
i_L(\theta) = i_L(\theta_4) + \left( \frac{V_{DC1} - nV_{DC2}}{2} \right) \theta_5.
\]
Substituting (15) in (16)–(21), current at different boundary conditions in terms of controllable variable $\delta$, $\varphi_1$, and $\varphi_2$ in each mode can be determined as:

$$i_L(\varphi_1) = -\frac{1}{4\omega L} (V_{DC1} - 2nV_{DC2}) \theta_a + (2nV_{DC2}) \theta_\delta + \theta_d,$$

$$- (2nV_{DC2}) \theta_d + (V_{DC1} - 2nV_{DC2}) \theta_e$$

$$+ (2V_{DC1} - 2nV_{DC2}) (\theta_a + \theta_d),$$

$$i_L(\varphi_2) = -\frac{1}{4\omega L} (V_{DC1} - 2nV_{DC2}) \theta_a - (2nV_{DC2}) (\theta_d + \theta_l),$$

$$- (2nV_{DC2}) \theta_d + (V_{DC1} - 2nV_{DC2}) \theta_e$$

$$+ (2V_{DC1} - 2nV_{DC2}) (\theta_a + \theta_d),$$

$$i_L(\varphi_3) = -\frac{1}{4\omega L} (V_{DC1} - 2nV_{DC2}) \theta_a - (2nV_{DC2}) (\theta_d + \theta_l),$$

$$+ (2nV_{DC2}) \theta_d - (V_{DC1} - 2nV_{DC2}) \theta_e$$

$$+ (2V_{DC1} - 2nV_{DC2}) (\theta_a + \theta_d),$$

$$i_L(\varphi_4) = -\frac{1}{4\omega L} (V_{DC1} - 2nV_{DC2}) \theta_a - (2nV_{DC2}) (\theta_d + \theta_l),$$

$$+ (2nV_{DC2}) \theta_d - (V_{DC1} - 2nV_{DC2}) \theta_e$$

$$- (2V_{DC1} - 2nV_{DC2}) (\theta_a + \theta_d).$$

Similarly,

$$i_L(\varphi_5) = -\frac{nV_{DC2}}{2\omega L} \lfloor 2\delta + \pi (k - 1) + 2\varphi_1 - k(\varphi_1 + \varphi_2) \rfloor,$$

$$i_L(\varphi_6) = -\frac{nV_{DC2}}{2\omega L} \lfloor 2\delta + \pi (k - 1) + 2\varphi_2 - k(\varphi_1 + \varphi_2) \rfloor,$$

$$i_L(\varphi_7) = -\frac{nV_{DC2}}{2\omega L} \lfloor \pi (k - 1) - k(\varphi_1 + \varphi_2) \rfloor.$$

By knowing initial value of current in each mode, instantaneous current for different modes can be obtained.

It can be observed from (23)–(27) that the inductor current is a function of $k$, $V_{DC2}$, $\varphi_1$, $\varphi_2$, and $\delta$. Thus, inductor current can be varied by changing step angle $\varphi_1$ and $\varphi_2$ or by phase shift $\delta$.

From Figure 6, it can be observed that $i(\varphi_1)$ corresponds to the peak current resulting into current stress for proposed transistor clamped DAB converter. Hence,

$$|i_L|_{\text{max}} = |i_L(\varphi_1)|,$$

$$|i_L|_{\text{max}} = \frac{nV_{DC2}}{2\omega L} \lfloor 2\delta + \pi (k - 1) + 2\varphi_1 - k(\varphi_1 + \varphi_2) \rfloor.$$
Based upon power flow control analysis, power can be regulated by controlling $\delta$, $\varphi_1$, and $\varphi_2$. This analysis is further used for comparison of current stress in proposed converter.

5.1 Power flow controllability

Figure 9 shows variation of per unit power flow when there is change in controllable parameter $\delta$, $\varphi_1$, and $\varphi_2$. Here, $\delta$ is varied from 0 to $\frac{\pi}{2}$. With different combination of $\varphi_1$ and $\varphi_2$, variation in per unit power flow is obtained. Four conditions are taken into account where values of $\varphi_1$ and $\varphi_2$ varies. It shows that with change in controllable parameters, power flow changes. Thus, proposed transistor clamped DAB has three degrees of freedom as compared to only one degree of freedom for conventional two-level DAB converter which enhances the power flow controllability of the proposed converter.
For fixed power flow and other parameters \(V_{\text{DC}1}, V_{\text{DC}2}, \delta, f\), desired value of leakage inductance is calculated and is found to be 33 \(\mu\)H. Leakage inductance of HFT is 11 \(\mu\)H. Additional 22 \(\mu\)H, inductance is added externally. Toroidal ferrite core of EPCOS N30 with inductance factor \(A_L\) of 5.46 \(\mu\)H is chosen for which two turns are required.

### 5.2.3 Switching frequency

Increasing switching frequency will reduce the size of magnetics and leads to increased power density. However, due to parasitic capacitance of MOSFET, with increased in switching frequency, switching losses increases which will reduce the efficiency of converter at lighter load. Therefore, selecting the switching frequency is a trade-off between high efficiency and power density. Taking into consideration all these parameter 20 kHz is selected as switching frequency.

### 5.2.4 High frequency transformer

For designing HFT, ferrite core is considered due to its high magnetic permeability and low electrical conductivity. Selection of specific core depends on operating power level (VA) and various other factors such as operating frequency \(f\), flux density \(B_m\), and current density \(J\) of the wire. Product area \(A_p\), core area \(A_c\), and window area \(A_w\) are calculated as,

\[
A_p = A_c \times A_w = \frac{VA}{2fB_mk_w}, \quad (36)
\]

where VA = 500 Watt, \(f = 20\) kHz, \(j = 2A/m^2\), \(k_w = 0.3\), and \(B_m = 0.2\) T. For these values of \(A_p\) is obtained as 10.4 cm\(^4\). Ferrite core E55/28/21 with \(A_p = 14.8\) cm\(^4\) is chosen for making HFT.

Number of turns are calculated as,

\[
N = N_p = N_c = \frac{V}{4fB_mA_c}, \quad (37)
\]

Considering maximum voltage of 150 V, number of turns are calculated as 26.5 approximated to 27. For transformer winding litz wires are used due to their low skin effect at higher frequency.

### 5.3 Current stress analysis

Power transfer in terms of input voltage \(V_{\text{DC}1}\) and load \(R\) can be derived as (38). Similarly, current stress for the proposed transistor clamped DAB and conventional DAB can be obtained as (39) and (40), respectively.

\[
P = \frac{\left(\frac{nV_{\text{DC}1}}{\omega L}\right)^2 R \left[\delta - \frac{\delta \varphi_1}{\pi} - \frac{\delta \varphi_2}{\pi}\right]^2, 0 < \delta \leq \varphi_1 \right]
\]

\[
|i_{L,\text{max}}^1| = \frac{V_{\text{DC}1}(\pi - \varphi_1 - \varphi_2) + \frac{n^2V_{\text{DC}1}R}{2\omega^2L^2}}{2\omega L} \times \left(\frac{\pi \delta - \delta \varphi_1 - \delta \varphi_2}{\pi} + \frac{2\delta}{\pi} + 1\right), 0 < \delta \leq \varphi_1
\]

\[
|i_{L,\text{max}}^2| = \frac{V_{\text{DC}1}(\pi - \varphi_1 - \varphi_2) + \frac{n^2V_{\text{DC}1}R}{2\omega^2L^2}}{2\omega L} \times \left(\frac{\pi \delta - \delta \varphi_1 - \delta \varphi_2}{\pi} + \frac{2\delta}{\pi} + 1\right), \quad \varphi_2 < \delta \leq \frac{\pi}{2}
\]

\[
|i_{L,\text{max}}^2| = \frac{\pi V_{\text{DC}1}}{2\omega L} + \frac{n^2V_{\text{DC}1}R}{2\omega^2L^2} \delta (\pi - \delta) \left(\frac{2\delta}{\pi} + 1\right), \quad (40)
\]

Figure 11(a) shows the comparison between conventional two-level DAB and proposed transistor clamped DAB for current stress variation with change in \(\delta\). Here, \(0 < \delta < \pi\) and \(\varphi_1 = \frac{\pi}{6}\) with \(\varphi_2\) fixed at \(\frac{11\pi}{36}\). It can be observed that with the increase in \(\delta\), power transfer increases, resulting into high current stress. In conventional DAB, it is not possible to control current stress because of the absence of any control parameter other than power angle \(\delta\). However, in the proposed converter, current stress can be easily regulated due to control variable \(\varphi_1\) and \(\varphi_2\). Figure 11(b) shows the variation of current stress with \(0 < \varphi_1 < \frac{\pi}{6}\), where \(\delta\) and \(\varphi_2\) are fixed at \(\frac{\pi}{5}\) and \(\frac{11\pi}{36}\), respectively. It depicts that the proposed transistor clamped DAB converter is having reduced current stress as compared to conventional two-level DAB over wide operating range. Parameters are taken same as that of laboratory prototype in Section 6.

The basic requirement for comparative analysis is that both conventional DAB and proposed converter must have same power transmission and voltage conversion ratio \(k\). The normalised transmission power \(\langle P \rangle\) for transistor clamped DAB is
\[ p = \frac{P}{P_N}, \]

\[ p = \begin{cases} 
\frac{4}{\pi^2}[\pi \delta - \delta \varphi_1 - \delta \varphi_2], & 0 < \delta \leq \varphi_1 \\
\frac{4}{\pi^2}[\pi \delta - \delta^2 - \varphi_1^2/2 - \delta \varphi_2], & \varphi_1 < \delta \leq \varphi_2 \\
\frac{4}{\pi^2}[\pi \delta - \delta^2 - \varphi_1^2/2 - \varphi_2^2/2], & \varphi_2 < \delta \leq \pi/2 
\end{cases} \]

Thus, the unified current stress \( G \) for the transistor clamped DAB topology can be obtained as

\[ G = \frac{V_{iL}}{2 \pi} = \frac{2}{\pi} \left[ k(\pi - \varphi_1 - \varphi_2) - \pi + 2\delta + 2\varphi_1 \right]. \]  

Unified current stress for conventional DAB and proposed converter can be given by (7) and (42), respectively.

With increase in voltage conversion ratio, current stress increases. Figure 12(a) shows the comparison between conventional two-level DAB and proposed transistor clamped DAB at different values of \( k \). Here, \( \pi > \delta > 0, \varphi_1 = \pi/6 \), and \( \varphi_2 = \frac{11\pi}{36} \).

In Figure 12(b), \( \pi > \varphi_1 > \frac{\pi}{6}, \delta = \frac{\pi}{5} \), and \( \varphi_2 = \frac{11\pi}{36} \). It can be observed that at each \( k \), the proposed converter has lesser current stress.

Figure 13 shows simulation results to verify the current stress for conventional DAB and proposed converter. \( V_{DC1}, V_{DC2} \) are 120 V, 48 V, respectively, at power transmission of 500W. Figure 13(a) and Figure 13(b) shows the simulation result for voltage and current waveform for conventional DAB and transistor clamped DAB topology, respectively. Figure 13(c) shows that current stress for proposed converter is lesser than that in conventional DAB which is further validated by laboratory prototype implementation.

### 5.4 Performance comparison

Performance of proposed transistor clamped DAB is compared with the conventional DAB when controlled with single phase shift (SPS), extended phase shift (EPS), dual phase shift (DPS), and triple phase shift (TPS) control techniques. Comparison is made in terms of parameters such as number of switches, voltage levels, degree of freedom (DoF), current stress, losses, and efficiency. For load of 200 W and 500 W which is 40% load and full load, respectively, for proposed converter, current stress, losses and efficiency are calculated as shown in Table 2.
FIGURE 13 Simulation result for (a) voltage and current waveform for conventional DAB. (b) Voltage and current waveform for proposed transistor clamped DAB. (c) Current stress comparison between conventional DAB and proposed transistor clamped DAB

TABLE 1 Switching states for proposed converter at primary side of HFT

| State | Output Voltage Level | Switching States |
|-------|----------------------|------------------|
|       | \( \frac{V_{DC}}{2} \) | \( S_1 \) \( S_2 \) \( S_3 \) \( S_4 \) \( S_5 \) |
| 1     | \( V_{DC} \)         | 0 1 0 0 1        |
| 2     | \( \frac{V_{DC}}{2} \) | 1 0 0 0 1        |
| 3     | 0                     | 0 0 1 0 1        |
| 4     | \( -\frac{V_{DC}}{2} \) | 1 0 0 1 0        |
| 5     | \( -V_{DC} \)         | 0 0 1 1 0        |

With SPS technique in conventional DAB, power is varied by changing phase shift only. Thus, it has only one degree of freedom (DoF) which confines its ability to regulate the power flow. When operated at light load and voltage conversion ratio differs from unity, its efficiency decreases due to more current stress.

In EPS technique, one more control parameter gets added apart from phase shift control. By changing inner phase shift of either primary or secondary side, power flow is regulated. For comparative analysis in EPS, \( \varphi_1 = \frac{\pi}{9} \) is considered as \( \frac{\pi}{\sqrt{3}} \). It improves the efficiency and reduces the current stress as compared to that of conventional DAB.

Conventional DAB when controlled by DPS technique has two control parameter known as inner phase shift ratio and outer phase shift ratio. Primary and secondary side H-bridges have same inner phase shift ratio. For comparison, \( \varphi_1 = \frac{\pi}{9} \) is considered for switches at both primary and secondary side. It leads to increase in efficiency and lesser current stress as compared to conventional DAB controlled by SPS technique.

In TPS technique, inner phase shift of both primary and secondary bridges are different. Considering outer phase shift and two inner phase shift, it has three control parameters. Similar to DPS, it also improves the efficiency at lighter load as compared to SPS technique. For the comparison, switching angle \( \varphi_1 \) for primary side and secondary side is taken as \( \frac{\pi}{9} \) and \( \frac{\pi}{18} \), respectively.

Despite of having one more switch, at 40% load, proposed converter has improvement of 10.81%, 5.67%, 3.52%, and 4.88% in efficiency as compared to conventional DAB controlled by SPS, EPS, DPS, and TPS techniques, respectively, due to reduced rms current and lesser conduction losses. Whereas at full load, the improvement in efficiency with the proposed converter is 3.48%, 1.17%, 1.03%, and 0.97% as compared to conventional DAB controlled by SPS, EPS, DPS, and TPS techniques, respectively. Moreover, current stress for proposed converter is 52.8% and 39.4% lesser as compared to conventional DAB controlled with SPS control technique at 40% and full load, respectively. Due to reduced current stress and ZVS operation, switching losses are also minimised.

5.5 Soft switching analysis

In order to obtain zero voltage switching (ZVS), parasitic capacitance must be discharged first then antiparallel diode conducts. As negative current flows through the body diode of switch, voltage across switch clamp to zero voltage which ensures ZVS operation. For conventional DAB, when operated with SPS control technique, at lighter load it suffer from hard switching of the secondary side. It is one of the major cause for reduced efficiency at lighter load and higher voltage conversion ratio [29].

At power of 200 W and 500 W, soft switching analysis is carried out as shown in Figure 14(a) and Figure 14(b), respectively. In order to verify ZVS operation of proposed transistor clamped DAB converter, from simulation study, all the parameters are taken same as that of converter prototype explained in Section 6. With voltage conversion ratio being 2.5 and at loading of 40% and full load, soft switching of switches are analysed. From Figure 14(a) and Figure 14(b), it can be observed that ZVS for all the switches except one switch (\( S_1 \)) of proposed converter are easily obtainable over entire load range. It ensures minimum switching losses and higher efficiency even at lighter load.
### TABLE 2  Performance comparison

| Parameters                                      | No of Switches | Voltage Level | DoF | Current Stress (A) | Losses (W) | Efficiency (%) |
|------------------------------------------------|----------------|---------------|-----|--------------------|------------|----------------|
|                                                 |                |               |     | 200 W              | 500 W      |                |
| DAB with single phase shift control            | 4              | 2             | 1   | 28.5               | 31.2       | 31.19 21.7     |
|                                                 |                |               |     | Conduction         | Switching  | 36.015 21.101  |
| DAB with extended phase shift control          | 4              | 2             | 2   | 23.4               | 26.9       | 19.834 17.63   |
|                                                 |                |               |     | Conduction         | Switching  | 24.55 18.56    |
| DAB with dual phase shift control              | 4              | 3             | 2   | 14.8               | 27.6       | 14.89 16.66    |
|                                                 |                |               |     | Conduction         | Switching  | 23.8 18.62     |
| DAB with triple phase shift control            | 4              | 3             | 3   | 17.5               | 27.2       | 17.5 17.75     |
|                                                 |                |               |     | Conduction         | Switching  | 23.9 18.01     |
| Proposed transistor clamped DAB                | 5              | 5             | 3   | 13.45              | 18.9       | 8.41 14.07     |
|                                                 |                |               |     | Conduction         | Switching  | 17.64 18.65    |
|                                                 |                |               |     | 200 W              | 500 W      | 89.89% 93.23%  |
|                                                 |                |               |     | 79.08% 89.75%      |
|                                                 |                |               |     | 84.24% 92.06%      |
|                                                 |                |               |     | 86.37% 92.2%       |
|                                                 |                |               |     | 85.01% 92.26%      |

**FIGURE 14**  Voltages across and currents through various switches under ZVS at primary and secondary side of HFT in proposed transistor clamped DAB. (a) at 40% loading (P = 200 W) and (b) at full load (P = 500 W)

### 6 IMPLEMENTATION OF TRANSISTOR CLAMPED DUAL ACTIVE BRIDGE DC–DC CONVERTER

Hardware prototype developed for the proposed transistor clamped dual active bridge dc–dc converter is as shown in Figure 15. All the electrical parameter’s specifications is provided in Table 3. Power MOSFET IRFPS37N50A are used for development of power circuit. For the generation of control pulses Xilinx Spartan-6 XC6SLX25 field programmable gate array (FPGA) board is used. It operates at frequency of 20 MHz. For verifying operation of the proposed converter, primary voltage is varied from 100 V to 150 V and secondary voltage is kept fixed at 48 V. Switching frequency f is 20 KHz and leakage inductance L is 33 µH. Without considering auxiliary switch, proposed converter can be made to operate as conventional two-level DAB, by employing only two H-bridges. It is unique feature of proposed converter.

With the increase in power, phase shift angle δ increases. In conventional two-level DAB power can only be regulated with δ due to one degree of freedom. As power increases, current stress increases. Figure 16(a) shows comparative analysis of current stress variation with change in δ for conventional two-level DAB and proposed converter. Due to three degrees of freedom in regulating power flow in proposed converter, its power flow controllability is wide. By regulating φ1 and φ2, current stress...
can easily be regulated. It can be observed that current stress for transistor clamped DAB is lesser as compared to conventional two-level DAB.

Increase in voltage conversion ratio $k$, results in increase in current stress. Figure 16(b) shows the comparative analysis between conventional two-level DAB and the proposed converter for current stress variation with change in voltage conversion ratio. It can be observed that conventional two-level DAB has more current stress as compared to proposed converter in whole operating region.

For validating efficacy of the proposed converter, power flow at 10%, 50%, and full load is obtained. For primary side DC link voltage of 120 V and secondary side DC link voltage of 48 V, switching angle $\varphi_1$ and $\varphi_2$ are kept fixed at 0.14$\pi$ and 0.305$\pi$, respectively.

The voltage and current waveform for conventional two-level DAB, is shown in Figure 17(a), whereas, Figure 17(b) shows the voltage and current waveform for the proposed transistor clamped DAB dc–dc converter with power transfer of 50 W and load resistance kept fixed at 46 $\Omega$. For conventional two-level DAB, voltages are of two levels and peak current is found to be 27.8 A. On the other hand, in the proposed converter primary voltage is of five-level and peak current is 11.35 A, which is only 40.8% of the peak current obtained in conventional DAB. Efficiency of conventional DAB and proposed transistor clamped DAB is found to be 48.93% and 70.36%, respectively. It shows that the efficiency of proposed converter is 21.43% higher than conventional DAB at 10% load.

Figure 18(a) and Figure 18(b) show the voltage and current waveforms for conventional two-level DAB and proposed transistor clamped DAB, respectively. For power transfer of 250 W, load resistance kept fixed at 9.2 $\Omega$. For conventional two-level
DAB, peak current is found to be 29.86 A. On the other hand, in the proposed converter, peak current is 14.40 A which is only 48.2% of the peak current obtained in conventional DAB. Efficiency of conventional two-level DAB and proposed transistor clamped DAB is found to be 82.48% and 91.08%, respectively. It shows that the proposed converter is 8.6% more efficient than the conventional DAB at 50% load.

Figure 19(a) and Figure 19(b) show the voltage and current waveform for conventional two-level DAB and the proposed transistor clamped DAB, respectively. At power transfer of 500 W, load resistance is kept fixed at 4.6 Ω. For conventional two-level DAB, peak current is found to be 32 A and for the proposed converter, peak current is 18.8 A which is only 58% of the peak current obtained in conventional DAB. The efficiency in conventional DAB and proposed DAB are 89.5% and 93.36%, respectively. It shows that the proposed converter is 3.86% more efficient than conventional two-level DAB at full load.

Loss comparison between conventional two-level DAB and the proposed transistor clamped DAB dc–dc converter is as shown in Figure 20. Transmission power is of 500 W with input voltage varying between 100 V and 150 V and output voltage is kept at 48 V to have different voltage conversion ratio. With increase in voltage conversion ratio, losses increases due to increase in current stress. In Figure 20, each bar corresponds to switching and conduction loss at particular voltage. In a single column, down side bar indicate conduction losses and upper side bar indicate switching losses. It can be observed from figure that despite having one extra switch as compared to conventional two-level DAB, proposed converter has lesser cumulative losses which causes increased efficiency of the converter.

Comparative analysis of efficiency between conventional two-level DAB and the proposed converter is as shown in Figure 21. As the voltage conversion ratio increases by varying input voltage from 100 V to 150 V, converter efficiency decreases due to increased current stress. Efficiency curve for different combination of \( \varphi_1 \) and \( \varphi_2 \) are different. In all the cases, efficiency of the proposed converter is higher than that of conventional two-level DAB. It can be observed that at input voltage of 150 V with \( \varphi_1 = 0.085 \pi \) and \( \varphi_2 = 0.25 \pi \), proposed converter has efficiency of 90%, whereas, conventional two-level DAB has efficiency of 82%. Over complete range proposed converter has high efficiency. This can be prominently noticed when voltage conversion ratio deviates largely from unity.

7 | CONCLUSION

In this paper, transistor clamped dual active bridge dc–dc converter is presented for medium and high voltage application. Comparative analysis between conventional two-level DAB and proposed converter is done to verify the current stress at different voltage conversion ratio. Detailed modelling is carried out to derive the power flow equation for the proposed converter. As compared to conventional two-level DAB, proposed converter has two additional control parameters (\( \varphi_1 \) and \( \varphi_2 \)) apart from phase shift angle (\( \delta \)) control for regulation of power flow and current stress. Thus, transistor clamped DAB has three degrees of freedom as compared to one degree of freedom in conventional two-level DAB. It was found that proposed converter has lesser current stress when voltage conversion ratio differ from unity. Furthermore, service life of switching devices can be prolonged due to lesser current stress and they can be selected with low stress level which will eventually reduces its cost. Loss calculation at different voltage conversion ratio over wide operating range is obtained. Proposed converter has significantly
lesser cumulative losses as compared to conventional two-level DAB. It is found that, despite of having one extra switch, it has higher efficiency. Moreover, due to five-level voltage on primary side of HFT, voltage stress will be reduced. Performance of the proposed converter is significantly improved at higher voltage conversion ratio and light load. The performance of the proposed converter is validated via simulation and experimentation on developed laboratory prototype.

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