An IoT Endpoint System-on-Chip for Secure and Energy-Efficient Near-Sensor Analytics

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Abstract—Near-sensor data analytics is a promising direction for IoT endpoints, as it minimizes energy spent on communication and reduces network load. However, performing feature extraction or classification directly on the end-nodes poses security concerns, as valuable data, distilled with application knowledge, is stored or sent over the network at various stages of the analytics pipeline. Using encryption to protect sensitive data at the boundary of the on-chip analytics engine is a way to address data security issues. To cope with the combined workload of analytics and encryption in a tight power envelope, we propose Fulmine, a System-on-Chip based on a tightly-coupled multi-core cluster augmented with specialized blocks for compute-intensive data processing and encryption functions, supporting software programmability for regular computing tasks. The Fulmine SoC, fabricated in 65 nm technology, consumes less than 20 mW on average at 0.8 V achieving an efficiency of up to 70 pJ/B in encryption, 50 pJ/px in convolution, or up to 25 MIPS/mW in software. As a strong argument for real-life flexible application of our platform, we show experimental results for three secure analytics use cases: secure autonomous aerial surveillance with a state-of-the-art deep CNN consuming 3.16 pJ per equivalent RISC op; local CNN-based face detection with secured remote recognition in 5.74 pJ/op; and seizure detection with encrypted data collection from EEG within 12.7 pJ/op.

Index Terms—Secure Internet-of-Things, Cryptography, Convolutional Neural Networks, System-on-Chip, Heterogeneous Computing

I. INTRODUCTION

The key driver for the development of the Internet-of-Things (IoT) is collecting rich and diverse information streams from sensors, which can then be fed to state-of-the-art learning-based data analytics algorithms. The information distilled by data analytics on such a rich input set can be used in a virtually unlimited set of applications, such as healthcare or home automation, which have the possibility to change the life of any person for the better [1]. However, in practice, the possibility to seamlessly tap into this rich stream of data is limited by two equally important factors. First, the amount of data an IoT end-node can extract from sensors and send over the network for analytics is essentially defined by the energy necessary for data transfer itself. Since IoT end-nodes must work within a tiny power envelope, this fact introduces a significant limit on the volume of data that can be transferred, e.g. the size of captured images, therefore curtailing their usefulness. Second, due to the ubiquitous nature of IoT devices, they often deal with private or safety critical input data even beyond the predictions of their designers; not only devices such as healthcare wearables acquire potentially safety-critical data, but also seemingly innocuous devices (such as cameras) can potentially acquire highly sensitive information [2]. To ensure practicality of IoT-based applications, it is imperative that data transmission from end-nodes to the network is protected from data theft or malicious tampering.

To address the first limiting factor, near-sensor smart data analytics is a promising direction; IoT end-nodes must evolve from simple data collectors and brokers into analytics devices, able to perform a pre-selection of potentially interesting data and/or to transform it into a more abstract, higher information density form such as a classification tag. With the burden of sensemaking partially shifted from centralized servers to distributed end-nodes, the energy spent on communication and the network load can be minimized effectively and more information can be extracted, making the IoT truly scalable. However, performing analytics such as feature extraction or classification directly on end-nodes does not address the security concerns. It worsens them: distilled data that is stored or sent over the network at several stages of the analytics pipeline is even more privacy-sensitive than the raw data stream [3], [4]. Protecting sensitive data at the boundary of the on-chip analytics engine is a way to address these security issues; however, cryptographic algorithms come with a significant workload, which can easily be of 100-1000s of processor instructions per encrypted byte [5].

This security workload is added to the computational effort imposed by leading feature extraction and classification algorithms, such as deep Convolutional Neural Networks (CNNs). CNNs are extremely powerful in terms of data analytics, and state-of-the-art results in fields such as computer vision (e.g. object detection [6], scene parsing [7], and semantic segmentation tasks [8]) and audio signal analytics [9] have been demonstrated. While effective, deep CNNs usually necessitate many billions of multiply-accumulate operations, as well as storage of millions of bytes of pre-trained weights [10]. The combined workload necessary to tackle these two limitations to the development of smarter IoT - namely, the necessity for near-sensor analytics and that for security - is formidable, especially under the limited available power envelope and the tight memory and computational constraints of deeply embedded devices. One possible solution is to augment IoT end-nodes with specialized blocks for compute-intensive data processing and encryption functions while retaining full software programmability to cope with lower computational-intensity tasks. Specialized processing engines should be tightly integrated both with the software-programmable cores and with one another, streamlining the process of data exchange between the different actors as much as possible to minimize the time and energy spent in data exchange; at the same time, to simplify their usage from the developer’s perspective, it should be possible to abstract them, integrating them in standard programming models used in software development for IoT-aware platforms.
In this work, we propose the 65 nm *Fulmine secure data analytics System-on-Chip* (SoC), which tackles the two main limiting factors of IoT end-nodes while providing full programmability, low-effort data exchange among processing engines, (sufficiently) high speed, and low energy. The SoC is based on the architectural paradigm of tightly-coupled heterogeneous shared-memory clusters\(^1\), where several engines (which can be either programmable cores or specialized hardware accelerators) share the same first-level scratchpad via a low-latency interconnect. In *Fulmine*, the engines are four enhanced 32-bit OpenRISC cores, one highly efficient cryptographic engine for AES-128 and KECCAK-based encryption, and one multi-precision convolution engine specialized for CNN computations. Due to their memory sharing mechanism, cores and accelerators can exchange data in a flexible and efficient way, removing the need for continuous copies between cores and accelerators. The proposed SoC performs computationally intensive data analytics workloads with no compromise in terms of security and privacy, thanks to the embedded encryption engine. At the same time, *Fulmine* executes full complex pipelines including CNN-based analytics, encryption, and other arbitrary tasks executed on the processors.

This claim is exemplified in three practical use cases: secure autonomous aerial surveillance in a nano-Unmanned Aerial Vehicle (nano-UV) consuming 3.16 pJ per equivalent RISC operation; on-device CNN-based face detection (as part of a recognition pipeline) with 5.74 pJ per operation, including image encryption for external face recognition; and seizure detection with secure data collection within 12.7 pJ per operation. We show that on a workload consisting of balanced contributions from CNNs, AES, and other SW-implementable filters, *Fulmine* provides the best result in terms of pJ-per-equivalent-RISC-operation, with the nearest state-of-the-art more than 89× more time to execute the workload.

The rest of this paper is organized as follows: Section II details the architecture of the *Fulmine* SoC and its main computing blocks. Section III evaluates the SoC implementation results and the performance on synthetic benchmarks, while Section IV reports results collected over a set of real-world use cases. In Section V, we compare and contrast *Fulmine* with the current state-of-the-art in low-power IoT computing devices. Section VI concludes the paper.

### II. SoC Architecture

The *Fulmine* multi-core System-on-Chip (Figure 1) implements a secure near-sensor data analytics architecture, which leverages highly efficient processors for software programmable signal processing and control, flexible hardware accelerator for cryptographic functions, convolutional neural networks, and a highly optimized subsystem implementing power management and efficient communication and synchronization among cluster resources. The architecture, based on the PULP platform\(^1\) is organized in two distinct voltage and frequency domains, cluster and SoC, communicating through an AXI4 interconnect and separated by dual-clock FIFOs and level shifters. Two frequency-locked loops (FLLS) are used to generate clocks for the cluster and the rest of the SoC, while the two domains rely on external voltage regulators for power supply.

Fig. 1: *Fulmine* SoC architecture. The SoC domain is shown in shades of blue, the cluster domain in shades of green.

The cluster domain is built around six processing elements (four general-purpose processors and two flexible accelerators) that share 64 kB of level 1 Tightly-Coupled Data Memory (TCDM), organized in eight word-interleaved SRAM banks. A low-latency logarithmic interconnect\(^3\) connects all processing elements to the TCDM memory, enabling fast and efficient communication among the resources of the cluster. The TCDM interconnect supports single-cycle access from multiple processing elements to the TCDM banks; if two masters attempt to access the same bank in the same clock cycle, one of them is stalled using a starvation-free round-robin arbitration policy. The two hardware accelerators, *Hardware Cryptography Engine* (HWCRYPT) and *Hardware Convolution Engine* (HWCE), can directly access the same TCDM used by the cores. This architecture allows data to be seamlessly exchanged between cores and accelerators, without requiring explicit copies and/or point-to-point connections. To avoid a dramatic increase in the area of the TCDM interconnect, as well as to keep the maximum power envelope in check, the two accelerators share the same set of four physical ports on the interconnect. The two accelerators are used in a time-interleaved fashion, allowing one accelerator full access to the TCDM at a time, which is suitable for data analytics applications where computation can be divided into several separate stages.

The four OR10N cores are based on an in-order, single-issue, four stage pipeline, implementing the OpenRISC\(^4\) instruction set architecture (ISA), improved with extensions for higher throughput and energy efficiency in parallel signal processing workloads\(^5\). GCC 4.9 and LLVM 3.7 toolchains are available for the cores, while OpenMP 3.0 is supported on top of the bare-metal parallel runtime. The cores share a single instruction cache of 4 KB of Standard Cell Memory (SCM)\(^6\) that can increase energy efficiency by up to 30% compared to an SRAM-based private instruction cache on parallel workloads\(^7\). The ISA extensions of the core include general-purpose enhancements (automatically inferred by the compiler), such as zero-overhead hardware loops and load and store operations embedding pointer arithmetic, and other DSP extensions that can be explicitly included by means of *intrinsic* calls. For example, to increase the number of effective operations per cycle, the core includes single instruction multiple data (SIMD) instructions working on 8 bit and 16 bit

\(^{1}\)http://www.pulp-platform.org
data, which exploit 32-bit registers as vectors. Furthermore, the core is enhanced with a native dot-product instruction to accelerate computation-intensive classification and signal-processing algorithms. This single-cycle operation supports both 8-bit and 16-bit vectors using two separate data paths to reduce the timing pressure on the critical path. Fixed point numbers are often used for embedded analytics and signal processing applications; for this reason, the core has also been extended with single-cycle fixed point instructions including rounded additions, subtractions, multiplications with normalization, and clipping instructions.

The cluster features a set of peripherals including a direct memory access (DMA) engine, an event unit, and a timer. The processors can access the control registers of the hardware accelerators and of the other peripherals through a memory-mapped interface implemented as a set of private, per-core demultiplexers (DEMUX), and a peripheral interconnect shared among all cores. Latency-critical peripherals such as the event unit and the DMA are directly connected to the DEMUXes, thereby guaranteeing very low latency access (i.e. one cycle) and eliminating contention when accessing their control ports. The other peripherals are mapped on the peripheral interconnect through an additional pipeline stage to remove them from the critical path of the core. As hardware accelerators can be busy executing jobs for hundreds to thousands of cycles with no or little need for interaction, their control ports are accessed through this lower-priority path. The peripheral interconnect implements the same architecture of the TCDM interconnect, featuring a different addressing scheme to provide 4 kB of address map for each peripheral.

The DMA controller available in the cluster is an evolution of the one presented in [13], and enables fast and flexible communication between the TCDM and the L2 memory through four dedicated ports on the TCDM interconnect and an AXI4 plug on the cluster bus. The DMA has a set of private per-core command FIFOs accessed through the DEMUXes that converge on a larger global command queue through a round robin arbiter. Hence, all the cores within the cluster can asynchronously and concurrently push transfers to the control ports, avoiding the usage of inefficient software locks to guarantee mutual access to the DMA internal resources. Moreover, in contrast to traditional memory mapped interfaces, access to the internal DMA programming registers is implemented through a sequence of control words sent to the same address, significantly reducing DMA programming overheads (i.e. less than 10 cycles to initiate a transfer, on average). The DMA supports up to 16 outstanding 1D or 2D transfers to hide L2 memory latency and allows 256 byte bursts on the 64-bit AXI4 interface to guarantee high bandwidth. Once a transfer is completed, the DMA generates an event to the cores that can independently synchronize on any of the enqueued transfers by checking the related transfer ID on the DMA control registers. Synchronization of DMA transfers and hardware accelerated tasks is hardware-assisted by the event unit. The event unit can also be used to accelerate the typical parallelization patterns of the OpenMP programming model, requiring, for example, only 2 cycles to implement a barrier, 8 cycles to open a critical section, and 70 cycles to open a parallel section. These features are all essential to guarantee high computational efficiency during execution of complex tasks such as CNNs in *Fulmine*, as detailed in section II-D.

The SOC domain contains 192 kB of L2 memory for data and instructions, a 4 kB ROM, a set of peripherals, and a power management unit. Furthermore, the SOC includes a (quad) SPI master, I2C, I2S, UART, GPIOs, a JTAG port for debug, and a (quad) SPI slave that can be used to access all the SoC internal resources. An I/O DMA subsystem (uDMA) allows to autonomously copy data between the L2 memory and the external interfaces, even when the cluster is in sleep mode. This mechanism allows us to relieve cores from the frequent control of peripherals necessary in many microcontrollers, and to implement a double buffering mechanism both between IOs and L2 memory and between L2 memory and TCDM. Therefore, I/O transfers, L2 memory to TCDM transfers, and computation phases can be fully overlapped.

### A. Power and Clock Management

A sophisticated power management architecture distributed between the SOC and CLUSTER domains can completely clock-gate all the resources when idle, as shown in Figure 2. The event unit is responsible for automatically managing the transitions of the cores between the active and idle state. Processors are put in idle by reading a configuration register of the event unit through their private port (mapped on the DEMUX). This happens when the processors execute an explicit Wait For Event instruction, for example during a synchronization barrier or after a DMA transfer. The processors are then stalled by the event unit, and once all pending transactions (e.g., cache refills) are complete, they are clock-gated.

A clock gate management unit probes the state of all engines of the cluster: the processors, the hardware accelerators, and the DMA. If none of the resources are busy, the SoC power manager is notified. It reacts accordingly to the policy stored in its configuration register: it gates the cluster clock if the idle mode is selected, or it activates the handshaking mechanism with the external regulator to power gate the cluster if the

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**TABLE I: *Fulmine* power modes.**

| Power Mode | Clock [MHz] | FLL Wakeup Power [µW] | Power Clock FLL Wakeup Power [µW] |
|------------|-------------|------------------------|-----------------------------------|
| active hi-freq | 50 ON N/A | 300 230 | 50 ON N/A |
| active low-freq | 0.1 OFF 300 210 | 0.1 OFF 300 130 | |
| idle | OFF 300 20 120 | OFF ON 300 120 |
| deep sleep | OFF OFF a <0.01 b OFF OFF 300 120 |

a Depends on DC/DC settling time.
b The CLUSTER domain is power-gated with external DC/DC in shutdown.
B. Hardware Encryption Engine

The Hardware Encryption Engine (HWCRYPT), as shown in Figure 3, implements a dedicated acceleration unit for a variety of cryptographic primitive operations, exploiting the advantages of the shared memory architecture of the SoC. The HWCRYPT is based on two parallel cryptographic engines, one implementing the AES-128 [19] block cipher and the other one implementing the one implementing the AES-128 [19] block cipher and the HWCRYPT is based on two parallel cryptographic engines, advantages of the shared memory architecture of the SoC. The in Figure 3, implements a dedicated acceleration unit for a

**Fig. 3: HWCRYPT datapath overview, with details of the AES-128 and the sponge engine.**

deep-sleep mode is selected. Once the wake-up event reaches the power management unit, the latter reactivates the cluster, then it forwards the event notification to the event unit, waking up the destination core. SOC and CLUSTER events can be generated by all SoC peripherals (including GPIOs), by hardware accelerators, by the DMA, by the cluster timer, or by processors through the configuration interface of the event unit mapped in the peripheral interconnect. Table I reports all the power modes along with their average wakeup time and power consumption, divided between the CLUSTER and SOC domains.

A programmable frequency-locked loop (FLL) with an external reference clock of 0.1 MHz is used for each domain of Fulmine. The FLL supports a fast frequency switch between different operating modes for the cluster, and in the worst case is able to complete the frequency switch in less than 10 cycles of the reference clock. To perform the switch, the cluster is first put in sleep mode, then woken up again when the FLL locks. As sleep and wakeup can employ the fast mechanism previously described, the frequency switch can be performed in as little as 10 μs.

The initial tweak $T_0$ is computed by encrypting the sector number $SN$, derived from the address of the data, using the encryption key $K_1$ and multiplying it with $\alpha^i$ with $i = 0$. The multiplication with $\alpha^i$ ensures that the tweak is different for each block. The depicted XTS mode in Figure 4a is represented in a mathematical form in Equation 1.

$$T_i = E_{K_1}(SN) \otimes \alpha^i$$

$$C_i = E_{K_2}(P_i \oplus T_i) \otimes T_i$$

The address-dependent tweak $T_i$ is derived by a multiplication between the initial tweak and $\alpha^i$. The multiplication is performed in the finite field or Galois field GF$(2^{128})$ defined by the irreducible polynomial $x^{128} + x^7 + x^2 + x + 1$.

AES-128-XTS requires a 128-bit finite field multiplier and exponentiator, which is rather complex in terms of VLSI implementation. To reduce this complexity, we first observe that $\alpha$ is constant with the recommended value $\alpha = 2$. We can derive the tweak for the current block sequentially as a function of the previous tweak $T_{i-1}$, turning the exponentiation into a sequential multiplication by two as shown in Equation 2.

$$T_i = T_{i-1} \otimes 2$$

A finite field is a finite set of elements supporting different operations and can be defined by a polynomial. $\alpha$ is one of the recommended constants (2 or 3), and $i$ is the relative address within the chunk to be encrypted. $\otimes$ denotes the 128-bit finite field multiplication in which also the exponentiation is performed.
In the finite field GF\(\left(2^{128}\right)\), a multiplication by two is much simpler and can be realized with a shift by one to the left with a conditional XOR with the irreducible polynomial.

The sponge engine implements two instances of the KECCAK-\(f[400]\) permutation, each based on three permutation rounds. KECCAK-\(f[400]\)’s architecture is optimized to match the length of the critical path of the AES-128 engine. Permutations support a flexible configuration of the rate and round parameters. The rate defines how many bits are processed within one permutation operation, and it can be configured from 1 bit to 128 bits in powers of two. This parameter supports a trade-off between security and throughput. The more bits are processed in one permutation call, the higher the throughput - but with a cost regarding the security margin of the permutation. The round parameter configures the number of KECCAK-\(f[400]\) rounds applied to the internal state. It can be set up as a multiple of three or for 20 rounds as defined by the specification of KECCAK-\(f[400]\). The two instances of permutations are combined to implement an authenticated encryption scheme based on a sponge construction with a prefix message authentication code that additionally provides integrity and authenticity on top of confidentiality. In Figure 4b, we show the sponge construction for encryption. Initially, the state of the sponge is filled with the key \(K\) and the initial vector \(IV\). After executing the KECCAK-\(f[400]\) permutation \(p\), we sequentially squeeze an encryption pad and apply the permutation function to encrypt all plaintext blocks \(P_i\) via an XOR operation.

Apart from this favorable mode of operation, the sponge engine also provides without authentication and direct access to the permutations to allow the software to accelerate any KECCAK-\(f[400]\)-based algorithm.

The HWCRYPT utilizes two 32 bit memory ports of the TCDM interconnect, while an internal interface performs the conversion from 32 bit to the 128 bit format used by the encryption engines. The system is designed so that memory interface bandwidth matches the requirements of all cipher engines. The HWCRYPT is programmed and started through a wrapper that connects and decouples the datapath streaming domain from the memory-based cluster; and a controller that provides a control interface for the accelerator. In the full-precision 16 bit mode, the sum-of-products datapath is used to perform a convolution between a preloaded filter \(W\) (stored in a weight buffer) and a \(5 \times 5\) window extracted from a linear \(x\) input feature map stream. Window extraction is performed by a line buffer, which is realized with latch-based SCMs for optimized energy efficiency. The line buffer is composed by a set of FIFO queues with two read pointers: one to implement the mechanism to pass the oldest pixel to the next FIFO and the other to extract the \(5 \times 5\) sliding window. The output of the sum-of-products is summed to an input pre-accumulated \(y_{in}\) value; in other words, the accelerator needs no internal memory to perform the feature map accumulation component of Equation 5 but uses directly the shared memory of the cluster. The wrapper, shaded in green in Figure 5, is responsible for generating memory accesses through four memory ports to the TCDM to feed the accelerator \(x, y_{in}\) streams and write back \(y_{out}\) (partial) results. The controller (red in Figure 5) contains a register file which can host a queue of two jobs, each consisting of pointers to \(x, W, y\), strides for the wrapper address generators, and other configuration such as the number of fractional bits to use. The controller is mapped in the cluster peripheral interconnect.

To support three different possible sizes for weights, the HWCE sum-of-products datapath must be able to perform 16 bit \(\times\) 16 bit products as well as 8 bit \(\times\) 16 bit and 4 bit \(\times\) 16 bit ones. The two or four filters hosted in the weight buffer in scaled precision modes are not consecutive, but they are interleaved: in full precision mode a location represents a single 16 bit weight; in the scaled precision modes, it represents two 8 bit or four 4 bit weights. The sum-of-products datapath is designed in a hierarchical way to maximize its reuse between the three configurations. Four submodules (shown in orange in Figure 5) compute the sum-of-products of \(x_{win}\) with a 4 bit slice of \(W\) each, using a set of signed multipliers and a first-stage reduction tree. A second-stage reduction tree and a set of multiplexers are used to combine these four partial sum-of-products to produce one, two or four concurrent \(y_{out}\) outputs; fractional part normalization and saturation are

\[ y(k_{out}) = b(k_{out}) + \sum_{k_{in}=0}^{N_{af}-1} \left( W(k_{out}, k_{in}) \ast x(k_{in}) \right). \]
also performed at this stage. As multiple accumulations of convolutions are performed concurrently, the $y_{in}$ and $y_{out}$ streamers are replicated four times. All HWCE blocks are aggressively clock gated so that each component consumes power only when in active use.

D. Shared-Memory Software/Hardware Cooperation

The shared-memory architecture of the HWCRIPT and HWCE accelerators enables efficient zero-copy data exchange with the cores and the DMA engine, while the event unit can be leveraged to efficiently switch computation from cores to accelerators and vice-versa and/or to trigger data transfers to/from the L2. These features, together with a highly optimized software runtime, are essential to guarantee a high level of programmability and highly efficient execution of complex tasks such as CNNs, which require complex computation patterns, frequent memory transfers for data set tiling, and synchronization between all the processing elements to implement efficient parallelization.

A typical application running on the Fulmine SoC operates conceptually in the following way. First, the input set (e.g. a camera frame) is loaded into the L2 memory from an external I/O interface using the uDMA. The cluster can be left in sleep mode during this phase and woken up only at its conclusion. The input set is then divided into tiles of appropriate dimension so that they can fit in the L1 shared TCDM; one tile is loaded into the cluster, where a set of operations are applied to it either by the SW cores or the HW accelerators. These operations can include en-/decryption and convolutions (in HW), plus any SW-implementable filter. The output tiles are then stored back to L2 memory using DMA transfers, and computation continues with the next tile. Operations such as DMA transfers can typically be overlapped with computation by using double buffering to reduce the overall execution time.

Cores are used both for actual computation on the data set and for control; to avoid inefficient busy waiting, events are employed by the HW accelerators to notify completed execution. Accelerator events trigger an appropriate interrupt in the controller core while it is either in sleep and clock-gated, or executing a filter of its own in parallel to HW-accelerated computation. For example, a secured convolutional layer of a CNN can comprise full decryption of all inputs, accumulation of convolutions, pooling, non-linear activation and encryption of all outputs, requiring both accelerator control and software-based computation.

III. EXPERIMENTAL EVALUATION

In this Section, we analyze measured performance and efficiency of our platform on the manufactured Fulmine prototype chips, fabricated in UMC 65 nm LL 1P8M technology. Figure 6 shows a microphotograph of a manufactured Fulmine chip, which occupies an area of 2.62 mm×2.62 mm.

A. System-on-Chip Operating Modes

An important constraint for the design of small, deeply embedded systems such as the Fulmine SoC is the maximum supported power envelope. This parameter is important to select the system battery and the external DC/DC converter. To maximize energy efficiency, the worst case for the DC/DC converter (i.e. the peak power) should not be too far from the average working power to be delivered. However, a SoC like Fulmine can operate in many different conditions: in pure software, with part of the accelerator functionality available, or with both accelerators available. These modes are characterized by very different average switching activities and active power consumption.

During the design of the Fulmine SoC, three distinct operating modes were defined, enabling to choose the right combination of active cores and accelerators in an application-driven fashion. When an application is run entirely in software, it is often useful to push frequency as much as possible to maintain a performance constraint. Conversely, execution on
accelerator cores is orders of magnitude faster than software, and it can be executed at a relaxed operating frequency with less overall cluster power consumption. Moreover, some of the internal accelerator datapaths are not easily pipelined, as adding pipeline stages severely hits throughput - this is the case of the HWCRYPT sponge engine (Section II-B), which relies on tight loops of KECCAK-f[400] rounds as visible in the datapath in Figure 7. Relaxing these paths can improve the overall synthesis results for the rest of the circuit.

Multi-corner multi-mode synthesis and place & route were used to define three operating modes: in the CRY-CNN-SW mode, all accelerators and cores can be used. In the KEC-CNN-SW mode, cores and part of the accelerators can be used: the HWCE fully, the HWCRYPT limited to KECCAK-f[400] primitives. In this mode, the frequency can be pushed significantly further than in the CRY-CNN-SW mode. Finally, in the SW mode, only the cores are active, and the operating frequency can be maximized. Figure 7 shows frequency scaling in the three operating modes while varying the cluster operating voltage $V_{DD}$. The three modes were designed so that at $V_{DD} = 1.2\, V$, current consumption under full load is close to 100 mA (i.e., 120 mW of power consumption), as can be seen in Figure 7.

\section*{B. HWCRYPT Performance and Power Evaluation}

Due to a throughput oriented hardware implementation, HWCRYPT achieves a significant acceleration compared to an optimized software implementation running on the OpenRISC cores. To encrypt one 8kB block of data using the AES-128-ECB mode, HWCRYPT requires $\sim 3100$ clock cycles including the initial configuration of the accelerator. This is a 450× speedup compared to a software implementation on one core. When parallelizing the software implementation to all four cores, the hardware accelerator still reaches a speedup of 120×. The throughput of HWCRYPT in AES-128-ECB mode is 0.38 cycles per byte (cpb).

The performance of the AES-128-XTS mode is the same with respect to the ECB mode, thanks to parallel tweak computation and encryption. When comparing that to an optimized software implementation on a single core, this speeds up the throughput by a factor of 495× and by a factor 287× when running on four cores. It is important to note that, contrarily to the ECB mode, XTS encryption cannot be efficiently parallelized in software due to a data dependency during the tweak computation step.

The authenticated encryption scheme based on KECCAK-f[400] achieves a throughput of 0.51 cpb by utilizing both permutation instances in parallel. The first permutation encrypts the data and the second one is used to compute the message authentication code to provide integrity and authenticity. This performance is achieved in a maximum-rate configuration of 128 bit per permutation call and 20 rounds as specified by KECCAK-f[400]. Reducing the rate and/or increasing the number of invoked permutations decreases the throughput while increasing the security margin.

In Figure 8a, we present the performance of HWCRYPT in terms of time and energy per byte, while scaling the $V_{DD}$ operating voltage of the cluster. When normalizing these values to the power consumption, we reach a performance of 67 Gbit/s/W for AES-128-XTS and 100 Gbit/s/W for KECCAK-f[400]-based authenticated encryption respectively.

\section*{C. HWCE Performance and Power Evaluation}

The Fulmine SoC includes many distinct ways to perform the basic operation of CNNs, i.e., 2D convolutions. In software, a naive single core implementation of a 5×5 convolution filter has a throughput of 94 cycles per pixel. Parallel execution on four cores can provide almost ideal speedup reaching 24 cycles/pixel. Thanks to the SIMD extensions described in Section II, an optimized multi-core version can be sped up by almost 2× down to 13 cycles/pixel on average.

With respect to this baseline, the HWCE can provide a significant additional speedup by employing its parallel dat-
apath, the line buffer (which saves input data fetch memory bandwidth), and weight precision scaling. We measured average throughput by running a full-platform benchmark, which therefore takes into account the overheads for real world usage: line buffer fill time, memory contention from cores, self-contention by HWCE inputs/outputs trying to access the same TCDM bank in a given cycle. Considering the full precision 16 bit mode for the weights, we measured an average inverse throughput of 1.14 cycles per output pixel for 5×5 convolutions and 1.07 cycles per output pixel for 3×3 convolutions - the two sizes directly supported by the internal datapath of the HWCE. This is equivalent to a 82× speedup with respect to the naïve single core baseline, or 11× with respect to a fully optimized 4-core version.

As described in Section II-C, the HWCE datapath enables application-driven scaling of arithmetic precision in exchange for higher throughput and energy efficiency. In the 8-bit precision mode, average inverse throughput is scaled to 0.61 cycles/pixel and 0.58 cycles/pixel for the 5×5 and 3×3 filters, respectively; in 4-bit mode, this is further improved to 0.45 cycles/pixel and 0.43 cycles/pixel, respectively. In the 4-bit precision mode, the HWCE is fully utilizing its 4-port memory bandwidth towards the TCDM in order to load 4 y_in partial results and store back 4 y_out ones. Further performance scaling would therefore require an increase in memory bandwidth.

Figure 8b reports time and energy per pixel, running the same set of filters in the KEC-CNN-SW operating mode while scaling the V_{PD} operating voltage. At 0.8 V, the energy to spend for an output pixel can be as low as 50 pJ per pixel, equivalent to 465 GMAC/s/W for a 5×5 filter.

IV. USE CASES

To evaluate the Fulmine SoC in full end-to-end applications, we consider three distinct use cases, representative of a wider set of possible applications for secure analytics in the IoT domain. We consider secure surveillance on a fully autonomous aerial vehicle based on a complex state-of-the-art CNN (ResNet-20 [10]); a smartwatch-based secure authentication using local face detection and remote cloud-based recognition, based on a smaller CNN [29]; and seizure detection based on principal component analysis and wavelet transform [30], with secure data collection for further analysis. The proposed use cases are not intended to exhaust the space for applications of the presented SoC, but to explain how the architectural features of Fulmine can be used to make advanced secure analytics capabilities feasible in small low-power computing end-nodes.

For our evaluation, we consider the system shown in Figure 9. To be able to work on state-of-the-art analytics based on deep learning, the Fulmine SoC is connected to low-power memory and Flash storage. We use two banks (16 MB) of Microchip SST26VF064B 512 kB Flash memory and FRAM and SPI traffic could be monitored or modified by using an Advanced SoCV95000 integrated circuit tester. We focus on the power spent for actual computation rather than on system power. We intend this in a broad sense, including e.g. power spent in memory transfers to/from flash and FRAM that are necessary for the computation itself, but excluding power spent for data acquisition and transmission, which are clearly separated from the computation phase. For the two external memories, we used publicly available data from their datasheets, considering worst case power whenever appropriate.

A. Secure Autonomous Aerial Surveillance

For the secure autonomous aerial surveillance use case, we consider deploying the system of Figure [9] on a low-power nano-UAV such as a CrazyFlie nano quadcopter [31]. Storms of tens or hundreds of these devices could provide diffused, fully autonomous, and low energy footprint aerial surveillance. Continuous data transmission from onboard cameras to a centralized surveillance server for analysis would require significant power from the limited UAV battery and reduce the overall flight time. Moreover, being fully dependent on wireless transmission might be detrimental from the UAV reliability viewpoint, especially in situations such as disaster recovery where UAV storms might otherwise be used with success. A sensible choice is therefore to perform part of the surveillance analysis directly on the UAVs, and then send it to the collecting server in the cloud. This saves energy and increases reliability, as collected labels are synthetic and can be collected for some time on the device if the wireless connection is temporarily unavailable. The power budget for computing on this category of aerial vehicle is extremely limited, as more than 90% of the battery must be dedicated to the quadrotor engines.

An additional constraint if one wants to use deep CNNs of medium and large size is that they require external memory for storage of weights and partial results. These memories cannot be considered to be secure. First, the weights deployed in the flash memory can be considered an important intellectual property and therefore need to be protected. Second, as the UAVs are fully autonomous, they are potentially vulnerable to malicious physical hijacking. Partial results stored in the FRAM and SPI traffic could be monitored or modified by an external agent, with the purpose of changing the final result classified by the UAV. Strong encryption for weights and partial results can significantly alleviate this issue, at the
cost of a huge overhead on top of the pure data analytics workload.

To model this use case, we consider a deep ResNet-20 CNN to classify scenes captured from a low power sensor producing a 224×224 input image. ResNet-20 has been shown to be effective on CIFAR-10 classification but can also be trained for other complex tasks. It consists of more than 1.35×10⁹ operations, a considerable workload for a low power end-node. It also requires using external memories for both weights (with a footprint of 8.9 MB considering 16 bits of precision) and partial results (with a maximum footprint of 1.5 MB for the output of the first layer). On top of this, all weights and partial results are en-/decrypted with AES-128-XTS; the Fulmine cluster is considered the only secure enclave in which decrypted data can reside.

Figure 10 shows execution time and energy spent at 0.8 V for this compound workload. We exploit the fast frequency switching capabilities of Fulmine described in Section II-A to dynamically switch from the CRNN-CNNSW operating mode (at 85 MHz) when executing AES to the KEC-CNNSW operating mode (at 104 MHz) when executing other kernels. The figure also shows a breakdown of energy consumption regarding kernels (convolution, encryption), other components of the CNN, DMA transfers, and external memories. In the baseline, where all the workload is run in software on a single core, energy consumption is entirely dominated by convolutions and encryption, with a 4-to-1 ratio between the two. When more features of the Fulmine SOC are progressively activated, execution time is decreased by 114× and energy consumption by 45×, down to 27 mJ in total - 3.16 pJ per equivalent elementary operation. When CNNs use the HWCE with 4 bit weights and AES-128-XTS uses the HWCrypt, the overall energy breakdown shows that cluster computation is no longer largely dominant, counting for only slightly more than 50% of the total energy. The energy expense for weights is decreased by using lower arithmetic accuracy weights, but the FRAM for partial results accounts for more than 30% of the total energy spent. Additional acceleration would likely require expensive hardware (e.g. more sum-of-products units or more ports in the HWCE) and would therefore yield diminishing returns in terms of energy efficiency.

To concretely estimate whether the results make it feasible to deploy a ResNet-20 on a nano-UAV, consider that a CrazyFlie UAV [31] can fly for up to 7 minutes. Continuous execution of secure ResNet-20 during this flight time corresponds to a total of 235 iterations in the operating point considered here. This would consume a total of 6.4 J of energy - less than 0.25% of the 2590 J available in the onboard battery. Together with peak power consumption, which is less than 24 mW, this result constitutes a strong argument in favor of the effectiveness of the platform we propose for complex secure classification workloads executed directly onboard of a surveillance device of this kind.

B. Local Face Detection with Secured Remote Recognition

Complete on-device computation might not be the most advantageous approach for all applications, particularly for those that can be clearly divided in a lower effort triggering stage and a higher effort one that is only seldom executed. A good example is the problem of face recognition. While state-of-the-art face recognition requires a significant workload in the order of billions of operations (e.g. FaceNet [32]), the problem can be easily decomposed in two stages: one where the input image is scanned to detect the presence of a face, and another where the detected faces are recognized. The first stage could be run continuously on a low-power wearable device such as a smartwatch, using an external device (e.g. a smartphone, the cloud) to compute the much rarer and much more complex second stage.

In this use case, we envision Fulmine to be integrated into an ultra-low power (ULP) smartwatch platform similar to that presented in Conti et al. [33]. We consider a similar camera with the one used in Section IV-A producing a 224×224 input image. Face detection is performed locally, using the first two stages (12-net and 24-net) of the multi-stage CNN proposed by Li et al. [29]. If faces are detected by this two-stage CNN, the full input image is encrypted and transferred to a coupled smartphone for the recognition phase. The networks are applied to small separate 24×24 windows extracted from the input image; partial results need not be saved from one window to the next. Therefore the CNN does not use any external memory and can rely exclusively on the internal L2.

Figure 11 reports the experimental results for the local face detection use case in terms of energy and execution time. Baseline energy is almost evenly spent between convolutions, AES-128-XTS encryption, and densely connected CNN layers. Software optimizations such as parallelization, SIMD extensions are much more effective on convolutional and dense layers than they are on AES, due to their highly parallel and regular structure and to XTS internal data dependencies in the tweak computation. Using hardware accelerators essentially reduces the energy cost of convolution and on AES-128-XTS to less than 10% of the total, and leads to a 24× speedup and a
Fig. 11: Local face detection, secured remote recognition use case based on the 12-net and 24-net CNNs from Li et al. \cite{29} on a 224×224 input image, with full AES-128-XTS encryption of the image if a potential face is detected. CRY-CNN-SW operating mode at \( V_{DD} = 0.8 \) V. We consider that the first stage 12-net classifies 10% of the input image as containing faces, and that the second stage 24-net is applied only to that fraction.

Fig. 12: EEG-based seizure detection and secure data collection. CRY-CNN-SW operating mode at \( V_{DD} = 0.8 \) V.

13× reduction in energy with respect to the baseline. The final test takes 0.57 mJ or 5.74 pJ per elementary operation. Further reduction could be enabled by algorithmic changes that favor a deeper network with more convolutional layers to one with many densely connected layers. Even without these potential improvements, the result we show enables deployment of this algorithm on a real ULP smartwatch. If we consider it to be powered by a small lithium-ion polymer 4 V 150 mA-h battery, face detection could be performed with no interruption for roughly 1.6 days before exhausting the battery charge. Duty cycling, taking advantage of the power management features of the SoC described in Section II-A, can prolong this time considerably.

C. Seizure Detection and Secure Long-Term Monitoring

While the first two use cases we propose focus on vision, that is not the only computationally intensive task that could be executed on a future computing end-node. Extraction of semantically relevant information out of biosignals such as electromyogram (EMG), electrocardiogram (ECG), and electroencephalogram (EEG) is a potentially huge market for low-power footprint IoT devices, as an enabler technology for smart fitness, personalized healthcare, and other human augmentation technologies.

In this use case, we consider a seizure detection healthcare application based on a support vector machine (SVM) trained on energy coefficients extracted from the principal components of a multi-channel EEG signal \cite{34,30}. Starting from a 256-sample window of 23 input EEG channels (represented as 32 bit fixed-point numbers), principal component analysis (PCA) is applied to extract 9 components, that are then transformed in a wavelet representation by a digital wavelet transform (DWT). Energy coefficients are extracted from this representation. Finally, a classifier SVM is used to determine if there is a seizure. For long-term monitoring, the components produced by the PCA have to be collected and sent to the network to be stored or analyzed. Given the high degree of sensitivity of this data, it cannot be transferred in plain format but must be appropriately encrypted, for which we consider AES-128-XTS. The sampling frequency is 256 Hz with 50% overlapped windows, i.e. seizure detection is performed every 0.5 s.

Figure 12 shows the results in terms of energy (split down between the various kernels) and execution time. Several components of PCA, like diagonalization, are not amenable to parallelization. Nonetheless, we observe a 2.6× speedup with four cores excluding AES encryption. Using the HWCRYPT, encryption becomes a transparent step of the algorithm and essentially disappears from the overall energy breakdown. Therefore, with combined SW parallelization and accelerated encryption, an overall 4.3× speedup and 2.1× energy reduction can be achieved. More importantly, the absolute energy consumption of 0.18 mJ (12.7 pJ per operation) means that a typical 2 Ah@3.3 V pacemaker battery \cite{35} would suffice for more than 130 million iterations, and more than 750 days if used continuously - as for most of the time the Fulmine SoC can be in the sleep mode described in Section II-A.

V. STATE-OF-THE-ART AND RELATED WORK

In this section, we discuss works related to our contribution, i.e. those proposing low-power hardware IPs for encryption or CNNs, and IoT end-node chips that constitute our direct point of comparison. Table \[\text{II}\] summarizes the positioning of Fulmine with respect to the state-of-the-art, restricted to platforms for which silicon measurements have been published.

A. Low-Power Encryption Hardware IPs

Authenticated encryption is a hot topic in the cryptographic community since it adds additional services on top of data confidentiality. AES in the Galois Counter Mode \cite{49} (AES-GCM) is one of the most used authenticated encryption schemes today. For example, Intel added a dedicated finite field multiplication to the AES-NI extension, with a throughput up to 1.03 cpb \cite{50}. However, solutions of this kind are clearly targeting a different scenario from small, low-power IoT devices.

Only a few IoT-oriented commercial AES controllers are available; an example is the Maxim MAXQ1061 \cite{51}, claiming up to 20 Mbit/s (power consumption data is not currently
disclosed). Research AES accelerators in the sub-100 mW range for the IoT domain have been proposed by Mathew et al. [56] in Intel 22nm technology, Zhang et al. [57] in TSMC 40 nm and Zhao et al. [58] in 65 nm; the latter reaches efficiency up to 620 Gbit/s/W thanks to efficient body biasing and a statistical design flow targeted at reducing worst-case guard bands. A device consuming as little as 0.25 µW for passive RFID encryption has been proposed by Hoquet et al. [59]. The main differentiating point between our contribution and these hardware encryption techniques is the tightly coupled integration within a bigger low-power system.

B. Low-Power CNN Hardware IPs

The most common way to accelerate CNNs is to rely on powerful GP-GPUs [7] [52]. Although able to reach extremely high throughput, this approach is clearly out of the mission profile for IoT end-nodes, due to their power footprint in the order of hundreds of Watts. Some programmable embedded platforms such as ODROID-XU [53], or Movidius Myriad 2 [44] improve the energy efficiency of software CNN implementations to up to 120 Gop/s/W within a few Watts of power envelope, targeting embedded systems such as smartphones or UAVs as well as the booming autonomous car business [55]. To the best of our knowledge, the only commercial solution specifically designed for IoT end-nodes is WiseEye, to be presented by CEVA at CES 2017 [56].

Most research architectures for acceleration of CNNs have focused on specialized architectures to accelerate convolutional layers (e.g. Origami [40]), or convolutional and pooling layers (e.g. ShidianNao [41] and Eyeriss [42]). These accelerators reach efficiencies in the order of a few hundreds of equivalent Gop/s/W. However, they all rely on highly specialized architectures, their flexibility is limited, and most of them are not capable of implementing the other functionality required by IoT end-nodes, including security and general-purpose signal processing tasks.

One big differentiating point between these platforms are their assumptions in terms of algorithmic and arithmetic accuracy. Jaehyeong et al. [43] rely on 24bit fixed-point arithmetic, but they approximate weights using a low-dimensional representation based on PCA. Most other works use either 16 bits [26], [44] or 12 bits [40]. However, recent algorithmic developments such as BinaryConnect [28] suggest that it is possible to reduce CNN weight precision down to a single bit with limited accuracy losses. This has been exploited in platforms such as YodaNN [57] to reach efficiency in the order of tens of equivalent Top/s/W. Another promising approach to improve energy efficiency in classification tasks are extreme learning machines (ELM), based on single-hidden layer feedforward neural networks. Although they have been proven to consume as little as 0.47 pJ/MAC [58][59], their applicability to real-life applications is still restricted to very simple problems.

In this work a flexible approach has been adopted, where the precision of images is fixed to 16 bits, while that of weights can be scaled from 16 to 4 bits. This approach avoids the requirement of specific training for binary connected networks, while weight precision can be scaled according to the specific application requirements in terms of accuracy, throughput and energy efficiency.

C. End-Node Architectures

Traditional end-node architectures for the IoT leverage tiny microprocessors, often Cortex-M0 class, to deal with the extreme low-power consumption requirements of applications. Several commercial solutions have been proposed, among the others, by TI [60], STMicroelectronics [61], NXP [62], and Ambiq [63], leveraging aggressive duty-cycling and sub-10 µW deep-sleep modes to provide extremely low power consumption on average. Other recent research platforms optimize also the active state, exploiting near-threshold or sub-threshold operation to improve energy efficiency and reduce

| Table II: Comparison between Fulmine and several platforms representative of the state-of-the-art in encryption, data analytics, and IoT end-nodes. |
|---------------------------------------------------------------|
| Technology | Area | Power | Com. Perf. | Conv. Perf. | Enc. Perf. | SW Perf. | SW Eff. | Eq. Eff. |
|------------|------|-------|------------|-------------|------------|----------|---------|---------|
|            | [mm²] | [mW]  | [GMAC/s]   | [GMAC/s/W]  | [Gbit/s]   | [MIPS]   | [MIPS/mW] | [pJ/op] |
| AES        |       |       |            |             |            |          |         |         |
| Mathew et al. [56] | 0.43V, 324MHz | Intel22nm | 2.74x10⁻³ | 0.43 | - | 0.124 | 289 | - | 0.19² |
| Zhang et al. [57] | 0.9V, 1.3GHz | TSMC40nm | 4.29x10⁻³ | 4.39 | - | 0.446 | 113 | - | 0.49⁷ |
| Zhao et al. [58] | 0.5V, 34MHz | 65nmLL | 0.013 | 0.05 | - | 0.027 | 574 | - | 0.1⁵ |
| Hoquet et al. [59] | 0.36V, 0.32MHz | 65nmLP | 0.018 | 2.5x10⁻⁴ | - | 3.6x10⁻⁷ | 144 | - | 0.3⁹⁶ |
| CNV        |       |       |            |             |            |          |         |         |
| Origami [40] | 0.8V, 190MHz | UMC65nm | 3.09 | 93 | 37 | 402 | - | - | 0.69⁷ |
| ShidianNao [41] | 65nm | 4.86 | 320 | 64 | 200 | - | - | - | 1.39⁷ |
| Eyeriss [42] | 1V, 200MHz | TSMC65nm LP | 12.25 | 278 | 23 | 83 | - | - | 3.3⁵ |
| Jaehyeong et al. [43] | 1.2V, 125MHz | 65nm | 16.00 | 45⁵ | 32 | 71⁷ | - | - | 0.3⁹ |
| Park et al. [44] | 1.2V, 200MHz | 65nm | 10.10 | 37⁷ | 41 | 110⁸³ | - | - | 0.2⁵³ |
| IoT        |       |       |            |             |            |          |         |         |
| SleepWalker [45] | 0.4V, 25MHz | 65nm | 0.42 | 0.175 | - | - | - | 25 | 143 | 6.9⁹ |
| Myers et al. [46] | 0.4V, 0.7MHz | 65nm | 3.76 | 0.008 | - | - | - | 0.7 | 88 | 11.4 |
| Konijnenburg et al. [47] | 1.2V, 10MHz | 180nm | 37.7 | 0.52 | - | - | - | 1.04 | 20 | 50.0 |
| Mia Wallace [48] | 0.65V, 68MHz | UMC65nm | 7.4 | 9.2 | 2.41 | 261 | - | - | 270 | 29 | 22.5 |
| Fulmine     |       |       |            |             |            |          |         |         |
| CRY-CNNG-SW | 0.8V, 85MHz | UMC65nm LL | 6.86 | 13 | 6.35 | 465 | 1.6 | 100 | 408 | 31 | 5.7⁴ |
| KEC-CNNG-SW | 0.8V, 104MHz | UMC65nm LL | 6.86 | 13 | 6.35 | 465 | 1.6 | 100 | 408 | 31 | 5.7⁴ |
| SW @ 0.8V, 120MHz | 12 | - | - | - | - | - | - | 470 | 39 |         |
power consumption during computation [46], [45], [61], [65].

Some commercial architectures leverage lightweight SW acceleration and optimized DSP libraries to improve performance. The NXP LPC54100 [62] is a commercial platform where a big Cortex-M4F core acts as an accelerator for a little ultra-low-power Cortex-M0 targeted at always-on applications. From a software viewpoint, some optimized libraries have been developed to efficiently implement crypto algorithms on Cortex-M3 and M4 architectures, given the criticality of this task for IoT applications. Examples of these libraries are SharkSSL [66] and FELICS [5], able to encrypt one block of AES-128-ECB in 1066 cycles and 1816 cycles respectively, both targeting a Cortex-M3. On the other hand, CMSIS [67] is a well-known set of libraries to optimize DSP performance on Cortex-M architectures.

However, even with software-optimized libraries, these tiny micro-controllers are unfortunately not suitable for secure near-sensor analytics applications using state-of-the-art techniques, which typically involve workloads in the orders of billions of operations per second. For this reason, a few recent SoCs couple programmable processors with hardwired accelerators, to improve execution speed and energy efficiency in cryptography and other performance-critical tasks. In the field of embedded vision, heterogeneous SoCs of this kind include the one recently proposed by Renesas [68], coupling a general purpose processor with an FPU, a DSP, and a signal processing accelerator. Intel [69] proposed a 14 nm SoC where a small core with light signal processing acceleration cooperates with a vision processing engine for CNN-based feature extraction and a light encryption engine, within a 22 mW power budget. Pullini et al. proposed Mia Wallace, a heterogeneous SoC [48] coupling four general purpose processors with a convolutional accelerator. In the field of bio-signals processing, Konijnenburg et al. [47] proposed a multichannel acquisition system for biosensors, integrating a Cortex-M0 processor and accelerators for digital filtering, sample rate conversion, and sensor timestamping. Lee et al. [70] presented a custom bio-signals processor that integrates configurable accelerators for discriminative machine-learning functions (i.e. SVM and active learning) improving energy by up to 145x over execution on CPU.

Similarly to the presented designs, Fulmine is a low-power, heterogeneous MPSoC. In contrast to the other architectures presented here, it tackles at the architectural level the challenge of efficient and secure data analytics for IoT end-nodes, while also providing full programmability with sufficient high performance and low power to sustain the requirements of several near-sensor processing applications.

D. Comparison with State-of-the-Art

To compare special-purpose devices with general-purpose microcontrollers, Table I compares Fulmine with the architectures that define the boundaries of the secure data analytics application space. Apart from area, power and performance, we also use an equivalent energy efficiency metric defined as the energy that a platform has to spend to perform an elementary RISC operation [5]. Fulmine achieves the highest result on this metric, 5.74 pJ per operation, thanks to the cooperation between its three kinds of processing engines.

The second-best result is of SleepWalker (6.99 pJ) - but in an operating point where execution takes 89× more time than in the case of Fulmine.

Moreover, Fulmine provides better area efficiency than what is available in other IoT end-nodes. For example, even discounting all complexity related to a setup with many computing chips on the same board, 32 SleepWalker chips would be needed to achieve a performance similar to ours on the face detection workload of Section IV-B. On the other hand, while coupling an efficient IoT microcontroller with external accelerators can theoretically provide an effective solutions, this would require continued data exchange between the devices for most of the secure data analytics scenarios for IoT devices. The necessity for high bandwidth for chip-to-chip communication within a ultra-low-power system makes this solution typically impractical.

Scaling to more deeply integrated technology and/or operating voltage could provide very significant benefits in terms of energy. If we consider a 28 nm technology at VDD =0.6 V with a similar frequency target, power would scale to ~4 mW, with an overall improvement to energy efficiency by 6×, making it comparable to dedicated accelerators and enabling even more complex integrated workloads.

VI. CONCLUSION

This work presented Fulmine, a 65 nm System-on-Chip targeting the emerging class of smart secure near-sensor data analytics for IoT end-nodes. We achieve this without using aggressive technology or voltage scaling, but through the architectural solution of combining cores and accelerators within a single tightly-coupled cluster. The use cases we have proposed show that this approach leads to improvements of more than one order of magnitude in time and energy with respect to a pure software based solution, with no sacrifice in terms of flexibility. The Fulmine SoC enables secure, integrated and low-power secure data analytics directly within the IoT node. Without any compromise in terms of security, the proposed SoC enables sensemaking in a budget of a few pJ/op - down to 3.16 pJ/op in one case, or 315 Gop/s/W.

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