Reliability and Power Analysis of FinFET Based SRAM

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Abstract
Demand for accommodating more and new functionalities within a single chip such as SOC needs novel devices and architecture such as FinFET devices instead of MOSFET. FinFET emerged as a non-planar, multigate device to overcome short channel effects such as subthreshold swing deterioration, drain induced barrier lowering and threshold voltage roll-off which degrade circuit performance. As the need of device technology is mounting in electronic gadgets the important parameters are taken into consideration such as low leakage, high reliability, low power dissipation, and high operating speed. Reliability is one of key considerations in converting a proof of concept into reality. In this work the reliability of FinFET device is studied experimentally according to ITRS (international technology roadmap for semiconductors) roadmap using several standard test protocols such as multiple current stressing, harsher environment conditions, and effect of electromigration. Furthermore, power analysis of FinFET based SRAM is done by using 7 nm BSIM-CMG Predictive technology model files (PTM) in mentor graphics tool. The FinFET based SRAM showed low leakage, low power dissipation, and less delay compared to existing conventional MOSFET based SRAM.

Keywords MOSFET · FinFET · SRAM · SOI · SCE · Reliability · ITRS

1 Introduction
Electronic devices are in high demand in the electronics sector and are utilized in a variety of applications including automobiles, computing, communications, entertainment, artificial intelligence, neural networks, computer vision, big data, and many others [1] in which advanced nanodevice FinFET is used as a transistor instead of MOSFET to achieve high performance, low power dissipation, low area at reduced technology. Channel electrostatics is controlled by single gate MOSFET whereas control of channel in 3 directions to reduce short channel effects is achieved by 3 gate FinFET [2–3]. For digital circuit, Mixed signal circuit, Analog/RF circuit, FinFET is emerged as superior device to get low power dissipation, high speed, low area at deep submicron range. FinFET can be fabricated in 2 ways one is SOI (silicon on insulator) and alternatively as BULK. Due to the presence of an insulating layer beneath oxide, SOI FinFETs with lower parasitic capacitance increase switching speed and reduce power consumption [4]. RF characteristics, Linearity, is achieved by spacer dielectric optimization. For nanoscale applications, reduction of leakage is required which in turn reduces power dissipation and improves system performance [4]. FinFET has a well established structure and fabrication due to this TSMC and Intel manufacturing Industries made use from 2011 to till date at sub 22 nm technology nodes [5]. SOI FinFET shows reduced device cross talk, lower junction leakage, fully dielectric isolation, lower junction leakage, reduced capacitance, and a nearly ideal subthreshold slope [6–8]. FinFET reduces short-channel effects by wrapping the gate over the channel from four sides. Due to continuous scaling, FinFET faces several challenges in terms of cost effectiveness, patterning, layout, device performance [9–12]. Due to several advantages FinFET can be used in a variety of applications such as terrestrial systems, infrared detectors, space, satellite communication, nuclear reactor, military [12–13]. One Fin is used in simulation and fabricated FinFET. reduction of current leakage occurs due to usage of multiple fins in which better control of the channel is done by the gate, thus increasing on current and reducing off current. The amount of current flow from higher potential to lower potential increases as the number of fins increases, thus resulting in an increase of speed.
Recent work on Analog/RF and DC performance metrics of 3 nm gate length FinFET showed high $I_{ON}/I_{OFF}$ high sub-threshold and lower DIBL, thus obeying Moore’s law at reduced technology nodes [14]. Recent research shows that the junctionless FinFET by using various dielectric constants improves device subthreshold performance [15]. Furthermore, the work on device performance of 5 nm trigate junctionless SOI FinFET with different spacer dielectric combinations showed excellent device parameters such as subthreshold slope, drain induced barrier lowering, $I_{ON}$, $I_{ON}/I_{OFF}$ [16]. Moreover, the limitation of FinFET with 10 nm junctionless nanosheet FET performance on Analog/RF and DC characteristics using a high k gate stack is done in [17]. In the literature survey no one has done research on reliability issues of FinFET devices and power analysis of 7 nm FinFET based SRAM, which is one of the gaps observed and covered under this work.

2 Reliability Study of FinFET

One of the most important factors to consider when turning a proof of concept into reality is reliability. It is critical to investigate the dependability of these surface passivation methods in more depth. The specific contact resistance is the most important factor in determining reliability. Under any adversity, the resistance values should not change dramatically. The ITRS (International Technology Roadmap for Semiconductors) developed a number of typical test techniques to ensure reliability. Multiple current stressing is a test that involves repeatedly passing a variable current of quite high amplitude through a test structure. There will be no major performance decrease in a trustworthy framework. Temperature cycling is another more rigorous reliability test that is performed on a regular basis. Repeating the numerous current stressing measurements at different temperatures is part of the experiment. -55 °C to +125 °C is the standard temperature range. In order to ensure reliability, the test structure should be able to withstand these circumstances without degrading. Last but not least, the test structure should be exposed to a harsher environment to account for variability caused by differing storage circumstances. Over a lengthy period of time, the test structure is normally maintained in a high relative humidity environment (usually RH > 60%) and at a high temperature (> 100 °C) (typically a week or more). To ensure trustworthiness, the repeat measurements should resemble those of the original measurements.

Preparation of the substrate, Fin etch, oxide deposition, planarization, recess etch, gate oxide deposition, and ultimately gate deposition was used in the fabrication of the FinFET device. Fig. 1 shows the TEM cross section of the fabricated FinFET device at the 22 nm CMOS technology node, whereas Fig. 2 shows the corresponding 3D FinFET device structure in the sentaurus TCAD simulation domain.

Prior to going for reliability studies, fabricated FinFET devices bonded with feeder lines (M1, M2) at low temperature (160 °C) and low pressure (2.5 mbar) for Kelvin structure design [22–24], process flow is explained below. Figure 3 shows the cross-sectional TEM of the bonded region of the feeder lines. Figure 4 shows the complete experimental process flow of the reliability study of FinFET devices.

2.1 Reliability Assessment of the Fabricated FinFET Using Multiple Current Stressing Test

For applications such as high-speed super-fast multi-core processor design, the electrical performance of the FinFET device is critical, especially when numerous operations are performed. As a result, the constructed Kelvin structure along with the FinFET device (with M1, M2 feeders) was treated to 1000 cycles of current stress with magnitudes ranging from $-0.1$ A to $+0.1$ A. At room temperature, all measurements were made with a Keithley source measuring unit. For every 100 cycles, the specific resistance was measured.

Even after 1000 cycles of current straining, no decrease of contact resistance was found as shown in Fig. 5, indicating that the constructed FinFET device is trustworthy.

2.2 Reliability Assessment of the Fabricated FinFET Device Using Temperature Cycling Test

The thermal stability test, as per the JESD22-A104B standard, involves subjecting the FinFET device through a feeder to 1000 cycles of current sweeping from $-0.1$ A to $+0.1$ A at various temperatures ranging from $-55$ °C to $+125$ °C. The resistance behavior of a FinFET device specimen pre and post temperature cycles is shown in Fig. 6. It can be inferred from the figure that even at very high and very low temperature the fabricated FinFET device is reliable and there is no deprivation of the specific resistance. As a result, FinFET devices may be viable and efficient at both high and low temperatures.

2.3 Reliability Assessment of the Fabricated FinFET Structure under Harsher Environment Conditions

The specimens were maintained under harsher environment circumstances for 96 h, with a high relative humidity (RH) of 65% and a high temperature of 130 °C, in order to investigate the effect of tougher environmental condition on the produced FinFET. The data taken after this storage correlate extremely well to the ones taken before this retention, as shown in Fig. 7. After such a lengthy period of exposure to harsher environmental results, it is clear that the unique resistance of both CMOS technology situations has not degraded. This shows that FinFET devices produced utilizing both CMOS and
CMOS technology is more resistant to dampness and high temperatures.

2.4 Electromigration Assessment of the FinFET Device Post Bonding

During an EM test, four-point sensing is used to evaluate electrical resistance. As shown in Fig. 8, resistance measurements taken during EM testing demonstrate a latency period during which the resistance remains unchanged, followed by a gradual and then rapid increase.

3 Static Random Access Memory (SRAM)

Cache memory which is made of SRAM cells [9–11] occupies 50% of the area in the processor; the leakage power due to cache memory in the processor is the major source of power dissipation [12]. Nowadays SRAM is operating in nanometre range in electronic gadgets so, the power dissipation in SRAM should be as low as possible in which leakage currents have to be less and speed should be more. Low power dissipation and more speed in SRAM is obtained by using advanced devices such as FinFET instead of MOSFET. SRAM is used in cache memory as it possesses low power and high speed. To meet technology scaling, new structure challenges have been proposed such as FinFET and Nanowire [13]. FinFET device attracted many SRAM designer’s as FinFET has superior short channel effects, reduced dopant fluctuations, independent gating, better subthreshold slope [13–18]. From device level to architecture level many FinFET based SRAM cells have been proposed [19–21]. The trend of SRAM along with Complementary technology metal oxide technology (CMOS) scaling in different processors and System on Chip (SOC)
Fig. 3 Bonded feeder lines for voltage and current feeding

Fig. 4 Process Flow of reliability analysis of fabricated FinFET device

Fig. 5 Electrical performance assessment using multiple current stress
products has fueled the need for innovation in the area of SRAM design. Simulation results are carried out for a 7 nm FinFET based SRAM to analyze the parameters for leakage power, delay and power dissipation, which is compared with existing MOSFET devices. BSIM-CMG stands for Berkeley short channel insulated gate field effect transistor model for common multigate (BSIM-CMG). This model files are mainly used for FinFET based product development and circuit
design as they provided basis for design infrastructure and in short time for delivery of product. BSIM-CMG is used as the speed of TCAD limits their use in circuit design and explanation. BSIM-CMG can be used to model three, two, one gate multigate. BSIM-CMG structures model files are used in SRAM as it incorporates short channel effects on devices such as parasitic extraction, velocity saturation, series resistance, Quantum mechanical effects on device characteristics. The power dissipation obtained in simulation is static power dissipation as the power dissipation is taken under no switching activity which given by \( P_s = I_{\text{Leakage}} \cdot V_{\text{DD}} \). Low-leakage current in FinFET based SRAM is due to junction leakage from source/drain junctions, subthreshold leakage through off transistors, gate leakage through gate dielectric. Supply voltage used is 0.7 V obeying ITRS for 7 nm FinFET based SRAM. Reduction of supply voltage results in reduction of power dissipation and increases gate delay thereby reducing operating frequency.

Operation of SRAM
The conventional 6 T SRAM cell has three different modes: stand by mode, write mode and read mode. In standby mode no write or read is performed which means the circuit is idle in read mode the data is read from output node to the bitlines and in write mode the data or contents are updated. The SRAM to operate in read mode should have “write stability”. The three different modes work as follows.

Standby: If the word line WL is low ‘0’ then the access transistors M5 & M6 turn off and the bitlines are disconnected from the inside latch circuit. The cross coupled inverters will continue to reinforce each other, in this mode the current drawn from supply voltage is called standby or leakage current.

Reading mode:- In read mode the word line WL is high ‘1’ which turns on the transistors M5 and M6, when both the transistors turn on the value of Q and \( Q \bar{b} \) are transferred to BL and \( \bar{B}L \) bitlines respectively but before giving the wordline high the bit lines BL and \( \bar{B}L \) should be precharged to \( V_{\text{DD}} \). Assume that 1 is stored at Q and 0 at \( \bar{B}L \) so no current flows through M6 and some current flows through M5 will discharge the \( \bar{B}L \) through M5 and M2. This small voltage difference is recognized by sense amplifier that pull the data and produce the output. The decoders are used to select the appropriate cell.

Writing mode:- In write mode suppose we want to write a ‘0’ at the output Q, we apply a ‘0’ to the bit line means setting BL to ‘0’ and \( \bar{B}L \) to ‘1’, after setting the bit line WL is then asserted. All the other transistors are turned off.

4 Conclusion
Reliability assessment of the experimental FinFET device under 7 nm and 22 nm is demonstrated under various tests such as temperature cycling test, harsher environment condition, multiple current stress, the results shown that the device

### Table 1

| Parameter      | Dimensions |
|----------------|------------|
| Node (nm)      | 07         |
| \( V_{\text{DD}} \) (V) | 0.7        |
| \( T_{\text{fin}} \) (nm) | 6.5        |
| \( H_{\text{fin}} \) (nm) | 18         |
| EOT (nm)       | 0.62       |

\( T_{\text{fin}} \) —Thickness of fin.

\( H_{\text{fin}} \) —Height of fin.

EOT —Effective oxide thickness.

\( V_{\text{DD}} \) —Supply Voltage.

### Table 2

| Parameter      | MOSFET | FinFET |
|----------------|--------|--------|
| Mode           | Write  | Read   | Write  | Read   |
| Technology     | 180nm  | 180nm  | 7nm    | 7nm    |
| Delay          | 143ps  | 974ps  | 96ps   | 603ps  |
| Leakage power  | 286nW  | 793nW  | 1.6nW  | 1.98nW |
| Power Dissipation | 1.50nW | 618pW  | 787pW  | 397pW  |

and simulation results shown in Fig. 9 and Fig. 10 respectively.
structure above to withstand under any circumstances without degrading to ensure reliability. The most important component to increase performance of a system is SRAM memory which is used as cache memory in a multiprocessor chip, requires low power dissipation, low leakages, high speed for the future Internet of things (IOT) devices which connects nearly $50$ billion devices in future. Analysis of leakage and power of SRAM is done using $7$ nm BSIM-CMG FinFET file in Mentor Graphic tool which shows low power dissipation and high speed compared to the existing MOSFET at high technology node. This SRAM limits the usage of still low power and high-speed circuits.
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Declarations

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Consent for Publication Yes

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