Model Predictive Control Scheme of a Four-Level Quasi-Nested Converter Fed AC-Drive, with dc-Link Voltage-Drift Compensation

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Abstract: In this paper, a Model Predictive Control (MPC) strategy is introduced for its application in a four-level quasi-nested topology, feeding an Interior Permanent Magnet Synchronous Machine (IPMSM) AC-drive. The proposed control strategy is capable to synthesize the required output space vectors to ensure perfect tracking of the AC-drive speed reference under different loading conditions, while also ensuring voltage balance between the dc-link capacitors. The proposed converter topology is based on a reduced number of components compared to other mature converter topologies, such as the neutral-point clamped converter (NPC) or the active neutral-point clamped converter (ANPC) topologies, when compared in terms of the number of output voltage levels, since this quasi-nested topology does not require passive clamping devices such as diodes or active switches. Moreover, no floating dc-link capacitors with asymmetrical voltage levels are employed, thus simplifying the dc-link capacitor voltage balance mechanism. This work presents the switching operation principles and MPC control law when supplying an IPMSM AC-drive load are addressed in detail. Simulation and validation results using a Hardware in the Loop (HIL) prototype under different operation conditions are presented in order to validate the proposed converter topology and control strategy.

Keywords: multilevel converter; quasi-nested converter; reduced switching devices topology; dc-link balance mechanism; model predictive control; permanent magnet synchronous machine; AC drive

1. Introduction

Modern industrial processes are commonly based on high demanding electric drive systems and high inductive loads. In this field of applications, voltage source multilevel power converters (MLC) have become an enabling technology for high demanding applications: renewable energy conversion, transportation (tractions of trains, ship propulsion, and electric vehicles), mining, manufacturing and petrochemical, etc. Many of the previously mentioned processes are continuously increasing their power ratings to reach higher production rates and efficiency, thus leading to higher voltage and current levels without compromising energy quality standards. These issues have promoted the research and development of the technology of semiconductors in order to reach higher operational voltages and currents, which are currently at 8 kV and 6 kA, respectively) [1–3], while maintaining traditional converter topologies (mainly two-level voltage and current source converters), and by introducing new converter topologies, preserving the traditional semiconductors, in new arrangements called multilevel converters [4].

The main benefits of classical topologies are referred to as their very well-known topological arrangements and control methods. However, when going into high power applications, semiconductors become more expensive and other requirements referred to their power quality have to be fulfilled, thus introducing the need of input/output filters. On the other hand, the multilevel converter approach uses cheaper switching devices
but the need of more complex topological structures, which introduces several challenges for their implementation and control. Nevertheless, these challenges have raised new improvement opportunities by introducing new topologies that could be used to improve the power conversion process. This fact has boosted new research and applications of multilevel converters during the last two decades.

Nowadays, multilevel converters are considered the main solution for industrial applications where high power quality and dynamic performance are required, within the power range going from 1 to 30 MW. [5–7]. Their success in industrial applications is mainly due to high voltage operating capability, reduction in the blocking voltage stress as well as conduction losses, reduced voltage spikes (voltage rate of change $\frac{dv}{dt}$ due to switching), reduced harmonic contents in the output voltage waveforms, with near sinusoidal currents components [8,9], smaller output and input filters (if required), an increased overall efficiency, and, depending on their topology, possible fault-tolerant capability [4]. These topologies have been studied and reported extensively in literature, with many contributions by Wu et al., Boldea et al., Kouro et al., and Leon et al. [10–14], showing the importance gained by this technology. The level of commercial penetration of multilevel topologies with a wide variety of topologies, control methods, and applications has to also be referred to.

Despite their main advantages, MLC topologies are affected by undesired voltage unbalance between the dc-link capacitors, thus resulting in an asymmetric energy flow of the dc-link capacitors on each switching period. This voltage drift effect produces distortion in the output voltages due to asymmetries in the synthesized waveforms or, in the worst case, loss of some of the voltage levels. Carrier based modulation strategies are not capable by themselves to balance the voltage drift effect, thus requiring an additional compensation strategy which is usually of complex implementation. In this context, the implementation of Model Predictive Control (MPC) has gained great research interest because of its fast dynamic response, flexibility, and easy inclusion of non-linearities and constraints, when including other control requirements, within the same control structure [15–19].

In this work, a novel multilevel converter, consisting in a four level quasi-nested converter (4L-QNC) topology, is introduced for its application in medium-voltage AC-drives. A control scheme based on a Model Predictive Control formulation has been implemented toward controlling an AC-drive and the dc-link capacitors unbalance, using optimum voltage vector selection criteria. Validation of the MPC scheme has been made using a Hardware in the Loop (HIL) Plexim, RT-Box CE HIL platform, via real-time simulation. A comparison with the existing industry standard topologies and classical oriented control schemes showed its performance in terms of efficiency (switching and conduction losses) and total harmonic distortion (THD), and the effectiveness of the control scheme based on a Model Predictive Control approach, to become a possible candidate for its application in industrial processes.

The remainder of the present work is organized as follows: In Section 2, the four level quasi-nested topology converter topology, switching states, and fundamental principle are discussed. Section 3 presents the Model Predictive Control formulation and control objectives. In addition, finally, Section 4 presents the simulation and Hardware in the Loop verification results of the multilevel topology and control scheme.

### 2. Quasi-Nested Topology

The proposed three-phase arrangement of the quasi-nested topology is presented in Figure 1. This particular topology consists of three dc-link capacitors that are connected in series to a common neutral point denoted as N. The active switch arrangement per cell may consist of six IGBTs or MOSFETs for high-voltage and high switching frequency operation [20,21]. This particular arrangement is based on the interconnection of individual H-Bridge half cells, whose output terminals have been labeled x and y, respectively. Terminal points x and y are connected to a full leg, which consists of two switching devices connected in series by their collector and emitter terminals. Each phase output termi-
nal is denoted by \( j \), and the load is connected to each one of the three output terminals, corresponding to each phase.

As presented in Figure 1, the 4L-QNC topology can be compared to a three-level NPC converter (3L-NPC) single cell, but without the clamping devices such as diodes or active switches as in the case of an Active-NPC converter.

![Figure 1. Quasi-nested four level inverter topology fundamental cell.](image)

In comparison to the nested topologies such as the NPC or ANPC, the 4L-QNC does not have a connection of each leg mid-point (leg output point) with each other. Instead, the inner legs mid-points are connected to a single output leg, conforming a quasi-nested topology. The most remarkable features of the presented topology are:

- Capability of single or three-phase arrangement.
- Four output voltage levels. Having one more voltage level than the 3L-ANPC and the 3L-NPC, but using the same number of semiconductor devices.
- No clamping diodes or active clamping switches like in the 3L-NPC or 3L-ANPC topologies.
- Inner switches blocking voltage rating is \( \frac{1}{3} \) of the total dc-link voltage, which represents an improvement respect to the nested arrangement, whose blocking voltage stress is \( \frac{1}{2} \) of the dc-link voltage.

### 2.1. Fundamental Principle

This topology generates four phases to neutral voltage levels: \( 0, \frac{1}{3} v_d, \frac{2}{3} v_d, \) and \( v_d \). Each voltage level is synthesized by connecting the output terminal \( j \) to the corresponding dc-link capacitors. The switching states per cell are presented in Table 1.

**Table 1.** Switching states and output voltages for the 4L-QN topology.

| \( \# \) | \( S_1 \) | \( S_2 \) | \( S_3 \) | \( v_{xN} \) |
|-------|--------|--------|--------|--------|
| 1     | 0      | 0      | 0      | 0      |
| 2     | 0      | 0      | 1      | \( \frac{1}{3} v_d \) |
| 3     | 0      | 1      | 0      | \( \frac{2}{3} v_d \) |
| 4     | 0      | 1      | 1      | \( \frac{2}{3} v_d \) |
| 5     | 1      | 0      | 0      | 0      |
| 6     | 1      | 0      | 1      | \( \frac{1}{3} v_d \) |
| 7     | 1      | 1      | 0      | \( v_d \) |
| 8     | 1      | 1      | 1      | \( v_d \) |
The synthesized voltage of each fundamental cell, assigned to the switching states presented in Table 1, can be expressed as in Equation (1)

$$v_{jN} = v_d S_1j S_2j + \frac{2}{3} v_d S_1j S_2j + \frac{1}{3} v_d \bar{S}_2j S_3j$$  \hspace{1cm} (1)

where $v_{jN}$ stands for the corresponding output voltage of the $j$-phase with respect to neutral $N$, and $v_d$ is the total dc-link voltage; $j \in \{a, b, c\}$ and $S_{\ell j} \in \{1, ..., 3\}$ represent the corresponding active switch and $\bar{S}_{\ell j}$ to its complementary state.

The corresponding output voltage space vector in the $\alpha \beta$ stationary reference frame $v_{s(\alpha\beta)}$ is obtained as follows from the $\alpha \beta$ transformation of the corresponding fundamental cell output voltages:

$$v_{s(\alpha\beta)} = \frac{2}{3} \left[ v_a + a v_b + a^2 v_c \right]$$  \hspace{1cm} (2)

where $a$ stands for the complex space operator given by $a = e^{j2\pi/3}$. These space vectors are shown in Figure 2.

![Figure 2. 4L-QNC topology space vectors.](image)

2.2. dc-Link Balance Problem

The main drawback of multilevel VSC is the possibility of having, in the presence of asymmetries in their switching strategy, the rise of unbalanced dc components present in each dc-link capacitor. This phenomenon is due to nonuniform power drawn for each capacitor, as a result of the modulation strategy employed and the modulation index [22]. In fact, when using carrier based modulation strategies, not all the dc-link capacitors deliver their stored energy on a duty cycle. In particular, the 4L-QNC topology presents some switching asymmetries when operating with a modulation index $m < \frac{1}{3}$. In this condition, either the upper or the middle dc-link capacitors are not being used, stimulating a dc voltage unbalance to build-up. On the other hand, when going into $m \geq \frac{1}{3}$, the voltage across the middle capacitor $C_2$ decreases, depending on the AC side power factor. If the output power factor $f_p = 1$ in one fundamental commutation period, $C_2$ is always in the
discharge condition, so eventually the voltage across $C_2$ falls to zero. This condition is presented in Figure 3.

![Figure 3](image_url)

**Figure 3.** (a) Current flow direction, (b) dc-capacitors charging and discharging regions in one fundamental period.

To overcome this problem, and making use of all the redundant switching state available in this topology, it is necessary to select the adequate switching state and switching interval (not symmetrical switching periods), according to the semi-cycle of the load current, and the charging/discharging region of each one of the dc-link capacitors in order to ensure full voltage drift compensation.

To deal with these switching constraints, Model Predictive Control appears as a feasible implementation due to its non-linear formulation and optimization objective, which can deal with several constrains, using a single cost function, compared to traditional PWM based strategy, which are limited by a symmetrical distribution of the active voltage space vectors, within one sample time $T_s$. 
3. Model Predictive Control Scheme

In this work, a Model Predictive Control (MPC) strategy using optimum voltage space vector selection is proposed to address the voltage drift issue, directly from the discrete model prediction and the selection of the optimal switching state. Due to the non-linear nature of the dc-link capacitors energy flow balance, the voltage drift compensation can be achieved across the whole modulation region and offer a better performance, compared to traditional schemes based on pulse width modulation (PWM) techniques.

3.1. Discrete Model

The variables to be controlled in the 4L-QNC correspond to the three-phase load currents (stator currents) $i_a$, $i_b$, $i_c$ and each dc-link capacitor voltage $v_{c1}$, $v_{c2}$, $v_{c3}$. All possible control actuations for this particular topology are defined for the fundamental cell in Table 1, corresponding to each of the possible output voltages.

As presented in the previous section, the quasi-nested topology presents three commutation cells involving each of the dc-link capacitors, which generate four output voltage levels per phase. As presented previously, the corresponding output voltage per phase (fundamental cell) can be expressed as in Equation (1), as an non-linear function $f$ of the switching state $S_i \ell \in [1, \ldots, 3]$, $\ell \in [a, b, c]$ and the total dc-link voltage $v_d$ as:

$$v_{ijN} = f(S_i \ell, v_d)$$

(3)

The dynamical model for the Permanent Magnet Synchronous Machines (PMSM) in the $a, b, c$ continuous time subspace is expressed in Equations (4)–(7).

$$\begin{bmatrix}
    v_a \\
    v_b \\
    v_c
\end{bmatrix} = R_s \begin{bmatrix} I \end{bmatrix} \begin{bmatrix} i_a \\
    i_b \\
    i_c \end{bmatrix} + \frac{d}{dt} \begin{bmatrix}
    \psi_a \\
    \psi_b \\
    \psi_c
\end{bmatrix}$$

(4)

The corresponding stator flux linkages are given in Equation (5).

$$\begin{bmatrix}
    \psi_a \\
    \psi_b \\
    \psi_c
\end{bmatrix} = \begin{bmatrix}
    L_a(\theta_k) & M_{ab}(\theta_k) & M_{ac}(p\theta_r) \\
    M_{ba}(\theta_k) & L_b(\theta_k) & M_{bc}(p\theta_r) \\
    M_{ca}(\theta_k) & M_{cb}(\theta_k) & L_c(p\theta_r)
\end{bmatrix} \begin{bmatrix} i_a \\
    i_b \\
    i_c \end{bmatrix} + \psi_m \begin{bmatrix}
    \cos (\theta_k) \\
    \cos (p\theta_r - \frac{2\pi}{3}) \\
    \cos (p\theta_r + \frac{2\pi}{3})
\end{bmatrix}$$

(5)

where $L_k$ $k \in [a, b, c]$ correspond to the stator inductance, $M_{kj}$ $j \in [a, b, c]$ and $k \neq j$ to the stator mutual inductance, and $\psi_m$ stands for the permanent magnet flux linkage. Due to the anisotropic nature of the rotor, the corresponding stator and mutual inductances can be expressed in terms of the average stator inductance $L_s$ and the variation in the self-inductance $\Delta L_m$ as in Equations (6) and (7)

$$L_k = L_s + \Delta L_m f(2p\theta_r) \ k \in [a, b, c]$$

(6)

$$M_{kj} = -\frac{1}{2} L_m + \Delta L_m f(2p\theta_r) \ j \in [a, b, c]; \ k \neq j$$

(7)

it has to be noted that both $L_k$ and $M_{kj}$ now are functions of $2p\theta_r$. Applying the $\alpha \beta$ transformation to the dynamical model presented in Equations (4) and (5), the following dynamics in the $\alpha \beta$ subspace are delivered

$$v_\alpha^{(\alpha \beta)}(a \beta) = R_s i_\alpha^{(a \beta)} + \frac{d}{dt} \psi_\alpha^{(a \beta)}$$

(8)

where the stator flux linkage in the $\alpha \beta$ subspace is expressed as in Equation (9)

$$\psi_\alpha^{(a \beta)} = L_s i_\alpha^{(a \beta)} + \Delta L_s e^{i2\theta_r} i_\beta^{(a \beta)} + \psi_m e^{i p \theta_r}$$

(9)
Finally, the dynamics in the $\alpha \beta$ stationary reference frame are rotated into the $d \ q$ synchronous reference frame by applying the unitary rotation matrix $\mathbf{U}$

$$
\mathbf{U} = \begin{bmatrix}
\cos(p \theta_r) & -\sin(p \theta_r) \\
\sin(p \theta_r) & \cos(p \theta_r)
\end{bmatrix}
$$

(10)

leading to Equation (11)

$$
\mathbf{v}_s^{(d\ q)} = R_s i_s^{(d\ q)} + L_s \frac{d}{dt} i_s^{(d\ q)} + \Delta L_s \frac{d}{dt} i_s^{(d\ q)} + j p \omega_r (\mathcal{L}_s i_s^{(d\ q)} + \Delta \mathcal{L}_s i_s^{(d\ q)} + \psi_m)
$$

(11)

defining $L_d = \mathcal{L}_s + \Delta \mathcal{L}_s$, $L_q = \mathcal{L}_s - \Delta \mathcal{L}_s$, the following Equations are obtained in the corresponding $d, q$ synchronous subspaces

$$
\mathbf{v}_s^d = R_s i_s^d + L_d \frac{d}{dt} i_s^d - p \omega_r L_q i_s^q
$$

(12)

$$
\mathbf{v}_s^q = R_s i_s^q + L_q \frac{d}{dt} i_s^q + p \omega_r L_d i_s^d + \omega_r \psi_m
$$

(13)

On the other hand, the electromechanical torque developed can be expressed as the change of stored energy, with respect to the mechanical position as given in Equation (14)

$$
T = \frac{\partial}{\partial \theta_r} \mathcal{W}_{fj}(\psi_s^{(d\ q)}, i_s^{(d\ q)})
$$

(14)

expressing Equation (14) in terms of the state variables in their respective synchronous orientations $d, q$ the following expression for the electromechanical is derived:

$$
T = \frac{3}{2} p [\psi_m i_s^q + i_s^d (L_d - L_q)]
$$

(15)

To predict the current state space vector $\mathbf{i}_s^{(d\ q)}$, within one horizon of prediction, the derivative function is approximated using the forward Euler approximation within sampling period $T_s$

$$
\frac{d}{dt} \mathbf{i}_s^{(d\ q)} = \frac{i_s^{(d\ q)}[k+1] - i_s^{(d\ q)}[k]}{T_s}
$$

(16)

The prediction model of the stator currents from Equations (12) and (13) within one horizon of prediction using Equation (16) leads to:

$$
i_s^d[k+1] = \left(1 - \frac{R_s}{L_d} T_s\right) i_s^d[k] + \frac{L_q}{L_d} T_s \omega_r[k] i_s^q[k] + \frac{1}{L_d} T_s v_s^d[k]
$$

(17)

$$
i_s^q[k+1] = \left(1 - \frac{R_s}{L_q} T_s\right) i_s^q[k] - \frac{L_d}{L_q} T_s \omega_r[k] i_s^d[k] + p \omega_r[k] \psi_m + \frac{1}{L_q} T_s v_s^q[k]
$$

(18)

where:

$$
\mathbf{v}_s^{(d\ q)}[k] = f^{(d\ q)}(S_{\ell j}, v_d)
$$

(19)

with $f^{(d\ q)}$ corresponding to a non-linear function that generates a specific voltage space vector in the $d\ q$ reference frame.

To establish the dc-link voltage dynamics, it has to be noted that due to the nature of this topology, depending on the switching state, the middle capacitor $C_2$ will be switched clamped through $x$ or $y$ establishing different current paths, which will affect the energy flow through each of the capacitors, as presented in Figure 4.
Figure 4. Current paths for each switching state.

As shown in Figure 4, depending on the switching state, the equivalent capacity changes, thus affecting the charging and discharging dynamics of each of the dc-link capacitors and the total stored energy in the dc-link, given in Equation (20)

$$\frac{d}{dt} W = C \sum_{n=1}^{3} \Delta V_n \frac{d}{dt} v_{cn}$$  \hspace{1cm} (20)

where $\Delta V_n$, $n \in [1, 2, 3]$ stands for the voltage drift and $v_{cn}$ to the corresponding capacitor voltage. Expressing now Equation (20) in terms of the capacitor voltage and the circulating dc current $i_{cn}$, Equation (21) is derived

$$C \sum_{n=1}^{3} \Delta V_n \frac{d}{dt} v_{cn} = \sum_{n=1}^{3} \Delta V_n i_{cn}$$  \hspace{1cm} (21)

From Equation (21), it can be inferred that the rate of change in the capacitor’s voltage is only due to the circulating current $i_{cn}$, as given in Equation (22)

$$C \frac{d}{dt} v_{cn} = i_{cn}$$  \hspace{1cm} (22)

To predict each individual capacitor voltage $v_{cn}$, within one horizon of prediction, the forward Euler approximation is used for the derivative function within sampling time $T_s$

$$\frac{d}{dt} v_{cn} = \frac{v_{cn}[k+1] - v_{cn}[k]}{T_s}$$  \hspace{1cm} (23)
\[ v_{cn} [k+1] = v_{cn} [k] + \frac{1}{C} T_s i_{cn} [k] \quad n \in \{ 1, 2, 3 \} \]  

where:

\[ i_{cn} [k] = g ( S_{\ell j}, i_j ) \]

### 3.2. Control Objectives

Using the previously derived discrete models for the PMSM and the dc-link voltage dynamics in Equations (17), (18), and (24), respectively, from which the \([k+1]\) system state is predicted when applying all the converter’s switching states \(S_{\ell j}\) in a time sample interval \(T_s\). The MPC control algorithm objectives are:

1. Capability to ensure full tracking of the stator currents references in the \(d\ q\) reference frame, within a maximum current limit.
2. Capability to valance the dc-link capacitor voltages, within the voltage reference.

To achieve these objectives, in Equation (26), a cost function \(g\) is defined, which considers the previously mentioned objectives and constrains. This function is constructed in terms of the respective quadratic errors for each of the previously defined state variables given a certain switching states \(i\).

\[ g[i] = \lambda_1 \left[ (i_{d*} - i_{d} [k+1, i])^2 + (i_{q*} - i_{q} [k+1, i])^2 + \hat{h}(i_{d} [k+1, i], i_{q} [k+1, i]) \right] + \lambda_2 \sum_{n=1}^{i} (v_{c*} - v_{cn}[k+1, i])^2 \]  

The first term in Equation (26) is linked to the stator currents error in the \(d\ q\) synchronous reference frame, with respect to their corresponding references \(i_{d*}\) and \(i_{q*}\). The term \(\hat{h}(i_{d} [k+1, i], i_{q} [k+1])\) corresponds to the saturation function on the maximum stator currents, which is described in Equation (27).

\[ \hat{h}(i_{d} [k+1, i], i_{q} [k+1]) = \begin{cases} 
\infty & |i_{d} [k+1]| > i_{max} \text{ or } |i_{q} [k+1]| > i_{max} \\
0 & |i_{d} [k+1]| \leq i_{max} \text{ and } |i_{q} [k+1]| \leq i_{max} 
\end{cases} \]  

The second term of Equation (26) corresponds to the dc-link capacitor voltage error on each capacitor, with respect to the dc voltage reference \(v_{c*}\). Coefficients \(\lambda_1\) and \(\lambda_2\) are the weighting factors, which are properly set to give the desired priority to the different variables to control. The control objective \(\mathcal{O}\) is to minimize the cost function \(g\) when evaluated for all available switching states \(S_{\ell j}\). In Figure 5, a flow diagram shows the proposed MPC algorithm working principle.

\[ \mathcal{O} = \min \{ g \} \]  

Figure 6 shows the implementation of the MPC strategy, with its corresponding stages.
Figure 5. MPC algorithm flow diagram.

\[ g[k] = \lambda_1 \left( (i_{\text{ref}}[k] - i_{\text{ref}}[k+1])^3 + (\dot{i}_{\text{ref}}[k] - \dot{i}_{\text{ref}}[k+1])^3 + \ddot{i}_{\text{ref}}[k] + 1, \dot{i}[k] + 1, i_{\text{ref}}[k] + 1, i_{\text{ref}}[k+1]) \right) + \lambda_0 \sum_{n=1}^{i} (i_{\text{ref}}[k]-i_{\text{ref}}[k+1, k])^{3} \]

Figure 6. MPC implementation diagram.
4. Results

This section presents the simulation and Hardware in the Loop validation results of the proposed Model Predictive Control strategy for the proposed quasi-nested arrangement. Simulation results have been carried out using PLECS software for modeling the converter topology and Permanent Magnet Synchronous Machine, and for the implementation of the MPC scheme in C code.

Hardware in the Loop implementation was carried out in a Plexim RT-Box CE HIL using a RT-Box LaunchPad Interface, running a TI C2000 microcontroller.

The analysis considered the same scenarios for the simulation and HIL validation in order to have a better conceptualization and verification of the results. The parameters used for simulation and implemented with HIL are shown in Table 2. Parameters used for the experimental validation have been selected within the limitations of the HIL processing capabilities.

Table 2. HIL-simulation parameters.

| Parameter          | Value       |
|--------------------|-------------|
| $v_{dc}$           | dc-link voltage 800 [V] |
| $C_{dc}$           | dc-link capacitors 1000 [µF] |
| $R_s$              | stator resistance 0.005 [Ω] |
| $L_{d}$            | direct-axis stator inductance 0.3 [mH] |
| $L_{q}$            | quadrature-axis stator inductance 0.3 [mH] |
| $p$                | pole pairs 4 |
| $T_s$              | sample time 10.19 [µs] |
| %                  | used processing capability 100% |

4.1. Simulation results

Simulation results have been performed for a current reference step inversion $i^q_s$ to show the MPC strategy performance to deal in the case of a high demanding torque change scenario. As presented in Figure 7a, the MPC strategy is capable to ensure full reference tracking, with high dynamic response, without overshoot or undershoot distortions.

As shown in Figure 7b, the MPC cost function also ensures voltage balancing, with near zero voltage drift of all three dc-link capacitors, thus ensuring near sinusoidal output currents and symmetrical output voltage waveforms, as presented in Figure 7c,d, respectively.

Figure 8 shows the performance of a classical Field Oriented Control (FOC) strategy, using level shifted PWM. As shown in Figure 8a, full current tracking control is achieved, as for the MPC scheme. However, as shown in Figure 8b, classical control schemes based on PWM and linear controllers are not capable to ensure voltage balance in the dc-link capacitors.

Moreover, it has to be noted that, when using the MPC scheme, the dc-link voltages do not exhibit any undershoot or overshoot transient during the current reference step inversion $i^q_s$, when compared with the performance of the dc-link voltages when using the FOC scheme.
Figure 7. Simulation results for current reference step inversion using the MPC control scheme: (a) $d$ $q$ stator currents, (b) dc-link capacitor voltages, (c) load three-phase currents, (d) line–line voltages $v_{ab}$, $v_{bc}$.

Figure 8. Simulation results for current reference step inversion using classical Field Oriented Control strategy with LS-PWM: (a) $d$ $q$ stator currents, (b) dc-link capacitor voltages.

### 4.2. Hardware in the Loop validation

Figure 9 shows the Hardware in the Loop implementation (HIL), consisting in a Plexim RT-Box CE HIL, a RT-Box LaunchPad Interface, and a TI C2000 microcontroller. In this implementation, the control strategy was implemented by the TI C2000 microcontroller, while the converter topology and the AC-drive were running in a real-time simulation. The obtained waveforms of the corresponding variables of interest were routed out using the RT-Box LaunchPad Interface and plotted into an oscilloscope.
In Figure 10, the quasi-nested topology implementation and the switching device characterization, corresponding to a SEMIKRON Semitrans-2 SKM75GB12V IGBT module, are shown. The selection criteria of this device considered: voltage blocking level and output current requirements.

Figure 11a,b shows the results for the load currents and output voltage waveforms, using the HIL test-bench, for a reference $i_q^*=0.8\ [pu]$. As presented in Figure 11, both current and voltage output waveforms exhibit symmetrical behaviour, and the currents in the $\alpha \beta$ reference frame also exhibit a sinusoidal pattern.

Figure 12 shows the results for each one of the dc-link capacitors voltage response, under the same operational condition for a reference $i_q^*=0.8\ [pu]$. As presented in the same figure, the three dc capacitor voltages exhibit a near constant voltage level without voltage unbalance, between them, ensuring full voltage-drift compensation.
Figure 11. HIL results: (a) alpha and beta stator current components, (b) line to line output voltages.

Figure 12. HIL results for the three dc-link capacitor voltages.
4.3. Converter Efficiency Analysis

The efficiency analysis of the quasi-nested topology has been performed in comparison with other classical multilevel topologies, such as the NPC, ANPC, and 4L-FC. The switching and conduction losses characteristics considered for this analysis were obtained from the data sheet of a Semikron Semitrans-2 SKM75GB12V IGBT. The calculation of switching and conduction losses used is based on the semiconductor data and the method given in [23]. Table 3 shows the results of the efficiency analysis for the different topologies studied (considering only the fundamental cell).

| Topology | Conduction Losses (W) | Switching Losses (mJ) |
|----------|------------------------|-----------------------|
| NPC      | 7.31                   | 20.5                  |
| ANPC     | 5.92                   | 3.8                   |
| 4L-FC    | 6.82                   | 3.2                   |
| 4L-QNC   | 5.55                   | 2.0                   |

Results presented in the previous table show that the proposed topology offers a better efficiency performance, in terms of conduction and switching losses compared to the other studied topologies, for the same operational conditions.

Performance analysis of the quasi-nested topology, with respect to its output voltage waveform, has been performed in comparison to other classical multilevel topologies. These results are presented in Table 4.

| Topology | THDv |
|----------|------|
| NPC      | 0.35 |
| ANPC     | 0.35 |
| 4L-FC    | 0.30 |
| 4L-QNC   | 0.23 |

As shown in Table 4, the proposed QNC yields the lowest THDv among the evaluated topologies.

4.4. Discussion

The proposed 4L-QNC shows a good performance in terms of the symmetry of the voltage and current waveforms and appears as an interesting alternative to classical multilevel topologies for applications on medium-voltage drives.

The use of Model Predictive Control has proved to be a good alternative to classical PWM strategies and oriented control schemes, dealing with both the requirement for synthesizing the required output voltage levels and to control the output currents and dc-link voltages. This final aspect has to be noted in terms of classical PWM strategies not being able to eliminate the voltage unbalance of d-link capacitors, requiring additional balancing schemes or asymmetrical modulation schemes. Being that MPC is a non-linear control strategy, it has the capability to easily deal with those constrains.

Finally, Hardware in the Loop simulation has proven to be a very useful platform to test the performance of the control strategy implemented in an independent microprocessor, while running the converter topology and load simulation model, in real time.

5. Conclusions and Future Work

In this work, a multilevel topology based on a quasi-nested arrangement, for applications in medium voltage AC-drives, has been described and validated using Hardware in the Loop real-time simulation. The proposed topology merged the benefits of classical multilevel topologies, with less active switches and without clamping devices.
The proposed strategy, based on a Model Predictive Control scheme, has been implemented in a TI C2000 microprocessor and validated using HIL real-time simulation, being capable to simultaneously control the load currents and the dc-link capacitors voltage balance. All these control requirements are included using a single prediction model of the state variables and a cost function considering the use of weighting factors, leading to an effective control scheme in a simple formulation. Moreover, when compared to a classical Field Oriented Control strategy, it showed a better dynamic performance without overshoot or undershoot, and it was also capable to deal with dc-link voltage drift, which appears when using classical control schemes based on the use of pulsed width modulation.

A performance comparison with other multilevel topologies has been made, where the main advantages of the quasi-nested topology, such as reduction in total number of semiconductors, switch stress, switching and conduction losses, and THD, have been highlighted for its application in medium and high-power applications.

Hardware in the Loop real-time simulation has proven to be an effective and near real setup implementation to test the effectiveness of the control scheme using a dedicated external microprocessor, while running the converter topology and AC-drive in a real-time simulation.

Future work will consider the implementation of adaptive weighting factors to reach an optimum solution for the cost function and also the implementation of an extended prediction horizons Model Predictive Control scheme.

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**Abbreviations**
The following abbreviations are used in this manuscript:

- $R_s$: Stator resistance
- $M_{kj}$: Mutual inductance of phases $k$ and $j$
- $L_k$: Inductance of phase $k$
- $L_d$: Direct axis inductance
- $L_q$: Quadrature axis inductance
- $L_s$: Average stator inductance
- $i_s(\alpha\beta)$: Stator current space vector in the $\alpha\beta$ stationary reference frame
- $i_s(dq)$: Stator current space vector in the $dq$ synchronous reference frame
- $v_s(\alpha\beta)$: Output voltage space vector in the $\alpha\beta$ stationary reference frame
- $v_s(dq)$: Output voltage space vector in the $dq$ synchronous reference frame
- $\psi_s(\alpha\beta)$: Stator flux linkage space vector in the $\alpha\beta$ stationary reference frame
- $\psi_s(dq)$: Stator flux linkage space vector in the $dq$ synchronous reference frame
- $\psi_m$: Permanent magnets flux linkage
- $S_\ell$: Switching state $\ell$
- $v_{cn}$: Voltage of the $n$ dc-link capacitor
- 3L-ANPC: Three Level Active Neutral Point Clamped
- 3L-FC: Three Level Flying Capacitor
- 3L-NPC: Three Level Neutral Point Clamped
4L-FC  Four Level Flying Capacitor
4L-QNC  Four Level Quasi-Nested Converter
ac Alternating Current
dc Direct Current
ANPC Active Neutral Point Clamped
CHB Cascaded H-Bridge
DSC Double-star converter
FC Flying Capacitor
HIL Hardware in the Loop
IGBT Isolated Gate Bipolar Transistor
IPMSM Internal Permanent Magnet Synchronous Machine
MLI Multilevel Inverter
MPC Model Predictive Control
MV Medium-Voltage
NLC Nearest level control
NPC Neutral Point Clamped
PWM Pulse Width Modulation
THD Total Harmonic Distortion

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