Investigation on the Effect of Dead Time on the Phase of Fundamental Voltage in VSI-PMSM Drive System

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Abstract. Both electric vehicle PMSM drive system and grid connected photovoltaic (PV) power generation need voltage source inverter (VSI). The dead time should be set properly when the power switches are turned on and off in the same bridge arm of VSI. During the dead time, the load is out of control, which will cause the abnormal output voltage amplitude and phase. However the influence of dead time on the output fundamental voltage phase has not been paid much attention to and studied. Firstly, in the paper, the phase shift of output fundamental voltage caused by dead time is simulated and analyzed for three-phase VSI - resistance inductance series (RL) load system under several conditions such as variable switching frequency, modulation index, output fundamental frequency and dead time. Secondly, take three-phase VSI - permanent magnet synchronous motor (PMSM) drive system for instance, the simulation analysis of output fundamental voltage phase shift and rotor positioning error caused by dead time are also performed, and an off-line method to compensate the fundamental voltage phase based on αβ coordinate is given. The above work provides a reference for further understanding the influence of dead time on fundamental voltage phase shift in VSI, so as to improve the monitoring and control precision of electric vehicle drive system. The analysis approach can be applicable to the grid connected photovoltaic (PV) power generation PMSM servo system.

1. Introduction
The physical structure and switching characteristics of power switches determine that their turn on-off transition takes time. For power electronic converters with bridge arm structure and voltage source power supply, such as voltage source rectifier (VSR) and voltage source inverter (VSI), the safe commutation conditions should be considered as follows: (1) any bridge arm can not be directly connected to prevent short-circuit of DC voltage source; (2) line current can’t be interrupted to prevent from surge voltage. Since VSI adopts reverse conduction power switches, freewheeling diodes (FWD) play the role of reverse voltage limitation and freewheeling, so the second condition is naturally satisfied. The setting of dead time means that the VSI-load system is out of control shortly during the transition (i.e. current commutation). Fortunately, the commutations of three-phase bridge arms don’t occur at the same time. As a result, the fundamental component of output phase voltage, output line voltage and load phase voltage deviate from the theoretical values, which leads to the poor power quality and the worse speed regulation performance of the drive system. These effects include the amplitude and phase changes of fundamental voltage, and some new high-order harmonic voltages arise accordingly, which directly affect the speed regulation performance of the drive system and produce a fixed position shift for PMSM rotor positioning. Also, the phenomenon would arise in other
VSI-powered systems, including PV grid connected power generation, PMSM servo system and wireless power transmission, etc.

The existing literature [1-17] basically focuses on the influence and compensation of dead time on the fundamental voltage amplitude. The impacts of the dead time are studied, including the disturbance due to dead time [1], the analytical calculation of the output harmonics due to dead time [2], common mode voltage characteristics considering the existence of dead time [3], as well as the inverter input current, dc-link dynamics and light-load instability for induction motor drives [4]. Some compensation approaches need sensing the polarity of inverter output current, which can lead to better compensation efficacy [5-7], and dead time compensation can be used to synthesize output voltage [8]. In reference [9], a mixed PWM technique for dead-time elimination and compensation in a grid-tied inverter grid-tied inverter is proposed. Reference [10, 11] discuss two novel dead time compensation methods. Reference [12] analyzes the time-domain characterization with dead time and sampling delay. Reference [13] provide the predictive current control for VSI considering dead time effect. Reference [14] is about harmonic quantitative analysis for dead time effect. Reference [15] depicts an optimal asymmetric variable dead-time setting. Reference [16] proposes a PWM generation approach without dead-time. In reference [17], according to the polarity of load current, a square wave voltage is obtained in equivalent form, and the influence of dead time on fundamental voltage is analyzed. At present, most of the dead time compensation strategies for SPWM or SVPWM algorithm aim at how to compensate the influence of dead time on fundamental voltage amplitude. The influence of dead time on fundamental voltage phase is neglected and seldom researched, which is closely related to the following parameters: dead time duration, switching frequency, the expected output frequency, load impedance property and output power level, etc. For inverter-PMSM drive system, the actual load is relevant to modulation index and output frequency. The influence of dead time on fundamental voltage phase has not been paid more attention to. For PMSM drive system, especially for the application which is very sensitive to position control, such as high precision aerospace, robot, CNC machine tool and position servo drive system, the dead time obviously affects rotor positioning, so this problem needs to be emphasized and solved.

For the basic pulse width modulation algorithms, there are three dead time setting methods: (1) on-delay, i.e. delayed turn on; (2) off-delay, i.e. premature turn off; (3) on/off delay. The former two have no the compensation ability of fundamental voltage amplitude, and the latter has the automatic compensation ability of fundamental voltage amplitude.

In this paper, for the first dead time setting method, in abc, αβ and dq coordinates, the influence of the dead time on the fundamental voltage phase is analyzed and simulated, and the compensation strategy of the influence of the dead time on the fundamental voltage phase is given in αβ coordinate. The mentioned work is helpful to develop the compensation method to overcome the influence of dead time on fundamental voltage phase.

2. Waveform analysis of VSI-RL load system

2.1. Effect of dead time on fundamental voltage waveform

The three-phase VSI-PMSM drive system is shown in Figure 1 (a), and the three-phase VSI-RL load system is shown in Figure 1 (b). In the two figures, diodes D1~D6 constitute three-phase rectifier, IGBTs S1~S6 constitute three-phase VSI.

![Figure 1](image-url)  
Figure. 1 Three phase VSI-load system (a) PMSM drive system; (b) RL load system
According to Figure 1, in the three-phase VSI-PMSM drive system, there are totally four kinds of voltages: (1) inverter bridge arm midpoint to DC negative voltage, including $u_{Ou}$ and $u_{Ou}$; (2) inverter output phase voltage, including $u_{UN}$, $u_{UV}$, and $u_{UN}$; (3) inverter output line voltage, i.e. load input line voltage, including $u_{UV}$, $u_{WV}$, and $u_{WU}$; (4) load phase voltage, including $u_{UN}$, $u_{VN}$, and $u_{WN}$.

In Figure 1, the input is three-phase 380V sinusoidal AC voltage, the input filter inductance is $200\mu H$, the DC filter capacitor is two groups of $4\times 680\mu F$ in series, and the load resistance is $5\Omega$, and the load inductance is 50mH.

As for on delay, as the frequently used setting of dead time, the corresponding relationship among ideal and actual driving pulses, output phase voltage and output phase current is shown in Figure 2, where $u_c$ is the carrier, $u_U$ and $i_U$ are the fundamentals of VSI output phase voltage and phase current respectively, $\phi$ is the load angle, PWM_H and PWM_L are the ideal driving pulses, and PWM_H’ and PWM_L’ are the actual driving pulses, $T_d$ denotes the dead time of $2\mu s$, and $T_o$ is the desired output period.

The ideal waveform, actual waveform and their difference of VSI output phase voltage are shown in Figure 3, where $u_{UN}$’ and $u_{UN}’’$ are the ideal and actual output phase voltages respectively, and $\Delta u_{UN}$ is their difference.

The ideal waveform, actual waveform and their difference of VSI output line voltage are shown in Figure 4, where $u_{UV}$’ and $u_{UV}’’$ are the ideal and actual output line voltage respectively, and $\Delta u_{UV}$ is their difference.

The ideal waveform, actual waveform and their difference of load phase voltage are shown in Figure 5, where $u_{UN}$ and $u_{UN}’$ are the ideal and actual load phase voltage respectively, and $\Delta u_{UN}$ is their difference.

It can be seen that the existence of dead zone causes distortion of the above voltage waveforms.

![Figure 2](image-url)
2.2. Effect of dead time on fundamental voltage phase
SPWM algorithm is adopted, switching frequency is 8 kHz, natural sampling is used, dead time is 2 μs, simulation step size is 1e-7s, modulation degree is 0.8, and DC voltage is 538.79 V. With and without dead time, the fundamental of VSI output phase voltage is shown in Figure 6, the fundamental of inverter output line voltage is shown in Figure 7, the fundamental of load phase voltage is shown in Figure 8, and output current waveform is shown in Figure 9. In figures 6~12 and 14, curve 1 refers to
without dead zone, and curve 2 refers to dead zone. It can be seen that the presence of dead zone causes the above fundamental voltage phase to lead, and the lead angle keeps the same.

**Figure 6.** Waveforms of the fundamental of inverter output phase voltage with and without dead time

**Figure 7.** Waveforms of the fundamental of inverter output line voltage with and without dead time

**Figure 8.** Waveforms of the fundamental of load phase voltage with and without dead time
Load phase current $i_U$ (5A/div)
0.28 0.285 0.29 0.295 0.30
-15 -10 -5 5 10 15
Time (0.005s/div)

Figure 9. Waveforms of the fundamental of load phase current with and without dead time

In the $\alpha\beta$ coordinate, $\alpha\beta$ components of the load phase current are shown in Figure 10. It can be seen when the dead zone exists, the two components of the output current decreases and the phase leads.

Load phase current $i_{\alpha\beta}$ (5A/div)
0.28 0.285 0.29 0.295 0.30
-15 -10 -5 5 10 15
Time (0.005s/div)

Figure 10. Waveforms of $\alpha\beta$ components in $\alpha\beta$ coordinate in view of the fundamental of load phase current with and without dead time

In the polar coordinate, the length and angle components of the load phase current are shown in Figure 11. It can be seen when the dead zone exists, the amplitude of the output current decreases and the phase leads.

Length and angle of load phase current (2A/div)
0.28 0.285 0.29 0.295
0 2 4 6 8 10 12 14
Time (0.005s/div)

Figure 11. Waveforms of length and angle in polar coordinate in view of the fundamental of load phase current with and without dead time
In the dq coordinate, the dq components of the load phase current are shown in Figure 12. It can be seen when the dead zone exists, the d component becomes large and the q component becomes small.

![Figure 12. Waveforms of dq components in dq coordinate in view of the fundamental of \( f_0 \) phase current with and without dead time](image)

### 2.3. Influence factors on the effect of dead time on fundamental voltage phase

In the following simulation analysis, simulation step size is \( 1e^{-7} \)s, using turn-on delay, natural sampling and SPWM algorithm.

When the dead time is 2 \( \mu \)s, the switching frequency is 8 kHz, and the modulation index is 0.8, the simulation results of the fundamental voltage phase shift caused by the change of expected output fundamental frequency are shown in Table 1.

#### Table 1. Fundamental voltage phase shift caused by the change of output fundamental frequency

| Expected \( f_0 \) (Hz) | Leading Angle (°) | Expected \( f_0 \) (Hz) | Leading Angle (°) |
|------------------------|-------------------|------------------------|-------------------|
| 0.5                    | 0                 | 50                     | 2.8               |
| 1                      | 0.1               | 75                     | 2.8               |
| 2                      | 0.3               | 100                    | 2.9               |
| 5                      | 0.8               | 150                    | 2.9               |
| 10                     | 1.5               | 200                    | 2.9               |
| 25                     | 2.4               | 250                    | 2.9               |
| 30                     | 2.6               | 300                    | 2.8               |
| 40                     | 2.7               | 400                    | 2.9               |

When the expected output frequency is 50 Hz, the switching frequency is 8 kHz, and the modulation index is 0.8, the simulation results of fundamental voltage phase shift caused by the change of dead time are shown in Table 2.

#### Table 2. Fundamental voltage phase shift caused by the change of dead time

| Dead time (\( \mu \)s) | Leading angle (°) | Dead time (\( \mu \)s) | Leading angle (°) |
|------------------------|-------------------|------------------------|-------------------|
| 0                      | 0                 | 2.5                    | 3.4               |
| 0.2                    | 0.3               | 3.0                    | 4.1               |
| 0.5                    | 0.7               | 3.5                    | 4.8               |
| 0.8                    | 1.1               | 4.0                    | 5.5               |
| 1.0                    | 1.3               | 4.5                    | 6.2               |
| 1.5                    | 2.0               | 5.0                    | 6.9               |
| 1.8                    | 2.4               | 6.0                    | 8.3               |
| 2.0                    | 2.7               | 8.0                    | 11.0              |
When the dead time is 2 μs, the expected output frequency is 50 Hz, and the modulation degree is 0.8, the simulation results of fundamental voltage phase shift caused by switching frequency change are shown in Table 3.

**Table 3. Fundamental voltage phase shift caused by the change of switching frequency**

| Switching frequency (kHz) | Leading angle (°) | Switching frequency (kHz) | Leading angle (°) |
|---------------------------|-------------------|---------------------------|-------------------|
| 1                         | 0.3               | 11                        | 3.8               |
| 2                         | 0.6               | 12                        | 4.1               |
| 4                         | 1.3               | 13                        | 4.5               |
| 5                         | 1.7               | 14                        | 4.8               |
| 7                         | 2.4               | 15                        | 5.2               |
| 8                         | 2.7               | 16                        | 5.5               |
| 9                         | 3.1               | 18                        | 6.2               |
| 10                        | 3.4               | 20                        | 6.9               |

When the dead time is 2 μs, the expected output frequency is 50 Hz, and the switching frequency is 8 kHz, the simulation results of fundamental voltage phase shift caused by modulation change are shown in Table 4.

**Table 4. Fundamental voltage phase shift caused by the change of modulation index**

| Modulation index | Leading angle (°) | Modulation index | Leading angle (°) |
|------------------|-------------------|------------------|-------------------|
| 0.05             | 49.2              | 0.55             | 4.0               |
| 0.10             | 22.6              | 0.60             | 3.7               |
| 0.15             | 14.9              | 0.65             | 3.4               |
| 0.20             | 11.1              | 0.70             | 3.1               |
| 0.25             | 8.9               | 0.75             | 2.9               |
| 0.30             | 7.4               | 0.80             | 2.7               |
| 0.35             | 6.3               | 0.85             | 2.6               |
| 0.40             | 5.5               | 0.90             | 2.4               |
| 0.45             | 4.9               | 0.95             | 2.3               |
| 0.50             | 4.4               | 1.00             | 2.2               |

From the above simulation data and other simulation data, it can be seen that the fundamental of output voltage will produce leading phase shift as long as there is dead time, no matter whether the delayed turn on or premature turn off, natural sampling or regular sampling, SPWM or SVPWM are adopted. The phase shift is strongly related to the expected output voltage frequency and modulation index. The longer the dead time, the greater the effect. The lighter the load, the more obvious the effect. Although the three-phase RL Series load is analyzed as an example, the conclusion is also applicable to the three-phase motor load. However, since the motor has back EMF, the influence of dead time on fundamental voltage phase should be changed to some extent. In addition, the simulation also verifies that when the on/off delay is used as dead time setting, the dead time has no effect on the amplitude and phase of the output fundamental voltage of the inverter-load system.

3. Phase shift of fundamental voltage in drive system

3.1. Effect of dead time on fundamental voltage phase shift

The simulation circuit of three-phase vector controlled VSI-PMSM drive system is shown in Figure 13. In the figure, the DC voltage is 300 V, PMSM has salient pole with sine wave back EMF, direct axis
and quadrature axis inductances are 0.02547 H and 0.02816 H respectively, stator resistance per phase is 18.7 Ω and flux linkage is 0.1716 V.S. When the angle is zero, rotor flux linkage aligns to u phase axis with lagging 90° (modified Park), load torque is 1.7 N.M, and moment of inertia J is 2.26e-05. The viscous damping f is 1.349e-05 N.M.S, the polar number P is 2, and the static friction Tf is 0 N.M. The expected operating speed is 3750 rpm, equivalent to 392.6990 rad/s and operating frequency of 125 Hz.

With or without dead zone, the waveform of steady-state stator current of PMSM is shown in Figure14, and the rotor angle with or without dead zone and their difference are shown in Figure15.

**Figure13.** Simulation circuit of three-phase vector controlled VSI-PMSM drive system

**Figure14.** Stator currents of PMSM in steady state with or without dead zone
It can be read out that with or without dead zone, the phase difference of PMSM stator current is about 8.10°, the rotor position difference is about 4.35°, and as expected, the relationship between them numerically is roughly two times.

### 3.2. Compensation of dead time on fundamental voltage phase shift

According to the whole operation condition of three-phase PMSM drive system, the phase shift angle of fundamental voltage caused by dead time under different operating conditions can be determined by simulation analysis and can be made into a phase compensation table, which is not given here, then the compensation angle can be determined by looking up the table. A modified vector controlled VIS-PMSM drive system considering the fundamental voltage phase shift caused by dead time is shown in Figure 16, where the polar stands for in polar coordinate αβ or dq for αβ coordinate or dq coordinate respectively. The block in dotted line is dedicated for phase shift compensation. \( \angle \theta_3 \) denotes the leading phase of fundamental voltage caused by dead time, and \( \angle \theta_4 \) is used as the phase shift compensation, and \( \angle (\theta_1 - \theta_2) \) is just the phase of rotation vector after compensation in αβ coordinate.

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**Figure 15.** PMSM rotor angles with or without dead zone and their difference

**Figure 16.** Modified three-phase VSI-PMSM drive system with dead time phase shift compensation
The amplitude and phase of one phase stator current is shown in Figure 17 when there is no dead zone, when there is no dead zone without phase shift compensation, and when there is dead zone with phase shift compensation. In the figure, "1" indicates without dead zone, 2 "indicates with dead zone without phase compensation, and "3 "indicates with dead zone with phase compensation. The upper right subgraph shows the stator current details near the peaks, and the lower left one shows those across the zeros. It is obvious to observe the effect of dead time on the produced voltage initial phase and the effect of compensation. After the compensation, there is no the phase shift any more. The position difference of PMSM rotor with dead zone and phase compensation is shown in Figure 18. It can also be seen that the used phase compensation can produce satisfactory phase compensation effect and the rotor position go back to normal.

**Figure 17.** Amplitude and phase relationship of one phase stator current when there is no dead zone, when there is dead zone without phase shift compensation, and when there is dead zone with phase shift compensation
4. Conclusions
By means of MATLAB/Simulink, three-phase VSI - resistance inductance series load system and three-phase VSI-PMSM drive system are analyzed and simulated, it can be concluded that the setting approaches of dead time of delayed turn-on and premature turn-off cause the leading phase of fundamental output voltage. The leading phase shift is closely related to the expected output frequency, switching frequency, sampling mode, modulation algorithm, modulation index, load property, modulation and other factors.

The leading phase will lead to fixed leading phase shift in closed-loop control system of PMSM drive system, which will affect the precise phase control of PMSM drive system. Reasonable phase compensation control strategy can be adopted and takes effect. The work in this paper is helpful to understand the influence of dead time on the phase of output fundamental voltage, especially applicable to the phase and position sensitive systems, including PMSM rotor positioning, PV grid connected power generation and wireless power transmission.

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