Temperature Sensitivity Analysis of Extended Source Double Gate Tunnel Field Effect Transistor

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Abstract Temperature-induced performance variation is one of the main concerns of the conventional stack gate oxide double gate tunnel field-effect transistor (SGO-DG-TFET). In this regard, we investigate the temperature sensitivity of extended source double gate tunnel-field-effect transistor (ESDG-TFET). For this, we have analyzed the effect of temperature variations on the transfer characteristics, analog/RF, linearity and distortion figure of merits (FOMs) using technology computer aided design (TCAD) simulations. Further, the temperature sensitivity performance is compared with conventional SGO-DG-TFET. The comparative analysis shows that ESDG-TFET is less sensitive to temperature variations compared to the conventional SGO-DG-TFET. Therefore, this indicates that ESDG-TFET is more reliable for low-power, high-frequency applications at a higher temperature compared to conventional SGO-DG-TFET.

Keywords Extended source · Linearity · stacked gate-oxide · Temperature sensitivity

1 Introduction

Conventional MOSFET scaling offers several advantages like high packing density, low-cost, and improved analog/RF performance. However, the continuous scaling of transistor size in the nanoscale regime deteriorates the performance of the device due to subthreshold slope limitation of 60 mV/decade, higher power dissipation, lower switching ratio ($I_{ON}/I_{OFF}$) and short-channel effects [1-4]. TFET, which operates on the mechanism of quantum tunneling, has emerged as an alternative device to solve the above issues of conventional MOSFET [5-8]. However, the major limitation of TFETs include ambipolarity and lower ON-state current ($I_{ON}$) [9]. Therefore, in order to overcome these issues, various methods have been reported by the researchers, such as TFET double-gate, hetero-dielectric, work-function engineering, stacked gate structure, electrically doped (ED), pocket doping, dielectric pocket, dual material and gate over source overlap [9-26]. In addition to the above issues, temperature-induced performance variation is also one of the major causes of concern in TFETs. Few works of literature [28-31] have reported the temperature sensitivity of different TFETs in terms of various performance parameters. Since the temperature induced performance variation in the device depends on the design, therefore, to improve the device reliability, a stack gate oxide ($SiO_2+HfO_2$) is applied, which makes the device less sensitive to various interface trap charges [32]. Further, to enhance the performance of conventional stack gate oxide double gate tunnel field-effect transistor (SGO-DG-TFET), the source is extended into the channel, and the device is named extended source double gate tunnel-field-effect transistor (ESDG-TFET) [24]. In this work, we investigate the temperature sensitivity in conventional SGO-DG-TFET and ESDG-TFET in terms of $I_{DS} - V_{GS}$ characteristics, analog/RF FOMs such as transconductance ($g_m$), cutoff frequency ($f_T$), gain-bandwidth product (GBP), maximum oscillating frequency ($f_{max}$), and linearity distortion FOMs such as $g_{m3}$, VIP3, IIP3 and IMD3 performance parameters using TCAD simulations.

The remaining part of this work is organised as follows. Section 2 presents the structural and simula-
tion details of the device. Section 3 describes the simulation results in three parts. The first part compares the $I_{DS} - V_{GS}$ characteristics of SGO-DG-TFET and ESDG-TFET. Second part investigates the analog/RF FOMs, and the third part presents the linearity and distortion FOMs at different temperatures. Finally, the key findings of this paper is presented in Section 4.

2 Device structure, parameters and simulation setup

The structural views of conventional SGO-DG-TFET and ESDG-TFET for the parameters listed in Table 1 are illustrated in Fig. 1(a) and Fig. 1(b), respectively. The ESDG-TFET device structure comprised of silicon film thickness ($t_{\text{Si}}$) of 15 nm and $P^+$ source with a doping concentration of $1 \times 10^{20} \text{ cm}^{-3}$ extended into the channel, which has a doping concentration of $1 \times 10^{17} \text{ cm}^{-3}$. The $N^+$ drain region has a doping concentration of $1 \times 10^{19} \text{ cm}^{-3}$. The source width and height are denoted by $S_W$ and $S_H$, respectively. Similarly, $C_W$ and $C_H$ are the width and height of the channel. Moreover, a stack gate oxide (1-nm $\text{SiO}_2$ and 2-nm $\text{HfO}_2$) is used, with a gate material work-function of 4.2 eV. The dimensions $S_H$ and $C_H$ are considered as 5 nm [24]. The gate is extended over the channel towards the drain side, acting as a gate field plate (GFP). This enhances the performance of the ESDG-TFET as the tunneling point (TP) path under the GFP is shorter than the tunneling line (TL) path under the gate, leading to earlier band-to-band tunneling under the GFP [27].

For simulations, a nonlocal band-to-band tunneling model is used to calculate the tunneling current in the device. SRH and auger recombination models are considered to observe the minority carrier recombination in the device. The bandgap narrowing model is activated because of high doping concentration in source and drain, concentration-dependent mobility model is used for concentration-dependent carrier transport.

3 Results and discussion

This section presents the impact of temperature variations in conventional SGO-DG-TFET and ESDG-TFET in terms of $I_{DS} - V_{GS}$ characteristics, analog/RF, and linearity performance parameters for temperature ranging from 300K to 480K

3.1 Temperature sensitivity analysis of $I_{DS} - V_{GS}$ characteristics

Fig. 2(a) and Fig. 2(b) illustrate the effect of temperature variations on $I_{DS} - V_{GS}$ characteristics for conven-
ional SGO-DG-TFET and ESDG-TFET in logarithmic scale at $V_{DS} = 1.0\, V$. From these figures, smaller $I_{ON}$ variations with temperature are noted for both devices because $I_{ON}$ depends mainly on the band-to-band tunneling instead of temperature. However, OFF-state current ($I_{OFF}$) varies significantly with temperature because of its dependency on minority carrier concentration, which increases with temperature. These results demonstrate that the temperature dependence of ESDG-TFET provides 0.30%/K change in $I_{ON}$, whereas it provides 0.44%/K change for SGO-DG-TFET. Hence, the $I_{ON}$ variation with temperature ranging from 300K to 480K is 0.14%/K lesser for the ESDG-TFET in comparison with SGO-DG-TFET. Also, due to the extended source, higher $I_{ON}$ is observed for ESDG-TFET as compared to SGO-DG-TFET.

### 3.2 Temperature sensitivity analysis of analog/RF figure of merits

This section compares the temperature sensitivity for SGO-DG-TFET and ESDG-TFET in terms of analog/RF FOMs such as $g_m$, $f_T$, GBP, and $f_{max}$. Parasitic capacitances ($C_{gs}$ and $C_{gd}$) are crucial parameters to analyze the analog/RF and linearity performance of the device. The plots for variations in $C_{gs}$ with $V_{GS}$ at the temperature range from 300K to 480K are shown in Fig. 3(a) and Fig. 3(b). The $C_{gd}$ variation with temperature for both the device are illustrated in Fig. 3(c) and Fig. 3(d), respectively. From these figures, temperature variations in $C_{gs}$ and $C_{gd}$ for both the devices are noted smaller at lower $V_{GS}$ as compared with higher $V_{GS}$. Further, the $C_{gs}$ and $C_{gd}$ for ESDG-TFET is noted to be larger than that of SGO-DG-TFET. Transconductance ($g_m$) is one of the critical parameters in the analog/RF and linearity performance analysis. Higher $g_m$ is required to achieve higher gain, $f_T$ and GBP in the design of analog circuits [33]. Fig. 4(a) and Fig. 4(b) illustrate the $g_m$ variations with temperature for SGO-DG-TFET and ESDG-TFET. These results demonstrate that in the subthreshold region $g_m$ of both the devices are very small, and it starts increasing due to steep rise in the ON-state current. However, it starts decreasing after a particular value of $V_{GS}$ because of mobility degradation [33]. Further, noted that $g_m$ of ESDG-TFET is larger as compared to SGO-DG-TFET. Moreover, these results demonstrate that ESDG-TFET shows 0.21%/K variations in $g_m$ for temperature ranging from 300K to 480K whereas, at the same biasing and temperature range, 0.37 %/K variation is noted for SGO-DG-TFET.

Another critical parameter for RF performance assessment of the device is cutoff frequency ($f_T$). It is defined as the frequency at which current gain becomes unity [31]. It is formulated as follows

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$  

(1)

It means $f_T$ depends on the parasitic capacitances and $g_m$ of the device. Fig. 5(a) and Fig. 5(b) depict the variation in $f_T$ with $V_{GS}$ at the temperature ranging from 300K to 480K for SGO-DG-TFET and ESDG-TFET. As seen from Fig. 5(a) and Fig. 5(b), $f_T$ initially increases with $V_{GS}$ due to an increase in $g_m$ and then decreases after a certain value of $V_{GS}$ due to the increased parasitic capacitances and reduced $g_m$ because of mobility degradation. These results demonstrate that ESDG-TFET exhibits 0.22%/K variation in $f_T$ for temperature range from 300K to 480K, whereas for the same biasing conditions and temperature range SGO-DG-TFET exhibits 0.41 %/K variation. Moreover, from these results, it is noted that $f_T$ for ESDG-TFET is higher than the conventional SGO-DG-TFET.
GBP is another crucial parameter for RF performance assessment of the device. It is defined as follows:

\[ GBP = \frac{g_m}{20\pi C_{gd}} \]  

(2)

The GBP variations for conventional SGO-DG-TFET and ESDG-TFET with \( V_{GS} \) at the temperature range from 300K to 480K are shown in Fig. 5(c) and Fig. 5(d), respectively. Simulation results demonstrate that maximum GBP is obtained for ESDG-TFET compared to the conventional SGO-DG-TFET due to the same
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Fig. 5 $f_T$ variation with temperature for (a) conventional SGO-DG-TFET (b) ESDG-TFET; gain bandwidth product (GBP) variation with temperature for (c) conventional SGO-DG-TFET (d) ESDG-TFET.

Fig. 6 Maximum oscillating frequency ($f_{\text{max}}$) variation with temperature for (a) conventional SGO-DG-TFET (b) ESDG-TFET.

reasons discussed earlier for the $f_T$. From the comparative analysis of both the devices, 0.19 %/K more variations in conventional SGO-DG-TFET is observed as compared with the ESDG-TFET. Another important parameter for RF performance analysis of the device is maximum oscillating frequency ($f_{\text{max}}$). Which is formulated as follows [28]

$$f_{\text{max}} = \sqrt{\frac{f_T}{8\pi C_{gd} R_{gd}}}$$  \hspace{1cm} (3)
The $f_{\text{max}}$ variation for SGO-DG-TFET and ESDG-TFET with $V_{\text{GS}}$ at the temperature ranges from 300K to 480K is illustrated in Fig. 6(a) and Fig. 6(b), respectively. These simulation results demonstrate that $f_{\text{max}}$ of ESDG-TFET is higher than the conventional SGO-DG-TFET due to the higher $f_T$. From the comparative analysis of both the devices, for the temperature ranging from 300K to 480K, 0.09 %/K more variations for conventional SGO-DG-TFET is observed as compared with the ESDG-TFET.

3.3 Temperature sensitivity analysis of linearity and distortion figure of merits

Modern high-speed communication system needs a device with maximum linearity and minimal distortion [33]. To attain better linearity, $g_m$ of the device should remain constant with $V_{\text{GS}}$. However, $g_m$ of MOSFET and TFET shows the variation with $V_{\text{GS}}$ and temperature. In this context, this paper examines the temperature sensitivity for linearity and distortion parameters i.e $g_{m2}$, $g_{m3}$, VIP3, IIP3, and IMD3 for conventional SGO-DG-TFET and ESDG-TFET. Where these parameters are defined as follows [33]

$$\text{VIP3} = \sqrt{24 \times \left( \frac{g_{m1}}{g_{m3}} \right)}$$

$$\text{IIP3} = \frac{2}{3} \times \left( \frac{g_{m1}}{g_{m2} \times R_S} \right)$$

$$\text{IMD3} = \left[ \frac{9}{2} \times (\text{VIP3})^2 \times (g_{m3})^2 \times R_S \right]$$

Where $R_S$ is assumed to be 50 $\Omega$ for most RF applications. To achieve better linearity and lower distortion of the device, VIP3 and IIP3 should be higher, while IMD3 must be lower [28]. Fig. 7(a) and Fig. 7(b) depict the impact of temperature variations on $g_{m2}$ with $V_{\text{GS}}$ for conventional SGO-DG-TFET and ESDG-TFET, respectively. Results demonstrate that $g_{m2}$ increases with temperature for both the devices, while the variation is lower for ESDG-TFET as compared to SGO-DG-TFET. Fig. 7(c) and Fig. 7(d) depict the impact of temperature variations ranging from 300K to 480K on $g_{m3}$ with $V_{\text{GS}}$ for conventional SGO-DG-TFET and
ESDG-TFET, respectively. Results demonstrate that $g_m$ variation is negligible at lower $V_{GS}$ for both devices. Further, it is also observed that ESDG-TFET is less sensitive to temperature variation compared to conventional SGO-DG-TFET.

Fig. 8(a) and Fig. 8(b) show variation of VIP3 with $V_{GS}$ at different temperatures from 300K to 480K for conventional SGO-DG-TFET and ESDG-TFET. A device with a higher value of VIP3 indicates better linearity. Therefore, the VIP3 results demonstrate that ESDG-TFET shows better linearity compared to SGO-DG-TFET. Further, it is also observed that noted that both the devices are temperature sensitive for lower side and higher side of $V_{GS}$. 
Table 2 Temperature sensitivity in % per kelvin of various parameters for conventional SGO-DG-TFET and ESDG-TFET.

| Parameters | SGO-DG-TFET | ESDG-TFET |
|------------|-------------|-----------|
| $I_{ON}$   | 0.44 %/K    | 0.30 %/K  |
| $I_{OFF}$  | $1.1 \times 10^3$ %/K | $8.8 \times 10^3$ %/K |
| $g_m$      | 0.37 %/K    | 0.21 %/K  |
| $f_T$      | 0.41 %/K    | 0.22 %/K  |
| GBP        | 0.41 %/K    | 0.21 %/K  |
| $f_{max}$  | 0.19 %/K    | 0.098 %/K |

IIP3 variation with $V_{GS}$ at different temperature ranges from 300K to 480K for conventional SGO-DG-TFET and ESDG-TFET is shown in Fig. 8(c) and Fig. 8(d). Again, an increase in IIP3 indicates improvement in the linearity performance of the device. Therefore, the simulation results demonstrate that ESDG-TFET exhibits better linearity compared to SGO-DG-TFET. It was further noted that both devices are temperature sensitive at lower and higher $V_{GS}$.

A device with lower IMD3 indicates that the device can withstand with higher distortions. Fig. 8(e) and Fig. 8(f) illustrate the variations in IMD3 with $V_{GS}$ for conventional SGO-DG-TFET and ESDG-TFET at different temperature range from 300K to 480K. Therefore, these results demonstrate that ESDG-TFET exhibits 0.10%/K variation in IMD3 for temperature range from 300K to 480K at $V_{GS}$ = 1.6 V and $V_{DS}$ = 1.0 V, whereas for the same biasing conditions and temperature range, conventional SGO-DG-TFET exhibits 0.41%/K variation. This indicates that ESDG-TFET shows better inter modulation distortion performance as compared to conventional SGO-DG-TFET. Finally, the temperature sensitivity in % per kelvin of various device parameters for SGO-DG-TFET and ESDG-TFET are presented in Table 2.

4 Conclusions

The actual performance of the device at the operating temperature may differ from the room temperature. Therefore, in this work, we have performed a comparative temperature sensitivity analysis for conventional SGO-DG-TFET and ES-DG-TFET. It has been observed that ESDG-TFET shows 0.14%/K less sensitivity for ON-state current to temperature variation ranging from 300K to 480K, while 0.16%/K less sensitivity for transconductance and 0.15%/K less sensitivity for cut-off frequency than for SGO-DG-TFET. Therefore, it can be stated that ESDG-TFET is more reliable at higher temperatures than conventional SGO-DG-TFET.

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