Bilayer Graphene Quantum Dot Defined by Topgates

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Abstract. We investigate the application of nanoscale topgates on exfoliated bilayer graphene to define quantum dot devices. At temperatures below 500 mK the conductance underneath the grounded gates is suppressed, which we attribute to nearest neighbour hopping and strain-induced piezoelectric fields. The gate-layout can thus be used to define resistive regions by tuning into the corresponding temperature range. We use this method to define a quantum dot structure in bilayer graphene showing Coulomb blockade oscillations consistent with the gate layout.
Since the first synthesis of graphene [1] by exfoliation, the realization of quantum dots (QDs) in this material, e.g. as promising host for spin qubits [2], has been an interesting but challenging topic [3]. One of the outstanding challenges to fabricate reliable graphene QDs includes the difficulty in opening a sizeable and well-defined bandgap in graphene in order to define a QD confinement potential. It is possible to open a bandgap in three ways (see, e.g., [4]): (1) by constricting the graphene in one dimension to form nanoribbons [5, 6, 7], (2) by biasing bilayer graphene [8, 9, 10, 11, 12] and (3) by applying strain to graphene [13, 14, 15, 16, 17, 18].

Nanoribbon-QDs (1) produced by etching have been realized showing Coulomb blockade at sufficiently low temperature [7] as well as single-electron pumping [19]. A disadvantage of this method is that the required widths are lithography challenging and cause large carrier-mobility degradation. Another way to obtain nanoribbons utilizes unzipping carbon nanotubes which yield clean nanoribbon-QDs exhibiting Coulomb blockade, Kondo effect, clear excited states up to 20 meV, and inelastic cotunnelling [20]. Following approach (2) QDs of arbitrary geometries and smooth tunable tunnel barriers may be achieved by local electrostatic gating of bilayers, as recently demonstrated by Allen et al. [21] in a dual-gate design. In their device a suspended bilayer membrane has been placed between a global backgate and small topgates, not touching the membrane. With an appropriately shaped top-gate a Coulomb-island was defined and corresponding conductance oscillations through this QD have been observed. It would be highly desirable to obtain QD-devices on a substrate, making the integration of more complex devices feasible. Recent success has been reported by Goossens et al. where the graphene bilayer is sandwiched between hexagonal boron nitride bottom and top gate dielectrics [22]. In this work we follow a simpler approach and employ bilayer-graphene exfoliated on a GaAs-substrate. Due to leakage currents as a result of bonding we decide to use an undoped substrate and therefore pass on a backgate. A dielectric and metallic surface gates are deposited on top which are shaped to form a QD. At sufficiently low temperature we observe Coulomb blockade oscillations, consistent with the charging energy and the location of the transport channel expected from the gate layout. At even lower temperature the conduction is exponentially suppressed over the whole gate voltage range. We attribute this behaviour to resistive regions forming underneath the gate metal, leading to hopping transport at sufficiently low temperature.

As the graphene is globally covered with a dielectric and not in direct contact with the metal gate we propose strain combined with strain induced piezoelectric fields inside the substrate as one of the possible origins for this behaviour.

Fig.1(a) shows a schematic of the device employed. The substrate of our device is undoped GaAs to increase the mobility at low temperatures due to the very low roughness, compared to the commonly used Si substrates with thermally oxidized SiO$_2$ on top [23]. In order to allow optical separation between graphene of different layer numbers a 200 nm thick GaAs/AlAs multilayer has been grown by molecular beam epitaxy onto the substrate which acts as a distributed Bragg reflector [23, 24]. Following the exfoliation technique [1] a bilayer of graphene has been identified by
optical microscopy and subsequent Raman spectroscopy. For the device a flake of about 20\(\mu\)m in length and 4\(\mu\)m in width has been chosen. It is contacted by pads of 10 nm thermally evaporated titanium followed by 50 nm gold. A dielectric is fabricated \cite{25} by first completely covering the whole device with an Al-layer of 2 nm thickness by thermal evaporation. After venting the evaporation chamber, the thin Al layer is fully oxidized. It protects the graphene during the subsequent high-energy process step in which a 15 nm thick gate dielectric of Al\(_2\)O\(_3\) is sputtered. Finally, topgates are deposited by thermal evaporation of 10 nm of titanium and 40 nm of gold. In analogy to standard GaAs and recent suspended bilayer graphene structures \cite{21} the gate geometry has been chosen to define a QD with dimensions as shown in Fig. 1(a). The continuous gates are labelled C1 and C2, the split-gates S1 and S2, respectively. For comparison, a control device with a 3\(\mu\)m wide gate covering the bilayer has been fabricated. A voltage \(U_{SD}\) is applied between the contacts labelled “source” and “drain”.

Fig. 1(b) shows the source-drain current \(I_{SD}\) as function of bias voltage \(U_{SD}\) at different temperatures for the QD device (blue curves). For comparison, the characteristic for the control device at \(T = 550\) mK is shown by the red curve. All
gate voltages are set to 0 V. A non-linear characteristic with decreasing conductance is observed for the QD device as the temperature is lowered. The conduction is completely suppressed at the base temperature of $T \approx 300 \text{ mK}$ below a threshold voltage for onset of conduction at $U_t \approx \pm 9 \text{ mV}$. Note that this source-drain gap is not lifted for voltages of ±1 V applied simultaneously to all gates. At higher voltages gate-leakage sets in. Hence, even without the application of an electric field the data show an apparent transport gap. This gap is not observed in the wide-gate control-device [red trace in Fig. 1(b)]. Note, however, that at high voltages applied to the control device (see Fig. 2(b)) transport under the gate becomes suppressed and an electric field induced opening of a band gap and resulting nonlinear IV characteristics are found (not shown). Therefore, the conduction suppression is likely to be caused only when the surface gates are small and only within their proximity. Below we will discuss the assumption, that a combination of piezoelectric fields and strain due to a mismatch in thermal expansion coefficients of gate metal, insulating layer and GaAs substrate is the origin of the conduction suppression. The local strain can be much stronger in smaller structures of the same thickness (see supplementary data).

A conduction suppression only in the vicinity of the surface gates would leave a small island conducting in the center of the gate structure, which defines the QD. However, in order to allow probing the QD by transport measurement the temperature has to be raised to allow measurable transport through the structure. Fig. 2 shows a corresponding measurement at $T = 550 \text{ mK}$. Here the conductance $G$ is shown as function of voltage applied equally to gates S1 and S2, $U_{S1} = U_{S2}$. A series of conduction peaks can be seen. We find that the application of a perpendicular magnetic field generally enhances the on-off ratio of these peaks (shown as blue trace), keeping the peak spacing approximately unchanged. For comparison, Fig. 2(b) shows the conduction-variation of the wide-gate control-device as function of gate voltage $U_C$, also measured at $T = 550 \text{ mK}$. The conduction reduces smoothly towards the charge neutrality point, showing the typical characteristic of gated bilayer devices. No resonance or Coulomb blockade features have been observed. For voltages beyond 10 V gate-leakage sets in which prevented the observation of carrier-type change. From this plot we conclude that the transport in the gated graphene layer is determined by holes.

Figs. 2(c) and (d) plot the conduction as the pairs of gate voltage $(U_{C1}, U_{C2})$ and $(U_{S1}, U_{S2})$ are varied, respectively. Apparently, all gates couple to the transport channel so that the total-conductance determining channel must be localized and close to the center of the gate structure. This is a strong indication that resistive regions are forming underneath the gate metal, confining the transport to the QD region. It can also be seen that while gates S1 and S2 couple approximately equally to the transport channel, C1 and C2 show a different coupling. The ratio of the corresponding gate capacitance is $C_{C1}/C_{C2} \approx 4.2$ and $C_{S1}/C_{S2} \approx 0.84$.

A discrete Fourier analysis of the conduction trace is shown in Fig. 2(e). It has been carried out for the conductance $G$ as function of simultaneously varied $U_{C1}$ and $U_{C2}$, over a range of $U_{C1+C2} = -1 \ldots + 1 \text{ V}$. The series of power spectra was calculated
Figure 2. Coulomb blockade characteristic of QD device at temperature $T = 550 \text{mK}$.

(a) Conductance $G$ versus $U_{S1+S2}$, for perpendicular magnetic fields of $B = 0$ (red) and $B = 3.3 \text{T}$ (blue), respectively. The magnetic field was set to $B = 3.3 \text{T}$ in the following plots. (b) Conductance of the control-device versus gate voltage $U_C$. (c) and (d) show the conductance versus different gate voltages, as labeled. The line-cut at the bottom corresponds to the lowest voltage on the vertical axis. (e) displays the power spectrum obtained from a discrete Fourier transform of $G(U_{C1+C2})$, averaged over $U_{S1+S2} = -0.3 \ldots + 0.3 \text{V}$. The inset shows the conductance $G$ as function of $U_{C1+C2}$ and $U_{S1+S2}$. The upper part of (f) displays the current $I_{SD}$ as function of bias voltage $U_{SD}$ and gate voltage $U_{C1}$ with all other gates grounded. The bottom part shows the current $I_{SD}$ for the cut indicated by the dashed red line in the upper panel.

for fixed voltages $U_{S1+S2}$ simultaneously applied to gates S1 and S2, over a range of $U_{S1+S2} = -3 \ldots +3 \text{V}$. The inset of Fig. 2(e) shows the corresponding $G(U_{S1+S2},U_{C1+C2})$-plot, and the main graph displays the average over all Fourier power spectra. A pronounced peak at a frequency of $17 \text{V}^{-1}$ can be seen, with a corresponding period of $\Delta U_{C1+C2} \approx 59 \text{mV}$.

Fig. 2(f) shows the variation of the current through the device as function of $U_{C1}$ and voltage applied between source and drain, $U_{SD}$. The current variation shows a typical Coulomb blockade oscillation (CBO) with a charging energy extracted from the Coulomb-diamond of $E_C \approx 2 \text{meV}$. The resulting total capacitance $C_T$ of the corresponding Coulomb island is then $C_T = e^2/E_C \approx 80 \text{aF}$. From the self-capacitance model one would obtain a disc-shaped Coulomb island with a diameter of $d_{\text{island}} \leq C_T/4\epsilon_0\epsilon_r \approx 220 \text{nm}$, using a dielectric constant $\epsilon_r = 10.4$, which is the average between $\epsilon_{\text{GaAs}} = 12.9$ of GaAs and $\epsilon_{\text{Al}_2\text{O}_3} = 7.9$ of Al$_2$O$_3$ [25]. The size estimated from this simple model is consistent in order of magnitude with the size of the gate defined island. Assuming that the main peak in the Fourier spectrum of Fig. 2(e)
corresponds to Coulomb blockade oscillations of a single island the gate capacitance
\( C_{C1+C2} = \frac{e}{\Delta U_{C1+C2}} \approx 2.7 \text{ aF} \). Using the ratio \( \frac{C_{C1+C2}}{C_{S1+S2}} = 2.25 \) extracted from the data in the inset of Fig. 2(e) one obtains a total gate capacitance of \( C_G \approx 3.9 \text{ aF} \).

In order to investigate the nature of the interface between Coulomb island and electron reservoir the temperature dependence of the conduction has been analyzed further in Fig. 1(c) and (d). The voltage settings on the gates (all 0 V) correspond to a region where conductance is not suppressed by Coulomb blockade. Therefore the suppression of conduction for \( |U_{SD}| \leq 9 \text{ mV at } T = 300 \text{ mK} \) [Fig. 1(b)] originates from the interface, i.e. the region underneath the surface-gates. The temperature dependence can be described by the exponential law \( R(T) = R_0 \exp (T_0/T)^p \), where \( T_0, R_0 \) and \( p \) are model specific constants. In order to determine the exponent \( p \) we calculate the value from \( \ln W = A - p \ln T \), where \( W = -\partial \ln R(T)/\partial \ln T = p(T_0/T)^p \) is the reduced activation energy and \( A \) is a constant [26]. The result can be seen in Fig. 1(d) extracting \( p = 1.1, R_0 = 2.9 \times 10^6 \text{ Ohm and } T_0 = 5.3 \text{ K} \). An exponent \( p \) close to 1 suggests activated transport with an activation energy \( E_a = 2k_B T_0 = 0.9 \text{ meV} \), with \( k_B \) Boltzmann’s constant.

Considering that the conduction at \( T \approx 300 \text{ mK} \) remains suppressed for voltages \( U_{C1+C2+S1+S2} = -1 \text{ V} \ldots +1 \text{ V} \) equally applied to all surface gates [see also Fig. 2(e) for CBO within \( U_{C1+C2} = -1 \text{ V} \ldots +1 \text{ V} \) at \( T = 550 \text{ mK} \)] the corresponding transport gap must be significantly larger than the activation energy \( E_a \). Therefore we interpret the simple activated behavior as a signature of nearest neighbor hopping (NNH) through localized states within the transport gap [27, 28]. Previously, NNH has been identified in bilayer graphene in which a band gap has been opened by a perpendicular electric field in a similar temperature range [29]. For our temperature study in Fig. 1(c) and (d) no external perpendicular electric field has been applied that could justify the existence of a band gap [8, 9]. There might be a built-in electric field due to possible strong hole doping as indicated by the control-device in Fig. 2(b). However, this field is unlikely to lead to the QD definition according to the gate layout. It has previously been established that deformation – described by a strain tensor \( \varepsilon \) – can induce a bandgap as well [30, 31, 32]. The bandstructure of strained bilayer graphene has been theoretically investigated [33, 17], and a band gap has been predicted for perpendicular strain exceeding \( \varepsilon_{zz} = 0.25 \). Also Choi et al. [16] predict a gap when the two layers of bilayer graphene are differently strained. To support our arguments we perform simulations of the deformation and the forces built up inside the material described by a stress tensor \( \sigma \). Indeed, at the substrate-graphene-dielectric interface of our sample both strain types exist.

The origin of deformation and internal forces in our sample is the fact that the insulator material and the metallic gates have different thermal expansion coefficients \( \alpha \). The sample holder was kept close to room temperature during the evaporation of the surface gates. The temperature of the sample during the Al\(_2\)O\(_3\) deposition was determined to be approximately 470 K. As the sample-temperature is changed the different materials will contract or expand at different rates and the deposited layers
Figure 3. Simulation of sample-deformation at \( T = 300 \text{ mK} \), using thermal expansion coefficients \( \alpha_{\text{GaAs}} = 14.2 \cdot 10^{-6} \text{ K}^{-1} \), \( \alpha_{\text{Ti}} = 8.6 \cdot 10^{-6} \text{ K}^{-1} \), \( \alpha_{\text{Al}_2\text{O}_3} = 6.5 \cdot 10^{-6} \text{ K}^{-1} \), and \( \alpha_{\text{GaAs}} = 5.7 \cdot 10^{-6} \text{ K}^{-1} \); assumed substrate temperature during deposition of \( \text{Al}_2\text{O}_3 \) was \( T_{\text{dep}} = 470 \text{ K} \); for Ti and Au \( T_{\text{dep}} = 290 \text{ K} \) was assumed. (a) Overview of the 3D model and its deformation, scaled by a factor of 30. (b) plots the stress \( \sigma_{zz} \) and (c) the displacement in \( z \) of the graphene layer.

will exert a force on the substrate resulting in mutual deformation. The deformation in turn generates an internal elastic stress \( \sigma \) that tends to restore the material to its original undeformed state.

The simulated deformation of the sample at \( T = 300 \text{ mK} \) is shown in Fig. 3(a), with parameters provided in the caption. The simulation has been performed using a commercial finite element solver \[34\]. Plotting the displacement of the GaAs-\( \text{Al}_2\text{O}_3 \) interface (i.e. the location of the graphene flake) in Fig. 3(b) and (c) reveals that only a small rectangular island bordered by C1 and C2, as well as S1 and S2 remains almost free of displacement and therefore stress. In contrast, the graphene-portion covered by the gates is strongly displaced and therefore experiences strain due to internal forces of the surrounding material. In addition, the bending will result in a different strain for the two graphene layers.

The stress was simulated for both a GaAs substrate and a Si substrate covered by \( \text{SiO}_2 \) and it turns out that the stress inside the graphene layer is in the same order of magnitude but slightly smaller in the case of Si/\( \text{SiO}_2 \). Concerning the latter graphene devices with comparable nanoscaled topgates have previously been investigated \[12, 21, 29\], but a transport gap has not been observed. Therefore the strain itself is not sufficient to clearly explain our results. In contrast to Si/\( \text{SiO}_2 \) in GaAs the strain will also lead to an electric displacement field \( D \) due its piezoelectric properties. By taking them into account in the simulations the \( z \)-component of the electric displacement field \( D_z \) at the boundary between the insulator and our piezoelectric substrate can be derived and converted into an electric field \( E_z \) by the
relation
\[ D_z = \epsilon_0 \epsilon_r E_z. \]

In Fig. 4(a) the calculated \( z \)-component of the electric field \( E_z \) is shown for two different sectional planes and in (b) for two section lines inside the graphene (see sample sketch). The maximum value of \( 18 \text{mV/nm} \) is reached beneath the gate edges and corresponds to a band gap opening of about \( 2 \text{meV} \) [12], which is in agreement with our experimental data.

In conclusion, we have investigated the functionality of nanoscale topgates on bilayer graphene exfoliated on a GaAs substrate. At low temperature the conductance through the gate covered graphene reduces exponentially even without the application of external voltages. We attributed this phenomenon to nearest neighbor hopping underneath the gate covered regions and propose a combination of strain and piezoelectric fields due to mechanical stress imposed by the gates above the graphene as a possible origin. For a certain temperature range allowing sufficient conduction Coulomb blockade dominated transport is observed, consistent with the nanoscale metallization layout. At present the low temperature range of our QD device is limited by the activated NNH transport through localized states underneath the gates. Here in the future a geometry optimized gate design as discussed in the supplement might allow to extend the operational temperature range of such strain defined devices.

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Appendix A: Supplementary Material

In this supplementary material we explore the prospects of strain engineering in a typical top-gate structure by exploiting different thermal coefficients and different device geometries. The application of Ti-Au top-gates as used in the main text for bilayer graphene is very common in conventional semiconductor structures, such as for defining nanostructures in GaAs electron gases. The possibility of stress and induced piezoelectric fields in the latter type has been considered previously, for instance in Ref. [35], where ideally it should be minimized. In the case of strain engineered graphene the opposite regime is desirable.

In Fig. A-1(a) we evaluate the stress tensor $\sigma$ in the vicinity of the gates as used in the main text. It shows the cross-section of a single-gate with dimensions corresponding to our experimental setup and the deformation being graphically enhanced by a factor of 30. The corresponding stress profile of the two tensor components $\sigma_{zz}$ and $\sigma_{xz}$ are encoded in color. The location of the graphene bilayer is shown by the dashed line. For the normal component $\sigma_{zz}$ we find tensile stress ($\sigma_{zz} > 0$, red) near the gate corner, while towards the center there will be compressive stress ($\sigma_{zz} < 0$, blue). In both cases strain induced band structure modifications and band gaps have been predicted [17]. The right part of Fig. A-1(a) shows the amount of shear stress $\sigma_{xz}$ obtained at the position of the bilayer. Note that band gap opening by shear strain has been predicted by Choi et al. [16]. As discussed in the main text strain in piezoelectric substrates can also lead to significant local electric fields. This effect is not further detailed in this supplement.

Our simulation further shows that an increase in gate width $W$ relaxes the stress, as illustrated in Fig. A-1(b). It shows the stress as function of position from the gate center, $X_{COG}$, as its width is varied. To allow comparison, the distance was normalized by the corresponding gate width $W$. Layer thicknesses according to the measured device in the main text have been used in the simulations [see Fig. A-1(a)]. It can be seen that at $W = 350\,\text{nm}$ the stress under the gate has relaxed to less than half of the maximum value at $W = 130\,\text{nm}$ of $\sigma_{zz}^{\text{max}} \approx -80\,\text{MPa}$. The stress of $\sigma_{zz} \approx -75\,\text{MPa}$ in the middle of the gate for $W = 100\,\text{nm}$ as used in our experiment lies close to the maximum (dashed horizontal line). These findings are consistent with the experimental results in the main text, where the wide-gate control device remained conducting at low temperatures.

The above discussion suggests that sandwiching graphene between strained substrate-gate structures provides a complementary tool for defining graphene-nanodevices with tailored transport properties. An appropriate choice of material-sequence, evaporation technique, thickness, geometry etc. should allow tailoring the strain profiles for various applications [18]. The wide opportunities of this technique can be derived from Fig. A-1(d). For example, the stress can be maximized by choosing an optimum gold-layer thickness $t_{\text{Au}}$ for a given gate width of $W = 100\,\text{nm}$, as seen in Fig. A-1(c). A maximal value of $\sigma_{zz} = -83\,\text{MPa}$ is predicted for $t_{\text{Au}} = 27.8\,\text{nm}$. The metal thickness in our experiment was $t_{\text{Au}} = 40\,\text{nm}$, as shown by the horizontal
Figure A-1. Simulation of the deformation and stress $\sigma$ at $T = 300$ mK of a single gate due to different thermal expansion coefficients. Geometrical parameters are provided in the cross-section in (a). The deformation has been scaled up by a factor of 30. The colors encode the stress distributions $\sigma_{zz}$ (left part of the gate) and $\sigma_{xz}$ (right part of the gate), as explained in the main text. The dashed orange line illustrates the location of graphene. (b) plots the stress felt by the graphene layer, $\sigma_{zz}$, as function of distance from the gate center and gate widths. The distance is normalized by the gate width $W$. (c) displays $\sigma_{zz}$ as the distance from the gate center is varied on the horizontal axis, for fixed $W = 100$ nm. On the vertical axis the gold-layer thickness was varied. The dashed lines indicate the actual experimental conditions. In (d) $\sigma_{zz}$ felt by the graphene layer under the center of the gate is plotted as function of gate width $W$ and gold-layer thickness. The white cross indicates the actual experimental condition. Between two contour lines $\sigma_{zz}$ varies by 2 MPa. From the black contour line on the subsequent lines are blanked out because of a too close spacing.

dashed line. The relaxation for increasing $t$, however, saturates at $\sigma_{zz} = -67$ MPa for $t_{Au} > 80$ nm. This is expected as the stress relaxes for regions in large distance from the substrate.

Fig. A-1(d) plots $\sigma_{zz}$ in the center of the gate as function of $t_{Au}$ and $W$. It can be seen that a unique combination of $W = 110$ nm and $t_{Au} = 35$ nm should globally maximize the stress. This example illustrates a possible procedure in finding optimal $t$ and $W$ parameters. The white cross in Fig. A-1(d) indicates the stress value for the experimentally chosen parameters. The procedure may be extended to include arbitrary gate shapes, spacial thickness variations or material combinations in order to engineer a large variety of strain profiles.
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