A small-signal description of black phosphorus transistor technologies for high-frequency applications

Leslie Valdez-Sandoval, Eloy Ramírez-García, Saungeun Park, Deji Akinwande, David Jiménez, Anibal Pacheco-Sanchez

Abstract

This work presents a small-signal high-frequency (HF) equivalent circuit (EC) to model AC performances of black-phosphorous field-effect transistors (BPFETs). The proposed EC is able to describe correctly both the experimental HF intrinsic and extrinsic figures of merit, as well as S-parameters, from different BPFET technologies. Single- and double-stage radio frequency gain amplifiers, are designed at 2.4 GHz using the experimentally-calibrated small-signal BPFET EC. Results show high-gain high-selective BPFET-based amplifiers.

Index Terms

small-signal, BPFET, RF amplifier.

I. INTRODUCTION

During recent years, proof-of-concept low-power HF BPFETs have been demonstrated with both extrinsic cutoff frequency $f_{1,e}$ and extrinsic maximum oscillation frequency $f_{max,e}$ within the range of some tens of GHz [1]-[8]. One of the technology issues to overcome in BPFETs in order to boost their dynamic capabilities is the high contact resistance associated to Schottky-like barriers at the metal contact and 2D channel interface [9]-[11]. Despite their optimistic HF performance projection [14]-[16] as well as their experimentally HF performance proven potential, there is a lack of RF BPFET-based circuits [3]. This can be alleviated by providing reliable device HF models. In the literature, the HF figures-of-merit (FoM) of BPFETs [1]-[8] have not been described so far by any model whereas a unique small-signal proposal has been compared only with numerical device simulation results [14]. In this work, a small-signal equivalent circuit (EC) of BPFETs has been proposed and experimentally validated for the first time across different fabricated technologies and the calibrated models have been used to design RF circuits.

II. SMALL-SIGNAL DESCRIPTION OF BPFETS

A quasi-static (QS) small-signal EC model of BPFETs, without the parasitic contributions of the access pads, is shown in Fig. 1.

The intrinsic elements in this approach, which are located between the nodes $g_i$, $s_i$ and $d_i$, represent all internal phenomena. Drain and source contact resistances, $R_{dc}$ and $R_{sc}$, respectively, have been included in the intrinsic device model since they can not be removed with standard de-embedding techniques: they embrace the contribution of bias-dependent potential barriers at the interfaces of the BP channel and the metallic contacts [9]-[11]. Their contribution can be mathematically removed however, if experimental S-parameters are available [12], [13]. Intrinsic electrostatics couplings are represented by the gate-to-source/gate-to-drain/drain-to-source capacitance $C_{gs/gd/ds}$: $g_{ds}$ is the intrinsic output conductance, $g_m$ the intrinsic transconductance and $V_{gs}$ the intrinsic gate-to-source voltage. The extrinsic model consists of the gate resistance $R_g$ and the parasitic gate-to-source/gate-to-drain/drain-to-source capacitance $C_{gsp/gdp/dsp}$. Pad-related parasitics not included in the model can be removed experimentally by on-wafer de-embedding methods [17]. Gate fingers-related inductance is negligible for emerging transistor technologies.

The model proposed here describes the performance of fabricated RF BPFETs with gate lengths of 250 nm and 500 nm from a technology 1 ($T_1$) [2] and of 300 nm [1] and 400 nm [3] from technologies 2 ($T_2$) and 3 ($T_3$), respectively. Devices layout and fabrication details have been presented elsewhere [1]-[3]. Small-signal parameters have been obtained at the operating bias point at which the pad de-embedded HF FoMs have been measured in [1]-[3]. $R_{dc}$ and $R_{sc}$ have been extracted with a $Y$-function method [16] considering an underlying transport equation without simplifications [18]. $R_g$ values have been calculated...
using the approach presented in [19]. Model parameters for the T1 500 nm-long device [3] have been extracted using a proper detachment of $R_{dc/sc}$ [12, 13] enabled by available experimental S-parameters. For the other devices, S-parameters data are not available and hence, the parameters extraction is as follows. $g_m$ and $g_{ds}$ have been obtained from the experimental curves provided in the corresponding works [1]-[3]. Intrinsic and extrinsic capacitances are obtained by a TCAD-based least-square error-function algorithm [29] towards a correct model description of the experimental HF FoMs reported in [1]-[3]. Model parameters for the studied BPFETs [1]-[3] are listed in Table I. Low values of intrinsic capacitances obtained here are within the same range of the ones obtained for BPFETs have been with another more intricate and experimentally-validated approach [21].

**TABLE I:** Parameter values of the small-signal EC shown in Fig. 1 for BPFET technologies with different gate lengths.

| Parameter | $T_1$ (500 nm) | $T_2$ (400 nm) | $T_3$ (300 nm) |
|-----------|----------------|----------------|----------------|
| $g_m$ (S) | 51.2 (2000)    | 34.4           |                |
| $g_{ds}$ (S) | 1.9 (2)       | 1.1       | 2.8 (0.1)     |
| $C_{gd}$ (fF) | 0.8 (7)       | 0.7 (6)   | 0.7 (6)       |
| $R_{ds}$ (kΩ) | 29.1 (29.3)   | 12.2      | 10            |
| $C_{gd}$ (fF) | 1.8 (5.8)     | 1.1 (3)   | 1.1 (3)       |
| $R_{ds}$ (kΩ) | 20.5 (5.6)    | 10.6     | 2.9           |

**TABLE II:** Intrinsic and extrinsic HF FoMs of BPFETs obtained from experimental data and with the proposed small-signal EC.

| Parameter (GHz) | $T_1$ (500 nm) | $T_2$ (400 nm) | $T_3$ (300 nm) |
|-----------------|----------------|----------------|----------------|
| $f_T$ (GHz)     | 14.92          | 14.92          | 14.92          |
| $f_M$ (GHz)     | 12.12          | 12.12          | 12.12          |
| $r_{y}/|s_{y,y}|$ | 17.24          | 17.24          | 17.24          |
| $r_{y}/|s_{y,y}|$ | 7.41           | 7.41           | 7.41           |

Figs. [2]-[4] present the results obtained from the small-signal EC of Fig. 1 and the experimental data at the range of frequencies reported in [1]-[3] for different BPFET technologies. Subscripts correspond to intrinsic ($i$) and extrinsic ($e$) data. The latter does not include pad-parasitics. The model describes well the HF short-circuit current gain $h_{21}$, the unilateral power gain $U$ as well as the ratio of the maximum available gain (MAG) to the maximum stable gain (MSG), i.e., the power gain, of the fabricated devices [1]-[3]. Table II reports the intrinsic and extrinsic HF FoMs obtained with experimental and simulation data where a maximum relative error of 7.9% has been achieved for the $f_{MAX,i}$ of the T1 250 nm-long device [2]. In contrast to [1] and [3], in this work $f_T$ and $f_{MAX}$ have been reported from the linear extrapolation of the curve at 20 dB/dec towards 0 dB of the corresponding gain curve. Furthermore, Fig. (2) validates the proposed model with experimental S-parameters. Hence, the EC indicated in Fig. 1 is an efficient option for modeling the HF performance of BPFETs at specific bias points and different frequencies. The modeling approach used here enables to evaluate the impact of metal-channel interface effects on the intrinsic devices performance by obtaining $f_{T,i}$ without including $R_{dc/sc}$ in the EC as shown in Figs. (2(a), (2(c), (3(a)) and (4(a)); the larger the $R_{dc/sc}$ the more degraded the intrinsic HF performance is. S-parameters obtained with the EC in Fig. 1 of the studied devices [1]-[3] are shown in Figs. (2(b), (2(d), (3(b) and (4(b).

As shown in Fig. 5, the intrinsic experimental (modeling) response of the open-circuit voltage gain $|z_{21}|$ of the T2 device [1] is 65.8 GHz (63 GHz) and the extrinsic one is 14.2 GHz (13.4 GHz). Hence, these results, along with the previous ones (cf. Figs. 2-4), indicate that the model is efficient in describing BPFETs at HF short- and open-circuit conditions. Synthetic
The small-signal model proposed in this work enables the design of HF circuits, e.g., multipliers, amplifiers, phase-shifters. The schematic of a single-stage maximum gain amplifier based on the T$_1$ 250 nm-long device [2] and designed by using the EC suggested in this work in common-source configuration and with a feedback topology is presented in Fig. 6. The amplifier has been designed to operate at a frequency equal to 2.4 GHz and at the same bias point in which the model has been validated for this device [2] (cf. Section II). QS conditions prevail in the device at this frequency since it is lower than the corresponding $f_{T,i}$ for this technology [2] (see Table II), as predicted elsewhere [22]. In contrast to [6] were a BPFET-based HF amplifier has been designed by coupling its output at 1 MΩ, in this work the device output has been matched to the 50 Ω-standard for RF environments.

The stability conditions [23] for the device ($K > 1$ and $\Delta < 1$ at the frequency range between 2.35 GHz and 2.6 GHz), as shown in the inset of Fig. 7(a), have been obtained using a drain-gate shunt $RC$ feedback network and also with a source series high-Q inductor $L$. The maximum width obtained for the feedback network components is $\sim 5 \mu m$ which enables monolithic integration along with the active device since the reference substrate thickness is much larger ($\sim 125 \mu m$) [2]. The corresponding plots, inset of Fig. 7(a), indicate that the device is stable in the range of frequency between 2.35 GHz and 2.6 GHz. Microstrip lines ($MLIN_1$ and $MLIN_2$) and short circuit stubs ($MLSC_1$ and $MLSC_2$) have been used for the matching networks at the input and output, designed so that $S_{11}$ and $S_{22}$ are lower than $-10$ dB at 2.4 GHz.

Fig. 2: HF FoM for devices from $T_1$ [2]. (a), (c) Top (bottom): extrinsic and intrinsic $|h_{21}|$ ($MAG/MSG$ and $U$) v.s. frequency. (b), (d) $S$-parameters. Data in (a) and (b) correspond to the $T_1$ 250 nm-long device [2]. Data in (c) and (d) correspond to the $T_1$ 500 nm-long device [2]. Markers are experimental data and solid lines correspond to modeling results obtained here.
Fig. 3: HF FoM for a 300 nm-long device in [1]. (a) Top (bottom): extrinsic and intrinsic $|h_{21}|$ ($U$) vs. frequency. Markers are experimental data reported in [1] and solid lines correspond to modeling results obtained here. (b) Synthetic $S$-parameters generated with the experimentally calibrated model.

Fig. 4: HF FoM for a 400 nm-long device in [3]. (a) Top (bottom): extrinsic and intrinsic $|h_{21}|$ ($(MAG/MSG)^{1/2}$) vs. frequency. Markers are experimental data reported in [3] and solid lines correspond to modeling results obtained here. Dashed lines show the linear extrapolation of the curves. (b) Synthetic $S$-parameters generated with the experimentally calibrated model.

Fig. 7 shows maximum available gain ($G_A$) and $S_{21}$ curves versus of single- and two-stage BPFET-based RF amplifiers. The latter has been obtained by connecting two single-stage amplifiers (cf. Fig. 6) in cascade. The correct design of feedback, stability and matching networks enable to improve the poor $S_{21}$ device response (see Fig. 2(b)) to a selective positive response of the single- (double-) stage amplifier at 2.4 GHz with a bandwidth of 12 MHz (14 MHz) and a $S_{21}$ of 6.6 dB (10.8 dB). A similar narrow bandwidth has been achieved for a different BPFET-based RF amplifier designed elsewhere [6]. The closeness between $S_{21}$ and the maximum gain of the single-stage design is $<0.5\%$ at 2.4 GHz and the frequency range in which the double-stage amplifier is above 3 dB is between 2.392 GHz and 2.408 GHz. The results suggest that BPFET-based amplifiers can be used, e.g., in RF front-ends in order to share the frequency spectrum efficiently and to obtain a dynamic access to the spectrum at narrow bandwidths [24]. The gain achieved at 2.4 GHz with the single-stage amplifier design indicates that BPFET-based HF amplifiers can compete with other more studied 2D technologies at similar operation frequencies, e.g., fabricated graphene FET-based single-stage circuits [26], [25] yield only $\sim1.5$ dB more, at 2.4 GHz and 2.5 GHz, respectively, than the results shown here. Inset of Fig. 7(b) shows a study of the impact of the quality factor ($Q$) of the inductors $L_1$ on the amplifiers performance by using values of $Q = 10$, 30, 50, in addition to the ideal $Q$-case previously considered. The gain performance of the single-stage amplifier is very close to the ideal case, obtaining 6 dB in the worst case ($Q = 10$). For the
Fig. 5: Experimental (markers) and simulation (lines) results of the intrinsic and extrinsic open-circuit voltage gain vs. frequency of the (a) $T_2$ device [1] and (b) of the $T_1$ [2] and $T_3$ [3] BPFETs.

Fig. 6: Schematic representation of the single-stage maximum gain amplifier based on BPFET in common-source topology.

Fig. 7: Available Gain for BPFET-based amplifiers: (a) single-stage and (b) double-stage. Inset in (a) shows stability coefficients where the x-axis corresponds to $f$ in GHz. Inset in (b) shows $S_{21}$ as a function of $Q$-factor for $L_1$ (cf. Fig. 5) of the single-stage (empty markers) and double-stage (filled markers) designs at 2.4 GHz.

two-stage amplifier the impact of $Q$ diminishes the gain 1.1 dB with respect to the ideal case.
The small-signal EC presented in this work is an efficient tool for modeling AC performances of black-phosphorous field-effect transistors. This model has described properly the intrinsic and extrinsic HF figures of merit of devices from different technologies over the range of frequencies in which these BPFETs are suitable for HF current and power amplification. Furthermore, this model has predicted with a difference $\leq 5\%$ the reported values of the intrinsic and extrinsic open-circuit voltage gain curves of a fabricated device. The small-signal model proposed here offers the first successful description of the experimental HF performance of BPFET technologies. Single- and two-stage BPFET-based amplifiers designed with an experimentally-calibrated model have gains equal to 6.6 dB and 10.8 dB, respectively, at 2.4 GHz, with narrow bandwidths each of them. Hence, BPFET-based gain amplifiers are good candidates to develop highly selective RF front-end designs.

REFERENCES

[1] W. Zhu, S. Park, M. N. Yogeesh, M. A. Enciso-Aguilar, D. Jiménez, A. Madjar, F. Xia, J. C. M. Hwang, "Black Phosphorus Field-Effect Transistor Technologies", in Proc. IEEE MTT-S International Microwave Symposium (IMS), San Francisco, CA, USA, May 2016. DOI: 10.1109/MWSYM.2016.7540290

[2] J. N. Ramos-Silva, A. Pacheco-Sánchez, M. A. Enciso-Aguilar, D. Jiménez, A. Ramirez-García, "Small-signal parameters extraction and noise analysis of CNFETs", Semiconductor Science and Technology, vol. 35, no. 4, pp. 045024, Mar. 2020. DOI: 10.1088/1361-6660/ab760b

[3] A. Pacheco-Sánchez, J. N. Ramos-Silva, E. Ramirez-Garcia and D. Jimenez, "A Small-Signal GFEF Equivalent Circuit Considering an Explicit Contribution of Contact Resistances," in IEEE Microwave and Wireless Components Letters, vol. 31, no. 1, pp. 29-32, Jan. 2021, doi: 10.1109/LMWC.2020.3036845.

[4] Y. Liu, A. T. Nenadić, M. Si, Y. Du, P. D. Ye, "The Effect of Dielectric Capping on Few-Layer Phosphorene Transistors: Tuning the Schottky Barrier Heights", IEEE Electron Device Letters, vol. 35, no. 7, pp. 795-797, Jul. 2014. DOI: 10.1109/LED.2014.2323951

[5] S. Singh, K. Thakar, N. Kaushik, B. Muralidharan, S. Lodha, "Performance Projections for Two-dimensional Materials in Radio-Frequency Applications", in Proc. IEEE MTT-S International Microwave Symposium (IMS), Boston, MA, USA, Jun. 2019. DOI: 10.1109/MWSYM.2019.8701078

[6] B. Das, S. Mahapatra, "A predictive model for high-frequency operation of two-dimensional transistors from first-principles," Journal of Applied Physics, vol. 121, no. 12, 223101, 2017. DOI: 10.1063/1.5003608

[7] W. Zhu, S. Park, M. N. Yogeesh, S. R. Bank, D. Akinwande, "Black Phosphorus Flexible Thin Film Transistors at Gighertz Frequencies", Nano Letters, vol. 16, no. 4, pp. 2301-2306, Mar. 2016. DOI: 10.1021/acs.nanolett.5b04768

[8] X. Luo, Y. Rahbarhaghigh, J. C. M. Hwang, H. Liu, Y. Du, P. D. Ye, "2.5GHz integrated graphene RF power amplifier on SiC substrate", IEEE Electron Device Letters, vol. 35, no. 12, pp. 1314-1315, Dec. 2014. DOI: 10.1109/LED.2014.2362841

[9] H. Liu, A. T. Nenadić, M. Si, Y. Du, P. D. Ye, "The Effect of Dielectric Capping on Few-Layer Phosphorene Transistors: Tuning the Schottky Barrier Heights", IEEE Electron Device Letters, vol. 35, no. 7, pp. 795-797, Jul. 2014. DOI: 10.1109/LED.2014.2323951

[10] L. Yang, A. Charnas, G. Qiu, Y.-M. Lin, C.-C. Lu, W. Tsai, Q. Paduano, M. Snure, P. D. Ye, "How Important Is the Metal-Semiconductor Contact for Schottky Barrier Transistors: A Case Study on Few-Layer Black Phosphorus?", ACS Omega, vol. 5, no. 8, pp. 4173-4179, Aug. 2017. DOI: 10.1021/acs.omega.7b00634

[11] J. N. Ramos-Silva, A. Pacheco-Sánchez, M. A. Enciso-Aguilar, D. Jiménez, E. Ramírez-García, G. Qiu, Y.-M. Lin, C.-C. Lu, W. Tsai, Q. Paduano, M. Snure, P. D. Ye, "How Important Is the Metal-Semiconductor Contact for Schottky Barrier Transistors: A Case Study on Few-Layer Black Phosphorus?", ACS Omega, vol. 5, no. 8, pp. 4173-4179, Aug. 2017. DOI: 10.1021/acs.omega.7b00634

[12] L. M. Valdez-Sandoval, E. Ramirez-Garcia, D. Jimenez, A. Pacheco-Sanchez, "Contact resistance assessment and high-frequency performance projection of black phosphorus field-effect transistors", Semiconductor Science and Technology, 2020.

[13] L. F. Tiermeer, R. J. Havens, A. B. M. Jansman, Y. Bouitte, "Comparison of the Pad-Open-Short and Open-Short-Load Deembedding Techniques for Accurate On-Wafer RF Characterization of High-Quality Passives", IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 2, pp. 723-729, Feb. 2005. DOI: 10.1109/TMTT.2004.840621

[14] A. Pacheco-Sánchez, D. Jimenez, "Accuracy of Y-function methods for parameters extraction of two-dimensional FETs across different technologies", Electronics Letters, vol. 52, no. 18, pp. 942-945, Sep. 2020. DOI: 10.1049/el.2020.1502

[15] S. Singh, K. Thakar, N. Kaushik, B. Muralidharan, S. Lodha, "Performance Projections for Two-dimensional Materials in Radio-Frequency Applications", IEEE Transactions on Electron Devices, vol. 64, no. 7, pp. 2984-2991, Jul. 2017. DOI: 10.1109/TED.2017.2699969

[16] E. Yarmoghaddam, N. Haratipour, S. J. Koester and S. Rakheja, "A Physics-Based Compact Model for Ultrathin Black Phosphorus FETs—Part II: Model Validation Against Numerical and Experimental Data," IEEE Transactions on Electron Devices, vol. 67, no. 1, pp. 397-405, Jan. 2020. doi: 10.1109/TED.2019.2955651

[17] B. Das, S. Mahapatra, "A predictive model for high-frequency operation of two-dimensional transistors from first-principles," Journal of Applied Physics, vol. 128, no. 2, pp. 234502, 2020. doi: 10.1063/5.0036033

[18] M. A. Beach, L. Laughlin, E. Arabi, S. Wilson, S. Ozan and C. Gamblith, "Enabling RF Technologies for Spectrum Sharing.", 14th European Conference on Antennas and Propagation (EuCAP), Copenhagen, Denmark, 2020. DOI: 10.23919/EuCAP.2020.9135411

[19] T. Hanna, N. Deltimple, M.S. Khenissa, E. Pallecchi, H. Happy, S. Frégone`se, "2.5GHz integrated graphene RF power amplifier on SiC substrate", Solid-State Electronics, vol. 127, pp. 26-31, 2017. DOI: 10.1016/j.sse.2016.10.002

[20] C.H. Yeh, Yi-Wei Lain, Y.C. Chiu, C.H. Liao, M. David, S. H. Hsu, and P.W. Chiu, "Gigahertz Flexible Graphene Transistors for Microwave Integrated Circuits", ACS Nano, vol. 8, pp. 7663-7670, 2014. DOI: 10.1021/nn5036087.