Bridgeless Single-stage Step-down Power Factor Corrector under Synchronous Switching Control Scheme

Chih-Lung Shen* and Li-Zhong Chen

Department of Electronic Engineering, National Kaohsiung University of Science and Technology, Kaohsiung City 82445, Taiwan

(Received December 1, 2019; accepted April 30, 2020)

Keywords: power factor corrector, bridgeless, galvanic isolation, high step-down voltage ratio

In this paper, a novel bridgeless power factor corrector (PFC) is proposed. The PFC can shape the waveform of the input current to be sinusoidal and in phase with the AC input voltage simply by sensing of the AC voltage, input current, and output voltage. That is, it is able to achieve a unity power factor. As compared with conventional PFCs, the proposed PFC possesses the particular features of high step-down voltage ratio, being bridgeless, galvanic isolation, and leakage energy recycling. All the active switches in the proposed PFC can be operated under an identical control signal. In addition, the output voltage can be regulated only by single-loop control, instead of dual- or multiloop control. Therefore, the control scheme for the PFC is simple and much easier to carry out. The operation principle, theoretical analysis, and hardware validation to verify the proposed PFC are described.

1. Introduction

Power-electronics-based devices have been applied in various fields from household appliances to industry equipment, and the total number of relevant products is increasing dramatically. Among them, converters to convert AC power to DC are widely required, especially for a low DC output voltage, such as for battery chargers, LED drivers, and computer power supplies.

AC-to-DC converters conventionally include a bridge rectifier and a huge filter capacitor. Similarly to the power-stage structure shown in Ref. 1, this configuration is simple, cheap, and without the need of an extra control circuit. Nonetheless, it may lead to serious harmonic distortion and results in a low power factor. Adding a current-shaping circuit at the input can not only improve the power factor but also reduce harmonic distortion. Nevertheless, power factor correctors (PFCs) are generally still based on a bridge configuration. The efficiency is therefore rather low. Furthermore, if a PFC is a boost type, the output DC voltage will be higher than the input, even with the obvious advantage of a continuous input current. To deal with a low-voltage load, buck-type PFCs are options, but the input current will be discontinuous and an active switch has to be driven on the high-voltage side. Therefore, a cascaded filter on the AC input side is necessary for achieving a better power factor.

*Corresponding author: e-mail: clshen@nkust.edu.tw
https://doi.org/10.18494/SAM.2020.2781

ISSN 0914-4935 © MYU K.K.
https://myukk.org/
To obtain a continuous input current and lower the output voltage simultaneously, a two-stage PFC has been considered. However, the requirement of more components and the associated lower efficiency are both its main drawbacks. This paper proposed a bridgeless single-stage step-down PFC (BSSPFC) with the feature of galvanic isolation to overcome the aforementioned problems. A high-frequency transformer is incorporated to feature galvanic isolation, the core material of which is Mn–Zn ferrite. All the active switches in the BSSPFC can be controlled simply by synchronous driving, which simplifies the control mechanism. In addition, the BSSPFC is capable of stepping down the input voltage significantly and improving the converter efficiency effectively. The volume of the AC input filter can also be reduced while operating in continuous conduction mode (CCM).

2. Main Structure and Steady-state Analysis

The structure of the proposed BSSPFC is shown in Fig. 1, which is derived from the integration of a single-ended primary-inductor converter (SEPIC) and a flyback converter. The frond-end of the BSSPFC can be regarded as a modified bridgeless SEPIC in charge of performing power factor correction, and the downstream is a flyback-based configuration for achieving a higher step-down voltage ratio and galvanic isolation. The output power of the BSSPFC can be raised when the current of the input inductor in CCM. In CCM, the current stress of active switches can be alleviated and the size of the EMC/EMI filter is also reduced. In this section, the operation principle and voltage gain will be discussed, where the following assumptions are made.

1) All capacitors are large enough to guarantee that the voltages across $C_1$, $C_2$, and $C_o$ can be regarded as constant.
2) Semiconductor devices such as diodes and switches are ideal.
3) The turn ratio $n$ is equal to $N_2/N_1$.
4) The duty ratio of the converter is $D$.
5) The switching period is defined as $T$.

2.1 Operation principle

The operation of the BSSPFC can mainly be divided into three modes over one switching cycle. Figure 2 depicts the conceptual key waveforms, which are the control signal and current
of switch $SW_1$, the current of diode $D_4$, and the current of inductor $L_2$. This figure has been included to aid understanding of the converter operation. The converter operation is discussed mode by mode in the following.

Mode 1 [$t_0$–$t_1$] (Fig. 3): At the beginning of Mode 1, switches $SW_1$ and $SW_2$ are turned on simultaneously and diodes $D_3$ and $D_5$ are in the ON-state. Inductor $L_{in}$ is magnetized by $v_{ac}$ and inductor $L_1$ is charged by capacitor $C_2$. Capacitor $C_1$ transmits its stored energy to inductor $L_2$ through the transformer. Meanwhile, $L_m$ and $L_k$ absorb energy from capacitor $C_1$.

Mode 2 [$t_1$–$t_2$] (Fig. 4): In mode 2, switches $SW_1$ and $SW_2$ are both in the OFF-state and therefore diodes $D_3$, $D_4$, and $D_6$ are forward biased. Inductor $L_{in}$ releases energy to capacitors $C_1$ and $C_2$. At the same time, capacitor $C_2$ also draws energy from $L_m$ and $L_k$. Mode 2 ends when the two currents flowing through inductors $L_m$ and $L_k$ drop to zero.

Mode 3 [$t_2$–$t_3$] (Fig. 5): After $L_m$ and $L_k$ fully discharge their stored energy, the operation mode of the BSSPFC enters Mode 3. During this mode, the circuit condition is the same as that in Mode 2 except for inductors $L_m$ and $L_k$. Mode 3 continues until the active switches are turned on again and then the converter operation over one switching cycle is completed.
2.2 Voltage gain derivation

The following is the voltage gain derivation of the proposed BSSPFC. Voltage polarity and current direction definitions are shown in Fig. 1. Applying the volt-second balance criterion to inductors \( L_{in} \), \( L_1 \), and \( L_2 \) and finding the voltage across the capacitor \( C_1 \) are the key points of this theoretical derivation.

1) Volt-second balance on \( L_{in} \)

When \( SW_1 \) is closed \( (0 \leq t \leq DT) \), the voltage across input inductor \( L_{in} \) is equal to the input source, that is,

\[ v_{L_{in}} = V_{ac}. \]  

(1)

According to Eq. (1), the variation of the inductor current \( \Delta i_{L_{in}} \) during the ON-state interval is

\[ \Delta i_{L_{in}} = v_{ac}DT. \]  

(2)

When \( SW_1 \) is OFF \( (DT \leq t \leq T) \), input inductor \( L_{in} \) will charge capacitors \( C_1 \) and \( C_2 \). Therefore,
From Eq. (3), the variation of the inductor current ($\Delta i_{\text{Lin}}$)\textsubscript{off} over the OFF-time interval can be estimated as

$$\Delta i_{\text{Lin}} = (v_{ac} - v_{C1} - v_{C2})(1 - D)T.$$  \hspace{1cm} (4)

Under a steady-state condition, the current increment and decrease on inductor $L_{\text{in}}$, ($\Delta i_{\text{Lin}}$)$\textsubscript{on}$ and ($\Delta i_{\text{Lin}}$)$\textsubscript{off}$, respectively, will be identical. Therefore,

$$(\Delta i_{\text{Lin}})_{\text{on}} + (\Delta i_{\text{Lin}})_{\text{off}} = v_{ac}DT + (v_{ac} - v_{C1} - v_{C2})(1 - D)T = 0.$$ \hspace{1cm} (5)

Solving Eq. (5) yields

$$v_{ac} = (v_{C1} + v_{C2})(1 - D).$$ \hspace{1cm} (6)

2) Volt-second balance on $L_1$

When $SW_1$ is conducted ($0 \leq t \leq DT$), capacitor $C_2$ will be in parallel with inductor $L_1$. That is,

$$v_{L1} = -v_{C2}.$$ \hspace{1cm} (7)

According to Eq. (7), the current increment on the inductor, ($\Delta i_{L1}$)$\textsubscript{on}$, during this time period is

$$(\Delta i_{L1})_{\text{on}} = -v_{C2}DT.$$ \hspace{1cm} (8)

When switch $SW_1$ is open during the time period $DT \leq t \leq (1 - D)T$, inductor $L_1$ provides energy to $C_1$ and thus,

$$v_{L1} = v_{C1}.$$ \hspace{1cm} (9)

From Eq. (9), the inductor current drop, ($\Delta i_{L1}$)$\textsubscript{off}$, during this time period can be calculated as

$$(\Delta i_{L1})_{\text{off}} = v_{C1}(1 - D)T.$$ \hspace{1cm} (10)

Based on the volt-second balance, the net change of the inductor current has to be zero. Accordingly,

$$(\Delta i_{L1})_{\text{on}} + (\Delta i_{L1})_{\text{off}} = -v_{C2}DT + v_{C1}(1 - D)T = 0.$$ \hspace{1cm} (11)

After solving Eq. (11), the relationship between $v_{C1}$ and $v_{C2}$ can be expressed as
\[ v_{C1} = \frac{D}{1-D} v_{C2}. \]  

(12)

3) Volt-second balance on \( L_2 \)

When \( SW_1 \) is ON, the voltage across inductor \( L_2 \) will be

\[ v_{L2} = n v_{C1} - V_o. \]  

(13)

According to Eq. (13), the variation of the inductor current \((\Delta i_{L2})_{on}\) during this ON-state period can be expressed as

\[ (\Delta i_{L2})_{on} = (n v_{C1} - V_o)DT. \]  

(14)

When the switch is open, inductor \( L_2 \) will provide energy to \( C_o \) and the voltage of \( L_2 \) is equal to \( V_o \).

\[ v_{L2} = V_o \]  

(15)

Thus, the current drop on the inductor current, \((\Delta i_{L2})_{off}\), is computed as

\[ (\Delta i_{L2})_{off} = -V_o (1-D)T. \]  

(16)

In steady-state operation, the magnitudes of \((\Delta i_{L2})_{on}\) and \((\Delta i_{L2})_{off}\) will be identical and the following relationship holds:

\[ (\Delta i_{L2})_{on} + (\Delta i_{L2})_{off} = n(v_{C1} - V_o)DT - V_o (1-D)T = 0. \]  

(17)

Solving Eq. (17), one can obtain

\[ V_o = nDV_{C1}. \]  

(18)

4) Capacitor voltage and converter gain

Substituting Eq. (18) into Eq. (6) gives the voltage across capacitor \( C_1 \):

\[ v_{C1} = v_{ac}. \]  

(19)

Likewise, the voltage across capacitor \( C_2 \) can be obtained by substituting Eq. (12) into Eq. (18). Accordingly,

\[ v_{C2} = \frac{D}{1-D} v_{ac}. \]  

(20)
Capacitor $C_2$ is irrelevant to the voltage gain and only performs energy recycling for leakage inductance and magnetizing inductance. According to Eqs. (18) and (19), the voltage gain of the BSSPFC is determined as

$$V_o = nDv_{ac}. \quad (21)$$

In addition, there are two active switches in the proposed circuit. The voltage stresses of the two switches are identical and are the series voltages across capacitors $C_1$ and $C_2$. That is, $SW_{stress}$ equals $v_{C1} + v_{C2}$.

3. Experimental Results and Discussion

To verify the feasibility of the proposed structure, a 200 W prototype dealing with a universal-line input is built, tested, and measured. Figure 6 shows the waveforms of input voltage $v_{ac}$ and current $i_{Lin}$, when the AC mains is 90 Vrms. As shown in Fig. 6(a), the input current is purely sinusoidal and in phase with the AC mains voltage. Figure 6(b) shows the measured output voltage and current, which indicate that a near ripple-free feature can be achieved at the DC output. Figures 7(a) and 7(b) show the voltages and currents of the input

Fig. 6. (Color online) Measured waveforms when AC mains is 90 Vrms. (a) Input voltage $v_{ac}$ and input current $i_{Lin}$. (b) Output voltage $V_o$ and output current $I_o$.

Fig. 7. (Color online) Measured waveforms when AC mains is 110 Vrms. (a) Input voltage $v_{ac}$ and input current $i_{Lin}$. (b) Output voltage $V_o$ and output current $I_o$. 
and output, respectively, when the AC mains voltage increases to 110 V<sub>rms</sub>. From Fig. 7, a high input power factor and near ripple-free feature are still accomplished. Figures 8 and 9 show the practical measurements performed at inputs of 220 and 264 V<sub>rms</sub>, respectively, both of which reveal that high performance can also be achieved by the proposed BSSPFC. Figure 10 is the transient response when the output power is stepped up from half load to full load. For the case of 220 V<sub>rms</sub> input and 200 W power rating, the measured result for <i>SW</i><sub>1</sub> is shown in Fig. 11.

---

**Fig. 8.** (Color online) Measured waveforms when AC mains is 220 V<sub>rms</sub>. (a) Input voltage <i>v<sub>in</sub></i> and input current <i>i_<sub>Lin</sub></i>. (b) Output voltage <i>V<sub>o</sub></i> and output current <i>I<sub>o</sub></i>.

---

**Fig. 9.** (Color online) Measured waveforms when AC mains is 264 V<sub>rms</sub>. (a) Input voltage <i>v<sub>in</sub></i> and input current <i>i_<sub>Lin</sub></i>. (b) Output voltage <i>V<sub>o</sub></i> and output current <i>I<sub>o</sub></i>.

---

**Fig. 10.** (Color online) Measured output voltage and current at step change under load.

---

**Fig. 11.** (Color online) Measured drain-to-source voltage and current of switch <i>SW</i><sub>1</sub>. 

From the measured waveform, it is found that the active switch is free from spikes. Figure 12 depicts the measured efficiency of the prototype under different input voltages, which reveals that the peak efficiency is up to 91.8% at 264 V_{rms} line voltage. Figure 12 also reveals that when the input voltage is higher, the current in the entire power stage is lower. Accordingly, conduction loss therefore drops and efficiency is raised. In addition, a photo of the prototype BSSPFC is shown in Fig. 13.

4. Conclusions

A high step-down bridgeless PFC is proposed, which possesses the following advantages: fewer rectifying diodes, a single power stage, galvanic isolation, active switches in synchronous control, universal-line input from 90 to 264 V_{rms}, and a simple control mechanism. The BSSPFC can accommodate universal-line input, and moreover, even at a high input voltage, a high power factor and near ripple-free output can still be obtained. Since fewer components are used, the cost can accordingly be lowered and conversion efficiency is improved. To verify the feasibility of the BSSPFC, hardware measurements from a 200 W prototype are carried out. The experimental results demonstrate the characteristics of the BSSPFC, and the average efficiency achieved is up to 90.08%.

References

1. P. S. Heljo, M. Li, K. E. Lilja, H. S. Majumdar, and D. Lupo: IEEE Trans. Electron Devices 60 (2013) 870. https://doi.org/10.1109/TED.2012.2233741
2. H. Wu, S. C. Wong, C. K. Tse, S. Y. R. Hui, and Q. Chen: IEEE Trans. Power Electron. 33 (2018) 6159. https://doi.org/10.1109/TPEL.2017.2739125
3. A. Anand and B. Singh: IEEE Trans. Ind. Electron. 65 (2018) 1117. https://doi.org/10.1109/TIE.2017.2733482
4. A. Marcos-Pastor, E. Vidal-Idiarte, A. Cid-Pastor, and L. Martinez-Salamero: IEEE Trans. Power Electron. 31 (2016) 4641. https://doi.org/10.1109/TPEL.2015.2476698
5. X. Liu, J. Xu, Z. Chen, and N. Wang: IEEE Trans. Ind. Electron. 62 (2015) 943. https://doi.org/10.1109/TIE.2014.234659
6. Z. Shan, X. Chen, J. Jatskevich, and C. K. Tse: IEEE Trans. Power Electron. 34 (2019) 685. https://doi.org/10.1109/TPEL.2018.2812223
7 C. Shen, L. Chen, and Y. Shen: J. Eng. 2019 (2019) 5379. https://doi.org/10.1049/joe.2018.5268
8 H. Choi: IEEE Trans. Power Electron. 28 (2013) 2629. https://doi.org/10.1109/TPEL.2012.2222930
9 S. H. Yang, C. H. Meng, C. C. Chiu, C. W. Chang, K. H. Chen, Y. H. Lin, S. R. Lin, and T. Y. Tsai: IEEE Trans. Ind. Electron. 63 (2016) 5912. https://doi.org/10.1109/TIE.2016.2527630
10 M. He, F. Zhang, J. Xu, P. Yang, and T. Yan: IET Power Electron. 6 (2013) 1544. https://doi.org/10.1049/iet-pel.2012.0097
11 L. Huber, L. Gang, and M. M. Jovanovic: IEEE Trans. Power Electron. 25 (2010) 85. https://doi.org/10.1109/TPEL.2009.2024667
12 L. Xiangrong, X. Dianguo, and Z. Xiangjun: 2006 CES/IEEE 5th Int. Power Electronics and Motion Control Conf. (CES/IEEE, 2006) 1. https://doi.org/10.1109/IPEMC.2006.4777995
13 H. Wu, S. Wong, C. K. Tse, S. Y. R. Hui, and Q. Chen: IEEE Trans. Power Electron. 33 (2018) 6159. https://doi.org/10.1109/TPEL.2017.2739125
14 Y. Lai and Z. Su: IEEE Trans. Ind Electron. 62 (2015) 6944. https://doi.org/10.1109/TIE.2015.2436872
15 K. Y. Lee and Y. S. Lai: IET Power Electron. 2 (2009) 625. https://doi.org/10.1049/iet-pel.2008.0190
16 A. Mallik and A. Khaligh: IEEE Trans. Ind. Electron. 64 (2017) 6371. https://doi.org/10.1109/TIE.2017.2682028
17 L. Gu, W. Liang, M. Praglin, S. Chakraborty, and J. Rivas-Davila: IEEE Trans. Power Electron. 33 (2018) 9399. https://doi.org/10.1109/TPEL.2018.2796582
18 C. Cheng, C. Chang, T. Chung, and F. Yang: IEEE Trans. Power Electron. 30 (2015) 956. https://doi.org/10.1109/TPEL.2014.2312024
19 C. Shen and J. You: Microsyst. Technol. (2018) 1. https://doi.org/10.1007/s00542-018-4172-z
20 A. Mallik and A. Khaligh: IEEE Trans. Veh. Technol. 67 (2018) 935. https://doi.org/10.1109/TVT.2017.2748582

About the Authors

Chih-Lung Shen was born in Tainan, Taiwan, in 1962. He received his B.S. degree from National Taiwan University of Science and Technology, Taipei, Taiwan, in 1988, his M.S. degree from National Tsing-Hua University, Hsinchu, Taiwan, in 1991, and his Ph.D. degree from National Chung Cheng University, Chia-Yi, Taiwan, in 2003, all in electrical engineering. From 1991 to 2008, he was with Nan Jeon University of Science and Technology, Tainan, Taiwan, where he was the chair of the Department of Electrical Engineering and the director of the Energy Technology Research Center. He is currently with the Department of Electronic Engineering, National Kaohsiung University of Science and Technology (NKUST), Kaohsiung, Taiwan, where he is a professor and the director of the Photovoltaics Technology Research Center. From 2013 to 2016, he was the chair of the Department of Electronic Engineering, National Kaohsiung First University of Science and Technology (NKFUST). He has been involved in power electronics education since 1991, has published more than 155 refereed technical papers in journals and conferences, and holds more than 30 patents. His research interests include power converter design, electric ignition systems, active power filters, and photovoltaic-powered systems. He has been inducted to the International Fellow of Chinese Innovation and Invention Society, Taiwan. In addition, he received the Outstanding Professor of Electrical Engineering Award in 2015 from the Chinese Electrical Engineering Association Kaohsiung Section, Taiwan. (clshen@nkust.edu.tw)
Li-Zhong Chen was born in Kaohsiung, Taiwan, in 1994. He received his M.S. degree in electronics engineering from National Kaohsiung University of Science and Technology, Kaohsiung, Taiwan, in 2019. He is currently working toward his Ph.D. degree in engineering science and technology at National Kaohsiung University of Science and Technology. His current research interests include switching power converters, multiport converters, and power factor correction. (0652807@nkust.edu.tw)