Investigation of parasitic bipolar transistor in rail-based electrostatic discharge (ESD) protection circuits

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Abstract In this paper, ESD triggering mechanism of the parasitic PNP bipolar transistor in rail-based ESD protection circuits was investigated. The device simulation results show that the triggering voltage of the parasitic PNP varies with the geometry of the base region (e.g., the spacing between P+ and N-well). Furthermore, the test structures of parasitic PNP devices with different width of collector and base region were fabricated using the 65nm low-k logic/Mixed-Mode CMOS process and characterized with the transmission line pulse (TLP) system. Both simulation and experimental results demonstrated that the triggering voltage of parasitic PNP structures has strong dependence on the base region and the simulation results also show that the triggering voltage is significantly affected by the spacing between P-well and N-well.

Key words: electrostatic discharge (ESD), rail-based ESD protection circuits, parasitic PNP

Classification: Electron Devices, Circuits

1. Introduction

The size of integrated circuits (ICs) has been decreasing due to the development of semiconductor technology. This has made the ICs and electronic devices more sensitive to the electrostatic discharge (ESD) [1, 2, 3]. ESD is a major reliability issue in the semiconductor industry. It is the single largest cause of all IC failures. ESD stress causes large electric fields and high current densities, resulting in breakdown of the oxide of CMOS and thermal damage [4, 5, 6, 7]. ESD protection in high-speed ICs becomes more challenging than others because it requests low parasitic capacitance, low leakage current and almost zero series resistance [8, 9, 10]. To address this, dual-diode based ESD protection circuits, often named “rail-based” ESD protection circuits [11], are widely implemented for radio-frequency (RF), digital and high-speed interface ICs [12-21]. Fig. 1 shows the schematic of the conventional rail-based ESD protection circuits. The circuitry consists of a pair of high-side and low-side diodes that direct the ESD current from input/output (IO) pins to power supply (VDD) and ground (GND). The ESD discharging path between VDD and GND, formed by the primary ESD cell, is shared by two or more IO pins [22, 23, 24]. When multiple IO pins share one primary ESD cell, total chip area consumed by ESD circuits is reduced. The rail-based ESD protection can not only save the layout area for ESD structures on IO pins, but also reduce the leakage current. The DC leakage current and parasitic capacitance on the primary ESD cells (e.g., ground-gate NMOS, active clamps [25, 26], etc) are large due to the big junction area. In rail-based ESD network, both the high-side and low-side diodes are reversed-biased during normal operation. The capacitance of the primary ESD cell is shielded by the high-side diode, which connected in series. Hence the parasitic capacitance and leakage current on the IO pins are mainly determined by the capacitance and area of high-side and low-side diodes. In fact, digital ICs and high-speed interface ICs are very sensitive to the parasitic capacitance and leakage current. The parasitic capacitance from the IO pins needs to be minimized, and the leakage current needs to be controlled to limit the standby power consumptions. Therefore, rail-based ESD protections are widely implemented.

Fig. 1 Rail-based ESD protection circuit with shared primary ESD cell.

In the rail-based ESD protection network, a parasitic PNP structure is inevitably generated between the high-side diode (i.e., P+/N-well diode) and substrate [27]. Fig. 2 shows the cross-section of the high-side diode with the built-in parasitic PNP structure. The emitter of the PNP is formed by the anode of the high-side diode. The base and collector of the parasitic PNP are the N-well and P-substrate respectively.

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Typically, the parasitic PNP is not expected to turn on during normal operation or ESD events. However, the characteristics of the parasitic PNP structure are determined by the layout of the high-side diode, making it uncontrolled and undesired. The non-uniform behaviors of the parasitic structure may cause it to trigger earlier than the primary ESD cell, which may create an un-controlled ESD path and lead to premature ESD failures. It may also cause latch-up problems. However, the parasitic PNP bipolar transistor in the rail-based ESD protection circuit, which is generated between the high-side diode and substrate, may have negative impacts on the ESD protection and normal operation of the digital and high-speed ICs. The leakage current of the parasitic PNP structure also has negative impacts on the ICs during normal operation. In order to improve the reliability of RF, digital and high-speed interface ICs, the parasitic components (i.e., the parasitic PNP bipolar transistor) in the rail-based ESD protection circuits have to be studied. Therefore, these two characteristics (i.e., triggering voltage and leakage current) should be investigated to guarantee the parasitic PNP cannot influence the primary ESD cell and internal circuits.

The triggering voltage of bipolar transistor is mainly decided by the avalanche breakdown voltage between the base and collector region. Eq. (1) defines the avalanche breakdown voltage:

$$V_B = \frac{\varepsilon E_{crit}^2}{2qN}$$

(1)

$E_{crit}$ is the critical value of electric field of the avalanche breakdown, $N$ is the doping concentration in the low-doped region [28]. In fact, the doping of the base and collector region can strongly affect the triggering voltage of the parasitic PNP. The triggering voltage also has strong dependence on the current gain which is determined by the width of the base region. The definition of the current gain can be seen in Eq. (2).

$$\beta = \frac{D_w W_a N_{hi} B}{D_w W_a N_{arti} e^2}$$

(2)

$W_E$ and $W_B$ are the width of emitter and base region respectively [28]. However, the width of emitter region cannot considerably affect the current gain due to the emitter current crowding effect which narrows the effective width of the emitter region. Furthermore, the current gain is influenced by the width of collector region under high current injection due to Kirk effect [29], which leads to a widening of effective base region. A wide collector region enhances the Kirk effect lowering the current gain.

Based on these fundamentals, we may adjust key parameters of the parasitic PNP bipolar transistor to investigate its ESD characteristics (i.e., triggering voltage) and leakage current.

2. Device simulation

Technology Computer Aided Design (TCAD) is a common method to simulate and estimate the behaviors and characteristics of semiconductor processes and devices. TCAD simulator includes 2D and 3D simulation. 2D simulator models the electrical, thermal and optical characteristics of a wide variety of devices. Therefore, 2D simulation is commonly used in TCAD simulation to analyze the ESD characteristics of semiconductor devices [30, 31, 32]. In this paper 2D Silvaco TCAD is utilized to analyze the ESD behavior of the parasitic PNP bipolar transistor.

2.1 Simulation environmental setup

The cross-section of the parasitic PNP in rail-based ESD protection circuits, which is built by the Silvaco TCAD, can be seen in Fig. 3. The highly doped P+ region, which doping concentration is 4.74e19cm$^{-3}$ becomes the emitter region of the parasitic PNP, and the P-well, which doping concentration is 3.5e17cm$^{-3}$, forms the collector region of the PNP. Furthermore, the doping of the N-well and P-sub are 3e17cm$^{-3}$ and 1.34e15cm$^{-3}$. The triggering voltage ($V(t)$) and leakage current of the parasitic PNP bipolar transistor are determined by the current gain that may be affected by changing the width of the collector region, base region, emitter region and distance between P-well and N-well. Therefore, four parameters, $D_1$, $D_2$, $D_3$ and $L$, which respectively correspond to these four regions, are focused in this investigation of the parasitic PNP.

The human body model (HBM), which is the traditional ESD testing standard [7], is used in the TCAD simulation. The ESD current pulse has 10ns rise time and 150ns exponential decay time, which corresponds to the HBM current waveform that is generated by 100pF capacitor through a 1.5K$\Omega$ resistor. This current pulse is applied to the emitter of the PNP with the base floating.
2.2 TCAD simulation of the parasitic PNP structure

Fig. 4(a) shows the simulated transient I-V curves of PNP structure with different D1 distance from 0.5 µm to 5 µm when D2 and L are same. Varying D1 distance does not affect the triggering voltage (V_{t1}) but change on-resistance (R_{on}) after triggering. V_{t1} is not changed with D1 since the current gain can only be affected by the width of the collector during high level injection [33]. Fig. 4(b) shows the simulation results of varying D2 distance while keeping the same D1 (i.e., =2 µm) and L (i.e., =0 µm). The V_{t1} shows strong dependence on D2. When D2 is decreased from 3 µm to 0.5 µm, V_{t1} decreases from 13.19 V to 7.3 V. The decrease in D2 results in narrowing of the base width of the parasitic PNP, which lowers the current gain and increases the V_{t1}. The results of changing D3 with D1=D2=2 µm and L=0 µm are shown in Fig. 4(c). As expected, the variation of the emitter region (i.e., D3) is not making a considerable change in the V_{t1} due to the emitter current crowding effect. As shown in Fig. 4(d), the smaller L also leads to decrease in the V_{t1}. Reducing L, which is the space between N-well and P-well, elevates the effective doping of the P-sub and N-well junction because the concentration of the P-well is much higher than the P-sub. This increase in the doping of the PN junction dramatically decreases the avalanche breakdown voltage, which strongly influences the V_{t1}. Therefore, the V_{t1} decreases with the reduction of L. Tab. I summarizes the Vt1 dependence on different geometry parameters of the parasitic PNP bipolar transistor-existing in the high-side diode for rail-based ESD protection circuits.

![Simulation Results of Parasitic PNP](image)

Fig. 4 The simulation results of parasitic PNP with different parameters of (a) D1 (P+ to P-well distance), (b) D2 (P+ to N-well distance), (c) D3 (high-side diode anode P+ width) and (d) L (P-well to N-well distance).

![Current Density Distribution](image)

Fig. 5 Current density contribution of the parasitic PNP of (a) D2=0.15 µm and (b) D2=2.0 µm with 8V bias in emitter.

### Table I. Simulation results on the triggering voltage of the parasitic PNP

| D1 (µm) | 0.5  | 1.0  | 1.5  | 2.0  | 3.0  | 5.0  |
|--------|------|------|------|------|------|------|
| V_{t1} (V) | 12.55 | 13.05 | 13.15 | 13.15 | 13.25 | 12.8 |
| D2 (µm) | 0.15 | 0.5  | 0.8  | 1.0  | 1.5  | 3.0  |
| V_{t1} (V) | 7.3  | 10.95 | 12.37 | 12.91 | 12.97 | 13.19 |
| D3 (µm) | 0.5  | 1.0  | 1.5  | 2.0  | 2.5  | 3.0  |
| V_{t1} (V) | 12.98 | 13.05 | 13.01 | 13.03 | 12.87 | 13.31 |
| L (µm)  | 0.2  | 0.3  | 0.5  | 0.8  | 1.0  | 1.0  |
| V_{t1} (V) | 13.15 | 14.2 | 17.3 | 21.6 | 30.2 | 39.2 |

Fig. 5 describes the current density distribution of parasitic PNP with D2=0.15 µm (Fig. 5a) and D2=2.0 µm (Fig. 5b). For both structures, the anode of high-side diode is biased at 8V. As shown in Fig. 5(a), the P-well and N-well is reverse-biased. The avalanche breakdown occurs at this current density level (i.e., 4.5×10^4 A/µm^2), generating the electron-hole pairs and turning on the parasitic PNP structure. From the TCAD simulation, the transient current, which flows from the anode of high-side diode to the substrate contacts, is mainly on the surface of the device. When D2 is changed from 0.15 µm to 2.0 µm, the current density (i.e., 9.05×10^4 A/µm^2) is too low to start avalanche breakdown (Fig. 5b).

3. Experimental Results

Fig. 6 shows the layout of the high-side diodes with parasitic PNP which were fabricated in UMC 65nm low-K logic/Mixed-Mode CMOS process with standard performance. Fig. 6(a) depicts the top view of a parasitic PNP structure (i.e., high-side diode and P-substrate contact).
The devices with different D1 can be seen in Module 1 (Fig. 6b), and the devices with different D2 are in Module 2 (Fig. 6c). The width of all these devices are 50 µm. The devices in both modules were tested to evaluate their triggering and leakage current characteristics.

3.1 TLP I-V Characteristics
The devices with different parameters were investigated by using the transmission line pulse (TLP) system (Model ES62X TLP from ESDEMC) with 10ns rise time and 100ns pulse width. The TLP measurement results of these devices can be seen in Fig. 7. As shown in Fig. 7(a), D1 has very limited impact on the \( V_{t1} \). The injected current at triggering point is not high enough to affect the current gain of parasitic device. Therefore, the \( V_{t1} \) of these devices are kept around 11 V even though D1 is changing from 5 µm to 0.5 µm. This aligns well with the device simulation result (Fig. 4a). In fact, the \( V_{t1} \) has strong dependence on the D2 as shown in Fig. 7(b). The smaller D2 (i.e., width of the base region of parasitic PNP) increases the current gain and effectively reduces the \( V_{t1} \). When D2 is changed from 0.5 µm to 0.15 µm, the \( V_{t1} \) decreases from 12 V to 8V. Low \( V_{t1} \) may cause the un-controlled ESD discharge path through parasitic PNP structure and result in early ESD failure risk due to possible low failure current of parasitic ESD path. It can also lead to strong substrate injection during system-level ESD event.

![Fig. 6 The Layout of the high-side diodes with parasitic PNP (a) top view of a single device, (b) Module 1 (different D1) and (c) Module 2 (different D2).](image)

3.2 Leakage Current Characteristics
Since the parasitic PNP bipolar transistor always exists within the high-side diode, the leakage current of parasitic PNP need to be evaluated to prevent it from impacting the normal operation of the internal circuitry. The DC voltage for the leakage measurement was conducted by using the source measure unit of Keithly. As shown in Fig. 8, the leakage currents of these devices are below 10pA. The DC breakdown voltage (BV) has less dependence on width of the collector region (i.e., D1). However, as shown in Fig. 8(b), the BV decreases with the reduction of D2. The leakage current increases when the base width of the parasitic PNP is reduced. The increase of the leakage current may affect the bandwidth of high-speed IO pins, it also increase the standby power consumption of ICs.

![Fig. 8 The DC leakage current of parasitic PNP with different parameters of (a) D1 and (b) D2.](image)

4. Conclusion
The parasitic PNP bipolar transistor in rail-based ESD protection circuits was investigated to prevent it from affecting the triggering of primary ESD cell and the normal operation of ICs. The triggering voltage and leakage current of the parasitic PNP can be changed by varying the base region and space between N-well and P-well, which is supported by the device TCAD simulation. A test chip designed with 65nm process has been characterized using the TLP and DC measurements. The results demonstrated that the triggering voltage and leakage current of the parasitic PNP are affected by distance from anode of high-side diode to the N-well. The layout of the high-side diode need to be carefully designed to prevent the early turn-on or excessive leakage current from parasitic PNP structures and guarantee the reliability of the rail-based ESD protection circuits.

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