Design of High-Performance 1-Bit Full Adder Cells Based on MOS-Type GNRFETs

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Abstract: In deep sub-micron technologies, conventional silicon-based transistors are faced main several problems related to the short-channel effects such as power dissipation, subthreshold leakage, and drain-induced barrier lowering (DIBL). Graphene nano-ribbon field-effect transistors (GNRFETs) have become a potential contender as a substitute for traditional silicon-based transistors in next generation nano-electronic devices. They exhibit fantastic properties such as high charge carrier mobility, mean free path of electrons, faster switching, and high $I_{ON}/I_{OFF}$ ratio. In order to prove the competences and superiority of these types of transistors, various circuits like full adder (FA) cells, which are the main building block of computational systems must be simulated and studied. This paper presents redesigning various 1-bit FA cells such as Complementary Metal-Oxide-Semiconductor (CMOS), Complementary Pass-Transistor Logic (CPL), Transmission-Gate (TG), Hybrid CMOS (HCMOS), and Transmission Function Adder (TFA) using MOS-GNRFET devices in 16nm technology node. Different HSPICE simulations are performed to obtain propagation delay, average power consumption, power-delay-product (PDP), and energy-delay-product (EDP) of FA cells and are compared with 16nm CMOS predictive technology model (PTM) at different supply voltages. The obtained results indicate that MOS-GNRFET based 1-bit FA cells have better performance than that of Si-CMOS one. The MOS-GNRFET based FA cells improve propagation delay and EDP at least 31.195% and 4.372%, respectively.

Keywords: Full Adder, Graphene Nanoribbon Field-Effect Transistor (GNRFET), High-Performance, Metal-Oxide-Semiconductor (MOS)

1. Introduction

Carbon-based nanomaterials are potential materials for next generations of semiconductor technology due to their extraordinary properties such as high charge carrier mobility and long mean free path of electrons [1]. Carbon nanotubes (CNTs) and graphene are two of the most studied allotropes of carbon [2], which exhibit the same properties [3]. However, graphene has received much attention because of its planar structure, so it does not need major technological shift [4]. Graphene is a single atomic layer of carbon film with two-dimensional honeycomb lattice, has no intrinsic bandgap and hence cannot be completely turned ON or OFF [5]. With tailoring the graphene to one-dimensional (1-D) graphene nanoribbons (GNRs) form with width less than 10 nm, a bandgap opens up and can be used as channel material [6]. GNR field effect transistors (FETs) (GNRFETs) are potential substitution for silicon-based transistors due to faster switching, reduced short channel effects, lower energy-delay product (EDP), and high $I_{ON}/I_{OFF}$ ratio [5, 7].

Full Adders (FAs) are main core of arithmetic operations in digital systems such as arithmetic and logic unit (ALU), microprocessors, and application-specific digital signal processing (DSP) architectures [8, 9]. In this paper, five various 1-bit FA cells based on MOS-GNRFET and Si-CMOS transistors are designed and simulated in the different supply voltages. These include Complementary Metal-Oxide-Semiconductor (CMOS), Complementary Pass-Transistor Logic (CPL), Transmission-Gate (TG), Hybrid CMOS (HCMOS), and Transmission Function Adder (TFA). The rest of the paper is organized as follows. Graphene and GNRFETs are described in section II. Five various 1-bit FA cells used in this paper are defined in section III. In section IV, the simulation results and the discussions are presented.
2. Review of Graphene and GNRFETs

Graphene is a zero-gap semi-metal in nature and transistors fabricated by that have a low \( I_{ON}/I_{OFF} \) ratio, and hence is not suitable for digital applications [5]. With converting the graphene into narrow strips, which are called GNRS with width < 10 nm, a bandgap opens up and can be used as a channel material in FETs [10]. Based on the edge geometry, there are two types of GNRS: 1) Zigzag-GNR (ZGNR) and 2) Armchair-GNR (AGNR). The ZGNR always acts as a metal, while the AGNR can have both metal and semiconductor properties [6]. The energy gap of graphene is in inverse proportion to its width [11]. On the other hand, the number of dimer lines \((N)\) determines the GNRS width \((W_{CH})\), which is in direct ratio to it. The following equations exhibit the dependency of \(W_{CH}\) and gate width \((W_{GATE})\) on \(N\) [5].

\[
W_{CH} = \sqrt{3}d_{cc} \frac{(N+1)}{2} \tag{1}
\]

\[
W_{GATE} = (W_{CH} + 2W_{sp}) \times n_{ribb} \tag{2}
\]

in which \(d_{cc} = 0.142\) \text{nm} is the carbon-carbon bond distance, \(2W_{sp}\) is the distance between two adjacent GNRS within the same device, and \(n_{ribb}\) is the number of ribbons. According to the three-periodic trend of \(N\), for \(N = 3p\), \(N = 3p + 1\), and \(N = 3p + 2\) \((p \in N)\), the bandgap is moderate, large, and small, respectively [12].

Based on the FET design, GNRFETs are of two types: 1) Schottky barrier (SB)-GNRFET (SB-GNRFET) and 2) MOS-GNRFET. SB-GNRFETs have a GNRS-based channel and metal-based contacts, which SBS occur at the graphene-metal junctions. On the other hand, MOS-GNRFETs consist of a GNRS-based channel and heavily doped source and drain reservoirs [13]. These doped reservoirs lead to a higher \(I_{ON}/I_{OFF}\) ratio and hence perform better than SB-GNRFETs. Other major advantages of MOS-GNRFET over the SB-GNRFETs are faster switching, resulting in smaller delay, and higher trans-conductance [14], hence we used the MOS-GNRFET to design the 1-bit FA cells. The structure of MOS-GNRFET is shown in Figure 1. The use of multiple parallel GNRS in the device leads to its drive strength increases. The used GNRS are armchair-type due to its semi-conducting property [6].

![Figure 1. Structure of MOS-type GNRFET.](image)

3. The 1-Bit Full Adder Cells

The 1-bit FA cells are the main component of computational circuits and extensively used in digital electronic systems like microprocessors. The limitations of FA cells design include small area, high-speed, lower power consumption, and high-throughput [15]. The 1-bit FA cells get three 1-bit inputs \(A, B, C_{in}\) and give two 1-bit outputs \(\text{Sum}\) and \(C_{out}\) which relate together as follows:

\[
\text{Sum} = (A \oplus B) \oplus C_{in} \tag{3}
\]

\[
C_{out} = A \cdot B + C_{in} \cdot (A \oplus B) \tag{4}
\]

Five different 1-bit FA cells are selected in this paper, which are described in the following [8, 9]:

1) The CMOS FA cell utilizes 28 transistors to implement the equations (3) and (4). It is designed based on mirror structure (pull-up and pull-down transistors).

2) The TG FA cell has 20 transistors and is based on transmission gates.

3) The CPL FA cell has 32 transistors and uses the CPL logic family.

4) The HCMOS FA cell consists of 20 transistors and uses the transmission-gates, pass-transistors, pull down and pull up transistors to implement the equations (3) and (4).

5) The TFA FA cell is based on the transmission function theory and has 16 transistors.

4. The Simulation Results and Discussion

In order to simulation of MOS-GNRFET based 1-bit FA cells in HSPICE software, we used the SPICE-compatible model of GNRFET, which is developed in [5]. Table 1 indicates the various MOS-GNRFET parameters. Five different 1-bit FA cells selected in the previous section are analyzed at a frequency of 125 MHz, and with ±10% variations at the nominal supply voltage of 0.5 V. The simulations are performed by adding buffers in the input and output sides, load capacitance of 15 \(\text{fF}\), at a temperature of 27 °C. The Si-CMOS based transistor sizing has been taken from [8, 9], and based on this sizing the number of GNRS \(n_{ribb}\) in MOS-GNRFET has been selected to be equal to Si-CMOS in terms of area.

| MOS-GNRFET parameter | Value |
|-----------------------|-------|
| Channel length \((L_{ch})\) | 16 nm |
| Number of dimer lines \((N)\) | 12 |
| Space between two adjacent GNRS \((2 \times W_{sp})\) | 2 nm |
| Number of GNRS \((n_{ribb})\) | 6 |
| Oxide thickness \((T_{ox})\) | 0.95 nm |
| Line-edge roughness percentage \((p_r)\) | 0 |
| Doping fraction | 0.001 |
| Supply voltage | 0.5 V |

In Table 1 \(n_{ribb}\) is the number of graphene nanoribbons and \(p_r\) is the probability of losing an atom on the edge of a GNRS due to incomplete fabrication, which is called line-edge.
roughness probability [5].

Table 2 shows the values of worst-case delay and average power consumption of both MOS-GNRFET and Si-CMOS based on all five types of 1-bit FA cells in the different supply voltages. We applied all possible states of the inputs to the cells and then measured the delays as the time duration from 50% of inputs to 50% of outputs. Finally, their worst is reported. From this table, the MOS-GNRFET based 1-bit FA cells (denoted by G-(FA cell name)) show an impressive reduction in the worst-case delay compared to Si-CMOS one and provide FA cells with high-speed performance. The average power consumption of the MOS-GNRFET based TFA and CMOS FA cells is very useful for energy-efficiency applications. In addition, all MOS-GNRFET based FA cells have lower PDP than that of Si-CMOS ones, except HCMOS FA cell at supply voltages of 0.45 V and 0.5 V.

Table 3 exhibits the values of PDP and EDP for all five types of 1-bit FA cells using MOS-GNRFET and Si-CMOS transistors in three supply voltage values. The results indicate MOS-GNRFET based FA cells have lower EDP than Si-CMOS one, which is very useful for energy-efficiency applications. In addition, all MOS-GNRFET based FA cells have lower PDP than that of Si-CMOS ones, except HCMOS FA cell at supply voltages of 0.5 V and 0.55 V.

Figure 2 shows the bar graph for the worst-case delay, average power, PDP, and EDP of both MOS-GNRFET and Si-CMOS based 1-bit FA cells in the different supply voltages. It is observed from these figures that designing 1-bit FA cells using MOS-GNRFETs is much better than Si-CMOS. Therefore, MOS-GNRFETs can be a potential replacement for Si-CMOS based transistors in the future scaled technologies.

5. Conclusion

This paper presents the designing five various 1-bit FA cells such as CMOS, CPL, TG, HCMOS, and TFA using MOS-GNRFET and Si-CMOS transistors. These FA cells are simulated in HSPICE software by ±10% changing at the nominal supply voltage of 0.5 V to obtain values of their main performance metrics such as worst-case delay, average power, PDP, and EDP. The results show that all five types of MOS-GNRFET designs have lower worst-case delay and EDP, which provide the devices with high-speed and energy-efficiency performances. The designing CMOS and TFA FA cells using MOS-GNRFETs have lower average power consumption in all three supply voltage values compared to Si-CMOS ones. All types of MOS-GNRFET based FA cells except HCMOS FA cell have lower PDP than that of Si-CMOS based FA cells.

| FA cell | Worst-case delay (ps) | Average Power (µW) |
|---------|-----------------------|---------------------|
|         | 0.45 V | 0.5 V | 0.55 V | 0.45 V | 0.5 V | 0.55 V |
| CMOS    | 511.083 | 308.453 | 216.029 | 0.047 | 0.061 | 0.076 |
| G-CMOS  | 71.071  | 53.990  | 44.821  | 0.028 | 0.037 | 0.050 |
| Improvement (%) | -86.094 | -82.497 | -79.252 | -40.426 | -39.344 | -34.211 |
| TG      | 433.101 | 268.919 | 191.933 | 0.026 | 0.036 | 0.052 |
| G-TG    | 65.695  | 50.485  | 40.502  | 0.026 | 0.076 | 0.221 |
| Improvement (%) | -84.901 | -81.227 | -78.898 | 0.000 | 111.111 | 325.000 |
| CPL     | 684.747 | 404.466 | 274.273 | 0.214 | 0.283 | 0.377 |
| G-CPL   | 73.510  | 56.785  | 45.517  | 0.129 | 0.233 | 0.494 |
| Improvement (%) | -89.265 | -85.961 | -83.404 | -39.720 | -17.668 | 31.030 |
| HCMOS   | 507.796 | 309.258 | 217.543 | 0.066 | 0.088 | 0.120 |
| G-HCMOS | 349.390 | 155.585 | 100.838 | 0.066 | 0.181 | 0.534 |
| Improvement (%) | -31.195 | -49.691 | -53.647 | 0.000 | 105.682 | 345.000 |
| TFA     | 425.100 | 262.907 | 188.422 | 0.018 | 0.026 | 0.038 |
| G-TFA   | 65.328  | 51.517  | 40.369  | 0.010 | 0.013 | 0.019 |
| Improvement (%) | -84.632 | -80.405 | -78.575 | -44.444 | -50.000 | -50.000 |

| FA cell | PDP (×10^10 W, s) | EDP (×10^-7 J, s) |
|---------|------------------|-------------------|
|         | 0.45 V | 0.5 V | 0.55 V | 0.45 V | 0.5 V | 0.55 V |
| CMOS    | 24.109 | 18.670 | 16.318 | 12.322 | 5.759 | 3.525 |
| G-CMOS  | 1.967  | 2.008  | 2.221  | 0.140  | 0.108 | 0.100 |
| Improvement (%) | -91.841 | -89.245 | -86.389 | -98.864 | -98.125 | -97.163 |
| TG      | 11.337 | 9.813  | 10.037 | 4.933  | 2.639 | 1.926 |
| G-TG    | 1.717  | 3.820  | 8.943  | 0.113  | 0.193 | 0.362 |
| Improvement (%) | -84.855 | -61.072 | -10.900 | -97.709 | -92.678 | -81.205 |
| CPL     | 146.489 | 114.449 | 103.396 | 100.308 | 46.291 | 28.359 |
| G-CPL   | 9.516  | 13.221 | 22.475 | 0.700  | 0.751 | 1.023 |
| Improvement (%) | -93.504 | -88.448 | -78.263 | -99.302 | -98.378 | -96.393 |
| HCMOS   | 33.315 | 27.313 | 26.076 | 16.917 | 8.447 | 5.673 |
| G-HCMOS | 22.998 | 28.1253 | 53.804 | 8.035 | 4.380 | 5.425 |
| Improvement (%) | -30.968 | 2.974 | 106.335 | -52.504 | -48.147 | -4.372 |
| TFA     | 7.550  | 6.729  | 7.125  | 3.210  | 1.769 | 1.343 |
| G-TFA   | 0.636  | 0.683  | 0.774  | 0.042  | 0.035 | 0.031 |
| Improvement (%) | -91.576 | -89.85 | -89.137 | -98.692 | -98.021 | -97.692 |
Figure 2. The bar graphs of (a) Worst-case delay, (b) Average power, (c) PDP, and (d) EDP of both MOS-GNRFET and Si-CMOS-based 1-bit FA cells in the different supply voltages.

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