Practicality of Boost-type DC-DC Converter for Single Solar Cell

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Solar cell systems have gained increasing attention with gradual improvements in their cost and conversion efficiency. Paint-type solar cells have been proposed. Such solar cells have several advantages, including a follow-up curved surface, free shape, and a seamless aesthetically pleasing design. In general, a solar cell is fabricated based on a series of possible configurations, and the output voltage of the solar module setup can be up to several tens of volts. In applications that involve exploiting a free shape, such devices may not provide a sufficient current. Moreover, this current may then be interrupted as a result of the small cell size or partial light blockage owing to the series construction. To address these problems, DC-DC converters based on the performance of aesthetically designed solar cells have been investigated. These components can be boosted to an easy-to-use voltage for practical daily applications. In this paper, the possibility of achieving their practical use based on a prototype is discussed based on experimental data.

Keywords: Single Solar Cell, Boost type DC-DC Converter, Start in low voltage, High boost-up voltage ratio

1. Introduction

Solar power generation systems are in widespread use globally (Fig. 1). In recent years, various types of solar cells, such as thin film solar cells, have been put into practical use along with crystalline Si-based solar systems. The efficiency of perovskite based solar cells has recently improved to over 25% [2], which has attracted the attention of researchers. Painted-type solar cells are unique with features that include a curved surface conformability, free shape, and high design without seams (Fig. 2, 3(b)). This type of solar cell can be built on clothes and is thus expected to be applied to charging systems for gadgets such as smartphones. In general, when using a solar cell, a series structure is formed into a module with an output voltage of tens of volts for ease of use (Fig. 3(a)). When curved surface compliance and a free-shape are required, there is a possibility that the generating power may be limited by the current of the shadow cell or the cell with the smallest area, when connected in series. As such, a painted solar cell may not be able to exhibit an acceptable performance (Fig. 3(a)). To address this problem, the authors have proposed a DC-DC converter that can boost the low voltage of a single-cell solar cell to a voltage that is easy to use and can maximize the performance of an aesthetically designed solar cell [3] (Fig. 3(b)).

The circuit that drives a single solar cell presents several challenges. One such challenge is starting the circuit from a voltage of as low as 0.5 V with a single solar cell. Conventionally, a method for starting using a low-threshold transistor through a) Stationary PV System (a) S Series-structured PV to achieve high-voltage. The part not in shadow also has decreased output. Residence use (SHARP) EV Charger (Nichicon) Watch (Casio) Vehicle (Toyota)

(b) Mobile PV System Charging Smart phone (InfinityPV)

Fig. 1 Example Applications of PV System

Charging a smartphone with a PV incorporated in a suit

Fig. 2 Schematic of painted PV application

It is able to make any shape PVs Output decreases only for shaded area

Fig. 3 Merit of single Solar Cell

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silicon on insulator (SOI) process has been proposed \cite{4}. This method can be started from 0.3 V but requires a special semiconductor process. Although a method for constructing a level shifter in the large scale integration (LSI) and starting from weak radio waves, \cite{5}, and a method for constructing a charge pump on an ultrathin process \cite{6}, have been developed, these methods are unable to provide sufficient voltage and current to the control circuit of the power converter. Another challenge is to provide the required voltage and power to the wearable device. A power supply of approximately 10 W (e.g., 5 V/2 A to 12 V/0.8 A) is desirable for charging mobile devices such as smartphones (USB charges at approximately 5 V/2 A). However, the booster circuit from a low voltage of less than 1 V is mainly used for sensors and low-power wireless communication \cite{7}, and the output power is on the order of micro watts. By contrast, battery charging converters have been proposed, although those that use commercial power as an input \cite{8,9} or even solar cells as a power source have a relatively high input voltage of 3–12 V \cite{10,11}. One example of a single solar cell battery charging system was proposed \cite{12}. Although this proposal is the closest in concept to the present study, its output wattage is less than 100 mW. To the best of our knowledge, there is no example of boosting an input from ~0.5 V to an output ~12 V rotating ~10 W of power. To address these challenges, the authors proposed the use of a low-voltage start up circuit and boost DC-DC converter. The low-voltage start up circuit using the RCC method, which consists of general and easily available parts, can be started with a low voltage of a single solar cell, and can output the power required for the control power supply of the DC-DC converter. The DC-DC converter boosts the voltage generated by a single solar cell from 0.5 V to 12 V and powers up to ~10 W.

In this paper, the practicality required for a DC-DC converter for a single solar cell is considered as the following and used as an evaluation standard.

First, regarding the low-voltage startup circuit:
- Sufficient power can be obtained for the initial operation of the control circuit.
- It can be started within a wide temperature range.
- Next, regarding the main circuit:
  - Sufficient voltage and power can be obtained for the operation of portable devices.
  - It is possible to operate from a low output voltage of 0 V up to 12 V, assuming charging applications such as batteries or capacitors.
  - Maximum power point tracking (MPPT) operation of solar cells is possible.

These practicalities of the DC-DC converter will be shown using experimental data.

The structure of this paper is as follows. Chapter 2 describes the entire circuit configuration, low-voltage startup circuit configuration, its operation, the main circuit configuration, and its operation. In Chapter 3, it will be considered a high output and high efficiency. Chapter 4 shows the experimental results. Chapter 5 discusses the total practicality of the proposed DC-DC converter.

2. Circuit configuration and its operation

2.1 Circuit configuration A block diagram of the boost type DC-DC converter system for a single solar cell is represented in Fig. 4. It consists of a low-voltage start up circuit, a control circuit, a control power supply, and a DC-DC converter. A general overview of the flow of operation is provided in Fig. 5. During operation, the low-voltage startup circuit is activated by

![Fig. 4 Block diagram of a single solar cell system](image-url)

![Fig. 5 Operation procedure of the single solar cell system](image-url)
the open voltage of the single solar cell and supplies power to the control circuit. The control circuit turns the semiconductor switch of the main circuit ON/OFF, and the main circuit boosts the voltage of the single solar cell to several tens of volts. The boosted output voltage is used as the control power supply, and when the operation is stabilized, the low-voltage starting power supply circuit is disconnected, and the operation shifts to the MPPT control. In the next section, the low-voltage start-up circuit and the DC-DC converter circuit will be described.

2.2 The low-voltage start-up circuit In the case of boosting the voltage from 0.5 to 0.7 V for a single cell solar cell, establishing a voltage to drive the switching device is a challenge. To address this problem, one possibility is to use a charge pump IC with a threshold voltage of 0.3 V using a SOI process. By contrast, in this report, a self-excited flyback, ringing choke converter (RCC) power supply circuit that can be initiated with a general transistor will be investigated.

The circuit diagram is shown in Fig. 6 and its operation mode is shown in Fig. 7. The current from the solar cell charges the capacitor \( C_P \) through the resistor \( R_S \). As the capacitor \( C_P \) is charged, the base potential \( V_B \) of the transistor \( Tr \) approaches the threshold voltage \( V_{TH} \), and the collector-emitter resistance \( R_{CE} \) gradually decreases. The voltage \( V_{LS} \) across the transformer primary winding \( L_3 \) approaches the solar cell voltage \( V_{PV} \). When a voltage is generated in \( L_3 \), a voltage corresponding to the winding ratio of \( L_3 : L_F \) is generated in the secondary winding \( L_F \). In addition, \( V_{LS} \) is equal to \( V_{PV} \), a voltage \( V_{LO} \) is generated in the tertiary winding \( L_O \), and energy is stored. When the charge of \( C_F \) is released and \( V_B \) becomes lower than \( V_{TH} \), \( Tr \) turns OFF; and a voltage of opposite polarity is generated from \( L_O \) to charge \( C_O \). This full cycle of operation is then repeated. When \( C_O \) is charged and the Pch-FET \( SW \) of the output stage is turned on, a switchable voltage is supplied to the control circuit.

This method uses the characteristics of a photovoltaic open-circuit voltage higher than the transistor threshold voltage. If this circuit pulls a high current, the photovoltaic voltage decreases to lower than the transistor threshold voltage, and thus it is necessary to keep a low current and maintain the photovoltaic voltage over the transistor threshold voltage. In practical use, it is necessary to start up within a wide range of equipment temperatures, e.g., -40 °C to 80 °C. In general, a photovoltaic open-circuit voltage and transistor threshold voltage also have negative temperature characteristics [11]. If the photovoltaic voltage is always higher than transistor threshold voltage it is able to startup and operate within a wide temperature range. To keep a low current, the settings of resistor \( R_S \) and turn numbers of transformer windings \( L_3 \) and \( L_F \) should not be too small. In this paper, these parameters are set to \( R_S = 470 \Omega \), \( L_3 = 5 \) Turns, and \( L_F = 10 \) Turns [15]. In addition, to endure the first start up current of the control circuit of a DC-DC converter, \( C_O \) should be set at a sufficiently high capacitance and in this paper is set to 100 μF.

2.3 The DC-DC converter circuit There are various topologies of DC-DC converters for photovoltaic cells or systems, for example, boost based [12], buck boost based [10], buck based [11], non-insulated [10-12], insulated [16, 17], continuous current mode (CCM), and discontinuous current mode (DCM) [18]. Many types of high-voltage gain DC-DC converters also have been proposed and non-insulated high voltage gain boost type DC-DC converters are classified mainly in several types of topologies [19] such as interleaved-based converters [20], multi-level based converters, cascade-based converters, coupled-inductor based converters, hybrid boost-flyback converters, switched capacitor based converters, and three stage switching cell converters. If voltage is added to a multiplier cell on the converter output side, it is also
possible to take a higher boost gain \(^{21}\). These converters are able to isolate the input to output and take a higher boost ratio by using a high-frequency transformer \(^{22}\). There is also a method of increasing the voltage by using multiple converters insulated by transformers and connecting the primary side in parallel and the secondary side in series \(^{23}\).

The required function and performance of a DC-DC converter for a single solar cell is discussed in the following. A single solar cell generates only an extremely low voltage of approximately 0.5 V. To input sufficient power to charge gadgets at approximately 10W, it is necessary to input a current of 20A. Therefore, the input resistance of the DC-DC converter should be set to a super low value. However, to the best of the authors’ knowledge, there have been no reports pointing out the challenges of the input resistance caused by an ultra-low input voltage of a single solar cell. Therefore, it is necessary to minimize the number of passes through the elements and it is desirable to use only one switching device in series. The input current also requires a low peak value, low ripple, and continuous conduction mode. This is because the loss on the input side is the square of the input current. For easy and stable control, a circuit topology that has a lower duty ratio on the Pulse Width Modulation (PWM) and a higher output voltage ratio is desired. To reduce the size and cost, it is desirable to hire only one control power semiconductor switch unified at the ground level. Because it is assumed that the system will be used with clothing, it is desirable to insulate the input and output when considering the level of safety. This is because if a solar cell, circuit, or connected equipment has a grounded fault, the voltage is low, and thus there is slight chance of electric shock, although smoke or fire should not occur. It is desirable to expand the circuits depending on the size and number of solar cells. This function is satisfied through a parallelization or serialization on the input or output sides. If the input side is parallelized, it is able to reduce the current into each switching device to a proportionate parallelization. If the output side is serialized, the output voltage is more boosted proportionately to the number of serializations. The requirements to a DC-DC converter for a single cell solar cell and a comparison of the basic suitable DC-DC converter topologies are shown in Table 1.

According to Table 1, the insulated boost type is selected as a basic converter \(^{24, 25}\). The circuit diagram of the boost type converter with a high-frequency transformer is shown in Fig. 8. The circuit consists of a single solar cell PV, input capacitor \(C_{IN1}\), DC inductor \(L_{OUT}\), high frequency transformer \(T_{M1}\), output diodes \(D_{O2}\) and \(D_{O3}\), output capacitor \(C_{OUT}\), and load resistance \(R_L\). The circuit operation mode is shown in Fig. 9. In Mode 1, SW1 and SW2 are both ON; the input current flows through \(L_{OUT}\), \(T_{M1}\), \(SW_1\), and \(SW_2\), and the energy is stored in \(L_{OUT}\). In mode 2, SW1 is ON, input current flows \(L_{OUT}\), \(T_{M1}\), and \(SW_2\). The output current flows through \(T_{M1}\), \(D_{O2}\), and \(R_L\). In mode 3, SW2 is ON, and the input current flows through \(L_{OUT}\), \(T_{M1}\), and \(SW_2\). The output current flows through \(T_{M1}\), \(D_{O2}\), and \(R_L\). In mode 4, SW1 and SW2 are both OFF; and in this paper, this mode is not used. Because it is necessary to secure a current path of the DC inductor current \(I_L\), there is no timing whereby both switches \(SW_1\) and \(SW_2\) are OFF. Therefore, it is necessary to control the switching timing within \(0.5 < \text{Duty} < 1\).

![Fig. 8 Boost-type DC-DC converter circuit.](image-url)

**4.2 Modeling of input resistance** To consider the

| Point | Boost | Buck | Buck Boost | Buck (Typical Pull Pull) | Buck Boost (Typical Flyback) |
|-------|-------|------|------------|-------------------------|-----------------------------|
| Importance | Non Insulated | Insulated | Non Insulated | Insulated | Insulated | Non Insulated | Insulated | Insulated |
| Galactic Insulated input to output | × Non Insulated | × Non Insulated | × Non Insulated | ●● Insulated | ○ Insulated | ○ Insulated | ○ Insulated |
| Low input series resistance | SW:ON \(R_{sw}+R_{L}\) | SW:OFF \(R_{sw}+R_{L}\) | SW:ON \(R_{sw}+R_{L}\) | SW:OFF Open | SW:ON \(R_{sw}+R_{L}\) | SW:OFF Open | SW:ON \(R_{sw}+R_{L}\) | SW:OFF Open |
| Lift ratio \(α\) (no input) \((\text{Winding ratio}=n2/n1)\) | \(0 < α < 1\) | \(0 < α < 1\) | \(10 < α < 50\) | \(0 < α < 9\) | \(10 < α < 50\) | \(0 < α < 9\) | \(10 < α < 50\) | \(0 < α < 9\) |
| Continuity of input current | Continuous | Different | Continuous | Continuous | Continuous | Continuous | Continuous | Continuous |
| Expandability of input | | | | | | | | |
| Purity of output | Possible | Possible | Possible | Possible | Possible | Possible | Possible | Possible |
| Number of switching devices | SW:ON SW1 | SW:ON SW1 | SW:ON SW1 | SW:ON SW1 | SW:ON SW1 | SW:ON SW1 | SW:ON SW1 | SW:ON SW1 |
| Same voltage level of SW (FEI) source and control power supply | same | different | different | same | same | same | same | same |
| Total judgment \((\text{Importance}^\star\text{point})\) | 98 | 0 | 8 | 245 | 108 | 140 |

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**Table 1 Comparison of suitable basic DC-DC converter topologies.**
operation of low-voltage input DC-DC converter, the circuit is modeled in the steady state of the converter, as shown in Fig. 10. The input resistance $R_{IN}$ is defined as an equivalent series resistance of each component: DC inductor $R_{Ldi}$, primary side winding of transformer $R_{TM1}$, semiconductor switches $R_{SW}$, and wiring on the printed circuit board (PCB) $R_{PCB}$.

\[ R_{IN} = R_{Ldi} + R_{TM1} + R_{SW} + R_{PCB} \]  
(1)

In the DC-DC converter with a low input voltage $V_{IN}$, a large current $I_{IN}$ flows through the input stage, and thus the loss owing to the input resistance $R_{IN}$ is large. The power $P_{IN,A}$ that can be input to the actual DC-DC converter is given by Equation (2).

\[ P_{IN,A} = -R_{IN} \cdot I_{IN}^2 + V_{IN} \cdot I_{IN} \]  
(2)

For example, when the input power $P_{IN}$ of a sample circuit is 3.5 W, the input resistance is $R_{IN} = 35.6 \text{ m}\Omega$, and the maximum real input power $P_{IN,MAX}$ is 1.76 W, which is shown by Equation (3).

\[ P_{IN,MAX} = \frac{V_{IN}^2}{4 \cdot R_{IN}} \]  
(3)

The relationship between the input current $I_{IN}$ and the actual input power $P_{IN,A}$ is shown in Fig. 11.

![Fig. 11 Relationship between input current and actual input power](image)

**3. Examination of high power and high efficiency**

**3.1 Resistance reduction of main circuit** Reducing the input resistance $R_{IN}$ leads to a high-power input and high efficiency. In a former study, it was confirmed that the switching devices and transformer make up more than 60% of whole loss, as shown in Fig. 12. Thus, it is important to reduce the loss of the devices. There are two directions on how to reduce the input resistance $R_{IN}$. One is reducing the resistance of the circuit elements itself, e.g., the switching devices, transformers, and DC inductors. The other is multiply parallelizing the circuit without changing the elements. This consideration was described in detail in a former study \(^{[10]}\), and thus it is recommended as a reference. In this study, parallelization is applied. The relationship between the actual input power $P_{IN,A}$ and the efficiency $\eta$ of the input stage when the input resistance $R_{IN}$ is used as a parameter is shown in Equation (4).

\[ \eta = 1 - \frac{R_{IN}}{V_{IN}} \cdot I_{IN} \]  
\[ V_{IN} = \sqrt{\left(\frac{V_{IN}}{R_{IN}}\right)^2 - 4 \cdot P_{IN,A}} \]  
(4)

**3.2 Main circuit parallelization** By parallelizing the primary side across the transformer of the main circuit, the input resistance $R_{IN}$ can be reduced, and by serializing the secondary side of the transformer, this contributes to a high-voltage output. The main circuit of the “m” parallel input and “n” serial output type is shown in Fig. 13. Assuming that the input resistance of the one main circuit is $R_{ON1}$, where the parallel number of the primary side is $P$. The actual input power $P_{IN,MAX}$ that can be input is

![Fig. 12 Losses on each part of main circuit](image)
his condition is shown in Equation (5).

\[ P_{\text{IN+MAX}} = \frac{V_{\text{PV}}^2}{4 \cdot R_{\text{IN}}} - \frac{V_{\text{PV}}^2 \cdot \text{Para}}{4 \cdot R_{\text{IN1}}} \]  

\[ R_{\text{IN}} = \frac{R_{\text{INL}}}{\text{Para}} \]  

In this case, by substituting the second line of Equation (5) into Equation (4), a relational expression between the real input power when the primary side of the main circuit is parallel with the efficiency \( \eta \) of the input stage is obtained. A graph of the real input power \( P_{\text{IN+MAX}} \) versus the input efficiency \( \eta \) under this condition is shown in Fig. 14. It can be seen that an input of 10 W or higher is possible if the primary side of the main circuit has six or more parallel circuits. The efficiency is approximately 60%.

### 3.3 Switching frequency and DC inductor setting

As shown in Fig. 12, the losses in the semiconductor switches are large, as determined through the basic experiments. This is largely due to the conduction loss from the low voltage and high current input of the single solar cell; however, as can be seen from Fig. 15, the ringing voltage and current when the switch is OFF are large as is the switching loss.

Thus, it is thought that reducing the switching frequency reduces the switching loss. When the switching frequency is low, the amplitude of the DC inductor current is large, which has the disadvantage of increasing the peak current. To suppress this peak current, the inductance of the DC inductor is increased. Therefore, it is necessary to reduce the switching frequency and increase the inductance together. The relationship between switching frequency \( f_{SW} \) and the inductance when the average current and the peak are constant is shown in Equation (6), and the model waveform of the current at this time is as shown in Fig. 16.

\[ f_{SW} \times L_d = \text{constant} \]  

(6)

As shown in Equation (7), the size of the inductor is determined by the maximum stored energy \( W \).

\[ W = \frac{1}{2} L_i \]  

(7)

The maximum stored energy is proportional to the inductance for the same current value. It is studied using two inductors, 15 and 150 \( \mu \)H, and applying the same cores for both, a 15 \( \mu \)H winding has 1 wire and 3 turns of \( \Phi_2 \), and a 150 \( \mu \)H winding has 4 wires and for each of the 10 turns of \( \Phi_1 \); the 4 wires are connected in parallel. In this case, the 150 \( \mu \)H inductor stores energy 10-times larger than the 15 \( \mu \)H inductor, although the 150 \( \mu \)H inductor still has some margin until the saturation of the magnetic flux density.

As the image of the inductor shown in Fig. 17 indicates, the core of the inductor is the same, and thus the size has not changed.
4. Experimental results

4.1 Target solar cell and load The target solar cell is assumed to be applied to wearable devices. Assuming that the area is 100,000 mm² (one side of approximately 300 mm) and the photoelectric conversion efficiency is 10%, the solar cell output when the solar radiation intensity is 1 kW/m² is set to \( P_{SV} = 10 \text{ W} \). When the solar cell voltage \( V_{PV} = 0.54 \text{ V} \), the current \( I_{PV} = 18.6 \text{ A} \) is obtained. Fig. 18 shows the P-V curve and I-V curve of the assumed solar cell. The current changes mainly with the solar radiation, the voltage changes mainly with temperature. In addition, the load is assumed to be a 12 V system battery or capacitor. Under this situation, a DC power supply with suitable specifications was used for a stable measurement of the electric performance.

4.2 Low-voltage startup circuit The low-voltage start-up circuit is shown in Fig. 6 and its operation is confirmed. The parameters are shown in Table 2 and the waveforms of each component are shown in Fig. 19. Fig. 19 (a) shows that the oscillation occurs at a frequency of 410 kHz, the duty cycle = 81%, and an output voltage of \( V_{CO} = 5 \text{ V} \) is obtained. Fig. 19 (b) shows the voltage waveforms before and after the output PchFET \( SW_{O} \). This indicates that the voltage before the FET output starts to gradually increase, beginning at the circuit starting time, until a certain threshold voltage is achieved. The FET then turns on and the voltage is outputted. As a result, startup failure owing to an inrush current of the control circuit connected to the subsequent stage is suppressed.

The static characteristics of the low-voltage start-up circuit are shown in Fig. 20. The output voltage is maintained at 5 V until the output power exceeds 0 to 12 mW, and when the output power is increased from there, the output voltage decreases. Therefore, the low-voltage start-up circuit can handle loads of up to 12 mW.

First, for the topic of practicality regarding a low-voltage startup circuit, sufficient power to start control circuit is required. The required power is defined based on the microcontroller and gate driver operation. The wattage of the microcontroller (Renesas RX220 series) is 5 V \( \times \) 2 mA = 10 mW, FET (ON Semiconductor NVMFS5C404N) with a gate drive power of 2 mW/FET at 10 kHz. The total consumption of the control circuit is 10 mW + 2 mW \times 2 = 14 mW. The low-voltage startup circuit can provide 12 mW and thus the power balance is approximately 2 mW in which a negative power is helped by the output capacitor \( C_{O} \). In this study, \( C_{O} = 100 \mu \text{F} \) is applied, and if the DC-DC converter can start the boot operation within 0.1 s, such value is sufficient. The output voltage \( V_{CO} \) waveform of the low-voltage startup circuit based on the simulation is shown in Fig. 21. If the main circuit needs longer to start up, it is able to do so by increasing the output capacitance \( C_{O} \).

Second topic of the practicality requirement on the low-voltage

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Table 2 Configuration of the low-voltage startup circuit

| Parts | Specifications |
|-------|----------------|
| \( T_{R} \) | 2n4923 |
| \( R_{L} \) | 470Ω |
| \( C_{F} \) | 5μF |
| \( R_{F} \) | 10Ω |
| \( L_{S} \) | 5Turn |
| \( L_{F} \) | 10Turn |
| \( L_{O} \) | 30Turn |
| \( C_{D} \) | 100μF |
| \( D_{O} \) | D1F3H3 |
| \( SW_{O} \) | REP15P05 |

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Fig. 18 Characteristics of target solar cell

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Fig. 19 Waveforms of low-voltage startup circuit
startup circuit is a startup within a wide temperature range. The temperature characteristics of the startable voltage of the low-voltage startup circuit are described. The temperature of the solar cell varies greatly from below freezing during winter before sunrise to high temperature during a hot summer, and thus it is considered that the startup characteristics are from −40 °C to 80 °C, as shown in Fig. 22. At −40 °C, the input voltage used for startup is approximately 0.65 V, and the required voltage becomes higher as the temperature decreases, although the output voltage of the solar cell also increases. In addition, at 80 °C, the startable voltage is as low as 0.42 V; however, the output voltage of the solar cell will also decrease, and caution is therefore required. With the combination of this circuit and a single solar cell, a startup is possible within the entire range of −40 °C to 80 °C, and a practical performance is achieved.

![Fig. 22 Temp. characteristics of low voltage start up circuit](image)

### 4.3 Main circuit operation and settings

To confirm the operation of the main circuit, an experiment under three circuit settings was conducted. Various parameters are shown in Table 3.

First, the waveforms with circuit setting 1 (one parallel, \( L_{dm} = 15 \mu H \), \( f_{SW} = 100 \text{ kHz} \)) at \( V_{PV} = 1.5 \text{ V} \), \( V_{OUT} = 12 \text{ V} \), and \( P_{OUT} = 10 \text{ W} \) are shown in Fig. 15. Fig. 15 (a) shows the DC inductor voltage \( v_{L} \) and current \( i_{L} \). Fig. 15 (b) shows the switch \( SW_{1} \) drain-source voltage \( v_{SW_{1}} \) and current \( i_{SW_{1}} \). Although the switch voltage and current are at 100 kHz, the DC inductor voltage and the current are at 200 kHz, and the currents of switches 11 and 21 are summed. In addition, at the moment when the conductor switch turns OFF, a large surge voltage is generated in both the switch and the DC inductor, whereby the DC inductor current drops sharply. Subsequently, the convergence of the surge voltage and the DC inductor current become constant.

Second, an extended (parallelized) circuit operation was conducted when fixed at \( V_{PV} = 0.5 \text{ V} \) and \( V_{OUT} = 12 \text{ V} \) on circuit setting 2 (4 parallel, \( L_{dm} = 15 \mu H \), \( f_{SW} = 100 \text{ Khz} \)). As shown in Fig. 23, the control phases of the four parallel circuits are shifted by 45°. The control phase of the “m” parallel circuit is obtained by 360/2 m. As shown in Fig. 24, the input and output voltage current waveforms are combined with the switching components of each circuit, resulting in a ripple of 800 kHz. The input voltage is 0.5 V with a 0.5 V p-p ripple, an input current of 11.3 A, and a 0.7 A p-p ripple. There is still room for improvement in terms of the voltage ripple, but current ripple is sufficiently reduced.

Third, a comparison was conducted regarding the output power and efficiency when fixed at \( V_{PV} = 0.5 \text{ V} \) and \( V_{OUT} = 12 \text{ V} \) between circuit setting 2 and circuit setting 3 (4 parallel, \( L = 150 \mu H \), 10 kHz). As shown in Fig. 25, when the input power increases the output power increases under both settings, although its pace decreases when more power increases. In addition, when the power increases the efficiency decreases, which is considered an increasing loss owing to the increase in current through the internal resistance of the main circuit. The maximum output power

![Fig. 23 Waveforms of the four phases of PWM pulses (each shifted by 45°)](image)

![Fig. 24 Waveforms of the four parallel four series circuit](image)

### Table 3 Main circuit configuration

| Circuit Configurations | Circuit Setting No. |
|------------------------|---------------------|
| Circuit                | 1 2 3               |
| DC Inductor \( L_{dm} \)| Core/TKD PC40 Ni-Zn |
| \( f_{SW} \)            | 100k 100k 10k       |
| Electrolytic cap. \( C_{Nnc} \) | 100μF |
| Transformer \( T_{dm} \) | Core TDK PC40 Ni-Zn |
| Switch \( SW_{1} \)     | ON Semi. NVMP855C404N |
| Diode \( D_{01a} \)     | Sanken FMEN-2208    |
| Simulated PV            | Kikusui             |
| DC Source               | PWR400L             |
| Simulated \( R_{c} \)   | Kikusui             |
| Electronic Load         | PLZ164WA            |

![Fig. 25 \( P_{OUT} \) and Efficiency on each \( f_{SW} \)](image)
of setting 2 was 4.6 W and the efficiency at this time was 40%, the maximum output power of setting 3 was 7.0 W, and the efficiency was 55.9%. Setting 3 is considered to contribute to a higher efficiency by reducing the switching loss owing to the reduced switching frequency. The maximum efficiency was 60.0% when \( P_{\text{OUT}} = 2.6 \text{ W} \) under setting 2, whereas it was 83.2% when \( P_{\text{OUT}} = 0.4 \text{ W} \) in setting 3. Because setting 3 achieved good results in the entire operational area, a subsequent evaluation will be conducted with setting 3.

4.4 Boost operation, output power, and efficiency

As the first topic of the practicality required on the main circuit, a sufficient voltage and power can be obtained for the operation of a portable device. A power supply of approximately 10 W (e.g., 5 V/2 A to 12 V/0.8 A) is desirable for charging mobile devices such as smartphones, home appliances, power tools, and outdoor equipment. Fig. 26 shows a static characteristic of \( P_{\text{IN}} \) versus \( V_{\text{OUT}} \) in each duty with \( V_{\text{PV}} = 0.5 \text{ V} \) constant. Within the full range, a higher \( V_{\text{OUT}} \) is obtained under higher duty. In addition, when \( P_{\text{IN}} \) increases, \( V_{\text{OUT}} \) decreases. The target voltage \( V_{\text{OUT}} = 12 \text{ V} \) is obtained at \( P_{\text{IN}} \) for approximately 10 W provided by a single solar cell. The maximum \( V_{\text{OUT}} \) is 45 V at \( P_{\text{IN}} = 10 \text{ W} \). This output voltage and power is useful for many varieties of applications. A static characteristic of \( P_{\text{IN}} \) versus \( P_{\text{OUT}} \) is shown in Fig. 27. On the whole, when \( P_{\text{IN}} \) increases, \( P_{\text{OUT}} \) increases; however, the efficiency decreases regardless of the duty. This is because when \( P_{\text{IN}} \) increases, the conduction loss increases owing to the \( I_{\text{IN}} \) flow through the internal resistance. In addition, comparing the same outputs, a higher duty (80%) indicates a lower \( P_{\text{OUT}} \) and efficiency than a lower duty (60%). This is because when the boost ratio increases, the switching loss increases. According to these results, it was confirmed that the required voltage and power are obtained, although there was room for improvement in terms of efficiency.

4.5 Study on capacitance loads and available area of MPPT

As the second and third topics of the practicality requirement on the main circuit, it is possible to operate from a low output voltage of 0 V up to 12 V, assuming charging applications such as batteries or capacitors, and MPPT operation under a wide range of situations is possible. Assuming that the power supply for wearable devices is an application, electricity will be stored in a battery or capacitor for use. Therefore, assuming a capacitor load, the circuit operation is confirmed when the capacitor voltage changes with the stored energy level. When \( V_{\text{OUT}} \) is lowered, the duty is narrowed down to prevent a decrease in \( V_{\text{PV}} \); however, owing to the limitation of the main circuit topology, the minimum duty is set to 50% or more. When stuck at a lower limit duty state, if \( V_{\text{OUT}} \) is lowered, \( V_{\text{PV}} \) will be lowered automatically. As shown in Fig. 28, the duty remains at 52% within the range of \( V_{\text{OUT}} \leq 5 \text{ V} \), and when \( V_{\text{OUT}} \) is further lowered, \( V_{\text{PV}} \) can be confirmed to drop from 0.5 V. When the capacitor load is assumed, it is necessary to operate from \( V_{\text{OUT}} = 0 \text{ V} \). When \( V_{\text{OUT}} = 0.1 \text{ V} \), and \( V_{\text{PV}} \) is as low as 0.28 V, the maximum power point of the solar cell is unable to be tracked; however, the output current flows 1 A, and thus the initial charging of the capacitor is possible. The least output voltage \( V_{\text{OUT}} \) that can operate at \( V_{\text{PV}} = 0.5 \text{ V} \) is 5 V. Namely, it is possible to operate at maximum power voltage \( V_{\text{PV,SP}} \) of the solar cell when \( V_{\text{OUT}} \geq 5 \text{ V} \). In addition, the output power \( P_{\text{OUT}} \) takes the maximum value when \( V_{\text{OUT}} = 14 \text{ V} \) and is 5.77 W. At \( V_{\text{OUT}} = 5 \text{ V} \), \( P_{\text{OUT}} = 4.9 \text{ W} \), which is almost 5 W. Within the range of \( V_{\text{OUT}} > 5 \text{ V} \), \( P_{\text{OUT}} \) is stable between 5 W and 5.77 W. Therefore, with a capacitor load, after
the initial charging, when operating at $V_{\text{OUT}} \geq 5 \text{ V}$, the maximum power of the solar cell can be reached. Regarding the power conversion efficiency, if it is operated in $V_{\text{OUT}} \geq 5 \text{ V}$, the mid-50% range is obtained and is considered to be practical. When the target output voltage $V_{\text{OUT}} = 12 \text{ V}$, the efficiency is 55.6%. According to these results, it was confirmed that operation is possible within an extremely low output voltage for the charging capacitor from 0 V, and that after pre-charging ($V_{\text{OUT}} \geq 5 \text{ V}$), an MPPT operation is possible.

5. Conclusion

The authors have been studying DC-DC converters for single solar cells thus far. In this paper, focus is on the practical use and confirmed performance through the operation of an actual circuit. For a low-voltage startup circuit, it was verified based on the static characteristics that sufficient power can be obtained to start the control circuit. Experimental data of the startup performance were collected in the presence of temperature changes, and it was confirmed whether a startup is possible in an environment of $-40 \degree \text{C}$ to $80 \degree \text{C}$.

Regarding the main circuit, a prototype circuit with four parallel connections on the primary side and four series connections on the secondary side was created and tested. The output voltage, power, and efficiency were measured using the studied circuit settings.

According to the test results, the DC-DC converter can provide a suitable voltage and power. In addition, it was confirmed that the DC-DC converter can achieve an initial charging of the capacitor load. When the output voltage is equal to or over 5 V, the MPPT operation is also acceptable.

In the following studies, additional research into more practical directions such as a further high efficiency and circuit miniaturization is planned.

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