EDCompress: Energy-Aware Model Compression with Dataflow

Zhehui Wang, Tao Luo, Joey Tianyi Zhou, Rick Siow Mong Goh
{wang_zhehui, luo_tao, joey_zhou, gohsm}@ihpc.a-star.edu.sg
Institute of High Performance Computing
Agency for Science, Technology and Research (A*STAR)

Abstract
Edge devices demand low energy consumption, cost and small form factor. To efficiently deploy convolutional neural network (CNN) models on edge device, energy-aware model compression becomes extremely important. However, existing work did not study this problem well because the lack of considering the diversity of dataflow in hardware architectures. In this paper, we propose EDCompress, an Energy-aware model compression method, which can effectively reduce the energy consumption and area overhead of hardware accelerators, with different Dataflows. Considering the very nature of model compression procedures, we recast the optimization process to a multi-step problem, and solve it by reinforcement learning algorithms. Experiments show that EDCompress could improve 20X, 17X, 37X energy efficiency in VGG-16, MobileNet, LeNet-5 networks, respectively, with negligible loss of accuracy. EDCompress could also find the optimal dataflow type for specific neural networks in terms of energy consumption and area overhead, which can guide the deployment of CNN models on hardware systems.

1 Introduction
Convolutional neural network (CNN) shows good performance in various applications such as image classification and object detection. However, traditional CNN is in large scale, which makes it challenging to implement on edge devices. For example, the VGG-16 network contains 528 MB weights [28]. To classify one image, we need to perform \(1.5 \times 10^{10}\) multiply–accumulate (MAC) operations. There are two consequences. First, the limited memory space of edge devices cannot store the parameters. Second, the edge device becomes power hungry because the calculation and data movement operations consume a large amount of energy.

Model compression method such as quantization and pruning, is an emerging technique developed in recent years to alleviate this problem. Most model compression method target to the reduction of model size. For example, Han et al. proposed Deep Compressing method [15], which helps to fit the neural networks into the on-chip memory of hardware accelerators. However, the model size does not directly decide the two significant metrics of edge device, i.e., the energy consumption and area overhead.

To prove this, we compare our work EDCompress (EDC) with Deep Compression (DC) in Figure[1] we can see that although EDCompress shows lower compression rate, it has higher energy and area efficiency than DC. This is because the energy consumption does not only depend on the model size, but also depend on the dataflow design, which is the way we reuse the data. In hardware accelerators, different processing elements may share the same input or output data. By reusing the data, there is no need to load the data from memory by multiple times. Given the fact that a large portion of the energy is spent on the data movement (e.g. around 72% in VGG-16). A good dataflow design can effectively improve the energy efficiency. In this paper, we propose EDCompress, which has two following features:

Preprint. Under review.
Algorithm 1 Computation of a typical convolutional layer

\[
\begin{align*}
\text{for } c_o & \text{ in range (}C_O\text{)} \text{ do} \\
& \quad \text{for } c_i \text{ in range (}C_I\text{)} \text{ do} \\
& \quad \quad \text{for } x \text{ in range (}X\text{)} \text{ do} \\
& \quad \quad \quad \text{for } y \text{ in range (}Y\text{)} \text{ do} \\
& \quad \quad \quad \quad \text{for } f_x \text{ from } -(F_X-1)/2 \text{ to } (F_X-1)/2 \text{ do} \\
& \quad \quad \quad \quad \quad \text{for } f_y \text{ from } -(F_Y-1)/2 \text{ to } (F_Y-1)/2 \text{ do} \\
& \quad \quad \quad \quad \quad \quad O[c_o][x][y]+=I[c_i][x+f_x][y+f_y] \times W[c_o][c_i][f_x][f_y]
\end{align*}
\]

• Dataflow Awareness: This paper first studies model compression problem with the knowledge of the diversity of dataflow designs. We study the impact of different dataflow designs on quantization and pruning, and exploit the best model compression strategy in terms of energy consumption and area.

• Automated Approach: We first formulate the energy-aware model compression as a multi-step optimization problem. At each step, we partially quantize or prune the model, and then fine tune the model by a few epochs. We further recast it into an reinforcement learning task.

2 Related work

Many energy based model compression methods have been proposed in the literature. For example, Wang et al. proposed a hardware-aware quantization method using the Deep Deterministic Policy Gradients (DDPG) algorithm [34]. He et al. proposed a pruning method for mobile devices using the DDPG algorithm [16]. Yang et al. proposed an energy-aware pruning method for low-power devices [38]. Cai et al. [2] and Yang et al. [39] proposed optimization methods to reduce the latency of neural networks. Several other work also focused on model compressing techniques, such as [15] [12] [35] [24] [3] [25] [22] [29]. According to the previous work, there are several effective model compression techniques, including pruning and quantization. In pruning [19] [21] [5] [6] [37] [14], we reduce the model size by replacing those weights with small absolute values by zeros. In quantization [6] [11] [32], we reduce the model size by decreasing the precision of the weights and the activations. These work reduce the size of parameters stored in the memory so that the compressed CNN can be applied on edge devices. Our proposed work EDCompress is different with them because we has considered the diversity of dataflow designs.

3 Energy-Aware Quantization/Pruning with Dataflow

Dataflow is an important concept in accelerators. It is related to the mapping strategy between the mathematical operations and the processing elements [40]. Algorithm 1 shows the computation of a typical convolutional layer. The algorithm contains six loops. One loop corresponds to one dimension in either the filter or the feature map. Here, \( C_O \) and \( C_I \) denote the number of output and input channels. \( X \) and \( Y \) denote the width and height of the feature map. \( F_X \) and \( F_Y \) denote the width and height of the filter. In each iteration of the innermost loop, we perform a basic operation called multiply–accumulate (MAC). Before the MAC operation, we read three elements from the memory, one from the input feature map, one from the weight, and one from the output feature map. After the MAC operation, we write the result into the memory. During the whole process, most of the energy is spent on the MAC calculation and data movement. To compute one conventional layer, we need to execute \( C_O \cdot C_I \cdot X \cdot Y \cdot F_X \cdot F_Y \) MAC operations in total.

In hardware accelerators using spatial architectures, we have an array or a matrix of processing elements, each one can execute the MAC operation independently. The strategy to map the operation into those elements becomes a key consideration in the hardware design. There is a large design space to explore. For example, given an array of processing element, we can unroll any one of the loops in the algorithm, and map each iteration in the loop into each processing element in the array.
we can save energy and reduce area overhead of the logic circuit using quantization and pruning. If the weights are quantized from 4 bits to 3 bits, we can skip the last row of adders; (c) If the weights are pruned, we can skip those multipliers whose weights are zero.

| Table 1: Popular dataflow types |
|---------------------------------|
| Dataflow | Applied by | Dataflow | Applied by | Dataflow | Applied by | Dataflow | Applied by |
| X: Y | [26] | X: F_X | [26] | X: F_X | [26] | C_f: C_O | [41] |

By similar rules, we can further unrolling two loops in the algorithm and map the MAC operations into a matrix of processing elements. With six loops in total, there are C_6^2=15 possibilities, each one corresponds to one dataflow design. Here, we introduce four popular dataflows in Table 1. They are denoted as A:B, where A and B stand for the name of each loop.

Different dataflow designs employ different data movement policies, and thus show different energy efficiency and area overhead. In Figure 2 (a), we show example of four popular dataflow designs. To simplify the figure, we only show four processing elements in each example. In real implementations, the A:B dataflow design requires A·B processing elements. In X:Y, we store MAC operation results in registers at output ports of processing elements. At each iteration, we read the last MAC operation result from registers. In F_X:F_Y, we store F_X·F_Y weights in registers at input ports of processing elements. At each iteration, we sum up F_X·F_Y MAC operation results. In X:F_X, we store F_X weights in registers at input ports of processing elements. At each iteration, we reuse the weights by X times, and sum up F_X MAC operation results. In C_f:C_O, at each iteration, we reuse the input feature map by C_O times, and sum up C_f MAC operation results.

3.1 Improvement on Energy and Area Efficiency

Quantization and pruning are two popular techniques in model compression. To quantize a model, we lower the precision of parameters based on the quantization depth (the number of digits presenting a parameter). After quantization, the low precision parameters may still store enough information for model inference. To prune a model, we replace some of the parameters in the model to be zero. A well-trained model usually contains many weights with small absolute values. We sort all the weights in the filter, and replace those weights with the least absolute values by zeros.

We can save energy and reduce area overhead of the logic circuit using quantization and pruning. Figure 2(b) shows the inner structure of a 4 bits×4 bits multiplier, which contains 12 adders. If the weights are quantized from 4 bits to 3 bits, we can skip the last row of adders, and thus save the energy consumption and reduce the area overhead. In real application, a high precision model with 32FP data type (32 bit float point) requires 23 bit×23 bit multipliers, with 506 adders in total. If both the activations and weights can be quantized, we can save a plenty of energy and area overhead. For example, if the activations are quantized from 32FP to 16FP, and the weights are quantized from 32FP to 8INT (8 bit integer), only 10 bit×8 bit multipliers are required, with 72 adders in total, which is 86% less than the original amount. Figure 2(c) shows an array of three processing elements, each containing a multiplier and an adder. If the weights are pruned, some processing elements would have inputs equaling zero. In this case, we can skip the related multiplier, and thus save the energy consumption.
We then fine-tune the model, train a few more epochs, and check the accuracy and energy of the model. We show an example of the multi-step optimization process in Figure 3 (a). In each step, we increase or decrease the quantization depth/pruning remaining amount at each step. The searching space of optimal solutions in this problem is very huge. In general, an L-layer model has $15 \times 10^L \times 23^L$ possible choices, assuming 1% pruning amount granularity. Designers are always facing many choices, and in most cases, they have to make decisions by their experience on different dataflows.

### 3.2 Recasting to the Multi-Step Problem

We recast the model compression process to a multi-step problem. Our goal is to lower the energy consumption and area overhead of edge devices while keeping the accuracy of the model. Instead of quantizing/pruning the model directly in one step, our final target is approached through a sequence of quantization/pruning steps. This is because we cannot alter the parameters too much at one time. Otherwise, the performance of the model will be reduced obviously, and it will be too difficult to restore the model [42].

We show an example of the multi-step optimization process in Figure 3 (a). In each step, we increase or decrease the quantization depth (the precision of the parameters) or the prune amount in different layers. For example, in step 1, we prune 40% weights, and quantize the remaining weights by 3 bit. Since the accuracy drops a lot at this step, we abort the optimization process. The quantization depth and pruning amount can be adjusted independently at each step. The searching space of optimal solutions in this problem is very huge. In general, an L-layer model has $15 \times 10^L \times 23^L$ possible choices, assuming 1% pruning amount granularity. Designers are always facing many choices, and in most cases, they have to make decisions by their experience on different dataflows.

### 3.3 Optimization through Reinforcement Learning

Reinforcement learning is a good candidate to solve the multi-step problem. We propose a method to search for the best model compression strategy for high energy efficiency and high area efficiency via reinforcement learning algorithms, considering the diversity of dataflow designs. This mechanism can automatically explore the design space, and find the optimal quantization/pruning policies for each dataflow. We show the overview of our reinforcement learning model in Figure 3 (b). In each episode, an agent interacts with the environment (the CNN model) via a sequence of steps. In each step $t$, the agent generates an action vector $a_t$ based on the state vector of the environment $S_t$. The environment responds to action $a_t$, quantize/prune the parameters in the model, and change its state to $S_{t+1}$. The model is then fine tuned by one or few epochs, and a reward $r_t$ considering both accuracy and energy consumption is returned. For large dataset such as ImageNet, the model is not fine tuned in the first few steps. The agent then updates its own parameters for achieving higher rewards in later actions. In each episode, we start from 100% pruning remaining amount and 8 bit...
quantization depth. An episode ends if the number of steps exceeds the limit, or the accuracy of the model drops below the predefined threshold. The reason of this limit is to make the episode stop when we reach the optimal point.

\[ Q_t^l = Q_0^l + \sum_{i=0}^{t-1} q_i^l \gamma^i \]
\[ P_t = P_0^l + \sum_{i=0}^{t-1} p_i^l \gamma^i \]

The quantization depth and the pruning remaining amount can be expressed by Equation 1. Here, \( Q_0^l \) and \( P_0^l \) denote the original quantization depth and pruning remaining amount of \( l \)-th layer in the CNN model before the optimization. \( Q_t^l \) and \( P_t^l \) denote the quantization depth and the pruning remaining amount after optimization step \( t - 1 \). To obtain \( Q_t^l \) and \( P_t^l \), we need \( t \) steps of optimization. In step \( i \), the agent changes the values of \( Q^l_i \) and \( P^l_i \) by \( q_i^l \) and \( p_i^l \) respectively. To get a better optimization result, we take smaller steps when \( Q_t^l \) and \( P_t^l \) are close to the optimal point. The discount factor \( \gamma \) is used to regulate the variance of \( q_i^l \) and \( p_i^l \). We test different values of \( \gamma \) in experiments, and find that \( \gamma = 0.9 \) is an optimal value.

\[ a_t = \left( \bigcup_{l=0}^{L-1} \{ q_t^l \} \right) \cup \left( \bigcup_{l=0}^{L-1} \{ p_t^l \} \right) \]

The action \( a_t \) can be expressed by Equation 2. Here \( a_t \) is the set containing changes of \( Q \) and \( P \) in all layers. Although the quantization depth is a discrete variable, we use the continuous action space. This is because we don’t want to lose the small changes of the quantization depth accumulated in each optimization step. When we fine tune the network, we round the quantization depth to the nearest integer value.

\[ s_t = \left( \bigcup_{m=t-\tau}^{t} \bigcup_{l=0}^{L-1} \{ Q_m^l \} \right) \cup \left( \bigcup_{m=t-\tau}^{t} \bigcup_{l=0}^{L-1} \{ P_m^l \} \right) \cup \left( \bigcup_{m=t-\tau}^{t} \{ r_m \} \right) \cup \{ t \} \]

The state \( s_t \) can be expressed by Equation 3. Here \( s_t \) is the set containing all the quantization depth \( Q \), the pruning remaining amount \( P \), and the reward \( r \) from step \( t - \tau \) to step \( t \). It also contains \( t \), the index of current step. We want the state of the environment to well reflect the history of the optimization process. Hence, the state contains the values of \( Q \) and \( P \) in previous \( \tau \) steps. To guarantee that the state set has the same dimension at any optimization step, we have \( Q_{t-\tau} = Q_0 \) and \( P_{t-\tau} = P_0 \) if \( t \) is less than \( \tau \).

\[ r_t = (\alpha_t / \alpha_{t-1} \lambda \beta_{t-1} / \beta_t) \]

The reward \( r_t \) can be expressed by Equation 4. Here, \( \alpha_t \) and \( \alpha_{t-1} \) are the accuracy at current step \( t \) and previous step \( t - 1 \), respectively. \( \beta_t \) and \( \beta_{t-1} \) are the energy consumption at step \( t \) and step \( t - 1 \). The area overhead is not involved in this equation because it is highly correlated with energy consumption. Low energy consumption comes with a low area overhead. In the optimization process, we want to reduce the energy consumption and at the same time maintain the accuracy of the model. Intuitively, decreasing the quantization depth and the pruning remaining amount would reduce the energy consumption and at the same time decrease the accuracy. The reinforcement learning algorithms can automatically find the trade-off point between the accuracy \( \alpha \) and the energy consumption \( \beta \). We use a third parameter \( \lambda \) to show the importance of accuracy over the energy consumption. It is normally greater than \( 1 \), and is fixed during the optimization. We test different values of \( \lambda \) in experiments, and find that \( \lambda = 3 \) is an optimal value.

### 4 Experiment

**Algorithm setup:** we use a state-of-the-art reinforcement learning algorithms SAC (soft actor-critic) [13] to train our optimization model. Compared with classical large-space problems, the search space in our problem is not large, and SAC can approach the optimal solutions very quickly (less than ONE day on ImageNet using a single graphic card Titan Xp). We test EDCompress on the ImageNet, CIFAR-10 and MNIST datasets using three different neural networks: VGG-16 [28], MobileNet [17] and LeNet-5 [20]. VGG is a complex deep neural network. MobileNet is designed for computation efficiency. LeNet-5 is a simple neural network with only two neural layers. We study four dataflow types, which are the most commonly used dataflow types. In each episode, we
Table 2: Comparison of EDCompress and HAQ [34] on ImageNet using MobileNet

| Dataflow   | Norm. Energy | Norm. Area |
|------------|--------------|------------|
| Ours       | [15] [12] [35] [24] [3] [25] | Ours [15] [12] [35] [24] [3] [25] |
| X : Y      | 5.44 1.41 5.27 | 6.31 1.81 2.53 1.00 |
| F_X : F_Y  | 6.32 1.81 2.53 1.00 | 4.38 1.00 505 92.0 |
| C_I : C_O  | 24.41 15.10 1.69 7.78 5.56 1.00 |
| Top-1 Acc. | 64.8 68.3 64.8 68.3 |
| Top-5 Acc. | 85.9 88.3 85.9 88.3 |

Table 3: Comparison of EDCompress and the previous work [22] [29] on CIFAR-10 using VGG-16

| Dataflow   | Norm. Energy | Norm. Area |
|------------|--------------|------------|
| Ours       | [15] [12] [35] [24] [3] [25] | Ours [15] [12] [35] [24] [3] [25] |
| X : Y      | 24.41 15.10 1.69 7.78 5.56 1.00 |
| F_X : F_Y  | 22.61 14.42 2.31 6.42 4.20 1.27 |
| C_I : C_O  | 19.68 12.21 1.00 434 451 47.58 |
| Accuracy   | 93.1 93.4 91.3 93.1 93.4 91.3 |

Table 4: Comparison of EDCompress and the previous work [18] [12] [35] [24] [3] [25] on MNIST using LeNet-5 network. Total area is the maximum area that can support the function of each layer.

| Energy (μJ) | Area (mm²) |
|------------|------------|
| Ours       | [15] [12] [35] [24] [3] [25] | Ours [15] [12] [35] [24] [3] [25] |
| X : Y      | 6.32 1.81 2.53 1.00 |
| F_X : F_Y  | 4.38 1.00 505 92.0 |
| C_I : C_O  | 24.41 15.10 1.69 7.78 5.56 1.00 |
| Conv1      | 1.62 3.44 6.29 2.93 3.61 15.76 |
| Conv2      | 0.60 1.47 1.75 1.20 0.92 8.29 |
| FC1        | 0.06 0.07 0.04 0.06 0.02 0.32 |
| FC2        | 0.03 0.09 0.17 0.07 0.08 1.14 |
| Total      | 2.31 4.96 24.41 15.10 2.73 6.42 25.5 |
| Conv1      | 1.17 3.44 6.05 3.05 3.70 12.93 |
| Conv2      | 0.58 1.58 1.86 1.29 0.99 7.78 |
| FC1        | 0.08 0.08 0.05 0.07 0.02 0.38 |
| FC2        | 0.03 0.09 0.17 0.07 0.08 1.14 |
| Total      | 2.03 4.84 7.75 4.16 4.42 23.21 |
| Conv1      | 1.09 0.09 0.05 0.07 0.02 0.38 |
| Conv2      | 0.03 0.09 0.17 0.07 0.08 1.14 |
| FC1        | 0.10 0.09 0.05 0.07 0.02 0.38 |
| FC2        | 0.03 0.09 0.17 0.07 0.08 1.14 |
| Total      | 2.01 5.31 8.28 4.56 4.84 23.13 |
| Accuracy   | 99.3 99.1 99.1 99.1 99.0 99.1 |

start from a well-train model. When the last episode ends, we restore the weights from a saved checkpoint, and reset the quantization depth/pruning remaining amount in each layer.

Hardware setup: We implement popular dataflows X : Y, F_X : F_Y, X : F_X and C_I : C_O on the Xilinx Virtex UltraScale FPGA, and obtain the energy consumption and area overhead from the Xilinx XPE toolkit [36]. The energy can be reported in a few seconds. In the logic part, the multipliers, adders and registers are implemented on LUTs (lookup tables). An M × N multiplier requires M/2 × (N + 1) LUTs [33]. In our experiment, parameters in the feature map are quantized by 10 bits, while the weights are quantized by q-bit (q ranging from 0 to 8). Hence, we need 5q LUTs for a single 10 × (q + 1) multiplier. In the memory part, the on-chip memory is implemented on RAM (Random-Access Memory) modules. During inference, to save the memory space, the input feature map is not kept after the computation of each layer. Hence, the size of the memory modules must support the weights in all layers plus the maximum feature map in the model.

4.1 Comparison with the State-of-the-Art

EDCompress is effective on all kinds of datasets. Table 2, Table 3 and Table 4 compare EDCompress with the state-of-the-art work on the ImageNet, CIFAR-10 and MNIST datasets. Compared with HAQ on ImageNet, our EDCompress test on four dataflow types and could achieve averaged 3.8X, and 3.9X improvement in energy and area efficiency with similar accuracy. We then focused on small-size dataset because we are targeting on edge devices running lite applications. It shows that among the four dataflows, EDCompress could more effectively reduce the energy consumption and area overhead, with negligible loss of accuracy. Compared with the state-of-the-art work, EDCompress shows 9X improvement on energy efficiency and 8X improvement on area efficiency in LeNet-5, in average of the four dataflows. It also shows 11X/6X improvement on energy/area efficiency in VGG-16. If we optimize the model by EDCompress, the dataflow F_X : F_Y is the most appropriate choice for LeNet-5 in terms of energy consumption and area overhead, and the dataflow X : Y is the most appropriate one for VGG-16.
Comparisons also indicate that instead of compressing the model size, EDCompress is more efficient in the reduction of energy consumption and area overhead. For example, in Figure 4 we compare the energy and area between EDCompress and Deep Compression (DC) \[15\], layer by layer. From the figure, EDCompress shows 2.4X higher energy efficiency and 1.4X higher area efficiency than DC. We can see that in the third layer, DC shows better performance than EDCompress on energy consumption because this layer contains 93\% of the total parameters. However, this layer does not contribute to most of the energy consumption. In fact, compressing the first layer would be more helpful on the energy reduction, although it only contains 0.1\% of the parameters. Figure 4 and Table 4 show that EDCompress reduces much more energy consumption and area overhead in the first layer, compared with previous work. Another example is the dataflow $C_1 : C_0$, whose third layer contributes to most of the area overhead. From the figure, we can see that EDCompress shows higher area efficiency than DC in the third layer. This observation further proves that EDCompress is more efficient in the reduction of hardware resources.

4.2 Insights on Dataflow

Quantization and pruning have different effects on different dataflow designs. Figure 5 shows the optimization process of the hardware accelerators using three neural networks in terms of energy consumption and accuracy. We start the optimization from a model with activations in 16FP data type and weights in 8INT data type. From the figure, we can see that the reinforcement learning algorithm could effectively reduce the energy consumption, with negligible loss of accuracy. Figure 6
Figure 6: Energy consumption breakdown before and after the optimization of EDCompress. The solid bar and patterned bar represent results before and after the EDCompress, respectively.

Figure 7: The performance of EDCompress by applying quantization technique only, pruning technique only, and both quantization/pruning techniques shows the energy consumption breakdown of each dataflow before EDCompress (model using 16FP activations and 8INT weight) and after EDCompress. If we compare the optimized result from EDCompress with the original model, the energy efficiency in VGG-16, MobileNet, LeNet-5 networks can be improve by 20X, 17X, 37X, respective. More specifically, around 55% energy consumption are saved from processing elements and the rest 45% are saved from data movement.

The results also indicate that optimization could change our choice on dataflow types. Those dataflows that do not show good energy efficiency before the optimization may show very high energy efficiency after the optimization. Take the VGG-16 for example, before the optimization, the dataflow X : Y consumes the most energy among the four dataflows. However, after the optimization, X : Y consumes the second lowest energy consumption. This is because the energy consumption of hardware accelerators include the energy of MAC operations on processing elements, and the energy on data movement. As we can see from Figure 6, given the fixed pruning remaining amount and quantization depth, the energy consumed on processing elements are almost the same. The only way to save the energy is to spent less energy on data movement. Due to the optimization, the energy consumed on data movement decreases because the amount of delivered data is reduced. In this process, different dataflow designs have different amount of reduction on the delivered data. X : Y, in this case, is more efficient in data movement reduction, and therefore we can save more energy consumption on this dataflow than other dataflow types.

4.3 Insights on Quantization/Pruning

The effectiveness of quantization and pruning techniques on the reduction of energy consumption and area overhead is highly related to the dataflow design. Figure 7 shows their individual contributions. From the figure, we can see that in most cases, both quantization and pruning can effectively reduce the energy consumption and area overhead. More specifically, if we apply quantization technique only, EDCompress can achieve 5.6X improvement on energy efficiency and 4.3X improvement on area efficiency. If we apply pruning techniques only, EDCompress can achieve 3.8X/1.7X improvement on energy/area efficiency.

We have two observations in Figure 7. First, pruning shows very little improvement on area overhead of the $C_I : C_O$ dataflow design. Second, the small-scale model LeNet-5 prefers quantization over pruning. This is because in these cases, the accelerator demands more area on the processing elements than the memory modules. Pruning can effectively reduce the area of memory modules.
because of the reduction of model size. However, it is not good at decreasing the area of processing elements. Quantization, on the other hand, could reduce the area of both processing elements and memory modules effectively. Hence, the quantization technique would be more useful in these cases.

5 Conclusions

We propose EDCompress, an energy-aware model compression method with dataflow. To the best of our knowledge, this is the first paper studying this problem with the knowledge of the dataflow design in accelerators. Considering the very nature of model compression procedures, we recast the optimization to a multi-step problem, and solve it by reinforcement learning algorithms. EDCompress could find the optimal dataflow type for specific neural networks, which can guide the deployment of CNN on hardware systems. However, deciding which dataflow type to use in the hardware accelerator depends on many other constraints, such as the expected computation speed, the thermal design power, the fabrication budget, etc. Therefore, we leave the final decision to hardware developers.

References

[1] Manoj Alwani, Han Chen, Michael Ferdman, and Peter Milder. Fused-layer CNN Accelerators. In 2016 49th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), pages 1–12. IEEE, 2016.

[2] Han Cai, Ligeng Zhu, and Song Han. Proxylessnas: Direct Neural Architecture Search on Target Task and Hardware. arXiv preprint arXiv:1812.00332, 2018.

[3] Jing Chang and Jin Sha. Prune Deep Neural Networks With the Modified $L_{(1/2)}$ Penalty. IEEE Access, 7:2273–2280, 2018.

[4] Tianshi Chen, Zidong Du, Ninghui Sun, Jia Wang, Chengyong Wu, Yunji Chen, and Olivier Temam. Dian nao: A Small-Footprint High-Throughput Accelerator for Ubiquitous Machine-Learning. ACM SIGARCH Computer Architecture News, 42(1):269–284, 2014.

[5] Yu-Hsin Chen, Joel Emer, and Vivienne Sze. Eyeriss: A Spatial Architecture for Energy-Efficient Dataflow for Convolutional Neural Networks. ACM SIGARCH Computer Architecture News, 44(3):367–379, 2016.

[6] Caiwen Ding, Shuo Wang, Ning Liu, Kaidi Xu, Yanzhi Wang, and Yun Liang. REQ-YOLO: A Resource-Aware, Efficient Quantization Framework for Object Detection on FPGAs. In Proceedings of the 2019 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 33–42. ACM, 2019.

[7] Zidong Du, Robert Fasthuber, Tianshi Chen, Paolo Ienne, Ling Li, Tao Luo, Xiaobing Feng, Yunji Chen, and Olivier Temam. ShiDianNao: Shifting Vision Processing Closer to the Sensor. In Proceedings of the 42nd Annual International Symposium on Computer Architecture, pages 92–104, 2015.

[8] Biyi Fang, Xiao Zeng, and Mi Zhang. NestDNN: Resource-aware Multi-tenant On-device Deep Learning for Continuous Mobile Vision. In Proceedings of the 24th Annual International Conference on Mobile Computing and Networking, pages 115–127. ACM, 2018.

[9] A. Frickenstein, C. Unger, and W. Stechele. Resource-Aware Optimization of DNNs for Embedded Applications. In 2019 16th Conference on Computer and Robot Vision (CRV), pages 17–24, May 2019.

[10] Mingyu Gao, Jing Pu, Xuan Yang, Mark Horowitz, and Christos Kozyrakis. Tetris: Scalable and Efficient Neural Network Acceleration with 3D Memory. In Proceedings of the Twenty-Second International Conference on Architectural Support for Programming Languages and Operating Systems, pages 751–764, 2017.

[11] Xue Geng, Jie Fu, Bin Zhao, Jie Lin, Mohamed M Sabry Aly, Christopher J Pal, and Vijay Chandrasekhar. Dataflow-Based Joint Quantization for Deep Neural Networks. In DCC, page 574, 2019.
[12] Yiwen Guo, Anbang Yao, and Yurong Chen. Dynamic Network Surgery for Efficient DNNs. In Advances in neural information processing systems, pages 1379–1387, 2016.

[13] Tuomas Haarnoja, Aurick Zhou, Pieter Abbeel, and Sergey Levine. Soft Actor-critic: Off-policy Maximum Entropy Deep Reinforcement Learning with a Stochastic Actor. arXiv preprint arXiv:1801.01290, 2018.

[14] Ghouthi Boukli Hacene, Vincent Gripon, Matthieu Arzel, Nicolas Farrugia, and Yoshua Bengio. Quantized Guided Pruning for Efficient Hardware Implementations of Convolutional Neural Networks. arXiv preprint arXiv:1812.11337, 2018.

[15] Song Han, Huizi Mao, and William J Dally. Deep Compression: Compressing Deep Neural Networks with Pruning, Trained Quantization and Huffman Coding. arXiv preprint arXiv:1510.00149, 2015.

[16] Yihui He, Ji Lin, Zhiqian Liu, Hanrui Wang, Li-Jia Li, and Song Han. AMC: AutoML for Model Compression and Acceleration on Mobile Devicesyang2 017designing. In Proceedings of the European Conference on Computer Vision (ECCV), pages 784–800, 2018.

[17] Andrew G Howard, Menglong Zhu, Bo Chen, Dmitry Kalenichenko, Weijun Wang, Tobias Weyand, Marco Andreetto, and Hartwig Adam. Mobilenets: Efficient Convolutional Neural Networks for Mobile Vision Applications. arXiv preprint arXiv:1704.04861, 2017.

[18] Norman P Jouppi et al. In-Datacenter Performance Analysis of a Tensor Processing Unit. In Proceedings of the 44th Annual International Symposium on Computer Architecture, pages 1–12, 2017.

[19] Hyeong-Ju Kang. Accelerator-Aware Pruning for Convolutional Neural Networks. IEEE Transactions on Circuits and Systems for Video Technology, 2019.

[20] Yann LeCun, Léon Bottou, Yoshua Bengio, Patrick Haffner, et al. Gradient-based Learning Applied to Document Recognition. Proceedings of the IEEE, 86(11):2278–2324, 1998.

[21] Carl Lemaire, Andrew Achkar, and Pierre-Marc Jodoin. Structured Pruning of Neural Networks with Budget-Aware Regularization. In Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition, pages 9108–9116, 2019.

[22] Hao Li, Asim Kadav, Igor Durdanovic, Hanan Samet, and Hans Peter Graf. Pruning Filters for Efficient Convnets. arXiv preprint arXiv:1608.08710, 2016.

[23] Huimin Li, Xitian Fan, Li Jiao, Wei Cao, Xuegong Zhou, and Lingli Wang. A High Performance FPGA-based Accelerator for Large-Scale Convolutional Neural Networks. In 2016 26th International Conference on Field Programmable Logic and Applications (FPL), pages 1–9. IEEE, 2016.

[24] Zhenhua Liu, Jizheng Xu, Xiulian Peng, and Ruiqin Xiong. Frequency-domain Dynamic Pruning for Convolutional Neural Networks. In Advances in Neural Information Processing Systems, pages 1043–1053, 2018.

[25] Franco Manessi, Alessandro Rozza, Simone Bianco, Paolo Napoletano, and Raimondo Schettini. Automated Pruning for Deep Neural Network Compression. In 2018 24th International Conference on Pattern Recognition (ICPR), pages 657–664. IEEE, 2018.

[26] Jiantao Qiu, Jie Wang, Song Yao, Kaiyuan Guo, Boxun Li, Erjin Zhou, Jincheng Yu, Tianqi Tang, Ningyi Xu, Sen Song, et al. Going Deeper with Embedded FPGA Platform for Convolutional Neural Network. In Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 26–35, 2016.

[27] Yongming Shen, Michael Ferdman, and Peter Milder. Overcoming Resource Underutilization in Spatial CNN Accelerators. In 2016 26th International Conference on Field Programmable Logic and Applications (FPL), pages 1–4. IEEE, 2016.

[28] Karen Simonyan and Andrew Zisserman. Very Deep Convolutional Networks for Large-scale Image Recognition. arXiv preprint arXiv:1409.1556, 2014.
[29] Pravendra Singh, Vinay Kumar Verma, Piyush Rai, and Vinay P Namboodiri. Play and Prune: Adaptive Filter Pruning for Deep Model Compression. arXiv preprint arXiv:1905.04446, 2019.

[30] Mingcong Song, Jiaqi Zhang, Huixiang Chen, and Tao Li. Towards Efficient Microarchitectural Design for Accelerating Unsupervised GAN-based Deep Learning. In 2018 IEEE International Symposium on High Performance Computer Architecture (HPCA), pages 66–77. IEEE, 2018.

[31] Naveen Suda et al. Throughput-optimized OpenCL-based FPGA Accelerator for Large-Scale Convolutional Neural Networks. In Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 16–25, 2016.

[32] F. Tung and G. Mori. CLIP-Q: Deep Network Compression Learning by In-parallel Pruning-Quantization. In 2018 IEEE/CVF Conference on Computer Vision and Pattern Recognition, pages 7873–7882, June 2018.

[33] E George Walters. Array Multipliers for High Throughput in Xilinx FPGAs with 6-input LUTs. Computers, 5(4):20, 2016.

[34] Kuan Wang, Zhijian Liu, Yujun Lin, Ji Lin, and Song Han. HAQ: Hardware-Aware Automated Quantization with Mixed Precision. In Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition, pages 8612–8620, 2019.

[35] Xuefeng Xiao, Lianwen Jin, Yafeng Yang, Weixin Yang, Jun Sun, and Tianhai Chang. Building Fast and Compact Convolutional Neural Networks for Offline Handwritten Chinese Character Recognition. Pattern Recognition, 72:72–81, 2017.

[36] Xilinx. Vivado Design Suite User Guide. Technical Publication, 2018.

[37] Haichuan Yang, Yuhao Zhu, and Ji Liu. Energy-Constrained Compression for Deep Neural Networks via Weighted Sparse Projection and Layer Input Masking. arXiv preprint arXiv:1806.04321, 2018.

[38] Tien-Ju Yang, Yu-Hsin Chen, and Vivienne Sze. Designing Energy-Efficient Convolutional Neural Networks Using Energy-Aware Pruning. In Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition, pages 5687–5695, 2017.

[39] Tien-Ju Yang, Andrew Howard, Bo Chen, Xiao Zhang, Alec Go, Mark Sandler, Vivienne Sze, and Hartwig Adam. Netadapt: Platform-aware Neural Network Adaptation for Mobile Applications. In Proceedings of the European Conference on Computer Vision (ECCV), pages 285–300, 2018.

[40] Xuan Yang, Mingyu Gao, Jing Pu, Ankita Nayak, Qiaoyi Liu, Steven Emberton Bell, Jeff Ou Setter, Kaidi Cao, Heonjae Ha, Christos Kozyrakis, et al. DNN Dataflow Choice Is Overrated. arXiv preprint arXiv:1809.04070, 2018.

[41] Chen Zhang, Peng Li, Guangyu Sun, Yijin Guan, Bingjun Xiao, and Jason Cong. Optimizing FPGA-Based Accelerator Design for Deep Convolutional Neural Networks. In Proceedings of the 2015 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, pages 161–170, 2015.

[42] Michael Zhu and Suyog Gupta. To Prune, or Not to Prune: Exploring the Efficacy of Pruning for Model Compression. arXiv preprint arXiv:1710.01878, 2017.