Designing Parity Preserving Reversible Circuits

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Abstract
Making a reversible circuit fault-tolerant is much more difficult than classical circuit and there have been only a few works in the area of parity-preserving reversible logic design. Moreover, all of these designs are ad hoc, based on some pre-defined parity preserving reversible gates as building blocks. In this paper, we for the first time propose a novel and systematic approach towards parity preserving reversible circuits design. We provide some related theoretical results and give two algorithms, one from reversible specification to parity preserving reversible specification and another from irreversible specification to parity preserving reversible specification. We also evaluate the effectiveness of our approach by extensive experimental results.

Keywords: Fault Tolerance, Parity, Quantum Computing, Reversible Circuits.

1 Introduction and Motivation

It is known that erasure of a single bit of information dissipates heat equivalent to \(K_B T \ln 2\) [10], where \(K_B = 1.38 \times 10^{-23}\) J/K is Boltzmann constant and \(T\) is the room temperature in Kelvin. This heat dissipation is in conformity with the laws of thermodynamics applied to any irreversible process. Though classical logic is not reversible, it is possible to represent classical Boolean functions using reversible

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computation \cite{2}. On the other hand, any quantum computation is based on unitary evolution of quantum mechanical systems and is inherently reversible. However, with increasing demand on low power design, reversible logic finds application not only in quantum circuits, but also in classical applications involving nanotechnology, optical circuits, encoding/decoding etc.

Any physical device performing classical or quantum computation is subject to error due to noise in the environment or imperfections in the device. Fault tolerant computing can mitigate this. One of the important approaches towards fault tolerant computing is by using redundant parity bits. For classical circuits, bit flip is the most common type of error. For quantum circuits, in addition to bit flip, there might be phase flip as well. In this paper, we consider bit flip errors only.

Most common method for detecting bit-flip errors in storage or transmission is by means of parity checking. Classically, most arithmetic and other processing functions do not preserve the parity. One has to use redundant circuitry to compute and check the parity. Making a reversible circuit fault-tolerant is much more difficult than classical circuit, since reversible logic allows no feedback or fan-out. In \cite{16}, the notion of parity preserving reversible circuits was introduced. The idea is to design the reversible circuit in such a way that the parity between the input and the output bits are automatically conserved in absence of any error.

After \cite{16}, there has been a series of sporadic works in this area, such as designing adders \cite{9}, divider \cite{4}, multiplier \cite{17}, multiplexer \cite{19}, ALU \cite{20} etc. However, all of these designs are ad hoc, based on some pre-defined parity preserving reversible gates as building blocks. To the best of our knowledge, in this paper, we for the first time propose a novel and systematic approach towards parity preserving reversible circuits design. We provide some related theoretical results and give two algorithms, one from reversible specification to parity preserving reversible specification and another from irreversible specification to parity preserving reversible specification.

2 Reversible Logic Synthesis

An $n$-variable Boolean function is reversible if all its output patterns map uniquely to an input pattern and vice-versa. It can be expressed as an $n$-input, $n$-output bijection or alternatively, as a permutation function over the truth value set $\{0, 1, \ldots, 2^n - 1\}$. The problem of reversible logic synthesis is to map such a reversible Boolean function on a reversible logic gate library.

The gates are characterized by their implementation cost in quantum technologies, which is dubbed as Quantum Cost (QC) \cite{13} \cite{15}. Reversible logic gates can also be represented as an unitary transformation, therefore serving as building blocks for quantum computers. Few prominent classical reversible logic gates are presented below.

- **NOT gate**: $f(A) = \overline{A}$.
- **CNOT gate**: $f(A) = A$, $f(B) = A \oplus B$.
- **CCNOT gate**: Also known as Toffoli gate. $f(A) = A$, $f(B) = B$, $f(C) = AB \oplus C$. This gate can be generalized with $ToF_n$ gate, where first $n - 1$ variables are used as control lines. NOT and CNOT gates are denoted as $ToF_1$ and $ToF_2$ respectively.
• Peres gate: A sequence of $\text{Tof}_3(a,b,c)$, $\text{Tof}_2(a,b)$ or its inverse is known as Peres gate.

• Controlled Swap gate: Also known as Fredkin gate. $f(A) = A$, $f(B) = \overline{A}.B + A.C$, $f(C) = \overline{A}.C + A.B$. This gate can be generalized with $\text{Fred}_n$ gate ($n > 1$), where first $n - 2$ variables are used as control lines.

Multiple sets of reversible gates form an universal gate library for realizing classical Boolean functions such as, (i) NCT: NOT, CNOT, Toffoli. (ii) NCTS F: NOT, CNOT, Toffoli, SWAP, Fredkin. (iii) GT: $\text{Tof}_n$. (iv) GTGF: $\text{Tof}_n$ and $\text{Fred}_n$.

Reversible logic synthesis begins from a given $n$-variable Boolean function, which can be irreversible. The first step is to convert it to a reversible Boolean function by adding distinguishing output bits, known as garbage outputs. When additional input Boolean variables are needed for constructing the output function, those are referred as ancilla.

Reversible logic synthesis methods can be broadly classified in four categories as following. A different and more detailed classification is presented in a recent survey of reversible logic synthesis methods [18].

**Exact and Optimal methods:** These methods consider step-by-step exhaustive enumeration or formulating the logic synthesis as a SAT problem [6] or reachability problem [8]. Optimal implementation up to only 4-variable Boolean functions are known [5].

**Transformation-based method** [11][26]: These methods use a weighted graph representation for performing the transformations, while [11] proceed row-wise in the Boolean truth-table.

**Methods based on decision diagrams** [24, 12]: In this approach, each node of the decision diagram is converted to an equivalent reversible circuit structure. These methods reported excellent scaling for large Boolean functions, low QC at the cost of high number of garbage bits.

**ESOP-based methods:** For classical logic synthesis, the exclusive sum of products (ESOP) formulation is studied well for specific target technologies [14]. For reversible logic synthesis, the ESOP formulation [7] maps directly to the basic reversible logic gates and has led to significant research interest.

Among the above methods, methods based on Decision Diagrams and ESOP-based methods can synthesize an Irreversible Boolean specification to reversible circuit by adding extra garbage lines. However, these methods do not guarantee the minimum garbage count. On the other hand, determination of minimum garbage count and their assignment is non-trivial, particularly for Boolean functions with large number of variables [25]. To the best of our knowledge, no automatic reversible logic synthesis tool supports automatic derivation of parity-preserving Boolean specification from an irreversible/reversible Boolean specification. Our flow proposed in the paper can be complemented with any reversible logic synthesis flows, which work on reversible Boolean specifications.

### 3 Our Results

First we discuss how to convert a reversible Boolean specification (that does not necessarily consider parity preservation) into parity-preserving reversible specification.
Before proceeding, we count the number of $n$-variable parity preserving reversible Boolean functions in Theorem 1.

**Theorem 1** Total number of $n$-variable parity preserving reversible Boolean functions is $(2^{n-1})!^2$.

**Proof:** In the truth table of an $n$-variable reversible Boolean function, there are $2^n$ input and output rows. Half of the $2^n$ input (or output) rows, i.e., total $2^{n-1}$ rows would have odd parity and the other half would have even parity. For the function to be parity-preserving, the odd-parity input rows must map to the odd-parity output rows. There are $2^{n-1}$! such mappings. Corresponding to each of these, the even-parity input rows must map to the even-parity output rows and there are again $2^{n-1}$! such mappings. Hence the result follows. ■

The method of constructing a parity-preserving reversible specification from any reversible specification is described in the proof of Theorem 2.

**Theorem 2** Given any $n$-variable reversible Boolean specification, it can be converted to a parity-preserving reversible Boolean specification with the introduction of at most one extra variable.

**Proof:** If the function is already parity-preserving, we need not do anything. If not, then in the output column of the truth table, we can just put a 0 in the parity-matching rows and a 1 in the parity-mismatching rows. On the input side, the extra variable can be set to the constant 0. Hence the result follows. ■

### 3.1 Direct Method of Converting Irreversible Specification to Parity-preserving Reversible Specification

Next, we discuss the case when we are given an irreversible Boolean specification. One simple approach can be a two-phase procedure: first, to use some standard approaches for converting the irreversible specification to a reversible specification, and next, use the result of Theorem 2. However, the first phase in this approach may incur unnecessary extra garbage bits. To avoid this problem, we provide a direct method of converting a given irreversible specification to a parity-preserving reversible specification with theoretically bounded number of extra bits. The method is as follows.

Since the specification is irreversible, the output rows must contain duplicate bit-strings. Suppose there are $n$ input variables and hence $2^n$ rows in the truth table. Suppose there are $k < 2^n$ distinct output bit-strings, with the counts $n_1, \ldots, n_k$, such that $\sum_{i=1}^{k} n_i = 2^n$. For each $i = 1, \ldots, k$, out of $n_i$ rows with the same output bit-string, let $n_{i,p}$ be the number of rows where the input and the output parity is matching and so $n_i - n_{i,p}$ is the number of rows where the parity is not matching.

To differentiate the matching rows we need at least $\lceil \log_2 n_{i,p} \rceil$ extra bits. Similarly, to differentiate the mismatching rows, we need at least $\lceil \log_2 (n - n_{i,p}) \rceil$ extra bits. Hence, for the rows corresponding to the bit-string category $i$, the number of extra bits needed is one more than the maximum of these two numbers. The one additional bit is required to match the parity. Thus, the total number of extra bits needed is given by the maximum of the above quantity over all $i$’s. Hence, with the above formulation, we have the following result.
Theorem 3 The minimum number of extra bits needed to convert an irreversible specification to parity-preserving reversible specification is given by

\[ \max_{i=1}^{k} \max \{ \lceil \log_2 n_{i,p} \rceil + 1, \lceil \log_2 (n - n_{i,p}) \rceil + 1 \}. \]

3.2 Algorithm and its Complexity Analysis

In Algorithm 1, we present the procedure for converting an irreversible specification to parity-preserving reversible specification. Suppose \( x_1, \ldots, x_k \) are \( k \) integers \( \in \{0, \ldots, 2^n - 1\} \) denoting the decimal equivalent of distinct output bitstrings. Note that according to our notation, \( x_i \) appears \( n_i \) times. We will keep two arrays \( \text{match} \) and \( \text{mismatch} \) as follows. In the algorithm, \( \text{match}[x_i] \) will contain \( n_i \) and \( \text{mismatch}[x_i] \) will contain \( n - n_i \). The array \( \text{count}[i] \), for \( 0, \ldots, 2^n - 1 \), is filled from top to bottom order, corresponding to each output row as follows: \( \text{count}[i] \) contains how many times the \( i \)-th output row has appeared so far starting from the top row. The sign of \( \text{count}[i] \) is positive, if the parity is preserved, else it is negative.

Algorithm 1: Irreversible to Parity Preserving Reversible Specification

Input: \( n \), An integer array \( \text{out}[0 \ldots 2^n - 1] \), containing the decimal equivalent of the output rows of an \( n \)-variable Boolean function.

Output: Parity preserving reversible specification.

1. \( \max = 0; \)
2. for \( i = 0 \) to \( 2^n - 1 \) do
3. \hspace{1em} \( \text{match}[i] = 0, \text{mismatch}[i] = 0, \text{count}[i] = 0; \)
4. for \( \text{row} \leftarrow 0 \) to \( 2^n - 1 \) do
5. \hspace{1em} If parity matches, increment \( \text{match}[\text{out}[\text{row}]] \) by 1;
6. \hspace{1em} Otherwise, decrement \( \text{mismatch}[\text{out}[\text{row}]] \) by 1;
7. \hspace{1em} if \( \max < \text{match}[\text{out}[\text{row}]] \) then
8. \hspace{2em} \( \max = \text{match}[\text{out}[\text{row}]], \text{count}[\text{row}] = \text{match}[\text{out}[\text{row}]]; \)
9. \hspace{1em} if \( \max < \text{mismatch}[\text{out}[\text{row}]] \) then
10. \hspace{2em} \( \max = \text{mismatch}[\text{out}[\text{row}]], \text{count}[\text{row}] = -\text{match}[\text{out}[\text{row}]]; \)
11. \( g = \log_2 \max + 1; \)
12. Add \( g \) columns to the Boolean output specification;
13. for \( \text{row} \leftarrow 0 \) to \( 2^n - 1 \) do
14. \hspace{1em} \( k = \text{abs}(\text{count}[\text{row}]); \)
15. \hspace{1em} Append binary value of \( k \) in the \( g - 1 \) bits;
16. \hspace{1em} Use the last bit to match parity;

Now we present the complexity of our algorithm in Theorem 4.

Theorem 4 For an \( n \)-input \( m \)-output Boolean specification, the running time of Algorithm 1 is \( O((n + m)2^n) \).

Proof: The maximum number of input or output rows in the Boolean specification is \( 2^n \). Let there be \( k < 2^n \) distinct output bit-strings with the counts \( n_1, \ldots, n_k \), such that \( \sum_{i=1}^{k} n_i = 2^n \). For each row we have to compute the number of 1’s in the input and output bit-strings for computing the parity. The algorithmic complexity for this
traversal is $O((n + m)2^n)$, which accounts for Steps 2 to 10. After this computation, we have one more iteration over the output rows through Step 13 to 16, the running time of which is dominated by $O((n + m)2^n)$. Hence the result follows.

4 Experimental Results

The proposed algorithm has been implemented and tested on several benchmark circuits, using C++ on an Intel(R) Core(TM) i5-3570 CPU (Quad-core) with 3.40GHz clock and 6 MB cache, having Linux version 2.6.32-358.6.2.el6.x86_64 as the OS, and gcc version 4.4.7 as the compiler. First, we compared our automatically generated parity-preserving reversible circuits with manually created parity-preserving reversible circuits reported by others. Our comparison metric is the number of additional garbage lines required for preserving parity.

4.1 Comparison with State-of-the-art

After following the proposed algorithm the irreversible Boolean specification is transformed to a reversible one (Table 1, Table 2) with the required number of constant input and garbage lines. The ancilla inputs and garbage outputs are referred as $A_i$ and $G_i$ respectively. The reversible specification thus obtained can be used to implement the reversible circuit using the well-known reversible logic synthesis methods for garbage-free synthesis [11].

| Table 1: Half adder Boolean Specification |
|------------------------------------------|
| Irreversible Specification               | Reversible Specification |
| **Input** | **Output** | **Input** | **$A_1$** | **$A_2$** | **Output** | **$G_1$** | **$G_2$** |
| 00 | 00 | 00 | 0 0 0 | 0 0 0 |
| 01 | 10 | 01 | 0 0 0 | 1 0 0 |
| 10 | 10 | 10 | 0 0 0 | 1 1 1 |
| 11 | 01 | 11 | 0 0 0 | 0 1 1 |

In terms of the ancilla and garbage count, we obtain exactly the same number for both the half-adder and full-adder circuits as obtained manually in [21] [1].

| Table 2: Full Adder Boolean Specification |
|------------------------------------------|
| Irreversible Specification               | Reversible Specification |
| **Input** | **Output** | **Input** | **$A_1$** | **$A_2$** | **Output** | **$G_1$** | **$G_2$** | **$G_3$** |
| 000 | 00 | 000 | 0 0 0 | 0 0 0 |
| 001 | 10 | 001 | 0 0 0 | 1 0 0 |
| 010 | 10 | 010 | 0 0 0 | 1 0 1 |
| 011 | 01 | 011 | 0 0 0 | 0 0 1 |
| 100 | 10 | 100 | 0 0 0 | 1 1 0 |
| 101 | 01 | 101 | 0 0 0 | 0 1 1 |
| 110 | 01 | 110 | 0 0 0 | 0 1 0 |
| 111 | 11 | 111 | 0 0 0 | 1 0 1 |
4.2 Testing for Boolean functions with Large Variable Count

Apart from this we had tried the algorithm for several Boolean functions with large number of variables, for which obtaining a parity-preserving Boolean specification manually would be hard. These are presented in Table 3. In the table, the tar_* functions are from Tarannikov’s paper [23]. From [23, Equation 2], we use the parameter $c$ as 001 to construct an 8-variable, 2-resilient function then we get tar82_001.pla. Similarly tar93_110.pla and tar93_101.pla are 9 variable 3-resilient functions with the $c$ vector as 110 and 101 respectively. The functions like rdNK is presented in several benchmarks on reversible logic synthesis [15]. The input weight function rdNK has $N$ inputs and $K = \lfloor \log N \rfloor + 1$ outputs. Its output is the binary encoding of the number of ones in its input. The other functions are obtained from RevKit benchmark [22].

Table 3: Summary of results for exemplary Boolean functions with large no. of variables

| Function      | Input | Output | Garbage | Ancilla | Runtime (ms) |
|---------------|-------|--------|---------|---------|--------------|
| tar82_001.pla | 8     | 1      | 8       | 1       | 0.657        |
| tar93_110.pla | 9     | 1      | 8       | 0       | 1.888        |
| tar93_101.pla | 9     | 1      | 8       | 0       | 1.631        |
| rd53          | 5     | 3      | 5       | 3       | 0.18         |
| rd73          | 7     | 3      | 7       | 3       | 0.35         |
| rd84          | 8     | 4      | 8       | 4       | 0.64         |
| rd20_5        | 20    | 5      | 19      | 4       | 34.698       |
| rd10_4        | 10    | 4      | 9       | 3       | 34.698       |
| 0410184_85.pla| 14    | 14     | 1       | 1       | 14.172       |
| cycle10_61.pla| 12    | 12     | 1       | 1       | 14.172       |
| ham15_30.pla  | 15    | 15     | 1       | 1       | 30.152       |
| ham7_29.pla   | 7     | 7      | 1       | 1       | 0.198        |
| ham8_64.pla   | 8     | 8      | 1       | 1       | 0.314        |
| life_175.pla  | 9     | 9      | 1       | 1       | 0.448        |
| squar5.pla    | 5     | 8      | 1       | 4       | 6.765        |
| urf4_89.pla   | 11    | 11     | 1       | 1       | 1.76         |
| urf6.pla      | 15    | 15     | 1       | 1       | 29.208       |
| plus63mod8192.pla | 13 | 13     | 1       | 1       | 6.757        |

Our proposed algorithm can be used on any irreversible specification unlike the methods described in [21] and [9] where a new specific gate is introduced to realize one particular circuit. These gates may not be useful to realize other circuits. Our method is fully automated and general.

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