Point-of-load switched-capacitor DC-DC converter for distributed power systems

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Abstract. Integrated circuit (IC) of point-of-load DC-DC converter is presented. It is intended mainly for use in distributed power systems as a stand-alone IC or as an on-chip block of the system-on-chip. The converter is based on multiphase switched-capacitor architecture and implemented in commercially available, 180 nm bulk-CMOS process. The paper discusses features of output voltage control in the multiphase system over a wide range of input and output voltages and load currents as well as output noise reducing techniques. The results of the test samples evaluation are presented.

1. Introduction
A rapid growth of electronic equipment, operating with limited power resources such as mobile battery powered devices and on-board equipment of spacecraft requires increasing the efficiency of power supply system. One of the main challenges in the design of such equipment is to convert an output of electrochemical sources to interconnect bus voltages and from them to the variety of supply voltages of the modern integrated circuits (ICs). The use of ICs manufactured in different technologies makes it necessary to have up to four or five or more supply voltages in the same unit. Point-of-load (POL) power supplies solve the challenge of high peak current demands and low noise margins, required by microcontrollers or application specific ICs, by placing individual linear regulators or DC-DC converters close to their point of use.

The requirement for energy efficiency leads to the widespread replacement of linear voltage regulators (LVR), traditionally used for the final DC-DC power conversion, onto the switched-mode power suppliers (SMPS), which allow achieving higher efficiency in a wide range of input and output voltages and load currents [1]. The most promising solution for on-chip SMPS is a switched capacitor DC-DC converter. In recent years, several papers have demonstrated the use of different types of integrated capacitors (MOS, stackable metal-insulator-metal – MIM and trench) to achieve a performance competitive with SMPS, using discrete inductances, at powers up to 1 W [2–4].

This paper presents a project of a fully integrated switched capacitor SMPS designed to convert supply rail voltages 3.3 V and 5 V as well as voltages of different types of lithium cells to a wide range of supply voltages of submicron ICs.
The rest of the paper is organized as follows. In Section 2 architectures of switched-capacitor converters are discussed. In Section 3 we consider circuit solutions, which were used in developed IC. In Section 4 the experimental results are provided. Finally, the paper is concluded in Section 5.

2. Switched-capacitor DC-DC converters

2.1. Architecture
In general, the architecture of switched-capacitor DC-DC converter is quite simple. It is a set of capacitors and switches for their switching [1]. Voltage conversion is performed due to a redistribution of a charge in the capacitor array. In the first phase, capacitors are charged from the input voltage source. In the second phase, they are discharged to the load. A voltage conversion ratio is determined by the topology of the capacitor circuitry in the first and second phases. For a commonly used parallel-series capacitor connection in down converter circuit with \( n \) capacitors the conversion ratio ranges from \( 1/(2n-1) \) to \( (2n-2)/(2n-1) \). As a rule, switched-capacitor DC-DC converters use a reconfigurable architecture with a variety of topologies [2]. This ensures high efficiency in a wide range of input and output voltages.

2.2. Sources of losses
Design factors normally limit the available set of conversion ratios by two or three values. This leads to efficiency depending on the input and output voltage levels. The residual voltage is dissipated on the output resistance of the circuit, just like in a linear regulator. When parameters are far from optimal, the loss of efficiency can be tens of percent, and one of the tasks of the developer is the proper selection of a set of the conversion ratios. The output impedance of the switched-capacitor SMPS at low switching frequencies inversely proportional to the product of the effective switched capacitance on the switching frequency, which is about 1 MHz for circuits with external discrete capacitors and up to several tens of megahertz for fully integrated solutions. Higher output impedance limits the competitiveness of switched-capacitor SMPS against inductive SMPS. The third major source of losses is the parasitic capacitors associated with technological features of manufacturing of on-chip capacitors. For MOS and MIM capacitors parasitic capacitance from bottom plate to the substrate can reach several percents of the nominal capacity. This may reduce the efficiency of the converter by 10–15% in some ranges of operating voltages and currents [1]. The design of fully integrated SMPS must also take into account losses due to MOS-switches gate-capacitance recharging because they operate at much higher frequencies than in the inductive SMPS or capacitive SMPS with discrete external capacitors. A Proper account of all major sources of loss is the basis for optimization of the capacitive SMPS to achieve maximum efficiency in the desired range of operating voltages and currents.

2.3. The control techniques
There are two phases of regulation. The first phase is a selection of conversion topology for a course adjustment. In the second phase, the control of the SMPS output resistance is performed for a fine-tuning. Topology selection is implemented by a feedforward control circuit based on the data on input and output voltage levels. Fine adjustment of the output voltage is performed by a feedback circuit, which regulates the output resistance of the circuit and thus the voltage drop across it. Regulation of the output resistance can be carried out in several ways [1]. The techniques based on a frequency conversion control are most frequently used. A number of such methods have been developed, including a continuous-time regulation that uses voltage controlled oscillator in a feedback loop, and a digital control [5].

3. Designed DC-DC converter
A design goal was to develop a capacitive DC-DC converter suitable for stand-alone use as well as for incorporation into the system-on-chip. Its main parameters are as follows: input voltage of 2.8 V to 5.5 V, the output voltage of 1.2 V to 3.3 V, the output current up to 300 mA, design rules – 180 nm.
3.1. Architecture of the converter

Figure 1 shows the architecture of the designed switched-capacitor DC-DC converter.

![Converter Architecture Diagram](image)

**Figure 1.** Converter architecture. Basic units indicated: TSU – topology selection unit; NOPG – non-overlapping phase generator; SWC – switches control; CARR – capacitor array; PLVR – power linear voltage regulator; STUP – startup; PCG – primary clock generator; SVC – selector of values of switched capacitors; CU – control unit; CMPA – comparator array; FBRC – feedback resistor circuitry; LPS – logic power supply linear regulators; VREF – voltage reference; CPS – comparators power supply linear regulator; SCG – secondary clock generator.

3.2. Basic conversion cell

The designed converter includes 512 identical basic conversion cells, divided into 8 groups, the corresponding conversion phases. Each group contains four subgroups including 16 basic cells in each of them. This solution is necessary to control the total value of switch capacitors and provide a multiphase operation of the converter, which reduces the output noise.

The basic cell provides voltage conversion ratios of 1/3, 1/2, and 2/3. On-chip linear regulator implements the ratio of 1/1. Set of topologies used allows, on the one hand, to ensure high efficiency in a wide range of input and output voltages, and on the other hand, it allows the use of simple basic cell consisting of two capacitors and nine switches (figure 2).

![Basic Conversion Cell Diagram](image)

**Figure 2.** A basic conversion cell.

To achieve the conversion ratio of 2/3, both capacitors are connected in parallel between input and output in a charging phase and sequentially between the output and ground in a discharging phase. Ratios of 1/3 and 1/2 are similarly implemented using a series-parallel connection of capacitors. Increase the number of capacitors and switches in the cell in order to more accurately adjust the conversion ratios is limited to increasing losses in the switches and increasing of the cell output impedance. Figure 3 shows simulated diagrams of the efficiency against the input voltage for the capacitive SMPS, taking into account losses, and for the ideal linear regulator at the output voltage of 1.8 V. You can clearly see the points of SMPS topology changes.
Figure 3. The efficiency of (a) capacitive SMPS and (b) ideal LVR depending on the input voltage.

If there is a small difference between input and output voltages, a built-in linear regulator is the primary power supplier. Otherwise, it is connected in parallel to the main capacitive converter, when the output current reaches a value of more than 60% of the maximum level.

Figure 4 shows the efficiency of designed capacitive SMPS and ideal LVR, depending on the output current at the input voltage of 3.3 V and the output voltage of 1.8 V. One can see quite a high efficiency at medium and low currents. Reduced SMPS efficiency at high currents is explained by the increasing share of the current of LVR integrated on a chip. The decline in efficiency at the currents of less than 30 mA is caused by the increase of the relative share of losses on the recharging of MOSFET gate capacitances in switches.

Figure 4. The efficiency of (a) capacitive SMPS and (b) ideal LVR depending on the output current.

3.3. The control unit

The control unit of the converter consists of three parts: topology selection unit, a conversion frequency control circuit and a selector of values of switched capacitors. The topology selection unit uses a feedforward regulation, while the other two – a feedback loop regulation. A topology selection unit contains a resistive circuit, which is supplied with the input signal. It forms dynamically threshold voltages for three comparators. Their output signals are used for topology selection.

The feedback block comprises a controlled resistive circuit that forms threshold voltages for four comparators that determine the output voltage position in one of five ranges [6]. If the output voltage is in a third range, the frequency of controlled oscillator is constant. If it is in first or second ranges, frequency rises. If the voltage is in fourth or fifth ranges, frequency decreases. If the output voltage does not differ by more than 5% of the nominal value, comparators operate at a lower frequency for power saving. If the voltage is outside of these limits, the clock frequency is increased to ensure a more rapid response to transients.

The generator generates 32 clock frequencies in the range from 3 to 35 MHz. Since a conversion frequency has a lower limit, the operating current also had to be limited to some minimum value. The regulation would not be possible at lower currents. To solve this problem, the converter incorporates the block of control of the total value of the switched capacitance [7]. If the frequency is minimal, when receiving a control signal to the further decrease of the frequency, a half of currently used cells will be disconnected.
Similarly, a control signal to increase the frequency above the maximum value causes a doubling
the number of cells used in conversion. The circuit has five levels of switchable capacitance,
corresponding to the inclusion of 512, 256, 128, 64 and 32 basic cells. This solution can significantly
improve the efficiency at low and medium output currents, as shown in Figure 4.

3.4. Power supplies of the converter
The supply voltage of control logic is 1.8 V. The supply voltage of comparators is 2.5 V. To power
these circuits chip contains four linear regulators: one for the comparators, the other two for the digital
clock generator and the conversion frequency generator, and a fourth – for the rest of the digital logic
circuits.

The reference voltage is generated by a built-in band-gap voltage source. It is powered by a pre-
regulator, which features low-noise and produces a voltage of 2.5 V. The core of band-gap reference
has a conventional architecture, but instead of used diode-connected vertical p-n-p bipolar transistors,
it uses a dynamic threshold voltage MOSFET (DTMOS) transistors [8].

4. Implementation and measuring results
For experimental studies aimed at the test of the effectiveness of proposed solutions, a test chip has
been designed and manufactured. It comprises a converter of reduced power and a number of
dedicated test structures of the main functional blocks of the converter. The test chip has been
manufactured in commercially available, 180 nm bulk-CMOS process with five metal layers and
stacked MIM-capacitors having a specific capacity of 3 fF/mm$^2$. Figure 5 shows the measured output
voltage depending on the input voltage for several test samples. It can be seen that the converter has
an output voltage error of less than ±6 % over most of the operating range.

![Figure 5](image)
**Figure 5.** Measured output voltage versus the input voltage for four samples.

Figure 6 shows reference voltage output versus temperature for two test samples.

![Figure 6](image)
**Figure 6.** Temperature dependences of reference voltages of two samples.

Measurements showed that the voltage reference temperature drift is less than 0.2 mV/°C in
a temperature range from -60 °C to +125 °C, while the spread of the reference voltage about
the nominal value of 1.02 V from chip to chip is less than 20 mV.
Figure 7 shows a photo of the test version of designed IC.

![Photo of the chip of switched-capacitor DC-DC converter.](image)

**Figure 7.** Photo of the chip of switched-capacitor DC-DC converter.

### 5. Conclusion

A step-down (back) switched-capacitor DC-DC regulator for converting rail voltages of 5 V and 3.3 V as well as lithium electrochemical cell voltages to modern IC power supply voltages has been designed and evaluated. The designed IC is fully compatible with commercially available CMOS technology. As compared with the widely available capacitive SMPS it has a smaller noise level because of the multiphase architecture. It is suitable as POL power supply for stand-alone applications, and for the integration into systems on a chip, where its use will reduce power consumption compared to the built-in power supply, based on a linear regulator. The effectiveness of the proposed design solutions has been confirmed by the results of experimental studies of the test chip containing basic functional units of IC prototype.

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