Delving into Macro Placement with Reinforcement Learning

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Abstract—In physical design, human designers typically place macros via trial and error, which is a Markov decision process. Reinforcement learning (RL) methods have demonstrated superhuman performance on the macro placement. In this paper, we propose an extension to this prior work [1]. We first describe the details of the policy and value network architecture. We replace the force-directed method with DREAMPlace for placing standard cells in the RL environment. We also compare our improved method with other academic placers on public benchmarks.

I. INTRODUCTION

Physical design is a critical stage in the chip design process. It transforms an abstract hypergraph representation (a netlist with devices as nodes and interconnections as hyperedges) into a geometric representation (a layout). Physical design can be treated as an optimization problem, where the objective is to maximize the performance of the circuit subject to design constraints.

Due to the complexity of physical design, it is generally decomposed into several sub-stages, including floorplanning, placement, routing, etc. This split introduces a problem that we lack a synergistic view of these sub-stages. Taking placement as an example, it is standard practice to minimize wirelength as the main objective, ignoring other metrics. Although there is work focusing on the co-optimization of these stages (e.g., routing congestion aware placement [2] and timing driven placement [3]), there is still a huge gap between these sub-stages. As a result, circuit designers must iterate many times through the end-to-end design flow, in order to achieve design closure in a production chip design setting. Specifically, designers conduct physical design in a setting, try another one according to the previous result. This procedure will continue until the design closure is achieved.

The design process above is essentially a Markov Decision Process (MDP). The environment, the design automation software or tools, provides feedback for the agent who makes the decision. Therefore, the physical design problem becomes an optimization problem in MDP, which is a control problem. Inspired by the observation above and the success of reinforcement learning (RL), RL methods can be applied to the sub-stages mentioned above.

In [1], the authors propose to place macros using an RL algorithm. The agent places one macro at each time step. After all macros are placed, the environment places the standard cells and provides feedback to the agent. The learning algorithm adjusts the agent’s policy according to this feedback, just as human designers learn from feedback at various stages of the physical design process. By balancing exploration and exploitation, the agent can make superhuman decisions on seen and unseen design benchmarks.

II. RELATED WORK

A. Analytical placement

Analytical placement is a nonlinear optimization problem, where the decision variables are the locations of movable nodes. We minimize the total wirelength such that there is no overlap between nodes. We can also consider other metrics and constraints in this formulation, such as routing congestion metrics and region constraints.

ePlace/RePlAce [2], [5] is a family of state-of-the-art placement algorithms. The density of the placement is modeled as an electrostatic system. In particular, cells are modeled as
electric charges, and density penalty is formulated as the potential energy. Thus, the movable nodes will spread gradually driven by electric force, which is the gradient w.r.t. the density penalty. DREAMPlace [4] uses a machine learning framework to accelerate the computation of the ePlace/RePlAce algorithm.

B. Standard cell placement and mixed-size placement

There are two types of movable nodes in the placement problem, standard cells and macros. Standard cells have similar height, and they are often much smaller than macros. Moreover, the number of standard cells is much larger than that of macros (1 million vs. 100).

Above all, compared with standard cell placement, it is more difficult to place macros, especially large macros. The reason is that the large macros make the optimization problem more discrete compared with the standard cell placement. We solve the global placement in a continuous optimization using gradient based method, such that a small displacement on a macro may induce a large degradation of the circuit performance during the legalization stage. Circuit designers usually have to tune the location of large macros by hand in practice.

Researchers also propose specified methods to tackle the mixed-size placement [5]. Macros are often placed and fixed with heuristic legalization method at first. Standard cell placement follows as a standard operator afterwards.

C. Macro placement with reinforcement learning

Mirhoseini et al. [11] propose to place macros using RL methods. In their work, the RL agent determines the location of macros one by one. After all macros are placed and fixed, the macro placement solution is delivered to the environment for evaluation. In the environment, the standard cells are placed using a force-directed method. Performance metrics, such as wirelength and congestion, are evaluated and provided as the reward feedback to the RL agent. The RL learning algorithm updates the agent to improve the reward until good results are achieved.

III. Method

A. Policy and value network structure

The original work [11] applies several explicit approximations so that the environment can provide fast feedback, such as (1) clustering standard cells, (2) ignoring pin offset when calculating wirelength, and (3) discretizing the placement canvas. We validate that these approximations do not hurt the quality of the feedback significantly, yet saving much time.

Other than that, we find that there are many techniques making a trade-off between time and accuracy implicitly, such as, graph embedding instead of hypergraph embedding, shallow policy and value neural networks rather than a deep one. The mask is another typical example. A mask is generated to do the post-processing on the decision made by the RL agent such that the RL agent will not generate overlaps. However, intuitively, a good agent should learn to avoid placing macros in a blank grid instead of an occupied one, which means the mask is unnecessary. Without the mask, it takes a very long time for the agent to learn to avoid placing macros over each other in our experiments, let alone improving the circuit performance. Therefore, we prefer to use the mask since it can accelerate the learning process significantly.

The golden rule is to accelerate the interaction between RL agent and environment since the agent can learn from approximation. It is not necessary to obtain accurate feedback for the RL agent.

B. DREAMPlace as standard cell placer

A force-directed method is originally used to conduct standard cell placement in [1]. We replace it with DREAMPlace, which yields better placement results. Also, we believe that DREAMPlace is more similar to the algorithms used in commercial tools. Since the result of the commercial tools will be treated as the ground truth, the environment will provide more accurate feedback for training agents. Another advantage of DREAMPlace is its fast execution time, which helps to reduce the learning time. Please note that the DREAMPlace (or the force-directed method) is only used in the environment. During the final evaluation, the standard cells are placed by the commercial EDA tools.

IV. Experiments

To make fair comparisons with academic placers, we demonstrate our results on public benchmarks.

The modern mixed-size (MMS) placement benchmarks [6] are widely used for macro placement tasks. However, they are often used to measure the wirelength optimization due to the missing technology information. Since our method is not designed only to optimize wirelength, we do not focus on these benchmarks. Instead, we make changes to the ISPD 2015 benchmarks and make an evaluation on them. We first remove all the blockage and area constraints, and then allow every macro movable in the placement area. The target density is also updated accordingly. Since most of the academic placers do not support macro orientation optimization, we fix the macro orientation. Table 1 shows the statistics of the 9 edited benchmarks. There are overlaps in the original 28nm superblue benchmarks so that it is infeasible for us to allow each single macro movable. We only pick the designs with macros in 65nm technology.

We evaluate three methods on these benchmarks. The only difference between these methods is the source of macro location, which comes from (1) original benchmark, (2) DREAMPlace, and (3) our methods, respectively. A commercial EDA tool is used to complete the following placement and routing for evaluation. The half perimeter wirelength (HPWL) and congestion after global routing are listed in Table 1. We obtain a better wirelength and congestion on these benchmarks on average. On design matrix mult_a, we achieve 17% HPWL reduction with a lower congestion.

The public benchmarks used in this paper are relatively simple. They do not represent industry circuit designs with
### TABLE I

Statistics and results on ISPD 2015 benchmarks with movable macros. CongH, CongV represents horizontal and vertical congestion. Macro locations are from three methods. Results are reported by a commercial EDA tool after global routing.

| Benchmark      | # Macros | # Std Cells | Utility | Max Density | Original Location | DreamPlace | Ours |
|----------------|----------|-------------|---------|-------------|-------------------|------------|------|
|                |          |             | HPWL    | CongH       | CongV                | HPWL       | CongH | CongV |
| dex_peri_a      | 4        | 108286      | 0.72    | 0.72        | 2.19E+06           | 2.46E+06   | 0.08  | 1.96  | 2.34E+06 | 0.86  | 0.45 |
| edit_disi_a     | 6        | 127413      | 0.62    | 0.62        | 5.42E+06           | 5.01E+06   | 11.79 | 13.16 | 4.76E+06 | 9.02  | 11.2 |
| fli_a           | 6        | 30625       | 0.74    | 1           | 1.29E+06           | 1.22E+06   | 0.64  | 0.12  | 1.16E+06 | 1.81  | 0.04 |
| fli_b           | 6        | 30625       | 0.74    | 1           | 1.46E+06           | 1.43E+06   | 4.67  | 0.37  | 1.50E+06 | 5.55  | 0.85 |
| matrix_mult_a   | 5        | 149650      | 0.77    | 0.92        | 5.36E+06           | 5.36E+06   | 1.57  | 1.33  | 4.43E+06 | 0.29  | 0.4  |
| matrix_mult_b   | 7        | 146435      | 0.73    | 1           | 5.31E+06           | 6.24E+06   | 2.79  | 2.33  | 5.02E+06 | 0.15  | 0.66 |
| matrix_mult_c   | 7        | 146435      | 0.73    | 1           | 4.99E+06           | 5.23E+06   | 1.57  | 0.48  | 5.33E+06 | 4.52  | 0.55 |
| pci_bridge32_a  | 4        | 29517       | 0.41    | 0.41        | 5.94E+05           | 5.06E+05   | 0.11  | 0.62  | 4.82E+05 | 0     | 0    |
| pci_bridge32_b  | 6        | 28914       | 0.51    | 0.51        | 7.63E+05           | 9.50E+05   | 0     | 0.06  | 7.85E+05 | 0     | 0    |

### TABLE II

Comparisons on force-directed (FD) method and DREAMPlace (DP). Four confidential benchmarks are used for evaluation.

| Design | # Movable Macros | RL-FD                | RL-DP                |
|--------|------------------|----------------------|----------------------|
|        |                   | HPWL     | CongH | CongV | HPWL     | CongH | CongV |
| 1      | 1                | 926      | 6.85E+06 | 0.01 | 0.02 | 6.50E+06 | 0.01 | 0.02 |
| 2      | 2                | 873      | 1.69E+07 | 0   | 0.01 | 1.64E+07 | 0   | 0.01 |
| 3      | 3                | 768      | 1.36E+07 | 0   | 0   | 1.30E+07 | 0   | 0   |
| 4      | 4                | 1026     | 2.46E+07 | 0   | 0.01 | 2.46E+07 | 0   | 0.01 |
| ratio  |                  | 1.02     | 1.00    |       |       |       |       |       |

V. Conclusion

We extend the original work [1] in three perspectives. First, we provide more details on the motivation and algorithm design. Second, DREAMPlace is integrated into the original framework. Finally, we conduct experiments on public benchmarks and make fair comparisons with academic tools. We demonstrate that RL can achieve better results and help circuit designers.

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