Interface trap charges associated reliability analysis of Si/Ge heterojunction dopingless TFET

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Abstract
The interface trap charges (ITC) associated reliability analysis of a charge-plasma based asymmetric double-gate (ADG) dopingless tunnel field effect transistor (DLTFET) with Si/Ge heterojunction and high-κ gate dielectric (HJADGDLTFET) has been studied. The HJADGDLTFET uses silicon at the drain and the channel region, and germanium at the source region, which enhances the band-to-band tunnelling at the source-channel junction, and hence drive current is increased by one order concerning ADGDLTFET. Also, ADG and high-κ dielectric (HfO₂) have been used to maintain low off-state current values. The primary intention of this work is to investigate the impact of ITC for HJADGDLTFET and compare it for ADGDLTFET considering DC, analog/RF, and linearity parameters such as transfer characteristics, electric-field, electric potential, first-, second-, and third-order transconductances (g_m1, g_m2, and g_m3), gate-to-drain capacitance (C_{gd}), cut-off frequency (f_T), gain–bandwidth product, device efficiency, second- and third-order voltage intercept points (VIP2, VIP3), third-order input intercept points (IIP3), and third-order intermodulation distortion. The ATLAS simulation results show that the HJADGDLTFET is more immune to ITC variation than conventional ADGDLTFET concerning different polarities of ITC available at the semiconductor-oxide interface.

1 | INTRODUCTION

Apart from the improved functional capability of integrated circuits (IC), the unabated scaling of semiconductor devices [1] at the subnanometer regime also fosters challenges in fabrication, such as the requirement of highly doped abrupt junctions [2], thin oxide layers, and surface smoothness [3]. So, there is a quest for new devices [4], which can overcome the challenges mentioned above. In this pursuit, tunnel field effect transistor (TFET) has been advancing as an appropriate candidate due to its fundamental advantage of low off-state current (I_{OFF}), low subthreshold swing (SS), and insusceptibility against short-channel effects, and random dopant fluctuations (RDFs) [4]. However, TFET experiences the predicament of low on-state current (I_{ON}), ambipolarity, and substandard high-frequency characteristics. In this respect, different reports have been published in the literature, such as heteromaterial engineering [5], high-κ dielectric [6], gate work function (WF), pocket doping [7], gate-drain overlap/underlap [8, 9]. Among them, a CP-based DLTFET [10] has engaged much attention, as it effaces RDFs and the requirement of thermal budget resulting in the formation of the abrupt junction without any chemical doping. However, Si-DLTFET demonstrates low I_{ON} as Si possesses large effective masses for electron, which leads to the modest lateral electric field in the source-channel tunnelling junction, like conventional Si-TFET. To intensify I_{ON}, a Si/Ge HJADGDLTFET has been reported earlier, in which germanium (Ge) and HfO₂ are used as the source region and gate dielectric instead of silicon (Si) and SiO₂ respectively [11]. The substitution of SiO₂ with a high-κ dielectric (HfO₂) precedes by a high leakage current as a result of direct tunnelling of carriers via SiO₂ and declined reliability against electrical breakdown [12].

Besides, from the TFET application aspect, the transfer characteristics, as well as its reliability, ought to be guaranteed. The reliability issues in the TFET are relatively severe because of the presence of trapped mobile ionic and fixed charges (in positive [PITC] as well as negative [NITC] polarity) at the
semiconductor-oxide interface [13]. These trap charges are formed due to unsaturated fourth bond at the interface originated during the process- [14], stress- [15], and radiation-induced damage [16] in the fabrication process, along with bias temperature instability and hot carrier stress [17]. The term WITC is used to represent the undamaged device (or without ITC) throughout this study. The reliability issues of a conventional TFET have already been reported in [18, 19]. However, there is hardly any published report on DLTFTET for the same. Therefore, in this article, for the first time, to the best of authors’ knowledge, the impact of ITC has been demonstrated by comparative analysis between a Si/Ge HJADGDLTFET and ADGDLTFET. A comparative analysis of DC performance in terms of energy band diagram (EBD), transfer characteristics, electric field, electric potential, and analog/RF performance in terms of transconductance ($g_{m1}$), gate-to-drain capacitance ($C_{gd}$), cut-off frequency ($f_T$), gain-bandwidth product (GBP), and device efficiency (DE).

Additionally, a device must maintain linearity, so that, nonlinear fragments at the output do not interfere with the desired signal [20, 21]. So, the performance parameters such as $g_{m2}$, $g_{m3}$, VIP$_p$, VIP$_n$, IIP$_n$, and third-order intermodulation distortion (IMD$_3$), evaluate the variation in device linearity characteristics due to interfering unwanted noise signals with different frequency components and maintain minimal or negligible higher-order harmonics and IMD at the output [22]. The variation in these performance parameters represents the degree of the device immunity towards ITC.

The organization of the rest of the study is as follows. Section 2 describes the device structure, simulation methodology, and simulation parameters, along with the proposed fabrication process flow of the device. Section 3 describes results and discussions and investigates the DC, analog/RF, and linearity performance parameters of the ADGDLTFET and HJADGDLTFET. In the last, Section 4 concludes the highlights of this work.

2 DEVICE ANALYSIS AND SIMULATION

2.1 Device parameter description

Figure 1(a) and (b) displays the cross-sectional structure of the ADGDLTFET and HJADGDLTFET, respectively. The simulation parameters for ADGDLTFET and HJADGDLTFET [23] are shown in Table 1. In HJADGDLTFET, the WF of the drain electrode is taken to be 4.6 eV to induce electron plasma, and the WF of the source electrode is taken to be 5.93 eV to induce hole plasma on the intrinsic semiconductor body [23, 24]. The WF of the gate electrode is taken to be 4.5 eV. Furthermore, we have used Ge (low bandgap and high mobility material relative to Si) for the source region in HJADGDLTFET to intensify $I_{ON}$. Subsequently, HJADGDLTFET exhibits high $I_{ON}$ while maintaining high $I_{ON}/I_{OFF}$ simultaneously. However, to suppress the enhancement in off-current associated with Ge source, we have used 4.6 eV as the drain electrode WF in HJADGDLTFET [25], instead of 4.4 eV. Additionally, an equivalent oxide thickness (EOT) of 0.37 nm [8] (HfO$_2$, $e = 22$) is provided between the source electrode and the semiconductor body to avoid silicide formation and form large hole plasma [11, 26]. We have the following reasons to do so:

An EOT is the gate oxide thickness of the SiO$_2$ film of a transistor that would be essential to attain comparable capacitance density as the high-$\kappa$ material is used. For device design, EOT can be defined as:

$$EOT = \left(\frac{\epsilon_{SiO_2}}{\epsilon_{high-\kappa}}\right) L_{high-\kappa}$$ (1)

where $\epsilon_{SiO_2}$ denotes the dielectric permittivity of silicon dioxide film, $\epsilon_{high-\kappa}$ signifies the dielectric permittivity of high-\kappa material, and $L_{high-\kappa}$ denotes the thickness of high-\kappa material being used. Additionally, $L_{high-\kappa}$ represents the high-\kappa material physical oxide thickness. The primary advantage of using high-\kappa material as a gate dielectric is that a low EOT can be obtained without decreasing the physical thickness of the gate, thus avoiding the problem of direct tunnelling of carriers through the gate [27] and improvement in tunnelling current. The volume of ITC density (i.e., $N_f$) is carefully selected on the grounds of numerous simulated and experimental available reports, integrating damage due to hot carriers, process, and radiation-induced variations, resulting in the $N_f$ between $10^{11}$ cm$^{-2}$ eV$^{-1}$ and $10^{13}$ cm$^{-2}$ eV$^{-1}$. The $N_f$ depends on annealing and oxidation processes occurring during fabrication. So, by efficient passivation of Si as well as Ge surface and then, atomic layer deposition (ALD) of HfO$_2$[28], $N_f$ at the semiconductor-dielectric interface can be maintained between the range mentioned above i.e., $10^{11} - 10^{13}$ cm$^{-2}$ eV$^{-1}$[29]. Therefore, to investigate the impact of ITC, we have considered the $N_f$ as $10^{12}$ cm$^{-2}$ eV$^{-1}$ for both PITC and NITC [30].

2.2 Simulation methodology

This uses Silvaco ATLAS as the two-dimensional device simulator so that HJADGDLTFET and ADGDLTFET can be simulated effectively [31]. Here, the nonlocal BTBT (BBT. NONLOCAL) model is used to take into account the spatial
deviation of the energy bands, along with the spatial segregation between electrons and holes generated in the conduction band (CB) and valence band (VB), respectively. The tunnelling probability is estimated by Wentzel–Kramer–Brillouin (WKB) method, which uses an electron-hole wave vector across the tunnelling path. The FERMI, NI. FERMI models represent the integration of Fermi–Dirac characteristics so that the induced charge carriers do not exceed the limit of the effective density of states of the substrate material. Additionally, the temperature-dependent and field-dependent variations in mobility are modelled by the Lombardi mobility model (CVT). Furthermore, the concentration-dependent Shockley Read Hall (CONSRH) recombination model has been used to account for the generation and recombination of carriers. Withal, quantum mechanical confinement across the semiconductor-dielectric interface has been modelled by Hansch (HANSCHQM) model. Furthermore, trap-assisted tunnelling (TAT) model accounts for the tunnelling of electrons from the VB to CB through trap or defect states at the high electric field. The INTERFACE statement is used to analyze the density of ITC at the semiconductor-dielectric interface. All the simulation has been performed at $V_G = 1.0\ \text{V}$, $V_D = 1.0\ \text{V}$, and 1 MHz small-signal input frequency.

### 2.3 Fabrication feasibility

The experimental demonstration of CP-based p-n junction [32], dopingless bipolar junction transistor [33], and junctionless TFET [34] has already been reported in the literature. The proposed fabrication process flow of the HJADGDLTFET does not involve ion-implantation and high-temperature annealing process, unlike the metal-oxide-semiconductor field effect transistor (MOSFET). The major fabrication steps using the state-of-the-art process technology for HJADGDLTFET are discussed below schematically.

Initially, high-quality intrinsic Ge film can be grown on intrinsic Si substrate via molecular-beam epitaxy (MBE) [35], Ultra-high vacuum chemical vapor deposition (UHVCVD) [36], or DC magnetron sputtering [37] as shown in Figure 2(a). After that, bottom gate (BG) can be formed independently before the front gate (FG) formation [38]. So, reactive ion etching (RIE) is used to etch the epitaxy and then a high-$\kappa$ gate dielectric layer (HfO$_2$) is deposited by using the ALD technique [39]. Then, patterning and wet etching of bottom side gate oxide in Hf are done, after which, the patterning of the BG region is done using lithography and at last, BG can be formed via the metallization process as shown in Figure 2(b). The same set of procedures as discussed previously is repeated to form FG as shown in Figure 2(c). Additionally, both BG and FG can be aligned using the same alignment marks. Then at last, patterning and etching of the FG oxide is done to form drain and source electrode regions. Subsequently, metallization is done to form source and drain electrodes as shown in Figure 2(d). Thus, we have confidence that HJADGDLTFET will show good experimental results.

### 3 RESULTS AND DISCUSSIONS

#### 3.1 Impact of ITC on DC performance

Figure 3(a) and (b) illustrates the impact of PITC, NITC, and WITC on electron concentration ($|EC|$) and hole concentration ($|HC|$) in the on-state ($V_G = 1\ \text{V}$, $V_D = 1\ \text{V}$), along the horizontal direction for ADGDLTFET and HJADGDLTFET, respectively. It is apparent from Figure 3(a) that the presence of PITC (donor traps) results in the increment in EC, while, the NITC (acceptor traps) reduces the EC at the interface.
Therefore, it is imperative to feature that the EC in the intrinsic region reaches on the order of $10^{19}$ cm$^{-3}$ after the application of an appropriate WF at the gate electrode. Therefore, the carrier concentration is less affected by the presence of ITC in the case of HJADGDLTFET, contrasting with ADGDLTFET.

Figure 4(a) and (b) represents the outcome of NITC, PITC, and WITC on the EBD across the horizontal cutline at 1 nm below the interface. In the on-state, the tunnelling barrier width is reduced as compared to the ADGDLTFET at the source-channel interface, which results in more band bending and consequently higher electron tunnelling from the VB of the source to the CB of the channel.

The leading cause for the reduction in the energy barrier width of HJADGDLTFET is that we have considered a low bandgap material (i.e., Ge with $E_g = 0.7$ eV) and a high-$\kappa$ dielectric (HfO$_2$ having $\varepsilon = 22$), which provides a better coupling between the gate and the channel as compared to SiO$_2$. However, from these EBD, it can be noticed that the variation due to the presence of ITC for the HJADGDLTFET under on-state is very tiny, unlike ADGDLTFET, in which energy bands are shifted more due to low-$\kappa$ dielectric which exhibits more variation and makes the device less reliable.

Figure 5(a) and (b) show the variation due to the presence of NITC, PITC, and WITC on the electric field along the horizontal cutline at 1 nm below the semiconductor–oxide interface for ADGDLTFET and HJADGDLTFET, respectively. The BTBT mechanism in TFETs results in a higher electric field at the source-channel junction as compared to the drain-channel junction.
Therefore, it can be observed from Figure 5 that the PITC (NITC) results in the increased (decreased) electric field. Nevertheless, for HJADGDLTFTET, the usage of HfO$_2$ results in further increment in the electric field at the source-channel tunnelling junction. Moreover, the alterations in the electric field for different ITCs are minimal in the case of HJADGDLTFTET relative to ADGDLTFTET. Figure 6(a) and (b) shows the variation due to the presence of NITC, PITC, and WITC on the electric potential along the X-direction at 1 nm below the interface for ADGDLTFTET and HJADGDLTFTET, respectively. It is detected from Figure 6 that the surface potential is high for a gate with lower metal WF. However, the high potential is required to improve band bending at the source-channel tunnelling junction so that a high drive current can be attained. Additionally, the high metal WF of the drain electrode decreases the surface potential and thus suppresses $I_{OFF}$. Furthermore, the surface potential increases (decreases) due to the impact of PITC (NITC), and this impact is more pronounced in the ADGDLTFTET.

The influence of different types of ITCs on transfer characteristics is illustrated in Figure 7(a) and (b) for ADGDLTFTET and HJADGDLTFTET, respectively, on a logarithmic scale. The presence of PITC (NITC) results in the increment (decrement) of the peak of the electric field resulting in the decrease (increase) in the flat-band voltage caused by the presence of PITC (NITC) [1], defined as:

$$V_{FB} = q \frac{N_f}{C_{OX}}$$  \hspace{1cm} (2)

where $q$ is the electronic charge, $N_f$ is the ITC density, and $C_{OX}$ is the gate oxide capacitance. The presence of PITC (NITC), decreases (increases) the flat-band voltage and, thereby, increases (decreases) the effective gate bias ($V_{eff} = V_{gs} - V_{FB}$) at the tunnelling junction. The enhanced (reduced) $V_{eff}$ is caused by the occurrence of PITC (NITC), thereby, enhancing (reducing) the gate controllability and BTBT at the tunnelling junction. Furthermore, for lower gate voltages, $V_{eff}$ is dominated by $V_{gs}$, resulting in more variation caused by ITC in comparison to high gate voltages [40]. From Figure 7(b), it is clear that HJADGDLTFTET exhibits less variation and stronger immunity against ITC than ADGDLTFTET as high-$\kappa$ dielectric (HfO$_2$) used in HJADGDLTFTET increases the gate capacitance and hence better gate controllability [41]. Furthermore, HJADGDLTFTET displays an improvement in $I_{ON}$ by one order when equated to ADGDLTFTET due to the usage of low bandgap material in the source region and high-$\kappa$ dielectric material. The electrical coupling has been increased between the gate and the source-channel junction due to increased gate capacitance. Therefore, the HJADGDLTFTET obtains an $I_{ON}$ ~1.5 × 10$^{-5}$/µm, $I_{OFF}$ ~1.5 × 10$^{-15}$/µm, and on-to-off ratio ~10$^{10}$ for a drain voltage of $V_{DS} = 1$ V and the gate voltage of $V_{GS} = 1$ V.

### 3.2 Impact of ITC on analog/RF performance

The effect of ITC on transconductance is demonstrated in Figure 8(a) and (b) for ADGDLTFTET and HJADGDLTFTET, respectively. The transconductance ($g_m$) is a critical device criterion for analog applications which convert gate voltage into drain current and govern gain of the device [42] and is stated as:
It is evident from Figure 8 that when PITC (NITC) is introduced at the semiconductor-dielectric, nonlocal BTBT increases (decreases), and hence $g_{m1}$ increases (decreases) for HJADGDLTFET as well as for ADGDLTFET. However, the impact of ITC on $g_{m1}$ for HJADGDLTFET is insignificant because of the introduction of low bandgap material for the source region, an asymmetric double gate structure, and a high-k dielectric.

At high frequencies, parasitic capacitances such as gate-to-drain capacitance ($C_{gd}$) and gate-to-source capacitance ($C_{gs}$) affect device performance dramatically as these capacitances undertake a feedback path among output and input signal; ensuing the parasitic oscillations and hence signal distortion. For TFETs, $C_{gd}$ dominates due to the formation of the inversion layer at the gate dielectric interface in the channel region [43–45] and is expressed as:

$$C_{gd} = \frac{\partial Q_{G}}{\partial V_{D}}$$  \hspace{1cm} (4)

The effect of ITC on gate-to-drain capacitance is illustrated in Figure 9(a) and (b) for ADGDLTFET and HJADGDLTFET, respectively, concerning the gate voltage, which shows that the $C_{gd}$ of HJADGDLTFET and ADGDLTFET is comparable and at high gate voltages, the increment in the density of states and capacitive coupling results in the formation of significant energy barrier at the drain-channel interface.

Furthermore, $C_{gd}$ of HJADGDLTFET is greater than that of ADGDLTFET because of the adoption of HfO$_2$ as gate dielectric and an increase in electron charges caused by heterojunction [46]. As illustrated in Figure 9, $C_{gd}$ increases (decreases) with PITC (NITC).

Moreover, cut-off frequency ($f_T$) is a significant factor of the device in wireless and RF applications. The frequency upon which the short circuit gain approximates to unity is known as cut-off frequency and is specified as:

$$f_T = \frac{g_m}{2 \prod (C_{gd} + C_{gs})}$$  \hspace{1cm} (5)

The effect of ITC on cut-off frequency is shown in Figure 10(a) and (b) for ADGDLTFET and HJADGDLTFET, respectively. It can be shown from Figure 9 that for both devices, as the gate voltage increases, $f_T$ increases due to increment in $g_{m1}$. As illustrated in Figure 10, $f_T$ increases (decreases) with PITC (NITC). However, variation in $f_T$ due to ITCs is less in HJADGDLTFET, unlike ADGDLTFET.

In addition to cut-off frequency, the gain–bandwidth product is also a vital device design parameter for RF applications and provided for a DC gain of 10. It can be articulated as:

$$GBP = \frac{g_m}{20 \prod C_{gd}}$$  \hspace{1cm} (6)

The effect of ITC on the gain–bandwidth product is presented in Figure 11(a) and (b) for ADGDLTFET and HJADGDLTFET, respectively. It is interpreted from Figure 11 that HJADGDLTFET obtains higher GBP in comparison to ADGDLTFET. As gate voltage increases, GBP increases due to substantial growth in $g_{m1}$. It is concluded that higher GBP illustrates a more significant gain as well as bandwidth for.
HJADGDLTFET as compared to ADGDLTFET. Additionally, the graph of GBP trails to the trend of the cut-off frequency graph, and the reason is pronounced from Equation (6).

DE is a vital device design specification for analog devices, together with RF performance. DE can be described as the competence of the device to translate given current into its equivalent transconductance and is expressed as:

$$DE = \frac{g_m}{I_D}$$  \hspace{1cm} (7)

The effect of ITC on DE is shown in Figure 12(a) and (b) for ADGDLTFET and HJADGDLTFET, respectively, outlining that the HJADGDLTFET shows better DE as it depends on transconductance and drain current.

### 3.3 Impact of ITC on linearity performance

Besides high speed, the advanced communication system must provide a surety for minimum signal distortion and linearity to ensure better signal-to-noise ratio and to establish the aptness of the device for analog applications. The transconductances of the device must be constant concerning the applied gate voltage to acquire linearity. However, the transconductances of both MOSFETs and TFETs rely on the input gain voltage, resulting in the nonlinear characteristics [47]. Therefore, we investigate the linearity performance parameters of ADGDLTFET and HJADGDLTFET, where these parameters are stated as:

$$g_{mn} = \frac{1}{n!} \frac{\partial^n I_d}{\partial V^{n}}$$ \hspace{1cm} n = 1, 2, 3… \hspace{1cm} \hspace{1cm} (8)

$$VIP_2 = 4 \times \frac{g_{m1}}{g_{m2}}$$ \hspace{1cm} (9)

$$VIP_3 = \sqrt{24 \times \frac{g_{m1}}{g_{m3}}}$$ \hspace{1cm} (10)

$$IIP_3 = \frac{2}{3} \times \frac{g_{m1}}{g_{m3}} \times R_s$$ \hspace{1cm} (11)

where $R_s = 50 \Omega$ for almost all RF applications

$$IMD_3 = \left(\frac{9}{2} \times (VIP_3)^2 \times g_{m3}\right)^2 \times R_s$$ \hspace{1cm} (12)

where $R_s = 50 \Omega$ for almost all RF applications

The higher-order derivatives of transconductance are the primary reason for nonlinearity and distortion in the device and determine the minimum limit of the distortion. Hence, the amplitude of $g_{m3}$ must be as small as possible, because, in the case of $IMD_3$, it determines the amplitude distortion via adjacent band signals.
TABLE 2 Comparison of device characteristics of ADGDLTFTET and HJADGDLTFTET with different trap charges (calculation of % increase (decrease) of PITC (NITC) is done with respect to WITC at $V_G = 1$ V and $V_D = 1$ V)

| Parameters | ADGDLTFTET | HJADGDLTFTET |
|------------|------------|---------------|
| $I_{ON}$ | 214.14 % ↑ (77.07 % ↓) | 14.80 % ↑ (13.33 % ↓) |
| $g_m$ | 165.50 % ↑ (68.46 % ↓) | 11.14 % ↑ (10.52 % ↓) |
| $C_{gd}$ | 20.73 % ↑ (0.18 % ↓) | 0.13 % ↑ (0.49 % ↓) |
| $f_T$ | 125.25 % ↑ (70.83 % ↓) | 11.62 % ↑ (11.10 % ↓) |
| GBP | 104.93 % ↑ (70.56 % ↓) | 11.53 % ↑ (11.14 % ↓) |
| DE | 21.24 % ↑ (28.18 % ↓) | 2.98 % ↑ (3.03 % ↓) |
| $g_{m2}$ | 150.77 % ↑ (71.69 % ↓) | 6.27 % ↑ (6.56 % ↓) |
| $g_{m3}$ | 12.23 % ↑ (14.39 % ↓) | 11.24 % ↑ (10.86 % ↓) |
| VIP$_3$ | 5.87 % ↑ (11.39 % ↓) | 4.58 % ↑ (4.24 % ↓) |
| VIP$_5$ | 53.81 % ↑ (39.30 % ↓) | 0.05% ↑ (0.19 % ↓) |
| IIP$_3$ | 52.96 % ↑ (61.41 % ↓) | 0.16 % ↑ (0.67 % ↓) |
| IMD$_3$ | 42.86 % ↑ (50.65 % ↓) | 5.25% ↑ (5.53 % ↓) |

smaller gate bias is essential for holding better linearity. It is apparent from Figure 16(a) and (b) that the value of VIP$_3$ increases (decreases) with PITC (NITC). On top of that, the relative amplitude of VIP$_3$ is larger for HJADGDLTFTET. For RF devices, IIP$_3$ is mainly the result of nonlinearity at the fundamental frequency and the frequency difference between two nearby signals. In literature, IIP$_3$ and IMD$_3$ have been studied as an essential linearity parameter [48]. Hence, we have also studied IIP$_3$ and IMD$_3$.

The effect of ITC on IIP$_3$ with respect to the applied gate voltage for ADGDLTFTET and HJADGDLTFTET is illustrated in Figure 17(a) and (b), respectively. It is found that HJADGDLTFTET is immune to the variations in IIP$_3$ and IMD$_3$ characteristics due to the presence of ITC. Nevertheless, the shifting of the peak of IIP$_3$ towards lower gate bias signifies that HJADGDLTFTET can attain better linearity characteristics at a reduced gate voltage. Furthermore, IMD$_3$ denotes the third-order intermodulation distortion, where the power of fundamental and third-order intermodulation components is equal, which must be of low amplitude to achieve better linearity characteristics. Figure 18(a) and (b) illustrates the effect of IMD$_3$ concerning the applied gate voltage with different types of ITC for ADGDLTFTET and HJADGDLTFTET, respectively. Table 2 shows the comparative analysis of various device characteristics for ADGDLTFTET and HJADGDLTFTET.

4 | CONCLUSION

The interface trap charge impacts the reliability of the device. Therefore, an Si/Ge heterojunction DLTFTET with a high-$\kappa$ dielectric and asymmetric double gate has been used to examine the impact of ITC. The HJADGDLTFTET provides
better driving capabilities, which can be used to enhance amplifier gain. Moreover, dopingless TFET based on the charge plasma concept can provide an integrated solution over its counterpart TFET in terms of fabrication steps. So, with the aid of TCAD-based simulation, a comparative analysis is performed between ADGDLTFET and HJADGD/LTFET to investigate the DC, analog/RF, and linear distortion parameters for variations due to different types of ITC. The comparative results illustrate that small variations occur in HJADGD/LTFET, making it more immune to variations caused by ITC. Additionally, the investigation of performance degradation due to the impact of ITC is essential to get an optimized device, as ITC is always present in physical devices.

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