Quantum-mechanical effect in atomically thin MoS₂ FET

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Abstract
Two-dimensional (2D) layered materials-based field-effect transistors (FETs) are promising for ultimate scaled electron device applications because of the improved electrostatics to atomically thin body thickness. However, compared with the typical thickness of ~5 nm for Si-on-insulator (SOI), the advantage of the ultimate thickness limit of monolayer for the device performance has not been fully proved yet, especially for the on-state at the accumulation region. Here, we present much stronger quantum-mechanical effect at the accumulation region based on the C–V analysis for top-gate MoS₂ FETs. The self-consistent calculation elucidated that the electrons are confined in the monolayer thickness, unlike in the triangle potential formed by the electric field for SOI, the gate-channel capacitance is ideally maximized to the gate insulator capacitance since the capacitive contribution of the channel can be neglected due to the negligible channel thickness. This quantum-mechanical effect agreed well with the experimental results. Therefore, monolayer 2D channels are suggested to be used to enhance the on-current as well as the gate modulation ability.

1. Introduction
The metal-oxide-semiconductor field-effect transistor (MOSFET) scaling requires the transition from planar to FinFET to overcome the short channel effect, which prolongs the life of the silicon complimentary MOS [1, 2]. The electrostatics have been improved, while 3-dimensional (3D) shape has drastically increased the parasitic capacitance (Cpara) to the level beyond the intrinsic gate capacitance, which results in the loss of gate controllability [3]. Therefore, it has been suggested that an attractive charge-based device scaling path should be back to 2D from 3D to reduce the parasitism [4].

So far, for the conventional 2D channel, i.e. silicon-on-insulator (SOI) MOSFETs, the electrostatic field-effect control of carriers has already been investigated by deepening the understanding of the bulk Si MOSFET, which is characterized by capacitance–voltage (C–V) measurements [5]. The bulk Si MOSFET usually operates at the inversion mode, and the carriers in the inversion layer are confined by the electrical-field-induced band bending, as shown in figure 1. In the classical simplest model, the carriers are assumed to stay just at the SiO₂/Si interface. The gate-channel capacitance (Cgc) is equal to the oxide capacitance (Cox). However, the electrons are governed by quantum mechanics and described by wave functions. Therefore, the carriers in the electrical-field-induced band bending are quantized into a 2D subband structure, where E₁ and E₂ correspond to the two lowest energy subbands. The distance between the centroid for the square modulus of the wave function and the interface is shown by zinv. Therefore, the additional contribution resulted from this distance in the semiconductor should be considered and called the quantum mechanical effect. This results in 1/Cgc = 1/Cox + 1/Cinv where Cinv is the inversion layer capacitance. For thin-channel SOI MOSFETs (e.g. 5 nm-thick silicon), the quantized carriers are further confined by the channel thickness, which results in the sharper carrier distribution and slightly enhances Cgc [5]. However, the C–V analysis at the atomic thickness limit, which is the case for the 2D layered channels, has not been experimentally demonstrated for the SOI MOSFET, because there is a drastic mobility degradation when the Si thickness decreases from 5 nm to 1 nm [6], and the fabrication of SOI with a uniform thickness of 1 nm is extremely difficult [6, 7].

For atomically thin 2D layered channels, C–V measurements were reported on MoS₂ FETs to analyze the interface state densities [8–15], electrical reliability on...
the gate oxide [16–18], quantum capacitance \((C_Q)\) [8], metal–insulator transition [19] and thickness-dependent depletion behavior [20]. It has been recognized that most of 2D-layered-channel-based FETs operate at the accumulation mode [20]. Therefore, the strong quantum-mechanical effect is expected at the accumulation region, which cannot be achieved in the SOI MOSFET.

In this work, the accumulation region in \(C-V\) for top-gate MoS\(_2\) FETs is systematically analyzed to elucidate the quantum-mechanical effect. In addition, the self-consistent calculation is performed by solving Poisson equation and Schrödinger equation. Finally, based on the comparison of the experimental and theoretical results, the quantum-mechanical effects on \(C_{gc}\) are discussed from the viewpoint of the 2D device thickness scaling.

2. Results and discussion

In this paper, MoS\(_2\) films were mechanically exfoliated onto the quartz substrate from natural bulk MoS\(_2\) flakes. Raman spectroscopy and atomic force microscopy (AFM) were employed to determine the layer number. Ni/Au was deposited as the source/drain electrodes. Then, Y metal with a thickness of 1 nm was deposited via thermal evaporation of the Y metal from a PBN crucible in an Ar atmosphere with a partial pressure of \(10^{-1}\) Pa, followed by oxidization in the laboratory atmosphere [21, 22]. Y\(_2\)O\(_3\) acts as the buffer layer for the nucleation sites on MoS\(_2\) because MoS\(_2\) surface is chemically inert. The Al\(_2\)O\(_3\) oxide layer with a thickness of 10 nm was deposited via atomic layer deposition (ALD), followed by the Al top-gate electrode formation. \(C-V\) measurements were conducted using 4980A LCR meters in a vacuum prober at the room temperature.

Figure 2 shows a schematic drawing and an optical image of the top-gate MoS\(_2\) FET. The MoS\(_2\) flakes with the large area (>30 \(\mu m^2\)) were selected for device fabrication and characterization because the measured capacitance should be larger than the stray capacitance (~10 fF) of the measurement system. Moreover, it should be emphasized that the quartz substrate was used to remove \(C_{par}\) completely [20]. \(C_{gc}\) was measured in the top-gate MoS\(_2\)-FETs, where the top-gate electrode was connected to the high terminal, while both source and drain were connected to the low terminal. The full equivalent circuit of the MoS\(_2\) accumulation region is shown in figure 2(b). \(C_A\) is the accumulation capacitance. \(C_i\) and \(R_i\) are the capacitance and resistance of the interface states, respectively, which account for the carrier capture and emission processes. \(R_{ch}\) is the channel resistance, which accounts for the carrier charging process to the channel through the source/drain. At the depletion region, \(C_i\) is important in the \(C-V\) characteristics because \(C_i\) is much larger than the depletion capacitance, while it can be neglected at the strong accumulation region in this study. \(R_{ch}\) becomes dominant at the depletion region but can be neglected at the strong accumulation region due to the high carrier density. More detailed information on the equivalent circuit can be found elsewhere [8, 20]. Therefore, at the accumulation region, the simplified equivalent circuit with \(C_A\) and \(C_{ox}\) can be considered, as shown in figure 2(c).

Figure 3(a) shows the experimental \(C_{gc}-V_{TG}\) curves for the MoS\(_2\) channel thicknesses \((t_{ch})\) of 1 layer (1L), 3L, and 10 nm at the frequency of 1 MHz. The 1L MoS\(_2\) shows (i) the highest saturation capacitance and (ii) a sharp rise at the accumulation region, while 10 nm MoS\(_2\) shows the lowest saturation capacitance and a slow rise to the accumulation region. Since all devices have identical \(C_{par}\) in principle due to the identical top-gate process, the thickness dependence of \(C_{gc}\) can arise from the contribution of \(C_A\). Here, in the case of the SOI MOSFET, the sharp rise of the capacitance

![Figure 1. Schematic illustration of the subband structures for bulk Si-MOSFET, 5 nm SOI, and monolayer 2D. Red lines indicate square modulus of the wave functions for subbands. Si-MOSFET and SOI operate at the inversion mode, while 2D FET operates at the accumulation mode. Therefore, the distance from the interface to the center of the square modulus of the wave function is expressed as \(z_{inv}\) and \(z_A\), respectively.](image-url)
was observed with the decrease in the thin body thickness [5]. However, the increase in the capacitance at the saturation region was not observed. The drastic increase in capacitance at the saturation region in the present MoS2 FET can be attributed to the giant quantum-mechanical effect at the monolayer limit, which is quite difficult to experimentally achieve by the channel thickness scaling of the SOI MOSFET.

The self-consistent calculation was performed by solving Poisson equation and Schrödinger equation to clarify the quantum-mechanical effect in the MoS2 FET. Figure 3(c) shows the example of the energy band diagram of the top Al2O3 (10 nm)/MoS2 (10 nm)/back Al2O3 (10 nm) gate stack used for the calculation. The gate voltage is always applied to the left Al2O3 oxide, which is used as the top-gate oxide. The right Al2O3 oxide is just considered as the substrate, and the effect of the thickness and oxide type on the calculated results can be ignored here. Schrödinger equation was solved in the effective mass approximation using the software by incorporating material properties specific to the device [23]. The parameters of MoS2 used in the calculation are shown in table 1. The thickness of MoS2 is varied from 1L to 10 nm at different gate biases. For simplicity, the continuous band is used instead of the discrete bands with the van der Waals energy gap. The layer number dependence of the dielectric constant ($\varepsilon_{ch}$) for MoS2 is adapted from the studies of first-principle calculation [24, 25]. This simplification is reasonable, since it provides a sufficient explanation of the experimental results. The calculated $C_{gc}$–$V_{TG}$ curves are shown in figure 3(b). The 1L MoS2 shows a sharp rise and the highest saturation capacitance at the accumulation region, which is consistent with the experimental results.

| Table 1. Physical parameters used in the simulation. |
|-----------------------------------------------|
| Dielectric constant | Effective mass | $N_D$ (cm$^{-3}$) |
|---------------------|----------------|-------------------|
| Monolayer           | 3.0            | 0.73              | $3 \times 10^{17}$ |
| Bilayer             | 4.2            | 0.73              | $3 \times 10^{17}$ |
| Bulk                | 6.3            | 0.73              | $3 \times 10^{17}$ |

Figure 2. (a) Whole image of the devices on a quartz substrate. The inset is the magnified image showing a top-gate MoS2 FET. (b) Schematics of the MoS2 FET structure and full equivalent circuit of the capacitance measurements. (c) Simplified equivalent circuit at the strong accumulation region.

Figure 3. (a) Experimental $C_{gc}$–$V_{TG}$ characteristics at 1 MHz of MoS2 FETs with a thickness of 1L, 3L, and 10 nm. (b) Simulated $C_{gc}$–$V_{TG}$ characteristics of the MoS2 FETs with a thickness of 1L, 2L, 3L, and 10 nm, respectively. The solid lines are the results from the self-consistent calculation by solving Poisson equation and Schrödinger equation [23]. (c) Typical example of the energy band diagram of the top Al2O3 (10 nm)/MoS2 (10 nm)/back Al2O3 (10 nm) gate stack. $E_C$, $E_V$, and $E_F$ are conduction band, valance band edge energies, and Fermi energy, respectively.
Here, the origin for the thickness dependence of \( C_{gc} \) is discussed. Figures 4(a)–(c) show the calculated three lowest subband energies \( (E_1, E_2, E_3) \), square modulus of wave function for each subband, and channel electron density \( (n) \) distribution for 10 nm MoS\(_2\) at the weak depletion. The energy difference between the subbands \( (E_2 - E_1 = 0.017 \text{ eV}) \) is smaller than the \( k_B T \) (\( k_B \) and \( T \) are defined as the Boltzmann constant and the temperature), which makes all of these subbands occupied by the electrons. As a result, \( n \) is distributed throughout the entire channel thickness with a peak near the back surface.

Meanwhile, when the positive gate bias is applied, the strong accumulation is achieved as shown in figures 4(d)–(f). The energy difference between \( E_1 \) and \( E_2 \) increases due to the confinement in the top surface triangle potential formed by the electrical field. As a result, most of electrons locate in the lowest energy subband \( E_1 \), and the wave function of \( E_1 \) is confined in the top surface triangle potential. That is, 2D electron gas (2DEG) is formed near the top surface of MoS\(_2\) with the distance of \( \sim 1.1 \text{ nm} \). Therefore, when the gate bias is modulated from the depletion to the accumulation, the centroid position for the square modulus of the wave function is gradually changed from the bottom to the top of the MoS\(_2\) body, which results in a slow rise of \( C_{gc} \) toward the accumulation region by the gate voltage.

When \( t_{ch} \) is reduced, in addition to the electrical field confinement, the thickness confinement will dominate the quantum-mechanical effect. It is similar to the consideration of a quantum well [26], and the thickness-confined subband energy eigenvalues can be estimated as \( E_n = \hbar^2 \pi^2 n^2 / 2m_{ch} t_{ch}^2 \), where \( m_{ch} \) is the effective mass of MoS\(_2\). By decreasing \( t_{ch} \), the energy difference between \( E_1 \) and \( E_2 \) will be much larger than \( 3k_B T \), and only subband \( E_1 \) can be considered to be occupied. As a result, the intrinsic 2DEG is formed in the ultrathin MoS\(_2\) channel. This is the scenario for 3L to 1L MoS\(_2\), as shown in figures 4(g)–(i). Subband \( E_1 \) is now confined in the MoS\(_2\) body. The electrical-field-induced band bending does not affect the electron distribution because \( E_1 \) is already higher than the triangle potential. The energy difference between \( E_1 \) and \( E_2 \) is quite large, so \( E_2 \) is not visible in figure 4(g). Therefore, when the gate bias is modulated from the depletion to the accumulation, the centroid position for the square modulus of the wave function is almost fixed and results in the effective modulation of \( n \). This scenario accounts for the sharper rise of the \( C_{gc} \)–\( V_{TG} \) curves for 3L to 1L MoS\(_2\). Moreover, in figure 3(b), the positive shift of \( C_{gc} \)–\( V_{TG} \) curves is observed by decreasing \( t_{ch} \). This result is attributed to the increase in the \( E_1 \) subband energy. However, the experimental \( C_{gc} \)–\( V_{TG} \) curves do not show a clear thickness-dependent shift. This is because the threshold voltage for the 2D layered channel is quite sensitive to the surface doping effect due to the extrinsic adsorbates especially for the ultra-thin channel case [27, 28].

The next task is to explain why the saturation capacitance drastically increases at the monolayer...
limit. In analogy to $C_{\text{inv}}$ in SOI MOSFETs, $C_{\text{gc}}$ in MoS$_2$ FETs at the accumulation region can be divided as $1/C_{\text{gc}} = 1/C_{\text{ox}} + 1/C_A = 1/C_{\text{ox}} + 1/C_{\text{DOS}} + 1/C_{\text{thickness}}$ [29, 30]. $C_{\text{DOS}}$ comes from the finite DOS of MoS$_2$ as $C_{\text{DOS}} = e^2 \delta_{2D}[1 + \exp(E_g/2k_B T)/2 \cosh(E_c/k_B T)]$, where $g_{2D} = g_s m_s \pi \hbar^2$ is the band-edge DOS [8, 20, 31]. $E_g$ is the bandgap, and $g_s$ and $g_v$ are the spin and valley degeneracy factors, respectively. $C_{\text{thickness}}$ comes from the distance between the centroid for the square modulus of the wave function and the gate insulator interface ($z_A$) as $C_{\text{thickness}} = \varepsilon_{\text{ch}}/z_A$. At the strong accumulation region, the Fermi energy ($E_F$) enters the conduction band, and $C_{\text{DOS}}$ corresponds to conduction band-edge DOS. MoS$_2$ has a relatively large effective mass, and therefore $C_{\text{DOS}}$ is large with the order of $\sim 80 \mu \text{F cm}^{-2}$ [8]. It is much larger than $C_{\text{ox}}$ (typically $\sim 0.3$–$0.4 \mu \text{F cm}^{-2}$) and can be neglected. As a result, it is simplified as $1/C_{\text{gc}} = 1/C_{\text{ox}} + z_A/\varepsilon_{\text{ch}}$ which indicates that $z_A$ determines $C_{\text{gc}}$. Therefore, the square modulus of the wave function for subband $E_1$ is shown for different MoS$_2$ thicknesses at the strong accumulation region in figure 5(a). In the 10 nm MoS$_2$ case, the centroid of the wave function is confined in the triangle potential induced by band bending instead of its body thickness, and $z_A$ is $\sim 1.1$ nm. By decreasing the MoS$_2$ thickness, the centroid approaches the interface due to the channel body confinement effect. In the monolayer case, $z_A$ is only $\sim 0.2$ nm.

From the above theoretical and experimental results, MoS$_2$ channel thickness seriously affects $z_A$, which further affects $C_A$. The contribution of $C_A$ on $C_{\text{gc}}$ is discussed quantitatively from the viewpoint of thickness scaling as below. Figure 5(b) shows the calculated $C_{\text{gc}}$ as a function of $t_{\text{ch}}$. When the equivalent oxide thickness (EOT) is 7.8 nm, the loss of $C_{\text{gc}}$ is $\sim 8\%$ at the multilayer and $\sim 2\%$ at 1L. For EOT = 1 nm, the loss of $C_{\text{gc}}$ becomes $\sim 20\%$ at the multilayer and only $6\%$ at 1L. This trend has been experimentally confirmed by C–V measurements with more than ten devices, as shown in figure 5(c). Although the variation is relatively large from sample to sample, the monolayer MoS$_2$ saturation capacitance is unambiguously larger than that of the thicker MoS$_2$. The above study indicates that monolayer 2D materials should be selected to maximize the carrier density ($n$) at the accumulation region as well as the gate modulation ability since $n = \int C_{\text{gc}} dV_{\text{TG}}$ and $C_{\text{gc}}$ is largest for monolayer. This is the big advantage of the 2D layered channel compared with SOI because thickness scaling of SOI to the ultimate regime ($\sim 1$ nm) negatively impact the electrical transport properties, i.e. the drastic degradation of the mobility [6, 7]. Of course, monolayer 2D materials also suffer from the interfacial issues, such as the remote phonon scattering from the high-$k$ oxide and Coulomb scattering due to charged impurities. These interfacial issues become more unavoidable because the carriers in the channel are close to the top gate oxide interface and even from the bottom oxide interface [32–34]. However, due to the inherent structural stability resulted from the layered structure provides the relatively high mobility even in the monolayer limit. By improving these interfacial issues, the ideal carrier electrostatics will be achieved by the gate electrical field.

3. Conclusion

In this study, the accumulation region of the $C$–$V$ characteristics was systematically investigated for top-gate MoS$_2$ FETs with the thickness from 1L to 16 nm. A strong quantum–mechanical effect due to the channel thickness confinement was experimentally demonstrated in monolayer MoS$_2$ FETs, which was supported by the self-consistent calculation. At the thickness scaling limit to the monolayer MoS$_2$, $C_{\text{gc}}$ is maximized to be $C_{\text{ox}}$ because $C_A$ can be neglected due to the negligible channel thickness. Therefore, monolayer 2D channels are suggested to be used to enhance the maximum on-current as well as the gate modulation ability.
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