Novel sifting-based solution for multiple-converter synchronization of ultra-fast TIADC systems

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Abstract: Multiple-converter synchronization (MCS) is essential for the reliability of ultra-fast time-interleaved analog-to-digital conversion (UF-TIADC) systems or instruments. In this paper, a novel and versatile solution based on phase-sifting approach is proposed in detail for generalized systems. And then, the instantiation design and test are carried out in a 20GSPS TIADC system consisted of four universal 5GSPS ADCs. The results show that the proposed solution is effective on solving the MCS issue and provides a solid timing foundation for further data processing in UF-TIADC systems. Moreover, it offers a practical reference for the MCS implementation of higher-speed sampling systems or instruments.

Keywords: time-interleaved ADC, multiple-converter synchronization, phase sifting, time interval measurement

Classification: Electronic instrumentation and control

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1 Introduction

Ultra-fast data acquisition systems or instruments have been widely applied in modern electronic systems for waveform observation and information processing on various complex signals. For breaking through the limitations of analog-to-digital converter (ADC) performance and acquiring waveform information of measured signals with higher sampling rate, parallelism based time-interleaved ADC (TIADC) technology has been widely adopted as a very effective and practicable method by improving real-time sampling frequency. In recent years, thanks to the development and perfection of mismatch calibration method of offset, gain, time and frequency-response, this technology has nearly solved the performance inconsistency among multiple converters and improved the overall sampling performance of the system to that of single ADC [1, 2, 3, 4]. With the further increase of sampling frequency, however, synchronous reset operations among multiple converters may cause the random nondeterminacy of phase differences among multiple data synchronous clocks (DCLKs). As a result, the combination of multiple sampled data at a same clock cannot be carried out uniquely and reliably. Furthermore, this phenomenon is extremely obvious for ultra-fast TIADC (UF-TIADC) systems with tens-of-giga Hertz and greatly influences the reliability of these system types [5, 6, 7, 8, 9, 10, 11]. Therefore, such multiple-converter synchronization (MCS) has been significant for the implementation of UF-TIADC systems.

In order to solve the MCS issue, its cause and solution have been illustrated in a lot of literatures since the existence was stated by [5] first. For example, the cause has been analyzed in [6, 7, 8], and several solutions based on master-slave configuration and counting-pulse exchange among multiple components have been proposed; but such solutions need to be supported by special components with these features. Moreover, some solutions based on a new interface standard-
JESD204 are stated in [12, 13, 14]. However, they are only applicable to specific ADC components that support the standard. In [11], the cause is analyzed from the timing of system design, and a general solution based on hardware synchronous reset is proposed. But such solution requires several high-speed logic components and a complicate hardware calibration process. In [9, 10], several post-calibration solutions based on time-to-digital conversion (TDC) are proposed for solving the MCS issue of universal ADCs. But such solutions need a complex process of synchronous calibration, and the possible variation of phase difference among DCLKs may influence reliable synchronization operation of the system clock. It can be concluded that existing MCS solutions cannot meet the requirement for the implementation of reliable UF-TIADC system with universal ADCs, as they require either specific ADCs or complex hardware and calibration process.

Therefore, this paper will focus on discovering a versatile solution for the MCS of UF-TIADC system which features universality, reliability and easy realization. By the further analysis of the post-calibration solution, an improved solution based on phase-sifting method is proposed in detail to be suitable for generalized UF-TIADC systems. To verify its feasibility and reliability, design instantiation and test analysis will be finally carried out in a 20GSPS TIADC system consisted of four universal 5GSPS ADCs.

2 General analysis

TIADC system is a multiple-converter system that adopts several (set as N) ADCs with $f_{SCLK}$ sampling frequency and time-interleaved parallel mode so as to achieve a full sampling frequency of $N \cdot f_{SCLK}$ (set as $f_{FCLK}$), as shown in Fig. 1 [5, 10].

![Fig. 1. Structure diagram of typical UF-TIADC system featuring the MCS](image)

The system contains five parts: sampling clock (SCLK) generator, signal conditioning, analog-to-digital conversion, data receiving and processing, and central controller. However, in order to match the core speed of universal digital signal processor (normally field programmable gate array (FPGA)), the system needs to reduce the transmitting speed of ultra-fast sampled data. The reduction process consists of two parts, namely pre-reduction of transmission and re-reduction of receiving. First of all, ADCs reduce the speed of sampled data and DCLKs ($N$ groups) in advance to meet the receiving speed of FPGA. Then, the FPGA...
further reduces these data speed with corresponding DCLKs to meet its core speed of real-time processing, and generates new core clock (CCLK) by digital clock manager (DCM), which is used to synchronize all sampled data for further data processing and storage.

The key for reliable combination of multiple data groups is that these data shall be synchronized to a same clock with a correct and fixed sequence from multiple clock domains. However, such synchronization cannot be implemented reliably due to the random indeterminate timing caused by the MCS resets of ADCs and DCMs, as shown in Fig. 2.

Because the phase difference of multiple DCLKs and the combination of sampled data groups are closely related, the resets of ADCs and corresponding DCMs in the timing analysis can be regarded as one synchronous reset (set as \( RST_i \), and \( t_{Ri} \) is the active edge). If the time of the speed reduction from SCLK to DCLK is \( M \), there are \( M \) possible sorts of phase difference between the DCLK_1 and DCLK_i (\( i \geq 2 \)), and the corresponding time interval \( P_{ik} \) can be expressed as:

\[
P_{ik} = (i - 1) \cdot T_{SCLK}/N + (k - 1) \cdot T_{SCLK},
\]

\( i, k \in N \) and \( i \in [2, N], \ k \in [1, M]. \) (1)

Fig. 2 shows the timing chart of \( M = 4 \). \( I_{ik} \) denotes the \( k \)-th possible reset interval of the ADC_i. \( t_{SR} \) indicates the instant of SCLK_i rising edge after \( t_{Ri} \). As the resets may be generated randomly in each SCLK domain, multiple combined sorts may occur in the synchronization of multiple sampled data groups or DCLKs. It results that data processing cannot be further carried out reliably. Furthermore, there is a metastable state region \( R_{NOK} \) at each SCLK edge (it would be further led into the uncertainty \( \sigma_{DCLK} \) of each DCLK edge), so the active reset may lay randomly in any valid reset regions before or after it. It means that metastable state region exists in the MCS reset process and increases the complexity of MCS timing analysis.

If hardware-based reset solution is employed, the key for successful MCS is to calibrate and ensure every reset moment in the stable interval in the basis of the component reset timing. With the increase of sampling frequency, however, the stable interval is narrowed tremendously so that hardware realization and calibration process become more complex and difficult. Therefore, post-synchronization solution based on the phase identification is generally applied for the MCS in most of general UF-TIADC systems. For example, as shown in Fig. 1, phase identi-
ification module (PIM) base on TDC is used to measure the phase differences of any two DCLKs and to calibrate the combined sequence of multiple sampled data groups. As a consequence, to lower the complexity and enhance the reliability during the implementation of existing post-synchronization methods, a versatile MCS solution should be further proposed.

3 Post-sifting solution

In this section, a novel MCS solution based on the phase identification and sifting method (PISM) will be proposed in detail.

3.1 Phase identification

The implementation of phase identification on DCLKs is decided by the measuring accuracy of the TDC in the PIM. By further analysis on Eq. (1), its minimum value is $P_{21}$, equaling to $T_{FCLK}$. If this interval is measured directly, the requirement of measuring accuracy $\Delta_{TDC}$ for the TDC is

$$\Delta_{TDC} \leq T_{FCLK} = T_{SCLK}/N.$$  

(2)

For a UF-TIADC system with tens-of-giga Hertz, the accuracy requirement is at tens-of-picosecond level and will be further narrowed down with the increase of sampling frequency. Associated with the timing in Fig. 2, it can be found that the measuring accuracy can be expanded effectively by the corresponding delay $t_{di}$ on each DCLK$_i$ except DCLK$_1$. But the range of such delays shall fall within a $T_{DCLK}$, and every time interval shall be measurable and separable strictly, i.e.,

$$P_{ik} + t_{di} < T_{DCLK}, \quad i, k \in \mathbb{N}, \text{ and } i \in [2, N], \quad k \in [1, M],$$

(3)

where $M$ is the reduced speed multiple of DCLKs from SCLKs. In combination with Eq. (1), it can be converted to

$$t_{di} < \left[M - (i - 1)/N - k + 1\right] \cdot T_{SCLK},$$

$$i, k \in \mathbb{N}, \text{ and } i \in [2, N], \quad k \in [1, M].$$

(4)

Therefore, the optimized time interval for the TDC requirement is

$$\Delta_{TDC} = P_{11} + \sup(t_{di}) = T_{SCLK}, \quad i \in \mathbb{N}, \quad i \in [2, N],$$

(5)

where $\sup(\cdot)$ is the supremum. Compared with Eq. (2), these intervals expand largely the measuring range of TDC and are not changed by the number of applied ADC components. This case decreases the hardware requirement for the TDC circuit and is more feasible for its implementation. However, this method needs to add $(N - 1)$ delayers for the phase adjustment of DCLKs.

In practical engineering, jitter exists at the edge of every DCLK (set the uncertainty as $\sigma_{DCLK}$) and the TDC circuit also has a uncertainty $\sigma_{TDC}$, so total uncertainty $\sigma_{D\Delta}$ of each measuring result shall fall within half of $\sigma_{TDC}$, at least. This indicates the TDC resolution requirement, i.e.,

$$\sigma_{TDC} < \sqrt{T_{SCLK}^2/4 - \sigma_{DCLK}^2 - \sigma_{DCLK}^2},$$

(6)

According to the timings of Fig. 1 and Fig. 2, influence factors of $\sigma_{DCLK}$ include: the uncertainty $\sigma_{SCLK}$ from SCLK generation source, the uncertainty $\sigma_{PT}$ during PCB transmission, the additional uncertainty $\sigma_{CC}$ in ADC, the incoming uncertainty $\sigma_{FC}$
in FPGA conversion, etc. If the source and the conversion of each DCLK are consistent, the uncertainties of their edges are equivalent. Therefore, the total uncertainty of the TDC shall satisfy:

\[
\sigma_{TDC} < \sqrt{T_{SCLK}^2/4 - 2(\sigma_{SS}^2 + \sigma_{PT}^2 + \sigma_{CC}^2 + \sigma_{FC}^2)}.
\]

### 3.2 Measuring circuit

The approach of TDC circuit design is decided by its measuring accuracy and range. For single-chip ADC with the highest sampling frequency in the market [15, 16], its \(f_{SCLK}\) is 2.5 GHz, and \(\sigma_{TDC}\) should be smaller than 400 ps, the measuring range as \(T_{DCLK} = M \cdot T_{SCLK}\) (generally in the range of several nanoseconds). According to the characteristics of high accuracy and small range, time interpolation (TIP) method is adopted for the TDC [17, 18], as shown in Fig. 3.

Fig. 3. Principle of TDC based Phase-identification for the MCS

A fixed-traversing method is adopted that contains two main modules: a controlling module of the reset signals and a PIM of DCLKs. Firstly, the controller outputs \(RST_1\) to reset ADC1 and obtains DCLK1 which is used to generate a CCLK in DCM for the data processing. Secondly, by remaining CCLK constant, the controller outputs \(RST_i\) \((i \geq 2)\) to reset ADC\(i\) in turn and the phase identification on DCLK\(i\) \((i \geq 2)\) with DCLK1 is accomplished in PIM. During the phase identification, multiple delay adjustments in terms of Eq. (4) are executed in DCM to obtain a maximum \(\Delta_{TDC}\). Before the TDC operation, the controller outputs a start signal \(EN_1\) to synchronously get the rising edge (starting phase) of DCLK1 and generate an initial edge \(Q_1\) of expanded pulse. After that, \(Q_1\) is taken as another enabling signal \(EN_2\) to synchronously obtain the rising edges (ending edge \(Q_2\) of expanded pulse) of rest DCLKs after the adjustment. \(Q_1\) and \(Q_2\) are transmitted into a time pulse expanding circuit (TPEC) which returns a pulse \((P_E)\) after the expansion to a high-speed counter for counting. The center controller receives the counting result to decide the consistency with the setting MCS requirement. If the result meets the requirement, the rest resets are carried out in sequence. If not, the reset operation should be repeated till the whole system achieves the MCS.

According to the measuring principle, the TDC result can be expressed as:

\[
\Delta t_i = N_C \cdot T_C/N_E + t_{ad}, \quad i \in \mathbb{N}, \text{ and } i \in [2, N],
\]
where $N_C$ is the counting value of the $i$-th ADC; $T_C$ is the period of the counting clock (e.g., $T_{DCLK}$); $N_E$ is the expanding time of measured pulse, and $t_d$ is the adjusting delay in DCM. Uncertainties in the measuring process mainly include: the DCLK uncertainty $\sigma_{DCLK}$, the $\pm 1$ error of the counting $\sigma_C$, and the jitter of expanding circuit $\sigma_j$. Therefore, the result of a certain TDC can be expressed as

$$
\Delta_{TDC} = \Delta t_i \pm \sigma_{\Delta t} = N_C \cdot T_{DCLK} / N_E + t_d
$$

$$
\pm \sqrt{T_C^2 / N_E^2 + \sigma_C^2 + 2(\sigma_{SS}^2 + \sigma_{PF}^2 + \sigma_{CC}^2 + \sigma_{JE}^2)}, \quad i \in \mathbb{N} \text{ and } i \in [2, N]. \quad (9)
$$

The larger $N_E$ is, the higher the accuracy of TDC is. However, the total measuring time $t_{\text{total}}$ shall satisfy the requirement of system capturing rate $R_S$, i.e.,

$$
t_{\text{total}} = t_{\text{ch}} + N_E \cdot T_{DCLK} + t_p < 1 / R_S; \quad (10)
$$

where, $t_{\text{ch}}$ is the charge-discharge time of TPEC, and $t_p$ is the time for TDC data processing. On the premise of Eq. (10) and the circuit realizability, $N_E$ shall be selected as large as possible within the minimum measuring error. In order to further decrease the uncertainty of measuring result, components with high-speed and low-jitter shall be adopted and the wiring principle of signal integrity shall be followed, so as to decrease $\sigma_j$ and $\sigma_{DCLK}$ as much as possible.

Furthermore, the expanded result for different sorts of pulse width has different deviations, so appropriate linear interval shall be selected to ensure the linearity. According to the analysis of Fig. 6, a fixed time interval ($2T_{DCLK}$) is added for the measured pulse in the TDC circuit to meet the linearity requirement. The principle of circuit implementation described in [19] is adopted in this system.

### 3.3 Sifting approach

To identify the sort of a certain TDC result correctly and rapidly, the system needs to select optimal sifting intervals in the basis of Eq. (7). These intervals have a close relation with the TDC values. Theoretically, the statistical property of these values generally manifests Gaussian distribution, as shown in Fig. 4.

$$
\begin{align*}
\mu_i &\text{ is the mean value of } f_i(t), & \text{and the adjacent interval is } T_{SCLK}. \\
\text{There are overlapping areas between any two adjacent distributions (e.g., } a_1, a_2). \\
\text{If Bayes classification criteria on minimum error probability is adopted and the intersection points (e.g., } t_i, t_{i+1}) \text{ of adjacent functions are taken as the boundary to classify the TDC values, the misclassification probability of each overlapping region is:}
\end{align*}
$$

$$
p_{\text{mis}}(e) = \int_{-\infty}^{t_i} f(t|\Delta t_{i-1})p(\Delta t_{i-1})dt + \int_{t_i}^{+\infty} f(t|\Delta t_i)p(\Delta t_i)dt, \quad (11)
$$

Fig. 4. Distribution and reliable interval selection for the TDC result
where \( i \in \mathbb{N} \), and \( i \in [2, N] \). If the error probability is too small to occur, such method can be considered as a great implementation approach for the phase sifting. On the contrary, the classification intervals shall be narrowed down to lower the error probability as much as possible. The specific approach is to diminish each identification interval by taking each mean value as the center, such as \( r_{i-1}, r_i, r_{i+1} \), as shown in Fig. 4. The error probability in region \( r_i \) is

\[
p_{th}(e) = \int_{p_i - r_i/2}^{p_i + r_i/2} [f(t|\Delta t_{i-1})p(\Delta t_{i-1}) + f(t|\Delta t_{i+1})p(\Delta t_{i+1})]dt,
\]

where \( i \in \mathbb{N} \), and \( i \in [2, N] \). If a maximum error probability of \( pr \) is required by a system, the design value of sifting region can be obtained by the inverse conversion of Eq. (12):

\[
r_i = p^{-1}_{th}(e)|_{e=pr}, \quad i \in \mathbb{N}, \quad \text{and} \quad i \in [2, N].
\]

The regions other than Eq. (13) are classified as unreliable regions (\( R_{NOK} \)). Then the purpose of required error probability can be achieved. In comparison with the intervals of Bayes criteria, the effective intervals of Eq. (13) are narrower, but such intervals can increase the correctness greatly and enhance the MCS reliability.

Therefore, the post-sifting MCS solution can be summarized into three main steps. Firstly, the hardware in the basis of the TDC requirements should be implemented; secondly, the statistical analysis on multiple reset results should be carried out to obtain the distribution characteristics; and then calculate the sifting intervals for reliable identification on the phase type; at last, the reset results are identified repeatedly in sequence till reliable MCS implementation of the whole system.

4 Instantiation and test

To verify the feasibility and reliability of sifting-based solution, its instantiation and test analysis will be carried out in a 20GSPS TIADC system.

4.1 Solution instantiation

The 20GSPS system is a typical multiple-converter UF-TIADC system consisted of four lower-speed ADCs (EV10AQ190A of E2V). The ADC is the latest single-chip converter with the highest sampling frequency (5GSPS) in the market that is consisted of four 1.25GSPS sub-ADC cores. Its \( f_{SCLK} \) is 2.5 GHz and \( f_{DCLK} \) is 625 MHz. During the MCS reset operation, it can complete internal 4-core synchronization by self [15]. For matching the core speed of FPGA, all DCLKs shall execute a speed-reduction with two times by DCM to be converted into CCLK of 312.5 MHz. And a 1:4 demultiplexer in FPGA is adopted for sampled data receiving and conversion. Therefore, the system can be regarded as a TIADC system consisted of eight 2.5GSPS sub-ADCs, and the minimum interval of all SCLKs phase is 50 ps. But the MCS resets can be still regarded as independent operations of four single-chip ADCs, and the speed of DCLKs can be regarded as 312.5 MHz after the speed reduction with 8 times from SCLKs. Therefore, relevant parameters are as follows: \( T_{FCLK} = 50 \) ps, \( T_{SCLK} = 400 \) ps, \( N = 4, M = 8 \).

The design scheme of the sifting-based solution is carried out in terms of the functional block in Fig. 3, as well as the reset operations as per the procedure of
fixed-traversing method. According to the requirement for the phase identification of DCLKs, a maximum time interval of 400 ps required by the TDC circuit is obtained. The delay adjustment of DCLKs in DCM shall be:

$$\max(t_{d,k}) = 400 - 100(i - 1), \quad i = 2, 3, 4.$$  \hspace{1cm} (14)

The TDC uncertainty can be estimated by the characteristic of employed components in the circuit, i.e., $\sigma_{SS} < 1$ ps, $\sigma_{CC} < 1$ ps, $\sigma_{FC} \approx 50$ ps, $\sigma_{PT} \approx 60$ ps. In terms of Eq. (7), $\sigma_{TDC} < 167$ ps. Therefore, the TDC circuit and final complete machine can be completed gradually, as shown in Fig. 5.

\[ Fig. \ 5. \ \text{Complete machine test platform and decomposition analysis of 20GSPS system} \]

The engineering sample and test platform of 20GSPS system is shown at the left of Fig. 5, including a testing oscilloscope, a signal calibrator, a RF signal generator and a fast-edge pulse generator. Decomposition analysis on the circuits is shown on the right. To satisfy the TDC requirements on uniformity and reliability, all DCLKs are transmitted independently to the TDC circuit for the generation and expansion of measured pulse. Expanded pulse is then returned to the FPGA for the counting, and the results are used for the statistical identification of MCS types.

### 4.2 Test analysis

The MCS uncertainty is generated by the indeterminacy of multiple hardware resets. The oscilloscope can be used to test the timing between the resets and DCLKs, and the combined result of multiple sampled data groups can be analyzed by the system software. For detail, see the reference [11].

1. TDC circuit performance

   Performance on the TDC circuit is the most important link in the sifting-based solution. In order to achieve millions of waveform capture rate, $t_{CP} < 10$us is required in terms of Eq. (13). As the sum of $t_{ch}$ and $t_{p}$ is generally less than 1 us in practical system, the TDC circuit shall satisfy $N_E < 2400$ in terms of Eq. (10). Finally, $N_E \approx 1000$ is selected in the system design. Its test results are shown in Fig. 6 and 7.

   According to the preliminary $N_E$, a set of pulses with fixed widths ($T_p = 250i$ ps, $i \in \mathbb{N}$) in the measured range are generated by the pulse generator and input into the TPEC for the circuit test. The scatter distribution of measured values is shown in the left of Fig. 6. The linearity interval of TDC variation by linear fitting can be found in (4.5 ns, 12.5 ns) that is suitable for the measured interval.
For making performance parameters of the TDC circuit more precise, multiple measurements on a fixed width pulse ($2T_{DCLK}$) are carried out to obtain the statistical distribution, as shown in the right of Fig. 6. $N_C$ is the counting result of expanded pulse, and $N_M$ is the times of different values. The distribution is characterized of Normal distribution approximately. After the curve fitting, its estimated expectation is $\hat{\mu} = 2049.2$, the estimated variance $\hat{\sigma}_{TDC}^2 = 7.6$, the corresponding time interval $\Delta t = 6.4$ ns, $\sigma_{\Delta t} = 14.3$ ps, and actual $N_E = 1024.6$. These results meet the requirement of the fixed pulse test, and the resolution satisfies the TDC requirement of Eq. (7) for the system. Therefore, a time width $P_F$ about $2T_{DCLK}$ is inserted into measured pulses of the TDC circuit in advance. Relevant expanding processes of multiple measured pulses are shown in Fig. 7.

Measured pulses are generated from two ADCs with adjacent phases by multiple resets. The left figure shows a set of actual measured pulses having inserted a $P_F$ width in the TPEC, and the right shows the actual pulses after the expansion and before the counting in FPGA. They show 8 width types of measured pulses before and after the expansion respectively ($P_{M_i}$ and $P_{E_i}$, $i = 1, 2, \ldots, 8$), covering both the fixed pulses width ($P_F, P_{FE}$) and the measured pulses width ($P_{MX}, P_{EX}$). Therefore, the counting of expanded pulses can be achieved by taking $T_{DCLK}$ as a counting period, and the statistical distribution is shown in Fig. 8.

Statistical result shows that there are 8 types of the phase difference, and the measured times of every type are equal relatively. If taking the right edge $P_{FE}$ of expanded pulse from $P_F$ as the start, the distances between the start and the estimated mean $\hat{\mu}_i$ are the time interval of $P_{EX_i}$, and $P_{FE} + P_{EX} = P_E$ in Fig. 7.
After estimating the mean and variance of each type, the approach specified in section 3.3 can be adopted to divide the sifting interval and eliminate \(NOK_i\) for reliable sifting of reset types. The variance of every type in the figure is relatively small and the reliable sifting interval between any two types are relatively broad. It means that Eq. (12) has a very small error probability and a very high classification accuracy which ensure a reliable identification of MCS type for the system.

Machine performance analysis

After establishing the statistic model and the sifting interval of the MCS resets, the sifting operation can be completed during the system startup or executed reset. To verify the correctness and reliability of the sifting result, fast-edge pulses and high-frequency signals are input and acquired to be an estimate approach for the possibly MCS-reliable system, whose mismatch of offset, gain and time skew is calibrated reasonably. And two of final test results after a mass of startup and shutdown tests are shown in Fig. 9.

Fig. 9 shows two results of correct combination of sampled data in real time mode (2.5 ns time base, 20GSPS) and interpolation expansion with 25 times (100 ps time base, 500GSPS) in the 20GSPS TIADC system. The test signals are a 2.5 GHz sinusoidal signal and a fast-edge pulse respectively. Signal Noise Ratio (SNR) of sinusoidal signal is 38.71 dB and the rising time of fast-edge pulse is 135 ps. There are not timing errors occurred in the combination of multiple sampled data groups, which implies that an accurate and reliable MCS has been implemented for the system. It lays the foundation for the data processing.
In conclusion, the sifting-based solution lessens immensely the requirement of time interval accuracy by the optimization of phase discrimination. And it obtains a unique and fixed running mode of cross clock domains by the sifting strategy which makes the system high-stability. Compared with the existing solutions, the proposed solution not only is effective and flexible on solving the MCS of major components but also provides a reliable clock running mode for the data processing of general UF-TIADC systems, as shown in Table I.

| Feature/Performance | Solutions |
|---------------------|-----------|
|                     | Customized components [6, 7, 8, 12, 13, 14] | Hardware synchronization reset [11] | Post-calibration solutions [9, 10] | Sifting-based solution |
| Approach            | Specific functions given by manufacturers | Delay calibration on reset operations | Data sequence calibration based on the detection of phase difference | Data sequence sifting based on the detection of phase difference |
| Process             | Defined hardware operations | Circular delay debugging | Single reset detection and data calibration | Multiple reset detections and select specific one |
| Complexity          | General | Difficulty | Easiness | Easiness |
| Stability           | Well | Well | General | Well |
| Synchronous time    | Fast | Fast | Fast | General |
| Applicability       | Less, only for ones featuring specific functions | General, for ones featuring synchronous reset interval | Majority, for ones featuring synchronous reset | Majority, for ones featuring synchronous reset |

5 Conclusion

In UF-TIADC systems or instruments, the MCS issue caused by multiple reset operations has greatly influenced the reliability of sampled data combinations among multiple converters. In this paper, a novel and versatile MCS solution based on the sifting method is proposed in detail for general UF-TIADC systems design. Finally, it is instantiated and verified in a 20GSPS TIADC system consisted of four 5GSPS ADCs. The results show that the sifting-based solution is reliable and effective on the MCS realization of UF-TIADC systems, which lays a solid foundation for the correct combination of multiple sampled data groups. Moreover, it offers a practical reference for the MCS implementation of higher-speed sampling systems or instruments.

Acknowledgments

This work was supported by the National Natural Science Foundation of China (Grant No. 61301263) and the Specialized Research Fund for the Doctoral Program of Higher Education of China (Grant No. 20120185130002).