Counting Cards: Exploiting Weight and Variance Distributions for Robust Compute In-Memory

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Abstract—Compute in-memory (CIM) is a promising technique that minimizes data transport, the primary performance bottleneck and energy cost of most data intensive applications. This has found wide-spread adoption in accelerating neural networks for machine learning applications. Utilizing a crossbar architecture with emerging non-volatile memories (eNVM) such as dense resistive random access memory (RRAM) or phase change random access memory (PCRAM), various forms of neural networks can be implemented to greatly reduce power and increase on chip memory capacity. However, compute in-memory faces its own limitations at both the circuit and the device levels. In this work, we explore the impact of device variation and peripheral circuit design constraints. Furthermore, we propose a new algorithm based on device variance and neural network weight distributions to increase both performance and accuracy for compute-in-memory based designs. We demonstrate a 27% power improvement and 23% performance improvement for low and high variance eNVM, while satisfying a programmable threshold for a target error tolerance, which depends on the application.

I. INTRODUCTION

Modern computing systems are heavily dependent on the capacity and access time of expensive memory banks due to the ever increasing performance gap between main memory and logic. The cost of moving data has become more expensive than operating on it \cite{1}, and thus not only has the memory become the fundamental bottleneck of computing, but both reading and transporting the data has become more expensive than the operation we seek to perform.

Popularization of machine learning and artificial intelligence have further exacerbated the long standing memory bottleneck. To mitigate these problems, solutions have been proposed at both the device and architecture level. To minimize the transport of data, architectures like \cite{1} have proposed reusing data as much as possible. In a different approach designs like \cite{2} interleave compute and memory where data transport only occurs locally. While these techniques yield strong results, they still face the fundamental technological limitations of CMOS. In particular, the large size of the SRAM bitcell ($\approx 100 - 150F^2$) results in limited on-die capacity, which necessitates movement of data from an external DRAM to the on-die SRAM.

Fortunately a new class of emerging non-volatile memory is positioned to minimize data transport by performing compute in-memory. In-memory computing seeks to perform matrix multiplication ($\tilde{y} = W\tilde{x}$) in a crossbar structure in the analog domain using Ohm’s law, exploiting the non-volatile conductance state(s) provided by the non-volatile memory. Using this technique, each weight of the matrix ($W_{ij}$) is programmed as the conductance of a bit-cell and each value of the vector ($\tilde{x}_i$) is converted to a corresponding voltage and applied to the rows of the memory crossbar. The current through each cell is proportional to the product of the programmed conductance ($W_{ij}$) and applied voltage ($\tilde{x}_i$) (Ohm’s Law). By Kirchhoff’s current law (KCL), the resulting currents that are summed along the columns of the crossbar are proportional to the product of the matrix and vector, ($\tilde{y}$). In this procedure, the only data transport required for matrix multiplication is the feature vector ($\tilde{x}$) from memory and result ($\tilde{y}$) to the memory. Therefore, in-memory computing enables in-place computing, thereby eliminating the majority of the data transfer and energy cost of data intensive operations.

Although compute in-memory using the crossbar architecture can greatly reduce data transport, it faces its own limitations at the device and circuit level. At the circuit level, the main bottleneck is the limited number of states the circuit can read simultaneously. To read states from the crossbar, an ADC (analog-to-digital converter) converts the analog current value from a column of the crossbar to a digital value. The speed and precision of this ADC directly limits how fast the array can operate.

At the device level, the fundamental bottleneck is a function of the device-to-device variance and the on-to-off ratio of each cell. These two properties define the number of distinguishable states that can be accurately read from a column of the crossbar. If more states are read than can be accurately distinguished, then errors in the operation will occur following the distribution of the device-to-device variance. Since these errors compromise the accuracy of the operation, the performance can no longer be compared to that of a bit-accurate CMOS implementation. Interestingly, in many data intensive applications, particularly in neural networks, limited amounts of variance can be tolerated.

Modern eNVM technologies such as PCRAM and RRAM suffer considerably from device-to-device variance. State of the art devices \cite{3} have been demonstrated with a resistance standard deviation of 3.5%, on-to-off ratio of $> 10^2$, logic process and voltage compatibility, and high density. That said, analyses focused on solely device variability have revealed that the intrinsic and cell-to-cell variability can results in standard deviation that range from 5 - 50% depending on the write effort and the final stored resistance state \cite{4, 5}. While lower nominal variability has been achieved in limited experimental research, real-world factors such as device drift and degeneration along with limited write-energy budget mean that well-controlled variance is rarely guaranteed and often practically impossible. The latter implies a precision/power trade-off design-space that encourages algorithmic solutions to the variance issue.

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In Figure 1 we demonstrate how, given enough variance, a compute in-memory operation will result in an error. We show three cases: 5%, 10% and 20% variance in the resistance of the memory state. This figure depicts the resultant variance expressed as the cumulative distribution of the computing error, when 7 on-state cells are being read (the maximum allowed by a 3-bit ADC) and when 15 on-state cells are read (the maximum for a 4-bit ADC).

In this work, we identify techniques that can be used at the circuit level to mitigate the device-to-device variance of eNVM. We quantify the relationship between device-to-device variance and the ADC precision and their role on the accuracy and performance of compute in-memory operations. Building upon this, we use hardware-based heuristics and feedback from the compute in-memory array to further improve the accuracy of our algorithm.

For our experiments we break down a typical convolutional neural network (CNN) into matrix multiplication operations that can be performed in a compute-in-memory array. Although we apply our techniques to deep learning, we claim that the techniques we propose can be extended to any compute in-memory application. Our results reveal power and performance improvements over commonly used compute-in-memory techniques. The proposed technique 1.8× (6×) better accuracy on CIFAR-10 inference than the baseline (zero-skipping) techniques. We also demonstrate how to compute the expected error for a given configuration and statistically ensure that an error threshold is satisfied enabling robust and reliable compute in-memory with high variance.

II. BACKGROUND AND MOTIVATION

The compute-in-memory (CIM) systems whose readout may be optimized by the technique presented here compute a fixed-point multiply-accumulate (MAC) operation, that is, they element-wise multiply fixed-point input vectors with weight vectors and sum the products together to produce a scalar output. In order for the bit-depth of the input weight vectors and sum the products together to produce a high-precision result, i.e.

\[ y = \sum_{i=0}^{B_x-1} y_i; y_i = 2^l \sum_{k=1}^{N} x_{ik} w_{jk} (1) \]

where \( x_{ij} \) and \( w_j \) are elements in an input vector and weight vector respectively, \( N \) is the length of these vectors, and \( B_x \) is the bit-depth of the input. Similarly, the required weight-precision \( (B_w) \) may exceed the number of bits that could feasibly be stored in a single memory cell, and so a weight may be distributed across several memory cells. This is shown here assuming \( w_{jk} \) are binary:

\[ y = \sum_{i=0}^{B_x-1} B_{w}-1 \sum_{j=0}^{B_{w}-1} y_{i}; y_{ij} = 2^2a^2 \sum_{k=1}^{N} x_{ik} w_{jk} \] (2)

Note that binary input vector \( \vec{x}_i \) selects a subset of the weights to sum. This captures the concept of zero-skipping. This can be rewritten as:

\[ y_{ij} = 2^2a^2 \sum_{k=1}^{N} x_{ik} \land w_{jk} = 2^2a^2 \sum_{w_{jk} \in W_{jk}} w_{jk} \] (3)

\[ W_{jk} = \{ w_{jk} | x_{ik} = 1 \} \] (4)

Hereafter, the collection of weight bits \( w_{jk} \) that are used to compute \( y_{ij} \) for some \( \vec{x}_i \) will be referred to as a column.

The error due to the resistance variation in the memory cell is modeled as:

\[ \epsilon_{ijk} \sim \mathcal{N}(0, w_{jk} \sigma_e^2) \] (5)

where \( \sigma_e^2 \) is the on-state cell variance normalized to the on-state resistance. The cell on/off ratio is assumed large enough that the off-state variance can be ignored. To manage the on/off ratio and to stay within the hardware limitations imposed by the finite ADC bit-depth and the limited bitline (BL) current handling, we adhere to a scheme where the weights in \( W_{jk} \) are broken into groups \( G_i \) of size \( N_r \). Rerphrasing, the current-summing operation of the many bits in a column is broken into a series of ADC reads. \( G_i \) are unique for each \( x, i, j \) with these additional subscripts omitted for readability. The intermediate result due to the sum of all of these groups in a column is:

\[ y_{ij} = 2^2a^2 \sum_{l} \sum_{b_{w_{jk} \in G_i}} (w_{jk} + \epsilon_{jk}) \] (6)

The group-error per \( G_i \) may be written:

\[ \epsilon_l \sim \mathcal{N}(0, S_l \sigma_e^2) \] (7)

where \( S_l \) is the unknown number of on-state weights in group \( l \). Representing the rounding performed by the ADC as \( a(x) \), the total column-error seen at \( y_{ij} \) is then:

\[ \epsilon_{ij} = 2^2a^2 \sum_{l} a(\epsilon_l) \] (8)

The qualitative goal of the algorithm to be presented may now be stated as, a technique that should select the largest possible \( N_r \), to maximize throughput and energy-efficiency, without introducing more errors than the application can tolerate (target error-rate). From equation [7] predicting this column error requires an estimate of the \( S_l \) for each group. To motivate a strategy for approximating the distribution of
When $N_r \leq N_{ADC}$, the error may be expected to have approximately zero mean assuming a symmetrical distribution of memory cell error. Under the operating regime where $N_r > N_{ADC}$ such that the ADC saturates at its maximum value ($= N_{ADC}$) when $S_i \geq N_{ADC}$, the error is expected to have a negative mean which must be cancelled (e.g. digitally) to avoid a systemic offset.

### III. Dynamic Readout Algorithm

With the model as presented above, it is possible to estimate the mean and standard deviation of the error contributed by a single $y_{ij}$ to the final MAC output. This also motivates us to tune $N_r$, given some knowledge about $p_{ijx}$. $p_{ijx}$ is the true probability of a single weight corresponding to bit $i$ in the set $W_{jx}$ being 1, and it cannot be accurately predicted at compile-time because it depends on the output of the dot product being computed. As a consequence, the proposed readout algorithm includes two components: (1) a compile-time step prepares a table of optimized $N_r$ selections for each $(i, j)$ using a worst-case estimate of $p_{ijx}$ and (2) a run-time step uses a more accurate estimate of $p_{ijx}$ to correct the offset wherever $N_r$ exceeds $N_{ADC}$.

In the context of realistic arrays, the proposed algorithm is able to control $N_r$ with limited granularity: a distinct $N_r$ may be selected for each set of columns in a CIM array that share the same WLs and for each input pulse. The makeup of these sets represents a design decision about where to place the weights. In typical vector-matrix multiplications, many weight vectors are dot-multiplied with the same input vector. For the remainder of this analysis it will be assumed that weight bits from separate weight vectors from the same matrix multiplication with the same binary weighting are placed in adjacent columns in the same array (to use the subscript notation introduced in section II). This simplifies the analysis and allows the readout algorithm to function optimally, since the binary weighting of bits has a dominant effect on the impact of their contributed error.

In step (1): Compile Time Procedure, a maximum $N_r$ value is chosen at compile-time for each group of columns that physically share the same wordlines (WLs) in the CIM array. $N_r$ is constrained by the accuracy required by the application, which dictates both the maximum allowed variance and the maximum residual output offset due to bias in the mean error that cannot be fully compensated at runtime. Compile-time here refers to the comparatively slow process that occurs prior to the use of the array with real data during which fixed weights are programmed into the array memory.

The first task when considering a group of columns whose $N_r$ must be optimized is to set $p_{ijx}$ to the worst-case anticipated value. Without claiming to be optimal this work proposes computing the fraction of weight bits set to 1 for each of the columns that will be controlled by this choice of $N_r$, and taking the maximum. The worst-case anticipated $\sigma_{ij}$ may then be computed using the intensive equation [13] for each choice of $N_r$. Since this step occurs at compile-time, the computational cost of the nested sums involved in computing $\sigma_{ij}$ is not a concern. Proceeding from here, $N_r$ is iteratively reduced until the application-specific constraint on the error standard deviation is achieved. A second component then verifies that the potential offset...
due to miscalculated mean error at runtime satisfies the requirements of the application. The details of this second component will be introduced after discussing step (2).

If the chosen application is expected to have approximately equal sensitivity to error in each of the vector dot-product operations comprising the vector-matrix multiplication, the weighting of the contribution to overall error due to a single column becomes $2^c$. That is, the bit-position in the input vector and the bit-position in the weight vector corresponding to the operation being computed in the column determine the choice of $N_r$.

This work proposes constructing a lookup table (LUT) at compile-time with length $B_x \times B_c$. This LUT indicates to the CIM array the correct runtime choice of $N_r$ based on the bit-positions of the current input pulse and of columns in the group. As indicated by equation (10), the CIM unit is instructed to operate slowest, with lowest $N_r$, when operating on the most significant input and weight bits and vice-versa. A pair of representative tables is shown in [2]. LUT table formatting is implementation-specific: if the anticipated worst-case $p_{ijx}$ varies significantly between arrays storing weight bits in the same bit-position for different weights vectors, as may be the case for more-significant bits, separate tables may be constructed for these arrays as is feasible given the hardware constraints. In a realistic hardware implementation, smaller LUTs with length $B_x$ may be placed at each CIM array within which columns can share WLS.

Step (2) is a runtime operation that employs a simplified method to estimate the mean error to be subtracted to center the error distribution around zero. This occurs once the total accumulated value, after all of the ADC reads in a column is computed. While a worst-case estimate of $p_{ijx}$ is appropriate for step (1), which is a compile-time step concerned with constraining the predicted error, such an overestimate could lead to an overzealous error correction that fails to reduce systemic bias.

Recall that correction is only necessary for cases where $N_r > N_{ADC}$. A proposed heuristic for computing offset leverages the fact that not only can $p_{ijx}$ be accurately computed at runtime, since both the number of reads and the final accumulated value for the column are known, but the number of times the ADC saturated at its maximum value is also known. This technique estimates expected value of error (per-ADC-read) given that the ADC reached its maximum output value as:

$$\hat{E}_r(\mu_c) = \frac{1}{C_n} \times \sum_{s=N_{ADC}}^{N_r} B(s, N_r, \hat{p}_{ijx}) \times (N_{ADC} - s)$$

(14)

$$C_n = \sum_{s=N_{ADC}}^{N_r} B(s, N_r, \hat{p}_{ijx})$$

(15)

where $\hat{p}_{ijx}$ is computed as:

$$\sum_{w_{jk} \in W_{jk}} w_{jk} / |W_{jk}|$$

(16)

The numerator of equation [14] is available as the accumulated total for the column under consideration, and the denominator is the product of $N_r$ and the total number of reads used for that column. The mean estimate provided by equation [14] is then multiplied by $N_{sat}$, the number of saturated ADC reads in the column, to yield the total offset:

$$\hat{E}_r(\mu_c) = N_{sat} \times \hat{E}_r(\mu_c)$$

(17)

This remains costly to compute in hardware. If the number of reads in a single column does not suffice to amortize the cost of this correction calculation, the results of equation [14] may be instead stored in a lookup table (LUT) indexed by $p_{ijx}$ sampled with the frequency allowed by the hardware constraints on lookup table size. The LUT approach is facilitated by the fact that tables may be shared across multiple CIM units, and that the only runtime parameter that influences $\hat{E}_r(\mu_c)$ as computed using equation [14] is $\hat{p}_{ijx}$.

Revisiting the compile-time portion of the technique, the second component of step (1) ensures that, if $N_r > N_{ADC}$, the associated offset in the mean can be adequately corrected at runtime. This is done by evaluating the maximum difference between the mean error as computed using equation [11] and the mean error as computed using equation [14] or as retrieved in the lookup table, e.g. as follows:

$$\delta_\mu = \frac{N_r}{N_r} \times |E_{p_{ijx}}[\mu] - P_{sat} \hat{E}_r(p_{ijx} + \delta_p)[\mu]|$$

(18)

$$\delta_p = \frac{E_{p_{ijx}}[\mu]}{N_r}$$

(19)

$$P_{sat} = \sum_{s=N_{ADC}}^{N_r} B(s, N_r, \hat{p}_{ijx})$$

(20)

Here, $E_{p_{ijx}}[\mu]$ is the estimated mean error computed using equation [11] for the largest anticipated $\hat{p}_{ijx}$, whereas $\hat{E}_r(p_{ijx} + \delta_p)[\mu]$ is the mean offset that would be corrected during step (2) for this $N_r$ with $\hat{p}_{ijx}$ miscalculated by $\delta_p$. The result of equation [19] is expected to be negative for $N_r > N_{ADC}$, meaning this method anticipates that the offset for step (2) will be calculated with the worst-possible underestimate of $p$.

IV. CIRCUIT AND ARCHITECTURE CO-DESIGN

In the design of compute in-memory accelerators, there are several abstraction levels to consider. In [6], [7], a compute in-memory array serves as a processing element (PE) similar to how traditional CMOS accelerators implement processing elements with ALUs and SRAM. From this PE, they design an architecture, tiling them into cores. These

![Fig. 2. Example lookup tables for a higher-variance ($\sigma_r = 0.15$) device in (a) and lower-variance ($\sigma_r = 0.05$) device in (b). Both tables demonstrate how the algorithm adjusts $N_r$ based on the X- and W- bit weights. A lower minimal $N_r$ is automatically selected for the higher-variance versus the lower-variance case in order to preserve accuracy with less accurate cells, while the same maximum $N_r$ is selected for the less-significant bits. Computed with $B_x = B_w = 8$, $N_{ADC} = 8$ (3-bit flash) and $N_r \in \{1, 16\}$](image-url)
cores are again, used as building blocks in the larger picture of the design. We further illustrate this idea in figure 3.

Traditional digital accelerators [1] utilize arrays of PEs to perform multiply-and-accumulate operations and accumulate partial sums. For each operation, input and weight data are read in through cache or main memory. Due to the low density SRAM caches that are used, data reuse is key to minimize the number of main memory accesses performed. As a result, many data flow architectures have been proposed that maximize both spatial and temporal reuse and consequently, minimize data transport. Despite these efforts, data transport still consumes a large fraction of the total energy consumption.

Compute in-memory offers an elegant solution to this problem with high density, non-volatile memory that performs the MAC operation using the physical properties of the cell and crossbar. The challenge compute in-memory faces is not with weight transport, but rather with weight placement. To maximize throughput, weights must be distributed in a way that allows each CIM PE to be operating at all times to maximize throughput. One example of an optimal weight mapping and data flow was demonstrated in [8]. Using redundant weights and clever mapping strategies, they maximize throughput of a large scale compute in-memory accelerator.

In this work, we use similar mapping strategies to maximize throughput, with an additional consideration as introduced in section III. In order to best optimize the choice of how many cells to read at once (and therefore how quickly and efficiently the read is completed, at the cost of accuracy) weight bits with the same binary weighting should be grouped together in arrays that share WLs. This is of course under the constraint that the weight vectors these bits belong to must be columns in the same matrix, as they will share activations.

A. Peripheral Circuit Design

Peripheral circuits are a core component of CIM systems: they translate device properties into computing performance. These circuits, the WL drivers and ADCs, must attempt to match the precision available due to the memory array while achieving maximum operating speed and staying within design power constraints. A completely analog approach uses digital-to-analog converters (DACs) to drive the WLs with greater than one bit of precision, accumulates a result in the analog domain, then uses an analog-to-digital converter (ADC) to return the result to the digital domain for further processing.

Analysis of the structure of modern emerging nonvolatile memory arrays such as [3] reveals why alternative, mixed-signal approaches to CIM may be more realistic than this purely analog approach. The access device that inputs data vectors to the matrix of weights stored in the array is in the most traditional case a transistor. Using a multiple-bit DAC to drive the WLs implies significant transistor and memory-cell matching requirements across the array. This burden is avoided by using a low-precision WL driver, as has been recognized in prior work, and for the analysis here we select a one-bit buffer [7]. On the other hand, the precision of the ADC is determined by the maximum number of on-state cells that can be read at once. Trivially, as these cells contribute current, the standard deviation (std.) of the total current scales by the square root of the number of on-state cells. In this work we consider 3-bit ADCs, as a compromise between throughput and design complexity. However, it should be noted that the proposed technologies can be applied to similar other designs.

V. Results

To benchmark our algorithm, counting cards, we compare against the two commonly used techniques. The first technique, we call baseline, is simply reading as many rows as the ADC precision allows (e.g. for a 3-bit ADC, we read 8 rows simultaneously). The next technique we call zero skipping, only reads rows with the 1s (skipping zeros). Zero skipping performs faster than the baseline technique because for most cases it will process more total rows per cycle. We empirically evaluate power, performance, and area for the three techniques using a prototypical CNN described in Table 1 on the CIFAR10 dataset. We run these techniques in a custom simulation framework designed to evaluate power and performance of compute in-memory. This framework is based in Python, but runs array level operations in C for faster evaluation. All code and results for this framework is available under: [repository link to be published in final paper]. We break all 8-bit matrix multiplication operations performed into binary matrix multiplications by the process described in Section IV.

Using our simulation framework we collect results for energy, performance, and accuracy (both at the MAC level as well as the algorithm level). To estimate energy we use parameters provided in [8]. Performance is measured as MAC per cycle. Energy consumption is measured as TMAC per watt. Given that neural networks have tolerance to erroneous operations, we evaluate both matrix multipli-
Fig. 5. Power, performance, and accuracy results for our 7 layer CNN on CIFAR10. (A) Mean square error vs device-to-device variance. We used a fixed target threshold of 0.5 for counting cards which is satisfied for all variance. Both baseline and zero skipping increase linearly with respect to variance. (B) Classification Accuracy vs device-to-device variance. Retains classification accuracy with increasing variance while both baseline and zero skipping diverge. (C) MAC/cycle vs device-to-device variance. Counting cards performance decreases to account for increasing variance, while both baseline and zero skipping remain fixed. (D) TMAC/W vs device-to-device variance. Counting cards efficiency remains fixed with variance since it lowers ADC precision. Both baseline and zero-skipping remain fixed as nothing changes in operation.

TABLE I

| Layer # | Type    | Input Size | Kernel Size | #MAC     |
|---------|---------|------------|-------------|----------|
| 1       | Conv    | (32,32,3)  | (3,3,64)    | 1769472  |
| 2       | Conv    | (32,32,64)| (3,3,64)    | 37748736 |
| 3       | Conv    | (16,16,64)| (3,3,128)   | 18874368 |
| 4       | Conv    | (16,16,128)| (3,3,128)   | 37748736 |
| 5       | Conv    | (8,8,128) | (3,3,256)   | 18874368 |
| 6       | Conv    | (8,8,256) | (3,3,256)   | 37748736 |
| 7       | FC      | 256        | (256,10)    | 2560     |

In this paper we demonstrate the efficacy of a novel compute in-memory algorithm, counting cards, as a dynamic readout technique using statistics based on both the device-to-device variance of eNVM cells and the distribution of weights in the matrix multiplication operation. This algorithm appears as a special case of a broader technique of scaling the readout rate of the bit-cells based on the importance of the data in the overall computation.
Furthermore, we use dynamic hardware heuristics to further increase the accuracy of the proposed algorithm to limit the impact of cell-to-cell variance. The proposed technique 1.8× (6×) better accuracy on CIFAR-10 inference than the baseline (zero-skipping) techniques.

VII. ACKNOWLEDGEMENT

This work was funded by the U.S. Department of Defenses Multidisciplinary University Research Initiatives (MURI) Program under grant number FOA: N00014-16-R-FO05 and the Semiconductor Research Corporation under the Center for Brain Inspired Computing (C-BRIC).

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