Sustainable AI Processing at the Edge

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Abstract

Edge computing is a popular target for accelerating machine learning algorithms supporting mobile devices without requiring the communication latencies to handle them in the cloud. Edge deployments of machine learning primarily consider traditional concerns such as SWaP constraints (Size, Weight, and Power) for their installations. However, such metrics are not entirely sufficient to consider environmental impacts from computing given the significant contributions from embodied energy and carbon. In this paper we explore the tradeoffs of convolutional neural network acceleration engines for both inference and online training. In particular, we explore the use of processing-in-memory (PIM) approaches, mobile GPU accelerators, and recently released FPGAs, and compare them with novel Racetrack memory PIM. Replacing PIM-enabled DDR3 with Racetrack memory PIM can recover its embodied energy as quickly as 1 year. For high activity ratios, mobile GPUs can be more sustainable but have higher embodied energy to overcome compared to PIM-enabled Racetrack memory.

Introduction

Deep neural networks have become a popular algorithm for a variety of applications using mobile devices including smart phones but also recently expanding to connected and autonomous vehicles (CAVs), robotics, or even unmanned aerial vehicles (UAVs), and other smart infrastructure. Convolutional Neural Networks (CNNs) have been demonstrated to provide solutions to these problems with relatively high accuracy. While there have been many proposals to improve the performance and energy efficiency of CNN inference, these algorithms are too compute and data intensive to execute directly on mobile nodes typically operating with limited computational and energy capabilities. Thus, edge servers, now being deployed often in conjunction with advanced (e.g., 5G) wireless networks, have become a popular target to accelerate CNN inference. Moreover, due to their deployment in the field, edge servers must operate under size, weight, and power (SWaP) constraints, while serving many concurrent requests from mobile clients. Thus, to accelerate CNNs, these edge servers often use energy-efficient accelerators, reduced precision, or both to achieve fast response time while balancing requests from multiple clients and maintaining a low operational energy cost. Recently, there has been a trend to push online training to edge server nodes to avoid communicating large datasets from edge to cloud servers [1]. However, online training typically requires much higher precision and floating-point computation compared to inference.

Unfortunately, the proliferation of computing, both the mobile devices, and the edge servers themselves, can come at the expense of negative environmental impacts. Broadly, there are many
concerns from computing infrastructure that range from the use of scarce rare earth elements to environmental costs from extracting materials for manufacturing integrated circuits and energy storage (i.e., batteries). Furthermore, computing infrastructure can lead to problematic emissions of everything from carcinogens to volatile organic compounds, not to mention greenhouse warming gases (GWG), particularly CO$_2$, but also including methane and others. As such, there is a significant and growing aspect of environmental impacts that come from embodied impacts of computing. Embodied impacts include the energy, carbon emissions, etc. from manufacturing computing infrastructure and particularly the semiconductor elements that form the heart of all computing systems. Recent evidence shows that for cloud servers, embodied impacts are equally as high as operational (runtime) effects [2]. For mobile devices and compact computers, embodied impacts can reach 80-90% of total life-cycle impacts and that these impacts are dominated by their integrated circuits [2–4]. Thus, for SWaP optimized systems, embodied energy is a higher proportion of the energy footprint making its amortization an important goal.

While specialty processing units including field-programmable gate arrays (FPGAs) and graphics-processing units (GPUs) can accelerate CNN applications while meeting low operational energy constraints, they come at the cost of increasing the silicon area of these edge systems. This creates a significant tradeoff between embodied energy from including accelerators and the operational energy impacts from executing the algorithms.

In this paper we explore our recently proposed processing-using-memory proposal of Racetrack memory (RM) to implement both CNN inference and training and compare the results with state-of-the-art proposals using GPU, FPGA, and PIM using DRAM. Our comparison considers the main two phases of energy consumption of embodied and operational energy [3]. Thus, we explore its total energy efficiency compare to other state-of-the-art technique to implement modern applications. This allows a evaluation of the sustainability of the system choices. We select energy as our metric as it bridges the manufacturing and operational phase of the system into a metric that can be directly compared. However, we will also discuss how these energy values inform other environmental metrics including GWG when including electrical grid mix profiles.

In particular, this paper makes the following contributions:

- We provide estimates of the embodied energy to fabricate PIM-enabled domain wall memory and recent GPU and FPGA comparison points.
- We characterize the operational power and performance of representative CNN applications for edge-scale execution including both inference and training.
- We conduct indifference and brake-even analyses of different target systems and usage scenarios to determine holistic sustainability calculations.
- We explore the environmental impacts of these systems.

In the next section we discuss the background and related work to conduct these analyses.

**Background**

The primary source of environmental impacts for computing systems comes from the integrated circuits that implement the core functionality of processing, data storage, etc [3]. To determine the holistic environmental impacts in terms of energy, GWG, and other concerns of a product or process, such as semiconductor fabrication, typically involves a technique called Life Cycle Assessment (LCA) [5]. LCA is most accurate when a detailed analysis of the process is used to determine the
assessment, but sometimes relative costs to similar processes can be used as a coarse-grain assessment called economic input/output (EIO) LCA. Relatively few process LCAs have been undertaken of semiconductor fabrication. One assessment considered CMOS, Flash, and DRAM fabrication covering technologies from 350 nm down to 32 nm [6]. Hybrid LCA used used process technology trends and EIO LCA to create a model scaling to 7 nm [4]. Recently, a similar effort with additional process information was used to estimate technologies from 28 nm to 3 nm [7]. This study includes a detailed analysis of the impact of moving from deep-ultraviolet (DUV) lithography to extreme ultraviolet (EUV), which relieves aggressive multiple patterning requirements for sub 30 nm features.

**Indifference and Break-even analyses**

One motivation to use a single metric of energy for both manufacturing and operational sustainability evaluation of the system is to allow quantitative comparison metrics such as indifference and break-even analyses. To compare two design choices to select the appropriate system for deployment we can use the indifference formula $t_I$ as shown in Eq. 1 [8]. For a system with higher embodied energy ($M$) and lower operational energy ($P$), $t_I$ is the time at which the increase in embodied energy will be completely amortized by the savings in operational energy. Thus, if the proposed service time $t < t_I$ the architecture with the lower embodied energy minimizes environmental impact. In contrast, for a proposed service time $t > t_I$ the architecture with the lower operational energy minimizes impact. If one choice is lower in both embodied and operational energy, then indifference analysis is not needed and the lower energy system can be selected independent of service time. A similar calculation can be considered for the break even time $t_B$, also defined in Eq. 1 [8]. Consider the case that an existing system is already deployed. Replacing the existing system is like assuming embodied energy of the deployed system is 0. Thus, $t_B$ is the time it takes for the replacement system to overcome the embodied energy of the replacement through operational energy savings. $t_B = t_I$ when $M_0 = 0$.

$$t_I = \frac{M_1 - M_0}{P_0 - P_1}$$

$$t_B = \frac{M_1}{P_0 - P_1}$$

While we characterize several accelerators in this work for CNN acceleration, we also consider an exotic technology that uses spintronics to store data and has been explored for PIM called Racetrack memory [9]. We provide some background on RM in the next section.

**Racetrack Memory**

Spintronic RM is made of ferromagnetic nanowires consisting of many magnetic domains separated by domain walls (DWs) as shown in Fig. 1. Each domain has its own magnetization direction such that binary values are represented by the magnetization direction of each domain, either parallel/antiparallel to a fixed reference. For a planar nanowire, several domains share one/few access point(s) (APs) for read and write operations [10]. RM is similar to and has many of the same advantages as STT-MRAM, including high endurance, fast access time, low energy, particularly static.
energy due to the device’s non-volatility. RM can have a density \( \leq 2F^2 \) because it can store multiple bits in a nanowire accessed using one transistor. In contrast, STT-MRAM requires 6-50F^2. Hence, RM has been proposed at several memory levels, from L1 cache to main memory. RM achieves this density by requiring shifting if data is not aligned with the access point. Shifting occurs through DW motion in the nanowire. DW motion is controlled by applying a short current pulse laterally along the nanowire governed by SL. Random access requires shifting the target domain to align it with an AP (dark blue) and apply a current to read or write the target bit. To avoid data loss when shifting, the blue domains store actual data while the grey domains are overhead domains to prevent data loss. Shift-based writing (Read/Write Port) [11] allows slower current writes to be replaced with orthogonal shifts from fixed magnetic alignment domains to reduce latency and energy.

RM, like many other novel memories including resistive memory PIM crossbars in PRIME, has also received significant attention for PIM, particularly for deep learning [12,13].

**Convolutional Neural Networks**

CNNs are a popular method to compute deep learning algorithms. CNNs are dominated by the convolution operation, which is a windowed point-wise multiplication accumulation of multiple channels of input features with a set of weights to generate output features. As an example, for the input features \( \mathbf{I} \) and weights \( \mathbf{K} \) of size \( N \times R_{in} \times C_{in} \) and \( M \times N \times 3 \times 3 \), respectively, the convolution operation for the window at \( m \) (output channel index), \( r \) (row), \( c \) (column) is:

\[
\text{Conv}(\mathbf{I}, \mathbf{K})(m, r, c) = \sum_{n=0}^{N-1} \sum_{j=0}^{2} \sum_{t=0}^{2} K_{m,n,j,t} \times I_{n,r+j,c+t}
\]

where \( M \) is the number of output channels, \( N \) is the number of input channels, \( R_{in} \times C_{in} \) is the size of an input feature map.

While deep learning with CNNs presumes calculations with floating-point values, CNN inference calculations can often be reduced to integer computation with as few as 8-bits achieving reasonable accuracy. Recent DRAM PIM work has shown that in many cases this can be further reduced to ternary \( w \in \{-1, 0, 1\} \) or even binary \( w \in \{0, 1\} \) computations operations to replace the multiplications. However, online training for all but the simplest CNNs still requires full 32-bit floating-point computations to work properly. Without this accuracy, the weight updates can be ineffective and possibly even detrimental.

In the next section we explore embodied energy calculations of a variety of accelerators suitable for CNN acceleration.

**Evaluation of Edge Acceleration Sustainability**

To consider holistic energy across embodied and operational phases requires LCA of the semiconductor fabrication process. In the next section we discuss how to obtain embodied energy and carbon footprint.

**Determining Embodied Energy and Carbon**

RM, like STT-MRAM, is a spintronic memory that can be implemented by adding additional layers of ferromagnetic materials and insulators on top of the completed CMOS layers. Typically these are added between the lower levels of the metal stack. The spintronic devices are composed of three conceptual layers, a fixed magnetic layer, an MgO barrier that separates the fixed layer from the free layer often made out of a ferromagnetic material like a CoFeB nanowire. CoFeB with different
doping properties can also be used for fixed magnetic layers. In terms of the process steps, they are essentially the same between STT-MRAM and RM. Thus, during manufacture, in addition to the CMOS and metal layers, three additional mask layers are required due to the different substances of each DWM sub layer. They are composed of three lithography, three dry etching and a deposition step [14]. We used a modified version of NVSIM [15] to calculate the die area of the NVM. We then calculated the additional die area required to support the PIM units area from PIRM [13].

To determine the embodied energy of the DRAM, FPGA, and GPU we used the die area and technology node along with process LCA reported in the literature for 350 nm–32 nm [6] processes and for 28 nm–3 nm [7]. There is a significant gap between the two studies with a significant gap between the reported 32 nm [6] and 28 nm [7] such that a third study that reports 32 nm [16] sits between the two. Thus, in our work we do not compare nodes that cross the studies.

Prior to reporting the embodied energy we created studied several grid mix scenarios reported in Table 1. Using the carbon footprint of multiple different electrical generation methods we report the grid mix for Arizona, California, Texas, and New York, all of which have significant semiconductor fabrication activity and very different grid mixes. Arizona and Texas have significant electrical generation from coal and the highest generation from natural gas. While Arizona has significant generation from nuclear plants and Texas has significant wind energy, their 395 and 438 g of CO$_2$ equivalent generated per kW h are much higher than California and New York, which still get more than a third of their electricity from natural gas. California is very balanced on renewable energy and New York has significant hydroelectric and nuclear power generation, thus their grid mix generates about half the carbon at 234 and 188 g CO$_2$ eq/kWh, respectively.

In Table 2 we report the embodied energy and embodied carbon using the grid mixes from Table 1. The RM is augmented with PIM capabilities to compute, binary, ternary, integer, and floating point computation [13, 19]. We calculated the sustainability DDR3-1600 as this is the device that has been used to implement DRAM PIM using ELP$^2$IM [20] and conduct ternary model reduction of CNN inference. For dedicated accelerators we selected edge server appropriate low-energy devices including the Versal Prime FPGA (VM1802) from AMD/Xilinx and the NVIDIA Jetson NX mobile GPU. Note, we were somewhat limited in our choice of, particularly FPGA, devices as die area is not typically reported, which is necessary to determine embodied energy/carbon estimates. We note that the RM is extremely dense, even compared to the DDR. However, the GPU and FPGA require an order of magnitude more embodied energy due to their much larger die sizes.

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**Table 1: Energy to gCO$_2$eq/kWh [17] and Grid Mixes [18]**

| Source       | gCO$_2$eq/kWh | AZ | CA | TX | NY |
|--------------|---------------|----|----|----|----|
| Coal         | 980           | 20%| 3% | 19%| –  |
| Natural Gas  | 465           | 40%| 39%| 53%| 37%|
| Geothermal   | 27            | –  | 5% | –  | –  |
| Hydroelectric| 24            | 5% | 18%| –  | 22%|
| Solar PV     | 65            | 7% | 20%| 2% | 2% |
| Wind         | 11            | –  | 7% | 17%| 4% |
| Nuclear      | 27            | 28%| 7% | 9% | 33%|
| Biopower     | 54            | –  | 3% | –  | –  |
| Mix (gCO$_2$eq/kWh) | 395 | 234 | 438 | 188 |
Table 2: Accelerator statistics, embodied energy, and embodied carbon emissions for grid mixes from Table 1.

|                  | RM | DDR3 | RM | RM | FPGA | GPU |
|------------------|----|------|----|----|------|-----|
| Tech Node        | 321.4 | 554 | 321.4 | 321.4 | 7 | 14 |
| Die Size (mm²)   | 38  | 73   | 38 | 38  | 324 | 350 |
| Die per wafer    | 1847 | 967  | 1847 | 1847 | 217 | 201 |
| PE (kWh/Wafer)   | 1626 | 1200 | 1254 | 832  | 1482 | 882 |
| Energy (MJ/die)  | 3.17 | 4.47 | 2.44 | 1.62 | 24.59 | 15.80 |
| AZ (gCO₂eq/die)  | 348  | 490  | 268 | 178  | 2698 | 1734 |
| CA (gCO₂eq/die)  | 206  | 291  | 159 | 105  | 1598 | 1027 |
| TX (gCO₂eq/die)  | 386  | 544  | 297 | 197  | 2992 | 1922 |
| NY (gCO₂eq/die)  | 166  | 233  | 127 | 85   | 1284 | 825 |

1 Calculated using process LCA from [6].
2 Calculated using process LCA from [16].
3 Calculated using process LCA from [7].
4 Requires extra steps for spintronics [14].
5 Requires 16 dies to build a the tested 1GB DIMM.

Table 3: Performance, Operational Power, and Efficiency per Power and Carbon of Different Edge Accelerators

| Inference Acceleration using Ternary Model Reduction and PIM | Benchmark | Target | Throughput | Power | Efficiency |
|------------------------------------------------------------|-----------|---------|------------|-------|------------|
|                                                             | Alexnet   | DDR3 [20] | FPS 84.8 | 2     | 42.4       | 0.35–0.81 |
|                                                             | Ternary   | RM      | FPS 490  | 0.93  | 526        | 4.6–10.8 |

| Training Acceleration using Floating-Point 32 Data | Benchmark | Target | Throughput | Power | Efficiency |
|---------------------------------------------------|-----------|---------|------------|-------|------------|
| Alexnet                                           | GPU       | 1335    | 21.05      | 63.4  | 521–1214   |
|                                                  | RM        | 50.72   | 5.65       | 8.97  | 74–172     |
|                                                  | FPGA      | 34.52   | 7.74       | 4.46  | 37–85      |
| VGG-16                                           | GPU       | 848     | 20.37      | 41.6  | 342–797    |
|                                                  | RM        | 81.95   | 5.7        | 14.37 | 118–275    |
|                                                  | FPGA      | 46.99   | 7.71       | 6.09  | 50–117     |
Holistic Sustainability Evaluation

To determine the overall energy (and carbon footprint) of these acceleration choices we compared a CNN conducting inference using DRAM PIM [20] and RM PIM [13]. RM provides both an embodied and operational energy improvement, ultimately providing order-of-magnitude benefits in mega frames per g CO$_2$eq. Of course presuming the edge system already contains DDR3, an important experiment is to evaluate the breakeven time beyond which adding the RM acceleration would holistically improve the energy. We illustrate this using the GreenChip tool [8] in Figure 2a. The chart shows the activity ratio, which is the ratio of compute to idle time, and the sleep ratio which is the ratio of active to sleep time [8]. Note, in this case the accelerator could be idle or sleeping while the host is still used. If the accelerator is active and operating nearly constantly the break-even time can be as low as 1 year. However, as the usage drops to 50% the break-even time moves to around 500 days, with lower usage scenarios pushing into the 2–3 time frame and beyond, reaching around 4 years in the upper right corner.

To explore CNN training we compare the GPU and FPGA using a PyTorch-based flow with hand optimization to generate GPU and FPGA implementations of the AlexNet and VGG-16 training [1] and hand mapped design for the RM accelerator [19]. From Tables 2 and 3 both embodied and operational energy for the FPGA are higher than both the RM and the GPU, so the indifference calculation will never pick the FPGA. However, the RM has a lower embodied energy and a higher operational energy than the GPU. We see the indifference results in Figures 2b and 2c. For AlexNet in high usage scenarios the indifference time is relatively short to makeup the embodied energy, but starting around 50% the indifference time starts increasing dramatically such that it becomes impractical in the mid 40% range. VGG-16 follows a similar trend, but because the operational energy gap between the two is closer it becomes harder to amortize the embodied energy so the reasonable indifference times fall off sooner.

CONCLUSION

In this work, we evaluated using RM, which requires additional embodied energy to manufacture, its holistic energy comparison when integrated in edge system while performing CNN applications. The break-even point to replace DRAM PIM with RM PIM resulted in a benefit within the $1 \leq t \leq 2$ years, likely on the low end of that time-frame given the rising popularity of CNN acceleration
on edge servers. In our indifference comparison between RM and the Jetson Xavier NX mobile
GPU the edge server activity ratio needs to be at least 40% for lightweight CNNs like Alexnet and
higher for more complex ones like VGG-16 to make a GPU lower overall energy than RM with an
in service time of $\leq 10$ years. We also include carbon emissions for both embodied and operational
energies where the ranges correspond to the ranges enumerated in the different grid mixes. Note,
the break-even and indifference charts for carbon are identical the same if a consistent grid mix is
used.

Another concern previously raised that remains true is that embodied effects remain high com-
pared to operational effects. Given it takes tera or even petaflops of GPU compute to be equivalent
to a g CO$_2$eq and the amortization time of embodied carbon measured in multiple kg CO$_2$eq is still
high (years to decades) and solutions to bring this down are necessary. We suggest that RM PIM
can be a solution insomuch as it competes in the operational phase with order of magnitude lower
embodied carbon.

Unfortunately, the observation that the process LCA models are considerably disjoint at their
meeting point of a similar technology node is a concern. Thus, the process LCA still requires
improvement and validation, or at least calibration, which makes convergence on a raw magnitude
difficult. However, if this is effectively a constant offset, then the relative comparisons are still
extremely useful in allowing considerable design space exploration.

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