A 3.125-to-22-Gb/s multi-rate clock and data recovery using voltage-regulated active filter

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Abstract: This letter presents a multi-rate clock and data recovery circuit realized in a standard 65-nm CMOS technology, which operates from 3.125 Gb/s to 22 Gb/s. In order to cover the wide frequency range, a modified four-stage differential ring VCO is exploited, which provides not only the fast tracking ability from its coarse tuning, but also the precise tracking from its fine tuning. Also, a voltage-regulated active filter is employed to reduce the ripples of the VCO control voltages. It helps to fasten the lock-in time of the proposed CDR circuit and improve the jitter characteristics against PVT variations. Measurements reveal that the CDR chip demonstrates very wide capture range of 3.125 ∼ 22 Gb/s, 3.3 psrms data jitter at 20 Gb/s, and 112-mW power dissipation from a single 1.2-V supply. The chip core occupies the area of 0.12 mm² only.

Keywords: CDR, multi-rate, PVT variation, ring VCO, voltage-regulated active filter

Classification: Integrated circuits

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1 Introduction

Clock and data recovery (CDR) circuits have been very popular in wireline applications including optical transceivers, backplane interconnections, chip-to-chip interconnects [1]. Even in wireless on-off keying communication systems, they may become attractive to obtain jitter-less gigabit data links. In particular, optical links mandate CDR circuitry to generate pure clock signals and recover clean data for its following digital processing units. In this paper, we present a multi-rate CDR circuit targeted for high-speed digital optical interface applications by utilizing a standard 65-nm CMOS technology. The proposed CDR incorporates a number of circuit techniques such as quarter-rate clock configuration, ring voltage-controlled oscillator (VCO) with compensation circuits against PVT variations, voltage-regulated active filter (VRAF), etc. Typically, the quarter-rate configuration is employed for alleviating the burden of VCO designs, because its clock frequencies become only 1/4 of the data-rates. In this work, we exploit a quarter-rate linear phase detector (PD). Instead of using a charge-pump, a voltage-to-current converter is utilized for high-speed operations [2]. Ring-type VCO is employed for wide tuning range characteristics [3]. However, since a conventional ring VCO may not be tolerant enough to overcome severe PVT variations, a compensation circuitry is added to improve the tune-ability of the ring VCO, particularly for the case of tracking failure. Moreover, an active filter with a low-dropout (LDO) voltage regulator is incorporated to reduce the ripples of the VCO control voltages, hence helping to improve clock and data jitter characteristics [4].

2 Circuit description

2.1 Architecture of the proposed CDR

Fig. 1 depicts the architecture of the proposed CDR circuit that shares the basic topology as a typical quarter-rate linear CDR, except for both replacing a charge-pump with a high-speed voltage-to-current (V-I) converter and substituting a second-order passive filter with a VRAF. Since our design targets to achieve wide tuning range for multi-rate operations, the proposed CDR is optimized to enable continuous operations from 3.125 Gb/s to 22 Gb/s. In this case, any desired bit-rate can be easily selected by the variation of the control voltage levels of the ring VCO. As an example, Fig. 1 illustrates four different operation speeds (i.e. 3.125 Gb/s, 5 Gb/s, 10 Gb/s, and 20 Gb/s) which are targeted for high-speed digital optical links.

Here, only quarter-rate clock frequencies (i.e. 0.78 GHz, 1.25 GHz, 2.5 GHz, and 5 GHz, respectively) are necessary, since the phase detector exploits a quarter-rate configuration.
2.2 Quarter-rate phase detector

Fig. 2 shows the block diagram of the linear quarter-rate phase detector, where two half-rate phase detectors and two XOR circuits are utilized. The error signals and the reference signals are generated through the XOR gates. The demuxed outputs, i.e. Dout1 and Dout2, are acquired at the second latches. It is noted that a MUX and a couple of buffers are additionally integrated to yield Dout3 which provides an output with the same operation-speed as that of the input data stream, hence facilitating the eye-diagram testing.

Fig. 2. Block diagram of the linear quarter-rate phase detector.
2.3 V-I converter

A V-I converter in this work replaces a conventional charge-pump, not only because it is suitable for high-speed operations, but also because the designed quarter-rate phase detector provides enough gain. The V-I converter is simply realized as a couple of differential pairs with diode-connected PMOS loads (shown in Fig. 3). The current-mirroring actions charge and discharge the following loop filter, in accordance with the incoming UP and DOWN signals. The UP signals correspond to the reference signals generated in the phase detector, whereas the DOWN signals corresponds to the error signals. Namely, this V-I converter yields charging currents when the clock signals lag the data, whereas it discharges the loop filter when the clock signals lead the data.

2.4 VRAF (voltage-regulated active filter)

As for a loop filter to produce a control voltage of VCO, a simple second-order passive filter is conventional and popular. Mostly, a passive filter consisting of a resistor and a couple of capacitors is utilized [4, 5]. However, the passive second-order filter is very prone to a number of noise sources such as injected noises from VCO itself, crosstalk noise, supply noises, thus giving rise to considerable ripples of control voltages.

Therefore, the VRAF configuration is proposed in this paper for the purpose of alleviating these ripple issues. Fig. 4 illustrates the schematic diagram of the proposed VRAF which comprises an op-amp, passive resistors and capacitors, and a PMOS pass-transistor. The negative input of the op-amp is connected to the reference voltage (@ a nominal 0.83 V), and therefore the output of the pass transistor follows the reference voltage even at the situations of severe perturbations from those noise sources. Namely, the VRAF can avoid ripples effectively, generate constant control voltages, and thus reduce clock and data jitters. This function can be accomplished by utilizing a low drop-out (LDO) voltage regulator which is optimized to yield a constant voltage as a reference for the VRAF [6]. Post-layout simulations in Fig. 5 reveal that the lock-in time and the ripple voltages of the proposed CDR circuit can be significantly reduced when compared to those of a
conventional CDR (that replaces the VRAF with a second-order passive filter). Here, the bandwidth of the VRAF is designed to be 6 MHz.

It is also noted that careful chip-layout should be conducted for simultaneously acquiring large power supply rejection ratio, efficient noise reduction, and good stability.

Fig. 4. Simplified circuit of the voltage-regulated active filter.

Fig. 5. Simulated lock-in time and the control voltage ripples of (a) the proposed CDR, and (b) a conventional CDR circuits.
2.5 Wide-tuning ring VCO

Fig. 6(a) illustrates the block diagram of the proposed VCO which is a four-stage differential ring-oscillator with 3-bit coarse tuning switches. For wide tuning-range characteristics, each gain-cell exploits an inverter-type differential pair with diode-connected PMOS loads [2]. Three switches are inserted between the differential pairs and the current-sources, such that a desired operation-speed can be selected depending upon which switch is turned on.

In addition, the proposed VCO has two different gain mechanisms, thereby providing fast tracking ability by coarse tuning and precise tracking capability by fine tuning.

![Block diagram of the proposed ring VCO and the schematic diagram of a gain-cell](a)

![Wide tuning range of the proposed VCO](b)

Fig. 6. (a) Block diagram of the proposed ring VCO and the schematic diagram of a gain-cell, (b) wide tuning range of the proposed VCO.
Fig. 6(b) shows the simulation results of the wide tuning range of the proposed ring VCO. It is clearly seen that the VCO covers the whole frequency range from 400 MHz to 5 GHz. Fig. 6(a) depicts the simulated clock signals (at 5 GHz) of the VCO outputs and its jitter characteristics, where the clock jitter is estimated to be 4.5 ps_p-p_p._

### 3 Chip fabrication and measured results

Test chips of the proposed multi-rate CDR circuit are fabricated by using a standard 65-nm 1P9M CMOS technology. Fig. 7 shows the chip micro-photograph where the chip occupies the area of 0.9 x 0.8 mm$^2$ (core area 0.25 x 0.48 mm$^2$).

Fig. 8 depicts the measurement setup for eye-diagrams where the chips were tested on-chip in the bit-rate of up to 22 Gb/s by utilizing Anritsu MP1800A pulse-pattern-generator and Agilent DCA-X 86100D oscilloscope. Fig. 9 demonstrates the measured eye-diagrams for $2^{15}$-1 PRBS inputs at different data rates of 3.125 Gb/s, 5 Gb/s, 8 Gb/s, and 10 Gb/s, respectively. The output voltage levels are measured to be larger than 185 mV_p-p at a 50-Ω matched single-ended output.

![Chip microphotograph of the proposed multi-rate CDR.](image)

**Fig. 7.** Chip microphotograph of the proposed multi-rate CDR.

![Test setup for eye-diagrams of the proposed CDR.](image)

**Fig. 8.** Test setup for eye-diagrams of the proposed CDR.
Fig. 9. Measured eye-diagrams for $2^{15} - 1$ PRBS at different data rates of: (a) 3.125 Gb/s, (b) 5 Gb/s, (c) 8 Gb/s, and (d) 10 Gb/s.

Fig. 10. Measured eye-diagrams for $2^{15} - 1$ PRBS at different data rates of: (a) 20 Gb/s, and (b) 22 Gb/s.

Table I. Performance summary of the proposed CDR and comparison with recently published CMOS Multi-Rate CDRs.

| Parameters                  | [1]    | [7]    | [8]    | This work |
|-----------------------------|--------|--------|--------|-----------|
| Technology                  | 90 nm CMOS | 90 nm CMOS | 90 nm CMOS | 65 nm CMOS |
| Configuration              | Half-rate | Quarter-rate | Quarter-rate | Quarter-rate |
| VCO type                    | Gated VCO | DLL     | LC VCO | Ring VCO |
| Operation speed (Gb/s)      | 20/10/5/2.5 | 6.0-to-44 | 20     | 3.125-to-22 |
| Data jitter @ 20 Gb/s       | 33 ps,p-p | -       | -      | 3.3 ps,rms |
| Clock jitter @ 5 GHz        | -       | -       | 1.44 ps,rms | *4.5 ps, p-p |
| Power dissipation (mW@1.2 V)| 90      | 230     | 318    | 112       |
| Core area (mm²)             | 0.2     | 0.2     | 0.56   | 0.12      |
| **FoM**                    | 4.5     | 5.2     | 15.9   | 5.1       |

*simulated jitter, **FoM = mW/Gb/s(max.)
Fig. 10 shows the measured eye-diagrams at different data rates of 20 Gb/s and 22 Gb/s, for $2^{15}-1$ PRBS inputs. Here, it is noted that considerable signal loss and distortion occur at cables and connectors, giving rise to eye-closure at 20 Gb/s and beyond. Thus, the effects from the inevitable loss and distortions (typically S-parameters) were de-embedded from the measured eye-diagrams at the 86100D oscilloscope itself.

DC measurements reveals the power dissipation of 112 mW (including output buffer) from a single 1.2-V supply. Table I summarizes the performance of the proposed CDR circuit, and the recently published CMOS multi-rate CDR circuits are listed for comparison.

4 Conclusion

A multi-rate clock and data recovery circuit is realized in a 65-nm CMOS technology, which exploits a voltage-regulated active filter for reduced ripples of VCO control voltages and improved jitter characteristics against PVT variations, and also employs a modified four-stage differential ring oscillator with compensation circuits for wide tuning-range. Measurements reveal that the proposed CDR demonstrate wide capture range from 3.125 Gb/s to 22 Gb/s with 112-mW power dissipation from a single 1.2-V supply. The chip core occupies the area of 0.12 mm$^2$ only. Hence, the proposed CDR circuit provides a low voltage, low power solution for the applications of short-haul optical links or low cost optical interconnects.

Acknowledgments

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT and future Planning (NRF-2014R1A2A2A01005686). Also, this work was supported by IDEC (EDA Tool).