Atomic scale characterization of graphene p-n junctions for electron-optical applications

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Graphene p-n junctions offer a potentially powerful approach towards controlling electron trajectories via collimation and focusing in ballistic solid-state devices. The ability of p-n junctions to control electron trajectories depends crucially on the doping profile and roughness of the junction. Here, we use four-probe scanning tunneling microscopy and spectroscopy (STM/STS) to characterize two state-of-the-art graphene p-n junction geometries at the atomic scale, one with CMOS polySi gates and another with naturally cleaved graphite gates. Using spectroscopic imaging, we characterize the local doping profile across and along the p-n junctions. We find that realistic junctions exhibit non-ideality both in their geometry as well as in the doping profile across the junction. We show that the geometry of the junction can be improved by using the cleaved edge of van der Waals metals such as graphite to define the junction. We quantify the geometric roughness and doping profiles of junctions experimentally and use these parameters in Nonequilibrium Green’s Function based simulations of focusing and collimation in these realistic junctions. We find that for realizing Veselago focusing, it is crucial to minimize lateral interface roughness which only natural graphite gates achieve, and to reduce junction width, in which both devices under investigation underperform. We also find that carrier collimation is currently limited by the non-linearity of the doping profile across the junction. Our work provides benchmarks of the current graphene p-n junction quality and provides guidance for future improvements.

I. INTRODUCTION

The discovery of graphene as a new two-dimensional electron system with high intrinsic mobility and photon-like band structure has led to a surge of interest in applying it to implement solid-state electron optics systems where the ballistic motion of electrons is explored in order to manipulate the flow of an electron beam [1]. Ballistic electron transport in GaAs two-dimensional electron gas already allows for carrier steering using electric and magnetic fields [2–5]. As an example, a local electrostatic potential in GaAs can be used to confine electrons laterally and thus control their flow in a device. However, such performance is limited to cryogenic temperatures in GaAs. Graphene displays ballistic transport over micron length scales at room temperature, renewing interest in solid-state electron optics [6–11]. However, the Dirac dispersion of graphene implies that local electrostatic potentials are not effective at carrier confinement due to Klein tunneling [12]. While electron flow in graphene cannot be turned off by doping, it was realized that the carrier trajectory can be modified by creating electrostatic doping profiles. In particular, two important predictions have been made for electron flow through p-n junctions [13–15], in which an interface is created between a p-type (hole-like) and an n-type (electron-like) region on the same graphene sheet [16, 17]. These predictions are shown schematically in Fig. 1a. The first prediction (upper panel) is for a sharp junction where the junction width d is much smaller than the electron’s Fermi wavelength $k_F d \ll 1$. In this case, electrons incident on the p-n interface from a point source will be focused to a point on the other side of the p-n interface [14], a phenomenon termed Veselago lensing. The second prediction (lower panel) is made for a wide junction where $k_F d \gg 1$. In this case, electrons incident on the p-n interface from a point source will be strongly collimated, with an angle-selective transmission probability given by $T(\theta) \sim e^{-\pi k_F \frac{d}{2} \sin^2 \theta}$. Therefore, only electrons near normal incidence transmit through the junction while the rest are reflected [13]. Both focusing and collimation, arising respectively from

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the plane wave and Bloch parts of the electron wave-
function, can be used to control the electron trajecto-
ries, and have given rise to a number of device concepts
[18–25]. Two examples are graphene p-n junction based
field effect transistors and radio frequency (RF) switches
where multiple angled p-n junctions can be used to turn
on and off current flow through the device [21, 25], and
enhanced Rudermann-Kittel-Kasuya-Yosida (RKKY)
interaction for scalable graphene-based spintronics devices
by utilizing Veselago focusing of graphene p-n junctions
[24]. Note that for an RF switch, a modest current on-off
ratio much lower than the ballistic $10^4$ or even $100$ would
suffice.

The theoretical predictions of geometric optics-like car-
rier transport in graphene have led to a number of ex-
perimental efforts to realize these predictions, primarily
via measuring electron transport across one or more p-n
junctions. Lee et al. conducted transport measurements
across a p-n interface where signatures of lensing were
observed, albeit after a background subtraction proce-
dure [26]. Chen et al. demonstrated negative refrac-
tion in a graphene p-n junction, but were able to ob-
serve the effect only under a magnetic field [27]. Barnard
et al. recently reported an electron beam collimator in
graphene based on collinear pairs of slits [28], but clean
collimation has yet to be realized in single p-n junctions
[13, 23]. Sajjad et al. proposed a collimation-based field
effect transistor using two graphene p-n junctions aligned
at different angles and predicted a $10^4$ on-off ratio for
ballistic trajectories with no edge scattering, ~$10^2$ for
perfect edges in a $1 \mu m$ wide device, and ~$10^3$ in the
presence of edge roughness [21, 22]. Experimentally, a
$R_{off}/R_{on} \sim 1.3$ was reported before in a similar de-
vice [29]. Recent effort has pushed this ratio value to
13 [30]. All of the experimental work so far on graphene
p-n junctions indicate that they fall far short of the ideal
predictions. Theoretically, it is expected that atomic
scale junction imperfections in real p-n junctions signifi-
cantly modify their electron-optical functions [31]. These
imperfections include junction interface roughness, finite
junction width, and non-linearity as well as asymmetry
of their doping profiles. It is thus important to measure
the nanoscale properties of state-of-the-art p-n junctions,
and to develop an understanding of how the non-ideality
of a junction affects the transport of carriers across the
interface. Scanning tunneling microscopy (STM) is an
ideal probe to achieve this in graphene. It is a technique
capable of giving atomic scale topographic and spec-
 troscopic information across a single p-n junction, allowing
us to characterize the junction completely [32, 33]. In
this work, we use a four-probe STM with in-situ scan-
ing electron microscopy (SEM) to study graphene p-n
junctions. The four-probe STM allows for each individu-
al probe to act independently as contacts for gating and
bias as well as the scanning probe for STM/STS mea-
surement. Our STM results are analyzed with Nonequi-
librium Green’s function (NEGF)-based simulation of
electron flow through inhomogeneously doped graphene
to develop a microscopic understanding of electron flow
through realistic graphene p-n junctions.

## II. RESULTS AND DISCUSSION

We perform our STM measurements on graphene p-n
junctions that are fabricated by two independent tech-
niques. Figure 1b illustrates the first type of junction
device based on a pre-patterned SiO$_2$/Si substrate with
buried polysilicon gate electrodes, shown as red/orange
bars in Fig. 1b. These highly doped polysilicon gates
are patterned to form interdigitated finger structures and
buried within the SiO$_2$ layer. We study this junction as
an example of what state-of-the-art CMOS-based pro-
cessing is able to achieve for the junction geometry. All
the red electrodes are electronically connected to a com-
on contact pad, as are the orange electrodes. They then
form coplanar split gates with 100 nm spacing within
each pair. We create a stack of exfoliated graphene atop
hexagonal boron nitride (hBN), and place it onto the
buried gate SiO$_2$/Si substrate using the standard poly-
mer dry transfer technique. A graphene p-n junction is
formed above each pair of split gates. Also shown in Fig.
1b is our experimental setup: two probes are used to
apply the gate voltages to the buried polysilicon gates, a
second probe (bias probe) is used to apply a sample bias to
the graphene for STM measurement, and the final probe
is used as the STM scanning probe. The second type of
p-n junction is shown in Fig. 1c. In this method, a piece
of few-layered graphite with a naturally cleaved sharp
deedge is used as one of the gate electrodes, while the sil-
icon wafer is used as the second gate. This method has
been shown in transport experiments to be an improved
choice for uniform, sharp gating for a new generation of
graphene devices [27, 34]. We use hBN to encapsulate the
graphite gate. On top of the hBN/graphite/hBN stack
sits a monolayer graphene flake, partially overlaying the
underlying encapsulated graphite gate. In the exper-
iment, independent back gate voltages are supplied to the
bottom layer graphite and the underlying Si substrate to
create a split gate on the monolayer graphene. Apart
from the sharpness of the graphite gate, the graphite
also avoids problems that arise from the grain structure
of typical metals (patch effect). For the sake of discus-
sion, we will refer to the first and second junction devices
as the polySi and graphite gate devices respectively. Our
four-probe STM system is combined with an in-situ UHV
SEM, which allows us to accurately locate a sample area
that only spans a few micrometers, and position the scan-
ing probe precisely at the junction interface [35]. Fig-
ures 1d-e show SEM images of each device, showing con-
trast between differently gated regions allowing landing
of the STM probe at the junction area as well as making
electrical contacts for the gate and bias with the other
probes. We note that with the in-situ four-probe capabil-
ity in our system, no lithography is needed to pattern the
electrodes. This greatly preserves the sample cleanliness,
FIG. 1. (a) Schematic of two electron optical functions for a graphene p-n junction: Veselago lensing for a sharp junction ($k_F d \ll 1$) and collimation for a wide junction ($k_F d \gg 1$). (b) Schematic of the polySi gate device and experimental setup. Two independent local gate $V_{G1}$ and $V_{G2}$ are supplied through a split buried polysilicon to the graphene forming a p-n junction. (c) Schematic of the graphite gate device and experimental setup. A global gate $V_{G2}$ and a partial gate $V_{G1}$ are supplied through $\text{SiO}_2/\text{Si}$ and graphite respectively to the graphene on top. A p-n junction forms at the sharp graphite edge. (d-e) SEM secondary electron images taken under gating conditions for polySi gate device (d) and graphite gate device (e). p-type (hole-like) and n-type (electron-like) regions display different contrast in terms of secondary electron emission, as denoted by red arrows. Also labeled are the gating probe, bias probe and scanning probe used in the experiment. (f) A representative STM topographic image of graphene on hBN in a polySi gate device. The image shows a moiré pattern due to lattice mismatch between graphene and hBN. STM topography set points are 0.6 V, 20 pA.

enabling high quality STM/STS measurements. Shown in Fig. 1f is a large-scale STM topography of graphene on hBN taken on the polySi gate device showing a clear moiré pattern due to the mismatch between the graphene and hBN lattices. Imaging of large clean areas is essential to characterize the graphene p-n junctions, and this in turn is enabled by the four-probe instrument.

Figure 2a is a large STM topographic image across a p-n junction in a polySi gate device, with a gate bias of +30/-30 V applied to the two gates. Also shown is a zoomed-in image across a part of the junction where the moiré pattern between graphene and hBN is clearly seen. The junction itself is visualized as a step in topographic contrast across the image. We also show STM topographies of the same junction area at other gating conditions (see Supplementary Fig. S1). This step feature at the junction is not visible in those conditions, indicating that the step seen in Fig. 2a arises from electronic contrast in the density of states (DOS) across the junction rather than height contrast. The STM images in Fig. 2a and its inset also show several point defects. These defects are likely present in the hBN substrate [36] and affect the graphene by electrostatic doping. To compare with the polySi gate geometry, Figure 2b shows a STM topographic image of the graphite gate p-n junction with a gating condition of 0V/-6V. This image also shows the junction clearly as a step in topographic contrast. In the case of the graphite gate junction, a large part of the topographic contrast actually comes from the height change as the tip goes over the edge of the underlying graphite gate. Additional topographic contrast arises when the gates are biased to create a p-n junction (see Supplementary Fig. S2 for additional AFM and STM topography images on the graphite gate device).

Simple visual inspection of Fig. 2a and 2b shows that real p-n junctions suffer from lateral roughness, and the graphite gate device has a significantly reduced roughness compared to the polySi gate device in this regard. To better characterize the lateral roughness of the junction, we performed spectroscopic $dI/dU$ mapping to measure the spatial local DOS (LDOS) at the energy of $E = eV_{bias}$ for both devices. $dI/dU$ mapping (a single $dI/dV$ value is taken at each pixel point) allows us to measure the LDOS with high spatial resolution in a short time com-
FIG. 2. (a) A large STM topographic image of the junction interface in a polySi gate device. Inset is a magnified image of the junction area. The STM topography set points are -0.2 V, 30 pA and 0.3 V, 30 pA for the inset. (b) A large STM topographic image of the junction interface in a graphite gate device. STM topography set points are 0.1 V, 50 pA. (c) A $dI/dU$ mapping of the polySi gate device at the same area as Fig. 2a. The image reflects a spatial distribution of Dirac point $E_D$ across the junction interface. Also labeled are $x$ and $y$ directions. (d) A $dI/dU$ mapping of the graphite gate device at the same area as Fig. 2b. (e) Lateral interface roughness $y(x)$ extracted from $dI/dU$ mapping in Fig. 2c-d. (f) Autocorrelation function of the profiles in Fig. 2e for both devices. The correlation length is marked by the star. (g) The RMS and correlation length from the analysis of Fig. 2e.

pared to $dI/dV$ mapping (a whole $dI/dV$ spectrum is taken at each pixel point), thus minimize drift errors. Figure 2c shows a $dI/dU$ map of the same region as Fig. 2a, taken at $V_{bias} = -0.2$ V. At this bias voltage, the DOS of p-doped graphene is higher than the DOS of n-doped graphene. Thus, the boundary between the two regions shows up clearly in the $dI/dU$ map with nanometer spatial resolution. We can then use this information to extract the lateral position $y$ of the boundary as a function of distance $x$ along the boundary. We do this in the following way: Graphene’s DOS has a simple linear relationship $\text{DOS}(E) = A|E - E_D|$ where $A$ is a constant and $E_D$ is the Dirac point energy. Therefore, a LDOS mapping at a fixed $E = eV_{bias}$ (such as Fig. 2c) can be used to generate a mapping of $E_D$ in space with high resolution. $E_D$ will shift across the p-n junction ($y$ direction in Fig. 2c). We pick the zero crossing of the Dirac point energy $E_D = 0$ to define the spatial position of the boundary $y_{\text{boundary}}$. The variation of $y_{\text{boundary}}$ along the $x$ direction in Fig. 2c thus characterizes the lateral roughness of the p-n junction. We plot such one-dimensional contour $y(x)$ as a blue line in Fig. 2e. The same procedure can also be performed on the graphite gate device, as shown in Fig. 2d and the red line in Fig. 2e. We quantify the magnitude of the junction roughness by calculating a root mean square (RMS) value of the line profiles in Fig. 2e. The RMS value of the roughness for the polySi gate device is 2.3 nm, compared to 0.81 nm for graphite gate. To analyze the lateral roughness of each junction in more detail, we calculate the autocorrelation function (ACF) of the junction profiles in Fig. 2e, and show them in Fig. 2f. We define a correlation length as the point where the ACF has dropped to $1/e$ of its initial value. Figure 2f shows that the roughness in the polySi gate has a shorter correlation length of $\lambda = 7.7$ nm than that in the graphite gate where $\lambda = 15.5$ nm. In Fig. 2g, we compare the junctions numerically. The graphite gate device is smoother, having lower RMS and a larger correlation length for its junction roughness.

Having characterized the junction roughness, we now turn to the actual doping profile as we transit from the hole doped to the electron doped side of the junction. In typical theoretical calculations of p-n junctions with width $d$, it is assumed that the doping profile linearly interpolates between the two sides of the junction as schematically illustrated in Fig. 3a (black line).
However, a real, non-ideal device inevitably possesses a certain non-linearity as denoted schematically by the orange line. To experimentally measure the junction potential profile, we take a series of $dI/dV$ spectra at equally spaced points along a line crossing the junction interface of the polySi gate device (green line at the top of Fig. 3b). In Fig. 3b, we show several selected $dI/dV$ spectra from a line-cut illustrating the evolution of the spectra across the junction. The STS spectrum of graphene has a minimum at the location of the Dirac point $E_D$. It is clearly seen that the Dirac point shifts from below to above the Fermi energy $E_F$ as the tip traverses the junction along the arrow direction, corresponding to a shift from $n$-doped to $p$-doped graphene. These line-cut $dI/dV$ profiles thus allow us to trace the spatial evolution of the Dirac point across the junction, and therefore the local doping profile of the graphene. In Figures 3c-d we plot the spatial evolution of the Dirac point position $E_D$ relative to the Fermi level for the graphite gate junction for two separate gating conditions, 0V/0V and 0V/-6V. In the absence of gating, this region of graphene is $n$-doped with the Dirac point $E_D$ at around -100 meV below $E_F$ (Fig. 3c). Substrates are known to dope graphene in similar devices [37]. When a voltage of -6V is applied to the graphite gate, a symmetric $p$-$n$ junction is created as shown in Fig. 3d. The situation is substantially more complicated in the case of the polySi gate devices. Shown in Fig. 3f-h are the doping profiles for the polySi gate device for three separate gating conditions: +30V/-30V, 0V/0V and -30V/+30V, respectively. In Fig. 3f, at +30V/-30V gate bias, two features of the profile stand out. Firstly, the measured potential profile displays a marked non-linearity as opposed to the ideal linear curve. Secondly, the measured junction has a very asymmetric potential profile, with higher doping on the $n$-side than the $p$-side, even under symmetric +30/-30V external gating conditions. We gain further insights into the device from the profile in Fig. 3g at 0V/0V gate bias. Surprisingly, a pronounced doping distribution exists even without the gating. We attribute this to trapped charge from the fabrication process, as will be
discussed below. There is a significant $n$-doping on both sides of the junction with a slightly $p$-doped region in the middle. Finally, Figure 3f shows the doping profile under $-30\mathrm{V}/+30\mathrm{V}$ gating. It is evident that we failed to create a $p$-n junction due to the inherent asymmetric doping in the device. We find similar results at different points along the junction. Our measurements of the local doping profiles in these graphene $p$-$n$ junctions provide useful microscopic insight into the quality of the $p$-$n$ junction, and confirm that lithographically fabricated gate structures are inferior to graphite based gate structures. The presence of a doping distribution in the polySi gate junction indicates the presence of non-uniform charge under the graphene sheet even in the absence of gate voltages. We have attempted to quantitatively model this scenario using a simple electrostatic model where inhomogeneous trapped charge is located at the top of the SiO$_2$ surface. Supplement S3 provides details of the simulation. We attribute the substrate doping to the fabrication process of the buried polysilicon gate electrodes, in particular the electro-polishing step used to smooth the SiO$_2$ above the polySi gates. In our simple model, we assume a uniform trapped charge density above each polySi gate electrode (independent of applied gate voltage), and use electrostatic COMSOL simulations of the real junction geometries, materials and potentials of our devices to best fit the measured doping profiles at all gating conditions. Figure 3e shows the built-in potential in the polySi gate device calculated by our COMSOL model for zero gating condition with the trapped charge necessary to fit our three gating conditions as shown by the dotted lines in Fig. 3f-h. To fit the three data sets optimally requires a piecewise trapped charge distribution above the SiO$_2$ of $7.5 \times 10^{12}$ charges/cm$^2$ above the left gate, $5.6 \times 10^{12}$ charges/cm$^2$ above the right gate and $7.5 \times 10^{11}$ charges/cm$^2$ above the area between the gates with linear transitions between them. Although the confinement of the trapped charge to the surface is a simplistic approximation, the good agreement between models and doping profiles in Fig. 3f-h suggests that trapped charge is a consistent explanation for the potential profiles seen at all three gating conditions. For the graphite gate, a uniform trapped charge density of $1.6 \times 10^{12}$ charges/cm$^2$ above the SiO$_2$ creates the best fit of the model to the data. We also quantify the non-linearity of the potential profile for both devices by applying a linear fitting to the experimentally measured profiles and using the residual sum of squares as a figure of merit (see Supplementary Fig. S3). The residual sum of squares from polySi gates is an order of magnitude larger than from graphite gates, implying a significantly larger non-linearity, as evident in Fig. 3c-h. Although it is impossible to escape junction non-linearity in full due to the finite distance from the gating electrodes to the graphene in any device, the graphite gate device architecture is superior to the polySi as its graphite gating electrode is closer to the graphene and it lacks the variable trapped charge distribution. One can also extract the $p$-$n$ junction width $d$ from these profiles. In Fig. 3d, we use red arrows to denote the start and the end of the junction interface giving rise to a junction width $d$ of around $40 \mathrm{nm}$ for graphite gates. Similarly, in Fig. 3f, $E_D$ starts to change from the center and almost saturates approaching the left edge (red arrows). The junction width $d$ is thus around $100 \mathrm{nm}$ for the polySi gate device, as expected since the spacing between the split gates was also $100 \mathrm{nm}$. Overall, the graphite gate device shows a narrower junction width, a smaller junction non-linearity and a more uniform substrate doping, allowing for gating to produce a symmetric profile, not possible in the polySi gate devices at reasonable voltages.

Having characterized the parameters at the atomic scale in real graphene $p$-$n$ junctions, we now assess the impact of these parameters on two key electron-optical functions: collimation and Veselago lensing. We do this through model simulations using the NEGF formalism. The analysis is helped by the fact that the width of the junction (40-100 nm) is much larger than the length scale of the lateral roughness (a few nm) in the junction. We can therefore independently model the effect of lateral roughness and of the doping profile in our junctions. Veselago lensing happens for a sharp $p$-$n$ junction where $k_Fd \ll 1$, while carrier collimation happens for $k_Fd \gg 1$. For our graphite gate device with a symmetric profile (a single $k_F$ value for both electron and hole doped side), a rough estimate gives $k_Fd \approx 1$. For the polySi gate device which has an asymmetric profile (different $k_F$ values for electron and hole doped sides), a rough estimate gives $k_Fd \approx 1 \sim 10$. These estimates put our junction devices in an intermediate regime between ideal collimation and ideal Veselago lensing. Given these considerations, we proceed to study what one would observe for each case with the real junction parameters. Figure 4a shows the device structure in our model where we have an electron injection source with finite contact width $W_s$ on the left side of the junction and an extended drain on the right side to reduce multiple scattering from the edge and quantum interference effects. This device is a generic structure for both polySi gate and graphite gate devices (in the graphite case, Gate 2 region is controlled by the back gate).

We first look at collimation. We use an extended source ($W_S = device width (160 \mathrm{nm})$ for Fig. 4b-c) to evaluate the performance as this permits electrons to arrive with various incidence angles allowing us to assess the angular filtering function. We calculate the low bias conductance $G$ of a single $p$-$n$ junction at 300 K, 

$$G(E_F) = \frac{4q^2}{h} \int T(E) \left( -\frac{\partial f_0}{\partial E} \right) dE \quad (1)$$

Here, $T(E)$ is the transmission probability, $f_0 = f(E - E_F)$ is the Fermi function, $q$ is the electron charge and $h$ is Planck’s constant (see Supplementary S5 for calculation details). $G$, the conductance, characterizes the
efficiency of electron transmission through the p-n junction. A higher conductance thus indicates a lower collimation, and vice versa. We first calculate the conductance for a linear doping profile with no roughness, which we use as a baseline for our calculations of real junctions. We then consider both the graphite and the polySi gate structures, and calculate the transmission through the junction with and without lateral roughness included in the calculation. The right panel of Fig. 4b shows the experimentally measured non-linear junction profile and its linear approximation for both devices which are both used in the calculation. Finally, the conductance for each case is scaled by the conductance for the linear doping profile with no roughness, which we use as a baseline for our calculations of real junctions. We clearly see that conductance of both devices deviates from the linear case in the p-n junction regime (-0.4 eV < E < 0.175 eV for polySi and -0.15 eV < E < 0.07 eV for graphite). This deviation is highest for the energy values close to the energy boundary of the junction where the slopes of the non-linear potential also differ most compared to the linear approximation. The deviation from unity in the conductance ratio is due to a variation in the slope for the non-linear case: a smaller slope of the potential is associated with a larger junction width $d$, which, in turn, creates a longer effective barrier (from the transmission probability formula stated above) and hence lower transmission probability (and hence higher collimation) and lower conductance. Similarly, larger slopes lead to higher transmission/conductance and lower collimation. The disadvantage of having a non-linearity is that the conductance $G(E_F)$ (hence the collimation) now strongly depends on the actual energy position of the Fermi level $E_F$ which itself is hard to control in real junction devices due to the substrate doping. In other words, the non-linearity makes collimation performance unpredictable, and therefore is a disadvantage from a design point of view. At the level of a single junction, the non-linearity in the junction doping profile plays an important role in determining the conductance of the junction, while the roughness does not have a significant impact on the conductance.

Although roughness does not greatly influence single junction conductance, it does affect the conductance of a two junction device. Sajjad et al. proposed using a graphene double p-n junction for electronic switching, taking advantage of a highly angle selective transmission [21]. For such a two junction device where electron transmission through each junction is coupled with the
other, one can create an effective gate-tunable “transport gap” in graphene to turn the current on and off by using it in a unipolar regime or bipolar regime (p-n junction). We have simulated electron conduction through such a two junction device. Figure 4c shows results for the polySi gate devices. The green curve corresponds to a unipolar regime while the red curve represents a bipolar regime with a much lower conductance than the “transport gap”. However, as we add the interface roughness, the conductance in the bipolar regime increases (blue dashed curve), implying a reduction in the effective current on/off ratio for such a device.

Next we look at Veselago lensing. For the Veselago simulation, we adopt a point source in our model ($W_s (= 32\text{nm}) \ll \text{device width (} = 160 \text{ nm})$) and a symmetric junction (equal doping on both sides) to evaluate the impact of the junction width and interface roughness on the focusing. We first consider an abrupt junction ($d = 0$) to isolate the contribution of interface roughness. Figure 4d shows the calculated LDOS for polySi gate and graphite gate devices. We also calculate the LDOS for the ideal junction without roughness as a comparison (result not shown in Fig. 4d). The LDOS was calculated using $\text{LDOS}(x, y; E) = A(x, y; E)/2\pi$ where $(x, y)$ is the coordinate of site $i$ and $A$ is the spectral function given by $A = 2\text{Im}(G^R)$ with $G^R$ being the retarded Green’s function obtained from the recursive Green’s function algorithm [38]. LDOS represents the probability density profile in the channel. In the case of Veselago focusing, electrons coming from the left point contact (source) should converge to a point on the right side of the junction at an equal distance from the junction. Therefore, the probability of finding electrons in the vicinity of the focal point should be higher and hence LDOS should also be higher than in the rest of the channel. Figure 4d suggests that Veselago focusing is robust against relatively low roughness of the graphite gate for an abrupt junction. However, focusing characteristic is strongly smeared out at the high roughness seen in the polySi gate, even for an abrupt junction. This is clearly shown in Fig. 4e, where line-cuts of Fig. 4d at $x = 50 \text{ nm}$ are compared. For the polySi gate case, the junction roughness plays an important role in randomizing the electron trajectories as they transit across the junction in a manner similar to roughness on an optical lens, and this effect is clearly seen in the LDOS as well. As the roughness is reduced (as is the case with the graphite gate), the focusing characteristics of the junction reappear and the LDOS becomes indistinguishable from the ideal junction case. We also repeat this calculation by varying the junction width $d$ to see its impact on the focusing. In Fig. 4f, we plot the central peak intensity (at $y = 0 \text{ nm}$) of the $x = 50 \text{ nm}$ line-cut as a function of junction width $d$ for ideal, polySi gate and graphite gate roughness cases. Again, the graphite gate shows a comparable performance to the ideal case, while the polySi gate randomizes the electron trajectories so much that the signal at the center point fluctuates at all widths. When the junctions are smooth enough (ideal and graphite gate cases), the focusing decays rapidly as the junction width $d$ increases, since fewer electrons can penetrate the junction and thus the signal intensity is reduced significantly. Two lessons are learned from these simulations. Firstly, the graphite gate is uniform and smooth enough to realize Veselago lensing whereas the polySi gate is fundamentally limited in these respects. Secondly, even in a perfect junction, the junction width imposes another limitation on lensing, thus preventing the graphite gate device from lensing even though it meets other requirements. In the future, one should consider exploring improved devices using graphite gates, for instance with thinner hBN, to utilize the uniformity and smoothness of the graphite gate junctions and to create sharper junctions where signatures of Veselago lensing may be seen in experiments.

III. CONCLUSIONS

We have reported atomic level characterization of two state-of-the-art types of graphene p-n junction devices using STM/STS. We find inherent imperfections as each junction exhibits finite width and lateral roughness as well as a chemical potential profile non-linearity and asymmetry which are directly measured with STS. We show that a significant improvement is exhibited in these parameters if one adopts an exfoliated graphite gate device geometry. To investigate the impact of these imperfections, we use our experimental findings as inputs into graphene p-n junction simulations of two important electron-optical applications: collimation and Veselago lensing. For Veselago lensing, junction roughness makes it impossible for polySi gates to lens for any junction width; graphite gates, although smooth enough, are inhibited by a junction width too large to lens. Collimation, as characterized by the conductance, is robust against junction roughness, but significantly affected by the non-linearity in the potential profile. Our work represents a significant advance in characterizing and analyzing graphene p-n junction for both fundamental research and practical applications.

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Supporting Information

Atomic scale characterization of graphene p-n junctions for electron-optical applications

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S1. STM TOPOGRAPHIC IMAGES OF THE POLYSI GATE JUNCTION AREA AT VARIOUS BIAS/GATING CONDITIONS

All STM topographic images were taken in a constant current mode. They show a convolution of electronic and structural contributions, but a feasible way to distinguish structural from electronic factors in STM topography is to collect the images at various sample bias conditions. Structural features should be independent of the sample bias while electronic features can change with bias. In our p-n junction devices, we can also change the external gating condition as this will change the density of states (DOS) landscape across the junction and therefore modulate the electronic contribution. In Fig. S1a-c, we display three topographic images taken in the same junction area at different bias/gating conditions. Figure S1a is the same as Fig. 2a, taken at -0.2 V bias and +30 V/-30 V external gating condition. A ‘step edge’ appears in the center of the image. Figure S1b was taken at -0.5 V bias and -30 V/+30 V external gating. The ‘step edge’ is less obvious in the image, indicating that it is not a true structural feature. In Fig S1c, we turned off the external gating and collected the image at 0.1 V bias. Instead of a ‘step edge’, a trench shows up in the image due to the change of DOS landscape across the junction. These images exclude any real structural step edge from the substrate as the origin of the ‘step edge’ shown in Fig. 2a.

FIG. S1. (a-c) STM topographic images of a polySi gate device taken at different external gating conditions of (a) +30V/-30V, (b) -30V/+30V and (c) 0V/0V respectively.
In a graphite gate device, the junction area should display a height contrast due to the underlying graphite gate. AFM across the junction, Fig. S2a, displays a height contrast of 5 Å at the junction, reflecting a true structural feature. Figure S2b,c are STM topographic images taken at 0V/-6V external gating but with 0.1 V and -0.1 V bias, respectively. While the measured height change across the junction in Fig. S2b is around 5 Å, consistent with the AFM result, it changes to 7.5 Å in Fig. S2c due to the relative change of local DOS at the two sides of the junction as we change the bias. We also note that the “trench” seen at STM topography at the junction is also due to the reduced local DOS.

- **FIG. S2.** (a) AFM image of the junction in a graphite gate device. (b, c) STM topographic image of the junction in a graphite gate device taken at 0.1 and -0.1 V bias, respectively, and 0V/-6V external gating.

**S3. ELECTROSTATIC CALCULATION OF THE JUNCTION POTENTIAL PROFILE**

We have carried out an electrostatic numerical simulation of the junction potential profile in order to verify our hypothesis that trapped charge leads to experimental asymmetries and non-linearity. Simulations were done using finite-element modeling via the electrostatics module of the commercial software COMSOL. To model the polySi gate devices, we created a two-dimensional device geometry in COMSOL with piecewise junction geometry (Fig. 3e in the main text) consisting of two polySi buried gates split by 100 nm, buried 100 nm below the surface of the 300 nm thick SiO$_2$ on silicon. Above the SiO$_2$ surface we modeled 20 nm of hexagonal boron nitride (hBN) (as in the experimental geometry). Next, the appropriate boundary conditions and voltages were applied to the gates, after which the potential profile was measured at the surface of the hBN, hence the graphene location. Finally, a graphene dispersion relation was applied to the potential profile to determine the piecewise Dirac point shifts. As this basic model clearly cannot reproduce the potential profiles with no gating nor the asymmetry for symmetric gating, we found that to reproduce experimental profiles, 3 different trapped charge densities at the surface of the SiO$_2$ are necessary: $7.5 \times 10^{12}$ charges/cm$^2$ atop one polySi gate, $5.6 \times 10^{12}$ charges/cm$^2$ above the second and $-7.5 \times 10^{11}$ charges/cm$^2$ between the two. These variable trapped charges likely arise due to the polishing involved to make the SiO$_2$ flat after burying the gates. A good agreement between the simulation with the given trapped charge values and the experiment is found, verifying that the asymmetry and non-linearity of our junction potential profile is consistent with these substrate-trapped charges.

**S4. ANALYSIS OF NON-LINEARITY OF JUNCTION POTENTIAL PROFILES**

To conduct a quantitative analysis of non-linearity of measured junction potential profiles, we apply linear fitting to the experimental profiles. Figure S3a-e show the experimental curves and their linear fitting for both polySi gate and graphite gate devices. Then we calculate the residual sum of squares for each fitting and use it to quantify the
non-linearity of junction potential profiles. Figure S3f lists the results. The residual sum of squares for the polySi gate is an order of magnitude larger than that of the graphite gate meaning a larger non-linearity.

**FIG. S3.** (a–e) Experimental junction potential profiles of polySi gate and graphite gate devices and their respective linear fittings. (f) Table lists the residual sum of squares after fitting to quantify the non-linearity.

### S5. CALCULATION OF THE CONDUCTANCE

In a quantum transport simulation, the current is obtained using Landauer’s formula,

$$ I = \frac{q}{h} \int T(E) [f_1(E, \mu_1) - f_2(E, \mu_2)] dE $$  \hspace{1cm} (S1)

where $T(E)$ is the transmission spectrum between contacts 1 and 2, $f_i(E, \mu_i)$ is the Fermi function of contact $i$, $q$ is the charge of an electron and $h$ is Planck’s constant. For numerical efficiency, we have employed the recursive Green’s function (RGF) algorithm [S1] where the channel is divided into $N$ blocks with block 1 connected to contact 1 and block $N$ connected to contact 2. In this approach, the transmission is calculated using a computationally efficient Green’s function formula,

$$ T(E) = \text{tr}\{\Gamma_{11}[-2\text{Im}(G_{11}) - G_{11}\Gamma_{11}G_{11}^\dagger]\} $$  \hspace{1cm} (S2)

where $G_{11}$ is the Green’s function for block 1 calculated using the RGF algorithm, and $\Gamma_{11} = -i(\Sigma_{11} - \Sigma_{11}^\dagger)$ with $\Sigma_{11}$ being the self-energy of contact $i$ calculated using the decimation algorithm. The Hamiltonian matrix used in the above calculations is obtained using the modified approach for computational efficiency [S2]. The electrostatic potential energy is modeled by modifying the diagonal elements of the Hamiltonian matrix by $-qV_i$ where $V_i$ is the electrostatic potential at side $i$.

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