Wideband High Gain Active Feedback Transimpedance Amplifier

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Abstract
A new wideband high gain CMOS transimpedance amplifier is presented without using any inductor. In the proposed TIA, gain enhancing path is introduced in the active voltage-current feedback TIA topology to increase both the gain and bandwidth. This path increases the transconductance of the proposed TIA which reduces the input resistance and leads to bandwidth extension. Additionally, for utilizing the benefit of this topology, cascading of common source stage is also done to increase the gain further without deteriorating the bandwidth. Mathematical analysis is also performed to evaluate both the gain and bandwidth enhancement. These analyses are supported by simulations that are done using TSMC 0.18 μm CMOS technology with the input photodiode capacitance of 0.3 pF. The proposed TIA occupies 0.019 mm² area and consumes 3.2 mW from 1.8 V supply voltage. The transimpedance gain of the proposed TIA is found to be 57.15 dBΩ over the bandwidth of 6.5 GHz. The input noise is 17.16 pA/√Hz.

Keywords  Active feedback · Inductorless · Transimpedance amplifier · Cascade

1 Introduction

The significant increase in the demand of huge data rates has motivated inventors to explore optical communication systems (OCS) that are apt to handle this requirement. Transimpedance amplifier (TIA) is the very crucial front-end block at the receiver link of OCS. TIA work is to convert small input current signal into an amplified voltage level. Therefore, gain is an important parameter of TIA and it should be as high as possible. Few design techniques are reported in the literature to boost the gain which includes positive feedback technique [1], self cascode structure [2, 3] and cascading of buffer stages [4]. Positive feedback increases the gain by reducing the overall output conductance, however, it has stability issues. Self cascode structure also increases the gain but it enhances the voltage headroom. Cascading of stages

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increases the gain but at the expense of power dissipation and bandwidth. Apart from gain, bandwidth is also an important parameter which is restricted due to large input photodiode capacitance. Various bandwidth enhancement techniques are reported such as inductive peaking [5, 6], capacitive degeneration [7, 8], capacitive feedback [9, 10], negative capacitance [11], common gate (CG) [12] and regulated cascode (RGC) [13, 14]. Both the inductive and capacitive compensation increase the bandwidth but they occupy the large chip area. CG topology also gives a wide operating frequency range but yields relatively higher noise. RGC is the very common topology to design TIA due to its high stability, low input impedance and wide bandwidth. On the other hand, it has higher power dissipation and headroom voltage.

In this work, active voltage-current feedback (AVCF) TIA topology [15] is used which provides low input and output impedances. In this topology, the gain enhancing path is introduced in such a way that it increases both gain and bandwidth. This path increases the transconductance and thereby, reduces the input resistance which leads to bandwidth extension. Moreover, a common source (CS) stage has been cascaded to use the advantage of this topology to increase the gain further without deteriorating the bandwidth.

AVCF topology is reviewed in Sect. 2. The proposed TIA design is discussed in Sect. 3. In Sects. 4 and 5, noise analysis and simulation results are discussed, respectively. Section 6 concludes the paper.

### 2 Active Voltage-Current TIA

The TIA circuit based on AVCF topology is shown in Fig. 1 in which transistor $M_1$ provides feedback path and decreases the output and input resistances [15]. In this circuit, transistor $M_1$ itself converts the current into a voltage whereas other topologies use resistor to do the same. The drain current of transistor $M_1$ is given by [15]:

$$I_{d2} = g_{m1} V_o = g_{m1} V_{in}.$$  

### Fig. 1 Active voltage-current TIA [15].
The input and output resistances are given in Eqs. (2), and (3) respectively [15].

\[ R_{in} = \frac{1}{g_{m1}}. \]  
\[ (2) \]

\[ R_o = \frac{1}{(1 + R_1 g_{m1})g_{m2}}, \]  
\[ (3) \]

where \( R_1 \) is the total resistance at the input port due to both current source \( CS_1 \) and the output resistance of transistor \( M_1 \). The transimpedance gain of the circuit is given by [15]:

\[ Z(s) = \frac{R_1 R_2 g_{m2}}{R_1 R_2 C_1 C_2 s^2 + (R_1 R_2 C_1 (g_{m2} + g_{mb2}) + R_1 (C_1 + R_2 C_2)s + R_1 R_2 g_{m1} g_{m2} + R_2 (g_{m2} + g_{mb2}) + 1}. \]  
\[ (4) \]

where \( C_2 \) and \( R_2 \) are the sum of parasitic capacitance and intrinsic resistance at the output port respectively. \( C_1 \) is the total capacitance at the input port. From Eq. (4), the transimpedance gain at low frequency has been deduced as:

\[ Z(0) = \frac{R_1 R_2 g_{m2}}{R_1 R_2 g_{m1} g_{m2} + R_2 (g_{m2} + g_{mb2}) + 1}. \]  
\[ (5) \]

Since the output impedance of TIA (shown in Fig. 1) is very low, therefore, cascading of the gain stage can be done without affecting the bandwidth. The number of gain stages can be chosen based on the trade-off that exists between gain, power consumption and noise.

3 The Proposed TIA

The proposed circuit of TIA is presented in Fig. 2 where \( C_{pd} \) is input photodiode capacitance and \( I_{in} \) is photodiode current. The active voltage-current feedback (AVCF) TIA is formed by transistors \( M_1 \) and \( M_2 \) in which transistor \( M_1 \) is providing voltage-current feedback. In AVCF TIA, modification has been done by introducing gain enhancing path which includes resistor \( R_p \) and transistor \( M_p \). This path not only increases the gain but also extends the bandwidth. It also increases the transconductance of the amplifier which leads to decrement in the input resistance. Additionally, a common source (CS) stage (\( M_3 \) and \( R_D \)) has also been cascaded.
with TIA to increase the gain further. This cascaded voltage gain stage does not affect the bandwidth due to the low output resistance of TIA as mentioned in Sect. 2. The small signal analysis is performed to show the gain enhancement and bandwidth extension.

In Fig. 3, the small signal equivalent circuit is depicted in which \( g_{mi} \) (where \( i = 1, 2, 3, P \)) are the transconductance of transistors \( M_i \) (where \( i = 1, 2, 3, P \)) respectively. \( C_{in} \) is the total capacitance at the input node which comprises of gate-to-source capacitance \( C_{gsp} \) of transistor \( M_p \) and the capacitance of photodiode. \( R_1 \) is the overall resistance at the input side and \( R_2 \) is the total resistance at the \( V_o \) (shown in Fig. 2) node. The transfer function is determined by applying Kirchhoff’s current law (KCL) at nodes \( V_1, V_2, V_3, \) and \( V_{out} \) shown in Fig. 3. Body bias effect is neglected because \( g_{mp,2} > g_{mbp,2}. \) \( C_{gs0} \) is the summation of the gate-to-source capacitances of \( M_1 \) and \( M_3 \) whereas \( C_{gd} \) is the total of the gate-to-drain capacitances of \( M_p \) and \( M_2. \)

The transimpedance gain is realized as:

\[
Z(s) = \frac{V_{out}}{I_{in}} = \frac{Z(0)}{(a_1 s + b_1 s + 1)}
\]

where \( Z(0) \) is transimpedance gain at low frequency and is obtained as:

\[
Z(0) = \frac{R_2 R_p R_D g_{m1} g_{m3} (1 - g_{mp} r_{op})}{(R_1 g_{mp} + g_{m2} R_2) R_p - g_{m2} r_{op} R_2 + R_p}. \tag{7}
\]

Assuming \( g_{m0} r_o > 1, \) Eq. (7) can be estimated as:

\[
Z(0) = \frac{R_1 R_2 R_p R_D g_{m1} g_{m3} g_{mp} r_{op}}{(R_1 g_{mp} + g_{m2} R_2) R_p - g_{m2} r_{op} R_2}. \tag{8}
\]

On comparing Eqs. (5) and (8), it can be determined that gain is enhanced by introducing path \((M_p \) and \( R_p) \) and the common source stage \((M_3 \) and \( R_D)\). The coefficients of Eq. (6) are found to be:

\[
a_1 = \frac{C_{gd3}}{g_{m3}} \tag{9}
\]

\[
b_1 = \frac{C_{gd1}}{g_{m1}} \tag{10}
\]

---

**Fig. 3** Small signal equivalent circuit
where \( C_1 = C_{gs0} + C_{gd1}, C_2 = C_{in} + C_{gd1} \) and \( C_3 = C_{gs0} + C_{gd1} \).

The dominant pole can be calculated as:

\[
P = \frac{(R_1 g_{mp} + g_m R_2) R_p - g_m r_{op} R_2}{R_1 R_p r_{op} C_{gs2} g_{mp} + R_1 R_2 R_p C_{gs2} g_{mp} + R_2 r_{op} C_{gs2} + R_2 R_p C_1 - R_1 R_2 R_p C_{1} g_{mp}}. \tag{13}
\]

The input resistance is obtained as:

\[
R_{in} = \frac{(1 + r_{op} g_{mp})(r_{op} + R_p)}{(g_m + g_{mp})(r_{op} + R_p) r_{op} + r_{op} g_{mp} + 1}. \tag{14}
\]

On comparing Eqs. (2) and (14), it is found that input resistance of proposed circuit is diminished by introducing path (\( M_p \) and \( R_p \)) which isolates input photodiode capacitance and thereby, extends the bandwidth. In the proposed circuit, biasing is provided in such a way that the transistors are operated in a saturation region. Aspect ratios of transistors are selected in order to minimize the trade-offs between gain, bandwidth and noise.

### 4 Noise Analysis

The input of the transimpedance amplifier is photodiode current which is very small in magnitude. Therefore, noise becomes an important parameter for TIA which has to be analysed. Main noises exist in TIA are flicker and thermal noise [16]. The small signal equivalent circuit for noise analysis is depicted in Fig. 4.

The total input-referred noise of modified ACVF-TIA is obtained by:

\[
I_{n,\text{total}}^2 = I_{n,M1}^2 + I_{n,Mp}^2 + I_{n,M2}^2 + I_{n,R1}^2 + I_{n,R2}^2 \tag{15}
\]
where $I_{n,M1}^2, I_{n,Mp}^2, I_{n,M2}^2$ and $I_{n,R2}^2$ are the noises due to transistors $M_1$, $M_p$, $M_2$, and $M_4$. These can be estimated as:

$$I_{n,M1}^2 = \frac{1}{g_{m1}^2} \left( 4KT\omega^2 C_{gs1}^2 (\gamma g_{d01}) + \frac{g_{m1}^2 K_F}{W_1 L C_{ox}} \right)$$ (16)

$$I_{n,M2}^2 = \frac{1}{g_{m2}^2} \left( 4KT\omega^2 C_{gs2}^2 (\gamma g_{d02}) + \frac{g_{m2}^2 K_F}{W_2 L C_{ox}} \right)$$ (17)

$$I_{n,Mp}^2 = \frac{1}{g_{mp}^2} \left( 4KT\omega^2 C_{in}^2 (\gamma g_{d0p}) + \frac{1}{R_p} + \frac{g_{mp}^2 K_F}{W_p L C_{ox}} \right)$$ (18)

$$I_{n,R1}^2 = \frac{4KT}{R_1}$$ (19)

$$I_{n,R2}^2 = 4KT \gamma g_{d0,R2}(1 + M)\omega^2 C_{g0}^2$$ (20)

$\gamma$ is noise factor of transistor, $K_F$ is process dependent constant, and $g_{d01}$, $g_{d02}$ and $g_{d0p}$ are zero-bias drain conductance [17] of transistors $M_1$, $M_2$ and $M_p$ respectively. First and the last terms in Eqs. (16) – (18) are thermal and flicker noises due to transistors respectively.

After substituting the values of $I_{n,M1}^2, I_{n,M2}^2, I_{n,Mp}^2, I_{n,R1}^2$ and $I_{n,R2}^2$ in Eq. (15), the total input-referred noise is expressed by:

$$I_{n,\text{total}}^2 = \frac{1}{g_{m1}^2} \left( 4KT\omega^2 C_{gs1}^2 (\gamma g_{d01}) + \frac{g_{m1}^2 K_F}{W_1 L C_{ox}} \right) + \frac{1}{g_{m2}^2} \left( 4KT\omega^2 C_{gs2}^2 (\gamma g_{d02}) + \frac{g_{m2}^2 K_F}{W_2 L C_{ox}} \right)$$

$$+ \frac{1}{g_{mp}^2} \left( 4KT\omega^2 C_{in}^2 (\gamma g_{d0p}) + \frac{1}{R_p} + \frac{g_{mp}^2 K_F}{W_p L C_{ox}} \right) + \frac{4KT}{R_1} + 4KT \gamma g_{d0,R2}(1 + M)\omega^2 C_{g0}^2$$ (21)

From Eq. (21), it is found that the value of the resistance $R_1$ and size of transistor $M_1$ should be high enough to minimize noise of proposed TIA. At higher frequency, noise rises due to the effect of dominating term $\omega C$. However, the total noise of the proposed circuit would be slightly more than noise given in Eq. (21) due to cascading of the common source stage.

### 5 Simulation Result

Simulations of the proposed TIA are done using Mentor Graphics based Eldo simulation tool in TSMC 180 nm technology. The values of parameters of proposed circuit are mentioned in Table 1. For the comparison purpose, AVCF-TIA has also been simulated using the same technology and tool with similar circuit parameters as that of proposed TIA.

Figure 5 represents the frequency responses of AVCF, AVCF with CS stage and proposed TIA (AVCF + CS + CGP). This figure shows that the proposed TIA circuit offers
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The highest gain (57.15 dBΩ). Further, it also displays improvement in bandwidth, which gets extended to 6.5 GHz as compared to 1.7 GHz of AVCF with CS stage. All these improvements are obtained in proposed TIA while consuming only 3.2 mW power. Figure 6 presents the DC transfer characteristic of proposed TIA, which shows an almost linear relationship between input current and output voltage. The transient response of proposed TIA is presented in Fig. 7. It is observed that the swing of output voltage is nearly 10 mV for 10 µA input current.

The variations in frequency response for different photodiode capacitances (Cpd = 0.1 pF, 0.2 pF, 0.3 pF and 0.4 pF) and at different temperatures are presented in Figs. 8 and 9, respectively. It can be concluded from Fig. 8 that the bandwidth reduces with the increasing values of Cpd. However, the variations in the bandwidth with photodiode capacitance are very low. Figure 9 shows that both the gain and bandwidth reduce with the increase in temperature. The effect of variations in temperature has been studied on DC behaviour of the proposed TIA and is depicted in Fig. 10. It can be observed that the variations in DC response due temperature changes are very nominal and the linearity is maintained. Figure 11 depicts the input-referred noise of proposed TIA which is around 17 pA/√Hz.

Above simulations have been carried out using the exact values of parameters mentioned in Table 1. However, in practical environment the fabricated devices will not possess the precise dimensions and will lead to variations in the behaviour of the proposed circuit as compared to the simulated results as shown above. To show the robustness of the proposed circuit in practical environment, Monte Carlo analysis and corner analysis of the proposed TIA has been carried out. To perform Monte Carlo analysis in proposed circuit, a set of 200 samples of width of the transistors with ±5% mismatch have been considered and the results obtained have been illustrated in Fig. 12. These results show

Table 1 Parameters of proposed circuit

| Parameters    | Values                                           |
|---------------|--------------------------------------------------|
| Resistance    | R_D = 800Ω, R_P = 500Ω                          |
| Bias voltage  | V_B1 = 1.2 V                                     |
| Aspect ratio  | M_1 = 15/0.18 µm, M_2 = 50/0.18 µm               |
|               | M_3 = 40/0.18 µm, M_p = 30/0.18 µm               |
| Capacitance   | C_p = 0.3 pF                                     |

Fig. 5 The frequency response of AVCF, AVCF with CS stage and proposed TIA
that the minimum and maximum gains of proposed TIA are 56.2 dBΩ and 57.9 dBΩ, respectively. To observe the variations in DC behaviour of the proposed TIA, its Monte Carlo analysis with similar runs and variations in aspect ratio have been performed. These variations in DC response have been plotted in Fig. 13. All these results confirm
that the variations observed in AC and DC responses with change in aspect ratio of transistors of the proposed TIA is quite nominal and thereby prove the robustness of the circuit in practical environment.

Further to justify the proper functioning of the proposed TIA without fail even in extreme design conditions in complete work space, the corner analysis of the proposed TIA has been performed. Since proposed TIA consist of only NMOS transistors, therefore, it has only two process corners that are Slow (S) and Fast (F). Figures 14 and 15 respectively show the frequency response and DC response of proposed TIA at different process corners. It can be observed that at the two process corners, bandwidth varies from 6.4 GHz to 7.3 GHz, while gain remains almost constant. Moreover, DC behaviour
Fig. 10  Effect of temperature variations on DC response of the proposed TIA

Fig. 11  Input-referred noise

Fig. 12  The frequency response using Monte Carlo simulation
also shows a linear response at the two corners, justifying the proper operation of the proposed TIA in complete design space.

Figure 16 presents the layout of proposed TIA which depicts that the proposed circuit occupies 0.0197 mm² chip area. The pre-layout and post-layout simulations are depicted in Fig. 17 which shows that the gain is the same as that of pre-layout simulation but the bandwidth is slightly reduced.

Table 2 illustrates the comparative results of existing TIAs and proposed TIA. It can be observed that performance of proposed TIA is superior than all other TIAs mentioned in Table 2 except [15]. However, the gain and bandwidth of TIA presented in [15] are higher than the proposed TIA but at the expense of noise, chip area and power dissipation. Furthermore, the chip area of proposed circuit is also lesser than all other TIAs except [21]. But, other parameters of the proposed design are better as compared to [21]. Additionally, proposed circuit indicates the supremacy over other existing TIAs in terms of Figure of merit (FOM), expressed by:
Fig. 15  Process corner analysis on DC response of the proposed TIA

Fig. 16  Layout of proposed TIA
Active feedback based TIA is proposed in which gain enhancing path is introduced to increase both gain and bandwidth. Bandwidth is extended by increasing the transconductance which reduces the input resistance. Moreover, a CS stage is also cascaded which leads to further gain enhancement without compromising the bandwidth. In the proposed TIA, gain and bandwidth both are enhanced along with both low power consumption and chip area.

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Declarations

Conflict of interest  The authors declare that they have no conflict of interest.

References

1. Amourah, M. M., & Geiger, R. L. (2010). A high gain strategy with positive-feedback gain enhancement technique. IEEE International Symposium on Circuits and Systems, 1, 631–634.
2. Yan, S., & Sanchez-Sinencio, E. (2000). Low voltage analog circuit design techniques: A tutorial. IEICE Transactions on Fundamentals of Electronics, 83, 179–196.
3. Singh, U., Gupta, M., & Srivastava, R. (2015). A new wideband regulated cascode amplifier with improved performance and its application. Microelectronics Journal, 46, 758–776.
4. Chien, J., & Lu, L. (2007). 40-Gb/s high-gain distributed amplifiers with cascaded gain stages in 0.18-um CMOS. IEEE Journal of Solid-State Circuits, 42, 2715–2725.
5. Mohan, S. S., Hershenson, M. D. M., Boyd, S. P., & Lee, T. H. (2000). Bandwidth extension in CMOS with optimized on-chip inductors. IEEE Journal of Solid-State Circuits, 35, 346–355.
6. Chien, J., & Lu, L. (2007). 40-Gb/s high-gain distributed amplifiers with cascaded gain stages in 0.18-um CMOS. IEEE Journal of Solid-State Circuits, 42, 2715–2725.
7. Sackinger, E., & Guggenbuhl, W. (1990). A high-swing, high-impedance MOS cascode circuit. IEEE Journal Solid-State Circuits, 25, 289–298.
8. Seifouri, M., Amiri, P., & Dadras, I. (2017). A transimpedance amplifier for optical communication network based on active voltage feedback. Microelectronics Journal, 67, 25–31.
9. Gray, P. R., & Meyer, R. G. (2001). Analysis and design of analog integrated circuits. Wiley.
10. Sansen, W. M. C., & Chang, Z. Y. (1991). Low-noise wide-band amplifiers in bipolar and CMOS technologies. Springer.
11. Han, S. M., Sun, G., & Jiang, F. (2009). Area-efficient CMOS transimpedance amplifier for optical receivers. Analog Integrated Circuit and Signal Processing, 58, 67–70.
12. Chen, D., Yeo, K. S., Shi, X., Do, M. A., Boon, C. C., & Lim, W. M. (2013). Cross-coupled current conveyor based CMOS transimpedance amplifier for broadband data transmission. IEEE Transactions on very large scale of integration (VLSI) systems, 21, 1516–1525.
13. Marufuzzaman, M., Reaz, M. B. I., & Yeng, L. S. (2018). Design of low-cost transimpedance amplifier for optical receiver. Transaction on Electrical and Electronic Material, 1, 7–13.

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