A Low-Power 20-Gb/s Discrete-Time Analog Front-End for ADC-Based Serial Link Equalizers

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Abstract—This paper presents a discrete-time analog front-end for an analog-to-digital (ADC) based equalizers. The front-end uses a discrete-time linear equalizer (DTLE) and ultra-low-power 4-bit time-interleaved charge-steering flash ADC. The DTLE serves two functions: linear equalization and sampling and holding for the following charge-steering ADC. The ADC uses fully differential low-power clocked comparators. Low power in the comparators is achieved by embedding a dynamic latch into the core of a charge-steering pre-amplifier. The 20-Gb/s front-end is designed and simulated in a 65-nm CMOS technology. The flash ADC uses 4-stage interleaving and thus requires 4 DTLEs running at 5 Gb/s. A 5-Gb/s DTLE consumes 0.57 mW from a 1.2-V supply and the ADC consumes 15.5 mW from a 1-V supply at 20 GS/s for a total power dissipation of 17.78 mW or 0.89 pJ/bit. The ADC has an SNDR of 23.9 dB, an SFDR of 33.6 dB, and an effective number of bits (ENOB) of 3.67 bits for a sinusoidal input of frequency 9.84 GHz and amplitude 600 mV

Keywords—Charge-Steering, Preamplifier, Regeneration, Ultra-low power, Comparator, Flash ADC, High-speed ADC, Time-interleaved, ADC-based systems, Dynamic latch, Discrete-Time, Linear Equalizer.

I. INTRODUCTION

High-speed comparators with low-power consumption and small sensitivity are essential blocks in many applications that require very high sampling rates and low resolution such as data-storage read channels and wired communication systems [1]. As the demand for high rates increases, comparators must cope with this need while achieving as low power consumption and small area as possible. For example, recent communication links try to use ADC-based receivers which mainly depend on analog-to-digital converters (ADCs). However, power consumption remains a concern. A comparator is the main building block in any ADC. Improving its performance by reducing its kick-back noise and power consumption while maintaining high sampling rate will directly improve the whole ADC. As a result, the multi-standard reconfigurable systems which heavily depend on an ADC near the front end and digital blocks at the back end are becoming more common.

Time-interleaving has been widely used to allow for higher speed ADCs while keeping power consumption at reasonable levels. The power consumption overhead of interleaving becomes insignificant above certain frequencies when compared to the increase of the power consumption of a single-channel ADC.

The goal of the paper is to propose and analyze a novel topology, based on the charge-steering concept, for an ultra-low-power ultra-high-speed comparator. Then this comparator is used to build a low-power flash ADC to be used in a high-speed serial link ADC-based equalizer. A 4-bit 20-GS/s 4x time-interleaved flash ADC is used. Usually, serial link equalizers need some linear equalization to compensate for precursor inter-symbol interference (ISI), as a result, the design of the analog front-end of the equalizer is completed by adding discrete-time linear equalizer (DTLE) at the input.

The design of the DTLE is explained in section II. Section III discusses the charge-steering concept. The proposed fully differential comparator is discussed in section IV along with its proposed single-ended version and its delay analysis. Section V shows the designed charge-steering Flash ADC based on that comparator. The simulation results of the comparator, the ADC, and its front-end are given in section VI. Finally, the work is concluded in section VII.

II. DISCRETE-TIME LINEAR EQUALIZER

Since the analog input is changing at very high speeds, Flash ADC-comparators might sample the input at different instances due to the different types of mismatches. To overcome this issue, a sample-and-hold (S/H) circuit is needed at the input of the ADC to make sure that the introduced input to all of the comparators is the same. During the reset mode of the comparators, the sample-and-hold circuit samples the input then hold it for the comparators during the amplification and the regeneration modes [2].

For pre-cursor ISI equalization, many designs adopted the conventional continuous-time linear equalizer (CTLE) [3]. The main disadvantage of the CTLE is the direct and continuous path from supply to ground. That is why it is not a proper option for the low-power applications. A DTLE is a linear equalizer that replaces the conventional CTLE and its continuous-time nature to a discrete-time nature [2] - [4]. It could be seen as a combined continuous-time linear equalizer and a sample-and-hold circuit.

The resistive loads in a conventional CTLE are replaced with switched resistors and the conventional current sources are replaced with clocked current sources as shown in Figure 1. The circuit has two main modes of operation, the hold mode, and the track-and-equalize mode. When CLK signal is “High”, the track-and-equalize mode is activated. The clocked current...
sources and the loading resistors are “ON”, hence the DTLE works as a peaking amplifier as shown in Figure 1 (b). When CLK signal goes “Low”, the circuit enters the hold mode. The clocked current sources are “OFF” and the switched resistors are at high impedance and hence the output values are almost not changing during this phase as presented in Figure 1 (c). This is good for the ADC to follow and cancels the need for a sample-and-hold circuit. As a result, power is saved. However, the input devices are not instantly switched off because some time is needed to charge the tails nodes to switch off the input devices, so the output nodes face some leakage and the amplitude drops a little. Some reset NMOS transistors $M_7$ and $M_8$ might be added to rapidly charge the tail nodes and thus switch off the input devices during the hold mode. This will decrease the leakage of the output node and solve the issue as shown in Figure 2. The input at the end of the clock is sampled, processed and held.

The circuit is degenerated with a capacitor $C_s$ which is the main reason for the gain peaking. This capacitor with the degeneration resistor $R_s$ form a zero at $\omega_z$ and a pole $\omega_{p1}$, and these are added to the existing pole at the output node at $\omega_{p2}$. The locations of the poles and the zero are as following:

$$\omega_z = \frac{1}{R_s C_s}$$  \hfill (1)

$$\omega_{p1} = 1 + \frac{(g_m + g_{mb}) R_s}{2 R_s C_s}$$  \hfill (2)

$$\omega_{p2} = \frac{1}{R_d C_{pl}}$$  \hfill (3)

where $R_d$ is the resistance of the clocked PMOS switch in the load that is kept in the linear region of operation.

$$R_d = \frac{1}{\mu_p C_{ox} (W/L)(|V_{GS}| - |V_{th}|)}$$  \hfill (4)

Some of the most important and meaningful quantities for the peaking amplifier is the DC gain, AC gain and the peaking it achieves. Peaking is defined as the ratio of the high-frequency gain to the low-frequency gain.

$$Gain_{DC} = \frac{(g_m + g_{mb}) R_d}{1 + (g_m + g_{mb}) R_s / 2}$$  \hfill (5)

$$Gain_{Hi-freq} = g_m R_d$$  \hfill (6)

III. CHARGE-STEERING CONCEPT

Instead of using current-steering power-hungry circuits, discrete-time charge-steering circuits consume less power than their continuous-time current-steering counterparts, especially at high speeds. This advantage can be utilized in designing semi-analog circuits such as latches, demultiplexers, clock-and-data recovery (CDR) circuits, and comparators as well as mixed-mode systems such as ADCs [4]. The main concept is converting the continuous-time current-steering circuit to a discrete-time charge-steering topology as in [4]. The tail current source, as in Figure 1 (a), is replaced with a charge source, and the load resistors with switched capacitors. Discrete-time operation requires two switches in the tail path and two at the output nodes as shown in Figure 2 (b).
The operation of this charge-steering-based differential amplifier is divided into two phases; reset phase and amplification phase. In the reset phase, the tail capacitor is discharged while the output nodes are pre-charged to \( V_{DD} \). In the amplification phase, the tail capacitor is connected to the tail node, drawing a current from the input pair while the outputs are disconnected from \( V_{DD} \). Then, the input pair draws a differential current from the load capacitors in proportion to the differential input voltage. This results in an output voltage proportional to the input voltage. Figure 4 was introduced in [5] as a dynamic latch for digital signals utilizing charge-steering circuits. The extra back-to-back PMOS pair \( M_7-M_8 \) helps in extending the swing of the original amplifier. This circuit cannot be used as a comparator for analog signals. The reason is that for small input signals, the input pair \( M_1-M_2 \) is fighting against the regenerative latch \( M_7-M_8 \) and will need a long time constant to produce an output. Hence, at high clock frequencies, the sensitivity of this circuit is compromised.

![Fig. 3. Differential Pair Using: (a) Current-Steering. (b) Charge-Steering.](image)

**IV. THE PROPOSED FULLY-DIFFERENTIAL COMPARATOR**

The proposed comparator is utilizing the charge-steering concept as shown in Figure 5. The basic charge-steering amplifier consists of transistors \( M_1-M_6 \), \( M_9-M_12 \) and two tail capacitors \( C_T \) amplifies the input signal. In order to regenerate the output signal, a regenerative latch might be added after this stage which will cause an increase in the power consumption of the comparator drastically. In this proposed design, an idea of an embedded regenerative latch as in [6] is used but it is turned “OFF” in the reset and amplification phases and is turned “ON” in the regeneration phase. This is achieved by switching the transistor \( M_{13} \) in Figure 5. \( M_{13} \) isolates the regenerative latch from both reset and amplification phases in order to avoid fighting. This results in an ultra-fast amplification for very low power consumption. The role of the embedded regenerative latch is to redistribute the differential charge increasing the output voltage. A new clocking scheme is introduced to facilitate the proposed operation. Figure 6 shows the proposed clocking scheme. The operation is divided into three phases of operation: reset phase, amplification phase, and regeneration phase. Figure 7 shows the proposed circuit in its three phases of operation.

![Fig. 4. A Schematic Diagram for a Charge-Steering Latch.](image)

**A. Reset phase**

This is the initial phase shown in Figure 7(a). It initializes the circuit when \( CLK_1 \) is low, \( CLK_2 \) is high and \( CLK_3 \) is high leading to \( M_5 \) and \( M_6 \) being “ON” and pre-charging the two output nodes to \( V_{DD} \) such that \( V_{out+} = V_{out-} = V_{DD} \). At the same time, \( M_9 \) and \( M_{10} \) are “OFF” and the tail capacitors \( C_T \) are discharged to GND through \( M_{11} \) and \( M_{12} \) resulting in \( V_{C_T} = 0 \), where \( V_{C_T} \) is the voltage across the tail capacitor.
B. Amplification phase

In the second phase, CLK1 turns high and CLK2 turns low while CLK3 is still high leaving all nodes at a high impedance state as shown in Figure 7(b). In this phase, the circuit acts like a differential amplifier typically as stated in section III. The steady state of the differential output is proportional to the input voltage. The gain is mainly governed by $g_{m,avg}$ like a differential amplifier typically as stated in section III. The output voltage difference is an amplified version of the input voltage difference is created by charge redistribution between the two output capacitors $C_{PL}$ and the tail capacitors $C_{T}$ while consuming little extra power consumption. At the end of this phase, the two output voltages are sitting at levels slightly higher than the voltage level $V_{min}$ as shown in Figure 6. The output voltage difference is an amplified version of the input as explained before. The small-signal output voltage at the end of the amplification phase can be given by:

$$V_{out} = g_{m,avg} R_{out} V_{in}$$  (7)

Where $g_{m,avg}$ is the average transconductance of the input pair and $R_{out}$ is the effective resistance of the switched capacitor structure resulting from charging and discharging of the load capacitors $C_{PL}$: $R_{out} = \frac{\Delta T}{C_{PL}}$. Where $\Delta T$ is the discharging time of $C_{PL}$, which equals the charging time of the tail capacitor $C_T$ to make $V_p$ rises from zero to $V_{CM} - V_{TH} - \Delta V$ where $\Delta V$ is somewhat small and arbitrary voltage. $\Delta T$ is given in (9) as:

$$\Delta T = \frac{C_T V_{CM} - V_{TH} - \Delta V}{K (V_{CM} - V_{TH}) \Delta V}$$  (8)

where $K$ is a physical constant of transistor parameters.

The output voltage at the end of the amplification phase can be given by:

$$V_{out} = 2 \times \frac{V_{CM} - V_{TH} - \Delta V}{V_{CM} - V_{TH} + \Delta V} \times \frac{C_T}{C_{PL}} \times V_{in}$$  (9)

C. Regeneration phase

The third phase shown in Figure 7(c) starts when CLK3 turns low. $M13$ turns ON, thus $M7$ and $M8$ form a cross-coupled regenerative latch with an initial condition given by the final value of the amplification phase. The differential output, hence, starts to grow exponential till it reaches its saturation limit where the upper limit is $V_{DD}$ and the lower limit is $V_{min}$. The cross-coupled devices work on regenerating the output voltage by charge redistribution between $C_T$, $C_{PL1}$ and $C_{PL2}$. Once one of the two outputs reaches $V_{DD}$ ($V_{out+}$), the regeneration operation stops and $M7$ turns “OFF” keeping ($V_{out-}$) sitting at a voltage $V_{min}$. The cross-coupled pair will prevent the lower output to be pulled high and hence preserves the regenerated output till the next reset phase.

On one hand, higher $C_T$ would lead to lower voltage levels after the charge-sharing operation taking place in the amplification phase. On the other hand, power consumption increases linearly with the $C_T$ value. In this design, a capacitance value of $30 \mu F$ is chosen which resulted in an effective voltage gain at the end of amplification phase of 2.5 and a value of $V_{min}$ equal to 40% of the supply. This proposed architecture combines the pre-amplification and the regeneration functions of a typical comparator circuit into one stage. It also relies on the concept of charge redistribution and re-using the stored charges to obtain the required output voltage at the end of each phase. The comparator is sensitive to very small input voltages at extremely high speeds by enabling the regeneration after the amplification phase is done. The circuit consumes very low power consumption since there is no direct path from $V_{DD}$ to GND after the initial reset phase.

A single-ended version of the proposed comparator is shown in Figure 8. This single-ended circuit works the same as the differential circuit with same timing scheme. A single-ended version can be used with a single-ended input where a clocked comparator is needed and will be used for comparison with the conventional StrongARM comparator.

D. Delay Analysis for the Proposed Circuit

According to the work published in [8], the total delay for the conventional StrongARM comparator is comprised of two time delays, $t_0$ and $t_{latch}$. In our proposed circuit. The delay $t_0$ represents the time taken in amplification phase which is the quarter of the clock cycle $T_x$. The delay $t_{latch}$ is the time taken by cross-coupled latch to regenerate outputs to distinct values. It is defined as the time taken to have a voltage difference at

\[ t_{latch} = \frac{T_x}{4} \]
the output ($\Delta V_{out}$) equal to $V_{DD}/2$ starting from an initial output voltage difference $\Delta V_{initial}$ from equation 9. The total delay can be given as:

\[ t_{delay} = t_0 + t_{latch} \]  \hspace{1cm} (10)

\[ t_0 = \frac{T_s}{4} \]  \hspace{1cm} (11)

\[ t_{latch} = \frac{C_{pL}}{g_{m,eff}} \ln \left( \frac{\Delta V_{out}}{\Delta V_{initial}} \right) = \frac{C_{pL}}{g_{m,eff}} \ln \left( \frac{V_{DD}/2}{V_{DD}/2} \right) \]  \hspace{1cm} (12)

Where $g_{m,eff}$ is the effective transconductance of the back to back PMOS pair.

V. CHARGE-STEERING FLASH ADC

Figure 8 shows the flash ADC architecture. 4x interleaving is used while all four channels share the reference ladder to reduce the total power consumption. Four groups of 5 GHz clocks separated by 90° phase shifts are used for the four channels. The proposed comparator is the main building block used in the ADC, it is followed by static RS latch to complete a flip-flop to successfully time the output with the clock edges. Sharing the reference ladder between the interleaved branches while keeping the kick-back noise at an acceptable level is also implemented and led to significant power reduction as well. The outputs of the four interleaved channels of Flash ADC were kept in thermometer code to be directly fed into digital signal processing (DSP) core for further digital feed-forward equalization (FFE) and/or decision-feedback equalization (DFE) according to the channel and link conditions. Moreover, This ADC can be used in a multi-standard system. It can be operated in a quarter-rate, a half-rate or a full-rate mode according to the required sampling rate. Noting that a DTLE circuit will replace the sample-and-hold circuit in each branch to equalize and sample and hold the input signal for each sub-ADC.

A. Sample-and-Hold Network

Since the analog input is changing at very high speeds, Flash ADC-comparators might samples the input at different instances due to the different types of mismatches. To understand this problem, consider a low-frequency input is introduced to the ADC, the input will almost have a constant amplitude while the array of comparators sampling it to make proper decisions. But with the case of a high-frequency input signal, its fast-varying nature and the mismatches between comparators, the input might be sampled at different instances by the different comparators and this will give wrong decisions across the comparators array.

An optional sample-and-hold circuit was designed at the beginning to buffer between input nodes and the comparators, thus isolating the input from the high input capacitance from the comparators bank. The input devices were found to have a small input capacitance and since the proposed comparator is dynamic, it already samples the input at an instance of time, so the sampling circuit is eliminated. For now, input signal could be directly fed to and sampled by the dynamic comparators banks. Usually, in ADC-based equalizers, a linear equalizer precedes the ADC. Using a discrete-time linear equalizer can merge the functions of both blocks together as explained in section II.

B. Clocking System and Buffers

For the proposed ADC, we need 3 clocks for each channel as in Figure 6 and hence we need 4 groups of these 3 clocks, each group is shifted by 90° from the other. To get these 12 clocks, there are two main thoughts, a quadrature PI or using logic operations between shifted clocks. The latter method is functional but quite inaccurate. However, we adopted it for testing and checking functionality.

Figure 10 presents the designed timing system used to provide our ADC with required 12 different clocks. A 10-GHz clock is provided from a higher level, it is introduced as a single-ended clock, this signal is buffered and inverted then injected into 2 CML latches. These 2 CML latches form together, with the shown connection, a divide-by-2 circuit. Since CML latches have non-rail-to-rail outputs, the outputs are fed into differential to single-ended CML to CMOS converters. The generated clock signals are buffered and used through NAND gates and other buffers to generate the whole 12 different clock signals. Buffers are used to be able to drive the comparators.

CML latch circuit was used to work properly with the input 10-GHz clock in a 65-nm technology. The differential to the single-ended converter with buffers are working as a CML to CMOS converter. Conventional CMOS NAND gates were adopted to generate the 75% duty cycle clocks. The buffer chain was used to generate the 25% duty cycle clocks as well and to drive the loads, the switches inside the comparators.

VI. SIMULATION RESULTS

The DTLE was simulated across a 12-inch FR4 channel, the model of the channel used is given in Figure 11. Data
was transmitted through the channel with a 20-Gb/s rate and DTLE was running on 5-GHz clocks while consuming only 0.57 mW from a 1.2-V supply. The eye diagram at the end of the channel, i.e. input of the receiver, and the eye diagram after the DTLE are shown in Figure 12. The first eye diagram is totally closed, while the latter eye diagram has a vertical eye opening of 120 mV. Since the ADC has a differential dynamic range of 600 mV<sub>pp</sub> and a common-mode input voltage of 750 mV, the DTLE needs to be followed by a programmable gain amplifier (PGA) to match the DTLE output with the dynamic range and the input common-mode voltage of the ADC. In summary, Table I compares the designed DTLE with the prior work in the literature.

The proposed 5-GHz comparator shown in Figure 5 has been designed using a digital 65-nm CMOS technology. The total power consumption of the proposed fully differential comparator is 189 µW and its single-ended version only consumes 66 µW. Simulated waveforms of clocks and outputs are shown in Figure 13. The power consumption of the single-ended topology is split into 54 µW for the reset and amplification phases and 12 µW for the regeneration phase, whereas the differential comparator consumes 163 µW and 26 µW, respectively. In this comparator, Kick-back noise level is as tiny as 1 mV because outputs of the comparator core don’t have rail to rail values.
TABLE I. DTLE PERFORMANCE COMPARISON.

| Specification                  | [1] | [10] | [11] | This Work |
|-------------------------------|-----|------|------|-----------|
| Technology                    | 130nm | 32nm | 90nm | 65nm      |
| Power Supply (V)              | 1.6  | 1.1  | 1.25 | 1.2       |
| EQ. Architecture             | Inductive-Loaded CTLE | CTLE + -ve C Bandwidth Extension | CTLE | Quarter-Rate DTLE |
| Data Rate (Gb/s)              | 10   | 12.5 | 8    | 5 (per channel) |
| Channel Loss (dB)             | 18   | 32   | N/A  | 12        |
| Gain @ Nyquist (dB)           | N/A  | 10 (Input Stage + 2-CTLE Stages) | N/A | 20        |
| Power (mW)                    | 41   | 5.25 | 2.32 | 0.57*     |

*for a single DTLE

Clock buffers have been designed to drive switches and comparators. The capacitive loading per branch is 160 fF. The power consumption of clock buffers for each interleaved branch is 1 mW. This gives a total power consumption of 4 mW for the clock buffers of the whole ADC. The designed 4-bit 20-GS/s flash ADC has a total power consumption of 15.5 mW. A breakdown of the power consumption of different blocks is given in Table III. Figure 14 shows the frequency response for the ADC output for sinusoidal inputs at 4.84 GHz and 9.84 GHz input frequencies while sampling at an effective frequency of 20 GHz. For the 9.84-GHz input frequency, Table IV summarizes the performance of the whole ADC.

Figure 15 shows the resulting ENOB versus input frequency. It shows a peak ENOB of 3.9 bits at 7.66 GHz input signal.

Small kick-back noise levels allow us to increase the used values of resistors in reference ladder, hence low power consumption for the ladder. DNL and INL for the ADC are shown in Figure 16 and Figure 17 respectively.

Table V shows a detailed comparison between this work and recently published ADCs, it shows that our proposed ADC is the best in class when compared to other high-speed ADCs.

Monte-Carlo simulation for the offset shows that the input-referred offset sigma of the comparator is 14.4 mV. The input-referred offset sigma of the input devices only is found to be 13.9 mV contributing to 97% of the total input-referred offset. This means that contribution of the newly added embedded regenerative latch is negligible when referred to the input. Keeping this in mind, making the input pair larger will drop down the input-referred offset significantly.

A detailed comparison between the single-ended topology and a conventional StrongARM comparator is shown in Table II. The conventional StrongARM is known to be a low-power structure. For comparison purposes, the input pair dimensions are kept equal between the two designs.

TABLE II. COMPARISON BETWEEN THE PROPOSED COMPARATOR AND STRONGARM COMPARATOR AT 5 GHz.

| Comparison Point                  | StrongARM | This work |
|-----------------------------------|-----------|-----------|
| Power consumption (µW)            | 256       | 66 (189 for diff-ended) |
| Max. speed for 5 mV input (GHz)   | 5         | 6         |
| Sensitivity at 5 GHz clock (mV)   | 4         | 1         |
| 3-Sigma Offset (w/o the input pair) (mV) | 11.16 | 0.5       |

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Figure 18 shows the FFT for the output of the whole ADC after parasitic extraction (PEX) working with the highest targeted speed of 20 GS/s. The Flash ADC with its clocking
TABLE III. POWER CONSUMPTION BREAKDOWN.

| Component       | Power Consumption |
|-----------------|-------------------|
| Ref. ladder     | 200 µW            |
| Comparators     | 11.34 mW          |
| Clock buffers   | 4 mW              |
| Total Power     | 15.5 mW           |

Fig. 14. Frequency Response of Output for Sinusoidal Inputs of 4.84 GHz and 9.84 GHz Input frequencies.

TABLE IV. THE DESIGNED ADC PERFORMANCE SUMMARY.

| Parameter                        | Value             |
|----------------------------------|-------------------|
| Sampling frequency               | 20 GS/s           |
| Input Range                      | 600 mV_{diff}     |
| SFDR                             | 33.58 dB          |
| SNDR                             | 23.86 dB          |
| ENOB (for 9.84 GHz input frequency) | 3.67 Bits        |
| Power at Nyquist frequency       | 15.5 mW           |
| FOMW*                            | 60.8 fJ/conv-step |

* FOMW = \frac{\text{Power}}{\text{Sampling rate} \times 2^{\text{ENOB}}}

Fig. 15. ENOB Vs. Input Frequency.

Fig. 16. DNL of the ADC.

Fig. 17. INL of the ADC.

Fig. 18. The Spectral Density of the Extracted-ADC Output.

Fig. 19. Layout of the ADC.

system and a testing current steering digital to analog converter (DAC) were laid-out in a total silicon area of 307µm*124µm. The layout is as shown in Figure 19.

VII. CONCLUSION

Charge-steering concept is an excellent candidate for high-speed circuits used in analog-mixed signal systems with low power requirements. It proves an advantageous usage over the current-steering traditional concept, as well as the conventional StrongARM comparator architecture. Charge-steering is used in this paper to design an ultra-low power, 189-µW 5-GHz charge-steering comparator. The proposed idea uses an embedded regenerative latch which is only enabled after the amplification cycle is completed. The input referred offset of this extra latch is negligible compared to the input pair
TABLE V. COMPARISON BETWEEN THIS WORK AND RECENTLY REPORTED FLASH ADCS.

| Item                     | [12] | [13] | [14] | This work |
|--------------------------|------|------|------|-----------|
| Process                  | 32-nm CMOS | 40-nm CMOS | 130-nm SiGe | 65-nm CMOS |
| Power (mW)               | 69.5 | 500  | 3000 | 15.5      |
| Bits                     | 6    | N/A  | 5    | 4         |
| Sample rate (GS/s)       | 20   | 25   | 22   | 20        |
| SNDR (dB)                | 30.7 | 25.8 | 20   | 23.86     |
| FOM$W^*$ (fJ/conversion-step) | 172.3 | 1255.8 | 16695.8 | 60.8      |

* $FOMW = \frac{\text{Power}}{\text{Sampling rate} \times 2^{\text{ENOB}}}$

offset contribution. Furthermore, the proposed comparator is used to build a 4-bit 4x time-interleaved Flash ADC that works on 20 GS/s sampling rate. ADCs were used to be the bottleneck of the ADC-based receivers. With the ADC designed in this work, ADC’s power consumption was as low as 15.5 mW, the thing that paves the way and relieves the burden facing the ADC in the high-speed designs. Moreover, the ADC was preceded by a modified version of a continuous-time linear equalizer, this modified version is called discrete-time linear equalizer (DTLE) and it merges a CTLE with a sample-and-hold network. This equalizer is used after a 12-inch FR4 channel to open the eye diagram of the received signal and enables it to be processed by the ADC and the digital equalizers in a DSP core after that.

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