Design and manufacture of lock-in amplifier

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Abstract. This design realizes the excellent performance of lock-in amplifier in detecting weak signal, which is composed of signal conditioning circuit and MCU control module. The single chip microcomputer is used to control the AD sampling of the filtered DC component after multiplication operation, and the FPGA is used to realize the phase shift control. Finally, the amplitude of the signal to be measured can be obtained by eliminating the gain generated in the whole circuit with the measured amplitude. After testing, it has the advantages of high sensitivity, high input impedance and low noise, and can realize accurate measurement.

1. Background and significance of the project

Since the advent of lock-in amplifier, it has shown superior performance in weak signal detection, and has been widely used in various fields of scientific research. In the era of Internet of things, lock-in amplifier has great application space for sensor design, which can improve the accuracy of sensor detection signal, so as to simplify the design, make the sensor smaller and smaller, and make the Internet of things technology more stable.

The lock-in amplifier can suppress the noise to a great extent. Firstly, the spectrum of the DC or slowly varying signal is transferred to the modulation frequency by the modulator to amplify, so as to avoid the adverse effect of 1/F flicker effect noise. Secondly, the phase sensitive detector is used to demodulate the modulated signal, and the frequency and phase are used for detection. Because the noise and signal are difficult to achieve the consistency of frequency and phase, the interference of noise signal can be greatly reduced after passing the low-pass filter with good performance, the weak original signal can be obtained, and then the measurement can be obtained through amplification, analog-to-digital conversion and curve fitting. In order to facilitate our research and analysis of various aspects.

2. Circuit design and simulation

2.1 System design objectives

A lock-in amplifier is designed and manufactured to detect the amplitude of weak sine wave signal and display the effective value of the amplitude digitally.

The indicators to be achieved are as follows:

- External signal source provides sine wave signal with frequency of 1kHz, which is input to R (T) end of reference signal, and R (T) is connected to s (T) end through resistance voltage dividing network. The effective value of S (T) amplitude is 10 μV ~ 1mV.
The reference channel output signal $R(T)$ can be continuously or step-by-step phase shifted relative to the reference signal $R(T)$.

At the output end of the lock-in amplifier, a circuit is designed to measure and display the $S(T)$ amplitude RMS value of the measured signal.

When the adder is used to add a noise with a frequency of 1050Hz, the influence of noise signal $n(T)$ on $S(T)$ should be reduced as far as possible, and the error is less than 10%.

When the amplitude of $n(T)$ is increased to 10$s(T)$, the measurement error of $S(T)$ rms of lock signal amplifier is less than 10%.

2.2. System design

According to the design requirements and the principle of lock-in amplifier, the design is detailed as shown in the figure 1.

![Figure 1. overall system structure and parameters of each module](image)

The input signal $R(T)$, through the resistance divider network, the weak signal $s(T)$ is obtained. The effective value range of the control input signal is between 10mV ~ 1V, and the weak signal whose amplitude RMS is between 10μV ~ 1mV can be obtained after 1000 times of partial voltage.

Because of the small signal, it is difficult to carry out phase sensitive detection, so low noise amplification is carried out first. The $S(T)$ is amplified 100 times by the AC amplifier with ina128 as the core, and then frequency selection, noise reduction and 7.5-fold amplification are realized by band-pass filter. The signal $x(T)$ with magnification of 750 is obtained.

$R(T)$ enters the reference channel and changes into square wave signal through comparator. Then, the amplitude of square wave signal is raised to 0 ~ 5V by boosting voltage, so as to facilitate FPGA phase shifting. The phase shift control is realized by single chip microcomputer, and the signal $R(T)$ is obtained.

The DC signal is obtained by modulating $x(T)$ and $R(T)$ with phase sensitive detector. Then through the low-pass filter, filter out the AC, pure DC. Then it is amplified by DC amplifier, and finally sampled and calculated by MCU, and the effective value of signal $s(T)$ to be measured is displayed.

2.3. Design and Simulation of each module

- Front stage amplifier module

Because one of the design specifications is to increase the interference signal of 1050Hz, and the bandwidth of the band-pass filter is 200Hz, the noise can enter the analog switch through the band-pass filter. If the amplification ratio of the front stage is large, the noise amplitude will be greatly increased at the same time, which will cause great interference to the amplitude of the measured signal and affect the measurement accuracy. Therefore, the amplification factor of the front stage amplifier circuit should not be too large. In this design, the amplification factor of the front stage amplifier circuit is set as 100 times, which can better reduce the influence of interference on the measurement signal.

- Bandpass amplifier module
The bandpass amplifier module uses tl084 chip, which is more common, easy to buy and cheap; it uses two-stage filter, the center frequency is 1kHz, and the bandwidth is 200Hz; and the inverse amplifier is used, and the simulation gain is 19.61db.

- Square wave generation module

The zero crossing comparator also uses tl084 to convert the sine wave into square wave, and then uses the voltage follower to isolate the influence of the comparator on the following level raising circuit. The level raising circuit raises the voltage amplitude to 0 ~ 5V, and sends the square wave signal to FPGA.

- Phase sensitive detection module

In this part, CD4053 analog switch is used, and the square wave signal output by FPGA is used to control the switch on and off, and the output signal amplitude is all above 0. After passing through the low-pass filter, only the DC component is left.

These switching circuits have very low static power consumption in the whole vdd-vss and vdd-vee power supply ranges, and are independent of the logic state of the control signals. When INH input = 1, all channels are cut off. When the control input is high level, "0" channel is selected, otherwise, "1" channel is selected. The truth table is shown in Table 1.

| CD4053 truth table |
|---------------------|

| INPUT STATES TRUTH TABLE | “ON” CHANNELS “OPEN” PASSAGEWAY |
|--------------------------|---------------------------------|
| INHIBIT prohibit | C       | B | A | CD4051B | CD4052B | CD4053B |
|---------------------|---------|---|---|---------|---------|---------|
| 0 0 0 0 | 0       | 0 | 0 | 0X,0Y   | cx, bx, ax |
| 0 0 0 1 | 1       | 0 | 1 | 1X, 1Y  | cx, bx, ay |
| 0 0 1 0 | 2       | 0 | 2 | 2X, 2Y  | cx, by, ax |
| 0 0 1 1 | 3       | 1 | 3 | 3X, 3Y  | cx, by, ay |
| 0 1 0 0 | 4       | 0 | 4 |    | cy, bx, ax |
| 0 1 0 1 | 5       | 1 | 5 |    | cy, bx, ay |
| 0 1 1 0 | 6       | 0 | 6 |    | cy, by, ax |
| 0 1 1 1 | 7       | 1 | 7 |    | cy, by, ay |
| 1 * * * | NONE    | NONE |

- Low pass filter part

Low pass filter mainly rectifies the output signal of correlator. The third-order filter is used to reduce the bandwidth of the low-pass filter to less than 1 Hz. Although the gain is 0, the gain remains unchanged within 0.5 Hz.

- Software circuit part

The software circuit mainly completes FPGA control, LCD display, A/D conversion and keyboard control, which is completed by msp430f5438a.

The main program block diagram is shown in the figure 2.
The 240 * 320 dot matrix color LCD screen is selected as the LCD screen, and the data reading mode of the screen is UART mode, which not only improves the utilization rate of I/O port, but also improves the reaction rate of the screen.

- **A/D conversion module**
  The function of A/D conversion part is to complete the measurement of signal amplitude, get the effective value and display it on the screen. Msp430f5438a itself contains a 12 bit A/D, the measurement frequency is about 1kHz, the use of A/D module of MCU can fully achieve the design target. If it is necessary to improve the sampling accuracy, an ads1118 chip can be used for 16 bit sampling.

- **General circuit diagram and PCB diagram**
  The PCB diagram is shown in the figure 3.

![Figure 3. 11 PCB diagram](image)

### 3. Test plan and test results
The output waveform of DC amplifier is tested, and the performance of low-pass filter and DC amplifier is detected by output waveform, the result is shown in Table 2.

| Table 2. Test Result |
|----------------------|
| The value of S (T) without noise | The value of S (T) with noise |
| range | Display value | error | Noise ratio | Frequency(Hz) | error |
|-------|---------------|-------|-------------|---------------|-------|
| 10μV | 0.010mV       | 0%    | 1:1         | 1050          | 0.5%  |
| 1mV  | 1.013 mV      | 1.3%  | 1:1         | 2000          | 0%    |
|       |               |       | 1:10        | 1050          | 0.2%  |
|       |               |       | 1:10        | 2000          | 2.5%  |

Analysis of test results: when there is no noise and the noise is increased by 1 or 10 times, the system can effectively measure the effective value of voltage, and the error is within 5%, which meets the design index.

4. Conclusion
This design is a mixed circuit of single chip microcomputer and analog circuit. We carefully analyze and select the most suitable module for this design from the perspective of cost and implementation difficulty. Because of the reasonable design of the system architecture, the realization of the functional circuit is better, the system performance is excellent and stable. The micro signal measurement is successfully realized, and all the indicators meet the requirements and are improved.

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