Abruptly-Switching MoS$_2$-Channel Atomic-Threshold-Switching Field-Effect Transistor With AgTi/HfO$_2$-Based Threshold Switching Device

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ABSTRACT

A two-dimension (2D) atomic-threshold-switching field-effect transistor (ATS-FET) was implemented, by connecting an AgTi/HfO$_2$-based threshold-switching (TS) device in series to the drain electrode of the 2D baseline-FET with molybdenum disulfide (MoS$_2$) channel material. We optimized/developed the Ag/HfO$_2$-based TS device because its characteristic is associated to the way to achieve high performance of the 2D ATS-FET. By reducing the effective device area of the Ag/HfO$_2$-based TS device down to 4 $\mu$m$^2$, low threshold voltage ($V_T \sim 0.42$ V), low threshold current ($I_{T, \text{drain current at the threshold voltage}} \sim 3.79 \times 10^{-11}$ A), and low $V_T$ variation ($\sim 0.09$ V) were achieved. This is because the randomly formed filaments and electric field are better controlled with the scaled effective area. Next, the titanium (Ti)-injection barrier layer was inserted between the top electrode and the switching layer, while maintaining the optimized area in the TS device. The inserted Ti-injection barrier layer prevents the migration of Ag ions into the switching layer, enabling the stable TS operation even under the compliance current of 100 $\mu$A. Additionally, it locally restricts the region where the filaments are created inside the switching layer, resulting in a 17% lower $V_T$ variation and stable $I_T$ to approximately $\sim 1.5 \times 10^{-11}$ A in 100 cycles. Due to the low off-state leakage current and low variation characteristic of the optimized AgTi/HfO$_2$-based TS device, the 2D ATS-FET (vs. 2D baseline-FET) shows the reduction of off-state leakage current (by $\sim 10^2$ in sub-threshold region) and the stable switching characteristic. The proposed 2D ATS-FET shows stably steep switching characteristics, e.g., sub-threshold swing under forward bias ($\sim 19$ mV/decade) and reverse bias ($\sim 26$ mV/decade), because of its abruptly switching characteristics of the TS device.

INDEX TERMS

Atomic threshold switching, threshold switching device, 2D ATS-FET.

I. INTRODUCTION

The power density of the state-of-the-art complementary metal oxide semiconductor (CMOS) devices in an integrated circuits has been increased for the past few decades, and it is one of the key factors in evaluating/developing the integrated circuit devices. In reality, the development process of the CMOS technology platform puts emphasis on implementing energy-efficiency in CMOS devices. However, the sub-threshold swing ($SS = dV_g/d\log I_d$, i.e., the gate voltage required to increase the drain current by ten times in sub-threshold regime, in the unit of mV/decade) of conventional metal oxide semiconductor field-effect transistor (MOSFET) is limited to 60 mV/decade at room temperature due to the thermionic carrier injection mechanism. The lowest limit of SS has caused to exponentially increase...
the off-state leakage current with monotonically decreasing the threshold voltage, and thereby, it is difficult to control the passive power consumption in integrated circuit (IC) [1].

An effective way to overcome the scaling limit has been suggested with various solutions in the material and device community. On one hand, in order to lower the off-state leakage current, molybdenum disulfide (MoS2), a two-dimensional (2D) transition metal dichalcogenides (TMDCs), has received lots of attention as one of the new channel materials in MOSFET. The conspicuous features of MoS2 are its low dielectric constant and high electron-effective mobility [2]–[4]. On the other hand, various types of steep slope device structures have been proposed, such as tunnel FET (TFET), impact ionization MOS (I-MOS), negative capacitance FET (NCFET), feedback FET, and atomic-threshold-switching FET (ATS-FET) [5]–[16]. Among them, ATS-FET has attracted considerable attention because it shows (i) abrupt steep-switching characteristics (i.e., a significant reduction in SS), (ii) significant suppression in off-state leakage current, and (iii) low drive voltage. The ATS-FET consists of a threshold switching (TS) device (which is independently connected/added to one of the electrodes in the transistor) plus a conventional baseline-FET. Since a high off-state leakage current of the ATS-FET can be suppressed due to the high resistance of the TS device, the investigation on the TS device is necessary.

A 2D phase-FET with vanadium dioxide (VO2) was proposed. However, the VO2-based 2D phase-FET has problems, e.g., high off-state leakage current, and high drive voltage [17], [18]. This is because the connected/integrated VO2-based TS device has a low off-state resistance \( R_{\text{off}} \sim 10^6 \ \Omega \) and a high threshold voltage \( V_T \). For these reasons, a hafnium dioxide (HfO2)-based resistive switching device has been demonstrated as a new class of TS device that can form unstable conductive filaments through compliance with current control (note that the filaments are formed and ruptured by applying a critical voltage). Compared with the VO2-based insulator-metal-transition device, the HfO2-based TS device can contribute to suppress the off-state leakage current as well as to lower the operating voltage of 2D ATS-FET because of its high off-state resistance \( R_{\text{off}} \sim 10^9 \ \Omega \) and low \( V_T \) [19], [20]. However, this type of device has problems, i.e., \( V_T \) variation, leakage issue due to the filament that is randomly formed in the switching layer of the TS device. In reality, the electrical performance of the ATS-FET with HfO2-based TS device is degraded due to the problems mentioned above.

In this work, the Ag/HfO2-based TS device is optimized by adjusting/reducing the effective device area. Note that a crossbar array pattern is used to adjust the effective device area. By scaling the effective device area from \( 8 \times 8 \ \mu m^2 \) to \( 2 \times 2 \ \mu m^2 \), the randomly formed filaments and electric fields were better controlled. As a result, the \( V_T \) variation of the TS device was significantly suppressed from \( \sim 0.76 \ \text{V} \) to \( \sim 0.09 \ \text{V} \), and the average value of \( V_T \) decreases from \( \sim 0.92 \ \text{V} \) to \( \sim 0.46 \ \text{V} \). Besides, the off-state leakage current decreases from \( \sim 3.65 \times 10^{-9} \ \text{A} \) to \( \sim 10^{-11} \ \text{A} \). Moreover, a stable TS device operation was implemented by inserting the Ti-injection barrier layer between the Ag top electrode and the HfO2 switching layer. Inserting a barrier layer prevents the injection of active metal ions, enabling the stable TS operation even under high compliance current conditions (e.g., under 100 \( \mu \text{A} \)). Finally, the 2D ATS-FET was built by connecting an AgTi/HfO2-based TS device to the drain electrode of 2D baseline-FET. The off-state leakage current of proposed 2D ATS-FET (vs. 2D baseline-FET) was suppressed by \( \sim 10^2 \) in the sub-threshold region and exhibited stable abrupt switching characteristics.

II. DEVICE DESIGN AND FABRICATION

Both a baseline-FET with MoS2 channel material and a TS device with AgTi/HfO2 material were fabricated separately, and then they were interconnected to construct the 2D ATS-FET. The baseline-FET is fabricated as follows: First, a 90 nm-thick SiO2 on Si substrate was thermally grown. Thereafter, the back-gate of 5 nm-thick Ti/15 nm-thick Au on the SiO2 layer was deposited and patterned by lithography, e-beam evaporation, and lift-off processes. Then, a 20 nm-thick Al2O3 gate oxide was deposited by atomic layer deposition (ALD). The channel layer of MoS2 was transferred onto the gate oxide by exfoliation method and dry-transfer machine. Afterward, using an e-beam evaporator, the source/drain electrodes of 15 nm-thick Ti/65 nm-thick Au were deposited/patterned on the MoS2 channel. The channel length and width of the fabricated 2D baseline-FET were 7.918 \( \mu m \) and 10.128 \( \mu m \), respectively.

Next, the TS device was fabricated in a crossbar-shaped structure, for the purpose of device isolation. The AgTi/HfO2-based TS device was fabricated as follows: First, SiO2 on Si substrate was thermally grown. Thereafter, the bottom electrode of 10 nm-thick Ti and 50 nm-thick Pt was deposited/patterned on the SiO2 layer, using e-beam evaporation. The 6 nm-thick HfO2 (i.e., switching layer of TS device) was deposited at 300 °C by ALD. To limit the switching area of the deposited HfO2, wet etching was performed for 1 minute, using 6:1 buffer-oxide-etchant (BOE). Then, the top electrode of 3 nm-thick Ti / 50 nm-thick Ag was deposited/patterned on the etched switching layer, using an e-beam evaporator. The areas of the patterned device were \( 2 \times 2 \ \mu m^2 \), \( 4 \times 4 \ \mu m^2 \), and \( 8 \times 8 \ \mu m^2 \).

Lastly, to fabricate an ATS-FET, the HfO2-based TS device was connected in series to the drain side of the baseline-FET via gold wire [see Fig. 1(a)]. An optical image of AgTi/HfO2-based TS devices in the crossbar-shaped structure is shown in Fig. 1(b).

When it comes to devices characterization, the Keithley 4200-A SCS semiconductor parameter analyzer was used to measure the electrical characteristics of the devices at room temperature. Note that the compliance current (which can limit the current flow between electrodes) was
set to $10^{-5} \sim 10^{-4}$ A, in order to realize threshold switching properties.

### III. RESULTS AND DISCUSSION

#### A. THE OPERATING PRINCIPLE OF ATS-FET

Fig. 1(c) shows the equivalent circuit of the drain-configuration ATS-FET (i.e., TS device connected/integrated in series to the drain side of the baseline-FET). The baseline-FET of the proposed ATS-FET follows the drain current ($I_D$) equation as below:

$$I_D = \frac{W}{L} \mu_{\text{eff}} C_{\text{ox}} \left( (V_{\text{GS}} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right)$$

The details of each parameter used in the $I_D$ equation above are as follows:

i. Gate-source voltage of ATS-FET ($V_{\text{GS}}$)
ii. Drain voltage of baseline-FET ($V_{\text{DS}}$) ($D'$ indicates the drain side internal node of ATS-FET)
iii. Drain voltage of ATS-FET ($V_{\text{DS}}$)

The operation of the ATS-FET can be understood with the resistive network of two variable resistors, i.e., the channel resistance of the baseline-FET ($R_{\text{CH}}$) and the resistance of the TS device ($R_{\text{TS}}$). The applied $V_{\text{DS}}$ is divided into $R_{\text{CH}}$ and $R_{\text{TS}}$. Once $V_{\text{GS}}$ increases, $R_{\text{CH}}$ decreases, so that the applied $V_{\text{DS}}$ is mostly dropped across the TS device.

When the voltage across the TS device ($V_{\text{TS}}$) becomes higher than its threshold voltage ($V_{T,TS}$), metal ion filaments are formed in the TS device, resulting in the resistance transition from a high-resistance state to a low-resistance state), the TS device turns on. In detail, as shown in Fig. 1(d), the ATS-FET operation can be divided into two cases (i.e., $V_{\text{GS}} < V_T$ or $V_{\text{GS}} > V_T$). Initially, at $V_{\text{GS}} < V_T$ (before the abrupt switching point of the ATS-FET), most of the applied $V_{\text{DS}}$ is dropped across the TS device due to the high off-state resistance of the TS device ($V_{\text{TS}} < V_{T,TS}$, i.e., the TS device is in a turn-off state). Accordingly, $V_{\text{DS}}$ is reduced, and the off-current state of the ATS-FET is suppressed. In this case, $I_D$ is constructed as follows:

$$V_{\text{DS}} = V_{\text{DS}} + V_{\text{TS}}, \quad V_{\text{GS}} \uparrow, \quad V_{\text{DS}} \downarrow$$

and therefore,

$$V_{\text{DS}} \approx 0 \quad (V_{\text{TS}} < V_{T,TS})$$

$$I_D \approx 0$$

At $V_{\text{GS}} > V_T$, abrupt switching occurs in the ATS-FET. When $V_{\text{GS}}$ that can sufficiently reduce $R_{\text{CH}}$ is applied, most of the applied $V_{\text{DS}}$ that the TS device can turn-on is dropped.
across the TS device ($V_{TS} > V_{T,TS}$). At this moment, the negative-differential-resistance (NDR) effect occurs due to the resistance state transition of the TS device. This causes a voltage drop as much as $\Delta V_{NDR}$ in the TS device, and therefore, the voltage amplification ($V_{CH} + \Delta V_{NDR}$) in the channel of baseline-FET is happened. As a result, an abruptly switching characteristic occurs in the ATS-FET, which can be used to implement a high device performance in the sub-threshold regime (even beyond the sub-threshold region). Then, $I_D$ is constructed as follows:

$$V_{DS} \approx V_{DS}(V_{TS} > V_{T,TS})$$

$$I_D = \frac{W}{L} \mu_{n, eff} C_0 (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2$$

The circuit schematic of the NDR effect due to the resistance transition is illustrated in Fig. 1(e).

**B. THE OPERATING PRINCIPLE OF TS DEVICE**

Based on the formation and rupture of metal ion filaments by active metal ion migration, the resistive switching device with active metal (i.e., Ag, Cu) ions works. Herein, the device can have non-volatile [i.e., memory switching (MS)] and volatile [i.e., threshold switching (TS)] switching characteristics, depending on the compliance current level (i.e., the on-state current flow between the top electrode and bottom electrode). Fig. 2(a) depicts an illustration of the MS characteristics. When the set voltage ($V_{SET}$, a specific voltage that forms metal ion filaments in a non-volatile resistive switching device) is applied to the top electrode of the resistive switching device without compliance current, the active metal ion filaments are stably formed in the switching layer (turn-on). Afterward, even when the applied voltage reaches to 0 V, the filaments are maintained, and therefore, the device shows MS characteristics (i.e., conductive-bridge random access memory). To rupture the stably formed filaments, the reset voltage ($V_{RESET}$, dissolving metal ion filaments in a non-volatile resistive switching device) should be applied to the top electrode (turn-off). Fig. 2(b) depicts an illustration of the TS characteristics. When the $V_T$ (i.e., the critical voltage for the transition from the high-resistance state to low-resistance state) is applied to a resistive switching device with a compliance current, the filaments are unstably formed in the switching layer. Compared against the devices with MS characteristics, the unstably formed filaments are ruptured at a positive hold voltage ($V_{H}$, the critical voltage for the transition from low-resistance state to high-resistance state). This is because the maximum current flow through the device is restricted by the compliance current, i.e., the filaments are easily transformed into small clusters of active metal atoms [21].

**C. EFFECT OF USING VARIOUS DEVICE AREAS**

The abrupt SS and low off-state leakage current of ATS-FET are attributed to the high performance of the TS device. In particular, the lower the off-state current and drive voltage of the TS device is, the lower the off-state current and drive voltage of the ATS-FET is. Thus, it is important to design and fabricate a TS device with excellent switching characteristics.
a critical electric field (i.e., the electric field which can form the local area). Finally, regarding the $I_T$ variation, the device with a large area, the electric field is more widely distributed in the local area. Therefore, the electric field is significantly lowered due to the enhanced electric field in the filament formation decreases locally, and thereby, $V_T$ can be significantly lowered due to the enhanced electric field in the local area. Finally, regarding the $I_T$, it is observed that the device with the area of $2 \times 2 \mu m^2$, $4 \times 4 \mu m^2$, and $8 \times 8 \mu m^2$ shows the average $I_T$ of $\sim 3.79 \times 10^{-11} A$, $\sim 1.68 \times 10^{-11} A$, and $\sim 3.65 \times 10^{-9} A$, respectively. Since the electric field is more widely distributed within the switching layer of a larger-area TS device, the leakage current path increases. As a result, the $I_T$ of the TS device with the area of $64 \mu m^2$ increased [see Fig. 3(c) and 3(e)].

The small $V_T$ variation, low $V_T$, and low leakage current characteristics of the TS device are necessary to construct a high-performance ATS-FET. Hence, among the TS devices of various areas, the $4 \mu m^2$ Ag/HfO$_2$-based TS device is the most suitable for ATS-FET.

D. EFFECT OF USING “INSERTED” Ti LAYER
The Ag/HfO$_2$-based TS device has excellent switching performance (e.g., low $V_T$, high off-state resistance).
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FIGURE 4. (a) Effect of compliance current on the Ag/HfO$_2$-based TS device’s operation. The TS device shows the MS characteristic under the compliance current of 50 µA. (b) Effect of compliance current on the AgTi/HfO$_2$-based TS device’s operation. The TS device shows the TS characteristic under the compliance current of 100 µA. (c) Measured current versus voltage of the AgTi/HfO$_2$-based TS device. Note that the I-V measurement was repeated ten times, and those ten different I-V curves are drawn together in each figure. (d) Variation of the threshold current of AgTi/HfO$_2$-based TS device. (e) Comparison of threshold voltage distribution for two different top electrode materials. Note that the threshold voltage variation is approximately suppressed with AgTi top electrode material, by ∼17%.

However, it does not show its stable TS operation under high-compliance current condition. Fig. 4(a) shows the effect of compliance current on the device operation. 4 µm$^2$ Ag/HfO$_2$-based TS device exhibits its MS characteristic under 50-µA compliance current condition. This is because Ag ions are excessively injected from the top electrode into the HfO$_2$ switching layer by the electric field. To operate an ATS-FET at a high on-state current, the TS device must exhibit stable TS performance under high-compliance current conditions. Therefore, in this work, a Ti-injection barrier layer with low Ag ion diffusivity is inserted between the top electrode and the HfO$_2$ switching layer, to control Ag injection [24]–[26]. Generally, a TS device with the Ti-injection barrier layer of 3 nm thickness (or thicker) causes an increase in $V_T$ [24]. In order to implement excellent switching characteristics (i.e., low $V_T$ condition), a TS device with a 3 nm-thick Ti-injection barrier layer was fabricated. In Fig. 4(b), the effect of the compliance current level on the TS device with the Ti-injection barrier layer is shown (see the measured current versus voltage). Under 100-µA compliance current condition, the 4 µm$^2$ AgTi/HfO$_2$-based TS device operates reliably with the TS characteristic [21]. Fig. 4(c) shows the measured current versus voltage of 4 µm$^2$ AgTi/HfO$_2$-based TS device. The current of the TS device is stably maintained, as shown in Fig. 4(d). As a result, this TS device has the average value of $I_T$, $\sim 1.5 \times 10^{-11}$A, and it performs a stable TS operation. Additionally, the $V_T$ variation of the TS device is well suppressed/decreased by 17%, compared to the 4 µm$^2$ Ag/HfO$_2$-based TS device [see Fig. 4 (e)], because this device with a Ti-injection barrier layer can form the conductive filaments only in the localized region inside the switching layer. Therefore, 4 µm$^2$ AgTi/HfO$_2$-based TS device with excellent performance (i.e., low off-state current, low $V_T$ variation, and stable TS operation) can be used to build up the 2D ATS-FET.

E. CHARACTERISTIC OF 2D ATS-FET

The 2D ATS-FET is fabricated by connecting the AgTi/HfO$_2$-based TS device in series to the drain side of the 2D baseline-FET. Fig. 5(a) shows the measured drain current versus gate voltage ($I_D$-$V_G$) characteristic of the baseline-FET vs. 2D ATS-FET at $V_D$ of 0.5 V. The average off-state leakage current of a 2D baseline-FET (see the blue-colored one) at the gate voltage of $\sim 3$ V to $\sim 2.5$ V is $\sim 2.2 \times 10^{-10}$ A/µm. At the same gate voltage, the 2D ATS-FET (see the purple-colored one) has the average off-state leakage current of $\sim 4.41 \times 10^{-12}$ A/µm. This is because the high off-state resistance of the connected AgTi/HfO$_2$-based TS device can effectively reduce the off-state current of the 2D ATS-FET. From the result, the off-state leakage current of the 2D ATS-FET was decreased by $\sim 10^2$, compared to that of the 2D baseline-FET. Both the 2D baseline-FET and 2D ATS-FET show the average on-state current of $\sim 1.03 \times 10^{-7}$ A/µm and
FIGURE 5. (a) Measured drain current versus gate voltage of the 2D baseline-FET versus 2D ATS-FET with AgTi/HfO$_2$-based TS device. Note that the drain voltage is set to 0.5 V. (b) Measured input transfer characteristics of the 2D ATS-FET. Note that the I$_D$-V$_G$ measurement was repeated for 10 cycles, and those 10 different I$_D$-V$_G$ curves are drawn together in the figure. (c) The measured sub-threshold slopes of the 2D ATS-FET under forward or reverse bias condition at 300 K.

TABLE 1. Comparison of this work TO THE other 2D ATS-FETS.

| 2D ATS-FETs | 2017 VLSI [18] | 2018 APL [27] | 2019 AML [17] | This work |
|--------------|----------------|----------------|----------------|------------|
| TS device material | VO$_2$ | Ta$_2$O$_5$ | VO$_2$ | Al$_2$O$_3$ |
| Channel material | MoS$_2$ | MoS$_2$ | WSe$_2$ | MoS$_2$ |
| Drain Voltage | 8 V | higher than 4 V | 10 V | 0.5 V |
| Sweep range of gate voltage | -50 V ~ -40 V | higher than 5 V | -60 V ~ -60 V | -3 V ~ 0 V |
| SS$_{min}$ (mV/decade) | N/A | N/A | N/A | 19 (Forward) 26 (Reverse) |
| Off-state current (A) | $\sim 10^{-6}$ | $2 \times 10^{-6}$ | $2.7 \times 10^{-6}$ | $3.6 \times 10^{-6}$ |
| EOT | 90 nm | 9 nm | NA | 8.7 nm |

$\sim 8.63 \times 10^{-8}$ A/$\mu$m at the gate voltage of $-0.5$ V to 0 V, respectively. Although the on-state drive current of 2D ATS-FET is slightly lower, the off-state leakage current in the sub-threshold region (i.e., the region before the abrupt switching is occurred) was effectively controlled. Thereby, the on/off-current ratio of the 2D ATS-FET is improved by $\sim 38$ times. Fig. 5(b) shows the measured I$_D$-V$_G$ characteristics of 2D ATS-FET in 10 cycles. Since the AgTi/HfO$_2$-based TS device exhibits the stable characteristics of V$_T$ variation, it demonstrates excellent switching performance in the 2D ATS-FET. The SS distributions (i.e., forward SS or reverse SS) of the 2D ATS-FET at 10 cycles are shown as box-and-whisker plots in Fig. 5(c). The minimum value of SS (SS$_{min}$) in the forward and reverse sweeps is $\sim 19$ mV/decade and $\sim 26$ mV/decade, respectively. Meanwhile, the average SS value of baseline-FET is $\sim 300$ mV/decade at the gate voltage of -2.1 V to -1.6 V. When the voltage applied to the TS device exceeds V$_T$, an abrupt switching of 2D ATS-FET occurs because the voltage across the TS device is dropped below V$_H$. Owing to the abrupt switching operation of the TS device, the SS of the 2D ATS-FET is reduced below the theoretical limit (i.e., 60 mV/decade) at 300 K. Additionally, the 2D baseline-FET and 2D ATS-FET in this work (compared against the other groups’ 2D-material-based FETs) have demonstrated a ultra-low gate voltage sweep of $-3$ V $\sim +0$ V (see Table 1 for benchmark results). This is because it has a low equivalent oxide thickness (EOT) of $\sim 8.7$ nm, using Al$_2$O$_3$ as the gate dielectric material for the 2D baseline-FET. Also, due to the optimized AgTi/HfO$_2$-based TS device, the 2D ATS-FET can exhibit excellent drain voltage characteristics ($\sim 0.5$ V in this work) in terms of low-power consumption.

IV. CONCLUSION

In this work, the AgTi/HfO$_2$-based TS device and the 2D ATS-FET with the TS device were investigated. 4 $\mu$m$^2$ AgTi/HfO$_2$-based TS device exhibited a low off-state leakage current (i.e., $I_T \sim 1.6 \times 10^{-11}$ A) as well as a low V$_T$ variation (i.e., $<0.07$ V). In addition, it exhibited the stable threshold switching operation under the high compliance current condition of $100 \mu$A and low drive voltage (V$_T \sim 0.47$ V). The 2D ATS-FET was built up by connecting the TS device in series to the 2D baseline-FET and has excellent low-power characteristics (i.e., low gate voltage sweep, low drain voltage). This 2D ATS-FET has shown excellent performance with stably abrupt switching characteristics (e.g., SS$_{min,forward}$ $\sim 19$ mV/decade, SS$_{min,reverse}$ $\sim 26$ mV/decade at 300 K) and low off-state leakage current ($\sim 2.2 \times 10^{-10}$ A/$\mu$m) in the sub-threshold region.

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