A single-supply sub-threshold level shifter with an internal supply feedback loop for multi-voltage applications

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Abstract: A single-supply level shifter with an internal supply feedback loop, which can shift an input signal from the sub-threshold level to the above-threshold level, is presented in this paper. This level shifter has a wider voltage conversion, less transmission delay, higher energy efficiency, and more flexibility in the physical layout than those described in previous citations. The proposed level shifter can convert a 210-mV input signal into a 1.2-V output signal across process corners with a flexible physical layout when implemented in 65-nm LP technology. For a voltage of 0.2 V, the circuit has a propagation delay of 19.4 ns, a static power dissipation of 1.84 nW, and an energy consumption per transition of 82.2 fJ for a 1-MHz input signal. Due to these excellent characteristics, the proposed design is particularly suitable for applications in multi-voltage digital systems.

Keywords: single-supply level shifter, dual-supply LS, ultra-low power, multi-threshold, sub-threshold

Classification: Integrated circuits

References

[1] Y. Osaki, \textit{et al.}: “A low-power level shifter with logic error correction for extremely low-voltage digital CMOS LSIs,” IEEE J. Solid-State Circuits 47 (2012) 1776 (DOI: 10.1109/JSSC.2012.2191320).

[2] S. Lutkemeier and U. Ruckert: “A sub-threshold to above-threshold level shifter comprising a Wilson current mirror,” IEEE Trans. Circuits Syst. II, Exp. Briefs 57 (2010) 721 (DOI: 10.1109/TCSII.2010.2056110).

[3] J. Zhou, \textit{et al.}: “A fast and energy-efficient level shifter with wide shifting range from sub-threshold up to I/O voltage,” IEEE A-SSCC Conf. (2013) 137 (DOI: 10.1109/ASSCC.2013.6691001).

[4] E. Maghsoudloo, \textit{et al.}: “A power-efficient wide-range signal level-shifter,” NEWCAS Conf. (2015) 1 (DOI: 10.1109/NEWCAS.2015.7182025).

[5] S. N. Wooters, \textit{et al.}: “An energy-efficient sub-threshold level convert in 130-nm CMOS,” IEEE Trans. Circuits Syst. II, Exp. Briefs 57 (2010) 290...
1 Introduction

Sub-threshold operation has emerged as a highly effective method for achieving ultra-low power consumption in recent years. In a digital system, certain parts can be used as conventional above-threshold logic to satisfy strict performance constraints, whereas other components are operated in sub-threshold mode to obtain power efficiency. This application leads to the need for multi-voltage system-on-chips (SoCs). A key challenge in discrete multi-voltage design is the level shifter (LS), which provides a required/critical communication interface to guarantee overall correct transmission and robustness when transferring signals from different voltage domains. Therefore, high-quality sub-threshold LSs are required in the design of energy-aware chips. It has been proven that converting a signal from high voltage (V_DDH) to low voltage (V_DDL) is unnecessary because standard CMOS inverters are adequate, whereas up-converting a signal from V_DDL to V_DDH may be problematic if V_DDL is below the transistor’s threshold voltage. Thus, more applicable LSs are required to efficiently convert voltage levels to other desired voltage levels.

The technique of half-latch-based LSs has been widely used in previous works. However, it is difficult to ensure correct functionalities in practice when input signals have sub-threshold voltage levels. Moreover, the power consumption is inefficient due to the large short-circuit current. To solve these problems, several LSs have been investigated in [1, 2, 3, 4, 5, 6, 7, 8, 9, 10]. Generally, these schemes can be summarized in three categories: the current mirror structure [1, 2, 3, 4], the cross-coupled latch structure [5, 6, 7, 8], and the hybrid voltage-current structure [9, 10].

However, these LS topologies, which are termed as dual-supply LSs, inherently require two supply lines (low supply V_DDL and high supply V_DDH) to realize...
voltage conversion. The two supply lines inevitably introduce power routing congestion, posing a restriction on cell placement, and then reducing the flexibility of the physical layout. Thus, a single-supply LS is an attractive option [11]. Unfortunately, this type of circuit has a narrow voltage conversion range, rendering it hard to be applied to sub-threshold systems.

To solve these issues, this paper presents a single-supply LS capable of handling extremely low voltage inputs and achieving an excellent balance between dual-supply LSs and current single-supply LSs. The proposed LS not only has a wide voltage conversion range and low transmission delay but also has a high energy efficiency and flexible physical layout. These advantages make it particularly suitable for multi-voltage digital systems.

The remainder of this paper is organized as follows. In Section 2, the conventional LS design techniques and previous works are introduced. Section 3 describes and analyzes the proposed LS. The simulation results and performance comparisons are presented in Section 4. Finally, Section 5 concludes the paper.

2 Conventional designs and previous works

Two conventional dual-supply LS structures are shown in Fig. 1. Fig. 1a shows a typical voltage-type LS structure, which consists of a pair of cross-coupled P-type transistors and two N-type transistors driven by complementary input signals (IN and INN). The LS behaves as a ratioed circuit, and there is a strong contention between pull-up and pull-down networks. Generally, when \( V_{DDL} \) is larger than the threshold voltage of the NMOS transistors, it is easy to realize the transition from \( V_{DDL} \) to \( V_{DDH} \). However, when \( V_{DDL} \) is lower than the threshold voltage of the NMOS transistors, the transition from \( V_{DDL} \) to \( V_{DDH} \) becomes extremely difficult, because the pull-down NMOS transistors that work in the sub-threshold region are driven by a sub-threshold current \( I_{off} \), whereas the pull-up PMOS transistors driven by a switch current \( I_{on} \) work in the saturation or linear region. By comparison, the \( I_{off} \) is less an order magnitude than the \( I_{on} \). In other words, an incredible wide NMOS should be chosen to support the conversion, which is doomed to be unacceptable. As a result, correct functionalities are difficult to achieve in practice when input signals have sub-threshold voltage levels. Another drawback of this circuit is its inefficiency in power consumption due to the large short-circuit current.

Fig. 1. Conventional dual-supply LSs.

a. Dual-supply voltage-type LS.
b. Dual-supply current-type LS.
Fig. 1b shows a representative current-type LS that uses a current mirror (two PMOS transistors, M2–M3) to implement voltage conversion instead of a PMOS half-latch-based circuit. This circuit can convert a sub-threshold signal to a high-voltage domain; however, its major limitation is the remarkable static current. These two designs are typically dual-supply LSs which are used for conversion just in above-threshold voltage domains.

To address these problems, several improved solutions are proposed. In [1], a distinctive LS scheme based on a current mirror structure is proposed, which uses a logic error correction circuit to realize voltage conversion by detecting the input and output logic levels. Such a strategy accomplishes a successful voltage conversion from 0.23 V to 3 V in 0.35-µm process technology; however, the power dissipation is 58 nW for a 0.4 V–10 kHz input pulse at the expense of a significant amount of area. Another solution based on the current mirror structure is described in [2]. The design allows a wide input supply voltage range and is robust across process corners, which is achieved by adding PMOS current limiters to the basic voltage LS to reduce the drive strength of the cross-coupled pull-up network. Unfortunately, its static power consumption increases because of the static on-current produced by the current limiters.

An LS based on a voltage latch structure is demonstrated in [5] using two stage LSs without intermediate power supplies. The first stage uses a traditional voltage LS with a diode-connected NMOS on the top, and the second is composed of a traditional voltage LS to achieve a full output swing. This design accomplishes a successful voltage conversion from 188 mV to 1.2 V in 130-nm process technology but at the price of speed. In [6], a sub-threshold LS based on the voltage latch structure for multi-voltage applications is presented. The circuit exploits several design strategies to limit energy and static power consumption while also achieving a high-speed performance and supporting a wide voltage conversion range. However, its minimum VDDL is limited due to the diode-connected NMOSs.

Various hybrid LSs based on a combination of the current mirror structure and voltage latch structure are exploited in [9, 10]. These LSs can successfully convert a signal from sub-threshold to nominal voltage, achieving an optimal trade-off between speed and power consumption. However, they all result in a notable area overhead.

It is clear that LSs based on a current mirror structure, voltage latch structure, or hybrid structure are all dual-supply circuits that require two supply voltages, VDDH and VDDL. These two supplies adversely affect the physical design, leading to an inflexible layout arrangement. A cross-sectional single-supply LS is shown in Fig. 2a, which is applied in [11]. This LS works as a buffer and implements full swing up-conversion using a diode-connected NMOS transistor and a feedback PMOS transistor. This topology requires only one supply to convert the incoming low-voltage signal to a high-voltage domain, making its placement more flexible in all of the high-voltage regions. This characteristic makes it particularly suitable to a semi-custom circuit.

Fig. 2b illustrates the voltage transmission curve (VTC) changes of inverter1. Before the transmission stage, the switch threshold of inverter1 is Vth1, the OUT remains at “0”, resulting in M4 on. In other words, if the input signal voltage
reaches Vth1, the circuit will enter into the voltage transmission stage. In the transmission stage, the switch threshold of inverter1 changes from Vth1 to Vth2 (Vth2 < Vth1) due to the diode-connected M1, providing a large driven current. In detail, at the beginning of the transition, node Q will be discharged by M3, and then OUT will be discharged by M5. Later, the OUT will be driven to an intermediate voltage which is larger than the threshold of M4. As a result, the M4 is turned off and the voltage value of node P changes from VDD to VDD-Vth1 due to the diode-connected M1. This pivotal circuit behavior poses a positive effect on inverter1, which leading to the switching threshold of inverter1 changing from Vth1 to Vth2 (Vth2 < Vth1). A large driven current is obtained through inverter1, facilitating the conversion. Eventually, the output achieves the VDDH.

Although this single-supply LS has a high physical flexibility, just like standard cells, it is unable to transfer sub-threshold signals because the minimal VDDL is of the LS depends on the Vth1, not the Vth2. Single-supply LSs also have been proposed in other references, however, their minimal VDDL can either hardly extend to the sub-threshold domain.

This paper presents a new single-supply LS circuit to convert extremely low voltage inputs. The objective is to demonstrate how simple design changes can offer conversion voltage, static power, and energy improvements compared with previous works.

3 Proposed single-supply sub-threshold LS

A single-supply LS with an internal supply feedback loop is proposed in this section. This LS can transfer a sub-threshold signal with a lower delay propagation and energy dissipation.

A schematic of the proposed LS circuit is shown in Fig. 3a, which primarily contains two inverters and a supply feedback loop. The first inverter, which is the main voltage conversion stage, is composed of a PMOS device, MP3, and a NMOS device, MN1. The input of the first inverter is connected to the low-voltage input signal, and the output is connected to node NM. Then, a diode-connected PMOS device, MP2, is coupled to the supply of the first inverter to limit the pull-up strength. Moreover, a power-gating PMOS transistor, MP1, is placed between the

Fig. 2. A single-supply LS.
 a. Circuit topology.
 b. Transient waveforms of inverter1.
pull-up logics and the high supply rail \(V_{DDH}\), where the gate is coupled to node NM, creating an internal supply feedback loop, which causes a voltage drop and a decreasing leakage current at node NM during the standby state. When entering the voltage conversion stage, this voltage drop can also exert a positive effect on reducing the contention current, lowering the energy dissipation, and widening the conversion range. To weaken the pull-up strength, MP1-MP3 are chosen as the high-threshold (hvt) device, whereas the low-threshold (lvt) device is adopted for MN4 to strengthen the pull-down network. The second inverter as the output circuit is connected to the first inverter to ensure a rail-to-rail conversion. The pull-down (MN2) of such an inverter uses a standard threshold (svt) NMOS device to guarantee a powerful pull-down operation because node NM has a degraded voltage level. In contrast, its pull-up (MP4 and MP5) is designed using two stacked hvt PMOS devices to suppress the leakage current and improve the robustness of the circuit.

We now briefly introduce the essential operating principle of the proposed design. The basic operation behavior is illustrated in Fig. 3b. These waveforms were simulated in 65-nm LP technology with \(V_{INL}\) and \(V_{DDH}\) set to 0.1 V and 1.2 V, respectively.

In standby mode, the input signal \(INL\) is grounded to \(V_{GND}\). Then, MP3 is turned on, and MN1 is strongly turned off. Node NM is then charged by \(V_{DDH}\) through MP1, MP2, and MP3. When the voltage level of node NM attains a certain value, MP1 is switched off. As a result, the internal supply feedback loop is cut off. The voltage value is approximately 30% lower than \(V_{DDH}\), which effectively reduces the leakage current through MN1 due to a drain-induced barrier lowering (DIBL). The final state of node NM is determined by the contention between the primarily DIBL current through MP1 and the sub-threshold current through MN1. Eventually, the output (OUTH) is driven to ground by MN2.

A low-to-high (0 \(\rightarrow\) \(V_{INL}\)) transition occurs at INL, which initiates up-conversion activity. Device MN1 goes to weak inversion, and MP3 is weakly turned
off. In the beginning, node NM is rapidly discharged by MN1 due to the switched-off supply feedback and the high pull-down strength. After awhile, the voltage level of node NM reaches a particular value below the threshold of MP1, which enables the supply feedback to begin working. However, the diode-connected device MP2 significantly undermines the strength of the pull-up logics at this time, which ensures that node NM is fully discharged to VGND. Ultimately, the output is charged to $V_{DDH}$ by MP4 and MP5.

When the opposite high-to-low ($V_{INL} \rightarrow 0$) transition occurs at INL, the pull-up network of the first-stage inverter charges $V_{NM}$ to a primary virtual high voltage through the supply feedback. Finally, the output is driven to ground by MN2.

During the entire process of voltage conversion, the proposed LS achieves a considerable improvement in energy dissipation and speed due to the internal supply feedback loop.

In Fig. 4a, the transistor sizes used in the design of the proposed LS are presented. Transistors MP1–MP3, with a channel length of 0.2 µm (twice the minimum allowed channel length), are used in the pull-up network of the main voltage conversion stage to reduce the contention, whereas the other transistors use a channel length of 0.1 µm to obtain excellent speed performance. Fig. 4b illustrates the corresponding physical layout of the proposed LS. The power and ground rails are placed at the top and bottom with metal-1, respectively. Layer metal-1 is adopted for routing. It can be seen that the entire layout has only one power supply, $V_{DDH}$, and the height of the layout is designed to match that of standard cells. With these characteristics, the proposed LS can be placed anywhere in $V_{DDH}$ voltage islands, thereby enabling much more flexible placement and power strip arrangement. This approach leads to a significantly smaller physical design overhead for LS insertion because the proposed LS can be inserted in any uncongested region. The layout of the proposed LS only consumes an area of 4.45 µm² (2.47 µm × 1.8 µm), which is approximately equal to the area of a standard data flip-flop (DFF).

| Transistor | W/L [µm] |
|------------|----------|
| MP1        | 0.15/0.2 |
| MP2        | 0.15/0.2 |
| MP3        | 0.15/0.2 |
| MP4        | 0.36/0.1 |
| MP5        | 0.36/0.1 |
| MN1        | 1.5/0.1  |
| MN2        | 0.2/0.1  |

**Fig. 4.** Transistor sizes and layout of the proposed LS.

a. Transistor sizes.

b. Layout of the proposed LS.
4 Results and discussion

In this section, the effectiveness and capabilities of the proposed LS are verified using the Hspice tool in TSMC 65-nm LP CMOS process technology. Post-layout simulations for three process-voltage-temperature (PVT) corners are performed, using an input signal frequency of 1 MHz and input signal rise- and fall-times of 10 ns. Additionally, $V_{DDH}$ and the output capacitive load are set to 1.2 V and 100 fF, respectively.

The typical case (TC) scenario involves typical NMOS and PMOS devices at a temperature of 25°C and a nominal 1.2-V $V_{DDH}$. The worst case (WC) corner adopts slow NMOS and fast PMOS devices, which could deteriorate the contention between pull-up and pull-down logics. Moreover, a 10% high voltage increase ($V_{DDH} = 1.32 V$) and a temperature of $-40°C$ are also considered, which further entail weaker transistor operations in the sub-threshold regions. Finally, fast NMOS and slow PMOS transistors operating at a temperature of 125°C and a 10% high voltage reduction ($V_{DDH} = 1.08 V$) are considered for the best case (BC) condition.

The propagation delay of the proposed LS against $V_{INL}$ is illustrated in Fig. 5. It is noted that the delay grows exponentially with $V_{INL}$ scaled into the sub-threshold regions. Additionally, the delay of the WC corner is 100x greater than that of the BC corner below 200 mV. Still, the LS operates accurately across the simulated PVT corners. At 200 mV, the delay of the proposed circuit is 19.4 ns, which is essentially equivalent to the value in [2]; however, the delay is nearly 3 times smaller than the 57.9 ns reported for the LS in [5]. Furthermore, this value is smaller than that of the majority of dual-supply LSs.

Fig. 5. Propagation delays across PVT corners.

Fig. 6 illustrates the total energy dissipation per transition and static power consumption of the proposed design for an input signal of 1 MHz. It is worth noting that the energy consumption per transition decreases relatively slowly by reducing

Fig. 6. Energy per transition and static power at TC versus $V_{INL}$.
the voltage in the above-threshold regions. The proposed LS has a relatively flat energy between 0.4 V and 0.6 V. However, as $V_{\text{INL}}$ continuously scales down to the sub-threshold regions, the energy starts to rise precipitously again because the static energy dominates the main energy consumption in the sub-threshold region, whereas the static power consumption exhibits a slight fluctuation in the proposed circuit as $V_{\text{INL}}$ decreases. This result is attributed to the internal supply feedback loop technique, diode technique, and stacked transistor technique presented in this design. For an input voltage of 200 mV, an energy consumption of 82.2 fJ per transition and a static power of 1.84 nW are achieved. By contrast, the LS in [2] consumes 93.9 fJ and 6.6 nW at this point. Moreover, the static power value of the proposed single-supply LS is far smaller than that of the majority of dual-supply LSs.

To illustrate how low of a $V_{\text{INL}}$ can be achieved, a 10000-point Monte Carlo simulation was performed with both global and local variations. As shown in Fig. 7, the proposed LS has a minimum $V_{\text{INL}}$ of 210.33 mV across the PVT corners.

**Fig. 7.** Distribution of the minimum $V_{\text{INL}}$ for the proposed design.

**Table 1.** Property comparisons of LSs

|                | [1] | [2] | [5] | [6] | [9] | [10] | [11] | Current |
|----------------|-----|-----|-----|-----|-----|------|------|---------|
| Type           | CMDS| CMDS| VLDS| VLDS| HDS | HDS  | SS   | SS      |
| Tech           | 0.35 µm | 0.09 µm | 0.13 µm | 0.09 µm | 0.18 µm | 0.18 µm | 65 nm | 65 nm   |
| $V_{\text{DDL}}$ | 0.23 V | 0.1 V | 0.188 V | 0.18 V | 0.19 V | 0.36 V | 0.43 V | 0.21 V  |
| $V_{\text{DDH}}$ | 3 V  | 1 V  | 1.2 V  | 1 V  | 1.8 V | 1.8 V | 1.2 V | 1.2 V   |
| Delay (ns)     | 104@0.4 V | 18.4@0.2 V | 57.9@0.2 V | 21.8@0.2 V | 21@0.4 V | 30@0.4 V | 3.2@0.5 V | 19.4@0.2 V |
| Etr. (fJ)      | 5800@0.2 V | 94@0.2 V-1 MHz | N.A | 74@0.2 V | 390@0.4 V-1 MHz | 327@0.4 V | 83.2@0.5 V | 82.2@0.2 V |
|                | 5800@0.2 V | 94@0.2 V-1 MHz | N.A | 74@0.2 V | 390@0.4 V | 327@0.4 V | 83.2@0.5 V | 82.2@0.2 V |
| Pstatic (nW)   | 0.23@0.4 V | 6.6@0.2 V | N.A | 6.4@0.2 V | 0.16@0.4 V | 0.13@0.4 V | 1.49@0.5 V | 1.84@0.2 V |
|                | 0.23@0.4 V | 6.6@0.2 V | N.A | 6.4@0.2 V | 0.16@0.4 V | 0.13@0.4 V | 1.49@0.5 V | 1.84@0.2 V |
| Area (µm²)     | 1880 | N.A | 96 | 36.5 | 95.6 | 120.9 | 3.6 | 4.45    |

[11]: replicated [11] in this work; CMDS: current mirror dual-supply; VLDS: voltage latch dual-supply; HDS: hybrid dual-supply; SS: single-supply; Etr.: energy consumption per transition.
which is similar to the values of the dual-supply LSs in [5] and [6]. In addition, a small normalized variance value $\sigma/\mu$ of 0.062 can be gained, exhibiting superior process variation tolerance compared with other LSs.

To further describe the characteristics of the new LS, this paper compares the properties of the proposed LS with those of other LS circuits in Table I. Based on these results, we can observe that the dual-supply LSs all have a wide voltage conversion range but at a significant expense of delay, energy, static power, and area. By contrast, the traditional single-supply LS has a smaller area, lower static power, and higher speed but at an unbearable penalty of minimum $V_{DDL}$.

However, the single-supply LS proposed in this paper, which benefits from the proposed internal supply feedback loop, achieves an excellent balance between these properties. This LS reaches a minimum input voltage of 0.21 V, a delay of 19.4 ns, and an energy dissipation of 82.2 fJ, which approaches the values of dual-supply LSs. In addition, only 1.84 nW of static power and 4.45 $\mu$m$^2$ of area are consumed, demonstrating a remarkable improvement compared with other LSs. All of these excellent characteristics as well as the flexibility of the physical layout make the proposed design particularly suitable for multi-voltage digital systems.

5 Conclusions

A single-supply LS with an internal supply feedback loop is presented in this paper. The proposed circuit is capable of shifting input signals from the sub-threshold to the above-threshold domain and consumes less static power and energy than previous circuits. In addition, the single power supply makes the proposed LS more flexible in placement, enabling an efficient physical design similar to that of standard cells to solve the unique physical challenges presented in multi-voltage systems.

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