Sub-Block Rearranged Staircase Codes

Min Qiu and Jinhong Yuan

Abstract

We propose a new family of spatially coupled product codes, called sub-block rearranged staircase (SR-staircase) codes. Each code block of SR-staircase codes is obtained by encoding rearranged preceding code blocks and new information block, where the rearrangement involves sub-blocks decomposition and transposition. The proposed codes can be constructed to have each code block size of $1/q$ to that of the conventional staircase codes while having the same rate and component codes, for any positive integer $q$. In this regard, we can use strong algebraic component codes to construct SR-staircase codes with a similar or the same code block size and rate as staircase codes with weak component codes. We characterize the decoding threshold of the proposed codes under iterative bounded distance decoding (iBDD) by using density evolution. We also derive the conditions under which they achieve a better decoding threshold than that of staircase codes. Further, we investigate the error floor performance by analyzing the contributing error patterns and their multiplicities. Both theoretical and simulation results show that the designed SR-staircase codes outperform staircase codes in terms of waterfall and error floor while the performance can be further improved by using a large coupling width.

Index Terms

Hard decision decoding, product codes, staircase codes.

I. INTRODUCTION

The explosive growth of data-hungry applications such as video streaming services and social networks has driven the development of high-speed optical networks. Forward error correction (FEC) codes are employed in optical communication systems to guarantee reliable data transmission. In particular, modern high-speed optical communication systems require FEC schemes: 1) to support throughput of 100 Gbit/s and beyond; 2) to have low power consumption; 3) to

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The authors are with the School of Electrical Engineering and Telecommunications, University of New South Wales, Sydney, NSW, 2052 Australia (e-mail: min.qiu@unsw.edu.au; j.yuan@unsw.edu.au).
achieve a large coding gain close to the theoretical capacity limits at a target bit error rate (BER) of $10^{-15}$; and 4) to be adapted to the peculiarities of the optical channel [2], [3].

A number of FEC codes that are popular for handling error correction in wireless communications have also been considered for optical communications [3], [4]. Among these FEC codes, low-density parity-check (LDPC) codes [5] and spatially coupled LDPC codes [6] have gained much attention [7] due to their provably close-to-capacity performance under belief propagation (BP) decoding [8], [9]. That said, the exchange of soft messages within their BP decoders significantly increases the internal data flow [10] as well as hardware and power cost for enabling high-resolution analog-to-digital conversion. An alternative solution is to resort to low-complexity hard decision decoding (HDD), which has significantly lower data flow [10] but suffers from some performance degradation. The FEC codes that are particularly suitable for high throughput HDD are product-like codes [11] with Bose-Chaudhuri-Hocquengham (BCH) or Reed-Solomon component codes [4]. HDD is performed iteratively by decoding the component codes using algebraic bounded distance decoding [12], which is referred to as iterative bounded distance decoding (iBDD) [3]. Owing to the low-complexity decoding, product codes with iBDD have been adopted in various optical communications standards, e.g., [13].

Product-like codes continue to evolve today for achieving larger net coding gains. The authors in [10] applied the idea of spatial coupling to product codes with BCH component codes and constructed staircase codes. Remarkably, it was shown that their error performance only has a gap of 0.56 dB from the binary symmetric channel (BSC) capacity under iBDD and outperform existing FEC solutions in ITU-T G.975.1 [13]. Another class of spatially coupled product codes called braided BCH codes were introduced in [14], which have comparable error performance to staircase codes. Both codes [10], [14] can be considered as instances of spatially coupled generalized LDPC (GLDPC) ensembles [15], [16] with BCH component codes as constraints. [17] has proved that this class of spatially coupled GLDPC ensembles under iterative hard-decision decoding can approach capacity at high rates. A unified framework called zipper codes was recently proposed in [18] for precisely describing the structure of most product-like codes with every variable node having degree two. Within this framework, the authors in [18] also proposed tiled diagonal zipper codes which can be seen as a combination of continuously interleaved BCH codes [19] and staircase codes [10]. In addition to spatial coupling, another line of work is to construct symmetry-based product codes [20] to reduce the blocklength of product codes [11] while having the same component code and similar code rates. With this
property, one can employ stronger algebraic component codes to construct symmetry-based product codes in a bid to achieve better waterfall and error floor performance while maintaining similar blocklengths and code rates as the conventional product codes. The first examples of such codes are half-product codes \([21]\), whose codewords are derived from product codes with the additional constraint that the code arrays are anti-symmetric. Since each off-diagonal symbol of a half-product code array is repeated twice, the repeated symbols are punctured before transmission. Therefore, half-product codes have an effective blocklength about half to that of the product codes from which they are derived. Later, this idea inspired the design of quarter-product codes and octal-product codes in \([22]\) as well as half-braided BCH codes in \([23]\). However, all the above symmetric-based product codes require square code blocks and the same component codes for row and column encoding. In addition, the codes in \([22]\) restrict the component codes to be reversible (i.e., a code that is invariant under a reversal of the coordinates in each codeword \([24]\)). These restrictions reduce the design space of symmetric-based product codes and may limit their potential applications.

This paper focuses on designing new FEC schemes under low-complexity iBDD to achieve better waterfall and error floor performance with lower miscorrection probability than staircase codes \([10]\). Motivated by spatial coupling and symmetry, we propose sub-block rearranged staircase (SR-staircase) codes. The proposed codes can be constructed to have each code block with a size of \(1/q\) to that of the conventional staircase codes with the same algebraic component codes while maintaining the same code rate, for any positive integer \(q\). This means that we can employ strong algebraic component codes to construct SR-staircase codes with a similar or the same code block size and rate as staircase codes with weak component codes. The proposed SR-staircase codes have a flexible structure and offer larger degrees of freedom in code design compared to the conventional staircase codes and symmetric-based product codes. However, unlike all the aforementioned symmetric-based product codes, the proposed codes do not impose any additional constraint on the component codes and code array shapes. The main contributions of this paper are as follows.

- We propose SR-staircase codes which inherit the benefits from both symmetry and spatial coupling. We first introduce the code structure, encoding and decoding procedures. We then extend the proposed construction to a large coupling width. The connections between SR-staircase codes, conventional staircase codes and other spatially coupled codes are discussed.
- We investigate the performance of the proposed codes under miscorrection-free iBDD (i.e.,
the component BDD only outputs either the correct codeword or the original received vector) on the BSC. By looking into the graph model, we first apply density evolution (DE) \[25\] on SR-staircase codes with deterministic structures and characterize the decoding thresholds. We also derive a necessary condition under which the proposed codes achieve a larger decoding threshold than staircase codes. In addition, we investigate the error floor performance by analyzing the contributing error patterns and their multiplicities. Our results demonstrate that the decoding threshold and error floor of SR-staircase codes can be improved by using a large coupling width.

- Numerical results are provided and show that the designed SR-staircase codes achieve better waterfall and error floor performance over staircase codes under iBDD. It is also interesting to note that the performance of the proposed codes under iBDD is very close to that under miscorrection-free iBDD due to the use of strong BCH component codes. We stress that the use of BCH component codes with stronger error correction capability can offer better error correction and error detection than employing BCH component codes with weaker error correction capability and extended parity bits, e.g., \[10\].

A. Notation

This paper uses the following notations. Scalars, vectors and matrices are written in lightface, boldface and boldface capital letters, respectively, e.g., \(x\), \(x\) and \(X\). The \(r\)-th row of a matrix \(X\) is represented by \(x_r \in X\). \(\mathbb{N} \triangleq \{1, 2, \ldots\}\) represents the set of natural numbers. We define \([n] \triangleq \{1, \ldots, n\}\) for any \(n \in \mathbb{N}\). \([x]\) gives the nearest integer that is not smaller than \(x\) while \(\lfloor x \rfloor\) gives the nearest integer that is not larger than \(x\). We define a function \(\varphi : \mathbb{N} \to \{1, 2\}\) as \(\varphi(x) = 3 - \frac{(-1)^x}{2}\). The binary field and the collection of binary matrices of size \(m \times n\) are denoted by \(\mathbb{F}_2\) and \(\mathbb{F}^{m,n}_2\), respectively. An \(m \times n\) all-zero matrix is represented by \(0_{m,n}\). The transpose operation is denoted by \((\cdot)^\top\). The Hamming weight function is denoted by \(w_H(\cdot)\). For a set \(S\), \(|S|\) outputs its cardinality. For a length-\(n\) vector \(x\), \(x(S)\) is a sub-vector of \(x\) by taking the elements in the positions of \(S \subseteq [n]\). The indicator function is represented by \(1\{\cdot\}\).

II. SUB-BLOCK REARRANGED STAIRCASE CODES

In this section, we introduce the encoding and decoding of SR-staircase codes. We also discuss the relationship between the proposed codes and the conventional staircase codes \[10\]. In this work, we consider the underlying component codes to be binary primitive BCH codes. However,
like the conventional staircase codes, the choice of the component codes for SR-staircase codes does not preclude other linear codes such as polar codes [26] and LDPC codes [27].

A. Encoding

A SR-staircase code comprises a sequence of code blocks \( B_1, B_2, \ldots \). At time \( i \in \mathbb{N} \), code block \( B_i = [K_i, P_i] \) is a concatenation of information block \( K_i \) and parity block \( P_i \). To construct the SR-staircase code, two shortened BCH codes \( C_j \) for \( j \in \{1, 2\} \) are used. We denote by \( k_j, n_j, t_j, e_j \), and \( G_j \) the message length, codeword length, error correction capability, shorten length, and generator matrix, respectively, of \( C_j \). Note that we can also express the codeword length and information length of \( C_j \) as \( n_j = 2^{\nu_j} - 1 - e_j \) and \( k_j = 2^{\nu_j} - 1 - \nu_j t_j - e_j \), respectively, for some positive integer \( \nu_j \geq 3 \), where \( \nu_j \) is Galois field extension [28] Ch. 3.3.

The encoding of SR-staircase codes is performed in a recursive manner like the conventional staircase codes. The main difference is that each preceding SR-staircase code block \( B_{i-1} \) is required to be decomposed into \( q_1 \) if \( i \in 2\mathbb{N} - 1 \) and \( q_2 \) if \( i \in 2\mathbb{N} \). Each sub-block is then transposed before performing the component code encoding. The size of \( B_i \) is \( \frac{m_1}{q_1} \times m_2 \) if \( i \in 2\mathbb{N} - 1 \) and \( \frac{m_2}{q_2} \times m_1 \) if \( i \in 2\mathbb{N} \). Moreover, all the bits in each row of \( B_i \) are the last \( m_2 \) bits of a codeword of \( C_2 \) when \( i \in 2\mathbb{N} - 1 \) and the last \( m_1 \) bits of \( C_1 \) when \( i \in 2\mathbb{N} \). Note that the numbers of columns of \( B_i \), \( m_1 \) and \( m_2 \), have to be divisible by \( q_1 \) and \( q_2 \), respectively. We also denote by \( w \) the coupling width, where \( w \geq 2 \) (i.e., \( w = 1 \) means uncoupled) and both \( m_1 \) and \( m_2 \) have to be divisible by \( w - 1 \). In the following, we present the encoding procedures.

1) Case \( w = 2 \): For ease of presentation, we first describe the encoding steps for \( i \in 2\mathbb{N} \).

Step 1 (Initialization): Set all the entries of \( B_0 \) to zero: \( B_0 = 0_{\frac{m_2}{q_2},m_1} \); \( B_0 \) is known by the encoder and decoder pair. Then, the encoding process starts from \( i = 1 \).

Step 2 (Decomposition): The preceding block \( B_{i-1} \) with size \( \frac{m_1}{q_1} \times m_2 \) is divided into \( q_2 \) consecutive equal-size sub-blocks \( B_{i-1,1}, B_{i-1,2}, \ldots, B_{i-1,q_2} \). That is,

\[
B_{i-1} = [B_{i-1,1}, B_{i-1,2}, \ldots, B_{i-1,q_2}].
\]  

Each sub-block of \( B_{i-1} \) has size \( \frac{m_1}{q_1} \times \frac{m_2}{q_2} \).

Step 3 (Transformation): Apply matrix transpose to each sub-block of \( B_{i-1} \) in Step 2 and combine them to form block \( B_{i-1}^T \) with size \( \frac{m_2}{q_2} \times \frac{m_1 q_2}{q_1} \), given by

\[
B_{i-1}^T = [B_{i-1,1}^T, B_{i-1,2}^T, \ldots, B_{i-1,q_2}^T].
\]
Each sub-block of $B_{i-1}^\pi$ is of size $\frac{m_2}{q_2} \times \frac{m_1}{q_1}$. Note that all bits in the same column position of every transposed sub-block, $B_{i-1,1}^T, \ldots, B_{i-1,q_2}^T$, belong to the same component codeword of $C_2$.

The transformation of $B_{i-1}$ into $B_{i-1}^\pi$ in (2) can be generalized by employing a permutation function $\pi(.)$ which permutes the rows and columns of a matrix, such that

$$B_{i-1}^\pi = \pi \left( [B_{i-1,1}^T, B_{i-1,2}^T, \ldots, B_{i-1,q_2}^T] \right).$$

(3)

**Step 4 (Concatenation):** Arrange the information bits to be encoded for the $i$-th code block as an $\frac{m_2}{q_2} \times (k_1 - \frac{m_1 q_2}{q_1})$ block $K_i$. Concatenate an all-zero block $0_{\frac{m_2}{q_2} \times e_1}$ (representing shortened bits), the rearranged preceding block $B_{i-1}^\pi$ from Step 3, and information block $K_i$ to construct an $\frac{m_2}{q_2} \times (k_1 + e_1)$ message matrix to be encoded at time $i$

$$K_i' = \left[ 0_{\frac{m_2}{q_2} \times e_1}, B_{i-1}^\pi, K_i \right].$$

(4)

**Step 5 (Component Code Encoding):** Perform row-by-row systematic component code encoding to obtain the codeword matrix with size $\frac{m_2}{q_2} \times n_1$ at time $i$

$$C_i = K_i' G_1 = \left[ 0_{\frac{m_2}{q_2} \times e_1}, B_{i-1}^\pi, K_i, P_i \right] = \left[ 0_{\frac{m_2}{q_2} \times e_1}, B_{i-1}^\pi, B_i \right],$$

(5)

where $P_i$ is the parity block with size $\frac{m_2}{q_2} \times (n_1 - k_1)$. Finally, $B_i = [K_i, P_i]$ is an $\frac{m_2}{q_2} \times m_1$ code block that will be transmitted. Each row of $[B_{i-1}^\pi, B_i]$ is a shortened codeword of $C_1$.

The encoding steps to obtain $B_i$ for $i \in 2N - 1$ are similar to the above. After Step 5, each row of $[B_{i-1}^\pi, B_i]$ is a shortened codeword of $C_2$ for $i \in 2N - 1$. The relation between the component codeword length, time index $i$, the number of decomposed sub-blocks in $B_i$ and the number of columns of $B_i$ satisfies

$$n_{\varphi(i)} = m_{\varphi(i)} + \frac{m_{\varphi(i)} \cdot q_{\varphi(i-1)}}{q_{\varphi(i)}},$$

(6)

where $\varphi(.)$ is a mapping function defined in Sec. I-A. The code rate is given by

$$R = \frac{1}{2} \left( \frac{k_1}{m_1} + \frac{k_2}{m_2} - \frac{q_2}{q_1} - \frac{q_1}{q_2} \right) = 1 - \frac{1}{2} \left( \frac{\nu_1 t_1}{m_1} + \frac{\nu_2 t_2}{m_2} \right).$$

(7)

Alternatively, SR-staircase codes can be described by using the zipper code framework [18], where $B_{i-1}^\varphi$ is the virtual buffer and $B_{i-1}$ is the corresponding real buffer. The transformation of $B_{i-1}$ into $B_{i-1}^\varphi$ in Step 3 can be described by using a bijective mapping function.

**Example 1.** Consider a SR-staircase code with $w = 2$, $q_1 = 2$ and $q_2 = 3$. The codeword matrices obtained in (5) from Step 5 are shown in Fig. 1. The sub-blocks indicated by light colors and gray dash lines are involved in the encoding but will not be transmitted. Specifically,
Thus, (4) in Step 4 is replaced by (9). The rest of the encoding steps are the same as those in Sec. II-A1. The overall code rate does not change with \( w \).

It is important to note that when \( w \geq q+1 \), the bits in different column positions of the coupled block \( [B_{i-1,1}^\pi, \ldots, B_{i-w+1,w-1}^\pi] \) are protected by different component codewords because any pair
Remark 1. Although we only consider using the same component code across the rows of each SR-staircase code block in this work for simplicity, it is possible to use component code mixtures such that the component code varies among the rows of the same code block. In fact, this was suggested for the conventional staircase codes in \cite[Sec. 4.4]{29}. However, it was proved that employing component code mixtures is not beneficial to the asymptotic performance of spatially coupled product codes \cite{30}. In addition, one may also use the proposed technique to construct uncoupled product codes in order to employ strong BCH component codes. In this case, the ‘checks on checks’ array on the resultant product codes will become different depending on whether rows or columns are encoded first. As a result, the parity bits of the ‘checks on checks’ array can only be protected by either column or row codewords, leading to some loss in performance.

B. Connections to Other Spatially Coupled Codes

SR-staircase codes are motivated and derived by introducing symmetry in the conventional staircase codes \cite{10}. Consider the SR staircase code in Sec. II-A1 with \( w = 2 \) and let \( q \doteq q_1 = q_2 \). By concatenating \( q \) identical SR-staircase code block \( B_i \), one obtains the resultant staircase code block at time \( i \) as

\[
B^*_i = \left[ B^T_i, \ldots, B^T_i \right]^T = \left[ \left[ K^T_i, P^T_i \right], \ldots, \left[ K^T_i, P^T_i \right] \right]^T = \left[ K^*_i, P^*_i \right].
\] (10)

where \( K^*_i = \left[ K^T_i, \ldots, K^T_i \right]^T \) and \( P^*_i = \left[ P^T_i, \ldots, P^T_i \right]^T \) are the \( i \)-th information block and parity block of staircase codes \cite{10}. Consider \( i \in 2\mathbb{N} \) for example. Then the sizes of the current and preceding staircase code blocks satisfy \( B^*_i \in \mathbb{F}^{m_2 \cdot m_1} \) and \( B^*_{i-1} \in \mathbb{F}^{m_1 \cdot m_2} \). Notice that \( B^*_{i-1} \) can be rearranged into \( B^*_{i-1} \in \mathbb{F}^{m_2 \cdot m_1} \), which consists of \( q \) identical rearranged code blocks \( B^*_{i-1} \in \mathbb{F}^{m_2 \cdot m_1} \), i.e.,

\[
B^*_{i-1} = \left[ \left( B^*_i \right)^T, \ldots, \left( B^*_i \right)^T \right]^T,
\] (11)

where the construction of \( B^*_{i-1} \) follows from either (3) or (2). As a result, each row of \( [B^*_{i-1}, B_i] \) is a valid codeword of \( C_1 \). Clearly, it can be seen that each code block \( B^*_i \) is drawn from a subset of the set of the code blocks of staircase codes due to symmetry, i.e., having \( q - 1 \) replicas of \( B_i \).
Fig. 2. The relation between a SR-staircase code with \( q = 3 \) and a staircase code (purple). The rearrangement of the sub-blocks of the SR-staircase code and two component codewords that belong to \( C_1 \) (blue) and \( C_2 \) (red), respectively, are indicated.

Thus, the resultant staircase code \( B'_1, \ldots \) is a subcode of the conventional staircase code. Notice that when \( q = 1 \), the encoding steps in Sec. II-A1 produce the conventional staircase codes. By removing any \( q - 1 \) replicas of \( B_i \) as they do not contain any new information, the resultant SR-staircase codes achieve the same rates and an effective code block size of \( 1/q \) to the conventional staircase codes from which they are derived. In this regard, the proposed construction enables to employ stronger BCH codes to construct SR-staircase codes with improved error performance while maintaining a similar or the same code block size and rate compared to staircase codes.

To visualize the relationships in (10) and (11), we show the code blocks of a SR-staircase code with \( q = 3 \) and a staircase code in Fig. 2 where both codes use the same component codes and have the same rate. Note that the colors follow a similar style as in Fig. 1. Clearly, the SR-staircase code has a block length of \( 1/3 \) to that of the benchmark staircase code.

The proposed SR-staircase codes are also close to tiled diagonal zipper codes [18, Sec. IV-E]. Specifically, tiled diagonal zipper codes can be seen as a special case of the proposed SR-staircase codes by fixing \( C_1 = C_2 \), \( w - 1 = q_1 = q_2 \), \( m_1 = m_2 \), and a specific permutation of (3). However, we emphasize that the proposed SR-staircase codes are motivated and derived by applying the idea of symmetry from symmetric-based product codes [20], [22] to staircase codes [10] as illustrated above. Compared to tiled diagonal zipper codes, the proposed codes have more code parameters, such as the decomposition number \( (q_1, q_2) \) and coupling width \( w \), which are explicitly defined and play very important roles in determining the rate, code block size, and
performance. This, together with the capability of using a pair of different component codes \((C_1, C_2)\), give rise to more flexible code structures for SR-staircase codes. Thus, the proposed codes can be constructed to meet a wider range of requirements. We emphasize that the aim of this work is to design codes with superior waterfall and error floor performance over staircase codes under iBDD. To this end, we use rigorous density evolution and error floor analysis to design code parameters \((w, q_1, q_2, m_1, m_2)\) and justify the choice of component codes \((C_1, C_2)\).

The proposed SR-staircase codes are also related to the class of partially coupled codes, i.e., [31]–[33], recently proposed by us in the sense that a fraction of information and/or parity bits in one code block are coupled and become a part of the input to the encoders of consecutive code blocks. These bits are repeated before coupling and component code encoding while all repeated bits are punctured before transmission. This allows us to introduce stronger component codes to improve the overall decoding performance of coupled codes.

C. Decoding

The decoding of SR-staircase codes is performed in a sliding window fashion, similar to staircase codes. To avoid repetition, we only point out the main difference. We denote by \(W\) the decoding window size satisfying \(W > w\) and \(Y_i\) the received code block corresponding to \(B_i\) after hard-decision demapping. Consider \(m_1 = m_2 \triangleq m\) and \(q_1 = q_2 \triangleq q\) for simplicity. The decoder constructs the received codeword matrix corresponding to \(C_i\) in (5)

\[
D_i = \begin{bmatrix}
0_{m_1}^T, e_{\psi(i)}, Y_{i-1,1}^\pi, Y_{i-2,2}^\pi, \cdots, Y_{i-w+1,w-1}^\pi, Y_i
\end{bmatrix},
\]  

where \(Y_{i-l,l}^\pi, l \in [w-1]\) is the \(l\)-th sub-block decomposed from \(Y_{i-l}^\pi\), which is obtained by applying the transformation of (2) to \(Y_{i-l}\). Then, BDD is applied to each row of \(D_i\) with non-zero syndrome and the rest of the decoding steps directly follow those in [10] Sec. IV-A.

In this work, we restrict the decoding to be iBDD due to its simplicity and low complexity. In Section V we will show that iBDD is suffice for SR-staircase codes to operate close to miscorrection-free performance as a result of using component codes with large \((t_1, t_2)\). We note that a range of decoding algorithms, e.g., [34]–[38] have been proposed for product-like codes to bring their decoding performance close to miscorrection-free performance or beyond at the cost of increased complexity. Hence, it is also beneficial to apply these decoding algorithms to SR-staircases. This will be investigated in our future work.
III. DECODING THRESHOLD ANALYSIS

In this section, we analyze the decoding thresholds of SR-staircase codes by using DE. Based on the analysis, we then present a guideline for designing the parameters for SR-staircase codes to achieve a better threshold than the conventional staircase codes.

A. Graph Model

We first study the graph model of the proposed codes. Following the approach in [25], we consider a deterministic code structure since the interleaver of the proposed codes is fixed. The analysis performed on a deterministic code structure allows one to make precise statements about the performance of actual codes. Although one can employ random interleaving in the proposed codes as shown in (3), the deterministic code structures often give rise to implementation advantages over random ensembles.

For ease of understanding, we first consider the case of \( w = 2 \). From Sec. II-A1, we know that code block \( B_i \) has \( \frac{m_2}{q_2} \) rows for \( i \in 2N \) and \( \frac{m_1}{q_1} \) rows for \( i \in 2N - 1 \). By using the Tanner graph representation [15], it can be seen that the \( i \)-th spatial position (time instance) on the graph has \( \frac{m_2}{q_2} \) check nodes (CNs) when \( i \in 2N \) and \( \frac{m_1}{q_1} \) CNs when \( i \in 2N - 1 \) because one component codeword poses constraints on a row of \( B_i \). Each bit in \( B_i \) is represented by a variable node (VN) that connects a pair of CNs in the \( i \)-th and \((i + 1)\)-th spatial positions via an edge. Thus, each VN always has degree 2. All CNs in any two neighboring spatial positions are fully connected. More precisely, each pair of CNs in the two neighboring spatial positions \( i \) and \( i + 1 \), are connected via \( q_1 \) and \( q_2 \) edges for \( i \in 2N \) and \( i \in 2N - 1 \), respectively, where a VN lies on each edge. We use an example to illustrate the graph representation of a SR-staircase code with given specific parameters.

**Example 2.** Consider a SR-staircase code with \((m_1, m_2) = (4, 9)\) and \((q_1, q_2) = (2, 3)\). The code blocks and the corresponding graph model of this SR-staircase code are shown in Fig. 3(a) and Fig. 3(b), respectively. Consider \( i \in 2N \). Since each VN always has degree 2, we use an edge to represent a VN that connects a pair of CNs for simplicity. We label two bits in \( B_i \), i.e., \( B_i(3, 1) \) and \( B_i(2, 4) \), in Fig. 3(a) and mark their corresponding edges (VN) in the Tanner graph with the same color in Fig. 3(b). Note that the code structure and graph model in Fig. 3 are based on the transformation in (2). If a random permutation function in (3) is adopted, the bit label of each edge in Fig. 3(b) will change while the connectivity between CNs remains unchanged. ■
We now consider the case of $w > 2$ and using the coupling pattern shown in (8) and (9). We set $m_1 = m_2 \triangleq m$ and $q_2 = q_2 \triangleq q$ by following Sec. II-A2. Different from $w = 2$, all CNs in spatially positions $i$ and $i + l, \forall l \in [w - 1]$, are fully connected. When $w \geq q + 1$, each pair of CNs in two coupling spatial positions, $i$ and $i + l$, are connected by only one edge. This is because the bits in different column positions of $[B_{\pi i-1,1}, \ldots, B_{\pi i-w,1}^w]$ are protected by different component codewords according to Sec. II-A2. As a result, each bit in $B_i$ is protected by two component codewords. It should be noted that this may not hold in general if the coupling pattern is completely random. In contrast, when $w = 2$ (and we still assume $m_1 = m_2 \triangleq m$ and $q_2 = q_2 \triangleq q$), the bits in the same column position of every coupled sub-block $B_{i-1,1}^\pi, \ldots, B_{i-w,1}^\pi$ are protected by the same component codeword. Hence, the SR-staircase code with $w = 2$ has a multi-edge graph representation shown in Fig. 3(b) such that every $q$ bits are protected by two component codewords. When $2 < w < q + 1$, the connectivity between CNs is mixed with single-edge and multi-edge. For this case, the number of connecting edges ranges from 1 to $\lceil \frac{q}{w-1} \rceil$ and depends specifically on the values of $q$ and $w$.

B. Density Evolution

We derive the DE equations for the BSC based on the graph model in (III-A). We note that various techniques were introduced in the literature to analyze the performance of product-like codes [17], [25], [39]. Both [17] and [39] applied DE to the ensembles that can represent a range of product-like codes. To make precise statements about the performance of the proposed codes with deterministic structures under iBDD, we adopt the approach in [25] to perform DE.
analysis. Moreover, we assume that the underlying BDD is misscorrection-free as it is a necessary condition to conduct the DE analysis \cite{25, 39}.

\textbf{1) :} We start with the case of \( w = 2 \). Consider the SR-staircase code constructed in Sec. \textsection{II-A1} with code blocks \( B_i, i \in [L] \). Let \( p \) be the crossover probability of a BSC. We define the effect channel quality to be

\[ M_{\varphi(i)} \triangleq p n_{\varphi(i)} \begin{pmatrix} m_{\varphi(i)} + \frac{m_{\varphi(i)} \cdot q_{\varphi(i-1)}}{q_{\varphi(i)}} \end{pmatrix}, \tag{13} \]

whose operational meaning is the expected average number of bits received in errors per component code constraint of \( C_{\varphi(i)} \) and \( \varphi(\cdot) \) is a mapping function defined in Sec. \textsection{I-A}. Hence, we are interested in the probability that a CN declares a decoding failure after \( \ell \) iterations as \( n_{\varphi(i)} \to \infty \). To track this probability as a function of \( \ell \), we define a parameter \( x_{\ell}^{(i)} \), \( i \in [L] \), whose operational meaning is that the probability of a randomly chosen erroneous bit attached to a component code of \( C_{\varphi(i)} \) in \( B_i \) is not recovered after \( \ell \) decoding iterations converges asymptotically to \( x_{\ell}^{(i)} \). The bit will not be recovered if its attached component codeword has more than \( t_{\varphi(i)} \) errors. According to \cite{25}, the total number of errors in \( B_i \) per component code constraint at the start of the \( \ell \)-th iteration converges to a Poisson random variable with mean \( M_{\varphi(i)} \left( x_{\ell}^{(i)} + x_{\ell-1}^{(i+1)} \right) \) as \( n_{\varphi(i)} \to \infty \), where the error probabilities \( x_{\ell}^{(i)} \) and \( x_{\ell-1}^{(i+1)} \) are taken into account due to coupling.

To characterize the iterative decoding process, one can first look at the error graph obtained from the corresponding Tanner graph, where all the VN's associated with the correctly received bits and their connected edges are removed. Then, the decoding of \( B_i \) is equivalent to removing any vertex in spatial position \( i \) and its edges connected to the vertices in position \( i + 1 \) if the number of those edges is no larger than \( t_{\varphi(i)} \). As a result, the iterative decoding is characterized by a recursive complementary Poisson cumulative distribution function. Note that since \( q_{\varphi(i)} \) is fixed and \( n_{\varphi(i)} \gg q_{\varphi(i)} \), the above properties hold regardless of whether the Tanner graph is single-edge or multi-edge. For notation simplicity, we define \( f(\lambda, t) \triangleq 1 - \sum_{i=1}^{t-1} \frac{\lambda^i}{i!} e^{-\lambda} \) to be the complementary Poisson cumulative distribution function for a Poisson random variable \( \lambda \) with support \( t \). The DE equation for SR-staircase codes is

\[ x_{\ell}^{(i)} = f \left( \frac{M_{\varphi(i)}}{2} \left( x_{\ell}^{(i-1)} + x_{\ell}^{(i+1)} \right), t_{\varphi(i)} \right), \tag{14} \]

where \( x_{0}^{(i)} = 1 \) for \( i \in [L] \) and \( x_{0}^{(i)} = 0 \) for \( i < 1 \) and \( i > L \). The BSC decoding threshold is defined as \( \bar{p} \triangleq \sup \left\{ p > 0 \mid \lim_{\ell \to \infty} x_{\ell}^{(i)} = 0 \right\} \).
2) : When \( w > 2 \), we have \( m_1 = m_2 \triangleq m \) and \( q_1 = q_2 \triangleq q \) according to Sec. II-A2. In this case, the expected number of initial errors per component code is \( M_1 = M_2 \triangleq M \). Recall that the \( l \)-th sub-block of preceding code block \( B_{i,l}^{\pi - 1} \) for \( l \in [w - 1] \) is used as a part of the inputs to encode \( B_i \). Similarly, \( B_i \) is also used as a part of the inputs to encode \( B_{i+1}, \ldots, B_{i+w-1} \).

The DE equation in (14) is then modified into
\[
x_{i}^{(\ell)} = f \left( \frac{M}{2(w-1)} \sum_{j=1}^{w-1} \left( x_{i-j}^{(\ell)} + x_{i+j}^{(\ell-1)} \right), t_{\varphi(i)} \right).
\] (15)

3) Windowed Decoding: The DE analysis above assumes that the decoding is performed for the entire spatial code chain. It is easy to extend the DE analysis to sliding window decoding. Consider a window size \( W \) satisfying \( w < W < L \). Then, the DE equation is modified into
\[
x_{i}^{(\ell)} = \begin{cases} 
\text{RHS of (14),} & \text{if } w = 2 \\
\text{RHS of (15),} & \text{if } w > 2 \\
x_{i}^{(\ell-1)}, & \text{otherwise}
\end{cases},
\] (i') \in [L - W + 1]
\]

where \( i' \in [L - W + 1] \) indicates the window position on the coupled code chain. It is important to note that under sliding window decoding, the error probability of coupled codes predicted by DE cannot reach 0 [40]. In this case, the definition of BSC decoding threshold should be modified by accounting for a target error probability \( \epsilon > 0 \) such that it becomes \( \bar{\epsilon} \triangleq \sup \left\{ p > 0 \mid \lim_{\ell \to \infty} x_{i}^{(\ell)} \leq \epsilon, \forall i \in [L] \right\} \). However, to accurately compute the threshold for \( w > 2 \), the window size needs to be very large for the decoding wave to form [40], [41].

C. Decoding Threshold Results

In this section, we use the DE equations to characterize the decoding threshold of SR-staircase codes under full decoding of the entire spatial code chain. We first investigate the effective channel quality \( \bar{M} \triangleq \sup \{ M > 0 \mid \lim_{\ell \to \infty} x_{i}^{(\ell)} = 0_L \} \) for SR-staircase codes with \( m_1 = m_2 \triangleq m \) and \( q_1 = q_2 \triangleq q \). This is because for given \( (t_1, t_2, w) \), \( \bar{M} \) becomes deterministic and will come in handy for quickly determining the BSC threshold of SR-staircase codes for various \( (m, q) \).

The results of \( \bar{M} \) are reported in Table I.

It can be seen that the effective channel quality improves with \( t_1, t_2 \) and \( w \). Notice that \( \bar{M} \leq t_1 + t_2 \), which is the necessary condition to guarantee successful decoding [25]. As both \( t_1 \) and \( t_2 \) become large, \( \bar{M} \) is getting closer to the \( t_1 + t_2 \) upper bound when \( w \) is large. Hence, it is more beneficial to use a large coupling width for a SR-staircase code with large \( (t_1, t_2) \) than that with small \( (t_1, t_2) \). Compared to the setting with \( t_1 = t_2 \), the one with \( t_1 \neq t_2 \) requires a larger
TABLE I
DECODING THRESHOLDS OF SR-STAIRCASE CODES IN TERMS OF EFFECTIVE CHANNEL QUALITY $\bar{M}$

| $(t_1,t_2)$ | (2, 2) | (3, 3) | (4, 4) | (5, 5) | (6, 6) | (7, 7) | (7, 8) | (8, 8) | (9, 9) | (10, 10) |
|------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|----------|
| $w = 2$    | 3.5880 | 5.7544 | 7.8397 | 9.8860 | 10.8607| 11.9087| 13.9434| 14.9517| 15.9655| 17.9875  |
| $w = 3$    | 3.5880 | 5.7548 | 7.8392 | 9.8854 | 10.9006| 11.9297| 13.9434| 14.9517| 15.9655| 17.9753  |
| $w = 4$    | 3.5880 | 5.7548 | 7.8392 | 9.8854 | 10.9028| 11.9297| 13.9434| 14.9517| 15.9655| 17.9753  |
| $w = 5$    | 3.5880 | 5.7548 | 7.8392 | 9.8854 | 10.9040| 11.9297| 13.9434| 14.9517| 15.9655| 17.9753  |
| $w = 6$    | 3.5880 | 5.7548 | 7.8392 | 9.8854 | 10.9040| 11.9297| 13.9434| 14.9517| 15.9655| 17.9753  |

$w$ for $\bar{M}$ to achieve its maximum value. Furthermore, it is interesting to note that this maximum value coincides with the potential threshold [42] of the GLDPC ensemble with $t$ error correcting constituent BCH codes [17, Table III]. This implies that choosing a reasonable coupling width, e.g., $w = 5$, is sufficient for the proposed codes to achieve the best possible threshold.

The BSC threshold $\bar{p}$ can then be easily determined by using $\bar{p} = \frac{\bar{M}}{2m}$ from (13). The following theorem provides a necessary condition for SR-staircase codes to achieve a higher rate and BSC threshold, and smaller block length than staircase codes when $t_1 = t_2 \triangleq t$.

**Theorem 1.** Consider a rate-$R'$ $(m', \nu', t')$ conventional staircase code with decoding threshold $\bar{p}'$ and effective channel quality $\bar{M}'$. For any rate-$R$ $(m, \nu, t, q)$ SR-staircase code with $t > t'$, $\nu \geq \nu'$, decoding threshold $\bar{p}$ and effective channel quality $\bar{M}$, satisfying

$$\left\lceil \frac{t \nu m'}{t' \nu' q} \right\rceil < \left\lfloor \frac{1}{q} \min \left\{ \sqrt{q m'}, \frac{\bar{M} m'}{\bar{M}} \frac{2^\nu - 1}{2} \right\} \right\rfloor,$$

we have $R \geq R'$, $\bar{p} > \bar{p}'$ and $\frac{m^2}{q} \leq (m')^2$.

**Proof:** See Appendix A.

Using Theorem 1 and the results from Table I, we can quickly determine whether it is possible construct a SR-staircase code that outperforms its conventional counterpart. In addition, it is possible to relax the rate requirement in Theorem 1 by introducing a small variable $\delta \in (0, 1)$ to allow SR-staircase codes to achieve a comparable rate to staircase codes, i.e., $R \geq R' - \delta$.

Once all the conditions in Theorem 1 are fulfilled, we can obtain $m = \left\lceil \frac{t \nu m'}{t' \nu' q} \right\rceil \cdot q$ from (34) in Appendix A since a smaller $m$ always gives rise to a larger BSC threshold for a given $\bar{M}$. When either $m_1 \neq m_2$ or $q_1 \neq q_2$, a search is required to find the optimal $m_1$ and $m_2$ that give the largest threshold.

We then design several SR-staircase codes for various rates and code block sizes by using Theorem 1 and the DE analysis. For simplicity, we consider $\nu_1 = \nu_2 \triangleq \nu$. The decoding
thresholds of the proposed codes and some existing staircase codes in the literature are reported in Table II. Since only hard channel output is used, the BSC threshold can be equivalently converted into the additive white Gaussian noise (AWGN) threshold. From Table II, it can be observed that the proposed codes achieve a larger threshold than the conventional staircase codes for the same or similar rates and with comparable block lengths. The threshold gain becomes larger if the conventional staircase codes are with a small \( t \), e.g., \( t \leq 3 \). More importantly, the actual coding gain of the proposed codes over staircase codes under iBDD can be larger than the corresponding threshold gain. This is because the thresholds gain is based on density evolution, where miscorrection-free iBDD is assumed [25]. For the staircase codes with a small \( t \), the error performance under iBDD will degrade due to miscorrection if their BCH component codes do not have any extended parity bits. In contrast, the proposed codes employ BCH component codes with larger \((t_1, t_2)\) such that the miscorrection probability can be greatly reduced. As a result, the actual coding gain of the proposed codes over staircase codes with a small \( t \) under iBDD is larger than the threshold gain based on density evolution. Nevertheless, the threshold gain still provide insights into designing good codes with better waterfall performance. It is also important to note
that \((q_1, q_2)\) should not be too large when \(w = 2\), i.e., \(\max\{q_1, q_2\} \leq \min\{t_1, t_2\}\). Otherwise, the error floor performance will become worse as we will see in Sec. IV. When using a large coupling width, we consider \(w \geq q\) by either choosing a large \(w\) if \(q\) is small or letting \(w = q\) if \(q\) is large. In most cases, this choice of coupling width is sufficient to achieve the largest decoding threshold according to Table I.

IV. ERROR FLOOR ANALYSIS

The error floor performance of the class of staircase codes is affected by stall patterns, which are referred to as a set of errors in the code block that cannot be corrected with iterative decoding as the number of iterations \(\ell \to \infty\). To determine the bit error rate (BER) due to stall patterns, we consider a fixed code block \(B_i\) and the error bits of stall patterns including positions in \(B_i\) and possibly additional positions in \(B_{i+1}, \ldots\) but not in \(B_{i-1}\). The BER of the error floor is dominated by the occurrence probability of the stall patterns with the smallest size [10], [23]. Consider a BSC with crossover probability \(p\). The BER can be approximated by using the union bound technique following [10]

\[
\text{BER}_{\text{floor}} \approx \frac{s_{\text{min}} A_{\text{min}} p^{s_{\text{min}}}}{m_1 m_2 \min\{q_1, q_2\}}, \tag{18}
\]

where \(A_{\text{min}}\) is the multiplicity of minimum stall patterns, and \(s_{\text{min}}\) is the number of error bits of a minimum stall pattern. The denominator \(\frac{m_1 m_2}{\min\{q_1, q_2\}}\) is the size of the code block in which a minimum stall pattern occurs. Since the stall patterns and the error floor behave completely different for different coupling widths, we analyze each term in (18) separately for different coupling widths. The analysis will be used to justify our choice of \(q_1, q_2,\) and \(w\).

A. Error Floor with \(w = 2\)

1) Minimum Stall Pattern Analysis: We first assume that a stall patterns only appears in the received blocks \(Y_i\) and \(Y_i^\pi\) as it allows us to easily determine \(s_{\text{min}}\). We denote by \(S_i\) the stall pattern matrix associated with \(Y_i\) such that \(Y_i = B_i + S_i\). In other words, the position of each non-zero element in \(S_i\) corresponds to the position of an error bit in \(Y_i\). Likewise, the stall pattern matrix associated with \(Y_i^\pi\) is denoted by \(S_i^\pi\), which is obtained from \(S_i\) by following the transformation in (2). We then have the following theorem for minimum stall patterns.
Fig. 4. Consider a SR-staircase code with $w = 2$, $(t_1, t_2) = (6, 4)$ and $(q_1, q_2) = (2, 3)$. A stall pattern is formed in (a) block $Y_1$, and (b) block $Y_2$. The errors in the bit positions that belong to the same component codeword are represented by the same marker with the same color.

**Theorem 2.** Consider a SR-staircase codes with parameters $(t_1, t_2)$, $(q_1, q_2)$, and $w = 2$. The exact number of the error bits of the minimum stall pattern is

$$s_{\min} = \min \left\{ \max \left\{ \left\lceil \frac{t_2 + 1}{q_1} \right\rceil (t_1 + 1), \left\lceil \frac{t_1 + 1}{q_1} \right\rceil (t_2 + 1) \right\}, \right.$$ 

$$\max \left\{ \left\lfloor \frac{t_1 + 1}{q_2} \right\rfloor (t_2 + 1), \left\lfloor \frac{t_2 + 1}{q_2} \right\rfloor (t_1 + 1) \right\} \right\}. \tag{19}$$

**Proof:** See Appendix B.

We use Example 3 to illustrate the idea of Theorem 2.

**Example 3.** Consider a SR-staircase code with $w = 2$, $(t_1, t_2) = (6, 4)$ and $(q_1, q_2) = (2, 3)$. The stall patterns formed in $Y_1 = [Y_{1,1}, Y_{1,2}, Y_{1,3}]$ and $Y_2 = [Y_{2,1}, Y_{2,2}]$ and their transformation in $Y_1^\pi = [Y_{1,1}^T, Y_{1,2}^T, Y_{1,3}^T]$ and $Y_2^\pi = [Y_{2,1}^T, Y_{2,2}^T]$ are illustrated in Fig. 4(a) and Fig. 4(b), respectively. As shown in the top figure of Fig. 4(a), the stall pattern formed in $Y_1$ has a size of $3 \times 5$. The transformation of this stall pattern in $Y_1^\pi$ is shown in the bottom figure of Fig. 4(a). On the other hand, a stall pattern with size $2 \times 7$ can be formed in $Y_1^\pi$ if we remove an error bit (represented by either the red, green, or blue marker) from the first erroneous row of $Y_1^\pi$. However, this is equivalent to removing an error bit from either the first, third, or fifth erroneous column in $Y_1$, leading to the correction of this stall pattern because one erroneous row in $Y_1$ will have at most 4 errors and $t_2 = 4$. Therefore, only the $3 \times 5$ stall pattern formed in $Y_1$ is not correctable during the decoding of $[Y_0^\pi, Y_1]$ and $[Y_1^\pi, Y_2]$. Similarly, a stall pattern formed in $Y_2$ has a minimum size of $3 \times 7$ as shown in the top figure of Fig. 4(b), whereas its transformation in $Y_2^\pi$ is illustrated in the bottom figure of Fig. 4(b). As a result, we have...
s_{\text{min}} = 15$ as the stall pattern formed in $Y_1$ has the smallest size.

2) Multiplicity Analysis: To determine multiplicity $A_{\text{min}}$, we consider that a minimum stall pattern can spread across $[Y_i^\pi, Y_{i+1}^\pi]$. From Theorem 2, we see that whether a minimum stall pattern occurs in the block with even or odd index depends on $q_1$ and $q_2$. Hence, we can consider $q_1 \geq q_2$ without loss of generality. As a result, the minimum stall pattern occurs in $Y_i, i \in 2\mathbb{N}$.

By inspecting $s_{\text{min}}$ in Theorem 2, it can be seen that a minimum stall pattern affects exactly $\left\lceil \frac{t_1+1}{q_1} \right\rceil$ rows and at most $\left\lceil \frac{s_{\text{min}}}{t_1+1} \right\rceil q_1$ columns in $[Y_i^\pi, Y_{i+1}^\pi]$. The intersections of these erroneous rows and columns form a rectangular array. We denote by $S_{\text{array}}$ and $S_{\text{stall}}$ the sets of error bit positions in the array and a minimum stall pattern, respectively, and define $Y_i^{\pi}$ and $Y_i$ to be the set of bit positions in $Y_i^\pi$ and $Y_i$, respectively. Clearly, we have $S_{\text{stall}} \subseteq S_{\text{array}} \subset (Y_i^{\pi} \cup Y_{i+1}^{\pi})$. The element in the $a$-th row and $b$-th column of matrix $[S_i^{\pi}, S_{i+1}]$, i.e., $S_{i,i+1}(a, b)$, is 1 when $(a, b) \in S_{\text{stall}}$ and 0 otherwise. Then, $A_{\text{min}}$ is the product of the number of ways to choose the positions of this array in $[Y_i^\pi, Y_{i+1}^\pi]$ and the multiplicity of minimum stall patterns formed in the array. We denote by $A_{\text{row}}$ and $A_{\text{col}}$ the number of ways to choose row and column indices, respectively, for $S_{\text{array}}$. It is immediate that

$$A_{\text{row}} = \left( \frac{m_1}{q_1} \left\lceil \frac{t_1+1}{q_1} \right\rceil \right).$$

To find $A_{\text{col}}$, we further divide the aforementioned rectangular array into $\left\lceil \frac{s_{\text{min}}}{t_1+1} \right\rceil$ sub-arrays of size $\left\lfloor \frac{t_1+1}{q_1} \right\rfloor \times q_1$ or $\left\lfloor \frac{t_1+1}{q_1} \right\rfloor \times q_2$. Hence, we have

$$S_{\text{array}} = \bigcup_{j=1}^{\left\lceil \frac{s_{\text{min}}}{t_1+1} \right\rceil} S_{\text{array},j},$$

where $S_{\text{array},j}$ is the $j$-th sub-array. The rectangular array is divided such that the sub-array satisfies either $S_{\text{array},j} \subset Y_i^{\pi}, S_{\text{array},j} \cap Y_{i+1}^{\pi} = \emptyset$ or $S_{\text{array},j} \subset Y_{i+1}, S_{\text{array},j} \cap Y_i^{\pi} = \emptyset$. In the former case, the sub-array is of size $\left\lfloor \frac{t_1+1}{q_1} \right\rfloor \times q_1$ and contains all possible positions of the error bits of an erroneous row vector in $Y_i$. In the latter case, the sub-array is of size $\left\lfloor \frac{t_1+1}{q_1} \right\rfloor \times q_2$ and contains all possible positions of the error bits of an erroneous row vector in $Y_{i+1}^{\pi}$. We denote by $(a, b)$ and $(a', b')$ a pair of position indices in $S_{\text{array},j}$, where $(a, b) \neq (a', b')$. Since all the bits of any erroneous row belong to the same component codeword, the column position indices of $S_{\text{array},j}$ satisfy $|b - b'| \in \{0, \frac{m_2}{q_2}, \ldots, \frac{m_1(q_1-1)}{q_1} \}$ when $S_{\text{array},j} \subset Y_i^{\pi}$ and $|b - b'| \in \{0, \frac{m_1}{q_1}, \ldots, \frac{m_1(q_2-1)}{q_1} \}$ when $S_{\text{array},j} \subset Y_{i+1}^{\pi}$. In other words, each sub-array always lies in the same column positions of each sub-block of $Y_i^{\pi}$ or $Y_{i+1}^{\pi}$. This means that given a column position of a sub-array $S_{\text{array},j}$, the rest of the column positions are deterministic. If there are $j$ sub-arrays in $Y_i^{\pi}$, i.e., $S_{\text{array},1} \subset Y_i^{\pi}, \ldots, S_{\text{array},j} \subset Y_i^{\pi}$, then there are $\left( \frac{m_2}{q_2} \right)$ ways to choose all column indices for
those $j$ sub-arrays. Similar arguments also apply to choosing the column indices for the other 
\[ \lceil \frac{s_{\min}}{t_1+1} \rceil - j \] sub-arrays in $Y_{i+1}$. As a result, we obtain the multiplicity of the column indices for the rectangular error array as

\[
A_{\text{col}} = \left( \begin{array}{c} m_2 \\ q_2 \end{array} \right) \begin{bmatrix} \frac{t_1}{q_1} \\ \frac{s_{\min}}{t_1+1} \end{bmatrix} + \mathbb{I} \left\{ q_2 > \frac{t_1}{q_1} \right\} \sum_{j=1}^{\left\lceil \frac{s_{\min}}{t_1+1} \right\rceil - 1} \left( \begin{array}{c} m_2 \\ q_2 \end{array} \right) \left( \begin{array}{c} \frac{m_2}{q_2} \\ j \end{array} \right) \left( \left\lfloor \frac{s_{\min}}{t_1+1} \right\rfloor - j \right),
\]

where the indicator function gives the condition that only the case $S_{\text{array}} \subseteq Y_1^\pi$, $S_{\text{array}} \cap Y_{i+1} = \emptyset$ is possible. The reasons are as follows. For any sub-array $S_{\text{array},j} \subseteq Y_{i+1}$, we know that its size is \( \lceil \frac{j+1}{q_1} \rceil \times q_2 \). Since this sub-array contains all the possible positions of the error bits of an erroneous row in $Y_{i+1}^\pi$, the erroneous row has at most $\lceil \frac{j+1}{q_1} \rceil q_2$ errors. This error vector is correctable by $C_1$ if $\lceil \frac{j+1}{q_1} \rceil q_2 \leq t_1$.

Example 4 illustrates the relationship between a minimum stall pattern and its associated error array and sub-arrays.

**Example 4.** Consider the SR-staircase code in Example 3 again. In the bottom figure of Fig. 4(a), a minimum stall pattern with size $s_{\min} = 15$ is inside a $2 \times 9$ array in $Y_1^\pi$. All the error bits of each erroneous row vector in $Y_1$ shown in the top figure of Fig. 4(a) are inside a $2 \times 3$ sub-array with its column positions marked by the dash lines with the same color in $Y_1^\pi$ in the bottom figure. In the bottom figure of Fig. 4(b), a (non-minimum) stall pattern formed in $Y_2^\pi$ is inside a $4 \times 6$ array. All the error bits of each erroneous error vector in $Y_2$ shown in the top figure in Fig. 4(b) are inside a $4 \times 2$ sub-array in $Y_2^\pi$. Note that the $2 \times 9$ array in $Y_1^\pi$ cannot spread into $Y_2$. If any of its three $2 \times 3$ sub-arrays is formed in $Y_2$, then this sub-array will become an erroneous row with at most 4 error bits in $Y_2^\pi$, which is correctable by $C_2$. Hence, the minimum stall pattern can only be formed in $Y_1^\pi$ rather than $[Y_1^\pi, Y_2]$.

It then remains to determine the multiplicity of minimum stall patterns formed in the error array. Following (21), consider that there are $j$ sub-arrays in $Y_i^\pi$ and the resultant error array is with size \( \lceil \frac{j+1}{q_1} \rceil \times (jq_1 + (\left\lfloor \frac{s_{\min}}{t_1+1} \right\rfloor - j)q_2) \). Next, we use an \( \lceil \frac{j+1}{q_1} \rceil \times \left\lfloor \frac{s_{\min}}{t_1+1} \right\rfloor \) integer matrix $A_{\text{array},j}$ to represent the error number assignment which assigns the error bits of a minimum stall pattern to the error array with $j$ sub-arrays contained in $Y_i^\pi$ and \( \left\lfloor \frac{s_{\min}}{t_1+1} \right\rfloor - j \) sub-arrays contained in $Y_{i+1}$. Its entry $A_{\text{array},j}(i_1, i_2)$ with $i_1 \in \left[ \left\lceil \frac{j+1}{q_1} \right\rceil \right]$ and $i_2 \in \left[ \left\lfloor \frac{s_{\min}}{t_1+1} \right\rfloor \right]$, represents the number of errors in the $i_1$-th row of the $i_2$-th sub-array. More importantly, $A_{\text{array},j}(i_1, i_2)$ must satisfy

\[
q_1 \geq A_{\text{array},j}(i_1, i_2) \geq t_1 + 1 - \left( \left\lceil \frac{j+1}{q_1} \right\rceil - 1 \right) q_1, \forall j_2 \in [j],
\]

(22)
\( q_2 \geq A_{\text{array},j}(i_1, i_2) \geq t_1 + 1 - \left( \left\lceil \frac{t_1 + 1}{q_2} \right\rceil \right) q_2, \forall i_2 \in \left[ \left\lceil \frac{s_{\text{min}}}{t_1 + 1} \right\rceil \right] \setminus [j], \) \tag{23}

\[
\sum_{i_1=1}^{\left\lceil \frac{t_1 + 1}{q_1} \right\rceil} A_{\text{array},j}(i_1, i_2) \geq t_2 + 1, \forall i_2 \in \left[ \left\lceil \frac{s_{\text{min}}}{t_1 + 1} \right\rceil \right],
\]

\[
\sum_{i_2=1}^{\left\lceil \frac{t_1 + 1}{q_1} \right\rceil} A_{\text{array},j}(i_1, i_2) \geq t_1 + 1, \forall i_1 \in \left[ \left\lceil \frac{t_1 + 1}{q_1} \right\rceil \right],
\]

\[
\sum_{i_1=1}^{\left\lceil \frac{t_1 + 1}{q_1} \right\rceil} \sum_{i_2=1}^{\left\lceil \frac{t_1 + 1}{q_1} \right\rceil} A_{\text{array},j}(i_1, i_2) = s_{\text{min}},
\] \tag{26}

where (22) and (23) give the ranges for the number of errors in each row of the \( i_2 \)-th sub-array in \( Y_i^\pi \) and \( Y_{i+1} \), respectively, (24) enforces the constraint that each row of a minimum stall pattern must have at least \( t_2 + 1 \) errors, (25) enforces the constraint that the total number of errors contained by each sub-array must be at least \( t_1 + 1 \), and finally (26) gives the constraint on the total number of errors of a minimum stall pattern.

**Example 5.** In the bottom figure of Fig. 4(a), the error number assignment of a minimum stall pattern to the \( 2 \times 9 \) array in \( Y_1^\pi \) is \( A_{\text{array},3} = \begin{bmatrix} 2 & 3 & 3 \\ 3 & 2 & 2 \end{bmatrix} \). Here, \( j = 3 \) because all the three \( 2 \times 3 \) sub-arrays are in \( Y_1^\pi \). Moreover, the entries of the first to third columns in \( A_{\text{array},3} \) correspond to the number of row errors in the sub-arrays marked with red, blue and green, respectively, in the bottom figure of Fig. 4(a).

In addition to the error number assignment, we also need to determine the error position assignment. For the \( i_1 \)-th row of the \( i_2 \)-th sub-array, there are either \( A_{\text{array},j}(i_1, i_2) \) ways to assign \( A_{\text{array},j}(i_1, i_2) \) errors for this sub-array contained in either \( Y_i^\pi \) or \( Y_{i+1} \). The assignment for each entry in \( A_{\text{array},j} \) is independent. Thus, given \( A_{\text{array},j} \), the combinations of all row error assignments has the form of either \( \prod_{i_1}^{q_1} \prod_{i_2}^{q_2} \left(A_{\text{array},j}(i_1, i_2)\right) \) or \( \prod_{i_1}^{q_1} \prod_{i_2}^{q_2} \left(A_{\text{array},j}(i_1, i_2)\right) \).

Finally, with (20) and (21) and the number of combinations of minimum stall patterns formed in the error array, the multiplicity \( A_{\text{min}} \) for the case \( q_1 \geq q_2 \) is obtained as

\[
A_{\text{min}} = \left( \left\lceil \frac{t_1 + 1}{q_1} \right\rceil \right) \left( \left\lceil \frac{t_1 + 1}{q_2} \right\rceil \right) \sum_{i_1=1}^{\left\lceil \frac{t_1 + 1}{q_1} \right\rceil} \prod_{i_2=1}^{\left\lceil \frac{t_1 + 1}{q_1} \right\rceil} \left( \prod_{i_1=1}^{\left\lceil \frac{t_1 + 1}{q_1} \right\rceil} \prod_{i_2=1}^{\left\lceil \frac{t_1 + 1}{q_1} \right\rceil} \left(A_{\text{array},j}(i_1, i_2)\right) \right)
\]

\[
+ 1 \left\{ q_2 \geq \frac{t_1 + 1}{q_1} \right\} \sum_{j=1}^{\left\lceil \frac{t_1 + 1}{q_1} \right\rceil} \left( \left\lceil \frac{t_1 + 1}{q_2} \right\rceil \right) \sum_{j=1}^{\left\lceil \frac{t_1 + 1}{q_1} \right\rceil} \left( \left\lceil \frac{s_{\text{min}}}{t_1 + 1} \right\rceil - j \right)
\]

\[
\times \sum_{A_{\text{array},j}} \prod_{i_1=1}^{\left\lceil \frac{t_1 + 1}{q_1} \right\rceil} \prod_{i_2=1}^{\left\lceil \frac{t_1 + 1}{q_1} \right\rceil} \left( A_{\text{array},j}(i_1, i_2) \right) \prod_{i_2=1}^{\left\lceil \frac{t_1 + 1}{q_1} \right\rceil} \left( A_{\text{array},j}(i_1, i_2') \right), \] \tag{27}
where the summation over $A_{\text{array},j}$ takes all the possible non-identical $A_{\text{array},j}$ with each of its entry satisfying (22)-(26). Finding the number of such matrices is closely related to the problem of matrices with prescribed row and column sums [45].

For the case of $q_2 \geq q_1$, the multiplicity $A_{\text{min}}$ can be directly obtained from (27) by swapping the argument between $m_1$ and $m_2$, $q_1$ and $q_2$, as well as $t_1$ and $t_2$.

3) Code Block Index and Size: We know that the minimum stall pattern occurs in $Y_i$ for $i \in 2\mathbb{N}$ when $q_1 \geq q_2$ and $i \in 2\mathbb{N} - 1$ when $q_1 \geq q_2$. Hence, the block which has the minimum stall pattern, contains $\frac{m_1 m_2}{\min\{q_1, q_2\}}$ bits.

Remark 2. Based on Theorem 2, it is desirable to have $\max\{q_1, q_2\} \leq \min\{t_1, t_2\}$ when $w = 2$ to ensure that any minimum stall pattern will not become a one-dimensional vector whose $s_{\text{min}}$ becomes very small. Although the size of a minimum stall pattern for SR-staircase codes is smaller than that for the conventional staircase codes when both codes are with the same $(t_1, t_2)$, the proposed codes can still achieve a better error floor due to much smaller multiplicity $A_{\text{min}}$ and the use of component codes with larger $(t_1, t_2)$. In addition, we note that the error floor can be improved by using some post-processing techniques proposed for the conventional staircase codes, e.g., [46, Sec. V-A]. For example, the simplest way is to flip the aforementioned error array that contains a minimum stall pattern, such that the residue errors will be corrected by iBDD. However, the analysis on the error floor after post-processing is non-trivial and beyond the scope of this work.

B. Error Floor with $w > 2$

For a large coupling width, we need to set $m_1 = m_2 \triangleq m$ and $q_1 = q_2 \triangleq q$ according to Sec. II-A2. Moreover, we are particularly interested in the case of $w \geq q + 1$ since this choice allows the proposed codes to achieve the largest decoding threshold as discussed at the end of Sec. III-C. In the interest of space, we consider $w \geq q + 1$ in the subsequent analysis.

1) Minimum Stall Pattern Analysis: Following Sec. IV-A1, we use $S_i$ and $S_{\pi i}$ to represent the stall pattern matrices associated with $Y_i$ and $Y_{\pi i}$, respectively. For notation simplicity, we define the stall pattern matrix associated with the coupling sub-blocks in (8)-(9) as $[S_{i-t+1,l}]_{l=1}^{w-1} \triangleq [S_{i-t+1,1}, S_{i-t+1,2}, \ldots, S_{i-t+1,w-1}]_l$. Obtaining the exact analytical expression for $s_{\text{min}}$ is difficult as it varies with $w$. Alternatively, we derive a lower bound on $s_{\text{min}}$, which will provide insights into the upper bound on the BER of the error floor.
Theorem 3. Consider a SR-staircase code with parameters \((t_1, t_2), m_1 = m_2 \triangleq m, q_1 = q_2 \triangleq q,\) and \(w \geq q + 1\). The error number of the minimum stall pattern is lower bounded by
\[
s_{\min} \geq \frac{(\min\{t_1, t_2\} + 1)(\min\{t_1, t_2\} + 2)}{2}.
\] (28)

Proof: See Appendix \[C\] \[\blacksquare\]

Based on Theorem (3), we have the following useful lemma.

Lemma 1. Consider the SR-staircase code in Theorem (3) with \(w \geq q + 1\) and assume \(t_1 \neq t_2\). If \((q, w, t_1, t_2)\) further satisfy one of the following conditions: 1) \(\min\{t_1, t_2\} \geq q\); 2) \(\min\{t_1, t_2\} + 1 \leq q\) and \(w \leq 2(\min\{t_1, t_2\} + 1)\), \(s_{\min}\) is strictly larger than the lower bound in (28).

Proof: See Appendix \[D\] \[\blacksquare\]

Corollary 1 follows immediately from Theorem (3) and Lemma 1 and their proofs in Appendices \[C\]-\[D\].

Corollary 1. For the SR-staircase code in Theorem 3 with \(w \geq q + 1\), \(s_{\min}\) achieves its lower bound in (28) if and only if \(w \geq (1\{t_1 \neq t_2\} + 1)(\min\{t_1, t_2\} + 1) + 1\) and \(q \geq \min\{t_1, t_2\} + 1\).

Remark 3. Notice that all of our designs in Table II satisfy \(|t_1 - t_2| \in \{0, 1\}\) because these designs achieve a better threshold than those with \(|t_1 - t_2| > 1\). Under this condition, the lower bound of \(s_{\min}\) in Theorem 3 is larger than the exact \(s_{\min}\) for \(w = 2, q_1 \geq 2\) and \(q_2 \geq 2\) in Theorem 2. Hence, the error floor can be improved by increasing \(w\). In addition, Lemma 1 shows that if both \(q\) and \(w\) are not too large, the size of the minimum stall pattern can become larger. In fact, this is also suggested according to Tables I-II because a moderate value of \(q\) and \(m\) suffice to achieve the best decoding threshold. Hence, a proper choice of \((q, w, t_1, t_2)\) would lead to a better trade-off between waterfall and error floor for SR-staircase codes.

2) Multiplicity Analysis: We find \(A_{\min}\) by assuming that \(s_{\min}\) achieves its lower bound. Hence, the code parameters satisfies the conditions in Corollary 1.

To begin with, we assign a row of \(\min\{t_1, t_2\} + 1\) errors to \(B_i\) such that the conditions of (61) and (62) in Appendix \[D\] are satisfied. Consider an erroneous row with index \(r_c\) in \(\left[[Y^\pi_{i-t+z}, l_i\right]]_{l=1}^{w-1} , Y_{i+z}\), where \(\bar{z} = \left\lceil \frac{wq}{m} \right\rceil\) and \(\bar{z} \in [w - 1] \cap (2\mathbb{N})\) by (58) in Appendix \[D\]. From (57)-(60) in Appendix \[D\] we know that the number of errors of each affected row is deterministic. As for the positions of those error bits, it can be seen that the column position of each error
Fig. 5. Consider a SR-staircase code with $w = 7$, $(t_1, t_2) = (2, 3)$ and $q = 6$. A minimum stall pattern with $s_{\text{min}} = 6$ is formed in blocks $Y_i, Y_{i+2}$ and $Y_{i+4}$ as well as their corresponding coupled sub-blocks. The position of each error bit is also shown.

bit in $[Y_{i-i+t, l}]_{l=1}^{w-1}$ is determined by the row position of that bit in the previous received block. Meanwhile, the row position of each error bit in $[Y_{i-i+t, l}]_{l=1}^{w-1}$ must be the same as that for the erroneous row in $Y_{i+1}$, which also determines the column position of that bit in the succeeding coupled blocks. In other words, once a row of $\min\{t_1, t_2\} + 1$ errors are assigned to $B_i$, the row and column positions of the rest of the error bits are determined. Therefore, the multiplicity is

$$A_{\text{min}} = \left( \frac{\min\{t_1, t_2\} + 1}{m} \right) \left( \frac{m}{q} \right)^{\min\{t_1, t_2\} + 1}$$

(29)

$$\geq \frac{m^{\min\{t_1, t_2\} + 2}}{(w - 1)q^{\min\{t_1, t_2\} + 1}}$$

(30)

where (30) holds for $w = (\mathbb{I}\{t_1 \neq t_2\} + 1)(\min\{t_1, t_2\} + 1) + 1$. Plugging (29) and (28) into (18) gives the estimation of the error floor.

**Example 6.** Consider a SR-staircase code with $(t_1, t_2, q, w) = (2, 3, 6, 7)$. Fig. 5 shows a minimum stall pattern with $s_{\text{min}} = 6$ formed in $[Y_{i-i+t, l}]_{l=1}^{16}, Y_{i+2}$] for $\bar{z} = 0, 2, 4, 6$. As shown in Fig. 5 given the row and column positions of each error bit in $Y_i$, the positions of the rest of the error bits are deterministic.

If $(t_1, t_2, q, w)$ satisfy the conditions in Lemma 1 the minimum stall pattern size is strictly larger than (28). Since it is difficult to find the exact minimum stall pattern size and its multiplicity in this case, we can use (28) and (30) to obtain an upper bound of its true error floor.
V. Numerical Results

We evaluate the performance of SR-staircase codes over the AWGN channel. A maximum of ten decoding iterations were performed over a decoding window. It should be noted that all BCH component codes used in our designs do not have any extended parity bits.

A. Theoretical Analysis Verification

We first use simulation results to validate our theoretical analysis by assuming miscorrection-free iBDD. We construct three SR-staircase codes with parameters $(m, \nu, t, q, w) = (126, 8, 2, 2, 2)$, $(126, 8, 2, 2, 3)$, and $(441, 9, 3, 3, 2)$, respectively. The decoding window size is set to $W = 7$. The simulated BER, decoding threshold and the estimated error floor BER$_{\text{floor}}$ are shown in Fig. 6. For the SR-staircase codes with $w = 2$, their simulated error floor BER matches closely to BER$_{\text{floor}}$ based on Theorem 2 and (27). Clearly, increasing $w$ leads to a lower error floor. It is also interesting to note that the code with $w = 3$ achieves a lower error floor than its estimated error floor BER$_{\text{floor}}$. This is because the code parameters $(t, q, w) = (2, 2, 3)$ satisfy the conditions in Lemma 1 such that the size of the minimum stall pattern is strictly larger than that in Theorem 3. Consequently, the BER$_{\text{floor}}$ based on 28 and (30) can only serve as an upper bound of the true error floor. Observe that the simulated waterfall performance for all the codes is also in agreement with the derived decoding threshold (the threshold curves for the codes with $t = 2$ and $w \in \{2, 3\}$ are overlapped). Therefore, both DE and error floor analysis can be used to...
effectively predict the simulated performance if the probability of miscorrection is low, which is the case in our subsequent design with a large \( t \).

**B. Performance Comparison**

Next, we compare the designed SR-staircase codes with the conventional staircase codes. For SR-staircase codes (labeled as “SR-SC”), we consider two designs from Table II, whose parameters are \((m, \nu, t, q, w) = (876, 11, 5, 3, 2)\), and \((m, \nu, t_1, t_2, q, w) = (964, 11, 6, 5, 4, 5)\), respectively. We also consider two benchmark conventional staircase codes, where the first one (labeled as “SC1”) has parameters \((m_1, m_2, \nu, t) = (510, 512, 10, 3)\) and two parity bits extended for BCH component codes following [10, Sec. IV-C] while the second one (labeled as “SC2”) has parameters \((m, \nu, t) = (478, 10, 3)\) and no extended parity bits. Notice that the BCH component codes of SR-staircase codes have a larger minimum distance than those of staircase codes. Thus, the decoding complexity of SR-staircase codes is expected to be higher than that of the benchmark staircase codes. All the codes have rate 0.9372 and comparable code block size as shown in Table II. The decoding window size is set to \( W = 9 \) for demonstration purposes. It can be reduced for achieving a lower decoding latency [47] at the cost of slightly inferior waterfall performance for both types of codes. The BER under iBDD (solid lines), miscorrection-free iBDD (dashed lines, labeled as “MF”), and the estimated error floor \( \text{BER}_{\text{floor}} \) are shown in Fig. 7 (the BER\(_{\text{floor}}\) of the SR-staircase code with \( w = 5 \) is not shown in the figure as it
is in the order of $10^{-33}$). Observe that SC2 under iBDD has the worst performance due to the highest probability of miscorrection. Even though SC1 uses two additional parity bits to reduce miscorrection probability, it still has a noticeable gap to its miscorrection-free performance. In contrast, all the proposed codes operate close to their miscorrection-free performance with iBDD and outperform the conventional staircase codes in terms of better waterfall and error floor performance. Most notably, the SR-staircase code with $w = 5$ has the best performance among all the codes and achieves slightly better waterfall performance with iBDD than the conventional staircase code with miscorrection-free iBDD.

C. Impacts of Decoding Window Size

We investigate the impacts of decoding window size on the performance of SR-staircase codes. Consider a SR-staircase code with parameters $(m, \nu, t, q, w) = (216, 9, 4, 4, 4)$ following Table II. In addition, we also consider a benchmark staircase code with parameters $(m, \nu, t) = (114, 9, 2)$ and one parity bit extended for BCH component codes following [37, Table I]. Both codes have the same rate 0.8333 while the designed SR-staircase code has a slightly smaller block size (11664 bits) than the benchmark staircase code (12996 bits). The error performance for both codes under iBDD with window size $W \in \{6, 7, 8, 9\}$ is shown in Fig. 8.

![Fig. 8. BER performance of SR-staircase codes and staircase codes with different decoding window sizes.](image)

The proposed SR-staircase codes outperform benchmark staircase codes in terms of waterfall and error floor performance for all the considered window sizes. For both codes, we see that
increasing the window size leads to improved waterfall performance. It is also worth noting that the proposed code with the smallest window size \( W = 6 \) outperform the staircase code with the largest window size \( W = 9 \). This demonstrates that the proposed codes are capable of achieving better error performance with a lower decoding latency than staircase codes.

VI. CONCLUDING REMARKS

We proposed SR-staircase codes, a new class of spatially coupled product codes. The proposed codes are derived from the conventional staircase codes and have a larger design space. The most appealing feature is that one can employ stronger BCH component codes to construct a SR-staircase code with a similar or the same rate and block size as staircase code. The decoding threshold and the error floor of SR-staircase codes were analyzed by using DE and the union bound technique, respectively. Both theoretical and simulation results demonstrate the superior performance of the proposed codes over staircase codes in terms of waterfall and error floor. In addition, it was shown that increasing the coupling width can further improve the performance.

For future works, it would be interesting to consider the design and analysis of the proposed SR-staircase codes with other component codes. Another worthwhile direction could be designing low-complexity concatenating coding schemes for soft-decision channels, where inner codes will use soft-decision decoding and SR-staircase codes under iBDD will be used as outer codes.

APPENDIX A: PROOF OF THEOREM 1

First, in order to satisfy the rate requirement, we have

\[
R \geq R' \Rightarrow 1 - \frac{t\nu}{m} \geq 1 - \frac{t'\nu'}{m'} \Rightarrow m \geq \frac{t\nu m'}{t'\nu'}. \tag{31}
\]

Then, to satisfy the BSC threshold requirement, we have

\[
\bar{p} > \bar{p}' \Rightarrow \frac{\bar{M}}{m} > \frac{\bar{M}'}{m'} \Rightarrow m < \frac{\bar{M}}{\bar{M}'} m'. \tag{32}
\]

The block length requirement leads to

\[
\frac{m^2}{q} \leq (m')^2 \Rightarrow m \leq \sqrt{qm'}. \tag{33}
\]

Combining (31)-(33) and \( m \leq \frac{2^{\nu+1}}{2} \), we have \( R \geq R' \), \( \bar{p} > \bar{p}' \) and \( \frac{m^2}{q} \leq (m')^2 \) for any \( m \) with

\[
\left\lfloor \frac{t\nu m'}{t'\nu'q} \right\rfloor \cdot q \leq m < \left\lfloor \frac{1}{q} \min \left\{ \sqrt{qm'}, \frac{\bar{M}'}{M'} m', \frac{2^{\nu} - 1}{2} \right\} \right\rfloor \cdot q, \tag{34}
\]

where \( [.] \) and \( \lfloor . \rfloor \) ensure that \( m \) is divisible by \( q \). In order to let (34) hold, one must have (17).
Appendix B: Proof of Theorem 2

First, we consider $i \in 2 \mathbb{N}$. Define $s_{i,r_1}$ to be the non-zero row of stall pattern matrix $S_i$ with index $r_1$, $s_{i-r_2}$ to be the non-zero row of the transformed stall pattern matrix $S_i^\pi$ with index $r_2$, and $\mathcal{R}_1$ and $\mathcal{R}_2$ to be the collections of indices $r_1$ and $r_2$, respectively, where $\mathcal{R}_1 \subseteq [\frac{m_2}{q_2}]$ and $\mathcal{R}_2 \subseteq [\frac{m_1}{q_1}]$. Since any stall pattern in $Y_i$ must not be correctable during the decoding of $[Y_i, Y_i^\pi, Y_i+1]$, then each non-zero row of $S_i$ and $S_i^\pi$ must satisfy

\[ w_H(s_{i,r_1}) \geq t_1 + 1, \forall r_1 \in \mathcal{R}_1 \triangleq \{ r_1 | s_{i,r_1} \in S_i, s_{i,r_1} \neq 0 \}, \]  
\[ w_H(s_{i-r_2}^\pi) \geq t_2 + 1, \forall r_2 \in \mathcal{R}_2 \triangleq \{ r_2 | s_{i-r_2}^\pi \in S_i^\pi, s_{i-r_2}^\pi \neq 0 \}, \]  
\[ \sum_{r_1 \in \mathcal{R}_1} w_H(s_{i,r_1}) = \sum_{r_2 \in \mathcal{R}_2} w_H(s_{i-r_2}^\pi). \]  

Recall that since $B_i^\pi = [B_{i,1}^\pi, \ldots, B_{i,q_1}^\pi]$, all bits in the same column position of every sub-block $B_{i,q}^\pi, l \in [q_1]$ belong to the same component codeword of $C_i$. This means that for any non-zero row vector with no less than $t_1 + 1$ errors in $S_i$, all these error bits occupy at least $[\frac{t_1+1}{q_1}]$ rows in $S_i^\pi$ due to the transformation in (2) in Section II-A1. Thus, the lower bounds on the required number of non-zero rows and error bits in $S_i^\pi$ to form a stall pattern are

\[ |\mathcal{R}_2| \geq \left[ \frac{t_1 + 1}{q_1} \right], \]  
\[ \Rightarrow \sum_{r_2 \in \mathcal{R}_2} w_H(s_{i-r_2}^\pi) \geq |\mathcal{R}_2| \min_{r_2 \in \mathcal{R}_2} \left\{ w_H(s_{i-r_2}^\pi) \right\} \geq \left[ \frac{t_1 + 1}{q_1} \right] \cdot (t_2 + 1). \]  

We are left with determining the required minimum number of the error bits in $S_i$ to form a stall pattern. To ensure that all the error bits of each erroneous row vector in $S_i$ only occupy at most $[\frac{t_1+1}{q_1}]$ rows in $S_i^\pi$ (otherwise, the size of the stall pattern in $S_i^\pi$ would become larger), each non-zero row of $S_i$ must satisfy

\[ \left[ \frac{t_1 + 1}{q_1} \right] \cdot q_1 \geq w_H(s_{i,r_1}) \geq t_1 + 1, \forall r_1 \in \mathcal{R}_1. \]  

Then, we obtain the minimum number of non-zero rows and error bits of $S_i$

\[ |\mathcal{R}_1| \geq \left[ \frac{\sum_{r_1 \in \mathcal{R}_1} w_H(s_{i,r_1})}{\max\{ w_H(s_{i,r_1}) \} \} \right] \geq \left[ \frac{t_1 + 1}{q_1} \right], \]  
\[ \Rightarrow \sum_{r_1 \in \mathcal{R}_1} w_H(s_{i,r_1}) \geq |\mathcal{R}_1| \min_{r_1 \in \mathcal{R}_1} \left\{ w_H(s_{i,r_1}) \right\} \geq \left[ \frac{t_1 + 1}{q_1} \right] \cdot (t_1 + 1). \]
To ensure that the conditions of (37), (39) and (41) are fulfilled simultaneously, the minimum number of error bits to form a stall pattern in $Y_i$ with $i \in 2\mathbb{N}$ is obtained as

$$s_{\text{min}} = \max \left\{ \min \left\{ \sum_{r_1 \in R_1} w_H(s_{i,r_1}) \right\}, \min \left\{ \sum_{r_2 \in R_2} w_H(s_{i,r_2}) \right\} \right\} \tag{42}$$

$$= \max \left\{ \left[ \frac{t_2 + 1}{q_1} \right] (t_1 + 1), \left[ \frac{t_1 + 1}{q_1} \right] (t_2 + 1) \right\}. \tag{43}$$

The $s_{\text{min}}$ for the case of $i \in 2\mathbb{N} + 1$ can be easily obtained from (43) by swapping the subscripts between 1 and 2. By taking the minimum of $s_{\text{min}}$ obtained for these two cases, the expression in (19) of Theorem 2 follows.

**APPENDIX C: PROOF OF THEOREM 3**

We first consider that the stall pattern spreads from block $Y_i$ to $Y_{i+1}, \ldots$. Following (35) in Appendix B, the weight of each non-zero row in $S_i$ satisfies

$$w_H(s_{i,r_1}) \geq t_{\phi(i)} + 1, \forall r_1 \in R_1 \subseteq \left\lfloor \frac{m}{q} \right\rfloor. \tag{44}$$

Due to coupling (9), the errors in one erroneous row vector in $Y_i$ will spread to some of the $w - 1$ consecutive received blocks $Y_{i+1}, \ldots, Y_{i+w-1}$ and affect at least $t_{\phi(i)} + 1$ rows, where each affected row is not correctable if a stall pattern is formed. This is because since $w \geq q + 1$, the erroneous row of each decomposed sub-blocks of $Y_i$ will become a column of errors in different received blocks due to coupling. Then, the corresponding stall pattern matrices satisfy

$$S_i \neq 0 \Rightarrow S^\pi_i = [S^\pi_{i,1}, \ldots, S^\pi_{i,w-1}] \neq 0 \tag{45}$$

$$\Rightarrow \left[ ([S^\pi_{i-l+1,1}]_{l=1}^{w-1})^T, ([S^\pi_{i-l+2,1}]_{l=1}^{w-1})^T, \ldots, ([S^\pi_{i-l+w-1,1}]_{l=1}^{w-1})^T \right]^T \neq 0 \tag{46}$$

$$\Rightarrow S^\pi_{\Sigma} \triangleq \left[ ([S^\pi_{i-l+1,1}]_{l=1}^{w-1})^T, ([S^\pi_{i-l+2,1}]_{l=1}^{w-1})^T, \ldots, ([S^\pi_{i-l+w-1,1}]_{l=1}^{w-1})^T \right]^T \neq 0, \tag{47}$$

where (46) follows by combining the stall pattern matrices associated with all the coupled sub-blocks, and (47) follows by considering the worst case where the stall pattern spreads to $[[Y^\pi_{i-l+\tau,1}]_{l=1}^{w-1}, Y_{i+\tau}]^T$ for some $\tau \geq w - 1$. For notation simplicity, we define the combined received block $[Y^\pi_\Sigma, Y_\Sigma] \triangleq [[Y^\pi_{i-l+1,1}]_{l=1}^{w-1}, Y_{i+1}]^T, \ldots, [[Y^\pi_{i-l+\tau,1}]_{l=1}^{w-1}, Y_{i+\tau}]^T]$, such that all erroneous rows except those in $Y_i$, are in this combined received block. Then, we obtain the
following conditions on each non-zero row of the corresponding combined stall pattern matrix 
\[ S^π_Σ, S_Σ \] with \( S^π_Σ \) and \( S_Σ \) defined in (47)
\[
\begin{align*}
  w_H([s^π_{rc}, s_{rc}]) &\geq \min\{t_1, t_2\} + 1, \forall r_c \in R_c \triangleq \left\{ r_c \mid s^π_{rc} \in S^π_Σ, s_{rc} \in S_Σ, [s^π_{rc}, s_{rc}] \neq 0 \right\}. \quad (48)
\end{align*}
\]
where \( r_c \) is the index of a non-zero row in \( [S^π_Σ, S_Σ] \) and \( R_c \subseteq \left\lceil \frac{m}{q} \right\rceil \) denotes the corresponding set of indices. Then, the total number of affected rows in \( [Y^π_Σ, Y_Σ] \) is lower bounded by the minimum number of row errors in \( Y_i \) due to coupling and (44)
\[
|R_c| \geq w_H(s_{i,r_1}) \geq t_ϕ(i) + 1. \quad (49)
\]
With (48) and (49), we lower bound the total number of error bits occur in \( [Y^π_Σ, Y_Σ] \)
\[
\sum_{r_c \in R_c} w_H([s^π_{rc}, s_{rc}]) \geq |R_c|(|\min\{t_1, t_2\} + 1) \geq (t_ϕ(i) + 1)(\min\{t_1, t_2\} + 1). \quad (50)
\]
Finally, using the fact that the number of errors in each erroneous code block is equal to that of its transformation (e.g., the number of errors in \( S_i \) is the same as in \( S^π_i \)), we obtain that
\[
\begin{align*}
  s_{\min} &= \sum_{r_c \in R_c} w_H(s^π_{rc}) \\
  &= \sum_{r_c \in R_c} w_H(s_{rc}) + \sum_{r_1 \in R_1} w_H(s_{i,r_1}) \\
  &= \sum_{r_c \in R_c} w_H([s^π_{rc}, s_{rc}]) + \sum_{r_1 \in R_1} w_H(s_{i,r_1}) \\
  &\geq \frac{(t_ϕ(i) + 1)(\min\{t_1, t_2\} + 1) + (t_ϕ(i) + 1)}{2} \quad \text{(by (44) & (50))} \\
  &\geq \frac{(\min\{t_1, t_2\} + 2)(\min\{t_1, t_2\} + 1)}{2}. \quad (51)
\end{align*}
\]

APPENDIX D: PROOF OF LEMMA 1

We use the notations and definitions from Appendix C and prove this lemma by contradiction. Consider \( t_1 < t_2 \) without loss of generality and assume that \( s_{\min} \) achieves the lower bound in (28) in Theorem 3 with \( (t_1, t_2, q, w) \) satisfying the conditions in Lemma 1, i.e.,
\[
s_{\min} = \frac{(t_1 + 1)(t_1 + 2)}{2}. \quad (52)
\]
By (44), (48) and (49) in Appendix C, the following conditions must hold simultaneously
\[
\begin{align*}
  w_H(s_{i,r_1}) &= t_1 + 1, r_1 \in R_1, |R_1| = 1, \\
  w_H([s^π_{rc}, s_{rc}]) &= t_1 + 1, r_c \in R_c, |R_c| = t_1 + 1. \quad (53) & (54)
\end{align*}
\]
It is important to note that $w_H(s^\pi_{r_c})$ gives the minimum number of erroneous rows above row $r_c$ while $w_H(s_{r_c})$ gives the minimum number of rows affected by row $r_c$ due to the spreading of errors as a result of the coupling in (9). If either $|\mathcal{R}| > 1$ or $w_H(s_{i,r_1}) > t_1 + 1$, then the number of affected rows caused by the errors in $Y_i$ is strictly larger than $t_1 + 1$, i.e., $|\mathcal{R}| > t_1 + 1$, leading to $s_{\min}$ larger than (52) and thus is not possible. Note that this will also be case if $w_H([s^\pi_{r_c}, s_{r_c}]) > t_1 + 1$, which cannot happen. In addition, if $|\mathcal{R}| < t_1 + 1$, one will get

$$|\mathcal{R}| < t_1 + 1 \Rightarrow \mathbb{E}_{r_c \in \mathcal{R}_c} [w_H([s^\pi_{r_c}, s_{r_c}])] \geq \frac{2s_{\min} - w_H(s_{i,r_1})}{|\mathcal{R}|} \geq t_1 + 1$$

(55)

$$\Rightarrow w_H([s^\pi_{r_c}, s_{r_c}]) > t_1 + 1, \exists r_c \in \mathcal{R}_c,$$

(56)

where (55) follows that the average number of row errors of the stall pattern must be greater than $t_1 + 1$ if $|\mathcal{R}_c| < t_1 + 1$, which leads to (56) that there must exist an erroneous row with index $r_c'$ such that the number of row errors is larger than $t_1 + 1$. However, (56) implies that $|\mathcal{R}_c| > t_1 + 1$, which is contradictory to $|\mathcal{R}_c| < t_1 + 1$. Thus, (54) must hold.

Based on (45)-(47) in Appendix C, (53) guarantees that

$$\left[[S^\pi_{i-l+z,l}]_{l=1}^{w-1}, S_{i+z}\right] = 0, \forall z \in \left[w - 1\right] \cap \left(2\mathbb{N} - 1\right)$$

(57)

$$\Rightarrow S^\pi_{i,l} = 0, \forall l \in \left[w - 1\right] \cap \left(2\mathbb{N} - 1\right).$$

(58)

If (58) is not satisfied, then there will be at least one erroneous row in $[Y^\pi_{\Sigma}, Y_{\Sigma}]$ defined in Appendix C with at least $t_2 + 1$ errors, leading to $s_{\min}$ larger than (52), which cannot happen.

We then determine the number of errors of each affected row caused by the errors spreading from the erroneous row in $Y_i$. To get the position of each affected row index, we list all elements of $\mathcal{R}_c$ as a sequence in ascending order and define a bijective function $g : \mathcal{R}_c \rightarrow [t_1 + 1]$ that maps index $r_c$ to its position of the sequence, i.e., $g(\min\{\mathcal{R}_c\}) = 1, g(\min\{\mathcal{R}_c \setminus \min\{\mathcal{R}_c\}\}) = 2, \ldots, g(\max\{\mathcal{R}_c\}) = t_1 + 1$. Consider that the $g(r_c)$-th affected row is in $[[S^\pi_{i-l+z,l}]_{l=1}^{w-1}, S_{i+z}]$, where $\bar{z} = \left\lfloor \frac{w}{m} \right\rfloor$ and $\bar{z} \in [w - 1] \cap (2\mathbb{N})$ by (58). Then, $\forall r_c \in \mathcal{R}_c$, the following must hold

$$\left(w_H(s^\pi_{r_c}), w_H(s_{r_c})\right) = \left(g(r_c), t_1 + 1 - g(r_c)\right),$$

(59)

$$\sum_{j=1}^{n} w_H(s^\pi_{i+z, r'_j}) = 1, \forall r'_j \in \mathcal{L}_{i+z} \subseteq [w - 1] \cap (2\mathbb{N}), |\mathcal{L}_{i+z}| = t_1 + 1 - g(r_c).$$

(60)

For (59), since there are $g(r_c)$ erroneous rows (including the erroneous row in $Y_i$) above the $g(r_c)$-th affected row, hence $w_H(s^\pi_{r_c}) \leq g(r_c)$. However, if $w_H(s^\pi_{r_c}) < g(r_c)$, then $w_H(s_{r_c}) > t_1 + 1 - g(r_c)$, leading to $|\mathcal{R}_c| > t_1 + 1$, which is contradictory to (54). Thus, (59) must hold.
As for (60), it means that the \( l' \)-th sub-block of \( Y_{i+z} = [Y_{i+z,1}, \ldots, Y_{i+z,w-1}] \), i.e., \( Y_{i+z,l'} \), must have only one error, where \( l' \) is even according to (58). \( L_{i+z} \) is the collection of these even indices, and \( s_{i+z,l',j} \) denotes the \( j \)-th row of the corresponding stall pattern matrix \( S_{i+z,l'} \). If \( \sum_{j=1}^{m} w_H(s_{i+z,l',j}) > 1 \), then \( S_{i+z,l'} \) must have either more than one non-zero rows or only one non-zero row but with more than one errors. In the former case, there will be at least two erroneous rows in \( Y_{i+z+l'} \) because \( S_{i+z+l',j} \neq 0 \Rightarrow [S_{i+z+l'-1,j}]_{1}^{w-1}, S_{i+z+l'} \] \( \neq 0 \). We denote the indices of these two erroneous rows by \( r'_c \) and \( r''_c \), respectively, and \( r''_c > r'_c > r_c \). By (59), we know that there are \( g(r'_c) - 1 \) erroneous rows above these two erroneous rows, and \( \max\{t_1 + 1 - g(r'_c), t_1 + 1 - g(r''_c)\} \) rows in \( Y_{i+z+l'+1}, \ldots, Y_{i+w-1} \) will be affected. In this case, the total number of affected rows in \( [Y_{\Sigma}, Y_{\Sigma}] \) will become \( t_1 + 2 \), which is contradictory to (62). In the latter case, it means that there will be at least two erroneous rows in \( Y_{i+z} \) because of the transformation of (2). Then, one will arrive at the conclusion that the total number of affected rows in \( [Y_{\Sigma}, Y_{\Sigma}] \) will become \( t_1 + 2 \), which cannot happen. Thus, (60) must hold.

Finally, by applying the arguments of (53), (58)-(60) to the erroneous row in \( Y_{i} \), we get
\[
\sum_{j=1}^{m} w_H(s_{i,l',j}) = 1, \forall l' \in L_1 \subseteq [w - 1] \cap (2N), |L_1| = t_1 + 1, \quad (61)
\Rightarrow \sum_{j=1}^{m} w_H(s_{i,l''},j) = 1, \forall l'' \in L_1' \subseteq [q], |L_1'| = t_1 + 1, \quad (62)
\]
where \( s_{i,l',j} \) and \( s_{i,l''},j \) denote the \( j \)-th rows of stall pattern matrices \( S_{i,l'} \) and \( S_{i,l''} \), respectively, and \( L_1 \) and \( L_1' \) are the corresponding sets of sub-block indices, respectively, with which the sub-block has one error. However, (61) requires that \( |w - 1| \cap (2N) | \geq t_1 + 1 \Rightarrow w - 1 \geq 2(t_1 + 1) \) while (62) requires that \( q \geq t_1 + 1 \), which are in contradiction with the conditions in Lemma 1. Hence, \( s_{\text{min}} \) is strictly larger than (52). The proof for the case of \( t_2 < t_1 \) follows similarly.

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