ABSTRACT In this work, we proposed a three-dimensional (3-D) channel stacked array architecture based on charge-trap flash (CTF) memory for an artificial neural network accelerator. The proposed synapse array architecture could be a promising solution for implementing efficiently a large-size artificial neural network on a limited-size hardware chip. We designed a full array architecture including a stacked layer selection circuit. In addition, we investigated the synaptic characteristics of CTF device by using technology computer-aided design (TCAD) simulation. We demonstrated the feasibility of the synapse array for neural network accelerators through a system-level MATLAB simulation with the Modified National Institute of Standards and Technology (MNIST) database.

INDEX TERMS 3-D stacked synapse array, neuromorphic system, artificial neural network, synapse array, synapse device, CTF memory.
TABLE 1. Comparison of basic properties of various synapse devices [11], [14], [35].

|                      | 2D RRAM | 2D PCM | 2D STT-RAM (NAND) | 3-D CTF (NAND) | 3-D CTF (NOR, this work) |
|----------------------|---------|--------|-------------------|----------------|--------------------------|
| Cell size            | 4-12 F^2| 4-12 F^2| 6-20 F^2         | 12 F^2        | 45 F^2                  |
| CMOS compatibility   | Good    | Good   | Moderate          | Very good     | Very good               |
| Multi-level operation with good retention | Good | Good | Moderate | Very good | Very good |
| Write power          | Low     | Low    | Low              | Mid           | High                    |
| Write latency        | 20 – 100 ns | 40 – 150 ns | 2 – 20 ns | > 1 μs | < 1 μs |
| Read latency         | < 10 ns  | 20 – 50 ns | 2 – 20 ns | < 10 ns | < 10 ns |
| Endurance            | 10^6 – 10^{11} cycles | < 10^{15} cycles | > 10^{12} cycles | < 10^{5} cycles | < 10^{5} cycles |
| VMM                  | Parallel | Parallel | Parallel | Sequential | Parallel |

memory [14], [15], [16], [17], [18], [19], [20], [32], [33], [34]. A specific comparison of synaptic memory devices is summarized in Table 1. CTF memory is a promising candidate for the synapse device because it has several advantages such as multi-level operation, good retention characteristic (> 10 years) [21], [22], [23], [24], and good compatibility with complementary metal-oxide-semiconductor (CMOS) process.

In this paper, channel-stacked 3-D synapse array based on CTF memory devices is proposed to implement high-density synapse array. Compared with our previous array based on the gate-stacked structure [14], the proposed array architecture has several advantages in terms of the unwanted interference between stacked layers and process cost. More details will be discussed in the next chapter.

We demonstrate the feasibility of CTF memory-based synapse array and neuromorphic system application through the results of device-level and system-level simulation. Both TCAD and MATLAB simulation tools are used to characterize the CTF memory device operation and pattern recognition application with MNIST database by implementing fully-connected single layer neural network. Also, fabrication process flow of the 3-D channel stacked synapse array with CTF memory devices is introduced.

II. 3-D CHANNEL-STACKED SYNAPSE ARRAY ARCHITECTURE

Fig. 1(a) illustrates an equivalent circuit diagram of the proposed 3-D channel-stacked synapse array architecture which is composed of synapse array and layer selection circuit. (b) Schematic diagram of synapse structure.

memory [14], [15], [16], [17], [18], [19], [20], [32], [33], [34]. A specific comparison of synaptic memory devices is summarized in Table 1. CTF memory is a promising candidate for the synapse device because it has several advantages such as multi-level operation, good retention characteristic (> 10 years) [21], [22], [23], [24], and good compatibility with complementary metal-oxide-semiconductor (CMOS) process.

In this paper, channel-stacked 3-D synapse array based on CTF memory devices is proposed to implement high-density synapse array. Compared with our previous array based on the gate-stacked structure [14], the proposed array architecture has several advantages in terms of the unwanted interference between stacked layers and process cost. More details will be discussed in the next chapter.

We demonstrate the feasibility of CTF memory-based synapse array and neuromorphic system application through the results of device-level and system-level simulation. Both TCAD and MATLAB simulation tools are used to characterize the CTF memory device operation and pattern recognition application with MNIST database by implementing fully-connected single layer neural network. Also, fabrication process flow of the 3-D channel stacked synapse array with CTF memory devices is introduced.

FIGURE 1. (a) Equivalent circuit diagram of the proposed 3-D channel-stacked synapse array architecture which is composed of synapse array and layer selection circuit. (b) Schematic diagram of synapse structure.

memory [14], [15], [16], [17], [18], [19], [20], [32], [33], [34]. A specific comparison of synaptic memory devices is summarized in Table 1. CTF memory is a promising candidate for the synapse device because it has several advantages such as multi-level operation, good retention characteristic (> 10 years) [21], [22], [23], [24], and good compatibility with complementary metal-oxide-semiconductor (CMOS) process.

In this paper, channel-stacked 3-D synapse array based on CTF memory devices is proposed to implement high-density synapse array. Compared with our previous array based on the gate-stacked structure [14], the proposed array architecture has several advantages in terms of the unwanted interference between stacked layers and process cost. More details will be discussed in the next chapter.

We demonstrate the feasibility of CTF memory-based synapse array and neuromorphic system application through the results of device-level and system-level simulation. Both TCAD and MATLAB simulation tools are used to characterize the CTF memory device operation and pattern recognition application with MNIST database by implementing fully-connected single layer neural network. Also, fabrication process flow of the 3-D channel stacked synapse array with CTF memory devices is introduced.

II. 3-D CHANNEL-STACKED SYNAPSE ARRAY ARCHITECTURE

Fig. 1(a) illustrates an equivalent circuit diagram of the proposed synapse array architecture. The proposed 3-D synapse array has a form in which conventional planar NOR flash memory arrays are vertically stacked. In order to selectively operate each stacked layer, the layer selection circuit is added. The detailed configuration and operation method will be discussed later. Fig. 1(b) represents a unit synapse structure where two CTF memory devices are connected in series. In each CTF device, respective conductance information ($G^+$ or $G^-$) is stored in a charge-storage node (silicon nitride...
The synaptic weight of each synapse is represented by the difference between two conductances: \( w = G^+ - G^- \). When an input voltage (\( x \)) is applied to the IL (input line), the drain currents of OL(+) and OL(-) flow into a neuron circuit. These drain currents are determined by \( x \cdot G^+ \) and \( x \cdot G^- \), respectively. In order to modulate the conductance of each CTF memory device, hot electron injection (HEI) and hot hole injection (HHI) can be used.

Fig. 2(a) shows a top view of the proposed full array architecture. The output of each neuron is defined as the difference between the output line currents [16]. The specific structure of the synapse array is depicted in Fig. 2(b). WLs and ILs are alternatively arranged in parallel at the top of the synapse array structure. OLs are configured for each stacked layer, and they are connected to the layer selection circuit as can be seen in Fig. 2(c). OL 1, 1(n(+)) of each synapse layer and OL 1(+) of neuron circuit are connected through layer selection transistor (LST). The gates of LSTs are connected by LSL (layer selection line). By selectively applying a turn-on voltage (\( V_{\text{PASS}} \)) to the LSLs, only the selected synaptic layer is connected to the neuron circuit. Specific operation bias schemes for the layer selection are shown in Table 2.

Note that the number of connected LSTs for one OL 1(+) (or OL 1(−)) of each neuron circuit is equal to the number of stacked layers. In addition, by arranging a plurality of LSTs in a direction parallel to each OL, the effective unit cell area (45 F\(^2\)) does not increase even if the number of stacked layers increase.

In our previous work [14], the gate-stacked type of 3-D synapse array architecture was proposed. In this work, unlike the previous one, the array architecture is based on the channel-stacked type. With respect to 3-D stacked array architecture design, unwanted electrical interference between stacked layer should be carefully considered. However, in the case of the gate-stacked type, the gate voltage drift of the unselected layer can be caused by the capacitive coupling between the stacked word lines (WLs). In the worst case, memory devices of the unselected layer may be turned on as the electrical potential of unselected WLs is boosted. To avoid this inherent risk, additional peripheral circuit part that applies voltages to the unselected layer is required [11] and this causes an increase in the area of the peripheral circuitry. On the other hand, in the case of the channel-stack type, only the current in the selected layer always flows to the neuron circuit by the layer selection circuit even if electrical coupling occurs between stacked channels. Therefore, there is no VMM calculation error or degradation of system accuracy due to unwanted interference between the stacked layers. In addition, the proposed synapse array architecture has the advantage of reducing process steps compared to the previous one. In the gate-stacked version of our previous work, two metal layers (source lines and drain lines) on top of the main synapse array are needed. On the contrary, the channel-stacked version only requires one metal layer (ILs and WLs are constructed within the same metal layer).
TABLE 3. Operation method for learning and inference process.

|        | Learning | Inference |
|--------|----------|-----------|
|        | HEI      | HHI       |
| $V_{WL}$ ($V$) | selected 6 V  -4 V | 3 V |
|         | unselected 0 V  0 V | 0 V  |
| $V_{OL}$ ($V$) | selected 5 V  4 V | 0 V  |
|         | unselected 0 V  0 V | 0 V  |
| $V_{IL}$ ($V$) | 0 V | 0 V (input ‘0’)  0.1 V (input ‘1’) |

Operation method of the proposed 3-D synapse array architecture is summarized in Table 3. HEI or HHI is used for the learning process. Synaptic weight of the synapse device can be modulated by changing conductance through hot carrier injection. The inference process can be done by applying $V_{WL,\text{inference}}$ and $V_{IL,\text{inference}}$ to WL and IL, respectively.

III. SIMULATION RESULTS

A. DEVICE MODELS AND MODEL PARAMETERS

Synopsys Sentaurus TCAD device simulation was used to demonstrate the synaptic operation of the proposed synaptic device. In order to describe basic transistor characteristics in TCAD device simulation, several models were used. Shockley-Read-Hall (SRH) recombination, band-to-band tunnelling (BTBT) models are used to describe recombination which occurs in channel. Spherical harmonics expansion (SHE) model, PhuMob, Enormal, and HighFieldSaturation models were used for mobility [36]. Specific parameters of charge-trapping layer such as trap concentrations, trap energy, and etc. are summarized in Table 4. Fiegna model [36] was used to calculate charge injection to charge-trapping layer through hot carrier injection during HEI or HHI [37]. The amount of injected charge of Fiegna model can be formulated as (1):

$$I_g = q A \frac{F^{3/2}}{3 \chi} \int P_{ins} \frac{F_{\text{eff}}^{3/2}}{e^{F_{\text{eff}}/E_B}} \xi \left( \frac{F_{\text{eff}}^{3/2}}{E_B} \right) \chi \left( \frac{3}{2} \right) ds$$

where $I_g$ is gate current, $\chi$ and $A$ are constant which determined by fitting experimental data, $P_{ins}$ is the probability of scattering in the image force potential well, $F_{\text{eff}}$ is the effective electric field, and $E_B$ is the semiconductor-insulator barrier height. We utilized default parameter values which provided by Sentaurus TCAD simulator for mobility models and recombination models. We modified fitting parameters of Fiegna model to adjust the HEI and HHI characteristics. The specific model parameters of Fiegna model are summarized in Table 5.

We verified our model used in the simulation by comparing simulated data and measured one from the reference CTF device [21]. As shown in Fig. 3, HEI and HHI speed of the simulated result approximately follows that of the measured one, validating our simulation models.

B. SYNAPTIC DEVICE CHARACTERISTICS

Basic structure of the device used in simulation is shown in Fig. 4. As summarized in Table 6, each CTF device has gate dielectric layers with 3 nm-thick silicon oxide (tunneling dielectric), 6 nm-thick silicon nitride (charge-trapping layer), 6 nm-thick silicon oxide (the 1st blocking dielectric), and an
TABLE 6. Physical parameters of the device used for TCAD simulation.

| Parameter | Value       |
|-----------|-------------|
| \(L_{\text{gate}}\) | 100 nm |
| \(T_{\text{channel}}\) | 30 nm |
| \(T_{\text{ON/OFF}}\) | 3/6/6 nm |
| \(T_{\text{X/Ox}}\) | 3 nm |

FIGURE 5. \(I - V\) characteristics of simulated single CTF memory devices.

Additional 3 nm-thick aluminium oxide (the 2nd blocking dielectric).

Fig. 5 shows the \(I - V\) characteristics of the TCAD simulated single CTF synaptic devices. The \(I - V\) curve is measured for each HEI pulse, which is applied to inject electrons into charge-trapping layer in total 64 times. Assuming that we define the threshold voltage as gate voltage when the current is 1 \(\mu\)A using the constant current method, the simulated device has shown 260 mV of threshold voltage, and \(~1.9\) V of memory window.

Fig. 6 shows a simulation result of HEI and HHI. The application of successive pulses makes a gradual change in conductance. The magnitude of pulse is listed in Table 3 and each pulse time is 50 ns for HEI and 100 ns for HHI. Dotted line shows an ideal linear behavior of a synapse device and circles are the simulation result. Both HEI and HHI showed nonlinear characteristics. Instead, interestingly, HEI showed more linear behavior than HHI. This can be interpreted as follows.

The most important factor determining the amount of HEI is the horizontal electric field in the channel region. Electrons locally trapped in the drain region by HEI do not have a significant effect on the horizontal electric field. As a consequence, even if the concentration of trapped electrons increases as HEI pulses are continuously applied, the amount of HEI per pulse does not change significantly. However, the most important factor determining the amount of HHI is the vertical electric field between the gate and the drain. Holes locally trapped in the drain region by HHI reduce the vertical electric field. Consequently, as HHI pulses are continuously applied and the concentration of trapped holes increases, the amount of HHI per pulse gradually decreases.

C. POTENTIATION AND DEPRESSION METHOD

The synaptic weight update by potentiation (increasing the synaptic weight) or depression (decreasing the synaptic weight) operation is the heart of learning process in a neuromorphic system. In this work, we tested two methods to perform potentiation or depression operation. The first method is a bidirectional update method in which both HEI and HHI are used for the conductance modulation. As can be seen the following equation, to increase \(w\), HHI pulses to the \(G^+\) CTF and HEI pulses to the \(G^-\) CTF are applied simultaneously. On the other hand, to decrease \(w\), HEI pulses to the \(G^+\) CTF and HHI pulses to the \(G^-\) CTF are applied simultaneously.

\[
\begin{align*}
\text{potentiation:} & \quad w(\uparrow) = G^+(\uparrow \text{ by HHI}) - G^-(\downarrow \text{ by HEI}) \\
\text{depression:} & \quad w(\downarrow) = G^+(\downarrow \text{ by HEI}) - G^-(\uparrow \text{ by HHI}) \quad (2)
\end{align*}
\]

Another method is a unidirectional update method in which only one injection mechanism (HEI or HHI) is used for the conductance modulation. As can be seen the following equation, to increase \(w\), HHI pulses to the \(G^+\) CTF and HEI pulses to the \(G^-\) CTF are applied simultaneously. On the other hand, to decrease \(w\), HEI pulses to the \(G^+\) CTF and HHI pulses to the \(G^-\) CTF are applied simultaneously.

\[
\begin{align*}
\text{potentiation:} & \quad w(\uparrow) = G^+(\text{fixed}) - G^-(\downarrow \text{ by HEI}) \\
\text{depression:} & \quad w(\downarrow) = G^+(\downarrow \text{ by HEI}) - G^-(\uparrow \text{ by HHI}) \quad (3)
\end{align*}
\]

In a unidirectional update method by using HEI, HEI pulses are applied to the \(G^-\) CTF and \(G^+\) CTF for potentiation and depression, respectively. At this time, no pulse is applied to the OL of the other CTF device. In addition, the \(G^+\) CTF during potentiation and the \(G^-\) CTF during depression.

A unidirectional update method by using HHI is described in (4).

\[
\begin{align*}
\text{potentiation:} & \quad w(\uparrow) = G^+(\uparrow \text{ by HHI}) - G^-(\text{fixed}) \\
\text{depression:} & \quad w(\downarrow) = G^+(\text{fixed}) - G^-(\uparrow \text{ by HHI}) \quad (4)
\end{align*}
\]
D. MNIST PATTERN RECOGNITION SIMULATION

System-level simulation of MNIST pattern recognition was performed to demonstrate the feasibility of the proposed synapse array for neuromorphic applications.

Binary MNIST image set is composed of 10 hand-written numbers (‘0’ to ‘9’) which are made with 784 (= 28 × 28) pixels and each pixel has the value of ‘1’ or ‘0’. This image set is made of 60000 training images and 10000 test images. MNIST pattern recognition was performed using a single-layer artificial neural network with 784 input neurons and 10 output neurons.

There are two types of learning method in the neuromorphic systems. First, off-chip learning method implement learning outside a neuromorphic chip. After external learning is completed in software, the conductance of a synapse device is adjusted to a target level through an iterative program-verify scheme. Second, on-chip learning method perform learning in a neuromorphic chip. The program (potentiation or depression) pulses are applied to each synapse device. At this time, the number of pulses to be applied is determined by the output current of the corresponding neuron circuit. In this work, we conducted on-chip learning simulation. We assumed that the neuron circuit performs a softmax activation function and a program pulse is applied for every input image according to a conventional stochastic gradient decent algorithm.

Fig. 7 shows the simulation result of recognition accuracy as a function of the number of trained samples. Accuracy baseline (88.18 %) is a simulation result of an ideal CTF memory in Fig. 7 as a reference. Unidirectional update methods exhibit better accuracy than bidirectional update methods. In particular, the unidirectional update method by using HEI with better linearity showed slightly better recognition accuracy than the unidirectional update method by using HHI.

However, if we use bidirectional update methods, the accuracy is stuck at around 50% level even with the more training. In a unidirectional update method, only HEI or HHI occurs in one CTF device. On the other hand, in a bidirectional update method, both HEI pulse and HHI pulse can be applied to one CTF device during learning process. If HHI pulses are applied in the conductance range 15∼60 μS, abrupt conductance change occurs as can be seen in Fig. 6, which means that sophisticated weight modulation of the learning process fails. Therefore, a bidirectional update method has very low learning accuracy compared with a unidirectional update method.

In addition to nonlinearity of conductance tuning, synaptic weight precision (the number of multi-level conductance states) has a great influence on the accuracy performance of neuromorphic systems [25]. The multi-level conductance states as a function of number of HEI pulses are depicted in Fig. 8. Fig. 9 shows the best recognition results for various the number of multi-level conductance states when a unidirectional update method with HEI is adopted.
IV. FABRICATION METHOD

Fabrication process flow of 3-D channel-stacked synapse array based on CTF memory device is represented in Fig. 8. Here, we assumed that there are four layers in the stack, but it is possible to expand the number of stacked layers. When the number of stacks increases by one layer, one row of LST in layer selection circuit in Fig. 2(a) is added. Note that even if the number of stacks increase, the area of synapse array region does not increase. The specific method of each step is summarized as follows.

Fig. 10(a): At first, multi-layer stacked alternately with silicon oxide and polysilicon is formed on a silicon substrate followed by deposition of Si$_3$N$_4$. Polysilicon will be used as a channel of CTF memory devices. The top Si$_3$N$_4$ layer will be used as a hard mask for etching and a CMP (chemical-mechanical polishing) stopper.

Fig. 10(b): After the multi-layer stacks are formed, patterning by photolithography and dry etching process is carried out. Then, gate dielectric materials are deposited.

Fig. 10(c): N$^+$-doped poly-Si deposition and CMP process are performed.

Fig. 10(d): Gate photolithography and poly-Si etching are carried out to form the gate formation. Then, n-type ion implantation is carried out for the formation of source and drain regions.

Fig. 10(e): Oxide deposition and planarization process are carried out to make the inter-layer dielectric (ILD).

Fig. 10(f): Photolithography and etching process is carried out for the formation of OL trench region and IL contact hole region. Then, selective wet etching of poly-Si is carried out. The region where poly-Si is removed will be filled with tungsten in the next contact process.

Fig. 10(g): The gate contact holes are formed through photolithography and etching processes.

Fig. 10(h): Tungsten deposition and removal of unwanted region are carried out for the contact process. The contact of WLs, ILs, and OLs are formed simultaneously.

Fig. 10(i): Oxide deposition is carried out.

Fig. 10(j): Stair-like OL structure is made for the connection with the layer selection circuits as shown in Fig. 2(c).

Fig. 10(k): Metal interconnection process for OLs is carried out.

Fig. 10(l): Finally, metal interconnection of WLs and ILs are formed.

V. CONCLUSION

In this paper, we have proposed a 3-D channel-stacked synapse array architecture. The synapse device is composed of a pair of CTF memory devices which have good CMOS compatibility and excellent reliability. The synapse device characteristic was demonstrated using a TCAD device simulation. In addition, we investigated the conductance update method through a MNIST pattern recognition simulation. Compared with our previous array based on the gate-stacked structure, the proposed array architecture has the advantage of preventing abnormal operation due to unwanted interference between stacked layers. The proposed 3-D channel-stacked synapse array architecture will be the promising technology for high-density neuromorphic systems.
ACKNOWLEDGMENT
The EDA tool was supported by the IC Design Education Center (IDEC), South Korea.

REFERENCES
[1] D. Kwon et al., “On-chip training spiking neural networks using approximated backpropagation with analog synaptic devices,” Front. Neurosci., vol. 14, p. 423, Jul. 2020, doi: 10.3389/fnins.2020.00423.
[2] B. Rajendran and F. Alibart, “Neuromorphic computing based on emerging memory technologies,” IEEE J. Emerg. Sel. Topics Circuits Syst., vol. 6, no. 2, pp. 198–211, Jun. 2016, doi: 10.1109/JETCAS.2016.2533298.
[3] C. Mead, “Neuromorphic electronic systems,” Proc. IEEE, vol. 78, no. 10, pp. 1629–1636, Oct. 1990, doi: 10.1109/5.88356.
[4] H.-S. Choi et al., “3-D floating-gate synapse array with spike-time-dependent plasticity,” IEEE Trans. Electron Devices, vol. 65, no. 1, pp. 101–107, Jan. 2018, doi: 10.1109/TED.2017.2775233.
[5] G. W. Burr et al., “Neuromorphic computing using non-volatile memory,” Adv. Phys., vol. 2, no. 1, pp. 89–124, 2017, doi: 10.1080/23746149.2016.1259585.
[6] D. Ielmini and S. Ambrogio, “Emerging neuromorphic devices,” Nanotechnology, vol. 31, no. 9, Dec. 2019, Art. no. 92001, doi: 10.1088/1361-6528/aab54b.
[7] S.-T. Lee et al., “Neuromorphic technology based on charge storage memory devices,” in Proc. IEEE Symp. VLSI Technol., Jun. 2018, pp. 169–170, doi: 10.1109/VLSIT.2018.8510667.
[8] S. Oh et al., “Unsupervised online learning of temporal information in spiking neural network using thin-film transistor-type NOR flash memory devices,” Nanotechnology, vol. 30, no. 43, Aug. 2019, Art. no. 435206, doi: 10.1088/1361-6528/aba3da.
[9] J. Park, M.-W. Kwon, H. Kim, S. Hwang, J.-J. Lee, and B.-G. Park, “Compact neuromorphic system with four-terminal Si-based synaptic devices for spiking neural networks,” IEEE Trans. Electron Devices, vol. 64, no. 5, pp. 2438–2444, May 2017, doi: 10.1109/TED.2017.2685519.
[10] B. Rajendran et al., “Specifications of nanoscale devices and circuits for neuromorphic computational systems.” IEEE Trans. Electron Devices, vol. 60, no. 1, pp. 246–253, Jan. 2013, doi: 10.1109/TED.2012.2227969.
[11] H.-S. Choi, Y. J. Park, J.-H. Lee, and Y. Kim, “3-D synapse array architecture based on charge-trap flash memory for neuromorphic application,” Electronics, vol. 9, no. 1, p. 57, 2020, doi: 10.3390/electronic09010057.
[12] H. Kim, S. Hwang, J. Park, and B.-G. Park, “Silicon synaptic transistor for hardware-based spiking neural network and neuromorphic device,” Nanotechnology, vol. 28, no. 40, Sep. 2017, Art. no. 405202, doi: 10.1088/1361-6528/aa8608.
[13] P. Narayanan et al., “Toward on-chip acceleration of the backpropagation algorithm using nonvolatile memory,” IBM J. Res. Dev., vol. 61, nos. 4–5, pp. 11:1–11:11, Jul.–Sep. 2017, doi: 10.1147/IRRD.2017.2716579.
[14] J. Y. Park et al., “3-D stacked synapse array based on charge-trap flash memory for implementation of deep neural networks,” IEEE Trans. Electron Devices, vol. 66, no. 1, pp. 420–427, Jan. 2019, doi: 10.1109/TED.2018.2881972.
[15] F. Akopyan et al., “TrueNorth: Design and tool flow of a 65 mW 1 million neuron programmable neurosynaptic chip,” IEEE Trans. Comput.-Aided Design Integ. Circuits Syst., vol. 34, no. 10, pp. 1537–1557, Oct. 2015, doi: 10.1109/TCAD.2015.2474396.
[16] S. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, and H.-S. P. Wong, “An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation,” IEEE Trans. Electron Devices, vol. 58, no. 8, pp. 2729–2737, Aug. 2011, doi: 10.1109/TED.2011.2147791.
[17] A. F. Vincent et al., “Spin-transfer torque magnetic memory as a stochastic neuromorphic synapse for neuromorphic systems,” IEEE Trans. Biomed. Circuits Syst., vol. 9, no. 2, pp. 166–174, Apr. 2015, doi: 10.1109/TBCAS.2015.2414423.
[18] N. Panwar, D. Kumar, N. K. Upadhyay, P. Arya, U. Ganguly, and B. Rajendran, “Memristive synaptic plasticity in Pr6Tc7Ca0.3Mn0.7O3 RRAM by bio-mimetic programming,” in Proc. 72nd Device Res. Conf., Jun. 2014, pp. 135–136, doi: 10.1109/DRC.2014.6872334.