Chaotic Amplitude Control for Neuromorphic Ising Machine in Silico

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Ising machines are special-purpose hardware designed to reduce time, resources, and energy consumption needed for finding low energy states of the Ising Hamiltonian. In recent years, most of the physical implementations of such machines have been based on a similar concept that is closely related to annealing such as in simulated, mean-field, chaotic, and quantum annealing. We argue that Ising machines benefit from implementing a chaotic amplitude control of mean field dynamics that does not rely solely on annealing for escaping local minima trap. We show that this scheme outperforms recent state-of-the-art solvers for some reference benchmarks quantitatively and qualitatively in terms of time to solution, energy efficiency, and scaling of its variance with problem size when it is implemented in hardware such as in a field programmable gate array that is organized according to a neuromorphic design where memory is distributed with processing.
One Sentence Summary (150 characters): The performance of Ising machines can be increased quantitatively and qualitatively by controlling the amplitude of the mean field dynamics especially when implemented on a neuromorphic hardware in silico.

1 Introduction

Many complex systems such as spin glasses, interacting proteins, large scale hardware, and financial portfolios, can be described as ensembles of disordered elements that have competing and frustrated interactions (1). There has been a growing interest in using physical simulators called “Ising machines” in order to reduce time and resources needed to identify configurations that minimize their total interaction energy, notably that of the Ising Hamiltonians $\mathcal{H}$ with $\mathcal{H}(\sigma) = -\frac{1}{2} \sum_{ij} \omega_{ij} \sigma_i \sigma_j$ (with $\omega_{ij}$ the symmetric Ising couplings, i.e., $\omega_{ij} = \omega_{ji}$, and $\sigma_i = \pm 1$) that is related to many NP-hard combinatorial optimization problems and various real-world applications (2). Recently proposed implementations include memresistor networks (3), micro- or nano-electromechanical systems (4), micro-magnets (5, 6), coherent optical systems (7), hybrid opto-electronic hardware (8–10), integrated photonics (11–13), flux qubits (14), and Bose-Einstein condensates (15). In principle, these physical systems often possess unique properties, such as coherent superposition in flux qubits (16) and energy efficiency of memresistors (3, 17), which could lead to a distinctive advantage compared to conventional computers (see Fig.1(a)) for solving hard combinatorial optimization problems. In practice, the difficulty in constructing connections between constituting elements of the hardware is often the main limiting factor to scalability and performance for these systems (14, 18). Moreover, these devices often implement schemes that are directly related to the concept of annealing (either simulated (19, 20), mean-field (21, 22), chaotic (17, 23), and quantum (16, 24)) in which the escape from the numerous local minima (25) and saddle points (26) of the free energy function can only be achieved under very slow modulation of the control parameter (see Fig.1(b)).

Interestingly, alternative dynamics that does not depend on the concept of annealing may perform better for solving hard combinatorial optimization problems (27–29). Various kinds of dynamics have been proposed (30–34), notably chaotic dynamics (17, 35–38), but have either
not been implemented onto specialized hardware (35, 39) or use chaotic dynamics merely as a replacement to random fluctuations (17, 36). We have recently proposed that the control of amplitude in mean-field dynamics can significantly improve the performance of Ising machines by introducing error correction terms (see Fig. 1 (d)), effectively doubling the dimensionality of the system, whose role is to correct the amplitude heterogeneity (27). Because of the similarity of such dynamics with that of a neural network, it can be implemented especially efficiently in electronic neuromorphic hardware where memory is distributed with the processing (40–42). In this paper, we implement a version of this scheme that we name chaotic amplitude control (CAC) on a field programmable gate array (FPGA, see Fig. 1 (c)) as a paradigmatic example and show that the developed hardware outperforms state-of-the-art Ising problem solvers for some reference benchmarks quantitatively and qualitatively in terms of time to solution, energy efficiency, and scaling of its variance with problem size.

2 Results

For the sake of simplicity, we consider the classical limit of Ising machines for which the state space is often naturally described by analog variables (i.e., real numbers) noted \( x_i \) in the following. The variables \( x_i \) represent measured physical quantities such as voltage (3) or optical field amplitude (7–12) and these systems can often be simplified to networks of interacting nonlinear elements whose time evolution can be written as follows:

\[
\frac{dx_i}{dt} = f_i(x_i) + \beta_i(t) \sum_j \omega_{ij} g_j(x_j) + \sigma_0 \eta_i, \quad \forall i \in \{1, \ldots, N\},
\]

(1)

where \( f_i \) and \( g_i \) represent the nonlinear gain and interaction, respectively, and are assumed to be monotonic, odd, and invertible “sigmoidal” functions for the sake of simplicity; \( \eta_i \), experimental white noise of standard deviation \( \sigma_0 \) with \( \langle \eta_i(t) \eta_j(t') \rangle = \delta_{ij} \delta(t - t') \) and \( N \), the number of spins. Ordinary differential equations similar to eq. (1) have been used in various computational models that are applied to nondeterministic polynomial-hard (NP-hard) combinatorial optimization problems such as Hopfield-Tank neural networks (43), coherent Ising machines (44), and

\[\delta_{ij}; \quad \delta(t)\] the Kronecker delta symbol and Dirac delta function, respectively.
correspond to the “soft” spin description of frustrated spin systems (45). Moreover, the steady states of eq. (1) correspond to the solutions of the “naive” Thouless-Anderson-Palmer (nTAP) equations that arise from the mean-field description of Sherrington-Kirkpatrick spin glasses when the Onsager reaction term has been discarded (46). In the case of neural networks in particular, the variables \( x_i \) and constant parameters \( \omega_{ij} \) correspond to firing rates of neurons and synaptic coupling weights, respectively.

It is well known that, when \( \beta_i = \beta \) for all \( i \) and the noise is not taken into account (\( \sigma_0 = 0 \)), the time evolution of this system is motion in the state space that seeks out minima of a potential function (47) (or Lyapunov function) \( V \) given as \( V = \beta \mathcal{H}(y) + \sum_i V_b(y_i) \) where \( V_b \) is a bistable potential with \( V_b(y_i) = -\int_0^{y_i} f_i(y) \, dy \) and \( \mathcal{H}(y) = -\frac{1}{2} \sum_{ij} \omega_{ij} y_i y_j \) is the extension of the Ising Hamiltonian in the real space with \( y_i = g_i(x_i) \) (see supplementary material A.1). The bifurcation parameter \( \beta \), which can be interpreted as the inverse temperature of the naive TAP equations (46), the steepness of the neuronal transfer function in Hopfield-Tank neural networks (43), or to the coupling strength in coherent Ising machines (7–9), is usually decreased gradually in order to improve the quality of solutions found. This procedure has been called mean-field annealing (22), and can be interpreted as a quasi-static deformation of the potential function \( V \) (see Fig. 1(b)). There is, however, no guarantee that a sufficiently slow deformation of the landscape \( V \) will ensure convergence to the lowest energy state contrarily to the quantum adiabatic theorem (48) or the convergence theorem of simulated annealing (49). Moreover, the statistical analysis of spin glasses suggests that the potential \( V \) is highly non-convex at low temperature and that simple gradient descent of the potential \( V \) very unlikely reaches the global minimum of \( \mathcal{H}(\sigma) \) because of the presence of exponentially numerous local minima (25) and saddle points (26) as the size of the system increases. The slow relaxation time of Monte-Carlo simulations, such as simulated annealing, might also be explained in the case of spin glasses by similar trapping dynamics during the descent of the free energy landscape obtained from the TAP equations (26). In the following, we consider in particular the soft spin description obtained by taking \( f_i(x_i) = (-1 + p) x_i - x_i^3 \) and \( y_i = g_i(x_i) = x_i \), where \( p \) is the gain

\[ \sigma_0(t)^2 \sim \frac{c}{\log(t+c)} \]

At fixed \( \beta \), global convergence to the minimum of the potential \( V \) can be assured if \( \sigma_0 \) is gradually decrease with \( \sigma_0(t)^2 \sim \frac{c}{\log(t+c)} \) and \( c \) sufficiently large (50). The parameter \( \sigma_0^2 \) is analogous to the temperature in simulated annealing in this case. The global minimum of the potential \( V \) does not, however, generally correspond to that of the Ising Hamiltonians \( \mathcal{H} \) at finite \( \beta \).
parameter, which is the canonical model of the system described in eq. (1) at proximity of a pitchfork bifurcation with respect to the parameter $p$. In this case, the potential function $V_b$ is given as $V_b(x_i) = (-1 + p)\frac{x_i^2}{2} - \frac{x_i^4}{4}$ and eq. (1) can be written as $\frac{dx_i}{dt} = -\frac{\partial V}{\partial x_i}, \forall i$.

The proposed amplitude control of mean-field dynamics consists in introducing error signals, noted $e_i \in \mathbb{R}$, that modulate the strength of coupling $\beta_i$ to the $i$th nonlinear element such that $\beta_i(t)$ defined in eq. (1) is expressed as $\beta_i(t) = \beta e_i(t)$ with $\beta > 0$. The time evolution of the error signals $e_i$ are given as follows (27):

$$\frac{de_i}{dt} = -\xi(g(x_i)^2 - a)e_i \tag{2}$$

where $a$ and $\xi$ are the target amplitude and the rate of change of error variables, respectively, with $a > 0$ and $\xi > 0$. If the system settles to a steady state, the values $y_i^* = g(x_i^*)$ become exactly binary with $y_i^* = \pm\sqrt{a}$. When $p < 1$, the internal fields $h_i$ at the steady state, defined as $h_i = \sum_j \omega_{ij} \sigma_j$ with $\sigma_j = y_j^*/|y_j^*|$, are such that $h_i \sigma_i > 0, \forall i$ (27). Thus, each equilibrium point of the analog system corresponds to that of a zero-temperature local minimum of the binary spin system.

The dynamics described by the coupled equations (1) and (2) is not derived from a potential function and the computational principle is not related to a gradient descent. Rather, the addition of error variables results in additional dimensions in the phase space via which the dynamics can escape local minima. The mechanism of this escape can be summarized as follows. It can be shown (see the supplementary material A.2) that the dimension of the unstable manifold at equilibrium points corresponding to local minima $\sigma$ of the Ising Hamiltonian depends on the number of eigenvalues $\mu(\sigma)$ with $\mu(\sigma) > F(a)$ where $\mu(\sigma)$ are the eigenvalues of the matrix $\{\frac{\omega_{ij}}{|h_i|}\}_{ij}$ (with internal field $h_i$) and $F$ a function given as $F(y) = \frac{\psi'(y)}{\psi(y)} y$ and $\psi(y) = f(y^{-1}(y))$. Thus, there exists a value of $a$ such that all local minima (including the ground state) are unstable and for which the system exhibits chaotic dynamics that explores successively candidate boolean configurations. The energy is evaluated at each step and the best configuration visited is kept as the solution of a run. Interestingly, this chaotic search is particularly efficient for sampling configurations of the Ising Hamiltonian close to that of the ground state using a single run although the distribution of sampled states is not necessarily given by the Boltzmann distribution. Note that the use of chaotic dynamics for solving Ising problems has been dis-
cussed previously (17, 51), notably in the context of neural networks, and it has been argued that chaotic fluctuations may possess better properties than Brownian noise for escaping from local minima traps. In the case of the proposed scheme, the chaotic dynamics is not merely used as a replacement to noise. Rather, the interaction between nonlinear gain and error-correction results in the destabilization of states associated with lower Ising Hamiltonian.

The target amplitude $a$ for which all local minima is unstable is not known a priori. Therefore, we propose instead to destabilize the local minima traps by dynamically modulating the target amplitude $a$ as a function of the visited configuration $\sigma$ using the heuristic function given as follows:

$$a(t) = \alpha - \rho \tanh(\delta \Delta \mathcal{H}(t)),$$

where $\Delta \mathcal{H}(t) = \mathcal{H}_{\text{opt}} - \mathcal{H}(t)$; $\mathcal{H}(t)$, the Ising Hamiltonian of the configuration visited at time $t$; and $\mathcal{H}_{\text{opt}}$, a given target energy. In practice, we set $\mathcal{H}_{\text{opt}}$ to the lowest energy visited during the current run, i.e., $\mathcal{H}_{\text{opt}}(t) = \min_{t' \leq t} \mathcal{H}(t')$. The function $\tanh$ is the tangent hyperbolic. $\rho$ and $\delta$ are positive real constants. In this way, configurations that have much larger Ising energy than the lowest energy visited are destabilized more strongly due to smaller target amplitude $a$.

Lastly, the parameter $\xi$ (see eq. (2)) is modulated as follows: $rac{d\xi}{dt} = \gamma$ when $t - t_r < \Delta t$, where $t_r$ is the last time for which either the best known energy $\mathcal{H}_{\text{opt}}$ was updated or $\xi$ was reset. Otherwise, $\xi$ is reset to 0 if $t - t_r \geq \Delta t$ and $t_r$ is set to $\bar{t}$.

In order to verify that chaotic amplitude control is able to accelerate the search of mean-field dynamics for finding the ground state of typical frustrated systems, we solve Sherrington-Kirkpatrick (SK) spin glass problems using the numerical simulation of eqs. (1) to (3) and two recently proposed implementation of the mean-field annealing method: noisy mean-field annealing (NMFA) (21) and the simulation of the coherent Ising machine (simCIM). Because the arithmetic complexity of calculating one step of these three schemes are dominated by the

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3The modulation described in eq. (3) is better suited for a digital implementation on FPGA than the one proposed in (27). Numerical simulations shown in this paper suggest that this modulation results in destabilization of non-trivial attractors (periodic, chaotic, etc.) for typical problem instances.

4See supplementary material E.1 and 2
Figure 1: Schematic representation of (a) conventional CPU architecture with the von Neumann bottleneck problem and (c) the proposed neuromorphic chip for combinatorial optimization. Schema of state-space dynamics of algorithms based on (b) annealing on a potential function and (d) the proposed chaotic amplitude control scheme.

Matrix-vector multiplication (MVM), it is sufficient for the sake of comparison to count the number of MVM, noted $\nu$, to find the ground state energy of a given instance with 99% success probability, with $\nu(K) = K \ln(\frac{1}{1 - 0.99})$ and $p_0(K)$ the probability of visiting a ground state configuration at least once after a number $K$ of MVMs in a single run. In Fig. 2, NMFA (a) and the CAC (b) are compared using the averaged success probability $\langle p_0 \rangle$ of finding the ground state for 100 randomly generated SK spin glass instances per problem size $N$. Note that the success probability of the mean-field annealing method does not seem to converge to 1 even for large annealing time (see Fig. 2 (a)). Because the success probability of NMFA and simCIM remains low at larger problem size, its correct estimation requires simulating a larger number
of runs which we achieved by implementing these methods using a GPU. On the other hand, the average success probability $\langle p_0 \rangle$ of CAC is of order 1 when the maximal number of MVM is large enough, suggesting that the system rarely gets trapped in local minima of the Ising Hamiltonian or non-trivial attractors. In Figure 2(c) and (d) are shown the $q^{th}$ percentile (with $q = 50$, i.e., the median) of the MVM to solution distribution, noted $\nu_q(K; N)$, for various duration of simulation $K$, where $K$ is the number of MVMs of a single run. The minimum of these curves, noted $\nu^{*}_q(N)$ with $\nu^{*}_q(N) = \min_K \nu_q(K; N)$, represents the optimal scaling of MVM to solution vs. problem size $N$ (14). For large $N$, the median MVM to solution $\nu^{*}_{50}(N)$ is better fitted by an exponential scaling with the square root problem size $N$, that is $\nu^{*}_{50}(N) \sim e^{\gamma \sqrt{N}}$ (see Fig. 2(e), p-value: $4.3 \times 10^{-5}$, R-value: 0.95), than an exponential scaling with $N$ (p-value: $1.1 \times 10^{-4}$, R-value: 0.91) although there are not enough data points to reject either of the two hypotheses. Using the former hypothesis, CAC exhibits significantly smaller scaling exponent ($\gamma = 0.26 \pm 0.03$) than the NMFA ($\gamma = 0.47 \pm 0.04$) and simCIM ($\gamma = 0.54 \pm 0.03$, see inset in Fig. 2(e)). We have verified that this scaling advantage holds for various parameters of the mean-field annealing (see supplementary material E.1).

Although comparison of algebraic complexity indicates that CAC has a scaling advantage over mean-field annealing, it is in practice necessary to compare its physical implementation against other state-of-the-art methods because the performance of hardware depends on other factors such as memory access and information propagation delays. To this end, CAC is implemented into a FPGA because its similarity with neural networks makes it well-fitted for a design where memory is distributed with processing (see supplementary material B for the details of the FPGA implementation). The organization of the electronic circuit can be understood using the following analogy. Pairs of analog values $x_i$ and $e_i$, which represent averaged activity of two types of neurons, are encoded within neighboring circuits. This micro-structure is repeated $N$ times on the whole surface of the chip which resembles the columnar organization of the brain. The nonlinear processes $f_i(x_i)$, which model the local-population activation functions and are independent for $i \neq j$, are calculated in parallel. The coupling between elements $i$ and $j \in \{1, \ldots, N\}$ that is achieved by the dot product in eq. (1) is implemented by circuits that are at the periphery of the chip and are organized in a summation tree reminiscent of dendritic branching (see Fig. 1(c)).
Figure 2: (a,b) Average success probability $\langle p_0 \rangle$ of finding the ground state configuration of 100 Sherrington-Kirkpatrick spin glass instances and (c,d) 50th percentile of the MVM to solution distribution $\nu_{50}$ vs. problem size $N$. (a,c) NMFA. (b,d) CAC. (e) Number of matrix-vector multiplication MVM to solution distribution. Lower, higher, and upper whisker of boxes show the 50th, 80th, and 90th percentiles of the distribution. The upper right inset shows the exponential scaling factor $\gamma$ of the 50th percentile with $\nu_{50} \sim e^{\gamma \sqrt{N}}$ for CAC, NMFA, and simCIM.

We compare the FPGA implementation of CAC against state-of-the-art methods implemented on various types of hardware: the single-core CPU implementation of break-out local search (52) (BLS) that has been used to find most of the best known maximum-cuts (equivalently, Ising energies) from the GSET benchmark set (53), a well-optimized single-core CPU implementation of parallel tempering (or random replica exchange Monte-Carlo Markov chain sampling) (54, 55) (PT, courtesy of S. Mandra), simulated annealing (SA) (56), and Toshiba’s bifurcation machine on GPU (TBM) (57). Figure 3(a) shows that the CAC on FPGA has the smallest real time to solution $\tau_q^*$ against the other Ising machines and state-of-the-art algorithms despite just 5W power-consumption where $\tau_q^*(N)$ is the optimal $q$th percentile of time to solution with 99% success probability and is given as $\tau_q^*(N) = \min_T \tau_q(T; N)$ where $\tau(T)$ of a given instance is $\tau(T) = T \frac{\ln(1-0.99)}{\ln(1-p_0(T))}$ and $T$ is the duration in seconds of a run. Predictions of time to solution obtained when increasing the clock frequencies of the FPGA are also
shown in dashed lines. Using 20W of power consumption, CAC on FPGA implementation has smaller time to solution than recently proposed on-chip implementation of simulated annealing called Digital Annealer (see results in (19)). Note that the power consumption of transistors in the FPGA scales proportionally to its clock frequencies. In order to compare different Ising machines despite the heterogeneity in their power consumption, the \( q \)th percentile of energy-to-solution \( E_q^* \), i.e., the energy \( E_q^* \) required to solve SK instances with \( E_q^* = P \tau_q^* \) and \( P \) the power consumption\(^5\) is plotted in Fig. 3(b). CAC on FPGA is \( 10^2 \) to \( 10^3 \) times more energy efficient than state-of-the-art algorithms running on classical computers. Moreover, the relatively slow increase of time to solution with respect to the number of spins \( N \) when solving larger SK problems using CAC suggests that our FPGA implementation is faster than the Hopfield neural network implemented using memresistors (mem-HNN) (3) and the restricted Boltzmann machine using a FPGA (FPGA-RBM) (58) for \( N \gtrsim 1000 \) (see Tab. 1 and supplementary material C).

| Ising machine    | \( N = 100 \)  | \( N = 700 \)  | \( N = 2000 \) |
|------------------|----------------|----------------|----------------|
|                  | experimental  | \( e^{\gamma N} \) fit | \( e^{\gamma \sqrt{N}} \) fit | \( e^{\gamma N} \) fit | \( e^{\gamma \sqrt{N}} \) fit |
| NTT CIM (9)      | \( 6 \times 10^{-2} \) | \( 6 \times 10^6 \) | \( 8 \times 10^2 \) | \( > 10^5 \) | \( > 10^5 \) |
| mem-HNN (59)     | \( 10^{-4} \) | \( 2 \times 10^3 \) | \( 10^{-1} \) | \( > 10^5 \) | \( 4 \times 10^2 \) |
| FPGA-RBM (58)    | \( 3 \times 10^{-5} \) | \( 2 \times 10^{-1} \) | \( > 10^5 \) | \( 3 \times 10^3 \) |
| 5 W FPGA-CAC     | \( 2 \times 10^{-3} \) | \( 5 \times 10^{-1} \) | \( 6 \times 10^4 \) | \( 2 \times 10^2 \) |

Table 1: Median time to solution in seconds and extrapolations for the NTT CIM (not parallelized) (9), mem-HNN (59), FPGA-RBM (58), and FPGA-CAC (this work). Extrapolations are based on the hypotheses of scaling in \( e^{\gamma N} \) and \( e^{\gamma \sqrt{N}} \) by fitting the available experimental data for each Ising machine (see supplementary material C).

We next consider the whole distribution of time to solution in order to compare the ability of various methods to solve harder instances. As shown in Fig. 4(a), the cumulative distribution function (CDF) \( P(\tau; T) \) of time to solution with 99% success probability \( \tau \) is not uniquely defined as it depends on the duration \( T \) of the runs. We can define an optimal CDF \( P^*(\tau) \) that is independent of the runtime \( T \) as follows: \( P^*(\tau) = \max_T P(\tau; T) \). Numerical simulations

\[^5\]For the sake of simplicity, we assume a 20 and 120 watts power consumptions for the CPU and GPU. These numbers represent typical orders to magnitude for contemporary digital systems.
Figure 3: (a) Lower, higher, and upper whisker of boxes show the 50th, 80th, and 90th percentiles of the real time to solution distribution in seconds for the FPGA implementation of CAC with a maximum of 5W power consumption, CAC, SA, and PT algorithm running on a CPU (20W) and TBM on a GPU (120W). The dashed and dotted red lines show the predictions of the real time to solution in the case of a 10W and 20W FPGA implementation, respectively. (b) The same as (a) for the energy-to-solution $E^*$. 

show that this optimal CDF is well described by lognormal distribution, that is $P^*(\log(\tau)) \sim \mathcal{N}(\mu, \sqrt{\nu})$ where $\sqrt{\nu}$ is the standard deviation of $\log(\tau)$ (see Figs. 4 (b), (c), and (d) for the cases of CAC, SA, and NMFA, respectively). In Fig. 4 (e), it is shown that the scaling of the standard deviation $\sqrt{\nu}(N)$ with the problem size $N$ is significantly smaller for CAC, which implies that harder instances can be solved relatively more rapidly than using other methods. This result confirms the advantageous scaling of higher percentiles for CAC that was observed in Figs. 2 and 3.

3 Conclusions

In order to test that hard instances of other types than SK can be solved by our FPGA implementation, we have benchmarked it against BLS on the GSET (53) (see supplementary material D): most of the best known solutions were found approximately a hundred times faster than the BLS algorithm (52) using less than 5W of power consumption although the current implementation
does not take advantage of the sparsity of GSET instances for reducing energy consumption. For some instances (14th and 15th of size $N = 2000$ from GSET), we have found solutions of better quality than previously known in (52) and (27). The framework described in this paper can be extended to solve other types of constrained combinatorial optimization problems such as the traveling salesman (43), vehicle routing, and lead optimization problems. Moreover, it can be easily adapted to a variety of recently proposed Ising machines (3–12, 14) which would benefit from implementing a scheme that does not rely solely on the descent of a potential function. In particular, the performance of CIM (8, 9), mem-HNN (3), and chip-scale photonic Ising machine (13), which have small time to solution for problem sizes $N \approx 100$ but with a relatively large scaling exponent that limit their scalability, could be significantly improved by adapting the implementation we propose if these hardware can be shown to be able to support larger problem sizes experimentally.

4 Methods

We target the implementation of a low-power system with maximum power supply of 5W using a XCKU040 Kintex Ultrascale Xilinx FPGA integrated on an Avnet board. The implemented circuit can process Ising problems of more than 2000 spins. Data are encoded into 18 bits fixed point vectors with 1 sign, 5 integer and 12 decimal bits to optimize computation time and power consumption. An important feature our FPGA implementation of CAC is the use of several clock frequencies to concentrate the electrical power on the circuits that are the bottleneck of computation and require high speed clock. For the realization of the matrix-vector product, each element of the matrix is encoded with 2 bits precision ($w_{ij}$ is $-1$, 0 or 1). An approximation based on the combination of logic equations describing the behavior of a multiplexer allows to achieve $10^4$ multiplications within one clock cycle. The results of these multiplications are summed using cascading DSP and CARRY8 connected in a tree structure. Using pipelining, a matrix-vector product for a squared matrix of size $N$ is computed in $2 + 5 \log(N-4)/\log(5) + (\frac{N}{u})^2$ clock cycles (see supplementary material B.4) at a clock frequency of 50MHz with $u = 100$ which is determined by the limitation of the number of available electronic component of the
Figure 4: (a) Cumulative distribution of the time to solution \( P(\tau) \) for \( N = 400 \) SK problems. (b,c,d) Optimal cumulative distribution \( P^*(\tau) \) with \( P^*(\log(\tau)) \sim N(\mu(N), \sqrt{v}(N)) \) for CAC (b), SA (c), and NMFA (d), respectively. (e) Standard deviation \( \sqrt{v} \) of the logarithm of time to solution distribution vs. problem size \( N \). Shaded regions show the 95% error in the scaling exponents.

XCKU040 FPGA\(^6\) The calculation of the nonlinearity \( f_i \) and error terms is achieved at higher frequency using DSP in \( 8+(N/u) \) and \( 9+(N/u) \) clock cycles, respectively. In order to minimize energy resources and maximize speed, the nonlinear and error terms are calculated multiple times during the calculation of a single matrix-vector product (see supplementary material B).

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\(^6\)The block size \( u \) can be made at least 3 times larger using commercially available FPGAs, which implies that the number of clock cycles needed to compute a dot product can scale almost logarithmically for problems of size \( N < 1000 \) (see supplementary material B.4 for discussions of scalability) and that the calculation time can be further significantly decreased using a higher-end FPGA.
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Supplementary material A: theoretical analysis

1. Derivation of a potential function

First, we analyze the system described by eq. (1) only, when $\sigma_0 = 0$ and $\beta_i = \beta$, $\forall i$. In this case, the potential function $V(y) = -\frac{1}{2} \beta \sum_{ij} \omega_{ij} y_i y_j - \sum_i \int_0^{y_i} f_i(g_i^{-1}(y)) \, dy$ has the following property (47):

$$\frac{dV}{dt} = - \sum_i \frac{dy_i}{dt} (\beta \sum_j \omega_{ij} y_j + f_i(g_i^{-1}(y_i))), \quad (4)$$

$$= - \sum_i \frac{dy_i}{dt} (\frac{dx_i}{dt}), \quad (5)$$

$$= - \sum_i (\frac{dy_i}{dt})^2 (g^{-1})'(y_i). \quad (6)$$

Consequently, $V$ is such that $\frac{dV}{dt} < 0$ because $g$ is strictly monotonic and $\frac{dV}{dt} = 0 \implies \frac{dy_i}{dt} = 0$, $\forall i$. In other words, the dynamics of the system can be understood in this case as the gradient descent on the potential function $V$ and its stable steady states correspond to local minima of $V$.

2. Analysis of CAC

Next, we analyze the system described in eqs. (1) and (2) ($a$ is constant) by considering the change of variable $y_i = g(x_i)$ with $g$ such that $g^{-1}(y_i) = x_i$. In this case, eqs. (1) and (2) can be rewritten as follows (note that $f$ and $g$ are odd functions):

$$\phi'(y_i) \frac{dy_i}{dt} = f(g^{-1}(y_i)) + \beta e_i \sum_j \omega_{ij} y_j, \quad (7)$$

$$\frac{de_i}{dt} = \xi(y_i^2 - a)e_i, \quad (8)$$

where $\phi(y) = g^{-1}(y)$.

We analyze the dimension of the unstable manifold of CAC by linearizing the dynamics near the steady states and calculating the real part of eigenvalues of the corresponding Jacobian matrices. The steady state of the system in eqs. (7) and (8) can be written as follows:
\[ y^*_i = \sigma_i \sqrt{a}, \quad (9) \]
\[ e^*_i = -\frac{f(g^{-1}(\sigma_i \sqrt{a}))}{\beta \sqrt{a} h_i} = -\frac{f(g^{-1}(\sqrt{a}))}{\beta \sqrt{a} \sigma_i h_i}. \quad (10) \]

with \( h_i = \sum_j \omega_{ij} \sigma_j \). The last equality is a consequence of the fact that \( g \), and thus also \( g^{-1} \), are odd functions.

The Jacobian matrix \( J \) corresponding to the system of eqs. (1) to (2) at the steady state can be written in the block representation \( J = [J^{yy}; J^{ye}; J^{ey}; J^{ee}] \) with its components given as follows:

\[ J_{ij}^{yy} = \psi'(\sqrt{a}) \delta_{ij} - \frac{\psi'(\sqrt{a})}{\sqrt{a}} \frac{\omega_{ij}}{h_i \sigma_i}, \quad (11) \]
\[ J_{ij}^{ye} = \frac{\beta \sqrt{a} h_i \delta_{ij}}{\phi'(\sqrt{a})}, \quad (12) \]
\[ J_{ij}^{ey} = -\frac{2 \xi f(g^{-1}(\sqrt{a}))}{\beta h_i} \delta_{ij}, \quad (13) \]
\[ J_{ij}^{ee} = 0. \quad (14) \]

with \( \psi(y) = \frac{f(g^{-1}(y))}{\phi'(y)} \) and \( \phi(y) = g^{-1}(y) \). Note that we define \( J_{ii}^{ey} J_{jj}^{ye} = b \) with \( b = -2 \xi \sqrt{a} \psi'(\sqrt{a}) \).

The eigenvalues of the Jacobian matrix \( J \) are solutions of the polynomial equation \( P(\lambda) = \det[J - \lambda I] = \det[(J^{yy} - \lambda I)\lambda I - bI] \). The eigenvalues of \( J \) are thus solutions of the quadratic equation \( z(z - \lambda_i) - b = 0 \) where \( \lambda_i \) is the \( i \)th eigenvalue of the matrix \( J^{yy} \). Therefore, the eigenvalues of \( J \) can be described by pairs \( \lambda^+_i \) and \( \lambda^-_i \) given as follows:

\[ \lambda^+_i = \frac{1}{2}(\lambda_i + \sqrt{\Delta_i}), \quad \text{with} \]
\[ \lambda_i = \psi'(\sqrt{a}) - \frac{\psi'(\sqrt{a})}{\sqrt{a}} \mu_i, \quad \text{and} \]
\[ \Delta_i = \lambda_i^2 + 4b, \quad (15) \]

where \( \mu_i \) is the \( i \)th eigenvalue of the matrix \( D[(\sigma h)^{-1}]\Omega \).
The eigenvalues $\lambda_i^+$ and $\lambda_i^-$ become complex conjugate when the $\Delta_i = 0$, i.e., $[\psi'(\sqrt{a}) - \frac{\psi(\sqrt{a})}{\sqrt{a}} \mu_i]^2 - 8\xi \sqrt{a} \psi(\sqrt{a}) = 0$, which can be rewritten as follows:

$$\mu_i = G_i^+ (\sqrt{a}),$$

with $G_i^+(y) = \frac{y}{\psi(y)} [\psi'(y) \pm 2\sqrt{2\xi |y| \psi(|y|)}]$.

Lastly, the real part of eigenvalues $\lambda_i^+$ become equal to zero at the condition given as follows (note that $\text{Re}[\lambda_i^+] \geq \text{Re}[\lambda_i^-]$ and $\mu_i$ are real at local minima for which, $\forall j$, $\sigma_j h_j > 0$):

$$\sqrt{a} = 0 \text{ or } \psi(\sqrt{a}) = 0 \text{ if } \Delta_i \leq 0,$$

$$\mu_i = F(\sqrt{a}) \text{ otherwise.}$$

with $F(y) = \frac{\psi'(y)}{\psi(y)} y$. The dimension of the unstable manifold at a given fixed point is then given by the number of indices $i$ for which $\text{Re}[\lambda_i^+]$ is positive. To illustrate the destabilization of the ground state configuration of an Ising problem, we show in Figs. 5 and 6 the dynamics of CAC when solving a problem of size $N = 15$ spins when the state encoding for the ground state configuration is stable and unstable, respectively, for two different examples of functions $f$ and $g$ defining eqs. (1) and (2). The first set of functions $f$ and $g$ with $f(x) = (-1 + p)x - x^3$ and $g(x) = x$ shown in Fig. 5(a,b,c,d) corresponds to the soft spin model (or simulation of CIM) with chaotic amplitude control whereas the second one (e,f,g,h) with $f(x) = -x + \tanh[0.99x]$ and $g(x) = \tanh[x]$ corresponds to an Hopfield neural network with amplitude heterogeneity error correction. These two figures show that the stability of a given local minima of the Ising Hamiltonian depends on the value of the target amplitude $a$ as predicted in eq. (20).

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7Because the vector $\sigma \cdot h$ has positive components at local minima, the eigenvalues of $D[(\sigma \cdot h)^{-1}]\Omega$ are the same as the ones of $D[(\sigma \cdot h)^{-1}] \hat{\Omega} D[(\sigma \cdot h)^{-1}] \hat{\Omega}$ (Sylvester’s law of inertia), which is a symmetric real matrix. Thus, the eigenvalues $\mu_j$ are always real.
Figure 5: (a,e) Bifurcation diagram in the space \(\{\sqrt{a}, \mu = \mu_j(\sigma)\} \), \(\forall j \in \{1, \ldots, N\}\), at configuration \(\sigma\). The full red and green dotted lines correspond to the set for which \(Re[\lambda_i^\pm] = 0\) (where fixed points corresponding to local minima become stable) and \(\Delta_i = 0\) (where oscillations start to occur around fixed points). Red + and black \(\times\) symbols correspond to the largest eigenvalues \(\mu_0(\sigma)\) of the Jacobian at the ground state and excited states, respectively, of an Ising problem of size \(N = 15\) and \(a = 0.03\). In (b,f) and (c,g) are shown the dynamics of the variables \(x\) and \(e\), respectively. In (d,h) are shown the Ising Hamiltonian \(H(t)\) with horizontal lines showing the values of the Ising Hamiltonian at local minima. (a,b,c,d) \(f(x) = (-1 + p)x - x^3\) and \(g(x) = x\) with \(p = 0.95\), \(\beta = 0.1\), \(\xi = 0.1\). (e,f,g,h) \(f(x) = -x + \tanh[0.99x]\) and \(g(x) = \tanh[x]\) with \(\beta = 0.1\), \(\xi = 0.1\).
Figure 6: Same as Fig. 5 with $a = 0.13$. 
Supplementary material B: FPGA implementation

1. FPGA implementation of CAC

CAC has been implemented on a XCKU040 Xilinx FPGA integrated into the KU040 development board designed by Avnet. The circuit can process Ising problems of more than 2000 spins. The reconfigurable chip is a regular Ultrascale FPGA including 484,800 flip-flops, 242,400 Look Up Table (LUT), 12,000 Digital Signal Processing (DSP) and 600 Block RAM (BRAM). Initial value for $x_i$, $e_i$ and $\omega_{ij}$ are sent through Universal Asynchronous Receiver Transmitter (UART) transmission. UART protocol has been chosen because it does not require a lot of resources to be implemented and its simplicity.

Data are encoded into 18 bits fixed point with 1 sign bit, 5 integer bits which represents a good compromise between accuracy and power consumption. The power consumption of the FPGA is equal or lower to 5W depending on the problem size. The system is defined by its top-level entity that represents the highest level of organization of the reconfigurable chip.

2. Top level entity

The circuit is organized into four principal building blocks as shown on Fig. 7(a). Several clock frequencies have been generated to concentrate the electrical power on the circuits that need high speed clock when these circuits constitute a bottleneck in the current implementation. Finally, the organization of the main circuit is represented in Fig. 7(b). The control block is composed of Finite State Machines (FSM) and is well tuned to pilot all computation core, the Random-Access Memory (RAM), and data flowing between computation cores and RAM. All circuits are synchronized although the system utilizes multiple clock frequencies. Clock Enable (CE) ports on the BUFGCE component are used to stop the power when a circuit is not used in order to reduce further the global power dissipation.
Figure 7: Organization of the FPGA circuit. (a) The top layer entity is divided into four modules: The Phased-Locked Loop (PLL) that convert a differential clock of 250MHz into three clocks $f_g=50$MHz, $f_x=300$MHz and $f_e=100$MHz respectively representing the global clock, the clock for $x_i$ and the clock for $e_i$. Two UART modules are used to receive parameters and to return the results of the computation. (b) The Max-Cut circuit is composed of several processes aiming to control the exchange of data between the memory and the computation cores ($x_i$, $e_i$, $x_i\omega_{ij}$ and Ising). The three generated clocks are controlled by the Clock Enable (CE) port of the BUFGCE component of the FPGA.
3. Temporal organization of the computation

The control circuit pilot the computation in order to calculate several steps of $x_i$ and $e_i$ per calculation of the Ising coupling. The dynamics of CAC (see eqs. (1), (2) and (3)) is implemented based on the following pseudocode:

**Algorithm** Pseudocode from which the FPGA implementation is adapted

```
1: for $\nu \in \{0, \cdots , K\}$ do ▷ Iterate on the number of MVMs
2: \hspace{1em} $x' \leftarrow x$ ▷ Save state
3: \hspace{1em} $I \leftarrow \epsilon e(\Omega x')$ ▷ calculation of injection term
4: \hspace{1em} $\sigma \leftarrow \frac{x'}{|x'|}$
5: \hspace{1em} $H \leftarrow -\frac{1}{2} \sigma (\Omega \sigma)$ ▷ Ising energy calculation
6: for $i \in \{0, \cdots , n_x\}$ do ▷ Update nonlinear terms
7: \hspace{1em} $\Delta_x \leftarrow (-1 + p)x - (x)^3 + I$
8: \hspace{1em} $x \leftarrow x + \Delta_x dt_x$
9: for $i \in \{0, \cdots , n_y\}$ do ▷ Update error terms
10: \hspace{1em} $\Delta_e \leftarrow -\beta ((x')^2 - a)e$
11: \hspace{1em} $e \leftarrow e + \Delta_e dt_e$
12: $\beta \leftarrow \beta + \lambda dt$ ▷ Update $\beta$
13: $\Delta H \leftarrow H - H_{opt}$ ▷ Update $a$
14: $a \leftarrow \alpha + \rho \tanh(\delta \Delta H)$
15: if $\nu - \nu_c > \tau / dt$ then ▷ Reset of $\beta$
16: \hspace{1em} $\nu_c \leftarrow \nu$
17: \hspace{1em} $\beta \leftarrow 0$
18: if $H < H_{opt}$ then ▷ Update optimal $H$
19: \hspace{1em} $H_{opt} \leftarrow H$
20: $\nu_{opt} \leftarrow \nu$
21: $\nu_c \leftarrow \nu$
```

Note that the order of operations described in the pseudocode are a simplification of the ones occurring on the FPGA.

The temporal organization of the circuit represented in Fig. 8 shows how is controlled the reading and writing state on the RAM in the case of a problem size $N = 500$ spins. Fig. 8 (a) shows the case of a single $x_i$ and $e_i$ calculation per dot product which is the classic way to integrate the differential equations (1) and (2) using the Euler method. Fig. 8 (b) represents the case of eight and four calculations of $x_i$ and $e_i$, respectively, per dot product. In this case, the error correction term is computed with a normalized time step of $2^{-4}$ (half of the time step.
used in the computation of $x_i$). The total power consumption can be reduced by increasing the frequency of circuits involved in the calculation of $x_i$ because these circuits are smaller than those involved in the dot product calculation (see Fig. 9 (d) and (e)). Increasing the problem size will increase the power consumption by filling up the calculation pipelines but this can be balanced out by reducing the frequency used for the calculation of $x_i$ for larger problem size. The end of the dot product is followed by an update of all RAM and saving of $\sigma_i$ which correspond to the Most Significant Bit (MSB) of $x_i$ values. This step is not represented here.

![Figure 8: Temporal representation of the circuits where the red bars represent the computation cores and the blue bars the use of RAM. Here, (r) stand for read and (w) for write. (a) One time step representing the classical way of solving differential equation. In this configuration, the dot product create a bottleneck to the computation speed. (b) 8 time steps for $x_i$ and 4 time step for $x_i$ accelerating the computation time to find the ground state energy and create a new bottleneck to the number of possible time step possible. Note that the time between every red bars are necessary update the $x_i$ RAM which is not represented in this figure for better clarity.](image)

The use of several $x_i$ and $e_i$ calculations per dot product allows to reduce the bottleneck
created by the later whose calculation is in principle the most time consuming. Fig. 9 (a) to (c) show the reduction in time to solution vs. the number of $x_i$ calculations per dot product.

Figure 9: (a) The number of iterations of the $x$ variable to solution vs. the number of update, noted $n_x$, of the $x$ variable per matrix-vector product. (b) The number of matrix-vector multiplications MVM to solution. (c) Real time to solution. (d) Maximum possible time step with and without clock modulation on $x_i$. (e) Maximum possible time step with and without clock modulation on $e_i$.

4. Coupling

Overview of the coupling circuit

The dot product operation (see Fig. 10) is preceded by a multiplication by $\beta$ so that the domain of $x_i$ is reduced and, in turn, the number of digits required to encode the integer part of $x_i$. The result of the dot product is multiplied by the error correction term as shown in Fig. 10. Since the dot product is performed at 50MHz clock speed, the optional registers of the DSP are no longer
required and have been removed for the two multiplications resulting in 1 clock cycle operation for each operation.

Figure 10: The circuit designed to compute the coupling is composed of three parts: the multiplication between \( x_i \) and \( \beta \), the dot product, and multiplication with the error correction term.

**High speed and massively parallel multiplication**

The multiplication of the elements of a vector \( x \) by the element of a matrix \( \Omega \) can be performed using an approximation based on a specific circuit combining logic equations describing the behavior of a multiplexer and the optimized use of FPGA components. This circuit allows the design to achieve 10,000 multiplications in 1 clock cycle. In our case an element of \( x \) is fixed point binary vector on \( k \) bits that are multiplied by an element of a matrix composed of two bits vectors where \( \omega \) is an element of \( \Omega \) and \( \omega \in \{-1, 0, 1\} \). The behavior of a multiplexer that implements the multiplication of \( x \) by \( \omega \) by selecting \( R \in \{-x, 0, x\} \) is given as follows (\( \bar{x} \) represent \(-x\)):

\[
R = x\bar{\omega}_1\bar{\omega}_0 + \bar{x}\omega_1\omega_0
\]

where \( x \) is an element of a vector, \( \omega_i \) a binary vector and an element of the matrix \( \Omega \) with \( i \) the index of the binary vector that is either 1, the most significant bit (MSB) or 0, the less significant bit (LSB). If we expand eq. (21) to each bits \( x_i \) of the vector \( x \) and use Boolean operation, we obtain the equation eq. (22) given as follows:

\[
R = x\bar{\omega}_1\omega_0 + (\bar{x} \oplus C)\omega_1\omega_0
\]
where \(-x\) is represented by the two-complement operation \(\bar{x} \oplus C\) that consist of inverting the bits of \(x\) and adding \(C\) a constant corresponding to \(2^{-d}\) with \(d\) the decimal part size of the vector. Here, \(\bar{x}\) now represents the bit-wise not operation. Applying De Morgans law on eq. (22) will lead to the following:

\[
R = x\bar{\omega}_1\omega_0 + \bar{x}\omega_1\omega_0 \oplus C\omega_1\omega_0, 
\]

(23)

\[
R = \omega_0(x \oplus \omega_1) \oplus C\omega_1\omega_0, 
\]

(24)

\[
R = \omega_0(x \oplus \omega_1), 
\]

(25)

In eq. (24), we consider \(C = 0\) which introduces an absolute error of \(-2^{-d}\) when the MSB and the LSB of \(\omega\) are equal to 0. The aim of such approximation is that eq. (25) can be implemented by a single LUT3 component. Consequently, achieving 10,000 operations require \(k \times 10^4\) LUT3 where \(k\) represents the precision of \(x\) and is chosen to lower the required resources and error.

**First adder stage**

The circuit shown in Fig. 11 represents the operations of multiplication used in the dot product based on eq. (25). To accelerate the computation time, multiple access memory is utilized: Fig. 11 (a) and (b) show the implementation of multiple block RAM (BRAM) that output 100 rows of 100 values at the same time. Eq. (25) is implemented in LUT3 as described in the circuit of the Fig. 11 (c) which compute the addition of two elements of the vector \({\omega_{ij}x_i}\). Using LUT3 for the elements at index \(2i\), with \(i\) the index of the generated vectors beginning at 0, and multiplexers for the elements at index \(2i + 1\) ensures the use of lower resources and the optimal use of the configurable logic block (CLB).

**DSP tree**

For block matrices and vectors of size \(u\) with \(u = 100\), the dot product requires to perform 10,000 multiplications and 8,100 additions. The circuit of the Fig. 11 (c) computes two multiplications and one addition. Thus, by reproducing this circuit 5,000 times, the FPGA computes 15,000 operations in a clock cycle and generates 100 vectors of 50 values that need to be added. This operation is done using an adder tree represented in Fig. 12. A first stage of adder, that is
not represented between the circuit of the Fig. 11 (c) and Fig. 12 is realized using the CARRY8 component that reduces the 100 vectors of 100 elements to 100 vectors of 25 elements each. The remaining elements are then added using a DSP tree in adder mode. The advantage of using an adder tree of DSP is the low LUT number that is required, the optimal use of power consumption and the possibility to increase the frequency of the circuit. The Ultrascale architecture provided by the FPGA KU040 possesses a high number of DSP that can be cascaded allowing to reduce the routing circuit and the computation time. The DSP tree of Fig. 12 is repeated 100 times to compute at the same time all elements of the dot product resulting in the use of 1,200 DSP.

**Scalability of such architecture for bigger FPGA**

The number of clock cycles required to perform the dot product is given as follows:

\[
C_t(u, N) = K + (N/u)^2
\]  

(26)

where \( N \) is the problem size, \( u \) the divider that partitions the matrix (in the current implementation \( u=100 \)) and \( K \) the number of clock cycles required for the multiplications and additions. The adder tree composed of CARRY8 and DSP previously proposed is constrained by the following condition:

\[
\frac{N}{2h_C + 5h_D} = 1, \tag{27}
\]

where \( h_C \) represents the height of the CARRY8 tree and \( h_D \) the height of the DSP tree. The CARRY8 requires only one clock cycle when two cascaded DSP need 5 clock cycles. The height \( K \) of the adder tree (in clock cycle) is then:

\[
K = h_C + 5h_D. \tag{28}
\]

We can fix \( h_C \) as a constant according to the proposed FPGA circuit and find \( h_D \) as follow:
\[ N = 2^{hc} + 5^{hd}, \]  
\[ N - 2^{hc} = 5^{hd}, \]
\[ \log(N - 2^{hc}) = h_D \log(5), \]
\[ h_D = \frac{\log(N - 2^{hc})}{\log(5)}. \]  
(29)  
(30)

Then the height \( K \) is equal to:
\[ K = h_C + 5\frac{\log(N - 2^{hc})}{\log(5)}. \]  
(31)

The adder tree increases logarithmically if we assume that an infinite amount of resources is available. Also, we show here that the design can be significantly improved if \( u \) become larger with more available resources.

5. Ising energy circuit

The Ising energy is computed at the same time as the main dot product of \( x_i \) by \( \omega_{ij} \) because it shares the same output from the RAM that store the \( \omega_{ij} \). As for the dot product, the Ising energy has been computed using logic equations to fit in a minimal number of LUT. The logic equation for the multiplication of \( \sigma \) by the matrix \( \Omega \) can be described as follows:

\[ S_1 = (\omega_1 \oplus \sigma_j)\omega_0, \]  
(32)
\[ S_0 = w_0. \]  
(33)

where \( \sigma_i \) is the sign of \( x_i \) and \( S \) is a 2 bits vector representing the multiplication of \( \sigma_i \) at index \( i \) by \( \omega \) (representing \( \omega_{ij} \)) which is also represented by 2 bits whose index is either 0 (LSB) or 1 (MSB).

The Fig. [13] shows a schematic of the circuit used to compute the Ising energy. Note that the Ising energy of a matrix \( M \) divided into matrices \( m_{ij} \), where \( i \) and \( j \) are the indexes of the partitioned \( M \), is equal to the sum of the energies of \( m_{ij} \). Thus, the output of the pipelined Ising energy circuit is added with itself.
6. **Non-linear term**

To optimize the use of the electrical power, $x_i$ has been designed to use the highest frequency $f_x$ and the error correction use and intermediate frequency $f_e$. Both are computed several times during the operation of the dot product to reduce the computation time. Fig. [14] shows the circuit use to compute one element of the vectors $x_i$ and $e_i$ that are reproduced 100 times. The circuits use pipelined DSP to compute additions, subtractions and multiplications. A shift register is used to multiply by the $dt$ of Euler approximation. To reduce the number of DSP into the design, $x_i^2$ is shared between $x_i$ and $e_i$ through a true dual port RAM that can be used with two different clocks to synchronize the two circuits. The RAM is controlled by an external FSM in the control module of Fig. [7].

7. **Modulation term**

The circuits implementing the modulation of the target amplitude $a$ defined in eq. (3) are shown in Fig. [15]. A saturation circuit has been designed to reduce the domain of the sigmoid function. Pre and post operations are available into the DSP for reducing the use of LUT.

The tangent hyperbolic function is approximated by Lagrange interpolation using only 96 LUT and 1 DSP. The Lagrange interpolation, defined by $L$, is given as follows:

$$L(x) = y_0 + \frac{y_1 - y_0}{x_1 - x_0} (x - x_0)$$  \hspace{1cm} (34)

where, $L(x)$ is the interpolation function, $[x_0, y_0]$ the coordinate of the point situated before the results and $[x_1, y_1]$ the coordinate of the point after the result (see Fig. [16]).

8. **Power consumption**

Energy consumption of the circuit is determined by the number of logic transitions (from 0 to 1 or 1 to 0) and the frequency with $P = \langle s \rangle CV^2F$ where $P$ is the power dissipated by a transistor based circuit, $C$ the switching capacitance, $V$ the voltage and $F$ the frequency, and $\langle s \rangle$ the average number of switch per clock cycle. Voltage and capacitance are FPGA dependent since it is already manufactured. The digital circuit are at the highest power consumption when the components are enabled and when the clock signal drives the Configurable Logic Block (CLB) or
the DSP. Thus, Enable and disable the block RAM is efficient to reduce the consumption however, clock gating shows better performances in this implementation. The methods have been extended on the available FF of the Xilinx FPGA and DSP which possess clock enable gate. However, when the design becomes large, high number of signal propagating enable towards CLB or DSP increase fanout and routing complexity. This can be solved by using BUFGCE component that are available in the FPGA and able to enable or disable the clock. Thus, when a given circuit is not needed, the clock can be disabled which will reduce significantly the power consumption.

The KU040 boards use Infineon regulators IR38060 incorporated voltage and current sensors. These sensors can be access either from the FPGA or from external bus with the PMBUS protocol which is based on i2c. We used here an Arduino to communicate with the regulators and record power data.

The power has been measured for different problem sizes and does not exceed 5W. Experiments show that the most critical operation for energy efficiency and computation time is the dot product which dissipates most of the FPGA power and needs more clock cycles to operate.
Figure 11: Representation of the high speed and multiple memory access apply to a circuit used for the dot product. (a) 100 RAM are instantiated and can be accessed at the same time. Each RAM corresponds to a row of the matrix $\Omega$. Each element $\omega_{ij}$ of $\Omega$ is encoded on a two bits vector. (b) As in (a), 100 RAM can be accessed at the same time to compose the vector $x$. (c) The $\Omega_{i,2j}$ and $x_{2i}$ values are injected into a LUT3 to compute the eq. (25). The $x_{2i+1}$ values are injected into a multiplexer (MUX) whose selector is controlled by the LSB of $\Omega_{i,2j+1}$. The output of the LUT3 and the MUX are propagated through the CARRY8 component that add or subtract according to the value of $\Omega_{i,2j+1}$ MSB.
Figure 12: Schematic representation of the DSP tree following the multiplication and the two addition stages shown in Fig. This first addition stage takes 5 clock cycles and produces 5 values that can be added into a new DSP stage of 5 clock cycles.
Figure 13: Ising energy circuit. The LUTs integrate eqs. (32) and (33) producing vectors of $\sigma_j \omega_{ij}$. The results are added up using an adder tree composed of CARRY8 resulting in a vector that is multiplied by $\sigma_i$ using a multiplexer (MUX). The MUXs select between the result or its negation with $\sigma_i$ as a selector. Then, the output of MUXs are added and negated.
Figure 14: Circuits of the non-linear terms $x_i$ and $e_i$. The two terms use different clocks and share their results through a dual port block RAM allowing to read and write at different speed. Both circuit use DSP for high speed computation and are generated one hundred times to perform parallel computation.
Figure 15: Circuit of the target amplitude using pre-subtractor into one DSP and post-subtractor into the other DSP. A saturation comparator has been added to reduce the range of value at the input of the sigmoid function. The sigmoid function uses an interpolation of the tangent hyperbolic.

Figure 16: (a) Schematic representation of the FPGA implementation of the Lagrange interpolation function. Each points used for the interpolation is separated by 0.5. A shift register allows to select the address of interpolated points into the Read Only Memory (ROM). The sign of x is conserved so that only the positive part is interpolated. (b) Representation of the tanh function and interpolated points.
11. Parameter values used for solving SK spin glass instances

The parameter values used for solving SK spin glass instances are shown in Tab. 2.

| Symbol | meaning                              | value          |
|--------|--------------------------------------|----------------|
| $\beta$ | coupling strength                     | 0.25           |
| $\alpha$ | target amplitude baseline            | 3.0            |
| $p$    | linear gain                           | $1 - \left(\frac{N}{220}\right)^{-2}$ |
| $\rho$ | amplitude and gain variation          | 3              |
| $\delta$ | sensitivity to energy variations      | 4              |
| $\gamma$ | rate of increase of $\xi$            | 0.00011        |
| $\tau$ | max. time w/o energy change          | 1200           |
| $n_x$  | number of iterations for nonlinear terms | 6              |
| $n_e$  | number of iterations for error terms | 4              |
| $dt_x$ | normalized time-step of nonlinear terms | $2^{-5}$       |
| $dt_e$ | normalized time-step of error terms  | $2^{-4}$       |

Table 2: Parameters used for solving SK problem instances.
Supplementary material C: scaling vs. recently proposed Ising machines

In order to assess the scalability of the chaotic amplitude control and its FPGA implementation, we compare its median time to solution in seconds and extrapolations against that of the NTT CIM (not parallelized) (9), Hopfield neural network implemented using memresistors (mem-HNN) (59), restricted Boltzmann machine using a FPGA (FPGA-RBM) (58). Extrapolations are based on the hypotheses of scaling in $e^{\gamma N}$ and $e^{\gamma \sqrt{N}}$ by fitting the available experimental data up to $N = 100$ for mem-HNN and FPGA-RBM, $N = 150$ for NTT CIM, and $N = 700$ for FPGA-CAC. Fig. 17 shows that mem-HNN, FPGA-RBM, and NTT CIM have similar scaling exponents, although FPGA-RBM tends to exhibit a scaling in $e^{\gamma N}$ rather than $e^{\gamma \sqrt{N}}$ for $N \approx 100$ (58). In the hypothesis of scaling in $e^{\gamma \sqrt{N}}$ for these three machines, extrapolations show that FPGA-CAC exhibits smaller time to solution for $N \gtrsim 1000$ even though we do not take into account the increase in scaling exponents that would occur when implementing larger problem sizes for mem-HNN and FPGA-RBM. Fig. 17 shows moreover that the 20W implementation of FPGA-CAC has smaller time to solution than DA (19) at $N \approx 700$. It should be noted that the experimental data points of Fig. 17 are directly taken from published results of each Ising machine (9, 58, 59) which are not based on the same benchmark instances. It can be nonetheless expected that the algorithm implemented in mem-HNN, which is similar to mean-field annealing, has the same scaling behavior as simCIM and NMFA (see Fig. 2).
Figure 17: Median time to solution and extrapolations based on the hypotheses of scaling in $e^{\gamma N}$ and $e^{\gamma \sqrt{N}}$ by fitting the available experimental data for each Ising machine (see text). Shaded regions show the 95% error in the scaling exponents. For FPGA-CAC and DA, the lower, higher, and upper whisker of boxes show the 50th, 80th, and 90th percentiles of the real time to solution distribution.
Supplementary material D: benchmark on GSET

Performance of FPGA-CAC in finding the maximum cuts known, i.e., lowest Ising Hamiltonian known, of graphs in the GSET benchmark are shown in Tab. 3.

Table 3: Performance of FPGA-CAC implementation in finding the maximum cuts known, i.e., lowest Ising Hamiltonian known, of graphs in the GSET benchmark. \(id\), \(C^{opt}\), and \(C^*\) are the name of instances, best maximum cuts known from (27, 52) and the proposed method, respectively, after 20 runs. \(p_0\) is the probability that FPGA-CAC finds the cut \(C^*\) in a single run. Moreover, \(< t_{BLS} >\) and \(< t_{FPGA} >\) are the averaged time to solution using BLS written C++ and running on a Xeon E5440 2.83 GHz (52) and the proposed scheme simulated implemented on the KU040 FPGA, respectively.

We believe a better tuning of the system parameters would allow to find the best known cut for all instances (except the 2nd instance of \(N = 2000\)). For instances 14 and 15 of size...
$N = 2000$, FPGA-CAC finds solutions of better quality than previously known from (52) and (27). The solutions found are given as follows.

- Solution of instance 14 of size $N = 2000$ with cut 7685:

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[1,-1, 1,-1,-1,-1,-1, 1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,
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Solution of instance 15 of size $N = 2000$ with cut 7679:
Parameter values used for solving instances of the GSET are shown in Tab. 4.

| Symbol | meaning                              | value          |
|--------|--------------------------------------|----------------|
| $\epsilon$ | coupling strength                     | $\frac{3}{d_0}$ |
| $\alpha$ | target amplitude baseline            | 3.0            |
| $\pi$ | linear gain baseline                 | $1 - 400d_1^{-2.5}$ |
| $\rho$ | amplitude and gain variation          | 1.0            |
| $\delta$ | sensitivity to energy variations     | $\frac{2}{N}$ |
| $\gamma$ | rate of increase of $\beta$         | $\frac{2}{N}$ |
| $\tau$ | max. time w/o energy change          | $9N$           |
| $n_x$ | number of iterations for nonlinear terms | 6              |
| $n_e$ | number of iterations for error terms | 4              |
| $dt_x$ | normalized time-step of nonlinear terms | $2^{-6}$       |
| $dt_e$ | normalized time-step of error terms  | $2^{-4}$       |

Table 4: Parameters used for solving GSET problem instances.

where $d_1$ is a function of the maximum degree given as $d_1 = \max\{d_0, 10\}$ and $d_0 = \text{mean}_i\{\sum_j |\omega_{ij}|\}$.
Supplementary material E: other algorithms

1. Details of NMFA simulation

Noisy mean-field annealing can be simplified to the following discrete system (21):

\[ y_i(n+1) = (1 - \alpha)y_i(n) + \alpha \tanh \left( \frac{1}{\sigma \omega T(t)} \sum_j \omega_{ij} y_j(n) \right) + \sigma_r r_i, \]  

(35)

with \( \sigma_\omega = \sqrt{\sum_j J_{ij}^2} \). When the noise is not taken into account (i.e., \( r_i = 0 \)), the steady state of eq. (35) is given as follows:

\[ y_i^* = \tanh \left( \frac{1}{\sigma \omega T(t)} \sum_j \omega_{ij} y_j(n) \right), \]  

(36)

Note that the solutions of the eq. (36) are the same as those of the TAP naive mean-field equations (see (22)). Moreover, they are the same as the steady state of eq. (1) when considering the change of variable \( y_i = g(x_i) \) with \( g(x) = \tanh(x) \) and \( \beta_i(t) = \frac{1}{T(t)} \). In fact, it can be shown that the two systems have the same set of attractors (60).

The default parameters used in the numerical simulations are given as follows (21):

| Symbol | meaning                        | value |
|--------|--------------------------------|-------|
| \( \alpha \) | recombination parameter | 0.15  |
| \( \sigma_r \) | standard deviation of noise   | 0.15  |

Moreover, the temperature \( T(t) \) is decreased with time according to an annealing schedule.

The eq. (35) is simulated on a GPU using CUDA code provided in (21). Various parameters of the temperature scheduling \( T(t) \) and parameters \( \alpha \) and \( \sigma_r \) have been tried in order to maximize the performance of this algorithm in finding the ground state of SK spin glass problems (see Figs. 18 and 19).
Figure 18: 50th (a) and 80th (b) percentiles of the step to solution distribution vs. the problems size $N$ of bimodal Sherrington-Kirkpatrick spin glass problems.

Figure 19: Exponential and inverse linear scaling of $T(t) = \frac{1}{\beta(t)}$ for $T = 1000$. 
2. Details of CIM simulation (simCIM)

The physical model of the measurement feedback coherent Ising machine developed in (8) can be simplified as follows:

\[ x_i(n + 1) = AG(x_i(n)) + r_1 + \sqrt{\xi_0} \Theta(B \sum_j \omega_{ij} G(x_i(n)) + r_3) \]  (37)

where \( \Theta(x) = R(-Fx; x_{\text{max}}) \) and \( R(x; y) \) is the saturation function defined as \( R(x; y) = x \) if \( |x| < y \) and \( R(x; y) = x_{\text{max}} \) otherwise. If we assume, for simplicity, that the saturation function \( \Theta(x) \) is simply linear with \( \Theta(x) = F_t x \), then eq. (37) can be written under the form of eq. (1) by using the following:

\[ f(x_i) = AG(x_i), \quad g(\beta x_i) = G(x_i), \quad \beta_i(t) = F(t) B \sqrt{\xi_0}, \] and \( r_1 + \sqrt{\xi_0} + r_3 = \sigma \eta_i \).

Eq. (37) is simulated using a GPU implementation in order to approximate accurately the success probability when it is small.
3. Benchmark set availability

Sherrington-Kirkpatrick instances used in this paper are available upon request. The GSET instances are available at https://web.stanford.edu/yye/yye/Gset/.