Probabilistic Memristive Networks – Part I: Application of a Master Equation to Networks of Binary ReRAM cells

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Abstract—The possibility of using non-deterministic circuit components has been gaining significant attention in recent years. The modeling and simulation of their circuits require novel approaches, as now the state of a circuit at an arbitrary moment in time cannot be precisely predicted. Generally, these circuits should be described in terms of probabilities, the circuit variables should be calculated on average, and correlation functions should be used to explore interrelations among the variables. In this paper we use, for the first time, a master equation to analyze the networks composed of probabilistic binary memristors. Analytical solutions of the master equation for the case of identical memristors connected in-series and in-parallel are found. Our analytical results are supplemented by results of numerical simulations that extend our findings beyond the case of identical memristors. The approach proposed in this paper facilitates the development of probabilistic/stochastic electronic circuits and advance their real-world applications.

Index Terms—memristors, networks, probabilistic computing, probabilistic logic

I. INTRODUCTION

RESISTANCE switching memories are a very promising class of memory devices that have been intensively studied in the past few decades. The simple device structure, scalability, fast speed, and compatibility with current silicon technology make them ideal candidates for the next generation of storage-class memory [1]. However, significant temporal (cycle to cycle) and spacial (device to device) parameter fluctuations observed in all reported ReRAM cells [2] present a major obstacle for their wide-scale commercialization. As it is obvious that the stochasticity is an inherent feature of the resistance switching memories, the accurate and predictable modeling of single ReRAM devices and circuits thereof require approaches beyond the deterministic models [3], [4].

The method of stochastic differential equations [5] is the standard way to take account for fluctuations in otherwise deterministic models. Some applications of this method to the problem of stochasticity in ReRAM cells have been reported [6], [7], [8], [9] including the postulation of stochastic memory elements by YVP and Di Ventra in 2011 [10]. However, the method of stochastic differential equations has yet to be adopted widely in the ReRAM community, possibly because of its relative complexity.

The randomness in the ReRAM switching can also be described in terms of probabilities ignoring the details of microscopic dynamics. In particular, it was shown experimentally that the off-to-on transition in electrochemical metallization cells (EMCs) occurs according to the Poisson distribution [11], [12]. Moreover, Medeiros-Ribeiro et al. [13] investigated the distribution of switching times in TiO$_2$ valence change memories, which are another type of ReRAM cells. They found that both off-to-on and on-to-off transitions are described by a log-normal distribution. The Poisson distribution observed in EMCs [11], [12] indicates a Markovian dynamic that can be conveniently described in terms of a master equation.

This is the first part of a series devoted to probabilistic memristive networks. In this first part we consider networks composed of $N$ binary ReRAM cells, or simply memristors governed by Poisson switching statistics. A master equation is introduced to describe the network dynamics on average that, in a particular realization, consists in consecutive jumps over some of $2^N$ states. The master equation is solved analytically for the cases of identical memristors connected in-series and in-parallel. The derivations made in this work assume an abstract two-state model of ReRAM cells and could be verified with those devices that behave according to such a model.

This paper is organized as follows. In Sec. II preliminaries are presented that include the probabilistic model summary, and numerical simulation details. Sec. III presents the master equation, and its solutions for the cases of in-series and in-parallel connected memristors. Correlation functions are introduced and derived in Sec. IV. We conclude in Sec. V. The appendix contains a concise mathematical treatment of the dynamics of the off-to-on transition in the circuit of $N$ in-parallel and in-series connected memristors, and some other supplementary results.

II. PRELIMINARIES

A. ReRAM cell switching model

In this paper we consider the networks of probabilistic binary resistance switching memories. By binary [17], [18] we mean that our devices can be found in one of two well-defined resistance states, $R_{on}$ and $R_{off}$. By probabilistic we mean that randomness plays a role in the process of switching. It is

$^1$The claim [14] that ReRAM cells are memristors [15] is debatable [19].
assumed that the switching events are instantaneous, and their probability is a well-known function of the applied voltage or current. For compactness, we use the terms “memristors” and “probabilistic binary resistance switching memories” interchangeably. However, it should be emphasized that the devices considered here are not described by the memristor equations \( [15] \). \[4\].

The studies \([11, 12]\) of the off-to-on transition in electrochemical metallization cells have shown that the probability of switching within the time interval \( \Delta t \) follows the Poisson distribution

\[
P(t) = \frac{\Delta t}{\tau(V)} e^{-t/\tau(V)}, \tag{1}
\]

where \( \tau(V) \) is the voltage-dependent characteristic switching time, and \( V \) is the voltage across the cell. A very good agreement with experimental data was obtained using

\[
\tau(V) = \tau_0 e^{-V/V_0}, \tag{2}
\]

where \( \tau_0 \) and \( V_0 \) are fitting parameters. Eq. \(2\) indicates that the resistance switching in EMCs is an activated process (an energy barrier must be overcome to change the cell resistance). We note that the exponent in Eq. \(1\) is the occupation energy barrier must be overcome to change the cell resistance).

To graphically represent Eqs. \(3\)–\(4\), Fig. 1 shows the current-voltage curves of a probabilistic binary memristor. In particular, Fig. 1(a) demonstrates a very stochastic behavior in the switching region, with a variability from cycle to cycle. After the averaging (Fig. 1(b)), the current-voltage curves resemble the curves in deterministic models. We emphasize that in Fig. 1(b) the hysteresis collapses at high frequencies – a well-known feature of the deterministic memristive behavior \([4]\).

**B. Numerical simulations**

In the simulations presented below, a circuit of \( N = 10 \) memristors initially in the off-state \((R(t = 0) = R_{\text{off}})\) is considered. It is assumed that the positive applied voltage drives all the memristors into the on-state. In some of our calculations, it is assumed that the memristors are identical with Fig. 1 parameters. Moreover, the impact of device variability was investigated numerically, assuming a uniform distribution of the parameters \( \tau_0 \) and \( V_0 \).

To simulate in-parallel connected memristors (Fig. 2(a)), each memristor is subjected to a voltage \( V_i = V_a \). A probability for any memristor to switch from the off- to on-state is then generated according to Eq. \(3\) as \( \Delta t \gamma_{0 \rightarrow 1}(V_a) \), where \( \Delta t \) is the simulation time step. This probability is then compared to a random number between zero and one. If the probability is greater than the number generated for that memristor, it switches on. Time is then incremented and the process continues until all memristors are in the on state. The time it takes for the last memristor to switch is then recorded.

To simulate in-series connected memristors (Fig. 2(b)), a chain of \( N \) memristors is subjected to a voltage \( V_a \). The simulation process is the same as in the case of in-parallel memristors, except the voltage across memristors change as the switching progresses. Therefore, at each step, the applied voltage and therefore the switching probabilities are generated for each memristor. As before, the time is then recorded when the final memristor has switched to the on state. For the purpose of comparison, the average voltage across each memristor in the in-parallel and in-series calculations was the same.

This same analysis is also performed for nonidentical memristors. That is \( \tau_0 \) and \( V_0 \) are no longer held constant, but are randomly generated for each memristor using uniform distributions.
Fig. 2. Memristive networks considered in this paper: (a) $N$ memristors connected in-parallel, (b) $N$ memristors connected in-series, and (c) circuit combining memristors, resistors, and subjected to several voltage sources.

III. MASTER EQUATION

A. General framework

Consider a network composed of $N$ probabilistic memristors, some (or no) resistors, voltage and/or current sources (for an example see Fig. 2(c)). There are $2^N$ possible network states corresponding to various combinations of the memristor states. Let’s use $\Theta = (...)jij$ to denote a particular network state. Here, $i$ is the state of the first memristor (0/1 for the off/on-state), $j$ is the state of the second memristor, and so on. For a particular network state $\Theta$, the voltage across $m$-th memristor, $V_{m}^{\Theta}$, can be found using Kirchhoff’s circuit laws.

Generally, each realization of circuit dynamics is unique as the time moments when the switchings occur cannot be predicted deterministically. Starting from the same initial state and repeating the experiment many times, one can find time-dependent occupation probabilities of network states, $p_{\Theta}(t)$, that describe the circuit evolution on average. These probabilities can be calculated using the master equation.

The master equation can be generally written as

$$\frac{dp_{\Theta}(t)}{dt} = \sum_{m=1}^{N} \left( \gamma_{m}^{\Theta} p_{\Theta_{m}}(t) - \gamma_{m}^{\Theta_{m}} p_{\Theta}(t) \right), \tag{5}$$

where $\Theta_{m}$ is the network state obtained from $\Theta$ by flipping the state of $m$-th memristor, $\gamma_{m}^{\Theta}$ are the transition rates for $m$-th memristor in the configuration $\Theta$ (given by, e.g., Eqs. (4) and (4)), and $\gamma_{m}^{\Theta_{m}}$ is defined similarly. We note that the general form of the master equation does not depend on the circuit topology, presence or absence of resistors in the circuit, and how the external signals are applied. This information is contained in the voltage-dependent transition rates, $\gamma_{m}^{\Theta}$ and $\gamma_{m}^{\Theta_{m}}$, that should be evaluated for each network state with the use of Kirchhoff’s laws. Examples of (reduced) transition schemes are presented in Fig. 3.

The solution of Eq. (5) can be employed to find various distributions and circuit characteristics on average. For instance, the average resistance of memristor 1 can be found using

$$\langle R_{1}(t) \rangle = R_{off}p_{01}^{0} + R_{on}p_{11}^{0}, \tag{6}$$

where $p_{01}^{0} = \sum_{k,j=0,1} p_{k,j0}(t)$, and $p_{11}^{0} = \sum_{k,j=0,1} p_{k,j1}(t)$. Here, the sums are taken over all possible states with a fixed state of memristor 1. Moreover, various terms in the right-hand side of Eq. (5) can be of great help in various calculations, including the calculations of average switching times and their distributions (presented in the next Sec. III-B).

B. Two memristors connected in-series: A case study

To exemplify the approach in Eq. (5), consider a relatively simple yet interesting problem of the resistance switching in a circuit of two probabilistic binary memristors connected in-series. It is assumed that the memristors are connected to a constant positive voltage, and experience switching from the off- into the on-state. Thus the initial conditions are $p_{00} = 1$ and $p_{ij} = 0$ for $(i,j) \neq (0,0)$, Fig. 3(a) presents a reduced transition scheme for the problem (Fig. 3(a)). It can be used to calculate the average switching time according to

$$\langle T_{11} \rangle = \int_{0}^{\infty} t2\gamma_{01}p_{01}(t)dt = \frac{1}{2\gamma_{00}} + \frac{1}{2\gamma_{01}}. \tag{13}$$

Average switching time of memristor 1. – This switching time is associated with transitions $00 \rightarrow 01$ and $10 \rightarrow 11$. 

Note that the sign of $V_{m}^{\Theta}$ depends on the memristor connection polarity.
For these processes, the switching probability distribution can be expressed as

\[ \Phi_1(t) = \gamma_{10} p_{00}(t) + \gamma_{10} p_{10}(t). \] (14)

Using Eq. (14), one can find

\[ \langle T_1 \rangle = \int_0^\infty t \Phi_1(t) dt = \frac{1}{2 \gamma_{10}} + \frac{1}{2 \gamma_{10}^2}. \] (15)

**Average resistance of memristor \( I \).** This quantity can be directly calculated using the probabilities (10)-(12) as

\[ \langle R_1(t) \rangle = R_{\text{off}} ( p_{00}(t) + p_{10}(t) ) + R_{\text{on}} ( p_{01}(t) + p_{11}(t) ). \] (16)

It is interesting to compare the switching time of memristors connected in series with the switching time for memristors connected in parallel. The latter is derived in the Appendix B (Eq. (B.6) for \( N = 2 \)). Using \( R_{\text{on}} = 1 \, \text{k} \Omega, R_{\text{off}} = 10 \, \text{k} \Omega, \tau_0 = 3 \times 10^5 \, \text{s}, V_0 = 0.05 \, \text{V}, V_a = 2 \, \text{V} \) (in-series), and \( V_a = 1 \, \text{V} \) (in-parallel), we find

\[ \langle T_{11} \rangle = 309 \, \text{\upmu s}, \] (17)
\[ \langle T_{12} \rangle = 928 \, \text{\upmu s}. \] (18)

This estimation indicates that the switching of memristors connected in-series occurs significantly faster compared to the switching of in-parallel connected ones. Physically, such behavior can be explained by the voltage divider effect where the switching of one memristor leads to a voltage increase across another accelerating its switching.

**C. More complex cases**

Using numerical simulations, we studied the switching in the networks of \( N = 10 \) memristors connected in-series and in-parallel. The simulation approach is described in Sec. II-B. We investigated the networks of identical and non-identical memristors. In the case of identical memristors, we have verified that numerical results are in agreement with analytical results presented in Appendix A. In fact, one of our main analytical findings is the expression for the network switching time, Eq. (A.15), which can be rewritten as

\[ \langle T_N \rangle = \sum_{j=0}^{N-1} \frac{1}{(N-j) \gamma_j}, \] (19)

where \( \gamma_j \) is defined below Eq. (A.1), and can be evaluated with the help of Eq. (3). We emphasize that Eq. (19) also describes the off-to-on transition in the network of in-parallel connected memristors (see Eq. (B.7)), and can be used to model the on-to-off transitions (with a proper selection of switching rates).

Fig. 4 shows distributions of switching times in the networks of identical and non-identical memristors connected in-parallel. In the case of non-identical memristors, \( \tau_0 \) and \( V_0 \) are determined by probabilistic distributions for each memristor to see if the randomness of \( \tau_0 \) and \( V_0 \) have any significant effect on the network dynamics. According to Fig. 4, the randomness of \( \tau_0 \) and \( V_0 \) significantly broadens the distribution of switching times in the case of in-parallel connected memristors. As memristors connected in-parallel switch independently, their network switching time depends significantly on the slowest switching memristor, which, statistically, has a longer characteristic switching time than that of identical memristors.

The distributions of network switching time for identical and non-identical memristors connected in-series are presented in Fig. 5. We note that Figs. 4 and 5 were obtained assuming the same voltage across each memristor on average. In the case of in-series connected memristors (Fig. 5), the voltages across memristors were recalculated at each time step according to the instantaneous network configuration. Generally, in-series connected memristors switch faster than the memristors connected in-parallel. This is explained by a cascading effect for in-series connected memristors: The switching to the on-state of one generates an increased probability to switch for the remaining off-state memristors. We note that the shorter (on-average) network switching time for the case of non-identical memristors in Fig. 5 is due to the important role of the fastest switching memristor in the network.

![Fig. 4. Distributions of time taken for \( N = 10 \) memristors connected in-parallel to all switch from the off- to on-state with at \( V_a = 1 \, \text{V} \). The identical memristors are with \( \tau_0 = 3 \times 10^5 \, \text{s}, \) and \( V_0 = 0.05 \, \text{V} \). The non-identical memristors are characterized by the random flat distributions of \( \tau_0 \) and \( V_0 \) in the intervals \([2 \times 10^5, 4 \times 10^5]\) s and \([0.04, 0.06]\) V, respectively. The mean switching time 1.81 ms for identical and 15.3 ms for non-identical memristors. The bin size is 0.05 ms.

![Fig. 5. Distribution of time taken for \( N = 10 \) memristors connected in-series to all switch from the off- to on-state with at \( V_a = 1 \, \text{V} \). The identical memristors are with \( \tau_0 = 3 \times 10^5 \, \text{s}, \) and \( V_0 = 0.05 \, \text{V} \). The non-identical memristors are characterized by the random flat distributions of \( \tau_0 \) and \( V_0 \) in the intervals \([2 \times 10^5, 4 \times 10^5]\) s and \([0.04, 0.06]\) V, respectively. The mean switching time 1.81 ms for identical and 15.3 ms for non-identical memristors. The bin size is 0.05 ms.](image-url)
IV. CORRELATION FUNCTIONS

A. General approach

When the memristors interact through a circuit, correlations between their states develop. Correlation functions [19] are a common tool used for their description. For instance, for two memristors $i$ and $j$, the correlation function can be defined as

$$K_{ij}(t, \tau) = \langle R_i(t)R_j(t+\tau) \rangle - \langle R_i(t) \rangle \langle R_j(t+\tau) \rangle.$$  (20)

Similarly, we can define the auto-correlation function

$$K_{ii}(t, \tau) = \langle R_i(t)R_i(t+\tau) \rangle - \langle R_i(t) \rangle \langle R_i(t+\tau) \rangle,$$  (21)

which allows us to find, in particular, the variance $\text{Var}(R_i)$ of the resistance of selected memristor $i$, by substituting $\tau = 0$ into Eq. (21).

B. Two memristors connected in-series

To derive correlation functions analytically, we first introduce a joint probability distribution function

$$\Phi(t_1, t_2)dt_1dt_2 = \gamma_0e^{-2\gamma_0|t_1-t_2|}t_2^2e^{-\gamma_0(t_1-t_2)}dt_1.$$  (22)

Eq. (22) describes the probability of switchings of memristor 1 in the time interval from $t_1$ to $t_1 + dt_1$, and memristor 2 in the time interval from $t_2$ to $t_2 + dt_2$ in the assumption of $t_1 > t_2$. The case of $t_2 > t_1$ is described by the right-hand side of Eq. (22) with $1 \leftrightarrow 2$. We note that in Eq. (22), one can recognize the well-known expression for the conditional probability.

Eq. (22) can be used to re-derive various quantities already discussed in Sec. II.B. For the convenience of the reader, some of the relevant relations are provided in Appendix C. To derive the correlation function (20) we note that the resistance as a function of time can be presented as

$$R_i(t) = R_{off} + (R_{on} - R_{off})H(t - t_j),$$  (23)

where $H(\cdot)$ is the Heaviside step function, and $t_j$ is the switching time of the memristor $i$. The average of $R_i(t)$ is given by Eq. (16). The calculation of $K_{12}(t, \tau)$ in Eq. (20) involves finding the average of the product of Heaviside functions

$$\langle H(t - t_j)H(t + \tau - t_2) \rangle = \int_0^\infty \int_0^\infty \Phi(t_1, t_2)H(t - t_j)H(t + \tau - t_2)dt_2dt_1 = p_{10}(t) + p_{11}(t) - e^{-\gamma_0\tau}p_{01}(t).$$  (24)

One can show that the correlation function can be written as

$$K_{12}(t, \tau) = \frac{R_{off} - R_{on}}{2} = [1 - p_0(t)]p_0(t + \tau) - p_{01}(t)e^{-\gamma_0\tau},$$  (25)

where $p_0(t) = p_{00}(t) + p_{01}(t)$. The same technique can be used to calculate the auto-correlation function $K_{ii}(t, \tau)$ defined by Eq. (21). In this case, it is even simpler to do it because we need only the switching probability distribution Eq. (14). As a result we get for the auto-correlation function

$$K_{ii}(t, \tau) = \frac{R_{off} - R_{on}}{2} = [1 - p_0(t)]p_0(t + \tau).$$  (26)

C. More complex cases

A normalized one-time correlation function for two randomly chosen memristors $i$ and $j$ can be calculated using

$$\tilde{K}_{ij}(t) = \frac{< R_i(t)R_j(t) > - < R_i(t) > < R_j(t) >}{(R_{off} - R_{on})^2},$$

where $R_i(t)$ is the resistance of one of the memristors at time $t$. The above expression was evaluated numerically for $N = 10$ memristive networks. The results are shown in Figure 6 for the networks of identical and non-identical memristors.

Several features in Fig. 6 can be mentioned here. First, at the initial moment of time $\tilde{K}_{ij}(0) = 0$ as the initial state of network is deterministic (all memristors are in the off-state initially). Second, the in-series correlation functions have a maximum when the probabilities of $R_{on}$ and $R_{off}$ are approximately the same. Moreover, the maximum value of these functions does not exceed 0.25. Third, at long times, the in-series functions approach zero as the memristor states at long times are nearly deterministic (all memristors end up in the on-state). Finally, $\tilde{K}_{ii}(t)$ for in-parallel connected memristors is always zero as such memristors do not interact through the network. Therefore, correlations among them do not develop.

V. DISCUSSION AND CONCLUSION

The modeling of probabilistic memristive networks presents opportunities and challenges. The opportunities open up as there is an increasing interest in the stochastic computing [12], [20], [21], [22], and, in principle, all ReRAM devices exhibit a certain level of stochasticity. The fact that the probabilistic memristive networks can be described in terms of the master equation offers strong possibilities to simulate various processes ranging from chemical reactions to radioactive decay in hardware. The challenges are due to the complexity of probabilistic modeling. In the case of binary memristors, the number of network states increases as $2^N$. Therefore, to describe even modest networks, say, of $N = 20$ memristors, already more than $10^6$ network states are required.

In the case of symmetries some simplifications are possible (e.g., identical memristors, etc.).
Electrochemical metallization cells have been considered as binary memristors \[17\], \[18\], and currently they are the most suitable type of ReRAM cells to test our theory. In fact, the model parameters used in this work (listed in Fig. 1 caption) were extracted from a fitting curve in Ref. \[11\] with a subsequent scaling of \( V_0 \) in the assumption of \( \sim 20 \text{ nm a-Si} \) layer. However, the extracted value of \( \tau_0 = 3 \cdot 10^5 \text{ s} \) is quite short\[1] A more realistic (in terms of the long-time information storage capability) model – an adaptive probabilistic threshold model (APTM) – is formulated in Appendix D. The results found with APTM are qualitatively similar to the ones found in the main text.

Finally, we note that care must be taken when the binary model is used to simulate experiments with physical devices. A limitation is related to the fact that in electrochemical metallization cells the off-to-on transition may occur in a step-by-step fashion when the filament advances through several hopping sites \[11\]. Moreover, in the resistor-EMC circuits the filament growth may be reduced due to the voltage divider effect \[11\]. These effects are beyond the binary approximation and will be addressed in the next part of the series.

To conclude, the modeling of stochastic memristors and their circuits is still in a nascent stage compared to the case of deterministic devices. In this paper we have introduced a master equation-based approach to model networks of probabilistic memristors. This approach provides the most complete information about the system including various switching times, occupation probabilities, and correlation functions. This work advances the field of probabilistic modeling of resistance switching memories by introducing the methodology to model their networks, and by finding the solution of a master equation in several model cases.

**APPENDIX A**

**Switching of \( N \) memristors connected in-series**

Consider the dynamics of \( N \) identical probabilistic memristors connected in-series to a constant voltage source \( V_o \). It is assumed that at \( t = 0 \) all the memristors are in the off-state, and the applied voltage induces their switching into the on-state.

**A. Equations**

We simplify the kinetic equation (5), made possible due to symmetric initial conditions and similarity of memristors.

In this situation the probabilities of all network states with the same number of memristors in the on-state are the same (for instance, for \( N = 2 \), \( p_{01}(t) = p_{10}(t) \)). To simplify the notation, in this Appendix we use \( p_m \) to denote the probability of a state with \( m \) memristors in the on-state. Then, Eq. (5) can be rewritten in the form

\[
\frac{dp_m}{dt} = m \gamma_{m-1} p_{m-1} - (N - m) \gamma_m p_m, \tag{A.1}
\]

where \( \gamma_{m-1} \) is the transition rate from \( p_{m-1} \) to \( p_m \), and \( \gamma_m \) is defined similarly.

\[\text{This constant is a measure of the information storage time at zero applied voltage.}\]

We note that the occupation probabilities are subjected to the constraint

\[
\sum_{m=0}^{N} \binom{N}{m} p_m(t) = 1. \tag{A.2}
\]

Here, the binomial coefficients \( \binom{N}{m} \) take into account the number of states with the same number of memristors in the on-state. Differentiating Eq. (A.2) with respect to \( t \) we get

\[
\sum_{m=0}^{N} \binom{N}{m} \frac{dp_m}{dt} = 0. \tag{A.3}
\]

In what follows, Eq. (A.1) is solved analytically using the following initial conditions: \( p_0(t) = 1, \ p_m(t) = 0 \) for \( m = 1, \ldots, N \).

**B. Building solution**

Defining \( a_m = (N - m) \gamma_m \) and \( b_m = m \gamma_{m-1} \), Eq. (A.1) takes the form

\[
\frac{dp_m}{dt} = b_m p_{m-1} - a_m p_m. \tag{A.4}
\]

For \( m = 0 \), it reduces to

\[
\frac{dp_0}{dt} = -a_0 p_0
\]

having the solution

\[
p_0(t) = e^{-a_0 t}. \tag{A.5}
\]

For \( m = 1 \), the equation is

\[
\frac{dp_1}{dt} = a_1 p_0 - b_1 p_1,
\]

whose solution can be presented as

\[
p_1(t) = b_1 \left( \frac{e^{-a_0 t}}{a_1 - a_0} + \frac{e^{-a_1 t}}{a_0 - a_1} \right). \tag{A.6}
\]

Finally, consider the case of \( m = 2 \). The solution of

\[
\frac{dp_2}{dt} = b_2 p_1 - a_2 p_2
\]

is given by

\[
p_2 = b_1 b_2 \left[ \frac{e^{-a_0 t}}{(a_1 - a_0)(a_2 - a_0)} + \frac{e^{-a_1 t}}{(a_0 - a_1)(a_2 - a_1)} + \frac{e^{-a_2 t}}{(a_0 - a_2)(a_1 - a_2)} \right]. \tag{A.7}
\]

**C. Solution**

Based on the above analysis, the probability \( p_m(t) \) involves \( m \) exponentially decaying terms. Therefore, at step \( m \) we can write

\[
p_m(t) = \sum_{i=0}^{m} C_i^m e^{-a_i t} \tag{A.8}
\]

and at step \( m-1 \)

\[
p_{m-1}(t) = \sum_{i=0}^{m-1} C_i^{m-1} e^{-a_i t}. \tag{A.9}
\]
Here, $C^m_i$ is the $i$-th pre-exponential factor at the step $m$.

To find the relation among the coefficients $C^m_i$ at different steps, consider Eq. (A.4). Substituting $p_{m-1}$ into Eq. (A.9) and solving this equation, one can find

$$p_m(t) = \sum_{i=0}^{m-1} b_m \frac{C^m_i}{a_m - a_i} e^{-a_i t} + C^m_m e^{-a_m t}. \quad (A.10)$$

Here, $C^m_m$ is the integration constant, that can be determined from the initial condition $p_m(t = 0) = 0$. Importantly, Eq. (A.10) shows explicitly how the pre-exponential factors $C^m_i$ evolve from step to step.

As we prove below, $C^m_m$ can be presented as

$$C^m_m = \prod_{i=0}^{m-1} \frac{b_{i+1}}{a_{i+1} - a_i}. \quad (A.11)$$

Therefore, the occupation probability of a state with $m$ memristors in the on-state is given by

$$p_m(t) = \left( \prod_{k=1}^{m} b_k \right) \sum_{j=0}^{m} e^{-a_j t} \prod_{i=0, i \neq j}^{m} \frac{1}{a_i - a_j}. \quad (A.12)$$

We note that the above expression works in the entire range of $m = 0, \ldots, N$. In the expression for $p_N(t)$, one should use $a_N = 0$. The coefficients $a_i$ and $b_i$ are defined above Eq. (A.4).

D. Coefficient $C^m_m$

To demonstrate that the expression (A.11) for $C^m_m$ is valid, we show that Eq. (A.11) leads to the correct initial condition $p_m(t = 0) = \delta_{m,0}$. For this purpose, it is sufficient to verify that the right-hand side of Eq. (A.12) is zero at $t = 0$. Explicitly, based on Eq. (A.12), it is necessary to show that

$$0 = \frac{1}{(a_1 - a_0)(a_2 - a_0)\ldots(a_m - a_0)} + \ldots + \frac{1}{(a_0 - a_m)(a_1 - a_m)\ldots(a_{m-1} - a_m)}. \quad (A.13)$$

For this purpose consider a contour integral

$$\oint \frac{1}{(a_0 - z)(a_1 - z)\ldots(a_m - z)} dz \quad (A.14)$$

over a circular path $R \to \infty$, see Fig. A.1. On the one hand, using Jordan’s lemma, it is clear that the integral is zero. On the other hand, its value can be found using the residue theorem. The combination of these approaches leads to Eq. (A.13).

E. Average switching time

The average switching time $\langle T_N \rangle$ into the final state $N$ can be evaluated following Eq. (13) approach. In the case of $N$ memristor network this time can be expressed as

$$\langle T_N \rangle = \lim_{t \to \infty} t \frac{dP_N(t)}{dt} = \int_0^\infty t b_N P_{N-1}(t) dt. \quad (A.15)$$

The substitution of Eq. (A.12) into Eq. (A.15) results in

$$\langle T_N \rangle = \left( \prod_{k=1}^{N} b_k \right) \sum_{j=0}^{N-1} \frac{1}{a_j^2} \prod_{i=0, i \neq j}^{N-1} \frac{1}{a_i - a_j}. \quad (A.16)$$

Eq. (A.16) can be substantially simplified. For this purpose, we considered a contour integral

$$\oint \frac{1}{z(a_0 - z)(a_1 - z)\ldots(a_N - z)} dz \quad (A.17)$$

over a circular path (as in Fig. A.1) in the limit of $R \to \infty$. The evaluation of Eq. (A.17) integral was performed based on the residue theorem (similarly to Sec. A-D). This procedure led us to certain relations that were used for a consecutive simplification of terms in the sum in Eq. (A.16). Eventually, the following relation for the average switching time has been derived:

$$\langle T_N \rangle = \sum_{j=0}^{N-1} \frac{1}{a_j}. \quad (A.18)$$

APPENDIX B

SWITCHING OF $N$ MEMRISTORS CONNECTED IN-PARALLEL

Consider the dynamics of $N$ identical probabilistic memristors connected in-parallel to a constant voltage source $V_0$. It is assumed that at $t = 0$ all memristors are in the off-state, and the applied voltage induces their switching into the on-state. The dynamics of each memristor is given by the following kinetic equation

$$\frac{dp_0(t)}{dt} = -\gamma_0^1 p_0, \quad (B.1)$$

whose solution

$$p_0(t) = e^{-\gamma_0^1 t} \quad (B.2)$$

gives the probability to find the memristor in the off-state, while the probability to find it in the on-state is

$$p_1(t) = 1 - e^{-\gamma_0^1 t}. \quad (B.3)$$

As memristors connected in-parallel are independent, the probability to find the system with all memristors in the on-state is given by the product of individual probabilities, namely,

$$p_{11\ldots11}(t) = p_1^N = \left( 1 - e^{-\gamma_0^1 t} \right)^N. \quad (B.4)$$
The corresponding switching time can be evaluated using
\[
T_{\parallel,N} = \int_0^1 t \, dp_{111111} = \int_0^\infty t \, dp_{111111} \, dt.
\] (B.5)

For \( N = 2 \), Eq. (B.5) leads to
\[
T_{\parallel,2} = 2 \int_0^\infty t \left(1 - e^{-\gamma_0 t}\right) e^{-\gamma_2 t} \gamma_0 dt = \frac{3}{2 \gamma_0}.
\] (B.6)

For an arbitrary \( N \), Eq. (B.5) leads to
\[
T_{\parallel,N} = \frac{1}{\gamma_0} \left(1 + \frac{1}{2} + \frac{1}{3} + \ldots + \frac{1}{N}\right).
\] (B.7)

The above equation is the exact expression for the average switching time of \( N \) memristors connected in-parallel. The asymptotic behavior of (B.7) at \( N \to \infty \) can be understood from the following expression, which is well-known:
\[
\sum_{k=1}^N \frac{1}{k} = \ln N + \gamma + O\left(\frac{1}{N}\right),
\] (B.8)

where \( \gamma \approx 0.577 \) is Euler’s constant.

We note that all formulae for \( N \) memristors connected in-parallel can be obtained from expressions in Appendix A in the limit of equal transition rates.

**APPENDIX C**

**SOME RELATIONS RELATED TO THE JOINT SWITCHING PROBABILITY DISTRIBUTION \( \Phi(t_1, t_2) \)**

It is straightforward to derive the following results based on Eq. (22) for \( \Phi(t_1, t_2) \). The average network switching time for the case \( N = 2 \) can be calculated as
\[
\langle T_{11} \rangle = \int_0^\infty \int_0^\infty dt_1 dt_2 \max(t_1, t_2) \Phi(t_1, t_2),
\] (C.1)

where the function \( \max(t_1, t_2) \) returns the maximum of two switching times \( t_1 \) and \( t_2 \). This definition leads to the same result Eq. (13) that is based on the kinetic equation approach.

Besides, the switching probability distribution \( \Phi_1(t_1) \) can be calculated by integration with respect to another switching time \( t_2 \):
\[
\Phi_1(t_1) = \int_0^\infty dt_2 \Phi(t_1, t_2),
\] (C.2)

Moreover,
\[
p_{11}(t) = \int_0^t dt_1 \int_0^t dt_2 \Phi(t_1, t_2),
\] (C.3)
\[
p_{01}(t) = \int_0^t dt_1 \int_0^\infty dt_2 \Phi(t_1, t_2),
\] (C.4)
\[
p_{00}(t) = \int_0^\infty dt_1 \int_0^\infty dt_2 \Phi(t_1, t_2).
\] (C.5)

**APPENDIX D**

**ADAPTIVE PROBABILISTIC THRESHOLD MODEL (APTM)**

The threshold-type resistance switching models [23], [24], [25] have gained popularity and significant research is being carried out based on such models. Here we formulate an adaptive probabilistic threshold model for probabilistic memristor modeling.

Similarly to the main text, we consider binary memristors characterized by two possible resistance states, \( R_{on} \) and \( R_{off} \). To take into account a wide range of possible switching behaviors, the following voltage-dependent switching rates are postulated:
\[
\gamma_{0\rightarrow 1}(V) = \begin{cases} \gamma_{on} \left( \frac{V}{V_{on}} - 1 \right)^{\alpha_{on}}, & V > V_{on} > 0 \\ 0, & \text{otherwise} \end{cases}
\] (D.1)
\[
\gamma_{1\rightarrow 0}(V) = \begin{cases} \gamma_{off} \left( \frac{V}{V_{off}} - 1 \right)^{\alpha_{off}}, & V < V_{off} < 0 \\ 0, & \text{otherwise} \end{cases}
\] (D.2)

where \( V_{on} \) and \( V_{off} \) are the threshold voltages for the transition into the off- and on-states, respectively, \( \gamma_{on}, \gamma_{off}, \alpha_{on}, \) and \( \alpha_{off} \) are constants.

An example of current-voltage characteristics for APTM memristor is presented in Fig. D.1.

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