Learning from Distinctive Candidates to Optimize Reduced-Precision Convolution Program on Tensor Cores

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Abstract

Convolution is one of the fundamental operations of deep neural networks with demanding matrix computation. In a graphic processing unit (GPU), Tensor Core is a specialized matrix processing hardware equipped with reduced-precision matrix-multiply-accumulate (MMA) instructions to increase throughput. However, it is challenging to achieve optimal performance since the best scheduling of MMA instructions varies for different convolution sizes. In particular, reduced-precision MMA requires many elements grouped as a matrix operand, seriously limiting data reuse and imposing packing and layout overhead on the schedule. This work proposes an automatic scheduling method of reduced-precision MMA for convolution operation. In this method, we devise a search space that explores the thread tile and warp sizes to increase the data reuse despite a large matrix operand of reduced-precision MMA. The search space also includes options of register-level packing and layout optimization to lesson overhead of handling reduced-precision data. Finally, we propose a search algorithm to find the best schedule by learning from the distinctive candidates. This reduced-precision MMA optimization method is evaluated on convolution operations of popular neural networks to demonstrate substantial speedup on Tensor Core compared to the state of the arts with shortened search time.

1. Introduction

Convolution is one of the fundamental operations of deep neural networks. Starting from the original work of (Krizhevsky et al., 2012a), convolution has been used as one of the core operations of convolutional neural networks (Krizhevsky et al., 2012b; He et al., 2016; Szegedy et al., 2016). More recently, convolution was incorporated in the other types of neural networks such as recurrent neural network (RNN) and Transformer (Dosovitskiy et al., 2020) to collaborate within various network structures for capturing useful features in the computer vision domain.

Although its versatility in various neural networks, convolution demands a large amount of computation and memory space. It is often computed Toeplitz matrix multiplication with dimension often spanning to hundreds to even thousands, taking up a significant portion of execution time. To alleviate the computational burden of convolution, various customized hardwares have been introduced. In a graphic processing unit (GPU), Tensor Core is a specialized matrix processing hardware equipped with reduced-precision matrix-multiply-accumulate (MMA) instructions to increase throughput. MMA instructions enable massively parallel execution of matrix multiplications grouped with a size of matrix operand increased inversely proportional to the bit-precision. For example, NVIDIA T4’s INT4 MMA takes a group of 8x32 elements as an operand, which is twice larger than INT8 MMA (8x16) (Carrasco et al., 2018). These reduced MMA instructions are designed to provide a significant increase of throughput in executing reduced-precision convolution.

However, it is challenging to use reduced precision MMA instructions of Tensor Cores to achieve optimal performance in convolution execution. With a careful analysis, we identified three main sources of inefficiency in reduced precision MMA when it is used for representative convolution computations. First, the data reuse opportunity is significantly limited since MMA requires many elements grouped as matrix operands. Such a large grouping often causes unbalancing in workload division when setting up blocks and tiles for GPU execution. Second, reduced precision input should be packed before it is executed as operands of reduced precision MMA. In the case of INT4 MMA, the packing includes quantization of 8 consecutive values (in 32-bit) into a packed vector of 4-bit elements. This low-level data alignment incurs noticeable overhead with additional memory accesses. Third, due to this packing, the data layout of the convolution operand should be adjusted in a way that its lowest dimen-

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Preliminary work.
ation matches with the packing granularity. Since the output of one convolution layer is often used as the input of the next convolution layer, mismatch of data layout between the output and input results in high re-layout cost due to uncoalesced memory accesses.

One might overcome these causes of inefficiency by finding optimal scheduling of MMA instructions such as setting up of tile and block sizes that maximizes the data reuse while suppressing the overhead of data packing and re-layout. However, the best scheduling of MMA instructions varies for different convolution sizes. Not alone the variety of neural network structures, various shapes and sizes of convolution operations are incorporated even within a single neural network. For example, ResNet18 includes four stages of convolution layers, each of which takes different feature map sizes and the number of channels. Since the shape of input and weight imposes significantly different computation behavior for a convolution operation, it is not feasible to generalize a certain MMA scheduling for achieving universally optimal speedup.

This work proposes an automatic scheduling method of reduced-precision MMA for convolution operation. In this method, we devise a search space that explores the thread tile and warp sizes to increase the data reuse despite a large matrix operand of reduced-precision MMA. The search space also includes options of register-level packing and layout optimization to lesson overhead of handling reduced-precision data. Finally, we propose a search algorithm to find the best schedule by learning from the distinctive candidates. This reduced-precision MMA optimization method is evaluated on convolution operations of popular neural networks to demonstrate substantial speedup on Tensor Core compared to the state of the arts with shortened search time.

2. Background

2.1. Reduced Precision Convolution on Tensor Cores

As a convolution consists of scalar multiplications and their accumulation, it is mathematically identical with vector inner product (Figure 1(a)). Therefore, we can convert convolution into GEMM (General Matrix to Matrix Multiplication) with some data layout transformation called im2col. Convolution with feature map width \(W\), height \(H\), input channel \(I\), output channel \(O\), and convolution kernel \(R, S\) with batch size of \(N\) can be translated into matrix multiplication of \((N*H*W, I*R*S) \times (I*R*S, O)\) where \(N*H*W\) is the number of rows of the output matrix, \(O\) is the number of columns and \(I*R*S\) is the accumulation dimension.

In order to redesign convolution into a simple matrix multiplication problem, the input feature map is lowered into im2col layout. As Figure 1(a) presents, every data required to process 3x3 convolution for each pixel are converted into a single matrix row. This process is also known as lowering as multi-dimensional tensors are converted into lower-level, two-dimensional matrix for efficient hardware implementation.

Enormous matrix multiplication can be parallelized using the matrix tiling procedure. As every element inside each row and column can be computed independently, each computation of the output matrix sub-title can be fully parallelized without any dependency among themselves. GPU, hardware specialized for parallelized workload, can exploit this nature of matrix multiplication. Furthermore, as all elements inside the output matrix can be parallelized, GPU can select any parallelization configuration. Figure 1(b) depicts one example of parallel processing of tiled matrix multiplication. The output matrix is divided into multiple thread block tiles and then into thread warp tiles. Finally, each thread warp tile is divided into the smallest atomic WMMA (warp matrix-multiply-accumulate) tile with predefined size for Tensor Core instructions.

2.2. Searching for Computation Schedule

As GPUs can have a massive space of parallelization options, finding the optimal tile size for parallelism is critical to the overall runtime of the neural networks. Figure 2(b),(c) depicts one example of such parallelization scheduling. Too small parallelization may result in occupancy problems or inefficiency due to resource starvation. At the same time, too much parallelization may result in the serialization of workload or inefficiency due to the parallelization limit. Furt-
convolution kernel sweeps every pixel on the original feature map, required feature map data for each pixel overlap each other, resulting in pixel-wise data duplicates. The bigger the kernel size the convolution has, the more duplicates the lowered feature map contains.

Note that the position of pixel-level data duplicates is determined by the algorithm-level convolution configuration such as convolution filter size, filter stride, and feature map size, which can be informed to the compiler. In other words, once a high-level convolution configuration is given, the compilation system can statically predict where the duplicates exist. As shown in Figure 4, the compiler already has information on a data tuple with index (1, 2) having the same data with a data tuple with index (9, 10). Likewise, every index with data duplicate can be told and be informed to the code generator. Based on the duplicate information, the code generator can generate code that can reduce the number of memory loads by not fetching data duplicates.

### 3.1.2. IMPLEMENTATION

Among duplicates on the feature map, let’s say one of the duplicates is the genuine datum and the others are duplicate data. Also, name the index pointing to the genuine datum as genuine index and index pointing to the duplicate datum as duplicate index. For example, in Figure 4 if index 8 is a genuine index for a datum 22, index 16 and 24 become duplicate indices for the corresponding datum. Then, the duplicate index to genuine index many-to-one-mapping represents the whole duplicates information of the lowered feature map data.

The main concept of the duplicate-aware load is to transform the address space with duplicates into the address space only with genuine data via the duplicates index information. By transforming the memory space itself into data space without any duplicates, every data access cannot structurally generate any data duplicate. This can be done both on GPU shared memory and GPU registers. Algorithm 1 shows the actual implementation of the duplicate-aware load. On the compile time, the compiler can identify the information about the position of the duplicates with a high-level def-

![Figure 4. Index view of duplicates and possibility of compiler’s static awareness.](image-url)

Figure 3. Pixel-wise duplicates generated on the process of lowering.

| Pixel # 0 | Pixel # 1 | Pixel # 2 |
|----------|----------|----------|
| 0 1 2 3 4 5 | 0 1 2 3 4 5 | 0 1 2 3 4 5 |
| 10 11 12 13 14 15 | 10 11 12 13 14 15 | 10 11 12 13 14 15 |
| 20 21 22 23 24 25 | 20 21 22 23 24 25 | 20 21 22 23 24 25 |
| 30 31 32 33 34 35 | 30 31 32 33 34 35 | 30 31 32 33 34 35 |

| Pixel # 0 | Pixel # 1 | Pixel # 2 |
|----------|----------|----------|
| 0 1 2 3 4 5 | 0 1 2 3 4 5 | 0 1 2 3 4 5 |
| 1 2 3 4 5 6 | 1 2 3 4 5 6 | 1 2 3 4 5 6 |
| 2 3 4 5 6 7 | 2 3 4 5 6 7 | 2 3 4 5 6 7 |
| 3 4 5 6 7 8 | 3 4 5 6 7 8 | 3 4 5 6 7 8 |

Figure 3. One example result of a search for optimal scheduling of MMA on Tensor Cores.

3. Method

3.1. Duplicate-Aware Load

3.1.1. IM2COL LOWERING

It appears that the lowered feature map data contains a considerable amount of data duplicates in Figure 3. As 3x3 input channels, output channels, convolution width, height, batch size, and 2) GPU architecture such as streaming multiprocessors (SMs), L1/L2 cache size, or processor performance. We search this massive search space using modified AutoTVM with our contribution to the search algorithm.

![Figure 2. One example result of a search for optimal scheduling of MMA on Tensor Cores.](image-url)
3.2. Register-level Data Packing

3.2.1. DATA BITS REQUIRED FOR ACCUMULATION

MMA (Matrix Multiply and Accumulation) execution, as its name suggests, consists of scalar multiplication and accumulation. The execution therefore needs an accumulation register to accumulate values on every vector multiplication. If we assume a 4-bit integer convolution with 128 input channels for accumulation, the accumulation register requires 16 data bits for the maximum possible value $(2^4 \times 2^4 + 2^4 \times 2^4 = 2^{15})$. Furthermore, quantized neural networks rarely exhibit such data with excessive magnitude \cite{choi2018efficient}. However, NVIDIA output tile accumulators set the accumulator bit width for 4-bit convolution as 32-bit, wasting a great number of bits as zeroes. Numerically, we need about 1 million input convolution channels for accumulation to fully utilize the 32-bit accumulator on 4-bit 3x3 convolution.

3.2.2. POST-CONVOLUTION DATA PROCESSING

On convolutional neural networks, after the convolution computation, remaining epilogue operations such as relu, batch normalization, and bias addition should be computed. We found that the accumulated data with high bit width are stored directly to shared memory for further epilogue processing, wasting a great amount of cache memory bandwidth. After the epilogue processing, the result data are finally clipped to lower bits and packed into 32-bit integer datatype (Figure 5). It is because lower bit clipping should not be done before all computations including the epilogue have ended. That is, on the other hand, lower bit clipping can be conducted after the epilogue processing is done. If we reorder the position of epilogue processing before storing data to shared memory (Figure 6), clipping and packing data can be carried out before shared memory store, saving a great amount of GPU cache bandwidth. Furthermore, as the allocated shared memory size for the output feature map is reduced (Figure 7), we can allocate more thread blocks on the GPU SMs (Streaming Multiprocessors) due to relaxed L1 constraints, reinforcing better parallelism.

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**Algorithm 1** Duplicate-aware load

1: Followings omit weight data load for simplicity:
2: `Duplicates_info = Compiler.get_info()`  
3: `foreach ThreadBlock do`
4:   `foreach dst in genuine_idx do`
5:     `f_shared[dst] = f_global[src]`
6:   `end for`
7: `foreach ThreadWarp do`
8:   `foreach dst in genuine_idx do`
9:     `src = get_genuine(src)`
10:    `f_reg[dst] = f_shared[src]`
11:   `end for`
12: `foreach f_idx do`
13:   `f_idx = get_genuine(f_idx)`
14:   `foreach w_idx do`
15:     `MMA(f_reg[f_idx], w_reg[w_idx])`
16:   `end for`
17: `end for`
18: `end for`

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*Figure 5.* Excessive usage of shared memory before data packing.

*Figure 6.* Reduce usage of shared memory after data packing.
3.2.3. IMPLEMENTATION

As clipped and well-packed data should be constructed before the shared memory store, the whole data packing process has to be handled on the registers. However, especially for intra-warp data gathering/scattering, a programmer cannot have full control of the registers as a single warp (32 threads) operates as an atomic unit of execution. Instead, a programmer can make use of CUDA’s “warp shuffle” intrinsic function, which allows threads to read or write to each other’s data registers in a predefined way. Figure 8 illustrates how a warp shuffle function works. Before a warp shuffle, sixteen threads are holding a single data on each register. Warp shuffle function with offset 4 moves a data of thread 4 to thread 0, thread 5 to thread 1, and so on. Such data movement is conducted on the granularity of warp shuffle width, in this case, 8.

Using warp shuffling, we can implement intra-warp, register-level data packing on a GPU. Figure 9 shows the actual CUDA implementation of 4-bit integer packing inside a 32-bit integer data register. As you can see in Figure 9, each 4-bit integer datum is gathered and packed inside a single warp in an iterative process. After the final step of the iterative process, only a single thread among the eight holds the useful data which may result in useless store requests even with data packing. To avoid this inefficiency, gather the other output register tiles into registers with don’t care values so that all store requests from all registers can be meaningful. (Figure 10)

3.3. DATA LAYOUT AWARE REGISTER MANIPULATION

3.3.1. COALESCED MEMORY ACCESS ON GPU

For the best practice of GPGPU programming, all global memory access should be coalesced, which means that addresses for memory access should not diverge inside a single warp. Otherwise, useless data transactions may occur. This is because the atomic data access unit is 32-byte in modern GPU architecture so consecutive huge accesses perform better than divergent small accesses.

Meanwhile, for Tensor Core operation, the input feature map tensor should be split into atomic WMMA register tile size. That is, NHWC data layout should be reshaped into NHWCnc layout where ‘n’ stands for the input feature map batch size as a row size of WMMA register tile and ‘c’ stands for the input feature map channel size as a column size of WMMA tile. We found that such data layout reshape results in uncoalesced memory access because the size of the lowest channel dimension ‘c’ is 16-bytes-wide because of GPU hardware intrinsic size of CUDA WMMA operation, which does not satisfy the atomic 32-bytes load of the GPU memory system. Moreover, such 16-bytes-wide memory accesses are diverged among batches, resulting in the failure of consecutive load (Figure 11).

3.3.2. CONSIDERATION ON THE DATA LAYOUT

To avoid this uncoalesced memory access, we suggest global memory layout be stored as NHWCnc layout rather than
NHWC when using NVIDIA Tensor Cores. Otherwise, all GPU kernels will suffer from uncoalesced memory access. However, additional effort is required to consistently maintain the same data layout. The number of output feature map channels depends on the number of filters, not the number of input feature map channels. So we cannot guarantee the last channel dimension (‘c’) of the output feature map would be the same as the input feature map after the convolution execution. once we are done with register-level data packing which section 3.2 suggests, the last channel dimension gets even more reformed.

Nevertheless, the ‘n’ and ‘c’ dimensions are originated from the warp level MMA operation, which means that the sub-tensor with such two dimensions is intentionally covered with registers inside a single warp. Therefore, for consistent data layout maintenance, only an additional single warp shuffle intrinsic function is required.

3.4. Diversity-Aware Schedule Search

Existing AutoTVM suggests a simulated-annealing-algorithm-based exploration module with statistical cost-model to efficiently search for optimal configuration in large exhaustive search space (Figure 12).

Statistical cost-model allows exploration module to compare which configuration’s low-level code is faster without real hardware measurement. The cost model is trained by (configuration, runtime) dataset with ranking loss objective function. AutoTVM can evaluate many configurations in a short time using this cost model.

The exploration module picks candidates which are expected to optimal configuration using a simulated annealing algorithm and cost-model (Figure 12-(b)). The exploration module repeats the selection a set number of times. To search candidates efficiently in a large search space, the exploration module mutate one random knob of previous candidates to explore better performance candidates. the exploration module uses a simulated annealing algorithm with the cost-model score as an energy function. The algorithm compares previous candidates and mutant candidates to pick better candidates repeatedly, finally selecting the top-performing batch of candidates to run on real hardware. The result of candidates’ performance data is used to update the cost-model.

The weakness of AutoTVM is Exploration module picks too many similar candidates that have similar performance and this does not help to improve the quality of the cost model. At the beginning of the AutoTVM search, the cost-model is only trained with a small number of randomly selected configurations. This cost model is hard to predict diverse configurations accurately. Inside the search space, not all knobs of configuration are critical to performance. Therefore, there are many similar configurations that have similar performance in the search space. The cost model overestimates many configurations similar to the previous best and underestimates many candidates who have not learned it. It causes a simulated annealing algorithm to pick candidates which are too similar to previous candidates and also have similar performance. These new candidates are not useful for improving the cost model quality because similar candidates are already trained.

We propose an improved exploration module that considers diversity-aware search to improve the training efficiency of the cost model (Figure 13). The proposed exploration
module creates two mutant candidates from one previous candidate. Then select half of the entire mutant candidates considering the configuration diversity. The selected mutant candidates compete with previous candidates, improving the quality of the competition. The proposed diversity-aware selection has a positive effect both on the diversity of candidates pool and diversity exploration through mutations. A slight tuning performance improvement was obtained through this method.

4. Experiments

4.1. Experimental Settings

We performed AutoTVM searches to find the best configuration for the 3x3 spatial feature extraction convolution of each stage of ResNet50. The search space consists of the following six knobs: BLK-ROW-WARPS, BLK-COL-WARPS, WARP-ROW-TILES, WARP-COL-TILES, CHUNK, and REORDER-INNER. BLK-ROW-WARPS and BLK-COL-WARPS refer to the number of warps for M and N dimensions in a single thread block, and similarly, WARP-ROW-TILES and WARP-COL-TILES refer to the number of WMMA tiles for M, N dimensions in a single warp. CHUNK is the loop split factor for input channel accumulation, and REORDER-INNER determines the order between the outer loop of the input channel and the kernel height loop. We searched the best configuration through 500 trials for each convolution, using AutoTVM on the NVIDIA T4 GPU.

Most simulated annealing algorithm settings are the same as previous AutoTVM default settings. The number of iterations of simulated annealing is 500 and stops iteration if the optimal set does not change in 50 rounds. We use the cost-model prediction score as an energy function of the simulated annealing algorithm. The temperature of the algorithm starts from 1 and cooling down 0.002 every iteration. The simulated annealing algorithm picks 128 candidates every iteration and passes them to the next iteration. At the last Exploration module pick, top-31 configurations from the candidates and one random configuration are added, and those 32 configurations are measured on real hardware. The exploration module only picks candidates that have not been measured before. If there are less than 31 new candidates, randomly generated configurations fill in the rest.

4.2. Schedule Search on ResNet50

Target convolutions are 3x3 convolutions of each residual block in ResNet50. Stage means a section in which residual blocks of the exact specification are repeated. For instance, stage2 means a residual block with a feature map size of 56x56. And in the next stage, the feature map size is halved, and the channel depth is doubled; therefore, the number of operations remains the same. We used two methods for the search: AutoTVM and exhaustive manual search. As a result, automatic-searched performance is faster or similar because AutoTVM measures many configurations faster than manual search. Baseline is the performance of TVM implementation of GitHub’s main branch. This result was also evaluated by finding the optimal configuration with AutoTVM. As shown in Table 1, our searched configurations achieve 2.8x to 3.85x speed-up compared to the baseline for all convolutions.

4.3. Diversity-Aware Search

Due to the implementation issue, here we conducted the experiments with the search space of the original AutoTVM. We evaluated the proposed diversity-aware exploration module with AutoTVM’s search space. Target convolution is 3x3 convolution of ResNet50 stage 2. Figure 14 shows the diversity-aware search method finds better performance configuration in the same trial.

4.4. Ablation Study

Figure 15 depicts accumulated speedup as gradually applying our improvements from the baseline on each convolution. The baseline on each convolution selects the execution schedule with fairly effective performance. Similar to Table 1, the figure shows that convolution with a larger height

| Stage | 2 | 3 | 4 | 5 |
|-------|---|---|---|---|
| OPs   | 1849688064 | 196.06 | 180.96 | 203.62 | 198.62 |
| Baseline (us) | 50.78 | 51.42 | 57.18 | 86.37 |
| Exhaustive (us) | 50.98 | 50.46 | 55.58 | 70.98 |
| Speed-up | 3.85x | 3.59x | 3.66x | 2.80x |

Table 1. Performance of 3x3 convolutions in ResNet50 executed with the searched configurations.
5. Related Work

There have been numerous studies to accomplish efficient Tensor Core computations. Some studies (Kim et al., 2020) tackle this challenge by providing microarchitectural supports to remove redundant memory accesses (Kim et al., 2020) or to handle sparsity in neural networks with indexing in the register file (Zhu et al., 2019). (Zhu et al., 2019) have also suggested efficient implementation of sparse operations that can hardly obtain performance gain on GPUs due to their irregularity of data layout. Since no algorithm other than GEMM utilizes Tensor Cores, optimizations for non-GEMM algorithms such as reduction and scan have been investigated as well (Navarro et al., 2020). Although Tensor Cores can boost the performance of MMA operations by an order of magnitude, optimizing for them is very challenging due to the fixed WMMA size and complicated memory hierarchy. Furthermore, experts have to spend tens to hundreds of hours to manually tune their kernel implementations on GPUs. In order to solve this problem, Bhaskaracharya et al. (2020) has developed automatic kernel generation using polyhedral techniques and implemented an efficient matrix multiplication kernel using the mma.m8n8k4 PTX instruction on a Volta GPU.

While various algorithms have been designed for Tensor Cores, there are limited researches on the optimization approaches to utilize reduced precision MMA on Tensor Cores. Liu et al. (2021), Sorna et al. (2018), Yan et al. (2020) use reduced precision to achieve faster speed and energy saving for their algorithms. However, only half-precision is used in these works and lower bit-precision types provided by Tensor Cores such as INT8 or INT4 are not investigated. Yao et al. (2021) proposes to use uniform and mixed-precision INT4/8 quantization for integer-only inference without any floating point operations. It also solves an integer linear programming problem to find the best bit-precision setting. Feng et al. (2021) introduces a framework to support arbitrary precision neural networks with INT1 compute primitives on Tensor Core.

Tensor programs can have numbers of implementations that are logically equivalent but differ significantly in performance because there can be various optimization strategies considering hardware factors such as data locality and pipelining. In order to efficiently explore the wide search space, AutoTVM (Chen et al., 2018) presents a statistical cost model and accelerate the process using transfer learning. However, writing templates used for AutoTVM requires a huge effort, so Ansor (Zheng et al., 2020) generates the search space automatically without manually developed templates and tune a program using evolutionary search. There also exists an approach for automatically learning a performance model for Tensor Processing Unit (TPU) (Kaufman et al., 2021).

6. Conclusion

In this work, we propose an automatic scheduling method of reduced-precision MMA for convolution operation. In this method, we devise a search space that explores the binding options for maximizing utilization of reduced-precision instructions of Tensor Cores. The search space also includes register-level data packing and layout optimization options, which is particularly beneficial for reducing the overhead of handling reduced-precision data. We further propose a search algorithm by learning from the distinctive candi-
Finally, this reduced-precision MMA optimization method is evaluated on convolution operations of popular neural networks with superior performance compared to the state-of-the-art.

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