Modulation of the high mobility two-dimensional electrons in Si/SiGe using atomic-layer-deposited gate dielectric

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Metal-oxide-semiconductor field-effect transistors (MOSFET’s) using atomic-layer-deposited (ALD) Al₂O₃ as the gate dielectric are fabricated on the Si/Si₁₋ₓGeₙ heterostructures. The low-temperature carrier density of a two-dimensional electron system (2DES) in the strained Si quantum well can be controllably tuned from 2.5×10¹¹ cm⁻² to 4.5×10¹¹ cm⁻² virtually without any gate leakage current. Magnetotransport data show the homogeneous depletion of 2DES under gate biases. The characteristic of vertical modulation using ALD dielectric is shown to be better than that using Schottky barrier or the SiO₂ dielectric formed by plasma-enhanced chemical-vapor-deposition (PECVD).

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Atomic layer deposition (ALD) is a surface controlled layer-by-layer process for the deposition of thin films with atomic layer accuracy. A variety of ALD oxides, such as Al₂O₃, has been intensively studied as high-k gate dielectrics for microelectronic device applications. Similar to SiO₂ and Si₃N₄, Al₂O₃ can significantly reduce the gate leakage current of metal-oxide-semiconductor field-effect-transistors (MOSFET’s). Al₂O₃ offers additional advantages of a large band gap (9eV), high dielectric constant (k=8.6-10), high breakdown field (10⁷V/cm), and thermal stability (amorphous up to at least 1000°C). Furthermore, it can be easily removed by wet-etching and is robust against interfacial reactions and moisture absorption. On the other hand, the research of ALD Al₂O₃ as the gate dielectric on high mobility two-dimensional electron system (2DES) has been sparse. A device using the ALD Al₂O₃ as gate dielectric, taking full advantage of its high permittivity, low defect density, high uniformity, conformal step coverage and moderate growth conditions, can be expected to cause least degradation on the quality of the 2DES and provide physical conditions to study yet unexplored low-temperature 2D electronic phenomena. Therefore, work combining ALD and high mobility 2DES would fill the existing gap in ALD applications between basic physics research and state-of-the-art microelectronic device research.

Among the various high mobility 2DES’s, the system of electrons confined to the strained Si quantum well in the Si/SiGe heterostructure has emerged as a promising system for the study of 2D electronic physics due to its increasing sample quality. Very high electron mobility (≈500,000 cm²/Vs) was reported in this system and strong electron-electron interaction physics phenomena, such as the fractional quantum Hall effect (FQHE) and the 2D metal-insulator transition (MIT), have been observed. However, the vertical modulation on high mobility n-type Si/SiGe proves to be a formidable task due to the difficulty of fabricating a functional field-effect transistor on the heterostructure material. Schottky gate suffers large gate leakage current and only a limited density tuning range can be achieved. At first glance, SiO₂ is the best choice for the gate dielectric. Unfortunately, conventional high temperature oxidation is not amenable to grow SiO₂ on modulation doped heterostructures, which are grown at much lower temperatures. Low temperature plasma-enhanced chemical-vapor-deposition (PECVD) grown SiO₂ has relative poor quality, i.e., a large amount of traps in bulk SiO₂ and at the SiO₂/Si interface, compared to thermally oxidized SiO₂. In a previous study, a layer of PECVD oxide with thickness less than 100nm cannot prevent a leakage path from the gate to the 2D plane. The low quality of this dielectric, mainly due to the large amount of charged traps inside the SiO₂, results in a slow response of the 2DES to the gate bias. As a result, a new gate dielectric material with better electrical properties is needed to modulate the high mobility 2DES in the strained Si quantum well.

In this letter, we report a novel Si/SiGe FET structure using 100nm ALD Al₂O₃ as the gate dielectric. The low-temperature magnetotransport data show that the 2D carrier density n can be homogeneously depleted from ~ 4.0 × 10¹¹ cm⁻² to below 2.5 × 10¹¹ cm⁻² with a few volts of gate bias (V_G) and virtually zero gate leakage current (I_leak). The observed instantaneous response of the 2DES to the change of V_G at T = 0.3K and a linear n vs. V_G relation manifests the high quality of the ALD dielectric. Results from similar FET structures using either Pd Schottky gate or the PECVD SiO₂ as the gate oxide are listed for comparison and the advantage of employing ALD Al₂O₃ as a gate dielectric is demonstrated.

Figure 1 shows the device structure of the fabricated
n-Si/SiGe MOSFET. The starting material (with an as-grown electron density \( n = 4.4 \times 10^{11} \text{cm}^{-2} \) and mobility \( \mu = 8.0 \times 10^{4} \text{cm}^2/\text{Vs} \)) is a modulation doped n-type Si/Si\(_{1-x}\)Ge\(_x\) heterostructure grown by molecular-beam epitaxy (MBE). On top of the 100nm Si buffer grown on a p-Si substrate, the relaxed SiGe buffer is realized by a graded layer of 0.5\( \mu \)m Si\(_{1-x}\)Ge\(_x\), with the Ge mole fraction \( x \) varying from 0 to 0.27. A layer of 2.5\( \mu \)m Si\(_{0.75}\)Ge\(_{0.25}\) is then grown, followed by a 15nm strained Si channel, a 12nm intrinsic Si\(_{0.75}\)Ge\(_{0.25}\) spacer, a 20nm doping layer, a 45nm Si\(_{0.75}\)Ge\(_{0.25}\), and a 10nm Si cap layer. After etched into a 100\( \mu \)m×320\( \mu \)m Hall bar, the sample was transferred \textit{ex situ} to an ASM Pulsar2000\textsuperscript{TM} ALD module. A 100nm-thick Al\(_2\)O\(_3\) layer was deposited at a substrate temperature of 300°C. The oxide on the contact regions was removed by diluted HF and Ohmic contacts were formed by thermal evaporation of 1\% Sb doped Au and 370°C anneal in a forming-gas ambient. The front gate was then formed by thermal evaporation of a Cr/Au layer and lift-off process. After FET fabrication, the sample density and mobility were degraded to \( n = 3.9 \times 10^{11} \text{cm}^{-2} \) and \( \mu = 5.7 \times 10^{4} \text{cm}^2/\text{Vs} \) at zero gate bias. The sample was mounted in a pumped He\(_3\) refrigerator at the base temperature of \( T = 0.3 \)K. Standard low-frequency (\( \sim 7 \)Hz) lock-in techniques were employed to measure the diagonal resistivity \( \rho_{xx} \) and the Hall resistance \( \rho_{xy} \). A low excitation current, 10nA, was used throughout the experiments.

Figure 2 shows a low temperature magnetotransport trace taken at \( V_G = -1.0 \)V (\( n = 3.4 \times 10^{11} \text{cm}^{-2} \) and \( \mu = 2.5 \times 10^{4} \text{cm}^2/\text{Vs} \)). The appearance of integer quantum Hall states at Landau level filling factors \( \nu = 2, 4, 6, 8 \ldots \) as both minima in \( \rho_{xx} \) and plateaus in \( \rho_{xy} \) demonstrates the high quality of the 2DES under gating. The fact that \( \nu \) changes by an even number is due to the remaining two-fold valley degeneracy in the strained Si system, with a valley-valley splitting too small to be resolved here in the presence of disorder broadening.

Figure 3 illustrates the excellent performance of the ALD Al\(_2\)O\(_3\) as a gate dielectric. As the gate voltage is swept from -2.5V to 2.5V, virtually no leakage current is detected and no hysteresis for up and down gate sweeps. However, when the 2DES was depleted into the insulating regime (for \( V < -2.5 \)V and \( \rho \geq \hbar/e^2 \)), hysteresis in gate sweep was seen, presumably due to the breakdown of screening. More remarkably, as shown in the inset of Figure 3, the 2DES responses to the applied \( V_G \) instantaneously and \( \rho \) stays constant as the gate bias stops sweeping, in sharp contrast to the case with low-quality PECVD SiO\(_2\) as the gate dielectric\[3]\.

To further compare the property of ALD dielectric to that of other gating materials on Si/SiGe, samples with either a Pd Schottky gate or a PECVD SiO\(_2\) gate di-
electric (deposited at 250°C) were fabricated. Figure 4 shows the \( n \) vs. \( V_G \) relation for the three different gating schemes, in which the carrier densities are determined by both the quantum oscillations of \( \rho_{xx} \) and the low field Hall slopes at 0.3K. As shown in Figure 4a, the carrier density in the ALD sample can be depleted from \( 4.1 \times 10^{11} \text{cm}^{-2} \) to below \( 2.5 \times 10^{11} \text{cm}^{-2} \) as a linear function of the applied gate voltage. A slope as high as \( 0.6 \times 10^{13} \text{cm}^{-2}/\text{V} \) is extracted in the linear region, even though the device had not received special surface cleaning before the ALD growth or post-growth oxide annealing as in the standard ALD MOSFET process. Further experiments are needed in order to understand the interface property between the Si and the ALD Al\(_2\)O\(_3\), and it is expected that devices with improved interfaces will bring the capacitance closer to the slope expected of an ideal parallel-plate capacitor – in this case, \( 2.8 \times 10^{11} \text{cm}^{-2}/\text{V} \). When the device operates in the accumulation regime with \( V_G > 0 \text{V} \), the data deviate from the linear \( n \) vs. \( V_G \) relation observed for \( V_G \leq 0 \text{V} \). This deviation is probably due to the accumulation of charges in the Si cap layer. For the Pd Schottky gate (Figure 4b), a gate leakage current in the order of 100pA is detected when \( V_G < -0.7 \text{V} \) and the density can only be reduced to about \( 3.0 \times 10^{11} \text{cm}^{-2} \). The data shown in Figure 4c were taken from a similarly fabricated device structure, where a 150nm PECVD SiO\(_2\) layer was deposited as the gate dielectric instead of 100nm ALD Al\(_2\)O\(_3\). Although the gate leakage current is negligible and the 2D density modulation could also be achieved, the gate oxide shows an inferior characteristic compared to the ALD Al\(_2\)O\(_3\). First, a gate bias voltage as high as \( \pm 20 \text{V} \) is needed to tune the similar density range, presumably due to the thicker gate oxide, the lower dielectric constant for SiO\(_2\) (\( \varepsilon_{\text{SiO2}}/\varepsilon_{\text{ALD3}} = 0.39 \)) and much higher trap density in bulk SiO\(_2\) and at the interface. Second, the \( n \) vs. \( V_G \) relation is highly nonlinear even in the depletion side, especially for \(-10 \text{V} < V_G < 0 \text{V} \). A possible origin of this nonlinearity in gate performance is the traps inside the PECVD oxide and at the interface, which screens the electric field from the metallic gate to the 2D plane.

In summary, we have demonstrated a working field-effect transistor using ALD Al\(_2\)O\(_3\) as gate dielectric on a Si/SiGe heterostructure. The electron density in the strained Si quantum well can be tuned linearly and instantaneously by applying a gate voltage. Neither leakage current nor hysteresis for up and down gate sweeps was observed. Similar FET structures using the Schottky barrier or the gate dielectric formed by PECVD SiO\(_2\) are also discussed for comparison and the ALD sample shows the best performance. The experimental technique described above opens up a way to implement ALD oxide as gate dielectrics on high mobility modulation doped heterostructures and to explore 2D physics in previously inaccessible regimes.

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c) Pd Schottky gate

FIG. 4: Carrier density \( n \) vs. \( V_G \) for (a) the 100nm ALD Al\(_2\)O\(_3\) gate, (b) the Pd Schottky gate, and (c) the 150nm PECVD SiO\(_2\) gate. Straight lines are linear fits to the measured data in the depletion region.

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