Effectively Prefetching Remote Memory with Leap

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ABSTRACT
Memory disaggregation over RDMA can improve the performance of memory-constrained applications by replacing disk swapping with remote memory accesses. However, state-of-the-art memory disaggregation solutions still use data path components designed for slow disks. As a result, applications experience remote memory access latency significantly higher than that of the underlying low-latency network, which itself is too high for many applications.

In this paper, we propose Leap, a prefetching solution for remote memory accesses due to memory disaggregation. At its core, Leap employs an online, majority-based prefetching algorithm, which increases the page cache hit rate. We complement it with a lightweight and efficient data path in the kernel that isolates each application’s data path to the disaggregated memory and mitigates latency bottlenecks arising from legacy throughput-optimizing operations. Integration of Leap in the Linux kernel improves the median and tail remote page access latencies of memory-bound applications by up to 104.04× and 22.62×, respectively, over the default data path. This leads to up to 10.16× performance improvements for applications using disaggregated memory in comparison to the state-of-the-art solutions.

1 INTRODUCTION
Modern data-intensive applications [5, 28, 29, 70] experience significant performance loss when their complete working sets do not fit into the main memory. At the same time, despite significant and disproportionate memory underutilization in large clusters [62, 78], memory cannot be accessed beyond machine boundaries. Such unused, stranded memory can be leveraged by forming a cluster-wide logical memory pool via memory disaggregation, improving application-level performance and overall cluster resource utilization [10, 44, 48].

Two broad avenues have emerged in recent years to expose remote memory to memory-intensive applications. The first requires redesigning applications from the ground up using RDMA primitives [14, 20, 35, 49, 59, 77]. Despite its efficiency, rewriting applications can be cumbersome and may not even be possible for many applications [9]. Alternatives rely on well-known abstractions to expose remote memory; e.g., distributed virtual file system (VFS) for remote file access [9] and distributed virtual memory management (VMM) for remote memory paging [27, 31, 44, 45, 65].

Because disaggregated remote memory is slower, keeping hot pages in the faster local memory ensures better performance. Colder pages are moved to the far/remote memory as needed [8, 31, 44]. Subsequent accesses to those cold pages go through a slow data path inside the kernel – for instance, our measurements show that an average 4KB remote page access takes close to 40 µs in existing memory disaggregation systems. Such high access latency significantly affects performance because memory-intensive applications can tolerate at most single µs latency [27, 44]. Note that the latency of existing systems is many times more than the 4.3 µs average latency of a 4KB RDMA operation, which itself is too high for some applications.

In this paper, we take the following position: an ideal solution should minimize remote memory accesses in its critical path as much as possible. In this case, a local cache can reduce the total number of remote memory accesses – a cache hit results in a sub-µs latency, comparable to that of a local page access. An effective prefetcher can proactively bring in correct pages into the cache and increase the cache hit rate.

Unfortunately, existing prefetching algorithms fall short for several reasons. First, they are designed to reduce disk access latency by prefetching sequential disk pages in large batches. Second, they cannot distinguish accesses from different applications. Finally, they cannot quickly adapt to temporal changes in page access patterns within the same process. As a result, being optimistic, they pollute the cache area with unnecessary pages. At the same time, due to their rigid pattern detection technique, they often fail to prefetch the required pages into the cache before they are accessed.

In this paper, we propose Leap, an online prefetching solution that minimizes the total number of remote memory accesses in the critical path. Unlike existing prefetching algorithms that rely on strict pattern detection, Leap works with an approximate mechanism. Specifically, it builds on the Boyer-Moore majority vote algorithm [16] to efficiently identify remote memory access patterns for each individual process. Relying on an approximate mechanism instead of looking for trends in strictly consecutive accesses makes Leap resilient to short-term irregularities in access patterns (e.g., due to multi-threading). It also allows Leap to perform well by detecting trends only from remote page accesses instead of tracing the full virtual memory footprint of an
application, which demands continuous scanning and logging of the hardware access bits of the whole virtual address space and results in high CPU and memory overhead. In addition to identifying the majority access pattern, Leap determines how many pages to prefetch following that pattern to minimize cache pollution.

While reducing cache pollution and increasing the cache hit rate, Leap also ensures that the host machine faces minimal memory pressure due to the prefetched cache. To move pages from local to remote memory, the kernel needs to scan through the entire cache to find eviction candidates—the more pages it has, the more time it takes to scan. As a result, memory allocation time for new pages increases. Therefore, alongside a background LRU-based asynchronous cache eviction policy, Leap eagerly frees up a cache entry just after it gets hit and reduces the page allocation wait time.

We complement our algorithm with an efficient data path design for remote memory accesses that is used in case of a cache miss. It isolates per-application remote traffic and cuts inessentials in the end-host software stack (e.g., the block layer) to reduce host-side latency and handle a cache miss with latency close to that of the underlying RDMA operations.

We make the following contributions in this paper:

- We analyze the root causes behind data path latency overheads for disaggregated memory systems. We then propose Leap, a novel online prefetching algorithm and an eager prefetch cache eviction policy along with a leaner data path, to improve remote I/O performance.
- We implement Leap on Linux Kernel 4.4.125 as a separate data path for remote memory access. Applications can choose either Linux’s default data path for traditional usage or Leap for going beyond the machine’s boundary using unmodified Linux ABIs.
- We evaluate Leap’s prefetching algorithm against practical real-time prefetching algorithms (Next-K Line, Stride, Linux Read-ahead) and show that the prefetcher itself improves application-level performance by 1.75–3.36× with an improved prefetch coverage of 3.06–37.51%. Leap’s prefetching technique also reduces cache pollution and cache miss by 1.28–1.62× and 1.74–10.47×, respectively. Depending on the memory access pattern, simply replacing the default Linux prefetcher with Leap’s prefetcher can provide application-level performance benefit even when they are paging to slower storage (e.g., HDD, SSD).
- In comparison to the Linux data path, Leap improves the median and tail latency of VMM disaggregation framework (e.g., Infiniswap [31] or LegoOS [65]) by up to 104.04× and 22.06×, respectively. For VFS disaggregation solutions (e.g., Remote Regions [9]), Leap also improves the 4KB page access latency characteristics by 24.96× at the median and 17.32× at the 99th percentile. Due its faster data path, Leap provides with application-level performance improvements of 1.27–10.16× for multiple unmodified memory-intensive applications: PowerGraph, NumPy, VoltDB, and Memcached with production workloads.

2 BACKGROUND AND MOTIVATION

2.1 Remote Memory

In memory disaggregation systems, unused cluster memory is logically exposed as a global memory pool that is used as the slower memory for machines with extreme memory demands. This improves the performance of memory-intensive applications that have to frequently access slower memory in memory-constrained settings. At the same time, the overall cluster memory usage gets balanced across the machines, decreasing the need for memory over-provisioning per machine.

Access to remote memory over RDMA without significant application rewrites typically relies on two primary mechanisms: disaggregated VFS [9], that exposes remote memory as files and disaggregated VMM for remote memory paging [31, 44, 65]. In both cases, data is communicated in small chunks or pages. In case of remote memory as files, pages go through the file system before they are written to/read from the remote memory. For remote memory paging and distributed OS, page faults cause the virtual memory manager to write pages to and read them from the remote memory.

2.2 Remote Memory Data Path

State-of-the-art memory disaggregation frameworks depend on the existing kernel data path that is optimized for slow disks. Figure 1 depicts the major stages in the life cycle of

Figure 1: High-level life cycle of page requests in Linux data path along with the average time spent in each stage.
a page request. Due to slow disk access times – average latencies for HDDs and SSDs range between 4–5 ms and 80–160 µs, respectively – frequent disk accesses have severe impact on application throughput and latency. Although the recent rise of memory disaggregation is fueled by the hope that RDMA can consistently provide single µs 4KB page access latency [10, 27, 31], this is often a wishful thinking in practice [79]. Blocking on a page access – be it from HDD, SSD, or remote memory – is often unacceptable.

To avoid blocking on I/O, race conditions, and synchronization issues (e.g., accessing a page while the page out process is still in progress), the kernel uses a page cache. To access a page from slower memory, it is first looked up in the appropriate cache location; a hit results in almost memory-speed page access latency. However, when the page is not found in the cache (i.e., a miss), it is accessed through a costly block device I/O operation that includes several queuing and batching stages to optimize disk throughput. As a result, a cache miss leads to more than 100× slower latency than a hit; it also introduces high latency variations.

2.3 Prefetching in Linux

The Linux kernel tries to store files on the disk in adjacent sectors to increase sequential disk accesses. The same happens for paging. Naturally, existing prefetching mechanisms are designed assuming sequential data layout. The default Linux prefetcher relies on the last two page faults: if they are for consecutive pages, it brings in several sequential pages into the page cache; otherwise, it assumes that there are no patterns and reduces or stops prefetching. This has several drawbacks. First, whenever it observes two consecutive paging requests for consecutive pages, it over-optimistically brings in pages that may not even be useful. As a result, it wastes I/O bandwidth and causes cache pollution by occupying valuable cache space. Second, simply assuming the absence of any pattern based on last two requests is over-pessimistic. Furthermore, all the applications share the same swap space in Linux; hence, pages from two different processes can share consecutive places in the swap area. An application can also have multiple, inter-leaved stride patterns – for example, due to multiple concurrent threads. Overall, considering only last two requests to prefetch a batch of future pages falter on both respects.

To illustrate this, we measure the page access latency for two memory access patterns: (a) Sequential accesses memory pages sequentially; and (b) Stride-10 accesses memory in strides of 10 pages. In both cases, we use a simple application with its working set size set to 2GB. For disaggregated VMM, it is provided 1GB memory to ensure that 50% of its access cause paging. For disaggregated VFS, it performs 1GB remote write and then another 1GB remote read operations.

Figure 2 shows the latency distributions for 4KB page accesses from disk and disaggregated remote memory for both of the access patterns. For a prefetch size of 8 pages, both perform well for the Sequential pattern; this is because 80% of the requests hit the cache. In contrast, we observe significantly higher latency in the Stride-10 case because all the requests miss the page cache due to the lack of consecutiveness in successive page accesses. By analyzing the latency breakdown inside the data path for Stride-10 (as shown in Figure 1), we make two key observations. First, although RDMA can provide significantly lower latency than disk (4.3µs vs. 91.5µs), RDMA-based solutions do not benefit as much from that (38.3µs vs. 125.5µs). This is because of the significant data path overhead (on average 34µs) to prepare and batch a request before dispatching it. Significant variations in the preparation and batching stages of the data path cause the average to stray far from the median. Second, existing sequential data layout-based prefetching mechanism fails to serve the purpose in the presence of diverse remote page access pattern. Solutions based on fixed stride sizes also fall short because stride sizes can vary over time within the same application. Besides, there can be more complicated patterns beyond stride or no repetitions at all.

Shortcoming of Strict Pattern Finding for Prefetching. Figure 3 presents the remote page access patterns of four memory-intensive applications during page faults when they are run with 50% of their working sets in memory (more details in Section 5.3). Specifically, we consider all page-fault sequences of size \( X \in \{2, 4, 8\} \) in these applications and divide them into three categories: sequential when all \( X \) are sequential pages, stride when all \( X \) have the same stride from the first page, and other when it is neither sequential nor stride.
3 REMOTE MEMORY PREFETCHING

In this section, we first highlight the characteristics of an ideal prefetcher. Next, we present our proposed online prefetcher along with its different components and the design principles behind them. Finally, we discuss the complexity and correctness of our algorithm.

3.1 Properties of an Ideal Prefetcher

A prefetcher’s effectiveness is measured along three axes:
- **Accuracy** refers to the ratio of total cache hits and the total pages added to the cache via prefetching.
- **Coverage** measures the ratio of total cache hits from the prefetched pages and the total number of requests (e.g., page faults in case of remote memory paging solutions).
- **Timeliness** of an accurately prefetched page is the time gap from when it was prefetched to when it was first hit.

**Trade-off.** An aggressive prefetcher can hide the slower memory access latency by bringing pages well ahead of the access requests. This might increase the accuracy, but as prefetched pages wait longer to get consumed, this wastes the effective cache and I/O bandwidth. On the other hand, a conservative prefetcher has lower prefetch consumption time and reduces cache and bandwidth contention. However, it has lower coverage and cannot hide memory access latency completely. An effective prefetcher must balance all three.

An effective prefetcher must be adaptive to temporal changes in memory access patterns as well. When there is a predictable access pattern, it should bring pages aggressively. In contrast, during irregular accesses, prefetch rate should be throttled down to avoid cache pollution.

Prefetching algorithms use prior page access information to predict future access patterns. As such, their effectiveness largely depends on how well they can detect patterns and predict. A real-time prefetcher has to face a tradeoff between pattern identification accuracy vs. computational complexity.
and resource overhead. High CPU usage and memory consumption will negatively impact application performance even though they may help in increasing accuracy.

**Common Prefetching Techniques.** The most common and simple form of prefetching is spatial pattern detection [51]. Some specific access patterns (i.e., stride, stream etc.) can be detected with the help of special hardware features [32, 34, 66, 80]. However, they are typically applied to identify patterns in instruction access that are more regular; in contrast, data access patterns are more irregular. Special prefetch instructions can also be injected into an application’s source code, based on compiler or post-execution based analysis [26, 39, 40, 60, 61]. However, compiler-injected prefetching needs static analysis of the cache miss behavior before the application runs. Hence, they are not adaptive to dynamic cache behavior. Finally, usage of these hardware- or software-dependent prefetching techniques are limited to the availability of the special hardware/software features and/or application modification.

**Summary.** An ideal prefetcher should have low computational and memory overhead. It should have high accuracy, coverage, and timeliness to reduce cache pollution; an adaptive prefetch window is imperative to fulfill this requirement. It should also be flexible to both spatial and temporal locality in memory accesses. Finally, hardware/software independence and application transparency make it more generic and robust.

Table 1 compares different prefetching methods.

### 3.2 Majority Trend-Based Prefetching

Leap has two main components: detecting trends and determining what to prefetch. The first component looks for any approximate trend in earlier accesses. Based on the trend availability and prefetch utilization information, the latter component decides how many and which pages to prefetch.

#### 3.2.1 Trend Detection

Existing prefetch solutions rely on strict pattern identification mechanisms (e.g., sequential or stride of fixed size) and fail to ignore temporary irregularities. Instead, we consider a relaxed approach that is robust to short-term irregularities. Specifically, we identify the majority $\Delta$ values in a fixed-size ($H_{size}$) window of remote page accesses (AccessHistory) and ignore the rest. For a window of size $w$, a $\Delta$ value is said to be the major only if it appears at least $\lfloor w/2 \rfloor + 1$ times within that window. To find the majority $\Delta$, we use the Boyer-Moore majority vote algorithm [16] (Algorithm 1), a linear-time and constant-memory algorithm, over AccessHistory elements. Given a majority $\Delta$, due to the temporal nature of remote page access events, it can be hypothesized that subsequent $\Delta$ values are more likely to be the same as the majority $\Delta$.

Note that if two pages are accessed together, they will be aged and evicted together in the slower memory space at contiguous or nearby addresses. Consequently, the temporal locality in virtual memory accesses will also be observed in the slower page accesses and an approximate stride should be enough to detect that.

**Window Management.** If a memory access sequence follows a regular trend, then the majority $\Delta$ is likely to be

|       | Low Computational Complexity | Low Memory Overhead | Unmodified Application | HW/SW Independent | Temporal Locality | Spatial Locality | High Prefetch Utilization |
|-------|-----------------------------|---------------------|-----------------------|-------------------|-----------------|-----------------|--------------------------|
| Next-N-Line [52] | ✓                           | ✓                   | ✓                     | ✓                 | X               | ✓               | X                        |
| Stride [13]     | ✓                           | ✓                   | ✓                     | ✓                 | ✓               | ✓               | ✓                        |
| GHB PC [54]     | X                           | X                   | ✓                     | ✓                 | X               | ✓               | ✓                        |
| Instruction Prefetch [26, 40] | X                  | X                   | X                     | X                 | ✓               | ✓               | ✓                        |
| Linux Read-Ahead [72] | ✓                           | ✓                   | ✓                     | ✓                 | ✓               | ✓               | X                        |
| Leap Prefetcher | ✓                           | ✓                   | ✓                     | ✓                 | ✓               | ✓               | ✓                        |

**Table 1: Comparison of prefetching techniques based on different objectives.**

**Algorithm 1 Trend Detection**

1: procedure FINDTREND($N_{split}$)
2: $H_{size} \leftarrow \text{size(AccessHistory)}$
3: $w \leftarrow H_{size}/N_{split}$ ★ Start with small detection window
4: $\Delta_{maj} \leftarrow \emptyset$
5: while true do
6:   $\Delta_{maj} \leftarrow \text{Boyer-Moore on} \{H_{head}, \ldots, H_{head-w-1}\}$
7:   $w \leftarrow w * 2$
8:   if $\Delta_{maj} \neq \text{major trend}$ then
9:     $\Delta_{maj} \leftarrow \emptyset$
10: if $\Delta_{maj} \neq \emptyset$ or $w > H_{size}$ then
11:   return $\Delta_{maj}$
found in almost any part of that sequence. In that case, a smaller window can be more effective as it reduces the total number of operations. So instead of considering the entire AccessHistory, we start with a smaller window that starts from the head position \((H_{head})\) of AccessHistory. For a window of size \(w\), we find the major \(\Delta\) appearing in \(H_{head}, H_{head-1}, \ldots, H_{head-w-1}\) elements.

However, in the presence of short-term irregularities, small windows may not detect a majority. To address this, the prefetcher starts with a small detection window and doubles the window size up to AccessHistory size until it finds a majority; otherwise, it determines the absense of a majority. The smallest window size can be controlled by \(N_{split}\).

**Example.** Let us consider a AccessHistory with \(H_{size} = 8\) and \(N_{split} = 2\). Say pages with the following addresses: 0x48, 0x45, 0x42, 0x3F, 0x3C, 0x02, 0x04, 0x06, 0x08, 0x0A, 0x0C, 0x10, 0x12, 0x14, 0x16 were requested in that order. Figure 5 shows the corresponding \(\Delta\) values stored in AccessHistory, with \(t_0\) being the earliest and \(t_{15}\) being the latest request. At \(t_6\), \(H_{head}\) stays at the \(t_1\)-th slot.

**FindTrend** in Algorithm 1 will initially try to detect a trend using a window size of 4. Upon failure, it will look for a trend first within a window size of 8.

At time \(t_3\), **FindTrend** successfully finds a trend of -3 within the \(t_0\)-\(t_3\) window (Figure 5a).

**Algorithm 2** Prefetch Candidate Generation

1. **procedure** GetPrefetchWindowSize(page \(P_i\))
2. \(PW_{size_i} \leftarrow \) Current prefetch window size
3. \(PW_{size_{i-1}} \leftarrow \) Last prefetch window size
4. \(C_{hit} \leftarrow \) Prefetched cache hits after last prefetch
5. if \(C_{hit} = 0\) then
6. if \(P_i\) follows the current trend then
7. \(PW_{size_i} \leftarrow 1\) \(\triangleright\) Prefetch a page along trend
8. else
9. \(PW_{size_i} \leftarrow 0\) \(\triangleright\) Suspend prefetching
10. else \(\triangleright\) Earlier prefetches had hits
11. \(PW_{size_i} \leftarrow \) Round up \(C_{hit} + 1\) to closest power of 2
12. \(PW_{size_i} \leftarrow \min(PW_{size_i}, PW_{size_{max}})\)
13. if \(PW_{size_i} < PW_{size_{i-1}}/2\) then
14. \(PW_{size_i} \leftarrow PW_{size_{i-1}}/2\) \(\triangleright\) Shrink window smoothly
15. \(C_{hits} \leftarrow 0\)
16. \(PW_{size_{i-1}} \leftarrow PW_{size_i}\)
17. return \(PW_{size_i}\)

18. **procedure** DoPrefetch(page \(P_i\))
19. \(PW_{size_i} \leftarrow \) GetPrefetchWindowSize\((P_i)\)
20. if \(PW_{size_i} \neq 0\) then
21. \(\Delta_{maj} \leftarrow FindTrend(N_{split})\)
22. if \(\Delta_{maj} \neq 0\) then
23. Read \(PW_{size_i}\) pages with \(\Delta_{maj}\) stride from \(P_i\)
24. else
25. Read \(PW_{size_i}\) pages around \(P_i\) with latest \(\Delta_{maj}\)
26. else
27. Read only page \(P_i\)

At time \(t_7\), the trend starts to shift from -3 to +2. At that time, \(t_4\)-\(t_7\) window does not have a majority \(\Delta\), which doubles the window to consider \(t_0\)-\(t_7\). This window does not have any majority \(\Delta\) either (Figure 5b). However, at \(t_8\), we will find a majority \(\Delta\) of +2 within \(t_5\)-\(t_8\) window and adapt to the new trend (Figure 5c).

Similarly, at \(t_{15}\), we have a majority of +2 in the \(t_8\)-\(t_{15}\) window, which will continue to the +2 trend found at \(t_8\) while ignoring the short-term variations at \(t_{12}\) and \(t_{13}\) (Figure 5d).

3.2.2 Prefetch Candidate Generation. So far we have focused on identifying the presence of a trend. Algorithm 2 determines whether and how to use that trend for prefetching for a request for page \(P_i\).

We determine the prefetch window size \(PW_{size_i}\) based on the accuracy of prefetches between two consecutive prefetch requests (see GetPrefetchWindowSize). Any cache hit
of the prefetched data between two consecutive prefetch requests indicates the overall effectiveness of the prefetch. In case of high effectiveness (i.e., high cache hit), $PW_{size_i}$ is expanded until it reaches a maximum size ($PW_{size_{max}}$). On the other hand, low cache hit indicates low effectiveness; in that case, the prefetch window size gets reduced. However, in the presence of drastic drops, prefetching is not suspended immediately. The prefetch window is shrunk smoothly to make the algorithm flexible to short-term irregularities. When prefetching is suspended, no extra pages are prefetched until a new trend is detected. This is to avoid cache pollution during irregular/unpredictable accesses.

Given a non-zero $PW_{size}$, the prefetcher brings in $PW_{size}$ pages following the current trend, if any (DoPrefetch). If no majority trend exists, instead of giving up right away, it speculatively brings $PW_{size}$ pages around $P_i$’s offset following the previous trend. This is to ensure that short-term irregularities cannot completely suspend prefetching.

**Prefetching in the Presence of Irregularity.** FindTrend can detect a trend within a window of size $w$ in the presence of at most $\lfloor w/2 \rfloor - 1$ irregularities within it. If the window size is too small or the window has multiple perfectly interleaved threads with different strides, FindTrend will consider it as a random pattern. In that case, if the $PW_{size}$ has a non-zero value then it performs a speculative prefetch (line 25) with the previous $\Delta_{maj}$. If that $\Delta_{maj}$ is one of the interleaved strides, then this speculation will cause cache hit and continue. Otherwise, $PW_{size}$ will eventually be zero and the prefetcher will stop bringing unnecessary pages. In that case, the prefetcher cannot be worse than the existing prefetch algorithms.

### 3.3 Analysis

**Time Complexity.** The FindTrend function in Algorithm 1 initially tries to detect trend aggressively within a smaller window using the Boyer-Moor Majority Voting algorithm. If it fails, then it expands the window size. The Boyer-Moor Majority Voting algorithm (line 6) detects a majority element (if any) in $O(w)$ time, where $w$ is the size of the window. In the worst case, it will invoke the Boyer-Moor Majority Voting algorithm for $O(\log H_{size})$ times. However, as the windows are continuous, searching in a new window does not need to start from the beginning and the algorithm never access the same item twice. Hence, the worst-case time complexity of the FindTrend function is $O(H_{size})$, where $H_{size}$ is the size of the AccessHistory queue. For smaller $H_{size}$, the computational complexity is constant. Even for $H_{size} = 32$, the prefetcher provides significant performance gain (§3) that greatly outweighs the slight extra computational cost.

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**Figure 6: Leap has a faster data path for a cache miss.**

**Memory Complexity.** The Boyer-Moor Majority Voting algorithm operates on constant memory space. FindTrend just invokes the Boyer-Moor Majority Voting algorithm and does not require any additional memory to execute. So, the Trend Detection algorithm needs $O(1)$ space to operate.

**Correctness of Trend Detection.** The correctness of FindTrend depends on that of the Boyer-Moor Majority Voting algorithm, which always provides the majority element, if one exists, in linear time (see [16] for the formal proof).

### 4 SYSTEM DESIGN

We have implemented our prefetching algorithm as a data path replacement for memory disaggregation frameworks (we refer to this design as Leap data path) alongside the traditional data path in Linux kernel v4.4.125. Leap has three primary components: a page access tracker to isolate processes, a majority-based prefetching algorithm, and an eager cache eviction mechanism. All of them work together in the kernel space to provide a faster data path. Figure 6 shows the basic architecture of Leap’s remote memory access mechanism. It takes only around 400 lines of code to implement the page access tracker, prefetcher, and the eager eviction mechanism.

#### 4.1 Page Access Tracker

Leap isolates each process’s page access data paths. The page access tracker monitors page accesses inside the kernel to provide the prefetcher with enough information to detect the page access trend of a specific application. Leap does not monitor in-memory pages (hot pages) because continuously scanning and recording the hardware access bits of a large number of pages causes significant computational overhead and memory consumption. Instead, it monitors only the cache look-ups and records the access sequence of the pages after I/O requests or page faults, trading off small loss in access pattern detection accuracy for low resource overhead. As temporal locality in the virtual memory space results in
spatial locality in the remote address space, just monitoring the remote page accesses is often enough.

The page access tracker is added as a separate control unit inside the kernel. Upon a page fault, during the page-in operation (do_swap_page() under mm/memory.c), we notify (log_access_history()) Leap's page access tracker about the page-fault and the process involved. Leap maintains process-specific fixed-size (Hsize) FIFO AccessHistory circular queues to record the page access history. Instead of recording exact page addresses, however, we only store the difference between two consecutive requests (\( \Delta \)). For example, if page faults happen for addresses 0x2, 0x5, 0x4, 0x6, 0x1, 0x9, then AccessHistory will store the corresponding \( \Delta \) values: 0, +3, -1, +2, -5, +8. This reduces the storage space and computation overhead during trend detection (§3.2.1).

4.2 The Prefetcher

To increase the probability of cache hit, Leap incorporates the majority trend-based prefetching algorithm (§3.2). Here, the prefetcher considers each process's earlier remote page access histories available in the respective AccessHistory to efficiently identify the access behavior of different processes. Because threads of the same process share memory with each other, we choose process-level detection over thread-based. Thread-based pattern detection may result in requesting the same page for prefetch multiple times for different threads.

Two consecutive page access requests are temporally correlated in the sense that they may happen together in the future. The \( \Delta \) values stored in the AccessHistory records the spatial locality in the temporally correlated page accesses. Therefore, the prefetcher utilizes both temporal and spatial localities of page accesses to predict future page demand.

The prefetcher is also added as a separate control unit inside the kernel. While paging-in, instead of going through the default swapin_readahead(), we re-route it through the prefetcher's do_prefetch() function. Whenever the prefetcher decides the set of pages which can be accessed in future, Leap bypasses the expensive request scheduling and batching operations of the block layer (swap_readpage()/swap_writepage() for paging and generic_file_read()/generic_file_write() for the file systems) and invokes leap_remote_io_request() to re-direct the request through Leap's asynchronous remote I/O interface over RDMA (§4.4).

4.3 Eager Cache Eviction

Leap maintains a circular linked list of prefetched caches (PrefetchFifoLruList). Whenever a page is fetched from the remote memory, besides the kernel's global LRU lists, Leap adds it at the tail of the PrefetchFifoLruList. After the prefetch cache gets hit and the page table is updated, Leap instantaneously frees the page cache and removes it from the PrefetchFifoLruList. As an accurate prefetcher is timely in using the prefetched data, in Leap, prefetched caches do not wait long in the PrefetchFifoLruList to get evicted by the background process. This eager eviction of prefetch caches reduces the scan time to select eviction candidates. As a result, the wait time to find and allocate new pages also reduces - on average, page allocation time is reduced by 750ns (36% less than the usual). Thus, new pages can be brought to the memory more quickly leading to a reduction in the overall data path latency.

However, if the prefetched pages need to be evicted even before they get consumed (e.g., at severe global memory pressure or extreme constrained prefetch cache size scenario), due to the lack of any access history, prefetched pages will follow a FIFO eviction order among themselves from the PrefetchFifoLruList. Reclamation of other memory (file-backed or anonymous page) follows the existing LRU eviction policy in kernel. We modify the kernel's Memory Management Unit (mm/swap_state.c) to add the prefetch eviction related functions.

Except for the above mentioned re-directions or modifications, we do not modify any other existing kernel functions.

4.4 Remote I/O Interface

Similar to existing works [9, 31], Leap uses an agent in each host machine to expose a remote I/O interface to the VFS/VMM over RDMA. The host machine's agent communicates to another remote agent with its resource demand and performs remote memory mapping. The whole remote memory space is logically divided into fixed-size memory slabs. A host agent can map slabs across one or more remote machine(s) according to its resource demand, load balancing, and fault tolerance policies.

The host agent maintains a per CPU core RDMA connection to the remote agent. We use the multi-queue IO queuing mechanism where each CPU core is configured with an individual RDMA dispatch queue for staging remote read/write requests. Upon receiving a remote I/O request, the host generates/retrieves a slot identifier, extracts the remote memory address for the page within that slab, and forwards the request to the RDMA dispatch queue to perform read/write over the RDMA NIC. During the whole process, Leap completely bypasses the expensive block layer operations.

4.5 Resilience, Scalability, and Load Balancing

One can use the existing memory disaggregation frameworks [9, 31, 65] and still have the performance benefits of Leap while maintaining respective scalability and fault tolerance characteristics. We do not claim any innovation here. In
our implementation, the host agent leverages power of two choices [53] to minimize memory imbalance across remote machines, and remote in-memory replication is the default fault tolerance mechanism in Leap.

5 EVALUATION

We have evaluated Leap over a 56 Gbps InfiniBand RDMA network on CloudLab [3]. Our key results are as follows:

- Leap provides a faster data path to remote memory. Latency for 4KB remote page accesses improves by up to 104.04× at the median and 22.06× at the tail in case of Disaggregated VMM. In case of Disaggregated VFS, the latency benefit is up to 24.96× at the median and 17.32× at the tail (§5.1).

- Our prefetching algorithm outperforms its counterparts (Next-K, Stride, and Linux Read-Ahead) by up to 1.62× in terms of cache pollution and up to 10.47× for cache miss. It improves prefetch coverage by up to 37.51%. (§5.2)

- Leap improves end-to-end application completion times of unmodified PowerGraph, NumPy, VoltDB and Mem-Cached by up to 9.84× and their throughput by up to 10.16× over existing memory disaggregation solutions (§5.3).

Methodology. As mentioned earlier, we integrated Leap inside the Linux kernel, both in its VMM and VFS data paths. As a result, we evaluate its impact on three primary mediums.

- Local disks: Here, Linux swaps to a local HDD and SSD.
- Disaggregated VMM (D-VMM): To evaluate Leap’s benefit for disaggregated VMM system, we integrate Leap with the latest commit of Infiniswap on GitHub [4].
- Disaggregated VFS (D-VFS): To evaluate Leap’s benefit for a disaggregated VFS system, we add Leap to Remote Regions [9] that we implemented as it is an open-source.

For both the memory disaggregation systems, we use respective load balancing and fault tolerance mechanism. Unless otherwise specified, we use AccessHistory buffer size $H_{\text{size}} = 32$, and maximum prefetch window size $PW_{\text{size max}} = 8$.

Each machine in our evaluation has 64 GB of DRAM and 2× Intel Xeon E5-2650v2 with 32 virtual cores supporting AVX instructions.

5.1 Microbenchmark

We start by analyzing Leap’s latency characteristics with the two simple access patterns described in Section 2.

During sequential access, due to prefetching, 80% of the total page requests hit the cache in the default mechanism. On the other hand, during stride access, all prefetched pages brought in by the Linux prefetcher are unused and every page access request experience a cache miss.

Due to Leap’s faster data path, for Sequential, it improves the median by 4.07× and 99-th percentile by 5.48× for disaggregated VMM (Figure 7a). For Stride-10, as the prefetcher can detect strides efficiently, Leap performs almost as good as it does during the sequential accesses. As a result, in terms of 4KB page access latency, Leap improves disaggregated VMM by 104.04× at the median and 22.06× at the tail (Figure 7b).

Leap provides similar performance benefit during memory disaggregation through the file abstraction as well. During sequential access, Leap improves 4KB page access latency by 1.99× at the median and 3.42× at the 99th percentile. During stride access, the median and 99th percentile latency improves by 24.96× and 17.32×, respectively.

As the idea of using far/remote memory for storing cold data is getting more popular these days [8, 31, 44], throughout the rest of the evaluation, we focus only on remote paging through a disaggregated VMM system.

5.2 Performance Benefit of the Prefetcher

In this section, we focus on the effectiveness of the prefetcher itself for real-world applications with complex access patterns. We choose the PowerGraph workload because it has significant amount of all three – stride, sequential, and irregular – remote memory access patterns.

We start with dissecting the latency contribution of our prefetcher. Then, we evaluate its efficiency over existing prefetchers. For the latter, we run PowerGraph on disk to separate only the prefetching algorithm’s benefit without any other data path optimizations.

5.2.1 Performance Benefit Breakdown. Figure 8a shows the performance benefit breakdown for each component of Leap data path. For PowerGraph at 50% memory limit, due to data path optimizations, Leap provides with single-digit µs latency for 4KB page accesses up to the 95th percentile. Inclusion of the prefetcher ensures sub-µs 4KB page access latency up to the 85th percentile and improves the 99-th percentile latency by 11.4% over Leap’s optimized data path.
The eager eviction policy reduces the page cache allocation time and improves the tail latency by another 22.2%.

5.2.2 Performance Benefit for Slow Storage. To observe the usefulness of the prefetcher for slow disk access, we incorporate it to Linux’s default data path while paging to disk. Due to the majority based prefetching algorithm, the overall application run time improves by 1.25× and 1.61× over SSD and HDD using the default prefetcher, respectively (Figure 8b).

5.2.3 Prefetch Utilization. Here, we run PowerGraph on disk (with existing block layer based data path) with 50% memory limit and compared the prefetching algorithm with the following practical and realtime prefetching techniques:

- **Next-N-Line Prefetcher** [52] aggressively brings N pages sequentially mapped to the page with the cache miss if they are not in the cache.
- **Stride Prefetcher** [13] brings pages following a stride pattern relative to the current page upon a cache miss. The aggressiveness of this prefetcher depends on the accuracy of the past prefetch.
- **Linux Read-Ahead** prefetches an aligned block of pages containing the faulted page [72]. Linux uses prefetch hit count and an access history of size 2 to control the aggressiveness of the prefetcher.

Impact on the Cache. As the volume of data fetched in cache increases, prefetch hit rate increases. However, thrashing begins as soon as the working set exceeds cache capacity. As a result, useful demand-fetched pages are evicted. Figure 9a shows that Leap’s prefetcher uses 28.15%–62.13% fewer page caches than the other prefetching algorithms.

A successful prefetcher reduces the number of cache misses by bringing the most accurate pages into cache. Leap’s prefetcher has the smallest cache miss: it experiences 7.19×, 10.47×, and 1.736× fewer cache miss events w.r.t. Next-N-Line, Stride, and Read-Ahead, respectively (Figure 9a).

Application Performance. Due to the improvement in cache pollution and reduction of cache miss, using Leap’s prefetcher, PowerGraph experiences the lowest completion time. PowerGraph experiences 2.59×, 3.36×, and 1.75× higher completion time than Leap when using Next-N-Line, Stride, and Read-Ahead, respectively (Figure 9b).

Effectiveness. If a prefetcher brings every possible page in the page cache, then it will be 100% accurate. However, in reality, one cannot have an infinite cache space due to large data volumes and/or multiple applications running on the same machine. Besides, optimistically bringing pages may create cache contention, which reduces overall performance.

Leap’s prefetcher trades off cache pollution with comparatively lower accuracy. Compare to other prefetchers, it shows 0.9–10.88% lower accuracy (Figure 10a). This accuracy loss is linear to the number of cache add done by the prefetchers. As all the other prefetchers bring in lots of pages, their chances of getting lucky hits also increase. Although Leap has the lowest accuracy, its high coverage (3.06–37.51%) (Figure 10a) allows it to serve with accurate prefetches with a lower cache pollution cost. At the same time, it has an improved timeliness (Figure 10b) over Read-Ahead (Next-K-Line) 12.37× (13.9×) at the median and 12.47× (1.52×) at the tail. Due to the higher coverage, better timeliness, and almost similar accuracy, Leap’s prefetcher thus outperforms others in terms of application level performance (Figure 9b). Note that despite...
having the best timeliness, Stride has the worst coverage and completion time that impedes its overall performance.

5.3 Leap’s Overall Impact on Applications

Finally, we evaluate the overall benefit of Leap (including all its components). We use four real-world memory-intensive application and workload combinations with different data access patterns (Figure 3) used in prior works:

- Twitter dataset[43] on PowerGraph[28];
- Matrix multiplication on NumPy[57];
- TPC-C benchmark[7] on VoltDB [70];
- Facebook workloads[12] on Memcached [5]

The peak memory usage of these applications varies from 9 GB to 38.2 GB. Unless otherwise mentioned, we use the same workload and application parameters as in prior works [9, 31]. To prompt remote paging, we limit an application’s memory usage to fit 100%, 50%, 25% of its peak memory usage through cgroups [2], a Linux kernel feature to control and monitor a process’s system resource usage. Here, we considered the extreme memory constrain (e.g., 25%) to validate the applicability of Leap to recent resource (memory) disaggregation frameworks that are expected to operate on minimal amount of local memory [65].

5.3.1 PowerGraph. PowerGraph suffers significantly for cache misses in Infiniswap (Figure 11a). In contrast, Leap experiences more cache hit as its prefetcher can detect 19.03% more remote page access patterns over Read-Ahead. The faster the prefetch cache hit happens, the faster the eager cache eviction mechanism frees up page caches and eventually help in faster page allocations for new prefetch. Besides, due to more accurate prefetching, Leap reduces the wastage in both cache space and RDMA bandwidth. This improves 4KB remote page access time by 8.17x and 2.19x at the 99-th percentile for 50% and 25% cases, respectively. Overall, integration of Leap to Infiniswap improves the completion time by 1.56x and 2.38x at 50% and 25% cases, respectively.

5.3.2 NumPy. We use NumPy to perform a matrix multiplication over two large matrices that is pretty common in any computational application of linear algebra (e.g., machine learning). We load two matrices of non-zero floating points with 100k × 100 and 50k × 100 dimensions from previously stored file and perform matrix dot product on them. Here, the peak memory usage is 38.2 GB.

Leap can detect most of the remote page access patterns (10.4% better than Linux’s default prefetcher). As a result, similar to PowerGraph, for NumPy, Leap improves the completion time by 1.27x and 1.4x for Infiniswap at 50% and 25% memory limit, respectively (Figure 11b). The 4KB page access time improves by 5.28x and 2.88x at the 99-th percentile at 50% and 25% cases, respectively.

5.3.3 VoltDB. Latency-sensitive applications like VoltDB suffers a lot due to the paging overhead. During paging, due to Linux’s slower data path, Infiniswap suffers (65.12% and 95.72% lower throughput than local memory behavior on 50% and 25%, respectively). In contrast, Leap’s better prefetching (11.6% better than Read-Ahead) and instant cache eviction improves the 4KB page access time ~ 2.51x and 2.7× better 99-th percentile at 50% and 25% cases, respectively. However, while executing short random transactions, VoltDB has irregular page access pattern (69% of total remote page accesses). At that time, Leap prefetcher’s adaptive throttling helps the most by not congesting the RDMA. Overall, Leap faces smaller throughput loss (3.78% and 57.97% lower than local memory behavior on 50% and 25% memory limits, respectively). Leap improves Infiniswap’s throughput by 2.76x and 10.16x for 50% and 25% configurations, respectively (Figure 11c).

5.3.4 MemCached. This workload has mostly random remote page access pattern. Leap’s prefetcher can detect most of them and avoids prefetching in the presence of randomness. This results in fewer remote requests and less cache pollution. As a result, Leap provides MemCached with almost the local memory level behavior at 50% memory limit while
the default data path of Infiniswap faces 10.1% throughput loss (Figure 11d). At 25% memory limit, Leap deviates from the local memory throughput behavior by only 1.7%. Here, the default data path of Infiniswap faces 18.49% throughput loss. In this phase, Leap improves Infiniswap’s throughput by 1.11× and 1.21× at 50% and 25% memory limits, respectively. Leap provides with 5.94× and 1.08× better 99-th percentile 4 KB page access time at 50% and 25% cases, respectively.

5.3.5 Performance Under Constrained Cache Size. To observe Leap’s performance benefit in the presence of limited prefetch cache size, we run the four applications in 50% memory limit configuration at different cache limit (Figure 12).

For MemCached, as most of the accesses are of random pattern, most of the performance benefit comes from Leap’s faster slow path. For the rest of the applications, as the prefetcher has better timeliness, most of the prefetched caches get used and evicted before the cache size hits the limit. For this reason, during O(1)MB cache size, all of these applications face minimal performance drop (11.87 – 13.05%) compared to the unlimited cache space scenario. Note that, for NumPy, 3.2MB cache size is only 0.02% of its total remote memory usage.

5.3.6 Multiple Applications Running Together. We run all four applications simultaneously with their 50% memory limit and observe the performance benefit of Leap for Infiniswap when multiple throughput- (PowerGraph, NumPy) and latency-sensitive applications (VoltDB, MemCached) concurrently request for remote memory access (Figure 13). As Leap isolates each application’s page access path, its prefetcher can consider individual access patterns while making prefetch decisions. Therefore, it brings more accurate remote pages for each application and reduces contention over the network. As a result, overall application performance improves by 1.1–2.4× over Infiniswap.

To enable aggregate performance comparison, we present end-to-end completion time of application-workload combinations defined earlier; application-specific metrics improve as well.

6 RELATED WORK

Remote Memory Solutions. A good number of software systems have been proposed over the years to access remote machine’s memory for paging [1, 19, 21, 25, 31, 44, 45, 50, 55, 64, 65], global virtual machine abstraction [6, 24, 42], and distributed data stores and file systems [9, 20, 41, 47, 58]. Hardware-based remote access using PCIe interconnects [48] or extended NUMA memory fabric [56] are also proposed to disaggregate memory. Leap is complementary to these works.

Kernel Data Path Optimizations. With the emergence of faster storage devices, several optimization techniques and design principles have been proposed to fully utilize faster hardware. Considering the overhead of the block layer, different service level optimizations and system re-designs have been proposed – examples include parallelism in batching and queuing mechanism [15, 75], avoiding interrupts and context switching during I/O scheduling [11, 18, 74, 76], better buffer cache management [33] etc. During remote memory access, optimization in data path has been proposed through request batching [36, 37, 71], eliminating page migration bottleneck [73], reducing remote I/O bandwidth through compression [44], and network-level block devices [46]. Leap’s data path optimizations are inspired by many of them.

Prefetching Algorithms. Many prefetching techniques exist to utilize hardware features [32, 34, 66, 80], compiler-injected instructions [26, 39, 40, 60, 61], and memory-side access pattern [22, 54, 67–69] for cache line prefetching. They are often limited to specific access patterns, application behavior, or require specified hardware design. More importantly, they are designed for a lower level memory stack than Leap’s prefetcher.

A large number of entirely kernel-based prefetching techniques have also been proposed to hide the latency overhead of file accesses and page faults [17, 23, 30, 38, 72]. Among them, Linux Read-Ahead [72] is the most widely used. However, it does not consider the access history to
make prefetch decision. It was also designed for hiding disk seek time. Therefore, its optimistic looking around approach often results in lower cache utilization for remote memory access.

To the best of our knowledge, Leap is the first to consider a fully software-based kernel-level prefetching technique for DRAM with remote memory as a backing storage over fast RDMA-capable networks.

7 CONCLUSION

We propose a remote page prefetching algorithm, Leap, that relies on majority-based pattern detection instead of strict detection. We implement it in a leaner and faster data path for remote memory access over RDMA without any modifications to the applications or hardware. By relying on a more permissible/approximate mechanism to detect access patterns instead of looking for trends in strictly consecutive accesses makes Leap resilient to short-term irregularities.

We have integrated Leap with two major memory disaggregation systems (namely, Infiniswap and Remote Regions), and Leap improves the median and tail remote page access latencies by up to 104.04× and 22.62×, respectively, over the default data path in Linux. This leads to application-level performance improvements of 1.27–10.16× over the state-of-the-art solutions. Applying Leap to slower storage systems such as HDD and SSD leads to large performance benefits too.
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