Effect of blocking and tunnel oxide layers on the charge trapping properties of MIS capacitors with ALD HfO$_2$/Al$_2$O$_3$ nanolaminated films

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Abstract. Electrical and charge trapping properties of HfO$_2$/Al$_2$O$_3$ nanolaminated stacks incorporated in three types of metal-insulator-silicon capacitor structures (without blocking and tunnel oxide layers; with 20 nm Al$_2$O$_3$ as blocking oxide and ~3 nm Al$_2$O$_3$ or thermal SiO$_2$ as tunnel layer) were investigated. HfO$_2$/Al$_2$O$_3$ stacks exhibit a positive initial oxide charge, and adding of the 3 nm Al$_2$O$_3$ tunnel layer to the capacitor doubles the amount of the positive charge and the density. Using SiO$_2$ as a tunnel layer resulted in a negative initial oxide charge which is interpreted by the effect of dipole formation at the Al$_2$O$_3$/SiO$_2$ interface. Tunnel SiO$_2$ provides lowest density of the interface states at silicon and leakage currents. The insertion of blocking and tunnel oxide layers to the capacitors significantly widens the memory windows; capacitors with a SiO$_2$ tunnel oxide demonstrate largest memory windows.

1. Introduction
The flash memories are preferred choice for data storage media for a variety of consumer and industrial devices as embedded or as standalone devices because they provide high data transfer rates, small size and weight, high robustness to mechanical shocks and low power consumption. With the rapid introduction of digital devices into every area of human life, the flash memory became the fastest growing product in the history of the semiconductor market. The majority of the existing non-volatile flash memories are based on the floating-gate (FG) cell technology. The requirements for aggressive shrinking of the memory cell size driven by the market, brought the floating-gate technology very close to its intrinsic physical limits [1]. There are several different new approaches offering non-volatile programmable memory effect, and each of them is in a different state of production readiness [1]. Among them, the charge trapping memory (CTM) is clearly gaining momentum recently promising to become main-stream in the near future. The CTM storage cell has the advantage of sharing the same operational principle as the floating-gate one, i.e. transfer of a charge from the MOSFET channel into and out of the gate dielectric stack, which facilitates significantly the migration from the FG production process to the new CTM one. The main difference between the CTM cell and FG one is the fact that in the latter case the charge is stored in an electrically isolated poly-Si floating gate embedded in the
dielectric, whereas in CTM charges are kept directly in discrete traps distributed in the dielectric band-gap of the gate dielectric. Although, the CTM effect based on Si$_3$N$_4$ [2] was established in the same year as the FG transistor (1967), the FG technology prevails up to now. The real progress of CTM is associated with the adoption of high-$k$ dielectrics in microelectronics. These materials apart of their much desired high dielectric constant were proven to have trap-rich nature, inferring that they are particularly suitable for the CTM. HfO$_2$ is one of the most thoroughly studied high-$k$ materials which has been already implemented in some advanced devices. Some recent studies have revealed that HfO$_2$ has better charge trapping efficiency than Si$_3$N$_4$ [3], and additional enhancement of the memory characteristics of HfO$_2$ layers can be obtained by introduction of Al in the film or forming nanolaminated HfO$_2$/Al$_2$O$_3$ stacks [4, 5].

Recently we have shown [6] that ALD nanolaminated HfO$_2$/Al$_2$O$_3$ stacks can provide excellent charge-trapping characteristics. It was noticed, however, that the reduction of the thickness of the HfO$_2$/Al$_2$O$_3$ film somehow degrades the effect of trapping [7]. In these previous studies the charge trapping properties were investigated on simple metal-insulator-silicon (MIS) capacitors – Al/(HfO$_2$/Al$_2$O$_3$ nanolaminate)/Si. Here we demonstrate that introduction of dedicated blocking (BO) and tunnel oxide (TO) layers into the MIS capacitor structure boosts the charge trapping into the stacks. The dependence of the charge trapping on the type of TO layers is also evaluated alongside with some of the electrical parameters of the stacked dielectric structures as oxide charges, interface states and leakage currents.

2. Experimental

The nanolaminated charge trapping HfO$_2$/Al$_2$O$_3$ stacks were fabricated on a Savannah-100 ALD system at a temperature of 135°C employing tetrakis(dimethylamido)hafnium (TDMAH) for HfO$_2$, trimethylaluminum (TMA) for Al$_2$O$_3$ and H$_2$O vapors as oxidant. The multilayered stacks were composed of equivalent bilayer blocks of HfO$_2$ and Al$_2$O$_3$ sublayers with constant thickness; the total stack was obtained by 5 repetitions of the bilayer block. For the deposition of each HfO$_2$ sublayer 20 ALD cycles were performed, and for the Al$_2$O$_3$ sublayers - 5cy, respectively. The deposition rate was ~0.14 nm and 0.1 nm per cycle in case of HfO$_2$ and Al$_2$O$_3$, respectively. (The deposition rates were estimated ellipsometrically on wafers covered by single HfO$_2$ and Al$_2$O$_3$ layers). The total thickness of the resulted HfO$_2$/Al$_2$O$_3$ stack was 16.5 nm. The MIS capacitors were produced using p-Si (100) wafers. The wafers received standard RCA chemical cleaning before deposition of the stacked dielectrics. Three different dielectric structures were produced. HfO$_2$/Al$_2$O$_3$ stack were deposited on: 1) bare Si surface; 2) on 3.5 nm SiO$_2$ film was grown by thermal oxidation of Si; and 3) on 3 nm thick Al$_2$O$_3$ layer deposited at the same ALD conditions as mentioned above in the same system without taking the substrate out. In case of structures 2 and 3 after finishing HfO$_2$/Al$_2$O$_3$ deposition process additional 20 nm top Al$_2$O$_3$ layer was deposited. According to the accepted notification, the 3.5 nm and 3 nm SiO$_2$ and Al$_2$O$_3$ layers at Si are referred as tunnel oxide (TO) layers and the 20 nm Al$_2$O$_3$ on the top of the HfO$_2$/Al$_2$O$_3$ is referred as a blocking oxide (BO) layer. MIS capacitors fabrication was accomplished by Al metallization through evaporation to create gate (top) and backside electrodes. The gate electrodes were patterned by photolithography. The schematic representation of the capacitors is given in figure 1. The electrical properties of the stacks were examined by measuring high-frequency capacitance-voltage ($C-V$) and current-voltage ($I-V$) measurements in dark chamber. The charge-trapping was evaluated by applying voltage pulses with different magnitudes and polarity to the gate electrode followed by the $C-V$ measurement to obtain the shift of the $C-V$ curve as a result of the charge trapped in the dielectric.

3. Results and discussion

In order to evaluate the quality of the interface between the dielectric stacks and the Si substrate as well as the density of the initial charges (prior to any charge storage) which define the initial state, high frequency $C-V$ measurements at 1 MHz and 10 kHz were performed. In these measurements the voltage across the capacitors were swept between -3 V to 1 V which was enough to record $C-V$ curves while
Figure 1. Schematics of the investigated MIS structures: (a) type 1 capacitor without BO and TO layers; (b) type 2 capacitor with SiO2 and Al2O3 as TO and BO, respectively; and (c) type-3 capacitor with TO and BO of Al2O3.

preventing carrier injection from both of the electrodes. The oxide charge was calculated using the values of the flat band voltage \( V_{fb} \) obtained from 1 MHz C-V curves [8]

\[
Q_{ox} = -(V_{fb} - \phi_{ms}) \times C_0,
\]

where \( \phi_{ms} \) is the work function difference between Al and Si, and \( C_0 \) is the capacitance in accumulation. \( V_{fb} \) was defined as the voltage corresponding to the flat-band capacitance [8]. The density of interface states was estimated by the Hill-Coleman method [9] from the C-V and conduction-voltage (G-V) curves measured simultaneously at 10 kHz and corrected for the effects of the parasitic serial resistance according to [8]

\[
D_{it} = \frac{2q}{\omega} \frac{G_{m,\max}/\omega}{(G_{m,\max}/\omega C_0)^2 + (1 - C_m/C_0)^2}
\]

\( G_{m,\max} \) is maximum measured conductance, \( C_m \) corresponding to \( G_{m,\max} \) capacitance, \( A \) – capacitor’s area, \( q \) – elementary charge, \( \omega \) - angular frequency.

The obtained results show that the initial oxide charge \( (Q_{ox}) \) and the density of the interface states \( (D_{it}) \) are strongly affected by the type of the tunnel oxide layer. Initial oxide charge in capacitors without BO and TO is positive with density \( \sim 1.4 \times 10^{12} \) cm\(^{-2}\). MIS structures with Al2O3 TO also exhibit positive \( Q_{ox} \), but with rather high density \( \sim 2.7 \times 10^{12} \) cm\(^{-2}\). This suggest that the thick Al2O3 TO introduces high amount of positive oxide charge. Employing silicon oxide as a tunnel layer, however, results in negative \( Q_{ox} \) \( \sim -4.6 \times 10^{11} \) cm\(^{-2}\). The last value is somewhat surprising taking into account that the interface between thermally grown SiO2 and Si is characterized by the presence of so called fixed positive charge [8], which strongly influences the \( V_{fb} \) values in the direction opposite to the observed. The negative \( Q_{ox} \) can be explained on the bases of a dipole formation at the Al2O3/SiO2 interface, as demonstrated in [10]. The \( V_{fb} \) shift in the positive \( V \) direction found in [10] was as high as 0.55 V for the ALD-Al2O3/SiO2 interface. The rough correction of the \( V_{fb} \) values with the dipole inflicted shift assessed in [10] for the capacitors with SiO2 TO leads to a positive oxide charge of \( \sim 5 \times 10^{11} \) cm\(^{-2}\). The impact of the Al2O3/SiO2 dipole might be additionally enhanced by the dipoles at HfO2-Al2O3 interfaces which have the same direction as the Al2O3-SiO2 dipole [11]. Simultaneously, even in presence of an ultrathin, 2-3 nm thick, intrinsic interfacial SiO2 layer at the Al2O3/Si interface, the data for the structures without BO and TO and those with Al2O3 tunnel oxide cannot be explained by the influence of dipole effects as both possible dipoles, HfO2-Al2O3 and Al2O3-SiO2, inflict changes in \( V_{fb} \) opposite to the shift caused by the positive oxide charge. Hence we suggest that the investigated HfO2/Al2O3 nanolaminated
stacks are characterized by a presence of positively charged centers. The location of these centers is unclear at present. Most likely, the positively charged defects are embedded into the HfO2 sublayers as hafnia is often reported to possess positive oxide charge, while the negative oxide charge is frequently found in Al2O3 [12]. Nevertheless, Al2O3 cannot be completely eliminated as a source of the observed here positive oxide charge, as in some works Al2O3 with positive oxide charge is detected [13]. It also should be noted that the obtained Qox values are in fact the effective ones. In multilayered dielectrics they are defined by the charges in the bulk of the dielectrics, charges at interfaces between them, possible dipole effects and the influence of the interface states at Si. The assessment of the contribution of each component mentioned above requires specially designed experiments with variation of the sublayer thicknesses which is out of the scope of the present work.

The estimated Dit from (2) shows that SiO2 tunnel layer provides, expectedly, the best interface between the 3 types of MIS capacitors – $D_{it} \sim 1.1 \times 10^{11}$ eV$^{-1}$cm$^{-2}$. The density of the interface states of the capacitor without BO and TO is about $1 \times 10^{12}$ eV$^{-1}$cm$^{-2}$ and for the capacitor with Al2O3 TO it is $2 \times 10^{12}$ eV$^{-1}$cm$^{-2}$. However, it should be taken into account that the interface states can be responsible for a part of the high amount of positive oxide charge. The fast interface states at the Si surface are amphoteric – positively charged when empty, neutral when occupied by one electron, and negatively charged if two electrons are trapped. In flat band condition a part of the interface states are empty and contribute to the measured positive oxide charge. The high Dit might pose a problem for the real transistor based memory cells as it will decrease the mobility of the carriers in the transistor’s channel.

The effect of the charge trapping into the memory capacitors is presented in figure 2 where the shifts in the flat band voltage, $\Delta V_{fb}$, after the applying voltage pulses in respect to its initial ( unstressed) value are shown. The voltage pulses (1s duration) with negative and positive polarity were applied to the top metal electrode (back Al electrode is grounded) and after each pulse a control C-V curve was recorded to observe the charge trapping (figure 2a). The maximum shown $|V_p|$ are defined by the dielectric breakdown of each capacitors type. Positive pulses lead to electron injection from Si into the dielectric, while at the negative ones holes from the substrate are transferred into the stack. As evidenced from figure 2b, in structures without BO and TO electron trapping starts after applying $V_p > +3$ V, and the maximum shift is at $+6$ V, while the negative pulses with amplitudes in this range does not result in any positive charge trapping (moreover after $-V_p$ pulse some negative charge still remains in the capacitors). At higher $|V_p|$, however, the positive charge build-up dominates the response of the capacitor to the voltage pulses. So, $\Delta V_{fb}$ turns-down and changes its sign for $V_p > 10$ V (C-V curves for both pulse polarities are relocated towards negative applied voltages). The resulting memory window, which is defined as a difference between $\Delta V_{fb}$ for $+V_p$ and $-V_p$, is $\sim 2.7$ V obtained under $|V_p| = 11$ V, largely owing to the contribution of the hole trapping. The insertion of blocking and tunnel oxide strongly affects the charge trapping characteristics (figure 2c and d). In case of memory capacitors with 3.5 nm SiO2 as TO, a shift of the C-V in the range up to $|V_p| \sim 20$ V is hardly visible, i.e. the charge accumulated into the stack is negligible. When $V_p$ exceeds $\pm 20$ V, trapping of electrons and holes begins at the respective polarities of $V_p$. The corresponding $V_{fb}$ shifts increase for both charge types with the increase of $V_p$ but still the positive charge build-up is stronger (higher $\Delta V_{fb}$ are obtained than at $-V_p$). The memory window reaches a value of 23 V at $|V_p| \sim 36$ V. The memory windows for the capacitors with the Al2O3 tunnel oxide start to develop at $\pm 9$ V. Prior to that a weak positive charge buildup takes place, as the C-V curves for both $V_p$ polarities tends to shift aside the negative voltages at $|V_p|$ above 9 V electron trapping begins, but unlike the SiO2 case, $\Delta V_{fb}$ saturates at values of 1 V. The hole trapping is generally the same as for the capacitors with SiO2 TO; $\Delta V_{fb}$ under $-V_p$ linearly increases with the pulse magnitude. For the three capacitor types the positive charge accumulation at $-V_p$ is stronger than the electron trapping, which can be explained either by more effective hole trapping (as hole’s mobility is lower than electron one, or by additional stress generation of positive charge under the high $-V_p$ a commonly observed phenomenon in MIS capacitors).
Figure 2 Effects of charge trapping into the capacitors as evaluated by \( C-V \) measurements: (a) illustration of the measurement procedure and (b, c, d) flat-band voltage shifts (\( \Delta V_{fb} \)) in respect to the initial \( V_{fb} \) value for the investigated MIS capacitors. Full symbols denote \( \Delta V_{fb} \) after positive pulses and opened ones after negative \( V_p \).

Figure 3 \( J-V \) curves of the investigated capacitor structures.

Leakage current characteristics of the investigated structures are illustrated in figure 3. The employment of BO and TO significantly reduces the leakage currents through the capacitor for both polarities. Although, a SiO\(_2\) TO provides better \( J-V \) characteristics than a TO of Al\(_2\)O\(_3\), the difference in \( J \) for the positive applied \( V \) (especially the onset of the high voltage conduction which is \( ~+10 \) V for both capacitors) is not as high as expected form the corresponding barrier heights at the Si interface. The SiO\(_2\) band gap of 9 eV is suggested to ensure the potential barrier of \( ~3.2 \) eV for electrons, while
in case of Al₂O₃ it is ~ 2 eV [14]. One tentative explanation can be the presence of an undesired interfacial SiO₂ layer at stack deposition affecting the barrier height. J corresponding to the beginning of the electron trapping is estimated to ~1.6×10⁻⁶ A/cm² from figure 2 and 3. The current at negative V is generally lower than J at positive voltages for capacitors with BO and TO. Moreover, the J values matching the beginning of the positive charge accumulation are also lower than J corresponding to onset of negative charge trapping. This suggests better effectiveness of the hole trapping (due to lower mobility of the holes) or that a part of the positive charge is a result of electron detrapping from initially neutral centers.

4. Conclusion
The results demonstrate that incorporation of dedicated blocking and tunnel oxide into the memory MIS capacitors with HfO₂/Al₂O₃ nanolaminated stacks improves the obtained memory windows, through enhancement of the electron trapping. The effect is associated, as suggested in [15], to the confinement of the injected into the HfO₂/Al₂O₃ stack electrons by the blocking and tunnel oxides which facilitates their capturing. The choice of the type of the tunnel layer type additionally affects the quality of the interface at Si and the oxide charges of the structures. The employment of SiO₂ as a tunnel layer ensures the best characteristics, but with the cost of increase of the voltages required to write and erase the information of the cell. Hence, further improvement of the cell structure is desirable.

Acknowledgment
The work is supported by Bulgarian National Science Fund under project KP-06-H37/32.

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