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Frequency Selective Degeneration for 6–18 GHz GaAs pHEMT Broadband Power Amplifier Integrated Circuit

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Abstract: In this paper, a frequency selective degeneration technique using a parallel network with a resistor and capacitor is proposed for a 6–18 GHz GaAs pseudomorphic high electron mobility transistor (pHEMT) broadband power amplifier integrated circuit (PAIC). The proposed degeneration network is applied to the source of the transistor to flatten the frequency response of the transistor in conjunction with feedback and resistor biasing circuits. An almost uniform frequency response was achieved at the wide frequency band through optimizing the values of the capacitor and resistor for the degeneration circuit. Single-section matching networks for small chip sizes were adopted for the two-stage amplifier following the flat frequency characteristics of the degenerated transistor. The proposed broadband PAIC for the 6 to 18 GHz band was fabricated using a 0.15 \( \mu \)m GaAs pHEMT process and had a chip size of 1.03 \( \times \) 0.87 mm\(^2\). The PAIC exhibited gain of 15 dB to 17.2 dB, output power of 20.5 dBm to 22.1 dBm, and linear output power of 11.9 dBm to 13.45 dBm, which satisfies the IMD3 of \( -30 \) dBc in the 6–18 GHz band. Flatness for the gain and output power was achieved as \( \pm 1.1 \) dB and \( \pm 0.8 \) dB, respectively.

Keywords: broadband; power amplifier; GaAs pHEMT process; integrated circuit; frequency selective degeneration

1. Introduction

Broadband PAICs that operate in a wide frequency range from C- to Ku-band have been used in various applications, including various point-to-point radios, test instruments, sensors, military or space applications, and so on. Broadband PAIC should be designed considering not only gain, output power, and chip size but also other characteristics, such as flatness, input reflection coefficient, and output reflection coefficient [1–22].

Broadband impedance matching techniques have been used to report broadband PAICs [1–3]. A broadband PAIC with a differential cascode structure was designed using a 0.13 \( \mu \)m SiGe BiCMOS process and it exhibited a gain from 11 dB to 16.6 dB and output power of from 21.3 to 25.5 dBm for the frequency band of from 4.5 to 15.5 GHz [1]. In spite of using on-chip transformers for broadband impedance matching, the flatness characteristics for gain and output power was not so good as \( \pm 2.8 \) dB and \( \pm 2.1 \) dB, respectively. These PAIC has relatively large chip sizes due to the large size of the on-chip transformer. In [2], a broadband GaAs (pHEMT) PAIC based on a dual-frequency selective impedance matching technique was reported with gain of from 16.4 to 18.4 dB and output power of from 19.2 to
21 dBm for the 6–18 GHz frequency band. However, the size of the circuit could be increased due to the multi-section matching network for the dual-frequency selective impedance matching.

Distributed PAs for broadband characteristics have been reported [4–6]. A broadband distributed PAIC based on the capacitive division technology to reduce gate capacitance using a GaN HEMT process was reported for very wide operating frequency range of from 2 to 18 GHz [5]. However, the chip size of the distributed PAICs was generally large due to the use of multiple transmission lines. In addition, distributed PAICs showed relatively low efficiency characteristics [4–6]. GaAs pHEMT processes have relatively lower power density but are cheaper compared to GaN pHEMT processes. Compared to other silicon processes, including the SiGe BiCMOS process, GaAs pHEMT processes are expensive but have a capability of high-power design due to the higher breakdown voltage.

In this paper, a broadband GaAs pHMET PAIC is presented using a proposed frequency selective degeneration technique based on a parallel network with a resistor and capacitor. By optimizing the component values in the frequency selective degeneration circuit, a flat frequency response can be achieved by gradually decreasing the degeneration level according to the increasing frequency only with single-section matching networks. Feedback and resistor biasing circuits were also used to obtain a flatter frequency response. The PAIC has a two-stage, single-ended structure and a very small chip size with single-section matching networks. It was designed using a 0.15 μm GaAs pHMET process. The experimental results will be summarized and compared to the previously reported works.

2. Design of the Proposed Broadband PAIC

Broadband PAIC should be designed to have uniform performances over a wide frequency band, which is very difficult because the gain of the transistor rapidly decreases as the frequency increases. A feedback and/or resistor biasing circuit have been conventionally used to reduce the gain at the low frequency without greatly reducing the gain of the high frequency band [2]. However, obtaining a very flat frequency response of the transistor over a wide frequency band is still a great challenge.

Figure 1 shows the source- and load-pull setup of the degenerated transistor with a resistance and feedback circuits for the proposed broadband PAIC. $R_F$ and $C_F$ are the series resistor and capacitor of the feedback circuits. $R_G$ is the resistor of the resistor bias circuit. The proposed frequency selective degeneration circuit consists of a resistor of $R_S$, capacitor of $C_S$, and an equivalent inductor of $L_{VIA}$ for the through-wafer via.

![Figure 1. Source- and load-pull setup for the proposed broadband power amplifier integrated circuit (PAIC).](image)

Figure 2a shows the frequency characteristics (S11) from DC to 30 GHz according to the capacitor values of the frequency selective degeneration circuit with a resistance of 1 Ω. According to the value of the capacitor, the frequency to have the real part of the impedance minimum (almost zero)
shifts. Figure 2b shows the maximum stable gain (MSG) characteristics with various values of the capacitor in the frequency selective degeneration circuit. Increased power gain can be observed at the frequency that has a minimum resistance. For a 6–18 GHz broadband PAIC application, a slightly higher frequency of 21 GHz from the upper corner was selected to have a minimum degeneration with a capacitance of 4.2 pF.

![Figure 2](image)

**Figure 2.** Frequency characteristics according to the capacitor values with a resistance of 2 Ω, (a) S11 for the frequency selective degeneration circuit, (b) maximum stable gain (MSG) of the transistor.

Figure 3a shows the frequency characteristics (S11) from DC to 30 GHz according to the resistor values of the frequency selective degeneration circuit with a capacitance of 4.2 pF. Figure 3b shows the MSG characteristics, which shows that the level of degeneration can be controlled by the value of the resistor. The $R_S$ value for the proposed broadband PAIC design was optimized as 1 Ω. The simulated MSGs according to the frequency for the main stage are shown in Figure 4. Using the feedback and resistor bias circuits, the MSG value at the low frequency band can be somewhat reduced. Through the proposed frequency selective degeneration circuit, the MSG characteristics at low frequencies can be further reduced, while the MSG at high frequencies, especially for 21 GHz, can be very well maintained. As shown, the simulation results show that the flatter frequency response across the wide frequency band can be achieved. The drive stage can also be designed using the same structure as the main stage. The component values used in the design of the main and drive stages are presented in Table 1.

![Figure 3](image)

**Figure 3.** Frequency characteristics according to the resistor values with a capacitance of 4.2 pF, (a) S11 for the frequency selective degeneration circuit, (b) MSG of the transistor.
Figure 4. Simulated MSGs of the main stage with optimized resistance and capacitance of 1Ω and 4.2 pF for the degeneration circuit, respectively.

Table 1. Component values for the feedback, resistor bias, and frequency selective degeneration circuits.

| Main Stage | Drive Stage |
|------------|-------------|
| $R_F$ | 200Ω |
| $C_F$ | 1 pF |
| $R_G$ | 50Ω |
| $R_S$ | 1 Ω |
| $C_S$ | 4.2 pF |
| $R_F$ | 300Ω |
| $C_F$ | 1 pF |
| $R_G$ | 126Ω |
| $R_S$ | 1 Ω |
| $C_S$ | 4.2 pF |

3. Experimental Results

Figure 5 shows the schematic diagram of the proposed broadband PAIC using the frequency selective degeneration circuit. The feedback, resistor biasing, and frequency selective degeneration circuits were simultaneously optimized to make the frequency response of the transistor as flat as possible. The proposed PAIC was designed with a two-stage and single-ended structure. The gate widths of the main and drive stages were $4 \times 75 \mu m$ and $2 \times 75 \mu m$, respectively. The flat frequency response, as shown in Figure 4, allows the adoption of the single-section matching networks for small chip size. The output and inter-stage matching networks were designed with a high-pass structure, while the low-pass matching network was adopted at the input. The shunt inductor at the high-pass matching network was used to supply the DC voltage of 5 V to the drain. Figure 6 shows a photograph of the proposed broadband PAIC designed using Win Semiconductor’s 0.15 μm GaAs pHEMT process, which provides an enhanced-mode GaAs PHEMT whose breakdown voltage is about 10 V. The quiescent currents of the main and drive stages were 64 mA and 41 mA, respectively.

Figure 5. Overall schematic diagram of the proposed broadband PAIC.
Figure 6. Overall schematic diagram of the proposed broadband PAIC.

Figure 7 shows the measurement results of the proposed 6 to 18 GHz GaAs pHEMT broadband PAIC. Figure 7a shows the measured S-parameters of the PAIC. For the 6 to 18 GHz band, S21 of 17.2 dB at 15 GHz, S11 of −9.15 dB or less, and S22 of −10.03 dB or less were measured. The flatness of S21 was ±1.1 dB in the band. The term ‘flatness’ can be defined for gain and output power in the given frequency band as follows

\[ \text{flatness} = \pm \frac{\text{maximum value} - \text{minimum value}}{2}. \]  

Figure 7. Experimental results of the proposed 6–18 GHz GaAs pHEMT broadband PAIC, (a) small-signal S-parameters, (b) saturated output power and PAE, and (c) linear output power with an IMD3 of −30 dBc and −40 dBc, (d) mu factor.
The measurement results using a CW signal and a two-tone signal with a tone spacing of 10 MHz are shown in Figure 7b,c. Flatness of the saturated output power ±0.8 dB in the frequency band of 6 to 18 GHz was achieved. Power-added efficiency (PAE) of up to 20.3% was measured at the saturated output power of from 20.5 dBm to 22.1 dBm at the band. The output power that satisfies the IMD3 of −30 dBc was obtained in the range of 11.9 to 13.45 dBm, while the output power that satisfies the IMD3 of −40 dBc was obtained in the range of 7.8 dBm to 9.96 dBm. For the frequency band of 0 GHz to 30 GHz, the mu factor of no smaller than 1 can be observed from Figure 7d. Keysight’s advanced design system (ADS) for the circuit design and the momentum in ADS for electro-magnetic (EM) field simulation are used.

In Table 2, the measured performances were summarized and compared to the previously published broadband PAICs. The proposed broadband PAIC had the smallest chip size compared to the sizes of the PAICs presented in the previous works. It also had the best output power flatness, which was ±0.8 dB in the 6–18 GHz band. Compared to [1], this work clearly shows better performances in gain, gain flatness, input reflection, and output reflection characteristics. The proposed PAIC exhibited a higher PAE compared to [5]. In addition, this work reported the highest output power compared to the broadband PAICs designed with the GaAs pHEMT process.
Table 2. Component values for the feedback, resistor bias, and frequency selective degeneration circuits.

| Ref. | Process          | Freq. (GHz) | Gain * (dB) | Gain Flatness (dB) | Input Reflection ** (dB) | Output Reflection ** (dB) | P<sub>out</sub> *** (dBm) | P<sub>out</sub> Flatness (dB) | PAE (%) | Size (mm<sup>2</sup>) | Structure              |
|------|-----------------|-------------|-------------|--------------------|--------------------------|---------------------------|---------------------------|-----------------------------|----------|----------------------|-------------------------|
| [1]  | 0.13 μm SiGe    | 4.5–15.5    | 13.8        | ±2.8               | −5.0                     | −2.3                      | 21.3                      | ±2.1                        | 11.9–28.7 | 1.96                 | Cascode differential    |
|      | BiCMOS          |             |             |                    |                          |                           |                           |                             |          |                      |                         |
| [5]  | 0.2 μm GaN      | 2.0–18.0    | 19.5        | ±1.5               | −14.0 +                 | −5.0 +                    | 26.0                      | ±2.0                        | 5.0–12.0 | 8.0                  | Distributed             |
|      | HEMT            |             |             |                    |                          |                           |                           |                             |          |                      |                         |
| [4]  | 0.15 μm GaAs    | 3.0–14.0    | 17.0        | ±1.0               | −15.0                    | −10.0                     | 15.0                      | −                           | −         | 7.44                 | Distributed             |
|      | pHEMT           |             |             |                    |                          |                           |                           |                             |          |                      |                         |
| [3]  | 0.25 μm GaAs    | 6.0–18.0    | 12.0        | ±1.0               | −10.0 +                 | −10.0 +                   | 15.0                      | ±1.5                        | −         | 5.2                  | Two-stage               |
|      | pHEMT           |             |             |                    |                          |                           |                           |                             |          |                      |                         |
| [2]  | 0.15 μm GaAs    | 6.0–18.0    | 17.4        | ±1.0               | −8.0 +                  | -                         | 19.2                      | ±0.9                        | 13.0–21.7 | 0.97                 | Two-stage               |
|      | pHEMT           |             |             |                    |                          |                           |                           |                             |          |                      |                         |
| This work | 0.15 μm GaAs  | 6.0–18.0    | 16.1        | ±1.1               | −9.1                     | −10.0                     | 20.5                      | ±0.8                        | 12.4–20.3 | 0.89                 | Two-stage               |

* median value; ** maximum value; *** minimum value; + graphically estimated.
4. Conclusions

In this paper, the frequency selective degeneration method for a 6 to 18 GHz GaAs pHEMT broadband PAIC was proposed. In order to achieve flatter frequency response of each stage, the feedback and resistor biasing circuits were used in addition to the frequency selective degeneration circuit. The level of degeneration and frequency range where the degeneration effect is minimized were controlled by optimizing the values of the capacitor and resistor in the frequency selective degeneration circuit. As a result, very flat frequency characteristics were achieved compared to the condition only using the feedback and resistor biasing circuits. The chip size was reduced by using single-section matching networks.

The proposed PAIC was designed using Win Semiconductor’s 0.15 µm GaAs pHEMT process and had a size of 1.03 × 0.87 mm². The fabricated PAIC has a two-stage and single-ended structure. It showed an average gain of 16.1 dB, gain flatness of ±1.1 dB, input reflection coefficient of no larger than −9.1 dB, and an output reflection coefficient of no larger than −10 dB in the frequency band of 6 to 18 GHz. The output power of 20.5 dBm to 22.1 dBm, output power flatness of ±0.8 dB, and PAE of from 12.4% to 20.3% were also experimentally obtained. It was experimentally verified that the proposed frequency selective degeneration circuit is beneficial to design broadband PAICs.

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