A New Absolute Phase Detection Scheme

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Abstract In this paper, the new absolute phase detection scheme (APDS) is presented. With a simple mathematical analysis, the proposed APDS algorithm is capable of accurately detecting the absolute phase without using reference phase like other conventional techniques. The other massive benefit of using the proposed APDS scheme is its range-expansion flexibility for each application depending on the selected traditional PD. Based on the proposed APDS, BPSK and QPSK demodulated simulations, accurately recovering 16-bit-information data, are implemented with the blind carrier recovery methods. Also, the analog multiplier PD was selected in order to verify the proposed QPSK demodulator under the AWGN channel. It is found that the output phase is irrelevantly disturbed by additive white Gaussian noise. For the QPSK-demodulated PSPICE simulation, the proposed technique is more compatible with the frame processing manner rather than the real time processing. From both PSPICE and Matlab simulations for BPSK and QPSK demodulation the proposed APDS scheme provides convenience, advantages, and acceptable results in comparison to other traditional techniques.

Keywords: carrier recovery, mono-stable multi-vibrator, phase detection, quadrature phase shift keying, synchronizer

1. Introduction

Phase constant \([1]\) of the oscillating signals has two different meanings. One called phase offset or phase difference is the initial angle of a sinusoidal function at its origin (see (1)). The other meaning is the position on the wave cycle that has elapsed relative to the origin. In the context of communication waveforms, the time-variant angle \(2 \cdot f_c \cdot t + \) is referred to as instantaneous phase of \(x(t)\).

\[
x(t) = A \cos(2 \cdot f_c \cdot t + \phi) = A e^{j(2 \cdot f_c \cdot t + \phi)}
\]

where \(A\), \(f_c\), and \(\phi\) are amplitude, local frequency and the phase of sinusoidal function, respectively. In the case of infinite sinusoids, the phase shift is considered as a time delay of the signal. Phase has been widely used in the communication industry especially in the modulation system. Two important types of phase measurements are an absolute phase and relative phase measurements.

The absolute phase \([2-3]\) is the actual phase of the vibration waveform at the frequency of interest, which is measured with respect to the standard time such as Coordinated Universal Time (UTC). Also, absolute phase can be defined as zero degree corresponding to the positive maximum of a cosine wave coincident with the on-time reference. Whenever measurements of any sort are made with reference to a consistent external standard, it becomes possible to compare measurements, which is therefore called the relative phase. These measurements are made at different times and places, and are known with certainty how they compare. Many researches have presented the methods to measure the absolute phase such as “Remote absolute phase measurement in a buried cable system [4]”, “Precise measurement of power system frequency and absolute phase based on GPS [5]” and “Absolute phase in power system applications [6]”. Not only do these researches have their own specific ways to measure the absolute phases, but these measurements can also be used to calculate the relative phases as well. For the relative phase, it is the difference between the absolute phases of two vibration waveforms \([7]\). It is necessary that both signals must be of the same frequency and vibration units i.e. if one signal is generated at the frequency of \(f_c\), and the other at \(2 \cdot f_c\), the relative phase cannot be measured. The usage of the relative phase has been expanded to many fields such as “Target detection on the ocean with the relative phase of compact
polarimetry SAR [8]”, “The method of signal processing of relative phase modulation [9]” and “MIMO system with relative phase difference time-shift modulation in Rician fading environments [10]”.

Also, many relative phase detection techniques [11] have been implemented in different purposes such as the analogue multiplier PD, the exclusive OR gate PD, and the mono-stable multi-vibrator and RS flip-flop. For the analogue multiplier PD, which has a narrow phase detection range (0° - 180°), the phase reference from the transmitter is required to be one of the multiplier inputs. The limitations of the exclusive OR gate PD are that the reference signal requirement, the type of both input-signal needs to be only square waves, and the phase detection range (0° - 180°) is narrow. In order to expand the phase detection to full range of 360°, the combination of the mono-stable multi-vibrator and RS flip-flop are obtained, but the requirement of a reference signal still exists. According to these limitations of these traditional phase detectors, a new absolute phase detection scheme (APDS) without the prior reference phase requirement so as to achieve all of the existing limitations is presented in this article. Not only does the proposed APDS not require the reference phase, but it also provides the flexibility for phase-detection-range expansion due to the ability of the proposed APDS in order to switch the sub-PD to suit each application.

In digital modulation, phase shift keying (PSK) has been used in order to transfer the information data to the receiver [12-14]. Phase shift keying is a massive class of digital modulation scheme such as the coherent binary phase shift keying (BPSK), the differential binary phase shift keying (DBPSK), and the quadrature phase shift keying (QPSK). Among all MPSK schemes, QPSK is the most popular modulation because it does not suffer from BER degradation [15] while the bandwidth efficiency is increased. With the phase detection property of the proposed APDS, it can be applied as BPSK and QPSK demodulation. The contributions of the proposed APDS for a new BPSK and QPSK demodulation will also be presented in this paper.

This article is organized as follows: the conventional phase detections, the proposed phase detection algorithm without using reference phase, and the non-ideal effects of the APDS’s components are mentioned in section 2. In section 3 and 4, the proposed BPSK and QPSK demodulation schemes with the blind carrier recovery method will be respectively discussed in detail. Section 5 illustrates the results of Matlab and PSPICE computer simulations. Finally, the conclusion is provided in section 6.

2. Phase Detections

2.1 Conventional phase detections

A phase detector [11] is the circuit, which compares and detects the phase difference from input signal and the reference signal generated by using the prior reference phase information. From Fig.1, \( \phi_d(t) \) is the phase difference between input phase \( \phi_i(t) \) and \( \phi_o(t) \). \( k_d \) and \( v_d(t) \) are the constant and the output of the phase detector, respectively.

2.2 An analogue multiplier PD

From Fig. 2, an analogue multiplier phase detector [11] is the circuit detecting the phase difference from sinusoidal signal input \( x_i(t) \) and the reference sinusoid \( x_{ref}(t) \) generated by using the prior reference phase information. The phase detection range of this PD is limited from 0° - 180°.

2.3 Exclusive OR gate PD

This circuit is used to detect the phase difference from a square wave input and the reference square wave. With the property of Ex-OR gate [11], the frequency of the output is twice the amount of the reference frequency. The characteristic of phase detection range is the slope \( \left( k_d \right) \) plotted between average output amplitude value and phase difference value. From Fig. 3, the maximum output amplitude occurs at the 180° phase difference implying that the phase detection range of Ex-OR gate can be only from 0° to 180°.

2.4 Mono-stable multi-vibrator and RS flip-flop

This RS flip-flop phase detector [11] depicted in Fig. 4 consists of two parts, which are the mono-stable multi-vibrator and the RS flip-flop. With the property of RS flip-flop, the frequencies of both input and output signals are the same.
where $A$, $\omega_0$ and $\theta$ are amplitude, angle frequency and the phase of the input signal respectively. By squaring (2), it yields

$$x^2(t) = A^2 \cos^2(\omega_0 t + \theta) = A^2 \left(\frac{1+\cos(2\omega_0 t + 2\theta)}{2}\right)$$

Eliminating the DC constant from (3) results in

$$y(t) = \frac{A^2 \cos(2\omega_0 t + 2\theta)}{2}$$

By using a divide-by-2 frequency divider, (4) can be rewritten as (5)

$$z(t) = \frac{A^2 \cos(2\omega_0 t + 2\theta)}{2}$$

Equation (5) is the regenerated reference signal without using the prior reference requirement. In order to detect the absolute phase of the input $x(t)$, one of the conventional phase detectors called the analogue multiplier PD is selected. By multiplying (5) with $x(t)$, it yields

$$x(t) \cdot z(t) = \frac{A^4}{4} \cos(2\omega_0 t + 3\theta) + A^4 \cos(\theta)$$

By using LPF, the low frequency component is obtained, which is

$$x(t) = \frac{A^4 \cos(\theta)}{4}$$

From (7), the phase of the input signal can be retrieved without the prior reference phase requirement. However, the limitation of the proposed APDS is that the phase detection range should be between 0° and 180°, otherwise the detected absolute phase might be duplicated. It should be noted that the proposed APDS has only four steps in order to detect the absolute phase, which are squaring the input signal, DC offset elimination, divide-by-2 frequency division and phase detection.

### 2.6 The non-ideal effects of the APDS’s components

In this section, the discussion about the non-ideal effects of the proposed scheme’s components such as the squaring part, the DC eliminator and the frequency divider is considered. The component that might affect to the proposed scheme the most is the squaring part. Hence, the analog four-quadrant multiplier depicted in [16] will be selected to discuss in detail about its static error for the proposed principle.

Generally, an analog four-quadrant multiplier produces an output which is proportional to the product of two independent bipolar inputs. In this paper, let the two inputs of this multiplier be the same, which are

$$V_x = V_y = A\cos(\omega t + \theta) + X_{\omega}$$

where $X_{\omega} = Y_{\omega}$

$$x(t) = A\cos(\omega t + \theta)$$

where $A$, $\omega_0$, and $\theta$ are amplitude, angle frequency and the phase of the input signal respectively. By squaring (2), it yields

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where $X_m$ and $Y_m$ are input offset. The ideal multipler’s output is

$$E_o = KV_x V_y = V_x V_y = K \left( A \cos(\omega t + \theta) + X_m \right)^2$$  \hspace{1cm} (9)

The proportionality constant $K = V_y^{-1}$ is usually fixed at 0.1$V^{-1}$, $|E_o| < V_y$, and 0 $\leq |V_x, V_y| \leq V_y$. The output of a practical multiplier will differ from the theoretical product of its inputs by an unpredictable amount, $\varepsilon(V_x, V_y)$, as defined in this equation

$$E_o = KV_x V_y \pm \varepsilon(V_x, V_y)$$  \hspace{1cm} (10)

There are four primary sources of static error in an analog multiplier which are the input offsets $(X_m, Y_m)$, the output offset $(Z_m)$, the scale factor $\Delta K$, and nonlinearity $f(X,Y)$ shown as follows

$$E_o = KV_x V_y + \Delta KV_x V_y + (K + \Delta K) \times \left[ V_x Y_m + V_y X_m + (X_m Y_m) + (Z_m) + f(X,Y) \right]$$  \hspace{1cm} (11)

For the nonlinearity, the unbalance current or offset-voltage mismatch between the two differential pairs, Q1A-B and Q3A-B is the primary source of the nonlinearity [16]. This error is generally irreducible; however, in this certain case, a large percentage of it can be eliminated. The 4-quadrant variable-transconductance multiplier circuit has predominantly second-order nonlinearity, so (11) can be rewritten as

$$E_o = KV_x V_y + \Delta KV_x V_y + (K + \Delta K) \times \left[ V_x Y_m + V_y X_m + (X_m Y_m) + (Z_m) + f(X,Y) \right]$$  \hspace{1cm} (12)

where $\delta$ is the constant factor to the nonlinear term. If the nonlinear term is independent of (or not strongly influenced by) $V_y$, then the nonlinearity term can be written as $\delta V_y^2$.

$$E_o = KV_x V_y + \Delta KV_x V_y + (K + \Delta K) \times \left[ V_x Y_m + V_y X_m + (X_m Y_m) + (Z_m) + \delta V_y^2 \right]$$  \hspace{1cm} (13)

The effects of these first three errors can be reduced to zero by precise adjustment of the scale factor to cancel the 3rd error and by introducing equal and opposite offsets for cancelling the 1st, 2nd errors. Assuming that $\Delta K = 0$, (13) is rewritten as

$$\frac{E_o}{K} = V_x V_y + \left[ V_x Y_m + V_y X_m + (X_m Y_m) + (Z_m) + \delta V_y^2 \right]$$  \hspace{1cm} (14)

Substituting $V_x, V_y$ in (14) by (8), then it results as

$$\frac{E_o}{K} = \left( A \cos(\omega t + \theta) + X_m \right)^2 + 2 \left( A \cos(\omega t + \theta) + X_m \right) X_m + \left( X_m \right)^2$$  \hspace{1cm} (15)

By rearranging and rewriting (15), it then becomes

$$\frac{E_o}{K} = \left( A \cos(\omega t + \theta) + 2X_m \right)^2 + \left( Z_m \right)^2$$  \hspace{1cm} (16)

By precisely introducing the equal and opposite offsets to this multiplier, it can then be assumed that $Z_m = 0$ and $X_m = 0$.

$$E_o = K(1 + \delta)(A \cos(\omega t + \theta))^2$$  \hspace{1cm} (17)

After eliminating the DC component, the result is

$$y(t) = K(1 + \delta) A^2 \left[ \cos(2\omega t + 2\theta) + \Delta \epsilon \right]$$  \hspace{1cm} (18)

where $\Delta \epsilon$ is the error constant from the DC elimination. By using a divide-by-2 frequency divider, (18) can be rewritten as

$$z(t) = K(1 + \delta) A^2 \left[ \cos\left((\omega + \Delta \omega) t + 2\theta\right) + \Delta \epsilon \right]$$  \hspace{1cm} (19)

where $\Delta \omega$ is the error frequency caused by the divide-by-2 frequency divider. By using the traditional analog multiplier phase detector, multiplying (19) by (8) thus yields

$$z(t) \cdot V_y = K(1 + \delta) A^2 \left[ \cos\left((\omega + \Delta \omega) t + 2\theta\right) + \Delta \epsilon \right] A \cos(\omega t + \theta) + \Delta \epsilon \cos(\omega t + \theta)$$  \hspace{1cm} (20)

By using LPF, the output of the proposed phase detector is

$$x_{\text{ilt}}(t) = K(1 + \delta) A^2 \left[ \cos(\Delta \omega t + \theta) \right]$$  \hspace{1cm} (21)

In the case of $\Delta \omega \neq 0$, the output in (21) is of a cosine function with the low frequency $\Delta \omega$, so it implies that the output amplitude will slowly swing along the x axis, which causes the incorrect demodulated information signal. Therefore, the divide-by-2 frequency divider must correctly regenerate the signal with the frequency of $\omega_{\text{dem}} = \frac{1}{2} \omega_m$ to aid the accurate demodulation scheme. In the case of $\Delta \omega = 0$, the relationship between the ideal output $x_1(t)$ in (7) of the proposed APDS and (21) is as follows
\[ x_s(t) = K(1 + \delta) x_c(t) \quad (22) \]

From (22), the ideal output in (7) is scaled by a constant factor of \( K(1 + \delta) \), which implies that the nonlinearity of the four-quadrant multiplier does not have any major effect on the proposed APDS and the impact of DC elimination is eliminated by the LPF.

3. The Proposed BPSK Demodulation Scheme with a Blind Carrier Recovery Method

3.1 Principle of BPSK transceiver

For the BPSK modulation scheme, binary data are represented by two signals with two different phases, which typically are 0 and \( \pi \). These signals, which have the same frequency and energy, are

\[ x_0(t) = A \cos(\omega_0 t), \quad \text{for } 1 \]
\[ x_1(t) = -A \cos(\omega_0 t), \quad \text{for } 0 \quad (24) \]

where \( A \) and \( \omega_0 \) are amplitude and angle frequency of the BPSK signal. The BPSK waveform whose phases are generally not continuous at the bit boundaries has a constant envelope and frequency. Unlike the simple conventional BPSK modulator, the coherent BPSK demodulator must generate the reference signal [16–18], which is synchronous to the received signal in frequency and phase in order to correctly demodulate the transmitted signal from the transmitter. For PSK signals, there is no spectral line at its carrier frequency, so there are two main types of carrier synchronizers, the \( M \)th power synchronizer, and the Costas loop [19]. The first method is the \( M \)th power device, which has the spectral line at \( Mf_c \). For BPSK, \( M = 2 \), thus it is a squaring loop. For QPSK, \( M = 4 \), so it is a quadrupling loop. The phase locked loop has been used as a tool to track and lock onto the frequency and phase of the \( Mf_c \) component. The divide-by-\( M \) device divides this component’s frequency in order to generate the desired carrier at \( f_c \).

![Fig. 7 The \( M \)th power synchronizer block diagram for carrier recovery](image)

From Fig. 7, let \( x(t) \) be the MPSK signal input of the \( M \)th power synchronizer, which is

\[ x(t) = \cos(2\pi f_c t + \theta) \quad (25) \]

where \( f_c \) and \( \theta \) are local frequency and phase of received MPSK signal respectively. After filtering by band-pass filter, the input has been fed to the \( M \)th power loop, it yields

\[ z(t) = \cos(2\pi Mf_c t + M\theta) \quad (26) \]

By feeding (26) as an input of the phase locked loop, the local carrier is generated as

\[ w(t) = \sin(2\pi Mf_c t + M\dot{\theta}) \quad (27) \]

where \( \dot{\theta} \) is phase of VCO output signal. Then dividing the component’s frequency of (27) by divide-by-\( M \) device and shifting the signal phase by 90 degrees, the recovered local carrier results as

\[ y(t) = \cos(2\pi f_c t + \dot{\theta}) \quad (28) \]

However, the difficulty in the circuit implementation of the \( M \)th power synchronizer is the \( M \)th power device, especially at the high frequencies. Therefore, the BPSK carrier recovery design of Costas loop [20–21] depicted in Fig. 8 can avoid this problem. Still, the complexity in Costas loop implementation is to maintain the balance between the I- and Q-channel. The two multipliers and low-pass filters in these two channels must be perfectly matched in order to achieve the theoretical performance. Moreover, its VCO has to generate a local carrier with a frequency close to the transmitted carrier frequency and some initial phase.

3.2 The proposed BPSK demodulation scheme

From Fig. 9, let \( x_{\text{BPSK}}(t) \) be the BPSK signal input, which is

\[ x_{\text{BPSK}}(t) = A \cos(\omega_0 t + \phi_0) \quad (29) \]

where \( A \), \( \omega_0 \) and \( \phi_0 \) are amplitude, angle frequency and phase of the BPSK signal input respectively. In order to detect the phase of the BPSK input \( x_{\text{BPSK}}(t) \), the analogue multiplier PD is used by following the steps from (3)-(6), it yields

\[ y_{\text{DATA}}(t) = \frac{A^3 \cos(\phi_0)}{4} \quad (30) \]

![Fig. 8 The Costas loop for carrier recovery for BPSK](image)
The block diagram of proposed BPSK demodulation scheme

The proposed APDS can be used as a BPSK demodulation scheme because it can simply recover the transmitted BPSK signal phase, which is the information data sent by the transmitter. Based on the proposed APDS, the proposed BPSK demodulation scheme with non-data aided carrier recovery method can avoid the synchronous problems of $M^{th}$ power loop, and the Costas loop.

4. The Proposed BPSK and QPSK Demodulation Schemes

4.1 Principle of QPSK transceiver

From Fig. 10, the quadrature phase shift keying (QPSK) is a digital modulation scheme which the phase $\phi_c$ of the modulated signal is shifted to the corresponding phase related with one of four possible two-bit input data. For example, the 4 phases are -135°, -45°, +45° or +135° for 00, 01, 10, and 11 input data, respectively.

According to this discussion, a generalized form of QPSK is modeled as follows:

$$\phi_{QPSK}(t) = A_t \cos(\omega_c t)$$

where $\phi_c = (2n + 1) \frac{\pi}{4}$, for $n = 0, 1, 2, 3$. $A_t$ and $\omega_c$ are the amplitude and frequency of the QPSK signal. By rewriting (31) in the quadrature form, it then yields

$$\phi_{QPSK}(t) = A_t [\cos(\phi_c) \cos(\omega_c t) - \sin(\phi_c) \sin(\omega_c t)]$$

From the equation (32), the QPSK signal can be generated by using two carriers, which are in-phase $\cos(\omega_c t)$ and quadrature $-\sin(\omega_c t)$. The quadrature carrier $-\sin(\omega_c t)$ is simply obtained by using 90°-phase shifter whose input is the in-phase $\cos(\omega_c t)$. At the receiver, the QPSK coherent demodulator depicted in Fig. 10 (b) must be provided in order to detect the binary stream back. Besides the local carrier must be regenerated, the 90°-phase shifter is also employed to generate the quadrature carrier.
4.2 The proposed QPSK demodulation scheme

From Fig. 12, let \( \phi_{QPSK}(t) \) be the input applied into the proposed phase detection scheme and \( x_c(t) \) be the output.

\[
\phi_{QPSK}(t) = A \cos(\omega_c t + \phi_0) \tag{33}
\]

where \( A \), \( \omega_c \) and \( \phi_0 \) are the amplitude, the angle frequency and the phase of QPSK signal respectively. By following the steps from (3) to (4), it yields

\[
y(t) = \frac{A^2 \cos(2\omega_c t + 2\phi_0)}{2} \tag{34}
\]

By using a divide-by-2 frequency divider, (34) can be rewritten as (35)

\[
z(t) = \frac{A^2 \cos(\omega_c t + 2\phi_0)}{2} \tag{35}
\]

Equation (35) can perform as the recovered carrier for the QPSK demodulator with blind carrier recovery method. In the case that the analogue multiplier PD is used by multiplying (35) with \( \phi_{QPSK}(t) \), it yields

\[
n(t) = \frac{A^2 \cos(2\omega_c t + 3\phi_0) + A^2 \cos(\phi_0)}{4} \tag{36}
\]

By using LPF, the low frequency component is obtained

\[
x_c(t) = \frac{A^2 \cos(\phi_0)}{4} \tag{37}
\]

4.3 The proposed QPSK demodulation scheme under the bandpass noise condition

In the section 4.2, the simulation was performed under noise free conditions, so it is imperative for the proposed scheme to be discussed and tested under the AWGN channel. From the block diagram of the QPSK-modulated system depicted in Fig. 13, the QPSK signal can be written as

\[
\phi_{QPSK} = A \cos[\omega_c t + \psi(t)] \tag{38}
\]

where \( \psi(t) = k_p m(t) \) is the signal phase, \( m(t) \) and \( k_p \) are the information signal and the constant, respectively. The channel noise \( n(t) \) at the demodulator input is a bandpass noise with the PSD \( S_n(\omega) \) and bandwidth \( 2(\Delta f + B) \).

The noise \( n(t) \) can be expressed in the term of quadrature components \([23]\) as

\[
n(t) = n_c(t) \cos(\omega_c t) + n_s(t) \sin(\omega_c t) \tag{39}
\]

where \( n_c(t) \) and \( n_s(t) \) are low-pass signals of bandwidth \( \Delta f_B \). This bandpass noise can be expressed in terms of amplitude \( E_n(t) \) and phase \( \theta_n(t) \) as given in Fig. 14.

\[
n(t) = E_n(t) \cos[\omega_c t + \theta_n(t)] \tag{40}
\]

For wide-band modulation, the signal \( m(t) \) changes very slowly relative to noise \( n(t) \). The modulating signal bandwidth is \( B \), and the noise bandwidth is \( 2(\Delta f + B) \). Hence, the phase and the frequency variations of the modulated carrier are much slower than the variation of \( m(t) \). In order to analyze the phase deviation caused by the noise at the output of the proposed system, the phasor diagram of the signal is constructed as given in Fig. 15.
The QPSK signal disturbed by the AWGN $x_i(t)$ has been fed as an input of the proposed QPSK demodulation scheme.

$$
x_i(t) = A \cos[\omega_i t + \psi(t)] + n(t)
$$

Equation (41)

where

$$
R(t) = \left[ \left[ A + E_n(t) \cos[\theta_0(t) - \psi(t)] \right]^2 + \left[ E_n(t) \sin[\theta_0(t) - \psi(t)] \right]^2 \right]^{1/2}
$$

Equation (42)

$$
\Delta \psi(t) = -\tan^{-1} \left[ \frac{E_n(t) \sin[\theta_0(t) - \psi(t)]}{A + E_n(t) \cos[\theta_0(t) - \psi(t)]} \right]
$$

Equation (43)

Applying (41) as an input of the proposed QPSK system, the output of the squaring is

$$
x^2_i(t) = R^2(t) \cos^2[\omega_i t + \psi(t) + \Delta \psi(t)]
$$

Equation (44)

After that the DC constant is removed, (44) can be rewritten as

$$
y(t) = \frac{R^2(t)}{2} \cos(2\omega_i t + 2\psi(t) + 2\Delta \psi(t))
$$

Equation (45)

By using the divide-by-2 frequency divider, the regenerated signal is expressed as

$$
z(t) = \frac{R^2(t)}{2} \cos(\omega_i t + 2\psi(t) + 2\Delta \psi(t))
$$

Equation (46)

In order to recover the signal’s phase and to less complex for the analysis, the conventional multiplier phase detector is applied, thus it yields

$$
z(t) \cdot x_i(t) = \frac{R^2(t)}{2} \cos[\omega_i t + 2\psi(t) + 2\Delta \psi(t)]
$$

Equation (47)

By using LPF, then it results as

$$
x_i(t) = \frac{R^2(t)}{4} \cos[\psi(t) + \Delta \psi(t)]
$$

Equation (48)

For the small noise case, where $E_n(t) \ll A$ and

$$
\Delta \psi(t) \leq \frac{\pi}{2}
$$

for all $t$, we can then assume that

$$
R(t) \ll A \text{ and } \Delta \psi(t) \ll \frac{E_n(t)}{A} \sin[\theta_0(t) - \psi(t)],
$$

and (48) can be rewritten as

$$
x_i(t) = \frac{R^2(t)}{4} \cos[\psi(t) + \Delta \psi(t)]
$$

Equation (49)

Note that the noise term $\Delta \psi(t)$ is a function of sine, whose range is between $[-1,1]$, multiplied by the factor of $\frac{E_n(t)}{A}$. With the condition of $E_n(t) \ll A$, it also causes the value of $\frac{E_n(t)}{A}$ to be less than a unit. Therefore, the noise term has minor impact towards the recovered information term.

5. Simulation Results

5.1 Results of the proposed phase detection algorithm

In the simulation, the characteristic results of the proposed absolute phase detector scheme without using the reference phase will be demonstrated. First, as depicted in Fig.16, the sinusoidal input given in Fig. 16 (a) is squaring to double the frequency and phase. Next, the DC offset in the squared signal is eliminated and then a divide-by-2 frequency divider is used in order to decrease half of the signal frequency, thus the output yields in Fig. 16 (b). After that the traditional analogue multiplier phase detection scheme, which is the combination of the multiplier and the LPF, detects the different phase from both input and reference signals (see Fig. 16 (d)). Therefore, the novel phase absolute detection scheme does not need any information about the reference phase in order to retrieve the signal phase. However, it should be concerned that the phase detection range of the proposed algorithm depends on the conventional PD used.

From (7), the proposed APDS’s output is represented in the cosine function which means that the cosine function value is not duplicative in the range of $0^\circ - 180^\circ$. In Fig. 17, the average output amplitude and $0 - 2\pi$ phase difference relationship of the proposed APDS shows that its phase detection range is from $0^\circ$ to $180^\circ$ depending on the analogue multiplier PD used. The approximate slope in the range of $(0 - \pi)$ X-axis can be calculated to -2.14. The negative slope indicates that the greater the phase differences are, the less the average output amplitudes becomes.
In order to expand the PD detection range, the Ex-OR PD is employed. The output of the proposed APDS is depicted in Fig. 18 (b) which is generated from the input sinusoid with the $\frac{\pi}{2}$ delay phase shown in Fig. 18(a). Both sinusoids are converted to be two square waves depicted in Fig. 18 (c) and (d) by using the comparators. In Fig. 18 (e), the phase differences from both square signals are produced by Ex-OR gate phase detector.

With the same procedures in the previous simulation illustrated in Fig. 18, the phase difference (from both square signals regenerated by using the comparators) depicted in Fig. 19 (e) are produced by Ex-OR gate phase detector. From both figures, the different phase value is directly proportional to input’s delay phase.

In Fig. 20, the characteristic of phase detection range is the slope $k_{\phi}$ plotted between average output amplitude value and phase difference value. From Fig. 20, the maximum output amplitude occurs at the 180° phase difference implying that the phase detection range of Ex-OR phase detector is between 0° and 180°.

5.2 Results of the proposed BPSK demodulation scheme

The BPSK signal depicted in Fig. 21 (b) is generated by using the 16-bit data [0 0 1 1 1 0 0 1 1 0 0 1 1 0 0 1] depicted Fig. 21 (a).
traditional PD as in the first simulation, Fig. 21 (c) and (d) represent the outputs of the divide-by-2 frequency divider and multiplier respectively.

Finally, the information data illustrated in Fig. 21 (e) is recovered by using the LPF. It should be noted that this simulation creates the BPSK demodulation scheme with a blind carrier recovery method based on the proposed PD scheme without using the reference phase and provides the accurately recovered 16-bit data.

5.3 Results of the proposed QPSK demodulation scheme

The QPSK signal is generated by using the 16-bit data [0 1 0 0 1 1 0 0 0 1 0 1 1 0 0] depicted Fig. 22 (a). To accurately detect the phase difference [Fig. 22 (f)] from these square-wave outputs of the comparators, instead of using the conventional PD, the PD which is the combination of the mono-stable multi-vibrator and the RS flip-flop, has been used because the range of this new combination PD is from 0° and 360°.

Fig. 20 The graph of average output amplitude and the different phase relationship

Fig. 21 The results of using the proposed phase detection algorithm without using the reference phase as a BPSK demodulation

Fig. 22 The results of using the proposed phase detection algorithm without using the reference phase as a BPSK demodulation

Fig. 23 The proposed QPSK demodulator’s simulation result according to the QPSK signal input disturbed by -30 dB noise power

After that, the four pulse-width sizes of the RS flip-flop output depicted in Fig. 22 (f) is the input of the matching procedure in order to regenerate the 16-bit data.

5.4 Results of the proposed QPSK demodulation scheme in the AWGN channel

A test simulation depicted in Fig. 23 was constructed followed by the QPSK demodulation scheme as in Fig.
and was investigated for the performance of the proposed QPSK demodulation scheme in additive white Gaussian noise (AWGN) channel. 

The inputs consisting of QPSK signals and Gaussian noise are fed to the proposed QPSK demodulation scheme. The evaluation of the proposed QPSK receiver’s performance includes the noise power levels of -30 dB, -28 dB and -25 dB illustrated in Fig. 23 (b), 24 (b) and 25 (b) respectively. For all simulation results, the top traces show the different 30-bit original data and the second traces show the AWGN signal with the power of -30 dB, -28 dB and -30 dB, respectively. In the third traces, the three inputs including QPSK signals with these noise powers were fed through the proposed QPSK demodulator in order to retrieve the original data bits. All bottom traces are the regenerated data bit plotted to compare with the original ones.

5.5 Results of the proposed QPSK demodulation scheme by using PSPICE simulation

In this section, this research presents the fundamental circuit simulation depicted in Fig. 26 by using the PSPICE simulation. According to the section 2.6 and 4.3, the discussion about the impact of the proposed system’s components and the impact of the AWGN in real time processing are provided, respectively.

Therefore, all simulation results in this section provide the essential knowhow to implement the actual circuit. These results are separated into three parts. In Fig. 27 and Fig. 28, the relationship between XOR’s output and the input phase, which agrees well with the result in Fig. 20, is confirmed.
Then the proposed BPSK-demodulated result, which is constructed by the same circuit in the previous simulation with 40 kHz-carrier BPSK input is given in Fig. 29. The result shows the 2-square-wave outputs depicted in the top trace (XOR) with the 2-different-size pulse widths distinguished by the data bit’s transition. Therefore, LPF and the matching process can be used for regenerating the data bits.

For real time processing of QPSK simulation depicted in Fig. 30, the false detected phases exist at every phase transition of the QPSK input signal. In this simulation, the multiplier, the DC eliminator, and the frequency divider work perfectly as illustrated by the signals in the Fig. 30. At the selected phase detection (mono-stable multi-vibrator and RS flip-flop) block in Fig. 12, both impulse trains in the top trace are generated correctly by the mono-stable multi-vibrator circuits. But it is found that the incorrect pulse width of square waves generated by the RS flip-flop occurred around the phase transition periods of the QPSK signal. Hence, the proposed scheme is incompatible with the real time processing for phase detection. But it works perfectly fine in the case of frame processing as depicted in Fig. 22, 23, 24 and 25.

6. Conclusions

With simple mathematical analysis, a novel absolute phase detection scheme is presented. Due to the variety of traditional PD-block in the proposed scheme, the flexibility of PD-range expansion is readily provided in order to suit the application’s purposes. Unlike the conventional phase detectors such as an analogue multiplier and the combination of mono-stable multi-vibrator and RS flip-flop, the proposed absolute PD absolutely detects the phase constant from the sinusoidal input without the prior reference phase requirement. By the analysis in section 2.6, it can be concluded that the divide-by-2 frequency divider has the most effect to the proposed scheme in comparison to the analog multiplier which its scale factor causes the amplitude variation of the output. Also the impact of the DC elimination procedure can be removed by the LPF in the conventional PD. With the PSPICE simulation, the total power consumption of the proposed APDS circuit is 427mW, which is most consumed by the multiplier (200mW) compared to other components.

For the proposed BPSK demodulation scheme, the analogue multiplier PD, which has the narrow phase detection range (0° - 180°), is selected for detecting the information data. In order to create the QPSK demodulation scheme, the combination of mono-stable multi-vibrator and RS flip-flop is required because the phase detection range needs to be expanded to 360° in order to avoid the ambiguity in data recovery. Based on the proposed absolute PD algorithm, it can be contributed as BPSK and QPSK demodulators. The results illustrate that both demodulating schemes implemented with a blind carrier recovery method can accurately recover the transmitted BPSK and QPSK signal phase, which are 16-bit data, respectively. Furthermore, both proposed demodulation schemes can avoid the synchronous conditions of Mth power loop,
and the Costas loop. Due to the analysis in the section 5.4, the analog multiplier PD was selected in order to verify the proposed QPSK demodulator under the AWGN conditions. The conclusion is the output phase is irrelevantly disturbed by additive white Gaussian noise. From the PSPICE results, it is noted that the false phase detection occurs at every phase transition of QPSK signal, so the proposed scheme for QPSK demodulator cannot be applied for the real time processing. However, the Matlab simulation results show that the proposed scheme for QPSK demodulator can be applied only for the frame processing case.

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Acknowledgment

We are so thankful for sharing the insight and expertise, which greatly assisted the research, from our colleagues. We are also immensely grateful to Journal of Signal Processing Editor and the reviewers for their very valuable comments and ideas on an earlier manuscript in order to improve our paper’s quality, although any mistakes are our own and should not harm the reputations of these esteemed persons.
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(Received January 14, 2016; revised May 25, 2016)