1. Introduction

Thin-film transistors (TFTs) have been investigated for many years and have shown great potential in applications such as large-area circuits, biochemical sensors, active-matrix flat panel displays, and radio-frequency identification tags.[1–3] It is generally accepted that the properties of the dielectric/transistor channel interface play a critical role in the electrical performance of TFTs.[4,5] An extremely common practice to improve the interface properties and electrical performance of organic TFTs is to apply a self-assembled monolayer (SAM), such as octadecyltrichlorosilane (OTS) and hexamethyldisilazane (HMDS), onto the gate dielectric, which enables tuning of the surface energy and reduction of the interface trap density.[6,7] A very large number of reports show that the carrier mobility and current on/off ratio of SAM-treated organic TFTs can be increased by orders of magnitude. SAM treatment has therefore become a standard process in organic TFT fabrication.[6–9] Despite such an effective treatment, to date it is still challenging for organic TFTs to obtain a carrier mobility comparable to that of oxide TFTs.

Similar to organic semiconductors, oxide semiconductors can also be deposited using solution processes. However, to obtain desirable electrical properties, the deposited films generally require high-temperature treatments,[10] which would damage SAMs. A far more common and industrial compatible method of depositing oxide semiconductors is sputtering. However, SAMs are typically less than 3 nm thick and their organic nature makes them less robust than inorganic films.[6,8] As a result, sputtering has rarely been used together with SAM treatment owing to the potential damage caused by the high energy ions in the plasma.[11] Although a previous paper showed that SAMs somewhat survived in the sputtering of InGaZnO (IGZO), the resulting TFTs displayed a carrier mobility less than 2 cm$^2$ V$^{-1}$ s$^{-1}$,[12] which is much lower than the typical carrier mobility ($\approx$10 cm$^2$ V$^{-1}$ s$^{-1}$) in IGZO TFTs reported in the literature. Furthermore, the mobility in the devices without the SAM treatment was not reported, making it impossible to determine whether the carrier mobility had been improved and if so, by how much.

We have recently demonstrated that by gating with solution-processed ultra-thin gate dielectrics (Al$_2$O$_3$ and HfO$_x$), IGZO TFTs are capable of operating under an ultra-low voltage of 1 V.[11–15] In this work, we explore the possibility of improving the performance of oxide TFTs by using a SAM treatment on the gate dielectric prior to the sputtering of oxide semiconductor. In order to study the possible plasma damage to the SAM during the sputtering, several sputtering powers and different dielectrics have been tested. The electrical characteristics in terms of the leakage current density, capacitance density,
interface trap density, and carrier mobility have been systematically studied to analyze the survival of the OTS layer after the sputtering. Under the optimized sputtering conditions, we are able to show that the OTS treatment on the Al$_x$O$_y$ dielectric enabled IGZO TFTs to show a significant performance enhancement, including a decrease of trap density by 50%, as well as an increase of current on/off ratio and carrier mobility by a factor of 76 and 2.3, respectively. Such a dramatic improvement in the dielectric/channel interface properties also enabled a substantial enhancement of device stability under bias stress. The optimized condition has also been used with OTS-treated thin HfO$_x$ gate dielectrics and the obtained IGZO TFTs show a mobility as high as 16 cm$^2$ V$^{-1}$ s$^{-1}$, which is increased by a factor of 2.1 compared with the devices gated with bare HfO$_x$.

Such an inexpensive and yet effective method might well be applicable to other sputtered oxide semiconductors and dielectrics, and it is possible that it may become a standard process in industry applications, such as manufacturing of display back plane drivers.

2. Results and Discussions

Figure 1a shows a schematic diagram of an IGZO TFT with an OTS treatment on anodized Al$_x$O$_y$. The chemical structure of OTS is shown in Figure 1b. The surface of the anodized film is hydrophilic with highly polar hydroxyl (–OH) groups and weakly adsorbed water molecules on the surface.\cite{15} By applying OTS, it could react with the hydroxyl groups on the surface and self-assemble a monolayer, resulting in a reduced surface polarity after the treatment.\cite{16} Hence, the surface of the film could be changed from hydrophilic to hydrophobic after the OTS treatment. As shown in Figure 1c, the contact angles before and after the deposition of OTS SAM were found to be 53$^\circ$ and 92$^\circ$, respectively, clearly showing that the surface of the film has been changed from hydrophilic to hydrophobic and suggesting a reduced –OH content.

The properties of the ultra-thin Al$_x$O$_y$ gate insulator with and without OTS treatment were first studied. Capacitance measurements were carried out using the structure shown in Figure 1d. At 100 kHz, a capacitance density of about 1000 nF cm$^{-2}$ was found in the Al/Al$_x$O$_y$/Al structure (Figure S1a,b, Supporting Information). After the application of OTS, the capacitance density was reduced to about 490 nF cm$^{-2}$ (Figure S1a,b, Supporting Information). The current density of the capacitors using bare Al$_x$O$_y$ and OTS-treated Al$_x$O$_y$ as the insulator is shown in Figure 1e. After the addition of the OTS layer, the leakage current density decreased by roughly three times and was less than 3.5 nA cm$^{-2}$ throughout the whole test. This confirms the formation of a monolayer and improved insulating properties.

The robustness of the films was tested by studying the breakdown voltage of the capacitors with bare and OTS-treated Al$_x$O$_y$. It was found that the breakdown voltage was 3.4 V for bare Al$_x$O$_y$ and 8.8 V for OTS-treated Al$_x$O$_y$, as shown in Figure S1c, Supporting Information. To analyze the vertical carrier transport mechanism of both types of insulators, the measured current was fitted with different models, as shown in Figure S1d,e, Supporting Information. The electron transport of bare Al$_x$O$_y$ was found to be dominated by Fowler–Nordheim (F–N) tunneling. However, in the case of OTS-treated Al$_x$O$_y$, most carriers get through the films via shallow traps and hence the dominant conduction mechanism was Poole–Frenkel (P–F) emission.

During the sputtering of IGZO on top of organic materials, plasma-induced damage may occur. A higher sputtering power not only means more energetic ion bombardments, but also...
higher deposition rate and thereby quicker coverage of the SAM. In order to study the dependence of possible damage to SAM on the sputtering power, transistors gated with bare $\text{Al}_x\text{O}_y$ (devices A, B, and C) and OTS-treated $\text{Al}_x\text{O}_y$ (devices D, E, and F) have been fabricated with IGZO channel layer sputtered at 25 W (devices A and D), 40 W (devices B and E), and 50 W (devices C and F). Figure 2a–f shows the transfer and output characteristics of the fabricated IGZO TFTs gated with bare $\text{Al}_x\text{O}_y$ and OTS-treated $\text{Al}_x\text{O}_y$. The obtained electrical characteristics of these devices are summarized in Table S1, Supporting Information. Here, only room-temperature deposited IGZO channel layers are studied, as the targeted area of using this method is flexible electronics. It was reported that IGZO TFTs could have an excellent device performance even with an IGZO layer deposited at room temperature.\[13,17–19\]

The comparisons between devices A and D, B and E, and C and F clearly show that the gate leakage current, $I_G$, of the TFTs gated with OTS-treated $\text{Al}_x\text{O}_y$ is much smaller than that of the TFTs gated with bare $\text{Al}_x\text{O}_y$, indicating superior insulating properties of the OTS-treated $\text{Al}_x\text{O}_y$ dielectric. Such a decrease of $I_G$ results in a decrease of off-current and hence an increase of current on/off ratio by more than one order of magnitude. In addition, a significant decrease in hysteresis is clearly seen after the OTS treatment, which is critical to many circuit applications. The water contact angles in Figure 1c show that the surface of the gate dielectric has been changed from hydrophilic to hydrophobic after the OTS treatment, indicating a decreased surface energy. Hence, a possible reason for the decreased hysteresis would be the application of OTS forming a less polar surface and thus reducing influence of surface hydroxyl groups and water vapor.\[20,21\] The subthreshold swing, $SS$, is found to be about 70 mV dec$^{-1}$ in all six devices, which is very close to the theoretical limit of $SS$ at 300 K.\[22\] This confirms a large insulator capacitance and a low interface trap density.

The capacitance of every device was measured by positively biasing the gate at +1 V so that the TFT was turned on and the semiconductor film did not contribute to the gate capacitance. At 100 Hz, the obtained capacitances in devices A, B, C, D, E, and F are 1090, 1130, 1080, 730, 560, and 580 nF cm$^{-2}$, respectively. A lower capacitance density is obtained in devices gated
with OTS-treated AlOx, suggesting that the OTS is not completely removed by the plasma and remains effective. The trap density, Dn, was then calculated using the following equation:

\[
D_n = \left[ \frac{SS \log(e)}{kT/q} - 1 \right] \frac{C}{q^2}
\]

where k is the Boltzmann constant, T is the temperature, \( q \) is the electron charge, and C is the capacitance per unit area. \( D_n \) is found to be between 1.2 \( \times 10^{12} \), 1.2 \( \times 10^{12} \), 1.1 \( \times 10^{12} \), 77 \( \times 10^{11} \), 4.8 \( \times 10^{11} \), and 8.6 \( \times 10^{11} \) cm\(^{-2}\)V\(^{-1}\) in devices A, B, C, D, E, and F, respectively. Since all the devices have a same IGZO thickness, the trap densities induced by the bulk and top surface are similar. Hence, the change of \( D_n \) here is mainly related to the change in density of interface states. It is noticed that although SS is almost the same for all the devices, owing to the decrease of gate capacitance, \( D_n \) is found to be much smaller in devices D, E, and F, suggesting a decrease of interface traps (Figure 2g).

It is found to be much smaller in devices D, E, and F, suggesting a decrease of interface traps (Figure 2g). By treating the surface of the as-deposited Al with OTS, it would react with the –OH groups, desorb the weakly adsorbed water molecules on the surface. It was previously reported that the hydroxyl groups and/or the water molecules at the dielectric/channel interface might function as the defects and trap carriers.\[16,23–26\] By treating the surface of the as-deposited AlOx with OTS, it would react with the –OH groups, desorb the weakly adsorbed water molecules and form a less polar surface with reduced interface trap states.\[16\]

As shown in Figure 2h, the threshold voltage, \( V_{TH} \), is found to be left-shifted after the OTS treatment of the device layer. The left shift of \( V_{TH} \) is mostly due to the increase in carrier density of IGZO caused by the hydrogen incorporation,\[27,28\] because the C–H bonds are not strong and might be broken during the IGZO sputtering. The decomposed components, such as H\(^+\), might be diffused into the IGZO channel layer, resulting in a reduced resistivity of IGZO film by providing additional electrons. Here, by taking the experimental data, the resistivity of IGZO on bare AlOx is estimated to be 2058 \( \Omega \) cm and the resistivity of IGZO on OTS-treated AlOx is estimated to be 1124 \( \Omega \) cm.

The mobility, \( \mu \), in the saturation regime can be derived from

\[
I_{D} = \frac{W}{2L} \mu C(V_{G} - V_{TH})^2
\]

where W/L is the channel width to length ratio and \( V_{G} \) is the gate voltage. As a result, the calculated \( \mu \) for devices A, B, C, D, E, and F are 4.9, 5, 8.2, 78, 13, and 9.6 cm\(^{2}\)V\(^{-1}\)s\(^{-1}\), respectively. A clear increase of mobility after the OTS treatment is shown in Figure 2i, and for the best devices the mobility is increased by a factor of 2.6 (comparison between devices B and E).

To further confirm if the improvement of the mobility is due to the improved interface quality, the devices gated with OTS-treated AlOx were annealed in air at 100 and 200 °C, both for 30 min. The transfer characteristics of the devices before and after the treatment are shown in Figure S2, Supporting Information. The 100 °C treatment does not degrade the device performance significantly mainly because the OTS is fully covered by the IGZO layer, which reduces the damage to the OTS layer. However, the device performance heavily drops after the 200 °C treatment. The subthreshold swing increases from 69 to 81 mV dec\(^{-1}\), suggesting a deteriorated interface owing to the damage to the OTS, which also explains the mobility drop by more than 50% and the hugely increased hysteresis. The results therefore demonstrated that the enhanced electrical performance is mainly due to the improved interface properties by the OTS treatment.

It was previously reported that the O\(_2\) plasma treatment could also remove the interface traps and improve device performance.\[29,30\] To compare the difference, IGZO TFTs gated with bare AlOx, O\(_2\) plasma-treated AlOx, and OTS-treated AlOx were fabricated, as shown in Figure S3, Supporting Information. Although O\(_2\) plasma treatment improves the device performance, the best device performance is found in devices with OTS treatment. A possible reason for it is that the OTS treatment could create a stable interlayer between AlOx and IGZO, and such an interlayer might have lower defect densities than bare AlOx and O\(_2\) plasma-treated AlOx. Also, owing to the addition of OTS, the thicker gate dielectric results in a decrease of leakage current and an increase of current on/off ratio compared with other two cases. The results therefore clearly demonstrated the advantages of using OTS-treated gate dielectrics.

The corresponding output characteristics of devices A, B, C, D, E, and F (Figure 2d–f) indicate that all TFTs work in n-type mode with linear, pinch-off and on-state regimes clearly shown. It is found that even though the gate capacitance is decreased after the OTS treatment, an increased on-current is achieved in all sputtering cases. This suggests improved interface properties owing to the OTS treatment and is in agreement with the decrease of \( D_n \). The combination of the highest \( \mu \), the lowest \( S_S \) and the lowest \( D_n \) is clearly seen in device E, which demonstrates that the use of 40 W for the sputtering of IGZO is the optimum deposition condition resulting in the minimum damage to the OTS layer.

Due to the difficulties in analyzing the chemical variation of the OTS surface as a function of IGZO sputtering powers after the formation of channel layers, we here measure the damage to the OTS layer by using electrical performance of IGZO TFTs. As shown in Figure 2g, unlike devices A, B, and C, \( D_n \) of devices D, E, and F changes with the IGZO sputtering power. A slightly higher \( D_n \) is obtained in device D than in device E, which might be due to a slightly more damaged OTS layer (much more disordered insulator/semiconductor interface) in device D. As the plasma damage occurs before the OTS layer is covered by the IGZO layer, the more severe damage to the OTS layer at a lower power may be attributed to the longer time required for IGZO to effectively cover the OTS. However, the comparison of \( D_n \) in devices E and F indicates that the worse interface quality was also obtained in the highest power case. This is likely due to the higher sputtering power resulting in Ar ions with higher energy, causing more damage to the OTS.

The comparison in terms of mobility of the devices also agrees well with this conclusion. While devices A, B, and C show an increase of mobility with sputtering power owing to the increase of indium composition and carrier concentration,\[31,32\] the highest mobility among OTS-treated AlOx/IGZO TFTs is achieved in device E instead of device F. This suggests...
that a worse dielectric/channel interface quality is present in device F, which could be due to more severe damage to the OTS layer caused by the strong plasma.

To investigate the damage to OTS layer due to sputtering further, parallel plate structures using Al/AlOy/OTS/IGZO/Al (Figure S4a, Supporting Information), Al/AlOy/OTS/Al (Figure S4b, Supporting Information), and Al/AlOy/IGZO/Al (Figure S4c, Supporting Information) have been fabricated. Regardless of the IGZO deposition power, devices with OTS-treated AlOy show lower current densities than the devices without OTS treatment (Figure S4d, Supporting Information). This indicates that the OTS SAM is at least not completely destroyed during the sputtering process. At an applied voltage of 1 V, the current density in devices using 25 and 50 W sputtered IGZO is double that of the devices without IGZO, which may be caused by a greater level of damage to OTS layers at these two sputtering powers. Similar current density is observed in the device without IGZO and the device using 40 W sputtered IGZO, indicating less damage to the OTS layer when using 40 W to sputter IGZO, in agreement with the results shown in Figure 2. For devices using 40 W sputtered IGZO, eight devices that were fabricated in different batches have been randomly chosen from 40 devices to test the current density. Similar current densities are found for all devices, demonstrating good uniformity and reproducibility (Figure S4e, Supporting Information).

The study of the uniformity and reproducibility of the 40 W sputtered IGZO TFTs was performed on ten OTS-treated AlOy/IGZO TFTs that were fabricated in different batches (Figure S5, Supporting Information). The devices show similar behaviors including a current on/off ratio of $(2.7 \pm 1.5) \times 10^3$, a mobility of $1.17 \pm 1.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, a subthreshold swing of $68 \pm 3 \text{ mV} \text{ dec}^{-1}$ and a threshold voltage of $0.3 \pm 0.09 \text{ V}$.

The device performance was then compared with previously reported oxide TFTs gated with solution-processed, ultra-thin dielectric layers (Table S2, Supporting Information). The comparison in terms of mobility, current on/off ratio, subthreshold swing, and operating voltage clearly show that our devices are one of the best reported to date (Table S2, Supporting Information).[13,14,33–35]

To study the role of the OTS interlayer on the device operational stability further, both types of devices (i.e., without and with OTS treatment) were positively biased at $V_G = +1 \text{ V}$ for 3000 s and the obtained results are shown in Figure 3. The devices gated with OTS-treated AlOy maintain a current on/off ratio of about $10^2$ and a maximum leakage current less than 0.1 nA throughout the whole test. This is much better than the devices gated with bare AlOy and suggests that a stable OTS layer is formed at the dielectric/channel interface. After a bias stress of 3000 s, the threshold voltage for the device gated with bare AlOy shifts by approximately $0.17 \text{ V}$ from 0.46 to 0.63 V, which is 0.06 V more than the threshold voltage shift of the device using OTS-treated AlOy. Both types of devices show little change of mobility after bias stress, but the mobility degradation in the device gated with OTS-treated AlOy is 20 times smaller than that of the device with bare AlOy. The devices were also negatively biased at $V_G = -1 \text{ V}$ for 3000 s, as shown in Figure S6, Supporting Information. Both devices show a left shift of threshold voltage due to the bias stress, but the change of threshold voltage is 20% less in the case of using OTS-treated AlOy, as shown in Figure S6c, Supporting Information. The results clearly demonstrate improved dielectric/channel interface properties owing to the effective OTS treatment.

To investigate whether such a treatment works with other gate dielectrics in improving transistor performance, IGZO TFTs gated with 2.5 V anodized HfOy (with and without OTS treatment) were also fabricated. The obtained electrical properties of both types of transistors are shown in Figure 4. HfOy is a common high dielectric constant ($\kappa$) gate insulator, with $\kappa$ as high as 20–25, much higher than SiO$_2$ ($\kappa = 3.9$) and AlOy ($\kappa = 9$).

Owing to the improved insulating properties, TFTs gated with OTS-treated HfOy showed a decreased leakage current and hence a decreased off-current. The on-current of the device improved after the OTS treatment, even though the gate capacitance is decreased from 1300 to 700 nF cm$^{-2}$ (measured in a TFT structure at 100 Hz by biasing the gate at $+1 \text{ V}$), suggesting an improved interface quality. To verify this, $D_H$ of both devices was calculated. With the use of the subthreshold swing values (73 mV dec$^{-1}$ for TFTs gated with bare HfOy and 69 mV dec$^{-1}$ for TFTs gated with OTS-treated HfOy), $D_H$ is found to be $1.8 \times 10^{12}$ and $6.7 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, respectively, showing a reduction of $D_H$ by more than 60% because of the effective OTS treatment. Similar to the case of AlOy, the anodized HfOy films may contain some defects (i.e., $\cdot$OH groups and adsorbed water molecules) at the surface. With the OTS treatment, the traps are passivated, resulting in a decreased interface trap density, and hence an increase of on-current. The carrier mobility is found to increase by a factor of 2.1 from 78 to 16 cm$^2$ V$^{-1}$ s$^{-1}$ after the OTS treatment. Such a carrier mobility is comparable to or better than that of low-voltage IGZO TFTs reported previously.[15,33,36,37]
Both types of the devices were then tested under bias stress conditions, as shown in Figure 5. The untreated devices show an increase of subthreshold swing after the bias stress, which can be explained by the stress-induced traps at the dielectric/channel interface. However, the OTS-treated devices show negligible change of subthreshold swing throughout the whole bias stress test, suggesting the creation of trap states at the dielectric/channel interface induced by the gate bias stress is negligible.[38] Also, the untreated devices show a large threshold voltage shift of +0.21 V after the bias stress, while only +0.06 V of threshold voltage shift is found in the case of using OTS-treated HfO$_x$. Furthermore, OTS-treated devices show about 5.3 times more resilience to carrier mobility degradation and maintain a high mobility of 15 cm$^2$Vs$^{-1}$ even after being stressed for 3000 s, which nearly triples the mobility of the untreated devices (5.2 cm$^2$Vs$^{-1}$ after the bias stress).

3. Conclusion

In this work, the effectiveness of a SAM treatment on gate dielectrics (Al$_x$O$_y$ and HfO$_x$) has been explored in TFTs with a sputtered oxide semiconductor channel layer. The results show that depending on the IGZO sputtering power the damage to the OTS SAM can be minimized and effectively controlled. Under the optimal conditions, a significant increase in electrical performance of TFTs has been achieved. This includes a more than twofold increase of carrier mobility, an increase of current on/off ratio by approximately two orders of magnitude, and a reduction of trap density by more than 50%. Such a hugely reduced trap density also dramatically improves bias stress stability, which is one of the issues of oxide semiconductors. This work demonstrates a convenient and yet effective method to substantially improve the performance of IGZO.
TFTs, which may have potential applications in oxide-semiconductor-based electronics.

4. Experimental Section

Gate/Dielectric: To fabricate Al$_2$O$_3$, first a 200 nm thick Al layer was thermally evaporated onto a glass substrate as the gate electrode. Next, approximately 3 nm thick Al$_2$O$_3$ was grown by anodizing the Al gate lines in 1 M citric acid using the process conditions reported previously. For Hf/HfO$_x$ first a 100 nm thick layer of Hf was sputtered as the gate electrode using radio frequency (RF) magnetron sputtering at 45 W in pure argon atmosphere. Then, the Hf gate lines were anodized applying 2.5 V in 1 M citric acid. The thickness of the formed HfO$_x$ layer was found to be approximately 11 nm.

OTS Treatment: The anodized gate dielectrics were then treated by spin coating of 0.1 wt% n-octadecytrichlorosilane (OTS) in trichloroethylene (TCE) in ambient conditions. IGZO TFTs: A 25 nm thick IGZO (In:Ga:Zn = 1:1:1) channel layer was deposited on top of the formed gate/dielectric layers by RF magnetron sputtering in pure argon ambient at room temperature. Three different IGZO sputtering powers were used, which were 25, 40 and 50 W. Finally, 150 nm thick Al source/drain electrodes were thermally evaporated through a shadow mask. The channel length and width of all the devices were 60 µm and 2 mm, respectively.

Measurement: The electrical characteristics of the devices were measured using an Agilent E5270B semiconductor analyzer and an Agilent E4980A LCR meter at room temperature. C–V, C–f, and J–V characteristics, and linear fitting of leakage current (Figure S1, Supporting Information), electrical properties obtained for IGZO TFTs gated with bare Al$_2$O$_3$ and OTS-treated Al$_2$O$_3$ (Table S1, Supporting Information), transfer characteristics of IGZO TFTs with Al$_2$O$_3$ treated with different methods (Figure S2, Supporting Information), post-annealing treatment (Figure S3, Supporting Information), current density (Figure S4, Supporting Information), statistical information (Figure S5, Supporting Information), comparison of oxide-semiconductor-based TFTs gated with solution-processed, ultrathin dielectric layer (Table S2, Supporting Information), and negative bias stress measurement (Figure S6, Supporting Information).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

interface treatment, octadecytrichlorosilane, oxide semiconductors, self-assembled monolayers, thin-film transistors
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