Cyclic Coding Algorithms under MorphoSys Reconfigurable Computing System

Hassan Diab  
diab@aub.edu.lb  
Department of ECE  
Faculty of Eng’g and Architecture  
American University of Beirut  
P.O. Box 11-0236  
Beirut, Lebanon

Issam Damaj  
damajiw@sbu.ac.uk  
Faculty of Eng’g, Science and Technology  
South Bank University  
103 Borough RD  
SE1 0AA  
London, U.K.

ABSTRACT: This paper introduces reconfigurable computing (RC) and specifically chooses one of the prototypes in this field, MorphoSys (M1) [1 - 5]. The paper addresses the results obtained when using RC in mapping algorithms pertaining to digital coding in relation to previous research [6 - 10]. The chosen algorithms relate to cyclic coding techniques, namely the CCITT CRC-16 and the CRC-16. A performance analysis study of the M1 RC system is also presented to evaluate the efficiency of the algorithm execution on the M1 system. For comparison purposes, three other systems where used to map the same algorithms showing the advantages and disadvantages of each compared with the M1 system. The algorithms were run on the 8x8 RC (reconfigurable) array of the M1 (MorphoSys) system; numerical examples were simulated to validate our results, using the MorphoSys mULATE program, which simulates MorphoSys operations.

Keywords: Reconfigurable Computing, MorphoSys, Information Coding, Cyclic Codes, Algorithms Mapping.

1. INTRODUCTION

Reconfigurable computing (RC) is becoming more popular and increasing research efforts are being invested in it [1-10]. It employs reconfigurable hardware and programmable processors. The user designs the program in a way where the workload is divided between the general-purpose processor and the reconfigurable device. The use of RC paves the way for an increased speed over general-purpose processors and a wider functionality than Application Specific Integrated Circuits (ASICs). It is a solution for applications requiring a wide range of functionality and speed [1]. RC Systems represent a solution to the inflexibility of ASICs on one end of the computing spectrum, and the inefficiency of General Purpose Processors (GPPs) on the other end of the spectrum. Reconfigurable computers (RCs) offer the potential to greatly accelerate the execution of a wide variety of applications. Its key feature is the ability to perform computations in hardware to increase performance, while retaining much of the flexibility of a software solution.

2. MORPHOSYS DESIGN

One of the emerging RC systems includes the MorphoSys designed and implemented at the University of California, Irvine. It has the block diagram shown in Figure 1 [2] and is composed of: 1) an array of reconfigurable cells called the RC array, 2) its configuration data memory called context memory, 3) a control processor (TinyRISC), 4) a data buffer called the frame buffer, and 5) a DMA controller [2]. A program runs on MorphoSys in the following manner: General-purpose operations are handled by the TinyRISC processor, while operations that have a certain degree of parallelism, regularity, or intensive computations are mapped to the RC array.
The TinyRISC processor controls, through the DMA controller, the loading of the context words to context memory. These context words define the function and connectivity of the cells in the RC array. The processor also initiates the loading of application data, such as image frames, from main memory to the frame buffer. This is also done through the DMA controller. Now that both configuration and application data are ready, the TinyRISC processor instructs the RC array to start execution. The RC array performs the needed operation on the application data and writes it back to the frame buffer. The RC array loads new application data from the frame buffer and possibly new configuration data from context memory. Since the frame buffer is divided into two sets, new application data can be loaded into it without interrupting the operation of the RC array. Configuration data is also loaded into context memory without interrupting RC array operation. This causes MorphoSys to achieve high speeds of execution [3].

3. RECONFIGURABLE DEVICE

As stated earlier, the reconfigurable device in MorphoSys is the RC array divided into four quadrants. It has the design and interconnection shown in Figure 2 [2]. The interconnection network is built on three hierarchical levels. The first is a nearest neighbor layer that connects the RCs in a 2-D mesh. The second is an intra-quadrant connection that connects a specific RC to any other RC in its row or column in the same quadrant. The third is an inter-quadrant connection that carries data from any one cell (out of four) in a row (or column) of a quadrant to other cells in an adjacent quadrant but in the same row (or column) [4].

The context words loaded into context memory configure the function of the RCs as well as the interconnection, thus specifying where their input is from and where their output will be written to [5]. MorphoSys is designed in a way where all the cells in the same row perform the same function and have the same connection scheme (in row context broadcast mode), or all the cells in the same column perform the same function and have the same connection scheme (in column context broadcast mode). All the cells of a row or of a column share the same configuration [5].

4. CODING ALGORITHMS UNDER MORPHOSYS

Reconfigurable hardware implementation of digital coding algorithms has been an active area of research [6 - 10]. Many coding algorithms where mapped onto the M1. Research done to date includes: performance study of coding algorithms (checksum), pipelined implementation of various non-standard linear sequential coding circuits, and other algorithms [8,10]. The linear sequential circuits considered here are finite state machines with a finite number of inputs and outputs. The inputs, outputs and state transition occur at discrete intervals of time. The elements used are adders (EX-OR) and the delays (D) to delay input words. A sequence of 0s and 1s can be expressed by a polynomial in which the 0s and 1s are coefficients of the powers of a dummy variable. Hence, the sequence 11001 can be written as:

$$1D^4 \oplus 1D^3 \oplus 0D^2 \oplus 0D^1 \oplus 1D^0$$

This representation is the basis of the Feed Forward Binary Circuits, which are very useful in coding techniques. A generalized form, shown in Figure 3, of these circuits is represented by

$$T(D) = (1 \oplus D^1 \oplus D^2 \oplus D^3)$$

This circuit is used to code any stream of input vector X and yields a set of outputs Y. Therefore, the input vector X is a vector of 0s and 1s and the output is the coded output Y
vector, which is the result of multiplying the input polynomial (vector) $X$ with the polynomial represented by $T(D)$. This could be generalized to take the form:

$$y_k = \sum_{j=0}^{N} \oplus x_{k-j} D^j,$$

or, finally

$$Y = (\sum_{j=0}^{N} \oplus D^j) X \text{ i.e. } Y = (D^0 \oplus D^1 \oplus D^2 \oplus \ldots \oplus D^N) X$$

Where, $N$ is the number of stages of the circuit, and $X$ is of the form $X = x_0 \ldots x_{k-1}x_k$ with $x_k$ being the first bit to enter the multiplier circuit. This paper focuses on the hardware implementation of cyclic redundancy codes checkers (CRCCs) with their standard circuits, namely the CRC-16 circuits.

5. CYCLIC REDUNDANCY CODES

Redundant encoding is a method of error detection that spreads the information across more bits than the original data. The more redundant bits used, the greater the chance to detect errors. CRCCs are check for differences between transmitted data and the original data. CRCCs are effective for two reasons: Firstly, they provide excellent protection against common errors, such as burst errors where consecutive bits in a data stream are corrupted during transmission. Secondly, systems that use CRCCs are easy to implement [11]. When a CRCC is used to verify a frame of data, the frame is treated as one very large binary number, which is then divided by a generator number. This division produces a reminder, which is transmitted along with the data. At the receiving end, the data is divided by the same generator number and the remainder is compared with the one sent at the end of the data frame. If the two remainders are different, then an error occurred during data transmission. Types of errors that a CRCC detects depend on the generator polynomial. Table 1 shows the most common generator polynomials.

5.1. CRC Serial Implementation

CRC implementation is usually done with linear-feedback shift registers (LFSRs). Figures 4 and 5 show the CCITT CRC-16 and CRC-16 generators with their serial implementation using LFSR. This serial method works well when the data is available in bit-stream form.

5.2. CRC Parallel Implementation

With the currently available high-speed digital signal processing (DSP) systems, the processing of data is done in a byte, word, double word, or larger widths rather than serially. Even with serial telecommunication systems, data is buffered in chips responsible for synchronizations and framing. For parallel implementation the data is available in 8-bit frames with manageable speed [11]. A one channel parallel CRC algorithm with LFSR approach is done by considering the state of the circuit on 8-shifts basis [11-12]. Tables 2-3 show two different implementations of the CCITT CRC-16 and CRC-16, respectively. The term Register, represents the LFSR internal register numbered “i”, while $XOR_i$ represents the output of the $XOR$ gate number “i”, and $XOR$ indicates the XOR operation. With the emergence of the highly scalable reconfigurable circuits, more implementation capabilities are present. Along with the byte-wise or word-wise CRC implementation it is possible to implement parallel channels each with byte-wise CRC implementation.
6. ALGORITHMS MAPPING

From the underlying architecture point of view, the mapping of any algorithm onto the proposed reconfigurable system requires in-depth knowledge of all the available interconnection topologies. Moreover, the designer should take into consideration the possibility of dynamically changing the shape of the interconnection. From the algorithmic point of view, the design of a parallel version of the addressed algorithms requires the best use of resources with the least possible redundancy in computations.

Three sets of data are required to map any algorithm onto the M1 system. The first set specifies the intended shapes of interconnections that are going to be used. The second set is the manipulated data. Lastly, the last set of code is the TinyRISC code that will orchestrate the load/save operations, parallel computations, and changing the interconnection pattern through the context words.

6.1. The CCITT CRC-16 Algorithm Mapping

The mapping of the parallel CCITT CRC-16 algorithm will make use of the redundant computations utilized in several steps of the algorithm. Firstly, the values of $XOR_i$ for all values of $i$ from 0 to 7 are calculated. In Table 2 the computations that are used more than once are shown. Particularly, the redundant values are $(XOR_{i+4} \oplus XOR_i)$ for $i$ from 0 to 3. Thus, the second computation step involve registers 4, 5, 6, 11, 12, 13, 14, and 15 depending on results found in the first step. In the final step the computations for registers 0,1,2,3,7,8,9 and 10 are carried out depending on the results calculated in the first and second step.

The algorithm mapping will be explained by introducing the three needed sets of code. The first set is the interconnection context words. The context word used in this algorithm is that for XOR with column broadcast, where each cell XORs two inputs from frame buffers A and B. This context word is stored at address 30000\text{hex}.

The second set of code is the input data and the initial data in the circuits registers. These two sets of data are stored in main memory address 10000\text{hex} and 20000\text{hex}.

The third set is that of the TinyRISC code, which is the main code. This code and its discussion are shown in Table 4. Main steps of the addressed algorithm are shown in Figures 6 and 7. The final contents of frame buffer A is shown in Figure 8.

6.2. The CRC-16 Algorithm Mapping

The mapping of this algorithm depends also on eliminating redundant computations, besides, the parallel computation of the required values. This mapping is of three steps. Firstly, the values of $XOR_i$ for all values of $i$ from 0 to 7 are calculated. From Table 3 the computations used more than once are shaded, particularly, the redundant value $X$ ($XOR_0 \oplus \ldots \oplus XOR_7$). Thus, the second computation step is for $X$. Thirdly, the rest of the values are calculated in parallel.

The algorithm mapping will be explained by introducing the three needed sets of code. The first set is the interconnection context words. The context words used in this algorithm are firstly, that for XOR with column broadcast, where each cell XORs two inputs from frame buffers A and B. Secondly, the same cell operation is used also by taking one input from the frame buffer, and the second from the output of the left adjacent cell. The context words are stored at address 30000\text{hex}. The second set of code is the input data and the initial data in the circuits registers. These two sets of data are stored in main memory address 10000\text{hex} and
20000_{\text{hex}}. The third set is that of the TinyRISC code which is the main code, this code and its discussion are shown in Table 5. Main steps of the addressed algorithm are shown in Figures 9 and 10. The final contents of frame buffer A is shown in Figure 11.

### 7. PERFORMANCE EVALUATION AND ANALYSIS

The performance is based on the execution speed of the algorithms presented in sections 6.1 and 6.2 corresponding to Tables 2 and 3 respectively, which show the states of the registers after 8 shifts. The MorphoSys system is considered to be operational at a frequency of 100 MHz.

The algorithm in Table 4 (CRC-CCITT-16 Parallel Algorithm for a single channel) takes 30 cycles to complete. The speed in bits per cycle of the algorithm of Table 4 is equal to 0.267 bits/cycles i.e. 3.75 cycles for each bit. The time for the algorithm to terminate is equal to 0.3 \( \mu \)sec, and the data rate is 26.67 Mbps.

The algorithm in Table 5 (CRC-16 Parallel Algorithm for a single channel) takes 26 cycles in order to terminate. The cycle time for the MorphoSys is equal to 10 nsec. Thus, the speed in bits per cycle of the algorithm of Table 5 is equal to 0.307 bits/cycles i.e. 3.25 cycles for each bit. The time for the algorithm to terminate is equal to 0.26 \( \mu \)sec, and then the rate in Mega bits per second (Mbps) is 30.76 Mbps.

Furthermore, a comparison is done with the same algorithms mapped onto some Intel microprocessing systems. In this research the chosen processors are the Intel 80486 and Pentium. Note that the instructions used are upward compatible with newer Intel processors. The code and discussion of the same algorithms in Tables 4 and 5 are shown in Tables 6 and 7 respectively. Note that the chosen systems have comparable frequencies of 100 ~ 133 MHz.

In addition to Intel systems, the RC-1000 FPGA is used for performance comparisons. The Celoxica RC1000 board provides high-performance, real-time processing capabilities and is optimized for the Celoxica DK1 design suite. The RC1000 is a standard PCI bus card equipped with a Xilinx\textsuperscript{a}® Virtex\textsuperscript{TM} family BG560 part with up to 2 million system gates. It has 8MB of SRAM directly connected to the FPGA in four 32-bit wide memory banks. The memory is also visible to the host CPU across the PCI bus as if it were normal memory. Each of the 4 banks may be granted to either the host SRAM on the board. It is then accessible to the FPGA directly and to the host CPU either by DMA transfers across the PCI bus or simply as a virtual address. Comparisons among those systems are shown in Tables 8 and 9.

For the maximum exploitation of the M1 capabilities, it should be noted that the M1 data items are byte-wise (8 bits). Thus, the M1 can calculate in parallel the input of up to 8-channels simultaneously. This is also shown in Tables 8 and 9. Note that the FPGA RC-1000 findings are the same for a single channel or 8-channels input because of its scalability. The speedup factors, besides the other chosen metrics, show the superiority of the used reconfigurable computing systems. The speedup factor is considered to be the ratio between the cycle times of the suggested systems.

### 8. CONCLUSION

New mapping algorithms are introduced dealing with coding operations and its performance analysis under MorphoSys is proposed. Many findings besides the speed of these mappings are calculated, and results are compared with other processing systems. The cyclic coding
algorithms are presented with their mapping onto the M1. Accordingly, speeds of 213.13 Mbps for the CRC-CCITT-16 and 246.15 Mbps for the CRC-16 were achieved. The speedup factors (ratio of number of clocks) ranged from 4.26 to 58.46 between the M1 and the Intel processing systems. Moreover, the speed up factors between the RC-1000 and the M1 were up to 3.75. Future efforts could be invested in trying to map other algorithms that make use of the already mapped ones for more advanced algorithms for digital coding. The current research includes the work with other cyclic redundancy check algorithms along with other state-of-the-art coding methods. Also, comparisons could be made with results available on other parallel processors.
REFERENCES

[1] Abdennour E, Diab H, and Kurdahi F. FIR filter mapping and performance analysis on MorphoSys. Beirut: 7th IEEE International Conference on Electronics, Circuits and Systems, 2000; (1): 99-102.

[2] Lu G, Singh H, Lee M, Bagherzadeh N, and Kurdahi F. The morphosys parallel reconfigurable system. Toulouse: the 5th International Euro-Par Conference, 1999; 727-730.

[3] Maestre R, Kurdahi F, Bagherzadeh N, Singh H, Hermida R., and Fernandez N. Kernel Scheduling in Reconfigurable Computing. Munich: Design and Test in Europe, 1999; 90-96.

[4] Maestre R, Kurdahi F, Fernandez M, Hermida R, Bagherzadeh N, Singh H. A framework for reconfigurable computing: task scheduling and context management, IEEE Transactions on VLSI Systems 2001; 6(9) 858-873.

[5] Singh H, Lu G, Lee M, Filho E, Maestre R, Kurdahi F, Bagherzadeh N. MorphoSys: Case study of a reconfigurable computing system targeting multimedia applications. California: Design Automation Conference, 2000; 573-578.

[6] Damaj I, Diab H. Performance evaluation of linear algebraic functions using reconfigurable computing. International Journal of Super Computing (Accepted).

[7] Damaj I, Diab H. Performance analysis of extended vector-scalar operations using reconfigurable computing. Beirut: International Conference of Computer Systems and Applications, 2001; (1):270-274.

[8] Diab H, Damaj I, Zomaya A. New applications on state-of-the-art RC multiprocessing systems. Beirut: International Conference on Research Trends in Science and Technology, 2002.

[9] Diab H, I. Damaj. Architectural modifications for optimizing mappings on MorphoSys RC-system. Las Vegas: International Conference on Parallel and Distributed Processing Techniques and Applications, 2002; 1528-1534.

[10] Diab H, Damaj I. New digital coding algorithms under MorphoSys. Dhahran: The 6th Saudi Engineering Conference, 2002 (Accepted).

[11] Lee R. Cyclic Code Redundancy. Digital Design 1987.

[12] Perez A. Byte-wise CRC Calculations. IEEE Micro 1983; 40-50.
Biographies

Biography for Hassan Diab

Hassan Diab received his B.Sc. in Communications Engineering, M.Sc. in Systems Engineering, and Ph.D. in Computer Engineering. He is a Professor of Electrical and Computer Engineering at the American University of Beirut, Lebanon. He has over 90 publications in international journals and conferences. His research interests include performance evaluation of parallel processing systems, reconfigurable computing, and simulation of parallel applications. Professor Diab is a Fellow of IEE and IEAust and a Senior Member of IEEE.

Biography for Issam Damaj

Issam Damaj received his B.Eng. in Computer Engineering, M.Eng. in Computer and Communications Engineering, and is currently a Ph.D. student at South Bank University, London. He is a Teaching Assistant in the Faculty of Engineering, Science and Technology at South Bank University, London. His research interests include reconfigurable computing, H.W./S.W. Co-Design, fuzzy logic, and wireless communications security. He is a Member of the IEEE.
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Figure 2. RC Array Interconnection.
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Figure 4. LFSR implementation of the CCITT CRC-16
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Figure 5. LFSR implementation of the CRC-16
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| Columns Rows | C₀   | C₁ | C₂ | C₃ | C₄ | C₅ | C₆ | C₇ |
|--------------|------|----|----|----|----|----|----|----|
| R₀           | Register₀ ⊕ DataIn₀ |    |    |    |    |    |    |    |
| R₁           | Register₁ ⊕ DataIn₁ |    |    |    |    |    |    |    |
| R₂           | Register₂ ⊕ DataIn₂ |    |    |    |    |    |    |    |
| R₃           | Register₃ ⊕ DataIn₃ |    |    |    |    |    |    |    |
| R₄           | Register₄ ⊕ DataIn₄ |    |    |    |    |    |    |    |
| R₅           | Register₅ ⊕ DataIn₅ |    |    |    |    |    |    |    |
| R₆           | Register₆ ⊕ DataIn₆ |    |    |    |    |    |    |    |
| R₇           | Register₇ ⊕ DataIn₇ |    |    |    |    |    |    |    |

Figure 6. RC array contents after calculating for XORᵢ.
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| Rows | Columns | C₀   | C₁   | C₂   | C₃   | C₄   | C₅   | C₆   | C₇   |
|------|---------|------|------|------|------|------|------|------|------|
| R₀   | XOR₀ ⊕ XOR₀ | .    | .    | .    | .    | .    | .    | .    | .    |
| R₁   | XOR₁ ⊕ XOR₁ | .    | .    | .    | .    | .    | .    | .    | .    |
| R₂   | XOR₂ ⊕ XOR₂ | .    | .    | .    | .    | .    | .    | .    | .    |
| R₃   | XOR₃ ⊕ XOR₃ | .    | .    | .    | .    | .    | .    | .    | .    |
| R₄   | .        | .    | .    | .    | .    | .    | .    | .    | .    |
| R₅   | .        | .    | .    | .    | .    | .    | .    | .    | .    |
| R₆   | .        | .    | .    | .    | .    | .    | .    | .    | .    |
| R₇   | .        | .    | .    | .    | .    | .    | .    | .    | .    |

Figure 7. RC array contents for the second computation step for CRC-CCITT-16.
Figure 8. Contents of Frame Buffer A after the algorithm terminates after one computation step the new registers values are shown at the specified locations.

| Address In HEX | Frame Buffer A | Address In HEX | Frame Buffer A |
|----------------|----------------|----------------|----------------|
| 0              | DataIn₀        | 40             | Register₀      |
| 1              | DataIn₁        | 41             | Register₁      |
| 2              | DataIn₂        | 42             | Register₂      |
| 3              | DataIn₃        | .              | .              |
| 4              | DataIn₄        | 50             | Register₄      |
| 5              | DataIn₅        | 51             | Registers      |
| 6              | DataIn₆        | 52             | Registers      |
| 7              | DataIn₇        | .              | .              |
| 8              | X₉OR           | 55             | Register₈      |
| 9              | X₉OR           | 56             | Register₉      |
| 10             | X₉OR           | 57             | Register₁₀     |
| 11             | X₉OR           | 60             | Register₃      |
| 12             | X₉OR           | 65             | Register₇      |
| 13             | X₉OR / Register₁₁ | .            | .              |
| 14             | X₉OR           | .              | .              |
| 15             | X₉OR           | .              | .              |
| 16             | X₉OR           | .              | .              |
| 17             | X₉OR           | .              | .              |
| 18             | X₉OR           | .              | .              |
| 19             | X₉OR           | .              | .              |
| 20             | X₉OR           | .              | .              |
| 21             | X₉OR           | .              | .              |
| 22             | X₉OR           | .              | .              |
| 23             | X₉OR           | .              | .              |
| 24             | X₉OR           | .              | .              |
| 25             | X₉OR           | .              | .              |
| 26             | X₉OR           | .              | .              |
| 27             | X₉OR           | .              | .              |
| 28             | X₉OR           | .              | .              |
| 29             | X₉OR           | .              | .              |
| 30             | X₉OR ⊕ X₉OR₀ / Register₌₂ | .         | .              |
| 31             | X₉OR ⊕ X₉OR₁ / Register₃₃ | .         | .              |
| 32             | X₉OR ⊕ X₉OR₂ / Register₃₄ | .         | .              |
| 33             | X₉OR ⊕ X₉OR₃ / Register₃₅ | .         | .              |

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| Columns | Rows | $C_0$ | ... | $C_7$ |
|---------|------|-------|-----|-------|
| R₀      |      | Register₀ ⊕ DataIn₀ | .   | .     |
| R₁      |      | Register₁ ⊕ DataIn₁ | .   | .     |
| R₂      |      | Register₂ ⊕ DataIn₂ | .   | .     |
| R₃      |      | Register₃ ⊕ DataIn₃ | .   | .     |
| R₄      |      | Register₄ ⊕ DataIn₄ | .   | .     |
| R₅      |      | Register₅ ⊕ DataIn₅ | .   | .     |
| R₆      |      | Register₆ ⊕ DataIn₆ | .   | .     |
| R₇      |      | Register₇ ⊕ DataIn₇ | .   | .     |

Figure 9. RC array contents after calculating for XORᵢ.
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| Rows | Columns | C₀ | C₁ | C₂ | C₃ | C₄ | C₅ | C₆ | C₇ |
|------|---------|----|----|----|----|----|----|----|----|
| R₀   | XOR₀    | XOR₀ ⊕ XOR₁| .  | .  | .  | .  | .  | XOR₀ ⊕ ... ⊕ XOR₇|
| .    | .       | .  | .  | .  | .  | .  | .  | .  | .  |
| R₇   | .       | .  | .  | .  | .  | .  | .  | .  | .  |

Figure 10. RC array contents for the second computation step for CRC-16.
Address In HEX | Frame Buffer A | Address In HEX | Frame Buffer A
--- | --- | --- | ---
0 | DataIn0 | . | .
1 | DataIn1 | 36 | Register8
2 | DataIn2 | 37 | Register9
3 | DataIn3 | 38 | Register10
4 | DataIn4 | 39 | Register11
5 | DataIn5 | 40 | Register12
6 | DataIn6 | 41 | Register13
7 | DataIn7 | . | .
. | . | 45 | Register14
10 | XOR3 | . | .
11 | XOR1 | 50 | Register15
12 | XOR2 | . | .
13 | XOR3 | 55 | Register16
14 | XOR4 | . | .
15 | XOR5 | . | .
16 | XOR6 | . | .
17 | XOR7 | . | .
. | . | . | .
30 | XOR0 ⊕ ... ⊕ XOR5/Register14 | . | .
31 | XOR0 ⊕ ... ⊕ XOR5/Register15 | . | .

Figure 11. Contents of Frame Buffer A after the algorithm terminates after one computation step the new registers values are shown at the specified locations.
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| Generator Name   | Polynomial                                  |
|------------------|---------------------------------------------|
| SDLC (CCITT)     | \(X^{16} + X^{12} + X^3 + X^0\)            |
| SDLC Reverse     | \(X^{16} + X^{11} + X^4 + X^0\)            |
| CRC-16           | \(X^{16} + X^{15} + X^2 + X^0\)            |
| CRC-16 Reverse   | \(X^{16} + X^{14} + X^1 + X^0\)            |
| CRC-12           | \(X^{12} + X^{11} + X^3 + X^2 + X^1 + X^0\) |
| Ethernet         | \(X^{32} + X^{26} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{9} + X^{7} + X^3 + X^2 + X^2 + X^1 + X^0\) |

Table 1. Common generator polynomials.
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| New Values After 8-shifts of the registers and the output of the XOR-gates |
|---------------------------------------------------------------|
| **XOR**<sub>i</sub> = | **Register**<sub>i</sub> ⊕ DataIn<sub>i</sub> | I = 0, 1, ..., 7 |
| **Register**<sub>0</sub> = | **Register**<sub>8</sub> ⊕ XOR<sub>4</sub> ⊕ XOR<sub>0</sub> |
| **Register**<sub>1</sub> = | **Register**<sub>9</sub> ⊕ XOR<sub>5</sub> ⊕ XOR<sub>1</sub> |
| **Register**<sub>2</sub> = | **Register**<sub>10</sub> ⊕ XOR<sub>6</sub> ⊕ XOR<sub>2</sub> |
| **Register**<sub>3</sub> = | **Register**<sub>11</sub> ⊕ XOR<sub>7</sub> ⊕ XOR<sub>3</sub> |
| **Register**<sub>4</sub> = | **Register**<sub>12</sub> ⊕ XOR<sub>4</sub> |
| **Register**<sub>5</sub> = | **Register**<sub>13</sub> ⊕ XOR<sub>5</sub> |
| **Register**<sub>6</sub> = | **Register**<sub>14</sub> ⊕ XOR<sub>6</sub> |
| **Register**<sub>7</sub> = | **Register**<sub>15</sub> ⊕ XOR<sub>7</sub> ⊕ XOR<sub>0</sub> |
| **Register**<sub>8</sub> = | XOR<sub>0</sub> ⊕ XOR<sub>5</sub> ⊕ XOR<sub>1</sub> |
| **Register**<sub>9</sub> = | XOR<sub>1</sub> ⊕ XOR<sub>6</sub> ⊕ XOR<sub>2</sub> |
| **Register**<sub>10</sub> = | XOR<sub>2</sub> ⊕ XOR<sub>7</sub> ⊕ XOR<sub>3</sub> |
| **Register**<sub>11</sub> = | XOR<sub>3</sub> |
| **Register**<sub>12</sub> = | XOR<sub>4</sub> ⊕ XOR<sub>0</sub> |
| **Register**<sub>13</sub> = | XOR<sub>5</sub> ⊕ XOR<sub>1</sub> |
| **Register**<sub>14</sub> = | XOR<sub>6</sub> ⊕ XOR<sub>2</sub> |
| **Register**<sub>15</sub> = | XOR<sub>7</sub> ⊕ XOR<sub>3</sub> |

Table 2. The states of the registers after 8-shifts for the CCITT CRC-16 Algorithm.
New Values After 8-shifts of the registers and the output of the XOR-gates

| XOR_i = | Register_i ⊕ DataIn_i  | i = 0, 1, ..., 7 |
|---------|------------------------|-----------------|
| X       | XOR_0 ⊕ XOR_1 ⊕ ... ⊕ XOR_7 |

| Register_0 = | Register_8 ⊕ X |
| Register_1 = | Register_9 |
| Register_2 = | Register_10 |
| Register_3 = | Register_11 |
| Register_4 = | Register_12 |
| Register_5 = | Register_13 |
| Register_6 = | Register_14 ⊕ XOR_0 |
| Register_7 = | Register_15 ⊕ XOR_1 ⊕ XOR_0 |
| Register_8 = | XOR_3 ⊕ XOR_2 |
| Register_9 = | XOR_4 ⊕ XOR_3 |
| Register_10 = | XOR_5 ⊕ XOR_4 |
| Register_11 = | XOR_6 ⊕ XOR_5 |
| Register_12 = | XOR_7 ⊕ XOR_6 |
| Register_13 = | XOR_8 ⊕ XOR_7 |
| Register_14 = | XOR_9 ⊕ X |
| Register_15 = | X |

Table 3. The states of the registers after 8-shifts for the CRC-16 Algorithm.
Table 4. The TinyRISC code for the CRC CCITT Algorithm.

| 0: | Ldri r1, 0x1; | R1 ← 1000\text{hex}. This is where DataIn Stored. |
| 1: | Ldfb r1, 0, 0, 2 ; | FB ← 2 x 32 bits at set 0, bank A, address 0. |
| 2: | Add r0, r0, r0; | No-operation. |
| 6: | Ldri r2, 0x1; | R2 ← 2000\text{hex}. This is where Circuit Registers Stored. |
| 7: | ldctxt r2, 0, 0, 0, 1; | Load 1 context word from main memory starting at the address stored in register 3 into plane 0, block 0 and starting at word 0. |
| 8: | add r0, r0, r0; | NOP. |
| 11: | ldri r4, 0x0; | R4 ← 0000\text{hex}. |
| 12: | dbcdc r4, 0, 0, 0, 0, 0; | Double bank column broadcast. It sends data from both banks address 0 in the FB and broadcasts the context words column-wise. It triggers the RC array to start execution of column 0 by the context word of address 0 in the column block of context memory operating on data in set 0. Bank A starting at 0. Bank B starting at (0 + 0). |
| 13: | wfbh 0, 0, 0, 0, 0\text{hex}; | Write data back to the FB A from the output registers of column 0 into set 0, address 0. Results for XOR. The value of Register 1. |
| 14: | wfbh 0, 0, 1, 0, 10\text{hex}; | Write data back to FB B from the output registers of column 0 into set 0, address 10\text{hex}. |
| 15: | dbcdc r4, 14\text{hex}, 0, 0, 0, 1, 0; | Double bank column broadcast. Bank A starting at 0x0. Bank B starting at (0x0 + 14), i.e. shifted 4 words from the starting point of XOR. The calculated items in this operation are the repeatedly used operations shaded in Table 1. |
| 16: | wfbh 0, 0, 0, 0, 30\text{hex}; | Write data back to FB from the output registers of column 0 into set 0, address 30\text{hex}. Values for Circuits Registers [12..15] are now available in FB A starting from address 30\text{hex}. |
| 17: | dbcdc r4, 8\text{hex}, 0, 0, 0, 0, 0\text{hex}; | Double bank column 0 broadcast. Bank A starting at 30\text{hex}. Bank B starting at (0x0 + 8\text{hex}). Thus, Registers [0..2] values are now available. |
| 18: | dbcdc r4, C\text{hex}, 0, 1, 0, 0, 0\text{hex}; | Double bank column 1 broadcast. Bank A starting at 1\text{hex}. Bank B starting at (0x0 + C\text{hex}). Thus, Registers [4..6] values are now available. |
| 19: | dbcdc r4, 10\text{hex}, 0, 2, 0, 0, 31\text{hex}; | Double bank column 2 broadcast Bank A starting at 30\text{hex}. Bank B starting at (0x0 + 10\text{hex}). Thus, Registers [8..10] values are now available. |
| 20: | wfbh 0, 0, 0, 0, 40\text{hex}; | Write data back to the frame buffer A from the output registers of column 1 into set 0, address 40\text{hex}. Values for Circuits Registers [0..2]. |
| 21: | wfbh 1, 0, 0, 0, 50\text{hex}; | Write data back to the FB A from the output registers of column 2 into set 0, address 50\text{hex}. Values for Circuits Registers [4..6]. |
| 22: | wfbh 2, 0, 0, 0, 55\text{hex}; | Write data back to the frame buffer A from the output registers of column 0 into set 0, address 55\text{hex}. Values for Circuits Registers [8..10]. |
| 23: | dbcdc r4, 10\text{hex}, 0, 0, 0, 0, 0\text{hex}; | Double bank column 0 broadcast. Bank A starting at 43\text{hex}. Bank B starting at (0x0 + 10\text{hex}). The output calculated here is the xor operation of XOR0, XOR1, & XOR3. The value is in cell 0 c 0. |
| 24: | wfbh 0, 0, 0, 0, 60\text{hex}; | Write data back to the FB A from the output registers of column 0 into set 0, address 60\text{hex}. |
| 25: | dbcdc r4, C\text{hex}, 0, 0, 0, 0, 0\text{hex}; | Double bank column 2 broadcast Bank A starting at 60\text{hex}. Bank B starting at (0x0 + C\text{hex}). Thus, Register 7 value is now calculated. |
| 26: | wfbh 0, 0, 0, 0, 65\text{hex}; | Write data back to the FB A from the output registers of column 0 into set 0, address 65\text{hex}. |

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Table 5. The TinyRISC code for the CRC-16 Algorithm.

| Label | Description | Clocks |
|-------|-------------|--------|
| MOV   | SP, D_Loc   | 80486  |
|       |             | Pentium|
|       |             | 1T     |
|       |             | 1T     |
The link to the formal publication is via https://doi.org/10.1016/S0965-9978(02)00101-1

| MOV | Description                  | Pentium | 80486 |
|-----|------------------------------|---------|-------|
| MOV | BP, IR_Loc                   | IT      | IT    |
| MOV | DI, XORs_Loc                 | IT      | IT    |
| MOV | BX, C_Value                  | BX      | Counter Value. IT IT |
| MOV | AL, [SP]                     | IT      | IT    |
| MOV | BX, [BP]                     | IT      | IT    |
| MOV | BL, AL                       | BL      | IT    |
| MOV | [DI], BL                     | IT      | IT    |
| INC | SP                           | IT      | IT    |
| INC | BP                           | IT      | IT    |
| INC | DI                           | IT      | IT    |
| DEC | BX                           | IT      | IT    |
| JNZ | ZIP                          | IT      | IT    |

Findings

| Label | Description                  | 80486 | Pentium |
|-------|------------------------------|-------|---------|
| MOV   | SP, D_Loc                    | IT    | IT     |

Table 6. The Intel code for the CRC-CCITT-16 Algorithm.

| Total Clocks | 142T | 128T |
|--------------|------|------|
| Frequency    | 100MHz | 133MHz |
| Total Time   | 1.42μsec | 0.96μsec |
| Number of Bits | 8     | 8     |
| Bits per Cycles | 0.056 | 0.0625 |
| Mega Bits per Second (Mbps) | 5.6 | 8.3 |
| Cycles per Bits | 17.86 | 16 |
The link to the formal publication is via
https://doi.org/10.1016/S0965-9978(02)00101-1

| MOV | Description | Instruction | | |
|-----|-------------|-------------|---|---|
| MOV | BP, IR_Loc | BP ← Location of Registers initial values in memory. | 1T | 1T |
| MOV | DI, XORs_Loc | SP ← Loc of the resultant XORs in memory. | 1T | 1T |
| MOV | BX, C_Value | BX ← Counter value. | 1T | 1T |
| ZIP: MOV | AL, [SP] | Get the vector element addressed by the SP register. | 1T | 1T |
| MOV | BL, [BP] | Get the vector element addressed by the BP register. | 1T | 1T |
| XOR | BL, AL | BL ← AL XOR BL. | 1T | 1T |
| MOV | [DI], BL | | 1T | 1T |
| INC | SP | Get next element. | 1T | 1T |
| INC | BP | Get next element. | 1T | 1T |
| INC | DI | Increment the destination. | 1T | 1T |
| DEC | BX | Decrement the counter. | 1T | 1T |
| JNZ ZIP | Jump of not finished to label AA. | 3/1T | 1T |
| MOV | BX, C_Value | BX ← Counter value: | 1T | 1T |
| MOV | AL, $30000 | Assign zero to AL. | 1T | 1T |
| MOV | BL, [DI] | Get the vector element addressed by the BP register. | 1T | 1T |
| XOR | AL, BL | AL ← AL XOR BL. | 1T | 1T |
| INC | DI | Increment the destination. | 1T | 1T |
| DEC | BX | Decrement the counter. | 1T | 1T |
| JNZ FUNNEL | Jump of not finished to label AA. | 3/1T | 1T |
| MOV | $20000, BL | Store the result of funneling in memory location 20000h. | 1T | 1T |
| MOV | AL, [BP + 8] | Store the value of Registers in AL. | 1T | 1T |
| XOR | AL, $20000 | XOR the contents of Register8, and the result of Funneling. | 1T | 1T |
| MOV | $30000, AL | Store the new value in Register8. | 1T | 1T |
| MOV | $30001, [BP + 9] | Store the value found in Registers in the new location of Register8. | 1T | 1T |
| MOV | $30002, [BP + 10] | Register8 ← Register11. | 1T | 1T |
| MOV | $30003, [BP + 11] | Register9 ← Register11. | 1T | 1T |
| MOV | $30004, [BP + 12] | Register10 ← Register11. | 1T | 1T |
| MOV | $30005, [BP + 13] | Register11 ← Register11. | 1T | 1T |
| MOV | AL, [BP + 14] | Store the value of Register14 in AL. | 1T | 1T |
| XOR | AL, [DI] | XOR the contents of Register14 with XORs. | 1T | 1T |
| MOV | $30006, AL | Store the new value in Register14. | 1T | 1T |
| MOV | AL, [BP + 15] | Store the value of Register15 in AL. | 1T | 1T |
| XOR | AL, [DI] | XOR the contents of Register15 with XORs. | 1T | 1T |
| MOV | $30007, AL | Store the new value in Register15. | 1T | 1T |
| MOV | AL, [DI + 2] | Store the value of XOR8 in AL. | 1T | 1T |
| XOR | AL, [DI + 3] | XOR with XOR8. | 1T | 1T |
| MOV | $30008, AL | Store the new value in Register8. | 1T | 1T |
| MOV | AL, [DI + 3] | Store the value of XOR8 in AL. | 1T | 1T |
| XOR | AL, [DI + 4] | XOR with XOR8. | 1T | 1T |
| MOV | $30009, AL | Store the new value in Register8. | 1T | 1T |
| MOV | AL, [DI + 4] | Store the value of XOR8 in AL. | 1T | 1T |
| XOR | AL, [DI + 5] | XOR with XOR8. | 1T | 1T |
| MOV | $3000A, AL | Store the new value in Register8. | 1T | 1T |
| MOV | AL, [DI + 5] | Store the value of XOR8 in AL. | 1T | 1T |
| XOR | AL, [DI + 6] | XOR with XOR8. | 1T | 1T |
| MOV | $3000B, AL | Store the new value in Register8. | 1T | 1T |
| MOV | AL, [DI + 6] | Store the value of XOR8 in AL. | 1T | 1T |
| XOR | AL, [DI + 7] | XOR with XOR8. | 1T | 1T |
| MOV | $3000C, AL | Store the new value in Register8. | 1T | 1T |
| MOV | AL, [DI + 7] | Store the value of XOR8 in AL. | 1T | 1T |
| XOR | AL, [DI + 8] | XOR with XOR8. | 1T | 1T |
| MOV | $3000D, AL | Store the new value in Register8. | 1T | 1T |
| MOV | AL, [DI + 8] | Store the value of XOR8 in AL. | 1T | 1T |
| XOR | AL, $20000 | XOR the contents with the result of Funneling. | 1T | 1T |
| MOV | $3000E, AL | Store the new value in Register8. | 1T | 1T |
| MOV | $3000F, $20000 | Store the new value in Register8. | 1T | 1T |

| Findings | Total Clocks | 190T | 162T |
|---------|-------------|------|------|
| Frequency | 100MHz | 133MHz |
| Total Time | | 1.9μsec | 1.22μsec |
| Number of Bits | 8 | 8 |
| Bits per Cycles | 0.042 | 0.049 |
| Mega Bits per Second (Mbps) | 4.2 | 6.56 |
| Cycles per Bits | 23.75 | 20.25 |

Table 7. The Intel code for the CRC-16 Algorithm.
| Algorithm                        | M1   | Pentium | Intel | 80486 | 80486  |
|---------------------------------|------|---------|-------|-------|--------|
| CRC-CCTT-16 parallel algorithm  | 30   | 128     | 4.26  | 0.96  | 0.0625 |
| for one channel                 |      | 142     | 4.73  | 1.42  | 0.056  |
| CRC-16 parallel algorithm       | 26   | 162     | 6.23  | 1.22  | 0.049  |
| for one channel                 |      | 190     | 7.3   | 1.9   | 0.042  |
| CRC-CCTT-16 parallel algorithm  | 30   | 1024    | 34.13 | 7.69  | 0.0625 |
| for 8-channel                   |      | 1136    | 37.86 | 11.36 | 0.056  |
| CRC-16 parallel algorithms      | 26   | 1296    | 49.84 | 9.74  | 0.05   |
| for 8-channels                  |      | 1520    | 58.46 | 15.2  | 0.042  |

Table 8. Comparison with the Intel systems.
Table 9. Comparisons with RC-1000 FPGA.

| Algorithm                        | System  | # of Cycles | Speedup of the RC-1000 over the M1 |
|----------------------------------|---------|-------------|-----------------------------------|
| CRC-CCITT-16 parallel algorithm  | M1      | 30          |                                   |
|                                  | RC-1000 | 8           | 3.75                              |
| CRC-16 parallel algorithm        | M1      | 26          |                                   |
|                                  | RC-1000 | 17          | 1.53                              |

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