All-digital half-rate referenceless CDR with single direction frequency sweep scheme using asymmetric binary phase detector

Changzhi Yu¹, Himchan Park¹, Qiwei Huang¹, Daewung Lee¹, Hyunmook Kim¹, Hyunbae Lee¹, and Jinwook Burm¹a)

Abstract This paper presents an all-digital half-rate referenceless CDR with a single direction frequency acquisition achieved. Thanks to asymmetric binary phase detector (ABPD), compared with existed inverse alexander phase detector (IAPD), we changed the input-output characteristic to enable accumulated phase error point in the same direction when frequency error happens while the output of IAPD has no directivity. Once the frequency of the digital controlled oscillator (DCO) enters the pull-in range of the CDR loop, the phase is automatically locked. To improve jitter tolerance (JTOL) performance further, IAPD logic is enabled, and ABPD is disabled after locking. The prototype was implemented in a 28 nm low power CMOS process with a data rate tracking range of 9–11 Gb/s. The measured JTOL is 0.35 UI at high frequency with PRBS31 input data pattern. 

Keywords: clock and data recovery (CDR), frequency acquisition, referenceless, jitter tolerance (JTOL), referenceless CDR, digitally controlled oscillator (DCO)

Classification: Integrated circuits

1. Introduction

With the continuous expansions of the applications of wired serial communication, the performance, cost, and scalability of clock and data recoveries (CDRs) as the core component of wireline receivers are getting more attention. Referenceless CDRs have the following advantages over existing CDRs that requires a reference clock: First, the operational data rate being neither fixed nor of a few predefined values, a referenceless CDR can adaptively operates at any data rate within the tuning range of DCO [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19]. Therefore, it has a wider range of applications and improves the reusability of IPs. Second, since any forms of reference such as crystal oscillators are not required, the number of pins can be further minimized, making a referenceless CDR cost-effective [3, 5].

To date, research on referenceless CDRs has focused on the following aspects: reduce the frequency acquisition time and increase the frequency acquisition range while maintaining small area and high performance [2]. The trade-off on these requirements makes it difficult to reduce the locking time without introducing area overhead while keeping low complexity of the loop.

In this paper, a new phase-detection logic based on an Inverse Alexander phase detector (IAPD) [23] named asymmetric binary phase detector (ABPD) for referenceless CDRs will be proposed to be used for frequency acquisition. On the basis of the existing digital CDR [8, 20, 21], the function of single direction frequency acquisition and phase tracking is realized by modifying the input-output characteristic of IAPD without a frequency locked loop. Since a single direction frequency acquisition is achieved based on the ABPD, in the worst case, its lock time is 17 µs to tracking the difference of 1 Gb/s when target frequency is higher than the initial frequency of DCO. Furthermore, since there is no frequency detection logic or frequency locked loop exists, its frequency detection range is no longer limited. The only limit is the tuning range of DCO.

2. Proposed frequency acquisition algorithm

The proposed all-digital referenceless CDR, is implemented as a single loop half-rate structure capable of single direction frequency acquisition and phase tracking. This achievement is possible thanks to the ABPD and digital loop filter, which the former makes the output signal directs to the same direction of the frequency error, and the later makes frequency sweep restart from the highest frequency when DCO frequency reaches its lower limit.
The input-output characteristic of conventional IAPD is shown in Fig. 1(a), assume input data signal has no jitter and there is a large frequency error, early ($E_{IAPD}$) and late ($L_{IAPD}$) signal appears alternatively at the output of IAPD. In the real case of input signal containing jitter, the input-output characteristic of IAPD is changed and there is no action in the jittered region, its output is zero. Therefore, jitter generation can be minimized. As a large frequency error exists in the CDR loop, $E_{IAPD}$ and $L_{IAPD}$ appear alternatively because the frequency error exceeds the pull-in range of the CDR loop. This pull-in range is very small, usually several hundreds of ppm [18].

In order to achieve a single direction frequency acquisition function, a new phase-detection logic ABPD is proposed. Our target is to perturb the output of IAPD logic to prefer the occurrence of early signal slightly more than late signal when large frequency error happens.

The improvement is made to set the output of the ABPD input-output characteristic to produce early signal where the output of IAPD is ambiguous between early and late states. The ambiguous conditions of IAPD normally happen at the edges of jittered input data (called jittered region) as shown in Fig. 1(a). The impact of this change is when frequency error exceeds CDR’s pull-in range, the accumulated early and late signals ACC [(No. of $L_{ABPD}$) – (No. of $E_{ABPD}$)], keeps reducing since ABPD preferentially produces early signals.

In the case of DCO initial frequency is higher than target frequency, the jitter of the input signal will cause the occurrence of $E_{ABPD}$ to be larger than the number of $L_{ABPD}$, the frequency of the DCO continues to decrease, and finally enters the pull-in range of CDR loop. Contrastively, in the case of DCO’s initial frequency is lower than target frequency outside of the pull-in range, DCO frequency will keep decreasing from the preferential early signal and reaches the lower limit of DCO tuning range. Then overflow of DCO frequency control word will happen so that the frequency sweep restarts from the highest frequency again.

In both cases, phase lock can be automatically completed as long as the target frequency is within the DCO tuning range, without any additional control. When frequency locking achieved, the locking point is slightly to the right rather than the center of the eye diagram, since the number of $E_{ABPD}$ is slightly larger than $L_{ABPD}$, as shown in Fig. 2(b).

3. Architecture of referenceless CDR

According to the illustrations of the input-output characteristic in Fig. 1(a), the block diagram of the dual-mode phase detector is shown in Fig. 1(b). The timing diagram of logic implementation on early and late signal generation of ABPD and IAPD is shown in Fig. 2: (a) shows that in jittered region, the output of both $E_{IAPD}$ and $L_{IAPD}$ are low to keep not to introduce jitter generation, the illustration of lock region is shown as green shaded region, and (b) shows that in jittered region, the output of $E_{ABPD}$ is high which makes that single direction frequency sweep is possible. The logic table of the proposed dual-mode phase detector is shown in Table I.

The overall structure of the referenceless CDR is shown in Fig. 3. Input signal is sampled by sampler [22], the sampled signals ($D_n$, $E_n$) are input to the dual-mode phase detection logic circuits to generate early and late signal (Fig. 1(a)) [23, 24, 25]. The phase-detection logic circuits generate two sets of phase error signals $E_{IAPD}/L_{IAPD}$ and $E_{ABPD}/L_{ABPD}$ according to its input-output characteristic respectively. The multiplexer control signal LOCK selects whether to operate in the frequency acquisition mode (LOCK = 0) or high jitter tolerance mode (LOCK = 1) depending on the state of lock detector. The deserializer further deserializes the high-speed serial phase error signal into an eight-bit low-speed parallel signal with a speed of 1/8 [1]. The deserialized parallel signals are summed by the adder array and a 5-bit correction signal in 2’s complement form is generated to facilitate digital processing of the digital loop filter. Finally, a 10-bit frequency control word is generated by DLF to control the frequency of the DCO. In addition, the lock detector output is low (LOCK = 0) when referenceless CDR is powered-on, during the meantime, the downward frequency sweep was performed with ABPD. As soon as the lock detector detects a frequency lock, the LOCK changes from low to high, further increasing the jitter tolerance.
4. Synthesized digital logic

The structure of the synthesis logic circuit is shown in Fig. 4 [21, 26, 27, 28, 29, 30]. Since deserialized 8-bit L.ls[7:0] and E.ls[7:0] are not binary but thermometer codes, an adder array is needed to summing every bit to generate 5-bit 2’s complement binary correction signal bin[4:0]. The correction signal passes through the proportional (controlled by p[3:0]) and integral (controlled by i[3:0]) gain controllers to generate prop1[20:0] and intg1[20:0] in Fig. 4. Among them, intg[20:0] is generated by accumulate intg1[20:0]. The output signal out[20:0] is the sum of prop1[20:0] and intg[20:0]. Among these 21-bit output signal, the MSB (sign bit) and 10-bit LSBs are discarded (in order to get 2–10 gain), the middle 10 bits are taken as the control signal of the DCO frequency (FCW[9:0]).

The implementation of the lock detector is by periodically detecting the change in the output value of the integration path within a certain period of time. That is, in the unlocked state, because EABPD is greater than LABPD, the value of the integration path is continuously decreasing, once the loop enters the locked state, the value of the intercepted integration path will remain the same or fluctuate slowly within the range of ±1. Therefore, the lock criterion is that when the value of the intercepted integration path fluctuates within a range of ±1, it can be determined as a lock. In the design, a proper margin is left, and its adjustable range is ±32.

5. Measurement results

The photomicrograph of the prototype chip is shown in Fig. 5(a), with an area of 0.099 mm². The recovered clock jitter with 11 Gb/s PRBS31 pattern is shown in Fig. 5(b), measured RMS jitter is 1.35 ps, peak-to-peak jitter is 12.2 ps, and BER obtained by the measurement is <10⁻¹².

The lock time is measured by signal source analyzer (Agilent E5052A) with setting the initial frequency to 5 GHz, corresponding to the input data of 10 Gb/s, and changing the input data to 9 Gb/s and 11 Gb/s, respectively, as shown in Fig. 6(a). When the initial frequency is higher than the target frequency (4.5 GHz for 9 Gb/s data), the frequency is scanned downward, and the phase is directly locked after reaching the target frequency, so the lock time is short, as indicated by the solid gray line. When the target frequency (5.5 GHz for 11 Gb/s data) is higher than the initial frequency (5 GHz), the downward frequency scanning is initially performed. Then with the overflow of DLF output out[20:0], the DCO frequency jumps from the lowest to the highest, and continues downward scanning down until the frequency lock, as indicated by the solid black line. Since the referenceless CDR proposed in this paper has the characteristics of single direction frequency sweep, the frequency locking time is long when the target frequency is slightly larger than the initial frequency of the DCO and outside the pull-in range of the CDR loop. Even for the worst case, the lock time is less than about 17 µs. The lock time is 1.2 µs and 17 µs when the final fDCO’s is 4.5 GHz and 5.5 GHz, respectively.

The measurement results of the jitter tolerance (JTOL) are shown in Fig. 6(b). As frequency and phase locking is achieved by ABPD, then IAPD is used to further increase the jitter tolerance at the high frequency to 0.35 UI. When the jitter of the input signal increases, the lock time decreases accordingly. However, continuing to increase the jitter of the input signal will cause the lock frequency to fail to lock, and then oscillate. The results of the designed prototype’s locking behavior under different channel losses are shown in Fig. 7.

6. Conclusion

This paper presents a single slope frequency sweep and phase locking method of single-loop referenceless CDR. With only 2X oversampling method, the phase detection
logic circuit designed according to the output phase error signal cooperates with the DLF to realize single direction frequency sweep and phase-locking within the DCO tuning range, which further simplifies the structure of the loop and further reduces the chip area. The prototype is fabricated in a 28 nm low-power CMOS process, powered by a 1 V supply voltage, and has an energy efficiency of 2.6 pJ/bit (26 mW for 10 Gb/s).

Acknowledgments

This research is supported by MOTIE (10080622), NRF-2018R1D1A1B07049663 and IITP-2018-0-01421. The authors would like to thank IDEC and Samsung Foundry to provide EDA tools and chip verification, respectively.

References

[1] D. Kim, et al.: “A 15-gb/s sub-baud-rate digital cdr,” IEEE J. Solid-State Circuits 54 (2019) 685 (DOI: 10.1109/JSSC.2018.2885540).
[2] Y. Kim, et al.: “A 10-gb/s reference-less baud-rate cdr for low power consumption with the direct feedback method,” IEEE Trans. Circuits Syst., II, Exp. Briefs 65 (2018) 1539 (DOI: 10.1109/TCSII.2017.2758923).
[3] K. Park, et al.: “A 6.7–11.2-gb/s, 2.25-pj/b, single-loop referenceless cdr with multi-phase, oversampling pdf in 65-nm cmos,” IEEE J. Solid-State Circuits 53 (2018) 2982 (DOI: 10.1109/JSSC.2018.2859947).
[4] J. Jin, et al.: “A 0.75–3.0-gb/s dual-mode temperature-tolerant referenceless cdr with a deadzone-compensated frequency detector,” IEEE J. Solid-State Circuits 53 (2018) 2944 (DOI: 10.1109/JSSC.2018.2856243).
[5] W. Rahman, et al.: “A 22.5-to-32-gb/s 3.2-pj/b referenceless baud-rate digital cdr with dfe and ecle in 28-nm cmos,” IEEE J. Solid-State Circuits 52 (2017) 3517 (DOI: 10.1109/JSSC.2017.2744661).
[6] J. H. Yoon, et al.: “A dc-to-12.5-gb/s 9.76 mw/gb/s all-rate cdr with a single lc vco in 90 nm cmos,” IEEE J. Solid-State Circuits 52 (2017) 856 (DOI: 10.1109/JSSC.2016.2646803).
[7] K. Lee and J. Y. Sim: “A 0.8-to-6.5-gb/s continuous-rate referenceless digital cdr with half-rate common-mode clock-embedded signaling,” IEEE Trans. Circuits Syst. I, Reg. Papers 63 (2016) 482 (DOI: 10.1109/TCSI.2016.2528480).
[8] G. Shu, et al.: “A 4-to-10.5-gb/s continuous-rate digital clock and data recovery with automatic frequency acquisition,” IEEE J. Solid-State Circuits 51 (2016) 428 (DOI: 10.1109/JSSC.2015.2497963).
[9] S. Choi, et al.: “A 0.65-to-10.5-gb/s reference-less cdr with asynchronous baud-rate sampling for frequency acquisition and adaptive equalization,” IEEE Trans. Circuits Syst. I, Reg. Papers 63 (2016) 276 (DOI: 10.1109/TCSI.2015.2512713).
[10] S. H. Chu, et al.: “A 22 to 26.5 gbps optical receiver with all-digital clock and data recovery in a 65 nm cmos process,” IEEE J. Solid-State Circuits 50 (2015) 2603 (DOI: 10.1109/JSSC.2015.2465843).
[11] M. S. Jalali, et al.: “A reference-less single-loop half-rate binary cdc,” IEEE J. Solid-State Circuits 50 (2015) 2037 (DOI: 10.1109/JSSC.2015.2429714).
[12] S. Huang, et al.: “An 8.2-gb/s/4-to-10.3-gb/s full-rate linear referenceless cdc without frequency detector in 0.18 um cmos,” IEEE J. Solid-State Circuits 50 (2015) 2048 (DOI: 10.1109/JSSC.2015.2427332).
[13] J. Han, et al.: “0.6–2.7-gb/s referenceless parallel cdc with a stochastic dispersion-tolerant frequency acquisition technique,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 22 (2014) 1219 (DOI: 10.1109/TVLSI.2013.2288682).
[14] G. Shu, et al.: “A reference-less clock and data recovery circuit using phase-rotating phase-locked loop,” IEEE J. Solid-State Circuits 49 (2014) 1036 (DOI: 10.1109/JSSC.2013.2296152).
[15] N. Kocaman, et al.: “An 8.5–11.5-gbps sonet transceiver with referenceless frequency acquisition,” IEEE J. Solid-State Circuits 48 (2013) 1875 (DOI: 10.1109/JSSC.2013.2259033).
[16] W. S. Titus and J. G. Kenney: “A 5.6 ghto 11.5 ghto dco for digital dual loop cdc,” IEEE J. Solid-State Circuits 47 (2012) 1123 (DOI: 10.1109/JSSC.2012.2185572).
[17] S. K. Lee, et al.: “A 650 mb/s-to-8-gb/s referenceless cdc with automatic acquisition of data rate,” 2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers (2009) 184 (DOI: 10.1109/ISSCC.2009.4977369).
[18] K. Hanamula, et al.: “A wide-ranging track and clock and data recovery circuit,” IEEE J. Solid-State Circuits 43 (2008) 425 (DOI: 10.1109/JSSC.2007.914290).
[19] D. Dalton, et al.: “A 12.5-mb/s to 2.7-gb/s continuous-rate cdc with automatic frequency acquisition and data-rate readback,” IEEE J. Solid-State Circuits 40 (2005) 2713 (DOI: 10.1109/JSSC.2005.856577).
[20] C. Yu, et al.: “8–10 gbit/s full synthesised continuous-half-rate reference-less all-digital cdc with sub-harmonic frequency extraction,” Electron. Lett. 54 (2018) 1156 (DOI: 10.1049/el.2018.6145).
[21] J. L. Sonntag and J. Stonick: “A digital clock and data recovery architecture for multi-gigabit/s binary links,” IEEE J. Solid-State Circuits 41 (2006) 1867 (DOI: 10.1109/JSSC.2006.875292).
[22] B. Nikolic, et al.: “Improved sense-amplifier-based flip-flop: Design and measurements,” IEEE J. Solid-State Circuits 35 (2000) 876 (DOI: 10.1109/4.845191).
[23] W. Verbeke, et al.: “A 1.8-gb/s, 12.5–25-gb/s wide range all-digital clock and data recovery circuit,” IEEE J. Solid-State Circuits 45 (2013) 470 (DOI: 10.1109/JSSC.2013.2755690).
[24] M. Rau, et al.: “Clock/data recovery pll using half-frequency clock,” IEEE J. Solid-State Circuits 32 (1997) 1156 (DOI: 10.1109/4.697310).
[25] C.-K. K. Yang, et al.: “A 0.5–sps pll mdmp CMOS 4.0-Gbit/s serial link transceiver with data recovery using oversampling,” IEEE J. Solid-State Circuits 33 (1998) 713 (DOI: 10.1109/4.668986).
[26] R. Itti, et al.: “A 0.5-to-2.5-gb/s reference-less half-rate digital cdc with unlimited frequency acquisition range and improved input duty-cycle error tolerance,” IEEE J. Solid-State Circuits 46 (2011) 3150 (DOI: 10.1109/JSSC.2011.2168872).
[27] D. S. Kim, et al.: “A 0.3–1.4 ghto all-digital fractional-n pll with adaptive loop gain controller,” IEEE J. Solid-State Circuits 45 (2010) 2305 (DOI: 10.1109/JSSC.2010.2064050).
[28] V. Kratyuk, et al.: “A design procedure for all-digital phase-locked loops based on a charge-pump phase-locked-loop analogty,” IEEE Trans. Circuits Syst., II, Exp. Briefs 54 (2007) 247 (DOI: 10.1109/TCSII.2006.889443).
[29] S. Tertinek, et al.: “Binary phase detector gain in bang-bang phase-locked loops with dco jitter,” IEEE Trans. Circuits Syst., II, Exp. Briefs 57 (2010) 941 (DOI: 10.1109/TCSI.2010.2083110).
[30] W. Yin, et al.: “A tdcss-less 7 mw 2.5-gb/s digital cdc with linear loop dynamics and offset-free data recovery,” IEEE J. Solid-State Circuits 46 (2011) 3163 (DOI: 10.1109/JSSC.2011.2168873).