Evolutionary Cell Aided Design for Neural Network Architectures

Philip Colangelo∗1,3, Oren Segal†2, Alexander Speicher‡2, and Martin Margala§1

1Department of Computer Engineering, University of Massachusetts Lowell
2Department of Computer Science, Hofstra University
3Intel PSG

Abstract

Mathematical theory shows us that multilayer feedforward Artificial Neural Networks(ANNs) are universal function approximators, capable of approximating any measurable function to any desired degree of accuracy. In practice designing practical and efficient neural network architectures require significant effort and expertise. We present a new software framework called Evolutionary Cell Aided Design(ECAD) meant to aid in the exploration and design of Neural Network Architectures(NNAs) for reconfigurable hardware. The framework uses evolutionary algorithms to search for efficient hardware architectures. Given a general structure, a set of constraints and fitness functions, the framework will explore the space of hardware solutions and attempt to find the fittest solutions.

1 Introduction

The difficulty in designing performant NNAs has brought a recent surge in interest in auto design of NNAs. The focus of the existing body of research has been on optimizing NNA design for accuracy [1]. Optimizing NNAs is typically a difficult process in part because of the vast number of hyperparameter combinations that exist, and in cases where a combination is not optimal, performance will suffer. In fact, many deep learning frameworks such as TensorFlow [2] and Keras [3] offer support for hyperparameter tuning, but these are typically Bayesian optimizations that treat the ANN as a black-box and are used for the neural network training process. Research shows that the parameters of a network can directly influence the accuracy, throughput, and energy consumption of that model in deployment [4].

Once an accurate NNA has been found, the next step is to try to fit it into existing hardware i.e. a CPU, GPU, or a custom built but general purpose neural network hardware device such as a TPU [5]. None of these hardware solutions offer network specific specialization. The gap between the two optimizations is where ECAD comes in, it allows to search for an optimal hardware/software co-design by exploring the design space on the software and the hardware side and allows to implement a custom hardware solution for a specific model using reconfigurable hardware.

2 ECAD Software

ECAD is intended to create a NNA that is optimized towards specific design goals. At the heart of the software side, lies an evolutionary algorithm and a vector of fitness functions. Fitness functions currently

∗philip.colangelo@intel.com
†oren.segal@hofstra.edu
‡aspeicher1@pride.hofstra.edu
§Martin_Margala@uml.edu
include measurements of accuracy, speed, energy efficiency, and throughput. ECAD allows to select the importance(weight) given to each of the fitness functions and by doing so guide an evolutionary process towards the required fitness goals. The result is a neural network design optimized towards the goals specified in the fitness functions.

2.1 ECAD Software Flow

Figure[1] shows an overview of the ECAD flow. The next sections provide detail for each of the stages in the flow.

2.1.1 The ECAD Configuration File

The process starts with a user generated description of the desired neural network. It includes a description of the structure, constraints, fitness goals and weight of each goal. Those values are stored in the ECAD configuration file in a textual JavaScript Object Notation (JSON) format. An example of the configuration file can be seen in Figure[2]. Lines 11 to 16 define population values such as initial and maximum population size, mutation rate etc. Lines 17 to 22 specify the worker types that will be used to evaluate our goals and their parameters. Lines 34 to 92 declare cell types and their parameters such as range of legal values, mutation rate and user defined functions to be called upon a change event such as a mutation. Lines 101 to 111 define the hardware we wish to target. Lines 113 to 119 declare a cell array that will hold the general structure of the network we would like to explore through the evolutionary process.

2.1.2 Population Generation

Initially the system will create a population of neural networks using the base design specified in the configuration file. The population initial size, maximum size and change rate are all controlled using the configuration parameters. Each auto generated network instance will be mutated and different from the original base design.

As the evolutionary process progresses and once a sufficient number of networks are evaluated according to all fitness parameters, the process of population generation will repeat itself continuously except that the mutations will be based on the most fit individuals in the population, selected according to their fitness scores (see steady-state model in [6]).

2.1.3 Testing Population Fitness

In the next stage each NN instance will be sent to one or more fitness evaluators or workers in ECAD terminology. The workers are designed as independent processes and can be distributed across a cluster of computers. They are orchestrated using a Master/Worker parallel computation model [7] running on top of MPI [8].

Each Worker sits in a separate process, inherits from a common C++ Worker class, and implements a common software interface. The system is built to be flexible and allow adding different types of workers easily. The implementation details for each worker can be completely different.

We currently have three types of workers implemented:

1. *Simulation Worker* capable of simulating a NN design and return accuracy and timing results

2. *Physical Worker* capable of synthesizing a NN design and return hardware synthesis results

3. *HWDB Worker* capable of accurately estimating NN synthesis results and return estimated hardware synthesis results

Once a worker’s fitness evaluation is complete it will return the results to the master/server process. The master process will collect the results from all the workers that evaluated each NN and apply a combined score to each NN. Scores are combined using a unique Id that is assigned to each generated NN instance when it is initially created.
2.1.4 Sorting Population by Fitness

In the next stage the ECAD system will sort the NN population according to the score each NN received. The top NN instances will be selected for mutation.

The mutation process will take the top NN performers and mutate the cell/layer fields randomly according to constraints specified in the configuration file. For example, the dense layer could specify a range of allowed number of neurons etc.

The mutated NN will be introduced to the population as new instances (2.1.2). Note that if we limit the population size in the configuration file and the addition of the new instances will cause an overflow, the worst performers will be removed from the population in this step as well.

We now have a new population containing a mix of old and new instances. New instances will be sent to evaluation and the evaluation process will repeat until the end condition is met.

The end condition could be the number of generations the simulation flow is requested to run or a desired accuracy.

During the evaluation process, ECAD outputs the top networks and their scores to a custom database (EcadDB). At the end of the simulation this database is examined, and the top networks can be extracted for further investigation and full hardware synthesis. Note that even though it is possible to run full synthesis during the ECAD flow we use the HW resource estimator option because of resource and time constraints. A full hardware compile can take several hours per network instance and so it is reserved for top network candidates that deserve further investigation.

2.2 From Abstract Network Description to Concrete Design

The process by which an abstract network description is transformed to a hardware or simulation design is depicted in Fig 3. The software layer is built to allow the transformation to be general. For each type of transformation we wish to make, we design a C++ object of type Actualizer (or a writer) which takes the abstract design and produces a model that we can test in software or hardware.

For hardware design generation we opted to use high-level OpenCL over low-level Hardware Description Language (HDL) since it allows auto generated designs to be more easily examined and maintained by human engineers. But since the system is flexible we can always move away from high-level to the HDL level if the need arises. Software level simulation of NN designs is used for testing accuracy, verifying results and estimating hardware resource usage without going through the costly hardware compilation process. For software level accuracy and validation we use a neural network simulator.

2.3 Neural Network Simulator

The Neural Network Simulator (NeuralNetSim) is responsible for testing and verifying the ECAD neural network architectures. We chose TensorFlow as the machine learning simulation framework as it supports both CPU and GPU training for deep neural networks, it enjoys continuous support and updates in addition to a high-level python API. This allows for quick trouble shooting as well as easily adding new features, such as different types of layers or activation functions to the simulator. The NeuralNetSim consists of three classes:

1. **ECAD Reader** servers as an interface to the evolutionary framework. It’s main responsibility is accepting inputs such as files and training arguments as well as returning data and reports after training has been completed. It extracts the network info from the ECAD file and passes it to the TF Model Builder.

2. **TF Model Builder** holds the actual TensorFlow graph and all other TensorFlow variables. It is responsible for dynamically creating the graph based on the info passed by the reader. It loads and handles the training and testing data. Finally it also holds the training functions which are called from the ECAD reader.
3. **TF Functions** is a collection of TensorFlow API functions that are called by the TF Model Builder when building the graph. New TensorFlow functions can be added here to expand support for other types of networks, optimizers, activation functions, etc.

### 2.3.1 Neural Network Simulation Flow

The ECAD reader is a flexible script responsible for accepting an ECAD file as well as several other arguments that affect the training of the neural network:

1. **ECAD file** containing the networks architecture.
2. **Destination Directory** used to return the report file, weights and biases.
3. **Epochs** dictates how many times the training set is used for training.
4. **Batch size** sets the amount of samples that are passed into the network at a time during training.
5. **SaveWB** is an optimal argument that tells the simulator to export the weights and biases after training.
6. **verboseTF** displays potential warning or deprecation messages when the graph is created.

In the first stage, the ECAD neural network architecture is converted into a TensorFlow graph to be trained. The ECAD network consists of cells which either represent the input, hidden layers, activation functions, or output which are encapsulated in a cell array. This cell array is sequentially traversed and the graph is dynamically generated. Whenever a new hidden layer is created a reference to the layers weights and biases is kept, which can later be used for retrieval of the values after training. The data type for the neural network is currently float32 which is used for both the input data, the weights and the biases as well.

After the full network graph is created the cost and optimizer are instantiated. Currently the softmax with cross entropy function is used for the MNIST classification problem and the utilized optimizer is the AdamOptimizer which is set to a learning rate of 0.001. None of these functions are final and as the project expands more cost functions and optimizers can be added.

The final step, before training can begin, is getting the training and testing data. In this case the MNIST data is imported using tf.keras.datasets and the input data is converted to float32 numpy arrays. All elements in the inputs are divided by 255 to normalize the values between 0 and 1. Since ECAD only supports MLP networks, as of now, the input samples are reshaped to arrays of 784 elements which is a flattened representation of the 28x28 images of the MNIST data-set. The training and testing labels are converted to one hot arrays so that they can be used with the TensorFlows softmax with cross entropy function.

After all related TensorFlow variables are created a TensorFlow session is instantiated and the training can begin. The training data is batched and fed to the network and optimizer for the defined amount of epochs. The optimizer will reduce the loss calculated by the given cost function for each batch. After each full pass of the training data, the epochs accuracy is noted and the final accuracy is returned to the ECAD reader. After the training has been completed the reader will create a report JSON file storing the networks name/id, accuracy, the number of epochs, the full training time, and the batch size. The file is stored in the destination directory and is utilized by the evolutionary algorithm to pick the most optimal networks for further development.

If the saveWB argument is set, the ECAD reader will call the references to the weights and biases and extract them as float32 arrays. These are then converted to binary files and stored in the destination directory. For a MLP network two files per layer are created, one weights and one biases file, and each are named after the cell from the ecad file for easy reference. These files can be utilized for testing the FPGA designs to further check if the actual design has benefits on a hardware level. To make the files more usable, each file contains 4 integers at the beginning which describe the dimensions of the stored data.
Figure 1: ECAD flow.

Figure 2: ECAD configuration file sample.
3 Hardware Design

Analysis of deep neural networks (DNNs) shows that while state-of-the-art networks are becoming more accurate over time, it often comes at the cost of increased parameter size leading to higher computational complexity and/or power consumption. The authors of [4] show the correlations between the number of operations required for inference, the time taken to classify an image or batches of images, the power consumption of various hardware, and the resulting top-1 accuracy of current top performing models. It is evident that each neural network has a unique structure that may or may not fit in a certain system, i.e., there are trade-offs related to system constraints like power consumption, latency, classification accuracy, or throughput. Benchmarks that are run to arrive at these correlations are typically executed on instruction set based architectures like CPU or GPU. Similar instructions being called for each network allows for a nice baseline, however, the intended solution space we are interested in also includes re-configurable hardware which provides a unique pipeline system capable of molding to a networks unique structure.

Field Programmable Gate Arrays (FPGAs) provide a "sea of logic" that can be programmed and re-configured to create unique circuits by routing together various primitive building blocks like those found in Intel®'s Arria 10 [10] FPGA. Intel's Arria 10 FPGA provides variable precision DSP blocks that can be configured for either integer based or single precision floating-point multiply and add operations, 8-input fracturable look-up table based ALMs for implementing various logic functions, and embedded M20K memory blocks. Leveraging the flexibility of the FPGA, we can find unique solutions for all machine learning models.

The evolutionary algorithm will guide a search for optimal FPGA hardware designs given a specific machine learning problem and optimization goals. Accomplishing this requires the evolutionary algorithm to have hooks into the FPGA solution space. Due to the nature of most DNN operations being vector and matrix based, we chose a 2-dimensional systolic array of processing elements (PEs) as shown in Figure 4. The evolutionary algorithm has the capability to change the hardware configurations such as the array structures height, width, and PEs so that it may produce a new design for each permutation.

Systolic arrays are a great fit for FPGA because of their pipelined data flow indicated by the arrows
in Figure 4. They can be scaled across one or many devices allowing for efficient data and model parallel solutions where each array has the capability to be uniquely configured. They are also modular. PEs are designed to do a portion of the work, typically computing a partial result as a dot-product, and each PE can be replaced with different types, e.g., low-bit, dense, sparse, or other hardware efficient computations. Details on our hardware implementation will be discussed in the following section.

Every unique array configuration, or permutation, the evolutionary algorithm finds will be judged by a fitness evaluation. Fitness functions are created to give a score so that future generations converge toward a fitness goal. Goals can be anything from power efficiency, throughput, or logic utilization, for example. Many solutions exist that would be functionally equivalent but have very different hardware. Some solutions will be computationally faster and others slower yet use less power. The ability to search for various levels of fitness such as performance, power, or cost allows a single design space to satisfy the needs of different vertical markets.

Giving the evolutionary algorithm hooks into the hardware design space means providing a way for the evolutionary algorithm to modify the hardware description. Traditional hardware design done through a hardware description language such as Verilog allows for complete control over the hardware but does not provide a modular, software-like paradigm that would make this process straightforward. We address this issue by using OpenCL [11] which is a high-level, C99-based programming language that can be used with Intel’s FPGA SDK for OpenCL [12] to target Intel FPGA devices. OpenCL provides the software-centric workflow necessary for allowing the evolutionary algorithm to modify the hardware while also providing a means for optimized HDL code to be integrated in through specialized libraries.

### 3.1 2D Systolic Array Implementation

Figure 4 shows the high-level architecture for our systolic array implementation. Describing the data flow is best understood by starting with the processing elements (PEs) and following the data back to global memory. Each PE is responsible for computing a dot-product. Peripheral PEs (PE0, PE1, PE2) get one input from a memory module (MMod) and the other from a neighbor except for the very first PE (PE0) who receives both inputs from MMods. Inner PEs (PE3) receive their input from both neighbor PEs. Each connection to a PE (except for the OMod connections that will be covered shortly) carries several data elements equal to the vectorization parameter of the array, or in other words, the width of the dot product. Each element size in our designs is 32-bits single-precision floating point format, however, the bit-width of the data type is another parameter that could be adjusted by the evolutionary algorithm. After computing a single dot product, the PE will store its partial result in a local register to be used again until a complete
result is ready to be stored back to global memory. A complete result from a PE is a sub-block of the final output matrix. The size of the PE cache is based on the arrays interleaving parameter which will be discussed next as part of the MMod description.

Peripheral PEs are connected to a memory module (MMod) which is nothing more than a double buffer that glues global memory to the PEs. MMods provide a means to keep the PEs busy while new data is blocked in from DDR. Each MMod has a cache that is sized interleave x vectorization x 2 (height x width x depth). Interleaving is a parameter that is adjusted for balancing data reuse (to ease bandwidth constraints) and block size. The larger the interleaving factor, the more data reuse and less bandwidth that is required to feed the PEs, but the block size grows as well making it less efficient for mapping to smaller matrix sizes.

MMods receive data from their neighbor except the edge modules which receive data from loader kernels (depicted as A and B). Loaders are responsible for sequencing the right data at the right time so that each dot product computation is doing work towards the correct output matrix block. MMods also expect a specific order to incoming data because it first fills its own cache before (deterministically) forwarding all other incoming data through to its neighbor who in turn fills its own cache, etc. Further, given a specific global memory type (DDR in this case), loaders should take advantage of the cache line size to utilize as much global bandwidth and efficiency it can per read.

Once a block of data is ready to be saved back to global memory, the PEs start the draining process which begins by writing the contents of its cache to its neighbor. Results are drained in rows, so each PE drains along its column. The first row of PEs is connected to an output module (OMod) which are connected to each other in a daisy chain fashion. O Mods continue the draining process by propagating the results along to a global drain whose responsibility is to prepare the data to be written back to global memory. Data being drained arrives to the output modules in a non-contiguous way, so the global drain has its own local cache that is used to buffer data back to DDR. Contiguous memory writes back to global memory are the most efficient way to take full advantage of available bandwidth. The hardware supports a traditional MLP style of compute meaning that the global drain also includes DSP resources to add bias values to the draining data. Additionally, the global drain has the capability to perform the ReLU activation function on every element before writing the final result back to DDR.

3.2 Hardware Model

Modeling the hardware design allows the framework to search for both constrained and unconstrained designs. Unconstrained means that the evolutionary algorithm has less knowledge of the target hardware and has the freedom to search a much larger design space. When constrained, the evolutionary algorithm will only return configurations that it believes can be synthesized. Further, having a software-based model provides a much faster means of exploration compared to running through a series of hardware compiles.

The framework uses a hardware worker object that is targeted for a specific design like the 2D systolic array. Neural network description files containing information about cell parameters and connectivity are sent to the worker whose job is to return the fitness of that description in context to the hardware accelerator. If the targeted hardware model can 1. provide the necessary hooks to the evolutionary algorithm to allow new permutations and 2. provide the required fitness metrics, then any accelerator can be used in the search. ECAD currently uses the 2D systolic array hardware design as the sole model that is used in search.

Inputs to the current model are explained in section 3.1. Any model that is used in ECAD must have inputs or ”hooks” that allow the evolutionary algorithm to permute the design. After a permutation is created, it is then evaluated by the hardware worker who then provides the following results:

- **Total time (ms)** the total time in milliseconds that it takes the accelerator to run the provided network description file.
- **Potential giga-operations per second (GOP/s)** the maximum performance that can be expected out of the accelerator, also known as the roofline performance.
- **Effective GOP/s** actual performance of the accelerator. This number is derived by mapping the network description to the potential performance of the accelerator.
• **Images per second (img/s)** useful for workloads that contain image data sets such as the MNIST dataset used in most of our experiments.

• **Latency (ms)** the amount of time in milliseconds before the accelerator provides the first output.

Each result is sent back to the framework and depending on the optimization settings and various pressures used in the search, the results are evaluated and weighted to compute the overall fitness of that permutation.

4 Related Work

Automating NNA search has been an ongoing effort for the past few decades, driven by the difficulty in designing networks which are ever growing in complexity. Using Evolutionary Algorithms (EAs) to search for performant architectures has been investigated extensively [13][14]. The reason for using EAs, is that they offer the possibility of searching spaces that are too large or complex to be exhaustively searched. Evolving neural networks is referred to as Neuro-evolution [14].

Recently, there has been growing interest in automated architecture search for deep neural networks that specialize in image recognition [1][15][16]. The focus of those recent efforts is on improving accuracy for a given task (image processing). Our work on the other hand is focused on optimizing hardware for a given task using re-configurable architectures.

As deep and complex neural networks became increasingly popular and with the realization that existing hardware architectures are not specifically optimized for such computation, new forms of specialized architectures have been proposed and designed [5] to help increase performance and energy efficiency. Designing such static new architectures can be prohibitively expensive and risky since the field of neural computing is evolving so rapidly.

Optimizing hardware for neural networks is a research topic that is constantly evolving and correlating with the ever-changing network structures that are being developed. Recent publications have shown new architectures carving their niche in deep learning by offering unique methods for accelerating the workloads of neural network applications [17][18][19]. Specifically, these reconfigurable architectures are a popular platform for both research and deployment due to their ability to change their fabric routing and resource structures to fit various workloads and optimizations by leveraging the resiliency of neural networks through low-numeric precision [20][21] and sparsity [22][23]. Other accelerator designs use reconfigurable fabrics to change the logic routing to preprocess data and offload to a specialized ASIC [24].

5 Experiments

The MNIST dataset [25] is a database of handwritten digits, it has a training set of 60,000 examples, and a test set of 10,000 examples. This dataset has been used extensively in the literature to demonstrate the ability of a neural network design to achieve accuracy goals.

In the following experiments we use the MNIST dataset to test and validate our hardware resource estimator and the complete ECAD framework flow.

5.1 Verifying the Hardware Model

First, we validated our hardware model to ensure the results from our HWDBWorker were accurate. Targeting Intel’s Arria 10 GX 1150 FPGA platform, the model considered various hardware resources including available DDR blocks, DSPs, and embedded memories. Averaging across several hardware compiles, we arrived at a target clock frequency of 250 MHz. Verifying the hardware model was accomplished by comparing the HWDBWorker outputs to the measured results. When describing a particular configuration for the 2D systolic array, we will use the following notation: (rows, cols, vector width, interleave, scale) which are all defined in section 3.1
Our goal was to validate the hardware model running an actual workload to not only verify performance but also the accuracy of the results. For this, we trained a 4-layer MLP with (196/190/150/10) neurons on the MNIST dataset and compared the resulting classification accuracy with the FPGA after running all 10,000 images. The first hardware design we ran had the configuration (4, 4, 8, 8, 8). First, we created a configuration file with the hardware specifics and ran it through the HWDBWorker to determine the modeled performance of the accelerator. Next, we compiled the design and measured the hardware performance, both results are presented in Table 1. The resulting classification accuracy obtained from running the MLP in hardware matched the accuracy reported by the Simulator. The results show that for higher batching (64 and above), our model averages 95% accurate and 81.7% accurate across all tests. Lower batching for this design, which can be interpreted as a less efficient workload mapping, has a greater effect on model accuracy especially at batch 1. The smaller the workload, the shorter time the processing occurs inside the DSP blocks and the performance becomes harder to predict due to various overheads not accounted for. In other words, the variance we see in the measured results becomes less significant with larger workloads. The model is always initialized with the theoretical ceiling for performance and works its way down once it considers the workload. Two observations from our results are: 1. This model is providing the theoretical limit for these workloads so instead of looking at the model and attempting to change it to match the inefficiencies of the hardware, we will instead look at optimizing the hardware further to match the model and 2. our model remains consistent across permutations so that while some absolute performance results may vary (low batch for example) the relationship between permutations will always remain the same.

Table 1: Modeled vs measured performance for configuration (4, 4, 8, 8, 8) running an MLP

| Batch size | Modeled | Measured |
|------------|---------|----------|
|            | Effective GOP/s | Execution time (ms) | Effective GOP/s | Execution time (ms) |
| 1          | 1.16    | 0.38     | 0.65        | 0.679     |
| 16         | 18.6    | 0.38     | 10.3        | 0.68      |
| 32         | 37.2    | 0.38     | 20.7        | 0.68      |
| 64         | 40.3    | 0.7      | 35.81       | 0.78      |
| 128        | 42      | 1.35     | 39          | 1.43      |
| 256        | 42.98   | 2.63     | 41.2        | 2.74      |
| 512        | 43.47   | 5.2      | 41.5        | 5.45      |
| 1024       | 43.7    | 10.35    | 42.4        | 10.66     |
| 2048       | 43.84   | 20.64    | 43          | 21        |

5.2 MNIST Design Exploration

In the following design experiments, our goal is to find an optimized hardware solution for a given network structure that consists of an input layer, a single hidden layer and an output layer (784/N/10). The input is a 28X28 image and the output is the digit found in the input image.

We start investigating the different individual pressures on the design by running an evolutionary process on individual goals.

5.2.1 Optimizing for Accuracy

To optimize for accuracy, we select to run the simulator worker and create an evolutionary pressure towards accuracy. We do this by setting the goal to maximize accuracy. The simulator will be given different network designs, it will then simulate them using TensorFlow for a given number of epochs (4) and return the accuracy results. Figure 5 shows accuracy vs number of neurons as the evolutionary process progresses through the generations. As can be seen in Figure 5 after 50 generations the number of neurons rises to above 700. As the evolutionary process progresses it finds that to achieve high accuracy the number of neurons must fluctuate.
Figure 5: optimize for accuracy - accuracy vs number of neurons

Figure 6: optimize for img/s - images per sec vs number of neurons
Figure 7: optimize for img/s and min accuracy - images per sec vs number of neurons

Figure 8: optimize for img/s and min accuracy - hardware parameters
to between 748 and 1024 with the best result at 894. Some support for these results can be found in the literature. Several prior works report competitive results for a single hidden layer of neurons containing 800 neurons.

5.2.2 Optimizing for Images per Second

In this stage our goal is to try to force the evolving hardware design to output the most images per second. This would be a common goal in hardware design exploration especially when using re-configurable hardware with a low overall power envelope. By maximizing the number of images per second (img/s) we could potentially save money and conserve energy. To create such evolutionary pressure, we use our HWDBWorker to evaluate potential designs and return information such as the images per second (see [25]) which we could use to select upon in the evolutionary process. As can be seen in Figure 6 to achieve an optimal number of img/s, the evolutionary process put pressure on the number of neurons to drop. In fact, to achieve the optimal performance, the number of neurons tends towards zero, this is because the EA found that less computation, i.e., less neurons, resulted in a higher throughput and because there was no pressure to maintain accuracy, it continued to drop. During this particular search, the hardware configuration started to converge (4,8,8,16,18) while the batch size began to rise (to 1024) and the neurons remained low. This resulted in hardware that was 100% efficient in the "batch" dimension which is used in every layer. Since the MNIST dataset requires an input size of 784, the EA needed to find a common dimension through the vector width and scale parameters that both kept total execution time of the MLP down but could also process the input efficiently. This dimension mapped to 91% efficiency. The trend of reducing the neurons did work for the EA but had pressure been placed on accuracy, it would have found it could utilize the entire common dimension with neurons.

5.3 Optimizing for both Accuracy and Images per Second

Now that we understand the different conflicting pressures we proceed to try and find an optimal compromise between the accuracy and the images per second (img/s) metric. If we do not give a constraint on each of the objectives our evolutionary process will find some middle ground compromise which might not be suited for our needs. So instead we force the evolutionary process towards a minimum accuracy goal and a maximum number of img/s goal. Figure 7 shows the resulting evolutionary process and the optimal combination of img/s. The minimum accuracy goal is set to ninety percent. The best img/s result (129,144) is lower than the unconstrained accuracy version (362,844) but given a minimum accuracy of 90% this result could be used in a practical design.

Trends in the hardware configurations that the EA displayed can be visualized in Figure 8. We noted previously that to get the best accuracy, the algorithm uses more neurons, yet to get the best performance, typically less neurons are desired. This forces the EA to find better results for how well the neurons are mapping on hardware. Table 2 shows the results of the top permutations for the optimization process. The only parameters that seem to be different are the columns, vector width, and interleaving factor. Rows seem to have converged to 2 because input to an MLP without batching is a vector and the EA decided that making this dimension in hardware small, better fits the solution. Further, batching during inference does not affect accuracy so the hardware is better utilized in other dimensions. Scale also converges at 2 and this is most likely because this parameters can be thought of as quantization along the matrix common dimensions, and a smaller number may result in a better fit. Beyond efficiency mapping, scale also provides a trade-off with global (off-chip) memory bandwidth, and because our model considers DDR memory reads and writes, scale will generally tend to be lower to help balance the transactions. The third column, fitness sum, gives the results of what the EA found to be the best fit solution given pressures. We notice that all the results lie in between the top permutations for accuracy and effective GOP/s. These results show how small variations in permutations yield large variations in fitness evaluations, and in most cases, top performers arrive at unique solutions that may never be considered if designed by hand.
Table 2: Top permutations from optimizing accuracy and img/s

| HW Config     | Accuracy | Effective GOP/s | Fitness Sum |
|---------------|----------|-----------------|-------------|
| 2,8,16,16,2   | 0.942    | 0.933           | 0.936       |
| 2,16,32,32,2  | 0.933    | 200.98          | 174         |
| 2,8,32,16,2   | 0.936    | 174             | 174         |

5.4 Hardware Generation and Measured Results

Now that we have a list of feasible permutations with the desired optimizations, we use the ECAD hardware flow to synthesize the design. This is achieved by exporting the neural network from the ECAD database into a network description file that can be fed to the ECAD framework for partial or complete hardware compile. A simple command line accepts the exported design and starts the build process.

During search, the HWDBWorker only returns configurations it believes to be valid, however, there are some cases where a design may not pass hardware compilation due to excess resource utilization. The recommended next step after search completes is to run a partial compile on the top performers. Partial compiles provide detailed information on resource utilization but the process takes a few minutes to complete which is why partial compiles are done after search completes. After finding the top performer that passes the partial compilation stage, it is sent through the full hardware flow which includes bitstream generation and testing in hardware. Currently, this process of weeding out designs that cannot produce hardware is done by hand, but could be automated into a post search process.

Performance results from running the top permutations in Table 2 through hardware are presented in Table 3 and their corresponding logic utilization are presented in Table 4. All the top permutations in Table 2 were valid configurations and passed the full hardware compilation stage. For convenience, the hardware configuration notation is rows, columns, vector width, interleaving, and scale. The execution time measured in milliseconds is the total time it takes to run a batch of MNIST images through the 2-layer MLP in hardware. These results further validate the hardware model. Table 4 shows as a percentage, how many resources each design is using. Note that each Fmax is slightly lower than the 250 MHz we searched at. This, in part, is due to only compiling a single seed design and having run more compiles could have resulted in an Fmax closer to that target. The model execution time listed in the table was scaled from 250 MHz to the actual MHz that the design closed at.

Table 3: Hardware performance results compared to model for top permutations

| Hardware Configuration | Modeled Execution Time (ms) | Measured Execution Time (ms) |
|------------------------|----------------------------|----------------------------|
| 2,8,16,16,2            | 9.59                       | 9.64                       |
| 4,8,8,16,18            | 4.66                       | 4.65                       |
| 2,8,32,16,2            | 4.64                       | 5.53                       |

Table 4: FPGA resource utilization for top permutations

| Hardware Compile | Partial Compile |
|------------------|-----------------|
| Hardware Configuration | Fmax | ALM | M20K | DSP | ALM | M20K | DSP |
| 2,8,16,16,2      | 220.41 | 37% | 36%  | 26% | 47% | 38%  | 26% |
| 4,8,8,16,18      | 228.26 | 38% | 34%  | 26% | 45% | 37%  | 26% |
| 2,8,32,16,2      | 212.18 | 50% | 30%  | 43% | 61% | 55%  | 43% |
6 Conclusions

We present a novel framework (ECAD) for the exploration and design of Neural Network Architectures (NNAs) based on evolutionary algorithms. We use a reconfigurable-hardware/software co-design approach to optimize NNA designs on both the software and the hardware side. We discuss and demonstrate the possibility to optimize NNA designs for different and multiple optimization objectives instead of the predominant approach to focus on accuracy optimization alone. Performance data of the top permutations for different optimizations including accuracy, img/s, and both simultaneously, is presented along with the complete end-to-end ECAD flow targeting an Intel FPGA Arria 10 1150 GX device. Finally, comparing the hardware performance of the top permutations against our model served to validate the results of the evolutionary process.

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References

[1] Hanxiao Liu et al. “Hierarchical representations for efficient architecture search”. In: arXiv preprint arXiv:1711.00436 (2017).
[2] Martin Abadi et al. “Tensorflow: A system for large-scale machine learning”. In: 12th Symposium on Operating Systems Design and Implementation 16. 2016, pp. 265–283.
[3] Antonio Gulli and Sujit Pal. Deep Learning with Keras. Packt Publishing Ltd, 2017.
[4] Alfredo Canziani, Adam Paszke, and Eugenio Culurciello. “An analysis of deep neural network models for practical applications”. In: arXiv preprint arXiv:1605.07678 (2016).
[5] Norman Jouppi et al. “Motivation for and Evaluation of the First Tensor Processing Unit”. In: IEEE Micro 38.3 (2018), pp. 10–19.
[6] David E Goldberg and Kalyanmoy Deb. “A comparative analysis of selection schemes used in genetic algorithms”. In: Foundations of genetic algorithms. Vol. 1. Elsevier, 1991, pp. 69–93.
[7] Thomas Rauber and Gudula Rünger. Parallel programming: For multicore and cluster systems. Springer Science & Business Media, 2013.
[8] Edgar Gabriel et al. “Open MPI: Goals, concept, and design of a next generation MPI implementation”. In: European Parallel Virtual Machine/Message Passing Interface Users’ Group Meeting. Springer. 2004, pp. 97–104.
[9] Diederik P. Kingma and Jimmy Ba. Adam: A Method for Stochastic Optimization. 2014. arXiv:1412.6980 [cs.LG].
[10] Intel Arria10 Device Overview. 2018. URL: https://www.intel.com/content/www/us/en/programmable/documentation/sam1403480274650.html (visited on 04/09/2018).
[11] The open standard for parallel programming of heterogeneous systems. URL: https://www.khronos.org/opencl/.
[12] Intel FPGA SDK For OpenCL. URL: https://www.intel.com/content/www/us/en/software/programmable/sdk-for-opencl/overview.html.
[13] Geoffrey F Miller, Peter M Todd, and Shailesh U Hegde. “Designing Neural Networks using Genetic Algorithms.” In: ICGA. Vol. 89. 1989, pp. 379–384.
[14] Kenneth O Stanley and Risto Miikkulainen. “Evolving neural networks through augmenting topologies”. In: Evolutionary computation 10.2 (2002), pp. 99–127.
[15] Esteban Real et al. “Large-scale evolution of image classifiers”. In: *Proceedings of the 34th International Conference on Machine Learning-Volume 70*. JMLR. org. 2017, pp. 2902–2911.

[16] Barret Zoph et al. “Learning Transferable Architectures for Scalable Image Recognition”. In: 2018 IEEE/CVF Conference on Computer Vision and Pattern Recognition (2018), pp. 8697–8710.

[17] Utku Aydonat et al. “An OpenCL(TM) Deep Learning Accelerator on Arria 10”. In: *CoRR* abs/1701.03534 (2017). arXiv: 1701.03534 [url: http://arxiv.org/abs/1701.03534].

[18] Naveen Suda et al. “Throughput-Optimized OpenCL-based FPGA Accelerator for Large-Scale Convolutional Neural Networks”. In: *Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*. FPGA ’16. Monterey, California, USA: ACM, 2016, pp. 16–25. DOI: 10.1145/2847263.2847276 [url: http://doi.acm.org/10.1145/2847263.2847276].

[19] Jinhwan Park and Wonyong Sung. “FPGA based implementation of deep neural networks using on-chip memory only”. In: *2016 IEEE International Conference on Acoustics, Speech and Signal Processing, ICASSP 2016, Shanghai, China, March 20-25, 2016*. 2016, pp. 1011–1015. DOI: 10.1109/ICASSP.2016.7471828 [url: https://doi.org/10.1109/ICASSP.2016.7471828].

[20] Philip Colangelo et al. “Exploration of Low Numeric Precision Deep Learning Inference Using Intel FPGAs”. In: *CoRR* abs/1806.11547 (2018). arXiv: 1806.11547 [url: http://arxiv.org/abs/1806.11547].

[21] Yaman Umuroglu et al. “FINN: A Framework for Fast, Scalable Binarized Neural Network Inference”. In: *CoRR* abs/1612.07119 (2016). arXiv: 1612.07119 [url: http://arxiv.org/abs/1612.07119].

[22] Ganesh Venkatesh, Eriko Nurvitadhi, and Debbie Marr. “Accelerating Deep Convolutional Networks using low-precision and sparsity”. In: *2017 IEEE International Conference on Acoustics, Speech and Signal Processing, ICASSP 2017, New Orleans, LA, USA, March 5-9, 2017*. 2017, pp. 2861–2865. DOI: 10.1109/ICASSP.2017.7952679 [url: https://doi.org/10.1109/ICASSP.2017.7952679].

[23] J. Yinger et al. “Customizable FPGA OpenCL matrix multiply design template for deep neural networks”. In: *2017 International Conference on Field Programmable Technology (ICFPT)*. Dec. 2017, pp. 259–262. DOI: 10.1109/FPT.2017.8280155.

[24] Eriko Nurvitadhi et al. “In-Package Domain-Specific ASICs for Intel®Stratix®10 FPGAs: A Case Study of Accelerating Deep Learning Using TensorTile ASIC(Abstract Only)”. In: *Proceedings of the 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*. FPGA ’18. Monterey, CALIFORNIA, USA: ACM, 2018, pp. 287–287. ISBN: 978-1-4503-5614-5. DOI: 10.1145/3174243.3174966 [url: http://doi.acm.org/10.1145/3174243.3174966].

[25] Yann LeCun. *THE MNIST DATABASE of handwritten digits*. 1998. URL: http://yann.lecun.com/exdb/mnist/ (visited on 02/24/2019).

[26] The 1st International Workshop on FPGAs for Domain Experts. Nov. 2018. URL: http://tytra.org.uk/fpode/ (visited on 03/03/2019).