Cryogenic characterization of 180 nm CMOS technology at 100 mK

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ABSTRACT: Conventional CMOS technology operated in cryogenic conditions has recently attracted interest for its use in low-noise electronics. We present one of the first characterizations of 180 nm CMOS technology at a temperature of 100 mK, extracting I/V characteristics, threshold voltages, and transconductance values, as well as observing their temperature dependence. We find that CMOS devices remain fully operational down to these temperatures, although we observe hysteresis effects in some devices. The measurements described in this paper can be used to inform the future design of CMOS devices intended to be operated in this deep cryogenic regime.

KEYWORDS: Electronic detector readout concepts (solid-state); Front-end electronics for detector readout

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1 Introduction

Microelectronics manufactured using conventional CMOS processes but operated at cryogenic temperatures of 4 K and below have recently attracted interest in quantum computing for their use as precision controllers and low noise amplifiers [1, 2]. This method of incorporating electronics directly into the cryogenic environment instead of operating them at room temperature can offer similar advantages in experiments like CUORE (Cryogenic Underground Observatory for Rare Events), which uses a cryogenic bolometric approach to search for neutrinoless double beta decay. CUORE uses Neutron Transmutation Doped (NTD) thermistors on TeO$_2$ crystals to sense temperature changes induced by physical energy deposits. At the moment, all the CUORE electronics, including those for biasing the NTDs, amplifying the signals, and performing readout, are operated at room temperature [3]. The future CUORE Upgrade with Particle ID (CUPID) plans to take advantage of the general cryogenic infrastructure developed for CUORE, but an upgrade to its electronics infrastructure is under consideration [4]. CMOS microelectronics engineered to be operated at or below 4 K offer an alternative approach to signal preamplification in CUPID, allowing a reduction in electronic noise and a possibility of introducing a modest channel multiplexing factor.

To date, there are very few measurements of CMOS device properties at sub-Kelvin temperatures, which will have to be understood if we wish to consider using them to construct amplifiers and multiplexers near the base operating temperature of CUPID. In this paper we present one of the first characterizations of 180 nm CMOS technology down to 100 mK, which will be used to inform the design of these devices.

2 Setup

We conduct our characterization measurements with a TSMC 180 nm CMOS test chip containing multiple arrays of PMOS and NMOS devices of a variety of thresholds with the widths and lengths varying from 180 nm to 10 µm. The MOSFET structures for quasi-static voltage-current (I/V) scan
characterization are shown in figure 1. We selectively wirebond the devices to be measured out of the array. The chip is placed at the mixing chamber stage of an Oxford Triton-400 dilution refrigerator, kept at 100 mK for these measurements. For voltage biasing and current readout, the MOSFETs are wired out to a Keithley 2450 SMU and a Keithley 6517B electrometer outside the cryostat. Since the dilution refrigerator has limited cooling power, the device power consumption was kept to a minimum by limiting the input voltage, the current range, and the amount of time they were kept on.

3 Results

3.1 Characterization

We perform standard I/V scans for an assortment of PMOS and NMOS devices on the test chip. All MOSFETs tested remain operational down to temperatures of < 100 mK; examples of I/V scan curves are shown in figure 2. From these measurements, we extract the transconductance and the threshold voltage. Their temperature dependence is shown in figure 3. The threshold voltage is obtained by plotting the drain current \( I_d \) against the gate voltage \( V_g \), extrapolating from the linear region of the \( I_d-V_g \) curve, and then finding the intersection with the \( V_g \) axis [5]. We observe that the threshold voltage increases as the temperature goes down; general models of MOSFET behavior predict that threshold voltage should scale as \( V_{th} \propto (V_{th,0} - T) \), and our data suggests no significant deviations from this behavior all the way down to 100 mK. Uncertainties in the threshold voltages are primarily due to uncertainties in the linear extrapolation of the \( I_d-V_g \) curves.

We select a simple square-law MOSFET model in order to obtain an approximation of transconductance in both the linear region and the saturation region. The drain current in each of these regions is given by

\[
I_D = 2k \left[ (V_g - V_T) V_d - 0.5 V_d^2 \right] \quad \text{(linear region)}
\]

\[
I_D = k (V_g - V_T)^2 \quad \text{(saturation region)}
\]
where $k$ includes details from the characteristic feature size and manufacturing process of the MOSFET and generally has a temperature dependence of $k \propto T^{-3/2}$ due to carrier mobility effects. For both of these regions, this gives an expected $g_m \propto T^{-3/2}$ relationship. However, while we observe that $g_m$ does increase at lower temperatures, this relation does not seem to hold for the entire temperature range. This indicates that this basic model likely becomes invalid at sufficiently low temperatures, where other effects such as carrier freeze-out may become relevant.

3.2 Hysteresis effects

Some of the MOSFETs exhibit a hysteresis effect when operated at low enough temperatures, with a kink appearing in the characteristic I/V curves when scanning from low $V_d$ to high $V_d$, but not when going from high $V_d$ to low $V_d$, as shown in figure 4. This effect is observed in different sized devices to different degrees, and the effect disappears once the temperature of the devices is high enough. The temperature dependence of this feature indicates it is likely related to charge carrier freeze-out in the MOSFETs. A similar kink in the I/V curves at cryogenic temperatures has previously been observed in [6], where it was explained by the formation of a forced depletion layer near the pinchoff region of the MOSFET. Taking NMOS for example, in this model, $V_d$ is high enough to cause impact ionization in the pinchoff region of the transistor as it starts to form. The electrons freed by this process then join the drain current, while the holes are pulled deeper into the substrate, enjoying the high carrier mobility induced by the low temperatures. The freed electrons from this initial forced formation of the depletion layer cause an increase in the drain current, but after the layer is formed it allows charge carriers coming from the inversion layer to pass through it normally without further interaction. This effect is only present at temperatures where carrier freeze-out is significant, as otherwise the depletion layer in the pinchoff region of the transistor can form normally from the movement of thermally excited charge carriers. The kink also does not occur when scanning from high $V_d$ to low $V_d$, as the extra current caused by the formation of the depletion layer does not change the monotonically decreasing drain current as drain voltage is decreased.

This explanation matches several of the characteristics of the hysteresis effect that we have observed. The magnitude of the kink in the I/V curves is smaller for NMOS with smaller channel
sizes, as seen in the top figures of figure 4, which matches the expectation of a smaller current surge from the formation of a smaller depletion layer. We observe that the effect gradually decreases in size as temperature increases until it disappears around 40 K, which is where carrier freeze-out should start becoming insignificant in our silicon-based substrates. We also did not observe this effect in our PMOS devices (see figure 2), which matches the model’s expectation that forced depletion layer formation is suppressed in PMOS due to the substantially lower substrate currents.

3.3 Simulation

We apply a basic BSIM3 model to try to replicate the behavior of our devices at cryogenic temperatures, tuning a limited set of the model parameters to fit the measurements [7]. The BSIM3 model is not designed to work below around 220 K, but previous work has shown it is possible to phenomenologically tune the model parameters to work down to 77 K [8, 9], and possibly even down to 4 K [10]. We tune the $V_{ih0}$, $K_1$, $U_A$, and $U_B$ parameters using measurements from one device size and then apply the resulting model to other sizes for comparison. An example is shown in figure 5, where the BSIM parameters are tuned to a 0.5/1.2$\mu$m NMOS at 100 mK but it can be seen that

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure3.png}
\caption{Top left: $I_d/V_g$ plot for a $W/L = 0.5/10\mu$m] NMOS, evaluated at $V_d = 0.02$ V. Top right: $I_d/V_g$ plot for a $W/L = 10/0.25\mu$m] PMOS, evaluated at $V_d = 0.02$ V. Bottom left: extracted threshold voltages for each device as a function of temperature. The lines are fits for $V_{th}$ as a linear function of temperature, with $\chi^2/DoF = 4.1/7$ for the NMOS and $\chi^2/DoF = 3.5/5$ for the PMOS. Bottom right: the maximum transconductance in the scan range for each device, evaluated in both the linear and saturation regions, as a function of temperature.}
\end{figure}
Figure 4. Characteristic I/V curves with $V_g$ scanned in 0.02 V increments, showing the presence of a temperature-dependent hysteresis. Top left: $W/L = 0.5/0.5 \mu m$ NMOS at 100 mK, for both increasing and decreasing scans of $V_d$, where it can be seen that the kinks are only visible when $V_d$ is increased. Top right: $W/L = 10/1.2 \mu m$ NMOS at 100 mK, where the same kind of behavior is observed. Bottom left: $W/L = 10/1.2 \mu m$ NMOS at 30 K, where the kinks are still present but less prominent. Bottom right: $W/L = 10/1.2 \mu m$ at 40 K, where the kinks have disappeared.

The resulting model does not accurately predict the I/V characteristics of a $0.5/0.5 \mu m$ NMOS at the same temperature. However, the simulated I/V curves obtained from the BSIM3 model work well for all device sizes at room temperature as expected, so this suggests that the size-dependence of the I/V characteristics changes substantially at very low temperatures in a manner that we have not captured. Further tuning of this model will be possible with measurements on a larger range of device sizes.

4 Conclusions

In this work, we have demonstrated successful operation of 180 nm CMOS technology down to temperatures of 100 mK and performed one of the first characterizations of its properties in this temperature range. We find that CMOS behavior at this temperature is qualitatively similar to the behavior at 4 K observed in previous works, which is a first step towards establishing that their usage as signal amplifiers or multiplexers can be extended down to temperatures as low as 100 mK. Such amplifiers will likely use MOSFETs operated in the weak inversion region in order to satisfy
the power budget allowed by a dilution refrigerator at these temperatures. While we have observed significant hysteresis effects in some NMOS devices, this can be accounted for in amplifier designs to avoid any undesirable effects on amplifier performance. Future extensions of this work will involve measurements with a larger range of device sizes to fine-tune our models of cryogenic behavior, as well as testing CMOS-based signal amplifiers in the 10 to 100 mK range, with the goal of minimizing noise and optimizing performance within the power dissipation constraints imposed by a dilution refrigerator.

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