Development of a low power and high integration readout ASIC for time projection chambers in 65 nm CMOS

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Abstract. The paper presents the development of a low power readout ASIC for time projection chambers (TPCs) for the CEPC (Circular Electron Positron Collider) experiments. In order to achieve high spatial and momentum resolution, large number of readout channels is demanded with waveform sampling capability in the resolution of 8-10 bit and the sampling rate of 10-40 MS/s. Power consumption became critical and has been addressed by using advanced 65 nm CMOS process and simplifying the analog circuits in our design. The prototype chip has been developed including the analog front-end and the waveform sampling SAR (Successive Approximation Register) ADC. This paper will present the detailed circuit design and test results. The development of the digital trapezoidal filter will also be described.

1. Introduction
The time projection chamber (TPC) can provide large-volume high-precision 3D track measurement with low material budget and hence has been widely applied in particle and nuclear physics experiments, including ILC (International Linear Collider) and CEPC (Circular Electron Positron Collider) experiments [1,2,3,4]. In order to achieve high spatial resolution small pads (~6 mm²) are needed, resulting in ~1 million channels of readout electronics per endcap [5]. The power consumption become critical especially for CEPC since the front-end electronics need to work continuously. Several TPC readout ASICs have been developed in the past two decades, including ADC based ASICs such as PASA/ALTRAO [6] and more recently SAMPA [7] and SCA based ASICs such as AFTER [8] and AGET [9]. However, none of these ASICs can meet the stringent requirements of low power consumption and high event rate for CEPC TPC. This motivated us to develop a low power and high integration readout ASIC for TPC using more advanced 65 nm CMOS process.

CMOS scaling only favors digital circuits and on the contrary brings more difficulties for analog circuits. The CR-RG shaper and the SAR (Successive Approximation Register) ADC were adopted for their simplicity in analog circuits and hence the power efficiency. The digital signal processing (DSP) circuits can then be applied such as baseline restoration, trapezoidal shaping and data compression. The prototype of readout ASIC has been developed in 65 nm CMOS, including the preamplifier and shaper...
as the analog front end (AFE) and a SAR ADC for waveform sampling. Trapezoid filter is implemented in Matlab and applied to the measured waveform samples. Section 2 will present the chip architecture and specifications. Circuit design will be described in Section 3 and test results and analysis will be shown in Section 4.

2. Chip Architecture and Specifications
The architecture diagram of the TPC readout electronics for CEPC is shown in figure 1. The front-end electronics consists of the AFE, the waveform sampling ADC, the DSP (digital signal processing) circuits with data compression and the de-randomize event buffer for each channel. The detector current signal is amplified by the preamplifier, followed by a semi-Gaussian shaper. The simplest CR-RC shaper has been adopted for low power consumption. Comparing to high order shapers, its output has a relatively long decay tail. Symmetric shapes such as trapezoid can be obtained by low power digital filters. The architecture of the SAR ADC is using only one comparator and a capacitive DAC (Digital to Analog Converter) in analog parts. After digitization, digital filters can be applied for better noise and more symmetrical pulse shape. Continuous sample data will be reduced by either zero suppression or Huffman coding. High speed serial link will be used to collect the data stored in event buffers and transmit to the DAQ (Data Acquisition System) for further processing.

![Figure 1. The architecture diagram of the TPC readout electronics.](image)

The first prototype TPC readout chip has been developed, focusing on the AFE and the ADC parts. The key specifications for the prototype chip are listed in table 1, including the specifications for the AFE and the ADC respectively. The total power consumption of less than 5 mW per channel is required, considering ~1 kW practical cooling power per endcap.

| AFE | Shaper | CR-RC | Shaping time | ~160 ns |
|-----|--------|-------|--------------|---------|
| Gain | ~10 mV/fC | Dynamic Range | 120 fC |
| ENC  | 500 e @ 10pF input cap | Resolution | 10 bit |
| ADC | Sampling rate | ≥20 MSPS | Power | ≤5 mW per /channel |
| Total channels | 0.5-1 million per endcap |

3. Chip Design

3.1. The AFE
The block diagram of the AFE is shown in figure 2. It consists of a CSA (charge sensitive amplifier) and a CR-RC shaper in two stages. The core amplifier of the CSA is based on folded cascode topology to obtain high gain and high output swing. The first stage CR shaping amplifier is implemented with a classic two stage OTA (operational transconductance amplifier) and a source follower. The second shaping stage amplifier is fully differential with CMFB (Common Mode Feed-Back). Both common mode and differential baseline voltages can be adjusted externally.

As the power supply voltage in 65 nm CMOS is reduced to 1.2 V, the output swing of each amplifier stage needs to be carefully optimized. The native NMOS transistor has been used for the source follower. The main noise contribution of the AFE is from the series voltage source of the input transistor of the CSA. It has been optimized for 10 pF input capacitance.
3.2. The SAR ADC
As shown in figure 3, the core of the SAR ADC consists of a sampling and hold (S/H) stage, a comparator, a DAC (digital-analog converter), and digital control logic [10]. Analog components are simplified compared to other ADC architectures such as the pipeline ADC. Since there is only one comparator, the input voltage is compared to the DAC thresholds for multiple times and for each time the DAC threshold is changed by the SAR logic according to the previous quantization result.

The most power consuming component in the SAR ADC is the capacitive DAC. Each capacitor value can be trimmed to compensate the mismatch and hence the power consumption is lowered further by using small capacitors. The trimmed value can be obtained through the calibration process based on code density statistic. A triangular signal generator is also implemented for calibration on chip. More details about the SAR ADC can be found in Ref [10].

3.3. The Chip Layout
The layout of the prototype ASIC is shown in figure 4, with the die size of the 1.8 mm x 0.44 mm. The die area of the AFE and the ADC are 1.06 mm x 0.18 mm and 0.48 mm x 0.18 mm respectively. The AFE and the ADC have isolated power supplies and grounds in order to reduce interference coupling from ADC to AFE.
4. Test Results

The test setup of the prototype chip is shown in figure 5. The chip is mounted on a dedicated test PCB board. It is powered with 1.2 V voltage and the input charge is injected with square wave signal through a 1pF serial capacitor for each channel. A clean clock of the ADC is provided by a SMB100 signal generator. The FPGA development board (TSW1400 EVM) is used for data acquisition. The data is transmitted to computer for further processing. The power consumption, the linearity and the ENC (Equivalent Noise Charge) of the chip are measured during the tests.

4.1. Power Consumption

The power consumptions of the AFE and the ADC part have been measured independently. The master bias current of the chip can be adjusted through an off-chip bias resistor. The consumed current of test PCB increases linearly with the master bias current, as shown in figure 6. The current and hence the power consumption of the ASIC chip can then be estimated from the slope of the linear fit. The power consumption of analog part was estimated to be 2.5 mW/channel when the master bias current is 25 \( \mu \)A.
The power consumption of the ADC is measured to be 5.41 mW/channel at 50 MS/s sampling rate. According to circuit simulation, the core of the SAR ADC consumes only 1/4 (1.35 mW/channel) of the whole SAR ADC circuits and the other 3/4 power is consumed by the referred buffer and the clock generation modules. There are common modules shared with all channels and hence the power consumption per channel for these modules will decrease as the channel number increases.

4.2. Linearity
The linearity is evaluated by injecting charges from 3 fC to 120 fC. The ADC output waveforms for different injected charges are shown in figure 7. The shaping time is about 160 ns. The pulse amplitude increases linearly with the injected charge, as shown in figure 8. For each injected charge, 200 groups of pulses were acquired and the mean value of the peak amplitude is used for fitting. The gain is estimated to be 5.08 LSB/fC with 1 LSB (Least Significant Digit) in 2 mV. The maximum INL (integral-nonlinearity) is about 0.55%.

4.3. ENC
The ENCs are measured for different input capacitances, as shown in figure 9. For each input capacitance, 10 groups of pedestal samples are acquired with each group consists of 5000 data points. The standard deviation is calculated as the output variance for ENC estimation. The measured ENC is fitted to be $633 \ e + 27.5 \ \text{e/pF*Cin}$, which is higher than the simulation results ($501 \ e + 3.2 \ \text{e/pF*Cin}$). The noise slope is much higher than the simulation results, indicating existence of the excess noise source or interference coupled to the input of the ASIC.
4.4. The Trapezoidal Filter

4.4.1. Implementation

Digital trapezoidal filter is implemented in MATLAB and applied to the measure waveforms. The block diagram of the trapezoidal filter based on unfolding method is shown in figure 10 [11]. The exponential signal is firstly unfolded into the unit impulse and then the trapezoidal output pulse is synthesized by accumulating, truncating and moving averaging. The hardware resource for the trapezoidal filter is minimized and hence low power consumption and compact size can be achieved. The output voltage signal of ASIC is filtered by trapezoidal filter with 0.2 us rise time and flat top time in MATLAB and the main node voltage signals of trapezoidal filter are shown in figure 11.

![Figure 10. The block diagram of trapezoidal filter.](image)

4.4.2. ENC with Trapezoidal Filtering

When the flat top of the trapezoid is longer than the maximum detector charge collection time, ballistic deficit can be avoided. The ENC with the trapezoidal filtering is shown in figure 12. Both the rise time and flat top time of the trapezoidal filter are 0.2 us. The ENC is fitted to be 592 e + 18 e/pF*Cin, which is lower than the result without filter. The ENC performance is improved with trapezoidal filter.

![Figure 11. The main node voltage signals of trapezoidal filter.](image)

![Figure 9. The ENC over different input capacitance.](image)
5. Conclusions
A low power and high integration TPC readout ASIC has been developed using 65nm CMOS process. The first prototype chips have been designed and tested. The test results showed in good agreement with the specifications including the power consumption, linearity and the ENC. The superior power consumption of 2.5 mW and 1.35 mW were achieved for the analog front-end and the SAR ADC core. The gain and maximum INL was measured to be 5.08 LSB/fC and 0.55% respectively. The measured ENC is fitted to be 633 e + 27.5 e/pF*Cin. After trapezoidal filtering, the ENC is fitted to be 592 e + 18 e/pF*Cin. The ENC performance is significantly improved with trapezoidal filter. A 16 channels of full chain readout ASIC is also under development. Several digital filters and compression methods are under study.

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