A 3.8 MHz CMOS Wien-bridge oscillator with differential capacitive automatic amplitude control

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Abstract: A 3.8-MHz Wien-bridge oscillator is designed in low-cost 0.35 µm CMOS process. The amplifier gain control is done by MOS capacitors rather than by more nonlinear MOS resistors. A differential amplitude control loop controls two MOS capacitors in differential manner, which greatly reduces the feedback loop bandwidth without using any off-chip filters, hence almost completely eliminate the unwanted operating point disturbance of the oscillator core. The fabricated chip consumes 0.22 mA from 2 V supply, and shows −41.1 dB of second harmonic component and −94.3 dBc/Hz phase noise at 100 kHz offset.

Keywords: Wien-bridge, harmonic oscillator, automatic amplitude control, ultra-low-power, CMOS

Classification: Integrated circuits

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1 Introduction

Ultra low power (ULP) radios have become increasingly needed as various energy-efficient long-battery-life wireless applications such as wireless sensor radios, internet-of-things, medical implantable devices, healthcare and monitoring circuits, emerge [1]. Many circuit design techniques for minimizing power consumption can be found in literature, for instance, in receiver [2], transmitter [3], and VCO [4]. However, ULP radios will not be possible unless a stable and precision clock generator can be also integrated on a chip. Only on-chip clock generators can remove bulky crystals out of total systems and thus improve the system form factor.

Possible candidates for sub-mW few-MHz on-chip CMOS clock generator include Wien-bridge oscillator [5], relaxation oscillator [6], and ring oscillator [7]. Among the three, Wien-bridge is the only harmonic oscillator that can provide a sinusoidal output while others provide an output with high harmonic contents. Such sinusoidal output is more favorable for various subsequent analog signal processing. Also, since the output frequency of the Wien-bridge is solely determined by passive RC components and not influenced by the active device parameters, the output frequency usually shows better accuracy and stability over process and temperature.

A previous 6-MHz Wien-bridge oscillator [5] was realized in 65 nm CMOS. But a lower cost CMOS process is desired for the wireless sensor nodes. Thus, this work presents a Wien-bridge oscillator in a lower-cost 0.35 µm CMOS technology. Also, this work adopts a capacitive gain control technique rather than a conventional more-nonlinear resistive gain control adopted in [5]. Moreover, this work introduces a differential amplitude control scheme in order to reduce the feedback loop bandwidth dramatically and thus eliminate an otherwise needed off-chip RC filter.

2 Circuit design and implementation

Fig. 1 shows a block diagram of a conventional Wien-bridge oscillator with an automatic amplitude control (AAC). A1 and RC’s around it form the Wien-bridge core. The loop gain is given by

\[
L(j\omega) = \frac{1 + C_2/(C_1 + C_F)}{3 + j(\omega CR - 1/\omega CR)}. \tag{1}
\]
Barkhausen criterion is met at $\omega = (RC)^{-1}$ when the amplifier gain $1 + C_2/(C_1 + C_V)$ becomes three. AAC is composed of a peak detector, $A_2$, and a low-pass filter (LPF). It controls the MOS capacitor $C_V$ to regulate the amplifier gain to a desired value.

The gain control by using a MOS capacitor is chosen rather than by using a conventional triode-region MOS variable resistor. Compared to the MOS variable resistor, the MOS capacitor provides more smooth transition of capacitance over a wider range of the control voltage $V_{\text{tune}}$. Yet, this capacitive gain control imposes a serious problem. A unwanted feedthrough from $V_{\text{tune}}$ to $V_{\text{out}}$ can drive the oscillator out of proper operating condition during the AAC process. Any transitions or ripples appearing at $V_{\text{tune}}$ during the AAC process will directly disturb $A_1$’s operating point, pushing $A_1$’s output common-mode level toward $V_{\text{DD}}$ or ground, and eventually leading to the AAC failure. The feedthrough from $V_{\text{tune}}$ to $V_{\text{out}}$ is simulated by using Fig. 2(a) and shown in Fig. 2(c). A straightforward solution to avoid this is to add a huge RC LPF before $C_V$. However, sufficient suppression of the feedthrough requires a sub-Hz corner frequency for this LPF, hence the RC LPF is not possibly integrated on a chip in conventional circuits. In this design, the unwanted feedthrough issue is suppressed by transforming the single-ended AAC to a differential AAC. Fig. 2(b) shows the proposed differential AAC. As shown, two varactors connected in opposite way are controlled by differential control voltages $V_{\text{tune,p}}$ and $V_{\text{tune,m}}$. As shown in Fig. 2(c), the differential AAC greatly suppresses the feedthrough by more than 90 dB over the entire frequency range of interest without any bulky off-chip RC filters.
Fig. 3 shows the proposed Wien-bridge oscillator employing the differential capacitive AAC. M1-M5 are diode-connected transistors acting as pseudo resistors. With five stacking of FETs, the current consumption is only 6.9 nA. It is used for generating a proper common-mode dc bias voltage for A1. M6-M9 are MOS-bipolar devices acting as pseudo-resistors. They act as diode-connected pFET when $V_{GS}$ is negative, and parasitic source-well-drain pnp bipolar transistor when $V_{GS}$ is positive. In both cases, the small-signal resistance is extremely high over several GΩ. R and C are 70 kΩ and 600 fF for 3.8 MHz oscillation. Both C1 and C2 are 500 fF. $C_V$ is the MOS capacitor with the capacitance tunable between 250 and 700 fF over the tuning voltage of 0.4–1.8 V.

The output signal $V_{out}$ is fed to the source-follower type rectifier M10-M12 and the subsequent low-pass filter $R_4$ and $C_4$. The rectifier creates a dc signal that is inversely proportional to $V_{out}$ amplitude. After the unity gain buffer A3, this dc signal is compared with a preset reference voltage $V_{ref}$, and converted to a differential signal by the single-to-differential comparator A2. On-chip $R_5$ and $C_5$ filter out residual ripples. Finally, the differential control voltage $V_{tune,p & m}$ controls the MOS varactors to achieve the optimum gain condition.

The oscillator is fabricated in 0.35 µm CMOS. A chip micrograph is shown in Fig. 4. The oscillator is measured after directly mounted and wire-bonded on a printed circuit board. It consumes 220 µA from a 2-V supply, of which the 170 µA is consumed by the Wien-Bridge core and the rest 50 µA is consumed by the AAC. Fig. 5(a) shows the frequency-domain spectrum of $V_{out}$ at 3.8 MHz. Fig. 5(b) is the time-domain waveform of $V_{out}$ with the peak-to-peak amplitude of 314 mV. Almost perfect sinusoidal waveform is observed without any noticeable distortion.
Fig. 5(c) shows the harmonic distortion levels at the output. The largest harmonic level is the $-41.1 \text{ dBc}$ second harmonic, which is considered sufficiently low. The measured phase noises at 100 kHz and 1 MHz offsets are $-94.3$ and $-110.8 \text{ dBc/Hz}$, respectively, as shown in Fig. 5(d). Measurement results show the successful operation of the proposed Wien-bridge based on the differential capacitive amplitude control loop.

3 Conclusion

A 3.8-MHz Wien-bridge oscillator that can be used as an on-chip clock generator in ULP radio is presented. The proposed Wien-bridge adopts a capacitive gain control scheme with the differential automatic amplitude control. The differential AAC greatly suppresses the unwanted feedthrough of the feedback signal at high frequency by more than 90 dB without any off-chip components. The fabricated chip demonstrates a successful sinusoidal oscillation at 3.8 MHz with satisfactory noise and distortion performances.

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