Design of DG MOSFET with Tri-Layered Strained Silicon Channel

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Abstract. The Strained Silicon material concept gained their popularity since the last two decades. Along with that the double gate semiconductor on insulator (DGSOI) MOSFET also came into being with novel material based device being the requirement, hence a strain Silicon (s-Si) material DGSOI device has been developed to be the core of this work. A concise of three layers (s-Si/s-SiGe/s-Si) is deployed in channel region with varied thicknesses, and biaxial strain is thereby inducted. This leads to increase in the mobility of charge due to the inclusion of the strain mechanism in the silicon layers. The additional gate control provides better control of the channel region. Therefore, this new device with three-layered channel resulted in 59.6% enrichment in drain current for 22nm channel length, in comparison to 45nm channel length with minimum leakage current.

1. Introduction
In nanoscale technology, the channel length of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) with silicon substrate shrinks leading to increase in charge sharing between source and drain due to less control of gate over the channel, thereby inducing short channel effects (SCEs) [1]. The device characteristics leading to device performance alter incorporating effects such as drain induced barrier lowering (DIBL), surface scattering, impact ionization, hot carrier injection (HCI) [1]. So, the double gate metal oxide semiconductor (DGMOS) transistors on buried oxide (BOX) developed as an alternative to reduce the SCEs and leakages. With the induction of strained silicon channel along with DGMOS change in the properties of silicon wafer by slightly stretching the placements of atoms have also been observed [2-7]. Having an induced strain in the channel of the device structure an advantage of consenting electrons and holes to move faster within the nano-channel region is admitted as have been carefully observed in the literature [1-4, 6-8].

Khiangte et al. [6, 9-11] developed a tri-layered s-Si/s-SiGe/s-Si channel based planar MOSFET, where strain channel engineering was inducted to modify the band structure, increasing the carrier mobility and lowering the resistance in the channel leading to enhanced device performance. The strain is persuaded perpendicular to the depletion region surface giving rise to splitting of energy bands into two fold and four fold valleys. The electron mobility is increased due to lower conductive mass of four fold valleys and less inter-valley scattering, thereby enriching the device performance [3, 6]. The Silicon on Insulator (SOI) technology is therefore, preferred over bulk silicon, due to
numerous advantages such as reduction of parasitic resistance and junction capacitance resulting in an increased circuit speed and dielectric isolation between devices in the CMOS [4, 5]. In this work considering the above aspect of channel engineering leading to development of enriched device the tri-layered (s-Si/s-SiGe/s-Si) channel based system is introduced for the first time with Double Gate (DG) structure leading to formation of DG SOI MOSFET for a 22nm channel length device.

2. Device structure and simulation
The double gate metal oxide semiconductor (DGMOS) structure developed comprises of the channel region with front and back gate with the tri-layer (s-Si/s-SiGe/s-Si) channel region as shown in figure 1(a) and zoomed in view of the channel in figure 1(b). The DGMOS with tri-layered channel is developed on buried oxide with two gates on front and back side of channel employing Sentaurus TCAD Tool [12] employing the parameters tabulated in Table 1. The front and back gates are equally biased on applying equal surface potential developed across the two oxide interfaces. The both gates have same work function, which control the electrostatic coupling off the device. So current flow through channel is suitably modulated by the applied electric field [13].

| Parameters                          | Dimensions |
|-------------------------------------|------------|
| Channel length                      | 22nm       |
| Ge mole fraction                    | 0.2        |
| s-Si layer thickness                | 2nm        |
| s-SiGe layer thickness              | 6nm        |
| Gate Oxide thickness                | 2nm        |
| Source/Drain doping (N_D)           | $10^{18}$ cm$^{-3}$ |
| Channel doping (N_A)                | $10^{16}$ cm$^{-3}$ |
| Drain bias                          | 50mv       |

Figure 1.(a) A schematic structure of double gate MOSFET with tri-layered channel on 22nm channel length (b) cross sectional view of double gate MOSFET with tri-layered channel
The mobility of electrons increases by combination of lower effective mass and reduced intervalley scattering. The Drift- Diffusion and Piezoresistive models [14-16] are used to solve Poisson and Carrier continuity equation in designated dielectric interfaces and the tri-layered (s-Si/s-SiGe/s-Si) interface with specified boundary condition is thereby introduced. The Drift-Diffusion simulation shows density distribution of electrons and holes in particular channel region, while the Piezoresistive model introduced analyzes the strain effect with the strained silicon material.

3. Results and Discussion

The 2D Sentaurus device simulator [17] is employed to simulate the DGMOS with tri-layered channel on 22nm channel length. The DGMOS with tri-layer channel is developed for the first time on 22nm channel length and analyzed for drain current enhancement. The narrow channel structure is formed on BOX comprising of the tri-layers (s-Si/s-SiGe/s-Si) with thickness of 2nm-6nm-2nm respectively. Due to quantum confinement of charge carriers and strain insertion in channel region as detected by Khangte et al. [6, 9-12] on sub-40nm channel length MOSFETs, increase in the mobility of charge carries is similarly observed here for the DGMOS structure. The 1D Schrodinger equations are solved by creating non-local mesh in tri-layered (s-Si/s-SiGe/s-Si) and oxide interfaces. The current voltage characteristics ($I_D-V_{GS}$) of DGMOS with tri-layered channel (s-Si/s-SiGe/s-Si) at 50mV drain bias voltage are compared with double gate Nano-FET on 45nm channel length as shown in figure 2. With the mobility of charge carries increasing the inversion layer and electric field penetration from source/drain to the substrate is controlled with two gates, thereby enhances drain current across the channel of the vertical device.

![Graph showing drain current ($I_D$) vs gate voltage ($V_{GS}$) for 22nm Tri-Layered Channel DGMOS and 45nm Double Gate Nano-FET.](image)

**Figure 2.** $I_D-V_{GS}$ transfer characteristics of double gate MOSFET with tri-layered channel on 22nm and double gate Nano-FET on 45nm channel length.

From figure 2, it has been observed that in off state of short channel device the subthreshold current flows between drain and source, because the threshold voltage decreases by shrinking the channel length. The threshold voltage in DGMOS with tri-layered channel is acquired to be 0.216V. Also slight increase in leakage current up to 2nA (acceptable amount as per the ITRS 2014 [18]), is observed in 22nm technology node as compared to the 45nm device.
On introducing this channel engineering along with strain in double gate enhanced the drive current with a minor increase in subthreshold leakage. Figure 3 shows the comparison of \((I_D-V_{DS})\) performance output.

![Graph](image1.png)

**Figure 3.** \(I_D-V_{DS}\) output characteristics of double gate MOSFET with tri-layered channel on 22nm and double gate Nano-FET on 45nm channel length.

Characteristics of double gate MOSFET with the novel tri-layered channel for 22nm to the double gate Nano-FET for 45nm channel length. The leakage current \((I_{off})\) and drain current \((I_{on})\) of 45nm and 22nm channel length are compared and presented in figure 4.

![Graph](image2.png)

**Figure 4.** \(I_{on}\) and \(I_{off}\) of double gate MOSFET with tri-layered channel on 22nm and double gate Nano-FET on 45nm channel length
From figure 4 it is perceived that the leakage current in 22nm channel length is higher to that of 45nm channel length device, which is within the range as per ITRS roadmap [18] but while from figure 3. the performance based drive current inculcated an increase of 59.6%. Thus, this tri-layered channel DGMOS showed enrichment in drain current on 22nm technology.

4. Conclusion
The novel double gate MOSFET with tri-layered channel is developed on 22nm channel length employing Sentaurus TCAD simulation tool in 3D structural format. The device characteristics are compared with the 45nm channel length double gate Nano-FET. The device performance is observed to have enriched as the drive current improvement is around 59.6% with acceptable leakage current of ~2nA. This double gate MOSFET thereby developed with the tri-layered 22nm channel length has the capability to meet the requirement of low power and faster operating device, which is the need of this era.

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