DetectX- Adversarial Input Detection using Current Signatures in Memristive XBar Arrays

Abhishek Moitra
Electrical Engineering department
Yale University
New Haven, CT, USA
Email: abhishek.moitra@yale.edu

Priyadarshini Panda
Electrical Engineering department
Yale University
New Haven, CT, USA
Email: priya.panda@yale.edu

Abstract—Adversarial input detection has emerged as a prominent technique to harden Deep Neural Networks (DNNs) against adversarial attacks. Most prior works use neural network-based detectors or complex statistical analysis for adversarial detection. These approaches are computationally intensive and vulnerable to adversarial attacks. To this end, we propose DetectX-a hardware friendly adversarial detection mechanism using hardware signatures like Sum of column Currents (SoI) in memristive crossbars (XBar). We show that adversarial inputs have higher SoI compared to clean inputs. However, the difference is too small for reliable adversarial detection. Hence, we propose a dual-phase training methodology: Phase 1 training is geared towards increasing the separation between clean and adversarial SoIs; Phase 2 training improves the overall robustness against different strengths of adversarial attacks. For hardware-based adversarial detection, we implement the DetectX module using 32nm CMOS circuits and integrate it with a Neurosim-like analog crossbar architecture. We perform hardware evaluation of the Neurosim+DetectX system on the Neurosim platform using datasets-CIFAR10(VGG8), CIFAR100(VGG16) and Tiny-Imagenet(ResNet18). Our experiments show that DetectX is 10x-25x more energy efficient and immune to dynamic adversarial attacks compared to previous state-of-the-art works. Moreover, we achieve high detection performance (ROC-AUC > 0.95) for strong white-box and black-box attacks. The code has been released at https://github.com/Intelligent-Computing-Lab-Yale/DetectX

Index Terms—Adversarial Attacks, Adversarial Input Detection, Analog Crossbar Arrays, Neurosim

I. INTRODUCTION

Deep Neural Networks (DNNs) have been shown to be proficient in carrying out tasks like autonomous driving, image segmentation and real-time object detection. However, they have been shown to be vulnerable to adversarial attacks. Here, extremely small noise is added to an image to fool the DNN [1], [2]. This prevents DNNs from being autonomously deployed in critical applications like medical diagnostics, aviation and defense [3], [4].

To harden DNNs against adversarial attacks, there are two different approaches that have been explored. The first approach focuses on improving the classification accuracy of the DNN on adversarial inputs (adversarial accuracy) [5], [6], [7]. This is achieved through techniques like adversarial training. In adversarial training, the DNN is trained on both clean and adversarial data till the DNN loss is minimized [6]. Other works have used image compression [8], input randomization [9], [10] and parameter noise injection [11] to improve the adversarial accuracy of the DNN. The second approach is adversarial input detection. Here, the goal is to detect and reject adversarial inputs from propagating deeper into the network [12].

Most prior works on adversarial input detection augment neural network based detectors at intermediate layers [13], [14], [12]. Others use complex mathematical analysis to detect adversarial and clean activations [15]. These methods are 1) difficult to realise on hardware, and 2) vulnerable to adversarial attacks. For example, neural network-based detectors have been shown to be vulnerable to dynamic adversarial attacks [13]. Here, the objective functions of both the neural network-based detector and the main DNN are used to generate much stronger attacks [13], [12]. To bypass these problems, we use a hardware driven approach. We monitor hardware signatures in DNN accelerators like currents in processing units to differentiate between adversarial and clean inputs. Several works on both digital von-neumann and analog crossbar based DNN accelerators have been proposed so far [16], [17], [18], [19], [20], [21]. In this work, we focus on intercepting hardware signatures in analog crossbar based DNN accelerators.

As seen in Fig. 1a, in analog crossbars [16], [17], multiplication between input voltages $v_i$ and conductances $G_{ij}$ are realised using Ohm’s law. The conductances are stored in Non Volatile Memory (NVM) devices like Resistive Random Access Memories (RRAMs) [22], [23], Ferroelectric Field Effect Transistors (FeFETs) [24], [25] among others. The accumulation is realised using summation of individual currents using Kirchoff’s Current Law (KCL). This results in column currents $I_j$. Thus, $I_j$’s are the result of a full Multiply Accumulate (MAC) operation. Equivalently, in software, MAC operations between inputs $x_i - x_e$ and the weights $W_{ij}$ result in weighted summation values $Z_j$. The activation value $A_j$ for each output neuron is obtained by applying an activation function $f$ on $Z_j$. This has been shown in Fig. 1b.

In this work, we use the Sum of Currents (SoIs) parameter in analog crossbar arrays to detect adversarial inputs. For a particular layer $l$, SoI is the sum of the magnitudes of all the column currents in the crossbar as shown in Fig. 1c. As an example, consider the crossbar shown in Fig. 1a having column currents, $I_1 - I_m$. Here, the SoI value can be
Fig. 1: a) MAC operations in analog crossbar arrays are realised using Ohm’s law and Kirchoff’s Current Law resulting in output currents $I_j$. The current $I_j$ is the result of a weighted summation operation between conductances $G_{ij}$ and inputs $v_i$. b) In software, the MAC outputs $Z_j$ is realised using weighted summation operations between the weights $W_{ij}$ and inputs $x_i$. $A_j$ is the output of the activation function applied to $Z_j$. c) The SoI in analog crossbars can be computed by summing up the magnitudes of all the column currents ($I_1$ to $I_m$). This is proportional to performing absolute value summation of all the weighted summation outputs $Z_j$. d) The DetectX module is integrated with a Neurosim-like analog crossbar architecture. The column currents are multiplexed using an analog multiplexer which are then converted to digital values using the Analog to Digital Converter (ADC). For crossbars in the first layer, the output of ADC is fed into the DetectX module and the Activation circuits. However, for other layers, the DetectX module is absent.

Motivation: Using SoI, we propose a detection mechanism that is hardware friendly and energy efficient. Absence of a neural network-based detector increases the robustness against dynamic adversarial attacks. As seen in Fig. 2a, the first layer adversarial SoIs are higher than clean SoIs. This is due to the added input perturbations. Note, the x-axis in Fig. 2a depicts the range of SoI values and the term frequency refers to the number of occurrences of each SoI values. The adversarial SoIs are the SoIs corresponding to strong Projected Gradient Descent (PGD) and Fast Gradient Sign Method (FGSM) attacks. Likewise, clean SoIs are the SoIs corresponding to clean inputs. Clearly, in Fig. 2a, the clean and adversarial SoI distributions are not well separated for reliable detection.

To this end, we propose a dual-phase training methodology as follows: In the first phase, we train the DNN to increase the separation between first layer clean and adversarial SoIs. This is shown in Fig. 2b. When we deploy the dual-phase trained DNN on hardware, we see a similar separation between clean and adversarial SoIs as Fig. 2b. This is shown in Fig. 2c. This shows that the SoI separation in software leads to SoI separation in hardware. In the second phase, we freeze the first layer synaptic weights and explicitly perform adversarial training. This improves the accuracy of the DNN on clean inputs (clean accuracy). Additionally, it further improves the robustness of the DNN. After the dual-phase training, a Look Up Table (LUT) is created with entries as follows: The first column contains a list of sample SoI values. The second column consists of the probabilities associated with each SoI value. A high probability denotes that the SoI corresponds to a clean input.

The dual-phase trained DNN is implemented on a Neurosim-like analog crossbar architecture [26]. For adversarial input detection, we integrate the analog crossbar with the DetectX module as shown in Fig. 1d. The DetectX module is implemented using a 32nm CMOS Predictive Technology Model (PTM) [27]. It contains a SoI Computing Unit and a LUT-based detector. During detection, the SoI value computed by the SoI Computing Unit is looked up in the LUT and a confidence score denoting the probability of clean input is generated. If the confidence score is low, the input is treated as adversarial and rejected. For hardware evaluation of the analog crossbar+DetectX system, we use Neurosim platform. Additionally, we perform robustness evaluation using different datasets like CIFAR10, CIFAR100 [28] and TinyImagenet [29].

To the best of our knowledge, this is the first work that exploits hardware based signatures for adversarial input detection in analog crossbar arrays. In summary, the key contributions of our work are as follows:.

1) We propose DetectX, a digital CMOS-based adversarial input detector. DetectX is a small digital module that uses SoI values in analog crossbar architectures to detect adversarial attacks. For this, it is appended at the end of an analog crossbar array. Note, although DetectX is a digital module, the crossbar+DetectX system is a mixed...
Fig. 2: Results of dual-phase training with CIFAR10 dataset on VGG8 network. a) The First layer SoI distribution corresponding to clean and adversarial inputs before the proposed dual-phase training methodology. The adversarial attacks correspond to PGD \( \epsilon=16/255, \alpha=2/255, n=10 \) and FGSM \( \epsilon=16/255 \) attacks b) Separated layer 1 clean and adversarial SoI distributions obtained after the dual-phase training. c) After implementing the dual-phase trained DNN on an ideal Neurosim-like crossbar architecture, we observe similar separation between clean and adversarial SoIs. In all the figures, the x-axis represents the range of SoI values and the y-axis represents the number of occurrences of each SoI value (Frequency).

2) To improve the SoI based detection performance, we propose a dual-phase training algorithm. The first phase is geared towards increasing the SoI separation between clean and adversarial inputs. While the second phase improves the adversarial robustness of the DNN on adversarial inputs that are not rejected by the detector.

3) We validate our methodology through experiments performed on the Neurosim platform. We use different datasets like CIFAR10, CIFAR100, and TinyImagenet. Additionally, we conduct a comprehensive analysis to compare the energy-robustness tradeoffs between DetectX and other state-of-the-art adversarial input detection works. DetectX outperforms these works in energy efficiency with comparable robustness against different adversarial attacks. Additionally, we also show that DetectX can improve the robustness of models against Black-Box and Dynamic Adversarial Attacks.

II. BACKGROUND

A. Analog Crossbar Arrays

Analog crossbar arrays have recently emerged as an energy efficient method for implementing MAC operations. In an analog crossbar, multiplications between inputs and synaptic weights are realised using Ohm’s law. As shown in Fig. 1a, the DNN weights are stored as conductance states \( G_{ij} \) of NVM devices (RRAMs,FeFETs) [24], [22]. The largest synaptic weight is mapped to the highest conductance state and vice-versa. Likewise, the inputs are encoded as voltage values \( v_i \). When a voltage is applied across an NVM device, a current proportional to \( G_{ij} \) and \( v_i \) is generated at a cross-point. The final MAC output is obtained by adding the individual device currents along a column by the virtue of KCL.

1) The Neurosim Platform: Neurosim [17] is a Python based platform that performs a holistic energy-latency-accuracy evaluation of analog crossbar-based DNN accelerators. The Neurosim platform supports both SRAM and memristive-based (RRAM and FeFET) computing devices.

Neurosim-like analog crossbar architecture: In this work, we use a Neurosim-like analog crossbar architecture as shown in Fig. 1d for all hardware evaluations. In the Neurosim-like analog crossbar, multiple columns are multiplexed using an analog multiplexer. The multiplexer serializes parallel input currents for the analog to digital conversion stage. This essentially reduces the number of Analog to Digital Converters (ADC) required at the cost of increased computation time (latency). The ADC converts analog currents to digital values using current-to-voltage sense amplifiers [30]. After the ADC stage, the activation unit applies an activation function like ReLU [31] or sigmoid [32] to the digital MAC outputs. Note, digital implementation of mathematical functions are more stable and hardware efficient than analog implementations.

For implementing DNNs on the Neurosim platform, first several hardware parameters are initialized. These include the crossbar size, on-off ratio of the memristive device, the conductance variation parameter and so on. The DNN is first mapped onto several analog crossbars using Neurosim’s novel, energy-efficient mapping strategy. The mapping strategy reduces the number of memory accesses during the MAC operations. After the DNN mapping stage, the Neurosim platform performs feed-forward operations on the inputs to the DNN. During this, MAC operations between the inputs and the DNN weights are performed in the crossbars resulting in output currents. The output currents are then converted to digital values by the ADC. During the MAC operations, Neurosim incorporates hardware non-idealities like conductance variation effects in memristive devices and data-quantization loss. This facilitates a realistic hardware evaluation of DNNs. Additionally, the Neurosim platform also computes the energy and latency of different hardware components used during the feed-forward operation. These include the analog crossbars and the peripheral circuits like the MUX, ADC, activation units among others.

Although, the Neurosim platform incorporates various hardware-based non-ideal effects like quantization noise and memristive conductance variations, it does not incorporate
the non-idealities arising due to process-voltage-temperature variations (PVT), device to device variations and so on.

In this work, for hardware based adversarial input detection, we append the DetectX module after the ADC stage of the first layer crossbar. The DetectX module uses the SoI parameter for adversarial input detection. It consists of a SoI computing unit for SoI value computation and a LUT-based detector that generates the detector output.

B. Adversarial attacks

In this paper we discuss two kinds of adversarial attacks: White-Box (WB) attacks and Black-Box (BB) attacks. In WB attacks, the attacker has complete access to the DNN network and parameters. This is a more difficult and stronger adversarial attack. BB attacks are easier to execute as they do not require complete access to the target DNN. The adversarial inputs can be generated using a different DNN model. In this work, we discuss two gradient based adversarial attacks.

1) Fast Gradient Sign Method (FGSM) [33] is a one step gradient based attack shown in Equation 1. First, the gradients of the DNN loss \( L(\theta, x, y_{true}) \) with respect to the input \( x \) are calculated. Then, a \( \text{sign}(\cdot) \) operation converts the gradients into unit directional vectors. The unit vector is multiplied by a scalar perturbation value, \( \epsilon \). Finally, the perturbation vector is added to the input \( x \) to create an adversarial data. Note, that perturbations are added to \( x \) along the direction of the gradients to maximize DNN loss \( L \).

\[
x_{adv} = x + \epsilon \ \text{sign}(\nabla_x L(\theta, x, y_{true})) \tag{1}
\]

2) Projected Gradient Descent (PGD) attacks have been shown to cause highly effective adversarial attacks [6]. The PGD attack, shown in Equation 2 is an iterative attack over \( n \) steps. In each step \( i \), perturbations of strength \( \alpha \) are added to \( x_{adv}^{i-1} \). Note, that \( x_{adv}^{0} \) is created by adding random noise to the clean input \( x \). Additionally, for each step, \( x_{adv}^{i} \) is projected on a Norm ball [6], of radius \( \epsilon \). The type of Norm ball \( (L_{\infty}, L_2 \) and so on) used signifies how the net perturbations with respect to the input is computed. In this work, we use the \( L_{\infty} \) Norm ball (of radius \( \epsilon \)) projection for all the PGD attacks. In other words, we ensure that the maximum pixel difference between the clean and adversarial inputs is \( \epsilon \).

\[
x_{adv} = \sum_{i=1}^{n} x_{adv}^{i-1} + \alpha \ \text{sign}(\nabla_x L(\theta, x, y_{true})) \tag{2}
\]

Strength of an Adversarial Attack: The strength of an adversarial attack is directly proportional to the amount of perturbations added to the input. To create strong adversarial attacks, high values of \( \epsilon \) (in case of FGSM attacks) and \( \alpha, \epsilon, n \) (for PGD attacks) are chosen. Similarly, weak adversarial attacks are created by choosing extremely small values of \( \alpha, \epsilon, n \). For moderate strength attacks, the values of \( \alpha, \epsilon, n \) lie in between the weak and strong adversarial attacks.

C. Performance Metrics for Adversarial Input Detection

To evaluate the adversarial detection performance, we use three performance metrics: ROC-AUC, Accuracy and Error.

- **Area Under the ROC Curve (ROC-AUC):** In this work, we use ROC-AUC score to analyse the performance of DetectX. The ROC-AUC for a detector is high if the detector has a high confidence score for positive classes and low confidence score for the negative classes. Previous works have shown that using ROC-AUC is more stable than True Positive Rate (TPR) and False Positive Rate (FPR) based performance analysis [14].

- **Accuracy and Error:** In the context of adversarial input detection, **Accuracy** and **Error** are not complements of each other. **Accuracy** refers to the fraction of clean inputs that are correctly classified and not rejected by the adversarial input detector. While, **Error** refers to the fraction of adversarial inputs that are classified incorrectly and not rejected by the adversary detector.

III. RELATED WORKS

A. Works improving adversarial robustness of DNNs

1) Algorithmic approaches: Among various algorithmic works that try to improve the adversarial accuracy of the DNN, adversarial training has been shown to achieve state-of-the-art performance [6]. Adversarial training aims to solve the min-max problem. This is done by first creating a suitable adversarial dataset such that the DNN loss is maximized. Next, the DNN is trained on the adversarial dataset until the loss value converges to a minimum. Additionally, adversarial training has been shown to posses higher transferability across different types of attacks. Further, He et al. [11] showed that adding noise into DNN parameters during adversarial training can improve the adversarial robustness of the DNN. Other works by Xie et al. [10] and Dziugaite et al. [8] show that input level randomization and compression, respectively, can improve the adversarial robustness of the DNN. However, these works do not use an adversarial training approach. The review work by [34] provides a comprehensive list of different algorithm level DNN robustness improvement methodologies.

2) Hardware approaches: Recently hardware centred approaches have been looked at from the perspective of improving the adversarial robustness of DNNs. The work by Panda et al., QUANOS [35], leverages data quantization in order to minimize the adversarial noise sensitivity parameter. The work by Lin et al., Defensive Quantization, [36] used quantization in order to minimize the adversarial noise magnification effect in the deeper layers. This is done by optimizing the DNN to have a lipschitz constant less than 1. Additionally, works like [37], [38] show that intrinsic bit-error noise in 6T SRAM cells in hybrid CMOS memories and non-idealities in analog crossbar arrays can improve the adversarial robustness of DNNs.

B. Works based on adversarial input detection

Towards adversarial input detection, most works so far have focused on algorithmic approaches. wherein the DNN is either
trained on augmented data or the network architecture of the DNN is modified in order to facilitate adversarial input detection. The work by Grosse et al. augmented the dataset with an additional class representing adversarial inputs. The adversarial inputs were classified at the end of the DNN [39], [40]. In contrast to this, Feinman et al. used a linear classifier at the end of the last hidden layer to classify the points lying away from the data manifolds as adversarial inputs [41]. The work by Yin et al. proposed training a binary classifier on subspaces created by partitioning the input space [14]. This resulted in multiple detectors that were used for adversarial input detection. Additionally, the work Li and Li proposes to detect adversarial features by training cascades of SVM classifiers on the Principal Component Analysis (PCA) of the outputs of the convolution layers of the main network [42].

Additionally, Metzen et al. and Sterneck et al. appended a binary classifier between convolutional layers to detect adversarial inputs using the intermediate activation maps as features [13], [12]. While Metzen et al. used a heuristic approach to append adversarial input detectors at the end of intermediate convolutional layers, Sterneck et al. strategically placed the detector at the end of a convolution layer chosen using a metric called the adversarial noise sensitivity. This improved the energy and resource efficiency of the detection. However, both the works showed that their detector performances are affected by dynamic adversarial attacks.

In this work, we take a hardware-based approach towards adversarial input detection. Using DetectX, we show that the parameter SoI can be used to perform energy efficient adversarial input detection in analog crossbar based DNN accelerators. Apart from energy efficiency, DetectX also improves the overall adversarial robustness of the DNN against black-box, white-box and dynamic adversarial attacks when compared to previous works.

IV. DUAL-PHASE TRAINING METHODOLOGY

The dual-phase training methodology is divided into two phases. The first phase is geared towards increasing the SoI separation between clean and adversarial SoIs. In the second phase, we perform adversarial training to further improve the adversarial robustness of the DNN.

A. Phase 1 Training

In the first phase training, a pre-trained model (DNN trained on clean data in the standard manner) is trained on dataset consisting of [clean+strong adversarial data]. For this we use the objective function shown in Equation 3. The adversarial data is generated using PGD attacks on the pre-trained DNN. The values $\lambda_c$ and $\lambda_a$ represent the desired clean and adversarial SoI values. The mean square loss ($L_{MSE}$) represents the Euclidean distances between the actual SoI values and the desired SoI values. During training, for adversarial inputs, $y$ activates the term $L_{MSE}(SoI_a, \lambda_a)$ while deactivating the term $L_{MSE}(SoI_c, \lambda_c)$ simultaneously and vice versa. We take $y=1$ when the input is adversarial and $y=0$ when the input is clean. For better convergence of Equation 3, the cross-entropy loss term $L_{CE}$ is scaled by a small factor $\beta$ (of the order of $10^{-6}$.

$$L = \beta L_{CE} + y L_{MSE}(SoI_a, \lambda_a) + (1-y) L_{MSE}(SoI_c, \lambda_c)$$  \hspace{1cm} (3)

Fig. 3 demonstrates the working of Phase1 training. Before phase 1 training, the mean SoI values for clean and adversarial inputs (black dotted line) are well separated. Additionally, they are shifted closer to the desired SoI values ($\lambda_c$ and $\lambda_a$). This shift is shown using the horizontal arrows. The black dotted line represents the SoI of clean and adversarial inputs before the Phase 1 training. The SoIs correspond to the CIFAR10 dataset on a VGG8 network.

Algorithm 1: Proposed Dual-Phase Training Methodology

Training Phase 1

Inputs: Pre-trained DNN model; Training dataset: 1:1 ratio of clean and adversarial data;
for $epochs \leq num\_epochs$ do
  Calculate first layer SoI;
  Forward pass;
  Compute loss using Equation 3;
  Backward pass;
end

Training Phase 2

Inputs: DNN after Training Phase 1; Training dataset: 1:1 ratio of clean and weak adversarial data;
for $epochs \leq num\_epochs$ do
  Forward pass;
  Compute loss using Equation 4;
  Backward pass;
end
the performance of the detection performance of DetectX is slightly lowered for extremely weak adversarial attacks (i.e., adversarial attacks having small input perturbations). Thus, in order to improve the clean accuracy and further improve the robustness of the DNN, we perform Phase2 training.

### B. Phase2 Training

In the second phase, we explicitly perform adversarial training on the DNN using the objective function shown in Equation 4. The adversarial training set comprises of [clean + weak adversarial data]. During adversarial training, we freeze the first layer weights in order to maintain the separation between clean and adversarial SoIs.

\[ \mathcal{L} = \mathcal{L}_{CE} \]  

(4)

### C. Creating the SoI-Probability LUT

The SoI-Probability LUT has the following structure: The first column stores the sample SoI values while the second column stores the corresponding clean probabilities \( P(\text{Clean}) \) for each SoI value. Fig. 4 shows the plot of the \( P(\text{Clean}) \) and \( P(\text{Adversarial}) \) values against the sample SoI values. The value of \( P(\text{Clean}) \) denotes the probability that a given SoI value belongs to a clean input. It is calculated using Equation 5. Here, \( n_c \) and \( n_a \) denote the frequencies of adversarial and clean SoIs, respectively, at a particular SoI value. Note, \( P(\text{Adversarial}) \) (shown in orange), is not stored in the LUT. For creating the SoI-Probability LUT, we select a random sample of clean images. To create the adversarial dataset, we add adversarial perturbations to the randomly selected clean images. Then, the SoI values are computed for both the clean and adversarial images. In this work, we refer to \( D_c \) as the SoI distribution corresponding to clean images and \( D_a \) as the SoI distribution corresponding to adversarial images. The choice of the adversarial distribution \( D_a \) is critical to the detector performance and will be discussed in the later sections.

\[ P(\text{Clean}) = \frac{n_c}{n_c + n_a} \]  

(5)

### D. Why the Dual-Phase Training Works?

From Fig. 1c, SoIs can be expressed as the absolute value of all the weighted summation outputs in a particular layer of the DNN. Moreover, in the first layer, the convolution operation is merely a linear operation on the inputs. In other words, any change in the input will affect the output linearly. We use these properties to understand why the dual-phase training works.

From Fig. 1b and Fig. 1c, SoI for clean input data, \( X_{\text{clean}} \), can be written as shown in Equation 6. For creating adversarial inputs \( X_{\text{adv}} \), perturbations \( \mathcal{P} \) are added to \( X_{\text{clean}} \) as seen in Equation 7. These added perturbations lead to a significant change in the adversarial SoI value as seen in Equation 8.

\[ \text{SoI}_{\text{clean}} = \sum_{j=1}^{m} \sum_{i=1}^{r} |W_{ij}X_{\text{clean},i}| \]  

(6)

\[ X_{\text{adv}} = X_{\text{clean}} + \mathcal{P} \]  

(7)

### E. Evaluating SoI separation

In this section, we will evaluate the Phase1 training performance based on different strengths of adversarial data. For this, a DNN is trained using the CIFAR10 dataset comprising of [clean+weak/ moderate/ strong adversarial data]. Fig. 5a shows the ROC-AUC scores corresponding to weak (Train-W), moderate (Train-M) and strong (Train-S) attacks under three different scenarios. In Train-W, the DNN is trained with weak adversarial data. Here, the ROC-AUC scores across all strengths of adversarial attacks are low (small separation between clean and adversarial SoIs). Although, with moderate strength adversarial attacks, the performance is better than the previous case, it is not able to achieve a higher SoI separation for strong attacks. Finally, in the case of Train-S, training with strong adversarial data achieves the highest SoI separation across different attack strengths. This is signified by an overall high ROC-AUC score across all attack strengths.

### F. Choosing adversarial distribution \( D_a \) for SoI-Probability LUT creation

In this section, we analyse the performance of DetectX based on three different adversarial SoI-Probability LUTs. For each LUT, the clean SoI distribution \( D_c \) is fixed while adversarial SoIs \( D_a \) can be different depending on the type of adversarial attack used.

We use a dual-phase trained DNN (trained on the CIFAR10 dataset [Clean+Strong PGD data]). This leads to maximum SoI separation as discussed in Section IV-E. Then, we create three different SoI-Probability LUTs with \( D_a = \text{weak} (\text{Detector-W}) \), \( D_a = \text{moderate} (\text{Detector-M}) \) and \( D_a = \text{strong} (\text{Detector-S}) \) adversarial SoI distributions. Fig. 5b shows the ROC-AUC scores...
corresponding to different strengths of adversarial attacks for the three different SoI-Probability LUTs. While Detector-W performs poorly across all strengths of attacks, Detector-S performs well with strong attacks only. Here, Detector-M has a high performance across all strengths of adversarial attacks. Thus, SoI-Probability LUT created using $D_a$ corresponding to moderate strength attacks are unbiased and will be used in all further experiments in this paper.

V. HARDWARE IMPLEMENTATION

In this section, we first define the hardware architecture of the DetectX module. Then we integrate it with an analog crossbar to perform hardware-based adversarial input detection.

A. DetectX

As shown in Fig. 6, DetectX consists of two sub-modules: 1) The SoI Computing Unit, and 2) The LUT-based detector. To show how the DetectX module is integrated with an analog crossbar, we show an 8x8 crossbar having four 2:1 multiplexers. The outputs of the four multiplexers are fed as inputs to four ADCs A1-A4. The outputs of the A1-A4 are the inputs to the L1 Adders. The L1 Adders can support both addition and subtraction operations. If the most significant bit of the input is 1, then a subtraction operation is performed and addition otherwise. With this, we implement the absolute value summation operation for computing SoIs. To implement an accumulation operation, we use registers Reg. Each Reg stores the intermediate summation outputs. At the end of all the read cycles, the final summation value is forwarded to the L2 Adders. As an example, in Fig. 6, due to the presence of four 2:1 MUXs, a total of 2 read cycles are required to read all the outputs from the crossbar. In each cycle, the analog current outputs are converted to digital values. These digital inputs are then added/subtracted to the previous accumulated values stored in the registers using the L1 Adders. After completion of all the read cycles, the accumulated values in each Reg are added using L2 adders in the adder-tree. This gives the final SoI value. The size of the SoI Computing Unit depends on the crossbar parameters (see Section V-C).

Next, the computed SoI value is passed to the LUT-based detector. Here, the SoI value is looked up (LookUp Stage) in the LUT memory [16]. The LUT stores the sample SoI values ($S_0$ to $S_n$) and the corresponding $P$(Clean) values $P_0$ to $P_n$. It is composed of 6T-SRAM cells. In the LookUp Stage, a binary search operation is performed. Depending on the value of the input SoI, the $P_k$ corresponding to $S_k$ (such that $S_k < \text{SoI} < S_{k+1}$) is chosen and passed to the Confidence Generator. The Confidence Generator generates a random sample using a SRAM-based Random Number Generator(RNG) [43]. The RNG exploits the principle of bit-instability of SRAM cells during the turn-on phase. The RNG output is then compared with the input probability value $P_k$. If the RNG output is lesser than $P_k$, then the Detector Output is 1. This means that the SoI belongs to a clean input and vice-versa.

B. Energy Analysis of the DetectX module

The DetectX module is implemented using 32nm CMOS PTM [27]. For energy overhead estimation, we consider the energy consumed by the most significant components only. The energy of all the components of DetectX are evaluated using the Cadence Virtuoso platform. These include the $L1+L2$ Adders, Registers, LUT and the RNG as shown in Fig. 7a. Here, Energy/Op is the energy consumed for a unit operation. For example, the 8-bit Adder requires 19.2fJ of energy for one 8-bit addition/subtraction. Similarly, Energy/SoI denotes the amount of energy consumed for each input SoI value by the DetectX module. Note, that the Energy/SoI value of each component (except the RNG) depends on parameters $N_{L1}, N_{L2}, N_R, N_X$ and $N_C$. They denote the number of $L1$ Adders, $L2$ Adders, Registers, read cycles and LUT accesses, respectively. The values $N_{L1}, N_{L2}, N_R$ and $N_C$ will be derived in Section V-C. Additionally, for each SoI,
Fig. 6: The DetectX module receives MAC outputs from the ADC stage (A1-A4) of the crossbar (last two rows of an 8x8 crossbar shown for example). The L1 Adders can support addition/subtraction depending on the most significant bit (MSB) value. This facilitates absolute value summation of the MAC values. Using registers Reg allows addition of MAC values from cycle to cycle. After all the cycles are completed, the L2 Adders compute the final SoI values which are passed to the LUT-based Detector. Here, a Binary Search is performed on the LUT and a sample SoI value $S_k$ and its corresponding $P_{(clean)}$ value is selected depending on the SoI value. The $P_k$ is then compared with a random sample generated by the RNG in the Confidence Generator. If the sample is less than $P_k$, the detector output is 1, meaning that the input is clean and vice-versa.

Fig. 7: a) Table showing the Energy/Operation of all the major components in the DetectX module. The Energy/SoI represents the energy required to compute and process a single SoI value. The Energy/SoI value for individual components depend on parameters like $N_{L1}$, $N_{L2}$, $N_R$, $N_C$ and $N_X$. $N_{L1}$, $N_{L2}$, $N_R$, $N_C$ depend on the analog crossbar array parameters shown in Fig. 9a. b) $N_X$ depends on the input SoI value due to the Binary Search Operation. The distribution corresponds to the number of LUT accesses for a dataset having equal amounts of clean and adversarial inputs.

RNG is accessed once. Hence, its Energy/SoI is equal to the Energy/Op.

The energies consumed by the L1+L2 Adders, Registers and the RNG are independent of the input SoI values. However, $N_X$ depends on the SoI value because of the Binary Search operation. Consequently, $E_{LUT}$ depends on the SoI value. To analyse the SoI dependent behaviour of $N_X$, we create a dataset of 10k samples having equal number of clean and adversarial inputs. The inputs are fed into the dual-phase trained Neurosim+DetectX model. Corresponding to each input, the SoI values are looked up in the LUT and the number of memory accesses are recorded. The distribution of $N_X$ has been shown in the Fig. 7b.

C. Hardware Evaluation of the crossbar+DetectX System

In this section, we perform hardware evaluations to analyse the performance of the analog crossbar+DetectX system. The hardware evaluation is performed on the Neurosim platform [26]. Neurosim efficiently maps large-scale DNN architectures (like VGG8, VGG16 [44]) on analog crossbar arrays. Additionally, the platform also considers device conductance variations and non-idealities. This motivates a more realistic hardware evaluation of DNNs.

Fig. 8 depicts the hardware implementation and evaluation steps used in this section. First, a dual-phase trained VGG8 network (on CIFAR10 dataset) is mapped on a Neurosim-like analog crossbar architecture. The VGG8 network is trained with 8-bit data precision for weights and activations. Fig. 8a shows the mapping of the first layer weights (dimension 128x3x3x3) onto the analog crossbar array. The analog MAC outputs from the crossbar are converted to digital values by the Peripheral circuits. The DetectX module being a digital circuit, is appended at the end of the Peripheral stage.

Effects of Crossbar Non-idealities on DetectX’s performance: DetectX is device agnostic, i.e, it can be integrated with different device-based crossbar architectures. However, the detection performance is affected by device non-idealities like variation in weights as shown in Fig. 8b. Here, for adversarial detection, we use PGD $[\epsilon=16/255,\alpha=2/255,n=10]$ attacks. For a SRAM device based analog crossbar architecture, the variation of weights is minimal. Hence, we observe a high
The crossbar is interfaced with Peripheral phase trained on CIFAR10 dataset) onto the crossbar array. Mapping of the first layer weights of the VGG8 network (dual-steps of the analog crossbar+DetectX system. a) Shows the Fig. 8: The overall hardware implementation and evaluation for mapping the DNN layer [17].

The deeper layers where multiple analog crossbars are used decreases. This leads to an increase in the ROC-AUC score. Hence, a higher ROC-AUC score is observed. Moreover, as the crossbar size is decreased, the overall device non-ideality decreases. This leads to an increase in the ROC-AUC score. Further, DetectX is immune to ADC quantization noise. This is because, DetectX is augmented at the end of the first layer of the DNN. Quantization noise effect is more prevalent in the deeper layers where multiple analog crossbars are used for mapping the DNN layer [17].

To improve the performance of DetectX under the impact of hardware non-idealities like device conductance variations, process-voltage-temperature (PVT) variations among others, variation aware training methods [45] can be employed during the dual-phase training. Additionally, new 3D crossbar architectures [46] and memristive devices [47] can be utilized to minimize the bit-line parasitic capacitance/resistances and device conductance variations, respectively which can ultimately improve the performance of DetectX.

**Energy Evaluation of the Crossbar+DetectX System:** For energy evaluation, we use a 128x128 RRAM based crossbar. The parameters of the RRAM device used is shown in Fig. 9a. In Neurosim, each memristive device has 4 analog levels (or 2-bits). Therefore, to implement 8-bit weights, each compute cell in the analog crossbar array contains 4 RRAM devices. Based on the mapping scheme followed by [26], each crossbar column outputs 1 output feature map (OFMs). Additionally, in Neurosim, each layer is mapped onto $K^2$ crossbars. Here, $K$ is the kernel dimension. Based on this, the number of crossbars required to map the first layer of the VGG8 network is 9. Each individual crossbar outputs a partial sum value of the total MAC output. The individual partial sums from each crossbar are summed up resulting in 128 final MAC outputs. The Peripheral circuit consists of 8:1 MUX and 8-bit ADCs for analog to digital conversion. For the given 128x128 crossbar, we require sixteen 8:1 MUX and sixteen 8-bit ADCs in the Peripheral circuit. This has been shown in the Fig. 9a.

The parameters $N_A, N_R, N_C$ are determined by the number of output ADCs in the Peripheral circuit. Based on 16 ADCs, the number of $L1$ Adders $N_{L1}$ is 16. This implies that the number of $L2$ Adders $N_{L2}$ are $16+8+4+2+1 = 31$. Likewise, the value of the parameter $N_R = 16$. This has been shown in Fig. 9b. Note that the number of LUT and RNG do not depend on the Peripheral circuit configurations.

Another factor that determines the energy of the DetectX module is $N_C$. $N_C$ denotes the number of cycles required to sample all the MAC outputs from the analog crossbar. To compute $N_C$, we consider a 32x32x3 sample input from the CIFAR10 dataset. The number of read cycles required to read all the OFMs is equal to the MUX ratio = 8. Additionally, there are 32x32 output features (OFs) corresponding to each OFM. Hence, the effective number of cycles $N_C = 32*32*8 = 8192$. This has been shown in the Fig. 9c.

The final Energy/SoI value of the DetectX module is calculated using the equation shown in Fig. 9d. The Energy/SoI of the DetectX module consists of two components: $E_{STATIC}$ and $E_{LUT}$. The $E_{STATIC}$ is independent of the input data and is the summation of energies $E_A$, $E_R$ and $E_{RNG}$. Hence, the value of $E_{STATIC}$ is 2674.7 pJ. To compute the energy of the data dependent $E_{LUT}$ value, we assume that $N_X = 9$. This is the highest number of LUT accesses (for the worst case) as seen in Fig. 9e. Using this, the total Energy/SoI value is 2679.7 pJ.

In the next section, we perform experiments using the Neurosim+DetectX system. Note, that crossbar non-idealities are beyond the scope of this paper. Hence, for all experiments, we assume that the crossbar outputs are free from any kind of device conductance variations. We will perform a detailed analysis of DetectX+non-ideal crossbar system in the future works.
Fig. 9: a) Tables showing the analog crossbar and RRAM device parameters used for hardware evaluation. b) Based on the crossbar configurations (16 output ADCs) as seen in (a), the parameters of the DetectX module are listed. c) The number of cycles required to read all the output features are computed based on the DNN network parameters like number of input and output feature maps (IFMs and OFMs), output size and size of the MUX. d) The data independent $E_{STATIC}$ is computed using $E_A$, $E_R$ and $E_{RNG}$ are computed from the Fig. 7a. The final Energy per SoI $E_{SoI}$ is computed by adding the data independent energy $E_{STATIC}$ and the data dependent LUT access energy $E_{LUT}$. Note, we assume that the number of accesses are 9 while calculating the value of $E_{SoI}$. e) The distribution of the data dependent LUT access energy $E_{LUT}$.

VI. EXPERIMENTS AND RESULTS

A. Experiment setup

We evaluate the crossbar implemented Neurosim+DetectX system using three datasets of varying complexity. First, the CIFAR10 image dataset, which has 60K samples (50k training/10k testing) divided among 10 classes. Second, the CIFAR100 dataset which has 60k samples (50k training/10k testing) divided among 100 classes. Finally, the TinyImageNet dataset having 110k samples (100k training/10k testing) divided among 200 classes. The input dimensions of the samples in CIFAR10/CIFAR100 and TinyImagenet are 32x32 and 64x64, respectively. For the CIFAR10, CIFAR100 and TinyImagenet datasets, we use the VGG8, VGG16 and ResNet18 network architectures, respectively.

The dual-phase training is performed on the Pytorch framework in an offline manner. For hardware evaluation, we implement the DNN+DetectX system of the Neurosim platform. In all our experiments, we use 8-bit quantization for both DNN weights and activations. For training, we use the Stochastic Gradient Descent (SGD) optimization algorithm. Additionally, for all datasets, we enforce the following hyper-parameters for training [learning rate (LR) = $10^{-3}$ and epochs= 257]. In all the experiments, for Phase1 training, we use the training dataset [clean + PGD ($\epsilon$=1/255, $\alpha$=4/255, n=10)]. While, in the Phase 2 adversarial training, we use training set [clean + PGD ($\epsilon$=4/255, $\alpha$=2/255, n=10)]. For creating the SoI-Probability LUT, we use $D_c$ = clean SoIs and $D_a$ = SoI distribution corresponding to PGD [$\epsilon$=8/255, $\alpha$=4/255, n=10] inputs. The adversarial inputs in all the cases are generated offline i.e on the Pytorch framework. The Neurosim framework is used only during the hardware evaluation explained in Section V-C. The value for hyperparameters $\lambda_c$ and $\lambda_a$ are 0.1 and 0.6, respectively, in all our experiments.

B. Robustness of the Neurosim+DetectX System

In this section, we evaluate the robustness of the Neurosim+DetectX system against different strengths and types of adversarial attacks. For evaluation, we use the metrics ROC-AUC, Error and Accuracy explained in Section II-C. Additionally we evaluate the performance of the DetectX module on random gaussian noise attacks.

In Fig. 10, we detect WB and BB PGD attacks of varying strengths using the Neurosim+DetectX system trained on CIFAR10 dataset and VGG8 architecture. Here, the strength of the adversarial attacks A, B, C and D increase from left to right. We find that the ROC-AUC curves for WB and BB attacks have similar trends. This shows that DetectX is agnostic towards WB and BB adversarial attacks.

Table I shows the overall robustness of the Neurosim+DetectX system for different datasets. For each dataset, we mention the DNN architecture, Phase1 and Phase2 adversarial data on the top. The notations $D$ and $B$ stand for Neurosim+DetectX system and the baseline model, respectively.
TABLE I: Robustness evaluation of the Neurosim+DetectX system with different image datasets and adversarial attacks. We mention the adversarial datasets used for Phase1 and Phase2 training corresponding to each dataset. D and B denote the Neurosim+DetectX system and baseline model respectively. The baseline model is a DNN trained on clean inputs in the standard manner.

| Attack | CIFAR10 VGG8 Phase1- [{\(e = 32/255\), \(n=10\)}], Phase2- [{\(e = 4/255\), \(n=255\), \(n=10\)}] | CIFAR100 VGG16 Phase1- [{\(e = 32/255\), \(n=10\)}], Phase2- [{\(e = 4/255\), \(n=255\), \(n=10\)}] | TinyImagenet ResNet18 Phase1- [{\(e = 32/255\), \(n=10\)}], Phase2- [{\(e = 4/255\), \(n=255\), \(n=10\)}] |
|--------|-------------------------------------------------|-------------------------------------------------|-------------------------------------------------|
| ROC-AUC | 0.97 / 0.99 | 0.97 / 0.99 | 0.97 / 0.99 |
| Accuracy D / B | 80.1 / 87 | 80.1 / 87 | 80.1 / 87 |
| WB Error D / B | 1.7 / 35.3 | 1.7 / 35.3 | 1.7 / 35.3 |
| BB Error D / B | 1.6 / 63.8 | 1.6 / 63.8 | 1.6 / 63.8 |
| CIFAR10 VGG8 Phase1- [{\(e = 32/255\), \(n=10\)}], Phase2- [{\(e = 4/255\), \(n=255\), \(n=10\)}] | CIFAR100 VGG16 Phase1- [{\(e = 32/255\), \(n=10\)}], Phase2- [{\(e = 4/255\), \(n=255\), \(n=10\)}] | TinyImagenet ResNet18 Phase1- [{\(e = 32/255\), \(n=10\)}], Phase2- [{\(e = 4/255\), \(n=255\), \(n=10\)}] |
| ROC-AUC | 0.98 / 0.99 | 0.98 / 0.99 | 0.98 / 0.99 |
| Accuracy D / B | 50.1 / 60.2 | 50.1 / 60.2 | 50.1 / 60.2 |
| WB Error D / B | 5.1 / 59.4 | 5.1 / 59.4 | 5.1 / 59.4 |
| BB Error D / B | 4.9 / 55.6 | 4.9 / 55.6 | 4.9 / 55.6 |
| CIFAR10 VGG8 Phase1- [{\(e = 32/255\), \(n=10\)}], Phase2- [{\(e = 4/255\), \(n=255\), \(n=10\)}] | CIFAR100 VGG16 Phase1- [{\(e = 32/255\), \(n=10\)}], Phase2- [{\(e = 4/255\), \(n=255\), \(n=10\)}] | TinyImagenet ResNet18 Phase1- [{\(e = 32/255\), \(n=10\)}], Phase2- [{\(e = 4/255\), \(n=255\), \(n=10\)}] |
| ROC-AUC | 0.84 | 0.84 | 0.84 |
| Accuracy D / B | 42.2 / 53.5 | 42.2 / 53.5 | 42.2 / 53.5 |
| WB Error D / B | 13.2 / 56.5 | 13.2 / 56.5 | 13.2 / 56.5 |
| BB Error D / B | 10.17 / 55.47 | 10.17 / 55.47 | 10.17 / 55.47 |

Fig. 10: DetectX is agnostic towards the type of adversarial attack (WB or BB). Hence, the ROC-AUC curves for both WB and BB attacks follow similar trends. Additionally, for weak adversarial attacks, the ROC-AUC score decreases slightly. Here, A- PGD[8/255, 2/255, 10], B- PGD[16/255, 4/255, 10] C- PGD[32/255, 4/255, 10] D- PGD[32/255, 8/255, 10]. Although, we show the results obtained for CIFAR10 dataset on a VGG8 network, the trends of the ROC-AUC scores remain constant across different datasets.

The baseline model is a DNN trained in the standard manner on clean data. We report a single ROC-AUC for both WB and BB attacks because of the attack agnostic property of DetectX. Additionally, the Accuracy is not affected by the type and strength of adversarial attacks. This is because \(D_c\) and the Soft-Probability LUT remains constant for each dataset. However, Error strongly depends on the type and strength of the attack. Hence, we individually report the Error values corresponding to WB and BB attacks.

For generating WB attacks, we use the cross-entropy loss function (Equation 4) of the Neurosim+DetectX system. For generating BB attacks, we use the following dataset and DNN combinations: (CIFAR10, VGG16), (CIFAR100, ResNet18) and (TinyImagenet, VGG16). All the networks are trained in the standard manner on clean data.

Overall, for both FGSM and PGD attacks, the Neurosim+DetectX system has a high ROC-AUC score. Consequently, this leads to very low Error values for both WB and BB attacks when compared to the baseline model. Additionally, the performance with CIFAR10 and CIFAR100 datasets is better than the TinyImagenet dataset. This is because of the wide data distribution of the TinyImagenet dataset. For weaker adversarial attacks, the ROC-AUC score is slightly lower than the stronger attacks. This increases the Error value. However, with Phase2 adversarial training the increase in the Error value is compensated. Additionally, the dual-phase training also causes a drop in Accuracy compared to the baseline model.

Fig. 11 demonstrates the efficacy of the dual-phase training. Here, weak WB PGD attacks are launched on the Neu-
In this work, we propose a hardware-centric adversarial detection strategy, DetectX. We show that hardware-based signatures like Sum of column Currents (SoI) in analog crossbar arrays can be used for adversarial detection. Since DetectX does not require any neural network-based detector, it is highly energy efficient compared to the previous state-of-the-art works. At the same time, DetectX is also proficient in defending the DNN against various gradient and non-gradient based adversarial attacks of different strengths. Finally, the DetectX approach is device agnostic. Meaning, that DetectX can be augmented with analog crossbar arrays irrespective of the memristive device used.

VII. Conclusion

In this work, we propose a hardware-centric adversarial detection strategy, DetectX. We show that hardware-based signatures like Sum of column Currents (SoI) in analog memristive crossbar arrays can be used to detect adversarial inputs. For this, we use a dual-phase training approach to increase the separation between clean and adversarial SoIs. We implement the DetectX module using 32nm CMOS Predictive
the state-of-the-art works. Note, PGD\[x,y,z\] means \(\epsilon=x/255, \alpha=y/255\) and \(n= z\). a) Comparison of ROC-AUC scores and Error values for CIFAR10 dataset implemented on the VGG16 Network. It can be seen that with weak \(\epsilon\) attacks, DetectX has a slightly lower performance when compared to Metzen et al. [13] and Sterneck et al. [12]. However, due to Phase2 training, the Error values are maintained at low values. b) With strong \(\epsilon\) attacks, DetectX outperforms both Sterneck et al. [12] and Yin et al. [14]. c) Due to attack agnostic behaviour of DetectX, the performance is equally high for \(\delta\) attacks. d) Finally, DetectX consumes more than 10x lower energy when compared to other state-of-the-art works. The neural network based detectors of Metzen et al. [13] and Sterneck et al. [12] are implemented on the Neurosim platform for energy evaluation. The energy of the DetectX module is computed using the procedure discussed in Section V.C.

![Comparison of detection performance and energy consumption of the Neurosim+DetectX system with other state-of-the-art works.](image-url)

**Fig. 13:** Comparison of detection performance and energy consumption of the Neurosim+DetectX system with other state-of-the-art works. Note, PGD\[x,y,z\] means \(\epsilon=x/255, \alpha=y/255\) and \(n= z\). a) Comparison of ROC-AUC scores and Error values for CIFAR10 dataset implemented on the VGG16 Network. It can be seen that with weak \(\epsilon\) attacks, DetectX has a slightly lower performance when compared to Metzen et al. [13] and Sterneck et al. [12]. However, due to Phase2 training, the Error values are maintained at low values. b) With strong \(\epsilon\) attacks, DetectX outperforms both Sterneck et al. [12] and Yin et al. [14]. c) Due to attack agnostic behaviour of DetectX, the performance is equally high for \(\delta\) attacks. d) Finally, DetectX consumes more than 10x lower energy when compared to other state-of-the-art works. The neural network based detectors of Metzen et al. [13] and Sterneck et al. [12] are implemented on the Neurosim platform for energy evaluation. The energy of the DetectX module is computed using the procedure discussed in Section V.C.

Technology Model: The DetectX module consists of a SoI computing unit and a simple Look-Up Table based detector. We integrate the DetectX module with the Neurosim crossbar evaluation platform. Our experiments on benchmark datasets show that DetectX is highly energy efficient and achieves state-of-the-art detection performance against strong white box and black box attacks in comparison to previous works. Thus, DetectX is an energy efficient and robust solution for adversarial input detection on hardware.

**VIII. ACKNOWLEDGEMENT**

This work was supported in part by C-BRIC, Center for Brain-inspired Computing, a JUMP center sponsored by DARPA and SRC, the National Science Foundation (Grant#1947826), the Technology Innovation Institute, Abu Dhabi and the Amazon Research Award.

**REFERENCES**

[1] S. Huang, N. Papernot, I. Goodfellow, Y. Duan, and P. Abbeel, “Adversarial attacks on neural network policies,” arXiv preprint arXiv:1702.02284, 2017.

[2] Y. Dong, F. Liao, T. Pang, H. Su, J. Zhu, X. Hu, and J. Li, “Boosting adversarial attacks with momentum,” in Proceedings of the IEEE conference on computer vision and pattern recognition, 2018, pp. 9185–9193.

[3] O. Ibitoye, O. Shafiq, and A. Matrawy, “Analyzing adversarial attacks against deep learning for intrusion detection in iot networks,” in 2019 IEEE Global Communications Conference (GLOBECOM). IEEE, 2019, pp. 1–6.

[4] N. Akhtar and A. Mian, “Threat of adversarial attacks on deep learning in computer vision: A survey,” IEEE Access, vol. 6, pp. 14 410–14 430, 2018.

[5] A. Shafahi, M. Najibi, A. Ghiasi, Z. Xu, J. Dickerson, C. Studer, L. S. Davis, G. Taylor, and T. Goldberg, “Adversarial training for free!” arXiv preprint arXiv:1904.12847, 2019.

[6] A. Madry, A. Makelov, L. Schmidt, D. Tsipras, and A. Vladu, “Towards deep learning models resistant to adversarial attacks,” arXiv preprint arXiv:1706.06083, 2017.

[7] Y. Ganin, E. Ustinova, H. Ajakan, P. Germain, H. Larochelle, F. Laviolette, M. Marchand, and V. Lempitsky, “Domain-adversarial training of neural networks,” The journal of machine learning research, vol. 17, no. 1, pp. 2096–2030, 2016.

[8] G. K. Dziugaite, Z. Ghahramani, and D. M. Roy, “A study of the effect of jpg compression on adversarial images,” arXiv preprint arXiv:1608.00853, 2016.

[9] C. Xie, J. Wang, Z. Zhang, Y. Zhou, L. Xie, and A. Yuille, “Adversarial examples for semantic segmentation and object detection,” in Proceedings of the IEEE International Conference on Computer Vision, 2017, pp. 1369–1378.

[10] C. Xie, J. Wang, Z. Zhang, Z. Ren, and A. Yuille, “Mitigating adversarial effects through randomization,” arXiv preprint arXiv:1711.01991, 2017.

[11] Z. He, A. S. Rakin, and D. Fan, “Parametric noise injection: Trainable randomness to improve deep neural network robustness against adversarial attack,” in Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition, 2019, pp. 588–597.

[12] R. Sterneck, A. Moitra, and P. Panda, “Noise sensitivity-based energy efficient and robust adversary detection in neural networks,” arXiv preprint arXiv:2101.01543, 2021.

[13] J. H. Metzen, T. Genevein, V. Fischer, and B. Bischoff, “On detecting adversarial perturbations,” arXiv preprint arXiv:1702.04267, 2017.

[14] X. Yin, S. Kolouri, and G. K. Rohde, “Gat: Generative adversarial training for adversarial example detection and robust classification,” in International Conference on Learning Representations, 2019.

[15] K. Grosse, P. Manoharan, N. Papernot, M. Backes, and P. McDaniel, “On the (statistical) detection of adversarial examples,” arXiv preprint arXiv:1702.06280, 2017.

[16] M. J. Marinella, S. Agarwal, A. Hoia, I. Richter, R. Jacobs-Gedrim, I. Niroula, S. J. Plimpton, E. Ipek, and C. D. James, “Multiscale code design analysis of energy, latency, area, and accuracy of a reram analog neural training accelerator,” IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 8, no. 1, pp. 86–101, 2018.

[17] P.-Y. Chen, X. Peng, and S. Yu, “NeuroSim: A circuit-level macro model for benchmarking neuro-inspired architectures in online learning,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 37, no. 12, pp. 3067–3080, 2018.

[18] A. Shafiee, A. Nag, N. Muralimanohar, R. Balasubramonian, J. P. Strachan, M. Hu, R. S. Williams, and V. Srikumar, “Isaac: A convolutional neural network accelerator with in-situ analog arithmetic in crossbars,” ACM SIGARCH Computer Architecture News, vol. 44, no. 3, pp. 14–26, 2016.

[19] P. Chi, S. Li, C. Xu, T. Zhang, J. Zhao, Y. Liu, Y. Wang, and Y. Xie, “Prime: A novel processing-in-memory architecture for neural network computation in reram-based main memory,” ACM SIGARCH Computer Architecture News, vol. 44, no. 3, pp. 27–39, 2016.

[20] X. Liu, M. Mao, B. Liu, B. Li, Y. Wang, H. Jiang, M. Barnell, Q. Wu, J. Yang, H. Li et al., “Harmonica: A framework of heterogeneous computing systems with memristor-based neuromorphic computing accelerators,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 5, pp. 617–628, 2016.

[21] Q. Xia and J. J. Yang, “Memristive crossbar arrays for brain-inspired computing,” Nature materials, vol. 18, no. 4, pp. 309–323, 2019.

[22] W.-H. Chen, K.-X. Li, W.-Y. Lin, K.-H. Hsu, P.-Y. Li, C.-H. Yang, C.-X. Xue, E.-Y. Yang, Y.-K. Chen, Y.-S. Chang et al., “A 65nm 1mb nonvolatile computing-in-memory reram macro with sub-10ns multiply- and-accumulate for binary dnn ai edge processors,” in 2018 IEEE
[23] H.-S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, and M.-J. Tsai, “Metal–oxide rram,” Proceedings of the IEEE, vol. 100, no. 6, pp. 1951–1970, 2012.

[24] M. Jerry, P.-Y. Chen, J. Zhang, P. Sharma, K. Ni, S. Yu, and S. Datta, “Ferroelectric fet analog synapse for acceleration of deep neural network training,” in 2017 IEEE International Electron Devices Meeting (IEDM). IEEE, 2017, pp. 6–2.

[25] D. Reis, M. Niemier, and X. S. Hu, “Computing in memory with fets,” in Proceedings of the International Symposium on Low Power Electronics and Design, 2018, pp. 1–6.

[26] X. Peng, S. Huang, Y. Luo, X. Sun, and S. Yu, “Dnn+ neurosim: An end-to-end benchmarking framework for compute-in-memory accelerators with versatile device technologies,” in 2019 IEEE International Electron Devices Meeting (IEDM). IEEE, 2019, pp. 32–5.

[27] A. Balijepalli, S. Sinha, and Y. Cao, “Compact modeling of carbon nanotube transistor for early stage process-design exploration,” in Proceedings of the 2007 international symposium on Low power electronics and design, 2007, pp. 2–7.

[28] A. Krizhevsky, G. Hinton et al., “Learning multiple layers of features from tiny images,” 2009.

[29] Y. Le and X. Yang, “Tiny imagenet visual recognition challenge,” CS 231N, vol. 7, p. 7, 2015.

[30] H. Jiang, W. Li, S. Huang, S. Cosemans, F. Catthoor, and S. Yu, “Analog-to-digital converter design exploration for compute-in-memory accelerators,” IEEE Design & Test, 2021.

[31] R. Arora, A. Basu, P. Mianjy, and A. Mukherjee, “Understanding deep neural networks with rectified linear units,” arXiv preprint arXiv:1611.01491, 2016.

[32] M. R. Zadeh, S. Amin, D. Khalili, and V. P. Singh, “Daily outflow prediction by multi layer perceptron with logistic sigmoid and tangent sigmoid activation functions,” Water resources management, vol. 24, no. 11, pp. 2673–2688, 2010.

[33] M. R. Zadeh, S. Amin, D. Khalili, and V. P. Singh, “Daily outflow prediction by multi layer perceptron with logistic sigmoid and tangent sigmoid activation functions,” Water resources management, vol. 24, no. 11, pp. 2673–2688, 2010.

[34] K. Grosse et al., “On the (statistical) detection of adversarial examples,” arXiv preprint arXiv:1702.06280, 2017.

[35] Z. Gong et al., “Adversarial and clean data are not twins,” arXiv preprint arXiv:1704.04960, 2017.

[36] R. Feinman et al., “Detecting adversarial samples from artifacts,” arXiv preprint arXiv:1703.00410, 2017.

[37] K. Grosse et al., “On the (statistical) detection of adversarial examples,” arXiv preprint arXiv:1702.06280, 2017.

[38] Z. Gong et al., “Adversarial and clean data are not twins,” arXiv preprint arXiv:1704.04960, 2017.

[39] R. Feinman et al., “Detecting adversarial samples from artifacts,” arXiv preprint arXiv:1703.00410, 2017.

[40] X. Li et al., “Adversarial examples detection in deep networks with convolutional filter statistics,” in Proceedings of the IEEE ICCV, 2017, pp. 5764–5772.

[41] L. T. Clark, S. B. Medapuram, and D. K. Kadiyala, “Sram circuits for true random number generation using intrinsic bit instability,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 26, no. 10, pp. 2027–2037, 2018.

[42] K. Simonyan and A. Zisserman, “Very deep convolutional networks for large-scale image recognition,” arXiv preprint arXiv:1409.1556, 2014.

[43] A. Agrawal, C. Lee, and K. Roy, “X-change: Changing memristive crossbar mapping for mitigating line-resistance induced accuracy degradation in deep neural networks,” arXiv preprint arXiv:1907.00285, 2019.

[44] J. K. Eshraghian, K. Cho, and S. M. Kang, “Crossstack: A 3-d reconfigurable ram crossbar inference engine,” arXiv preprint arXiv:2102.06536, 2021.

[45] H. An, M. S. Al-Mamun, M. K. Orlowski, L. Liu, and Y. Yi, “Robust deep reservoir computing through reliable memristor with improved heat dissipation capability,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020.