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Abstract: The inner spacer thickness (T_{IS}) variations in sub-3-nm, node 3-stacked, nanosheet field-effect transistors (NSFETs) were investigated using computer-aided design simulation technology. Inner spacer formation requires a high selectivity of SiGe to Si, which causes inevitable T_{IS} variation (ΔT_{IS}). The gate length (L_G) depends on the T_{IS}. Thus, the DC/AC performance is significantly affected by ΔT_{IS}. Because the effects of ΔT_{IS} on the performance depend on which inner spacer is varied, the sensitivities of the performance to the top, middle, and bottom (T, M, and B, respectively) ΔT_{IS} should be studied separately. In addition, the source/drain (S/D) recess process variation that forms the parasitic bottom transistor (tr_{pbt}) should be considered with ΔT_{IS} because the gate controllability over tr_{pbt} is significantly dependent on ΔT_{IS,B}. If the S/D recess depth (T_{SD}) variation cannot be completely eliminated, reducing ΔT_{IS,B} is crucial for suppressing the effects of tr_{pbt}. It is noteworthy that reducing ΔT_{IS,B} is the most important factor when the T_{SD} variation occurs, whereas reducing ΔT_{IS,T} and ΔT_{IS,M} is crucial in the absence of T_{SD} variation to minimize the DC performance variation. As the T_{IS} increases, the gate capacitance (C_{gg}) decreases owing to the reduction in both parasitic and intrinsic capacitance, but the sensitivity of C_{gg} to each ΔT_{IS} is almost the same. Therefore, the difference in performance sensitivity related to AC response is also strongly affected by the DC characteristics. In particular, since T_{SD} of 5 nm increases the off-state current (I_{off}) sensitivity to ΔT_{IS,B} by a factor of 22.5 in NFETs, the ΔT_{IS,B} below 1 nm is essential for further scaling and yield enhancement.

Keywords: nanosheet FET; inner spacer; inner spacer thickness variation; performance sensitivity; source/drain recess depth; TCAD simulation

1. Introduction

Silicon fin-shaped field-effect transistors (FinFETs) have been continuously scaled down from 22-nm to 5-nm nodes using fins with high aspect ratios and design technology co-optimization [1–6]. However, increasing the fin aspect ratio is challenging owing to the process complexity, and FinFETs with narrow fins exhibit threshold-voltage variations and performance degradation induced by the quantum confinement effect [7–10]. By contrast, Silicon gate-all-around nanosheet field-effect transistors (NSFETs) have received considerable attention as promising devices that can replace FinFETs in sub-3-nm nodes, as they can overcome these limitations through stacked nanosheet (NS) channels [11]. Furthermore, NSFETs provide excellent electrostatics because the gate surrounds the NS channels and drives a larger current within the same footprint with a wider effective channel width than FinFETs [11,12].

The inner spacer is a distinctive structural feature of NSFETs that has not been employed in previous devices. Typically, selective etching of the SiGe sacrificial layers is performed to form the inner spacer. However, selective etching requires a high selectivity of SiGe to Si and lateral etching. Therefore, it can be vulnerable to process variations [13,14].
Furthermore, because the inner spacer determines the gate length ($L_G$), these variations result in NSFETs with unintended $L_G$ changes and cause unoptimized leakage and DC/AC performance. Therefore, precise control of the inner spacer thickness ($T_{IS}$) is crucial for performance optimization.

Previous studies related to the inner spacer have focused on the electrical properties of NSFETs, assuming the same shape and thickness from the top inner spacer to the bottom inner spacer. However, in the actual process, the $T_{IS}$ variation ($\Delta T_{IS}$) may not occur uniformly. In addition, for three-stacked NSFETs, the top and middle inner spacers adjoin two adjacent NS channels, while the bottom inner spacer adjoins only one NS channel and a punch-through stopper (PTS) region. Thus, the thickness variations of the top/middle/bottom ($T/M/B$) inner spacers have different effects on the device behavior; i.e., the $T/M/B$ $\Delta T_{IS}$ ($\Delta T_{IS,T}/\Delta T_{IS,M}/\Delta T_{IS,B}$) have different effects on the performance. Therefore, the performance sensitivities must be studied separately. Additionally, the over-etched S/D recess is a crucial factor determining the effects of the parasitic bottom transistor ($t_{pbt}$) on the DC performance. The effects of $t_{pbt}$ on performance become more pronounced as $L_G$ decreases, which is a potential threat for further scaling. However, there have been no studies on the effects of the S/D recess depth ($T_{SD}$) along with $T/M/B$ $\Delta T_{IS}$ on the device behavior. In this study, for the first time, we comprehensively analyzed the sensitivity of the DC/AC characteristics to each $\Delta T_{IS}$ considering the $T_{SD}$, and the off-state characteristics were analyzed in detail using fully calibrated computer-aided design (TCAD) simulation technology.

### 2. Device Structure and Simulation Methodology

The sub-3-nm node NSFETs investigated in this study were simulated using Sentaurus TCAD tools. The following physical models were considered in the TCAD simulation:

- The drift–diffusion model was considered using Poisson’s equations and the continuity equations to determine the electrostatic potential and carrier transport.
- The density gradient model was considered for the quantum confinement effect in the drift-diffusion model.
- The Slotboom bandgap narrowing model was considered for doping-dependent bandgap narrowing in Si and SiGe.
- A low-field ballistic mobility model was considered for quasi-ballistic transport.
- Mobility degradation at the interfaces was considered for remote phonon scattering and remote Coulomb scattering.
- The inversion and accumulation layer mobility models were considered for Coulomb impurity, phonon scattering, and surface roughness scattering.
- A high-field saturation model was considered for carrier velocity saturation under a strong electric field.
- The deformation potential model was considered for the strain-induced density of states, effective mass of carriers, and energy-band shift.
- The Auger and Shockley–Read–Hall (SRH) recombination models were used.

Figure 1a shows schematics of the sub-3-nm node 3-stacked NSFETs. Among the $T/M/B$ $\Delta T_{IS}$, we varied only one of the $T/M/B$ $T_{IS}$, with the others fixed at 5 nm, to investigate the effects of the $T/M/B$ $\Delta T_{IS}$ on the DC/AC characteristics separately. Here, the thicknesses of the $T/M/B$ inner spacers were defined as $T_{IS,T}$, $T_{IS,M}$, and $T_{IS,B}$, respectively. In addition, $T_{SD}$ of 0 and 5 nm were used to consider the effects of $T_{SD}$ along with those of $\Delta T_{IS}$. Therefore, a comprehensive analysis of $\Delta T_{IS}$ considering the $T_{SD}$ effect was performed.
The $T_{IS}$ without variation ($T_{IS,ref}$) was set as 5 nm, and only one of the three $T_{IS}$ was varied from 3 to 7 nm (Figure 1b). In this study, $\Delta T_{IS}$ was defined as $T_{IS} - T_{IS,ref}$, and the $L_G$ of each channel depended on $\Delta T_{IS}$ ($L_G = 22 - 2 \times (T_{IS,ref} + \Delta T_{IS})$). $Si_{0.98}Ge_{0.02}$ ($Si_{0.5}Ge_{0.5}$) S/D doped with phosphorus (boron) at $4 \times 10^{20}$ cm$^{-3}$ was used for the NFETs (PFETs). The contact resistance of the S/D was set as 1 n$\Omega$·cm$^{2}$. The PTS layer was doped at $3 \times 10^{18}$ cm$^{-3}$, and the drain voltage ($V_{ds}$) was fixed at $|0.7|$ V. The geometric parameters are presented in Table 1. The NSFETs were calibrated to TSMC’s 5-nm node FinFETs [5], and the same physical parameters were used, as shown in our previous studies [29]. The drain current was fitted by adjusting the doping profile, ballistic coefficient, and saturation velocity. The doping profile was changed to fit the device behaviors in the subthreshold region. The ballistic coefficient was tuned to fit the drain current in the linear region, and the saturation velocity was set to fit the drain current in the saturation region. We extracted the on-state current ($I_{on}$) and gate capacitance ($C_{gs}$) at $|V_{gs}| = 0.7$ V and $|V_{ds}| = 0.7$ V. Moreover, the off-state current ($I_{off}$) and parasitic capacitance ($C_{para}$) were extracted at $|V_{gs}| = 0$ V and $|V_{ds}| = 0.7$ V.

Figure 1. (a) Structure of NSFETs with the $T_{SD}$ and cross-sectional views. (b) Schematics of $\Delta T_{IS}$ and its definition.
### Table 1. Geometric parameters for sub-3-nm node NSFETs.

| Fixed Parameters                      | Values                      |
|---------------------------------------|-----------------------------|
| Contact poly pitch (CPP)              | 42 nm                       |
| Fin pitch (FP)                        | 60 nm                       |
| Gate length ($L_G$)                   | 12 nm                       |
| Spacing thickness ($T_{SP}$)          | 10 nm                       |
| NS thickness ($T_{CH}$)               | 5 nm                        |
| NS width ($W_{NS}$)                   | 25 nm                       |
| Interfacial layer thickness ($T_{IL}$)| 0.6 nm                      |
| HfO$_2$ thickness ($T_{HfO2}$)        | 1.1 nm                      |
| $T_{IS}$ without variation ($T_{IS,ref}$) | 5 nm                       |
| S/D doping concentration ($N_{SD}$)    | $4 \times 10^{20}$ cm$^{-3}$|
| PTS doping concentration ($N_{PTS}$)   | $3 \times 10^{18}$ cm$^{-3}$|
| Variable parameters                   |                             |
| Excess S/D recess depth ($T_{SD}$)    | 0 or 5 nm                   |
| Inner spacer thickness ($T_{IS}$)      | 3–7 nm                      |

### 3. Results and Discussion

Figure 2 shows the transfer curves of NSFETs with different $T_{IS,B}$ for $T_{SD} = 0$ and 5 nm. No significant dependence of the DC performance on $\Delta T_{IS,B}$ was observed at $T_{SD} = 0$ (Figure 2a). By contrast, at $T_{SD} = 5$ nm, the $I_{off}$ increased significantly as $T_{IS,B}$ increased (Figure 2b). The $T_{SD}$ typically impacts the $I_{off}$ of tr$_{pbt}$ [17], where $T_{IS,B}$ determines the $L_G$ of tr$_{pbt}$. Because the $L_G$ of tr$_{pbt}$ affects the gate controllability over the PTS region, an increase in $\Delta T_{IS,B}$ significantly degrades the DC performance. As an increase in $T_{SD}$ degrades the gate controllability of tr$_{pbt}$, $T_{IS,B}$ is a critical factor determining the parasitic punch-through current ($I_{pbt}$) in the PTS region. Therefore, the subthreshold swing and DIBL are significantly degraded, as shown in the inset of Figure 2 and Table 2.

![Figure 2](image_url)

**Figure 2.** Transfer curves of the NSFETs having different $T_{IS,B}$ with (a) $T_{SD} = 0$ nm and (b) $T_{SD} = 5$ nm.
The $I_{\text{off}}$ sensitivities to the T/M/B $\Delta T_{\text{IS}}$ ($S_{\text{loff,T}}/S_{\text{loff,M}}/S_{\text{loff,B}}$) are compared in Figure 3. We defined $S_{\text{loff}}$ as the slope of $I_{\text{off}}-\Delta T_{\text{IS}}$, which indicates how sensitively $I_{\text{off}}$ varies with respect to $\Delta T_{\text{IS}}$. For the NFETs with $T_{\text{SD}} = 0$ nm, the $S_{\text{loff,T}}$ (0.208) and $S_{\text{loff,M}}$ (0.228) slightly exceeded the $S_{\text{loff,B}}$ (0.104 nA/nm), and similar $S_{\text{loff}}$ tendencies were observed for the PFETs. The $T_{\text{SD}}$ variation not only increased $I_{\text{off}}$, but also significantly increased $S_{\text{loff,B}}$ for both the NFETs and the PFETs. The $S_{\text{loff,B}}$ for the NFETs is greater than that for the PFETs, which is mainly attributed to the S/D dopant diffusion into the PTS region. Phosphorus has a higher diffusivity than boron; therefore, more S/D dopant diffuses into the PTS region in NFETs than in PFETs [30]. Consequently, the NFETs are more sensitive to the $\Delta T_{\text{IS,B}}$ in terms of $I_{\text{off}}$. For the NFETs with $T_{\text{SD}} = 5$ nm, $S_{\text{loff,T}}, S_{\text{loff,M}}$, and $S_{\text{loff,B}}$ were 0.195, 0.209, and 2.34 nA/nm, respectively. $S_{\text{loff,T}}$ and $S_{\text{loff,M}}$ were almost identical regardless of the $T_{\text{SD}}$, but $S_{\text{loff,B}}$ increased by a factor of 22.5 when the $T_{\text{SD}}$ increased from 0 to 5 nm. This indicated that the S/D recess process variation slightly affects $S_{\text{loff,T}}$ and $S_{\text{loff,M}}$ but significantly affects $S_{\text{loff,B}}$. Thus, if the $T_{\text{SD}}$ variation is not perfectly eliminated, $\Delta T_{\text{IS,B}}$ should be controlled below 1 nm, because devices with greater than 10 times in $I_{\text{off}}$ are not suitable for the intended system-on-chip applications.

![Figure 3. $I_{\text{off}}$ of NSFETs according to $\Delta T_{\text{IS}}$ with $T_{\text{SD}} = 0$ and 5 nm.](image)

The differences in the $S_{\text{loff}}$ shown in Figure 3 can be explained using the $I_{\text{off}}$-density profiles (Figure 4). In NSFETs with $T_{\text{SD}} = 0$ nm, most carriers existed in the NS channels, and a few were in the PTS region owing to the heavily doped PTS. Furthermore, $\Delta T_{\text{IS}}$-induced $I_{\text{off}}$ density variations mainly arose in the NS channels next to the inner spacer.

| Type  | $T_{\text{IS,B}}$ [nm] | DIBL [mV/V] |
|-------|------------------------|-------------|
|       |                        | $T_{\text{SD}} = 0$ nm | $T_{\text{SD}} = 5$ nm |
| NFETs | 3                      | 60          | 67          |
|       | 5                      | 62          | 72          |
|       | 7                      | 67          | 81          |
| PFETs | 3                      | 51          | 54          |
|       | 5                      | 53          | 57          |
|       | 7                      | 58          | 61          |

Table 2. DIBL of NSFETs according to the $T_{\text{IS,B}}$ and $T_{\text{SD}}$. No significant changes in $I_{\text{off}}$ were observed.
with variations in the thickness. Thus, the top and middle inner spacers adjacent to the NS channels with high carrier concentrations exhibited larger changes in the $I_{\text{off}}$ density than the bottom inner spacer. Therefore, $S_{\text{off},T}$ and $S_{\text{off},M}$ are higher than $S_{\text{off},B}$ for the NSFETs with $T_{SD} = 0 \text{ nm}$. By contrast, $S_{\text{off},B}$ was the highest when the $T_{SD}$ was $5 \text{ nm}$. Figure 4b shows the $I_{\text{off}}$ density profiles for NSFETs with different $T_{IS,B}$ in the case of $T_{SD} = 5 \text{ nm}$. As $T_{IS,B}$ increased, the off-state $I_{\text{pt}}$ ($I_{\text{pt,off}}$) was not suppressed, resulting in a significant increase in $I_{\text{off}}$ as shown in Figure 2. The $I_{\text{off}}$ density varied according to $\Delta T_{IS,B}$ in the bottom NS and PTS regions but varied to a significantly larger extent in the PTS region. Specifically, the $T_{SD}$ variation significantly enhanced the effects of $T_{IS,B}$ on $I_{\text{off}}$, and the change in $I_{\text{pt,off}}$ was a dominant factor in the $S_{\text{off},B}$ increment. This is because the PTS region was only controlled by the bottom gate. Therefore, the bottom gate could not effectively control the PTS region far from the bottom gate. As a result, worse short-channel effects (SCEs) were observed in the PTS region than in the NS channel.

![Figure 4](image_url)

*Figure 4.* (a) $I_{\text{off}}$ density profiles of the NSFETs with $T_{SD} = 0 \text{ nm}$ and each $\Delta T_{IS}$ equal to $2 \text{ nm}$. (b) $I_{\text{off}}$ density profiles of the NSFETs with $T_{SD} = 5 \text{ nm}$ for different values of $\Delta T_{IS,B}$.

Figure 5a shows the conduction band energy ($E_c$) diagrams of the source–PTS–drain in the NSFETs, which were extracted under the off-state bias condition. As the $T_{SD}$ increased from 0 to $5 \text{ nm}$, the significant reduction in the energy barrier height ($\Phi_b$) from 478 to $402 \text{ mV}$ was caused by the larger amount of S/D dopant diffusion into the PTS region at a $T_{SD}$ of $5 \text{ nm}$. In NSFETs with $T_{SD} = 0 \text{ nm}$, the $\Phi_b$ of the PTS region was sufficiently high to control $I_{\text{pt,off}}$ regardless of $\Delta T_{IS,B}$ (Figure 5b). Therefore, $I_{\text{off}}$ can be effectively controlled even with $\Delta T_{IS,B}$. However, if $\Phi_b$ is not sufficiently high, the additional $\Phi_b$ reduction due to $\Delta T_{IS,B}$ can be a critical factor in inducing $I_{\text{pt,off}}$. An additional $\Phi_b$ reduction was observed when $T_{IS,B}$ increased, and the change in $\Phi_b$ by $\Delta T_{IS,B}$ significantly contributed to the $I_{\text{pt,off}}$ variation (Figures 3 and 5c). Therefore, the bottom $I_{\text{G}}$ of $t_{pbt}$, which is related to $T_{IS,B}$, is important for suppressing SCEs in the PTS region. According to these results, $S_{\text{off},B}$ is significantly affected by $T_{SD}$. Thus, minimizing $\Delta T_{IS,B}$ is more crucial when an over-etched S/D recess occurs.

Figure 6 shows the relationship between the on-state current ($I_{\text{on}}$) and $\Delta T_{IS}$, and the slope indicates the $I_{\text{on}}$ sensitivity ($S_{\text{on}}$). For the NSFETs, the $S_{\text{on},T}$ and $S_{\text{on},M}$ are slightly higher than the $S_{\text{on},B}$ regardless of the $T_{SD}$. By contrast, for the PFETs, the $S_{\text{on},B}$ varied significantly with respect to the $T_{SD}$, leading to an increase in $S_{\text{on},B}$ by a factor of 1.9. Thus, an increase in $\Delta T_{IS,B}$ can cause severe $I_{\text{on}}$ variations when the $T_{SD}$ is not precisely controlled. The reason for the differences in the $S_{\text{on}}$ is explained in Figure 7.
Figure 5. (a) Energy band diagram of the source–PTS–drain in NFETs with $T_{SD} = 5$ nm (solid line) and $T_{SD} = 0$ nm (dashed line). The $E_c$ of the PTS region with different $T_{IS,B}$ at (b) $T_{SD} = 0$ and (c) $T_{SD} = 5$ nm.

Figure 6. $I_{on}$ of NSFETs having different $\Delta T_{IS}$ with $T_{SD} = 5$ nm (solid symbols) and $T_{SD} = 0$ nm (open symbols).
The $R_{sd}$ sensitivity ($S_{Rsd}$) and on-state $I_{pt}$ ($I_{pt,on}$)-density variations to the $\Delta T_{IS}$ account for the differences in $T/M/B$ $S_{Ion}$ (Figure 7). $R_{sd}$ was extracted using $Y$-function techniques, as described in [31]. Two main factors determine $S_{Ion}$: $R_{sd}$ and inversion charges in the PTS region. Additionally, the major factors affecting $S_{Ion}$ depend on the $T_{SD}$. For both the NFETs and PFETs with $T_{SD} = 0$ nm, $S_{Ion}$ was mainly affected by the change in $R_{sd}$, which consisted of the series $S/D$ epi resistance ($R_{epi}$) and extension resistance ($R_{ext}$). $R_{epi}$ did not change with respect to $\Delta T_{IS}$, but $R_{ext}$ did. Because $S_{Rsd}$ varied proportionally to the number of NS channels adjacent to the inner spacer where $\Delta T_{IS}$ occurred (Figure 7a), $S_{Ion,T}$ and $S_{Ion,M}$ were greater than $S_{Ion,B}$. However, the inversion charges in the PTS region significantly affected $S_{Ion}$ when $T_{SD}$ was 5 nm. As the deep $T_{SD}$ caused a substantial current to flow through $tr_{pbt}$, the $I_{on}$ contribution of the PTS region was no longer small. The inversion charges in the PTS region should also be considered (Figure 7b). For the NFETs, the $I_{pt,on}$ density in $tr_{pbt}$ decreased slightly as $T_{IS,B}$ increased, whereas the large decrease in $I_{pt,on}$ was observed for the PFETs. This is because higher SCEs and $V_{th}$ reductions were observed in the NFETs, as the large amounts of diffused S/D dopants reduced $\Phi_b$ (Figures 2b and 5a). Therefore, in the NFETs, the $V_{th}$ reduction of $tr_{pbt}$ lowered the effects of the increase in $R_{sd}$, which was the dominant factor determining $S_{Ion,B}$. By contrast, in the PFETs, the $V_{th}$ reduction of $tr_{pbt}$ was small; thus, $I_{pt,on}$ decreased significantly owing to the increase in the $R_{sd}$ of $tr_{pbt}$. Consequently, $S_{Ion,B}$ was the smallest for the NFETs, but for the PFETs, the $T_{SD}$ variation caused $I_{on}$ to be most sensitive to $\Delta T_{IS,B}$.

Based on these results, we can provide two guidelines for controlling the DC performance variation, which depends on $T_{SD}$. In the case of $T_{SD} = 0$, precisely controlling $T_{IS,T}$ and $T_{IS,M}$ rather than $T_{IS,B}$ is effective for minimizing the variations in $I_{off}$ and $I_{on}$, as shown in Figures 3 and 6. However, considering the $T_{SD}$ variation, it is necessary to focus on the bottom inner spacer, because a precisely controlled $T_{IS,B}$ can considerably reduce the performance variation. Otherwise, the effects of $tr_{pbt}$ on the DC performance become large as $T_{IS,B}$ increases, resulting in the worst case with the highest $I_{off}$ and lowest $I_{on}$ in PFETs, which significantly diminishes the performance advantages of NSFETs.

The gate capacitance ($C_{gg}$) with respect to $\Delta T_{IS}$ for NSFETs ($T_{SD} = 0$) is shown in Figure 8, and $C_{gg}$ is decomposed into the intrinsic capacitance ($C_{int}$) and parasitic capaci-
ittance (C_{\text{para}}). C_{\text{para}} was extracted under the off-state bias, and C_{\text{int}} was calculated by subtracting C_{\text{para}} from C_{\text{gg}} under the on-state bias. As shown in Figure 8a, the differences in the C_{\text{gg}} sensitivity to T/M/B \Delta T_{\text{IS}} (S_{\text{Cgg}}) were small. However, the changes in C_{\text{int}} and C_{\text{para}} for each \Delta T_{\text{IS}} did not have the same sensitivity. C_{\text{para}}, which was determined by the fringing field between the gate and S/D, was affected by the T_{\text{IS}}. Therefore, the sensitivity of C_{\text{para}} to \Delta T_{\text{IS}} was almost identical among the T/M/B \Delta T_{\text{IS}} (Figure 8b). However, the sensitivity of C_{\text{int}} to \Delta T_{\text{IS,B}} was lower than those of \Delta T_{\text{IS,T}} and \Delta T_{\text{IS,M}} (Figure 8c). Although the inversion charge variations caused by \Delta T_{\text{IS,B}} mainly occurred in the bottom NS and PTS regions, the charge variations in the PTS region were smaller than those in the NS channels, leading to different AC sensitivities to the T/M/B \Delta T_{\text{IS}}. However, because the differences in the C_{\text{int}} sensitivity to the T/M/B \Delta T_{\text{IS}} were not large, it can be concluded that the overall performance sensitivity difference induced by each \Delta T_{\text{IS}} has greater effects on DC (I_{\text{off,T}}, I_{\text{off,M}}) rather than the AC performance.

![Figure 8](image_url)

**Figure 8.** (a) C_{\text{gg}}, (b) C_{\text{para}}, and (c) C_{\text{int}} for NFETs with respect to \Delta T_{\text{IS}} (T_{\text{SD}} = 0). The capacitances were extracted at a frequency of 1 MHz.

4. Conclusions

The sensitivities of the DC/AC performance to the T/M/B \Delta T_{\text{IS}} in sub-3-nm node NSFETs were quantitatively investigated using a fully calibrated TCAD simulation. The DC performance sensitivities (I_{\text{off,T}}, I_{\text{off,M}}) to the T/M/B \Delta T_{\text{IS}} differed. However, there were no significant differences in the AC sensitivities. One of the notable results was that \Delta T_{\text{IS}}, which varied the performance the most, was different according to the T_{\text{SD}} variations. In NSFETs with T_{\text{SD}} = 0 nm, S_{\text{off,B}} was lower than S_{\text{off,T}} and S_{\text{off,M}} because the effects of \Delta T_{\text{IS,B}} were primarily observed in the bottom NS channel. However, tr_{\text{pbt}} was no longer negligible when the T_{\text{SD}} was 5 nm. Thus, if the T_{\text{SD}} variation is not controlled, NFETs (PFETs) have higher S_{\text{off,B}} (S_{\text{Ion,B}}) because of the effects of tr_{\text{pbt}}. It can be concluded that
the bottom inner spacer is the element with the most significant effect on the DC/AC performance. Hence, reducing ΔTIS,B is important for yield enhancement.

**Author Contributions:** Conceptualization, S.L. (Sanguk Lee); methodology, S.L. (Sanguk Lee), J.-S.Y. and J.J.; formal analysis, S.L. (Sanguk Lee); investigation, S.L. (Sanguk Lee), J.J., S.L. (Seunghwan Lee) and J.L. (Junjoung Lee); writing—original draft preparation, S.L. (Sanguk Lee); writing—review and editing, J.-S.Y., J.J., S.L. (Seunghwan Lee), J.L. (Junjoung Lee) and J.L. (Jaewan Lim); supervision, J.J. and R.-H.B.; project administration, R.-H.B.; funding acquisition, R.-H.B. All authors have read and agreed to the published version of the manuscript.

**Funding:** This work was supported in part by POSTECH-Samsung Electronics Industry-Academia Cooperative Research Center; National Research Foundation of Korea (NRF) grant funded by the Korea Government (MSIT) (No. NRF-2022R1C1C1004925, NRF-2020M3F3A2A02082436, NRF-2020R1A4A0797777); MOTIE (Ministry of Trade, Industry & Energy) (No. 20019450, 20020265) and KRSC (Korea Semiconductor Research Consortium) support program for the development of the future semiconductor device and BK21 FOUR Program.

**Data Availability Statement:** Not applicable.

**Acknowledgments:** The EDA tool was supported by the IC Design Education Center, Korea.

**Conflicts of Interest:** The authors declare no conflict of interest.

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