Analysis and evaluation of noise coupling between through-silicon-vias

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Abstract Three-dimensional stacking of ICs with through-silicon-vias (TSVs) is one of the most expected way to integrate an enormous scale system in a small footprint. Shortened distance and expanded interconnect area are proofed to enable low-power, ultra-wide bandwidth communication among logic, memory, and analog component. In the 3-D integrated system with massive vertical interconnects, noise coupling among TSVs can be problem, by degrading signal integrity. We made a simple model to estimate noise coupling among TSVs and analyzed the coupling strength against parasitic capacitance of liner oxide. A test chip is fabricated, and the noise coupling strength is evaluated through on-chip waveform capturing circuitry. The analytical result and measured result show good consistency, and they indicate smaller size TSVs show better noise isolation characteristics as well as process simplicity.

Keywords: substrate noise, TSV, 3D-SIC, PDN, on-chip evaluation

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Three-dimensional stacked ICs (3D-SICs) with through-silicon-vias are known as a solution to realize high-density multi chip module on a small footprint and has been started to be used in several high-performance electronics [1, 2, 3, 4, 5, 6, 7].

Through-silicon-vias (TSVs), the biggest feature of 3D-SICs, enable vertical signal transfer among stacked ICs which enhances performance and energy by optimized signal lines between stacked ICs [8, 9, 10, 11, 12, 13].

Although wider signal bus is required for enormous scale data transfer, densely manufactured signal bus needs to solve crosstalk among the channels [14, 15, 16, 17, 18, 19, 20] as well as power line noise [21, 22, 23, 24, 25, 26, 27]. To avoid bit error caused by such crosstalk, it requires frequency or voltage optimization that cause additional issues like lower data transfer speed or larger power consumption, respectively [28, 29]. As for 3D-SICs, dominant factor of the crosstalk is liner oxide of TSVs, because of minimized metal routing of CMOS process and relatively larger size of TSVs.

We analyze relationship between crosstalk strength and TSV capacitance of liner oxide, using simple model consists of lumped components, and evaluate actual crosstalk strength on test chip with TSVs.

2. Simple model to explain TSV-TSV noise coupling

To consider TSV-TSV noise coupling, we created a simple model as shown in Fig. 1, including a couple of TSVs and buffers to drive them on a single-tier substrate. The two TSVs in the model act as an aggressor and a victim, which electrical nodes are depicted as TSV_A and TSV_V, respectively. We also defined substrate node as SUB in the diagram, which is at the center of two TSVs.

To simplify the crosstalk analysis, we divided the TSV-TSV coupling model into a TSV-substrate and a substrate-TSV couplings models. The SUB node is connected to TSVs through R_SUB of substrate resistance and C_SUB of capacitance of liner oxide. The SUB node is also biased with ground through R_GND of resistance between SUB and stabilized ground. In the analysis, the aggressor TSV is act as a signal source, and the victim TSV has dumping component of C_PDN and R_DRIV, from parasitic capacitance to V_PD and V_DS and resistance of R_DN of driver CMOS, respectively. In the case of TSV-substrate coupling, noise propagation ratio is explained as Eq. (1).

\[
\frac{V_{SUB}}{V_{TSV}} = \frac{R_{GND} / (R_{SUB} + 1/2\pi f C_{TSV} + R_{DRIV} / (1/2\pi f C_{PDM}))}{R_{SUB} + 1/2\pi f C_{TSV}}
\]

(1)

The parallel component of R_GND and Substrate-TSV coupling part is dominated by R_GND, due to enough high impedance of C_TSV (for example, about 1.6k Ohm in case of 100 IF of C_TSV at 1 GHz).

Hence, noise propagation ratio can be approximated as Eq. (2) in the case of TSV-substrate coupling.

\[
\frac{V_{SUB}}{V_{TSV,A}} \cong \frac{R_{GND}}{R_{SUB} + 1/2\pi f C_{TSV}}
\]

(2)

The noise propagation ratio is explained with amplitude in TSVs, V_TSV,A and V_TSV,V, is modeled as voltage division between TSV_A to SUB and SUB to ground impedance. From the equation, we can see C_TSV and R_GND are dominant factor of noise propagation ratio from TSV to substrate. The substrate to TSV noise propagation ratio can be also explained with the simplified model, as Eq. (3).

\[
\frac{V_{TSV,V}}{V_{SUB}} = \frac{R_{DRIV} / (1/2\pi f C_{PDM})}{R_{SUB} + 1/2\pi f C_{TSV}}
\]

(3)
The noise propagation ratio consists of $R_{DRIV}$ and $C_{PDN}$, in addition to $R_{SUB}$ and $C_{TSV}$.

Figs. 2(a) and (b) shows analytical result of the noise coupling ratio of from aggressor TSV to substrate and from substrate to victim TSV, respectively. In this analysis, 800 fF of $C_{PDN}$, 3k Ohm of $R_{DRIV}$, 10 Ohm of $R_{SUB}$, and 100 Ohm of $R_{GND}$ are set according to a test chip design that mentioned in next section. The red dot in the graph shows coupling ratio with 28 fF of $C_{TSV}$ in the test chip, including capacitance of liner oxide around Cu plug with 5μm of diameter and 20 μm of length and capacitance of M1 pad connected to TSV. The frequency in the analysis is set to 400 MHz, according to measured fall time of the signal in the aggressor TSV. As these graphs show, the coupling strengths monotonically increase as $C_{TSV}$ increases, because of large contribution of $C_{TSV}$ in the Eq.(2) and (3) around this frequency bandwidth. Due to small size as a via-last TSV, our TSV shows 0.0070 and 0.034 of the aggressor TSV to Si substrate and the Si substrate to victim TSV noise propagation ratio, respectively. These propagation ratios suggest that -72 dBV noise suppression in the case of single couple of TSVs. From the Eq. (3), although larger $C_{PDN}$ is alternative idea to suppress noise propagation, high power consumption and increased powerline noise may cause performance
degradation in total.

3. Measurement

Fig. 3 shows structure of our test chip to measure TSV-TSV noise propagation. The test chip is designed and manufactured by 0.18 μm CMOS process. After the CMOS process completion, the wafer is flipped and thinned down to 20 μm Si thickness for TSV formation. A diameter of conductor Cu is 5 μm and liner SiO2 thickness is 0.5 μm.

Fig. 3 (a) shows cross-sectional structure of the test chip, including thinned CMOS chip with TSVs mounted on support Si tier with die attach film. This test structure is same as the model structure depicted in Fig. 1. A photo after chip-on-board integration is shown in Fig. 3(b). Fig. 3(c) depicts physical layout design around evaluation circuitry. The evaluation circuitry consists of waveform capturing circuitry [30], evaluation area with two TSVs, and drivers for the aggressor and the victim TSV. The waveform capturing circuitry consists of sample-hold and output buffer, to capture pulse waveform in the aggressor TSV, noise on Si substrate between two TSVs, and noise in the victim TSV.

Fig. 4 shows captured waveforms from embedded waveform capturer. The timing resolution of the measurement is 0.05 ns, and the plot is average of 16 waveforms for minimizing environmental noise from off-chip. A red and blue lines in Fig. 4(a) shows signal voltage in the aggressor TSV, captured by two types of waveform capturer that targets $V_{DD}$ level and $V_{SS}$ level, respectively. The fall time of signal in the aggressor TSV is measured as the time from 90 to 10% of voltage swing between $V_H$ and $V_L$. Figure 4(b) shows substrate noise of - 9 mV peak, exited by voltage swing in aggressor TSV. A red dotted line and a blue line in Fig. 4(c) show measured row waveform and filtered waveform in victim TSV. In this graph, simple moving average (SMA) filter is applied with $n=9$ as lowpass filter (LPF), to see small voltage swing without background noise. As for about 1 mV peak-peak voltage swing in victim TSV, it is considered to be noise induced to victim TSV driver from aggressor TSV driver through substrate between the drivers, due to opposite direction of substrate noise between TSVs and larger noise propagation ratio than expected ratio in analysis.

From these results and consideration, we can say measured noise in the victim TSV is enough small to be hidden with other noise. Absence of the noise propagation from aggressor TSV to victim TSV is consistent with expectation from analysis, as well as substrate noise in Fig. 4(b) with comparable voltage variation to $1.72 \text{ V} \times 0.007$ from analysis.

4. Conclusion

In 3D-SICs with dense interconnects through TSVs, crosstalk among TSVs may degrade signal integrity, due to large coupling factor consists of capacitance of liner oxide. This paper constructed simple lumped component model to explain TSV to TSV noise propagation, and fabricated test chip including TSVs on 0.18 μm CMOS. The analytical model focus on a couple of aggressor and victim TSVs, to simplify the target structure, and test chip is designed to measure noise propagation among TSVs with mitigated effect from structures without TSVs with on-chip measurement technology. The analytical and measured result suggests that smaller TSV capacitance suppresses both TSV to substrate and substrate to TSV coupling.

This consideration suggests that small TSVs are worth the risk of handling extremely thinned wafer, by noise suppres-
sion as well as shortened etching process and electroplating process of TSVs. The presented equations also suggest that reduction of substrate resistance to ground has large effect if TSV driver has small parasitic capacitance or large capacitance of liner oxide around TSVs.

The constructed model is extendable by multiplying values in the equations when number of TSVs increased, and further measurement with enormous number of TSVs for process and design co-optimization in high-performance stacked module. These are left for future studies.

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