F-Shaped Tunnel Field-Effect Transistor (TFET) for the Low-Power Application

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Abstract: In this report, a novel tunnel field-effect transistor (TFET) named ‘F-shaped TFET’ has been proposed and its electrical characteristics are analyzed and optimized by using a computer-aided design simulation. It features ultra-thin and a highly doped source surrounded by lightly doped regions. As a result, it is compared to an L-shaped TFET, which is a motivation of this work, the F-shaped TFET can lower turn-on voltage ($V_{\text{ON}}$) maintaining high on-state current ($I_{\text{ON}}$) and low subthreshold swing ($SS$) with the help of electric field crowding effects. The optimized F-shaped TFET shows 0.4 V lower $V_{\text{ON}}$ than the L-shaped TFET with the same design parameter. In addition, it shows 4.8 times higher $I_{\text{ON}}$ and 7 mV/dec smaller average $SS$ with the same $V_{\text{ON}}$ as that for L-shaped TFET.

Keywords: band-to-band tunneling; tunnel field-effect transistor (TFET); L-shaped TFET; line tunneling; electric field crowding; corner effect

1. Introduction

Tunnel field-effect transistor (TFET) has been regarded as a promising candidate to replace the metal-oxide-semiconductor FET (MOSFET) for a low power device because its subthreshold swing (SS) can be scaled less than 60 mV/dec [1–8]. However, Si-based TFET suffers from low-level on-state current ($I_{\text{ON}}$) due to its limited band-to-band tunneling (BTBT) rate. Furthermore, there are just a few reports which have demonstrated sub-60 mV/dec SS with the experimental devices. Several strategies have been proposed to address these issues [9–19]. Among them, L-shaped TFET has efficiently improved $I_{\text{ON}}$ and SS by increasing BTBT junction area and by decreasing BTBT barrier width ($W_{\text{TUN}}$) with the help of a novel structure [20]. In spite of these advantages, there is a drawback that turn-on voltage ($V_{\text{ON}}$), which is defined as gate voltage ($V_{\text{GS}}$) when BTBT starts to occur, becomes much higher than conventional TFET. It is contradictory to apply the low-power logic elements [21,22]. Therefore, in this manuscript, a new-structure TFET is proposed to address the technical issue of L-shaped TFET maintaining its advantages. Figure 1a shows a schematic structure of proposed device named ‘F-shaped TFET’ because the shape of source is similar to the fingers. It resembles an L-shaped TFET except the ultra-thin sources which are surrounded by intrinsic (or lightly doped) Si regions [20]. It is expected that the F-shaped TFET can reduce $V_{\text{ON}}$ with the help of electric field crowding effect as the thickness of source ($T_{\text{S}}$) gets thinner. In order to examine the electrical characteristics of F-shaped TFET, technology computer-aided design (TCAD) simulation is performed [23]. Nonlocal BTBT, Shockley–Read–Hall
recombination, bandgap narrowing, and concentration-dependent mobility models are considered for an accurate examination. Table 1 shows the parameters used for the simulation. Gate length ($L_G$) is set by 20 nm and drain regions are lightly doped to suppress ambipolar behavior.

This manuscript is composed as follows. First, the electrical performance of the F-shaped TFET with a single-source region (i.e., one finger) is examined (Figure 1b). Many parameters such as $T_S$, lateral length of tunnel region ($L_T$), and space above and below source ($T_E$) have been set as variables. In Section 2, the influences of $T_S$, $L_T$, and $T_E$ have been discussed. In Section 3, feasibility for the better performance with F-shaped TFET is examined by adding one more source region (i.e., two fingers) and its design is optimized by adjusting the distance between two source regions ($T_I$). In Section 4, the optimized design is compared with the conventional L-shaped TFET. In Section 5, an exemplary process flow for the fabrication of F-shaped TFET is proposed.

2. Influences of Design Parameters

2.1. Length of Tunnel Region ($L_T$)

Figure 2 shows transfer characteristics as $L_T$ changes from 10 to 2 nm. It shows that $V_{ON}$ increases as $L_T$ decreases. This is explained by the surface potential depending on $L_T$ with the help of the voltage division model in series-connected capacitors [24]. In detail, if $L_T$ decreases, the surface potential at the fixed $V_{GS}$ is reduced because the capacitance of the fully depleted Si tunnel region increases; results in
a high $V_{ON}$. On the other hand, the average $SS$ ($SS_{AVG}$) decreases if $L_T$ decreases (Figure 2 and its inset). It is attributed to the smaller $W_{TUN}$ (at $V_{GS} = V_{ON}$) with the smaller $L_T$ [24]. Similarly, $I_{on}$ increases as $L_T$ decreases, because the $W_{TUN}$ at on-state decreases. The optimum $L_T$ is determined as 4 nm, since the increase of $V_{ON}$ is significant while the reduction of $SS_{AVG}$ is negligible as $L_T$ becomes less than 4 nm (inset of Figure 2).

![Figure 2](image)

**Figure 2.** Log scale transfer characteristics with various $L_T$ at 0.7 V-drain voltage ($V_{DS}$). The inset figure shows turn-on voltage ($V_{ON}$) and average $SS$ ($SS_{AVG}$) which is extracted by measuring $SS$ from $V_{ON}$ to $V_{ON} + 0.7$ V.

### 2.2. Source Thickness ($T_S$)

Figure 3a shows transfer characteristics depending on $T_S$. The drain current ($I_D$) is normalized by $T_S$ to exclude the influence of $T_S$ on the BTBT junction area and on the magnitude of $I_D$. There are two noteworthy points in terms of $I_{ON}$ and $V_{ON}$ as shown in the inset of Figure 3a. Both results can be analyzed by electric field contour plots shown in Figure 3b–f. As shown in Figure 3b, electric field at sharp source corner ($E_{COR}$) is much larger than that for flat source region ($E_{FLAT}$) due to field crowding effect [25]. Because $V_{ON}$ and $I_{ON}$ of TFETs sensitively depend on electric field at source-to-channel junction, the source corner and the flat source regions can be regarded as different TFETs; $FET_{COR}$ and $FET_{FLAT}$. In other words, F-shaped TFET can be regarded as $FET_{COR}$ and $FET_{FLAT}$ connected in parallel as shown in Figure 3g. If $T_S$ decreases, the $FET_{COR}$ contributes more to $I_D$ than $FET_{FLAT}$. As a result, the normalized $I_D$ by $T_S$ is increased because $FET_{COR}$ has higher current than $FET_{FLAT}$.

Unlike to $I_{ON}$, $V_{ON}$ is solely determined by $FET_{COR}$ which is turned on first. Although $T_S$ decreases (i.e., the portion of $FET_{COR}$ increases), the $E_{COR}$ is unchanged. Therefore, $V_{ON}$ is not affected by $T_S$ from 40 to 10 nm (Figure 3b–d). On the other hand, if $T_S$ becomes less than 10 nm, $FET_{FLAT}$ is completely disappeared and $FET_{COR}$ at two corners starts to be merged (Figure 3e,f). As a result, the magnitude of electric field is increased further and $V_{ON}$ starts to be decreased. Considering process capability, $T_S$ is optimized as 5 nm.
Figure 3. (a) Normalized log scale transfer characteristics with various $T_S$ at $V_{DS} = 0.7$ V. The inset figure shows $V_{ON}$ and normalized on-state current ($I_{ON}$) which is defined as $I_D$ at $V_{GS} = 0.5 + V_{ON}$ divided by $T_S$. Electric field contour plots for (b) $T_S = 40$ nm, (c) $T_S = 15$ nm, (d) $T_S = 10$ nm, (e) $T_S = 7.5$ nm, and (f) $T_S = 5$ nm. These plots are extracted at $V_{DS} = 0.7$ V and $V_{GS} = 0.86$ V which is corresponded to the $V_{ON}$ of $T_S = 40$ nm. (g) Schematic circuit model for F-shaped TFET.
2.3. Space Above and Below Source (\(T_E\))

As discussed in Figure 1, unlike the L-shaped TFET, the source of the F-shaped TFET is surrounded by lightly doped Si regions. Therefore, it is worthwhile to study about the influence of \(T_E\) on electrical characteristics of F-shaped TFET because it can influence on electric field crowding. As shown in Figure 4, the \(V_{ON}\) slightly decreases as the \(T_E\) increases due to the increase of electric field crowding effect. In other word, the number of electric field flux is increased since the tunnel junction is affected by the larger gate area. Consequently, band bending at tunnel junction becomes abrupt, and hence decreases \(V_{ON}\). However, large \(T_E\) is contradictory to the process capability (i.e., abrupt etching profile). In addition, if \(T_E\) increases more than 15 nm, the decrease of \(V_{ON}\) is negligible as shown in the inset of Figure 4. Based on the above results, \(T_E\) is optimized as 15 nm.

![Figure 4](image)

*Figure 4.* Transfer characteristic with the various \(T_E\) at \(V_{DS} = 0.7\) V. The inset figure shows extracted \(V_{ON}\) with the variation of \(T_E\) ranging from 5 to 30 nm.

3. Optimized F-Shaped TFET

In Section 2, the parameters (\(T_S, L_T, T_E\)) which can influence on the electric field crowding effect have been optimized by several simulations. Although F-shaped TFET can achieve the higher normalized \(I_D\) (i.e., current density) as \(T_S\) decreases, the smaller BTBT junction area is problematic in terms of total current for its real application. It can be addressed by adding an additional source (i.e., figure) as shown in Figure 5a. From the previous results in Section 2.3, it can be expected that the electrical characteristic of F-shaped TFET with multiple source regions is sensitively affected by the distance between the two sources (\(T_I\)). Therefore, the influences of \(T_I\) on the electrical performance of F-shaped TFET are investigated to determine an optimum \(T_I\). Figure 5b,c shows the effect of \(T_I\) on the magnitude of the electric field at source-to-channel junction. If \(T_I\) gets smaller, the electric field of both sources start to become merged and each electric field at tunnel junction is decreased. As a result, \(V_{ON}\) is increased as shown in Figure 5d and its inset. The result is well corresponded to the phenomena discussed in Section 2.3. Considering the process capability and the influence of \(T_I\) on the electrical performance, \(T_I\) is optimized as 30 nm.
Figure 5. (a) Structure of F-shaped TFET with multiple sources. Electric field contour plots for (b) $T_I = 30$ nm and for (c) $T_I = 5$ nm at $V_{DS} = 0.7$ V, $V_{GS} = 0.86$ V. (d) Transfer characteristic as $T_I$ increases from 2 to 50 nm at $V_{DS} = 0.7$ V. The inset figure shows extracted $V_{ON}$. 
4. Comparison with L-Shaped TFET

Figure 6a shows a schematic structure of L-shaped TFET studied in [24]. Most of design parameters such as $L_G$, $T_{OX}$, $N_S$, $N_D$, $N_B$, $W_{FN}$ and $W$ are the same as that for the F-shaped TFET. In case of L-shaped TFET, $T_S$ is set by 70 nm which is the same as $T_G$ in optimized F-shaped TFET; $T_S = 5$ nm, $T_E = 15$ nm, and $T_I = 30$ nm, $T_G = 2T_S + 2T_E + T_I$ (Figure 5a). On the other hand, $L_T$ is set as 4 nm or 6 nm to compare with F-shaped TFET in two points of view; the same dimension or $V_{ON}$.

In case of 4 nm-$L_T$, L-shaped TFET has the same dimension as the optimized F-shaped TFET discussed in Section 2.1. As shown in Figure 6b, it is clear that the $V_{ON}$ of F-shaped TFET is about 0.4 V lower than that for L-shaped TFET in spite of the same dimension with the help of the electric field crowding effect. The inset of Figure 6b confirms that $V_{ON}$ of F-shaped TFET is always smaller than that for L-shaped TFET with the same $L_T$. 

**Figure 6.** (a) Structure of L-shaped TFET. (b) Transfer characteristics of L-shaped and F-shaped TFETs at $V_{DS} = 0.7$ V. The inset figure shows $V_{ON}$ of both TFETs as a function of $L_T$ from 2 to 8 nm.
If the $L_T$ of L-shaped TFET is 6 nm, its $V_{ON}$ becomes the same as that of an optimized F-shaped TFET (Figure 6b). Comparing both TFETs with the same $V_{ON}$, the $I_{ON}$, and $SS_{AVG}$ of F-shaped TFET are 4.8 times higher and 7 mV/dec lower than that for L-shaped TFET, respectively. The results are clearly attributed to the enhanced BTBT rate with the geometrical merits (i.e., field crowding), because F-shaped TFET has smaller BTBT junction area than L-shaped TFET.

5. Device Fabrication

Figure 7 summarizes an exemplary self-align process flow for F-shaped TFET with multiple source regions; fingers. (Figure 7a) P-type Si layers doped by $10^{20}$ cm$^{-3}$ and $10^{15}$ cm$^{-3}$ are alternately stacked on Si-on-insulator (SOI) wafer through epitaxial layer growth processes. After defining an active region, SiO$_2$ hard-mask is deposited by a chemical vapor deposition (CVD). This layer is also helpful to passivate active sidewall. (Figure 7b) Mesa patterning is followed by SiO$_2$ buffer layer deposition. (Figure 7c) After dummy gate formation by deposition and etch-back processes, drain region is defined by arsenic (As) ion implantation and rapid thermal annealing (RTA). (Figure 7d) SiO$_2$ deposition is followed by chemical-mechanical polishing (CMP) to expose the dummy gate. (Figure 7e) After selectively removing the dummy gate and SiO$_2$ buffer layer, selective epitaxial layer growth (SEG) is performed to form ultra-thin tunnel region. (Figure 7f) The gate stack is formed by high-k/metal gate atomic layer deposition (ALD) processes. The back-end-of-line process is not shown here.

6. Summary

A novel F-shaped TFET is proposed and its device physics and operating mechanisms are studied in detail by using two-dimensional TCAD simulations. The results confirm that it can achieve a relatively lower $V_{ON}$ (~0.6 V) than that for L-shaped TFET (~1.0 V) with the same $L_T$. In addition, the current drivability of F-shaped TFET can be further improved by adding additional sources (fingers). Last of all, F-shaped TFET is expected to be fabricated by self-aligned processes. Therefore, F-shaped TFET can be regarded as one of the promising candidates for low-power digital logic applications.
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