Charge Crowding in Graphene-Silicon Diodes

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ABSTRACT—The performance of nanoscale electronic devices based on a two-three dimensional (2D-3D) interface is significantly affected by the electrical contacts that interconnect these materials with external circuitry. This work investigates charge transport effects at the 2D-3D ohmic contact coupled with the thermionic injection model for graphene/Si Schottky junction. Here, we focus on the intrinsic properties of graphene-metal contacts, paying particular attention to the nature of the contact failure mechanism under high electrical stress. According to our findings, severe current crowding (CC) effects in highly conductive electrical contact significantly affect device failure that can be reduced by spatially varying the contact properties and geometry. The impact of electrical breakdown on material degradation is systematically analyzed by atomic force, Raman, scanning electron, and energy dispersive X-ray spectroscopies. Our devices withstand high electrostatic discharge spikes over a longer period, manifesting high robustness and operational stability. This research paves the way towards a highly robust and reliable graphene/Si heterostructure in futuristic on-chip integration in dynamic switching. The methods we employed here can be extended for other nanoscale electronic devices based on 2D-3D interfaces.

Index Terms— Graphene/Silicon (Gr/Si) heterostructure, Electrostatic Discharge (ESD), Transmission Line Pulse (TLP), Breakdown Voltage (Vbd).

I. INTRODUCTION

Vast multidisciplinary applications of graphene have promoted enormous developments and made breakthroughs in the high-tech fields. The extraordinary potential of graphene lies in its remarkable thermal conductivity [1] dangling bond-free interfaces, efficient charge transfer [2] high electron mobility [3], [4] chemical resilience [5], [6] high-temperature sustainability [7] and broadband optical absorption and sensing [8], [9] which make it an ideal material for high-performance electronics and optoelectronics.

However, the main physical limitation of graphene lies in the weak interface contact between graphene and metal electrode [10] which results in excessive heat generation, the creation of local hot spots [11] electromigrations [12] and consequently compromising the lifetime and reliability of the device [13]. One of the critical factors limiting the performance, robustness, and durability of electronic devices through electrical conduction is the current crowding (CC) effect, defined as an inhomogeneous distribution of current density at two dissimilar highly conductive contacts [10], [14]–[24]. Numerous researches have demonstrated the CC effects in 2D materials, e.g., MoS2 or graphene [25]–[27] with different strategies to reduce the CC effect and improve the current transport in the electrical contact [28]–[30]. Understanding the 2D-3D contact failure mechanism is critical for the real future application of 2D-3D heterostructure devices.

The 2D-3D Schottky junctions require special attention to understand how they differ from traditional metal-semiconductor Schottky and the key benefit of using a 2D heterostructure (graphene) as an alternative of metal. Typically, metal-based electronic devices suffer from high noise, Fermi level pinning, non-ideal interfaces, large surface, and trapping sites limiting efficient charge transfer between metal and semiconductor [31], [32]. The Gr/Si Schottky junction has been reported as fast and highly responsive photodiodes with broadband and high sensing applications [33], [34]. However, the impact of inherent time-dependent instabilities in the charge transport at the 2D-3D interface (graphene-metal/SiO2/Si) demands special consideration. The weak 2D-3D contacts (graphene-metal) [35] remarkably deteriorate the performance of graphene-based electronic devices. Graphene is highly sensitive to the environment due to its 2D nature and is strongly influenced by metal contacts. The electrical properties of graphene can be tuned when in contact with different metals such as Pt, Au, and Cu [36]. The charge loses a fraction of energy as phonon vibrations, causing scattering in the lattice and raising the material temperature [37]. The non-uniform distribution of the carriers across the graphene-metal contacts forms thermal hot spots, deteriorating device performance and causing material failure [38].
II. EXPERIMENTAL METHOD AND MEASUREMENTS

The Gr/Si Schottky devices are fabricated on a low doped n-type Si wafer with a 300 nm, 100 nm and 18 nm thick SiO$_2$ layer. Au/Ti (70/10, 60/10 and 40/10 nm) electrodes are patterned by the 1st lithography followed by e-beam evaporation and lift-off. In the 2nd lithography, the Si window is exposed, and the wafer is immersed into buffered oxide etchant to remove the oxide layer. Then, graphene is chemically transferred onto the Si window to form a Schottky junction. Finally, the 3rd lithography and O$_2$ plasma remove residues on the surface. A metallic Ohmic contact is formed on the backside of the Si substrate. We used a TLP tester (Barth pulse curve tracer semiconductor analyzer, model 4002) with short ESD pulses (100 ns pulse widths and 10 ns rise times) for the Electrostatic testing. SEM and XRD images were obtained using a Hitachi S4800 field emission microscope at an acceleration voltage of 5 kV. A confocal Raman microscope (Senterra, Bruker) and a Renishaw Invia with a 532 nm excitation wavelength were used to measure Raman spectroscopy.

III. RESULTS AND DISCUSSION

This work employs Gr/Si Schottky junction to signify the charge transport at the 2D-3D contact under high electrical stress. The 3D schematic of the Gr/Si Schottky junction is presented in Fig. 1(a). The surface roughness model consists of four regions, graphene-metal lateral and edge contact ($R_{G,M}$), suspended graphene region ($R_{G-SiO_2}$), and Gr/Si ($R_{G-Si}$) interface to measure the surface roughness shown in Fig. 1(b). The low density of state (DOS) close to the Dirac point limits the charge injection from metal to graphene. The amount of charge transport across the metal-graphene interface is controlled by the work functions and contact resistance presented in Fig. 1(c). The current-voltage characteristics of the Gr/Si Schottky diode showed rectification behavior with ideality factor ($\eta = 1.1$) and series resistance ($R_s = 480 \ \Omega$) calculated by Cheung’s method (Fig. 1(d)) [39]. Reducing the contact roughness to minimize the contact resistance will improve the device charge transport and reliability. The influence of contact, surface morphology and roughness of the 2D-3D interface of the intrinsic Gr/Si junction is exhibited through AFM and SEM, as shown in Fig. 1(e) and Fig. 1(f). The AFM images with the different roughness of the junctions between dissimilar materials composed of roughness at graphene-metal ($R_{G,M}$) = $\sim 4$ nm (lateral), $\sim 35$ nm (edge site), RG-SiO$_2$ = $\sim 10$ nm, and $R_{G-Si}$ = $\sim 3$ nm for18 nm thick oxide layer.

![Fig. 1](image_url)

Fig. 1. (a) 3D schematic of CVD Gr/Si Schottky diode. (b) The cross-section image shows the effect of charge injection at graphene-metal, Gr-SiO$_2$ contact (insufficient for a heat sink) and Gr/Si (heat transfer to the substrate). (c) Energy band diagram of metal–graphene contact (The Fermi levels are aligned and show a charge transfer mechanism at the graphene-metal interface). (d) Static I-V characteristic (e) AFM morphological between dissimilar materials Gr/Au (lateral and edge), Gr/SiO$_2$ (edge), and Gr/Si are showing the surface roughness at four different sites. (f) SEM image of the device structure.

IV. ELECTROSTATIC DISCHARGE (ESD) FAILURE MECHANISMS OF GRAPHENE-SI DIODE

The 2D-3D contact, like graphene-metal contact, suffers from interfacial defects and weak contact, compromising the current carrying capability and switching speed of the device. When the excessive heat energy is not dissipated properly, it can lead to the device breakdown that creates permanent damage to the material [38, 40–43].
A part of the excess energy gained by electrons from an external source (e.g., an electrical bias) is transferred to the lattice via phonon emission, increasing the lattice temperature due to Joule heating. Therefore, heat mitigation is an essential factor that significantly impacts the graphene-based structure, where 2D materials demand extensive heat sink contact with the underlying substrate. Here, we experimentally investigated the influence of Joule heating that is caused by the CC effect in 2D-3D contacts. AFM morphological roughness measurements at graphene-metal (lateral and edge site), Gr/SiO$_2$ and Gr/Si for 100 and 300 nm thick oxide layer are presented in Fig. 2(a) and Fig. 2(b). The AFM result reveals the prevailing roughness distribution at the edge contacts. It confirms that lowering these thicknesses minimize interface gaps, reduce the roughness of edge contacts and improve the charge transport. Moreover, we perform thermal annealing to smooth the gold surface as a result shows low edge roughness, which significantly improves thermal mitigation. The larger gaps at the interfaces also stretch the graphene laid on the contact and substrate, producing more wrinkles enhance phonon vibration resulting in earlier device failure for the thicker oxide layer.

We executed a TLP testing with a sharp rising time (10 ns) and pulse width (100 ns). The TLP test is suitable for ensuring device reliability and stability under ESD stress [44]. The excess heat caused by graphene electrons cannot be dissipated effectively through the thicker oxide resulting in a temperature rise and enhanced electron-phonon scattering. A thick oxide layer creates a large area of suspended graphene that has no direct contact with the solid surface, which serves as an inefficient heat sink. Therefore, suspended graphene is easy to heat up to high temperature under high electrical stress and gets damaged earlier than graphene with contact with a solid substrate. As a result, the transferred heat can quickly spread and provide a better heat sink, suggesting efficient heat mitigation for thinner oxide [45], [46].

The TLP results verify that a thinner oxide layer reduces surface roughness and contact resistance, consequently increasing the graphene-substrate contact area to improve the electron transportation and heat mitigation, resulting in extended device breakdown voltage and significantly enhance the current density, as shown in Fig. 2 (c). Intrinsically, the Gr/Si Schottky junction possesses a low dark current in reverse mode and a high on/off ratio, applicability as a fast Gr/Si Schottky diode.
The reverse bias TLP testing justifies the low leakage current resulting in large breakdown voltage, demonstrating the device ability to bear high-amplitude ESD spikes in Fig. 2(d). We performed a repetitive TLP test (70 times) on the same device to investigate the repeatability and explore any evident changes in the I-V characteristic due to electrical stress. As a result, the I-V characteristic did not deviate, demonstrating Gr/Si junction is robust enough (Fig. 2(e)). The possible charge movement, CC effect, the high current density at 2D-3D contact, and their impact on the time-dependent dynamics are directly dependent upon the junction area of the device. A device with a smaller junction exhibits lower breakdown voltages than that with a larger junction due to the high current density. In Fig. 2(f) increasing the Gr/Si junction area from 0.1 × 0.1, 0.3 × 0.3, to 0.5 × 0.5 mm² significantly pushing the high forward breakdown voltage (V_{BD}) as illustrated in Fig. 2(f) inset.

The excessive charge movement across the junction introduces a heating effect along the graphene channel. It is observed that the heat is appropriately mitigated, where graphene is laterally contacted with metal and substrate. The graphene near the edge contacts appears to be more resistive, less efficient at managing heat, and prone to device failure. The stress accumulation and defect generation are more severe at high ESD, which produces hot spots and localized heating at contact corners due to field crowding [47]. Furthermore, as electrical stress increases, cracks/defects grow further, melting the metal electrode and causing device breakdown (from soft to hard), as presented in Fig. 3(b-g). Fig. 3(h) shows a complete breakdown at 26 V, with no conductive path available for graphene on Si to contact the Au electrode for the further utility of the Gr/Si junction. By carefully monitoring the visuals, the failure region was detected at Gr/Au and Gr/SiO₂ edges but had a minor impact on the Gr/Si junction.

Furthermore, we performed the SEM of three different functional regions of the device to determine the exact graphene degradation sites leading to device failure, as presented in Fig. 4(a) and Fig. 4(b). Raman spectroscopy is an appropriate characterization tool for evaluating the atomic disorder of the material[48]–[51]. We spectroscopically measure 10 spots that encompass the Gr/Au (1,2), Gr/SiO₂ (3-6), and Gr/Si (7-10) to probe the material degradation under high electrical stress. In Fig. 4(a) at position (1-10), the Raman spectra demonstrated an excellent sp² hybridized monolayer graphene with high (I_D/I_G > 2) and low (I_S/I_G < 1) peak ratios. The D band corresponds to scattering from local defects or disorders present in carbon, and the G band originates from the in-plane tangential stretching of the C–C bonds in the graphitic structure [52].

The catastrophic effect of electrical breakdown occurs under high electrical stress, demonstrated in Fig. 4(b). Our result indicates that failure occurs due to excessive phonon vibrations resulting in C-C bond breaking that finally electrically disconnects the graphene in the device. The Raman spectra of the areas from 3 to 6 conclude that extensive current activity boosted the edge contact heating effects, leading to material failure. At the positions (7,8) from the SEM in Fig. 4(b), the 2D peak appears at 2690 cm⁻¹ with an emerging D’ adjacent to a high D peak at (1620/1350 cm⁻¹), owing to graphene self-roll.
(folded) at after covalent bond breaking [53]. In contrast, graphene retains its continuity and symmetry at the Gr/Si junction, as represented by positions 9 and 10.

Moreover, we examined the role of graphene nanoribbons (GNRs) in interaction with a substrate under high electrical stress. The GNRs exhibit remarkable electrical and optical properties, and numerous studies highlight the innovative characteristic of advanced nanotechnology [54]–[57]. Fig. 5(a) and Fig. 5(b) demonstrate static IV characterization and pre-failure SEM images of GNRs device. Fig. 5(c) shows the Raman spectra of pristine GNRs, with a low D-peak at 1340 cm\(^{-1}\), G peak at 1580 cm\(^{-1}\), and a 2D peak at 2680 cm\(^{-1}\) as the \(I_{2D}/I_G>2\) and \(I_D/I_G<1\) peak intensity ratios. The D peak is not observable in pristine graphene because of crystal symmetries [58]. Several studies have demonstrated different densities of defects in graphene ribbons, including symmetry-breaking, disorder, crystal alignment, lattice, and edge defects that can limit the device performance [55], [59]–[66].

In Fig. 4(d-f), Raman mapping shows significantly high defect density at the edge contact, enhancing the charge crowding, excessive phonon vibrations at high current density, and C-C bond breaking at Gr/Au and Gr/SiO\(_2\) edge contact (Fig. 4 (g-i)). Finally, the energy dispersive X-ray (EDX) spectroscopy approach is used for qualitative materials analysis with the elemental composition at points 1-10 of the device before and after the breakdown in Fig. 4(a) and Fig. 4(b). In Fig. 4(c), the elemental compositions of all associated components in the device, such as carbon C, oxygen O, and Si, are shown in percentages versus points 1-10. The graphene was ruptured at the edge contact (points 3-6), reducing carbon atoms, as evidenced by EDX spot mapping. The decrease of C and increase of O percentages correspond to C-C covalent bond breaking at Gr/SiO\(_2\) areas.

![Graphene-Silicon Raman Spectra](image)

**Fig. 4.** SEM images and Raman spectra of Gr/Au, Gr/SiO\(_2\) and Gr/Si contacts (a) before and (b) after breakdown, respectively. The D and D' peaks, indicative of disorder, increase and become more prominent with increased electrical stress. Conversely, the D, G, and 2D peaks weaken, and graphene ruptures at the edge contact (points 3-6), reducing carbon atoms after an electrical breakdown. (c) EDX data of C/Au/Ti, O, and Si elements in (a) and (b). (Note: SEM images in (a) and (b) with point distributions across the three regions of Gr/Au (positions of 1-2), Gr/SiO\(_2\) (positions of 3-6), and Gr/Si (positions of 7-10). (d-i) Raman mapping at ~1340 cm\(^{-1}\) (D-band), ~1580 cm\(^{-1}\) (G-band), ~2680 cm\(^{-1}\) (2D-band) before and after breakdown.

![Device Structure](image)

**Fig. 5.** (a) Static IV characterization. (b) SEM images. (c) Raman spectroscopy of Graphene-Silicon Schottky ribbon device at different points.

However, there has been limited research into how the density of defects influences GNRs properties under high electrical stress. The electrical charge injection generates thermal heat and produces phonon scatters, significantly affecting the Gr/Si junction. Raman spectroscopy uses to quantitatively identify the defects in the graphene ribbons by observing D, G, 2D, D', and \(I_D/I_G\) peak intensity ratios.
In a symmetry-breaking with a high D-band peak, a charge carrier must be excited and inelastically scattered by a phonon (the D-band denoting disorder-induced). As the amount of disorder in graphene increases, the Raman intensity increases for the different disorder peaks D (1350 cm⁻¹), which scatters from K to K' (internally); D' (1620 cm⁻¹), which scatters from K to K (intravalley) [67]. It has been reported that the ratio of D, I_D/I_G and I_D'/I_G intensity can be used to discriminate the disorder, sp³ and vacancy-type defects in graphene-based devices [50], [68]. Fig. 6(a) shows a forward breakdown of the GNRs device under high electrical stress. The SEM images and Raman spectra in Fig. 6(b) and Fig. 6(c) show high D, D', and large I_D/I_G > 2 peak ratio, revealing a higher defect density, breaking the C-C symmetry, and more phonon dispersion after electrical stress breakdown. The GNRs that suffer higher charge crowding is less efficient for heat management, leading to phonon scattering and potentially damaging the Schottky junction, as presented in Fig. 6(b) and Fig. 6(c). The GNRs have sharp and distinct uniform boundaries before electrical stress breakdown (Fig. 6(d-f)). The sharp GNRs changed into non-uniform and irregular termination at edges resulting from the disruption of GNR due to electrical stress.

Fig. 6. (a) TLP forward breakdown of Gr/Si Schottky diode with GNR (b), (c) Post-failure S.E.M. images show that higher defect density creates more phonon dispersion after electrical stress. (d) The evolution of D, G, and 2D peaks was observed, and Raman peak intensity ratios of the D, D', and I_D/I_G ratio increased after an electrical breakdown. Note: The higher D, D', and I_D/I_G indicate the formation of more defects in the graphene ribbons. Raman mapping of a G.N.R./Si Schottky junction. Raman map at (e) ~1340 cm⁻¹ (D-band), (f) ~1580 cm⁻¹ (G-band), (g) ~2680 cm⁻¹ (2D-band) before and after a breakdown. (e-f) Pre-failure G.N.R. had sharp and distinct uniform boundaries. (h-j) Sharp GNR changed into non-uniform and irregular termination at edges resulting from the disruption of GNR due to electrical stress.
Gr/Si Schottky devices broke down due to graphene rupturing at edge contacts rather than the active device area. So, the Gr/Si junction is unaffected and intact even after graphene is burnt on contact edges. We fabricated a multi-electrode device with the same Gr/Si junction for a broader investigation. The I-V curves of multiple electrodes are shown in Fig. 7(a). A 3D schematic of multiple electrodes is shown in an inset of Fig. 7(a). When the device loses its graphene contact with one electrode, the other electrodes can act as an additional electrode, enhancing its usability even after multiple breakdowns. As illustrated in Fig. 7(b), when E-1 was undergoing high electrical stress, the neighboring electrode-2 (E-2) remained unaffected. When electrical stress was applied to E-2, the device was still functional and failed at 103 V. The above-stated technique, as Gr/Si Schottky junction, is thermally stable under ESD conditions and can use a single junction multiple times.

Fig. 7. (a) I-V characterization of multiple electrodes of Gr/Si junction (Inset: 3D schematic of multiple electrodes). (b) Gr/Si junction current density is a function of the forward voltage (V_F) at electrodes E-1 and E-2 after a breakdown.

In the light of the present work, it is shown that the Gr/Si Schottky diode is a suitable candidate for being utilized in high frequency and charge dynamics due to its proven robustness. The fast response and absorption of ESD spiking lead us to new applications to protect spike-sensitive devices.

V. CONCLUSION

The 2D-3D heterostructures are essential to electrical and optoelectronic study as providing a fundamental approach to exploring charge transport. The challenges of 2D-3D heterostructures lie in ensuring their robustness, highly durable, and reliability, which demands extensive study. We have used transmission line pulse and microscopic techniques to explore the electrical charge dynamic at 2D-3D contact. Our data indicate that charge crowding significantly limits the device performance. The role of current crowding will reduce, and charge transport will enhance by improving the heat mitigation. It has important facts for the design of graphene-based devices, as the graphene ribbon device appears to be more defective and prone to disruptions under high electrical stress. In contrast, the Gr/Si Schottky junction (with graphene sheet) is structurally stable and robust without sacrificing its junction performance. Benefitting its broadband photodetection in parallel, it has excellent potential for applications where high current carrying capability and avalanche photodetection at large voltage biases. Our work also draws attention to the significance of engineering the 2D-3D interface, which often is the bottleneck preventing the nanoscale 2D-3D device far from reaching its ideal performance.

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