Memory devices obtained by $\text{Si}^+$ irradiation through poly-Si/SiO$_2$ gate stack

P Dimitrakis$^1$, P Normand$^1$, E Vontitseva$^2$, K H Stegemann$^2$, K H Heinig$^3$ and B Schmidt$^3$

$^1$Institute of Microelectronics, NCSR “Demokritos”, P.O. Box 60228, 15310 Aghia Paraskevi, Greece
$^2$Zentrum Mikroelektronik Dresden AG, Grenzstrasse 28, D-01109 Dresden, Germany
$^3$Research Center Rossendorf, P.O. Box 510119, D-01314 Dresden, Germany

E-mail: pdimit@imel.demokritos.gr

Abstract. Ion irradiation induced interface mixing was used to generate silicon nanoclusters at the SiO$_2$-Si interface of metal-oxide-semiconductor (MOS) structures aiming at electronic memory applications. No particular processing issues have been encountered during integration of this technique in standard submicronic C-MOS technology. The memory properties of the fabricated structures as a function of the $\text{Si}^+$-irradiation dose and post-irradiation temperature and time have been examined through electrical measurements of capacitors and transistors. Low-voltage operating devices that can endure more than $10^6$ programming/erasing cycles have been successfully achieved. While excellent device uniformity and reproducibility have been observed over 6-inch wafers, more research is still required to improve charge retention and ensure the standard 10-year retention time needed for true non-volatile memory applications.

1. Introduction

Nonvolatile memory technology using discrete charge storage nodes embedded in the gate oxide of metal-oxide-semiconductor (MOS) devices offers an attractive alternative for extending the scaling of conventional floating-gate memories. Among the various processing routes explored during the last few years for generating such storage nodes, the ion-beam-synthesis (IBS) technique has received substantial attention due to its flexibility and manufacturing advantages. Particular emphasis has been placed upon Si ion implantation to obtain gate oxides with excess silicon [1, 2] or silicon nanocrystals (ncs, [3-7]). The potential of IBS for nc-based memories operating at low voltages has been recently enhanced through the synthesis in the ultra-low-energy (ULE) regime (typically 1keV) of single Si-nc layers in thin SiO$_2$ films [5-7]. This technique leads to promising device results and many fabrication issues have been identified and solved for its integration at an industrial level [7]. While ion implantation into uncapped gate oxides offers a number of processing alternatives for damage recovery [5], removal of near surface atoms (sputtering effect) during implantation and oxide contamination (e.g. from ambient moisture) between the implantation and annealing steps cannot be avoided. To be efficient, the alternative of using a protecting layer (e.g. poly-silicon) deposited onto...
the gate oxide before ion implantation would require high-energy implants and thus, the advantages of
the low-energy IBS technique will be rapidly lost.

In an effort to overcome this concern, Schmidt and Heinig [8] have recently proposed a different
approach using Si ion irradiation through a poly-Si/SiO$_2$ gate stack. In this approach, the projected
range of the implanted Si ions is much larger than the locations of the poly-Si/SiO$_2$/Si substrate
interfaces. Excess of silicon atoms in the gate oxide generated by Si-SiO$_2$ interface mixing leads after
proper thermal annealing to the formation of δ-layers of Si nanoclusters in close proximity to each
interface. This approach is basically different from the IBS technique since the excess of Si
participating to the formation of the Si-nc δ-layers is not caused by the implanted silicon ions but by Si
recoil atoms that are displaced from the Si substrate and the poly-Si capping layer into the oxide layer
as a result of nuclear collisions [9,10].

In the present contribution, the electrical properties of MOS devices irradiated with silicon to
various fluences and subsequently thermally annealed following different regimes are reported. The
charge storage characteristics of these devices are examined in terms of memory windows for different
programming/erasing times and voltages. Endurance to successive program/erase cycles and retention
time characteristics up to 125°C of selected devices are presented.

2. Experimental
Test MOS capacitors were fabricated on 6-inch p-type silicon wafers. Si irradiation was carried out
after the growth of a 14.5nm-thick gate oxide capped with a 50nm-thick deposited poly-Si layer. The
structures were irradiated with 50keV $^{28}$Si$^+$ to doses ranging from $5 \times 10^{15}$ to $2 \times 10^{16}$ cm$^2$. An additional
200nm-thick poly-Si layer was then deposited and subsequent phosphorus ion implantation was
performed. Finally, rapid thermal annealing (RTA) in N$_2$ for 30s at 950 to 1050°C was carried out for
the purpose of Si-nc δ-layer formation and electrical activation of P in the poly-Si gate. After capacitor
evaluation, nMOSFET devices were fabricated on 6-inch silicon wafers following a process similar to
that of conventional MOS devices using 0.6µm C-MOS technological rules. The same gate-stack
fabrication sequence as that of capacitors was performed. The structures were irradiated to a fluence of
$7 \times 10^{15}$ Si$^+$ cm$^{-2}$. The formation of the source/drain regions was achieved during the doping and
annealing steps of the poly-Si gate layer.

3. Results and discussion
High-frequency capacitance-voltage (C-V) measurements were performed on $10^{-4}$cm$^2$-gate area
capacitors annealed for 30s. Flat-band voltage shifts ($\Delta V_{fb}$) due to charge storage in the gate oxide
were clearly observed under rounded gate voltage sweeps (sweep rate ~ 0.5V/s) for all samples
irradiated to a fluence smaller than $2 \times 10^{16}$ Si$^+$/cm$^2$. Under these sweep conditions and for samples
exhibiting a memory behavior, charge storage initiates at very low voltages (ca. 2V) and continuously
increases with the applied gate voltage. Full charge storage was observed for gate voltages lower than
5V. These characteristics as well as the attainable memory windows, leakage current densities, and
interface state densities substantially depend on the ion irradiation fluence and weakly on the post-
irradiation annealing regime. Typical results are presented in figures 1 and 2.

Time-of-Flight (ToF) SIMS and cross-sectional TEM analyses have been performed on 1×$10^{16}$
Si$^+$/cm$^2$-irradiated and 1050°C/30s-annealed structures. Si$_6$ (n=1-5) ToF-SIMS signals clearly indicate
the presence of two Si-rich regions in the gate oxide layer near the poly-Si/SiO$_2$ and SiO$_2$/Si substrate
interfaces, but their weak intensity and the absence of Si$_6$ signal suggest that, if present, Si ncs are too
small or in too low density to be imaged by XTEM. While no Si-ncs were observed by conventional
TEM examination, the presence of a δ-layer of tiny Si ncs (~ 1.5nm) at about 3nm from the SiO$_2$/Si
substrate interface has been recently confirmed by using a mass contrast enhancement method where
Si-ncs are decorated with Ge [9]. Finally, although TEM analysis reveals the presence of extended
defects (dislocation loops) centered at about 70nm under the SiO$_2$/Si substrate interface, the channel
region underneath this interface remains free of defects.
According to the aforementioned results, n-MOSFET memory devices with a gate width (W) of 20µm and gate lengths (L) ranging from 0.6 to 20µm were prepared using irradiation dose of 7×10^{15} Si⁺/cm² and annealing regimes at 1050°C for 30s. Typical transfer characteristics (I_DS-V_GS) of the devices are shown in figure 2. Application of symmetric +7V/-7V (P/E) gate voltage pulses of 1ms width leads to a threshold voltage (defined at I_DS = (W/L) x 10nA) window of about 0.5V. The subthreshold swing of these devices is 86mV/dec.

Figure 1. Flat-band voltage as a function of the gate voltage round sweep for MOS capacitors irradiated at 5×10^{15} Si⁺ cm⁻² and annealed at various temperatures.

Figure 2. Flat-band voltage as a function of the gate voltage round sweep for MOS capacitors irradiated at 1×10^{16} Si⁺ cm⁻² and annealed at various temperatures.

Figure 3. Typical transfer characteristics for 20µm×20µm for fresh n-MOSFET and after programming and erasing operations.

Figure 4. Memory window characteristics obtained by sequential P/E pulses with different heights and widths.

The memory windows (ΔV_TH) attainable after application of symmetric negative (E) and positive (P) gate voltage pulses of different lengths and widths are presented in figure 3. Threshold voltage saturation occurs for pulses of ±5V/100ms, ±6V/10ms, ±7V/1ms, ±8V/100µs leading to memory windows of 0.7, 0.6, 0.5 and 0.4V, respectively. For higher pulse voltages or lower pulse durations, the trapped charges escape to the poly-Si gate leading to smaller ΔV_TH. Charge storage efficiency is mainly due to electron injection (programming regime) from the channel into the Si-ncs δ-layer. Contrary to MOS capacitors a very weak action of negative pulses in terms of hole injection was detected. Furthermore, statistical ΔV_TH evaluation performed through the wafer and repeated for a second batch show small memory window fluctuations clearly indicating that the fabrication process is uniform and reproducible.
The endurance of the devices was tested under 1ms and 10ms +7/-7V P/E pulse regimes (see figure 5). While the ±7V/10ms stressed devices exhibit an increasing drift in threshold voltage with P/E cycles and clear degradation after $10^6$ cycles, neither degradation nor drift in memory window was detected after $10^7$ P/E cycles in the case of ±7V/1ms stressed devices. Typical charge retention characteristics of un-cycled devices at room temperature and 125°C are shown in Fig. 6. The threshold voltage decay due to charge detrapping is logarithmically dependent on the waiting time and presents a decay rate (~75mV/dec) almost independent on the temperature after 100s. Long time extrapolation indicates that a 10-year memory window required for true nonvolatile memory applications cannot be ensured.

Figure 5. Endurance characteristics for tested n-MOSFET subjected to different pulses.

Figure 6. Charge retention characteristics obtained at different ambient temperatures.

4. Conclusions
Si ion irradiation through a poly-silicon/SiO$_2$ gate stack has been examined as a technological route for generating Si-nc δ-layer floating-gate memory structures. Low-voltage and high-speed operating memory cells that can endure $10^7$ programming/erasing cycles have been demonstrated. While excellent device uniformity and reproducibility have been observed over 6-inch wafers, data retention evaluation reveals that more research is still required to fine tune the fabrication process and insure a 10-year memory window for nonvolatile memory applications.

5. Acknowledgements
This work was financially supported by the NEON/GROWTH EU project under contract GRD1-2000-25619.

6. References
[1] Kalnitsky A, Boothroyd A R and Ellul J P 1988 *IEDM Tech. Digest* (IEEE) p 516
[2] Ohzone T, Matsuda T and Hori T 1996 *IEEE Trans. Elec. Devices* **43** 1374
[3] Hanafi S, Tiwari S and Khan I 1996 *IEEE Trans. Elec. Devices* **43** 1553
[4] von Borany J, Gebel T, Stegemann K H, Thees H J and Wittmaack M 2002 *Solid-State Electron.* **46** 1729
[5] Müller T et al. 2004 *Appl. Phys. Lett.* **85** 2373
[6] Normand P et al. 2003 *Appl. Phys. Lett.* **77** 3450
[7] Dimitrakis P et al. 2004 *Solid-State Electron.* **48** 1511
[8] Schmidt B, Grambole D and Herrmann F 2002 *Nucl. Instrum. Methods B* **191** 482
[9] Schmidt B and Heinig K H Patent No. DE 199 33 362
[10] Heinig K H et al. 2003 *Appl. Phys* **A77** 17
[11] Röntzsch L, Heinig K H and Schmidt B 2004 *Mate. Science in Semic. Proces.* **7** 357