On Linear Learning with Manycore Processors

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Abstract—A new generation of manycore processors is on the rise that offers dozens and more cores on a chip and, in a sense, fuses host processor and accelerator. In this paper we target the efficient training of generalized linear models on these machines. We propose a novel approach for achieving parallelism which we call Heterogeneous Tasks on Homogeneous Cores (HTHC). It divides the problem into multiple fundamentally different tasks, which themselves are parallelized. For evaluation, we design a detailed, architecture-cognizant implementation of our scheme on a recent 72-core Knights Landing processor that is adaptive to the cache, memory, and core structure. Our library efficiently supports dense and sparse datasets as well as 4-bit quantized data for further possible gains in performance. We show benchmarks for Lasso and SVM with different data sets against straightforward parallel implementations and prior software. In particular, for Lasso on dense data, we improve the state-of-the-art by an order of magnitude.

Index Terms—Manycore, performance, machine learning, coordinate descent, GLM, SVM, Lasso

I. INTRODUCTION

The evolution of mainstream computing systems has moved from the multicore to the manycore area. This means that a few dozen to even hundreds of cores are provided on a single chip, packaged with up to hundreds of gigabytes of memory at high bandwidth. Examples include Intel Xeon Phi (up to 72 cores), ARM ThunderX2 (64 cores), Qualcomm Centriq 2400 (48 cores), and of course CPUs (100s of cores). One declared target of the recent generation of manycores is machine learning. While much work has been devoted to efficient learning and inference of neural nets on CPUs, e.g. [1], [2], other domains of machine learning and manycores have received less attention.

One exciting trend in manycore is the move from accelerators (like GPUs) to standalone manycore processors. These remove the burden of writing two types of code and enable easier integration with applications and legacy code. However, the efficient mapping of the required mathematics to manycores is a difficult task as compilers have inherent limitations to perform it given straightforward C (or worse, Java, Python, etc.) code, a problem that has been known already for the earlier, simpler multicore and single core systems [3]. Challenges include vector instruction sets, deep cache hierarchies, non-uniform memory architectures, and efficient parallelization.

The challenge we address in this paper is how to map machine learning workloads to manycore processors. We focus on recent standalone manycores and the important task of training generalized linear models used for regression, classification, and feature selection. Our core contribution is to show that in contrast to prior approaches, which assign the same kind of subtask to each core, we can often achieve significantly better overall performance and adaptivity to the system resources, by distinguishing between two fundamentally different tasks. A subset of the cores will be assigned a task $A$ that only reads the model parameters, while the other subset of cores will perform a task $B$ that updates them. So in the manycore setting, while the cores are homogeneous, we show that assigning them heterogeneous tasks results in improved performance and use of compute, memory, and cache resources. The adaptivity of our approach is particularly crucial: the number and assignment of threads can be adapted to the computing platform and the problem at hand.

We make the following contributions:

1) We describe a novel scheme, consisting of two heterogeneous tasks, to train generalized linear models on homogeneous manycore systems. We call it Heterogeneous Tasks on Homogeneous Cores (HTHC).

2) We provide a complete, performance-optimized implementation of HTHC on a 72-core Intel Xeon Phi processor. Our library supports both sparse and dense data as well as data quantized to 4 bits for further possible gains in performance. Our code is publicly available1.

3) We present a model for choosing the best distribution of threads for each task with respect to the machine’s

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1https://github.com/ElizaWszola/HTHC
memory system. We demonstrate that with explicit control over parallelism our approach provides an order of magnitude speedup over a straightforward OpenMP implementation.

4) We show benchmarks for Lasso and SVM with different data sets against straightforward parallel implementations and prior software. In particular, for Lasso on dense data, we improve the state-of-the-art by an order of magnitude.

II. Problem Statement & Background

This section details the considered problem class, provides necessary background on asynchronous stochastic coordinate descent and coordinate selection, and introduces our target platform: the Intel Knights Landing (KNL) manycore processor.

A. Problem specification

We focus on the training of generalized linear models (GLMs). In mathematical terms this can be expressed by the following optimization task:

$$\min_{\alpha \in \mathbb{R}^n} \mathcal{F}(\alpha) := f(D\alpha) + \sum_{i \in [n]} g_i(\alpha_i),$$

where $[n] = \{1, \ldots, n\}$, $f$ and $g_i$ are convex functions, and $\alpha \in \mathbb{R}^n$ is the model to be learned from the training data matrix $D \in \mathbb{R}^{d \times n}$ with columns $d_1, \ldots, d_n$. The function $f$ is assumed to be smooth. This general setup covers many widely applied machine learning models including logistic regression, support vector machines (SVM), and sparse models such as Lasso and elastic-net.

B. Coordinate descent

A popular method for solving machine learning problems of the form (1) is stochastic (a.k.a. random) coordinate descent, where the separability of the term $g := \sum_i g_i(\alpha_i)$ is crucial for its efficiency. Coordinate descent methods [4] form a group of algorithms which minimize $\mathcal{F}$ coordinate-wise, i.e., by performing the optimization across multiple iterations $i \in \{1, \ldots, T\}$, where each iteration updates a single model parameter $\alpha_i$ using the corresponding data column $d_i$, while the other parameters remain fixed. In this way, an optimization over a complex model with many variables can be split into a sequence of one-dimensional optimization problems. Note that this approach can also be extended to batches where a subset of coordinates is updated at a time. While the coordinate descent algorithm is by its nature sequential, it can be parallelized such that the coordinates are updated asynchronously in parallel by multiple threads. It can be shown that such a procedure maintains convergence guarantees if the delay between reading and updating the model vector is small enough [5]. This delay, which is a proxy for the staleness of the model information used to compute each update, depends on the data density and the number of threads working in parallel.

Typically, the coordinates to update are picked at random. However, to accelerate the coordinate decent procedure, we can assign importance measures to individual coordinates. Different such measures exist and they depend either on the dataset, the current model parameters, or both. They can be used for the selection of important coordinates during the coordinate descent procedure, speeding up overall convergence, either by deriving sampling probabilities (importance sampling, e.g., [6], [7]), or by simply picking the parameters with the highest importance score (greedy approach, e.g., [8], [9]).

C. Duality-gap based coordinate selection

A particular measure of coordinate-wise importance that we will adopt in this paper, is the coordinate-wise duality gap certificate proposed in [10]. The authors have shown that choosing model parameters to update based on their contribution to the duality gap provides faster convergence than random selection and classical importance sampling [11]. To define the duality gap measure we denote the convex conjugates of $g_i$ by $g^*_i$, defined as $g^*_i(v) := \max_u v u - g_i(u)$. Then, the duality gap (see [12]) of our objective (1) can be written as

$$\text{gap}(\alpha; w) := \sum_{i \in [n]} \text{gap}_i(\alpha_i; w), \quad \text{with}$$

$$\text{gap}_i(\alpha_i; w) := \alpha_i(w, d_i) + g_i(\alpha_i) + g^*_i(-\langle w, d_i \rangle),$$

where the model vector $\alpha, w$ are related through the primal-dual mapping $w := \nabla f(D\alpha)$. Importantly, knowing the parameters $\alpha$ and $w$, it is possible to calculate the duality gap values (2) for every $i \in [n]$ independently and thus in parallel. In our implementation, we introduce the auxiliary vector $\nu = D\alpha$ from which $w$ can be computed using a simple linear transformation for many problems of interest.

D. The Knights Landing architecture

Intel Knights Landing (KNL) is a manycore processor architecture used in the second generation Intel Xeon Phi devices, the first host processors, i.e., not external accelerators, offered in this line. It provides both high performance (with machine learning as one declared target) and x86 backwards compatibility. A KNL processor consists of 64–72 cores with low base frequency (1.3–1.5 GHz). KNL offers AVX-512, a vector instruction set for 512-bit data words, which allows parallel computation on 16 single or 8 double precision floats. It also supports vector FMA (fused multiply-add) instructions (e.g., $d = ab + c$) for further fine-grained parallelism. Each core can issue two such instructions per cycle, which yields a theoretical single precision peak performance of 64 floating point operations (flops) per cycle. Additionally, AVX-512 introduces gather-scatter intrinsics facilitating computations on sparse data formats. The KNL cores are joined in pairs called tiles located on a 2D mesh. Each core has its own 32 KB L1 cache and each tile has a 1 MB L2 cache. The latter supports two reads and one write every two cycles. This bandwidth is shared between two cores. Each core can host up to four hardware threads. KNL comes with two types of memory: up to 384 GB of DRAM (6 channels with an aggregate bandwidth of 80 GB/s as measured with the STREAM benchmark [13])
and 16 GB of high-bandwidth MCDRAM (8 channels and up to 440 GB/s respectively). The MCDRAM is configurable to work in one of three different modes: 1) cache mode in which it is used as L3 cache, 2) flat mode in which it serves as a scratchpad, i.e., a software-controlled memory (in this mode, there is no L3 cache), 3) hybrid mode in which part is working in cache mode and part in flat mode. In this paper, we use a KNL with 72 cores, 1.5 GHz base frequency, and 192 GB of DRAM in flat mode. The flat mode allows us to clearly separate the memory needed by the subtasks characterized in the next section.

III. METHOD DESCRIPTION

Our scheme adopts an asynchronous block coordinate descent method where coordinate blocks are selected using the duality-gap as an importance measure as described in Section II-C. The workflow is illustrated in Figure 1 and can be described as two tasks \( A \) and \( B \) running in parallel. Task \( A \) is responsible for computing duality gap values \( g_p \) based on the current model \( \alpha \) and the auxiliary vector \( v \). These values are then stored in a vector \( z \in \mathbb{R}^n \) which we call gap memory. In parallel to task \( A \), task \( B \) performs updates on a subset of \( m \) coordinates, which are selected based on their importance measure. For computing the updates on \( B \) we opt to use parallel asynchronous SCD (note that other importance sampling schemes or optimization algorithms could be applied to HTHC, as long as they allow \( B \) to operate on the selected columns \( d_i \) in batches). Since \( B \) operates only on a subset of data, it is typically faster than \( A \). Therefore, it is very likely that \( A \) is not able to update all coordinates of \( z \) during a single execution of task \( B \) and some entries of the gap memory become stale as the algorithm proceeds. In practice, the algorithm works in epochs. In each epoch, \( B \) updates the batch of selected coordinates, where each coordinate is processed exactly once. At the same time, \( A \) randomly samples coordinates and computes \( g_p \) with the most recent (i.e., obtained in the previous epoch) parameters \( \alpha, v \) and updates the respective coordinate \( z_i \) of the gap memory. As soon as the work of \( B \) is completed, it returns the updated \( \alpha \) and \( v \) to \( A \). \( A \) pauses its execution to select a new subset of coordinates to send to \( B \), based on the current state of the gap memory \( z \). The robustness to staleness in the duality gap based coordinate selection scheme has been empirically shown in [10].

A. Implementation challenges

We identify the most computationally expensive parts of the proposed scheme. Task \( A \) computes the coordinate-wise duality gaps (2), which requires an inner product between \( w \), computed from \( v \), and the respective data column \( d_i \):

\[
z_i = h(\langle w, d_i \rangle, \alpha_i).
\]

(3)

\( h \) is a scalar function defined by the learning model with negligible evaluation cost.

Task \( B \) performs coordinate descent on the selected subset of the data. Thus, in each iteration of the algorithm, a coordinate descent update on one entry of \( \alpha \) is performed, i.e., \( \alpha_i^{t+1} = \alpha_i + \delta \). Also this update takes the form

\[
\delta = \bar{h}(\langle w, d_i \rangle, \alpha_i),
\]

(4)

where \( \bar{h} \) is a scalar function. The optimal coordinate update has a closed-form solution [4], [14] for many applications of interest, and otherwise allows a simple gradient-step restricted to the coordinate \( i \). With every update on \( \alpha \) we also update \( v \) accordingly: \( v^+ = v + \delta d_i \), to keep these vectors consistent.

The asynchronous implementation of SCD introduces two additional challenges: First, staleness of the model information \( v \) used to compute updates might slow down convergence or even lead to divergence for a large number of parallel updates. Second, writing to shared data requires synchronization, and generates write-contention, which needs to be handled by appropriate locking.

IV. IMPLEMENTATION ON MANYCORE PROCESSORS

The main contribution of this paper is to show that a scheme for learning GLMs based on multiple heterogeneous tasks is an efficient solution for implementation on a standalone, state-of-the-art manycore system such as KNL. As we will see, our approach is typically over an order of magnitude faster than simple C++ code with basic OpenMP directives. Due to the need for careful synchronization, locking and separation of resources, a straightforward implementation is not efficient in the manycore setting: a detailed calibration to the hardware resources and an associated implementation with detailed thread control is the key. In the following we will detail the challenges and key features for achieving an efficient implementation.

A. Parallelization of the workload

Our implementation uses four levels of parallelism: 1) \( A \) and \( B \) are executed in parallel. 2) \( A \) performs updates of \( z_i \) in parallel and \( B \) performs parallel coordinate updates. 3) \( B \) uses multiple threads for each vector operation. 4) The main computations are vectorized using AVX-512.

1) Allocation of resources to the tasks: To map HTHC onto the KNL we divide compute and memory resources among the two tasks \( A \) and \( B \). We divide the compute resources by assigning separate sets of cores (in fact tiles for better data sharing) to each task. The respective number of

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Fig. 1: Visualization of our HTHC approach.
cores is a parameter that makes our implementation adaptive to the problem and target platform. We use the threading library pthreads for fine-grained control over thread affinity, synchronization, and locking over critical regions of the code. For more details we refer to Section IV-F. To split the memory resources between the two tasks we use the KNL in flat mode where the MCDRAM memory serves as a scratchpad. This setting is particularly suited for our scheme because we can allocate the data for $A$ to DRAM and the data for $B$ to MCDRAM. As a consequence, saturating the memory bandwidth by one task will not stall the other. This approach has another advantage. While the large datasets could not fit entirely into MCDRAM, $B$ can be configured to work only with a subset of data small enough to be allocated there.

2) Parallelization of the individual tasks: For $A$, we use only one thread for every update of a single $z_i$ due to the high risk of deadlocks when computations on $B$ are finished and $A$ receives a signal to stop. The number $T_A$ of threads used for $A$ is a parameter used for adaptation.

In contrast to $A$, $B$ performs $T_B$ updates in parallel and also parallelizes the inner product computation of each update across $V_B$ threads. Thus, the total number of threads used by $B$ is $T_B \cdot V_B$. Both are parameters in our implementation. When $V_B$ threads are used per update, $v$ and the corresponding $d_i$ are split into equal chunks.

A simple model can be used to determine a good choice for $V_B$ as explained next. The performance of both the inner product and the $v$ update is limited by the memory bandwidth. For this reason, it is desirable that $v$, which is reused, stays in cache. To achieve this, the cache has to hold $v$ and two columns $d_i$, $d_j$. Since $v$ and $d_i$ have the same length, this means the chunk size should be about a third of the cache size, i.e., about 87,000 single precision numbers for the L2 caches in KNL. Optimizing with the same reasoning for the 32KB L1 cache would yield a length of $v$ below 4096 elements. Such short vectors would not benefit from parallelism due to issues discussed later. Thus, we do not consider this setup applicable to the L1 caches. The best choice for $T_B$ is influenced by several factors as will be discussed in Section IV-F.

3) Vectorization with AVX-512: We implemented both the scalar product (executed on both $A$ and $B$) and the incrementation of $v$ (performed on $B$) using AVX-512 FMA intrinsics with multiple accumulators for better instruction-level parallelism. The peak single core performance of KNL is 64 flops/cycle, but in the scalar product, each FMA requires two loads from L2 cache, reducing the peak to 16. In practice, our entire coordinate update achieves about 7.2 flops/cycle, about three times faster than without AVX.

B. Synchronization

Task $A$ does not write to shared variables and thus requires no synchronization between threads. In contrast, the updates on $B$ are performed with multiple threads per vector as explained above. For the updates in Equation (4), three barriers are required to separate the resetting of the shared result from the scalar product and the computation of $\hat{h}$ based on the new shared result.

For the implementation we use pthreads which provides synchronization mechanisms with mutexes and thread barriers. Since barriers are relatively expensive, we replace them with a mechanism based on integer counters protected by mutexes similar to [15].

In addition to synchronization per thread, we need to coordinate running and stopping the tasks at the beginning and the end of each epoch $t$ (see Fig. 1). To avoid the overhead of creating and destroying threads, we use a thread pool with a constant number of threads for $A$ and $B$. To synchronize, we use another counter-based barrier scheme similar to the one described above.

C. Atomic operations

We enforce atomic updates to the shared vector $v$ to preserve the primal-dual relationship between $w$ and $\alpha$ and thus maintain the convergence guarantees of asynchronous SCD derived by Hsieh et al. [16]. The pthreads library does not provide atomic operations, but the mutexes can be used to lock chosen variables. To avoid overhead, we use medium-grained locks for chunks of 1024 vector elements.

D. Sparse representation

To efficiently support also sparse datasets, we use a special data structure for $D$ akin to the CSC (compressed sparse-column) format, while $v$ and $\alpha$ remain in dense format. $D$ is represented as an array of structures containing pointers, one for each column. Each column contains only the nonzero elements, encoded as (index, value) pairs. $B$ stores its own data columns $\{d_i\}_{i \in P}$ in a similar way, with the columns additionally split into chunks of a fixed length, implemented as linked lists. This way, efficient movement of columns of variable length between $A$ and $B$ into preallocated space is possible, accommodating possible large differences in column length. The minimal chunk size of 32 enables the use of multiple AVX-512 accumulators, but the optimal size depends on the density of $D$. We use locking as described in the previous section. Since the locks are fixed to equal intervals of the dense vector $v$, the number of operations performed under a given lock depends on the density of the corresponding interval of $d_i$ and 1024 might no longer be an efficient choice of the lock size and vary on each dataset. Initially, $B$ allocates a number of empty chunks determined by the $m$ densest columns $d_1$ in $D$, and places the chunks on a stack. When $A$ copies data to $B$, the pointers to chunks are obtained from the stack and rearranged into the linked lists, long enough to accommodate the new set of columns processed by $B$. Next, the data of $\{d_i\}_{i \in P}$ is copied to the corresponding lists. At the same time, the pointers to the chunks linked by the lists corresponding to the columns which are swapped out of $B$ are returned to the stack. With this representation, we observe fastest runtime when one thread is used per vector: in most cases, the sparse vectors are shorter than 130,000 elements.
E. Quantized representation

Stochastic quantization to reduced bit width reduces data size while still maintaining performance for many iterative optimization and machine learning algorithms (e.g., [17]). To investigate and provide potential benefits, we extend HTHC with support for 4-bit quantization using an adaptation of the Clover library [18], which provides efficient quantized low-level routines including the scalar product. We find that 4-bit precision is enough to represent the data matrix \( D \), without significantly sacrificing model accuracy. For \( \nu \) and \( \alpha \), low precision results in excessive error accumulation; thus we leave those at 32-bit floating point. The overall benefit is reduced data movement and memory consumption at the overhead of packing and unpacking 4-bit data for computation. We show runtime results in Section V.

F. Balancing compute resources

A major challenge posed by the implementation of HTHC is how to balance the computing resources across the different levels of parallelism as discussed in Section IV-A. The configuration of HTHC is parameterized by \( T_A, T_B, \) and \( V_B \), and can be adjusted to the hardware and problem at hand. We identified two important factors that impact the optimal setting:

\( a) \) Balanced execution speed: If \( B \) works significantly faster than \( A \), the latter executes only few \( z_i \) updates. As a consequence most coordinate importance values become stale, and convergence suffers. This effect has empirically been investigated in [10], which showed that satisfactory convergence requires about 15% or more of the \( z_i \) being updated in each epoch. We will discuss this further in Section V. On the other hand, if \( B \) is too slow, the runtime suffers. Hence, the efficiency of the implementation is a crucial factor that impacts the best configuration.

\( b) \) Cache coherence: The parallelization of the gap memory updates on \( A \) across a large number of threads can lead to DRAM bandwidth saturation. Additionally, more threads mean higher traffic on the mesh, which can impact the execution speed of \( B \). For fast convergence, the threads must be assigned so that \( A \) performs a sufficient fraction of \( z_i \) updates in each epoch. Our results will confirm \( \tilde{r} = 15\% \) of the columns of \( D \) updated by \( A \) as a safe choice.

\( c) \) Performance model: Let us consider dense data. Recall that we operate on the data matrix \( D \in \mathbb{R}^{d \times n} \), where each of the \( n \) coordinates corresponds to a column represented by vector \( d_i \) of length \( d \), and that \( B \) processes \( m \) coordinates per epoch. Let \( t_{I,d}(\ldots) \) denote the time of a single coordinate update on task \( I \in \{A,B\} \) with vector length \( d \). This function is not trivial to derive, due to relatively poor scalability of the operations used and the dependence on memory and synchronization speed. Thus, we precompute the values for different thread setups and \( d \) during installation and store them in a table. Using this table, we then use the following model to obtain the thread counts:

\[
\min_{m,T_A,T_B,V_B} \quad m \cdot t_{B,d}(T_B,V_B) \quad \text{s.t.} \quad \frac{m \cdot t_{B,d}(T_B,V_B)}{t_{A,d}(T_A)} \geq \tilde{r} \cdot n
\]
Fig. 3: Performance (in flops/cycle) of operations of task $B$ for different numbers $T_B$ of parallel updates. Different curves represent different values of $V_B$.

### TABLE I: Data sets used in the experiments

| Dataset   | Samples  | Features | Representation | Approx. Size |
|-----------|----------|----------|----------------|--------------|
| Epsilon  [19] | 400,000  | 2,000    | Dense          | 3.2 GB       |
| DvsC      [20] | 40,002   | 200,704  | Dense          | 32.1 GB      |
| News20    [21] | 19,996   | 1,355,191| Sparse         | 0.07 GB      |
| Criteo    [22] | 45,840,617 | 1,000,000| Sparse         | 14.4 GB      |

To analyze the impact of the parameters $V_B$ and $T_B$ on the performance of task $B$, we allocate $D$ and $V$ to MCDRAM. Fig. 3 illustrates the impact of $V_B$ and shows results for $T_B = \{1, 4, 8, 16\}$. The few outliers in plots drawn for larger numbers of threads are caused by background processes which stall the execution of the program on particular cores. We note that below $d = 130,000$ it is best to use one thread per vector, independent of the number of parallel updates. For larger vectors, the best strategy is to use as many threads per vector as possible. We observe that for the vector lengths considered, higher performance is obtained with more parallel updates rather than with more threads per vector. This can be attributed to the overhead of synchronization when multiple threads work with the same vector.

Fig. 4 shows the speedup of isolated $B$ runs with different values of $T_B$ over a run with $T_B = 1$. For each value of $T_B$, we plot results for the runs with the best corresponding $V_B$. We observe that the algorithm used by $B$ does not scale well. This is due to many synchronization points during updates. Profiling with Intel VTune shows that while the bandwidth of L2 caches is a bottleneck on each tile, the saturation of MCDRAM bandwidth remains low. For this reason, we benefit from the flat mode, since it keeps MCDRAM as a separate allocation space. The raw update speed of $B$, contrary to the convergence of the complete scheme, is not affected by too many parallel updates of $V$. In practice, the optimal value for $T_B$ is rarely the maximum, as we will see in the following experiments.

### Performance evaluation

The second series of experiments compares the performance of HTHC to several reference schemes of the two selected linear models across three data sets of different size. We consider Lasso and SVM on the two dense and two sparse data sets in Table I. Dogs vs. Cats (abbreviated as DvsC in our tables) features were extracted as in [20] and the number of samples was doubled. The same pre-processing was used in [10]. The regularization parameter $\lambda$ was obtained to provide a support size of 12% for Lasso on Epsilon and Dogs vs. Cats, and using cross validation in all other cases.

1) **Comparison to our baselines:** In the following we will denote HTHC as $A + B$ emphasizing that it runs two tasks, $A$ and $B$. As detailed in Section IV-A1, HTHC allocates the data for $A$ to DRAM and the data for $B$ to MCDRAM. For each experiment, except those on the Criteo dataset, we used exhaustive search to find the best parameter settings, i.e., percentage of data updated by $B$ per epoch $V_B$, and the thread settings $T_A, T_B, V_B$ described in Section IV. The obtained parameters presented in Tables II, III roughly correspond to the analysis in Section IV-F. We compare HTHC against four reference implementations:

1) **ST (single task):** We consider a parallel, but homogeneous single task implementation, which allocates the data matrix $D$ to DRAM and the remaining data to MCDRAM. It performs randomized asynchronous SCD.
We used the same low-level optimizations in ST as in task \( \mathcal{B} \) of HTHC but without duality-gap-based coordinate selection. Instead, in each epoch we update \( v, \alpha \) (allocated to MCDRAM) for all coordinates of \( D \). Again, we run a search for the best parameters. These are shown in Tables II and III.

2) ST (\( \mathcal{A} + \mathcal{B} \)): Like ST but run with the best setting of \( T_B \) and \( V_B \) for \( \mathcal{A} + \mathcal{B} \).

3) OMP: A straightforward implementation of \( \mathcal{A} + \mathcal{B} \): standard looped C code using the OpenMP directives simd reduction and parallel for for parallelization with the thread counts \( T_A, T_B \) and \( V_B \). To synchronize the updates of \( v \), we use the directive atomic.

4) OMP WILD is as OMP, but without the atomic directive.

We perform OMP runs only for the dense representations. For the large Criteo dataset, we consider only \( \mathcal{A} + \mathcal{B} \) and ST due to the long time to run all experiments.

Fig. 5 shows the results for Lasso and SVM for each data set. Each plot shows the precision of the algorithm versus the running time. For Lasso, we measure suboptimality, for Lasso and SVM we show the duality gap. Each algorithm is run until the duality gap reaches a parametrized threshold value or until timeout.

First, we discuss \( \mathcal{A} + \mathcal{B} \), ST, and ST (\( \mathcal{A} + \mathcal{B} \)). For all Lasso runs, we observe a speedup varying from about 5× for Epsilon to about 9× for News20 compared to the best ST run, depending on the desired precision. As expected, ST (\( \mathcal{A} + \mathcal{B} \)) is never better than ST since the latter uses the best parameters found during the search. The results for suboptimality are consistent with those for the duality gaps.

For the SVM runs, we achieve 3.5× speedup for Dogs vs. Cats and competitive performance for Epsilon and News20.

For Criteo we observe that the ST implementations beats \( \mathcal{A} + \mathcal{B} \). This is mostly due to skipping the update \( v = v + d_i \times \delta \) when \( \delta = 0 \). This leads to selection of relevant data based on the result of \( \langle v, d_i \rangle \), and avoids expensive locking at the same time: thus, in some cases, ST drops enough operations to beat the execution time and the overhead of \( \mathcal{A} + \mathcal{B} \).

Next we discuss the OpenMP runs. For OMP, as expected, the atomic operations severely impact performance and thus OMP WILD is much faster than OMP. While OMP WILD is also faster than the standard HTHC implementations, it does not guarantee the primal-dual relationship between \( w \) and \( \alpha \) and thus does not converge to the exact minimizer; hence the plateau in the figures presenting suboptimality. The duality gap computation \( \text{gap}_D(\alpha; \hat{w}) \) is based on \( \hat{v} \neq D\alpha \), and thus do not correspond to the true values: therefore, the gap of OMP WILD eventually becomes smaller than suboptimality. The OMP run fails to converge on the Dogs vs. Cats dataset with the used parameters.

C. Comparison against other parallel CD implementations

The work [10] implements a similar scheme for parallelizing SCD on a heterogeneous platform: an 8-core Intel Xeon E5 x86 CPU with NVIDIA Quadro M4000 GPU accelerator (we note that this is a relatively old GPU generation: the newer accelerators would give better results). It provides results for Dogs vs. Cats with \( \mathcal{B} \) updates set to 25% (the largest size that fits into GPU RAM): a suboptimality of \( 10^{-5} \) is reached in 40 seconds for Lasso and a duality gap of \( 10^{-5} \) is reached in about 100 seconds for SVM. With the same percentage of \( \mathcal{B} \) updates, HTHC needs 29 and 84 seconds, respectively. With our best setting (Fig. 5(d)–5(f)) this is reduced to 20 and 41 seconds, respectively. In summary, on this data, our solution on the standalone KNL is competitive with a state-of-the-art solution using a GPU accelerator with many more cores. We also show that its performance can be greatly improved with proper number of updates on \( \mathcal{B} \).

Additionally, we compare the SVM runs of HTHC (\( \mathcal{A} + \mathcal{B} \)) and our parallel baseline (ST) against PASSCoDe [16], a state-of-the-art parallel CD algorithm, which, however does not support Lasso. We compare SVM against the variant with atomic locks on \( v \) (PASSCoDe-atomic) and a lock-free implementation (PASSCoDe-wild) which is faster, but does not maintain the relationship between model parameters as discussed in Section IV-C. The results are presented in Table IV. On Epsilon, the time to reach 85% accuracy with 2 threads (the same as \( T_B \) for ST) is 8.6 s for PASSCoDe-atomic and 3.21 s for PASSCoDe-wild, but these times decrease to 0.70 s with 24 threads and 0.64 s with 12 threads respectively. For Dogs vs. Cats, greatly increasing or decreasing the \( T_B \) compared to ST did not improve the result. For Dogs vs. Cats, we are 2.4–5× faster, depending on the versions we compare. For Epsilon, we are roughly 2× faster, but exploiting the HTHC design is required to prevent slowdown. On the other hand, PASSCoDe works about 7× faster for the News20 dataset. We attribute this to our locking scheme for \( v \) updates, which is beneficial for dense data, but can be wasteful for sparse representations. Disabling the locks brings the ST execution time down to 0.02 s.

We also compare the Lasso runs against Vowpal Wabbit (VW) [24], which is considered a state-of-the-art library.
Fig. 5: Convergence for Epsilon, Dogs vs. Cats, News20 and Criteo.

Since VW does not implement coordinate descent, we opt for stochastic gradient descent. We run the computation on previously cached data. We find that too many nodes cause divergence for dense datasets and opt for 10 nodes as a safe value. For News20, we use a single node. We compare the average squared error of HTHC against the progressive validation error of VW. The results are presented in Table V. Again we observe that while we perform well for dense data, the training on sparse data is slow. Also, the runs on our code and Vowpal Wabbit’s SGD result in two different scores for News20.

Overall, we observe that our approach is more efficient for dense representations. On sparse datasets, the amount of computation is too small to compensate for synchronization overhead.
D. Experiments on sensitivity

During the search for $A+B$, we considered four parameters: size of $B$, $T_A$, $T_B$ and $V_B$. Our goal was not only to find the best parameters, but also to identify parameters giving a close-to-best solution. Fig. 6 presents parameters which provided no more than overall 110% convergence time of the best solution found. The overall convergence time depends on the number of epochs which varies from run to run for the same parameters: therefore, we consider all the presented parameters capable of obtaining the minimum runtime. The plots present four dimensions: the axes correspond to $T_B$ and $V_B$ while different markers correspond to different percentages of data updated by $B$ per epoch. The labels next to the markers correspond to $T_A$. The color of each label corresponds to its marker. Multiple values per label are possible. To save time during the search, we used a step of 8 and 4 for $T_A$ on Dogs vs. Cats and Epsilon respectively. Additionally, we use a step of 2 for $T_B$ on both datasets. We also note that while Lasso on Epsilon converges faster for $T_B > 8$, the rate of diverging runs is too high to consider it for practical applications.

To examine how the number of $z_i$ updates per epoch on $A$ affects the convergence, we run tests in which we always perform a fixed number of updates. We use the best parameters found for different datasets and models, but we set $T_A = 10$. We present example results in Fig. 7. We observe that relatively few updates are needed for the best execution time: we observe 10% on both datasets. While these runs need more epochs to converge, the epochs are executed fast enough to provide an overall optimal convergence speed.

E. Evaluation of quantized representation

We run experiments on the dense datasets using the quantized 4-bit representation of the data matrix $D$ with the modified Clover library. Table VI shows the comparison of
TABLE VI: Comparison of 32-bit to mixed 32/4-bit.

| Dataset | Model | Target gap | 32-bit  | 32/4-bit |
|---------|-------|------------|---------|----------|
| Epsilon | Lasso | $10^{-5}$  | 1.6 s   | 1.0 s    |
| Epsilon | SVM   | $10^{-5}$  | 5.5 s   | 5.8 s    |
| DvSC    | Lasso | $10^{-3}$  | 55.5 s  | 32.4 s   |
| DvSC    | SVM   | $10^{-5}$  | 38.2 s  | 51.6 s   |

the fastest $A + B$ runs using the mixed 32/4-bit arithmetic to the fastest 32-bit $A + B$ runs. We can observe that while we reduce the data size, the computation times do not deviate significantly from those obtained with 32-bit representation.

VI. RELATED WORK

Variants of stochastic coordinate descent [25] have become the state-of-the-art methods for training GLMs on parallel and distributed machine learning systems. Parallel coordinate descent (CD) has a long history, see e.g. [26]. Recent research has contributed to asynchronous variants such as [5] who proposed AsySCD, the first asynchronous CD algorithm, and [16] who proposed the more practical PaSSCoDe algorithm which was the first to keep the shared vector $v$ in memory.

There are only few works that have studied CD on non-uniform memory systems (e.g. memory and disk). The approach most related to ours is [27] where the authors proposed a strategy to keep informative samples in memory. However, [27] is specific to the SVM problem and unable to generalize to the broader class of GLMs. In [28] a more general setting was considered, but the proposed random (block) coordinate selection scheme is unable to benefit from non-uniformity in the training data. In a single machine setting, various schemes for selecting the relevant coordinates for CD have been studied, including adaptive probabilities, e.g. [7] or fixed importance sampling [11]. The selection of relevant coordinates can be based on the steepest gradient, e.g. [8], Lipschitz constant of the gradient [29], nearest neighbor [30] or duality gap based measures [10]. In this work, we build on the latter, but any adaptive selection scheme could be adopted.

Manycore machines, including KNL, are widely used for deep learning, as standalone devices or within clusters, e.g. [31], [32]. SVM training on multicore and manycore architectures was proposed by You et al. [33]. The authors provide evaluation for Knights Corner (KNC) and Ivy Bridge, proving them to be competitive with GPUs. The LIBSVM library [34] is implemented for both GPU [35] and KNC [36]. All SVM implementations use the sequential minimization algorithm [37]. The library and its implementations are more fitted for kernel SVM than the linear version. For training on large-scale linear models, a multi-core extension of LIBLINEAR [38] was proposed by Chiang et al. [39]. This library is tailored mainly for sparse data formats used e.g. in text classification. While [16], [39] do not perform coordinate selection, they use techniques like shrinking benefitting from increasing sparsity of the output models. Rendle et al. [40] introduced coordinate descent for sparse data on distributed systems, achieving almost linear scalability: their approach can be applied to multi- and manycore. The existing open-source libraries support mainly sparse data and rarely implement CD models other than SVM or logistic regression.

VII. CONCLUSIONS

We introduced HTHC for training general linear models on standalone manycores including a complete, architecture-cognizant implementation. We support dense, sparse, and quantized 4-bit data representations. We demonstrated that HTHC provides a significant reduction of training time as opposed to a straightforward parallel implementation of coordinate descent. In our experiments, the speedup varies from $5\times$ to more than $10\times$ depending on the data set and the stopping criterion. We also showed that our implementation for dense datasets is competitive against the state-of-the-art libraries and a CPU-GPU code. An advantage of HTHC over the CPU-GPU heterogeneous learning schemes is the ability of balancing distribution of machine resources such as memory and CPU cores between different tasks, an approach inherently impossible on heterogeneous platforms. To the best of our knowledge, this is the first scheme with major heterogeneous tasks running in parallel proposed in the field of manycore machine learning. The inherent adaptivity of HTHC should enable porting it to other existing and future standalone manycore platforms.

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