Research on Real-time Simulation of Power Electronic Circuits Based on Simscape

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Abstract. In order to realize hardware-in-the-loop simulation of commonly used power electronic circuits, a method of joint simulation using Simcape and field programmable gate array (FPGA) is proposed. This article adopts a switch modeling method suitable for high-frequency characteristics, namely the switch function method. It effectively solves the problem of rigidity non-convergence in the modeling of the binary resistance method, as well as the transient error caused by the binary LC method when the system state is switched with the increase of the switching frequency, which reduces the simulation accuracy. Taking the single-phase full-bridge inverter circuit as an example, a Simscape model based on the state-space averaging method was established, and the HDL code was automatically generated using the Simscape HDL Workflow Advisor tool, and the hardware-in-the-loop simulation was completed with FPGA. Finally, the simulation results with Simulink comparison verify the effectiveness and feasibility of the method.

1. Introduction

At present, power electronics simulation mainly includes real-time simulation and off-line simulation [1] Offline simulation has been gradually replaced by real-time simulation because of its slow simulation speed. The traditional real time simulation based on CPU is limited by the serial execution mode, and the simulation step size is generally in the range of 10~20us, which is no longer applicable to the power electronic system with switching frequency in nanosecond or microsecond level. FPGA has become a hot spot for many scholars to study real-time simulation due to its high parallelism and good real-time performance. RTLAB tools used controllers and real-time simulators for simulation, and verified the correctness of their respective algorithms [2] However, this simulation platform is expensive and the solver is not open source, so this paper adopts Simcape tool for development. The hardware-in-the-loop simulation is carried out directly in Simulink environment, which shortens the development cycle and research cost of the project.

In addition, the construction of switch model also directly affects the simulation results. A pair of resistors are used to represent the on-off of the switch. Although this method can simulate the on-off of the switch, when the switching state changes, the admittance matrix formed by the circuit will change accordingly. If it is a huge MMC system, it will result in a large amount of computation [3] Using an inductor and capacitor to simulate the switching dynamic process can solve the problem of admittance matrix change caused by switching state change, but LC method will cause numerical oscillation when
switching state change, which reduces the simulation accuracy [4]. In order to solve the above problems, this paper adopts the switching function method to model the switching device, and takes the single-phase full-bridge inverter circuit as an example to establish its state space equation. Finally, the accuracy and transient performance of the model are verified by simulation, which provides an idea for hardware-in-the-loop simulation.

2. Model design and implementation

2.1. SPWM control model

Assuming that VT1~VT4 are ideal switching devices, based on the working principle of a single-phase full-bridge inverter circuit, VT1 and VT3 are turned on at the same time, and VT2 and VT4 are turned on at the same time, and a complementary conduction mode is adopted. The switch function method can be used to obtain:

\[ S = \begin{cases} 
1, & \text{VT1, VT3 ON, VT2, VT4 OFF} \\
-1, & \text{VT2, VT4 ON, VT1, VT3 OFF}
\end{cases} \]  

(1)

When ignoring the dead zone and adopting SPWM modulation, the relationship between the DC power supply \( u_{dc} \) and \( u_1 \) is known as:

\[ u_1 = S u_{dc} \]  

(2)

It can be seen from Figure 1:

\[
\begin{align*}
\frac{d}{dt}i_1(t) & = u_0(t) + r \cdot i_1(t) + L \cdot \frac{di_1(t)}{dt} \\
\frac{d}{dt}u_0(t) & = C \cdot \frac{du_0(t)}{dt}
\end{align*}
\]

(3)

Since the Simscape model adopts open-loop control, the on-off of the switch is controlled by the SPWM signal generated by comparing a sine wave with a frequency of 50 Hz and a modulation ratio of \( m \) with a triangular wave with a variable frequency of \( f_c \) and an amplitude of 1. When the difference between the two is greater than 0, it means that the VT1~VT3 switch tubes are turned on, and VT2~VT4 are turned off. On the contrary, the VT2~VT4 switch tubes are turned on, and VT1~VT3 are turned off. Using the mask function to package it into a subsystem is convenient to change the triangle wave frequency \( f_c \), the modulation ratio \( m \) (0 < \( m \) \leq 1), and the carrier frequency \( f \) for subsequent simulation and debugging. Figure 1 is the design diagram of the control model. Among them, the SPWM wave generation process is shown in Figure 1 (a) and the mask package diagram is shown in Figure 1 (b).

![Figure 1 Control model design diagram](image)

(a) SPWM wave generation diagram  
(b) Mask package diagram

2.2. Inverter model construction

The inverter model is constructed by Simscape module, and each module should use the physical model in Simscape library, so as to ensure the generation of HDL code for FPGA call. Figure 2 is an inverter model designed using Simscape. In addition, nonlinear modules cannot be used in the process of model building. Numerical integration algorithm adopts backward Euler method. PS and Simulink conversion module and Rate Transition proportional conversion module (zero-order hold) must be used to connect.
2.3. State space model generation

After the Simscape model is successfully constructed, simulation verification is required before it can be converted to HDL low-level model. To convert the physical model to an equivalent Simulink state-space model, type sschdladvisor(gcs) on the MATLAB command line to open the Simscape HDL Workflow Advisor. We need to check the setup of the Solver Configuration Solver and check if the Simscape model contains nonlinear modules, then extract and discretize the state space equation. The setting of time and step size should be related to the frequency of switch opening and closing, generally not less than 1/20. In each switching mode, the number of iterations is generally set to 3-5. If the number of iterations is too small, the simulation accuracy is not high, and too many iterations will increase the conversion time. The number of iterations set in this paper is 3. The accuracy of floating-point data is generally single, and the three steps indicated by the arrow in Figure 3 represent the entire conversion process. After the discrete state space model is generated, the tool will count the input and output, states, and the number of valid modes in the Simscape model. The state includes resistance, capacitance, inductance, etc. in the Simscape model.

2.4. FPGA in the loop model generation

In order to realize FPGA-based in-the-loop simulation, a hardware description language (Verilog) embedded in the FPGA is required. The HDL subsystem containing the inverter will be downloaded to the FPGA for calculation, and the control system that generates the SPWM signal will be downloaded
to the CPU for calculation. Use HDL Workflow Advisor tool to convert HDL Subsystem into FPGA in the loop model. In this tool, we select the target device, check model compatibility, generate HDL code, and generate FPGA-in-the-loop model. The target device we choose here is the AX7035 development board, the chip is XC7A35T-2FGG484I, the development tool is Xilinx Vivado 2020.2, and the clock frequency is set to 50MHz. Check the compatibility of the HDL System code generated before, that is, you cannot use the variable step size and the calculator must implement the discrete model. Set the generated HDL top-level file and testbench detection file to adopt Verilog language, and the pipeline is optimized. If the oversampling rate is set to 50, the FPGA operation frequency is 50/50=1MHz, that is, 1us operation is performed once. This setting can effectively solve the timing problem. After selecting the connection method between FPGA and computer as JTAG, the tool can automatically generate the FIL model and the bit file loaded into the FPGA. The entire simulation process is implemented in the Simulink environment. Figure 5 shows the entire setup steps.

Figure 6 shows the generated FIL model, which includes the Interface System (Simscape model) and the generated HDL System model. The two models directly need to be connected by the Rate Transition module to solve the problem of module rate mismatch. The output result of the whole model is the voltage and current of the resistive load, and the conversion accuracy is single.

3. Simulation results
In order to verify the accuracy of FPGA in the loop system design, the simulation results are compared with those in Simulink, as shown in Figure 7. The simulation time was set as 0.2s, and the power supply changed from 600V to 360V at 0.1s DC side, and the simulation step was set as 3us. It can be seen from the figure that the voltage and current on both sides of the load in the loop simulation system based on FPGA are basically consistent with the simulation results in Simulink, and the voltage source mutation moment and the load voltage transient recovery on the inverter side are basically consistent. The overall simulation results show that the simulation method based on FPGA is effective and feasible.
(a) Contrast diagram of load voltage

(b) Contrast diagram of load current
4. Conclusion

According to the above discussion and experimental results, the following conclusions are drawn.

1) Simscape tool can be used to convert the simulation model into a state space model, HDL Workflow Advisor can be used to convert the HDL Subsystem into FPGA in the loop model, and the effectiveness and feasibility of the design method are verified by simulation experiments.

2) Compared with the traditional development method, this design method can save the development cost and shorten the development time to a certain extent. More importantly, it can also carry out FPGA in-loop simulation without writing complex hardware programming language [5]. It lays a foundation for further research on FPGA automatic code generation technology and power electronics transient simulation.

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