Digital frequency domain multiplexing readout electronics for the next generation of millimeter telescopes

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ABSTRACT

Frequency domain multiplexing (fMux) is an established technique for the readout of transition-edge sensor (TES) bolometers in millimeter-wavelength astrophysical instrumentation. In fMux, the signals from multiple detectors are read out on a single pair of wires reducing the total cryogenic thermal loading as well as the cold component complexity and cost of a system. The current digital fMux system, in use by POLARBEAR, EBEX, and the South Pole Telescope, is limited to a multiplexing factor of 16 by the dynamic range of the Superconducting Quantum Interference Device pre-amplifier and the total system bandwidth. Increased multiplexing is key for the next generation of large format TES cameras, such as SPT-3G and POLARBEAR2, which plan to have on the order of 15,000 detectors.

Here, we present the next generation fMux readout, focusing on the warm electronics. In this system, the multiplexing factor increases to 64 channels per module (2 wires) while maintaining low noise levels and detector stability. This is achieved by increasing the system bandwidth, reducing the dynamic range requirements though active feedback, and digital synthesis of voltage biases with a novel polyphase filter algorithm. In addition, a version of the new fMux readout includes features such as low power consumption and radiation-hard components making it viable for future space-based millimeter telescopes such as the LiteBIRD satellite.

1. INTRODUCTION

Technological advances in millimeter-wavelength detectors over the past decade have resulted in telescopes with sensitivity limited mainly by the number of the detectors. The next generation of large millimeter-wavelength telescopes, such as SPT-3G and POLARBEAR2 will have on the order of 15,000 detectors, an order of magnitude larger than current cameras. Millimeter cameras employ bolometers that operate at sub-Kelvin temperatures to detect the incident radiation. Reading out each bolometer individually would create a significant thermal load on the cryogenic stages of the camera. Additionally, the complexity and cost of such a system would be restrictive. In order to accommodate the large number of bolometers, the readout is multiplexed, a technique in which many detectors are read out on a single pair of wires.

The bolometer cameras currently operating on the South Pole Telescope and POLARBEAR telescope as well as the EBEX balloon-boorne telescope use digital frequency domain multiplexing (fMux) to read out arrays of transition-edge sensor (TES) bolometers. In those systems, up to 16 bolometers can be multiplexed together by separating the operating bandwidth of each detector in frequency space. In this paper, we present the next generation of the digital fMux readout in which 64 bolometers are multiplexed together, focusing on the room temperature electronics. In addition to the 64x digital fMux electronics for ground-based telescopes, we present a second version of the electronics designed for satellite platforms.

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2. SYSTEM OVERVIEW

A TES bolometer absorbs heat from incident photons, which results in a change in the electrical resistance of a thermistor. Applying a strong voltage bias to the thermistor provides electrical power, holding the TES in the superconducting transition. The constant voltage bias enables negative electrical feedback, where the electrical power changes with the TES resistance keeping the total power constant, and changes the current through the device.

In an fMux readout, bolometers are multiplexed together by placing each in series with an inductor $L$ and capacitor $C$ creating a unique frequency resonance (see Figure 1). The $LCR_{\text{bolo}}$ segments are placed in parallel with each other. A sinusoidal voltage bias is tuned to the resonant frequency of each bolometer and summed together into a single waveform (referred to as the comb of carriers) and input on a pair of wires. The sky signal amplitude modulates each carrier and appears as sidebands in the resulting current. Because the sidebands for each bolometer occupy a unique frequency band, the signals from each of the bolometers are transmitted over a single pair of wires.

The summed bolometer signals are amplified using Superconducting Quantum Interference Devices (SQUIDs). The SQUID is a low-noise, low input-impedance transimpedance amplifier. After the SQUIDs, the signal undergoes additional stages of amplification and signal processing in the room temperature electronics before being digitized and demodulated down to baseband.

One significant challenge in increasing the number of bolometers multiplexed together is dynamic range. As the multiplexing factor increases the dynamic range of the SQUID quickly becomes a limiting factor. Since the sky signal is modulated into the carrier sidebands, the SQUID dynamic range requirements can be significantly reduced by injecting an inverted copy of the carrier comb with a 180 degree phase shift prior to the SQUID input coil (the nuller). In the legacy version of the digital fMux readout, statically applying the nuller was sufficient to ensure that the remaining current into the SQUID coil met the dynamic range requirement. However, the static nulling method is no longer sufficient when the multiplexing factor increases to 64. Instead, an active feedback loop referred to as Digital Active Nulling (DAN) nulls both the carriers and sidebands for each bolometer.

The dynamic range of the synthesizer chain also limits the number of channels that can be multiplexed together. A typical bolometer for a ground-based telescope has a saturation power of 15 pW, and will require a voltage bias of about 3 $\mu$V$_{\text{RMS}}$ for $R_{\text{bolo}} = 1\Omega$, corresponding to a current of 3 $\mu$A$_{\text{RMS}}$. The achievable dynamic range at the bolometer from the synthesizer chain is derived from the properties of the digital-to-analog converter (DAC), a current source, paired with the requirement that the total noise contribution of the DAC at
the bolometer be no more than the SQUID noise (3 pA/√Hz). For the new electronics, the upper limit of the dynamic range of the synthesizer chain at the bolometers is 1.2 mA_{P−P} (424 μA_{RMS}).

In the simplest conceptual mode of operation all synthesized carrier sinusoids are started in phase, limiting the multiplexing factor to far below the goal of 64. By randomizing the relative phases of each carrier frequency, the available bandwidth can be used far more effectively.

The crest factor (sometimes called the “peak-to-average ratio”) is the ratio of the maximum excursion of a waveform amplitude to the root-mean-square (RMS) waveform amplitude,

\[
\text{Crest Factor} = \frac{A_{\text{Peak}}}{A_{\text{RMS}}}.
\]  
\hspace{1cm} (1)

The crest factor for a single sinusoid is \(A_{\text{Peak}}/A_{\text{RMS}} = \sqrt{2}\). Crest factor minimization refers to the practice of reducing the crest factor through a judicious choice of waveform parameters, in this case, the carrier phases. For \(N\) carriers of peak amplitude \(A\), the total waveform RMS grows proportional to \(\sqrt{N}\). In the worst-case scenario, such that all carriers are in phase, the waveform peak amplitude would be \(N \cdot A\), and the crest factor would be \(N \cdot A / (\sqrt{N} \cdot A / \sqrt{2}) = \sqrt{2N}\). An algorithm to adjust the phase of many sinusoids and search for a set of parameters that minimizes the crest factor exists. Since the DAN feedback technique is constantly making small adjustments to the phases of each nuller we look for smoothness of the parameter-space to ensure the existence of broad minima instead of a narrow global minimization. We note that no simple analytic formula to determine a minimum crest factor exists. Instead, the problem is usually addressed with numerical techniques wherein a set of phases is chosen randomly, and the crest factor is estimated by simulating the waveform. We find that, when the phases are chosen randomly, the typical crest factor is 4.25 for 64 carriers, with a spread of \(\sim 4\%\). The resulting waveform peak is \(4.25\sqrt{N} \cdot A / \sqrt{2}\), approximately \(3\sqrt{N}\) larger than the maximum value for a single sinusoid.

Given these results, we can relate the required dynamic range \(A_{\text{dr},P−P}\) to the peak amplitude of a single sinusoid,

\[
\frac{A_{\text{dr},P−P}}{2} = 3\sqrt{N} \cdot A,
\]  
\hspace{1cm} (2)

where \(A = \sqrt{2} \cdot 3\mu A_{\text{RMS}}\) for the desired voltage bias. For ground-based bolometers with a multiplexing factor of 64 a minimum DAC dynamic range of \(A_{\text{dr},P−P} = 204\ \mu A_{P−P}\) is required. The typical dynamic range of the new 64x digital fMux electronics is 1.2 mA_{P−P}, a factor of 6 higher than the minimum required.

Overall, there are three key components of the 64x multiplexing digital fMux readout: SQUID operation, the DAN feedback, and the generation of sinusoidal voltage biases. The following sections describe these components, focusing on the changes necessary to increase the multiplexing factor from 16 to 64.

Figure 2. Photographs of the synthesizer/digitizer mezzanine board (left) and SQUID controller board (right) for the 64x digital multiplexing readout system.
2.1 SQUID Operation

The high gain, low input-impedance, and low noise of SQUIDs make them ideal devices for the first amplification stage of the fMux readout. When a current bias of sufficient magnitude is applied to a SQUID it develops a periodic voltage output as a function of the magnetic flux in the input coil. By applying a direct current flux bias to the input coil, the SQUID can be tuned to the region of maximum gain and linearity (see Figure 7). This functionality, together with other tuning controls, is supplied by the SQUID controller board (Figure 2), each of which can operate four SQUIDs.

The legacy digital fMux readout included a shunt feedback loop to lock the SQUID at the desired tuning point and limit the input signal to the region of linear sensitivity. The 64x digital fMux employs DAN feedback and therefore no longer requires the SQUID shunt feedback. The shunt feedback had a bandwidth of 1 MHz, limiting the multiplexing factor. Removing the shunt feedback, we are able to substantially increase the bandwidth of the system to 10 MHz or higher.

While DAN feedback ensures operation in the linear region of the SQUID, it is desirable to also have a low-frequency feedback loop to ensure the SQUID stays locked at the optimal tuning point. For example, SQUIDs can be sensitive to changing external magnetic fields (e.g., when rotating through the Earth’s field). We implement an analog integral feedback loop between the output of the first stage amplifier and the SQUID input coil (see Figure 1) that has a bandwidth of approximately 10 kHz to ensure a fixed point of operation on long time scales with no additive noise.

2.2 DAN

Digital Active Nulling (DAN) provides feedback to the input coil of the SQUID over a small frequency range around each of the carrier frequencies. In DAN, the amplitude and phase of the nuller current is continuously adjusted with digital signal processing algorithms implemented in firmware at rates much faster than the bolometer time constant. Samples are taken from the demodulator, weighted by a user programmable gain and accumulated to provide integral control to each of the 64 channels. The sky signal is now encoded in the nuller feedback amplitude and the SQUID output becomes an error signal that is used to adjust the nulling levels.

DAN was first implemented as a modification to the legacy digital fMux readout. The South Pole Telescope polarization camera (SPTpol) successfully used DAN for the 2013 observing season, with no significant change in the measured white noise level of the bolometers.

2.3 Digital Signal Processing Firmware

The signal path of the digital fMux system has evolved significantly since the most recent published technical description. These changes have allowed the digital fMux system to aggressively scale to higher channel counts, without substantial increases in either power consumption or Field Programmable Gate Array (FPGA) resource usage. Additionally, we have shifted development of our hardware, firmware, and software stack to a new FPGA motherboard based on Xilinx’s Kintex-7 product line. This platform is a major upgrade from our legacy Virtex-4 platform, and grants us substantial opportunities to improve the firmware’s performance and design margins. In the following sections, we describe these changes.

Although portions of the signal path (e.g., the synthesizer) have become wholly unrecognizable from their earlier incarnations, we have maintained consistent control and data interfaces. The model from the legacy digital fMux readout still serves as a conceptual guide, even though it no longer maps closely to the hardware implementation. The digital signal processing (DSP) framework will continue to evolve. In particular, recent optimizations in the synthesizer structure will also be applied to the demodulator structure, reducing the complexity and power requirements associated with the readout portion of the system. In addition, we continue to optimize the signal path to fully exploit the capabilities of our new hardware platform.
2.3.1 ICE Motherboard FPGA Platform

McGill’s legacy digital fMux readout platform was based on a custom Virtex-4 motherboard first commissioned in 2008. FPGA technology has progressed rapidly since then. To reduce cost, increase channel density, and take advantage of newer FPGAs, we have developed and built a new family of readout hardware. This family includes backplane/crate hardware, FPGA motherboards, and daughtercards based on the FPGA Mezzanine Card (FMC) standard. In this section, we provide a brief technical description of the CPU and FPGA subsystems on the new ICE motherboard.

The CPU subsystem is a stand-alone ARM Cortex-A8 processor, connected to 1 GB DDR3 SDRAM and dual gigabit Ethernet ports. The CPU manages the many small sensors (temperature, voltage) and interfaces (mezzanine power switches, backplane control, various SPI, USB, and I2C buses). It communicates with the FPGA via high-speed SPI, JTAG, and a PCIe link. The CPU boots from a network or from an SD flash card, and manages the FPGA’s boot-up and command interactions.

The FPGA subsystem centers around a Xilinx Kintex-7 ’420T FPGA. The FPGA’s 28 high-speed serial (GTX) ports are committed to two QSFP ports, one selectable SFP or PCIe port, and a 19-channel backplane interconnect. The bulk of the FPGA’s I/O is committed to hosting two high-pin-count (HPC) FPGA Mezzanine Card (FMC) sockets for daughtercards.

Like the previous FPGA platform, the ICE motherboard uses only a single clock reference for all of its onboard systems. This clock is typically sourced from a backplane, although it can also be generated on-board or supplied via an SMA connector. Single-sourced clocking is critical to avoid aliased noise from contaminating the analog data.

![Image of the ICE motherboard](image)

Figure 3. The ICE motherboard, McGill’s new FPGA platform. The black heat sink covers the FPGA; the CPU, DDR3 RAM, and Ethernet PHYs are visible on the right. The red mezzanines are two FMC-compliant high-speed data-acquisition boards.

2.3.2 Mezzanine Interface

The mezzanine board (see Figure 2) interfaces between the ICE FPGA motherboard and SQUID controller board. The mezzanines host the following subsystems:

- Digital-to-Analog Converters (DACs) for synthesizing carrier and nuller waveforms,
• Analog-to-Digital Converters (ADCs) for digitizing bolometer signals,
• A low-speed digital interface for communicating with SQUID controller boards, and
• Programmable-gain amplifiers (PGAs) for optimizing ADC and DAC dynamic range.

These mezzanines, intended for deployment in ground-based experiments, each support 4 SQUID readout modules.

2.3.3 Synthesizer

Of all the portions of the DSP logic, the synthesizer module (Figure 4) has evolved the most. It is barely recognizable from its earlier form. In the following section, we describe the current synthesizer design. Formerly, the carrier and nuller synthesizers directly modulated signals from baseband to the relevant carrier/nuller frequency using a Direct Digital Synthesis (DDS) oscillator and mixer. Both the oscillator and mixer operate at the system’s output sampling rate (25 MSPS). Since the FPGA logic is capable of running substantially faster than 25 MHz, the synthesizer implementation has been optimized by time-multiplexing each mixer and DDS among eight channels. The system’s scalability is ultimately linear; doubling the number of channels required approximately double the logic.

The new carrier and nuller synthesizer is based on a Polyphase Filter Bank (PFB) synthesizer. This synthesizer is best described backwards: The DAC output bandwidth (operating at 20 MHz) is divided into 128 bins; each synthesizer channel frequency is reduced to a choice of the nearest bin, plus some residual frequency offset. The offset is applied via a DDS mixer, which operates at a low enough sampling rate that a single time-multiplexed DDS and mixer suffices for more than 128 channels.

In logical order, the synthesizer’s signal path begins with the offset mixer. After generating sinusoids for each channel at a low sampling rate (625 kHz), amplitudes are applied from either static settings (i.e. in non-DAN mode) or a streaming amplitude port (i.e. in DAN mode.)

Next, a multiplexer combines carrier and nuller in such a way that, after the Fast Fourier Transform (FFT), the carrier appears solely in the real (I) outputs, and the nuller appears solely in the imaginary (Q) components. This permits the use of a single, complex FFT instead of two real FFTs. This multiplexing process is also...
responsible for combining channels that share the same frequency bin, translating the system from a time-multiplexed set of individual channels to a single FFT input buffer. Next, the FFT processes blocks of input data into blocks of output data.

Finally, a polyphase Finite Impulse Response (FIR) filter applies a windowing function that smoothly combines adjacent blocks of FFT outputs. The result is a 20 MSPS stream of independent carrier and nuller data, which is sent to the appropriate DACs. The carrier comb provides the detector biases, and the nuller approximately cancels the signal at the SQUID.

### 2.3.4 Demodulator

The demodulator design (Figure 5) has evolved only slightly from the previous implementation. It still consists of a chain of DDS oscillators, mixers, Cascaded Integrator-Comb (CIC) filters, and FIR filters.

![Diagram of the demodulator signal path](image)

The digitized SQUID signal is first mixed to baseband, then decimated by a CIC filter. In DAN mode, the signal is then passed to a dedicated DAN module for processing. Next, it is decimated by a second CIC filter, processed by a compensating FIR filter, timestamped, and streamed across the network.

The digitized inputs from the system’s ADCs are first processed by DDS-based complex mixers, creating 64 channels at different frequencies from a single ADC source.

Once mixed down to baseband, the signal in each channel is decimated by a factor of 128 using a CIC filter (CIC1). The output of this first decimation step is passed from the demodulator module out to the external DAN module, which automatically adjusts nuller amplitudes when the DAN feedback loop is closed.

The decimated output from the CIC1 filter is also passed to an 8-stage, 112-bit CIC filter (CIC2). This filter is designed with a variable decimation rate, selectable between 16, 32, 64, 128, 256, and 512. The filter’s extreme word length is required to gracefully handle these decimation rates without a degradation in signal quality. To keep CIC2’s implementation tractable, the 112-bit words are broken down into 14-bit sub-words and computed across eight consecutive clock cycles.

Finally, the output from CIC2 is compensated using an 152-tap FIR filter. This filter is necessary to correct passband non-uniformity due to the CIC1 and CIC2 filters.

In the legacy DSP designs, CIC2 was a fixed-rate decimator, followed by 5 FIR filters. Streamed data could be chosen from any of these FIRs. In contrast with the current design, the older version was extremely costly in terms of DSPs and block RAMs within the FPGA. Functionally, the two designs are indistinguishable.
2.3.5 Streaming & Control Interface

The digital fMux control and streaming interfaces are evolving gradually from the legacy system. In this section, we briefly describe recent improvements.

Most importantly, the system’s software stack now runs on the ICE motherboard’s Cortex-A8 CPU. This CPU is an order of magnitude faster than the older system’s MicroBlaze CPU, and includes a hardware floating-point unit. The increase in processor speed takes a substantial burden off the system’s software development.

Now that the CPU is physically separated from the FPGA, we cannot simply access the signal path as a memory-mapped peripheral. The control interface has been moved to an ARM controlled SPI link, which permits reads and writes of the FPGA registers.

For data streaming, the FPGA generates UDP packets directly, and emits them via its SFP interface to a gigabit Ethernet port.

2.4 Cryogenic Components

The previous sections summarized the room temperature electronics for the 64x digital fMux readout. Parallel improvements to the cryogenic components (the SQUIDs, cables, inductors, and capacitors depicted in the 4 K and 0.25 K portions of Figure 1) of the readout system are also underway. These developments are presented in complementary proceedings. Here, we describe the cryogenic components used during the laboratory commissioning of the room temperature electronics presented in Section 4.

For the results presented in this paper, cryogenic readout electronics similar to those currently deployed with the SPTpol camera are used. A two-part manganin wire harness connects the SQUID controller board to a set of NIST series-array SQUIDs inside the cryostat at a temperature of 4 K. A stripline connects the SQUIDs to an SPTpol style LC board and a prototype SPTpol bolometer wafer. The bolometers are dark, i.e. isolated so that very little incident radiation is absorbed. The LC board is populated with chips of 22 µH inductors (also fabricated at NIST) and commercial capacitors. The capacitors are selected to give $LCR_{\text{bolo}}$ resonances equally spaced from 200 kHz – 5 MHz for the 38 working bolometers on the wafer. An additional six resonances are created by populating 1 Ω calibration resistors and the appropriate capacitors on the LC board.

These cryogenic components have two important parasitic contributions that can affect the stability and noise of TES bolometers. The first is the equivalent series resistance (ESR) of the capacitors in the $LCR_{\text{bolo}}$ filter. At frequencies less than 1 MHz, the ESR in the commercial capacitors is on the order of 0.1-0.3 Ω, small in comparison to the bolometer normal resistance ($\sim$ 1.5 Ω). However, ESR increases as a function of frequency. When the ESR is comparable to the bolometer normal resistance, the TES is no longer able to operate as deeply in the superconducting transition. The second parasitic of interest is the stray inductance in series with the bias resistor and that of the stripline. These strays alter both the amplitude of the voltage bias and associated noise level at the bolometer.

3. FLIGHT REPRESENTATIVE ELECTRONICS

TES detectors with SQUID-based multiplexed readout are an enabling technology for a new generation of space missions. These include, for example, the LiteBIRD mission and the SAFARI instrument on the SPICA mission. A second set of room temperature electronics (mezzanine and SQUID controller boards) were developed in collaboration with COM DEV Canada to be flight representative and demonstrate the technological suitability for satellite platforms (see Figure 6). A flight representative FPGA motherboard has not yet been developed as FPGA technology evolves rapidly and the requirements of an FPGA motherboard for a satellite application would be highly mission-specific. Consequently, the commissioning of the flight representative electronics used a Xilinx Kintex-7 FPGA evaluation board (model KC705) for the digital signal processing platform.

The general architecture for the flight representative electronics is the same as that described in Section 2 but space applications have additional design requirements, such as reduced power consumption and robustness to the environment. The digital fMux power budget is dominated by the fixed overhead in running the boards and the number of independent mux modules. A substantial reduction in power consumption per bolometer is
achievable by increasing the multiplexing factor to 64. Furthermore, the contribution of the generally power-hungry flight electronics components was offset by modifying the SQUID controller and part of the mezzanine design to use single rail supplies. Further power savings were made by allowing the software to dynamically scale down the reference current of the high speed DACs, which also enables fine tuning of the system gains. Overall, with the KC705 board and four modules of 64 bolometers each, we measure a power consumption of 48.9 mW per bolometer, which satisfies the LiteBIRD design goal of 50 mW per bolometer. Further reductions are possible with higher multiplexing factors.

The Flight Representative SQUID controller and mezzanine board have also been redesigned to operate in the environment of space. The first environmental consideration is radiation. Assuming a minimum mission lifetime of 2.5 years at the sun-earth L2 point, the electronics will experience a total ionizing dose of 50 krads under one millimeter of aluminum shielding. Electronic components with a radiation rating of 50-100 krads were selected. This required the use of the radiation-hardened Analog Device’s AD768 DAC to generate the carrier and nuller signal at >25 MSPS. The electronic components of both boards were chosen based on existing suitable flight parts with matching commercial versions with the same performance specification, circuit topology, and die layout. In most cases, the commercial versions of the components have been used on the boards as they differ from the flight counterparts only in terms of packaging and screening. The layout of the boards includes the area necessary to accommodate the larger packages of flight components, ensuring representative part spacing.

The range of temperatures over which the electronics will operate is another important environmental consideration. Assuming an approximately fixed attitude with respect to the Earth/Moon and the Sun and the thermal fluctuations in similarly oriented satellites, the digital fMux electronics should expect to experience slowly varying temperatures (~1°C per 24 hours) between 0°C and +40°C. Flight qualified components typically have a range of storage temperatures much larger than this, so no special component selection is required. To ensure that the readout system performance is not degraded as a function of ambient temperature, the flight representative mezzanine and SQUID controller boards were operated in a temperature controlled chamber at temperatures between -20°C to +40°C (in order to show margin against the likely future requirements). Both power consumption and noise decrease by about 10% as the temperature is reduced from +40°C to -20°C. The bias currents and references show excellent temperature stability and vary less than 1% over the full temperature range, which does not impact system operation. Similarly, the frequency response of the electronics changes by a few percent and does not affect system operation. Overall, the system performs well across the full temperature range, with a small benefit to operating at temperatures below 0°C.

A final environmental concern is the effect of electromagnetic interference (EMI) from the spacecraft electronics on the digital fMux electronics (specified by MIL-STD-461). The analog portion of the electronics on both the mezzanine and SQUID controller boards are sensitive to EMI from the digital portion, therefore it
is critical to self-shield (both in the ground-based and flight representative versions). The flight representative boards include bolt-down machined aluminum EMI enclosures with EMI gaskets.

4. SYSTEM PERFORMANCE

In this section we present the performance of the 64x digital fMux readout electronics with the full system, including the laboratory cryogenic components. The results shown equally represent the ground-based electronics controlled with the ICE motherboard and the flight representative versions that were evaluated using the KC705 evaluation board.

4.1 SQUID Operation

The performance of the SQUID controller is first evaluated on the benchtop. All DACs are exercised through a range of input values and the output voltage is measured. To ensure a 10 MHz bandwidth, the frequency response of the board is also measured. After passing the benchtop tests, the SQUIDs in the cryostat are operated through a range of bias currents and flux bias currents (Figure 7). The resulting voltage-flux curves have the expected sinusoidal shape and peak-to-peak amplitude.

![Figure 7. SQUID voltage response as a function of current through the SQUID input coil for a range of bias current values.](image)

Tuning the SQUID to the optimal bias point, we are able to measure the transimpedance (current to voltage gain) by injecting a small calibrated sinusoid on the nuller wires. Measuring the amplitude after demodulation, we find a transimpedance of approximately 383 Ω. This value is typical for these laboratory quality SQUIDs, and is comparable to the transimpedance measured with the previous digital fMux readout.

We also characterize the behavior of the analog low-frequency integral feedback loop. To achieve this, the SQUID is first tuned to the point on the voltage-flux curve with the maximum peak-to-peak response. The integral feedback is enabled and a pilot signal is injected on the nuller wires. The flux bias DAC is then scanned through a range of values, mimicking the effect of a changing external magnetic field. We find that the amplitude of the pilot signal has a maximum deviation from its mean amplitude of less than 1% while scanning through approximately 1/2 of the SQUID flux quanta.

4.2 Operation of 64 Channels

Before the bolometers can be operated in the superconducting transition, the specific location of the $LCR_{\text{bolo}}$ resonances must be known. We measure the frequency response of the cold electronics by injecting pilot signals on the carrier and nuller wires and measuring the output demodulated amplitude (see Figure 8). Signals are injected
simultaneously using all 64 readout channels, each at a different frequency, iterating until the full bandwidth of the system is probed. As stated in Section 2.4, the module shown here has 38 bolometers and an additional six resistors for a total of 44 resonances.

Bolometers are operated by first raising their physical temperature above that of the superconducting transition. At this temperature the bolometers behave like resistors. DAN feedback is enabled and voltage biases are applied to the bolometers (this is referred to as the overbiased state). The voltage biases are large enough to hold the bolometers normal while the physical temperature is lowered back to the base value below the transition temperature. The voltage biases are simultaneously reduced for all bolometers, slowly lowering them into the superconducting transition. Figure 9 shows the measured current through the bolometer as a function of decreasing voltage bias for three bolometers at different carrier frequencies. The linear current-voltage region at high bias voltage shows the normal regime of the bolometer that then transitions through a turnaround and into the superconducting transition at low bias voltage. Similarly, the resistance is shown to be approximately constant in the normal regime and then sharply decreases as the bolometer enters the superconducting transition.

Figure 8. Response as a function of frequency for a readout module containing 38 bolometers and six calibration resistors multiplexed together between 0 and 5 MHz.

Figure 9. Top row: Measured current as a function of voltage bias for three bolometers (low-, mid- and high-frequency resonance) as they are lowered into the superconducting transition. Bottom row: Bolometer resistance as a function of voltage bias for the same three bolometers.
We find a general trend that as carrier frequency increases the minimum stable fraction of the normal resistance at which the bolometer operates increases (it is biased higher in the superconducting transition). This is due to the known increase in capacitor ESR with frequency (see Section 2.4). Despite this behavior, we are able to successfully operate the 38 bolometers in the superconducting transition. To more closely approximate the conditions for operating 64 bolometers, the remaining 20 channels are set to off-resonance frequencies. These channels are used to simulate the total load on the nuller, carrier, and demodulator signal chains and can also be used to measure the properties of the readout electronics.

4.3 Noise Performance

TES bolometers have been demonstrated to achieve photon-noise-dominated performance. A key performance criterion for the 64x digital fMux readout is to contribute a negligible amount to total noise. We show the amplitude spectral distribution for a representative dark bolometer operated in the laboratory with a bias frequency of \( f = 1.24 \text{ MHz} \) in Figure 10. In the overbiased state, the bolometer behaves as a resistor with noise contributions from Johnson noise as well as from the warm and cold readout electronics. When operated in the superconducting transition, the bolometer has an additional contribution from phonon noise.

![Figure 10. Amplitude spectral density for a bolometer while overbiased (red) and while in the superconducting transition (black). A linear fit to the time domain data was removed prior to taking Fourier transform to remove a drift from the slowly changing physical temperature. Note that the white noise level (indicated by the dashed lines) increases as expected in the transition due to the phonon noise contribution.](image)

The white noise noise level increases significantly between the overbiased and in-transition state, indicating that the contribution of the readout electronics is subdominant. A few high-frequency lines are present in Figure 10 occupying approximately 5% of the total bandwidth. These lines are mostly outside the typical signal band (<30 Hz for a telescope with a one arcminute beam scanning at one degree per second). Ideally, we would also evaluate the noise as a function of bias frequency. However, the cryogenic components used with the room temperature electronics have known parasitic contributions that increase with frequency (see Section 2.4). Therefore, in this work we focus only on the lower frequency bolometers (<2 MHz) where the effect of these parasitics is less significant. At these frequencies, we measure the readout noise to be essentially independent of frequency. When the improved cryogenic components currently under development become available, we will evaluate the noise at higher frequencies.

5. CONCLUSION

We have presented room temperature electronics for the next generation digital fMux readout that multiplexes 64 bolometers together into a single SQUID module. These electronics include a SQUID controller, a mezzanine
interface board, and a FPGA motherboard. The system bandwidth is increased from the legacy system to \( \sim 10 \) MHz, allowing for additional \( LCR_{bolo} \) resonances. Digital Active Nulling (DAN) provides active feedback on the observed sky signal, reducing the dynamic range requirements of the SQUIDs. The digital synthesizer uses a novel polyphase filter bank approach to generate the carrier and nuller signals.

Flight representative versions of the SQUID controller and mezzanine boards were also developed. These boards were designed to operate in the environment of space, focusing in particular on high radiation tolerance and performance across a range of ambient temperatures. The boards were characterized in a temperature-controlled chamber from -20°C to +40°C. They performed well at all temperatures, and a small benefit was found to operating below 0°C. The boards were also designed to have low power consumption, a necessary criterion of space applications. For 64 detectors per readout module, we measure 49.8 mW per bolometer of power consumption for the flight representative electronics, which meets the LiteBIRD satellite design goal. Further power reductions are possible by increasing the multiplexing factor and by implementing the polyphase filter bank technique in the demodulator.

We demonstrate the ability of the new electronics to tune SQUIDs to their optimal operation point, bias detectors, and read out 64 channels per SQUID module. We have shown system performance using a test-module containing 44 bolometers and use the remaining 20 channels to characterize readout system noise. The sub-Kelvin electronics used for these tests has stray reactances that become important at several MHz, so we focus on detectors at 1-2 MHz. Parallel development and testing of new sub-Kelvin electronics is ongoing and these components will be available soon. Comparing the white noise levels of the bolometers while overbiased and while operating in the superconducting transition, we find that the contribution of the readout electronics to the total measured white noise level is small compared to the intrinsic bolometer noise.

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