An Improved Implementation of Grain

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Abstract—A common approach to protect confidential information is to use a stream cipher which combines plain text bits with a pseudo-random bit sequence. Among the existing stream ciphers, Non-Linear Feedback Shift Register (NLFSR)-based ones provide the best trade-off between cryptographic security and hardware efficiency. In this paper, we show how to further improve the hardware efficiency of Grain stream cipher. By transforming the NLFSR of Grain from its original Fibonacci configuration to the Galois configuration and by introducing a clock division block, we double the throughput of the 80 and 128-bit key 1bit/cycle architectures of Grain with no area penalty.

I. INTRODUCTION

Constrained environments applications such as hardware authentication devices (RFID, etc), smartcards, and wireless networks (Bluetooth, NFC, etc) require power-efficient, area-efficient and high-performance hardware encryption systems with large security margins. Until today, no adequate cryptographic solution has been proposed which satisfies the extreme limitations of devices like RFIDs [1]. Even the most compact of today’s encryption systems - Non-Linear Feedback Shift Register (NLFSR)-based stream ciphers - contain an order of magnitude more gates than can be dedicated for security functionality in the low-cost RFID tags [2]. The lack of adequate encryption mechanisms gives rise to many security and privacy problems and blocks off a variety of potential applications of RFIDs.

Motivated by these needs, in 2004-2008 the EU ECRYPT network carried out the eSTREAM project with the objective to identify the best stream ciphers designs [3]. Stream ciphers Grain-80 [4], Trivium [5], and Mickey-v2 [6] were selected as finalists for the hardware-oriented profile. Grain-80 with 1 bit/cycle throughput has the smallest hardware among all eSTREAM candidates, which makes it a particularly interesting case.

Grain-80 consists of one 80-bit LFSR [7], one 80-bit NLFSR [8], and a function combining selected state bits. The shift registers take almost 80 percent of the total area of the system and define its critical path. In this paper, we show that by transforming the shift registers of Grain from their original Fibonacci configuration to the Galois configuration, we can significantly improve its throughput. In the Fibonacci configuration of shift registers, the feedback is applied to the first bit of the register only. In the Galois configuration, the feedback can be applied to any bit. Thus, the depth of the circuits implementing feedback functions of the Galois configuration can potentially be smaller, leading to shorter propagation time and higher throughput.

However, unlike the LFSR case in which the mapping from the Fibonacci configuration to the Galois configuration is one-to-one, in the NLFSR case multiple Galois NLFSRs can be equivalent to a given Fibonacci one [9]. The problem of selecting a “best” Galois NLFSR for a given Fibonacci one is still open. One of the contributions of this paper is finding the minimal-throughput Galois configurations of NLFSRs for Grain-80 and Grain-128 [10]. Another contribution is the introduction of the clock division block which divides the clock frequency of Grain by two or four during the initialization phase. Without such a block, the potential benefits of the Galois configuration can not be utilized.

II. BACKGROUND

A. Definition of NLFSRs

A Non-Linear Feedback Shift Register (NLFSR) consists of $n$ binary storage elements, called bits. Each bit $i \in \{0, 1, \ldots, n - 1\}$ has an associated state variable $x_i$ which represents the current value of the bit $i$ and a feedback function $f_i : \{0, 1\}^n \rightarrow \{0, 1\}$ which determines how the value of $i$ is updated.

A state of an NLFSR is an ordered set of values of its state variables. At every clock cycle, the next state is determined from the current state by updating the values of all bits simultaneously to the values of the corresponding $f_i$‘s. The output of an NLFSR is the value of its 0th bit.

If for all $i \in \{0, 1, \ldots, n - 2\}$ the feedback functions are of type $f_i = x_{i+1}$, we call an NLFSR the Fibonacci type. Otherwise, we call an NLFSR the Galois type.

Two NLFSRs are equivalent if their sets of output sequences are equal.

B. The Transformation from the Fibonacci to the Galois Configuration

Let $f_i$ and $f_j$ be feedback functions of bits $i$ and $j$ of an $n$-bit NLFSR, respectively. The operation shifting, denoted by $f_i \rightarrow f_j$, moves a set of product-terms $P$ from $f_i$ to $f_j$. The index of each variable $x_k$ of each product-term in $P$ is changed to $x_{(k-i+j) \mod n}$.

The terminal bit $\tau$ of an $n$-bit NLFSR is the bit with the maximal index which satisfies the following condition: For all bits $i$ such that $i < \tau$, $f_i$ is of type $f_i = x_{i+1}$.

Definition 1: An $n$-bit NLFSR is uniform if the following two conditions hold:

(a) all its feedback functions are singular functions of type $f_i(x_0, \ldots, x_{n-1}) = x_{(i+1) \mod n} \oplus g_i(x_0, \ldots, x_{n-1})$,
where \( g_i \) does not depend on \( x_{(i+1) \mod n} \).

(b) for all its bits \( i \) such that \( i > \tau \), the index of every variable of \( g_i \) is not larger than \( \tau \).

**Theorem 1:** [9] Given a uniform NLFSR with the terminal bit \( \tau \), a shifting \( g_i = P \cdot g_{i'}, \tau' < \tau \), results in an equivalent NLFSR if the transformed NLFSR is uniform as well.

### III. The Description of Grain

There are two versions of Grain: 80-bit [4] key and 128-bit key [10]. Both consist of an LFSR, an NLFSR, and two combining functions.

In Grain-80 the shift registers are 80-bits. They are both the Fibonacci type, i.e. all bits except the 79th repeat the value of the previous bit. The feedback function of the 79th bit of the LFSR is given by:

\[
f_{79} = s_{62} \oplus s_{51} \oplus s_{38} \oplus s_{23} \oplus s_{13} \oplus s_0
\]

where \( s_i \) is the state variable of the \( i \)th bit, \( i \in \{0, 1, \ldots, 79\} \).

The feedback function of the \( i \)th bit of the NLFSR is given by:

\[
g_i = s_{60} \oplus b_0 \oplus b_{62} \oplus b_{60} \oplus b_{52} \oplus b_{45} \oplus b_{37} \oplus b_{33} \oplus b_{38} \\
\quad \oplus b_{21} \oplus b_{14} \oplus b_{9} \oplus b_{63} \oplus b_{60} \oplus b_{37} \oplus b_{33} \oplus b_{15} \oplus b_{60} \oplus b_{52} \oplus b_{45} \\
\quad \oplus b_{33} \oplus b_{25} \oplus b_{21} \oplus b_{63} \oplus b_{66} \oplus b_{60} \oplus b_{52} \oplus b_{37} \oplus b_{33} \oplus b_{63} \oplus b_{60} \oplus b_{21} \oplus b_{15} \\
\quad \oplus b_{63} \oplus b_{60} \oplus b_{25} \oplus b_{37} \oplus b_{33} \oplus b_{52} \oplus b_{45} \oplus b_{37} \oplus b_{33} \oplus b_{63} \oplus b_{60} \oplus b_{21} \oplus b_{15} \\
\quad \oplus b_{63} \oplus b_{60} \oplus b_{25} \oplus b_{37} \oplus b_{33} \oplus b_{52} \oplus b_{45} \oplus b_{37} \oplus b_{33} \oplus b_{63} \oplus b_{60} \oplus b_{21} \oplus b_{15}
\]

where \( b_i \) is the state variable of the \( i \)th bit, \( i \in \{0, 1, \ldots, 79\} \).

The first combining function of Grain-80 produces it output value based of the selected bits from the NLFSR and the LFSR:

\[
H = s_{25} \oplus b_{63} \oplus s_{36} \oplus s_{26} \oplus s_{13} \oplus s_{25} \oplus s_{66} \oplus s_{25} \oplus s_{26} \oplus s_{13} \oplus s_{66}
\]

The second combining function of Grain-80 generates the output stream of the system from the selected bits from the NLFSR and LFSR states and the output of \( H \):

\[
Z = \sum_{k \in A} b_k \oplus H,
\]

where \( A = \{1, 2, 4, 10, 31, 43, 56\} \).

For Grain-128, the corresponding functions are:

\[
\begin{align*}
f_{127} &= s_{68} \oplus s_{77} \oplus s_{88} \oplus s_{70} \oplus s_{81} \oplus s_{96} \\
g_{127} &= s_{60} \oplus b_0 \oplus b_{26} \oplus b_{26} \oplus b_{26} \oplus b_{56} \oplus b_{56} \oplus b_{56} \oplus b_{56} \oplus b_{56} \oplus b_{56} \oplus b_{56} \\
&\quad \oplus b_{17} \oplus b_{18} \oplus b_{27} \oplus b_{29} \oplus b_{40} \oplus b_{48} \oplus b_{61} \oplus b_{61} \oplus b_{61} \\
H &= b_{12} \oplus s_{13} \oplus s_{20} \oplus s_{25} \oplus s_{26} \oplus s_{60} \oplus s_{70} \oplus s_{25} \oplus s_{26} \oplus s_{60} \oplus s_{70} \\
Z &= \sum_{k \in A} b_k \oplus s_{93} \oplus H
\end{align*}
\]

where \( A = \{2, 15, 36, 45, 64, 73, 89\} \).

Before generating a stream of data, a cipher must be initialized with default keys. During the initialising phase the cipher does not produce any output for 160 clock cycles for Grain-80 and 256 cycles for Grain-128. The output of the \( Z \) function is XOR-ed with the outputs of LFSR and NLFSR and then fed into the inputs of both shift registers, as shown in Figure 1. After the initialization, the loops are opened and there is no feedback between the two shift registers.

It is possible to increase the throughput of Grain at the expense of extra hardware by introducing parallelism in its architecture. In parallelized versions of Grain, in each clock cycle blocks of duplicated NLFSR and LFSR feedback functions produce output bits in parallel. To allow for up to 16 (32) degrees of parallelization, Grain-80 (128) is designed so that the bits \( 65 < i < 79 \) (97 < \( i < 127 \)) of the shift registers are not used in the feedback functions or in the input to the combining functions.

### IV. Grain with Galois Configuration

Grain can be modified by transforming its LFSR and NLFSR from their original Fibonacci configurations to the Galois configurations. The transformation of LFSRs is done using standard techniques, in this section we only describe the transformation of NLFSRs.

The NLFSR of Grain-80 (128) can be transformed to the Galois configuration by shifting the product-terms of the feedback function of 79th (127th bit) to the feedback functions of bits with lower indexes. By Theorem 1 if the NLFSR after shifting satisfies the conditions of the Definition 1 then it produces the same sets of output sequences as the NLFSR before shifting.

Ideally, in order to maximize the throughput, we want to distribute the products equally among feedback functions. However, according to [9], to guarantee equivalence of NLFSRs before and after shifting, we cannot shift to bits with indexes lower that the bit \( \tau \) which is given by:

\[
\tau = \max (\max_{p \in P} (\max_{index(p)}(P) - \min_{index(p)}(P))),
\]

where \( P \) is the set of all product-terms of the feedback function of the Fibonacci NLFSR, and \( min_{index(p)}(P) (max_{index(p)}(P)) \) denotes the minimal (maximal) index of variables the product-term \( p \).

For Grain-80, the product-term with the maximal difference in indexes of variables is \( b_{63}b_{45}b_{26}b_{17}b_2 \), so \( \tau = 54 \). For Grain-128, we have \( \tau = 64 \) due to the product-term \( b_2b_{67} \).

However, in order to avoid modifications of the encrypting algorithm of Grain, we need to guarantee not only the equivalence of the sequences of output bits, but also the equivalence of the sequences of all internal bits of the NLFSR used by the combining functions. A modification of the encrypting algorithm could lead to undesirable changes in the Grain security. For Grain-80, the bit 63 of the NLFSR is used in the function \( H \), and bits 1, 2, 4, 10, 31, 43, 56 are used in the function \( Z \). Since 56 and 63 are greater than 54, we cannot use \( \tau = 54 \) as the terminal bit of the Galois configuration. We need to set the terminal bit to 63. Then, for all bits \( i \in \{0, 1, \ldots, 62\} \), the feedback functions will be of type \( g_i = b_{i+1} \), an the output sequences of the bits \( i \in \{1, 2, \ldots, 63\} \) will be the same as the output sequence of the bit 0 shifted in time. Consequently, the algorithm of Grain will not change.

For Grain-128, the bits 12 and 95 of the NLFSR are used in \( H \) and the bits 2, 15, 36, 45, 64, 73, 89 are used in \( Z \). Therefore, the terminal bit has to be 95.
After we have chosen the position of the terminal bit, we can start shifting products from the function $g_{79}(g_{127})$ to the functions with indexes larger or equal than the terminal bit. Shifting can be done in many different ways. At present there is no systematic technique which guarantees that the transformation produces an NLFSR with the minimal throughput for a given technology. We found the solutions presented below by trying many different choices.

A. One Bit per Cycle Version

According to our simulation results, the following Galois NLFSR results in the maximal throughput for 1bit/cycle version of Grain-80:

$$
g_{79} = s_0 \oplus b_0 \oplus b_{37}$$
$$g_{78} = b_{37} \oplus b_{44}$$
$$g_{77} = b_{78} \oplus b_{50}$$
$$g_{76} = b_{77} \oplus b_{57}$$
$$g_{75} = b_{76} \oplus b_{58}$$
$$g_{74} = b_{75} \oplus b_{32}b_{28}$$
$$g_{73} = b_{74} \oplus b_{3}$$
$$g_{72} = b_{73} \oplus b_{8}b_{2}$$
$$g_{71} = b_{72} \oplus b_{55}b_{37}b_{29}b_{1}$$
$$g_{70} = b_{71} \oplus b_{24}b_{19}b_{12}b_{6}b_{0}$$
$$g_{69} = b_{70} \oplus b_{53}b_{50}$$
$$g_{68} = b_{69} \oplus b_{49}b_{41}b_{26}b_{22}$$
$$g_{67} = b_{68} \oplus b_{9} \oplus b_{21}b_{10}b_{9}$$
$$g_{66} = b_{67} \oplus b_{15} \oplus b_{17}b_{39}b_{32}$$
$$g_{65} = b_{66} \oplus b_{0} \oplus b_{38}b_{31}b_{23}b_{19}b_{14}b_{7}$$
$$g_{64} = b_{65} \oplus b_{18} \oplus b_{48}b_{15}b_{16}b_{0}$$
$$g_{63} = b_{64} \oplus b_{17}b_{14}b_{36}b_{29}b_{21}$$

Here and further in this section, all omitted feedback functions are of type $g_i = b_{i+1}$.

For Grain-128, the maximal-throughput Galois NLFSR is:

$$g_{127} = s_0 \oplus b_0 \oplus b_{37}b_{67}$$
$$g_{124} = b_{125} \oplus b_0b_{64}$$
$$g_{116} = b_{117} \oplus b_0b_2$$
$$g_{110} = b_{111} \oplus b_0b_1$$
$$g_{102} = b_{103} \oplus b_1$$
$$g_{101} = b_{102} \oplus b_0$$
$$g_{100} = b_{101} \oplus b_{63}$$
$$g_{99} = b_{100} \oplus b_{63}$$
$$g_{98} = b_{96} \oplus b_{27}$$
$$g_{97} = b_{98} \oplus b_{38}b_{54}$$
$$g_{96} = b_{97} \oplus b_{38}b_{34}$$
$$g_{95} = b_{96} \oplus b_{8}b_{16}$$

B. Multiple Bit per Cycle Version

We can extend the theory presented in [9], [11] to $k$ bits/cycle versions of Grain by restricting bit positions to which the feedback can be applied. It is easy to see that, to ensure times $k$ degree of parallelization of an $n$-bit Galois NLFSR with the terminal bit $\tau$, all bits except

$$n - 1 - i \cdot k$$

for all $i = \{0, 1, \ldots, \lfloor (n - 1 - \tau)/k \rfloor - 1\}$ should have feedback functions of type $g = b_{i+1}$.

So, for example, for 4 bits/cycle version of Grain-80, we can apply feedback to the bits 79, 75, 71 and 67:

$$g_{79} = s_0 \oplus b_0 \oplus b_{52} \oplus b_{33} \oplus b_{28} \oplus b_{21} \oplus b_{15}b_9$$
$$\oplus b_{25}b_{15}b_{37}b_{33}b_{28}b_{21}$$
$$g_{75} = b_{76} \oplus b_{41} \oplus b_{33} \oplus b_5 \oplus b_{56}b_{56} \oplus b_{33}b_{29} \oplus b_{59}b_{41}b_{24}b_{5}$$
$$g_{71} = b_{72} \oplus b_{44} \oplus b_{25}b_{26}b_{13}b_7 \oplus b_{25}b_{26}b_{13}b_7b_1$$
$$g_{67} = b_{68} \oplus b_{48} \oplus b_2 \oplus b_4b_{10}b_{14} \oplus b_{14}b_{40}b_{25}b_{21}$$
$$\oplus b_{11}b_{18}b_{40}b_{33}b_{25}$$

For 8 bit/cycle version of Grain-80, we can apply feedback to the bits 79 and 71:

$$g_{79} = s_0 \oplus b_0 \oplus b_{14} \oplus b_0 \oplus b_{15}b_9 \oplus b_{60}b_{52}b_{45} \oplus b_{13}b_{28}b_{21}$$
$$\oplus b_{60}b_{62}b_{37}b_{33}b_{33}b_{30}b_{21}b_{15} \oplus b_{33}b_{26}b_{21}b_{15}b_9$$
$$g_{71} = b_{72} \oplus b_{44} \oplus b_{37} \oplus b_{29} \oplus b_{25} \oplus b_{20} \oplus b_{13} \oplus b_{65}b_{52}$$
$$\oplus b_{64} \oplus b_{29}b_{25} \oplus b_{55}b_{37}b_{20}b_{1} \oplus b_{55}b_{52}b_{44}b_{37}b_{29}$$
$$\oplus b_{44}b_{37}b_{29}b_{25}b_{20}b_{13}$$

For 16 bit/cycle version of Grain-80, we can apply feedback only to the bit 79, i.e. no transformations can be done.

For 4 bit/cycle version of Grain-128, we can apply feedback to the bits 127, 123, 119, 115, 111, 107, 103 and 99:

$$g_{127} = s_0 \oplus b_0 \oplus b_{38}b_{67}$$
$$g_{123} = b_{24} \oplus b_{64}b_{80}$$
$$g_{119} = b_{120} \oplus b_5$$
$$g_{115} = b_{126} \oplus b_{60}b_{53}$$
$$g_{111} = b_{112} \oplus b_2$$
$$g_{107} = b_{108} \oplus b_8 \oplus b_{76}$$
$$g_{103} = b_{104} \oplus b_{67} \oplus b_3b_{35}$$
$$g_{99} = b_{100} \oplus b_2 \oplus b_{12}b_{20}$$

For 8 bit/cycle version of Grain-128, we can apply feedback to the bits 127, 119, 111, 103:

$$g_{127} = s_0 \oplus b_0 \oplus b_{56} \oplus b_3b_{67}$$
$$g_{123} = b_{120} \oplus b_8 \oplus b_{88} \oplus b_3b_5$$
$$g_{111} = b_{112} \oplus b_{75} \oplus b_2 \oplus b_{52}b_{68}$$
$$g_{103} = b_{104} \oplus b_3b_{35} \oplus b_{10}b_{24} \oplus b_{37}b_{41}$$

For 16 bit/cycle version of Grain-128, we can apply feedback to the bits 127 and 111.

$$g_{127} = s_0 \oplus b_0 \oplus b_{56} \oplus b_3b_{67} \oplus b_{11}b_{13} \oplus b_{40}b_{48}$$
$$g_{111} = b_{112} \oplus b_{10} \oplus b_{75} \oplus b_{80} \oplus b_1b_2 \oplus b_{11}b_{43} \oplus b_{45}b_{49}$$
$$\oplus b_{52}b_{68}$$

For 32 bit/cycle version of Grain-128, we can apply feed-back only to the bit 127, i.e. no transformations can be done.

C. Design Details

By transforming Grain’s shift registers to the Galois configuration as described in the previous section, we can obtain up to 40 % reduction in their propagation time. However, the clock frequency of the overall Grain system improves only about 10%. The problem is in the hardware architecture of Grain during key initialization, during which the output value of $Z(x)$ is fed back to the LFSR and NLFSR making two loops, as shown in Figure 1. After the transformation from the Fibonacci to the Galois configuration, due to the reduction of the critical path in the NLFSR, the critical path of the system
is no longer in the NLFSR but is in the initialization loops, which are closed only during initialization. Thus, the highest frequency that the system supports during initialization is lower than the highest frequency supported during key stream generation (see Table I).

![Fig. 1. Initialization loops Grain](image1)

**TABLE I**

| Galois Grain-80 Block Size | Maximum Clock Frequency |
|---------------------------|-------------------------|
| 1 bit/cycle               | 1 (GHz) 4 (GHz)         |
| 4 bits/cycle              | 1 (GHz) 2.7 (GHz)       |
| 8 bits/cycle              | 1 (GHz) 2.3 (GHz)       |

![Fig. 2. Clock divider by four](image2)

To obtain a higher improvement in the throughput of Grain, we introduce a clock division block to divide the frequency of the clock during the initialization phase. The clock divider is realized as a simple block containing one or two D-flipflops which divides the clock frequency of the system by 2 or 4. In Figure 2, we show the structure of the clock division block for division of the clock frequency by 4. In some versions of Grain, division by 2 is sufficient to ensure correct operation during the initialization phase. Division by 3 would be suitable in some cases, but it would overcomplicate the hardware for only a modest speedup of the initialization phase. The clock division block is a very small component. Clock division by four gives area overhead of 25.67 GE and negligible power consumption.

![Fig. 3. Grain with Galois configuration and clock divider by four](image3)

Grain always moves from the slower to the faster clock frequency and the run signal is set internally by the counter on the positive edge of the clock. Because of the delay in the production of the run signal, the first clock cycle of the key generation phase will be shortened, which could potentially lead to critical path violations in a performance-optimized design such as Grain. We can handle this problem by using a flip-flop in front of the run signal which is output by the counter. In this case, if the run signal rises to 1 after a positive edge of the faster clock signal, the clock of the system changes to the faster clock in the next positive edge of the system. This solution is shown in Figure 4.

![Fig. 4. A: delay between positive edges of two clocks. B: delay between run signal and high frequency clock. C: shortened clock](image4)

**V. EXPERIMENTAL RESULTS**

We have synthesized the Fibonacci and the Galois versions of Grain using Cadence RTL compiler in the TSMC 90nm standard cell technology library. Since the synthesis tool does not handle multiple clocking, we set the two initialization loops as false paths and optimized the designs for the key-generation phase.

Table II shows the results for throughput, power consumption, area, and frequency. Area is measured in terms of NAND2 Gate Equivalents (GE). The total power consumption of the system is estimated as a combination of dynamic and leakage power for operation at 25 C, with a power supply of 1.2 V at 10MHz clock frequency as in [2].

As we can see, the throughput for Galois 1bit/cycle Grain-80 and Grain-128 is more than doubled compared to Fibonacci. Trivium is the highest ranked finalist in the eSTREAM project. In Table III, we compared the frequency and area of Trivium (T) and Grain-80 with Galois configuration (G). Both ciphers were implemented in TSMC 90 nm technology. Due to the Galois configuration, Grain-80 (1bit/cycle) is faster and smaller than Trivium (1bit/cycle), with a significantly better throughput/area ratio. This is an important result for applications such as RFID systems which require efficiency in both throughput and area. The throughput/area figures are compared graphically in Figure 5, where the figures for the Fibonacci configuration (Grain(F)) of Grain-80 are also reported.

**VI. CONCLUSION**

In this paper, we presented an improved version of the Grain stream cipher. We found new implementations for its
### TABLE II

**Synthesis results for Galois and Fibonacci configurations of Grain in TSMC 90nm technology**

| Cipher    | Block Size | Frequency (GHz) | Area (GE) | Power (mW) | Throughput (Gbit/Sec) |
|-----------|------------|-----------------|-----------|------------|------------------------|
|           |            | Galois          | Fibonacci |            |                        |
|           |            | Fib. impr.      | Fib. impr.|            |                        |
| Grain-80  | 1          | 4               | 1.9       | 1772       | 0.035                  | 4                      |
|           |            | 4               | 2.7       | 2471       | 0.095                  | 2                      |
|           |            | 8               | 2.3       | 3575       | 0.127                  | 8                      |
| Grain-128 | 1          | 4               | 2.7       | 2207       | 0.12                    | 4                      |
|           |            | 4               | 3.5       | 3021       | 0.13                    | 3                      |
|           |            | 8               | 3.2       | 3902       | 0.15                    | 2                      |
|           |            | 16              | 2.7       | 5346       | 0.20                    | 32                     |

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NLFSRs which generate the same cryptographically strong pseudo-random bit sequences as the ones of the original Grain, but have a better hardware efficiency. The presented technique is general and can be applied to any NLFSR-based stream cipher. Its efficiency depends on the feedback function of the NLFSR and the desired degree of parallelization. For Trivium the presented technique brings no improvement.

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