Comprehensive Analysis of Quantization Effects on Digital-Controlled Adaptive Self-Interference Cancellation System

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ABSTRACT A digital-controlled adaptive self-interference cancellation system with capabilities of high interference cancellation ratio and strong environmental applicability is presented. The key part - analog-to-digital converter (ADC) / digital-to-analog converter (DAC) quantization effect, is analysed comprehensively. Specially, the analytical relation between the quantization noise and the interference cancellation ratio is derived, which can provide important guidance for system implementation and performance optimization. The theoretical deductions are validated firstly by Simulink simulation and then by practical experimental measurements. Both the analysis and experiments show that the system stability and convergence property are not affected by ADC/DAC. The magnification of the conditioning circuit in front of the error-sampled ADC plays an important role in the cancellation ratio improvement. The practical space channel measurements presented an average interference cancellation ratio of 59 dB for the single-tone interference waveform and 50 dB for the amplitude-modulated (AM) interference waveform, rendering the system as a powerful tool for solving the in-band self-interference problem.

INDEX TERMS adaptive, self-interference, quantization, ADC, DAC.

I. INTRODUCTION
The growth in wireless communications necessitates more efficient utilization of spectrum, especially for the space-limited ship, vehicle, aircraft environments [1]–[3], where multiple type and multiple frequency band of communication systems are co-site placed. That includes the High Frequency (HF, 3-30MHz), Very High Frequency (VHF, 30-300MHz), Ultra High Frequency (UHF,300-3000MHz) and satellite transceivers. In some cases, several transceivers in the same frequency band are required to operate simultaneously, e.g., eight VHF radios are required in Expeditionary Fighting Vehicle [2]. Due to the limited space isolation between transmitter (TX) and receiver (RX) antennas and the non-ideal properties of the high power amplifier, part of the strong TX power (i.e. 100W ~ 1000W in HF band), can be coupled into the sensitive receiver passband, potentially jamming or even damaging the receiver.

The adaptive interference cancellation system (AICS) based on vector modulation principle is an attractive approach to tackle the co-site self-interference (SI) problem [4], [5] and has been used in practical shipboard HF/UHF communications [6]. Besides, the AICS is actually a one-tap analog least mean square loop [7], which can serve as an effective analog method to suppress the self-interference in radio frequency (RF) domain. AICS can also be potentially employed in full-duplex relaying [8], generalized continuous wave synthetic aperture radar [9] and military electronic warfare [10]. The AICS cancels the interference by taking a reference of the strong transmit signal and adjusting the amplitude and phase, so that it exactly composes an amplitude-matched and phase-reversed cancel signal to null out the self-interference at the receiver [6]. The traditional approach to implement AICS is based on analog circuits [4], [5], [7], [11] which encounters analog intrinsic shortcomings including /Q imbalance [12], time delay mismatch [5], correlator zero-point temperature drift [13], low control stability, poor component parameter consistency and so on. Our previous paper [14] proposed a new digital-controlled interference cancellation structure to overcome the shortages of the analog cancellation system with its internal diagram shown in Fig.1. The main idea was to implement the correlating operation and weight coefficient...
Updating operation inside the digital circuits like Field Programmable Gate Array (FPGA), meanwhile reserving the reference modulation implemented by the analog components, namely the electrically tuned attenuator, orthogonal splitter, power combiner and the like. The main advantage of the structure is that it can reserve the capacity of the analog components for handling high-power jamming interference (HF, SI>30 dBm; VHF, SI>16 dBm), and also make full use of the digital circuit characteristics like the immunity to environmental temperature vibration, the relatively higher loop gain setting limit, the convenience to algorithm implementation and updating. Therefore, stronger practicality can be anticipated.

However, regarding the key part of the new structure – digital quantization effects, specially the ADC/DAC quantization noise impact, there so far has not been a comprehensive theoretical quantitative research [14]–[17], resulting in some blindness on the system design and optimization. Our previous papers carried on the research mainly through simulation [14], [15] or only focused on DAC noise [16]. Korpi et al. [17] introduced down-converters and ADC/DAC circuits to implement the correlation in the digital baseband, but the quantization noise impact was not mentioned. Korpi et al. [18] also performed ADC analysis in the full-duplex ratio, but not focused on the digital-controlled structure. As shown in Fig. 1, three ADCs are introduced to acquire the references and error signal. The relatively large quantization noise induced by limited ADC resolution can worsen the sampled SNR, probably incurring system performance deterioration in terms of cancellation speed and cancellation ratio.

Two DACs output weighting signals to control the amplitude and phase of I/Q reference signal, and its quantization noise can be injected directly into the receiver. In some cases, serious problems such as noise floor increase and sensitivity degradation of the receiver can be raised when the system parameters are not selected appropriately. For instance, in LTE systems, the typical receiver sensitivity is -88.9 dBm [18], which corresponds to 21.6 μVpp at 50 Ω load. In order to avoid deteriorating the receiver sensitivity, the residual self-interference power should be smaller than that. If ADC is adopted to directly sample the residual interference signal without system parameter optimization, the required minimum quantization level is 7.2 μV (=21.6 μV/3) according to [19]. The resulting resolution is 18.08 bit for ADCs with the full-range of 2 Vpp. However, the achievable converter resolution is limited within 16-bit if the sampling rate is beyond 50 Msps. In the case, ADC may become the system bottleneck. Actually, the quantization noise analysis is one important research object in the self-interference cancellation research field as indicated in [18]. Considering the importance of the ADC/DAC noise analysis, this paper provides a comprehensive theoretical analysis of the quantization effects on the self-interference cancellation system. The main purpose of the analysis is to understand the working mechanism of the quantization effect in depth, research the lower and upper performance boundary of the new structure, and master the parameter optimization method. At last, the guideline for ADC/DAC selection and other parameter setting can be deduced for the practical system implementation.

Contributions of this paper are summarized as follows: (1) it provides an analytical mean to investigate the impact of the converter quantization noise on the performance of the AICS in terms of convergence property, stability, interference cancellation ratio. (2) it derives the analytical relation between the converter quantization noise and interference cancellation ratio, which is critical from the system design perspective. The relation provides a reference for evaluating the AICS performance under ADC/DAC imperfections and also determining how to choose proper ADC/DAC and other model parameters. For instance, we find that the low resolution of 6-bit is sufficient for the reference sampling ADCs, but the high resolution ADC beyond 12-bit should be adopted to sample the error signal. A high-dynamic auto gain control (AGC) circuit is highly desirable to be placed in front of the error-sampling ADC. Besides, the DAC noise is not serious provided that the updating frequency is much higher than the receiver bandwidth. (3) it provides not only simulation but also experimental results to validate the theoretical analyses. Both the results are consistent with the theoretical ones. Measured results showed that the average ICR of 65.86 dB, 59 dB and 50 dB could be achieved by the prototype demonstrator for the case of attenuator coupling channel with the single-tone waveform, real space channel with single-tone waveform and AM waveform, receptively.

The rest of this paper is organized as follows. The system model is introduced briefly and the performance analytical expressions under cases of the ideal, ADC included and DAC included are deduced in detail in Section II. In Section III, numerical simulation based on Simulink is presented and the main discussions are included. The practical performances of the digital-controlled system are assessed in hardware, and the correctness the theoretical deduction and the practicability of the system are further proved in Section IV. The conclusion is shown in Section V.
II. SYSTEM MODELLING AND ANALYSIS

A. ANALYSIS MODEL

The block diagram representing the analysed AICS system is given in Fig.1. AICS is simply divided into two parts: the analog vector modulator and the digital correlator. The analog vector modulator contains the relevant components to compose the cancellation signal. The weight generation related components such as ADCs/DACs are grouped into the digital correlator part.

Denoting the RF transmitting signal after HPA as \( x(t) \) and its equivalent baseband signal as \( x_i(t) \), we have \( x(t) = Re[x_i(t)e^{j2\pi f_c t}] \), where \( f_c \) is the carrier frequency. Generally, the AICS is suitable for cancelling the line-of-sight (LoS) narrow band interference \[4\], this is, \( x(t) \) can be expressed as \( A\cos(2\pi f_c t + \theta) \), resulting in \( x_i(t) = Ae^{j\theta} \).

A directional coupler is adopted to couple part of the reference signals and the error signal in order to obtain the weight coefficients for the electrically tuned attenuators. The transfer function in Laplace domain of the LPF is \( H(s) = a/(s + a) \).

The weight coefficient updating equation for Channel I is:

\[
\frac{d\omega_i(t)}{dt} + a\omega_i(t) = ak_a k_i k_d k_f e(t)Re\{\xi_i(t)e^{j2\pi f_c t}\}
\]  

Similarly, Channel Q has:

\[
\frac{d\omega_q(t)}{dt} + a\omega_q(t) = ak_a k_i k_d k_f e(t)Im\{\xi_i(t)e^{j2\pi f_c t}\}
\]

B. PERFORMANCE ANALYSIS UNDER THE IDEAL CASE

For the ideal case, the sampling, quantization and digitization processes induced by ADC/DAC in Fig.1 are ignored.

As shown in Fig.1, two one-order low pass filters (LPFs) are introduced to implement the correlation process between the reference signals and the error signal in order to obtain the weight coefficients for the electrically tuned attenuators. The transfer function in Laplace domain of the LPF is \( H(s) = a/(s + a) \).

The weight coefficient updating equation for Channel I is:

\[
\frac{d\omega_i(t)}{dt} + a\omega_i(t) = ak_a k_i k_d k_f e(t)Re\{\xi_i(t)e^{j2\pi f_c t}\}
\]

Similarly, Channel Q has:

\[
\frac{d\omega_q(t)}{dt} + a\omega_q(t) = ak_a k_i k_d k_f e(t)Im\{\xi_i(t)e^{j2\pi f_c t}\}
\]

Considering \( w(t) = w_i(t) + jw_q(t) \) and assigning \( \rho = k_a k_i k_d k_f \), we have:

\[
\frac{d\omega(t)}{dt} + a\omega(t) = a\rho e(t)\xi_i(t)e^{j2\pi f_c t}
\]

For the simplest passive RC implementation of LPF, \( a \) is the cut-off angular frequency with value of \( 1/(RC) \). The weighting coefficient \( w(t) \) can be solved by executing the convolution of the input signal \( \rho e(t)e^{j2\pi f_c t} \) with the LPF impulse response of \( ae^{-at}e^{j\omega_c t} \). \( e(t) \) is the step function with value of 1 for \( t \geq 0 \) and 0 for \( t < 0 \): we have:

\[
w(t) = \rho a \int_{-\infty}^{+\infty} e^{-at-\tau}e^{j\omega_c \tau}e^{j2\pi f_c \tau} (e(t) - \tau) d\tau
\]

Substituting \( e(t) \) shown in (3) into (7), we can get another \( w(t) \) form shown in (8). In the derivation, the cut-off frequency \( f_{cut} \) of the LPF is practically far smaller than the carrier \( f_c \), i.e. \( f_{cut} < f_c \), so that the signals mixed by \( 2f_c \) carrier are considered to be totally eliminated.

\[
w(t) = \rho a \int_0^t e^{-at-\tau}Re\{[(h - k_a k_b w(t))^* x_i(\tau) + s_j(\tau)]e^{j2\pi f_c \tau}\} d\tau
\]

\[
\frac{1}{2} a \rho a \int_0^t e^{-at-\tau}Im\{[(h - k_a k_b w(t))^* x_i(\tau) + s_j(\tau)]e^{j2\pi f_c \tau}\} d\tau
\]

\[
\int x_i(\tau) e^{j2\pi f_c \tau} d\tau
\]

By assigning \( u(t) = h - k_a k_b w(t) \) and after simple algebraic rearrangement, (8) can be expressed as:

\[
u(t) = h - \frac{1}{2} k_a k_b a \int_0^t e^{-at-\tau}|u(t)x_i^*(\tau) + s_j^*(\tau)|x_i(\tau) d\tau
\]
Rewriting (9) as \( u(t) = h - \frac{1}{2} k_a k_b \rho a e^{-at} \int_0^t e^{at} \left[ u(\tau) s_1^2(\tau) + s_1^2(\tau) \right] d\tau \), and taking the derivation with respect to \( t \) on both sides, we have:

\[
\begin{align*}
\frac{du(t)}{dt} &= \frac{1}{2} k_a k_b \rho a e^{-at} \int_0^t e^{at} \left[ u(\tau) s_1^2(\tau) + s_1^2(\tau) \right] d\tau \\
&= -\frac{1}{2} k_a k_b \rho a e^{-at} \left[ u(t) s_1^2(t) + s_1^2(t) \right] x_1(t) \\
&= a[h - u(t)] - \frac{1}{2} k_a k_b \rho a [u(t) s_1^2(t) + s_1^2(t)] x_1(t) 
\end{align*}
\]

(10)

After simple algebraic rearrangement, (10) can be written as:

\[
\frac{du(t)}{dt} + [a + \frac{1}{2} k_a k_b \rho x_1^2(t) x_1(t)] u(t) = ah - \frac{1}{2} k_a k_b \rho a s_1^2(t) x_1(t) 
\]

(11)

In general, the solution to the first-order differential equation \( dy/dt + P(t) y = Q(t) \) can be expressed as \( y = Ce^{-\int P(t)dt} + e^{-\int P(t)dt} \int Q(t)e^{\int P(t)dt}dt \) \[20\], where \( C \) is a constant. For the case of (11), \( P(t) = a[1 + \frac{1}{2} k_a k_b \rho x_1^2(t) x_1(t)] = a(1 + \frac{1}{2} k_a k_b \rho A^2) = aL \), \( Q(t) = ah - \frac{1}{2} k_a k_b \rho a s_1^2(t) x_1(t) \), where \( L = (1 + \frac{1}{2} k_a k_b \rho A^2) \). Therefore, the solution of (11) is:

\[
\begin{align*}
u(t) &= Ce^{alL} + \frac{e^{-alL}}{aL} \int_0^t ahe^{-alL} d\tau - \frac{1}{2} k_a k_b \rho a e^{-alL} x_1(t) s_1^2(t) x_1(t) d\tau \\
&= \frac{h}{L} + \frac{(h - \frac{1}{2} k_a k_b \rho a e^{-alL})}{L} e^{-alL} + u_0(t) 
\end{align*}
\]

(12)

where \( u_0(t) = -\frac{1}{2} k_a k_b \rho a e^{-alL} \int_0^t s_1^2(t) x_1(t) e^{alL} d\tau \). For the initial value assignment of \( w(0) = 0 \), the value of \( u(0) \) can be easily deduced to be \( h \). Substituting it to (12), we have the constant \( C \) to be \( h \). Therefore, \( u(t) \) can be rewritten as:

\[
\begin{align*}
u(t) &= \frac{h}{L} + \frac{h(L - 1)}{L} e^{-alL} + u_0(t) 
\end{align*}
\]

(13)

Rewriting \( e(t) \) in (3) as \( Re\{u^*(t)x_1(t) e^{\pi f_2 t} \} + s(t) \), the expression of \( e(t) \) can be rewritten accordingly as:

\[
\begin{align*}
e(t) &= \frac{Re\{h^*x_1(t) e^{\pi f_2 t} \}}{L} + \frac{L - 1}{L} e^{-alL} Re\{h^*x_1(t) e^{\pi f_2 t} \} \\
&= Re\{a(L - 1)e^{-alL} \int_0^t s_1(t) e^{alL} d\tau e^{\pi f_2 t} \} + s(t) 
\end{align*}
\]

(14)

From (14), we can make the following observations.

1) The 1st item on the right-hand side of the equation represents the stable residual interference after the cancellation when considering \( z(t) = Re\{h^*x_1(t) e^{\pi f_2 t} \} \). Clearly, the amplitude of the interference is attenuated by \( L \) times. Here, the interference cancellation ratio (ICR) is introduced as an important performance assessment criteria for AICS, which is defined as the power difference in \( dB \) of the spurious signals falling into the receiver passband before and after cancellation in the stable state. The power of the self-interference before cancellation is \( P_{b0} = 1/2E[|h^*x_1(t)|^2] = 1/2A^2|h|^2 \), while the power after cancellation is \( P_{af} = 1/2A^2|h|^2/L^2 \). Accordingly, ICR is calculated as:

\[
ICR = 10\log_{10}(P_{b0}/P_{af}) = 20\log_{10}L 
\]

(15)

2) The cancellation speed of the self-interference signal is jointly determined by the parameters \( a, L \) as they appear in the exponentially decreasing part \( e^{-alL} \).

3) Let the desired signal pass through the cancellation loop, we can get the 3rd right-hand side item. The part of \( e^{-alL} \int_0^t s_1(t) e^{alL} d\tau \) is actually the convolution result of \( s_1(t)e^{\pi f_2 t} \) with \( e^{-alL}e^{\pi f_2 t} \), and can be resolved to be \( A_s(e^{-alL} - e^{2\pi f_2 t} e^{\pi f_2 t})/(aL + j2\pi \Delta f) \) by using Laplace transforms and inverse transforms. Noted that \( s_1(t) = A_s e^{2\pi \Delta f t} \) is used in the derivation.

Therefore, the 3rd item can be rewritten as \( a(L - 1)Re\{A_s e^{-alL} - A_s e^{2\pi \Delta f t} e^{\pi f_2 t} \} \). Combing the stable part of the new 3rd item with the 4th item, the desired signal after cancellation can be calculated as \( A_s cos(2\pi (f_c + \Delta f) t + \phi)/sqrt(1 + a^2 L^2/(4\pi^2 \Delta f^2)) \) for \( L \gg 1 \), where \( \phi = arctan(aL/(2\pi \Delta f)) \). It is easy to see that the amplitude attenuation of the desired signal \( s(t) \) is jointly determined by the parameters \( a, L, \) and \( \Delta f \).

Here, the desired signal cancellation ratio (SCR) \[4\] is defined as the stable power difference of the desired signal in \( dB \) before and after the cancellation process, and can be calculated as:

\[
SCR = 10\log_{10}(1 + a^2 L^2/(4\pi^2 \Delta f^2)) 
\]

(16)

C. PERFORMANCE ANALYSIS WITH ADC QUANTIZATION NOISE

As shown in Fig.1, three ADCs are adopted to acquire the in-phase reference, quadrature reference and error signals, and are denoted as ADC1, ADC2, ADC3, respectively.

The quantization noise for the uniform scalar quantizers \[21\] is usually assumed uncorrelated and additive to the input signal with the mean value of 0 and average power of \( q^2/12 \).

That assumption holds on condition that the acquiring signal has a dynamic range coverying as few as three quantum levels (denoted as \( q \)) \[19\]. In the case, the quantization noise can be regarded as the white uniform noise \[21, 22\], whose power density spectrum spreads uniformly over Nyquist bandwidth from \(-f_s/2 \) to \( f_s/2 \), \( f_s \) is the sampling frequency of ADC. Otherwise, the probability density distribution of the quantization noise is not necessarily uniformly distributed and the additive noise model is not accurate \[19\].

In practical system, the resolution of ADC is at least 8 bits. Therefore, the condition for the additive quantization noise model is easily satisfied for ADC1 and ADC2, because the reference signals usually have relatively bigger dynamic range than the ADC quantum level in order to gain high ICR.

However, the condition is not always met for ADC3 because the error signal would gradually decrease after the cancellation process begins.

For the case of the additive quantization noise model satisfied, the signals after ADC1, ADC2 and ADC3 become
\( x_a(t) = k_x x(t) + n_i(t) \), \( x_g(t) = k_x x(t) + n_g(t) \), \( x_c(t) = k_x x(t) + n_i(t) \). Noted that the performance of the sampled-data systems is still analysed by employing the same signal representation with the ideal continuous system by ignoring the sampling effect, which is in accordance with [19]. Meanwhile, the quantization noise of DAC is ignored. In the case, (6) can be rewritten as:

\[
\frac{dw(t)}{dt} + aw(t) = a_\rho e(t)x(t)e^{2\pi f_s t} + ak_b k_w e(t)n_{iq}(t) + a_\rho x(t)e^{2\pi f_s t} x(t)\frac{n_{id}(t)}{k_e} + ak_b k_w e(t)n_{iq}(t)
\]

where \( n_{id}(t) = n_i(t) + jn_q(t) \). Considering the relatively smaller amplitude of the \( e(t) \), \( n_i(t) \) and \( n_{iq}(t) \) in the stable state after the cancellation process, the 2nd and 4th items of the right side equation can be safely ignored. After similar process with (7) and (8), we obtain a new formula of \( w(t) \) shown as:

\[
w(t) = \frac{1}{2} \rho a \int_0^t e^{-a(t-\tau)} [e(t) x(t) + s(t)] x(t) d\tau + ak_b k_w e(t)n_{iq}(t) \int_0^t e^{-a(t-\tau)} x(t) e^{2\pi f_s \tau} n_e(\tau) d\tau
\]

where \( u(t) = h - k_b w(t) \).

Following the same process with (9), (10) and (11), we have:

\[
\frac{du(t)}{dt} + au(t) = ah - \frac{1}{2} k_b k_w a_\rho \int_0^t e^{-a(t-\tau)} [e(t) x(t) + s(t)] x(t) d\tau + ak_b k_w e(t)n_{iq}(t)
\]

Compared with (11), the equation has an additional term of \(-ak_b k_w e(t)n_{iq}(t)\frac{n_{id}(t)}{k_e} \) which is introduced by ADC acquisition process.

After implementing further similar manipulations with (12), (13) and (14), the final error signal can be expressed as:

\[
e(t) = \frac{1}{2} a L e^{aL} + \frac{2}{L} e^{-aL} \Re[h^* x(t) e^{2\pi f_s t}] - \Re[\frac{a L}{k_e} \int_0^t s(t) e^{aL} d\tau] + s(t) + \Re[\frac{2}{k_e} \frac{L-1}{L} e^{-aL} \int_0^t n_e(\tau) e^{aL} e^{-aLt - 2\pi f_s t} d\tau] + e^{2\pi f_s t}
\]

Compared (20) with (14), we can obtain some observations under the case of the additive quantization noise model satisfied for ADC3.

1) SCR, loop stability and convergence speed are not affected by ADC quantization noise as the front four right-side items are not changed.

2) The additional last item represents the noise induced by the ADC3. The exact analytic expression of the noise power is hard to obtained because of its \( R \) (insert) operation. However, the power of the variable inside the \( \Re(\cdot) \) symbol, denoted as \( n'_e(t) \), can be easily obtained. \( n'_e(t) \) can be regarded as the output of the linear system with the transfer function of \( \frac{2L-1}{k_e(\frac{k}{2} L + aL - 2\pi f_s t)} \) and the input \( n_e(t) \). Supposing the quantization noise \( n_e(t) \) with the power spectrum density of \( N_q \) within the frequency band of \([-f_s/2, f_s/2]\), we have \( N_q = q^2/(12f_s) \). Therefore, the power of \( n'_e(t) \) is calculated as:

\[
P_{n'_e}(f) = \int_{-f_s/2}^{f_s/2} N_q \left| \frac{2L-1}{k_e(\frac{k}{2} L + aL - 2\pi f_s t)} \right|^2 df = \frac{2N_q(\frac{k}{2} L + aL - 2\pi f_s t)}{k^2} \int_{-f_s/2}^{f_s/2} \left( \frac{2L-1}{k_e(\frac{k}{2} L + aL - 2\pi f_s t)} \right) < (\pi q^2 L) / (6k_q^2 f_q).
\]

Actually, the \( P_{n'_e}(f) \) is far smaller than that of the interference after cancellation because the sampling frequency \( f_s \) is far bigger than \( f_a \). In the case, the ICR is still almost the same with the ideal case.

For the case of the additive quantization noise model dissatisfied, i.e., the dynamic range of the error signal is below the minimum distinguishable level of ADC induced by high \( L \) setting, the original error signal cannot be recovered completely by the quantized data [19]. However, due to the automatic adjustment property of the convergence loop, the dynamic range of the error signal before ADC3 would be reduced gradually to be equal to \( q \). That is, the amplitude of the stable interference after cancellation is \( q/(2k_e) \), resulting in \( P_{\text{quant}} = q^2/(8k_q^2) \). \( \text{ICR} = 10 \log_{10}(P_{\text{quant}}/P_{\text{inter}}) = 20 \log_{10}(2A) |h| k_e / q \).

Finally, the ICR is calculated as:

\[
\text{ICR} = \begin{cases} 
20 \log_{10} L & \text{if } A |h| / L \geq \frac{3q}{2\pi} \\
20 \log_{10} \left( 2A \right) |h| k_e / q & \text{if } A |h| / L \leq \frac{3q}{2\pi} 
\end{cases}
\]

It is visible that the ICR is calculated in sections depending on the amplitude of the residual interference signal of the ideal case. The section of \( A |h| / L \geq 3q/(2k_e) \) corresponds to the case when the additive quantization noise model is satisfied, which requires the peak magnitude of the input signal three times larger than the ADC quantum level [19]. The section of \( A |h| / L \leq q/(2k_e) \) corresponds to the case when the peak magnitude of the input signal under the ideal case is less than one ADC quantum level, and the the ICR is fully limited by DACs. Regarding the intermediate section, the quantization noise is causally related to the input signal, and the precise ICR is hard to be calculated. Here, we approximatively calculate the ICR still by using additive quantization model. The accuracy is verified by simulation shown in the following section.

\[D. \text{ PERFORMANCE ANALYSIS WITH DAC QUANTIZATION NOISE}\]

As shown in Fig.1, denoting weighting coefficient \( w_i(t) = w_{i1}(t) + j w_{i2}(t) \) and \( w(t) \) as the input and output of DACs respectively, we have \( w(t) = k_w q(t) + k_w w(t) \), where \( w(t) \) and \( w(t) \) are all complex signals. \( w(t) \) represents the complex DAC quantization noise, and satisfies \( P_w(t) = w_{ns1}(t) + j w_{ns2}(t) \). The mean value and the average power of \( w(t) \) can be calculated as follows:

\[E[w(t)] = E[w_{ns1}(t)] + j E[w_{ns2}(t)] = 0\]

\[E[|w(t)|^2] = E[|w_{ns1}(t)|^2] + E[|w_{ns2}(t)|^2] = \frac{q^2}{16}/6 \]
where the quantization noise of two DACs are assumed to be independent with each other.

The complex weighting coefficient $w_k(t)$ can be written as:

$$\frac{dw_k(t)}{dt} + aw_k(t) = \frac{a\rho}{k_d} e(t)x(t)e^{2\pi f_L t}$$  (23)

Substituting $e(t)$ in (3) into it, and removing the $4\pi f_c$ part, we have:

$$w_k(t) = \frac{\rho a}{2k_d} \int_0^t e^{-a(t-\tau)}(h - k_d k_b w(t))s^2(t) \cdot s^2(t) \cdot x(t)d\tau$$  (24)

Similar to the former process, we still assign $u(t) = h - k_d k_b w(t)$ in (24), $u(t)$ is shown below:

$$u(t) = h - k_d k_b w(t) - \frac{1}{2}k_d k_b \rho a \int_0^t e^{-a(t-\tau)} (u(t)x^2(t) + s^2(t))d\tau$$  (25)

By adopting the same process with (9), (10) and (11), the differential equation of $u(t)$ is expressed as:

$$\frac{du(t)}{dt} = a[l + \frac{1}{2}k_d k_b \rho x^2(t)x(t)]u(t)$$

$$= ah - \frac{1}{2}k_d k_b \rho x(t)x(t) - ak_d k_b k_d w(t) - k_d k_b w(t)$$

Similar to the process of achieving (13) and (14), the error signal with DAC noise inclusion can be expressed as:

$$e(t) = \frac{Re[h^* x(t)e^{2\pi f_L t}]}{L} + \frac{1-L}{L} e^{-aL} Re[h^* x(t)e^{2\pi f_L t}]$$

$$- Re[a(1-L)] e^{-aL} \int_0^t s(t)e^{aL}d\tau e^{2\pi f_L t}$$

$$- \frac{s(t)}{2} + Re[k_d k_b w(t)x(t)e^{2\pi f_L t}] + Re[ak_d k_b k_d x(t)e^{2\pi f_L t}]$$

$$= (L-1)e^{-aL} \int_0^t e^{aL}d\tau e^{2\pi f_L t}$$  (27)

Several observations can be made by comparing (27) with (14) of the ideal case:

1) The first four items on the right side of the equation are the same with the ideal case, indicating that the SCR, stability and the convergence speed are not affected by the DAC quantization noise.

2) The additional 5th and 6th items on the right side of the equation, denoted as $n_{d1}(t)$ and $n_{d2}(t)$, represent the DAC noise coupling directly into the receiver and the DAC noise weighted by the AICS loop, respectively. Actually, when $n_{d1}(t)$ passes through a linear time invariant (LTI) system with impulse response $h(t) = Re(2a(L-1)e^{-aL} e^{2\pi f_L t})$ and transfer function $H(f) = \frac{ak_d k_b}{al_2 + \pi^2 f_L^2 + f_L^2}$, the output is $n_{d2}(t)$. Therefore, $n_{d2}(t)$ and the input $n_{d1}(t)$ are jointly wide-sense stationary (WSS) random process, and several relations hold: $S_{n_{d1}(f)} = S_{n_{d2}(f)}|H(f)|^2$, $S_{n_{d1}(f)}|n_{d2}(f)|^2 = S_{n_{d1}(f)}|H(f)|^2$ [23]. Although $w_n(t)$ is actually a wideband signal compared to the interference carrier frequency $f_c$, it can still be regarded as the narrowband bandpass signal within the receiver band pass filter (BPF) passband $[f_c - B/2, f_c + B/2]$, providing the possibility to calculate the power of the DAC noise in the equivalent baseband domain. $B$ represents the receiver BPF bandwidth.

The power spectral density of $z(t) = -n_{d1}(t) + n_{d2}(t)$ is given by $S_z(f) = S_{n_{d1}}(f) + S_{n_{d2}}(f) - 2Re[S_{n_{d1} n_{d2}}(f)]$ [23]. The corresponding baseband equation is $S_f(f) = S_{n_{d1}}(f) + S_{n_{d2}}(f) - 2Re[S_{n_{d1} n_{d2}}(f)]$. After further manipulation, we have: $S_{n_{d2}}(f) = S_{n_{d1}}(f) + S_{n_{d2}}(f) - 2Re[S_{n_{d1} n_{d2}}(f)]$. Therefore, we have the power of $z(t)$ calculated below:

$$P_{z(t)} = \frac{1}{2} \int_{-B/2}^{B/2} \left| S_{n_{d2} n_{d2}}(1 + |H(f)|^2 - 2Re[H(f)]) \right| df$$

$$= \int_{-B/2}^{B/2} \frac{k^2 a^2 k_b^2 A^2 q_{d1}^2}{12f_s} (1 + \frac{a^2}{a^2 L^2 + 4\pi^2 f_L^2} df)$$

$$= \frac{2k^2 a^2 k_b^2 A^2 q_{d1}^2}{12f_s} (B + \frac{a(1-L)^2}{\pi L} \arctan \frac{\pi B}{aL})$$  (28)

where the front weight of 1/2 is added based on the fact that the power of the band-pass signal is a half of the power of its equivalent baseband.

3) ICR is calculated as:

$$ICR = 10log_{10} \frac{1/2A^2 |b|^2}{1/2A^2 |b|^2 + P_{z(t)}}$$  (29)

### E. PERFORMANCE ANALYSIS WITH BOTH ADC AND DAC QUANTIZATION NOISE

It is observed from Fig.1 and (27) that the DAC quantization noise $w_n(t)$ is firstly weighted by $k_d k_b k_d x(t)$ and then by $k_e$ before being coupled into ADC3. When the low resolution DAC (i.e. 8-bit) are adopted, the dynamic range of the coupling noise may cover more than three ADC quantum levels. As a result, the additve quantization noise model is valid. In the case, by using the same signal notations appearing in the previous two subsections, the complex weighting coefficient $w_k(t)$, which is the output of the LPFs, can be written:

$$\frac{dw_k(t)}{dt} + aw_k(t) = \frac{a\rho}{k_d} e(t)x(t)e^{2\pi f_L t} + ak_d k_f e(t) w(t)$$

$$+ \frac{a\rho}{k_d k_e} x(t)e^{2\pi f_L t} + ak_d k_b k_d w(t) + ak_f n(t)$$

$$= \frac{a\rho}{k_d} e(t)x(t)e^{2\pi f_L t} + ak_d k_f e(t) w(t)$$

Assigning $u(t) = h - k_d k_b w(t) = h - k_d k_b k_d w(t) - k_d k_b k_d w(t)$ as before, and substituting $e(t)$ shown in (3) into (30), and then ignoring the right-hand 2nd and 4th quantization
where the noise parts, we at last get:

$$\frac{du(t)}{dt} + a[1 + \frac{1}{2}k_2k_b\rho \chi_i^2(t)x_i(t)]u(t) = ah - \frac{1}{2}k_2k_b\rho s_1^*(t)x_i(t) - ak_2k_bk_dw_i(t) - k_2k_bk_d \frac{w_p(t)}{dt} - ak_2k_b\rho x_i(t)e^{2\pi f_1t} \frac{n_e(t)}{k_e}$$  (31)

Compared with $u(t)$ expression in (19) and (26), it can be seen that both the ADC and DAC quantization noise terms are included.

By adopting the same process to obtain (14), the final error signal $e(t)$ can be expressed as:

$$e(t) = \frac{Re[h^*x_i(t)e^{2\pi f_1t}]}{L} + \frac{L-1}{L}e^{-at}Re[h^*x_i(t)e^{2\pi f_1t}]$$

$$-Re[a(L-1)e^{-at}\int_0^t s_i(\tau)e^{a\lambda\tau}d\tau \cdot e^{2\pi f_1t} + s(t) +$$

$$Re(\frac{2(L-1)a}{k_e}e^{-at}\int_0^t n_e(t)e^{a\lambda\tau}e^{-2\pi f_1\tau}d\tau \cdot e^{2\pi f_1t})$$

$$-Re[k_2k_bk_dw_i^*(t)x_i(t)e^{2\pi f_1t}] + Re(ak_2k_bk_d(L-1))$$

$$e^{-at}\int_0^t w_p(t)e^{a\lambda\tau}d\tau \cdot x_i(t)e^{2\pi f_1t}$$  (32)

Clearly, the final $e(t)$ expression includes ADC noise term and DAC noise term, which are represented by the 5th, 6th, and 7th items of the right-hand equation, respectively. The corresponding noise power, denoted as $P_{n_{ADC}(t)}$ for ADC and $P_{n_{DAC}(t)}$ for DAC, have been calculated in the previous subsections. $P_{n_{ADC}(t)}$ can be still be ignored. The calculation of ICR is the same with (29).

Another case arises when high resolution DACs ($\geq 16$ bit) are adopted. The coupling DAC noise is so small that the performance analysis is almost the same with the case where only ADC is included. Therefore, the ICR is still a piecewise function as shown as:

$$ICR = \begin{cases} 
10\log_{10} \frac{1/2^a|b|^2}{1/2^a|b|^2 + P_{n_{ADC}}} & \text{if } M_p \geq \frac{3q}{2\pi c} \\
10\log_{10} \frac{1/2^a|b|^2}{1/2^a|b|^2 + P_{n_{DAC}}} & \text{if } M_p \in \left[ \frac{q}{2\pi c}, \frac{3q}{2\pi c} \right] \\
10\log_{10} \frac{4\pi^2|b|^2k_d^2}{q^2} & \text{if } M_p \leq \frac{q}{2\pi c} 
\end{cases}$$  (33)

where $M_p$ is the cut-off point with value of $(A|h|/L + k_2k_bk_d|A_{qDAC}|/\sqrt{2})$, and $q$ is the quantum level of ADC. Compared with (21), the additional factor $k_2k_bk_d|A_{qDAC}|/\sqrt{2}$ of $M_p$ comes from the DAC noise item $n_{DAC}(t)$ which is defined in the discussion section of (27). The expanded form of $n_{DAC}(t)$ is $k_2k_bk_dA_{qDAC}/\sqrt{2}$ when $w_i(t)$ and $w_q(t)$ are chosen to their maximum value of $q_{DAC}/2$.

It is noted that the DAC noise item $n_{DAC}(t)$ is ignored within the $M_p$ calculation. It is reasonable because $n_{DAC}(t)$ is actually the output of the narrow filter $H(f)$ whose input is $n_{DAC}(t)$. As a result, $n_{DAC}(t)$ only occupy small percentage of the $n_{DAC}(t)$ power. The definitions of $n_{DAC}(t)$, $n_{DAC}(t)$ and $H(f)$ refer to the discussion of the equation (27).

III. NUMERICAL SIMULATION AND DISCUSSION

A. SIMULATION MODEL

The simulation model is implemented with Matlab Simulink as shown in Fig.2. The complex cosine wave generator and ‘Complex to Real-Imag’ module are taken to emulate the transmitter and the orthogonal splitter, respectively. The interference channel is assumed to be static, and is modelled with a fixed small delay component (denoted as Delay1) connected in series with an adjustable gain component (denoted as Gain5), which can emulate the LoS interference coupling channel effectively. The desired signal is emulated by the Desired signal source module with the frequency and amplitude adjustable. ADC and DAC are modelled as the combination of a Zero-order Hold component and a Quantizer as illustrated. The sampling frequency of the Zero-order Hold component, and the quantization interval of the Quantizer are adjustable. In order to simulate the performance of the ideal case without ADC/DAC quantization noise, we apply the Simulink command “Comment Through” on the ADC/DAC internal Quantizer module. Two one-order digital LPFs, denoted as LPF1 and LPF2, are incorporated in the model. The Z-domain transfer function of the LPF is converted from the S-domain transfer function of $H(s) = k_f/(s + 1)$ by using the bilinear transformation method with the conversion relation of $s = 2f_c(1 - z^-1)/(1 + z^-1)$, where $f_c$ is the ADC sampling frequency. Two BPFs are added to emulate the practical case inside the receiver. The Scope and Spectrum are used to obtain the error signal in the time domain and frequency domain, respectively. The model is simulated by the Fixed-step solver with the fundamental sample time of 1 ns. The analysis benchmark is built based on the following default parameters: $k_b = 0.707$ (3 dB attenuation), $k_p = 0.707$ (3 dB attenuation), $k_c = 0.0631$ (24 dB attenuation), $k_d = 0.0631$ (10 dB attenuation), $k_f = 1000$, $h_1 = 0.1$ (20 dB channel isolation), $A = 19$ (transmitter 35.6 dBm), $a = 10$ (RC constant 0.1 second), $N_{ad} = 10$bit (resolution of ADCs), $q_{ad} = 2/2^{N_{ad}}$ (quantization level), $N_{DAC} = 18$bit (resolution of DACs), $q_{DAC} = 10/2^{N_{DAC}}$.

B. RESULTS UNDER THE IDEAL CASE

Initially, the simulated results of the convergence process and ICR are obtained and compared with the theoretical deduction. The ADC/DAC quantization noise is ignored for the ideal case. Other model parameters are identical with the default setting. Simulated results are shown in Fig.3. It is noted that the envelope of the error signal coincides exactly with that calculated by (14) in Fig.3(a), indicating that the cancellation speed is indeed determined by the loop gain $L$ and the LPF cut-off angular frequency $a$. Similar
coherence also exists in the ICR calculation presented in our previous paper [14].

Next, the correctness of the SCR deduction is assessed with results shown in Fig. 3(b). Generally, it is desired that AICS should fulfill the requirements: (1) achieving the maximum reduction in power for the interference, which requires as large loop gain \( L \) as possible. (2) fastest convergence speed to support communication systems such as high-speed frequency hopping communication, which needs a big \( aL \) value. (3) minimum power loss for the desired signal, which corresponds to the small SCR. However, those requirements cannot be fulfilled simultaneously. That is because small SCR means small \( aL \) as indicated by (16). The correctness of the (16) can be verified by the results in Fig. 3 where the quantization noise of the reference signal sampling ADC can be indeed ignored, as the precondition for additive quantization noise model is usually satisfied in practice.

The analytical ICR expression of (21) also provides optimization clues to alleviate the ADC quantization impacts, such as increasing the antenna isolation and transmitting power, adopting high-resolution ADCs, increasing the \( k_e \) value. Fig. 4(b) depicts the ICR variation tendency under different \( k_e \) setting. Increasing \( k_e \) value may be the most effective way which can be implemented by adding an AGC conditioning circuit in front of ADC. AGC circuit has low gain at the beginning of the cancellation to avoid ADC saturation, and high gain in the stable stage to obtain a high \( k_e \) value. For the \( k_e \) setting among \([0.3162 \text{ (default), 3.162, 10}]\), the LPF gain \( k_f \) is adjusted correspondingly among \([1000, 100, 31.6]\) to keep the loop gain fixed and the resulting ideal ICR stable. Overall, big \( k_e \) setting can considerably reduce the resolution requirement. For example, only 6-bit ADC is sufficient to achieve the ideal ICR for \( k_e=10 \), while the requirement is increased to 11-bit for \( k_e=0.3162 \).

The waveform capture in time domain for the error signal in front of the receiver and before/after ADC3 can provide more information to understand the system behaviour for the case that ICR is limited by ADC resolution. With ADC3 resolution fixed at 8-bit, Fig. 5(a) depicts the error signal simulation results. It can be seen that the amplitude decreases exponentially as expected by (14) calculation before reaching.
the crosspoint around 0.4 ms. After then, the dynamic range of the error signal remains constant, whereas it is expected to continue decreasing in the ideal case without ADC with comparison shown in the internal graph of Fig.5(a). Fig.5(b) illustrates the waveform of the error signal before and after ADC3 in the time range of 0.598 ms to 0.6 ms during which AICS is in the stable state. Clearly, the amplitude of the signal exactly equals $q/2$. The sampled signal after ADC3 consists of a series of pulses, introducing significant waveform distortion. However, that distortion can not prevent the convergence loop to obtain a rational weight coefficient because of the still existence of the fundamental frequency component contained in the sampled data and the dynamic adjustment character of AICS.

D. RESULTS WITH DAC INCLUDED

As regards DAC included, Fig.6 illustrates the comparison results between the simulation and theoretical calculation in terms of the convergence property and ICR, as shown in Fig.6(a) and Fig.6(b) respectively. For Fig.6(a), simulation parameters are the same with the default except that DAC resolution is fixed at 10-bit. For Fig.6(b), apart from $k_d$, receiver BPF bandwidth $B$ and DAC resolution setting shown in the figure, and $k_f$ adjusted correspondingly to be [10000, 1000] for $k_f$ setting among [0.1, 1], other parameters are the same the default values described in Section III-A. For both figures, the ADC is assumed to be ideal.

It can be deduced from (27) that the system stability and convergence speed are not affected by DAC quantization noise. The conclusion can be verified by Fig.6(a) where the interference signal in front of the receiver is actually exponentially attenuated as expected. Fairly good consistency occurs between the simulated interference signal envelope and result of the ideal case predicted by item $(1 - 1/L)e^{-a/L} \Re \{h^\ast x(t)e^{2\pi jf_c t}\}$ of (14) within the time ranging from 0 to 0.25 ms. It is also observed that the interference convergence curve is composed of a series of steps whose time length increases as the simulation goes. The step phenomenon is more noticeable when DAC resolution is lower. The phenomenon can be explained by the inset graph in Fig.6(a) where the weight signal $w_i(t)$ waveform before and after DAC are captured. As the system converges to be steady, the amplitude of the weight signal becomes more and more smaller, resulting in a gradual longer time occupation for each DAC quantization level. Nevertheless, the convergence property can still be predicted by (27).

When it comes to the ICR with DAC included, the ICR relation with DAC resolution is simulated as shown in Fig.6(b). Overall, simulation results agree well with the theoretical calculations, indicating the ICR can be indeed calculated by (29). When DAC resolution is low, the ICR is mainly limited by DAC noise, and increases with a slope of 6 dB/bit as DAC resolution grows. Narrowing the bandwidth of receiver BPF can reduce the requirement of DAC resolution. Besides, a small $k_d$ value can weaken the DAC noise impact on the ICR effectively. For the BPF bandwidth of 200kHz, the required DAC resolution to reach the ideal ICR is 14-bit with $k_d = 1$, while the requirement decreased to only 8-bit with $k_d = 0.1$. Results show that with appropriate parameter optimization, the DAC quantization noise would not be the limiting factor of the system performance.

E. RESULTS WITH BOTH ADC AND DAC INCLUDED

Regarding the scenario of both ADC and DAC included, Fig.7 presents the simulation results. Firstly, the time domain waveforms are shown in Fig.7(a) for the error signal, and in the inset figure for the signals before and after ADC3. In order
to compare the results with Fig.6(a) and Fig.5(b), resolutions of DAC and ADC3 are fixed at 10-bit and 8-bit, respectively. Simulation model parameter setting: interference signal frequency $f_{\text{sig}} = 5\, \text{MHz}$, receiver BPF bandwidth $B = 5\, \text{MHz}$, other parameters except ADC/DAC resolution are identical with the default setting. It is notable that: (1) The convergence property are not affected with ADC addition when compared with the case of only DAC included shown in Fig.6(a); (2) The ADC input signal are more random when compared with the case of only ADC included shown in Fig.5(b). This is mainly due to the DAC quantization noise.

Fig.7(b) shows the simulated ICR with respect to the ADC and DAC resolution. The calculations based on (33) are also depicted for comparison. The simulation model parameter settings are the same with that used in Fig.7(a) except the ADC/DAC resolution configuration. The ideal case ICR is 62.1 dB, and is labelled with the black dash line. It is visible that: (1) Three stages exist for ICR as ADC3 resolution increases: stage-1 limited by ADC, stage-2 affected by both ADC and DAC, stage-3 limited by DAC. The existence of three stages is consistent with the deduction of equation (33) where the ICR is calculated based on the ratio of $2^k M_p/q$. It should be pointed out that this phenomenon only occurs at the condition of high resolution of DAC adoption ($\geq 10$-bit). When low-resolution DAC (i.e. 6-bit) is adopted, the weighted quantization noise is so high that the ICR is fully limited by DAC. (2) There is a high goodness of fit between the simulation and calculation for the stage-1 and stage-3, proving the correctness of the theoretical deduction of ICR calculation in (33). (3) In the stage-2, the DAC quantization noise can act as the “dither noise” to improve the ICR under low ADC resolution condition [19], [24]. For example, when ADC3 resolution is fixed at 8-bit, the ICR should be 43 dB if DAC is excluded. However, the simulated ICR is 53 dB with DAC fixed at 12-bit, 10 dB higher than that without DAC.

IV. DEMONSTRATOR IMPLEMENTATION AND EXPERIMENTAL RESULTS
A. DEMONSTRATOR IMPLEMENTATION
The experimental set-up is shown in Fig.8(a). The R&S SMB100A signal generator and R&S spectrum analyser were used to emulate the transmitter and receiver. The high power amplifier AR 150A100BM3 was adopted to validate the high power endurance of the system. Several parts including the ADC card, DAC card, bipolar electronic controlled attenuator card were self-developed. ADC was chosen to be ADS62P45, a 14-bit, maximum 125 Msps dual channel ADC from Texas Instruments.Inc. In the experiments, the sampling of ADC was fixed at 100 MHz. DAC was selected to be DAC9881, a monolithic, 18-bit DAC from Texas Instruments.Inc, whose integral linearity error is typically within $\pm 1$ LSB, and differential linearity error is within $\pm 0.5$ LSB. Due to the limit of the available RF components, the testing frequency range was restricted to short-wave band among 2 MHz to 30 MHz. The transmitted power after HPA was adjusted to be around 34 dBm.

Fig.1 shows that the correlation operation inside FPGA can be simply divided into two cascaded procedures: multiplication and low pass filtering. In our implementation, the data in the two procedures are all represented with double format so that the truncation behaviour inside FPGA can be ignored. The program structure is shown in Fig.8(b) where the data representation format at each stage is displayed. Fix_m_n indicates a signed fixed-point format with total m-bit and n-bit fraction. We adopt Xilinx System Generator to build and simulate the program in Simulink, and to generate HDL codes to verify the program in FPGA. Xilinx System Generator provides an add-on library Xilinx blockset to Simulink, and allows bit and cycle accurate floating and fixed-point simulations in Simulink with exactly same behaviour as that in FPGA. It also provides the automatic HDL code generation function to simplify the DSP algorithm development inside FPGA. Fig.8(b) shows the IP core type within each stage which can be found in the Xilinx blockset library. The realization challenge of the digital LPF and implementation details can refer to our previous paper [15]. ADC decoder modules are introduced to obtain the sampled analog value.
at ADC input. Similarly, the cascaded modules of DAC coder and Float-to-Fix are designed to transfer the filtered digital voltage from LPF into the DAC chip acquired format.

The purpose of this experiment is to validate the theoretical analysis with a practical interference channel and demonstrate the practicability of the digital-controlled cancellation system. Therefore, an adjustable attenuator ranging from 20 dB to 79 dB was initially adopted to emulate the ideal single-path coupling channel. That setting is consistent with the analysis channel assumption, and is beneficial to obtain the effective comparable practical results with the simulation. Next, the system performance was assessed based on real space channel with shortwave TX/RX antennas located on the roof of our building with location distance of 30m. They are monopole antennas whose radiation patterns in the H-plane (horizontal) are omnidirectional while in the E-plane (vertical) are inverted “8”. The antenna height is 10m, and the surroundings can be seen in Fig.8.

B. EXPERIMENTAL RESULTS

The measured model parameters of the demonstrator are extracted below: $k_d = 0.5012$, $k_e = 0.0631$, $k_d = 0.25$, $A = 15.8$, effective $N_{ad} = 10.35$ bit, $d_{ad} = 1.5324mV$, $N_{da} = 18$ bit, $d_{da} = 38.15μV$. Two values for $k_e$ exists. One is 0.1 for the case of AGC AD8367 excluded in front of ADC, the other is 1.561 for the scenario of AGC included. The value of $k_f$ is determined by software. Here, $N_{ad}$ corresponds to the effective number of bit (ENOB) which has taken the noise into account from the ADC itself and peripheral circuits.

For the practical digital-controlled cancellation system, $k_e$ and $k_f$ are two important parameters. The importance of the ADC front coefficient $k_e$ can be seen from the simulation in Fig. 4(b), where increasing the $k_e$ value can significantly reduce the ADC resolution requirement to obtain a required ICR. Actually, $k_e$ decides the ICR upper bound when the transmitter power and ADC type are pre-arranged, and the upper bound of ICR is calculated to be $20log_{10}(2A|h/k_e/q)$ by (21). Besides, when the hardware has been designed, the LPF DC amplification coefficient $k_f$ is the only software adjustable parameter. The ICR relation with $k_e$ and $k_f$ is calculated and depicted in Fig.9(a). Noted that the calculation is based on (33) with the extracted demonstrator parameters.

It is found that the ICR level grows by 20 dB when $k_f$ is ten times larger. Furthermore, ICR would stand at the upper bound level after $k_f$ reaches the segment point of 5500. Experiment results shown in Fig.9(b) also verify the trend. For example, ICR increases by 20 dB from average 23.23 dB to average 43.18 dB when $k_f$ grows up from 500 to 5000 for the NoAGC situation. Furthermore, calculation shows that the segment point of $k_f$ holds the same regardless of $k_e$ variation, and ICR should increase by $20log_{10}(k_{new}/k_{old})$. Measured results also prove the correctness of the calculation. For instance, as $k_e$ increases 15.61 times larger to 1.561 by adding an AGC in front of ADC3, the measured ICR increases by 22.67 dB to average 65.86 dB. It is also observed from Fig.9(b) that the digital-controlled AICS is suitable for the whole HF band, which is mainly attributed to the absence of the frequency factor in the ICR calculation equation (33). In practice, the ICR calculation has no relation with the interference frequency, provided that the Nyquist sampling theorem is satisfied.

The practicability of the AICS is also evaluated based on the real space coupling channel and real transmitting signal with results shown in Fig.10. The frequency response of the space coupling channel is shown in Fig.10(a) where the strong frequency-selective response is visible with the isolation variation up to 40 dB. Multi-path phenomena between the Tx and Rx antennas are expected from the channel measurement, which may deteriorate the ICR performance. However, the AICS still have the average ICR of 59 dB for the mono-sine waveform and 50 dB for the AM signal with 30% modulation depth.

V. CONCLUSION

In conclusion, we have presented a digital-controlled self-interference cancellation structure that builds upon our previous efforts by adding the comprehensive theoretical analysis on the ADC/DAC quantization noise impact. The analysis allows a deep understanding on the function mechanism of the quantization noise, and provides a practical guideline for performance optimization. It is found that the cancellation loop stability and convergence property are not affected by the ADC/DAC addition. The quantization noise of the reference sampling ADC has marginal influence over the ICR, thus a low-price 8-bit ADC can satisfy the requirement. However, the quantization noise of the error sampling ADC...
may induce increasingly large degradation of ICR. Therefore, a high-resolution ADC like 12-bit or large magnification of the front conditioning circuit are necessary for achieving desired high ICR. The impact of DAC noise is not so serious because of wide distribution of the noise over the Nyquist bandwidth and relatively narrower passband bandwidth of the receiver, although the DAC noise can be directly injected into the receiver. The parameter optimization on the interface circuit following DAC to obtain a high noise attenuation can further decrease the DAC noise impact. Finally, the correctness and accuracy of the theoretical deductions are validated by the simulation and experimental measurements. An average ICR of 65.86 dB, 59 dB and 50 dB was achieved on the cases of the attenuator coupling channel with mono-tone waveform, real space channel with mono-sine waveform and AM waveform, respectively, demonstrating its favourable practicability.

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