Can Tunnel Transistors Scale Below 10nm?

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Abstract—The main promise of tunnel FETs (TFETs) is to enable supply voltage \( V_{DD} \) scaling in conjunction with dimension scaling of transistors to reduce power consumption. However, reducing \( V_{DD} \) and channel length \( L_{ch} \) typically deteriorates the ON- and OFF-state performance of TFETs, respectively. Accordingly, there is not yet any report of a high performance TFET with both low \( V_{DD} \) (~0.2V) and small \( L_{ch} \) (~6nm). In this work, it is shown that scaling TFETs in general requires scaling down the bandgap \( E_g \) and scaling up the effective mass \( m^* \) for high performance. Quantitatively, a channel material with an optimized bandgap \( E_g \sim 1.7eV \) and an engineered effective mass \( (m^* \sim 40\sqrt{2\hbar^2m_0}) \) makes both \( V_{DD} \) and \( L_{ch} \) scaling feasible with the scaling rule of \( L_{ch}/V_{DD} = 30 \text{ nm/V} \) for \( L_{ch} \) from 15nm to 6nm and corresponding \( V_{DD} \) from 0.5V to 0.2V.

Index Terms—TFETs, nanowire, scaling, sub-10nm, direct tunneling, NEGF.

I. INTRODUCTION

Although tunnel FETs (TFETs) were originally proposed for low power applications [1]–[3], the low ON-current \( I_{ON} \) challenge in TFETs has concealed their scaling problem [4]–[6]. The low \( I_{ON} \) challenge can be solved by increasing the electric field at the tunnel junction; e.g. by using dielectric engineering [7], atomistically thin channels [8]–[11], or internal polarization [12]. However, the scaling challenge is more tricky since the tunneling currents \( I_{ON} \) and \( I_{OFF} \) depend on the same device parameters. Hence an attempt to decrease \( I_{OFF} \) would reduce \( I_{ON} \) and vice versa. In contrast, \( I_{ON} \) and \( I_{OFF} \) in MOSFETs are more independent of each other and a channel material with a large bandgap (or optimized effective mass) can be used for sub-12nm channels to suppress the direct source-to-drain tunneling [13], [14].

Fig. 1a shows the device structure of an InAs nanowire (NW) TFET with a diameter of 3.4nm. The transfer characteristics of the device simulated by the NEMO5 tool [25]–[27] are shown in Fig. 1b with \( I_{OFF} \) fixed at 1nA/µm. In the simulations, we scale \( V_{DD} \) down with the channel length \( L_{ch} \). The results indicate that the InAs NW-TFET exhibits a promising performance with long channel lengths (i.e. \( L_{ch} > 9 \text{ nm} \)), however it completely fails to switch from ON- to OFF-state for the case of \( L_{ch}=6\text{ nm} \) and \( V_{DD}=0.2V \) (i.e. \( I_{ON}/I_{OFF} \approx 10 \ll 10^5 \)).

Roughly, the transmission in the ON-state \( (T_{ON}) \) and OFF-state \( (T_{OFF}) \) of TFETs depends on [13], [16]:

\[
\log(T_{ON}) \propto \Lambda \sqrt{m^*E_g} \tag{1}
\]

\[
\log(T_{OFF}) \propto L_{ch} \sqrt{m^*E_g} \tag{2}
\]

where \( \Lambda \) and \( L_{ch} \) are the tunneling distances in the ON- and OFF-state (Fig. 1b) respectively. \( m^* \) and \( E_g \) are the reduced effective mass and the bandgap of the channel material.

The scaling of the channel below 10nm brings \( L_{ch} \) close to \( \Lambda \) which reduces \( I_{ON}/I_{OFF} \) significantly. One apparent solution can be a heterostructure channel where the term \( m^*E_g \) is different in (1) and (2) due to different materials used in those regions [12], [18]. However, it has been shown that the presence of band discontinuity and interface states in heterostructures can deteriorate the OFF-state performance of TFETs [19], [20]. Hence, in this work the homojunction TFETs have been considered as a more practical steep sub-threshold swing (SS) device.

On top of the length scaling problem which increases \( I_{OFF} \) significantly, the voltage scaling reduces \( I_{ON} \). The maximum tunneling window in TFETs approximately equals \( qV_{DD} \). Thus a short channel TFET with a small \( V_{DD} \) is expected to have a small \( I_{ON}/I_{OFF} \).

In this work, it is shown that by using a channel material with optimized \( m^* \) and \( E_g \), it is still feasible to obtain an

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acceptable $I_{ON}/I_{OFF}$ for ultra-scaled TFETs (i.e. $I_{ON}/I_{OFF} > 10^5$ for $L_{ch}=6$nm and $V_{DD}=0.2$V). The solution to the scaling problem of TFET is to *scale down* $E_g$ of channel material to the smallest possible value to achieve a high $I_{ON}$. Of course $E_g$ cannot be smaller than $qV_{DD}$, otherwise the channel cannot cover and block the tunneling energy window in the OFF-state. On the other hand, $m^*$ should *scale up* with scaling down the dimensions to decrease $I_{OFF}$. Fig. 1 shows that the performance of 6nm long gate-all-around TFET can be improved more than 4 orders of magnitude by *scaling down* $E_g$ and *scaling up* $m^*$. The favorable design space for $m^*$ and $E_g$ is discussed in Sec. IV.

II. SIMULATION DETAILS

The self-consistent 3D Poisson-NEGF (Non-Equilibrium Green’s Function) method is used in the NEMO5 software for the simulation of InAs TFETs [25]–[27]. The InAs channel material is described by a 10 band nearest neighbor tight-binding model [28]. To find the impact of $m^*$ and $E_g$ on the performance of TFETs, a model is needed where $m^*$ and $E_g$ can be set as free input parameters, in contrast to the atomistic approach where $m^*$ and $E_g$ are the output of the simulation through material composition and geometry induced confinement effects. To reduce the number of free parameters, it is assumed that the electron and hole effective masses are equal ($m^*_e=m^*_h=m^*$). Recently, an analytical model was developed which produces results in excellent agreement with NEGF simulations [21]. To show the validity of this analytical model for ultra-scaled TFETs, the simulation results of scaled InAs TFETs with the scaling rule of $L_{ch}/V_{DD} = 30$ nm/V obtained from the analytical model are benchmarked against the NEGF results first. Fig. 2 compares the results of analytical model and NEGF simulations. Notice that in Fig. 2 the OFF-state is not fixed unlike Fig. 1. The accuracy and speed of the analytical model and tuneability of $m^*$ and $E_g$ makes this model an ideal tool for optimizing the TFET design.

III. SIMULATION RESULTS

To analyze different TFET designs, the tunneling transmission path at the top of the tunneling window ($E = \mu_S$) is indicated as a function of source-channel tunneling window ($\Delta E$) in Fig. 3a. Knowledge of the tunneling transmission probability as a function of $\Delta E$ (i.e. $T(\Delta E)$) provides information about the transfer characteristics [8]. Fig. 3b shows an example of $T(\Delta E)$ with the corresponding TFET operational regimes (e.g. ON- and OFF-states, and n- and p-branches). Notice that $\Delta E \approx 0$ is the ON-OFF transition point. For a small drain-source voltage, the I-V can be calculated by integrating the $T(\Delta E)$ in the tunneling energy window (energies between $\mu_S$ and $\mu_P$). The tunneling transmission shows how far the TFET is from its ideal performance (i.e. $T = 0$ and $T = 1$ at OFF- and ON-state, respectively). Accordingly, $I_{ON}$, $I_{OFF}$, and $SS$ can be estimated from the maximum and minimum values of $T(\Delta E)$ and its slope at subthreshold region. The impact of $L_{ch}$ scaling on the transmission profile of InAs NW-TFET is shown in Fig. 3c. Reducing the channel length increases $T_{OFF}$ significantly while $T_{ON}$ remains intact which was expected from equations (1) and (2).

Fig. 3c shows the effect of bandgap on $T(\Delta E)$; Obviously, a larger bandgap decreases both $T_{OFF}$ and $T_{ON}$. Notice
that changing $E_g$ does not improve the subthreshold slope of $T(\Delta E)$ (black lines in Fig. 3d). Increasing $E_g$ decreases $T_{OFF}$ more than $T_{ON}$ since the prefactor of $\sqrt{m^*E_g}$ is larger for $T_{OFF}$ (note that $L_{ch} > \Lambda$ in equations (1) and (2)). On the other hand, to reach this lower $T_{OFF}$ a larger gate voltage change is needed for larger band gaps (i.e. $\Delta E_{OFF} \approx \frac{-E_g}{2}$). Thus, there is no noticeable improvement in $SS$ with larger $E_g$. On the other hand, increasing $m^*$ improves $SS$ as shown in Fig. 3e. Since a larger $m^*$ does not require a larger gate voltage change, contrary to a larger $E_g$. Fig. 3 compares TFETs with a constant $\sqrt{m^*E_g}$ but different $m^*/E_g$ ratios. Notice that not only $SS$ improves with increasing $m^*/E_g$ ratio, but also $T_{ON}$. The reason for improved ON-state performance is that reducing $E_g$ decreases the depletion width at the source-channel interface and $\Lambda$ decreases in equation (1) \[15\].

**IV. CHANNEL MATERIAL WITH OPTIMIZED PROPERTIES**

Fig. 4a shows the $I_{ON}/I_{OFF}$ ratio of NW-TFETs with $L_{ch}=6nm$ and $V_{DD}=0.2V$ and a channel material with different $m^*$ and $E_g$. To suppress the p-branch of TFETs, the drain doping level is chosen to be much smaller than source doping level ($N_S = 20N_D = 10^{20}cm^{-3}$) and a gate leakage of $1nA/\mu m$ is assumed ($I_{OFF} \geq 1nA/\mu m$) \[29\]. The maximum $I_{ON}/I_{OFF}$ ratio is obtained with an $E_g$ of about $1.2qV_{DD}$.

Moreover, with increasing $E_g$, the optimum $m^*_opt$ reduces and for $E_g \geq 1.5qV_{DD}$ the product $m^*_optE_g^{opt}$ (circle symbols) saturates (dashed line). Fig. 4 shows that TFETs with $E_g$ between $1.1qV_{DD}$ and $1.5qV_{DD}$ have acceptable $I_{ON}/I_{OFF}$ ratios according to ITRS requirements ($I_{ON}/I_{OFF} > 10^5$).

Fig. 3 illustrates the favorable design space for $m^*$ as a function of $V_{DD}$ for TFETs with the scaling rule of $L_{ch}/V_{DD} = 30nm/V$. The shaded area in Fig. 3 shows higher and lower bounds on $m^*$ and $E_g$ of the channel material for a high performance ultra-scaled NW-TFET. Fig. 3 shows the transfer characteristics of NW-TFETs with optimized $E_g$ and $m^*$ from equations (3) and (4). $I_{ON}/I_{OFF}$ ratio of larger than $10^5$ and $SS$ below $15mV/\text{decade}$ are obtained for all the cases including the 6nm long channel.

**V. CONCLUSION**

In summary, the scaling of TFETs pushes the semiconductor industry to look for channel materials with higher $m^*$, similar to ultra-scaled MOSFETs \[13\]. However, in TFETs channel material should have both $m^*$ and $E_g$ optimized. More accurately, the scaling of high performance NW-TFETs below 10nm requires:

1. A channel material with scaled down band gap
   \[E_g^{Best} \sim 1.2qV_{DD}[eV]\]

2. A channel material with scaled up effective mass
   \[m^*_{opt} \sim 40V_{DD}^2[m_0^{-1}]\]

3. Higher doping level in the source ($N_S$) than drain ($N_D$).
   \[N_S \gg N_D\]

4. A channel material with low dielectric constant ($\epsilon_{ch}$) and a high-k oxide.
   \[\epsilon_{ox} \gg \epsilon_{ch}\]

Fig. 4: a) $I_{ON}/I_{OFF}$ ratio for a NW-TFET with $L_{ch}=6nm$ and $V_{DD}=0.2V$ for different $E_g$ and their optimized values ($I_{ON}/I_{OFF})^{opt}$ (circle symbols). b) ($I_{ON}/I_{OFF})^{opt}$ as a function of $E_g$ for $V_{DD}=0.2V$ and 0.3V.

Fig. 5: a) The optimum effective mass as a function of $V_{DD}$ for TFETs with the scaling rule of $L_{ch}/V_{DD} = 30nm/V$ for $L_{ch}$ from 15nm to 6nm. b) $I_{OFF}/V_{G}$ of NW-TFETs with optimized $E_g$ and $m^*$ from (3) and (4).

Best channel material: Optimum $m^*$ and $E_g$
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