Effects of substrate heating and post-deposition annealing on characteristics of thin MOCVD HfO$_2$ films

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Abstract. It is well known that Hf-based dielectrics have replaced the traditional SiO$_2$ and SiON as gate dielectric materials for conventional CMOS devices. By using thicker high-k materials such as HfO$_2$ rather than ultra-thin SiO$_2$, we can bring down leakage current densities in MOS devices to acceptable levels. HfO$_2$ is also one of the potential candidates as a blocking dielectric for Flash memory applications for the same reason. In this study, effects of substrate heating and oxygen flow rate while depositing HfO$_2$ thin films using CVD and effects of post deposition annealing on the physical and electrical characteristics of HfO$_2$ thin films are presented. It was observed that substrate heating during deposition helps improve the density and electrical characteristics of the films. At higher substrate temperature, $V_{fb}$ moved closer to zero and also resulted in significant reduction in hysteresis. Higher O$_2$ flow rates may improve capacitance, but also results in slightly higher leakage. The effect of PDA depended on film thickness and O$_2$ PDA improved characteristics only for thick films. For thinner films forming gas anneal resulted in better electrical characteristics.

1. Introduction

1.1. Impact on scaling on MOS gate stack

Over the last decade, MOS gate stack combination has undergone several changes. Conventional CMOS structure includes Polysilicon gate electrode, SiO$_2$ gate oxide and Silicon substrate. For the 45nm node and below, this combination had to be changed due to several factors. SiO$_2$ thickness has been scaled down in accordance with Moore’s law ever since miniaturization started over half a century ago in order to ensure sufficient gate capacitance which affects the performance of the device. When the silicon dioxide thickness is reduced to less than 5nm, direct tunnelling occurs through the oxide leading to higher leakage currents. For the 45nm node and below, the SiO$_2$ thickness required had become less than 1nm, causing the leakage to become unacceptable [1]. While there are circuit techniques to overcome this leakage [2], these can only be temporary solutions. Using a thicker film with a higher dielectric constant is the most practical and long-term solution. SiON gate dielectrics [3], having k value between 4 and 7 were used till the 65nm node. Among the other high-k dielectrics

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studied in literature, HfO$_2$ [4, 5], ZrO$_2$ [6,7], and Hafnium silicate [8,9] are the most promising ones based on their physical and electrical properties. It is known that since the 45nm node, Hf-based dielectrics such as HfO$_2$ have been implemented in the gate stack along with metal gate electrodes [10]. Polysilicon had to be replaced with metal gate electrodes due to several issues such as thermal stability in contact with high-k, and poly depletion effect which degrades the gate oxide capacitance [11]. Hence the dual-poly approach had to be replaced with dual-metal gate approach since different work-functions are required for NMOS and PMOS devices. One serious issue with high-k dielectrics has been the low carrier mobilities observed in high-k dielectric based MOSFETs, especially in the high-field regions. This has been addressed by using ‘strained-Si’ in the channel as in the 45nm node [10] which results in improved mobilities, and perhaps by using Germanium in the channel region in future [12]. Figure 1 shows the modifications in gate stack in traditional CMOS over the last decade.

![Fig. 1: Modifications in CMOS gate stack since the 45nm node](image1)

![Fig. 2: Gate stack structure in typical Flash memories](image2)

1.2. Dielectrics for flash memory applications

While HfO$_2$ has been implemented in CMOS, there has been another area where it has been widely considered for. Charge-trapping flash memories such as NOR and NAND flash memories, consist of an inter-poly dielectric layer (also called blocking dielectric), a charge - trapping layer, and a tunnel dielectric layer (fig. 2). For this, HfO$_2$ is believed to be a potential candidate for all the three layers. These devices require high-k materials for improved capacitance leading to better memory retention while maintaining low leakage densities [13, 14]. In addition, this also enables the device to withstand higher operating voltages, thereby enhancing the programming and erasing speeds of the flash memory (Kim and Lee 2005). In the 2015 edition of International Technology Roadmap of Semiconductors (ITRS 2015), high-k materials are included as part of requirements for Flash Memory Technology, to be used as an blocking dielectric, in the next few years. Among the various potential candidates for Non-volatile memory, HfO$_2$ is considered as one of the most suitable candidates.

In spite of the fact that HfO$_2$ has been studied extensively in the past, there is not much study in the 9-25nm thickness regime –especially certain aspects such as effects of substrate heating, post deposition anneals, and effects of constant voltage stress on electrical characteristics. As this thickness is also suitable for flash memory applications, it becomes important to understand the behaviour of HfO$_2$ in this thickness regime. In this work, HfO$_2$ films were deposited by MOCVD on Silicon substrates. The effects of substrate heating and O$_2$ flow rate while depositing HfO$_2$ on the electrical and physical characteristics of HfO$_2$ films are presented. In addition, effects of post deposition annealing ambient on electrical properties are also presented.
2. Experimental Details

Metal – Oxide - Semiconductor capacitors (N-MOSCAPs) were fabricated using p-type Si (100) substrates with a resistivity of 1 - 10 Ωcm. The wafers were cleaned using standard RCA cleaning followed by a dilute HF-dip. HfO2 was deposited by MOCVD using Applied Materials’ Centura. The precursor flow rate is 20mgm, while the oxygen flow rate was varied between 200 - 500sccm. The substrate temperature was varied between 400ºC and 700ºC, while the pressure was kept at 6 Torr. After film deposition, selected samples were annealed in O2 or Forming gas ambient or both. After PDA, Aluminium metallization was done using shadow mask.

The material characterization was performed by determining the refractive-index and thickness using an Ellipsometer (SE800). The electrical measurements were carried out using the Semiconductor Parameter Analyzer (Agilent 4155C), LCR meter (Agilent 4284), and the Semiconductor Characterization System (Keithley 4200). The Capacitance–Voltage characteristics were determined at 10 kHz – 1MHz, with the applied AC voltage peak-to-peak signal level of 50 mV. Equivalent oxide thickness (EOT), Interface state density (Dit), and flatband voltage (Vfb) were obtained using CVC Hauser program.

3. Results and Discussion

3.1. Effect of substrate temperature on thickness and film quality

One of the key variables in an MOCVD process is the substrate temperature. Figure 3 shows the physical thickness and refractive index under varied substrate temperature. It was observed that the film thickness decreased with increasing substrate temperature indicating that the films deposited at higher temperatures have more density. The films were subsequently annealed in O2 ambient at 500ºC for 15 seconds. Refractive index obtained in as-deposited films were observed to be very close to reported values of 1.9 – 2.0 [15] indicating good quality HfO2 films. It can be observed that annealing reduces physical thickness in all cases probably due to further densification of deposited film [16]. This results in improved film quality after PDA. Films deposited at higher substrate temperatures also showed much higher dielectric constant and significantly lower EOT (Table 1). This is understandable because at lower substrate temperatures, the organic precursors of Hafnium leave behind small amounts carbon contamination in the films [17] which reduces overall k-value of HfO2. At higher temperatures these contaminants are removed [17] by the formation of CO2. The lowering of the k-value for the 700ºC sample is most likely due to formation of a thin interfacial layer (probably HfSiOx) between HfO2 and Si substrate [18]. For the sample deposited at 400ºC the carbon impurity is removed upon subsequent O2 anneal. This is corroborated by the improvement in refractive index after O2 anneal for this sample. For the samples deposited at 600ºC and 700ºC, the slight reduction in refractive index after O2 annealing is attributed to the formation of the above mentioned interfacial layer. The observed improvement in overall dielectric constant of these samples is attributed to higher density HfO2 films free from carbon contamination.

| Substrate Temperature | EOT (nm) | Dielectric Constant |
|-----------------------|----------|---------------------|
| 400 C                 | 7.46     | 11.78               |
| 600 C                 | 2.45     | 22.18               |
| 700 C                 | 2.73     | 16.95               |

Table 1: Substrate temperature effects on EOT and dielectric constant of HfO2
3.2. Effect of substrate temperature on C-V characteristics
The C-V characteristic of the films deposited at different temperature has been shown in Figure 4a. The sample deposited at 500°C was found to be defective. The maximum capacitance value has increased with increasing temperature due to densification at higher temperatures. But the important pattern to be noted here is the shift in the flatband voltage towards zero with increasing temperature (fig. 4b). This reflects removal of carbon impurities from film and the resultant reduction in fixed charges in the film at higher substrate temperatures. The reduction in hysteresis at higher temperatures also indicates reduction in fixed charges in film (fig. 4b) [5, 8, 17].
3.3. **Effect of post deposition annealing on C-V characteristics**

The effect of annealing was found to be dependent on film thickness. For thicker films, sufficient PDA is required to fully oxidise the film and capacitance improves with annealing as a result (fig. 5a). It can be seen in the figure that the shape of CV for the 35nm film in accumulation improves upon annealing, but is still not matching with the simulated CV indicating that the film is still not fully oxidized. But on the other hand, for thinner films, O₂ PDA results in lowering of capacitance owing to the formation of a SiO₂-like interface (fig. 5b) [18]. The shape of the CV even without O₂ anneal is also quite typical suggesting a fully oxidized film even before PDA.
Now since \( \text{O}_2 \) anneal cannot be used for thinner films, Forming gas anneal was tried (400°C, 20mins) as a PDA for the 12nm film. The results obtained can be seen in Figure 6 which shows a comparison of CV of the un-annealed film with the ones annealed in \( \text{O}_2 \) and Forming gas. As seen previously, the \( \text{O}_2 \) anneal resulted in a thick interface formation and subsequent reduction in capacitance. On the other hand, with forming gas anneal, it was observed that the accumulation capacitance reduces slightly perhaps due to the reducing environment of forming gas. But more importantly, forming gas anneal considerably improves the slope of the CV curve as seen from the inset in the figure. Forming gas is known to cause hydrogen passivation of oxide-silicon interface thereby reducing the dangling bonds [19] which leads to reduction in the interface state density.
3.4. Effect of \( O_2 \) flow rate (during \( \text{HfO}_2 \) deposition) on film properties

The effect of \( O_2 \) flow rate during CVD on the film characteristics was studied. Fig 7a shows the effect of \( O_2 \) flow rate on film thickness and refractive index of \( \text{HfO}_2 \) films. As the \( O_2 \) flow rate is varied from 100sccm to 500sccm (while keeping other parameters constant), the \( \text{HfO}_2 \) thickness varies very slightly from 19nm to 20.6nm, which is attributed to higher reaction rate in presence of more oxygen. Meanwhile, the refractive index is more or less unaffected (variation between 2.05 and 2.01 is within measurement error). The important thing is to see if there is any variation in electrical characteristics. Fig 7b shows the effect of \( O_2 \) flow rate on CV characteristics. A higher \( O_2 \) flow rate improves the capacitance and \( K \)-value of the film suggesting that higher \( O_2 \) flow rates ensure complete oxidation of film and removal of carbon contamination. The \( V_{fb} \) of higher \( O_2 \) flow rate samples also shifts to more positive values similar to the higher substrate temperature cases seen in fig 4. It is possible that if there is not sufficient oxygen during deposition, the unoxidized \( \text{Hf} \)-ions add to fixed charge near the bottom interface. Either a higher deposition temperature or higher \( O_2 \) flow rate results in more oxidation of ions and impurities and hence leads to reduced fixed charge near interface.

![Fig. 7(a): Effect of \( O_2 \) flow rate on film thickness and refractive index](image1)

![Fig. 7(b): Effect of \( O_2 \) flow rate on CV characteristics (measured at 100kHz)](image2)
3.5. Effect of $O_2$ flow rate (during HfO$_2$ deposition) on hysteresis and leakage

Figure 8(a) shows the hysteresis of the hafnium oxide films under different $O_2$ flow rates. It can be seen that while higher $O_2$ flow rates can marginally lower the hysteresis values, the samples without PDA have significantly larger hysteresis values than the samples with PDA. PDA helps remove the ionized charges in the film which are present close to bottom interface. PDA also helps remove carbon contamination. Higher $O_2$ flow rates lead to slightly higher leakage which arises probably as a result of higher capacitance (fig. 8b).

Fig. 8(a): Hysteresis of films with different $O_2$ flow rates with and without PDA

4. Summary and Conclusion

HfO$_2$ films were deposited on Silicon substrates using MOCVD. The effects of substrate heating on the electrical and material characteristics of HfO$_2$ were studied. It was observed that higher substrate...
temperatures resulted in thinner films with higher density. However, the 700°C deposition also resulted in formation of thick interfacial layer causing deterioration of overall dielectric constant. The highest k value obtained was around 22 at 600°C substrate temperature. Higher deposition temperatures also resulted in shifts in $V_{fb}$ closer to zero and significant reduction in hysteresis indicating that fixed charges and carbon contamination can be minimized by going to higher substrate temperatures. The effect of PDA on the device characteristics was studied and it was found that it depended on the thickness of the HfO$_2$ film. For example, for a 35nm HfO$_2$ film, O$_2$ annealing results in fully oxidizing the film and thereby improves capacitance and $V_{fb}$. But for a 12nm HfO$_2$, O$_2$ annealing results in decrease in overall capacitance due to interfacial layer formation. For the HfO$_2$ films thinner than 12nm, annealing in forming gas helps reduce interface states by H-passivation and results in better CV characteristics. The effect of O$_2$ flow rate on film characteristics was studied. It was observed that having a higher flow rate improves the capacitance and $V_{fb}$ values. At higher flow rates, the film is fully oxidized and the carbon contamination and fixed charges are reduced leading to improved capacitance. However, at higher flow rates, the films were found to be slightly leakier. In conclusion, it was observed that process parameters have significant impact on electrical characteristics of MOCVD HfO$_2$. For ideal MOS capacitor characteristics, using a substrate temperature of 600°C along with O$_2$ flow rate of 500sccm gives the best film in terms of k-value for the thickness range studied. Further annealing in O$_2$ ambient is recommended for thick films, while doing PDA in an inert ambient such as N$_2$ is recommended for thinner films. Performing a forming gas anneal before or after the gate electrode deposition is critical for improving the interface quality without sacrificing the capacitance much.

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6. References

[1] Weir B E, Silverman P J, Alam M A, Baumann F, Monroe D, Ghetti A, Bude J D, Timp G L, Hamad A, and Oberdick T M, Zhao N X, Ma Y, Brown M M, Hwang D, Sorsch T. W and Madic J 2000 Tech. Dig. IEDM p. 437

[2] Priya M G, Baskaran K, and Krishnaveni D 2012 European Journal of Scientific Research 74 96-105

[3] Lucas A, Gopalan S, Lee J C, Kaushal S, Niino R, and Tada Y 2000 Electrochemical and Solid-State Letters 3(8) 389-391

[4] Mohsenifar S, Shahrakhabadi M H 2015 Microelectronics and Solid State Electronics 4(1) 12-24

[5] Kim Y H and Lee J C 2005 Hf-Based High-k Dielectrics: Process Development, Performance Characterization, and Reliability (USA, Morgan & Claypool)

[6] Qi W J, Nieh R, Lee B H, Kang L G, Jeon Y, Onishi K, Banerjee S and Lee J C 1999 Tech. Dig. Int. Elec. Dev. Meet 145-148

[7] Nieh R, Choi R, Gopalan S, Onishi K, Kang C S, Cho H J, Krishnan S and Lee J C 2002 Appl. Phys. Lett. 81 1663-1665

[8] Gopalan S 2002 Process Development, Material Analysis, and Electrical Characterization of Ultra-Thin Hafnium Silicate Films for Alternative Gate Dielectric Application (Ph.D. Thesis University of Texas at Austin, USA)
[9] Gao-Bo X and Qiu-Xia X 2009 Chin. Phys. B 18(2) 768
[10] Auth C 2008 IEEE Proc. Cust. Int. Circ. Conf. 15-2-1
[11] Yu B, Ju D H, Lee W C, Kepler N, King T J and Hu C 1998 IEEE Trans. Electr. Dev. 45(6) 1253
[12] Dimoulas A, Gusev E, McIntyre P C and Heyns M 2007 Advanced Gate Stacks for High Mobility Semiconductors (New York, Springer Berlin Heidelberg) 181-202
[13] Alessandria M, Piaggea R, Albericia S, Bellandia E, Caniattia M, Ghidinia G, Modellia A, Paviaa G, Ravizzaa E, Sebastiania A, Wiemerb S, Fanciullib M, Fiorentinic V, Cadelanoc E and Lopez G M 2006 ECS Transactions 1(5) 91-105
[14] Breuil L, Lisoni J G, Blomme P, Van den Bosch G and Houd J V 2014 IEEE Elec. Dev. Lett. 35(1) 45-47
[15] Vargas M, Murphy N R and Ramana C V 2014 Optical Materials 37 621-628
[16] Cimalla V, Baeumler M, Kirste L, Prescher M, Christian B, Passow T, Benkhelifa F, Bernhardt F, Eichapfel G, Himmerlich M, Krischok S and Pezoldt J 2014 Materials Sciences and Applications 5 628-638
[17] Jones Anthony C, Aspinall Helen C, Chalker Paul R, Potter Richard J, Kukli Kaupo, Rahtu Antti, Ritalac Mikko and Leskela Markku 2004 J. Mater. Chem. 14 3101-3112
[18] Elshocht Van S, Caymax M, Gendt De S, Conard T, Pe’try J, Date L, Pique D, and Heynsa M M 2004 Journal of The Electrochemical Society 151(4) F77-F80
[19] Onishi K, Kang Chang Seok, Choi Rino, Cho Hag-Ju, Gopalan Sundar, Nieh Renee E, Krishnan Siddharth A, and Lee Jack C 2002 IEEE Transactions on Electron Devices 50(2), 384-390