5 bit current steering low power DAC for threshold voltage adjustment

E Atkin, I Sagdiev
National Research Nuclear University MEPhI (Moscow Engineering Physics Institute), 115409, Kashirskoe highway 31, Moscow, Russia
IGSagdiyev@mephi.ru

Abstract. A low power area efficient 5 bit current steering DAC is presented. The proposed DAC is integrated to prototype the readout channel for muon chamber in CBM experiment. DAC was implemented with an area of 0.019 mm$^2$ in the CMOS process using UMS MMRF 180 nm technology. This DAC has ultralow power consumption - 25μW. The measured differential nonlinearity (DNL) is better than 0.25 LSB, integral nonlinearity (INL) is better than 0.2 LSB. In this paper the main steps of design flow, simulation results and measurement results are presented.

1. Introduction
A prototype readout channel for CBM experiment was designed and manufactured by the UMC 180 nm CMOS technology. The structure of the channel [1] is shown in figure 1. The analog part of channel includes a preamplifier, shaper, DAC, comparator and ADC. The comparator generates the start of conversion signal for ADC, when the signal from detector comes to the input of comparator. It is necessary to exclude false triggering by noise, so the threshold voltage of comparator must be adjustable.

![Figure 1. Structure of the channel](image-url)
One of the most wide-spread methods of adjusting voltage is doing that by a digital to analog converter. Because of the large number of channels in one chip, the proposed DAC must be low power and efficient by area on chip. Also, the threshold voltage adjustment must be quite accurate, so the proposed DAC must have a high linearity.

2. DAC structure
The DAC adjusts the differential threshold of comparator in the channel. The threshold is formed in differential driver by current injection by DAC. Thus, the proposed DAC has a binary weighted current steering architecture. This architecture is well suited for small resolution because of a low power consumption and small area on chip. Also, this architecture provides a high linearity of output current. The resolution of the DAC is caused by noise level and threshold range.

The proposed DAC consists of a biasing circuit, current matrix and output stage. The biasing circuit produces bias voltages for the correct work of current matrix. It is presented in figure 2. Current matrix consists of five current sources.

The schematic of current source is presented in figure 3. One of the most important parameters of the current source is linearity. Transistor mismatch in current sources causes the nonlinearity of the DAC [2].

Increasing the area of transistors in current sources reduces nonlinearity [3]. Thus, the transistors in the cascade (M1, M2) must have the maximum available channel length in the technology (50 μm). The series combination of current producing transistors M1 and M2 is implemented for the same unit current to achieve larger area and consequently a better matching and higher linearity. Another thing, which improves DAC nonlinearity, is a high output impedance of each current source. To increase output impedance a cascode transistor has been used. Because of the large area of main transistors M1 and M2, the output impedance is reduced. Since the cascode transistor does not affect the output current, it will not contribute any mismatch. Thus, the cascode transistor (M2) must have the minimum available channel length in the technology (180 nm). Also, to compensate the reduction of output impedance associated with the large current producing transistors, gain boosting has been used to increase the output impedance in each current cell [4]. To achieve high enough output impedance the feedback path should be implemented.

The output stage (not shown) is based on current mirrors and makes differential current signal to make differential threshold for the comparator.
3. Simulation
The main characteristics were simulated in Cadence Analog Design Environment (ADE) by using Monte-Carlo analysis. Since the designed DAC is static, the main static nonidealities, such as differential nonlinearity (DNL), integral nonlinearity (INL), gain error and offset, were simulated. DNL(k) is a vector that quantifies for each code k the deviation of this width from the "average" width (step size). DNL(k) is a measure of uniformity, it does not depend on gain and offset errors. Scaling and shifting a transfer characteristic does not alter its uniformity and hence DNL(k). DNL calculation is [5]:

\[
DNL(i) = \frac{I_{out}(i+1) - I_{out}(i)}{LSB} - 1
\]

Integral nonlinearity is the maximum between transfer characteristic and a straight line drawn through the endpoints from each relevant point of transfer characteristic. Just as with DNL, the INL of a converter is by definition independent of gain and offset errors. INL calculation:

\[
INL(i) = \frac{I_{out}(i) - I_{uniform}(i)}{LSB}
\]

Offset is the deviation of bottom endpoint from its ideal location. Gain error is the deviation of top endpoint from its ideal location with offset removed.

4. Layout
Layout of the proposed DAC is shown in figure 4. The chip was fabricated by UMC 180 nm CMOS technology and area of the DAC is 190 by 100 μm².

![Figure 4. Layout of the DAC](image)

5. Measurement results
Experimental results were obtained by using following instruments: pulse function arbitrary generation by Keysight 81160A, oscilloscope DSO9104H, probe station by Cascade Michrotech. Figure 5 and figure 6 show DNL and INL respectively, the maximum DNL and INL are 0.25 LSB and 0.2 LSB respectively. Offset error is 0.7 LSB, gain error is 3.5 LSB.
6. Conclusion
A 5 bit current steering low power area efficient DAC has been designed in UMC 180 nm CMOS technology. Main characteristics are presented in table 1. The DAC was designed in binary weighted architecture. To reduce nonlinearity two voltage driven transistors with maximum channel length were used in each current source. The power consumption is 25 μW at 1.8 V power supply. Presented DAC was integrated to prototype readout channel for CBM experiment at FAIR.

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