Proposal of a Takagi-Sugeno Fuzzy-PI Controller Hardware

Sérgio N. Silva\textsuperscript{a}, Felipe F. Lopes\textsuperscript{b}, Carlos Valderrama\textsuperscript{b}, Marcelo A. C. Fernandes\textsuperscript{a,c,1,*}

\textsuperscript{a}Laboratory of Machine Learning and Intelligent Instrumentation, Federal University of Rio Grande do Norte, Natal 59078-970, Brazil.
\textsuperscript{b}Department of Electronics & Microelectronics, Polytechnic Faculty, University of Mons, Mons, 7000, Belgium.
\textsuperscript{c}Department of Computer Engineering and Automation, Federal University of Rio Grande do Norte, Natal, RN, 59078-970, Brazil.

Abstract

This work proposes dedicated hardware for an intelligent control system on Field Programmable Gate Array (FPGA). The intelligent system is represented as Takagi-Sugeno Fuzzy-PI controller. The implementation uses a fully parallel strategy associated with a hybrid bit format scheme (fixed-point and other floating-point). Two hardware designs are proposed; the first one uses a single clock cycle processing architecture, and the other uses a pipeline scheme. The bit accuracy was tested by simulation with a non linear control system of robotic manipulator. The area, throughput, and dynamic power consumption of the implemented hardware are used to validate and compare the results of this proposal. The results achieved allow that the proposal hardware can use in several applications with high-throughput, low-power and ultra-low-latency restrictions such as teleportation of robot manipulators, tactile internet, industrial automation in industry 4.0, and others.

Keywords: FPGA, Hardware, Takagi-Sugeno, Fuzzy, Fuzzy-PI

1. Introduction

Systems based on Fuzzy Logic (FL), have been used in many industrial and commercial applications such as robotics, automation, control and classification problems. Unlike high data volume systems, such as Big Data and Mining of Massive Datasets (MMD) \cite{1,2,3}, one of the great advantages of Fuzzy Logic is its ability to work with incomplete or inaccurate information.

Intelligent systems based on production rules that use Fuzzy Logic in the inference process are called in the literature of Fuzzy Systems (FS) \cite{4}. Among the existing inference strategies, the most used, the Mamdani and the Takagi-Sugeno, are differentiated by the final stage of the inference process \cite{1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20}.

The interest in the development of dedicated hardware implementing Fuzzy Systems has increased due to the demand for high-throughput, low-power and ultra-low-latency control systems for emerging applications.
such as the tactile Internet \cite{21,22}, the Internet of Things (IoT) and Industry 4.0, where the problems associated with processing, power, latency and miniaturization are fundamental. Robotic manipulators used on tactile internet need a high-throughput and ultra-low-latency control system, and this can be achieved with dedicated hardware \cite{21}.

The development of dedicated hardware, in addition to speeding up parallel processing, makes it possible to operate with clocks adapted to low-power consumption \cite{23,24,25,26,27,28,29}. The works presented in \cite{30,31,32,33,34,35,36,37} propose implementations of FS on reconfigurable hardware (Field Programmable Gate Array - FPGA), showing the possibilities associated with the acceleration of fuzzy inference processes having a high degree of parallelization. Other works propose specific implementations of Fuzzy Control Systems (FCS) using the Fuzzy Mamdani Inference Machine (M-FIM) and the Takagi-Sugeno Fuzzy Inference Machine (TS-FIM) \cite{5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20}. The works presented in \cite{38,39,40} propose the Takagi-Sugeno hardware acceleration for other types of application fields.

This work aims to develop a new hardware proposal for a Fuzzy-PI controller with TS-FIM. Unlike most of the works presented, this project offers a fully parallel scheme associated with a hybrid platform using fixed-point and floating-point representations. Two TS-FIM hardware modules have been proposed, the first (here called TS-FIM module one-shot) takes one sample time to execute the TS-FIM, and the second (here called as TS-FIM module pipeline) uses registers inside the TS-FIM. Two Fuzzy-PI controller hardware have been proposed, one for the TS-FIM one-shot module and another for the TS-FIM module pipeline. The proposed hardware have been implemented, tested and validated on a Xilinx Virtex 6 FPGA. The synthesis results, in terms of size, resources and throughput, are presented according to the number of bits and the type of numerical precision. Already, the physical area on the target FPGA reaches less than 7%. The implementation achieved a throughput between 10 and 18Mps (Mega samples per second), and between 490 and 882 Mflips (Mega fuzzy logic inferences per second). Validation results on a feedback control system are also presented, in which satisfactory performance has been obtained for a small number of representation bits. Comparisons of results with other proposals in the literature in terms of throughput, hardware resources, and dynamic power savings will also be presented.

2. Related works

In \cite{30}, a high-performance FPGA Mamdani fuzzy processor is presented. The processor achieved a throughput of about 5 Mflips at a clock frequency about 40 MHz and it was designed for 256 rules and 16 inputs with 16 bits. The proposal used a semi-parallel implementation and thus reduced the number of the operations per Hz. The work presented in \cite{30} has about $\frac{5}{40} = 0.125$ flips/Hz and the work proposed here can achieve about $\frac{256+40}{40} = 256$ flips/Hz due the fully parallel hardware scheme used. The significant difference between throughput and operation frequency also implies a high power consumption \cite{41}. The work presented in \cite{39} uses a Mamdani inference machine and the throughput in Mflips is about 48.23 Mflips. The hardware was designed to operate with 8 bits, four inputs, 9 rules and one output. Similar to the work presented
in [30], the proposal introduced in [31] adopted a semi-parallel implementation, and this way decreased the throughput and increased power consumption. Other Mamdani implementations following the same strategy are also found in [32, 33, 34, 35].

A multivariate Takagi-Sugeno fuzzy controller on FPGA is proposed in [5]. The hardware is applied to the temperature and humidity controller for a chicken incubator and it was projected to two inputs, 6 rules and three outputs. When compared to other works, the hardware proposed in [5] achieved a low throughput about 6 Mflips. A hardware accelerator architecture for a Takagi-Sugeno fuzzy controller is proposed in [7] and this proposal achieved a throughput about 1.56 Msps with three inputs, two outputs and 24 bits.

In [11, 12, 13] a design methodology for rapid development of fuzzy controllers on FPGAs was developed. For the case with two inputs, 35 rules and one output (vehicle parking problem), the proposed hardware achieved a maximum clock about 66.251 MHz with 10 bits. However, the TS-FIM takes 10 clocks to complete the inference step, and this decreases the throughput, and it increases the power consumption.

The implementation presented in [14] aims at creating a hardware scheme of fuzzy logic controller on FPGA for the maximum power point tracking in photo-voltaic systems. The implementation takes 6 clocks cycles over 10 MHz and this is equivalent a throughput about \( \frac{10 \text{MHz}}{6} \approx 1.67 \text{Msps} \). In [16], a Mamdani fuzzy logic controller on FPGA was proposed. The hardware carries out a throughput of about 25 Mflips with two inputs, 49 rules.

The work presented in [17] implements a semi-parallel digital fuzzy logic controller on FPGA. The work achieved about 16 Msps per clock frequency of 200 MHz, that is, 0.08 Msps/MHz. On the other hand, this manuscript uses a fully parallel approach and it achieves 1 Msps/MHz, in other words, it can execute more operations per clock cycle. In the same direction, the proposals presented in [18, 20] shows a semi-parallel fuzzy control hardware with low-throughput, about 1 Msps.

Thus, this manuscript proposes a hardware architecture for the Fuzzy-PI control system. Unlike the works presented in the literature, the strategy proposed here uses a fully parallel scheme associated with a hybrid use in the bit format (fixed and floating-point). After several comparisons with other implementations of the literature, the scheme proposed here showed significant gains in processing speed (throughput) and dynamic power savings.

3. Takagi-Sugeno Fuzzy-PI Controller

Figure 1 shows the Fuzzy-PI intelligent control system operating a generic plant [41, 42, 43]. The plant output variable \( y(t) \) is called the controlled variable (or controlled signal), and it can admit several kinds of physical measurements such as level, angular velocity, linear velocity, angle, and others depending on the plant characteristics. The controlled variable, \( y(t) \), passes through a sensor that converts the physical measure into a proportional electrical signal that it is discretized at a sampling rate, \( t_s \), generating the signal, \( y(n) \).
The plant drives the kind of sensor that will be used. For level control in tanks used in industrial automation, the sensor can be characterized by the pressure sensor. For robotics applications (manipulators or mobile robotics), the sensor can be position sensor (capture angle information) or encoders sensor (capture angular or linear velocity information).

In the $n$-th time, the Fuzzy-PI controller (see Figure 1) uses the signal, $y(n)$, and it calculates the error signal, $e(n)$, and difference of error, $e_d(n)$. The signal $e(n)$ is expressed by

$$e(n) = y_{sp}(n) - y(n),$$

where the $y_{sp}(n)$ is the reference signal also called the set point variable and the signal $e_d(n)$ by

$$e_d(n) = e(n) - e(n - 1).$$

After the computation of the signals $e(n)$ and $e_d(n)$, the Fuzzy-PI controller generate the signals $x_1(n)$ and $x_2(n)$, which can be expressed as

$$x_0(n) = K_p \times e_d(n)$$

and

$$x_1(n) = K_i \times e(n).$$

The variables $K_p$ and $K_i$ represent the proportional gain and the integration gain, respectively. Subsequently, the signals $x_0(n)$ and $x_1(n)$ are sent to the fuzzy Takagi-Sugeno inference, called in this article of Takagi-Sugeno - Fuzzy Inference Machine (TS-FIM) (see Figure 1).

The TS-FIM is formed by three stages called fuzzification, operation of the rules (or rules evaluation) and defuzzification (or output function). In the fuzzification each $i$-th input signal $x_i(n)$ is applied to a set of $F_i$ pertinence functions whose output can be expressed as

$$f_{i,j}(n) = \mu_{i,j}(x_i(n)) \text{ for } j = 0, \ldots, F_i,$$

where, $\mu_{i,j}(\cdot)$ is the $j$-th membership function of the $i$-th input and $f_{i,j}(n)$ is the output of the fuzzification step associated with the $j$-th membership function and the $i$-th input in the $n$-th time. For two inputs, $x_0(n)$ and $x_1(n)$, the membership functions can be expressed as

$$\mu_{0,j}(x_0(n)) = \frac{1}{1 + \left(\frac{x_0(n) - \delta_j}{\Delta_j}\right)^2} \text{ for } j = 0, \ldots, F_0,$$

$$\mu_{1,j}(x_1(n)) = \frac{1}{1 + \left(\frac{x_1(n) - \delta_j}{\Delta_j}\right)^2} \text{ for } j = 0, \ldots, F_1,$$

where, $\delta_j$ and $\Delta_j$ are the parameters used to shape the membership functions. The output of the fuzzification step is the set of membership functions, $f_{i,j}(n)$, for each input in the $n$-th time.
and \( x_1(n) \), the TS-FIM generates a set of \( F_0 + F_1 \) fuzzy signals (\( f_{0,j} \) and \( f_{1,j} \)) and these signals are processed by a set of \( F_0 F_1 \) rules in the operation (or evaluation) phase. Each \( g \)-th rule can be expressed as

\[
o_g = \min(f_{0,l}, f_{1,k}) \text{ for } g = 0, \ldots, (F_0 F_1) - 1,
\]

where \( g = F_0 l + k \) for \((l, k) = (0, 0), (0, 1), \ldots, (F_0 - 1, F_1 - 1)\). Finally, the output (defuzzification) of TS-FIM, called here \( v_d(n) \), can be expressed as

\[
v_d(n) = \frac{a(n)}{b(n)} = \frac{\sum_{g=1}^{(F_0 F_1)-1} a_g}{\sum_{g=0}^{(F_0 F_1)-1} a_g} = \frac{\sum_{g=1}^{(F_0 F_1)-1} a_g \times (A_g x_0(n) + B_g x_1(n) + C_g)}{\sum_{g=0}^{(F_0 F_1)-1} a_g},
\]

where \( A_g, B_g \) and \( C_g \) are parameters defined during the project [4]. Thus it can be said that every \( n \)-th instant TS-FIM receives as input \( x_0(n) \) and \( x_1(n) \) and generates as output \( v(n) \), that is,

\[
v_d(n) = TSFIM(x_0(n), x_1(n)),
\]

where \( TSFIM(\cdot) \) is a function that represents TS-FIM.

After the TS-FIM processing, the Fuzzy-PI controller integrates the signal \( v_d(n) \) generating the signal \( v(n) \) (see Figure 1). The signal is the output of the Fuzzy-PI controller, and it can be expressed as

\[
v(n) = v_d(n) + v(n - 1).
\]

The signal \( v(n) \) is saturated between \( v_{\min} \) and \( v_{\max} \), generating the signal \( r(n) \) that it is expressed as

\[
r(n) = \begin{cases} 
  v_{\max} & \text{for } v(n) > v_{\max} \\
  v(n) & v(n) < v_{\max} \\
  v_{\min} & \text{for } v(n) < v_{\min}
\end{cases}
\]

Finally, the signal \( r(n) \) is sent to a actuator, which transforms the discrete signal into a continuous signal, \( r(t) \), to be applied to the plant.

4. Hardware Proposal

Figure 2 presents the general structure of the proposed hardware in which it consists of three main modules called Input Processing Module (IPM), TS-FIM Module (TS-FIMM) and Integration Module (IM). The hardware was developed for the most part using a fixed-point format for the variables, in which, for any given variable, the notations \([uT.W]\) and \([sT.W]\) indicate that the variable is formed by \( T \) bits of which \( W \) are intended for the fractional part and the symbols "s" and "u" indicate that the variable is signed or unsigned, respectively. For the case of signed variables, type \( s \), the number of bits destined for the integer part is characterized as \( T - W - 1 \) and for unsigned variables, type \( u \), the number of bits is \( T - W \) for the integer part.
4.1. Input Processing Module (IPM)

The IPM (shown in Figure 3) is responsible for processing the control signal generated by the plant to the input of the Fuzzy-PI controller. The IPM computes the Equations 1, 2, 3 and 4. The signals associated with this module were implemented with $M$ bits where, one is reserved for the sign and $N$ for the fractional part where, the value of $M$ can be expressed as

$$M = N + \log_2 (\lceil y_{\text{max}} \rceil) + 1,$$

where $y_{\text{max}}$ represents the maximum value, in modulus, of the process variable, $y(n)$. The values of $K_p$ and $K_i$ should be designed to try to maintain the output signals of the module, $x_0[V.N](n)$ and $x_1[V.N](n)$, between $-1$ and $1$, respectively. In this way, you can set $V = N + 1$, aiming at reducing the number of bits associated with the project. It is important to note that the two gain modules, $K_p$ and $K_i$, also saturate the signal in $[V.N](n)$ bits after multiplication.

4.2. TS-FIM Module (TS-FIMM)

The TS-FIMM is composed of three hardware components: Membership Function Module (MFM), Operation Module (OM) and Output Function Module (OFM). The MFM is the first module associated with TS-FIMM and it corresponds to the fuzzification process, the OM component completes the rules evaluation
phase and the OFM performs the defuzzification step (see Section 3). This work proposes two designers for TS-FIMM.

The first one, presented in Figure 4 and called here as TS-FIMM One-Shot (TS-FIMM-OS), performs all modules MFM, OM, and OFM in one sample time, in other words, it takes one sample time to generate the $n$-th output associated of the $n$-th input. The second, presented in Figure 5 and called here as TS-FIMM Pipeline (TS-FIMM-P), used registers (blocks called R in the Figure 4) among the input, MFM, OM, OFM and output. The TS-FIMM-P takes four sample time to perform all modules MFM, OM, and OFM, in other words, there is a delay of the four samples between the $n$-th output and $n$-th input.

Figure 4: Hardware architecture of TS-FIMM One-Shot (TS-FIMM-OS).

Figure 5: Hardware architecture of TS-FIMM Pipeline (TS-FIMM-P).

The TS-FIMM-OS will have a longer sample time than TS-FIMM-P because the critical path is also longer; however, the TS-FIMM-OS does not have a delay. It is important to empathize that the delay inside the feedback control can take a system to instability. The instability degree depends on the system and how long is the delay. The instability will depend on the characteristics of the system and the size of the delay.
4. On the other hand, the pipeline scheme associated with TS-FIMM-P has a short sample time (short critical path), and this permits a high-throughput when it compares to TS-FIMM.

4.2.1. Membership Function Module (MFM)

In the MFM, each \( i \)-th input variable is associated with a module that collects \( F_i \) membership functions, called here Membership Function Group (MFG). Figure 6 shows the \( i \)-th MFG, called of the MFG-\( i \), related with the \( i \)-th input, \( x_i[sV.N](n) \).

Each MFG-\( i \) collects \( F_i \) membership functions (see Figure 6) called MF-\( ij \) and each module MF-\( ij \) implements the \( j \)-th membership function associated with the \( i \)-th input, \( \mu_{i,j}(x_i(n)) \). In every \( n \)-th time instant all membership functions, \( \sum_i F_i \), are executed in parallel and at the output of each MF-\( ij \) is generated a \( N \) bits signal of type \( u \) and without the integer part, called \( f_{i,j}[uN.N](n) \) (see Figure 6). The Fuzzy-PI controller proposed here uses \( F_0 + F_1 \) membership functions.

Figure 7 shows the membership functions implemented in the MFM. For both variables, \( x_0[sV.N](n) \) and \( x_1[sV.N](n) \), seven functions of pertinence were created (trapezoidal type in the extremes and triangular in the remaining). The linguistic terms associated with membership functions are Large Negative (LN), Moderate Negative (MN), Small Negative (SN), Zero (ZZ), Small Positive (SP), Moderate Positive (MP) and Large Positive (LP).

*Figure 6: Hardware architecture of module MFG-\( i \) associated with the \( i \)-th input, \( x_i[sV.N](n) \).*

*Figure 7: Membership functions from inputs \( x_0[sV.N](n) \) and \( x_1[sV.N](n) \).*
Each \( j \)-th membership function associated with \( i \)-th input was implemented directly on hardware based on the following expressions

\[
\mu_{i,j}^{RT}(x_i[sV.N](n)) = \begin{cases} 
0 & \text{if } x_i[sV.N](n) > d_{i,j}[sW.T] \\
G_{i,j}^{RT}(n) & \text{if } c_{i,j}[sW.T] \leq x_i[sV.N](n) \leq d_{i,j}[sW.T], \\
1 & \text{if } x_i[sV.N](n) < c_{i,j}[sW.T] 
\end{cases}
\]

(12)

being \( \mu_{i,j}^{RT}(\cdot) \) the trapezoidal function on the right, \( c_{i,j}[sW.T] \) and \( d_{i,j}[sW.T] \) are constants (\( c_{i,j}[sW.T] < d_{i,j}[sW.T] \)) and

\[
G_{i,j}^{RT}(n) = \frac{d_{i,j}[W.T] - x_i[sV.N](n)}{d_{i,j}[W.T] - c_{i,j}[W.T]},
\]

(13)

where \( W \) and \( T \) are the number of bits in the integer and fractional part relative to the constants of the \( j \)-th activation function associated with \( i \)-th input. For the trapezoidal of the left one has

\[
\mu_{i,j}^{LT}(x_i[sV.N](n)) = \begin{cases} 
0 & \text{if } x_i[sV.N](n) < e_{i,j}[sW.T] \\
G_{i,j}^{LT}(n) & \text{if } e_{i,j}[sW.T] \leq x_i[sV.N](n) \leq f_{i,j}[sW.T], \\
1 & \text{if } x_i[sV.N](n) > f_{i,j}[sW.T] 
\end{cases}
\]

(14)

with \( \mu_{i,j}^{LT}(\cdot) \) the left trapezoidal function, \( e_{i,j}[sW.T] \) and \( f_{i,j}[sW.T] \) constants (\( e_{i,j}[sW.T] < f_{i,j}[sW.T] \)) and

\[
G_{i,j}^{LT}(n) = \frac{x_i[sV.N](n) - e_{i,j}[W.T]}{f_{i,j}[W.T] - e_{i,j}[W.T]}.
\]

(15)

Finally, for the triangular membership function is expressed as

\[
\mu_{i,j}^{T}(x_i[sV.N](n)) = \begin{cases} 
\mu_{i,j}^{LT}(x_i[sV.N](n)) & \text{if } x_i[sV.N](n) < m_{i,j}[sW.T] \\
\mu_{i,j}^{RT}(x_i[sV.N](n)) & \text{if } x_i[sV.N](n) \geq m_{i,j}[sW.T] 
\end{cases},
\]

(16)

where \( m_{i,j}[sW.T] \) is the triangle center point, that is, \( m_{i,j}[sW.T] = c_{i,j}[sW.T] = f_{i,j}[sW.T] \). The values of \( W \) and \( T \) will set the resolution of the activation functions. In the implementation proposed in this work, the value of \( W \) is always expressed as \( W = 2 \times T + 1 \). The use of non-linear pertinence functions can be accomplished by applying Lookup Tables (LUTs) in the implementation.

Although this implementation uses only two inputs \( x_0[sV.N](n) \) and \( x_1[sV.N](n) \) and seven membership functions for each input, this can be easily extended for more inputs and functions, since the entire implementation is performed in parallel.

4.2.2. Operation Module (OM)

The \( F_0 + F_1 \) outputs from the MFM module are passed to the OM module that performs all operations relative to the \( F_0F_1 \) rules, as described in Equation [6] on Section 3. Figure 8 details the hardware structure of one of the \( F_0F_1 \) operating modules, here called O-\( lk \), which performs the minimum operation ("AND" connector) between the \( l \)-th membership function from input 0, \( f_{0,l}[nN.N](n) \), with the \( k \)-th membership function from input 1, \( f_{1,k}[uN.N](n) \) (see Equation [7]).
4.2.3. Output Function Module (OFM)

The OFM, illustrated in Figure 9, performs the generation of the TS-FIMM output variable during the step called defuzzification. This step essentially corresponds to the implementation of the Equation 7 presented in Section 3. The blocks called NM and DM perform the numerator and denominator operations presented in Equation 7, respectively.

Figures 10 and 11 show the hardware implementation of the NM. The NM is composed of the $F_0F_1$ hardware components called WM-$g$ and an adder tree structure. Each $g$-th WM-$g$, detailed in Figure 11, is a parallel hardware implementation of the variable $a_g$ presented in Equation 7. The $F_0F_1$ WMs hardware components are also implemented in parallel and they generated $F_0F_1$ signals $a_g[\text{sH.N}](n)$ in each $n$-th time instant. Since $-1 < x_0[\text{V.N}](n) < 1$, $-1 < x_1[\text{V.N}](n) < 1$, $0 < a_g[\text{uN.N}](n) < 1$, $-1 < A_g < 1$, $-1 < B_g < 1$ and $-1 < C_g < 1$ for $g = 0, \ldots, F_0F_1$ the variable $H$ can be expressed as $H = N + 3$.

The adder tree structure, illustrated in Figure 10 has a depth expressed as $\log_2([F_0F_1])$ thus the output signal $a(n)$ (see Equation 7) can be performed as $a[\text{sP.N}](n)$ where

$$P = H + \log_2([F_0F_1]).$$

The DM, presented in Figure 12 is characterized with an adder tree structure with depth also expressed as
\[ \log_2([F_0 F_1]). \] The output signal of DM can be expressed as \( b[sQ.N](n) \) where

\[ Q = N + \log_2([F_0 F_1]) + 1. \] (18)

For the division calculation, the output signals, in fixed-point, of the NM and DM modules \( a[sP.N](n) \) and \( b[sQ.N](n) \) are transformed to a 32-bit floating-point (IEEE754) standard by the Fixed-point to Float (FP2F) module \( (\tilde{a}[\text{Float32}](n) \text{ e } \tilde{b}[\text{Float32}](n)) \) and after division the TS-FIMM output is converted back into fixed-point by the Float to Fixed-point (F2FP) module.

Since the TS-FIMM inputs and the values of \( A_g, B_g \) and \( C_g \) are between \(-1\) and \(1\), it can be guaranteed, from Equation 7, that the output, \( v_d[sV.N](n) \), continue normalized between \(-1\) and \(1\). Thus, one can use the same input resolution, that is, \( N \) for the fractional part and \( V = N + 1 \) for the integer part, as shown in Figure 9.
4.3. Integration Module (IM)

The IM, shown in Figure 13, implements the Equation 9 presented in Section 3. This module is the last step on the Fuzzy-PI hardware and it is composed of the accumulator with a saturation. The output signal, \( r(n) \), is expressed as \( r[\text{sG.N}](n) \) where

\[
G = N + \log_2([v_{\text{max}} - v_{\text{min}}]) + 1.
\]  

(19)

5. Synthesis Results

The synthesis results were obtained to Fuzzy-PI controller (see Figure 2) and also to specific modules TS-FIMM-OS (see Figure 4) and TS-FIMM-P (see Figure 5). The separate synthesis of the TS-FIMM allows to analysis of the Fuzzy inference algorithm core in the complete hardware proposal. All synthesis results used an FPGA Xilinx Virtex 6 xc6vlx240t-1ff1156 and that has 301,440 registers, 150,720 logical cells to be used as LUTs and 768 multipliers.
5.1. Synthesis Results - TS-FIMM Hardware

Tables 1 and 2 present the synthesis results related to hardware occupancy and the maximum throughput, \( R_s = \frac{1}{t_s} \), in Mega samples per second (Mps) of the system for several values of \( N \) and \( T \). Tables 1 and 2 show the synthesis results associated with TS-FIMM-OS and TS-FIMM-P, respectively. The columns, NR, NLUT and NMULT represent the number of registers, logic cells used as LUTs and multipliers in the hardware implemented in the FPGA, respectively. The PNR, PNLUT, and NMULT columns represent the percentage relative to the total FPGA resources.

| N  | T   | NR   | PR     | NLUT     | PLUT    | NMULT  | PNMULT | \( t_s \) (ns) | \( R_s \) (Mps) |
|----|-----|------|--------|----------|---------|--------|--------|--------------|--------------|
| 4  | 8   | 217  | 0.07%  | 6339     | 421     | 49     | 6381   | 79.72       | 12.54        |
| 8  | 8   | 49   | 4.38%  | 6452     | 4.28%   | 79     | 6904   | 81.96       | 12.20        |
| 10 | 10  | 6598 | 4.38%  | 6452     | 4.28%   | 79     | 6404   | 81.96       | 12.20        |

Synthesis results show that the hardware proposal for TS-FIMM takes up a small hardware space of less than 1%, PR, in registers and less than 7% in LUTs, PLUT, of the FPGA (see Tables 1 and 2). These results enable the use of several TS-FIMM implemented in parallel on FPGA, allowing to accelerate several applications in massive data environments. On the other hand, the low hardware consumption allows the use of TS-FIMM in small FPGAs of low cost and consumption for applications of IoT and M2M. Another
Table 2: Synthesis results (hardware requirement and time) associated with TS-FIMM-P hardware.

| N  | T  | NR   | PR     | NLUT  | PLUT  | NMULT | PNMULT | t_s (ns) | R_s (Msps) |
|----|----|------|--------|-------|-------|--------|--------|----------|------------|
| 8  | 4  | 746  | 0.25%  | 5326  | 3.53% | 5350   | 3.55%  | 5326     | 16.72      |
| 8  | 6  | 5422  | 3.60%  | 5422  | 3.60% | 5422   | 3.60%  | 5422     | 17.80      |
| 10 |    | 5590  | 3.71%  | 5590  | 3.71% | 5590   | 3.71%  | 5590     | 17.55      |
| 8  | 6  | 6093  | 4.04%  | 6093  | 4.04% | 6093   | 4.04%  | 6093     | 17.48      |
| 8  | 10 | 6141  | 4.07%  | 6141  | 4.07% | 6141   | 4.07%  | 6141     | 17.28      |
| 10 |    | 6199  | 4.11%  | 6199  | 4.11% | 6199   | 4.11%  | 6199     | 17.35      |
| 8  | 6  | 6317  | 4.19%  | 6317  | 4.19% | 6317   | 4.19%  | 6317     | 17.63      |
| 10 |    | 6910  | 4.58%  | 6910  | 4.58% | 6910   | 4.58%  | 6910     | 17.27      |
| 8  | 6  | 7016  | 4.65%  | 7016  | 4.65% | 7016   | 4.65%  | 7016     | 17.06      |
| 10 |    | 7172  | 4.76%  | 7172  | 4.76% | 7172   | 4.76%  | 7172     | 17.77      |
| 12 | 6  | 1113  | 0.37%  | 1113  | 0.37% | 1113   | 0.37%  | 1113     | 17.06      |
| 8  | 6  | 1301  | 0.43%  | 1301  | 0.43% | 1301   | 0.43%  | 1301     | 17.16      |
| 10 |    | 7823  | 5.19%  | 7823  | 5.19% | 7823   | 5.19%  | 7823     | 17.18      |
| 8  | 6  | 7905  | 5.24%  | 7905  | 5.24% | 7905   | 5.24%  | 7905     | 17.16      |
| 10 |    | 8031  | 5.33%  | 8031  | 5.33% | 8031   | 5.33%  | 8031     | 16.66      |
| 14 | 6  | 8713  | 5.78%  | 8713  | 5.78% | 8713   | 5.78%  | 8713     | 16.83      |
| 16 | 6  | 8737  | 5.80%  | 8737  | 5.80% | 8737   | 5.80%  | 8737     | 17.20      |
| 8  | 6  | 8819  | 5.85%  | 8819  | 5.85% | 8819   | 5.85%  | 8819     | 17.27      |
| 10 |    | 8955  | 5.94%  | 8955  | 5.94% | 8955   | 5.94%  | 8955     | 16.98      |

An important point to be analyzed, still in relation to the synthesis, is the linear behavior of the hardware consumption in relation to the number of bits, unlike the work presented in [45], and this is important, since it makes possible the use systems with higher resolution.

The values of throughput, $R_s$, were very relevant, with values about 11.5Msps for TS-FIMM-OS and values about 17Msps for TS-FIMM-P. These values enables its application in various large volume problems for processing as presented in [30] or in problems with fast control requirements such as tactile internet applications [22, 21]. It is also observed that throughput has a linear behavior as a function of the number of bits.

The TS-FIMM-P has a speedup about $1.47 \times \left( \frac{17 \text{Msps}}{11.5 \text{Msps}} \right)$ regards the TS-FIMM-OS. This speedup was driven by the critical path reduction with the pipeline scheme. However, the pipeline scheme in TS-FIMM-P used about 3.4× registers (NR) more than TS-FIMM-OS.

The figures 14 and 15 show the behavior surfaces of the number of LUTs (NLUT) and throughput in
function of N and T for TS-FIMM-OS, respectively. For both cases an adjustment was made, through a regression technique, to find the plane that best matches the measured points. For the case of NLUT, the plane, $f_{\text{NLUT}}(N, T)$ expressed by

$$f_{\text{NLUT}}(N, T) \approx 1682 + 532.2 \times N + 6.493 \times 10^{-13} \times T,$$

(20)

with a $R^2 = 0.9766$. For throughput in MspS was found a plane, $f_{R_s}(N, T)$, characterized as

$$f_{R_s}(N, T) \approx 13.24 - 0.1163 \times N + 3.414 \times 10^{-16} \times T,$$

(21)

with $R^2 = 0.7521$.

![Figure 14](image1.png)

Figure 14: Plane, $f_{\text{NLUT}}(N, T)$, found to estimate the number of LUTs in function of the number of bits N and T for TS-FIMM-OS.

![Figure 15](image2.png)

Figure 15: Plane, $f_{R_s}(N, T)$, found to estimate throughput, $R_s$, for different number of bits N and T for TS-FIMM-OS.

The behavior surfaces of the number of LUTs (NLUT) and throughput in function of N and T for TS-FIMM-P are presented in Figures 16 and 17 respectively. For the case of NLUT, the plane, $f_{\text{NLUT}}(N, T)$ expressed by

$$f_{\text{NLUT}}(N, T) \approx 1171 + 491.1 \times N + 4.245 \times 10^{-13} \times T,$$

(22)
with a $R^2 = 0.9838$. For throughput in Mps was found a plane, $f_{R_s}(N, T)$, characterized as

$$f_{R_s}(N, T) \approx 18.48 - 0.09704 \times N - 5.365 \times 10^{-16} \times T,$$

(23)

with $R^2 = 0.5366$.

Figure 16: Plane, $f_{NLUT}(N, T)$, found to estimate the number of LUTs in function of the number of bits $N$ and $T$ for TS-FIMM-P.

Figure 17: Plane, $f_{R_s}(N, T)$, found to estimate throughput, $R_s$, for different number of bits $N$ and $T$ for TS-FIMM-P.

5.2. Synthesis Results - Fuzzy-PI Controller Hardware

Tables 3 and 4 present the synthesis results related to hardware occupancy and throughput, $R_s$ for the Fuzzy-PI controller hardware (see Figure 2). The results are presented for several values of $N$ and $T = 10$.

Synthesis results, drawn on Table 3 and 4, show that the proposed implementation requires a small fraction of hardware space, less than 1% PR, in registers and less than 8% in LUTs, PLUT, of the FPGA. In addition, it is possible to see the numbers of embedded multipliers, PNMULT, remained below 7%. This occupation enables the use of several Fuzzy-PI controllers in parallel in the same FPGA hardware and this allows various controls systems running in parallel on industrial applications. The low size implementation also allows the use in low cost and power consumption IoT and M2M applications. Regarding throughput,
Table 3: Synthesis results (hardware requirement and time) associated with Fuzzy-PI controller hardware with TS-FIMM-OS.

| N  | NR | PR    | NLUT | PLUT | NMULT | PNMULT | ts (ns) | Rs (Mps) |
|----|----|-------|------|------|-------|--------|---------|----------|
| 8  | 261| ≈ 0.09% | 6834 | ≈ 4.53% | 49 | ≈ 6.38% | 92.87 | 10.77 |
| 10 | 307| ≈ 0.10% | 7331 | ≈ 4.86% | 49 | ≈ 6.38% | 98.44 | 10.16 |
| 12 | 375| ≈ 0.12% | 8409 | ≈ 5.58% | 49 | ≈ 6.38% | 98.68 | 10.13 |
| 14 | 438| ≈ 0.15% | 9460 | ≈ 6.28% | 49 | ≈ 6.38% | 99.98 | 10.00 |
| 16 | 488| ≈ 0.16% | 10595| ≈ 7.03% | 49 | ≈ 6.38% | 104.31| 9.59   |

Table 4: Synthesis results (hardware requirement and time) associated with Fuzzy-PI controller hardware with TS-FIMM-P.

| N  | NR | PR    | NLUT | PLUT | NMULT | PNMULT | ts (ns) | Rs (Mps) |
|----|----|-------|------|------|-------|--------|---------|----------|
| 8  | 790| ≈ 0.26% | 5826 | ≈ 3.87% | 49 | ≈ 6.38% | 66.08 | 15.13 |
| 10 | 965| ≈ 0.32% | 6317 | ≈ 4.19% | 49 | ≈ 6.38% | 72.16 | 13.86 |
| 12 | 1164| ≈ 0.39% | 7434 | ≈ 4.93% | 49 | ≈ 6.38% | 68.95 | 14.50 |
| 14 | 1355| ≈ 0.45% | 8328 | ≈ 5.53% | 49 | ≈ 6.38% | 73.23 | 13.66 |
| 16 | 1537| ≈ 0.51% | 9298 | ≈ 6.17% | 49 | ≈ 6.38% | 74.56 | 13.41 |

R_s, the results obtained were highly relevant, with values between 15.33, and 13.41 Msp. Which enables its application in several problems with large data volume for processing as presented in [30] or in problems with fast control requirements such as tactile internet applications [21].

6. Validation Results

6.1. Validation Results - TS-FIMM Hardware

The Figures 18 and 19 show the mapping between input (x_0(n) and x_1(n)) and output v_d(n) for proposed hardware and a reference implementation with Fuzzy Matlab Toolbox (License number 1080073) [46], respectively. The Matlab implementation, shown in Figure 19 uses floating-point format with 64 bits (double precision) while in Figure 18 the proposed hardware-generated mapping is presented using lower resolution synthesized (N = 8, V = 9 and T = 4). These figures are able to present a qualitative representation of the proposed implementation, in which the obtained results are quite similar to those expected.

The Table 5 shows the mean square error (MSE) between the Fuzzy Matlab Toolbox and the proposed hardware implementation for several cases N and T. For the experiment, the calculation of MSE is expressed as

\[
MSE = \frac{1}{Z} \sum_{n=0}^{Z-1} (v_{ref}[Float64](n) - v_d[sV.N](n))^2, \quad (24)
\]

where Z represents the number of tested points that corresponded to 10000 points spread evenly within the limits of the input values (−1 and 1). The Figures 18 and 19 were generated with these points.
The results obtained in relation to $MSE$ were also quite significant, showing that the TS-FIMM hardware has a response quite similar to the implementation with 64 bits even for a fixed-point resolution of 8 bits ($MSE = 2.395 \times 10^{-6}$). Another interesting fact was related to the values of $T$ that did not significantly influence the $MSE$ value for the pertinence functions used (see Figure 7) in the project. It is important to note that the implementation of TS-FIMM hardware with few bits leads to smaller hardware, low-power consumption or high-throughput values.

6.2. Validation Results - Fuzzy-PI Controller Hardware

In order to validate the results of the Fuzzy-PI controller in hardware, bit-precision simulation tests were performed with a non-linear dynamic system characterized by a robotic manipulator system called the Phantom Omni [47, 48, 49, 50]. The Phantom Omni is a 6-Degree Of Freedom) manipulator, with rotational joints. The first three joints are actuated, while the last three joints are non-actuated. As illustrated in Figure 20, the device can be modeled as 3-Degree robotic manipulator with two segments $L_1$ and $L_2$. The segments are interconnected by three rotary joints angles $\theta_1$, $\theta_2$ and $\theta_3$. The Phantom Omni has been widely used in literature, as presented in [47, 48, 49]. Simulations used $L_1 = 0.135$ mm, $L_2 = L_1$, $L_3 = 0.025$ mm and $L_4 = L_1 + A$ where $A = 0.035$ mm as described in [49].

Non-linear, second order, ordinary differential equation used to describe the dynamics of the Phantom Omni can be expressed as

$$
\mathbf{M}(\mathbf{\theta}(t)) \ddot{\mathbf{\theta}}(t) + \mathbf{C} \left( \mathbf{\dot{\theta}}(t), \mathbf{\ddot{\theta}}(t) \right) \dot{\mathbf{\theta}}(t) + \mathbf{g}(\mathbf{\theta}(t)) - \mathbf{f}(\mathbf{\dot{\theta}}(t)) = \tau(t)
$$

(25)

where $\mathbf{\theta}(t)$ is the vector of joints expressed as

$$
\mathbf{\theta}(t) = \begin{bmatrix} \theta_1(t) & \theta_2(t) & \theta_3(t) \end{bmatrix}^T \in \mathbb{R}^{3 \times 1},
$$

(26)
\[ \tau(t) = \begin{bmatrix} \tau_1(t) & \tau_2(t) & \tau_3(t) \end{bmatrix}^T \in \mathbb{R}^{3 \times 1}, \] (27)

\[ \mathbf{M} (\theta(t)) \in \mathbb{R}^{3 \times 3} \text{ is the inertia matrix, } \mathbf{C} (\theta(t), \dot{\theta}(t)) \in \mathbb{R}^{3 \times 3} \text{ is the Coriolis and centrifugal forces matrix, } \mathbf{g} (\theta(t)) \in \mathbb{R}^{3 \times 1} \text{ represents the gravity force acting on the joints, } \theta(t), \text{ and the } f \left( \dot{\theta}(t) \right) \text{ is the friction force on the joints, } \theta(t). \]

Figure 21 shows the simulated system where the plant is the 3-DOF Phantom Omni robotic manipulator. The controlled variables are the angular position of the joints \( \theta_1, \theta_2 \) and \( \theta_3 \) and the actuator variables are the torques \( \tau_1, \tau_2 \) and \( \tau_3 \). The control system has three angular position sensors and each \( i \)-th Sensor-\( i \) convert the \( i \)-th continuous angle signal, \( \theta_i(t) \) to discrete angle signal, \( \theta_i(n) \). There are three Fuzzy-PI hardware running in parallel and every \( i \)-th Sensor-\( i \) is connected with a Fuzzy-PI hardware, Fuzzy-PI-\( i \). Each \( i \)-th Fuzzy-PI-\( i \) hardware generates the \( i \)-th discrete torques acting signal, \( \tau_i(n) \), and every \( i \)-th discrete torque signal, \( \tau_i(n) \), is connected to \( i \)-th actuator, Actuator-\( i \). Finally, each \( i \)-th actuator, Actuator-\( i \), generates the \( i \)-th continuous torque signal, \( \tau_i(t) \) to the applied on the robotic manipulator. The set point variables (or reference signal) are angular position of the joints and they are expressed by \( \theta_{1sp}(n), \theta_{2sp}(n) \) and \( \theta_{3sp}(n) \).

Figures 22, 23 and 24 present the hardware validation results for various resolutions in terms of the number of bits of the fractional part, \( N = \{12, 14, 16\} \) for discrete controlled variables \( \theta_1(n), \theta_2(n) \) and \( \theta_3(n) \), respectively. The simulation trajectory was of 10 seconds and every 2 seconds was changing. Table 6 shows the angle trajectory changing for set point variables \( \theta_{1sp}(n), \theta_{2sp}(n) \) and \( \theta_{3sp}(n) \). Simulations used \( t_s = 1 \times 10^{-5}, Kp = 2000 \) and \( Ki = 0.1 \) for each \( i \)-th Fuzzy-PI-\( i \) hardware.

In the results presented in Figures 22, 23 and 24 it is possible to observed that the controller followed
Table 5: Mean square error (MSE) between the Fuzzy Matlab Toolbox and the proposed hardware implementation for several cases $N$ and $T$.

| $N$ | $T$ | $MSE$ (see Equation 24) |
|-----|-----|--------------------------|
| 4   | 6   | $2.4 \times 10^{-6}$     |
| 8   | 8   |                           |
| 10  |     |                           |
| 4   | 6   | $1.3 \times 10^{-7}$     |
| 10  |     |                           |
| 4   | 6   | $7.2 \times 10^{-9}$     |
| 10  |     |                           |
| 4   | 6   | $4.9 \times 10^{-10}$    |
| 10  |     |                           |
| 4   | 6   | $2.7 \times 10^{-11}$    |
| 10  |     |                           |

the plant reference in all cases. Results also showed that the Takagi-Sugeno Fuzzy-PI hardware proposal has been following the reference even for a small amount of bits, that is, a low resolution.

7. Comparison with other works

7.1. Throughput comparison

Table 7 shows a comparison with other works in the literature. Parameters like inference machine (IM) type (Takagi-Sugeno or Mamdani), number of inputs (NI), number of rules (NR), number of outputs (NO), number of bits (NB), throughput in Msps, $R_s$, and Mflips (Mega fuzzy logic inference per second) are showed. In additional, Table 7 also shows the speedups (in Msps and Mflips) achieved of the TS-FIMM-OS, TS-FIMM-P, Fuzzy-PI controller with TS-FIMM-OS (Fuzzy-PI-OS) and with TS-FIMM-P (Fuzzy-PI-P) over the other works in the literature. The value in flips can be calculated as $NR \times R_s$.

In the work presented in [11], the results were obtained for several cases and for one with two inputs, 35 rules and one output (vehicle parking problem) the proposed hardware achieved a maximum clock about
Figure 20: Structure of 3-DOF Phantom Omni robotic manipulator.

Table 6: Angle trajectory changing for set point variables $\theta_1^{sp}(n), \theta_2^{sp}(n)$ and $\theta_3^{sp}(n)$.

| Set point          | $0 - 2\,s$ | $2\,s - 4\,s$ | $4\,s - 6\,s$ | $6\,s - 8\,s$ | $8\,s - 10\,s$ |
|--------------------|------------|----------------|----------------|----------------|-----------------|
| $\theta_1^{sp}(n)$ | 90°        | 0°             | 45°           | -45°          | 90°             |
| $\theta_2^{sp}(n)$ | 45°        | 45°            | 0°            | 22.5°         | 45°             |
| $\theta_3^{sp}(n)$ | 45°        | 22.5°          | 0°            | 22.5°         | 45°             |

66.251 MHz with 10 bits [12, 13]. However, the FIM takes 10 clocks to complete the inference step; in other words, the hardware proposal in [11] achieves a throughput in Msps of about $\frac{66.251}{10} \approx 6.63$ Msps and in Mflips of about $6.63 \times 35 \approx 232.05$ Mflips. The speedup in Msps for the TS-FIMM-OS, TS-FIMM-P, Fuzzy-PI-OS and Fuzzy-PI-P are $\frac{12.05\,\text{Msps}}{0.63\,\text{Msps}} \approx 1.92$, $\frac{17.63\,\text{Msps}}{6.63\,\text{Msps}} \approx 2.66$, $\frac{10.16\,\text{Msps}}{6.63\,\text{Msps}} \approx 1.53$, and $\frac{13.86\,\text{Msps}}{6.63\,\text{Msps}} \approx 2.09$, respectively. As the hardware proposal in this paper used 49 rules, the speedup in Mflips can be calculated as the throughput in Msps $\times \frac{49}{35}$, that is, the speedup for the TS-FIMM-OS, TS-FIMM-P, Fuzzy-PI-OS and Fuzzy-PI-P are $1.82 \times 1.4 \approx 2.55$, $1.82 \times 1.4 \approx 3.72$, $1.53 \times 1.4 \approx 2.14$, and $2.09 \times 1.4 \approx 2.93$, respectively.

The work presented in [5] proposes a Takagi-Sugeno fuzzy controller on FPGA with two inputs, 6 rules and three outputs. The hardware achieved a throughput of about 1 Msps with 8 bits on the bus. With 8 bits, the speedup in Msps for the TS-FIMM-OS, TS-FIMM-P, Fuzzy-PI-OS and Fuzzy-PI-P are $\frac{11.94\,\text{Msps}}{1\,\text{Msps}} \approx 11.94$, $\frac{17.55\,\text{Msps}}{1\,\text{Msps}} \approx 17.55$, $\frac{10.77\,\text{Msps}}{1\,\text{Msps}} \approx 10.77$, and $\frac{15.13\,\text{Msps}}{1\,\text{Msps}} \approx 15.13$, respectively. The speedup in Mflips is about $\frac{40}{6} \approx 8.16 \times$ over the speedup in Msps.

In [16], a Mamdani fuzzy logic controller on FPGA was proposed. The hardware carries out a throughput of about 25 Mflips with two inputs, 49 rules, one output, and 16 bits. Using 16 bits, the speedup in Mflips for the TS-FIMM-OS, TS-FIMM-P, Fuzzy-PI-OS and Fuzzy-PI-P are $\frac{11.28\times\text{49 Mflips}}{25\,\text{Mflips}} \approx 22.11$, $\frac{16.98\times\text{49 Mflips}}{25\,\text{Mflips}} \approx 33.28$, $\frac{9.59\times\text{49 Mflips}}{25\,\text{Mflips}} \approx 18.79$, and $\frac{13.41\times\text{49 Mflips}}{25\,\text{Mflips}} \approx 26.28$, respectively. As the number of rules is 49, the speedup in Msps is equal to Mflips.

The work presented in [31] uses a Mamdani inference machine and the throughput in Mflips is about
48.23 Mflips. The hardware designed in [31] operated with 8 bits, four inputs, 9 rules and one output. The speedup in Mflips, with 8 bits, for the TS-FIMM-OS, TS-FIMM-P, Fuzzy-PI-OS and Fuzzy-PI-P are approximately 12.13, 17.83, 10.94, and 15.37, respectively. The speedup in Mps is about \( \frac{23}{25} \approx 0.92 \times \) over the speedup in Mflips.

The hardware used in [14] takes 6 clocks cycles over 10 MHz (in four states) to execute a M-IM with 16 bits. This is equivalent to a throughput of about \( \frac{10 \text{ MHz}}{6} \approx 1.67 \text{ Mps} \). The scheme proposed in [14] used two inputs, 25 rules and one output. The speedup in Mps for the TS-FIMM-OS, TS-FIMM-P, Fuzzy-PI-OS and Fuzzy-PI-P are approximately 6.75, 10.17, 5.74, and 8.03, respectively. The speedup in Mflips is about \( \frac{25}{29} \approx 1.96 \times \) over the speedup in Mps.

The works presented in [18, 20] shows a hardware can achieve about 1 Mps. The work presented in [18] uses two inputs, 25 rules, one output and 8 bits and the designer presented in [20] was projected with three inputs, 42 rules and one output. The speedup in Mps for the TS-FIMM-OS, TS-FIMM-P, Fuzzy-PI-OS and Fuzzy-PI-P are equal to previously calculated values used in [3]. The speedup in Mflips are about \( \frac{25}{29} \approx 1.96 \times \) and \( \frac{23}{29} \approx 1.16 \times \) over the speedup in Mps for works [18] and [20], respectively.

Finally, the hardware proposes in [7] achieved a throughput of about 1.56 Mps with three inputs, two outputs and 24 bits. The speedup in Mps for the TS-FIMM-OS, TS-FIMM-P, Fuzzy-PI-OS and Fuzzy-PI-P are approximately 7.23, 10.88, 6.15, and 8.59, respectively. The fuzzy system proposed in [7] does not use linguistic fuzzy rules and it cannot calculate the throughput in Mflips.

7.2. Hardware occupation comparison

Table 8 shows a comparison regarding the hardware occupation between the proposed hardware in this work and other literature works presented in Table 7. The second, third, fourth and fifth columns show the
Figure 22: Validation results from the proposed Takagi-Sugeno Fuzzy-PI hardware. Simulation trajectory for $\theta_1(t)$ with $\theta_1(n)$ using $N = \{12, 14, 16\}$ bits in the fractional part.

Figure 23: Validation results from the proposed Takagi-Sugeno Fuzzy-PI hardware. Simulation trajectory for $\theta_2(t)$ with $\theta_2(n)$ using $N = \{12, 14, 16\}$ bits in the fractional part.

type of FPGA, the number of logic cells (NLC), the number of multipliers (NMULT) and the number of bits in memory block RAMs (NBitsM), respectively and the last three columns show the ratio of the hardware occupation between the proposal presented here, $N_{\text{work hardware}}$, and literature works, $N_{\text{ref hardware}}$, presented in Table 7. The ratio of the hardware occupation can be expressed as

$$R_{\text{occupation}} = \begin{cases} \frac{N_{\text{work hardware}}}{N_{\text{ref hardware}}}, & \text{for } N_{\text{work hardware}} > 0 \text{ and } N_{\text{ref hardware}} > 0 \\ \frac{1}{N_{\text{ref hardware}}}, & \text{for } N_{\text{work hardware}} = 0 \text{ and } N_{\text{ref hardware}} > 0 \\ N_{\text{work hardware}}, & \text{for } N_{\text{work hardware}} > 0 \text{ and } N_{\text{ref hardware}} = 0 \\ 1, & \text{for } N_{\text{work hardware}} = 0 \text{ and } N_{\text{ref hardware}} = 0 \end{cases},$$

(28)

where $N_{\text{work hardware}}$ and $N_{\text{ref hardware}}$ can be replaced by NLC, NMULT or NBitsM.

The work presented in [11] used a Spartan 3A DSP FPGA from Xilinx and it has a hardware occupation of about 199 slices, 4 multipliers and 1 block RAM. As this FPGA uses about 2.25 LC per slice, it used about
Figure 24: Validation results from the proposed Takagi-Sugeno Fuzzy-PI hardware. Simulation trajectory for $\theta_3(t)$ with $\theta_3(n)$ using $N = \{12, 14, 16\}$ bits in the fractional part.

447 LC and it has 1512 K bits per block RAM. The scheme proposed in [5] used a Cyclone II EP2C35F672C6 FPGA from Intel and it has a hardware occupation of about 1622 logic cells and 8.19 Kbits of memory. The EP2C35 FPGA has 105 block RAM and 4,096 memory bits per block (4,608 bits per block including 512 parity bits).

In [10], the work assign a Arria V GX 5AGXFB3H4F40C5NES FPGA from Intel and it has a hardware occupation of about 3248 ALMs and 6.592 Kbits of memory. The Arria V GX 5AGX has two combinational logic cells per ALM. The hardware proposed in [31] employs a Spartan 6 FPGA from Xilinx and it has a hardware occupation of about 544 LUTs and 32 multipliers. As this FPGA uses about 1.6 LC per LUT, it used about 447 LC.

The hardware presented in the manuscript [14] utilizes a Spartan 6 FPGA from Xilinx and it has a hardware occupation of about 1802 slices and 5 multipliers. As this FPGA works with 6.34 LC per slice, it used about 11425 LC. The proposal described in [20] take advantage of Virtex 5 xc5vfx70t-3ff1136 FPGA from Xilinx and it has a hardware occupation of about 8195 LUTs and 53 multipliers. As this FPGA uses about 1.6 LC per LUT, it used about 13108 LC. 6-input LUT, they use the multiplier 1.6. The work presented in [7] used a Virtex 7 VX485T-2 FPGA from Xilinx and it has a hardware occupation of about 1948 slices and 38 multipliers. As this FPGA uses about 6.4 LC per slice, it used about 12468 LC.

7.3. Power consumption comparison

Table 9 shows the dynamic power saving regards the dynamic power. The dynamic power can be expressed as

$$P_d \propto N_g \times F_{\text{clk}} \times V_{DD}^2, \quad (29)$$

where $N_g$ is the number of elements (or gates), $F_{\text{clk}}$ is the maximum clock frequency and $V_{DD}$ is the supply voltage. The frequency dependence is more severe than equation 31 suggests, given that the frequency at which a CMOS circuit can operate is approximately proportional to the voltage [41]. Thus, the dynamic
power can be expressed as
\[ P_d \propto N_g \times F_{\text{clk}}^3. \]  
(30)

For all comparisons, the number of elements, \( N_g \), was calculated as
\[ N_g = N_{\text{LC}} + N_{\text{MULT}}. \]  
(31)

Based on Equation (30) the dynamic power saving can be expressed as
\[ S_d = \frac{N_{g}^{\text{ref}} \times (F_{\text{clk}}^{\text{ref}})^3}{N_{g}^{\text{work}} \times (F_{\text{clk}}^{\text{work}})^3}, \]  
(32)

where the \( N_{g}^{\text{ref}} \) and \( F_{\text{clk}}^{\text{ref}} \) are the number of elements (NLC + NMULT) and the maximum clock frequency of the literature works, respectively and the \( N_{g}^{\text{work}} \) and \( F_{\text{clk}}^{\text{work}} \) are the number of elements (NLC + NMULT) and the maximum clock frequency of this work, respectively. Differently from the literature, the hardware proposed here uses a fully parallelization layout, and it spends a one clock cycle per sample processing. In other words, the maximum clock frequency is equivalent to the throughput, \( F_{\text{clk}}^{\text{work}} \equiv R_s \).

7.4. Analysis of the comparison

Results presented in Tables 7 and 9 demonstrate that the fully parallelization strategy adopted here can achieve significant speedups and power consumption reductions. On the other hand, the fully parallelization scheme can increase the hardware consumption, see Table 8.

The mean value of speedup was about 10.89× in Msps and 30.89× in Mflips (see Table 7) and this results are very expressive to big data and MMD applications [1, 2, 3]. High-throughput fuzzy controllers are also important to speed control systems such as tactile internet applications [22, 21].

This manuscript proposal has LC resource higher utilization than the literature proposals (Table 8). The mean value regarding NLC utilization was about 6.89×; in other words, the fuzzy hardware scheme proposed here has used 6.89× more LC than the literature proposals. In the case of multipliers (NMULT), the mean value of the additional hardware was about 17.69×. Despite being large relative values, Tables 1, 2, 3 and 4 show that the fuzzy hardware proposals in this work expend no more than 7% of the FPGA resource. Another important aspect is the block RAM resource utilization (NBitsM). The fully parallel computing scheme proposed here, do not spend clock time to access information in block RAM and this can increase the throughput and decrease the power consumption (see references [11], [5] and [16] in Tables 7, 8 and 9).

The fully parallel designer allows to execute many operations per clock period, and this reduces the clock frequency operation and increases the throughput. Due to the non-linear relationship with clock frequency operation (see Equation 30), this strategy permits a considerable reduction of the dynamic power consumption (see Table 9). The results presented in Table 9 show that the power saving can achieve values from 4 until \( 10^6 \) times and these results are quite significant and enable the use of the proposed hardware here in several IoT applications.
8. Conclusions

This work aimed to develop a dedicated hardware for a fuzzy inference machine of the Takagi-Sugeno applied a Fuzzy-PI controller. The developed hardware used a fully parallel implementation with fixed-point and floating-point representation in distinct parts of the proposed scheme. All details of the implementation were presented as well as results for synthesis and bit-precision simulations. The synthesis results were performed for several bit size resolutions and showed that the proposed hardware is viable and can be used in applications with critical processing time requirements. Through the synthesis data, curves were generated to predict hardware consumption and throughput to untested bit values, in order to characterize the proposed hardware. In addition, comparison results concerning throughput, hardware occupation, and power saving with other literature proposals were presented.

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Conflicts of interest

The authors declare no conflict of interest.

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Table 7: Throughput comparison with other works.

| References | IM  | NI | NR | NO | NB | Msps | Mflips | Speedup |
|------------|-----|----|----|----|----|------|--------|---------|
| (2013)     | TS-IM | 2  | 35 | 1  | 10 | ≈ 6.63 | ≈ 232.05 | TS-FIMM-OS ≈ 1.82× | ≈ 2.55× |
|            |      |    |    |    |    |       |        | TS-FIMM-P ≈ 2.66× | ≈ 3.72× |
|            |      |    |    |    |    |       |        | Fuzzy-PI-OS ≈ 1.53× | ≈ 2.14× |
|            |      |    |    |    |    |       |        | Fuzzy-PI-P ≈ 2.09× | ≈ 2.93× |
| (2014)     | TS-IM | 2  | 6  | 3  | 8  | ≈ 1.00 | ≈ 6.00  | TS-FIMM-OS ≈ 11.94× | ≈ 97.43× |
|            |      |    |    |    |    |       |        | TS-FIMM-P ≈ 17.55× | ≈ 143.20× |
|            |      |    |    |    |    |       |        | Fuzzy-PI-OS ≈ 10.77× | ≈ 87.88× |
|            |      |    |    |    |    |       |        | Fuzzy-PI-P ≈ 15.13× | ≈ 123.46× |
| (2015)     | M-IM | 2  | 49 | 1  | 16 | ≈ 0.51 | ≈ 25.00 | TS-FIMM-OS ≈ 2.18× | ≈ 12.13× |
|            |      |    |    |    |    |       |        | TS-FIMM-P ≈ 3.20× | ≈ 17.83× |
|            |      |    |    |    |    |       |        | Fuzzy-PI-OS ≈ 1.97× | ≈ 10.94× |
|            |      |    |    |    |    |       |        | Fuzzy-PI-P ≈ 2.76× | ≈ 15.37× |
| (2016)     | M-IM | 4  | 9  | 1  | 8  | ≈ 5.36 | ≈ 48.23 | TS-FIMM-OS ≈ 6.75× | ≈ 13.23× |
|            |      |    |    |    |    |       |        | TS-FIMM-P ≈ 10.17× | ≈ 19.93× |
|            |      |    |    |    |    |       |        | Fuzzy-PI-OS ≈ 5.74× | ≈ 11.25× |
|            |      |    |    |    |    |       |        | Fuzzy-PI-P ≈ 8.03× | ≈ 15.74× |
| (2018)     | M-IM | 2  | 25 | 1  | 16 | ≈ 1.67 | ≈ 41.75 | TS-FIMM-OS ≈ 11.94× | ≈ 23.40× |
|            |      |    |    |    |    |       |        | TS-FIMM-P ≈ 17.55× | ≈ 34.40× |
|            |      |    |    |    |    |       |        | Fuzzy-PI-OS ≈ 10.77× | ≈ 21.11× |
|            |      |    |    |    |    |       |        | Fuzzy-PI-P ≈ 15.13× | ≈ 29.65× |
| (2019)     | M-IM | 2  | 25 | 1  | 8  | ≈ 1.00 | ≈ 25.00 | TS-FIMM-OS ≈ 11.94× | ≈ 13.85× |
|            |      |    |    |    |    |       |        | TS-FIMM-P ≈ 17.55× | ≈ 20.36× |
|            |      |    |    |    |    |       |        | Fuzzy-PI-OS ≈ 10.77× | ≈ 12.49× |
|            |      |    |    |    |    |       |        | Fuzzy-PI-P ≈ 15.13× | ≈ 17.55× |
| (2019)     | M-IM | 3  | 42 | 1  | –  | ≈ 1.00 | ≈ 42.00 | TS-FIMM-OS ≈ 7.23× | – |
|            |      |    |    |    |    |       |        | TS-FIMM-P ≈ 10.88× | – |
|            |      |    |    |    |    |       |        | Fuzzy-PI-OS ≈ 6.15× | – |
|            |      |    |    |    |    |       |        | Fuzzy-PI-P ≈ 8.59× | – |
Table 8: Hardware occupation comparison with other works.

| References | FPGA        | NLC | NMULT | NBitsM | This work | \( R_{\text{occupation}} \) |
|------------|-------------|-----|-------|--------|-----------|-----------------------------|
| [11] (2013)| Spartan 3A  | 447 | 4     | 1512 K | TS-FIMM-OS \( \approx 26.24 \times \) | \( \approx 12.25 \times \) \( \approx 10^{-6} \times \) |
|            |             |     |       |        | TS-FIMM-P \( \approx 22.61 \times \) | \( \approx 12.25 \times \) \( \approx 10^{-6} \times \) |
|            |             |     |       |        | Fuzzy-PI-OS \( \approx 26.24 \times \) | \( \approx 12.25 \times \) \( \approx 10^{-6} \times \) |
|            |             |     |       |        | Fuzzy-PI-P \( \approx 22.61 \times \) | \( \approx 12.25 \times \) \( \approx 10^{-6} \times \) |
| [5] (2014) | Cyclone II  | 1622| 0     | 8.19 K | TS-FIMM-OS \( \approx 6.51 \times \) | \( \approx 10^{-3} \times \) |
|            |             |     |       |        | TS-FIMM-P \( \approx 5.51 \times \) | \( \approx 10^{-3} \times \) |
|            |             |     |       |        | Fuzzy-PI-OS \( \approx 6.74 \times \) | \( \approx 10^{-3} \times \) |
|            |             |     |       |        | Fuzzy-PI-P \( \approx 5.75 \times \) | \( \approx 10^{-3} \times \) |
| [16] (2015)| Arria V GX  | 6496| 0     | 6.592 K| TS-FIMM-OS \( \approx 2.53 \times \) | \( \approx 10^{-3} \times \) |
|            |             |     |       |        | TS-FIMM-P \( \approx 2.21 \times \) | \( \approx 10^{-3} \times \) |
|            |             |     |       |        | Fuzzy-PI-OS \( \approx 2.61 \times \) | \( \approx 10^{-3} \times \) |
|            |             |     |       |        | Fuzzy-PI-P \( \approx 2.29 \times \) | \( \approx 10^{-3} \times \) |
| [31] (2016)| Spartan 6   | 871 | 32    | 0 K    | TS-FIMM-OS \( \approx 12.13 \times \) | \( \approx 1.53 \times \) 1x |
|            |             |     |       |        | TS-FIMM-P \( \approx 10.28 \times \) | \( \approx 1.53 \times \) 1x |
|            |             |     |       |        | Fuzzy-PI-OS \( \approx 12.56 \times \) | \( \approx 1.53 \times \) 1x |
|            |             |     |       |        | Fuzzy-PI-P \( \approx 10.71 \times \) | \( \approx 1.53 \times \) 1x |
| [14] (2018)| Spartan 6   | 11425| 5     | 0 K    | TS-FIMM-OS \( \approx 1.44 \times \) | \( \approx 0.98 \times \) 1x |
|            |             |     |       |        | TS-FIMM-P \( \approx 1.25 \times \) | \( \approx 0.98 \times \) 1x |
|            |             |     |       |        | Fuzzy-PI-OS \( \approx 1.48 \times \) | \( \approx 0.98 \times \) 1x |
|            |             |     |       |        | Fuzzy-PI-P \( \approx 1.30 \times \) | \( \approx 0.98 \times \) 1x |
| [20] (2019)| Virtex 5    | 13108| 53    | 0 K    | TS-FIMM-OS \( \approx 1.25 \times \) | \( \approx 0.93 \times \) 1x |
|            |             |     |       |        | TS-FIMM-P \( \approx 1.09 \times \) | \( \approx 0.93 \times \) 1x |
|            |             |     |       |        | Fuzzy-PI-OS \( \approx 1.29 \times \) | \( \approx 0.93 \times \) 1x |
|            |             |     |       |        | Fuzzy-PI-P \( \approx 1.13 \times \) | \( \approx 0.93 \times \) 1x |
| [7] (2019) | Virtex 7    | 12468| 38    | 0 K    | TS-FIMM-OS \( \approx 1.32 \times \) | \( \approx 1.29 \times \) 1x |
|            |             |     |       |        | TS-FIMM-P \( \approx 1.15 \times \) | \( \approx 1.29 \times \) 1x |
|            |             |     |       |        | Fuzzy-PI-OS \( \approx 1.36 \times \) | \( \approx 1.29 \times \) 1x |
|            |             |     |       |        | Fuzzy-PI-P \( \approx 1.19 \times \) | \( \approx 1.29 \times \) 1x |
Table 9: Dynamic power comparison with other works.

| References | FPGA     | $N_g^{ref}$ | $F_{clk}^{ref}$ (MHz) | This work | $N_g^{work}$ | $F_{clk}^{work}$ (MHz) | $S_d$  |
|------------|----------|-------------|-----------------------|-----------|--------------|------------------------|--------|
| [11] (2013)| Spartan 3A | 451         | 66.251                | TS-FIMM-OS | 11779        | $\approx 38.20 \times$ |        |
|            |          |             |                       | TS-FIMM-P  | 10157        | 6.63                   | $\approx 44.30 \times$ |
|            |          |             |                       | Fuzzy-PI-OS | 11779        | $\approx 38.20 \times$ |        |
|            |          |             |                       | Fuzzy-PI-P  | 10157        | $\approx 44.30 \times$ |        |
| [16] (2015)| Arria V GX | 6496        | 125                   | TS-FIMM-OS | 16453        |                       |        |
|            |          |             |                       | TS-FIMM-P  | 14377        | 0.51                   | $\approx 10^6 \times$ |
|            |          |             |                       | Fuzzy-PI-OS | 17001        |                       |        |
|            |          |             |                       | Fuzzy-PI-P  | 14926        |                       |        |
| [31] (2016)| Spartan 6 | 903         | 20                    | TS-FIMM-OS | 6598         | $\approx 4.42 \times$ |        |
|            |          |             |                       | TS-FIMM-P  | 5590         | 5.36                   | $\approx 5.22 \times$ |
|            |          |             |                       | Fuzzy-PI-OS | 6834         | $\approx 4.27 \times$ |        |
|            |          |             |                       | Fuzzy-PI-P  | 5826         | $\approx 5.01 \times$ |        |
| [14] (2018)| Spartan 6 | 11430       | 10                    | TS-FIMM-OS | 10252        | $\approx 149.16 \times$ |        |
|            |          |             |                       | TS-FIMM-P  | 8955         | 1.67                   | $\approx 170.70 \times$ |
|            |          |             |                       | Fuzzy-PI-OS | 10595        | $\approx 144.35 \times$ |        |
|            |          |             |                       | Fuzzy-PI-P  | 9298         | $\approx 164.42 \times$ |        |
| [7] (2019) | Virtex 7  | 12506       | 150                   | TS-FIMM-OS | 10252        |                       |        |
|            |          |             |                       | TS-FIMM-P  | 8955         | 1.56                   | $\approx 10^5 \times$ |
|            |          |             |                       | Fuzzy-PI-OS | 10595        |                       |        |
|            |          |             |                       | Fuzzy-PI-P  | 9298         |                       |        |