Ion Drift and Polarization in Thin SiO$_2$ and HfO$_2$ Layers Inserted in Silicon on Sapphire

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Abstract: To reduce the built-in positive charge value at the silicon-on-sapphire (SOS) phase border obtained by bonding and a hydrogen transfer, thermal silicon oxide (SiO$_2$) layers with a thickness of 50–310 nm and HfO$_2$ layers with a thickness of 20 nm were inserted between silicon and sapphire by plasma-enhanced atomic layer deposition (PEALD). After high-temperature annealing at 1100 °C, these layers led to a hysteresis in the drain current–gate voltage curves and a field-induced switching of threshold voltage in the SOS pseudo-MOSFET. For the inserted SiO$_2$ with a thickness of 310 nm, the transfer transistor characteristics measured in the temperature ranging from 25 to 300 °C demonstrated a triple increase in the hysteresis window with the increasing temperature. It was associated with the ion drift and the formation of electric dipoles at the silicon dioxide boundaries. A much slower increase in the window with temperature for the inserted HfO$_2$ layer was explained by the dominant ferroelectric polarization switching in the inserted HfO$_2$ layer. Thus, the experiments allowed for a separation of the effects of mobile ions and ferroelectric polarization on the observed transfer characteristics of hysteresis in structures of Si/HfO$_2$/sapphire and Si/SiO$_2$/sapphire.

Keywords: silicon-on-sapphire; hafnia; alumina; interlayers

1. Introduction

Silicon-on-sapphire (SOS) substrates with silicon device nanolayers are a promising material for the next generation (5G) of mobile phone “digital radio” chips, but the structural perfection of the thin silicon layers in them obtained by different methods is still worse than that of ultrathin layers of silicon-on-insulator (SOI) structures, such as HR-TR SOI [1–3]. There have been few reports of the SOS structure being produced using the hydrogen-induced thin Si layer transfer on sapphire by wafer bonding [3–7]. Usually, sapphire bonding is used for nitride semiconductors or niobate dielectric wafers with coefficients of thermal expansion (CTE) similar to that of sapphire. To overcome the CTE difference, the authors [3] used local fast laser heating to diminish the full stresses in the bonded wafers and obtained only partial Si layer transfer. Instead, in [4–7], we suggested silicon and sapphire wafer bonding at a moderate temperature, followed by hydrogen-induced thin Si layer transfer on the whole sapphire wafer at an elevated temperature. We developed a method similar to SmartCut® by implanting a hydrogen-induced Si layer transfer in vacuum at an elevated temperature [4–7]. The need for high-temperature annealing of implantation defects has led to the growth of a nanometer-thin silicon oxide interlayer, formed as a result of silicon oxidation by decomposed water molecules at the bonding interface and alumina reduction by silicon atoms. Under these conditions, a large built-in positive charge is formed at the SOS structure interface [5]. During measurements, this charge caused a large negative threshold voltage, $V_{t,e} = V_{th,e}$, for the current $I_{ds}$ in the pseudo-MOSFET channel. With a sapphire substrate thickness of 100 µm, the threshold gate voltage $V_{th,e}$ exceeds −10 kV. To reduce the effect of this charge on the pseudo-MOSFET characteristics, we proposed inserting SiO$_2$ layers with a thickness of 300 nm embedded...
between the device silicon layer and sapphire, and that provides $V_{t,e} > -0.5 \text{kV}$ [3–5]. Even SiO$_2$ layers with a thickness of 50 nm gave $V_{t,e} < -6.0 \text{kV}$, which was outside the available gate bias voltage range $V_g = \pm 6 \text{kV}$. However, a thick SiO$_2$ layer dramatically reduces the heat sink from the silicon device layer [8]. Moreover, there is a problem with choosing another inserted dielectric layer between the semiconductor and sapphire due to the large lattice and CTE mismatches [9]. Use of the PEALD Al$_2$O$_3$ interlayer is a standard approach for A3B5 semiconductor integration with sapphire by bonding. However, such an interlayer leads to the high interface state density of $\approx 6 \times 10^{11} \text{cm}^{-2}\text{eV}^{-1}$ in the case of substitution of the A3B5 layer by silicon [10]. Previously, we proposed and developed methods for inserting thin SiO$_2$ and HfO$_2$ layers in SOS structures using both silicon thermal oxidation and atomic layer deposition, followed by hydrogen transfer of silicon and annealing of SOS structures, to reduce the large positive charge in the transfer pseudo-MOSFET characteristics [5–7]. The inserted additional dielectric layers of silicon and metal dioxides (SiO$_2$ and HfO$_2$) at the silicon and sapphire boundary prevented internal oxidation and, accordingly, the formation of vacancies in sapphire during high-temperature furnace annealing (FA) of the SOS structure. However, the large hysteresis in the transfer pseudo-MOSFET characteristics was observed for both inserted layers after such FA.

The aim of this study was to establish the hysteresis mechanism using the temperature dependences of the transfer pseudo-MOSFET characteristics. The transport and capture of electrical charges, the recharging of interface states, ion drifts, and ferroelectric polarization in the SOS with inserted dielectrics—silicon and hafnium dioxides—were studied in detail.

The dominant mechanisms of the hysteresis in such structures are analyzed in this investigation with various inserted dielectric layers in the temperature range of 25–300 °C.

2. Materials and Methods

The silicon layer transfer from Si (100) wafers with a resistivity of 10–20 Ohm cm ($3–5 \times 10^{14} \text{cm}^{-3}$) by hydrogen implanted into sapphire was carried out according to the technology [4]. A hafnium dioxide layer with a thickness of 20 nm was grown on some of the wafers before bonding by PEALD using the FlexAl tool (Oxford Instruments Plasma Technology, Yatton, UK). The silicon wafers with a 2 nm native oxide were previously nitrided from a 400 W N$_2$ plasma remote ICP source at 500 °C for 5 min in the same tool without breaking the vacuum between the processes of nitridization and HfO$_2$ deposition. The organometallic Hf precursor TEMAH (Dalchem, Nizhny Novgorod, Russia) was used to deposit hafnium oxide; the precursor was heated to 70 °C and its vapors were delivered from the bubbler to the chamber by a 250 sccm Ar flow during the 1 s step of each cycle. The remote O$_2$ plasma source was used as an oxidizing precursor at a pressure of 15 mTorr and a power of 250 W for 3 s in a cycle. The sample temperature during the PEALD of HfO$_2$ was maintained at 250 °C.

Part of the sapphire substrates with the C-orientation were implanted with N$^+$ ions with an energy of 50 keV and fluence of $10^{16} \text{cm}^{-2}$ at room temperature. The Si layer transfer was carried out using the method described in Supplementary Materials (Figure S1) and earlier in [5–7]. Immediately before bonding, the surfaces of a pair of sapphire and silicon wafers were treated in O$^+$ or N$^+$ plasma. Finally, after the transfer at 450 °C for 1 h, silicon layers with thicknesses of $\approx 0.5 \ \mu\text{m}$ and $\approx 0.3 \ \mu\text{m}$ for thin and thick inserted dielectric layers, respectively, formed the SOS structures. All the obtained SOS wafers were subjected to an FA sequential heat treatment in a high-purity argon atmosphere at temperatures of 800, 1000, and 1100 °C.

The structural properties and composition of the layers were determined using X-TEM and X-HRTEM transmission electron microscopy, as well as the electron dispersion spectra (EDS) on FEI Titan 80–300 (FEI Company, Hillsboro, OR, USA) and JEM2000FX (JEOL, Ltd Tokyo, Japan) microscopes, respectively (Figure 1). The electric properties of the SOS structures were measured using a home-built high-voltage automatic unit ($V_g = \pm 6 \text{kV}$) from the drain–gate characteristics of pseudo-MOSFETs with tungsten needles at a distance of 100 µm and a tip radius of 20 µm and the clamping force of 60 g as source–drain Schottky
barrier contacts in the temperature range of 25–300 °C. Electron and hole mobilities were calculated on the basis of the drain–gate characteristics using the Y-function method (Y = I_{DS}/\sqrt{\beta m}) [11,12]:

$$\mu_{e,h} = (\beta_{e,h})^2/\left(4C_{OX}V_{ds}\right),$$

where $I_{DS}$ is the drain current, $\beta_m$ is the channel conductivity, $\beta_{e,h}$ are the Y-function branch slopes for electrons and holes, respectively, $f = 0.75$ is the geometric factor for two contact measurements, $C_{OX}$ is the gate dielectric capacity, and $V_{ds}$ is the drain voltage, where $V_{ds} = 1.5–20$ V.

![Figure 1](image.png)

**Figure 1.** EDS profiles of elements (a) and X-TEM micro-images with X-ray fluorescence maps (b) for the SOS cross-section with the 500 nm Si layer and the 20 nm PEALD inserted HfO$_2$ layer on the sapphire substrate after annealing at 1100 °C.

3. Results

The structural properties and composition of the layers in the SOS structures with the (0001) C-orientation of the 100 mm sapphire substrate were determined using X-TEM, X-HRTEM, and EDS measurements (Figure 1).

Silicon layers, after annealing at temperatures of 1000 °C and higher, are almost free of defects and do not differ in their crystal structure from original bulk silicon. Initially, the amorphous PEALD HfO$_2$ layers recrystallize into large-block textured layers, in contrast to the remaining amorphous structure of 50–300 nm SiO$_2$ layers [6,7]. Figure 1a shows the distributions of the main elements over the cross-section of such layers, including their distribution maps (Figure 1b). From the X-HRTEM and EDS data, it can be seen that, after high-temperature annealing, a silicon oxide interlayer was formed between the silicon layer and the PEALD inserted HfO$_2$ layer. Moreover, aluminum atom diffusion in the hafnium dioxide layer was also observed. Due to the overlap of the Si K and Hf Ma lines, as well as the partial overlap of Al Ka and Hf M and the small (2–3 nm) thickness of the interlayer between silicon and hafnium dioxide, it was not possible to determine the exact composition, although the most likely composition was Hf$_x$Si$_y$O$_z$, which has been experimentally observed many times [13,14].

Measurements of quasi-static transfer (drain–gate $I_{DS}$-$V_g$) characteristics of pseudo-MOSFETs were performed using repeated stepwise high gate voltages ($-6$ kV $< V_g < 6$ kV) changing from the rear contact on the sapphire substrate at a rate of 20–500 V/s relative to the gate voltage $V_{g,off}$, providing a depletion mode for the carriers in the silicon layer (Figures 2–4). The gate voltage rate was chosen automatically to satisfy a complete charge relaxation at each voltage step (Figure S2b) [15]. The maximum negative or positive voltages corresponded to the hole or electron conductivity in the silicon layer, respectively. Fixed
and mobile charge densities in the SOS structures with different inserted dielectric layers were extracted from the drain–gate $I_{ds}-V_{g}$ characteristics of pseudo-MOSFET transistors. SOS structures with a SiO$_2$ thickness of 310 nm without N$^+$ ion implantation (w/o NII) in the sapphire substrates were compared with N$^+$-implanted (w NII) SOS structures with a SiO$_2$ layer thickness of 50 nm only, with hole and electron branches in the $I_{ds}-V_{g}$ range of our high-voltage unit (Figure 2, Figure 3, Figure 4 and Figure S2a). The analysis of IV and CV curves allowed for the determination of embedded charge densities in the SOS with inserted dielectrics, which was carried out as follows. The linear extrapolation of the voltage-positive section of the Y-function for a sapphire substrate with a thickness of 70 µm and a HfO$_2$ inserted layer provides a threshold voltage $V_{T,e} = -1250 \pm 100$ V and an electron mobility $\mu_e = 230 \pm 30$ cm$^2$/V·s at $V_{ds} = 1.5$ V (shown in Figure 3 in [6]), but only in one $V_{g}$ direction from $-2.5$ to $+3.0$ kV for the correct mobility measurements, according to [11,12]. The measurements of the $I_{ds}-V_{g}$ hysteresis performed in this work at a higher $V_{ds} = 10$ V (in order to increase the $I_{ds}$ value) in the pseudo-MOSFET structure are presented in Figure 3a. The electron mobility dropped to $\mu_e = 100$ cm$^2$/V·s and the drain current saturated. The threshold voltage of holes, $V_{T,h} = -1540 \pm 100$ V, corresponded to the flat band voltage $V_{FB}$. The $V_{T,e}$-$V_{FB}$ difference should not change with a change in the $V_{ds}$ drain voltage and gate dielectric thickness $d$ if there are no short-channel effects due to a thick gate dielectric with $(\ell_{i} = 11.5$, which gives EOT = $\left(\frac{\varepsilon_{Si}}{\varepsilon_{sapphire}}\right)d = 0.34$ d. For sapphires with a thickness of 70 µm, EOT = 2.4 µm, which is much less than the distance between the source and the drain (i.e., 500 µm). Indeed, the experimentally determined threshold voltage value using the slope of the Y-function or the peak of the second derivative of the drain–gate characteristic $I_{ds}-V_{g}$ for samples with a thickness of less than 150 µm indicates the threshold voltage independence from the voltage $V_{ds}$ at the drain. Using the slope of the dependence $\log I_{ds}(V_{g}) = \log I_{g} + V_{g}/S$ at $V_{g} < V_{T,e}$, where the maximum subthreshold slope for electrons $S = 255$ V/dec, it is possible to estimate the state density $D_{it}$ from the data in Figure 3, Figure 4 and Figure S2 using the following formula [11,12]:

$$S = 2.3 \frac{kT}{q} \left[ 1 + \frac{C_{ht1}}{C_{ox}} + \frac{C_{Si}C_{it2}}{C_{ox}(C_{Si} + C_{it2})} \right]$$

where $C_{it1,2} = q \cdot D_{it1,2}$ and $q$ is the electron charge. There are capacitances of states on the lower and upper heterogeneous borders of the Si layer. The typical density of broken bonds at the silicon heterogeneous border with the native oxide is $D_{it2} = 2.0 \times 10^{13}$ cm$^{-2}$eV$^{-1}$, but most of them are passivated with hydrogen. Indeed, since $C_{ox}$ is small, $C_{ox} = C_{sa}$, and $qD_{it2} >> C_{Si} = \varepsilon_{o} \varepsilon_{Si} / t_{Si} \approx 20$ nF/cm$^2$ in the depletion mode, $D_{it1} = D_{it(e)}$ is equal to

$$D_{it(e,h)} = \frac{C_{ox}}{q} \left[ \frac{S_{eh}}{2.3kT} - \left( 1 + \frac{C_{Si}}{C_{ox}} \right) \right]$$

According to (1), we have $D_{it(e)} = 7.0 \times 10^{11}$ cm$^{-2}$eV$^{-1}$. The hole mobility $\mu_h$ in the inversion channel of the pseudo-MOSFET turned out to be significantly less than $\mu_e$. It was only $35 \pm 10$ cm$^2$/V·s at $V_{ds} = 1.5$ V and dropped to $\mu_h = 15$ cm$^2$/V·s due to the saturation at $V_{ds} = 3$ V. A large negative threshold voltage value for electron and hole conductivities, $V_{T,e}$ and $V_{T,h} = V_{FB} > 4$ kV, for the SOS structures with a thickness of $t_{sa} \geq 70$ µm without inserted dielectric layers corresponded to the capture of a positive charge at the border. The observed positive charge may have been a consequence of the vacancy formation in the SiO$_x$ interlayer due to the oxygen atom diffusion into the high-k dielectric [16,17]. The introduction of an intermediate HfO$_2$ layer in the SOS partially compensated for this charge and made it possible to roughly estimate the density of states and the effective charge at the heterogeneous interface with silicon using the difference in the threshold voltages of the channels in the enrichment and inversion mode [18]:

$$V_{Tn} - V_{Tp} \cong 2\Phi_F + \frac{q}{\varepsilon_0 \varepsilon_{sa}} (N_0t_{Si} + 2\Phi_F D_{it})$$
where $N_0$ is the donor concentration, $\Phi_F = E_F - E_i = 0.144$ eV is the Fermi level position in the silicon layer bulk with the donor concentration $N_D = 4 \times 10^{14}$ cm$^{-3}$, $C_{sa} = \varepsilon_{sa} / t_{sa}$ is the sapphire capacity, $C_{sa} \approx 113$ pF/cm$^2$ for 90 µm sapphire (dielectric permittivity $\varepsilon_{sa}$ for the field along the axis $C$ $\varepsilon_{11} = 11.5$), $D_R$ is the density of states at the interlayer, and $t_{sa}$ is the silicon layer thickness. Then, according to (2), $D_{it(h)} = 2.4 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$.

Figure 2. Drain–gate $I_{ds}$-$V_{g}$ transfer characteristics of SOS pseudo-MOSFET structures with a 310 nm thick inserted SiO$_2$ layer without N$^+$ ion implantation. The sapphire substrates were thinned by grinding to the thicknesses of 70 µm (a) and 150 µm (b).

Figure 3. Drain–gate $I_{ds}$-$V_{g}$ transfer characteristics of SOS pseudo-MOSFET structures with a 20 nm thick inserted HfO$_2$ layer without N$^+$ ion implantation. The sapphire substrates were thinned by grinding to the thicknesses of 70 µm (a) and 150 µm (b).

The partial depletion mode of the channel made it possible to roughly estimate the positive charge value in the dielectric, reduced to an inserted layer interface with a Si layer as $Q_{OX} = -V_{FB \cdot C_{OX}} / q = 1.2 \times 10^{12}$ cm$^{-2}$. Similar calculations carried out for the drain–gate characteristics of SOS structures with a built-in 50 nm silicon dioxide layer at the heterogeneous interface with sapphire, additionally modified by the nitrogen ion implantation, as well as with a 310 nm thick SiO$_2$ layer, provided a two times smaller value of $D_{it}$ (Table 1) [6]. A decrease in the positive charge in the presence of a HfO$_2$ layer or thermal oxides at the heterogeneous SOS structure interface made it possible to control this...
charge value, but the $D_{it}$ value turned out to be higher than for the 310 nm thermal SiO$_2$ layer (Table 1).

![Figure 4](image-url)  
*Figure 4. Temperature dependences of pseudo-MOSFET drain–gate $I_{ds}$-$V_{gs}$ transfer characteristics for SOS structures with a 310 nm thick inserted SiO$_2$ layer (a) and 20 nm thick inserted HfO$_2$ layer (b) without NII after the annealing.*

| No. and IL Description | $\mu_e/\mu_h$, cm$^2$/Vs | $Q_{ox}$, cm$^{-2}$ | $D_{it(e)}/D_{it(h)}$, cm$^{-2}$eV$^{-1}$ |
|------------------------|--------------------------|-------------------|----------------------------------|
| #1 Thin SiO$_2$ 50 nm N⁺, 50 keV | 105/37 | $2.1\times10^{11}$ | 1.3$\times10^{12}$/3.8$\times10^{11}$ |
| #2 Thick SiO$_2$ 310 nm | 250/50 | $4.7\times10^{11}$ | 6.3$\times10^{11}$/4.1$\times10^{11}$ |
| #3 Thin HfO$_2$ 20 nm | 230/35 | $1.2\times10^{12}$ | 7.0$\times10^{11}$/2.4$\times10^{12}$ |

Table 1. The values of mobility $\mu_e$ and $\mu_h$, built-in charge $Q_{ox}$, and density of states for electrons $D_{it(e)}$ and holes $D_{it(h)}$ at the interface with the transferred Si layer for three types of SOS structures measured at $V_{ds} = 1.5$ V for the correct mobility measurements according to [11,12,18].

The absence of a depletion mode in the gate voltage operating range in SOS pseudo-MOSFET structures without inserted layers of silicon dioxide or hafnium dioxide is presumably associated with a large positive charge at the silicon–sapphire interface, as well as with an insufficient electric field near the interface due to the thick sapphire substrate. To confirm this assumption, the SOS structures were thinned from the side of the sapphire substrate by grinding and polishing to a thickness value of less than 100 $\mu$m without introducing additional defects [5,6].

The measurement of transport properties of carriers using pseudo-MOSFET transistors with a back gate on the substrate side showed normal characteristics of pseudo-MOSFET transistors not only for structures with SiO$_2$ layers but also for structures with a 20 nm hafnia layer at the interface with a thin sapphire substrate (Figures 2–4). Thinning the substrate allowed pseudo-MOSFET transistors with the SiO$_2$ layer to operate in depletion and inversion modes at a bias $V_{gs}$ on the substrate of up to ±4 kV.

At the same time, a 20 nm thick hafnia layer provided the appearance of the space charge region of the pseudo-MOSFET, as well as the depletion and inversion modes during the pretreatment of sapphire in nitrogen plasma or nitrogen ion implantation (NII) to compensate for the positive charge, even for 500 $\mu$m of the sapphire substrate. In addition, the built-in positive charge at the silicon interface decreased so much that it allowed for the measurements of both electron and hole drain–gate characteristics in the pseudo-MOSFET conducting channel, even with the relatively large sapphire substrate thickness of 150 nm without NII (Figure 3b). Nevertheless, the residual positive charge did not allow for the
sapphire thickness of 150 μm to completely repolarize hafnium dioxide with an external field of \(\approx 1 \times 10^5\) V/cm in the hole conduction mode, unlike the field of \(\approx 4 \times 10^5\) V/cm for the 70 μm substrate thickness (Figure 3a). The measurement results for the drain–gate characteristics of \(I_{ds}-V_g\) pseudo-MOSFETS on sapphire with a built-in SiO₂ and HfO₂ dielectric, depending on their temperature, are shown in Figure 4. One interesting feature is the double \(I_{on}/I_{off}\) ratio increase with temperature increase for the 310 nm thick inserted SiO₂ layer, while this ratio decreased for the inserted hafnia layer.

Another relevant factor is the triple increase in the hysteresis window observed for the inserted SiO₂ layer with rising temperature (Figure 4a), while it was below one-third of the increase for the inserted hafnia layer (Figure 4b). The latter had a thermally stable hysteresis, \(\Delta V_g \approx 600\) V, at the SOS pseudo-MOSFET drain–gate characteristics, and this suggests the formation of a ferroelectric phase in the inserted hafnia layer after annealing at 1100 °C, whereas when the charge is captured on traps, the hysteresis bypass loop direction should be the opposite. The HfO₂ ferroelectric polarization shifted the threshold voltage \(\Delta V_{FT} \approx 600\) V at \(\pm 4\) kV, which corresponded to a change in the potential \(\Delta V_{HfO_2} = \pm 100\) mV and the maximum field of \(5 \times 10^4\) V/cm in a 20 nm thick HfO₂ layer. This shift corresponded to a polarization charge of \(P = \pm (80–100)\) nC/cm² instead of the theoretical value of \(P = 56\) μC/cm² in a field greater than \(2 \times 10^6\) V/cm, when the orthorhombic phase is most stable [19]. In the measured structure, only part of the hafnia film had ferroelectric properties. The reason is that a further increase in the substrate gate potential was prevented by a surface breakdown. Nevertheless, the polarization field and charge in the hafnium oxide layer can be increased by reducing the sapphire substrate thickness.

Finally, for the various inserted layers, the measurements of transfer (drain–gate \(I_{ds}-V_g\)) characteristics and calculations of the mobility of electrons and holes were carried out, wherein the spread of values were 35–50 and 105–250 cm²/(Vs), respectively. The built-in charge and interface state density values were (2.1–13) \(\times 10^{11}\) cm⁻² and (3.8–24) \(\times 10^{11}\) cm⁻²eV⁻¹, respectively. The polarization charge \(P\) was observed to be as low as \(P = \pm (80–100)\) nC/cm² at the electric field of \(5 \times 10^4\) V/cm in a 20 nm thick inserted HfO₂ layer.

4. Discussion

The PEALD HfO₂ layer on silicon usually leads to an increase in the positive charge in the MOSFET dielectric [16], in contrast to the observed decrease in its value in our experiments with high-temperature annealing of SOS. This can be due to different built-in charge formation mechanisms. For example, the negative threshold voltage shift of \(\Delta V_{FB}\) below 0 V due to the predominance of a positive charge at the silicon/sapphire interface for the SOS structures without preliminary inserted dielectrics may be due to the diffusion of O²⁻ anions from sapphire into silicon dioxide during high-temperature treatments of T > 800 °C [17]. However, the estimation of the diffusion length \(L\) based on the volume diffusion coefficient \(D(T) = 3.27 \times 10^{-4} \exp(-7.21eV/kT)\) m²/s for the maximum thermal treatment budget (1100 °C during 2 h) provides a too small value of \(L = 0.01\) nm [13]. Another reason for the accelerated diffusion of point defects in this layer may be a chemically reactive fusion border enriched with both vacancies, hydrogen and oxygen atoms. Tangential compression stresses and sapphire tensile stresses normal to the surface can make an additional contribution to the acceleration of diffusion during annealing due to the lower silicon value of CTE. The oxygen atoms exit in planes parallel to the surface, which reduces the misalignment of the lattices during annealing. The probable cause of the large positive charge formation at the silicon/sapphire interface (without inserted dielectrics) is aluminosilicates formed at the SiO₂/Al₂O₃ interface [14]. The inserted HfO₂ layer reduces the possibility of their formation, which should lead to a decrease in this charge.

It is known that the difference in the chemical bonding polarities of two dielectrics leads to the formation of dipoles at their interface, creating a potential jump. Part of the
charges can recombine during dielectric bonding by tunneling through a potential barrier, which leads to a partial loss of the dipole charges [20]. On the other hand, when connecting two flat surfaces of dielectrics (a typical situation), for example, anions are displaced from aluminum oxide, which has a higher surface density of oxygen atoms, into hafnium dioxide, with a 1.37 times lower density [19], leading to the formation of oriented dipoles with a negative charge towards the interface with silicon and the positive shift in the threshold voltage $\Delta V_{FB}$ observed in the experiment [21,22]. Experimental results show a negative shift of $\Delta V_{FB} \approx -0.4 \ V$ for lanthanum oxides with a thickness of 1 nm or more, as well as multiple smaller positive shifts for hafnia and alumina [23].

In our samples, the positive charge at the insulator interface with silicon can be estimated as $Q_{eff} = P_P - P_n = 1.4 \times 10^{11} \ cm^{-2}$. The repolarization of the inserted HfO$_2$ dielectric at room temperature shifted the p- and n-thresholds $\Delta V_T \approx 600$ and $-790 \ V$, which corresponded to the electric field $4 \times 10^4 \ V/cm$ and polarization charge density $(6-7) \times 10^{11} \ cm^{-2}$ at surface potential change $\Delta \phi_S = 80 \ mV$. The ion charge in the inserted SiO$_2$ layer demonstrated a quasi-ferroelectric hysteresis, since this hysteresis increases with temperature, and that contradicts the behavior of hysteresis according to the Curie–Weiss law (Figure 4a). The hysteresis memory window (MW) growth at $I_{ds}$ $= 20 \ \mu A$ for holes from MW$_h = 410 \ V$ to 1180 $V$ and for electrons from MW$_e = 550 \ V$ to 1280 $V$ with an increase in temperature from 25 to 250 $^\circ C$ was due to the greater diffusion mobility of H$^+$ and OH$^-$ ions in SiO$_2$ [23]. For the inserted HfO$_2$ dielectric, the memory window temperature increase was much less pronounced. However, the minimum current $I_{ds,min}$ in the depletion mode of the pseudo-MOSFET transistor grew faster than for the SOS pseudo-MOSFET structure with silicon dioxide (Figure 4b). Therefore, the hysteresis windows were determined for the current difference $\Delta I_{ds} = I_{ds} - I_{ds,min} = 50 \ \mu A$ with a HfO$_2$ layer in the same temperature range. They varied for holes from MW$_h = 600 \ V$ to 680 $V$ and for electrons from MW$_e = 790 \ V$ to 1000 $V$ with a temperature increase from 25 to 250 $^\circ C$. According to the published data [24], the ion concentration $N_{ion}$ of H$^+$ and OH$^-$ in the hafnia-based dielectric can reach $(1-200) \times 10^{18} \ cm^{-3}$. Accordingly, the ion current contribution to the charge hysteresis can be estimated as the product of their concentration by the distance $l$ that hydroxyl ions (equivalent to oxygen vacancy) will overcome during the time of pulse signal $t$ with a drift velocity $v$ equal to [25]:

$$v = a f \ exp \left( \frac{-E_a}{kT} \right) \ \sinh \left( \frac{q a E}{kT} \right) \ and \ l = vt \quad (3)$$

Here, $q$ is the charge, which, for a proton and hydroxyl, is equal to $\pm 1$ elementary charge; $a = 0.25 \ nm$ is the jump distance; $f = 10^{15} \ Hz$ is the oxygen atom oscillation frequency; $E_a = 0.45 \ eV$ is the hydroxyl (oxygen vacancies) activation energy of movement; $k$ is the Boltzmann constant; $T$ is the temperature; $E = 1 \times 10^6 \ V/cm$ is the electric field strength; and $t = 200 \ s$ is the time until the pulse is applied at the next point of quasi-static drain–gate $I_{ds}$-$V_g$ measurements. For these parameters, the drift length $l$ is equal to 0.48 nm at RT and 28 $\mu m$ at 300 $^\circ C$. These estimates show that, in a SOS pseudo-MOSFET with a 20 nm HfO$_2$ inserted dielectric, the hysteresis at room temperature is associated with ferroelectric repolarization, and a temperature increase of up to 300 $^\circ C$ can collect all ions at their boundaries. The full ion charge is $Q_{ion} = N_{ion} \ d_{HfO2} = 2 \times 10^{20} \ 2 \times 10^{-6} = 4 \times 10^{14} \ cm^{-2}$. Since the polarization measured by the hysteresis window was three orders of magnitude lower, the ion density in the inserted HfO$_2$ dielectric was also reduced by more than these three orders and did not exceed $N_{ion} \approx 1 \times 10^{17} \ cm^{-3}$.

5. Conclusions

To reduce the built-in positive charge value at the silicon-on-sapphire (SOS) phase border obtained by bonding and a hydrogen transfer, thermal silicon oxide (SiO$_2$) layers with a thickness of 50–310 nm and HfO$_2$ layers with a thickness of 20 nm were inserted between silicon and sapphire by plasma-enhanced atomic layer deposition (PEALD). After high-temperature annealing at 1100 $^\circ C$, these layers led to a hysteresis in the drain
current–gate voltage curves and a field-induced switching of threshold voltage in the SOS pseudo-MOSFET. The transfer transistor characteristics measured in the temperature ranging from 25 to 300 °C demonstrated a triple increase in the hysteresis window with increasing temperature for inserted SiO$_2$ with a thickness of 310 nm. It was associated with the ion drift and the formation of electric dipoles at the silicon dioxide boundaries. A much slower increase in the window with temperature for the inserted HfO$_2$ layer was explained by the dominant ferroelectric polarization switching in the inserted HfO$_2$ layer. The experiments allowed for a separation of the effects of mobile ions and ferroelectric polarization on the observed transfer characteristics of hysteresis in Si/HfO$_2$/sapphire and Si/SiO$_2$/sapphire structures.

The SOS pseudo-MOSFET with the inserted HfO$_2$ layer on <150 μm thick sapphire demonstrated normal drain–gate characteristics with charge carrier mobility, as in bulk silicon, as well as a smaller (compared to the SOS structure without an inserted dielectric layer) positive charge value of up to $1 \times 10^{12}$ cm$^{-2}$ and stable ferroelectric-type hysteresis with $\Delta V_g > 600$ V. Such characteristics are promising for developing elements of built-in memory and expanding the functionality of integrated SOS circuits for radiophotonics, microwave, and optoelectronics.

The physical reason for the low-field switching in the SOS pseudo-MOSFET with the inserted hafnium dioxide layer is the compressive biaxial stress due to the large CTE difference between silicon and sapphire after heat treatment. The density of ions and charge traps in the HfO$_2$ and SiO$_2$ layers was found to be small (<$5 \times 10^{11}$ cm$^{-2}$) and did not mask the ferroelectric switching in HfO$_2$, even in the case of nitrogen-implanted sapphire. Our continued experiments with various thicknesses of inserted hafnia layers in silicon on sapphire yield a potential jump value due to the dipoles at the HfO$_2$/SiO$_2$ interface.

Supplementary Materials: The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/nano12193394/s1, Figure S1. SOS structure fabrication process for the wafer #3 used in the investigation; Figure S2. (a) Transfer characteristics (drain current–gate voltage) for mutual $V_g$ sweep between $V_g = \pm 3500 \pm 5000$ V of SOS pseudo-MOSFET with 50 nm SiO$_2$ BOX layer and nitrogen implanted sapphire substrate; (b) the drain current $I_{ds}$ evolution for sweeping bias voltage $V_g$ during one unit sweep. Reference [26] are cited in the Supplementary Materials.

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