Near-threshold SIDO DC-DC converter with a high-precision ZCD for phase change memory chip

Jie Miao\textsuperscript{1,2}, Houpeng Chen\textsuperscript{1,2a}, Yu Lei\textsuperscript{1,2b}, Yi Lv\textsuperscript{1,2}, Weili Liu\textsuperscript{1,2}, and Zhitang Song\textsuperscript{1,2}

Abstract This letter proposes a near-threshold single-inductor double-output (SIDO) DC-DC converter with a high-precision zero current detector (ZCD) circuit which supply voltage to phase change memory (PCRAM) chip in wireless sensor network. It has a specific startup procedure to provide wide input voltage range. And the ZCD circuit is designed according to volt-second balance theory and minimizes the duration of reverse inductor current to about 1 nS. The DC-DC converter is implemented in 110 nm standard CMOS process and the maximum power efficiency is 89.47\% with no cross regulation.

Keywords: DC-DC converter, SIDO, zero current detector

1. Introduction

With the development of CMOS technology, CMOS device size shrinks and memory devices have reached their size limitation, such as DRAM, SRAM and Flash [1, 2, 3]. Therefore, scientists from academia and industry devote their energies to research new memory material in recent years, such as STT-MRAM [4, 5], FeRAM [6, 7], RRAM [8, 9] and PCRAM [10]. Among the new memory material, phase change random access memory (PCRAM) is regarded as the most probable next-generation nonvolatile memory for its dramatically low latency and exponentially great endurance [11]. Recently, Intel announced that they had cooperated with Micron on PCRAM technology and would roll out the second generation of 3D XPiont in the first half of 2019 [12].

Flash memory can only work in block manipulation. Comparing with traditional nonvolatile memory, PCRAM can be changed resistance to store data by different current, so it can be operated bit-by-bit and reduce power consumption in wireless sensor network [13, 14]. In PCRAM chips, write operation needs high power voltage to ensure success, and read and logic operation use low power voltage to reduce power consumption. Therefore, two various power voltages often supplied to PCRAM chips [15, 16].

Because DC-DC converter can supply two respective high voltages with a single inductor and reduce the area of power management unit [17, 18, 19, 20], this letter presents a near-threshold single-inductor double-output (SIDO) DC-DC converter with a high-precision zero current detector (ZCD) for PCRAM device in wireless sensor network.

This letter is organized as follow. In Section 1, a DC-DC converter for PCRAM is introduced. In Section 2, the startup procedure for low input voltage and the topology of the SIDO DC-DC converter are illustrated. After that, volt-second balance theory used in ZCD circuit is explained and its implementation is given in Section 3. At last, the simulation results follow in Section 4 and Section 5 concludes the letter.

2. Architecture of near-threshold SIDO DC-DC converter

2.1 Startup procedure of the converter

The system is driven by solar cell or dry battery at the voltage from 0.7 V to 1.5 V [21, 22, 23], and the threshold voltage of CMOS is about 0.7 V, so we should design a specific startup procedure to drive DC-DC converter. Fig. 1 shows all stages of the startup procedure of the near-threshold DC-DC converter along with driving voltages. V\textsubscript{OA} and V\textsubscript{OB} are two output voltages of the DC-DC converter, and V\textsubscript{OA} is the higher one. Initially, the circuit judges the input voltage at Stage1. If V\textsubscript{IN} is more than 1.1 V which is high enough to drive the power tubes, the input voltage will connect to the V\textsubscript{OA} though power tube by linear start-up module until V\textsubscript{OA} is close to V\textsubscript{IN}. Elsewise, the 2x charge pump module will work. After a fixed delay time about 0.7 mS, the output voltage of the charge pump (V\textsubscript{CP}) is high enough to drive power tube in DC-DC module and then the system runs into next stage. In Stage2, the maximum voltage of V\textsubscript{IN}, V\textsubscript{CP} and V\textsubscript{OA} drives open-loop DC-DC module by a fixed duty cycle. After V\textsubscript{OA} is charged to a special voltage about 1.75 V which is high enough to empower the control circuit works properly, the circuit turns into final stage. In stage 3, the circuit works into close-loop DC-DC stage which is illustrated in detail in the follow section.

2.2 Topology of SIDO DC-DC converter

The DC-DC converter supply two output voltage V\textsubscript{OA} and V\textsubscript{OB} by single inductor, so that a part of modules can be
In phase voltage magnetizes inductor and the inductor current raises, while the inductor charges output voltage $V_{OA}$. Until MN switches on and MPa, MPb keep off, module N shared to two paths, such as power tube MN and its driver module N, Dr, oscillator, current sensor and bandgap module, as shown in Fig. 2(a). This converter works in current controlled pulse width modulation (PWM) mode to have well load and line regulation.

The inductor current and control signals of SIDO DC-DC converter is shown in Fig. 2(b). Oscillator generates a square wave OSC whose duty time is 50% for the sake of charging two paths respectively by single inductor. In phase $\Phi_{on}$, signal OSC drops down, and then power tube MN switches on and MPa, MPb keep off, while input voltage magnetizes inductor and the inductor current raises. In phase $\Phi_{off}$, MPa switches on and MN switches off, while the inductor charges output voltage $V_{OA}$. Until inductor current is zero, signal PWM Pa which is generated by zero current detector (ZCD) circuit turns MPa off. The details of the ZCD technique are illustrated in Section 3. Then all of the power tubes turn off. When the signal OSC raises up, the current will charge output voltage $V_{OB}$ in the second half cycle T2 in the same way. The SIDO DC-DC converter always works in discontinuous conduction mode (DCM) and the two output voltages are charged in their respective half cycle, so that the system would avoid cross regulation.

![Fig. 1. The startup procedure of the near-threshold DC-DC converter.](image)

Fig. 1. The startup procedure of the near-threshold DC-DC converter.

3. High-precision ZCD technique for power consumption

When inductor current reduces to zero in phase $\Phi_{off}$, ZCD will turn off MP and the DC-DC converter turns into phase $\Phi_{wait}$, as shown in Fig. 3(a). The traditional way to judge whether the inductor current is zero is to compare the voltage of node SW ($V_{SW}$) and output voltage ($V_O$). Therefore, the performance of traditional ZCD relies on the speed and precision of its comparator [24, 25]. However, when the comparator detects that the output voltage is higher than $V_{SW}$, the reverse inductor current which flows from MP to inductor has happened, as illustrated in Fig. 3(b). With the reduction of inductance and on-resistance of PMOS power tube, DC-DC converter works in high energy consumption by the way of comparing $V_{SW}$ and $V_O$. In this letter, a high-precision ZCD is applied in SIDO DC-DC converter according to volt-second balance theory as follow.

![Fig. 2. Topology architecture and signals of SIDO DC-DC converter](image)

Fig. 2. Topology architecture and signals of SIDO DC-DC converter

\[ I_L = \frac{1}{L} \int_{t_{off}}^{t_{on} + t_{off}} [V_{IN} - V_{SW}(t)] dt = 0 \] (1)

According to equation (1), we can get the relationship between voltage $V_{IN}$, $V_{SW}$ and time $t_{on}$, $t_{off}$, which is

\[ 1 \int_{t_{off}}^{t_{on}} [V_{IN} - V_{SW}(t)] dt = 1 \int_{t_{on}}^{t_{on} + t_{off}} [V_{SW}(t) - V_{IN}] dt \] (2)

Where $t_{on}$ is the time of magnetizing the inductor and $t_{off}$ is the time of empowering output voltage.

The time integral of voltages ($V_{IN} - V_{SW}$) of two phases can be converted to voltage signals by the particular circuit which is illustrated in section 3.2. The equations are

\[ V_1 = k_1 \int_{t_{off}}^{t_{on}} [V_{IN} - V_{SW}(t)] dt \]
\[ V_2 = k_2 \int_{t_{on}}^{t_{on} + t_{off}} [V_{SW}(t) - V_{IN}] dt \] (3)

Where $k_1$ and $k_2$ are same coefficient.

According to equations (2) and (3), we find that $t_{on}$ and $t_{off}$ have the same value when $V_2$ is equation to $V_1$. Therefore, comparing $V_3$ and $V_1$ for equality, we can judge whether the inductor current is zero and we should turn off MP.

3.2 Circuit implementation of zero current detector

There are three various voltage detection circuits that consist of six resistances, three 2-1 multiplexers and three voltage-current (V-C) converters in Fig. 4(a). R1~R6 have same value to divide the sensing voltages. Because node SW whose voltage ($V_{SW}$) jumps from output voltage to zero is a transition node, multiplexers are used to smooth the sensing voltages when the DC-DC converter works in other phases. Voltage-current converter which is composed
by four p-MOS M1∼4, a resistor and an amplifier transforms voltage signal to current signal, as shown in Fig. 4(b). M1∼M4 are cascode structure in order to restrain the channel length modulation effect. And then we get the current $I_1$, $I_2$ and $I_3$

$$I_1 = \frac{V_{IN} + V_{SW(on)}}{2R}, \quad I_2 = \frac{V_{IN}}{2R}, \quad I_3 = \frac{V_{SW(off)}}{2R}$$ \hspace{1cm} (4)

A zero current detector circuit shown in Fig. 5(a) is proposed according to volt-second balance theory mentioned above. Signal PWM.N is input voltage and Signal PWM.P is output voltage of ZCD circuit to control power tube MPa or MPb, as shown in Fig. 5(b). At the beginning of each cycle, when power tube MN turns on and inductor L is magnetized, M5 turns on controlled by PWM.N and current ( ) starts charging capacitor C1. At the meantime, DFF is reset by PWM.N. When the DC-DC converter turns into phase $\Phi_{off}$, M5 turns off by PWM.N and M6 turns on by PWM.N. The voltage on C1($V_{C1}$) is maintained and current ( ) starts charging capacitor C2, so the voltage on C1 and C2 can be expressed as

$$V_{C1} = \frac{1}{C} \int_{0}^{t} \frac{V_{in} - V_{SW(t)}}{2R} dt, \quad V_{C2} = \frac{1}{C} \int_{t_{on}}^{t} \frac{V_{SW(t)} - V_{in}}{2R} dt$$ \hspace{1cm} (5)

Comparing equation (3) and (5), we find that $V_{C1}$ and $V_{C2}$ are similar to $V_1$ and $V_2$. When the comparator detects that $V_{C2}$ is higher than $V_{C1}$, DFF is triggered by comparator and signal P.SHUT turns to “1”. Therefore, power tube MP turns off by signal PWM.P and the DC-DC converter turns into phase $\Phi_{wait}$. M6 turns off and M7, M8 turn on, so the capacitors C1 and C2 are both discharged to ground and wait to work until next cycle.

$\quad$

4. Simulation results

The proposed near-threshold SIDO DC-DC converter with high precision ZCD is designed and simulated with 110 nm standard CMOS process. The total silicon chip of the DC-DC converter occupies an area of 2.2 mm$^2$ (including pads), as shown in Fig. 6. The SIDO DC-DC converter provides 1.8 V ($V_{OA}$) and 2.5 V ($V_{OB}$) output voltage from input voltage of 0.7~1.5 V.

![Fig. 4. Voltage detection circuits](image)

![Fig. 5. Zero current detector architecture and timing diagram](image)

![Fig. 6. Layout view of the DC-DC converter](image)

![Fig. 7. Simulation result of the startup procedure of the converter](image)

Fig. 7 illustrates the simulated voltages of the startup procedure of the converter at different input voltage. And the setting time of the proposed converter is less than 5 ms. $V_{PWR}$ is the voltage which drives the DC-DC converter internally. Fig. 8 shows the simulation waveforms of inductor current $I_L$, voltages on capacitors and control signals P.SHUTa, P.SHUTb. As a result, the two ZCD circuits can minimizes the duration of reverse inductor current to about 1 ns. The simulated line regulations of the output terminals $V_{OA}$ and $V_{OB}$ are 1.14 and 0.79 mV/V, respectively, as shown in Fig. 9.

A maximum power efficiency of 89.47% can be achieved when the input voltage is 1.5 V and load current in each channel is 20 mA. Because the charge pump only works in low input voltage, power efficiency at 1.5 V input voltage is high than 0.7 V, as shown in Fig. 10. The performance of the SIDO DC-DC converter compared with the reported DC-DC converters are summarized in Table I. Comparing with other designs, the proposed DC-DC converter has wide input voltage range, small inductor, small line regulation and no cross regulation. Those advantages are suitable for PCRAM chip in wireless sensor network.
5. Conclusion

This letter presents a high-precision ZCD with volt-second balance theory, which is applied to near-threshold SIDO DC-DC converter for PCRAM chip in wireless sensor network. The converter has a wide input voltage range from 0.7 V to 1.5 V and the setting time of the converter is less than 5 mS. The presented ZCD circuits can minimize the duration of reverse inductor current to about 1 nS. The maximum efficiency of the DC-DC converter is 89.47%.

Lastly, the proposed DC-DC converter has a wide input voltage range, small inductor, small line regulation and no cross regulation.

Acknowledgments

Supported by the National Key Research and Development Program of China (2017YFA0206101, 2017YFB0701703, 2017YFA0206104, 2018YFB0407500, SQ2017YFGX020134), Strategic Priority Research Program of the Chinese Academy of Sciences (XDPB12), National Natural Science Foundation of China (61874129, 61874178, 61504157, 61622408), Science and Technology Council of Shanghai (17DZ2291300, 18DZ2272800).

References

[1] S. Yu and P.-Y. Chen: “Emerging memory technologies: Recent trends and prospects,” IEEE Solid State Circuits Mag. 8 (2016) 43 (DOI: 10.1109/MSSC.2016.2546199).

[2] W. Zhang, et al.: “Fast persistent heap based on non-volatile memory,” IEICE Trans. Inf. & Syst. E100.D (2017) 1035 (DOI: 10.1587/transinf.2016EDP7429).

[3] Y. Han and E. Lee: “CRAST: Crash-resilient data management for a key-value store in persistent memory,” IEICE Electron. Express 15 (2018) 20180919 (DOI: 10.1587/transele.2018CDP0007).

[4] K. Lee, et al.: “Unified embedded non-volatile memory for emerging mobile markets,” IEEE/ACM ISLPED (2014) 131 (DOI: 10.1145/2627369.2631641).

[5] M. Hayashikoshi, et al.: “A cost-effective 1T-4MTJ embedded MRAM architecture with voltage offset self-reference sensing scheme for IoT applications,” IEICE Trans. Electron. E102.C (2019) 287 (DOI: 10.1587/tse.2018CDP0007).

[6] S. Kawashima, et al.: “An 8-Mbit 0.18-μm CMOS 1T1C FeRAM in planar technology,” IEICE Trans. Electron. E98.C (2015) 1047 (DOI: 10.1587/transele.E98.C.1047).

[7] M. G. Kim, et al.: “Nonvolatile organic field effect transistors
fabricated on Al foil substrates,” IEICE Electron. Express 14 (2017) 20170143 (DOI: 10.1587/elex.14.20170143).
[8] A. M. S. Tosson, et al.: “A study of the effect of RRAM reliability soft errors on the performance of RRAM-based neuromorphic systems,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 25 (2017) 3125 (DOI: 10.1109/TVLSI.2017.2734819).
[9] J. Yun, et al.: “An efficient stream cipher for resistive RAM,” IEICE Electron. Express 14 (2017) 20170179 (DOI: 10.1587/elex.14.20170179).
[10] S. Li, et al.: “A study of the effect of RRAM reliability soft errors on the performance of RRAM-based neuromorphic systems,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 25 (2017) 3125 (DOI: 10.1109/TVLSI.2017.2734819).
[11] F. Rao, et al.: “Reducing the stochasticity of crystal nucleation to enable subnanosecond memory writing,” Science 358 (2017) 1423 (DOI: 10.1126/science.aao3212).
[12] Micron and Intel Announce Update to 3D XPoint Joint Development Program (2018) https://newsroom.intel.com/news-releases/micron-intel-announce-update-3d-xpoint-joint-development-program/
[13] X. Fan, et al.: “Optimization of periphery circuits in a 1 K-bit PCRAM chip for highly reliable write and read operations,” IEICE Electron. Express 11 (2014) 20141071 (DOI: 10.1587/elex.11.20141071).
[14] Y. Lei, et al.: “Enhanced read performance for phase change memory using a reference column,” IEICE Electron. Express 14 (2017) 20170032 (DOI: 10.1587/elex.14.20170032).
[15] Q. Zhang, et al.: “Design and security evaluation of PCM-based RPUF using cyclic refreshing strategy,” IEICE Electron. Express 15 (2018) 20180239 (DOI: 10.1587/elex.15.20180239).
[16] Y. Du, et al.: “Logic area reduction using the deep trench isolation technique based on 40 nm embedded PCM process,” IEICE Electron. Express 14 (2017) 20170628 (DOI: 10.1587/elex.14.20170628).
[17] R. J. Wai and K. H. Jheng: “High efficiency single-input multiple-output DC–DC converter,” IEEE Trans. Power Electron. 28 (2013) 886 (DOI: 10.1109/TPEL.2012.2205272).
[18] M. Yang, et al.: “A dual-mode single-inductor dual-output dc–dc converter with fast transient response,” IEICE Electron. Express 9 (2012) 1780 (DOI: 10.1587/elex.9.1780).
[19] N. Takai, et al.: “Single-inductor dual-output DC-DC converter design using RC ripple regulator method,” IEJE Trans. Electron. Inf. Syst. 136 (2016) 101 (DOI: 10.1541/ieejeiss.136.101).
[20] Y. Nakase, et al.: “On-chip single-inductor dual-output DC-DC boost converter having off-chip power transistor drive and micro-computer controlled MPPT modes,” IEICE Trans. Electron. E96.C (2013) 1420 (DOI: 10.1587/transene.E96.C.1420).
[21] M. Tanaka: “Recent progress in crystalline silicon solar cells,” IEICE Electron. Express 10 (2013) 20132006 (DOI: 10.1587/elex.10.20132006).
[22] Y. Arima and M. Ehara: “On-chip solar battery structure for CMOS LSI,” IEICE Electron. Express 3 (2006) 287 (DOI: 10.1587/elex.3.287).
[23] M. Yoshimoto, et al.: “Recent progress of biomedical processor SoC for wearable healthcare application: A review,” IEICE Trans. Electron. E102.C (2019) 245 (DOI: 10.1587/transelec.2018CD0001).
[24] C. L. Kok and L. Siek: “Unbalanced input pair zero current detector for DC–DC buck converter,” Electron. Lett. 51 (2015) 1359 (DOI: 10.1049/el.2015.0323).
[25] Z. Sun, et al.: “Adaptive gate switching control for discontinuous conduction mode DC–DC converter,” IEEE Trans. Power Electron. 29 (2014) 1311 (DOI: 10.1109/TPEL.2013.2263579).
[26] Y. S. Roh, et al.: “Active power factor correction (PFC) circuit with resistor-free zero-current detection,” IEEE Trans. Power Electron. 26 (2011) 630 (DOI: 10.1109/TPEL.2010.2070080).
[27] H.-M. Chen, et al.: “High-efficiency PPF boost converter with an accurate zero current detector,” IEEE Trans. Circuits Syst. II, Exp. Briefs 65 (2018) 1644 (DOI: 10.1109/TCSII.2017.2754514).
[28] M.-H. Huang, et al.: “Sub-1 V input single-inductor dual-output (SIDO) DC–DC converter with adaptive load-tracking control (ALTC) for single-cell-powered systems,” IEEE Trans. Power Electron. 25 (2010) 1713 (DOI: 10.1109/TPEL.2010.2042073).
[29] W. Sun, et al.: “A ripple control dual-mode single-inductor dual-output buck converter with fast transient response,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 23 (2015) 107 (DOI: 10.1109/TVLSI.2014.2299973).
[30] C.-W. Liu, et al.: “Dual-source energy-harvesting interface with cycle-by-cycle source tracking and adaptive peak-inductor-current control,” IEEE J. Solid-State Circuits 53 (2018) 2741 (DOI: 10.1109/JSSC.2018.2844358).
[31] A. Mahmoud, et al.: “A charge pump based power management unit with 66%-efficiency in 65 nm CMOS, ISCAS (2018) (DOI: 10.1109/ISCAS.2018.8350898).