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Investigation of resistive switching and transport mechanisms of Al$_2$O$_3$/TiO$_2$$_{-x}$ memristors under cryogenic conditions (1.5 K)

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ABSTRACT

Resistive switching and transport mechanisms of Al$_2$O$_3$/TiO$_2$$_{-x}$ memristor crosspoint devices have been investigated at cryogenic temperatures down to 1.5 K, for the future development of memristor-based cryogenic electronics. We report successful resistive switching of our devices in the temperature range of 300–1.5 K. The current–voltage curves exhibit negative differential resistance effects between 130 K and 1.5 K, attributed to a metal–insulator transition of the Ti$_4$O$_7$ conductive filament. The resulting highly nonlinear behavior is associated with an $I_{ON}/I_{OFF}$ diode ratio of 84 at 1.5 K, paving the way for selector-free cryogenic passive crossbars. Temperature-dependent thermal activation energies related to the conductance at low bias (20 mV) are extracted for memristors in a low resistance state, suggesting hopping-type conduction mechanisms. Finally, the transport mechanism analysis at 1.5 K indicates that for all resistance states, the conduction follows the space-charge limited current model in low fields, whereas trap-assisted tunneling dominates in higher fields.

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I. INTRODUCTION

Resistive switching memory devices, also called memristors, are being widely investigated as scalable non-volatile memories and artificial synapses in neuromorphic architectures. Current developments focus on room temperature applications such as large-scale storage class memory, monolithic 3D integration, or embedded artificial intelligence hardware for low-power edge computing. In the meantime, there are growing needs of scalable cryogenic electronics based on mature and emerging silicon technologies, especially in the field of quantum computing. Continuous progress in solid-state quantum technologies has led to promising high-quality silicon-based quantum bits (qubits) working below 100 mK. More recently, Yang et al. have demonstrated the operation of a silicon quantum processor with two qubits confined to quantum dots at $\sim$1.5 K. However, such quantum systems are currently controlled by room-temperature classical electronics connected to the cryostat by cumbersome electrical wires. While this approach allows us to operate few-qubit systems, it causes major scalability, automation, and performance issues hindering the fabrication of many-qubit architectures. It is, thus, necessary to explore novel cryogenic integration and packaging technologies enabling the fabrication of scalable silicon-based quantum systems. One of the most promising ways is the development of CMOS-compatible quantum-classical interfaces located inside the cryostat at one or multiple temperature stages. Such an interface would be composed of logic and memory systems dedicated to control and store qubit states as well as error correction algorithms. In that scope, several research groups are...
investigating cryogenic controllers based on CMOS and fully depleted silicon on insulator (FD-SOI) technologies operating at 4 K\textsuperscript{14,15} and 100 mK, respectively.\textsuperscript{16,17} However, only a few studies were reported on memory systems, aiming to investigate the performance of DRAM-based devices at temperature as low as 77 K.\textsuperscript{18,19} In that scope, demonstrating reversible, non-volatile, and highly non-linear resistance programming of resistive memory devices at cryogenic temperatures would offer opportunities for hybrid memristor–CMOS cryogenic electronics. This approach could enable local high-capacity data storage and memristor-based neuromorphic computing capabilities designed to control many-qubit systems. Until now, the lowest temperature at which resistive memories were studied is 4 K,\textsuperscript{10,11} mostly to obtain a better understanding of temperature-dependent behavior and conduction mechanisms of devices based on transition metal oxides.

In this work, we investigate the resistive switching, current–voltage–temperature (I–V–T) characteristics, and carrier transport mechanisms of Al\textsubscript{2}O\textsubscript{3}/TiO\textsubscript{2−x} memristor crosspoint devices at temperature as low as 1.5 K. Resistive switching cycles in the temperature range of 300–1.5 K are first demonstrated. Then, we discuss the influence of temperature on SET/RESET voltages and I–V characteristics, which exhibits a negative differential resistance (NDR) effect at low temperature from 130 K. Finally, we investigate the temperature-dependent conduction mechanisms at low bias as well as the transport behavior at 1.5 K.

II. EXPERIMENTS

The studied memristors with a TiN/Al\textsubscript{2}O\textsubscript{3}/TiO\textsubscript{2−x}/Ti/Pt structure and a 2 × 2 \( \mu \)m\textsuperscript{2} area were fabricated through contact UV lithography on thermally oxidized 1 × 1 cm\textsuperscript{2} silicon substrates. As illustrated in Fig. 1(a), the process flow starts with the fabrication of 2 \( \mu \)m wide and 80 nm high TiN bottom electrodes (BEs) using a back-end-of-line compatible damascene process in SiO\textsubscript{2}. The switching junction is then fabricated by depositing a 1.4 nm thick layer of Al\textsubscript{2}O\textsubscript{3} and a 30 nm thick layer of non-stoichiometric TiO\textsubscript{2−x} by atomic layer deposition (ALD) and physical vapor deposition (PVD), respectively. Finally, 2 \( \mu \)m wide and 75 nm thick Ti/Pt top electrodes (TEs) are patterned using lift-off techniques. A schematic cross section of the final devices is visible in Fig. 1(b). The test sample was wire bonded to a chip holder [see Fig. 1(c)] in order to conduct electrical characterizations at ambient and cryogenic temperatures in a Janis variable temperature insert (VTI) cryostat. In the latter case, the sample is located in a metallic cylinder under helium atmosphere to prevent any moisture condensation, which could influence the experimental results. A total of 10 devices and test structures were characterized from 300 K to 1.5 K with an Agilent E5270B parametric measurement system. For all measurements, the BEs were grounded and the signals were applied to the TEs. The average resistances of BEs and TEs were measured at each temperature, allowing the calculation of the voltage \( V_{\text{junction}} \) seen at the switching junction by subtracting from the total voltage \( V_{\text{total}} \) the drop of voltage resulting from access resistances.

III. RESULTS AND DISCUSSION

Figure 2 shows current–voltage characteristics of one of the studied memristors at 300 K and 1.5 K. Electroforming was initially performed at ambient temperature with a positive bias applied to the top electrode and a current compliance of 0.6 mA (see top-left inset). Successful resistive switching is visible at both room and cryogenic temperatures, with typical progressive SET–RESET behavior of TiO\textsubscript{2}–based memristors. However, significant differences are noticeable in I–V curves between 300 K and 1.5 K. First, the SET and RESET voltages determined by the inflexion point of dI/dV appear to vary differently as a function of temperature. As visible in the bottom-right inset of Fig. 2, the SET and RESET absolute voltages are first similar at 300 K, with values of about \( V_{\text{SET}} = 1.08 \) V and \( |V_{\text{RESET}}| = 1.05 \) V. However, only the RESET voltages tend to be significantly affected by temperature with a value of \( V_{\text{RESET}} = −1.28 \) V at 1.5 K. Regarding the SET voltages, the values are mostly stable around \( V_{\text{SET}} = 1.1 \) V as temperature decreases. The asymmetrical variations of \( V_{\text{SET}} \) and \( V_{\text{RESET}} \) with temperature could be related to the different temperature dependencies of

![FIG. 1. (a) Schematic representation of the fabrication process: (i) bottom electrode patterning by dry etching of the SiO\textsubscript{2}; (ii) TiN sputter deposition and planarization by chemical–mechanical polishing; (iii) deposition of the Al\textsubscript{2}O\textsubscript{3}/TiO\textsubscript{2−x} switching junction by ALD and PVD; (iv) Ti/Pt top electrode patterning by lift-off techniques and dry etching of the switching stack to open the bottom electrode contacts. (b) Schematic cross section of the devices. (c) Photograph of the 1 × 1 cm\textsuperscript{2} test sample wire bonded to the chip carrier used for cryogenic electrical measurement in a variable temperature insert (VTI) cryostat.](attachment:figure1.png)
the SET and RESET processes, involving oxygen vacancy migration and redox mechanisms.\textsuperscript{23} On the one hand, the growth of the conductive filament (CF) during the SET step is mainly due to the migration of oxygen vacancies induced by the electric field\textsuperscript{24} and thermophoretic forces emerging from local temperature gradients.\textsuperscript{25} On the other hand, several studies describe the RESET process as field-assisted and temperature-activated diffusion of oxygen ions and oxygen vacancies, leading to the rupture of the CF and, thus, a decrease in conductance.\textsuperscript{23,26,27} Therefore, a higher RESET bias must be applied as the temperature decreases in order to generate enough Joule heating to trigger ionic migration. It is worth mentioning that such an asymmetrical behavior was not observed on all tested memristors due to commonly reported device-to-device variability, seemingly accentuated at low temperature. This highlights the fact that working under cryogenic conditions can lead to different temperature-dependent variations between SET and RESET processes, which should be taken into account while developing adaptable conductance programming techniques.\textsuperscript{28}

The second major observable difference between 300 K and 1.5 K is the high nonlinearity of the $I$–$V$ curve under cryogenic conditions, exhibiting a negative differential resistance (NDR) behavior around 0.5 V. To further investigate the origin of this temperature-dependent phenomenon and its interplay with the cycle-to-cycle variability of the CF geometry, Fig. 3(a) shows $I$–$V$ characteristics of a memristor in the low resistance state (LRS) at various temperatures. The applied voltage $V_{\text{total}}$ was kept below the resistive switching regime in order to maintain the same resistance state for a given temperature stage. However, between each temperature stage, a full SET/RESET cycle was performed. At low bias, we can observe a global decrease in conductance with decreasing temperature, which is expected for metal–oxide–metal structures. Starting from 130 K and down to 1.5 K, one can notice significant NDR effects during current-controlled positive sweeps and a sudden current increase during voltage-controlled negative sweeps. The latter is better illustrated in Fig. 3(b), exhibiting local hysteresis behaviors at 77 K, 35 K, and 1.5 K. This phenomenon, often referred to as threshold switching, is volatile as only one stable state is visible at low voltage and is characterized by threshold voltages $V_{\text{th}}$ (forward sweep) and holding voltages $V_h$. The variation of $V_{\text{th}}$ and $V_h$ values does not seem
to be solely temperature-dependent as the highest values correspond to the resistive switching performed at 35 K. However, the results of multiple voltage sweeps (dotted lines) exhibit a reproducible behavior within the same switching cycle at a given temperature. This indicates that this threshold switching behavior is also affected by the structural properties of the CF. It has been demonstrated that the CF of TiO$_2$-based memristors could be composed of sub-oxide phases such as Ti$_4$O$_7$.\textsuperscript{23,26} This Magnéli phase of titanium oxide is known to undergo an abrupt metal–insulator transition (MIT) at temperatures ranging from 135 down to 120 K.\textsuperscript{23,26} We, therefore, attribute the drastic modification of the $I$–$V$ curves around 130 K to MIT of the Ti$_4$O$_7$ domains inside the CF induced by Joule heating. The threshold and holding voltages visible in Fig. 3(b), thus, correspond to the transition to metallic and insulating regimes, respectively, where their difference $D = V_{\text{th}} - V_h$ denotes an unstable phase of the Ti$_4$O$_7$. The values of $V_{\text{th}}$ and $V_h$ being directly related to the geometry and composition of the CF, the stochastic nature of the SET and RESET processes inducing fluctuations in resistance states\textsuperscript{23} can explain the seemingly anomalous data obtained at 35 K in Fig. 3(b). This observation comes in addition to the device-to-device variability previously mentioned, which should be considered when operating TiO$_2$-based devices in a cryogenic environment. Nevertheless, the fact that $V_{\text{th}}$ values tend to increase with decreasing temperature is due to the higher power needed to heat up the Ti$_4$O$_7$ to the critical temperature range of 120–155 K corresponding to MIT.\textsuperscript{23}

Interestingly, such high nonlinearity of our Al$_2$O$_3$/TiO$_2$-based memristors induced by the thermoelectrically triggered MIT of the CF paves the way for selector-free cryogenic passive crossbar architectures. In that scope, we calculated the $I_{\text{ON}}/I_{\text{OFF}}$ diode ratio as a function of temperature, with $I_{\text{ON}}$ and $I_{\text{OFF}}$ currents evaluated at $V_{\text{READ}} = 0.6$ V and $V_{\text{READ}}/2$, respectively. The obtained values listed in Fig. 3(a) are from 2 at 300 K up to a maximum of 84 at 1.5 K, with a significant increase after 130 K. This result is in the same order of magnitude as other oxides such as VO$_2$ or NbO$_2$ currently considered as promising candidates for room temperature MIT-based access devices in memristor arrays.\textsuperscript{33}

The following sections are dedicated to gain a better understanding of the influence of temperature on the conduction mechanisms. We first investigate the temperature dependence of the conductance at low bias, i.e., below non-volatile resistive switching regime and MIT. As observed in Fig. 3(a), the conductance $G$ decreases with the decrease in temperature $T$. In general, the temperature-dependent conductance $G(T)$ of disordered insulating thin films such as TiO$_{2-x}$, can be described by

$$G(T) = G_0 \exp \left( -\frac{E_a}{k_B T} \right),$$

where the temperature exponent $\alpha$ depends on the transport mechanism, $T_0$ is the characteristic temperature, and $G_0$ is the conductance at $T_0$.\textsuperscript{34,35} In order to determine the value of $\alpha$, Fig. 4 shows the fitting results for the Arrhenius plot of the low bias conductance of a device in LRS, measured from $I$–$V$–$T$ curves at 20 mV. A change in the slope is clearly noticeable as temperature decreases, defining two different regimes that we can associate with the metallic and insulating states of the CF. Between 300 K and 77 K, the data fit linearly with the Arrhenius equation,

$$G(T) = G_0 \exp \left( -\frac{E_a}{k_B T} \right),$$

where $G_0$ is a pre-exponential factor, $E_a$ is the thermal activation energy, and $k_B$ is the Boltzmann constant. This implies that $\alpha = 1$ in that temperature range, which can correspond to a nearest neighbor hopping (NNH) conduction mechanism between the localized states.\textsuperscript{34,37} The extracted thermal activation energy of the hopping electrons is $E_a = 53 \pm 3$ meV, which is in agreement with the recent work on TiO$_2$-based memristors.\textsuperscript{23} Regarding the insulating regime, while no activation energy can usually be found for pure TiO$_2$-based films,\textsuperscript{36} we extracted an activation energy of $E_a = 0.3 \pm 0.01$ meV. Such a low energy value implies that the NNH behavior is replaced by a weakly temperature-dependent conduction mechanism at cryogenic temperature. Based on Eq. (1), we found that $\ln(G)$ varies linearly with $T^{1/2}$ between 35 K and 1.5 K, as depicted in the inset of Fig. 4. The fact that $\alpha = 1/2$ suggests that, below 35 K, the transport mechanism at low bias follows the Efros–Shklovskii variable-range hopping (ES-VRH) conduction mechanism.\textsuperscript{35}

In this case, the hopping occurs under the influence of long-range electron–electron interactions between localized electrons, creating a Coulomb gap in the density of states near the Fermi energy.\textsuperscript{34,57}

To get insights into the electronic transport behavior at 1.5 K in the voltage range corresponding to the insulating regime ($\lesssim 0.3$ V), $I$–$V$–$T$ curves of LRS and HRS for a negative bias range are plotted at the double-logarithmic scale in Figs. 5(a) and 5(b), respectively. All curves exhibit well-linear fitting, which can be described by $I \propto V^m$, where the index $m$ is the slope of the fit. At 300 K, the current is linearly proportional to the applied voltage ($I \propto V$), which is in good agreement with the Ohm’s law. This is due to the density of thermally generated free carriers inside the switching junction being predominant over the electrode-injected charge carriers. As temperature decreases, the index $m$ increases up to a point where the current varies as $I \propto V^{1/2}$ at 77 K. This transport behavior can
FIG. 5. I–V–T curves of (a) LRS and (b) HRS in the negative bias range below the MIT (<∼0.3 V) plotted in double-logarithmic scale. The slopes of the various fitting lines are represented for each temperature. Their values suggest ohmic conduction at 300 K, trap-controlled SCLC at 77 K, and trap-filling SCLC at 1.5 K.

These curves can be explained in terms of the trap-controlled space-charge-limited conduction (SCLC) mechanism, where oxygen vacancies located in the TiO$_{2-x}$ layer act as traps for the electrons. Furthermore, according to the SCLC model, the current density depends on the thermal emission rate of the trapped electrons, which decreases with decreasing temperature and/or applied electric field. The observation of a decrease in current levels as temperature decreases is, thus, consistent with the SCLC model. Based on the assumption of single energy trapping levels, the current density can be described by

$$J_{\text{SCLC}} = \frac{9}{8} \varepsilon \mu \theta \frac{V^2}{L^3},$$

where $\varepsilon$ is the permittivity of the switching junction, $\mu$ is the electron mobility, $\theta$ is the ratio of free and shallow trapped charge, and $L$ is the thickness of the switching stack. Below 77 K, the index $m$ further increases to reach a maximum value of ∼3.5 at 1.5 K. This $I$–$V$ relation governed by a power law corresponds to the situation where all traps are being filled. The electrons in excess are injected into the conduction band of the oxide and, thus, contribute directly to conduction.

In the voltage range of the metallic regime at 1.5 K (∼0.6–1 V), trap-assisted tunneling (TAT) was found to be the dominating transport mechanism in all resistance states and bias ranges. The current density associated with the TAT model can be described by

$$J_{\text{TAT}} = A \exp\left(-\frac{8\pi q m^*}{3hE}\Phi_T^{1/2}\right),$$

where $A$ is a constant, $q$ is the electronic charge, $m^*$ is the effective mass of the electron in the oxide (∼9$m_0$ for the electrons in TiO$_2$), $h$ is Planck’s constant, $E$ is the electric field, and $\Phi_T$ is the energy of the trap below the oxide conduction band minimum (CBM). Figure 6 shows the ln$(J)$ vs $(1/E)$ plot of the SET process at 1.5 K, which exhibits well-linear fitting (note that the RESET process presents identical behavior). Using Eq. (4), the slope of the fits allows us to extract trap energy barrier values of 15 meV and 22 meV for LRS and HRS, respectively. TAT involves electrode-to-trap, trap-to-trap, and trap-to-electrode tunneling, where oxygen vacancies present in the switching junctions would play the role of traps. However, such low energy barrier values are not consistent with deep trap energy levels of ∼1 eV generally observed for oxygen vacancies in rutile by calculation and experiment. On the other hand, studies using density functional theory (DFT) have shown that localized energy states ∼0.2 eV below the CBM can be created by oxygen vacancies in rutile. Furthermore, recent DFT calculations
suggest that oxygen vacancy filaments in both bulk rutile and bulk anatase can introduce shallow traps with a wide defect conduction band close to the CBM. The low energy barrier values could, thus, be explained by a density of oxygen vacancies high enough to create localized states tens of meV below the CBM. The fact the TAT is the dominating conduction mechanism for both resistance states suggests that the CF is only partially formed at all time (see schematics in Fig. 6). Furthermore, the symmetry between positive and negative bias can be explained by a parabolic distribution of oxygen vacancies between the tip of the CF and the electrode. Finally, the higher trap energy barrier 49,50 found for HRS compared to LRS is related to the lower oxygen vacancy density, leading to a lowering of the defect conduction band. These results are in agreement with the recent work of Garbin et al. investigating the modelization of resistive memory devices based on trap-assisted tunneling only. This model also explains the cycle-to-cycle variability by random migration and placement of traps in the partially formed conductive filament.

IV. CONCLUSIONS

In summary, electrical characterizations of Al2O3/TiO2-x memristor crosspoint devices in cryogenic conduction have been performed, demonstrating successful resistive switching at temperature as low as 1.5 K. The volatile threshold switching is observed in the temperature range of 1.3–1.5 K attributed to metal–insulator transitions of the TiO2 conductive filament induced by Joule heating. The cycle-to-cycle dependence of this phenomenon is an additional factor of variability and should be further investigated through material engineering. Nevertheless, the resulting highly nonlinear behavior of the current–voltage characteristics exhibits an IOFF/IIFF ratio of 84 at 1.5 K, offering opportunities for selector-free memristor crossbar development for cryogenic electronics. Finally, at low bias and in a low resistance state, the study of the temperature dependence of the conductance suggests that hopping is the dominant transport mechanism, with the nearest neighbor hopping from 300 K to 77 K and Efros–Shklovskii variable-range hopping between 35 K and 1.5 K. In low fields, this behavior is characterized by an Ohmic conduction at 300 K, trap-controlled SCLC at 77 K, and trap-filling SCLC at 1.5 K. At such a low temperature and for higher field strengths, the lack of thermally activated carriers leads to a conduction mechanism dominated by trap-assisted tunneling for all resistance states and for both positive and negative bias regions. Our work is the first step toward memristor-based cryogenic electronics dedicated to quantum technologies and will lead to further investigations on conductance programming dynamics of TiO2-x-based memristors at very low temperature.

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