High gain DC/DC converter with continuous input current for renewable energy applications

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In this paper, a new design of a non-isolated high-voltage gain DC/DC converter that operates at a reasonable duty cycle, by merging the dual boost converter with the switched inductor structure, is presented as a solution for the high-conversion ratio requirement. The proposed converter operates in discontinuous-current mode (DCM) with zero current switching for all switches and diodes. Wide duty cycle range operation, high output voltage gain, low switching stress, small switching losses, and high efficiency are achieved efficiently. Operating the converter in DCM can support a wide range of the duty cycle operation, maintain lower voltage stress of all devices, ensure the same current sharing among inductors, make it easy to control, provide more stability, and require a smaller inductor which reduces size and weight of the proposed converter. Moreover, the converter operates with a continuous input current. These features make the converter a good choice for many applications such as photovoltaic, x-ray, fuel cells, etc. To prove the converter’s effectiveness, theoretical analysis, project specifications, and operation principles are presented and studied. Experimental results in an open and closed-loop, and a comparison with other recent converters are also introduced to confirm the validity of the proposed converter.

Scientists have been interested in renewable energy sources such as photovoltaic (PV) to produce electricity because they appeared to be the most efficient and effective solution to the environmental problems that the world faces today. The unregulated low-level DC output voltage from these sources is considered the biggest and the most important challenge that requires to be boosted to a regulated higher level using power electronic conditioning. The power electronic interface specification is dependent not only on the renewable energy supply but also on its effects on the power-system operation1. To obtain the voltage step-up function, a conventional non-isolated DC/DC boost converter was used2 because of its simple structure, simple control, and low cost. But it provided a limited practical gain because of their parasitic elements and must be operated at an extreme duty cycle in order to obtain high voltage gain. That causes a high-semiconductors voltage stress, diode reverse recovery problems, and high switching loss which decrease the system performance and efficiency. In3, cascaded boost converter has been successful in solving some of the problems appeared with conventional boost converter as it can attain a reasonable high voltage gain without working at extreme duty cycle, and the voltage stress through the switches remains lower than the voltage across the load. But, it has higher losses, lower efficiency, and electromagnetic interference problems. In switched-capacitor-based converters4,5 and switched capacitor/switched inductor-based converters6–9 high-voltage gain with small duty cycle, small voltage stress across the switches can be attained, and these converters can be used in a wide range of power. However, they have some problems such as higher losses, lower efficiency, electromagnetic interference problems, and reverse recovery problem.

The use of high-frequency transformers can increase the voltage gain as well as isolation, and then, full-bridge-based topologies can be used10, but with limited power capability, higher losses, lower efficiency, and higher cost. Full-bridge, half-bridge, fly back, forward, and push–pull converters are used at various voltage and power levels11–13 where isolation is needed. However, they suffer from numerous restrictions which reduce their efficiency, reduce performance in high step-up applications, and make the system more complicated and bulkier. They have also a limited range of increasing the voltage level besides higher voltage stress. Also, a massive turn-off voltage spikes in the power switch is generated due to the leakage inductance, which results in additional voltage stress on the components that require a snubber circuit to clamp the switch voltage resulting in a bigger size and more expensive. A high gain DC/DC converter utilizing coupled inductor and voltage multiplier cell that achieves high gain at a small duty ratio, and low voltage stress across the semiconductor components is

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An impedance network DC/DC boost converter is used in that reaches a high voltage gain with a small number of passive components which increase the losses and reduce the efficiency. The major drawback is it has a large number of passive components that make the system bulkier and more expensive. A high voltage gain p-type DC/DC converter is presented in that has the advantages of high gain with small duty cycle, continuous input current, common ground, and low voltage stress on semiconductors devices. However, it operates with hard switching and requires a high number of components that make the system larger and more expensive. To improve the voltage gain, a single switch three-Z-network converter is presented in. Although a high voltage gain is achieved, it has a large number of passive components which increase the losses and reduce the efficiency. An impedance network DC/DC boost converter is used in that reaches a high voltage gain with a small number of diodes and small duty cycle that avoids instability caused by saturation of its inductors. But, the main drawback of the converter is the lower efficiency. In, a step-up DC/DC converter with switched capacitor cells is presented. The converter provides high voltage gain at low duty ratios, low voltage stress on the switches and, switched capacitors, and it can be expanded. However, it has a large number of active and passive components that make the converter size larger and more expensive.

A single power switch high gain DC/DC converter with advantages of continuous input current, a small number of active components, and low voltage stress across the power switch and diodes is proposed in. But, it is limited power and has a large number of passive components. A non-isolated high gain DC/DC converter for dc micro grid applications with a single switch is presented in, with the advantage of simple control, and low voltage stress across the semiconductor devices. Even so, it operates with hard switching and has a large number of passive components. A transformer-less DC/DC converter based on a coupled inductor and switched capacitor–boosting techniques that increase the voltage gain with a low duty cycle is presented in. Although the voltage stresses across the active components are reduced, it operates with hard switching, has large losses and large number of elements, and hence large size and high expensive. A switched-inductor double power switches high gain DC/DC converter (SL-DS-DC) with higher voltage gain is presented in. However, it has more passive and active components which make the system bulkier and more expensive. A simple control scheme to improve the performance of a quadratic boost converter is presented in. This scheme provides a faster transient response and better noise immunity, but it has a large number of passive components, high losses because of hard switching, low efficiency, large size, and more expensive. High gain-switched boost DC/DC converters contain switched capacitor/switched inductor cells are presented in. The converters have advantages such as high voltage gain at non-extreme duty cycle, low voltage stresses across the switches and output diode, and they can be expanded to give higher gain. To provide higher gain, more cells should be added but this makes the system bulkier and is more expensive. In, a transformer-less high step-up DC/DC converter consisting of an active switched-inductor with quasi-Z-source circuit is offered. High voltage gain at the low duty cycle and high efficiency are achieved. The main drawback is the semiconductors’ components increased by increasing the switched-capacitor cells. A double boost-fly back converter is introduced in, the static gain is increased with the reduction of input current ripple where a combination between two conventional boost-fly back converters with input-parallel and floating output is done. However, if the converter operates with a duty cycle less than 0.5, the input current will be discontinuous with greater ripple. Also, with the increased number of fly back cells more sensors are needed which makes the system bulkier and more expensive.

In this paper, a new design of a non-isolated high-voltage gain DC/DC boost converter operating with a reasonable duty cycle by integrating dual boost converter with switched inductor structure is presented. The proposed converter operates with soft-switching (zero current switching (ZCS) mode for all switches and diodes. High voltage gain, low switching stress, small switching losses, and high efficiency are achieved. The operating modes, steady-state analysis, and design guidelines of the proposed circuit are discussed. Experimental results for the open and closed loops are conducted to verify the validity of the proposed circuit.

**Description and operating modes**

The proposed converter is composed of two similar converters connected to the same source as shown in Fig. 1. Each converter has two inductors, one capacitor, four diodes, and one switch. The four inductors have the same magnitude. The two switches are controlled in 180° phase delay to each other simultaneously. The proposed converter works in four modes as presented in Fig. 2. The key operating waveforms of the proposed converter are displayed in Fig. 3.

**Mode 1.** In this mode, i.e. \(0 \leq t \leq t_1\), the switch \(SW_1\) turns on, the switch \(SW_2\) turns off, the diodes \(D_2, D_4, D_6,\) and \(D_8\) are reversed biased and the diodes \(D_1, D_3, D_5,\) and \(D_7\) are forward biased. The first switched inductors \(L_1\) and \(L_2\) are connected in parallel with each other and being charged through the input voltage source \(V_i\) and the current through them increases. The current through the second switched inductors \(L_3\) and \(L_4\), which connected in series with each other, decreases and the voltage across them becomes \(V_5 - V_6\) that charges the capacitor \(C_2\).
with input source $V_s$. However, the capacitor $C_1$ discharges through the load. It is noted that $V_s$ is in series with both the output capacitors where the output load voltage ($V_o$) is $V_{C1} + V_{C2} - V_s$.

The voltage and current equations related to this mode are:

\[ V_s = V_{L1} = V_{L2}; \quad V_{C2} = V_s + V_{L3} + V_{L4}; \quad V_o = V_{C1} + V_{L3} + V_{L4} = V_{C1} + V_{C2} - V_s \tag{1} \]

\[ i_{S1} = i_{L1} + i_{L2}; \quad i_{L3} = i_{L4} = i_{C2} + i_o; \quad i_o = i_{C1}. \tag{2} \]
Mode 2. During this mode, i.e. \((t_1 \leq t \leq t_2)\), the switch \(SW_1\) is still turn on, the switch \(SW_2\) is still turn off, the diodes \(D_3, D_4, D_5, D_6, D_7, \) and \(D_8\) are reversed biased and the diodes \(D_1, D_2\) are forward biased. The first switched inductors \(L_1\) and \(L_2\) are still connected in parallel with each other and being charged through \(V_S\) and the current through them still increasing. The current through the second switched inductors \(L_3\) and \(L_4\) becomes zero as the diodes \(D_6\) and \(D_8\) are reversed biased. The capacitors \(C_1\) and \(C_2\) discharged through the load, and \(V_s\) is in series with them.

The voltage and current equations related to this mode are:

\[
V_S = V_{L1} = V_{L2}; \quad V_o = V_{C1} + V_{C2} - V_S
\] (3)

\[
i_{L3} = i_{L4} = 0; \quad i_{L1} = i_{L2} + i_{L3}; \quad i_o = i_{C1} = i_{C2}.
\] (4)

Mode 3. In this mode, i.e. \((t_2 \leq t \leq t_3)\), both switches \(SW_1\) and \(SW_2\) turn off. The diodes \(D_3, D_4, D_5, \) and \(D_6\) are reversed biased and the diodes \(D_1, D_2, D_7, \) and \(D_8\) are forward biased. The first switched inductors \(L_1\) and \(L_2\) are connected in series with each other, and the voltage across them is \(V_S - V_{C1}\). Also, the current through them decreases and charges the capacitor \(C_1\) with input voltage source \(V_S\) as diode \(D_7\) is forward biased. The second switched inductors \(L_3\) and \(L_4\) are connected in series with each other, and the voltage across them is \(V_S - V_{C2}\). Also, the current through them decreases and charges the capacitor \(C_2\) with input voltage source \(V_S\) as diode \(D_8\) is forward biased. Both the output capacitors are charged, and their voltage increases. They are in series with \(V_S\).

The voltage and current equations related to this mode are:

\[
V_{L1} + V_{L2} = (-V_{C1} + V_S); \quad V_{L3} + V_{L4} = (-V_{C2} + V_S); \quad V_o = V_{C1} + V_{C2} - V_S
\] (5)

Figure 3. Operating waveforms of the proposed converter at \(D=0.4\).
i_1 = i_3 + i_4; \; i_3 = i_2 = i_{C2}; \; i_4 = i_{C1} + i_o; \; i_1 = i_{C1} + i_{C2} + i_o.

\textbf{Mode 4.} In this mode, i.e. \((t_3 \leq t \leq T_S)\), the switch SW_1 is still turn off and the switch SW_2 is still turn on. The diodes D_1, D_2, D_3, D_6, D_7, and D_8 are reversed biased, and the diodes D_4 and D_5 are forward biased. The current through the first switched inductor L_1 and L_2 becomes zero as the diodes D_3 and D_7 are reversed biased. The second switched inductors L_3 and L_4 are still connected in parallel with each other and being charged through V_s, and the current through them still increasing. The capacitors C_1 and C_2 discharged through the load, and \(V_s\) is in series with both the output capacitors.

The voltage and current equations related to this mode are;

\[
V_o = V_{C1} + V_{C2} - V_s
\]

\[
i_{L1} = i_{L2} = 0; \; i_{S2} = i_{L3} + i_{L4}; \; i_o = i_{C1} = i_{C2}.
\]

\textbf{Derivation of voltage gain.} For the analysis point of view, the power losses are ignored. For the reason that both converters are boost type, it is assumed that the capacitor voltages \(V_{C1}\) and \(V_{C2}\) are larger than the input voltage \(V_s\). Also, both converters have equal duty cycles, the same value of inductances, and the output voltage for each converter has the same average value.

\[
D_1 = D_2 = D; \; L_1 = L_2 = L; \; V_{C1} = V_{C2} = V_c.
\]

During the on-state for one converter, the switch SW is closed. Therefore, the input voltage \(V_s\) appears across the switched inductors. As a result, a change in the current \(\Delta i_L\) flows through the switched inductors during a time period \(\Delta t\) by the formula:

\[
\Delta i_L = \left(\frac{1}{L_{eq1}}\right) V_s \Delta t.
\]

where \(L_{eq1}\) is the equivalent inductance of the switched inductors during the on-state, and it is equal to L/2 as the two inductors are connected in parallel.

At the end of the on-state, the increase of \(i_L\) is:

\[
\Delta i_{L-on} = \left(\frac{1}{L_{eq1}}\right) V_s \Delta t = \frac{2}{L} V_s (DT - 0)
\]

\[
\Delta i_{L-off} = \left(\frac{1}{L_{eq2}}\right) T \int_{t_{on}}^{T_{on}} V_{in} \Delta t = \frac{T}{2L} \left[ \int_{t_{on}}^{T} (-V_{C1} + V_s) \Delta t + \int_{t_{on}}^{T} (-V_{SW1} + V_s) \Delta t \right]
\]

and \(t_1 = (D + 0.2) T\)

\[
\Delta i_{L-off} = (T/2L)[(2 + 14D)V_s - (2 - 0.5D)V_{C1}] = (1/20) V_s T - (7/20) V_{C1} T.
\]

On the basis that the converter works in steady-state conditions, the amount of stored energy in each of its components has to be the same at the beginning and at the ending of the commutation cycle. Particularly, the stored energy in the inductor is given by:

\[
E = 0.5 L i^2.
\]

Therefore, the inductor current has to be the same at the start and end of the commutation cycle. This means the overall change in the current (the sum of the changes) is zero:

\[
\Delta i_{L-on} + \Delta i_{L-off} = 0
\]

Substituting \(\Delta i_{L-on}\) and \(\Delta i_{L-off}\) by their expressions yields:
Each module is a separate boost converter with switched inductors. Therefore, the voltage across the output capacitors \( C_1 \) and \( C_2 \) can be expressed as:

\[
\frac{V_{C_1}}{V_S} = \frac{1 + 9D}{1 - 0.25D}
\]

As clarified through the explanation of the different modes of operation, the two output capacitors are always in series with the input voltage source. Then, the output voltage can be given by:

\[
V_o = V_{C1} + V_{C2} - V_S.
\]  

From (12) and (13), the voltage gain of the proposed converter can be calculated by:

\[
G = \frac{V_o}{V_S} = \frac{1 + 18.25D}{1 - 0.25D}.
\]  

**Design consideration**

In this part, the main converter components are chosen using analytical relations derived from the converter operation. The design of inductors and capacitors depends on both the voltage across them and the current flowing through them.

**Inductor Design.** In case of \( D < 0.5 \), the inductors and input currents at \( t = \frac{T}{2} \) can be obtained by:

\[
i_4 \left( \frac{T}{2} \right) = \left( \frac{1 + 9D}{1 - 0.25D} \right) i_o + \frac{\Delta i_l}{2} - \frac{\Delta i_l}{1 - D} (0.5 - D);
\]

\[
i_2 \left( \frac{T}{2} \right) = \left( \frac{1 + 9D}{1 - 0.25D} \right) i_o - \frac{\Delta i_l}{2}; \quad i_1 \left( \frac{T}{2} \right) = \left( \frac{1 + 18.25D}{1 - 0.25D} \right) i_o - \frac{\Delta i_l}{2}.
\]

The input current can be obtained by:

\[
i_1 = i_4 + i_2 - i_o.
\]  

Using (15)–(16), the input current ripple can be expressed as:

\[
\Delta i_l = \frac{2(0.5 - D)}{1 - D} \Delta i_L.
\]  

The inductor current ripple can be expressed as:

\[
\Delta i_l = \frac{(V_C - V_S)(1 - D)}{L_{eq\cdot\text{on}}} T.
\]

From (17) and (18) the inductance can be obtained by:

\[
L = \frac{4(V_C - V_S)(0.5 - D)}{f_S \Delta i_l}
\]

where \( f_S \) is the switching frequency.

In a similar way in case of \( D > 0.5 \), the inductors and input currents at \( t = \frac{T}{2} \) can be obtained by:

\[
i_4 \left( \frac{T}{2} \right) = \left( \frac{1 + 9D}{1 - 0.25D} \right) i_o + \frac{\Delta i_l}{2} - \frac{\Delta i_l}{1 - D} (D - 0.5);
\]

\[
i_2 \left( \frac{T}{2} \right) = \left( \frac{1 + 9D}{1 - 0.25D} \right) i_o - \frac{\Delta i_l}{2}; \quad i_1 \left( \frac{T}{2} \right) = \left( \frac{1 + 18.25D}{1 - 0.25D} \right) i_o - \frac{\Delta i_l}{2}.
\]

Using (16) and (20), the input current ripple can be expressed as:

\[
\Delta i_l = \frac{2(D - 0.5)}{1 - D} \Delta i_L.
\]  

The inductor current ripple can be expressed as:

\[
\Delta i_l = \frac{V_S(1 - D)}{L_{eq\cdot\text{on}}} T.
\]

From (21) and (22) the inductance can be obtained by:
Finally, the larger value of the two calculated from (19) to (23) is chosen.

**Capacitor Design.** In case of $D > 0.5$, the capacitors and output voltages at $t = D \cdot T$ can be obtained by,

$$
V_{C1}(DT) = \left( \frac{1 + 9D}{1 - 0.25D} \right) V_S - \frac{\Delta V_C}{2}; \quad V_{C2}(DT) = \left( \frac{1 + 9D}{1 - 0.25D} \right) V_S + \frac{\Delta V_C}{2} - \frac{\Delta V_C}{D} (D - 0.5);
$$

$$
V_o(DT) = \left( \frac{1 + 18.25D}{1 - 0.25D} \right) V_S - \frac{\Delta V_o}{2}.
$$

Using (13) and (24), the output voltage ripple can be expressed as:

$$
\Delta V_o = \frac{2(D - 0.5)}{D} \Delta V_C.
$$

The capacitor voltage ripple can be calculated by:

$$
\Delta V_C = \frac{D i_o}{f_S C}.
$$

From (25) and (26), the capacitance can be obtained by:

$$
C = \frac{2(D - 0.5)i_o}{f_S \Delta V_o}.
$$

In a similar way, in case of $D < 0.5$, capacitor and output voltages at $t = D \cdot T$ can be obtained by,

$$
V_{C1}(DT) = \left( \frac{1 + 9D}{1 - 0.25D} \right) V_S - \frac{\Delta V_C}{2}; \quad V_{C2}(DT) = \left( \frac{1 + 9D}{1 - 0.25D} \right) V_S + \frac{\Delta V_C}{2} - \frac{\Delta V_C}{D} (0.5 - D);
$$

$$
V_o(DT) = \left( \frac{1 + 18.25D}{1 - 0.25D} \right) V_S - \frac{\Delta V_o}{2}.
$$

Using (13) and (28), the output voltage ripple can be expressed as:

$$
\Delta V_o = \frac{2(0.5 - D)}{D} \Delta V_C.
$$

The capacitor voltage ripple can be expressed as:

$$
\Delta V_C = \frac{D i_o}{f_S C}.
$$

The capacitance can be obtained by:

$$
C = \frac{2(0.5 - D)i_o}{f_S \Delta V_o}.
$$

Finally, the larger value of the two calculated from (27) and (30) is chosen.

**Converter power losses and efficiency**

In this section, the converter losses are analyzed by calculating the switching losses and conduction losses. The power losses of each device in the proposed converter are estimated, then the total power losses are investigated. Then, the converter efficiency is determined. The proposed converter model with the parasitic components is shown in Fig. 4. For the calculation of conduction loss in the converter, all diodes are considered with cut in voltages $V_{D1}$, $V_{D2}$, $V_{D3}$, $V_{D4}$, $V_{D5}$, $V_{D6}$, $V_{D7}$ and $V_{D8}$. Also, the internal resistances are $r_{D1}$, $r_{D2}$, $r_{D3}$, $r_{D4}$, $r_{D5}$, $r_{D6}$, $r_{D7}$, and $r_{D8}$. In a similar way, all inductors and capacitors are also considered with a lumped DC resistance and an equivalent series resistance, respectively. They can be represented as $r_{L1}$, $r_{L2}$, $r_{L3}$, $r_{L4}$ and $r_{C1}$, $r_{C2}$, respectively. Both conduction and switching losses are considered for switch with on-state resistance taken as $r_{SW1}$, $r_{SW2}$ for both switches.

**The switches losses.** The practical power switch has conduction and switching losses. Assume that the two switches ($SW_1$ and $SW_2$) have the same rms value of current and on-state resistance.

$$
i_s1 = i_s2 = i_s \quad \text{and} \quad r_{SW1} = r_{SW2} = r_{SW}
$$

The loss of the switching $SW_1$ is the sum of the conduction and switching losses and can be written as:

$$
P_{loss-\text{total}(SW1)} = P_{loss-\text{conduction}(SW1)} + P_{loss-\text{switching}(SW1)}
$$

where the switching loss of $SW_1$ can be expressed as:
The switching loss ($P_{loss\text{-switching}}$) of the power switch $SW_1$ can be determined by:

$$P_{loss\text{-switching}}(SW_1) = \frac{tr_{rt} \times r_{SW}}{2} + \frac{tf_{ft} \times V_{SW} \times i_{SW\text{-avg}} \times f_s}{4R(1-0.25D)}.$$  

(34)

The switching loss ($P_{loss\text{-switching}}$) of the power switch $SW_1$ can be determined by:

$$P_{loss\text{-switching}}(SW_1) = P_{loss\text{-switching}(SW_1)\text{-on}} + P_{loss\text{-switching}(SW_1)\text{-off}}.$$  

(33)

where $t_{rt}$ and $t_{ft}$ is the rise time and fall time of the switch, respectively.

Since the switches operate at ZCS during the turn-on transition period, the switching loss can be expressed as:

$$P_{loss\text{-switching}}(SW_1) = \frac{f_{ft} \times V_{SW} \times i_{SW\text{-avg}} \times f_s}{2}.$$  

(32)

Then, the switching loss of $SW_1$ is:

$$P_{loss\text{-total}(SW_1)} = \frac{V_o^2(1+18.25D)^2D \times r_{SW}}{4R^2(1-0.25D)^2} + \frac{f_{ft} \times V_o^2(1+9D)D \times f_s}{4R(1-0.25D)}.$$  

(35)

and the total switching loss can be expressed as:

$$P_{loss\text{-total}(Switches)} = P_{loss\text{-total}(SW_1)} + P_{loss\text{-total}(SW_2)}.$$  

(36)
\[ P_{loss\text{-total(Switcher)}} = \frac{V_o^2(1 + 18.25D)^2D \ast r_{SW}}{2R^2(1 - 0.25D)^2} + \frac{f_s \ast V_o^2(1 + 9D)D \ast f_s}{2R(1 - 0.25D)}. \] (36)

**The diodes losses.** The diodes are assumed to have the same cut in voltages and equivalent series resistance,

\[ V_{D1} = V_{D2} = V_{D3} = V_{D4} = V_{D5} = V_{D6} = V_{D7} = V_{D8} = V_D \]

\[ r_{D1} = r_{D2} = r_{D3} = r_{D4} = r_{D5} = r_{D6} = r_{D7} = r_{D8} = r_D \]

\[ i_{D1avg} = i_{D2avg} = i_{D4avg} = i_{D5avg} = i_{Davg} \]

\[ i_{D1rms} = i_{D2rms} = i_{D4rms} = i_{D5rms} = i_{Drms} \]

\[ i_{D3avg} = i_{D6avg} = i_{D7avg} = i_{D8avg} = i_{Davg1} \]

\[ i_{D3rms} = i_{D6rms} = i_{D7rms} = i_{D8rms} = i_{Drms1} \]

The total diodes losses can be expressed as:

\[ P_{loss\text{-total(Diodes)}} = \sum_{i=1}^{8} P_{loss\text{-Di}i} \] (37)

where

\[ P_{loss\text{-D1}} = P_{loss\text{-D2}} = P_{loss\text{-D4}} = P_{loss\text{-D5}} = V_D \ast i_{Davg} + i_{Drms} \ast r_D \]

\[ P_{loss\text{-D1}} = P_{loss\text{-D2}} = P_{loss\text{-D4}} = P_{loss\text{-D5}} = \frac{V_o(1 + 18.25D)D}{4R(1 - 0.25D)} + \frac{V_o^2(1 + 18.25D)^2D}{16R^2(1 - 0.25D)^2} \ast r_D \]

\[ P_{loss\text{-D3}} = P_{loss\text{-D6}} = P_{loss\text{-D7}} = P_{loss\text{-D8}} = V_D \ast i_{Davg1} + i_{Drms1} \ast r_D \]

\[ P_{loss\text{-D3}} = P_{loss\text{-D6}} = P_{loss\text{-D7}} = P_{loss\text{-D8}} = \frac{V_D \ast V_o(1 + 18.25D)D}{2R(1 - 0.25D)} + \frac{V_o^2(1 + 18.25D)^2D}{4R^2(1 - 0.25D)^2} \ast r_D \]

\[ P_{loss\text{-D3}} = P_{loss\text{-D6}} = P_{loss\text{-D7}} = P_{loss\text{-D8}} = \frac{V_o(1 + 18.25D)D}{4R(1 - 0.25D)} \left( 2V_D + \frac{V_o(1 + 18.25D)}{R(1 - 0.25D)} \ast r_D \right). \] (38)

Then, the total power loss in the diodes can be determined as:

\[ P_{loss\text{-total(Diodes)}} = \frac{V_o(1 + 18.25D)D}{R(1 - 0.25D)} \left( 3V_D + \frac{5V_o(1 + 18.25D)}{4R(1 - 0.25D)} \ast r_D \right). \] (39)

**The capacitors losses.** The proposed converter contains two capacitors. The total power loss due to the two capacitors is given by:

\[ P_{loss\text{-total(Capacitors)}} = \sum_{i=1}^{2} P_{loss\text{-Ci}} = i_{C1rms}^2 \ast r_C + i_{C2rms}^2 \ast r_C. \]

The two capacitors are assumed have the same equivalent series resistance, then:

\[ P_{loss\text{-total(Capacitors)}} = i_{C1rms}^2 \ast r_C + i_{C2rms}^2 \ast r_C = 2i_{Crms}^2 \ast r_C. \] (41)

The \( rms \) value of current through the capacitor can be estimated using the expression:

\[ i_{C1rms} = i_{C2rms} = i_{Crms} = \frac{V_o}{R} \left( D + \frac{(1 - 0.25D)(1 - D)}{(1 + 18.25D)} \right). \] (42)

Then total power loss due to the two capacitors is given by:

\[ P_{loss\text{-total(Capacitors)}} = \frac{2V_o^2}{R^2} \left( \frac{0.25(1 + 18.25D)^2D}{(1 - 0.25D)^2} + \frac{17(1 - D)D^2}{(1 - 0.25D)^2} + 0.8(1 - D) \right) \ast r_C \] (43)

**The inductors losses.** The inductors loss can be expressed as
\[ P_{\text{loss-total(Inductors)}} = \sum_{i=1}^{4} P_{\text{loss-}}L_i = \sum_{i=1}^{4} i_{L rms}^2 r_L i \]

\[ P_{\text{loss-total(Inductors)}} = i_{L1 rms}^2 r_{L1} + i_{L2 rms}^2 r_{L2} + i_{L3 rms}^2 r_{L3} + i_{L4 rms}^2 r_{L4} \quad (44) \]

If the inductors are assumed to have the same internal resistance \( r_{L1} = r_{L2} = r_{L3} = r_{L4} = r_L \), and have the same \( rms \) value of the inductor currents.

\[ i_{L1 rms} = i_{L2 rms} = i_{L3 rms} = i_{L4 rms} = i_{L rms} \]

\[ P_{\text{loss-total(Inductors)}} = i_{L rms}^2 (r_{L1} + r_{L2} + r_{L3} + r_{L4}) \]

\[ P_{\text{loss-total(Inductors)}} = 4 i_{L rms}^2 r_L. \quad (45) \]

Using the equations in the “Description and operating modes” section, the \( rms \) value of the inductor current can be noticed

\[ i_{L rms} = \frac{V_O (1 + 18.25D)}{4R(1 - 0.25D)} (0.4 + 0.6D). \quad (46) \]

Then, substituting in Eq. (45), the total power loss in the inductors can be stated as

\[ P_{\text{loss-total(Inductors)}} = \frac{V_O^2 (1 + 18.25D)^2 (0.4 + 0.6D)^2}{4R^2 (1 - 0.25D)^2} r_L. \quad (47) \]

Substituting from Eqs. (36), (40), (43), and (47) into the below equation, the total converter loss can be obtained.

The expression for total losses is as follows:

\[ P_{\text{loss-total}} = P_{\text{loss-total(Switches)}} + P_{\text{loss-total(Diodes)}} + P_{\text{loss-total(Capacitors)}} + P_{\text{loss-total(Inductors)}}. \quad (48) \]

Finally, the efficiency \( (\eta) \) of the proposed converter can now be determined as:

\[ \eta = \frac{P_O}{P_O + P_{\text{loss-total}}} \quad (49) \]

where \( P_o \) is the output power.

**State space representation**

This section presents the state space modelling of the proposed converter. The state variables in the proposed converter are selected as the inductor currents \((i_{L1}(t), i_{L2}(t))\), the capacitor voltages \((v_{C1}(t), v_{C2}(t))\), and the output voltage \((v_{vo}(t))\). The input variables are chosen as the input voltage \((V_i(t))\) and the input current \((i_i(t))\). The equivalent circuits showing the converter behavior of the four modes of operation are used as given in Fig. 2. The corresponding state space differential equations are obtained from these equivalent circuits. Kirchhoff’s voltage and current laws are applied for this purpose.

From equivalent circuit of Fig. 2a, the differential equations for operation mode 1 are derived as,

\[ \begin{align*}
L_1 \frac{di_{L1}(t)}{dt} &= V_S \\
L_2 \frac{di_{L2}(t)}{dt} &= V_S \\
C_1 \frac{dv_{C1}(t)}{dt} &= \frac{v_{vo}(t)}{R} \\
C_2 \frac{dv_{C2}(t)}{dt} &= -i_{L1}(t) - i_{L2}(t) + i_i(t) \\
\end{align*} \quad (50) \]

From equivalent circuit of Fig. 2b, the differential equations for operation mode 2 are derived as,

\[ \begin{align*}
L_1 \frac{di_{L1}(t)}{dt} &= V_S \\
L_2 \frac{di_{L2}(t)}{dt} &= V_S \\
C_1 \frac{dv_{C1}(t)}{dt} &= \frac{v_{vo}(t)}{R} \\
C_2 \frac{dv_{C2}(t)}{dt} &= v_{C2}(t) \\
\end{align*} \quad (51) \]

From equivalent circuit of Fig. 2, the differential equations for operation mode 3 are derived as,
\[ \begin{aligned}
L_1 \frac{di_{L1}(t)}{dt} &= -\frac{V_c(t)}{R} + \frac{V_0}{R} \\
L_2 \frac{di_{L2}(t)}{dt} &= -\frac{V_c(t)}{R} + \frac{V_0}{R} \\
\frac{di_{C1}(t)}{dt} &= C_1 \frac{dv_{C1}(t)}{dt} = \frac{i_{L1}(t) - V_c(t)}{R} \\
\frac{di_{C2}(t)}{dt} &= C_2 \frac{dv_{C2}(t)}{dt} = \frac{i_{L2}(t) - V_c(t)}{R} \\
\frac{dv_o(t)}{dt} &= \frac{i_{L1}(t)}{C_1} - \frac{V_c(t)}{R} + \frac{i_{L1}(t)}{C_2} + \frac{i_{L2}(t)}{C_2}
\end{aligned} \]

(52)

From equivalent circuit of Fig. 2d, the differential equations for operation mode 4 are derived as,

\[ \begin{aligned}
L_1 \frac{di_{L1}(t)}{dt} &= 0 \\
L_2 \frac{di_{L2}(t)}{dt} &= 0 \\
\frac{di_{C1}(t)}{dt} &= C_1 \frac{dv_{C1}(t)}{dt} = \frac{V_c(t)}{R} \\
\frac{di_{C2}(t)}{dt} &= C_2 \frac{dv_{C2}(t)}{dt} = \frac{V_c(t)}{R} \\
\frac{dv_o(t)}{dt} &= \frac{i_{L1}(t)}{RC_1} + \frac{i_{L2}(t)}{RC_2}
\end{aligned} \]

(53)

To derive the transfer function of the proposed converter from the duty ratio to the output voltage, the previous differential equations are used.

The average state space model can be written as:

\[ \begin{aligned}
\dot{x}(t) &= Ax(t) + Bu(t) \\
y(t) &= Cx(t)
\end{aligned} \]

(54)

where the coefficient matrices \(A\), \(B\), and \(C\) are given by:

\[ [A] = A_1 d_1 + A_2 d_2 + A_3 d_3 + A_4 d_4 \]

\[ [B] = B_1 d_1 + B_2 d_2 + B_3 d_3 + B_4 d_4 \]

\[ d = d_1 + d_2 + d_3 + d_4 = 1 \]

(55)

where

\[ d_1 = (d - 0.5) \]

\[ d_2 = (1 - d) \]

\[ d_3 = (d - 0.5) \]

\[ d_4 = (1 - d). \]

(56)

State space modeling of the proposed DC-DC converter is written as:

\[ \begin{bmatrix}
\dot{i}_{L1}(t) \\
\dot{i}_{L2}(t) \\
\dot{v}_{C1}(t) \\
\dot{v}_{C2}(t) \\
\dot{v}_O(t)
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & \frac{1}{L_1} \left( \frac{2d-1}{4} \right) & 0 & 0 \\
0 & 0 & -\frac{1}{L_1} \left( \frac{2d-1}{4} \right) & 0 & 0 \\
\frac{1}{C_1} \left( \frac{2d-1}{2} \right) & 0 & 0 & 0 & \frac{1}{R} \left( 1 - d \right) \\
\frac{1}{C_2} (2d-1) & -\frac{1}{C_2} (2d-1) & \frac{1}{C_2} (2d-1) & 0 & 0 & \frac{1}{RC_1} \left( 1 - d \right) \\
(2d-1) \left( \frac{1}{L_1} + \frac{1}{L_2} \right) & \frac{1}{C_2} (2d-1) & \frac{1}{C_2} (2d-1) & 0 & 0 & \frac{1}{RC_1} + \frac{1}{RC_2}
\end{bmatrix}
\begin{bmatrix}
i_{L1}(t) \\
i_{L2}(t) \\
v_{C1}(t) \\
v_{C2}(t) \\
v_O(t)
\end{bmatrix} \]

(57)

\[ \begin{bmatrix}
\frac{1}{L_1} \left( \frac{1+2d}{4} \right) & 0 \\
\frac{1}{L_2} \left( \frac{1+2d}{4} \right) & 0 \\
0 & 0 \\
0 & \frac{1}{C_1} (2d-1) \\
0 & \frac{1}{C_2} (2d-1)
\end{bmatrix}
\begin{bmatrix}
V_S(t) \\
i_1(t) \\
i_2(t)
\end{bmatrix} \]

\[ y(t) = v_o(t) = \begin{bmatrix}
0 & 0 & 0 & 1
\end{bmatrix}
\begin{bmatrix}
i_{L1}(t) \\
i_{L2}(t) \\
v_{C1}(t) \\
v_{C2}(t) \\
v_O(t)
\end{bmatrix}. \]

(58)

**Experimental results**

To prove the validity of the proposed converter, it is tested on the laboratory hardware platform as shown in Fig. 5. The schematic diagram of the experimental system is shown in Fig. 6. For experimental analysis, the converter parameters are listed in Table 1.

**Open loop performance.** Figures 7, 8, 9 and 10 show the experimental waveforms of the proposed converter at duty cycle 0.4. These figures include the resulted waveforms of the gate signal of switches SW1 and...
Figure 5. Experimental set up of the proposed converter.

Figure 6. A schematic diagram of the experimental system.

Table 1. Converter component specifications for experimental test.

| Devices                  | Value         |
|--------------------------|---------------|
| Inductances ($L_1, L_2, L_3, L_4$) | 9.3 mH        |
| Capacitances ($C_1, C_2$) | 4.7 μF        |
| Power switches ($SW_1, SW_2$) | CM100DY-24H   |
| Diodes ($D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8$) | MUR1560       |
| Input voltage ($V_i$)    | 24 V          |
| Output voltage ($V_o$)   | 226 V         |
| Switching frequency ($f_s$) | 1 kHz        |
| Duty cycle ($D$)         | 0.4           |
| Gain ($G$)               | 9.4           |
Figure 7. Experimental waveforms of the proposed converter. Part I. (a) Gate signals of switches, (b) Input voltage, $V_s$, (c) Output voltage, $V_o$, (d) Input current, $I_s$, (e) Voltage of capacitor $C_1$, and (f) Voltage of capacitor $C_2$.

Figure 8. Experimental waveforms of the proposed converter. Part II. (a) Voltage–Current of switch SW$_1$, and (b) Voltage–Current of switch SW$_2$. 

SW2, the input and output voltages, the input current, the voltage across the capacitors, and the voltage-current of the switches, diodes, and inductors. Figure 7a shows the gate pulses of SW1 and SW2. The input voltage supplied from PV is shown in Fig. 7b and equal to 24 V. It can be seen from Fig. 7c that the output voltage equals to 226 V which gives a gain of 9.4. This performance proves that the proposed converter gives a high voltage gain at reasonable duty cycle. Figure 7d shows the continuous input current waveform. As shown in Fig. 7e,f, both the voltage of the capacitors is equal and has an average value of 125 V that is equal to 55.3% of output voltage.

Figure 9. Experimental waveforms of the proposed converter. Part III. (a) Voltage–Current of diode D1, (b) Voltage–Current of diode D2, (c) Voltage–Current of diode D3, (d) Voltage–Current of diode D4, (e) Voltage–Current of diode D5, (f) Voltage–Current of diode D6, (g) Voltage–Current of diode D7, and (h) Voltage–Current of diode D8.
That ensures a low voltage stress of the capacitors, and it also achieves the Eq. (7). As shown from Fig. 8a,b, the maximum voltage across each switch (SW1 or SW2) is almost equal to 57.5% of the output voltage which shows a low voltage stress for all switches. Furthermore, all switches operate in soft switching mode (ZCS) that decrease the switching losses of the switches. Moreover, from Fig. 9, the absolute maximum voltages across diodes $D_1$, $D_2$, $D_3$, $D_4$, $D_5$, and $D_6$ and across diodes $D_7$ and $D_8$ are almost equal to 39.8% and 53.1% of the output voltage, respectively which show a low voltage stress for all diodes. Also, all diodes operate in soft switching mode (ZCS) that decrease the diodes losses.

The inductor current ($i_L$) is discontinuous as seen in Fig. 10 which shows that the converter is operating in DCM as mentioned before. Figure 11 shows the experimental measured efficiency of the proposed converter, in which it ascertains a high efficiency of the proposed topology. The maximum overall efficiency equals 93% measured at 120 W load. Figure 12 shows the voltage gain versus duty cycle of the theoretical equation, simulation results, and experimental results. It can be concluded that the experimental results are in good agreement with the theoretical analysis (Equation-14), and simulation results. From the previous experimental results, the proposed converter provides a high voltage gain with a low duty cycle, and it has small voltage stress of all semiconductor devices. Furthermore, a continuous input current is attained which a desirable feature of the DC/DC converter is making it suitable for PV applications. Therefore, it has low switching losses without any
additional circuits. Also, it has components with a low nominal rating that makes the proposed converter small size, low price, and high overall efficiency. The aforementioned advantages make the proposed converter suitable for numerous industrial applications.

**Closed loop performance.** To examine the performance of the proposed converter under closed-loop control, the OWON TDS8204 oscilloscope and DSP1104 are used to record the results. PI controller is also used for control. The parameters for the PI controller are $K_p = 0.38$ and $K_i = 200$. A schematic diagram of the circuit that is used to control the output voltage of the proposed circuit is shown in Fig. 13. First, the proposed converter is tested by changing the reference voltage (increased/decreased) by 100 V. It can be seen from Fig. 14 that the output voltage of the proposed converter responds to the step change (increase/decrease) of the reference voltage and changes from 100 to 200 V and then from 200 to 100 V according to the value of reference voltage. Also, the

Figure 12. Voltage gain versus duty cycle of the proposed converter.

Figure 13. A schematic diagram of the control circuit used.

Figure 14. Experimental step change (increase/decrease) in reference voltage.
Figure 15. Experimental response to step increasing in input voltage.

Figure 16. Experimental response to step decreasing in input voltage.
transient period is found very small and less than 200 ms. Second, the proposed converter is tested by changing the input voltage source (increase/decrease) by 4 V. It can be seen from Figs. 15 and 16 that the output voltage value is remaining constant at the reference voltage value of 150 V. Also, the overshoot value is less than 7.5 V, and it is equal to 5% of the output voltage. Finally, the proposed converter is tested for variation in load values. The response to the step change (increase/decrease) in load is shown in Fig. 17. The converter is operating at 65% of full load. At first, the load increased by 35% of full load value to make the converter operate at full load, and then the load decreased by 35% of full load value to make the converter operate at 65% of the full load again. It is evident from the figure that the proposed converter operates at constant output voltage under load changes.

Comparison of the proposed converter with recent converters. The proposed converter is compared with SL-Boost, single-active switch, non-inverting, SL-DS-DC, cascaded boost, SC/SL-SBC, double boost flyback, and ZSC converters. For a valid comparison, coupled inductor turns ratio (n) of the double boost-flyback converter was set to unity. The comparison results are presented in Table 2. The voltage gain comparison is presented in Fig. 18. It is clear that the proposed converter can operate with a wide range of duty cycle while the SL-DS-DC, and SC/SL-SBC converters operate only up to 0.3 duty cycle, and ZSC operates up to 0.5 duty cycle. Furthermore, the proposed converter has a higher gain at most of the duty cycle in comparison with SL-boost,
single-active switch, cascaded boost, SC/SL-SBC, double boost fly back, and ZSC converters except SL-DS-DC converter that have the highest gain up to 0.3 only and the non-inverting converter. For the number of passive and active components, the proposed converter shows a modest number of active and passive components in comparison with SL-boost, single-active switch, non-inverting, SL-DS-DC, double boost fly back, and SC/L-SBC converters except cascaded boost and ZSC converters that have the lower components counts. However, they (cascaded boost and ZSC converters) operate at a larger duty cycle which may produce saturation problems in the inductor current or core. All the converters operate in continuous input current except the SL-boost, and ZSC converters. Also, the double boost fly back converter presents a discontinuous input current if it operates at a duty cycle of less than 0.5. The current ripple is low and within the allowed limit for all converters except the ZSC converter. Also, all converters operate with hard switching except the proposed converter that operates in soft switching for all semiconductor devices which makes lower losses and higher efficiency at higher gains. The switch voltage stress comparison is shown in Fig. 19. The proposed converter has a lower maximum switch voltage stress if it compared with all the converters except the single-active switch converter which has the smallest switch voltage stress. A lower switch voltage stress makes the losses lower and selecting a low nominal rating of switches that makes the converter small size, low price, and high overall efficiency. The capacitor voltage stress comparison is shown in Fig. 20. The proposed converter has a lower capacitor voltage stress if it compared with single-active switch, SL-DS-DC, SC/SL-SBC, and ZSC converters. A lower capacitor voltage stress gives a benefit of choosing a low nominal rating of capacitors that makes the converter smaller in size, and hence lower price. The output diode voltage stress is compared as shown in Fig. 21. The diode voltage stress of the proposed converter is lower than all the converters except the single-active switch converter. Lower voltage stress of output diode makes the nominal rating of diode much lower which affects the converter size and price. The efficiency of the proposed converter is reasonable compared to the other converters except for the cascaded boost converter which has the highest efficiency. However, the cascaded boost converter cannot accomplish a higher gain due to parasitic. Alternatively, a single-active switch converter has low voltage gain although it has similar elements count as the proposed converter. Theoretically, the converter power density depends on the number of semi-

Figure 18. Voltage gain comparison.

Figure 19. Switch voltage stress comparison.
conductor devices and the volume of the passive components. As known, the volume of passive components is proportional to the energy stored in them. So, if the stored energy is computed, then the volume of the passive components can be estimated. The total energy stored for the inductor is calculated by

\[ E_L = 0.5 \times L \times (i_{L_{av}})^2 \]

where \( i_{L_{av}} \) is average current through the inductor \( L \), and the total energy stored for the capacitor is given as

\[ E_C = 0.5 \times C \times (V_C)^2 \]

where \( V_C \) is voltage through the capacitor \( C \).

While evaluating the energy stored in the inductor, it is assumed that the frequency and ripple currents are the same for all the compared converters. Furthermore, the energy stored in the capacitor is computed for a similar value of capacitances.

For voltage gain, \( G = 5 \), the total energy stored in the inductor and capacitor for all the converters is recorded in Table 2. It is obvious that the total energy stored, i.e., volume required is modest in the proposed topology (38). The double boost flyback converter is the smallest (27), however it has minimal voltage gain. The quantity of energy stored in inductors and capacitors that mentioned in Table 2 is made to be unitless.

Based on the previous various performance parameters and characteristics comparison, the proposed converter gives a high voltage gain at a low duty cycle. It has a modest number of semiconductor devices with low voltage stress and hence small nominal voltage rating, and lower losses making the converter smaller in size, higher efficiency, and has a good performance. According to these comparisons, the proposed converter is considered a strong competitor to the other converters.

**Conclusion**

In this paper, a new non-isolated high voltage gain DC/DC converter by integrating a dual boost converter with a switched inductor structure is proposed. The proposed converter operates with a modest duty cycle (less than 0.5) with a continuous input current. The converter operates with a soft switching (ZCS) for all diodes and
switches which plays an important role in reducing the losses. A wide operating range of the duty cycle is available. An equal current sharing among boost inductors makes it easy to control. Also, the proposed converter offers high efficiency due to the low switching losses, lower voltage stress for all passive and active components, and the lack of reverse recovery loss on diodes. It requires a small inductor, and a small nominal rating for all semiconductor devices which reduces the size, weight, and price of the proposed converter. These features make the converter a good choice for many applications such as PV, x-ray, fuel cells, etc. Moreover, the description, operating modes in DCM, design guidelines, and open and closed-loop performance are presented. Besides, a comparative analysis with recent converters is presented. The converter is examined at various power ratings for efficiency analysis and maximum efficiency of 93% is achieved. Experimental results in open and closed-loop prove the good performance of the proposed converter.

Data availability
All data generated or analyzed during this study are included in this published article.

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A.S.M. performed visualization, data acquisition and curation, methodology, software, supervision and reviewing and editing. A.H.H.A. performed conceptualization, writing—original draft preparation. E.E.E-K. performed supervision, visualization, validation, reviewing and editing. M.S.Z. helped with formal analysis, writing—review, and editing.

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**Additional information**
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