Interface Optimization and Transport Modulation of Sm$_2$O$_3$/InP Metal Oxide Semiconductor Capacitors with Atomic Layer Deposition-Derived Laminated Interlayer

Jinyu Lu $^{1}$, Gang He $^{1,*}$, Jin Yan $^{1}$, Zhenxiang Dai $^{2}$, Ganhong Zheng $^{1,*}$, Shanshan Jiang $^{3}$, Lesheng Qiao $^{1}$, Qian Gao $^{1}$ and Zebo Fang $^{1,*}$

1. Introduction

As the integration of IC continues to increase, CMOS feature sizes will also continue to decrease in order to reduce the cost of individual transistors, increase the switching speed of transistors, and reduce the power consumption of the circuit. As the feature size of CMOS devices continues to decrease, it will also cause the SiO$_2$ gate dielectric and Si substrate used in conventional processes to decrease in size as well. When the size is smaller than a certain limit, the gate leakage current will grow exponentially, while the device will not operate properly due to the laws of quantum physics [1,2]. The use of high-k materials for the replacement of SiO$_2$ gate dielectrics is an option that has been shown to be feasible [3]. Among these high k materials, samarium oxide (Sm$_2$O$_3$) is considered as the next potential gate dielectric due to its high dielectric constant (~15) [4], sufficiently large band gap (5.1 eV) [5], low hygroscopicity, and high chemical and thermal stability [6]. Coulomb scattering and phonon scattering at the interface between the high-k gate dielectric and the channel material lead to a significant reduction in channel mobility, which severely affects...
the further increase in the speed of CMOS logic devices. Selecting channel materials with high mobility is an effective way to solve this problem [7]. Compared with conventional Si-based material CMOS devices, III-V group semiconductors have advantages due to their large switching speed and small dynamic power consumption [8]. Among the group III-V semiconductors, InP has received more attention due to its higher carrier mobility and smaller band gap [9].

However, InP is prone to the formation of interfacial defects, which can limit the operating performance of the device [10]. Also, a surface with many chemical impurities can have a considerable impact on the performance of InP MOS capacitors [11]. High $D_{it}$ leads to the frequency dispersion of the Fermi energy level pegging and capacitance, which also prevents the formation of inverse or accumulation layers in CMOS devices [12].

Different InP surface passivation methods have been investigated for a long time, including low-temperature processes [13], ozone treatment [14], chemical etching [15], and sulfide solution passivation [16,17]. A great deal of work has also been devoted to atomic layer deposition (ALD) passivation layers to modulate the InP interface [18]. It has been demonstrated that ALD-derived Al$_2$O$_3$ films can effectively suppress the interfacial diffusion from the substrate to the high-k films. More importantly, the operating temperature can be kept low (~200 °C) when the Al$_2$O$_3$ film is on the passivated substrate surface. There are previous reports confirming that the insertion of Al$_2$O$_3$ between the high-k gate dielectric and GaAs can improve the thermal stability. However, even in the presence of an Al$_2$O$_3$ passivation layer to improve the interface, the diffusion of In and P elements into the gate dielectric still has an impact on the electrical characteristics of the device when fabricating InP MOS capacitors. R. V. Galatage et al. reported that the In-O and P-O states at the interface lead to a degradation of the electrical characteristics [19]. Their results also demonstrated the effectiveness of ALD-derived Al$_2$O$_3$ passivation layers between the gate dielectric and the InP substrate. Chee-Hong An et al. systematically analyzed that Al$_2$O$_3$ can inhibit dissociation and reactant diffusion in InP substrates [20]. However, the effect of the position of the Al$_2$O$_3$ passivation layer on the electrical properties and interfacial bonding state of InP MOS devices has not been reported systematically.

In this work, we deposited Sm$_2$O$_3$ films by magnetron sputtering and obtained Al$_2$O$_3$ passivation layers by ALD equipment to fabricate three different gate stacks on InP substrates, corresponding to Al$_2$O$_3$/Sm$_2$O$_3$/InP, Al$_2$O$_3$/Sm$_2$O$_3$/Al$_2$O$_3$/InP, and Sm$_2$O$_3$/Al$_2$O$_3$/InP, respectively. X-ray photoelectron spectroscopy (XPS) and electrical measurements were used to investigate the effect of Al$_2$O$_3$ passivation position on the chemical composition and electrical parameters of the interface. In addition, the leakage current conduction mechanisms (CCMs) of InP-based MOS capacitors with three different laminated gate electrical stacks measured at room temperature and low temperature (77–227 K) were systematically investigated.

2. Materials and Methods

In this work, we chose sulfur-doped n-type InP wafers as the substrate for fabricating MOS capacitors. Before depositing the Sm$_2$O$_3$ gate dielectric, the wafers were subjected to a standard degreasing process by sequential immersion in ethanol and acetone for 5 min each. After that, the wafers were immersed in 20% ammonium sulfide solution for 15 min to remove the native oxides. Then, the wafers are rinsed with deionized water and then blown dry with high purity nitrogen gas. The cleaned wafers were transferred to an ALD system (MNT-PD1000z-L651G2, MNT Micro and Nanotech). On the ALD process, plasma O$_2$ and trimethylaluminum (TMA) were selected as the oxidant and aluminum metal precursor, and a 2 nm Al$_2$O$_3$ passivation layer was deposited on the InP substrate. The Al$_2$O$_3$ passivation layers were deposited by using 30 pulse cycles of plasma O$_2$ precursors [O$_2$(2s)/Ar purge (25s)] and 15 pulse cycles of trimethylaluminum (TMA) and plasma O$_2$ [TMA (0.03s)/O$_2$ 2s/Ar purge (25s)], respectively. During this process, the chamber pressure and the deposition temperature were maintained at 35 Pa and 200 °C. After ALD Al$_2$O$_3$ passivation, the wafers were transferred to a sputtering chamber to deposit Sm$_2$O$_3$ gate...
dielectrics by sputtering samarium target with purity of 99.9%. When the chamber pressure was 0.8 Pa, Sm$_2$O$_3$ thin film was deposited under an Ar/O$_2$ (50/10 sccm) atmosphere. To explore the electrical characteristics of Sm$_2$O$_3$/InP MOS capacitors with different stacking positions of Al$_2$O$_3$ passivation layers, a 200-µm-diameter Al electrode was deposited by thermal evaporation, while an aluminum electrode was grown on the back side to form an ohmic contact. Figure 1 demonstrates the schematics of InP-MOS capacitors based on different stacked gate dielectric structures. Sample S1 corresponds to Al$_2$O$_3$ (2 nm)/Sm$_2$O$_3$ (8 nm)/InP, sample S2 corresponds to Al$_2$O$_3$ (2 nm)/Sm$_2$O$_3$ (6 nm)/Al$_2$O$_3$ (2 nm)/InP, and sample S3 corresponds to Sm$_2$O$_3$ (8 nm)/Al$_2$O$_3$ (2 nm)/InP, respectively. By using the ESCALAB 250Xi system, XPS (X-ray photoelectron spectroscopy) measurements were performed at Al Ka (1486.7 eV) to investigate the interfacial chemical properties of the Sm$_2$O$_3$/InP gate stack and the chemical function of the Al$_2$O$_3$ passivation layer. Furthermore, the escape angle used in obtaining the XPS profiles is 50° and the corresponding probing depth is about 1–10 nm. Ultraviolet-visible spectroscopy (Shimadzu, UV-2550) was performed to obtain the samples’ optical band gap. The physical thickness of the above samples was extracted by using spectroscopic ellipsometry measurements (SANCO Inc., Shanghai, China, SC630) with the help of the Cauchy-Urbach model. The Cascade Probe Station was connected to the semiconductor analysis equipment (Agilent B1500A) for capacitance-voltage (C-V), transconductance-voltage (G-V), and leakage current-voltage (I-V) measurements at room temperature. For low temperature (77–227 K) leakage current testing, the Lake Shore Cryotronics Vacuum Probing Station was used.

![Figure 1. Schematics of InP-based MOS capacitors based on different stacked gate dielectrics.](image)

3. Results and Discussion

3.1. XPS Analyses

To evaluate the chemical bonding states of various stacked gate dielectrics, XPS measurements were carried out. Figure 2 displays the In 3d, P 2p, and O 1s XPS spectra of three samples with various stacked gate dielectrics. It can be noted that In 3d spectra can be deconvoluted into four components that represent the InP, InPO$_4$, In(PO$_3$)$_3$, and In$_2$O$_3$, respectively. The relative intensity values of the different components have been extracted and are shown in Figure 3a. For S2 and S3, the contents of In(PO$_3$)$_3$ and In$_2$O$_3$ show a decreasing trend, indicating that the ALD-derived Al$_2$O$_3$ passivation layers prior to Sm$_2$O$_3$ deposition can significantly prohibit the formation of In and P suboxides, which can be attributed to the interface cleaning function of plasma O$_2$ [21]. Compared to S2, the peak areas of InPO$_4$ corresponding to S1 and S3 remain approximate at about 7.89% and 5.20%, which is much lower than that of S2 (19.41%), indicating that double deposition of ALD-derived Al$_2$O$_3$ may accelerate the diffusion of oxygen in the substrate and the formation of indium phosphate. During the secondary deposition of Al$_2$O$_3$, more oxygen vacancies may generate, which can be ascribed to plasma O$_2$ acting as an oxygen source, and promote the oxygen interdiffusion between Al$_2$O$_3$ passivation layers and the InP substrate. In(PO$_3$)$_3$ can react with In to produce InP and InPO$_4$ using the following reaction Equation [22].

$$8\text{In} + 4\text{In(PO}_3\text{)}_3 \rightarrow 3\text{InP} + 9\text{InPO}_4$$  (1)
substrate. In(PO₃)₃ can react with In to produce InP and InPO₄ using the following reaction:

\[ 4\text{Al} + 7\text{O}_2 + 2\text{In(PO}_3\text{)}₃ + 2\text{InP} \rightarrow 4\text{AlPO}_4 + 4\text{InPO}_4 \] (2)

The peak area ratio of In(PO₃)₃ for S₂ and S₃ showed a significant decreasing trend compared to S₁, indicating that Al₂O₃ prior to the deposition of AlPO₄ passivation layers increase the formation of AlPO₄, which is confirmed by the reaction Equation (2). In the plasma O₂ atmosphere, In(PO₃)₃ can react with O₂ to produce AlPO₄ and InPO₄ and leads to the disappearance of In(PO₃)₃. In agreement with the previous In 3d and P 2p spectra, S₁ has the largest In(PO₃)₃ content, leading to a decrease in interfacial quality and deterioration of electrical properties. Meanwhile, AlPO₄ of S₂ is the highest, originating from the second deposition of Al₂O₃. For S₃ sample, the contents of InPO₄, AlPO₄, and In₂O₃ were significantly controlled, indicating that the addition of an ALD-derived Al₂O₃ layer prior to the deposition of Sm₂O₃ gate dielectric could reduce the generation of suboxides and improve the interfacial quality.

Figure 2. (a) In 3d, (b) P 2p, and (c) O 1s XPS spectra for S₁, S₂, and S₃ sample.

Figure 3. Peak area ratio histograms of (a) In 3d, (b) P 2p, and (c) O 1s spectra.

More importantly, sample S₃ shows a tendency to decrease the content of In(PO₃)₃ and AlPO₄ compared to sample S₂, which can give a detailed illustration from the phenomenon of P 2p spectral changes. As shown in Figure 2b, it can be noted that P 2p spectra can be deconvoluted into four components, which represent InP, InPO₄, In(PO₃)₃, and AlPO₄, respectively. No P₂O₅ was detected in all samples, which can be attributed to the fact that gaseous P₂O₅ generated during the deposition can easily diffuse through the defects in the gate dielectric [22]. The peak area ratio of In(PO₃)₃ for S₂ and S₃ showed a significant decreasing trend compared to S₁, indicating that Al₂O₃ prior to the deposition of Sm₂O₃ gate dielectric can inhibit the formation of P-O bound states and improve the interfacial quality. The detection of AlPO₄ in P 2p spectra can be attributed to the reaction equation described below [23].

Based on the mentioned reaction above, it can be inferred that two depositions of Al₂O₃ passivation layers increase the formation of AlPO₄, which is confirmed by the change in peak area ratio shown in Figure 3c. In order to systematically explore the interfacial chemistry of various stacked gate dielectrics, O 1s spectra were investigated and are shown in Figure 2c. O 1s spectra can be deconvoluted into Sm₂O₃, Al₂O₃, InPO₄, In(PO₃)₃, and AlPO₄. According to the reaction Equation (2), in the plasma O₂ atmosphere, In(PO₃)₃ can react with O₂ to produce AlPO₄ and InPO₄ and leads to the disappearance of In(PO₃)₃. In agreement with the previous In 3d and P 2p spectra, S₁ has the largest In(PO₃)₃ content, leading to a decrease in interfacial quality and deterioration of electrical properties. Meanwhile, AlPO₄ of S₂ is the highest, originating from the second deposition of Al₂O₃. For S₃ sample, the contents of InPO₄, AlPO₄, and In₂O₃ were significantly controlled, indicating that the addition of an ALD-derived Al₂O₃ layer prior to the deposition of Sm₂O₃ gate dielectric could reduce the generation of suboxides and improve the interfacial quality.
3.2. Band Alignment Characteristics

To assess the optical characteristics of the three various stacked gate dielectrics, UV-Vis spectroscopy was used to obtain the absorption spectra and the optical bandgap values (Figure 4) of samples S1, S2, and S3 were determined to be 5.49, 5.51, and 5.63 eV, respectively, based on the Tauc relationship [24]. Compared with pure Sm$_2$O$_3$ and pure Al$_2$O$_3$, the band gaps of three various stacked gate dielectrics showed a value balance [25]. Also, this section investigates the valence band maximum (VBM) of various stacked gate dielectrics, as the valence band alignment is crucial for assessing the interface quality. As shown in Figure 5a, the band gap values of InP substrates were derived from XPS measurements, while the valence bands of samples S1, S2, and S3 were deduced from the absorption spectra by linear extrapolation. Based on Kraut’s method [26], we also calculated the valence band shift ($\Delta E_v$) to evaluate the valence band electronic structure of the samples. By using Sm 3d$_{5/2}$ and In 3d core-level spectra, the $\Delta E_v$ of high-k/InP gate stacks was determined based on the following formula:

$$\Delta E_v = (E_{\text{In 3d}} - E_v)_{\text{InP}} - (E_{\text{Sm 3d}} - E_v)_{\text{high-k}} - (E_{\text{In 3d}} - E_{\text{Sm 3d}})_{\text{high-k/InP}}$$

where $E_{\text{In 3d}}$ (InP) and $E_{\text{Sm 3d}}$ (high-k) corresponding to the core-level positions are extracted to be 445.8 and 1084.3 eV. In addition, the $E_v$ (InP) and $E_v$ (high-k) represent the VBM (Valence-Band Maximum) of the bulk materials. The values of $\Delta E_v$ are calculated as 1.87, 1.82, and 1.76 eV, respectively, based on the binding energy difference in the high-k/InP structure. Meanwhile, the value of the conduction band offset ($\Delta E_c$) is obtained by subtracting the extracted $\Delta E_v$ and the band gap of the InP (1.34 eV) from the band gap of dielectric layers [27].

$$\Delta E_c = \Delta E_v - E_g (\text{high-k/InP})$$

As shown in Figure 5b, the $\Delta E_c$ values for the three samples were calculated as 2.28, 2.35, and 2.53 eV. According to previous reports in the literature, $\Delta E_c$ is related with the tunneling leakage current. The higher $\Delta E_c$ indicates that the leakage current of the Sm$_2$O$_3$/Al$_2$O$_3$/InP samples is smaller.

![Figure 4](image-url)  
*Figure 4. The determination of band gaps for sample S1, S2, and S3.*

3.3. Electrical Properties of InP-MOS Capacitors

3.3.1. Capacitance-Voltage Measurements

The frequency dependent capacitance-voltage curves of sample S1, S2, and S3 with double sweep mode are shown in Figure 6a-c. When the frequency increases, all samples show a decreased accumulation capacitance.
Table 1.

| Sample | EOT (nm) | Qox | Nbt |
|--------|----------|-----|------|
| S1     | 2.28 eV  | 1.07 × 10^{10} | 1.78 eV |
| S2     | 2.35 eV  | 1.07 × 10^{10} | 1.74 eV |
| S3     | 2.53 eV  | 1.07 × 10^{10} | 1.71 eV |

Figure 5. (a) Valence band spectra; (b) Schematic band diagram of S1, S2, and S3 sample.

Figure 6. (a–c) Capacitance–voltage (C–V) curves for S1–S3 measured at different frequency (0.6–1 MHz). (d) Capacitance–voltage (C–V) curves for all samples measured at 1 MHz.

Meantime, at high frequency conditions, the series resistance will deviate from the predetermined theoretical value due to the disappearance of the interface trap charge. On the contrary, at low frequencies, when the oxide capacitance (Cox) connects with the space charge capacitance (Csc), the value of the accumulation region increases with the series resistance due to the interface state showing frequency-dependent properties [28–30].

The decrease in the accumulation capacitance can be attributed to the fact that the interfacial traps do not have enough time to respond to the voltage frequency [30]. The maximum accumulation capacitance and minimum hysteresis voltage were observed in the S3 sample, indicating that the Al2O3 passivation layer suppressed the appearance of In and P oxides and the formation of low-K interfacial layers. To evaluate the interface quality, important electrical parameters such as equivalent oxide thickness (EOT), dielectric constant (k), flat band voltage (Vfb), hysteresis voltage (ΔVfb), oxidation charge density (Qt), and boundary trapped oxide charge density (Nbt) were extracted from the test curves, and these data are presented in Table 1. The variation of Vfb depends on the values of oxide capacitance and bulk oxide charge [31]. The k values corresponding to samples S1, S2,
and S3 are calculated to be 12.96, 14.39, and 14.75, which are consistent with the previous investigation [4].

**Table 1.** MOS capacitors electrical parameters obtained from C−V and J−V Curves.

| Sample | EOT (nm) | k | $V_{fb}$ (V) | $\Delta V_{fb}$ (mV) | $Q_{ox}$ (cm$^{-2}$) | $N_{bt}$ (cm$^{-2}$) | J (A/cm$^{-2}$) |
|--------|---------|---|-------------|---------------------|---------------------|---------------------|----------------|
| S1     | 3.01    | 12.96 | 0.25       | 3.44                | $-1.62 \times 10^{12}$ | $-2.46 \times 10^{10}$ | $1.07 \times 10^{-5}$ |
| S2     | 2.71    | 14.39 | 0.21       | 5.16                | $-1.43 \times 10^{12}$ | $-4.11 \times 10^{10}$ | $8.42 \times 10^{-6}$ |
| S3     | 2.65    | 14.75 | 0.19       | 1.55                | $-1.30 \times 10^{12}$ | $-1.26 \times 10^{10}$ | $2.87 \times 10^{-6}$ |

A small $V_{fb}$ of 0.19 V was observed for sample S3. This phenomenon can be explained by the following statement: electrons are easily captured by oxygen vacancies to form negatively charged interstitial oxygen atoms [32] and as fewer oxygen vacancies exist at the interface, the smaller the positive flat voltage required to maintain the band unbent [33]. Also, the hysteresis voltage depends on the boundary trap caused by the intermixing of the high K layer and the interfacial layer [34]. The value of the hysteresis voltage reaches a minimum (1.55 mV) for S3, indicating that the boundary trapping charge becomes weaker after the insertion of Al$_2$O$_3$ between the gate dielectric and the substrate. The $Q_{ox}$ and $N_{bt}$ values were calculated from the obtained $V_{fb}$ and $\Delta V_{fb}$ values by the following equations [35].

$$Q_{ox} = - \frac{C_{max} \left( V_{fb} - \phi_{ms} \right)}{qA}$$  \hspace{1cm} (5)

$$N_{bt} = - \frac{C_{max} \Delta V_{fb}}{qA}$$  \hspace{1cm} (6)

where $\phi_{ms}$ is the contact potential difference between Al electrode and InP substrate, $q$ is the electronic charge, and $A$ is the Al electrode areas. According to Table 1, it can be noticed that S3 has the lowest $Q_{ox}$ and $N_{bt}$, which implies the reduction of interfacial trap defects and the optimization of interfacial properties.

### 3.3.2. Conductivity-Voltage Measurements

Moreover, to quantify the interface defect distribution for all samples, the interface state density ($D_{it}$) has been extracted by the conductivity-voltage measurements with frequencies varying from 100 kHz to 1 MHz. $D_{it}$ is related to the parallel interfacial trap capacitance ($C_{it}$) and parallel conductivity (G). At the same time, $C_{it}$ can be related by the following equation. $C_{it} = qD_{it}$, while the condition is that the position of the energy level does not change $D_{it}$. The basic principle of conductivity measurements is to analyze the losses due to the diversity of charge states at the trap level. Near the Fermi level, the synchronous conductivity occupancy is mobilized by the interfacial traps to produce a regular variation. The maximum loss occurs when the interface trap is resonantly shifted with the applied AC signal ($\omega \tau = 1$). The response time of the characteristic trap changes the frequency, $\tau = 2\pi/\omega$. The capture and emission rates from Shockley-Redhall theory modulate the response time [36]:

$$\tau = \exp\left[\frac{\Delta E/k_B T}{\sigma v_{th} D_{dos}}\right]$$  \hspace{1cm} (7)

where there is an energy difference $\Delta E$ between the trap level $E_T$ and the edge of the majority carrier band, $v_{th}$ is the majority carrier being thermally activated to obtain the average velocity, $D_{dos}$ is the effective density of states of the majority carrier band, $k_B$ is the Boltzmann constant, and $T$ is the temperature [37]. The curves between conductivity (G/\omega) and gate voltage for all samples are shown in Figure 7a–c. The apparent shift of the conductivity peak proves the validity of the Fermi-level shift and confirms the existence of
the Fermi-level deconvolution effect [38]. Assuming that the underlying surface oscillations can be neglected, the value of $D_{it}$ is inferred using the normalized parallel conductivity peak $(G_p/\omega)_{max}$ [39].

$$D_{it} \approx \frac{2.5}{A q} \left( \frac{G_p}{\omega} \right)_{max}$$

(8)

where $A$ is the device area. It is necessary to confirm the transformation law between the band bending potential of the energy location $E_T$ and the trap energy level distribution. Furthermore, the values of $E_T$ can be determined by the frequency of $(G_p/\omega)_{max}$, where Equation (8) is used to calculate $D_{it}$ and to correspond its value to $\Delta E$ [40].

$$\Delta E = (E_C - E_T) = \frac{k_B T}{q} \ln \left( \frac{\sigma_0 D_{dos}}{2 \pi f_{max}} \right)$$

(9)

Figure 7d shows the variation of $D_{it}$ for the three samples. With the increase of $\Delta E$, the value of $D_{it}$ shows an increasing trend. However, S3 possesses a lower density of interfacial states compared to S1 and S2, which indicates that the insertion of an Al$_2$O$_3$ passivation layer between the Sm$_2$O$_3$ gate dielectric and the InP substrate can suppress the formation of In and P suboxides and improve the quality of MOS capacitors.

We compared some of the data obtained from this work with some previously published work. As can be seen in Table 2, the Sm$_2$O$_3$ dielectric has a smaller leakage current density than TiO$_2$ and HfO$_2$, indicating that the Sm$_2$O$_3$ stacked gate dielectric has a larger conduction band shift, resulting in an increased barrier height and thus a reduced leakage current density. The Sm$_2$O$_3$ stacked gate dielectric has the smallest hysteresis value, indicating that the trapped charge in the gate dielectric is not very sensitive to the frequency response of the voltage, and will trap fewer electrons to keep the energy band from being bent, while the device maintains a consistent response to different test voltages in the antipattern region. In the interface state density, it is smaller than HfO$_2$ as the gate dielectric directly deposited in InP, but it seems to be higher than TiO$_2$ gate dielectric, considering the different testing methods, the interface state density of the current work is obtained directly by conductivity method with accuracy, the previous work is by C–V curve, there may be some differences.

Figure 7. Multi-frequency G–V characteristics of InP-based MOS capacitors of (a) S1, (b) S2, and (c) S3. (d) Energy distributions of Dit for S1, S2, and S3.
Table 2. Comparison of different InP MOS capacitor parameters.

| Sample                  | Leakage current density (A/cm²) | ΔVfb (mV) | Dn (cm⁻²·eV⁻¹) | T1/2 (G-V) | Tn (G-V) |
|-------------------------|---------------------------------|-----------|----------------|------------|----------|
| Sm₂O₃/Al₂O₃/InP (This Work) | 2.87 × 10⁻⁶ at 1 V | 14.75 | 1.05 × 10¹¹ | / | / |
| PMA-TiO₂/5-InP [41]     | 1.9 × 10⁻⁷ at 2 V  | 39       | 5 × 10¹¹   | 1.21×10⁻¹ | / |
| TiO₂/5-InP [41]         | 5.01 × 10⁻⁶ at 2 V | 250      | 3.8×10¹² | 1.47×10⁻¹ | / |
| 10 Å Si IPL/51 Å HfO₂/InP [42] | 1.32 × 10⁻³ at 1 V | /         | 2.9×10¹² | / | / |
| 70 Å HfO₂/InP [42]  | 3.94 × 10⁻² at 1 V | /         | /         | / | / |
| HfO₂ (10 nm)/Al₂O₃ (0.2 nm)/InGaAs/InP [43] | 2.4 × 10⁻² | / | / | / | / |

3.3.3. J–V Analyses and Conduction Mechanisms at Room Temperature

Figure 8a shows the leakage current characteristics of all samples measured at room temperature. The leakage current density (J) values for S1, S2, and S3 at 1 V are 1.07 × 10⁻⁵, 8.42 × 10⁻⁶, and 2.87 × 10⁻⁶ A/cm², respectively. It can be seen that S1 has a higher leakage current density, which can be attributed to larger interface traps and the border traps that deteriorate the interface quality and degrade the device performance [44]. For the S3 sample, the minimum leakage current density has been observed, which is due to the higher ΔEc and the suppressed tunneling in the Sm₂O₃/Al₂O₃/InP gate stack [45].

To investigate the leakage current characteristics of various stacked gate dielectrics, we systematically studied three different current conduction mechanisms (CCMs) under substrate injection, as shown in Figure 8b–d. The extracted important electrical parameters are listed in Table 3.

Table 3. Extracted MOS capacitors electrical parameters measured at room temperature.

| Sample | J (A/cm²) | εr | n | εox | q₁ (eV) |
|--------|-----------|----|---|-----|--------|
| S1     | 1.07 × 10⁻⁵ | 4.00 | 2.00 | 11.90 | 0.53  |
| S2     | 8.42 × 10⁻⁶ | 4.96 | 2.23 | 13.01 | 0.54  |
| S3     | 2.87 × 10⁻⁶ | 4.23 | 2.06 | 13.41 | 0.55  |

Figure 8. (a) J–V characteristics measured at room temperature. (b) SE emission, (c) PF emission, and (d) FN tunneling plots for all the samples under substrate injection.
Schottky emission (SE) is a typical type of thermal ionization emission in which charges gain energy to overcome barriers to migration into the dielectric. The standard SE can be described as \[ J_{SE} = A^* T^2 \exp \left[ -\frac{q(q_B - \sqrt{qE/4\pi\epsilon_0\epsilon_r})}{k_B T} \right] \] (10)

\[ A^* = \frac{4\pi q k_B^2 m_{ox}^*}{\hbar^3} = 120 m_{ox}^* m_0 \] (11)

where \( A^* \) is the effective Richardson constant, the free electron mass and the effective mass of electrons in the gate dielectric correspond to \( m_0 \) and \( m_{ox}^* \), \( E \) is the electric field, \( q \phi_B \) is the Schottky barrier height, and \( \epsilon_0 \) and \( \epsilon_r \) represent the vacuum dielectric constant and the optical dielectric constant, respectively \[47\]. It is observed in Figure 8b that at lower electric fields (0.36–0.81 MV/cm), there is a good linear relationship between \( \ln(J/T^2) \) and \( E^{1/2} \) for S1, S2, and S3. The slope of the SE diagram is denoted as \( \sqrt{q^3/4\pi\epsilon_0\epsilon_r k_B T} \). The fitted \( \epsilon_r \) and the refractive index \( n (n = \epsilon_r^{1/2}) \) for S1, S2, and S3 are (4, 2), (4.96, 2.23), and (4.23, 2.06), respectively. All the fits are consistent with the previously reported values \[48\], revealing that CCM (current conduction mechanism) at room temperature is dominated by SE emission in the low electric field region.

The Poole–Frenkel (PF) emission can be ascribed to the thermally excited electrons obtaining sufficient energy to escape from traps into the conduction band of the dielectric at a higher electric field, which can be expressed by the following formula \[49\]:

\[ J_{PF} = AE \exp \left[ -\frac{q(q_I - \sqrt{qE/\pi\epsilon_0\epsilon_{ox}})}{k_B T} \right] \] (12)

where \( A \) represents a constant, the trap energy level of the conduction band corresponds to \( q_I \), and \( \epsilon_{ox} \) represents the dielectric constant. According to the previous theory, \( \ln(J/E) \) should have a good proportionality with \( E^{1/2} \), as shown in Figure 8c. The \( \epsilon_{ox} \) extracted from the slope of the fitted line for all samples was calculated as 11.90, 13.01, and 13.41, which is in agreement with the reported reference \[4\]. It can be concluded that at higher electric fields (1.21–1.69 MV/cm), the PF emission dominates the CCM of all samples. Also, the value of the trap energy level (\( q_I \)) can be extracted based on the intercept point of the fitted curve described as \( \ln B - qI_{q} q_{ox} \). As shown in Figure 8c, the calculated values of \( q_I \) are 0.53, 0.54, and 0.55 eV, corresponding to S1, S2, and S3. S3 has the largest \( q_I \) value in the three samples, indicating that the electrons obtain more energy to cross the trap, leading to present the smallest leakage current density in the S3 sample.

The high-field dependent conduction mechanism is represented by Fowler-Nordheim tunneling, which is manifested by the fact that the insulating layer can be penetrated by electrons, which enter the conduction band of the gate dielectric in a high electric field. The leakage current density is linked to other parameters of Fowler-Nordheim (FN) tunneling and is described by the following Equation \[46\]:

\[ J_{FN} = \frac{q^3 E^2}{16\pi^2 \hbar q_{ox}} \exp \left[ -\frac{4\sqrt{2m^*_T q_B^{3/2}}}{3h q E} \right] \] (13)

where \( q_{ox} \) is oxide barrier height; \( m^*_T \) is the tunneling effective electron mass in the gate oxide film, and the other notations remain unchanged from the previous definitions. Figure 8d shows the curve of \( \ln(J/E^2) \) versus \( 1/E \). The slope of the linear fit for the above samples shows an increase in current with increasing electric field, indicating that at high electric fields (1.47–1.85 MV/cm), all three samples are consistent with the FN tunneling conduction mechanism. Based on the previous analysis, it can be concluded that all samples are dominated by three main conduction mechanisms. In the lower electric fields,
SE emission dominates, however, in the higher electric fields, PF emission dominates together with FN tunneling.

3.3.4. Low Temperature J–V Analyses and Conduction Mechanisms

To investigate the variation of CCMs in Sm$_2$O$_3$/Al$_2$O$_3$/InP MOS capacitor, low temperature (77–227 K) measurements were performed. The leakage current densities of Sm$_2$O$_3$/Al$_2$O$_3$/InP MOS capacitors measured at 1 V were extracted as 4.64 × 10$^{-9}$, 1.48 × 10$^{-8}$, 1.13 × 10$^{-7}$, and 1.02 × 10$^{-6}$ A/cm$^2$, corresponding to the temperature range of 77–227 K, respectively. By observing the leakage current densities at different temperatures, the Sm$_2$O$_3$/Al$_2$O$_3$/InP gate stack exhibits nearly three orders of magnitude lower leakage current density at 77 K than that measured at room temperature, indicating that the low temperature is favorable for the MOS capacitor to exhibit optimized J–V characteristics. Figure 9b–d show the variation of the CCM under substrate injection along with the temperature trend. The extracted important electrical parameters are listed in Table 4. Figure 9b shows the fitted lines for the vertical temperature range suitable for SE emission at lower electric fields (0.49–0.90 MV/cm). The extracted important electrical parameters are listed in Table 4. With increasing temperature, the values of $\epsilon_r$ and $n$ calculated from the slope and intercept are (20.39, 4.52), (18.53, 4.31), (10.40, 3.22), and (6.10, 2.47). It can be noted that at extremely low temperature of 77–177 K, these values are completely different from the theoretical values, indicating that SE emission is not the dominant conduction mechanism at lower temperatures. Figure 9c shows the curves in the temperature range 77–227 K compatible with PF emission at higher electric fields (0.64–1.44 MV/cm). Again, it can be noted that $\phi_b$ and $\epsilon_{ox}$ are not in the expected range of values, indicating that the PF emission is not compatible for all samples at intermediate electric fields of 0.64–1.44 MV/cm. FN tunneling is a potential conduction mechanism because of its dependence on the electric field at low temperatures. Figure 9d shows the fitted line of FN tunneling with a temperature range of 77–227 K at higher electric fields (1.11–1.67 MV/cm), and the established slope indicates that FN tunneling is dominant at low temperatures. In conclusion, the effects of SE emission and PF emission are attenuated due to low temperature, and FN tunneling is used to explain the Sm$_2$O$_3$/Al$_2$O$_3$/InP stacked gate dielectric structure showing low drain current density.

### Table 4.

| Temperature (K) | $J$ (A/cm$^2$) | $t$ (eV) | $\epsilon_r$ | $n$ |
|----------------|--------------|----------|-------------|-----|
| 77             | 4.64 × 10$^{-9}$ | 20.39 | 4.52 |
| 127            | 1.48 × 10$^{-8}$ | 18.53 | 4.31 |
| 177            | 1.13 × 10$^{-7}$ | 10.40 | 3.22 |
| 227            | 1.02 × 10$^{-6}$ | 6.10  | 2.47 |

Figure 9. (a) J–V characteristics measured at low temperature. (b) SE emission, (c) PF emission, and (d) FN tunneling plots for all the samples under substrate injection.
Table 4. S3’s MOS capacitors electrical parameters measured at low temperature.

| T (K) | J (A/cm²) | ε_r | n | ε_ox | \( \varphi_t \) (eV) |
|-------|-----------|-----|---|------|-----------------|
| 77    | 4.64 × 10^{-9} | 20.39 | 4.52 | 164.88 | 0.54 |
| 127   | 1.13 × 10^{-8}  | 18.53 | 4.31 | 108.14 | 0.53 |
| 177   | 1.48 × 10^{-7}  | 10.40 | 3.22 | 42.66  | 0.50 |
| 227   | 6.10 × 10^{-6}  | 2.47  | 31.05 | 0.47  |

Additionally, the integrated dielectric properties in MOS capacitors can be estimated from two important values, including the electron effective mass \( m^*_o \) and the barrier height \( q\varphi_B \) [50]. The intercept of the SE emission fitting curve described as \( \ln \left( \frac{120 m^*_o}{m_0} \right) - \frac{q\varphi_B}{k_BT} \) and the slope of the FN tunneling fitting curve expressed as \( -6.83 \times 10^7 \sqrt{\left( \frac{m^*_T}{m_0} \right) q^3 \varphi_B^3} \) can be calculated together with the above two values. By setting the equation \( m^*_o = m^*_T \), the two key physical quantities \( m^*_o \) and \( q\varphi_B \) of Sm\(_2\)O\(_3\)/Al\(_2\)O\(_3\)/InP MOS capacitor are obtained by applying mathematical analysis, which are calculated as 0.23 \( m_0 \) and 0.95 eV, respectively. Figure 10 shows the determination of the electron effective mass and barrier height for S3 sample. The smaller \( m^*_o \) and the higher \( q\varphi_B \) are beneficial to obtain better electrical properties and optimized interface quality.

4. Conclusions

In this work, we explore in detail the effect of ALD-derived laminated interlayers on the interfacial chemistry and transport properties of sputter-deposited Sm\(_2\)O\(_3\)/InP gate stacks. It has been found that Sm\(_2\)O\(_3\)/Al\(_2\)O\(_3\)/InP gate stack can obviously prevent the diffusion of the substrate diffusion oxide and substantially optimize the electrical properties of MOS capacitors, including a larger dielectric constant of 14.75, a larger accumulation capacitance, and a lower leakage current density of 2.87 \( \times \) 10^{-6} A/cm². Three different stacked gate dielectric structures are also evaluated by means of conductivity of the interfacial density of states. The results show that the Sm\(_2\)O\(_3\)/Al\(_2\)O\(_3\)/InP stacked gate dielectric achieves the lowest interfacial density of states of 1.05 \( \times \) 10^{13} cm\(^{-2}\)eV\(^{-1}\). According to the analysis of CCMs, SE emission is dominant in lower electric fields and higher temperature environments, and PF emission as well as F-N tunneling is dominant in higher electric fields. Meanwhile, FN tunneling is the only dominant mechanism at...
lower temperatures. Also, to evaluate the properties of the whole MOS capacitor in low temperature environment, $m^*_0$ and $q\phi_B$ have been determined by a self-consistent method. These findings are of crucial importance for the future fabrication of high mobility InP-based MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices.

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