Development of a Predictive Process Design kit for 15-nm FinFETs: FreePDK15

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Abstract—FinFETs are predicted to advance semiconductor scaling for sub-20nm devices. In order to support their introduction into research and universities it is crucial to develop an open source predictive process design kit. This paper discusses in detail the design process for such a kit for 15nm FinFET devices, called the FreePDK15. The kit consists of a layer stack with thirteen-metal layers based on hierarchical-scaling used in ASIC architecture, Middle-of-Line local interconnect layers and a set of Front-End-of-Line layers. The physical and geometrical properties of these layers are defined and these properties determine the density and parasitics of the design. The design rules are laid down considering additional guidelines for process variability, challenges involved in FinFET fabrication and a unique set of design rules are developed for critical dimensions. Layout extraction including modified rules for determining the geometrical characteristics of FinFET layouts are implemented and discussed to obtain successful Layout Versus Schematic checks for a set of layouts. Moreover, additional parasitic components of a standard FinFET device are analyzed and the parasitic extraction of sample layouts is performed. These extraction results are then compared and assessed against the validation models.

Index Terms—FreePDK, FinFET 15nm, Process Design Kit, Middle-of-Line layers, DRC, LVS, parasitic extraction.

I. INTRODUCTION

The International Technology Roadmap for Semiconductors (ITRS) forecasts the physical length of the transistors to scale down to 16nm by 2016 [1]. However, the scaling of bulk MOS technology for sub-20nm transistors has faced major problems - these include high leakage power, random dopant fluctuations, Drain-Induced-Barrier-Lowering (DIBL) and other short channel effects. An alternative device called a FinFET has emerged, and it has been demonstrated to advance scaling of semiconductor technology beyond 20-nm processes. FinFETs achieve lower sub-threshold leakage and improved short channel characteristics due to an advanced three dimensional multi-gate geometry. Further, due to an improved gate control and a depleted thin fin structure, they achieve better short channel performance and have lower random dopant fluctuation [2].

The Process design kits (PDKs) for these technologies have already been developed for commercial FinFET processes at the 14 nm. However, these processes are not readily available for the university education purposes due to the critical nature of intellectual property. Additionally, a large investment is required for licensing these processes, which is beyond the scope of universities. Thus, there is an immediate need for development of an open source predictive process design kit to help students gain a detailed understanding of standard design processes. The development of FreePDK15, is thus a step towards achieving a complete predictive process design.

In this paper, the development of an entire metal layer stack based on the ITRS [1] estimates has been presented. The standard FinFET layout is evaluated from the point of view of fabrication and design rules. Additionally, due to limitations of the standard photo-lithography processes, state-of-the-art techniques like double-patterning lithography have been assumed for critical dimensions. Moreover, cut masks and Middle-of-Line (MOL) layers are facilitated to enhance cell density and thus require special design rules. To validate these design rules, layouts of an Inverter, NAND4, and their cascaded cells have been designed and their density is evaluated. A set of the formulae required to accurately identify and calculate the source and drain dimensions of the FinFET layout are presented. Additionally, layout extraction rules for double patterning, metal stitching and gate cut layers are implemented and validated. The parasitic characteristics of a standard FinFET device are studied and the extraction rules for parasitic capacitance and resistance are implemented. The extraction of a set of standard layouts is compared and assessed against first order capacitance and resistance models for metal layers.

This paper discusses the intermediate steps involved in the development of process design kit FreePDK15. In section II, the layers used for the PDK are discussed. In section III, a standard FinFET layout cell is presented and the design rules for these layouts are explained in section IV. Section V discusses steps involved in layout extraction. In section VI parasitic extraction and validation is discussed and the paper is concluded in section VII.

II. FREEPDK15 LAYER STACK

The layer stack for FreePDK15 is developed considering multiple factors, including multi-pattern lithography, metal stitching, dense routing and improvement of contact resistances. The layer stack includes additional layers to accommodate for the three-dimensional nature of the FinFET device and the layer properties follow the predictions from the International Technology Roadmap for Semiconductors 2011 for the 2016 node [3].

The standard cross-section for a FinFET can be seen in Figure 1. The cross-section indicates the use of Middle-Of-Line (MOL) layers along with the standard Back-End-Of-Line (BEOL) layers, and Front-End-Of-Line(FEOL) layers.
A. **BEOL Layers**

The ITRS-2011 tables for the 2016 node predicts use of 13 metal layers. The metal layer stack thus includes 13 layers and follows hierarchical scaling used for standard ASIC architecture [3]. This is further divided into Metal1 layer, Intermediate metal layers, Semi-Global metal layers and Global metal layers.

B. **Middle-of-Line Layers**

The MOL layers act as an interface between FEOL layers like ACT and BEOL layers like Metal1. The MOL layers are implemented for overcoming electrical resistance concerns and the loss of performance between inter-connected layers [4]. Although the concept of MOL layers has been studied in the past the primary inspiration behind their use for FreePDK15 comes from [5]. In [5] 14nm bulk FinFET standard cells have been implemented and the impact of MOL layers, local interconnect layers IM1 and IM2, on cell parasitics is analyzed. MOL layers can be used for connecting internal nets as indicated in Figure 2. Thus these layers help in achieving denser layouts with the provision for connecting internal nets, internal devices as well as providing connection to the power rails. This eliminates the use of Metal1 layer for internal routing and thus that of additional contacts/vias. The function of all MOL layers is listed in Table I.

C. **Double patterning and other techniques**

1) **Double patterning:** Fabrication beyond 20nm involves multiple challenges, primarily from the standpoint of photolithography as the gate pitch is much smaller. It is very difficult to fabricate devices using the standard 193nm Argon Fluoride (ArF) lasers. We also assume that Extreme Ultra-Violet (EUV) lithography is not used in this process because it has not been able to achieve the desired yield for volume production. Instead, double patterning is the technique assumed for FreePDK15, since it achieves greater pitch density compared to standard single-patterning lithography. This is due to superior contrast obtained from exposed and unexposed areas. In principle, the layout is decomposed into two masks, each with different colors each with half the pattern to be printed. In FreePDK15 this is implemented by providing two different colored layers for layers with critical dimensions, like lower metal layers and gate layer.

For example, in FreePDK15, double patterning is assumed for gate layers. GATEA and GATEB are two differently colored gate layers

2) **Cut layers:** In addition to these layers, FreePDK15 also consists of a Gate Cut mask/cut layer called GATEC to remove unwanted features printed by its preceding mask. This helps in printing non-uniform device structures and in overcoming errors due to mask misalignment. It is used to break connectivity between gate layers that are continuous. It is very convenient to form long GATEA/GATEB/GATEAB shapes and then create multiple individual gate shapes by using a grid of GATEC layers, rather than patterning multiple gate shapes at specific places on the wafer.

III. **FINFET LAYOUT ABSTRACTIONS/APPROACHES**

As the FinFET device has three-dimensional thin fin structure, it requires additional fabrication steps compared to a standard planar MOSFET. These differences are primarily due to width quantization and use of MOL Layers.
### TABLE I: MOL layers and their functions

| Layer                                      | Purpose                                                |
|--------------------------------------------|--------------------------------------------------------|
| Active Interconnect Layer-1 (AIL1)         | Connecting individual fins                             |
| Active Interconnect Layer-2 (AIL2)         | Connecting AIL-1 to Metal-1 through a via              |
| Gate Interconnect Layer (GIL)              | Connecting Gate to Metal1                               |

### TABLE II: Standard design rules and their functions

| Rule            | Function                                           |
|-----------------|----------------------------------------------------|
| Minimum width   | Defined by the resolution of the lithographic      |
|                 | process used, prevents open-circuits.              |
| Minimum spacing | Ensure electrical isolation between two shapes     |
| Enclosure       | Prevent overlay errors due to misalignment of      |
|                 | layers                                              |
| Overlap         | Ensure reliability during misalignment of layers    |
| Area            | Ensure adhesion and prevent overlay errors         |

### A. Single FinFET transistor

The layout of a single planar MOS transistor with width $W$ and gate length $L$ is presented in Fig. 3.a. The active layer has a direct contact to Metal1 layer for the planar MOS. But, in the layout of a FinFET transistor, contact is established through local interconnect layers. Figure 3.b shows the representation of the FinFET layout drawn in the design tool, however, due to the quantization of the fin width the device structure on the physical mask looks different and is illustrated in Fig. 3.

In order to ensure process uniformity [6] in sub-20nm transistors “dummy” gates are also printed at the end of the Fins as seen in Figure 4. Moreover, GATEA and GATEB have different patterns for double patterning lithography.

### IV. DESIGN RULE DEVELOPMENT

The design rules define the basic geometric and connectivity restrictions for a device technology and are thus important to its development. They ensure sufficient margins against manufacturing process variability. In addition to that they help the designer in verification of the design before it is sent for fabrication. Violations of these rules can result in undesirable operation of the circuits, thus they are critical to the circuit reliability. Furthermore, these design rules are crucial in defining the density of the integrated circuit as non-optimum design rules would result in wastage of critical design space. Also, with the use of emerging technologies like FinFETs, it is necessary to introduce new sets of design rules to efficiently achieve correct functionality.

Typically, the number of design rules can vary from few hundreds to thousands. The design rules for FreePDK15 are implemented considering the geometric, electrical and lithographic constraints. They incorporate standard minimum width and spacing rules, along with certain restrictive design rules.

#### A. Standard design rules

The standard design rules are listed in Table II.

#### B. Advanced design rules

These rules are specific to FinFET layout and double patterning lithography.

1) **Incremental width rule: Active:** The incremental width rule is introduced due to the discrete nature of the FinFET width. The total width of a FinFET device is defined by the number of fins in the device and thus can only increase in discrete steps. As it can be seen in Figure 5 the active width can only increment in steps of 40nm, which is the pitch of the active layer [7].

2) **Multi-colored design rules:** A distinct feature of device fabrication in the sub-20nm technology is implementation of multi-patterning lithography. In FreePDK15 double patterning lithography (DPL) is assumed. It is thus necessary to use
different rules for different colored metal layers. Figure 6 shows that the required minimum pitch between two similar metal layers, Metal1A layers in this case, is bigger than the minimum required pitch between metal layers of different colors, Metal1A and Metal1B.

3) Restrictive design rules: Restrictive design rules are introduced to maintain the conventional design methodologies with introduction of a new set of restrictions. An example of restrictive design rule is allowing only discrete gate lengths. Another example is restriction of jogs and bends in gate layers as it can result in pinching [8]. However, as this rule causes an increase in the overall area of the layout, it is only implemented for critical dimensions.

C. Design rule validation

The design rules for FreePDK15 are predictive at best and need further validation. A set of layouts were drawn and a design rule check was performed on them for validating these rules [7], [9].

1) Inverter cell: A standard minimum sized FreePDK15 Inverter cell is presented in Figure 7. It uses AIL-2 for connecting the internal nets and power rails. Additionally, GATEA and GATEB are implemented for process uniformity [9], [10].

2) NAND4 cell: A standard NAND4 cell shown in Figure 8 consists of double colored metal1 layer for layout density; the design rules were further validated by running design rule checks.
3) Tiled cells: Tiled Inverter and NAND4 layouts presented in Figure 9 and Figure 10 resp. are also designed for validating the design rules of higher order metal layers.

4) Layout density comparison: The area of minimum sized FinFET inverter is compared with the standard bulk MOS inverter designed using 45nm bulk FreePDK45 process in order to evaluate the layout density of the FinFET process. The layout density in FinFETs does not scale as in bulk MOSFETs. In [12] the layout density for a FinFET design is found to be 1.3 times that for the bulk process at the same process node of 65nm. The primary reason for this can be attributed to the area overhead and width quantization issue in FinFETs.

The area of a standard CMOS bulk technology (FreePDK45) as shown in Figure 11 was compared with the FeePDK Inverter. The area shrink factor of 45nm CMOS inverter to 15nm FinFET inverter was found to be around 1/6.

V. LAYOUT EXTRACTION AND DEVICE RECOGNITION

A crucial element in the development of the process design kit is error-free layout extraction. Layout extraction involves both device recognition and connectivity extraction, and its output is a netlist that contains connectivity information of all the recognized devices. Thus, layout extraction rules for FreePDK15 have been developed for transistor devices NFinFETs and PFinFETs, however, no passive structures are defined yet [13].

A. Device recognition: Bulk MOS vs FinFET

The shift from traditional bulk planar CMOS devices to FinFETs cause problems in device recognition. In contrast to the planar devices, FinFETs have a three dimensional folding of gate layer over the fin which adds to the complexity of creating layouts. However, as indicated in section III the layout of a FinFET device is drawn similar to planar devices with a few exceptions. The comparison of a standard NMOS layout in FreePDK45 and an NFinFET in FreePDK15 is shown in Figure 12. However, this doesn’t account for the multi-fin nature of the FinFETs which results in modification of the formulae used for calculating source and drain dimensions of the FinFET device. Additionally, the gate length is only restricted to 14, 16 and 20 nm. In most cases a single length of 16nm would be enforced, but it is possible that the critical dimensions of all devices may be lengthened to 20 nm or shortened to 14 nm across the entire wafer.

It is also very important to correctly extract the drain and source dimensions i.e. the area, and perimeter, as they define the parasitic source and drain capacitances.

1) Source and Drain dimensions: Planar MOS: The formulae used for estimating the areas \(A_P, A_S\) and the perimeters \(P_D, P_S\) of source and drain for planar devices from [14] are given below.

\[
A_D = A_S = W \times L_{D/S} \tag{1}
\]

\[
P_D = P_S = 2 \times L_{D/S} + W \tag{2}
\]

2) Source and Drain dimensions: FinFET: For bulk FinFET devices, the drain and source area is represented by \(A_{DEJ}\), and \(A_{SEJ}\) respectively, while the perimeter of the drain and source is represented by \(P_{DEJ}\), and \(P_{SEJ}\). The formulae for these parameters account for the number of fins and are as shown in following equations [15].

\[
A_{DEJ} = A_{SEJ} = n_{fin} \times W_{fin} \times L_{fin(D/S)} \tag{3}
\]

\[
P_{DEJ} = P_{SEJ} = 2 \times L_{fin(D/S)} \times n_{fin} + W_{fin} \times n_{fin} \tag{4}
\]

B. Layout Extraction rules

In order to accurately extract a layout, a layout vs schematic (LVS) rule file is defined. Its accuracy depends on the accuracy of the rule file with regards to device definition and extraction, and connectivity extraction. These rules are validated by creating sample layouts and performing LVS checks on sample layouts.

FreePDK15 primarily follows the same LVS rules as defined for bulk MOS technology, however, due to the definition of MOL layers and introduction of cut-layers some of these rules are modified.

C. MOL connectivity rules

Due to the introduction of the MOL layers the device contact rules are modified. As indicated in section III AIL1 acts as the first local interconnect to active while GIL acts as the first local interconnect to Gate. However, AIL2 can act as local interconnect layer to AIL1 as well as GIL. This provides multiple device contact options: AIL1 - AIL2 - M1, GIL - M1 or GIL - AIL2 - M1.

D. Gate Cut rules

Gate cut layer acts as a negative mask and additional rules are defined to identify break in connectivity if a gate cut (GATEC) layer is present. As shown in Figure 13 use of GATEC facilitates denser layouts in case of four tiled inverters by breaking GATE connectivity where required.

E. Double patterning rules

BEOL rules concern the way in which metal layers are connected. The connection of various metal layers is through the alternating via layers, as can be seen in the metal layer stack. For multiple patterned layers, all layers at the same level in the hierarchy, even with different colors, are treated as identical for layout extraction and can be connected to any of the multiple patterned layers of higher or lower levels of the hierarchy using the corresponding via. For example, intermediate metal layer MINT3, MINT3A, MINT3B are considered same and either of them can be connected to either of MINT4, MINT4A or MINT4B using via VINT3. Similarly, they can be connected to either of MINT2, MINT2A or MINT2B using via VINT2.

FreePDK15 has been developed to allow metal stitching, which is a means to connect multiple patterned layers to...
Fig. 12: Comparison of NFinFET and NMOS layout

Fig. 13: GATEC for breaking connectivity between Inverters each other in order to save area. For example, MINT5 can connect to both MINT5A and MINT5B and vice versa. In situations where there are multiple violations to design rules, specifically spacing rules, instead of modifying the layout to increase the area, multiple patterned layers can be used to color different nets and wherever required metal stitching can be used to short two colors (two nets). This is illustrated in Figure 14. The metal stitched layout in figure 14(b) permits a smaller spacing between the ZN, VDD, and VDD_2 nets than would be possible if the ZN net were drawn with one color. The downside of metal-stitching, however, is reduced predictability of wire parasitics and possibly increased chances of a manufacturing defect.

VI. PARASITIC EXTRACTION

Another important component of the process design kit is the capability to correctly extract the interconnect and device parasitics. Parasitic extraction is an essential step in analyzing the performance of the design and parasitic capacitance and resistance of the layout are essentially defined by the following layer characteristics:

1) Geometrical characteristics: Minimum-drawn widths, spacing and layer thickness, via enclosures, and trapezoidal shapes for layers.
2) Electrical properties: Resistivities (or sheet resistances), permittivities for various dielectric layers (dielectric constants), via and contact resistances.

For FreePDK15, the layer definitions and the characteristics are defined in a technology file or .mipt file and the Mentor Graphics’ Calibre xCalibrate and Calibre xRC tools are utilized for parasitic extraction.

A. Layer properties

The values for widths and pitches for various metal layers were derived from the Interconnect tables from ITRS 2011 predictions for the 2016 node [3]. However, ITRS-2011 predictions are more aggressive for metal1 and intermediate metal layer scaling than existing 15 nm processes [5]. Therefore, the minimum width for the metal1 layer, which is often assumed to be roughly 1.5 times the minimum gate length, is assumed to be 28 nm, which is twice that of the minimum gate length. Similarly, the dimensions of the intermediate metal layers are based on this assumption, while the semi-global and global layer dimensions are derived from the ITRS-2011 tables. The
electrical and geometrical characteristics of the layer stack are listed in Table III and Table IV. This stack was chosen to follow [5] while filling in the gaps with materials that provide the approximate resistivity and dielectric constants predicted by ITRS.

### TABLE III: BEOL Layer properties

| Layer Name | Thickness (nm) | Resistivity (ohm-m) | Relative Dielectric Permittivity | Minimum Width (nm) | Minimum Spacing (nm) |
|------------|----------------|---------------------|----------------------------------|-------------------|---------------------|
| MG2        | 260            | 1.0e-08             | 2.5                              | 112               | 112                 |
| VG1        | 260            | 1.0e-08             | 2.5                              | 112               | 112                 |
| MG1        | 260            | 1.0e-08             | 2.5                              | 112               | 112                 |
| VSM05      | 130            | 5.26e-08            | 2.5                              | 56                | 72                  |
| MSM03      | 130            | 5.26e-08            | 2.5                              | 56                | 72                  |
| VSMG4      | 130            | 5.26e-08            | 2.5                              | 56                | 72                  |
| MSAG3      | 130            | 5.26e-08            | 2.5                              | 56                | 72                  |
| MSM03      | 130            | 5.26e-08            | 2.5                              | 56                | 72                  |
| VSMG2      | 130            | 5.26e-08            | 2.5                              | 56                | 72                  |
| VSMG1      | 130            | 5.26e-08            | 2.5                              | 56                | 72                  |
| VINT5      | 60             | 7e-08               | 2.5                              | 28                | 36                  |
| MINT5      | 60             | 7e-08               | 2.5                              | 28                | 36                  |
| VINT4      | 60             | 7e-08               | 2.5                              | 28                | 36                  |
| MINT4      | 60             | 7e-08               | 2.5                              | 28                | 36                  |
| VINT3      | 60             | 7e-08               | 2.5                              | 28                | 36                  |
| MINT3      | 60             | 7e-08               | 2.5                              | 28                | 36                  |
| VINT2      | 60             | 7e-08               | 2.5                              | 28                | 36                  |
| MINT2      | 60             | 7e-08               | 2.5                              | 28                | 36                  |
| VINT1      | 60             | 7e-08               | 2.5                              | 28                | 36                  |
| MINT1      | 60             | 7e-08               | 2.5                              | 28                | 36                  |
| V1         | 60             | 7e-08               | 2.5                              | 28                | 36                  |
| V0         | 60             | 7e-08               | 2.5                              | 28                | 36                  |

The appropriate identification of the metal stack is validated by the output of the XCalibrate’s stack-viewer tool shown in Figure 13 while that for the FEOL and MOL stack is shown in Figure 16.

### B. Capacitance extraction of FinFET

The modeling of internal parasitics is highly complex due to the three-dimensional nature of the FinFET structure. However, the BSIM-CMG (for common multi-gate devices) [16] spice model developed by the BSIM group at UC Berkeley accounts for most of the internal device capacitances. However, the fin rises above the substrate resulting in additional capacitance with the external layers.

Figure 17 illustrates various capacitances associated with a FinFET device. As indicated in Table V, internal device capacitances like $C_{sd}$, $C_{gc\_top}$ are accounted for in the BSIM-CMG [16] spice model. The other capacitances like contact-to-contact, gate to contact, and gate-to-substrate are accurately extracted through parasitic extraction process.

The comparison of this model with the FreePDK15 shows that the capacitances $C_{gf\_top}$, $C_{g1}$, $C_{gc}$ and $C_{gct}$ are extracted by the rules developed for FreePDK15. The capacitance $C_{gf\_top}$ is the fringing capacitance for gate over fins, $C_{g1}$ is the capacitance between GATE/GIL and AIL1. $C_{gct}$ and $C_{cc}$ are again GIL to AIL1 and GIL to M1 (in case of a direct connection) respectively. In FinFET layouts, fins are not represented as thin strips, however, the width of the active area is defined as the sum of fin width, and fin pitch times number of fins as shown in equation 5.

$$W = W_{fin} + (n_{fin} - 1) * Pitch_{fin}$$

Thus, due to the way in which the width is defined, capacitance $C_{g1}$ is not currently modeled in FreePDK15. Additionally, these extracted capacitances have not been validated as that can only be achieved by comparing these results against results from a complex simulation using a 3D field solver. Thus, the current kit only represents an approximate value of the extracted FinFET capacitances.
Fig. 15: BEOL layer stack in Mentor Graphics’ Stack Viewer

Fig. 16: FEOL and MOL layer stacks in Mentor Graphics’ Stack Viewer
TABLE V: FinFET capacitances [17]

| Capacitances                                      | Domain      |
|--------------------------------------------------|-------------|
| Contact to contact \( (C_{cc}) \)                | Extraction  |
| Gate to contact \( (C_{gct}) \)                  | Extraction  |
| Gate to top of fin \( (C_{gf_{top}}) \)          | Extraction  |
| Gate to substrate between fins \( (C_{g1}) \)    | Extraction  |
| Gate to diffusion between fins \( (C_{dif}) \)   | Extraction  |
| Source to drain \( (C_{sd}) \)                   | Spice model |
| Gate to channel \( (C_{g}) \)                    | Spice model |
| Fin to substrate \( (C_{f}) \)                   | Spice model |
| Gate to fin inside channel \( (C_{gc_{top}}, C_{gc_{side}}) \) | Spice model |
| Diffusion to substrate \( (C_{diff}) \)          | Spice model |
C. Validation of parasitic extraction

The parasitic extraction process involves capacitive and resistive extraction of a given layout. The validation process includes design of simple layout and the comparison of their parasitics with first order models and approximations. Capacitance validations include validation of parallel plate capacitance, fringing capacitance and coupling capacitance, while resistance validation includes comparison of sheet resistance.

1) Parallel plate approximation: Capacitance between combination of metal layers of varying dimensions are compared against their parallel plate approximation model. It is found that for larger dimensions extracted capacitance for these metal layers matches the parallel plate capacitance. However, for smaller dimensions, (1um*1um) the difference between the extracted value and the estimated value was as high as 100%. This difference is due to the fringing capacitance which is not included in the parallel plate model, and starts dominating at lower dimensions.

2) Fringing capacitance modification: In order to account for the Fringing capacitance, the parasitic capacitances are compared against the total capacitance values obtained from Sakurai’s [18] and Chang’s [19] approximation. It is found that the estimated parasitics have a significantly lower variation (<10%) even for lower dimensions.

3) Inclusion of coupling capacitance: Coupling capacitance also significantly contributes to the overall parasitic capacitance of the layout, and thus in order to thoroughly validate it, the total extracted capacitance must be compared with the model that accounts for the coupling capacitance. The process of validation thus involves modifying the dimensions and spacing between the metal layers and comparing that against Sakurai’s approximation. It is found that the difference significantly improves (<2%) and remains the same even when separation or lengths are modified.

4) Resistance validation: Simple sheet resistance formula was used to validate resistance extraction. The process involves varying the lengths and widths of different metal layer shapes and observing their effects on the extracts parasitic resistance. Sheet resistance values were calculated from the layer properties table and were used to validate the resistance values. However, in modern chips, the metal layer often is substituted for silicides or mixture of metals with varying quantities is used, which cannot give a simple value of resistivity. Moreover, with effects like skin effect at higher frequencies, resistance varies with distance from surface and hence parasitic resistance validation is kept to this simple sanity check.

The delay analysis was performed for nine-stage FO1 and FO4 Inverters and the average propagation delay for each single stage was calculated. Also, the technology models used for the HSPICE simulations were PTMs 14 nm High Performance nfet and pfet models [20], which are based on the BSIM models for common multi-gate devices [16].

In order to study the impact of additional parasitics on these models the following the propagation delay was computed for each of the following cases

1) Basic circuit based on only the spice models
2) Circuit with source and drain dimensions defined. This enables inclusion of parasitic capacitance in the spice model.
3) Circuit with extracted parasitic netlist for the corresponding circuit layout.

From the delay analysis performed for these cases, it is found that the addition of spice model parasitics as well as inclusion of the parasitic extraction results increases the propagation delay of the circuit. This is in agreement with the estimated behavior of the circuit. Furthermore, another objective of the delay analysis is to evaluate whether the results obtained from the simulations have the same order of magnitude and are within the neighborhood of the propagation delay predicted by ITRS. The simulation result for FO1 Inverter is 1.81 ps, while that predicted by ITRS is 3 ps. Similarly, the result obtained for FO4 Inverter is 4.39 ps, while that predicted by ITRS is 7.18 ps [1]. This indicates that results are close to the predicted values.

VII. CONCLUSIONS

The introduction of integrated circuit design using FinFET devices in university education is currently constrained due to high licensing cost of the commercial design flows. FreePKD15 attempts to remove this constraints by providing an open source predictive process design flow platform wherein circuits for 15 nm FinFET devices can be designed and verified. In this paper, a PDK is described which consists of a layer stack based on existing FinFET designs and ITRS predictions. The design rules encompassing special rules for double patterning lithography, gate cut layers and MOL layers are implemented. Since the geometrical characteristics of a FinFET layout differ from that of a planar MOSFET, the modifications required for correctly extracting the source and drain dimensions (accounting for the number of fins) and FinFET device recognition are executed. Additional rules requiring layout extraction of interconnects because of double patterning and metal stitching are introduced and validated.

A study of the parasitic capacitance components of the FinFET device indicates additional capacitances due to the folding of gate over channel. However, due to the manner in which the current layouts are drawn all the parasitic components have not been accounted for and would require further complex modeling of the 3D gate structure. However, the interconnect capacitances and resistances are validated against standard models and are found to be closer to the estimated values. The complete design flow is proven by
TABLE VI: Propagation delay for Inverter chains

| Circuit       | tp - PTM (ps) | tp - S/D specified (ps) | tp - extracted (ps) |
|---------------|---------------|-------------------------|---------------------|
| FO1 Inverter  | 1.28          | 1.75                    | 1.80                |
| FO4 Inverter  | 3.94          | 4.30                    | 4.39                |

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Running simulations on extracted netlists of FO1 and FO4 Inverters and the propagation delay results of these simulations were found within the vicinity of the results predicted by ITRS-2011 tables for 2016 node.