Different improvement designs of conventional comparator

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Abstract. Comparators play a significant role in the semiconductor industry and have become indispensable in the design of ADC. The delay and energy consumption are two important indicators of the comparator. Many designs have been made to reduce the delay and energy consumption, such as separated gate-biasing cross-coupled transistors for a new latching stage, and pMOS is used to replace nMOS in comparators. This paper analyzes the working principle of the proposed comparators designed for different needs reported on different papers. It compares their simulation results about key data such as delay and energy consumption.

1. Introduction
Comparator is at the heart of most integrated circuits. The delay and energy consumption are two important indicators of the comparator. A lot of works have been done to reduce delay and energy consumption, such as the charge-steering system [1], approaches employing body-driven transistors [2], and supply promotion means [3]. Besides, many other methods were proposed to reduce them after that. The representative common-mode insensitive dynamic comparator is described in [4]. Until now, more methods are proposed [5].

This paper has studied five representative papers and summarized the methods or techniques they used to decrease delay and energy consumption. This key article is well established in detail. Section II depicts the system architecture of the Conventional Dynamic Comparator. The methods and effects used in each paper are discussed in Section III, and Section IV offers the experimental findings of each paper. Lastly, Section V shows the reference.

2. Conventional comparator
Fig.1 demonstrates the traditional dynamic comparator, which is comprised of a preamplifier and a latch stage. At the reset phase, resets the 1st and 2nd stages, respectively, to GND and VDD. Then, clk is on and off to start the regeneration phase. The opportunistic capacitors of the preamplifier's output nodes start to be charged differently in the light of the input differential signal. However, with the development of science and technology, the conventional comparator has been unable to meet the needs of the current circuit, so a variety of innovations is carried out based on it to achieve better performance.
3. A novel design for comparator

3.1. Energy-Efficient Comparator with Dynamic FIA

To present an energy-efficient comparator, Xiyuan Tang et al. proposed two methods focusing on preamplifier improvement design: replacing preamplifier with CMOS DB integration [6]. Another is using a floating inverter with a Reservoir capacitor as the preamplifier. By comparing Gain, Noise, and energy efficiency, it is obvious that the proposed circuit is better.

For CMOS DB Integration Pre-Amplifier, a proposed CMOS DB incorporation model is shown in Fig.2.

V_s- in the base source node raises during integration phase, while the upper one V_s+ decreases. It makes a decrease in overdrive voltage of input pairs of nMOS and pMOS. The preamplifier (Gm) transconductance is the sum of the transconduction of the nMOS and the pMOS input couples. As demonstrated in Fig.3, as a result, the integration increases the average G_m/ID of the preamplifier by more than 2.5 times, and energy efficiency also experiences an increase. And its input common-voltage variations are indicated in Fig.4(a).
For Floating Inverter Preamplifier with Reservoir Capacitor, to decrease the size of capacitance and to provide an isolated voltage domain for preamplifier, this article merges the two tail $C_{TAIL}$ into single floating reservoir capacitor $C_{RES}$ and this operation shown in Fig.5 [7].

![Fig.3 Gm/ID comparison](image)

This new design guarantees a persistent output common-mode potential. It can make the input-output current of $C_{RES}$ keep until the isolated voltage will be automatically changed with the variation of input common-mode potential. And its input common-voltage fluctuation is displayed in Fig.4(b).

![Fig.4 Input common-mode voltage variation (a) Pre-amplifier behavior (b) FIA behavior](image)

Referred to noise analysis in paper [8] is Noise analysis, the input-referred noise of the traditional nMOS combination pre-amplifier can be expressed as

$$
\sigma^2_{in,sa}(T_{INT}) = \frac{2nkT}{V_{THN} \cdot C_X} \frac{I_D}{g_m}
$$

(1)

Where $T_{INT}$ is the integration phase.

The input-referred noise of DB comparator at the end of $T_{INT}$ is

$$
\sigma^2_{in,db}(T_{INT}) = \frac{2nkT}{C_p \cdot \Delta V_{X,CM}(T_{INT})} \frac{I_D}{g_m}
$$

(2)

And it of FIA is calculated as
A new variate is built to weigh energy consumption and noise, a figure of merit, which is briefly written as FoM. FoM is characterized as the creation of expenditure and the input-referred noise power.

\[
\text{FoM} = \text{Energy} \cdot (\text{Noise Power})
\]

So, it is obvious that the lower FoM, the higher the comparator efficiency. And energy efficiency of the comparator can be estimated by that of the pre-amplifier [9].

FoM of DB integration is

\[
\text{FoM}_{\text{DB}} = 4nkT \cdot V_{DD} \cdot \frac{I_D}{g_m}
\]

FoM of FIA is

\[
\text{FoM}_{\text{FIA}} = 4nkT \cdot V_{DD} \cdot \frac{I_D}{G_m}
\]

Comparing the noise, FoM, and inputting common voltage variations in Fig.4(a) and (b), it is no doubt that FIA provides higher integration gain, and it also can release the input-referred noise of latch. As a result, the FIA-based comparator is the best choice.

By observing Fig. 6, it is suitable to find a CRES value that can guarantee a smaller FoM and a smaller noise. So a 2-pF CRES ensures energy efficiency.

![Fig.6 Simulation of (a) CLK-Q gap with a 1-mV differential input and (b) Energy effectiveness of the suggested comparator vs. CRES value](image)

![Fig.7 (a) Modeled CLK-Q interval vs. input common-mode potential. (b) Assessed input-referred noise vs. input common-mode potential.](image)
In Fig. 7(a), obviously, with the change of comparator input, the delay of the FIA comparator hardly changes, while the Strong Arm latch changes significantly. It attested its callousness to input common-mode variation.

In Fig. 7(b), it is easy to find that for the suggested FIA comparator, the input noise basically keeps in still, while for SA latch, it changes obviously with comparator input.

(a) Fig. 8 Quantified accumulative likelihood density distribution and obey Gaussian distribution (a) SA latch comparator (b) The anticipated comparator

By comparing the measured rms of the proposed comparator and SA latch comparator, the proposed FIA comparator has smaller rms, so it is more stable (Fig. 8).

Fig. 9 shows the relationship between input-referred offset investigation and the input common-mode potential. It’s quite clear that the proposed one diminishes the deviation by larger than 5 times.

Fig. 10 Determined energy expenditure vs. input potential for the SA latch and suggested comparator.
Because of the insensitivity of the input common-mode, the proposed comparator has four times less power than the SA latch [10].

3.2. A low-noise PD-based comparator
Chin-Yu Lin et al. proposed a new low-noise phase-detector-base comparator, which enables the reduction of the thermal-induced noise and the possibility of meta stability.

![Fig.11](a) Single-stage comparator (b) Double-tailed comparator

Compared with the traditional single-stage comparator [11] exhibited in Fig.11(a), one double-tailed comparator in Fig.11(b) improves speed, noise, and offset. So, based on these, the PD-based comparator is proposed in Fig.12.

![Fig.12](Configuration of comparator in line with PD)

This new comparator consists of 2 forward-end dynamical comparators and a back-end phase sensor, and the front stage is made by 2 traditional comparators, demonstrated in Fig.13.

![Fig.13](a) Illustration of a comparator employed in front-end (b) The dynamic phase detector (PD)
Unlike traditional ones, the proposed comparator can guarantee a shorter delay, which means less occurrence of metastability (Fig.14).

\[ J_{\text{out,1-stg}} = \frac{32kT\gamma \tau_{R1}^2 \tau_{s1}}{3C_{z1}V_{OS}^2(t_1-t_0)} + \frac{32kT\gamma \tau_{R1}^2 \tau_{s2}}{3C_{z1}V_{OS}^2(t_1-t_0)^3} + \frac{48kT\gamma \tau_{R1}^2 \tau_{s1}^2}{C_{out}V_{OS}^2(t_1-t_0)} + \frac{32kT\gamma \tau_{R1}^2 \tau_{s1}^2}{C_{z1}V_{OS}^2(t_1-t_0)^2} \]  

For the PD input-referred noise,

\[ J_{\text{in,2-stg}} = \frac{16kT\gamma \Delta t_s}{g_{m31}V_{OV}} + \frac{8kT\gamma C_{out}}{g_{m31}^2V_{OV}} + \frac{16kT\gamma C_{out}}{g_{m31}^2V_{OV}} \]  

So, it is easy to say that the noise which is caused by PD is indeed reduced than the front-end circuit, so the PD noise can be ignored while considering the input-referred noise (Fig.15).

As a result, through the above, it is obvious that the anticipated comparator corresponds to a lower noise level than the conventional one.
To consider the key factor of speed, the most important is the propagation delay. The delay of the front-end comparator is

$$t_{d,1-stg} = \frac{2C_{out}V_{thp}}{I_{MNT}} + \tau_{R1}\ln\left(\frac{V_{mid}\tau_{11}\tau_{12}I_{MNT}^2}{2C_{out}V_{thp}^2(\Delta V + V_{OS})}\right)$$  \hspace{0.5cm} (8)$$

And the delay of PD is

$$t_{d,2-stg} = \frac{2C_{out}V_{thp}}{g_{m31}V_{OV}} + \tau_{R2}\ln\left(\frac{2C_{out}V_{mid}}{(g_{m31}V_{OV})(G_{VT}\Delta V)}\right)$$  \hspace{0.5cm} (9)$$

Based on the equations above and Fig.16, PD can regenerate fast with a small input, and the proposed comparator is improved in the speed within a bounded input range [13].

3.2.2. Measurement result

In Fig.17, the proposed circuit obtains smaller noise.

And from Fig.18(a), the noise perturbation causes little effect on the proposed one.

Fig.16 Modeled and projected delays for comparators

Fig.17 Assessed input-referred noise for comparators
Fig. 18 (a) Determined delay concerning the input potential difference (b) Measured delay in relation to the common-mode voltages

Fig. 18(b) shows the PD-based comparator’s relative delay in different common-mode-voltage compared with the normal method. This one has a more stable delay.

3.3. Dynamic comparator with a transconductance improved latching stage

The transistors in red in Fig. 19 are the optimization part of the proposed design. The delay of the proposed dynamic comparator is expressed as:

$$t_{delay} = \frac{V_{THN} C_{OUT}}{g_{m,eff}} \cdot 2\mu_p C_OX \frac{W}{L} + \frac{C_{OUT}}{g_{m,eff}} \cdot \ln \frac{V_{DD}}{\Delta V_0}$$  \hspace{1cm} (10)

The effective total transconductance of the latch is given by

$$g_{m,eff} = g_{mm} + g_{mp} = \mu_n C_{OX} \left( \frac{W}{L} \right) V_{dnm} + \mu_p C_{OX} \left( \frac{W}{L} \right) |V_{dep}|$$  \hspace{1cm} (11)

Eq.(10) shows that $g_{m,eff}$ is a highly useful means to decrease the delay. The bigger the $g_{m,eff}$ is, the smaller the delay is. And Eq.(11) shows the width of switches $M_2$ and $M_3$ determine the magnitude of $g_{m,eff}$. According to Fig.20, when the width of $M_2$ and $M_3$ is larger than 1 μm, boosting the width cannot help to reduce the delay significantly, unfortunately, with great power expenditure. Therefore, the proposed design sets the width of $M_2$ and $M_3$ to 1 μm.
Fig. 20 Modeled delay and power expenditure of the suggested comparator vs. the width of $M_2$ and $M_3$.

Fig. 21 (a) Post-layout simulated delay and (b) energy consumption versus $V_{cm}$.

Fig. 21(a) and Fig. 21(b) show that the delay and energy consumption of the suggested design is all the better than the design before. In the application, we may choose $V_{cm}$ between 0.9V and 1.1V. Because in this range, the delay is small, and the power consumption is not too high.

Fig. 22 (a) Post-layout simulated delay and (b) Energy consumption versus $V_{DD}$. 
Fig. 22(a) and Fig. 22(b) show that when \( V_{id} = 50 \text{ mV} \) and \( V_{cm} = V_{DD} - 0.1 \text{ V} \), the delay and energy consumption of the suggested design is the least in different \( V_{DD} \). In the application, we choose 1.2V as \( V_{DD} \). Because at this \( V_{DD} \), the delay is small enough, and the energy consumption is not too big.

Fig. 23 Post-layout simulated delay versus \( V_{id} \) Fig. 24 Delay and energy consumption versus \( V_{cm} \)

Fig. 24 shows the evaluated and modeled delay and energy consumption at 2 GHz and 0.1 V. Their trends are roughly the same, so the test results agree with the simulation results. The numerical difference may be due to measuring instrument accuracy and circuit loss. The measurement energy consumption of the proposed design at 2GHz operating frequency and 1.2V supply voltage is 112.5fJ.

3.4. Double-Tail comparator

Samaneh Babayan-Mashadi designs a new dynamic comparator to reduce energy consumption and delay time significantly [14].

When \( CLK = 0 \), \( M_{tail1} \), and \( M_{tail2} \) are off during the reset phase, \( M_3 \) and \( M_4 \) pull \( fn \) and \( fp \) nodes to \( V_{DD} \). Consequently, transistors \( M_{c1} \) and \( M_{c2} \) are cut-off. \( M_{R1} \) and \( M_{R2} \) reset both latch outputs to the ground.

During the comparison phase, when \( CLK = V_{DD} \), \( M_{tail1} \), and \( M_{tail2} \) are on. Transistor \( M_1 \) and \( M_4 \) turn off. At the beginning of this phase, the control transistor \( M_{c1} \) and \( M_{c2} \) are still off. \( fn \) and \( fp \) start to drop with different rates according to input potentials. Supposing \( V_{INP} > V_{INN} \), \( fn \) drops faster than \( fp \). The \( M_{c1} \) will always pull the \( fp \) node back to the \( V_{DD} \) and allow \( fn \) to be discharged entirely.

Therefore, by time passing \( \Delta V_{fn}/fp \) increases in an exponential. According to Eq.(12) and Eq.(13), \( V_0 \) and \( gm \) are proportional to \( \Delta V_{fn}/fp \). However, according to Eq.(15), \( V_0 \) and \( gm \) are inversely proportional to delay. In this way, delays will be significantly reduced. Besides, the energy per comparison consumption will be reduced. Because in the proposed design, only node \( (fn/fp) \) has to be charged. To overcome stationary energy expenditure, 2 nMOS switches \( M_{sw1} \) and \( M_{sw2} \), are applied below the input transistors, shown in Fig. 25(b).

Similar to the \( \Delta V_0 \) equation of doubled-tail structure, in this comparator, we have:

\[
\Delta V_0 = V_{T_h} \frac{\Delta I_{latch}}{I_{B1}} \approx 2V_{T_h} \frac{\Delta I_{latch}}{I_{tail2}} = 2V_{T_h} \frac{gmR_{1,2}}{I_{tail2}} \Delta V_{fn/fp} \tag{12}
\]

\( \Delta V_{fn/fp} \) can be calculated by:

\[
\Delta V_{fn/fp} = \Delta V_{fn(p)0} \exp \left( (A_V - 1) t/\tau \right) \tag{13}
\]

\( \Delta V_{fn(p)0} \) is obtained from:

\[
\Delta V_{fn(p)0} = 2V_{THp} \left| \frac{gm_{1,2}}{I_{tail1}} \Delta V_{fn} \right| \tag{14}
\]

The overall delay of the proposed comparator is achieved from:
\[ t_{\text{delay}} = 2 \frac{V_{\text{Thn}} C_{\text{Lout}}}{I_{\text{tail2}}} + \frac{C_{\text{Lout}}}{g_{m,\text{eff}} + g_{m1,2}} \cdot \frac{\ln \left( \frac{V_{DD}/2}{\Delta V_0} \right)}{\ln \left( \frac{V_{DD}/2}{g_{m,\text{eff}} + g_{m1,2}} \cdot \frac{V_{DD}/2}{g_{m,\text{eff}} + g_{m1,2}} \cdot \exp \left( \frac{G_{m,\text{eff}} \cdot V_{\text{In}}}{C_{L,PW}} \right) \right) + \frac{C_{\text{Lout}}}{g_{m,\text{eff}} + g_{m1,2}} \cdot \ln \left( \frac{4V_{\text{Thn}}/V_{Thp}}{g_{m1,2} \cdot V_{\text{Thp}} / I_{\text{tail3}}} \cdot \frac{g_{m1,2} \cdot V_{\text{En}} / I_{\text{tail1}}} \right) \]

Fig. 25 Scheme of the intended dynamic comparator (a) Main idea (b) Final structure

Fig. 26 Peak input voltage error due to kickback noise
Fig. 27 (a) Post-layout modeled delay and (b) Energy per conversion as a function of the supply potential.

Fig. 28 (a) Post layout modeled delay and (b) Energy per conversion as a function of input common-mode potential.

Fig. 27 reveals the simulated delay and energy consumption of three different comparators in different supply voltages. It is obvious that the proposed comparator has the minimum delay and energy. Besides, when the supply voltage is more than 1V, the delay is nearly stable, but the energy consumption increase quickly. So in practical application, it is reasonable to choose 1V as the supply voltage.

Fig. 28 shows the delay and energy expenditure of three unique comparators in different $V_{\text{cm}}$. It is obvious that the suggested comparator has the minimum delay and energy. Besides, when $V_{\text{cm}}$ is more than 0.8V, the delay of the suggested comparator is nearly stable, but the energy will increase. So in practical application, it is reasonable to choose 0.8V as the $V_{\text{cm}}$.

This proposed design is simulated in 180 nm CMOS technology. The delay of this comparator is 550 ps, and the energy expenditure of it is 329 µW at 1.2 V and 0.5 GHz.

3.5. A Low-Power High-Speed Comparator

This is a new design that pMOS transistors use at the input of the preamplifier and the latch stage of the comparator proposed by Ata Khorami, which achieves the optimum delay for preamplification and prevent excess energy expenditure [15].

The schematic is displayed in Fig. 26(a).
Fig. 30 Simplified circuit diagram of the latch right

For the suggested comparator, the latch delay is

\[ t_{latch} = \tau_{inv} \times \ln \left( \frac{V_{DD} - V_{GND}}{V_{id}} \right) + \frac{K_{latch}}{(V_{DD} - V_{cm} - V_{th})^2} \]  \hspace{1cm} (16)

\( V_{cm} \) is the input common-mode potential, and \( V_{id} \) is the differential voltage of the latch coming from the preamplifier stage \([16]\).

Fig. 31 shows the model results and analytical derivations about the delay of the suggested comparator versus input \( V_{cm} \) and \( V_{id} \).

Fig. 31 (a) Delay of the suggested comparator vs. input \( V_{cm} \) (b) Delay of the suggested comparator vs. input \( V_{id} \)

With the increase of \( V_{cm} \), although the variation of delay fluctuated, the overall trend is increasing. And with the increase of \( V_{id} \), the delay velocity decreases.

Fig. 32 shows the simulation results and analytical derivations about the offset voltage of the proposed comparator versus input \( V_{cm} \). With the increase of \( V_{cm} \), the offset voltage is basically stable.

Fig. 32 Scheme and analytical model results of offset voltage vs. \( V_{cm} \)
Fig. 33 The offset potential of the suggested comparator versus (a) Delay and (b) Power (at 500 MHz) derived from various delay values.

Fig. 33 shows the offset potential of the suggested comparator vs. tamp and vs. energy expenditure derived from various values of tamp. Evidently, tamp = 150 ps is the optimum design point.

Fig. 34 Offset potential vs. energy expenditure for the suggested and the traditional comparators.

Fig. 35 (a) Delay versus $V_{id}$ considering $V_{cm} = 0.7, 1.1$ for nMOS input and pMOS input comparators (b) Delay vs. $V_{cm}$ given $V_{id} = 1$ mV.

Fig. 36 (a) energy expenditure of comparators vs. input $V_{cm}$ (b) energy expenditure of the suggested comparator vs. tamp, $V_{cm} = 1.1$ V.
Fig. 36(a) introduces the energy expenditure vs. \( V_{cm} \) at the clock frequency of 500 MHz. Neglecting the power consumption of the latch, the total power consumption is calculated as

\[
\text{Power} = \frac{1}{T} \int_0^{T - T_{\text{clk}}/2} v(t) \cdot i(t) \, dt + P_{\text{latch}}
\]

\[
= \frac{1}{T} \int_0^{t_{\text{amp}}} V_{DD} \cdot (I_1 + I_2) \, dt + P_{\text{latch}} \approx \frac{t_{\text{amp}}}{T} V_{DD} \times I_{MS}
\]  

(17)

Fig. 36(b) presents the power consumption versus delay for \( V_{cm} = 1.1 \) V. The conventional power stays pretty much the same, because the preamplification delay is fixed to \( T_{\text{clk}}/2 \). But in the proposed comparator, the power consumption has a linear connection with \( t_{\text{amp}} \).

Fig. 37(a) shows the power versus input \( V_{cm} \), at \( f = 500 \) MHz and \( V_{id} = 0.1 \) V, the average power consumption is less than 250 \( \mu \)W for 500-MHz clock frequency. Fig. 37(b) shows the power versus clock frequency at \( V_{cm} = 1.1 \) V. With the increase of frequency, the power also increases. And the proposed comparators offer a low power consumption in different frequencies. Fig. 37(c) shows the delay versus input \( V_{cm} \), at \( V_{cm} = 0.1 \) V and \( V_{id} = 0.1 \) V.

\begin{align*}
V_{\text{out}} &= \frac{V_{G1} + V_{G2}}{2} = \frac{I \times \frac{t_{\text{amp}}}{C}}{I + \alpha \frac{t_{\text{amp}}}{C}}, \quad I = I_1 + I_2
\end{align*}

\[
V_{\text{out}} = \frac{\Delta t \times \frac{t_{\text{amp}}}{C}}{1 - \alpha \frac{t_{\text{amp}}}{C}}, \quad \Delta t = I_1 - I_2.
\]  

(18)

TABLE 1 shows these improvements clearly. From TABLE 1, it is clear that every comparator has its own improvement,
4. Conclusion

This review totally focuses on comparator design. In most of the selected review papers, they have made some changes to the traditional structure and improved the performance. Some replace its pre-amplifier by FIA, which decreases its energy consumption. Some use a transconductance-enhanced latching stage to attain low power high-speed comparator, and some add a special local clock to satisfy low voltage and power.

The challenge nowadays is that how to design a comparator achieve all these improvements at the same time.

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