**Effect of atomic layer deposited ultra-thin SiO₂ layer on vapour-liquid-solid (VLS) grown high dielectric TiO₂ film for Si-based MOS device applications**

## 1 | INTRODUCTION

There has been continuous development of Si-based metal-oxide semiconductor field effect transistors (MOSFETs) in the last few decades, which has been possible due to the availability of natural gate oxide (SiO₂) and its suitable mechanical, elastic and electronic properties. Utilizing benefits of Si with advance technologies, there has been a continuous scaling down in the successive nodes of complementary-metal-oxide-semiconductor (CMOS) technology. Due to such aggressive scaling, the thickness of gate dielectric has been reduced to a few atomic layers, consequently increasing the leakage current to unacceptable level. However the constant demand for smaller device with an increase of data rate for mobile computing requires a continuous improvement of low power devices with high speed of operation. Thus, continuous efforts are made to replace SiO₂ as gate dielectric by high-k dielectrics such as, TiO₂, Al₂O₃, Ti₃O₅, La₂O₃, ZrO₂, Y₂O₃, HfO₂ etc. thereby, increasing the physical oxide thickness. Higher oxide thickness helps to reduce static power dissipation by reducing the gate leakage current which provides better control over the gate [1–3].

TiO₂ as a gate dielectric has huge potential for its high dielectric constant of 10–100, high resistivity of 10¹⁹–10²⁴ ohm m, thermal stability, and abundance in nature due to its presence in several kinds of rocks and mineral. It also presents a superior Si–dielectric interface state density, during the growth process at high temperature it can be segregated and produce SiO₂ and metallic oxide. To get rid of this problem a thin layer of SiO₂ is deposited over Si, so that the performance of the device can be improved with the same interface quality [1–7].

TiO₂ is found in three crystalline forms: anatase, rutile and brookite. Among them brookite is the least explored crystalline form [8]. To the best of our knowledge till date no work is reported on electrical characterization and reliability study for the brookite TiO₂ gate dielectric MOS structure on Si substrate with atomic layer deposited (ALD) amorphous SiO₂ passivation layer by employing vapour-liquid-solid (VLS) process. So in the present work, the mentioned study has been done on the least studied VLS grown brookite TiO₂ ultra-thin film gate dielectric MOS structure, with and without ALD SiO₂ passivation layer. The film quality and structural properties of the as-grown TiO₂ films are studied by using scanning electron microscope (SEM) images and X-ray diffraction (XRD) measurements, respectively. The electrical characterization of the TiO₂/SiO₂/Si and TiO₂/Si MOS capacitors is performed by the C–V and I–V measurements.

## 2 | EXPERIMENTAL DETAILS

Thin films of ≈13 nm TiO₂ are grown on SiO₂/Si and Si substrates by employing VLS technique. Prior to growth, p-type Si substrate is cleaned by standard (RCA) cleaning process. A thin layer of metal catalyst (in this case, Gold (Au)) of ≈7 nm, is deposited on the SiO₂/Si and Si substrate by sputtering technique. After Au coating, samples are placed in a dual-zone furnace. The sample is kept at 600 °C to achieve supersaturation of TiO₂ vapour and hence rise in the deposited oxide film thickness will also occur. So, ≈7 nm Au coating is adequate to grow ≈13 nm TiO₂ thin film. Mixture of TiO₂ and graphite, proportionate to their atomic weights, is kept in the other zone of the furnace at a comparatively higher temperature in order to form vapour, so that it can be carried by Argon (Ar) flow at 183.9 Torr, and get absorbed by the liquid alloy and the alloy gets supersaturated. The furnace is maintained at the growth temperature for 30 min, and then cooled down slowly. The growth process is stimulated by the components of the vapour which form precipitate at the liquid–solid interface. Aluminum (Al) gate electrode is deposited by thermal evaporation method on TiO₂ film. Electrical characterization of the sample is done with Keithley–4200 SCS parameter analyzer. Structural analysis and crystallographic orientation of the
RESULTS AND DISCUSSION

SEM images of the as-grown ultra-thin TiO₂ film tilted at ≈75° are shown in Figure 1, where in Figure 1(a) SEM image of the sample with SiO₂ passivation layer in between Si and TiO₂ and in Figure 1(b) SEM image of the TiO₂/Si are shown. SEM images reveal superior quality TiO₂ films grown on SiO₂/Si and Si substrate by employing VLS technique.

XRD patterns shown in Figure 2 reveal crystalline TiO₂ films for both as deposited samples. The orthorhombic (brookite) TiO₂ films with [130], [160] and [212] planes, can be seen from peaks in Figure 2 at 2θ = 33.5°, 61.7° and 75.7° respectively, which are consistent with the JCPDS card no. 82-1123 [9]. So, it can be concluded from the dominant peaks in XRD pattern that brookite TiO₂ films are formed on both the substrates. A wide peak is also observed from Figure 2(a), which is due to the presence of ALD amorphous SiO₂ [10].

Average crystallite size (D) is measured by using Debye–Scherrer’s formula [3]:

\[ D = \frac{k\lambda}{\beta \cos\theta} \]  

where, \( k \approx 0.9 \) is a constant, \( \lambda \) (0.015406) is the X-ray wavelength, \( \beta \) is the FWHM (full width at half maximum) and \( \theta \) is diffraction angle. Crystallite size calculated by using Equation (1) is listed in Table 1. Report suggests that brookite with crystallite size greater than 11 nm is more stable compared to anatase [8]. In comparison to other reported crystallite size of brookite TiO₂ of ≈50 nm [11] and 3.4–19.8 nm [12], crystallite size achieved in the present work is remarkably high, which suggests uniform film.

The SE measurement has been used to measure the thickness for both the samples. The relevant model structures are considered to be Air/TiO₂/SiO₂/Si and Air/TiO₂/Si. The optical constants of air and the wavelength of incident light have been considered to remain constant in the fitting process. Thickness of TiO₂ films for samples with and without SiO₂ is found to be 12.51 and 12.75 nm, respectively.

A useful technique to understand the interface quality is C–V characterization. So, the C–V measurement has been performed at 100 kHz for TiO₂/SiO₂/Si and TiO₂/Si MOS capacitors and plotted in Figure 3 for both as grown samples. Vertical (black) arrows in Figure 3(a,b) indicate forward and reverse sweep direction. C–V characteristics for TiO₂/Si sample (Figure 3(b)) is found to be more stretched through the voltage axis compared to the TiO₂/SiO₂/Si sample. Therefore it can be observed that the occurrence of donor and acceptor like interface traps, existing in a section of the semiconductor band gap is more for the TiO₂/Si sample [1]. Thus, introducing SiO₂ layer in between TiO₂ and Si improves the surface quality by reducing the interface traps (Figure 3(a)). The existence of interface traps and/or mobile charges within the oxide layer is also confirmed by the hysteresis voltage. It has been observed that incorporation of SiO₂ passivation layer reduces the hysteresis voltage significantly (as shown in Figure 3(a,b) with horizontal (blue) arrows, thereby improving the interface quality. TiO₂/SiO₂/Si sample exhibits a much smaller hysteresis voltage of 0.34 V in comparison with TiO₂/Si sample which shows comparatively higher hysteresis voltage of 1.32 V. Dielectric constant calculated from accumulation capacitance for the TiO₂/SiO₂/Si and TiO₂/Si sample at 100 KHz are found to be 44.5 and 35.8, respectively. The larger dielectric constant for the former sample may be due to the suppression of the lossy dielectric layer in between TiO₂ film and Si substrate by incorporating SiO₂ passivation layer. Dielectric constant achieved in the present work is

| Sample       | 2θ (°) | Crystallite size (nm) |
|--------------|-------|-----------------------|
| TiO₂/SiO₂/Si | 33.5  | 61                    |
|              | 61.7  | 89                    |
|              | 75.7  | 93                    |
| TiO₂/Si      | 33.5  | 56                    |
|              | 61.7  | 89                    |
|              | 75.7  | 64                    |

Where: D (nm)
comparable to other reported data of 14–65 [1], 24–33 [3], 31–78 [13] and 32–60 [14]. The C–V characteristics are simulated by using a device simulator, SILVACO and are shown in Figure 3(c,d). The Shockley–Read–Hall (SRH) and CVT mobility models along with interface trap modelling have been included in the simulation. The simulated characteristics match well with the experimental data. It is to be noted that, the thickness and dielectric constant of the dielectric layer, and the interface trap density from simulation are in agreement with the experimentally extracted values.

Owing to the interface traps formed at the interface of the substrate and oxide, frequency dispersion is observed for both the samples in the C–V characteristics, and is shown in Figure 3(e,f). Frequency dispersion for TiO2/SiO2/Si sample (Figure 3(e)) is observed to be very small in comparison to the former sample has lower interface traps [1]. The capacitance density for both the samples are calculated using conventional formulas and are listed in Table 2 along with hysteresis characteristics, and is shown in Figure 4–c). The Shockley–Read–Hall (SRH) and CVT mobility models along with interface trap modelling have been included in the simulation. The simulated characteristics match well with the experimental data. It is to be noted that, the thickness and dielectric constant of the dielectric layer, and the interface trap density from simulation are in agreement with the experimentally extracted values.

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Mostly Fowler–Nordheim (FN) tunnelling, Poole–Frenkel (PF) tunnelling and Schottky emission are the transport mechanisms found through the oxide layers [10]. To know the dominant transport mechanism of TiO2/SiO2/Si sample, the leakage current is plotted and it shows a linear fit with FN tunnelling mechanism at low field (Figure 4(c)) and PF tunnelling at high field (Figure 4(b)), whereas dominant transport mechanism of the second sample (TiO2/Si) is a linear fit with Schottky emission at the low field (Figure 4(d)) and PF tunnelling at high field (Figure 4(b)) [1, 16]. It can be noticed from Figure 4(b) that, PF tunnelling is higher for the TiO2/Si sample. This might be due to the trap-assisted tunnelling owing to the generation of oxygen vacancies in TiO2 during the growth process [1]. So, it can be concluded that SiO2 layer incorporation in between TiO2 and Si substrate makes the interface of TiO2 and SiO2/Si better with lesser oxygen vacancies in TiO2.

Dielectric constant and equivalent oxide thickness (EOT) of TiO2 film for both the samples are calculated using conventional formulas and are listed in Table 2 along with hysteresis voltage, TiO2 film thickness and leakage current.

Another way to understand the interface quality is by studying the interface traps. High-k dielectrics produce significant number of interface traps which may degrade the electrical performance of the MOS device [17]. Lower interface traps signify superior interface. Figure 5 shows interface trapped ($D_n$) charge density for both the samples. $D_n$ is calculated by low frequency-high frequency of C–V measurement technique [18], given by the following Equation (2):

$$D_n = \frac{C_{ox}^2}{C_{ox}} \left( \frac{C_{ox}}{C_{ox}} - \frac{C_{ox}}{C_{ox}} \right)$$

It can be seen from the plot that number of interface traps has been reduced significantly for the sample with SiO2 passivation layer. So, it can be concluded from the plot that a better interface is achieved with the introduction of SiO2 layer.

To ascertain the device stability, reliability study is done under constant voltage and current stressing. Flat-band voltage shift
Figure 4: Plot of leakage current and its tunnelling fitting. (a) Leakage current of both the samples. (b) Poole–Frenkel (PF) tunnelling fitting of leakage current for both the sample at high field. (c) Fowler–Nordheim (FN) tunnelling fitting of TiO₂/SiO₂/Si sample at low field. (d) Schottky emission fitting of TiO₂/Si sample at low field.

Table 2: Hysteresis voltage, dielectric constant, EOT and leakage current from C–V and I–V curve

| Sample       | Hysteresis voltage (V) | Dielectric constant (TiO₂) | EOT (nm) | Leakage current (A/cm² at +2 V) |
|--------------|------------------------|---------------------------|----------|----------------------------------|
| TiO₂/SiO₂/Si | 0.34                   | 44.5                      | 12.51    | ≈8.61 × 10⁻⁸                     |
| TiO₂/Si      | 1.32                   | 35.8                      | 12.75    | ≈4.05 × 10⁻⁶                     |

obtained from the C–V characteristics at 100 kHz under a constant voltage stressing of −3 V and under a constant current stress of 50 μA over a considerable period of time (1000 s) for both samples are shown in Figures 6 and 7, respectively. Both the samples exhibit positive shift in the flat-band voltage, thus indicating the presence of electron traps in the oxide [1]. Sample with SiO₂ passivation layer reveals (Figure 6(a) and Figure 7(a)) better reliability over the sample without SiO₂ passivation layer (Figure 6(b) and Figure 7(b)) which again confirm better interface quality of the former sample. The shift in flat band voltage reveals that charge generation in the TiO₂/SiO₂/Si sample is lower than TiO₂/Si sample.

The stress-induced leakage current (SILC) at +2 V under a constant voltage stress of 5 V over 1000 s is shown in Figure 8. It can be seen from Figure 8, sample with SiO₂ passivation layer exhibits better performance with negligible stress-induced leakage current, while both the devices show very low SILC under constant voltage stressing. Hence, these devices can work reliably under constant voltage stressing.

Another important parameter that influences the reliability of the MOS devices is the position of the interface oxide charges, as it plays an important role in the flat band voltage shift and change in SILC. Charges appearing close to the interface degrade the MOS device performance badly [1].

4 | Conclusion

TiO₂ thin film of ≈13 nm thickness on Si <400> substrate with high dielectric constant and good reliability can be grown by employing cost effective VLS technique on Si substrate, with and without 5 nm ALD SiO₂ passivation layer. Incorporation of ALD SiO₂ layer makes significant improvements in the electrical characteristics and reliability of the device, which can be used to get superior quality MOS devices. XRD and SEM images reveal high quality crystalline TiO₂ films with corresponding substrates. XRD study reveal brookite TiO₂.
FIGURE 6  Flat-band voltage shift under a constant voltage stress of $-3 \, \text{V}$. (a) Sample with SiO$_2$ passivation layer. (b) Sample without SiO$_2$ passivation layer

FIGURE 7  Flat-band voltage shift under a constant current stress of 50 $\mu\text{A}$. (a) Sample with SiO$_2$ passivation layer. (b) Sample without SiO$_2$ passivation layer

Ultra-thin films on both the substrates at $2\theta = 33.5^\circ$, 61.7$^\circ$, and 75.7$^\circ$ with [130], [160] and [212] planes, respectively. The dielectric constant of TiO$_2$ film on SiO$_2$/Si substrate is 44.5 and on Si substrate is 35.8. $C$–$V$ plots show remarkable improvements in hysteresis voltage from 1.32 V for TiO$_2$/Si sample to 0.34 V for TiO$_2$/SiO$_2$/Si sample. Notable improvement of frequency dispersion is also observed for the sample with SiO$_2$ passivation layer. Reliability study reveals better performance of the sample with SiO$_2$ passivation layer. $I$–$V$ characteristics exhibits lower leakage current of $\approx 8.61 \times 10^{-8} \, \text{A/cm}^2$ for the TiO$_2$/SiO$_2$/Si device in comparison to the TiO$_2$/Si device with $\approx 4.05 \times 10^{-6} \, \text{A/cm}^2$ leakage current at $+2 \, \text{V}$ gate voltage. The dominant transport mechanism of leakage current for TiO$_2$/SiO$_2$/Si sample is due to FN tunnelling at low field and PF tunnelling at high field, whereas TiO$_2$/Si sample shows Schottky emission at low field and PF tunnelling at high field. Interface trapped charge density calculation reveals lower interface charges for the sample with SiO$_2$ passivation layer. Thus, the VLS growth process can be used as an alternative cost-effective technological route to grow high quality crystalline TiO$_2$ film for developing the future MOS devices on Si/SiO$_2$ substrates for electronic and photonic integrated circuits.

Soham Lodh$^{1,3}$
Rajib Chakraborty$^1$
Anindita Das$^2$

$^1$ Department of Applied Optics and Photonics, University of Calcutta, JD-2, Sector-III, Salt Lake, Kolkata 700106, India
$^2$ Department of Basic Science and Humanities, Regent Education and Research Foundation, Kolkata 700121, India
$^3$ Department of Electronics and Communication Engineering, MCKV Institute of Engineering, Howrah 711204, India

Correspondence
Rajib Chakraborty, Department of Applied Optics and Photonics, University of Calcutta, JD-2, Sector-III, Salt Lake,
Kolkata 700106, India.
Email: rcaop@caluniv.ac.in

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