A 31.5-to-40.5 GHz injection-locked CMOS frequency tripler with injection-current enhancement technique

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Abstract This letter presents an injection-locked 36 GHz frequency tripler (ILFT) for 5G applications. With the high order transformer based LC tank, over the target operating frequency range its phase response is flat at around 0 degree, and the injection-current is enhanced with a 3rd harmonic LC tail filter, thereby achieving a wide locking range. Fabricated in a 65 nm CMOS process, the ILFT consumes about 7.2 mW from a 0.6 V supply, and its core area without the output buffer and input matching network is only 0.25 × 0.4 mm². With 0 dBm input injection power, the proposed ILFT achieves a locking range from 31.5 to 40.5 GHz (25%).

Keywords: injection-locked frequency tripler, low power, injection current enhancement, transformer based LC tank

1. Introduction

According to [1, 2], the millimeter-wave (mm-Wave) band for 5G wireless network is planned to be 24.75–27.5 GHz, 27.5–28.35 GHz, 37–38.6 GHz, 38.6–40 GHz, and 37–42.5 GHz band worldwide. For these mmWave bands, the MIMO and phased-array transceiver systems are required. To simplify the LO distribution and to achieve low phase noise performance with low power consumption, the LO can be generated with low frequency PLL and frequency multiplier topologies [2, 3, 4, 5].

In general, the frequency multiplier can be realized with the harmonic amplifier [6, 7, 8] and injection locked frequency multiplier (ILFM) structures [9, 10, 11, 12, 13]. With the harmonic amplifier structure, the frequency multiplier can achieves relatively large bandwidth, but it consumes a high power consumption due to the low harmonic power efficiency. To address these issues and to achieve a wide locking range, an ILFM is proposed by combining with a transformer based high order LC tank and injection-current enhancement techniques.

As shown in Fig. 1, the ILFM working principle can be simply described with a half-circuit model [9, 10]. With the cross-couple pair current $i_{OSC}$, the loss of the LC tank can be compensated, ensuring self-oscillation start-up at the target operating frequency $f_0$. With an injection harmonic current $i_{INJ}$, the total current $i_{TOTAL}$ into the LC tank is the vector sum of $i_{OSC}$ and $i_{INJ}$, leading to a phase shift $\phi$. In principle, the maximum tolerable phase shift $\phi_{max}$ can be expressed as,

$$\phi_{max} = \arctan \frac{i_{INJ}}{i_{OSC}} \left(1 - \frac{\phi_{INJ}}{\phi_{OSC}}\right)^{-0.5}$$  \hspace{1cm} (1)

Accordingly, the frequency locking range can be enhanced either by flattening the phase response of the LC tank [9, 14] or increasing the injection current [2, 9, 15]. For the traditional ILFM LC tank, as its Q-factor is high, its locking range is very narrow, thereby requiring a complex calibration circuit to ensure a reliable operation. To solve this problem, based on the transformer element, the multi-order passive LC tank is widely used for ILFM and injection-locked frequency divider (ILFD) [16, 17].

Fig. 1. The working principle of the ILFM.

In this letter, by combining the high order passive transformer based LC tank and injection current enhancement techniques, a wide locking range, low power 36 GHz ILFT is presented. This letter is organized as follows. In Section 2, the circuit design and analysis of the proposed ILFT are undertaken. Section 3 presents the implementation and measurement results of the chip. Finally, a conclusion is drawn in Section 4.

2. Circuit design and analysis

Fig. 2 presents the proposed ILFT structure, which consists of the injection stage, the transformer based high order LC tank, the cross-coupled pair and the output buffer for test purposes. As indicated, in the transformer based LC tank, three inductors are coupled with each other, and each inductor and capacitor form a resonator, achieving a 6th-order LC tank [9, 18]. Note that, $K_{ad}$, $K_{as}$ and $K_{id}$ are the coupling coefficients of $L_a$, $L_d$, $L_a$ and $L_d$, $L_s$, and $L_d$, respectively. For the input injection stage, a 3rd harmonic LC tail filter is connected at its transistor source terminal.
As to be shown shortly, to illustrate the working mechanism of the proposed ILFT, the small signal model of the transformer based LC tank will be analyzed, deriving its input impedance. Moreover, with simulations the injection-current enhancement will be proved.

For calculation convenience, Fig. 3 shows the small signal model of the transformer based LC tank. With the small signal test current signal $I_{in}$, the input impedance of this LC tank can be derived as,

$$
Z_{ind} = \frac{1}{sC_d} \left( sL_d + R_d \right) \left( \frac{s^2 M^2_{ad}}{Z_{RLC}} + Z_{RLC} \right) + \frac{s^2 M^2_{ad}}{Z_{RLC}} Z_{RLC} Z_{RLCa} \left( s^2 \frac{M^2_{as}}{Z_{RLCd}} + Z_{RLCd} \right) / sC_a
$$

with

$$
M_{ad} = k_{sd} \sqrt{L_d L_s}, M_{ad} = k_{sd} \sqrt{L_d L_s},
$$

and

$$
\begin{align*}
Z_{RLC} &= sL_d + R_d + 1/sC_d \\
Z_{RLCa} &= sL_s + R_s + 1/sC_s \\
Z_{RLCd} &= sL_a + R_a + 1/sC_a
\end{align*}
$$

Note that, with calculations and simulations, it is found that each element parameter will affect $Z_{ind}$ poles if these three inductors are closely coupled with each other, thereby making the design very difficult. In the above derivation, $Z_{ind}$ expression is simplified by setting $k_{sd}$ to be 0, and this expression is also 6th-order, achieving almost the same phase response as the case with non-zero $k_{sd}$. Moreover, without loss of the calculation accuracy, here for calculation convenience, the capacitor series parasitic resistance is ignored as its $Q$-factor is very high at the target operating frequency range. For the inductor, due to its limited $Q$-factor, the series resistances of $L_d$, $L_s$ and $L_a$, i.e., $R_d$, $R_s$ and $R_a$, are taken into account.

For a wide locking range, as shown in Fig. 4, the inductor and capacitor value of the LC tank is optimized to achieve about 0 degree flatten phase response in the target locking range (about 30 to 40 GHz). Here for performance optimization, the magnitude response of $Z_{ind}$ and $Z_{ina}$ at terminal $V_d$ and $V_a$ is also plotted. Accordingly, the ILFM start-up condition can be ensured by sizing the negative $g_m$ of the cross-couple pair to be larger than $1/|Z_{ind}|$ [19, 20]. As indicated, in the range of 30 to 40 GHz, the impedance varies from 75 to 100 $\Omega$, thus satisfying the start-up condition. In addition, the $V_a$ terminal impedance, $Z_{ina}$ is also flat, which helps to realize a flatten frequency response of the injection current and the output power.

As mentioned before, the ILFM locking range can be also improved by increasing the injection current. For this purpose, Fig. 5 presents the detailed structure of the proposed input injection stage, in which the load $Z_{tank}$ represents the loading effect of the above discussed transformer based LC tank. Here, to increase the input power of the injection transistors, the transformer based balun is connected in between the input pads and the transistors, realizing the purpose of impedance matching. To generate a large harmonic current, the injection transistors work in the class-B mode [9, 21, 22, 23], and the neutralization capacitor $C_N$ is specially added to enhance its gain performance [24, 25]. To improve the ILFT working efficiency, a 3rd harmonic LC tail filter is connected at the injection transistor source terminal [19, 26, 27, 28, 29, 30].
Fig. 6 shows the performance comparison of the 3rd harmonic injection current with and without the tail filter. As indicated, with the tail filter, the injection current can be improved to be about 2 times larger. Moreover, it is indicated that, with the tail filter the injection transistor loading impedance on the LC tank can be improved over the target working frequency range, thus increasing the ILFT working efficiency and locking range further.

3. Implementation and measurement results

Fig. 7 presents the micrograph of the proposed ILFT. Fabricated in a 65 nm CMOS process, the whole chip area is about 0.5 × 0.8 mm², and the core area of the ILFT without output buffer and input matching network is only 0.25 × 0.4 mm². The cross-couple pair and injection transistors consume 7.2 mW for from a 0.6 V power supply, while the output buffer consumes 6 mW for test purposes.

With the Rhode & Schwarz phase noise analyzer equipment, the ILFT is measured. With 0 dBm injection power, the output spectrum of 31.5 and 40.5 GHz is shown in Fig. 8, indicating a 31.5–40.5 GHz (25%) locking range.

Fig. 9(a) presents the power comparison of the output harmonics, i.e. the fundamental injection frequency, 2nd harmonic and 3rd harmonic output power. As indicated, due to above design efforts the 3rd harmonic output power is about −10 dBm, which is flat from 31.5 to 40.5 GHz. Moreover, the ratio of the 3rd harmonic and the fundamental injection power is about −30 dBc, and the 2nd harmonic output power is slightly larger at locking range edges. Fig. 9(b) plots the measured input sensitivity curve. As indicated, the ILFT achieves the highest sensitivity at 12 GHz injection frequency, which agrees well with the frequency response of the transformer based LC tank. At the locking range edges, the locking sensitivity decreases and a larger injection power is required. Note that, in the measurement the injection power includes the cable loss and input network insertion loss.

![Simulation of the 3rd harmonic injection current.](image)

![Chip micrograph](image)

![Output spectrum at 40.5 and 31.5 GHz.](image)

![Output harmonics power comparison, measured input sensitivity.](image)
output signal in-band phase noise is about 20 log10(3) = 9.5 dB higher than that of the input injection signal. Here, due to the low input power, the out-of-band noise floor is slightly higher.

Table I presents the performance comparison with the state-of-the-art ILFT. By combining with the transformer based high order LC tank and tail current enhancement techniques, this work achieves low power consumption, a large locking range and low in-band phase noise.

Table 1. Performance summary of state-of-the-art ILFT

|                | This work | JSSC [9] | TCSI [11] | JSSC [12] | JSSC [13] |
|----------------|-----------|----------|-----------|-----------|-----------|
| Phase          |           |          |           |           |           |
| Locking range  | 31.5–40.5 | 34–48.2  | 22.4–24.8 | 25–28     | 27.4–30.8 |
| Bandwidth (%)  | 25        | 34.5     | 12.7      | 11.4      | 11.7      |
| Pnoise0 (dBc/Hz@100kHz) | -103 | -86     | -104.5    | -106.4    | -90       |
| Pnoise1 (dBc/Hz@1MHz)  | -120     | -111    | -120      | -105.3    | -113      |
| Power (mW)      | 7.2       | 16.8     | 10.4      | -         | 20.8      |
| ILFT only       |           |          |           |           |           |
| Chip area (mm²) | 0.1       | 0.12     | 0.125     | -         | 0.064     |
| Process (nm)    | 65        | 65       | 65        | 28        | 65        |

*Normalized to 40.5 GHz.
**Core area

4. Conclusion

An ILFT is presented for 5G applications with injection-current enhancement and the high-order transformer based LC tank techniques. Fabricated in a 65 nm CMOS process, the proposed ILFT achieves a 31.5-to-40.5 GHz (25%) locking range, and it consumes 7.2 mW from a 0.6 V supply.

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