Parallel Distributed Breadth First Search on the Kepler Architecture

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Abstract

We present the results obtained by using an evolution of our CUDA-based solution for the exploration, via a Breadth First Search, of large graphs. This latest version exploits at its best the features of the Kepler architecture and relies on a 2D decomposition of the adjacency matrix to reduce the number of communications among the GPUs. The final result is a code that can visit 400 billion edges in a second by using a cluster equipped with 4096 Tesla K20X GPUs.

1 Introduction

In some recent works [1, 2] we presented two multi-GPU codes that are able to explore very large graphs by using a cluster of GPUs. In the beginning, we proposed a new method to map CUDA threads to data by means of a prefix-sum and a binary search operation. Such mapping achieves a perfect load-balancing: at each level of a Breadth First Search (BFS) one thread is associated with one vertex to be visited. Then, we presented an enhanced algorithm whose main contributions were:

1. a modified Compressed Sparse Row data structure which allows for a faster and complete filtering of already visited edges;

2. a reduction of data exchanged among GPUs obtained by sending the predecessors of the visited vertices only in the end of the BFS.

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In the present work we further extend our work in two directions: i) on the single GPU we implement a new approach for the local part of the search that relies on the efficiency of the atomic operations available in the Nvidia Kepler architecture; ii) for the multi-GPU version, we follow a different approach for the partitioning of the graph among GPUs that is based on a 2D decomposition of the adjacency matrix that represents the graph. The latter change improves the scalability by leveraging on a communication pattern that does not require an all-to-all data exchange as our previous solution, whereas the former improves the performance of each GPU. The combination of the two enhancements provides a significant advantage with respect to our previous solution: the number of Traversed Edges Per Second (TEPS) is four times greater for large graphs that require at least 1024 GPUs.

The paper is organized as follows: in Section 2, we discuss our previous solution presented in [1] and [2]. Our current work is presented in Section 3. Section 4 reports the results obtained with up to 4096 GPUs. In Section 5 we briefly review some of the techniques presented in related works and compare our results with state-of-the-art implementations. Finally Section 6 concludes the work with a perspective on future activities.

2 Background on parallel distributed BFS

2.1 Parallel distributed BFS on multi-GPU systems

In a distributed memory implementation, the graph is partitioned among the computing nodes by assigning to each one a subset of the original vertices and edges sets. The search is performed in parallel, starting from the processor owning the root vertex. At each step, processors handling one or more frontier vertices follow the edges connected to them to identify unvisited neighbors. The reached vertices are then exchanged in order to notify their owners and a new iteration begins. The search stops when the connected component containing the root vertex has been completely visited.

The partitioning strategy used to distribute the graph is a crucial part of the process because it determines the load balancing among computing nodes and their communication pattern. Many authors reported that communications represent the bottleneck of a distributed BFS [3,4,5]. For what concerns computations, using parallel architectures such as GPUs, introduces a second level of parallelism that exploits a shared memory approach
for the local processing of the graph.

In our first work [1] we implemented a parallel distributed BFS for multi-GPU systems based on a simple partitioning of the input graph where vertices were assigned to processors by using a modulo rule. Such partitioning resulted in a good load balancing among the processors but required the processors to exchange data with, potentially, every other processor in the pool. This aspect limited the scalability of the code beyond 1024 GPUs.

As to the local graph processing, in our original code we parallelized the frontier expansion by using a GPU thread per edge connected to the frontier. In that way each thread is in charge of only one edge and the whole next level frontier set can be processed in parallel. In [1] we described a technique to map threads to data that achieves a perfect load-balancing by combining an exclusive scan operation and a binary search function.

The distributed implementation requires the data to be correctly arranged before messages can be exchanged among computing nodes: vertices reached from the frontier must be grouped by their owners. Moreover, many vertices are usually reached from different frontier vertices [6, 7, 1], therefore it is important to remove duplicates before data transfers in order to reduce communication overhead.

The removal of duplicates and the grouping of vertices can be implemented in a straightforward way by using the atomic operations offered by CUDA. However, at the time of our original work, atomics were quite penalizing so we implemented the two operations by supporting benign race conditions using an integer map and a parallel compact primitive [2]. The scalability of the code, however, was still limited to 1024 nodes.

Different partitioning strategies can be employed to reduce the number of communications [3, 5, 8]. Hereafter, we present the results obtained by combining a 2D partitioning scheme of the adjacency matrix representing the graph with our frontier expansion approach that takes advantage of the improved performance of the atomic operations available with the Nvidia Kepler architecture.

### 2.2 2D Partitioning

We implemented a 2D partitioning scheme similar to that described by Yoo et al. in [3], where \( RC \) computing nodes are arranged as a logical grid with \( R \) rows and \( C \) columns and mapped onto the adjacency matrix \( A_{N \times N} \), partitioning it into blocks of edges. The processor grid is mapped once horizontally
and $C$ times vertically thus dividing the columns in $C$ blocks and the rows in $RC$ blocks, as shown in Figure 1.

Processor $P_{ij}$ handles all the edges in the blocks $(mR + i, j)$, with $m = 0, ..., C - 1$. Vertices are divided into $RC$ blocks and processor $P_{ij}$ handles the block $jR + i$. Considering the edge lists represented along the columns of the adjacency matrix, this partitioning is such that (i) the edge lists of the vertices handled by each processor are partitioned among the processors in the same grid column and (ii) for each edge, the processor in charge of the destination vertex is in the same grid row of the edge owner.
Algorithm 1 Parallel BFS with 2D partitioning.

Require: Root vertex \( r \).

Require: Processor \( P_{ij} \).

1: \( \text{level}[] \leftarrow -1 \)
2: \( \text{pred}[] \leftarrow -1 \)
3: \( \text{bmap}[] \leftarrow 0 \)
4: \( \text{front} \leftarrow \emptyset \)
5: if \( r \) belongs to processor \( P_{ij} \) then
6: \( \text{level}[r] \leftarrow 0 \)
7: \( \text{pred}[r] \leftarrow r \)
8: \( \text{bmap}[r] \leftarrow 1 \)
9: \( \text{front} = \{r\} \)
10: end if
11: \( \text{lvl} \leftarrow 1 \)
12: while true do
13: \( \text{front} \leftarrow \text{gather front}[] \) from column \( j \) //vertical comm
14: for each \( u \) in \( \text{front} \) do
15: for each \( (u,v) \) in local edge list do
16: \( \text{col} \leftarrow \text{column of } v \)'s owner
17: send \( (u,v) \) to processor \( P_{i,col} \) //horizontal comm
18: end for
19: end for
20: \( \text{front} \leftarrow \emptyset \)
21: for each received edge \( (u,v) \) do
22: if \( \text{bmap}[v] = 0 \) then
23: \( \text{bmap}[v] \leftarrow 1 \)
24: \( \text{pred}[v] \leftarrow u \)
25: \( \text{level}[v] \leftarrow \text{lvl} \)
26: \( \text{front} = \text{front} \cup \{v\} \)
27: end if
28: end for
29: \( \text{lvl} \leftarrow \text{lvl}+1 \)
30: if \( \text{front} = \emptyset \) for all processors then
31: break
32: end if
33: end while

With a similar decomposition, each step of the BFS requires two communication phases, called expand and fold. The first one involves the processors in the same grid column whereas the second those in the same grid row. Algorithm 1 shows a pseudo code for a parallel BFS with 2D decomposition. At the beginning of the each step, each processor has its own subset of the frontier set of vertices (initially only the root vertex). The search entails the scanning of the edge lists of all the frontier vertices. Due to property \( (i) \) of the 2D decomposition, each processor gathers the frontier sets of vertices from the other processors in the same processor-column (vertical exchange, line 13). The frontier is then expanded by having each column of processors to collectively scan the edge lists of the gathered sets of vertices in search of edges leading to unvisited neighbors. For property \( (ii) \), edges found are sent
to the processors, in the same grid row, that own the destination vertices (horizontal exchange, lines 14-19). Unvisited destination vertices of the received edges form the frontier of the next BFS step (lines 20-28). The search ends when the frontier of each processor is empty, meaning that the whole connected component containing the root vertex has been visited [9].

The main advantage of the 2D partitioning is a reduction of the number of communications. If $P$ is the number of processors, our first implementation required $O(P)$ data transfers at each step whereas the 2D partitioning only requires $2 \times O(\sqrt{P})$ communications.

3 BFS on a multi-GPU system with 2D partitioning

Our work loosely follows the Graph500 [10] benchmark specifications. The benchmark requires to generate in advance a list of edges with an R-MAT generator [11] and to measure the performances over 64 BFS operations started from random vertices. It poses no constraint about the kind of data structures used to represent the graph but it requires the vertices to be represented using at least 48 bits. Since the focus of the present work is the evaluation of the new local part of the search and the 2D partitioning with respect to our original code, we do not strictly adhere to the Graph500 specifications and represent vertices with 32 bits\(^1\) (more than enough to index the highest number of vertices storable in the memory of current GPUs).

3.1 Local graph data structure

Each processor stores its part of the adjacency matrix as a $(N/R) \times (N/C)$ local matrix (Figure 1) where blocks of edges are stored in the same row order as in the global matrix. This allows to map global indexes to local indexes so that global row $v$ is mapped to the same local row for every processor in the same processor-row of the owner of vertex $v$. In a similar way, global column $u$ is mapped to the same local column for every processor in the same processor-column handling the adjacency list of vertex $u$.

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\(^1\)This choice does not limit the total size of graphs. They are generated or read by using 64 bits per vertex. The 32-bit representation is used to store local partitions.
Local adjacency matrices are sparse as the global matrix, so they are stored in compressed form. Since they are accessed by reading an entire column for each vertex of the frontier, we used a representation that is efficient for column access, the Compressed Sparse Column (CSC) format. As a consequence, processors may scan adjacency lists by accessing blocks of consecutive memory locations during the frontier expansion (one block for each vertex in the frontier of the same processor-column). Since the non-zeroes entries of an adjacency matrix have all the same value, the CSC is represented with only two arrays: the column offset array col and the row index array row.

Predecessors and BFS levels are stored in arrays of size \( N/R \) (number of rows of the local matrix). For the frontier, since it can only contain local vertices, we use an array of size \( N/(RC) \) and the information about visited vertices is stored in a bitmap with \( \lceil \frac{N/R}{32} \rceil \) 32-bit words.

### 3.2 Parallel multi-GPU implementation

The code may generate a graph by using the R-MAT generator provided by the reference code available from the Graph500 website[^referencecode]. Then the graph is partitioned as described in Section 2.2. The BFS phase is performed entirely by the GPUs with the CPUs acting as network coprocessors to assist in data transfers.

Algorithm [2] shows the code scheme of the BFS phase. Every processor starts with the level, predecessor and bitmap arrays set to default values (lines 1-4). The owner of the root vertex copies its local column index into the frontier array and sets its level, predecessor and visited bit (lines 5-10). All the data structures are indexed by using local indexes. At the beginning of each step of the visit, the expand communication is performed (line 13). Every processor exchanges its frontier with the other processors in the same processor-column and stores the received vertices in the all_front array. Note that in this phase, since processors send subsets of their own vertices, only disjoint sets are exchanged. After the exchange, in the expand_frontier routine, processors in each column collectively scan the whole adjacency lists of the vertices in all_front (line 14). For each vertex, its unvisited neighbors are set as visited and the vertex is set as their predecessor. For neighbors owned locally the level is also set. The routine returns the unvisited neigh-

[^referencecode]: http://www.graph500.org/referencecode
Algorithm 2 Parallel BFS with 2D partitioning.

Require: Root vertex \( r \).
Require: \( \text{CSC} = \text{(row[]),col[]} \).
Require: Processor \( P_{ij} \).

1: level[:] ← −1
2: pred[:] ← −1
3: bmap[:] ← 0
4: front ← []
5: if \( r \) belongs to \( P_{ij} \) then
6:   level[LOCAL_ROW(r)] ← 0
7:   pred[LOCAL_ROW(r)] ← r
8:   bmap[LOCAL_ROW(r)] ← 1
9:   front[0] ← LOCAL_COL(r)
10: end if
11: lvl ← 1
12: while true do
13:   all_front ← expand_comm(front)
14:   dstVerts ← expand_frontier(row, col, level, pred, bmap, all_front)
15:   front[:] ← dstVerts[j][:]
16:   dstVerts[j] ← []
17:   int_verts ← fold_comm(dstVerts)
18:   front ← front ⊕ update_frontier(row, col, level, pred, bmap, int_verts)
19:   if len(front) = 0 for all processors then
20:     break
21: end if
22: lvl ← lvl+1
23: end while

After the frontier expansion, neighbors local to the processor are moved from the \( j \)-th block of the \text{dstVerts} array into the \text{front} array (lines 15-16) and the \text{fold} communication phase is performed. Unvisited neighbors just discovered are sent to their owners, located in the same processor-row, and received vertices are returned in the \text{intverts} array (line 17). Finally, the \text{update_frontier} routine selects, among the received vertices, those that have not been visited yet and sets their level and bitmap bit (line 18). Returned vertices are then appended to the new frontier and the cycle exit condition is evaluated (line 19). The BFS continues as long as at least one processor has a non-empty frontier at the end of the cycle.
The output is validated by using the same procedure included in our original code.

3.3 Communications

The expand and fold communication phases are implemented with point-to-point MPI primitives and make use of the following scheme:

- start send operations;
- wait for completion of receive operations posted in the previous round;
- post non-blocking receive operations for the next round.

that hides the latency of the receive operations in the BFS round and avoids possible deadlocks due to the lack of receive buffers.

Since the communication involves only local indexes, the expand and fold phases are carried out by exchanging 32-bit words.

3.4 Frontier expansion

After the local frontiers have been gathered, the frontier expansion phase starts. This phase has a workload proportional to the sum of the degrees of the vertices in the current frontier. There are no floating point operations, just few integer arithmetic operations, mainly for array indexing, and it is memory bandwidth bound with an irregular memory access pattern. It is characterized by a high degree of intrinsic parallelism, as each edge originating from the frontier can be processed independently from the others. There could be, however, groups of edges leading to the same vertex. In those cases, only one edge per group should be processed. In our code we use a thread for each edge connected to the frontier and this allows the selection of the single edge to be followed in, at least, two ways: either by taking advantage of benign race conditions or by using synchronization mechanisms such as atomic operations.

In our previous work, we chose to avoid atomic operations because they were quite penalizing with the Nvidia Fermi architecture, available at that time. The current architecture, codenamed Kepler, introduced many enhancements including a significant performance improvement of the atomic operations (almost an order of magnitude with respect to Fermi GPUs). As
a consequence, we decided to use atomics in the new 2D code. The resulting code is much simpler because there is no longer the need to support the benign race conditions on which the original code relied \[\pi\]. Atomics are used to access the bitmap in both the frontier expansion and update phases and to group outgoing vertices based on destination processors.

At the beginning of the expansion phase, the vertices in the blocks of the all\_front array are copied in a contiguous block of device memory and then the corresponding columns of the CSC matrix are processed. We employ a mapping between data and threads similar to the one used in our previous code \[\pi\] where a CUDA thread is used for every edge originating from the current frontier. The mapping allows to achieve an optimal load balancing as

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**Figure 2:** Threads to data mapping assigning one thread per edge. From top to bottom, the first array represents the local column indexes corresponding to frontier vertices. The second contains the local degrees of each vertex, \textit{i.e.} the number of non-zeroes per column (23 in total), and the third one is the cumulative degree array. The CUDA grid is launched with (at least) 23 threads. By searching the cumulative array for the greatest entry less than its global id, each thread finds its frontier vertex. Finally, threads mapped to the same frontier vertex process its edge list (a CSC column).
edge data are evenly distributed among the GPU threads. Given the frontier vertices \( u_0, u_1, u_2, \ldots, u_{n-1} \) with degrees \( d_0, d_1, d_2, \ldots, d_{n-1} \) and adjacency lists:

\[
v_0^0, v_0^1, \ldots, v_{d_0-1}^0 | v_1^0, v_1^1, \ldots, v_{d_1-1}^1 | \ldots | v_{d_{n-1}-1}^0, v_{d_{n-1}-1}^1, \ldots, v_{d_{n-1}-1}^{n-1}
\]

thread \( i \) is mapped onto the \( j \)-th edge connected to vertex \( u_k \):

\[
i \leftrightarrow (u_k, v_j^k), \quad k = \max \left\{ t \left| \sum_{s=0}^{t} d_s \leq i, \ \forall l < n \right. \right\} \quad j = i - \sum_{s=0}^{k} d_s
\]

After vertices in \textbf{all_front} are copied to device memory, we use their degrees to compute a cumulative degree array by means of an exclusive scan operation. The column scan kernel is then launched with \( r = \sum_{s=0}^{n-1} d_s \) threads. Each thread processes one local edge \((u, v)\) originating from the frontier, i.e. one element of column \( u \) of the CSC (see Figure 2). Algorithm 3 shows the pseudo code for the column scan kernel. The source vertex \( u \) is found by performing a binary search for the greatest index \( k \) such that \( \text{cumul}[k] \) is less than or equal to the global thread id (line 2) and by accessing the \( k \)-th location of the \textbf{frontier} array (line 3) \[12\].

The column offset of vertex \( u \) is found in the \( u \)-th element of the CSC column index array \textbf{col}. The row offset of the destination vertex is computed by subtracting from the thread id the degrees of the vertices preceding \( u \) in the \textbf{frontier} array. Finally, the local id \( v \) of the destination vertex is found by accessing the CSC row index array at the location corresponding to the sum of both the column and the row offsets (line 4).

The status of the neighbor \( v \) is then checked (lines 5-6). If the vertex has already been visited, then the thread returns. Otherwise, it is marked as visited with an \textit{atomicOr} operation (line 7). That instruction returns the value of the input word before the assignment. By checking the vertex bit in the return value, it is possible to identify the first of different threads handling edges leading to the same vertex (assigned to different columns) that set the visited bit (line 8). Only the first thread proceeds, the others return.

The bitmap is used not only for the vertices owned locally but also for those, belonging to other processors (in the same processor-row), that are reachable from local edges. In other words, the bitmap has an entry for each row of the CSC matrix. This makes possible to send external vertices just once in the fold exchanges because those vertices are sent (and marked in
the bitmap) only when they are reached for the first time in the frontier expansion phase.

**Algorithm 3** CUDA atomic-based column scan kernel.

**Require:** frontier[].
**Require:** current level.
**Require:** dst_cnt[] = 0.
**Require:** cumulative degree array cumul[].
**Require:** Processor $P_{ij}$.
**Require:** CSC=(row[], col[]), bmap[], level[] and pred[].

1: gid ← (blockDim.x*blockIdx.x + threadIdx.x)
2: k ← binsearch_maxle(cumul, gid)
3: u ← frontier[k]
4: v ← row[col[u] + gid - cumul[k]]
5: m ← 1 << (v mod 32)
6: if (bmap[v/32] & m) return
7: q ← atomicOr(&bmap[v/32], m)
8: if !(m & q) then
9: tgtj ← v/(N/(RC))
10: off ← atomicInc(&dst_cnt[tgtj])
11: if (tgtj != j) then
12: dst_verts[tgtj][off] ← v
13: else
14: dst_verts[j][off] ← ROW2COL(v)
15: lvl[v] ← level
16: end if
17: pred[v] ← u
18: end if

Each unvisited neighbor is added to the array associated to the processor-column of its owner processor in preparation for the subsequent fold exchange phase (lines 12 and 14). The processor-column is computed based on the local index of the neighbor (line 9) and the counter for such column is atomically incremented to account for multiple threads appending for the same processor (line 10). If the neighbor belongs to the local processor its level is also set (line 15). Finally, regardless of the owner, the neighbor predecessor is set (line 17).

After the kernel has completed, the array containing the discovered vertices (grouped by owner) is copied to host memory in preparation for the fold communication phase.
3.4.1 Optimizations

In the current CUDA implementation, we introduced an optimization to mitigate the cost of the binary searches performed at the beginning of the column scan kernel. Since threads search for their global index in the cumulative array, non-decreasing indexes are returned to consecutive threads:

\[ \text{binsearch\_maxle}(\text{cumul}, \text{gid}) \leq \text{binsearch\_maxle}(\text{cumul}, \text{gid}+1) \]

Where \( \text{gid} \) is the global thread identifier that is equal to:

\[ \text{threadIdx.x} + \text{blockIdx.x} \times \text{blockDim.x} \]

That relation makes possible to scan the columns with fewer threads than the number of edges originating from the frontier without increasing the number of binary searches performed \( \text{per thread} \). This is done by assigning each thread to a group of consecutive elements in the CSC columns. If not enough elements are available in the column, the group overlaps on the next column. Then, each thread performs a binary search only for its first edge to obtain a base column index. The indexes for subsequent edges \( tid + i \) are found by incrementing the base index until \( (tid + i) \geq \text{cumul[base + 1]} \).

The overhead introduced by these linear searches is very limited because the majority of edge groups are contained in a single column and so the base column index is never incremented.

Among other optimizations, there is the passage of read-only arrays to kernels with the modifiers \text{const/restrict}. In this way the compiler uses the read-only data cache load functions to access them. Moreover, in order to increase instruction-level parallelism, edges assigned to a thread are not processed sequentially. Instead, they are processed together in an interleaved way by replicating and grouping together kernel instructions for different edges.

We found that the maximum performance is obtained by assigning four edges per thread. In this case, we measured a performance gain of \( \sim 40\% \) with respect to the case with a thread per neighbor.

3.5 Frontier update

In the frontier update phase, local vertices remotely discovered and received during the fold exchange, are processed to find those that are locally unvisited, \( i.e., \) whose visited bit is not set. Since this phase processes the vertices
received, instead of their adjacency lists, fewer computational resources are required compared to those necessary in the frontier expansion phase.

As in the expand communication phase, vertices returned by the fold exchange are grouped by sender in different blocks and thus, before starting the processing, they are copied to device memory in contiguous locations.

After the copy, the frontier update kernel is launched with a thread per vertex. Threads are mapped linearly onto the arrays of vertices and each thread is responsible of updating the level and predecessor of its vertex, if unvisited, and to add it to the output array. As in the frontier expansion kernel, we make use of atomic operations in order to synchronize the accesses to the bitmap and the writes to the output buffer.

As to the predecessor, since in the fold phase we do not transmit source vertices, the thread, lacking this information, stores the sender processor-column in the predecessor array (the sender saved the predecessor).

After the kernel has completed, the output array is copied to host memory and it is appended to the frontier array.

4 Results

The performances hereafter reported have been obtained on the Piz Daint system belonging to the Centro Svizzero di Calcolo Scientifico (CSCS). Piz Daint is a hybrid Cray XC30 system with 5272 computing nodes interconnected by an Aries network with Dragonfly topology. Each node is powered by both an Intel Xeon E5-2670 CPU and a NVIDIA Tesla K20X GPU and is equipped with 32 GB of DDR3 host memory and 6 GB of GDDR5 device (GPU) memory.

The code has been built with the GNU C compiler version 4.8.2, CUDA C compiler version 5.5 and Cray MPICH version 6.2.2. For the GPU implementation of the exclusive scan we used the CUDA Thrust library [13], a well-known, high performance template library implementing a rich collection of data parallel primitives.

The code uses 32-bit data structures to represent the graph because the memory available on a single GPU is not sufficient to hold $2^{32}$ or more edges and it transfers 32-bit words during the communications because the frontier expansion/update and expand/fold communications work exclusively on local vertices. We use 64-bit data only for graph generation/read and partitioning. For the generation of R-MAT graphs we use the make_graph routine found

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| # of GPUs | grid size | scale | edge factor | # of GPUs | grid size | scale | edge factor |
|-----------|-----------|-------|-------------|-----------|-----------|-------|-------------|
| 1         | 1 x 1     | 21    |             | 128       | 8 x 16    | 28    |             |
| 2         | 1 x 2     | 22    |             | 256       | 16 x 16   | 29    |             |
| 4         | 2 x 2     | 23    |             | 512       | 16 x 32   | 30    |             |
| 8         | 2 x 4     | 24    | 16          | 1024      | 32 x 32   | 31    | 16          |
| 16        | 4 x 4     | 25    |             | 2048      | 32 x 64   | 32    |             |
| 32        | 4 x 8     | 26    |             | 4096      | 64 x 64   | 33    |             |
| 64        | 8 x 8     | 27    |             |           |           |       |             |

Table 1: Processor grid and R-MAT graph configurations used for the tests.

Figure 3: Harmonic mean TEPS measured with a number of GPUs ranging from 1 to 4096 keeping the graph scale per processor fixed.

Figure 4: Speedup of the 2D code measured by visiting an R-MAT graph with scale=2^{25}.

in the reference code for the Graph500 benchmark. The routine returns a directed graph with 2^{scale} vertices and \( \sim edge\_factor \times 2^{scale} \) edges. We turn the graph undirected by adding, for each edge, its opposite. Most of the following results are expressed in Traversed Edges Per Second (TEPS), a performance metric defined by the Graph500 group as the number of input edge tuples within the component traversed by the search, divided by the time required for the BFS to complete, starting right after the graph partitioning. The tests have been performed with both R-MAT generated and real-world graphs. Table 1 reports the processor-grid configurations, scales and edge factors used for R-MAT graphs.

Figure 3 shows the weak scaling plot obtained by using a number of
GPUs ranging from 1 to 4096. In order to maintain a fixed problem size per GPU, the graph scale has been increased by 1 for each doubling of the number of processors, starting from scale 21 (the edge factor had been set equal to 16). For each scale, we report the harmonic mean of the TEPS measured in 64 consecutive BFS operations (a different root vertex is chosen at random for each search). The code scales up to 4096 GPUs where the performances reaches $\sim$400 GTEPS on a graph with $2^{33}$ vertices and $\sim$280 billions of directed edges. Figure 4 shows the strong scaling plot obtained by visiting a fixed R-MAT graph with scale 25 and edge factor 16 with an increasing number of GPUs. The code scales linearly up to 16 GPUs. With 32 processors, the cost of data transfers becomes comparable to the cost of computations and with more GPUs the advantage becomes marginal and the efficiency drops.

Figure 5 reports the compute and transfer times of the code. The compute time is the aggregate time required by the frontier expansion and update phases whereas the transfer time includes the time spent in the expand and fold exchanges and in the allreduce operation at the end of the BFS loop. Up to 2048 GPUs, data transfers require less than half of the total BFS time. With 4096 GPUs the communications become dominant and take almost 60% of the total search time. Above 4096 GPUs, we do not expect the code
Figure 7: Comparison of computation (left plot) and communication (right plot) times between the new code based on 2D decomposition and our original code. Both codes have been run on graphs as specified in the Table 1.

to scale anymore but we did not test it directly.

In Figure 6 it is reported the timing breakdown of the four steps performed in the BFS round: expand exchange, frontier expansion, fold exchange and frontier update. Times are summed across the BFS steps and averaged across 64 operations. By increasing the number of processors, the time required by the frontier expansion phase reduces and, as expected, the weight of the communications increases, becoming dominant with 4096 GPUs. The time required by the frontier update phase is always much smaller than the time spent in the frontier expansion. With any configuration, it accounts for less than 10% of the total time required by the four steps.

In Figure 7 we report the comparison of computation and communication times between our original code and the new one, both run on the Piz Daint cluster. For what concerns the communications (right plot), the advantage of 2D partitioning is apparent with any number of GPUs up to 1024, where 2D transfers are almost eight times faster than those in the original code. For what concerns the computations, with 1024 GPUs the 2D code is $\sim 3.5$ times faster. This advantage is mainly due to the performance improvement of the atomic operations implemented in the Kepler architecture. Figure 8 shows a comparison of frontier expansion times between our present code using atomics and our original code. Starting from 16 GPUs, the frontier expansion performed with atomic operations is 2 times faster than our original
Figure 8: Comparison of the time required by the frontier expansion phase in the new code and the original code. The former is based on atomic operations whereas the latter uses scatter/compact parallel primitives to support benign race conditions.

In Table 2, we report the performance of the 2D code obtained on a single GPU with both the Fermi and Kepler architectures. The code runs more than twice as fast on the Kepler GPU.

Table 2: GTEPS obtained by running the 2D code on a Tesla S2050 (Fermi) and on a Tesla K20X (Kepler) using an R-MAT graph with scale 21 and edge factor 16.

| # of GPUs | Tesla S2050 | Tesla K20X |
|-----------|-------------|------------|
| 1         | 0.48        | 1.13       |

In Table 2, we report the performance of the 2D code obtained on a single GPU with both the Fermi and Kepler architectures. The code runs more than twice as fast on the Kepler GPU.

Finally, Table 3 reports the results obtained traversing real-world graphs obtained from the Stanford Large Network Dataset Collection [14]. Among them we selected undirected graphs with the highest number of edges.
Table 3: BFS performance of the 2D code with real-world graphs from the Stanford collection. For each graph are reported the number of vertices, of edges, and the (approximate) scale and edge factor (to facilitate the comparison with RMAT graphs). Each traversal has been performed 64 times starting from random vertices, with the specified number of GPUs. Performances reported are the harmonic means of the TEPS measured in the traversals. Within parenthesis are reported the performance figures of the original code.

| Data Set Name    | Vertices | Edges   | Scale | EF | GPUs | GTEPS  |
|------------------|----------|---------|-------|----|------|--------|
| com-LiveJournal  | 3997962  | 34681189| ∼ 22  | ∼ 9 | 2    | 0.77 (0.43) |
| soc-LiveJournal1 | 4847571  | 68993773| ∼ 22  | ∼ 14| 2    | 1.25 (0.47) |
| com-Orkut        | 3072441  | 117185083| ∼ 22  | ∼ 38| 4    | 2.67 (1.43) |
| com-Friendster   | 65608366 | 1806067135| ∼ 25  | ∼ 27| 64   | 15.68 (5.55) |

5 Related works

In recent years high performance implementations of graph algorithms have attracted much attention. Several works tackled the issues related to both shared memory and distributed memory systems.

On the single GPU different solutions have been proposed to address workload imbalance among threads. The naive assignment, in which each thread is assigned to one element of the BFS queue, may determine a dramatic unbalance and poor performances [1]. It is also possible to assign one thread to each vertex of the graph but, as showed by Harish et al. [15], the overhead of having a large number of unutilized threads results in poor performances. To solve this problem, Hong et al. [16, 17] proposed a warp centric programming model. In their implementation each warp is responsible of a subset of the vertices in the BFS queue. Another solution has been proposed in the work of Merrill et al. [6]. They assigned a chunk of data to a CTA (a CUDA block). The CTA works in parallel to inspect the vertices in its chunk.

We devised an original data mapping described in [1]. Then, to reduce the work, we used an integer map to keep track of visited vertices. Agarwal et al., first introduced this optimization using a bitmap that has been used in almost all subsequent works.

On distributed memory systems many recent works rely on a linear algebra based representation of graph algorithms [5, 18, 19, 20].
Ueno et al. [21] presented a hybrid CPU-GPU implementation of the Graph500 benchmark, using the 2D partitioning proposed in [3]. Their implementation uses the technique introduced by Merrill et al. [6] to create the edge frontier and resort to a novel compression technique to shrink the size of messages. They also implemented a sophisticated method to overlap communication and computation in order to reduce the working memory size of the GPUs.

A completely different algorithm that uses a bottom-up approach was proposed by Beamer et. al [7] and extended in [20] for a cluster of CPUs. Although the algorithm is really effective in terms of TEPS, it actually does not traverse all the edges in the connected component but only a fraction that is sufficient to build a valid BFS tree.

Satish et al. [8] implemented independently a technique to exchange predecessors very similar to our method.

It is worth noting that our implementation is relatively simple compared to other sophisticated implementations [21, 8, 19, 20].

Moreover we focused our attention on a full GPU implementation whereas all other works, as far as we know, are CPU only or hybrid implementations that use GPUs for the most expensive computational levels of the BFS.

### 5.1 Comparisons with state-of-the-art implementations on shared memory and distributed memory systems

| Authors     | scale | $ef$ | GTEPS | Num Processors  | Arch. Type         | Output |
|-------------|-------|------|-------|-----------------|--------------------|--------|
| Beamer      | 21    | 32   | 10.45 | 2 sockets/16 cores | Sandy Bridge ES-2680 | parent |
| Merrill     | 21    | 32   | 8.3   | 4               | Tesla C2050        | distance |
| Agarwal     | 22    | 64   | 1.3   | 4 sockets       | Nehalem EX          | parent |
| Hong        | 25    | 16   | 0.9   | 1               | CPU+GPU            | distance |
| Bader       | 27    | 5    | 0.5   | 40              | Cray MTA-2         | distance |
| Present work| 21    | 16   | 1.1   | 1               | Kepler K20X        | parent |

Table 4: Best performances reported by different authors for BFS operations on shared memory systems. For all the implementations the graph is of type R-MAT. The average number of edges per vertex is indicated with $ef$. The number of vertices is equal to $2^{scale}$.

Tables 4 and 5 report the best performances of different codes on, respectively, shared memory systems and distributed memory systems. It is
difficult to compare these results because each implementation uses different parameters that have a huge impact on the number of TEPS. For example, independently on the number of processors, a large graph scale almost always determines a higher number of TEPS. Even when comparing results for the same scale, there is no guarantee that we are comparing the same numbers because the input graph is randomly generated and, for each source vertex selected, the visited component may vary.

| Authors  | scale | el | GTEPS | Num Processors (CPU/GPU) | Arch. Type         | Output       |
|----------|-------|----|-------|--------------------------|-------------------|-------------|
| Buluç [5]| 32    | 16 | 17.8  | 3300 (40000 cores)       | Cray XT6          | distance    |
| Lv [4]   | 32    | 16 | 12.1  | 1024 (6144 cores)        | Xeon X5650        | parent      |
| Ueno [18]| 36    | 16 | 103   | 1366 (16302 cores)       | Xeon X5670(Tsubame 2.0) | parent      |
| Ueno [21]| 35    | 16 | 317   | 1366 (16362 cores) + 4096 GPU | Xeon X5670, Fermi M2050 | parent      |
| Ueno [21]| 35    | 16 | 115   | 320 (5120)               | Xeon E52670       | parent      |
| Satish [8]| 33   | 16 | 250   | 4096 (65536)             | BG/Q              | parent      |
| Beamer [20]| 35 | 16 | 240  | 7187 (115000)            | Cray XK6 Gemini   | parent      |
| Present work | 33 | 16 | 396  | 4096                     | Kepler K20X       | parent      |

Table 5: Best performances for distributed BFS implementations. For all the implementations the graph is of type R-MAT.

It is apparent from Table 4 that our implementation has good performance on the single GPU even when compared to CPU shared memory implementations. This is mainly due to the efficiency of our data mapping and atomic primitives of the Kepler architecture. Our results with 4096 GPUs (400 GTEPS) outperform all distributed implementations. The comparison however is not completely fair in some cases because our code is not fully compliant with the Graph500 benchmark.

6 Conclusions

We presented the performance results of our new parallel code for distributed BFS operations on large graphs. The code employs a 2D partitioning of the adjacency matrix for efficient communications and uses CUDA to accelerate local computations. The computational core is based on our previous work on GPU graph processing and is characterized by optimal load balancing among GPU threads, taking advantage of the efficient atomic operations of the Kepler architecture.

The result is a code that scales up to 4096 Nvidia K20X GPUs, visiting 400 billion edges per second of an R-MAT graph with \(2^{33}\) vertices and \(\sim 280\) billions of directed edges.
We compared the performances of the new code with those of the original one, which relied on a combination of parallel primitives in place of atomic operations, on the same cluster of GPUs. The 2D code is up to four times faster on R-MAT graphs of the same size.

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In order to reduce the amount of exchanged data, in the fold phase we send only destination vertices, instead of edges. Moreover, to avoid sending more than once the same vertex to its owner, we use a bitmap to keep track of local vertices that have been visited.

Graph 500 benchmark (www.graph500.org).

Deepayan Chakrabarti, Yiping Zhan, and Christos Faloutsos. R-mat: A recursive model for graph mining. Computer Science Department. Paper 541. (http://repository.cmu.edu/compsci/541), 2004.

Since consecutive threads search for consecutive values, sequences of threads mapped onto the same adjacency lists access the same memory locations during the binary search. Different sequences share an initial part of the search path whose length depends on their relative distance. As a consequence, the memory access pattern is quite efficient since threads in each sequence perform broadcast memory accesses that are served with single memory transactions, one for each search jump.

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