Retraction

Retraction: Review on Radiation Hardness Assurance by Design, Process and NextGen Devices (J. Phys.: Conf. Ser. 1916 012002)

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This article (and all articles in the proceedings volume relating to the same conference) has been retracted by IOP Publishing following an extensive investigation in line with the COPE guidelines. This investigation has uncovered evidence of systematic manipulation of the publication process and considerable citation manipulation.

IOP Publishing respectfully requests that readers consider all work within this volume potentially unreliable, as the volume has not been through a credible peer review process.

IOP Publishing regrets that our usual quality checks did not identify these issues before publication, and have since put additional measures in place to try to prevent these issues from reoccurring. IOP Publishing wishes to credit anonymous whistleblowers and the Problematic Paper Screener [1] for bringing some of the above issues to our attention, prompting us to investigate further.

[1] Cabanac G, Labbé C and Magazinov A 2021 arXiv:2107.06751v1

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Review on Radiation Hardness Assurance by Design, Process and NextGen Devices

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Abstract. Aggressive scaling, shrinking device size and exponential rise in device density over the past two decades has contributed significantly in improving the power and performance metrics of Integrated Circuit (IC) technology. For specific applications like Space electronics, Implanted Biomedical, Sensor devices etc. drastic scaling has resulted in increasing the susceptibility of the nanoscale circuits to radiation effects. The objective of the paper is to provide an overview of the radiation hardening techniques at various levels of IC design and development, i.e. at Device Structure-Fabrication process (Radiation Hardening by Process) and Circuit and layout design (Radiation Hardening by Design), to mitigate the effects of radiation and improve reliability. The work also presents comparison of next generation device structure that utilize Carbon Nano Tubes (CNTs) and Semiconductor NanoWires (GAA-Si, GaAs, InN) against traditional MOSFET based device structures for operation under the radiation environment.

Keywords: Radiation Hardness Assurance, TID, SEE, SOI, SOS, CNTFETs, FinFETs, NanoWires.

1. Introduction
Traditionally technology scaling is focused on decreasing feature size (Esp. Channel length) to increase density, reduce power consumption and enhanced performance. Reduction in feature size also lowers the node capacitance and in turn the charge stored. For digital logic the stored charge (~potential) at an output node represents the computation value of the circuit. For nanoscale circuits when they are exposed to Space radiation, the radiation particle strike causes ionization and generates Electron-Hole Pair (EHP). Particle incidence mechanism can be categorized into following steps as shown in Figure 1 1) direct ionization, 2) Indirect Ionization and 3)Charge Collection, which creates instabilities in the semiconductor device, worst case can lead to permanent damage. In direct ionization, the particle incident on the device generates electron-hole pairs along the path of the particle as mentioned above, with the holes created getting trapped in the oxide. In indirect ionization, the particle causes nuclear reactions leading to ionization with the holes getting trapped in the oxide. This absorbed (trapped) dose is the Total Ionization Dose that causes semiconductor degradation increase with time. With increase in the trapped charge there is shift in biasing potential which can cause the device to change the operation status from either On to Off or Off to On. Thereby resulting in the output node to flip in logic i.e. change the charge stored. If the change in logic level at the output node is temporary, it is termed as Single Event Transient (SET) especially when observed in combinational circuits. If in case the charge
in logic level cannot be restored, it is termed as Single Event Upset (SEU) most commonly associated with memory cells.

The radiation environment around earth atmosphere can be due to (i) Particles trapped around the earth’s atmosphere (in the Van Allen belts) that comprising of high energy $p^+$ (protons), $e^-$ (electrons) and heavy ions and (ii) Transient Radiation consisting of cosmic ray particles from solar events. Over the time exposure to this radiation environment can degrade the performance of electronic devices and can also cause a permanent functional failure. If the damage device operation is compromised and the effect is permanent, it is termed as Total Ionizing Dose (TID). The cumulative long-term damage can cause the device to undergo threshold shifts, increased device leakage (which contributes to the static power consumption), timing changes, decreased functionality, etc. if it is temporary or transient, it is termed as Single Event Effect (SEE). So, SEE can be expressed in terms of failure rate that is random and TID in terms of failure rate that is described by Mean Time to Failure [1]. There are many device shielding techniques that can be used to reduce the TID and SEE [2]. The TID tolerance in CMOS devices increase due to the decreased trapped charge yield as the oxide volume decreases. In CMOS with gate oxide thickness less than or equal to 7 nm, the shift in threshold voltage due to radiation is eliminated.

SEEs are classified as soft and hard errors. Soft errors are nondestructive, functional errors caused by ions of high energy. Soft errors include Single Event Upsets (SEUs), Single Event Transients (SETs), Single Event Functional Interrupts (SEFIs), Multiple-Bit Upsets (MBUs), and Multi-cell Upsets (MCUs). An SEU corresponds to the flip of the cell state, mostly in a memory device, latch and register. A SET in a combinational logic corresponds to the transient pulses generated in a gate by a charge from a high energy particle that can propagate along the path and latched in a storage cell. SETs are fundamental to all the SEEs i.e., SEU, MBU, SEL etc. A SEL occurs by triggering of parasitic activities in a bulk CMOS structure, which induces a low impedance path between power and ground, and thereby causes an increase in the supply current. This in turn can over heat the structure and may cause latent and hard errors. Transient pulses can cause SEFIs causing long duration functional loss (component reset, lock-up etc.). This functionality can be recovered by a power cycle or reset/reload of a configurable register [3].

Hard errors cause permanent damage to the device which is irreversible and causes data loss. Even with a power reset the data cannot be recovered. SEE hard errors are potentially destructive. Typical examples of hard errors are Single Event Latch-up (SEL), Single Event Gate Rupture (SEGR) and Single Event Burnout (SEB). A Single Event Burnout (SEB) is a condition where the device, when hit by a high energy particle, is burned out due to high current, causing catastrophic failure. SEBR is a destructive condition which is the result of the burn out of a gate insulator in a MOSFET device [4].

The TID radiation effects can be reduced by designing devices with a very fine geometry and thinner oxides thereby improving its tolerance. Similarly, SEEs can be decreased by increasing the IC scaling such that SETs and SEUs need less energy. In devices with high operational frequencies, most of the SETs turn into SEUs, while increasing SEFIs count [5].

Radiation hardness for a semiconductor device or circuit is to be resilient to the effects of the above-mentioned high-energy particle strike that causes ionization. They are referred as Radhard devices or circuits that preserve the electrical characteristics under the harsh radiation environment. Further, a radhard circuit continues to demonstrate functional correctness to a specified amount and type of radia-
tion that is at higher level than anon-radhard/conventional circuit. Applications of radhard device and circuits include Space electronics, Nuclear reactors and Particle accelerators. Processing factors that influence the radhard device are W/L ratio, doping concentration, structure fabrication-construction, oxide layers (insulating thickness) and electrical fields/potential distribution at physical layout.

Another type of damage possible due to radiation is Displacement Damage (DD). DD occurs when the particle strikes the silicon substrate. It displaces an atom in the substrate and can create Frenkel defects consisting of vacancy and interstitial defect. DD has not much of an effect on CMOS devices, rather they effect the bipolar devices. Because of the displacement damage, the gain of the device is reduced slowly leading to permanent damage of the device [6]. SEE is relative to DD and TID with each particle traversing through the semiconductor (mostly high energy hadrons – HEH) with a certain probability of interaction [7]. SEU, SET and SEL effects are of utmost concern for radiation hardening for SEE.

To combat with such effects, designers employ techniques like shielding which is simple but adds weight to the system. Another limitation for shielding is that it is less effective for high energy radiation. Because of this the devices can be radiation hardened before being put into space. So, mitigation strategies need to be studied to reduce the threats of radiation for various devices [8].

2. Threat Reduction Strategies
At system level, the shielding can be effective for Total Ionization Dose (TID) and Displacement Damage (DD). Derating in power transistors can decrease susceptibility to SEB & SEGR. SEL can be decreased by limiting the operational temperatures. The probability of a SET can be reduced by operating at very lower frequencies through performance matching techniques making the device less susceptible to errors. Redundancy and opportunistic strategies are one of the most versatile techniques among mitigation strategies, yet they are not effective against degrading. Last among threat reduction strategies is to rely on the infrastructure which rely on the software to take care of the errors received. These strategies need not be effective to radiation threats at all times. In some cases, different strategies may be combined to achieve a better mitigation [9].

3. Radiation Hardening Techniques
Custom Radhard electronic designers rely on heterogenous solutions to enable failure proof trusted computing. To understand better the radiation hardening techniques are classified as physical and Logical to avoid data corruption. [10] Electronic devices can be physically radiation hardened by design (RHBD) through component configuration, layout and solutions for redundancy or by process (RHBP) using transistor bodies that are less sensitive to degrading effects. These can be done by insulating the substrate, using bipolar integrated circuits, radiation tolerant – SRAM, capacitor-based DRAM, using larger process nodes, selecting a substrate with wide gap and shielding using depleted boron. Logical radiation hardening techniques adapts techniques like error correcting memories, using redundant elements, hardened latches, using a watch dog timer etc.

3.1. Radiation hardened by design (RHBD)
Most frequently used techniques for RHBD are layout level techniques that provide partial protection by employing H-gate, T-gate, annular gate and STI (Shallow Trench isolation), circuit level techniques like TMR (Triple Modular Redundancy) used for mitigating SEU but incur large area overhead and high-power dissipation, system level techniques that employ ECCs for soft error tolerance. Circuit level RHBD memory cell is preferred over layout and system level as it provides more fault tolerance and less overhead [11].

Alessandra Camplani et al., observed that special design techniques can be used to improve the tolerance of devices to radiation. They noticed that annular gate geometry of edgeless transistors (ELT) help reduce the leakage current in NMOS devices when they are exposed to high TID. PMOS devices do not need ELT shape as they are not prone to current leakages. ELTs provide internal side of ring shape transistor used as drain with a reduced size and the external side is used as source of the
NMOS device. SEL can be prevented by using double rings around P-wells and N-wells with same type of biasing thereby reducing the current leakages, if any. At the same time, for use of ELT and ring guards large area of silicon is required [12]. Most of the studies on radiation hardened by design are on SEU hardened memory cells based on storage node redundancy and upset recoveries. There is no standard available for the validation of SEU immune circuits [13]. The research in [14] shows that the SEU cross section decreases with an improvement in scaling, while the LET is reduced. This has increased the multiplicity of multiple upsets (MBU & MCU). Especially for the work done on 6T memory cell, it is observed that the tolerance to radiation has improved with the increase in the cell area (1.2 to 1.5 times).

3.1.1. Layout Rules for RHBDMemory Cell. In the design of layout utmost care should be taken to make sure that the sensitive nodes maintain maximum distance within the memory cell and with the adjacent cells. Every cell has a n-well with a p+ ring along it. [15] To improve the nodal capacitance, lightly doped regions are filled with n type or substrate material to decrease the area with an increase in channel width. Highly doped regions that are connected to Vcc or GND are introduced between the sensitive nodes wherever there is free space. With the improvement in channel width, the LET threshold and critical charge induced can be improved. To reduce leakage (drain-to-source) current during dose irradiation, the channel length of n-transistors of the cell’s latch is increased 1.5 to 2 times [16] as shown in figure 2.

![Figure 2. Process options (a) Bulk CMOS, (b) SOI-CMOS and (c) SOS-CMOS.](image)

4. Radiation Hardened by Process (RHBP)
RHBP is the most fundamental way to minimize the impact of radiation [17]. In the designer perspective, for very high radiation environments, Radiation Hardened by process (RHBP) is preferred as it can provide immunity to both TID and SEE. In RHBP, the manufacturing process and transistor design is modified to make the base transistor radiation tolerant in such a way that the TID tolerance is very high, the device insensitive to SEE’s and with no Latchup. RHBP methods use SOI (Silicon on Insulator) or SOS (Silicon on Sapphire) processes for SEE mitigation. SOI technique is implemented with Silicon insulator – Silicon substrate to reduce parasitic device capacitance and resistance to latch-up.

SOS is a special case of SOI family of CMOS technologies and is a hetero-epitaxial process that grows thin layer of silicon on a sapphire wafer [18]. Compared to conventional IC’s, SOI and SOS chips can survive some 10’s (>10 krad) of magnitude greater. The main disadvantage of this procedure is in continuously decreasing the size and maintaining the insensitivity to another SEE’s. Also, RHBP applies specific materials and non-standard procedures to mitigate radiation effects. Another disadvantage is the cost and the availability of vendors. The Cost for RHBP is very high compared to RHBD. Often RHBD and RHBP are combined to achieve specific tolerance [19].

FinFET devices are replacing the planar bulk CMOS devices at Sub-22nm due to improved short-channel controllability, lower parasitics, lower leakage, and better yield. For example- CMOS technologies-based SRAMs have improved their performance over the years. [20] However, due to aggressive shrinking of transistors sizes, traditional planar SRAMs are more vulnerable to soft-errors caused by radiation. Adapting to FDSOI based FinFET technologies helps reducing soft error rate at
cell level primarily due to the presence of the insulating layer of buried oxide that isolates the n- and p-wells as shown in Figure 3.

Figure 3. FDSOI FinFET Particle Radiation Strike.

Commercial production has attested that FinFET’s are better and offer more control over channel compared to traditional CMOS devices. For radiation mitigation research has shown that FinFET DICE (Dual Interlocked Storage Cells) memory has a higher tolerance for SEUs of different amplitudes and long periods for both read and hold operations [21]. In Bulk FinFET’s, TID response is based on the charges trapped in the STI (fin). Electrical field inside the fin is affected by these charges. As the fin narrows down, the current leakage due to drain current degrades the device. Because of larger sensitive volume for charge deposition the charge collection in bulk FinFET is greater than SOI FinFET. This charge can be reduced by dual or triple well technologies. The charge collection in SOI-FinFET is observed to be 70% less than that of planar technologies. In Bulk FinFET’s the transients at drain and source are different while in SOI FinFET’s it is same [22].

5. NextGen Radiation Hardended Devices

Over the past decade many promising next generation nanoscale devices are being considered to implement circuitry. This is primarily due to aggressive scaling has resulted in drastic increase in the source-to-drain leakage and reduction in current drive [23]. To overcome the scaling drawbacks the popular nextgen devices are – Carbon Nano Tubes based FETs – CNTFETs, Nanowires.

Figure 4 (a) shows CNTFETs based devices use graphene-based CNT as channel instead of doped-Si substrate as channel like in most the classical devices. Due to ballistic transport of carriers and low resistive properties CNTFETs offer better performance at lower $V_{DD}$ with low-off current values and therefore are considered an excellent alternate to implement memory units. [24] compared logic gates, interconnect and memory circuits based on Single-Walled CNTFETs and FDSOI MOSFETs for power, performance and radiation robustness (SET and SEU). In this study, CNTFETs exhibited 45% better resilience to SET than MOSFET circuits with two orders of improvement on the energy-delay metric. This due to higher current density and less effects due to parasitic in CNTFETs than MOSFETs.
Figure 4. (a) CNTFET particle strike charge and (b) NW based Device Structure.

[25] compared the 5Ch-Nano Wire (NW) Gate All Around (GAA) with conventional FinFET structure as shown in Figure 4 (b). To match the current levels and device size 5-Ch nanowire FETs were stacked. GAA structure with larger oxide area and larger gate controllability showed less Vt variation compared to the conventional FinFETs. However, FinFETs were affected by variation VDD when low radiation was applied but no such affect was found on 5Ch NW. Because of better controllability the device electrical parameter was not affected due to TID and channel doping had little influence on TID.

6. Conclusion
The paper focuses on the various mitigation techniques for radiation hardening of electronic devices, which can be achieved in many different forms. The work presents radiation tolerance depends on semiconductor technologies, materials used and fabrication process. The main effort of the paper is to provide an quick overview in to the subject of radiation hardening with contemporary approach and with regard to promising devices of the future.

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