Multi-Core Processor Scheduling with Respect to Data Bus Bandwidth

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Abstract. The paper considers the problem of scheduling software modules on a multi-core processor, taking into account the limited bandwidth of the data bus and the precedence constraints. Two problem formulations with different levels of problem-specific detail are suggested and both shown to be NP-hard. A mixed integer linear programming (MILP) model is proposed for the first problem formulation, and a greedy algorithm is developed for the second one. An experimental comparison of the results of the greedy algorithm and the MILP solutions found by CPLEX solver is carried out.

Keywords: Multi-core processor · Data bus · Scheduling · Greedy algorithm · Mixed integer linear programming

1 Introduction

The goal of the paper is to investigate resource constraint scheduling problems that arise when developing a program for a multi-core processor. In this case, it is necessary to schedule the execution of software modules on the processor cores, taking into account the restrictions on the data bus bandwidth. The data bus is a part of the system bus that is used to transfer data between computer components, in this particular case, between the CPU and the random access memory (RAM). Different software modules need different amount of data flow via data bus, therefore in the case of simultaneous execution of several modules, each one of them can take longer time than in the case of single-thread execution. The problem of scheduling software modules on a multi-core processor w.r.t the limited bandwidth of the data bus is important for processor manufacturers and parallel software developing companies, since the more efficiently the data bus is used, the higher the software performance.

From the point of view of scheduling theory, the problem of allocating the software modules to processor cores with respect to the limited data bus bandwidth is similar to the scheduling problems with renewable resources (see e.g. [12]), but unlike those problems, in our case the resource constraint (data
bus bandwidth) does not exclude some infeasible combinations of jobs (software modules) but rather increases their execution times. A distinctive feature of our problem is that each job would be processed at different speeds depending on its requirement of the data bus bandwidth and the loading of the data bus by the simultaneous jobs on other cores.

There are a number of approaches to task scheduling with variable processing times in the literature. First of all, in the area of parallel software development for multi-core processors, such problems are usually solved using fast heuristics, which work in the online mode, i.e. the jobs arrive sequentially and only a limited number of jobs is considered in each moment. The task scheduling heuristics proposed in [10], [18] and some other works are based on the principle that tasks should be allocated on the CPU cores in a complementary fashion, so that the tasks with most different resource consumption requirements are co-scheduled for simultaneous execution (in [10], [18] such resources imply the usage of data bus bandwidth and the cache utilization at different levels).

The tasks scheduling method proposed in [7] is based on the co-run degradation coefficients, equal to an increase in the execution time of an application when it shares a cache with a co-runner, relative to running solo. In the case of dual-core CPUs, the threads may be represented as nodes connected by edges, and the weights of the edges are given by the sum of the mutual co-run degradations between the two threads. Then, under some simplifying assumptions, an optimal schedule may be found by solving a min-weight perfect matching problem. In the case of greater number of cores per CPU, the problem is shown to be NP-hard and several heuristic approximation algorithms are suggested. Although the methodology from [7] and the corresponding algorithms would be too expensive to use online, they are acceptable for offline evaluation of the quality of other approaches.

Authors of [17] propose a novel fairness-aware thread co-scheduling algorithm based on non-cooperative game to reduce L2 cache misses. The execution time of a thread varies depending on which threads are running on other cores of the same chip, because different thread combinations result in different levels of cache contention. In [16], the cache on each of $m$ chips is shared by $u$ cores on each chip. The execution speed of a job running on a chip depends on what jobs are placed on the same chip. The number of jobs is equal to the total number of cores, all the jobs start at the same time. It is proved that the problem is NP-hard and a series of algorithms is presented to compute or approximate the optimal schedules.

In the production scheduling applications, the problem formulations with variable processing times are also important, e.g. in [9], a coke production scheduling problem is considered, where jobs influence on the processing time of other jobs due to increased production unit temperature. The authors of [9] construct an integer programming model to minimize the makespan, propose several heuristics, including a genetic algorithm, and compare their performance.

In the scheduling theory, similar problem formulations may be found in the area of scheduling with controllable processing times. The models and methods
for the case of preemptive scheduling are surveyed in [15]. In [13], the problem of job scheduling on identical parallel machines is considered, where the processing time of jobs is controlled by allocating a non-renewable shared limited resource. It is proved that if job preemptions are allowed, then the problem of minimizing the makespan time is solvable in $O(n^2)$ operations. In the present paper, however, we consider a non-preemptive problem formulation. Since the data bus bandwidth is a renewable resource, we refer to [8] and [2] for the surveys on problems with renewable resources, where the resource allocations may vary over time. The case of discrete resources is considered in [2], and the continuous resources are considered in [8]. The latter paper contains a problem formulation similar to our formulation F1 considered below, however in [8] it is supposed that the amount of resources allocated to each job is limited, but continuous and decided by the scheduler at each moment of time. In our case, the jobs execution speeds are completely defined by the set of co-scheduled jobs on the other cores (or machines in the traditional scheduling terminology). In a recent work [1], the authors focus on assignment of shared continuous resources to the processors, while the job assignment to processors and the ordering of the jobs is fixed. These are the main differences to the problem considered in our paper. One more difference is that unlike [1], we make a continuous time assumption. The authors of [1] show that, even for unit size jobs, finding an optimal solution is NP-hard if the number of processors is a part of the input, however a polynomial-time algorithm for any constant number of processors and unit size jobs exists.

In the present paper, two mathematical problem formulations for the problem of allocating the software modules to processor cores are proposed with different levels of problem-specific detail and both shown to be NP-hard. A mixed integer linear programming (MILP) model using the concept of event points (see e.g. [4]) is proposed for the more detailed problem formulation, and a greedy algorithm is developed for the other one. A comparison of the greedy algorithm results and the MILP solutions found by CPLEX solver is carried out.

The paper has the following structure. Two problem formulations are proposed in Section 2. NP-hardness of both problem formulations is shown in Section 3. A mixed integer linear programming model for the first problem formulation is suggested in Section 4. The greedy heuristic for the second problem formulation is described in Section 5. Methods of real-life input data generation and testing are explained in Section 6. The results of computational experiments are presented in Section 7. Concluding remarks are given in Section 8.

2 Problem Formulations

Informally, our problem is to schedule execution of software modules (jobs) on a number of processor cores, while there is one resource of a renewable type, the bandwidth of the data bus, and the precedence constraints for execution of these modules are given as a partial order on the set of jobs, and the objective is to minimize the makespan. Here we assume that each module creates a uniform data flow through the data bus, so that the amount of information sent by a
module through the data bus in both directions (from CPU to RAM and back) is proportional to the fraction of the completed job (i.e. the ratio of the executed elementary operations of a job to the total number of elementary operations in this job). Examples of software modules with (almost) uniform data flow may be the computational routines with multiple repetitions of the same loop or copying large data arrays.

**Formulation F1.** There are \( m \) jobs, \( c \) processor cores. The jobs are performed with no preemption and do not migrate from one core to another during the execution. No more than one job can be performed on a single core.

For each job \( p \), \( p = 1, ..., m \), let \( s_p \) denote its processing time under ideal conditions. Here and below, by *ideal conditions* we mean job execution when no other job is performed simultaneously.

We will call a *configuration* any set of jobs which may be performed simultaneously on different cores, taking into account the partial order on the set of jobs (a configuration can not contain a pair of jobs where one job precedes another according to the partial order) and the restrictions on the number of cores. Let \( K \) denote the set of all configurations. Suppose that in zero configuration no job is performed. Clearly, the partial order on the set of jobs also induces a partial order on the set of configurations \( K \).

Let us call a *processing speed* of job \( p \) in configuration \( k \in K \) the ratio of the time of full execution of job \( p \) under ideal conditions to the time of full execution of job \( p \), if \( p \) was executed all this time in configuration \( k \). Throughout each configuration, the speed of all jobs is supposed to be constant, but the processing speed of a job may vary during its execution, depending on the configuration in which it is performed. The configuration can be changed in two cases: the first case is when one of the jobs in the current configuration has completely completed and the second case is when some job(s) is added to the current configuration. If the configuration is changed, the speed of those jobs that are still in progress may change.

So, for each configuration of \( k \in K \) we know which jobs it consists of. For each job \( p \) in configuration \( k \), the speed of its execution \( v_{pk} \) is known.

The problem consists in scheduling the jobs on the processor cores with the minimum makespan (i.e. the time of completion of all jobs).

Since the number of configurations can be very large (up to \( \sum_{i=0}^{c} \binom{m}{i} \), depending on the partial order), the problem formulation F1 can be simplified by introducing the assumption that the job execution speeds are calculated based on their actual consumption of the data bus. In practice, the job speed depends on a large number of factors such as the number of memory access channels for the processor, the number of processor cache levels and their free volume, the processor frequency and its temperature (depending on the specific processor and related components). Explicit consideration of all these factors is beyond the scope of this paper. Based on practice, we suggest another problem formulation which is based on the jobs usage of data bus bandwidth. This problem formulation can be written as follows.
Formulation F2. There are $m$ jobs, $c$ processor cores and one renewable resource, the data bus. Just like in Formulation F1, the jobs are performed without preemption or migration from one core to another, and a partial order on jobs is given. It is required to schedule the jobs on the processor cores with the minimum makespan.

Now we suppose that for each job $p$, $p = 1, ..., m$, the percentage of data bus consumption $b_p$ under ideal conditions is known. During the execution of job $p$, a smaller percentage of the data bus can be allocated than $b_p$ if other jobs are simultaneously performed on other cores. Denote by $z_{pk}$ the actually allocated percentage of the data bus to job $p$ in configuration $k$. In practice, the distribution of values $z_{pk}$ among the threads is very hardware-specific and depends on many factors, which we can not afford to take into account (see e.g. [11]). As a simple approximation, we assume that the data bus bandwidth allocation to jobs in any configuration $k$ may be found by Algorithm 1, described below. The speed $v_{pk}$ of execution of job $p$ in the configuration $k$ is then proportional to the ratio $z_{pk}/b_p$.

Algorithm 1. Calculation of data bus consumption for a given configuration

Step 0. Put the percentage of the free data bus $freePercent := 100\%$ (the entire data bus is free) and set the number of jobs for which the data bus is not allocated, $jobsCount$ to be the number of jobs in configuration $k$.

Step 1. While $jobsCount$ is not 0, do:

1.1 Calculate a percentage of data bus that can be allocated to each job: $percent := freePercent/jobsCount$.

1.2 If the configuration has such a job $p$ that $b_p < percent$, then put:

$z_{pk} := b_p$,

$freePercent := freePercent - b_p$,

$jobsCount := jobsCount - 1$.

If no such job is found, then put $z_{pk} := percent$ for each remaining job and $jobsCount := 0$.

Step 3. Output computed values $z_{pk}$.

This method of capacity allocation is different from the concurrent network flow allocation, well-known in multicommodity flow problems (see e.g. [14]), where the ratio of the flow of each commodity to the predefined flow demand for that commodity must be the same for all commodities. We expect that the capacity allocation represented by Algorithm 1 is more adequate to the case of data bus information flows because in this case a software module has no explicit way to communicate its flow demand to the system.

3 Problem Complexity

We will show that the decision versions in both formulations contain an NP-complete special case of MULTIPROCESSOR SCHEDULING problem [3] as a special case. Here is a formulation of this problem:
Given a set $T$ of tasks, number $w \in \mathbb{Z}^+$ of processors, length $l(t) \in \mathbb{Z}^+$ for each $t \in T$, and a deadline $D \in \mathbb{Z}^+$, is there a $w$-processor schedule for $T$ that meets the overall deadline $D$?

In [3] it is also proved that the MULTIPROCESSOR SCHEDULING problem remains NP-complete in the special case of $w = 2$.

**Proposition 1.** The problem of multi-core processor scheduling with respect to data bus bandwidth is NP-hard for both formulations F1 and F2.

**Proof.** The MULTIPROCESSOR SCHEDULING problem is a special case of the decision version of the problem of multi-core processor scheduling with respect to data bus bandwidth in Formulation F2 in the special case where: (i) jobs do not slow each other, (ii) there is no partial order constraint, and (iii) the set of tasks $T$ is equal to the set of jobs, assuming that the number of processors is the number of cores.

To prove the NP-hardness of the problem in Formulation F1, put the number of cores equal to 2. In this case, the number of configurations is $1 + m + \frac{m(m-1)}{2}$ and, therefore, the input size of the problem in question is limited by a polynomial of the input size of the MULTIPROCESSOR SCHEDULING problem. □

4 Mixed Integer Linear Programming Model

Consider a mixed integer linear programming (MILP) model for the first problem formulation. We define the concept of an event point similar to that introduced in [4]. In this paper, an event point characterises a time interval in which a single configuration is performed. It is defined by the number of the interval, its duration and the configuration used in it.

Let $P = \{1, ..., m\}$ denote the set of all jobs. The following set of parameters may be computed on the basis of an instance given in Formulation F1:

- $q_{pk} = 1$ if and only if job $p$ is performed in configuration $k$, 0 otherwise.
- $a_{ij} = 1$ if and only if configuration $i$ should run after configuration $j$, 0 otherwise.
- $T_{\text{max}}$ is an upper bound on the duration of any configuration at any event point.

Let us denote by $N = \{0, 1, 2, ..., e\}$ the set of all event points, where $e$ is the maximal index of event points, and introduce the problem variables:

- $t_{nk}$ is duration of execution of configuration $k$ at the event point $n$.
- $d_{nk} = 1$ if and only if configuration $k$ is performed at the event point $n$, 0 otherwise. For consistency of the MILP model, we assume that the zero configuration is performed at the zero point of events. Then $d_{00} = 1$ and $d_{0k} = 0$, $k \in K$.
- $y_{pn} = 1$ if and only if job $p$ started at the event point $n$, 0 otherwise.
Then the MILP model can be written as follows:

$$\min \sum_{n \in N} \sum_{k \in K} t_{nk},$$

(1)

$$t_{nk} \geq 0, \ n \in N, \ k \in K,$$

(2)

$$t_{nk} \leq d_{nk}T_{max}, \ n \in N, k \in K,$$

(3)

$$\sum_{k \in K} d_{nk} = 1, \ n \in N,$$

(4)

$$\sum_{n \in N} \sum_{k \in K} t_{nk}v_{pk} = s_p, \ p \in P,$$

(5)

$$\sum_{k \in K} d_{nk}q_{pk} - \sum_{k \in K} d_{n_{1,k}k1}q_{pk} \leq y_{pn}, \ p \in P, \ n \in N,$$

(6)

$$\sum_{n \in N} y_{pn} = 1, \ p \in P,$$

(7)

$$a_{k1,k2}d_{n1,k2}(n1 + 1) \leq a_{k1,k2}(d_{n2,k1} + (1 - d_{n2,k1})e)n2, \ k1,k2 \in K, \ n1,n2 \in N,$$

(8)

$$d_{nk} \in \{0, 1\}, \ y_{pn} \in \{0, 1\}, \ p \in P, \ n \in N, \ k \in K.$$

(9)

The objective function (1) defines the makespan criterion. Inequality (2) guarantees that the duration of execution of configuration $k$ at the event point $n$ is non-negative, and inequality (3) guarantees that the duration of execution of configuration $k$ will be zero only if this configuration is not executed at the event point $n$, otherwise it will be no more than $T_{max}$. Equality (4) means that one and only one configuration is performed at each event point, and equality (5) means that each job must be completed completely. Inequality (6) and equality (7) guarantee continuity of job. Inequality (8) sets a partial order between configurations. Expression (9) describes the range of the $d_{nk}$ and $y_{pn}$ variables.

**Proposition 2.** There is an optimal solution to MILP model (1)–(9) using $2m + 1$ event points, which defines an optimal schedule in Formulation $F1$.

**Proof.** Note that each event point corresponds to a change of configurations, and a change only occurs when any job (or several jobs) has begun or has ended. Suppose that at each event point only one job begins or ends, then it is easy to see that in this case $2m$ event points are needed. We also take into account that we need a zero point of events, the point at which no configuration is performed. This implies that in the case when no two jobs start and end at the same time, the number of event points is $2m + 1$. In any other case, a smaller number of event points would be required. □
Thus, in what follows we assign $e := 2m$.

It is worth noting that the solutions to MILP model $\text{(1)}$–$\text{(9)}$ provide the information about which configurations are performed at which event point, but do not contain the distribution of jobs to the cores. For scheduling the execution of jobs on the processor cores (as Formulation $F1$ requires), the following Algorithm $2$ is proposed which takes as input $k_1, k_2, \ldots, k_h$, configurations sorted by execution order, as well as their execution time $l_{k_1}, l_{k_2}, \ldots, l_{k_h}$ and the number of cores $c$. The algorithm returns the starting time $u_p$ and the completion time $f_p$ for each job $p$.

**Algorithm 2. Jobs scheduling on the basis of MILP solution**

**Step 1.** For each job $p$ from $k_1$ assign a free core and set $u_p := 0$

**Step 2.** For each $k_i, i = 2, \ldots, h$ do:

1. For each job $p \in k_i \cap k_{i-1}$, keep the same core.
2. For each job $p \in k_{i-1} \setminus k_i$ free the core on which job $p$ was performed, and set $f_p := \sum_{j=1}^{i-1} l_{k_i}$.
3. For each job $p \in k_i \setminus k_{i-1}$ assign a free core and set $u_p := \sum_{j=1}^{i-1} l_{k_i}$.

5 Greedy Algorithm

In view of the fact that the problem is NP-hard, a constructive heuristic has been proposed for formulation $F2$. In what follows, this heuristic is called the *greedy algorithm*, because it assigns jobs to all cores, not allowing them to stand idle, if possible. At each iteration, the algorithm selects a set of jobs (configuration) to perform, trying to select jobs so that when allocation the data bus between them, each job gets the most closest share of the data bus to the one it needs, but at the same time the maximum possible number of cores should be loaded. After selecting a configuration, the greedy algorithm determines the completion of which of the selected jobs will lead to switching the next configuration. To this end, firstly, the algorithm calculates what percentage of the data bus will be allocated to each job, and then, on the basis of these data, it determines the speed of processing the selected jobs. To give a detailed description of the greedy algorithm, let us denote by $k_1, k_2, \ldots, k_i, \ldots$ the sequence of configurations generated by the greedy algorithm, and denote by $\text{duration}_i$ the duration of the configuration $k_i$. Then the algorithm can be written as follows.

**Algorithm 3. Greedy algorithm**

**Step 0.** Put percentage of free data bus $\text{freePercent} := 100\%$ (the entire data bus is free); number of free cores $\text{freeCores} := c$ (all cores are free); $i := 1$; $k_i := \emptyset$; $\text{duration}_i := 0$; time remaining for job $p$ to completion under ideal conditions $\text{leftTime}_p := s_p$; a set of all jobs that have not started yet: $\text{jobs} := \{1, \ldots, m\}$

**Iteration $i$.** Repeat Steps 1–7:

**Step 1.** While $\text{freePercent} > 0$ and $\text{freeCores} \neq 0$, repeat 1.1.-1.2:
1.1. Find an admissible (not started earlier and not forbidden by the partial order) job \( p \in \text{jobs} \) for which the value \( |\text{freePercent} - b_p| \) is minimal. In other words, find such valid job \( p \in \text{jobs} \), which has the bus requirement closest to \( \text{freePercent} \). If no such job is found, then go to Step 3.

1.2. Put

\[
\begin{align*}
\text{freePercent} & := \text{freePercent} - b_p; \\
\text{freeCores} & := \text{freeCores} - 1; \\
\text{jobs} & := \text{jobs} - \{p\}; \\
k_i & := k_i \cup \{p\}.
\end{align*}
\]

Step 2. While \( \text{freeCores} \) is not 0, repeat 2.1.-2.2:

2.1. Find an admissible job \( p \in \text{jobs} \) that has the lowest data bus consumption. If no valid job is found, then go to Step 3.

2.2. Put

\[
\begin{align*}
\text{freeCores} & := \text{freeCores} - 1; \\
\text{jobs} & := \text{jobs} - \{p\}; \\
k_i & := k_i \cup \{p\}.
\end{align*}
\]

Step 3. If \( k_i = \emptyset \), then go to Step 8. Otherwise, distribute the data bus capacity between the jobs according to Algorithm 1, which gives the value \( z_{pk_i} \) – allocated percentage of the data bus to job \( p \) in configuration \( k_i \).

Step 4. Calculate processing speed \( v_{pk_i} \) of all jobs \( p \in k_i \) in configuration \( k_i \):

\[
v_{pk_i} := z_{pk_i} / b_p.
\]

Step 5. Determine which job will be fully completed first in the chosen configuration and set the duration of the configuration \( k_i \) equal to the duration of this job in the configuration \( k_i \):

\[
duration_i := \min_{p \in k_i} \{ \left\lfloor \text{leftTime}_p / v_{pk_i} \right\rfloor \}.
\]

Step 6. For all \( p \in k_i \), for which \( \text{leftTime}_p / v_{pk_i} \) is equal to \( \text{duration}_i \), set \( \text{leftTime}_p := 0 \).

Step 7. Put

\[
\begin{align*}
\text{freeCores} & := c; \\
\text{freePercent} & := 100\%; \\
k_{i+1} & := \emptyset.
\end{align*}
\]

For all \( p \in k_i \), for which \( \text{leftTime}_p / v_{pk_i} \) is not equal to \( \text{duration}_i \), put

\[
\begin{align*}
\text{leftTime}_p & := \text{leftTime}_p - \left\lfloor \text{duration}_i v_{pk_i} / s_p \right\rfloor; \\
k_{i+1} & := k_{i+1} \cup \{p\}; \\
i & := i + 1; \\
\text{freePercent} & := \text{freePercent} - b_p; \\
\text{freeCores} & := \text{freeCores} - 1.
\end{align*}
\]

Step 8. Distribute the jobs among the cores according to Algorithm 2.

It is not difficult to see that the greedy algorithm constructs a feasible schedule and may be implemented with time complexity \( O(n^2) \).
6 Methods of Data Generation and Schedules Testing

All calculations described in Sections 6 and 7 were carried out on a computer with 16 GB of RAM and Intel Core i7-8565U 1.80 GHz CPU. The operating system used was Windows 10 version 1909. The number of threads used for calculations did not exceed the number of processor cores, so the impact of other processes and the operating system itself can be considered insignificant. Turbo Boost and Hyper-threading options were turned off in order to be sure that the CPU temperature and other uncontrolled factors do not influence the jobs processing times. All the programs described below were implemented in C++. For the computational experiment, the following procedures taken from the Intel MKL (Math Kernel Library) are used as jobs:

– copying a vector to another vector,
– calculation of the sum of magnitudes of the vector elements,
– calculation of a vector-scalar product and adding the result to a vector,
– calculation of the QR factorization of a matrix.

The choice of such procedures is due to the fact that they consume the data bus in different ways. The input data to the procedures has different sizes (for procedures with vectors, this is the vector length, for procedures with matrices, this is the matrix size). For vectors, the dimensions from 10 to 70 million elements were used, for matrices, the dimensions varied from 1000 to 1300. Such sizes are due to the requirement that the jobs data should not be kept in the processor’s cache and their durations should not be too small (otherwise large measurement errors can occur) and they should not be too large (otherwise the measurements will take too much CPU time).

Input parameters for the generator:

– The number of jobs for which a schedule needs to be made. Values used: 4, 6, 7, 8, 10 (finding optimal solutions for 11 or more jobs takes about one hour, and for 13 and more jobs the generated model size is more than 26 Gb).
– Partial order to be generated for the jobs. Values used: (i) with a trivial partial order (no dependencies between the jobs), (ii) constructed at random (With probability 0.5 we decide that a job $p_1$ should be performed after job $p_2$. To avoid cycles, only pairs of jobs $(p_1, p_2)$ where ($p_1 > p_2$) are considered.), (iii) a binary tree, and (iv) one-to-many-to-one.
– Number of cores. Values used: 2, 3, 4.

6.1 Calculation of the Data Bus Consumption

All data, except for the data bus consumption by each job, necessary for the greedy algorithm, was taken from the examples generated in Section 6: the number of time units needed for each job, the partial order, and the number of cores. To calculate the percentage of the data bus consumed by job $p$, we used a program that works as follows:
Job \( p \) was started simultaneously in \( c \) copies (\( c \) is equal to the number of cores on the computer used), after that the speed \( s^*_{p} \) of the job was calculated as the execution time of job \( p \) under ideal conditions, divided by the execution time of job \( p \) along with \((c - 1)\) copies of the same job, then \( \frac{100\%}{s^*_{p}c} \) is taken as the desired data bus consumption.

If \( c \) copies of job \( p \) running simultaneously did not slow down each other, then this job was started with \((c - 1)\) copies of job \( g \), which has the highest data bus consumption. In this case, the percentage of data bus consumption by job \( p \) can be found as follows: \( 100\% - (c - 1)x \), where \( x \) is the percentage of the data bus required by job \( g \), multiplied by the speed of \( g \) in this configuration. If, in this case, no job has slowed down, then job \( p \) in any configuration does not affect the speed of other jobs, therefore, the data bus consumption by job \( p \) can be set equal to 0.

6.2 Experimental Measurement of Makespan for the Constructed Schedules

Using the generator from Subsection 6, we calculated the real speed of jobs in various configurations. However, the greedy algorithm calculates these speeds based on data on the consumption of the data bus by each job according to formulation F2. In order to understand how adequate the completion times are estimated in the MILP model using formulation F1 and in the greedy algorithm using formulation F2, and how the greedy solutions compare to the MILP solutions, a program code was written that simulated the execution of a given schedule on the processor cores.

In this testing program, threads are created in an amount equal to the number of cores of the simulated processor. Each thread is passed a job queue in the order in which they need to be executed. Before starting to perform the next job, the thread expects the completion of all previous jobs. If the core should be idle between performing two jobs, then a fictitious job is added to the queue between the corresponding jobs.

7 Computational Experiment

Schedules constructed using GAMS modeling system with MILP model \((1)-(9)\) were tested using the program described in Subsection 6.2. Fig. 1 shows the histogram of relative deviation (in percentage) of the makespan calculated by the CPLEX package from the measured makespan. In total, 964 schedules were tested, in all of them the deviation does not exceed 11\%, in 98\% of them it does not exceed 10\%, and in 73\% it does not exceed 5\%.

Schedules constructed by the greedy algorithm were also tested using the program described in Subsection 6.2. Fig. 2 shows a histogram of relative deviation (in percentage) of completion time reported by the greedy algorithm from the real completion time.
Fig. 1. Histogram of relative deviation of the minimum completion time in formulation F1 from the real completion time

Fig. 2. Histogram of relative deviation of completion time reported by the greedy algorithm from the real completion time
In total 984 schedules with different number of jobs, different partial orders, and different number of cores were tested. In most of the cases (95%), the makespan evaluation computed in greedy algorithm differs from that obtained in the experiment by no more than 10%, and in 73% of cases by at most 5%. In 100% of cases the deviation does not exceed 14%. Such results show a fairly high accuracy of evaluation of the jobs processing time in the greedy algorithm.

Let us denote by \( r := \frac{ga_{f2\_real}}{opt_{f1\_real}} \) the ratio of the real measured makespan of the greedy schedules \((ga_{f2\_real})\) in formulation F2 to the real measured makespan of the optimal schedules \((opt_{f1\_real})\) in formulation F1. Fig. 3 shows a box-plot diagram of \( r \) ratio for different numbers of jobs.

For each number of jobs, 192 schedules with different partial orders and number of cores were tested. It can be noted that the median ratio \( r \) for each number of jobs is close to 1.05, which allows us to conclude that the greedy algorithm is highly accurate. It is also worth noting that even in the worst cases, the makespan of greedy schedule exceeds the mistaken found by the MILP model in formulation F1 not more than by a factor of 1.4. In Fig. 3 one can also see that in some cases the solutions of the greedy algorithm in real life turn out to be faster than the optimal solutions, however, the difference does not exceed 10% and may be related to the error in calculating the input data of the problem and in testing of the obtained solutions.

Tables 2 and 1 show the CPU time of the greedy algorithm (Table 2) and the CPU time of the CPLEX package (Table 1) for different types of partial order and different numbers of jobs. The CPLEX package most quickly finds solutions
Table 1. Average CPU time of the CPLEX package

| No ordering | One to many to one | Random order | Bitree order |
|-------------|--------------------|--------------|-------------|
| 0.4 sec     | 0.2 sec            | 0.2 sec      | 0.2 sec     |
| 4.3 min     | 3 sec              | 3.6 sec      | 4 sec       |
| 13 min      | 26 sec             | 18 sec       | 1.5 min     |
| 16 min      | 6.3 min            | 32 sec       | 7.2 min     |
| 15.5 min    | 14.8 min           | 3.6 min      | 16 min      |

Table 2. Average CPU time of the greedy algorithm

| No ordering | One-to-many-to-one | Random order | Bitree order |
|-------------|--------------------|--------------|-------------|
| 2.5 µs      | 2.5 µs             | 2.6 µs       | 2.8 µs      |
| 3.9 µs      | 4.6 µs             | 4.4 µs       | 4.5 µs      |
| 4.8 µs      | 5.8 µs             | 6.2 µs       | 6 µs        |
| 6.4 µs      | 6.9 µs             | 7.7 µs       | 6.9 µs      |
| 8.1 µs      | 9.6 µs             | 11.4 µs      | 9.5 µs      |

for jobs with random partial order, since this type of partial order is usually more constraining than others, and most slowly for the trivial partial order. The greedy algorithm, on the contrary, works faster with trivial partial order, and slower for the random partial order. Still for all types of partial order and for any number of jobs it is much faster than CPLEX.

8 Conclusions

In the paper, the problem of multi-core processor scheduling was analyzed taking into account the bandwidth limitations of the data bus. Two problem formulations are suggested. A mixed integer linear programming model is proposed for the first problem formulation and the MILP solutions were found by CPLEX solver. A greedy algorithm for approximate solving the problem is proposed for the second problem formulation.

The schedules found by the CPLEX package and the greedy algorithm were tested using a program simulating the execution of jobs on the processor cores. The greedy algorithm has only a quadratic running time and a fairly high accuracy: a real-life testing showed that in 83% of the cases the makespan of a greedy schedule deviated from the optimal solution of MILP model less than by 10%, and in 60% of the cases the deviation was less than by 5%. We can conclude that the proposed algorithm of calculation of data bus consumption for a given configuration and the method of calculating the speed of jobs based on these data are close to what happens in real life.

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