ATLAS Upgrade Instrumentation in the US

Gustaaf Brooijmans\textsuperscript{a}, Hal Evans\textsuperscript{b}, Abe Seiden\textsuperscript{c}

\textsuperscript{a}Columbia University
\textsuperscript{b}Indiana University
\textsuperscript{c}University of California Santa Cruz

Abstract

Planned upgrades of the LHC over the next decade should allow the machine to operate at a center of mass energy of 14 TeV with instantaneous luminosities in the range $5-7 \times 10^{34}$ cm$^{-2}$ s$^{-1}$. With these parameters, ATLAS could collect 3,000 fb$^{-1}$ of data in approximately 10 years. However, the conditions under which this data would be acquired are much harsher than those currently encountered at the LHC. For example, the number of proton-proton interactions per bunch crossing will rise from the level of 20–30 per 50 ns crossing observed in 2012 to 140–200 every 25 ns. In order to deepen our understanding of the newly discovered Higgs boson and to extend our searches for physics beyond that new particle, the ATLAS detector, trigger, and readout will have to undergo significant upgrades. In this whitepaper we describe R&D necessary for ATLAS to continue to run effectively at the highest luminosities foreseen from the LHC. Emphasis is placed on those R&D efforts in which US institutions are playing a leading role.
1 Introduction

The LHC is expected to be the world’s Energy Frontier machine for at least the next 15 years. Data to be collected will allow much more detailed studies of the Higgs boson, the search for other new phenomena and the study of these if found, and in general push the sensitivity for new physics well into the multi-TeV range \[1\]. This physics program provides the challenge of simultaneously looking at many decay and production channels for a 125 GeV particle, resulting in final state particles of moderate transverse momenta, and also searching for particles at the highest mass scale that can be probed by the accelerator, which can result in very high momentum particles and large missing energy, all with very many superposed pile-up events.

The mass of the Higgs boson is ideal for the study of many decay and production channels, allowing an incisive test of our model for electro-weak symmetry breaking. However, present data samples are quite limited and all channels are still crudely measured. Providing much more precise measurements will require much more data. A major goal of the Phase-II upgrade of the LHC is to provide approximately 300 times as many events in the various Higgs channels as presently exist (and 10 times what will exist prior to the upgrade). This sample will also open up some new channels with small rates to provide a more comprehensive Higgs picture. In addition, to more fully complete the picture of electro-weak symmetry breaking, the measurement of W-W scattering at the TeV mass scale is very important. Acquiring such an event sample requires accelerator upgrades in luminosity, and detector upgrades that maintain trigger thresholds to enable collection of key events while preserving a high quality detector with broad capabilities to limit systematic errors on the quantities we wish to measure.

The presently planned machine upgrade will be to an instantaneous luminosity of \(5\sim7\times10^{34}\ \text{cm}^{-2}\ \text{s}^{-1}\) and would use luminosity leveling at a 14 TeV center-of-mass energy to provide the largest number of events. The goal is to collect 3,000 fb\(^{-1}\) of data in approximately a 10 year time span. The number of interactions will rise from the present 20 to 30 per 50 nsec crossing to at least 140 and possibly 200 every 25 ns.

The Phase-II detector will require fundamental upgrades in the trigger and detector electronics across all systems to maintain thresholds and efficiency, as well as an entirely new tracker to deal with the increased radiation damage, occupancy, and data rates. These improvements will be based on advances in technology over the more than 15 years since the present ATLAS detector was designed, and the vigorous ATLAS upgrade R&D program now ongoing. The various major parts of the Phase-II upgrade are described below with an emphasis on US efforts. A much more detailed discussion can be found in the ATLAS Phase-II Letter of Intent (LoI) \[2\] with more background material available in the Phase-I LoI \[3\].
2 Tracker Upgrade

2.1 General Design Goals and R&D Areas

The design of the upgraded ATLAS tracker is governed by the physics needs of the experiment and the desire to minimize cost. The design under consideration is based entirely on layers of pixel and strip silicon sensors, which can provide the granularity and radiation hardness required for the tracker. Minimizing cost and material in the tracking volume requires the fewest layers that can provide robust pattern recognition and track parameter measurement. This has been determined by simulations to be four pixel layers surrounded by five double-sided strip layers spread out over the 1 meter radius tracking volume inside the ATLAS solenoidal magnet. Maintaining an occupancy below about 1% per sensor element allows good matching of strip layers arranged to provide small angle stereo information with few fake tracks. In order to keep the occupancy below 1%, we must reduce each cell size, resulting in an increase in the number of readout channels by an order of magnitude compared to the present ATLAS detector. The inner radius of the less costly strip layers is determined by radiation damage and the desire to have at least half the signal strength from a passing particle, as compared to an unirradiated detector, after collecting 3,000 fb\(^{-1}\) of data.

To identify many of the physics signatures, the tracker must provide excellent momentum measurements for energetic leptons and establish that they are in fact isolated. The material in the tracker affects the efficiency and resolution in the detection of isolated electrons, due to bremsstrahlung and nuclear interactions. The performance of \(b\)-tagging algorithms based on displaced vertices also requires controlling the tails in the impact parameter measurement due to errors in pattern recognition and hadronic interactions within the active volume of the tracker. The upgraded tracker therefore must maintain careful control of the material inside the tracking volume, despite the larger channel count. This has significant implications on the mechanical design of the support structure, the powering scheme, and the cooling.

In addition new physics analysis techniques have emerged that place stringent requirements on future trackers. For example, the use of highly boosted jets require that track reconstruction work efficiently in very collimated jets, where particle tracks remain close to each other over long distances. This demands small pixels and thin sensors to avoid large cluster sizes.

An important lesson from the 8 TeV run is that tracking can be used to build powerful tools to mitigate the effects of pileup for a wide range of objects measured by other subdetectors. Therefore, another important requirement on the upgraded tracker is the need to provide fast momentum information on tracks to select events of interest at the first trigger level. Since the readout and reconstruction of all tracks for a first level trigger is presently beyond the state-of-the-art, the ATLAS plan is to only readout a fraction of the tracking detector (~5%) for participation in the first level trigger, chosen via regions of interest based on information from the calorimeter and muon systems. This requires high-bandwidth frontend and controller chips that allow for readout paths both for triggering and more general readout.

The large integrated fluences for Phase-II will require more radiation hard sensors than in the present ATLAS detector but also at a minimum cost. In the case of pixels the goal has been to develop larger detectors (for example 4cm × 4cm in area) that can be bump bonded to several (for example four) frontend chips, significantly reducing bump bonding costs. For the strip sensors, units that are about 10cm × 10cm allow cost minimization with further segmentation provided by reading out shorter strip segments (for example 2.5cm length) using hybrids and electronics located on top of the sensor. Maintaining the sensor signal after large fluences requires the collection of electrons. For most of the pixels and all of the strips cost minimization then determines that the sensor be of the n-on-p type. For the two very inner pixel layers, 3-D sensors, where readout collection columns are embedded in the silicon, allow very short collection distances and the highest radiation tolerance. The use of slim-edges for the sensors will avoid having to overlap them to maintain hermetic coverage, reducing material and the number of sensor units.

The issues described above lead to a number of major R&D areas. US groups have played a large
role in many of the analogous areas for the present ATLAS detector. Currently, three national lab groups and six university groups are playing a major role in the R&D program for Phase-II. Some primary areas in that program are:

- Development of minimum cost sensor assemblies in n-on-p technology, aimed at both the strip detector and outer pixel layers.
- Optimizing 3-D sensors for the two inner pixel layers. Other options for this part of the detector are diamond sensors or planar detectors that can run at rather high voltages. In addition new approaches, for example CMOS sensors, could have a large impact but require significantly more development and testing.
- Developing slim-edge sensors.
- Developing pixel frontend chips, with those for the inner two layers being most challenging and requiring very high performance CMOS technology.
- Development of strip front-end electronics, including features for first level triggering.
- Developing very light-weight supports for mass minimization.
- Developing novel powering schemes to save on cabling, mass, and cost.
- Developing chips which provide for interfaces to the data acquisition and also to the powering system.
- Developing fabrication schemes that minimize assembly time and complexity.
- Developing cooling systems with minimum mass, which are robust and allow running well below room temperature.

An additional area of importance is the optical fiber system, the optical transmission components, and read-out-drivers. This is an area where options from industry develop rapidly over time and we are mainly following options available commercially. However, high bandwidth readout is expected to be of great importance in moving the information from the sensors to a region at larger radius.

All of the newly developed items must be tested for radiation hardness (e.g. signal properties for sensors; speed, gain changes, and single event upset for electronics), which leads to a very demanding and time-consuming test program.

The next section presents the performance of the tracker we expect to be able to build given several more years of R&D. This assumes that the R&D projects listed above converge to construction-ready status over that time period. The R&D over the past few years and performance of the present detector provide some confidence that this can be achieved given adequate funding.

2.2 ATLAS Letter of Intent Tracker

Figure 1 shows the tracker that has been simulated and on which the following performance plots are based. It consists of four pixel layers and five double-sided strip layers in a long barrel, and a collection of disk layers to cover more forward rapidities. The use of a barrel that is much longer than in the present ATLAS detector leads to a reduction in material as well as pushing material to larger rapidities. The layout has been adjusted to maintain 14 precision measurements on nearly all tracks, required for good pattern recognition. Figure 2(a) shows the number of hits on tracks originating from the origin and also from 15cm along the beam-line, indicating the excellent coverage. Figure 2(b) shows the material traversed (in radiation lengths) by a high momentum track as a function of rapidity. The different sources
of material are indicated. The layout arranges for a minimum amount of material at rapidity below 1.6, with most of the services beyond this. Figure 3 shows the occupancy expected in the tracker for each barrel layer for the case of 200 interactions in a crossing.

Figure 1: Diagram showing the layout of the tracker presented by ATLAS in the Phase-II LoI.

Figure 2: (a) Number of hits on a high momentum track originating from the origin (solid) and 15cm from interaction point (points), broken down between pixel hits, hits on strip detector, and total hits. (b) The material traversed by tracks from the origin, broken down by source of material.

2.3 Performance Expectations

The tracker is designed for physics at up to 200 events per crossing. We present below some of the performance expectations. Figure 4(a) shows the expected momentum resolution for muons of three different transverse momenta. Despite the discrete layer spacing the tracker achieves a rather smooth distribution versus rapidity and improves on the present tracker. Figure 4(b) shows the ratio of reconstructed to generated tracks from $t\bar{t}$ events as a function of pileup for two different track selections: requiring track reconstruction with at least 9 hits per track (a), and with at least 11 hits per track (b). The choice of 14 hits allows us to achieve good performance (that is no increase in fake tracks with pileup) with some redundancy, for example with some missing hits (1 pixel layer and 1 double-sided strip layer). Figure 4(c)
Figure 3: Occupancy expected in the LoI tracker for 200 interactions per crossing.

shows the expected $b$-tagging performance for different levels of pileup as well as a comparison to the expectations for the present tracker, including the new Insertable B-Layer (IBL). The performance for $b$-tagging of the upgraded tracker (labeled ITK) with 140 events per crossing is approximately as good as that for the present tracker with no extra occupancy. This level of performance is also crucial for reconstructing $\tau$ leptons.
Figure 4: (a) Predicted momentum resolution for muons as a function of pseudorapidity for the new inner tracker (solid lines) compared with the current tracker (dotted lines) for three different values of the momentum. (b) Ratio of reconstructed to generated tracks from simulated $t\bar{t}$ events at various levels of pileup for two different track selections: requiring track reconstruction with at least 9 hits per track (b-a), and with at least 11 hits per track (b-b). (c) Expected b-tagging performance, the efficiency to tag a $b$-jet and related rejection factor for light-quark jets.
3 Calorimetry

Calorimetry at high-luminosity, high-energy hadron colliders faces a number of major challenges:

- Front-end electronics need to be radiation-tolerant and consume little power while achieving high-precision (typically 16-bit dynamic range) and high data transmission bandwidth. Furthermore, these usually need to be installed on-detector, i.e. in inaccessible locations that impose stringent reliability requirements.

- High radiation levels and particle fluxes, particularly in the forward regions, impose the use of technologies that are simultaneously very radiation tolerant and able to yield high-precision measurements in the presence of high background fluxes.

The value of high-precision calorimetry to accurately measure electrons, photons and hadronic jets has been well established by the discovery of the Higgs boson and e.g. precision measurements in top quark physics [1]. During Phase-II operation, particle fluxes and the average energy deposited in the calorimeters are expected to be typically five to ten times higher than specified in the LHC design values. Under these conditions it is certain that the front-end electronics will have to be replaced. This is due both to radiation damage and the need for ATLAS to upgrade the trigger system, with the latter requiring real-time performance capabilities that the current electronics cannot satisfy.

The ATLAS calorimeters are based on two technologies: liquid argon sampling for the electromagnetic and forward hadronic calorimeters, and scintillating tile sampling for the central hadronic calorimeter. In both cases, the front-end electronics currently send coarse data to the Level-1 trigger system while buffering the precision data for readout on Level-1 accept. Ongoing R&D work is aimed at exploiting technological progress to send the full precision data to the Level-1 trigger system for all beam bunch crossings.

The US has played a leading role in the development and construction of the initial ATLAS calorimeter electronics: most of the ASICs for the liquid argon front-end electronics were developed in the US, and the 1524 front-end boards were produced in the US. The liquid argon back-end electronics were initially designed in the US. For the TileCal, the US led the front-end electronics design and played a major role in their construction.

3.1 Liquid Argon Front-End Electronics

The main architectural difference between the existing readout system and the planned upgrade is the switch from an (analog) on-detector Level-1 pipeline to a free-running design in which signals from all calorimeter cells are digitized at 40 MHz and sent off-detector. This approach effectively removes all constraints imposed by the liquid argon calorimeter (LAr) readout on the trigger system, since full precision, full granularity data will be available and the latency and Level-1 bandwidth will become essentially unlimited. Furthermore, due to its minimal coupling to the trigger system, the new architecture will provide significant flexibility for further evolutions in the ATLAS trigger system or overall detector readout. It will be able to accommodate a trigger system with a low-latency, low-granularity Level-0 trigger stage just as well as a system with a high-latency, full-detector Level-1 trigger, or both. Figure 5 shows the readout architecture for Phase-II.

The front-end boards (FEB) perform analog shaping of the calorimeter signals, then sample the analog waveform at 40 MHz before multiplexing the digitized outputs for transmission over fast optical links. (The LAr trigger digitizer boards perform very similar tasks with somewhat worse precision and coarser granularity to provide a more manageable data volume for the Level-0 trigger.) Each FEB reads out 128 calorimeter channels and transmits data at approximately 100 Gbps. A total of 1524 FEBs are needed to read out the full calorimeter.
Figure 5: Phase-II readout architecture for the liquid argon calorimeters. The front-end and LAr Trigger Digitizer boards are located on-detector, and send the data over fast optical links to the off-detector ROD and Digital Processing System. The LTDB and DPS will be installed in the Phase-I upgrades in 2018.

The new front-end board architecture is designed to remove the bottlenecks inherent in the current boards by exploiting progress in technology, while maintaining the analog performance: 16-bit dynamic range (currently achieved with three gains at 12 bits each) and coherent noise below 5% of the incoherent noise level. The main functional blocks are: analog pre-amplification and shaping, production of (summed) analog signals for the LTDB, analog-to-digital conversion of all signals at a rate of 40 MHz, multiplexing and serialization of digital data, and transmission over high-speed optical links. Since there will be no Level-1 pipeline, the control logic will be limited to clock distribution and slow controls for configuration and calibration.

US R&D Efforts address all aspects of the necessary front-end electronics development. The analog preamplification and shaping stages will be integrated in a single ASIC. The Liquid Argon Preamp and Shaper (LAPAS) test-chip, designed by the University of Pennsylvania and Brookhaven National Laboratory, and fabricated in 2009 in IBM’s 8WL SiGe process, validated the design approach of implementing a wide dynamic range single ended preamp followed by low power differential shaping stages with multiple gains to achieve the required 16 bit resolution. An integral non-linearity of less than 0.6% was demonstrated in both the $1 \times$ and $10 \times$ gain shaping stages and measurements of ionizing radiation indicated robust performance for TID in excess of 1 MRad [4]. Less expensive SiGe process alternatives are currently being explored: IHP SG25H3P and IBM’s 7WL.

The requirements on the ADC are a large dynamic range (16 bits can be achieved using three gains and 12-bit ADCs if needed) and precision (at least 12 bits), low power ($< 100$ mW/channel), high speed (40 MSPS), small footprint (128 channels on a 50 cm-wide board) imposing serialized outputs, and substantial radiation tolerance. Many commercial devices meet most of these criteria but are very sensitive to single event upsets (SEUs). Irradiation tests are being performed to verify if recent devices are suitable.

In addition to radiation tolerance, ASIC solutions have lower latency and power consumption. The former aspect is crucial if the signals are to be used in the Level-0 or Level-1 trigger systems. A recent test chip (nevis12, developed at Columbia Universitys Nevis Labs) in IBM CMOS 8RF (130 nm) technology uses four 1.5-bit pipeline stages followed by an 8-bit SAR. The output data are serialized at 640 Mbps.
A predecessor has allowed to demonstrate analog performance of the pipeline part at least equivalent to that of a commercial 12-bit ADC together with excellent radiation tolerance, and early test results from nevis12 are promising. Full testing will be completed in 2013 to confirm its analog precision, radiation tolerance, and determine the optimal operational parameters. The power consumption is expected to be approximately 40 mW/channel (40% of typical COTS ADCs) and the latency 65 ns (100 ns less than the typical COTS pipeline ADC). Figure 6 shows a schematic diagram of the nevis12 chip.

After digitization, the raw data produced on a FEB represents $128 \times 14$ bits (including two gain scale bits) $\times$ approximately 40 MHz, or about 72 Gbps. Conservatively assuming 25% overhead for control words and encoding, each board needs to multiplex, serialize and transmit 90 Gbps of data, leading to a total data transmission rate of 140 Tbps for the full calorimeter. A radiation-tolerant serializer in 250 nm silicon-on-sapphire technology able to run at 8 Gbps has already been developed by Southern Methodist University, and with a newer process, speeds of 10 Gbps should be achievable. It should therefore be possible to use a single 12-fiber ribbon to transmit the data produced by each FEB.

Further US ASIC R&D plans include: the production of a quad-channel 12-bit ADC, a 5.5 Gbps multiplexer and serializer chip and a 5.5 Gbps laser driver chip for the Phase-I upgrades; developing a 16-bit dynamic range (12-bit precision) ADC which could possibly incorporate the pre-amplification and shaping stages; incorporation of the ADC and high speed (5-10 Gbps) output serializers.

An oft-overlooked but crucial issue is the power distribution to the front-end electronics. The powering concept for Phase-II is based on a distributed power architecture with crate-level main converters providing 48 V and board-level point-of-load converters (POL). Modular main converters with 1.5 kW per module are under development with conversion efficiencies above 80%. Operation in external fields up to 300 Gauss, as present at the location on the LAr detector, has been successful. POL converters need to operate in even stronger magnetic fields, which prevents the usage of magnetic materials for inductance cores. Several developments of air-core based POLs are currently ongoing at Brookhaven National Laboratory and different technologies, based on SiCMOS and GaN, are under study.

### 3.2 Tile Calorimeter Front-End Electronics

The goals of the Tile Calorimeter Phase-II upgrade are to increase the radiation tolerance of the front-end electronics and to maximize the resolution and configurability of the tower triggers by sending all tile cell data to the sROD off-detector. This is feasible with the advent of $> 10$ Gbps optical communications.

Achieving these goals requires replacement of all the on-detector electronics as well as the sROD off-detector readout. Preservation of data integrity is achieved in three stages. The first line of defense is achieved by using better radiation tolerant components. Next, there is the creation of redundancy in the on-board electronics so that data is preserved if one power supply or microprocessor fails. Additionally, tile cells are read out by two phototubes sent to separate readout channels. Finally, error correction is employed in the serial communication scheme. An overview of the tile electronics system is shown in the Figure 7.

In the upgraded scheme, the on-detector electronics are housed in a mechanical drawer on which are mounted phototubes, an amplifier/shaper card (which might also digitize the signal), a Main Board which distributes low voltage and control signals, holds the ADCs, and routes data to a high-speed Daughter Board where the error correction and communications processing occurs. Additionally, the drawer houses a High Voltage control card for the phototubes. The Main Board is a complex 69 cm PCB of 14 layers, currently prototyped by the University of Chicago group. This board must handle all controls, signal digitization, and timing delays.

Integrity of the Low- and High-Voltage systems is paramount to the reliability of the Tile system, and both have been a source of problems in the past. The Argonne group has undertaken to redesign both systems. Their earlier redesign of the low-voltage modules for the current detector reduced noise and increased radiation tolerance by an order of magnitude.
Figure 6: Schematic diagram and photo of the nevis12 chip: a dual channel, 12-bit ADC test chip.
The Daughter Board preserves the philosophy of redundancy, with each half handling 6 phototubes with a separate Kintex-7 FPGA. The DB handles the high-speed optical communications, which is currently envisioned to occur using radiation tolerant 40 Gbps optical modulators. This communications pipeline will send all tile cell data to the sROD at 40 MHz for recording and formation of a digital trigger. An additional benefit of the optical communication of the trigger (as opposed to the current analog tower sum sent over 70 m cables) is much lower noise, allowing for better jet trigger turn-on resolution.

The Argonne and Chicago groups are also conducting R&D on optical communications. At ANL, modifications of a Luxtera modulator-based optical transmitter are being studied and prototypes will be radiation tested. Modulators are faster than commercial vcsel-based transmitters, achieving transmission rates of greater than 10 Gbps with very low error rates and likely high radiation tolerance. Use of a modulator rather than a vcsel transmitter could reduce system cost considerably. The University of Chicago group is setting up a radiation test facility at FNAL to study the single event upset rate in the optical transmitters and FPGA controls. This test facility will simulate the HL-LHC cavern environment.

Currently R&D is being conducted on three potential front-end amplifier/shaper boards. These boards process the phototube signal and send it to the Main Board, control the calibrations via charge injection and also the calibration achieved using a Cs source (this requires a slow integrator). A redesign of the current 3-in-1 card has been prototyped by the University of Chicago group and has been shown to be radiation tolerant and extremely linear; this card sends LVDS analog data to ADCs on the Main Board.

Two alternative front end boards are also being studied. These are ASIC-based with internal ADCs. One version is a joint effort of the Argonne ATLAS group and the FNAL CMS group to produce a new version of the QIE ASIC. This chip integrates the input current and digitizes in 4 gain ranges. The other ASIC R&D uses the current conveyor concept to digitize three gain ranges and incorporates a custom radiation tolerant ADC. The decision on which front-end card to be incorporated in Phase-II will only be made after beam testing of all three options.

![Figure 7: Tile electronics in Phase-II.](image)

### 3.3 Off-Detector Electronics

The main tasks of the off-detector electronics for the calorimeters are the reception of digitized data from the FEBs, data filtering and processing, as well as data transmission to the trigger and DAQ systems. The total input data rate for the LAr off-detector electronics amounts to about 140 Tbps.

The central components will be Read-Out Driver boards (ROD) implemented in ATCA standard. These receive the data using serial optical links on multi-fiber ribbons. Conversion to electronic signals is performed by commercial components and deserialization is handled by fast FPGA transceivers. The RODs will apply digital filtering using FPGAs to calculate calibrated energy deposits together with the signal time for each cell as well as signal quality criteria. The digital filtering will correct for electronic and pile-up noise and will be adjustable to the expected high-luminosity conditions by parametrized FPGA algorithms. The RODs will buffer the processed data in digital memory blocks according to
the number of hardware trigger levels and their corresponding trigger latencies, until data are eventually transmitted to the DAQ system. The data from the individual LAr cells are further processed by the RODs in order to provide input to the Level-1 hardware trigger. The signal processing may go beyond simple sums of cell energy or transverse energies. More complex algorithms like the extraction of features of electromagnetic shower shapes or fast tagging of $\pi^0 \rightarrow \gamma\gamma$ signals using the finely segmented first calorimeter layer may be possible given the availability of the full granularity of the LAr calorimeters. The detailed algorithmic layout is the subject of on-going R&D, which will take into account how many channels can be concentrated in one processing FPGA and the latency required by the trigger system.

US R&D activities at Brookhaven National Laboratory, the State University of New York at Stony Brook and the University of Arizona tackle all aspects of this work: use of fast, small form-factor optical transceivers, data handling and processing in high-end FPGAs, and optimal exploitation of the ATCA standard for this application. It should be noted that by going to ATCA, only six racks will be needed to read out the full LAr calorimeter, to be compared with the 17 VME crates currently installed, even though the data volume will have been multiplied by more than 50.

For the TileCal, the groups at Michigan State University and the University of Texas at Arlington are central to this effort. They are working with engineers at CERN and IFIC Valencia to prototype the system and devise detector control protocols.

### 3.4 Summary of Main Calorimeter R&D Areas

Areas in which US groups are playing a leading role are listed below.

1. **Analog Signal Processing**: The liquid argon calorimeter signals need to be amplified and shaped to reduce sensitivity to pile-up and electronics noise. ASIC design efforts based on silicon-germanium bipolar technology have shown amplification and shaping can be integrated in a single chip without compromising signal quality.

2. **Analog to Digital Conversion**: The large number of channels and stringent specifications make ASIC ADC solutions very attractive and cost effective. Integration of additional, ATLAS-specific functionalities will allow to further optimize the readout architecture.

3. **High Bandwidth Data Transmission**: The ATLAS calorimeters will transmit over 200 Tbps of data off-detector in Phase-II. Low power, radiation tolerant data transmission will be key to realize this on the front-end, while highly integrated solutions (optical links on FPGAs) would be very attractive off-detector.
4 Trigger and Data Acquisition

Running conditions anticipated during Phase-II LHC operations cause significant stresses on the ATLAS Trigger and Data Acquisition (TDAQ) systems. Luminosities of up to $7 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, leading to an average number of proton-proton collisions per bunch crossing, $\langle \mu \rangle$, of approximately 200 every 25 ns, require major upgrades of the TDAQ in the areas of dataflow and event processing capabilities. Work has already started in evaluating technologies that will allow us to meet these challenges. Many of these solutions are expected to take advantage of advances in commercially available hardware yielding an upgraded system that is more uniform and easily maintainable than the current TDAQ, but that is also flexible enough to adjust to changes in our goals as understanding of the physics driving the upgrades advances.

4.1 Physics Motivation

Stresses on the TDAQ system at luminosities expected to reach $7 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ are one of the main motivations for Phase-II upgrades of the ATLAS experiment. In order to achieve the physics goals outlined in Ref. [1], the TDAQ will have to maintain or improve upon performances achieved in 2012 running and those foreseen to be realized in the ATLAS Phase-I upgrade program. A brief summary of trigger requirements needed to maintain sensitivity to important physics channels is given in Table 1.

| Channel | Trigger | Target Thresholds |
|---------|---------|------------------|
| $W, Z$  | single-lepton $e, \mu$ | $p_T \sim 20 \text{ GeV}$ |
| $t\bar{t}$ | di-jet | $E_T \sim 60-80 \text{ GeV}$ |
| $HH \rightarrow b\bar{b} \gamma\gamma$ | di-photon | $E_T \sim 10 \text{ GeV}$ |
| VBF    | single-lepton + forward jets | $E_T^{\text{jet}} > 50 \text{ GeV}$ |
| SUSY   | single-lepton + $E_T^{\text{miss}}$ | $p_T^{\ell} \sim 20 \text{ GeV}, E_T^{\text{miss}} \sim 150 \text{ GeV}$ |

All aspects of the ATLAS TDAQ system are impacted by these requirements. However one of the main drivers of the Phase-II TDAQ upgrade is the desire to maintain Level-1 trigger thresholds for isolated electrons and muons at around 20 GeV, with an accept rate of 20 kHz or less, for luminosities of up to $7 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Estimates of the Level-1 EM trigger rate vs. threshold are shown in Figure 8(a) for the EM trigger configuration anticipated in Phase-I. Even for isolated EM triggers, a threshold of 40 GeV or more would be required to achieve an accept rate of 20 kHz or lower. However, Figure 8(b) shows that raising the Level-1 lepton trigger thresholds from their current values (around 20 GeV) to the 40 GeV required to meet bandwidth limitations would reduce acceptance by a factor of 1.5–3 depending on the physics channel.

4.2 TDAQ System before Phase-II

The trigger architecture currently used by ATLAS and foreseen through the end of Phase-I running consists of three levels.

1. **Level-1 (L1)** uses custom hardware to construct trigger Regions of Interest (ROIs) based on information from the Calorimeters and Muon system and takes advantage of correlations between objects using a Topological Trigger Processor. During Phase-I running the Level-1 trigger system will generate trigger accepts at an average rate of 100 kHz, with a latency of approximately 2.5 $\mu$s. An overview of the L1 system during Phase-I operation is given in Figure 9(a).
Figure 8: (a) Projected EM trigger rates for the Phase-I trigger system at $\langle \mu \rangle = 115$, corresponding to $4 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$, as a function of trigger threshold. (b) Acceptance of muons from $t\bar{t}$, WH, and SUSY processes as a function of the true muon momentum.

2. Level-2 (L2) is implemented in software on a farm of PCs and constructs triggers using information from all ATLAS sub-systems, but only in ROIs identified by L1.

3. Event Filter (EF) runs on the same farm of PCs as L2, but has access to data from the full event and uses algorithms similar, if not identical, to those run in offline reconstruction. Trigger accepts from the EF at a rate of up to 1 kHz are foreseen in Phase-I.

L2 and the EF, which in Phase-I will run in the same CPU along with Event Building, are collectively referred to as the High Level Trigger (HLT). The ATLAS DAQ is centered around system-specific Readout Drivers (RODs) that collect data from the individual sub-system front ends (FE) on L1 accepts, and the common Readout System (ROSs) that provides this data on request to the HLT. The configuration of the DAQ system, as it is foreseen in Phase-I running, is shown in Figure 9 (b).

Figure 9: Functional diagrams of: (a) the L1 trigger system; and (b) the TDAQ in Phase-I. Note that in Phase-I EF, Event Builder, and Level-2 nodes will be implemented in the same processor.
4.2.1 Involvement of US Groups in the TDAQ

The US has played a strong role in the development and operation of the ATLAS TDAQ system. US groups are making major contributions to TDAQ effort in the following areas:

- Calorimeter and Muon sub-system electronics that provide data to the L1 trigger system;
- L1 Calorimeter Trigger upgrades in Phase-0 and Phase-I;
- the L2 Fast Tracker (FTK) trigger;
- the Region-of-Interest Builder;
- development of general-purpose, ATCA-based RODs;
- HLT and DAQ core software, particularly in the areas of dataflow and parallelization.

4.3 Phase-II Trigger Architecture

4.3.1 Rate Estimates for the Trigger at Phase-II Luminosities

The main issues in continuing to operate the Phase-I trigger system at luminosities up to \(7 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}\) (a factor of 2–3 higher than those foreseen in Phase-I) come from the L1 system. The Phase-I L1 trigger is constrained to operate with a maximum latency of 2.5 \(\mu\text{s}\) and a maximum accept rate of 100 kHz due to detector readout capability. This limits possibilities for coping with higher rates expected in Phase-II.

Estimates of the rates of Phase-I L1 leptons triggers have been made based on simulations of the functionality of the Phase-I electromagnetic calorimeter Feature Extractors and extrapolations of the performance of the muon trigger using existing data, including the expected performance of the new forward muon chambers, the New Small Wheels. These estimates indicate that a single electron/photon trigger with an \(E_T\) threshold of 25 GeV including hadronic isolation requirements would produce a L1 rate of 125 kHz. To achieve a manageable rate of 20 kHz would require raising this threshold to 40 GeV. For single muon triggers with a \(p_T\) of 20 GeV rates above 40 kHz are predicted, depending upon assumptions made about background conditions. In both of these cases, ATLAS physics goals would be severely compromised by L1 trigger restrictions. Estimates of expected Phase-I L1 trigger rates for a variety of different triggers at \(7 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}\) are given in Table 2\[2\].

4.3.2 Proposed Phase-II Architecture

The architecture of the Phase-II trigger system is driven by the ATLAS physics goals described in Ref. [1] and by constraints imposed by the detector sub-systems. As mentioned above, one of the most stringent physics requirements is the need to maintain efficient L1 single-lepton triggers with thresholds in the 20 GeV range. On the detector side, planned Phase-II upgrades relax the L1 rate and latency limitations from their Phase-I values of 100 kHz and 2.5 \(\mu\text{s}\). However, the inaccessibility of approximately 30% of the electronics of the MDT system’s Barrel Inner (BI) layer results in this system being the new bottleneck. The existing MDT electronics can operate with a latency of up to 20 \(\mu\text{s}\) at a maximum L1 accept rate of \(\sim 200 \text{ kHz}\).

As can be seen from Table 2, the total rate for L1 triggers that allow ATLAS to achieve its Phase-II physics goals using the Phase-I hardware exceeds the 200 kHz maximum by a factor of 2.5. The strategy proposed by ATLAS to deal with this involves creating a two-stage hardware trigger. Level-0 (L0), which will use the Phase-I L1 trigger hardware, accepts events at a rate of 500 kHz with a latency of 6 \(\mu\text{s}\). Following an L0 accept a new L1 system, using additional information and more sophisticated algorithms, will reduce the accept rate to the 200 kHz target with an added latency of 14 \(\mu\text{s}\). Thus, the
Table 2: Expected trigger rates at $7 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}$ for the L1 Phase-I and the baseline split L0/L1 Phase-II trigger systems. The EM triggers all assume the hadronic energy veto (VH) is used. For the photon and di-photon triggers it is assumed that the full granularity in the L1 calorimeter trigger will bring an additional factor 3 in background rejection power. The $\tau \tau$ trigger rate assumes a factor 2 reduction in the tau fake rate from the eFeX. The exclusive rates for $e\tau$ and $\mu\tau$ are not included as these will depend strongly on the exact trigger menu and trigger thresholds used. The rates for the JET and MET triggers are estimates based on an extrapolation of the current fraction of the trigger budget used for these triggers.

| Object(s) | Trigger | Estimated Rate |
|-----------|---------|----------------|
| $e$       | EM20    | 200 kHz        | 40 kHz         |
| $\gamma$ | EM40    | 20 kHz         | 10 kHz         |
| $\mu$    | MU20    | >40 kHz        | 10 kHz         |
| $\tau$   | TAU50   | 50 kHz         | 20 kHz         |
| $ee$     | 2EM10   | 40 kHz         | <1 kHz         |
| $\gamma \gamma$ | 2EM10 | as above | ~5 kHz |
| $e\mu$   | EM10\_MU6 | 30 kHz | <1 kHz |
| $\mu\mu$ | 2MU10   | 4 kHz          | <1 kHz         |
| $\tau \tau$ | 2TAU15I | 40 kHz | 2 kHz |
| Other    | JET + MET | ~100 kHz | ~100 kHz |
| Total    | ~500 kHz | ~200 kHz |

total latency from the L0/L1 system matches the 20 $\mu$s constraint from the MDT readout electronics. Four new features at L1, made possible by changes to the ATLAS detector in Phase-II, are foreseen to make possible this extra rate reduction.

1. **Tracking Information:** Association of tracks found using data from the silicon inner tracker (ITK) to calorimeter objects and to muons will provide a substantial reduction in the electron, muon, and tau trigger rates.

2. **Full Granularity Calorimeter Information:** All data from both the LAr and TileCal calorimeters will be available to the L1Calo trigger providing extra background rejection in (di)photon and (di)tau triggers.

3. **MDT Information:** Muon track momentum reconstruction, using the precise Monitored Drift Tubes (MDT), will be possible at L1. This is particularly effective at rejecting background for relatively low momentum muons.

4. **Topology:** The Phase-I L1Topo trigger will be enhanced to include new information from L1Track, L1Calo, and L1Muon.

The proposed Phase-II L0/L1 trigger architecture is shown in Figure 10. Its effect on estimated trigger rates is summarized in Table 2. More information on the individual elements of the system is given in the following and in [2].

**4.4 Calorimeter Trigger**

As described in Section 5, the entire calorimeter front-end and back-end electronics systems will be replaced in Phase-II, allowing digitization of all channels on every bunch crossing and transmission of
Figure 10: Functional diagram of the L0/L1 trigger system in Phase-II.

this data off-detector. The low-level calorimeter trigger in Phase-II will take advantage of this new, higher-granularity data and will be separated into two pieces. Level-0 (L0Calo) will approximate the functionality of the Phase-I L1Calo but will produce accepts at a much higher rate. Level-1 (L1Calo) will use the full-granularity calorimeter information and more sophisticated algorithms to process events at the average L0 accept rate of 500 kHz, up to a possible peak rate of 20 MHz.

The Phase-II L0Calo system will use electron and jet feature extractors (FEXs) as in the Phase-I L1Calo. However, L0Calo inputs will differ from those in Phase-I due to higher precision data being available at the trigger level in the new calorimeter readout scheme. As in Phase-I, HCAL data will be divided into regions of size 0.1×0.1 in η×φ, while four layers of LAr ECAL data (pre-sampler and three ECAL sampling layers) will be delivered in the “1-4-4-1” arrangement. In this arrangement, the first two ECAL sampling layers have a four times finer segmentation in η (0.025×0.1 in η×φ) than the pre-sampler and third ECAL sampling layers. All of this data is sent to the L0Calo on 4064, 10 Gb/s optical links, where it will be processed in the FEXs using firmware modified from the Phase-I versions, but running similar algorithms to Phase-I L1Calo.

The Phase-II L1Calo system will have access to full granularity calorimeter data in Regions of Interest (ROIs) defined by L0 and will therefore be able to deliver improved measurements of the energies and positions of trigger objects. For example, the second ECAL sampling layer has a full granularity segmentation of 0.025×0.025 in η×φ (compared to 0.025×0.1 at L0Calo), while the very finely grained first ECAL sampling layer (0.003125×0.1 in η×φ) could be used to suppress EM trigger backgrounds due to π⁰ → γγ decays.

A common area of R&D in both of these systems centers on the large data volumes (2 Tbps in L0Calo and 200 Tbps in L1Calo) sent to and among system elements.

4.5 Muon Trigger

Upgrades to the Phase-I L1Muon system required to retain p_T thresholds in the 20 GeV range for the split L0/L1 trigger scheme in Phase-II fall into three main categories. First, most muon readout electronics in the barrel and endcaps will need to be replaced to deal with the new trigger architecture. Second, tracking performance of the Resistive Plate Chambers (RPCs) in the barrel can be improved by using time-over-threshold information. Finally, precise hit information from the Monitored Drift Tubes (MDTs) will be
added to the L0 or L1 trigger logic to improve muon trigger momentum resolution, aiding in the rejection of low-momentum backgrounds.

For the MDTs, bunch-crossing identification for hits in individual tubes will be transmitted to the L0 or L1 trigger systems using high speed optical links. This information will allow \( p_T \) reconstruction at L0 or L1 with a quality similar to that of the current L2 muons, resulting in a reduction of the L1Muon rate by a factor of approximately three over much of the detector.

The L1Muon \( p_T \) resolution can also be sharpened by using the charge distribution in clusters of RPC \( \eta \) strips. This charge distribution can be accessed because the signal duration in the current RPC front-end electronics is correlated to the input charge. Measurements with a TDC could thus deliver the charge distribution in adjacent strips, from which a centroid could be formed. R&D is currently under way to evaluate the potential of this idea in detail.

### 4.6 Level-1 Track Trigger

Despite improvements to L1Calo and L1Muon in Phase-II, these systems alone are unlikely to entirely meet the physics goals of ATLAS. For this reason a crucial element of the ATLAS Phase-II upgrade program is the addition of a new trigger system at L1 using information from the Inner Detector. Charged particle tracks reconstructed by this L1Track trigger would be combined with EM objects from L1Calo and muon candidates from L1Muon to yield significant rate reductions. Current estimates, using simulation studies and extrapolations of current L1 trigger rates from data, indicate that reductions in the rate of more than a factor of five compared to L0 for 20 GeV single muon triggers and 18 GeV isolated single electron triggers using L1Track information are possible. Examples of these studies are give in Figure 11.

![Figure 11](image-url)

(a) Muon trigger efficiencies with a 20 GeV threshold as a function of true muon \( p_T \) after matching to a true muon, assuming a track trigger with different \( p_T \) resolutions. (b) Trigger rate vs L1 EM cluster \( E_T \) threshold for simulated minimum bias events with \( \langle \mu \rangle = 70 \).

Two possible L1Track architectures are currently under study. The baseline architecture, *RoI-Driven L1Track*, would provide all tracks in areas near L0 EM and Muon RoIs, while an alternate, *Self-Seeded L1Track*, would reconstruct all high momentum (\( p_T > 10 \) GeV) tracks independent of L0 RoIs.

In the RoI-Driven approach, Inner Detector data, buffered in on-detector electronics, is read out through associated Readout Drivers (RODs) only for those regions near a L0 EM or Muon RoI. This regional readout feature is already included in the design of Phase-II front-end readout ASICs for the strip tracker upgrade. The main challenge will be to perform the data readout and tracking within the...
Phase-II L1 latency budget of 20 µs. Preliminary studies indicate that this will be feasible.

The alternate, Self-Seeded, approach to L1Track requires a huge reduction in inner detector data volume. This could be accomplished by a combination of the use of fewer tracking layers in the trigger, and the early rejection of low $p_T$ tracks using cluster sizes and the inclination angle between the hits in stacked double strip layers. This approach requires major changes to the layout of the inner detector layers over what is currently assumed (see Section 2).

In both approaches L1Track pattern recognition might be done using associative memory (AM) technology similar to that being developed for the Phase-I ATLAS L2 Fast Tracker (FTK) [3]. R&D is ongoing to exploit novel ASIC design technologies, such as 3-D, to meet the experiment’s goals here.

4.7 Central Trigger System

Changes to the Central Trigger (CT) for Phase-II include development of separate L0 and L1 CTs, with topological capabilities included in each; and an update of the trigger, timing, and control (TTC) system. As can be seen from Figure 10, the L0CT and L1CT are structurally rather similar. The intent is to use the same technologies for these systems to ease design and maintenance requirements. For the upgraded TTC, the required topology matches that of a Passive Optical Network (PON). Studies are under way to assess the feasibility of using commercially available components for the final system.

4.8 High Level Trigger

In order to remain within limitations of 5–10 kHz on the total data recording rate, the Phase-II High Level Trigger (HLT) will need to provide a rejection factor of 20–40 beyond the L1 accept rate of 200 kHz. To achieve this goal, the HLT will employ offline-type selections and will rely increasingly on multi-object signatures. Advances in computer hardware performance over the next 10 years will help here, but upgrades to the HLT farm as well as improvements to selection software will also be required. One particularly promising area of development in HLT software involves the increased use of many-core architectures (e.g. GPUs) and parallelization of code. This will require significant changes to both the HLT framework and to the algorithms themselves. Another challenge will be to maintain commonality with offline software, a feature that substantially eases the burden of code development and maintenance.

4.9 Data Acquisition

Increased L1 accept rates (200 kHz) and larger event sizes (>4 MB) due to high levels of pileup at Phase-II luminosities indicate that at least a factor of four increase in bandwidth will be required of the ATLAS data acquisition system in Phase-II beyond that needed in Phase-I running. Additionally, higher values of pileup ($\langle \mu \rangle$ approaching 200 at luminosities of $7\times10^{34}$ cm$^{-2}$ s$^{-1}$) imply a significant increase in event processing time. Meeting these challenges will require changes in both hardware and software. Principal areas under study are: network technologies, online databases, information sharing mechanisms, and expert systems. Although it is premature to specify details of an upgraded data acquisition system, given the speed at which the relevant technologies are developing, a possible architecture for Phase-II readout is given in Figure 12. Figure 9(b) shows the current readout architecture for comparison. The Phase-II system aims for increased levels of commonality across detector sub-systems, taking advantage of emerging technologies and commercially available components. For example, aggregators feeding commercial, high-speed network switches allow data from different sub-systems to be read out into a common Readout Driver (ROD). Aside from simplifying issues of production and maintenance, this scheme could allow the possibility of re-organizing readout connectivity without physical re-cabling as well as leading to increased flexibility in terms of scalability and staging.
4.10 Summary of Main TDAQ R&D Areas

Aside from system-specific studies, the main areas of TDAQ-related R&D that are of general interest are summarized below. Work in most of these areas is just starting. However, most of the approximately 15 US institutes currently participating in TDAQ activities are playing strong roles in upgrade R&D planning.

1. **High-speed optical links**: Particular areas of concentration here are in the Calorimeter trigger system where approximately 200 Tbits of data must be transmitted per second in L1Calo; and in detector front-end to back-end links, which must operate at speeds of up to 10 Gbps in high radiation environments.

2. **Novel ASIC technologies**: For example, 3D technologies for use in Track Trigger Associative Memory chips.

3. **ATCA applications**: Standardized RODs implemented as ATCA cards could save costs by providing high performance, flexible platforms for a wide variety of readout applications.

4. **Parallelism and multi-core processing applications**: R&D is ongoing in using multi-threaded code and GPU architectures to improve performance and open new possibilities in the HLT and DAQ.

5. **High-speed switching networks**: Clever use of commercial high-speed network switches within a common readout framework could provide a flexible, cost-effective solution to sub-system readout needs.
5 Conclusion

The ATLAS Phase-II upgrade will allow exploration of the Energy Frontier to the highest masses as well as precision studies of the Higgs boson and any other new phenomena, fulfilling the promise of the LHC. To achieve this requires significant upgrades to the detector focused primarily on a new tracking detector, new calorimeter electronics, and a new TDAQ system. All of these upgrades to ATLAS require near-term R&D on sensors, electronics, and high bandwidth data-transmission components, areas in which US groups are already playing leading roles. Upgrades are also planned to the ATLAS muon system, particularly to the readout electronics and trigger systems. US groups have broad expertise in these areas and could contribute effectively to the Phase-II muon system upgrade effort were more R&D money to become available. Although the focus of this whitepaper has been on ATLAS and the LHC, many of the advances planned will be of general value to the community as they require mastering the latest technologies and exploring their limits.
References

[1] Anthony Liss and Jason Nielsen. Physics at a High-Luminosity LHC with ATLAS. ATL-COM-PHYS-2013-959, https://cds.cern.ch/record/1560796/, 2013.

[2] Philip Allport and Marzio Nessi. Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment. CERN-LHCC-2012-022, https://cds.cern.ch/record/1502664/, 2012.

[3] Philip Allport and Marzio Nessi. Letter of Intent for the Phase-I Upgrade of the ATLAS Experiment. CERN-LHCC-2011-012, https://cdsweb.cern.ch/record/1402470/, 2011.

[4] N Dressnandt, F M Newcomer, S Rescia, and E Vernon. LAPAS: A SiGe Front End Prototype for the Upgraded ATLAS LAr Calorimeter. ATL-LARG-PROC-2009-017, 2009.