3PO: Programmed Far-Memory Prefetching for Oblivious Applications

Christopher Branner-Augmon\textsuperscript{1}, Narek Galstyan\textsuperscript{1}, Sam Kumar\textsuperscript{1}, Emmanuel Amaro\textsuperscript{1}, Amy Ousterhout\textsuperscript{1}, Aurojit Panda\textsuperscript{2}, Sylvia Ratnasamy\textsuperscript{1}, Scott Shenker\textsuperscript{13}
\textsuperscript{1}UC Berkeley, \textsuperscript{2}NYU, \textsuperscript{3}ICSI

Abstract
Using memory located on remote machines, or far memory, as a swap space is a promising approach to meet the increasing memory demands of modern datacenter applications. Operating systems have long relied on prefetchers to mask the increased latency of fetching pages from swap space to main memory. Unfortunately, with traditional prefetching heuristics, performance still degrades when applications use far memory. In this paper we propose a new prefetching technique for far-memory applications. We focus our efforts on memory-intensive, oblivious applications whose memory access patterns are independent of their inputs, such as matrix multiplication. For this class of applications we observe that we can perfectly prefetch pages without relying on heuristics. However, prefetching perfectly without requiring significant application modifications is challenging.

In this paper we describe the design and implementation of 3PO, a system that provides pre-planned prefetching for general oblivious applications. We demonstrate that 3PO can accelerate applications, e.g., running them 30-150\% faster than with Linux’s prefetcher with 20\% local memory. We also use 3PO to understand the fundamental software overheads of prefetching in a paging-based system, and the minimum performance penalty that they impose when we run applications under constrained local memory.

1 Introduction
The rise of memory-intensive big-data applications such as machine learning \cite{51} has caused memory demands in datacenters to increase drastically \cite{11}. At the same time, the slowing of Moore’s Law means that memory costs (per GB) are no longer decreasing \cite{24, 29}. This has two consequences: first, applications often want to access more memory than is available on their local server and second, datacenter operators are incentivized to use their available memory as efficiently as possible. Recently far memory has emerged as a solution to these challenges, enabling applications to make use of unused memory elsewhere in a cluster \cite{4, 5, 19, 39}. By moving some data to far memory when local memory is full, far memory systems allow applications to run with less local memory and improve overall resource utilization.

Unfortunately, while existing far-memory systems \cite{4, 5} enable good performance at high local memory ratios,\textsuperscript{1} their performance degrades significantly as you decrease the amount of local memory. For example, with Fastswap, application runtime degrades by 11-226\% with 40\% local memory \cite{5}. A fundamental reason for this degradation is that far memory has higher latency than local memory (a few microseconds vs. about 100 ns). One way to reduce overhead is to more carefully decide what data to move from local memory to far memory when local memory is full, in order to reduce the number of memory accesses that stall on far memory. However, prefetching is a more promising approach because it has the potential to prevent all stalls on far memory. Unfortunately, state-of-the-art prefetching algorithms \cite{4, 17, 21, 22, 26, 41, 42} rely on heuristics, which are imperfect and often behave suboptimally. Therefore, they are not effective enough to fully mask the latency of far memory.

However, we observe that some applications—including linear algebra operations (e.g., matrix multiply), certain machine learning algorithms, and Fourier transforms—have a special property that admits heuristic-free, nearly optimal prefetching. This special property is that the sequence of memory accesses issued by such programs is independent of the program’s inputs. For deterministic applications of this type, we can determine the memory access pattern up front and then use it to guide prefetching when the program is run on any input.

This special property is called obliviousness and it has been studied primarily in the context of computer security \cite{18, 31, 50, 53}. Obliviousness is useful for security because it guarantees that no information about a program’s input is leaked via memory-related side channels. One recent prior work, MAGE \cite{25}, goes further and exploits this obliviousness for memory management, including prefetching. Though MAGE is limited to a family of cryptographic applications called Secure Computation, we observe that the implications of obliviousness for memory management extend beyond these security-related settings. In this context, we ask the question: can we enable nearly perfect prefetching of far memory for general oblivious applications, with little to no modification? To answer this question, we design and implement 3PO, a system that provides pre-planned prefetching for oblivious applications. 3PO builds on the operating system’s virtual memory subsystem, treating far memory as swap

\textsuperscript{1}The local memory ratio is the fraction of an application’s total memory that is allowed to reside in local memory.
space. Using 3PO, we (1) explore how much the oblivious applications mentioned above can benefit from programmed prefetching, and (2) push prefetching to the limit and study the fundamental software overheads of prefetching in a paging-based virtual memory subsystem.

In designing 3PO, we could not directly leverage designs from prior work. MAGE’s techniques and design are specialized to Secure Computation; it assumes that the program is written in a DSL and that it is acceptable to run it in a software interpreter. Other approaches to application-directed prefetching assume that the program is built with a particular compiler [33] or that the programmer provides hints to the prefetcher [36, 45, 48]. These approaches are not suitable for 3PO, which aims to support general oblivious applications with little to no modification. Instead, 3PO works in two phases, as follows. First, 3PO observes a program as it executes (with a given input) and generates a tape indicating which pages of memory need to be fetched as this program executes. Second, when the program is run later on a different input, 3PO prefetches pages from far memory, using the tape as a guide. Realizing this design required overcoming two main challenges.

3PO’s first challenge is generating a program’s tape. To do this, 3PO introduces a tracer, which records the pages accessed by a program as it executes. Existing tools based on dynamic binary instrumentation (DBI) [32, 34] can collect such a trace but are not efficient; they are known to take impractically long and result in a trace that is impractically large [25].

We address this challenge with two insights. The first insight is that, for the purpose of page-based prefetching, page-granularity traces (rather than access-granularity) are sufficient. This enables us to design an efficient in-kernel tracer that ensures that it incurs a page fault each time a new page is accessed and then records those page accesses in the page fault handler. We improve on this further with our second insight: to organize the trace not as a series of page accesses, but as a series of microsets—small working sets. With microsets, our tracer records sets of pages that are accessed consecutively, but does not record the complete sequence of accesses within each set of pages. This accelerates tracing and produces smaller traces. Microsets omit information about the exact sequence of page accesses within a microset, yet we find that we can use microsets that are up to hundreds of pages in size without degrading prefetching accuracy. 3PO additionally post-processes each trace to filter out pages that are likely to already be in local memory, leaving a more concise tape of pages to be prefetched at runtime. Note that the tape only specifies which pages to prefetch; 3PO lets Linux’s default eviction policy determine which pages to evict.

3PO’s second challenge is to ensure that prefetching is timely. 3PO does not have visibility into where the program is in its execution, so it is difficult for 3PO to know when it should prefetch the next page on the tape. Prior approaches circumvent this by having the application software manage memory (e.g., in a software interpreter [25]) or by relying on a compiler [33] or developer [37, 46, 49] to insert prefetch directives. But such techniques are unsuitable for supporting generic applications with minimal modifications, as 3PO aims to do.

To solve this problem, 3PO identifies pages in the tape that are guaranteed to page fault when accessed (because they are not present), and selects a subset of them as key pages. Key pages serve as synchronization points from which to initiate prefetching, so 3PO aims to space them evenly along the tape. Specifically, 3PO uses the page fault on each key page as a signal to select the next key page and to prefetch all pages that will be accessed in between. 3PO generalizes both its tracing and prefetching techniques to support multithreaded applications, with a separate tape and separate key pages for each thread.

We implemented a prototype of 3PO in the Linux 4.11.0 kernel, and evaluated it by combining the 3PO prefetcher with Fastswap [5], a state-of-the-art far-memory system. We found that 3PO can collect the memory-access trace of a program orders of magnitude faster than Intel Pin [32], a state-of-the-art tool for dynamic binary instrumentation. Using 3PO, we can run applications at much lower local memory ratios than with Linux or state-of-the-art prefetchers such as Leap [4], or run them at the same local memory ratio with better performance. For example, with 3PO, applications run 30-150% faster at 20% local memory than with Linux’s prefetcher.

Despite 3PO’s benefits, we find that we cannot completely prevent performance degradation at low local memory ratios. Overheads such as minor page faults on prefetched pages and TLB flushes for multithreaded applications still cause runtimes to degrade, for example by 0-300% at a local memory ratio of 20%. Even so, we believe that 3PO can be a useful tool for oblivious applications and that it sheds light on the fundamental limitations of how much performance we can hope to salvage with better prefetching.

2 Background

2.1 Far Memory

Far memory is an emerging datacenter design that allows operators to improve cluster resource utilization by leveraging the unused memory of remote servers or memory blades. In a typical setup, an oversubscribed machine fetches memory over a low-latency network using RDMA, [5, 19, 30] or even traditional TCP [39]. Applications can leverage far memory using custom APIs [3, 39] or in ways that remain transparent to applications [4, 5, 19, 40]; this transparency is achieved by using the existing virtual memory subsystem to swap pages. 3PO takes the latter approach because of its goal of generality. Indeed, some cloud operators argue that adopting specialized APIs for far memory in large scale clusters is impractical [27].

Running applications that swap at low local memory ratios can impose very high bandwidth requirements. In the worst case, if the allowed local memory for an application is close to zero, then the network bandwidth would need to be comparable to the local memory bus bandwidth—e.g., 800 Gbps on
one modern platform [7]—in order to achieve performance similar to that of only using local memory. Thus, running applications at low local memory ratios would be infeasible with older storage technologies such as HDDs, even with perfect prefetching hiding access latency, because they provide less than 5 Gbps [8]. In contrast, recent high-bandwidth non-volatile memory technologies can achieve tens of Gbps per memory module [23], while network bandwidth can exceed 100 Gbps. These technologies make it feasible to explore running applications with severely restricted local memory. However, as an application’s local memory ratio decreases, accurate and timely prefetching become more important.

2.2 Memory Management in Linux

Most modern processors manage memory at the granularity of pages, typically 4 KB each. When a program tries to access a page, the processor checks its page table entry (PTE) to see if it is marked as “present” in local memory, and the CPU trigger a page fault if the page is “not present”. The operating system is responsible for handling faults by fetching the faulted page from a swap device. When fetching pages from swap, Linux will also prefetch a dynamically-sized batch of pages that are consecutive (either in swap space or virtual address space) to the page that triggered the fault.

Linux’s paging mechanisms impose overheads on applications primarily in two ways. First, if an application tries to access a page that Linux failed to prefetch, it incurs a major page fault and must block until the page has been fetched from the swap device and mapped into the process’s address space. Second, if a page is present but not yet mapped into a process’s address space (e.g., because it was prefetched but has not yet been accessed), the first access to it will incur a minor page fault. Handling minor page faults entails some software overhead but typically does not require waiting on I/O. Most prefetching algorithms aim to eliminate overheads from major page faults, though as we will discuss (§3.3), oblivious applications provide an opportunity to reduce the overheads of minor page faults as well.

2.3 Application Requirements

3PO requires two main properties from applications: (1) obliviousness, meaning that application’s memory access patterns are independent of their inputs, and (2) deterministic memory access patterns at page granularity. Obliviousness originates from security contexts, where it is useful because it can guarantee that a program does not leak information via memory-related side channels [18, 31, 50, 53]. Instead, 3PO leverages obliviousness for its potential to improve prefetching performance. As a result, 3PO’s requirements for applications differ slightly from those for traditional oblivious applications. First, because 3PO fetches memory at the granularity of pages, it requires only page-level obliviousness rather than access-level obliviousness; an application that might reorder accesses within a page is sufficiently oblivious for 3PO. Second, 3PO can eliminate some inputs that might prevent an application from being traditionally oblivious (e.g., matrix size) by retracing the application for each of these inputs (e.g., generate one tape for each target matrix size).

We observe that many memory-intensive applications today meet these requirements. Examples include linear algebra operations such as matrix multiplication, determinant computation, and eigenvalue computation. In addition, Fourier transforms, and some graphics workloads (e.g., ray tracing, marching cubes) and machine learning algorithms (e.g., neural networks) also have these properties. 3PO targets these workloads.

3 3PO’s Design

3PO’s goal is to enable nearly perfect prefetching of far memory for oblivious applications, without requiring significant application modifications. To limit modifications to the application, we build 3PO into the Linux kernel and leverage Linux’s machinery for page-based memory management, rather than requiring applications to use a new API as in some existing approaches [3, 25, 39]. By “nearly perfect” we mean that memory accesses should almost never stall because they are waiting for memory to be swapped in, even when running applications with very limited local memory. Ideally 3PO would also achieve this with low overhead, allowing an application to achieve the exact same runtime when run with a low local memory ratio (e.g., 5%) as when run with 100% local memory. While 3PO is able to provide high accuracy, we find that it does entail some overheads which prevent it from achieving performance that is completely independent of the local memory ratio (§5.3).

There are two main challenges in designing 3PO: (1) obtaining a tape for an application describing which pages to prefetch, and (2) prefetching pages at the correct times during execution, i.e., ensuring that prefetching is timely. 3PO addresses these challenges with a three-step process, as shown in Figure 1. First, before actually running an oblivious program, a user executes it offline with sample input data, using 3PO’s in-kernel tracer to record the program’s sequence of memory accesses, or trace. When the user later executes their program online, many accesses in the tape will not trigger
prefetches, because the pages will be resident in memory from earlier accesses in that run. Thus 3PO’s second step is for the user to feed the trace through 3PO’s post-processor, which simulates which pages are evicted given a specific target local memory ratio, in order to generate a more concise tape of pages to prefetch during execution. This reduces overheads during prefetching, because the prefetcher does not have to scan through a long list of pages that are already present. Finally, the user can run their program with different input data under constrained local memory, with 3PO’s prefetch loading the tape and accurately prefetching according to it. Note that 3PO assumes that the amount of available local memory remains fixed throughout the execution of the program.

3PO uses Linux’s default eviction policy, which is similar to LRU. One could extend 3PO’s current design to use Belady’s optimal MIN [12] algorithm to precompute what pages should be evicted; we leave this to future work. Next we describe each step of 3PO—tracing (§3.1), post-processing (§3.2), and prefetching (§3.3)—in more detail. We describe how 3PO handles single-core applications, and then explain how we extend the techniques to multicore in §3.4.

3.1 Collecting a Memory Trace

When collecting a trace of a program’s memory accesses, 3PO aims to: (1) collect a concise trace, (2) collect it quickly, and (3) support general programs—programs that are not written in a specialized way for memory-trace collection. Existing general-purpose tracing options based on dynamic binary instrumentation (DBI) [14, 32, 34] have very high overheads and are slow enough that it is impractical to trace even small programs this way. This is because DBI-based approaches involve instrumenting most memory accesses which adds significant overhead, particularly for memory-intensive applications that can access memory very frequently. 3PO aims to retain the generality of DBI but at higher efficiency, by allowing most memory accesses to execute without software intervention. We achieve this benefit via two techniques we discuss next: page-granularity tracing and microsets.

Note that 3PO’s tracing techniques apply to regular applications as well as those that are data oblivious. Thus we believe that 3PO’s tracer is useful independent of 3PO, as a tool for helping researchers and developers better understand the memory-access patterns of their programs.

3.1.1 Page-Granularity Tracing

Because operating systems typically fetch memory (from storage or far memory) in units of pages, it is sufficient to record traces at page-granularity. By page-granularity, we mean that consecutive accesses to the same page are condensed into a single entry in the trace. This approach not only makes the trace smaller, but also allows us to leverage the processor’s hardware page table support to only perform tracing work when an application accesses a different page, rather than on most memory accesses.

3PO’s high-level approach to page-granularity tracing is to modify the page-fault handler to record all page accesses, and to force a program to incur a page fault each time it accesses a different page. This approach incurs many more page faults than a program would normally incur during execution, but allows 3PO to record a complete trace of page accesses.

More precisely, the tracer maintains an invariant over $S$, the set of pages whose accesses are recorded in a trace. The invariant is that of all pages in $S$, only the most recently accessed page has its “present” bit set in its page table entry (PTE). If the next access to a page in $S$ is to a different page than the most recently accessed page, the memory management unit will observe that the page is not present and raise a page fault. This allows 3PO’s tracer to record the access in the trace, mark this page as “present,” and mark the previous page as “not present”. Alternatively, if the next access to a page in $S$ is to the most recently accessed page, then the access proceeds without a page fault, thereby coalescing all consecutive accesses into a single entry in the trace with no additional tracer overhead.

This approach poses a challenge: how can 3PO distinguish between pages that are actually present but have been marked as “not present” by the tracer, and those that are truly not present? For example, when a process accesses a page for the first time, the Linux page fault handler needs to execute to allocate a page frame to back the page; simply setting the “present” bit in the PTE would cause incorrect behavior. To distinguish between these two cases, when 3PO’s tracer marks the PTE of a present page as “not present”, it also sets a special bit in the PTE, which we call the 3PO bit. On a page fault, the tracer can then check if the 3PO bit is set and use this to determine if it can simply set the “present” bit to true and return, or if this page must be handled by Linux’s regular page-fault handler.

The invariant of at-most-one-page-present-at-once poses challenges with instructions that can access multiple pages at once, such as movdqu or vscatterqpd. Though we relax this invariant below (§3.1.2), these instructions require that a specific set of pages are present simultaneously, which requires special care. For example, movdqu can require that up to two pages are present simultaneously. 3PO handles this case by recognizing when a sequence of page faults on the same instruction alternates between two pages (e.g., pages ABAB) and responds by temporarily marking both pages as “present” until the instruction pointer advances. This technique handles instructions that access two pages at once. It can be extended to support instructions that can access more than two pages, such as vscatterqpd; we leave this to future work.

The tracer provides a system-call-based interface for processes to specify when tracing begins and ends (§4); pages allocated outside of this interval will be excluded from $S$. Processes should invoke the syscall to start tracing as soon as possible during startup and before allocating the large memory buffers they will use for computation (e.g., on the heap), so that accesses to that memory will be included in the trace. This approach has tradeoffs: it may miss some page accesses
that need to be prefetched during execution, but it also allows tracing to skip memory accesses that occur only during process initialization. In addition, to speed up tracing and focus only on the large memory buffers used for computation, the tracer explicitly excludes stack pages from $S$ by checking which virtual memory area an access falls in. The tracer also ignores page faults due to instruction fetches by checking a bit in the page-fault error code.

**Assumptions.** The current implementation of $3PO$’s tracer assumes that during tracing, page faults only occur for two reasons: (1) self-induced page faults caused by marking present pages as “not present” or (2) page faults due to memory allocation. It may be possible for the tracer to handle other special minor page faults, such as those due to copy-on-write resulting from a call to mmap. This could be done by detecting a minor page fault on a page that has its 3PO bit set and is already marked as present, and then executing the regular Linux page-fault handler; we leave this to future work.

$3PO$ could similarly support tracing in the presence of major page faults, i.e., when a process’s memory does not fit in available local memory. While a page is swapped out of memory, Linux repurposes its PTE to record information about where the page is stored, so the 3PO bit may be overwritten and cannot be used to determine if a page is physically present or not. However, $3PO$ could leverage other mechanisms to detect if a page was swapped out, and still rely on the 3PO bit for pages that remained physically present.

**3.1.2 Microsets** While page-granularity tracing provides a significant improvement relative to a DBI-based solution, it still wastes time and space by recording information at significantly higher granularity than necessary for prefetching. In practice, when a program runs, more than one page will be resident in local memory at once, and tracing accesses for these already-present pages provides no useful information for the prefetcher. For example, if a program accesses the sequence of pages $ABABAB$, as long as the amount of local memory is at least two pages, $A$ and $B$ should remain present, so the last four accesses will not trigger prefetches and are therefore not useful to record.

Thus to improve efficiency, $3PO$’s tracer relaxes the invariant described above (§3.1.1) to allow multiple pages—a small microset of up to MICROSET_SIZE pages—to remain marked as “present” simultaneously. As shown in Algorithm 1, the microset starts out empty and each time a new page is accessed, triggering a page fault, the tracer adds it to the microset (line 10) and marks it as present (line 15). When a new page is accessed and the current microset is full (lines 4–9), the tracer adds all pages in the microset to the trace, marks them as “not present”, and resets the microset to empty. Then when pages in that microset are accessed again, they will incur minor page faults and be added to the microset again.

With microsets, each trace consists of a sequence of microsets where each microset represents a small working set of MICROSET_SIZE pages that are accessed consecutively, as illustrated in Figure 2. During tracing, only MICROSET_SIZE page faults are incurred per microset, and the remaining accesses proceed without software intervention. In most cases increasing the microset size yields a shorter trace, and tracing time decreases commensurately with the length of the trace.

![Figure 2: A sequence of accessed pages and resulting traces with different microsets sizes.](image)

How large should MICROSET_SIZE be? At one extreme, MICROSET_SIZE could be the number of pages in the smallest local memory size that we intend to use for this application. However, microsets this large degrade prefetching accuracy. The reason for this is that $3PO$ assumes that at runtime, Linux will not evict any page in a microset between when the page is first and last accessed as part of that microset; if a page was evicted during this interval, it would not be prefetched before its next access and would incur a major page fault. In practice this assumption holds as long as MICROSET_SIZE is not too large, so that pages within a microset are accessed close together in time. However, because Linux’s eviction policy is not strictly LRU, this assumption may not hold with very large values of MICROSET_SIZE. Overall we found that a wide range of microset sizes are able to strike a good balance, significantly accelerating tracing without degrading accuracy (§5.5); by default $3PO$ uses a MICROSET_SIZE of 1024 pages.

```python
microset = {}
def on_page_fault(page p):
    // record access to p
    if size of microset == MICROSET_SIZE:
        // start a new microset
        for p' in microset:
            append p' to trace
            clear present bit for p'
        microset = {}
    add p to microset

    // resolve page fault
    if p's 3PO bit is set:
        // skip normal page-fault handling
        set p's present bit
    else:
        // first access to p
        set p's 3PO bit
        run normal page-fault handling
    return
```

**Algorithm 1:** The main logic in $3PO$’s tracer.
3.2 Computing the Tape from the Trace

In principle, 3PO could accurately prefetch data at runtime using the memory trace produced in §3.1 directly, by interpreting it as a list of pages to prefetch. However, this would result in needlessly attempting to prefetch many pages that are already present in local memory from an earlier access. For example, in Figure 2 with a microset size of 2, if our local memory contained at least 4 pages, 3PO probably would not need to prefetch BA again, because they would still be in memory from the earlier accesses to AB. To avoid prefetching BA again, 3PO must traverse the page table to discover whether the pages are already local, adding overhead. In addition, despite the techniques in §3.1, the redundant accesses in the trace can make it large enough (e.g., gigabytes) that traversing it at runtime would consume significant memory and CPU cycles.\(^2\)

Therefore, we perform a \textit{post-processing} step on the trace to filter out pages that are likely to be in local memory and therefore do not need to be prefetched. Conceptually, this transforms the trace, which is a sequence of accessed pages structured as microsets, into a \textit{tape} describing what to prefetch at runtime. The tape allows 3PO to avoid extraneous prefetching and reduces the amount of memory the prefetcher must traverse at runtime (§5.5).

The set of pages that remains in memory at runtime depends on three factors: the prefetching algorithm, the eviction policy, and the amount of available local memory. Thus to generate a tape, 3PO’s post-processor traverses the trace, simulating 3PO’s perfect prefetching algorithm and an eviction policy with a particular target local memory size to determine which pages will not be present and will need to be prefetched. Ideally 3PO would simulate Linux’s eviction policy, since this is what will be used at runtime. Unfortunately, Linux’s eviction policy is quite complex and depends on the timing of different events [13], so it would be difficult to simulate it accurately. Instead, 3PO simulates a simple LRU eviction policy. Linux’s eviction policy bears some resemblance to LRU but differs in many ways; despite this we found that simulating LRU instead is accurate enough to avoid major page faults in practice (§5.5).

A user should run post processing to generate a separate tape for different local memory ratios they would like to be able to run their program at. However, we have found that tapes generated for a specific target local memory ratio can be used for executions at slightly larger local memory ratios; this adds a small runtime overhead from scanning through the extra pages on the tape, but does not degrade accuracy (§5.5). For example, a user could generate tapes at increments of 10% local memory, and round their local memory ratio down when choosing which tape to use.

3.3 Prefetching using the Tape

The goal of the 3PO prefetcher is to use the tape to bring pages from remote memory to local memory ahead of time, thereby avoiding major page faults. Though the tape provides information about exactly which pages need to be prefetched, it has no information about when to prefetch them. For example, a naive prefetcher could prefetch all of an application’s remote memory at once according to the tape as soon as the application started, but this would provide no benefit since the prefetched pages would be evicted to make room for subsequent prefetches, before any of them were accessed. Thus the main challenge faced by the prefetcher is to provide \textit{timely} prefetching. This involves two components. First, the prefetcher needs to stay \textit{synchronized} with the application, that is, it must know roughly where along the tape the application currently is in its execution. Second, the prefetcher must fetch each batch of pages \textit{in advance} so that the pages are likely to arrive by the time the application accesses them.

**Synchronization.** In order to provide synchronization, 3PO introduces \textit{key pages}. At any given time, the prefetcher maintains one key page for each application. When choosing a key page, 3PO chooses a page that will be accessed in the near future and that will trigger a page fault (because it is not currently mapped). When a page fault occurs on a key page, the prefetcher can resynchronize, updating its state about where the application is in its execution along the trace. In addition, the prefetcher will prefetch the next batch of pages and choose the next key page at this time. Though the prefetcher prefetches key pages, it does not mark them as present, so they will still trigger a minor page fault when accessed.

3PO chooses each key page by scanning forward along the tape to find a page that is guaranteed to trigger a page fault. Because the prefetcher fetches pages in batches, it starts looking for the next key page at the index of the current key page plus \texttt{BATCH\_SIZE}. However, it is possible that this page is already currently present and mapped, and will thus not trigger a page fault. This can occur because the post processing uses an approximate rather than an exact model of Linux’s eviction policy, or due to other threads executing concurrently (§3.4). In either case, the prefetcher scans forward along the tape after the current key page plus \texttt{BATCH\_SIZE}, checking if each page is mapped by consulting the page table, until it finds a page that is unmapped and uses this as the next key page.\(^3\)

**Prefetching in advance.** When a page fault occurs on a key page, the prefetcher needs to decide which pages to prefetch next. One approach to do this would be to start with the next page on the tape after the key page and prefetch all pages through the next key page. However, this approach does not prefetch pages far enough in advance and causes delayed hits [9]. These can occur due to either the latency overhead of fetching pages or due to bandwidth limitations. For latency, each page prefetch takes several microseconds to complete, so if the program accesses the first page after the key page in the

\(^2\)One could in theory prefetch the trace, but this would save memory at the expense of network bandwidth and would still consume CPU cycles.

\(^3\)In an alternate approach, you could always advance the key page by \texttt{BATCH\_SIZE} and force it to trigger a page fault by marking its PTE as “not present”, but this would add overheads from TLB shootdowns.
Even when work is statically partitioned across threads, perfect prefetching is challenging because threads may run in a non-deterministic order (e.g., thread A runs first during tracing but thread B runs first at runtime). This can cause the complete sequence of page accesses (across all threads) to also be non-deterministic. 3PO addresses this by handling each thread separately. 3PO collects a separate tape for each thread, post-processes each tape individually to generate per-thread tapes, and prefetches for each thread using its own tape.

While this is conceptually straightforward, additional challenges arise because multiple threads may access the same page. During tracing, if thread A accesses a page while it is already mapped due to an access by thread B, it will not trigger a page fault and that page will be omitted from A’s trace. This can cause a major page fault at runtime if thread A happens to access that page before thread B. 3PO addresses this by pinning all threads to the same core during tracing, so that multiple threads cannot concurrently access the same page. Counter-intuitively, this approach also makes tracing faster. This is because the tracer modifies PTEs frequently (§3.1), and each modification requires a TLB shootdown to invalidate any cached copies of this PTE on other cores. These shootdowns add significant overhead [6] and we found that it is much faster to trace programs on a single core, where we can leverage cheaper core-local TLB invalidations instead.

During post-processing, the target amount of local memory is a key input parameter, but 3PO does not know what fraction of the target local memory will be utilized by each of the N threads. 3PO addresses this by post processing each tape with one Nth of the target local memory. The intuition is that each thread is entitled to roughly one Nth of the memory if threads operate on disjoint memory and perhaps more if they share memory; we have found that this approach works well in practice (§5.5).

Finally, during prefetching at runtime, concurrent threads risk breaking 3PO’s synchronization mechanism, by violating the guarantee that each thread’s key page will cause that thread to incur a page fault. For example, suppose thread A chooses its next key page, but before thread A accesses it, thread B accesses that page. B will incur a page fault and will map A’s key page in the process’ virtual address space, preventing thread A from incurring a page fault when it accesses the page. Thus, the prefetcher will lose track of A’s position on its tape. 3PO takes special measures to prevent this from happening. Each time a thread B maps a page, it checks if this page is a key page for another thread A, and if it is, B advances A’s key page to the next unmapped page on B’s tape. To prevent a race condition in which one thread maps a page concurrently with another thread selecting that page as its key page, threads use a lock-protected variable to declare that they are about to map a page before doing so, so that other threads can identify the page as ineligible for use as a key page.
4 Implementation

3PO’s implementation consists of two parts. First, a kernel component comprised of 1400 lines of C code added to the Linux kernel memory subsystem; this code exposes a system call API to applications (Table 1), creates and manages trace files within the Linux kernel, and prefetches from remote memory according to a tape. Second, a trace post-processing tool written in 250 lines of Python. To use 3PO, a user first uses the sys_begin(RECORD) syscall to generate a trace for their application. Next, they run the post processor to generate a tape. Finally, they use the sys_begin(PREFETCH) syscall to load the tape and run the program with 3PO’s prefetcher. Users can also use the sys_begin(AUTO) syscall to avoid re-compiling their program between tracing and execution.

As we mentioned in §3.1.1, our tracer sets a 3PO bit and marks as “not present” the PTEs of the pages accessed by the traced application. Using the special bit this way is done carefully because if the kernel sees our special bit when it does not expect it, it could cause unexpected behavior or software bugs. Therefore, we also modified the kernel to make sure that when tracing, the 3PO bit is cleared before any kernel procedure reads a PTE, and is set again afterwards.

We considered leveraging multiple different existing far-memory systems for far-memory support; each has pros and cons. One system, Fastswap [5], offloads the work of choosing pages to evict and writing them to far memory to a separate “reclaimer core”, accelerating applications by freeing application cores from this task in most cases. However, Fastswap performs evictions synchronously, only allowing one outstanding write per core and wasting CPU cycles on evictions. As a result, applications are throttled because a single reclaimer core cannot handle all evictions for an application when evicting one page at a time, even at moderate local memory ratios. Another far-memory system, Leap [4], overcomes this by supporting asynchronous evictions, but does not offload reclamation to a separate core. To achieve the best of both systems, we built on top of Fastswap, but augmented it with support for asynchronous evictions, changing about 80 lines of code. This allows us to handle evictions for several applications with a single reclaimer core (§5.4).

For simplicity, 3PO’s implementation does not support transparent huge pages or address space layout randomization; we disable both when tracing and running applications.

We have tested our 3PO implementation with C++ binaries and with Python programs that use numpy (see Table 2). For the Python applications, we disable the garbage collector by calling gc.disable() at the beginning of the application to avoid its non-deterministic memory accesses. We experimented with another Python library, scikit-learn, but found that it yielded traces that are not oblivious, even for oblivious algorithms. One possible cause is that Python import statements trigger calls to mmap, which can map memory in different locations in different runs.

5 Evaluation

In evaluating 3PO, we focus on four main questions:

1. How do applications perform with 3PO, compared to with other prefetchers? (§5.1)
2. How do network characteristics impact prefetching performance with 3PO? (§5.2)
3. What prevents 3PO from achieving constant performance as we decrease the local memory ratio? (§5.3)
4. What are 3PO’s CPU and network requirements? (§5.4)
5. How fast are 3PO’s tracer and post processor, and how are speed and accuracy impacted by parameters such as MICROSET_SIZE? (§5.5)

Applications. We evaluate 3PO using the seven applications listed in Table 2. For each application, we measure its maximum memory usage (or resident set size) when running with unlimited local memory (using /usr/bin/time -v) and use this as the amount of memory it is allocated at a local memory ratio of 100%. The only modification we applied to each application was to invoke the 3PO syscalls.

Systems evaluated. We evaluate four systems:

1. 3PO, our proposed system. Unless stated otherwise, we use a MICROSET_SIZE of 1024 pages, BATCH_SIZE of 100 pages, and LOOKAHEAD of 400 pages. We found that these values performed well across different local memory ratios and across the applications we evaluated.
2. Leap [4], a state-of-the-art far-memory prefetcher.
3. Linux (Fastswap*), which consists of Linux’s default prefetching policy and our version of Fastswap, augmented to support asynchronous evictions.
4. Linux (Leap), which consists of Linux’s default prefetching policy using Leap’s Infiniswap-based RDMA backend [19] for fetching pages from far memory.

For all systems we use the most recent Linux kernel version they support; for 3PO and Linux (Fastswap*) we use version 4.11, and for Leap and Linux (Leap) we use version 4.4.125. Kernel versions <4.14 prefetch a window of pages that are contiguous to the faulted page in swap space. In versions ≥4.14 there is second prefetching policy that builds the window of pages to prefetch based on each application’s virtual address space. We did not evaluate the latter as none of the systems in our evaluation support it.

Experimental setup. We ran experiments on CloudLab. To evaluate how different network latencies and bandwidths impact performance, we used three different setups.

| Function          | Description                                                                 |
|-------------------|----------------------------------------------------------------------------|
| sys_begin(RECORD) | Begin recording a trace for the current process.                           |
| sys_begin(PREFETCH) | Begin prefetching with an existing tape.                                  |
| sys_begin(AUTO)   | If the kernel does not have a trace for this binary, generate it. Otherwise use existing tape to prefetch. |
| sys_end()         | Indicates end of trace recording or prefetching. Resources get freed here. |

Table 1: 3PO’s tracing and prefetching system-calls.
| Workload | Language | Max RSS (MB) | Description |
|----------|----------|-------------|-------------|
| dot_prod | C++      | 2000        | computes the dot product of two vectors using Eigen [1] |
| mvmul    | C++      | 2100        | multiplies a square matrix by a vector using Eigen [1] |
| matmul   | C++      | 400         | multiplies two matrices using Eigen [1] |
| matmul_p | C++      | 400         | same as matmul, but parallelized over p threads using static work partitioning with OpenMP [44] |
| sparse_mul | C++   | 1200        | multiplies two square matrices in a sparse representation using Eigen [1], matrices are 90% zeroes |
| np_matmul | Python  | 400         | multiplies two square matrices using the numpy library [2] |
| np_fft   | Python   | 4100        | computes a discrete Fourier transform using the numpy library [2] |

Table 2: Applications used for evaluation. Resident set sizes (RSS) are rounded to the nearest 100 MB.

Figure 4: Runtime vs. local memory ratio (see also Figure 5).

1. 25gb. For our default setup we use xl170 machines with Intel E5-2640v4 CPUs, connected with a 25 Gbps network. Reading a 4 KB page over this network takes 5.0 μs.
2. 10gb. While most prior far-memory research has focused on settings within a single rack, we also evaluate what happens if far memory is placed in a different rack, leading to higher latencies to access it. For these experiments, we use programmable Dell-S4048 switches to build networks where the xl170 machines are separated by multiple switches; these switches only support 10 Gbps bandwidth. Reading a 4 KB page takes from 5.5 μs with 0 intervening switches (10gb_0switch) to 15.2 μs with 4 intervening switches (10gb_4switch).
3. 56gb. Finally, we were unable to use the Leap kernel with the xl170 instances, so we evaluate Leap with c6220 instances instead. These instances have 2 Intel Xeon E5-2650v2 CPUs and are connected by a 56 Gbps Infiniband fabric where reading one page takes 3.4 μs.

We use Linux’s cgroup feature to limit the physical memory available to each application to induce memory pressure.

5.1 Application Performance

We begin by comparing the performance of 3PO and Linux (Fastswap*) for a variety of workloads and local memory ratios (Figures 4 and 5). Overall, 3PO provides a measurable improvement over Linux on most workloads. 3PO’s speedup varies depending on the application and memory ratio, with the speedup generally higher at lower memory ratios. This is because memory accesses go to far memory more frequently at low memory ratios, making performance more sensitive to the prefetching algorithm that is used.

Next, we evaluate how 3PO’s performance compares to Leap [4], a state-of-the-art prefetching system. Figure 6 shows the wall-clock runtime of the matrix multiply workload for all 4 setups, as we vary the amount of local memory from 100% (no memory pressure) to 5% (95% percent of resident set in far memory). Due to the previously mentioned Leap limitations, we use c6220 instances connected by a 56 Gbps network for this evaluation. In this case we find that Leap and Linux (Leap) perform similarly, and 3PO and Linux (Fastswap*) perform similarly, suggesting that prefetching algorithms have a minimal impact on runtime. This is to be expected due to the low-latency network used for this evaluation. The performance difference between Linux (Leap) and Linux (Fastswap*) is comparatively larger due to offloaded evictions in Fastswap*, which suggests that the choice of RDMA backend is more important than the prefetching policy for this hardware setup. Although Figure 6 only shows the results for sparse_mul, these same observations hold for other workloads as well.
5.2 Impact of Network Characteristics

In a datacenter deployment, far memory may be located in a different rack than the machine accessing it. This would result in higher latency to access far memory, impacting the performance implications of 3PO’s prefetching. To explore this, we measure the speedup of 3PO and Linux on the 25gb, 10gb_0switch, and 10gb_4switch setups.

The results, shown in Figure 8, show that 3PO has larger speedups on higher latency networks. This is because the cost of a major page fault is higher on such networks, causing perfect prefetching to have a bigger impact on performance. For some workloads, such as dot_prod, 3PO has a higher speedup on 10gb_0switch than on 25gb, even though 25gb has lower latency. The reason is that the network bandwidth becomes a bottleneck. Once the network is saturated, the latency of accessing far memory increases due to queuing delays, causing performance to degrade due to delayed hits. This affects both 3PO and Linux, causing the speedup of 3PO relative to Linux to decrease for the 10gb setup for these workloads.

Overall, at a 20% memory ratio, 3PO’s speedup compared to Linux ranges from 0.9× to 1.8× on the low-latency 25gb setup. On the higher-latency 10gb_4switch setup, the speedup increases to 1.3× to 2.5×.

5.3 3PO Overheads

In previous sections, we saw that performance degrades as the local memory ratio is reduced, even with 3PO. This section aims to characterize the sources of this degradation.

Figure 9 and Figure 10 show a breakdown of the performance degradation at 20% local memory on the 25gb setup into various components, to help determine the relative contribution of each. Extra user time refers to the amount of additional time spent in userspace when executing at 20% memory ratio. 3PO’s “3PO pf time” is about 2.1; it is cut off in the displayed graph.

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Eviction time, “miss pf time” and “delayed hit time” components are small for 3PO, leading us to conclude that 3PO can effectively avoid requiring the application to block on I/O. Therefore, these items do not significantly contribute to 3PO’s performance degradation at low memory ratios.

One cause of the degradation is overhead that 3PO does not reduce. For example, the extra user time is about the same for 3PO and Linux. Additionally, a significant amount of degradation, both for 3PO and for Linux, is due to software overheads in the page fault handler unrelated to 3PO. This could be due to reading and updating the state Linux maintains separate from the page table (e.g., swap cache, cgroups, etc.). Systems that implement prefetching in user space [39, 54] or via cache coherence [15] could avoid some of these overheads, though they may suffer from different overheads (e.g., “software page faults” cause high overheads from smart pointers [35, 39]).

Another cause of degradation is overhead of 3PO itself. 3PO’s routines for prefetching and prefaulting pages add overhead not present in Linux, and in some cases, these overheads eat away significantly at the gains from eliminating I/O time. This is consistent with other observations that software overheads can be significant compared to I/O that completes in microsecond timescales [10].

5.4 CPU and Network Requirements

3PO enables applications to run at low local memory ratios, but doing so requires extra network bandwidth and CPU usage to handle the high rates of prefetching and evicting. Here we measure the extra CPU cores and network bandwidth required to support low local memory ratios.

Like Fastswap, 3PO offloads evictions to a separate reclaimer core as much as possible; once the reclaimer is saturated, the application cores must assist with handling evictions. To measure when the reclaimer core or the network becomes a bottleneck in 3PO, we run multiple instances of our applications in parallel and for each memory ratio record the number of application cores that can successfully offload their evictions to the single reclaimer core (or spend less than 5% of their runtime handling evictions).

As shown in Figure 11, 3PO can handle at least 2 and up to 8 or more application cores with a single reclaimer core, depending on the network bandwidth and local memory ratio. The primary bottleneck in this experiment seemed to be the network, rather than the reclaimer core. This is evident from the fact that we can support more application cores with the 25 Gbps network than the 10 Gbps network. In addition, we observed that when application cores start handling evictions, the network bandwidth is close to saturation. However, these results show the worst-case behavior, because all applications start at the same time, aligning their peak bandwidth usage, which is about 50-100% higher than average usage. Thus, 3PO could support more applications if their start times were staggered. Because running applications at low memory ratios can impose significant network bandwidth requirements, 3PO is most suitable for making use of a moderate number of extra cores on a memory-constrained server.

5.5 Tracing and Post Processing

We now aim to understand how 3PO’s performance is affected by the microset size. Although the microset size is a parameter of only the tracing phase, the microset size indirectly affects the postprocessing and runtime phases via the size and quality of the produced trace.
Tracing Time (s) | Trace Size (MiB) | PostP Time (s) 
---|---|---
matmul | 4.74 | 17.3 | 2.18 
matmul_3 | 6.30 | 29.4 | 1.26 
mvmul | 2.91 | 8.16 | 1.77 
dot Prod | 2.94 | 8.00 | 1.77 
sparse_mul | 69.2 | 1110 | 102 
np_matmul | 4.98 | 16.2 | 2.02 
np_fft | 10.5 | 94.9 | 17.1 

Table 3: Tracing time, trace size, and postprocessing time for microset size 1024, presented to 3 significant figures.

The tracing time (Figure 12) and trace size (not shown) have similar patterns. Trace size has a similar pattern as tracing time because our tracing algorithm (§3.1.2) incurs page faults proportional to the size of the result trace. Postprocessing time (not shown) has a very similar pattern to trace size because the postprocessing procedure linearly scans the trace, operating on it in a streaming fashion. These three quantities (tracing time, trace size, and postprocessing time) remain the same or decrease as the microset size is increased, for each workload. This is because, when the microset size is doubled, the programs’ locality causes the number of accesses covered by a microset to increase by more than a factor of two. Programs that do not exhibit locality, like dot Prod, do not become more efficient to trace at larger microset sizes. Some workloads have one or more “cliffs” in the graph, at points where the microsets become large enough to contain larger aspects of the program’s structure. Similar trends have been observed in prior systems (e.g., lifetime curves [16]).

The size of the postprocessed tape (Figure 13) follows a different pattern—for most workloads it is flat, with a cliff at high microset sizes. This is because much of the unnecessary accesses preserved at low microset sizes are “filtered out” by the postprocessing. Thus, the postprocessing allows the tape to be small even at small microset sizes, for which the trace is large. This suggests that we could rely solely on postprocessing instead of using microsets, but this would be undesirable because larger microset sizes make tracing faster, whereas postprocessing does not. At very high microset sizes, the tape size decreases. One explanation for this is that, at these very high microset sizes, the tracing process filters out information that the postprocessing would have preserved. Indeed, we can see that this “cliff” in the tape size often corresponds to an increase in runtime in Figure 14. This may be because the information lost by using these very large microset sizes resulted in lower prefetching quality.

Our goal with microsets in §3.1.2 was to make it practical to trace programs. Even using a microset size of 2 is borderline impractical for some workloads; for example, for sparse_mul, the trace is > 40 GiB and takes over 40 minutes to collect. Using DBI would be much slower than even this.

3PO postprocesses the collected trace by simulating an LRU, but the actual eviction policy used by Linux at runtime may differ significantly from this (§3.2). To evaluate the impact of using this approximation, we vary the amount of memory used when simulating LRU for postprocessing, while keeping the available memory at runtime fixed. The results are shown in Figure 15. For some workloads, like np_fft and sparse_mul, prefetching accuracy increases when postprocessing is done assuming a smaller amount of memory than is actually available at runtime. This indicates that these workloads are affected by inaccuracies of assuming LRU, which can be somewhat mitigated by assuming less memory when postprocessing to be more conservative.

6 Related Work

The prior work most similar to 3PO is MAGE [25]. MAGE computes the memory access pattern of an oblivious program in advance and both prefetches and evicts according to it at runtime. However, MAGE’s techniques for collecting the access pattern and managing memory at runtime are tailored to Secure Computation, a type of cryptographic computation. For example, MAGE assumes that the program is written in a specific DSL. In contrast, 3PO develops techniques that apply to Linux processes that are oblivious and deterministic, but are otherwise generic.

Other prior works use a variety of heuristics for prefetching. Some perform prefetching by predicting a program’s future accesses based on earlier memory accesses, often from within the same execution [4, 17, 22, 42]. Others perform targeted prefetching based on measurements of a program’s working sets from prior executions [47, 52]. Some prior works have even used machine learning to predict future memory accesses based on prior ones [21, 26, 41]. Unlike these lines of research, 3PO prefetches data using the access pattern directly instead of heuristics.

Another line of work aims to allow application developers to include prefetch hints in their program [36, 45, 48], or otherwise gain increased control of paging from userspace [20, 39]. For example, the recent AIFM system [39] allows applications to use far memory via “remoteable” data structures with custom prefetching policies designed using special AIFM APIs. In contrast, 3PO does not require the application developer to extensively modify her code or provide hints.

Another approach to memory management is for the compiler, rather than the application developer, to insert prefetch directives into the program [33]. With this approach, the compiler analyzes the source code to prefetch data for future iterations of a loop, without requiring hints from the application.

Figure 15: Major page faults (30% memory ratio) vs. memory ratio used for postprocessing.
3PO: Programmed Far-Memory Prefetching for Oblivious Applications

developer. In contrast, 3PO operates on Linux processes as a black box. It is agnostic to the language the program is written in, and can prefetch for the entire application, not just loops.

7 Conclusion

In this paper we describe 3PO, a system that enables perfect heuristic-free prefetching from far memory for general oblivious applications. With 3PO, applications can run at low local memory ratios with significantly less performance degradation than with existing prefetchers such as Linux’s prefetcher and state-of-the-art Leap [4]. 3PO also allows us to study the fundamental overheads of paging-based prefetching.

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