Phase locked loop-based clock synthesizer for reconfigurable analog-to-digital converters

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Received: 16 March 2021 / Revised: 30 July 2021 / Accepted: 2 August 2021 / Published online: 25 August 2021 © The Author(s) 2021

Abstract
This paper presents the complete design of a phase locked loop-based clock synthesizer for reconfigurable analog-to-digital converters. The synthesizer was implemented in TSMC 65 nm CMOS process technology and the presented results were obtained from extracted layout view with parasitics. The synthesizer generates clock frequencies ranging from 40 to 230 MHz considering a reference frequency of 10 MHz and a supply voltage of 1.2 V. Worst case current consumption is 634 μW, settling time is 6 μs, maximum jitter is 1.3 ns in a 0.037 mm² area. Performance was validated in a test ΣΔ Modulator with bandwidths of 200 kHz, 500 kHz and 2 MHz, and oversampling frequencies of 40, 60 and 80 MHz respectively, with negligible signal-to-noise ratio degradation compared to an ideal clock.

Keywords PLL · Clock · ADC · Wireless

1 Introduction
With the rising number of wireless standards in the past decades either with the evolution and wide adoption of Bluetooth and Global Positioning System (GPS) in mobile devices, the continuous use of 3G technology, popularization of 4G technologies and the recent introduction of 5G in commercial products, receiver reconfigurability becomes an interesting and beneficial feature in System-on-Chip (SoC) embedded devices that require a large variety of Radio Frequency (RF) standards for signal processing.

One possible way of reconfiguration in wireless receivers (depicted in Fig. 1) is in the Analog-to-Digital Converter (ADC). By varying its clock sampling frequency, the output data rate can be reduced for a particular standard and thus allowing for lower power consumption when fast conversion is not necessary.

In this paper, an integer-N Phase Locked Loop-based (PLL) clock synthesizer is designed to provide the necessary frequencies for two different ADC architectures. The first ADC architecture is based on a Sigma-Delta structure for GSM, Bluetooth and UMTS standards, and the second architecture is based on Pipelined structure, employed for DVB-S2 standard.

Signal-to-Noise ratio (SNR) degradation due to clock jitter is a major problem and becomes more significant in higher frequencies regardless of ADC topology [1]. Another point of concern in large SoCs is the area availability for each sub-circuit. This was a major constraint during the design phase of this project, limiting the possible topologies of voltage controlled oscillators (VCOs).

This paper is organized as follows: Sect. 2 presents a general overview of the proposed PLL, followed by the circuit design of the main sub-blocks of the system in Sect.
In Sect. 4 the results are presented followed by the conclusion in Sect. 5.

2 PLL based clock synthesizer overview

The complete diagram of the proposed PLL is shown in Fig. 2 and its operation is as follows: first $F_{REF}$ of 10 MHz is compared with the feedback $F_{DIV}$ frequency, which is the voltage-controlled oscillator (VCO) output frequency $F_{VCO}$ divided by the pulse-swallow frequency divider (PSFD). The comparison result is fed to the charge pump (CP) circuit, which injects a current in the loop filter (LF), altering the control voltage $V_{CONT}$. This feedback scheme controls the VCO output frequency, until the system reaches locked condition in the steady-state operation.

The output VCO frequency can also be divided by two, three or four, resulting in $F_{OUT}$.

The clock frequency requirements obtained from the ADCs specifications are presented in Table 1 and the frequency planning is shown in Table 2. Jitter requirements of Table 1 are taken from [2], based on (1)

$$SNR = -20\log(2\pi f_{in}\sigma)$$  \hspace{1cm} (1)

where SNR is the ADCs Signal-to-Noise Ratio, $f_{in}$ is the maximum input frequency and $\sigma$ is the rms value of jitter.

3 Circuit design

3.1 PFD, CP, LPF and VCO

The designs of the phase and frequency detector (PFD), CP, LF and VCO are shown in Fig. 3.

The first sub-circuit of the PLL system is the PFD. As the name implies, it detects the phase an frequency from two waveforms A and B shown in Fig. 3. It is a simple and robust design consisting of two resettable D flip-flops controlled by an AND gate [3].

After the phase and frequency detection performed by the PFD, the signals $Q_A$ and $Q_B$ control if the CP sinks our sources charge in the LF. An always-on transmission gate was used at the input $Q_B$ to avoid skewing due to the delay introduced by the inverter at the $Q_A$ input and therefore...
equalizing the delays in both control switches. To avoid the imbalance of the up and down currents wider transistors were chosen for the current sources. The increased capacitance from larger transistor did not impact the PLL operation as the synthesized frequencies are not very high.

The basic idea of the capacitor $C_1$ is to store or release the charge coming from the CP, and control the voltage $V_{\text{CONT}}$. The VCO adds another pole at the origin, thus, through the addition of resistor $R_1$ in series with $C_1$, the loop is stabilized with the addition of a zero at $-1/R_1 C_1$. The addition of $R_1$ introduces a ripple in the $V_{\text{CONT}}$ waveform, and hence spurs in the spectrum. The magnitude of the ripple is proportional to the resistor size and the current coming from the CP. To reduce the ripple, the capacitor $C_2$ is introduced. Choosing $C_2 \leq 0.2 C_1$, the closed loop transfer function settling behavior is negligibly affected [3]. Based on the linear model of Fig. 4, its transfer function can be written as (2) [4]

$$H(s) = \frac{K'}{s^3 + \frac{1}{R_1 C_1} s^2 + K' s + \frac{1}{R_1 C_1}},$$

(2)

where $K_{\text{VCO}}$ is the VCO gain, $I_p$ is the CP current, $M$ is the division ratio of the PLL and $K'$ is

$$K' = \frac{K_{\text{VCO}} I_p}{2 \pi MC_2}.$$

(3)

One of the requirements during development of the DVB-S2 SoC project was a small area availability for the PLL clock synthesizer. Thus an optimum choice of VCO topology is the inverter-based voltage-controlled ring oscillator (VCRO) as it will combine small area and low power consumption. Three inverters are connected in series, with the output of the third inverter connected to the input of the first. The oscillation frequency control is made by the source-gate-bulk voltage in the n-type MOSFET varactors connected to each inverter output. The varactors

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Analog Integrated Circuits and Signal Processing (2021) 109:647–656 649

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**Fig. 4** PLL linear model: frequency domain representation

**Fig. 5** Pulse swallow frequency divider (PSFD) architecture

**Fig. 6** Complete design of the pulse swallow divider

**Fig. 7** Non-overlapping clock generation
decrease in capacitance as $V_{\text{CONT}}$ (Fig. 3) increases, hence the oscillation frequency increases.

### 3.2 Programmable loop frequency divider

From the specifications defined by Table 1, an integer-N second order PLL-based frequency synthesizer is a proper structure to obtain all desired frequencies. Therefore, the Pulse-Swallow Frequency Divider (PSFD) was chosen. The overall divide ratio ($M = F_{\text{VCO}}/F_{\text{REF}}$ in Fig. 2) can be adjusted only by a programmable counter named Swallow Counter (SC) in Fig. 5.
From Fig. 2, the operation of the PSFD can be described as follows: initially P and S are reset and the frequency at A is equal to \( F_{VCO} = (N + 1) \). After \((N + 1)S\) pulses, the SC changes B to HIGH. Now the frequency at A is equal to \( F_{VCO} = N \). After \((P - S)\) pulses, P goes HIGH and resets the SC, restarting the process. The resulting output frequency is \( F_{DIV} = F_{VCO} / (NP + S) \) as long as \( P > S \).

In this design the values N, P and S are 2, 8 and 7 respectively, allocating three bits for the SC control and allowing the reference frequency to be multiplied by 16 up to 23.

The Dual Modulus Prescaler (DMP) is shown in Fig. 6 and consists of a divide by 3 with a modified logic to accommodate an external selection bit. When Modulus Control (MC) is HIGH, \( FF_1 \) has no effect and the circuit divides by 2. If MC is LOW, the circuit divides by 3. Fig. 6 also presents the SC design, it is a slight variation from the design present in [3]. The input frequency is counted from 000 up to the word defined by D<0>, D<1> and D<2>. Then, it changes the output to HIGH, altering the DMP division, disabling all dividers while it retains the output on HIGH until the Program Counter (PC) resets all dividers. Now the output returns to LOW and the process is repeated. The PC is a simple divide by 8 circuit with an end of count reset, also shown in Fig. 6.

### Table 3 PLL performance summary

| Parameter                     | Min. | Typ. | Max. |
|-------------------------------|------|------|------|
| Supply voltage (V)            | 1.1  | 1.2  | 1.3  |
| Power (\(\mu\)W)              | 299  | 385  | 634  |
| Freq. Range (MHz)             | 40   | –    | 260  |
| \(K_{VCO}\) (MHz/V)           | 156.8| 198.4| 198.5|
| Settling time\(^a\) (\(\mu\)s) | 3.7  | 4    | 6    |
| Maximum overshoot (V)         | 0.96 | 1.1  | 1.15 |
| Jitter\(^a\) (ns)             | 0.3  | 0.5  | 1.3  |
| Maximum Spur\(^a\) (dB)       | – 60 | – 29 | – 18 |
| Area (\(\mu\m (mm^2)\))      | 114 × 324 (0.037) | | |

\(^a\) Measured when 200 MHz is selected
3.3 Non-overlapping clock generation and clock buffers

Generally in switched-capacitor circuits two phases of non-overlapping clocks are required to avoid unwanted charge transfer during sampling and transfer stages. A common design implementation of non-overlapping clock phases $\phi_1$ and $\phi_2$ is shown in Fig. 7. Additional phases $\phi_3$ and $\phi_4$ are delayed versions of $\phi_1$ and $\phi_2$.

To drive large capacitors in the ADCs the clock phases require proper buffering. This is achieved by the buffer tree shown in Fig. 8 for each phase [5].

| Type      | This Work | [6] | [7] | [8] | [9] |
|-----------|-----------|-----|-----|-----|-----|
| Design Phase | PLL       | PLL | PLL | DTC-DDS | PLL |
| Ref. Freq. (MHz) | 10    | 20  | 20  | 100  | 6.25 |
| Tuning Range (Hz) | 40–230 M | 200 M | 100–560 M | 4.7–5 G | 100–300 M |
| Tech. (nm) | 65       | 90  | 180 | 65   | 250 |
| Supply (V) | 1.2      | 1.2 | 3.3 | 1.2  | 3.3 |
| Area (mm$^2$) | 0.037  | 0.18 | 0.16 | n/a  | Not informed |
| Power (mW) | 0.634    | 9   | 24  | 20   | 6   |
| Jitter (ps)| 1300     | 3   | 4   | 1.1  | 12  |

Table 4 Comparison with other works
Table 5 Comparison between ideal and worst case clock results in an \(\Sigma\Delta\) Modulator

| Param./Mode       | GSM   | Bluetooth | UMTS  |
|-------------------|-------|-----------|-------|
| Samp. Freq. (MHz) | 40    | 60        | 80    |
| Bandwidth (MHz)   | 0.2   | 0.5       | 2     |
| Modulator Order   | 2nd   | 2nd 2.5 bit | 3rd 2.5 bit |

| Clock Type       | Ideal PLL | Ideal PLL | Ideal PLL |
|------------------|-----------|-----------|-----------|
| SNR (bits)       | 12.78     | 12.6      | 11.68     |
| SFDR (dB)        | 84.3      | 82        | 75.2      |

4 Results

All simulations were performed using Cadence Virtuoso environment in a extracted layout view, including parasitics and corners for process, supply variation and temperature. The PLL design was realized in TSMC 65 nm process. For the LF, Metal-Oxide-Metal (MoM) capacitors were used, while for the \(\Sigma\Delta\) Modulator circuit validation, Metal-Insulator-Metal (MiM) capacitors were used. Poly-Resistors were used in both designs. Complete layout is presented in Fig. 9. The total area is 114x324 \(\mu\)m \((0.037 \text{ mm}^2)\).

The VCO frequency characteristic varying with the control voltage is shown in Fig. 10 and the phase noise for worst case (FF, 1.3 V, 80°C) is shown in Fig. 11. The phase noise performance, of around – 90 dBc/Hz at 100 kHz frequency offset, is the expected for the ring oscillator topology. Improvements in phase noise response can be achieved at the expense of power consumption [3].

Figure 12 presents the settling behavior of the control voltage fed to the VCO when 200 MHz is selected. Worst case condition in this case is specifically for total settling time, which happens with slow-slow devices at 0°C and with supply at 1.1 V resulting in total settling time of about 6 \(\mu\)s. Although the worst case results in worst settling time, the ripple in settled condition is actually smaller than typical operation, resulting in a cleaner spectrum, and less jitter, which is desirable for the proposed application since there are no strict requirements in regards to settling time. Figure 13 presents the settling behavior for each possible frequency selection defined by the PSFD.

Figure 14(a), (b) show the obtained spectrum for a selected frequency of 200 MHz in typical conditions (TT devices, supply at 1.2 V and 27°C) and worst case condition (FF devices, supply at 1.3 V and 80°C) respectively, spanning between 100 MHz and 300 MHz. The spectrum showed severe degradation as devices tend to fall in the fast-fast process variation.

Jitter response was obtained by eye diagram plot performed in Cadence Virtuoso environment shown in Fig. 15. As expected from spectrum curves, jitter showed to be worst in-fast-fast, 1.3 V supply voltage and 80°C condition, resulting in 1.3 ns, while in typical conditions the resulting jitter is 500 ps. Of course this simulations will only capture the deterministic portion of the total jitter, however this verification is a sufficient preliminary result to give an idea of the PLL behavior in worst case conditions.

Performance summary of the PLL is presented in Table 3 and comparison with other works is shown in Table 4. It is clear that compared with other works, this design trades power dissipation for jitter degradation.

Validation of the generated clock was performed in the reconfigurable \(\Sigma\Delta\) Modulator shown in Fig. 16. The non-overlapping clocks are generated by the circuit of Fig. 7 and are inserted in the switches of modulator highlighted by the symbols \(\phi_1\), \(\phi_2\), \(\phi_{1d}\) and \(\phi_{2d}\) of Fig. 16. Clock frequencies for each case and results compared with an ideal clock are summarized in Table 5. The tests were performed with clocks at 40, 60 and 80 MHz, in a second order modulator for 40 and 60 MHz tests and third order for the 80 MHz test.

GSM, Bluetooth and UMTS bandwidths, obtained values of Signal-to-Noise Ratio (SNR) and Spurious Free Dynamic Range (SFDR) are in accordance with several reported reconfigurable \(\Sigma\Delta\) modulators such as [10] and [11]. Modulator spectra are presented in Fig. 17 comparing ideal clock and worst case PLL generated clock for each case. Overall the results showed negligible degradation in SNR and no noticeable additional spurs are present in the spectra, confirmed by the obtained values of SFDR. Although the SNR degradation proved more severe in the 60 MHz case, the results are still satisfactory and validate the clock synthesizer design for the \(\Sigma\Delta\) type ADC.

From Table 1, jitter performance requirements for the Pipeline topology were not met. Several jitter and duty cycle correction circuits have been reported [12, 13] and will be necessary alongside calibration techniques to improve SNR degradation.

5 Conclusions

A PLL-based clock generator to be used in reconfigurable ADCs was designed to generate clocks in the span between 40 and 230 MHz. Results were validated in extracted layout simulations including parasitics and PVT corners. Additional validation was performed in a prototype reconfigurable \(\Sigma\Delta\) Modulator for oversampling frequencies of 40, 60 and 80 MHz, with no significant degradation in performance compared with the results of an ideal clock.
Fig. 17 Power Spectrum Density comparison between ideal clock and PLL-based clock for different oversampling frequencies. Hanning Window with 8192 FFT points. 53 kHz input frequency for (a) and (b), 124 kHz for (c) and (d) and 166 kHz for (e) and (f).
Acknowledgements The authors would like to thank Eldorado Research Institute for supporting this work.

Data Availability Statement Data sharing not applicable to this article as no datasets were generated or analysed during the current study.

Declaration

Conflict of interest Partial financial support was received from Eldorado Research Institute.

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