S$^3$NAS: Fast NPU-aware Neural Architecture Search Methodology

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ABSTRACT

As the application area of convolutional neural networks (CNN) is growing in embedded devices, it becomes popular to use a hardware CNN accelerator, called neural processing unit (NPU), to achieve higher performance per watt than CPUs or GPUs. Recently, automated neural architecture search (NAS) emerges as the default technique to find a state-of-the-art CNN architecture with higher accuracy than manually-designed architectures for image classification. In this paper, we present a fast NPU-aware NAS methodology, called S$^3$NAS, to find a CNN architecture with higher accuracy than the existing ones under a given latency constraint. It consists of three steps: supernet design, Single-Path NAS for fast architecture exploration, and scaling. To widen the search space of the supernet structure that consists of stages, we allow stages to have a different number of blocks and blocks to have parallel layers of different kernel sizes. For a fast neural architecture search, we apply a modified Single-Path NAS technique to the proposed supernet structure. In this step, we assume a shorter latency constraint than the required to reduce the search space and the search time. The last step is to scale up the network maximally within the latency constraint. For accurate latency estimation, an analytical latency estimator is devised, based on a cycle-level NPU simulator that runs an entire CNN considering the memory access overhead accurately. With the proposed methodology, we are able to find a network in 3 hours using TPUv3, which shows 82.72% top-1 accuracy on ImageNet with 11.66 ms latency. Code are released at https://github.com/cap-lab/S3NAS

1 INTRODUCTION

As there are growing needs of deep learning applications based on convolutional neural network (CNN) in embedded systems, improving the accuracy of CNNs under a given set of constraints on latency and energy consumption has brought keen interest to researchers as a challenging problem in various areas. A popular hardware solution is to develop a hardware accelerator, called neural processing unit (NPU), that achieves higher performance per watt than CPUs or GPUs.

For a given hardware platform, several software techniques have been proposed to accelerate CNNs by approximate computing since deep learning applications can tolerate a certain range of computation inaccuracy. Some examples in this software approach are filter pruning [17], quantization [22], low-rank approximation [16]. Accelerating CNNs is helpful to improve the accuracy by running a more compute-intensive CNN with higher accuracy within a given time budget.

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space grows exponentially as the allowed computation complexity grows. Hence, reducing the search space, as well as the search time, is very challenging for NPU-aware NAS techniques. While the aforementioned work for Google’s Edge TPU trains each architecture candidate from scratch to estimate the performance, it is not computationally efficient. In contrast, we adopt a fast differentiable hardware-aware One-Shot NAS, called Single-Path NAS [28], in order to reduce the search time.

Figure 2 shows an overview of the proposed NAS methodology that consists of three steps. In the first step, we change the supernet structure of the Single-Path NAS, which has a hierarchical structure based on MobileNetV2 [27]: A supernet structure consists of a series of stages that contain a series of blocks containing an MBConv micro-architecture inside. Since the network accuracy depends on the supernet structure, we make two extensions on the supernet structure to widen the search space. First, we allow stages to have a different number of blocks, called depth of the stage, considering the effect of stage depth on the accuracy and the latency. Second, we add parallel layers with different kernel sizes in each block, adopting the idea of mixed depthwise convolution [33] (MixConv).

With the extended supernet structure, we apply the Single-Path NAS, which is also extended to support the extended supernet structure. In this step, we assume a shorter latency constraint than the required to reduce the search space and the search time. The last step is to scale up the baseline CNN adopting the compound scaling technique proposed in [32] until the latency constraint is met. The proposed NAS methodology is named as $S^3$NAS since it consists of 3 steps: Supernet design, SinglePath NAS, and Scaling and post-processing.

For accurate latency estimation, an analytical latency estimator is devised, based on a cycle-level NPU simulator that runs an entire CNN considering the memory access overhead accurately. Since the NPU assumed in this paper can execute depth-wise separable convolution (DWConv), squeeze-and-excitation (SE), and h-swish activation function efficiently, the proposed supernet prefers DWConv to regular convolution. Observing that the accuracy is improved by around 1% if SE and h-swish activation function are used, we add a post-processing phase after a CNN network is found by NAS to add SE layers and to replace ReLU to h-swish activation function.

Experiments show that the proposed NAS technique could improve the accuracy-latency tradeoff over existing SoTA CNN models. Our best model achieves 82.72% top-1 accuracy on ImageNet with 11.66ms latency without any special data augmentation. Note that the latency is estimated by cycle-accurate simulation. For a fair comparison with the related work, the latency of each compared network is also estimated with the same simulator.

2 RELATED WORK
2.1 Neural Architecture Search (NAS)

After an automated NAS technique based on reinforcement learning successfully found a better CNN architecture than manually-designed architectures [36], extensive research has been conducted to develop various NAS techniques based on reinforcement learning [31, 37]. However, these NAS techniques are computationally intensive because they train each candidate architecture from scratch to estimate the goodness of it. Thus, one-shot neural architecture search approach [24] was introduced to reduce the search cost. In this approach, an over-parameterized super-model network is defined, and architecture search is performed by parameter optimization to reduce the complexity of the network. Gradient-based differentiable search has gained increasing popularity, and various NAS techniques have been proposed with different super-models and hyper-parameters [2, 5, 8, 19, 24].

Among diverse techniques to decrease the search cost, Single-Path NAS [28] was recently proposed to find a good architecture faster than the existing differentiable NAS techniques. This technique is extended to broaden the search space by including the squeeze-and-excitation (SE) block in the search space [29]. Our work is grounded on the original Single-Path NAS technique.

2.2 Hardware-friendly Neural Architecture Design

Finding a hardware-friendly neural architecture has been facilitated as NAS algorithm improved. MNASNet [31] added a latency term in the objective function to discover better architectures with a given latency constraint on their target hardware platform. EfficientNet [32], whose search method is similar to MNASNet, introduced a novel scaling method, called compound scaling, to find more accurate networks as the latency constraint or FLOPS increases. Instead of finding a network directly for a given long latency constraint, they scale up the depth and the width of a small network with shorter latency and the input image size in a balanced way. They could achieve a set of networks with state-of-the-art performance over a range of latency constraints. They removed SE blocks and h-swish activation function from their search space for hardware platforms that do not support them efficiently to name the resultant network as EfficientNet-lite.

While EfficientNet searches a set of networks over a range of latency constraints by scaling up, Once-For-All [1] network takes an opposite approach, scaling down. They first train a super-graph architecture by a novel method called progressive shrinking and search a sub-graph network that achieves good accuracy for a given latency constraint without re-training but cheap fine-tuning. They claim that a scaled-down network from the super-graph gives better accuracy than a network that is trained from scratch. They could
find more accurate networks than EfficientNet for small latency constraints.

To explore more efficient neural architectures on specific hardware, some NAS methods have proposed to define the design space of architecture exploration, tailored for the hardware platform. Gupta et al. [9] devised a building block named fused inverted bottleneck convolution block and showed that this block is often more efficient than MBConv on their target NPU, Edge-TPU. They adopted compound scaling method to find high-performing architectures on Edge-TPU. Our work is closely related to this method. We devise a building block that consists of parallel DWConv layers with different kernel sizes, based on a preliminary experiment to find that it is better than the other alternative building blocks in terms of performance per latency [33]. And we increase the search space by allowing stages to have a different number of blocks in the baseline supernet.

2.3 Deciding the Depth of Stages

A neural network typically consists of multiple stages, a sequence of blocks with the same number of output channels (width). There are studies on how to assign the number of blocks (depth) to each stage. Meng et al. [21] observed that the way of assigning depth to each stage affects the accuracy. Moreover, they argued that the good depth assignment of each stage could be inherited from the shallow ones as the total depth is increased, and proposed a layer-growing NAS method that could significantly reduce the search space. Furthermore, Radosavovic et al. [25] discovered that among neural architectures with similar computational complexity, the ones whose stage width and depth have a quantized linear relationship tend to have higher accuracy. Based on similar observations, we apply this design principle to change the structure of the conventional One-Shot NAS supernet. In addition, we argue that placing more blocks in a stage with a larger width is beneficial.

2.4 Depthwise Convolution with Multiple Kernel Sizes

While the original DWConv block uses a single kernel size for depthwise convolution, mixing multiple kernel sizes for depthwise convolution was recently proposed, named as MixConv [33]. Mixing multiple kernel sizes can be understood as having parallel branches inside a block. It is shown that MixConv is more efficient than ordinary DWConv [33]. There exist some recent NAS methods [4, 20] that also broaden their search space using DWConv with multiple kernel sizes to find better neural architectures. We adopt this approach in the supernet and formulate a differentiable latency model of this operation, enabling a latency-aware differentiable One-Shot NAS with MixConv.

3 BACKGROUND

In this section, we will briefly review the Single-Path NAS technique and our target NPU. Before going further, we define some terminologies used in this paper, as shown in Figure 3. A neural architecture consists of stages at the top level. A stage consists of a sequence of blocks whose output feature maps have the same dimension. In the proposed supernet, a block is defined as MBConv that typically starts with 1x1 conv (expansion layer) and ends with 1x1 conv. Adopting the MixConv approach, the depthwise convolution layer consists of parallel superkernels whose kernel size will be determined during the NAS process. The width of block denotes the number of channels in the final output feature map of the block, and the width of stage is the width of the final block in the stage. We will call the total number of blocks starting from the very first block in the network up to the last block in a specific stage S, as the cumulative depth up to stage S.

3.1 Single-Path NAS

Differentiable NAS methods usually define architecture parameters to choose which convolution layer to use in the block, training each convolution layer independently. Single-Path NAS [28] reduce the search cost by decreasing the number of trainable parameters by sharing the kernel weights between convolution layers. The key idea is designing an over-parameterized depthwise convolution kernel named superkernel, and letting each depthwise convolution kernel of candidate MBConvs directly inherit the weights of this superkernel.

Let $w_{k,e}$ denote the depthwise convolution kernel of candidate MBConv with kernel size $k$ and expansion ratio $e$ (MBConv$_{k,e}$).
First, they introduce a large \( w_{5,6} \), which is the DWConv kernel of MBConv\(_{3,6} \). Then, the inner core of \( w_{5,6} \) can be considered as \( w_{3,6} \), a DWConv kernel of MBConv\(_{3,6} \). A superkernel containing these two kernel size options can be expressed as Figure 4:

\[
\mathbf{w}_{*6} = \mathbf{w}_{3,6} + \mathbb{1}(\text{use kernel size 5}) \cdot \mathbf{w}_{5,3,6}
\]

(1)

where \( \mathbf{w}_{5,3,6} \) means the outer part, \( \mathbf{w}_{5,6} - \mathbf{w}_{3,6} \). Next, they formulate conditions to determine the kernel size. They define a certain threshold value \( t \) and compare the norm of the kernel weights with the threshold. If the norm of a subset weight is larger than the threshold, it remains in the supernet. To this end, Eq. (1) is changed as follows:

\[
\mathbf{w}_{*6}(t_k = 5) = \mathbf{w}_{3,6} + \mathbb{1}(\|\mathbf{w}_{5,3,6}\|^2 > t_k = 5) \cdot \mathbf{w}_{5,3,6}
\]

(2)

The threshold value is also trainable to be automatically chosen during training. To enable back-propagation, they relax \( 1(x > t) \) to \( \sigma(x - t) \) when computing gradients. In addition, they optimize kernel weights and threshold values simultaneously. For a given tight search time, this method is shown to be more effective than the other methods [29].

Moreover, we can vary the number of channels by varying the expansion ratio of each block: we can use only the first half channels of \( w_{5,6} \) and \( w_{3,6} \) as \( w_{3,3} \) and \( w_{3,3} \), respectively. By defining another set of trainable thresholds, the following formula is defined to determine the expansion ratio:

\[
\mathbf{w}_{*6}(t_e = 3, t_e = 6, t_k = 5) = \mathbb{1}(\|\mathbf{w}_{3,3}\|^2 > t_e = 3) \cdot \mathbf{w}_{3,3}(t_k = 5) + \mathbb{1}(\|\mathbf{w}_{3,3}\|^2 > t_e = 3) \cdot \mathbb{1}(\|\mathbf{w}_{5,3,6}\|^2 > t_e = 6) \cdot \mathbf{w}_{5,3,6}(t_k = 5)
\]

(3)

where \( \mathbf{w}_{k,6} \) means the remaining half of channels, \( \mathbf{w}_{k,6} - \mathbf{w}_{k,3} \). Note that if \( t_e = 3 \) is sufficiently large, all channels can be removed to make the block a plain skip connection. Thus, they replace the original depthwise convolution kernel of MBConv\(_{5,6} \) with \( \mathbf{w}_{*6} \), yielding a differentiable and searchable MBConv with respect to the kernel size and expansion ratio.

They also design a differentiable latency-aware loss function to consider hardware latency in the search algorithm. To this end, they define a function to estimate latency as follows:

\[
L_e^k = \mathbb{1}(\|\mathbf{w}_{k,3}\|^2 > t_e = 3) \cdot (P_{k,5}^l + \mathbb{1}(\|\mathbf{w}_{k,6}\|^2 > t_e = 6) \cdot (P_{k,6}^l - P_{k,3}^l)) \tag{4}
\]

\[
L_i^k = P_{k,5}^l / P_{k,5}^l + L_e^k + \mathbb{1}(\|\mathbf{w}_{k,3,6}\|^2 > t_k = 5) \cdot L_e^k \cdot (1 - P_{k,6}^l / P_{k,5}^l) \tag{5}
\]

where \( P_{k,e}^l \) is a profited latency value for MBConv\(_{k,e} \) for the \( k \)th block in the supernet. Note that they used \( P_{k,6}^l, P_{k,5}^l, \) and \( P_{k,6}^l, P_{k,5}^l, P_{k,6}^l \) only to formulate \( L_e^k \), and the latency for MBConv\(_{3,3} \) is approximated using these values. Here is the latency-aware loss function designed:

\[
CE + \lambda \cdot \log(\sum_t L_t^1) \tag{6}
\]

Finally, they search for a neural architecture in two phases. First, they train the supernet by randomly choosing one of the candidate subgraphs in each training step. In this phase, they use CrossEntropy loss only. Next, they enable latency-aware loss function and train the supernet with the loss function, to decide the threshold values. By doing this, they could get a high-quality neural architecture with only eight epochs of ImageNet training set.\(^1\)

### 3.2 Target NPU

Even though the proposed methodology can be applied to any type of NPU, the current implementation is made for an adder-tree type NPU, called MIDAP [15]. It has a fully-pipelined micro-architecture that consists of separate hardware modules and memory modules for convolution, activation function, and various reduction operations. Since it enables us to make a fully static schedule of operations without resource contention in the data path, we can estimate the end-to-end latency of a CNN quite accurately analytically. Unexpected delay may incur from off-chip DRAM delay that is not fully hidden by double buffering.

Another good feature of MIDAP is that it efficiently supports the following operations that would lower the MAC (multiply-accumulate) utilization in other NPUs that have many MAC units: pooling, DWConv, and squeeze-and-excitation (SE). For DWConv operation, it does not use an adder tree but an alternative hardware logic that consists of a set of individual accumulators connected to the multiply units. For pooling and SE operations, reduction logic is included in the pipeline. Note that MIDAP has not been implemented as a real hardware chip yet but as a virtual prototype with a cycle-accurate simulator. Thanks to the cycle-accurate simulator that considers the DRAM access contention and parametrized DRAM access delay, we could build an accurate analytical model for end-to-end latency estimation, based on the profiling result with the simulator.

Inverted bottleneck with depth-wise convolution (MBCnv) [27] is a popular building block in recent mobile-friendly networks. However, it is not efficiently supported in existing NPUs that do not have specialized hardware units for DWConv [7, 9]. Thus Gupta et al. [9] replaced an MBCnv block with a fused building block that fuses an expansion layer and DWConv in MBCnv into a single full convolution. Even though the fused block increases the number of multiplications significantly, it improves the MAC utilization larger so that the fused block is observed faster than MBCnv on their target NPU, EdgeTPU. By adding this building block to their search space, they could successfully obtain different neural architectures for EdgeTPU from those for GPUs.

\(^{1}\)In our implementation, we changed the probability of selecting each candidate MBConvs to be equal.
Since DWConv is efficiently supported in MIDAP, however, the improvement of MAC utilization by fusing does not outweigh the increased computation complexity, which is observed in preliminary experiments. The experiment setup is similar to main experiment setup that will be explained in section 5.2. The experimental result is shown in Table 1. The latency constraint for fused block experiment is set to 7.0ms, while others are set to 2.15ms. In the combined experiment, we use the fused block in the 1st and the 2nd stages, and MBConv for the remaining stages since the latency gap between two building blocks is too high. As shown in the table, MBConv block shows the best tradeoff between accuracy and latency. Hence we prefer MBConv to the fused building block as the basic building block in the supernet for MIDAP.

Table 1: NAS comparison with different building blocks

| building block     | accuracy (%) | latency (ms) |
|--------------------|--------------|--------------|
| Fused inverted bottleneck conv | 77.34        | 6.90         |
| MBConv             | 77.75        | 2.05         |
| Combined           | 76.55        | 2.20         |

4 PROPOSED S3NAS METHODOLOGY

In this section, we explain the proposed S3NAS methodology that consists of three steps as displayed in Figure 2.

4.1 Supernet Design

The number of blocks is one of the key parameters in neural networks. It is observed that the total number of blocks affects the accuracy of neural architecture [11, 32]. In conventional One-Shot NAS methods, each stage in the supernet has the same number of blocks [2, 28, 34]. On the other hand, some recent studies [21, 25] report that the way of assigning the number of blocks in each stage has a noticeable impact on the accuracy, even with the same number of blocks in total. Hence we allow stages in the supernet to have a different number of blocks.

We investigate the impact of assigning the number of blocks in the supernet with another preliminary experiment. We construct a network based on MobileNetV2, which has four blocks in every stage, and observe the change of accuracy as we reduce two blocks in a different stage in each experiment. Figure 5 shows that MBConvs with larger width has more impact on accuracy.

As the number of multiplications in a DWConv is $W \times H \times C \times K^2$, the later stage of DWConv tends to have shorter latency since the reduction of $H \times W$ is larger than the increase of $C$. Thus the impact on the latency by increasing the number of blocks in a later stage is not significant as displayed in Figure 5.

Thus, we place more blocks to stages with larger width in the supernet, making the cumulative depth up to a specific stage is proportional to the width of the stage, which is similar to PyramidNet [10]. A recent study [25] also claims that neural architectures with a linear relationship between the cumulative depth and the width tend to have higher accuracy with a similar amount of computation complexity. Our experiment shows that our modification to supernet enhances the efficiency of the search result in terms of accuracy as well as latency (Table 4).

Figure 5: Impact of reducing the number of blocks in different stages in a MobileNetV2-based model

Another feature of the proposed supernet is to use mixed convolution (MixConv) that mixes different kernel sizes in the depthwise convolution layer [33]. Some recent NAS methods [4, 20] also broaden their search space using DWConv with various kernel sizes and could find better neural architectures.

Figure 6 depicts our building block structure. This block starts and ends with $1 \times 1$ convolution, with $N$ searchable superkernels in the middle. Each searchable superkernel is designed similarly to Eq. (3), while we may use different threshold values in each superkernel. The kernel sizes and expansion ratios are selected among predetermined values. If the $j$-th searchable superkernel chooses an expansion ratio $e_j$, the $j$-th kernel has $e_j$ times more channels than the first $1 \times 1$ convolution. Compared with the original MixConv suggested in [33], the proposed building block supports more diverse combinations of kernel sizes and expansion ratios. It enhances the efficiency of search results on our target NPU (Table 5).

Figure 6: Our MixConv-based building block for supernet

We finish this subsection by highlighting the merit of Single-Path NAS on building a MixConv-based differentiable NAS. Conventional multi-path NAS methods would have difficulties when adding inverted bottleneck convolution with MixConv to their search space. Since the number of possible choices of such blocks grows proportionally to the partition number, multi-path NAS methods would introduce a significant increase in memory requirements and the search time. On the contrary, MixConv can be efficiently supported in Single-Path NAS, as explained below.
4.2 Modified SinglePath NAS

We use a different latency estimation model, and a loss formula from the original SinglePath NAS technique explained in section 3.1.

4.2.1 Differentiable Latency Model. Suppose we concatenate $N$ searchable superkernels to build a MixConv-based building block, and let $\tilde{k} = (k_1, \ldots, k_N), \tilde{e} = (e_1, \ldots, e_N)$ where $k_j, e_j$ denote the kernel size and the expansion ratio of the $j$th searchable superkernel. The estimated latency of a DConv operation depends on the kernel size and the expansion ratio.

For latency formulation, we first define two condition variables, $F_{j,k}, G_{j,e}$, that denote whether the $j$th searchable superkernel chooses the kernel size $k_j$ and the expansion ratio $e_j$, respectively; For example, $F_{j,k_j}$ is 1 if and only if the $j$th searchable superkernel chooses $k_j$ and 0 otherwise.

Let $k_1 < \cdots < k_N$ be the candidate kernel sizes, and $0 = e_1 < \cdots < e_F$ denote the candidate expansion ratios of the $j$th searchable superkernel, respectively. Suppose $k_j = k_c$, then $F_{j,k_c}$ can be formulated as follows:

$$F_{j,k} = \prod_{2 \leq i \leq e} \{ \mathbb{I}(\|w_j, k_i, k_{i-1}, e_i\|^2 > t_j, k_i) \} \cdot F_{j,k_c} \cdot g_{j,e},$$

where

$$g_{j,e} = \begin{cases} \mathbb{I}(\|w_j, k_j, e_j\|^2 > t_j, k_j), & \text{if } c < K_j \\ 1, & \text{if } c = K_j \end{cases}$$

Figure 7: An example of Eq. (7) when a searchable superkernel chose kernel size $k_2$.

Figure 7 depicts an example of this formula when the $j$th searchable superkernel that has four candidate kernel sizes $k_1 < \cdots < k_4$ chooses $k_2$ as the kernel size: $k_j = k_2$. It means that weight $w_j, k_i, e_i$ and $w_j, k_j, e_j$ are used, but the remaining weights starting from $w_j, k_i, e_i$ are not used. Since $w_j, k_i, e_i$ is always used, it is not included in the formula. To use $w_j, k_j, e_j$, the norm of it has to be larger than $t_j, k_j$ while the norm of $w_j, k_i, e_i$ should not be larger than $t_j, k_i$ to avoid the use of larger kernel sizes.

We can formulate $G_{j,e}$ similarly:

$$G_{j,e} = \prod_{2 \leq i \leq d} \{ \mathbb{I}(\|w_j, s, e_i, e_{i-1}\|^2 > t_j, e_i) \} \cdot g_{j,e},$$

where

$$g_{j,e} = \begin{cases} \mathbb{I}(\|w_j, s, e_d, e_{d-1}\|^2 < t_j, e_d), & \text{if } d < E \\ 1, & \text{if } d = E \end{cases}$$

when $e_j = e_d$. Then the condition for a MixConv-based building block to choose $\tilde{k}, \tilde{e}$ can be expressed as $\prod_{j=1}^{N} F_{j,k_j} G_{j,e_j}$.

Now, the estimated latency of a single block is formulated as follows:

$$L = \sum_{k, e}^N \{ P(\tilde{k}, \tilde{e}) \} \prod_{j=1}^{N} F_{j,k_j} G_{j,e_j}$$

where $P(\tilde{k}, \tilde{e})$ denotes the profiled latency value of a MixConv-based building block corresponding to $\tilde{k}, \tilde{e}$.

Unlike the original Single-Path NAS that approximates the latency in Eq. (5) in some cases, we use the profiled latency value in all cases. Note that an expansion ratio can be zero, and if only one superkernel has a nonzero expansion ratio, the MixConv block is reduced to a plain MConv block. Finally, we can estimate the latency by summing up these estimated latencies for all superkernels in the block, $\sum L$.

Figure 8: Two implementations of a same block. While their FLOPS are identical, their estimated latencies are different.
4.3 Post-processing

In the second step, we intentionally use shorter latency to reduce the search space for the baseline network. After finding the baseline network with a shorter latency, we apply compound scaling to find an architecture with the final latency constraint. In this step, we conduct post-processing to add SE block and h-swish activation function if beneficial.

4.3.1 Compound Scaling. It is well known that increasing depth [11], width [35], or input image size improves accuracy while it increases latency. However, if only one of these three factors is increased, the accuracy improvement is quickly saturated. Observing this fact, Tan et al. [32] proposed a compound scaling method that increases all three factors together. A scaling coefficient is defined for each factor. By judiciously assigning the scaling coefficients in a balanced fashion, they could improve the accuracy much larger than scaling a single factor only. Adopting this approach, we apply the compound scaling to the baseline architecture obtained in the previous step. Based on the ratio between the true latency constraint and the assumed latency constraint in the second step, we find the scaling coefficients considering the estimated latency increment. To keep the linear relationship between the width and cumulative depth, we use the same scaling coefficient for width and depth, differently from [32]. Note that how to realize scaling depends on the baseline architecture. While the baseline architecture assumed in [32] has a series of identical blocks in each stage, a stage consists of heterogeneous blocks in our baseline architecture. Thus depth scaling is not realized by merely adding new blocks in each stage. We need to choose what types of blocks to add in each stage. We increase the number of blocks with more parameters first. To compute how many blocks to add in a stage, we multiply the depth of the stage by depth coefficient and round the multiplication result. Width scaling is applied to all blocks equally. Finally, we consider latency when we scale.

4.3.2 Add h-swish and SE. In addition to compound scaling, we add two components in the post-processing step: h-swish activation function and squeeze-and-excitation (SE) block. A recent study [23] reports that SE and the h-swish activation function are no hurdles for 8-bit quantization. They could quantize a network with SE and h-swish without noticeable accuracy loss.

Extensive studies have been conducted to find a better activation function than ReLU, and the swish activation function [26] was found. Several neural networks [20, 32, 33] use swish activation function instead of ReLU to improve accuracy. Howard et al. [12] proposed a quantization-friendly version of the swish activation function called h-swish that has a similar impact on accuracy. So, we replace ReLU with h-swish [12] activation function.

Squeeze-and-Excitation(SE) is a lightweight operation which is shown to be beneficial to accuracy [13]. Figure 10 depicts the structure of a SE block. For a given input feature map, it first computes the importance of each feature channel. Firstly, channel-wise multiplication is performed between the activation and the input feature map by global average pooling. After such squeeze operation generates channel-wise statistics, excitation operation captures channel-wise dependencies by two cascaded fully-connected layers to produce activation values, which represents the importance of each feature channel. Finally, channel-wise multiplication is performed between the activation values induced by the excitation operation and the input feature map for each channel. SE block is used in many recent architectures [12, 25, 32]. By adding SE blocks to the baseline network, we also observe the accuracy improvement.

Figure 10: Structure of SE block

4.3.3 Selective removal of SE. Figure 11 depicts an example distribution of activation values produced by two different SE blocks for three different images. The authors of the original paper [13] conjectured that if such distribution from a SE block does not differ widely between image classes, the SE block is not important. Thus, after training, they obtained averaged activation values of a SE block over multiple images in the same class. They compared the distributions of the averaged values over different image classes. They observed that removing the SE blocks that have similar distributions over different image classes incurs only a marginal loss in accuracy.
Inception preprocessing
RMSProp with decay 0.9,
0.2
channel index
activation
0.2
0.4
0.6
0.8
1
0 20 40
0
0.2
0.4
0.6
0.8
1
image 0
image 1
image 2
channel index
activation
0 20 40
0
0.2
0.4
0.6
0.8
1
image 0
image 1
image 2

Figure 11: Distribution of activation values produced by two different SE blocks for three different images

Inspired by this observation, we propose to remove SE blocks selectively to minimize the additional computation cost caused by SE blocks. We obtain activation values from a SE block for each input image and measure how the distribution of activation values varies over different input images. For each channel $c$, we calculate the standard deviation $\sigma_c$ of activation values over different images. If $\sigma_c$ is small in most channels, the activation values from the SE block do not differ much over images. Conceptually, it implies that the SE block does not help to discriminate further which channel is more influential. From the engineering perspective, it means that channel-wise multiplication of a SE block is similar to constant multiplication, which can be handled by the following convolutional layer.

We define a metric as the average of standard deviation values $\sigma_c$ over all channels that represent the diverseness of the activation distribution over different images. If the metric value is small, we remove the SE block. For example, in Figure 11, our metric of the SE block on the left side has a value of 0.021, while the right side has a value of 0.118, more than 5x larger than the left side; The left side is a better candidate for SE block removal. When we remove SE blocks according to this metric, the accuracy is found to be similar, while the latency got shorter (Table 6).

5 EXPERIMENTS

5.1 Setup

We evaluate the proposed NAS technique for image classification with the ImageNet dataset. The current implementation is made for MIDAP [15] that can perform DWConv and SE operations efficiently so that MBConv is preferred to full 3-D convolution as the basic building block, as explained above. Latencies on the target NPU are obtained with the cycle-accurate simulator$^2$.

A superkernel has two parameters to search: expansion ratio and kernel size. To limit the search space, we choose the expansion ratio among 0, 2, 4, and 6, and the kernel size between 3 and 5 when MBConv or full convolution is used as the building block. In the case of the MixConv-based building block, we use $N=3$ superkernels whose expansion ratio is 0 or 2; The sum of the expansion ratio of three superkernels has the same range as the expansion ratio of a single MBConv block. To allow three superkernels to have different kernel sizes, we let one of three superkernels be able to have 7 as the kernel size.

In the first phase of the neural architecture search, we train the supernet by randomly choosing one of the candidate subgraphs in each training step. We train the supernet for 8 epochs, with $\lambda_1 = 0$ in the loss function of Eq. 9, focusing only on the accuracy. We decrease the learning rate by 0.97 every 2.4 epochs, starting from 0.064. The other setting for network training is displayed in Table 2. Gradient clipping with a value of 10 is used in this phase. In the second phase, we set $\lambda_1 = 15, \lambda_2 = 100$ to consider latency in the loss function, and optimize the weights and threshold values of supernet for 2 epochs. After this second phase finishes, the final architecture topology is decided.

Next, we train the final architecture again to determine the filter weights for 350 epochs with the ImageNet again, using the same setting described in Table 2. Unlike the search phase, the learning rate is increased from 0 to 0.064 in the first 5 epochs, then decayed by 0.97 every 2.4 epochs. Since we observed that the batch size is critical to accuracy when using the EfficientNet training code, we use a large batch size. Both network architecture search and final training are conducted on Google Cloud TPUs.

Table 2: Settings for network training, which is similar to [32]$^3$.

| train batch size | 1024 |
|------------------|------|
| optimizer        | RMSProp with decay 0.9, momentum 0.9, epsilon 0.001 |
| image preprocessing | Inception preprocessing |
| weight decay     | 1e-5 |
| label smoothing  | 0.1 |
| stochastic depth | 0.2 |
| Exponential Moving Average | 0.9999 |

5.2 Supernet Design

Table 3: The supernet architecture of the proposed NAS technique

| input | block | width | depth | strides |
|-------|-------|-------|-------|---------|
| 224$^2 \times 3$ | 7x7 conv | 32 | 1 | 2 |
| 112$^2 \times 32$ | TBD | 32 | $d_1$ | 2 |
| 56$^2 \times 32$ | TBD | 64 | $d_2$ | 2 |
| 28$^2 \times 64$ | TBD | 128 | $d_3$ | 2 |
| 14$^2 \times 128$ | TBD | 160 | $d_4$ | 1 |
| 14$^2 \times 160$ | TBD | 256 | $d_5$ | 2 |
| 7$^2 \times 256$ | fc | 1280 | 1 | 1 |
| 7$^2 \times 1280$ | avgpool | 1280 | 1 | 1 |
| 1$^2 \times 1280$ | fc | 1000 | 1 | 1 |

In the proposed NAS technique, two major extensions are made to the supernet, compared with the original SinglePath NAS technique. Table 3 shows the proposed supernet architecture with configuration parameters, block types and depths. It starts with a 7x7

$^2$https://github.com/cap-lab/MidapSim

$^3$The setting is similar to EfficientNet training code: https://github.com/tensorflow/tpu/tree/master/models/official/efficientnet
We apply the proposed NAS method with the supernet architecture for feature extraction and 2 fully-connected networks for classification.

The first extension is to allow stages to have a different number of blocks. To verify the goodness of this extension, we design two kinds of MBConv-based supernet with 20 blocks in total: a supernet with constant depth (baseline), a supernet with linear depth where the cumulative depth up to a specific stage is proportional to the width of the stage.

Table 4: Comparison of two MBConv-based supernets with different block assignment schemes to stages

| strategy       | accuracy (%) | latency (ms) |
|----------------|--------------|--------------|
| constant (baseline) | 75.85        | 1.28         |
| linear         | 77.09        | 1.24         |

As shown in Table 4, a supernet with linear depth outperforms a supernet with constant depth in terms of accuracy with similar latency. It confirms that this simple change of block assignment in supernet gives notable accuracy boost with the same latency constraint, without any additional optimization techniques.

Table 5: Comparison of two supernets with different building blocks: MBConv and MixConv

| building block | accuracy (%) | latency (ms) |
|----------------|--------------|--------------|
| DWConv (baseline) | 75.85        | 1.28         |
| MixConv        | 76.58        | 1.30         |

The second extension is to use multiple parallel superkernels in an MBConv block. To verify the benefit of it, we compare two different supernets with the same number of blocks in each stage. The accuracy and latency performance of the baseline supernet is the same as the previous experimental result shown in Table 4. Table 5 shows that the extended supernet with MixConv-based building blocks gives a better accuracy-latency tradeoff.

5.3 Comparison with existing models

We apply the proposed NAS method with the supernet architecture described above. The depth of 5 stages is set to 3, 4, 7, 4, 11, respectively. The latency constraint is set to 2.5 ms that corresponds to the latency of EfficientNet-B1 on our target NPU, MIDAP. Table 6 compares our search results with the state-of-the-art models: EdgeTPU [9], EfficientNet [32], Once-For-All [1]. The latency of the other models is obtained by running the network on the MIDAP cycle-accurate simulator. We compare the accuracy without quantization, assuming that quantization effects will be similar to all models.

As shown in Table 6, the baseline model, ours-M, found by the proposed NAS technique has higher accuracy than the other models on our target NPU; ours-M achieves more than 1.7% higher top-1 accuracy than EfficientNet-lite2 with similar latency. Moreover, it is 0.5% higher than EfficientNet-B1, even without using SE and h-swish activation function. Note that the number of parameters and the number of FLOPS in ours-M is larger than EfficientNet-B1. It implies that the complexity of the network is not a direct indicator of the end-to-end latency of the network. The end-to-end latency depends on the NPU architecture, and the proposed NAS technique could find a larger network with shorter latency by adding the latency factor to the loss function directly. The main benefit comes from different block assignment to stages.

We improve the baseline network by adding the h-swish activation function and squeeze-and-excitation(SE) block to get the ours-M+ model. Figure 12 shows the topology of ours-M+ architecture in which the height of each block is proportional to the expansion ratio of the block. Compared with the baseline network, ours-M, we achieve around 1% accuracy boost with ours-M+, paying the cost of 16% latency increase. This model outperforms the other models, 0.5% higher accuracy and 14% faster than EfficientNet-B1. Since EfficientNet-B2 is too large to run with the default configuration on MIDAP, we increase the memory size for filter weights.

Next, we applied compound scaling [32] to ours-M+ to obtain ours-L+ and ours-XL+. When we determine scaling coefficients, we keep the linear relationship between the cumulative depth and width of each stage, and scale the input image size more aggressively than [32]. We make the number of filters to be multiples of 16 to maximize the MAC unit utilization on MIDAP. When we train our scaled model, we set the dropout ratio to 0.4, similar to EfficientNet-B4 training. The accuracy of ours-L+ is higher than EfficientNet-B3 and EfficientNet-lite4, while the accuracy of ours-XL+ is similar to EfficientNet-B4. Note that the difference between the searched network and the EfficientNet decreases as the network size increases.
Table 6: Performance comparison among network models with the ImageNet dataset. (∗: Trained again with official EfficientNet code using baseline preprocessing only. ††: We convert the wall clock time to GPU-hours [29] to compare with the other methods. +: using squeeze-excitation and the h-swish function. ‡: When we compare the search cost, we compare the time needed to get one final architecture. ‡: The search time contains training time.)

| Model                  | FP32 Top-1 acc(%) | latency(ms) | #Params | #FLOPS | Search Cost(h) |
|------------------------|-------------------|-------------|---------|--------|----------------|
| EdgeTPU-S [9]          | 77.23             | 4.41        | 5.4M    | 2.35B  | 40,000         |
| Inception V3 [30]      | 78.8              | 6.75        | 23.8M   | 5.71B  | manual         |
| EfficientNet-B1 [32]   | 78.8              | 2.47        | 7.8M    | 0.69B  | 40,000         |
| EfficientNet-lite2 [32]| 77.6              | 2.51        | 6.1M    | 0.86B  | 40,000         |
| random selection       | 78.55~79.19       | 2.45~2.49   | 8.7M~11.0M | 0.97B~1.14B | 720(7200)‡    |
| random search          | 78.93             | 2.49        | 10.4M   | 1.06B  | (30)††         |
| ours-M                 | 79.35             | 2.47        | 12.8M   | 1.29B  | (30)††         |
| EdgeTPU-M [9]          | 78.69             | 6.86        | 6.9M    | 3.66B  | 40,000         |
| EfficientNet-B2 [32]   | 79.8              | 3.50        | 8.2M    | 1.38B  | 40,000         |
| EfficientNet-lite3 [32]| 79.8(79.15)**     | 3.50        | 8.2M    | 1.38B  | 40,000         |
| Once-For-All [1]       | 80.0(78.50)*      | 2.18        | 9.1M    | 0.60B  | 1,200‡         |
| ours-M+                | 80.28             | 2.86        | 15.4M   | 1.29B  | (30)††         |
| EfficientNet-B3 [32]   | 81.0              | 5.22        | 12.2M   | 1.83B  | 40,000         |
| EfficientNet-lite4 [32]| 81.5(80.38)**     | 5.84        | 13.0M   | 2.55B  | 40,000         |
| ours-L+                | 81.49             | 5.23        | 20.7M   | 2.47B  | (30)††         |
| EdgeTPU-L [9]          | 80.62             | 15.55       | 10.6M   | 9.66B  | 40,000         |
| EfficientNet-B4 [32]   | 82.6              | 11.42       | 19.3M   | 4.39B  | 40,000         |
| ours-XL                | 82.67             | 11.87       | 27.9M   | 5.95B  | (30)††         |
| ours-XL-rmSE+          | 82.72             | 11.66       | 26.9M   | 5.95B  | (30)††         |

Finally, we selectively removed SE blocks from ours-XL+, resulting in ours-XL-rmSE+. We collected the activation values using randomly sampled 10K images from the training dataset and calculated the metric explained in Sec. 4.3.3. After removing SE blocks from ours-XL+ based on the metric, only about 60% of the blocks in the network have SE blocks. As a result, we could make the latency shorter, while the accuracy was slightly improved than ours-XL+. This model achieves 82.72% top-1 accuracy with only 11.66ms latency. It is much better than EfficientNet-EdgeTPU-L [9] that achieves 80.62% FP32 top-1 accuracy with more than 20ms on EdgeTPU. Our architecture on MIDAP is about 2 times faster with 2.1% higher accuracy.

Finally, we compare the search time. Since the TPU is faster than GPU, we report the wall clock time and the estimated GPU time (in parenthesis) that is 10 times longer than the wall clock time in the last column of Table 6. Our method takes 3 hours, which is much faster than the other methods. Note that we compare the total time to get one architecture from scratch without trained weights. Once-For-All [1] would require only short fine-tuning time after a neural architecture is searched. In contrast, we need to train the network after a network architecture is found. It took 40 hours on TPuv3 to train ours-M+.

5.4 Ablation Studies

5.4.1 Comparison with Random Search. While most NAS techniques are not compared with a random search method, the authors [18] reported that a random search method is highly competitive. So we conducted an experiment to compare the proposed NAS technique with two random search methods, exploring the same search space defined by the supernet structure of ours-M. First, we designed a simple random search method that has the similar time complexity of the proposed technique. In this method, we randomly generate 15 models having a similar latency with ours-M, from the same search space. Then we train each of them for 1 epoch with cosine learning rate decay. After evaluating each of them, we choose the architecture with the topmost top-1 accuracy. Since the random selection method performs search and training simultaneously, it is slower than the proposed technique by the number of randomly generated models.

Comparison results are reported in Table 6. It is confirmed that both random selection and random search are quite competitive, but noticeably inferior to ours-M in terms of accuracy. In detail, the worst case of random selection showed 0.8% lower accuracy than ours-M. The best performance obtained from 20 randomly generated models is 79.19%, still lower than the accuracy of ours-M. Note that random search and random selection show similar performance that is no smaller than the other networks. It means
that the search space defined by the supernet architecture has a more significant effect on the accuracy than the search method.

Table 7: Comparison between compound scaling and direct search on large target latency.

|                  | accuracy (%) | latency (ms) |
|------------------|--------------|--------------|
| Compound scale   | 81.78        | 10.81        |
| Direct search    | 81.87        | 10.84        |

5.4.2 Comparison between compound scaling and direct search. There are two methods to find an architecture with a loose latency constraint. One is to use compound scaling that scales a small network with shorter latency, and the other is to search a network directly. To compare these two methods, we first scaled ours-M using the same scaling coefficients that we used to scale ours-M+ to ours-L+ and trained it. When conducting a direct search, we scaled the depth and width of the supernet and the input image size first and applied the proposed NAS technique for the scaled supernet. We used batch size 512 instead of 1024 during the architecture search due to the memory limitation of TPU. The comparison result is shown in Table 7 in terms of top-1 accuracy(%) and the latency on the target NPU(ms). Two results were similar while direct search needed 10 hours on TPUv3; It means that compound scaling is an effective method to find a large network fast.

Table 8: Impact of SE and h-swish on accuracy.

|                  | ReLU | h-swish |
|------------------|------|---------|
| w/o SE           | 79.35| 79.36   |
| w SE             | 80.04| 80.28   |

5.4.3 Affect of SE and h-swish. To examine how SE and h-swish impact accuracy individually, we compare four combinations as displayed in Table 8. The baseline is ours-M that does not use SE and h-swish activation function. Replacing ReLU with h-swish gives a marginal improvement on accuracy while adding SE blocks improves the accuracy noticeably. Adding both SE and h-swish activation function improves the accuracy by around 1%.

6 CONCLUSION

In this work, we propose a fast NPU-aware NAS methodology extending the Single-Path NAS technique [28]. We modify the supernet architecture by varying the number of blocks in stages and adding mixed depthwise convolution [33] to the search space. By modifying the loss function to directly include the target latency estimated by a cycle-accurate simulator of the target NPU, we could find a better baseline architecture with a shorter latency than the latency constraint. Using a tight latency constraint, we can reduce the search space to find the baseline network fast. Afterward, we apply compound scaling to find a larger network than the baseline network, and add SE blocks and h-swish activation functions in the post-processing step. Through the proposed NAS methodology, we could obtain a network with 82.72% accuracy with 11.66ms latency on our target NPU, without special data augmentation in training. It dominates the existing network models on the target NPU. It confirms the importance of supernet architecture design for a given NPU and effectiveness of the three-step approach in the proposed NAS methodology: supernet design, SinglePath NAS with a tighter latency constraint, and compound scaling and post-processing.

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