Convolutional neural networks (CNNs) are typically trained using 16- or 32-bit floating-point (FP). Lower precision is often sufficient for inference, most commonly 8-bit integer values. However, recent research has shown that low-precision FP can be highly effective for inference. Low-precision FP can be implemented in hardware FPGA and ASIC accelerators, but existing processors do not, in general, support custom precision FP.

We propose hardware optimized bit-sliced floating-point operators (HOBFLOPS), a method of generating efficient custom-precision emulated bitsliced software FP arithmetic. We generate custom-precision software FP routines using a hardware design flow. An FP unit generator creates high-level FP arithmetic hardware descriptions, and we use a standard hardware design flow to optimize and synthesize these designs into circuits. We provide standard cell libraries that match the bitwise operations on the target microprocessor architecture, and a custom code-generator to translate the resulting circuits to bitslice software equivalents. We exploit bitslice parallelism to create a very wide (32–512 element) vectorized CNN convolution.

Experiments show that HOBFLOPS provides a fast approach to emulating custom, low-precision FP in software. We demonstrate implementing various widths of HOBFLOPS multiplier and adder in the multiply-accumulate (MAC) of a CNN convolution. The HOBFLOPS optimized C/C++ MAC performance of the convolution on Arm Neon, Intel AVX2, and AVX512 processors is compared to the Berkeley’s SoftFP16 equivalent MAC. Implemented on an Intel AVX512, SoftFP16 performs at around 50 million MACs/second, and HOBFLOPS16 performs at 414 million MACs/second, approximately 8× the performance. HOBFLOPS16 on Arm Neon achieves approximately 0.5× the performance of SoftFP16, and on AVX2 platform HOBFLOPS16 achieves 2.5× the performance of SoftFP16. HOBFLOPS also offers arbitrary-precision FP with custom range and precision, e.g., FP9 containing a 1-bit sign, 5-bit exponent and 3-bit mantissa. We show HOBFLOPS9 performs at approximately 2 billion MACs/second on an AVX512, around 5× the performance of HOBFLOPS16. HOBFLOPS allows researchers and hardware developers to prototype different levels of custom FP precision for use in the arithmetic of CNN accelerators. Furthermore, HOBFLOPS fast custom-precision FP CNNs in software may be valuable in cases where memory bandwidth is limited.
We propose hardware optimized bit-sliced floating-point operators (HOBFLOPS) which offers arbitrary-precision FP arithmetic, using software bitslice [27] arithmetic. We generate efficient arbitrary-precision software FP emulation types and arithmetic, optimized using hardware tools and converted to the host processor bitwise logic instructions. HOBFLOPS supports bitwise instructions from vector instruction processors such as Intel’s AVX512, and Arm NEON processors, but is not dependent upon vector processors to perform efficiently.

HOBFLOPS supports the emulation of any required precision of FP arithmetic at any bit-width of mantissa or exponent. However, to evaluate performance we demonstrate HOBFLOPS8–HOBFLOPS16e MACs in CNN convolution, implemented on Arm Neon, Intel AVX2 and AVX512 processors, demonstrating arbitrary-precision performance. We compare the performance of HOBFLOPS16 MAC to Berkeley’s SoftFP16 MulAdd [14] both implemented on AVX2 and AVX512 processors, showing HOBFLOPS offers significant performance boosts.

We make the following contributions:

- We present a full design flow from a VHDL core generator to arbitrary-precision software bitslice FP operators, optimized using hardware design tools and our logic cell libraries, and our domain-specific code generator;
- We demonstrate how 3-input Arm NEON bitwise instructions e.g., SEL (multiplexer) and AVX512 bitwise ternary operations can be used in standard cell libraries to improve the efficiency of the generated code greatly;
- We present an algorithm for implementing CNN convolution with the very wide vectors that arise in bitslice vector arithmetic;
- We evaluate various widths of HOBFLOPS from HOBFLOPS8–HOBFLOPS16e and find e.g., HOBFLOPS9 performs at approximately 45 million MACs/second on Arm Neon processor around 6× that of HOBFLOPS16, and 2 billion MACs/second on an Intel AVX512 platform, around 5× that of HOBFLOPS16;
- We also evaluate HOBFLOPS16 on Arm Neon and Intel AVX2 and AVX512 processors and find our approach achieves approximately 0.5×, 2.5×, and 8× the performance of SoftFP16 respectively. The increased performance is due to:
  - Bitslice parallelism of the very wide vectorization of the MACs of the CNN;
  - Our efficient code generation flow.

The rest of this article is organized as follows. Section 2 gives background on other CNN accelerators use of low-precision arithmetic types. Section 3 outlines bitslice operations and introduces HOBFLOPS, shows the design flow, types supported and how to implement arbitrary-precision HOBFLOPS FP arithmetic in a convolution layer of a CNN. Section 4 shows results for HOBFLOPS8–HOBFLOPS16e emulation implemented on Arm Neon, Intel AVX2 and AVX512 processors. We compare HOBFLOPS16 to Berkeley SoftFP16 on Intel’s AVX2 and AVX512 processors and show significant increases in performance. We outline related work in Section 5 and conclude with Section 6.

2 BACKGROUND

Reduced-precision CNN inference, particularly weight data of CNNs, reduces computational requirements due to memory accesses, which dominate energy consumption. Energy and area costs are also reduced in application-specific integrated circuits (ASICs) and field programmable gate arrays (FPGAs) [26].

Kang et al., [23] investigate short, reduced FP representations that do not support not-a-numbers (NANs) and infinities. They show that shortening the width of the exponent and mantissa reduces the computational complexity within the multiplier logic. They compare fixed point integer representations with varying widths up to 8-bits of their
short FP in various CNNs, and show around a 1% drop in classification accuracy, with more than 60% reduction in ASIC implementation area.

Researchers often use custom precision in the design of arithmetic accelerators implemented in hardware such as FPGA or ASIC. For their Project Brainwave [6, 10], Microsoft proposes MS-FP8 and MS-FP9, which are 8-bit and 9-bit FP arithmetic that they exploit in a quantized CNN [6, 10]. Microsoft alters the Minifloat 8-bit that follows the IEEE-754 specification (1-sign bit, 4-exponent bits, 3-mantissa bits) [18] slightly for more efficient implementation in a FPGA by creating MS-FP8, of 1-sign bit, 5-exponent bits, and 2-mantissa bits. MS-FP8 gives a larger representative range due to the extra exponent bit but lower accuracy than Minifloat, caused by the reduced mantissa. However, this more than doubles the performance on a Intel Altera Stratix V D5 FPGA running at 225MHz to 4.5 tera floating-point operations per seconds (FLOPS) (TFLOPS) when compared to the 2.0 TFLOPS for 8-bit integer operations. This performance increases to more than 90 TFLOPS on the 14nm Stratix 10 280 FPGA running at 500MHz. To improve the precision, they propose MS-FP9, which increases the mantissa to 3 bits and keeps the exponent at 5 bits. The MS-FP8 / MS-FP9 bit-widths are suitable for FPGA implementation and application of neural net acceleration in Microsoft data centers. Their later work [10] uses a shared exponent with their proposed MS-FP8 / MS-FP9, i.e., one exponent pair used for many mantissae, something this work does not investigate.

Other researchers investigate optimizing different representations of FP arithmetic. Xu et al., [27] propose bitslice arithmetic and present FP calculations undertaken on a fixed point unit. Instead of storing vectors in the traditional sense of storing 17-bit vectors inefficiently in a 32-bit register, they instead store thirty-two 17-bit words transformed into bitsliced format and stored in memory. Xu et al., manually construct bitwise arithmetic routines to perform integer or FP arithmetic, while the vectors remain in a bitsliced format. When coded in C/C++ and AVX2 single instruction multiple data (SIMD) instructions, they demonstrate this approach is efficient for low-precision vectors, such as 9-bit or 11-bit arbitrary FP types.

3 APPROACH

In this section, we present our approach to producing HOBFLOPS arithmetic units that we demonstrate in the convolution layer of a CNN. HOBFLOPS is a method for generating efficient software emulation FP arithmetic units optimized using hardware synthesis tools. Figure 1 outlines our flow for creating HOBFLOPS arithmetic units. We generate the register transfer logic (RTL) representations of arbitrary-precision FP multipliers and adders using the FP unit generator, FLOating-POint COres (FloPoCo). We use the ASIC synthesizer tool, Cadence Genus, in conjunction with our hardware cell libraries and tool command language (TCL) automation script to synthesize the adders and multipliers into Verilog netlists. The open-source synthesis and technology mapping suite, Yosys-ABC, allows us to optimize further and topologically sort the netlists. Our custom-code generator converts the topologically sorted netlists into a C/C++ header of bitwise operations. In parallel, we convert the hardware cell libraries into the equivalent C/C++ cell library headers. We create a CNN convolution layer to include the HOBFLOPS adder and multiplier header and cell library header corresponding with the target processor architecture, and compile with G++.

3.1 Arm Neon, Intel AVX2 and AVX512 Cell Libraries

We create three Synopsys Liberty [25] standard cell libraries supporting the equivalent hardware gate-level representations of Arm Neon [2], Intel’s X86.64, AVX, AVX2 and Intel’s AVX512 intrinsic SIMD vector instructions [20]. The Arm Neon SEL (multiplexer) bitwise multiplexer instruction is a 3-input gate, whereas all other gates modeled in the cell library are 2-input. The ternary logic look up table (LUT) of the Intel AVX512 is a three-input gate that can implement three-input boolean functions. An 8-bit immediate operand to this instruction species which of the 256 three
Fig. 1. Flow for Creating the HOBFLOPS Bitwise Operations.

Table 1. Bitwise Logic Operations Supported in Cell Libraries

| Arm (64-bit) | Arm Neon (128-bit) [2] | Intel (64-bit) | Intel AVX2 (128-, 256-bit) | Intel AVX512 (512-bit) [20] |
|--------------|------------------------|----------------|---------------------------|---------------------------|
| AND A & B    | AND A & B              | AND A & B      | AND A & B                 | LUT000 0                  |
| OR A | B                 | OR A | B                 | OR A | B                 | LUT001 (A | (B | C)) ~ 1          |
| XOR A ` B    | XOR A ` B             | XOR A ` B      | XOR A ` B                 | LUT002 ~ (B | A) C            |
| NOT ~A       | NOT ~A                | NOT ~A         | NOT ~A                    | LUT003 (B | A) ~ 1            |
| ORN A & (~B) | ORN A | ~B                | ORN A | ~B                | LUT004 ~(A | C) B            |
| SEL (~((S & A) | (~S & B))) |                    |                  | LUT005 (C | A) ~ 1            |
|              |                        |                | ANDNOT ~A & B             | ... (truncated)           |
|              |                        |                |                          | LUT253 A | (C ` 1))           |
|              |                        |                |                          | LUT254 A | (B | C)            |
|              |                        |                |                          | LUT255 1                |
input functions should be used. We create all 256 equivalent cells in the Liberty cell library when targeting AVX512 devices. Table 1 lists the bitwise operations supported in the cell libraries for each architecture. The AVX512 column shows a truncated example subset of the available 256 gates; see Intel’s Intrinsics Guide [20] and Software Developers manual [19] for the complete set.

To demonstrate the capabilities of the cell libraries, we show an example of a single bit full adder. Figure 2a shows a typical 5-gate full adder implemented with our AVX2 cell library. The same full adder can be implemented in three Arm Neon gates, Figure 3, one of which is the SEL bitwise multiplexer instruction. Intel AVX512 intrinsics can implement the full adder in two three-input bitwise ternary instructions, Figure 2b. While the inputs and outputs of the hardware gate level circuits are single bits, these IO are parallelized by the bit-width of the SIMD vector registers and instructions, which, when converted to bitwise software operations, produce vast parallel scaling of the arithmetic.

3.2 Bitsliced Operations

HOBFLOPS exploits bitslice operations to represent FP numbers in a bitwise manner that are processed in parallel. For example, 512 9-bit values are transformed to bitslice representations, see Figure 4. A simple example of how nine registers of 512-bit bitsliced data are applied to a 512-bit wide bitsliced FP adder is shown in Figure 5. Each instruction within the adder has a throughput of around half a clock cycle (see Intel’s Intrinsics Guide for details of the precise throughput of each of the SSE, AVX2 and AVX512 logic Bitwise Operations [20] and Arm’s Intrinsics Reference [2] for details of Arm Neon bitwise operational throughput). In this example, The adder’s propagation delay is related to the
number of instruction-level parallelism and associated load/store commands. The number of gates in the HOBFLOPS
Table 2. HOBFLOPS MAC Types

| Inputs Bit Width | Outputs Bit Width | Range            |
|------------------|-------------------|-------------------|
| Expo | Mant | Expo | Mant | Range          |
| Soft FP16        | 5 10 | 5 10 | -65504 to 65504 |
| HOBFLOPSIEEE8    | 4 3 4 4 | -496 to 496      |
| HOBFLOPSIEEE8e   | 4 3 4 7 | -510 to 510      |
| HOBFLOPS8        | 5 2 5 3 | -123000 to 123000|
| HOBFLOPS8e       | 5 2 5 5 | -129000 to 129000|
| HOBFLOPS9        | 5 3 5 4 | -127000 to 127000|
| HOBFLOPS9e       | 5 3 5 7 | -130600 to 130600|
| HOBFLOPS10       | 5 4 5 5 | -129000 to 129000|
| HOBFLOPS10e      | 5 4 5 9 | -130940 to 130940|
| HOBFLOPS11       | 5 5 5 6 | -130000 to 130000|
| HOBFLOPS11e      | 5 5 5 11 | -131040 to 131040|
| HOBFLOPS12       | 5 6 5 7 | -130600 to 130600|
| HOBFLOPS12e      | 5 6 5 13 | -131064 to 131064|
| HOBFLOPS13       | 5 7 5 8 | -130800 to 130800|
| HOBFLOPS13e      | 5 7 5 15 | -131070 to 131070|
| HOBFLOPS14       | 5 8 5 9 | -130940 to 130940|
| HOBFLOPS14e      | 5 8 5 17 | -131071.5 to 131071.5|
| HOBFLOPS15       | 5 9 5 10 | -131010 to 131010|
| HOBFLOPS15e      | 5 9 5 19 | -131071.88 to 131071.88|
| HOBFLOPS16       | 5 10 5 11 | -131040 to 131040|
| HOBFLOPS16e      | 5 10 5 21 | -131071.97 to 131071.97|

adder or multiplier is dependent on the required HOBFLOPS precision, see Table 2 for examples of HOBFLOPS MAC precision, and Section 4 for associated HOBFLOPS MAC gates counts and performance.

3.3 Design Flow

We investigate whether bitsliced logic can be optimized using hardware tools to reduce the hardware logic gate count or area, and subsequent lines of bitwise software operations. We use the industry-standard hardware ASIC synthesizer, Cadence Genus, with our custom-designed logic cell libraries to optimize the bitslice FP arithmetic.

Taking inspiration from Microsoft’s MS-FP8 / MS-FP9 [6, 10] and Minifloat 8-bit that follows the IEEE-754 specification [18], we create single-precision and extended-precision HOBFLOPS adders and multipliers. For example, we create the single-precision HOBFLOPS8 multiplier to take two 5-bit exponent, 2-bit mantissa, 1-bit sign inputs, and produce a single 5-bit exponent and 3-bit mantissa and 1-bit sign output. We also create extended-precision HOBFLOPS8e multiplier to take two 5-bit exponent, 2-bit mantissa, and 1-bit sign to produce a single 5-bit exponent, 5-bit extended mantissa and 1-bit sign output. Details of all demonstrated HOBFLOPS are in Table 2, although, other arbitrary combinations of mantissa and exponent bit-widths are supported in the flow (see Figure 1).

FloPoCo [7], the FP unit generator, generates VHDL [17] RTL descriptions of FP adders and multipliers of varying exponent and mantissa bit-widths for standard and extended precision HOBFLOPS types, see Table 2. Figure 6 shows an example of the HOBFLOPS8 multiplier logic produced by FloPoCo when synthesized with our Arm Neon cell Library, and shows the Arm SEL (multiplexer) gate in use. As a baseline of area and performance, we produce the 16- and 16e-bit IEEE-754 FP versions of the multiplier and adder, for comparison against Berkeley’s SoftFP16. FloPoCo automatically produces the corresponding VHDL test benches and test vectors required to test the generated cores. FloPoCo has a slightly different way of encoding the FP numbers when compared to the IEEE 754-2019 specification and does not support subnormal numbers. A FloPoCo FP number [7] is a bit-vector consisting of the following 4 fields: 2-bit exception
field (01 for normal numbers); a sign bit; an exponent field \(wE\) bits wide; a mantissa (fractional) field \(wF\) bits wide. The significand has an implicit leading 1, so the fraction field \(ff...ff\) represents the significand 1.ff...ff.

We configure FloPoCo to generate combinatorial plain RTL VHDL cores with a 1MHz frequency, no pipelining, and no use of hard-macro FPGA multipliers or adders. These settings ensure that FloPoCo generates reduced area rather than reduced latency multipliers and adders. We simulate the FP multipliers and adders in a VHDL simulator with the corresponding FloPoCo generated test bench to confirm that the quantized functionality is equivalent to IEEE-754 FP multiplier and adder.

We create Synopsys Liberty [25] standard cell libraries to support the target processor architecture. Cadence Genus (version 16.22-s033_1) [5], the industry-standard ASIC synthesis tool, synthesizes the adder and multiplier VHDL cores with our standard cell libraries and configuration TCL script [24] into a Verilog [16] netlist of the logic gates. See Figure 6 for an example of a HOBFLOPS8 multiplier targeted at the Arm Neon logic gate SIMD instructions. Note how Genus has synthesized the design to include the 3-input SEL gate (multiplexer) supported by Arm Neon.

All HOBFLOPS designs are combinatorial, so synthesis timing constraints are not required. In the standard cell libraries Liberty file, we assign a value of 1.0 to the cell area and cell leakage power of all the cells. The value of 1.0 ensures that the synthesizer assigns equal optimization priority to all gates and produces a netlist with the least number of logic gates rather than creating a netlist optimized for hardware timing propagation.

We further optimize the netlist using the open-source Yosys ASIC synthesizer [4] and ABC optimizer [3]. We use ABC’s strash command to transform the current network into an AND-inverter graph (AIG) by one-level structural hashing. We then use the refactor function to iteratively collapse and refactor the levels of logic and area of the netlist. Our TCL script configures Yosys to produce a topologically sorted Verilog netlist of logic gates. The topological sorting is required as Cadence Genus writes the netlist file in an output port to input port order, whereas the C/C++ compiler requires the converted netlist to have input to output ordering. We formally verify the topologically sorted netlist against the original netlist with Yosys satisfiability (SAT)-solver. These netlists are re-simulated with the test bench used to simulate the FloPoCo generated VHDL designs and compared for correlation.

Our conversion script translates the Verilog adder and multiplier netlists to Intel AVX2, AVX512, or Arm Neon bitwise operators with the correct types and pointers. Figure 9 shows a snippet of code of the HOBFLOPS8 multiplier, with 81 bitwise operations, referenced from the cell library of Figure 8. A single input bit of the hardware multiplier becomes...
The corresponding architecture type, e.g., uint64 for a 64-bit processor, an __mm256i type for an AVX2 processor, an __mm512i type for an AVX512 processor, uint32x4_t type for a Neon processor.

### 3.4 CNN Convolution with HOBFLOPS

We present a method for CNN convolution with HOBFLOPS arithmetic. We implement HOBFLOPS MACs in a CNN convolution layer, where up to 90% of the computation time is spent in a CNN [8]. We perform data layout transformations of the input feature map (IFM) and kernel weight data into bitslice format. We compare HOBFLOPS MAC performance to IEEE FP MAC and to Berkeley’s SoftFP16 MulAdd function [14].
void hobFlopsMul(__m256i *_restrict_ X, __m256i *_restrict_ Y, __m256i *_restrict_ R) {
    AND2X1(&X[0], &Y[0], &n_9);  // Intel AVX2 AND Gate from AVX2 Intrinsics Cell Library
    OR2X1(&n_9, &Y[1], &n_19);  // Intel AVX2 OR Gate from AVX2 Intrinsics Cell Library
    AND2X1(&n_19, &X[1], &n_25);
    AND2X1(&X[0], &Y[1], &n_8);
    . . . . . .  // Code Truncated
    ANDNOT2X1(&n_20, &n_19, &n_21); // Intel AVX2 ANDNOT Gate from AVX2 Intrinsics Cell Library
    XOR2X1(&n_21, &X[1], &R[2]);  // Intel AVX2 XOR Gate from AVX2 Intrinsics Cell Library
    XOR2X1(&X[7], &Y[7], &R[8]);
    XOR2X1(&X[0], &Y[0], &R[1]);
}

Fig. 9. Code Snippet of AVX2 HOBFLOPS8 Multiplier - 81 Bitwise Operations.

1 const exp signed NINBITS = 10;  // HOBFLOPs Input, 2−exc, 1−sign, 5−mant, 2−exp bits
2 const exp signed NOUTBITS = 11; // HOBFLOPs Output, 2−exc, 1−sign, 5−mant, 3−exp bits
3 const exp signed PADDED_BYTES = (NINBITS/8) + ((NINBITS%8) ? 1 : 0); // Byte padding if needed
4 const exp signed HOBFLOPS_KERNELS_TILE = (M/ LANES);  // Nr. tiles for M kernels
5 const exp signed TRUE_KERNELS_SIZE = (HOBFLOPS_KERNELS_TILE * NOUTBITS);  // Nr. __m256i to store kernels
6 for (h = 0; h < IFM_H; h++) {
7    for (w = 0; w < IFM_W; w++) {
8        for (kh = -(K / 2); kh <= ( K / 2); kh++) {
9            if (h+kh >= 0 && h+kh < IFM_H) {
10                for (kw = -(K / 2); kw <= ( K / 2); kw++) {
11                    if (w+kw >= 0 && w+kw < IFM_W) {
12                        __m256i hoblopsSumRes[NOUTBITS] = _mm256_setzero_si256();
13                        for (c = 0; c < C; c++) {
14                            __m256i hoblopsMulRes[NOUTBITS] = _mm256_setzero_si256();
15                            __m256i hoblopsBcastIfm[NOUTBITS] = _mm256_setzero_si256();
16                            uint_t * ifmPtr = &(ifm[(h) * (IFM_W * (C * PADDED_BYTES)) + (w) * (C * PADDED_BYTES) + (c * PADDED_BYTES)]);
17                            ifm_broadcast_scalar(ifmPtr, &hoblopsBcastIfm[0]));  // IFM broadcast Function
18                            __m256i * kerPtr = &(ker[(kh+(K/2)) * K_SIZE * C * TRUE_KERNELS_SIZE + (kw+(K/2)) * C * TRUE_KERNELS_SIZE + (c) * TRUE_KERNELS_SIZE + (m * NOUTBITS)]);
19                            hobFlopsMulWrap(&hoblopsMulRes[0], &kerPtr);
20                            &hoblopsMulRes);  // HOBFLOPs Multiplier with load/stores
21                            hobFlopsAddWrap(&hoblopsMulRes[0], &hoblopsSumRes[0]), &hoblopsSumRes[0]);  // HOBFLOPs Adder with load/stores
22                        }
23                        } } } } } }
24}
25
26 Fig. 10. Simplified Code Snippet of AVX2 HOBFLOPS8 Convolution Loop.

Figure 7 shows HOBFLOPS IFM and kernel values convolved and stored in the output feature map (OFM). To reduce cache misses, we tile the IFM H × W × C dimensions, which for Conv dw / s2 of MobileNets CNN is 14 × 14 × 512 = 100,352 elements of HOBFLOPS IFM values. We tile the M kernel values by LANES × NINBITS, where LANES corresponds to the target architecture registers bit-width, e.g., 512-lanes corresponds to AVX512 512-bit wide register.
The \( \text{LANES} \times \text{NINBITS} \) tiles of binary values are transformed to \( \text{NINBITS} \) of machine-type values, where machine-type correspond to the target architecture register width, e.g., \text{uint64} \) type for a 64-bit processor architecture, \text{__mm512i} \) type for \text{AVX512} \) processor.

We broadcast the IFM channel tile of \( \text{NINBITS} \) across the corresponding channel of all the kernels tiles of \( \text{NINBITS} \) to convolve image and kernel values using \text{HOBFLOPS} \) multipliers, adders and rectified linear unit (ReLU) activation function. The resultant convolution machine-type values of \( \text{NOUTBITS} \) wide are stored in corresponding location tiles in the OFM. The HOBFLOPS IFM and kernel layout for single-precision, as defined by FloPoCo is:

\[
\text{NINBITS} = \text{EXCEPTION\_BITS} + \text{SIGN\_BIT} + \text{EXponent\_IN\_BITS} + \text{MANTISSA\_IN\_BITS}
\]

The HOBFLOPS OFM layout for single-precision is:

\[
\text{NOUTBITS} = \text{EXCEPTION\_BITS} + \text{SIGN\_BIT} + \text{EXponent\_IN\_BITS} + \text{MANTISSA\_IN\_BITS} + 1
\]

and for extended-precision:

\[
\text{NOUTBITS} = \text{EXCEPTION\_BITS} + \text{SIGN\_BIT} + \text{EXponent\_IN\_BITS} + (2 \times \text{MANTISSA\_IN\_BITS}) + 1
\]

For example, HOBFLOPS9, as can be seen in Table 2, the input layout \( \text{NINBITS} \) has 2-bit exception, 1-bit sign, 5-bit exponent, 3-bit mantissa which added comes to 11-bits. The single-precision \( \text{NOUTBITS} \) would be 12-bits (essentially \( \text{NINBITS} + 1 \)). The extended-precision \( \text{NOUTBITS} \) would be 15-bits.

If HOBFLOPS is implemented in a multi-layer CNN, the data between each layer could remain in HOBFLOPS format until the last convolution layer. The OFM at the last convolutional layer could be transformed from HOBFLOPS values to floats resulting in the transformation overhead only occurring at the first and last convolutional layers of the CNN model. An additional pooling layer could be developed in the HOBFLOPS format, for the interface between the last convolutional layer and the fully connected layer of MobileNets, not done in this work.

A simplified convolution loop, see Figure 10, shows an example of how the bitsliced FP IFM is broadcast across the kernels, loaded into SIMD registers, multiplied and accumulated using the HOBFLOPS multiplier and adder, and OFM result tile stored in the output register. The broadcast of the IFM is handled in the \text{ifm\_broadcast\_scalar} \) routine (not show). We repeat the above for MACs up to HOBFLOPS16e on each processor architecture.

### 4 EVALUATION

We implement each of the 8- to 16e-bit HOBFLOPS multipliers and adders in a convolution layer of the MobileNets CNN [15]. We use layer \text{Conv dw / s2} \) of MobileNets as it has a high number of channels \( C \) and kernels \( M \), perfect for demonstrations of high-dimensional parallelized MAC operations. We compare the HOBFLOPS16 multipliers and adders round-to-nearest-ties-to-even and round-towards-zero modes performance to Berkeley’s efficient SoftFP16 MulAdd rounding near_even adn round min modes [14], and acts as a baseline as Soft FP8 is not supported by Berkeley’s emulation tool.

We target 32-bit to 512-bit registers for \text{AVX2} \) and \text{AVX512} \) processors and target 32- and 128-bit registers for the Cortex-A15 processor. We implement 32- to 512-lanes of HOBFLOPS multipliers and adders and capture each of the \text{AVX2} 32-, 64-, 128- and 256-bit, \text{AVX512} 32-, 64-, 128-, 256 and 512-bit, and Cortex-A16 32-, 64- and 128-bit results.

Three machine types are used to test the HOBFLOPS MAC:

- Arm Cortex-A15 Neon embedded development kit, containing an ARMv7 rev 3 (v7l) CPU at 2GHz and 2GB RAM;
- Intel Core-i7 PC, containing Intel Core-i7 8700K CPU at 3.7GHz and 32GB RAM;
- Intel Xeon Gold server PC, containing Intel Xeon Gold 5120 at 2.2GHz and 256GB RAM.
Our cell libraries model specific cells, see Table 1. We do not include the bit clear (BIC) of the Arm Neon in our cell library. Inclusion of bit clear (BIC) prevents the synthesis tool, Cadence Genus, from optimizing the netlist with SEL (multiplexer) units, leading to a less area efficient netlist.

To further decrease area and increase performance, we produce round-towards-zero versions of the HOBFLOPS8–HOBFLOPS16e adders as the rounding can be dealt with at the end of the layer in the activation function, assuming the non-rounded part of the FP value is retained through to the end of the layer.

The MACs per second of an average of 1000 iterations of a HOBFLOPS adders and multipliers are captured and compared. We use the GNU G++ compiler to optimize the code for the underlying target microprocessor architecture and numbers of registers. We compile the HOBFLOPS CNN code (see Figure 10) with our HOBFLOPS adders and multipliers (e.g. Figure 9 for AVX2), and our cell library (e.g., Figure 8 for AVX2) with G++ (version 8.2.1 20181127 on Arm, version 9.2.0 on Intel AVX2 and version 6.3.0 20170516 on Intel AVX512 machines). We target C++ version 17 and using −march=native, -mtune=native, -fPIC, -O3 compiler switches with -msse for SSE devices and -mavx2 for AVX2 devices. When targeting an Intel AVX512 architecture we use the the -march=skylake-avx512, -mtune=skylake-avx512, -mavx512f, -fPIC, -O3 switches. When targeting an Arm Neon device we use -march=native, -mtune=native, -fPIC, -O3, -mfpu=neon to exploit the use of Neon registers.

After the G++ compilation, we inspect the assembler object dump. Within the multiplier and adder units, we find an almost one-to-one correlation of logic bitwise operations in the assembler related to the gates modeled in the cell libraries, with additional loads/stores where the compiler has seen fit to implement.

4.1 Arm Cortex-A15

We configure an Arm Cortex-A15 Development kit with 2GB RAM, ARCH Linux version 4.14.107-1-ARCH installed, and fix the processor frequency at 2GHz. We run tests for 32-, 64- and 128-lanes and capture performance. We use taskset to lock the process to a core of the machine for measurement consistency.

Figure 11 shows 128-lane round-to-nearest-ties-to-even performance for all arbitrary-precision HOBFLOPS FP between 8- and 16e-bits, IEEE 8- and 32-bit equivalents and Berkeley’s SoftFP versions. HOBFLOPS16 round-to-nearest-ties-to-even achieves approximately half the performance of SoftFP16 MulAdd rounding near_even mode on Arm Neon. However, HOBFLOPS offers arbitrary precision FP between 8- and 16-bits and can be configured for any bit-width of mantissa and exponent of FP, outperforming SoftFP16 between HOBFLOPS8 and HOBFLOPS11 bits. Similarly, HOBFLOPS16 round-towards-zero version shown in Figure 12 demonstrates a slight improvement in performance compared to Berkeley’s SoftFP16 MulAdd rounding min mode. Figure 12 also shows HOBFLOPS round-towards-zero versions have an increased performance when compared to HOBFLOPS16 round-to-nearest-ties-to-even. The low bit-width and thus reduced hardware synthesis gate count or area as seen in Figure 13 and Figure 14 would benefit memory storage and bandwidth within the embedded system allowing for reduced energy consumption, however energy consumption is not measured here.

4.2 Intel AVX2

We configure an Intel Core i7-8700K desktop machine with 32GB RAM, and ARCH Linux 5.3.4-arch1-1 installed. For consistency of performance measurements of various HOBFLOPS configurations, within the BIOS we disable:

- Intel’s SpeedStep (i.e., prevent the CPU performance from ramping up and down);
- Multi-threading (i.e., do not split the program into separate threads);
- TurboBoost (i.e., keep all processor cores running at the same frequency);
Fig. 11. Arm Neon HOBFLOPS8-16e MACs Round-to-Nearest-Ties-To-Even Throughput - **higher is better**.

Fig. 12. Arm Neon HOBFLOPS8-16e MACs Round-Towards-Zero Throughput - **higher is better**.
Fig. 13. Arm Neon HOBFLOPS8-16e MAC Gate Count: Round To Nearest, Ties To Even - lower is better.

Fig. 14. Arm Neon HOBFLOPS8-16e MAC Gate Count: Round Towards Zero - lower is better.
Fig. 15. Intel AVX2 HOBFLOPS8-16e MACs Round-to-Nearest-Ties-To-Even Throughput - **higher is better**.

- Hyperthreading Control (*i.e.*, keep one program on one processor core);
- C-States control (*i.e.*, prevent power saving from ramping down the processor core clock frequency).

We alter the GRUB configuration so `intel_pstate` (*i.e.*, lock the processor core clock frequency in the Linux Kernel) and `intel_cstate` are disabled on both `GRUB_CMDLINE_LINUX` and `GRUB_CMDLINE_LINUX_DEFAULT`. This BIOS and Linux Kernel configuration ensures the processor frequency is fixed at 4.6GHz, no power-saving, and each HOBFLOPS instance running at full performance on a single thread and single CPU core. When executing the compiled code, `taskset` is used to lock the process to a single core of the CPU. These configurations allow a reproducible comparison of timing performance of each HOBFLOPS configuration against Berkeley’s SoftFP16.

We run tests for 32-, 64-, 128- and 256-lanes capture performance. Figure 15 shows 256-lane round-to-nearest-ties-to-even results for all arbitrary-precision HOBFLOPS FP between 8- and 16e-bits, IEEE 8- and 32-bit equivalents and Berkeley’s SoftFP versions. HOBFLOPS16 performs over 2.5× higher MACs/second when compared to Berkeley’s SoftFP16 `MulAdd` rounding near_even mode. The round-towards-zero version of HOBFLOPS16 performs at around 2.7× higher MACs/second when compared to Berkeley’s SoftFP16 `MulAdd` rounding min mode. In fact, HOBFLOPS outperforms SoftFP16 for all versions of between HOBFLOPS8 and HOBFLOPS16e for both round-to-nearest-ties-to-even and round-towards-zero rounding modes.

HOBFLOPS8 performance gain is due to reduced synthesis area of the HOBFLOPS units as seen in Figure 16. Again, this reduction in area, also seen for round-towards-zero, is key to reduced SIMD bitwise operations being created for the HOBFLOPS MACs and therefore reduced latency through the software HOBFLOPS MACs.
4.3 Intel AVX512

We configure an Intel Xeon Gold 5120 server-class machine with 256GB RAM, and Debian Linux 4.9.189-3+deb9u2 installed. As this is a shared server-grade machine, we cannot change the BIOS or pin the clock to its maximum frequency as done for the AVX2-based machine. However, taskset is used to lock the process to a single CPU core.

We run tests for 32-, 64-, 128-, 256- and 512-lanes and capture performance 512-lane performance. Figure 17 shows 512-lane round-to-nearest-ties-to-even results for all arbitrary-precision HOBFLOPS FP between 8- and 16e-bits, IEEE 8- and 32-bit equivalents and Berkeley’s SoftFP versions. HOBFLOPS16 performs with 8.2× greater MACs throughput when compared to Berkeley’s SoftFP16 MulAdd rounding near_even mode. For the 512-lane round-towards-zero results, HOBFLOPS16 performs at 8.4× the MACs throughput when compared to Berkeley’s SoftFP16 MulAdd rounding min mode. HOBFLOPS outperforms SoftFP16 for all versions of between HOBFLOPS8 and HOBFLOPS16e for both round-to-nearest-ties-to-even and round-towards-zero. HOBFLOPS9 performs at approximately 2 billion MACs/second, around 5× the performance of HOBFLOPS16.

HOBFLOPS performance is due to HOBFLOPS lower hardware synthesis area, which when the netlists are converted to software bitwise operations, translates to fewer SIMD 3-input ternary logic LUT instructions in the MACs. As seen in Figure 18, HOBFLOPS16 area on the AVX512 platform is 38% smaller than the HOBFLOPS16 area on AVX2. A further slight performance boost is seen for round-towards-zero.

5 RELATED WORK

Researchers investigate different bit precision and representations of the FP number base. Google’s tensor processing unit (TPU) ASIC [22] implements brain floating point 16-bit (bfloat16) [13], a 16-bit floating radix point format offering wide numerical dynamic range. Essentially, bfloat16 is a truncated IEEE-754 FP single-precision format. bfloat16
Fig. 17. Intel AVX512 HOBFLOPS-16e MACs Round-to-Nearest-Ties-To-Even Throughput - **higher is better**.

Fig. 18. Intel AVX512 HOBFLOPS-16e MAC Gate Count: Round To Nearest, Ties To Even - **lower is better**.
preserves dynamic range of the 32-bit format due to the 8-bit exponent. The precision is reduced in the mantissa from IEEE’s 24-bits down to 7-bits. bfloat16 is not restricted to machine learning; Intel Nervana use it in their network processing unit (NPU), Intel Xeon processors support AVX512 bfloat16 extensions, Intel Altera’s FPGAs use it, Arm’s ARMv8.6-A architecture, and ROCm libraries use bfloat16.

CNNs require a great deal of computation, so, many researchers focus on proposing methods of optimizing FP arithmetic within the CNNs either at the register level or the bit-precision level. Traditionally, researchers propose SIMD register and data path optimizations from within the compiler. An early example from Fisher et al., [9] is the SIMD within a register (SWAR) model which treats a wide data path within a processor as multiple, thin SIMD parallel data paths. This model accelerates arithmetic, allowing wide registers to be partitioned for smaller operations, such as subdividing 32-bit integer adders into eight 8-bit adders, assuming one adder’s carry to the next adder is suppressed.

Typically 32-bit or 64-bit precision FP arithmetic is used for inference or training of a CNN. Jeff Johnson at Facebook Research [21] shows the need for lower-power and faster performing artificial intelligence (AI) designs for mobile devices and data-centers for both inference and training. They suggest improving existing FP implementations to propose a more efficient FP arithmetic, which keeps the same precision and dynamic range while reducing power.

Garland et al., [11] show that they can vary the bit-width of their parallel accumulate shared MAC (PASM) between 4-bit and 32-bit in ASIC and maintain performance and accuracy while reducing power and area of the multiplier. In their follow up work, Garland et al., [12] show PASM can be implemented on an FPGA and vary the bit-width between INT8 and 32-bit, saving significant energy with only a slight increase in latency and no change in classification accuracy.

There are byte precision arithmetic accelerators in software. Anderson et al., [1] exploit the SIMD nature of the processor by proposing flytes, which is a scheme for byte-level customizable precision FP arithmetic in the SIMD vector registers. They use SIMD instructions to convert between the custom format and native FP while packing and unpacking the data into the vector registers.

Note there are converter tools, such as Verilator, that converts hardware description language (HDL) code like Verilog to C/C++. Verilator does not merely convert Verilog netlists to C/C++ as Verilator’s focus is on fast, optimized, threaded compiled C++ model of Verilog for simulation purposes. Verilator does not produce a circuit in a format convertible to bitwise instructions, something our custom code-generator does.

6 CONCLUSION

We introduce HOBFLOPS, a method of generating efficient custom-precision emulated bitsliced software FP arithmetic using a hardware design flow, our cell libraries and custom code-generator. We generate efficient arbitrary-precision emulated software multipliers and adders. We show that using these bitslice representations, HOBFLOPS retains FP-like accuracy at arbitrary-precision in multiplication and addition operations. HOBFLOPS is advantageous in CNN convolution for increased precision, accuracy and throughput. We also show that HOBFLOPS offers arbitrary-precision FP with custom range and precision values, useful for FP CNN acceleration where memory storage and bandwidth are limited.

We experiment with large numbers of channels and kernels in CNN convolution. When HOBFLOPS16 MAC is implemented in the convolution layer on Arm Neon and Intel AVX2 and AVX512 processors and compared to Berkeley’s SoftFP16 MulAdd FP emulation, HOBFLOPS achieves approximately 0.5×, 2.5× and 8× the performance of SoftFP16 respectively. We show e.g., HOBFLOPS9 performs at approximately 2 billion MACs/second on an AVX512, around 5× the performance of HOBFLOPS16 and approximately 45 million MACs/second on Arm Neon processor around 6× that of HOBFLOPS16.
The performance gains are due to the optimized hardware synthesis area of the MACs, which translates to fewer bitwise operations. Additionally, the bitslice parallelism of the very wide vectorization of the MACs of CNN convolution contributes to the performance boost. While we show results for 8- and 16-bit with a fixed exponent, HOBFLOPS supports the emulation of any required precision of FP arithmetic at any bit-width of mantissa or exponent, e.g., FP9 containing a 1-bit sign, 5-bit exponent and 3-bit mantissa, or FP11 containing a 1-bit sign, 5-bit exponent and 5-bit mantissa, not supported with other software FP emulation methods.

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