Reconfigurable and Storable Chaotic Logic Operations in Drive-Response VCSELs with Optical Feedback

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ABSTRACT Based on the system of drive-response vertical cavity surface emitting lasers (VCSELs) with optical feedback and the new electro-optic (EO) modulation theory, we propose a novel reconfigurable and storable logic operations scheme to perform the behaviors of flexible switching and delayed storage among different logic operations. Here, the optical feedback intensity is modulated into logic input, the applied electric field in drive system and response system are modulated into logical control signals, the logic output is decoded by threshold mechanism. When the logical control signal in drive system and response system remain equal and both of them satisfy different logic operation relationships with the logic inputs, the system can perform the mutual conversion and delayed storage among the logic operations such as AND, NAND, OR, NOR, XOR and XNOR. Furthermore, the half adder logic operations are also being realized. Finally, the influence of bit duration time and noise intensity on the reliability of the logic operations is analyzed, and the results indicate that the logic operations have good anti-noise performance.

KEYWORDS Vertical cavity surface emitting laser, reconfigurable, chaotic logic operations, success probability

I. INTRODUCTION

It is well known that the chaotic laser signal is not only extremely sensitive to the initial conditions of the system and external interference, but also has the characteristics of aperiodic and high randomness, which makes it widely used in the field of optical communication, such as high-speed physical random number generators, high-speed key distribution and signal carrier, etc. In recent years, optical chaotic logic operations based on semiconductor laser has attracted widespread attention since it provides a scheme to realize reconfigurable logic operation, where different logic operations such as AND, OR, XNOR, NAND, NOR, XOR, etc., are flexibly converted by the slight change of the parameters in a chaotic system. And optical chaotic logic operations are the most critical technology in future optical chaotic network secure communication, however, the technology of the optical chaotic logic operations still lags behind. For most of the logic processing of optical chaotic signals, such as multiplexing, demultiplexing, switching, regeneration, storage and calculation, it is necessary to implement all-optical chaotic logic devices and sequential logic ones with low power consumption and high speed. Compared to edge emitting laser, vertical cavity surface emitting laser (VCSEL) exhibits many advantages such as large modulation bandwidth, low threshold current, round beam output and easy coupling with fiber, etc. [1]-[4]. Under the conditions of external light injection or bias current injection, the VCSEL is easy to emit mutually orthogonal chaotic x-polarized light (x-PL) and chaotic y-polarized light (y-PL), and it can also exhibit rich dynamic behaviors such as polarization switch and polarization bistability [5]-[14]. Based on the dynamic characteristics of VCSEL’s polarization bistability, the C. Masoller’s research group successfully implemented stochastic logic gates with different technical schemes [1], [2], [15]. In 2013, Yan put forward a feasible plan to implement all-optical logic gates based on "master-slave-response" synchronization system of chaotic multiple-quantum-well lasers [16]. In 2015, Zhong’s team obtained optoelectronic composite logic gates based on electro-optic (EO) modulation theory and the VCSEL subjected to external optical injection [17].
2016, all-optical stochastic logic gates and their delay storages were successfully implemented based on generalized chaotic synchronization and polarization switch in system of the cascaded VCSELs with optical-injection [18]. In 2017, based on polarization bistability, the reconfigurable all-optical chaotic logic gates were firstly being successfully realized by the scheme for VCSEL subject the injection of light from tunable sampled grating distributed Bragg reflector laser [19]. In 2020, my research group use a simple technical scheme for the VCSEL subject the optical feedback to implement the reconfigurable optoelectronic chaotic logic gates [20]. Next year, a novel scheme for the reconfigurable optical chaotic logic operations with fast rate of picoseconds scale were proposed in our laboratory [21].

However, the most of logic operations implemented by the above schemes are static, the development of dynamic and reconfigurable chaotic logic operations are still in the initial stage. Since the VCSEL with external optical feedback or external optical injection, as a nonlinear system with high dimension has rich nonlinear dynamic behaviors, it is great prospect that reconfigurable chaotic logic operations are implemented. In this paper, we put forward a novel implementation scheme for reconfigurable and storable chaotic logic operations in a chaotic polarization system of drive-response VCSELs with optical feedback. And the half adder logic operations can also be performed based on this system. Finally, the reliability of logic operations is further analyzed.

II. THEORY AND MODEL

The composition of the drive-response system and detailed light path are displayed in Figure 1. In the drive system, the light emitted by D-VCSEL first passes through the isolator 3 (IS3), and then is separated into x-PL and y-PL by polarization beam splitter 2 (PBS2). The x-PL passes through the light intensity meter 1 (LIM1) and then is divided into two beams by beam splitter 2 (BS2). One beam of the x-PL is feedback to the periodic poled LiNbO3 (PPLN1) crystal by the plane mirror 1 (M1). M2 and M6 in the feedback cavity, and the other beam of x-PL is directly injected into the PPLN2 crystal. The y-PL from PBS2 is divided into two beams by BS5. One beam of y-PL is reflected by M3, M4, and M5 and then passes through the Faraday rotator 1 (FR1) and half wave plate 1 (HWP1), and finally injected into the PPLN1 crystal. The other beam of y-PL is directly injected into the PPLN1 crystal through FR2 and HWP2. The above FR and HWP are mainly used to convert the polarized direction of y-PL to the z-axis direction of the crystal. The x-PL and y-PL injected into the crystal are regarded as the initial input of o-light and e-light respectively. The electric fields applied to PPLN1 and PPLN2 are denoted by E1 and E2, respectively. The x-PL and y-PL from the PPLN1 crystal (e-light is converted into y-PC by FR2 and HWP2) pass through IS1 and IS2 respectively, and then are injected into PBS1 together. The light output from PBS1 is divided into two beams by BS4, and then these two beams are injected into D-VCSEL through polymer tunable diffraction grating variable attenuator 1 (VA1) and VA2, respectively. The x-PL and y-PL from the PPLN2 crystal pass through IS4 and IS5 respectively, and then are combined by PBS5 into a beam of light, which is injected into the R-VCSEL through VA3.

In order to implement dynamic switching between different logic operations, the logical control signal needs to meet the different logic operation relationships with the logic inputs synchronously. To solve this problem, we give the following technical solutions: the time-varying current source 1 (I1) and 2 (I2) output the current u1, u1′, u2 and u2′. Here, the current u1 and u2, in turn, are encoded into two electric logic inputs of the field programmable gate array (FPGA) such as i1 and i2. Because the polymer tunable diffraction grating VA is controlled by the current, the optical feedback intensity k1 and k2 are determined by u1′ and u2′ respectively (see Fig. 1). Here, the k01 and

![Image](https://example.com/image.png)
\[ k_{I2} \] are encoded into optical logic inputs \( I_1 \) and \( I_2 \), respectively. Due to \( u_i = u_i^+ \) and \( u_i = u_i^- \), the logic sets of the signals \( I_1 \) and \( I_2 \) are synchronized with those of the signals \( I_1 \) and \( I_2 \). The two logic outputs of the FPGA are defined as \( Y_1 \) and \( Y_2 \), which respectively control the \( E_1 \) and \( E_2 \).

Here, \( Y_1 = Y_2 = 0 \) is encoded in the low level \( E_0 \); \( Y_1 = Y_2 = 1 \) is encoded in the high level \( E_2 \). Namely if \( Y_1 = Y_2 = 0 \), we obtain \( E_1 = E_2 = E_0 \) and \( C_D = C_R = 1 \); when \( Y_1 = Y_2 = 1 \), we have \( E_1 = E_2 = E_0 \) and \( C_D = C_R = 1 \). Using the FPGA, \( Y_1 \) and \( Y_2 \) both can perform different logic operations with \( i_1 \) and \( i_2 \), so that \( C_D \) and \( C_R \) can implement different logic operations with \( I_1 \) and \( I_2 \) indirectly.

The D-VCSEL in the drive system is injected by the light from the PPLN\(_1\) crystal, its rate equations are derived as:

\[
\frac{dE_{D_1}(t)}{dt} = k(1+ia)[(N_{D_1}(t)-1)] \begin{pmatrix} E_{D_1}(t) \\ iN_{D_1}(t) \end{pmatrix} + k(1+ia)n_{D_1}(t) \begin{pmatrix} E_{D_1}(t) \\ iN_{D_1}(t) \end{pmatrix} 
\]

\[
T\gamma_\sigma + i\gamma_\rho \begin{pmatrix} E_{D_1}(t) \\ iN_{D_1}(t) \end{pmatrix} + k_{1D} \begin{pmatrix} E_{P_{D_1}}(t-\tau_1) \\ E_{P_{D_1}}(t-\tau_1) \end{pmatrix} \times \exp(-io_\sigma \tau) 
\]

\[
\frac{dN_{D_1}(t)}{dt} = -\gamma_\sigma [N_{D_1}(t) - \mu_{D_1} + \gamma_{D_1}(t)] E_{D_1}(t)^2 + |E_{D_1}(t)|^2 
\]

\[
+ in_{D_1}(t)(E_{D_1}(t)E^*_{D_1}(t) - E_{D_1}(t)E^*_{D_1}(t)) 
\]

Similarly, the rate equations of the R-VCSEL in the response system can be expressed as:

\[
\frac{dE_{R_1}(t)}{dt} = k(1+ia)[(N_{R_1}(t)-1)] \begin{pmatrix} E_{R_1}(t) \\ iN_{R_1}(t) \end{pmatrix} + k(1+ia)n_{R_1}(t) \begin{pmatrix} E_{R_1}(t) \\ iN_{R_1}(t) \end{pmatrix} 
\]

\[
+ \gamma_\sigma + i\gamma_\rho \begin{pmatrix} E_{R_1}(t) \\ iN_{R_1}(t) \end{pmatrix} + k_{1R} \begin{pmatrix} E_{P_{R_2}}(t-\tau_2) \\ E_{P_{R_2}}(t-\tau_2) \end{pmatrix} \times \exp(-io_\sigma \tau) 
\]

\[
\frac{dN_{R_1}(t)}{dt} = -\gamma_\sigma [N_{R_1}(t) - \mu_{R_1} + \gamma_{R_1}(t)] E_{R_1}(t)^2 + |E_{R_1}(t)|^2 
\]

\[
+ in_{R_1}(t)(E_{R_1}(t)E^*_{R_1}(t) - E_{R_1}(t)E^*_{R_1}(t)) 
\]

In the above rate equations, the subscripts \( x \), \( y \), \( D \), and \( R \) respectively mean the \( x \)-PL, \( y \)-PL, D-VCSEL and R-VCSEL; \( E \) represents the complex amplitude of light; \( N \) is the total carrier concentration; \( n \) is the difference in concentration between carriers with spin-up and carriers with spin-down; \( k_i \) represents the optical feedback intensity; \( \tau_1 \) is the round-trip time in the external cavity; \( \tau_2 \) is the propagation time of light from the PPLN\(_2\) to the R-VCSEL; \( \omega_0 \) represents the center frequency of D-VCSEL and R-VCSEL; \( \zeta_x \) and \( \zeta_y \) are a pair of gaussian white noises that are independent of each other and obey the standard normal distribution. \( E_{P_{x1}} \) and \( E_{P_{y1}} \) are the complex amplitudes of the \( x \)-PL and \( y \)-PL output from the PPLN\(_1\) crystal; similarly, \( E_{P_{x2}} \) and \( E_{P_{y2}} \) are the those of \( x \)-PL and \( y \)-PL from the PPLN\(_2\) crystal. The meanings and values of other physical parameters are presented in Table I below.
### Table I The parameters of the system

| Parameters                                | value |
|-------------------------------------------|-------|
| Line-width enhancement factor $a$         | 3     |
| Effective refractive index of active layer $n_g$ | 3.6   |
| field decay rate $k$                      | 300   |
| Polar angle $\theta/\pi$                  | 1/2   |
| Spin relaxation rate $\gamma_s$          | 50 ns$^{-1}$ |
| Azimuth $\phi$                           | 0     |
| Nonradiative carrier relaxation $\gamma_e$ | 1 ns$^{-1}$ |
| Normalized injection current $\mu_0$     | 1.5   |
| Dichroism $\gamma_d$                     | -0.1 ns$^{-1}$ |
| Refractive index of crystal $n_1$         | 2.24  |
| Crystal length $L$                       | 15 mm |
| Delay time $\tau_1$                      | 2 ns  |
| Normalized injection current $\mu_k$     | 1.5   |
| Delay time $\tau_2$                      | 4 ns  |
| Effective area of light spot $S_A$        | 38.485 um$^2$ |
| Refractive index of e-light $n_2$         | 2.17  |
| Length of the laser cavity $L_c$          | 10 um |
| Optical injection intensity $k_{ij}$      | 1.13 ns$^{-1}$ |
| Volume of the active layer $V$            | 384.85 um$^3$ |
| Central wavelength $\lambda_0$            | 1550 nm |
| Differential material gain $g$            | $2.9 \times 10^{12}$ s/m$^{-1}$ |
| Field confinement factor to the active region $\Gamma$ | 0.05 |
| The bit duration time $T$                | 10 ns |
| The noise intensity $\beta_{sp}$         | $2 \times 10^9$ |

Considering the $x$-PL and $y$-PL from D-VCSEL as the original inputs of the o-light and the e-light in PPLN$_1$ crystal, respectively, we have

$$E_{o,e}(0,t-\tau_i) = \sqrt{\frac{\hbar \alpha V}{S_A T_{l_i} n_{1,2}}} E_{in, o,e}(t-\tau_i)$$ (7)

In the same way, the amplitude of the original inputs of the o-light and e-light in PPLN$_2$ crystal satisfy

$$E_{o,e}(0,t-\tau_2) = \sqrt{\frac{\hbar \alpha V}{S_A T_{l_2} n_{1,2}}} E_{in, o,e}(t-\tau_2)$$ (8)

In the above formula, $E_o$ and $E_e$ represent the amplitude of o-light and e-light respectively; $\hbar$ is the Planck constant; $S_A$ denotes the effective area of the light spot; $V$ is volume of the active layer; $T_{l_i}$ is the round trip time in the laser cavity and $T_{l_i} = 2n_i \nu_c / c$, $L_c$ is the length of the laser cavity, $n_g$ represents the effective refractive index of active layer, $\nu_c$ is the speed of light in vacuum; $c$ is the light velocity in a vacuum, $n_1$ and $n_2$ are the undisturbed refractive indices of the o-light and the e-light, respectively. Due to the phase mismatch and the weak second-order nonlinear effect, the analytical solutions of the wave-coupling equations of the linear EO effect for the light in the PPLN$_1$ and the PPLN$_2$ are written as:

$$E_{o,e}(L,t-t_0) = \rho_{o,e}(L,t-t_0)\exp(i\beta_{L}L)\exp[i\phi_{o,e}(L,t-t_0)]$$ (9)

where $t_0 = \tau_i$ or $\tau_2$, the meanings and mathematical expressions of other physical parameters are present in Ref. [18]. When the D-VCSEL are subject to the injection of the output x-PL and y-PL from the PPLN$_1$ crystal, we have:

$$E_{p_{1,2},o,e}(t-\tau_i) = \sqrt{\frac{S_A T_{l_i} n_{1,2}}{\hbar \alpha_o V}} U_{o,e}(L,t-\tau_i)$$ (10)

Similarly, while the output x-PL and y-PL from the PPLN$_2$ crystal are injected into the R-VCSEL, we obtain

$$E_{p_{1,2},o,e}(t-\tau_2) = \sqrt{\frac{S_A T_{l_2} n_{1,2}}{\hbar \alpha_o V}} U_{o,e}(L,t-\tau_2)$$ (11)
III. RESULTS AND DISCUSSION

Here, we suppose that the optical feedback intensity equals to the sum of two square waves that encode the two logic inputs, i.e., $k_1=k_{1R}+k_{1D}$. Here, the logic input for the optical feedback intensity $k_{1R}$ is defined as $I_1$, and that for the optical feedback intensity $k_{1D}$ is defined as $I_2$. In this case, there are four logic input sets: (0, 0), (0, 1), (1, 0), and (1, 1). Representing the (0, 1) and (1, 0) with the same optical feedback intensity $k_{1R}$, we can encode the four inputs with the three-level signals $k_{1R}$, $k_{1Ri}$, and $k_{1Di}$, where $k_{1R}$ accounts for the set (0, 0), and $k_{1Di}$ represents the set (1, 1). The three-level signal used to vary $k_1$ is constant during a time interval $T$, defined as the bit duration time.

We suppose that $I_1=I_2=0$ when $k_{1R}=k_{1D}=0.56ns^{-1}$ ($k_{1Ri}=1.12ns^{-1}$); when $k_{1R}=k_{1D}=0.57ns^{-1}$, $I_1=I_2=1$ ($k_{1Ri}=1.14ns^{-1}$); $I_1=0$, $I_2=1$ if $k_{1R}=0.56ns^{-1}$ and $k_{1D}=0.57ns^{-1}$ ($k_{1Di}=1.13ns^{-1}$), similarly $k_{1R}=0.57ns^{-1}$, $k_{1D}=0.56ns^{-1}$ ($k_{1Di}=1.13ns^{-1}$) indicate that $I_1=1$, $I_2=0$. The applied electric field $E_1$ and $E_2$ in drive-response system are modulated into the logical control signal $C_{D}$ and $C_{R}$ respectively, it means that, if $E_1=E_2=E_{0i}=0.3kV/mm$, $C_{D}=C_{R}=0$; else if $E_1=E_2=E_{0i}=0.75kV/mm$, $C_{D}=C_{R}=1$. The logic output $X_1$ of the drive system is demodulated by the difference between the average value $A_{D}$ of the x-PL intensity from the D-VCSEL and the threshold $A_T$; similarly, the logic output $X_2$ of the response system is demodulated by the difference between the average value $A_{R}$ of that from the R-VCSEL and the threshold $A_T$. Namely, if $A_D-A_T>0$, $X_1=1$, else $X_1=0$; in the same way $X_2=1$ if $A_R-A_T>0$, else $X_2=0$.

The threshold value $A_T$ determines the reliability of the logic operations. In order to obtain a suitable threshold, we adopt the following technical solutions: since $C_{D}$ and $C_{R}$ can perform different logic operations with $I_1$ and $I_2$ by FPGA, such as AND, OR, XOR, etc. For different cases of logic operation $C_{D,R}$, we have calculated the maximum value $A_{Dmax}$ of $A_D$ when $C_{D}=0$, and the minimum value $A_{Dmin}$ of that under $C_{D}=1$. The maximum value $A_{Rmax}$ of $A_R$ when $C_{R}=0$, and the minimum value $A_{Rmin}$ of that under $C_{R}=1$ also have been calculated. The specific calculation results are displayed in table II. From the table, we obtain that the maximum value of $A_{Dmax}$ equals to 0.0053, and the minimum value of $A_{Dmin}$ equals to 0.016. Therefore, the threshold $A_T$ needs to satisfy the following condition: $0.0053<=A_T<=0.016$. Hence, we take $A_T$ as 0.01, that is, if $A_D<0.01$ and $A_R<0.01$, $X_1=X_2=0$; else $X_1=X_2=1$ when $A_D>0.01$ and $A_R>0.01$.

| Logic operations | $(I_1, I_2) = (0, 0)$ | $(I_1, I_2) = (0, 1)$ | $(I_1, I_2) = (1, 0)$ | $(I_1, I_2) = (1, 1)$ |
|------------------|---------------------|---------------------|---------------------|---------------------|
| $C_{D,R} = I_1 + I_2$ | $A_{Dmax}=0.051$ | $A_{Rmin}=0.003$ | $A_{Dmin}=0.0025$ | $A_{Rmax}=0.019$ |
| $C_{D,R} = I_1 \cdot I_2$ | $A_{Dmax}=0.022$ | $A_{Rmin}=0.019$ | $A_{Dmin}=0.0048$ | $A_{Rmax}=0.0024$ |
| $C_{D,R} = I_1 \oplus I_2$ | $A_{Dmax}=0.0053$ | $A_{Rmin}=0.0042$ | $A_{Dmin}=0.0034$ | $A_{Rmax}=0.018$ |
| $C_{D,R} = I_1 \ominus I_2$ | $A_{Dmax}=0.0048$ | $A_{Rmin}=0.0019$ | $A_{Dmin}=0.0005$ | $A_{Rmax}=0.0002$ |
| $C_{D,R} = I_1 \otimes I_2$ | $A_{Dmax}=0.005$ | $A_{Rmin}=0.002$ | $A_{Dmin}=0.0048$ | $A_{Rmax}=0.0031$ |

The system can realize different logic operations when the logical control signal meets different logic operation relationships with the logic inputs. In this paper, relying on FPGA to convert the logic operation relationships between the logical control signals $C_D$ ($C_R$) and $I_1$, $I_2$, the response system has the same logic outputs as the drive system when $C_R$ remains equal to $C_D$, i.e., $X_2(t) = X_1(t-\tau^\pm \tau_1)$, so as to realize the reconfigurable and storable logic operations.

Figure 2 shows the numerical simulation results of logic operations. The blue dotted line in Fig. 2(a) represents the applied electric field $E_1$ (encoded into $C_{D}$), and the red dotted line represents the three-level signals $k_{1R}$, $k_{1D}$, and $k_{1Di}$ (encoded into the logic inputs), the solid black line in Fig. 2(b) denotes the intensity $I_{Dx}$ of x-PL from the D-VCSEL, and $I_{Dx}=|E_{Dx}|^2$. The logic output $X_1$
obtained by the threshold mechanism as shown in Fig. 2(c). From Figs. 2(a), 2(b) and 2(c), it is found that when the noise intensity $\beta_{sp}$ is $2 \times 10^9$, the different logic operations at different time periods can be implemented, controlling the logic operation between $C_D$ and two logic inputs. For example, if $C_D = I_1 \cdot I_2$ when the time $t$ is between $10$ ns and $50$ ns, we obtain the logic AND operation, i.e., $X_1 = I_1 \cdot I_2$; while $t$ is between $50$ ns and $90$ ns, the logic OR operation can be performed when $C_D = I_1 + I_2$, i.e., $X_1 = I_1 + I_2$; with $t$ varying from $90$ ns to $130$ ns, $X_1 = I_1 \odot I_2$ if $C_D = I_1 \odot I_2$, the logic output is logic XNOR operation; in the case that $C_D = I_1 \cdot I_2$, the logic output is of logic NAND operation, i.e., $X_1 = I_1 \cdot I_2$, and when $130$ ns $\leq t \leq 170$ ns; If $C_D = I_1 + I_2$, it is converted into the XNOR operation, i.e., $X_1 = I_1 + I_2$. Finally, with $t$ being between $210$ ns to $250$ ns, the logic output is further converted into logic XOR operation due to the fact that $C_D = I_1 \oplus I_2$.

The logical control signals $C_D$ and $C_R$ remain equal at all times, the logic operations performed by the response system are the same as that of the drive system, as shown in Figs. 2(d), 2(e) and 2(f), indicating that the system has the ability to reconstruct and store logic operations.

Controlling the logic operation between the logical control signals and two logic inputs, the reconfigurable and storable logic operations such as XOR, AND, XNOR, OR, NAND and NOR are further implemented as shown in Fig. 3.

Depending on FPGA, we have $C_D = I_1 \cdot I_2$ and $C_R = I_1 \oplus I_2$ (see Figs. 4(a) and 4(d) ) at the same time, thus the drive system can implement the logic AND operation, i.e., $X_1 = I_1 \cdot I_2$, and the response system can realize the logic XOR operation, i.e., $X_2 = I_1 \oplus I_2$, as shown in Figs 4(b), 4(c), 4(e) and 4(f). Therefore, the half adder logic operations are also successfully implemented.

The reliability of logic operations depends strongly on some system parameters. In the following we calculate the success probability $P_1$ and $P_2$ (as the ratio between the number of correct bits to the total number of bits) to quantify the reliabilities of the logic operations performed by the drive system and the response system, respectively.

![FIGURE 2. Reconfigurable chaotic logic operations and their delayed storage.](image)

![FIGURE 3. Reconfigurable chaotic logic operations and their delayed storage](image)
Here, we take the logic operations shown in Fig. 2 as an example to calculate the evolutions of $P_1$ and $P_2$ in the space of noise intensity $\beta_{sp}$ and bit duration $T$, as shown in Fig 5. It is found that the area of $P_1$<0.8 in Fig. 5(a) accounts for a larger proportion when $T$ varies from 0ns to 1ns, indicating that the reliability of logic operations is poor; As $T$ gradually increases from 1ns to 2ns, the area with $P_1$>0.9 accounts for a larger proportion, denoting that the reliability of logic operations is enhanced; when $T$ continues to increase from 2ns to 10ns, the proportion of the area with $P_1$=1 increases rapidly. It can also be seen that as the noise intensity $\beta_{sp}$ increases from 0 to $4\times 10^9$, the proportion of area with $P_1$=1 is gradually shrinking, showing that reliability is slowly getting worse. The evolution trajectory of $P_2$ in Fig. 5(b) is similar to that of $P_1$ in Fig. 5(a).

In order to show the local changes of $P_1$ and $P_2$ in Fig. 5 in more detail, we further analyze the dependence of the success probability on the $\beta_{sp}$ for different $T$, as displayed in Fig. 6. As we can see from the Fig. 6(a) that if $T$=4ns, the value of $P_1$ is always equal to 1 when $0<\beta_{sp}<1\times 10^9$, which indicates that the reliability of the logic operations is strong, and no error appeared in logic outputs; as $\beta_{sp}$ exceeds $1\times 10^9$, the value of $P_1$ begins to fluctuate, but is still above 0.9. When $0<\beta_{sp}<3.75\times 10^9$, the $P_1$ is always equal to 1 if $T=8$ns, denoting that the logic operations are of reliability and stability; $P_1$ varies in a small range when $\beta_{sp}$ exceeds $3.75\times 10^9$, the reliability of the logic operations gets slightly worse. When $\beta_{sp}$ varies from 0 to $4\times 10^9$, the logic operations are so reliable that $P_1$ is always equal to 1 if $T=10$ns. From Fig. 6(b), one sees that value of $P_2$ oscillates severely with $\beta_{sp}$ increasing if $T=4$ns. When $\beta_{sp}$ increases from 0 to $2.7\times 10^6$, the value of $P_2$ always equals to 1 since $T=8$ns; with $\beta_{sp}$ further increasing from $2.7\times 10^6$ to $4\times 10^9$, $P_2$ begin to fluctuate. The $\beta_{sp}$ within the range of $4\times 10^9$ will not cause errors to the logic outputs due to the $P_2$ is always equal to 1 when $T=10$ns.

From the above results, it is concluded that the success probability $P_1$ and $P_2$ for logic operations implemented by the drive system and response system respectively are seriously dependent on the noise intensity $\beta_{sp}$ and bit duration time $T$. The values of $P_1$ and $P_2$ will become small and unstable if the value of $T$ is too small or the value of $\beta_{sp}$ is too large. It is noted that the logic operations are highly reliable that both $P_1$ and $P_2$ are always equal to 1 under appropriate conditions such as $T=8$ns and $\beta_{sp}<2.7\times 10^6$, or $T=10$ns and $\beta_{sp}$ within the $4\times 10^9$. 
VI. CONCLUSIONS

We propose a novel reconfigurable and storable chaotic logic operations scheme by using the drive-response VCSELs with optical feedback, based on the EO modulation theory. Here, the optical feedback intensity is modulated into logic input, the applied electric field in drive system and response system are modulated into logical control signals, and logic outputs are demodulated by the threshold mechanism. Relying on FPGA to convert the logic operation relationships between the logical control signals and logic input, the system can perform the reconfigurable and storable processing of logic operations. Furthermore, the system can also implement the halfadder logic operations when the chaotic logic AND and XOR operations are performed by the drive system and the response system, respectively. It is noted that the bit duration time and noise intensity have an impact on success probability of logic operations. And the reliability of logic operations are so strong that the success probability can be always equal to 1 even though the noise intensity is as high as $4 \times 10^5$, indicating that the logic operations have good anti-noise performance. These results have potential application in the reconfigurable and storable chaotic logic computing system with high speed, security and low power cost.

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