A 12-bit 100-MS/s 83 dB SFDR SAR ADC with sampling switch linearity enhanced technique

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Abstract A 12-bit 100-MS/s 83 dB SFDR SAR ADC with sampling switch linearity enhanced technique is proposed. With the variation of input signals, the parasitic capacitance variation of sampling switch is reduced and the total parasitic capacitance is also depressed. Moreover, with substrate boost technique, the on-impedance of sampling switch would decrease. To demonstrate the proposed technique, a design of 12-bit 100-MS/s SAR ADC is fabricated in 40-nm CMOS technology, consuming 2 mW from 1 V power supply with a SNDR >65 dB and SFDR >83 dB. The proposed ADC core occupies an active area of 0.02 mm², and the corresponding FoM is 13.8 fJ

Keywords: analog-to-digital converter (ADC), linearity enhanced sampling switch, successive-approximation-register (SAR) ADC

Classification: Integrated circuits

1. Introduction

In recent years, with the improvement of CMOS technology, successive approximation register (SAR) analog-to-digital converters ADCs have been able to achieve sampling rates of several hundreds of MS/s with high power efficiency and small area [1, 2, 3, 4, 5, 6, 7, 8, 9, 10]. Meanwhile, 8 to 12-bit SAR ADCs could reach sampling rates of hundreds or thousands MS/s and provide compact area and outstanding power efficiency [11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22]. Based on high performance SAR ADC, time-interleaved SAR ADCs (TI SAR ADC) are superior in aspects of highly scalable and power efficiency to advanced CMOS technology. Several calibration techniques are provided in [23, 24, 25, 26, 27, 28] to correct the non-ideal errors produced by channel mismatches in time-interleaved SAR ADC. For every type of SAR ADCs, linearity of sampling switch is the bottleneck for system linearity, the parasitic diodes of source/drain to substrate exist in the sampling switch. The equivalent capacitance of the parasitic diodes will change with input signal, it indicates the voltage coefficient of sampling net of SAR ADC is not a constant and linearity of the sampling switch is restricted. Especially, in high speed implementations, large size of sampling switch is required to obtain small on-impedance. In order to achieve a high Spurious-Free-Dynamic-Range (SFDR), high linearity sampling switch is demanded in the design of high-speed SAR ADCs. A buffered bootstrapping technique is provided in [29] to reduce signal-dependent charge injection in the design of sampling switch. A high linearity technique is introduced in [30] to reduce the parasitic capacitance of sampling switch. But three auxiliary switches are needed and more parasitic capacitances are imported. A linearity-improved sampling switch with parasitic capacitance compensation technique is exhibited in [31] without the triple-well process, the change of parasitic capacitance is reduced, but the total parasitic capacitance will increase after compensation and the sampling speed is restrained. This Letter proposes a substrate floating technique for high linearity sampling switch of SAR ADC, the change of parasitic capacitance and total parasitic capacitance of sampling switch are both reduced. Further, lower on-impedance of sampling switch is introduced with substrate boost technique. Lastly, only one auxiliary switch is used to simplify the structure and unnecessary parasitic capacitance is depressed.

2. Design implementation

2.1 System architecture

The 12-bit SAR ADC and time sequence are presented in Fig. 1. With 12b resolution or less for SAR ADCs, the mismatch of capacitor could be satisfied with capacitance of several femto Faradays by using MOM capacitor. In order to achieve high linearity, the Vp-p of input signal is set to 0.8 V. For 1.5 fF unit capacitor, the kT/C noise is about 0.04 mVrms, the equivalent input-referred noise of the dynamic comparator should smaller than 0.24 mVrms. Because of serial conversion pattern, the sampling time of high speed SAR ADC is reduced (~500 ps in this design) compared with pipeline and flash ADCs, the size of sampling switch is increased to reduce the on-resistance. However, the linearity of SAR ADC is influenced by large sampling switch, which has parasitic diodes from source/drain to substrate.

2.2 Circuits implementation

Fig. 2(a) exhibits the schematic of a conventional NMOS sampling switch. Fig. 2(b) illustrates the cross-section of a conventional NMOS sampling switch in triple-well proc-
ess, P-SUB is the substrate of wafer, DNW is deep-nwell, PW is isolated substrate of NMOS sampling switch, NW is nwell, P⁺ and N⁺ are the P and N injection regions, respectively. As shown in Fig. 2(b), both of D1 and D2 work in reverse bias region when the sampling switch is on. That means the reverse bias diodes D1 and D2 could be deemed as two variable barrier capacitors C1 and C2. The simplified expression of C1 and C2 with abrupt junction approximation is

\[
C_{1,2} = A \left( \frac{\varepsilon q N_A}{2V_{\text{in}}} \right)^{1/2}
\]

where \( A \) is the area of PN+ junction, \( q \) is the unit charge quantity, \( \varepsilon_s \) is the dielectric constant of material, \( N_A \) is doping concentration of N+ region and \( V_{\text{in}} \) is the input signal, \( V_{\text{in}} \) is also the reverse bias of D1 and D2. It can be concluded from equation (1) that the value of \( C_{1,2} \) changes with the change of \( V_{\text{in}} \), the SFDR of SAR ADC will deteriorate with the parasitic capacitance variation of sampling switch.

Fig. 3(a) illustrates the schematic of proposed sampling switch, auxiliary switch K connects the PW of sampling switch M and GND. To obtain smaller on-resistance of sampling switch, the substrate voltage of sampling switch is boosted in sample phase. When sampling switch is off, K is turned on and the substrate of sampling switch (PW) is pulled to 0. When the sampling switch is on, K is turned off, the PW is floating and coupled by Cc. Because the value of Cc is very small (\( \sim 5 \text{ fF} \)), we do not use capacitor model in the PDK (MOM capacitor). In this design, Cc is designed by the parasitic capacitance of metal3-metal5, thus, the value of Cc is adjusted flexible to match with the real condition, such as the real parasitic capacitance and the substrate voltage of sampling switch. Therefore, the threshold voltage of sampling switch is increased and the on-resistance is reduced. In order to reduce the leakage of PW, the boosting of PW is moderate (0.3 V\( \sim \)0.4 V), Cc and the parasitic capacitance of K are much smaller than the parasitic capacitance of sampling switch M. Fig. 3(b) illustrates the cross-section of proposed sampling switch. We take the parasitic capacitance change of C1 (PN+ diode) and C3 (PN diode) as an example, the relationship of C2 and C4 is similar to C1 and C3. Firstly, the variable parasitic capacitance of C1 and C3 are in series, if we ignore Cc, the total parasitic capacitance of sampling switch is \( C_1 \parallel C_3 \), the parasitic capacitance is reduced by the series connection. Secondly, the PW voltage \( V_P \) will change with input signal \( V_{\text{in}} \), because of the partial voltage effect of C1 and C3, the change of \( V_P \) is decided by \( V_{\text{in}} \) and the values of C1 and C3.

With small-signal equivalent, from kirchhoff’s current law at point P, we could get

\[
(\Delta V_{\text{in}} - \Delta V_P) \cdot C_1 \cdot s = \Delta V_P \cdot C_3 \cdot s
\]

We set \( C_3 \) equals to 3\( C_1 \), \( \Delta V_P = 0.25V_{\text{in}} \) can be obtained: From equation (1), based on the mode in MATLAB, the maximal variation of \( C_1 \) and \( C_3 \) is \(-34\%\) and \(10\%\) as \( V_{\text{in}} \) changes from 0.1 V to 1.1 V. Because C1 and C3 are in series, the total parasitic capacitance is obviously depressed. In addition, the unbalance change of C1 and C3 is evidently reduced. Moreover, the bias variation of C1 and C3 are in contrary, thereby, the parasitic capacitance variation of sampling switch is extraordinary small. Because of the series relationship of C1 and C3, the variation of parasitic capacitance is halved compared to \([29]\). The change of parasitic capacitance in the proposed structure is a half
compared with [29]. In structure [30], three auxiliary switches are used and unnecessary parasitic capacitance of sampling switch will increase obviously. The total parasitic capacitance is also depressed compared with [31], in which, the parasitic capacitance and compensation capacitance are in parallel. Consequently, the equivalent parasitic capacitance of the proposed switch is reduced obviously. Further, with substrate boost technique, the voltage of PW could be boosted by Cc in sampling phase. That means the threshold voltage of sampling switch is reduced and the on-impedance of sampling switch will decrease. A small Cc is used to bias the PW instead of additional switches in [30] and [31], low on-impedance is achieved with small parasitic capacitance in the proposed structure.

2.3 Performance of comparisons

To demonstrate the proposed linearity-enhanced switch technique, we design the four sampling switches with the same size in 40 nm CMOS technology. The parasitic capacitance of sampling switches in 40-nm CMOS process are imported to MATLAB. Simulation results of the relationship between total source/drain to substrate parasitic capacitance (CB) of sampling switch and Vin in [29, 30, 31] and the proposed technique are exhibited in Fig. 4. As input signal changes from 0.1 V to 1.1 V, the change of parasitic capacitance in [29] and [31] are higher 33%, and 11%, respectively. The change of parasitic capacitance is small in [30], however, with three auxiliary switches, the total parasitic capacitance is increased. Because of the substrate floating technique, the change of parasitic capacitance in the proposed sampling switch is only 3.7%. In addition, the total average parasitic capacitance of [31] is higher than 48 fF, the total average parasitic capacitance of [29] and [30] are about 30 fF, and 25 fF, respectively. Considering the parasitic capacitance of switch K and Cc, the total parasitic capacitance of the proposed sampling switch is smaller than 12 fF, which is only 40% and 46% compared with [29] and [30], the value is 25% compared with [31]. That means the proposed sampling switch could provide higher linearity compared with previous structures. The threshold voltage variation of sampling switch is smaller than 10 mV, which is small for 12-b ADC.

The four sampling switches are simulated with 12-bit 100 MS/s ADC systems in 40-nm CMOS technology, with sampling time of 500 ps and sampling capacitance of 3 pF, the SFDR of sampling switches comparison versus input frequency is exhibited in Fig. 5. The SFDR average improvement of proposed structure is about 8 dB compared with [29], the corresponding values are 5.2 dB and 7.3 dB compared with [30] and [31]. In the condition of PVT variation, as the input frequency changes from DC to 50 MHz, the least SFDR improvement of proposed structure is about 5 dB compared with [29, 30, 31]. As the peak to peak voltage (Vp-p) changes from 0.6 V to 1.2 V, the SFDR comparison versus input Vp-p is shown in Fig. 6. Because of tiny variation of the parasitic capacitance and small total parasitic capacitance, the deterioration of SFDR is only 6 dB. However, the deterioration of [29] is 13 dB, the corresponding values are 9.5 dB and 8.7 dB in [30] and [31], respectively. Especially, as the increasing of Vp-p, the advantage of proposed linearity technique becomes more evident compared with previous techniques. As the input Vp-p increases to 1.2 V, the least SFDR improvement of proposed structure is higher than 5 dB compared with [29, 30, 31].

3. Measurement results and discussions

The proposed SAR ADC is designed in 1P10M 40-nm CMOS technology. The die micrograph of proposed SAR ADC is shown in Fig. 7. The core area is 0.14 μm x 0.14 μm. The measurements of differential nonlinearity (DNL) and integral nonlinearity (INL) of the proposed ADC are shown in Fig. 8. The peak DNL and INL are −0.85/+0.46 LSB and −1.2/+1.3 LSB. The measurement results with 10 MHz input without and with proposed linearity enhanced technique are shown in Fig. 9(a) and Fig. 5. SFDR of sampling switches versus input frequency.

Fig. 5. SFDR of sampling switches versus input frequency.

Fig. 6. SFDR comparison versus input Vp-p.
Fig. 7. The die micrograph of proposed SAR ADC.

Fig. 8. Measured DNL and INL.

Fig. 9. Measurement output spectrums with 10MHz input without proposed linearity enhanced technique (a) and with the proposed linearity enhanced technique (b) with sampling rate 100MHz.

78 dB, which is limited by the total value and voltage coefficient of parasitic capacitance. With the proposed linearity enhanced technique, the SFDR is improved from 78 dB to 85 dB. The total power consumption is about 2 mW at 1 V power supply with operating frequency is 100 MHz. The measurement results with 49 MHz input with proposed linearity enhanced technique are shown in Fig. 10, the SFDR and SNDR are 83 dB and 65 dB, respectively.

TABLE I. The performance comparisons

| Reference     | [6] | [9] | [10] | This work |
|---------------|-----|-----|------|-----------|
| Technology    | 40  | 40  | 40   | 40        |
| Resolution    | 12  | 12  | 12   | 12        |
| Supply (V)    | 0.9 | 1.1 | 0.9  | 1         |
| Sampling rate | 100 | 160 | 150  | 100       |
| SNDR (dB)     | 67.3| 65.3| 56.2 | 65        |
| SFDR (dB)     | 81.8| 86.9| 63.5 | 83        |
| Power (mW)    | 2.6 | 4.96| 1.5  | 2         |
| FoM (fJ/conv) | 14.6| 20.6| 18.9 | 13.8      |
| Area (mm²)    | 0.014| 0.042| 0.04 | 0.02      |

The performance comparison with other related 12b 100 MS/s to 160 MS/s SAR ADCs is listed in Table I. With the sampling switch linearity enhanced technique, the proposed 12-bit SAR ADC achieves SFDR of 83 dB and a figure-of-merit of 13.8 fJ/conversion step with Nyquist frequency.

4. Conclusions

A linearity enhanced sampling switch technique for SAR ADC is proposed. Firstly, a substrate floating technique is provided, with the change of input signal Vin, the change and the total value of parasitic capacitance are both depressed obviously. Secondly, a substrate boost technique of sampling switch is exhibited to decrease the on-impedance of sampling switch with minimum additional parasitic capacitance. Lastly, a 12-bit 100 MS/s SAR ADC is designed in 40-nm CMOS technology to demonstrate the proposed technique. The proposed SAR ADC gives a
>65 dB SNDR and achieves SFDR >83 dB with Nyquist rate. The proposed sampling switch provides better linearity compared with previous sampling structures.

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