Design of 4-Channel Photoelectric Transceiver System-in-Package for Next Generation Radar Applications

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Abstract. This paper introduces a four-channel photoelectric transceiver system-in-package. It has four-channel digital photoelectric transceiver, analog IF transceiver and signal processing functions. It integrates four-channel optical module, four-channel parallel ADC, four-channel synchronous DDS, static random access memory, two Flash memories, crystal oscillator and NTC thermistor. Structurally, the ceramic integrated shell is used for high density integration, and its volume is less than 40 mm x 40 mm x 6 mm. The test results show that the bit error rate is $6.36E^{-13}$ at 6.25Gbps data rate, and the eye diagram is normal.

1. Introduction
Digital radar receiver, usually referred to as digital receiver, is a rapidly developing radar receiver technology in recent decades. Because of the rapid development of microwave integrated circuits, high-speed and ultra-high-speed digital circuits, the development of digital radar receivers is very fast. Especially with the rapid development of high-speed and high-precision fast A/D converter and the high speed of DDS up to 1 GHz and digital signal processing technology, the hardware foundation of digital radar receiver is provided. With the development of high-speed digital signal processing technology and microwave technology, the key development direction of phased array radar is bound to be digital array radar [1][2].

The improvement of microsystem technology makes it possible for the development of digital array radar in the future. With the rapid development of multi-functional integrated chips, new semiconductor devices, advanced integration, packaging technology, efficient switching circuits and new materials in recent years, digital array radar will make great breakthroughs in function, cost and system in the future. Based on the development of Microsystem technology, digital array radar is developing towards multi-function and ideal array. The characteristics of ideal array can be considered from integration mode, system architecture, beamforming, receiving channel and transmitting channel. For beamforming, it can generate multiple non-interference receiving beams, the beam pointing can change rapidly, the beam shape can also change maneuverably according to the different working modes, and the amplitude and phase control is accurate, the sideband can be suppressed, and the speed can be synchronized. For construction, the ideal array is easy to reconstruct, update and upgrade, and it has excellent performance by relying on broadband high efficiency circuits [3]. Embedded heat dissipation management makes the system smaller in size and lighter in weight. Selecting new devices and materials makes the cost of the system lower. The transmitting channel of ideal array has the
characteristics of high PAE, wide bandwidth and high power. The improvement of the efficiency and power density of broadband devices will help to detect stealth targets, and increase the operating distance and peak power. The receiving channel of ideal array has the characteristics of low power consumption, low noise figure and large dynamic range. This design describes the optoelectronic transceiver processing module in the ideal array. The article is arranged as follows: the second part introduces the overall architecture design; the third part introduces the circuit design; the fourth part introduces the structure design of the microsystem; the fifth part introduces the verification situation; and the sixth part is the summary [4].

2. System Architecture Design
This design is a general module of digital radar optoelectronic transceiver standard. It has four channels of digital optoelectronic transceiver, analog IF transceiver and signal processing functions. It integrates four channels of optical module, four channels of parallel ADC, four channels of synchronous DDS, static random access memory, two Flash memory, crystal oscillator and NTC thermistor. Its system structure is shown in Fig. 1, as shown in the thick wire frame.

![Figure 1 Digital Radar System Framework](image)

As shown in the framework of radar system in Fig. 1, the design can complete analog-to-digital conversion of 400 MHz to 650 MHz of 4-channel RF TR unit and 50 MHz bandwidth of analog IF, and complete IF data processing through FPGA. The 4-channel optical transceiver unit (the highest transceiver rate is 6.25 Gbps) is connected to the radar data processing and control center through optical fibers to complete data transceiver, monitoring, clock management and other signal control in the radar system link.

3. Circuit Design

3.1 FPGA
In Fig. 2, the BNAK of each device is initially allocated. In the FPGA K7, the number of pins of HR BANK (12-18) is 50, the IO level range is 1.14-3.465V, the number of pins of HP BANK (32-35) is 50, and the IO level range is 1.14-1.89V. The communication rate between each chip and the FPGA in the system is 100 Mbps, and the speed level of K7 fully meets the design requirements. GTX BANK (115-118) is a group of transceivers. Each group of transceivers contains four pairs of transceivers and two pairs of clocks. Serial transceivers are used in the system for two sending and one receiving. Therefore, only BANK117 is used in the schematic diagram, and BANK118 can meet the requirements. In addition, two 12 bit, 1 Msps sampled ADCs and on-chip sensors (built-in temperature sensors and power sensors) are integrated in the K7 chip, which can real-time monitor the key information such as the voltage and core temperature of the chip. At the same time, 12 serial sampling
channels can be extended to sample the temperature of NTC temperature measurement unit inside the module and the voltage, current and temperature of external power supply. Summarizing all the information and building the module prediction and health management model in the FPGA to predict the performance deterioration of the chip, and eliminate the system failure as soon as possible.

Figure 2. Circuit schematic diagram of 4-channel digital photoelectric transceiver and processing module

3.2 ADC
For ADC, VREF, RBIAS, SENSE and VCM are added on the basis of system IO to facilitate the flexibility of testing and configuration. They mainly provide external voltage reference input/output, bias resistance, mode selection and common-mode level interface.

3.3 DDS
For DDS, in order to facilitate the flexibility of testing and configuration, SYNC_SMP_ERR, SYNC_CLK, IO_UPDATE, SYNC_IN* (Internal Link FPGA), SYNC_OUT*, DAC_RESET, REF are added on the basis of system IO. They are mainly used for multi-chip synchronization of DDS, channel reference resistance setting, channel reference configuration, etc.

3.4 Optical Module
In the optical transmitting part, four parallel high-speed digital differential signals are input into the laser driver chip through the high-speed serial interface pin of the FPGA, and the driver chip drives four laser array light emitting devices, which are converted into four parallel digital optical signals which are transmitted into the optical fiber through the optical fiber coupling components; in the optical receiving part, four parallel high-speed digital optical signals are transmitted to four channels through the optical fiber coupling components. The detector array is converted to 4-channel electrical signal, which is amplified and shaped by driver chip, and the 4-channel parallel digital differential electrical signal is output to the high-speed serial receiving pin of the FPGA. The control circuit manages and controls the working state of the optical emission and optical reception.
3.5 Other
In the definition of IO, ADC channel 1-12 is an integrated 1MSPS sampling 12bit ADC in the FPGA. It is mainly used for module health management, sampling voltage, current and temperature signals in the optical transceiver module and power module.

4. Structural Design
The product is a highly integrated modular product. The high-temperature co-fired ceramic integrated needle grid array shell technology is used for high-density integration. The main body has a double-sided multi-cavity structure. The structure diagram is shown in the figure 3.

Figure 3 Structure Design

The above structure has been repeatedly verified, taking into account the design performance requirements, the processing capacity of ceramic substrate factory and the processing capacity of packaging plant, while meeting the thermal and mechanical requirements.

This design integrates analog, digital, high-speed photoelectric transceiver and other chips, which are operating in a complex electromagnetic environment, in high-density integrated design, how to achieve digital and analog isolation, to ensure their respective ground as complete as possible; for analog part of the radio frequency signal, how to strengthen the isolation between radio frequency signal and other signals, how to increase between signals California floor and ground crossing holes improve signal isolation, and propose what kind of requirements to ensure impedance matching of RF signal lines by shell manufacturers. It requires a detailed analysis of the system signal integrity at the beginning of the design to achieve impedance matching of high-speed signals and ensure signal insertion loss and crosstalk in a controllable range. In addition, this product is a multi-power domain system. How to effectively control the impedance, DC voltage drop and current density of the power plane to ensure the normal operation of the system, which also requires detailed analysis of the power integrity of the system at the beginning of the design. Finally, the integrated devices of the system, such as FPGA and DDS, consume a lot of power, so we should consider the way of heat dissipation in the early layout. We need to complete the thermal simulation of device level, board level and system level according to the thermal simulation, guide the module layout design in the early stage, and apply the board level and system level heat dissipation design.

Single-core optical fiber gas sealing technology is relatively mature at present, but 12-core optical fiber gas sealing technology is very difficult, for the optical fiber through-cavity sealing is the weak link of the whole product to achieve air tightness. For single-core and 12-core optical fibers, the existing mature technology is to metallize the optical fibers, melt tin through the Kovar optical fibers sealing pipe, and then weld the Kovar optical fibers sealing pipe and the sealing ring of the shell to achieve air-tightness. Metallization and welding seals of 12-core optical fibers are technical difficulties. In the process of metallization, the coating should be uniform, compact and able to withstand a certain degree of bending. In molten tin, the temperature operation of solder is very important. The temperature is too high to damage the optical fiber, and the temperature is too low. The melting of solder is not uniform, which can not achieve the effect of gas tightness.
5. Test Result
Fig. 4 is the test result of this design. It can be seen that at the rate of 6.25 Gbps, the eye opening is normal and the bit error rate is about $6.36 \times 10^{-13}$.

![Eye Diagram](image)

Figure 4. 6.25 Gbps Digital Optical Transceiver and Processing System Test Eye Diagram

6. Summary
The combination of micro-system technology and digital radar technology provides a new opportunity for the development of digital array radar. The combination of the two makes the next generation radar greatly improve the previous generation technology in terms of volume, power consumption, reliability and cost, so it becomes the research hotspot of the next generation radar technology. This design realizes the high integration of digital radar photoelectric transceiver system, which is of great significance for the rational alignment application of the next generation radar.

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