Comparative Study of Negative Capacitance Field-Effect Transistors with Different MOS Capacitances

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Abstract
We demonstrate the negative capacitance (NC) effect of HfZrO x-based field-effect transistors (FETs) in the experiments. Improved $I_{DS}$, SS, and $G_m$ of NCFET have been achieved in comparison with control metal oxide semiconductor (MOS) FET. In this experiment, the bottom MIS transistors with different passivation time are equivalent to the NC devices with different MOS capacitances. Meanwhile, the electrical properties of NCFET with 40 min passivation are superior to that of NCFET with 60 min passivation owing to the good matching between $C_{FE}$ and $C_{MOS}$. Although SS of sub-60 mV/decade is not achieved, the non-hysteretic transfer characteristics beneficial to the logic applications are obtained.

Keywords: Germanium, Negative capacitance, Passivation time

Introduction
With the scaling down of transistor, the integration level of integrated circuit (IC) is continuous growing. An accompanying power dissipation problem is urgent to be solved. In order to circumvent this problem, the operation voltage of the transistor should be reduced [1]. The subthreshold swing (SS) of MOSFET cannot be below 60 mV/decade at room temperature, which restricts the reduction of threshold voltage $V_{TH}$ and supply voltage $V_{DD}$ [2]. Many efforts have been devoted to the research and the development of devices with novel transport and switching mechanisms to beat the Boltzmann limit, including negative capacitance field-effect transistor (NCEFT) [3, 4], resistive gate FET [5], nano-electro mechanical FET (NEMFET) [6, 7], impact ionization metal-oxide-semiconductor (I-MOS) [8, 9], and tunneling FET [10, 11]. Among them, NCFET has aroused much attention because it can achieve a steep SS without losing the drive current [12–15]. Doped HfO$_2$ (e.g., HfZrO$_x$ (HZO) and HfSiO$_x$) has been widely used in NCFETs [4, 16, 17]; it is compatible with the CMOS process [18]. A theoretical study has shown that the undesired hysteresis occurs due to unmatched ferroelectric capacitance $C_{FE}$ to underlying MOS capacitance $C_{MOS}$ in NCFET [19]. However, the effect of matching between $C_{FE}$ and $C_{MOS}$ on the electrical characteristics of NCFETs is still a concern in the experiments.

In this work, the electrical characteristics of NC Ge FETs with different MOS capacitances are studied based on the different matching between $C_{FE}$ and $C_{MOS}$. Although SS less than 60 mV/decade does not appear, the hysteresis-free transfer characteristics and better electrical properties are obtained. Apparent peaks of $C_{FE}$ versus $V_{FE}$ curves demonstrate NC effect of HZO based NCFETs. The better matching of $C_{FE}$ and $C_{MOS}$ contributes to steeper SS and higher on current, which is beneficial to the logic applications.

Methods
The key fabrication process of Ge NCFETs is shown in Fig. 1a. Four-inch n-Ge(001) wafers with a resistivity of 0.088–0.14 Ω·cm were used as the starting substrates. After pre-gate cleaning, Ge wafers were loaded into an ultra-high vacuum chamber for surface passivation using Si$_2$H$_6$. Two passivation durations of 40 and 60 min were used. Then, TaN/HZO/TaN/HfO$_2$ stack was deposited. The thicknesses of the HfO$_2$ dielectric layer and HZO...
FE layer are 4.35 and 4.5 nm, respectively. After gate patterning and etching, source/drain (S/D) regions were implanted using boron ions (B⁺) at an energy of 30 keV and a dose of $1 \times 10^{15}$ cm⁻². S/D metal Nickel was formed using a lift-off process. Finally, rapid thermal annealing at 450 °C for 30 s was carried out. Control MOSFET with TaN/HfO₂ stack was also fabricated. Figures 1b and c show the schematics of fabricated NCFET and control MOSFET, respectively. The internal metal gate in the fabricated NCFET counterbalances the potential at the channel surface, which is called the MFMIS structure.

**Results and Discussion**

Figure 2a plots the measured $I_{DS}$-$V_{GS}$ curves of a pair of NCFET and control MOSFET with 40 min surface passivation. Both devices have a gate length $L_G$ of 3.5 μm. The NC device with 40 min passivation has a significantly improved $I_{DS}$ than the control MOSFET. The transfer curves of NCFET exhibit a non-hysteretic feature. Point SS versus $I_{DS}$ curves in Fig. 2b show that the NC transistor has improved SS over the control device, although SS of sub-60 mV/decade does not appear. Figure 2c shows that NC transistor obtains a significantly boosted linear transconductance $G_m$ over the control device at $V_{DS}$ of −0.05 V. Figure 3 compares the electrical performances of NCFET and control MOSFET with surface passivation for 60 min. Similarly, the $I_{DS}$, point SS and $G_m$ of NCFET are superior to that of control MOSFET.

Figure 4a shows the statistical results of the drive current of NCFETs and control MOSFETs at $V_{DS}$ of −0.05 V and $V_{GS}$-$V_{TH} = −1.0$ V. NCFETs demonstrate 18.7% and 35.6% improvement in $I_{DS}$ for the 60 min and 40 min surface passivation, respectively, in comparison with the control devices. It is speculated that the
NCFETs passivated for 40 min have a better matching between $C_{\text{MOS}}$ and $C_{\text{FE}}$ over the NC devices with 60 min. Figure 4b shows that NCFETs obtain 26.4% and 51.3% improvement in maximum transconductance $G_{\text{m,max}}$ for 60 min and 40 min surface passivation, respectively, in comparison with the control devices. It is seen that the control MOSFETs with surface passivation for 40 min have a higher $I_{DS}$ and $G_{\text{m,max}}$ than the devices passivated for 60 min, which is due to the larger $C_{\text{MOS}}$ induced by the smaller equivalent oxide thickness ($EOT$). The internal metal gate provides an equipotential plane; the device can be equivalently modeled as a capacitive voltage divider. The total capacitance $C_{\text{G}}$ is a series of $C_{\text{FE}}$ and $C_{\text{MOS}}$. The internal gate voltage is amplified owing to the NC effect. The internal voltage amplification coefficient $\beta = |C_{\text{FE}}| / |C_{\text{FE}} - C_{\text{MOS}}|$ gets the maximum when $|C_{\text{MOS}}| = |C_{\text{FE}}|$ [20, 21]. Achieving the optimized matching of $C_{\text{FE}}$ and $C_{\text{MOS}}$ is the prerequisite of the improvement of on current.

The extracted $V_{\text{int}}$ versus gate voltage $V_{\text{GS}}$ curves are shown in Fig. 5a. $V_{\text{int}}$ of NC transistor can be extracted on account of the hypothesis that $I_{DS}-V_{\text{int}}$ curve of NC transistor is exactly identical with $I_{DS}-V_{\text{GS}}$ curve of the control device. The internal voltage amplification coefficient $dV_{\text{int}}/dV_{\text{GS}}$ is shown in Fig. 5b. $dV_{\text{int}}/dV_{\text{GS}} > 1$ is achieved in the wide sweeping range of $V_{\text{GS}}$ for the NCFET with 40 min surface passivation, contributing to a steeper SS than the control device during the measuring process.
which is due to the local polarization switching [22]. It is consistent with the aforementioned results in Fig. 2b. For the NCFET with 60 min passivation, the internal voltage amplification coefficient \( \frac{dV_{\text{int}}}{dV_{\text{GS}}} > 1 \) is achieved during the range of \( V_{\text{GS}} < 0 \) V for the double sweeping of \( V_{\text{GS}} \), which is in agreement with the elevated SS in Fig. 3b.

Figure 6a shows the extracted \( C_{\text{MOS}} \) versus \( V_{\text{GS}} \) curves for NC transistor, which is relying on the \( V_{\text{int}}-V_{\text{GS}} \) in Fig. 5a and the \( C_{\text{G}}-V_{\text{GS}} \) curves of control MOSFETs. The extracted \( C_{\text{MOS}} \) is in good agreement with the measured \( C_{\text{G}} \). Hence, the validity of the calculation method is demonstrated. The \( C_{\text{FE}} \) and \( C_{\text{MOS}} \) versus \( V_{\text{FE}} \) curves are depicted in Fig. 6b. From the initiation of NC effect, the absolute value of negative \( C_{\text{FE}} \) of the transistor exceeds \( C_{\text{MOS}} \) for double sweeping of \( V_{\text{GS}} \) all the time in Fig. 6b. \( |C_{\text{FE}}| > C_{\text{MOS}} \) and \( C_{\text{FE}} < 0 \) can cause hysteresis-free characteristics, and the matching of \( C_{\text{MOS}} \) and \( C_{\text{FE}} \) is beneficial to the logic applications [23, 24]. Hysteresis-free characteristics in Figs. 2a and 3a are observed attributed to all the domain matching and inhibited charge trapping [25]. The
stable polarization switching is responsible for the non-hysteretic characteristics [26]. Furthermore, the large internal gate gain \( \frac{dV_{int}}{dV_G} > 1 \) is ascribed to the slight discrepancy between \( C_{FE} \) and \( C_{MOS} \) in the subthreshold region, resulting in the steep SS of NC device. Meanwhile, there is a better matching between \( C_{FE} \) and \( C_{MOS} \) for the NCFET with 40 min passivation than the NCFET with 60 min passivation. Thus, this provides direct evidence to indicate that the NCFET with 40 min passivation possesses a better electrical performance than the NCFET with 60 min passivation. The FE polarization changes the \( V_{FE} \); hence the charge of FE varies. The total charge multiplies, which is attributed to the FE polarization besides the increment of \( V_{GS} \). In other words, for the given \( V_{GS} \), the charge in the channel increases so the \( I_{DS} \) improves. As a consequence, the steep SS of transfer characteristic appears in the experiments.

**Conclusions**

The hysteresis-free transfer characteristics are obtained for the NCFETs with 40 and 60 min passivation. NC Ge pFETs with 40 min passivation have better electrical characteristics than the NC device with 60 min passivation in experiments. We also demonstrate the NC effect of HZO based NCFETs. For NCFETs, the steep SS and \( \frac{dV_{int}}{dV_G} > 1 \) are obtained. The NCFET with 40 min passivation has achieved a good matching between \( C_{FE} \) and \( C_{MOS} \), which contributes to the non-hysteretic characteristics. The different NC behaviors are considered to be related to the microscopic domain wall switching in the FE thin films.

**Abbreviations**

\( B^+ \): Boron ions; \( E_{OX} \): Equivalent oxide thickness; FETs: Field-effect transistors; HZO: HfZrO\(_x\); IC: Integrated circuit; I-MOS: Impact ionization metal-oxide-semiconductor; MOS: Metal oxide semiconductor; NC: Negative capacitance; NCFET: Negative capacitance field-effect transistor; NEMFET: Nano-electro-mechanical FET; S/D: Source/drain; SS: Subthreshold swing

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**Author’s Contributions**

RJZ carried out the experiments. JL tested the experimental results and drafted the manuscript. GQH and YL supported the study and helped to revise the manuscript. All the authors read and approved the final manuscript.

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**Availability of Data and Materials**

The datasets supporting the conclusions of this article are included in the article.

**Competing Interests**

The authors declare that they have no competing interests.

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