102 PFLOPS Lattice QCD quark solver on Fugaku

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Abstract

We present results on the world’s first over 100 PFLOPS single precision lattice QCD quark solver on the Japanese new supercomputer Fugaku. We achieve a factor 38 time speedup from the supercomputer K on the same problem size, $192^4$, with 102 PFLOPS, 10% floating-point operation efficiency against single precision floating-point operation peak. The evaluation region is the single precision BiCGStab for a Clover–Wilson Dirac matrix with Schwarz Alternating Procedure domain decomposition preconditioning using Jacobi iteration for the local domain matrix inversion.

Keywords: High performance computing; Lattice QCD; Iterative solver; A64FX.

1. Introduction

Lattice quantum chromodynamics (LQCD) is an application to solve problems in elementary particle physics. In LQCD, we compute the quantum chromodynamics (QCD) theory of quarks and gluons on the four-dimensional (4D) regular lattice. The solver of the Dirac equations, which is called “quark solver” and solved by iterative methods, consumes a large portion of CPU time in this application.

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The coefficient matrix of the quark solver using Wilson type fermions is a large sparse matrix. The 4D space and time is discretized to a 4D square lattice. Quark field of 12 complex numbers is put at the site and gauge field of 9 complex numbers is put at the link on the lattice. Computational speed is usually limited by the main memory bandwidth and the network bandwidth, although the required memory size is relatively small compared to other applications. Therefore achieving nice strong scaling is very challenging in LQCD.

In 2014, the Japanese government launched a project called “FLAGSHIP 2020 project”, aimed to develop a new national flagship supercomputer covering a wide range of applications that would run on the system to solve societal and scientific issues. The key concept of the project is “co-design” of the system and applications, where the application is optimized for the system, while the system is designed to satisfy the requirements of the application [1]. Using the applications developed for such societal and scientific issues including LQCD, the performance of the system had been estimated to explore the design space such as SIMD-length, cache sizes and so on [2]. LQCD contributes to the co-design as an application requiring high memory bandwidth and network bandwidth, the communication mechanism of direct memory access, low cache latency, low network latency, no OS jitter, and enough registers to maximize performance of floating-point arithmetic unit by out-of-order (OoO) execution. In this context, we describe our advanced optimization of the quark solver for Fugaku and the benchmark results of a practical physical problem size with the entire system of Fugaku.

This paper is organized as follows. In section 2, we explain the specification of the supercomputer Fugaku (hereinafter referred to as Fugaku). In section 3, we describe the structure and algorithms of the quark solver, and the regions to be optimized and measured for the benchmarking on Fugaku. The details of optimization employed in the quark solver on Fugaku are explained in section 4. The results of the benchmark tests on Fugaku are presented in section 5. Our conclusions are summarized in section 6.

2. Fugaku

Fugaku is a new Japanese supercomputer developed by RIKEN and Fujitsu, which is the successor of the supercomputer K (hereinafter referred to as K). In the recent TOP500, HPCG, HPL-AI, and Graph500 benchmark rankings, it has been ranked No. 1 in the world for three consecutive terms (June
It has a total of 432 racks with a total of 158,976 nodes (384 nodes × 396 racks + 192 nodes × 36 racks). One node has one A64FX processor \[4\] and 32 GiB main memory (four 8 GiB High Bandwidth Memory 2). The peak memory bandwidth per node is 1024 GB/s. The node has two external interfaces, one is computational network called Tofu interconnect D (TofuD) \[5\] and another is PCIe Gen3 16 lanes.

The A64FX processor has designed based on Armv8.2-A instruction sets with the Scalable Vector Extension (SVE). A64FX has 48 cores for compute and two or four assistant cores for OS services. It consists of four Core Memory Groups (CMG) connected by ring bus. Each CMG has 12 compute cores which share L2 cache. Two operating frequency modes of normal 2.0 GHz and boost 2.2 GHz are available on Fugaku. While the specification of the Armv8.2-A with SVE allows hardware developers to select a vector length from 128 to 2,048 bits, the 512-bit-width SIMD arithmetic units had been chosen on Fugaku. The processor supports OoO execution of instructions.

Other specifications are summarized in Table 1. The CPU die picture of A64FX is shown in Fig. 1.

| description | |
|-------------|-------------|
| Architecture | Armv8.2-A SVE (512 bit SIMD) |
| Core | 48 (+ 2 or 4 assistant cores) |
| Performance | |
| Normal mode | double prec. | single prec. | half prec. |
| 3.072 TF | 6.144 TF | 12.288 TF |
| Boost mode | 3.3792 TF | 6.7584 TF | 13.5168 TF |
| Cache | |
| L1D/core: 64 KiB, 4way, 256 GB/s (load), 128 GB/s (store) |
| L2/CMG: 8 MiB, 16way |
| L2/node: 4 TB/s (load), 2 TB/s (store) |
| L2/core: 128 GB/s (load), 64 GB/s (store) |
| Memory | 32 GiB, 1024 GB/s |
| Interconnect | TofuD (28 Gbps × 2 lane × 10 port) |
| PCIe | Gen3 16 lanes |
| Technology | 7nm FinFET |

We have developed “Lattice quantum chromodynamics simulation library for Fugaku with wide SIMD” (QWS \[6\]) to get high performance for computing quark solver on Fugaku. It is an open source software on github. The QWS
Figure 1: Die picture of A64FX.
library contains not only the optimized linear solver for quark solver but also may functions such as the sparse-matrix-vector multiplication routines or linear-algebra routines for quark fields, which can be used as building blocks of algorithms developed by the library users. As a practical example, we introduce the use in the multi-grid solver algorithm implemented in the Bridge++ code set in which the domain-decomposed Clover-Wilson operator in QWS is called alternatively to the original code and achieves considerable acceleration [7]. While the convention of the gamma-matrix and data layout are different in QWS and Bridge++, they are properly converted before and after the QWS functions are called.

We also expect that QWS provides a working example of the optimization techniques for A64FX architecture. While the quantitative evaluation of the components of QWS is specific to the fermion operator and execution setup, the improved implementation is generic and applicable to the other kinds of fermion operators as well as to many ingredients of LQCD simulations. Indeed in the multi-grid solver in [7] the other ingredients, such as the fermion operator on the coarse lattice and the inter-process communication, are accelerated by partly referring to the QWS implementation.

3. Quark solver on Fugaku

We consider to solve a linear equation derived from the equation of motion of quarks by the lattice discretization of the 4D space-time. We employ the so-called Clover–Wilson Dirac lattice quark action for the equation of motion of quarks on the lattice. In LQCD, we have to solve the following linear equation

\[ Ax = b, \]

by a huge amount of times using the quark solver. The coefficient matrix \( A \) derived from the Clover–Wilson lattice quark action is called the Clover–Wilson Dirac operator in the literature.
The explicit structure of the matrix-vector multiplication $Ax$ is as follows.

$$
\sum_{\beta=1}^{4} \sum_{b=1}^{3} \sum_{m} A_{(a,\alpha),(b,\beta)} (n,m) x_{(b,\beta)} (m) \\
= x_{(a,\alpha)} (n) - \kappa \sum_{\beta=1}^{4} \sum_{b=1}^{3} \sum_{\mu=1}^{4} \left[ (C_{\text{inv}} T_{\mu}^{+})_{(a,\alpha),(b,\beta)} (n) x_{(b,\beta)} (n + \hat{\mu}) \\
+ (C_{\text{inv}} T_{\mu}^{-})_{(a,\alpha),(b,\beta)} (n) x_{(b,\beta)} (n - \hat{\mu}) \right],
$$

where $n$ and $m$ denote the 4D lattice site indices, $a$ and $b$ are color indices running from 1 to 3, and $\alpha$ and $\beta$ are spin indices from 1 to 4. $x_{(a,\alpha)} (n)$ is a quark field element with the color index $a$ and spin index $\alpha$ located at the lattice site $n$ and takes a complex number. $\hat{\mu}$ denotes a unit vector pointing $\mu$-th direction in the 4D lattice. The small coefficient matrices $C_{\text{inv}} T_{\mu}^{\pm}$ represent the local dynamics among quarks and gluons by acting on the 12 complex components of the quark field, and vary during LQCD simulations. The details of $C_{\text{inv}} T_{\mu}^{\pm}$ are given in Appendix A. $\kappa$ parametrizes the quark mass, the smaller the heavier and the larger the lighter. Suppressing indices and its summation for simplicity, we use the following notation

$$
Ax = [I - \kappa C_{\text{inv}} H] x,
$$

where $C_{\text{inv}} H$ is called the hopping matrix and defined as the collection of the 4D three point stencil acting on the 12 components of the quark vector.

To solve Eq. (1), we employ the BiCGStab algorithm. Directly solving Eq. (1) in double precision is, however, not efficient due to the following mathematical and engineering reasons: incorporating preconditioning is quite recommended for iterative algorithms for numerical stability and efficiency, and current supercomputer systems are more powerful with lower precision arithmetic. We, therefore, employ the Schwartz Alternating Procedure (SAP) preconditioning with domain-decomposition [8] combined with the mixed-precision iteration technique [9, 10, 11]. In the following, we explain the structure of the SAP preconditioning and the mixed-precision solver technique implemented in QWS for Fugaku.

The SAP preconditioning is an approximation of the block Gauss-Seidel iteration. In our implementation on Fugaku, the block corresponds to the non-overlapping domain-decomposition of the lattice volume. We divide the
whole lattice volume into non-overlapping domains as shown in Fig. 2. Attached two colors (even or oddness of the domain indices) to each domain and using block notation, the coefficient matrix $A$ and vector $x$ can be expressed as

$$A = \begin{bmatrix} A_{EE} & A_{EO} \\ A_{OE} & A_{OO} \end{bmatrix}, \quad x = \begin{bmatrix} x_E \\ x_O \end{bmatrix},$$

where subscripts $E$ and $O$ denote the site indices belong to the even and odd domains, respectively. $A_{EE}$ only acts on $x_E$ located on even-colored domain sites, while $A_{EO}$ maps a vector $x_O$ located on odd-colored domain to a vector on even-colored domain. From the three-point stencil structure of $A$, $A_{EO}$ ($A_{OE}$) are the stencil operation from the surface sites of the nearest neighbor odd (even) domain to the ones of the even (odd) domain, respectively.
The SAP preconditioner $M_{\text{sap}}$ is defined as

$$M_{\text{sap}} = K \sum_{j=0}^{N_{\text{sap}}-1} (1 - AK)^j,$$

where $B_{EE}$ represents an approximation for $A_{EE}^{-1}$, $B_{OO}$ represents an approximation for $A_{OO}^{-1}$. $N_{\text{sap}}$ is an integer parameter of the SAP iteration. When $B_{EE}$ ($B_{OO}$) is exact to $A_{EE}^{-1}$ ($A_{OO}^{-1}$), the matrix $AK$ becomes upper triangular as

$$AK = \begin{bmatrix} A_{EE} & A_{EO} \\ A_{OE} & A_{OO} \end{bmatrix} \begin{bmatrix} A_{EE}^{-1} & O \\ -A_{OO}^{-1}A_{OE}A_{EE}^{-1} & A_{OO}^{-1} \end{bmatrix} = \begin{bmatrix} I - A_{EO}A_{OO}^{-1}A_{OE}A_{EE}^{-1} & A_{EO}A_{OO}^{-1} \\ O & I \end{bmatrix}. \quad (6)$$

Therefore it is expected the matrix $AK$ has a smaller condition number than that of $A$ even with approximation $B_{EE} \simeq A_{EE}^{-1}$ ($B_{EE} \simeq A_{EE}^{-1}$). The SAP preconditioner $M_{\text{sap}}$ is an approximation for $A_{EE}^{-1}$ followed by a truncated Neumann series for $(AK)^{-1}$ with the preconditioned matrix $AK$.

The approximate inverse matrix $B_{EE}$ are evaluated with the truncated Neumann series or equivalently Jacobi iteration as

$$B_{EE} = \sum_{j=0}^{N_{\text{jac}}} (I - A_{EE})^j. \quad (7)$$

The same form holds for $B_{OO}$ by replacing $EE$ with $OO$.

To achieve an efficient parallel performance, we divide the whole lattice volume consistent with the SAP preconditioning as shown in Fig. 2. We include two neighboring domains on an MPI rank, the one is even-colored and the other is odd-colored, so that all the MPI ranks participate in computing either of $B_{EE}$ or $B_{OO}$. On the other hand, in computing $A_{EO}$ or $A_{OE}$, it always requires MPI communication to do nearest neighbor stencil computation between surface sites in opposite colored domains. To minimize the communication time overhead, we overlap the point-to-point communication to the computation related to $A_{EE}$ or $A_{BB}$. We will explain the details of
the communication-computation overlapping using Fugaku’s Tofu hardware
and software in section 4.

The algorithms for matrix vector multiplication \( x = M_{\text{SAP}} b \) and \( x_E = B_{EE} b_E \) are shown in Algorithms 1 and 2 respectively. The communication-computation overlapping is possible for \( M_{\text{SAP}} \) as shown in lines 4 and 10 of Algorithm 1. However, the last communication (line 17) cannot be overlapped. To further overlap the last communication over the computation, we also provide \( AM_{\text{SAP}} \) as a combined matrix-vector multiplication routine for the iterative solver. The algorithm for \( x = AM_{\text{SAP}} b \) is shown in Algorithm 3, where all communications are overlapped with computations.

Provided the above matrix-vector multiplication routines (Algs. 1, 2, and 3) as building blocks, instead of solving Eq. (1) directly, we apply the BiCGStab algorithm to solve

\[
(AM_{\text{SAP}})y = b,
\]

for \( y \) and the solution for \( x \) is given by

\[
x = M_{\text{SAP}} y.
\]

In this paper, we focus on the performance tuning details of the single-precision BiCGStab solver for solving Eq. (8). However, realistic LQCD simulations need the double-precision (DP) solutions of Eq. (1). To obtain the double-precision solution using single-precision (SP) arithmetic as far as possible, we employ the so-called mixed-precision strategy [9]. Here we briefly explain the idea of the strategy before explaining the details of the single-precision BiCGStab algorithm implemented in QWS for Fugaku.

The key idea of the mixed-precision is in the Richardson-iteration or equivalently deficit correction iteration method with the approximate single-precision solutions. When an approximation \( x_{\text{SP}} = A_{\text{SP}}^{-1} b_{\text{SP}} \) with SP is available, the backward error in DP for Eq. (1) is

\[
r = b - AP_{\text{DP}}(x_{\text{SP}}),
\]

where \( r, b \) and \( A \) are in DP, and it is omitted for clarity. The operation \( P_{\text{DP}}(\ldots) \) converts the precision of the argument from SP to DP. The DP solution \( x \) requires \( r = 0 \) in DP, we can enforce this by adding a correction vector \( \delta x \) to \( P_{\text{DP}}(x_{\text{SP}}) \) as

\[
x = P_{\text{DP}}(x_{\text{SP}}) + \delta x.
\]
The vanishing residual for $x$ in Eq. (11) requires

$$0 = b - Ax$$

$$= b - A(P_{DP}(x_{SP}) + \delta x)$$

$$= b - AP_{DP}(x_{SP}) - A\delta x$$

$$= r - A\delta x. \tag{12}$$

The correction vector $\delta x$ must be the solution of $A\delta x = r$ and it is again obtained approximately with a SP iterative solver as $\delta x_{SP} = A_{SP}^{-1}r_{SP}$. This process repeats until the residual converges below a tolerance in DP.

Algorithm 4 shows the pseudo-code. $R_{SP}(\ldots)$ reduces the precision of the argument from DP to SP. The rescalings with err at lines 5 and 7 are required to avoid underflow in the single precision solver at the line 6. This DP iteration loop (lines 4–14) is called outer-loop while the iterative loops in the SP solver (line 6) are inner-loop. We can employ more sophisticated algorithms for the outer-loop where the SP solver (inner-loop) is regarded as a flexible preconditioner to the target linear equation. The “flexible” means that the preconditioner can be flexibly varied iteration by iteration during the outer-loop iterations. Flexible GMRES, Flexible BiCG and BiCGStab are examples of the flexible iterative solver algorithms for non-Hermitian matrices \cite{12}. As seen from Algorithm 4, it is expected that the residual norm $|r|$ reduces by a factor of $O(10^{-6})$ by every iteration provided that the SP solution has an accuracy of $|p_{SP} - A_{SP}q_{SP}| < O(10^{-6})$, and the DP solution will be obtained after a few iterations of the outer-loop.

Algorithm 5 shows the single-precision BiCGStab solver to solve Eq. (8) in QWS on Fugaku. In our implementation, we employ a slightly different algorithm from those in the literature. The iteration has two loop-exit points (lines 14 and 22), saving the cost of one matrix-vector multiplication at the convergence. There are several global synchronization points for the norm and dot-product computations. To reduce the number of synchronization points, we move the computation of $\rho = \langle \tilde{r}|r \rangle$ from just before line 24 to line 20. As we will explain in the next section, Fugaku’s TofuD has a capability to reduce three floating-point elements simultaneously in a single reduction operation. In our implementation, therefore, each latency of the global reduction communication is identical to that of the single element reduction communication.
Algorithm 1 QWS SAP preconditioner: $x = M_{\text{SAP}} b$, $M_{\text{SAP}} = \text{prec}_s \simeq A^{-1}$. Input and output vectors: $b, x$, and working vectors: $s, q$

Input: $b$: source vector, $N_{\text{SAP}}, N_{\text{JAC}}$: iteration count

Output: $x$: multiplied by the SAP preconditioner $x = M_{\text{SAP}} b$

1. $s = b$
2. for $i = 0; i < N_{\text{SAP}}; i++$
   ▷ [Algorithm 2]
3. $s_E = B_{\text{EE}} s$
4. [Start sending surface data of $x_E$ for $A_{OE} x_E$.]
5. $q_E = A_{EE} x_E$
6. $s_E = s_E + b_E - q_E$
7. [Wait for receiving surface data of $x_E$ from line 4]
8. $s_O = s_O - A_{OE} x_E$
9. $x_O = B_{OO} s_O$
   ▷ [Algorithm 2]
10. [Start sending surface data of $x_O$ for $A_{EO} x_O$.]
11. $q_O = A_{OO} x_O$
12. $s_O = s_O + b_O - q_O$
13. [Wait for receiving surface data of $x_O$ from line 10]
14. $s_E = s_E - A_{EO} x_O$
15. end for
16. $x_E = B_{\text{EE}} s_E$
   ▷ [Algorithm 2]
17. [Start sending surface data of $x_E$ for $A_{OE} x_E$.]
18. [Wait for receiving surface data of $x_E$ from line 17]
19. $s_O = s_O - A_{OE} x_E$
20. $x_O = B_{OO} s_O$
   ▷ [Algorithm 2]

Algorithm 2 QWS approximate inversion of $A_{EE}: x_E = B_{EE} b_E$, $B_{EE} = \text{jinv}_d_{dd}_d_{in}_s \simeq (A_{EE})^{-1}$. Input and output vectors: $b_E, x_E$, and working vectors $q_E$.

Input: $b_E$: source vector, and $N_{\text{JAC}}$: iteration count

Output: $x_E$: approximate solution vector, $x_E = B_{EE} b_E$

1. $q_E = A_{EE} b_E$
2. $x_E = 2 b_E - q_E$
3. for $j = 1; j < N_{\text{JAC}}; j++$
   ▷ $q_E = A_{EE} x_E$
4. $x_E = x_E + b_E - q_E$
5. end for
Algorithm 3 QWS multiplying preconditioned matrix: $x = AM_{SAP}b$

$AM_{SAP} = \text{prec}_{ddd}s \simeq I$. $AM_{SAP}$ is Domain-decomposition preconditioned operator. Input and output vectors: $b, x$, and working vectors: $s, q$.

**Input:** $b$: source vector, $N_{SAP}, N_{JAC}$: iteration count for Algorithms 1 and 2

**Output:** $x$: multiplied by preconditioner, $x = AM_{SAP}b$

[Lines: 1–15 are the same as those of Algorithm 1.]

16: $q_E = A_{EES}E$
17: [Start sending surface data of $q_E$ for $A_{OE}q_E$.]
18: $x_E = A_{EE}q_E$
19: [Wait for receiving surface data of $q_E$ from line 17]
20: $s_O = s_O - A_{OE}q_E$
21: $q_O = A_{OOS}O$
22: [Start sending surface data of $q_O$ for $A_{EO}q_O$.]
23: $x_O = x_O + A_{OO}q_O$
24: [Wait for receiving surface data of $q_O$ from line 22]
25: $x_E = x_E + A_{EO}q_O$

Algorithm 4 Deficit correction iteration to obtain DP solution using SP iterative solver.

**Input:** $b$: DP source vector, tol: stopping condition

**Output:** $x$: DP solution vector, $x = A^{-1}b$ with $|b - Ax|/|b| < tol$

1: $x = 0$
2: $r = b$
3: err = $|r|$
4: loop
5: $p_{SP} = R_{SP}(r/\text{err})$
6: $q_{SP} = A_{SP}^{-1}p_{SP}$ \hspace{1cm} \triangleright \text{an iterative solver}
7: $\delta x = \text{err} P_{DP}(q_{SP})$
8: $x = x + \delta x$
9: $r = b - Ax$ or $r = r - A\delta x$
10: err = $|r|$
11: if err$/|b| < tol$ then
12: Exit loop
13: end if
14: end loop
Algorithm 5 QWS $x = (AM_{SAP})^{-1}b$, bicgstab_precdd_s_. Single precision BiCGStab solver for $AM_{SAP}x = b$. Suffixes SP are omitted. Input and output vectors $b, x$, working vectors $p, q, r, \tilde{r}, t$.

**Input:** $b$ : source vector, $N_{SPA}, N_{JAC}$ : iteration count, tol : stopping condition

**Output:** $x$ : solution vector, $x = (DM_{SAP})^{-1}b$ with $|b - DM_{SAP}x|/|b| < tol$

1: $x = 0$
2: $r = b$
3: $p = b$
4: $\tilde{r} = b$ $\triangleright$ [1-real reduction = 1 float reduction]
5: $\text{bnorm2} = |b|^2$
6: $\rho_0 = \text{bnorm2}$
7: for iter = 0; iter < maxiter; iter++ do
8: $q = (DM_{SAP})p$ $\triangleright$ [Algorithm 3]
9: $\alpha = \rho_0/(\tilde{r}|q|)$ $\triangleright$ [1-complex reduction = 2 float reductions]
10: $x = x + \alpha p$
11: $r = r - \alpha q$
12: $rnorm2 = |r|^2$ $\triangleright$ [1-real reduction = 1 float reduction]
13: if $\sqrt{rnorm2}/\text{bnorm2} < tol$ then
14: exit
15: end if
16: $t = (DM_{SAP})r$ $\triangleright$ [Algorithm 3]
17: $\omega = (t|r|/|t|^2$ $\triangleright$ [1-complex + 1-real reductions = 3 float reductions]
18: $x = x + \omega r$
19: $r = r - \omega t$
20: $\text{rnorm2} = |r|^2, \rho = \langle \tilde{r}|r \rangle$ $\triangleright$ [1-real and 1-complex reductions = 3 float reductions]
21: if $\sqrt{\text{rnorm2}}/\text{bnorm2} < tol$ then
22: exit
23: end if
24: $\beta = \alpha \rho / (\rho_0 \omega)$
25: $\rho_0 = \rho$
26: $p = r + \beta (p - \omega q)$
27: end for

4. Tuning quark solver on Fugaku

To get high performance on Fugaku, effective SIMD vectorization with 512 bits wide SIMD is very important. Since the matrix-vector multiplication of LQCD, which is nine-point stencil type on 4D Euclidean space-time, has a less local complexity using complex arithmetics, we have to locate single precision data appropriately fit in 512bits wide SIMD vector along with the physics local structure. We employ the following real number data layout
(C-style array or Row major order),

Fugaku(double) : \[nt][nz][ny][nx/8][3][4][2][8] ,
Fugaku(single) : \[nt][nz][ny][nx/16][3][4][2][16] ,
Fugaku(half) : \[nt][nz][ny][nx/32][3][4][2][32] ,
cf. K : \[nt][nz][ny][nx][3][4][2] ,

\begin{equation}
(13)
\end{equation}

where nt, nz, ny, nx are the local domain lattice size in t,z,y,x directions, respectively. nx is divided and packed to the SIMD of Fugaku. The factor 3 sized rank corresponds to the color index, the 4 sized rank to the spin index, and the 2 sized rank to the complex real-imaginary index. We used the complex number data major layout on K. For Fugaku, we layout continuous x site index first by blocking to fit with 512 bits wide SIMD vector. We optimize the x-direction calculation by using Arm C Language Extensions (ACLE) \[13\]. For the stencil computation in the x-direction, the vector element shift operation is required. Instead of shifting data on vector registers, we utilize vector load with mask operation (named predicate operation) functionality of SVE. Fig \[3\] is a schematic picture of the x-direction shift for double precision data layout by using two load operations with predicate registers and one XOR operation.

We also have applied other general optimizations, e.g., removing temporal arrays, manually prefetching explicitly 256 B for all arrays by software prefetch, OMP Parallel region expansion that we put “omp parallel” on higher level caller routines because making omp parallel region is costly. This is important on many core architectures.

A function \_\_mult_clvs\_, which corresponds to local matrix multiplication of \(C_{inv}\) in Eq. \[3\], is used in \texttt{ddd\_in\_s\_} (\(A_{EE}\) or \(A_{OO}\)), \texttt{jinv\_ddd\_in\_s\_} (\(B_{EE}\) or \(B_{OO}\)), and \texttt{ddd\_out\_s\_} (\(A_{EO}\) or \(A_{OE}\)). We found that a naive implementation of \_\_mult_clvs\_ was inefficient due to load and store operations caused by register spill/fill. It is difficult for the compiler to calculate the optimal instruction schedule for such a large computation. However, we found a pattern on the code that allows an efficient schedule. Then, we reordered the operations at the source code level. Fig. \[4\] is the outline of the original code. The blocks starting with the red line share four values. So by arranging the rows of these blocks in a round robin fashion, we can minimize the interval of value reuse and get instruction-level parallelism. Fig. \[5\] is the the optimized code, where 16 streams of chained FMA (Fused Multiply-Add) operations are executed in a round robin fashion. Since the FMA latency
Figure 3: X–direction shift by using two load operations with predicate registers and one XOR operation for data layout in double precision.
is 9 and the number of the FMA pipelines is 2, 18 independent operations are required to fill the pipelines. Therefore, the theoretical efficiency of this code is 89 % (=16/18). In addition, the schedule allows for the reuse of register values at short intervals; the number of registers required does not exceed 32 (the number of registers in the architecture). Since each loaded value is reused once, the number of FMAs and loads are equal. Since the FMA and load pipelines are also equal in number, the load pipeline will not become a bottleneck. We prevented undesired compiler optimization, which is common subexpression elimination for long-distance reuse, by splitting blocks with if statements. We also specified the compiler flags that suppress instruction scheduling (-Knosch_post_ra -Knosch_pre_ra -Knoeval). We confirmed that these optimizations reduced the number of spills from the original 512 to the optimized 14.

4.1. Minimizing communication

The boundary matrices $A_{EO}$ and $A_{OE}$ contain nearest neighbor stencil communication between surface sites. To minimize communication time, we adopt the double buffering algorithm and implement it by using the uTofu API library to directly use the RDMA engine called Tofu Network Interface (TNI) instead of the MPI communication library. The uTofu interface has lower latency than that of MPI and they can be used together in an application, so that global operations such as reduction for vector inner-product are processed by MPI functions while the nearest neighbor 1-to-1 communications are done by uTofu. Choice of a proper rankmap and assignments of TNIs are also important to extract the best performance of TofuD in the neighboring communication.

The double buffering algorithm uses one send buffer and two receive buffers for each neighboring direction. The outline of the algorithm is depicted in Fig. 6. The RDMA put is issued by utofu.put instruction. We use a strong ordering mode with which the arrival of the last byte in the buffer guarantees the arrival of the whole data in the buffer. The integer valued flag byte at the end of the buffer is updated by the sender. In order the cache injection mechanism to work, which directly puts the data to the last level cache of the receiver as well as the main memory, the receiver should not modify the contents of the receive buffer. The receiver polls the last byte

\footnote{We may call it process placement more generally.}
void __mult_clvs(rvecs_t sc[3][4][2], rvecs_t a[2][36]) {
    rvecs_t x[2][6][2];
    rvecs_t y[2][2];
    for (int c=0; c<3; c++) {
        for (int ri=0; ri<2; ri++) {
            for (int v=0; v < VLENS; vv++) {
                x[0][0+c][ri].v[v] = sc[c][0][ri].v[v] + sc[c][2][ri].v[v];
                x[0][3+c][ri].v[v] = sc[c][1][ri].v[v] + sc[c][3][ri].v[v];
                x[1][0+c][ri].v[v] = sc[c][0][ri].v[v] + sc[c][2][ri].v[v];
                x[1][3+c][ri].v[v] = sc[c][1][ri].v[v] + sc[c][3][ri].v[v];
            }
        }
    }
    for (int i=0; i<2; i++) {
        for (int v=0; v < VLENS; vv++) {
            y[i][0].v[v] = a[i][0].v[v] * x[i][0][0].v[v] + a[i][6].v[v] * x[i][1][0].v[v] + a[i][8].v[v] * x[i][2][0].v[v] + a[i][10].v[v] * x[i][3][0].v[v] + a[i][12].v[v] * x[i][4][0].v[v] + a[i][14].v[v] * x[i][5][0].v[v] - a[i][7].v[v] * x[i][1][1].v[v] - a[i][9].v[v] * x[i][2][1].v[v] - a[i][11].v[v] * x[i][3][1].v[v] - a[i][13].v[v] * x[i][4][1].v[v] - a[i][15].v[v] * x[i][5][1].v[v];
            y[i][1].v[v] = a[i][0].v[v] * x[i][0][1].v[v] + a[i][6].v[v] * x[i][1][1].v[v] + a[i][8].v[v] * x[i][2][1].v[v] + a[i][10].v[v] * x[i][3][1].v[v] + a[i][12].v[v] * x[i][4][1].v[v] + a[i][14].v[v] * x[i][5][1].v[v] + a[i][7].v[v] * x[i][1][0].v[v] + a[i][9].v[v] * x[i][2][0].v[v] + a[i][11].v[v] * x[i][3][0].v[v] + a[i][13].v[v] * x[i][4][0].v[v] + a[i][15].v[v] * x[i][5][0].v[v];
        }
    }
    for (int v=0; v < VLENS; vv++) {
        sc[0][0][0].v[v] = y[0][0].v[v] + y[1][0].v[v];
        sc[0][0][1].v[v] = y[0][1].v[v] + y[1][1].v[v];
        sc[0][2][0].v[v] = y[0][0].v[v] - y[1][0].v[v];
        sc[0][2][1].v[v] = y[0][1].v[v] - y[1][1].v[v];
        sc[0][2][2].v[v] = y[0][2].v[v] - y[1][2].v[v];
    }
}

The same pattern follows by 6 times

Figure 4: __mult_clvs before optimizations.

of the buffer and wait until it has been updated. After using the arrived data, the parity flag to specify the receive buffer out of two buffers is flipped in both sender and receiver sides. Note that the sender also needs to know to which buffer the data to be sent. To detect that the sending has been finished, the sender polls a queue called Transmit Complete Queue (TCQ) in the RDMA engine. Another queue to be polled is Message Receive Queue (MRQ), which stores notices related to data receiving. Although we do not
use the information in the MRQ, to avoid flooding of the queue we insert a polling to clean it before waiting the data arrival; since the communication takes longer than the calculation in the bulk, this is the best place to poll the MRQ.

A natural network topology for LQCD is 4D torus while the network of Fugaku is 6-dimensional mesh-torus. We need a proper rankmap to build a 4-dimensional logical torus, that is, 4 closed loops of MPI ranks or MPI processes, to reduce the hopping in the neighboring communication. The network of Fugaku has 3 closed loops along X-, Z-, and B-axes of TofuD. Y-axis is open, A- and C- axes are made of 2 nodes. We divide Z-axis into two-dimensional mesh-torus, as depicted in Fig. 7, where Zc is continuous open 3 nodes and Zd makes a closed loop made of 8 nodes. Noting that provided 2 independent axes it is easy to construct a closed loop topology,
we construct the following 4 logical QCD loops of nodes:

- QCD X: 6 nodes, $A \times Z_c$
- QCD Y: 16 nodes, $C \times Z_d$
- QCD Z: 24 nodes, X
- QCD T: 64 nodes, $B \times Y$

Each node has 4 processes, which are divided into $1 \times 2 \times 2 \times 1$ along the logical 4D torus. In total, we have 4D torus of $6 \times 32 \times 48 \times 64$ processes for problem size of $192^4$.

The uTofu interface allows us to specify which TNI to be used in each communication. We assign the TNIs such that the communication load is balanced. In counting the amount of data that the TNI injects, the data to $Z_d$ axis is weighted by 3 because of its stride in the hopping. The intra-node commutation is also counted as weight 1, as we send the data thorough TNI without using the shared memory of the node.
Figure 6: Sketch of double buffering algorithm. The receive buffer is doubled and there is no step to check whether the receive buffer is available. The primed steps use the second receive buffer. 1–2 and 1’–2’ are for [Start sending...] and 4 and 4’ is for [Wait for receiving...] in Algorithms 1 and 3. Note that the receiver does not clear the integer flag at the end of the buffer but the sender update it before starts sending. “isend”, “recv”, and “send” correspond to those in Table 5.

Figure 7: The Z axis (left panel) is divided into a two dimensional mesh-torus topology (the right panel). Since the original Z axis has a torus topology, Zd axis is also a torus.
5. Benchmark results

Benchmark tests are performed on the boost mode 2.2 GHz in which both two floating-point arithmetic pipelines are fully utilized at the high frequency.

The elapse time and performance of 500 BiCGStab iterations and $A_{EE}$ and $A_{OO}$ regions are listed in Table 2 and Table 3 for several problem sizes per MPI process. We see that the performance of BiCGStab iteration for $32 \times 6 \times 4 \times 6$ is the best in the tests when the communication is not taken into consideration.

Table 2: Elapse time and performance of 500 BiCGSTab iterations measured on two MPI processes using two CMGs for several problem sizes per MPI process. FLOP indicates a floating-point operation count calculated theoretically. Efficiency indicates floating-point operation efficiency against the single precision floating-point operation peak.

| Size       | Elapse [s] | TFLOPS | Efficiency | FLOP       |
|------------|-----------|--------|------------|------------|
| $32 \times 6 \times 4 \times 3$ | 0.334867  | 0.8272 | 12.24%     | 69254421000 |
| $32 \times 6 \times 4 \times 6$ | 0.515010  | 1.0839 | 16.04%     | 139560981000 |
| $32 \times 6 \times 8 \times 6$ | 1.145754  | 0.9786 | 14.48%     | 280304661000 |
| $32 \times 6 \times 8 \times 12$ | 2.606202  | 0.8616 | 12.75%     | 561369621000 |
| $32 \times 12 \times 8 \times 12$ | 5.778703  | 0.7773 | 11.50%     | 1122981141000 |

Table 3: Same as Table 2 but for regions of $A_{EE}$ and $A_{OO}$ during 500 BiCGSTab iterations.

| Size       | Elapse [s] | TFLOPS | Efficiency | FLOP       |
|------------|-----------|--------|------------|------------|
| $32 \times 6 \times 4 \times 3$ | 0.068043  | 1.1208 | 16.58%     | 19065600000 |
| $32 \times 6 \times 4 \times 6$ | 0.119455  | 1.3170 | 19.49%     | 39329280000 |
| $32 \times 6 \times 8 \times 6$ | 0.219403  | 1.4693 | 21.74%     | 80593920000 |
| $32 \times 6 \times 8 \times 12$ | 0.559297  | 1.1699 | 17.31%     | 163584000000 |
| $32 \times 12 \times 8 \times 12$ | 1.192644  | 1.1146 | 16.49%     | 332328960000 |

Global Allreduce can be a bottleneck when the number of processes is large. The Allreduce of the MPI implementation for Fugaku is accelerated by using Tofu barrier which is an offload engine to execute collective operations without involving CPU. Up to three elements of MPI_DOUBLE or

---

2A64FX has an Eco mode that one of the two floating-point arithmetic pipelines is stopped
MPI_FLOAT, the reduction arithmetics are performed on the Tofu barrier. It is one of the achievements of co-design that this feature, which was applicable to only one element on K, has been extended to three elements on Fugaku, and we stressed the importance of this to the hardware development department early in the project. Taking advantage of this feature, QWS has constructed a solver algorithm as introduced in section 3. To reduce the number and latency of Allreduce for inner product calculation, three independent real numbers can be summed up in a single Allreduce operation.

Here we show the benchmark results of the standalone Allreduce function. In Table 4, we show Allreduce benchmark results on 72 racks, 27648 nodes of $48 \times 12 \times 48$ node shape by using “Intel(R) MPI Benchmarks 2019 Update 6, MPI 1 part (IMB–MPI1)”. We see that Allreduce up to three elements with the Tofu barrier is about six times faster than one without the Tofu barrier and it is faster to split MPI_Allreduce for 15 elements into five MPI_Allreduce for three elements.

Table 4: Allreduce benchmark by IMB–MPI1 on $48 \times 12 \times 48$ nodes with and without Tofu barrier. Minimum (min), maximum (max), and average (avg) time for repetition number, 10000 are shown. The number of bytes (byte) is a message length to be reduced per one MPI_Allreduce call. And the number of counts (count) is a number of elements. The data type of MPI_FLOAT is reduced as default of IMB–MPI1.

| byte | count | with Tofu barrier | without Tofu barrier |
|------|-------|------------------|----------------------|
|      |       | min [ µs] | max [ µs] | avg [ µs] | min [ µs] | max [ µs] | avg [ µs] |
| 0    | 0     | 0.09       | 0.14       | 0.10       | 0.10       | 0.16       | 0.12       |
| 4    | 1     | 7.60       | 11.33      | 9.46       | 55.69      | 69.05      | 62.83      |
| 8    | 2     | 8.25       | 10.79      | 9.50       | 55.79      | 68.93      | 62.91      |
| 12   | 3     | 8.25       | 10.93      | 9.57       | 55.89      | 69.02      | 62.94      |
| 16   | 4     | 58.99      | 66.95      | 62.68      | 56.42      | 69.71      | 63.51      |
| 32   | 8     | 61.50      | 72.34      | 66.32      | 78.24      | 97.57      | 88.14      |
| 64   | 16    | 61.61      | 72.38      | 66.31      | 78.63      | 97.84      | 88.42      |
| 128  | 32    | 63.70      | 74.45      | 68.43      | 80.46      | 99.56      | 90.10      |

We show a weak scaling plot of the evaluation region in Fig. 8. We see a nice weak scaling from 432 nodes to the targeted 147456 nodes with a few exceptions caused by OS jitters. The elapse time increases 0.05 ms (about 7 %) from 432 nodes to 147456 nodes due to the time for Allreduce. We can see that the increase time is roughly the same as the Allreduce time in Table 5. The elapse times of five benchmark tests on 147456 nodes are 0.8000,
0.7998, 0.7982, 0.7989, and 0.7978 ms, respectively. These are about 38.3 times faster than the elapse time, 30.65 ms, for same problem setup on the full system of K.

This performance on Fugaku is 102 PFLOPS sustained with SP arithmetic and corresponds to 10% efficiency to 996 PFLOPS of the peak SP performance of 147456 nodes of Fugaku. Averaged power of the evaluation region is about 20 MW. The power efficiency is 5 GFLOPS/W. For comparison, the power efficiency on the LINPACK benchmark at November 2020 is about 15 GFLOPS/W [3].

Figure 8: Weak scaling of the evaluation region. 158976 nodes is a total nodes of Fugaku. The vertical line at 147456 nodes denotes the number of nodes used in the benchmark for the target problem size.

Table 5 shows a breakdown of total elapse time for target problem size on 147456 nodes. The elapse times for “isend”, “recv”, and “send” are the elapse times for “isend”, “recv”, and “send” shown in Fig 6 respectively.
The elapse times of “reduc1”, “reduc2”, and “reduc3” are of 1, 2, and 3 float reductions in the for loop of iter respectively in Algorithm 5. Summed total elapse time in the table is slightly longer than 0.8000 ms which is measured in peak performance tests. The difference is due to a non-negligible overhead to measure elapse times for each region. We see the half of time is spent for communication. In the practical production runs, we may better use less nodes.

Table 5: Elapse time breakdown. Total time is divided into calculation time (all_calc) and communication time (all_comm). all_comm is divided into three parts for neighboring communication and three parts for Allreduce.

| region  | Elapse time [ms] |
|---------|------------------|
| all_calc| 0.400            |
| all_comm| 0.407            |
| isend   | 0.029            |
|recv     | 0.254            |
|send     | 0.062            |
|reduc1   | 0.015            |
|reduc2   | 0.016            |
|reduc3   | 0.031            |
|total    | 0.807            |

6. Summary

We have achieved 102 PFLOPS, 10% floating-point operation efficiency against single precision floating-point operation peak, of Clover–Wilson quark solver on 192^4 lattice on the supercomputer Fugaku. Optimization techniques used in QWS are general except for that using ACLE and uTofu and can be available in other applications. All the results have been obtained on the evaluation environment in the trial phase. It does not guarantee the performance, power and other attributes of the supercomputer Fugaku at the start of its public use operation. However, we expect we shall get better performance with improved compiler, middleware, and McKernel\(^3\) which is a light-weight multi-kernel operating system designed for high-end supercomputing [14].

\(^3\)No OS jitter is expected.
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Appendix A. Clover–Wilson Dirac operator

Clover–Wilson Dirac operator is

\[
D = 1 + C - \kappa H ,
\]

\[
D = 1 + C - \kappa \sum_{\mu=1}^{4} (T^{+}_{\mu} + T^{-}_{\mu}) ,
\]

where

\[
C = \frac{i}{2} \kappa c_{SW} \sigma_{\mu\nu} F_{\mu\nu}(n) \delta_{m,n} ,
\]

\[
T^{\pm}_{\mu} = (1 \mp \gamma_{\mu}) U_{\pm\mu}(n) \delta_{n,m \pm \hat{\mu}} .
\]

\( \kappa \) and \( c_{SW} \) are input parameters. \( n \) is 4D, \( n = (n_1, n_2, n_3, n_4) , n_{\mu} \in \mathbb{Z} \). \( \hat{\mu} \) is unit vector of \( \mu \), for instance, \( \hat{1} = (1,0,0,0) \). \( U_{\mu}(n) \) is SU(3) matrix. \( U_{-\mu}(n) = U_{\mu}^{\dagger}(n - \hat{\mu}) \). \( \sigma_{\mu\nu} = i/2(\gamma_{\mu}\gamma_{\nu} - \gamma_{\nu}\gamma_{\mu}) \). \( 3 \times 3 \) matrix valued \( F_{\mu\nu}(n) \) is a field strength. \( C \) is a block diagonal matrix made by \( 12 \times 12 \) Hermitian matrices. \( C_{\text{inv}} \) appeared in section 3 is defined as

\[
C_{\text{inv}} = (1 + C)^{-1} .
\]

Multiplication of \( H \) and vector is an eight points stencil calculation for multiplication between \( 3 \times 3 \) matrix and four vectors of three elements, i.e. 4
spinor and 3 color. Gamma matrices $\gamma_\mu$ are

$\gamma_1 = \begin{pmatrix} 0 & 0 & 0 & +i \\ 0 & 0 & +i & 0 \\ 0 & -i & 0 & 0 \\ -i & 0 & 0 & 0 \end{pmatrix}$ \hspace{1cm} (A.4)

$\gamma_2 = \begin{pmatrix} 0 & 0 & 0 & +1 \\ 0 & 0 & -1 & 0 \\ 0 & -1 & 0 & 0 \\ +1 & 0 & 0 & 0 \end{pmatrix}$ \hspace{1cm} (A.5)

$\gamma_3 = \begin{pmatrix} 0 & 0 & +i & 0 \\ 0 & 0 & 0 & -i \\ -i & 0 & 0 & 0 \\ 0 & +i & 0 & 0 \end{pmatrix}$ \hspace{1cm} (A.6)

$\gamma_4 = \begin{pmatrix} +1 & 0 & 0 & 0 \\ 0 & +1 & 0 & 0 \\ 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & -1 \end{pmatrix}$ \hspace{1cm} (A.7)

This is one of the unitary equivalent representations of Gamma matrices.

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