ABSTRACT
The recent breakthroughs in deep neural networks (DNNs) have spurred a tremendously increased demand for DNN accelerators. However, designing DNN accelerators is non-trivial as it often takes months/years and requires cross-disciplinary knowledge. To enable fast and effective DNN accelerator development, we propose DNN-Chip Predictor, an analytical performance predictor which can accurately predict DNN accelerators’ energy, throughput, and latency prior to their actual implementation. Our Predictor features two highlights: (1) its analytical performance formulation of DNN ASIC/FPGA accelerators facilitates fast design space exploration and optimization; and (2) it supports DNN accelerators with different algorithm-to-hardware mapping methods (i.e., dataflows) and hardware architectures. Experiment results based on 2 DNN models and 3 different ASIC/FPGA implementations show that our DNN-Chip Predictor’s predicted performance differs from those of chip measurements of FPGA/ASIC implementation by no more than 17.66% when using different DNN models, hardware architectures, and dataflows. We will release code upon acceptance.

Index Terms— DNN accelerator, ASIC, FPGA, design simulator, design automation

1. INTRODUCTION
Deep Neural Networks (DNNs) have achieved record-breaking performance in various applications, such as image classification [1][2] and natural language processing [3]. However, their powerful performance often comes with a prohibitive complexity [4][5][6][7][8]. Moreover, DNN-based applications often require not only high accuracy, but also aggressive hardware performance, including high throughput, low latency, and high energy efficiency. As such, there has been intensive research on DNN accelerators in order to take advantage of different hardware platforms, such as FPGAs and ASICs, for improving DNN acceleration efficiency [9][10][11][12][13][14].

While DNN accelerators can be 1000× more efficient than general purpose computing platforms [15], developing DNN accelerators presents significant challenges, because: (1) mainstream DNNs have millions of parameters and billions of operations; (2) the design space of DNN accelerator is large due to numerous design choices of architectures, hardware IPs, DNN-to-accelerator-mappings, etc.; and (3) there is an algorithm/hardware co-design need for the same DNN functionality to have a different decomposition that would require different hardware IPs and thus correspond to dramatically different hardware performance/energy/area trade-offs. Therefore, high-quality DNN accelerators often take months/years to design and require a large team of cross-disciplinary experts with knowledge in DNN algorithms, micro-architectures, and physical chip design. Such a barrier makes it difficult to scientifically explore innovative DNN accelerator design and thus limits DNNs’ more extensive applications.

To address the aforementioned challenges, we propose DNN-Chip Predictor, an analytical performance predictor which can efficiently and accurately predict DNN accelerators’ performance prior to time-consuming ASIC/FPGA hardware implementation. Specifically, our Predictor formulates DNN accelerators’ energy, throughput, and latency based on parameters that characterize the DNN models and corresponding accelerators’ architectures and algorithm-to-hardware mapping methods (i.e., dataflows). Such a generic Predictor (1) enables fast evaluation of DNN accelerator innovations and (2) can be used as an efficient design exploration and optimization tool for DNN accelerators, given their large design space. To the best of our knowledge, our proposed Predictor is the first that highlights the following three features simultaneously for practical and wide adoption: (1) analytical and thus fast; (2) covering both ASIC and FPGA DNN accelerators; (3) are validated using different DNN models and accelerator designs (i.e., architectures, dataflows, and process technologies).

2. BACKGROUND
DNN Accelerators. There have been intensive studies of DNN accelerators. For example, the first well-optimized FPGA DNN accelerator [16] uses loop tiling; the DianNao series [13][17] is an early effort on synthesis based ASIC accelerators; Eyeriss proposes a row-stationary dataflow [14] to reduce expensive DRAM accesses; and Google TPUs [11][12] use a systolic array to achieve high throughput.

DNN Accelerator Performance Prediction. DNNs often feature a high complexity while there exists various opportunities for reuse, pipeline, and resource allocation to maximize DNN accelerators’ performance. Therefore, an accurate yet fast performance predictor is desired to enable efficient design space exploration and optimization with different performance trade-offs. Various methods have been developed for predict-
ing or simulating DNN accelerators’ performance. Roofline models [16,18] and customized analytical models which are closely tied to the specific design attributes [9][19][20] are used. However, the roofline model lacks fine-grained estimation and customized models are not general as desired. Timeloop [21] and Eyeriss [22] use for and parallel-for to describe the temporal and spatial mapping of DNN accelerators. Specifically, Timeloop obtains the number of memory accesses and estimates the latency by calculating the maximum isolated execution cycle across all hardware IPs based on a double-buffering assumption. Accelergy [23] proposes a configuration language to describe hardware architectures and depends on plug-ins, e.g., Timeloop, to calculate the energy as in [14]. The work in [24] adopts Halide [25], a domain-specific language for image processing applications, and proposes a modeling framework which is similar to that of [14]. MAESTRO [26] is the very first to adopt a data-centric approach.

### 3. THE PROPOSED DNN-CHIP PREDICTOR

This section presents the proposed DNN-Chip Predictor which is an analytical modelling framework to formulate DNN inference accelerators’ energy cost, latency, and throughput when employing different dataflows and hardware architectures. We first introduce the employed design space description method, and then describe the developed performance models. The advantages of the DNN-Chip Predictor are that it (1) matches well with actual implementation results (<18%); (2) is analytical and intuitive (directly ties to the DNN model and accelerator parameters), facilitating its ease of use for time-efficient design space exploration and optimization; and (3) is programmer friendly and compatible with commonly used DNN frameworks (e.g., Pytorch [27]) thanks to its adopted generic description of DNN accelerators’ design space.

#### 3.1. Design Space Description

For modeling DNN accelerators’ performance given their large design space, one critical question is how to describe the whole design space, i.e., cover all possible design choices, in a way that is easy to follow? For ease of use and better visualization, we adopt a nested for-loop description [14] to describe the design space as shown in Fig. 1. Specifically, we employ (1) the primitive, for, to describe the temporal operations of each process element (PE) as well as the temporal data tiling and mapping operations at the DRAM, global buffer (GB) and register file (RF) levels; and (2) the primitive, parallel-for, to describe the spatial data tiling and mapping operations at the network-on-chip (NoC) level (i.e., in the PE array). Without loss of generality, we consider four levels of memory hierarchy, i.e., off-chip DRAM, on-chip GB, NoC in the PE array, and RF within the PEs. The design space of DNN accelerators mainly includes two aspects: hardware architectures and dataflows.

**Hardware architecture.** It can be described using a set of architecture-dependent hardware parameters and technology-dependent IP parameters. In particular, the architecture-dependent hardware parameters includes PE array architecture (e.g., spatial array, systolic array, and adder tree), number of PEs, NoC design (e.g., unicast, multicast, or broadcast), memory hierarchies, and the storage capacity and communication bandwidth of each memory hierarchy; the technology-dependent IP parameters includes unit energy/delay costs of (1) a MAC operation, (2) memory accesses to various memory hierarchies, and (3) the clock frequency.

**Dataflow.** This describes how a DNN is temporally and spatially scheduled to be executed in an accelerator. Specifically, a dataflow answers the following questions: (1) how to map and schedule the computations in the PE array and within each PE?; and (2) what are the loop ordering and tiling factors on the DRAM and global buffer levels? The former captures the design choice of holding a certain type of data locally in the PE once being fetched from the memories, e.g., row/weight/output stationary. The latter shows how to store data in SRAM and DRAM to accommodate data stationary effectively. These two questions can be described using three groups of parameters as defined below in the context of the example in Fig. 1. Loop ordering factors for the twenty-four nested for-loops associated with the six dimensions of the 3D convolution operation and the four considered memory hierarchies (i.e., DRAM, GB, NoC, and RF); Loop tiling factors for the twenty-four nested for-loops associated with the six dimensions of the 3D convolution operation and the four considered memory hierarchies; and Data access locations in which of the nested for-loops we refresh the on-chip GB and in-PE RFs for the activations and weights.

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**Fig. 1:** A nested for-loop description of DNN accelerators’ design space, using a CONV layer as an example, where $0,1,2,3$ denotes the four memory hierarchies (i.e., RF, NoC, GB, and DRAM, respectively), and $M, C, R, S, E, F$ denote the six dimensions of a CONV layer (i.e., input/output feature maps, kernel width/height, and output feature map width/height, respectively).

```plaintext
1: // DRAM level
2: for ($m_3=0; m_3 < M_3; m_3++) {
3:   // Global buffer level
4:     ⇒ GB<weight> refresh
5:     ⇒ GB<input> refresh
6:     for ($c_2=0; c_2 < E_2; c_2++) {
7:       ⇒ GB<output> refresh
8:       for ($c_2=0; c_2 < C_2; c_2++) {
9:         // NoC level
10:        parallel-for ($f_1=0; f_1 < F_1; f_1++) {
11:          // RF level
12:            ⇒ RF<input> refresh, RF<weight> refresh
13:            for ($r_0=0; r_0 < R_0; r_0++) {
14:              for ($s_0=0; s_0 < S_0; s_0++) {
15:                MAC operation
16:                ⇒ RF<output> refresh }}
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3.2. The DNN-Chip Predictor

3.2.1. Overview

Fig. 2 shows a high-level view of the proposed DNN-Chip Predictor, which accepts DNN models (e.g., number of layers, layer structure, bit-precision, etc.), hardware architectures (e.g., memory hierarchy, number of PEs, NoC design, etc.), dataflows (e.g., row/weight/output stationary, loop tiling/ordering factors, etc.), and technology-dependent unit costs (e.g., unit energy/delay cost of a MAC operation and memory accesses to various memory hierarchies), and then outputs the estimated energy consumption, latency, and throughput when executing the DNN in a target accelerator. It can thus be used to (1) validate DNN accelerator techniques prior to the time- and cost-consuming DNN ASIC/FPGA accelerator implementation, and (2) perform time-efficient design space exploration and optimization.

3.2.2. The Proposed Analytical Models

This subsection introduces the Predictor’s analytical models.

Energy Models. DNN accelerators’ energy cost include both computational (Ecomp) and data movement (EDM) costs, where $E_{\text{comp}} = N_{\text{MAC}} \times \epsilon_{\text{MAC}}$ with $N_{\text{MAC}}$ denoting the total number of MACs in the DNN. Similarly, the data movement cost can be calculated by multiplying the unit energy cost per access ($\epsilon_{\text{DM}_{i,j}}$, $i \in \{I, O, W\}$) with the total number of accesses ($N_{\text{DM}_{i,j}}$, $i \in \{I, O, W\}$) to the $i$-th memory hierarchy (e.g., GB) using the $j$-th type of data (i.e., inputs (I), outputs (O), and weights (W)):

$$E_{\text{DM}} = \sum_{i \in \{I, O, W\}} \sum_{j \in \{I, O, W\}} N_{\text{DM}_{i,j}} \times \epsilon_{\text{DM}_{i,j}}$$

where $S_{\text{Memory}} = \{ \text{DRAM} \rightarrow GB, GB \rightarrow \text{NoC}, \text{NoC} \rightarrow RF, RF \rightarrow PE \}$ for inputs/weights; and $S_{\text{Memory}} = \{ \text{DRAM} \leftrightarrow GB, GB \leftrightarrow \text{NoC}, \text{NoC} \leftrightarrow RF, RF \leftrightarrow MAC \}$ for outputs.

The key challenge is to obtain $N_{\text{DM}_{i,j}}$ for various memory hierarchies and data types when using different DNN models, hardware architectures, and dataflows. We are the first to find that $N_{\text{DM}_{i,j}}$ can be calculated as the product of the $j$-th data volume ($V_{\text{ref}_{i,j}}$) involved in each refresh and the total number of such refreshes ($N_{\text{ref}_{i,j}}$) for the $i$-th memory:

$$N_{\text{DM}_{i,j}} = N_{\text{ref}_{i,j}} \times V_{\text{ref}_{i,j}}$$

To obtain $N_{\text{ref}_{i,j}}$ and $V_{\text{ref}_{i,j}}$, we propose an intuitive methodology: we first (1) choose a refresh location, which can be straightforwardly decided once the dataflow is known, in the nested for-loops (see Fig. 1) for a given data type; (2) $N_{\text{ref}_{i,j}}$ is equal to the product of all the loop bounds in the for-loops above the refresh location; and (3) $V_{\text{ref}_{i,j}}$ is equal to the product of all the loop bounds in the for-loops below the refresh location and associated with the particular type of data. Once $N_{\text{ref}_{i,j}}$ and $V_{\text{ref}_{i,j}}$ are obtained, the energy can be calculated as:

$$E_{\text{DRAM}} = \sum_{j \in \{I, O, W\}} N_{\text{ref}_{GB,j}} \times V_{\text{ref}_{GB,j}} \times \epsilon_{\text{DM}_{\text{DRAM},j}}$$

$$E_{\text{GB}} = \sum_{j \in \{I, O, W\}} N_{\text{ref}_{RF,j}} \times V_{\text{ref}_{RF,j}} \times \frac{N_{PE}}{M_j} \times \epsilon_{\text{DM}_{\text{GB},j}}$$

$$E_{\text{NoC}} = \sum_{j \in \{I, O, W\}} N_{\text{ref}_{RF,j}} \times V_{\text{ref}_{RF,j}} \times N_{PE} \times \epsilon_{\text{DM}_{\text{NoC},j}}$$

$$E_{\text{RF}} = \sum_{j \in \{I, O, W\}} N_{\text{MAC}} \times \epsilon_{\text{DM}_{\text{RF},j}}$$

where $N_{PE}$ is the number of active PEs and $M_j$ is the number of PEs that share the same data.

Latency Models. Similarly, the latency of DNN accelerators can be formulated as:

$$L = L_{\text{setup}} + \max \{ L_{\text{DRAM}}, L_{\text{GB}}, L_{\text{comp}} \}$$

where $L_{\text{comp}}, L_{\text{DRAM}}, L_{\text{GB}}$, and $L_{\text{setup}}$ denote the latency of computation in the PE array, accessing the DRAM from the GB, accessing the GB from an RF in the PEs, and setting up the first set of the weights and inputs, respectively. Adopting $N_{\text{bit}}$-bit precision for inputs/outputs/weights is $N_{\text{bit}}$, $j \in \{I, O, W\}$, we have:

$$L_{\text{comp}} = N_{\text{MAC}} \times t_{\text{comp}}$$

$$L_{\text{DRAM}} = \max_{j \in \{I, O, W\}} \frac{N_{\text{ref}_{GB,j}} \times V_{\text{ref}_{GB,j}} \times N_{\text{bit}}}{\min \{ BW_{\text{GB}}, BW_{\text{DRAM}} \}}$$

$$L_{\text{GB}} = \max_{j \in \{I, O, W\}} \frac{N_{\text{ref}_{RF,j}} \times V_{\text{ref}_{RF,j}} \times N_{\text{bit}} \times N_{PE}}{BW_{\text{GB}}^j}$$

$$L_{\text{setup}} = \max \{ L'_{\text{DRAM}}, L'_{\text{GB}} \}$$

$$L'_{\text{DRAM}} = \max_{j \in \{I, O, W\}} \frac{V_{\text{ref}_{GB,j}} \times N_{\text{bit}}}{\min \{ BW_{\text{GB},j}, BW_{\text{DRAM}} \}}$$

$$L'_{\text{GB}} = \max_{j \in \{I, O, W\}} \frac{N_{\text{ref}_{RF,j}} \times N_{\text{bit}}}{\min \{ BW_{\text{RF},j}, BW_{\text{GB},j} \}}$$

where $BW_{\text{GB}}^j$ is the memory bandwidth for the $i$-th memory hierarchy for the data type $j \in \{I, O, W\}$.

4. EXPERIMENT RESULTS

We validate our proposed DNN-Chip Predictor by comparing its predicted performance with actual chip measured ones in [14], FPGA implementation results in [28], and synthesis results based on a commercial CMOS technology, under the same experiment settings (e.g., unit energy, clock frequency, DNN model, architecture design and dataflow, etc).

Validation against Chip Measurements. For this set of experiments, we compare our Predictor’s predicted performance with Eyeriss’s chip measurement results using their
normalized unit energy \[14\]. First, Table 1 compares the energy breakdown of AlexNet’s first and fifth CONV layers (denoted as CONV1 and CONV5, respectively), showing that the maximum difference is 5.15% and 1.64%, respectively.

Second, Fig. 3 compares the number of DRAM/GB accesses. The difference between the predicted number of DRAM accesses and Eyeriss’s measured results is between 2.18% and 12.10%, while the difference in terms of GB accesses is between -0.70% and 17.66%. Our Predictor’s predicted DRAM access number is smaller than that of Eyeriss because the RLC overhead of sparse activations depends on the input images and we lack the information about which set of images were used in Eyeriss’s measurements. Additionally, Fig. 3 shows that the difference between the predicted number of GB accesses and Eyeriss’s results is less than 5% except for the CONV1 layer where the relative larger prediction error is caused by its larger stride, which is 4. Specifically, a larger stride leads to lower utilization of inputs fetched from the GB, whereas our current Predictor considers the generic case where stride is 1 as it is more often seen in recent DNN models. For better prediction accuracy, our Predictor can be adjusted to cover cases with other stride values, i.e., more considered cases for the analytical models in Section 3.2.2.

Third, Fig. 4 compares the latency of executing AlexNet’s five CONV layers, and shows that the predicted ones and Eyeriss’s differ by ≤ 15.51%. The predicted latency is smaller than the measured one because our Predictor’s analytical models do not consider the corner cycles when the memory accesses and computation cannot be fully pipelined where processing stalls occur. Finally, the predicted throughput of executing AlexNet is 46.0 GOPS while the one measured by Eyeriss is 51.6 GOPS, showing a prediction error of ≤ 11%.

Validation against FPGA Implementation. We compare our Predictor’s predicted latency with FPGA measured ones under the same DNN model and hardware configurations [31]. Specifically, for the FPGA one we use the open source implementation of the award winner [31] in a state-of-the-art design contest [32]. Fig. 5 shows that our Predictor’s predicted latency differs from the FPGA-synthesized ones by ≤ 16.84%. Note that in FPGA implementations the GB can be partitioned into smaller chunks to be accessed simultaneously for increasing the parallelism and minimizing the latency. Our current models do not include the overhead of this partition, which is larger when the GB is partitioned into more chunks for layers with a larger size, leading to a larger prediction error for the CONV4/CONV5/CONV6 layers in Fig. 5.

Validation against Synthesis Results. Table 2 compares our Predictor’s energy breakdown with that from the synthesis results for AlexNet’s CONV3-CONV5 layers when using an in-house dedicated accelerator using a commercial 65nm CMOS technology. It can be seen from Table 2 that the difference between our Predictor’s predicted energy breakdown and that from the synthesis results is less than 5.28%.

5. CONCLUSION

To close the gap between the growing demand for dedicated DNN accelerators with various specifications and the time-consuming and challenging DNN accelerator design, we develop DNN-Chip Predictor, which can efficiently and effectively predict an accelerator’s energy, latency, and resource consumption. Such an analytical performance prediction tool will facilitate fast development of innovations for not only DNN accelerators but also hardware-aware efficient DNNs.
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