Practice of power electronic hardware loop simulation based on fpga

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Abstract. To develop and design the power electric hardware, the hardware-in-the-loop simulation system suitable for power electronics is carried out. An architecture of hardware-in-the-loop simulation system in power electronic based on multi field-programmable gate array (FPGA) is presented. The functional modules of the hardware-in-the-loop simulation system are independent, and different functional boards are formed to facilitate the system expansion. The full hardware FPGA architecture is adopted, and multi-chip FPGA is used as the parallel core operation unit. Therefore, the system simulation capacity is effectively increased. At the same time, the simulation step is shortened, and the simulation precision of the system is ensured. In addition, the hardware-in-the-loop simulation platform based on multi FPGA is built. The external controller and the hardware-in-the-loop simulation platform are connected to realize the closed-loop simulation control of the hardware in the 10kV STATCOM. The experimental results show that the system can take a long and stable hardware-in-the-loop simulation for the power electronic devices with ideal condition and non-ideal condition. The controller can be directly applied to the actual platform by the hardware-in-the-loop-simulation.

Key words: hardware-in-the-loop-simulation; power electronic; multi FPGA system; module independence.

1. Introduction

The development and design of power electronic devices will generally be simulated in advance. The traditional method is to use software simulation. With the improvement of power and electronic devices, the demand for the authenticity of the simulation is becoming higher and higher by the R & D engineers. Moreover, the fierce competition in the current market requires that the development time of the product must be short enough. As a result, the defects of software simulation are gradually exposed [1].

In the development and design of power electronic products, it is often required to carry out full simulation and verification in advance. There are two kinds of simulation verification methods: One is software simulation and the other is hardware in the loop simulation [2]. In response to the simulation of large power electronic devices, the defects of long simulation time and low accuracy are gradually revealed. The hardware in the loop simulation is a real-time simulation technology, which has been widely used in the fields of automobile, aviation and power systems. In the field of power electronics, the hardware in the loop simulation can accelerate the development of complex power electronic devices
and shorten the development cycle of the devices. Some of the faults which are difficult to be simulated can be simulated safely and conveniently through the hardware in the loop simulation system and are used to examine the response of the control system to the fault [3]. However, many high-speed switching devices, such as IGBT, require that the step size of the power electronics must be small enough. Therefore, the realization of high precision power electronic hardware in the loop simulation becomes very difficult.

The commercial power electronics hardware in the loop system is monopolized by foreign companies. The price is expensive, while the simulation capacity and the interface are also limited. The capacity expansion of the system is often involved when verifying the large power electronic devices. However, its proprietary communication protocols are not open to the outside world, resulting in system upgrading and high maintenance cost. Other open source hardware in the loop simulation systems in foreign serve only internal laboratories or certain specific projects. The reusability of the system is very low and the generality is poor. Thus, it is easy to cause resource waste [4].

Compared with foreign countries, there are few researches on hardware in the loop simulation in China. What's more, all kinds of hardware in the loop simulation systems developed in China are mostly based on others' hardware devices. They only develop specific software systems [5]. Therefore, in view of the demand for hardware in the loop simulation system in power electronics field, we have developed a set of hardware in the loop simulation platform with good real-time performance, high simulation accuracy, large capacity, low price and good universality. Based on this research background, a research on the hardware in the loop simulation system suitable for power electronics is carried out. How to design a set of power electronic hardware in the loop simulation platform with high simulation precision, low cost, large capacity and good generality is studied centrally.

2. Hardware in the loop simulation system based on multi FPGA

2.1. Overall architecture of the power electronics hardware in the loop simulation system

At present, there are many examples of the hardware in the loop simulation system in both business and academics. However, most of the hardware in the loop simulation system cannot meet the simulation requirements of good power electronic generality, large capacity, small step and high real time.

Generally, there are 4 kinds of IO interfaces between the power electronic main circuit and the control circuit, which are analog input, analog output, digital input and digital output interface. Between the actual device and the hardware in the loop simulation system, the data exchange is carried out through these IO interfaces. Therefore, the design of the hardware architecture of the real-time simulation system is mainly the design of the IO interface module and the simulation calculation module. The larger the capacity of the simulation module is, the richer the interface resource is, then the wider the application of the corresponding hardware in the loop simulation system is [6].

In order to increase the number of all kinds of interfaces and facilitate the expansion of modules and systems, all interface modules and simulation modules are designed into an independent board card structure. The analog input (A/D) card, analog output (D/A) card, digital input (DI) card, digital output (DO) card and core computing board (FPGA card) are formed respectively. The data calculation, storage and communication of each card are realized by FPGA. Among them, the communication interface is integrated in the FPGA card. The calculated data can be exported to the PC machine through the communication interface according to the corresponding requirements. At the same time, the external instructions can be sent to the FPGA card. A hardware in the loop simulation system consists of a backplane, 4 FPGA core computing boards, 2 A/D boards, 2 D/A boards, 2 DI cards and 2 DO cards. When a set of system capacity is not enough, the capacity of the whole system can be expanded to achieve greater capacity simulation. The architecture has greater flexibility, but it requires a higher rate of data communication between boards [7].

All cards are connected through the backboard, and the data management and communication of each card are implemented by FPGA. The design framework maximizes the number of interfaces and greatly facilitates the expansion of the functional interface modules and even the system. The FPGA
card and the interface board are all transmitted by the enhanced SPI communication protocol. When the capacity of the simulation is insufficient and the FPGA card needs to be expanded, the data transfer between the FPGA cards adopts the high speed LVDS communication protocol.

2.2. Analysis of key points in the design of multi FPGA system
In order to make up for the defects of the single FPGA capacity and the high price, a multi FPGA and module independent architecture is selected. A rich communication link on a development board can often increase the rate of data communication. The demand for communication networks varies with different circuits. A good communication network can effectively reduce communication complexity. The main FPGA board has a high demand for communication. The selection of cascaded topology forms is a key factor in the design of the main FPGA simulation board.

Multi FPGA is widely used in the system on chip and network on chip. There are many interconnected topology structures in the multi FPGA cascade, which can be divided into two types: fixed connection network and programmable cross switch [8]. Based on the architecture of the hardware in the loop simulation system designed in this paper, a star symmetric interconnection structure is designed as the interconnection topology of the main FPGA simulation board. The system uses 5 FPGA cascades to meet the needs of the vast majority of complex power electronics for real time simulation resources. Among them, there is no hardware connection between Slave1 FPGA and Slave4 FPGA, which is convenient for the intermediate Master FPGA out of line. The existence of central FPGA plays three roles: First, it acts as a medium of information exchange between the various FPGA in the board. Second, when the single block FPGA card resource is still insufficient, it is used for data communication between the extended FPGA simulation cards. Third, it is convenient for the layout and wiring of the PCB board and avoids the intersecting between the diagonal FPGA.

In the FPGA development software Quartus II of Altera company, there is a free LVDS communication IP core for use. This facilitates the serial and conversions of communication data and the operation of data transmission. The phase-locked loop (PLL) module in Quartus software can also be transferred through the IP core. The internal parameters can be adjusted online according to the actual effect, and the phase modulation of LVDS communication can be realized quickly. These self-contained IP cores greatly shorten the development time of LVDS communications [9]. The total length of the board space between the hardware in the hardware simulation system will not exceed 1 meters. The two FPGA cards contain 8 pairs of independent LVDS interfaces. 4 pairs are used for receiving, and other 4 pairs are used for sending. These correspond to the communication bandwidth of 3200Mbps and meet the communication bandwidth requirements when the simulation step is 2us.

In order to reduce the complexity of PCB circuit design, all LVDS communication interfaces are designed with the True LVDS interface within FPGA.

2.3. Implementation and performance analysis of multi FPGA hardware in the loop simulation system
In the current market, 90% of FPGA are from both Altera and Xilinx companies, and the FPGA of the two companies mainly uses the SRAM process. Based on the lookup table technology, the FPGA product is divided according to the different application areas. It can be divided into two types: high performance type and high density type [10]. The hardware in the loop simulation system designed in this paper is still in the primary stage, which is mainly aimed at the general application. In the aspect of high cost performance, the development and design of the hardware in the loop simulation system of FPGA in Altera company is adopted. In this system, all functional modules needed in the hardware in the loop simulation are independent, and different functional boards are formed. There is an independent hardware connection between the different functional boards and the FPGA simulation cards. The same type of functional board takes up the same bus when it is enlarged. On the premise of satisfying the bandwidth of data transmission between boards, the more the number of interfaces in a single block interface card is better. Therefore, the FPGA with small capacity and multiple IO ports is the best choice for the interface board control chip.
In the early stage of the project development, the JTAG online configuration is generally used to verify the program. The systems constructed with multi FPGA interconnection will face a large number of cross network marking problems. Especially in the design stage, the FPGA with BGA dense packaging technology is adopted. It is almost impossible to manually adjust all the cross-connected pins. The dynamic network redistribution function of Altium Designer software and the features of FPGA free exchange of IO pins are used. Therefore, the design of the FPGA core computing board without cross interconnected PCB is realized, which greatly reduces the time consuming of manually adjusting the FPGA I/O interface network label in the multi-pin FPGA project.

Due to the use of FPGA chips, there must be 3.3V, 2.5V and 1.2V power supply. The capacity of EP4CE6F17C8 and the number of IO ports are not much. TI's LM1117-3.3V, LM1117-2.5V and LM1117-1.2V can provide 0.8A current to meet the demand for FPGA power supply.

Like the A/D chip, the D/A board uses a AD7244 dual channel digital analog conversion (D/A) chip provided by AD company. The conversion rate is 250ksps and the conversion precision is 14 bits. The single block card contains 16 D/A chips and a total of 32 analog-to-digital conversion channels. In order to meet the post level observation and sampling requirements, the output signal of the D/A output signal is output after the conditioning circuit, and the output voltage range is up to ±9V.

The design standard of the DO board is the same as the DI card. In this study, a single block DO card contains 112 channels digital signal output. The FPGA in the DO card receives the data from the FPGA simulation card through the enhanced SPI bus. After passing the level conversion module, 3.3V is converted to 5V level, and it is divided into 14 groups. Each group has 8 cards and contains 8 digital signals. Finally, it is output when the electrical safety is ensured by isolation module.

3. Experimental verification and waveform analysis

Based on the experimental point, taking the 10kV static synchronous compensator as an example, the simulation model and the actual controller are compiled. The waveform diagrams of hardware in the loop simulation under ideal and non-ideal conditions are provided respectively. In addition, the waveform diagrams are compared with the Matlab simulation waveforms to verify the correctness of theoretical analysis.

3.1. Experimental parameter

In order to verify the feasibility of the real-time simulation system, the experimental verification machine of 10kV STATCOM is built and compared with Matlab simulation results. Table 1 is the 10kV STATCOM related circuit parameters designed in this paper.

| Circuit parameter                                      | value   |
|--------------------------------------------------------|---------|
| Line voltage of power grid                             | 10kV    |
| Inductance                                             | 30mH    |
| Capacitance                                            | 1mF     |
| Maximum reactive current compensation (peak value)     | 100A    |
| MMC submodule DC side voltage                           | 800V    |
| MMC submodule numbers                                   | 12      |

In the test, the circuit model of 10kV STATCOM is loaded into the FPGA core computing board. The external controller sends the state control signal such as the PWM control signal and the contactor through the DI board. The DI card sends the received data to the model input interface of the FPGA core computing board. The internal model begins with the hardware in the loop simulation. The data calculated by the simulation model is transmitted to the D/A board and the DO card through the FPGA card. The external controller realizes the closed loop control of the simulation model by sampling the analog signal output from the D/A and receiving the digital feedback signal from the DO card. The prototype built on the basis of the above principles is shown in figure 1.
3.2. Experimental results and analysis

In the hardware in the loop simulation system, there are new data updates for each simulation step. It is almost impossible to derive the calculated data in real time under the simulation step of 2us. The system first stores the data calculated by FPGA in FIFO, then exports the calculated data through the Virtual JTAG IP core module of FPGA, and shows it through Matlab.

Figure 3 and Figure 4 compare the waveform of the steady-state output 100A reactive current of the 10k V STATCOM under two simulated closed loop controls. Figure 3 is a Matlab simulation waveform. Figure 4 is a waveform diagram for the D/A output of the hardware in the loop simulation system. Uca represents the DC side capacitance voltage of a single MMC sub module. ia represents the charging current of the A phase power grid in pre-charge. Ug_ab represents the AB phase voltage, and the compensated phase current is 90° in advance phase voltage. That is, when the line voltage is 60° in advance, the simulation waveform in the diagram is in accordance with the theoretical analysis. At the same time, the small error to system output is adjusted when the accuracy of the D/A card conversion and the extension of the hardware circuit are ignored. The simulation waveforms in the two simulation methods are basically the same.
Fig. 3 Waveform diagram of the hardware in the loop simulation

The point output voltage waveform of the three-phase bridge arm in 10k V STATCOM steady state under the closed loop control of two simulation modes is compared. Among them, the hardware in the loop simulation waveform is output by the D/A board with its own system. The simulation waveform is consistent with the theoretical analysis, and the consistency between Matlab and hardware in the loop simulation fully verifies the normal operation of the hardware in the loop simulation system and the testing function of the controller.

4. Conclusion

The main content of this paper is to design a hardware in the loop simulation system for complex power electronics application, aiming to solve the problems of limited intellectual property rights, high cost, large simulation step and insufficient resources. First, the advantages and disadvantages of the current hardware in the loop simulation system are compared and analyzed, and the architecture of modular multi FPGA hardware in the loop simulation system is studied. Then, the key problems such as simulation step, communication structure, communication demand of multi FPGA hardware in the loop simulation system are studied, and a specific design is provided. Finally, the circuit model of 10k V STATCOM is set up, and the experimental verification for the hardware in the loop simulation system is carried out with the external controller. The experimental results verify the correctness and feasibility of the multi FPGA power electronic hardware in the loop simulation system designed in this paper.

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