Efficient Realization of Householder Transform through Algorithm-Architecture Co-design for Acceleration of QR Factorization
Farhad Merchant, Tarun Vatwani, Anupam Chattopadhyay, Senior Member, IEEE, S K Nandy, Senior Member, IEEE, and Ranjani Narayan

Abstract—QR factorization is a ubiquitous operation in many engineering and scientific applications. In this paper, we present efficient realization of Householder Transform (HT) based QR factorization through algorithm-architecture co-design where we achieve performance improvement of 3-90x in-terms of Gflops/watt over state-of-the-art multicore, General Purpose Graphics Processing Units (GPGPUs), Field Programmable Gate Arrays (FPGAs), and ClearSpeed CSX700. Theoretical and experimental analysis of classical HT is performed for opportunities to exhibit higher degree of parallelism where parallelism is quantified as a number of parallel operations per level in the Directed Acyclic Graph (DAG) of the transform. Based on theoretical analysis of classical HT, an opportunity re-arrange computations in the classical HT is identified that results in Modified HT (MHT) where it is shown that MHT exhibits 1.33x times higher parallelism than classical HT. Experiments in off-the-shelf multicore and General Purpose Graphics Processing Units (GPGPUs) for HT and MHT suggest that MHT is capable of achieving slightly better or equal performance compared to classical HT based QR factorization realizations in the optimized software packages for Dense Linear Algebra (DLA). We implement MHT on a customized platform for Dense Linear Algebra (DLA) and show that MHT achieves 1.3x better performance than native implementation of classical HT on the same accelerator. For custom realization of HT and MHT based QR factorization, we also identify macro operations in the DAGs of HT and MHT that are realized on a Reconfigurable Data-path (RDP). We also observe that due to re-arrangement in the computations in MHT, custom realization of MHT is capable of achieving 12% better performance improvement over multicore and GPGPUs than the performance improvement reported by General Matrix Multiplication (GEMM) over highly tuned DLA software packages for multicore and GPGPUs which is counter-intuitive.

Index Terms—Parallel computing, dense linear algebra, multiprocessor system-on-chip, instruction level parallelism

1 INTRODUCTION
QR factorization plays pivotal role in computing solution of linear systems of equation, solving linear least square problems, and computing eigenvalues. Such problems arise in navigation to wireless communication systems. For a matrix \( A \) of size \( m \times n \), QR factorization is given by

\[
A = QR
\]

where \( Q \) is \( m \times m \) orthogonal and \( R \) is \( m \times n \) upper triangle matrix [1]. There are several methods in the literature to perform QR factorization namely Givens Rotation (GR), Householder Transform (HT), Modified Gram-Schmidt (MGS), and Cholesky QR. Following are the two real life application examples, Kalman Filtering (KF) and QR algorithm where QR factorization is used as a tool to solve certain computational problems.

Application 1: Kalman Filtering
KF is used in navigation to econometrics since it is capable of filtering out noisy data and at the same time it also facilitates prediction of the next state. A simplistic multi-dimensional KF is shown in the figure [1]. In the KF there is an initial state that contains state matrix and process co-variance matrix. Based on the current state and the previous state, next state is predicted as shown in the figure [1]. Based on the predicted state and co-variance matrix, and measured input, Kalman Gain (KG) is computed and KG is used to predict the next state. Using KG and the predicted state, error in the process is computed. A new state matrix and co-variance matrices are output of the iteration that becomes previous state for the next iteration.

![Fig. 1: Multi Dimensional Kalman Filter](image_url)

An iteration of KF requires complex matrix operations ranging from matrix multiplication to computation of numerical stable matrix inverse. One such classical GR based numerical stable approach is presented in [2]. From figure [1] matrix inverse being
the most complex operation in KF, and computation of inverse using QR factorization being a numerical stable process, proposed library based approach is the most suitable for such applications.

Application 2: Eigenvalue Computation

Algorithm 1 QR Algorithm

1: Let \( A^{(0)} = A \)
2: for \( K = 1,2,3... \) do
3: \( \text{Obtain the factors } Q^{(k)} R^{(k)} = A^{(k-1)} \)
4: \( \text{Let } A^{(k)} = R^{(k)} Q^{(k)} \)
5: end for

Computation of eigenvalues is simplified due to QR algorithm where QR algorithm is based on the QR factorization given in equation 1. Eigenvalue computation is shown in the algorithm 1. As a result of QR iteration, eigenvalues appear on the diagonal of the matrix \( A \) while columns of the matrix \( Q \) are the eigenvectors. QR algorithm has gained immense popularity for computing eigenvalues and eigenvectors. Some of the examples where eigenvalues and eigenvectors are useful are in communication where eigenvalues and eigenvectors are computed to determine the theoretical limit of the communication medium for the transfer of the information, dimensionality reduction in the principle component analysis for face recognition, and graph clustering. Considering important engineering and scientific applications of QR factorization, it is momentous to accelerate QR factorization. Traditionally, for scalable realization of QR factorization, library based approach is favored due to modularity and efficiency. Graphical representations of HT based QR factorization (XGEQR2) and HT based block QR factorization (XGEQRF) routines in Linear Algebra Package (LAPACK) are shown in figure 2 where X stands for double/single precision version of the routine. It can be observed in the figure 2 that the routine XGEQR2 is dominated by General Matrix-vector (XGEMV) operations while XGEQRF is dominated by General Matrix-matrix (XGEMM) operations. Performance of XGEQR2 is observed to be magnitude higher than XGEQRF due to highly optimized XGEMM operations. XGEMV and XGEMM are part of Basic Linear Algebra Subprograms (BLAS). Typically, performance of LAPACK routines can be measured as a relative performance of BLAS XGEMM since in routines like XGEQRF (QR factorization), XGETRF (LU factorization with partial pivoting), and XPBTRF (Cholesky factorization), XGEMM is dominant and the performance achieved is usually 80% of the performance achieved by XGEMM for the underlying platform.

Algorithm 1

Contemporary multicore and General Purpose Graphics Processing Units (GPGPUs) are considered as an ideal platform for efficient realization of BLAS and LAPACK. Multicores are optimized for sequential programs and they are highly efficient in exploiting temporal parallelism exhibited by the routines while GPGPUs are more suitable for the routines that exhibit spatial parallelism. Experimentally, none of these platforms are capable of exploiting parallelism that is exhibited by the BLAS and LAPACK routines very efficiently. Moreover, routines in BLAS and LAPACK can be further examined for attaining higher degree of parallelism. We quantify parallelism by depicting routines as a Directed Acyclic Graphs (DAGs) and average number of operation per level (\( \beta \)) in the DAGs is considered as a measure for fine-grained parallelism exhibited by the routine. Higher \( \beta \) means more parallelism in the routine.

For exploiting spatio-temporal parallelism in BLAS and LAPACK, domain specific customizations are recommended in the platform that is executing these routines. We choose REDEFINE as a platform for our experiments. REDEFINE is a Coarse-grained Reconfigurable Architecture (CGRA) in which several Tiles are connected through a Network-on-Chip (NoC). Each Tile contains a router for communication and a Compute Element (CE). CEs in REDEFINE can be enhanced with Custom Function Units (CFUs) specifically tailored for domain of interest. CFUs can be Application Specific Integrated Circuits (ASICs), Reconfigurable Data-path (RDP), and micro/macro reprogrammable units. In the present approach we rearrange computations in LAPACK routines vis-à-vis amend CFU presented in [19] that can efficiently exploit parallelism exhibited by the modified routine. Thus our approach becomes algorithm-architecture co-design. Considering importance of QR factorization in scientific computing, in this paper we focus on efficient realization of HT based QR factorization through algorithm-architecture co-design. Contributions in this paper are as follows:

- Firstly, we discuss evaluation of routines of BLAS and LAPACK on Intel multicore processors and Nvidia GPGPUs. We identify limitations of these machines in exploiting parallelism exhibited by the routines. It is shown that even with highly optimized Dense Linear Algebra (DLA) software packages, the contemporary multicore and GPGPUs are capable of achieving only 0.2-0.3 Gflops/watt.
- XGEQR2 routine of LAPACK that computes HT based QR factorization is revisited where it is identified that the computations in the classical HT can be re-arranged to exhibit higher degree of parallelism that results in Modified HT (MHT). Empirically, it is shown that realization of MHT (DGEQR2HT) achieves better performance than realization of classical HT (DGEQR2) and better or similar performance compared to DGEQRF in LAPACK while through quantification of parallelism, theoretically it is shown that the parallelism available in the MHT is higher than that of exploited by contemporary multicore and GPGPUs. Realization of MHT on multicore and GPGPU is presented and compared with the state-of-the-art tuned software packages for DLA. Source code of our implementation on multicore and GPGPU is supplied with the exposition.
- To exploit available parallelism in MHT, we realize MHT on Processing Element (PE) presented in [19]. We adopt methodology presented in [20] and identify macro operations in DAGs of MHT that can be realized on RDP resulting in 1.2-1.3x performance improvement over classical

Fig. 2: DGEQR2 and DGEQRF Routines
HT realization on the PE. MHT is capable of achieving 99.3% of the theoretical peak performance achieved by DGEMM in the PE shown in figure [4(c)] which is counter-intuitive as for multicore and GPGPU, the performance achieved by DGEQRF is mostly 80-85% of the performance achieved by DGEMM.

- Compared to multicore, GPGPU, and ClearSpeed CSX700, 3-80x performance improvement in terms of Gflops/watt is attained. Realization of MHT, outperforms realization of DGEMM as shown in figure [4(d)]. We also show scalability of our solution by attaching PE as a CFU in REDEFINE.

Due to availability of double precision floating point arithmetic units like adder, multiplier, square root, and divider, we emphasize on the realization of DGEQR2, and DGEQRF using HT and MHT [21][22]. Organization of the paper is as follows: In section 2, we briefly discuss about REDEFINE and some of the recent realization of QR factorization. In section 3, case studies of DGEMM, DGEQR2, and DGEQRF is presented and limitations of the recent multicore and GPGPU in exploiting parallelism are identified. In section 4, HT is revisited and MHT is presented. In section 5, custom realization of HT and MHT on multicore and GPGPU is presented. Parallel realization of MHT on multicore and GPGPU is presented. We summarize our work in section 6.

**Nomenclature:**

BLAS_DGEMM: Legacy realization of DGEMM

LAPACK_DGEQR2: Legacy realization of HT based block QR factorization

LAPACK_DGEQRF: Legacy realization of HT based block QR factorization

LAPACK_DGEQR2HT: Realization of MHT based block QR factorization

PLASMA_DGEQR2: Legacy realization of HT based block QR factorization

PLASMA_DGEQRF: Legacy realization of HT based block/tile QR factorization

MAGMA_DGEQRF: Legacy realization of HT based block/tile QR factorization

MAGMA_DGEQR2HT: Realization of MHT based block/tile QR factorization

MAGMA_DGEQRFHT: Realization of MHT based block/tile QR factorization

**2 BACKGROUND AND RELATED WORK**

We revisit REDEFINE micro-architecture briefly and discuss performance of some of the recent DLA computations realized on REDEFINE. Classical HT and its WY representation of HT is also discussed. In the latter part of the section, we discuss some of the recent realization of QR factorization in the literature and their shortcomings.

**2.1 REDEFINE and DLA on REDEFINE**

A system level diagram of REDEFINE is shown in figure 3 where a PE designed for efficient realization of DLA is attached. Micro-architecture of the PE is depicted in figure 4.

The PE is taken through several architectural enhancements to improve the performance of the PE and also to ensure maximal overlap of computations and communication [19]. Performance variations in the PE due to architectural enhancements is shown in figure 5(a) while change in the performance in terms of Gflops/watt due to each enhancement is depicted in figure 5(b). Further details of PE can be found in [19], and [24]. Due to unique features of PE and REDEFINE, we choose PE for our methodology of algorithm-architecture co-design for HT. It can be observed in figure 5(c) that the PE achieves almost 3-140x performance improvement over some of the commercially available multicore, FPGA, and GPGPUs for DGEMM [23]. It is also shown in [23] that when PE used as a CFU in REDEFINE, facilitates scalable parallel realization of BLAS.

**2.2 Classical HT**

In this section, we briefly explain HT and its WY representation. Householder matrix for annihilation of $m - 1$ elements in a matrix $A$ of size $m \times n$ is given by

$$P_{m \times m} = I_{m \times m} - 2v_{m \times 1}v_{m \times 1}^T$$

where $P$ is orthogonal (for real matrices, and Hermitian for complex matrices) and $v$ is householder vector.

Computations steps for computing householder vector are as follows for matrix $A = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix}$:

$$\alpha = -sign(a_{21}) \sqrt{\sum_{j=1}^{3} a_{j1}^2}$$

$$r = \sqrt{\frac{1}{2}(\alpha^2 - a_{11}^2)}$$

From $\alpha$ and $r$, we can compute $v$ as follows:

$$v = \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}$$

where $v_1 = \frac{a_{11} - r}{r}$, $v_2 = \frac{a_{21}}{r}$, and $v_3 = \frac{a_{31}}{r}$. From $v$ vector, $P$ can be computed that annihilates $a_{21}$, and $a_{31}$. $P$ matrix is then multiplied with second and third columns of $A$. In the next iterations, similar procedure is followed to annihilate updated $a_{21}$ and $a_{31}$.
DGEQR2 was the first implementation that was dominated by previous iteration. Directed Acyclic Graphs (DAGs) for annihilation of \( a_{31} \) and \( a_{21} \) are shown in figure 6.

It can be observed in the figure 6 that there exist minimal parallelism in computation of \( v \) vector. Major source of parallelism is matrix-vector operations and matrix-matrix operations encountered in computation of \( P \) matrices. As per Amdahl’s law, the performance of the routine is limited by the piece of program that can not be parallelized that is computation of \( v \) vectors [25].

### 2.3 Related Work

HT was first presented in [26] by Alston S. Householder in 1958 that showed significant improvement in terms of computations over classical Givens Rotation (GR). Since then there were several innovations at algorithmic and technology level that prompted different styles of realizations for HT proposed in [26]. First breakthrough arrived with advent of efficient processors with memory hierarchy that induced innovation in efficient realization of Level-3 BLAS [27]. Considering efficiency of Level-3 BLAS in the processors at that juncture, there was a successful attempt to realize higher level routines in terms of Level-3 operations. This attempt gave rise to LAPACK, a successor of LINPACK that uses matrix-matrix operations as a basic building block for realization of routines like LU, QR, and Cholesky factorizations [6]. Simultaneously, there was an innovation in HT that resulted in WY-representation of HT presented in [28]. The WY-representation proposed in [28] is storage efficient and exploits memory hierarchy of the underlying platform more efficiently due to heavy use of Level-3 BLAS operations at comparable operations to its predecessor proposal in [29]. Since then WY-representation of HT is preferred due to its computational density and over the years there have been several realizations of HT on contemporary platforms like multicore, GPGPUs, and FPGAs.

LAPACK DGEQR2 was the first implementation that was dominant in matrix-vector operations (also depicted in figure 2) while improved version of LAPACK DGEQR2 is LAPACK_DGEQRF that performs block QR factorization based on HT rich in matrix-matrix operations.

In the recent years, with advent of multicore and GPGPUs, two major packages are developed namely Parallel Linear Algebra Software for Multicore Architectures (PLASMA) for multicore architectures and Matrix Algebra for GPU and Multicore Architectures (MAGMA) for heterogeneous computing environment [7][30]. Corresponding routine realized in PLASMA is PLASMA_DGEQRF that uses LAPACK_DGEQR2 and BLAS_DGEMM along with Queuing and Runtime for Kernels (QUARK) for efficient realization of HT based QR factorization on multicore platforms [31]. Similarly, MAGMA uses efficiently realized MAGMA_BLAS and MAGMA_DGEQRF for realization of MAGMA_DGEQRF. Software stacks of PLASMA and MAGMA are explained in section 4.1. There have been several attempts for scalable parallel realization of HT based QR factorization on FPGAs [32][33]. The approach presented in [33] is a multicore based approach emulated on FPGA while LAPACKrc presented in [32] is a scalable parallel realization of LU, QR and Cholesky factorizations, FPGA based realizations clearly outperform multicore and GPGPU based realizations. A major drawback of FPGA based realization is the energy efficiency of the final solution. It is shown in [23] that CFU tailored for DLA computations clearly outperforms multicore-, GPGPU, and FPGA based solutions and is an ideal platform for our experiments. Surprisingly, multicore, GPGPU, and FPGA based solutions for HT based QR factorization dwell on efficient exploitation of memory hierarchy but none of them focus on rearrangement of computations to expose higher degree of parallelism in HT. In this paper, we present modification to classical HT where we maintain same computation count and memory access of classical HT. We also realize proposed MHT in PLASMA and MAGMA and show marginal improvement in multicore and no improvement in GPGPU.
3 CASE STUDIES

We present case study on different available realizations of DGEMM, DGEQR2, and DGEQRF in LAPACK, PLASMA, and MAGMA, and discuss results on multicore and GPGPU platforms.

3.1 DGEQR2

Algorithm 2 Pseudo code of DGEQR2

1: Allocate memory for input matrix
2: for $i = 1$ to $n$ do
3: Compute Householder vector $v$
4: Compute $P$ where $P = I - 2vv^T$
5: Update trailing matrix using DGEMV
6: end for

Pseudo code of DGEQR2 is described in algorithm 2. It can be observed in the pseudo code in the algorithm that, it contains three steps, 1) computation of a householder vector for each column 2) computation of householder matrix $P$, and 3) update of trailing matrix using $P = I - 2vv^T$ (from equation 2). Cycles-per-Instruction (CPI) attained for LAPACK_DGEQR2 executed on commercially available micro-architectures is shown in figure 7(a). For our experiments, we use Intel C Compiler (ICC) and Intel Fortran Compiler (IFORT). We also use different compiler switches to improve the performance of LAPACK_DGEQR2 on Intel micro-architectures. It can be observed in the figure 7(a) that in Intel Core i7 4th Gen machine which is a Haswell micro-architecture, CPI attained saturates at 1.1. It can be observed in figure 7(b) that attained Gflops saturates at 3 Gflops. Similarly, it can be observed that the percentage of peak performance saturates at 7-8% of the peak performance in case of Intel Haswell micro-architectures as observed in figure 7(d). In case when compiler switch $-maxx$ is used that enables use of Advanced Vector Extensions (AVX) instructions, the CPI attained is increased. This behavior is due to AVX instructions that use Fused Multiply Add (FMA). Due to this fact, the CPI reported by VTune™can not be considered as a measure of performance for the algorithms and hence we accordingly double the instruction count reported by VTune™.

In case of GPGPUs, MAGMA_DGEQR2 is able to achieve up to 16 Gflops in Tesla C2050 which is 3.1% of the theoretical peak performance of Tesla C2050 while performance in terms of Gflops/watt is as low as 0.04 Gflops/watt.

3.2 DGEMM

Pseudo code for BLAS_DGEMM routine in BLAS is shown in algorithm 3. It can be observed in the algorithm that DGEMM has three nested loops in the algorithm. DGEMM is Level-3 BLAS and it has applications in realization of block algorithms in the DLA software packages since computations in DGEMM are regular in nature and easy to parallelize. CPI attained in BLAS_DGEMM is 0.37 as shown in figure 7(a) for Intel Haswell micro-architectures. We have used Netlib BLAS for our experiments with platform specific compiler and all the compiler optimizations enabled. BLAS_DGEMM is able to achieve up to 8.5 Gflops in Intel Haswell micro-architectures with all optimizations as shown in figure 7(b) which is 17% of the theoretical peak performance of the micro architecture as depicted in figure 7(d). In case of GPGPU, MAGMA_DGEMM is able to achieve up to 295 Gflops in Nvidia Tesla C2050 which is 57% of the peak performance as shown in the figures 7(c) and figure 7(d) respectively. In-terms of Gflops/watt, LAPACK_DGEMM is capable of attaining 0.12 Gflops/watt in Intel Haswell micro-architecture while for Tesla C2050, it is 1.21 Gflops/watt in MAGMA_DGEMM.

Algorithm 3 Pseudo code of DGEMM

1: Allocate memories for input and output matrices and initialize input matrices
2: for $i = 1$ to $m$ do
3: Compute Householder vectors for block column $m \times k$
4: Compute $P$ matrix where $P$ is Computed using Householder vectors
5: Update trailing matrix using DGEMM
6: end for

Pseudo code for DGEQRF routine is shown in algorithm 4. In terms of computations, there is no difference between algorithms and 3. In a single core implementation, LAPACK_DGEQRF is observed to be 2-3x faster than LAPACK_DGEQR2. The major source of efficiency in LAPACK_DGEQRF is efficient utilization of processor memory hierarchy and BLAS_DGEMM routine which is a compute bound operation. CPI attained in LAPACK_DGEQRF is 0.43 as shown in figure 7(a) which is much lower than the CPI attained by LAPACK_DGEQR2. In-terms of Gflops, LAPACK_DGEQRF is 2-3x better than LAPACK_DGEQR2 as shown in figure 7(b) while the performance attained by LAPACK_DGEQRF is 85% of the performance attained by LAPACK_DGEMM. LAPACK_DGEQRF achieves 6-7 Gflops in Intel Haswell micro-architecture as shown in figure 7(b). In Nvidia Tesla C2050, MAGMA_DGEQRF is able to achieve up to 265 Gflops as shown in figure 7(c) which is 51.4% of the theoretical peak performance of Nvidia Tesla C2050 as shown in the figure 7(d) which is 90.5% of the performance attained by MAGMA_DGEMM. In MAGMA_DGEQR2, performance attained in terms of Gflops/watt is as low as 0.05 Gflops/watt while for MAGMA_DGEMM and MAGMA_DGEQRF it is 1.21 Gflops/watt and 1.09 Gflops/watt respectively in Nvidia Tesla C2050 as shown in figure 7(c). In case of PLASMA_DGEQRF, the performance attained is 0.39 Gflops/watt while running PLASMA_DGEQRF for four cores.

Based on our empirical case studies of DGEQR2, DGEMM, and DGEQRF, we make following observations.

- Due to presence of bandwidth bound operations like DGEMV in DGEQR2, the performance of DGEQR2 is not satisfactory in Intel or Nvidia micro-architectures.
Despite presence of compute bound operations like DGEMM in LAPACK DGEMM, DGEQRF, and MAGMA DGEMM, these routines are able to achieve only 8-16% of the peak GFlops in Intel Haswell and 51.5% of the peak GFlops in Nvidia Tesla C2050 respectively..

Performance achieved by DGEQR2, DGEMM, and DGEQRF in Intel Haswell and Nvidia Tesla C2050 is as low as 0.05-1.23 GFlops/watts

Based on above observations, we see a scope in optimization of DGEQR2 and furthermore improvement in DGEQRF routines in LAPACK. In the next section, we continue our quest for optimizations of these routines for commercially available micro-architectures.

4 MODIFIED HOUSEHOLDER TRANSFORM

In this section, we revisit the classical HT described in algorithm 2 and look for further tuning of the algorithm assuming infinite memory bandwidth and infinite number of arithmetic units required for computing $R$ matrix. It can be observed in the algorithm 2 that the computations of Householder vector is Level-1 BLAS operation and there is no further scope for optimization in computation of Householder vector. The computations that are dependent on the computation of Householder vector are computation of $P$ matrix which is a Householder matrix and trailing matrix update of the input matrix $A$. In classical HT, the trailing matrix update is performed by pre-multiplying matrix $A$ with the Householder matrix $P$ as shown in equations 4 and 5:

$$ P = I - 2vv^T $$

$$ PA = A - 2vv^TA $$

Algorithm 5 Pseudo code of Householder Transform

1: Allocate memories for input matrix
2: for $i = 1 \text{ to } n$ do
3: Compute Householder vectors for block column $m \times k$
4: Compute $P$ matrix where $P = I - 2vv^T$
5: Compute $PA$ where $PA = A - 2vv^TA$
6: end for

Equation 5 in algorithm form is shown in 5. It can be observed in the algorithm 5 that the computation of $2vv^TA$ and computation of $A - 2vv^TA$ can be merged. Routine where we merge these two loops is shown in algorithm 6.

Algorithm 6 Pseudo code of Modified Householder Transform

1: Allocate memories for input matrix
2: for $i = 1 \text{ to } n$ do
3: Compute Householder vectors for block column $m \times k$
4: Compute $PA$ where $PA = A - 2vv^TA$
5: end for
MHT for $3 \times 3$ matrix is shown in figure 8. It can be observed from the figure 6 and 8 that due to fusing of the inner and intermediate loops in MHT, the depth of the graph decreases. It can also be observed that there are more operations per level in the graph. If we take number of operations per level in the DAG of HT as $\beta$, then average $\beta$ is given by equation 6.

$$\beta = \frac{\text{Total Number of Computations in the routine}}{\text{Number of Levels in the DAG of the routine}} \quad (6)$$

Considering ratio of $\beta_{HT}$ and $\beta_{MHT}$,

$$\beta_{HT} = \frac{\text{Number of Operations in HT}}{\text{Number of Levels in DAG of HT}} \quad (7)$$

$$\beta_{MHT} = \frac{\text{Number of Operations in MHT}}{\text{Number of Levels in DAG of MHT}} \quad (8)$$

The parameter $\theta$ in equation 9 is ratio of quantified parallelism in HT and MHT respectively. For our analysis $\theta$ is independent of the computations since there is no change in the computations and it is also independent of communication since the communication pattern remain identical in HT and MHT. As value of $\theta$ decreases the parallelism in MHT is more. For HT and MHT, $\theta$ saturates at 0.749 as shown in figure 9. The method used here to quantify the parallelism in the routine is simple since the computations are regular in nature. For complex algorithms, method described in [36] can be used. To support proposition of improvement in the parallelism in MHT, we experiment on several commercially available multicore and GPUs. For our experiments on multicore, we have used LAPACK available in the Netlib with vendor specific optimizations and we have ensured to use LAPACK program semantics while realizing and integrating realization of MHT in LAPACK [6]. For GPGPUs we have used highly tuned MAGMA package and ensured that the program semantics of MAGMA_DGEQR2HT confirms with MAGMA semantics for ease of integration with the package [30].

### 4.1 Realization on Multicore and GPGPU

We realize MHT on two different commercially available Intel Haswell and AMD Bulldozer micro-architectures as shown in figure 11(a). Figure 11(a) also depicts performances of DGEQRFHT where DGEQRFHT is blocked algorithm analogous to DGEQRF in LAPACK. Since PLASMA is developed using LAPACK as shown in figure 10(a) we integrate LAPACK_DGEQRFHT in PLASMA for experiments.

Pseudo code of LAPACK_DGEQRF2HT is shown in algorithm 7. The routine is implemented as dgeqr2_bt.f in the source code provided with this exposition. Pseudo code of BLAS_UPDATE function that is implemented as update1.f is shown in algorithm 8. It can be observed in the algorithms 7 and 8 that BLAS_UPDATE function forms a major computationally intensive part of LAPACK_DGEQRF2HT. BLAS_UPDATE function becomes part of BLAS that is used inside LAPACK as a basic building block. The routines shown in algorithms 7 and 8 and their wrappers to integrate these routines in LAPACK are supplied with this exposition where directory structure of legacy LAPACK software package is maintained. LAPACK along with Queuing and Runtime for Kernels (QUARK) are used in the PLASMA software stack for multicore realization of LAPACK software package as depicted in figure 10(a) [7].

**Algorithm 7 LAPACK_DGEQRF2HT**

1: Input: Matrix A of size $M \times N$
2: do
3: Norm = 0, S = 0, B = 0
4: if Norm = -SIGN(DNRM2(L,X,1), X(1)) X(1) then
5: Beta = (X(1) - Norm) / Norm
6: Tau = -Beta/Norm
7: L = M - I + 1
8: UPDATE(L, A(I:M,I), A, LDA, I, M, N, Beta, Norm)
9: while (I != N)

Similarly, for realization of MHT on GPGPU, we use MAGMA software stack described in figure 10(b). MHT when implemented for GPGPU is shown in algorithm 9. It can be observed in the algorithm 9 that the computationally intensive part of MAGMA_DGEQRF2HT is MAGMABLAS_UPDATE function shown in algorithm 10. Similar to BLAS_UPDATE in LAPACK_DGEQRF2HT where BLAS_UPDATE is part of BLAS, MAGMABLAS_UPDATE is part of MAGMABLAS. MAGMA_UPDATE is realized as a series
Algorithm 8 BLAS_UPDATE
1: do
2: \[ B = A(K,I) \ast \text{Beta} \]
3: \[ S = \text{DDOT}(L-1, X(2:L, 1, A(K+1:M,I),1) \]
4: \[ B = B + S \]
5: \[ B = B / (\text{Norm} \ast \text{Beta}) \]
6: \[ A(K,I) = A(K,I) + (\text{Beta} \ast B) \]
7: \[ I = K + 1 \]
8: do
9: \[ A(I, I) = A(I, I) + A(J,K) \ast B \]
10: \[ J = K + 1 \]
11: while \( J = M \)
12: while \( I = N \)

of kernels in CUDA C shown in the algorithms [11] [12] [13] [14] [15] and [16].

It can be observed in figure [11(a)] that in AMD Bulldozer micro-architecture LAPACK_DGEQR2HT performs better than LAPACK_DGEQRF, LAPACK_DGEQRF, and LAPACK_DGEQRFHT. The performance of LAPACK_DGEQRFHT and LAPACK_DGEQRF is observed to be same in AMD Bulldozer. In Intel Core i7 4th Gen which is a Haswell micro-architecture, the performance of LAPACK_DGEQRFHT and LAPACK_DGEQRF is same. Apart from that LAPACK_DGEQRFHT and LAPACK_DGEQRF perform around 10% better than LAPACK_DGEQR2HT. When we integrate LAPACK_DGEQR2HT in PLASMA, the attained performance is depicted in the figure [11(b)] that results in PLASMA_DGEQR2HT since the trailing matrix update is using LAPACK_DGEMM along with QUARK. For integration of LAPACK_DGEQR2HT in PLASMA, we have replaced the instance of LAPACK_DGEQRF in PLASMA with the instance of LAPACK_DGEQR2HT. It can be observed in the figure [11(b)] that the performance attained by PLASMA_DGEQR2HT is 10% worse than that of performance attained by PLASMA_DGEQRF.

Performance of MAGMA_DGEQR2HT, MAGMA_DGEQRF, MAGMA_DGEQRF.
Algorithm 10 MAGMABLAS_UPDATE
1: if (m%BLOCK_SIZE != 0) then
2:   dim3 grid ((m/BLOCK_SIZE)+1, 1, 1)
3:   threads (BLOCK_SIZE,1,1)
4: else if (m%BLOCK_SIZE = 0) then
5:   dim3 grid (m/BLOCK_SIZE, 1,1)
6:   threads (BLOCK_SIZE,1,1)
7: end if
8: cublasDgemv(handle, cublas_trans_const(MagmaTrans), M, N, &alpha, dC, lddc, dv, 1, &beta, dtau,1)
9: dtemp<<<1, 1, 0, queue >> cuda_stream()>>>(dC(0,0), dtu, dwork)
10: dcnst<<<grid, threads, 0, queue >> cuda_stream()>>>(n, dC(0,0), lddc, dtu, dwork)
11: ddoff<<<1,1,0,queue >> cuda_stream()>>>(dC(0,0), dwork, dtu, dwrk)
12: drow1<<<<<grid, threads, 0, queue >> cuda_stream()>>>(n, dC(0,0), lddc, dtu, dwork)
13: dtemp<<<<<grid, threads, 0, queue >> cuda_stream()>>>(m, dC(0,0), lddc, dtu, dv)
14: dcnst<<<<<grid, threads, 0, queue >> cuda_stream()>>>(m, dv, dtu, dwork)

Algorithm 11 dtemp
1: Inputs: dot, matrix
2: beta = sqrt(dot)
3: temp = -copysign(beta, matrix)

Algorithm 12 dcnst
1: Inputs: N, matrix, ldda, temp
2: i = blockIdx.x*blockDim.x + threadIdx.x
3: if (i<N) then
4:   dot[i] = MAGMA_D_DIV(dot[i], temp[0] + (matrix[0] - temp[0])) - MAGMA_D_DIV(matrix[ldda*i], (matrix[0] - temp[0]))
5: end if

Algorithm 13 ddiff
1: Inputs: matrix, temp
2: ddiff = matrix - temp

Algorithm 14 drow1
1: Inputs: matrix, ldda, dot, diff
2: i = blockIdx.x*blockDim.x + threadIdx.x
3: if (i<N) then
4:   ltemp = matrix[ldda*i] + MAGMA_D_MUL(dot[i], diff)
5:   matrix[ldda*i] = ltemp
6: end if

MAGMA_DGEQRFHT is shown in figure 11(b). It can be observed that the performance of MAGMA_DGQR2 and MAGMA_DGEQRF2HT is almost similar on Nvidia Tesla C2050 while the performance of MAGMA_DGEQRF and MAGMA_DGEQRFHT is also similar. Unlike Intel or AMD micro-architectures, performance of MHT in Nvidia is nowhere close to the performance of MAGMA_DGEQRF (or MAGMA_DGEQRFHT). This performance figures are not satisfactory since $\beta_{MHT} \geq \beta_{HT}$, and we expect that the performance achieved in LAPACK/PLASMA/MAGMA_DGEQRF2HT is 1.1-1.3x better over LAPACK/PLASMA/MAGMA_DGEQRF2. We also expect that LAPACK/PLASMA/MAGMA_DGEQRF2HT outperforms LAPACK/PLASMA/MAGMA_DGEQRF. Due to lack of domain customizations for BLAS and LAPACK, we are not able to exploit parallelism that is available in MHT and hence we achieve marginally better performance in multicores while we achieve same performance in GPGPU for realization MHT compared to realization of HT. In this section, we presented modification to classical HT and arrived at MHT where through algorithm-architecture co-design, performance of the algorithms can be improved significantly. We adopt methodology presented in [27], and [19], and design a Processing Element (PE) that is efficient in overlapping computations and communication. The PE presented here is also efficient in exploiting Instruction Level Parallelism (ILP) exhibited by BLAS [23][24]. We use this PE as a CFU for REDEFINE for parallel realization to show scalability of algorithms and architecture.

5 Custom Realization of Householder Transform and Results

In this section we present custom realization for HT and show that through algorithm-architecture co-design, performance of the algorithms can be improved significantly. We adopt methodology presented in [27], and [19], and design a Processing Element (PE) that is efficient in overlapping computations and communication. The PE presented here is also efficient in exploiting Instruction Level Parallelism (ILP) exhibited by BLAS [23][24]. We use this PE as a CFU for REDEFINE for parallel realization to show scalability of algorithms and architecture.
5.1 Processing Element Design and Algorithm-architecture Co-design for HT

Design of PE is depicted in figure 12 and it is also shown. It can be observed that PE is separated into two modules: 1) Floating Point Sequencer (FPS), and 2) Load-Store CFU. All the double precision floating point computations are performed in the FPS while Load-Store CFU is responsible for loading/storing data from/to Global Memory (GM) to Local Memory (LM) and LM to Register File, where GM is next level of memory in parallel realization while LM is the private memory of PE, and Register File is small memory of 256 registers [19][21]. Operation of PE can be described in following steps:

- **Step 1**: Send a load request to GM for input matrices and store the arriving elements of the input matrices to LM
- **Step 2**: Store input matrix elements from LM to Register File
- **Step 3**: Perform computations in FPS
- **Step 4**: Store the final/intermediate results from Register File to LM in the Load-Store CFU
- **Step 5**: Store final result to GM

In our implementation of DGEQR2, DGEQRF, DGEQR2HT, and DGEQRFHT, we use similar mechanism. FPS has several resources to perform computations. In this exposition, we use carefully designed DOT4, a square root, and a divider for realization of DGEQR2, DGEQRF, DGEQR2HT, and DGEQRFHT routines [21][22]. Logical place of arithmetic units is shown in the figure 12 and structure of DOT4 is shown in figure 13.

DOT4 can perform inner product of a 4-element vector. DOT4 is a reconfigurable data-path that can be reconfigured to act as different macro operations encountered in the algorithms [19].

In DGEQR2HT, due to fusion of inner most and intermediate loops, we identify a new macro operation apart from usual macro operations. We explain this with an example of a $3 \times 3$ matrix

$$A = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix}.$$  

Applying DGEQR2HT to the matrix $A$ to annihilate $a_{31}$ and $a_{21}$, we compute Householder matrix $P$ and pre-multiply with $A$ as shown in the equation 11.

$$PA = A - 2vv^TA$$  \hspace{1cm} (11)

where $v = \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}$ is Householder vector as explained in section 2

$$PA = \begin{bmatrix} a_{12} & a_{13} \\ a_{22} & a_{23} \\ a_{32} & a_{33} \end{bmatrix} - 2 \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \begin{bmatrix} a_{12} & a_{13} \\ a_{22} & a_{23} \end{bmatrix} = \begin{bmatrix} a_{12} - 2v_1a_1 \\ a_{22} - 2v_2a_1 \\ a_{32} - 2v_3a_1 \end{bmatrix} - 2a_3a_2a_1
$$

where $a_1 = v_1a_{12} + v_2a_{22} + v_3a_{32}$ and $a_2 = v_1a_{13} + v_2a_{23} + v_3a_{33}$.

Taking a close look at the expressions of the updated matrix $PA$ in equation [12] we observe a new macro operation in the expression $a_{12} - 2v_2(v_1a_{12} + v_2a_{22} + v_3a_{32})$. For a $3 \times 3$ matrix there are 6 such macro operation encountered as shown in equation [12]. We realize this macro operation on DOT4 hardware structure as shown in figure 13. For larger matrices, we break the expressions to fit on the DOT4 hardware structure. Performance
after realization of DGEQR2, DGEQRF, DGEQR2HT, and DGEQRFHT is depicted in figure 14(a).

![Reconfigurable Data Path](image)

**Fig. 13:** DOT4 and New Configuration of DOT4 for Realization of DGEQR2HT

It can be observed in figure 14(a) that DGEQR2HT achieves 2x better performance over DGEQR2, 1.23x over DGEQRF, and 1.23x over DGEQRFHT. Interestingly, DGEQR2HT achieves close to 74% of the peak performance that is 99.3% of the performance attained by DGEMM in the PE as shown in figure 14(b). In terms of Gflops/watt DGEQR2HT achieves 2x better performance compared to DGEQR2, 1.23x over DGEQRF, and 1.2x over DGEQRFHT. Surprisingly, compared to some of the state-of-the-art implementations of HT based QR factorization, the proposed MHT based QR factorization attains 3-90x better performance which is better than the performance improvement reported for DGEMM in [23]. Such an unexpected result is attained since for the state-of-the-art platforms, the performance attained by LAPACK/PLASMA/MAGMA DGEQRF is mostly 80-85% of the peak performance attained by DGEMM in the platform while in the PE the performance attained by MHT based QR factorization is 99.3% of the performance attained by DGEMM.

### 5.2 Parallel Implementation of HT

For parallel realization of DGEQR2, DGEQRF, DGEQR2HT, and DGEQRFHT routines, we use simulation environment depicted in figure 12. We attach PE to the Routers in the Tiles of REDEFINE except the last column. In the last column, we attach CFUs with memories that contain same address space. We use this memory as Global Memory (GM).

To show scalability, for experiments, we consider three configurations with different sizes of Tile arrays like $2 \times 2$, $3 \times 4$, and $4 \times 4$. Two configurations are shown in figure 15 namely **Configuration 1** and **Configuration 2** wherein **Configuration 1** is composed of $2 \times 2$ Tile array as a fabric for computations and **Configuration 2** is composed of $3 \times 3$ Tile array as a fabric for computations. Matrix partitioning schemes for different configurations is also depicted in the figure 15 along with configurations. In the matrix partitioning scheme, we have followed an approach that is used in [7] where input matrix is divided into sub-matrix blocks. For a $K \times K$ fabric of computations and $N \times N$ matrix size, we divide matrix in to the blocks of $\frac{N}{K} \times \frac{N}{K}$ sub-matrices. Since, objective of our experiments is to show scalability, we choose $N$ and $K$ such that $\%K = 0$. Results for parallel implementation of DGEQR2, DGEQRF, DGEQR2HT, and DGEQRFHT routines are depicted in the figure 14(e). It can be observed in the figure 14(f) that the speed-up in parallel realization of DGEQR2, DGEQRF, DGEQR2HT, and DGEQRFHT approaches $K \times K$ when realized using Tile array of size $K \times K$.

In figure 14(e) speed-up attained in parallel realization of any routine is the speed-up over corresponding sequential realizations of the routines. Percentage of theoretical peak performance attained by DGEQR2, DGEQRF, DGEQR2HT, and DGEQRFHT is shown in figure 14(f). It can be observed in the figure 14(e) that DGEQR2HT is capable of attaining 66% of the theoretical peak of the Tile array utilized for computations while DGEQR2 attains 16%, DGEQRF attains 39.5%, and DGEQRFHT attain 42% of the theoretical peak performance in REDEFINE. DGEQR2HT in REDEFINE clearly outperforms all other routines as depicted in the figure 14(f) while REDEFINE scales well for DGEQR2, DGEQRF, DGEQR2HT, and DGEQRFHT.

### 6 Conclusion

Performance attained by Householder Transform based QR factorization in the state-of-the-art multicore and GPGPUs is usually 80-85% of the performance attained by General Matrix Multiplication. In this paper, we achieved performance in Modified Householder Transform similar to the performance of General Matrix Multiplication in terms of Gflops which is contrary to the performance attained in the conventional multicore and GPGPU platforms with the state-of-the-art software packages for Dense Linear Algebra. We moved away from classical approach where optimized Basic Linear Algebra Subprograms are used for realization of Householder Transform based QR factorization and fused inner loops in the Householder Transform based QR factorization based routine (DGEQR2 routine) that resulted in higher degree of parallelism. A simplistic approach for quantification of parallelism was adopted to show 1.3 times higher parallelism in Modified Householder Transform. The classical Householder Transform based QR factorization and Modified Householder Transform based QR factorization along with their optimized block implementations were evaluated on the state-of-the-art multicore and GPGPU where it was observed that the parallelism exhibited by Modified Householder Transform is not fully exploited by these platforms. Design of an existing Processing Element was amended to support the macro operations encountered in Modified Householder Transform by adding a new configuration in the Reconfigurable Data-path in the Processing Element. The approach of realizing macro operations on a Reconfigurable Data-path resulted in 2x performance improvement in Modified Householder Transform over classical Householder Transform in the PE. Realization of Modified Householder Transform could also outperform custom realization of block Householder Transform based QR factorization by 1.2-1.3x. Performance improvement of 3-80x is reported in terms of Gflops/watt over multicore, GPGPU, FPGA, and ClearSpeed CSX700. The performance improvement reported is higher than that of General Matrix Multiplication due to counter-intuitive results obtained in Modified Householder Transform. Finally, it is shown that Processing Element as a Custom Function Unit in REDEFINE results in scalable high performance realization of Householder based and Modified Householder based QR factorization.

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For a computer named **Proc**.

In-terms of the Percentage of Peak Performance Attained by DGEMM in [23]

(d) Performance Comparison of REDEFINE-PE with Other Platforms
(e) Performance Comparison of REDEFINE-PE with Other Platforms
(f) Performance Comparison of REDEFINE-PE with Other Platforms

**Fig. 14:** Performance of DGEQR2, DGEQRF, DGEQR2HT, and DGEQRFHT in PE

**Fig. 15:** Simulation Environment for Parallel Realization of DGEQR2, DGEQRF, DGEQR2HT, and DGEQRFHT Routines

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**Anupam Chattopadhyay** Anupam Chattopadhyay received his B.E. degree from Jadavpur University, India in 2000. He received his MSc. from ALaRI, Switzerland and PhD from RWTH Aachen in 2002 and 2008 respectively. From 2008 to 2009, he worked as a Member of Consulting Staff in CoWare R&D, Noida, India. From 2010 to 2014, he led the MPSoC Architectures Research Group in RWTH Aachen, Germany as a Junior Professor. Since September, 2014, he is appointed as an assistant Professor in SCE, NTU.

**Soumyendu Raha** Soumyendu Raha obtained his PhD in Scientific Computation from the University of Minnesota in 2000. Currently he is a Professor of the Computational and Data Sciences Department at the Indian Institute of Science in Bangalore, which he joined in 2003, after having worked for IBM for a couple of years. His research interests are in computational mathematics of dynamical systems, both continuous and combinatorial, and in co-development and application of computing systems for implementation of computational mathematics algorithms.

**Ranjani Narayan** Dr. Ranjani Narayan has over 15 years experience at IISc and 9 years at Hewlett Packard. She has vast work experience in a variety of fields computer architecture, operating systems, and special purpose systems. She has also worked in the Technical University of Delft, The Netherlands, and Massachusetts Institute of Technology, Cambridge, USA. During her tenure at HP, she worked on various areas in operating systems and hardware monitoring and diagnostics systems. She has numerous research publications. She is currently Chief Technology Officer at Morphing Machines Pvt. Ltd, Bangalore, India.

**S K Nandy** S. K. Nandy is a Professor in the Department of Computational and Data Sciences of the Indian Institute of Science, Bangalore. His research interests are in areas of High Performance Embedded Systems on a Chip, VLSI architectures for Reconfigurable Systems on Chip, and Architectures and Compiling Techniques for Heterogeneous Many Core Systems. Nandy received the B.Sc (Hons.) Physics degree from the Indian Institute of Technology, Kharagpur, India, in 1977. He obtained the BE (Hons.) degree in Electronics and Communication in 1980, MSc.(Engg.) degree in Computer Science and Engineering in 1986, and the Ph.D. degree in Computer Science and Engineering in 1989 from the Indian Institute of Science, Bangalore. He has over 170 publications in International Journals, and Proceedings of International Conferences, and 5 patents.