Efficient Sparse-Dense Matrix-Matrix Multiplication on GPUs Using the Customized Sparse Storage Format

Shaohuai Shi, Qiang Wang, Xiaowen Chu
Department of Computer Science, Hong Kong Baptist University
{cshshi, qiangwang, chxw}@comp.hkbu.edu.hk

Abstract—Multiplication of a sparse matrix to a dense matrix (SpDM) is widely used in many areas like scientific computing and machine learning. However, existing works under-look the performance optimization of SpDM on modern many-core architectures like GPUs. The storage data structures help sparse matrices store in a memory-saving format, but they bring difficulties in optimizing the performance of SpDM on modern GPUs due to irregular data access of the sparse structure, which results in lower resource utilization and poorer performance. In this paper, we refer to the roofline performance model of GPUs to design an efficient SpDM algorithm called GCOOSpDM, in which we exploit coalescent global memory access, fast shared memory reuse and more operations per byte of global memory traffic. Experiments are evaluated on three Nvidia GPUs (i.e., GTX 980, GTX Titan X Pascal and Tesla P100) with CUDA-8.0 using a large number of matrices including a public dataset and randomly generated matrices. Experimental results show that GCOOSpDM achieves 1.5-8× speedup over Nvidia’s library cuSPARSE in many matrices. We also analyze instruction-level operations on a particular GPU to understand the performance gap between GCOOSpDM and cuSPARSE. The profiled instructions confirm that cuSPARSE spends a lot of time on slow memory access (including DRAM access and L2 cache access), while GCOOSpDM transfers such slow memory access to faster shared memory, which mainly contributes to the performance gain. Results also show that GCOOSpDM would outperform the dense algorithm (cuBLAS) with lower sparsity than cuSPARSE on GPUs.

Index Terms—Sparse Matrix Multiplication; COO; GCOO; GPU;

I. INTRODUCTION

Sparse-dense matrix-matrix multiplication (SpDM) has many application areas. It is not only exploited in traditional research fields (e.g., graph analytics [1], biology [2]), but becoming a potential faster implementation for sparse deep learning [3][4][5][6][7]. However, it requires very high sparsity of the model to achieve accelerated speed compared to the original dense implementations [8].

Dense matrix multiplication, i.e., $C = A \times B$ or general purpose matrix multiplication (GEMM) has been well studied on GPUs to achieve high efficiency [9][10][11][12][13][14][15][16][17][18]. However, multiplication of a sparse matrix to a dense matrix (SpDM), in which the sparse matrix is stored with memory-saving formats like compressed row storage (CRS) [19], is understudied, and it easily loses efficiency on modern GPUs. For example, the time cost of calculating the multiplication of a $8000 \times 8000$ sparse matrix with sparsity of 0.9 (i.e., 90% of elements are zeros) to a dense matrix with single precision requires 780 ms by using cuSPARSE on an Nvidia Tesla P100 GPU, while the corresponding dense algorithm by cuBLAS only requires 121 ms. In other words, though the sparse matrix can reduce the number of multiplication and accumulation operations (MACs) by 90% (since a zero element times any numbers produces zeros that has no contribution to the final results, so such operations can be avoided.), the highly optimized cuBLAS is about 7× faster than cuSPARSE in the above example. For a much higher sparsity of 0.995, cuSPARSE can be about 50% faster than cuBLAS at the dimension of $8000 \times 8000$ matrices on the P100 GPU. High sparsity requirement on SpDM makes it difficult to be deployed as the efficient implementation of matrix multiplication because of the inefficient algorithm design of the SpDM algorithm in cuSPARSE. In practical problems, on one hand, if the sparsity is not high enough, doing SpDM could result in very low efficiency, while using the dense form could get results faster if there is enough memory; on the other hand, if the sparsity is very high, using the dense form not only leads to low efficiency, but it also wastes memory. From our empirical studies of cuSPARSE and cuBLAS, the sparse algorithm of cuSPARSE requires the matrix sparsity to be larger than 0.99 to outperform the dense counterpart of cuBLAS. One of our key observations of cuSPARSE is that it has many slow memory access that easily leaves the computational resources (i.e., cores) stale in its SpDM APIs. To this end, we would like to design an efficient SpDM algorithm to better utilize the GPU computational resources.

Only a small number of research works focus on high-performance SpDM algorithms for modern GPUs. The most relevant work is [20][21] and [22][23]. On one hand, Ortega et al. [20] try to better optimize the GPU memory access pattern (i.e., coalesced memory access) to achieve higher efficiency. On the other hand, besides the optimization of coalesced memory access, Yang et al. [21] use the principles of row split [24] and merge path [25] in sparse matrix-dense vector multiplication (SpMV) to design more efficient algorithms for SpDM on GPUs. Jiang et al. [23] mainly

1Both cuSPARSE and cuBLAS are from the library of CUDA-8.0.
re-order the row data and Parger et al. [22] propose the parameter tuning technique to optimize the performance of SpDM. However, in [21], the authors design their algorithms mainly for the cases that the dense matrices are tall-skinny, and it requires a heuristic to choose whether to use merge-based or row split for better performance. In this paper, we not only exploit the GPU algorithm optimization principles (e.g., coalesced memory access), but also revisit the popular roofline performance model [26] on GPUs to analyze how to increase operational intensity, and then we propose an efficient SpDM algorithm. Our contributions are summarized as follows:

- We design an efficient SpDM algorithm called GCOOSpDM on GPUs with several optimization techniques including coalescing memory access, bank conflict avoidance of the shared memory and high computation-to-memory ratios.
- We evaluate the proposed algorithm on a large number of sparse matrices including the public dataset and randomly generated matrices, and the experimental results show that GCOOSpDM outperforms cuSPARSE 1.5-8× faster in a large proportion of matrices on Nvidia GPUs.
- We conduct instruction-level analysis for the kernels of GCOOSpDM and cuSPARSE, and the profiled results confirm that our proposed algorithm uses much less slow memory access (DRAM and L2 cache) than cuSPARSE.
- As compared to cuSPARSE, GCOOSpDM decreases the sparsity requirement from 0.99 to 0.98 in order to outperform dense implementation of cuBLAS.

The rest of the paper is organized as follows. Section II gives introductions to the preliminaries related to SpDM and GEMM. We present our proposed algorithm for efficient SpDM in Section III. The experimental evaluation and analysis are illustrated in Section IV. Section V introduces the related work, and finally we conclude this paper in Section VI.

II. Preliminaries

A multiplication of two matrices $A \in \mathbb{R}^{m \times k}$ and $B \in \mathbb{R}^{k \times n}$ produces an result matrix $C \in \mathbb{R}^{m \times n}$, i.e.,

$$C(i,j) = \sum_{l=0}^{l=k-1} A(i,l) \times B(l,j). \quad (1)$$

To simplify the analysis of the algorithms, we assume that the dimensions of $A$ and $B$ are both $n \times n$. The sparsity $s$ of matrix $A$ is defined as the ratio of the number of zero elements over the total number of elements.

A. The roofline model

The roofline model [26] is commonly used in performance modeling of multi-core/many-core architectures like GPUs [27][16][28]. The term operational intensity $r$ (operations per byte of DRAM traffic) is defined to predict the performance of kernels. In the model, there is an upper bound of the GPU throughput when $r$ reaches some threshold, which indicates the program is computation-bound. If $r$ is smaller than the threshold, the GPU throughput is a linear function with respect to $r$, which indicates the program is memory-bound. Using cuBLAS GEMM as an example, in Fig. 1 we compare the experimental throughput of dense matrix multiplication with the theoretical throughput from roofline model on two different Nvidia GPUs, GTX980 and Titan X.

Though GEMM in cuBLAS has achieved nearly optimal throughput on matrix multiplication, directly applying GEMM for sparse matrices could result in many useless calculations due to the large amount of zeros. The irregular non-zero elements in sparse matrices make the data access from global memory to registers become the bottleneck of matrix multiplication. In other words, each time of data reading from the sparse matrix, only a limited number of computational operations. Therefore, algorithms for SpDM are generally memory-bound, and for such problems, one should design the algorithm to increase $r$ to achieve higher efficiency.

![Image of Fig. 1: The roofline models for theoretical peak throughput and cuBLAS throughput with single-precision on GPUs.](image-url)

B. GPU memory hierarchy

From the roofline model, one should improve the memory access efficiency to fully utilize the computational power of GPUs. There are several types of memories in the GPU memory hierarchy. From fast to slow of access speed, it contains registers, the shared memory (or L1 cache), L2 cache and the global memory [9][29][30]. The shared memory and global memory are two kinds of memories that can be flexibly manipulated by programming. In general, data that is repeatedly used could be put into the shared memory or registers for better utilization of GPU cores.

C. COO: The coordinate storage format

Assume that the matrix is a row-major matrix. The coordinate storage format (COO) [24] is a simple storage scheme for sparse matrices. COO uses an array `values` to store the values of all non zero elements. The coordinate information of each non zero element is sequentially stored in array `rows`
and array \( cols \) respectively. Take a real-valued example of a \( 4 \times 4 \) sparse matrix as follows:

\[
A = \begin{bmatrix}
7 & 0 & 0 & 8 \\
0 & 10 & 0 & 0 \\
9 & 0 & 0 & 0 \\
0 & 0 & 6 & 3
\end{bmatrix},
\]

the COO format of \( A \) is represented by

\[
\begin{align*}
\text{values} &= [7, 8, 10, 9, 6, 3], \\
\text{rows} &= [0, 0, 1, 2, 3, 3], \\
\text{cols} &= [0, 3, 1, 0, 2, 3].
\end{align*}
\]

### III. Efficient Algorithm Design

In this section, we describe the design of our proposed efficient SpDM algorithm on GPUs including the customized storage format for sparse matrices and its conversion from the dense ones. According to the above analysis in operations of SpDM on GPUs, we first design a new sparse format called grouped COO (GCOO), which is convenient for coalesced memory access and is useful to increase the operational intensity \( r \). Then we propose an efficient SpDM algorithm by using GCOO.

#### A. GCOO: Grouped COO storage format

A similar format of GCOO is the sliced COO (SCOO) format proposed in [31], with which the authors achieved higher throughput on sparse matrix-vector multiplication (SpMV) on both CPUs and GPUs. In this paper, we bring the idea of SCOO to propose GCOO for matrix multiplication. The sparse matrix is partitioned to \( g \) groups according to the number of columns \( n \), and each group is stored in the COO format, so we call it GCOO. For an \( n \times n \) matrix stored in the GCOO format, there are \( g = \left\lceil \frac{n}{p} \right\rceil \) groups, and each group contains \( p \) columns except the last one who has \( n-(g-1)\times p \) columns. If \( n \) is divisible by \( p \), then the last group also has \( p \) columns. In GCOO, each group is stored in the COO format, and COOs from all groups are concatenated into one array. Let group \( i \) be stored in the COO format with \( \text{rows}_i, \text{cols}_i \) and \( \text{values}_i \), where \( i = 0, 1, ..., g-1 \). We have the stored values of GCOO with \( \text{rows}, \text{cols} \) and \( \text{values} \) that are generated from the concatenation of \( \text{rows}_i, \text{cols}_i \) and \( \text{values}_i \), respectively.

An example of grouping in matrix \( A \) is shown in Fig. 2. Matrix \( A \) is divided into 2 groups. Group 0 is represented by \( \text{rows}_0 = [0, 1, 2], \text{cols}_0 = [0, 1, 0] \) and \( \text{values}_0 = [7, 10, 9] \); and group 1 is represented by \( \text{rows}_1 = [0, 3, 3], \text{cols}_1 = [3, 2, 3] \) and \( \text{values}_1 = [8, 6, 3] \). Finally, two groups are concatenated into one array with an extra index array \( gIdxes \) to indicate which positions are corresponding to related groups. Therefore, the final stored format of GCOO is as follows:

\[
\begin{align*}
\text{values} &= [7, 10, 9, 8, 6, 3], \\
\text{rows} &= [0, 1, 2, 0, 3, 3], \\
\text{cols} &= [0, 1, 0, 3, 2, 3], \\
gIdxes &= [0, 3],
\end{align*}
\]

where \( gIdxes \) is an auxiliary array to store the group indexes. It is noted that \( \text{rows}, \text{cols} \) and \( \text{values} \) in GCOO are not the same as those of COO since a single group in GCOO is in a COO format. In order to easily access each group’s elements, we use an extra auxiliary array, \( \text{nnzPerGroup} \), to store the number of non-zero elements in each group. In the above example, the values of \( \text{nnzPerGroup} \) should be:

\[
\text{nnzPerGroup} = [3, 3].
\]

In practice, GCOO spends slightly more memory space than COO and CSR, but it provides more convenient access of data with a higher probability. The comparison of memory consumption to store an \( n \times n \) matrix with a sparsity of \( s \) (note that \( \text{nnz} = s \times n^2 \)) is shown in Table I.

| Format | Memory complexity |
|--------|-------------------|
| CSR    | \( 2 \times \text{nnz} + n \) |
| COO    | \( 3 \times \text{nnz} \) |
| GCOO   | \( 3 \times \text{nnz} + 2 \times \lceil \frac{n+p-1}{p} \rceil \) |

The main advantage of GCOO is to help reuse the data from slow memories (e.g., global memory and L2 cache). Specifically, if there exist two or more continuous non-zero elements in one group that are in the same row, then the fetched element from the dense matrix \( B \) can be reused in the register instead of being read from the slow memory again.

#### B. Matrix conversion to GCOO

For the cases that the input matrices \( A \) and \( B \) are stored in the dense form, there would be an extra overhead in the format conversion to apply the SpDM algorithm. For example, cuSPARSE provides an API “cusparseSdense2csr” to convert the dense matrix to the CSR format so that one can apply the SpDM APIs. For our proposed GCOO, we also need to provide an efficient conversion scheme to convert the dense matrix to GCOO. We use two steps to convert the dense matrix to the GCOO storage.

Step 1: Count the number of non-zero elements. To convert a dense form of a matrix to the sparse form, one should first count the number of non-zero elements (\( \text{nnz} \)) of that matrix in order to allocate the memory according to the value of \( \text{nnz} \). As for GCOO, we have pre-grouped the matrix by pre-defined \( p \), so it is straightforward to calculate the non-zero elements in parallel for different groups such that the array \( \text{nnzPerGroup} \).
can also be calculated. Therefore, in this step, nnz, gIdxes and nnzPerGroup can be calculated by scanning the original dense matrix.

Step 2: Store the non-zero elements to rows, cols and values. First, the memories of rows, cols and values are allocated according to nnz, and then we can read the non-zero elements with their coordinate information and write them to rows, cols, and values according to the indexes by nnzPerGroup in parallel.

The pseudocode of the matrix conversion on the GPU from the dense form to GCOO is shown in Algorithm 1.

**Algorithm 1 convertToGCOOFormat**

**Input:** A, wA, hA, p  
**Output:** values, cols, rows, gIdxes, nnzPerGroup

1: nGroup = (hA + p - 1)/p;
2: Allocate memory for gIdxes and nnzPerGroup according to nGroup;
3: Calculate gIdxes and nnzPerGroup and nnz by scanning A;
4: Allocate memory for values, cols, and rows according to nnz;
5: Set values of values, cols and rows by scanning A;

C. GCOOspDM: an efficient SpDM algorithm

In the proposed algorithm GCOOspDM, we focus on three factors that have major impact on the performance. 1) Data partition for the CUDA execution context [32]. 2) The coalesced memory access of global memory on the sparse matrix A and the two dense matrices B and C. 3) When exploiting the faster memory on Nvidia GPUs with the shared memory, we guarantee that the access of the shared memory has no bank conflict. 4) After accessing a single element of the sparse matrix A, we strive to calculate more results for C, i.e., achieving higher operational intensity, so that we can achieve higher GFLOPS.

Data partition of matrices. In the context of CUDA, a thread is the smallest execution unit of instructions. A group of threads forms a thread block, which is executed in a stream multiprocessor (SM) of GPU. Multiple thread blocks form a grid, and some thread blocks are executed in parallel on different SMs at one time. Let b denote the size of a thread block. In our algorithm, each thread block calculates \( b \times p \) elements of C separately, so a resulting \( n \times n \) matrix requires \( \lceil \frac{p}{n} \rceil \times \lceil \frac{b}{p} \rceil \) thread blocks. All threads in a thread block share a group of sparse data of A, but each thread reads continuous columns B to do the operations of multiplication and addition to the continuous columns of C. An example of data partition for \( b = 4, p = 2 \) and \( n = 6 \) is shown in Fig. 3. In the grid, it has 6 thread blocks. Each thread block contains \( b = 4 \) threads, and it calculates 8 elements of C. Each thread calculates \( p = 2 \) elements of C.

Coalesced memory access. Three matrices including one sparse matrix A with the GCOO format and two dense arrays (B and C) are needed to interactive with the global memory. Irregular global memory access would result in performance degradation on modern GPUs, so we should read the input matrices (A and B) and write the output matrix C in a coalesced way.

First, we consider the sparse matrix A stored with the GCOO format. Since each group in GCOO of A is assigned to one thread block, we just need to consider the block level access of one group of GCOO, i.e., a COO format that has \( p \) columns. The number of floating point operations is determined by the number of non-zero elements of A, so we scan COO to find the corresponding columns of B. Due to the sparse property, COO could not have many elements, which means we can load COO to the shared memory such that all the threads can read the data fast. Therefore, the \( b \) threads in one thread block read \( b \) elements of COO from the global memory to the shared memory in a coalesced way. After A has been put into the shared memory, it is no need to re-read the elements of A from the global memory.

Second, the dense matrix of B should be read-aware. The matrix B only needs to be accessed when a \((col, row, a)\) of COO has been read from the shared memory, so every thread reads the same \((col, row, a)\), the corresponding column of B should be same while the rows should be different to keep all the threads busy and work balance. So threads \( t_0, t_1, \ldots, t_{b-1} \) need to read \( B(row_0, col), B(row_1, col), \ldots, B(row_{b-1}, col) \) in the current block respectively. In order to support the coalesced memory read of B, the row elements should be in the continuous memory. It is easy to do this because we can just transpose B or store B in a column-major matrix such that the above elements are in the continuous memory.

Finally, for the result matrix C, we should only write the matrix once with the final result for each thread to achieve higher throughput. As discussed above, thread \( t_i \) reads \((col, row, a)\) of A, and multiplies with the elements indexed by \((row_i, col)\) in B, so the write position of C should be \((row_i, row)\). As a result, C should also be column-major or transposed for the coalesced memory writing.

None bank conflict access of the shared memory. The shared memory used in our algorithm is only proper to the sparse matrix of A with the COO format (in one thread block). The kernel allocates a fixed size \( b \) of shared memory, and the threads in one thread block read \( b \) non-zero elements from A each time. Since all the threads in one thread block need to read all elements of A to calculate the corresponding columns of C, all threads read the same element of A. Therefore, the data in the shared memory can be accessed by all threads in a broad cast way [32], which would not result in any bank conflict, and the broadcast access of the shared memory requires only a very small number of clock cycles to fetch the data.

High computation-to-memory ratio. Achieving a high operational intensity \( r \) is very important to a high throughput. Regarding the multiplication and accumulation of each thread, each thread reads the shared memory of A to get \((col, row, a)\) (donated by \(a_r\)), and then multiplies \(B(row_i, col)\) (donated by \(b_r\)) of B. In such scenario, we have two opportunities to have more calculations with \(a_r\) and \(b_r\) since they have been loaded into the registers. The first chance is to find other element of
\( B \) to be multiplied with \( a_r \), but the other element that can be multiplied with \( a_r \) has been assigned to the other block, so this chance cannot be fulfilled. The second one is to find a next element of \( A \) who has the same column with the previous one while its row is different, i.e., \((col, row), a)\). Therefore, we can search the next \( a_{r+1} \) (since \( A \) has been loaded in the shared memory, the time cost of searching is low.) to reuse \( b_r \). If such an \( a_{r+1} \) exists, then we can have \( b \) times of multiplication and accumulation without an extra global memory (or L2 cache) access, which results in a higher \( r \). For a uniform distributed sparse matrix with sparsity of \( s \), there could be \((1-s) \times n\) non-zero elements in the same column.

According to the above four criteria, we conclude the GCOOSpDM algorithm with the following three steps.

Step 1. Each thread block iteratively reads the COO values into the shared memory such that all threads in this thread block can read the COO values for their rows. We exactly know the columns that we need to calculate in the current thread block.

Step 2. The \( s \)th thread scans the COO items from the shared memory, and the item contains \( row, col \) and \( value \). According to \( col \), the thread reads the element \( B(t, col) \) of \( B \), and then performs the multiplication of \( value \times B(t, col) \), whose result is added to the local variable \( c_{t, col} \). I.e., \( c_{t, col} = value \times B(t, col) \).

Step 3. Since the current group of data is stored as the COO format, for the current element \((row, col, value)\), its next element should have the same \( col \) index if that column has more than one element. So we continue scanning the shared memory to check if there are elements that have the same \( col \) such that we can reuse the element of \( B(t, col) \).

To show the effectiveness of our proposed algorithm, we do varies of experiments across three Nvidia GPU cards (i.e., GTX 980, GTX Titan X Pascal and Tesla P100) using two kinds of data. The first one is the public sparse matrix dataset [33] which has different patterns of matrices, and the second one is randomly generated matrices whose zero-valued elements have a uniform distribution. The characteristics of tested GPUs are shown in Table [11]. And the software installed is CUDA-8.0.

### IV. Evaluation and Analysis

#### A. Results on public sparse matrices

We use the public sparse matrices in [33]. Since we only consider the schemes of square matrices, we pick

![Fig. 3. Partition of matrices. A is the sparse matrix, B is the dense matrix, and C is the result matrix.](image-url)

The visualization of the algorithm executed with the CUDA programming model is shown in Fig. 3. On the grid level, there are 6 thread blocks, and each thread block calculates the results of sub-matrix with size of \( b \times p \) from \( b \) rows of \( B \), and \( p \) columns (i.e., one group in GCOO) of \( A \). On the thread block level, the GCOO data of sparse matrix are loaded into faster memory once (the shared memory) which is shared among all the threads in the thread block. On the thread level, each thread independently takes charge of computing \( p \) elements of \( C \), say the thread scans the shared memory to read \( row, col \) and \( value \), and then reads the values in column \( row \) of \( B \), which are multiplied by \( value \) separately, and each result is accumulated to column \( col \) of \( C \). The algorithm of GCOOSpDM is shown in Algorithm [2].

In Algorithm 2, we first (line 1-10) initialize some local variables including the thread level indexes of output and COO for the current thread block. Then we iteratively scan a block of COO in the for-loop of line 11, and at each iteration, a thread block of COO values are loaded into the shared memory (line 12-15). After that each value of COO in the shared memory is read by all the threads in one thread block, and the corresponding value \( b \) in \( B \) is also read to calculate the result (line 21-26). Instead of continuing the above step, we keep the value of \( b \) in the register, and scan the shared COO to check whether we can reuse \( b \) so that less memory operations are required (line 28-36). By this way, we can achieve higher operational intensity, i.e., \( b \) is reused to do more floating point calculations. At the end, the local results of each thread are written back to \( C \) that is stored in the global memory with corresponding indexes (line 38-39). Note that both reading of matrix \( A \) and matrix \( B \) from the global memory is in a coalescent way, the result writing to matrix \( C \) is also coalescent. In term of access of the shared memory, it broadcast the data to all the threads in a warp with a small number of cycles.

### Table II

| Characteristics of tested GPUs. |
|-------------------|---|---|---|
| Model             | GTX980 | TitanX | P100 |
| SMs \times cores per SM | 16×128 | 28×128 | 56×64 |
| Peak TFLOPS       | 4.981 | 10.97 | 9.3 |
| Memory Bandwidth (GB/s) | 224 | 433 | 732 |

2 Codes of GCOOSpDM and scripts of performance evaluation can be found in [https://github.com/hclhkbu/gcoospdm](https://github.com/hclhkbu/gcoospdm) And the raw data of our experimental results can be found in [https://github.com/hclhkbu/gcoospdm/tree/master/results](https://github.com/hclhkbu/gcoospdm/tree/master/results)
Algorithm 2 GCOOSpDM

Input: values, cols, rows, gIdxes, nzPerGroup, wA, hA, B, wB, hB, C

Output: C
1. Cj = blockIdx.y * b + threadIdx.x;
2. C0i = blockIdx.x * p;
3. Initial local temporary results c[0...p];
4. Set number of non-zero elements of current group: nnz;
5. // Set the context group of C0
6. vals = values + gIdxes[blockIdx.x];
7. cols = cols + gIdxes[blockIdx.x];
8. rows = rows + gIdxes[blockIdx.x];
9. iter = (b + nnz - 1)/b;
10. extra = nnz%b;
11. for i = 0 to iter do
12.   cooOffset = i * b;
13.   sVals[threadIdx.x] = vals[cooOffset];
14.   sCols[threadIdx.x] = cols[cooOffset];
15.   sRows[threadIdx.x] = rows[cooOffset];
16.   nnz = max(extra, b);
17.   __syncthreads();
18.   if Cj < wB then // Not exceed the boundary
19.     k = 1;
20.     for j = 0 to nnz, step = k do
21.       col = sCols[j];
22.       row = sRows[j];
23.       av = sVals[j];
24.       bv = B[col * wB + Cj]; // Registered.
25.       outIdx = rowk(p - 1);
26.       c[outIdx] += av * bv;
27.       k = 1;
28.     while j + k < nnz do // Search A to reuse bv
29.       newCol = sCols[j + k];
30.     if newCol ≠ col then
31.       break;
32.       av = sVals[k + j];
33.       row = sRows[k + j];
34.       outIdx = rowk(CPG - 1);
35.       c[outIdx] += av * bv;
36.       k + = 1;
37.     __syncthreads();
38.     for i = 0 to p do // Write results to the global memory
39.       C[Cj + (C0i + 0) * wB] = c[i];

up all the square matrices in the dataset to evaluate the performances of GCOOSpDM and cuSPARSE. The chosen dataset contains 2694 matrices, whose sparsity is in the range of [0.98, 0.999999], and their dimensions are in the range of [64, 36720]. The performance comparison between GCOOSpDM and cuSPARSE is shown in Fig. 4 where T_{algorithm} is used to denote the execution time of algorithm. We first compare the overall performance of our algorithm with cuSPARSE on the 2694 matrices, and we then choose 14 types of matrices from various of applications to compare the performance of the algorithms.

Overall performance. In the 2694 tested matrices, there are about 78% matrices that GCOOSpDM outperforms cuSPARSE on the P100 GPU, and the other 22% matrices that GCOOSpDM achieves better performance than cuSPARSE on both GTX980 and TitanX. The average speedups are 1.66×, 1.7× and 1.68× on GTX980, TitanX and P100 respectively. Moreover, the maximum speedups of GCOOSpDM are 4.5×, 6.3× and 4.2× on GTX980, TitanX and P100 GPUs respectively. By contrast, on the 22% matrices that cuSPARSE is better than GCOOSpDM on the P100 GPU, cuSPARSE only outperforms GCOOSpDM about 1.2× on average. On GTX 980 and Titan X GPUs, there are about 10% cuSPARSE outperforming GCOOSpDM about 1.14×. cuSPARSE performs better on the P100 GPU than GTX 980 and Titan X GPUs mainly because the P100 GPU has a much higher memory bandwidth than the other two GPUs as shown in Table III.

14 types of matrices. It can be seen that GCOOSpDM does not always outperform cuSPARSE. To further understand the main reasons, we select 14 types of matrices that have different structures and non-zero patterns from a range of areas to analyze their performance differences. The details of the selected matrices are shown in Table III. To normalize the algorithm performances, we use effective GFLOPS to measure the algorithms as the following Equation

\[ P_{algorithm} = \frac{2 \times n^3 \times (1 - s)}{T_{algorithm}}. \] (2)

The performance comparison is shown in Fig. 5. On three matrices (“nemeth11”, “plbuckle” and “fpga_decp_01”), GCOOSpDM is worse than cuSPARSE due to the non-zero
distribution of the matrices. On these three matrices, the non-zero elements are mainly located on the diagonal of the matrices, such that there is little opportunity to reuse the pre-fetched value of bv (i.e., line 30 will intermediate hold and no further calculations for current bv), but it still spends extra overheads to search A.

![Graph](image-url)

Fig. 5. The performance comparison of selected matrices on a Tesla P100 GPU. (The higher the better.)

## B. Random sparse matrices

We randomly generate square matrices whose dimension are in the range of [400, 14500] with a step size of 100. For each size of a matrix, we generate the elements with the sparsity in two ranges (i.e., [0.8, 0.995] at a 0.005 step and [0.995, 0.9995] at a 0.0005 step). In total, there are 6968 matrices with uniformly distributed non-zero elements for evaluation.

**Overall performance.** The performance comparison between GCOOSpDM and cuSPARSE using the randomly generated matrices is shown in Fig. 6. Our GCOOSpDM algorithm outperforms cuSPARSE in 99.51%, 99.23% and 97.37% matrices on GTX980, TitanX and P100 GPUs respectively, and the average speedups are 2.13×, 2× and 1.57× respectively. Particularly, the maximum speedups on the three GPUs are 4.7×, 6.5× and 8.1× respectively. On the cases that cuSPARSE is better GCOOSpDM, they only occupy a very small proportion (less than 3%), and the average performance ratio is only around 1.17, which indicates very close performance on less than 3% cases.

**Time vs. sparsity.** As we have shown the efficiency of GCOOSpDM in large range of matrices and sparsity, we want to study further about the performance related to the sparsity $s$. We take two matrices with medium ($n = 4000$) and large ($n = 14000$) dimensions to show the relationship between performance and sparsity. The range of sparsity is kept at [0.95, 0.9995]. Here we also put the time cost of the dense algorithm from cuBLAS into comparison so that we can understand under what sparsity GCOOSpDM can outperform cuBLAS. The results for these two sizes of matrices on GTX980, TitanX and P100 GPUs are shown in Fig. 7 and Fig. 8 respectively. On one hand, it can be seen that cuBLAS has a constant time cost when the sparsity of matrix increases since the dense algorithm does not consider zero values. On the other hand, the sparse algorithms of $\text{11}$ and $\text{12}$ respectively.
cuSPARSE and GCOOSpDM tend to have a linear speedup when the sparsity increases. Given the two specific dimensions of matrices, GCOOSpDM outperforms cuSPARSE with all sparsity. When the sparsity becomes larger than some thresholds, the sparse algorithm would have advantages than the dense one. However, cuSPARSE needs the sparsity be up to 0.995 to outperform cuBLAS, while our proposed algorithm GCOOSpDM can outperform cuBLAS with sparsity larger than 0.98. In summary, the GCOOSpDM algorithm is more applicable for matrix multiplication on GPUs than cuSPARSE and cuBLAS under sparsity larger than 0.98 to achieve higher performance on current GPUs.

![Fig. 10. Performance vs. dimension on GTX980. The higher the better.](image1)

![Fig. 11. Performance vs. dimension on TitanX. The higher the better.](image2)

![Fig. 12. Performance vs. dimension on P100. The higher the better.](image3)

**Performance vs. matrix size.** To further show the sensitivity of the algorithm to the matrix size, we demonstrate the throughput (GFLOPS) in a range of matrix dimensions (i.e., $n \in [400, 14000]$) at two sparsity 0.98 and 0.995. The experimental results with sparsity of 0.98 and 0.995 are in Fig. 10 and 12 on three different GPUs. On the three tested GPUs, GCOOSpDM outperforms cuSPARSE with different values of $n$ and two sparsity. For small matrices (e.g., $n < 1500$), cuBLAS still outperforms GCOOSpDM since it takes only a small number of cycles in calculating small matrices while GCOOSpDM needs extra overheads on memory allocation and matrix conversion. Given the sparsity of 0.98 and $n > 2000$, GCOOSpDM achieves similar performance as (or slightly better than) cuBLAS. With the sparsity of 0.995, cuSPARSE achieves close performance with cuBLAS, while GCOOSpDM outperforms cuBLAS up to 2 times.

**C. Breakdown of time costs**

In this subsection, assume that given $A$ and $B$ are both in the dense form, while $A$ is of high sparsity, we would like to present the time costs of matrix conversion and the kernel calculation to finish the matrix multiplication using the sparse algorithm. The different overheads are summarized into three categories: memory allocation for sparse matrix storage, matrix conversion from the dense form to the sparse form, and SpDM kernel calculation. We summarize the first two categories as an extra overhead (EO), and the third one as the real time cost of kernel calculation (KC). The metrics of EO and KC are used to compare GCOOSpDM and cuSPARSE.

Instead of using three GPUs, we only choose a TitanX GPU as our analysis platform, since three GPUs should have similar time distribution. Similar to the previous subsection, we use two sizes of matrices (i.e., $n = 4000$ and $n = 14000$) with sparsity of $[0.95, 0.96, 0.97, 0.98, 0.99]$ for comparison. The results are shown in Fig. 13. It can be seen that EO has only a small proportion of the total time, and both GCOOSpDM and cuSPARSE have a very close overhead of EO. The dominated part is the execution time of the kernel that calculates the matrix multiplication.

![Fig. 13. Time breakdown for two sizes of matrices. “GCOO.” represents the GCOOSpDM algorithm, and “cuSPA.” represents the algorithm in cuSPARSE.](image4)

**D. Instruction analysis**

In this subsection, we compare the instruction distributions of cuSPARSE and GCOOSpDM and explore how the matrix dimension $n$ and the sparsity $s$ take effects on them. The instruction distribution is the runtime statistics of kernel instructions executed on the real GPU hardware. Not only does it help reveal the major performance bottleneck of the GPU kernel, but also determine some quantitative relationships between instructions and kernel performance.
We use `nvprof` to collect the runtime instructions of different types, including single-precision floating-point operations, DRAM memory access, L2 cache access, shared memory access and L1/Texture memory access. We use the TitanX GPU as our testbed in the profiling experiments. The other two GPU platforms, GTX980 and P100, can be analyzed with the same experimental methodology.

We conduct two sets of random sparse matrix experiments on cuSPARSE and GCOOSpDM respectively. First, we fix the matrix sparsity \( s \) as 0.995 and scale the matrix dimension \( n \) from 500 to 10000. This setting helps exploit how \( n \) affects the instructions of those two algorithms. Second, we fix the matrix dimension \( n \) as 4000 and scale the matrix sparsity \( s \) from 0.8 to 0.9995. This setting helps exploit how \( s \) affects the instructions of those two algorithms. Furthermore, we can also witness the difference of instruction distributions of cuSPARSE and GCOOSpDM under the same experimental setting. The results are demonstrated in Fig. 14, in which \( n_{\text{dm}} \) denotes the number of DRAM memory access transactions, \( n_{\text{l2}} \) denotes the number of L2 cache access transactions, \( n_{\text{shm}} \) denotes the number of shared memory access transactions, \( \text{tex}_{\text{l1}}_{\text{trans}} \) denotes the number of L1/Texture memory access transactions. We find that the DRAM memory access transactions of both two algorithms only take a very few percentage of total number of memory access transactions. Recall that the DRAM memory has the highest access latency and lowest throughput in the GPU memory hierarchy. Avoidance of very frequent DRAM memory access helps decrease the data fetch overhead of the GPU kernel execution. Both cuSPARSE and GCOOSpDM have well-organized data access patterns to utilize L2 cache and on-chip cache (including shared memory and L1/Texture cache). However, the major parts of memory access instructions of those two algorithms are different. \( n_{\text{l2}} \) takes great majority in cuSPARSE, while \( n_{\text{l2}}, n_{\text{shm}} \) and \( \text{tex}_{\text{l1}}_{\text{trans}} \) take approximately the same partitions in GCOOSpDM. GCOOSpDM has higher utilization of on-chip cache of GPUs than cuSPARSE so that it generally outperforms cuSPARSE on randomly generated sparse matrices, which confirms the experimental results in Fig. 6.

We then focus on how \( n \) and \( s \) influence the numbers of those major memory access instructions. The above two figures in Fig. 14 show the effects of \( n \) on cuSPARSE and GCOOSpDM respectively, while the bottom two show the effects of \( s \). We observe that \( n_{\text{l2}} \), \( n_{\text{shm}} \) and \( \text{tex}_{\text{l1}}_{\text{trans}} \) of GCOOSpDM all indicate quadratically increasing trends with respect to \( n \). It is reasonable since the element number of the output matrix \( C \) is \( n^2 \), each of which needs nearly equal workloads of one vector dot product operation. However, the effects of \( s \) show a few differences. \( n_{\text{l2}} \) of cuSPARSE performs a nearly quadratically decreasing trend with respect to \( s \), while \( n_{\text{l2}}, n_{\text{shm}} \) and \( \text{tex}_{\text{l1}}_{\text{trans}} \) of GCOOSpDM show a nearly linearly decreasing trend. Those observations are also reflected in the performance changing behaviors with respect to \( n \) and \( s \), as illustrated in Fig. 15. On one hand, as the matrix size \( n \) increases, the performance of both cuSPARSE and GCOOSpDM demonstrates similar quadratically increasing trends, which meets changing behaviors of their dominating memory instructions. On the other hand, as matrix sparsity \( s \) increases, the performance of cuSPARSE shows an approximately quadratically decreasing trend, while that of GCOOSpDM shows a linearly decreasing trend. They are also similar to those changing behaviors from exploring the effects of \( s \) to the dominating memory instructions of those two algorithms.

![Fig. 14. The instruction distribution comparison with respect to the matrix size \( n \) and the sparsity \( s \) between cuSPARSE and GCOOSpDM on the TitanX GPU. The upper two figures show instruction distributions of different \( n \) with fixed \( s = 0.995 \). The bottom two figures show instruction distributions of different \( s \) with fixed \( n = 4000 \).]

![Fig. 15. The performance scaling behaviors with respect to the matrix size \( n \) and the sparsity \( s \) between cuSPARSE and GCOOSpDM on the TitanX GPU. The lower the better.]

**V. RELATED WORK**

Multiplication of sparse matrices to dense vectors (SpMV) on GPUs have been well studied (e.g., [34][35][24][25]). Even SpDM can be implemented by multiple SpMVs, the
performance could be bad due to a large number of kernel invokes if the matrix is with a large dimension. However, some optimization principles can be applied for SpDM. For example, Yang et al. \cite{Yang:2014} use split row \cite{split_row} and merged path \cite{merged_path} to design SpDM algorithms particularly for tall-skinny matrices.

Regarding the SpDM algorithm analysis, Greiner et al. \cite{Greiner:2009} propose an I/O model to interpret the lower bound of efficient serial algorithms. Cache oblivious dense and sparse matrix algorithms are presented by Bader et al. for multicore CPUs \cite{Bader:2012}. Performance benchmarks \cite{Bader:2012} are conducted to evaluate the efficiency of different sparse matrix formats for SpDM. Koanantakool et al., \cite{Koanantakool:2018} introduce the communication-avoiding SpDM algorithms that are applied in distributed memory systems. Recent work in designing the row reordering technique to achieve better data temporal locality \cite{Koanantakool:2018} and the dynamic parameter tuning \cite{Koanantakool:2018} to improve the SpDM performance on GPUs.

VI. CONCLUSION AND FUTURE WORK

Sparse-dense matrix-matrix multiplication is commonly used in many scientific computing areas, while designing such algorithms on modern GPUs is non-trivial due to the irregular structure of the sparse matrix. In this paper, we propose an efficient sparse matrix-dense matrix multiplication algorithm on GPUs, called GCOOSpDM. The main optimization techniques used in our algorithm are the coalesced global memory access, proper usage of the shared memory, and reuse the data from the slow global memory. The experimental results show that our proposed algorithm outperforms the vendor-based library: cuSPARSE several times on both the public sparse dataset and randomly generated matrices on three recent Nvidia GPUs (i.e., GTX 980, Titan X Pascal, and Tesla P100). We also analyze in depth the performance improvement on instruction-level to understand why GCOOSpDM performs better than cuSPARSE. The key observation of the instruction-level analysis is that the reduced number of global memory access contributes a lot to the performance gain.

It is difficult for a single algorithm to fit all structures of matrices, sparsity and different types of GPUs. Auto-tune algorithms play an important role for algorithms to find efficient configuration or implementations in different cases. We would like to consider the auto-tune scheme to set proper $p$ and $b$ for our GCOOSpDM algorithm in the future work, and try to extend the GCOO storage format to the multiplication of two sparse matrices.

REFERENCES

\begin{enumerate}
\item A. Tiskin, “All-pairs shortest paths computation in the BSP model,” in \textit{International Colloquium on Automata, Languages, and Programming}, Springer, 2001, pp. 178–189.
\item F. Vazquez, E. Garzon, and J. Fernandez, “A matrix approach to tomographic reconstruction and its implementation on GPUs,” \textit{Journal of Structural Biology}, vol. 170, no. 1, pp. 146–151, 2010.
\item B. Liu, M. Wang, H. Foroosh, M. Tappen, and M. Pensky, “Sparse convolutional neural networks,” in \textit{Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition}, 2015, pp. 806–814.
\item S. Shi and X. Chu, “Speeding up convolutional neural networks by exploiting the sparsity of rectifier units,” \textit{arXiv preprint arXiv:1704.07724}, 2017.
\item W. Wen, Y. He, S. Rajbhandari, W. Wang, F. Liu, B. Hu, Y. Chen, and H. Li, “Learning intrinsic sparse structures within long short-term memory,” \textit{arXiv preprint arXiv:1706.05027}, 2017.
\item X. Sun, X. Ren, S. Ma, and H. Wang, “meProp: Sparsified back propagation for accelerated deep learning with reduced overfitting,” in \textit{Proceedings of the 34th International Conference on Machine Learning-Volume 70}. JMLR. org, 2017, pp. 3299–3308.
\item S. Shi, Q. Wang, K. Zhao, Z. Tang, Y. Wang, X. Huang, and X. Chu, “A distributed synchronous SGD algorithm with global top-k sparsification for low bandwidth networks,” in \textit{2019 IEEE 39th International Conference on Distributed Computing Systems (ICDCS)}. IEEE, 2019, pp. 2238–2247.
\item S. Narang, G. Diamos, S. Sengupta, and E. Olsen, “Exploring sparsity in recurrent neural networks,” \textit{arXiv preprint arXiv:1704.05119}, 2017.
\item V. Volkov and J. W. Demmel, “Benchmarking GPUs to tune dense linear algebra,” in \textit{High Performance Computing, Networking, Storage and Analysis}, 2008. SC 2008. International Conference for. IEEE, 2008, pp. 1–11.
\item X. Chu, K. Zhao, and M. Wang, “Practical random linear network coding on GPUs,” in \textit{International Conference on Research in Networking}. Springer, 2009, pp. 573–585.
\item R. Nath, S. Tomov, and J. Dongarra, “An improved MAGMA GEMM for Fermi graphics processing units,” \textit{The International Journal of High Performance Computing Applications}, vol. 24, no. 4, pp. 511–515, 2010.
\item K. Matsumoto, N. Nakasato, T. Sakai, H. Yahagi, and S. G. Sedukhin, “Multi-level optimization of matrix multiplication for GPU-equipped systems,” \textit{Procedia Computer Science}, vol. 4, pp. 342–351, 2011.
\item J. Kurzak, S. Tomov, and J. Dongarra, “Autotuning GEMM kernels for the fermi GPU,” \textit{IEEE Transactions on Parallel and Distributed Systems}, vol. 23, no. 11, pp. 2045–2057, 2012.
\item J. Lai and A. Szecsi, “Performance upper bound analysis and optimization of SGMEM on Fermi and Kepler GPUs,” in \textit{Proceedings of the 2013 IEEE/ACM International Symposium on Code Generation and Optimization (CGO)}. IEEE Computer Society, 2013, pp. 1–10.
\item A. Abdelfattah, A. Haidar, S. Tomov, and J. Dongarra, “Performance, design, and autotuning of batched GEMM for GPUs,” in \textit{International Conference on High Performance Computing}. Springer, 2016, pp. 21–38.
\item X. Zhang, G. Tan, S. Xue, J. Li, K. Zhou, and M. Chen, “Understanding the GPU microarchitecture to achieve bare-metal performance tuning,” in \textit{Proceedings of the 22nd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming}. ACM, 2017, pp. 31–43.
\item D. Yan, W. Wang, and X. Chu, “Demystifying tensor cores to optimize half-precision matrix multiply,” in \textit{2020 IEEE International Parallel and Distributed Processing Symposium, IPDPS 2020}. Rio de Janeiro, Brazil, May 20-24, 2019. IEEE, 2020.
\item C. Liu, Q. Wang, X. Chu, and Y.-W. Leung, “G-CRS: GPU accelerated cauchy reed-solomon coding,” \textit{IEEE Transactions on Parallel and Distributed Systems}, vol. 29, no. 7, pp. 1484–1498, 2018.
\item J. Dongarra, “Compressed row storage,” \textit{Templates for the Solution of Algebraic Eigenvalue Problems: A Practical Guide}, Z. Bai, J. Demmel, J. Dongarra, A. Ruhe, and H. van der Vorst, Eds. \textit{Philadelphia: SIAM}, 2000.
\item G. Ortega, F. Vázquez, I. García, and E. M. Garzón, “FastSpMM: An efficient library for sparse matrix matrix product on GPUs,” \textit{The Computer Journal}, vol. 57, no. 7, pp. 968–979, 2013.
\item C. Yang, A. Buluc, and J. D. Owens, “Design principles for sparse matrix multiplication on the GPU,” in \textit{International European Conference on Parallel and Distributed Computing (Euro-Par)}, 2018.
\item M. Parger, M. Winter, D. Mlakar, and M. Steinberger, “spECK: accelerating GPU sparse matrix-matrix multiplication through lightweight analysis,” in \textit{Proceedings of the 25th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming}, 2020, pp. 362–375.
\item P. Jiang, C. Hong, and G. Agrawal, “A novel data transformation and execution strategy for accelerating sparse matrix multiplication on GPUs,” in \textit{Proceedings of the 25th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming}, 2020, pp. 376–388.
\item N. Bell and M. Garland, “Implementing sparse matrix-vector multiplication on throughput-oriented processors,” in \textit{Proceedings of the conference on high performance computing networking, storage and analysis}. ACM, 2009, pp. 1–8.
\item D. Merrill and M. Garland, “Merge-based parallel sparse matrix-vector multiplication,” in \textit{Proceedings of the International Conference for High
[26] S. Williams, A. Waterman, and D. Patterson, “Roofline: an insightful visual performance model for multicore architectures,” *Communications of the ACM*, vol. 52, no. 4, pp. 65–76, 2009.

[27] K.-H. Kim, K. Kim, and Q.-H. Park, “Performance analysis and optimization of three-dimensional FDTD on GPU using roofline model,” *Computer Physics Communications*, vol. 182, no. 6, pp. 1201–1207, 2011.

[28] E. Konstantinidis and Y. Cotronis, “A quantitative roofline model for GPU kernel performance estimation using micro-benchmarks and hardware metric profiling,” *Journal of Parallel and Distributed Computing*, vol. 107, pp. 37–56, 2017.

[29] X. Mei and X. Chu, “Dissecting GPU memory hierarchy through microbenchmarking,” *IEEE Transactions on Parallel and Distributed Systems*, vol. 28, no. 1, pp. 72–86, 2017.

[30] X. Mei, K. Zhao, C. Liu, and X. Chu, “Benchmarking the memory hierarchy of modern GPUs,” in *IFIP International Conference on Network and Parallel Computing*. Springer, 2014, pp. 144–156.

[31] H.-V. Dang and B. Schmidt, “The sliced COO format for sparse matrix-vector multiplication on CUDA-enabled GPUs,” *Procedia Computer Science*, vol. 9, pp. 57–66, 2012.

[32] C. Nvidia. “Programming guide,” 2010.

[33] T. A. Davis and Y. Hu, “The university of florida sparse matrix collection,” *ACM Transactions on Mathematical Software (TOMS)*, vol. 38, no. 1, p. 1, 2011.

[34] J. L. Greathouse and M. Daga, “Efficient sparse matrix-vector multiplication on GPUs using the CSR storage format,” in *Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis*. IEEE Press, 2014, pp. 769–780.

[35] K. Hou, W.-c. Feng, and S. Che, “Auto-tuning strategies for parallelizing sparse matrix-vector (SpMV) multiplication on multi-and many-core processors,” in *Parallel and Distributed Processing Symposium Workshops (IPDPSW), 2017 IEEE International*. IEEE, 2017, pp. 713–722.

[36] G. Greiner and R. Jacob, “The I/O complexity of sparse matrix dense matrix multiplication,” in *Latin American Symposium on Theoretical Informatics*. Springer, 2010, pp. 143–156.

[37] M. Bader and A. Heinecke, “Cache oblivious dense and sparse matrix multiplication based on Peano curves,” in *Proceedings of the PARA*, vol. 8, 2008.

[38] S. Ezouaoui, Z. Mahjoub, L. Mendili, and S. Selmi, “Performance evaluation of algorithms for sparse-dense matrix product,” in *Proceedings of the International MultiConference of Engineers and Computer Scientists*, vol. 1, 2013.

[39] P. Koanantakool, A. Azad, A. Buluç, D. Morozov, S.-Y. Oh, L. Oliker, and K. Yelick, “Communication-avoiding parallel sparse-dense matrix-matrix multiplication,” in *Parallel and Distributed Processing Symposium, 2016 IEEE International*. IEEE, 2016, pp. 842–853.