Reducing T-count with the ZX-calculus

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Reducing the number of non-Clifford quantum gates present in a circuit is an important task for efficiently implementing quantum computations, especially in the fault-tolerant regime. We present a new method for reducing the number of T-gates in a quantum circuit based on the ZX-calculus, which matches or beats previous approaches to T-count reduction on the majority of our benchmark circuits in the ancilla-free case, in some cases yielding up to 50% improvement. Our method begins by representing the quantum circuit as a ZX-diagram, a tensor network-like structure that can be transformed and simplified according to the rules of the ZX-calculus. We then show that a recently-proposed simplification strategy can be extended to reduce T-count using a new technique called phase teleportation. This technique allows non-Clifford phases to combine and cancel by propagating non-locally through a generic quantum circuit. Phase teleportation does not change the number or location of non-phase gates and the method also applies to arbitrary non-Clifford phase gates as well as gates with unknown phase parameters in parametrised circuits. Furthermore, the simplification strategy we use is powerful enough to validate equality of many circuits. In particular, we use it to show that our optimised circuits are indeed equal to the original ones. We have implemented the routines of this paper in the open-source library PyZX.

Keywords: Quantum Circuit Optimisation, T-count Optimisation, ZX-calculus, Phase Polynomials, Local Complementation and Pivoting

1 Introduction

Quantum circuits give a simple, universal language for describing quantum computations at a low level. It is often useful when studying circuits to distinguish between two kinds of primitive operations: Clifford gates and non-Clifford gates. Circuits consisting only of Clifford gates can be efficiently classically simulated [1], and can be implemented in a fault-tolerant manner with relative ease within many quantum error correcting codes such as the surface code [31, 22]. However, achieving universality requires at least one non-Clifford gate, such as the \( T \) gate. While techniques such as magic state distillation and injection allow for fault-tolerant implementation of \( T \) gates, they typically require an order of magnitude more resources than Clifford gates [12]. Hence, minimisation of non-Clifford gates within a circuit is of paramount importance to fault-tolerant quantum computation.

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There are methods for computing exact-optimal solutions to the problem of T-count minimisation, but they do so at the cost of an exponential running time \cite{7, 17}. To date, the most successful scalable approaches to T-count minimisation have been based on phase polynomials. Such methods rely on an efficient representation of circuits consisting of just CNOT and Z-phase gates in terms of their action on basis states. The first heuristic method for efficiently reducing T-count and T-depth using this representation, called Tpar, was introduced by Amy et al in Ref. \cite{6}. The results of that paper were later improved upon in Ref. \cite{8} and \cite{21} by exploiting equivalences between the phase polynomial optimisation problem and other known hard problems: respectively, least-distance Reed-Muller decoding, and least-rank factorisation of certain 3-tensors.

Phase-polynomial methods share the limitation that they cannot deal directly with arbitrary quantum circuits. In particular, an arbitrary circuit will also contain Hadamard gates, which destroy the phase polynomial structure. Na"i"vely, one can simply cut the circuit into Hadamard-free sections and apply the optimisation locally. This can be significantly improved by preprocessing to produce larger Hadamard-free sections: either by simple gate transformations \cite{2, 28} or introducing ancillae and classical control \cite{21}.

While these approaches introduce various tricks and refinements, they share a reliance on phase polynomials as a common core. In this paper, we propose a new approach to reducing non-Clifford gate count based on the theoretical framework laid out in Ref. \cite{18}. We first transform a circuit into a special kind of tensor network called a ZX-diagram \cite{14, 15}. This diagram is then subject to a collection of graphical transformation rules called the ZX-calculus \cite{9}. By breaking the rigid circuit structure, ZX-diagrams are then subject to simplifications that have no circuit analogue.

It was noted in Ref. \cite{18} that non-Clifford phases (i.e. angles which are not multiples of $\pi/2$) form an obstruction to the simplification. To overcome this issue, we introduce one crucial refinement to the simplification procedure: the gadgetization of non-Clifford phases. By splitting a node containing a phase into two parts consisting of the node itself, and a new phase gadget, phases can propagate non-locally through a ZX-diagram and potentially cancel or combine with each other. In the case where there are no Hadamard gates in the circuit, these gadgets correspond to phase-parity terms in the representation of a phase polynomial, hence this non-local propagation can be seen as a generalisation of phase polynomial techniques to general circuits.

After performing a combination of phase-gadgetization, simplification, and phase-gadget cancellation, we can use a variation on the technique described in Ref. \cite{18} to re-extract a quantum circuit from the ZX-diagram with fewer non-Clifford phases. Alternatively, we can exploit the fact that our simplification procedure is completely parametric in non-Clifford phase angles to do something more lightweight: rather than combining two phase-gadgets into one, we can simply let the angle from one phase gadget ‘jump’ onto the other one: $(\alpha_i, \alpha_j) \rightarrow (\alpha_i + \alpha_j, 0)$. Since this doesn’t have any effect on the graphical structure of the ZX-diagram, performing this modification to the phases of the original circuit will result in a new circuit that reduces to the same ZX-diagram as before. As a consequence, the new circuit is provably equivalent to the old one.

Hence, rather than re-extracting a circuit from a ZX-diagram, we use it as a tool for discovering phases that can be shifted around non-locally without changing the computed unitary. We call this technique phase teleportation. A pleasant property of phase teleportation, as opposed to the simplify-and-extract method, is that it leaves the structure of the quantum circuit completely intact, only changing the parameters. Hence, 2-qubit gate count is never increased and gates are always applied between the same pairs of qubits as before. As pointed out in Ref. \cite{28}, this could be advantageous when the circuit has been
designed with limited qubit connectivity of the physical qubits in mind. Both optimisation routines are implemented in the open source Python library PyZX [25].

By leaving the circuit model we can sometimes ‘look around’ obstructions such as Hadamard gates to find more optimisations. We see this translated in our results. In benchmark circuits with an abundance of Hadamard gates we can significantly outperform previous methods.

We also use the simplification routine for ZX-diagrams to validate equality of circuits. We do this by composing the adjoint of the optimised circuit with the original circuit and checking whether our simplification routine reduces the resulting ZX-diagram to the identity. While this method cannot detect errors in a circuit, the set of rewrite rules forms a certificate of equality when it does reduce a circuit to the identity. While the general problem of circuit equality validation is QMA-hard [11], and hence a general efficient validation strategy is unlikely to exist, our method is powerful enough to validate equality of our optimised circuits as well as those produced in Ref. [28].

It should be noted that we target ancilla-free optimisation and compare ourselves to the best known results for ancilla-free T-count reduction. It is already known that the required amount of T gates can decrease when ancillae are allowed [6]. Ref. [21] obtains lower T-counts on many of the circuits we consider by introducing ancillae via a technique called Hadamard gadgetization. Using a hybrid of our approach and more advanced phase polynomial techniques, we can obtain ZX-diagrams which in principle exhibit very low T-counts, but re-extracting a quantum circuit from the ZX-diagram becomes an obstacle, and will almost certainly require introducing ancillae. This remains an open problem, which we will discuss in more detail in Section 3.

Note: A few days after the first version of this paper appeared as a preprint [26], Zhang and Chen reported nearly identical numbers to those in Table 1, using an independent approach based on Pauli rotations [33]. It is a topic of ongoing research as to why these seemingly quite different methods produce the same T-counts.

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2 Results

Our procedure simplifies quantum circuits formed from the following primitive set of gates:

$$\begin{align*}
\text{CNOT} &:= \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix} & \quad Z_\alpha &:= \begin{pmatrix} 1 & 0 \\ 0 & e^{i\alpha} \end{pmatrix} & \quad H &:= \frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix}
\end{align*}$$

(1)

with the goal of reducing the total number of gates of the form $Z_\alpha$ where $\alpha \neq k \cdot \frac{\pi}{2}$ for $k \in \mathbb{Z}$. For all of the benchmark circuits, all of those gates are $T := Z_{\pi/4}$, so from hence forth, we will simply refer to this number as the T-count.

The four main steps of our procedure are depicted in Fig. 1 and described in detail in Section 4. If a circuit has gates which are not in the gate set (1) (as in Fig. 1a), we
| Circuit            | $n$ | $T$ | Best prev. | Method    | PyZX | PyZX+TODD |
|--------------------|-----|-----|------------|-----------|------|----------|
| adder$_8$ [3]     | 24  | 399 | 213        | RM$_{m}$ | 173  | 167      |
| Adder$_8$ [27]    | 23  | 266 | 56         | NRSCM    | 56   | 56       |
| Adder$_{16}$ [27] | 47  | 602 | 120        | NRSCM    | 120  | 120      |
| Adder$_{32}$ [27] | 95  | 1274| 248        | NRSCM    | 248  | 248      |
| Adder$_{64}$ [27] | 191 | 2618| 504        | NRSCM    | 504  | 504      |
| barenco-tof$_3$ [27] | 5   | 28  | 16         | T$_{par}$| 16   | 16       |
| barenco-tof$_4$ [27] | 7   | 56  | 28         | T$_{par}$| 28   | 28       |
| barenco-tof$_5$ [27] | 9   | 84  | 40         | T$_{par}$| 40   | 40       |
| barenco-tof$_{10}$ [27] | 19  | 224 | 100        | T$_{par}$| 100  | 100      |
| tof$_3$ [27]      | 5   | 21  | 15         | T$_{par}$| 15   | 15       |
| tof$_4$ [27]      | 7   | 35  | 23         | T$_{par}$| 23   | 23       |
| tof$_5$ [27]      | 9   | 49  | 31         | T$_{par}$| 31   | 31       |
| tof$_{10}$ [27]   | 19  | 119 | 71         | T$_{par}$| 71   | 71       |
| csla-mux$_3$ [27] | 15  | 70  | 58         | RM$_{r}$ | 62   | 45       |
| csla-mux$_9$ [27] | 30  | 196 | 76         | RM$_{r}$ | 84   | 72       |
| cycle$_{173}$ [3] | 35  | 4739 | 1944      | RM$_{m}$ | 1797 | 1797     |
| gf($2^1$)-mult [27] | 12  | 112 | 56         | TODD     | 68   | 52       |
| gf($2^2$)-mult [27] | 15  | 175 | 90         | TODD     | 115  | 86       |
| gf($2^3$)-mult [27] | 18  | 252 | 132        | TODD     | 150  | 122      |
| gf($2^4$)-mult [27] | 21  | 343 | 185        | TODD     | 217  | 173      |
| gf($2^5$)-mult [27] | 24  | 448 | 216        | TODD     | 264  | 214      |
| ham$_{15}$-low [3] | 17  | 161 | 97         | T$_{par}$| 97   | 97       |
| ham$_{15}$-med [3] | 17  | 574 | 230        | T$_{par}$| 212  | 212      |
| ham$_{15}$-high [3] | 20  | 2457 | 1019      | T$_{par}$| 1019 | 1013     |
| hwbs$_8$ [3]      | 7   | 105 | 75         | T$_{par}$| 75   | 72       |
| mod-mult-55 [27]  | 9   | 49  | 28         | TODD     | 35   | 20       |
| mod-red-21 [27]   | 11  | 119 | 73         | T$_{par}$| 73   | 73       |
| mod$_{54}$ [27]   | 5   | 28  | 16         | T$_{par}$| 8    | 7        |
| nth-prime$_6$ [3] | 9   | 567 | 400        | RM$_{mkr}$ | 279  | 279      |
| nth-prime$_8$ [3] | 12  | 667 | 4045       | RM$_{mkr}$ | 4047 | 3958     |
| qcla-adder$_{10}$ [27] | 36  | 589 | 162        | T$_{par}$| 162  | 158      |
| qcla-com$_{7}$ [27] | 24  | 203 | 94         | RM$_{m}$ | 95   | 91       |
| qcla-mod$_7$ [27] | 26  | 413 | 235$^a$    | NRSCM    | 237  | 216      |
| re-adder$_6$ [27] | 14  | 77  | 47         | RM$_{mkr}$| 47   | 47       |
| vbe-adder$_3$ [27] | 10  | 70  | 24         | T$_{par}$| 24   | 24       |

Table 1: Benchmark circuits. The columns $n$ and $T$ contain the amount of qubits and T gates in the original circuit. Best prev. is the previous best-known ancilla-free T-count for that circuit and Method specifies which method was used: RM$_{m}$ and RM$_{r}$ refer to the maximum and recursive Reed-Muller decoder of Ref. [8], T$_{par}$ is Ref. [6], TODD is Ref. [21] and NRSCM refers to Ref. [28]. PyZX and PyZX+TODD specify the T-counts produced by the procedures outlined in the Methods section. Numbers shown in bold are better than previous best, and italics are worse. The superscript (a) indicates an error in a previously reported T-count. The error was found using Amy's Feynman tool [4].
first expand those gates in terms of CNOT, H, and T gates and translate that circuit into a ZX-diagram (Fig. 1b). We then apply the simplification procedure described in Section 4.4 to obtain a reduced ZX-diagram (Fig. 1c). Finally, we use the data about corresponding phases obtained from this simplification to perform phase teleportation in the original circuit to reduce T-count (Fig. 1d).

For our benchmarks, we have used all of the Clifford+T benchmark circuits from Refs. [6, 28], minus some of the larger members of the $\text{gf}(2^n)\text{-mult}$ family. These benchmark circuits were also used in Refs. [8, 21] and include components that are likely to be of interest to quantum algorithms, such as adders or Grover oracles. Of these 36 benchmark circuits, we are at or improving upon the state of the art for 26 circuits (≈72%), and we improve on the state of the art on 6 (≈17%). If we apply some simple post-processing afterwards and feed the resulting circuit into the TODD phase polynomial optimiser [21], we improve on the state of the art for 20 circuits (≈56%). These two methods seem to complement each other well in the ancilla-free regime, obtaining significantly better numbers than either of the two methods alone, and matching or beating all other methods for every circuit tested. These results are given in Table 1.

We achieve an identical T-count to the previously best-known result for 20 of the 36 circuits. This is interesting, since the methods we use are quite different from previous methods. As a result this can be seen as evidence that those T-counts exist in some kind of ‘local optimum’, at least in the ancilla-free case. The circuits where PyZX seems to do considerably better are ones that contain many Hadamard gates. The fact that PyZX achieves improvements when there are many Hadamard gates is as expected, as most other successful methods employ a dedicated phase-polynomial optimiser [6, 8, 28, 21] that is hampered by the existence of Hadamard gates. On the other hand, the only circuits where phase polynomial techniques significantly out-perform our methods are in the $\text{gf}(2^n)\text{-mult}$ family. After some simple pre-processing, these circuits have almost no Hadamard gates, hence they are very well-suited to phase polynomial techniques.

It should be noted that while the circuits of Table 1 are all written in the Clifford+T gate set, our optimisation routine is agnostic to the values of the non-Clifford phases. We have also tested our routine on the quantum Fourier transform circuits of Ref. [28] that include more general non-Clifford phases, and in each case found that our non-Clifford gate count exactly matched their results.

The optimisation routines are implemented in the open source Python library PyZX [25].
All circuit optimisations were run on a consumer laptop. Our method took a few seconds to run for most circuits, with some of the bigger ones taking up to a few minutes. We tested the correctness of the optimisation by generating the matrix of the original and the optimised circuit for thousands of small randomly generated circuits and checking equality, in addition to doing the same for the smaller benchmark circuits. We can also use the ZX-calculus for verification of equality [13]. For all benchmark circuits, we composed the original circuit with the adjoint of the optimised one, and then ran our simplification routine on this circuit. In every case, the resulting circuit was reduced to the identity. Since the set of rewrites needed to do this is vastly different then the ones used to produce the original optimised circuit, this is strong evidence that the optimised circuit is correct, as it is very unlikely that an error in our rewrites would cancel itself in this way. With the same validation scheme we have also verified correctness of all the optimised benchmark circuits of Ref. [28], except for qcla-mod, which was then shown to be incorrect using the Feynman tool [4].

3 Discussion

We have implemented a novel quantum circuit optimisation routine that uses ZX-diagrams to go beyond the rigid structure of the circuit model. This routine matches or beats the previous best-known T-count for the majority of the benchmark circuits we have tested. We have furthermore shown that combining our routine with the TODD compiler [21] achieves T-counts that are better than either of these methods separately. Finally, our simplification routine is powerful enough to validate the correctness of our optimised circuits.

There are quite a few ways in which our routine can be improved or be made more versatile. Our method currently does not affect the amount of CNOT or Hadamard gates in the circuit. This is because we are not actually making use of the simplified ZX-diagram to extract a new circuit, but we are simply using this diagram to track cancellation of phase gates. It is possible to extract a circuit directly from the ZX-diagram produced by our routine, but at this stage such a circuit often contains more gates than we started out with. For future work, an obvious direction then is to improve our circuit extraction methods to produce better circuits directly from the ZX-diagrams.

Our method currently only supports ancilla-free optimisation. It has been shown [6, 21] that allowing additional ancillae can greatly decrease the required T-count. A promising approach to introducing ancillae into our simplification procedure is the following. We can treat the reduced ZX-diagram as a phase polynomial circuit, where every non-input corresponds to introducing an ancilla in the $|+$ state and every non-output corresponds to projecting (i.e. post-selecting) onto $|+$. Indeed we can transform it into a circuit of this form using the $(f)$ rule of the ZX-calculus (cf. Section 4.1):
The middle part of the right-hand side can be described as a phase polynomial (cf. Section 4.3), and hence can be further reduced by powerful phase polynomial techniques such as Reed-Muller decoding [8] or 3-tensor factorisation [21]. The resulting circuit contains post-selection and cannot be realised deterministically in general. However, in Ref.[18], we showed that, if certain graph-theoretic constraints are respected, these interior vertices (i.e. ancillae) can always be eliminated. However, phase polynomial techniques typically break those constraints, so it is an interesting open problem to see if deterministic computation can still be recovered, possibly by introducing measurements and classical control.

While the ZX-calculus forms a powerful language for reasoning about low-level gate sets (e.g. Clifford+T), it can only reason about Toffoli and CCZ gates in an indirect manner, by first translating those gates into Clifford+T representations. The ZH-calculus [10] in contrast, makes it straightforward to reason about mid-level quantum gates such as Toffoli and CCZ gates. It then stands to reason that we can achieve further optimisations for circuits defined in terms of these mid-level gates (such as adders and classical oracles), by first doing simplifications in the ZH-calculus, then translating the diagram into a Clifford+T gate set, and doing further simplifications in the ZX-calculus.

It was already noted in the introduction that our simplification is completely parametric in non-Clifford phase angles. Indeed we show the correctness of the phase teleportation routine in Section 4.5 by working on a representation of a circuit where all non-Clifford angles are replaced with free parameters. The procedure itself then proceeds by combining and eliminating some parameters. An immediate consequence is that our simplification procedure generalises from concrete circuits to parametrised circuits, where the analogue of T-count reduction is elimination of redundant free parameters. This could potentially yield significant improvements in the performance of hybrid classical/quantum algorithms relying on parametrised circuits, such as the quantum variational eigensolver [30].

One final open question concerns the power of our circuit equality validation scheme, using the ZX-calculus simplifier. We have already noted that this scheme seems to be powerful enough to validate any optimisation made by our simplification routine or the one found in Ref. [28]. It is then an interesting question to explore the exact power (and limitations) of this scheme.

4 Methods

In this section we will explain our main contributions in depth, namely how to do T-count optimisation using the ZX-calculus. On a high level this proceeds in the following way:

- First we translate a quantum circuit into a ZX-diagram. See Section 4.1.
- We apply the diagrammatic simplification procedure \textit{ZX-simplify} laid out in Sections 4.2-4.4.
- Finally, by keeping track of certain simplification steps, and how they affect phases in the original circuit, we will decrease the T-count of the circuit by means of phase teleportation. See Section 4.5.

Section 4.6 explains our how our PyZX-produced circuit is combined with post-processing and the TODD compiler.

4.1 Background: the ZX-calculus

We will provide a brief overview of the ZX-calculus. For an in-depth reference see Ref. [16].
The ZX-calculus is a diagrammatic language similar to the familiar quantum circuit notation. A **ZX-diagram** (or simply **diagram**) consists of **wires** and **spiders**. Wires entering the diagram from the left are **inputs**; wires exiting to the right are **outputs**. Given two diagrams we can compose them by joining the outputs of the first to the inputs of the second, or form their tensor product by simply stacking the two diagrams.

Spiders are linear operations which can have any number of input or output wires. There are two varieties: $Z$ spiders depicted as green dots and $X$ spiders depicted as red dots:

\[
\begin{align*}
\begin{array}{c}
\vdots \\
\vdots \\
\end{array}
\end{align*}
\begin{align*}
\begin{array}{c}
\vdots \\
\vdots \\
\end{array}
&:=|0\cdots0\rangle\langle0\cdots0|+e^{i\alpha}|1\cdots1\rangle\langle1\cdots1| \\
\begin{array}{c}
\vdots \\
\vdots \\
\end{array}
&:=|+\cdots+\rangle\langle+\cdots+|+e^{i\alpha}|-\cdots-\rangle\langle-\cdots-|
\end{align*}
\]

The diagram as a whole corresponds to a linear map built from the spiders (and permutations) by the usual composition and tensor product of linear maps. As a special case, diagrams with no inputs represent (unnormalised) state preparations.

**Example 4.1.** We can immediately write down some simple state preparations and unitaries in the ZX-calculus:

\[
\begin{align*}
\begin{array}{c}
\vdots \\
\vdots \\
\end{array}
&=|0\rangle+|1\rangle \propto |+\rangle \\
\begin{array}{c}
\vdots \\
\vdots \\
\end{array}
&=|0\rangle\langle0|+e^{i\alpha}|1\rangle\langle1| = Z_\alpha \\
\begin{array}{c}
\vdots \\
\vdots \\
\end{array}
&=|\rangle\langle+|+e^{i\alpha}|-\rangle\langle-| = X_\alpha
\end{align*}
\]

In particular we have the Pauli matrices:

\[
\begin{align*}
\begin{array}{c}
\vdots \\
\vdots \\
\end{array}
&= Z \\
\begin{array}{c}
\vdots \\
\vdots \\
\end{array}
&= X
\end{align*}
\]

It will be convenient to introduce a symbol – a yellow square – for the Hadamard gate. This is defined (up to a global phase) by the equation:

\[
\begin{align*}
\begin{array}{c}
\vdots \\
\vdots \\
\end{array}
&= \frac{1}{\sqrt{2}}(2)
\end{align*}
\]

We will often use an alternative notation to simplify the diagrams, and replace a Hadamard between two spiders by a blue dashed edge, as illustrated below.

Both the blue edge notation and the Hadamard box can always be translated back into spiders when necessary. We will refer to the blue edge as a **Hadamard edge**.

Two diagrams are considered **equal** when one can be deformed to the other by moving the vertices around in the plane, bending, unbending, crossing, and uncrossing wires, as long as the connectivity and the order of the inputs and outputs is maintained. Equivalently, a ZX-diagram can be considered as a graphical depiction of a tensor network, as in e.g. [29]. Then, just like any other tensor network, we can observe that the interpretation of a ZX-diagram is unaffected by deformation. As tensors, $Z$ and $X$ spiders can be written

\[
\begin{align*}
\begin{array}{c}
\vdots \\
\vdots \\
\end{array}
&\text{Z spiders will appear lightly-shaded and X darkly-shaded.}
\end{align*}
\]

If you are reading this document in monochrome or otherwise have difficulty distinguishing green and red, $Z$ spiders will appear lightly-shaded and $X$ darkly-shaded.
as follows:

\[
(\alpha)_{j_1...j_n}^{i_1...i_m} = \begin{cases}
1 & \text{if } i_1 = ... = i_m = j_1 = ... = j_n = 0 \\
\epsilon^{i\alpha} & \text{if } i_1 = ... = i_m = j_1 = ... = j_n = 1 \\
0 & \text{otherwise}
\end{cases}
\]

\[
(\alpha)_{j_1...j_n}^{i_1...i_m} = \frac{1}{\sqrt{2}} \begin{cases}
1 + \epsilon^{i\alpha} & \text{if } i_1 \oplus ... \oplus i_m \oplus j_1 \oplus ... \oplus j_n = 0 \\
1 - \epsilon^{i\alpha} & \text{if } i_1 \oplus ... \oplus i_m \oplus j_1 \oplus ... \oplus j_n = 1 
\end{cases}
\]

where all \(i_\alpha, j_\beta\) range over \(\{0, 1\}\).

In addition to simple deformations, ZX-diagrams satisfy a set of equations called the ZX-calculus. There exists several variations of the ZX-calculus. The set of rules we will use is presented in Figure 2. Diagrams that can be transformed into each other using the rules of the ZX-calculus correspond to equal linear maps (up to normalisation). ZX-diagrams with arbitrary angles are expressive enough to represent any linear map \[15\]. It is often useful to consider Clifford ZX-diagrams, by analogy to Clifford circuits, where all angles are restricted to multiples of \(\pi/2\). In that case, the rules given in Figure 2 are complete with respect to linear map equality \[9\]. That is, if two Clifford ZX-diagrams describe the same linear map, one can be transformed into the other using the rules in Figure 2. Extensions of the calculus exist that are complete for larger families of ZX-diagrams/maps, including Clifford+T ZX-diagrams \[23\], where phases are multiples of \(\pi/4\), and arbitrary ZX-diagrams where any phase is allowed \[19, 24, 32\].

Quantum circuits can be translated into ZX-diagrams in a straightforward manner. We will take as our starting point circuits constructed from the following universal set of gates:

\[
\text{CNOT} := \begin{pmatrix}
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 0 & 1 \\
0 & 0 & 1 & 0
\end{pmatrix}, \quad
Z_\alpha := \begin{pmatrix}
1 & 0 \\
0 & \epsilon^{i\alpha}
\end{pmatrix}, \quad
H := \frac{1}{\sqrt{2}} \begin{pmatrix}
1 & 1 \\
1 & -1
\end{pmatrix}
\]

This gate set admits a convenient representation in terms of spiders:

\[\text{CNOT} = \quad Z_\alpha = \quad H = \]

(3)

Note that for the CNOT gate, the green spider is the first (i.e. control) qubit and the red spider is the second (i.e. target) qubit. Other common gates can easily be expressed in terms of these gates. In particular, \(S := Z_{\pi/2}, T := Z_{\pi/4}\) and:

\[X_\alpha = \quad \text{CZ} = \quad = \]

(4)
Definition 4.2. A ZX-diagram is graph-like when:

1. All spiders are Z-spiders.
2. Z-spiders are only connected via Hadamard edges.
3. There are no parallel Hadamard edges or self-loops.
4. Every input or output is connected to a Z-spider and every Z-spider is connected to at most one input or output.

In Ref. [18] it is shown that any ZX-diagram can efficiently be transformed into a graph-like ZX-diagram using the rules of the ZX-calculus. This transformation essentially amounts to turning all X spiders into Z spiders with the \((h)\) rule, fusing as many spiders together as possible with \((f)\), and removing parallel edges/self-loops with the following derived rules:

\[
\begin{align*}
\alpha _1 & = \alpha _1 + \pi \\
\alpha _n & = \alpha _n + \pi \\
\end{align*}
\]  

(5)

In particular, the number of non-Clifford phases in a diagram is never increased, and can actually be decreased by the \((f)\) rule, as phases are added together. We call this graph-like because the resulting ZX-diagram is essentially an indirected, simple graph whose vertices are labelled by phase angles.

4.2 Clifford simplification of ZX-diagrams

A spider connected to an input or an output is called a boundary spider, whereas all other spiders are called interior spiders. If we interpret an \(N\)-qubit circuit as a ZX-diagram, there are precisely \(N\) inputs and \(N\) outputs, hence there are at most \(2N\) boundary spiders. On the other hand, there will in general be a very large number of interior spiders.

The main idea behind the first part of our simplification strategy is to remove as many interior Clifford spiders, i.e. spiders whose phase is a multiple of \(\pi/2\), as possible. We do this by using two rewrite rules based on the graph-theoretic operations of local complementation and pivoting. For the proof of correctness of these rewrite rules we refer to Ref. [18].

The first rule, based on local complementation, deletes a spider with a phase of \(\pm \pi/2\) and introduces edges between all of its neighbours:

\[
\begin{align*}
\alpha _1 & = \alpha _1 - \pi \\
\end{align*}
\]  

(6)

\[\text{LC}\]
Since parallel edges vanish (cf. equations (5)), this can be seen as complementing the set of edges connecting the neighbours of the deleted vertex, hence the name.

The second rule deletes pairs of Pauli spiders, i.e. spiders whose phase is a multiple of $\pi$. For a pair of connected Pauli spiders $u, v$, we can split the neighbourhood of $\{u, v\}$ into three pieces: $U$ the spiders only connected to $u$, $V$ the spiders only connected to $v$, and $W$, the spiders connected to both. We can then delete the pair of spiders $u, v$ provided we introduce complete bipartite graphs on $(U, W)$, $(V, W)$ and $(U, V)$:

\[
\begin{align*}
\alpha_1 + k\pi \\
\alpha_n + k\pi \\
\beta_1 + (j+k+1)\pi \\
\beta_n + (j+k+1)\pi \\
\gamma_1 \\
\gamma_n \\
\end{align*}
\]

Again, thanks to (5), this can be seen as complementing the sets of edges present in the three bipartite graphs $(U, W)$, $(V, W)$ and $(U, V)$.

Since the rules $(LC)$ and $(P1)$ both delete at least one spider, we can simply apply them repeatedly until no rule matches. This gives us a terminating procedure for simplifying our diagram. Note that we do not target the spiders in any specific order. Different orders of application will yield different diagrams (i.e. these rules are not confluent), but we always obtain the same amount of non-Clifford spiders at the end.

At this point, the simplification procedure in Ref. [18] employs a variation of $(P1)$ to remove a few more Pauli spiders and terminates. In particular, nothing is done to eliminate non-Clifford spiders. This is the goal of the next 2 sections.

### 4.3 Phase gadgets

We first introduce a new concept for ZX-diagrams: a phase gadget. A phase gadget is simply an arity-1 spider with angle $\alpha$, connected via a Hadamard edge to a spider with no angle:

Phase gadgets are a useful tool for working with ZX-diagrams corresponding to unitaries. For example, the diagram

\[
\text{phase gadget} \begin{array}{c}
\alpha \\
\vdots
\end{array}
\]

yields an $n$-qubit unitary $U$ defined by:

\[
U :: |x_1, ..., x_n\rangle \mapsto e^{i\alpha(x_1 \oplus ... \oplus x_n)} |x_1, ..., x_n\rangle
\]

In fact, it is straightforward to show concretely (or in the ZX-calculus) that this unitary is equal to a ladder of CNOT gates, followed by a single phase gate, followed by the reverse
ladder of CNOT gates. For example, on 4 qubits:

\[ \alpha = \alpha = \alpha \quad (9) \]

Since these gates are diagonal in the computational basis, they commute with each other. This also follows straightforwardly from the \((\mathcal{Z})\) rule:

\[ \alpha = \beta = \beta \]

Arbitrary diagonal unitaries, i.e. unitaries of the form:

\[ U :: |x_1, x_2, x_3, x_4\rangle \mapsto e^{i f(x_1, x_2, x_3, x_4)} |x_1, x_2, x_3, x_4\rangle \]

for some \( f : \{0, 1\}^n \rightarrow \mathbb{R} \), can easily be expressed in terms of phase gadgets. For example:

\[ |x_1, x_2, x_3, x_4\rangle \mapsto e^{i \left( \frac{\pi}{4} x_1 \oplus x_4 + \frac{\pi}{8} x_2 \oplus x_1 - \frac{\pi}{4} x_1 \oplus x_3 \right)} |x_1, x_2, x_3, x_4\rangle \]

In fact, the angles appearing in the phase gadgets correspond to the Fourier expansion\(^2\) of the semi-boolean function \( f \). That is, we can express any function \( f : \{0, 1\}^n \rightarrow \mathbb{R} \) as follows:

\[ f(x) = \alpha + \sum_{\vec{y}} \alpha_{\vec{y}} (x_1 y_1 \oplus \ldots \oplus x_n y_n) \quad (10) \]

where \( \vec{x}, \vec{y} \in \{0, 1\}^n \) and \( \alpha, \alpha_{\vec{y}} \in \mathbb{R} \). In the context of diagonal unitaries, \( \alpha \) yields a global phase (which we ignore), and each \( \alpha_{\vec{y}} \) corresponds to a phase gadget.

Phase polynomial techniques perform transformations on the function \( f \) in order to reduce the T-count needed to implement \( U \) (or some \( U' \) that is Clifford-equivalent to \( U \)). In the sequel, we will consider not just phase gadgets arising from unitaries such as (8), but phase gadgets appearing in arbitrary graph-like ZX-diagrams. Hence, our simplification procedure can be seen as a generalisation of phase polynomial techniques.

**4.4 Full simplification of ZX-diagrams**

In this section, we will introduce rules that reduce the number of non-Clifford spiders in the ZX-diagram, and hence the T-count in the resulting circuit.

\(^2\)A brief discussion of the form (10), and its relation to the usual Fourier transform of a semi-boolean function, can be found in the appendix of Ref. [5].
First, it is worth noting that the \( (P1) \) rule from section 4.2 was only able to remove an interior Pauli spider adjacent to another interior Pauli spider. We can now introduce two variations of this rule, \( (P2) \) and \( (P3) \), which together allow us to remove any remaining interior Pauli spider, at the cost of introducing a phase gadget.

\[
\alpha \beta = \alpha + \beta \quad (ID)
\]

\[
\alpha \beta = \alpha + \beta \quad (GF)
\]

We apply \( (P2) \) when the interior Pauli spider is connected to any other interior spider, while \( (P2) \) is applied when it is connected to some boundary spider. Applying these rules to every remaining interior Pauli spider yields a diagram where every internal spider is either non-Clifford or part of a phase-gadget. If the phase-gadget is Clifford, then it can be removed by either \( (P1) \) or by two applications of \( (LC) \). Hence we can reduce to a case where all phase-gadgets are non-Clifford.

We can now apply the following two rules, which both strictly decrease the number of non-Clifford spiders:

When a phase gadget is connected to exactly one other spider, its phase can be combined with the phase on that spider via \( (ID) \). This is essentially an application of the rules \( (i1) \) and \( (i2) \).

When two phase gadgets are connected to exactly the same set of spiders, they can be fused into one via the gadget-fusion rule \( (GF) \). This rule can be shown using the ZX-calculus.

\[
\alpha \beta = \alpha + \beta \quad (GF)
\]
where \((b')\) is the \(n\)-ary generalisation of the rule \((b)\), which follows from the other rules (see e.g. [16], §9.4). For unitaries of the form \((8)\), it corresponds to a well-known simplification used in phase-polynomial circuits, where two phases acting on the same parity of the input qubits can be summed together.

Each of the rewrite rules \((ID)\) and \((GF)\) removes a non-Clifford spider, and transforms another non-Clifford spider into a Clifford spider, which can be removed by one of the previous rules. We can now fully describe our simplification procedure for graph-like ZX-diagrams.

**Algorithm 4.3. ZX-simplify:** Starting with a graph-like ZX-diagram, do the following:

1. Apply \((LC)\) until all interior proper Clifford vertices are removed.
2. Apply \((P1)\), \((P2)\) and \((P3)\) until all interior Pauli vertices are removed or transformed into phase-gadgets.
3. Remove all Clifford phase-gadgets using \((LC)\) and \((P1)\).
4. Apply \((ID)\) and \((GF)\) wherever possible. If any matches were found, go back to step 1, otherwise we are done.

This algorithm always terminates as every step either removes a spider or a phase-gadget. In terms of complexity we see that if the original diagram had \(n\) spiders, that this algorithm takes at most \(n\) steps. Each step might need us to toggle the connectivity of all the neighbours of the involved spider. As this spider has at most \(n\) neighbours, this could involve \(n^2\) operations on the diagram. The complexity of the algorithm is therefore bounded above by \(O(n^3)\) elementary graph operations. In practice though, the ZX-diagrams resulting from quantum circuits will be quite sparse, and we tend to see a time scaling roughly between \(O(n)\) and \(O(n^2)\) on our benchmark circuits.

It will be useful to have a name for the diagrams produced by this simplification procedure.

**Definition 4.4.** We say a graph-like ZX-diagram is in *reduced gadget form* when

- Every internal spider is a non-Clifford spider or part of a non-Clifford phase-gadget.
- Every phase-gadget has more than one target.
- No two phase-gadgets have the same set of targets.

### 4.5 Phase teleportation

The simplification procedure described in the previous section produces a ZX-diagram which does not look at all like a circuit. In order to get a new, simplified circuit out, we could apply (a variation of) the circuit extraction procedure described in Ref. [18]. Alternatively, we can short-circuit the extraction using a trick we refer to as phase teleportation.

We begin by replacing every non-Clifford phase in our starting circuit \(C\) with a fresh variable name, \(\alpha_1, \ldots, \alpha_n\), and storing the angles in a separate table \(\tau : \{1, \ldots, n\} \rightarrow \mathbb{R}\).

We can then perform the simplification procedure described in the previous section symbolically. That is, we work on a ZX-diagram whose spiders are labelled not just with phase angles, but with polynomials over the variables \((\alpha_1, \ldots, \alpha_n)\).
Then, consider what happens when two variables are added together during the \((\text{ID})\) and \((\text{GF})\) rules. One of two things can occur: (a) the two variables have the same sign or (b) they have different signs:

\[
\begin{align*}
\alpha_i + \alpha_j + P & \quad \rightarrow \quad \pm (\alpha_i + \alpha_j) + P + Q \\
\alpha_i + P & \quad \rightarrow \quad \pm \alpha_i + P \\
\alpha_j + Q & \quad \rightarrow \quad \pm \alpha_j + Q \\
\alpha_i - \alpha_j & \quad \rightarrow \quad \pm (\alpha_i - \alpha_j) + P + Q
\end{align*}
\]

Since none of our simplifications will copy any of the variables we started with, these are the only occurrences of \(\alpha_i\) and \(\alpha_j\) in the ZX-diagram. Hence, in case (a), if we replace \(\alpha_i\) with \(\alpha_i + \alpha_j\) and \(\alpha_j\) with 0, we get an equivalent diagram.

Put another way, in case (a), we can update our table \(\tau\) by setting \(\tau'(i) := \tau(i) + \tau(j)\), \(\tau'(j) := 0\), and \(\tau'(k) := \tau(k)\) for \(k \notin \{i, j\}\). Then, \((C, \tau)\) and \((C, \tau')\) describe circuits which are provably equivalent by the rules of ZX-calculus. Case (b) is similar, except we should set \(\tau'(i) := \tau(i) - \tau(j)\).

This observation yields the following algorithm:

**Algorithm 4.5. Phase teleportation:** Staring with a circuit, do the following:

1. Choose unique variables \(\alpha_1, \ldots, \alpha_n\) for each non-Clifford phase and store the pair \((C, \tau)\), where \(C\) is the parametrised circuit and \(\tau: \{1, \ldots, n\} \rightarrow \mathbb{R}\) assigns each variable to its phase.

2. Interpret \(C\) as a ZX-diagram and run the **ZX-simplify** algorithm on the simplified diagram while doing the following:

   Whenever \((\text{ID})\) or \((\text{GF})\) are applied to a pair of vertices or phase-gadgets containing variables \(\alpha_i\) and \(\alpha_j\), respectively, update the phase table \(\tau\) as described for cases (a) and (b) above.

3. When **ZX-simplify** finishes, the pair \((C, \tau')\) describes an equivalent circuit.

Even though we do compute the reduced gadget form of the circuit \(C\), the new circuit we output has the same structure as \(C\) itself, but with some of the phases changed. As a result, no new gates are introduced, but many non-Clifford phase gates will have their angles set to 0 or to multiples of \(\pi/2\). Hence, running a dedicated gate minimising circuit optimisation routine afterwards will often be much more effective.

### 4.6 Circuit optimisation and TODD

We now briefly describe a combined optimisation routing consisting of first running the phase teleportation procedure, then doing some simple post-processing, and finally applying the **TODD** algorithm described in Ref. [21].

The circuit post-processing works by doing forward and backward passes through the circuit. During the forward pass, we commute 1-qubit gates as far forward as possible using standard gate commutation rules, cancelling and combining gates whenever we can.
We then take the adjoint of the circuit and repeat the process, and keep repeating the process until no more gates are removed.

We then apply the ancilla-free version of the TODD algorithm using the C++ tool Topt [20]. This tool is designed to optimise CNOT+Phase circuits, so we first cut our circuit into Hadamard-free chunks. Then, before running Topt on each chunk, we again use standard gate commutation laws to pull as many gates as possible from neighbouring chunks into the current one. Since Topt is non-deterministic, we run it multiple times and we take the best result. Running Topt on each chunk in this manner then yields the T-counts reported in the last column of Table 1.

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