Radiation-enhanced channel length modulation induced by trapped charges in buried oxide layer

Xin Xie¹,²,³,a), Huilong Zhu¹,², Mengying Zhang¹,², Dawei Bi¹, Zhiyuan Hu¹, Zhengxuan Zhang¹, and Shichang Zou¹

Abstract By skillfully applying the voltage bias, we firstly observed radiation-enhanced channel length modulation (CLM) of main transistor in 130 nm partially-depleted SOI nMOSFETs. And we found the radiation-enhanced CLM under Pass-Gate bias is more severe than that under ON bias, which reveals that the radiation-induced positive trapped charges in buried oxide is more responsible for this effect. A partially full depletion model is used to interpret this effect. And a TCAD simulation was used to verify our model. Good agreement between simulation and experiment is demonstrated.

key words: buried oxide (BOX), channel length modulation (CLM), partially-depleted (PD), silicon-on-insulator (SOI), total-ionizing-dose (TID), trapped charge

Classification: Electron devices

1. Introduction

Silicon-on-insulator (SOI) technology has become a mainstream commercial technology for its advantages of high speed, low power consumption, high integration, and latch-up effect immunity, etc. It has also been developed for radiation-hardened applications due to single event upset immunity, which benefits from fully dielectric isolation of shallow trench isolation (STI) and buried oxide (BOX) [1, 2]. However, the thick buried oxide induces more complicated total ionizing dose (TID) effect, which has been studied in numerous papers [3, 4, 5, 6, 7, 8, 9, 10, 11]. With the scale decreasing, the short channel effects emerge [12, 13]. Typically, the channel length decreases as drain voltage increases, which is known as channel length modulation (CLM) [12, 14]. It induces the uptrend of drain current in saturation region and decreases alternating current (AC) output resistance [15]. Hence, channel length modulation can greatly reduce the performance of integrated circuit. The influence of radiation on short channel effects was firstly studied by G.U. Youk et al. [16], and they found the radiation-enhanced short channel effects. Then Zhi-yuan Hu et al. [17] analyzed off-state leakage of STI sidewall channel and found the radiation enhanced channel-length modulation effect in STI sidewall parasitic transistors, which was also verified by Xue Wu et al. [18]. However, previous studies only focus on STI sidewall parasitic transistors. The radiation-enhanced CLM effect of the main transistor has not been observed. In fact, there are many other kinds of short channel effects [12, 19], such as hot-carrier degradation, velocity saturation effect, drain induced barrier lowering (DIBL). It is difficult to distinguish the CLM phenomenon of main transistor. Especially, the main transistor has high drain current. Self-heating of main transistor is very serious, which offsets the uptrend of drain current induced by CLM effect [20, 21].

In this paper, we skillfully applied voltage bias to weaken hot-carrier degradation, velocity saturation effect, DIBL, and self-heating, and firstly observed radiation-enhanced CLM effect of main transistor in deep submicron partially-depleted (PD) SOI devices. Different irradiation biases (Pass-Gate bias and ON bias) are compared. The mechanism of radiation-enhanced CLM effect is analyzed and verified by TCAD simulation.

2. Experimental details

The PDSOI devices in this paper are fabricated in 130 nm process technology. The SOI wafer is 200 nm diameter UNIBOND® wafer from SOITEC corporation. The thickness of top Si film and BOX are 100 nm and 145 nm, respectively. STI is applied for isolation. Body contact is introduced by T-Gate layout as shown in Fig. 1. The average body doping concentration (N_a) is about 4.7×10¹⁷ cm⁻³. The thickness of gate oxide is 6 nm and operating voltage (V_DD) is 3.3 V. The input/output (I/O) NMOS devices with different channel lengths (W/L=10 μm/10 μm, 10 μm/1.2 μm, 10 μm/0.7 μm, 10 μm/0.35 μm) are selected. All samples are 24-pin DIP ceramic packaged. Radiation experiments were carried out in Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy of Sciences. The radiation source is ⁶⁰Co γ-ray with dose rate 100 rad(Si)/s. Pass-Gate (PG) bias (source

¹State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050
²University of Chinese Academy of Sciences, Beijing 100049
³Science and Technology on Reliability Physics and Application Technology of Electronic Component Laboratory, Guangzhou 510610

a) xiexin@mail.sim.ac.cn

DOI: 10.1587/eleex.16.20190454
Received July 17, 2019
Accepted September 17, 2019
Publicized October 15, 2019

Copyright © 2019 The Institute of Electronics, Information and Communication Engineers
and drain are biased at 3.3 V, others are grounded) and ON bias (front gate is biased at 3.3 V, others are grounded) were used during radiation exposure. Characteristics of devices were measured by a Keithley 4200B parameter analyzer at room temperature before irradiation and after irradiation up to 30 krad(Si), 50 krad(Si), 100 krad(Si). All measures were taken within half an hour to avoid anneal effect. To be clear, we always defined the source voltage as the reference voltage (0 V). $V_{ds}$, $V_{gs}$, $V_{hs}$, $V_{pks}$ correspond to drain, front gate, body, and substrate (back gate) biases, respectively.

![Fig. 1: The layout of T-gate PDSOI I/O nMOSFETs.](image)

**3. Results and Discussion**

Fig. 2 is the $I_d - V_{ds}$ characteristics of devices with different channel lengths at $V_{gs} = 0.8$ V and $V_{ds} = 0.1$ V. $V_{ds}$ is applied below 1 V to weaken velocity saturation effect, DIBL, self-heating, and to avoid kink effect [22, 23]. Actually, from Fig. 3, we can find that the DIBL effect occurs when $V_{ds} > 1.9$ V. This drain voltage is far higher than what we set in our experiment. Hence, we keep a safe region for device to avoid DIBL effect. The $V_{ds}$ we set can also suppresses impact ionization, because electrons need acquire more than about 1.5 eV of energy to impact ionizing [24, 25]. Furthermore, from Fig. 4, we can clearly see that there is no big body current when $V_{ds} < 1.1$ V, which means there is no impact ionization since the body current is proportional to the impact ionization [26, 27]. However, the CLM effect is also weakened under low drain voltage bias. For compensating, gate is biased at 0.8 V, close to threshold voltage $V_{th}$. In Fig. 2, we can find that the drain current of short-length devices shows more significant uptrend in saturation region than the drain current of long-length devices. This exhibits CLM effect. By comparing the drain current of device at different TID levels, we observed that drain current in saturation region rise more significantly as the dose level increases. This reveals that radiation can enhance the CLM effect.

As is known, the drain current can be expressed as [15]:

$$I_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 (1 + \lambda V_{ds}).$$  \hspace{1cm} (1)

where $\mu_n$ is electron mobility, $C_{ox}$ is gate oxide capacitance per unit area, $W$ and $L$ are channel width and channel length, respectively. And $\lambda$ in Eq. (1) is the channel-length
modulation coefficient, which is defined by

$$\lambda = \frac{\Delta L}{LV_{ds}}.$$  \hspace{1cm} (2)

Here $\Delta L$ is the length of pinch-off region. Bigger $\lambda$ shows more severe CLM effect. According to Eq. (1), we can reverse extend the $I_d - V_{ds}$ curve in saturation region and extract the voltage (denoted by $V_f$) at the intersection of the extended line and abscissa axis. The $\lambda$ is gotten by $\lambda = -1/V_f$. Fig. 5 is the $\lambda$ extracted from Fig. 2. Short devices show bigger $\lambda$, which indicate that short devices suffer worse CLM effect. As for same devices, higher total dose levels show bigger $\lambda$, which reveals radiation-enhanced CLM effect. You may notice that the $\lambda$ of the device with 0.35 $\mu$m channel length decreases at 100 Krad(Si) dose level. This will be discussed later.

Different irradiation biases (PG bias and ON bias) are compared. Fig. 6 shows the channel-length modulation coefficient $\lambda$ of nMOSFET with 0.35 $\mu$m channel length under PG bias and ON bias. The $\lambda$ under PG bias is bigger than that under ON bias, which reveals that irradiation under PG bias induces more significant radiation-enhanced CLM effect. According to previous study [28], irradiation under PG bias induces more trapped charges in the BOX, whereas irradiation under ON bias induces more trapped charges in the BOX near the source/drain-body junctions. The silicon film near source/drain-body junction will be fully depleted due to light body concentration, whereas the center part of silicon film will keep neutral. That is to say, partially full depletion occurs. As a result, the channel above full depletion region will be influenced by the trapped charge in the BOX. The surface potential ($\Phi_s$) of the channel above full depletion region can be expressed as Eq. (3) [12], where $\Phi_{MS}$ and $\Phi_{MS, bg}$ are the front and back work function differences, respectively; $Q_{ox}$ and $Q_{ox, bg}$ are the fixed charge density at the front and back silicon/oxide interfaces, respectively;
Fig. 7: The non-uniform distribution of radiation-induced trapped charges in BOX and generated electric field. The dash lines are build-in electric field under PG bias and the solid lines are electric field induced by trapped charges.

$C_{ox}$ and $C_{ox, bg}$ are the front and back gate oxide capacitances, respectively; $C_{si} = \varepsilon_{si}/t_{si}$ is the silicon capacitance; $Q_{depl} = -qN_{at}t_{si}$ is the total depletion charges in the silicon film. As TID increases, $Q_{ox, bg}$ will have an increment

$$\Delta Q_{ox, bg} = Q_f = q(N_{at} - N_{it}) > 0,$$

where $Q_f$ is the density of net trapped charges in the BOX; $N_{at}$ is the density of BOX trapped charges and $N_{it}$ is the density of interface traps. Hence, $\Phi_{s1}$ will increase

$$\Delta \Phi_{s1} = \frac{Q_f}{(1 + \frac{C_{ox}}{C_{si}})(C_{ox, bg} + C_{si}) - C_{si}} > 0. \tag{5}$$

That is to say, the electric field of trapped charges in the BOX will elevate the surface potential of the channel near to drain. When a high voltage is applied on drain, drain voltage can more easily penetrate into channel and increase the length of pinch-off region ($\Delta L$), leading to more severe CLM effect.

Fig. 8: simulated potential distribution and electric field direction of device with $L = 0.35 \mu m$ (a) before irradiation and after (b) 30 krad(Si), (c) 50 krad(Si), (d) 100 krad(Si). The biases are: $V_{bs} = V_{bgs} = V_{ds} = 0 \ V$, $V_{gs} = 0.8 \ V$. The white lines show the depletion regions.

However, the $\lambda$ of the device with $W/L = 10 \mu m/0.35 \mu m$ decreases at 100 krad(Si) TID level in Fig. 5. This phenomenon can be explained as self-heating effect [20, 31, 32]. The temperature increment induced by self-heating effect in SOI can be described as:

$$\Delta T = \frac{R_{th}I_dV_{ds}}{C_TWL}V_{ds} \tag{6}$$

where $R_{th} = (kT_{BOX})/(C_TWL)$ is the thermal resistance. Here, $k$ is a constant; $t_{BOX}$ and $C_T$ are the thickness and the thermal conductivity of BOX. Since the device with $L = 0.35 \mu m$ has larger drain current of unit width at 100 krad(Si) TID level, the $\Delta T$ is higher. Hence, the device with $L = 0.35 \mu m$ suffers more severe self-heating effect. The self-heating effect offsets some increment of drain current and hence decreases the $\lambda$.

Fig. 9: (a) simulated surface potential $\Phi_{s1}$ and (b) differences of simulated surface potential $\Delta \Phi_{s1} (= \Phi_{s1, irradiation} - \Phi_{s1, pre})$ along the channel $x$ of device with $L = 0.35 \mu m$ at bias: $V_{bs} = V_{bgs} = 0 \ V$, $V_{ds} = 1 \ V$, $V_{gs} = 0 \ V$ and 0.8 V.

In order to verify the theoretical analysis, TCAD simulations are performed. To imitate TID effect of devices, extra positive charges are placed at the top interface of silicon and BOX. The density of positive charge is calibrated by experimental $I_d - V_{bg}$ curves. This simulation method is the same as [33]. Fig. 8 shows the simulated potential, electric field, and depletion regions of device with $L = 0.35 \mu m$ at $V_{gs} = 0.8 \ V$. The depletion regions increase with TID,
however no full depletion but partially full depletion occur. These are fully compatible with our model. Fig. 9 is the simulated surface potential and the differences of the simulated surface potential along the channel of device with $L = 0.35 \mu \text{m}$ at bias: $V_{ds} = 1 \text{V}$, $V_{gs} = 0 \text{V}$ and 0.8 V. When $V_{gs} = 0 \text{V}$, the surface potential of the channel near drain rises, but the potential barrier between source and drain does not decreases obviously. This reveals that the electric field of trapped charges in the BOX elevates the surface potential of the channel near to drain, but not induces DIBL effect. When $V_{gs} = 0.8 \text{V}$, the surface potential of the channel near drain rises more obviously. This demonstrates that the trapped charges in the BOX enhances the effect of drain voltage penetrating into channel. In Fig. 9, the pinch-off positions which are estimated by saturation voltage ($V_{gs} - V_{th}$) are marked as red squares. As the trapped charges in the BOX increase, the pinch-off positions shift left, which are in agreement with the radiation-enhanced CLM effect. Fig. 10 is the comparison between simulated and experimental $I_d - V_{ds}$ characteristics. The experimental data and simulated data are very close. And the simulated $\lambda$ increases with TID. These are generally in agreement with experimental phenomena.

![Figure 10: simulated and experimental $I_d - V_{ds}$ characteristics of nMOSFETs with $W/L = 10 \mu \text{m}/0.35 \mu \text{m}$ at different TID levels.](image)

4. Conclusion

Radiation-enhanced channel length modulation of main transistor in 130 nm PDSOI I/O nMOSFETs is observed. As the total ionizing dose level increases, the drain current in saturation region increases more significant, which reveals radiation-enhanced channel length modulation. Different irradiation biases are compared. The radiation-enhanced channel length modulation under PG bias is more severe than that under ON bias, which reveals the radiation-induced trapped charges in the BOX is more responsible for this effect. A partially full depletion model is used to interpret the radiation-enhanced channel length modulation. Radiation-induced positive trapped charges in the BOX fully deplete silicon film near drain and elevate the surface potential of the channel near drain. As a result, drain voltage penetrates into channel more easily, which broadens the pinch-off region and enhances channel length modulation.

However, at high total ionizing dose level or high drain current, the CLM effect of short device is covered up due to severe self-heating effect. This means the radiation-enhanced channel length modulation is a effect at low total ionizing dose level.

To make circuits more reliable in radiation environments, radiation-enhanced CLM needs to be considered, and low saturation voltage is not recommended.

Acknowledgments

This work was supported by the Opening Project of Science and Technology on Reliability Physics and Application Technology of Electronic Component Laboratory [grant numbers ZHD201702].

References

[1] J. R. Schwank, et al.: “Radiation effects in SOI technologies,” IEEE Transactions on Nuclear Science, 50 (2003) 522 (DOI: 10.1109/tns.2003.812930).

[2] E. Simoen, et al.: “Radiation effects in advanced multiple gate and silicon-on-insulator transistors,” Ieee Transactions on Nuclear Science, vol. 60, no. 3, pp. 1970-1991, Jun 2013. DOI: 10.1109/tns.2013.2255313.

[3] H. J. Barnaby: “Total-ionizing-dose effects in modern CMOS technologies,” IEEE Transactions on Nuclear Science, 53 (2006) 3103 (DOI: 10.1109/tns.2006.885952).

[4] T. R. Oldham and F. B. McLean: “Total ionizing dose effects in MOS oxides and devices,” IEEE Transactions on Nuclear Science, 50 (2003) 483 (DOI: 10.1109/tns.2003.812927).

[5] J. R. Schwank, et al.: “Radiation effects in MOS oxides,” IEEE Transactions on Nuclear Science, 55 (2008) 1833 (DOI: 10.1109/tns.2008.2001040).

[6] Q. W. Zheng, et al.: “Enhanced total ionizing dose hardness of deep sub-micron partially depleted silicon-on-insulator n-type metal-oxide-semiconductor field effect transistors by applying larger back-gate voltage stress,” Chinese Physics Letters, 31 (2014) 3 (DOI: 10.1088/0256-3071/s/31/1216101).

[7] Y. Zhang, et al.: “Investigation of unique total ionizing dose effects in 0.2um partially-depleted silicon-on-insulator technology,” Nuclear Instruments & Methods in Physics Research Section a Accelerators Spectrometers Detectors and Associated Equipment, 745 (2014) 128 (DOI: 10.1016/j.nima.2014.01.052).

[8] C. Peng, et al.: “Total-ionizing-dose induced coupling effect in the 130-nm PDSOI I/O nMOSFETs.”
IEEE Electron Device Letters, **35** (2014) 503 (DOI: 10.1109/led.2014.2311453).

[9] H. Huang, et al.: “Investigation of the total dose response of partially depleted SOI nMOSFETs using TCAD simulation and experiment,” Microelectronics Journal, **45** (2014) 759 (DOI: 10.1016/j.mejo.2014.04.027).

[10] B. X. Ning, et al.: “Comprehensive study on the TID effects of 0.13 μm partially depleted SOI nMOSFETs,” Microelectronics Journal **44** (2013) pp (DOI: 10.1016/j.mejo.2012.09.004).

[11] H. Huang, et al.: “Total dose irradiation-induced degradation of hysteresis effect in partially depleted silicon-on-insulator nMOSFETs,” IEEE Transactions on Nuclear Science, **60** (2013) 1354 (DOI: 10.1109/tns.2013.2239660).

[12] J.-P. Colinge: *Silicon-on-insulator technology: Materials to VLSI* (Kluwer Academic Publishers, New York, 2004) 3rd ed. 167.

[13] M. Conti and C. Turchetti: “n the short-channel theory for MOS transistor,” IEEE Transactions on Electron Devices, **38** (1991) 2657 (DOI: 10.1109/16.158687).

[14] S. M. Sze and M.-K. Lee: *Semiconductor devices physics and technology* (John Wiley & Sons, America, 2012) 3rd ed. 195.

[15] B. Razavi: *Design of analog CMOS integrated circuits* (McGraw-Hill, New York, 2001) 25.

[16] G. U. Youk, et al.: “Influence of channel length on total ionizing dose effect in deep submicron technologies,” Acta Physica Sinica, **61** (2012) 050702 (DOI: 10.7498/aps.61.050702).

[17] X. Wu, et al.: “Influence of channel length and layout on TID for 0.18 μm NMOS transistors,” Nuclear Science and Techniques, **24** (2013) 060202 (DOI: 10.13538/j.1001-8042/nst.2013.06.019).

[18] A. Chaudhry, M. J. Kumar: “Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: A review,” IEEE Transactions on Device and Materials Reliability, **4** (2004) 99 (DOI: 10.1109/tdmar.2004.824359).

[19] Y. H. Cheng and T. A. Fjeldly: “Unified physical I-V model including self-heating effect for fully depleted SOI/MOSFETs,” IEEE Transactions on Electron Devices, **43** (1996) 1291 (DOI: 10.1109/16.506782).

[20] T. A. Karatsori, et al.: “Analytical compact model for lightly doped nanoscale ultrathin-body and BOX SOI MOSFETs with back-gate control,” IEEE Transactions on Electron Devices, **62** (2015) 3117 (DOI: 10.1109/led.2015.2464076).

[21] C. Peng, et al.: “Enhanced radiation sensitivity in short-channel partially depleted silicon-on-insulator n-type metal-oxide-semiconductor field effect transistors,” Chinese Physics Letters, **30** (2013) 098502 (DOI: 10.1088/0256-307x/30/9/098502).

[22] Yuhua. and C. Hu: MOSFET modeling & BSIM3 user’s guide (Kluwer Academic Publishers, New York, 2002) 44.

[23] C. M. Hu, et al.: “Hot-electron-induced MOSFET degradation - model, monitor, and improvement,” IEEE Trans-