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Low Cost Autonomous Lock-In Amplifier for Resistance/Capacitance Sensor Measurements

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Abstract: This paper presents the design and experimental characterization of a portable high-precision single-phase lock-in instrument with phase adjustment. The core consists of an analog lock-in amplifier IC prototype, integrated in 0.18 µm CMOS technology with 1.8 V supply, which features programmable gain and operating frequency, resulting in a versatile on-chip solution with power consumption below 834 µW. It incorporates automatic phase alignment of the input and reference signals, performed through both a fixed −90° and a 4-bit digitally programmable phase shifter, specifically designed using commercially available components to operate at 1 kHz frequency. The system is driven by an Arduino YUN board, thus overall conforming a low-cost autonomous signal recovery instrument to determine, in real time, the electrical equivalent of resistive and capacitive sensors with a sensitivity of 16.3 µV/Ω @ ε_{rS} < 3% and 37 kV/F @ ε_{rS} < 5%, respectively.

Keywords: lock-in amplifiers; phase shift adjustment; programmable circuits; low-cost sensors; real time monitoring; Arduino

1. Introduction

Device miniaturization has been key to the development of innovative sensing technology with application in different fields [1], ranging from biology and medicine [2,3], to environmental monitoring [4–6], or limnology and civil structural monitoring [7–9]. Therefore, the interest in new large scale integrated systems including sensing technology is growing substantially, since they make it possible to carry out the same analysis usually performed by traditional sophisticated equipment but with the advantage of reduced size, power, and cost.

However, according to each application, different challenges are faced in the achievement of high performance low-voltage low-power (LVLP) miniaturized solutions, not only in terms of the sensing element but also in the necessary electronic instrumentation: the measurement system must adequately perform the sensor signal acquisition to recover the target information preserving accuracy and reliability, with real-time operation, portability, and through an intuitive and friendly interface to make it accessible to different users [2].

One of the main concerns in the acquisition system is the low amplitude sensor signal, often buried in high noise levels interfering with the whole detection, so a suitable recovery technique such as lock-in amplification is required [10]. A lock-in amplifier (LIA) is based on phase-sensitive detection (PSD), where the signal of interest (V_{IN}, f_0) is multiplied by a reference signal (V_R) whose frequency is also set at f_0 to perform a synchronous detection; the resulting signal is low-pass filtered with a
suitable corner frequency to recover a DC component proportional to the amplitude of interest \( [10,11] \), according to:

\[
V_{\text{OUT, DC}} = 2AV_{\text{IN}} \cos \theta/\pi + V_{\text{dd}}/2, \quad (1)
\]

where \( A \) is the voltage gain of the LIA, \( \theta \) is the \( V_{\text{IN}} - V_R \) phase shift, and a square reference signal \( V_R \) is assumed. The term \( V_{\text{dd}}/2 \) is the common-mode voltage reference level for single \( V_{\text{dd}} \) supply systems compatible with battery operation. As the system presents the maximum sensitivity for the in-phase condition \( (\theta = 0^\circ) \), single phase lock-in amplifiers work with input and reference signals operating at the same frequency and in phase.

Commercial LIA equipment is non-portable, bulky and expensive, limiting the test scenario to specialized laboratories \([12–14]\). On the other hand, general purpose commercial integrated solutions of LIAs are almost nil since their building blocks involve specific and rigorous design requirements that cannot always be fully accomplished, presenting inconveniences as no amplification stage, limited resolution and offset susceptibility \([15]\). To solve these setbacks, a few analog LIAs integrated in CMOS technology can be found in the literature, mainly designed for the characterization of different kinds of sensors like magnetic, mechanical, optical or resistive \([16–20]\). However, when conditioning resistive/capacitive sensors with an AC excitation source, issues like phase shift, overheating or decoupling at high frequencies may arise. Both decoupling and overheating can be solved by choosing an appropriate operating frequency, but the phase shifting problem remains \([21,22]\), so a phase adjustment circuit is required. In addition, phase adjustment allows for versatile/generic implementations that can be adapted to different sensors by recalibration and reconfiguration of the operating parameters \([23]\).

The above mentioned integrated solutions consider only the read-out channel, but do not include the signal phase alignment (also called signal synchronization) circuit, which is crucial for the proper operation of the LIA. As a consequence, they require manual adjustment, thus losing autonomy and not being suitable for portable and remote applications. Therefore, it becomes necessary to develop a complete LIA-based recovery system profiting from the advantages of analog integrated prototypes in terms of LVLP and reduced size, while also including automatic phase alignment with a low-cost hardware efficient approach, so as to obtain a truly portable high-precision autonomous instrument \([2]\).

This paper addresses the implementation of such an instrumentation board, based on an analog integrated lock-in amplifier \([19]\) that exhibits low power consumption, flexibility due to its programmable gain and operating frequency and small size compared to state-of-art LIAs, being therefore a very competitive choice in terms of large scale reproducibility \([4,5,24]\), with an automatic signal synchronization system driven by an Arduino YUN board which manages all the measurement process and that acts as an intuitive interface between the processing system and the data storage in the PC \([25]\). The result is a complete portable and autonomous single-phase LIA measurement system able to detect low amplitude signals resulting from resistive or capacitive sensors, while at the same time performs an automatic phase shift adjustment independent of the input signal amplitude or its variations with a simpler and more flexible design compared to state-of-art solutions. Additionally, although not presented in this paper, the system can also be used as a dual-phase LIA for complex impedance measurements \([26–28]\), which makes it very versatile and suitable for novel portable applications such as bio-impedance measurements.

The paper is organized as follows. Section 2 describes the proposed system, explaining the operation of its building blocks. Section 3 presents the experimental characterization of the whole system, as well as its validation through the impedance measurement of resistive and capacitive sensors. Finally, conclusions are drawn in Section 4.

2. Proposed Lock-In Architecture

The block diagram of the proposed LIA-based measurement instrument is shown in Figure 1. It consists of two main stages: the in-phase channel \((\text{IP-Channel, } X)\) and the quadrature channel \((\text{Q-Channel, } Y)\), with identical PSD read-out \((\text{LIA}_X, \text{LIA}_Y)\) biased at a single \( V_{\text{dd}} \) and driven by quadrature reference signals \( V_{RX}, V_{RY} \). Each channel includes a Phase Shifter (PS) that adequately
adjusts the phase of the corresponding reference signals \(V_{RX} \) and \(V_{RY}\), sinusoidal), which are next converted by analog Comparators into \(0-V_{dd}\) square signals \(V_{RX} \) and \(V_{RY}\) to perform the synchronous rectification. The DC output voltages \(V_X \) and \(V_Y\) are acquired by the Arduino YUN platform, also in charge of the automatic signal phase alignment task, and finally data are stored in the PC.

The system operation when the information is contained in the signal amplitude is next explained in more detail. A source generator signal \(V_S = A_S \sin(\omega_0 t)\) excites the sensor, typically placed in a voltage divider or a Wheatstone bridge configuration, whose output voltage signal \([19,29]\) constitutes the LIA input \(V_{IN}(t) = V_{IN} \sin(\omega_0 t + \theta)\) for both channels. As reference signals \(V_{RX}, V_{RY}\) are in quadrature, from Equation (1) the output DC voltage of each channel can be written for a general situation as:

\[
V_X = 2AV_{IN} \cos \theta/\pi + V_{dd}/2, \tag{2}
\]

\[
V_Y = 2AV_{IN} \sin \theta/\pi + V_{dd}/2. \tag{3}
\]

Thus, when the DC output signal for the Q-Channel is \(V_{dd}/2\), \(V_{RX}\) and \(V_{IN}\) are either in phase or in counter-phase, and the change in \(V_X\) is maximum for a given input voltage. Both solutions are actually valid operation conditions though, for simplicity, the X-Channel is called the in-phase Channel, as already mentioned.

![Figure 1. Block diagram of the proposed autonomous lock-in amplifier (LIA) System.](image)

To perform phase alignment, the output DC voltage \(V_Y\) in the Q-Channel is detected by the Arduino, which adjusts the Programmable Phase Shifter (PPS) by means of a 4-bit digital word \(B(4) = [b_3, b_2, b_1, b_0]\) until the condition \(V_Y = V_{dd}/2\) is met. Then, the reference signal \(V_{RY}\) in the IP-Channel is shifted \(-90^\circ\) with a fixed PS to produce \(V_{rX}\), and the consequent digital reference signal \(V_{RX}\) drives the PSD through the X-Channel. The maximum contribution of the DC level \(V_X\) proportional to the amplitude of the input signal is thus obtained.

Note that this arrangement with an in-phase and an in-quadrature channel is equivalent to a dual phase LIA, which can recover both the magnitude and phase information, or equivalently the real \((V_X)\) and the imaginary part \((V_Y)\), of electrical impedances \([26]\). Thus, the proposed system can be operated as single-phase LIA with automatic phase alignment, or as a dual phase LIA \([26–28,30–32]\).

### 2.1. Lock-In Amplifier

As shown in Figure 2, the LIA consists of an integrated Current-Mode Instrumentation Amplifier (CMIA) in CMOS 180 nm technology with power supply \(V_{dd} = 1.8\) V. A transconductance amplifier is used to convert the input signal into current, so the phase-sensitive detection is performed in the current domain, resulting in high linearity and reduction in area and power consumption compared with voltage mode implementations \([19,33]\). A Current Divider provides gain programmability to the amplifier, to adjust it as required for the application. Finally, the resulting signal is converted back
into voltage through a transimpedance amplifier (TIA). This integrated CMIA is followed by a voltage buffer implemented with a low cost discrete Operational Amplifier (OA) HA17458 [34] for proper impedance coupling with the output Low Pass Filter (LPF).

The transistor-level schematics of the CMIA building blocks are presented in Figure 3, and briefly described below:

**Transconductor:** The input stage consists of a source degenerated differential pair with a negative feedback $gm$-boosting circuit as shown in Figure 3a. M1 transistors work as source followers, buffering the input signal to the degeneration resistor $R_d$. Thus, the $V_{IN}$ signal is converted into current ($I_{AC} = V_{IN}/R_d$) in a linear way and copied out by loading the $A$ nodes with the output mirror branches with cascode transistors to improve the current copy, resulting in the $I_O$ signal.

**Mixer:** The phase-sensitive detection is performed in the current domain using a class AB current follower; the direction of the current $I_A$ is controlled by the square reference signal $V_R$ connected to the cascode transistors which act as switches. The fully rectified output current is $I_O = (-1)^{VR} \cdot I_O$, with $V_R = (0,1)$.

**Current Divider:** To provide gain programmability to the CMIA, a 3-bit current divider based on an R-2R ladder implemented with PMOS transistors in the triode region was used, achieving a highly linear current-division [35], according to:

$$\Delta = \frac{1}{2^n}[1 + \sum_{j=0}^{n-1} (2^j - d_j 2^j)] \text{ with } n = 3.$$  \hspace{1cm} (4)

**Transimpedance Amplifier:** A single stage differential amplifier with a feedback resistor $R_f = 100 \, k\Omega$ converts back the signal into voltage domain. A compensation capacitor $C_C = 500 \, fF$ is used to ensure stability. The transfer function for the complete CMIA is:

$$\frac{V_{OUT}}{V_{IN}} = (-1)^{VR} R_f \left( \frac{1}{2^n} \sum_{j=0}^{n-1} (2^j - d_j 2^j) \right) \text{ with } n = 3.$$  \hspace{1cm} (5)

It can be seen that the gain depends mainly on the ratio $R_f$ and $R_d$. Thus, both resistors were implemented with a high-resistivity polysilicon layer and will, therefore, suffer the same variations with process and temperature, thus ensuring good accuracy and robustness.

Finally, as shown in Figure 2, to complete the lock-in system, an external LPF was used. It consists of a second order passive RC network with $R = 40 \, k\Omega$ and $C = 300 \, nF$ or $C = 3 \, \mu F$ to set a cutoff frequency of 5 Hz or 0.5 Hz, respectively.
Figure 3. Building blocks of the integrated CMIA: (a) Transconductor; (b) Mixer; (c) Current Divider; (d) Transimpedance Amplifier.

Note that the LIA can process either a single input signal by connecting the minus input terminal to $V_{dd}/2$, or a differential input signal. The prototype was experimentally characterized and used for the detection of small concentrations of carbon monoxide, providing a Dynamic Reserve of 35.5 dB, which indicates that it is capable of recovering a signal submerged in noise levels 60 times higher [19,33]. In fact, the LIA can be seen as a Band-Pass Filter with a very high quality factor $Q = f_0/f_{LP}$, where $f_0$ is the operating frequency and $f_{LP}$ is the LPF cutoff frequency, so it filters most of the noise contributions at frequencies different from that of the signal of interest. It has been chosen over other proposals of the authors [36,37] due to its good features in terms of input dynamic range, resolution, linearity, input referred noise, programmable gain, low power consumption and low integration area, which makes it a versatile and adaptable solution for different applications. Its main characteristics are summarized in Table 1.

Table 1. Summary of CMIA experimental characterization.

| Parameters                  | Integrated CMIA          |
|-----------------------------|--------------------------|
| CMOS Technology             | 180 nm                   |
| Power Supply                | 1.8 V                    |
| Gain                        | 25–42 dB                 |
| Bandwidth                   | 125 kHz                  |
| Input Voltage Range         | 4.5–17 mV                |
| Dynamic Reserve             | 35.5 dB                  |
| Resolution                  | 25 $\mu$V                |
| THD (0.3 $V_{pp}$ at 1 kHz) | $-54.6$ dB               |
| Input referred noise (at 1 kHz) | 5.9 nV/Hz$^{1/2}$      |
| Power Consumption           | 417 $\mu$W               |
| Integrated Area             | 0.013 mm$^2$             |

2.2. Phase Shifter

Phase Shifters provide at their output a replica of the input signal with a phase displacement [38,39]. In our proposal, to perform phase alignment, two phase shifters, one variable (Q-Channel) and one fixed (IP-Channel), are required. Both are based on a simple topology that adjusts the signal phase by means
of a passive element. The PS core topology is the first order OA-based All-Pass Filter (APF) [40, 41] shown in Figure 4a. The phase angle:

$$\theta_{PS} = 180^\circ - 2 \tan^{-1}(2\pi \cdot R_{PS} \cdot C \cdot f_0),$$  

(6)

depends on the passive elements $R_{PS}$ and $C$, as well as on the operation frequency $f_0$. A frequency $f_0 = 1$ kHz was chosen to avoid any contribution of low frequency flicker noise, and because it matches the typical operation frequency of biosensors used to characterize electrodes, organs and tissues, an application field where this portable low-cost approach can provide significant advantages over classical laboratory equipment [19, 28, 42–44].

The sine wave $V_r$ is converted into a square reference signal $V_R$ (Figure 4a) by means of a comparator, which introduces a delay which depends on $f_0$, causing an additional phase shift of $16^\circ$ for $f_0 = 1$ kHz. As a result, the resulting phase angle of the entire adjustment block is:

$$\theta_{VR} = \theta_{PS} - 16^\circ,$$  

(7)

For the IP-Channel, a PS with constant $-90^\circ$ phase shift is required. Therefore, considering Equation (6), $R_1 = 1$ kΩ, $C_1 = 100$ nF and $R_{PS} = 1.25$ kΩ are used. The Q-Channel uses the same values of $R_1$, $C_1$, and the variable resistor $R_{PS}$ presented in Figure 4b, which consists of a programmable R-2R ladder ($R = 10$ kΩ). Through the activation or deactivation of its branches, by means of the 2N2222A BJT transistors [45] acting as switches controlled by a 4-bit digital word $B(4) = \{b_3, b_2, b_1, b_0\}$, the equivalent resistance can be adjusted in an easy and fast way. A larger number of bits leads to a wider tuning phase range with finer tuning steps, but also leads to an increase in the number of components in the R-2R ladder. A 4-bit resolution was chosen to get an adequate phase adjustment with a small amount of components driven by a very simple program.

![Figure 4. (a) Generation of sine and square reference signals with the PPS and Comparator circuits; (b) Programmable Phase Shifter ($R_{PS}$ adjustable).](image)

Simulations were carried out with NI Multisim. A signal $V_S = 100$ mV at 1 kHz was used and the $R_{PS}$ resistance was set to vary from 10 kΩ to 0.63 kΩ, obtaining a phase displacement $\theta_{PS}$ ranging from approximately $18^\circ$ to $137^\circ$ (Figure 5a), so that the overall $\theta_{VR}$ varies from $2^\circ$ to $120^\circ$ for the 4-bit PPS. The conversion of $V_r$ to a square reference signal $V_R$ was also verified by simulation. Figure 5b shows the signals before and after the comparator, where the desired waveform, voltage range (0–1.8 V) and phase adjustment are achieved. Experimentally, both PS and comparators were implemented with discrete dual OA HA17458 [34].
why, for the operation of the system, the Arduino YUN [46] platform was used. It has a microcontroller with digital and analog input/output ports, it is compatible with the technology used, and it is also easy to manage and program, while widely available [47]. That is why, for the operation of the system, the Arduino YUN [46] platform was used. It has a microcontroller with digital and analog input/output ports, it is compatible with the technology used, and it is also easy to manage and program, while widely available [47].

The automation of the phase alignment and measurement processes has the advantage of increasing both speed and reliability, as well as reducing operation costs compared to manual execution [5]. That is why, for the operation of the system, the Arduino YUN [46] platform was used. It has a microcontroller with digital and analog input/output ports, it is compatible with the technology used, and it is also easy to manage and program, while widely available [47].

As for the programming, constants and variables for measurement and control are first defined, and inputs/outputs (I/O) are assigned. Next, the phase shift control word is initialized to \( B(4) = [1, 1, 1, 0] \) to set \( \theta_{VR} = +90^\circ \), and the output of both channels is recorded. If phase alignment is needed, i.e., if \( V_Y \neq V_{dd}/2 \), a cycle begins in which \( B(4) \) is initialized to \( [0, 0, 0, 0] \) and increased to adjust the phase shift provided by the PPS, until the quadrature condition is reached at the output of \( Q\text{-Channel} \). Then, the system finishes the phase tuning step and the measurement process begins: with the last saved value of \( B(4) \), the data of \( IP \) and \( Q \text{ Channels} \) \((V_X \text{ and } V_Y)\) are recorded. The flow chart of the program is detailed in Figure 6.

![Figure 5](image_url)  
Figure 5. Simulation of Phase Shifter as a function of resistor \( R_{PS} \): (a) \( V_r \) signal; (b) \( V_r \) and \( V_R \) signals.

Note that it is necessary to design the passive elements \((R_{PS} \text{ or } C)\) based on the target frequency. This is why, for a general purpose instrument, the PS implementation is externally done through commercially available components, but for a specific application operating at a given frequency, a fully integrated solution can be considered.

2.3. Phase Alignment and Data Transmission Interface

The automation of the phase alignment and measurement processes has the advantage of increasing both speed and reliability, as well as reducing operation costs compared to manual execution [5]. That is why, for the operation of the system, the Arduino YUN [46] platform was used. It has a microcontroller with digital and analog input/output ports, it is compatible with the technology used, and it is also easy to manage and program, while widely available [47].

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![Figure 6](image_url)  
Figure 6. Flow chart of the Arduino program to perform the phase alignment step and the sensing measurements.
3. Experimental Results

3.1. Autonomous Lock-In Performance

The whole system board is shown in Figure 7a. It incorporates two integrated CMIAs in CMOS technology, discrete components and the Arduino YUN. The system has a silicon area of 0.026 mm$^2$ and PCB area of $10 \times 14$ cm$^2$, constituting a solution easily transportable and cheap to implement. The integrated system uses $V_{dd} = 1.8$ V, discrete components (OA) use 3.3 V power supply, while BJT transistors are turned on/off with 5 V from the Arduino platform. Figure 7b shows the laboratory equipment used to perform the experimental characterization: a Keysight E3611A power supply, Keithley 2602 Source Meter Unit (SMU), Tektronix 4104 Oscilloscope and a computer using Universal Serial Bus (USB) for data transfer with Arduino.

Note that the Arduino microcontroller limits the resolution to 4.9 mV (10 bits from ground to 5V). As the resolution of the integrated CMIAs is 25 µV [33], a microcontroller of the Microchip group such as the PIC24FJ128GC010 with 16-bit ADC or equivalent could be used to increase the resolution of the LIA to 55 µV.

Figure 7. Photograph of experimental setup: (a) Test PCB; (b) Laboratory equipment.

The proper operation of the PPS circuit was first tested. $V_S$ and $V_{rY}$ signals were monitored to check the signal phase displacement for each resistor value, as shown in Figure 8. Based on the measured phase shift, the real resistive value in the R-2R network was estimated according to Equation (5), to compare theoretical and measured data. Table 2 shows that the phase displacement becomes wider as $R_{PS}$ is decreased. Thus, first fine and then coarse phase tuning is performed, which results in fast adjustment to the desired value. Good matching between the calculated and the measured data is observed, with a phase absolute error $\epsilon_{ap} \leq 1.5^\circ$ which in turn corresponds to a maximum relative error in the output voltage $\epsilon_{r\theta}$ due to phase misalignment of 0.03%, an overall phase adjustment range of 236° and a phase resolution of 2°. The 4-bit resolution is therefore enough in practical cases to get high accuracy.
As already mentioned, there are two valid solutions to operate the single-phase LIA: with $V_{IN}$ and $V_{RX}$ in phase or in counter-phase, i.e., with a final phase shift between $V_{IN}$ and $V_{RY}$ of 90° or 270°. Figure 9 shows the phase adjustment steps in the Q-channel in both cases, starting with a 0 or 180° phase shift between $V_{IN}$ and $V_{RY}$. Note that from 120° to 180° (300° to 360°), a 60° range of adjustment is lost. It is worth mentioning that this issue can be solved by increasing the number of bits or redesigning the R-2R ladder to obtain a smaller value of $R_{PS}$. Even though it was not experimentally implemented, it was verified by simulation that the ideal $R_{PS}$ range of values for $f_0 = 1$ kHz would be from 10 kΩ to 50 Ω to cover the entire phase adjustment range.

As explained in Section 2.3, during the phase adjustment the control word $B(4)$ is initialized to $\{1, 1, 1, 0\}$, so $\theta = 90^\circ$. If $V_Y < V_{dd}/2$, $B(4)$ is set to $\{0, 0, 0, 0\}$ and starts increasing while monitoring $V_Y$ until it crosses $V_{dd}/2$, and the last digital word $B(4)$ after the crossing occurs is saved. For a more friendly-user operation, the Arduino was programmed to provide $V_X > V_{dd}/2$ even in the counter-phase condition.

Figure 8. Photograph of $V_S$ signal versus $V_{RY}$ signal with phase shift $\theta_{PS}$ of: (a) 105°; (b) 26°.

Figure 9. Phase adjustment steps at Q-Channel for in-phase condition (red) and counter-phase condition (blue).
Table 2. R_{PS} and Phase Shift steps for each digital word.

| Digital Word | Theory | Measured | Phase Error |
|--------------|--------|----------|-------------|
| dec \( b_3, b_2, b_1, b_0 \) | \( R_{PS} \) (kΩ) | \( \vartheta_{VR} \) (deg) | \( \epsilon_{VR} \) (deg) | \( \epsilon_{ap} \) (deg) |
| 00 | 0, 0, 0, 0 | 10.0 | 2.1 | 10.1 | 2.0 | 0.1 |
| 01 | 0, 0, 1, 1 | 9.38 | 3.3 | 9.50 | 3.0 | 0.2 |
| 02 | 0, 1, 0, 0 | 8.75 | 4.4 | 9.00 | 4.0 | 0.4 |
| 03 | 0, 1, 1, 0 | 8.13 | 6.2 | 8.20 | 6.0 | 0.2 |
| 04 | 0, 1, 1, 1 | 7.50 | 8.0 | 7.48 | 8.0 | 0.0 |
| 05 | 0, 1, 1, 1 | 6.88 | 10.1 | 6.90 | 10.0 | 0.1 |
| 06 | 0, 1, 0, 0 | 6.25 | 12.6 | 6.38 | 12.0 | 0.6 |
| 07 | 0, 1, 0, 1 | 5.63 | 15.6 | 5.73 | 15.0 | 0.6 |
| 08 | 1, 0, 0, 0 | 5.00 | 19.3 | 5.05 | 19.0 | 0.3 |
| 09 | 1, 0, 0, 1 | 4.38 | 23.9 | 4.50 | 23.0 | 0.9 |
| 10 | 1, 0, 1, 0 | 3.75 | 36.0 | 3.84 | 35.0 | 1.0 |
| 11 | 1, 0, 1, 1 | 3.13 | 37.9 | 3.20 | 37.0 | 0.9 |
| 12 | 1, 1, 0, 0 | 2.50 | 49.0 | 2.55 | 48.0 | 1.0 |
| 13 | 1, 1, 0, 1 | 1.88 | 64.5 | 1.90 | 63.0 | 1.5 |
| 14 | 1, 1, 1, 0 | 1.25 | 87.8 | 1.22 | 89.0 | 1.2 |
| 15 | 1, 1, 1, 1 | 0.63 | 120.8 | 0.64 | 120.0 | 0.8 |

For the complete system characterization, sinusoidal signals \( V_{IN} \) and \( V_S \) were generated separately in order to modify the \( V_{IN} \) phase externally. The signals were chosen within the dynamic range of each block, namely \( V_{IN} = 6 \text{ mV} \) and \( V_S = 600 \text{ mV} \), both at 1 kHz. An initial random phase shift of 75° between \( V_R \) and \( V_{IN} \) was set. The system performs the calibration process until \( V_Y \) output satisfies the quadrature condition, and then the measurement process is started. This procedure was repeated for an initial phase shift of 210°, chosen again in a random way just to verify that the calibration and measurement processes were performed correctly.

The steps in phase that the PPS circuit performs for both phase shifts in the Q-Channel, and how the IP-Channel follows the same steps but with a constant −90° shift, are shown in Figure 10, where it is verified that both channels are adjusted to operate in the required phase conditions.

![Figure 10. Experimental phase adjustment of \( V_X \) and \( V_Y \) for a 75° (purple) and 210° (green) initial phase shift between \( V_{RY} \) and \( V_{IN} \) signals.](image-url)
It is important to notice that the offset was calibrated: the systematic output offset of each LIA were measured at no signal level, then those values were subtracted from the experimental dc output values $V_X$ and $V_Y$ through the Arduino program before storing the measured data to the PC.

The $V_Y$ output is displayed in Figure 11a. Considering the cut-off frequency of the LPF, during the calibration stage a delay of 120 ms was added at each digital bit change ($b_3$-$b_0$) to allow $V_X$ and $V_Y$ to be properly established. When the quadrature condition is satisfied, i.e., $V_Y = V_{dd}/2$, the in-phase condition is set for the IP-Channel and the measurement procedure can begin. For this test, the phase adjustment and measurement processes were performed in periods of approximately 2 seconds each. During these same measurements, the $V_X$ voltage was also monitored as shown in Figure 11b, where the two outputs, $V_X$ and $V_Y$, for the cases of 75° and 210° phase shifts are presented. When $V_Y = V_{dd}/2$, the $V_X$ output shows the expected DC voltage (1.139 V with relative error $\varepsilon_{rV} = 0.2\%$), meaning that $V_{IN}$ and $V_{RX}$ signals are in-phase.

![Figure 11](image-url)

**Figure 11.** Real time monitoring for 75° and 210° phase shifts between $V_X$ and $V_{IN}$ signals of: (a) $V_Y$ signal; (b) $V_X$ and $V_Y$ output signals.

Table 3 summarizes the experimental system performance corresponding to different initial phase shifts. The ideal values of $V_X$ and $V_Y$ were calculated by using Equations (2) and (3), respectively. Even though, as shown in Figure 11, adjustment was achieved much faster for 75° than for 210° initial phase-shift, calibration is correctly performed in a few seconds with relative errors $\varepsilon_{rV}$ below 0.7% for the $V_Y$ output. Besides, $V_X$ output meets the in-phase condition with a relative error $\varepsilon_{rV}$ below 0.2%. It is worth mentioning that the relative error presented by the system is also affected by the gain mismatch between LIAs. However, the system manages to overcome this problem by presenting an error $\varepsilon_{rV}$ below 1% in both output channels.

| Phase Shift | Ideal Value (V) | Measured Value (V) | $\varepsilon_{rV}$ (%) |
|-------------|-----------------|--------------------|-----------------------|
|             | $V_X$ | $V_Y$ | $V_X$ | $V_Y$ | $V_X$ | $V_Y$ |
| 0°          | 1.141 | 0.900 | 1.140 | 0.904 | 0.1  | 0.5  |
| 75°         | 1.141 | 0.900 | 1.139 | 0.900 | 0.2  | 0.0  |
| 180°        | 1.141 | 0.900 | 1.140 | 0.904 | 0.1  | 0.5  |
| 210°        | 1.141 | 0.900 | 1.139 | 0.906 | 0.2  | 0.7  |

3.2. Impedance Measurements

Once the reference signals $V_{RX}$ and $V_{RY}$ are in phase and in quadrature with the input signal, respectively, the final 4-bit PPS digital word is saved and the measurement process begins. Measurement of non-complex impedances, either purely resistive or capacitive, is possible with
single-phase LIA operation, i.e., by monitoring the in-phase channel \( V_X \) output. However, if the sensor consists of a complex impedance, with both resistive and capacitive components, the system should be used as a dual-phase LIA where both outputs deliver the complete information of the sensor [26,27]. In this work, the proposed LIA system is characterized as a single-phase instrument with phase alignment for low-amplitude resistive and capacitive sensors measurements, since in previous works [33,36] the circuit noise immunity was already tested. The electrical equivalent of resistive and capacitive sensors was measured under controlled environmental conditions to eliminate any variation due to temperature, humidity, and light.

The measurement setup system is shown in Figure 12. Figure 12a shows the electrical symbol of the resistive and capacitive sensors with a tolerance of 2% and 5%, respectively, that were placed into a voltage divider and stimulated with a sinusoidal signal \( V_S = 600 \text{ mV} \) at 1 kHz, with reference resistor \( R_0 = 5 \text{ k}\Omega \) and reference capacitor \( C_0 = 1.6 \text{ \mu F} \), respectively. The sensors were previously measured independently to determine their real value, therefore, the estimated value of the resistive and capacitive sensors based on the measured voltages is compared with the exact value of the sensor. This way, the accuracy of the proposed LIA when determining the sensors values can be quantified.

The values of the reference impedances in each case where chosen to maximize the detection of variations at \( V_X \) output and improve the data collection of the Arduino YUN platform. Figure 12b presents the connection diagram of the whole system. Coupling between the sensing circuit and the LIA was made by means of a decoupling capacitor \( C_{dec} = 1 \text{ \mu F} \) followed by an analog inverter which was used to further reduce the \( V_m \) signal amplitude, in this case, 100 times \((R_2 = 100 \times R_1)\) at the input of the LIA, in order to emulate a more realistic bio-signal test (in the order of 0.01–10 mV [48,49]).

![Figure 12](image)

**Figure 12.** Measurement System: (a) Resistive and Capacitive sensor connection; (b) Complete experimental setup.

The gain of both LIAs was set at maximum (42 dB) and the inverter and LIAs common mode input were connected to the required \( V_{dd}/2 \) DC level. Finally, the Arduino platform was the interface between the measurement system and the PC, as previously explained, allowing to control the phase alignment and store the measured data.

In Figure 13 the \( V_X \) and \( V_Y \) outputs for resistive and capacitive sensors are displayed and compared to the theoretical values. It can be observed that information on the resistive (Figure 13a) and capacitive (Figure 13b) sensor is provided by \( V_X \), while \( V_Y \) output remains equal to \( V_{dd}/2 \) in both cases.
Based on the experimental LIA output voltages, the resistive and capacitive sensor values are determined by:

\[
R_S = R_0[(\frac{1}{C_{\text{CMIA}}} R_1 V_S/\pi R_2 V_X) - 1],
\]

\[
C_S = C_0[(\frac{1}{C_{\text{CMIA}}} R_1 V_S/\pi R_2 V_X) - 1].
\]

Figure 14 shows the \( R_S \) and \( C_S \) sensor values obtained from these equations. It can be observed in both cases that the use of a smaller cut-off frequency for the LPF results in higher measurement accuracy. For the first case (Figure 14a) the system presents a sensor measurement relative error \( \epsilon_{rS} \) lower than 3%; for the second case (Figure 14b) the relative error \( \epsilon_{rS} \) is below 5% in the determination of the capacitive value. The proposed system operating at maximum gain has a measurement sensitivity of 16.3 \( \mu \)V/\( \Omega \) and 37 kV/Farad for resistive and capacitive sensor, respectively.

Finally, Table 4 presents a comparative of the proposed Lock-in Amplifier with other recent LIA solution. Even though special emphasis was made on searching solutions focused on a single phase LIA with phase alignment, only a few papers were found [50,51], implemented with discrete components or, as the proposed system, consisting of a mixed approach. However, it should be noted that in [50] and [51], three and four PSDs are required, respectively, for a single measurement output, while in the proposed LIA only two PSD are used, and it can be configured as a single or dual phase LIA.
Besides, in [50] the DC output voltages are measured by a data acquisition board (DAQ), which is a bulky module that reduces autonomy. On the other hand, the proposed solution not only uses a portable platform (Arduino) but also offers a wider frequency range from 0 to 125 kHz and input dynamic range (4.5–17 mV) with a resolution of 25 μV, faster phase calibration (<2.5 s) and smaller silicon power consumption. Thus, it constitutes a more versatile, hardware efficient and power efficient solution for phase adjustment without degrading the performance on integrated LIAs prototypes.

Alternatively, in [18,20,26,27,31] the implementation of a dual phase LIA is chosen to avoid the dependence with the phase of the input signal, being oriented to bioimpedance measurement. These papers are also included in the comparison. The proposed LIA shows greater versatility and flexibility compared to those solutions, as the phase alignment circuit can be enabled/disabled for its use as single-phase or dual-phase LIA. In addition, the gain adjustment (25–42 dB) as a function of the input signal amplitude, the reduced power consumption (834 μW for integrated prototypes and 7 mW for the whole system) and smaller silicon area (0.026 mm²), high sensitivity, and compatibility with microcontrollers as Arduino YUN, that enable fast data acquisition, make it a suitable and adaptable option for its use in truly portable applications.
Table 4. Performance comparison of LIA system with other solutions.

| Parameters               | This Work | [26]*04 | [20]*08 | [27]*09 | [18]*10 | [50]*12 | [31]*15 | [51]*16 |
|--------------------------|-----------|---------|---------|---------|---------|---------|---------|---------|
| Implementation           | CMOS 180 nm & Discrete components | Discrete components | CMOS 350 nm | CMOS 180 nm | CMOS 350 nm | Discrete components | CMOS 180 nm | CMOS 350 nm & Discrete components |
| Power Supply             | 1.8 V\text{LIA} \text{a} |
|                          | 3.3 V\text{OA} \text{a}  |
|                          | n.a.       | 3.3 V   | 1.8 V   | 3.3 V   | 5 V     | 1.8 V   | 1.8 V   |
| LPF implementation       | RC external | External | RC external | SC internal | Gm-C internal | RC external | RC external | RC external |
| Gain                     | 25–42 dB   |
|                          | n.a.       | 108 dB  | −12–0 dB | 120 dB\text{O} | 112 dB   | 0–40 dB | 106 dB |
| BW                       | 125 kHz    |
|                          | 10 MHz     | 800 kHz | 100 kHz | 13–25 kHz | n.a.     | 1 MHz   | 2.5–25 Hz |
| Freq. op.                | 1 kHz      |
|                          | 100 kHz    | 30 kHz  | 1 kHz   | 20 kHz   | 77 Hz   | 10–100 kHz | 11 Hz |
| Input range              | 4.3–17 mV  |
|                          | n.a.       | 1 µV    | 3 mV    |
|                          | n.a.       | 0.002–7 mV | 0.2–14 mV | 35–700 nV |
| Resolution               | 25 µV      |
|                          | n.a.       | n.a.    | n.a.    | n.a.    | 200 nV  | 1 µV    | 12.5 nW |
| Dynamic Reserve          | 35.5 dB    |
|                          | n.a.       | n.a.    | n.a.    | 1.31 dB | n.a.    | 39 dB   | 34 dB   |
| Sensor Sensitivity       | 16.3 µV/Ω  |
|                          | 37 kV/F    |
|                          | n.a.       | n.a.    | 4.2 µV/Ω | 75 MV/F |
|                          | n.a.       | n.a.    | n.a.    | n.a.    | n.a.    | n.a.    | n.a.    |
| Sensor Range             | 1–10 kΩ    |
|                          | 20–220 Ω   |
|                          | 0.75–2.8 µF|
|                          | n.a.       | 10–40 kΩ| 0.5–1.8 nF |
|                          | n.a.       | n.a.    | n.a.    | n.a.    | n.a.    | n.a.    | n.a.    |
| LIA config.              | Single & Dual Phase | Dual Phase | Dual Phase | Dual Phase | Single Phase | Single Phase | Dual Phase | Single Phase |
| Phase Calibration        | Included   |
| Phase Cal. Error $\Delta \phi$ | $<1.5^\circ$ | n.a.    | n.a.    | n.a.    | n.a.    | n.a.    | n.a.    | n.a.    |
| Phase Cal. Time          | $<2.5$ s   |
|                          | n.a.       | n.a.    | n.a.    | n.a.    | n.a.    | 25–80 s | n.a.    | 1 s     |
| Silicon Area             | 0.026 mm$^2$|
|                          | n.a.       | 2.5 mm$^2$ | 2 mm$^2$ | 1.5 mm$^2$ | n.a.    | 0.048 mm$^2$ | 8 mm$^2$ |
| Power Consumption        | 834 µW\text{a} |
|                          | 7 mW\text{b} | n.a.    | 110 mW\text{a} | 2 mW\text{a} | 13 mW\text{a} | n.a.    | 3.5 mW\text{a} | 2 mW\text{b} |

\text{a} Silicon Power Consumption, \text{b} System Power Consumption.
4. Conclusions

A fully autonomous single-phase lock-in amplifier solution has been proposed in this article, implemented with two integrated CMIAIs in CMOS UMC 180 nm technology and Arduino YUN platform. The discrete implementation was designed to have adjustable high gain and phase in order to measure signal amplitude or electrical impedances without degrading the performance of the CMOS integrated prototypes. It has a resolution of 25 µV, with sensor sensitivity of 16.3 µV/Ω @ εS < 3% and 37 kV/F @ εS < 5% for resistive sensor and capacitive sensor measurements, respectively. The low power consumption of 834 µW and low integration silicon area of 0.026 mm² of the two CMIA prototypes, in addition to its capacity to be used as a dual-phase LIA, make it highly suitable for portable devices and innovative applications such as bio-impedance measurements. Besides, its compatibility with microcontrollers, in this case Arduino YUN, allows it to be adapted to different applications within the operating ranges of the CMIA.

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