PA-Boot: A Formally Verified Authentication Protocol for Multiprocessor Secure Boot under Hardware Supply-chain Attacks

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ABSTRACT

Hardware supply-chain attacks are raising significant security threats to the boot process of multiprocessor systems. This paper identifies a new, prevalent hardware supply-chain attack surface that can bypass multiprocessor secure boot due to the absence of processor-authentication mechanisms. To defend against such attacks, we present PA-Boot, the first formally verified processor-authentication protocol for secure boot in multiprocessor systems. PA-Boot is proved functionally correct and is guaranteed to detect multiple adversarial behaviors, e.g., processor replacements, man-in-the-middle attacks, and tampering with certificates. The fine-grained formalization of PA-Boot and its fully mechanized security proofs are carried out in the Isabelle/HOL theorem prover with 306 lemmas/theorems and ~7,100 LoC. Experiments on a proof-of-concept implementation indicate that PA-Boot can effectively identify boot-process attacks with a considerably minor overhead and thereby improve the security of multiprocessor systems.

CCS CONCEPTS

- Security and privacy → Formal security models.

KEYWORDS

Formal verification, secure boot, authentication protocol.

1 INTRODUCTION

Attacks during the boot process are notoriously hard to detect because at this early stage of a device’s lifecycle, traditional countermeasures like firewalls and anti-viruses are not yet in place [1]. A widely adopted defence against boot attacks is known as secure boot [2, 3], which enforces every boot stage to authenticate the subsequent stage such that only the firmware signed by an authorized entity (i.e., the device manufacturer) can be loaded and thereby establishes a chain-of-trust in the entire boot process. During this process, the processors of a device serve as the root-of-trust (RoT) to bootstrap the trust chain [3]. The authenticity of processors is thus of vital importance to system security.

However, the globalized and increasingly complicated hardware supply chains are threatening the trustworthiness of processors – the RoT in secure boot – therefore exposing various modern devices to inevitable supply-chain attacks [4–9]. Specifically, many original equipment manufacturers (OEMs) nowadays outsource their hardware and/or firmware development to third-party suppliers without full inspection into their cybersecurity hygiene [10, 11], where the devices can be intercepted and implanted with compromised components during multiple hands of trade. Such supply-chain attacks raise significant security threats and thereby an urgent request in identifying device vulnerabilities [12], particularly, in the boot process [13, 14].

We focus on new hardware supply-chain attacks that can bypass secure boot of multiprocessor systems. A multiprocessor system includes a bootstrap processor (BSP) responsible for initializing and booting the operating system and multiple application processors (APs) activated after the operating system is up

\[1\]. As instances of hardware supply-chain attacks, an attacker can intercept a customer’s multiprocessor device and either (i) replace an AP with a compromised one, e.g., an AP with a bootkit implanted; or (ii) implant an extra chip sabotaging the inter-processor communications (man-in-the-middle attacks [15]). Such supply-chain attacks may incur the load of malware images or even take control of the system already at the boot stage, see, e.g., a proof-of-concept for Bloomberg’s “Big Hack” [16, 17].

Existing research efforts focus on firmware integrity and provide no countermeasures against hardware supply-chain attacks in multiprocessor secure boot. Specifically, both the authenticity of APs and the inter-processor communications are conventionally trusted by default universally across all modern multiprocessor systems.

\[^1\]The same convention applies to symmetric multiprocessing (SMP). Whereas all the processors in an SMP system are considered functionally identical, they are distinguished as two types in the boot process.
In fact, defending against this new hardware attack surface is challenging: It is difficult to examine all steps through the global supply chain from manufacturers to customers; moreover, identifying malicious components via hardware tampering detection techniques, e.g., circuit-based sensors and X-ray imaging, requires expertise and is time consuming [18, 19]. Some work uses runtime monitors to record external behaviors of CPU chips (i.e., IO/memory read and write) and verifies chip integrity [20]. However, specialized hardware components are required to extend the system. It is thus desirable to equip the existing multiprocessor secure boot process with a mechanism for authenticating APs and securing communications without requiring custom hardware changes.

In this paper, we present a processor-authentication protocol, called PA-Boot, to assure both the authenticity of APs and the confidentiality of inter-processor communications in the early stage of secure boot process for multiprocessor systems. PA-Boot is capable of detecting multiple adversarial behaviors including AP replacements, man-in-the-middle attacks, and tampering with certificates. The boot process is aborted if any of the adversarial behavior is detected to prevent the attacker from taking control of the system. The security and functional correctness of PA-Boot is verified based on deductive reasoning techniques. The formalization of PA-Boot and its fully mechanized security proofs (in terms of the AP authentication, certificate integrity, etc.) are conducted in the (interactive) theorem prover Isabelle/HOL [21]. This fine-grained formalization of PA-Boot in Isabelle/HOL succinctly captures its key components, the system behaviors, and a full range of adversarial capabilities against the protocol. To the best of our knowledge, PA-Boot is the first formally verified processor-authentication protocol for secure boot in multiprocessor systems. We further implement in C an instance of PA-Boot called CPA-Boot. Experiments simulated via ARM Fixed Virtual Platforms (FVP) suggest that CPA-Boot can effectively identify multiple boot-process attacks – by either manipulating the APs or tricking the AP-authentication mechanism – with a considerably minor overhead and thus essentially improve the security of multiprocessor systems.

Contributions. The main contributions are summarized as:

- **Design of PA-Boot**: We inspect critical steps in multiprocessor secure boot, identify a new, prevalent attack surface – exhibiting hardware supply-chain attacks – that may bypass secure boot due to the lack of AP authentication. To defend against such attacks, we design the first processor-authentication protocol PA-Boot for secure boot in multiprocessor systems that is amenable to formal verification via theorems proving. Our method does not require changes to or customization of the underlying hardware.

- **Verification of PA-Boot**: We formalize PA-Boot based on multi-level abstraction-refinement in Isabelle/HOL via 91 locale/definitions. Meanwhile, we formalize multiple properties on both functional correctness and security (e.g., authenticity and integrity). The proof that PA-Boot satisfies these properties is then fully mechanized in the form of 306 lemmas/theorems and ~7,100 LoC.

- **Implementation and evaluation**: We implement CPA-Boot in compliance with the formalization of PA-Boot. We integrate CPA-Boot in a real-world bootloader and show on FVP that CPA-Boot can effectively identify multiple adversarial behaviors like replacing APs, man-in-the-middle attacks, and tampering with certificates, with a considerably minor overhead (4.98% on Linux boot).

Paper structure. Sect. 2 recaps necessary background knowledge. Sect. 3 identifies the new attack surface and sketches the general workflow of our approach. Sect. 4 presents the detailed design of PA-Boot. We present the formalization of PA-Boot in Sect. 5 and its fully mechanized proof in Sect. 6. Sect. 7 reports our implementation CPA-Boot together with its evaluation in terms of security and performance. After a brief discussion in Sect. 8 and a review of closely related work in Sect. 9, we conclude the paper in Sect. 10.

2 BACKGROUND

This section recapitulates secure boot in multiprocessor systems and hardware supply-chain attacks.

2.1 Normal flow and limitation of secure boot

Secure boot [2] establishes a chain-of-trust to attain firmware integrity. It serves as a default (or sometimes even mandatory) feature in most modern, secure devices such as laptops, desktops, smartphones, and IoT devices [3, 22]. It starts by executing the very first immutable bootloader located in read-only storage, commonly considered as the hardware root-of-trust (RoT). The RoT performs necessary initializations to locate the next boot stage image from its storage, typically in Non-Volatile Memory (NVM) such as NAND flash, and loads it into memory. The RoT then performs authentication and integrity checks of the image using the Root of Trust Public Key (ROTPK) with the help of the cryptographic engines and later hands off control to only authenticated images. The ROTPK is the burned-in, tamper-proof OEM’s Root certificate authority (CA) public key, whose hash or itself is stored in internal immutable memory such as One-Time Programmable (OTP) memory to check the cryptographic hash and signature of the next stage image. Such an authentication mechanism propagates through all the subsequent boot stages until the load of a verified kernel image and thereby achieves integrity of the entire boot process. Following the basic idea of establishing a CoT, the implementation of secure boot varies in different architectures and platforms [23], leaving significant room for platform-specific operations.

However, the secure boot’s CoT can be easily subverted by a malicious RoT. Specifically, the security of its whole integrity checking scheme hinges on the requirement that the code executes in the first boot stage (act as RoT) is inherently trustworthy, or at worst buggy but non-malicious. Early systems use a single write-protected flash memory embedded on-board to store the very first boot code (also called BIOS for PCs). Unfortunately, BIOS ROM is not well-protected and is easily writable, resulting in many proof of concept attacks that took advantage of the lack of access control on the BIOS reflashing procedure to introduce malicious code into the BIOS [24]. After suffering decades of high-profile attacks, most modern systems use hardwired bootROM – the immutable hardware integrated inside a CPU chip – to store the RoT code [25, 26]. Relying on existing physical attack resistance techniques, most existing research considers the CPU chip as part of the trusted computing base (TCB) and only anything off-chip is part of the
threat model that is vulnerable to compromise and manipulation [25–27]. Therefore, the general trust model assumption has it that the on-chip RoT is tamper-resistant and trustworthy. However, in this work, we show that the hardware supply chain opens the door for replacing malicious CPU chips, enabling an attacker with access to the hardware supply chain to subvert the RoT in secure boot and thus take control of the target system.

### 2.2 Secure Boot in Multiprocessor Systems

Fig. 1 depicts the typical, key components in multiprocessor secure boot. Without loss of generality, we assume throughout the paper that the motherboard of a multiprocessor device is equipped with two processors on physically separated chip sockets – one acts as BSP and the other as AP. Each of them has a burned-on-chip private key serving as its hardware-specific identifier. The two processors are connected – via a shared bus – to a (mutable) NVM and a shared memory. In addition to the shared bus, the BSP and the AP can also communicate with each other through a dedicated channel for exchanging inter-processor interrupts (IPIs).

The multiprocessor secure boot process starts by executing the immutable code burned into the bootROM of the processors – commonly considered as the hardware RoT – which conducts basic hardware initializations. The AP then enters a suspended state, whilst the BSP proceeds by (i) locating the bootloader image stored in the NVM, (ii) loading the image into the shared memory, (iii) checking the authenticity and integrity of the image via the cryptographic accelerators – secure boot is thus able to detect adversarial behaviors tampering with the certified images in the NVM, and (iv) executing the image to load the next firmware image. Such an authentication mechanism propagates through all the subsequent layers until the operating system (OS) kernel is up and running. The BSP then broadcasts an IPI (encoding the address of subsequent executions) via its built-in local advanced programmable interrupt controllers (LAPIC); the AP, whose LAPIC passively monitors the IPI channel, is activated and eventually runs the OS kernel image – from the instructed address – with the same privilege as the BSP. Note that there are variants of the typical multiprocessor architecture shown in Fig. 1, e.g., other types of inter-processor communications.

### 2.3 Hardware Supply-Chain Attacks

Nowadays, as an emerging trend, both the chip and printed circuit board (PCB) supply chains have become globalized in terms of, e.g., design, manufacturing, and distribution [28]. Chip or PCB designers devise and produce merely a small portion of components in-house, while relying on a variety of possibly malicious third-party components, contract manufacturers, distributors, and EDA tools, thus rendering the supply chains vulnerable to hardware attacks from external entities. For instance, a PCB in-transit exhibits a typical attack surface (aka, an interdiction attack, ibid.), where an adversary intercepts a shipment, disassembles it, replaces chips and/or inserts additional chips that probe on certain PCB buses [28, 29], repackages the shipment, and releases it to the supply chain until it eventually reaches the intended recipient. For example, a proof-of-concept for Bloomberg’s “Big Hack” [16, 17] interposes between a flash chip and a BMC (baseboard management controller) to alter bits of firmware in transit. For OEMs who acquire different chips and PCBs from outsourced manufacturers and produce electronic devices such as PCs and smartphones, the security risk is even more prominent as the underlying hardware supply chains involve more hands of trade (than individual chips or PCBs) that are beyond the control of OEMs.

In the context of secure boot, as identified in our threat model below, an attacker with access to the hardware supply chain may bypass secure boot by exploiting either a compromised AP or an additional chip sabotaging the IPI channel and thus taking control of the target system.

### 3 OVERVIEW OF OUR APPROACH

This section identifies our threat model exhibiting the new attack surface in multiprocessor secure boot as hardware supply-chain attacks, and outlines our method against these attacks.

#### 3.1 Threat Model

In our threat model, we trust the CPU chip manufacturer (e.g., Qualcomm), PCB board manufacturer, and device OEM (e.g., Apple). In other words, the design and fabrication process of original CPU chips and boards are trusted, since they come from reliable hardware supply chains controlled by the OEM. The OEMs can also take measures for tampering detection, like checking credentials, to ensure they receive genuine components from the vendors. In addition, attacks at the manufacturing steps can’t easily target a specific end-product, making attacks highly unlikely.

We assume a realistic and powerful attacker who has physical access to the target multiprocessor device in the post-manufacturing hardware supply chain, i.e., in-transit from the OEM to the end-user or in the field. Therefore, the attacker can intercept the device and then replace the pluggable CPU chips on board and have malicious modification to the PCB, such as implanting hardware Trojans on the board wires, to launch the following two attack vectors (see Fig. 1) under no awareness of the BSP:

(a) AP-replacement attack: The attacker replaces the original AP with a malicious one that has, e.g., a bootkit implanted in its bootROM. Such a malicious AP can obtain – via the shared memory bus – secret information or high-privilege resources; even worse, it can manipulate the memory content and overwrite (parts of) the bootloader to be executed to take control of the system already at the boot stage.

(b) Man-in-the-middle attack: The attacker implants an extra interposer chip snooping on the IPI channel for inter-processor

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**Figure 1: Key components in multiprocessor secure boot.**

marks potential vulnerabilities to supply-chain attacks.
communications. Such an extra chip can sabotage the traffic along the IPI channel by, e.g., substituting the memory entry pointer encoded in the activation IPI from BSP to AP, and thus yield control-flow hijacking for arbitrary code executions; moreover, the extra chip can sniff the IPI channel to capture secret data and/or interfere with runtime inter-processor communications concerning, e.g., remote TLB shootdowns.

**Assumptions.** We restrict ourselves to the usual case where (i) We assume BSP as the root of trust. Depending on platform-specific requirements for different multiprocessor devices, the authenticity of BSP can be guaranteed by the BMC (baseboard management controller) [30] on board or a coprocessor like Intel Management Engine (ME) [31] in the boot sequence before our protocol execution. (ii) The attacker can neither learn private keys of the processors, guaranteed by existing techniques like [1, 32], nor (partially) modify the on-chip bootROM (as is exceptionally difficult [27, 33]). Sophisticated attacks such as fault injection of on-chip bootROM and use of electron microscopes to exfiltrate on-chip secrets are out of scope. (iii) The cryptographic accelerators employed for, e.g., elliptic-curve cryptography (ECC) and integrity check (SHA-256), are trusted. This is realistic given that they are implemented as on-chip internal cryptography extension modules or extended with dedicated instructions [34, 35]) in modern CPUs.

Note that hardware replacement/modification is traditionally considered a strong attack model, the adversary can physically tamper with all components on the device. Uniquely in our case, we only focus on the two new novel attack vectors. For instance, we do not consider physical attacks such as cold boot attacks or snooping attacks of the shared memory bus, given that such attacks have been studied and mitigated as in prior studies [36, 37]. Physical attacks other than internal hardware replacement, such as side-channel attacks are out of our scope.

### 3.2 Workflow of Our Approach

Fig. 2 sketches the overall workflow of our approach. To defend against the hardware supply-chain attacks (a) and (b) identified in our threat model, we develop the processor-authentication protocol PA-Boot, which orchestrates the secure boot process via an *initiation phase* to validate the processor certificates and a *challenge-response phase* to authenticate the AP identity and to secure the inter-processor communication channel. We then formalize it and the possible (adversarial and normal) behaviors thereof in Isabelle/HOL as a *high-level specification* $S_h$ and a set of *high-level properties* (encoding security and functional correctness). These high-level ingredients – capturing the core components of PA-Boot – are further *refined* into their low-level counterparts, i.e., the *low-level specification* $S_l$ and a set of *low-level properties*. We then conduct a fully mechanized proof via theorem proving that $S_l$ satisfies the low-level properties. Finally, we derive an implementation of PA-Boot from the formalized model as CPA-Boot based on a code-to-spec review [38]. We show that CPA-Boot effectively identifies various boot-process attacks with a considerably minor overhead and thereby improves the security of multiprocessor systems.

Separating the formalization of a protocol and/or its properties into high- and low-levels is a common technique used to achieve adequate abstraction and refinement (see, e.g., [38, 39]). The high-level specification gives the simplest description of the system behavior, whereas the low-level specification – closer to the implementation layer – encodes a more fine-grained characterization of all possible executions of the protocol and the attacker. Although our verification of the security properties and the functional correctness is conducted on top of the low-level specification (as it requires specific protocol configurations and execution traces), the refinement relation between the high- and low-level perspectives can be used to establish the validity of more general properties w.r.t. the low-level specification by proving it only on the high-level abstraction.

### 4 DESIGN OF PA-BOOT

This section presents the detailed design of our processor authentication protocol PA-Boot. It augments multiprocessor secure boot with several key components as depicted in Fig. 3. PA-Boot steers the secure boot process in a certificate-based, two-phase manner: The processor certificates are validated in the *initiation phase* and thereafter, in the *challenge-response phase*, the AP identity is authenticated and the inter-processor communication channel is encrypted. In what follows, we first explain necessary operations to set up the stage for running PA-Boot and then elucidate key message flows in the abovementioned two phases. Frequently used notations are collected in Table 1.
Our protocol requires the request and storage of the two processors’ certificates issued by the certificate authority (CA) at the OEMs. More concretely, the OEM first generates authorized certificates CertBSP and CertAP respectively by signing PubK_{BSP} and PubK_{AP} with its own private keys (these certificates thus can be validated by the OEM’s public key in Cert\_root), and then stores all necessary certificates \langle Cert\_root, CertBSP, CertAP \rangle in the NVM. Meanwhile, the hash value of the root certificate Cert\_root is stored in the bootROM of the processors. Recall that any attacker that can compromise the BSP’s bootROM is beyond the scope of this paper.

Due to the storage of certificates in the NVM, deploying PA-Boot may induce an adversarial behavior in addition to the aforementioned attack vectors (a) and (b):

(x) Tampering with certificates: The attacker modifies necessary certificates stored in the (mutable) NVM in order to trick PA-Boot from recognizing, e.g., a malicious AP.

However, as elaborated later, this adversarial behavior can be detected by PA-Boot during its initialization phase.

4.1 The Initialization Phase

The two processors BSP and AP behave symmetrically in the initialization phase: As depicted in (the upper part of) Fig. 4, each processor first reads the precomputed hash value RootCertHash of Cert\_root from its bootROM as well as the chain of certificates \langle Cert\_root, CertBSP, CertAP \rangle from the NVM. It then checks the validity and integrity of Cert\_root, namely, checking whether RootCertHash = Hash(Cert\_root). If this is indeed the case, then Cert\_root is used to validate the certificate of the other processor by applying the function validCert(Cert), which further reveals the public key of...
the other processor. Such a certificate-validation process suffices to detect the aforementioned adversarial behavior (x), i.e., tampering with certificates in the NVM.

4.2 The Challenge-Response Phase

As depicted in (the lower part of) Fig. 4, once confirming the validity of CertBSP in the initiation phase, the AP sends – via the interprocessor communication channel – a challenge packet \((N_{AP})_{PubK_{BSP}}\), that is, a randomly generated nonce \(N_{AP}\) encrypted with PubK_{BSP}. Note that a typical nonce is a 32-byte random number which is practically infeasible to guess. Upon receiving this packet, the BSP decrypts the packet via PrivK_{BSP} to get \(N_{AP}\) and then sends a challenge-response packet

\[
\left( (N_{AP}, N_{BSP}, \text{Hash} (EPubK_{BSP}))_{PubK_{AP}}, EPubK_{BSP} \right)
\]

where \(N_{AP}\) is the challenge nonce generated by AP, \(N_{BSP}\) is the response nonce generated by BSP, and EPubK_{BSP} is the ephemeral public key generated by BSP (for computing the shared session key \(K_{c}\) later); this challenge-response packet is encrypted by PubK_{AP} except for the EpubK_{BSP} part. After receiving the challenge-response packet, the AP first decrypts the packet and checks its integrity, i.e., checking whether the received \(N_{AP}\) is identical to the previously generated one and whether the decoded Hash (EPubK_{BSP}) is identical to the hash value of the received EPubK_{BSP}. If this is indeed the case, the AP stores EPubK_{BSP} and generates its ephemeral key pair (EPubK_{AP}, EPrivK_{AP}). Then, analogously, the AP responds to the BSP with a response packet

\[
\left( (N_{BSP}, \text{Hash} (EPubK_{AP}))_{PubK_{BSP}}, EPubK_{AP} \right).
\]

The BSP then decrypts the packet and checks its integrity by similar means as mentioned above.

These message flows by now in the challenge-response phase are able to detect the aforementioned attack vector (a), i.e., AP replacements, and (b) man-in-the-middle attacks attempting to sabotage the communication packets. To protect the communication channel from future interference, PA-Boot further produces a shared session key \(K_{c}\), such that subsequent inter-processor communications can be secured using \(K_{c}\). This concludes the entire challenge-response phase of PA-Boot. We remark that the (symmetric) shared session key \(K_{c}\) can be calculated by BSP (resp. AP) based on EPubK_{AP} and EPrivK_{BSP} (resp. EPubK_{BSP} and EPrivK_{BSP}) using the Diffie-Hellman (DH) key exchange algorithm [40].

5 FORMALIZATION IN ISABELLE/HOL

This section presents the formalization of PA-Boot in the (interactive) theorem prover Isabelle/HOL [21]. The formal model of PA-Boot consists of a high-level specification \(S_{h}\) and a refined low-level specification \(S_{L}\); \(S_{h}\) captures the core components of PA-Boot and gives the simplest description of the system behavior, whereas \(S_{L}\) – closer to the implementation layer – encodes a more fine-grained characterization of all possible executions of the system. We opt for deductive verification as implemented in Isabelle/HOL due to its scalability and inherent support of abstraction refinement [41] and code generation [42, 43]. A detailed discussion on other verification approaches can be found in Sect. 9.

Adversary model. For the adversarial behavior (a) identified in Sect. 3.1, we consider the possibility that the agent AP is compromised, and thus the adversary can manipulate the long-term keys of a compromised agent. For the adversarial behavior (b) identified in Sect. 3.1, we explicitly model a classical Dolev-Yao-style adversary [44] who has full control over the insecure BSP-AP communication channel. However, the adversary is limited by the constraints of the cryptographic methods used: He cannot forge signatures or decrypt messages without knowing the key (the black box cryptography assumption).

5.1 High-Level Specification

The high-level specification \(S_{h}\) of PA-Boot is encoded as a finite-state acyclic labelled transition system representing the protocol executions under certain security contexts:

Definition 1 (High-Level Specification of PA-Boot). The high-level specification of PA-Boot is a quintuple

\[
S_{h} \triangleq \langle S, s_0, \tilde{s}, \Lambda, \Delta \rangle,
\]

where

- \(S\) is a finite set of states encoding the protocol configurations,
- \(s_0 \in S\) is the initial state,
- \(\tilde{s} \in S\) is the ideal state signifying attack-free authentication,
- \(\Lambda\) is a finite set of event labels representing actions of the processors and the attacker, and
- \(\Delta \subseteq S \times \Lambda \times S\) is a finite set of labelled transitions.

A labelled transition \(\delta = (s, \alpha, s') \in \Delta\), denoted by \(s \xrightarrow{\alpha} s'\), yields a jump from the source state \(s\) to the target state \(s'\) on the occurrence of event \(\alpha\). We consider deterministic transitions, i.e., if \(s \xrightarrow{\alpha} s', s \xrightarrow{\alpha} s''\) are both transitions in \(\Delta\), then \(s' = s''\). The set of terminal states is defined as \(S^T \triangleq \{ s \in S \mid \forall \alpha \in \Lambda. \exists s' \in S. (s, \alpha, s') \in \Delta\}\), i.e., a state \(s\) is terminal iff \(s\) has no successors. Note that the ideal state \(\tilde{s}\) is necessarily a terminal state in \(S^T\).

A run \(\pi\) of \(S_{h}\), denoted by \(s_0 \xrightarrow{\alpha_1} s_1 \xrightarrow{\alpha_2} \cdots \xrightarrow{\alpha_n} s_n\) with \(\alpha = \alpha_1\alpha_2 \cdots \alpha_n \in \Lambda\), is a finite sequence \(\pi = s_0 \xrightarrow{\alpha_1} s_1 \cdots \xrightarrow{\alpha_n} s_n\) with \(s_n \in S^T\). A run \(\pi\) is defined as \(s_0 \xrightarrow{\alpha_1} s_1 \cdots \xrightarrow{\alpha_n} s_n\) if for any \(1 \leq i \leq n\), and \(s_i \neq s_j\) for any \(0 \leq i \neq j \leq n\). We denote by \(\Pi\) the set of all possible runs of \(S_{h}\). Given a run \(\pi = s_0 \xrightarrow{\alpha_1} s_1 \cdots \xrightarrow{\alpha_n} s_n \in \Pi\), 

\[
\text{Tail1}(\pi) \text{ denotes the tail state } s_n \text{ of } \pi.
\]

Security contexts and indicator functions. Every state \(s\) in \(S\) encodes, amongst others, the current security context \(c\in C\) consisting of security-related system configurations of the underlying security assets, including the two processors, the NVM, and the inter-processor communication channel. We apply the function \(\Gamma: S \rightarrow C\) to extract the security context pertaining to a state; for simplicity, we write \(\Gamma_s\) as shorthand for \(\Gamma(s)\). Let \(\mathbb{B} = \{\text{true}, \text{false}\}\). We employ two indicator functions to witness the presence/absence of security threats: The (partial) benignity function \(B: C \rightarrow \mathbb{B}\) signifies whether a security context \(c\) is benign (in the state that \(c\) is associated with), i.e., whether the AP and the certificates in the NVM are genuine; the free-of-attack function \(M:\Pi \rightarrow \mathbb{B}\) determines whether a man-in-the-middle attack has not occurred along a run of \(S_h\), i.e., during one possible execution of the protocol.

The high-level specification \(S_h\) together with, e.g., its indicator functions are formalized as a locale module [41] in Isabelle/HOL – an emerging mechanism for abstract reasoning – consisting of
abstract types and primitive operations that can be interpreted in different contexts. We omit the detailed locale formulation here.

5.2 Low-Level Specification

Next, we refine the high-level specification $S_h$ of PA-Boot (in the form of a locale module) to its low-level counterpart $S_l$ (expressed as 90 Isabelle/HOL definitions) by instantiating the state space as concrete protocol configurations and the labelled transitions as event-triggered actions of the processors or the attacker. The fact that $S_l$ refines $S_h$, written as $S_h \subseteq S_l$, is proved in Isabelle/HOL by interpreting locales as parametric theory modules [41].

5.2.1 The State Space Encoding Protocol Configurations. A state in $S_l$ is encoded as a record construct in Isabelle/HOL collecting all fields related to the protocol configuration:

```
record State = { bsp :: Processor, ap :: Processor, env :: Envir, status :: Status }
```

Here, the types of the involved components are declared as

```
record Processor = {
  root_cert_hash* :: RCHash, private_key* :: PrivKey, packet_buffer :: Packet,
  cert_chain :: Certs, local_nonce :: None, remote_nonce :: None,
  local_ephe_key :: EpheKey, remote_ephe_key :: EpheKey, session_key :: SessKey
}
record Envir = {
  nvm* :: Certs, channel :: Packet
}
```

where $Processor$ encapsulates all the BSP/AP-related ingredients in PA-Boot (cf. Fig. 4); $Envir$ encodes the environment of the processors, i.e., the NVM storing certificates and the inter-processor channel carrying communication packets; * marks fields that cannot be empty during the entire execution of PA-Boot; $Status$ signifies the current status of PA-Boot, which can be INIT (initialization), OK (normal execution), ERR (failure in certificate validation or packet parsing), ATTK (presence of man-in-the-middle attacks), END (normal termination), and ABORT (abnormal termination). In particular, a man-in-the-middle attack will be recognized by PA-Boot when parsing the attacked communication packet and thus leads to an ERR state; moreover, once a run visits an ERR state, it raises an error-specific alarm and terminates in the (unique) ABORT state. In fact, END and ABORT represent terminal states $S^1$ as defined in $S_h$, where $END$ particularly marks the ideal state $i$.

Note that OK, ERR, and ATTK are refined to more fine-grained status types using prefixing, e.g., CHALRESP_ATTK indicates the occurrence of man-in-the-middle attacks attempting to read or modify the challenge-response packet along the inter-processor communication channel. Other fine-grained types of status can be found in Fig. 5. For simplicity, we omit detailed declarations of low-level types like RCHash and Packet in Processor and Envir.

### Table 2: The set $\Lambda$ of events in $S_l$.

| ID | Name | Description of the event |
|----|------|---------------------------|
| 1  | Read_ROM | read RootCertHash in bootROM |
| 2  | Read_NVM | read $(\text{Cert}_{\text{boot}}, \text{Cert}_{\text{RSP}}, \text{Cert}_{\text{AP}})$ in NVM |
| 3  | Verify_RCHash | verify if RootCertHash = Hash $(\text{Cert}_{\text{root}})$ |
| 4  | Verify_Cert | verify the other processor’s cert. via $\text{Cert}_{\text{root}}$ |
| 5  | GenNonce | generate a fresh nonce |
| 6  | Send_Packet | send a packet to the channel |
| 7  | Receive_Packet | receive a packet via the channel |
| 8  | Parse_Packet | decrypt a packet and check its integrity |
| 9  | Gen_EpheKey | generate ephemeral public-private key pair |
| 10 | Gen_SessKey | calculate $K_s$ to secure the comm. channel |

### Adversarial behavior (executed by the attacker)

```
11 Attack perform a man-in-the-middle attack
```

5.2.2 Event-Triggered Transitions. As listed in Table 2, the set $\Lambda$ of event labels in $S_h$ is instantiated in $S_l$ as concrete actions of the protocol participants. Given a state $s$ and an event $e$ in $S_l$, whether $e$ is enabled in $s$ or not is specified in Isabelle/HOL as

```
definition event_enabled ≡ "State ⇒ Event ⇒ B" where
"event_enabled s e ≡ case (status s, e) of
(INIT, Read_ROM) ⇒ true |
(ok READ_ROM_OK, Read_NVM) ⇒ true |
⋯ |
(ok SEND_CHAL_OK, Receive_Packet) ⇒ true |
(ok SEND_CHAL_OK, Attack) ⇒ true |
(attk CHAL_ATTK, Receive_Packet) ⇒ true |
⋯ |
(ok RESP_OK, Gen_Sesskey) ⇒ true |
(err RESP_ERR, Send_Packet) ⇒ true |
(\_) ⇒ false".
```

The set $\Lambda$ of event-triggered transitions in $S_l$ is specified in an analogous way. Fig. 5 depicts parts of the state machine $S_l$, which represent typical scenarios in PA-Boot, e.g., validating NVM certificates (Fig. 5a) and detecting AP replacements or man-in-the-middle attacks on the response packet (Fig. 5b). A complete view of $S_l$ is found in Appx. A.

The security-related utility functions $\Gamma$, $\mathcal{B}$ and $M$ as described in the high-level specification are instantiated in the lower-level counterpart as well. For example, for a state $s$ in $S_l$ and $\pi$ in $\Gamma(s)$ yields the security context associated with $s$, that is, the components (bsp, ap, env) in $s$; moreover, given a run $\pi$ of $S_l$, $M(\pi)$ determines whether or not a man-in-the-middle attack, i.e., $\Box$, is absent along $\pi$.

---

2 Other contents in the NVM, e.g., the bootloader and the OS kernel image, are not relevant, as secure boot per se is able to detect adversarial behaviors tampering with these certified contents (see Sect. 2.2).
FORMAL VERIFICATION

This section presents the mechanized proof in Isabelle/HOL that PA-Boot is functionally correct and suffices to detect aforementioned adversarial behaviors (a), (b), and (x). The core ingredient to the proof is the formalization of the correctness of the property on functional correctness and security — first at the level of ρh and then at δ1 in a refined form.

6.1 High-Level Properties

Functional correctness. We require PA-Boot to be functionally correct, in the sense that the benignity of the security context remains invariant during any possible execution of PA-Boot:

**Property 1 (Functional Correctness w.r.t. ρh).** Any run π = s0 ⇝ ρh sn ∈ Π of ρh satisfies

\[ \mathcal{B}(\Gamma_{s_i}) \iff \mathcal{B}(\Gamma_{s_0}) \quad \text{for any} \ 1 \leq i \leq n . \]

Recall that \( \mathcal{B}(\Gamma_{s_0}) = \text{true} \) if the AP and the certificates in the NVM are genuine upon the start of PA-Boot, thereby witnessing the absence of adversarial behaviors (a) and (x). Provided a reasonable assumption that these two adversarial behaviors can only be conducted during the hardware supply chain, i.e., before the launch of PA-Boot, Property 1 ensures that our protocol per se does not alter the benignity of the security context during all of its possible executions.

Security property. PA-Boot should be able to secure the boot process, in the sense that the successful authentication by PA-Boot (indicated by reaching the ideal state s) guarantees that every boot flow thereafter involves only trusted security assets and is free of man-in-the-middle attacks:

**Property 2 (Security w.r.t. ρh).** Any run π ∈ Π of ρh satisfies

\[ \text{Tail}(\pi) = s \iff \mathcal{B}(\Gamma_{s_i}) \land M(\pi) . \]

Intuitively, Property 2 ensures that a run π of ρh terminates in the ideal state s if and only if M(π) = true and \( \mathcal{B}(\Gamma_{s_i}) = \text{true} \) (so is \( \mathcal{B}(\Gamma_{s}) \) for any s along π, due to (7)), that is, π is free of man-in-the-middle attacks and both the AP and the certificates in the NVM remain genuine along π. Moreover, the established shared session key \( K_s \) ensures that PA-Boot is able to secure the entire boot process.

6.2 Low-Level Properties

Next, Properties 1 and 2 are refined w.r.t. ρ1 in the form of Isabelle/HOL lmmas. We use to extract specific fields of a state in \( \rho_1 \), e.g., \( s, \text{ap}_\text{private}_\text{key} \) denotes PrivKAP in s.

**Functional correctness.** At the level of ρ1, Property 1 boils down naturally to the requirement that the private keys of the two processors, RootCertHash stored in their bootROMs, and the certificates stored in the NVM remain unchanged during all possible executions of PA-Boot.

**Lemma 1 (Functional Correctness w.r.t. ρ1).** Any run π = s0 ⇝ ρ1 sn ∈ Π of ρ1 satisfies

\[ s_i, \text{ap}_\text{private}_\text{key} = s_0, \text{ap}_\text{private}_\text{key} \land \]

\[ s_i, \text{bsp}_\text{private}_\text{key} = s_0, \text{bsp}_\text{private}_\text{key} \land \]

\[ s_i, \text{ap}_\text{root}_\text{cert}_\text{hash} = s_0, \text{ap}_\text{root}_\text{cert}_\text{hash} \land \]

\[ s_i, \text{bsp}_\text{root}_\text{cert}_\text{hash} = s_0, \text{bsp}_\text{root}_\text{cert}_\text{hash} \land \]

\[ s_i, \text{env}_\text{NVM} = s_0, \text{env}_\text{NVM} \quad \text{for any} \ 1 \leq i \leq n . \]

**Security properties.** In the presence of adversarial behaviors (a), (b), and (x), we aim to establish — by the end of protocol execution — three types of security goals of the underlying security assets at the level of ρ1:

- **Authenticity** (against (a)): The identity of AP is validated.
- **Integrity** (against (b) and (x)): The inter-processor communication packets and the certificates in NVM remain unmodified (even before the execution of PA-Boot).

**Confidentiality** (against (b) for future executions): The established shared session key \( K_s \) (for encrypting future communication messages) is known only to BSP and AP.

The goal on confidentiality has been proved achievable (see, e.g., [45]) due to the secrecy of \( K_s \) established by the DH key exchange algorithm [40]. The other goals on authenticity and integrity are

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\(^3\)The authenticity of the inter-processor communication packets is addressed by the low-level security properties, cf. Lemmas 2.1 and 2.3.
encoded as three individual lemmas interpreting different protocol-execution scenarios. Specifically, the protocol under normal execution (cf. Lemma 2.1) should eventually terminate in the END state where the processors are mutually authenticated and $K_1$ is established; otherwise, if an adversarial behavior that violates either authenticity or integrity is identified — i.e., the AP has been replaced or the certificates in NVM have been tampered with (Lemma 2.2), or an inter-processor communication packet has been modified by a man-in-the-middle attack (cf. Lemma 2.3) — then the protocol should raise error-specific alarms by visiting the ERR states and eventually terminate in the ABORT state.

**Lemma 2.1 (Security w.r.t. $\delta_I$ under Normal Executions).** Any run $\pi \in \Pi$ of $\delta_I$ satisfies

$$\forall \pi \in \Pi, \delta_I \vdash B(\Gamma_{s_0}) \land M(\pi) \implies \text{Tail}(\pi).\text{status} = \text{END}.$$  

Lemma 2.1 declares that starting from the initial state $s_0$ where the associated security context is benign, if there is no man-in-the-middle attack during the execution, PA-Boot must terminate in the END state signifying attack-free authentication and the establishment of $K_1$.

**Lemma 2.2 (Security w.r.t. $\delta_I$ against Tampered Configurations).** Any run $\pi = s_0 \xrightarrow{A} s_n \in \Pi$ of $\delta_I$ satisfies

$$\neg B(\Gamma_{s_0}) \implies \exists i < n : \text{Tail}(\pi).\text{status} = \text{ABORT} \land s_i.\text{status} = \text{*_ERR} \quad \text{for some} \quad 0 < i < n$$  

where * matches $A_{\text{CERTS}}, B_{\text{CERTS}},$ or $\text{RESP}$, see Fig. 5.

Lemma 2.2 states that in case $\Gamma_{s_0}$ is compromised (due to adversarial behaviors (a) and (x)), PA-Boot should raise an error-specific alarm by visiting the corresponding ERR state ($A_{\text{CERTS}}$ ERR and $B_{\text{CERTS}}$.ERR for (x); $\text{RESP}.\text{ERR}$ for (a)) until it eventually terminates in the ABORT state.

**Lemma 2.3 (Security w.r.t. $\delta_I$ against Man-in-the-Middle Attacks).** Any run $\pi = s_0 \xrightarrow{A} s_n \in \Pi$ of $\delta_I$ satisfies

$$\exists i < j < n : \text{Tail}(\pi).\text{status} = \text{ABORT} \land s_i.\text{status} = \text{*_ATTK} \land s_j.\text{status} = \text{*_ERR} \quad \text{for some} \quad 0 < i < j < n$$  

where * matches $\text{CHAL}, \text{CHALRESP},$ or $\text{RESP}$, see Appx. A.

Lemma 2.3 states that if a (challenge, challenge-response, or response) packet is modified by a man-in-the-middle attack (adversarial behavior (b)), PA-Boot should raise an error-specific alarm by visiting the corresponding ERR state (after the $\text{ATTK}$ state) and finally terminate in the ABORT state.

**Mechanized Proof in Isabelle/HOL.** In our specification $\delta_I$, an agent BSP/AP can extend a trace (i.e., a run $\pi$ of $\delta_I$) in any way permitted by the protocol. An adversarial behavior can also change the current state and extend a trace. Low-level properties on both functional correctness and security are formalized as trace properties and proved by induction on traces of $\delta_I$. In particular, security properties Lemmas 2.2 and 2.3 both cover different possible traces of $\delta_I$ (corresponding to different attack scenarios). Therefore, we further decompose these lemmas into a set of auxiliary lemmas to account for different traces and prove by induction on each trace. Then, by chaining these auxiliary lemmas together in Isabelle/HOL, we obtain a fully mechanized proof that all possible traces of $\delta_I$ (i.e., all possible executions of PA-Boot) fulfill the requirements on functional correctness and security. Table 3 collects the statistics with regard to the proof efforts conducted in Isabelle/HOL, which amount roughly to 8 person-months.

| Level | Specifications | Proofs |
|-------|---------------|--------|
| $\delta_I$ | $\sim 50$ | $\sim 50$ |
| $\delta_I$ | $\sim 850$ | $304$ | $\sim 6,150$ |

### 7 IMPLEMENTATION AND EVALUATION

This section presents CPA-Boot — a proof-of-concept implementation of PA-Boot embedded in multiprocessor secure boot — together with the evaluations in terms of its security and performance on ARM Fixed Virtual Platform (FVP) based on Fast Models 11.18 [46]. Specifically, we conduct all the experiments on the Foundation Platform [47] equipped with ARM Cortex-A72 CPUs, amongst which CPU0 performs as BSP and CPU1 as AP. The empirical evaluations are geared toward answering the following two research questions:

- **RQ1**-security: Does CPA-Boot suffice to identify adversarial behaviors (a), (b), and (x) as per PA-Boot?
- **RQ2**-performance: Is the overhead caused by CPA-Boot considerably minor in multiprocessor secure boot?

We will provide affirmative answers to both questions.

#### 7.1 Proof-of-Concept Implementation

We derive CPA-Boot in C ($\sim$1,400 LoC) for the ARM64 bare-metal environment as an instance of the (low-level) formalization of PA-Boot in Isabelle/HOL. This instantiation is justified by a code-to-spec review in the same way as [38], which establishes a (nearly) one-to-one correspondence between the formalization and the implementation, e.g., the correspondence between the events defined in $\delta_I$ (see Sect. 5.2) and the C functions declared in CPA-Boot.

We build CPA-Boot using GCC 9.4.0 cross-compiler on a server running 64-bit Ubuntu 20.04. CPA-Boot is further embedded in bootwrapper v0.2 [48], a bootloader for the ARMv8 architecture, to perform authentication at the initial boot stage. To use cryptographic primitives in the boot environment, CPA-Boot adopts wolfSSL 5.3.0 [49]. Moreover, CPA-Boot uses Newlib 4.3.0 [50] as the C standard library. Functional correctness of CPA-Boot is evaluated on the functional-accurate simulator FVP.

**CPA-Boot bootloader.** We integrate CPA-Boot at a later phase of bootwrapper such that necessary hardware initialization is finished before the execution of CPA-Boot. We refer to the resulting bootloader as the CPA-Boot bootloader. Upon the launch of CPA-Boot, both processors concurrently validate the other processor’s certificate until the initiation phase (cf. Sect. 4.1) is completed, i.e., when both processors have retrieved each other’s public key and the
Table 4: Instances of adversarial behaviors simulated via FVP. 

| Category                  | (a) | (b) | (x) |
|---------------------------|-----|-----|-----|
| Adv. behavior             | APR | CPM | CPROM | RPM | RCT | APCT |
| Detected                  | ✓   | ✓   | ✓   | ✓   | ✓   | ✓   |

validations are successful\(^4\). During the challenge-response phase, both processors sequentially send encrypted packets to each other (as the inter-processor communications cannot be parallelized) using asymmetric cryptography and then establish a shared session key (in the concurrent mode) to secure the communication channel. Since FVP does not support inter-processor communication buses, the channel is mimicked by the main memory where both processors can read from and write to a pre-defined memory location. Moreover, CPA-Boot uses Set Event (SEV) and Wait For Event (WFE) instructions for inter-processor synchronizations: once a processor finishes writing its packet to the channel, it executes an SEV instruction to wake up the other processor and then immediately suspends itself by executing WFE.

CPA-Boot makes use of asymmetric cryptography primitives implementing elliptic-curve cryptography (ECC). Concretely, we use elliptic-curve digital signature algorithm (ECDSA) [51] for certificate generation and validation, elliptic-curve Diffie-Hellman (ECDH), symmetric cryptography AES-256-CBC and HMAC-SHA256 for channel-packet encryption and decryption, and elliptic-curve Diffie-Hellman ephemeral (ECDHE) for session-key generation. The private keys, certificates, and the hash values are linked to the boot process of a Linux system, namely, the Gentoo Linux boot process. We measure the boot process in terms of performance, we additionally measure the number of executed instructions rather than CPU cycles of the boot process. For the AP-certificate manipulation, CPU0 uses the root-certificate manipulation using the hash and terminates the boot process. However, since the attacker does not know the private keys of CPU0 and CPU1, he/she cannot manipulate the encrypted hash values of ephemeral public keys. As a consequence, CPA-Boot observes unmatched hash values and thus raises an alarm and aborts the boot process.

**Library compatibility.** We tune compile-time configurations of the invoked libraries for compatibility with the bare-metal environment: bootwrapper, Newlib, and wolfSSL are compiled with the flag -mstrict-align to disable unaligned accesses; For Newlib, we adapt for response-packet manipulation, RPM for chal.-resp.-packet manipulation, RCT for root-certificate tampering, and APCT for AP-certificate tampering.

**7.2 Security Evaluation**

We perform empirical security evaluations of CPA-Boot to detect aforementioned adversarial behaviors simulated in FVP covering (a) AP replacement, (b) man-in-the-middle attacks, and (x) tampering with certificates. In particular, we introduce an extra processor CPU2 mimicking the interposer chip to launch man-in-the-middle attacks. As summarized in Table 4, CPA-Boot succeeds in detecting all different instances of these adversarial behaviors where the BSP returns error-specific alarms to abort the boot process. We show below how the adversarial behaviors are implemented and how CPA-Boot detects them.

**AP replacement.** We modify the private key PrivK\(_{AP}\) of CPU1 to simulate the AP-replacement attack\(^5\). Such attack does not trigger alarms in certificate validation and CPA-Boot enters the challenge-response phase. In this phase, CPU1 attempts to forge packets to pass the authentication. However, since the modified private key of CPU1 does not match the stored certificate Cert\(_{AP}\) that has been validated in initiation phase, CPU0 cannot decrypt the challenge packet and hence raises an AP-replacement error and aborts the boot process.

**Man-in-the-middle attacks.** CPU2 attempts to eavesdrop on or tamper with the (challenge, challenge-response or response) packets transmitted over the inter-processor communication channel (mimicked by memory) during protocol execution. Particularly, for the latter two types of packets, CPU2 acts as a skilled attacker who attempts to replace E\(_{PubK_{BSP}}\) in the challenge-response packet and E\(_{PubK_{AP}}\) in the response packet aiming to establish a shared session key for future communications. However, as the attacker does not know the private keys of CPU0 and CPU1, he/she cannot manipulate the encrypted hash values of ephemeral public keys. As a consequence, CPA-Boot observes unmatched hash values and thus raises an alarm and aborts the boot process.

**Tampering with certificates.** We modify certificates linked to CPA-Boot bootloader to simulate certificate manipulations. Specifically, the attacker tries to modify the root certificate or the AP certificate to bypass the processor authentication in the challenge-response phase. However, since the attacker cannot modify the hash value of the root certificate stored in the bootROM, CPU0 detects the root-certificate manipulation using the hash and terminates the boot process. For the AP-certificate manipulation, CPU0 uses the validated root certificate to verify the manipulated AP certificate (signed by Cert\(_{root}\)) which leads to abortion as well.

**7.3 Performance Evaluation**

We report the performance of CPA-Boot within a complete boot process from bootloader to shell login on FVP. We measure the number of executed instructions rather than CPU cycles of the boot process, as FVP is not cycle-accurate and each instruction takes equally one cycle to execute [52]. To this end, we enable PMU (short for performance monitor unit [53]) monitoring by setting a PMU control register at every critical point of the main boot stages, which records the total CPU cycles, i.e., the number of instructions executed on FVP. To demonstrate how CPA-Boot affects the entire boot process in terms of performance, we additionally measure the boot process of a Linux system, namely, the Gentoo Linux distribution (stage archive 3, with systemd as init system, kernel

\(^4\)The processor that finishes the validation earlier than the other halts and waits for the other processor.

\(^5\)PrivK\(_{AP}\) is unknown to the attacker and therefore he/she cannot partially modify the AP while keeping PrivK\(_{AP}\) unchanged.
Valid: ECC-based certificate verification; ECCEnc/ECCDec:

Table 5: #instructions consumed by the main boot stages, i.e.,
kernel to avoid kernel’s modification on the PMU counters.

Table 5 quantifies the experimental performance
of the entire boot process consisting of three main boot stages, i.e.,
bootwrapper, CPA-Boot, and Linux kernel boot. It shows that the overhead
induced by integrating CPA-Boot in multiprocessor secure boot is overall 4.98% (roughly 3% per CPU), which is indeed relatively small. We further estimate the execution time of CPA-Boot on real
hardware based on MIPS (million instructions per second) statistics:
Given that a 1.5GHz ARM Cortex-A53 core runs 3450 DMIPS [55], CPA-Boot consumes ideally 15 milliseconds on both CPU0 and CPU1. Moreover, we report the performance of different operations conducted in CPA-Boot. As depicted in Fig. 6, the main overhead of CPA-Boot stems from asymmetric cryptography used for certificate validation, packet encryption and decryption, and key exchange.

As the instruction numbers on FVP may vary slightly in different boot trials, Table 5 reports numbers averaged over 3 boot trials.

8 DISCUSSION AND FUTURE WORK

In this section, we briefly discuss some issues pertinent to our approach and several interesting future directions.

General applicability. Whereas we focused on the authenticity of APs and the confidentiality of inter-processor communication channels in multiprocessor secure boot, we expect that our protocol PA-Boot can be adapted – without substantial changes (subject to future work) – to authenticate other hardware components and to secure other types of communication channels. Promising applications include the authentication of (i) physically separated onboard chips such as integrated graphics processors (IGPs) or network cards; and (ii) hardware components within a single system-on-chip (SoC), e.g., FPGA IP cores. The latter is based on the observation that, in contemporary SoC designs, each of those hardware components acts directly on the shared memory bus of the main CPU, and therefore is endowed with similar attack capabilities, e.g., unauthorized memory accesses during the boot process. For instance, Jacob et al. demonstrated in [56] the feasibility and practical impact of attacks conducted by FPGA IP cores during SoC secure boot by a proof-of-concept on the Xilinx Zynq-7000 FPGA SoC. In fact, our protocol is applicable to general authentication scenarios where (i) every agent owns its key pair (with the private key inaccessible to attackers) and read-only storage (e.g., on-chip bootROM or off-chip flash ROM) that stores the hash value of the root certificate issued by a trusted CA; (ii) all the agents are specified a priori and hence their certificates can be stored during manufacturing; and (iii) one of the agents is benign (acting as BSP) and is able to communicate with other potentially malicious agents (acting as APs) through a (possibly insecure) communication channel.

Code generation. Our prototypical implementation CPA-Boot in C (see Sect. 7) is derived from the fine-grained formalization of PA-Boot in Isabelle/HOL based on a code-to-spec review, à la [38], to exploit the efficiency of C. An alternative way to construct the implementation is to use the built-in functionality of code generation in Isabelle/HOL [42, 43], which synthesizes functional executable code (e.g., Scala, Haskell, and ML) that inherits the correctness assurance from the verified protocol specification yet is hardly optimal in terms of efficiency. A detailed comparison of CPA-Boot against the synthesized functional implementation is subject to future work. Furthermore, it is interesting to extend the existing Isabelle toolchain to synthesize C code directly, as has been observed in [57]. To this end, we intend to refine our low-level specification in Isabelle/HOL using the Simpl language [58] (with C-like syntax) and then create a verified compiler from Simpl to C embedded in Isabelle/HOL.

9 RELATED WORK

This section reviews research efforts highly related to our approach, involving formal methods used in bootstrap authentication and protocol verification.

Secure boot/Authenticated load verification. In [59], Cook et al. verified the memory safety of the boot code running in Amazon data centers via the CBMC model checker [60]. Straznickas [61] proved the functional correctness of a bootloader program specified in RISC-V semantics using the Coq proof assistant [62]. Huang et
al. [63] proposed a co-verification method for concurrent firmware in modern SoCs using instruction-level abstractions for hardware. More pertinently, Muduli et al. [64] verified the end-to-end security of authenticated firmware loaders leveraging model-checking techniques [65, 66]. The targeted scenarios and security properties are different from ours: [64] checks the firmware-load protocol against protocol-state hijacking, time-of-check to time-of-use (TOCTOU) vulnerabilities, and confused deputy attacks during the load of the firmware image into memory, whilst our protocol verifies the processor authenticity and inter-protocol communication confidentiality before firmware loading. Similar differences apply to [67], which modeled flows of firmware loading in the Promela language and performed correctness verification leveraging the Spin model checker [68] to certify the absence of TOCTOU attacks. Cremers et al. in [69] formalized the SPDM (Security Protocol and Data Model) 1.2 protocol standard in the Tamarin prover [70]. SPDM [71] aims for device attestation, authentication and secure communication and can be used during system boot process. However, the formalized SPDM is not fully verified due to its size and complexity. Although Cremers et al. split all possible protocol flows into four separate models and verified them separately, they do not analyze cross-protocol attacks between the sub-protocols and do not verify security properties on the complete model. In summary, no existing work addresses defending against the hardware supply-chain attack surface as identified in Sect. 3.1.

Protocol verification. Formal methods have witnessed a spectrum of applications in assessing the security of large-scale, real-world security protocols like TLS 1.3 [72], messaging protocols [73–75], and entity authentication protocols [76–78]. There are dedicated tools for protocol verification, such as Tamarin [70] and ProVerif [79]. However, protocols verified in these frameworks are highly abstract versions of the actual protocol implementation and cannot guarantee the properties also holding on the implementation [80]. In contrast, we establish a justified correspondence between the formalized protocol model and the derived implementation. For instance, there is a one-to-one correspondence between the events defined in $\mathcal{Y}$ and the C functions declared in CPA-Boot. Such a correspondence provides strong assurance on the security of our implementation. It further triggers an interesting future direction to investigate the ability of code generation in proof assistants to achieve correct-by-construction synthesis as discussed in Sect. 8. As a seminal work that also uses Isabelle/HOL, Paulson [81, 82] proposes an inductive approach to model network protocols and prove their security properties. However, it does not verify our security properties Lemma 2.2 and Lemma 2.3, i.e., once an adversarial behavior is performed during protocol execution, the protocol should detect it, raise an alarm, and terminate the protocol. These properties ensure our protocol to identify the targeted attack vectors and prevent the attacker from taking control of the system.

Interactive theorem proving. Our verification of PA-Boot (cf. Sect. 6) boils down to an interactive, machine-checked proof. Extensive efforts have been made in the literature to apply interactive theorem proving to system verification. As the first verified general-purpose microkernel, seL4 [83, 84] has pioneered many aspects of the design and deployment processes. For instance, it provides a framework to certify that the C code extracted from Isabelle/HOL refines a high-level specification on functional correctness. Isabelle/HOL has also been employed in reasoning about memory management in Zephy RTOS [85] and sensitive resources in trusted execution environments [86]. Another well-known study in the realm of operating systems is CertiKOS [87], which presents a layered approach to verifying the correctness of an OS kernel with a mix of C and assembly code and establishes a proof of noninterference. An extension of CertiKOS [88] achieves the first functional-correctness proof of a concurrent OS kernel. Compilers have been yet another fruitful field for formal verification. Most prominently, the CompCert compiler [89] – targeting multiple commercial architectures like PowerPC, RISC-V, ARM, and x86 – is the first formally verified C optimizing compiler using machine-assisted mathematical proofs in Coq. Interactive theorem proving has also been extensively used in the verification of cryptographic libraries due to their essential role in security. For example, verified code from EverCrypt [90] and Fiat-Crypto [92] is used by Mozilla and Google, respectively; Amazon’s s2n TLS implementation [93] is verified via a combination of manual and automated proofs.

10 CONCLUSION

We have identified a new, prevalent hardware supply-chain attack surface that can bypass multiprocessor secure boot due to the absence of processor-authentication mechanisms. To defend against these attacks targeting “assumed-safe” components (e.g., processors and inter-processor communication channels), we presented PA-Boot, the first formally verified processor-authentication protocol for multiprocessor secure bootstrap. We showed – using a machine-checked mathematical proof in Isabelle/HOL – that PA-Boot is functionally correct and is guaranteed to detect multiple adversarial behaviors, e.g., man-in-the-middle attacks, processor replacements, and tampering with certificates. Experiments on ARM FVP suggested that our proof-of-concept implementation CPA-Boot can effectively identify boot-process attacks with a considerably minor overhead and thereby improve the bootstrap security of multiprocessor systems.

Interesting future directions include the extension of PA-Boot to contexts beyond multiprocessor secure boot and automatic code generation in Isabelle/HOL (cf. Sect. 8).

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Figure 7: The state machine $\mathcal{S}_1$ of PA-Boot. A state $s$ is identified by its status and colored in light green (normal termination), red (abnormal termination), or in blue, dark green, yellow, or orange if the transition to $s$ is triggered by BSP, AP, both BSP and AP, or the attacker, respectively; The (condensed) transition $\circ \rightarrow \tau_s$ for $p, q \in \{3, 4, 8\}$ (cf. Table 2), is triggered if all the checks in the event sequence $\circ \circ \ldots \circ$ are successful, and $\circ \circ \ldots \perp$ is triggered otherwise.