Single stage Boost Cascaded Multilevel Inverter Based on Switched Inductor Structure

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Abstract. This paper presents the experimental investigations of Switched Inductor cell (SL-FLCHBqSBI) based Five-Level Cascaded H-Bridge quasi Switched Boost Inverter for Renewable Energy (RE) applications. The SL-FLCHBqSBI topology is based on the ripple input current Switched Inductor Boost Inverter (SLBI) structure which is available in the literature. In this work, a stiff DC voltage of 36 V is taken as input to deliver a power of 100 W across a resistive load is designed. The control signals for the active devices are generated using Phase-Shifted sinusoidal Pulse Width Modulation (PS-PWM) modulation technique. The SL-FLCHBqSBI topology provides a higher voltage gain of 2.83 compared to the conventional topologies for a low duty ratio. The simulation is performed in MATLAB/Simulink environment and the simulation results are presented. A hardware set up is implemented and experiments are carried out to check the consistency of the theoretical concepts with the working of the proposed topology in practical.

Keywords: Voltage Source Inverter; Phase Shifted triangular carrier PWM; Shoot Through; quasi Switched Boost Inverter (qSBI); Switched Inductor Boost Inverter (SLBI)

1. Introduction

The Voltage-Source Inverter (VSI) [1-2] converts the DC voltage to the AC voltage which is always less than the DC input voltage. A DC-DC boost converter is connected with a traditional inverter module to achieve a maximum ac output voltage. This results in a two stage power conversion system. This circuit yields low efficiency but the cost is high. A conventional two stage Multi Level Inverter (MLI) is required to boost and invert the low DC voltage availed from the RE sources for medium voltage applications. The Multi-Level Inverters (MLIs) are featured with good quality voltage, reduced Total Harmonic Distortion (THD), reduced voltage stress, better Electro Magnetic Interference (EMI) and reduced switching losses [3-9]. The suitable arrangement of DC voltage links of MLI considerably delivers the high output voltage with improved power quality [7-9].

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MLIs are categorized into three as follows:- Flying Capacitor (FC), Neutral Point Clamped Inverter (NPC) and Cascaded H bridge Inverter (CHB) inverter. Compared to CHB type, the remaining two types need more number of switching devices. CHB inverters find major applications in industry due to their high reliability, modular features and easy controllability compared to NPC and FC [1], [7-9]. More number of identical modules is connected in cascade to increase the output voltage levels of CHB which in turn reduces the filter size at the load terminals. However, the inverted voltage obtained from the traditional CHB offers the always less than the input dc voltage. To eliminate this issue, Z source inverter and its derived circuits are suggested by the researchers. These converter circuits are able to boost the dc voltage using shoot through pulses generated by modified PWM techniques. Hence it produces a boosted and inverted voltage in single stage of power conversion [10]-[25]. Only limited voltage gain is possible with ZSI/qZSI converter circuits.

Various ZSI based MLI circuits are proposed which possess the advantages of both MLI and ZSI circuits. In ZSI/qZSI based CHB [26-32], each module produces boosted DC link voltage with duty ratio control. The single phase qZSI based CHB is presented in [29] with the details of closed loop control. But the impedance network of Z source based circuits increase the cost and weight of the system. Switched Boost Inverter and its derived topologies are presented to overcome the problems with the ZSI based in [33-35]. The class of quasi SBI is available to overcome the drawbacks of SBI like discontinuous input current, higher voltage stress across the capacitor [36]. A comparison between qZSI and qSBI topologies is presented in [37]. Due to their advantages, qSBI based CHB topology is proposed in [39]. A three phase cascaded five level qSBI is discussed in [40]. To achieve a high boost factor in fuel cells and photovoltaic based applications, switched-inductor (SL) [38], switched capacitor (SC) [41] and transformer structures [42] are used along with the switched boost network topology. A five level cascaded switched-capacitor (SC) based qSBI is presented in [43]. To overcome the shortcomings of SBI, SLBI topology is introduced.

In this research article, the experimental investigation of a five-level SL based cascaded H-Bridge qSBI presented and it is named as SL-FLCHBqSBI topology in this article. This new topology is based on the ripple-input current SLBI topology [38]. Two identical SLBIs modules are cascaded to obtain the five level ac output voltages. The overall load voltage of the cascaded inverter is superior to one SLBI module. In addition, an improved harmonic spectrum of output voltage is obtained.

2. Five Level CHB qSBI based on switched inductor (SL-FLCHBqSBI)

Inspired from the literature and as a preliminary study, modeling and simulation of a mobile smart waste bin in webots is presented in this section. This section also describes the use of different sensors, actuators, and controllers associated with the modeling of the mobile smart bin.

2.1 Circuit topology

Figure. 1 illustrates a five-level switched inductor based cascaded H-bridge qSBI. Two identical SLBI modules A and B [38] are connected in cascade to obtain a five level voltage at the inverter terminals. The source voltages $V_{g1}$, $V_{g2}$ are taken as 24 V each.
2.2 Operating Principle of SL-FLCHBqSBI

Two identical modules of ripple current SLBI topology explained in [38], is cascaded here to form a five level CHB qSBI based on SLBI. It can operate in two stages i.e. shoot-through stage and non-shoot-through stage. Both stages of operations are depicted in the Figure. 2 and Figure. 3.

2.2.1 Shoot-through stage

Figure. 2 shows the shoot through stage of module A of SL-FLCHBqSBI topology. The capacitor is initially assumed to be fully charged. The diodes D4 and D5 are reverse biased. The boost network switch $S_A$ conducts along with the inverter leg switches $S_1$ and $S_2$ which causes the shoot through state in the circuit. During this stage, capacitor $C_A$ charges the inductors $L_A$ and $L_B$.

2.2.2 Non-shoot through stage

Figure. 3 shows the non-shoot through stage of module A. In this stage, inductors discharge through the capacitors. The diodes D4 and D5 are forward biased whereas diodes D1 and D2 are reverse biased. The switch $S_A$ is turned off and the load current flows as depicted in Figure.3.
2.2.3 Steady state analysis

The voltage across the inductors and current through the capacitors during shoot-through stage are derived as,

\[
\begin{align*}
L_A \frac{dI_{L_A}}{dt} &= L_B \frac{dI_{L_B}}{dt} = V_{g1} + V_{C_A} \\
C_A \frac{dV_{C_A}}{dt} &= -I_{L_A} - I_{L_B} = -I_{\text{input}}
\end{align*}
\]

The inductor voltage and capacitor current values during non-shoot through state \([38]\) are derived as,

\[
L_A \frac{dI_{L_A}}{dt} = V_{g1} - V_{C_A} - V_{L_{B_non}}
\]

\[
L_A \frac{dI_{L_B}}{dt} = V_{L_{B_non}}
\]

\[
C_A \frac{dI_{C_A}}{dt} = I_{L_A} - I_{PN} = I_{L_B} - I_{PN} = I_{\text{input}} - I_{PN}
\]

Using equations (1) to (5), inductor voltage \(V_{L_{B_non}}\) during the non-shoot through state is obtained as,

\[
V_{L_{B_non}} = \frac{D}{1-D} (V_{g1} + V_{C_A})
\]

Similarly, current through inductor \((L_A)\) and voltage across the capacitor \((C_A)\), it gives,

\[
V_{C_A} = \frac{1+D}{1-3D} V_{g1}
\]

\[
I_{\text{input}} = I_{L_A} = I_{L_B} = \frac{1-D}{1-3D} I_{PN}
\]

\[
I_{\text{input}} = (1+D) I_L
\]

The DC link voltage \((V_{PN})\) across the inverter of the module A during non-shoot through state is derives as,

\[
V_{PN} = V_{C_A} = \frac{1+D}{1-3D} V_{g1} = BV_{g1}
\]

The module A \([38]\) of the proposed SL-FLCHBqSBI provides the boost factor \((B)\) as,

\[
B = \frac{1+D}{1-3D}
\]

3. Design equations for passive elements

The value of inductors \(L_A\) and \(L_B\) is given by,

\[
L_A = \frac{V_{g1} + V_{C_A}}{I_{L_A}} DT_s
\]

\[
L_B = \frac{V_{g1} + V_{C_A}}{I_{L_B}} DT_s
\]

The value of capacitance \(C_A\), \(C_B\) are given by

\[
C_A = \frac{I_{\text{input}}}{V_{C_A}} DT_s \quad ; \quad C_B = \frac{I_{\text{input}}}{V_{C_B}} DT_s
\]
4. Simulation Results
For the simulation analysis the topology is designed for 200 W power rating. Both the modules are supplied with the input voltage of 24 V separately to obtain a five level ac voltage across the resistive load. The expressions mentioned in (12)-(14) are used to design the passive elements. The phase shifted triangular carrier PWM is used to produce the firing pulses for the switching devices [39]. The design values used in the MATLAB simulations are presented in Table 1.

Table 1 Design specifications

| Parameters                  | Attributes        |
|-----------------------------|-------------------|
| Source Voltage ($V_g$)      | 24 V (each module)|
| Capacitors ($C_A$ & $C_B$)  | 470 µF            |
| Load Resistance ($R_L$)     | 100 Ω             |
| Shoot through duty ratio ($D$) | 0.26              |
| Inductors ($L_A$ & $L_B$)   | 1 mH              |
| Switching Frequency ($f_S$) | 10 KHz            |
| Modulation Index ($M$)      | 0.74              |

The simulation results obtained using MATLAB/SIMULINK platform is shown in Figure 6. With the $V_{g1}$ and $V_{g2}$ of 24 V, the inverter generates the inductor currents ($I_{LA}$, $I_{LB}$) of 5 A as depicted in Figure 4(a). The diodes D1 and D2 are in series with the inductors and hence the same current flows through the diodes as shown in Figure 4(a). The diode currents D3, D4 are depicted in Figure 4(b). The switch voltage stress $S_A$ in the boost network of module A and source current waveform are depicted in Figure 4(b). Figure 4(c) depicts the voltage across the capacitors $C_A$ and $C_B$, DC link voltages ($V_{PN1}$ and $V_{PN2}$) of modules A and B which are obtained the same as 120 V.
Figure 4. Simulation results of five level CHB qSBI based on switched inductor
(a) Inductor currents ($I_{LA}$, $I_{LB}$) and diode currents ($I_{D1}$, $I_{D2}$)
(b) Diode currents ($I_{D3}$, $I_{D4}$), switch stress ($S_A$) and source current
(c) Capacitor stress ($C_A$, $C_B$), DC link voltages ($V_{PN1}$, $V_{PN2}$) of module A and module B
(d) Output voltage across inverter module A, B, load voltage and load current

Figure 4(d) depicts the voltage across the inverter module A and B of 120 V and five level peak ac load voltage of 240 V. The five level peak load current is obtained as 2.25 A as in Figure 4(d).

5. Experimental results
A hardware set up of 100 W is developed to experiment the high boost capability of SL-FLCHBqSBI is depicted in Figure 5. The hardware design parameters are presented in Table 2. Figure 6(a) to Figure 6(g) exhibit the hardware results of the SL-FLCHBqSBI topology. The switching pulses in Figure 6(a) and Figure 6(b) are generated in FPGA platform.

Table 2. Hardware Design Parameters

| Parameters                  | Specification     |
|-----------------------------|-------------------|
| Input Voltage               | 18 V (each module)|
| Output Power                | 100 W             |
| Resistor                    | 100 Ω             |
| Capacitors ($C_A$ & $C_B$)  | 100 µF            |
| Modulation Index ($M$)      | 0.74              |
| Power IGBT- H20R1203        | 1200 V, 20 A      |
| Shoot-through Mosfet-       |                   |
| IRFP250N                    |                   |
| Inductors ($L_A$ & $L_B$)   | 1 mH              |
| Driver Circuit- TLP250      | 20 V, 1.5 A       |
| Switching Frequency ($f_s$) | 10 kHz            |
| Shoot through duty ratio ($D$)| 0.26             |
| Power Diode- LT6221         | 100 V, 20 A       |
Figure 5 Experimental setup

(a) S1
(b) S3
(c) S2
(d) S4
Figure 6. Experimental results of SL-FLCHBqSBI topology
(a) Gate pulse to switch S1 and S2
(b) Gate pulse to switch S3 and S4
(c) Inverter output voltage
(d) Inverter switch stress
(e) Peak DC-link voltage
(f) Load voltage and load current waveforms

Figure 6(a) and Figure 6(b) represents the gate pulses given to module A of the inverter through the
gate driver circuit. Figure 6(c) shows the output voltage waveform of one module of SL-FLCHBqSBI. The value of 48.4V peak is obtained across the load. Figure 6(d) shows the inverter
switch stress of SL-FLCHBqSBI. The value of 54.4V peak voltage is obtained across the inverter
switch. Figure 6(e) shows the DC-link voltage of module A of SL-FLCHBqSBI. The value of 60V peak is obtained across the DC-link. The output voltage obtained across the load of SL-FLCHBqSBI is depicted in Figure 6(f). The values of 102V peak output voltage and 1.86 A output current is obtained across the load.

6. Performance Comparison
Table 3 presents the comparison of passive elements and switch count among the cascaded SL-FLCHBqSBI and classical cascaded MLI circuits. The cascaded SL based qSBI uses four inductors and 10 switches. In addition, it has 2 capacitors and 10 diodes and. It has two reduced number of capacitors, same number of inductors and passive devices, two additional active devices compared to cascaded qZSI. The SL-FLCHBqSBI has two less capacitors; four less diodes compared to SCCFqSBI keeping the switch count the same. The switching losses are high compared to qZSI topology [39]. But, the conduction loss is significantly less.

| Components          | Cascaded DC-DC boosted VSI [13] | Cascaded qZSI [39] | Cascaded qSBI [30] | SCC-CFqSBI [43] | SL-FLCHBqSBI (Proposed) |
|---------------------|----------------------------------|--------------------|--------------------|-----------------|-------------------------|
| Switches            | 10                               | 8                  | 10                 | 10              | 10                      |
| Capacitors          | 2                                | 4                  | 2                  | 4               | 2                       |
| Diodes              | 10                               | 10                 | 12                 | 14              | 10                      |
| Inductors           | 2                                | 4                  | 2                  | 2               | 4                       |

Table 3 Circuit elements comparison of existing MLIs with SL-FLCHBqSBI
Figure 7. Performance comparison of SL-FLCHBqSBI topology
(a) D Vs B
(b) (M) Vs (B)

Figure 7(a) depicts the comparison between boost factor (B) and duty ratio (D). It is understood that a small duty ratio of SL-qSBI offers a high boost (B). The variation between voltage gain (G) and modulation index (M) of the conventional cascaded qSBI and SL-FLCHBqSBI is presented in Figure 7(b). It is clear that the SL-FLCHBqSBI provides a high voltage gain conventional CHBqSBI topology at the same modulation index.

7. Conclusion
In this research article experimental investigation of single phase cascaded five levels quasi qSBI based on switched inductor structure is discussed. The working principle of the proposed circuit and steady state analysis of a five level cascaded H-bridge qSBI based on switched inductor are detailed in this article. From the experimental investigations, it is obvious that SL-FLCHBqSBI offers a five level maximum ac voltage of 102V with the source voltage of 36V. A voltage gain of 2.83 is achieved at reduced shoot through duty ratio. Higher efficiency of 94.86% is achieved. Hence the topology is suitable for photovoltaic applications where a low voltage is required to provide a high boosted ac voltage.

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