Design and Analysis of a Continuously Tunable Low Noise Amplifier for Software Defined Radio

Aayush Aneja and Xue Jun Li *

Department of Electrical and Electronic Engineering, Auckland University of Technology, Auckland 1010, New Zealand; aayush.aneja@aut.ac.nz
* Correspondence: xuejun.li@aut.ac.nz; Tel.: +64-9-921-9999

Received: 22 January 2019; Accepted: 8 March 2019; Published: 13 March 2019

Abstract: This paper presents the design and analysis of a continuously tunable low noise amplifier (LNA) with an operating frequency from 2.2 GHz to 2.8 GHz. Continuous tuning is achieved through a radio frequency impedance transformer network in the input matching stage. The proposed circuit consists of four stages, namely transformer stage, tuning stage, phase shifter and gain stage. Frequency tuning is controlled by varying output current through bias voltage of tuning stage. The circuit includes an active phase shifter in the feedback path of amplifier to shift the phase of the amplified signal. Phase shift is required to further achieve tunability through transformer. The LNA achieves a maximum simulated gain of 18 dB. The LNA attains a perfect impedance match across the tuning range with stable operation. In addition, it achieves a minimum noise figure of 1.4 dB.

Keywords: green radio; software defined radio; low noise amplifier; transformer network; tuning transistor; phase shifter

1. Introduction

The number of wireless standards has increased rapidly in the last decade. Together with advancements in integrated circuit (IC) technologies, it has proliferated research in multiband radio systems. As such, Software Defined Radio (SDR) has gained popularity due to its ability to handle multiple bands through a single system. In addition, SDR can enable green radio networks (GRNs) by adapting the operating frequency to a band with less interference. Next-generation SDR systems possess the capability to eliminate external processing hardware and implement associated software instead for digital signal processing and digitization [1]. The literature on this topic focuses on improving the flexibility of SDR with specific attention on the front end.

In general, the design requirements for an SDR low noise amplifier (LNA) are yet to be standardized. An LNA is the first active circuit in the receiver front-end chain of an SDR. It should primarily have a high voltage gain, low noise figure (NF) and wideband impedance matching. In case of a band-limited SDR, the LNA should support reconfigurable multiband operation [2]. Additionally, a stable and linear operation is desired at all frequencies of operation. It is challenging for a reconfigurable LNA to achieve a desired narrowband bandpass response at individual center frequencies [3] so that out-of-band interferers in the operational bandwidth can be filtered out. Designing a reconfigurable input matching network with narrowband response is highly efficient as compared to a wideband matching network, where noise and interference from adjacent bands are difficult to suppress [4].

Reconfigurable LNAs for SDRs are broadly divided as switchable LNAs and tunable LNAs. For an SDR with limited bandwidth, tunable LNAs with continuous or discrete tuning are preferred. Tunable LNAs are further divided as input tuning LNAs and output tuning LNAs.
Input tuning is referred to the capability to reconfigure the frequency response of the input impedance by variation of one or more elements in the input matching stage [5]. On the contrary, output tuning refers to variation of elements in the output matching or loading stage to vary the response of output impedance. Output tuning LNAs [6,7] usually implement a wideband input matching network and a tunable output load. Wideband matching in such LNAs requires careful frequency planning to filter out interference. Input tuning LNAs implement a wideband load and a tunable input matching. It is important to select an appropriate topology for designing an input tuning LNA. Common gate (CG) topology was implemented in [8,9] to get the wideband response and stable operation. However, the topology is not desired for designing an input tuning LNA due to the dependence of gain and NF on transconductance $g_m$. Common Source (CS) LNA with inductive degeneration increases the real part of input impedance. It further improves the overall gain and noise matching of the circuit. Figure 1 illustrates the concept of input tuning LNA using a conventional source degenerated narrowband LNA. Replacing gate inductor $L_g$ with a variable inductor $L'_g$ provides reconfigurable input impedance matching and therefore variable minimum input return loss ($S_{11}$) at different center frequencies. Nevertheless, implementing an LNA with $L'_g$ will consume a large on-chip area and hysteresis due to tunable inductor would degrade the overall Figure-of-Merit (FOM) of the LNA.

![Conceptual representation of a conventional input tuning LNA with $L_g$.](image1)

![Small signal equivalent of conventional LNA.](image2)

For input tuning LNAs, impedance transformer [10,11], tunable floating inductor [5] and switched inductors [12] were explored. The design in [10] proposed a continuously tunable LNA (CTLNA) to accommodate a large bandwidth with relatively less on-chip area. To achieve this, an ideal amplifier was applied to the feedback of $L_g$. Consequently, $L_g$ can be scaled by a factor that is proportional to the gain of the amplifier. However, adding additional amplifier increases the noise in the circuit and power consumption as well.
For output tuning LNAs [13], variable capacitor [6,14], switched capacitors [15,16] and varactor [17] were implemented as output load. Switched capacitors and inductors provide agile discrete tuning, but lead to substantial increase in chip area and manufacturing costs. In addition, tunable active inductors were explored to overcome the low $Q$ of inductors and their large area consumption on chip. However, drawbacks associated with active inductors are higher power consumption, high noise and nonlinearity. As compared to input tuning LNAs, output tuning LNAs are more susceptible to process variations. They also need additional passives for designing a wideband input matching network. Furthermore, less input tuning LNAs were reported in the literature as compared to output tuning LNAs [18].

FPGA based reconfigurable amplifiers [19] have been explored for lower frequency applications other than SDR. Transformer based matching networks [11,20] feature an interesting alternative with a wider tuning range [21] and reduced power consumption. In this paper, we provide a comprehensive design and analysis of an input tuning LNA that implements a physical radio frequency (RF) transformer to dynamically tune the input impedance. The LNA achieves a tunable input matching and a wideband output matching from 2.2 GHz to 2.8 GHz. The organization of the paper is as follows—Section 2 presents the motivation. Section 3 discusses the analysis and design of the proposed CTLNA. Section 4 presents the overall architecture of CTLNA with analysis of input impedance, gain and NF. Section 5 discusses simulation results and finally Section 6 concludes the paper.

2. Motivation

A conventional narrowband LNA as shown in Figure 1a consists of a gate inductor and a source inductor in its input matching stage. The input impedance of this LNA can be derived from the small signal equivalent circuit shown in Figure 1c. Applying KVL to the circuit, the total input voltage $V_{in}$ is

$$V_{in} = j \omega L_g I_{in} + \frac{I_{in}}{j \omega C_1} + \frac{I_{in}}{j \omega C_{gs1}} + (I_{in} + g_m V_{gs1}) j \omega L_s$$

(1)

$$\frac{V_{in}}{I_{in}} = j \omega (L_g + L_s) + \frac{1}{j \omega C_1} + \frac{1}{j \omega C_{gs1}} + \frac{j \omega L_g g_m V_{gs1}}{I_{in}}$$

(2)

$$V_{gs1} = \frac{I_{in}}{j \omega C_{gs1}}$$

(3)

From Equations (2) and (3), input impedance $Z_{in}$ of conventional narrowband LNA can be given as

$$Z_{in} = \left( j \omega (L_g + L_s) - j \left( \frac{1}{\omega C_{gs1}} + \frac{1}{\omega C_1} \right) \right) + \frac{g_m 1 L_s}{C_{gs1}}$$

(4)

where $g_m$ and $C_{gs1}$ are the transconductance and gate-source capacitance of transistor $Q_1$, respectively. The resonant frequency of input matching network depends on $C_{gs1}$, $L_g$ and source inductor $L_s$. The resonant frequency at which $Z_{in}$ is real can be determined as

$$f_0 = \frac{1}{2 \pi \sqrt{(L_s + L_g) \cdot C_x}}$$

(5)

where $C_x$ is equivalent capacitance of $C_{gs1}$ and $C_1$. It can be concluded from Equations (4) and (5) that $Z_{in}$ and $f_0$ can be made tunable by either varying $L_g$ and $L_s$. Since, $\text{Re}(Z_{in})$ is directly proportional to $L_s$, replacing $L_s$ with $L'_s$ could be a viable solution. Nevertheless, additional amplification stage is required to make $L_g$ tunable or floating, which increases the die-area, implementation costs, NF and power consumption.

A feasible and efficient solution is to replace $L_g$ with a physical RF impedance transformer, whose secondary winding can act as a variable inductor. The secondary inductance can be changed through an
additional circuit connected to the primary winding of transformer network. Using switching circuits with primary winding and inductive-capacitive resonant networks would not provide continuous tuning. Moreover, additional switching circuits shall increase power consumption and NF of the circuit. In this paper, we propose a CTLNA with tunable input matching network, comprising of a physical RF impedance transformer network. Input impedance can be varied to achieve minimum $S_{11}$ at each center frequency by changing the magnitude of current flowing through secondary winding of the transformer network. This can be achieved through magnetic coupling between primary and secondary windings of the transformer. Furthermore, the proposed LNA architecture comprises of an inductive load that provides a wideband response in the tuning range. This approach is expedient to maintain small area, continuous tuning and avoiding noise contributing elements in the signal path.

3. Proposed Circuit Topology

Figure 2 shows the block representation of the proposed CTLNA which consists of four different stages. The first stage is the input matching stage that consists of an input capacitor $C_1$ and a physical transformer. The second stage consists of a phase shifter network that comprises of two CG transistors connected in parallel to a CS transistor to get a relative 0° or 180° phase shift between the currents through primary and the secondary windings of the transformer. The third stage consists of tuning transistor whose bias voltage $V_{tune}$ can be varied to get the desired tunability. Finally, the fourth stage is the amplification stage that achieves a tunable wideband gain when $V_{tune}$ is varied. For better understanding of the proposed circuit topology, design and synthesis of each stage is described as follows.

![Conceptual block of proposed CTLNA.](image)

3.1. Transformer Network

The transformer in the input stage is an RF impedance transformer. One end of its primary winding $L_u$ is connected to the output of tuning transistor, while the other end is connected to the voltage supply $V_{DD2} = 1.3$ V. The secondary winding $L_d$ is connected to the input transistor via a DC bias network. If $L_d$ is considered as a variable inductor as shown in Figure 2, then scaling its value will provide a 50 Ω impedance matching at different center frequencies. The design utilizes a similar concept by implementing an RF impedance transformer in place of a variable inductor. Therefore, frequency reconfigurability can be achieved if current passing through $L_d$ can be changed. The magnetism property of transformer can be utilized [22] to change current through $L_d$. However, the currents $i_1$ and $i_2$ through $L_u$ and $L_d$ must have a relative phase shift $\phi$ of either 0° or 180° to allow continuous frequency tunability. This is because the RF impedance transformer circuit, shown in Figure 3a, provides a 50 Ω impedance match at a phase difference of 0° or 180° and the impedance is purely real at $\phi = 0°$. This can be substantiated by deriving the relationship between transformer’s
input impedance $Z_{inT}(\omega)$ and $\phi$. From the simplified transformer network shown in Figure 3b and $Z_{inT}(\omega)$ can be given as

$$\frac{1}{Z_{inT}(s)} = \frac{1}{sL_1 + sM} + \frac{1}{R_c} + sC_t$$  \hspace{1cm} (6)

$$\frac{1}{Z_{inT}(s)} = \frac{R_c + sL_{i1} + sM + s^2 \alpha_1 R_c + s^2 \alpha M R_c C_t}{R_c(sL_{i1} + aM)}$$  \hspace{1cm} (7)

Inverting Equation (7) and substituting $s = j\omega$, $Z_{inT}(\omega)$ is

$$Z_{inT}(\omega) = \frac{j\omega R_c (L_{i1} + aM)}{R_c (1 - \omega^2 C_t (L_{i1} - aM)) + j\omega (L_{i1} + aM)}$$  \hspace{1cm} (8)

where $\alpha = i_2/i_1$ is the ratio of primary and secondary winding currents in the transformer network, $M$ is the mutual inductance, $L_{i1}$ is primary leakage, $C_t$ is interwinding capacitance and $R_c$ is core loss resistance. Inductances $L_{i1}$ and $L_{i2}$ correspond to inductances $L_w$ and $L_d$ in the implemented transformer network and given as.

$$L_{i1} = \frac{L_p}{k} - 1$$  \hspace{1cm} (9)

$$L_{i2} = \frac{L_{i1}}{N^2}$$  \hspace{1cm} (10)

where $k$ is the coefficient of coupling and $N$ is the turns ratio. Due to phase difference between $i_2$ and $i_1$, $i_2 = \beta i_1 e^{-j\phi}$ where $\beta$ is the gain and $\alpha = \beta e^{-j\phi}$ [22]. Therefore, Equation (8) can be expanded as

$$Z_{inT}(\omega) = \frac{j\omega R_c (L_{i1} + \beta e^{-j\phi} M)}{R_c (1 - \omega^2 C_t (L_{i1} - \beta e^{-j\phi} M)) + j\omega (L_{i1} + \beta e^{-j\phi} M)}$$  \hspace{1cm} (11)

Substituting values for variables in Equation (11) as $R_c = 0.91 \ \Omega$, $\beta = 1$, $\omega = 2\pi f$, $f = 3$ GHz, $L_{i1} = 3.37$ nH, $M = 0.5$ nH, $C = 995$ fF and plotting Re($Z_{in}$) vs. $\phi$ from $0^\circ$ to $360^\circ$, we can verify that $|\text{Re}(Z_{in})| = 50 \ \Omega$ at $0^\circ$ and $180^\circ$ as shown in Figure 4a, despite the fact that our transformer model is different to that in [22].

Figure 3. (a) Physical transformer equivalent circuit for designed CTLNA (b) simplified transformer model for calculations.

Additionally, Im($Z_{in}$) is maximum at $\phi = 180^\circ$ which leads to a phase mismatch between $i_1$ and $i_2$; however, the desired relative phase shift between $i_1$ and $i_2$ is $0^\circ$ for continuous tuning. Moreover, the amplified signal is an inverted version of input signal. A possible solution is a phase shifter circuit that can provide a phase mismatch of $0^\circ$ to ensure that currents $i_1$ and $i_2$ are in phase. The resonant frequency $f_T$ of transformer can be determined as

$$f_T = \frac{1}{2\pi (L_{i1} \pm aM) C_t}$$  \hspace{1cm} (12)
The transformer’s coefficient of coupling $k$ is related to $M$ as $M = k \sqrt{L_i L_d}$. A lower value of $k$ would result in lower $M$ and less sensitivity of transformer network to large frequency variation and current mismatch. Therefore, the value of $k$ was kept low to achieve the desirable input match. Table 1 summarizes the design parameters for the transformer network.

![Graph](image-url)

**Figure 4.** (a) $\text{Re}(Z_{in})$, (b) $\text{Im}(Z_{in})$ as a function of $\phi$.

**Table 1.** Transformer design parameters.

| Parameter                  | Value    |
|----------------------------|----------|
| Turns Ratio ‘N’            | 0.69     |
| Magnetising Inductance ‘$L_p$’ | 2.23 nH |
| Cross loss resistance ‘$R_c$’ | 1000 $\Omega$ |
| Coefficient of Coupling ‘$k$’ | 0.11     |
| Primary loss resistance ‘$R_{q1}$’ | 0.91 $\Omega$ |
| Secondary loss resistance ‘$R_{q2}$’ | 4.47 $\Omega$ |
| Primary capacitance ‘$C_{q1}$’ | 924 $fF$ |
| Secondary capacitance ‘$C_{q2}$’ | 150 $fF$ |
| Interwinding capacitance ‘$C_{i}$’ | 340 $fF$ |

### 3.2. Phase Shifter

The circuit implements a conventional active phase shifter (APS) [23] to shift the phase of the amplified signal. The APS receives the amplifier output and is applied in the feedback path of the circuit. The circuit embeds two CG transistors in parallel to a CS transistor. Figure 5a shows the schematic of adapted APS circuit with a conventional topology. The designed circuit is capable of providing a phase shift of more than 90°, thereby leading to elimination of phase mismatch between complex currents $i_1$ and $i_2$. A simplified small signal equivalent circuit to illustrate the conventional APS operation is shown in Figure 5b. According to [23], $Y_{21}$ in admittance matrix for the APS is given as:

$$Y_{21}(\omega) = \frac{i_2}{v_1} = -g_{m3} \left( \frac{1}{L_p (C_p + C_{g2})} - j \omega \left( \frac{1}{C_p + C_{g2}} \right) \left( \frac{R_{q1} R_{q2} - 1}{R_p} \right) - \omega^2 \right),$$

(13)

Transformation of $Y_{21}(\omega)$ to $S_{21}(\omega)$ can be expressed as

$$S_{21}(\omega) = \left( \frac{2 \mu_5 \omega Z_{outPS}}{Z_{inPS} Z_{outPS} - Z_{inPS} \frac{\mu Z_{outPS}}{\omega^2} Z_{outPS}} + \frac{\mu Z_{outPS}}{\omega^2} Z_{outPS} \right) \cdot \left( \frac{1}{L_p (C_p + C_{g2})} + \frac{1}{R_p (C_p + C_{g2})} - \omega^2 \right),$$

(14)
From Equation (14), the phase of $S_{21}(\omega)$ can be derived as

$$\angle S_{21}(\omega) = -\tan^{-1}\left(\frac{\omega Z_{inPS}}{\frac{1}{R_p} + Z_{inPS}}\right) - 2\tan^{-1}\left(\frac{\omega}{R_p \left(\frac{1}{Z_{inPS}} - (C_p + C_{gs4})\omega^2\right)}\right)$$

(15)

where $Z_{inPS}$ and $Z_{outPS}$ are the input impedance and the output impedance of APS, respectively. It can be concluded from Equation (15) that phase of $S_{21}(\omega)$ depends upon inductor $L_p$ and capacitor $C_p$. The shift in phase of the signal with constant signal amplitude is accomplished by variation in inductance or capacitance of the resonant circuit. The values of $L_p$ and $C_p$ for 2.2 to 2.8 GHz band are 17.5 nH and 10 pF, respectively. Figure 6 shows variation of phase of $S_{21}(\omega)$ of APS with $V_X$. The circuit provides a more than 90° phase shift in our desired frequency range.

Figure 5. (a) Implemented PS circuit, (b) equivalent small signal model [23].

![Figure 5](image_url)

Figure 6. Frequency at different values of $V_X$.

3.3. Tuning Stage

Figure 7a shows the tuning stage of the designed CTLNA. It consists of a CS transistor biased with a positive gate voltage through a bias resistor. The CS transistor is placed in the feedback path and the input to its gate terminal is a phase shifted signal from the output of APS circuit. The output drain terminal is connected to one end of primary winding $L_u$ of transformer network in the input stage. Varying the bias voltage ($V_{tune}$) of tuning transistor $Q_6$ continuously leads to incessant variation in its drain current $i_{d6}$. This further leads to variation in current $i_1$ flowing through $L_u$ and resultantly in $\alpha$ and $\beta$. Figure 7b shows the variation of $i_{d6}$ with $V_{tune}$. The resultant change in $Z_{inT}$ (depends on $\beta$) varies the input impedance of CTLNA, leading to continuous tunability.
4. Circuit Analysis

Figure 8 shows the complete architecture of designed CTLNA with source degeneration and cascode topology. The cascode topology increases the circuit’s AC resistance and aids in augmenting the gain. Inductive degeneration increases the real part of input impedance. The primary consideration while designing a CTLNA is to determine the band of operation. \( C_t, L_p \) and \( k \) values in transformer network are then selected to focus the desired operating band that ranges from 2.2 GHz to 2.8 GHz. One end of primary winding of the transformer in input stage is terminated with output from the tuning transistor, while the other end is connected to voltage supply. Input capacitor \( C_1 \) resonates with \( L_d \) to achieve a continuously tunable impedance matching at different center frequencies. Continuous tuning shall only take place when \( i_1 \) and \( i_2 \) are in phase. The input of APS circuit is connected to the drain of \( Q_1 \) via \( L_3-C_3 \) network. It provides a phase mismatch of \( 0^\circ \) between the currents \( i_1 \) and \( i_2 \) through \( L_d \) and \( L_d \). The output of APS is fed to gate of \( Q_6 \) whose drain terminal further connects to \( L_d \) to achieve tunable input matching.

A resistance \( R_b \) is also added for the purpose of providing DC bias to the input transistor \( Q_1 \). For simplicity, a fixed inductor \( L_2 \) was adopted in the output loading section of LNA to achieve a wideband gain. A large resistance \( R_1 \) is added in parallel to \( L_2 \) for improving LNA stability at different frequencies and DC voltage gain.

![Figure 8. Complete CTLNA architecture.](image-url)
4.1. Input Impedance

The input stage of the proposed CTLNA consists of capacitor $C_1$ and the transformer network. Secondary inductor $L_d$ can be considered as a tunable inductor $L_g'$ that replaces $L_g$ in Figure 1 to achieve tunable input impedance. As $L_d$ cannot be directly varied, magnetic coupling can be utilised to vary the input impedance of LNA. Since $Z_{inT}(\omega)$ depends on $\alpha$, the input impedance of CTLNA in Figure 8 is derived as

$$Z_{in}(\omega) = j\left(\omega L_s + \omega L_d \pm \omega \alpha M - \frac{1}{\omega C_{gs1}} - \frac{1}{\omega C_1}\right) + \frac{g_{m1} L_s}{C_{gs1}}$$

The value of $\alpha$ can be varied by changing $V_{tune}$ that controls $i_d6$ and $i_1$. Note that the real part of input impedance depends on $L_s$ and can be changed by varying $L_s$ only. Its value has been selected to ensure that $Z_{in}$ is matched to the source. The quality factor of input matching network ($Q_{in}$) is one of the primary elements used to determine the bandwidth of network. For the designed CTLNA, $Q_{in}$ can be expressed as

$$Q_{in} = Q_{in}^L\frac{\omega L}{\text{Re}(Z_{in})} = \frac{\omega(L_s + L_d \pm \alpha M)}{(g_{m1} L_s C_{gs1})}$$

$\omega L_s \pm \alpha M \cdots \text{16)$

where $X_L$ and $R$ are imaginary and real part of input impedance, respectively. From (17) and (18), $Q_{in}$ can be simplified as

$$Q_{in} = \frac{1}{\omega(g_{m1} L_s + C_{gs1})}$$

It can be concluded from (19) that the bandwidth and $f_{op}$ of CTLNA increases as $Q_{in}$ becomes smaller.

4.2. Gain

Gain of designed CTLNA can be derived similar to a narrowband LNA shown in Figure 1. However, in this case, the input gate inductor $L_g$ is replaced with a transformer based variable inductor $L_d$ and its impedance $Z_{inT}(\omega)$ depends on $M$ and $\alpha$. The output loading network is similar to a conventional load. The low noise voltage gain for CTLNA can be derived from its small signal model of input and amplification stage shown in Figure 9. For cascode LNAs, since all transistors are the same,

$$g_{m1} = g_{m2} = 2k_n (V_{gs} - V_T)$$

where $k_n$ is conduction parameter, $g_{m2}$ is the transconductance of the transistor $Q_2$ and $V_T$ is the threshold voltage of implemented Philips MOS transistor. The small signal voltage gain $A_v$ of an LNA is defined as

$$A_v = \frac{V_{out}}{V_{in}}$$

$$V_{out} = i_d Z_{out} = g_{m1} V_{gs1} \cdot Z_{out}$$

$$V_{in} = V_{gs1}(1 + Z_{in})$$

Substituting Equation (16) in Equation (23), $V_{in}$ expands to

$$V_{in} = V_{gs1}\left(1 + j\omega(L_s + L_d + \alpha M) + \frac{1}{j\omega C_x} + \frac{g_{m1} L_s}{C_{gs1}}\right)$$
Also,

\[ Z_{out} = \frac{g_m L_2}{C_{g2}} \]  \hspace{1cm} (25)

From Equations (22) and (25),

\[ V_{out} = \frac{g_m g_{m2} L_2}{C_{g2}} V_{gs1} \] \hspace{1cm} (26)

Finally, substituting Equations (24) and (26) in Equation (21), \( A_v \) can be derived as

\[ A_v = \frac{V_{out}}{V_{in}} = \frac{j \omega g_m g_{m2} L_2 C_x C_{gs1}}{(C_{gs1}(1 - \omega^2 C_x (L_d + L_s + R M)) + j \omega C_x (1 + g_m L_s)) \cdot (C_{g2})} \] \hspace{1cm} (27)

where \( C_{g2} \) is the gate-source capacitance of the transistor Q2. Equation (27) substantiates that \( A_v \) for the designed CTLNA depends on \( \alpha \) and eventually on \( V_{tune} \). Hence the gain can also be tuned continuously in the desired band by sweeping \( V_{tune} \) from 0.5 V to 1.5 V.

**Figure 9.** Simplified small signal model of CTLNA for gain analysis.

### 4.3. Noise Figure

Figure 10 shows the noise equivalent model for the designed circuit. NF for the proposed CTLNA can be quantified by deriving its noise factor \( F \). The main noise source in the circuit is thermal noise and all passives in the circuit are considered as ideal. Considering that there are multiple noise sources in the circuit, it would be rather impractical to evaluate \( F \) without detailed noise model for all noise sources. Therefore, an expression for output noise current due to all noise sources is calculated. The short circuit noise current due to source is

\[ i_{sc, Rs} = \frac{g_{m2} V_{n, s}}{j \omega C_{gs3} R_s + Z_{in}} \cdot \omega_z \] \hspace{1cm} (28)

and

\[ Z'_{in} = 1 - \omega^2 C_{gs1} (L_s + L_d) + j \omega g_m L_s, \ \omega_z = \frac{g_{m2}}{g_{mE} + j \omega C_{Eeq}} \] \hspace{1cm} (29)

where \( g_{mE} = g_{m2} + g_{m3} + g_{m4} \) and \( C_{Eeq} = C_{g2} + C_{g3} + C_{g4} \). \( \omega_z \) is the zero introduced due to noise effect from other transistors Q2, Q3 and Q4 in parallel and \( V_{n, s} \) is the noise voltage at source. The short circuit noise current due to thermal drain noise of transistor Q1, Q2 in amplification stage is

\[ i_{sc, d1} = \left( i_{n, d1} - \frac{j \omega g_m L_s R_s}{j \omega C_{gs3} R_s + Z_{in}} \right) \cdot \omega_z \]

\[ i_{sc, d2} = i_{n, d2} (1 - \omega_z) \] \hspace{1cm} (30)
where \( i_{n,d1} \) and \( i_{n,d2} \) are drain noise currents of \( Q_1 \) and \( Q_2 \). The transistors \( Q_3, Q_4 \) and \( Q_5 \) in the PS circuit also contribute to the overall NF of CTLNA. Therefore, short circuit noise current due to drain noise of \( Q_3, Q_4 \) and \( Q_5 \) is

\[
\begin{align*}
    i_{sc,d3} &= i_{n,d3} \cdot (-\omega_s) \\
    i_{sc,d4} &= i_{n,d4} \cdot (-\omega_s) \\
    i_{sc,d5} &= i_{n,d5} \cdot \left( \frac{g_m}{g_m} \right)
\end{align*}
\]

(31)

The short-circuit noise current due to drain noise of tuning transistor \( Q_6 \) is

\[
i_{sc,d6} = \frac{j\omega g_m i_{n,d6}}{j\omega C_{gs1} R_s + Z_{in}} \cdot (-\omega_s)
\]

(32)

and due to load is

\[
i_{sc,r1} = i_{n,r1}
\]

(33)

where \( i_{n,d3}, i_{n,d4}, i_{n,d5}, i_{n,d6} \) are the noise currents of transistors \( Q_3, Q_4, Q_5 \) and \( Q_6 \) and \( i_{n,r1} \) is the noise current of load resistance \( R_L \). Using (28) to (33), \( F \) for the proposed LNA can be derived as

\[
F = \frac{1 + \sum_{x=1}^{6} i_{n,dx}^2 + i_{sc,r1}^2}{i_{sc,rs}^2}
\]

(34)

5. Results and Discussion

The proposed CTLNA is designed and simulated in MIC process. Keysight ADS and MATLAB are used as simulation tools for CTLNA analysis. The circuit is biased with 1.8 V supply and sinks 9 mA current. As can be seen in Figure 11a, \( S_{11} \) achieves a peak minimum for all different values of \( V_{tune} \) from 0.5 V to 1.5 V in steps of 0.2 V. It is below \(-10\) dB at each center frequency for the entire tuning range and achieves as low as \(-40.4\) dB at \( V_{tune} = 1.2\) V.

The LNA input matching network has been designed to match to 50 Ω at a particular centre frequency in the tuning range. The calculated 3 dB bandwidth at 2.2 GHz, 2.3 GHz, 2.41 GHz, 2.52 GHz and 2.65 GHz are 20 MHz, 100 MHz, 10 MHz, 10 MHz and 30 MHz, respectively.

Figure 11b shows simulated gain for the designed CTLNA. The LNA gain directly depends on value of loading inductor \( L_2 \). However, due to its dependency on \( a \) it can be tuned to different frequencies from 2.2 to 2.8 GHz. In addition, the CTLNA gain depends upon \( g_{m1}, g_{m2}, C_{gs1} \) source degeneration inductor \( L_n \), and designed transformer parameters. The LNA achieves a maximum gain of 18 dB at 2.36 GHz in the stipulated tuning range. The minimum gain at 2.2 GHz center frequency is approximately 8 dB. Transistors \( Q_7 \) and \( Q_8 \) in the buffer stage are capable enough to stabilize the LNA and achieve high output impedance.
For the designed LNA, $K > 1$ and $|\Delta| < 1$ at all center frequencies within the tuning range. $K_t > 1$ is a single variable criterion to determine the unconditional stability of LNA [24]. Subsequently, the LNA is stable in the entire tuning range.

Figure 4. Simulated (a) input return loss ($S_{11}$) (b) Gain ($S_{21}$) (c) Reverse isolation ($S_{12}$) and output return loss ($S_{22}$).

The output return loss $S_{22}$ is less than -8dB in the tuning range and achieves a peak minimum at center frequency of 2.35 GHz, which is the resonant frequency of output matching network. The reverse isolation $S_{12}$ also remains more than 30dB across the tuning range. Figure 11c shows the variation of $S_{12}$ and $S_{22}$ with frequencies of selected band.

Figure 12a,b show simulated NF for designed CTLNA with tuning frequency and $V_{tune}$, respectively. It is clear from Figure 12b that minimum NF at each center frequency varies between 1.4 dB to 4.8 dB. NF is a bit higher for 2.2 GHz and 2.3 GHz, which are initial frequencies in the tuning range. However, it is lower than 2 dB at center frequencies ranging from 2.4 GHz to 2.8 GHz.

The LNA stability depends upon the source and the load matching networks, which depends on the frequency of operation. Consequently, the designed CTLNA is supposed to be stable at a particular center frequency while it is unstable at other frequencies. Stability of LNA can be determined by calculating stability factor $K$ and stability constant $\Delta$ or by plotting stability circles. $K$ and $\Delta$ are can be mathematically determined using either Rollet’s criteria or Tan’s formulae [24] as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} \quad (35)$$
\[ \Delta = S_{11}S_{22} - S_{12}S_{21} \]  
\[ K_t = \frac{3 - 2|S_{11}|^2 - 2|S_{22}|^2 + |\Delta|^2 - |1 - |\Delta||^2}{4|S_{12}S_{21}|} \]  

Figure 12. Simulated NF vs. (a) Frequency (b) \( V_{tune} \).

For the designed LNA, \( K > 1 \) and \( |\Delta| < 1 \) at all center frequencies within in the tuning range. \( K_t > 1 \) is a single variable criterion to determine the unconditional stability of LNA [24]. Subsequently, the LNA is stable in the entire tuning range. Figure 13 shows variation of \( K \) with \( V_{tune} \) at different center frequencies.

Linearity of LNA is commonly measured by determining 1-dB compression point \( P_{1dB} \) and third-order intercept point \( IIP_3 \). Non-linearities in the system lead to gain-compression that causes the LNA gain to deviate from the normal curve. \( P_{1dB} \) and \( IIP_3 \) calculations have been performed using 1-tone and 2-tone inputs, respectively. A non-linear model of the amplifier is analyzed with a frequency offset of 10 MHz between two tones. The source and load impedances have been set to 50 \( \Omega \), while the harmonic frequency was selected to be 2.4 GHz. \( IIP_3 \) and \( P_{1dB} \) values for the designed CTLNA, range between \(-15 \) dBm to \(-31 \) dBm and \(-25 \) dBm to \(-42 \) dBm, respectively. Figure 14 shows the variation of \( P_{1dB} \) with \( V_{tune} \) in steps of 0.1V for the proposed CTLNA.

Figure 13. Variation of Stability factor \( K \) with \( V_{tune} \).
6. Conclusions

The design and analysis of an input tuning LNA with transformer based variable inductor matching is presented. The proposed CTLNA can be primarily used for SDR applications, such as green radio networks. The presented design takes advantage of continuous tuning due to magnetic coupling between primary and secondary windings of transformer. This occurs by changing the ratio of currents through primary and secondary windings of the transformer network. To achieve tunability, currents through transformer windings should be in phase. The methodology can be used to further implement a tunable LNA along the frequency band of 2.2 to 2.8 GHz. The design effectively integrates the matching network into an inductively degenerated CS amplifier. The LNA achieves a wideband and tunable gain in the stipulated bandwidth. The input return loss is less than −10 dB and achieves a minimum of −40.4 dB at 2.57 GHz. The NF ranges between 1.4 to 4.8 dB. In addition, mathematical analysis of transformer model, phase shifter and amplification stage are discussed. The proposed technique outlines an idea of continuous tuning that can be implemented to scale the input inductor value for any related application. Table 2 summarizes the simulated performance of designed CTLNA and comparison with previously published works.

| Ref. | Freq. (GHz) | S21 (dB) | S11 (dB) | NF (dB) | IP3 (dBm) | VDD | Tech.       | PDC (mW) |
|------|-------------|----------|----------|---------|-----------|-----|-------------|---------|
| This work | 2.2–2.8     | 7–18     | −40−11   | 1.4–4.8 | −31−15    | 1.8 | MIC         | 16.2    |
| [16]  | 1–5         | 19–27    | −16−5    | 2.4–3.8 | −6.7      | 1.2 | 65 nm CMOS  | 12.1    |
| [5]   | 1.9–2.4     | 10–14    | −25−12   | 3.2–3.7 | −20.4−9.7 | 1   | 0.13 μm CMOS| 17      |
| [12]  | 2.4–5.4     | 9.9–22   | −14−30   | 2.4–4.9 | 1         | 1   | 0.13 μm CMOS| 3.1–4.6 |
| [13]  | 0.8–2.5     | 17–20    | −27−11   | 3.1–3.6 |           | 1.8 | 0.18 μm CMOS| 3.1–4.6 |

Table 2. CTLNA performance summary and comparison with previously published works.

Author Contributions: Supervision, X.J.L.; conceptualization, A.A. and X.J.L.; formal analysis, A.A.; investigation, A.A.; methodology, A.A. and X.J.L.; writing, A.A. and X.J.L.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

References
1. Bazrafshan, A.; Taherzadeh-Sani, M.; Nabki, F. A 0.8–4-GHz Software-Defined Radio Receiver With Improved Harmonic Rejection Through Non-Overlapped Clocking. *IEEE Trans. Circuits Syst. I Regul. Pap.* 2018, 65, 3186–3195. [CrossRef]
2. Adom-Bamfi, G.; Entesari, K. A multiband low noise amplifier with a switchable Gm active shunt feedback for SDRs. In Proceedings of the IEEE Radio and Wireless Symposium (RWS), Austin, TX, USA, 24–27 January 2016; pp. 179–182.

3. Aneja, A.; Li, X.J.; Li, B.E. Design of Continuously Tunable Low Noise Amplifier for Multiband Radio. In Proceedings of the 2017 Mediterranean Microwave Symposium (MMS), Marseille, France, 28–30 November 2017; pp. 1–4.

4. Yu, X.; Neihart, N.M. A 2–11 GHz reconfigurable multi-mode LNA in 0.13 μm CMOS. In Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Montreal, QC, Canada, 17–19 June 2012; pp. 475–478.

5. El-Nozahi, M.; Sanchez-Sinencio, E.; Entesari, K. A CMOS low-noise amplifier with reconfigurable input matching network. IEEE Trans. Microw. Theory Tech. 2009, 57, 1054–1062. [CrossRef]

6. Wu, C.-R.; Hsieh, H.-H.; Lai, L.-S.; Lu, L.-H. A 3–5 GHz frequency-tunable receiver frontend for multiband applications. IEEE Microw. Wir. Compon. Lett. 2008, 18, 638–640. [CrossRef]
23. Hayashi, H.; Mauraguchi, M. An MMIC active phase shifter using a variable resonant circuit [and MESFETs]. *IEEE Trans. Microw. Theory Tech.* 1999, 47, 2021–2026. [CrossRef]

24. Tan, E.L. A quasi-invariant single-parameter criterion for linear two-port unconditional stability. *IEEE Microw. Wirel. Compon. Lett.* 2004, 14, 487–489. [CrossRef]