Transformations for Accelerator-based Quantum Circuit Simulation in Haskell

YOUSSEF MOAWAD, University of Glasgow, UK
WIM VANDERBAUWHEDE, University of Glasgow, UK
RENÉ STEIJL, University of Glasgow, UK

For efficient hardware-accelerated simulations of quantum circuits, we can define hardware-specific quantum-circuit transformations. We use a functional programming approach to create a quantum-circuit analysis and transformation method implemented in Haskell. This tool forms a key part of our larger quantum-computing simulation toolchain. As an example of hardware acceleration, we discuss FPGA-based simulations of selected quantum arithmetic circuits, including the transformation steps to optimise the hardware utilisation. Future development steps in the Haskell-based analysis and transformation tool are outlined. The described toolchain can be found on GitHub: https://github.com/DevdudeSami/fqt.

1 INTRODUCTION

Efficient simulation of quantum computers is essential for the development of quantum algorithms and for further development of quantum hardware. Quantum computers promise to deliver up to exponential complexity improvements for certain algorithms[16]; however, this is also where the difficulty in simulating them arises. The state of a coherent $n$-qubit quantum register in a quantum processor can be defined using $2^n$ complex numbers, also termed the quantum state vector. In contrast to the register in a classical computer, the quantum state in a coherent qubit register is in a state of superposition until quantum measurement operations are performed. Measurement (partially) collapses the quantum state superposition, and the complex amplitudes define the likelihood of finding a given state after measurement. Quantum superposition is the key principle creating the potential speed-up for most quantum algorithms.

The Quantum Circuit Model is the most common model for interacting with current quantum hardware and reasoning about quantum algorithms. In this work, Qubit-Wise Multiplication (QWM) is chosen as the baseline simulation method. While this requires the storage of the full state-vector, $2^n$ complex amplitudes, it does give the most control and allows full inspection of the state during computation. To process one quantum gate in QWM, the entire state vector is updated. Data-locality during these operations is not guaranteed, as pairs of amplitudes have to be accessed with strides that grow exponentially depending on the target qubit. However, for each gate, due to the implied quantum parallelism, these operations can be executed in parallel.

Classical simulations of quantum circuits are most commonly performed on multicore computers and clusters[5, 6]. A range of high-performance simulators exists. Typically, the quantum-circuit implementation of quantum algorithms is represented by a Domain Specific Language (e.g. QASM). Quantum computer simulations have also been performed on GPUs[8, 10] and FPGAs[1, 11, 13, 17]. The underlying idea of such hardware-accelerated simulations is to use the specific hardware features to process the quantum circuit more efficiently. In our ongoing research, we focus on FPGAs (Field Programmable Gate Arrays) as accelerators. FPGAs are programmable circuits that allow to construct highly parallel architectures that closely mimic the properties of quantum computing. To allow us to investigate different architectures, we developed a quantum simulation toolchain that includes a Quantum Circuit Analysis and Transformation tool. We target quantum algorithms for computational science and engineering applications. In contrast to a significant body of work focusing on general and even randomized circuits, the present work aims to explicitly take advantage of the quantum-circuit structure using the knowledge of the domain experts developing...
the algorithms. Specifically, our work differs in scope and context from previous quantum computing tool chains employing Functional Programming, e.g. Quipper and Microsoft’s Q# and Liquid.

The key contributions of this paper can be summarized as follows:

- Discussion of the design and implementation of our toolchain.
- An implementation of an FPGA-based quantum circuit simulator embedded in our toolchain and its embedded DSL
- A new circuit optimisation technique based on the reduction of input and workspace qubits for generating specialised circuits with fewer qubits, reducing the memory space required for the full state-vector simulation approach;

2 SIMULATION OF QUANTUM CIRCUITS

2.1 CPU/GPU Simulation

Extensive research has resulted in a range of highly-optimized quantum computer simulators for multi-core and distributed computing architectures. Intel Quantum Simulator (IQS, formerly known as qHiPSTER) [18] is a quantum simulator optimised for multi-node systems. ProjectQ [19] offers a modular compiler engine that can optimise at different levels of abstraction defined by the user, and includes optimised tools for local simulation of circuits. JUMPIQCS [6] is a Fortran 90-based simulator that utilises MPI for distribution. Qrack [20] and QCGPU [10] are cross platform OpenCL-based full state-vector simulators.

2.2 FPGA Simulation

The simulation of quantum computers and, specifically, quantum-circuit implementations of algorithms on FPGAs has been the topic of more recent research works. Examples of works focusing on FPGAs include [11], [1], [3], [13], [14], [17], [15], [12], and [2].

2.3 Simulator architecture for FPGAs

Our main goals for developing an FPGA simulator for quantum circuits are: universality (ability to simulate any theoretical gate), reuseability (a recompilation process should not be necessary between different circuit runs), and scalability (we should be able to simulate any feasible number of qubits without recompiling). We achieve universality by making sure the system has built-in at least a universal set of quantum gates. Our current architecture (implemented in OpenCL and tested with Intel’s AOCL compiler) stores the state vector in FPGA DRAM and compute kernels corresponding to each quantum gate access the memory to perform the necessary computations. Since in general each gate application needs to access the entire memory space, we perform gate applications sequentially and attempt to optimise the performance of the application of a general gate.

3 HASKELL TOOLCHAIN

Debugging complex quantum circuits at the level of our FPGA instruction set can be very tedious and so several higher level languages exist for expressing quantum algorithms, including Quipper [7], OpenQASM 3 [4], and Microsoft Q# [9]. We decided to include a custom eDSL with our toolchain to maintain control and facilitate future development of architecture-specific optimisations in the instruction set. However, implementing frontends for these already existing high-level languages would allow for a tighter integration with the current ecosystem.

The main contribution of this work is the introduction of a Haskell-based toolchain and eDSL for specifying and compiling quantum circuits for an FPGA-based architecture.
3.1 Core

The Core modules of the toolchain provide the constructs used in the specification of a quantum circuit. This includes primary definitions for types used throughout the tool and an inner Circuit type to represent a circuit over an indexed quantum register (i.e. very close to what the FPGA will actually process). On top of this Circuit type, the eDSL constructs are defined. This includes utilities for referring to qubits by names instead of indices (essentially defining arbitrary "quantum pointers"), arbitrary controls and negative controls defined over a gate or a set of gates, circuit chaining, looping and tiling subcircuits, etc.

```
fullAdd :: QReg -> QReg -> Qu -> Qu -> Circ
fullAdd in1 in2 c z = if length in1 /= length in2 then error "fullAdd: Input qubit register lengths must be identical." else let
  combinedRegister = c : interleave in2 in1
  in
  ladderQC 2 3 maj combinedRegister ++
  cnot (last in1) z ++
  reverseLadderQC 2 3 unmaj combinedRegister
```

Listing 1. Generic input size full Cuccaro adder and square circuit example implementation in the presented Haskell eDSL.

The Core modules also include two simulators, implemented in Haskell, for convenience. One is a general full state-vector QWM simulator with no optimisations which was used to model early QWM-based simulators. Additionally, a "logic" simulator is also provided which can simulate circuits containing only the \(\text{NOT} \) gate with any number of controls; this is useful for quickly debugging circuits which operate only in the computational basis. Since only one state is set at any point in the circuit, simulating such circuits can be performed in linear time and memory.

3.2 Testing

As is the case with classical software, effective unit testing of quantum circuits is very important. This involves running quantum circuits with different input states and checking that the output states fit some expectations. To facilitate automating this task, a testing framework is provided with the toolchain. Currently, the side of this which interacts with the FPGA simulator takes qubit preparations which it uses to compute the input state of the circuit. The circuit is then simulated by the FPGA and the output state is passed back into the toolchain (currently this is manual but automation is planned), decoded, and checked against the test expectations. There is also an option to run the tests against the included logic simulator, which proved particularly useful for debugging complex computational-basis circuits.

3.3 Compiler

The compiler modules include functions and tools for going from the eDSL representation to the FPGA instructions. Alternatively, the compiler can also read a QASM-like file specifying the circuit.

The compilation process is demonstrated in Figure 1. First, the specified circuit is verified, ensuring all qubits used are valid (have an index in the register) and no gates are specified with invalid target/controls. Then the named qubit identifiers are parsed away and the qubits are mapped to an index in the quantum register. At this point in the process, some constructs are still available to the tool which would not necessarily be available to the FPGA (like direct calls to a SWAP gate,
or a high number of controls), which need to be reduced away. SWAP gates are replaced with their equivalent CNOT specifications, negative controls are reduced by negating the control qubits before and after the gate, and gates with a higher number of controls than is supported are expanded to several gates with fewer controls. This results in a circuit which is ready to be converted to a QP (Quantum Problem) file which is simply a list of integers specifying the circuit. Taking into account the maximum number of controls allowed by the architecture, each emitted gate consists of its opcode, target qubit, followed by a constant number of controls. The resulting list is then written to disk, ready to be read by the simulator host.

3.4 Circuit Qubit Reduction

Quantum circuits representing quantum algorithms which employ computational-basis encoding of can have some qubits reduced out by generating two different circuits for each possible qubit input. In this way, the total memory required for one run of the circuit is reduced by half for each qubit reduced out. Qubits which are only used as controls throughout the circuit are ideal candidates for this type of reduction, and the toolchain provides functionality to automate this. While this approach is useful for reducing the total memory required across any platform, it is especially good for an FPGA which would, in theory, be able to run both (for one reduced qubit) circuits concurrently on completely independent memory spaces, which improves data locality.

As an example quantum-circuit transform, the Cuccaro modulo 4-qubit adder is considered. The original 9-qubit circuit is shown in Figure 2, where \(|a_3|a_2|a_1|a_0\rangle\) and \(|b_3|b_2|b_1|b_0\rangle\) represent the two 4-qubit inputs, so that \(|a_3|a_2|a_1|a_0\rangle\) remains unchanged and after completion \(|b_3|b_2|b_1|b_0\rangle\) holds the summation (for clarity renamed as \(|s_3|s_2|s_1|s_0\rangle\)). Since the qubits in \(|a_3|a_2|a_1|a_0\rangle\) are the same after completion, a transformation can be defined so that circuits for specific inputs \(|a_3|a_2|a_1|a_0\rangle\) are created. Also, if we move the input qubits that remain the same to the top of the circuit (here the most significant qubits), then 4-qubit circuits can be created that add a specific integer in 4-qbit binary representation. This transformation is illustrated here, where the qubits \(|a_3|a_2|a_1|a_0\rangle\) are first moved to top of circuit, as shown in Figure 2. Then, by specializing \(|a_3|a_2|a_1|a_0\rangle = |0001\rangle\), \(|a_3|a_2|a_1|a_0\rangle = |0010\rangle\) or \(|a_3|a_2|a_1|a_0\rangle = |0011\rangle\), the three example 4-qubit reduced circuits shown in Figure 3 can be created. One of the aims of the Haskell-based transformation tool is to perform this type of transformation automatically for more complex circuits where ‘constant’ qubits acting (predominantly) as control to gate operations on other qubits can be identified.

4 CONCLUSION AND FUTURE WORK

We presented a Haskell-based toolchain for compilation and optimisation of quantum circuits for the purpose of FPGA-based simulation. Currently, our toolchain facilitates encoding, debugging, and unit testing circuits before compiling to a QASM format specific to our FPGA architectures. Preliminary implementations of the described circuit qubit reduction optimisation are also included.
We demonstrate how these circuit reduction techniques can be applied to computational-basis circuits to facilitate splitting them to smaller circuits; reducing the memory required for simulation and benefiting customised parallel accelerators. Future work will focus on circuit analysis methods to facilitate implementing FPGA-specific optimisations including dynamic reconfiguration of the FPGA bitstream at runtime, cost-modelling of the memory and caches, and further automation of Circuit-Qubit Reduction transformations.

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