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LETTER

A Low Power Read-out Integrated Circuit for Multiple Sensors

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Abstract This paper proposes a low power read-out integrated circuit (ROIC) for multiple sensors having a DC output signal. It comprises a chopper-stabilized instrumentation amplifier (CSIA) followed by a second-order incremental analog-to-digital converter (IADC). The CSIA has a dual-frequency path to effectively eliminate any 1/f noise and offset. A variable gain module (VGM) is also connected to the CSIA to improve its range of potential applications. A CMOS buffer amplifier followed by the CSIA is used to achieve the ROIC’s linearity and drive capability. The back-end of the ROIC has a switched-capacitor IADC to provide a digital output. The correlated double sampling (CDS) technique was used in the IADC’s first integrator to reduce the offset and noise. The combination of these techniques enables the ROIC to achieve an input referred offset of 5 µV and a best error voltage of ±0.01 mV. The ROIC was implemented in 0.18 µm CMOS technology. It occupies an area of approximately 2.56 mm² and consumes 835 µA of current from a 1.6 V of supply voltage.

Key words: Chopper-stabilized, correlated double sampling, delta-sigma modulation, low power, sensor systems, switched-capacitor circuits.

Classification: Integrated circuits

1. Introduction

Currently, sensors are ubiquitous in our lives and indispensable in many applications across multiple areas such as in the automotive, medical, and consumer sectors [1-3]. For example, many parameters need to be measured and controlled in industrial automation systems, including pressure, position, temperature, vibration, humidity, and fluid properties. Different sensors are therefore required to measure a range of different parameters. In recent years, multiple sensors integrated onto the same chip have become a new trend in sensor development [4].

Most sensors, such as thermocouples, thermopile infrared (IR) sensors, and bridge transducers (Hall sensors and resistive Wheatstone bridge sensors), typically have a low-frequency output and small DC voltage signals of the millivolt-level [5-7]. Therefore, precision amplifiers are required to boost such small signals to levels that are compatible with the input ranges typical of the analog-to-digital converters of the read-out IC (ROIC). In contrast, CMOS is the preferred technology because of its low cost and the powerful capability of digital signal processing. However, in CMOS technology, the sensors and their ROIC exhibit non-idealities, such as offset and 1/f noise [8], which is the dominant noise source of the system because the sensor operates with a bandwidth of a few Hz that is near to DC. Therefore, the performance of the interface of the sensors with the ROICs has become increasingly important.

Instrumentation amplifiers (IAs), such as the three-opamp IA (3OIA), switched-capacitor IA, or capacitively-coupled IA are commonly used in ROIC [9], [10]. To achieve high resolution and a sufficient signal-to-noise ratio, the input referred error of the amplifier should be reduced to a sufficiently low level. Thus, the amplifier must have a low thermal and 1/f noise, high accuracy, and low drift. However, achieving these parameters is quite challenging for today’s mainstream CMOS technology whose inherent precision is limited by 1/f noise, component mismatch, gain error, and drift.

This paper proposes a low power ROIC to achieve improved performance. The front-end signal-conditioning module of a ROIC is a fully differential low noise and offset CSIA. This CSIA has a dual-frequency path to effectively eliminate 1/f noise and any residual offset. The back-end of the ROIC has a second-order IADC to provide a digital output. Correlated double sampling (CDS) was used in IADC’s integrator to reduce the offset voltage and error [11]. This ROIC can provide solutions for multiple sensors having a DC output signal.

The remainder of this paper is organized as follows. In Section 2, the system level design of the ROIC is described in detail, and Section 3 discusses circuit implementation. The measurement results and discussions of the proposed ROIC are presented in Section 4, and finally, Section 5 concludes the paper.

2. System level design

In a multiple sensor application, a thermocouple sensor, Hall magnetic sensor, and resistive Wheatstone bridge sensor are routinely used to measure the temperature, magnetic field, and pressure, respectively. The output of each sensor is connected to the ROIC by a switch.
according to time division multiple technology. Fig. 1 shows the block diagram of the ROIC studied in this paper. It comprises a CSIA, a VGM, a CMOS buffer amplifier, and an IADC. The ROIC employs a fully differential structure to diminish the harm caused by the common mode voltage of the sensors. Since different sensors have different output voltage amplitudes, the closed-loop gain of the CSIA is set through the VGM, which switches freely between 50 times and 300 times. The CSIA is chopped to achieve a low offset and low noise [12]. To achieve significant improvements in the linearity and drive capability of the ROIC, a high-swing CMOS buffer amplifier is used after the CSIA. The IADC employs a cascade of integrators with a feed forward (CIFF) structure [13]. The modulated offset is then averaged out by the digital decimation filter [14].

2.1 Dynamic offset cancellation techniques of CSIA
There are three types of CMOS dynamic offset cancellation techniques: trimming, auto-zeroing [15], and chopping [16]. According to a previous study [17], chopping is superior to trimming and auto-zeroing because it is a continuous-time modulation technique that does not cause noise folding. Therefore, chopping was applied in this work to achieve high power efficiency.

The topology of the proposed CSIA is shown in Fig. 2. The main operational amplifier, OTA1, has an offset voltage, $V_{OS1}$, and the stabilizing amplifier, OTA2, has an offset voltage, $V_{OS2}$. There is a dual-frequency path to eliminate the input referred error. The first path is the high-gain low-frequency path (HFP), which is formed by OTA1. The second path is the low-gain high-frequency path (LFP), formed by OTA2 and OTA3. The low-frequency noise and residual offset are determined by the LFP, while the unity gain frequency is determined by the HFP. Since OTA2 determines the low-frequency noise and the offset of the overall amplifier, OTA2 is chopped to eliminate its $1/f$ noise and to achieve a $\mu$V-level offset.

The chopper amplifier is composed of a stabilizing amplifier OTA2 and choppers CH1 and CH2 with a chopping frequency, $f_{ch}$, which senses the offset $V_{OS1}$ of the main amplifier OTA1. A switched-capacitor sample-and-hold notch filter (SC notch) is used to suppress the chopper ripple due to the chopped offset $V_{OS2}$ of OTA2.

As discussed in [18], the offset of the CSIA includes two main parts. One is due to the finite gain of the OTA, which can be expressed as

$$V_{OS, gain} \approx \frac{A_1}{A_2 A_3} V_{OS1}$$  \hspace{1cm} (1)

Where $A_1$, $A_2$, and $A_3$ are the DC gains of OTA1, OTA2, and OTA3, respectively. The other part is due to the parasitic output capacitor, $C_p$, at the output of OTA2 and can be expressed as

$$V_{OS, par} = \frac{4 f_{ch} C_p V_{OS1} G_{m1}}{G_{m2} G_{m3}}$$  \hspace{1cm} (2)

Where $G_{m1}$, $G_{m2}$, and $G_{m3}$ are the transconductances of OTA1, OTA2, and OTA3, respectively.

From the above discussion, the offset of the CSIA can be reduced in a number of ways; by reducing the $f_{ch}$, by reducing the size of MOS in OTA2 to reduce the $C_p$, by increasing $G_{m2}$ and $G_{m3}$ or by reducing $G_{m1}$. However, chopping gives rise to a chopper ripple at the OTA2 output. The equivalent amplitude of this ripple at the input of the CSIA can be approximated by

$$V_{in, ripple} \propto \frac{V_{OS1} G_{m2} G_{m3}}{f_{ch} G_{m1} C_L}$$  \hspace{1cm} (3)

Where $C_L$ is the load capacitor of the CSIA. According to (3), the ripple of the CSIA can be reduced by increasing $f_{ch}$, by reducing $G_{m2}$ and $G_{m3}$ or by increasing $G_{m1}$. Therefore, it is necessary to optimize the trade-off between the offset and the ripple when designing the CSIA. On the other hand, the input referred noise is largely determined by chopper CH1 and OTA2. The total input referred noise voltage can be expressed as

$$\bar{V}_{in}^2 \approx 2 \left(4 K T R_{ch} + \frac{4 K T \gamma}{g_{m1}} + \frac{4 K T \gamma g_{m, current}}{g_{m1}^2} \right)$$  \hspace{1cm} (4)

where $K$ is the Boltzmann constant, $T$ is the temperature, $\gamma$ is the noise coefficient (as a rule of thumb, it is assumed that $\gamma \approx 1$), $g_{m1}$ is the transconductance of the
differential pair in OTA2, $g_{m\_current}$ is the transconductance of the biasing MOS current sources in OTA2, and $R_{ch}$ is the channel on-state resistance of the chopper.

According to the chopping principle in the frequency domain, as can be seen in Fig. 2, the low-frequency errors, such as offset and noise, will be modulated and filtered out along with the offset.

2.2 Analysis of second-order IADC

The output of the CMOS buffer amplifier is digitized by a second-order IADC [19]. Fig. 3 illustrates the IADC employed in this paper, which comprises a second-order CIFF delta–sigma ($\Delta\Sigma$) modulator and a decimation filter. All memory elements are reset at the beginning of each conversion cycle. Then, an input voltage, $D_{IN}$, is applied to the input of the IADC for the first $n$ clock cycle and the output signal will be derived after the first $n$ clock cycles.

The noise transfer function is derived as follows:

$$NTF(z) = \frac{(z-1)^2}{(z-1)^2 + a_2b(z-1) + a_3bc}$$  \hspace{1cm} (5)

Where $a_2$, $a_3$, $b$ and $c$ are the coefficients in fig.3. Then, the IADC was designed using the delta–sigma toolbox in MATLAB. Dynamic-range scaling was performed to prevent loading the integrators and the quantizer, thus providing the values of the branch factors as shown in Fig.3.

![Fig. 3 Block diagram of the IADC.](image)

In DC and low-frequency measurements, it is important to suppress the noise. In this paper, a third-order sinc$^3$ filter is used to provide adequate noise suppression [20]. Its transfer function is given by:

$$H(z) = \frac{1}{M^3} \left( 1 - \frac{z^{-M}}{1 - z^{-1}} \right)^3$$  \hspace{1cm} (6)

Where $M$ is the decimation ratio. The final output $D[n]$ of the digital filter is given by:

$$D[n] = \frac{D_{IN}}{V_{ref}} + \frac{2!}{n(n-1)} \varepsilon$$  \hspace{1cm} (7)

Where $\varepsilon$ is the value of the quantization error and $V_{ref}$ is the reference voltage.

According to the behavioral simulation that considers most of the modulator nonidealities, the first integrator must have a DC gain of at least 140 dB to meet the accuracy requirements.

3. Circuit implementation

3.1 Main blocks CSIA design

Fig. 4 shows the schematic of OTA2 in the LPF which is the most important part of the CSIA [21]. The OTA2 is implemented as a fully differential folded cascade topology with a rail-to-rail input stage to achieve substantial swing. The current through MN3 and MN4 is controlled by the common mode feedback (CMFB) circuit designed with a differential pair MN7 and MN8, the gates of which connect to the output to hold the output CM voltage constant.

![Fig. 4 Schematic of OTA2.](image)

The SC notch is used to suppress the chopper ripple as it does not consume static power and improve energy efficiency [22]. The schematic of the SC notch filter is shown in Fig. 5(a) which is discussed in [23]. The SC notch filter comprises the transmission gates driven by CLK and CLKB and the capacitors C1 and C2, respectively. The operating principle of the SC notch filter is also depicted in Fig. 5(b). CH_CLK is the chopper clock signal.

![Fig. 5 (a) Schematic of the SC notch filter. (b) Operating principle of the SC notch filter.](image)

3.2 Design of VGM and CMOS buffer amplifier

As different sensors have different output ranges, as discussed in [5], a typically measured thermocouple voltage is 0–3 mV from 15 °C to 90 °C. ±15 mV with
the dc magnetic set form −15 to 15 mT as discussed in [6]. Herein, a VGM was used in the CSIA to configure different input ranges and improve the ROIC’s application. The block diagram of the VGM and its function table is shown in Fig. 6, which comprises variable resistors and analog switches.

To achieve significant improvements in the linearity and drive capability of the ROIC, a high-swing CMOS buffer amplifier was used after the CSIA. For large swing applications, the CMOS buffer amplifier uses class-AB at the output stage [24], [25]. Therefore, the output of the buffer \( D_{IN} \) is

\[
D_{IN} = V_{IN} \left( G \pm e \right)
\]

(8)

Where \( G \) is the closed-loop gain of the CSIA, which is about \( R_2/R_1 \), and \( e \) is the gain error of the CSIA’s closed-loop gain.

3.3 IDAC

Fig. 7 shows a schematic of the second-order ΔΣ modulator. The reference voltage, \( V_{REF} \), is set to 1.6 V, the sampling frequency is 1 MHz and the number clock period is 8192 to meet an 8ms conversion time. For maximum linearity, a single-bit DAC was employed [26].

The CDS technique is used in integrators to overcome the impacts of flicker noise and offset voltage. The CDS technique can decrease the noise and offset with a set of additional switches and capacitors, but at the same time it increases the loading capacitor since \( C_{CDS} \) is paralleled with the sampling capacitor \( C_{S1} \) and the parasitic capacitors. Therefore, it is necessary to optimize the trade-off between the offset and the speed when designing the IADC.

As stated in the above discussion, the first integrator must have a gain of about 100dB. However, a traditional folded cascode amplifier cannot meet this requirement [27]; therefore, a fully differential folded cascode amplifier with a gain-boosted stage was used herein (Fig. 8).

Fig. 8 Gain-boosted operational amplifier.

Fig. 9 Comparator.

4. Results and discussion

The proposed ROIC has been implemented in a standard 0.18 μm CMOS technology. A micrograph of the chip is shown in Fig. 10. The entire chip area including the ESD I/O pads is 1.62 × 1.65 mm². The chip consumed 835 μA current from a 1.6 V supply voltage. All of the results were measured at room temperature and verified from seven samples within one batch of a COB package.

Fig. 11 shows the measurement system setup, which is composed of a waveform generator (Keysight 3360A series), a digital multimeter (Keithley 2000), DAQ (National Instruments), FPGA (Altera DE2-115 Board), and a DC power supply (Agilent E3620A). An Altera DE2-115 Board was used to provide the necessary timing for the IADC circuit to ensure normal operation of the entire system.
Fig. 12 shows the measured input referred offset histogram of the ROIC, where it can be seen that the worst-case input referred offset is 5 µV, which is 200 times better than the performance of a previously reported ROIC [28]. and the quantization error of the IADC.

Fig. 14 shows the measured error voltage of the ROIC. As seen from Fig. 14(a), the worst-case error voltage of the ROIC is ±0.07 mV for a closed-loop gain of 50 times. Fig. 14(b) shows the measured error voltage at a different closed-loop gain of the VGM from 100 times to 300 times for Chip 2. To prevent overloading the integrators and the quantizer had a closed-loop gain of 300 times, and the input voltage range was ±5 mV. It can be seen that the worst-case error voltage of the ROIC is ±0.02 mV. The best-case error voltage of the ROIC was ±0.01 mV at a gain of 100 times.

The performance of the ROIC is summarized in Table I and compared with that of other state-of-the-art devices [28-30]. Compared with other designs, the power of the ROIC discussed in this paper is 1.3 mW, which is 1.8 times better than that of [28] and 5 times better than that of [30]. The conversion time of this paper is 2 ms, 25 times better than that of [28] and 85 times better than that of [29]. Moreover, the ROIC achieves a max input range of ±25 mV at a gain of 50.

5. Conclusion
To integrate multiple sensors with a DC output signal, a low power ROIC has been presented that comprises a CSIA with a VGM, a CMOS buffer amplifier, and a switched-capacitor IADC to improve its range of potential applications. The ROIC was implemented in a 0.18 µm CMOS technology. The ROIC combines...
chopping in CSIA with the CDS technique in IADC to achieve low offset and noise. The measurement results show that the offset and conversion time performance of the proposed ROIC exceeds the state-of-the-art circuits and has a best error voltage of ±0.01 mV.

| Item | This work | [28] * | [29] | [30] |
|------|-----------|-------|-----|-----|
| Year | 2019 | 2016 | 2012 | 2011 |
| Technology | 0.18 µm | 0.18 µm | 0.7 µm | 0.35 µm |
| Die area (mm2) | 2.56 | 0.45 | 6 | 1.2 |
| Supply voltage (V) | 1.6 | 1.55 | 5 | 3.3 |
| Supply current (µA) | 835 | 1660 | 270 | 2000 |
| Input range (mV) | ±25 | ±10** | ±40 | ±1.65 |
| Gain range | 50-300 | 50-300 | 50-300 | 50-300 |
| Input referred offset (µV) | 5 | 100 | 0.048 | - |
| Conversion time (ns) | 50 | 170 | 4.11 |
| Architecture*** | CSA*+DT-DSM | OTA*+CT-DSM | CFI已久DT-DSM | SHA*+DT-DSM |

* The data of [28] includes only the fractions of ADC and IA.
** Calculated as full scale range/max IA gain.
*** DT-DSM = discrete-time ΔΣ modulator; CT-DSM = continuous-time ΔΣ modulator; CFI已久 = current-feedback instrumentation amplifier; SHA已久 = sample and hold amplifier.

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