Robust Offset-Cancellation Sense Amplifier for an Offset-Canceling Dual-Stage Sensing Circuit in Resistive Nonvolatile Memories

Taehui Na
Department of Electronics Engineering, Incheon National University, Incheon 22012, Korea; taehui.na@inu.ac.kr; Tel.: +82-32-835-8452

Received: 14 August 2020; Accepted: 28 August 2020; Published: 30 August 2020

Abstract: With technology scaling, achieving a target read yield of resistive nonvolatile memories becomes more difficult due to increased process variation and decreased supply voltage. Recently, an offset-canceling dual-stage sensing circuit (OCDS-SC) has been proposed to improve the read yield by canceling the offset voltage and utilizing a double-sensing-margin structure. In this paper, an offset-canceling zero-sensing-dead-zone sense amplifier (OCZS-SA) combined with the OCDS-SC is proposed to significantly improve the read yield. The OCZS-SA has two major advantages, namely, offset voltage cancellation and a zero sensing dead zone. The Monte Carlo HSPICE simulation results using a 65-nm predictive technology model show that the OCZS-SA achieves 2.1 times smaller offset voltage with a zero sensing dead zone than the conventional latch-type SAs at the cost of an increased area overhead of 1.0% for a subarray size of 128 x 16.

Keywords: nonvolatile memory (NVM); offset voltage; offset-canceling dual-stage sensing circuit (OCDS-SC); read yield; sense amplifier (SA); sensing dead zone; time-diﬀerence inputs

1. Introduction

Although resistive nonvolatile memories (NVMs) such as spin-transfer-torque random access memory (RAM) and resistive RAM promise higher density and lower power than conventional memories such as static RAM, dynamic RAM, and Flash memory [1–3], they suffer from degraded read yield following technology scaling due to the increased process variation, reduced supply voltage, and decreased read cell current ($I_{\text{read}}$) [4–6].

In general, two output voltages of a sensing circuit (SC), namely, $V_{\text{SA, data}}$ and $V_{\text{SA, ref}}$, are introduced into a sense amplifier (SA) to generate a digital signal (zero or one) [7]. Considering the offset voltage in the SA ($V_{\text{OS}}$) and assuming that the statistical distributions of the input voltage diﬀerence ($\Delta V$) between $V_{\text{SA, data}}$ and $V_{\text{SA, ref}}$ as well as $V_{\text{OS}}$ are modeled by a Gaussian distribution, the read yield can be statistically expressed as the read-access pass yield for a single cell ($\text{RAPY}_{\text{CELL}}$) [8], i.e.,

$$\text{RAPY}_{\text{CELL}} = \frac{\mu_{\Delta V} - \mu_{\text{OS}}}{\sqrt{\sigma_{\Delta V}^2 + \sigma_{\text{OS}}^2}},$$

where $\mu_{\Delta V}$ ($\mu_{\text{OS}}$) and $\sigma_{\Delta V}$ ($\sigma_{\text{OS}}$) are the mean and standard deviation of $\Delta V$ ($V_{\text{OS}}$), respectively.

The recently proposed offset-canceling dual-stage SC (OCDS-SC) has improved $\text{RAPY}_{\text{CELL}}$ by reducing $\sigma_{\Delta V}$ due to the offset voltage cancellation in the SC and by increasing $\mu_{\Delta V}$ due to the double-sensing-margin structure [6]. Figure 1a shows an example of the $\Delta V$ distribution of the OCDS-SC with $\mu_{\Delta V} = 200$ mV and $\sigma_{\Delta V} = 23$ mV. Figure 1b shows that $\text{RAPY}_{\text{CELL}}$ can be significantly improved by developing a novel SA with much smaller $\sigma_{\text{OS}}$ than the typical $\sigma_{\text{OS}}$ value of 20 mV [7]. If the improved $\text{RAPY}_{\text{CELL}}$ value is greater than a target $\text{RAPY}_{\text{CELL}}$ value, the read energy can be significantly saved by trading-oﬀ the improvement in $\text{RAPY}_{\text{CELL}}$ [9,10].

Electronics 2020, 9, 1403; doi:10.3390/electronics9091403 www.mdpi.com/journal/electronics
(VLSA) is used. Figure 3 shows the capacitive-coupling problem in the VLSA in which a capacitive-coupling problem occurs when a conventional voltage-latched SA (VLSA) is used. Figure 3 shows the capacitive-coupling problem in the VLSA in which a capacitive-coupling problem occurs when a conventional voltage-latched SA (VLSA) is used. The remainder of this paper is organized as follows: Section 2 describes the problems in conventional latch-type SAs; Section 3 introduces the proposed OCZS-SA; Section 4 presents the simulation results and comparison; and Section 5 presents the conclusions drawn from our study.

2. Problems in Conventional Latch-Type SAs

In this paper, we propose an offset-canceling zero-sensing-dead-zone SA (OCZS-SA) that is capable of significantly reducing $\sigma_{SA,OS}$ by offset-voltage cancellation with a zero-sensing-dead-zone characteristic. The proposed OCZS-SA achieves 2.1 times smaller $\sigma_{SA,OS}$ of 9.62 mV without any sensing dead zone at the cost of an increased area overhead of 1.0% for a subarray size of $128 \times 16$. The remainder of this paper is organized as follows: Section 2 describes the problems in conventional latch-type SAs; Section 3 introduces the proposed OCZS-SA; Section 4 presents the simulation results and comparison; and Section 5 presents the conclusions drawn from our study.

(a) Example of $\Delta V$ distribution of the offset-canceling dual-stage sensing circuit (OCDS-SC) at $\mu_{\Delta V} = 200$ mV and $\sigma_{\Delta V} = 23$ mV. (b) RAPYCELL according to $\sigma_{SA,OS}$.

In the OCDS-SC, two SA input voltages, $V_{SA,\text{data}}$ and $V_{SA,\text{ref}}$, are generated with a time difference due to the dual-stage sensing operation, as shown in Figure 2. In the first stage, $SS1$ is activated, and $V_{SA,\text{data}}$ generated in the OCDS-SC is introduced into the SA. In the second stage, $SS2$ is activated, and $V_{SA,\text{ref}}$ generated in the OCDS-SC is introduced into the SA. However, because of the time-difference input, a capacitive-coupling problem occurs when a conventional voltage-latched SA (VLSA) is used. Figure 3 shows the capacitive-coupling problem in the VLSA in which $V_{SA,\text{ref}}$ changes $V_{SA,\text{data}}$ to some extent ($\Delta$) through parasitic capacitors. This problem increases $\sigma_{SA,OS}$ from 20 mV to 30–50 mV, depending on the ratio of the output loading capacitance to the parasitic capacitance. Thus, the SA for the OCDS-SC should not be a VLSA type to avoid the capacitive-coupling problem.

Figure 2. Schematics of the OCDS-SC and symbolized sense amplifier (SA).
with a sensing dead zone cannot be applied to the OCDS-SC to achieve a supply-rail sensing capability. Figure 4 shows the sensing-dead-zone problem in a CLSA with an NMOS footswitch (FS-CLSA) and (b) headswitch (HS)-CLSA [7]. In the FS-CLSA, the input transistors (MN3 and MN4) should be turned on for correct operation, which means that \( V_{SA_{data}} > V_{THN} \) to turn on MN3/MN4, \( \Rightarrow \) Sensing dead zone: \( V_{SA_{data}} < V_{THN} \) and \( V_{SA_{data}} < V_{DD} - |V_{THP}| \) to turn on MP3/MP4, \( \Rightarrow \) Sensing dead zone: \( V_{SA_{data}} > V_{DD} - |V_{THP}| \).

3. Proposed OCZS-SA

In this section, we propose the OCZS-SA that offers two major advantages of offset voltage cancellation and zero sensing dead zone.
3.1. Circuit Diagram and Operation

Figure 5 shows the schematic and timing diagrams of the proposed OCZS-SA. Before we explain the OCZS-SA operation in detail, we should note that the OCZS-SA operation is fully pipelined with the OCDS-SC operation, as shown in the timing diagram in Figure 5. Phases 1 and 2 of the OCZS-SA are pipelined during SS1, and phases 3 and 4 are pipelined during SS2. Thus, the OCZS-SA does not incur any sensing delay penalty.

![Figure 5. Schematic and timing diagrams of the proposed offset-canceling zero-sensing-dead-zone SA (OCZS-SA).](image)

Figure 6 shows the detailed operations of the OCZS-SA. Before phase 1, the PRE signal is high, and the gates of the input NMOSs (IN and INB) are precharged to \( V_{DD} \). During phase 1 (Figure 6a), the \( P1 \) signal is activated, and the IN and INB nodes are discharged to threshold voltages \( V_{TH1} \) and \( V_{TH2} \) of the input NMOSs, respectively, by the diode-connected configuration. The OUT and OUTB nodes remain GND to isolate the IN and INB nodes. In phase 2 (Figure 6b), the \( P2 \) signal is activated, and \( V_{SA_data} \) is captured at both the IN and INB nodes by the capacitive coupling of \( C_{SA} \). As a result, the voltages in the IN and INB nodes become \( V_{TH1} + V_{SA_data} \) and \( V_{TH2} + V_{SA_data} \), respectively. Simultaneously, the OUT and OUTB nodes are precharged to \( V_{DD} \) for reliable sensing operation. In phase 3 (Figure 6c), the \( P3 \) signal is activated, and the OCZS-SA waits for \( V_{SA_ref} \) to be generated in the OCDS-SC. In phase 4 (Figure 6d), the \( P4 \) signal is activated, and \( V_{SA_ref} \) is captured at the INB node. Thus, the voltages in the IN and INB nodes \( V_{IN} \) and \( V_{INB} \) become \( V_{TH1} + V_{SA_data} \) and \( V_{TH2} + V_{SA_data} \), respectively. After phase 4, the SAE signal is activated, and a digital signal (zero or one) is generated by the voltage difference between \( V_{IN} (= V_{TH1} + V_{SA_data}) \) and \( V_{INB} (= V_{TH2} + V_{SA_ref}) \). We note that the operation after phase 4 is the same as that in the FS-CLSA.
3.2. First Advantage: Offset Voltage Cancellation

The first advantage of the OCZS-SA is the offset voltage cancellation of the two input NMOSs. As mentioned earlier, in phase 4, $V_{IN}$ and $V_{INB}$ become $V_{TH1} + V_{SA\_data}$ and $V_{TH2} + V_{SA\_ref}$, respectively. Because the overdrive voltage ($= V_{GS} - V_{TH}$) of the input NMOS, where $V_{GS}$ is the input NMOS gate-to-source voltage, does not depend on the $V_{TH}$ variation, a $V_{TH}$ mismatch between the two input NMOSs does not influence $\sigma_{SA\_OS}$.

In addition, in the FS-CLSA (Figure 4a), because $\sigma_{SA\_OS}$ is dominantly determined by the input NMOSs, $\sigma_{SA\_OS}$ can be effectively reduced by canceling only the offset in the input NMOSs. Figure 7 shows $\sigma_{SA\_OS}$ of the FS-CLSA according to the SA input voltage ($V_{SA\_data}$) when process variation is applied only to the input NMOSs (MN3 and MN4), only to the latch NMOSs (MN1 and MN2), only to the latch PMOSs (MP1 and MP2), and to all the transistors. Figure 7 clearly shows that $\sigma_{SA\_OS}$ is more sensitive to the input NMOSs than to the transistors because the input NMOSs operate in the saturation region, whereas the latch NMOSs operate in the linear region. Thus, the $V_{TH}$ mismatch between MN1 and MN2 becomes less sensitive. Meanwhile, the latch PMOSs do not operate at the initial sensing period. Thus, the $V_{TH}$ mismatch between MP1 and MP2 becomes negligible. The variation in the latch NMOSs of the FS-CLSA has more effect on the $\sigma_{SA\_OS}$ as $V_{SA\_data}$ increases because the initial voltage in the small parasitic capacitance between MN1 (MN2) and MN3 (MN4) is discharged much faster with increasing $V_{SA\_data}$, resulting in the latch NMOSs operating in the saturation region.
VLSAs such as the VLSA with an NMOS footswitch and PMOS access transistors, VLSA with a PMOS VLSA with double switches and transmission gate access transistors (DSTA-VLSA) without C

Thus, the variation in the latch NMOSs of the OCZS-SA significantly affected V

On the other hand, Figure 8 clearly shows that the OCZS-SA achieved 2.1 times smaller applied to the DSTA-VLSA. The FS-CLSA and HS-CLSA suffer from the sensing-dead-zone problem. Unlike the FS-CLSA with a sensing dead zone in the region of V_SA_data < V_THN, as shown in Figure 7, the OCZS-SA does not have any sensing dead zone because in phase 4, V_IN and V_INB are always greater than V_TH1 and V_TH2, respectively, even if V_SA_data and V_SA_ref are 0 V. Thus, supply-rail sensing capability is achieved.

3.3. Second Advantage: Zero Sensing Dead Zone

Unlike the FS-CLSA with a sensing dead zone in the region of V_SA_data < V_THN, as shown in Figure 7, the OCZS-SA does not have any sensing dead zone because in phase 4, V_IN and V_INB are always greater than V_TH1 and V_TH2, respectively, even if V_SA_data and V_SA_ref are 0 V. Thus, supply-rail sensing capability is achieved.

4. Simulation Results and Comparison

HSPICE Monte Carlo simulations were performed using a 65-nm predictive technology model at V_DD = 1.1 V. To fully pipeline the operation with the OCDS-SC, each phase operation time (T_P1, T_P2, T_P3, and T_P4 for phases 1–4, respectively) was set to 0.5 ns.

Figure 8 shows σ_SA_OS according to the SA input voltage (V_SA_data) of the FS-CLSA, HS-CLSA, VLSA with double switches and transmission gate access transistors (DSTA-VLSA) without time-difference inputs, DSTA-VLSA with time-difference inputs, and OCZS-SA. Among the various VLSAs such as the VLSA with an NMOS footswitch and PMOS access transistors, VLSA with a PMOS headswitch and NMOS access transistors, and DSTA-VLSA, only the latter is compared in this paper because only the DSTA-VLSA can achieve a zero sensing dead zone [7]. As mentioned in Section 2, the capacitive-coupling problem increases σ_SA_OS of the DSTA-VLSA when time-difference inputs are applied to the DSTA-VLSA. The FS-CLSA and HS-CLSA suffer from the sensing-dead-zone problem. On the other hand, Figure 8 clearly shows that the OCZS-SA achieved 2.1 times smaller σ_SA_OS of 9.62 mV on average (minimum σ_SA_OS = 5.07 mV at V_SA_data = 0.3 V; maximum σ_SA_OS = 25.41 mV at V_SA_data = 1.1 V) with a zero sensing dead zone. In the same manner as that of the FS-CLSA, the variation in the latch NMOSs of the OCZS-SA significantly affected σ_SA_OS as V_SA_data increased. Thus, σ_SA_OS tended to increase with V_SA_data.

Figure 9 shows the average σ_SA_OS of the OCZS-SA according to the width of the PMOSCAP for C_SA (W_CSA) when the PMOSCAP length (L_CSA) was 0.2 μm. By considering the area overhead, a W_CSA value of 2.0 μm was selected. We note that the effect of the C_SA size on the loading of the OCDS-SC is negligible because C_SA was serially coupled to the input capacitance (C_IN) at nodes IN and INB (total loading capacitance = C_SA/C_IN ≈ C_IN).

Figure 10 shows normalized σ_SA_OS of the OCZS-SA according to T_P1. Because σ_SA_OS is saturated at T_P1 of approximately 0.2 ns, the OCZS-SA can be fully pipelined without any problem.
loading capacitance =

By employing the OCZS-SA together with the OCDS-SC, the OCZS-SA can be fully pipelined without any problem. From the array architecture viewpoint, however, the OCZS-SA requires 37% more layout area (Figure 11a) and 125% of the OCZS-SA, which sacrifices some of the improvement in CELL.

Table 1 lists the performance summary and comparison between the proposed OCZS-SA and conventional SAs. The OCZS-SA achieves minimum \( \sigma_{SA_OS} \) of 9.62 mV on average (minimum \( \sigma_{SA_OS} \) = 5.07 mV at \( V_{SA_data} = 0.3 \) V; maximum \( \sigma_{SA_OS} \) = 25.41 mV at \( V_{SA_data} = 1.1 \) V).

Table 1. Performance summary and comparison between the proposed OCZS-SA and conventional latch-type SAs. The OCZS-SA achieved a zero sensing dead zone and a 2.1 times...
smaller $\sigma_{SA,OS}$ of 9.62 mV, on average, than the FS-CLSA. From the SA viewpoint, owing to the additional transistors and phases, the OCZS-SA requires 37% more layout area (Figure 11a) and 125% more read energy compared with the FS-CLSA. From the array architecture viewpoint, however, the area overhead is only 1.0% when the subarray size is 128 × 16 (Figure 11b), and it decreases as the subarray size increases. In addition, the read-energy consumption of the SC part is much greater (>70 fJ [6]) than that of the SA part. As a result, if $R\text{APY}_{\text{CELL}}$, which is improved by employing the OCZS-SA, is greater than a target $R\text{APY}_{\text{CELL}}$, the total read energy in the SC and SA can be saved by reducing the SC operation time ($T_{\text{SC}}$) and/or $I_{\text{read}}$. This result can be achieved in spite of the higher read energy of the OCZS-SA, which sacrifices some of the improvement in $R\text{APY}_{\text{CELL}}$ but satisfies target $R\text{APY}_{\text{CELL}}$. By employing the OCZS-SA together with the OCDS-SC, $R\text{APY}_{\text{CELL}}$ increases from 6.0$f$ to 8.7$f$. The $R\text{APY}_{\text{CELL}}$ values of 6.0$f$ and 8.7$f$ correspond to sensing error rates of $9.87 \times 10^{-10}$ and $1.66 \times 10^{-18}$, respectively. Therefore, the OCZS-SA yields an eighth-order improvement in the read yield relative to the conventional SAs.

Table 1. Performance summary and comparison between the proposed OCZS-SA and conventional latch-type SAs.

|                  | DSTA-VLSA | FS-CLSA | OCZS-SA |
|------------------|-----------|---------|---------|
| Average $\sigma_{SA,OS}$ (mV) | 33.8 ¹) | 20.0 ²) | 9.62 |
| Sensing dead zone | None | $V_{\text{SA, data}} < V_{\text{THN}}$ | None |
| Normalized area overhead (SA viewpoint) | 0.95 | 1 | 1.37 |
| Normalized area overhead (Array viewpoint) | 0.999 | 1 | 1.010 |
| Normalized read energy/bit (SA viewpoint) | 0.94 | 1 | 2.25 |
| Normalized read energy/bit (SC + SA viewpoint) | 1.43 | 1 | 0.84 |

¹) Due to the capacitive coupling problem. ²) Sensing dead zone is not included. ³) Read energy when the minimum $I_{\text{read}}$ that satisfies a target $R\text{APY}_{\text{CELL}}$ of 6$f$ is applied at $T_{\text{SC}} = 2$ ns.

Figure 11. (a) Simplified layouts of DSTA-VLSA, FS-CLSA, and OCZS-SA. (b) Estimated array architecture areas when DSTA-VLSA, FS-CLSA, and OCZS-SA are employed.

Figure 12 shows that the minimum $I_{\text{read}}$ that satisfies a target $R\text{APY}_{\text{CELL}}$ value of 6$f$ is reduced by 21–32% by sacrificing the improvement in $R\text{APY}_{\text{CELL}}$. Figure 13 shows that the read energy in the SC and SA is accordingly reduced by approximately 13–16%.
Conflicts of Interest:
This work was supported by Incheon National University Research Grant in 2020.

The conventional latch-type SAs cannot be applied to the OCDS-SC due to the capacitive-coupling and sensing-dead-zone problems. In this paper, we have proposed the OCZS-SA, which offers two major advantages: offset voltage cancellation and zero sensing dead zone. The simulation results prove that the OCZS-SA can achieve a 2.1 times smaller $\sigma_{SA,OS}$ value of 9.62 mV without any sensing dead zone at the cost of an increased area overhead of 1.0% for a subarray size of 128 $\times$ 16. Furthermore, a 13–16% read-energy saving is achieved due to the 21–32% reduction in $I_{\text{read}}$. Thus, the OCZS-SA can be a compelling candidate for the OCDS-SC in deep submicrometer resistive NVMs.

5. Conclusions

The conventional latch-type SAs cannot be applied to the OCDS-SC due to the capacitive-coupling and sensing-dead-zone problems. In this paper, we have proposed the OCZS-SA, which offers two major advantages: offset voltage cancellation and zero sensing dead zone. The simulation results prove that the OCZS-SA can achieve a 2.1 times smaller $\sigma_{SA,OS}$ value of 9.62 mV without any sensing dead zone at the cost of an increased area overhead of 1.0% for a subarray size of 128 $\times$ 16. Furthermore, a 13–16% read-energy saving is achieved due to the 21–32% reduction in $I_{\text{read}}$. Thus, the OCZS-SA can be a compelling candidate for the OCDS-SC in deep submicrometer resistive NVMs.

Funding: This work was supported by Incheon National University Research Grant in 2020.

Conflicts of Interest: The author declares no conflict of interest.

References

1. Kawahara, A.; Azuma, R.; Ikeda, Y.; Kawai, K.; Katoh, Y.; Hayakawa, Y.; Tsuji, K.; Yoneda, S.; Himeno, A.; Shimakawa, K.; et al. An 8 Mb Multi-Layered Cross-Point ReRAM Macro With 443 MB/s Write Throughput. *IEEE J. Solid State Circuits* **2012**, *48*, 178–185. [CrossRef]

2. Lin, C.; Kang, S.; Wang, Y.; Lee, K.; Zhu, X.; Li, X.; Hsu, W.; Kao, Y.; Liu, M.; Chen, W.; et al. 45nm low power CMOS logic compatible embedded STT MRAM utilizing a reverse-connection 1T/1MTJ cell. *IEEE Int. Electron Devices Meet. (IEDM)* **2009**, 1–4. [CrossRef]
3. Rizzo, N.D.; Houssameddine, D.; Janesky, J.; Whig, R.; Mancoff, F.B.; Schneider, M.L.; de Herrera, M.; Sun, J.J.; Nagel, K.; Deshpande, S.; et al. A Fully Functional 64 Mb DDR3 ST-MRAM Built on 90 nm CMOS Technology. IEEE Trans. Magn. 2013, 49, 4441–4446. [CrossRef]

4. Chang, M.-F.; Shen, S.-J.; Liu, C.-C.; Wu, C.-W.; Lin, Y.-F.; King, Y.-C.; Lin, C.-J.; Liao, H.-J.; Chih, Y.-D.; Yamauchi, H. An Offset-Tolerant Fast-Random-Read Current-Sampling-Based Sense Amplifier for Small-Cell-Current Nonvolatile Memory. IEEE J. Solid State Circuits 2013, 48, 864–877. [CrossRef]

5. Na, T.; Kim, J.; Kim, J.P.; Kang, S.H.; Jung, S.-O. Reference-Scheme Study and Novel Reference Scheme for Deep Submicrometer STT-RAM. IEEE Trans. Circuits Syst. I Regul. Pap. 2014, 61, 3376–3385. [CrossRef]

6. Na, T.; Kim, J.; Kim, J.P.; Kang, S.H.; Jung, S.-O. A Double-Sensing-Margin Offset-Canceling Dual-Stage Sensing Circuit for Resistive Nonvolatile Memory. IEEE Trans. Circuits Syst. II Express Briefs 2015, 62, 1109–1113. [CrossRef]

7. Na, T.; Woo, S.-H.; Kim, J.; Jeong, H.; Jung, S.-O. Comparative Study of Various Latch-Type Sense Amplifiers. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 2013, 22, 425–429. [CrossRef]

8. Nho, H.; Yoon, S.-S.; Wong, S.; Jung, S.-O. Numerical Estimation of Yield in Sub-100-nm SRAM Design Using Monte Carlo Simulation. IEEE Trans. Circuits Syst. II Express Briefs 2008, 55, 907–911. [CrossRef]

9. Na, T.; Kim, J.; Kim, J.P.; Kang, S.H.; Jung, S.-O. An Offset-Canceling Triple-Stage Sensing Circuit for Deep Submicrometer STT-RAM. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 2014, 22, 1620–1624. [CrossRef]

10. Na, T.; Kim, J.P.; Kang, S.H.; Jung, S.-O. Read Disturbance Reduction Technique for Offset-Canceling Dual-Stage Sensing Circuits in Deep Submicrometer STT-RAM. IEEE Trans. Circuits Syst. II Express Briefs 2016, 63, 578–582. [CrossRef]

11. Kim, J.; Ryu, K.; Kang, S.H.; Jung, S.-O. A Novel Sensing Circuit for Deep Submicron Spin Transfer Torque MRAM (STT-MRAM). IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 2010, 20, 181–186. [CrossRef]

12. Na, T.; Kang, S.H.; Jung, S.-O. Distribution Analysis and Multiple-point Tail Fitting Yield Estimation Method for STT-MRAM. J. Semicond. Technol. Sci. 2020, 20, 271–280. [CrossRef]

© 2020 by the author. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).