Accelerated degradation HEMT based on AlGaN / SiC

A S Evseenkov1, V G Tikhomirov1

1Saint-Petersburg Electrotechnical University “LETI”, Prof. Popova 5, St. Petersburg 197376, Russia

Abstract. Created HEMT based on the structures of the AlGaN/SiC. Was studied all the basic characteristics of the transistors and determine their operating parameters, including power, Gm, delay time, current saturation, etc. A study was made of the degradation of the characteristics of transistors under stress conditions of operation. Modes of express testing were found that allow to estimate the reliability of HEMT. Based on the results of the field distribution simulation was carried out near the gate for a more detailed description of the degradation mechanisms.

1. Introduction

Currently heteroepitaxial structures of group III nitrides are actively replacing traditional AIIIB5 materials on the basis of gallium arsenide in the optical and microwave electronics [1-3]. Large values of electron concentration in the channel in combination with high breakdown fields make it possible to provide a microwave power density in GaN-based field effect transistors 5-10 times larger than in GaAs-based devices. In the transition to a new group of materials, the use of silicon nitride as a dielectric becomes particularly topical. There are a number of problems arising from the operation of HEMT based on nitrides in microwave modes. In connection with the increasing current densities, the issue of heating the device and its degradation resistance is acute [4]. The temperature of the working area of the device can exceed 150 degrees Celsius. One of the most important problems is the presence in the transistor structures of defects of various types, which substantially reduce both the speed and power of the device. This is especially evident with prolonged operation of the device. Possible degradation can cause both changes in the instrument parameters beyond the specification limits, as well as a complete failure of the device.

2. The samples

For the experiment, several AlGaN/SiC wafers were made, on which HEMT with a gate width of 720 μm and a length of 0.5 μm are placed. SiC was used as a substrate, on which the epitaxial transistor structures, shown in figure 1, were grown. The main functional layers are: barrier layer Al0.25Ga0.75N, sub-buff layer of AlN, GaN channel layer and the top layer Al0.3Ga0.65N. As the dielectric silicon nitride was used. The wafer was divided into individual transistors from which for further experiments control samples were selected on the following parameters: the saturation current - 310 to 360 mA and a cut-off voltage - not less than 5 V, the leakage current at 60 V – no more than 800 microamps.
3. Experiment

Created HEMTs passed extensive testing, including a study of the basic characteristics and identification of operating parameters. In particular, their power parameters, delay times, saturation currents, etc. were determined. The test was conducted for continuous operation of transistors. The voltage at the source-drain was 0 Volts, while the voltage from -10 to -50 V was applied to the gate-drain. It should be noted that the voltage did not go to 0 V between the readings at the measurement points, but kept on a constant bar for 1 minute.

The volt-ampere characteristic for comparison with the degradation tests was investigated and without a slight delay between the measurements. After a cycle of staggered degradation, there was a sharp increase in reverse currents through the gate at a critical voltage equal to 32 V (Figure 3). The experiment included a series of samples of 10 transistors, most of which showed similar dependencies. On average, the sample changed its characteristics as follows: reduction of saturation currents from 360 to 345 mA, leakage currents increased from 40 to 160 μA, the drainage losses increased from 17 to 21%.
A sharp increase in the leakage current under the indicated experimental conditions was observed by groups of researchers from leading scientific laboratories and described in [7,8]. To date, one of the common explanations is that when a high electric field intensity occurs under the gate due to the inverse piezoelectric effect, crystallographic defects appear in the material of the barrier layer, which serve as trap centers for the electrons of the shutter material and allow them to enter the channel layer, creating a leakage current through the shutter. The described mechanism is clearly shown in Fig. 5.

From the consideration of the leakage current paths in this image, it can be seen that the key initial factor triggering this mechanism is the distribution of the electric field under the gate. However, in known published works, there is no detailed analysis of the electric field in the gate region at a depth of the order of a dozen nanometers. Despite the seeming obviousness of the problem, a reliable calculation of the distribution of the electric field under the gate with reverse bias has a number of complex features. For example, layers of different semiconductor and dielectric materials under the gate have the dimensions of one and tens of nanometers. In this case, at a depth of 20-30 nm there is a heteroboundary directly below which is a 2D electron gas (2DEG) of very high concentration. The layers have essentially different properties and the exact calculation of the depletion region under the
gate, taking into account the whole set of their characteristics and the influence of the interface between the layers, is a very difficult task. In turn, the distribution of the electric field strength determines the force and the area of mechanical action on the barrier layer due to the inverse piezoelectric effect and, as a consequence, the probable paths of leakage current flow. It can be, as vertical breakdown, and lateral, or some intermediate, directed towards the nearest electrode with zero potential. With a strictly symmetrical arrangement of the gate between the source and the drain, it is obvious that the field will also have a symmetrical character and the path of the breakdown current will be determined by the inhomogeneities at the edge of the shutter, fig.5.

![Electric Field Distribution](image)

**Figure 5.** The result of the numerical calculation of the electric field of the gate region of one of the basic variants of the design of the transistor.

To confirm the observed effect, numerical modeling was carried out using a developed package of subprograms that worked together with known numerical modeling systems and described by the authors in previous publications [5].

Figure 6 shows the result of such a numerical calculation of the electric field of the gate region of one of the basic variants of the design of the transistor. Analyzing the results of the calculation, we can conclude that the main gradient of the field is located almost entirely in the barrier layer, and the electric field strength reaches under the gate and near the channel several megavolts per centimeter.

Thus, it becomes clear that one of the main mechanisms of degradation is the inverse piezoelectric effect [6-8], which leads to irreversible damage to the structure of the transistor when the field strength is reached above the threshold, which ultimately can lead to the formation of defects on the edge of the shutter on side drain [9]. One of the other factors that degrade performance is the hot charge carriers, which pass into the gate region as a result of the Paul-Fraenkel mechanisms [10]. The current-voltage gate-drain characteristic of the transistor after a degradation is shown in Figure 6.
Figure 6. Volt Ampere characteristic gate-drain transistor after a different number of cycles of degradation

4. Conclusion

Thus, during work, transistors with high electron mobility based on AlGaN / SiC structures were created. The gate width was 720 μm, the length was 0.3 μm. All the basic characteristics of transistors were studied and their operating parameters were determined: steepness, source lags, saturation currents, etc. To evaluate the reliability of transistors, a stepwise express degradation test was developed, which is especially important for this class of devices. Intensive degradation began in the samples, beginning with a critical voltage equal to 31 volts. The sample changed its characteristics as follows: reduction of saturation currents from 360 mA to 345 mA, leakage currents increased from 60 μA to 160 μA, lags increased from 17 to 21%. With the subsequent repetition of degradation cycles, the degradation process continued until the transistor failed.

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