Designs for a two-dimensional Si quantum dot array with spin qubit addressability

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Electron spins in Si are an attractive platform for quantum computation, backed with their scalability and fast, high-fidelity quantum logic gates. Despite the importance of two-dimensional integration with efficient connectivity between qubits for medium- to large-scale quantum computation, however, a practical device design that guarantees qubit addressability is yet to be seen. Here, we propose a practical 3 × 3 quantum dot device design and a larger-scale design as a longer-term target. The design goal is to realize qubit connectivity to the four nearest neighbors while ensuring addressability. We show that a 3 × 3 quantum dot array can execute four-qubit Grover’s algorithm more efficiently than the one-dimensional counterpart. To scale up the two-dimensional array beyond 3 × 3, we propose a novel structure with ferromagnetic gate electrodes. Our results showcase the possibility of medium-sized quantum processors in Si with fast quantum logic gates and long coherence times.

Results
3 × 3 QD array. Figure 1 illustrates our proposal of a 3 × 3 QD array. Figure 1a shows a model in which nine QDs are formed within a Si/SiGe heterostructure. We assume QD regions of 70-nm squares (red regions) separated by 50-nm barrier gates (deep blue regions) that are used to control exchange interactions between the adjacent QDs. The reservoirs (orange regions) connected to ohmic contacts (not shown) supply electrons to the QDs.

We consider two approaches to deplete electrons outside the QDs and reservoirs. The first one is etching followed by Al deposition and the second one is to use screening gates. Figure 1b shows a layer-by-layer schematic of overlapping Al gates12 in the first approach, and Fig. 1c, d show vertical cross sections at the QD position

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and the barrier gate centers, respectively. In the first approach, a chemical mechanical polishing process may be used to obtain SiO₂ layer planarization³³, easing the deposition of four overlapping gate layers—two for barrier gates (the first- and third-layer gates) and the other two for plunger gates (the second- and fourth-layer gates). Table 1 summarizes the layer indexes, gate names, and colors in Fig. 1b–d and the respective gate sizes. In this approach, we can reduce the number of overlapping gate layers. An overlay accuracy of 10 nm is assumed. (c), (d) Cross sections of the QDs (A–A’) and barrier gates (B–B’) in (b). The gate thickness increases in the upper layers to ensure gate continuity. In (d), the black and gray areas are both SiO₂, with the Si layer underneath etched in the latter. (e) Electrostatic potential in the Si QW at applied voltages of 0.6 V on plunger gates and 0.4 V (0.3 V) on the barrier gates between QDs (between a QD and a reservoir). (e) is drawn with COMSOL Multiphysics ver. 5.5 (https://www.comsol.com).

Table 1. Overlapping-layer gate characteristics.

| Layer index | Gate name | Gate color | Gate width (nm) | Gate height (nm) |
|-------------|-----------|------------|-----------------|-----------------|
| 1           | B₁₁–₁₂, B₂₁–₂₂,… | Blue       | 50              | 15              |
| 2           | P₁₁, P₂₁,… | Red        | 90              | 25              |
| 3           | B₁₁–₁₂, B₂₁–₂₂,… | Yellow     | 60              | 40              |
| 4           | P₂₂       | Magenta    | 70              | 60              |

Qubit operation in a two-dimensional QD array. In order to utilize this QD array as a quantum processor, it needs to be capable of spin readout, initialization, and manipulation. While this device does not have dedicated change sensor QDs, spin readout can be performed by the gate-based sensing techniques to detect the Pauli spin blockade (PSB) between neighboring QDs. The spin state can be initialized, for instance, by relaxation to the doubly occupied ground singlet state and rapid adiabatic passage. For spin manipulation, we
employ the electric-dipole spin resonance (EDSR) control based on micromagnets (MMs). The advantage of this scheme is that we can control the resonance frequency difference $\Delta f_r$ between neighboring QDs with the MM design. While spin manipulation can also be implemented with ESR striplines, the control of $\Delta f_r$ in this case relies on the difference of $g$-factors between QDs and it may be difficult to obtain controlled $\Delta f_r$ across a large QD array with device viabilities. In contrast, MMs can potentially control $f_R$, $f_{\text{Rabi}}$, and $\Delta f_r$ in a consistent manner across the qubit array by properly designing them, as we will show through simulations in the following.

Figure 2a shows the MM design for inducing the spatially inhomogeneous magnetic field ($B_{\text{MM}}$) in which the external magnetic field ($B_{\text{ext}}$) is applied in the direction of the arrow. The MM field $B_{\text{MM}}$ contains two essential components: a transverse field ($b_{\text{trans}}$) perpendicular to $B_{\text{ext}}$ and a longitudinal field ($B_{\text{long}}$) parallel to $B_{\text{ext}}$. $b_{\text{trans}}$ enables spin rotations combined with a QD displacement ($\Delta 1x$) by inducing an effective oscillating magnetic field. On the other hand, $B_{\text{long}}$ provides the qubit addressability by shifting the Zeeman energy at each QD. Moreover, this QD-dependent energy shift is essential for implementing two-qubit gates such as the controlled-not gate, controlled-phase gate, and resonant SWAP gate. For high fidelity single-qubit gates, $f_{\text{Rabi}}$ faster than 1 MHz is desirable.

Table 2 and Fig. 2b show the simulated transverse field slope ($b_{\text{trans}}$) at the QD positions. $b_{\text{trans}}$ at each QD position is calculated to be 0.56–1.2 mT/nm, comparable to the values in the previously demonstrated linear QD arrays. We estimate $f_{\text{Rabi}}$ to be 6.8–14 MHz assuming a conversion factor from $b_{\text{trans}}$ to $f_{\text{Rabi}}$ of 12 MHz mT, which is taken from previous experiment. We assume that the MW drive is applied to the barrier gate next to the QD (along $B_{\text{ext}}$) to maximize $f_{\text{Rabi}}$. In order to assess the qubit addressability, we calculate $B_{\text{long}}$ (Fig. 2c) and Table 3). The minimum $B_{\text{long}}$ difference ($\Delta B_{\text{long}}$) over the set of nine QDs is 6 mT (between Q23 and Q33) and it corresponds to $\Delta f_r$ of 160 MHz. This is much larger than our calculated $f_{\text{Rabi}}$ and therefore large enough to prevent the crosstalk of single-qubit gates. These results show this MM design can induce field gradients necessary for the qubit addressability even in a 3 × 3 QD array.

Figure 2. The schematics of MM design and simulation results. (a) MM design. The right panel illustrates the layout of the MM (yellow) along with the 3 × 3 QD array (center), designed so that the values of $\Delta f_r$ are robust against misalignment between the QD array and the MM. The magnet is 250 nm thick and 143 nm apart from the bottom of the magnet to the QD. Left panel shows an enlarged view of the region surrounded by the black dashed rectangle in the right. The magnet has a groove in the middle with its shape shown by the red dashed rectangle to make $\Delta f_r$ in each QD row moderate. $B_{\text{ext}}$ indicates the direction of the external magnetic field. (b), (c) Simulation results for $b_{\text{trans}}$ and $B_{\text{long}}$ in the Si QW. Magnetization of the MM is 1400 kA/m in the direction parallel to $B_{\text{ext}}$. (b), (c) are drawn with COMSOL Multiphysics.
Efficient quantum circuit execution in a two-dimensional QD array. One of the potential advantages of two-dimensional qubit arrays is the reduced circuit depth of quantum algorithm implementations thanks to better qubit connectivity\(^3\). Here, we discuss the efficiency of the four-qubit Grover’s search algorithm\(^3\) implemented in our two-dimensional QD array, see Fig. 3. This algorithm allows one to search for \(\left| q_3 q_2 q_1 q_0 \right\rangle = \left| 1101 \right\rangle\) using the superposition of four qubits with the same probability (we define \(\left| 0 \right\rangle\) by the spin
down state). The four-qubit Toffoli gates play a central role in implementing this circuit and can be synthesized from 15 two-qubit gates including 2 SW AP gates for compensating the lack of direct qubit couplings (Fig. 3b) (see Methods for the details). The spin state of qubit \( q_X \) is read out by PSB with a measurement ancilla qubit \( M_{qX} \). For comparison, we consider a linear array of four QDs which are lined up together with adjacent QDs for spin readout as shown in Fig. 3c. In this qubit layout, 18 two-qubit gates including 5 SW AP gates are necessary to implement a four-qubit Toffoli gate. This shows that the two-dimensional QD array enables efficient quantum circuit execution due to improved qubit connectivity.

**A larger scale two-dimensional array.** The scalability of the EDSR control based on MMs has often been questioned because of its difficulty in inducing strong field gradients over large areas. We have nevertheless shown that it is possible to induce field gradients in a small two-dimensional QD array. In the following, we propose a longer-term design approach that allows us to apply \( B_{\text{long}} \) while ensuring sufficient \( b_{\text{trans}} \) for each QD in a large two-dimensional array. The simple idea behind this approach is to decouple the magnet inducing \( b_{\text{trans}} \) from the one inducing \( B_{\text{long}} \). Under the device design shown in Fig. 4a, \( b_{\text{trans}} \) is induced by the plunger and barrier gate electrodes made of Co instead of Al, whereas \( B_{\text{long}} \) is induced by a large Co magnet located outside of the QD array. This structure may be amenable to a larger qubit array with fast, MM-mediated electrical spin control at the expense of introducing vias to enhance QD density and connectivity as compared to the 3 × 3 QD array.

Under this novel magnet structure, it would be possible to integrate about \( 40 \times 40 = 1600 \) QDs within a \( 5 \times 5 \text{μm}^2 \) area because each QD occupies only \( 120 \times 120 \text{nm}^2 \). Assuming that PSB is used for spin state initialization as discussed above, we can consider an example of implementing qubits and ancillas in this QD array as shown in Fig. 4b. In this example, the 3 × 3 QD array consisting of 4 data qubits (red) and 4 ancillas functions as a unit cell. QDs with a cross are not used, so they can be empty, in which case coherent inter-site qubit transport may be used to maintain high qubit connectivity. Alternatively, in the case of single occupancy, two-qubit exchange gates would be needed for connection. As can be seen from this example, such a device would be able to host more than a thousand of qubits, a number of qubits much larger than those in any other
existing quantum processors\textsuperscript{11-15}, in a way compatible with high qubit connectivity and the spin operation scheme discussed above.

Figures 4c, d show simulated values of $B_{\text{long}}$ slope in the x and y directions induced by a large Co magnet located outside the QD array (yellow square). In the QD array, the $\Delta f_{\text{Rabi}}$ values between the nearest-neighbor QDs are larger than 100 MHz (corresponding to $\approx 0.03 \text{ mT/nm}$), which are sufficient for unconditional single-qubit operations and two-qubit gate manipulations. Figure 4e shows simulated values of $f_{\text{Rabi}}$ induced by the Co gates. Although the formation of QDs in such a gate structure may not have been demonstrated, the electromagnetic field of each QD can be controlled independently by the plunger gate and the interaction between neighboring QDs can be adjusted by the barrier gate, ensuring precise manipulation of qubits. This electrical controllability, in conjunction with local magnetic fields, may also be used to compensate for qubit frequency shifts that can potentially be induced by the strain electric and the stray magnetic fields. Here, we use a 5 × 5 QD array for simulation simplicity and assume the gate sizes of Co plunger and barrier gates are 60 nm × 60 nm and 60 nm × 40 nm, respectively. The estimated average value of $f_{\text{Rabi}}$ for the 25 QDs is 39 MHz (assuming the same conversion factor used in the previous discussion), which is about three times faster than that in the 3 × 3 array discussed above owing to the close proximity of the magnet and QDs. The value of $B_{\text{trans}}$ induced by the Co gates is more than ten times larger than the transverse component of the field induced by the large Co magnet, so that we can safely approximate it to be due to the Co gates. By applying the proposed magnet fabrication approach, quantum processors with large numbers of qubits may be achieved with high-speed qubit manipulation, leveraging mature fabrication and integration techniques in Si. We anticipate that even larger arrays will be possible by further improving the magnet design.

**Discussion**

In this study, we discuss the feasible device designs of a two-dimensional Si QD array for multi-qubit quantum processing with qubit addressability. We reveal the possibility to provide qubit addressability in the two-dimensional array of 3 × 3 QDs, which can execute quantum circuits more efficiently compared with the one-dimensional array. We note that this method is essentially based on experimentally realized MM and QD structures with device viabilities. We have furthermore presented a possibility of hosting hundreds of qubits with $f_{\text{Rabi}}$ increased by roughly three times by employing a novel magnet-incorporated QD structure. We believe both methods will allow to scale up QD array sizes, to a level that was previously thought to be difficult with this scheme, while maintaining consistency with established fabrication techniques and qubit controllability in the presence of observed device variabilities. Our results have shown how to guarantee qubit addressability when electron spin qubits in Si are integrated to a larger scale. Quantum processors with large numbers of qubits, high-fidelity quantum logic gates, and long coherence times might accelerate research on quantum algorithms and architectures, enhancing the potential of quantum computing.

**Methods**

The method for mapping quantum circuits to QD arrays. We employed Qiskit’s LookaheaesSwap routing method\textsuperscript{40} for mapping quantum circuits via insertion of SWAP gates to construct quantum circuits for four-qubit Grover’s search algorithm. This method repeats the process of selecting the SWAP gate that maximizes the number of subsequent executable two-qubit gates when there is a two-qubit gate that cannot be executed in the current physical qubit layout. While Qiskit provides other methods to map circuits by inserting SWAP gates, we chose this method because it produces the circuit with smaller numbers of SWAP gates for both two-dimensional and one-dimensional QD arrays.

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Author contributions
M.T., T.N., T.K., and A.N. contributed to the device design. M.T. and K.T. performed simulations. M.T.

Competing interests
The authors declare no competing interests.

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