Thermally stable In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As pHEMTs using thermally evaporated palladium gate metallization

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Abstract
This work described the fabrication and performances of strained channel In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As/InP pHEMTs with thermally evaporated Pd/Ti/Au gate metallization. The electrical characteristics of these Pd-gate devices are studied to investigate the effects of changing the Pd metal thickness, annealing temperature and annealing time. Following annealing at 200 °C for 35 min, a 10 nm Pd-gate device displays a $V_{TH}$ of −0.25 V, which is significantly smaller compared to those with Ti/Au gate schemes showing $V_{TH} = −0.75$ V. A 1 μm gate length device exhibits an improved $G_m$ of 580 mS mm$^{-1}$ (from 500 mS mm$^{-1}$), a high $I_{DS,max}$ of 400 mA mm$^{-1}$ (from 330 mA mm$^{-1}$) and good $f_T$ and $f_{max}$ of 24.5 and 49 GHz commensurate with the 1 μm gate length. All these enhancements are attributed to the controllable gate sinking of Pd. The device shows no significant degradation even after annealing at 230 °C for more than 5 h, which implies that the reliability of these Pd-gate structures is excellent.

Keywords: palladium (Pd) gate metallization, pseudomorphic high-electron mobility transistor (pHEMT), InAlAs/InGaAs, InP, heat treatment, thermal annealing, thermal stability

(Some figures may appear in colour only in the online journal)

1. Introduction

III–V compound semiconductors have long been recognized as prospective contenders for the ITRS post 22 nm node due to their intrinsic high electron mobility and high carrier densities [1, 2]. The enhanced dc and RF performance of III–V materials attracts great interest for various applications such as low noise amplifier, power amplifier and sub-millimetre wave circuits approaching THz operations in nanoscale devices. Researchers worldwide have attached considerable importance to the pseudomorphic high electron mobility transistor (pHEMT) which utilizes the high carrier mobility property of a two-dimensional electron gas (2DEG). The channel modulation efficiency of heterojunction devices are highly dependent on the quality of Schottky contact, which implies a strong impact on many critical device parameters, such as gate leakage current, transconductance and threshold voltage, etc.

Therefore, the optimization of gate structure will be key to improve the device performance and stability.

In the past, various approaches such as gate recess techniques with deep etching to reduce the effective gate–channel distance [3, 4] or the use of strained supply layer to increase the effective barrier height ($\Phi_B$) [5], have been investigated for promoting positive threshold voltage shift and improved transconductance. In addition, gate sinking technique with refractory metals such as palladium (Pd) or platinum (Pt), which have rather strong diffusion in III–V compounds, are often employed to reduce the effective gate–channel distance for the enhancing device performances. Extensive studies have been done by resorting to Pt buried gate structure on GaAs and InP substrates, respectively [6–10].

Meanwhile, Pd has become a better alternative to Pt for the following reasons. Firstly, Pd is a more process-friendly option compared with Pt because of its higher vapour pressure
The strained In$_{0.7}$Ga$_{0.3}$As channel was sandwiched by two InAlAs buffer layers. A double delta-doping scheme was employed to enhance the carrier confinement in the channel. In this work, strained channel In$_{0.7}$Ga$_{0.3}$As-In$_{0.52}$Al$_{0.48}$As pHEMTs were fabricated by implementing a Pd/Ti/Au gate metallization scheme with conventional thermal evaporation. By combining the Pd-gate diffusion effect and the benefit of highly strained In$_{0.7}$Ga$_{0.3}$As channel structure, the device performance has shown over 50% enhancement over those reported in [12, 13]. The interrelations between Pd metal thickness, heat treatment time and temperature are explored to evaluate the thermal stability of these Pd-gate devices.

### 2. Device structure and fabrication process

The device fabrication was done on an InP-based epitaxial structure grown using a RIBER V100H molecular beam epitaxy system, as shown in figure 1. The surface defects from the substrate were smoothed by the 450 nm lattice-matched InAlAs buffer layer. A double delta-doping scheme was employed to enhance the carrier confinement in the channel. The strained In$_{0.7}$Ga$_{0.3}$As channel was sandwiched by two In$_{0.52}$Al$_{0.48}$As spacer layers, which helps to avoid the Coulomb scattering between the 2DEG and the double delta-doping. A 15 nm wide band gap In$_{0.52}$Al$_{0.48}$As barrier layer was grown for the formation of the Schottky barrier and it was covered by an undoped 50 Å narrow band gap In$_{0.53}$Ga$_{0.47}$As cap layer to protect it from oxidation and also to lower the resulting barrier height for the formation of Ohmic contact. The sheet resistance is 155 $\Omega$\per\square and the corresponding carrier concentration and mobility are $2.4 \times 10^{12}$ cm$^{-2}$ and $13900$ cm$^2$ V s$^{-1}$ at room temperature. These figures are 30–100% better than similar GaAs and InP based structures reported in [12] and [13]. Breakdown voltages up to 14 V have also been reported on similar structures in our previous work [15].

The fabrication of double fingers, 1 $\mu$m gate pHEMT consists of mainly five steps. The MESA step is defined by using a phosphoric-based etchant followed by a selective sidewall etching to eliminate possible MESA sidewall leakage and thereby improve thermal stability during subsequent heat treatments [16]. Alloyed Ohmic contacts with AuGe/Au = 50/100 nm were formed by thermal evaporation followed by annealing in a forming gas environment for 90 s at 280 °C. Transmission line method measurement shows that the contact resistance ($R_C$) and sheet resistance ($R_{SH}$) are on average 0.16 $\Omega$ mm and 170 $\Omega$/\square, which are acceptable considering the thin gold layer in the Ohmic, contact scheme used. The gate recess is defined by a highly selective (InGaAs:InAlAs = 120:1) succinic etchant. Thermal evaporation with four different metallization schemes, including Ti/Au (50/450 nm), Pd/Ti/Au (5/50/450 nm), Pd/Ti/Au (10/50/450 nm) and Pd/Ti/Au (20/50/450 nm), were employed for the formation of the gate Schottky contacts. The process was completed with bonding pad formation by evaporating Ti/Au of thickness 50/450 nm. The high temperature silicon nitride (Si$_3$N$_4$) passivation step was skipped to prevent Pd diffusion prior to the heat treatment study. The samples were firstly annealed in a N$_2$-rich furnace for 5 min at 200 °C, followed by an additional 30 min of heat treatment to ensure Pd diffusion into the InAlAs supply layer.

### 3. Results and discussion

Room temperature dc and RF characterizations were carried on the 1 $\mu$m gate device with 100 $\mu$m gate width and 5 $\mu$m drain–source spacing by using a Cascade three fingers (G-S-G) prober, an HP 4142 dc parameter analyser and an Anritsu vector network analyser. The presented data were normalized with the device gate width. For simplicity, the device with the Ti/Au scheme will be referred to as Ti-gate device and 5 nm Pd-gate, 10 nm Pd-gate and 20 nm Pd-gate devices for those with Pd/Ti/Au metallization schemes.

#### 3.1. Effect of palladium metal thickness

The first part of the study was to identify a suitable palladium metal thickness for optimal device performance through heat treatment studies at fixed annealing temperature and time. Figure 2 depicts the Schottky diode characteristics for the Ti-gate and Pd-gate devices. The barrier height ($\Phi_B$) and ideality factor ($n$) were extracted from the forward bias region. The Ti-gate device showed $\Phi_B$ = 0.56 eV and $n = 1.59$ when compared to the 5 nm and 10 nm Pd-gate devices which have $\Phi_B$ = 0.58 eV and $\Phi_B$ = 0.59 eV and $n = 1.58$ and $n = 1.57$, respectively. The increased $\Phi_B$ and $n$ for the Pd-gate devices are attributed to the break-down of native oxides on the InAlAs surface during the heat treatment [11], therefore, leading to the reduction of off-state leakage.

However, as the Pd metal thickness increased to 20 nm, the device showed very poor Schottky behaviour with $\Phi_B$ = 0.24 eV and $n = 2.83$. The effective thickness of Pt after diffusion was reported to be up to ~1.4 times that of the deposited metal thickness [7]. As Pd and Pt have close physical
properties, it can be inferred that the effective diffusion thickness of 20 nm Pd could be up to 28 nm, which is larger than the entire thickness of the barrier and spacer layer. Hence, the tunnelling current increases rapidly with the excessive amount of Pd diffusion. This suggests that the thickness of Pd metal layer must be carefully controlled to prevent the degradation of Schottky contact due to excessive gate-sinking. For this reason, the discussion below will be focused on the 5 and 10 nm Pd-gate structures.

The change of threshold voltage ($V_{TH}$) and transconductance ($G_m$) at fixed drain voltage ($V_{DS}$ = 1.0 V) are illustrated in figure 3. By comparing the Ti-gate with 5 and 10 nm Pd-gate devices, $V_{TH}$ is shifted from $-0.75$ to $-0.35$ and $-0.22$ V and the peak $G_m$ is increased from 500 to 540 and 580 mS mm$^{-1}$, respectively. The Pd-gate devices demonstrate significant positive $V_{TH}$ shift and improved $G_m$ due to the reduction of effective gate–channel separation ($d$) through the Pd gate sinking, and these changes show a strong correlation with the Pd metal thickness.

The dc $I$–$V$ characteristics for the Ti-gate, 5 nm Pd-gate and 10 nm Pd-gate devices are depicted in figure 4. Considering the difference in their $V_{TH}$, the bias conditions were set from $V_{GS-START} = V_{TH}$ to $V_{GS-STOP} = V_{TH} + \Delta V$, where $\Delta V = +0.8$ V and step size = $+0.2$ V, for a fair comparison. With Pd-gate sinking, the peak drain–source current ($I_{DS}$) at $V_{DS} = 2$ V current is increased from 330 to 360 and 400 mA mm$^{-1}$, yielding 10 to 20% better current drivability on the Pd-gate devices. Moreover, the moderate kink-effect observed on the Ti-gate device is suppressed with Pd-gate metallization. The improvement is attributed to the enhanced Schottky barrier and the reduction of impact ionization with the formation of Pd compounds during the heat treatment process [11].

Microwave measurements were performed on the devices from 45 MHz to 40 GHz at $V_{DS}$ = 1.0 V and $V_{GS}$ biasing at peak $G_m$, as illustrated in figure 5. The cut-off frequencies ($f_T$) for the 5 and 10 nm Pd-gate devices are 22 and 24.5 GHz and their corresponding maximum frequency of oscillation ($f_{max}$) are 46 and 49 GHz, respectively. These figures are approximately 10 to 20% better than those of the Ti-gate device, which is a net result of the improved $G_m$ and also the decreased intrinsic gate capacitances ($C_{GS}$ and $C_{GD}$) [10].

3.2. Effect of annealing temperature and time

The device with 10 nm Pd metal is identified as the most attractive option between performance gain and gate leakage current. To probe further, a heat treatment study was performed on the 10 nm Pd-gate device at 200, 230 and 250 °C for 35 min. Figure 6 depicts the change of Schottky diode characteristics as a function of different annealing temperatures. The devices show similar characteristics in the forward and reverse bias regions with $\Phi_B = 0.58$ eV and 0.58 eV and $n = 1.58$ and
Figure 6. Change of Schottky diode characteristic as a function of annealing temperature for 10 nm Pd-gate device (annealing time = 35 min).

Figure 7. Change of barrier height and ideality factor as a function of annealing time in log scale for 10 nm Pd-gate device at 200 and 230 °C (error bar indicated).

After 340 min heat treatment, the device shows a $V_{TH}$ shift of 0.2 and 0.25 V with Gm improvement of 14% and 23% at 200 and 230 °C. This suggests that the magnitude of $V_{TH}$ shift and increased Gm is proportional to the annealing temperatures, which enable tuning the device parameters by changing the heat treatment conditions. The change of $f_T$ and $f_{max}$ in response to the annealing time at 200 and 230 °C are depicted in figure 9. The saturation of these parameters is also observed after 35 min annealing. After the full heat treatment, $f_T$ and $f_{max}$ are 24.6 and 50 GHz for 200 °C and are 25 and 48.5 GHz for 230 °C. It turns out that the annealing temperature makes no contribution to the absolute value or to the degree of improvement of $f_T$ and $f_{max}$. The stable dc and RF performances with Pd-gate structure provides a good guarantee for long term device reliability.

4. Conclusion

In this study, a comprehensive analysis on strained In$_0.7$Ga$_0.3$As/In$_0.52$Al$_0.48$As/InP pHEMT using Pd buried gates is reported for the first time. Different parameters such as gate metallization (Ti/Au and Pd/Ti/Au), Pd-gate metal thicknesses (5, 10 and 20 nm), annealing temperatures (200, 230 and 250 oC), and annealing times (5 to 340 min) have been investigated to understand the characteristics of Pd-gate structure on InP-based pHEMT.
By implementing a Pd-gate scheme using a simple thermal evaporation, the device exhibits a thermally stable shift of threshold voltage and retains a high quality Schottky contact. These devices are very promising with respect to the enhancement of the dc and RF characteristics such as increased $G_m$ and $I_{DS}$, enhanced $f_T$ and $f_{max}$, and elimination of kink effect. The thermal stability of Pd-gate device is demonstrated from its stable dc and RF characteristics, which shows no observable change even after over 5 h annealing.

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