Memcomputing Numerical Inversion with Self-Organizing Logic Gates

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Abstract—We propose to use Digital Memcomputing Machines (DMMs), implemented with self-organizing logic gates (SOLGs), to solve the problem of numerical inversion. Starting from fixed-point scalar inversion we describe the generalization to solving linear systems and matrix inversion. This method, when realized in hardware, will output the result in only one computational step. As an example, we perform simulations of the scalar case using a 5-bit logic circuit made of SOLGs, and show that the circuit successfully performs the inversion. Our method can be extended efficiently to any level of precision, since we prove that producing \( n \) bit precision in the output requires extending the circuit by at most \( n \) bits. This type of numerical inversion can be implemented by DMM units in hardware, it is scalable, and thus of great benefit to any real-time computing application.

Index Terms—Numerical Linear Algebra, Memcomputing, Self-organizing systems, Emerging technologies

I. INTRODUCTION

In recent decades, a growing interest into novel approaches to computing has been brewing, leading to several suggestions such as quantum computing, liquid-state machines, neuromorphic computing, etc. [1] [2] [3]. Along these lines, a new computational paradigm has been recently introduced by two of us (FLT and MD), based on the mathematical concept of Universal Memcomputing Machines (UMMs) [4]. This novel approach utilizes memory to both store and process information (hence the name “memcomputing” [5]), and in so doing it has been shown to solve complex problems efficiently [6]. The fundamental difference with Turing-like machines as implemented with current architectures, i.e., von Neumann, is that the latter do not allow for an instruction fetch and an operation on data to occur at the same time, since these operations are performed at distinct physical locations that share the same bus. Memcomputing machines, on the other hand, can circumvent this problem by incorporating the program instructions not in some physically separate memory, but encoded within the physical topology of the machine.

UMMs can be defined and built as fully analog machines [6]. But these are plagued by requiring increasing precision depending on the problem size for measuring input/output values. Therefore, they suffer from noise issues and hence have limited scalability. Alternatively, a subset of UMMs can be defined as digital machines [7]. Digital Memcomputing Machines (DMMs) map integers into integers, and therefore, like our present digital machines are robust against noise and easily scalable. A practical realization of such machines has been suggested in Ref. [7], where a new set of logic gates, named self-organizing logic gates (SOLGs), has been introduced. Such logic gates, being non-local in time, can adapt to signals incoming from any terminal. Unlike the standard logic gates, the proposed SOLGs are non-sequential, namely they can satisfy their logic proposition irrespective of the directionality in which the signal originates from: input-output literals or output-input literals. When these gates are then assembled in a circuit with other SOLGs (and possibly other standard circuit elements) that represents – via its topology – a particular Boolean problem, they will collectively attempt to satisfy all logic gates at once (intrinsic parallelism). After a transient that rids of the “logical defects” in the circuit via an instantonic phase [8], and which scales at most polynomially with the input size, the system then converges to the solution of the represented Boolean problem [7].

In this paper, we suggest to apply these digital machines within their SOLG realization to numerical scalar inversion. We will also briefly mention how to generalize this approach to linear systems and matrix inversion. These problems scale polynomially with input size, so one would expect our present work to be of limited benefit. On the contrary, numerical scalar and matrix inversion, and solving linear systems are serious bottlenecks in a wide variety of science and engineering applications such as real-time computing, optimization, computer vision, communication, deep learning, and many others [9] [10] [11] [12] [13]. An efficient hardware implementation of such numerical operations would then be of great value in the solution of these tasks.

The rules for basic numerical manipulations for engineering and scientific applications are given by the IEEE 754 floating point standard [14]. In modern day processors, alongside the arithmetic logic units which operate on integers, there exist floating-point units (FPUs) that operate on floating point numbers with some given precision [15]. Whilst addition and multiplication operations are quite optimized in hardware, floating-point division, which typically employs a Newton-Raphson iteration [16], performs three to four times slower in latency and throughput [1]. In the case of matrices, inversion is typically performed in software (LAPACK, BLAS). Most algorithms must continuously communicate between the CPU and memory, eventually running into the von Neumann bottleneck. This is a prime concern for software matrix inversion. In fact, methods to minimize communication with memory to solve linear systems is an active area of research. [17] In recent years, real-time matrix inversion has been implemented in hardware by FPGAs for wireless coding. [18] Even a quantum

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1Latency - Number of clock cycles it takes to complete the instruction. Throughput - Number of clock cycles required for issue ports to be ready to receive the same instruction again.
algorithm to speed up the solution of linear systems has been proposed [19]. However, these hardware solutions are typically constrained to very small systems or cryogenic temperatures, respectively.

In this paper, we avoid many of these issues by introducing a fundamentally different approach to scalar (and matrix) inversion. We propose solving the inversions in hardware by employing DMMs implemented with self-organizable logic circuits (SOLCs), namely circuits made of a collection of SOLGs. In this way, the need for a complicated approach to inversion is greatly simplified since the ‘algorithm’ implemented is essentially a Boolean problem, and the computational time is effectively reduced to real time when done in hardware. Our novel, and non-trivial contribution here is extending the factorization solution in [7] to a circuit which inverts fixed point scalars. We demonstrate that this can be done efficiently at any desired precision by proving that requiring \( n \) bits of precision in the result demands extending the factorization circuit by at most \( n \) more bits. To the authors’ knowledge, this is the first explicit construction of a fixed point inversion, with an arbitrary specified precision, into an exact factorization between integers. We also provide a roadmap from our scalar inversion method toward full matrix inversion and the solution of linear systems, the full implementation of which is left for future work.

This paper is organized as follows: In Sec. 2 we briefly outline the concept of DMMs and SOLCs. In Sec. 3 we describe in detail how the scalar inversion problem can be solved so that the reader can follow all its conceptual and practical steps without being bogged down by details. In this section we also simulate the resulting circuit for several cases, and discuss the scalability of our approach. In Sec. 4 we describe how matrix inversion can be done by repeated application of our solution for scalars. Finally, in Sec. 5 we report our conclusions.

II. DIGITAL MEMCOMPUTING MACHINES AND SELF-ORGANIZING LOGIC CIRCUITS

The method we employ for numerical inversion is an extension of the factorization solution done by Traversa and Di Ventra in Ref. [7]. We build on their method to perform scalar inversion, and by generalization, find the inverse of a matrix.

The SOLCs we utilize here are a practical realization of DMMs, which themselves are a subclass of UMMs, and thus take advantage of information overhead, namely the information embedded in the topology of the network rather than in any memory unit, and the intrinsic parallelism of these machines, which refers to the fact that the transition function of the machine acts simultaneously on the collective state of the system [4]. Digital memcomputing machines can be formally defined in much the same way as Turing machines, as the following eight-tuple: [7]

\[
\text{DMM} = (\mathbb{Z}_2, \Delta, \mathcal{P}, S, \Sigma, p_0, s_0, F).
\]

Here \( \Delta \) is a set of transition functions,

\[
\delta_\alpha : (\mathbb{Z}_2^{m_\alpha} \setminus F) \times \mathcal{P} \to (\mathbb{Z}_2^{m_\alpha} \setminus \mathcal{P}^2) \times S,
\]

where \( S \) is a set of indices \( \alpha \), \( \mathcal{P} \) is a set of arrays of pointers \( p_\alpha \), that select memprocessors called by \( \delta_\alpha \), \( \Sigma \) is a set of initial states, \( p_0 \) an initial array of pointers, \( s_0 \) the initial index, and \( F \), a set of final states.

From the above abstract definition we take two concrete points relevant to our discussion here. The first point is the fact that \( \delta_\alpha \), the transition functions, act on the collective states of the memprocessors, which gives rise to the intrinsic parallelism of the DMM. They also map finite sets of states to finite sets and hence describe a digital system. Secondly, we can explicitly see the novelty of DMMs, and how they differ from Turing machines. The way the DMM works is by first encoding a given problem into the topology of the network of memprocessors, which specifies the structure of the set \( \mathcal{P} \), which in turn facilitates a non-trivial communication between states by the transition functions. Thus, the DMM works by leveraging the structure of a given problem as reflected in the topology of the machine. This gives rise to the information overhead, and not in any additional software or instructions. This makes the DMM a special purpose machine designed to solve a specific problem in an efficient way. Compare this to a Turing machine, which is a more general computational paradigm but lacks the ability to specialize its processing to a given task, without some external instruction set.

All this is realized in practice by SOLCs [7]. In these circuits, the computation is performed by first constructing the “forward problem” with standard logic gates, namely the Boolean circuit that would solve such a problem, if the result were known. This specifies the topology of the DMM. To be more precise, if we let \( f : \mathbb{Z}_2^n \to \mathbb{Z}_2^n \) be a system of Boolean functions where \( \mathbb{Z}_2 = \{0, 1\} \), then we ask to find a solution \( y \in \mathbb{Z}_2^n \) of \( f(y) = b \). If numerical inversion is such a problem and we replace the gates of the Boolean functions with those that self-organize, the SOLC so constructed would find \( f^{-1}(b) \), its solution.

There is a fundamental difference between standard networks of logic gates and ones that self-organize, in that the latter ones allow for any combination of input/output satisfiable in the Boolean sense, i.e., non contradictory. One can, in principle, provide these logic circuits with combinations that are not satisfiable. In this case, the system will not settle to any fixed (equilibrium) point. For the formal analysis of these dynamical systems and convergence properties, we refer the reader to the details in Ref. [7], and Ref. [20] where it was demonstrated that chaotic behavior cannot emerge in DMMs with solutions. We stress that this is not the same as a “reversible logic gate” that requires the same number of input and output literals and an invertible transition function [21].

From a physical point of view, the entire network of gates acts as a continuous dynamical system and self-organizes into a global attractor, the existence of which was demonstrated in [7]. This network of logic gates exploits the spatial non-locality of Kirchhoff’s laws and the adaptability afforded by the time non-locality to find the solution of a given problem in one computational step if implemented in hardware. The fundamental point is that although the computation occurs in an analog (continuous) sense, SOLCs represent a scalable digital system since both the input and output are written and
read digitally, namely require a finite precision.

III. DETAILED ANALYSIS OF SCALAR INVERSION

In this section, we outline a detailed construction of a system of self-organizing logic gates which solves a scalar inversion problem consisting of fixed precision binary numbers. In terms of circuit topology, scalar inversion is almost bitwise the same as scalar multiplication, and thus our inversion circuit looks similar to the factorization circuit it is based on. However, in the inversion case a few more complications emerge. Namely, how does one map a general scalar inversion problem onto a logical circuit, and hence an exactly satisfiable problem?

This problem can be solved by constructing an “embedding” into a higher dimensional space where the arithmetic is between natural numbers, and hence exact. We do this by padding the problem with an extra register of satisfiability bits. Also, one must be especially careful with the interpretation of the input and output since the bitwise input into the circuit does not map transparently into the numerical values of input and output.

To clarify all this, let us consider the problem of inverting a scalar, say $a \times b = c$. We are given $a$ and $c$ with fixed-point exponents and $n$-bit mantissas where we normalize the leading bits of $a$ and $c$ to be 1, so we are guaranteed that there is always a solution. We forgo the discussion of the sign, as the sign bit of the product is simply an XOR between the sign bits of the constituents. The task before us is to perform an analysis of the forward problem, making sure that we translate the problem into a satisfiability (SAT) problem, since this is essentially what the SOLC solves.

In its most general form the problem is:

$$2^{m_a}(0.a_{n-2} \ldots a_0) \times 2^{m_b}(0.b_{n-1} \ldots b_0) = 2^{m_c}(0.c_{n-2} \ldots c_0),$$

where $a_i$, $b_i$ and $c_i$ in the above equation are either 0 or 1.

We immediately see that the following relationship between the exponents holds: $m_a + m_b = m_c$. By setting the unknown exponent value to be $m_b = m_c - m_a$, we are left with only the relationship between the mantissas.

What remains is a detailed analysis of the scalar inversion of the binary mantissas which we now consider independently of the exponent, essentially treating the arithmetic between natural numbers – where each mantissa can be reinterpreted explicitly as an integer. For example, the $n$ bits of $a$ would be reinterpreted now as,

$$a = a_{n-1}2^{n-1} + a_{n-2}2^{n-2} + \cdots + a_02^0$$

The same procedure would be performed with $b$ and $c$.

It is obvious that to satisfy the consistency of the arithmetic, the size of the mantissa of $c$ needs to be equal to the sum of the number of bits of $a$ and $b$. To that effect, we must add $n$ bits – which we refer to as consistency bits – to $c$ which we set to zero.

There now remain two issues. Since this is arithmetic between natural numbers, it must be exact, and under the current constraints it is not always the case (take $a = 3$ and $c = 1$, in digital representation, for example). To address this issue, we pad both $b$ and $c$ with what we call satisfiability or SAT bits, labeled $b_f$ and $c_f$ respectively, which are not specified and are allowed to float. This is to give the problem enough freedom to be exactly satisfiable in the Boolean sense (and hence solvable by a SOLC). Below we address the issue of how many such bits one needs to ensure exact satisfiability.

There is finally the issue of the accuracy of our answer $b$ in bits. In order to control precision, we pad $a$ with an $n_a$ number of zeros or enhanced precision bits, which we actually show do not change the solution.

We now show all these steps explicitly. In a more compact representation, and keeping in mind the above definitions, we write our original problem as

$$[a][0] \times [b][b_f] = [c][0] [c_f]$$

Here $a$, $b$ and $c$ represent the bits of the mantissas, $b_f$ and $c_f$ represent the floating bits, and $n_a$ and $n_b$ represent the size of the accuracy register and floating bit register, respectively. We are essentially constructing an “embedding” of the problem to one in a higher dimensional space where the arithmetic can indeed be satisfied exactly. The goal is to then ‘project’ back, or truncate, onto the original space to obtain $b$ with the desired accuracy.

The embedding is given by the following injective map where $\tilde{a}$ and $\tilde{c}$ represent the precision and consistency bits of zeroes,

$$\tilde{a} = a 2^{n_a} + \tilde{\hat{\alpha}}$$
\[ \hat{b} = b2^{n_b} + b_f \]
\[ \hat{c} = c2^{n_a+n_b} + \hat{c}2^{n_a+n_b} + c_f \]  
(6)

Since \( \hat{a} \) and \( \hat{c} \) are identically zero, the inversion we solve, \( \hat{a} \times \hat{b} = \hat{c} \) is written,
\[ a2^{n_a}(b2^{n_b} + b_f) = c2^{n_a+n_b} + n + c_f \]
\[ ab2^{n_a+n_b} + ab_f2^{n_a} = c2^{n_a+n_b} + c_f \]  
(7)

We know that the number of bits of the left in Eq. (7) must be equal to the number of bits on the right. The problem then becomes:
\[ \begin{array}{cccc}
| & | & | & 0 \\
| & | & 0 & 0 \\
n & n & n_b & n_a
\end{array} + \begin{array}{cccc}
| & | & | & 0 \\
| & | & 0 & 0 \\
n & n & n_b & n_a
\end{array} = \begin{array}{cccc}
| & | & | & 0 \\
| & | & 0 & 0 \\
n & n & n_b & n_a
\end{array} + \begin{array}{cccc}
| & | & | & 0 \\
| & | & 0 & 0 \\
n & n & n_b & n_a
\end{array} + \begin{array}{cccc}
| & | & | & 0 \\
| & | & 0 & 0 \\
n & n & n_b & n_a
\end{array}
\]  
(8)

The black boxes represent generic non-zero bits. Here, we can see that the last \( n_a \) bits of the 2nd term on the rhs of Eq. (8) are required to be zero. Therefore, additional accuracy padding on \( a \) gives us no more significant digits in our solution of \( \hat{b} \) and the problem reduces to:
\[ \begin{array}{cccc}
| & | & | & 0 \\
| & | & 0 & 0 \\
n & n & n_b & n_a
\end{array} + \begin{array}{cccc}
| & | & | & 0 \\
| & | & 0 & 0 \\
n & n & n_b & n_a
\end{array} = \begin{array}{cccc}
| & | & | & 0 \\
| & | & 0 & 0 \\
n & n & n_b & n_a
\end{array} + \begin{array}{cccc}
| & | & | & 0 \\
| & | & 0 & 0 \\
n & n & n_b & n_a
\end{array}
\]  
(9)

We are now ready to organize the main result of this section in the following theorem.

**Theorem 1.** Given a scalar inversion problem with a mantissa of size \( n \), the number of floating bits, \( n_b \), necessary to invert the input is at most \( n \).

**Proof.** Our original problem has now been cast as one between integers \( a \times \hat{b} = \hat{c} \), seen in Eq. (9). Assuming \( a \neq 0 \) (which, in our method, it is not by construction) by Euclidean division we are guaranteed that \( c2^{n_a+n} = aq + r \) where \( q, r \in \mathbb{Z} \) and \( 0 \leq r < |a| \).

\[
\frac{ab}{c} = \hat{c}
\]
\[
a(b2^{n_b} + b_f) = c2^{n_a+n} + c_f
\]
\[
a(b2^{n_b} + b_f) - c_f = aq + r
\]  
(10)

Since \( r < |a| \), and \( a \) has \( n \) bit length, one would need at most \( n_b = n \) bits to represent the floating bits, and our final output is provided by the first \( n \) bits of \( q \).

We conclude that to recover \( n \) bits of precision in the numerical inverse, one would need to extend the register of \( b \) (and for consistency, also \( c \)) by \( n \) bits. By doing so, the scalar inversion problem becomes a problem in exact bitwise arithmetic, and thus a circuit which can be exactly satisfied and solved by a SOLC.

**Numerical Simulations**- We constructed the solution of numerical inversion by extending the factorization solution found in [7]. The modified circuit contains the extended registers of satisfiability bits and freely floating nodes attached to voltage-controlled differential current generators representing them. We performed simulations on up to 5-bit examples with different initial conditions using the Falcon\textsuperscript{©} simulator\textsuperscript{2}. A simplified circuit of a 2-bit inversion is shown in figure [1] with the internal logic gates inside the 2-bit and 3-bit adders shown for clarity. In figure [2] we plot the simulated voltages across several cases of scalar inversion. The topmost simulation is of a 5-bit circuit inverting \( a = 10_{10} = 01010_2 \) as

\textsuperscript{2}Falcon\textsuperscript{©} simulator is an in-house circuit simulator developed by F. L. Traversa optimized to simulate self-organizing circuits. Some examples of other simulations can be found, e.g., in [7], [8], [22]-[24]. In all cases, the resulting \( n \) bits of the inverse always matched the corresponding \( n \) bits of the exact answer.
a function of time, which converges to the logical 1 (voltage \(V_{\text{gate}} = 1V\)) and logical zero (\(V_{\text{gate}} = -1V\)) once the inverted solution is found. The solution is \(b = 0.1_{10} = 0.00011001001100\ldots 2\). While expressible in base 10 as a finite decimal, in binary the expression does not terminate. However, our circuit finds the correct 5 truncated digits of the exact solution \(b \approx 0.00011_2\) in binary representation.

A few more examples are plotted for comparison. The simulation in the middle finds the inverse of \(a = 3\) in a 5-bit circuit. Finally the bottom-most simulation finds the inverse of \(a = 3\) in a 3-bit circuit.

**Scaling**—The multiplication operation on two \(n\) bit numbers involves \(n^2\) AND gates and \(n\) additions. In our case, if we fix the number of bits of the input and increase the precision \(p\) of the inverse, the number of logic gates will scale as \(O((n+p)^2)\). The resulting circuit scales quadratically in the number of input bits with fixed precision, and also quadratically in the precision, while fixing the number of bits of the input. Since the inversion is essentially an extended factorization, the equilibria will be reached exponentially fast and the total energy will scale polynomially in the amount of time to reach the equilibria as discussed in [7].

It is also worth noting that our inversion circuit performs the search of the equilibrium point collectively, by employing instantons [8]. This makes convergence times, if implemented in hardware, remain relatively independent from the system size since instantons are non-local objects that span the entire circuit irrespective of its size [8]. A demonstration of this point is shown in Fig. 3 where we plot the machine time (namely the number of steps required to find the solution) versus the number of bits for a given inversion problem. We say the problem has converged when the maximum distance between all the voltages at the logic gates and true logical voltages (-1 and 1) is less than \(\epsilon = 0.01\). More precisely, the simulation has reached the convergence time, \(t_c\), as soon as the following inequality is satisfied:

\[
C(t_c) = \max_i \left\{ \min_{\nu_{\text{logical}} \in \{1,-1\}} |v_i(t_c) - \nu_{\text{logical}}| \right\} \leq \epsilon \quad (11)
\]

Here \(v_i(t)\) represents the voltage at the \(i\)-th logic gate terminal in the circuit as a function of time. Taken first is the minimum over the logical voltages 1 and -1 which represent the Boolean 1 and 0 respectively. For clarity, we plot the function \(C(t)\) in Fig. 4 together with the corresponding simulation. These numerical results give further evidence for the efficiency and scalability of the approach to numerical inversion we have developed here.

**IV. EXTENSION TO MATRIX INVERSION AND LINEAR SYSTEMS**

Once we have discussed explicitly the case of scalar inversion, it is now a simple (although cumbersome) exercise to extend it to the matrix inversion case. However, the explicit procedure for a general matrix inversion would require too many details to fit in this paper and we will report it in a subsequent publication. We then just provide the explicit procedure given a \(2 \times 2\) non-singular matrix \(A\).

Consider then the following matrix equation \(AX = I\), where the matrix \(A\) is given with \(n\) bit binary entries, \(X\) is the solution we seek, and \(I\) is the identity matrix,

\[
\begin{bmatrix}
  a_{11} & a_{12} \\
  a_{21} & a_{22}
\end{bmatrix}
\begin{bmatrix}
  x_{11} & x_{12} \\
  x_{21} & x_{22}
\end{bmatrix}
=
\begin{bmatrix}
  1 & 0 \\
  0 & 1
\end{bmatrix}.
\]

This is equivalent to solving the following two linear systems of the form \(Ax = b\), one system for each column of the resulting inverse matrix.

\[
\begin{bmatrix}
  a_{11} & a_{12} \\
  a_{21} & a_{22}
\end{bmatrix}
\begin{bmatrix}
  x_{11} \\
  x_{21}
\end{bmatrix}
=
\begin{bmatrix}
  1 \\
  0
\end{bmatrix},
\]

\[
\begin{bmatrix}
  a_{11} & a_{12} \\
  a_{21} & a_{22}
\end{bmatrix}
\begin{bmatrix}
  x_{12} \\
  x_{22}
\end{bmatrix}
=
\begin{bmatrix}
  0 \\
  1
\end{bmatrix}.
\]

The systems above are independent and can be solved in parallel. This gives us the following coupled equations that we must solve simultaneously with a SOLC:

\[
a_{11}x_1 + a_{12}x_2 = b_1
\]
\[
a_{21}x_1 + a_{22}x_2 = b_2.
\]

![Fig. 4. The function C(t) [see Eq. (11)] and the related SOLC simulation for the case of 4-bit inversion of a = 2.](image-url)
There are 6 total arithmetical operations to be performed: 4 products and 2 sums. We approach the general inversion problem by constructing the relevant bit-wise logic circuit modules that will perform the fixed precision multiplication and addition. We perform all of the products in the manner we discussed above. The results of these four products are then summed (with signs) and set equal to $b_1$ and $b_2$ respectively.

The signed binary addition can be performed using the 2’s complement method [25]. First, an XOR is applied to every non-sign bit of the products ($a_{11}x_1$, $a_{12}x_2$, etc.) with the sign bit ($\text{sign}(a_{11}x_1)$ ..). The sign bit is then added to the result of the XOR. This makes it such that if the product was negative, it takes the 2’s complement (which is flipping every non-sign bit and adding 1 to the result) or if the product is positive, then the result is not modified. These 2’s complement additions are applied to the outputs of all four products which occur in our $2 \times 2$ system. After which the resulting two additions are set equal to the 2’s complements of $b_1$ and $b_2$. This completes the SOLC for the linear system. The full inverse is found by applying this circuit to all columns of the given matrix.

V. Conclusion

We have demonstrated the power, and more importantly, the realizability, of self-organizing logic gates applied to scalar/matrix inversion and the solution of linear systems. The extensions and applications of this work are plentiful and far reaching. The method developed in the paper has direct applications and benefit to many fields (machine learning, statistics, signal processing, computer vision, engineering, optimization) that employ high-performance methods to solve linear systems. While the current work is immediately applicable to many problems, the concept can be extended to support IEEE floating point specification in the input and output for scientific computation.

The authors envision the effectiveness of these machines to be realized in specialized hardware that is designed to interface with current computers. These DMMs built in hardware will be capable of solving efficiently many numerical problems, scalar and matrix inversion being a small subset of potential applications which include matrix decompositions, eigenvalue problems, optimization problems, training models in machine learning, etc.

In analogy with how specialized GPUs interface with the standard CPUs of present computers to solve specific parallel problems much more efficiently than a CPU, a dedicated DMM can be constructed to work in tandem with current computers where the CPU/GPU would outsource computationally intensive problems which the DMM can solve rapidly. We thus hope our work will motivate experimental studies in this direction.

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