Laser Processing For 3D Junctionless Transistor Fabrication

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Abstract—To take fully advantage of Junctionless transistor (JLT) low-cost and low-temperature features we investigate a 475°C process to create onto a wafer a thin poly-Si layer on insulator. We fabricated a 13nm doped (Phosphorous, 10^19 at/cm^3) poly-silicon film featuring excellent roughness values (R_{max}=1.6nm and RMS=0.2nm). Guidelines for grain size optimization using nanosecond (ns) laser annealing are given.

Keywords 3D monolithic integration; Junction-less transistor; poly-si; nanosecond laser;

I. INTRODUCTION

3D-monolithic integration, also named 3D sequential integration, consists in stacking active layers on top of each other in a sequential manner onto a given wafer substrate (Fig. 1). Direct wafer bonding can be used to transfer the top silicon layer of a Silicon-On-Insulator (SOI) substrate onto a processed bottom wafer for the channel formation. This approach requires the use of an SOI wafer and is very challenging in terms of thermal budget to avoid bottom tier degradation. In fact, a maximal thermal budget of 500°C during 2 hours has been establish to preserve the integrity of the bottom tier [1-3].

Fig. 1: 3D monolithic stack overview with two interconnected tiers.

Thus, a good candidate for top tier devices is the junctionless transistor (JLT), for which the uniform device doping avoids high-temperature Source-Drain (SD) formation [4]. Furthermore, the channel material can be directly deposited on a bottom tier without damages [5-6]. However, this integration scheme suffers from poly-silicon roughness obtained after processing. For instance, typical RMS values are 0.7nm [5]-1.2nm [6] (Green Nanosecond Laser Crystallization (GNS-LC) + Chemical Mechanical Polishing (CMP)) or 0.6nm [7] (HPA trimming).

To take benefits from JLT low cost feature, this work is focused on the following process: low-temperature amorphous silicon (a-Si) deposition followed by nanosecond laser annealing and CMP (Fig. 2). The specifications are the following: a maximum thermal budget of 500°C, 2hours, and a 12-15nm thick a-Si layer doped at 10^19 at/cm^3 for future JL device formation with a ≤0.5nm RMS variation to lower device variability.

II. PROCESS FLOW

A. 475°C Low Pressure Chemical Vapor Deposition

A 35 nm thick a-Si layer is deposited at 475°C on an oxidized blanket bulk wafer. Ex-situ doping (using ion implantation) and in-situ doping have been compared. For in-situ doping deposition, a 90sccm phosphorus flow is used in order to achieve a 10^19 at/cm^3 doping concentration [8]. For ex-situ doping, the implantation conditions have been simulated by Kinetic Monte-Carlo TCAD (Silvaco).

B. UV Nanosecond (ns) Laser Annealing (UV-NLA)

Thanks to low depth penetration, UV-NLA is suitable for crystallizing a top a-Si layer while preserving the integrity of the bottom tier [9]. For these reasons, an excimer laser (wavelength: 308nm, optimized pulse duration 160ns [10]) is used to activate the dopants and recrystallize the a-Si layer.

Fig. 2: Integration scheme. In-situ and ex-situ doping are compared.
Based on Time Resolved Reflectometry (TRR) analysis (energy density screening from 0.3 to 1.4 J/cm²), three regimes can be identified (Figs 3-6). In fact, in-situ reflectometry monitoring allows us to detect film melting (Reflectivity decreases).

For low energy density (<0.775 J/cm²), no melting is detected though TRR. An explosive melt followed by a spontaneous recrystallization can occur for such energy densities (see Fig.4). For intermediate energy densities (preferred processing window), a part of the a-Si film melts and recrystallizes, forming grains and lowering the film resistivity. For higher energy density (> 1.025 J/cm²), the layer is entirely melted before the end of the laser pulse resulting in an amorphous film.

Moreover, maintaining the stage temperature at 450°C reduces the thermal gradient undergone by the film. It could slow down the cooling, yielding larger grain and thus lower resistivity [11]. For instance, at the melt threshold, melting time is 156 ns (chuck at 450°C) compared to 130 ns at 25°C. In addition, a 2nd laser annealing (two pulses) can be used to preferentially melt the smaller grains. These coalesce with grains leading to an overall grain size increase [12].

As far as the comparison of in- and ex-situ doping is concerned (Figs 6-9), no significant difference can be observed in terms of energy response and grain size. To probe further, two energy density conditions are studied (0.625 J/cm² for I₁, E₁, and 0.675 J/cm² for I₂, E₂, as defined in Fig.7) with a stage temperature of 450°C using up to four cumulative pulses.
Patterns from grazing incidence X-ray diffraction in-plane and out-of-plane geometry (Fig. 8) correspond to poly-Si with no texture, indicating no preferential direction regrowth during annealing.

### C. Chemical mechanical polishing (CMP)

| Extracted from 5µm*5µm (AFM) | In-situ doped | Ex-situ doped |
|-------------------------------|--------------|--------------|
| Before CMP | | |
| $R_{\text{MAX}}$ (nm) | 50 | 63 | 49 | 71 |
| $R_q$ (nm) | 9 | 9.6 | 7 | 10 |
| After CMP | | |
| $R_{\text{MAX}}$ (nm) | 4 | 2.3 | 1.6 | 1.7 |
| $R_q$ (nm) | 0.25 | 0.29 | 0.2 | 0.2 |

Fig. 9: Roughness measured by Atomic Force Microscopy (AFM) on 5x5µm² scan before and after CMP.

To adjust the thickness and to lower the roughness, 25nm silicon is removed by CMP. For instance, for the $E_1$ condition, the peak-to-valley thickness variation ($R_{\text{MAX}}$) is reduced from 49 nm (before CMP) to 1.6 nm (after CMP) and RMS ($R_q$) from 7nm to 0.2 nm (Fig. 9).

Furthermore, Atomic Force Microscopy measurements (Fig. 10) evidence that grain size is unchanged after CMP, highlighting that the film morphology is homogeneous within the depth.

Finally, a 13 nm average thickness is achieved (Fig. 11), which is appropriate for 15nm gate length and width JL transistor (equivalent oxide thickness of =0.8nm and DIBL=70mV/V) (Fig. 12).

### III. Conclusion

We provide guidelines, to form thin doped poly-Si film on insulator suitable for JLT 3D monolithic low temperature and low cost integration (475°C). When considering processing time and thus cost, in-situ doping, 450°C stage temperature and low laser pulses number are preferred for optimized recrystallization.

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Fig. 10: AFM after CMP highlighting the poly-si grain size ($I_2$).

Fig. 11: Silicon thickness before/after CMP ($E_i$).

Fig. 12: TCAD simulated $I_D=V_G$ for a junctionless transistor featuring 13nm 10⁵ doped channel.