Understanding of Feedback Field-Effect Transistor and Its Applications

Changhoon Lee,Juho Sung and Changhwan Shin *

Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, Korea; cha2202@naver.com (C.L.); tjdwngnh@naver.com (J.S.)
* Correspondence: cshin@skku.edu; Tel.: +82-31-290-7694

Received: 3 April 2020; Accepted: 23 April 2020; Published: 28 April 2020

Abstract: Feedback field-effect transistors (FBFETs) are devices based on a positive feedback loop in which the electrons and holes in the channel region act on the energy states of the potential barrier and wall. Owing to the positive feedback phenomenon, FBFETs have an excellent subthreshold swing (~0 mV/decade at 300 K), a high on-/off current ratio (~10^10), and a clear saturation region. The power consumption of both the turn-on state and turn-off state is significantly low until operation commences. In addition, the hysteresis caused by the carriers accumulated in the potential wall allows the FBFET to act as a memory device. Moreover, the power consumption of neuromorphic devices can be suppressed by ~100 times with the use of FBFETs. In this work, we analyze the device structure and operating principle of the FBFET and summarize its applications.

Keywords: positive feedback; steep-switching device; feedback field-effect transistor; low power application; neuromorphic computing; integrate-and-fire

1. Introduction

Metal-oxide-semiconductor field-effect transistors (MOSFETs) have been scaled down over the last half-century to achieve high density, high performance, and high cost-effectiveness [1–3]. In spite of the advantages of scaling, some issues have arisen as the device sizes continue to shrink. For instance, the power consumption and operating temperature of the transistor have increased significantly [2,3]. In addition, the leakage current has increased to the extent that it may surpass the dynamic power consumption [2,3]. Various techniques have been introduced to reduce both the leakage current and power consumption, but those efforts have thus far been restricted by the theoretical limit of subthreshold swing (SS) (i.e., SS ~60 mV/decade at 300 K) of MOSFET [2]. In order to improve the subthreshold swing of the transistor, various novel steep-switching devices have been explored. The major novel devices are classified as follows: negative capacitance FET (NCFET) that exhibits steep slope by using the negative capacitance effect of ferroelectric layer [4–8], phase FET, which consolidates additional components to use the unique properties of phase transition material like abrupt and reversible resistivity switching with a conventional thermionic emission process through low-drive voltage [9,10], Nano-Electro-Mechanical (NEM) relay using the mechanical operation for causing connection and disconnection of the channel [11], impact ionization MOS (I-MOS) device controlled by impact ionization which is generated by a high electric field [12–14], and tunnel FET (TFET), utilizing the band-to-band tunneling (BTBT) operational mechanism [15–17].

Of these, field-effect transistors (FETs) using a positive feedback mechanism have attracted particular attention. Feedback FETs (FBFETs) show excellent subthreshold swing (~0 mV/decade at 300 K) and high on-/off current ratios (~10^10) [18,19]. For those reasons, many researchers have expressed interest in FBFETs and proposed various types of FBFETs, such as positive feedback devices (PF devices) [20–22], zero-impact ionization, zero subthreshold swing FETs (Z2-FETs) [23–29], and zero...
subthreshold swing, zero-impact ionization, and zero-gate FETs ($Z^3$-FETs) [30–32]. In this study, we will summarize the characteristics of FBFETs (i.e., operating mechanism, structure modeling, and transfer characteristics).

Compared to conventional FETs, the superior properties of FBFETs can be utilized in a circuit composed of invertors or especially for neuromorphic devices. One of these properties involves a saturation region that is clearly distinguished according to gate voltage ($V_g$). Especially at threshold voltage ($V_{th}$), the power supplied to a device in both the on-state and off-state can be very low, and the power consumption is low both during operation and in the off-state until operation.

FBFETs have demonstrated their potential as memory devices. A representative example is the capacitor-less dynamic random-access memory (DRAM). The 1T-DRAM was first proposed two decades ago [33], however, it still remains in the academic research stage. These devices exhibit fatal drawbacks such as low reliability, high power consumption, or lack of compatibility with standard process technologies such as meta-stable DRAM (MSDRAM) [34–36] and A2RAM [37,38]. Heretofore, the conventional 1-transistor 1-capacitor DRAM (1T-1C DRAM) succeeded in overcoming difficulties in the development process without serious problems. The 1T-DRAM has not yet demonstrated the ability to become commercially available to replace the DRAM [37–42]. However, the DRAM is facing huge challenges that are proving hard to overcome. The primary issue is that scaling the capacitor in the bit-cell of the DRAM can no longer keep up with the access transistor in the bit-cell [41,42].

A capacitor requires a minimum size to store a certain amount of charge and to ensure accurate memory cell operation. As various studies have been conducted on replacing the traditional DRAM with a new one, a DRAM using FBFETs has emerged as promising [43–48]. The positive feedback mechanism is based on the accumulation of electrons and holes in the potential wall, which leads to a collapse of the potential barriers, resulting in hysteresis. In general, hysteresis is considered as a side effect that is generally handled as being parasitic and unnecessary [49–51]. However, FBFETs could play the role of memory for a promising new 1T-DRAM with this feature.

A new static random-access memory (SRAM) utilizing FBFET unit cells has been proposed. For these SRAM unit cells, a special ability induced by the positive feedback operation allows for high-speed memory operation. Moreover, the big cell area, which has been noted as a limitation of the conventional SRAM, is solved by a simple device structure using FBFETs. The cell achieves a small area at $8\mu^2$, enabling high-density design, while the low switching current dramatically reduces the rapid switching characteristics, simultaneously enabling the performance of low-power memory [52–54].

The FBFET-based SRAM unit cell also demonstrates the excellent operating performance of the SRAM, including a write speed, fast read speed, and competent retention time because of its positive feedback mechanism [52–54]. These results demonstrate the great potential of FBFET for next-generation DRAM/SRAM memory applications.

FBFETs are also being studied for application to neuromorphic devices to solve the issue for energy efficiency [21,55,56]. Based on the mechanisms of biological neurons, artificial neural networks (ANNs) have been proposed as powerful tools for pattern recognition and classification [57,58]. Beyond ANNs, spiking neural networks (SNNs) have been proposed [59–62]. However, conventional neuronal circuits in SNNs require large areas as well as high power consumption [21]. PF devices with a split-gate floating body have been proposed as new neuron devices that demonstrate integration-and-fire capabilities [21,55,56]. A recent simulation study of those devices used a common magnetic controller in the neuron layer and demonstrated successful operation of a high-density multiple PF neuron system with reset and lateral suppression capabilities. The study proposed a method for SNNs to reduce power consumption by ~100 times with FBFET-based circuits [21].
2. Feedback Field-Effect Transistors (FBFETs)

2.1. FBFET Device Structure

FBFETs were first proposed in 2008 [63]. The design of the new FET is similar, with a P-I-N diode under forward bias. It exhibits positive feedback with double potential barriers. Surrounding the channel region close to the source and drain, gate-sidewall spacers fabricated to trap charges play the role of potential barriers on the FBFET (see Figure 1). Each barrier that blocks the flow of electrons and holes makes it possible to utilize P-I-N diodes as FBFETs. This can be understood and analyzed using energy band diagrams (see Figure 2). The whole steps for the mechanism above are described in detail in Section 2.2.

![Illustrated device structure of a P-I-N feedback field-effect transistor (FBFET) with trap-charged spacers, (c) its cross-sectional view along the channel direction, and (d) the corresponding energy band diagram for the FBFET [63].](image)

**Figure 1.** (a,b) Illustrated device structure of a P-I-N feedback field-effect transistor (FBFET) with trap-charged spacers, (c) its cross-sectional view along the channel direction, and (d) the corresponding energy band diagram for the FBFET [63].

![Energy band diagram and (b) current-voltage characteristics of P-I-N diode and FBFET. Note that the anode/cathode of the P-I-N diode is corresponding to the source/drain of the FBFET.](image)

**Figure 2.** (a) Energy band diagram and (b) current-voltage characteristics of P-I-N diode and FBFET. Note that the anode/cathode of the P-I-N diode is corresponding to the source/drain of the FBFET.

The FBFET can overcome the limits of conventional MOSFETs. The FBFET can have steep switching values (i.e., subthreshold swing ~2 mV/decade at room temperature) and a high on-/off current ratio (~10⁷) [63,64]. Based on the voltage applied to the gate, the FBFET can, of course, operate
as both an n-type and p-type transistor. However, the mechanism that depends on the trapped charge can cause issues. For example, as the device operates, the stimulus applied to the spacer creates instability. Furthermore, an additional process is needed to store the carrier on the spacer attached to the source and drain regions, which should be simplified.

Based on the FBFET structure, many studies have been conducted to improve the electrical properties of the FBFET [23–32,37–42]. The most common framework among them is to change the means of fabricating the two potential barriers implemented by the trapped charges of the gate-sidewall spacers. There are two approaches: (1) the first is to replace them with potential barriers created by the junctions of Si regions with different doping concentrations. Depending on the location of the gate, next to the source or drain, the type of operation is determined by the n- or p-type FET. Therefore, it can play the role of n- and p-type transistors simultaneously through the modification of device structure having double gates adjacent to the source and drain [63–65]. (2) The other approach is to form an additional gate next to the source (S) and drain (D) regions by using electrical energy as a potential barrier. This device structure can perform as an n- or p-type FET, depending on the voltage applied to the gate. However, it has the disadvantage that there is the energy consumption by the gate voltage for the barrier.

2.2. Positive Feedback Mechanism

Feedback indicates that all or part of the output returns back to the input. Positive feedback has the characteristic that the input condition increases after a single process, and the re-input condition is repeated for the second process. Regenerative cycles thus continue to be positively amplified.

FBFETs have two potential barriers, which are located in the channel region next to the source and drain, as in thyristors, and these prevent the flow of electrons and holes. As the potential barrier is formed, a potential wall is simultaneously formed on the opposite side, which has the lowest energy state for carriers. When a gate voltage is applied, positive feedback begins to operate through the lowered potential barrier. It is possible for carriers to flow from the source to the drain through the lowered potential barrier. Some electrons or holes are trapped in the potential wall in the channel region [63–65]. Charges induced by carriers trapped in the potential wall act on the energy band. Electrons increase the energy band in the adjacent region, meaning that the potential barrier on the opposite side of the potential wall is lowered. Holes have the opposite effect of electrons, causing the energy band to become higher. Trapped holes near the potential wall will cause barrier collapse. As the barriers have a lowered height, additional carrier flow occurs through the lowered barrier to operate the former process repeatedly. Once the operation has begun, the positive feedback loop can continue to operate without any additional voltage. As a result, higher currents can flow, as compared with the case in which only voltage was applied to the gate primarily to lower the potential barrier [63–65].

Figure 3 shows the loop for showing the positive feedback mechanism after the spacer is conditioned with trapped charges. The potential barrier height to block the electron flow induced by the trapped charge on the spacer is expressed as $V_{Be}$, with an initial state between the N$^+$ doping concentration region and the spacer region adjacent to the N$^+$ region without the gate and drain bias at equilibrium. If there is super-elevation on the gate bias ($V_{G0}$) and drain bias ($V_{D0}$) at equilibrium, the additional reduction of the electron (hole) injection barrier can be defined as $\phi_e$ ($\phi_h$). The height of the potential barrier blocking the electrons can be defined as $(V_{Be} - \phi_e)$ [65]. The drift current can be neglected owing to the dominance of the diffusion current in the ideal diode equation. $D_e$ and $D_h$ are the diffusivity of electrons or holes, and $L_n$ and $L_p$ are the diffusion length for electrons or holes, respectively. $n_p$ is the minority carrier concentration at the boundary $x = -x_p$, and $p_n$ is the minority carrier concentration at the boundary $x = x_n$. $k$ is Boltzmann’s constant. When $V_{G0}$ is applied to the gate and $V_{D0}$ is applied to the drain, the initial electron current can be written using the Shockley equation, as follows:

$$I_{e0} = qA(D_p p_n L_p^{-1} + D_n n_p L_n^{-1}) \left( e^{[qV/(kT)]} - 1 \right),$$

$$= I_{e1} \left( e^{[\phi_e/(kT)]} - 1 \right)$$

(1)
For the same bias, the hole barrier (at the drain side) induced by the initial hole current can be written as follows:

\[ I_{h0} = qA(D_pP_nL_p^{-1} + D_nP_lL_n^{-1}) (e^{[qY/(kT)]} - 1) \]
\[ = I_{h0} (e^{[\phi_e(kT)]} - 1) \]  
(2)

Step 1. If we set the condition of a small change in the gate voltage or drain voltage, a small perturbation, \( \Delta Y \), of the electron injection barrier will occur. The \( \Delta Y \) caused by an exterior change will allow more electrons to be injected into the intrinsic Si region from the N+ region. The resulting change in electron current (\( \Delta I_e \)) is presented as follows:

\[ \Delta I_e = I_0 (e^{[\Delta Y/(kT)]} - 1) \]
\[ I_e = I_{el} (e^{[\phi_e(kT)]} - 1) \]
\[ \Delta I_e = I_{el} (e^{[\phi_e(kT)]} - 1) (e^{[\Delta Y/(kT)]} - 1) \]  
(3)

Using the Taylor’s expansion on the \( e^{[\Delta Y/(kT)]} \) for the first two terms yields the following:

\[ e^{[\Delta Y/(kT)]} = 1 + [\Delta Y/(kT)] \]
\[ \Delta I_e = I_{el} (e^{[\phi_e(kT)]} - 1) [\Delta Y/(kT)] \]  
(4)

Assuming that no recombination occurs in the channel region, the electrons flowing from the N+ region will accumulate in the potential wall next to the P+ region. Some carriers will be stored in the wall, while others will cross the potential wall barrier and have sufficient kinetic energy to be injected into the drain and be recombined. Letting the charge stored in the potential wall be \( Q \), the electron carrier lifetime be \( \tau_e \), the barrier potential seen by the electrons in the potential wall be \( \phi_B \), and \( A \) be a parameter, the following can be obtained:

\[ \Delta I_e = \Delta Q - \tau_e^{-1} + \Delta I_e \ A e^{[-\phi_B/(kT)]} \]  
(5)

The charge, \( \Delta Q \), from the electrons stored in the potential wall can be given by:

\[ \Delta Q = \Delta I_e \ \tau_e (1 - A e^{[-\phi_B/(kT)]}) \]  
(6)

Step 2. \( V_{Bh} \) will be decreased and \( \phi_B \) will be increased by the \( \Delta Q \) affected by the stored electrons. More holes will be injected into the channel from the collapsing potential barrier. The changes in the hole barrier (\( \Delta Z \)) and hole current (\( \Delta I_h \)) are given as follows:

\[ \Delta Z = \Delta Q - C_p^{-1} \]  
(7)
\[ \Delta I_h = I_{hil} (e^{[\phi_h(kT)]} - 1) (e^{[\Delta Z/(kT)]} - 1) \]  
(8)
The capacitance under the P+ spacer is $C_p$. Again, using the Taylor’s expansion on $e^{[\Delta Z/(kT)]}$ and only including the first two terms yields the following:

$$\Delta I_h = I_{hi}(e^{[\phi B_e/(kT)]} - 1) [\Delta Z/(kT)]$$

Through the same processes and conditions as perturbation of energy band next to the drain, the hole current flows to the source side and is trapped in a potential wall near the N+ source, affecting the valance band ($E^v$) potential. Thus, $V_{Be}$ decreases by $\delta Y$.

$$\Delta Q_+ = \Delta I_h \tau_+ (1 - Be^{[-\phi B_e/(kT)]})$$

$$\delta Y = \Delta Q + C_n^{-1} \tag{11}$$

Let the charge stored in the potential wall be $\Delta Q$ near the N+ region, $C_n$ be the capacitance under the potential wall conditioning with trapped electrons region, the hole carrier lifetime be $\tau_+$, the barrier potential seen by the hole in the potential wall be $\phi_{Be}$, and $B$ be a parameter. The equation for gain can be described with these parameters:

$$\Delta Y = (kT \Delta I_e) (I_{ei} (e^{[\phi_e/(kT)]} - 1))^{-1}$$

$$\text{Gain} = \delta Y/\Delta Y = \Delta Q + (I_{ei} (e^{[\phi_e/(kT)]} - 1) (kT \Delta I_e C_n)^{-1}) \tau_+ \tau_+ I_{ei} (e^{[\phi_e/(kT)]} - 1) (1 - Be^{[-\phi B_e/(kT)]}) (C_n C_p (kT)^2)^{-1} \tag{13}$$

where,

$$I_{ei}^* = I_{ei} (e^{[\phi_e/(kT)]} - 1) (1 - Be^{[-\phi B_e/(kT)]})$$

$$I_{hi}^* = I_{hi} (e^{[\phi h/(kT)]} - 1) (1 - Be^{[-\phi B_e/(kT)]})$$

When the gain is $\geq 1$, FBFET will be operated with steep-switching by the positive feedback. As the positive feedback mechanism uses both electrons and holes, the type of transistor is determined by which of the two potential barriers blocks the flow of holes/electrons and applies a negative/positive voltage to initiate a feedback operation (see Figure 4) [63–65].

![Figure 4](image-url)
2.3. PF and Band-Modulation Devices (FED, Z2-FET, Z3-FET)

Depending on the specific mechanisms and the device structures, FBFETs have various names, such as PF devices [21,22], band-modulation devices (BM devices) [66,67], Z2-FET devices [23–29], and Z3-FET devices (see Figure 5) [30–32]. The positive feedback first proposed in FBFETs is their key operation principle. Based on the positive feedback mechanism, two potential barriers are created in three ways: the first one is through a trapped charge of the spacer or insulator layer (see Figure 1) [23,63,64,68,69], the second one is by creating a virtual doping concentration through the gate voltage in the channel region next to the source/drain (see Figure 5) [30–32,70–73], and the third one is through the junction of Si regions with different doping concentrations (see Figure 5) [74,75]. The mechanism used in the first and second is called band modulation, and devices with positive feedback and band modulation can be classified separately (see the list in Table 1).

![Figure 5](image-url) Structure and energy band diagram for band-modulation devices: (a) FED (field effect diode), (b) Z2-FET (zero-impact ionization and zero subthreshold swing FET), and (c) Z3-FET (zero subthreshold swing, zero-impact ionization, and zero gate FET) with bias for virtual potential barriers [19].

![Figure 6](image-url) Structure and energy band diagram for the dual gate FBFET with PN junction barriers [75].
First, all devices including FBFETs that rely on positive feedback can be considered as PF devices. Secondly, these devices can be identified as band-modulation devices if they depend on the band modulation mechanism for barrier formation. Band-modulation devices include field-effect diodes (FEDs) [77–79], Z²-FETs, and Z³-FETs, as already shown in Figure 5. The Z³-FET device appears similar to forward-biased P-I-N diodes with undoped ultra-thin silicon films. The device configuration can be seen as a reverse FED. This new device is configurable by applying the standard design rules for fully depleted silicon-on-insulator (FDSOI) technologies [30–32]. The ground plane under the thin buried oxide (BOX) allows the threshold voltage of the complementary metal-oxide-semiconductor (CMOS) circuit to be adjusted. As the top gate stack is replaced with a buried ground plane, a reliability issue arises concerning whether it can withstand much higher breakdown voltage through a sufficiently thick BOX rather than the previous thin gate insulator layer. An important feature of Z³-FETs that benefit from using a gate oxide as a BOX is that a high back gate bias can be maintained. Compared with Z²-FETs, Z³-FETs have no high-voltage metal gate stack, and thus there is no problem with high-voltage stability [30,31]. Z³-FETs with these features show their potential as sensors with internal memory for various applications.

3. Characteristics of FBFET

The theoretical limit of SS is defined as 60 mV/decade at 300 K [2]. However, surpassing the theoretical limit of SS can be achieved with novel device structures and/or new materials. Various steep-switching devices have been explored to overcome this limit [4–18]. Among them, devices relying on the positive feedback mechanism have been proposed and demonstrated with extraordinary abilities [21–32]. FBFETs show excellent subthreshold swing (~0 mV/decade at 300 K) and high on-/off current ratios (~10¹⁰) [18,19].

When the temperature or the $V_{DS}$ value increases, the on-/off current ratio increases. As the depth of the channel decreases, the device exhibits features that have characteristics more suitable for...
FDOSI structures. As the dielectric constant of the insulator layer increases, threshold voltage ($V_{TH}$) increases, while $V_{TH}$ decreases with increasing the work function of gate material. Depending on the gate voltage, there is a limit to the channel length, and, depending on the gate length, there is a limit on $V_{TH}$. N-/p-type FBETs are formed based on the gate location adjacent to the source/drain [75]. As the channel length increases over 500 nm, $V_{on}$ increases, $I_{on}$ decreases, and abrupt switching decreases due to the fast regeneration of minority carriers. In addition, hysteresis disappears as the channel length increases [80].

Various simulation studies have found that, the shorter the region of the FBFET channel is, the better the performance is. Shortening the channel length improves the switching characteristics, and the outstanding characteristics of the FBFET are represented with the benefits from scaling a device, unlike the existing MOSFETs [75]. In contrast, as the channel length increases, low SS values and on/off-current without saturation can be obtained. For channel lengths longer than 100 nm, FBETs do not exhibit ideal switching characteristics. Nevertheless, all of the SS values were less than 60 mV/decade at 300 K.

However, recent studies have shown that the positive feedback mechanism does not work, in contrast to the improved characteristics that have been achieved on the ~10 nm scale. The cause lies in the role of the potential barriers, which are key in the operation of FBFET. As the channel length increases, the potential barrier becomes wider. The energy and time required to collapse the potential barrier increase when the channel length is longer than 40 nm. At smaller scales, however, the potential barrier becomes too narrow, resulting in short channel effects (SCE), which are expected to block the carrier flow. To solve this limitation, it is necessary to consider ways to overcome the SCE, as in conventional MOSFETs [75].

When the channel length decreases, the threshold voltage decreases and the on/off current ratio increases. However, there are limitations on $V_{DS}$ depending on the channel length. If the channel length is 40 nm, the $V_{DS}$ value will not be able to cut off the current at 1.1 V. When $V_{DS}$ is 1 V, the channel length of 30 nm cannot cut off the current. As a result, there is a limit on the possible shrinking in FBFET, as shown in Figure 7 [75]. In addition, as the drain current increases, a problem arises in that the value of the potential voltage preventing carrier flow in the drain becomes low [63–65,75].

![Figure 7. $I_D$-$V_G$ curve for 30–50 nm channel lengths when 1 V is applied to the drain (left), and for a 0.9–1.1 V drain bias with an $L_{CH}$ of 40 nm (right) [75].](image)

4. Applications of FBFET

4.1. Logic Device Applications (FBFET-Based Inverter)

An inverter design that functions properly requires efficient operation of the pullup and pulldown devices. As the device must be operated under a forward bias, the magnitude of $V_{DS}$ should be higher than the built-in potential of FBFET [81]. This can be optimized through various combinations of bias, which requires a significant amount of effort. Nevertheless, the advantages of an inverter with a
combined FBFET are as follows: FBFETs have a steep-switching feature and high current on/off-current ratio; moreover, the saturation region is clear, especially beyond $V_{\text{TH}}$. In other words, the amount of current supplied to the operating and non-operating regions can be distinguished by the gate voltage ($V_g$), and thus the power consumption during operation and in the off-state can become minimal. The steep-switching characteristic of the FBFET is utilized in digital integrated circuits. A typical example is that the switching is controlled by an FBFET in the inverter. In a conventional inverter circuit, as the input voltage continues to increase, the charge stored in the capacitor of the circuit tends to run low over a long period of time [81,82]. However, if the FBFET plays the role of controlling the input voltage supply for the operation of the inverter, the voltage stored in the capacitor changes rapidly at $V_{\text{TH}}$ of the FBFET. In addition, starting from $V_{\text{TH}}$, the voltage supply appears as a saturation region, showing stable on/off-states. The FBFET-based inverter is shown in Figure 8.

![Figure 8. Illustration of an FBFET-based inverter circuit.](image)

### 4.2. Memory Cells

The traditional 1T-1C DRAM has allowed the reduction of device sizes to improve the performance and density of cells. The conventional 6-transistor static random-access memory (6T-SRAM) exhibits high performance with low density [83–89], while DRAM exhibits relatively low performance but provides high density [90]. FBFETs can be used for next-generation DRAM and SRAM to overcome the technical limits of each. A large amount of research has been carried out to demonstrate the competitive characteristics in the field of DRAM, and the capacitor-less DRAM (1T-DRAM), which was first proposed twenty years ago, has received much attention [33]. 1T-DRAM utilizes side effects such as hysteresis, which some studies consider harmful and have tried to remove. When the parasitic carriers that generally cause hysteresis are stored in the body and increase the potential, the threshold voltage is lowered and high current can be achieved—this is defined as the ‘1’ state. The ‘0’ state features a lower current achieved by removing the carriers from the body [34–36,43–48,88].

The 1T-DRAM has remained stalled in its current state as a potential next-generation candidate. While the 1T-DRAM has great structural advantages, it is necessary to demonstrate its ability to be fully commercialized in order for it to replace the conventional DRAM. Unfortunately, fatal drawbacks such as low reliability, high power consumption, or incompatibility with standard process technologies have emerged for various proposed models [37–42]. Most importantly, the traditional DRAM continues to succeed in the development process without serious problems. At present, the conventional 1T-1C DRAM memory cell is reaching its scaling limit. One of its biggest problems is that scaling the cell capacitor can no longer keep up with the transistor [41,42]. To ensure correct memory cell operation, a minimum space is required to store a certain amount of charge. The conventional methods...
for improving performance through scaling are thus now stagnating in the 1T-1C DRAM device architecture. In addition to devising various technologies to overcome these difficulties, it seems reasonable to consider a new DRAM structure. One promising candidate is memory cell types that store charges in the body of the transistor, thus modulating the threshold voltage and exhibiting distinct drain currents without the capacitor facing scale limitations. The body of the memory cell is then fully depleted of the accumulated carriers to obtain two distinct current levels corresponding to the complementary logic states. There are some device structures, such as MSDRAM [34] and A2RAM [37,38], that can meet most of the DRAM requirements: the ability to work under low voltage, low power consumption, long retention times, and scalability. Among 1T-DRAM cell candidates, the devices containing FBFETs exhibit excellent possibilities with a steep subthreshold swing owing to their positive feedback mechanism. These devices stand out for their performance and feasible integration with the standard fabrication process for ultra-thin body structures (see Figure 9).

![Figure 9. Illustration of a capacitorless dynamic random-access memory (DRAM) circuit composed of an FBFET [43,44].](image)

There are reasons why FBFET devices should command particular attention. First, the MSDRAM uses a mechanism based on the meta-stable dip hysteresis effect, which requires hysteresis [34]. However, the super-coupling effect, which occurs below 10 nm, makes it difficult for the electrons and hole channels to coexist [35,36]. Secondly, A2RAM considers the high state as that when sufficient holes are stored in the body to create a current bridge from the source to the drain [37]. The other state is defined by the disconnected bridge in the fully depleted state [38]. However, the fabrication and variability of bridges in films is limited when the overall thickness is less than 10 nm. The operation mechanism of the FBFET as 1T-DRAM is as follows. The FBFET has potential barriers controlled by the gate voltage that blocks the flow of electrons or holes along the channel. The mechanism by which hysteresis occurs is that the voltage applied to the gate causes a small collapse owing to the band modulation at the potential barrier [43-48]. A flow of carriers then occurs, which are sequentially trapped in the potential wall. The potential walls affected by the accumulated carriers cause a constant change in the height of the opposite potential barrier, which controls the flow of the other carriers. As a result, there is a huge difference in the current flowing to the source and drain repeatedly, which eventually collapses both potential barriers through the carriers trapped in the potential walls [46].

The condition in which carriers are trapped in the potential wall to allow the current to flow well is defined as “1”. Accordingly, the process of trapping the carriers in the potential wall is referred to as the process of “writing”, whereas “holding” is the process of maintaining the data value, and “reading” is the current value in the trapped state [43-48]. In contrast, the carrier is released from the potential wall, and thus the height of the potential barrier is high, and the current is blocked. In this case, the state can be written by removing the trapped carrier by adding applied voltage to the opposite gate voltage to release the carrier.
To write the state of ‘0’, the gate voltage is dropped to 0 V to remove the carrier from the channel region located below the gate. Holding state ‘0’ involves returning to a highly negative $V_G$ ($V_{Ge}$) range, the device is not in equilibrium because there are no carriers that can be pulled to construct the inversion layer (deep depletion). The rapid change in potential makes the hole injection barrier very steep. To read the ‘0’ state, data is read with a negative pulse. $V_D$ should be allowed to select between the measured $V_{De}$ values in the DC and transient modes, so that the diode does not turn on to ignore uncalled current. State ‘0’ must be refreshed constantly because the energy barrier and $V_{De}$ are lowered by trapped carriers that are generated to recharge the channel region under the gate (see Figures 10 and 11) [46].

![Illustrated waveform of a capacitor-less DRAM’s operation. The DRAM is composed of a $Z^2$-FET with $V_{BG} = 2$ V [43,44].](image)

**Figure 10.** Illustrated waveform of a capacitor-less DRAM’s operation. The DRAM is composed of a $Z^2$-FET with $V_{BG} = 2$ V [43,44].

![Diagram of a capacitor-less DRAM equivalent circuit with logic values “0” and “1” in three states: writing, holding, and reading (logic). The arrow line at Hold “0” corresponds to the leakage current of the reverse-biased drain junction limiting the hold time [43].](image)

**Figure 11.** Diagram of a capacitor-less DRAM equivalent circuit with logic values “0” and “1” in three states: writing, holding, and reading (logic). The arrow line at Hold “0” corresponds to the leakage current of the reverse-biased drain junction limiting the hold time [43].

As the gate voltage is set to 0 V to remove the potential barrier, state ‘1’ is written. The $V_A$ pulse causes the forward bias of the P-I-N diode, allowing electrons and holes to flow into the channel region when the FBFET is viewed separately from the gate. To hold state ‘1’, $V_C$ is applied such that carriers flowing through the channel region are attracted to a certain space under the gate. The barrier is lower
than that in the state of holding ‘0’, and $V_{ON}$ is reduced. Reading state ‘1’ uses the pulse on the source of the FBFET to create a current in the device, which should be high [46].

In summary, in the ‘1’ state, carriers are stored in the potential wall located in the channel on the body and increase the potential, thus lowering the potential barrier, which leads to a reduced threshold voltage and a high current. In state ‘0’, carriers are removed from the trap located in the channel region on the body and reduce the affordable current [43–48].

In addition, a novel FBFET-based SRAM cell has been proposed. For these SRAM cells, the steep-switching characteristic conferred by the positive feedback operation allows for high-speed memory operation, while the high cell area, which has been considered a limitation in conventional SRAM, is solved through a simple device structure using the FBFET (see Figure 12) [52–54]. The cell achieves a small area of $8F^2$, enabling high-density integrated memory cell design, while the low switching current dramatically reduces the switching characteristics, simultaneously allowing the performance of low-power memory. The SRAM bit-cell also demonstrates the excellent operating performance of SRAM, including a write speed, fast read speed, and competent retention time based on the trapped charges in the channel region next to the source/drain [52–54]. As a result, these results show the great potential of FBFET DRAM and SRAM for the next-generation memory applications.

![Figure 12. Illustrated 2T-static random-access memory (SRAM) circuit composed of FBFET [52].](image)

### 4.3. Neuromorphic Cells

ANNs, which have been developed based on the neurotransmitter structure of biological neurons, have been proposed as a powerful method that can be used in place of conventional Neumann computing, especially for pattern recognition and classification [57,58]. Unlike von Neumann’s existing computer architecture, ANNs have been proposed to solve the problem of not being able to compete with the energy efficiency of the biological brain. A new generation of ANNs have been proposed using spiking neural networks (SNNs) (see Figure 13) [59–62]. However, the traditional neuron circuits of SNNs require large areas as well as high power consumption. The application of FBFETs to neuromorphic devices is being investigated to solve these issues. PF devices with a split-gate floating body are proposed as new neuron devices that demonstrate integration-and-fire capabilities (see Figure 13). This simulation used a common magnetic controller in the neuron layer and demonstrated the successful operation of a high-density multiple-PF neuron system exhibiting reset and lateral suppression. A reduction in power consumption of ~100 times was reported, demonstrating the potential for use of FBFETs in neuromorphic circuits. The energy consumption of the current is proportional to the number of spikes. The average energy consumption of the total output neurons was reduced by approximately 94% compared to conventional neuron circuits. When the PF device
value was applied, a low threshold swing (0.04 mV/decade) of the device was obtained, which reduced the existing 25 pJ/spike of the neuron circuit to ~0.25 pJ/spike (see Figure 13c,d). In addition, charge storage through trapping in the potential walls of the wider body of the FBFET functions to imitate the integration in biological neurons without large capacitors. By replacing the $C_{\text{mem}}$ of the conventional neuron circuit, which requires a large space, by using positive feedback for the charge trap layer of the device, a smaller area and higher density of devices are available. Note that $C_{\text{mem}}$ refers to the membrane capacitor of the average neural circuit. As many transistors and capacitors have traditionally been needed for neuromorphic circuits, creating high density is important for their development. A 17-fold reduction in the area of the neurons was reportedly achieved through the use of FBFETs [21].

Figure 13. (a) Illustration of pattern classification with a spiking neural network and (b) the proposed neuron circuit diagram for a capacitorless structure with FBFETs for “integration-and-fire” [55,91]. (c,d) Transient currents flowing through the trigger device in three different neurons when the same number of input pulses are provided to the neuron circuit [21].

5. Conclusions

In this paper, starting with the first proposed FBFET, various device structures were explored, and the positive feedback mechanism comprising their principle of operation was explained in detail. As a result of the positive feedback phenomenon, FBFETs show excellent subthreshold swing values (~0 mV/decade at 300 K) and high on/off current ratios (~10$^{10}$), giving them potential for use as next-generation memory cells with hysteresis. FBFETs are applied to 1T-1C DRAM to create a capacitor-less DRAM and to 6T-SRAM to create 2T-SRAM. These novel DRAM and SRAM devices can overcome the limits of conventional devices. FBFETs have also been applied to neuromorphic circuits, which have shown significantly improved performance. They can simultaneously solve both the power consumption and large-required areas. These data confirm the possibility of replacing existing devices with next-generation devices having ultra-low power, high performance, and high density.

Author Contributions: C.L., J.S. and C.S. equally contributed to this work. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2020R1A2C1009063). And, this work was supported by the Future Semiconductor Device Technology Development Program (10052925) funded by the Ministry of Trade, Industry & Energy (MOTIE) and the Korea Semiconductor Research Consortium (KSRC).

Conflicts of Interest: The authors declare that there is no conflict of interest.
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