Abstract—For large scale applications, hybrid pixel detectors, in which sensor and read-out IC are separate entities, constitute the state of the art in pixel detector technology to date. They have been developed and start to be used as tracking detectors and also imaging devices in radiography, autoradiography, protein crystallography and in X-ray astronomy. A number of trends and possibilities for future applications in these fields with improved performance, less material, high read-out speed, large radiation tolerance, and potential off-the-shelf availability have appeared and are momentarily matured. Among them are monolithic or semi-monolithic approaches which do not require complicated hybridization but come as single sensor/IC entities. Most of these are presently still in the development phase waiting to be used as detectors in experiments. The present state in pixel detector development including hybrid and (semi-)monolithic pixel techniques and their suitability for particle detection and for imaging, is reviewed.

Index Terms—pixel detector, hybrid pixels, monolithic pixels, tracking, imaging

I. INTRODUCTION

Albeit being similar at first sight, the requirements for charged particle detection in high energy physics compared to imaging applications with pixel detectors can be very different. In particle physics experiments charged particles, usually triggered by other subdetectors, have to be identified with high demands on spatial resolution and timing. In imaging applications the image is obtained by the un-triggered accumulation (integrating or counting) of the quanta of the impinging radiation, often also with high demands (e.g. > 1 MHz per pixel in certain radiography or CT applications). Si pixel detectors for high energy charge particle detection can assume typical signal charges collected at an electrode in the order of 5,000-10,000 electrons even taking into account charge sharing between cells and detector deterioration after irradiation to doses as high as 60 Mrad. In 3H-autoradiography, on the contrary, or in X-ray astronomy the amount of charge to be collected with high efficiency can be much below 1000 e. The spatial resolution is governed by the attainable pixel granularity from a few to about 10 µm at best, obtained with pixel dimensions in the order of 50 µm to 100 µm. The requirements from radiology are similar. Mammography (~ 80 µm pixel dimensions) is most demanding with respect to space resolution. Some applications in autoradiography, however, require sub-µm resolutions, not attainable with present day semiconductor detectors. For applications with lower demands on the spatial resolution (PSF ~ 5-10 µm) but with requirements on real time and time resolved data acquisition, semiconductor pixel detectors are very attractive.

Very thin detector assemblies are mandatory for vertex detectors at collider experiments, in particular for the planned linear $e^+e^-$ collider. This imposes high demands on the detector development. While silicon is almost a perfect material for particle physics detectors, allowing the shaping of electric fields by tailored impurity doping, the need of high photon absorption efficiency in radiological applications requires the study and use of semiconductor materials with high atomic charge, such as GaAs or CdTe. For such materials the charge collection properties are much less understood and mechanical issues in particular those related to hybrid pixels are abundant, most notably regarding the hybridization of detectors when they are not available in wafer scale sizes. Finally, for applications in high radiation environments, such as hadron colliders, radiation hard sensors are developed using either Si with a dedicated design or CVD-diamond.

II. HYBRID PIXELS: THE STATE OF THE ART IN PIXEL DETECTOR TECHNOLOGY

In the hybrid pixel technique sensor and FE-chips are separate parts of the detector module connected by small conducting bumps applied by using the bumping and flip-chip technology. All LHC-collider-detectors [1], [2], [3] ALICE, ATLAS, and CMS, LHCb for the RICH system [4], as well as some fixed target experiments (NA60 [5] at CERN and BTeV [6] at Fermilab) employ the hybrid pixel technique to build large scale ($\sim m^2$) pixel detectors. Pixel area sizes are typically 50 µm × 400 µm as for ATLAS or 100 µm × 150 µm as for CMS. The detectors are arranged in cylindrical barrels of 2–3 layers and disks covering the forward and backward regions. The main purpose of the detectors at LHC is (a) the identification of short lived particles (e.g. b-tagging for Higgs and SUSY signals), (b) pattern recognition and event reconstruction and (c) momentum measurement. The detectors need to withstand a total (10 yr) particle fluence of $10^{15} n_{eq}$ corresponding to a radiation dose of about 50 Mrad. The discovery that oxygenated silicon is radiation hard with respect to the non-ionizing energy loss of protons and pions [7] saves pixel detectors at the LHC for which the radiation is most severe due to their proximity to the interaction point. $n^+$ electrode in n-bulk material sensors have been chosen to cope with the fact that type inversion occurs after about $\Phi_{eq} = 2.5 \times 10^{13}$ cm$^{-2}$. After type inversion the $p$-diode sits on the electrode side thus allowing the sensor to be

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operated partially depleted. Figure I(a) shows the development of the effective doping concentration and the depletion voltage $V_{dep}$ as a function of the fluence expected for 10 years of operation at the LHC (see also [8]). Figures I(b) and (c) show the ATLAS pixel sensor wafer with 3 tiles [9] and the detector response after irradiation over two adjacent pixels showing a very homogeneous charge collection except for some tolerable loss at the outer edges and in an area between the pixels. These are due to the bump contact and a bias grid, respectively, which has been designed to allow testing of the sensors before bonding them to the electronics ICs.

The chip and sensor connection is done by fine pitch bumping and subsequent flip-chip which is achieved with either PbSn (solder) or Indium bumps at a failure rate of $<10^{-4}$. Figure 2 shows rows of $50\,\mu m$ pitch bumps obtained by these techniques.

Indium bumping is done using a wet lift-off technique applied on both sides (sensor and IC) [12]. The connection is obtained by thermo-compression. The Indium joint is comparatively soft and the gap between IC and sensor is about $6\,\mu m$. PbSn bumps are applied by electroplating [13]. Here the bump is galvanically grown on the chip wafer only. The bump is connected by flip-chipping to an under-bump metallization on the sensor substrate pixel. Both technologies have been successfully used with 8" IC-wafers and 4" sensor wafers.

In the case of ATLAS a module of $2.1\times6.4\,cm^2$ area consists of FE-chips bump-connected to one silicon sensor. The I/O lines of the chips are connected via wire bonds to a kapton flex circuit glued atop the sensor. The flex houses a module control chip (MCC) responsible for front end time/trigger control and event building. The total thickness at normal incidence is in excess of 2\% $X_0$. Figure 3 shows a $^{241}$Am ($60\,keV\gamma$) source scan of an ATLAS module with 46080 pixels and an amplitude spectrum obtained using the ToT analog information without clustering of pixels.

The modules are positioned by dedicated robots on carbon-carbon ladders (staves) and cooled by evaporation of a fluorinert liquid ($C_3F_8$) at an input temperature below $-20^\circ C$ in order to maintain the entire detector below $-6^\circ C$ to minimize the damage induced by radiation. This operation requires pumping and the cooling tubes must stand 16 bar pressure if pipe blocking occurs. All detector components must survive temperature cycles between $-25^\circ C$ and room temperature. The LHC pixel detectors are presently in production. A sketch of the final ATLAS pixel detector is shown in fig. 4.

III. TRENDS IN HYBRID PIXEL DETECTORS

To improve the performance of Hybrid Pixel detectors in certain aspects several ideas and developments are being pursued.

A. HAPS

Hybrid (Active) Pixel Sensors (HAPS) [14] exploit capacitive coupling between pixels to obtain smaller pixel cells and pixel
pitch with a larger readout pitch resulting in interleaved pixels. The pixel pitch is designed for best spatial resolution using charge sharing between neighbors while the readout pitch is tailored to the needs for the size of the front-end electronics cell. This way resolutions between 3\(\mu\)m and 10\(\mu\)m can be obtained with pixel (readout) pitches of 100\(\mu\)m (200\(\mu\)m) as is shown in fig. 5(b) together with the layout of a prototype sensor in fig. 5(a).

### B. MCM-D

The present hybrid-pixel modules of the LHC experiments use an additional flex-kapton fine-print layer on top of the Si-sensor (fig. 6(a)) to provide power and signal distribution to and from the module front-end chips. An interesting alternative to the flex-kapton solution is the so-called Multi-Chip-Module Technology deposited on Si-substrate (MCM-D) [16]. A multiconductor-layer structure is built up on the silicon sensor. This allows to bury all bus structures in four layers in the inactive area of the module thus avoiding the kapton flex layer and any wire bonding at the expense of a small thickness increase of 0.1\% \(X_0\). In addition, the extra freedom in routing makes it possible to design pixel detectors which have the same pixel dimensions throughout the sensor, i.e. without larger edge pixels usually necessary to accommodate the sensor area which remains uncovered by electronics in between chips. Figure 6(b) illustrates the principle and fig. 6(c) shows scanning electron microphotographs (curtesy IZM, Berlin) of a via structure made in MCM-D technology.

### C. Active edge 3-D silicon

The features of doped Si allow interesting geometries with respect to field shapes and charge collection. So-called 3D silicon detectors have been proposed [17] to overcome several limitations of conventional planar Si-pixel detectors, in particular in high radiation environments, in applications with inhomogeneous irradiation and in applications which require a large active/inactive area ratio such as protein crystallography [18]. A 3D-Si-structure (fig. 7(a)) is obtained by processing the n\(^+\) and p\(^+\) electrodes into the detector bulk rather than by conventional implantation on the surface. This is done by combining VLSI and MEMS (Micro Electro Mechanical Systems) technologies. Charge carriers drift inside the bulk parallel to the detector surface over a short drift distance of typically 50\(\mu\)m. Another feature is the fact that the edge of the sensor can be a collection electrode itself thus extending the active area of the sensor to within about 10\(\mu\)m to the edge. This results from the undepleted depth at this electrode. Edge electrodes also avoid inhomogeneous fields and surface leakage.
Fig. 6

(A) Schematic view of a hybrid pixel module showing ICs bonded via bump connection to the sensor, the flex hybrid Kapton layer atop the sensor with mounted electrical components, and the module control chip (MCC). Wire bond connections are needed as indicated. (B) Schematic layout of a MCM-D pixel module. (C) SEM photograph of a MCM-D via structure (top) and a cross section after bump deposition (bottom).

currents which usually occur due to chips and cracks at the sensor edges. This is seen in fig. 7(b) which shows the two structures in comparison. The main advantages of 3D-silicon detectors come from the fact that the electrode distance is short (50 µm) in comparison to conventional planar devices at the same total charge, resulting in a fast (1-2 ns) collection time, low (< 10V) depletion voltage and, in addition, a large active/inactive area ratio of the device.

The technical fabrication is much more involved than for planar processes and requires a bonded support wafer and reactive ion etching of the electrodes into the bulk. A compromise between 3D and planar detectors, so called planar-3D detectors maintaining the large active area, use planar technology but with edge electrodes [19], obtained by diffusing the dopant from the deeply etched edge and then filling it with poly-silicon. Prototype detectors using strip or pixel electronics have been fabricated and show encouraging results with respect to speed (3.5 ns rise time) and radiation hardness (> 10^{15} protons/cm²) [20].

D. Diamond Pixel Sensors

Diamond as a potentially very radiation hard material has been explored intensively by the R&D collaboration RD42 at CERN [21]. Charge collection distances up to 300 µm have been achieved. Diamond pixel detectors have been built with pixel electronics developed for the ATLAS pixel detector and operated as single-chip modules in testbeams [22]. A spatial resolution of σ = 22 µm has been measured with 50 µm pixel pitch, compared to about 12 µm with Si pixel detectors of the same geometry and using the same electronics. This reveals the characteristic systematic spatial shifts observed in CVD diamond due to the crystal growth. Grain structures are formed in which trapped charges at the boundaries produce polarization fields inside the sensor which cause the observed spatial shifts of the order of 100-150 µm.

IV. HYBRID PIXELS IN IMAGING APPLICATIONS

A. Counting Pixel Detectors for (Auto-)Radiography

A potentially new route in radiography techniques is the counting of individual X-ray photons in every pixel cell. This approach offers many features which are very attractive for X-ray imaging: full linearity in the response function and a principally infinite dynamic range, optimal exposure times and a good image contrast compared to conventional film-foil based radiography. It thus avoids over- and underexposed images. Counting pixel detectors must be considered as a very direct spin-off of the detector development for particle physics into biomedical applications. The analog part of the pixel electronics is in parts close to identical to the one for LHC pixel detectors while the periphery has been replaced by the counting circuitry [23].

The challenges to be addressed in order to be competitive with integrating radiography systems are: high speed (> 1 MHz) counting with a range of at least 15 bit, operation with very little dead time, low noise and particularly low threshold operation with small threshold dispersion values. In particular the last item is important in order to allow homogeneous imaging of soft X-rays. It is also mandatory for a differential
energy measurement, realized so far as a double threshold with energy windowing logic \[23, \ 25\]. A differential measurement of the energy, exploiting the different shapes of X-ray spectra behind for example tissue or bone, can enhance the contrast performance of an image. Finally, for radiography high photon absorption efficiency is mandatory, which renders the not easy task of high Z sensors and their hybridization necessary.

Progress with counting pixel systems have been reported at this conference \[24, \ 27, \ 28\]. The MEDIPIX chip developed by the MEDIPIX collaboration \[29, \ 25\] uses \(256 \times 256\), \(55 \times 55 \mu \text{m}^2\) pixels fabricated in \(0.25 \mu \text{m}\) technology, energy windowing via two tunable discriminator thresholds, and a 13 bit counter. The maximum count rate per pixel is about 1 MHz. Figure 8 shows an image of a \(^{55}\text{Fe}\) point source obtained with the Medipix2 chip bonded to a \(14\times14 \text{ mm}\^2\), \(300 \mu \text{m}\) thick Si sensor \[26\]. A similar image with a single chip CdTe detector and a higher energy \(^{109}\text{Cd}\) source (122 keV \(\gamma\)) has also been taken and the capability to detect low energy beta decays from tritium has been demonstrated \[26\].

A Multi-Chip module with 2x2 chips using high-Z CdTe sensors with the MPEC chip \[27\] is shown in fig. 9. The MPEC chip features 32 \(\times\) 32 pixels (200\(\times\)200\(\mu\)m\(^2\)), double threshold operation, 18-bit counting at \(\sim\)1 MHz per pixel as well as low noise values (\(\sim\)120e with CdTe sensor) and threshold dispersion (2\(\delta\)e after tuning) \[30, \ 27\]. A technical issue here is the bumping of individual die CdTe sensors which has been solved using Au-stud bumping with In-filling \[31\].

A challenge for counting pixel detectors in radiology is to build large area detectors. Commercially available integrating pixellated systems such as flat panel imagers \[32, \ 33\] constitute the levelling scope.

B. Protein Crystallography

Hybrid Pixel detectors as counting imagers lead the way to new classes of experiments in protein crystallography with synchrotron radiation \[33\]. Here the challenge is to image, with high rate (\(\sim\)1-1.5 MHz/pixel) and high dynamic range, many thousands of Bragg spots from X-ray photons of typically 12 keV or higher (corresponding to resolutions at the 1\(\AA\) range), scattered off protein crystals. The typical spot size of a diffraction maximum is \(100-200\mu\text{m}\), calling for pixel sizes in the order of \(100-300\mu\text{m}\). The high linearity of the hit counting method and the absence of so-called "blooming effects", i.e. the response of non-hit pixels in the close neighborhood of a Bragg maximum, makes counting pixel detectors very appealing for protein crystallography experiments. A systematic limitation and difficulty is the problem that homogeneous hit/count responses in all pixels, also for hits at the pixel boundaries or between pixels where charge sharing plays a role must be maintained by deliberate threshold tuning. Counting pixel developments are made for ESRF (Grenoble, France) \[35\] and SLS (Swiss Light Source at the Paul-Scherrer Institute, Switzerland) beam lines. The PILATUS 1M detector \[36\] at the SLS (217\(\mu\text{m} \times217\mu\text{m}\) pixels) is made of fifteen 16-chip-modules each covering \(8 \times 3.5\text{ cm}\^2\), i.e. a total area of \(40 \times 40\text{ cm}\^2\). Figure 10(a) shows a photograph of this detector with 15 modules and close to \(10^6\) pixels covering an area of \(20 \times 24\text{ cm}\^2\) \[37\]. It is the first large scale hybrid pixel detector in operation. Figure 10(b) shows a Bragg image of a Lysozyme with 10s exposure to 12 keV synchrotron X-rays \[37\]. Many spots are contained in one pixel which is the limit of the achievable point spread resolution.

In summary hybrid pixel detectors are the present state of the art in pixel detector technology. For tracking as well as for imaging applications large (\(\sim\)m\(^2\)) detectors are being built or already in operation (PILATUS). On the negative side are the comparatively large material budget, the complicated assembling (hybridization) with potential yield pitfalls, and the difficulty to obtain high assembly yields with non-wafer scale high-Z sensor materials. As trends within this technology,
V. MONOLITHIC AND SEMI-MONOLITHIC PIXEL DETECTORS

Monolithic pixel detectors, in which amplifying and logic circuitry as well as the radiation detecting sensor are one entity, produced in a commercially available technology, are the dream of semiconductor detector developers. This will not be possible in the near future without compromising. Developments and trends in this direction have much been influenced by R&D for vertex tracking detectors at future colliders such as a Linear $e^+e^-$ Collider. Very low ($\ll 1\% X_0$) material per detector layer, small pixel sizes ($\sim 20\mu m \times 20\mu m$) and a good rate capability (80 hits/mm$^2$/ms) is required, due to the very intense beamstrahlung of narrowly focussed electron beams close to the interaction region which produce electron positron pairs in vast numbers. High readout speeds of 50 MHz line rate with 40$\mu s$ frame time are necessary.

Interleaved pixels and MCM-D promise better resolution and more homogeneous modules, while 3D-silicon detectors can address applications in high radiation environments or those where a large active/inactive area ratio is mandatory.

Among the developments of monolithic or semi-monolithic pixel devices perhaps the following classifying list can be made.

- **Non-standard CMOS on high resistivity bulk**
  The first monolithic pixel detector, successfully operated in a particle beam already in 1992 [39], used a high resistivity p-type bulk p-i-n detector in which the junction had been created by an n-type diffusion layer. On one side, an array of ohmic contacts to the substrate served as collection electrodes (fig. 11(a)). Due to this only simple pMOS transistor circuits sitting in n-wells were possible in the active area. The technology was certainly non-standard and non-commercial. No further development emerged.

- **CMOS technology with charge collection in epi-layer**
  Commercial CMOS technologies use low resistivity silicon which is not suited for charge collection. However, in some technologies an epitaxial silicon layer of a few to 15$\mu m$ thickness can be used [40], [41], [42]. The generated charge is kept in the epi-layer by potential wells at the boundary and reaches an n-well collection diode by thermal diffusion (fig. 11(b)). The signal charge is therefore very small ($< 1000e$) and low noise electronics is a real challenge. As this development uses standard processing technologies it is potentially very cheap. Despite using CMOS technology the potential of full CMOS circuitry in the active area is not available (only nMOS) because of the n-well/p-epi collecting diode which does not permit other n-wells.
DETECTOR USING HIGH RESISTIVITY SILICON BULK INSULATED FROM THE AMORPHOUS SILICON ON TOP OF STANDARD CMOS VLSI CMOS on SOI (non-standard) - Amorphous silicon on standard CMOS ASICs Hydrogenated amorphous-Silicon (a-Si:H), where the H-content is up to 20%, can be put as a film on top of CMOS ASIC electronics. a-Si:H has been studied as a sensor material long ago and has gained interest again with the advancement in low noise, low power electronics. The signal charge collected in the <30 µm thick film is in the range of 500-1500 electrons. A cross section through a typical a-Si:H device is shown in fig. 12b. From a puristic view it is more a hybrid technology, but the main disadvantage of the hybridization connection is absent. The radiation hardness of these detectors appears to be very high >10^{15}cm^{-2} due to the defect tolerance and defect reversing ability of the amorphous structure and the larger band gap (1.8 eV). The carrier mobility is very low (\mu_e = 2-5 cm^2/Vs, \mu_h = 0.005 cm^2/Vs), i.e. essentially only electrons contribute to the signal. Basically any CMOS circuit and IC technology can be used and technology changes are uncritical for this development. For high-Z applications poly-crystalline HgI_2 constitutes a possible semiconductor film material. The potential advantages are small thickness, radiation hardness, and low cost. The development is still in its beginnings and – as for CMOS active pixel sensors – a real challenge to analog VLSI design.

- Amplification transistor implanted in high resistivity bulk In so-called DEPFET pixel sensors a JFET or MOS-FET transistor is implanted in every pixel on a sideways depleted bulk. Electrons generated by radiation in the bulk are collected in a potential minimum underneath the transistor channel thus modulating its current (fig. 13). The bulk is fully depleted rendering large signals. The small capacitance of the internal gate offers low noise operation. Both together can be used to fabricate thin devices. The sensor technology is non-standard and the operation of DEPFET pixel detectors requires separate steering and amplification ICs (see below).

Because CMOS active pixels and DEPFET pixels are most advanced in their development, they are discussed in more detail below.

A. CMOS Active Pixels The main difference of CMOS monolithic active pixel sensors to CMOS camera chips is that they are larger in area and must have a 100% fill factor for efficient particle detection. Standard commercial CMOS technologies are used which have a lightly doped epitaxial layer between the low resistivity silicon bulk and the planar processing layer. The epi-layer is – technology dependent – at most 15 µm thick and can also be completely absent. Collaborating groups around IReS/LEPSI, RAL and Irvine-LBNL-Ohio use similar approaches to develop large scale CMOS active pixels also called MAPS (Monolithic Active Pixel Sensors). Prototype detectors have been produced in 0.6µm, 0.35µm and 0.25µm CMOS technologies. In the MAPS device (fig. 11b) electron-hole pairs created by ionization energy loss in the epitaxial layer remain trapped between potential barriers on both sides of the epi-layer and reach, by thermal diffusion, an n-well/p-epi collection diode. The sensor is depleted only directly under the n-well collection diode where full charge collection is obtained; the charge collection is incomplete in all other areas. With small pixel cells collection times in the order of 100 ns are obtained. The signal...
is small, some hundred to 1000e, depending on the thickness of the epi-layer. A chip submission using a process with no epi-layer, but with a low doped substrate of larger resistivity has also been tried (MIMOSA-4) which proved to function with high detection efficiency for minimum ionizing particles. This renders the uncertainty and dependence on the future of the epi-layer thickness in different technologies less constraining.

Matrix readout performed using a standard 3-transistor circuit (line select, source-follower stage, reset) commonly employed by CMOS matrix devices, but can also include current amplification and current memory. For an image deployed by CMOS matrix devices, but can also include circuit (line select, source-follower stage, reset) commonly employed by CMOS matrix devices, but can also include current amplification and current memory. For an image deployed by CMOS matrix devices, but can also include circuit (line select, source-follower stage, reset) commonly employed by CMOS matrix devices, but can also include circuit (line select, source-follower stage, reset) commonly employed by CMOS matrix devices, but can also include circuit (line select, source-follower stage, reset) commonly employed by CMOS matrix devices, but can also include circuit (line select, source-follower stage, reset). The radiation hardness of CMOS devices is always a crucial question for particle detection in high intensity colliders. MAPS appear to sustain non-ionizing radiation (NIEL) to $\sim 10^{12}n_{eq}$ while the effects of ionizing radiation damage (IEL) are at present still unclear. Apart from this the focus of further development lies in making larger area devices and in increasing the charge collection performance in the epi-layer. For the former, first results in reticle stitching, that is electrically connecting IC area over the reticle border, have been encouraging (fig. 14(a)). Full CMOS stitching over the reticle border still has to be demonstrated. The poor charge collection by thermal diffusion is another area calling for ideas. Approaches using more than one n-well collecting diode, a photo-FET, or a photo-GATE are currently investigated. The photo-FET called technique (fig. 14(b)) has features similar to those of DEPFET pixels (see below). A pMOS FET is implanted in the charge collecting n-well and signal charges affect its gate voltage and modulate the transistor current.

![Fig. 14](image)

(A) SEAMLESS STITCHING IN BETWEEN WAFER RETICLES TO OBTAIN LARGE AREA CMOS ACTIVE PIXELS, (B) SCHEMATIC OF A pMOS PHOTO-FET TO IMPROVE CHARGE COLLECTION IN MAPS.

Above all, the advantages of a fully CMOS monolithic device relate to the adoption of standard VLSI technology and its resulting low cost potential (potentially $\sim 25\text{ per cm}^2$). In turn the disadvantages also come largely from the dependence on commercial standards. The thickness of the epi-layer varies for different technologies. It becomes thinner for smaller processes and with it also the number of produced signal electrons vanishes. Only a few processing technologies are suited. With the rapid change of commercial process technologies this is an issue of concern. The fact that good detector performance has been seen with non-epi wafers material provides some relief. Furthermore, in the active area, due to the n-well collection diode, no CMOS (only nMOS) circuitry is possible. The voltage signals are very small ($\sim \text{mV}$), of the same order as transistor threshold dispersions requiring very low noise VLSI design. The radiation tolerance of CMOS pixel detectors for particle detection beyond $10^{12}n_{eq}$ is still a problem although the achieved tolerance should be sufficient for a Linear Collider. Improved readout concepts and device development for high rate particle detection at a linear collider is under development. For the upgrade of the STAR microvertex detector the use of CMOS active pixels is planned.

**B. DEPFET Pixels**

The Depleted Field Effect Transistor structure (DEPFET) provides detection and amplification properties jointly and has been experimentally confirmed and successfully operated as single pixel structures and as large (64x64) pixel matrices. The DEPFET detector and implanted amplification structure is shown in fig. 15. Sidewards depletion provides a parabolic potential which has – by appropriate biasing and a so-called deep-n implantation – a local minimum for electrons ($\sim 1\mu m$) underneath the transistor channel. The channel current can be steered and modulated by the voltage at the external gate and - important for the detector operation - also by the deep-n potential (internal gate). Electrons collected in the internal gate are removed by a clear pulse applied to a dedicated CLEAR contact outside the transistor region or by other clear mechanisms. The very low input capacitance (few fF) and the in situ amplification makes DEPFET pixel detectors very attractive for low noise operation. Amplification values of 400 pA per electron collected in the internal gate have been achieved. Further amplification enters at the second level stage (current based readout chip).

DEPFET pixels are currently being developed for three very different application areas: vertex detection in particle physics, X-ray astronomy and for biomedical autoradiography. Figure 15 summarizes the achieved performance in noise and energy resolution with single pixels structures (fig. 15(a)) and in spatial resolutions with 64x64 pixels matrices (fig. 15(b)). With round single pixel structures noise figures of 2.2e at room temperature and energy resolutions of 131 keV for 6 keV X-rays have been obtained. With small (20x30 $\mu m^2$) linear structures fabricated for particle detection at a Linear Collider the noise figures are about 10e. The spatial resolution read off from fig. 15(b) in matrices operated with 50 kHz line rates is

$$\sigma_{xy} = (4.3 \pm 0.8)\mu m \quad \text{or} \quad 57 \frac{LP}{mm} \quad \text{for} \quad 22\text{ keV } \gamma$$

$$\sigma_{xy} = (6.7 \pm 0.7)\mu m \quad \text{or} \quad 37 \frac{LP}{mm} \quad \text{for} \quad 6\text{ keV } \gamma$$
The capability to observe tritium in autoradiographical applications is shown in fig. 15(c).

![Image](45x576 to 306x700)

Fig. 15

(A) RESPONSE OF A SINGLE DEPFET PIXEL STRUCTURE TO 6KEV X-RAYS FROM AN $^{55}$Fe SOURCE, (B) IMAGE OBTAINED WITH $^{55}$Fe AND A TEST CHART, THE SMALLEST STRUCTURES HAVE A PITCH OF 50µM AND ARE 25µM WIDE, (C) 3H LABELED LEAF.

The very good noise capabilities of DEPFET pixels are very important for low energy X-ray astronomy and for autoradiography applications. For particle physics, where the signal charge is large in comparison, this feature is used to design very thin detectors (≈50µm) with very low power consumption when operated as a row-wise selected matrix [50]. Thinning of sensors to a thickness of 50µm using a technology based on deep anisotropic etching has been successfully demonstrated [61]. For the development of DEPFET pixels for a Linear Collider matrix row rates of 50 MHz and frame rates for 520x4000 pixels of 25 kHz, read out at two sides, are targeted. Sensors with cell sizes of 20x30 $\mu$m$^2$ have been fabricated and complete clearing of the internal gate, which is important for high speed on-chip pedestal subtraction, has been demonstrated [59]. A large matrix is readout using sequencer chips for row selection and current based chip for column readout [59]. Both chips have been developed at close to the desired speed for a Linear Collider. The estimated power consumption for a five layer DEPFET pixel vertex vertex detector is only 5W rendering a very low mass detector without cooling pipes feasible. The most recent structures use MOSFETs as DEPFET transistors for which the radiation tolerance still has to be investigated.

VI. SUMMARY

Driven by the demands for high spatial resolution and high rate particle detection in high energy physics, semiconductor pixel detectors have started to also become exploited for imaging applications. Hybrid pixel detectors, in which sensor and electronic chip are separate entities, connected via bump bonding techniques represent today’s state of the art for both, particle detection and imaging applications. New trends include interleaved pixels having different pixel- and readout-pitches, MCM-D structures and 3D-silicon detectors with active edges. Monolithic or semi-monolithic detectors, in which detector and readout ultimately are one entity, are currently developed in various forms, largely driven by the needs for particle detection at future colliders. CMOS active pixel sensors using standard commercial technologies on low resistivity bulk and SOI pixels, a-Si:H, and DEPFET-pixels, which try to maintain high bulk resistivity for charge collection, classify the different ways to monolithic detectors which are presently carried out.

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