Performance Analysis of FDSOI based Gate Diffusion Input Logic Gates at 28nm Technology Node

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Abstract. In this paper, Fully Depleted Silicon on Insulator (FDSOI) MOSFET at 28nm channel length are simulated in COGENDA Visual TCAD tool. Buried Oxide layer (BOX) between channel and substrate in FDSOI improves the electric field inside the device. The device characteristics are compared in terms of threshold voltage, transconductance parameter, I_on/I_off ratio and Short Channel Effects (SCEs). To implement VLSI circuits, Complementary Metal Oxide Semiconductor (CMOS) logic is a common choice. However, in the case of CMOS, the logic implementation requires a transistor count equal to twice the number of logic inputs. Therefore, the area is always an issue in the case of the CMOS logic family. To address this issue, Gate Diffusion Input (GDI) based logic has been investigated because it uses less number of transistors. Hence FDSOI MOSFET based GDI logic gates are proposed in this article. FDSOI MOSFET exhibits improved electrical characteristics which can reduce the power consumption considerably and help in expanding the battery life of devices while the GDI logic helps in designing the compact circuit for portable equipment.

1. Introduction
Designers are pushing billions of transistors on a single VLSI chip to realize a wide variety of applications [1]. The complexity of the chip has compounded many applications but has also given rise to problems like thermal variations, process variations, packaging, cooling issues etc. The Computer-Aided Design (CAD) has further aided the growth in the complexity and performance of integrated circuits in the nanoscale integrated circuits [2]. With such a phenomenal increase in complexity, it is more crucial than ever before to manage the design process, in order to maintain the reliability, quality, and extensibility of the given circuit. The design process involves several hierarchical steps that address the chip design complexity from system specification down to the physical layout. Just above the layout design is the logic level followed by the device level of abstraction [3-6]. At a logic level, the focus is to reduce power dissipation and circuit complexity. While at a device level, the focus is to improve the performance by altering the transistor structure and design parameters. The work presented in this paper focuses on the circuit level as well as the device level.

Usually, Complementary Metal Oxide Semiconductor (CMOS) logic is popularly used for VLSI circuits at the logic level. However, in the case of CMOS, the logic implementation requires a transistor count equal to twice the number of logic inputs. Therefore, the area is always an issue in the case of CMOS logic family. To address this issue, a novel logic based on Gate Diffusion Input (GDI) has been investigated by researchers. GDI cell looks similar to CMOS inverter but it consists of three inputs as compared to single input in a CMOS inverter [10]. Next at the device level, industry has
relied on Silicon on Insulator (SOI) MOSFET structure. The structure of SOI MOSFET consists of an insulating layer placed over the substrate which may refer as Si-insulator-Si substrate [8]. This provides reduction in power consumption, parasitic capacitances, gate to source voltage, leakage current and temperature dependency. It also provides complete isolation of source and drain region [9]. Therefore, Fully Depleted SOI (FDSOI) MOSFET is used instead of conventional MOSFET to improve the performance of the proposed logic gates [12].

First, the FDSOI and conventional (bulk) MOSFET are simulated. The characteristics like threshold voltage, transconductance, I_{on}/I_{off} current ratio and Drain Induced Barrier Lowering (DIBL) are used as parameters for comparison of FDSOI MOSFET with the conventional (bulk) MOSFET at device level. The process parameters at 28nm channel length are used while calculating all simulation results. The FDSOI MOSFET is then used to implement the inverter and FDSOI based Gate Diffusion Input (GDI) logic gates that include GDI 'NOT, GDI 'F1', GDI 'F2', GDI 'OR', GDI 'AND' [13]. Noise Margin and transient characteristics of FDSOI based GDI logic have also been discussed.

2. Device Level Design Description

2.1. Structure and Simulation

In FDSOI MOSFET the silicon layer placed over the buried oxide layer is very thin so that the full body region is deprived of charge carriers and the device is therefore called fully depleted [11-13]. In contrast to planar bulk technology, the parasitic capacitance between the source and drain region is reduced due to the presence of oxide layer under the channel region deep into the bulk [14-16]. This buried oxide layer helps in reducing leakage currents and hence the power dissipation in the MOSFET is minimized [17].

![Figure 1: (a) Structure of Bulk MOSFET (b) Device drawing showing Bulk NMOS Mesh](image)

| Parameter                 | Bulk MOSFET | FDSOI MOSFET |
|---------------------------|-------------|--------------|
| Gate Length               | 28 nm       | 28 nm        |
| Gate Oxide thickness      | 6 nm        | 6 nm         |
| Substrate thickness       | 60 nm       | 20 nm        |
| Buried oxide thickness    | -           | 20 nm        |
| Source/Drain length       | 20 nm       | 20 nm        |
| Source/Drain doping depth | 4 nm        | 6 nm         |
| Source/Drain doping conc. | 1e-20 cm$^3$| 1e-18 cm$^3$|
| Substrate doping conc.    | 1e-18 cm$^3$| 1e-17 cm$^3$|
The structure of Bulk nMOSFET and its TCAD mesh drawing is shown in figure 1(a) and figure 1(b), respectively. Mesh nodes are used for calculations. For precise results, the mesh is kept more refined at interfaces of source and drain with channel [18]. The operating temperature of the bulk and FDSOI MOSFET is done at the room temperature [20]. The TCAD device design considerations are listed in Table 1.

![Figure 1(a) Structure of Bulk nMOSFET and Figure 1(b) Mesh Drawing](image)

**Figure 1.** (a) Structure of Bulk nMOSFET (b) Mesh Drawing showing Bulk pMOS Mesh

2.2. Transfer Characteristics

For both the devices as discussed above, threshold voltage ($V_{th}$) is calculated by the transfer characteristics shown in figure 3. The plot is drawn at constant drain voltage of 1 V. Threshold voltage is a minimum gate to source voltage at which channel inversion takes place and transistor starts conducting [19]. It has been observed from figure 3 that $V_{th}$ for bulk is 0.5 V and is 0.48 V for FDSOI. Transconductance ($g_m$) for bulk MOSFET is calculated as $18.3 \times 10^{-5}$ S/µm and for FDSOI MOSFET it is $20 \times 10^{-5}$ S/µm. Gate Capacitance ($C_g$) is found out to be 48.32 pF for both devices. Figure of Merit (FOM) is calculated to be $3.7 \times 10^6$ and $4.1 \times 10^6$ for Bulk MOSFET and FDSOI MOSFET, respectively. Even at an operating voltage of 0.8V, it is found that FDSOI MOSFET has a greater level of ON state current ($I_{on}$) as compared to bulk MOSFET. It is observed that the order of $I_{on}$ is increased and the amount of undesired leakage current has declined to the order of $10^{-11}$ A/µm. For Bulk MOSFET the ratio ($I_{on}/I_{off}$) is $9.375 \times 10^4$ whereas it is quite high of the order of $8.34 \times 10^7$ for FDSOI MOSFET.

![Figure 2. (a) Structure of FDSOI MOSFET (b) Device drawing showing FDSOI NMOS Mesh](image)

**Figure 2.** (a) Structure of FDSOI MOSFET (b) Device drawing showing FDSOI NMOS Mesh

![Figure 3. Transfer Characteristics](image)

**Figure 3.** Transfer Characteristics
2.3. Drain Characteristics

Drain characteristics are analysed for Bulk MOSFET and FDSOI MOSFET at $V_{gs}$ 0.5V to 2 V as shown in figure 4. FDSOI MOSFET shows better drain characteristics and higher level of drain current when compared for the same value of gate voltage, $V_{gs}$.

![Bulk nMOSFET vs FDSOI nMOSFET Drain Characteristics](image1)

**Figure 4.** Drain Characteristics of Bulk and FDSOI MOSFET at $V_{gs}$ 0.5V to 2V

2.4. Curve to Study Drain Induced Barrier Lowering (DIBL)

DIBL is derived using logarithmic transfer characteristics by using the conventional method. For FDSOI MOSFET, DIBL is derived as 0.067 whereas for Bulk, it is 0.156 as shown in figure 5. As summarized in Table 2, the DC study of results discussed so far show an enhancement in electrical characteristics of proposed device structure as compared to conventional planar MOSFET design. It is realized that FDSOI MOSFET has a better current ratio than Bulk MOSFET and a lower threshold voltage in comparison with Bulk MOSFET. Figure of Merit, for FDSOI, is comparable to Bulk MOSFET. FDSOI structure has shown substantial decrease in DIBL and it can be concluded that FDSOI MOSFET is a promising substitute which is less sensitive to short channel effects such as...
saturation velocity, hot carriers, surface scattering and hence makes it suitable for analyzing GDI logic gates. This study is carried out keeping in view harnessing the potential of FDSOI at device level and take further benefit from GDI logic at the circuit level.

### Table 2 Electrical Characteristics of Bulk and FDSOI MOSFET at 28nm Channel Length

| Electrical Parameter Values (at Vds=1V) | STRUCTURE OF MOSFET |
|----------------------------------------|---------------------|
|                                        | BULK               | FDSOI               |
| Vth (v)                                | 0.50               | 0.48                |
| Ion (A)                                | 1.5 x 10^{-4}      | 1 x 10^{-3}         |
| Ioff (A)                               | 1.6 x 10^{-9}      | 1.2 x 10^{-11}      |
| Ion/Ioff                               | 9.375 x 10^{1}     | 8.34 x 10^{1}       |
| Transconductance (g_m)                 | 18.3 x 10^{-5}     | 2 x 10^{-5}         |
| Figure of Merit (FOM)                  | 3.7 x 10^{6}       | 4.1 x 10^{6}        |
| DIBL                                   | 0.157              | 0.067               |

2.5. Proposed FDSOI Inverter

FDSOI inverter is made by fabricating p-FDSOI and n-FDSOI MOSFETs which is simulated to realize DC characteristics [22]. The logic diagram, SPICE simulation and TCAD layout are given below in figure 6. Both NMOS and PMOS are designed on the same parameters which have a 20 nm silicon substrate as a base, 20 nm SiO2 buried oxide layer (BOX) on the substrate and Si film thickness is 10 nm. Source/Drain of length 20 nm and their contact material is Aluminium. Gate material for NMOS and PMOS is N-Poly Silicon and P-Poly Silicon respectively. A substrate doping of acceptor type of the order of 1e-17 cm^{-3} and Source/Drain is doped with donor type impurity of the order of 1e-18 cm^{-3}. Gate height and Gate oxide thickness of both the structures is 6 nm and 2 nm respectively.

![Figure 6. (a) Logic Diagram and symbol of Inverter (b) Simulated Inverter Circuit](image)

2.6. FDSOI based Logic Gates

**GDI ‘NOT’ Logic:** input G = A, P = V_{DD} [1 or High] and N = GND [0 or Low] then output Y = A’ which is NOT logic. When input G = A, P = B and N = GND [0 or Low] then output Y = A’B which is F1 logic. When input G = A, P = V_{DD} [1 or High] and N = B then output Y = A’+B which is F2 logic. **GDI ‘OR’ Logic.** When input G = A, P = B and N = V_{DD} [1 or High] then output Y = A+B
which is OR logic. *GDI ‘AND’ Logic.* When input \( G = A, P = \text{GND} \) and \( N = B \) then output \( Y = AB \) which is AND logic [21].

![GDI Logic Gates and Truth tables Simulated in this Work](image)

### 3. Results

#### 3.1. Simulation Results of FDSOI Inverter

The DC characteristics of FDSOI Inverter are given below in figure 8. Critical Voltages have also been calculated which help us in calculation of Noise Margin.

| Parameters                        | Values (V) |
|-----------------------------------|------------|
| Max. Output Voltage for Logic level HIGH, \( V_{OH} \) | 1.80       |
| Min. Input Voltage Interpreted as Logic level HIGH, \( V_{IH} \) | 0.98       |
| Min. Output Voltage for Logic level LOW, \( V_{OL} \) | 0          |
| Max. Input Voltage Interpreted as Logic level LOW, \( V_{IL} \) | 0.68       |
| Noise Margin HIGH, \( \text{NM}_H \) | 0.82       |
| Noise Margin LOW, \( \text{NM}_L \) | 0.68       |
| Logical Threshold, \( V_{TH} \) | 0.88       |
DC Characteristics

Critical Parameters

Figure 8. DC Characteristics and values of Critical parameters for FDSOI Inverter

3.2. Simulation Results of FDSOI based GDI Logic Gates

The transient result of GDI NOT logic is shown in figure 9, where $A_{in}$ [V] is referred to as input voltage at $G$ and $Y_{out}$ [V] is an output voltage at $Y$.

Figure 9. Transient result of ‘NOT’ Logic

The transient result of GDI F1 logic is shown in figure 10, where $A_{in}$ [V] is referred to as input voltage at $G$, $B_{in}$ [V] is an input voltage at $P$ and $Y_{out}$ is an output voltage at $Y$.

Figure 10. Transient result of ‘F1’ Logic

The transient result of GDI F2 logic is shown in figure 11, where $A_{in}$ [V] is referred to as input voltage at $G$, $B_{in}$ [V] is an input voltage at $P$, and $Y_{out}$ is an output voltage at $Y$. 
Figure 1. Transient result of ‘F2’ Logic

The transient result of GDI OR logic is shown in figure 12, where $A_{in}[v]$ is referred to as input voltage at G, $B_{in}[V]$ is an input voltage at P and $Y_{out}$ is an output voltage at Y.

Figure 12. Transient result of ‘OR’ Logic

The transient result of GDI AND logic is shown in figure 13, where $A_{in}[v]$ is referred to as input voltage at G, $B_{in}[V]$ is an input voltage at P and $Y_{out}$ is an output voltage at Y.
3.3. Noise Margin in GDI Logic

The noise margin values obtained from inverter characteristics are $NM_H = 0.82$ V and $NM_L = 0.68$ V for logic HIGH and logic LOW, respectively. The minimum Noise Margin of an inverter is 0.68 V. The transient characteristics show some deviation of output with respect to input. Considering all the cases, it is maximum of 0.15 V. Since the voltage deviation is less than the NM value, therefore, all logics in the GDI logic gates are in the acceptable range because these variation can be corrected by connecting the buffer stages at the output of FDSOI based GDI Logic.

4. Conclusion

As expected the FDSOI device structure has improved DC characteristics as compared to conventional bulk MOSFET. This improvement is realized in terms of better current ratio, reduced DIBL at comparable value of threshold voltage and Figure of Merit. Thus, FDSOI is a potential alternative at device level which exhibits a smaller amount of sensitivity to second order effect at reduced channel length. This drops the power dissipation at device level, which in turn expands the battery life of the device. Additionally, for circuit level implementation of electronic VLSI circuits GDI based logic requires less number of transistors, hence it can be seen as an alternative to CMOS design. Thus, FDSOI based MOSFETs are used to simulate NOT, F1, F2, OR and AND GDI logic gates. From the transient analysis of these logic gates, some deviation in maximum and minimum value of output response is witnessed. Since these deviations are less than the overall Noise Margin, therefore, these are acceptable and can be corrected using buffer stage at the output. To avoid deviation in output voltage swing, GDI logic with buffer can be implemented.

A channel length of 28 nm has been taken into consideration for this work. So, further reduction in channel length can be analysed in FDSOI MOSFET. Analysis of variation in parameters such as width of buried oxide, gate oxide material etc. can also be done in the future.
5. References

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