Integrating Epitaxial-Like Pb(Zr,Ti)O$_3$ Thin-Film into Silicon for Next-Generation Ferroelectric Field-Effect Transistor

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The development of ferroelectric random-access memory (FeRAM) technology with control of grain boundaries would result in a breakthrough for new nonvolatile memory devices. The excellent piezoelectric and electrical properties of bulk ferroelectrics are degraded when the ferroelectric is processed into thin films because the grain boundaries then form randomly. Controlling the nature of nucleation and growth are the keys to achieving a good crystalline thin-film. However, the sought after high-quality ferroelectric thin-film has so far been thought to be impossible to make, and research has been restricted to atomic-layer deposition which is extremely expensive and has poor reproducibility. Here we demonstrate a novel epitaxial-like growth technique to achieve extremely uniform and large rectangular-shaped grains in thin-film ferroelectrics by dividing the nucleation and growth phases. With this technique, it is possible to achieve 100-μm large uniform grains, even made available on Si, which is large enough to fabricate a field-effect transistor in each grain. The electrical and reliability test results, including endurance and retention test results, were superior to other FeRAMs reported so far and thus the results presented here constitute the first step toward the development of FeRAM using epitaxial-like ferroelectric thin-films.

In spite of other proposed new memory devices, the only practical chip-featured non-volatile memory (NVM) device is charge-trapping (CT) flash memory device. However, the CT flash memories will eventually face some limitations such as slow ~microsecond program/erase (P/E) speed and poor endurance (maximum 10$^6$ cycles$^{14}$). In addition, the compensating peripheral circuits that are required due to its high operation voltage and slow P/E speed reduces its effective storage area by making the integration level of CT flash memory lower than that of the other random-access memories (RAMs). Thus, the applications of CT flash memory have been extremely limited to auxiliary portable storage devices, such as universal serial bus (USB) and secure digital (SD) memory cards. Therefore, new concepts for NVM, such as phase-change RAM (PeRAM)$^7$, magnetoresistive RAM (MRAM)$^8$, resistive RAM (RRAM)$^9$, and ferroelectric RAM (FeRAM)$^{10,12}$, have been demonstrated for the next generation NVM.

Among these emerging new NVM, the FeRAM uses ferroelectric materials as storage elements and has been a promising candidate since the late 1970s$^{13}$. There were many attempts to replace the current NVM or well-developed dynamic random-access memory (DRAM) because of its similar structure and operation to DRAM and its non-volatility similar to NVM. In a particular type of FeRAM, the ferroelectric field-effect transistor (FeFET) with metal-ferroelectric-insulator-semiconductor (MFIS) structure has been focused for the very-large-scaled-integrated (VLSI) memory cells since 1974$^{14}$. The FeFET can theoretically feature a nano-scaled NVM, nanosecond P/E speed, low-operation voltage, and nondestructive readout operation$^{15-17}$. However, it is reported that it is almost impossible to integrate a high-quality ferroelectric thin-film into Si-based devices because of its naturally formed grain boundaries and undesirable inter-diffusion reaction between the Si and ferroelectric material. It is reported that perovskite SrTiO$_3$ is an excellent substrate for growth of ferroelectric thin-films such as BaTiO$_3$ with near perfect epitaxy but is cannot be applied in the gate oxide of Si-based...
field-effect transistor (FET)\textsuperscript{18,19}. In terms of well-developed semiconductor manufacturing technology, depositing a ferroelectric material directly into Si have no choice but to use a polycrystalline ferroelectric thin-film for gate oxide. Unfortunately, the grain-boundaries in ferroelectric thin-film result in a decreased remnant polarization ($P_r$), a decreased coercive electric field ($E_c$), and an increase leakage current\textsuperscript{20,21}. Moreover, the ferroelectricity is degraded in hydrogen ambient annealing which is a necessary step for back-end-of-line process in FET\textsuperscript{22,23}. Therefore, so far no one truly has demonstrated a FeFET with long retention and good endurance characteristics. In our group, we have analyzed the grain-boundary degradation effects in Pb(Zr,Ti)O$_3$ (PZT) and proposed a solution to achieve an epitaxial-like single-grains by seeding method\textsuperscript{24–27}. This technology is termed selectively nucleated lateral crystallization (SNLC). Separating the nucleation and growth mechanism in PZT can control the grain size and grain-boundaries at a desirable location. Our previous works of were mostly focused on the metal-ferroelectric-metal capacitor for the replace of DRAM capacitor\textsuperscript{24}.

In this work, we have investigated the SNLC mechanism for first time and successfully fabricated a FeFET with epitaxial-like PZT thin-film achieved by SNLC. The grains were in highly uniform rectangular shape with (111) preferred orientation. Based on the high-quality SNLC-PZT, the FeFET showed a long retention and excellent endurance characteristics which is comparable to current CT memory.

Figure 1. SNLC-PZT grain-growth mechanism. Schematic illustration of (a) 1-step: formation of TiO$_x$ and PbO$_x$ traces, (b) 2-step: reaction of TiO$_2$, PbO$_2$ and ZrO$_2$ for PbTiO$_3$ and PbZrO$_3$, (c) 3-step: nucleation of PZT seed formation and (d) 4-step: rosette grain-growth by PbTiO$_3$ migration. Observation of Pt-dot array and its crystal-PZTs by magnitude microscope in (e-f). FE-SEM image of SNLC-PZT grains and its multi-layer cross-section observed by HR-TEM and the corresponding SNLC-PZT diffraction pattern.
The x-ray diffraction (XRD) 2-theta profiles confirm the SNLC perovskite PZT and the intermediate phase of PbTiO$_3$ and PbTi$_3$O$_7$ (Fig. 2a). Since the ZrTiO$_4$ and PZT were deposited below 300°C, there an amorphous-PZT is achieved in the as-deposited condition. The Pt seed showed (111) and (200) of polycrystalline texture at 40 and 46°. After 1-sec of rapid thermal annealing (RTA) at 700°C, various pyrochlore PbTiO$_3$ intermediate phases were observed. Although there were no intensified perovskite-PZT observed in this step, this step is thought to be step 1 and 2 of SNLC mechanism. Afterward, the samples were annealed at 1 and 2 hrs at 550°C by tube-furnace. The intensity of (100) and (101) oriented peaks of PbTiO$_3$ was increased and the intensity of (111) oriented peaks of perovskite-PZT was observed at 38°. After annealing 2-hrs, a (111) preferred perovskite-PZT peak confirms the single-grain of perovskite PZT. The increased (111)-PZT is resulted by converting the pyrochlore intermediate phase to the perovskite PZT, which is considered as the step 4 of SNLC mechanism. If only a single Pt-seed exists, the rosette grain-size cannot be grown infinity. The radius of grain size is strongly influenced by the annealing temperature, not by the annealing time. The behavior of SNLC-PZT grain-growth as a function of annealing temperature and time is shown in Fig. 2b. It is found that the radius of grains are linearly increased at the initial 1hr and eventually saturated after 2 hrs. The saturation phenomenon is a unique process observed only when the nucleation and growth is divided. In classical nucleation and growth, it is reported that the nucleation site controlled by Boltzmann thermodynamics is simultaneously generated with the grain-growth.$^{33-35}$ Thus, typically the grain size is strongly determined by the competing energy of the generating the nucleation site to the energy of the grain-growth. In SNLC mechanism, the average grain size can be obtained up to 52 μm at 650°C; however, it shows a wide standard deviation of grain size. The distributions of the grain size above 650°C annealing showed large formation of nucleation sites which are not artificially controlled by the Pt-seed (Fig. 2c). It is observed that these randomly generated nucleation sites are also competing its energy with the grain-growth energy which becomes similar to the classical nucleation and growth. To understand competing energy of nucleation and growth in SNLC mechanism, the grain-growth activation energy (E$_{Ga}$) is estimated from the extracting the Arrhenius plot of grain-growth rate while the nucleation activation energy (E$_{Na}$) is determined by the onset temperature of the PZT nucleated seed confirmed from the XRD 2-theta profiles. The E$_{Ga}$ was 0.8 eV and the E$_{Na}$ was 0.3 eV which was 0.5 eV lower than the nucleation energy. According to the different energy level, it is effectively suppresses the generation of nucleation sites during the grain-growth (Fig. 2d). Note that the driving force of SNLC is from volume shrinkage in perovskite-to-pyrochlore transformation and it is related to the thermodynamic equilibrium condition. The internal-energy of pyrochlore-structure should be balanced with the

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**Figure 2.** (a) XRD 2-theta profile of as-deposited, after 1-sec pulse of RTA at 700°C for nucleation, and grain-growth of PZT after 1 and 2 hrs in 550°C. (b) Grain-growth in SNLC method as a function of furnace annealing time and temperature. (c) Distribution of SNLC-PZT grain size after various annealing temperatures at 2 hrs fixed time. (d) The schematic energy diagram for the SNLC nucleation and growth mechanism.
perovskite interface-energy. When the grain size becomes large enough, the interface energy dominates the internal energy. The results in a self-limiting behavior which is consistent with grain saturation at a certain annealing time. Otherwise, increasing the annealing temperature enlarges the internal energy which means it has no choice but to generate nucleation sites in order to balance thermodynamic equilibrium condition.

Integration of SNLC-PZT into Si FET. In order to fabricate a FeFET with SNLC-PZT, the fabrication procedure begins with forming a 400-nm depth of SiO₂ shallow-trench-isolation (STI) on (100) oriented p-type Si wafer (Fig. 3a). Then, a 2-nm thick ZrTiO₄ was deposited by RF magnetron sputtering for the inter-diffusion barrier to prevent the reaction of PZT and Si. The quality of ZrTiO₄ is significantly important to obtain a clear, smooth, low-grain boundary density and crack-free film. In addition, the formation of ZrTiO₄ is not considered as the intermediate phase of PZT. There were no typical peaks observed by the XRD 2-theta profiles. Then, a 200-nm thick amorphous-PZT was sequentially deposited by RF magnetron sputtering using a single-composite target of Pb(Zr₀.₅₂Ti₀.₄₈)O₃ at 200 °C using O₂:Ar = 1:1. Next, the 50-nm thick Pt-seed array was formed by 5 μm off-set from the Si active region (Fig. 3b). The samples were annealed by 1-sec pulse of RTA at 700 °C in air ambient in order to form an artificial PZT-seed underneath the Pt-seed (Fig. 3c). Next, the samples were annealed at 550 °C by tube-furnace in ambient for 2 hrs in order to cover the Si active layer. According to the Fig. 2b, the grain size is 30 μm which is enough to fabricate a single FeFET structure within the grain. After the grain growth, a 200-nm thick Pt was deposited for gate electrode and completion of MFIS capacitor (Fig. 3d). Then, the Pt/PZT/ZrTiO₄ was etched away for self-aligned PH₃ doping to form source and drain (Fig. 3e). The phosphorous ions were implanted at 15 keV of accelerating voltages and RF power of 150 W at room temperature (Fig. 3f). Afterward, a 500-nm thick SiO₂ passivation layer was deposited and open for 500-nm thick Al contacts in gate, source and drain (Fig. 3g). All of the device dimension were measured at W/L = 3.5/2 μm.

Electrical and Endurance Characteristics. The hysteretic transfer (Iₜ - Vₜ) characteristics of the SNLC-PZT FeFET were investigated at 0.1 V of drain voltage with W/L = 20/5 μm (Fig. 4a). For the program and erase operation, the device was pulsed for 500 nsec at ±6 V, which is ultra-fast for that low an operating voltage, the best reported thus far. It shows a large threshold voltage (Vth) shift (~2.15 V) from the lower and upper curve. The lower and upper curve defined the erase (“0” state) and program state (“1” state). In addition, the Vth is defined as the gate voltage at which the drain current reaches 10 nA x W/L at drain voltage of 0.1 V. It is important to obtain a large Vth shift in order to sense a clear distinguished “0” and “1” state. These shifts in turn-on gate voltage of the FeFET are originated from the polarization of PZT. In the view point of the transistor, excellent electrical properties were also successfully confirmed. Field-effect mobility (μₑ) can be determined by applying the simplified equation below the low drain voltage, which belongs to the linear regime in the transfer characteristics:

$$\mu_e = \frac{L}{W} \frac{g_m}{C_{ox} V_d} \left. \frac{\partial I_d}{\partial V_g} \right|_{V_g=0.1V}$$  \hspace{1cm} (1)

where C_{ox} and g_m correspond to the gate oxide (PZT + ZrTiO₄) capacitance per unit area and transconductance extracted from the variation of drain current and gate voltage. The obtained μₑ was approximately 350 cm²/V/sec. Other important parameters of subthreshold slope (SS) and the Iₜ/Iₜoff ratio were 75 mV/dec and 1.4 x 10⁸ in both...
“0” and “1” states. These characteristics showed that the SNLC-PZT FeFET has excellent performances that have not been reported so far, and they are concluded to result from the single-grain PZT. To characterize the endurance performance, the gate voltage was pulsed at \( \pm 6 \) V in 1 MHz of frequency. After the various fatigue cycles, the hysteresis transfer curves have been maintained even after \( 10^{11} \) cycles (Fig. 4b). There was no degradation in the memory window, but also no degradation in the transistor properties, such as \( I_{on}/I_{off} \) ratio, SS, and \( \mu_{fe} \). In particularly, the SS is related to the charge-trapping in the interface of ZrTiO\(_4\)/Si and can be expressed as follow:

\[
\Delta SS = \ln 10 \frac{kT}{q} \left( \frac{\Delta C_{it}}{C_{ox}} \right)
\]

where the \( kT/q \) is the Boltzmann constant and \( \Delta C_{it} \) is the capacitance originated from the generation of interface traps. The interfacial defects can be roughly estimated by \( \Delta C_{it} = qD_{it} \). In our SNLC-PZT, there was no SS change even after \( 10^{11} \) cycles. These excellent results are the result of the smooth interface which avoids small undesirable charge-trappings in the PZT layer. With regard to the current CT flash memory, its maximum fatigue cycle was \( 10^6 \) with a 10-V high operating voltage. Moreover, it is reported that the poly-grain PZT shows \( 10^6 \) of maximum fatigue cycles\(^{1-6,35}\). In statistical view, the \( V_{th} \) distribution was shown in order to verify in VLSI memory (Fig. 4c). The average \( V_{th} \) of “0” and “1” state in initial state were 0.79 and 2.17 V and the standard deviations of “0” and “1” state in initial state cycles were 0.19 and 0.18. After \( 10^{11} \) cycles of fatigue, the average of \( V_{th} \) in “1” state slightly shift (less than 1%) to the positive gate voltage without a change in standard deviation. To evaluate the P/E speed, the \( V_{th} \) was measured under various pulses at 6 V for erasing and \(-6\) V for programming (Fig. 4d). The programming speed and erasing speed showed a saturation of \( V_{th} \) about \( 5 \times 10^{-7} \) sec at 6 V of operating voltage. It is reported that the switching speed of a FeFET is determined by the polarization speed which is observed in a nanosecond whereas the CT flash memory speed is determined by the quantum tunneling phenomenon which is observed in a microsecond\(^{1-6}\). Moreover, the switching speed of the FeFET on a single-grain of PZT was not changed even after \( 10^{11} \) of fatigue cycles. These excellent results are not easily overserved in current CT flash memory. Unlike the CT flash memory, it is reported that the switching kinetics are typically related to the polarization characteristics\(^{17,37}\):

\[
\Delta V_{th} \approx 2E_c t_f \approx 2V_c
\]

where \( E_c \) is the coercive field, \( V_c \) is the coercive voltage and \( t_f \) is the thickness of the ferroelectric thin-film. According to the equation, PZT requires a large \( E_c \) to achieve a large \( V_{th} \) shift because the physical height of gate-stack is fixed. It was found that the \( V_c \) is 1.05 and it was slightly reduced to 0.98 after the \( 10^{11} \) cycle of fatigue test (Fig. 4e). However it did not affect the \( I_{on} - V_{th} \) hysteresis. In the polarization curve, the SNLC-PZT showed a 25 \( \mu \)C/cm\(^2\) of large polarization remnant field (\( P_r \)) which is comparable with the epitaxial-grown PZT (20–50 \( \mu \)C/cm\(^2\))\(^{38,39}\). The reliable switching properties are affected by the quality of ferroelectric thin-film. It is reported that the electric-field induced oxygen vacancies are likely to migrate toward the near metal electrodes or grain boundaries in high defect density PZT\(^{40,41}\). However, these results are still controversial because the perovskite-structures...
could not afford large point defects. Instead, the perovskite lattice is collapse with shear vector of \(111/2\) and eventually forms a Ruddlesden-Popper stacking fault lattices \(^{42}\). Fortunately, the stacking fault observation is not observed in the single or high-quality perovskite-thin-films. It can be concluded that the SNLC-PZT showed a strong immune to the fatigue cycles.

Retention Characteristics. In general, the FeFET with MFIS capacitor has a short retention time comparing to CT flash memory. The short retention time in FeFET are attributed by two major problems \(^{43,44}\): 1) generation of self-depolarization field \((E_{de})\) and 2) high gate leakage conduction. These properties are influenced by the quality of ferroelectric and buffer insulator thin-film. Considering the metal-ferroelectric-metal (MFM) structured capacitor, the generation of \(E_{de}\) is effectively suppressed by the compensating charge presented on both sides of metals. In fact, there are some generations of \(E_{de}\) even in the MFM capacitor because the metallic impurities and oxygen vacancies can be lose compensated charges near the electrode. Some of the research groups attempt to insert conductive metal-oxides for inter-diffusion barriers, such as \(IrO_2^{45,46}\) and \(RuO_2^{47,48}\). On the other hand, for the FeFET with MFIS structures, the \(E_{de}\) always exists due to the finite semiconductor and buffer insulator. Figure 5 shows the equivalent circuits of MFIS in series with ferroelectric \((C_{FE})\), buffer insulator \((C_i)\), and semiconductor capacitance \((C_s)\). When a gate voltage induces a polarization in ferroelectric thin-film, the charge is balanced as:

\[
V_{FE} = \frac{C_i V}{C_i + C_{FE}} - \frac{P}{C_i + C_{FE}} \tag{4}
\]

where the \(V_{FE}\) is the voltage drop at the ferroelectric thin-film. When \(V_{FE}\) is zero-bias, it is rewritten as:

\[
V = V_{FE} + V_j = \frac{Q_{FE} - P}{C_{FE}} + \frac{Q_j}{C_i} = 0 \tag{5}
\]

From this result, the ferroelectric charges can be expressed as:

\[
Q_{FE} = P \frac{C_i}{C_i + C_{FE}} \tag{6}
\]

This can lead the \(E_{de}\), as:

\[
E_{de} = \frac{P}{\varepsilon_{FE} C_i + C_{FE}} = \frac{P}{\varepsilon_{FE} \left( \frac{1}{C_i/C_{FE} + 1} \right)} \tag{7}
\]

where \(\varepsilon_{FE}\) is the dielectric constant of the ferroelectric thin-film. According to equation (7), there is always a finite depolarization field as long as the \(C_i\) is not infinity. Thus, it is important to develop a high dielectric constant for buffer insulator for low \(E_{de}\). Recently, the \(HfO_2\) \((\varepsilon_r \sim 20)\) buffer layers were demonstrated in the MFIS structured FeFET. Ishiwara reported that the \(Hf\) based oxides, such as \(HfO_2\) and \(HTaO\) buffer layer can improve the retention time up to several days \(^{49,50}\). In addition, other groups attempt to use relatively low dielectric constant ferroelectric thin-films, such as \(SrBi_2Ta_2O_9\) \((\varepsilon_r \sim 50)\) \(^{51}\) and polyvinylidenefluoride (PVDF) polymer \((\varepsilon_r \sim 8.4)\) \(^{52}\). However, it still needs to considerable improvements of retention time with high dielectric constant ferroelectric thin-film. In our SNLC-PZT FeFET, both \(ZrTiO_4\) \((\varepsilon_r \sim 50)\) and the SNLC-PZT showed \((\varepsilon_r \sim 1000)\) showed high dielectric constants.

The transfer characteristics as a function of data retention time are shown in Fig. 6a. The \(P/E\) operation was the same as the fatigue test and the data were measured until 1 month (=31 days). The “0” and “1” states were pulse for 500 nsec at \(\pm 6\) V. Only a parallel \(V_{th}\) shift was observed without any changes in the transistor properties. After 1 month of waiting time, the \(V_{th}\) shift only degraded 11%, which is a record in PZT based FeFET. There was no degradation until 15 days and the window started to slightly decrease after 15 days (Fig. 6b). After 10-years later, 25% of \(V_{th}\) is expected by the extrapolation. In statistical view, the \(V_{th}\) distribution was shown in Fig. 6c. The average \(V_{th}\) of “0” and “1” state in initial state were 0.79 and 2.1 V and the standard deviations of “0” and “1” state.
in initial state cycles were 0.17 and 0.18. After 1 month of awaiting time, the average of \( V_{th} \) in “1” state slightly shift (~11%) to the negative gate voltage. Although the retention time is the highly recorded FeFET, it still needs large improvements to be comparable with the current CT flash memory. Another major cause of the short retention time is the gate leakage conduction and charge trapping of electron carriers in the interfaces of gate oxide. When the FeFET is programmed, the polarization induces an inversion layer in the p-type Si. However, these induced electrons are easily attracted from the gate electrode and semiconductor sides. This injected electrons leads to local charge compensation and gradually diminished the effect of polarization. Thus, there is a trade-off between the thick and thin buffer insulator layer. A thick insulator layer could efficiently suppress the gate leakage conduction; however the generation of \( E_{0} \) is appeared by the increased \( C_{t} \). It is important to balance the buffer insulator thickness. In addition, the quality of ferroelectric layer strongly affects the gate current density. In terms of grain boundary, it is observed that gate leakage current density of polycrystalline-PZT (poly-PZT) is one order of magnitude higher than the SNLC-PZT (Fig. 7a). Moreover, the gate current conduction of poly-PZT is dramatically increased from \( 10^{-8} \) to \( 10^{-1} \) A/cm² after \( 10^{11} \) of fatigue cycles. On the other hand, there was almost no increase in the SNLC-PZT. It is well known that oxide leakage conduction shows an interface-limited Schottky emission in low bias region and bulk-limited space-charge-limited conduction (SCLC) or Poole-Frenkel emission current in high bias region. In addition, it should be noted that the SCLC is not related whether the contact is depletion or accumulation type. The injection charges are trapped into the insulator and form space-charge distribution. In the SNLC-PZT, the gate current density conduction only shows an Ohmic-like conduction (slope 1.5) extracted from the \( \log(V) \) and \( \log(I_G) \) (Fig. 7b). On the other hand, the slope of poly-PZT showed 2, which considers to fit in a single trap.
| Condition | Si3N4 | Dy2O3 | Y2O3 | HfO2 | HfTaO | ZrTiO4 |
|-----------|-------|-------|------|------|-------|-------|
| Gate Leakage Conduction | NA | 5 | 8 | 8 | 5 | 10 |
| Program/Erase Speed | 10 nsec | NA | NA | NA | NA | 500 nsec |
| Retention Time (loss%/Time) | Loss 39%/3-Days | Loss 30%/10^5 sec | Loss 11.5%/10^5 sec | Loss 34%/1 Month | Loss 10%/1 Month | Loss 11%/1 Month |
| Fatigue Test (loss%/Cycle) | Loss 1%/10^11 cycles |Loss 1%/10^11 cycles |Loss 1%/10^11 cycles | Loss 1%/10^11 cycles | Loss 1%/10^11 cycles | Loss 1%/10^11 cycles |

Table 1. Progress of FeFET with MFIS Structure.

\[ I_d = \frac{9 \mu_{FET} V^2}{8 d} \] (8)

After filling the single-trap, it begins to fill a large number of multi-level trap distributions in the ZTO. Thus the slope is increased to 7 and 12 at high bias regime. To understand the grain-boundary effect in MFIS capacitor, Fig. 7c shows a schematic energy diagram showing the entire possible damage and conduction path in poly-PZT. The induced electrons can damage the interface of ZrTiO4/Si which may contribute to the leakage path toward the PZT. Once the electrons flow to the ZrTiO4, it is accumulated in the interface of PZT/ZrTiO4. Afterward, the electrons fill the multi-traps in PZT, which leads to the high SCLC slope.

**Progress of FeFET.** Most of the extensive researches of FeFET are focused on the finding a suitable high-k insulator for buffer layers without improving the quality of ferroelectric thin-film in order to achieve a long retention and good endurance characteristics50,57–60. In addition, some of the researchers have successfully achieved a high quality ferroelectric thin-film by using atomic-layer deposition; however its high cost and low reproducibility cannot be a solution in the mass-product industry. Here, the SNLC technology is the possible solution to minimize the effects of both Egd and gate leakage density conduction by simply achieving an epitaxial-like PZT. The performances of state-of-the-art FeFET are summarized in Table 1. Comparing with the current CT flash memory, the tunnel oxide thickness must be thicker than 7-nm to ensure low gate leakage conduction to realize a 10-year retention time. Generally speaking, most of the ferroelectric thin-films are over 100-nm because a “dead layer” is generally observed in ultra-thin-film ferroelectrics60. Thus, it is important to develop a novel processing method for high quality ferroelectric.

**Conclusion**

We have made a progress of integrating an epitaxial-like PZT thin-film into Si for nonvolatile FeFETs. Dividing the nucleation and grain-growth mechanisms, it is possible to obtain uniform and large rectangular-shaped grains, large enough to fabricate a transistor with a single-grain PZT thin-film. Surprisingly, the fabricated FeFET showed a Vth shift (2.2 V), low operation voltage (6V), and an ultra-fast P/E speed (5 \times 10^{-7} sec). Moreover, the there was no degradation after 10^{15} cycles of bipolar fatigue testing and the sample even showed a long retention time after 1 year. All of these characteristics correspond to the best performance among all types of ferroelectric field-effect transistors reported thus far.

**Experimental Methods**

**Device Fabrication.** The fabrication process for a FeFET with epitaxial-like single-grain PZT was started by forming a 400-nm deep shallow isolation trench, by inductively coupled plasma etching (Oxford Instruments, ICP 380) and depositing 400-nm SiO2 for filling the trench by plasma-enhanced chemical vapor deposition (Unaxis, VL-LA-PECVD). Then, a 2-nm thick ZTO layer for inter-diffusion barrier was deposited using an RF magnetron sputtering system (Vacuum Science, 2-inch 3-Gun) and a single composite target (purity 99.999%) at 200°C with O2:Ar = 1:2. Next, a 200-nm thick amorphous-phase PZT was consecutively deposited by RF magnetron sputtering (Vacuum Science, 2-inch 3-Gun) using a single composite target (purity 99.999%) of PbZr0.52Ti0.48O3 at 200°C with O2:Ar = 1:2. Next, a 50-nm thick Pt dot matrix was formed by depositing the Pt with a DC magnetron sputtering system (Vacuum Science, 2-inch mini-chamber) at room temperature and patterning the Pt with photolithography (Karl SUSS, MA-1006). The samples were annealed with a 1-sec pulsed Xe flash lamp at 650°C in ambient air, for generating artificial nucleation seeds underneath the Pt dots. Then the samples were post-annealed for 2 hrs in a horizontal tube-furnace at 550°C in air ambient for the grain growth. Then, a 200-nm thick Pt was deposited to form a gate electrode, by using a DC magnetron sputtering system (Vacuum Science, 2-inch mini-chamber) at room temperature and it was patterned by wet-etching. The source and drain were formed by ion implantation using PH3 (99% diluted in H2) plasma with 15 keV of accelerating voltage and 150 W of RF power. The dopants were electrically activated by 2 hrs of annealing at 500°C. Afterward, a 500-nm thick SiO2 was deposited by plasma-enhanced chemical vapor deposition and opened for 500-nm thick Al metallization contacts.
Measurement. The measurements for electrical properties and capacitance properties were carried out by E3270B semiconductor analyzer (Agilent Technologies) and 4284A precision LCR meter (Agilent Technologies, Inc.). In addition, the polarization measurements were performed by RT66A (Radiant Technologies, Inc.).

Characterization. The crystal orientations were measured by XRD (PANalytical, X’pert Pro). The cross-sectional image was observed by high-resolution transmission electron microscopic image (JEOL, JEM-2100F).

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Author Contributions

J.H.P. and S.K.J. conceived and designed the experiments. J.H.P., G.S.J., K.H.S., H.J.C., S.K.L. and Z.K. performed the fabrication. J.H.P. analyzed the performance and H.Y.K. analyzed the material characteristics. J.H.P. and S.K.J. interpreted the data and provided fruitful discussion all the coauthors.

Additional Information

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Retraction: Integrating Epitaxial-Like Pb(Zr,Ti)O₃ Thin-Film into Silicon for Next-Generation Ferroelectric Field-Effect Transistor

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This Article has been retracted by the authors. The data presented in Figures 1e, 1g, 1h, 2b-d, 4a-b, 4d-e, 6a-b and 7a-b were manipulated and are duplicated in other papers1–5.

All authors acknowledge these issues and agree to the retraction of the Article.

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