Abstract—This paper presents a wireless neural recording system featuring energy-efficient data compression and encryption. An ultra-high efficiency is achieved by leveraging compressed sensing (CS) for simultaneous data compression and encryption. CS enables sub-Nyquist sampling of neural signals by taking advantage of its intrinsic sparsity. It simultaneously encrypts the data with the sampling matrix being the cryptographic key. To share the key over an insecure wireless channel, we implement an elliptic-curve cryptography (ECC) based key exchanging protocol. The CS operation is executed in a custom-designed IC fabricated in 180nm CMOS technology. Mixed-signal circuits are designed to optimize the power efficiency of the matrix-vector multiplication (MVM) of the CS operation. The ECC algorithm is implemented in a low-power Cortex-M0 microcontroller (MCU). To be protected from timing and power analysis attacks, the implementation avoids possible data-dependent branches and also employs a randomized ECC initialization. At a compression ratio of 8x, the average correlated coefficient between the reconstructed signals and the uncompressed signals is 0.973, while the ciphertext-only attacks (CoA) achieve no better than 0.054 over 200,000 attacks. The prototype achieves a 35x power saving compared with conventional implementation in low-power MCUs. This work demonstrates a promising solution for future chronic neural recording systems with requirements in high energy efficiency and security.

Index Terms—Neural recording, compressed sensing, hardware security, cryptographic circuits, low power, mixed-signal IC.

I. INTRODUCTION

Large-scale neural recording with high energy efficiency and safety is crucial to the growing number of therapies employing closed-loop neurostimulation and neuroprosthetics to treat brain injury and disease [1]. Although the research community has devoted a considerable amount of effort to improve the performance and power efficiency of neural recorders, few investigations have been done to mitigate the security risks. In fact, cybersecurity issues have already emerged in FDA-approved medical devices [2]. Medical devices, including neural interfacing devices, pose serious risks from malicious attacks. Compromised neural interfacing devices may not only disclose critical health-related information, but also leave the users vulnerable to life-threatening attacks. Thus, it is urgent to investigate secure neurotechnologies.

Battery-powered wireless neural recording devices are especially vulnerable to malicious attacks, and their restrained energy budget imposes a significant challenge to implementing data encryption. In this work, we propose a framework that achieves ultra-high energy efficiency by leveraging the compressed sensing (CS) technique for joint neural signal compression and encryption, as illustrated in Fig. 1. The key concept of CS is that a sparse signal can be sampled at a reduced rate (below Nyquist frequency) based on the actual amount of information it contains [3]. Since the CS operation can be implemented in low-complexity hardware, it is especially attractive in low-power applications. Neural signals are proven to be sparse in certain domains (or pre-learned dictionaries) [4]. Recent studies have successfully demonstrated highly efficient CS-based neural recorders [5]-[10]. Moreover, CS theory also permits its application in data encryption [11]. It has been proven that CS can provide a computational guarantee of secrecy, provided that an adversary doesn’t know the sampling matrix [12]. Recently, several works have explored this property in image processing [13], [14] and internet of things (IoT) applications [15], [16]. We present in this paper, to the best of our knowledge, the first implementation in neural recording systems.

To implement CS-based encryption in a neural recording system, several challenges must be addressed. First, the sampling matrix (i.e. the cryptographic key) must be safely exchanged between the neural recorder and authorized external system. Secondly, mechanisms must be introduced to protect the energy features of the neural signals from being leaked. Thirdly, the hardware implementation must be protected from side-channel attacks, such as timing and power analysis attacks [17], [18]. Last but not least, the overall encryption cannot lead to a significant power penalty. To conquer these challenges, we propose a novel system that combines an ASIC for ultra-low power CS operations, and a general-purpose microcontroller (MCU) for low duty-cycle key establishment.

The paper is structured as follows. Section II describes the operating principles of the proposed system. Section III presents the implementation details. Section IV shows the experimental results. Finally, Section V concludes the paper.

Fig. 1. Illustration of the proposed neural recorder with CS and encryption.

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Digital Object Identifier

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II. OPERATING PRINCIPLES

A. CS for Joint Signal Compression & Encryption

Suppose the targeting signal $x$ has a sparse representation $s$ on a certain basis $\Psi$. CS theory predicts that $x$ can be sampled at a reduced rate (depending on its sparsity) with nearly no information loss. This compressed sampling process can be expressed as a simple linear projection, given by:

$$y = \Phi x$$

where $x \in \mathbb{R}^{N \times 1}$, $y \in \mathbb{R}^{M \times 1}$, and $\Phi \in \mathbb{R}^{M \times N}$. Note that $N > M$, and the term $N/M$ is referred to as compression ratio (CR). Although $y$ cannot be solved directly from Eq. (1), if the sampling matrix $\Phi$ is incoherent with $\Psi$ (obeying the restricted isometry property (RIP) [19, 21]), then the sparse representation $s$, thus the original signal $x$, can be solved as a convex optimization problem [20]:

$$\min ||s||_0 \text{ (or 1)} \quad \text{s.t.} \quad y = \Phi x = \Phi \Psi^{-1}s$$

It has been proven that a random matrix $\Phi$ with a Gaussian probability density distribution is sufficient in fulfilling the incoherent requirement [20].

The secrecy property of CS has also been rigorously discussed in the literature [11, 12, 22, 23]. Although achieving Shannon’s perfect secrecy is conditional [23], computational secrecy can be guaranteed [11]. Encryption algorithms with computational secrecy are commonly adopted in cryptography standards, given that extracting information without the key is a nondeterministic polynomial time problem (NP-problem) [12, 22]. However, since the CS projection is linear, the energy of $x$ can be revealed in $y$ without an accurate decipher. Unfortunately, the energy feature of neural signals can contain private information [24]. This information may be leaked if no additional protection is used.

To mitigate this risk, Chen and colleagues proposed a method of inserting watermarks to mask the energy features [16]. Cambareri and colleagues proposed a multiclass encrypting scheme [25]. In our application of neural recording, we hope not to degrade the reconstructed signal quality, or significantly increase the hardware complexity. Thus, we propose a pseudo-random key shuffle as well as a synchronized key updating for disturbing the energy features. The power penalty of this scheme is negligible for the overall system due to its low active duty cycle.

B. Elliptic-Curve Cryptography and Key Exchanging

There are two mainstream encryption schemes: symmetric encryption and asymmetric encryption [26]. Although asymmetric encryption algorithms have the advantages of stronger security, they often come at a higher computational cost than symmetric encryption algorithms. As a result, asymmetric encryption is often used to share the key for symmetric encryption. This work adopts a similar strategy. CS is a symmetric encryption strategy, given that the key (the sampling matrix) is used in both ciphering and deciphering the messages. We share the key using an asymmetric encryption scheme.

This work adopts an ECC based key exchanging protocol, namely Elliptic-curve Diffie-Hellman (ECDH) [27]. ECDH is an ECC variant of the Diffie-Hellman protocol. ECDH allows two parties to establish a shared secret key independently. The shared secret key can then be used directly or for deriving other keys, which in our case are the sampling matrices.

C. Framework of the Proposed Hybrid Encryption

In a common scenario of neural signal transmission, the neural recorder (the conventional character Alice) sends the sampled data to the authorized external system (Bob) via an insecure wireless channel. Illegitimate parties (Eve) may steal the messages by eavesdropping. Here we consider the context where Eve knows the communication protocol, the encryption algorithms as well as the public keys, but doesn’t have access to the private keys (CS sampling matrices).

The operation principle of the proposed cryptographic neural recording system is as follows:

1) Alice and Bob first agree on a set of domain parameters (public) for the cryptography, including the parameters of the elliptic curve, the generator point $G$, etc.;
2) Alice picks a private key $K_A$, and generates a public key $K_A = K_\alpha \circ G$, where $\circ$ is a multiplication defined by ECC; Similarly, Bob picks a private key $K_B$ and generates a public key $K_B = K_\beta \circ G$;
3) Alice and Bob exchange their public keys $K_A$ and $K_B$;
4) Alice and Bob generate a shared secret key $K_s$ using their private keys and the public keys:

$$K_s = K_A \circ K_B = (K_\alpha \circ G) \circ K_\beta \quad (\leftarrow Bob) \quad (3)$$

$$K_s = K_\alpha \circ (G \circ K_\beta) = K_\alpha \circ K_B \quad (\leftarrow Alice) \quad (4)$$

5) Alice and Bob individually generate a set of sampling matrices $\Psi_S$ using the secret key $K_s$;
6) Alice performs CS on acquired neural signal $x$, and sends the lower-dimensional measurement $y$ to Bob;
7) Bob recovers the neural signal $x$ from $y$ by solving optimization problem using $\Phi_S$;
8) Alice and Bob shuffle the $\Phi_S$ according to a pre-agreed protocol, and then repeat the CS encryption;
9) To prevent from using the same set of $\Phi_S$ repeatedly, Alice and Bob would update the $K_S$ (thus the sampling matrix $\Phi_S$) periodically on a synchronized manner.

III. SYSTEM IMPLEMENTATION

The high-level block diagram of the proposed neural recorder (Alice) is shown in Fig. 2. The system consists of an ultra-low power ASIC and a general-purpose Cortex-M0 MCU. The ASIC integrates low-noise neural amplifiers, a mixed-signal CS core, an ultra-low power backscattering transmitter, and peripheral circuits. A computer interfacing device (Bob) has been designed for reading back the data from the neural recorder. A standard USB 2.0 port is integrated for high-speed communication with the computer system. This design reuses aspects of our previous work [28, 29].

A. Mixed-Signal CS Core Design

The CS measurement is implemented using mixed-signal circuits. The execution of the matrix-vector multiplication
Hardware cost is the ACRs. After the MAC operations finished greatly simplified by the analog multiplication. The primary power saving during sleep. The digital operations have been the input buffer and comparator will be gated with the PGA for the SAR ADC mainly scales with the sampling rate, whereas different PGA gain configurations. The power consumption of the ADC samples four times during one input period with the results in the corresponding result registers. The digital operations include logical bit shifting and complement.

A programmable gain amplifier (PGA) provides a gain of using a combination of analog and digital processing circuits. Amplified analog signal is fed into the CS core, and multiplication is implemented as a result of arithmetic simplification and memory access reduction. Since MVM requires repeated MAC operations, improving its energy efficiency is critical. This work adopts a resolution reduction scheme for reducing computational costs and power consumption. We choose to use 4-bit $\Phi$s with elements of $\{0, \pm 1/8, \pm 2/8, \pm 3/8, \pm 4/8, \pm 5/8, \pm 6/8, \pm 7/8\}$. Fig. 3(b) shows the block diagram of the mixed-signal CS core. Amplified analog signal $x$ is fed into the CS core, and multiplication is implemented using a combination of analog and digital processing circuits. A programmable gain amplifier (PGA) provides a gain of $\times 4, \times 5, \times 6,$ or $\times 7$. An ADC samples the amplified data and saves the results in the corresponding result registers. The digital operations include logical bit shifting and complement.

Fig. 3(c) shows the timing diagram of the CS operation. The ADC samples four times during one input period with different PGA gain configurations. The power consumption of the SAR ADC mainly scales with the sampling rate, whereas the input buffer and comparator will be gated with the PGA for power saving during sleep. The digital operations have been greatly simplified by the analog multiplication. The primary hardware cost is the ACRs. After the MAC operations finished after $N$ sampling periods, a parallel to serial converter (P2S) shifts the measurement $y$ out for wireless transmission.

### B. Implementation of the ECDH protocol

As discussed in Section II-B, ECC based algorithms have advantages over conventional asymmetric cryptography algorithms in terms of speed, security level (given a key length), as well as the corresponding computational cost. These features make it attractive for both security-critical applications and resource-constrained applications, including medical devices.

Among established elliptic curves, we choose Curve25519 for our application, because of its low requirements in memory and computational resources. Curve25519 and the corresponding Diffie-Hellman functions were originally proposed by Daniel Bernstein in 2006 [27]. The function is a field-restricted scalar multiplication on an elliptic curve $E$:

$$y^2 = x^3 + 486662x^2 + x \quad (x, y) \in \mathbb{F}_p^2$$

where $p$ is $2^{255} - 19$. When a point $P$ (on the curve $E$) multiplies a scalar $S$, it adds to itself ($S$-1) times to a point $Q$, which remains on the curve $E$ (the set forms an abelian group). The computation only uses the $x$-coordinate, thus is often called $x$-coordinate scalar multiplication. The $x$-coordinate scalar multiplication is repeated twice (on each party) during the ECDH protocol, for generating the public key and the shared secret key, respectively.

In this work, we adopt a 256-bit key using a radix $2^{32}$ representation for the code implementation. The $x$-coordinate scalar multiplication can be efficiently computed using the classic Montgomery ladder [30]. Algorithm 1 describes the operation in pseudo-codes. Each Ladderstep performs one differential addition and one doubling [31].

### Algorithm 1 Scalar Multiply, (Original)

#### Inputs: $P$ (a point on the curve $E$), $S$ (a scalar)

#### Output: $Q$ (a point on the curve $E$)

1. $Q \leftarrow$ Initial point
2. for each bit $b$ of $S$ (254 downto 0) do
3. if $b$ is 1 then
4. swap the values of $P$ and $Q$
5. end if
6. $(P, Q) \leftarrow$ Ladderstep($P, Q$)
7. if $b$ is 1 then
8. swap the values of $P$ and $Q$
9. end if
10. end for

### Algorithm 2 Scalar Multiply, (Time-Constant Implementation)

#### Inputs: $P$ (a point on the curve $E$), $S$ (a scalar)

#### Output: $Q$ (a point on the curve $E$)

1. $Q \leftarrow$ Initial point
2. for each bit $b$ of $S$ (254 downto 0) do
3. if $b$ is 0 then
4. $(P, Q) \leftarrow$ Ladderstep($P, Q$)
5. else
6. $(P, Q) \leftarrow$ Ladderstep($P, Q$)
7. end if
8. end for

To make the implementation immune to timing attacks, all input-dependent branches or operations should be avoided. In this work, we modify the Ladderstep function into two identical timing functions Ladderstep0 and Ladderstep1, which will be executed depending on the loop’s variable bit $b$, as described in Algorithm 2. In addition, the initial coordinates are randomly projected in each execution according to [17] to protect the implementation from differential power attacks.

The 256-bit multiplication and squaring are the most computationally intensive operations. The 256-bit multiplication is implemented as a three-level Karatsuba multiplication with time-constant implementation [32]. Squaring operations use the same Karatsuba algorithm with a faster computing speed as a result of arithmetic simplification and memory access reduction [33].
IV. EXPERIMENTAL RESULTS

The ASIC was fabricated in 180nm CMOS technology. The system was assembled on a 4-layer printed circuit board (PCB). The main PCB contained the ASIC and a microconnector for pairing with recording electrodes. The MCU and the 2.4GHz RF transceiver were assembled on an extension PCB. The device was powered by a 3.7V lithium battery.

The CS function was tested with pre-recorded intracranial EEG signals of epilepsy patients [34]. Seizure onset times have been labeled by experts. The original data was digitized at 12 bits with a sampling rate of 250Hz, and was synthesized by an arbitrary function generator. Fig. 5 shows the experimental results. The reconstructed signals from 4x and 8x compression are plotted in comparison with the original uncompressed signal. The time-domain waveforms are shown in Fig. 5 (a), and the spectrograms of a continuous recording of 7.5 hours are shown in Fig. 5 (b). The reconstructed signals achieved a high PSNR of 32.75dB.

The neural recording system was tested under mock attacks. We primarily consider a ciphertext-only attack (CoA) model, where the attacker (Eve) has access to the ciphered texts, the encryption algorithms and public domain parameters. Fig. 6 shows the results of a total of 200,000 CoA attacks. For each data segment, Bob had one reconstruction using the genuine key, while Eve made 1000 attempts using randomly generated keys. Here we assumed Eve had prior knowledge of the signals’ characteristics, thus Eve used the same basis \( \Psi \) for the signal reconstruction. Fig. 6 (a) shows the Pearson correlation coefficients \( \rho \) (the higher the better) between Bob’s and Eve’s reconstructed signals and the original signals. The \( \rho \) of Eve’s reconstructions are within a random noise level. Fig. 6 (b) is the scatter graph with x-coordinate being the \( \rho \) of Bob’s reconstruction and y-coordinate being the \( \rho \) of Eve’s best shot. Note that Eve doesn’t know which one is the best shot since Eve doesn’t possess the ground truth. The circled red dots highlight the trails where the performance of Eve’s best attack was closest to Bob’s reconstruction. The corresponding waveforms are plotted Fig. 6 (c). Eve’s reconstruction doesn’t reveal meaningful information about the neural signals. The results suggest that the system is safe from CoA attacks.

As discussed in Section II-A, the CS-based encryption cannot prevent the energy of the signal, and potentially private information, from being revealed. Each marker in Fig. 7 indicates a data segment with x-coordinate being the energy of the signal \( x \) and y-coordinate being the energy of the CS measurement \( y \) (without decipher). The plots in the left column use the same key for CS all measurements. The results show that seizure events can be classified using only the
achieved an over 35x power-saving comparing with systems. Less neural interfaces become more prevalent in the treatment work will be increasingly needed as therapies involving wire-over time. The framework and techniques introduced in this from malicious attacks while maintaining an ultra-low power cryption. Novel techniques are proposed to minimize the risks CR of 8x was 442
The resulting power consumption with a corresponding to a 5.7x power saving. At last, the power consumption of the proposed operation with a CR of 8x was 442µW. In summary, the developed prototype achieved an over 35x power-saving comparing with systems using conventional encryptions.

V. Conclusion

This paper presents an energy-efficient wireless neural recording system with simultaneous data compression and encryption. Novel techniques are proposed to minimize the risks from malicious attacks while maintaining an ultra-low power consumption. Experimental results show that the developed system achieves a secure, reliable, energy-efficient recording over time. The framework and techniques introduced in this work will be increasingly needed as therapies involving wire-less neural interfaces become more prevalent in the treatment of neurological disorders.

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