Design Optimization of Nanotube Tunnel Field-Effect Transistor with Bias-Induced Electron-Hole Bilayer

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Abstract
In this paper, a novel nanotube tunneling field-effect transistor (NT-TFET) with bias-induced electron-hole bilayer (EHBN-TFET) is proposed for the first time. By the intentional misalignment and an asymmetric bias configuration of the inner-gate and outer-gate, the line tunneling takes place inside the channel, significantly improving the tunneling rate and area. The device principle and performance are investigated by calibrated 3-D TCAD simulations. Compared to the conventional NT-TFET, the proposed EHBN-TFET exhibits an increased ON-state current ($I_{ON}$) about 57.2 times and a sub-60 mV/dec subthreshold swing for seven orders of magnitude of drain current. Furthermore, the increased $I_{ON}$ and reduced gate capacitance achieve improved dynamic performance. Compared with conventional NT-TFET, the intrinsic delay decreased about 142 times is obtained in EHBN-TFET.

Keywords Band-to-band tunneling · nanotube · electron-hole bilayer · line tunneling · steep switching

1 Introduction

As feature size scales down constantly, conventional MOS-FETs have reached physical limitation. Power dissipation rises considerably due to the high-leakage current and unscalable supply voltage ($V_{DD}$) [1]. With the rising demand for mobile phones, lower power is becoming an important requirement and some novel devices have been proposed, such as negative capacitance field-effect transistor, impact ionization metal-oxide-semiconductor transistor and tunnel field-effect transistor [2–7]. The quantum tunneling in tunnel field-effect transistor (TFET) achieves an extremely-low OFF-state current ($I_{OFF}$) and a steep subthreshold slope (SS) below 60 mV/dec at room temperature [7], so that $V_{DD}$ could be further scaled down.

However, two major challenges restrict TFET in practical applications. The first one is the difficulty of achieving the highly doped source/channel junction with ultra-steep profile experimentally [8]. Though dopingless TFET provides a solution to avoid the high-temperature doping/annealing processes [9], the ON-state current ($I_{ON}$) degrades due to the existence of large barrier width between source and gate electrodes [10]. The second one is low $I_{ON}$, caused by poor band-to-band tunneling rate and the point tunneling mechanism. To improve $I_{ON}$ of TFET, several approaches have been proposed, such as low bandgap material engineering [11, 12], high-k gate dielectric engineering [13], source pocket engineering [14, 15] and line tunneling engineering [16–20]. Bias-induced electron-hole bilayer (EHB) concept was applied to double-gate TFET to induce line tunneling in the channel [17–19]. However, 2-D planar structure is difficult to achieve large $I_{ON}$ with small chip-area [20]. Besides, nanowire TFET (NW-TFET) also presents a great potential for performance enhancement because of the excellent electrostatic control. However, dynamic performance and power dissipation of NW-TFET are bound to be affected, when multiple nanowires are vertically stacked to increase the tunneling area. Compared to NW-TFET, nanotube TFET (NT-TFET) achieves similar electrostatic control by the inner/outer-gate, and offers larger tunneling area and current by hollowed cylindrical shaped nanotube structure [21–24]. However, NT-TFET still suffers from the two challenges mentioned above.
In this paper, a novel NT-TFET with a misaligned inner/outer-gate, named EHBNT-TFET, is proposed for the first time. With appropriate gate work-function and bias configuration, electron-hole bilayer is induced separately, forming an abrupt p⁺-n⁺ junction in the intrinsic channel. As a result, the highly doped source/channel junction with abrupt profile is not required in EHBNT-TFET. Using 3-D device simulation, the advantage of EHBNT-TFET is explored and demonstrated in detail. The line tunneling inside the channel dominates the current, instead of the point tunneling between source and channel. Compared to the conventional NT-TFET, \( I_{ON} \) of EHBNT-TFET is found to increase about 57.2 times and keep a high \( I_{ON}/I_{OFF} \) ratio of \( 1.94 \times 10^9 \). Furthermore, the impact of doping concentration, critical geometric parameters, gate work-function and bias are discussed, which benefits to adopt appropriate parameters to achieve excellent performance.

1.1 Device Structure and Simulation Methodology

3-D schematic view of conventional NT-TFET and proposed EHBNT-TFET are shown in Fig. 1(a) and (b), respectively, and the corresponding cross-sectional view along A-A’ cut-plane are presented in Fig. 1(c) and (d). Conventional NT-TFET has a symmetric inner/outer-gate with the same metal work-function, and generally the same bias is applied to the inner/outer-gate. The EHBNT-TFET presents an intentional misaligned inner/outer-gate. The inner-gate has a higher work-function, compared to the outer-gate. When a positive voltage is applied to the outer-gate and a negative voltage is applied to the inner-gate, a bias-induced electron-hole bilayer is formed in the thin silicon nanotube channel. Consequently, an abrupt p⁺-n⁺ junction is formed in the intrinsic channel. Then the line tunneling occurs between electron-hole bilayer, i.e., the overlapped region between the inner-gate and outer-gate. Furthermore, the underlap at the source and drain end could eliminate parasitic tunneling current in OFF-state. Referring to the fabrication of previous NT-TFET [24–27], a possible process flow for proposed EHBNT-TFET is presented in Fig. 2. The main difference in EHBNT-TFET is the formation of misaligned inner/outer-gate using different materials.

The simulations are performed using Sentaurus TCAD [28]. Besides the regular physical models, dynamic nonlocal path band-to-band tunneling (BTBT) and density gradient (DG) model are also activated. Dynamic BTBT adopts Wentzel-Kramers-Brillouin (WKB) approach to account for phonon-assisted tunneling process [29]. DG model is used to consider the quantum confinement effect. For the moment, trap-assisted tunneling process has not been considered in our simulations. The simulation environment is calibrated with the previous result of conventional NT-TFET under the same geometric parameters [24]. As shown in Fig. 3(a), the simulated transfer curve shows a good agreement with the data in [24]. For tunneling occurring at electron-hole bilayer, the correct computation of carrier density is critical. Therefore, DG model has been calibrated on the solution of the Poisson-Schrödinger equation with the structure in Fig. 1(c). Calibrated DG model parameters are given as follows: \( \gamma_n = 7, \gamma_p = 10.5, \eta_n = 1.02, \eta_p = 0.8, \theta_n = 0.91, \theta_p = 0.97 \). As shown in Fig. 3(b), charge distributions in the channel arising from calibrated density gradient model matches properly with Schrödinger results for EHBNT-TFET.

The key physical parameters of simulated NT-TFET and EHBNT-TFET are listed in Table 1. The intrinsic Si is adopted as the channel. To keep the same geometry, gate
The length of NT-TFET is 40 nm, while the overlap between inner/outer-gate of EHBNT-TFET is 20 nm, with a 10 nm underlap between inner-gate (outer-gate) and drain (source). The work-function of NT-TFET is tuned to obtain the same $I_{OFF}$ with EHBNT-TFET. By default, the applied voltage $V_{DD}$ is 0.5 V.
2 Results and Discussion

2.1 Characteristics of NT-TFET and EHBNT-TFET

Transfer characteristics for both NT-TFET and EHBNT-TFET are depicted in Fig. 4(a). For EHBNT-TFET, the outer-gate controls the switch between OFF-state and ON-state. Compared to the conventional NT-TFET, EHBNT-TFET offers an increased \( I_{ON} \) by 57.2 times without any \( I_{OFF} \) degradation. Here, \( I_{OFF} \) is defined as drain current when the outer-gate bias \( (V_{OG}) \) is 0 V and inner-gate bias \( (V_{IG}) \) is \(-0.1\) V. \( I_{ON} \) is defined as drain current when \( V_{OG} \) is \( V_{DD} \) with fixed \( V_{IG} \) of \(-0.1\) V. Besides, proposed EHBNT-TFET presents a significant improvement in terms of drain current and subthreshold slope \( (SS) \), exhibiting a sub-60 mV/dec \( SS \) for seven orders of magnitude of drain current, as shown in Fig. 4(b). Furthermore, the minimum \( SS \) in EHBNT-TFET is 2.1 mV/dec, while it is 28.5 mV/dec in NT-TFET. The steep \( OFF/ON \) switch offers a reduced \( SS \) which proves the excellent gate control in EHBNT-TFET.

In TFET devices, \( I_{ON} \) is governed by the inter-band tunneling current across tunneling barrier. With WKB approximation, the tunneling current is calculated as [30].

\[
I_{BTBT} \propto Ae^{-\frac{4\sqrt{m^*E_g}}{3q\hbar}} \tag{1}
\]

Where \( m^* \), \( E_g \), \( q \) and \( h \) is carrier effective mass, band gap, elementary charge and Planck’s constant, respectively. \( E \) is electric field across tunneling junction. \( A \) is the tunneling area. The improved \( I_{ON} \) in the proposed EHBNT-TFET can first be ascribed to the increased tunnel area \( A \). In conventional NT-TFET, the point tunneling dominates and the tunneling area equals the interface between source and channel. However, the line tunneling exists in EHBNT-TFET and the tunneling area equals the overlap between inner-gate and outer-gate. As indicated in Fig. 4(c), EHBNT-TFET obtains a larger tunneling area and then an improved \( I_{ON} \) is expected. Besides, the enhanced electric field also contributes to improved \( I_{ON} \) as demonstrated in Fig. 4(d). The maximum \( E \) in NT-TFET is about 2.2 MV/cm, while it is 2.7 MV/cm in EHBNT-TFET. Furthermore, the maximum \( E \) in EHBNT-TFET appears around the inner/outer-gate overlap, and it is parallel to line tunneling direction. Thus, an improved BTBT rate exists in EHBNT-TFET.

To evaluate the physical mechanism further, the energy band diagrams of two transistors along B-B’ (parallel to channel) and C-C’ (perpendicular to channel) cut-line are shown in Fig. 5(a)–(d). For EHBNT-TFET, there is no...
overlap between the conduction band and valence band of channel in OFF-state, no matter along channel or perpendicular to channel, as shown in Fig. 5(a) and (b). As $V_{OG}$ increases, the energy band bends downward and energy overlap appears. The tunneling distance along C-C’ cut-line is much shorter than that along B-B’ cut-line. Therefore, the line tunneling dominates in EHBNT-TFET, and the lateral point tunneling from source to channel is negligible. On the contrary, as demonstrated in Fig. 5(c) and (d), only point tunneling along the source/channel interface exits in NT-TFET. Due to the limited silicon channel thickness, the line tunneling distance in EHBNT-TFET is greatly lower than the point tunneling distance in NT-TFET, as presented in Fig. 5(e). Furthermore, the line tunneling distance decreases with $V_{OG}$ increasing. The total tunneling strength in both devices is depicted in Fig. 5(f) as a function of gate voltage. It is the smaller tunneling distance that results in the improvement of tunneling rate. The short tunneling distance and large tunneling rate contribute to the improved tunneling strength in EHBNT-TFET.

Table 2 Dynamic performance for the NT-TFET and EHBNT-TFET

| Parameters            | NT-TFET     | EHBNT-TFET |
|-----------------------|-------------|------------|
| Gate capacitance ($C_{gg}$) | 1.60 fF    | 0.66 fF   |
| Intrinsic delay time ($\tau$) | 9.96 $\mu$s | 0.07 $\mu$s |
The dynamic performance of NT-TFET and EHBNT-TFET is compared in Table 2. The intrinsic delay time $\tau$ is calculated as $C_{gg} \times V_{DD} / I_{ON}$ [31], where $C_{gg}$ is the extracted gate capacitance. $C_{gg}$ of EHBNT-TFET is lower than that of NT-TFET by 59% due to the existence of underlap between inner-gate (outer-gate) and drain (source). Furthermore, intrinsic delay time $\tau$ of EHBNT-TFET is reduced about 142 times, due to the combined result of decreased $C_{gg}$ and improved $I_{ON}$.

The transfer characteristics of EHBNT-TFET under various supply voltage is depicted in Fig. 6(a). The extracted transition voltage ($V_{TR}$) keeps constant while $I_{ON}$ declines as $V_{DS}$ decreases from 0.5 V to 0.1 V, as shown in Fig. 6(b). $V_{TR}$ is defined as the outer-gate voltage where the line tunneling starts, and $SS$ has the minimum value [17]. As the outer-gate voltage increases to $V_{TR}$, electrons start to tunnel from the valence band of induced $p^+$ layer to the conduction band of induced $n^+$ layer in channel. Here the line tunneling in EHBNT-TFET is dominated by gate electric field, while is not affected by drain voltage. Therefore, a constant $V_{TR}$ is expected as $V_{DS}$ increases. A lower $V_{TR}$ could allow a lower supply voltage.

2.2 Impact of Doping in EHBNT-TFET

The impact of drain doping ($N_D$) on EHBNT-TFET under various underlap between inner-gate and drain ($L_{IGUD}$) is depicted in Fig. 7, where source doping ($N_S$), overlap between inner/outer-gate ($L_{IOGO}$) and underlap between outer-gate and source ($L_{OGUS}$) keeps unchanged. $I_{OFF}$ remains nearly unchanged for lower $N_D$, while it begins to increase once $N_D$ exceeds $1 \times 10^{18}$ cm$^{-3}$, and the increasing trend is weakened as $L_{IGUD}$ increases, as depicted in Fig. 7(a). $I_{ON}$ monotonically increases as $N_D$ increases for a small $L_{IGUD}$, while it keeps nearly unchanged once $L_{IGUD}$ exceeds 6 nm, as depicted Fig. 7(b). Furthermore, a larger $L_{IGUD}$ presents an improved $I_{ON}$. In EHBNT-TFET, $I_{OFF}$ is comprised of SRH recombination as well as parasitic tunneling from drain to induced $p^+$ layer. As $N_D$ increases, the carrier lifetime declines and then SRH recombination increases. As shown in Fig. 8(a), SRH recombination dominates $I_{OFF}$ under lower $N_D$, and the parasitic tunneling dominates $I_{OFF}$ under high $N_D$. The sharply increased $I_{OFF}$ under $N_D$ of $1 \times 10^{19}$ cm$^{-3}$ is the result of increased parasitic tunneling. As demonstrated in Fig. 8(b), there is no band overlap between drain and channel under low $N_D$. However, when $N_D$ rises to $1 \times 10^{19}$ cm$^{-3}$, the energy band has overlap and the tunneling distance between drain and channel is

![Fig. 6](image1)

1. Transfer curve and $V_{TR}$ and $I_{ON}$ with various $V_{DS}$ for EHBNT-TFET

![Fig. 7](image2)

2. Impact of $N_D$ with various $L_{IGUD}$ on (a) $I_{OFF}$ and (b) $I_{ON}$ for EHBNT-TFET
enough thin, leading to an increased parasitic tunneling current. As shown in Fig. 8(c), the tunneling distance between drain/channel junction increases under larger $L_{IGUD}$. Thus, $N_D$ has less impact on $I_{OFF}$ with $L_{IGUD}$ increasing. The trend of $I_{ON}$ could be illustrated by Fig. 8(d), taking the case of $L_{IGUD} = 2$ nm and $10$ nm for example. At $L_{IGUD} = 2$ nm, due to the effect of inner-gate, the energy band in drain region is lifted up. The high barrier between channel and drain leads to a low $I_{ON}$. With $N_D$ increasing, the energy band in drain bends downward, resulting a lower barrier and then a higher $I_{ON}$. When $L_{IGUD}$ rises up to 10 nm, the energy band in drain is barely affect by inner-gate, so that no high barrier hinders the flow of electron. $I_{ON}$ is barely affected by $N_D$ at $L_{IGUD} = 10$ nm. The smaller $L_{IGUD}$, the higher dependence of $I_{ON}$ on the $N_D$. It is observed that the proposed device achieves better dc performance at $L_{IGUD} = 10$ nm and $N_D = 1 \times 10^{18}$ cm$^{-3}$.

Figure 9 depicts the impact of $N_S$ under various $L_{OGUS}$, where $N_D$, $L_{LOGO}$ and $L_{IGUD}$ keeps unchanged. As shown in Fig. 9(a). When $N_S$ is lower than $1 \times 10^{19}$ cm$^{-3}$, $I_{OFF}$ remains unchanged for arbitrary $L_{OGUS}$. As $N_S$ further increase, $I_{OFF}$ gradually increase especially for the smaller $L_{OGUS}$, such as 2 nm and 4 nm. $I_{ON}$ increases with $N_S$ increasing especially for smaller $L_{OGUS}$ as shown in Fig. 9(b). Here the parasitic tunneling between drain and channel could be ignored due to the large $L_{IGUD}$ and low $N_D$. As shown in Fig. 10(a), SRH recombination keeps constant and therefore BTBT from source to channel dominates the trend with $N_S$. As $N_S$ rises
up to $5 \times 10^{19}$ cm$^{-3}$, particularly for $L_{OGUS} = 2$ nm, electron begins to tunnel from source to channel. The larger $I_{OFF}$ under $N_S$ of $1 \times 10^{20}$ cm$^{-3}$ is the result of energy band overlap between source and channel in OFF-state. Due to low work-function of the outer-gate, the increased $N_S$ leads to a declined tunneling distance and an improved tunneling rate from source to channel under low $L_{OGUS}$ as represented in Fig. 10(b). Thus, the parasitic tunneling between source and channel increases and dominates $I_{OFF}$ under low $L_{OGUS}$ and high $N_S$, leading to a large $I_{OFF}$. However, with $L_{OGUS}$ increasing, tunneling between source and channel hardly takes place due to large tunneling distance. The impact of outer-gate on the energy band of source declines gradually as $L_{OGUS}$ increases. $I_{ON}$ increases more obviously with $N_S$ at a small $L_{OGUS}$. The effect of $N_S$ with various $L_{OGUS}$ on $I_{ON}$ is similar to that of $N_D$ with various $L_{IGUD}$, so the phenomenon is not illustrated anymore. Considering the trade-off between $I_{OFF}$ and $I_{ON}$, $L_{OGUS} = 10$ nm is recommended as the most suitable geometry. Meanwhile, lower $N_S$ could be adopted and the requirement of extremely steep doping profiles between source and channel is not necessary for EHBNT-TFET.

In conventional TFET, $I_{OFF}$ is mainly affected by $N_D$ and $I_{ON}$ is only sensitive to $N_S$ [31]. However, in EHBNT-TFET, $I_{ON}$ is dominated by the line tunneling in channel, and the large underlap at source and drain end eliminate the effect of $N_D/N_S$ on $I_{OFF}$. Therefore, $N_D$ and $N_S$ have little impact on device performance of EHBNT-TFET with large $L_{IGUD}$ and $L_{OGUS}$.

### 2.3 Impact of Geometric Parameters in EHBNT-TFET

The effect of $L_{IODO}$ and inner-gate diameter ($D_{IG}$) are shown in Fig. 11. $I_{ON}$ and $I_{ON}/I_{OFF}$ gradually improves with $L_{IODO}$ and $D_{IG}$ increasing, due to the increased line tunneling area. Although the increased $L_{IODO}$ and $D_{IG}$ also leads to a degraded $I_{OFF}$, $I_{ON}$ has greater improvement than $I_{OFF}$ so that $I_{ON}/I_{OFF}$ is improved. The EHBNT-TFET provides much higher scalability with the help of circular cylinder channel. Compared with EHBTFET, tunneling area can be

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**Table 3** Performance comparison of EHBTFET and EHBNT-TFET

| Parameters | EHBTFET [17] | EHBNT-TFET |
|------------|--------------|-------------|
| $L_{IODO}$ (nm) | 50 | 50 |
| $I_{OFF}$ ($\mu$A/um) | $1.3 \times 10^{-11}$ | $1.3 \times 10^{-11}$ |
| $I_{ON}$ ($\mu$A/um) | 0.016 | 0.036 |
| $I_{ON}/I_{OFF}$ | $1.2 \times 10^9$ | $2.8 \times 10^9$ |
| $V_{DD}$ (V) | 0.5 | 0.5 |

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**Fig. 10** (a) SRH recombination rate and BTBT generation rate under OFF-state with various $L_{OGUS}$ for EHBNT-TFET. (b) Energy band along B-B’ cut-line under OFF-state for EHBNT-TFET

**Fig. 11** Impact of (a) $L_{IODO}$ and (b) $D_{IG}$ on $I_{OFF}$ and $I_{ON}$ for EHBNT-TFET

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extended with smaller device size by larger $D_{SC}$ for EHBNT-TFET. Larger $I_{DGO}$ can achieve higher current drivability without any integration density loss. Furthermore, the proposed EHBNT-TFET shows much higher normalized $I_{ON}$ and $I_{ON}/I_{OFF}$ than conventional EHBTFET due to better gate control, as shown in Table 3.

Figure 12(a) shows the transfer characteristics of EHBNT-TFET with varied silicon channel thickness ($T_{SC}$). $I_{OFF}$ remains constant as $T_{SC}$ increases, while $I_{ON}$ is found to increase first and then gradually drops, as depicted in Fig. 12(b). Parasitic BTBT current is weakened by large $L_{IGUD}$ and low $N_D$, so that $I_{OFF}$ is dominated by SRH recombination current and keeps constant. The energy band perpendicular to channel is shown in Fig. 12(c). As $T_{SC}$ increases, the line tunneling distance increases monotonously and then the tunneling rate degrades. On the other hand, the energy band overlapped region becomes larger, leading to an increased tunneling rate. Besides, the tunneling volume is directly proportional to $T_{SC}$. The tunneling distance, overlapped energy range and tunneling volume contribute to total tunneling strength together, leading to an extremum of tunneling strength at $T_{SC}$ of 4 nm, as shown in Fig. 12(d). At $T_{SC}=3.5$ nm, the smaller energy range and tunneling volume results in the declined $I_{ON}$. When $T_{SC}$ exceeds 4 nm, $I_{ON}$ declines due to the large tunneling distance.

As shown in Fig. 13, the extracted $V_{TR}$ decreases, i.e., the line tunneling starts at lower $V_{OG}$ with $T_{SC}$ increasing.
The energy band perpendicular to channel in OFF-state is presented in Fig. 13(b). No overlap exists between the conduction band and valence band when \( T_{SC} \) increases from 3.5 nm to 5.5 nm. The conduction band near outer-gate is 0.189 eV higher than the valence band near inner-gate at \( T_{SC} = 3.5 \) nm, while it is only 0.011 eV at \( T_{SC} = 5.5 \) nm. Therefore, a larger \( V_{OG} \) is required at \( T_{SC} = 3.5 \) nm to pull down the energy band to create the line tunneling in channel, compared to the case of \( T_{SC} = 5.5 \) nm. As a result, a higher \( V_{TR} \) is obtained for smaller \( T_{SC} \). According to the analysis above, a \( T_{SC} \) of 4 nm could be adopted to improve dc performance of EHBNT-TFET.

### 2.4 Impact of Gate Work-Function and Inner-Gate bias in EHBNT-TFET

The effect of work-function of outer-gate (\( \Phi_{OG} \)) is shown in Fig. 14. \( I_{OFF} \) and \( I_{ON} \) increases monotonously, while \( V_{TR} \) decreases as \( \Phi_{OG} \) decreases from 3.95 eV to 3.75 eV. The lower \( \Phi_{OG} \) causes more inverse electron in the channel, leading to a higher SRH recombination rate and an increased \( I_{OFF} \). As \( \Phi_{OG} \) decreases, the energy band of channel beneath outer-gate moves downward and a steeper \( p^+\)-\( n^+ \) junction is formed, as shown in Fig. 14(c). As a result, an increased \( I_{ON} \) is observed due to the decreased tunneling distance and increased overlapped energy range. To explore the variation of \( V_{TR} \), the energy band perpendicular to channel in OFF-state is plotted in Fig. 14(d). In the case of \( \Phi_{OG} = 3.95 \) eV, the conduction band near outer-gate is 0.138 eV higher than the valence band near inner-gate, while it is only 0.013 eV at \( \Phi_{OG} = 3.75 \) eV. As a result, a higher \( \Phi_{OG} \) results in a larger \( V_{TR} \).

The impact of work-function of inner-gate (\( \Phi_{IG} \)) is shown in Fig. 15. In contrast to the case of \( \Phi_{OG} \), \( I_{OFF} \) and \( I_{ON} \) increases monotonously, while \( V_{TR} \) decreases as \( \Phi_{IG} \) increases from 5.25 eV to 5.45 eV. The increased \( \Phi_{IG} \) have the similar effect on device performance with decreased \( \Phi_{OG} \). More carrier in the channel due to increased \( \Phi_{IG} \) leads to an increased \( I_{ON} \). Similarly, by decreasing surface potential of the channel near inner-gate, the energy band of channel beneath inner-gate is pulled upward, as shown in Fig. 15(c), resulting in an increased \( I_{ON} \). As for transition voltage \( V_{TR} \), the energy band perpendicular to channel in OFF-state is plotted in Fig. 15(d). In the case of \( \Phi_{IG} = 5.25 \) eV, the conduction band near outer-gate is 0.136 eV higher than the valence band near inner-gate, while it is only 0.013 eV at \( \Phi_{IG} = 5.45 \) eV, leading to a lower \( V_{TR} \) at high \( \Phi_{IG} \). In short, the characteristics improve with increasing \( \Phi_{IG} \).

The effect of \( \Phi_{IG} \) and \( V_{IG} \) on EHBNT-TFET is compared by design of experiment in Table 4. It is found that transfer characteristics of experiment No. 1 is exactly the same with that of experiment No. 3, experiment No. 2 and No. 4 is also the same. In short, the reduction of \( \Phi_{IG} \) have the same
effect on device performance with increased $V_{IG}$. The same effect of $\Phi_{IG}$ and $V_{IG}$ makes it more flexible for device and circuit design.

### 3 Conclusion

In this paper, a novel NT-TFET with an intentional misaligned inner/outer-gate has been proposed, achieving excellent static and dynamic performance. Line tunneling between electron-hole bilayer offers the steep transition from OFF-state to ON-state and high drive current. $I_{ON}$ is found to improve by 57.2 times, and a sub-60 mV/dec subthreshold slope for seven orders of magnitude of drain current is obtained. In addition, the impact of doping on static performance was discussed in detail. The performance of EHBNT-TFET is almost unaffected by source and drain doping with large underlap. The immunity of doping eliminates the requirement for formation of abrupt source/channel junction and high thermal budget in fabrication process. Meanwhile, the characteristics of various geometric parameters was studied to obtain better device performance. Due to the electron-hole bilayer induced by appropriate gate configuration, gate work-function and bias are significantly important to offer superior performance.

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### Author Contributions

Conceptualization, methodology, writing-original draft preparation: Xueke Wang; Data analysis: Xueke Wang and Yabin Sun; Writing-review and editing: Yun Liu and Xiaojin Li; Supervision: Ziyu Liu and Yanling Shi; Resources and funding acquisition: Ziyu Liu.

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### Data Availability

The data and material that support the findings of this study are available on request from the corresponding author.

### Code Availability

Not Applicable.
Disclosures

Ethics Approval  Not Applicable.

Consent to Participate  Not applicable.

Consent for Publication  Yes.

Informed Consent  Not applicable.

Research Involving Human Participants and/or Animals  Not applicable.

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