Optimizing T gates in Clifford+T circuit as $\pi/4$ rotations around Paulis

Fang Zhang$^1$ and Jianxin Chen$^{1}$

$^1$Alibaba Quantum Laboratory, Alibaba Group, Bellevue, WA 98004, USA

(Dated: April 1, 2019)

In this work, we introduce a new circuit optimization technique to reduce the number of $T$ gates in Clifford+T circuits by treating $T$ gates conjugated by Clifford gates as $\frac{\pi}{4}$-rotations around Pauli operators. The tested benchmarks shows up to 71.43% and an average 42.67% reduction in T-count, both surpass the best performance reported. The worst case complexity of our algorithm is $O(nk^2)$ where $n$ is the number of qubits and $k$ is the number of $T$ gates in the original Clifford+T circuit.

PACS numbers: 03.65.Ud

I. INTRODUCTION

Much effort has been devoted to build the world’s first meaningful quantum computer, which can deliver the ability to help scientists/engineers to develop new materials from drugs to battery, and to solve optimization problems from finance to logistics. In the past several years, prototypes of early-stage quantum computers are demonstrated by universities and tech companies. To understand the ability of these noisy intermediate-scale quantum (NISQ) devices and the capability of future practical quantum computers, it is essential to develop efficient implementations of quantum algorithms, which are typically expressed in terms of quantum circuits. Quantum compilation, or more specifically, circuit optimization plays an important role in both regimes.

There are many factors to take into consideration when executing quantum circuits on NISQ devices. Just like in classical computer science, efficiency measures the execution time necessary for an algorithm to finish its job. Limited connectivity of existing quantum hardwares have a significant impact on the cost of quantum algorithms. This raise a related problem called qubit allocation or quantum scheduling. Furthermore, there may be significant variation in the error rate of qubits and links, or system reliability in general, on existing hardwares. Such variation makes implementing a given circuit on NISQ hardwares to achieve better performance even more complicated.

Among all the above-mentioned factors, execution time of a circuit is crucial since it will not only affect the performance but also decide if a circuit is realizable on hardware. Quantum states are very fragile due to decoherence which will limit the size of quantum circuits that can be executed on hardware. As a demonstration, various circuit optimization passes are implemented and tested in a recent paper, a measurable performance change of NISQ devices has been observed.

Building NISQ devices will not be our eventual goal. We expect to be able to protect quantum systems from various types of noises and scale up quantum devices using quantum error correction techniques. In the regime of fault tolerant quantum computing, one promising approach is to decompose logic operations on a surface code into Clifford+T circuits. If we take the number of physical qubits involved (space cost) and protocol implementation time (time cost) into consideration, then $T$ gate will be much more expensive than Clifford gates. For example, in a distance-$d$ surface code, the space-time cost of a logical $T$ gate is of order $O(d^3)$ when employing Bravyi-Haah codes. Although the cost of Clifford gates is of same order, the constant pre-factor is less by several orders of magnitude.

Various Clifford+T circuit optimization schemes have been proposed in literature. $T$-count exactly by meet-in-the-middle brute force search, which guarantees optimality, but does not go very far. Namely, it works for two qubits with $m = 12$, or three qubits with $m = 6$. It also introduces the notation of $R(\pm P)$, which is convenient for our approach. $T_{par}$ primarily optimizes $T$-depth by resynthesizing the $T$ gates in each CNOT+T section, but it also improves $T$-count by cancelling pairs of $T$ gates that are moved to the same place. It deals with Hadamard gate $H$ by synthesizing all $T$ gates that “will not be computable” before synthesizing the $H$, which is not quite optimal because some of those $T$ gates may become “computable” again after the next $H$ gate. RM further optimizes CNOT+T sections by showing that optimizing $T$-count in such circuits is equivalent to the minimum distance decoding problem of a certain Reed-Muller code. Although the decoding problem itself is hard,
by using existing Reed-Muller decoders, RM is able to achieve an improved T-count on many benchmark circuits. The handling of H gates is still the same as T gate. TOpt \[12\] uses the idea of gadgetization to deal with H gates: Hadamard gates are eliminated from the first part of the circuit using an ancilla beginning in the \(|+\rangle\) state, which is later measured and classically controls a Clifford gate (which may not be a Pauli, so the quantum controlled version may not be a Clifford). It also uses a new heuristic method on the resulting CNOT+T circuit to reduce T-count in polynomial time.

In this paper, we adapt the \(R(\pm P)\) notation used in \[9\] to regard any Clifford+T circuit as a series of \(\pi/4\) rotations, then cancel pairs of T gates with the help of certain commutation relations. Compared to \(T_{\text{PAR}}\[10\], our method handles all Clifford gates in a unified way instead of having to consider \(H\) as a special case. This allows our method to achieve a strictly higher T-count reduction.

The tested benchmarks shows up to 71.43% and an average 42.67% reduction in T-count, both surpassing the best performance reported. It is worth mentioning that unlike other T-count optimizers which usually cause more than 100% increase in CNOT-count, our optimization procedure will not increase CNOT-count while reducing T-count. Furthermore, one may apply our optimization procedure to those optimized circuits generated from other circuit optimization tools no matter it optimizes CNOT-count or T-count, to get an even smaller T-count without affecting other performance parameters (CNOT-count).

The detailed benchmarking result can be found in Sec\[VI\]

II. PRELIMINARIES

In this section we establish some necessary notations needed for presenting our work. Throughout this paper, we use \(U\) to denote a unitary gate and use \(U\) to denote the matrix corresponds to \(U\).

The Pauli operators on a single qubit are 

\[I = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}, \quad X = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}, \quad Y = \begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix}, \quad Z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}.\]

The set of Pauli operators on \(n\) qubits is defined as \(P_n = \{\sigma_1 \otimes \cdots \otimes \sigma_n | \sigma_i \in \{I,X,Y,Z\}\}\), and \(|P_n| = 4^n\). We use subscripts to indicate qubits on which an operator acts. For example, in a 3-qubit system, \(X_1Z_2 = X_1 \otimes Z_2 = (X \otimes I) \otimes I \times (I \otimes Z) \otimes I = X \otimes Z \otimes I\).

The single-qubit Clifford group is generated by the Hadamard gate \(H\) and phase gate \(S\) where \(H = \frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix}\), \(S = \begin{pmatrix} 1 & 0 \\ 0 & i \end{pmatrix}\). Multi-qubit Clifford group is generated by these two gates along with the CNOT gate \((|0\rangle\langle0| \otimes I + |1\rangle\langle1| \otimes X)\), acting on any, 1 or 2, of those \(n\) qubits.

It is worth mentioning that the Clifford+T universal set attracts a lot of attention and has been widely studied in literature\[13\[14\]. “Universal” here means any multi-qubit unitary gate can be implemented to any given accuracy by using a sequence of gates from Clifford+T set. The number of T gates appear in this sequence is defined as T-count of that Clifford+T circuit representation. Similarly, we can define CNOT-count.

Some T gates on distinct qubits may be performed simultaneously; we will say these T gates are in the same T-cycle. For a given Clifford+T representation, we may have different ways to group these T gates into T-cycles. The minimum number of T-cycles is defined as T-depth of that representation.

A fundamental problem arise: Given a quantum algorithm represented as a unitary gate, what is the most hardware-efficient way to implement it? As we explained in the introduction, much effort have been devoted to understand the hardware efficiency. The choice of cost function may depend on the architecture of the hardware.

Let’s assume a unitary \(U\) has an exact representation over the Clifford+T gate set. Thus there exist Clifford operators \(C_0, C_1, \cdots, C_k\) such that

\[U = C_0(T_{\otimes m_1})C_1(T_{\otimes m_2})\cdots C_{k-1}(T_{\otimes m_k})C_k\]

By substituting variables, there exist Clifford operators \(C_0, C_1, \cdots, C_k\) such that

\[U = C_0(T_{\otimes m_1})C_1(T_{\otimes m_2})(C_1)^\dagger \cdots (C_{k-1})(T_{\otimes m_k})(C_k)^\dagger.\] (1)

Each \(C_i(T_1 \otimes T_2 \cdots \otimes T_{m_i+1})C_i^\dagger\) can be further written as \(C_i T_1 C_i^\dagger C_i T_2 C_i^\dagger \cdots C_i T_{m_i+1} C_i^\dagger\), a sequence of T gates acting on different qubits conjugated by Clifford operator \(C_i\).
III. T gates as π/4 rotations

The T gate can be defined as a π/4 phase rotation around the single-qubit Pauli Z:

\[
T = |0\rangle\langle 0| + e^{i\pi/4}|1\rangle\langle 1| = \frac{1 + e^{i\pi/4}}{2}I + \frac{1 - e^{i\pi/4}}{2}Z. \tag{3}
\]

The key insight is that, when the T gate acting on the i-th qubit is conjugated by any multi-qubit Clifford \( C \), it remains a π/4 phase rotation around a multi-qubit Pauli:

\[
CT_iC^\dagger = 1 + \frac{e^{i\pi/4}}{2}I + \frac{1 - e^{i\pi/4}}{2}CZ_iC^\dagger = R(CZ_iC^\dagger) \tag{4}
\]

where we borrow the following notation from [9]:

\[
R(P) = 1 + \frac{e^{i\pi/4}}{2}I + \frac{1 - e^{i\pi/4}}{2}P, \quad P \in \pm P_n^*. \tag{5}
\]

By the definition of the Clifford group, \( CZ_iC^\dagger \in \pm P_n^* \), where \( P_n^* = P_n \setminus \{I\} \). Also notice that

\[
R(I) = I, \quad R(-I) = e^{i\pi/4}I. \tag{6}
\]

While those are not π/4 rotations, they are both the identity up to a phase, and we choose to allow them because they may be convenient in some circuit transformations.

Another way of understanding \( R(P) \) is that the set \( \{R(P)\} \) is invariant under commutation with any Clifford \( C \):

\[
CR(P) = CR(P)C^\dagger C = R(CPC^\dagger)C. \tag{7}
\]

By applying (7) to shift all Clifford gates to the back, any Clifford+T circuit can be represented as a series of π/4 rotations followed by a Clifford (up to a global phase):

\[
U = e^{i\phi} \left( \prod_{j=1}^{m} R(P_j) \right) C_0 \tag{8}
\]

where \( P_j \in \pm P_n^* \), \( C_0 \in C_n \), and \( m \) is the number of T gates in the circuit. This same form is also presented in [9], except that here we allow negative Paulis as \( P_j \) (because they are sometimes convenient), and we do not assume that \( m \) is the minimum T-count (because computing the minimum is likely to be a computationally hard problem).

IV. A SIMPLE ALGORITHM FOR OPTIMIZING THE T-COUNT

Once we have written a Clifford+T circuit in the form of (8), there are several transformations we can apply to simplify it. The most obvious ones are:

\[
R(P)R(-P) = I, \quad R(P)R(P) = R(P)^2 = \frac{1 + i}{2}(1 - iP) \in C_n, \tag{9}
\]

i.e. two opposite π/4 rotations will cancel each other, and two identical π/4 rotations can be combined into a π/2 rotation, which is a Clifford (namely, it is \( CZ_1C^\dagger \), for any Clifford \( C \) such that \( CZ_1C^\dagger = P \)) and can be shifted to the back with (7). Applying either transformation will reduce the T-count of the circuit by 2.

Of course, it is rare for a Clifford+T circuit to have two π/4 rotations around the same Pauli directly adjacent to each other. However, it is not rare for two adjacent π/4 rotations to commute with each other. For example, if a group of T gates can be executed in parallel, then their corresponding π/4 rotations all commute pairwise. In the \( R(P) \) representation, it is easy to determine which rotations commute:

\[
[R(P), R(Q)] = 0 \iff [P, Q] = 0. \tag{10}
\]

As it turns out, when we take (10) into account, there are many more opportunities to apply (9). Specifically, in the
CNOT + T circuits studied in [10], all the “rotation axis” Paulis are either I or Z on every single qubit; hence, as [10] shows, they all commute with each other.

By studying the Clifford + T circuit as a whole, however, we can find more commuting $\pi/4$ rotations than [10]. For example, in the Mod 5$_4$ circuit, there are several appearances of $(I \otimes H)CNOT(I \otimes H)$, which is really a CZ gate in disguise. It is possible to rewrite the CZ gate as a $CNOT + S$ circuit:

$$CZ = (S \otimes S)CNOT(I \otimes S^1)CNOT. \quad (11)$$

If we apply this transformation before feeding the circuit to the algorithm of [10], then it correctly recognizes that there is a $CNOT + T$ section of the circuit encompassing all the $T$ gates, and optimizes the $T$-count down to 8, as opposed to 16 when this transformation is not applied.

Below, we describe our algorithm that applies (9) and (10) to reduce the $T$-count on its own, it enables other rules like (11) to be applied. Furthermore, reordering $T$ gates may be interesting for its own sake if we consider other goals of circuit optimization, such as minimizing the $T$-depth. The bottleneck of this algorithm is step 2(b); in the worst case, for each $R(P)$ factor in the input circuit, we need to scan through every $R(Q)$ factor in $U_0$, checking equality and commutativity each time. Therefore the worst case complexity is $O(k^2n)$, where $n$ is the number of qubits and $k$ is the number of $T$ gates in the original circuit.

V. THE STRUCTURE OF $\pi/4$ ROTATIONS AS A DAG AND APPLICATION TO $T$-DEPTH OPTIMIZATION

As we have seen, the commutation relation (10) proves quite useful in manipulating Clifford + $T$ circuits. Although it does not decrease the $T$-count on its own, it enables other rules like (9) to be applied. Furthermore, reordering $T$ gates may be interesting for its own sake if we consider other goals of circuit optimization, such as minimizing the $T$-depth.

Since (10) just swaps adjacent $\pi/4$ rotations, applying (10) repeatedly is equivalent to applying some permutation to all the $\pi/4$ rotations in a circuit. However, it may not be immediately obvious which permutations are permissible. Fortunately, there is a simple description for the set of permissible permutations if we regard the structure of $\pi/4$ rotations as a directed acyclic graph (DAG).
Definition 1. The $\mathcal{T}$-graph of a circuit $U$ in the form of

$$U = e^{i\phi} \left( \prod_{j=1}^{m} R(P_j) \right) C_0$$

(13)

is defined as $G_T(U) = (V, E)$, where $V = \{v_j\}$ for $j = 1, \ldots, m$, and

$$E = \{(v_i, v_j) \mid [P_i, P_j] \neq 0 \land i < j\},$$

(14)
i.e. $G_T(U)$ has a vertex for each $\pi/4$ rotation in $U$, and an edge for each pair of $\pi/4$ rotations whose Pauli anti-commute with each other, with the direction of the edge determined on the order in which the two rotations appear in the original circuit.

The $\mathcal{T}$-graph $G_T(U)$ of a circuit is always a DAG, since the order $v_1, \ldots, v_m$ is a topological ordering of $G_T(U)$. In fact, we have the following stronger result:

Theorem 1. By applying only (10), a circuit in the form of (13) can be transformed into

$$e^{i\phi} \left( \prod_{j=1}^{m} R(P_{p_j}) \right) C_0$$

(15)

If and only if $v_{p_1}, \ldots, v_{p_m}$ is a topological ordering of $G_T(U)$.

Proof. First, suppose that repeated applications of (10) can indeed transform (13) into (15). Let $e = (v_{p_i}, v_{p_j})$ be any one edge of $G_T(U)$. By the definition of $G_T(U)$, in the original circuit (13):

- $R(P_{p_i})$ appears before $R(P_{p_j})$;
- $[P_{p_i}, P_{p_j}] \neq 0$.

The latter condition means that application of (10) cannot change the relative order of $R(P_{p_i})$ and $R(P_{p_j})$, so in (15), $R(P_{p_i})$ still appears before $R(P_{p_j})$, i.e. $i < j$. Since this argument is valid for every edge $e = (v_{p_i}, v_{p_j})$ of $G_T(U)$, it follows that $v_{p_1}, \ldots, v_{p_m}$ is a topological ordering of $G_T(U)$.

Conversely, suppose that $v_{p_1}, \ldots, v_{p_m}$ is indeed a topological ordering of $G_T(U)$. Then (13) can be transformed into (15) by doing a bubble sort on the $\pi/4$ rotations until they match the order $R(P_{p_1}), \ldots, R(P_{p_m})$. At each time step, such a bubble sort will only swap two adjacent rotations, $R(P_{p_i})$ and $R(P_{p_j})$, if both of the following are true:

- $p_j < p_i$ (so in (13) $R(P_{p_j})$ comes before $R(P_{p_i})$);
- $i < j$ (so in (15) $R(P_{p_i})$ comes before $R(P_{p_j})$).

The first condition guarantees that $(v_{p_i}, v_{p_j})$ is not an edge of $G_T(U)$, and the second condition, together with the assumption that $v_{p_1}, \ldots, v_{p_m}$ is a topological ordering, guarantees that $(v_{p_i}, v_{p_j})$ is not an edge of $G_T(U)$ either. Therefore $[P_{p_i}, P_{p_j}] = 0$, and (10) can indeed be applied to make the swap. \[\square\]

We note that the “only if” direction of Theorem 1 allows only applications of (10). For example, Both $R(Z)R(-Z)R(X)R(-X)$ and $R(Z)R(X)R(-X)R(-Z)$ evaluates to $I$ by (9), so they are indeed equivalent, but that is not covered by Theorem 1.

We have alluded to the relation between the representation (20) and $\mathcal{T}$-depth of a circuit when we mentioned that $\mathcal{T}$ gates that can be applied in parallel always translate to commuting $\pi/4$ rotations. Unfortunately, the strong converse is not always true — a group of pairwise commuting $\pi/4$ rotations cannot always be translated into a group of $\mathcal{T}$ gates applied in parallel. Instead, we need an extra condition:

Theorem 2. A group of $\pi/4$ rotations, $\prod_{j=1}^{m} R(P_j)$, can be translated into a Clifford + $T$ circuit of $\mathcal{T}$-depth 1 (i.e. one where all the $\mathcal{T}$ gates can be applied in parallel) if both of the following are true:

- All $P_j$ commute with each other;
- There does not exist a non-empty subset $S$ of $\{1, \ldots, m\}$ such that $\prod_{j \in S} P_j = \pm I$. 


Proof. Those two conditions are exactly the conditions under which there exists a Clifford $C \in \mathcal{C}_n$ such that $CP_jC^\dagger = Z_j$ holds for $j = 1, \cdots, m$. The circuit is then given by

$$C^\dagger \left(T^\otimes m \otimes I^\otimes (n-m)\right) C = C^\dagger \left(\prod_{j=1}^m R(Z_j)\right) = \prod_{j=1}^m R(C^\dagger Z_j C) = \prod_{j=1}^m R(P_j). \quad (16)$$

Notice that translating a $\pi/4$-depth 1 circuit back into $\pi/4$ rotations with (7) will indeed result in a circuit in the form of (20) satisfying the conditions of Theorem 2. However, as written, the converse of Theorem 2 is not true, because a circuit that initially does not satisfy those conditions may be simplified or otherwise transformed to satisfy them.

As [10] points out, when the goal is to minimize $\pi$-depth, additional ancilla qubits initialized in the $|0\rangle$ state may be useful. However, they are also tricky: when using ancilla qubits to implement a unitary, they must return to a constant state at the end of the circuit, or otherwise the output state may be entangled with the ancilla instead of being a pure state.

A obvious way to satisfy this condition is to ensure that, when the circuit is transformed into the form of (20), all the ancilla qubits stay in the state $|0\rangle$ throughout the circuit. It turns out that this is more or less what [10] does, too.

**Lemma 1.** Let $P = P_0 \otimes Q$, where $P \in \mathcal{P}_{n+1}$, $P_0 \in \mathcal{P}_n$, and $Q \in \mathcal{P}_1$. Then the following statements are equivalent:

1. $\forall |\psi\rangle \exists |\varphi\rangle \ R(P)(|\psi\rangle \otimes |0\rangle^\otimes) = |\varphi\rangle \otimes |0\rangle^\otimes$;
2. $\exists |\psi\rangle \forall |\varphi\rangle \ R(P)(|\psi\rangle \otimes |0\rangle^\otimes) = |\varphi\rangle \otimes |0\rangle^\otimes$;
3. $Q \in \{I, Z\}^\otimes$;
4. $\forall |\psi\rangle \ R(P)(|\psi\rangle \otimes |0\rangle^\otimes) = (R(P_0)|\psi\rangle) \otimes |0\rangle^\otimes$.

*Proof.* (1) $\Rightarrow$ (2): Obvious.

(2) $\Rightarrow$ (3): The left hand side can be expanded as follows:

$$R(P)(|\psi\rangle \otimes |0\rangle^\otimes) = \left(\frac{1 + e^{i\pi/4}}{2} I + \frac{1 - e^{i\pi/4}}{2} P\right)(|\psi\rangle \otimes |0\rangle^\otimes) \quad (17)$$

$$= \frac{1 + e^{i\pi/4}}{2} (|\psi\rangle \otimes |0\rangle^\otimes) + \frac{1 - e^{i\pi/4}}{2} P(|\psi\rangle \otimes |0\rangle^\otimes)$$

$$= \frac{1 + e^{i\pi/4}}{2} (|\psi\rangle \otimes |0\rangle^\otimes) + \frac{1 - e^{i\pi/4}}{2} (P_0|\psi\rangle \otimes Q|0\rangle^\otimes).$$

The last line should be equal to $|\varphi\rangle \otimes |0\rangle^\otimes$. Equivalently, both of the following must hold:

$$Q|0\rangle^\otimes = |0\rangle^\otimes, \quad (18)$$

$$\frac{1 + e^{i\pi/4}}{2} |\psi\rangle + \frac{1 - e^{i\pi/4}}{2} P_0|\psi\rangle = |\varphi\rangle. \quad (19)$$

The desired statement, $Q \in \{I, Z\}^\otimes$, follows from (18).

(3) $\Rightarrow$ (4): Notice that, in (19), the left hand side evaluates to $R(P_0)|\psi\rangle$. The rest easily follows.

(4) $\Rightarrow$ (1): Obvious. \qed

By repeated application of “(3) $\Rightarrow$ (4)”, we immediately get an easy way to incorporate ancilla qubits into our circuits:

**Corollary 1.** A circuit in the form of (20) implementing the unitary $U$ can always be extended with $\tau$ ancilla qubits as follows:

$$U' = e^{i\phi} \left(\prod_{j=1}^m R(P_j \otimes Q_j)\right) (C_0 \otimes I^\otimes) \quad (20)$$

where $Q_j \in \{I, Z\}^\otimes$. The extension satisfies $U'(|\psi\rangle \otimes |0\rangle^\otimes) = (U|\psi\rangle) \otimes |0\rangle^\otimes$ for all $|\psi\rangle$. 
Theorem 3. Adding ancilla qubits to a circuit $U$ using Corollary 1 does not change its $T$-graph $G_T(U)$.

Proof. It suffices to show that $G_T(U)$ and $G_T(U')$ have the same set of edges, which is equivalent to showing that $[P_i \otimes Q_i, P_j \otimes Q_j] = 0$ if and only if $[P_i, P_j] = 0$. Since $Q_i, Q_j \in \{I, Z\}^m$, $[Q_i, Q_j] = 0$ always holds, so indeed we have $[P_i \otimes Q_i, P_j \otimes Q_j] = 0 \iff [P_i, P_j] = 0$.

Now we revisit Theorem 2. With the help of ancilla qubits, we can remove the second condition.

Theorem 4. A group of $\pi/4$ rotations, $\prod_{j=1}^m R(P_j)$, can be translated into a Clifford + $T$ circuit of $T$-depth 1, with $m$ ancilla qubits, as long as all $P_j$ commute with each other.

Proof. We apply Corollary 1 to extend the group of rotations into $\prod_{j=1}^m R(P_j \otimes Q_j)$, where $Q_j = Z_j \in \{I, Z\}^m$. Now the second condition of Theorem 2 is naturally satisfied, and the first condition of Theorem 2 will continue to be satisfied due to the proof of Theorem 3. Hence an application of Theorem 2 on the extended group of rotations gives the desired result.

For some Clifford + $T$ circuits, the combination of the commutation relation (10) and Theorem 4 is a powerful tool for optimizing the $T$-depth (with an unlimited number of ancilla qubits).

Theorem 5. Using only (10) and Theorem 4, the minimum $T$-depth that can be achieved for a circuit $U$ is exactly equal to the length of (i.e. the number of vertices on) the longest path in $G_T(U)$.

Proof. First, we show that the minimum $T$-depth cannot be less than the length of the longest path in $G_T(U)$. Suppose the longest path in $G_T(U)$ is $v_{j_1}, v_{j_2}, \ldots, v_{j_k}$. By the construction of $G_T(U)$, we have $\{P_{j_1}, P_{j_2}\} = \{P_{j_2}, P_{j_3}\} = \cdots = \{P_{j_{k-1}}, P_{j_k}\} = 0$. When using (10) to swap the rotations, the relative order of $R(P_{j_1}), R(P_{j_2}), \cdots, R(P_{j_k})$ cannot change; then when using Theorem 4 to group the rotations into layers, each of them must go into a different layer, since the rotations in the same layer must pairwise commute. Therefore the minimum $T$-depth that can be achieved this way is $k$, the length of the longest path.

Next, we show that a $T$-depth of $k$ is indeed achievable. To this end, we first sort the vertices of $G_T(U)$ in ascending order of the length of the longest path ending at each vertex. Since the minimum length of such path is 1, and the maximum is $k$, this essentially divides the vertices of $G_T(U)$ into $k$ layers. Edges in $G_T(U)$ can only go from a layer to a later layer, not to any prior layer nor to the same layer. Therefore, this sort is a topological ordering, and by Theorem 1 we can reorder the $\pi/4$ rotations in $U$ accordingly. The fact that there does not exist any edge between vertices in the same layer also means that all rotations corresponding to those vertices commute with each other, so by applying Theorem 4 we can transform each layer into a $T$-layer. The end result is a Clifford + $T$ circuit with $T$-depth $k$.

Again, Theorem 5 restricts the rules of transformation allowed. In particular, cancellation with (9) is not taken into account. In our experiments, we utilize cancellation by applying the algorithm described in [17] before applying Theorem 5; this is also similar to the approach taken in [10].

VI. BENCHMARKING

In this section, we will benchmark our T-Optimizer software with two leading Clifford+T optimizers, T-par and TOpt. The specifications of circuit inputs that T-par and TOpt take are slightly different. T-Optimizer takes a circuit in the .qc format that T-par accepted.

Listing 1: An example: mod5_4.qc

```
.v b c d e a
.i b c d e

BEGIN
 X a
 H a
 Z b e a
 Z d e a
 H a
tof e a
 H a
 Z c d a
```
A description of the .qc format can be found at https://github.com/aparent/QCViewer. For the sake of readability, we briefly explain the basics of .qc file, which indeed serves as textual representation of what the circuit consists of. In the header, .v defines names of the circuit qubits, .i and .o specify which qubits accept primary inputs and report primary outputs respectively. In the body, H refers the Hadamard gate and tof refers to the Toffoli gate. The identifiers following the names refer to the qubits the gate is applies to. For instance, the line H a indicates a Hadamard gate on the qubit named a. In the case where there is more than one qubit as with the Toffoli gate, the rightmost one is the target qubit and the rest are the control qubits.

As mentioned in [12], T-count does not account for the full space-time cost of quantum computation. Thus in our benchmarking result, we present both the CNOT-count and the T-count. The other two leading circuit optimization softwares, T-par and TOpt often produce the output circuit with increased CNOT-count. We also aware that these two open source packages are under active development even after they reported their results in [10–12]. For some instances we tested, the output result is actually better than those reported number. Thus we choose to benchmark our T-Optimizer with these two open source packages rather than the reported results. TOpt has a heuristic subroutine, so we run each instance 100 times, pick the best pair (CNOT-count, T-count) in the sense of reverse lexicographical order on the Cartesian product; if it is worse than the report number, then we will run 100 more times.

![Quantum Circuit describe in mod5_4.qc](image)

FIG. 1: Quantum Circuit describe in mod5_4.qc

VII. SUMMARY AND FUTURE WORK

In this work, we present a new optimization technique to reduce the number of T gates in Clifford+T circuits by treating every T gate conjugated by Clifford operators as $\frac{\pi}{4}$-rotations around Pauli operators. For benchmarking circuits like Adder8 and Mod5_4, T-Optimizer will reduce significantly more T gates than any other circuit optimization software.

As we learn through the benchmarking result, all these benchmarked quantum circuit optimizers have “sweet spots” in which their performance has no equal. A unified framework of circuit optimization would be very interesting.

Another avenue of work is to start from the original unitary gate $U$ which may not be exactly represented by Clifford+T. Many attempts have been made to address this fundamental open question. An algorithm based on exhausted search was presented in [25]. Given its exponential runtime, it is hard to practically use that for reasonable small accuracy $\epsilon$. For quantum algorithms based on phase estimations, phase kickback tricks will introduce ancillary qubits to perform phase gates[26]. The Solovay-Kitaev algorithm and its variants are also well-studied in literature[27]. The algorithm runs in $O(\log^2 (1/\epsilon))$ time and produce a quantum circuit of size $O(\log^3 (1/\epsilon))$ to approximate the desired unitary gate up to accuracy $\epsilon$. In the past several years, several efficient algorithms with improved circuit size (compared with the Solovay-Kitaev algorithm) have been proposed for single-qubit unitary approximation[28–31]. For instance, [30] presents an efficient algorithm to achieve T-counts of $\sim 10 + 4 \log_2 (1/\epsilon)$, which matches the information-theoretic lower bound of $K + 3 \log_2 (1/\epsilon)$. However, to efficiently approximate general multi-qubit unitary gates, there is still ample room for improvement in circuit size.

Note added: Simultaneously with our results, Kissinger and Wetering demonstrated a method to reduce the number of T-gates in a quantum circuit by presenting the quantum circuit as a ZX-diagram and then using the phase teleportation technique[32]. Surprisingly, KW method produces benchmarking results identical to ours and both methods do not change number or locations of any non-phase gates.
| Benchmark     | (CNOT-count, T-count) original | (CNOT-count, T-count) after T-par[18, 19] | (CNOT-count, T-count) after TOpt[20] | (CNOT-count, T-count) after T-Optimizer |
|---------------|--------------------------------|------------------------------------------|--------------------------------------|---------------------------------------|
| Mod_\(X\) [15] | (63,246)                      | (45,163)                                 | (72,121)                             | (38,70)                               |
| VBE-Adder [16] | (80,70)                       | (114,244)                                | (106,36)                             | (70,24)                               |
| CSLA-MUX [17] | (70,70)                       | (379,623)                                | (176,64)                             | (80,62)                               |
| CSUM-MUX [17] | (196,196)                     | (566,841)                                | (984,76)                             | (168,34)                              |
| QCLA-Conn [18] | (235,200)                     | (37,279)                                 | (820,153)                            | (186,35)                              |
| QCLA-Mux [18] | (441,145)                     | (915,347)                                | (595,367)                            | (382,145)                             |
| QCLA-Adder [18] | (267,238)                    | (484,162)                                | (799,187)                            | (283,162)                             |
| Adders [19]   | (466,399)                     | (741,213)                                | (749,258)                            | (409,753)                             |
| RC-Adders [20] | (106,72)                     | (165,47)                                 | (145,39)                             | (93,47)                               |
| Mod-6  [21]   | (124,119)                     | (122,121)                                | (106,30)                             | (106,26)                              |
| Mod-Mults [21] | (33,75)                       | (104,35)                                 | (104,28)                             | (48,35)                               |
| \(A_{QCLA-\text{Adder}}\) - [22] | (26,28) | (52,16) | (32,22) | (24,10) |
| \(A_{1}(X)\) - [22] | (21,21) | (35,13) | (26,15) | (18,15) |
| \(A_{2}(X)\) - [22] | (50,56) | (96,26) | (69,54) | (48,29) |
| \(A_{3}(X)\) - [22] | (35,35) | (63,23) | (42,23) | (30,23) |
| \(A_{4}(X)\) - [22] | (84,84) | (134,40) | (104,54) | (72,40) |
| \(A_{5}(X)\) - [22] | (40,40) | (95,31) | (60,31) | (42,31) |
| \(A_{10}(X)\) - [22] | (224,224) | (332,100) | (284,134) | (192,100) |
| \(A_{15}(X)\) - [22] | (119,119) | (236,71) | (150,71) | (102,71) |
| GF(2^2) Mult [24] | (115,112) | (307,69) | (549,56) | (99,68) |
| GF(2^2) Mult [24] | (179,179) | (502,115) | (1250,53) | (154,115) |
| GF(2^3) Mult [24] | (257,252) | (660,150) | (2449,116) | (221,150) |
| GF(2^4) Mult [24] | (349,345) | (996,217) | (2906,152) | (300,217) |
| GF(2^5) Mult [24] | (469,448) | (1254,264) | (4441,214) | (405,264) |
| GF(2^6) Mult [24] | (575,567) | (1712,391) | (6052,273) | (494,313) |
| GF(2^7) Mult [24] | (789,789) | (2264,479) | (1068,351) | (699,410) |
| GF(2^8) Mult [24] | (1832,1792) | (6724,1040) | (727,23) | (1501,108) |
| GF(2^{15}) Mult [24] | (7292,7168) | (33209,4128) | (727,23) | (6268,1120) |
| GF(2^{25}) Mult [24] | (28860,28672) | (180892,16448) | (727,23) | (24765,16448) |
| Average Reduction | (+142.30%, -141.31%) | (+260.32%, -38.03%) | (0.00%, -42.67%) |
| Maximum T-count Reduction | (+42.50%, -65.71%) | (+40.36%, -61.22%) | (0.00%, -71.45%) |

\( ^a\)CNOT-count better than reported.

\( ^b\)TOpt’s TODD implementation cannot finish the optimization within 24 hours on a cluster node with Intel(R) Xeon(R) Platinum 8163 CPU @ 2.50GHz and 16GB of memory.

\( ^c\)The difference between our CNOT-count and the original CNOT-count reported in Column 2 is caused by different decompositions of Toffoli gates. In our optimization procedure, we didn’t further reduce CNOT-count though it looks we did from the numbers here.

### TABLE I

We report the CNOT-count and T-count after no optimization (original) and after T-par, TOpt and T-Optimizer optimizations with no ancillae.

### Acknowledgements

The authors would like to thank Mario Szegedy and Neil Julien Ross for helpful discussions. J. C. would like to thank Yuneong Nam for sharing benchmarking circuit file used in [33]. Their benchmarking circuits may involve some rotations which may not be Clifford gates anymore, therefore the benchmark result is not included here.

---

[1] M. Y. Siraichi, V. F. d. Santos, S. Collange, and F. M. Q. Pereira, in *Proceedings of the 2018 International Symposium on Code Generation and Optimization* (ACM, 2018) pp. 113–125.

[2] G. Li, Y. Ding, and Y. Xie, arXiv preprint arXiv:1809.02573 (2018).

[3] S. S. Tannu and M. K. Qureshi, arXiv preprint arXiv:1805.10224 (2018).

[4] A. W. Cross, L. S. Bishop, S. Sheldon, P. D. Nation, and J. M. Gambetta, arXiv preprint arXiv:1811.12926 (2018).

[5] A. G. Fowler, M. Marianioni, J. M. Martinis, and A. N. Cleland, *Phys. Rev. A* 86, 032324 (2012).

[6] E. T. Campbell, B. M. Terhal, and C. Vuillot, *Nature* 549, 172 (2017).

[7] A. G. Fowler, S. J. Devitt, and C. Jones, *Scientific reports* 3, 1939 (2013).

[8] J. O’Gorman and E. T. Campbell, *Physical Review A* 95, 032338 (2017).

[9] D. Gosset, V. Klivans, M. Mosca, and V. Russo, arXiv preprint arXiv:1308.4134 (2013).

[10] M. Amy, D. Maslov, and M. Mosca, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 33, 1476 (2014).

[11] M. Amy and M. Mosca, arXiv preprint arXiv:1601.07363 (2016).

[12] L. E. Heyfkon and E. T. Campbell, Quantum Science and Technology 4, 015004 (2018).

[13] G. Nebe, E. M. Rains, and N. J. Sloane, Designs, Codes and Cryptography 24, 99 (2001).

[14] G. Nebe, E. M. Rains, and N. J. A. Sloane, *Self-dual codes and invariant theory*, Vol. 17 (Springer, 2006).
[15] D. Maslov, “Reversible logic synthesis benchmarks page,” (last accessed, Jan. 2019).
[16] V. Vedral, A. Barenco, and A. Ekert, Physical Review A 54, 147 (1996).
[17] R. Van Meter and K. M. Itoh, Physical Review A 71, 052320 (2005).
[18] T. G. Draper, S. A. Kutin, E. M. Rains, and K. M. Svore, Quantum Info. Comput. 6, 351 (2006).
[19] Y. Takahashi, S. Tani, and N. Kunihiro, Quantum Info. Comput. 10, 872 (2010).
[20] S. A. Cuccaro, T. G. Draper, S. A. Kutin, and D. P. Moulton, arXiv preprint quant-ph/0410184 (2004).
[21] I. L. Markov and M. Saeedi, Quantum Info. Comput. 12, 361 (2012).
[22] A. Barenco, C. H. Bennett, R. Cleve, D. P. DiVincenzo, N. Margolus, P. Shor, T. Sleator, J. A. Smolin, and H. Weinfurter, Phys. Rev. A 52, 3457 (1995).
[23] M. A. Nielsen and I. L. Chuang, Quantum Computation and Quantum Information (Cambridge University Press, 2000).
[24] D. Maslov, J. Mathew, D. Cheung, and D. K. Pradhan, Quantum Info. Comput. 9, 610 (2009).
[25] A. G. Fowler, Quantum Info. Comput. 11, 867 (2011).
[26] A. Y. Kitaev, A. Shen, M. N. Vyalyi, and M. N. Vyalyi, Classical and quantum computation, 47 (American Mathematical Soc., 2002).
[27] C. M. Dawson and M. A. Nielsen, arXiv preprint quant-ph/0505030 (2005).
[28] V. Kluchnikov, D. Maslov, and M. Mosca, Physical review letters 110, 190502 (2013).
[29] V. Kluchnikov, D. Maslov, and M. Mosca, IEEE Transactions on Computers 65, 161 (2016).
[30] P. Selinger, arXiv preprint arXiv:1212.6253 (2012).
[31] N. J. Ross and P. Selinger, arXiv preprint arXiv:1403.2975 (2014).
[32] A. Kissinger and J. v. d. Wetering, arXiv preprint arXiv:1903.10477 (2019).
[33] A. M. Childs, D. Maslov, Y. Nam, N. J. Ross, and Y. Su, Proceedings of the National Academy of Sciences 115, 9456 (2018) [https://www.pnas.org/content/115/38/9456.full.pdf].