Monolithic Si-Based AlGaN/GaN MIS-HEMTs Comparator and Its High Temperature Characteristics

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Abstract: Monolithic GaN High Electron Mobility Transistor (HEMT)-integrated circuits are a promising application of wide band-gap materials. To date, most GaN-based devices behave as NMOS-like transistors. As only NMOS GaN HEMT is currently commercially available, its control circuit requires special design if monolithic integration is desired. This article analyzes the schematics of a GaN-based comparator, and three comparator structures are compared through ADS simulation. The optimal structure with the bootstrapped technique is fabricated based on AlGaN/GaN Metal–Insulator–Semiconductor (MIS) HEMT with the recessed gate method. The comparator has excellent static characteristics when the reference voltage increases from 3 V to 8 V. Dynamic waveforms from 10 kHz to 1 MHz are also obtained. High-temperature tests from 25 °C to 250 °C are applied upon both DC and AC characteristics. The mechanisms of instability issues are explained under dynamic working condition. The results prove that the comparator can be used in the state-of-art mixed-signal circuits, demonstrating the potential for the monolithic all-GaN integrated circuits.

Keywords: AlGaN/GaN MIS-HEMT; monolithic comparator circuit; static and dynamic tests; high-temperature stability

1. Introduction

GaN-based power devices have shown superior performances in communication systems and power conversion to Si-based devices, especially in high-speed, high power, and high-temperature applications. These advanced properties benefit from the high electron mobility and low resistance of the two-dimensional electron gas (2DEG) between the AlGaN/GaN interlayer and the high thermal conductivity of the materials [1].

In order to reduce the physical size of the modules and parasitic parameters to show the superiority of the material, the monolithic integrated circuits on GaN epitaxial wafers have undergone extensive research in the last 20 years. However, p-channel GaN devices and GaN CMOS circuits are still under research and need to be improved. The Direct Coupled FET Logic (DCFL) inverter and ring oscillators are the iconic methods to demonstrate successful monolithic implementation. In 2005, the first DCFL inverter and a 23-stage ring oscillator were fabricated [2]. In 2006 and 2007, the fluorine plasma treatment method was also used to achieve the enhancement-mode (E-mode) in the circuits [3,4]. For recessed gate MIS-HEMT technology and p-GaN gate E-mode HEMT, a DCFL inverter was also used as the benchmark for integration to achieve a wide noise margin, large input voltage swing and small propagation delay [5–7]. In 2018, monolithic logic circuits
including NOT, NAND and NOR were reported because of their large noise margin and high-temperature performances [8]. In 2019, GaN power-integrated components and circuits, including HEMTs, Schottky–Barrier Diodes (SBD), Metal–Insulator–Metal (MIM) capacitors and 2DEG resistors, were successfully implemented on GaN-on-SOI (silicon-on-insulator) to form an integration platform [9]. Compared with the conventional CMOS technology, GaN-integrated circuits focus on integrating different power modules such as power, driver and controller to achieve all-GaN integration, which also occurred when the GaAs IC design was carried out in the 1980s [10,11]. However, the systematic comparison and optimization of GaN IC design parameters still needs further improvement.

As an essential part of GaN logic circuits, the comparator draws considerable attention in power electronics for control blocks and power conversion [12]. In 2011, the first GaN comparator circuit was fabricated based on the ion implantation method with DC and AC tests [13]. In 2015, the GaN monolithic comparator was used to perform a PWM circuit, and the hysteresis structure was used to provide feedback from the pulse generation stage to the comparator input [14,15]. In 2021, the impact of D-mode threshold voltage on the comparator circuit was reported [16].

Regarding the circuit-level stability test, the impact of threshold instability for the DCFL inverter was reported for the first time in 2021 [17], while the comparator suffers from the same limitations that may cause fault. This article focuses on the circuit-level high-temperature stability of the monolithic AlGaN/GaN MIS-HEMT-integrated comparator. The simulation of three comparator circuits resulted in an optimized circuit structure with good logic conversion characteristics. The static and dynamic results under 250 °C environments are presented to explore how the high-temperature conditions affect the circuit stability. This comparator indicates the advantages of the integrated circuits for high-temperature applications and provides additional directions for future design.

2. Circuit Simulation

In this section, three different circuit structures as well as the ADS simulation results are discussed. In Figure 1, three comparator circuit schematics are presented for comparison.

![Figure 1. Topologies of three comparator circuits with different active loads. (a) Using the diode structure at the top. (b) Connecting the gate and source nodes together as the active load. (c) Employing the bootstrapped structure at the output current path.](image)

Structure 1: The diodes in the GaN comparator. The diode is used to replace the PMOS current mirror M3 and M4 in the traditional comparator layout. The diode configuration can be seen as a resistor to provide current paths for the differential pair M1 M2.

Structure 2: Figure 1b uses the current source circuit connections for M3 and M4. In 2020, researchers used this structure to design current sensing amplifiers [18]. This can be used for the first stage of GaN amplifiers [19]. If NMOSFET is used to replace PMOS for M3,
and M4 in the amplifier, the current source theory in this circuit, for M3 and M4, the current source can provide a higher resistance. The circuit structure that is successfully used in the amplifier circuit indicates it has a relatively high gain in small-signal applications. For a comparator circuit with an input range of several volts, the circuit is expected to perform a comparison among different reference voltage levels.

Structure 3: Figure 1c demonstrates the bootstrapped structure. The input and output signals are in the same path, where the output is connected to the common gate of M3 and M4, forming a feedback loop. This structure can accelerate the output transition from V_{OH} to V_{OL} [20,21]. In this way, the function of the comparator is improved when the input signal exceeds the reference level.

In Figure 2, the three graphs from top to bottom are the optimized output voltage transfer curves of structures 1, 2 and 3. The six curves in each graph from left to right correspond to the six reference voltages from 3 V to 8 V with a step of 1 V. For structure 1, V_{OH} cannot remain stable where the reference voltage is higher than 5 V since the structure provides a lower output resistance. The simulation results verify that a low resistance can result in low gain at the output stage, which causes the distortion of voltage transition from high to low. For structure 2, the comparison range is larger while the V_{OH} starts to drop below 10 V at a reference of 5 V; this may cause a problem in some applications. Meanwhile, the shift of the voltage swing at different reference voltage levels is still not solved, as in structure a, which is attributed to the unstable current source with fluctuating output by the n-channel device. The output resistance is also not as high as the p-channel current source structure. Moreover, in order to ensure that M3 and M4 are turned on, the upper limit of V_{out} is equal to V_{DD} minus the threshold voltage of the active load, the output swing will be smaller, and the V_{OL} level rises, leading to the reduction of voltage swing with the increase of reference voltage for structures 1 and 2.

![Optimized voltage transfer curves of structures 1, 2 and 3 in ADS simulation.](image)

**Figure 2.** The optimized voltage transfer curves of structures 1, 2 and 3 in ADS simulation.

3. Device Fabrication

Figure 3 shows the device structure. It contained a 4.2 µm GaN buffer grown by Metal–Organic Chemical Vapor Deposition (MOCVD) on the silicon substrate, a 420 nm GaN channel layer above the buffer and a 25 nm AlGaN with the 2DEG channel at the AlGaN/GaN interface. On the top, a 1 nm GaN cap was used to protect the surface from oxidation, which is shown in Figure 3. The MIS-HEMT gate recessed technique was used to realize a high gate voltage swing E-mode structure. The whole process used Au-free fabrication flow. The work began with 400 nm of mesa etching using Inductive Coupled
Plasma (ICP). After that, a coating of SiNₓ was covered by Plasma Enhanced Chemical Vapor Deposition (PECVD). The recessed gate was achieved by a digital etch process using Reactive Ion Etching (RIE) after opening Si₃N₄ at the gate area. At the same time, 18 nm of AlGaN was etched away to deplete the 2DEG channel. Then, the source and drain were formed by depositing metal stacks of Ti/Al/Ni/TiN using the E-beam evaporation. The wafer was put in N₂ ambient at 960 °C for 30 s for rapid thermal annealing to form ohmic contacts. This process was followed by dielectric growth, where 20 nm of Al₂O₃ was deposited using Atomic Layer Deposition (ALD). After that, another layer of Si₃N₄ was deposited. Then, the contact holes on the gate, source, and drain were created by BOE solution. The gate metal of Ni/TiN was deposited using the E-beam evaporation. Finally, the interconnections of the circuit were patterned by depositing another layer of 200 nm Al on the top.

![Cross-section view of recessed gate MIS-HEMT E-mode (left) and D-mode (right) devices.](image)

**Figure 3.** Cross-section view of recessed gate MIS-HEMT E-mode (left) and D-mode (right) devices.

### 4. Results and Discussion

Figure 4 shows the output and transfer characteristics of D-mode and E-mode devices. The I_D-V_D output curves on the left can reveal the maximum output current (when V_D is 10 V). The I_D'-V_G transfer curve determines the threshold voltage. At 25 °C, E-mode device demonstrated a threshold voltage of 0.88 V and a maximum output current I_D of 334 mA/mm when V_G was 10 V. The D-mode threshold voltage was read at about −8.91 V, and the maximum current was 502 mA/mm. The GaN MIS-HEMT had an on/off ratio of 10⁷ with a contact resistance of 4.5 Ω·mm.

Figure 5 shows the top-view micrograph of the fabricated comparator. The connections for DC and AC tests are also presented. The gate width W_g of M₁ and M₂ is 200 µm, and the L_g/L_ds/L_gS is 3/13/5 µm. The V_DD, V_Ref, and V_Bias were provided using an Agilent power supply. For DC analysis, the input voltage sweep and output voltage capture were completed by the Keysight B1500A analyzer. For AC analysis, the input signal came from the RIGOL signal generator, while the output signal was captured by an Agilent oscilloscope.

![Output and transfer characteristics of D-mode and E-mode devices.](image)

**Figure 4.** Output and transfer characteristics of D-mode and E-mode devices.
Figure 5. The top-view micrograph of the fabricated comparator and connections for both DC and AC tests.

Figure 6 shows the voltage transfer curve of the comparator, in which the reference voltage increased from 3 V to 8 V with a 1 V step. The temperature ranged from 25 °C to 250 °C, under a supply voltage of 10 V and a bias voltage of 5 V. The circuit showed a large comparison range, and a high gain of this design. The curve fits the simulated result from the previous Figure 2. When \( V_{\text{in}} \) was larger than the reference voltage, \( V_{\text{out}} \) swept from the logic-high stage to logic-low state. The experiment results showed that \( V_{\text{out}} \) can reach close to \( V_{\text{DD}} \) of 10 V as well as 0 V, realizing the rail-to-rail operation of the comparator circuit. For the thermal stability test, the curves slightly varied with the temperature increasing from 25 °C to 250 °C, showing the \( V_{\text{th}} \) shift of the device in a high-temperature environment. This figure proves the thermal stability of the circuit, which illustrates the advantage of GaN material for extreme environment applications.

Figure 6. The voltage transfer curves of the fabricated comparator from 25 °C to 250 °C. The reference voltages were applied from 3 V to 8 V with a step of 1 V.

Figure 7a shows the first five pulses of the dynamic waveform with a 100 kHz triangular input from \(-10\) V to 10 V. The test was carried out under different temperature conditions from 25 °C to 250 °C. The \( V_{\text{DD}} \) was 10 V, while the reference voltage \( V_{\text{Ref}} \) and bias voltage \( V_{\text{Bias}} \) were both 5 V in this test. It can be seen that the output waveforms maintained a stable square shape at all temperature conditions.

Figure 7b shows the zoomed-in view of one period to investigate the circuit stability further. Under the 100 kHz input frequency, the 2.5 µs up-sweep from 0 V to 10 V was enough to charge the traps at the gate oxide of \( M_2 \). At the down-sweep phase from 10 V to 0 V, the detrapping of gate oxide occurred. The negative phase from 0 V to \(-10\) V of the triangular wave was used to reset the devices.

Figure 7c demonstrates high-temperature dynamic impact on circuit \( V_{\text{OH}} \), \( V_{\text{OL}} \) and duty cycle. The \( V_{\text{OH}} \) suffered a 0.5 V reduction and the \( V_{\text{OL}} \) showed little variation, while the duty cycle suffered a distortion from the high-temperature environment. This can be
explained by taking the distinctive propagation delay \( t_p \) from Figure 7b into account. The average of the high-to-low delay \( t_{pHL} \) and low-to-high delay \( t_{pLH} \) at 250 °C is more than 500 ns larger than the delay at room temperature. This is the main reason that the duty cycle is worsened when \( V_{OH} \) and \( V_{OL} \) remains at a relatively steady level.

**Figure 7.** (a) The first five pluses from the dynamic test under a 100 kHz triangular input. (b) The zoom-in pulse from figure (a) that shows different outputs under temperature from 25 °C to 250 °C. (c) The extracted \( V_{OH} \), \( V_{OL} \) and duty cycle of output curves from 25 °C to 250 °C.

Figure 8 shows the waveforms under different input frequencies at room temperature. It can be seen that the increased frequency has a significant impact on the output curves. The high frequency limit mainly comes from the following three aspects. Firstly, the limit is similar to the propagation delay problems stated before. When the input frequency is 1 MHz with a period of 1 µs, the effect of propagation delay time will be more visible than low frequency output waveforms. This limit can be solved by further reducing the on-resistance of the device and improving the match among devices in comparator circuit. Secondly, the \( V_{OH} \) and \( V_{OL} \) degrade since there is not enough time to maintain the maximum and minimum voltage levels. At 1 MHz, the asymmetry between rising and falling edges indicates the difference between the charging time through active load \( M_4 \) and discharging time through \( M_2 \), which leads to worsened sensitivity with a given 5 V reference voltage. Moreover, the circuit is fabricated using MIS-HEMT technology, and the trap sites of the insulator are charge and discharge in dynamic switching. The interface trap-induced degradation will also affect the high frequency performance. Careful surface treatment under the gate region can help to improve the high frequency performance. In general, both the static and dynamic performance of this monolithic comparator circuit show a significant superiority for working in high-temperature and high-frequency environment compared to silicon-based CMOS counterparts [22].
5. Conclusions

This article discussed the design, fabrication and stability testing of comparator circuits. These circuit schematics were systematically analyzed under a supply voltage of 10 V and reference voltages from 3 V to 8 V. Then, the comparator with a bootstrapped structure was chosen and fabricated based on AlGaN/GaN MIS-HEMT recessed gate technology. The GaN comparator showed good performance that matched the simulation results. The circuit was tested under both static and dynamic working conditions. The high-temperature test was applied, and the output showed reasonable variations up to 250 °C. The mechanism of such variations was explained based on the dynamic output waveform. Furthermore, a frequency test was carried out. The circuit suffered distortion at 1 MHz; future research can focus on improving the fabrication process and matching between D-mode and E-mode components in comparator circuits.

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