Impact of asymmetric dielectric on the performance of TFET

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Abstract. In this work first time we propose the dielectric modulated TFET model and observe the impact of asymmetry on different parameters like ON current, OFF current and intrinsic gate delay for a wide range of dielectric constant by simulation technique. We obtain satisfactory result for ON/OFF current as well as intrinsic delay by applying asymmetric dielectric. Our observation shows that by using the material of dielectric constant in the range of 5 to 20 at source side of TFET gives the best result for ON/OFF current as well as intrinsic delay.

Keywords: Band to band tunneling, ON current, OFF current, intrinsic delay.

1. Introduction
Continuous downsizing of MOSFET’s landed up with some technological barriers and physical limitations. Therefore the need of the hour is to explore alternative device structures. \cite{1} New technologies are required to boost up the performance of the device. Tunnel field effect transistors (TFETs) is a promising member and a good replacement of conventional MOSFETs due to their low subthreshold swing and small leakage current because of its different carrier booster technique based on Band-To-Band Tunneling (BTBT) effect. A steep subthreshold slope which is less than 60 mV/dec at room temperature, large current gain and exceptionally low leakage current made TFETs suitable for low power and high energy circuit applications \cite{2, 3}. There are various interesting features of TFET which are vividly studied in recent literatures. Since tunneling current depends on the tunnel barrier height and internal electric field, low band gap materials are often used to lower the tunneling barrier. In \cite{4} a comparison of subthreshold slopes for low voltage logic applications is represented considering different materials of different band gaps. Whereas in \cite{5} the source drain engineering of the Ge channel TFET is studied. Effects of dielectrics on performance of TFET are also presented in different ways \cite{6-9}. In \cite{6} a DG TFT model with high-k dielectric is proposed and the basic static operation is studied thoroughly. An improved ON-OFF current ratio and less than 60 mV/dec subthreshold slope is found for the simulated architecture. \cite{7} deals with a DG TFET where a multi-layer dielectric is applied and the device physics is studied by analytical approach. Again a heterogeneous dielectric is proposed in \cite{8} for TFET where device and circuit performance for static and dynamic levels are investigated. But the
dielectric is not modulated and performance is also not optimized. In [9] an experimental study is carried out with optimal source doping and gate–source overlapping in the process level. A high ON current as well as low subthreshold slope is obtained for the proposed technique. Impact of the pocket doping on the performance of Scottky TFET are also studied [10-12]. In [10] the effect of pocket doping is studied for source and drain ends and barrier height is optimized whereas [11] proposed an asymmetrical double pockets Schottky barrier TFET structure in which gate drain underlap is incorporated and its effects are studied on the ambipolar behavior.

In this paper we propose a dielectric modulated TFET structure in which the front insulator is divided in two regions, the drain side dielectric is considered as fixed and the source side dielectric is modulated by varying the dielectric constant. The effects of asymmetry are studied on different device parameters and the optimum condition is obtained. The structure and modeling of the dielectric modulated TFET is demonstrated in section 2. A detail result is analyzed after the calibration in section 3. Finally in section 4 conclusions are drawn.

2. Modelling

ATLAS [14] is used to simulate the dielectric modulated TFET. The device is simulated by using a 50-nm n-type ultrathin body Si layers of 8 nm channel thicknesses with a doping concentration of $1 \times 10^{15}$ cm$^{-3}$, $1 \times 10^{19}$ cm$^{-3}$ and $3 \times 10^{18}$ cm$^{-3}$ in formation of channel, source and drain respectively. The front insulator consists of a 2-nm thick dielectric layer which is divided in two equal region, dielectric 1 and dielectric 2 adjacent to source side and drain side respectively, as shown in Fig. 1. A 25 nm SiO$_2$ gate dielectric is used for bottom gate. Dielectric 1 is modulated and dielectric 2 is kept same. For dielectric 2, SiO$_2$ is chosen whereas for dielectric 1, dielectric constant is varied from 3.9 to 28. Work function of Gate material is considered as 4.2 eV. Fermi-Dirac statistics, concentration and field dependent carrier mobility, velocity saturation, band gap narrowing and band to band tunneling model are employed for

![Figure 1. Schematic diagram of TFET](image-url)
the simulation. OFF state and ON state of the device is obtained and depicted in Fig. 2a, Fig 2b and 2c respectively. In Fig. 2b, schematic of energy-band diagram of the ON-state of the Tunnel FET is demonstrated considering Al₂O₃ in region 1 whereas in Fig. 2c, ON-state of the Tunnel FET is presented for HfO₂ in region 1. The figures show that the energy barrier is thin enough in the ON state so that electrons can tunnel from valance band of the p+ region to the conduction band of the intrinsic region. We obtained various electrical parameters like ON current, OFF current, intrinsic delay from the simulation and optimization of ON/OFF current is also done.

**Figure 2a.** OFF-state of the TFET for the device structure corresponds to Fig. 1

**Figure 2b.** ON-state of the TFET considering Al₂O₃ in region 1
3. Result and discussions

The current-voltage characteristic for TFET has been determined in all the regions of device operation. Fig. 3 depicts the variation of drain current with effective gate voltage ($V_G - V_{BT}$) where HfO$_2$ is considered for both the regions of the front insulator. Thus it is similar to a symmetric insulating layer.
Figure 4. Variation of drain current power spectral density against gate voltage for different trap charge densities. Other parameters are $l = 50$ nm, $t = 7$ nm, $t_{eq} = 3$ nm, and $V_{ds} = 1$V.

with HfO$_2$. From the graph it is followed that the results obtained from our model is well matched with the experimental data which ensures validity of our model. Next we varied the dielectric constant of region 1 with respect to SiO2 in region 2 and obtained the drain current in ON-OFF conditions. Fig. 4 demonstrates the effect of asymmetric insulating layer on drain current of TFET. It is observed that ON and OFF current are strongly dependent on the k value of region 1. One can see from the graph that when a symmetric dielectric layer (HfO$_2$) is used, maximum ON current is obtained but at the same time OFF current is also high. But OFF current can be minimized by using asymmetric dielectric layer. Thus a change in ON and OFF current is observed when the dielectric constant of region 1 is varied from 7.5 to 29 with respect to SiO$_2$ layer in region 2. It is clear from the figure that ON/OFF current can be

Figure 5. Plot ON/OFF current against k value in region 1. Other parameters are $l = 50$ nm, $t = 7$ nm, $t_{eq} = 3$ nm, and $V_{DD} = 1$V.
improved significantly by using low value of dielectric constant in region 1. From Fig. 5 we can see that ON/OFF current decreased non linearly for increasing of dielectric constant in region 1. The reason is clear from figure 4 which shows that a low value of dielectric constant in region 1, can reduce the OFF current a lot with respect to the ON current. As a result of which maximum value of ON/OFF current is obtained for $k=7.5$. Fig. 6 depicts the variation of intrinsic delay with dielectric constant. We can notice that although low value of dielectric constant in region 1 offers high ON/OFF current but high intrinsic delay can also be obtained from it because of its lower ON current as found from figure 4. Again Fig. 6 shows that intrinsic delay is gradually decreased with increasing the $k$ value but beyond a particular value ($k=15$) it starts to increase with increasing $k$. Because intrinsic delay $\tau$ is directly proportional to the dielectric constant, so that a high value of $k$ can also make $\tau$ larger. Thus it is better to kept the dielectric constant in between 5 to 20 in region 1 in order to maintain a balance between the ON/OFF current and intrinsic delay.

4. Conclusion
We have proposed a dielectric modulated TFET model in which the drain side dielectric is kept constant and source side dielectric is varied from 3.9 to 29. We obtained that a low dielectric constant in the source side region can improve the ON/OFF current but it offers lower ON current for which intrinsic gate delay is increased. On the other hand instead of contributing high ON current, high $k$ value ($k>20$) in source side region not only reduces the ON-OFF current ratio but also deteriorates intrinsic delay. Thus it is preferable to use $k$ value in between 5 to 20 in source side region to get optimum result.
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