Modified Topology for Three-Phase Multilevel Inverters Based on a Developed H-Bridge Inverter

Samuel Nii Tackie 1,* and Ebrahim Babaei 2

1 Engineering Faculty, Near East University, North Cyprus, Mersin 10, 99138 Nicosia, Turkey
2 Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz 5166616471, Iran; e-babaei@tabrizu.ac.ir
* Correspondence: samuel.niitackie@neu.edu.tr

Received: 7 October 2020; Accepted: 23 October 2020; Published: 5 November 2020

Abstract: This paper proposes a modified three-phase inverter from the developed H-bridge structure having multilevel functionality. The proposed topology can generate 7-levels of phase voltages and 13-levels of line voltages. Simple control methods such as fundamental frequency control method can be applied to the proposed topology. By adding three single-phase transformers, galvanic isolation is created for use in three-phase Dynamic Voltage Restorer systems. The proposed three-phase inverter utilizes less number of components; dc sources, semiconductor switches and driver circuits. Lower rated power switches with reduced blocking voltages are also used. These attributes make the proposed topology less complex in-terms of architecture and control. Comprehensive analysis of the proposed three-phase multilevel inverter and other presented topologies are investigated with respect to levels of output voltage, driver circuit quantity, dc voltage count, total component quantity and standing voltage. Details of the appropriate control technique employed is explained. Finally, practicability of the proposed inverter is validated by simulation using EMTDC/PSCAD software and experimental prototype.

Keywords: multilevel inverter; three-phase inverter; three-phase multilevel inverter; component count; standing voltage

1. Introduction

Multilevel inverters (MLIs) have been in existence for well over three decades now and continue to receive maximum attention from researchers in industry and academia because they are regarded as being more advantageous when compared to their conventional predecessors the two-level inverters [1]. These advantages are minimum switching losses, reduced harmonic content, minimum electromagnetic interference, application of lower rated switches, decreased voltage stress on switches, high quality output waveform, medium and high power compatibility and high efficiency [2,3]. Multilevel inverters are well suited for application in renewable energy systems, electric drives, hybrid electric vehicles, flexible alternating current transmission systems (FACTS) [4,5], dynamic voltage restorers (DVRs), reactive power compensation and high voltage direct current (HVDC) [6]. The majority of these applications require three-phase multilevel inverters for medium to high power system applications. Multilevel inverters are generally categorized into three topologies: cascaded H-bridge (CHB) MLI, diode clamped (DC) MLI and the flying capacitor (FC) MLI. Other topologies of multilevel inverters are modular MLI [7] and hybrid MLI topologies.

Current trends in multilevel inverter development seek to maximize the efficiency of the various MLI topologies by improving the topological structures as well as the control techniques. Minimizing the component count, especially power switches and DC sources [8–10] while increasing the stepped output voltages are critical features of any improved MLI topology. A hybrid clamped ML inverter is
presented by the authors in [11]; this topology offers a minimum component count when compared to similar converters, the structure is mainly composed of 24 switches, one DC source and six capacitors. It also offers better performance and minimum converter cost. A single DC source 7-level inverter is presented in [12], where the component count for each phase are 12 switches, one DC source and three capacitors. This topology is derived from the combination of T-type and active neutral point clamped (NPC) converters. A novel active NPC 7-level inverter is presented in [13]; the basic unit of each phase is composed of 18 switches, four capacitors and one DC source, which translates to a high component count in the three-phase structure. A three-phase cascaded symmetric MLI having a reduced DC source count is presented in [14]. Two DC sources are required for the entire three-phase while each phase is composed of one full-HB and two half-HB, galvanic isolation is provided by a three-phase transformer, minimum component count is achieved with this topology however, the stepped output voltage is 5-levels. Addition of a half HB to each phase will produce 7-levels of output voltage.

A hybrid controlled cascaded MLI is presented in [15] which utilizes the subtraction and addition of sources method to achieve multilevel functionality. Only positive polarity is generated with this method, and a HB topology is required to generate both polarities of voltage. The presented three-phase topology has 10 switches and two DC sources for each phase. Amalgamation of a T-type and a HB structure produces a cascaded MLI. This topology is suitable for high power density and low voltage applications. Each phase is composed of eight switches, three capacitors and one DC source [16]. Two MLI converters are presented in [17]; the first converter has one DC source whiles the second converter has three DC sources, the converter structures are similar. Each converter has 14 switches and three capacitors and generates 7-levels. A 7-levels minimum common-mode voltage converter is presented in [18], the structure of which is composed of one DC source, 10 switches and three capacitors for each phase. A new multilevel inverter structure presented by [19] is composed of one three-phase HB and three single-phase HB structures, to obtain increased multilevel functionality, an auxiliary three-phase HB structure is added to the basic unit, so the phase output voltages are not evenly distributed between positive and negative cycles. Without any auxiliary circuit, 18 switches and four DC sources are used to generate 7-levels having one negative voltage component. A 9-levels modular MLI topology is presented in [20]; the hybrid cascaded structure is composed of 24 switches, one DC source and multiple capacitors. A novel NPC converter with minimum component count when compared to other NPC topologies is presented in [21], this topology generates output voltage of 7-levels for a three-phase system. Eight switches and two capacitors constitute the component total in each phase while 24 switches, eight capacitors and one DC source make-up the component total in the three phase system. A novel NPC converter with minimum component count when compared to other NPC topologies is presented in [21], this topology generates output voltage of 7-levels for a three-phase system. Eight switches and two capacitors constitute the component total in each phase while 24 switches, eight capacitors and one DC source make-up the component total in the three phase system. A novel 7-levels MLI topology is presented in [22], where the component count is 12 unidirectional switches, six bidirectional switches (diode bridge) and six DC sources. A hybrid cascaded three-phase MLI is presented in [23]. The structure is composed of HB and FC topologies utilizing one DC source, 24 switches and five capacitors.

A newly developed three-phase inverter topology having less number of components is proposed in this paper. The proposed topology generates 7-levels of load voltage for each phase and 13-levels of load voltage for line-to-line voltages. The proposed topology only needs a simple control method. Detailed descriptions of the proposed topology with emphasis on component count, blocking voltage, inverter power losses and switching states are provided. To show the advantages of the proposed topology, a comparative investigation of the proposed inverter and other recently presented topologies in terms of switch count, DC-source count, IGBT count and driver circuit count is provided. Finally, simulation and laboratory results are produced to validate the performance of the proposed topology.

2. Proposed Topology

The structure of the proposed three-phase 7-levels inverter is shown by Figure 1. The proposed topology is a further development of the presented structure in [24] which is suitable for single-phase cascaded MLI applications hence the need to develop a topology for three-phase applications.
The extension technique is used in developing the three-phase MLI which reduces the dc voltage quantity from six to four. From voltage point of view, the proposed three-phase topology is composed of 18 unidirectional switches and four DC sources. Each phase is made-up of six switches and two isolated DC sources. When compared to other presented topologies, the proposed topology offers the best trade-off between component count and levels of output voltage. In the proposed topology of Figure 1b, by using three single-phase transformers, it is possible to have galvanic isolation between the sources and loads. One application of this topology is in DVR systems to protect the sensitive loads against sag and swell.

![Figure 1](image-url)

**Figure 1.** Proposed three-phase multilevel inverter; (a) Three independent loads; (b) Three-phase load connected in Y configuration.

Operation of the proposed three-phase inverter is similar to that of a conventional H-Bridge. Diagonally gated switches produce positive or negative output voltages while upper or lower gated switches generate the sum of voltages in each phase. The switching pattern of the proposed three-phase inverter is indicated in Table 1. Phase A output voltages are produced when \( S_{a2}, S_{a3} \), and \( S_{a6} \) conduct, positive \( V_{\text{dc}} \) output voltage is generated, when \( S_{a1}, S_{a4} \), and \( S_{a6} \) conducts positive 2 \( V_{\text{dc}} \) output voltage is generated, when \( S_{a1}, S_{a3} \), and \( S_{a6} \) conducts, positive 3 \( V_{\text{dc}} \) output voltage is generated. Similarly, when \( S_{a1}, S_{a4} \), and \( S_{a5} \) conducts, negative \( V_{\text{dc}} \) output voltage is generated, when \( S_{a2}, S_{a3} \), and \( S_{a5} \)
The symmetric characteristics (for the various phases) of the input voltages provides equal conditions. The proposed topology have subscript descriptions to determine the phase they belong to, hence $S_{a1}$, $S_{a2}$, etc. corresponds to switches in phase A. $S_{b2}$, etc. corresponds to switches in phase B and $S_{c1}$, $S_{c2}$ etc. corresponds to switches in phase C. The output voltages for phases A, B and C are given by $V_A$, $V_B$ and $V_C$ respectively whiles the line-to-line voltages are given by $V_{AB}$, $V_{BC}$ and $V_{CA}$. To generate the desired 7-levels of output voltage in each phase, the magnitude of the input dc voltages should vary i.e., $V_1$ should not equal to $V_2$ and $V_2 \neq V_3$, $V_3 \neq V_4$; if the magnitudes of input dc voltages are equal, 5-levels of output voltage will be generated. Asymmetric feature of the dc sources ensures higher levels of output voltage. Also the polarity connections of the dc sources should be antiparallel or should have a series connection when analyzed from both sides of the converter for each phase. The symmetric characteristics (for the various phases) of the input voltages provides equal conditions for all the phases of the converter. The dc voltage equation is given by:

$$V_2 = V_4 = V_{dc}$$
$$V_1 = V_3 = 2V_{dc}$$

Table 1. Phase Switching Pattern.

| State | Switches | $V_A$ | Switches | $V_B$ | Switches | $V_C$ |
|-------|----------|-------|----------|-------|----------|-------|
| I     | $S_{a2}, S_{a3}, S_{a6}$ | $V_{dc}$ | $S_{b2}, S_{b3}, S_{b5}$ | $V_{dc}$ | $S_{c2}, S_{c3}, S_{c6}$ | $V_{dc}$ |
| II    | $S_{a1}, S_{a4}, S_{a6}$ | $2V_{dc}$ | $S_{b1}, S_{b4}, S_{b5}$ | $2V_{dc}$ | $S_{c1}, S_{c4}, S_{c6}$ | $2V_{dc}$ |
| III   | $S_{a1}, S_{a3}, S_{a6}$ | $3V_{dc}$ | $S_{b2}, S_{b4}, S_{b5}$ | $3V_{dc}$ | $S_{c1}, S_{c3}, S_{c6}$ | $3V_{dc}$ |
| IV    | $S_{a2}, S_{a3}, S_{a5}$ | 0 | $S_{b2}, S_{b3}, S_{b5}$ | 0 | $S_{c2}, S_{c3}, S_{c5}$ | 0 |
| V     | $S_{a1}, S_{a4}, S_{a5}$ | $-V_{dc}$ | $S_{b1}, S_{b4}, S_{b6}$ | $-V_{dc}$ | $S_{c1}, S_{c4}, S_{c6}$ | $-V_{dc}$ |
| VI    | $S_{a2}, S_{a3}, S_{a5}$ | $-2V_{dc}$ | $S_{b2}, S_{b3}, S_{b6}$ | $-2V_{dc}$ | $S_{c2}, S_{c3}, S_{c5}$ | $-2V_{dc}$ |
| VII   | $S_{a2}, S_{a4}, S_{a5}$ | $-3V_{dc}$ | $S_{b1}, S_{b3}, S_{b6}$ | $-3V_{dc}$ | $S_{c2}, S_{c4}, S_{c5}$ | $-3V_{dc}$ |

The proposed topology requires the following component count:

$$N_{\text{switches}} = 18$$
$$N_{\text{Driver}} = 18$$
$$N_{\text{DC-Source}} = 4$$
$$N_{\text{Level}} = 7$$

The above listed parameters $N_{\text{switches}}$, $N_{\text{Driver}}$, $N_{\text{DC-Source}}$ and $N_{\text{Level}}$ corresponds to switch count, driver circuit count, dc source count and number of levels, respectively.

Considering Figure 1b, the pole voltages at $V_{AN}$, $V_{BN}$ and $V_{CN}$ are determine from the equations below:

$$V_{AB} = V_{AN} - V_{BN}$$
$$V_{BC} = V_{BN} - V_{CN}$$
$$V_{CA} = V_{CN} - V_{AN}$$

According to Figure 1b, it is clear that:

$$V_{AN} = V_A$$
$$V_{BN} = V_B$$
$$V_{CN} = V_C$$
Considering the Equations (2) and (3), Equation (2) can be rewritten as follows:

\[
V_{AB} = V_A - V_B \\
V_{BC} = V_B - V_C \\
V_{CA} = V_C - V_A
\]  
(4)

The maximum phase output voltages and stepped voltages are given by:

\[
V_A = V_B = V_C = \pm 3V_{dc} \quad (0, \pm V_{dc}, \pm 2V_{dc}, \pm 3V_{dc})
\]  
(5)

The maximum the line to line output stepped voltages are given by:

\[
V_{AB} = V_{BC} = V_{CA} = 6V_{dc} \quad (0, \pm V_{dc}, \pm 2V_{dc}, \pm 3V_{dc}, \pm 4V_{dc}, \pm 5V_{dc}, \pm 6V_{dc})
\]  
(6)

Power ratings of semiconductor switches is a critical factor which determines the cost of an inverter, operational cost (mostly power losses) and maintenance cost thus it’s desirable to employ lower rated switches to minimize these financial obligations. The blocking voltage of a switch is the maximum magnitude of voltage of either polarity that must be blocked by the switch when opened (not conducting) while the sum of the blocked voltages by the various switches employed in an inverter constitutes the standing voltage of the inverter. The Blocking voltage equations for each phase (1φ) and three-phase (3φ) of the proposed inverter are given below:

\[
V_{1\phi,\text{Block}} = 4(V_1 + V_2) \\
V_{3\phi,\text{Block}} = 3V_{1\phi,\text{Block}} = 12(V_1 + V_2)
\]  
(7)

2.1. Inverter Losses

The overall power losses of the proposed three-phase inverter topology are determined by three parameters known as switching power losses, blocking voltage power losses and conduction power losses. The blocking voltage power losses can be ignored because off-state currents of semiconductors switches are negligible.

2.1.1. Switching Losses

Switching power losses of semiconductor power switches arise during the states of turn-on and turn-off of each switch. Switching power losses of the proposed multilevel inverter are expressed in terms of lost energy during the period of turn-on and turn-off, therefore let \(E_{on}\) and \(E_{off}\) represent these two states respectively. The total switching energy losses is given by \(P_{SW}\). \(V_{sw}\) is the switch voltage when off, \(I\) and \(I'\) are the switch currents before and after switch turn on and off respectively. \(t_{on}\) and \(t_{off}\) are the turn-on time and turn-off time, respectively:

\[
E_{on,k} = \int_{0}^{t_{on}} v(t) i(t) dt = \int_{0}^{t_{on}} \left[ \left( \frac{I'}{t_{on}} t - \frac{V_{sw,k}}{t_{on}} (t - t_{on}) \right) \right] dt = \frac{1}{6} V_{sw,k} I' t_{on}
\]  
(8)

\[
E_{off,k} = \int_{0}^{t_{off}} v(t) i(t) dt = \int_{0}^{t_{off}} \left[ \left( \frac{V_{sw,k}}{t_{off}} (t - t_{off}) \right) \right] dt = \frac{1}{6} V_{sw,k} t_{off}
\]  
(9)

\[
P_{SW} = f_s \sum_{k=1}^{\text{Nswitch}} \left( \sum_{i=1}^{\text{Non,k}} E_{on,k} + \sum_{i=1}^{\text{Noff,k}} E_{off,k} \right)
\]  
(10)
2.1.2. Conduction Losses

Conduction losses of a semiconductor power switch occurs during the on-state of the switch, each power switch of the proposed inverter is composed of one transistor and antiparallel connected diode. The conduction power losses $P_C$ is expressed as the sum of the transistor power losses $P_{C,T}$ and the diode power losses $P_{C,D}$. $R_T$ and $R_D$ are the resistances of the transistor and diodes respectively whiles $V_T$ and $V_D$ are the voltages of the transistors and diodes respectively. The average conduction power losses of Equations (13) and (14) are obtained by integrating Equations (11) and (12) for a period. The period of conduction varies when the load characteristics and control methods are considered:

\[
P_{C,T}(t) = (V_T + R_T i(t))i(t) \tag{11}
\]
\[
P_{C,D}(t) = (V_D + R_D i(t))i(t) \tag{12}
\]
\[
P_{C,T} = \frac{1}{2\pi} \int_0^{2\pi} n_T(t)[VT + R_T i(t)]i(t)\mathrm{d}(\omega t) \tag{13}
\]
\[
P_{C,D} = \frac{1}{2\pi} \int_0^{2\pi} n_D(t)[V_D + R_D i(t)]i(t)\mathrm{d}(\omega t) \tag{14}
\]

Total inverter power loss $P_{\text{LOSS}}$ is given by:

\[
P_{\text{Loss}} = P_{\text{sw}} + P_C \tag{15}
\]

Therefore the efficiency $\eta$ of the inverter is evaluated by:

\[
\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{P_{\text{in}} - P_{\text{Loss}}}{P_{\text{in}}} \tag{16}
\]

3. Comparison with Other 7-Levels Inverters

This section presents a detailed comparison of the proposed topology’s power circuit with other recently presented three-phase 7-levels inverters as well as the three conventional multilevel inverter topologies (NPC, CHB and FC). This comparison is done with respect to the component count; IGBTs, diodes, capacitors, dc sources, transformers and driver circuit circuits. All references of comparison have seven levels of output voltage except for [20] which has 9-levels. Table 2 presents the detailed comparative summary; it can be seen that the proposed topology offers minimum component count in all parameters of comparison except for number of dc sources. MLI with minimum component quantity yields the following advantages; reduced converter losses, reduced size and volume and reduced inverter cost. The general progress made by researchers over the past years in reducing the component quantity of multilevel inverters is exhibited by the great difference in the total component count between the conventional MI topologies and the other references as shown by $N_{\text{Total}}$ column of Table 2.

Table 3 shows the mathematical relationship between the level count ($n$) and the other parameters of comparison which are utilized in plotting the graphs of Figures 2-5. The four parameters used in plotting the graph of comparison are quantity of IGBTs, the quantity of driver circuit, the quantity of dc sources and finally the total component count. These parameters are utilized as against the number of levels to plot the various graphs. The stepped output voltage counts in the proposed topology and presented topologies of Table 3 are all 7-levels.

Figure 2 shows the graph of comparison of IGBT quantity between the proposed topology and other presented topologies of Table 3 with respect to level count. As shown by the graph, the proposed topology together with two other references [19,22] requires the least number of IGBTs to generate the
desired 7-levels. The number of IGBTs and diodes are equal in all topologies under review because of the use of unidirectional switches, however the diode clamped topology requires extra diodes for voltage clamping purposes.

Figure 3 shows the comparison of driver circuit quantity between the proposed topology and other presented topologies of Table 3 with respect to level count. The required driver circuit quantity is dependent on the quantity of switches been utilized; this is because each switch requires an independent driver circuit. For all unidirectional based switches, the driver circuit quantity will always equal to the number of IGBTs. It is evident from the graph of Figure 3 and that of Figure 2 that the proposed topology together with references [19,22] requires the least quantity of driver circuits.

Table 2. Comparative analysis of proposed topology and other presented topologies.

| Topology | N_{level} | N_{IGBT} | N_{DC} | N_{Driver} | N_{MD} | N_{CD} | N_{CF} | N_{C} | N_{T} | N_{Total} |
|----------|-----------|----------|--------|------------|--------|--------|--------|-------|-------|-----------|
| Proposed | 7         | 18       | 4      | 18         | 18     | 0      | 0      | 0     | 1     | 59        |
| [11]     | 7         | 36       | 1      | 36         | 36     | 0      | 0      | 6     | 1     | 116       |
| [12]     | 7         | 36       | 2      | 36         | 36     | 0      | 0      | 9     | 0     | 119       |
| [13]     | 7         | 54       | 1      | 54         | 55     | 0      | 0      | 17    | 0     | 181       |
| [14]     | 7         | 30       | 3      | 30         | 30     | 0      | 0      | 0     | 0     | 94        |
| [15]     | 7         | 30       | 6      | 30         | 30     | 0      | 0      | 0     | 0     | 96        |
| [16]     | 7         | 24       | 1      | 24         | 30     | 0      | 0      | 9     | 0     | 88        |
| [17]     | 7         | 14       | 3      | 14         | 12     | 0      | 0      | 3     | 0     | 46        |
| [18]     | 7         | 30       | 2      | 30         | 30     | 0      | 0      | 9     | 0     | 101       |
| [19]     | 7         | 18       | 6      | 18         | 18     | 0      | 0      | 0     | 0     | 60        |
| [20]     | 9         | 24       | 4      | 24         | 24     | 0      | 0      | 8     | 0     | 84        |
| [21]     | 7         | 24       | 1      | 24         | 24     | 0      | 0      | 8     | 0     | 81        |
| [22]     | 7         | 18       | 6      | 18         | 36     | 0      | 0      | 0     | 0     | 78        |
| [23]     | 7         | 24       | 1      | 24         | 24     | 0      | 0      | 5     | 0     | 78        |
| NPC      | 7         | 36       | 1      | 36         | 36     | 90     | 0      | 6     | 0     | 205       |
| FC       | 7         | 36       | 1      | 36         | 36     | 0      | 45     | 6     | 0     | 160       |
| CHB      | 7         | 36       | 9      | 36         | 36     | 0      | 0      | 0     | 0     | 117       |

Note: N_{level}: Number of levels, N_{IGBT}: number of IGBT, N_{DC}: Number of dc sources, N_{Driver}: Number of driver circuits, N_{MD}: Number of main diodes, N_{CD}: Number of clamping diodes, N_{CF}: Number of clamping capacitors, N_{C}: Number of capacitors, N_{T}: number of transformers, N_{Total}: Total number of components.

Table 3. Comparison Based Equations.

| Topology | N_{IGBT} | N_{Driver} | N_{MC} | N_{DC} | N_{Total} |
|----------|----------|------------|--------|--------|-----------|
| Y-Proposed | 2(n + 2) | 2(n + 2) | -      | n - 3  | (8n + 3)  |
| Y1 [11]   | 6(n - 1) | 6(n - 1)  | n - 7  | n - 6  | (16n + 6) |
| Y2 [12]   | 6(n - 1) | 6(n - 1)  | n + 3  | n - 5  | 17n       |
| Y3 [13]   | (10n - 15) - 1 | (10n - 15) - 1 | 2n + 3 | n - 6  | (27n - 8) |
| Y4 [14]   | 3(2n - 4) | 3(2n - 4) | -      | n - 4  | (13n + 3) |
| Y5 [15]   | 3(2n - 4) | 3(2n - 4) | -      | n - 1  | (13n + 5) |
| Y6 [16]   | 3n + 3   | 3n + 3    | n + 3  | n - 6  | (12n + 4) |
| Y7 [18]   | 3(2n - 4) | 3(2n - 4) | n + 3  | n - 5  | (14n + 3) |
| Y8 [19]   | 2(n + 2) | 2(n + 2)  | -      | n - 3  | 3(2n + 4) + 6 |
| Y9 [20]   | 3n + 3   | 3n + 3    | n + 1  | n - 3  | 12n       |
| Y10 [21]  | 3n + 3   | 3n + 3    | n + 1  | n - 6  | 3(4n - 1) |
| Y11 [22]  | 2(n + 2) | 2(n + 2)  | -      | n - 1  | 3(4n - 2) |
| Y12 [23]  | 3n + 3   | 3n + 3    | n - 2  | n - 5  | 3(4n - 6) |
| Y13 [NPC] | 6(n - 1) | 6(n - 1)  | n - 1  | n - 5  | 6(5n + 1) - (n + 4) |
| Y14 [CHB] | 6(n - 1) | 6(n - 1)  | n - 1  | n - 5  | (22n + 6) |
| Y15 [FC]  | 6(n - 1) | 6(n - 1)  | -      | n + 3  | 3(6n - 2) - 3 |
Figure 2. Graph of $N_{\text{IGBT}}$ versus $N_{\text{LEVEL}}$.

Figure 3. Graph of $N_{\text{DRIVER}}$ versus $N_{\text{LEVEL}}$.

Figure 4. Graph of $N_{\text{TOTAL}}$ versus $N_{\text{LEVEL}}$. 
Variation of total component quantity (N\textsubscript{TOTAL}) between the proposed topology and other aforementioned topologies of Table 3 is shown by Figure 4. Similar to the other abovementioned comparison parameters, the proposed topology requires the least quantity of components as against the other presented topologies. However, the graph of the proposed topology and reference [19] are same for Figure 4 because the difference in total component count is 1 as shown in Table 2. The maximum number of total component count is found in the three conventional topologies of CHB, NPC and FC where NPC and CHB have the highest and the least component count respectively.

The final parameter of comparison is illustrated by Figure 5. Here the number of dc sources required is compared between the proposed topology and the other topologies of Table 3. The conventional topologies of CHB, NPC and FC each requires nine, one and one DC sources respectively, the proposed topology requires four DC sources. However, it’s worth mentioning that no clamping capacitors or blocking diodes are required in the proposed topology but FC and NPC topologies require capacitors to provide the different levels of stepped voltages. Hence there’s a trade-off between the dc source count and the capacitor count by the proposed and presented topologies.

4. Simulation and Experimental Results

To prove the practicability of the proposed topology, simulation and experimental results are provided. The power circuit of the proposed three-phase MLI as shown in Figure 1b with an RL load is built in PSCAD/EMTDC software and a prototype is implemented by using the topology shown in Figure 1a. Switching techniques have the basic functions of producing quality stepped voltages, minimize harmonic content and reduce switching power losses [25]. Fundamental frequency modulation technique is employed as the switching mechanism for the proposed inverter because it offers minimum switching losses when compared to other PWM techniques such as the sinusoidal PWM technique [26,27]. The parameters utilized for simulation and experimental setup are indicated in Table 4. In simulated topology, the turns ratio of transformers is considered N\textsubscript{1}/N\textsubscript{2} = 1.
### Table 4. Parameters for simulation and implementation.

| Parameter                  | Value                  |
|----------------------------|------------------------|
| Input voltage $V_{dc}$     | $V_1 = V_3 = 20$ V, $V_2 = V_4 = 10$ V |
| Output Resistance $R$      | 100 Ω                  |
| Output Inductance $L$      | 55 mH                  |
| Switching Frequency $f_s$  | 4 kHz                  |
| Output Frequency $f_o$     | 50 Hz                  |
| Modulation Index           | 1                      |

### 4.1. Simulation Results

Simulation investigation of the proposed three-phase 7-levels multilevel inverter is carried out by building and simulating the power circuit of the proposed topology in PSCAD/EMTDC software. The generated output waveforms are illustrated by Figures 6–9. The phase voltages are illustrated by Figure 6, with an input voltages of 10 V and 20 V for each phase, the generated seven level output or load voltages with peak to peak magnitude of ± 30 V are plotted together with the desired sinusoidal reference voltage. As shown in Figure 6, $v_a$ corresponds to phase A load voltage, $v_b$ corresponds to phase B load voltage and $v_c$ correspond to phase C load voltage whiles the corresponding reference voltages are represented by $Ref_a$, $Ref_b$ and $Ref_c$, respectively, the incremental step magnitude is ± 10 V. The load currents are illustrated by Figure 7 where $I_a$, $I_b$ and $I_c$ correspond to phases A, B and C load currents respectively, the maximum magnitude of the load currents is 300 mA. The generated line to line load voltage which is composed of thirteen levels (13-levels) with peak to peak magnitude of ± 60 V is illustrated by Figure 8, where $v_{ab}$ corresponds to line to line voltage between phase A and B, $v_{bc}$ corresponds to line to line voltage between phase B and C and $v_{ca}$ corresponds to line to line voltage between phase C and A whiles the corresponding reference voltages are represented by $Ref_{ab}$, $Ref_{bc}$ and $Ref_{ca}$, respectively, the incremental step magnitude is ± 10 V.

Figure 9 shows the blocking voltage of switches in Phase A. The blocked voltage of the four main switches is dependent on the reverse connected dc sources whiles the blocked voltage of the lower and upper switches is the sum of the two voltage sources ($V_1 + V_2 = 30$ V). The symmetric features of the inverter provide same characteristics for all phases. Using Equation (6) and the simulation parameters ($V_1 = V_3 = 20$ V and $V_2 + V_4 = 10$ V), the standing voltage of the proposed inverter for single phase and three-phase modes are 120 V and 360 V, respectively.

### 4.2. Experimental Results

To prove the validity of the simulation results, a laboratory setup is built. The photo of experimental setup is shown in Figure 10. Due to the use of the same conditions for three phases, the output voltage and current waveforms are shown for first phase. Figure 11 shows the waveforms of voltage and current for phase A. Comparing this figure with Figures 6 and 7, it is clear that there is good agreement between the simulation and experimental results. Figure 12 shows the voltage across the switches $S_{a1}$, $S_{a3}$ and $S_{a5}$. The validity and practicality of the proposed inverter is affirmed by given theories, simulation results, and experimental prototype.
Figure 6. Phase output voltage waveform.
Figure 7. Phase output current waveform.
Figure 8. Lin-to-line output voltage waveform.
Figure 9. Blocked voltage of switches in Phase A. (a) Blocked voltage of switch $S_{a1}$; (b) Blocked voltage of switch $S_{a2}$; (c) Blocked voltage of switch $S_{a3}$; (d) Blocked voltage of switch $S_{a4}$; (e) Blocked voltage of switch $S_{a5}$; (f) Blocked voltage of switch $S_{a6}$.

Figure 10. Photo of the experimental setup.
5. Conclusions

A modified three-phase inverter based on developed H-bridge topology is proposed in this paper. The proposed three-phase MLI topology is realized with less number of components, namely 18 unidirectional switches and four DC voltage sources. In the proposed topology, there is no need to use
capacitors. This means that there is no need to use complicated control methods to balance the voltage across capacitors. The main advantages of the proposed topology are less component count hence reduced inverter volume and size, reduced inverter cost, less inverter losses and application of lower rated switches. Fundamental frequency modulation technique was applied in generating 7-levels of load voltage for each phase and 13-levels of load voltage for line-to-line voltages. Comparative analysis of the proposed topology and other recently presented topologies with respect to the component count were investigated and it was evident that the proposed topology required less number of components. Computation of the blocking voltage was also explained theoretically and validated with simulation results. Finally, simulation and experimental results are used to reconfirm the accuracy of theoretical results.

**Author Contributions:** Conceptualization, S.N.T.; methodology, E.B.; software, E.B.; validation, S.N.T. and E.B.; formal analysis, S.N.T.; investigation, S.N.T.; resources, E.B. and S.N.T.; data curation, E.B.; writing—original draft preparation, S.N.T.; writing—review and editing, E.B. and S.N.T.; visualization, E.B.; project administration, E.B.; funding acquisition, S.N.T. and E.B. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research received no external funding.

**Conflicts of Interest:** The authors declare no conflict of interest.

**References**

1. Masoudinia, F.; Babaei, E.; Sabahi, M.; Alipour, H. New Basic Unit and Cascaded Multilevel Inverters with Reduced Power Electronic Devices. *Int. J. Electron.* 2020, 107, 1177–1194. [CrossRef]

2. McGrath, B.P.; Holmes, D.G. Natural capacitor voltage balancing for a flying capacitor converter induction motor drive. *IEEE Trans. Power Electron.* 2009, 24, 1554–1561. [CrossRef]

3. Babaei, E. A Cascade multilevel converter topology with reduced number of switches. *IEEE Trans. Power Electron.* 2008, 23, 2657–2664. [CrossRef]

4. Kim, J.-H.; Sul, S.-K.; Enjeti, P.N. A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltage-source inverter. *IEEE Trans. Ind. Appl.* 2008, 44, 1239–1248. [CrossRef]

5. Buccella, C.; Cecati, C.; Cimoroni, M.G.; Razi, K. Analytical method for pattern generation in five-level cascaded h-bridge inverter using selective harmonic elimination. *IEEE Trans. Ind. Electron.* 2014, 61, 5811–5819. [CrossRef]

6. Leon, J.I.; Kouro, S.; Vazquez, S.; Portillo, R.; Franquelo, L.G.; Carrasco, J.M.; Rodriguez, J. Multidimensional modulation technique for cascaded multilevel converters. *IEEE Trans. Ind. Electron.* 2010, 58, 412–420. [CrossRef]

7. Lesnicar, A.; Marquardt, R. An innovative modular multilevel converter topology suitable for a wide power range. In Proceedings of the 2003 IEEE Bologna Power Tech Conference Proceedings, Bologna, Italy, 23–26 June 2003. [CrossRef]

8. Babaei, E.; Kangarlu, M.F.; Sabahi, M.; Pahlavani, M.R.A. Cascaded multilevel inverter using sub-multilevel cells. *Electr. Power Syst. Res.* 2013, 96, 101–110. [CrossRef]

9. Malinowski, M.; Gopakumar, K.; Rodriguez, J.; Perez, M.A. A survey on cascaded multilevel inverters. *IEEE Trans. Ind. Electron.* 2009, 57, 2197–2206. [CrossRef]

10. Ebrahimi, J.; Babaei, E.; Gharehpetian, G.B. A new topology of cascaded multilevel converters with reduced number of components for high-voltage applications. *IEEE Trans. Power Electron.* 2011, 26, 3109–3118. [CrossRef]

11. Tian, H.; Li, Y.; Li, Y.W. A Novel Seven-Level Hybrid-Clamped (HC) Topology for Medium-Voltage Motor Drives. *IEEE Trans. Power Electron.* 2017, 33, 5543–5547. [CrossRef]

12. Yadav, A.K.; Gopakumar, K.; Umanand, L.; Bhattacharya, S.; Jarzyna, W. A Hybrid 7-Level Inverter Using Low-Voltage Devices and Operation with Single DC-Link. *IEEE Trans. Power Electron.* 2019, 34, 9844–9853. [CrossRef]

13. Sheng, W.; Ge, Q.; Weihui, S. A Novel Seven-Level ANPC Converter Topology and Its Commutating Strategies. *IEEE Trans. Power Electron.* 2017, 33, 7496–7509. [CrossRef]
14. Hasan, M.; Abu-Siada, A.; Dahidah, M.S.A. A three-phase symmetrical DC-Link multilevel inverter with reduced number of DC sources. *IEEE Trans. Power Electron.* 2017, 33, 8331–8340. [CrossRef]

15. Sabyasachi, S.; Borghate, V.B.; Karasani, R.R.; Maddugari, S.K.; Suryawanshi, H.M. A Fundamental Frequency Hybrid Control Technique Based Three Phase Cascaded Multilevel Inverter Topology. *IEEE Access* 2017, 5, 26912–26921.

16. Yu, H.; Chen, B.; Yao, W.; Lu, Z. Hybrid Seven-Level Converter Based on T-Type Converter and H-Bridge Cascaded Under SPWM and SVM. *IEEE Trans. Power Electron.* 2017, 33, 689–702. [CrossRef]

17. Sun, X.; Wang, B.; Zhou, Y.; Wang, W.; Du, H.; Lu, Z. A Single DC Source Cascaded Seven-Level Inverter Integrating Switched-Capacitor Techniques. *IEEE Trans. Ind. Electron.* 2016, 63, 7184–7194. [CrossRef]

18. Sanjeevan, A.R.; Kaarthik, R.S.; Gopakumar, K.; Rajeevan, P.; Leon, J.I.; Franquelio, L.G. Reduced common-mode voltage operation of a new seven-level hybrid multilevel inverter topology with a single DC voltage source. *IET Power Electron.* 2016, 9, 519–528. [CrossRef]

19. Saedabadi, S.; Gandomi, A.A.; Hosseini, S.H.; Sabahi, M.; Gandomi, Y.A. New improved three-phase hybrid multilevel inverter with reduced number of components. *IET Power Electron.* 2017, 10, 1403–1412. [CrossRef]

20. Karasani, R.R.; Borghate, V.B.; Meshram, P.M.; Suryawanshi, H.M.; Sabyasachi, S. A three-phase hybrid cascaded modular multilevel inverter for renewable energy environment. *IEEE Trans. Power Electron.* 2016, 32, 1070–1087.

21. Siwakoti, Y.P.; Mahajan, A.; Rogers, D.; Blaabjerg, F. A Novel Seven-Level Active Neutral Point Clamped Converter with Reduced Active Switching Devices and DC-link Voltage. *IEEE Trans. Power Electron.* 2019, 34, 10492–10508.

22. Raushan, R.; Mahato, B.; Jana, K.C. Comprehensive analysis of a novel three-phase multilevel inverter with minimum number of switches. *IET Power Electron.* 2016, 9, 1600–1607. [CrossRef]

23. Tirupathi, A.; Kirubakaran, A.; Tirumala, S.V. A Seven-Level VSI with a Front-end Cascaded Three-Level Inverter and Flying Capacitor fed H-Bridge. *IEEE Trans. Ind. Appl.* 2019, 55, 6073–6088.

24. Babaei, E.; Aliu, S.; Laali, S. A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge. *IEEE Trans. Ind. Electron.* 2013, 61, 3932–3939. [CrossRef]

25. Pan, Z.; Peng, F.Z.; Corzine, K.A.; Stefanovic, V.R.; Leuthen, J.M.; Gataric, S. Voltage balancing control of diode clamped multilevel rectifier/inverter systems. *IEEE Trans. Ind. Electron.* 2005, 41, 1698–1706. [CrossRef]

26. Gaur, P.; Singh, P. Various control strategies for medium voltage high power multilevel converters: A review. In Proceedings of the 2014 Recent Advances in Engineering and Computational Sciences (RAECS), Chandigarh, India, 6–8 March 2014; pp. 1–6.

27. Babaei, E.; Laali, S.; Bayat, Z. A Single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches. *IEEE Trans. Ind. Electron.* 2014, 62, 922–929. [CrossRef]

**Publisher’s Note:** MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.

© 2020 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).