ABSTRACT

We propose the first reversible coherence protocol (RCP), a new protocol designed from ground up that enables invisible speculative load. RCP takes a bold approach by including the speculative loads and merge/purge operation in the interface between processor and cache coherence, and allowing them to participate in the coherence protocol. It means, speculative load, ordinary load/store, and merge/purge can all affect the state of a given cache line. RCP is the first coherence protocol that enables the commit and squash of the speculative load among distributed cache components in a general memory hierarchy. RCP incurs an average slowdown of (3.0%, 8.3%, 7.4%) on (SPEC2006, SPEC2017, PARSEC), which is lower compared to (26.5%, 12%, 18.3%) in InvisiSpec and (3.2%, 9.4%, 24.2%) in CleanupSpec. The coherence traffic overhead on average 46%, compared to 40% and 27% of InvisiSpec and CleanupSpec, respectively. Even with higher traffic overhead (∼46%), the performance overhead of RCP is lower than InvisiSpec and comparable to CleanupSpec. It reveals a key advantage of RCP: the coherence actions triggered by the merge and purge operations are not in the critical path of the execution and can be performed in the cache hierarchy concurrently with processor execution.

1. INTRODUCTION

As Spectre [15], Meltdown [18] and other attacks [4, 24] demonstrated, modern processor architectures based on speculation are facing major security issues. These attacks exploit the speculative execution to modify or leave trace in the memory system, and extract secrets using side-channels. Yu et al. [30] analyzed the problem systematically and recognized three key steps for a successful speculative execution based attack: speculative accessing the secret, sending it through microarchitectural covert channels, and receiving the secret. Based on this insight, speculative taint tracking (STT) framework is developed for the constructing efficient and low cost defense mechanisms. The key principle of STT is to track the access of speculative data with dynamic tainting and block the sending of a potential secret by stalling the execution of an instruction when it is dependent on speculative data. Based on STT, the Speculative Data-Oblivious Execution (SDO) [29] took a further step by performing low overhead speculative data-oblivious with the prediction that does not depend on speculative data. The results show that the overhead of STT is 14.5% and SDO can further reduce it to 10.0%.

Before or concurrent with STT, a number of solutions, including InvisiSpec [28], SafeSpec [14], CleanupSpec [22], and MuonTrap [1] attempt to ensure the invisible speculative load execution in memory hierarchy. They do not block the speculative load execution but instead prevent the creation of the cache-based covert channels that can send the secret. Compared to STT, they provide weaker security property by only considering invisible speculative loads.

Should we settle down with STT-based solutions and abandon the study of invisible speculative load execution? We believe the answer is NO for three reasons. First, the overhead of SDO is still higher. It provides the “complete” protection against some of the wildest attacks such as [3]. In reality, it is not entirely unreasonable to offer the partial protection to typical cases. Second, in the cache coherence protocol of distributed nature, how to eliminate the effects of speculative loads, potentially spreading across multiple components in memory hierarchy, is intriguing and intellectually challenging on its own right. Based on our analysis in Section 3.3, only InvisiSpec, without change to coherence protocol, can truly provide the truly “invisible” speculative load execution. The pitfalls of CleanupSpec and MuonTrap, which modify coherence protocol, reveal the difficulty of developing any solution that affects the coherence protocol—simply “patching the coherence states” is unlikely to succeed. However, the low overhead still show the promise of such approach.

Finally, it is an important problem that fills a “gap” of the contemporary architectures that existed for decades. Speculative execution is the key technique for achieving high performance. Architects have long understood the need and mechanisms to roll back the effects of speculatively executed instructions inside the processor, but missed the equally important danger of the effects in the cache hierarchy. Filling the fundamental gap is essential to complement our knowledge of cache coherence.

This paper makes a case for the first Reversible Coherence Protocol (RCP), a new protocol designed from ground up that enables invisible speculative load. RCP takes a bold approach by including the speculative loads in the interface between processor and cache coherence, and allowing them to participate in protocol operations. Specifically, the interface includes three new operations from the processor: (1) speculative load; (2) merge, which is performed when a speculative load becomes safe; and (3) purge, which is performed with a speculative load is squashed. These operations can be unified: speculative load, ordinary load/store, and merge/purge can all affect the state of a given cache line. RCP is the first coherence protocol that enables the commit and squash of the
speculative load among distributed cache components in a general memory hierarchy.

To achieve this goal, RCP uses speculative buffers in all cache levels to track the data movements of speculative execution. The difficult and new problem is how to correctly maintain and recover the cache line states when the line is accessed concurrently by multiple speculative and non-speculative loads. We show that this problem is tractable with lazy speculation transition—keeping the effects of speculative load local as much as possible, making it easier to reverse cache states. Based on the principle, we develop the complete RCP protocol. We verified the correctness of RCP protocol using Murphi model checking tool [9].

We implemented RCP with speculative buffers in Gem5 [6]. We compare RCP with InvisiSpec and CleanupSpec using SPEC2006, SPEC2017, and PARSEC. RCP incurs slowdown of (3.0%, 8.3%, 7.4%) on (SPEC2006, SPEC2017, PARSEC), which is lower compared to (26.5%, 12%, 18.3%) in InvisiSpec and (3.2%, 9.4%, 24.2%) in CleanupSpec. The coherence traffic overheads are on average 46%, compared to 40% and 27% of InvisiSpec and CleanupSpec.

Even with the relatively higher traffic overhead, the performance overhead of RCP is lower than InvisiSpec and comparable to CleanupSpec. It validates a key advantage of RCP: the coherence actions triggered by the merge and purge operations are not in the critical path of the execution and can be performed in the cache hierarchy concurrently with processor execution. With the clean interface between processor and cache coherence protocol, RCP can be treated as a "black box", and the coherence traffic can be reduced with further optimizations.

2. BACKGROUND

2.1 Out-of-Order Execution

Modern processors perform speculative out-of-order execution to exploit instruction level parallelism. Recent studies [16, 18] revealed that speculative execution can cause irreversible cache state changes or data movement (e.g., left the speculatively accessed cache block in L1 cache) that can lead to a covert channel. The goal of the paper is to completely eliminate all the effects of speculative load—both cache state and the location of the data in memory hierarchy.

2.2 Threat model

We assume the same threat model of InvisiSpec [28], Safe-Spec [14], and CleanupSpec [22]. We focus on defending transient attacks that is enabled by speculative loads in the futuristic attack model [28]. Stores cannot execute speculatively—assumed by all existing designs. We consider attacks that exploits the entire cache hierarchy, including both private and shared caches (L2/LLC). The TLB and branch predictors can be protected by other orthogonal techniques [23, 28]. We assume that attackers can measure the latency of load and store, but cannot the latency change due to the increase amount of coherence traffic in the system.

Moreover, we focus on protecting the SameThread and Cross-Core models and do not consider simultaneous multi-threading (SMT), which can be prevented by recent techniques such as adding defense when context switch happens [1] or making the cache way-partitioned to avoid SMT-side channels [22]. We also do not protect microarchitectural channel that monitors the timing of execution units [15] including floating-point units [2] and SIMD units [24], which can be mitigated by not scheduling the victim and adversary in adjacent SMT contexts [28]; or speculative attacks based on resource contention [3, 11].

3. FORMAL SECURITY PROPERTY

3.1 Definitions

We consider three key points during the lifetime of a speculative load (SpecRd): 1) Issue point (I): when it is ready to be issued speculatively; 2) Non-speculative point (NS): when it is no longer speculative, either becoming safe or squashed; and 3) Globally perform point (G): when all effects of SpecRd are finalized, either becoming a part of system state (if it becomes safe at NS), or completely cleared (if it is squashed at NS). If a SpecRd becomes safe and committed (denoted as a property C for each SpecRd), we have SpecRd[C] = true, otherwise SpecRd[C] = false. I and G can be defined for both load (speculative SpecRd or not Rd) or stores Wr, and we call [I, G] as the pending period. A Wr is globally performed (all other copies are invalidated) at G. Section 6 shows that non-atomic writes do not affect in our model.

We consider two “effects” of a SpecRd: 1) location of the cache line accessed after G; and 2) state of the cache line after G. In a multi-level cache hierarchy, a cache line can reside at various components. A cache level may have multiple private caches, or one shared cache. The locations of a cache line A in a multi-level cache hierarchy can be defined as a function L[A] shown below. Each L[A] is a bit vector e1,1,...,e1,m, where m is the number of private caches in level i; or a bit ei when the level i is shared. Each ei,j,j ∈ {1,...,m} or ei indicates whether the cache line resides in the corresponding cache. L[A] is a concatenated bit vector indicating present information of a cache line among all cache components. We define the state of a cache line in all cache components by a function S[A], replacing ei,j/lej with s1,j/sj, which indicates the cache line state.

\[
L[A] = (L_1[A],...L_l[A]),
\]

\[
L_i[A] = \begin{cases} (e_1,1,...,e_1,m) & \text{cache level } i \text{ is private} \\ (e_i) & \text{cache level } i \text{ is shared} \end{cases} 
\]

\[
e_{i,j} \in \{0,1\}, \text{ where } i \in \{1,...,l\}, j \in \{i,...,m\}
\]

\[
S[A] = (S_1[A],...S_l[A]),
\]

\[
S_i[A] = \begin{cases} (s_1,1,...,s_1,m) & \text{cache level } i \text{ is private} \\ (s_i) & \text{cache level } i \text{ is shared} \end{cases} 
\]

\[
e_{i,j} \in \{\text{cache block states}\}, \text{ where } i \in \{1,...,l\}, j \in \{i,...,m\}
\]

If the pending period of a ∈ {Rd, Wr} is not overlapped with any other accesses’ pending periods, \(L(\mathcal{A}, a)[A]\) defines the locations of the cache line containing address A after \(G_a\), starting from the initial locations \(\mathcal{A}\) before the execution of a. Similarly, \(S(\mathcal{A}, a)[A]\) defines the states of the cache line, where \(\mathcal{A}\) is the states of the cache line before a is executed.
To capture the effects of a number of concurrent accesses \((a_1, \ldots, a_n)\), \(a_i \in \{Rd, W\rvert\}\), \(L(\mathcal{L}', (a_1, \ldots, a_n)_j)_{\text{init,Gmax}}[A]\) and \(S(\mathcal{J}', (a_1, \ldots, a_n)_{\text{init,Gmax}})\) specify the locations and states of the cache line after all accesses are globally performed serialized with certain total order. \(I_{\text{min}}\) and \(G_{\text{max}}\) are the minimum and maximum I and G among \(a_1, \ldots, a_n\). Each access may cause the changes of the locations and states. Assuming the total order is \(a_1 \rightarrow a_2 \rightarrow \cdots \rightarrow a_n\), the sequences of the location and state change are \(\mathcal{L}_1 \rightarrow \mathcal{L}_2 \rightarrow \cdots \rightarrow \mathcal{L}_n\) and \(\mathcal{J}_1 \rightarrow \mathcal{J}_2 \rightarrow \cdots \rightarrow \mathcal{J}_n\). Specifically, the transition functions when \(a_i\) is serialized right after \(a_{i-1}\) are:

\[
L(\mathcal{L}_{a_{i-1}}, a_i)[A] = \mathcal{L}_i
\]

\[
S(\mathcal{J}_{a_{i-1}}, a_i)[A] = \mathcal{J}_i
\]

### 3.2 Security Property

**Property 1: (Non-overlapping) No effects from mis-specified load, same effects from correct speculated load as non-speculative load.** Consider a \(\text{SpecRd}\), \([I_{\text{SpecRd}}, G_{\text{SpecRd}}]\) is not overlapped with any other access.

If \(\text{SpecRd}[C] = \text{true}\), the locations and states of the cache line should be equivalent to these of an execution by only replacing the \(\text{SpecRd}\) with a normal Rd to the same memory location. Assuming the initial locations and states before \(\text{SpecRd}\) \(\mathcal{L}\) and \(\mathcal{J}\):

\[
L(\mathcal{L}', \text{SpecRd})[A] = L_{\text{SpecRd}}[A] = L(\mathcal{L}', \text{Rd})[A]
\]

\[
S(\mathcal{J}', \text{SpecRd})[A] = S_{\text{SpecRd}}[A] = S(\mathcal{J}', \text{Rd})[A]
\]

If \(\text{SpecRd}[C] = \text{false}\), the locations and states of the cache line should be equivalent to the execution before \(\text{SpecRd}\):

\[
L(\mathcal{L}', \text{SpecRd})[A] = L_{\text{SpecRd}}[A] = L(\mathcal{L}', \text{Rd})[A]
\]

\[
S(\mathcal{J}', \text{SpecRd})[A] = S_{\text{SpecRd}}[A] = S(\mathcal{J}', \text{Rd})[A]
\]

**Property 2: (Overlapping) Serialization of the correct speculated loads.** Two accesses which have overlapping pending period, the first is a speculative load \(\text{SpecRd}\), the second is an access \(acc \in \{\text{Rd, SpecRd, Wr}\}\). If \(\text{SpecRd}[C] = \text{true}\), then the two accesses should be correctly serialized. From Property 1, the final locations and states should be equivalent to the execution that replaces the speculative loads with the corresponding non-speculative load.

\[
L((\text{SpecRd}, acc))[A] = \begin{cases} L(L(\mathcal{L}', \text{SpecRd}), acc), & \text{if SpecRd} \rightarrow acc \\ L(L(\mathcal{L}', acc), \text{SpecRd}), & \text{if acc} \rightarrow \text{SpecRd} \end{cases}
\]

Property 3: (Overlapping) No effects to overlapping accesses from mis-specified loads. With the same accesses as in Property 2, if \(\text{SpecRd}[C] = \text{false}\), the squashed \(\text{SpecRd}\) should not have any effects on the other overlapped accesses.

\[
L(\mathcal{L}', (\text{SpecRd}, acc))[A] = L(\mathcal{L}', acc)[A]
\]

\[
S(\mathcal{J}', (\text{SpecRd}, acc))[A] = S(\mathcal{J}', acc)[A]
\]

**Corollary: A non-speculative request \(acc \in \{\text{Rd, Wr}\}\) is not aware of any overlapping speculative \(\text{SpecRd}\) to the same address before NS point of \(\text{SpecRd}\). It can be directly obtained from Property 3. If the execution is affected by \(\text{SpecRd}\) before its NS point and \(\text{SpecRd}\) is later squashed, \(\text{acc}\) may not reach \(L(\mathcal{L}', acc)[A]\) and \(S(\mathcal{J}', acc)[A]\).**

### 3.3 Analysis of Existing Solutions

**InvisSpec [28].** It satisfies all security properties by not allowing the speculative load to participate the coherence protocol before NS point. The cost is the “double” accesses (redo) for all speculative loads after NS.

**CleanupSpec [22].** It is an undo approach with low overhead. On mis-speculation, besides squashing the execution effects of processor, cache system performs cleanup operations to roll back to the state before the mis-speculation. It ensures that the correctly speculated loads (the common case) are only performed once, and requires random L1 cache replacement and randomized cache design such as CEASER [20, 21].

More importantly, we show that CleanupSpec does not provide completely correct invisible speculative load execution. Let us consider a short sequence of memory accesses from three processors shown in Figure 1 (a) and (b), \(P_1\) is the victim, \(P_2\) and \(P_3\) are attackers. Limited by space, we do not show the complete program for the attack. At high level, \(P_1\) is induced to speculatively access a cache line \(A\) (but later squashed) whose address will reveal secret. \(P_2\) tries to guess and access a cache line that may be \(A\) before \(P_1\)’s \(\text{SpecRd}\) is squashed, then and \(P_3\) can infer the line by measuring the response latency difference caused by irreversible cache state changes. Specifically, if the guess is wrong, \(P_3\) gets the line from \(C_1\), which gets the forwarded request from \(C_2\), since \(P_2\) is the first to access the line (Figure 1 (a)); if the guess
is correct (both $P_1$ and $P_2$ have accessed the line), $P_3$ will directly get the line from $C_2$ (indicated as the red arrow) with shorter latency since $P_1$ is the first to access the line and $P_2$ has changed it to shared (Figure 1 (b)). Based on the latency difference, $P_3$ can infer whether the guess is correct, and if so, the line accessed by $P_3$. Our security properties can prevent such attack (Attack 1) by guaranteeing, even if the line is speculatively accessed by $P_1$, if the load is squashed, $P_3$ should get the line with the same latency as if $P_1$ did not execute the SpecRd. Essentially, a protocol satisfying these properties will behave in the same way as Figure 1 (a).

Let us examine what happens in CleanupSpec for the “correct guess” case illustrated in Figure 1 (c). CleanupSpec allows the state changes to $E$ in $C_{1,1}$, when $P_2$ accesses it before $P_1$’s SpecRd is squashed, $C_{1,1}$ is the one who forward the line. It is different from the scenario if $P_1$’s SpecRd does not exist, in which $P_2$ should experience a cache miss in both L1 and L2 and get the data from memory. In another word, the SpecRd effects the timing of $P_2$’s request (violation of Property 3). In an attempt to ensure the property, CleanupSpec adds a “dummy latency” by forcing an artificial cache miss in $C_2$, which effectively prevents $P_2$ to sense the latency difference. It successfully ensures Property 3 for SpecRd w.r.t. $P_2$’s request. Later, when $P_1$’s SpecRd is squashed, $C_{1,1}$ locally invalidates the line. Unfortunately, this operation does not reverse the state change in $C_2$. In consequence, when later $P_3$ accesses the cache line, it will get the response from $C_2$ with a shorter latency since it is in shared state (both $P_1$ and $P_2$ have accessed it). But the attackers knows that the latency should be longer—forwarded by $C_{1,2}$—if $P_1$ had not accessed the line. This example explains that CleanupSpec does not protect such an attack and Property 3 is violated by SpecRd in $P_1$ w.r.t. $P_1$’s request: the mis-speculation in $P_1$ effects the state of the line in $C_2$ (making it shared), which is later inferred by $P_3$ with response latency difference.

MuonTrap [1]. It uses an L0 cache to keep the speculatively accessed data in restrictive cases when coherence state changes are not exposed. The basic design degrades an MESI protocol to MSI. To benefit from $E$ state, MuonTrap introduces $SE$ state in L0. A line is brought to L0 as $SE$ by SpecRd when a $Rd$ would have brought it to L1 as $E$. It “behaves like $S$ to the coherence protocol”, but when the SpecRd is committed, an “asynchronous upgrade” is performed to invalidate the other copies so that the line can be install in L1 as $E$. Figure 1 (d) shows how the previous example works in MuonTrap. We can see that while $P_2$ and $P_3$ have the same behavior as no SpecRd from $P_1$, thanks to the L0, but when $P_1$’s SpecRd becomes safe, it causes different effects than a normal $Rd$ (violating Property 1). The asynchronous upgrade operation makes every line brought into L0 cache by SpecRd behave like writes—not only introducing more invalidation traffic, but may creating potential side channels.

Both CleanupSpec and MuonTrap stall a speculative load when it is about to change a remote L1 cache copy from $M/E$ to $S$, shown in Figure 1 (e). It is to defend Attack 2: attacker $P_1$ first performs a write to install the line in $M$ in $C_{1,1}$, it tries to infer whether $P_2$ will speculatively access it. If so, a protocol without protection will change the state $M$ in $C_{1,1}$ to $S$ and $C_{1,2}$ will get the line in $S$ (shown in parentheses). The attacker can later detect the state change by longer write latency. It explains why the SpecRd in $P_2$ needs to be stalled. We indicate the behaviors of RCP for Attack 1&2 in Figure 1 (f)(g)(h), which ensure the complete state reversal and the exact same timing and data sources for non-speculative accesses. They will be discussed in Section 6.

DOM [23, 27]. By restricting the speculation, Sakalis et al. [23] delays speculative load on L1 miss (DOM) and avoids processor stall by value prediction. A speculative load does not change the coherence states when missing in the L1 cache. Tran et al. [27] reduces the overhead of DOM by refining the safety condition so that more loads are considered to be safe. DOM is simple solution with higher overhead due to the stall.

Other solutions. Conditional speculation [23] defines security dependency and stalls speculative execution when execution pattern matches the dependency. SpecCFI [17] performs static analysis on the control flow graph to prevent the malicious indirect branch. These designs stall speculative loads when they lead to attacks, orthogonal to RCP.

### 4. HARDWARE STRUCTURE

#### 4.1 Processor Model and Interface

We define three additional operations in the interface between processor and cache system: (1) speculative load; (2) merge, performed when a speculative load becomes safe; and (3) purge, performed with a speculative load is squashed. The processor performs a merge or purge operation by issuing a PrMerge or PrPurge request to L1 cache. The processor tracks the Visibility Point (VP) dynamically during execution determined by the attack model.

In the Spectre-model, an instruction reaches VP if all older control-flow instructions have resolved. In the Futuristic-model, an instruction reaches VP if it cannot be squashed for any reason. All the instructions before (after) VP are considered to be unsafe (safe). With VP maintained during execution, the process can determine whether each instruction becomes safe in each cycle. When an instruction is fetched, it is marked as “unsafe”. When the load is issued, if it becomes safe, then a Rd is generated; otherwise, a SpecRd is issued. The update of VP in a cycle will trigger the merge or purge of sequence of instructions, which can be sent to L1 in batch. To
purge a sequence of speculative loads, only the oldest one is sent and all younger ones are squashed together. For merge, only the youngest is sent and all older ones will be merged. Figure 2 shows the processor model.

### 4.2 Speculative Buffer Structure

RCP uses speculative buffer (specBuf) to keep the effects of speculation. Similar to InvisiSpec [28]; there is a one-to-one mapping relation between a processor’s load queue (LQ) entry and a specBuf entry in both L1 and L2. Figure 3 shows the specBuf organization. For a given LQ entry in core(i)—LQ[i, j]—there is a corresponding specBuf entry in L1 cache, SB_L1[i, j], and L2 cache, SB_L2[i, j]. We denote the specBuf of a core(i) in L1 and L2 as SB_L1[i, j] and SB_L2[i, j], respectively. In this paper, we assume private L1 cache and shared L2 cache as the LLC, so in hardware, SB_L1[i, j] is associated with each core’s L1 cache and all cores’ SB_L2[i, j] are organized together associating with the shared L2. The format of each specBuf in L1 and L2 is the same. The valid bit indicates whether the entry is in use—only the LQ entries for speculative loads have valid specBuf entries. The ready bit indicates whether the coherence transactions related to the entry is in transient. The metadata field keeps speculative access information, e.g., the number of accesses performed to the cache line while it is speculative. This information is used to update the cache status if the line is merged later. While we indicate SpecData field, it is only used to store the actual data of the cache line if it is not allocated in cache. Thus, there is not much data movement between specBuf and cache during merge. Similarly, Coh_State records the coherence state of the line, and is only used when it does not exist in cache. Otherwise, the normal state field in each cache line is used to keep the state. The combined size of all SB_L1[i, j] and SB_L2[i, j] is \(2 \times \text{(number of cores)} \times \text{(number of LQ entries)}\). The number of specBuf entries is the same as InvisiSpec [28].

The additional hardware structure associated with each SB_L2[i, j] is a counting bloom filter (CBF) [10], which approximately records the address set of cache lines that present in each SB_L2[i, j]. In CBF, addresses can be both inserted and removed, thus maintaining a dynamic changing set. Using bloom filters, the membership check can be done very fast, it can generate false positives but never false negatives. The usage of CBFs in L2’s specBufs is that, after each speculative load from core(i) is recorded in the corresponding SB_L2[i, j], RCP requires to get a counter, spec core, which indicates the current total number of speculative loads to this line. Since all speculative loads are recorded in specBuf of L2, this can be obtained by checking all SB_L2[j, *], where \(j \neq i\). However, such operations are expensive. The CBFs associated with each SB_L2[j, *] can be used as the filter to avoid most of the search: we first perform membership check of the line address with all \(CBF_j\) \((j \neq i)\), search is only performed on those having positive outcomes. To prevent timing side-channels, we make the time to check the CBFs constant.

### 4.3 Speculative Buffer Operations

At L1, we define operations in a complete space determined by: (1) access type: speculative or non-speculative; (2) specBuf hit or miss; and (3) L1 hit or miss. Conceptually we have \(2 \times 2 = 8\) scenarios.

For a non-speculative load, it should only access data in L1, not specBuf. Thus, on L1 miss, no matter whether the line is hit in specBuf, a request will be sent to L2 to bring the line to L1. The line in specBuf is created by a speculative load in program order after the non-speculative load. It triggers certain transitions according to RCP, which ensures that the state reached is the same as if the non-speculative load is performed first. If the line misses in specBuf, the request will follow normal coherence protocol.

For a speculative load, it is recorded in specBuf and does not bring data into the cache. If missed in both cache and specBuf, the line is brought to the specBuf, no cache block is allocated, and the state is recorded in specBuf. If it hits in cache but misses in specBuf, the cache line is brought from cache to specBuf, the state is changed into a speculative state, and the cache line and specBuf entry have the same state (recorded in L1). If it misses in cache but hits in specBuf, there is no state change and the speculative load gets data from specBuf. Each specBuf entry has a counter for the number of SpecRds on this entry. It is decreased on a merge or purge. A coherence transition is only triggered when the counter reaches zero.

For L2, the only additional operation is that, for speculative load, after similar operations as L1 are performed, we need to keep track of the number of cores which currently speculatively access a cache line (denoted as spec core) and use that in the protocol operations.

**Relation to InvisiSpec.** We use the similar specBuf structures to store the speculatively moved cache lines, but the similarity ends here. InvisiSpec does not change coherence protocol at all, and when a speculative load becomes safe, it is performed twice. RCP modifies the coherence protocol with extended operations, states, and transitions, which will be described next. **The key distinction in a nutshell**: in RCP, the cache lines accessed by speculative loads are first brought to specBuf and then copied from specBuf to cache on merge; in InvisiSpec, these cache lines are brought to cache by normal coherence operations of an unmodified protocol in the second load (redo).

### 5. RCP COHERENCE PROTOCOL

We develop detailed specifications of the RCP coherence protocol that can reverse all state changes of speculative loads. We build the protocol on top of a typical MESI protocol [19]. While the problem of reversing the global state changes in a completely distributed fashion seems to be quite challeng-
ing, our techniques and principles lead to a systematically designed protocol that is both tractable and verifiable.

### 5.1 Lazy Speculative Transition

To track the effects of speculative loads, we propose the principle of **lazy speculative transition** and introduce the speculative states (SS), in addition to the non-speculative states (NSS) \{M,E,S,I\}. If accessed by a SpecRd from processor, an NSS X at L1 will transition to the corresponding SS \(X_{\text{Spec}}\), \(X \in \{M,E,S,I\}\): \(\text{SpecRd} \Rightarrow X_{\text{Spec}}\). When SpecRd is merged, \(X_{\text{Spec}}\) will transition to state Y and trigger some additional actions to L2, where \(X \xrightarrow{Rd} Y\) is the transition in the MESI protocol. In another word, Y is the state that is determined by the normal MESI protocol on a \(Rd\). When the SpecRd is purged, \(X_{\text{Spec}}\) will transition back to state X in L1. At L2, the transition is based on the updated counters that track the number of speculative copies. The key rationale of the “laziness” is to keep the effects of a SpecRd local as much as possible, making it easier to reverse cache states. Table 1 indicates the speculative states and the corresponding status in RCP.

| States | Global Status               |
|--------|----------------------------|
| SSpec | No non-spec copy, one local spec copy |
| ESpec | One non-spec copy (E), one/more spec copies |
| SSpec | Multiple non-spec copies, one/more spec copies |
| MSpec | One non-spec copy (M), one or more spec copies |

### 5.2 Coherence Requests and Events

RCP has two types of request: 1) Non-Speculative Coherence Requests (NSR), which are the same as the requests in the MESI protocol (Table 2); and 2) Speculative Coherence Requests (SR), which are used for speculative loads and their merge/purge (Table 3). SR can be further divided to the Local Speculative Requests (LSR), which are requests from processor to the local L1 cache; and Remote Speculative Requests (RSR), which are requests forwarded from L2 cache. Table 4 lists the coherence actions that are triggered by coherence requests.

| Type   | Msg   | From   | Description                                           |
|--------|-------|--------|------------------------------------------------------|
| LSR    | SpecRd | Proc   | Speculative read from processor                      |
|        | PrMerge | Proc   | Merge from processor                                 |
|        | PrPurge | Proc   | Purge from processor                                 |
| RSR    | GetSpec | L1,L2  | Notify L2/other L1 sharers that a processor requests a shared copy |
|        | L1Merge | L1,L2  | Notify L2/other L1 sharers that a processor requests a copy to modify, need to invalidate other speculative and shared copies |
|        | L1Purge | L1,L2  | Notify L2/other L1 sharers that a processor is changed from S to M state, need to invalidate other speculative and shared copies |

| Actions | S  | Description                                           |
|---------|----|------------------------------------------------------|
| Flush   | L1 | Flush dirty data back to L2                         |
| Fwd     | L1 | Fwd data to other L1                                 |
| FwdData | L2 | Fwd data from L2 to L1                               |
| FwdSpecData | L2 | Fwd speculative data from L2 specBuf to other L1 |
| GetFromMem | L2 | Fetch cache line from memory and create cache entry at L2 |
| GetSpecFromMem | L2 | Fetch cache line from memory but create entry in L2 specBuf |
| FwdGetX | L2 | Fwd GetX to other sharer (including speculative sharers) to invalidate these copies |
| FwdUpgr | L2 | Fwd Upgrade to other sharer (including speculative sharers) to invalidate their copies |
| FwdGetS | L2 | Fwd GetS to exclusive sharers (E or M) to trigger state downgrades |
| FwdGetSpec | L2 | Fwd GetSpec to other non-spec and spec sharers for state update |
| FwdL1Merge | L2 | Local merge and Fwd L1Merge to non-spec and spec sharers for state update |

### 5.3 L1 Cache State Transitions

**NSR on NSS.** See Figure 4 (a). RCP works exactly the same as MESI.

**LSR on NSS.** See Figure 5 (b). If X is I, the request misses in L1, and a GetSpec request is sent to L2. NSS
cannot receive PrMerge or PrPurge.

RSR on NSS. See Figure 5 (a). When L1 receives the forwarded GetSpec, the cache line can be in either M or E. The owner forwards the data but stays in the same state, otherwise the speculative load will have effects (violation of Property 3). When a remote SpecRd is merged, the owner L1 cache will receive an L1Merge, which finalizes the transition to S. For M, the dirty line is flushed to L2 cache, which should be performed only when the speculative load becomes safe. L1Purge from L2.

LSR on SS. See Figure 5(d). For all SS, when the processor issues another SpecRd, the state is not changed, similar to a read hit on \{M,E,S\} in MESI. For PrPurge, XSpec, \(X \in \{M,E,S\}\), will transition to \(X\) because L1 still holds a non-speculative copy. For PrMerge on ISpec, an L1Merge is sent to L2 cache. If the line is shared (S), ISpec will transition to S; otherwise (non-S), it will transition to E. While the L1 cache is waiting for the response from L2, it resolves the race condition by NACK-ing all requests to the cache line.

NSR on SS. See Figure 5(e). The key insight is that SS can transition among each other by NSR, and when later a PrMerge or PrPurge is received, the state will return to the correct NSS. All SS will transition to I on receiving an invalidation (GetX or Upgrade), but processor will still send PrMerge or PrPurge for the previous SpecRd that caused the transition to SS. In these scenarios, L1 should ignore these requests by staying in \(I\) (Figure 5(b)). The speculative load may be re-issued depending on memory consistency model. More details are discussed in Section 6.

RSR on SS. See Figure 5(c). The three SS states are the same as the corresponding NSS states except that there is a pending speculative load from the processor.

5.4 L2 Cache State Transitions

NSR on NSS. See Figure 4 (b). RCP works exactly the same as MESI.

RSR on NSS. See Figure 6 (a). GetSpec is generated when a SpecRd misses in L1. For M/E, SpecRd request is forwarded to the current owner, which provides data without changing the state (Figure 5(a)).

NSR on SS. See Figure 6 (b). A L1Merge/L1Purge will transition SS back to NSS, before that, the transitions among SS are the same as the transitions among NSS. There is no transition to I since replacement of a line in SS is not allowed.

RSR on SS. See Figure 6 (c). L2 maintains a counter spec core for each cache line to indicate the number of speculative copies among the L1 caches. The counter is increased or decreased when a GetSpec or a L1Merge/L1Purge is received. If it becomes 0 after an L1Purge, meaning that there is no other speculative loads, each XSpec, \(X \in \{M,E,S,I\}\), will transition back to \(X\); otherwise they stay in the same state.

If it becomes 0 after an L1Merge, the SS transitions to an NSS as if a GetS is received. For MSpec, it transitions to S since there are more than one shared copies, in addition, L2 forwards a L1Merge to the current owner. For ESPEC, it can transition to E or S. The caveat is that the speculative and non-speculative copy can be brought by the same processor. It can be determined by comparing the current non-speculative owner cur_owner with the sender of L1Merge, if they are the same, then ESPEC transitions to E. Otherwise, it transitions to S, and L2 also forwards a L1Merge to cur_owner. Note that cur_owner information already exists in the normal MESI protocol to identify the owner when a line is in M/E in L2. In RCP, cur_owner is updated in two additional cases: 1) a GetS is received in ISpec—a Rd will get the only non-speculative copy of the line in an L1; or 2) L1Merge is received in ISpec—a speculative copy becomes the only non-speculative copy.

If spec core>0 after decreasing by L1Merge, there are still speculative loads pending, but the four SS will transition due to different number of non-speculative copies. Specifically, MSpec will transition to SSpec, because now we have more than one non-speculative copies plus some speculative copies. For SSpec and ESPEC, they will both transition to SSpec, because there are more than one non-speculative copies plus at least one speculative copy. For ISpec, it transitions to ESPEC, because now we have one non-speculative copy (just merged) and at least one speculative copy (spec core>0).

5.5 Non-Atomic Transactions

The non-atomic transaction means a state transition in a given cache component cannot be completed with a single step. For example, when a write is performed on a shared cache line, the transition of state from S to M is not atomic. The problem can be solved by introducing a transient state, e.g., SM for the above case, and Nack-ing all incoming requests while the line is in transient states, or developing additional transitions from transient states.

In RCP, such non-atomic transactions from the original
MESI protocol are assumed to be handled with the existing mechanisms—any real protocol implementation needs to consider them. We only consider non-atomic transactions related to speculative load requests and states. Only the transitions related to ISpec may lead to transient period. It happens when transitioning to ISpec or from ISpec to an E/S. In L1, when a SpecRd misses in L1, a GetSpec request is sent to L2 and when the response is received, the state transitions to ISpec. When L1 receives a PrMerge/PrPurge at ISpec, a request is sent to check whether the line is shared or not, then ISpec transitions to E (non-S) or S (S) accordingly. These two cases can be handled by keeping all requests during such transient period and only processing them when the state is stable. Due to the few transient scenarios in RCP, we do not need to introduce a new transient state, and instead use a bit to indicate that the cache line is in ISpec but it is waiting for the data (I → ISpec) or non-S/S information (ISpec → E/S). When the bit is set, the incoming requests are queued and processed later. Note that queuing the coherence requests is a standard technique and used in all real implementations.

The reason why RCP is mostly not affected by non-atomic transactions is that, the additional states and transitions are introduced to handle only speculative loads, while most complications are due to writes. Two requests on the same state, as long as the state is stable, do not cause any problem—they are not the same as non-atomic transactions. For example, consider ESpec in an L1, it can “concurrently” receive a forwarded GetSpec and a local PrPurge. In RCP, processing them in either order is correct. If PrPurge is processed first, the state transitions to E, and the cache will forward data as the response to GetSpec but stays in E. If GetSpec is processed first, the state is still ESpec, which will transition to E when PrPurge is processed.

5.6 Protocol Verification

We use Murphi model verification tool [9] to verify our protocol and quantify the complexity of RCP. We model the two level MESI protocol from GEM5 implementation suite and make it as a baseline. To keep the number of explored states tractable, as the similar verification methodology in [8], we used a single address, two data values with private L1 cache and a shared L2 with directory. As we model only one address to reduce the number of states explored, we modeled replacements as unconditional events that can be triggered at any time. The verification explored 3,244,350 reachable states, which is 70% more than MESI, in 1,186 seconds. We verify that the protocol states and transitions happen exactly as designed. The verification can reach all speculative states, which can always transition back to NS eventually.

5.7 3-Level and Non-inclusive Cache

RCP can be extended to 3-level cache with a shared L3 and private L1 and L2. The cache state and transitions of the two private cache levels can be developed in a similar manner as the private L1 in RCP; and the L3 shared level cache is similar to L2 in RCP. The interactions between L1 and L2 in RCP resemble the interactions between L2 (the last level of private cache) and the shared L3. The operations in L1 and L2 are similar. While there must be special cases, we do not see fundamental obstacles.

The design principles can work in the new setting: (1) speculative load requests will be downward propagated from L1 to a lower level, which can serve or forward the request. Whenever such request travels to a cache component, specBuf entry is allocated and the state transitions are triggered. (2) PrMerge and L1Merge follow the same downward path to trigger the delayed final state transition and merge of specBuf entry. The shared L3 may forward L1Merge upward to the relevant cache components (e.g., to the current owner so that it transitions to shared). (3) PrPurge and L1Purge follow the same downward path to trigger state rollback and specBuf data elimination but are never sent upward. The key observation is, the downward and upward message propagation path and the relevant cache components are known according to how a normal load is performed.

RCP can be in principle extended to non-inclusive cache. The difference between inclusive and non-inclusive is, the insertion of a line in a cache may cause the line to be deleted from other caches. Based on RCP, we can augment the state of a cache line with the destination location, which provides the information on which cache the line will be moved to on merge. It should be incorporated to the actual non-inclusive policy implementation which should already have such structure [12]. In general, non-inclusive policy may incur less extra traffic for merge and purge, because less cache components keep the data. We leave the concrete extension to non-inclusive cache as future work.

6. SECURITY ANALYSIS

In this section, we prove that RCP satisfies the three properties in Section 3.2. For a normal load/store A, the serialization point ($S_A$) is the point during its pending period that the access is serialized in the global total order of accesses to this address. For a speculative load A, in RCP it does not have a
Figure 7: Proof of RCP’s Security Properties 2&3

**Property 2: Serialization of correct speculation**

**Property 3: No effects for mis-speculation**

**Property 2/3: Two speculative loads**

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single serialization point, instead, it has a **reach point** ($R_A$), indicating the point that it reaches L1/L2; and a **merge point** ($M_A$) or **purge point** ($P_A$), indicating the point that it is merged or purged in L1/L2.

**Proof of Property 1**: We need to show the correctness of an individual $SpedRd$ (since its pending period is not overlapping with others): 1) after a merge, the change to the location and state of the cache line is equivalent to performing a non-speculative read to the same location; 2) after a purge, the effects of $SpedRd$ are completely eliminated.

- **Cache states.** a) Merge. In RCP, the speculatively accessed data are all stored in specBuf until the merge. The copying of data from specBuf to L1/L2 (local merge) always happens when L1/L2 receives $PrMerge/L1Merge$, which also causes the state transition to NSS. Thus, the speculatively accessed cache line is installed in the same cache components as a non-speculative load to the same address. b) Purge. The cache line in specBuf will be simply eliminated—no data is installed in any cache components.

**Proof of Property 2** ($SpecRd$ overlaps with load/store):
We consider all possible behaviors of a non-speculative access $B$ and a speculative load $A = \text{SpecRd}$, where $R_A < S_B < M_A$. Note that we only need to consider this case, because if $S_B < R_A$, $B$ will not affect $A$ and $A$’s behavior is ensured by Property 1. Similarly, we do not need to consider $S_B > M_A$. Given this setting, we have four cases, when $B$ is a load $Rd$ or a store $Wr$, and when they are issued from the same or different L1 cache: $C_{1A} = C_{1B}$ or $C_{1A} \neq C_{1B}$. We show that for each case and all possible initial states, the state and location of the cache line is the same as $B$ is serialized before a non-speculative load $A$ to the same location; and the timing for the non-speculative access does not change. Figure 7 (left) illustrates that, the eventual cache line state and location changes for all four cases with all initial states possibilities in L1 and L2 are the same for $\Theta$ and $\Phi$.

**Proof of Property 3 (SpecRd overlaps with load/store):**

We use the same proof strategy for Property 2. In this case, $A$ is squashed so $R_A < S_B < I_A$, and the effects should be equivalent to executing just $B$. Figure 7 (middle) shows such equivalence for all cases.

**Proof of Property 2 and 3 (SpecRd overlaps with another SpecRd):**

We consider two SpecRd $A$ and $B$, there are three cases: 1) $A$ and $B$ merge; 2) $A$ purges and $B$ merges; and 3) $A$ purges and $B$ purges. They should be correspondingly equivalent to the execution of: 1) two non-speculative loads serialized according to the merge order; 2) one non-speculative $B$; and 3) no load. Figure 7 (right) shows such equivalence for all cases.

**Explanation of Case 4 of Property 2.** We hope it will provide guidance for understanding other cases. The Case 4 shown in Figure 7 assumes Total-Store-Order (TSO) model, which prevents the reordering of loads. When a write ($B$) is serialized before a non-speculative read ($A$) from a different core, the eventual state in $C_{1A}$ and $C_{1B}$ should be $S$ ($\Theta$). For $\Phi$, if the line is in $S$ or $I$ ($X = S/I$) in $C_{1A}$ and $C_{1B}$ (the case above dashed line), it must be in $S$ or $I$ in $C_2$. So $R_2$ will transition from $X$ to $XSpec$, $C_{1B}$ is not affected. When $B$ is serialized ($S_B$), the line in $C_{1B}$ and $C_2$ both transition to $M$. In $C_{1A}$, it is invalidated. At this point, MCM matters: in TSO, if a load cache line is invalidated before the load retires from the processor, it has to be “replayed”. It is the “Peekaboo” problem discussed in [25]. The replay is needed because otherwise, the load might be reordered with an earlier load—prohibited by TSO. Thus, the SpecRd is re-issued to $C_{1A}$, first reaching $ISpec$ ($C_2$ transitions from $M$ to $MSpec$), and finally reaching $S$ on merge in both $C_{1A}$ and $C_2$.

If the cache line is already in an exclusive state in the write $B$’s cache $C_{1B}$ ($X = M/E$ shown below dashed line), it must be in $I$ in the SpecRd’s cache $C_{1A}$. At $R_A$, SpecRd misses in $C_{1A}$ and $C_2$, forwards it to $C_{1B}$. RCP provides the data but $M/E$ state does not changes (emphasized in red). At $C_{1A}$, $R_A$ changes the state to $ISpec$. After that, when the write is performed ($S_B$), it can still hit in $C_{1B}$—not affected by SpecRd. When SpecRd is merged, the state in both $C_{1A}$ and $C_2$ transition to $S$. In both cases ($X = S/I$ or $X = M/E$), final state and location of the cache line are the same as $\Theta$.

**RCP and memory consistency models (MCMs).** We also use the earlier case to show RCP works with release consistency (RC) with or without write atomicity. In RC, since loads to different locations can be reordered, even if a load cache line is invalidated before it retires from the processor, the load do not need to be replayed. In this case, for $\Theta$ the final state in $C_{1B}, C_{1A}$, and $C_2$ are $M, I, M$, respectively. However, it is not inconsistent with $\Phi$, because, without the load replay, the read $B$ is essentially serialized before the write $A (Rd \rightarrow Wr)$, and the eventual states are the same. In RC, without load replay, it is not possible to have $Wr \rightarrow Rd$.

We show RCP also works with processors (e.g., IBM PowerPC) that do not enforce write atomicity, i.e., stores are visible to different cores at different time. The argument is simple, RCP supports invisible speculative load, which only interacts with stores when it is invalidated. In another word, what matters is write performance w.r.t. individual speculative load, which is always well-defined. Whether there is a single point of global write performance does not affect the functionality of the protocol.

**Remarks:** All proofs consider two instructions, but the security property of the whole program can be inductively obtained. Specifically, we can consider the two-instruction case as the initial case in mathematical induction, then we can assume that these properties hold with a sequence less than $n$ instructions, we need to prove they are true with $(n + 1)$ instructions. The crux of the argument is that, the first $(n - 1)$ instructions satisfy the properties (inductive assumption), and they will produce a state and location setting denoted by $\mathcal{F}_{n-1}$ and $\mathcal{L}_{n-1}$ satisfying the properties. Then the last two instructions $n$ and $(n + 1)$ execute from $\mathcal{F}_{n-1}$ and $\mathcal{L}_{n-1}$, preserving the properties based on our proof.

**Security of SpecBuf.** We show that specBuf cannot be used to create new channels. Referring to Section 4.2, there is a one-to-one mapping between a core’s LQ entry, $LQ[i, j]$, to specBuf entries in L1 $SB_{L1}[i, j]$ and L2 $SB_{L2}[i, j]$. There is no fully associative or set-associative hardware structures, thus it is not vulnerable to cache-based side-channel attacks such as Prime+Probe. In fact, the specBuf organization is exactly the same as InvisiSpec—with the same number of entries—expect the bloom filters in L2’s specBuf and some counters for each entry. In RCP, we make the time to check the bloom filter in L2 constant, so the present/absence information in the specBuf cannot be revealed through the time for the check.

**Case study.** Figure 1 (f) shows the execution of Attack 1 with $P_1$’s SpecRd accessing the line that are probed by the attackers and later squashed. Assuming the line is invalid in all cache component initially, when SpecRd is issued, the state transitions to $ISpec$ and the line is only kept in specBuf in both $C_{11}$ and $C_2$. Before SpecRd is squashed, $P_2$ accesses the line, and misses in both L1 and L2, even if the line is in their specBuf. Thus, the cache line is brought from memory and installed in $C_{12}$ and $C_2$. RCP provides the same latency for $P_2$’s access as if SpecRd of $P_1$ is not performed. In L2, the state transitions to $E$Spec indicating the fact that currently there is one non-speculative copy (in $C_{12}$) and one speculative copy (in $C_{11}$). Next, when SpecRd is squashed, the state in $C_{11}$ transitions locally to $I$ and an L1Purge is sent to $C_2$, which transition the state from $E$Spec to $E$—correctly indicating that there is no speculative copy and still one non-speculative copy. After this, $P_1$’s load will be sent to $C_2$ and served by $C_{12}$ after forwarding—exactly the same as if SpecRd in $P_1$ has not happened. Thus, Attack 1 does not succeed in RCP. Unlike MuonTrap, the state and location of the cache line
after all these accessed are the same as when only \( P_2 \) and \( P_3 \) perform non-speculative accesses.

Figure 1 (g) shows the execution when \( P_1 \)'s SpecRd is committed after \( P_2 \)'s access. After \( P_2 \)'s request, both \( C_{1,2} \) and \( C_{1,3} \) have the line in \( S \) state, and the \( C_2 \) state transitions to \( SS\text{pec} \), indicating that there are multiple non-speculative copies. When SpecRd in \( P_1 \) commits, \( C_{1,1} \) checks with \( C_2 \) and finds that it should transition to \( S \), then sends an \( L1\text{Merge} \) to \( C_2 \). There is only one speculative copy, so \( spec\ core=1 \), after the merge, it becomes 0. Thus, the state transitions from \( SS\text{pec} \) to \( S \) with three non-speculative copies.

Figure 1 (h) shows the execution of Attacker 2 in RCP, in which SpecRd in \( P_2 \) does not stall even if \( P_1 \) (the attacker) controls the dirty copy. According to Figure 5 (a), when a GetSpec is received on \( M \) state in \( C_{1,1} \), it can forward data but does not transition to \( S \). It is the crucial mechanism that allows the execution of SpecRd on remote E/M. When SpecRd is committed, an \( L1\text{Merge} \) will be forwarded to \( C_{1,1} \), at this point, \( M \) will transition to \( S \) and flush the data to \( C_2 \).

7. EVALUATION

7.1 Environment Setup

We implemented RCP protocol in Gem5 [6]. We simulate the single core system under System-call Emulation (SE) mode, and multi-core system under Full System (FS) mode. We compare the performance of RCP with the performance of InvisiSpec (corrected) and CleanupSpec using their public open source codes. For InvisiSpec, we evaluate Futuristic model. For CleanupSpec, we evaluate the scheme for Cleanup FOR L1L2. The simulator configuration is shown in Table 5, which is similar to InvisiSpec, except that the coherence protocol is replaced by RCP.

We choose SPEC CPU2006 [13] and SPEC CPU2017 [7] for single-core evaluation, while using PARSEC 2.1 [5] for multi-core evaluation. For SPEC CPU2006, we use 19 workloads [26] with the reference data-set. For SPEC CPU2017, we run 9 workloads in intrate and fprate suits with reference input size. We forward the execution by 10 billion instructions and simulate 1 billion instructions. For PARSEC, we run 9 of the multi-threaded workload with the simmedium input size. We run all these benchmarks with the setting of 4 cores for the entire region of interest. The overhead of InvisiSpec and CleanupSpec may not be exactly same as stated in their paper because of the different range of benchmarks and different configuration setting, but the trend is similar. We run SPEC2006 under TSO and SPEC2017 under RC.

| Architecture | 1 core (SPEC) or 4 cores (PARSEC) at 2.0GHz |
|--------------|------------------------------------------|
| Core         | 8-issue, out-of-order, no SMT, 32 Load Q entries, 32 Store Q entries, 192 ROB, Tournament branch predictor, 4096 BTB, 16 RAS |
| Private L1-I | 12KB, 64B line, 8-way, 1 cycle RT lat., 1 port |
| Private L1-D | 64KB, 64B line, 16-way, 1 cycle RT lat., 5 ports |
| Shared L2    | 2MB bank, 64B line, 16-way, 8 cycles RT local latency, 16 cycles RT remote latency (max) |
| Network      | 4x2, 1.2GB link width, 1 cycle per hop |
| Coherence    | RCP and MESI |
| DRAM         | RT latency: 50 ns after L2 |

Table 5: Architecture Configurations

7.2 SPEC Analysis

Figure 8 shows normalized execution time overhead of RCP, InvisiSpec and CleanupSpec, normalized to execution time of a non-secure baseline, on SPEC2006 benchmarks under TSO. Over all 19 workloads, RCP on average incurs a slowdown of 3.0%, while CleanupSpec and InvisiSpec incurs a slowdown of 3.2% and 26.5%, respectively. The overheads of RCP are caused by merge/purge operations. Due to different mis-speculation rates, RCP is not always better than InvisiSpec and CleanupSpec. For some applications, e.g., GemSFDFTD, RCP runs slightly faster, because specBuf can eliminate some L1 misses (details in Section 7.3).

Figure 9 shows the results for SPEC2017 under RC (only 14 for CleanupSpec). With similar trends, InvisiSpec and CleanupSpec incur overheads about 12% and 9.4% on average, while RCP achieves the lowest 8.3% on average. Overall, the benchmarks with lower mis-prediction rate, CleanupSpec incurs lower slowdown. For those with higher mis-prediction rate, RCP benefits from merge/purge operations that can be performed concurrently and reduce the overhead. For lbm_r, it has an extremely low mis-prediction rate (0.36%), thus RCP has negligible slowdown and CleanupSpec even has a decent speedup. Technically, CleanupSpec should never lead to speedups, unlike InvisiSpec and RCP. A probable reason is that some supports of InvisiSpec may not have been completely eliminated (CleanupSpec is modified from InvisiSpec). Nonetheless, it shows the first-order trends reasonably.

7.3 PARSEC Analysis

The execution time overheads on multi-core PARSEC workloads are shown in Figure10. Overall, InvisiSpec incurs a 18.3% slowdown in on average under TSO, while cleanupSpec has a 24.2% slowdown. RCP reduces the overhead to 7.4% on average. With the help of the specBuf, RCP increases the hit rate for speculative loads, which leads to slight performance improvement of some benchmarks such as blackscholes and swap. Note that the behavior also exists for InvisiSpec, for blackschole, the “speedup” is quite significant (∼20%). For vips and freq, RCP is the only design that gains speedups. It is due to a combination of the effects of
specBuf and the unique benefit of RCP. A SpecRd can bring a cache line in specBuf, which may have evicted some L1 cache line in baseline execution. If SpecRd becomes safe, such replacement is delayed; otherwise, the replacement will never happen. In both scenarios, normal load may have more hits in L1. While InvisiSpec can also enjoy this effect, the “double” load and the need for excessive “validation” can offset the benefit. In contrast, RCP’s merge/purge—not in critical path—can preserve this benefit. The overheads of CleanupSpec for these two are higher than others because of the high mis-prediction rates.

7.4 Coherence Traffic Overhead

Figure 11 shows the comparison of traffic overhead among RCP, InvisiSpec and CleanupSpec, normalized to the baseline MESI protocol. We measure the traffic overhead by counting the total number of bytes transferred among the cache system and between cache and the main memory. For RCP, we also count the bytes for each type of the message and show their distribution in Figure 11. RCP incurs on average 46% traffic overhead, while InvisiSpec and CleanupSpec incur 40% and 27%, respectively. Coherence traffic overhead of RCP is mainly attributed to PrMerge, PrPurge, and L1Merge messages. For swap, RCP incur slightly less traffic, it is because specBuf may increase hit rate, some traffic to L2 and memory can be eliminated. InvisiSpec and CleanupSpec show the similar behavior. The key observation from the results is that, even with higher additional traffic the performance overhead of RCP is still lower than the other two schemes. It confirms the crucial advantage of RCP: the merge and purge are performed concurrently with processor execution. With coherence decoupled with processor, traffic can be further reduced with protocol optimizations.

8. CONCLUSION

This paper proposes the first Reversible Coherence Protocol (RCP), that enables invisible speculative load. RCP takes a bold approach by including the speculative loads and merge/purge operation in the interface between processor and cache coherence, and allowing them to participate in the coherence protocol. RCP incurs an average slowdown of (3.0%, 8.3%, 7.4%) on (SPEC2006, SPEC2017, PARSEC), which is lower compared to (26.5%, 12%, 18.3%) in InvisiSpec and (3.2%, 9.4%, 24.2%) in CleanupSpec. The coherence traffic overhead is on average 46%, compared to 40% and 27% of InvisiSpec and CleanupSpec, respectively. Even with higher traffic overhead (∼46%) the performance overhead of RCP is lower than InvisiSpec and comparable to CleanupSpec because the coherence actions triggered by the merge and purge operations can be performed in the cache hierarchy concurrently with processor execution.

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