Contact resistance assessment and high-frequency performance projection of black phosphorus field-effect transistor technologies

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Abstract
In this work, an evaluation of the contact quality of black phosphorus field-effect transistors from different technologies previously reported is performed by means of an efficient and reliable contact resistance extraction methodology based on individual device practical characteristics. A good agreement is achieved between the extracted values with the Y-function method used here and reference values obtained with other methods considering internal values as well as with more expensive methods involving fabricated test structures. The method enables a direct evaluation of different steps in the same technology and it embraces the temperature dependence of the contact characteristics. Channel phenomena have no impact on the extracted contact resistance values. High-frequency performance projections are obtained for fabricated devices based on the extracted contact resistance.

Keywords: contact resistance, Schottky barrier, BPFET, AC performance

1. Introduction

Over the past decade, two dimensional (2D) semiconductors have emerged as promising candidates for future generations of nanoelectronic devices, due to their ultrathin bodies and high carrier mobility [1, 2], that are considerably different from those in their bulk parental materials. More recently, black phosphorus (BP), with a direct bandgap of \( \sim 0.3 \) eV in its bulk form and up to \( 2 \) eV for monolayers [3], has shown an excellent electronic efficiency for high performance transistors [3, 4]. Experiments have shown that, for certain device bias and temperature conditions, BP field-effect transistors (FETs) can exhibit an on/off ratio up to \( 10^6 \) and mobility up to 1000 cm\(^2\)/V \cdot s [3]. With its tunable band gap and high carrier mobility, BP is a suitable material to implement transistors for low-power high-frequency applications [5–7].

One of the major challenges in understanding and exploiting the intrinsic charge transport properties in emerging transistor technologies, such as BPFETs, arises from the contact resistance \( R_C \) associated to interfaces between metal and low-dimensional channels such as 2D atomic layers. \( R_C \) is often associated to an energy- and material-dependent potential barrier induced by the interaction between the source and drain contacts and the two-dimensional channel material, as is the case for BP [8]. In these Schottky-like FETs, it is important to understand the contact properties before extracting intrinsic properties of the channel such as a channel resistance \( R_{ch} \) describing the transport phenomena within the device channel. Hence, a reliable and \( R_{ch} \)-independent characterization of \( R_C \) is required.

In general, the total contact resistance \( R_C \) embraces the contribution of the source contact resistance \( R_{C,S} \) and the drain
contact resistance $R_{C,tot}$. In order to ease the study, these resistances are lumped here in a symmetrical disposal such as $R_C = R_{C,S} + R_{C,D}$. The total device resistance $R_{ds}(=V_{DS}/I_D)$ is the sum of channel and contact resistances, i.e., $R_{tot} = R_{ds} + R_C$.

In this work, an $R_C$-extraction methodology based on individual device characteristics is presented in section 2. Contacts of fabricated BPFET technologies are characterized by extracting their corresponding $R_C$ in section 3. $R_C$-enabled discussions regarding the impact of temperature and doping on potential barriers of metal-channel interfaces of some of the studied BPFETs are also included in section 3. A high-frequency performance projection of fabricated BPFETs, enabled by $R_C$ and other device parameters, is also presented. The final part of the work draws some conclusions.

2. Contact resistance extraction

In the literature, values for $R_C$ of BPFETs have been obtained either by means of the fabrication of special test structures [4, 9, 10, 24] or by describing the device behaviour with adjusted models [11–13]. The latter is a technology-specific approach which relies on the fitting parameters of an analytical or compact model (CM) and on the physical thoroughness of the model. The use of conventional extraction techniques in BPFETs, such as 4-point-probe (4PP) methods [24] and the transfer length method (TLM) [4, 9, 10], provides $R_C$ values at the cost of additional process steps and whose reliability depends on a high-yield not reached yet by this emerging technology.

The drift-diffusion-based $Y$-function [14] has been used to extract values of $R_C$ from individual device characteristicics of different 2D [15–17] emerging transistor technologies and without the need of additional test structures. $Y$-function-based methods rely on the relation between the drain current $I_D$ in the linear regime and the square root of the transconductance $g_{ms}(=\partial I_D/\partial V_{GS})$ of a device such as $Y = I_D/\sqrt{g_{ms}}$.

In this work, the electron drain current ($I_D$) at the linear operation is considered as [17, 18]

$$ I_D \approx \frac{\beta V_{GS,eff}}{1 + \theta V_{GS,eff}} V_{DS}, $$

(1)

where $V_{GS,eff} = V_{GS} - V_{th} - V_{DS}/2$ is the effective gate-to-source voltage with $V_{GS/DS}$, the gate-to-source/drain-to-source voltage, $V_{th}$ the threshold voltage, $\theta = \theta_0 + R_C \beta$ is the extrinsic mobility degradation coefficient [14, 19], embracing the mobility degradation inside the channel due to vertical fields $\theta_0$, $\beta = \mu_0 C_{ox} w_g/L_g$ with $\mu_0$ as the low-field mobility, $C_{ox}$ the oxide capacitance, and $w_g$ and $L_g$ the gate width and gate length, respectively.

From equation (1) and by using the $Y$-function and an auxiliary $X$-function ($X = 1/\sqrt{g_{ms}}$), a bias-dependent contact resistance can be obtained as [20]:

$$ R_C = \frac{V_{DS}}{\beta} V_{GS,eff} \left( \frac{XY}{V_{GS,eff}^2} - 1 \right) \left( \frac{1}{V_{GS,eff}} - \theta_0 \right). $$

(2)

Notice that in contrast to other works [5, 16] where a different $Y$-function based extraction method (YFM) has been used in BPFETs, $R_C$ extracted here considers the effect of $\theta_0$, as well as a more complete model for $I_D$, and hence, more accurate and complete information can be obtained by using equation (2) [18, 23].

3. Results and discussion

The development of BPFET technology has been demonstrated by different groups in the literature with fabricated proof-of-concept devices [4–7, 9, 10, 21, 24, 25]. In this section, the YFM discussed above has been applied in order to characterize the contacts of these transistors.

3.1. $R_C$ characterization of fabricated devices

The contacts of different BPFET technologies [4–7, 9, 10] have been evaluated by extracting the corresponding $R_C$ values with the YFM discussed above. Table 1 lists the device geometry of some of the studied technologies [4, 5, 9, 10, 21], as well as the reference contact resistivity $R_{C,ref}$, with $w_g$ as the device gate width, obtained with other methods as reported in the corresponding references. Notice that a different technology implies different device footprints, e.g. gate length $L_g$, architectures and fabricated processes, and hence, a systematic scaling study is not feasible in this work despite the universality of the method presented here. However, doping- and temperature-dependent $R_C$ studies are presented (cf figures 3 and 4).

The experimental transfer characteristics of some of the devices under study (DUT) [9, 13] are shown in figure 1. The drain current obtained by equation (1) with the extracted parameters is also shown within the bias range in which YFM has been applied in each device. The good match between experimental data and equation (1) indicates the validity of the extracted parameters. Similar results have been obtained for the other devices studied in this work. According to the
authors knowledge this verification step has not been previously reported for BPFETs.

Figure 2(a) highlights the $R_C$ extracted values of the different DUTs [9, 10, 13] at different $V_{GS}$. In contrast to the reference values, $R_{C,YFM}$ shows a bias-dependence, due to the contact characteristics, i.e. modulation of potential contact barriers by an electric field. In addition, $R_{C,YFM}$ extracted values are close to the reference values extracted using the TLM-method and CM-method (filled markers in figure 2(a)) [9, 10, 13]. The slight differences between extracted and reference values can be due to an extraction under different bias conditions (see table 1), e.g. the bias point or range at which reference $R_C$ for the 300-nm long device [13] is valid has not been reported.

The ratio between channel resistance and extracted contact resistance indicates the impact of $R_{ch}$ and $R_C$ on the device performance. Figure 2(b) shows this ratio, for the DUTs [9, 10, 13] over the bias range in which $R_C$ has been extracted. $V_{GS,0}$ is the $V_{GS}$ closest to the threshold voltage. If the ratio $R_{ch}/R_C$ is close to 1, it means that both, $R_{ch}$ and $R_C$ contribute similarly to the device total resistance, which is the case for the DUTs included in table 1. [9, 10, 13]. The impact of the contact or channel properties on the device performance can be quantified independently. This is embraced by the extraction method as demonstrated by analyzing the ratio of $R_{ch}$ to the extracted $R_C$ of the 200 nm device [10] with and without boron nitride (BN)-induced potential barriers at the source and drain contacts. As shown also in figure 2(b), $R_C$ dominates the performance of the 200 nm-long device [10] with BN barriers, because they add an additional resistance to the metal-channel interface while the channel properties remain the same. Furthermore, figures 2(a) and 2(b) show that YFM is as reliable as other methods, however, in contrast to the latter, YFM allows the evaluation of different technologies from the $I – V$ characteristics and at different temperatures of individual devices without the need of test structures or an adjustment of a complete set of model parameters.

Figure 3 shows the contact $R_C \cdot w_g$, channel $R_{ch} \cdot w_g$ and total resistivity $R_{tot} \cdot w_g$ of the 200 nm-long devices with and without additional BN barriers at the contacts [10]. Notice that $R_C$ has been extracted for each device at similar transistor operation regions with respect to $V_{GS}$ towards a fair comparison in terms of transport conditions. For both cases, $R_{tot}$ has been obtained using $R_{tot} = V_{DS}/I_D$, $R_C$ by the YFM method, equation (2) and $R_{ch} = R_{tot} \sim R_C$. $R_C$ is higher for the device with additional barrier compared to the barrier-free device. Therefore $R_{tot}$ also increases, which will cause an $I_D$ decrease. The $R_{ch}$ results are almost equal in both devices. This implies that (i) transport phenomena within the channel material have minimum impact on the device performance, in contrast to the phenomena associated with the characteristics of contacts and (ii) the extraction method used here is totally independent of channel phenomena.

Figure 4(a)–(b) shows the extracted $R_{C,YFM}$ with reference values reported over a bias range of a 100 nm-long device and a 170 nm-long device. The reported values ($R_{C,TLM}$) in figure 4(a), are evaluated at a $V_{GS}$-bias range lower than the $V_{GS}$-bias range in this paper, however, by extrapolating the incremental trend of $R_{C,TLM}$ the values of $R_{C,YFM}$ are obtained. The comparison between $R_{C,TLM}$ measured in [9] and $R_C$ extracted by the YFM method at several $V_{GS}$ is shown in figure 4(b), this comparison highlights that the difference between $R_{C,TLM}$ and $R_{C,YFM}$ is minimal within the similar bias range in which both methods have been applied. Figure 4(c), shows the variation of $R_C$ for a BP-device at different temperatures, and it can be concluded that the $R_C$ decreases as the temperature increases, which coincides with an analytical model of a temperature-dependent contact resistance model shown elsewhere [12]. Furthermore, the $V_{DS}$-dependence of $R_C$ reveals the sensitivity of phenomena within the metal-BP interface to lateral electric fields. The contribution at source and drain interfaces of these fields can be either symmetrical or unbalanced, however, this is out of the scope of this study.

The method has been proven to extract the contact resistivity, also for BPFETs with more challenging channel configurations, since $R_{ch}$ has no impact on the $R_C$ extraction in YFM,
such as the device in [24] where the YFM-extracted contact resistivity is of $107 \text{k}\Omega \cdot \mu \text{m}$ which is $\approx 6\%$ close to the reported value of $101 \text{k}\Omega \cdot \mu \text{m}$ (see figure 2(c) in [24]) for $V_{GS}$ in the range of $-53.1 \text{V}$ to $-55.6 \text{V}$.

3.2. $R_C$-based high-frequency performance projection

The $R_C$ extracted for high-frequency BP-FETs [5–7] in figures 5(a)–(c) show that $R_C$ decreases as $V_{DS}$ increases, as well as a larger variation with $V_{GS}$. The latter embraces the potential barrier change due to vertical fields. The $R_C$ values extracted from [5] are shown in figure 5(a), it can be seen that $R_C$ extracted ($\approx 5.6 \text{k}\Omega \cdot \mu \text{m}$) at $V_{DS} = -0.1 \text{V}$ is between the values reported in [5] (see table 1), therefore, this is indicative that the YFM method obtains more accurate data with fewer simplifications, compared to the simplified YFM method used in [5].

The high-frequency performance of bias-dependent BP-FETs can be described by an equivalent small-signal circuit model shown elsewhere [17, 22]. For a symmetrical disposal of source contact resistance and drain contact resistance, i.e. $R_C/2 = R_s = R_d$, the extrinsic cutoff frequency $f_{T,e}$ and the extrinsic maximum oscillation frequency $f_{\text{MAX},e}$ are given by [22]

$$f_{T,e} \approx \frac{g_{m,i}}{2\pi \{C_{gg,i}[1 + g_d,iR_C] + C_{gd,i}(g_{m,i}R_C)\}},$$

(3)

$$f_{\text{MAX},e} \approx \frac{g_{m,i}}{4\pi \sqrt{\Psi_1 + \Psi_2 + \Psi_3}},$$

(4)

where the total gate-to-source capacitance ($C_{gg,i}$) and total gate-to-drain capacitance ($C_{gd,i}$) have been obtained by a simple practical approach towards the evaluation of the impact of $R_C$ over the HF performance, i.e. by using equations (4) and (5) in [22], the experimental intrinsic $f_T$ and $f_{\text{MAX}}$ reported in the corresponding references [5–7, 25] (see table 2) and by assuming bias-independent capacitances within the bias range of interest for this study.

**Table 2. FoMs of different technologies of BPFETs.**

| [Reference] | $f_{T,e}$ (GHz) | $f_{\text{MAX},e}$ (GHz) | $R_{C,\text{ref}} \cdot w_g$ (k$\Omega \cdot \mu $m) |
|-------------|----------------|-------------------------|-----------------------------------|
| [5]         | 6              | 10.72                   | 4.5–6.7 (bias not reported)       |
| [6]         | 8              | 12                      | —                                  |
| [7]         | 2              | 17                      | —                                  |
| [25]        | 37             | 22                      | 6 ($V_{GS} = -0.5 \text{V}, V_{DS} = -1 \text{V}$) |

Figure 3. Contact resistivity, channel resistivity, and device total resistivity of the 200 nm-long transistor, $R_{C,\text{tot}}$ has been extracted from transfer curves in [10] at $V_{DS} = -0.1 \text{V}$. Unfilled markers correspond to a 7 nm thick BP-PMOSFET without boron nitride (BN) tunneling barrier at source/drain. Filled markers correspond to the same device but with bilayer BN tunneling barriers at source and drain.

Figure 4. Contact resistivity of the BP device calculated by equation (2) from transfer characteristics. (a) for a 100 nm-long device [4], dotted line represents a linear extrapolation, (b) for a 170 nm-long device [9], (c) for a 300 nm-long device [13] at different temperatures.
Figure 5. Contact resistivity of high frequency BP devices from different technologies: (a) a 250 nm-long device [5], (b) a 300 nm-long device [6], and (c) a 400 nm-long device [7].

Table 3. Capacitances and gate resistance of different technologies of BPFETs.

| [Reference] | $C_{gg,t}$ (aF) | $C_{gd,t}$ (aF) | $R_C$ (Ω) |
|-------------|----------------|----------------|-----------|
| [5]         | 0.28           | 0.13           | 14.66     |
| [6]         | 168.19         | 83.78          | 12.22     |
| [7]         | 53.8           | 26.5           | 10        |

$R_C$ values have been obtained by using equation (6) in [22] considering the corresponding device geometry. Similarly, $\Psi_1$, $\Psi_2$, $\Psi_3$ have been calculated using equation (9) in [22]. Table 3 shows the bias-independent calculated values for each device in this study. For the intrinsic transconductance $g_{m,t}(= \partial I_D/\partial V_{GS,t})$, obtained from transfer characteristics, and intrinsic output conductance $g_{d,t}(= \partial I_D/\partial V_{DS,t})$, obtained from output characteristics, the intrinsic gate-to-source voltage $V_{GS,t} \approx V_{GS} - I_D R_C/2$ and intrinsic drain-to-source voltage $V_{DS,t} \approx V_{DS} - I_D R_C$, have been obtained by considering the extracted $R_{C,YFM}$ for each device (cf figure 5).

The high-frequency figures of merit (FoM) expressed by equations (3) and (4) have been obtained for BPFET technologies for high-frequency applications: a 250 nm-long device [5], a 300 nm-long device [6] and a 400 nm-long device [7]. FoMs are reported in figure 6. The FoMs in [25] are not analyzed in this study because the YFM method is valid for a three-terminal device (gate, source, and drain), while in [25] two extra terminals are considered (five contacts in total) to induce electrostatic doping both in the source and drain, however, we report these FoMs because the device described in [25] achieved the best $f_{T}/f_{MAX}$ performances for a BPFET technology.

Notice that ($f_{T,e}$, $f_{MAX,e}$), inferred from $R_{C,YFM}$, roughly approximate the reported values of (6, 10.72) GHz [5], (8, 12) GHz [6] and (2, 17) GHz [7]. The obtained $f_{T,e}$ values in figure 6, are comparable with $f_{T}$ reported in [6] at $-1.8 \leq V_{GS} \leq -1.7$ V and in [7] at $-1.2 \leq V_{GS} \leq -0.9$ V. The bias-dependence observed for $f_{T,e}$ and $f_{MAX,e}$ is related to the $V_G$ dependent $R_C$ extracted for each device (cf figure 5).

Interestingly, the highest $f_{T,e}$ has been obtained for the shortest device [5] despite having the highest $R_C$ among the three devices under study (see figure 5). This result can be explained by an outstanding device electrostatics, i.e. the low values of $C_{gg,t}$ and $C_{gd,t}$ associated to the device reported in [5] (see table 3) diminish the impact of $R_C$ on $f_{T,e}$. $R_C$ extracted for the 400 nm-long transistor [6] is the lowest and most bias-independent at $V_{DS} = -0.1$ V of the devices under study. Therefore, the device described in [6] has the most linear $f_{T,e}$ performance among the devices highlighted in figure 6(a), the non-optimal electrostatics of this device [6], i.e. large capacitance values (see table 3), hinders higher $f_{T,e}$ values despite the lower $R_C$ in comparison to [5]. Figure 6(b) shows that $f_{MAX,e}$ in [6] and [7] are close to each other despite a lower $R_C$ has been obtained for the 300 nm-long device [6] in comparison to the largest one [7]. Furthermore, $R_C$ is similar for both devices as shown in table 3. Hence, the large value of the capacitances obtained here for the device in [6] compared to the ones obtained for [7] impedes higher values of $f_{MAX,e}$ for [6]. It is important to highlight that a minimal change in these capacitances together with the $R_{C,YFM}$ formed in the metal-channel interface, can modify the performance of these devices in HF. Therefore, in order to improve the dynamic HF performance of BPFETs, extreme care must be taken with $R_C$ and the device electrostatics. The first parameter strongly influences not only
the magnitude but the $f_{T,e}$ and $f_{\text{MAX},e}$ response over bias, while the latter related parameters can define its value in combination with $R_C$. $R_P$ has not shown an important impact on the HF performance due to a lower sheet resistance of the metal gates as previously pointed out elsewhere [22].

4. Conclusion

The drift-diffusion-based Y-function method has been used here to find the bias dependence of the $R_C$ of different BPFET technologies, without the need of additional test structures or adjustment of a set of parameters, in contrast to other methods, i.e. TLM or CM. In general, extracted $R_C$ values with Y-function are similar to the reference values, obtained with other costly and less straightforward extraction methods. Y-function method also captures the temperature dependence of $R_C$ for a BP-device. Additionally, it has been found that the influence of the contact and channel resistance can be studied since YFM values are not affected by the latter one. Combined with other key parameters, namely, $g_{m0}$, $g_{ds}$, $R_P$ and intrinsic capacitances, it is possible to get the RF FoMs such as $f_{T,e}$ and $f_{\text{MAX},e}$ which are usually strongly influenced by $R_C$, especially at short channel lengths. YFM method is applicable to obtain $R_C$ at different biases, potential contact barriers and temperature ranges, which means that it is an efficient and reliable methodology for data extraction based on the individual DC characteristics of BPFETs.

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