Versatile sputtering technology for Al$_2$O$_3$ gate insulators on graphene

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Abstract
We report a novel, sputtering-based fabrication method of Al$_2$O$_3$ gate insulators on graphene. Electrical performance of dual-gated mono- and bilayer exfoliated graphene devices is presented. Sputtered Al$_2$O$_3$ layers possess comparable quality to oxides obtained by atomic layer deposition with respect to a high relative dielectric constant of about 8, as well as low-hysteresis performance and high breakdown voltage. We observe a moderate carrier mobility of about 1000 cm$^2$V$^{-1}$s$^{-1}$ in monolayer graphene and 350 cm$^2$V$^{-1}$s$^{-1}$ in bilayer graphene, respectively. The mobility decrease can be attributed to the resonant scattering on atomic-scale defects, likely originating from the Al precursor layer evaporated prior to sputtering.

Keywords: graphene, high-κ dielectric, atomic layer deposition, sputtering

1. Introduction
Graphene is a single-atom-thick layer of carbon arranged in a honeycomb crystal lattice. One of its most important features is the relatively easy control over the charge carriers, typically realized by an electrostatic gate [1]. Because of this property and the high carrier mobility, graphene is predicted to be the future material in semiconductor industry [2] and quantum resistance metrology [3]. Consequently, graphene has been intensively studied both theoretically and experimentally. Since the beginning of exfoliated graphene research, thermally oxidized silicon is successfully used as both the support and back-gate insulator for graphene [4]. However, a great demand for alternative technologies has emerged when it became clear that epitaxially grown graphene on SiC may fulfill industrial requirements [5]. Moreover, to explore effects occurring in p–n junctions [6, 7], electron waveguides [8] or single-electron transistors [9], high-quality dielectric material is required to form efficient gates for these devices. To date, the major efforts of graphene top-gate fabrication are focused on utilizing HfO$_2$ and Al$_2$O$_3$ as high-κ materials in atomic layer deposition (ALD) facilities [10, 11]. ALD may provide a high-quality dielectric with a precisely defined thickness. On the other hand, due to the hydrophobic behavior of graphene, ALD may result in non-uniform material deposition [10]. To overcome this problem, an additional technological step is introduced, in which the graphene surface is pretreated before the fabrication of main dielectric [11]. Recently, it has been shown that deposition and subsequent oxidation of 1–2 nm of aluminum sufficiently prepares the graphene surface to the ALD process and leads to a more uniform Al$_2$O$_3$ dielectric coverage [11–13]. In this work we employed the same approach, but instead of utilizing ALD we used sputtering, which is much simpler and economically more favorable than ALD.

2. Fabrication
Graphene samples were prepared in a standard procedure. Graphene flakes were exfoliated from natural graphite onto Si/SiO$_2$ and shaped into a Hall bar geometry using e-beam lithography with Ar/O$_2$-ion etching. Then Ti/Au contacts (10 nm/50 nm) were evaporated. In the next process phase, to fabricate top gates, samples were coated by poly(methyl methacrylate), and masks for Al$_2$O$_3$ layers were made by e-beam lithography. Next, 2 nm of aluminum was thermally evaporated at a rate of 0.1 nm s$^{-1}$. The aluminum fully oxidized after the samples were removed from the chamber.
and acted as a protection layer during the subsequent Al₂O₃ oxide deposition. In this step, a 26-nm-thick Al₂O₃ layer was sputtered on the samples by an RF sputtering process from a pure Al₂O₃ target using a power of 350 W. After sputtering the Al₂O₃ layer the samples were heated to anneal the dielectric internal structure. This procedure has been carried out in a sputtering chamber by placing the samples near a target heated to about 375 °C for 1 min. Then the samples were cooled down to room temperature within about 10 min. An acetone lift-off was performed for 12 h to define the final dielectric shape. In the last fabrication phase, top-gate electrodes were created in the same fashion as the graphene contacts. In the described approach the dielectric area was made larger than the graphene sheet and the top-gate electrode contacts. In addition, we applied this layout to all Al₂O₃ samples. Further reduction of this safety distance should be possible by optimizing the lithography process. In addition, we successfully deposited a conformal dielectric layer onto a SiC substrate with an epitaxially grown graphene [14] using the same Al₂O₃ oxide technology, as a preliminary experiment before fabrication of fully functional top gates.

3. Results and discussion

To locally investigate the quality of the dielectric layers, we employed atomic force microscopy (AFM) imaging using a Nanostation II AFM by SIS (now N8 Neos by Bruker) in the intermittent contact mode (tapping mode). In addition to the topography image, we have simultaneously recorded the phase shift map of probe vibrations (the phase shift between the mechanical excitation of the cantilever base and the resulting mechanical oscillation of the cantilever tip), which allows mapping of the local material inhomogeneities on the surface. Figures 1(a) and (b) show an AFM image and a line profile of Al₂O₃ deposited on exfoliated graphene, whereas figures 1(e) and (f) depict an AFM image and a profile of Al₂O₃ on SiC. For the latter sample we omitted the annealing step at 400 °C. All samples exhibited continuous oxide layers with a mean rms surface roughness of about 0.6 nm. For annealed samples we observed, in both topography and phase shift images, distinct but sparse features of a maximum lateral size of approximately 20 × 20 nm² and a depth of approximately 4 nm (insets (c) and (d) of figure 1(a)). AFM data analysis revealed a defects density of about 0.16%. Such features were not observed in unannealed samples, and we therefore conclude that the annealing procedure introduced contaminations, probably originating from the environment. On the other hand, we cannot unambiguously exclude the formation of pinhole defects. In this case, small but abrupt pits may distort AFM cantilever vibrations and produce topography and phase shift artifacts. These features, however, are shallow and do not introduce Al₂O₃ discontinuities.

To assess the effect of the top-gate dielectric on graphene quality, we employed Raman spectroscopy. Raman spectra were acquired using a LabRAM ARAMIS micro-Raman spectrometer (Horiba Jobin Yvon) equipped with a thermoelectrically cooled CCD detector (−70 °C) and 100× objective (NA 0.90). The graphene samples were excited by a frequency-doubled Nd:YAG laser at 532 nm wavelength. Figure 2 shows the Raman spectra of exfoliated monolayer graphene on SiO₂ covered by Al₂O₃ (red trace) and of an uncovered monolayer graphene flake on SiO₂ (black trace). The spectrum of Al₂O₃-covered graphene is dominated by the D peak at ~1345 cm⁻¹ arising from
Figure 2. Raman spectra of a graphene device on SiO$_2$ substrate without (black line) and with (red line) Al$_2$O$_3$ dielectric sputtered on the top surface.

Figure 3. (a) Graphene resistivity as a function of applied top-gate and back-gate voltages (lower black and upper red traces, respectively). Inset (b) presents a fabricated graphene Hall-bar and an electrical connection scheme.

Figure 4. Resistivity maps of graphene (a) and graphene bilayer (b) as a function of top-gate and back-gate voltages. Transport measurements were carried out in the four-terminal configuration in a vacuum of $\sim 10^{-5}$ mbar at room temperature, applying DC current of 1 $\mu$A.

Transport measurements were carried out in the four-terminal configuration in a vacuum of approximately $10^{-5}$ mbar at room temperature (RT), and some of the samples were also characterized at 1.6 K. In further calculations we extracted graphene resistivity defined as a four-terminal resistance multiplied by a geometrical factor $w/l$, where $w$ and $l$ are Hall bar widths and voltage contact distances, respectively, for all measured devices. Figure 3(a) presents a typical dependence of resistivity on the top-gate and back-gate voltages for a monolayer graphene device. The respective counter gate was kept at the ground potential. The experimental setup is schematically depicted in inset (b) of figure 3. To extract quantitative information about the electronic properties, the experimental data were fitted by the expression $\rho(n) = 1/\mu en + \rho_0$, where $\mu$ is the field-effect mobility, $e$ is the elementary charge, $n$ is the graphene carrier concentration and $\rho_0$ is the residual resistivity [19].

The carrier concentration was estimated from the formula $n^2 = n_0^2 + [C_G(V_G - V_G0)/e]^2$, where $n_0$ is the residual carrier concentration, $C_G$ is the gate capacitance per unit area, $V_G$...
and $V_{G0}$ are the gate voltage and voltage at the charge neutrality point (CNP), respectively. We ignored the quantum gate capacitance contribution in our model [12]. As shown in figure 3(a), we have produced an excellent fit to the experimental data. Residual carrier concentrations for the top-gate and back-gate curves were similar, about $5.5 \times 10^{11}$ and $5.9 \times 10^{11}$ cm$^{-2}$, respectively, and the residual resistivity values were about 1.4 k$\Omega$ in both cases. The mobility was about 10% higher when extracted from the top-gate dependence than from the back-gate dependence of resistivity, the values reaching 1100 and 1000 cm$^2$ V$^{-1}$ s$^{-1}$, respectively. For bilayers, the residual carrier concentrations were on the order of $1.5 \times 10^{13}$ cm$^{-2}$. While the residual carrier concentrations of top-gated samples were practically the same as those of samples fabricated in the same fashion but without top gate, we observed a significant reduction of carrier mobility and a dramatic rise of residual resistivity in the former case. Samples without top gates typically showed a mobility of 3000–5000 and 1000–1500 cm$^2$ V$^{-1}$ s$^{-1}$ for monolayer and bilayer graphene, respectively, and the residual resistivity was typically below 300 $\Omega$. Al$_2$O$_3$-covered structures, however, had mobilities around 1000 cm$^2$ V$^{-1}$ s$^{-1}$ for monolayer and 350 cm$^2$ V$^{-1}$ s$^{-1}$ for bilayer graphene, while their residual resistivity was in the range of 1.3–1.6 k$\Omega$. These observations agree with the presence of the D and D’ peaks in the Raman spectra, as the measured values are independent of graphene carrier concentration and can be attributed to short-range, resonant carrier scattering on lattice defects [18, 19]. It has also been shown that resonant scatterers are responsible for limiting the graphene mobility, which would explain the low mobility in our top-gated devices [20]. A further improvement of the fabrication process of Al$_2$O$_3$ top gates, for devices requiring high carrier mobility like transistors or quantum resistance standards, might be achieved by covering graphene sheets with a thin buffer layer before the oxide formation. This additional layer would protect graphene against atomic-scale deformations during dielectric deposition [21]. However, in applications utilizing other electrical properties of graphene, such as graphene memory devices, this auxiliary fabrication step may be omitted [22]. Furthermore, it was reported that even the deposition of the top coating may significantly reduce the mobility [23, 24]. This result suggests that one may need to optimize the formation of this layer, as it makes a direct contact with the graphene sheet. The subsequent Al$_2$O$_3$ sputtering procedure should bring only a minor contribution to the mobility decrease in graphene.

Figures 4(a) and (b) present the resistivity maps of monolayer and bilayer graphene as a function of top-gate and back-gate voltages. Only a linear shift of the CNP is observed for the monolayer graphene device, whereas in the bilayer a pronounced rise of resistivity at CNP for increasing opposite top-gate and back-gate voltages clearly indicates a gap opening between the valence and conduction bands [25]. In the analysis of dual-gate measurements the carrier concentration formula is modified to $n^2 = \frac{n_0^2}{\tau_{BG}} + \frac{C_{BG}(V_{BG} - V_{BG0})}{e + C_{BG}(V_{BG} - V_{BG0})/e}$, where subscripts TG and BG denote the top gate and back gate, respectively [26]. From the CNP slope $\tan(\alpha) = C_{BG}/C_{TG}$, we estimated $C_{TG}$. From the known thickness (300 nm) and dielectric constant (3.9) of the SiO$_2$ back-gate insulator we calculated $C_{BG} = 1.1 \times 10^{-4}$ Fm$^{-2}$ and from the slopes $\tan(\alpha_m) = 1/20$ and $\tan(\alpha_e) = 1/23$, $C_{TG} = 22 \times 10^{-4}$ Fm$^{-2}$ and $C_{TG} = 25.3 \times 10^{-4}$ Fm$^{-2}$ for mono and bilayer devices, respectively. Based on the AFM estimation of oxide thickness as about 28 nm we then calculated an effective Al$_2$O$_3$ relative dielectric constant of 7.3 for the monolayer graphene device shown in figure 2(a) and 8.4 for the bilayer device shown in figure 4(b). These values prove the very high quality of the Al$_2$O$_3$ dielectric layers in our devices, which is comparable to the best results reported.
for ALD-made $\text{Al}_2\text{O}_3$, where effective dielectric constants ranged from 6 to 8 [12, 27, 28].

An imperfect structure of the dielectric layer leads to the charge transfer within the oxide bulk, but this may also happen at the oxide/graphene interface. This charge transfer has a strong influence on the electronic transport in graphene, often resulting in a resistivity hysteresis. Therefore, we studied the hysteretic behavior of top-gated samples at RT and 1.6 K (figure 5) to obtain additional qualitative information about the sputtered oxide. Only a negligible hysteresis of less than 60 mV of top-gate voltage and $\sim 1\%$ of resistivity change at the CNP was observed when the top-gate voltage was kept in the range of $\pm 2$ V at room temperature, indicating a low density of interface states. At low temperature (figure 5(e)) the low-hysteresis performance was maintained up to $\pm 4$ V (figures 5(f) and (g)). We attribute this hysteretic behavior to charge trapping in the oxide layer. For a negative top-gate voltage, after exceeding a threshold of about $-4$ V at low temperature, holes from the bilayer graphene become trapped, and this process results in electron doping of the graphene sheets. This in turn weakens the top-gate efficiency of inducing carriers, and also shifts the CNP towards lower voltages due to additional electron doping. Analogously, a positive top-gate voltage exceeding the threshold value shifts the position of CNP to higher voltages. At room temperature, for top-gate voltages below the trapping threshold, however, the hysteresis had an opposite direction. This may happen when the electrostatic potential around the graphene is altered, e.g. by changing dipole orientations in oxide layers due to an applied external electric field [29]. We typically observed RT $\text{Al}_2\text{O}_3$ dielectric breakdown voltages of about $\pm 9$ V, whereas at low temperature the safe top-gate voltage range extended up to about $\pm 19$ V. This means that the breakdown in the 28-nm-thick oxides occurred for an electric field of approximately $0.32$ V nm$^{-1}$, a value comparable to that of $\text{SiO}_2$ at RT [29].

4. Conclusions

In summary, we have presented a simple $\text{Al}_2\text{O}_3$ sputtering process in graphene gating technology. In terms of low-hysteresis performance, high breakdown voltage and high effective dielectric constant, the quality of the dielectric layers was comparable to the best results obtained with the ALD process. While we report a deterioration of the graphene mobility due to the resonant scattering on atomic-scale defects, we also believe that there is a room for technology improvements. In further experiments, and when high mobility is crucial, one may introduce a buffer dielectric layer between graphene and the sputtered oxide, optimize deposition of the Al precursor layer, and/or optimize the oxide post-processing annealing procedure.

While preparing this article we became aware of the work [30]. The authors report significant mobility decrease in graphene devices after formation of a 2 nm-thin oxide layer by Al oxidation, which fully supports our experimental results.

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