Accelerator-Aware Pruning for Convolutional Neural Networks

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Abstract—Convolutional neural networks have shown tremendous performance in computer vision tasks, but their excessive amount of weights and operations prevent them from being adopted in embedded environments. One of the solutions involves pruning, where some unimportant weights are forced to be zero. Many pruning schemes have been proposed, but have focused mainly on the number of pruned weights. The previous pruning schemes hardly considered ASIC or FPGA accelerator architectures. When the pruned networks are run on the accelerators, the lack of architecture consideration causes some inefficiency problems including internal buffer mis-alignment and load imbalance. This paper proposes a new pruning scheme that reflects accelerator architectures. In the proposed scheme, pruning is performed so that the same number of weights remain for each weight group corresponding to activations fetched simultaneously. In this way, the pruning scheme resolves the inefficiency problems. Even with the constraint, the proposed pruning scheme reached a pruning ratio similar to that of the previous unconstrained pruning schemes not only in AlexNet and VGG16 but also in the state-of-the-art very-deep networks like ResNet. Furthermore, the proposed scheme demonstrated a comparable pruning ratio in slimmed networks that were already pruned channel-wise. In addition to improving the efficiency of previous sparse accelerators, it will be also shown that the proposed pruning scheme can be used to reduce the logic complexity of sparse accelerators.

Index Terms—Deep learning, convolutional neural networks, neural network pruning, neural network accelerator

I. INTRODUCTION

CONVOLUTIONAL neural networks (CNNs) are attracting interest in the fields of image recognition [1]–[5], object detection [6]–[10], and image segmentation [11]. Although they provide great performance for computer vision tasks, there are some obstacles before they can be adopted in embedded environments. A CNN usually requires an excessive amount of weight storage and arithmetic operations. For fast processing and low power consumption under these requirements, ASIC or FPGA accelerators have been proposed [12]–[18], but the amount of weights and operations is still a major concern. The amount of weights can be reduced by network pruning [19]–[33], where some unimportant weights are forced to be zero. Multiplication with zero is meaningless, so reduction in operation amount can be expected, too. Various pruning schemes have been proposed. Some of them prune the weights without a constraint [19], [20], and others prune the weights along the neural network structures. It is known that a larger part of the weights can be pruned in fully connected layers than in convolutional layers. However, pruning convolutional layers can save more energy and reach higher throughput [21]. Since the operation structure of the convolutional layers is more complex than that of the fully connected layers, the pruning of the convolutional layers is more varied [22]–[32].

The pruned networks can be executed on some ASIC or FPGA accelerators that can exploit the weight sparsity. The EIE proposed in [34] used the sparsity of weights generated by the pruning algorithm of [20], but the architecture only processes fully-connected layers. The EIE architecture was modified for a long short-term memory (LSTM) network to become the ESE architecture [35]. Cambricon-X is an architecture that can exploit the weight sparsity in the convolutional layers [36]. SCNN proposed in [37] exploits both the weight sparsity and activation sparsity for convolutional layers. In the ZENA proposed in [38], operating efficiency was reached by skipping zero weights and activations.

Despite the various pruning schemes and accelerators, it is hard to efficiently utilize the performance of the ASIC or FPGA accelerators with pruned networks. The previous pruning schemes were developed without considering accelerator adoptability. They mainly focused on the amount of weights that can be pruned away. Pruning with no constraints creates irregular patterns in the remaining non-zero weights. The irregular pattern causes some inefficiency when the pruned networks are performed on the sparse accelerators. The misalignment of the activation fetching and the weight fetching requires padding zero insertion. The processing elements (PEs) process different numbers of weights, so some PEs need to wait for other PEs to complete. To alleviate this problem, some accelerators use complex structures. For example, Cambricon-X uses very wide (256×16-bits width) memory and very-wide (256-to-1) multiplexers (MUXs).

This paper proposes a new approach, a pruning algorithm considering the accelerator architecture. There can be various architecture consideration points, this paper will focus on the activation groups fetched and processed simultaneously in a PE and the number of remaining weights for each group. Those points are related with some critical parameters in an accelerator design including the number of multipliers and the width of the internal weight buffer. In the proposed algorithm, pruning is applied to weight groups, each of which corresponds to an activation group, and after pruning, a fixed
number of weights remain in a group. Since the pruning is applied to a weight group aligned with the operating boundary of a PE, the scheme can resolve the mis-alignment problem, removing the waste of the internal buffer or multipliers. The pruning group can be adjusted to reduce the data selection and indexing logic complexity. Furthermore, since the remaining non-zero weights are distributed evenly, the load-imbalance problem can be solved naturally.

This paper is organized as follows. Section II explains CNNs, the previous pruning schemes, and the accelerator architectures. The accelerator-aware pruning is proposed in Section III, and the experimental results are shown in Section IV. Section V makes the concluding remarks.

II. CNN AND PRUNING

A. CNN

A CNN usually consists of many convolutional layers and a few fully-connected layers. Between the layers, there are activation layers like rectified linear units (ReLU), pooling layers, and batch-normalization layers. It is known that the convolutional layers occupy more than 90% of the arithmetic operations. Since the fully-connected layers require a lot of weight storage, recent CNNs have tended to have just one fully-connected layer [3], [4] or none [5].

The operation in a convolutional layer is as follows:

\[
fo(m, h, w) = \sum_{c=0}^{K-1} \sum_{i=0}^{K-1} w(m, c, i, j) \times fi(c, S \times h + i, S \times w + j),
\]

where \(fo(m, h, w)\) is the activation of row \(h\) and column \(w\) in output feature map \(m\), and \(fi(c, y, x)\) is the activation of row \(y\) and column \(x\) in input feature map \(c\). In the equation, \(C\) is the number of input feature maps or channels, \(K\) is the spatial size of the kernel, and \(S\) is the stride size. The \(w(m, c, i, j)\)'s are the convolution weights. Fig. 1 shows the structure of the weights consisting of \(M\) filters with spatial size \(K \times K\) and depth \(C\).

For ease of discussion, some axes are defined. The channel axis of the input activations is \(fi(c, y, x)\)'s with the same \(y\) and \(x\). Similarly, the channel axis of the weights is \(w(m, c, i, j)\)'s with the same \(m, c, i, j\). The spatial axis is \(fi(c, y, x)\)'s with the same \(c\) or \(w(m, c, i, j)\)'s with the same \(m\) and \(c\). The filter axis is \(w(m, c, i, j)\)'s with the same \(c, i, j\). Fig. 1 shows the weights along each axis.

B. Pruning

The pruning of neural networks removes some unimportant weights or nodes, to reduce the amount of storage and operations. The early works are presented in [29]–[31]. Recently, pruning in CNNs was proposed in [19], whose pruning results are summarized in Table I. The table shows the ratio of the pruned weights at the first convolutional layer, the other convolutional layers, the first and second fully-connected layers, and the last fully-connected layer of AlexNet and VGG16. The quantization with indirect indexing and Huffman coding were added in [20], and a special architecture for the pruned fully-connected layers was proposed in [34]. The pruning scheme can prune many weights but shows irregularity in the pruned pattern. Moreover, the corresponding accelerator architecture can only deal with the fully-connected layers. The energy-aware pruning scheme proposed in [21] focuses on the convolutional layers since the convolutional layers consume more energy. However, the regularity of the pruning pattern was not considered in this work, either.

The regularity of the pruning has been considered in some other studies [22]–[31]. The pruning schemes of these studies can be categorized as channel-wise, filter-wise, and shape-wise pruning as shown in Table II. For example, in the channel-wise pruning, all of the weights in a channel, \(w(\cdot, n, i, \cdot)\)'s, are pruned or not at all. These pruning schemes are called structured pruning whereas the pruning schemes with no constraint like [19], [20] are called unstructured pruning.

Some pruning schemes target a General-Purpose Graphic Processing Unit (GPGPU). In a GPGPU implementation, the convolution is usually transformed into a matrix multiplication. By removing columns in the transformed weight matrix, the amount of operations can be reduced [28]. A column in the weight matrix corresponds to the weights, \(w(\cdot, n, i, j)\)'s, so this scheme can be thought of as a shape-wise pruning. A strided version was proposed in [29].
C. Neural Network Accelerators

Some ASIC or FPGA accelerator architectures have been proposed for unpruned, dense CNNs, which will be called dense architectures. An accelerator usually consists of several processing elements (PEs), each of which has a single multiplier or many multipliers. In a PE with many multipliers, the multipliers may multiply multiple weights and multiple activations (MWMA), multiple weights and single activation (MWSA), or single weight and multiple activations (SWMA). The MWMA and MWSA structures are shown in Fig. 2, where \( N_{\text{PE}} \) PEs operates in parallel. With the same naming convention, a PE with a single multiplier can be called a single weight and single activation (SWSA) structure.

If a PE has multiple multipliers, it is important to fetch the operands of the multipliers simultaneously. In this paper, a fetching group means the activations or weights that are fetched and processed simultaneously in a PE. If the size of a fetching group is \( N_{\text{par}} \) and the number of multipliers in a PE is \( N_{\text{mul}} \), \( N_{\text{par}} \) is usually equal to \( N_{\text{mul}} \). The weights and activations are usually fetched from the internal buffers, but the buffers are not drawn in the figure.

The PE structures can be further categorized by the axis that the weight and activation fetching groups follow. For example, DianNao\cite{12} adopts the MWMA structure where the multiple weights and activations are fetched along the channel axis. A process example of such an architecture is shown in Fig. 3. A part of the input activations along the channel axis are fetched with a part of the kernel weights and multiplied. The multiplication results are summed and accumulated to be one output activation.

The MWSA structure is adopted in Cnvlutin \cite{13} to exploit the sparsity of the input activations. The multiple weights are fetched along the filter axis. The Cnvlutin architecture skips the MAC operations of zero valued input activations. The outputs of the multiplications in PEs are gathered to \( N_{\text{par}} \) \( N_{\text{PE}} \)-input adder trees. The architectures proposed in \cite{14}–\cite{17} adopt MWMA-structured PEs, and some of them fetch the activations and weights along the spatial axis \cite{16}, \cite{17}.

D. Sparse Accelerator Architectures

The architectures in Fig. 2 can be modified to exploit the weight sparsity, which will be called sparse architectures. In such architectures, only non-zero weights are stored in the weight memories to save weight storage. An example of the sparse MWMA structure is shown in Fig. 4, where \( N_{\text{par}} \) activations are fetched simultaneously. \( N_{\text{par}} \) is usually larger...
than the number of multipliers, $N_{\text{mul}}$, since some weights are zero and multiplications with zero weights are meaningless. Multipliers receive non-zero weights and their corresponding activations. Selecting the $N_{\text{mul}}$ activations from the $N_{\text{par}}$ fetched ones requires $N_{\text{mul}} \cdot w$ 256-to-1 MUXs, where $w$ is the bit-width of the activations. To select a proper activation, a non-zero weight is stored with an index, which is drawn as a grey rectangular in Fig. 4. A process example of the sparse MWMA PE structure is illustrated in Fig. 5, where non-zero weights are marked with a grey color. In the figure, the upper MUX selects the second activation from the front, and the lower one selects the fifth one.

As an example of such sparse architectures, Cambricon-X consists of PEs of the sparse MWMA structure with $N_{\text{par}} = 256$ and $N_{\text{mul}} = 16$. In the architecture, 256 activations are fetched simultaneously, and 16 activations are selected from them. For the selection, there are $16 \cdot w$ 256-to-1 MUXs for each PE, and the MUXs are gathered into a block called IM to reduce the number of wires between blocks.

In those sparse architectures, less weights are usually fetched than activations because only non-zero weights are necessary. For ease of discussion, however, the weight fetching group is defined to include all the zero and non-zero weights corresponding to an activation fetching group. If the number of non-zero weights in a weight fetching group is larger than $N_{\text{mul}}$, the weights are fetched and processed through several cycles with the same activation group. In Fig. 5, one more cycle is required to process the third non-zero weight. If the number of non-zero weights for a weight fetching group is $N_{\text{non-zero}}$, it takes $\lceil N_{\text{non-zero}} / N_{\text{mul}} \rceil$ cycles for a PE to process the activation and weight fetching group.

Other PE structures have been used in some sparse architectures, too. EIE [34] and ESE [35] are sparse architectures for sparse fully-connected layers. To exploit the irregular pattern of sparse weights, they exploit SWSA structured PEs. ZENA [38] also adopts SWSA structured PEs and skips both of zero-valued activations and weights. SCNN [37] has multiple multipliers in a PE, but exploits a special structure of Cartesian Products. In the structure, all of the fetched non-zero activations are multiplied with all of the fetched non-zero weights. The multiplication results are delivered to proper output accumulators.

### E. Previous Pruning Scheme and Accelerator Architecture

The previous unstructured pruning schemes like [19] could reach high pruning ratio, but they rarely result in pruned networks that fit sparse accelerator architectures well. The main reason is the non-uniform distribution of the non-zero weights left after pruning, especially the number of non-zero weights, $N_{\text{non-zero}}$, for each weight fetching group.

This non-uniform distribution can cause a mis-alignment between the activations and weights required for multiplications. In an accelerator with MWMA PEs, the multiplier operands should be fetched simultaneously. When $N_{\text{par}}$ activations and $N_{\text{mul}}$ non-zero weights are fetched from the internal buffers, it is not guaranteed that every fetched weight can find its counterpart in the fetched activations. Another activation fetching group may have to be fetched for the process of the weights.

To solve this mis-alignment problem, Cambricon-X introduces the padding-zero scheme, where padding-zeros are inserted so that the number of non-zero weights and padding-zeros for each activation fetching group is always a multiple of $N_{\text{par}}$, 16. The padding zeros, however, not only waste the internal weight buffer but also cause another inefficiency. The number of total padding zeros would be smaller with a larger $N_{\text{par}}$. This seems one of the reasons that Cambricon-X uses a very large $N_{\text{par}}$ compared to $N_{\text{mul}}$. For a usual pruning ratio of 75% in convolutional layers [19], $N_{\text{par}} = 64$ may be enough for $N_{\text{mul}} = 16$, but Cambricon-X uses $N_{\text{par}} = 256$. Due to the large $N_{\text{par}}$, the activation selection part, the IM
block, has very wide, 256-to-1, MUXs. Since the number of the MUXs is also large, 16·w 256-to-1 MUXs per PE, these wide MUXs cause a large IM block area, which occupies more than 30% of the total chip area. The large $N_{\text{par}}$ also requires a very-wide (256·w bit-width) internal activation buffer. Such a wide memory usually induces a larger area than a square-shaped memory.

Furthermore, the load balance between PEs is also a problem. A PE processes an activation fetching group for $\lceil N_{\text{non-zero}}/N_{\text{mul}} \rceil$ cycles. Because of the diversity of $N_{\text{non-zero}}$, the number of cycles will vary, too. This may cause a problem in some architectures like DianNao and Cambricon-X, which share the fetched activations between PEs to reduce the required bandwidth between the internal buffers and the external memories. If some PEs complete the process of the fetched activations early, the PEs need to wait for the other PEs to finish. The load-imbalance problem is also a major concern in accelerators with a weight serial structure like the SWMA and SWSA structures, where the zero weights are skipped [35], [38].

There are few studies on pruning with considering the divergent distribution of remaining non-zero weights. The reference [33] considers the distribution of non-zero weights, but deals with only fully-connected layers. Furthermore, the target was to reduce the width of ternary weight coding, so the accelerator architecture was not considered. A load-balance-aware pruning was proposed in [35], which prunes the weights so that the total number of nonzero weights processed in a PE is balanced with that in another PE. However, the pruning scheme was only proposed for fully connected layers, and the accelerator architecture discussion is insufficient, too. In contrast, the proposed scheme, which will be presented in the next section, is closely related to accelerator architectures, resolving all of the mentioned inefficiency problems. Furthermore, my scheme focuses on both the convolutional layers and the fully-connected layers.

III. ACCELERATOR-AWARE PRUNING

In this section, I will propose an accelerator-aware pruning algorithm, which will generate a more regular non-zero weight pattern that fits accelerator architectures well. There can be various architecture consideration points, and this paper will concentrate on two parameters, the activation and weight fetching group and the number of non-zero weights left for the weight group. The two parameters are closely related to accelerator architectures. The size of the activation and weight fetching group determines the internal buffer widths, and the number of non-zero weights is associated with the required number of multipliers and the processing cycles. The previous pruning schemes do not consider these points, creating irregular distribution of the non-zero weights and the problems mentioned in the previous section. I will discuss the pruning for the architectures mentioned in the previous section, but the algorithm is not limited to the architectures.

A. Proposed Accelerator-Aware Pruning Scheme

In the proposed pruning scheme, the weights are pruned within the weight fetching groups so that the number of remaining non-zero weights, $N_{\text{non-zero}}$, is uniform for all of the weight fetching groups. The accelerator in Fig. 5 for example, simultaneously fetches and processes an activation fetching group consisting of eight activations along the channel axis. The $N_{\text{non-zero}}$ for the corresponding weight fetching group is three in the figure. However, there is no guarantee about $N_{\text{non-zero}}$ in the previous pruning schemes. $N_{\text{non-zero}}$ can be two or four in another weight fetching group. Even zero or the size of a weight fetching group is possible. In contrast, the proposed scheme leaves a fixed number of non-zero weights for all the weight fetching groups as shown in Fig. 6. In the figure, every weight fetching group has six weights pruned away and two non-zero weights left ($N_{\text{non-zero}} = 2$), which are marked by white and grey colors, respectively.

The result of the proposed pruning scheme can be applied to the previous sparse accelerators, resolving the inefficiency problems mentioned in the previous section. The misalignment problem in the sparse MWMA and MWSA structures will be solved if the number of remaining non-zero weights per group is set to be a multiple of $N_{\text{mul}}$. This alignment would make the padding zeros obsolete in Cambricon-X. Furthermore, the proposed scheme can solve the load-imbalance problem, one of the main concerns in the weight serial structures, too. Every weight fetching group has the same number of remaining non-zero weights, so the number of weights for a PE to process is naturally balanced if every PE processes the same number of weight fetching groups. Every sparse architecture mentioned in the previous section can benefit from the proposed pruning scheme.
B. Accelerator Complexity Reduction

In addition to improving efficiency in the previous sparse architectures, the proposed scheme can also be used to reduce accelerator complexity, especially the indexing and activation selection logic. To deal with the irregular distribution of non-zero weights by the previous pruning schemes, Cambricon-X has very wide (256-\*w-bit width) activation buffers and very wide (256-to-1) MUXs in the activation selection logic, as mentioned in Subsection II-E. The input width of the MUXs can be narrowed by the proposed pruning scheme, simplifying the activation selection logic. First, every weight fetching group is divided evenly into m sub-groups, which will be called pruning groups. The size of a pruning group, \( g \), will be \( N_{par}/m \). Then the pruning is performed so that each pruning group has a constant number of non-zero weights. Since a weight corresponds to one of \( g \) activations, the width of a MUX for the activation selection can be reduced to \( g \). With the smaller \( g \), the PE structure in Fig. 4 can be simplified into the structure in Fig. 7. As can be seen in the figure, the activation selection logic becomes simplified with narrower MUXs. When \( g \) becomes smaller, however, the network performance can degrade more with the same pruning ratio. The experiment shows that \( g = 16 \) with 75% pruning ratio does not deteriorate the CNN performance.

The proposed pruning scheme induces the reduction of \( N_{par} \), too. As mentioned in Subsection II-E, \( N_{par} = 256 \) of Cambricon-X is large compared to \( N_{mul} = 16 \). With the common pruning ratio of 75% in convolutional layers, \( N_{par} = 64 \) is enough. The large \( N_{par} \) may be chosen to reduce the amount of padding zeros. However, the proposed scheme makes the padding zeros unnecessary, so \( N_{par} = 64 \) can be used. Then the width of the activation buffers can be reduced to 64, enabling more square-like memories to be used, which are more area-efficient than wide memories.

Furthermore, the indexing logic can be simplified, too. For indexing of the irregular non-zero weights, Deep Compression and EIE use relative indexing [20], [34], where the number of zero weights between two adjacent non-zero weights is stored. An interval is encoded with 4 bits, and an interval larger than the encoding bound requires filler zero insertions. A similar indexing is used in Cambricon-X, called step indexing. The indexing can be simplified with the proposed pruning scheme. In the proposed scheme, the pruning is performed within a pruning group of \( g \). The small \( g \) enables direct indexing, where an index indicates the position of the non-zero weight within the pruning group. Since \( g \) is small, the indexing bit width, \( w_i \), is also small, \( \lceil \log_2 g \rceil \) bits, even with the direct indexing. The direct indexing is much simpler than the relative indexing in EIE or the step indexing in Cambricon-X and does not require the filler zeros, removing the waste of the weight storage.

C. Pruning Ratio and Pruning Weight Selection

The proposed pruning scheme can set the pruning ratio directly, as opposed to the previous schemes. In [19], weights with a magnitude less than a threshold are pruned away. With this scheme, the pruning ratio cannot be predicted easily. The pruning ratio is determined after pruning. If the target ratio is not reached, the pruning is tried again with a smaller threshold. The process is iterated until the target pruning ratio is reached. In the proposed pruning, however, the target is the number of pruned weights per pruning group. In other words, the pruning ratio is directly focused. If the number of weights pruned away in a pruning group is \( p \), the pruning ratio will be \( p/g \).

Various methods can be used to select the weights to be pruned. The simplest one is to select the weights by weight magnitude. In a more complex method, the effect of weights is estimated and the weights with the smaller effect are removed earlier. The proposed pruning scheme can be used with any selection method, but, in this paper, the simplest method will be used. The weights with the least magnitude are pruned first in a pruning group.

D. Incremental Pruning

In the proposed scheme, \( p \) weights are pruned in a pruning group. The pruning can be processed in a few ways. In an extreme, the target number of weights with the least magnitude in each group are pruned at the same time, and the pruned network is retrained. This scheme will be called one-time pruning. In the other extreme, only one weight with the least magnitude in each group is pruned at first. After a period of retraining, one more weight with the least retrained magnitude is selected and pruned. The retraining is performed again. The one weight pruning and retraining are iterated until the target number is reached. In the middle of the two extreme methods, we can set the initial pruning number and the increment number. This scheme will be called the incremental pruning in this paper.

Obviously, the incremental pruning would be better than or equal to the one-time pruning method. However, the incremental pruning requires a long retraining time, so, in this paper, it will be applied when one-time pruning is not sufficient.
To show that the proposed pruning scheme can preserve the performance of CNNs well even with the constraint, the top-5 accuracy for the ImageNet 2012 validation data set was measured. The retraining was performed by Caffe in one of three modes. In Retraining 1, after one-time pruning, the retraining was performed with the learning rate of $5 \cdot 10^{-4}$ for 12 epochs. If the original accuracy was not recovered, 8-epoch retraining was performed additionally with the learning rate of $10^{-5}$. If Retraining 1 was not enough, Retraining 2 was applied, where the learning rate begins with $5 \cdot 10^{-4}$ and decreases to $10^{-4}$, $10^{-5}$, and $10^{-6}$ when the validation accuracy is saturated. In Retraining 3, Retraining 2 is applied with incremental pruning. When the validation accuracy is saturated with the learning rate of $10^{-6}$, $p$ is increased, and the retraining resumes with the learning rate of $5 \cdot 10^{-4}$. The retraining mini-batch size was set to 256. The network models were obtained publicly. The pruning of the convolutional layers will be discussed first because convolutional layers occupy most of the computations. Then my pruning scheme was applied to the fully connected layers with the pruned convolutional layers. It will be shown that the proposed pruning can be applied to networks that are already slimmed by the previous channel pruning schemes, too. In the last subsection, the accelerator complexity reduction will be analyzed.

## A. Convolutional Layer Pruning

Table [I] shows the accuracy results right after the pruning of the convolutional layers. The weights are grouped along the channel axis, and the first convolutional layer is not pruned since it has a much smaller number of weights and operations than the other layers. The table shows that 30% (3/8 or 6/16) pruning already begins to degrade the accuracy. However, the degradation can be recovered with retraining as shown in Table [VIII]. Retraining 1 and 3 are applied, and the results of Retraining 3 are marked by asterisks.

In the table, up to 75% (6/8 or 12/16) pruning, the validation accuracy could be recovered to the baseline accuracy with Retraining 1 in the very-deep networks including VGG16, ResNet-50, and ResNet-152. The result of VGG16 matches that of the unstructured pruning algorithm in [19], where the pruning ratio of the convolutional layers are more or less than 75% in VGG16. The experiment shows that a similar pruning ratio can be reached with the proposed pruning scheme considering the accelerator constraint. It can also be seen that a 75% pruning ratio does not degrade the accuracy in the residual networks, ResNet-50 and ResNet-152, too. The networks have more complicated structures like the residual path and the $1 \times 1$ convolution. The results show that the proposed scheme can be applied to recent state-of-the-art CNNs.

In the relatively shallow networks like AlexNet and SqueezeNet, it was harder to recover the accuracy degradation. With the more advanced effort of Retraining 3, however, the original accuracy can be recovered with pruning ratios comparable to those in [19] and [5]. In AlexNet, Retraining 3 begins with $(p, g) = (5, 8)$ or $(10, 16)$, and $p$ is increased

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**Table IV. Retraining 1 and 3 are applied, and the results of Retraining 3 are marked by asterisks.**

| Network   | Pruning Ratio | Retraining 1 | Retraining 3 |
|-----------|---------------|--------------|--------------|
| VGG16     | 50%           | 1.00         | 0.99         |
| ResNet-50 | 75%           | 1.00         | 0.99         |
| ResNet-152| 75%           | 1.00         | 0.99         |

**Table III. Retraining 1 and 3 are applied, and the results of Retraining 3 are marked by asterisks.**

| Network   | Pruning Ratio | Retraining 1 | Retraining 3 |
|-----------|---------------|--------------|--------------|
| AlexNet   | 50%           | 1.00         | 0.99         |
| SqueezeNet| 50%           | 1.00         | 0.99         |

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## IV. Experimental Results

To show that the proposed pruning scheme can preserve the performance of CNNs well even with the constraint, the top-5 accuracy for the ImageNet 2012 validation data set was measured. The retraining was performed by Caffe in one of three modes. In Retraining 1, after one-time pruning, the retraining was performed with the learning rate of $5 \cdot 10^{-4}$ for 12 epochs. If the original accuracy was not recovered, 8-epoch retraining was performed additionally with the learning rate of $10^{-5}$. If Retraining 1 was not enough, Retraining 2 was applied, where the learning rate begins with $5 \cdot 10^{-4}$ and decreases to $10^{-4}$, $10^{-5}$, and $10^{-6}$ when the validation accuracy is saturated. In Retraining 3, Retraining 2 is applied with incremental pruning. When the validation accuracy is saturated with the learning rate of $10^{-6}$, $p$ is increased, and the retraining resumes with the learning rate of $5 \cdot 10^{-4}$. The retraining mini-batch size was set to 256. The network models were obtained publicly. The pruning of the convolutional layers will be discussed first because convolutional layers occupy most of the computations. Then my pruning scheme was applied to the fully connected layers with the pruned convolutional layers. It will be shown that the proposed pruning can be applied to networks that are already slimmed by the previous channel pruning schemes, too. In the last subsection, the accelerator complexity reduction will be analyzed.

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TABLE III
| g | p | AlexNet | SqueezeNet v1.0 | VGG16 | ResNet-50 | ResNet-152 |
|---|---|---------|----------------|-------|-----------|-----------|
| - | - | 0.79812 | 0.80390 | 0.88444 | 0.91136 | 0.92201 |
| 8 | 1 | 0.79766 | 0.79566 | 0.88308 | 0.90942 | 0.92123 |
| 8 | 2 | 0.79166 | 0.76610 | 0.88020 | 0.90296 | 0.91691 |
| 8 | 3 | 0.76888 | 0.68436 | 0.85524 | 0.88272 | 0.90716 |
| 8 | 4 | 0.65020 | 0.35740 | 0.70204 | 0.78792 | 0.86372 |
| 8 | 5 | 0.32194 | 0.03494 | 0.12234 | 0.17206 | 0.46580 |
| 16 | 1 | 0.79826 | 0.80240 | 0.88466 | 0.91158 | 0.92217 |
| 16 | 2 | 0.79762 | 0.79938 | 0.88356 | 0.91082 | 0.92177 |
| 16 | 4 | 0.79352 | 0.77876 | 0.88190 | 0.90800 | 0.92073 |
| 16 | 6 | 0.77996 | 0.71332 | 0.86642 | 0.88880 | 0.91363 |
| 16 | 8 | 0.69992 | 0.43120 | 0.75344 | 0.80744 | 0.87900 |
| 16 | 9 | 0.60840 | 0.23148 | 0.55150 | 0.59390 | 0.80360 |
| 16 | 10 | 0.38612 | 0.07712 | 0.20118 | 0.32418 | 0.65674 |

TABLE IV
| g | p | AlexNet | SqueezeNet v1.0 | VGG16 | ResNet-50 | ResNet-152 |
|---|---|---------|----------------|-------|-----------|-----------|
| - | - | 0.79812 | 0.80390 | 0.88444 | 0.91136 | 0.92201 |
| 8 | 4 | 0.80446 | 0.80514 | 0.90706 | 0.91950 | 0.93027 |
| 8 | 5 | 0.80580 | 0.79932 | 0.90454 | 0.91142 | 0.92329 |
| 8 | 6 | 0.80422 | 0.77586 | 0.89914 | 0.91142 | 0.92329 |
| 8 | 7 | 0.79472 | 0.68064 | 0.88480 | 0.88880 | 0.91363 |
| 16 | 8 | 0.80456 | 0.80928 | 0.90734 | 0.91956 | 0.93021 |
| 16 | 9 | 0.80236 | 0.80650 | 0.90798 | 0.91800 | 0.92885 |
| 16 | 10 | 0.80288 | 0.80294 | 0.90798 | 0.91800 | 0.92885 |
| 16 | 11 | 0.80008 | 0.89190 | 0.90798 | 0.91800 | 0.92885 |
| 16 | 12 | 0.79470 | 0.79472 | 0.88480 | 0.88880 | 0.91363 |

TABLE V
| g | p1 | p2 | p3 | AlexNet | VGG16 | ResNet-50 | ResNet-152 |
|---|---|---|---|---------|-------|-----------|-----------|
| - | - | - | - | 0.79812 | 0.80390 | 0.88444 | 0.91136 | 0.92201 |
| 16 | 12 | 12 | 12 | 0.80256 | 0.89842 | 0.91240 | 0.92543 |
| 16 | 12 | 13 | 12 | 0.80236 | 0.89562 | 0.91240 | 0.92543 |
| 16 | 12 | 14 | 12 | 0.80008 | 0.89190 | 0.91240 | 0.92543 |
| 16 | 12 | 15 | 12 | 0.79470 | 0.88946 | 0.91240 | 0.92543 |

by one. While the pruning ratio of the AlexNet convolutional layers was around 65% with the unstructured pruning in [19], the proposed scheme can reach a pruning ratio of 81.25%. In SqueezeNet, $p = g/2$ weights are pruned initially, and $p$ is increased by one, too. In the network, the unstructured pruning can reach a 66.3% pruning ratio [5], which is similar to $p = 10$ or 11 with $g = 16$ in the proposed scheme. With this pruning ratio, the accuracy degradation of the proposed pruning scheme is around 0.005.

B. Fully-Connected Layer Pruning

After the pruning of the convolutional layers, the fully connected layers were pruned along the row axis. In the fully connected layer pruning, there was an attempt to prune more weights than were pruned initially, and $p$ is increased by one, too. In the network, the unstructured pruning can reach a 66.3% pruning ratio [5], which is similar to $p = 10$ or 11 with $g = 16$ in the proposed scheme. With this pruning ratio, the accuracy degradation of the proposed pruning scheme is around 0.005.

The table shows that the proposed pruning scheme can reach a pruning ratio similar to that of the previous pruning scheme in the fully connected layers, too. In [19], 90–96% of the weights were pruned in the first and the second fully connected layers of AlexNet and VGG16 and 75–77% of the weights in the last layer. In all of the presented networks, the proposed pruning scheme could prune 75% of the weights ($p3 = 12$) in the last fully connected layers. For the first and second fully-connected layers of VGG16, the pruning with $p2 = 15$ (93.75% pruning) did not degrade the accuracy. In AlexNet, $p2 = 15$ showed an accuracy of 0.79470, which is slightly worse than the accuracy of the pruned AlexNet in [20], 0.7968. Since $p1 = 12$ in the convolutional layers is larger than 62–65% in [20], the pruning result is quite comparable.
TABLE VI

| g  | p  | VGG16-4X | VGG16-5X | ResNet-50 CP |
|----|----|----------|----------|--------------|
| -  | -  | 0.89056  | 0.86978  | 0.89636      |
| 16 | 8  | 0.89532  | 0.88252  | 0.91442      |
| 16 | 10 | 0.88580  | 0.87906  | 0.91284      |
| 16 | 12 | 0.87050  | 0.87360  | 0.90300      |

TABLE VII

| Accelerators (Measurement Condition) | Area (mm²) | Delay (ns) | Power (W) |
|--------------------------------------|------------|------------|-----------|
| Cambricon-X (P&R)                    | 0.55       | 1.05       | 1.78      | 6.38      | 1.00 | 0.954 |
| Reimplemented (Synthesis)            | 0.32       | 0.43       | 2.39      | 1.46      | 4.91 | 1.02 | 3.30  |
| Reduced (g = 8, Synthesis)           | 0.11       | 0.11       | 0.43      | 0.17      | 1.19 | 2.01 | 1.05 | 1.70 |
| Reduced (g = 16, Synthesis)          | 0.11       | 0.11       | 0.43      | 0.27      | 1.41 | 2.34 | 1.02 | 1.90 |
| Reduced (g = 32, Synthesis)          | 0.11       | 0.11       | 0.43      | 0.44      | 1.44 | 2.53 | 1.02 | 1.97 |
| Cambricon-X Reduced (g = 16, Estimation) | 0.19   | 0.19       | 1.05      | 0.22      | 1.72 | 3.84 | 1.00 | 0.549 |

C. Slimmed Network Pruning

Some of the previous works pruned convolutional layers channel-wisely or filter-wisely \([22], [23]\). The resulting networks are the slimmer ones with fewer channels in the layers. The slimmed networks can also be pruned by the proposed pruning scheme, too. For the experiment, the networks slimmed in \([24]\) were used because their models are publicly available \([48]\). In \([24]\), the weight amount of the networks was also reduced by other methods, like decomposition. The proposed scheme was applied with \(g = 16\). In some layers of the slimmed networks, \(C\) is not a multiple of \(g\). In that case, it is assumed that zero weights are added to make \(C\) a multiple of \(g\).

The accuracy results are shown in Table VI. The table shows that the proposed pruning scheme prunes weights pretty well even in the already slimmed networks. The 50% pruning of convolutional layers \((p = 8)\) does not degrade the accuracy of the slimmed networks. This shows that the proposed pruning scheme provides a comparable pruning for the slimmed networks. It is also noticeable that 75% pruning of \(p = 12\) does not degrade the accuracy of VGG16-5X and ResNet-50 CP.

D. Accelerator Logic Complexity

As mentioned in Subsection III-B, the proposed pruning scheme can reduce accelerator complexity. In this subsection, reduction of the area of Cambricon-X will be attempted. The second row in Table VII presents the area, delay time, and power consumption of Cambricon-X. In the table, NBin, NBout, and SB are the input activation buffer, the output activation buffer, and the weight buffer, respectively. IM is the indexing and the activation selection unit.

Since the RTL code of Cambricon-X is not publicly available, I reimplemented the blocks in the table for the area comparison. The other blocks in Cambricon-X are not affected by the proposed scheme. Hardware parameters are inferred from the context of the paper. The synthesis results of the reimplemented one is presented at the third row. The synthesis was performed by Synopsys DesignCompiler with the Global Foundry 65nm process library. Since the results of Cambricon-X are obtained after the placement and routing (P&R) process with a different library, it is hard to compare the values of the second and third rows directly. Therefore, the expected reduction effect on Cambricon-X will be estimated from the reduction in the reimplemented version, which is shown at the following rows. Measurement and implementation conditions are described in the parenthesis of the first column. \(N_{par}\) is 256 for Cambricon-X and 64 for the other cases. \(N_{mul}\) and \(N_{PE}\) are 16.

The forth to sixth rows present the synthesis results of the reduced implementation assuming the application of the proposed pruning scheme with various \(g\) values. Compared to the results of the reimplemented Cambricon-X at the third row, the area is reduced very much, especially that of NBin, NBout and IM. The area of NBin and NBout is reduced by the memory width reduction from 256×16 to 64×16. Although the memory capacity is not changed, more square-shaped memory configuration results in a smaller area. The area reduction of the IM block is more astonishing, with a decrease of 82–93%. The wide MUXs, 256-to-1 MUXs, in the IM block of Cambricon-X are substituted with the narrow \(g\)-to-1 MUXs. Since the area of a MUX logic is proportional to the input width, the narrow MUXs lead to a smaller IM block. With the smaller area, the table also shows lower power consumption. The delay increased slightly, but the difference is negligible. The last row shows the estimated Cambricon-X when the simplification proposed in Subsection III-B is applied. The values were obtained by comparing the third and fifth rows. Due to the area reduction of NBin, NBout, and IM, the total area can be reduced by 40%.

V. Conclusions

In this paper, an accelerator-aware pruning scheme was proposed for CNNs. In the pruning process, the proposed scheme considers accelerator parameters like the width of the internal activation buffer and the number of multipliers. After pruning, each weight fetching group has a fixed number of non-zero weights left. The network pruned by the proposed scheme...
can be efficiently run on a target accelerator. Furthermore, the proposed pruning scheme can be used to reduce accelerator complexity, too. Even with the accelerator constraint, it was shown that the proposed scheme can reach the pruning ratio close to that of the previous unstructured pruning schemes. In the paper, the pruning scheme was discussed in relation to some representative sparse accelerator architectures, but the scheme can be applied for any sparse architectures.

REFERENCES

[1] A. Krizhevsky, I. Sutskever, and G. E. Hinton, “ImageNet classification with deep convolutional neural networks,” in Proc. Advances in Neural Inf. Process. Syst., 2012, pp. 1097–1105.

[2] K. Simonyan and A. Zisserman, “Very deep convolutional networks for large-scale image recognition,” in Proc. Int. Conf. Learning Representations, 2015. [Online]. Available: http://arxiv.org/abs/1409.1556

[3] C. Szegedy, W. Liu, Y. Jia, P. Sermanet, S. Reed, D. Anguelov, D. Erhan, V. Vanhoucke, and A. Rabinovich, “Going deeper with convolutions,” in Proc. Comput. Vision and Pattern Recognition, 2015, pp. 1–9. [Online]. Available: http://arxiv.org/abs/1409.4842

[4] K. He, X. Zhang, S. Ren, and J. Sun, “Deep residual learning for image recognition,” in Proc. Comput. Vision and Pattern Recognition, 2015. [Online]. Available: http://arxiv.org/abs/1512.03385

[5] F. N. Iandola, S. Han, M. W. Moskewicz, K. Ashraf, W. J. Dally, and K. Keutzer. (2016) SqueezeNet: AlexNet-level accuracy with 50x fewer parameters and <0.5MB model size. [Online]. Available: http://arxiv.org/abs/1602.07360

[6] P. Sermanet, D. Eigen, X. Zhang, M. Mathieu, R. Fergus, and Y. LeCun, “OverFeat: Integrated recognition, localization and detection using convolutional networks,” in Proc. Int. Conf. Learning Representations, 2014. [Online]. Available: http://arxiv.org/abs/1312.6229

[7] R. Girshick, J. Donahue, T. Darrell, and J. Malik, “Rich feature hierarchies for accurate object detection and semantic segmentation,” in Proc. Comput. Vision and Pattern Recognition, 2014, pp. 580–587.

[8] R. Girshick, “Fast R-CNN,” in Proc. Int. Conf. Computer Vision, 2015, pp. 1440–1448. [Online]. Available: http://arxiv.org/abs/1504.08053

[9] S. Ren, K. He, R. Girshick, and J. Sun, “Faster R-CNN: Towards real-time object detection with region proposal networks,” in Proc. Advances in Neural Inf. Process. Syst., 2015, pp. 1–9.

[10] N. McLaughlin, J. M. del Rincon, and P. C. Miller, “Person reidentification with deep convolutional neural networks,” in Proc. Int. Conf. Computer Vision and Pattern Recognition, 2016, pp. 770–778. [Online]. Available: http://arxiv.org/abs/1512.03385

[11] Y. He, X. Zhang, and J. Sun, “Channel pruning for accelerating very deep neural networks,” in Proc. Int. Conf. Computer Vision, 2017. [Online]. Available: http://arxiv.org/abs/1707.06168

[12] J. Yu, A. Lukefahr, D. Palframan, G. Dasika, R. Das, and S. Mahlke, “Scalpel: Customizing DNN pruning to the underlying hardware parallelism,” in Proc. Int. Conf. Computer Architecture, 2017.

[13] P. Molchanov, S. Tyree, T. Karras, T. Aila, and J. Kautz, “Pruning convolutional neural networks for resource efficient inference,” in Proc. Int. Conf. Learning Representations, 2017. [Online]. Available: http://arxiv.org/abs/1611.06440

[14] N. Yu, S. Qiu, X. Hu, and J. Li, “Accelerating convolutional neural networks by group-wise 2D-filter pruning,” in Proc. Int. Joint Conf. Neural Networks, 2017, pp. 2502–2509.

[15] V. Lebedev and V. Lempitsky, “Fast ConvNets using group-wise brain damage,” in Proc. Comput. Vision and Pattern Recognition, 2016, pp. 2554–2564. [Online]. Available: http://arxiv.org/abs/1506.02515

[16] S. Anwar, K. Hwang, and W. Sung, “Structured pruning of deep convolutional neural networks,” ACM J. on Emerging Technologies in Computing Sysytems, vol. 13, no. 3, p. Article No. 32, feb, 2017.

[17] H. Mao, S. Han, J. Pool, W. Li, X. Liu, Y. Wang, and W. J. Dally, “Exploring the regularity of sparse structure in convolutional networks,” in Proc. Int. Conf. Learning Representations, 2017. [Online]. Available: http://arxiv.org/abs/1705.08922

[18] D. Kadetotad, S. Arunachalam, C. Chakrabarti, and J.-S. Seo, “Efficient memory compression in deep neural networks using coarse-grain sparsification for speech applications,” in Proc. Int. Conf. Comput. Aided Design, 2016.

[19] S. Anwar, S. Li, W. Wen, P. T. T. Tang, H. Li, Y. Chen, and P. Dubey, “Faster ConvNets with direct sparse convolutions and guided pruning,” in Proc. Int. Conf. Learning Representations, 2017.

[20] Y. Boo and W. Sung, “Structured sparse ternary weight coding of deep neural networks for efficient hardware implementations,” in Proc. IEEE Workshop on Signal Process. Syst. Design and Implementation, 2017.

[21] S. Han, X. Liu, H. Mao, J. Pu, A. Pedram, M. A. Horowitz, and W. J. Dally, “EIE: Efficient inference engine on compressed deep neural network,” in Proc. Int. Symp. Computer Architecture, 2016, pp. 243–254. [Online]. Available: http://arxiv.org/abs/1602.01528

[22] S. Han, J. Kang, H. Ma, Y. Hu, X. Li, Y. Li, D. Sze, H. Luo, S. Yao, Y. Wang, H. Yang, and W. J. Dally, “ESE: Efficient speech recognition engine with sparse LSTM on FPGA,” in Proc. ACM/SIGDA Int. Symp. Field Programmable Gate Arrays, 2017.

[23] S. Zhang, Z. Du, L. Zhang, H. Lan, S. Liu, L. Li, Q. Guo, T. Chen, and Y. Chen, “Cubricorn-X: An accelerator for sparse neural networks,” in Proc. Symp. Int. Symp. Microarchitecture, 2016.

[24] A. Parashar, M. Rhu, A. Mukkara, A. Puglielli, R. Venkatesan, B. Khailany, J. Emer, S. W. Keckler, and W. J. Dally, “SCNN: An accelerator for compressed-sparse convolutional neural networks,” in Proc. Int. Symp. Computer Architecture, 2017.

[25] D. Kim, J. Ahn, and S. Yoo, “A novel zero weight/activation-aware hardware architecture of convolutional neural network,” in Proc. Design, Automation & Test in Europe Conf. & Exhibition, 2017, pp. 1462–1467.

[26] Y. LeCun, J. S. Denker, and S. A. Solla, “Optimal brain damage,” in Proc. Advances in Neural Inf. Process. Syst., 1990, pp. 598–605.

[27] B. Hassibi and D. G. Stork, “Second order derivatives for network pruning: Optimal brain surgeon,” in Proc. Advances in Neural Inf. Process. Syst., 1993, pp. 293–299.

[28] B. Hassibi, D. G. Stork, and G. J. Wolff, “Optimal brain surgeon and general network pruning,” in Proc. Int. Conf. Neural Networks, 1993.
[42] O. Russakovsky, J. Deng, H. Su, J. Krause, S. Satheesh, Z. Ma, S. Huang, A. Karpathy, A. Khosla, M. Bernstein, A. C. Berg, and L. Fei-Fei, “ImageNet large scale visual recognition challenge,” Int. J. Comput. Vision, vol. 115, no. 3, pp. 211–252, Dec. 2015.

[43] Y. Jia, E. Shelhamer, J. Donahue, S. Karayev, J. Long, R. Girshick, S. Guadarrama, and T. Darrel. (2014) Caffe: Convolutional architecture for fast feature embedding. [Online]. Available: http://arxiv.org/abs/1408.5093

[44] Y. Jia, E. Shelhamer, J. Donahue, S. Karayev, J. Long, R. Girshick, S. Guadarrama, and T. Darrell. Caffe. [Online]. Available: https://github.com/BVLC/caffe

[45] K. Simonyan and A. Zisserman. VGG16/19. [Online]. Available: http://www.robots.ox.ac.uk/~vgg/research/very_deep

[46] K. He, X. Zhang, S. Ren, and J. Sun. ResNet. [Online]. Available: https://github.com/KaimingHe/deep-residual-networks

[47] F. N. Iandola, S. Han, M. W. Moskewicz, K. Ashraf, W. J. Dally, and K. Keutzer. SqueezeNet. [Online]. Available: https://github.com/DeepScale/SqueezeNet

[48] Y. He, X. Zhang, and J. Sun. Channel pruning for accelerating very deep neural networks. [Online]. Available: https://github.com/yihui-he/channel-pruning