A bias network for small duty-cycle fast-pulsed measurement of RF power transistors

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Abstract. Radio-frequency power transistors affected by dispersive phenomena such as thermal and charge trapping effects can be effectively characterized and modeled by means of pulsed current-voltage measurements. This work presents the design of a passive bias network made out of off-the-shelf components and tailored for the application of fast pulses through its capacitive path, yet extending the bandwidth down to a few kHz. This custom component enables small duty-cycle (e.g., 0.1 %) fast-pulsed excitations of several tens of V of ac voltage in the presence of bias voltages up to 50 V and bias currents up to 2 A.

1. Introduction
Pulsed current-voltage (PIV) measurements [1] allow for the iso-thermal and iso-dynamic acquisition of IV characteristics, which represent a reliable approximation of the transistor behavior in application-like radio-frequency (RF) operating regimes. Pulsed techniques are effective not only for transistor modeling [2], but also for technological process improvement [3] and device lifetime tests [4]. The advent of Gallium Nitride (GaN) on Silicon Carbide (SiC) High-Electron-Mobility Transistors (HEMTs) has recently imposed more demanding specifications to the setups for pulsed measurement. In fact, baside showing significant charge trapping effects with time constants ranging from ms to ps, the dynamic behavior of charge trapping in GaN-on-SiC HEMTs is nonlinear, involving a complex dependency on the applied voltages. As a consequence, distortion effects such as overshoots and ringing in the generated pulsed waveforms must be minimized for avoiding spurious excitation.

In standard PIV characterization setups, a pulsed voltage is applied through the dc path of the bias networks (BNs) by means of source-measurement units (SMUs), typically allowing to reach undistorted pulsed waveforms with pulse widths down only to a few $\mu$s, as the impedance mismatch introduced by the measurement fixture and by access cables inevitably reduces the available bandwidth. A different approach for the fast-pulsed characterization is shown in Fig. 1. In this setup, traveling-wave pulses are applied through the ac path of the BNs by means of arbitrary function generators (AFGs) with 50-Ω source impedance [5]. The excitation in a 50-Ω environment entails reduced overshoots and prevents oscillations, allowing to reach < 100 ns pulse widths. Moreover, it maximizes the available bandwidth, allowing to apply properly shaped pulsed waveforms. On the other hand, when considering the power specifications of the typical device-under-test (DUT), the necessity to generate small duty-cycles to ensure iso-thermal operation, and the wide-bandwidth requirement, the design of suitable BNs for the proposed 50-Ω-matched setup represents a challenging task.
2. Design of the bias network

BNs are three-port networks used to provide biasing to an active RF device, yet ensuring proper impedance termination (50 Ω) in the microwave range at a frequency-diplexed RF (ac) port. Classic BNs for Vector Network Analyzers (VNAs) feature a frequency response from a few MHz up to several GHz, and typically allow to apply bias currents of a few hundreds mA. Beside the dc power limitation, this type of BNs is not suitable for the setup of Fig. 1, as it does not provide a proper bandwidth for pulsed excitation in the lower frequency range. Low-frequency (LF) active BNs have been proposed for noise measurement [6], but active circuitry is not recommended for large-signal characterization of DUTs showing nonlinear dynamic behavior.

The design here proposed stems from the basic lumped circuit of Fig. 2(a), composed by a shunt inductor on the dc path (between port 2 and port 3) and a series capacitor on the ac path (between port 1 and port 3). For a bandwidth $BW = [f_{\text{min}}, f_{\text{max}}]$ on the ac path (between port 1 and port 3), $f_{\text{max}}$ should be sufficiently large to allow applying narrow-width (e.g., 100 ns) square pulses, while $f_{\text{min}}$ should be small enough to enable large excitation periods (e.g., tens of μs). In addition, the insertion loss of the ac path and the parasitic resistance of the dc path must be as low as possible. Finally, the isolation between the dc and ac ports (1 and 2) should be maximum, while adequate matching to the reference impedance $Z_0$ should be provided at port 1 and 3 for low return loss. By terminating port 3 of the BN with $Z_0$ as shown in Fig. 2(b), one obtains a total input admittance of:

$$Y_T = Y_C + Y_L = \frac{1}{Z_0} \frac{j\omega CZ_0 + (\omega CZ_0)^2}{1 + (\omega CZ_0)^2} - j \frac{1}{\omega L},$$

where $Y_C$ and $Y_L$ are the capacitive and inductive admittances, respectively. By a few simple mathematical steps and by introducing the reflection coefficient $\rho$ at port 3, we obtain the design formulas linking $C$ and $L$ with $\rho$ at $f_{\text{min}}$ [7]:

$$C = \frac{1}{2\pi f_{\text{min}} Z_0} \sqrt{\frac{1 - \rho}{2\rho}}; \quad L = \frac{Z_0}{2\pi f_{\text{min}}} \frac{1 + \rho}{1 - \rho} \sqrt{\frac{1 - \rho}{2\rho}}.$$

For achieving $\rho = -25$ dB and $f_{\text{min}} = 10$ kHz, the design formulas in (2) result in $C = 0.92$ μF and $L = 2.58$ mH, whereas the maximum frequency $f_{\text{max}}$ will only be limited by the parasitic reactances associated with $C$ and $L$. Commercial BNs targeting pulsed applications may employ custom wideband components, such as conic inductors and multilayer capacitors, resulting in several hundreds $\$ cost. Here, we target a low-cost implementation by using multiple capacitors and inductors to handle high voltages (several tens of V) and currents (up to a few A), where...
bandwidth effects are compensated by a suitable circuit topology. Small-signal and large-signal transient simulations of the $L$ and $C$ equivalent circuits in Fig. 3 have been implemented in CAD (Keysight ADS) for performance evaluation and tuning. Depending on the reactive parasitics, the actual bandwidth of operation is compromised as self-resonances appear at $f_{0,C} = 1/2\pi \sqrt{L_pC}$ and $f_{0,L} = 1/2\pi \sqrt{LC_p}$.

As far as the dc path is concerned, a series of ten wirewound through-hole inductors of increasing value from 4 $\mu$H to 500 $\mu$H has been designed. For each inductor, appropriate high-value parallel resistors have been placed for mitigating the self-resonance peaks, thus maximizing the flatness of the frequency response. In addition, a branch with a resistor and a capacitor in series configuration has been suitably tuned by simulation in order to distribute the overvoltages across the series of inductors. Concerning the ac path, the availability of low-parasitics high-frequency capacitors with breakdown voltages of 50 V (125 V peak) allowed to synthesize the desired capacitance as a simple parallel of nine wideband surface mount device (SMD) 100 nF capacitors. A couple of high-voltage shunt electrolytic capacitors (amounting to 60 $\mu$F) have been added at Port 2 for compensating the increase of the supply output impedance in the kHz range. Finally, since the BN should show an input resistive termination at Port 3 also beyond $f_{max}$ to ensure stability, an additional LC structure composed by a 4.2 nH series SMD inductor and a parallel 1.2 pF SMD capacitor terminated into a 50 $\Omega$ resistor has been added to the ac path. The resulting circuit (Fig. 4) has been implemented as a printed circuit board (PCB) on single layer FR4 substrate (Fig. 5).

![Figure 3](image1.png)  
**Figure 3.** Equivalent circuits of the capacitor (a) and inductor (b) including parasitics.

![Figure 4](image2.png)  
**Figure 4.** Circuit implementation of the bias network.

### 3. Experimental results

The linear behavior of the designed BN in the kHz to MHz range was characterized by means of an oscilloscope-based setup. Similarly to the setup in Fig. 1 (yet removing the biasing, and using the BN as the DUT, excited by small-signal sine waves), two bi-directional bridge couplers and four oscilloscope receivers build up a basic two-port low-frequency VNA. A classic Short-Open-Load-Thru calibration was performed at the BN coaxial connectors from 0.5 kHz to 100 MHz, allowing S-parameters characterization. The relevant performance parameters are reported in Fig. 6, showing adequate insertion loss, return loss, and isolation in the measured range. Table 1 summarizes the performance of the realized BN ($f_{min}$ and $f_{max}$ defined for a maximum $\rho = -20$ dB), which is suitable for excitation rise/fall times of a few ns, periods of up to 100-µs widths down to tens of ns (duty-cycle $\leq 0.1$ %) applied to RF transistors of tens of W of available power.

![Table 1](image3.png)  
**Table 1.** Summary of the performance of the realized BN ($f_{min}$ and $f_{max}$ defined for a maximum $\rho = -20$ dB), which is suitable for excitation rise/fall times of a few ns, periods of up to 100-µs widths down to tens of ns (duty-cycle $\leq 0.1$ %) applied to RF transistors of tens of W of available power.

Finally, the BN has been successfully used within the setup of Fig. 1 for the PIV characterization of a 8x125 $\mu$m GaN-on-SiC HEMT (0.25 $\mu$m gate length) biased at the nominal value for class AB amplifier operation (drain voltage: 30 V, drain current: 80 mA). The applied
voltage waveforms, featuring a period of 100 $\mu$s and pulse widths of 100 ns are shown in Fig. 7, while the pulsed current and the resulting PIV characteristic are shown in Fig. 8.

![Figure 5. Photo of the realized PCB. (a) Front view. (b) Rear view.](image1)

![Figure 6. S-parameters of the designed bias network.](image2)

Table 1. Performance parameters of the designed bias network.

| $f_{\text{min}}$ (kHz) | $f_{\text{max}}$ (MHz) | max $V_{\text{DC}}$ (V) | max $I_{\text{DC}}$ (A) | $R_{\text{DC}}$ (Ω) |
|------------------------|------------------------|-------------------------|------------------------|-----------------|
| 7                      | 70                     | 50                      | 2                      | 1.4             |

![Figure 7. Pulsed gate (a) and drain (b) voltage waveforms applied to the DUT, with pulse width: 100 ns, period: 100 $\mu$s (duty-cycle: 0.1%).](image3)

![Figure 8. (a) Pulsed current for the voltages in Fig. 7. (b) PIV characteristic. Symbols 'x' correspond to the waveforms in (a).](image4)

References

[1] Scott J, Rathmell J G, Parker A and Sayed M 1996 Pulsed device measurements and applications IEEE Trans. Microw. Theory Techn. 44(12) 2718-2723
[2] Santarelli A, Niessen D, Cignani R, Gibiino G P, Traverso P A, Florian C, Schureurs D and Filicori F 2014 GaN FET nonlinear modeling based on double pulse IV characteristics IEEE Trans. Microw. Theory Techn. 62(12) 3262-3273
[3] Santarelli A, Cignani R, Niessen D, Gibiino G P, Traverso P A, Di Giacomo V, Chang C, Floriot D, Schreurs D, and Filicori F 2014 Evaluation of GaN FET power performance reduction due to nonlinear charge trapping effects Proc. European Microw. Integrated Circ. Conf. 198-201
[4] Paine B M, Polmanter S R, Ng V T, Kubota N T and Ignacio C R, 2017 Fast-Pulsed Characterization of RF GaN HEMTs in Lifetest Systems IEEE Trans. Device Mater. Rel. 17(1) 130-137
[5] Santarelli A, Cignani R, Niessen D, Traverso P A and Filicori F 2012 New pulsed measurement setup for GaN and GaAs FETs characterization Int. J. Microw. Wirel. Technol. 4(3) 387-397
[6] Florian C and Traverso P A 2008 Active bias network-based measurement set-up for the direct characterization of low-frequency noise currents in electron devices. 16th IMEKO TC4 Int. Symp. 185-190
[7] Bahl I J 2009 Fundamentals of RF and Microwave Transistor Amplifiers (Hoboken, NJ: Wiley).