The following review was selected from those recently published in various IEEE journals, magazines, and newsletters. They are reprinted here to make them conveniently available to the many readers who otherwise might not have access to them. Each review is followed by an identification of its source.

Evolvable Systems 1998—Proceedings of the Second International Conference on Evolvable Systems: From Biology to Hardware (ICES’98)—M. Sipper, D. Mange, and A. Pérez-Uribe, Eds. (Heidelberg, Germany: Springer-Verlag, 1998, ISBN 3-540-64954-9, 383 pp.) Reviewed by Julian F. Miller.

The conference on evolvable systems grew out of a workshop entitled “Toward Evolvable Hardware” which took place in October 1995 at the Logic Systems Laboratory in the Department of Computer Science of the Swiss Federal Institute of Technology in Lausanne. The first ICES conference took place in October 1996 at the Electrotechnical Laboratory in Tsukuba, Japan. The ethos of ICES has been evolutionary electronic engineering in which traditional design methodologies have been replaced by direct attempts to evolve machines to achieve a desired level of behavior. In the first workshop there were just 11 contributions largely from Switzerland, Japan, and the United Kingdom. One year later there were 33 papers divided into nine topics: invited talks (three), overview (three), evolvable (four), cellular systems (two), engineering applications of evolvable hardware (two), evolutionary robotics (four), and innovative architectures (four). Eighteen were from Japan, five were from Switzerland, two each from the United States and the United Kingdom, and one each from Germany, Japan, and Brazil. Many of the papers were preliminary attempts at the newly coined field of “evolvable hardware.” There were also quite a few papers which provided overviews of the subject area. The conference did much to establish promising research areas within the general theme of evolvable systems: extrinsic (off line), intrinsic (on line), gate- and function-level evolution, evolvable, embryonic, non-Von Neumann computing architectures, and evolution in silico.

There were also some groundbreaking contributions using actual electronic hardware, most notably, Thompson’s pioneering work [5] on the intrinsic evolution of a frequency discrimination task directly in hardware. He famously demonstrated the extraordinary process whereby a 10 × 10 array of cells of a digital field programmable gate array (FPGA) could through blind evolution (a genetic algorithm) and physical testing be taught to construct a circuit which could discriminate between two square wave signals (1 and 10 kHz). The circuit used was very compact and utilized the electronic/electrical properties of the underlying silicon substrate. Goeke et al. [1] presented a hardware implementation of a cellular programming algorithm which could solve computational tasks (e.g., global synchronization), but whose only external connection to the outside world was via the power supply cable, thus in their view implementing on-line autonomous evolution, or evolware.

In Evolvable Systems 1998—Proceedings of the Second International Conference on Evolvable Systems: From Biology to Hardware (ICES’98), there were 38 papers mainly from the United Kingdom (ten), Japan (nine), United States (five), and Switzerland (four), with the rest being largely from Europe. Twenty-six papers were given as talks and the remainder as posters. The papers were divided into the following categories: evolution of digital systems (12), evolution of analog systems (five), embryonic electronics (four), bio-inspired systems (four), artificial neural networks (four), adaptive robotics (two), adaptive hardware platforms (six), and molecular computing (one). It is not possible in the scope of this review to examine all of the contributions.

Japanese researchers are at the leading edge in real-world applications of evolvable hardware. Many of these are based at the Electrotechnical Laboratory in Tsukuba under the guiding hand of T. Higuchi. Kajitani et al. described their work on the implementation and application of a gate-level evolvable hardware large-scale integration (LSI) chip with embedded reconfigurable hardware and genetic algorithm (GA). Such a chip makes it possible to make an evolvable hardware unit which is small and light enough to put in a myoelectric artificial hand. Their paper describes how they implemented a steady-state GA with uniform crossover, and an elitist recombination strategy [4]. The reconfigurable logic was in the form of a programmable logic array (PLA). They first showed that the hardware-implemented GA ran 62 times faster than the same GA running on a Ultra Sparc 2 (200 MHz). The intended application for the chip was to improve the time taken for a human to adapt to a myoelectric artificial hand. Currently, it takes a human subject about a month to become adapted to a conventional artificial hand. Neural networks with back propagation have been used but the training time for the network is very long. They showed that with the evolvable hardware approach, the artificial hand could be more accurately controlled and required substantially less training time.

A couple of authors examined data compression. Building on the work of Salami [3] at ICES’96, Tanaka et al. describe a data compression system using evolvable hardware for a digital electrophotographic (EP) printer. Essentially a GA was used to create a pixel template which could then be used for pixel value prediction. The template could be adapted and improved by the GA while the image was being scanned. The paper described an entire hardware system which would be able to compress image data and reconstruct it. The authors showed in simulation that the evolvable hardware produced superior compression ratios for EP (e.g., global synchronization), but whose only external connection
Stoica et al., who are based at the Jet Propulsion Laboratory at Caltech, describe in their paper on evolvable hardware for space applications the need for low-power, adaptive, hardware for use in automatic spacecraft. Given the safety-critical nature of spacecraft control systems, they suggest that there is a potential role for evolvable hardware systems in sensor adaptation and sensory information processing systems. These tasks can be broken down further into: signal acquisition (e.g., sensor sensitivity, activity), signal preprocessing (e.g., filtering, amplification), information extraction for on-board decisions (e.g., sensor-pointing), and signal preparation for transmission (e.g., compression). Authors have often alluded to the likely usefulness of evolvable hardware for space applications but have not provided any specific examples. Therefore, this paper was a welcome addition to the literature of evolvable hardware. Stoica et al. point out that, for spacecraft with on-board evolvable hardware, image compression could usefully take place either intrinsically (evolving image compression in hardware on the spacecraft) or extrinsically (in the latter case, by sending exemplar images back to earth, where a specially adapted FPGA might be evolved and subsequently uploaded to the spacecraft). To investigate the feasibility of this concept they developed an efficient genetic programming (GP) system for nonlinear predictive lossless image compression. They showed that they could obtain image compression which was competitive with standard methods. They also described some experiments in intrinsic evolution on a programmable analog neural network chip for analog function learning and vision-motor tracking for a mobile robot.

There was a marked increase in the number of papers concerned with analog evolution. This was partly due the recent availability of reprogrammable analog devices. Murakawa et al. show how one could evolve the configuration of the hardware to construct intermediate frequency filters (IF). If filters are widely used in cellular phones. The natural tolerances of analog components often mean that the cellular phone will not be tuned to the center frequency. By evolving the hardware configuration of the chip that they designed, however, it is possible to meet the stringent specifications required by the mobile phone industry.

Evolving analog circuits extrinsically is not likely to be practical unless one is extremely careful about the assumptions made by the simulation software. Zebulum et al. examine this by evolving amplifier circuits extrinsically using the SMASH simulator but with the addition of further constraints. They subsequently actually built the circuits and compared the real and the simulated circuits. Simulators assume user knowledge so that using them “blind” can lead to evolved circuits which are not practically implementable; such a situation can happen, for instance, when the simulator does not handle overcurrent and overvoltage conditions. The authors show that by carefully taking these factors into account, one can obtain simulated circuit behavior which is in close agreement with actual behavior.

Evolvable hardware, rooted as it is in hardware or hardware implementable models, is seen by some as an inherently applied field of research where the objective is simply to develop real-world applications as swiftly as possible. This view is premature and places an unnecessary pressure away from more fundamental science. The use of electronic circuits has developed extraordinarily fast in the second half of this century. Such an enormous weight of modern electronic technology can lead people to imagine that the way circuits are designed is somehow finished and precise. Evolvable hardware might be seen as a process of using novel algorithms to merely connect standard components together. It is hard to overstate the narrowness of this view. When components are connected together and the circuit’s effectiveness measured without the use of human design principles, a cornucopia of new possibilities emerge. The circuits may function in entirely unknown ways, and may exploit subtle, physical properties, which can only be guessed at. Such an approach to evolvable hardware was pioneered by Thompson at ICES’96. His follow-up paper on this work, presented at ICES’98, set out to investigate whether robust circuits could be designed which would function correctly within a given operational envelope. The paper describes the construction of the so-called “Evolvatron,” an apparatus which allowed the evolution of circuits on five FPGA’s under a variety of conditions: silicon batch, temperature, temperature-gradient, circuit position, and electronic surroundings, packaging, and power supply. He demonstrated that some circuits worked well in three different operating conditions, showing partial robustness was being obtained. Moreover, the more robust circuits were not obviously more complex than those obtained on a single FPGA. The circuits which performed well in one set of conditions could be quite quickly adapted to perform well in another scenario.

Huelsbergen et al. looks at the intrinsic evolution of oscillators using the Xilinx 6216 FPGA. They found that it was relatively easy to evolve circuits which oscillated at harmonics of the target frequency. They also observed a temperature-dependent behavior. Interestingly their circuits would still work when implemented on other chips of the same type (with a shift in oscillation frequency).

One of the difficulties with evolving circuits on proprietary FPGA’s is that one cannot examine the internal signals, neither can one change the basic components (e.g., logic gates). Layzell described his work on the construction and use of an “evolvable motherboard.” This is an array of programmable crosspoint switches which can connect together a number of “plug-in” circuit elements. With this device it is possible to inspect any internal signals and thus investigate the way an evolved circuit is able to function. The evolvable motherboard may well become an important fundamental research tool in this area.

Hayworth introduces a new approach to analog intrinsic evolution called the “modeling clay” approach. This employs a vector field, a state-space representation of an electronic circuit. He has built a simple prototype analog computer to test these ideas out. This is a thought-provoking approach and subsequent results will be interesting.

Koza’s work in the field of extrinsic analog circuit synthesis is well known [2], so it was interesting to see this method becoming an inspiration for further development. Lohn and Colombano have developed a linear chromosome representation with simple component connection opcodes for connecting resistors, inductors, and capacitors within a limited range of topologies. They were able to evolve some passive analog filters using the SPICE simulator.

Categorizing papers in this field is difficult but it would have been useful to distinguish between intrinsic and extrinsic evolution of circuits. Some papers were categorized as being digital which could easily have been regarded as analog. Really the divisions between these areas are quite fuzzy.

This Proceedings as a whole will be essential reading to all researchers interested in evolvable hardware. There are still many fundamental questions to be investigated by future researchers. Will it be possible to evolve robust systems? What type of chip architectures and components will be best for evolving new circuits? Can new principles of circuit design be discovered by studying evolved circuits (both digital and analog)? What new real-world applications will develop? These are just a few of the interesting questions which will occupy the still growing and developing field of evolvable hardware.
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