FULLY FPGA-BASED IMPLEMENTATION OF A MODIFIED CONTROL STRATEGY FOR POWER ELECTRONIC TRANSFORMER IN RAILWAY TRACTION APPLICATIONS

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Abstract
Due to its several advantages (especially low volume and weight), power electronic transformer has gained notable attraction in railway applications. The main focus of this work is devoted to development a fully filed programmable gate array (FPGA)-based control platform for power electronic transformer in the aforementioned application. Due to the parallel processing of FPGAs that results in a faster control algorithm execution, reliable operation (which is of major importance in traction applications) is guaranteed. For this purpose, an input series output parallel power electronic transformer structure is built, and various considerations for reliable and stable operation of the power electronic transformer in traction applications, such as safe start-up and bidirectional power flow, along with the required control and pulse generation schemes, have been designed and implemented in a Xilinx FPGA control platform. Moreover, a modified control algorithm is proposed for controlling the power electronic transformer in a simple and more reliable manner. This control scheme is developed based on the output voltage of the DC–DC–LLC resonant converter, and can effectively control the sum of rectifier DC-link voltages and track the input sine reference current, with a lower number of required sensors. Finally, the effectiveness of the proposal has been tested from various aspects by experimental tests.

1 | INTRODUCTION

The electric railway system has been highly developed today, due to its several advantages such as being convenient, economical and making possible the massive transportation [1]. The main research efforts in the field of modern electric railways concentrate on improving the speed, efficiency and reducing the system volume and weight. A notable amount of the overall weight of these systems is the line-frequency bulky transformers [2]. In order to solve this issue, the power electronic transformers (PETs) have been proposed, which significantly reduce the weight and volume by employing a high-frequency transformer (HFT) in their configuration [3]. Besides, they can provide several other advantages such as more controllability and four-quadrant operation, compared to the conventional transformer. These advantages could be efficiently achieved through employing a control scheme implemented in a digital control platform [4].

By reviewing the literature, it could be seen that most research efforts on power electronic transformer (PET) have been devoted to different control objectives such as power control [5], voltage balancing [6] and also topology improvement [7–10]. In order to realise efficient performance of the PET, appropriate voltage-balancing strategies and power-sharing schemes between different cells of the PET should be employed. Moreover, several configurations are suggested for different applications. For instance, PET implementations based on conventional [7] and SiC semi-conductors [8] have been studied. Also, in order to fulfil the requirements of the medium-voltage high-power applications, modular multilevel converters [9] and CHB topology [10] are proposed and developed. The most popular configuration for the PET in traction application is composed of a single-phase cascaded H-Bridge (CHB) as the active front end (AFE) rectifier, and several parallel DC–DC–LLC resonant converters. This structure is called input series output parallel PET [11].
To balance the output voltage of CHB-AFE and also realise output power sharing of parallel DC–DC converters, She et al. [12] suggest a straightforward solution based on the PET model in dq reference frame. Also, this work proposes a power-balancing strategy for PET in traction applications, which eliminates the sensors used for measuring the inductor current. In the later strategy, the CHB converter is controlled based on the power component of duty-cycle controller, while the DC–DC stages are controlled based on a feed-forward strategy. However, it should be noted that the efficiency of the DC–DC parallel stages could be low, due to the single-phase shift (SPS) control. Some modified SPS schemes are suggested in [13–15] in order to improve the PET efficiency. However, these approaches suffer from relative complexity for hardware implementation.

On the other hand, the real-time hardware implementation of the PET control algorithm could face many challenges in practical applications such as traction railway systems. If a control platform with a single digital signal processor (DSP) chip is employed, some major problems such as low number of PWM units for high-voltage systems, and limited sampling rate value would exist. In [16], a single-phase PET has been realised through employing a digital control platform, which is composed of DSP and PIC controllers. Moreover, the combination of FPGA and DSP is studied in [17–19] in grid-connected applications. In these works, since there are two different controller ICs, there may exist a communication delay. Moreover, development and implementation of the control algorithm in these control platforms needs significant prior knowledge.

This paper employs a control platform based on a single FPGA chip in order to implement the control and pulse generation algorithms of PET for railway traction applications. This would solve the issues regarding the multiple-chip control platforms mentioned above. Moreover, the designed control algorithms are more reliable and could be implemented with a very high sampling rate, by taking advantage of the parallel-processing capability of the FPGAs. Also, a novel control algorithm based on the output voltage value is proposed with a lower number of voltage sensors, which results in controlling the PET in a simple, more reliable and cost-effective manner for traction applications.

2 | PET CONFIGURATION FOR RAILWAY TRACTION APPLICATIONS

The PET configuration for traction applications generally consists of \( N \) two-stage cells. A two-cell topology is depicted in Figure 1. Both PET stages, that is, AC–DC and DC–DC converters, provide bidirectional power flow capability. The AC–DC stage of each cell is an AFE H-bridge rectifier and is connected in series with the AC–DC stages of the other cells. This topology is called CHB topology. The inductor used at the input of CHB is responsible for boost operation of the AFE rectifier, improving the quality of the input current and protection against short-circuit current. The DC–DC stage consists of a DC–DC–LLC resonant converter, which is made of two full-bridge converters, an HFT, a high-frequency inductor and a resonance capacitor. The output of DC–DC stages in different cells is connected in parallel. In order to efficiently design the corresponding controllers, it is necessary to develop appropriate models for AC–DC and DC–DC stages. These models are described in the next subsections.

2.1 | AFE H-bridge operating principles and modelling

The H-bridge topology of a single cell is shown in Figure 2. According to this figure and considering unipolar modulation,
four possible switching states could be distinguished for this topology, which are listed in Table 1. According to this table, the I and IV states are same. Moreover, two of the distinguished switching states have the same equations. By writing state equations for the equivalent circuit of different switching states, the matrix form of the converter state equations will be as follows:

\[
\dot{x} = A_1 x + B_1 u \\
\dot{y} = C x,
\]

where

\[
x = \begin{bmatrix} i_s \\ u_c \end{bmatrix}, \quad u = \begin{bmatrix} u_i \end{bmatrix}
\]

\[
A_1 = \begin{bmatrix} \frac{R_s}{L} & -1/L \\ 1/C & -1/R_1 C \end{bmatrix}, \quad A_2 = \begin{bmatrix} -R_s/L & 0 \\ 0 & -1/R_1 C \end{bmatrix}
\]

\[
B_1 = B_2 = \begin{bmatrix} 1/L \\ 0 \end{bmatrix}
\]

\[
C = \begin{bmatrix} 0 & 1 \end{bmatrix}.
\]

In order to obtain the small-signal equations of the system, the average model and also the steady-state equations of the converter should be achieved. The average state matrices are provided in the Appendix.

2.1.1 | Steady-state equations

In order to determine the operating point, the converter should be modelled in the steady-state condition, by omitting the derivative terms. The steady-state model equations could be found in the Appendix.

2.1.2 | Small-signal equations

Before determining the small equation, the \( A, B \) and \( C \) matrixes could be defined as follows:

\[
A = A_1 D + A_2 (1 - D) \tag{4}
\]

\[
B = B_1 D + B_2 (1 - D) \tag{5}
\]

\[
C = C_1 D + C_2 (1 - D), \tag{6}
\]

where \( D \) is the duty cycle. As the coefficients of the state matrixes are constant for all the operating points; therefore, the small-signal model will be same for different operating points. The deviations of different variables at the operating point are as follows:

\[
\tilde{x} = x + \dot{x}
\]

\[
\tilde{u} = u + \dot{u}
\]

\[
\tilde{d} = D + \dot{d}
\]

\[
\tilde{y} = y + \dot{y}.
\]

In the above equations, \( \tilde{x}, x \) and \( \dot{x} \), represent the operating point, large signal and deviation variables, respectively. By substituting the above equations in (4)–(6), and omitting the multiplication of two small deviation terms, the final small-signal state equations of the AFE rectifier are as follows:

\[
\begin{align*}
\tilde{x} &= A \tilde{x} + B \tilde{u} + ((A_1 - A_2)x + (B_1 - B_2)u) \tilde{d} \\
\tilde{y} &= C \tilde{x} + (C_1 - C_2)x \tilde{d}.
\end{align*}
\]

According to the calculated state equations, the transfer functions of the AFE H-bridge are as follows:

\[
\begin{align*}
\frac{\tilde{i}_s}{\tilde{u}_i} &= \frac{R_l Cs + 1}{R_l LCs^2 + (R_l R_1 C + L)s + R_s + D^2 R_l} \\
\frac{\tilde{u}_c}{\tilde{i}_s} &= \frac{R_1 L_i s - R_l D u_c + R_s R_l i_s}{-R_l C u_c s - R_l i_s D - u_c}.
\end{align*}
\]
Finally, it should be noted that all the equations of different models developed above are for a single H-bridge topology. For modelling the overall active front end cascaded H-Bridge (AFE-CHB), the sum of the all capacitors should be considered in these equations.

2.2 DC–DC–LLC resonant converter operating principles and modelling

An extremely important part of the PET configuration is the DC–DC–LLC resonant converter, which is depicted in Figure 3. As shown in this figure, two full-bridge structures are employed at each side of the HFT. The HFT is the most important component, which is responsible for matching the high- and low-voltage DC links with a galvanic isolation, and realising soft-switching operation. Moreover, an LLC circuit is employed in the topology of the DC–DC stage. In order to completely form the LLC circuit, an external capacitor should be used besides the HFT. To design and characterise the LLC resonant circuit, the two resonant frequencies that are resulted by the leakage (\(L_r\)) and magnetising (\(L_m\)) inductances, and the resonant capacitor (\(C_r\)) are considered:

\[
f_o = \frac{1}{2\pi \sqrt{L_r C_r}} \quad (12)
\]

\[
f_p = \frac{1}{2\pi \sqrt{(L_r + L_m) C_r}} = \frac{f_o}{\sqrt{1 + L_m/L_r}}, \quad (13)
\]

where the ratio of \((L_r + L_m/L_o)\) is represented by \(L_n\).

Figure 4 depicts the LLC resonant circuit gain versus the normalised switching frequency diagram, for different values of \(Q\) (the LLC impedance ratio to the equivalent load impedance) and \(L_n = 17\). According to this figure, this gain will be independent of the load value in the vicinity of the operating points with a switching frequency equal to the resonant frequency defined in (12). This value is nearly 1. Therefore, a 50% duty cycle at a fixed switching frequency is considered, where the input-to-output voltage ratio of the DC–DC stage will be determined by the transformer turns ratio. In this condition, one side operates as diode rectifier and the other side experiences switching, based on the power flow direction. The best operating point for the LLC circuit will be in the frequency region of \(f_p < f_s < f_o\). In this region, the primary side switches will operate at zero voltage switching (ZVS) condition (during the forward operation condition), and will turn off at the maximum value of the magnetising current. Moreover, the secondary side rectifier will operate at zero current switching (ZCS). These will result in the decrease in the losses.

Since this stage operates in the steady-state condition, the transient components could be approximately omitted. Moreover, as the LLC circuit variables have nearly sine waveforms, they could be approximated using their first-order harmonic. On the other hand, the non-linear terms can be approximated using extended describing functions, by their DC or main fundamental harmonic. These will finally result in achieving the reduced large-signal state equations, which could be linearised employing the Taylor expansion and then, the corresponding transfer functions are obtained.

Figure 5 depicts the equivalent circuit of the DC–DC–LLC resonant converter. According to this figure, the state equations are as follows:

\[
L_r \frac{di_{L_r}}{dt} = -R_p i_{L_r} - L_m \frac{di_{L_m}}{dt} - u_{Cr} + u_{ab} \quad (14)
\]

\[
L_m \frac{di_{L_m}}{dt} = \text{sgn} (i_{L_r} - i_{L_m}) u_{on} \quad (15)
\]

\[
C_r \frac{du_{Cr}}{dt} = i_{L_r} \quad (16)
\]
Approximation of variables

Steady-state equations

Small-signal equations

The typical input waveform of the LLC circuit, where its pulse width is determined using the phase-shifted modulation or the duty-cycle change, can be approximated using a sine term that its Fourier series is as follows:

\[ f_1(t) = b_1 \sin \omega_c t = \frac{4}{\pi} u_{in} \cos \phi \sin \omega_c t. \]  

(21)

If the pulse width modulation is considered:

\[ u_{ab} = \frac{4}{\pi} u_{in} \cos \left( \frac{\pi}{2} - d\pi \right) \sin \omega_c t = \frac{4}{\pi} u_{in} \sin (\pi d) \sin \omega_c t \]

for \( 0 < d < \frac{1}{2} \) .

(22)

Since \( u_{Cm} \), \( i_{L,m} \), and \( i_{L} \) have nearly sine waveforms, they can be approximated by their first-order sine and cosine components. By this approximation, each state variable is decomposed into two different variables and considering the output voltage, the state equations would include seven variables in overall:

\[ i_{L,m} \approx i_{m} \sin (\omega_c t) + i_{m} \cos (\omega_c t) \]  

(24)

\[ u_{Cp} \approx u_{p} \sin (\omega_c t) + u_{p} \cos (\omega_c t) \]  

(25)

By derivation and rearranging the above equations, the approximated equations are achieved as follows, based on replacing the non-linear terms with their DC and first-order harmonic components:

\[ I_L \frac{di_{rs}}{dt} = -R_{r}i_{rs} + L_{m} \omega_{c} i_{rs} - u_{rs} - \frac{4n_{in} - i_{ms}}{\pi} u_{Co} \]

\[ + \frac{4}{\pi} u_{in} \sin (\pi d t) \]  

(26)

\[ I_L \frac{di_{rs}}{dt} = -I_L \omega_{c} i_{rs} - R_{l}i_{rs} - u_{rs} - \frac{4n_{in} - i_{ms}}{\pi} u_{Co} \]

(27)

\[ I_{in} \frac{di_{ms}}{dt} = I_{in} \omega_{c} i_{ms} + \frac{4n_{in} - i_{ms}}{\pi} u_{Co} \]

(28)

\[ I_{in} \frac{di_{ms}}{dt} = -I_{in} \omega_{c} i_{ms} + \frac{4n_{in} - i_{ms}}{\pi} u_{Co} \]

(29)

\[ C_{L} \frac{du_{Co}}{dt} = i_{rs} + C_{L} \omega_{c} u_{rs} \]

(30)

\[ C_{L} \frac{du_{Co}}{dt} = i_{rs} - C_{L} \omega_{c} u_{rs} \]

(31)

\[ C_{L} \frac{du_{Co}}{dt} = \frac{R_{o}}{R_{o} + r} \left( \frac{2n_{in}}{\pi} i_{o} \right) - \frac{4}{\pi} i_{p} \]  

(32)

2.2.1 Approximation of variables

The steady-state model could be achieved from the above large-signal equations, by considering all derivatives and the output current \( i_{o} \) to be 0. The resulted equations could be found in the Appendix.

2.2.2 Steady-state equations

Small-signal equations

In order to control the desired output variables, a small-signal model should be developed for identifying the system performance against changes. The small-signal equations could be obtained as in (33)–(40), by similar procedure discussed for the AFE-CHB stage, and based on decomposing the operating point state variables into large signal and deviation variables, and rearranging the equations:

\[ \frac{\hat{di}_{m}}{dt} = -\left( \frac{R_{p} + k_{i_{m}}}{I_{m}} \right) \hat{i}_{m} + \left( \frac{\omega_{c} + k_{i_{m}}}{I_{m}} \right) \hat{i}_{m} + k_{i_{m}} \hat{\omega}_{c} \]

\[ -\frac{k_{i_{m}} \hat{\omega}_{c}}{I_{m}} i_{m} - \frac{1}{I_{m}} \hat{u}_{rs} - \frac{2k_{u_{p}}}{\omega_{c}} \hat{u}_{Co} + k_{u_{p}} \hat{i}_{m} + k_{u_{p}} \hat{\omega}_{c} + i_{p} \hat{\omega}_{s} \]

(33)
The definitions of various parameters in above equations are provided in the Appendix. Finally, it should be mentioned that the required transfer functions for designing the control system could be achieved by applying the Laplace transform to the above equations.

3 PET CONTROLLER DESIGN

In this section, the required controllers for the AFE-CHB rectifier and DC–DC–LLC resonant converter stages of the PET are designed, based on the transfer functions determined in the previous sections. Then, a modified controller is proposed based on the output voltage of the PET.

3.1 Design of the AFE-CHB controller

The configuration of the AFE-CHB rectifier controller, which consists of the voltage and current control loops, has been depicted in Figure 6. The voltage control loop is responsible for maintaining the sum of AFE-CHB DC link voltages at the desired value. On the other hand, the current control loop provides the input reference sine waveform, based on the desired input power factor. Since the input current has a sine waveform, the Proportional-Resonant (PR) controller is used in our work.
in order to improve the control performance. The output of the current control loop generates a sine reference waveform, which is then compared with the carrier waveform.

The voltage control loop of the AFE-CHB rectifier, which includes a Proportional-Integral (PI)-type controller, has been shown in Figure 7. The transfer function \( u_c/\mathcal{L}_c \) is required for the voltage control loop. By substituting the designed PET parameters, this transfer function will be as follows:

\[
G \left( \frac{U_c}{I_c} \right) = \frac{162.5}{s + 5} \tag{41}
\]

The simplified model of the voltage loop transfer function is \(1/C_{qu} s\), which can be used.

Figure 8 shows the current control loop, which consists of a PR controller with the transfer function shown in (42).

\[
G_c (I_s) = K_p + \frac{2K_i s}{s^2 + \omega^2}
\]

In this equation, \( K_p \), \( K_i \), and \( \omega \) are, respectively, the proportional and resonance gains, and the resonance frequency. The required transfer function for the current control loop is \( I_s/U_s \), which is calculated as follows, based on the PET parameters:

\[
G \left( \frac{I_s}{U_s} \right) = \frac{500s + 2500}{s^2 + 51s + 53,050} \tag{43}
\]

The simplified form of the control current transfer function is \(1/(L_s s)\). Finally, the controller coefficients are determined using the tuning tools of the MATLAB/Simulink software.

Considering the calculated coefficients for current and voltage control loops, the closed loop transfer function will be as follows:

\[
\frac{u_c}{u_c^*} = \frac{1.145 \times 10^8 (s + 23.64) (s^2 + 400s + 9.86 \times 10^4)}{s^2 + (s + 9754) + (s + 135.8) + (s^2 + 110 + 1.86 \times 10^5)} \tag{44}
\]

Figure 9 shows the bode diagram of the current control loop for the open and closed loop cases. As it is obvious in these figures, the PR controller has a notable gain in a small range at the grid frequency.

Figure 10 depicts the transfer function of \( u_c^*/u_c \), which corresponds to both the current and voltage control loops. According to the frequency response, the system has a gain margin of 15.3 in gain crossover frequency of 77 Hz, and a phase margin of 54° in phase crossover frequency of 7.7 Hz. Therefore, the system is stable for a wide range of the loads. Moreover, suitable values are considered for the phase and gain margins, in a way that the system response would be fast and also the oscillations are low.

### 3.2 DC–DC–LLC resonant converter control scheme

Figure 11 depicts the control block diagram for the DC–DC stage, which consists of the voltage control loop of the parallel cells. The output of the DC–DC stage could be controlled via two parameters: (a) duty cycle; (b) converter switching frequency. The fixed duty-cycle control scheme can be employed due to its superior efficiency performance. Moreover, only one of the H-bridges is active in DC–DC–LLC resonant topology at each instance, based on the forward or backward operation. A controller is used for recognising the operating condition. The operating principles of this controller is such that when the output voltage exceeds the upper band limit, the backward state is activated; and when the output voltage is below the lower limit, the forward state is employed.

### 3.3 Proposed simplified control scheme for the PET

The block diagram of the proposed simplified control scheme is depicted in Figure 12. In the traditional controller, the block diagrams in Figures 6 and 11 are performed together. Therefore, it is required to measure all the output voltages of the AC–DC stages. In the proposed control algorithm, by only measuring the PET output voltage with only one voltage sensor, the control goals could be fulfilled. If the number of input cells is high, the required voltage sensors and the corresponding ADC units are reduced from \( N \) to 1 by the suggested method; and hence, the system reliability is increased and the cost of the system is reduced. Moreover, the PET output voltage could be directly controlled by this control scheme. In order to calculate the PI controller coefficients, the dynamics of the DC–DC–LLC resonant converter could be neglected. As a result, the output voltage is simply multiplied by the cell numbers and also the transformer turns ratio, in order to control the input stage. Finally, it should be mentioned that in the proposed control scheme, the DC–DC stage operates with a fixed duty cycle. Moreover, a hysteresis controller is employed for recognising the forward or backwards modes. The operating principles of this deadbeat controller are like what was discussed in Section 3.2.
4 FPGA IMPLEMENTATION OF THE CONTROL SCHEME

This work employs the control platform that is designed based on the XC6SLX45 chip, manufactured by Xilinx. Since the FPGA chips do not have analogue inputs, four AD9231 chips, which are 20 mega samples per second (MSPS) ADCs, are used. In order to eliminate the high-frequency noises, low-pass filters are employed at the input of these ADCs. In order to implement the designed continuous controllers in s-domain into the FPGA platform, they were firstly discretised and transformed into the z-domain, employing the backward transformation, in which the s operator is replaced with \[ \frac{z-1}{z} \]. The Xilinx Signal Generator blocks are employed to implement and simulate the control algorithm in MATLAB. Next, a module of codes is generated from this model, which could be employed in ISE. Other components such as ADC, clock generation and virtual input–output units could be also considered in ISE. When the controller is implemented in the ISE, all different parts of the developed code can be executed simultaneously and in the parallel form; since the logic sources in the FPGA chip can be configured and operate independently. This fact not only significantly improves the reliability but would nearly eliminate the restriction regarding the sampling rate is DSPs, which is of high
importance, especially during fast dynamic changes. Finally, note that ISE automatically applies some optimisation procedures during executing the developed code, by considering a trade-off between the amount of code and execution speed. In order for capturing the waveforms and debugging purposes, the ChipScope tools of the ISE software are employed.

Figure 13 presents different parts of the overall control scheme implemented in the FPGA chip, using the MATLAB System Generator. Figure 13(a) depicts the overall schematic of the AFE-CHB switching and control strategies. As the first stage, the grid voltage and current, and also the PET internal voltages are measured and after passing ADC units, are used as the algorithm inputs. These variables are fed into an low pass filter (LPF) and gain block, in order to attenuate the noises and improve their signal quality. Next, block 2 determines whether the conventional or proposed method is selected. The phase-locked loop (PLL) (block 3), which is of TD type, determines the grid current reference angle, using the grid voltage and reference reactive power (lagging or leading). In order to calculate the reference current magnitude, the main voltage controller (block 4) is employed, which consists of the designed controllers and their corresponding coefficients. After passing through a rate limiter that smoothens its sudden changes (especially during start-up), the reference DC voltage is compared with its real value and the resulted error is fed to this block. In the next stage, the reference magnitude and angle of the input current are combined in block 5 and compared with the real input current. The resulted error is used as the input of current control loop (block 6). This stage generates the appropriate modulation index, considering the calculated controller coefficients in the last section. Finally, the unipolar modulation is responsible to determine the switching states. Figure 13(b) shows the employed TD-type PLL structure, which is based on \(\alpha\beta\)-dq transform. Since its input voltage is single phase, a 90° delay of this voltage is used as the second input. Then, the output \(q\) component is used for regulating the PLL. The output of the internal PI controller is added to reference \(\omega\). By integrating this value, the angle is determined. Figure 13(c) presents the DC–DC stage controller. The output low voltage (LV) voltage is fed to this part as the input. Based on the value of this voltage and also the limits of the hysteresis controller, the forward or regenerative mode is activated. After selection of the operation mode, the switching pulses for this stage are determined with a fixed duty cycle. Figure 13(d) depicts different protections considered for the PET. These include the PLL enable command, overcurrent and overvoltage protections and the user enable command. Finally, Figure 13(e) depicts the digital implementation of the PI controller. Moreover, the anti-wind-up function has been considered by the \(K_c\) gain, in order to compensate the integral component operation.

5 | HARDWARE IMPLEMENTATION RESULTS

In order to evaluate the effectiveness of the developed control platform and also verify the performance of the designed controller different aspects, a laboratory-scale PET (Figure 14) has been built. Different parameters of the designed PET have been shown in Table 2. These parameters are calculated based on the rated power and operating voltage and frequency of the scaled-down prototype. The semi-conductor switches for the AFE-CHB are IKW30N60T IGBTs, with a maximum voltage and current ratings of 600 V and 30 A. Two 1 mH inductors have been employed in series at the input of the PET. It should be noted that in a real-scale PET, semi-conductor devices with higher voltage and current ratings should be employed at the AC–DC stage, and their switching frequencies are significantly lower. Moreover, a lower value of inductance is utilised at the input. The switches of the DC–DC stage are implemented by 2SK3681 MOSFETs, which their voltage and current ratings are, respectively, 600 V and 40 A. Also, two variable resistors are used as the output loads. Each of the series-connected AC–DC H-bridge cells operates in the boost mode; and provides a higher voltage than its input, at the high voltage (HV) DC-link capacitor. The value of the DC-link capacitors has been determined based on the maximum allowable CHB-AFE output voltage ripples, which is 2% in our work. In a real-scale system, the maximum allowable ripple is more (5%, for example), and these capacitor values could become smaller. Moreover, the area product approach has been considered for designing the HFT [20]. The PQ cores have been use for both the HFT and inductors, due to their reduced leakage flux. The sampling rate considered for implementing the controller in the FPGA-based control platform is 10 MHz. Note that if the controller was intended to be implemented on a DSP chip, the sampling rate could not go further than a few tens of kilohertz. On the other hand, the sampling rate for FPGAs is not restricted by the minimum time needed for algorithm execution, due to the parallel-processing feature. However, some factors such as resolution of
calculations and ADC conversion rate are considered for choosing the sampling rate for FPGAs. Moreover, the main clock frequency and conversion rate of the ADC blocks are, respectively, 100 MHz and 40 MSPS. Finally, it should be mentioned that due to the laboratory limitations, the tests have been conducted at the half of the nominal voltage.

5.1 | PET start-up

In the start-up condition, due to the small input impedance, charging of high-voltage DC-link capacitors, the inrush current of the high-frequency transformer and charging of the output capacitors, the PET will draw a significant current from the grid. In order to limit this current and protect the devices, a start-up circuit, which includes that a series resistance is required. The value of the employed resistance here is 1.6 Ω. Figure 15(a) depicts the start-up waveform. In this figure, the HV DC-link voltage, grid current and voltage, and also the input voltage of the CHB configuration \(v_r\) are shown. The maximum current is 82.4 A in this condition, which reaches zero after 150 ms. The HV DC-link capacitors are charged to 160 V. In order to limit sudden changes of the grid current in Figure 15(a) (that is due to voltage change of the high-voltage DC link), a start-up scheme for the PWM rectifier control is also considered and the results are shown in Figure 15(b) and (c). In the start-up instance, the voltage reference value is set to its minimum value (10% of the grid voltage) and after start-up, the voltage value will increase to the nominal value, with the rate of 20 V/s. As it is shown in Figure 15(c), the start-up scheme of the control strategy will be activated at the first zero-crossing point of the grid voltage and this results in the decrease of the current.

5.2 | Load change

The PET controller should be robust against instantaneous load changes. In order to verify this, a load change from 60 to 1080 W and vice versa has been considered and the results are shown in Figure 16. According to this figure, the output voltage overshoot will reach 10 V for the load change case. It should be mentioned that in a real-scale high-power PET, this overshoot value will be significantly lower, due to the smaller DC-link capacitances. Also, the response time is 200 ms. Moreover, with the increase in load, the output voltage oscillations’ magnitude will approximately increase by 2.5 V. Due to the control algorithm performance, the PET is stable and the output average voltage will remain unchanged in this case.

5.3 | Input voltage change

The proposed controller for PET can effectively maintain the output voltage value at its desired range, when the grid voltage is
changed. Figure 17 depicts the experimental results of this condition. According to this figure, the grid maximum voltage value has decreased by 58 V. With the decrease in the grid voltage, its current is increased; since the output load is fixed. However, the value of the output voltage remains completely the same before and after the voltage decrease. This verifies the grid voltage drop compensation by the designed controller for CHB-AFE.

5.4 Reactive power control

The designed controller is capable of providing reactive power control for the CHB-AFE. Figure 18(a)–(c) depict the experimental results of the reactive power control with the unity, inductive and capacitive power factors. Figure 18(a) depicts the normal condition of the CHB-AFE with unity power factor, where the root mean square (RMS) value of the input current is 5.5 A. By changing the reference output of the PLL by 60° (lagging), the results in Figure 18(b) are obtained. In this case, the grid current RMS value increases from 5.5 to 8.37 A, and an active power of 330 W is drawn from the grid. The waveforms of the system with a 60° reference leading power angle are presented in Figure 18(c). The RMS value of the current is 8 A in this case, which results in injection of 300 Var to the grid.

5.5 Regenerative operation

One of the most important advantages of PET, is the regenerative operation capability. The CHB-AFE stage inherently
provides the regenerative capability. In order to determine the DC–DC–LLC resonant converter operation mode, the output voltage is used and upper and lower limits are considered for its value. If this voltage exceeds the upper band due to the regenerative current injection, the regenerative mode is activated. As stated before, the primary side H-bridge of DC–DC–LLC resonant converter acts as a diode rectifier, and the secondary side H-bridge will be active in this condition. Figure 19 demonstrates the waveform for the regenerative mode. As it can be seen, there is a phase difference of $180^\circ$ between the grid voltage and current.

### 5.6 Current sharing performance

The experimental results of the output currents for both cells are shown in Figure 20. According to these waveforms, it is obvious that the values of these currents are equal (3.9 A); and hence, the output power is equally provided by the both cells. This is achieved since only two input cells are connected in series, and the switching frequency is fixed. Note that if there is a serious problem regarding current sharing performance in very high-power applications with $N > 2$, simple feedback controllers could be designed for current sharing; and easily implemented in the FPGA-based platform.

### 5.7 Grid current THD

The THD values of grid current waveforms with different magnitudes have been presented in Table 3. These values are less than 5% for a wide range of operating points (the ones above 15% of the nominal current magnitude); which would be acceptable according to well-known standards such as IEEE 519. Note that for a high-power PET, although the switching frequency and input inductance values are smaller, but the THD
performance would remain satisfactory, since the number of voltage levels are significantly increased, due to the higher value of $N$.

### 5.8 PET efficiency

The efficiency of the PET set-up for different loads has been shown in Figure 21. According to these results, the maximum efficiency is $90.43\%$. Moreover, the efficiency is more than $88\%$ for a wide range of output currents. Note that in a real-scale system, the switching losses of the AC–DC stage will be lower, due to the smaller switching frequency. Regarding the conduction losses, despite the increase of current magnitude, their value won’t significantly increase due to the lower values of $R_{on}$ for high-power switches. Therefore, the overall efficiency will not be degraded, and even could be improved.

### 5.9 Computational time analysis

In this subsection, the computational burden analysis is conducted for the developed algorithm. The execution time of an algorithm can be defined as the amount of the time between the instance of the input variables transfer from the ADC blocks to the FPGA unit; and finally obtaining the duty-cycle values at the FPGA unit output. If there was no delay, the whole algorithm could be performed in a single sampling period, that is, $1/10\,\text{MHz} = 100\,\text{ns}$, due to the parallel-processing capability of FPGA. However, there are several delays due to the existence of components such as input registers of different blocks, multiplier units, PI controllers etc. The total number of delay components between the input and output of our implemented algorithm is 18. Therefore, the total execution time would be $18 \times 100\,\text{ns} = 1.8\,\text{s}$. Moreover, the utilisation percentage of different FPGA chip resources is provided in Table 4.

### 5.10 LLC circuit currents at different loads

Figure 22 shows the input and output currents of the HFT. These waveforms are obtained for different loads with average output currents of 1.5, 7.5 and 13.6 A. The considered value for the magnetising inductance is $550\,\mu\text{H}$. According to this figure, the maximum magnetising current is $1.6\,\text{A}$. Moreover, as it
is obvious, the output current values are zero at the switching instance, which validates the ZCS operation of the output rectifier in a wide range of output loads. Also, the input H-bridge topology of this stage operates at ZVS condition.

TABLE 3 Grid current THD values

| RMS value (A) | THD (%) |
|---------------|---------|
| 1.059         | 5.62    |
| 1.45          | 5.68    |
| 4.94          | 3.54    |
| 8.89          | 2.85    |
| 11.21         | 2.86    |

6 | CONCLUSION

This research discusses a fully FPGA-based prototype of a single-phase PET for railway applications. The designed control platform includes a single Xilinx FPGA chip, along with other required components such as ADC blocks. The system generator package of the MATLAB software is employed, in order to easily implement different designed control loops and also additional requirements such a PLL, protection schemes etc. Moreover, some modifications have been made in order to simplify the traditional controller implementation and meeting the requirements of the traction application. According to the experimental results, it could be seen that the PET experiences...
In conclusion, the real-time high-power traction system implementation using a modular multilevel DC–DC converter demonstrated the feasibility of using such systems in practical railway applications. The developed control platform was shown to effectively control the converter operations, ensuring smooth start-ups with limited inrush currents and maintaining high efficiency and low grid current Total harmonic distortion (THD). The experimental results validated the design and performance of the traction system.

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APPENDIX
A.1 AVERAGE MODEL EQUATIONS OF AFE H-BRIDGE

\[ \dot{x} = \begin{bmatrix} -\frac{R_c}{L_c} & -\frac{D}{L} \\ \frac{D}{C} & -\frac{1}{R_c C} \end{bmatrix} \begin{bmatrix} i_s \\ n_c \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} u_i, \quad (A1) \]

\[ y = (C_1 D + C_2 (1 - D)) \begin{bmatrix} i_s \\ n_c \end{bmatrix}, \quad (A2) \]

where \( D \) is the duty cycle and \( C_1 \) and \( C_2 \) could be defined as in (10).

A.2 STEADY-STATE MODEL EQUATIONS OF AFE H-BRIDGE

\[ i_s = \frac{1}{R_s + R_i D} u_i, \quad (A3) \]

\[ u_c = \frac{R_i}{R_s + R_i D} u_v, \quad (A4) \]

A.3 STEADY-STATE MODEL EQUATIONS OF DC–DC–LLC RESONANT CONVERTER

\[ i_{v_r} = \frac{V_c}{\alpha^2 + \beta^2} \left( \alpha + \frac{L_m \omega \beta}{R_m} \right), \quad (A5) \]

\[ i_{v_c} = \frac{V_c}{\alpha^2 + \beta^2} \left( \frac{L_m \omega \alpha}{R_m} - \beta \right), \quad (A6) \]

\[ i_{m_r} = \frac{\alpha V_c}{\alpha^2 + \beta^2}, \quad (A7) \]

\[ i_{m_c} = -\frac{\beta V_c}{\alpha^2 + \beta^2}, \quad (A8) \]

\[ u_{v_c} = \frac{1}{C_i \omega_c} \frac{V_c}{\alpha^2 + \beta^2} \left( \frac{L_m \omega \alpha}{R_m} - \beta \right), \quad (A9) \]

\[ u_{v_r} = -\frac{1}{C_i \omega_c} \frac{V_c}{\alpha^2 + \beta^2} \left( \alpha + \frac{L_m \omega \beta}{R_m} \right), \quad (A10) \]

\[ u_{v_{cs}} = \frac{2 \pi R_i}{\pi} \frac{L_m \omega_a}{\alpha^2 + \beta^2} V_c \sqrt[4]{\alpha^2 + \beta^2}. \quad (A11) \]

In the above equations, \( V_c, \alpha \) and \( \beta \) are related to \( i_{pd}, u_0 \) and \( i_{m_r} \) with the following equations:

\[ i_{pd} = \frac{L_m \omega_a}{\alpha^2 + \beta^2} \sqrt[4]{\alpha^2 + \beta^2} \quad (A12) \]

\[ u_0 = \frac{L_m \omega_a}{\alpha^2 + \beta^2} \left( \frac{R_c r}{R_i + r \pi} + \frac{R_c}{R_i + r \pi} \right), \quad (A13) \]

\[ i_{m_r} = \frac{2}{\pi} \sin (\pi d) \left( \frac{V_c}{\alpha^2 + \beta^2} \left( \alpha + \frac{L_m \omega \beta}{R_m} \right) \right), \quad (A14) \]

A.4 PARAMETERS OF THE SMALL-SIGNAL MODEL EQUATIONS OF DC–DC–LLC RESONANT CONVERTER

\[ k_i = \frac{4 \mu C_2}{\pi} \quad (A15) \]

\[ e_{sr} = \frac{1}{i_{pd}} - \frac{(i_{rd} - i_{mr})^2}{i_{pd}^2} \quad (A16) \]

\[ e_{sr} = \frac{1}{i_{pd}} - \frac{(i_{rd} - i_{mr})^2}{i_{pd}^2} \quad (A17) \]

\[ e_{sr} = e_{sr} = (i_{rd} - i_{mr}) \frac{(i_{rd} - i_{mr})}{i_{pd}^3} \quad (A18) \]

\[ e_{C_{mr}} = 2n \frac{i_{pd}}{\pi} (i_{rd} - i_{mr}) \quad (A19) \]

\[ e_{C_{mr}} = 2n \frac{i_{pd}}{\pi} (i_{rd} - i_{mr}) \quad (A20) \]

\[ k_c = \frac{4}{\pi} \sin (\pi d) \quad (A21) \]

\[ k_3 = 4 n \cos (\pi d) \quad (A22) \]

\[ R_c = \frac{R_o r}{R_o + r} \quad (A23) \]