Single-Input Quadruple-Boosting Switched-Capacitor Nine-Level Inverter with Self-Balanced Capacitors

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This work was supported by Finnish Electronic Library (FinELib), Finland under the FinELib consortium’s agreement with IEEE.

ABSTRACT This paper suggests a single-input switched-capacitor Nine-level inverter configuration advantaging from quadruple voltage-boosting ability, natural voltage balancing of capacitors, and reduced components per level. Also, the single-source character of the proposed topology makes it cheaper and more compact. The cascaded version of the suggested topology has also been introduced, by which high boosting factors, as well as large number of steps, can be obtained. The proposed topology can effectively supply the resistive-inductive or pure inductive load types. The capacitors’ impulsive-charging-current issue has been solved by simple small-inductance-based inductor-diode (L-D) networks. The comparative analysis affirms the fewer device-usage in suggested configuration per equal gain or level count than existed structures, resulting in less size and cost. The usage of Nearest-Level modulation guarantees the low-frequency operation of semiconductors and reduces the switching losses. The comparative analysis and experimental outcomes affirm the competitiveness and accurate functionality of suggested configuration.

INDEX TERMS Multilevel inverter, Number of levels, Self-balanced capacitors, Switched-capacitor, Voltage gain

I. INTRODUCTION

The Multi-Level Inverters (MLIs) are well-known for high-quality output voltage and low voltage stress on switching devices [1]. The conventional MLIs are mainly categorized as: A) Cascaded H-Bridge (CHB), B) Diode-Clamped (DC), and C) Floating-Capacitor (FC) inverters. The CHB inverters produce many voltage steps but have no voltage boosting ability and usually require numerous DC supplies and power semiconductors [2-4]. Also, the DC and FC inverters demand more clamping-diodes, DC-link, or floating-capacitors to acquire increased-levels. The requirement of voltage sensors and complex strategies for balancing the charge of capacitors is another shortcoming of NPC and FC inverters [5, 6].

To increase the number of voltage steps in MLIs, more DC supplies, semiconductors, and driver circuits are required, which leads to a bulky, heavy, and costly converter. So, many studies have focused on presenting reduced-component structures like [7, 8]. In [9], the authors aimed to decrease the semiconductors (and gate-driver circuits). As aimed in [10, 11], reducing the number of DC supplies (as large and expensive parts) is more beneficial than other components. The utilization of Switched-Capacitor Cells (SCCs) in MLIs can provide a higher number of levels without the need to increase DC sources. This critical feature improves output voltage quality and simultaneously keeps the converter as compact/cheap as possible [12, 13]. From viewpoint of voltage boosting ability, the Switched-Capacitor Multi-Level Inverters (SCMLIs) are classified into boost (step-up), step-down or unity-gain categories. The [14, 15] present two step-down converters, where the peak voltage (\(V_{\text{rms}}\)) is lower than total inputs. The topologies presented in [16-19] are examples of unity-gain converters with equal peak output voltage and summation of input sources. Usually, the MLIs utilizing capacitors only in DC-link(s) produce unity gain. But, the step-up or boost SCMLIs like [11, 20-24] have voltage boosting ability and can produce larger voltage than total inputs. The voltage boosting ability becomes very vital for grid-tied SCMLIs fed by Photovoltaics (PVs) or Fuel Cells (FCs), where the input...
voltage(s) is (are) much less than the grid voltage [25, 26]. The semiconductors' blocking-voltage is relatively high in step-up SCMLIs that may impact the price and efficiency of converter [27]. For the applications where significant step-up capability is not required, mild or low-gain structures with low voltage stress are preferred [28].

The SCMLIs usually realize the bipolar waveform through the conventional or developed H-bridge, two half-bridges, or inherently. The topologies presented in [29-31] apply an H-bridge unit, whose switches must tolerate \( V_{o,\text{max}} \). The [32] employs a developed H-bridge for negative voltage level generation, where two switches tolerate the maximum output voltage. The generation of a bipolar waveform in [33] is achieved inherently, but four switches suffer from voltage stress of \( V_{o,\text{max}} \). The [34, 35] use two half-bridges for a negative voltage-level generation. Accordingly, 2 and 0 switches tolerate \( V_{o,\text{max}} \) respectively in [34, 35]. Similar to [29-31] and due to application of the H-bridge in [36], four switches withstand the \( V_{o,\text{max}} \). The structures with a larger number of switches tolerating \( V_{o,\text{max}} \) suffer from large Total Voltage Stress (TVS) on semiconductors. The [30, 31, 33-36] outputs nine voltage levels through a single DC source, while the [32] requires two input sources. The application of more sources negatively impacts the converter's overall size, cost and weight. The [37] presents a double-input two H-bridge-based switched-capacitor 27-level topology that gives a gain of 1.3. The TVS of semiconductors in [37] is relatively low, and none of them tolerate the \( V_{o,\text{max}} \).

This article suggests a single-source 9-level switched-capacitor inverter that is capable of providing quadruple voltage-gain. The large boosting capability, capacitors' natural charge balancing as well as fundamental frequency operation of H-bridge switches are distinguished features of suggested inverter. In the following, the suggested basic and cascaded topologies are introduced and explained in Sections II and III. The design consideration of capacitors, suppression of capacitors’ charging current, and modulation strategy are presented in Sections IV-VI. Section VII provides the comparative analysis. The loss analysis is done in Section VIII. Finally, implemented set-up results and conclusion are given in Sections IX and X, respectively.

**II. PROPOSED 9-LEVEL INVERTER**

The proposed switched-capacitor-based inverter (shown in Fig. 1) is composed of level generation and polarity generation units. The level generation unit is formed of a single DC source, single-diode, two capacitors, and seven switches (MOSFETs), as (1). The \( S_1 - S_2 \) are bidirectional common-source switches. The others are unidirectional switches. The end-side H-bridge plays the role of the polarity generation unit.

\[
N_{\text{Source}} = 1, \quad N_{\text{Switch}} = N_{\text{Driver}} = 11, \quad N_{\text{MOSFET}} = 13, \\
N_{\text{Capacitor}} = 2, \quad N_{\text{Diode}} = 1, \quad N_{\text{Component}} = 26
\]  

Table I shows different switching states of switches, forward/reverse bias of \( D_1 \) diode, and charge/discharge mode of \( C_1-C_2 \) capacitors. The green up and red down symbols represent the charging and discharging modes, respectively. Fig. 2 displays various operational modes of the suggested circuit. As seen, the positive and negative voltage steps are generated respectively by turning on the \( (H_1, H_3) \) and \( (H_2, H_3) \) switch pairs. Also, there is only one redundant state, which leads to zero voltage level.

![FIGURE 1. Proposed 9-level inverter.](image-url)
$V_{C1} = V_{dc}, \quad V_{C2} = 2V_{dc}, \quad V_{o,max} = 4V_{dc},$

\[ G = \left( \frac{V_{o,max}}{V_{dc}} \right) = 4 \]  

**TABLE II**  
VOLTAGE STRESS ON SEMICONDUCTORS

| Semiconductor | Voltage Stress | Voltage Stress |
|---------------|----------------|---------------|
| $S_1$         | $3V_{dc}$      | $S_2$         | $3V_{dc}$      |
| $S_1$         | $2V_{dc}$      | $H_1$         | $4V_{dc}$      |
| $S_2$         | $V_{dc}$       | $H_1$         | $4V_{dc}$      |
| $S_1$         | $2V_{dc}$      | $H_2$         | $4V_{dc}$      |
| $S_2$         | $2V_{dc}$      | $D_1$         | $V_{dc}$       |

The Voltage Stress (VS) on the semiconductors has been shown in Table II. The H-bridge switches tolerate the $V_{o,max}$, but operate at low-frequencies, leading to limited switching losses.

**FIGURE 2.** Operational-modes of suggested 9-level inverter.

**States 1-2 (Figs. 2(a) and 2(b)):** During zero voltage level generation ($V_o = 0$), the input-source charges the $C_1$ ($V_{C1} = V_{dc}$) through $D_1$ and $S_1$.

**States 3-4 (Figs. 2(c) and 2(d)):** The $V_o = \pm V_{dc}$ voltage levels are produced by the input DC source. Simultaneously, the $C_1$ capacitor keeps on being charged by the input DC source.

**States 5-6 (Figs. 2(e) and 2(f)):** The $V_o = \pm 2V_{dc}$ voltage steps are generated by a series connection of input source and $C_1$ capacitor. At the same time, the $C_2$ capacitor is paralleled with the cascaded input source and $C_1$ capacitor. So, the $C_2$ capacitor is charged to $v_{C2} = V_{dc} + v_{C1} = 2V_{dc}$.

**States 7-8 (Figs. 2(g) and 2(h)):** In order to synthesize the $V_o = \pm 3V_{dc}$ on the load, the input source is cascaded with $C_2$ capacitor. Meanwhile, the parallel connection of the input source and $C_1$ capacitor keeps its voltage on $v_{C1} = V_{dc}$.

**States 9-10 (Figs. 2(i) and 2(j)):** Finally, the $V_o = \pm 4V_{dc}$ voltage steps are provided by cascading the input DC source, $C_1$ and $C_2$ capacitors.

Table I and Fig. 2 show that the suggested converter can produce 9 voltage steps (including $0, \pm V_{dc}, \pm 2V_{dc}, \pm 3V_{dc}$ and $\pm 4V_{dc}$) with a maximum output voltage of $V_{o,max} = 4V_{dc}$. So, the voltage gain ($G$) of the suggested topology is equal to 4. Also, as shown in (2), the $C_1$ and $C_2$ capacitors are charged to $V_{dc}$ and $2V_{dc}$, respectively.

**FIGURE 3.** Suggested extended configurations: (a) First version ($T_1$), (b) Second version ($T_2$).

**III. PROPOSED CASCADED STRUCTURES**

According to Fig. 3, the suggested basic 9-level inverter can be extended in two forms to achieve an increased number of levels: First extended topology ($T_1$), which employs multiple H-bridges (Fig. 3(a)), and Second extended topology ($T_2$) that applies single H-bridge (Fig. 3(b)). These structures are explained in the following.

**A. 1ST EXTENDED TOPOLOGY ($T_1$)**

As evident from Fig. 3(a), the number of required devices in proposed first extended topology are as (3):
\[ N_{\text{Source}} = n, N_{\text{Switch}} = N_{\text{Driver}} = 11n, N_{\text{MOSFET}} = 13n, \]
\[ N_{\text{Capacitor}} = 2n, N_{\text{Diode}} = n, N_{\text{Component}} = 26n \tag{3} \]

For level-count maximization, the DC-sources’ voltage is decided as (4). The DC-sources’ variety is \( n \).
\[ V_i = V_{dc}, V_i = 9^{-i}V_{dc} \tag{4} \]

Where, the \( V_{o,\text{max}} \) denotes the maximum output voltage of \( j^{th} \) cascaded unit. Also, the \( V_i \) represents the input source of \( j^{th} \) cascaded unit \((j=1, 2, \ldots, n)\).

The maximum output voltage of each unit, as well as the whole cascaded structure, are computed as (5).
\[ V_{o,\text{max}} = 4V_i = 4(9)^{-1}V_{dc}. \tag{5} \]

The voltage-levels and gain are as (6)-(7), respectively.
\[ N_{\text{Level}} = 9^i \tag{6} \]
\[ G = \left(V_{o,\text{max}} / \sum_{i=1}^{n} V_i \right) = 4 \tag{7} \]

The TVS for first extended topology is calculated from (8).
\[ TVS = \sum V_{S,H,D} = \frac{30}{8}(9^i - 1)V_{dc} \tag{8} \]

The Average Voltage Stress (AVS) on switches/diodes of first extended topology is as (9).
\[ AVS = \frac{TVS}{N_{\text{Switch}} + N_{\text{Diode}}} = \frac{30}{96n}(9^i - 1)V_{dc} \tag{9} \]

**B. 2\textsuperscript{ND} EXTENDED TOPOLOGY (T2)**

The 2\textsuperscript{nd} extended structure is shown in Fig. 3(b). The number of different components has been presented in (10).
\[ N_{\text{Source}} = n, N_{\text{Switch}} = N_{\text{Driver}} = 7n + 4, N_{\text{Diode}} = n, \]
\[ N_{\text{Capacitor}} = 2n, N_{\text{MOSFET}} = 9n + 4, N_{\text{Component}} = 18n + 8 \tag{10} \]

For level-count maximization in 2\textsuperscript{nd} extended structure, the size of DC-sources is decided as (11).
\[ V_i = V_{dc}, V_i = 8^{-i}V_{dc} \tag{11} \]

The peak output voltage of each unit and the total output voltage are shown in (12).
\[ V_{o,\text{max}} = 4V_i = 4(8)^{-1}V_{dc} \tag{12} \]
\[ V_{o,\text{max}} = \sum_{i=1}^{n} V_{o,\text{max}} = (8^i - 1)V_{dc} \]

According to (12), the level-count and gain of 2\textsuperscript{nd} extended structure is computed respectively from (13) and (14).
\[ N_{\text{Level}} = 2(8)^i - 1 \tag{13} \]
\[ G = \left(V_{o,\text{max}} / \sum_{i=1}^{n} V_i \right) = 4 \tag{14} \]

The TVS and AVS of the second extended topology are obtained respectively from (15) and (16).
\[ TVS = \frac{30}{4}(8^i - 1)V_{dc} \tag{15} \]
\[ AVS = \frac{30}{4(8n + 4)}(8^i - 1)V_{dc} \tag{16} \]

**IV. DESIGN OF CAPACITORS**

The proper determination of capacitances leads to low voltage ripple and power loss in capacitors. The capacitors are designed such that their voltage ripple during Longest Discharge Interval (LDI) be limited to the desired value (\( \Delta V_C \)). According to Fig. 4, the LDI of C1 capacitor occurs during the generation of \( \pm 4V_{dc} \). Also, the LDI of C2 capacitor happens at \( \pm 5V_{dc} \) and \( \pm 4V_{dc} \). The beginning and ending of LDI of C1 capacitor are \( \theta_h \) and \( \pi - \theta_h \), respectively. Also, the LDI of C2 capacitor starts at \( \theta_h \) and finishes at \( \pi - \theta_h \). So, the duration of LDI of C1 - C2 capacitors are \( \theta_{c1} = \pi - 2\theta_h \) and \( \theta_{c2} = \pi - 2\theta_h \), respectively.

![FIGURE 4. Charge/Discharge intervals of C1-C2 capacitors.](image)

From (17), the capacitances are determined to limit their voltage-ripple to \( \Delta V_C \). Note that \( I_{o,\text{max}} \): maximum load current, \( \theta_c \): duration of LDI of C capacitor, \( \cos \varphi \): load power-factor, \( f \): fundamental-frequency, \( \Delta V_C \): capacitor’s voltage-ripple.
\[ C \geq \frac{I_{o,\text{max}} \cos \varphi \sin(\theta_c / 2)}{\pi f \Delta V_C} \tag{17} \]

**V. SUPPRESSION OF CAPACITORS’ CHARGING CURRENT**

The capacitors’ impulse charging current is one of the main challenges associated with switched-capacitor-based multi-level inverters, which subject the semiconductors to large current stress and increase the losses. In this study, the \( C \)'s charging-current is restricted by inductor-diode \( (L_i - D_i) \) cells, as Fig. 5. The presented equivalent circuits show that the
limiting inductors \((L)\)s are placed on the charging path of capacitors, leading to lower charging currents. But, at discharging modes, these charge-limiting inductors are bypassed by the reverse diodes \((D)\)s.

\[ \text{FIGURE 5. Proposed inverter and its operational modes in presence of inrush-current limiting cells.} \]

VI. NEAREST LEVEL MODULATION (NLM)

In recent years many different modulation techniques have been presented for MLIs. This paper employs the "Fundamental Frequency" or "Nearest Level" modulation technique, which profits from generality, simplicity, ease of implementation, fast operation speed and low-frequency operation of semiconductors, and reduced switching losses [9]. A sinusoidal reference \((V_{\text{ref}} = A \sin(\omega t))\) waveform with an amplitude of \(A\) and frequency of \(f = \omega / 2\pi = 50[\text{Hz}]\) is compared with producible levels \((0, \pm V_{dc}, \pm 2V_{dc}, \ldots, \pm NV_{dc})\), where \(0 < A \leq N_{P}\) and the \(N_{P}\) denotes the maximum positive level. The control block diagram of “Nearest Level” modulation techniques as well as resulted switching pulses have been shown in Fig. 6. It is seen that the H-bridge switches \((H_1 - H_4)\) operate at fundamental frequency. The other remaining semiconductors also operate at low frequencies.
VII. COMPARISONS

This part compares the suggested topologies with existing SCMLIs from viewpoints of level and device count, voltage-stress on semiconductors, voltage-boosting capability and efficiency. In Table III, the suggested basic 9-level inverter is compared with similar 9-level inverters.

As seen, the proposed basic topology requires fewer total switches and diodes than other counterparts for producing 9 levels. Among selected topologies, the [32] utilizes two DC-sources, while the others and suggested basic configuration use on a single DC source. Table III confirms that the proposed basic topology employs only two capacitors (the same as [32, 35]), while the others use 3 capacitors. According to Table III, the proposed basic topology and [31, 32, 34] use minimum total devices, where the [22] utilize maximum devices. As seen from Table III, the TVS on semiconductors of suggested basic inverter is higher than other counterparts, which is considered as its main drawback. Among selected topologies, the [22] has the least maximum voltage stress (=0.25\(V_{\text{o,max}}\)) on its semiconductors than other structures. The maximum voltage gain (quadruple gain) belongs to proposed basic inverter and [22, 30, 31, 34, 35], where the [32] has the least gain (double gain).

### Table III

| Topology | \(N_{\text{level}}\) | \(N_{SW}+N_D\) | \(N_{DC}\) | \(N_C\) | \(N_{TC}\) | \(TVS\) | \(TVS_{\text{pu}}\) | \(MVS\) | \(V_{\text{o,max}}\) | Gain | NMB | Efficiency | Negative level generation |
|----------|----------------|----------------|-------------|---------|--------|---------|---------------|-------|----------------|-------|-----|-------------|------------------------|
| [22]     | 9              | 22             | 1           | 3       | 45     | 19\(V_{dc}\) | 4.75          | 0.25\(V_{o,max}\) | 4\(V_{dc}\) | 4    | 0           | 88.9% @74W             | Inherent              |
| [30]     | 9              | 13             | 1           | 3       | 27     | 25\(V_{dc}\) | 6.25          | \(V_{o,max}\) | 4\(V_{dc}\) | 4    | 4           | 91.5% @138W            | H-Bridge              |
| [31]     | 9              | 14             | 1           | 3       | 26     | 26\(V_{dc}\) | 6.5           | \(V_{o,max}\) | 4\(V_{dc}\) | 4    | 4           | 91.6% @60W             | H-Bridge              |
| [32]     | 9              | 12             | 2           | 2       | 26     | 22\(V_{dc}\) | 5.5           | \(V_{o,max}\) | 4\(V_{dc}\) | 2    | 2           | 90-94.5% @50-500W      | Developed H-Bridge    |
| [34]     | 9              | 11             | 1           | 3       | 26     | 24\(V_{dc}\) | 6             | \(V_{o,max}\) | 4\(V_{dc}\) | 4    | 2           | 96-97.7% @5-50W        | 2 Half-Bridges        |
| [35]     | 9              | 12             | 1           | 2       | 27     | 21\(V_{dc}\) | 5.25          | 0.5\(V_{o,max}\) | 4\(V_{dc}\) | 4    | 0           | 97.9% @160W            | 2 Half-Bridges        |

Proposed: Number of levels, \(N_{SW}\): Number of switches, \(N_{D}\): Number of diodes, \(N_{DC}\): Number of sources, \(N_C\): Number of capacitors, \(N_{TC}\): Number of total components, \(TVS\): Total voltage stress, \(N_{Var}\): Number of DC sources variety, \(V_{o,max}\): Maximum output voltage, \(G\): voltage gain, \(NMB\): Number of switches tolerating \(V_{o,max}\)

### Table IV

| Type | Topology | \(N_{\text{level}}\) | \(N_{sw}\) | \(N_{DC}\) | \(N_C\) | \(N_{TC}\) | \(TVS/V_{dc}\) | \(N_D\) | \(N_{DC}\) | \(V_{o,max}\) | \(N_{TC}\) | \(N_{Var}\) | \(G\) | NMB |
|------|----------|----------------|-----------|-----------|---------|--------|---------------|-------|--------|-------|--------|---------|-----|-----|
| Asymmetric | [38] | (2n+3)^2 | 4n+8 | 4n+8 | 2n | 20n/4+4n+16 | 2n | 2 | 2n+4n+4 | 12n+18 | 2 | n+1 | 2 |
| | [39] | 2(3n+3)^2+1 | 10n+8 | 10n+8 | 4n | (3n+2) | (12n^2+1) | 2n | 2 | 3(3n+2) | 20n+18 | 2 | 0 |
| | [36] | 2n+1 | 3n+3 | 3n+3 | n | 7(2n-3) | 1 | 1 | 2n | 7n+8 | 2 | n | 4 |
| | [30] | 5n | 6n+6 | 6n | n | 5(5n-1)/2 | n | n | (5n-1)/2 | 15n | n | 2 | 0 |
| Proposed \(T_1\) | 9n | 11n+1 | 11n | 2n | 30n(9n-1)/8 | n | n | (9n-1)/2 | 26n+4 | n | 4 | 0 |
| Proposed \(T_2\) | 2(5n-1) | 7n+4 | 7n+4 | 2n | 30n(5n-1)/4 | n | n | 5n-1 | 18n+8 | n | 4 | 4 |
| Symmetric | [33] | 8n+1 | 6n+2 | 6n+2 | 2n | 16n+8 | n | n | 4n | 16n+4 | 1 | 2 | 2 |
| | [10] ISC | 4n+1 | 2n+8 | 2n+8 | 1 | 12n-2 | n | - | n | 2n | 5n+17 | 1 | 2 | 0 |
| | [10] 2SC | 6n+1 | 2n+14 | 2n+14 | 2 | 18n-2 | n | - | n | 3n | 5n+30 | 1 | 3 | 0 |
| | [40] | 6n+1 | 11n | 11n | 2n | 16n | 0 | n | 3n | 25n | 1 | 3 | 0 |
| | [28] | 8n+1 | 10n | 10n | 2n | 11n | 0 | n | 4n | 23n | 1 | 2 | 0 |
| | [41] | 4n+1 | 9n | 9n | 9n | 0 | n | 2n | 20n | 1 | 2 | 0 |
| Proposed \(P_1\) | 8n+1 | 11n+1 | 11n | 2n | 31n | n | n | 4n | 26n | 1 | 4 | 0 |

\(N_{\text{level}}\): Number of levels, \(N_{sw}\): Number of switches, \(N_{D}\): Number of diodes, \(N_{DC}\): Number of sources, \(N_C\): Number of capacitors, \(N_{TC}\): Number of total components, \(TVS\): Total voltage stress, \(N_{Var}\): Number of DC sources variety, \(V_{o,max}\): Maximum output voltage, \(G\): voltage gain, \(NMB\): Number of switches tolerating \(V_{o,max}\)
Based on Table III, none of semiconductors in [22, 35] tolerate $V_{o,max}$. In [32, 34] two semiconductors tolerate $V_{o,max}$, while this amount in proposed basic inverter and [30, 31] is four. Based on Table III, none of semiconductors in [22, 35] tolerate $V_{o,max}$. In [32, 34] two semiconductors tolerate $V_{o,max}$, while this amount in proposed basic inverter and [30, 31] is four.

Table III presents and compares the efficiency of proposed converter with that of [22, 30-35]. As seen, the efficiency of topologies presented in [22], [30] and [31] are 88.9%, 91.5%, and 91.6%, respectively at 74[W], 138[W], and 60[W]. The efficiency of proposed converter in this range of output power is about 90.9% to 93.5%, which is higher than the reported efficiency of [22, 30, 31]. The reported efficiency range of [32] across output power range of 50[W] to 500[W] is [90%-94.5%]. During almost the same output power range, the efficiency of proposed topology is about 90.6% to 95.5%, which is slightly higher than that of [32]. Meanwhile, the reported efficiencies of topologies presented in [34, 35] are higher than the efficiency of proposed converter.

The proposed basic inverter and [30, 31] use an H-bridge, while the [32] use a developed H-bridge and [34, 35] employ two half-bridges for negative voltage generation. This feature is realized inherently in [22].

The proposed cascaded inverter and generalized counterparts presented in [10, 28, 30, 33, 36, 38-41] are compared in Table IV. Fig. 7 present the comparison results as plots. The topologies presented in [38, 39] utilize 2 DC sources, but the proposed topology ($T_1$, $T_2$ and $P_1$) and [10, 28, 30, 33, 36, 40, 41] demand only a single DC source at basic version. This further decreases the overall weight, expense and volume of the converter (Fig. 7(a)). Fig. 7(b) - 7(c) show that the proposed $T_1$ and $T_2$ topologies and [30, 36] require equal or less switching devices (switches and diodes) than other counterparts, which accordingly leads to less gate-driver circuits, less complexity, low size and low losses. Based on Fig. 7(d), the proposed $T_1$ and $T_2$ topologies utilize the second least number of capacitors to produce equal levels with similar counterparts. Also, it is seen from Fig. 7(e) that the proposed $T_1$ and $T_2$ topologies provide the third-highest (after [30, 36]) ratio of levels to total devices ($N_{TC} = N_{DC} + N_{SW} + N_{GD} + N_{D} + N_{C}$). This can result in a compact and less-complicated structure. As seen from Fig. 7(f), the gain of converters presented in [36, 38] increases at extended versions, but the gain of converters presented in [10, 28, 30, 33, 39-41] remains constant. Among these constant-gain converters, the proposed $T_1$, $T_2$ and $P_1$ topologies have the maximum step-up capability. According to Fig. 7(g), the Average Normalized Standing Voltage (ANSV) of the proposed symmetric converter ($P_1$) is quite low, while this amount in proposed asymmetric ($T_1$ and $T_2$) converters is rather high. Fig. 7(h) shows that the ANSV of converters reduces by an increment of cascaded units. Also, at equal units, the ANSV of proposed $T_1$, $T_2$ and $P_1$ topologies is lower than that of [33, 36, 38, 39], which is desirable. The proposed topology and [30, 31] require an H-bridge to create a bipolar voltage-waveform. Thus, the H-Bridge's switches are exposed to $V_{o,max}$. The negative voltage-level generation in [32] is achieved through a developed-H-bridge, where two switches tolerate $V_{o,max}$. The [34, 35] employ two half-bridges and the [33] inherently produce the negative voltage levels. The number of semiconductors tolerating the maximum output voltage ($N_{MVS}$) in [33, 34] and [35] are 4, 2 and 0, respectively. The [35] has the least TVS, because none of its semiconductors tolerate the Maximum Voltage Stress (MVS) of $V_{o,max}$.
MOSFETs, which can be modelled with an on-state resistance \((R_{on,T} \text{ or } R_{on,H})\). The conduction loss of switches happens at on-state resistances. Also, the switching losses occur during switch on-off transitions. The switching losses depend on voltage stress \((V_{stress})\), average current \((I_{ave})\), turn on and off times \((t_{on}, t_{off})\) and switching frequency \((f_s)\) of a switch. The total switch losses (conduction and switching) can be computed from (18).

\[
P_{\text{Loss Switch}} = \frac{1}{6} f_s V_{stress} I_{ave} (t_{on} + t_{off}) + R_{on} I_{rms}^2
\]  

(18)

**B. DIODES**

The diodes are modelled with a series connection of forward voltage drop \((V_{FD})\) and on-state resistance \((R_{on,D})\). Thus, the diode losses can be calculated from (19).

\[
P_{\text{Loss Diode}} = R_{on} I_{rms}^2 + V_{FD} \times I_{ave}
\]  

(19)

**C. CAPACITOR**

The capacitor losses (including voltage ripple and equivalent series resistance (RESR) losses) is obtained from (20):

\[
P_{\text{Loss Capacitor}} = \frac{1}{2} f_s C (AV)^2 + (R_{ESR} \times I_{rms})
\]  

(20)

The total power losses, as well as the efficiency \((\eta)\) of suggested, can be achieved from (21) and (22), respectively.

\[
P_{\text{Loss Total}} = P_{\text{Loss Switch}} + P_{\text{Loss Diode}} + P_{\text{Loss Capacitor}}
\]  

(21)

\[
\eta = \left(\frac{P_o}{P_o + P_{\text{Loss Total}}} \right) \times 100
\]  

(22)

**IX. EXPERIMENTAL RESULTS**

Fig. 8 displays the laboratory-scale prototype implemented to verify theoretical analysis and correct performance of suggested basic inverter. Table V shows the experimental parameters.
(17), the capacitances should be selected in $C_1 \geq 1822$ [µF] and $C_2 \geq 1682$ [µF]. To satisfy the (17), the $C_1 - C_2$ have been assumed to be $C_1 = C_2 = 2200$ [µF]. Assuming the input voltage as $V_{dc} = 30$ [V], the voltage stress on $C_1$ and $C_2$ capacitors will be 30 [V] and 60 [V], respectively. The employed $C_1$ and $C_2$ capacitors have been selected to withstand up to 50 [V] and 100 [V], respectively, to meet the voltage stress requirement. Based on voltage and current stress of semiconductors, the IRFP260NpF, IRFS40 and MUR1560G have been respectively used for realizing $H_1 - H_4$, $S_1 - S_2$ and $D_1$.

| TABLE V EXPERIMENTAL PARAMETERS OF PROPOSED TOPOLOGY |
| Parameters | Magnitude |
|------------|-----------|
| Input DC voltage | 30 [V] |
| Load ($R, L$) | 90 [$\Omega$], 110 [mH] |
| Capacitor $C_1$ | 2200 [µF], 50 [V] |
| Capacitor $C_2$ | 2200 [µF], 100 [V] |
| Diode ($D_1$) | MUR1560G |
| Switches ($H_1-H_4$) | IRFP260NpF, 200 [V], 50 [A], $R_{diss} = 0.04$ [$\Omega$] |
| Switches ($S_1-S_2$) | IRFS40, 100 [V], 28 [A], $R_{diss} = 0.077$ [$\Omega$] |
| Fundamental frequency | 50 [Hz] |

Figs. 9(a) and 9(b) respectively depict the output voltage-current waveforms for (i) $R = 90$ [$\Omega$] and (ii) $R = 90$ [$\Omega$] and $L = 110$ [mH]).

![FIGURE 9. Experimental results for output voltage-current waveforms (a) $R=90(\Omega)$, (b) $R=90(\Omega)$ & $L=110$ [mH].](image)

As seen from Fig. 10, the even-order harmonics have been eliminated from the output voltage. Among available harmonic orders, the 21st, 17th, 25th and 23rd harmonic orders have the highest magnitudes, which are respectively about 3.1%, 2.97%, 2.88% and 2.7% of fundamental harmonic. These high order harmonics can be eliminated through a small filter. The Total Harmonic Distortion (THD) of the suggested 9-level inverter is about 8.53%. Fig. 11 displays the current and voltage waveform of $C_1 - C_2$ capacitors.

![FIGURE 10. Harmonic spectrum of the output voltage.](image)

As expected, the voltage across $C_1-C_2$ capacitors has been naturally balanced on 28 [V] and 58 [V], respectively. Also, appropriate design of capacitances has suppressed voltage-ripple on $C_1$ and $C_2$ to equal or less than 5% ($\Delta V_{C1} = 1.5$ [V], $\Delta V_{C2} = 2$ [V]). Note that the experimental results have been obtained in presence of $L-D$ inrush-current limiting cells with small inductances of 50[µH]. Figs. 11(a)-11(b) confirms that the charging current of both $C_1$ and $C_2$ capacitors have been suppressed to less than 10[A], which is
acceptable.

Fig. 12 indicates the dynamic operation of the suggested topology during sudden load change conditions. It is seen that during decrement of load to half (from 120 [Ω] to 60 [Ω]), the peak load-current is doubled without considerable change in output-voltage. While changing load from 60 [Ω] to 120 [Ω], the peak load-current reduces to half, but its voltage remains unaltered. This confirms the appropriate dynamic performance of the suggested topology during sudden load change conditions.

![Dynamic operation during sudden load changes.](image)

FIGURE 12.

Figs. 13(a)-13(g) show the voltage waveforms of semiconductors. As seen, the voltage-stress of switches and diodes are as: \( V_{S1} = V_{S7} = 86 \text{ [V]} \) (Figs. 7(a) and 7(d)), \( V_{S2} = V_{S3} = V_{S6} = 58 \text{ [V]} \) (Figs. 7(a) and 7(c)), \( V_{S3} = V_{S4} = 30 \text{ [V]} \) (Fig. 7(b)), \( V_{S1} = 28 \text{ [V]} \) (Fig. 7(g)), and \( V_{H1} = V_{H2} = V_{H3} = V_{H4} = 117 \text{ [V]} \) (Figs. 7(e) and 7(f)). Despite the high voltage stress on \( H_1 - H_4 \), their low operation-frequency (fundamental frequency) limits the switching-losses.

![Voltage waveforms on semiconductors.](image)

FIGURE 13.

Fig. 14(a) illustrates efficiency of suggested topology at various input-voltages. The peak-efficiency is about 95.5% that occurs at \( V_{dc} = 70 \text{ [V]} \).

![Measured efficiency Vs. input voltage, (b) Loss distribution for \( V_{dc} = 30 \text{ [V]} \).](image)

FIGURE 14.

According to Fig. 14(b), the efficiency of converter at the operating point \( (P_o = 60 \text{ [W]}, V_{dc} = 30 \text{ [V]} \) is about 90.9%, where the conduction-loss of switches/diode are about 4.5 [W] (6.77%) and 1.5 [W] (2.26%), respectively. The ripple-loss of capacitors is about 0.4 [W] (0.6%). The employment of Nearest-Level technique has decreased switching-loss of semiconductors to 0.00048%, which is negligible.

**X. CONCLUSION**

This paper has proposed a basic switched-capacitor 9-level inverter that is extendable to higher levels. The single-source nature, quadruple voltage-boosting ability, capacitors' natural charge-balancing, increased levels per device, and capability of feeding low power factor (resistive-inductive or inductive) load types are the main advantages of the suggested topology. The H-bridge switches tolerate \( V_{omax} \), but due to their fundamental-frequency operation, their switching-loss is
suppressed. The capacitors' impulse-charging current has been reduced by a small-inductance-based L-D network. The output voltage THD of the suggested topology is about 8.5%. The comparative analysis confirms that the suggested topology has higher ratios of a number of levels and gain to devices, which is an important advantage. The efficiency of an implemented laboratory-scale prototype of the suggested topology for $V_n = 30$ [V] is about 90.9%, which is acceptable. Two extended versions of the suggested basic topology have been introduced to achieve more levels and voltage-gains. The experimental outcomes validate the proper performance of the suggested switched-capacitor 9-level inverter.

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