Simulation and analysis of T-PUC9 inverter fed single phase induction motor application

I William Christopher*, Delsa Davis, P Infanto Robbin, S Jovita Dixit and A Asif Iqbal

Department of Electrical and Electronics Engineering, Loyola-ICAM College of Engineering and Technology (LICET), Loyola Campus, Chennai-600034, India.

*E-mail: williamchristopher.i@licet.ac.in

Abstract. This paper presents the simulation and analysis of a Nine-Level T-Type Packed U-Cell (T-PUC9) Inverter fed single phase Induction Motor. This inverter includes a T-type neutral point clamped (NPC) pole, two identical DC voltage sources and a one half-bridge module. It employs a Multiple pulse width modulation (PWM) scheme for generating the pulses for all the eight switches to synthesis the desired nine level voltages namely 2V_{dc}, 1.5V_{dc}, V_{dc}, 0.5V_{dc}, 0, -0.5V_{dc}, -V_{dc}, -1.5V_{dc} and -2V_{dc} which resembles a nearly sinusoidal wave owing to the rise in the number of steps. Due to its low-level harmonic distortion in the output it is used in industrial applications. The simulation model of the presented inverter has been developed for a single-phase induction motor application for a two identical DC voltage sources of 110V each using the MATLAB Simulink platform. The theoretical predictions and the performance of the Nine-Level T-Type Packed U-Cell (T-PUC9) Inverter fed single phase induction motor have been successfully validated with the help of simulation results.

Keywords: T-Type Packed U Cell (T-PUC), Nine level inverter, Induction Motor

1. Introduction
In the recent times the Multilevel Inverter (MLI) has become an indispensable technology in the area of high-power and medium-voltage energy control applications. The fundamental principle of different multilevel inverters has been introduced systematically and a brief summary of various topologies and their control strategies is discussed [1]. Due to the restrictions in the conventional topologies, the author [2] reviewed and analysed some of the recently proposed multilevel inverter topologies with reduced power switch count. Here [3], the high power voltage-source inverter and the most widely used multilevel-inverter topologies are discussed including the neutral-point clamped (NPC), cascaded H-bridge, and flying capacitor converters. The operating principle of the topology is presented and a review of the most relevant modulation methods used by the industry is also discussed. An overview of multilevel converters for medium voltage with minimum harmonic distortion and high efficiency at the low switching frequency [4] is presented. The recent developments made in control and modulation of converters have been introduced [5]. At present, these techniques are commercialised in a wide range of applications, like conveyors, turbines, rolling mills, traction etc. Also the recent industrial applications of multilevel inverters with the reduced switches which finds its application in numerous systems and drives are discussed [6].
The authors [7] proposed a new symmetric multilevel converter with reduced count of on-state switches which is regularly appropriate for medium-voltage applications and which offers reduced power losses. In the suggested topologies [8], for an exact number of voltage levels, the number of dc voltage sources is reduced to 50% and the number of switches is also reduced. In addition to that a novel enhanced pulse-width modulation (PWM) method is introduced to control the suggested topologies. The authors [9] uses a blended methodology involving both IGCT and IGBT switches functioning in synergism. It aims to explore a blended multilevel power translation system naturally appropriate for high performance and high power applications. The new MLI [10] is presented which consists of a series connection of the suggested unit and is capable to generate only +ve voltage levels at the output side. It also adds an H-bridge unit to the suggested inverter. A novel topology MLI [11] is presented which can be used in intermediate voltage level applications. It consists of series-connected sub-MLI blocks which is used as an asymmetrical inverter. A new power MLC topology [12] which is made up of packed U cells (PUC), which consists of a pair power semiconductor switches with a single capacitor is suggested [12]. It provides high-energy translation quality using a less number of capacitors and power switches and subsequently, has a very low fabrication rate. A new sensor-less switching technique built on logic gates for a 5L packed U-cell (PUC5) converter [13] is recommended. It contains only 2L-shifted triangular carriers and logic gates with a remarkable reduction in intricacy of the suggested modulation method. The PUC5 converter has been employed in both stand-alone and grid-connected functioning modes. A MP5 converter has a pair of similarly controlled detached dc links, which can function at no load circumstance which is worthwhile for active power filter application is suggested [14]. A Sensor-Less PUC5 Inverter [15] has been presented for functioning in stand-alone and grid-connected applications. This sensor-less voltage controller eases the intricacy of the governor system, which creates it attractive for industrial applications. One of the significant applications of Multilevel inverters is AC motor control applications. A single-phase altered H-bridge MLI for induction motor application is discussed [16-17] in detail. This paper presents the Nine-Level T-Type Packed U-Cell (T-PUC9) Inverter [18] for single phase induction motor (IM) application. The schematic of the Single Phase IM control using T-PUC9 Inverter is illustrated in figure.1.

![Figure 1. Schematic of the single phase IM control using T-PUC9 Inverter](image)

This paper is drafted as follows. In section 2, the T-PUC9 inverter power circuit arrangement and its features are described. Then, the operation T-PUC9 inverter power circuit with its various modes of operation are discussed in section 3 in detail. The fourth section concisely explains the operation of single phase induction motor. The functionality validation and the performance characteristics of the single phase IM control using T-PUC9 Inverter are discussed in section 5. Last section concludes with the future scope of the presented inverter.

2. T-PUC9 Inverter Power Circuit Configuration

The T-Type Packed U-Cell (T-PUC9) nine-level inverter [18] comprises of two identical DC sources, a T-type neutral point clamped (NPC) pole and a half-bridge module. The T-type NPC pole consists of four MOSFET switching devices namely switches S1, S2, S3 and S4. While the half bridge consists of
two MOSFET switches namely $S_7$ and $S_8$. Two switches $S_5$ and $S_6$ will decide the $+\text{ve}$ and $-\text{ve}$ voltage levels of output and operate under the fundamental frequency (50Hz). There are four pairs of switching combinations such as $S_1$ and $S_3$, $S_2$ and $S_4$, $S_5$ and $S_6$, $S_7$ and $S_8$ essentially function in complementary. Henceforth during the $+\text{ve}$ half cycle (PHC), one zero voltage level (0) and four $+\text{ve}$ voltage levels namely $0.5V_{dc}$, $V_{dc}$, $1.5V_{dc}$ and $2V_{dc}$ can be generated. Similarly, during $-\text{ve}$ half cycle (NHC), one zero voltage level (0) and four $-\text{ve}$ voltage levels namely $-0.5V_{dc}$, $-V_{dc}$, $-1.5V_{dc}$ and $-2V_{dc}$ can be generated. Thus, totally nine voltage levels are generated by the T-PUC9 inverter. The T-PUC9 inverter circuit configuration [18] is illustrated in figure 2.

![Circuit configuration of T-PUC9 Inverter](image)

**Figure 2.** Circuit configuration of T-PUC9 Inverter

The Table.1 provides the comparisons of the T-PUC9 Inverter with the other nine level inverter topologies, and it is observed that it requires lesser count of switches, capacitors and the DC sources. Also the below mentioned inverter topologies could be used for grid connected applications and they have the capability of bidirectional power flow.

**Table 1.** Comparison of other Nine-level topologies with T-PUC9 topology

| Component Specifications | Symmetric [7] | Extended [8] | Hybrid [9] | Semi Cascaded [11] | Packed U-Cell [12] | T-PUC9 [18] |
|--------------------------|---------------|--------------|------------|-------------------|------------------|-------------|
| No. of Switches          | 8             | 12           | 12         | 10                | 8                | 8           |
| No. of Capacitors        | –             | 4            | –          | –                 | –                | 2           |
| No. of DC-Sources        | 4             | 2            | 3          | 4                 | 3                | 2           |
3. T-PUC9 Inverter Power Circuit Operation

The T-PUC9 inverter [18] power circuit is capable of generating nine voltage levels \( +2V_{\text{dc}}, +1.5V_{\text{dc}}, +V_{\text{dc}}, +0.5V_{\text{dc}}, 0, -0.5V_{\text{dc}}, -V_{\text{dc}}, -1.5V_{\text{dc}}, -2V_{\text{dc}} \) from two identical DC sources and the theoretical nine level voltage waveform is illustrated in figure 3. The switching sequence needed for generating the nine levels of output voltage is given in the Table 2 followed by the modes of operation.

**Figure 3.** Theoretical nine level output voltage waveform

**Table 2.** Switching sequence needed for generating the nine levels of output voltage

| S.No | S₁ | S₂ | S₃ | S₄ | S₅ | S₆ | S₇ | S₈ | Voltage Level |
|------|----|----|----|----|----|----|----|----|---------------|
| 1    | 1  | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 2V_{\text{dc}} |
| 2    | 0  | 1  | 1  | 0  | 0  | 1  | 1  | 0  | 1.5V_{\text{dc}} |
| 3    | 0  | 0  | 1  | 1  | 0  | 1  | 1  | 0  | V_{\text{dc}} |
| 4    | 0  | 1  | 1  | 0  | 0  | 1  | 0  | 1  | 0.5V_{\text{dc}} |
| 5    | 0  | 0  | 1  | 1  | 0  | 1  | 0  | 1  | 0  |
| 6    | 0  | 1  | 1  | 0  | 1  | 0  | 1  | 0  | -0.5V_{\text{dc}} |
| 7    | 0  | 0  | 1  | 1  | 1  | 0  | 1  | 0  | -V_{\text{dc}} |
| 8    | 0  | 1  | 1  | 0  | 1  | 0  | 0  | 1  | -1.5V_{\text{dc}} |
| 9    | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 1  | -2V_{\text{dc}} |

3.1 Mode I Operation

The switches S₁, S₂, S₆ and S₇ needs to be in turned ON condition for generating the ‘2V_{\text{dc}}’ voltage level. Whereas the remaining switches S₃, S₄, S₅ and S₈ needs to be in turned OFF condition. The mode I operation and the current flow direction is shown in figure 4.

3.2 Mode II Operation

The switches S₁, S₂, S₆ and S₇ needs to be in turned ON condition for generating the ‘1.5V_{\text{dc}}’ voltage level. Whereas the remaining switches S₃, S₄, S₅ and S₈ needs to be in turned OFF condition. The mode II operation and the current flow direction is shown in figure 5.
3.3 Mode III Operation

The switches S₃, S₄, S₆ and S₇ needs to be in turned ON condition for generating the ‘V_{dc}’ voltage level. Whereas the remaining switches S₁, S₂, S₅ and S₈ needs to be in turned OFF condition. The mode III operation and the current flow direction is shown in figure 6.

![Figure 4. Mode I Operation](image)

![Figure 5. Mode II Operation](image)

![Figure 6. Mode III Operation](image)

![Figure 7. Mode IV Operation](image)

![Figure 8. Mode V Operation](image)

![Figure 9. Mode VI Operation](image)

![Figure 10. Mode VII Operation](image)

![Figure 11. Mode VIII Operation](image)

![Figure 12. Mode IX Operation](image)
3.4 Mode IV Operation
The switches S2, S3, S4 and S7 needs to be in turned ON condition for generating the ‘0.5Vdc’ voltage level. Whereas the remaining switches S1, S5, S6 and S8 needs to be in turned OFF condition. The mode IV operation and the current flow direction is shown in figure 7.

3.5 Mode V Operation
The switches S2, S3, S4 and S7 needs to be in turned ON condition for generating the ‘0’ voltage level. Whereas the remaining switches S1, S5, S6 and S8 needs to be in turned OFF condition. This condition disconnects both the DC sources from the switches and hence the output voltage attains a 0-level. The mode V operation is shown in figure 8.

3.6 Mode VI Operation
The switches S3, S4, S5 and S7 needs to be in turned ON condition for generating the ‘-0.5Vdc’ voltage level. Whereas the remaining switches S1, S2, S6 and S8 needs to be in turned OFF condition. The mode VI operation and the current flow direction is shown in figure 9.

3.7 Mode VII Operation
The switches S3, S4, S5 and S7 needs to be in turned ON condition for generating the ‘-Vdc’ voltage level. Whereas the remaining switches S1, S2, S6 and S8 needs to be in turned OFF condition. The mode VII operation and the current flow direction is shown in figure 10.

3.8 Mode VIII Operation
The switches S2, S3, S4 and S8 needs to be in turned ON condition for generating the ‘-1.5Vdc’ voltage level. Whereas the remaining switches S1, S5, S6 and S7 needs to be in turned OFF condition. The mode VIII operation and the current flow direction is shown in figure 11.

3.9 Mode IX Operation
The switches S3, S4, S5 and S6 needs to be in turned ON condition for generating the ‘-2Vdc’ voltage level. Whereas the remaining switches S1, S2, S7 and S8 needs to be in turned OFF condition. The mode IX operation and the current flow direction is shown in figure 12.

4. Single Phase Induction Motor
The single phase motors are simple in construction, low cost, reliable and less maintenance compare to three phase motors. Due to all these benefits, the single phase motor finds its application in small power ratings such as vacuum cleaners, fans, washing machines, centrifugal pumps and blowers etc. Single phase induction motors are one of the important classification single phase AC motors. Its construction is almost like to the squirrel cage type of three-phase induction motor, but the stator has two windings namely main winding and auxiliary winding for making it as self-starting motor. One important type of single-phase induction motors is capacitor start-run induction motor and it is shown in figure.13.

![Figure 13. Single Phase Capacitor Start –Run Induction Motor](image)

This capacitor start run induction motor has a squirrel cage rotor, and its stator has two windings known as main windings and auxiliary windings or starting winding. The two windings are displaced
by 90 degrees apart. There are two capacitors are used in this motor, one at the time of the starting and is known as the starting capacitor $C_S$. The other one is for continuous running of the motor and is known as a run capacitor $C_R$. Therefore, it is known as Capacitor Start Capacitor Run Motor. This motor is also known as Two-Value Capacitor Motor. It is appropriate for higher inertia loads where periodic starts are needed in applications like pumps, refrigerator and air conditioner compressors, etc.

5. Simulation Results and Discussions
MATLAB Simulink, established by MathWorks, which is a viable tool for modelling, simulating and analysing in control systems and digital signal processing for multi-field simulation design. This MATLAB software helps to work matrix functions, plotting of data, implementing algorithms etc. Therefore, the T-PUC9 inverter power circuit is designed and simulated using this software tool and the nine level output stepped waveform is obtained. Table 3 and Table 4 lists the simulation parameters with specifications for the T-PUC9 inverter and the single-phase induction motor respectively.

| S. No | Parameters | Specifications |
|-------|------------|----------------|
| 1.    | DC voltage sources, $V_{dc1}, V_{dc2}$ | 110V |
| 2.    | MOSFET $R_m$, $R_d$, $R_s$ | 0.1Ω, 0.01Ω, 100kΩ |
| 3.    | Fundamental frequency, $f$ | 50Hz |
| 4.    | Capacitors, $C_1$, $C_2$ | 220μF |

Table 3. Simulation Parameters for T-PUC9 Inverter

5.1 MATLAB Simulink Model of T-PUC9 Inverter
The simulation circuit of the T-PUC9 Inverter fed single phase induction motor using MATLAB Simulink is shown in figure.14. The simulation circuit of T-PUC9 Inverter fed single-phase Induction motor has been developed using the MATLAB Simulink power system block set, contains of components such as power electronic devices like MOSFETs and elements such as capacitors and resistors.
The PWM signals for all the eight switches (S₁ to S₈) of the T-PUC9 inverter circuit are obtained from the PWM generation block. This block includes all the switching pulses are multiplexed on a single bus and given to the T-PUC9 inverter power circuit. The two identical dc voltage sources (V_{dc1} and V_{dc2}) of 110V each with two capacitors (C₁ and C₂) are connected as input to the T-PUC9 inverter power circuit.

5.2 Simulation Results of T-PUC9 Inverter

The PWM pulses for all the eight MOSFET switches of the T- PUC9 inverter are shown in figure 15. The PWM pulses for the switches S₁, S₃, S₅, S₆ are generated using single PWM method and operates at fundamental frequency. Whereas the PWM pulses for the remaining switches S₂, S₄, S₇ and S₈ are generated using multiple PWM method and operates at high frequency.

Based on the PWM pulse generation for all the eight MOSFET switches for a two identical DC voltage sources (V_{dc1} and V_{dc2}) of 110V each, the T-PUC9 inverter circuit which generates a nine-level simulated output voltage as shown in figure 15 for one complete cycle. From the nine-level output voltage it is observed that, it is almost identical to the theoretical nine-level voltage waveform shown in figure 3.
The simulated output has the following nine voltage levels such as $+2V_{dc} = 220V$, $+1.5V_{dc} = 165V$, $V_{dc} = 110V$, $0.5V_{dc} = 55V$, $0V$, $-0.5V_{dc} = -55V$, $-V_{dc} = -110V$, $-1.5V_{dc} = -165V$ and $-2.5V_{dc} = -220V$ (for a scale of Horizontal: 10ms/division and Vertical: 50V/division) is shown in figure 16.

**FFT Analysis and THD**

The FFT analysis of the T-PUC9 inverter is illustrated in figure 17. The Total Harmonic Distortion (THD) for 50 cycles is obtained as 12.64% without using additional filters circuits. Table 5 shows the other parameters of the FFT analysis.

**Table 5. FFT Analysis**

| S. No | Parameters                              | Specifications |
|-------|----------------------------------------|----------------|
| 1     | Maximum Fundamental Voltage (50Hz)     | 216.7V         |
| 2     | RMS Fundamental Voltage (50Hz)         | 153.2V         |
| 3     | DC Component                           | 1.58V          |
| 4     | Total Harmonic Distortion (THD)        | 12.64%         |
| 5     | Sampling Time                          | 0.0002s        |
| 6     | Samples per cycle                      | 100            |
5.3 Simulation Results of T-PUC9 Inverter Fed Single Phase Induction Motor

The performance characteristics of the T-PUC9 Inverter Fed Single Phase Induction Motor are presented and deliberated in this section. The simulated nine-level voltage waveform for 50 cycles is shown in figure 18, which consists of nine voltage levels such as +220V, +165V, +110V, +55V, 0, -55V, -110V, -165V and -220V.

![Nine Level Output Voltage](image)

**Figure 18.** The nine level output voltage waveform (50 cycles)

The simulated waveform of the main winding current for T-PUC9 inverter fed induction motor is shown in figure 19. It is observed that initially the main winding current oscillates between 20A and 30A during the transient state period of 0.3ms and it reaches a steady-state value of 5A after a period 0.3ms.

![Main Winding Current](image)

**Figure 19.** Main winding current

![Auxiliary Winding Current](image)

**Figure 20.** Auxiliary Winding current

The simulated waveform of the auxiliary winding current for T-PUC9 inverter fed induction motor is shown in figure 20. It is observed that initially the auxiliary winding current oscillates between 10A and 15A for during a transient state period of 0.2ms and it reaches a steady-state value of 2.5A after a period 0.2ms.

![Stator Flux](image)

**Figure 21.** Stator flux

![Capacitor Voltage](image)

**Figure 22.** Capacitor voltage

The simulated waveform of the stator flux for T-PUC9 inverter fed induction motor is shown in figure 21. It is observed that the stator flux reaches a steady-state value of almost 0.7wb after a period of 0.3ms. The simulated waveform of the capacitor voltage for T-PUC9 inverter fed induction motor is
The capacitor voltage reaches a steady state value between 310V and 330V during a steady state period of 0.35ms.

The simulated waveform of the electromagnetic torque reaction for T-PUC9 inverter fed induction motor is illustrated in figure 23. This developed torque or induced torque in an induction motor is known as the torque generated by the electrical power to mechanical power energy conversion. Hence, this torque is also known as electromagnetic torque.

The simulated waveform of the rotor speed characteristics for T-PUC9 inverter fed induction motor is illustrated in figure 24. The transient state period of the rotor is 0.35ms. After the transient state period of 0.35ms the rotor reaches a steady state speed of 1500rpm, i.e. the rated speed of the single phase capacitor start-run induction motor.

6. Conclusion

The simulation model of T-PUC9 Inverter fed single phase induction motor using MATLAB Simulink has been successfully developed. This inverter which employs both single PWM and multiple PWM methods for generating the pulses for the switches to synthesize the desired nine level output voltage. The performance characteristics of single-phase capacitor start-run induction motor using T-PUC9 inverter has been analysed and discussed elaborately in this paper. The concurrence between the theoretical forecasts and the simulation results successfully demonstrates and controls the single-phase induction motor using T-PUC9 inverter power circuit efficiently. This inverter could also be realized and utilized for the real-time applications like Renewable Energy Systems (RES), Electrical Drives and Control (EDC) and grid connected systems using the digital controllers.

References

[1] José Rodríguez, Jih-Sheng Lai, Fang Zheng Peng, 2002, “Multilevel Inverters: A Survey of Topologies, Controls, and Applications”. IEEE Transactions on Industrial Electronics, Vol. 49, no. pp 724-738
[2] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S.Jain, 2016, “Multilevel Inverter Topologies With Reduced Device Count: A Review,” IEEE Transactions on Power Electronics, vol. 31, no. 1, pp. 135–151.
[3] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, 2007, “Multilevel Voltage-Source-Inverter Topologies for Industrial Medium-Voltage Drives,” IEEE Transactions on Industrial Electronics, vol. 54, no. 6, pp. 2930–2945.
[4] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, 2010, “Medium-Voltage Multilevel Inverters: State of The Art, Challenges, and Requirements in Industrial Applications,” IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2581–2596.
[5] S. Kouro et al., 2010, “Recent Advances and Industrial Applications of Multilevel Converters,” IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2553–2580.
[6] P. R. Bana, K. P. Panda, R. T. Naayagi, P. Siano, and G. Panda, 2019, “Recently Developed Reduced Switch Multilevel Inverter for Renewable Energy Integration and Drives...
Application: Topologies, comprehensive analysis and comparative evaluation,” *IEEE Access*, vol. 7, pp. 54888–54909.

[7] M. R. J. Oskuee, E. Salary, and S. Najafi-Ravadanegh, 2015, “Creative Design of Symmetric Multilevel Inverter to Enhance the Circuit’s Performance,” *IET Power Electronics*, vol. 8, no. 1, pp. 96–102.

[8] E. Babaei, M. F. Kangarlu, and M. Sabahi, 2014, “Extended Multilevel Converters: An Attempt to Reduce the Number of Independent DC Voltage Sources in Cascaded Multilevel Converters,” *IET Power Electronics*, vol. 7, no. 1, pp. 157–166.

[9] M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, 2000, “Hybrid Multilevel Power Conversion System: A Competitive Solution for High-Power Applications,” *IEEE Transactions on Industry Applications*, vol. 36, no. 3, pp. 834–841.

[10] E. Babaei, S. Laali, and Z. Bayat, 2015, “A Single-Phase Cascaded Multilevel Inverter Based On a New Basic Unit with Reduced Number of Power Switches,” *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 922–929.

[11] M. R. Banai, M. R. J. Oskuee, and H. Khounjahan, 2014, “Reconfiguration of Semi-Cascaded Multilevel Inverter to Improve Systems Performance Parameters,” *IET Power Electronics*, vol. 7, no. 5, pp. 1106–1112.

[12] Y. Ounejjar, K. Al-Haddad, and L. A. Grégoire, 2011, “Packed U Cells Multilevel Inverter Topology: Theoretical Study and Experimental Validation,” *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1294–1306.

[13] M. Abarzadeh, H. Vahedi, and K. Al-Haddad, 2019, “Fast Sensor-Less Voltage Balancing and Capacitor Size Reduction in PUC5 Converter Using Novel Modulation Method,” *IEEE Transactions on Industrial Informatics*, to be published, DOI: 10.1109/TII.2019.2893739.

[14] H. Vahedi, A.A. Shojaei, L. Dessaint and K. Al-Haddad, 2018, “Reduced DC Link Voltage Active Power Filter Using Modified PUC5 Inverter,” *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 943–947.

[15] H. Vahedi, P. Labbé, and K. Al-Haddad, 2016, “Sensor-Less five-Level Packed U-Cell (PUC5) Inverter Operating in Stand-Alone and Grid-Connected Modes,” *IEEE Transactions on Industrial Informatics*, vol. 12, no. 1, pp. 361–370.

[16] J. William Christopher and R. Ramesh, 2014, ’1-Phase Induction Motor Control Using Modified H-Bridge 11-level Inverter’, *Applied Mechanics and Materials*, vol. 622, pp. 211-217.

[17] J. William Christopher, R. Ramesh, A. Deepa, K. Hemalatha, S. Madhubala and J. Hemalatha, 2012, “Microcontroller based single-phase Simplified Nine-Level Inverter Fed Induction Motor,” in Proceedings IEEE 5th India International Conference on Power Electronics IICPE 2012, pp.1-6.

[18] Decunniiu, Feng Gao, Panrui Wang, Futain Qin, Zhan Ma, 2020, “A Nine-Level T-Type Packed U-Cell Inverter,” *IEEE Transactions on Power Electronics*, vol.35, no 2, pp.1171-1175.