Effect of Hysteresis-based Simple Negative Feedback A/D Conversion on Channel Estimation for Single Carrier Modulation

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Abstract: In wireless communication systems, simplification of the receiver circuits is an important issue. In particular, an analog-to-digital converter (ADC) is one of the most important circuit blocks. To deal with this issue, a low-resolution ADC utilizing hysteresis-based simple negative feedback (SNF) technique (hysteresis-based SNF-ADC) was proposed to mitigate nonlinear distortion. In this article, we investigate a recursive channel estimation technique for single carrier modulation with one-bit resolution hysteresis-based SNF-ADC. Simulation results clarify that the channel estimation accuracy is improved by using hysteresis-based SNF-ADC and bit error rate (BER) performance is improved compared to cases with only a comparator.

Keywords: A/D converter (ADC), Channel estimation, Hysteresis, Single carrier modulation

Classification: Wireless Communication Technologies

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1 Introduction

In wireless mobile communication devices, circuit design techniques for low-power dissipation have attracted much attention. From a viewpoint of power-efficiency at transmit power amplifier (PA), it is promising to use single carrier modulation schemes with a low peak to average power ratio characteristic [1]. Therefore, non-linear power-efficient PAs for single carrier modulation have been studied (e.g. [2]). On the other hand, in order to suppress power dissipation, other approaches to reducing the required resolution of analog-to-digital (A/D) converters (ADCs) are also important. In general, using low-resolution ADC (i.e., a fewer number of quantization bits per sample) can realize low power consumption at the ADC circuit. However, a low-resolution ADC affects bit error rate (BER) performance due to heavy non-linearity [3][4]. To cope with the non-linearity problem in ADC, linearity enhancement techniques are investigated for wireless communication systems [5][6]. One of the effective approaches to suppress the non-linearity in ADC, taking advantage of simple negative feedback (SNF) utilizing hysteresis effect for a one-bit resolution A/D conversion technique (i.e., hysteresis-based SNF-ADC) has been proposed [5]. It is also reported that using the hysteresis-based SNF-ADC is effective in improving the BER performance of single carrier modulation with a low-resolution ADC [6]. However, in [6], ideal channel estimation (CE) was assumed and thus the impact of the hysteresis-based SNF-ADC on channel estimation has not been clarified yet.

In this article, we investigate an extended recursive channel estimation technique with one-bit resolution hysteresis-based SNF-ADC to discuss the impact of using the simple negative feedback technique utilizing hysteresis effect on channel estimation in single carrier modulation with a nonlinear equalization.

2 System Model

Figure 1 (a) shows the block diagrams of single carrier modulation systems considered in this paper, where the hysteresis-based SNF-ADC is used on the receiver side. We consider an offset quadrature phase-shift keying (OQPSK), where the transmit signal is band-limited by a low-pass filter (LPF) whose...
frequency transfer function is the square root of raised cosine LPF. On the receiver side, the received signal is affected by multipath Rayleigh fading and additive white Gaussian noise (AWGN). Then, at the receiver, a band-pass filter (BPF) is used to eliminate out-of-band noise. An intermediate frequency (IF) sampling ADC digitizes the signal, where the digitized signal is frequency down-converted to the base-band signal in the digital domain. In this study, we apply a hysteresis-based SNF-ADC as a linearity enhancement technique. The detail of the hysteresis-based SNF-ADC is explained in the next section. In this study, channel estimation is carried out by receiving a known training sequence. After that, a nonlinear equalization based on a maximum likelihood sequence estimation (MLSE) is adopted to detect the data.

Figure 1 (b) shows the block diagram of the MLSE equalizer. In this equalizer, square errors are calculated for all possible candidate sequences that replicate the received signals corresponding to all possible data sequences, where channel estimates and the equivalent hysteresis-based SNF-ADC are used.
ADC function are used to generate the replicated signal candidates [4]. We assume the number of candidate sequences is $2^M$, where $M$ denotes the memory length in the MLSE. The data sequence that results in the minimum mean square error (MSE) is selected as the most reliable candidate, i.e., as the demodulated data sequence. The channel parameters for MSLE are estimated by a recursive channel estimator.

3 Channel estimation with the hysteresis-based SNF-ADC

In this section, we investigate an extended recursive channel estimation technique for single carrier modulation with one-bit resolution hysteresis-based SNF-ADC, where a channel estimation technique for one-bit resolution ADC [4]
is extended to take the SNF based on hysteresis effect.

One of the effective ideas for improving hard nonlinearities of a low-resolution ADC is a hysteresis-based SNF configuration [5]. Comparator hysteresis is a phenomenon that current ADC output is partially fed back to the input side, and it causes the DC offset of the input signal at the next sampling time. In the hysteresis-based SNF-ADC, the hysteresis effect is explicitly utilized to realize negative feedback and mitigate the influence of the nonlinearity caused by a low-resolution ADC.

Figure 2 (a) shows a block diagram of the hysteresis-based SNF-ADC that consists of a hysteresis comparator, an analog sample-and-hold (S/H) circuits as a analog chopper, and MUX as a digital chopper, where \( \beta \) denotes feedback factor.

Figure 2 (b) is a mathematical equivalent model of Fig. 2 (a). The key idea for linearity enhancement in the hysteresis-based SNF-ADC is to invert the hysteresis sign of the comparator by taking advantage of analog/digital chopper [5].

The input-output characteristics of the hysteresis-based SNF-ADC is given as

\[
\hat{y}[n] = \text{sgn}(y[n] - \beta \hat{y}[n - 1]),
\]

where \( \beta \) is the gain of the feedback signal. In the MLSE in Fig. 1, Eq.(1) is implemented as a function to generate the candidate signals. Here, \( n \) denotes the sample index.

Figure 2 (c) shows the block diagrams of the channel estimator, where the least mean square (LMS) algorithm is carried out to estimate channel parameters. The received training signal is given as

\[
y(n\Delta T) = \sum_{m=0}^{\infty} h(m\Delta T)x((n-m)\Delta T),
\]

where \( h(m\Delta T) \) and \( x(m\Delta T) \) denote the impulsive response of the channel and transmit training signal, respectively. \( \Delta T \) is time difference between two consecutive paths of the impulse response. Let \( e^{(i)} \) denotes the error vector between actually received training signal and estimated training signal at iteration step \( i \) given as

\[
e^{(i)} = y - \hat{y}^{(i)},
\]

where \( y = [y(\Delta T), y(2\Delta T), ... , y(N\Delta T)] \) and \( \hat{y}^{(i)} = [\hat{y}^{(i)}(\Delta T), \hat{y}^{(i)}(2\Delta T), ... , \hat{y}^{(i)}(N\Delta T)] \) are the actual received training signal and estimated received training signal at iteration step \( i \) given as

\[
\hat{y}^{(i)}(n\Delta T) = \sum_{m=0}^{\infty} \hat{h}^{(i)}(m\Delta T)x((n-m)\Delta T),
\]

where \( N \) is the number of paths of the channel. Let \( \hat{h}^{(i)} = [\hat{h}^{(i)}(\Delta T), \hat{h}^{(i)}(2\Delta T), ... , \hat{h}^{(i)}(N\Delta T)] \) denotes the estimated channel in the time domain at iteration step \( i \). The estimated channel is updated as follows.

\[
\hat{h}^{(i+1)} = \hat{h}^{(i)} + \mu x^{H} e^{(i)},
\]
where superscript $H$ is the Hermitian transpose. $\mu$ is a step size. $x = [x(\Delta T), x(2\Delta T), ..., x(N\Delta T)]$ is a known transmit training signal. In this study, we assume that $\Delta T$ and $N$ are known at the channel estimator for simplicity of discussion.

4 Performance evaluation

The performance of a single carrier modulation system using channel estimation with hysteresis-based SNF-ADC is evaluated by computer simulation, where $\beta$ in Eq.(1) is set to 0.4. The system block diagram is the same as in Fig. 1, where both models of ADC in actual received signal and MLSE equalizer are used as Eq.(1). A roll-off factor of the LPF is 0.5. A step size in Eq.(5) is set to $\mu = 0.1$. Training signal is the PN sequence and its length is 512 [4]. The channel model is assumed to be quasistatic and equal level 6-path Rayleigh fading ($N = 6$). The receiver consists of a sixth-order Butterworth filter as a BPF, followed by the ADC. The IF sampling frequency at the ADC is given as $f_{\text{sample}} = 32f_s$, where $f_s$ is the base-band symbol frequency. The normalized IF frequency is 1.5.

Figure 3 (a) depicts distributions of the normalized MSE (NMSE) of the estimated channel for 1000 different channel realizations, where one and two-bit resolution traditional ADCs and one-bit resolution hysteresis-based SNF-ADC are used. Here, NMSE is defined as

\[
\text{NMSE} = \frac{||h - \hat{h}^{(N_{it})}||_2^2}{||h||_2^2},
\]

where $|| \cdot ||_2$ denotes the Euclidean norm and $N_{it}$ denotes the number of iterations in the LMS algorithm. We assume that $N_{it}$ is high enough for the parameter convergence. Here, the blue and the green plots show the case with the one-bit ADC and the two-bit ADC [4]. The red plots show the one-bit hysteresis-based SNF-ADC. For comparison, the case with the ideal ADC, which resolution is infinity, is also shown as the black line. From this figure, we can confirm that channel estimation with the hysteresis-based SNF-ADC achieves better MMSEs than cases with traditional ADC. We can also see that the variance of the NMSE in channel estimation can be reduced by using hysteresis-based SNF-ADC compared with the case of the traditional two-bit ADC.

Figure 3(b) shows the cumulative distribution function (CDF) of the NMSE in channel estimation. Here, CDF of a random variable $Z$ is defined as $\text{CDF}(z) = \text{Prob}(Z \leq z) = \int_{-\infty}^{z} P(t)dt$, where $P(z)$ denotes a probability density function of $z$. In this figure, channel estimation results with hysteresis-based SNF-ADC are compared with those of conventional one or two-bit ADC [4]. For comparison, the result of an ideal ADC is also shown. It is clear from this figure that NMSE of the hysteresis-based SNF-ADC is improved by about 11dB at CDF=0.95, while NMSE of the hysteresis-based SNF-ADC at CDF=0.05 is degraded by 3dB compared with that of conventional channel estimation with one-bit ADC [4]. It is worth mentioning \footnote{In [4], channel estimation is carried out without knowing actual $\Delta T$ and $N$ beforehand.}
that the hysteresis-based SNF-ADC achieves better NMSE than case with two-bit traditional ADC at CDF=0.95. This means that using the hysteresis-based SNF-ADC is effective in improving the worst-case accuracy in channel estimation compared with traditional ADC.

Figure 3 (c) shows BER performance of single carrier modulation systems using the one-bit ADC [4], the two-bit ADC [4], and hysteresis-based SNF-ADC. For comparison, BER with ideal channel estimation is shown with dotted lines. From this figure, it is confirmed that BER performance of case with hysteresis-based SNF-ADC is improved compared to the one-bit traditional ADC in both ideal and actual channel estimation cases.

5 Conclusion
In this article, we have investigated an extended iterative channel estimation technique with one-bit resolution hysteresis-based SNF-ADC to discuss the impact of using the hysteresis-based SNF-ADC on channel estimation
accuracy in single-carrier modulation with a nonlinear equalization. Simulation results show that the channel estimation accuracy is improved by using hysteresis-based SNF-ADC and bit error rate (BER) performance is improved compared to cases with only one bit resolution ADC.

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