Phase engineering techniques in superconducting quantum electronics

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Abstract. Due to the pulse driven nature of the Rapid Single Flux Quantum electronics nearly every basic cell requires the capability of temporary data storing. Implementing phase shifting elements in this essential device leads to several advantages concerning the device characteristics. There are different concepts enabling phase shifting elements. We give a comparative overview about these approaches. The effect of this novel element on a basic cell is analyzed exemplifying a toggle-flip-flop. Based on the effective noise temperature determined from the experimental results of a standard flip-flop, the bit error rate for several toggle-flip-flop realizations containing different phase shifting elements was calculated. A significantly improved area of function could be shown by simulated error rates lower than $10^{-12}$ with a DC bias margin better than $\pm 63.5\%$.

1. Introduction
The Rapid Single Flux Quantum (RSFQ) electronics is a fast intrinsically digital circuit family where the information is represented by the magnetic flux quantum $\Phi_0 = h / 2e$ with the Planck’s constant $h$ and the elementary charge $e$ [1]. It consists of small superconducting loops disrupted by a well designed barrier called Josephson junction. The Josephson junction is the active element of this network technique acting like a kind of gate allowing the controlled exchange of flux quanta between adjoining loops. Combined with the inductance $L$ and the bias current source $I_B$ there are three elements in RSFQ defining the functionality which is in static conditions comprehensively described by the current-phase relation. Using them the three basic blocks for transmission, decision and storing can be constructed, which are fundamental for every superconducting circuit [2].

Since the pulse driven nature of RSFQ electronics the capability of temporary data storage is important for every logic device. A superconducting loop which is able to store a flux quantum is a naturally tristable system [3], thus a bistable characteristic has to be artifically created. In the conventional way a bias current source is used to restrict the number of stable states. Often this current has to be injected between the junction pair of a comparator. This injection spot is very sensitive to any parameter variation, so the biasing perturbs the decision process. This is a drawback for the resulting device restricting the area of operation. Using phase shifting elements to establish a bistable data storage as proposed in [4] is an expedient approach to provide a bistable circuit characteristic without a negative influence on comparator configurations. The resulting circuits feature distinctly improved stability and delivers a high fabrication yield.
2. Phase shifting elements

Phase shifting elements can be accounted as a fourth novel component of RSFQ electronics. There are several approaches leading to such an additional element. Some of them can easily be integrated into standard mature fabrication processes whereas others require a new technology. One well known way is to utilize a constant current flowing through an inductance biasing the phase like illustrated in Fig.1. This technique was already used in the early stages of RSFQ electronics realizations [5]. The phase shift caused by this configuration can be varied by the current source $I_p$. Thus the current-phase relation of the whole device is given by

$$\varphi = \frac{2\pi L}{\Phi_0} (I + I_p). \tag{1}$$

According to Eq.1 every arbitrary phase shift can be created with this concept. To implement this technique into a standard RSFQ circuit an external negative bias source is required. To realize it in small circuits the superconductive chip only needs an additional connection which is used to contact the negative bias source. The requirements on the semiconducting control environment are growing because of the negative voltage source. The application in large scale integration is more complex hence the technology needs to be improved by an additional superconducting layer which provides the second bias source.

Another concept based on trapped magnetic flux inside a superconducting ring with a total

![Figure 1. The configuration of the simplest phase shifting element](image)

loop inductance of $2L_r$ is proposed in [6]. The configuration is displayed in Tab.1 labeled with version (A). This concept was already successful implemented into a RSFQ circuit [7]. It is important to ensure that exactly one flux quantum is trapped inside the ring. Thus the ring has to be designed in a reasonable way to guarantee only one single flux quantum can be trapped [8]. In Tab.1 this circumstances is represented in the equivalent circuit by the $2\pi$ phase shift within the loop. The effective realized phase shift can only be regulated during the layout process by varying the location of the terminals. If both terminals split the loop inductance into equal parts the realized phase shift is $\pi$, which is the maximum producible phase shift with this concept. In that case the current-phase relation can be calculated by

$$\varphi = \pi + \frac{\pi L_r I}{\Phi_0}. \tag{2}$$

The configuration illustrated in Fig.1 has the same current-phase relation, if the inductance is defined to $L = L_r/2$ and the current is arranged to a convenient value

$$I_p = \frac{\Phi_0}{2L}. \tag{3}$$

We use this analogy in simulations to model a phase shift within RSFQ circuits. The two other phase shifting techniques (version B and C in Tab.1) are based on $\pi$ junctions.
Table 1. Overview about several concepts of phase shifting elements. The parameters of the simulation model are $L^* = 1\, \text{fH}$ and $I^* = 1.034\, \text{A}$.

| Version | Topology | Equivalent circuit | Simulation model |
|---------|----------|--------------------|------------------|
| A)      | ![Diagram A](image) | ![Diagram B](image) | ![Diagram C](image) |
| B)      | ![Diagram D](image) | ![Diagram E](image) | ![Diagram F](image) |
| C)      | ![Diagram G](image) | ![Diagram H](image) | ![Diagram I](image) |

They behave like Josephson junctions with a negative critical current $I = -I_c \sin(\phi)$. That means the current-phase characteristic has a constant phase shift $I = I_c \sin(\phi - \pi)$. Currently there are two approaches known providing such a new component. One of them based on the d-wave symmetry of YBCO [9]. This technique enables the construction of superconducting rings consisting of two junctions and an inductance enclosing an intrinsic $\pi$-phase shift. This phase offset occurs at one of the junctions, thus the symbol in the equivalent circuit of version (B) in Tab.1 is coupled with one of them, to which one can not be determined. To generate the equivalent circuit, one junction has to be defined to normal or incorporated $\pi$-shift behavior. The current-phase relation of the neighboring junctions results from this definition.

Table 1 also shows the concept (C) based on ferromagnetic material within the separating barrier between two superconducting materials. They are denoted by SFS-junctions. Depending on the thickness of the ferromagnetic barrier a standard Josephson junction or a $\pi$-junction can be constructed [10]. This technology provides $\pi$-junctions as lumped elements independent of any constructed loops or environmental circuits and it is therefore a very universal solution.

From our present point of view, the simulation model of both types of $\pi$-junctions is the same albeit they are based on different technologies. To model a $\pi$-junction we utilized the analogy to the Josephson junction. The phase offset is produced by an inductance in combination with a current source (Fig.1). The inductance value is chosen in a way that it is negligible in comparison to every other inductance inside the circuit. According to Eq.(3) the value of the current source...
to provide a $\pi$-phase shift can be calculated.

3. Toggle-flip-flop Realizations in different technologies

The Toggle-Flip-Flop (TFF) is a well known logic cell of RSFQ-electronics and it has often been the subject of studies. It was, for example, one of the first mentioned RSFQ basic cells [5] and it is today the device with highest ever measured clock frequency of 770GHz [11]. We investigated the influence of the previously mentioned phase shifting elements to this standard device.

3.1. TFF in a standard Niobium trilayer fabrication process

The reference device is a TFF fabricated in the standard 1kA/cm² Niobium trilayer process of FLUXONICS Foundry [12]. The equivalent network is illustrated in Fig.2. The core of the TFF is composed of two comparators (J4,J2) and (J5,J3) coupled by the inductance $L_{\text{store}}$. If a flux quantum enters the TFF cell input and pass through J1, the junctions of the core will switch in pairs J2 and J3 or J4 and J5 depending on the direction of the current flowing in the inductance $L_{\text{store}}$. This circulating current represents the internal logical state of the flip-flop. For each input pulse the state toggles between "0" and "1" which directly corresponds to the number of flux quanta stored in the loop. This behavior is illustrated in Fig.3.

![Figure 2. a) The equivalent circuit of a TFF in standard Niobium trilayer technology b) and the photograph of the circuit fabricated at FLUXONICS-Foundry [12]. The critical currents of the junctions are: 150$\mu$A: J5; 200$\mu$A: J4,J6; 250$\mu$A: J1,J3,J7,J8; 300$\mu$A: J2.](image)

The TFF core is embedded in Josephson transmission lines (JTL) to reduce the redistribution currents into adjoining cells and ensure therewith the main principle of a cell based design. The bias currents IB1 and IB3 serve as supply for these JTL's, but the current source IB2 is functional because it creates the bistable nature of the TFF core. One typical problem in the RSFQ circuit fabrication is the global deviation of the critical current densities. This effect can be compensated by an adaption of the global circuit bias level, but this technique does not work in case of IB2, because its value is defined by the inductance By compensating deviations of the critical current density IB2 is wrongly changed, leading to a wrong value of the phase shift within inductance $L_{\text{store}}$. This effect and the influence of noise, introduced by the current source IB2 between the two junctions, on the comparator (J2,J4) is a serious problem for the dynamic reliability of the standard TFF.

3.2. TFF with $\pi$-rings

The first successful realization of a digital circuit containing active junctions with intrinsic $\pi$-phase shifts exemplifies a TFF whose core is composed of $\pi$-rings [13]. This device behaves like the mentioned standard TFF, while the equivalent network displayed in Fig.4 differs in some details. The core consists of two $\pi$-rings (J4-$L_{\text{store}}$-J3 and J2-$L_{\text{store}}$-J5) introduced in section 2.
The circulating current flowing in the shared inductance $L_{store}$ has in contrast to the standard TFF the same magnitude in both logical states of the device. Together with the direction of this current toggles the magnetic flux stored in the $\pi$-rings between $-\Phi_0/2$ and $+\Phi_0/2$. The result of this characteristic is an unsurpassed network symmetry (Fig.4a) delivering a remarkable improved tolerance against parameter deviations like mentioned in [3].

There are several restrictions during the layout process as consequence of the d-wave symmetry of YBCO. The relative adjustment of the junctions within a loop determinate $\pi$-rings and conventional rings, according to section 2. Thus the geometrical orientation of a junction becomes restricted. For example, the junction J7 of the JTL connected to an output of the TFF requires the same orientation as the output junction J5, displayed in Fig.4b. For this loop the sum of all phase shifts is $2\pi$ and so it is a conventional ring.

### 3.3. TFF with a frozen flux quantum inside a superconducting ring

The realization based on a passive phase shifting element substituting the storage inductance as proposed by Ustinov [4]. In contrast to this concept the utilization of a small ring with a frozen...
single flux quantum has a linear current-phase relation, mentioned in section 2. In difference to the TFF described in the preceding paragraph the source of the phase shift is here the magnetic flux trapped inside the ring composed by $2L_r$. This element causes the bistable characteristic of the TFF core. The functionality as well as the quality of state representation is the same as in the TFF with $\pi$-rings.

The equivalent circuit illustrated in Fig.5 exclusively consists of conventional RSFQ components. Thus no special considerations have to be done while implementing such a phase shifting element into a RSFQ circuit, fabricated in a standard technology. A challenge is the design of the flux trapping ring [8]. Indeed the principle of flux quantization ensures an integer number of stored flux quanta, but the configuration has to be reasonably designed to guarantee a single frozen flux quantum. A first successful realization and experimental analyses are reported in [7].

### 3.4. TFF with active $\pi$-junctions

Applying SFS-junctions is at present the most promising technique to realize a lumped element $\pi$-junction. There exist several successful demonstrations of such a junction type reported by several groups [14][15][16][17]. But to realize the concept displayed in Fig.6 it requires a technology providing Josephson junctions in combination with $\pi$-junctions. It can be expected that properties and conclusions determined for circuits with $\pi$-rings can also be transferred to such a future technology. One possible advantage of such a fabrication process could be a reduced number of restrictions resulting directly in a relaxed design process. Figure 6 shows a reasonable layout of an assumed SFS-technology. In contrast to d-wave introduced $\pi$-junction the orientation of a junction is not restricted here. Current developments in this area are based on intrinsically shunted junctions, hence our layout concept also consists of this junction type. While a single octagon marks a Josephson junction, the $\pi$-junctions have an additional black painted circle.

### 4. Bit Error Rate

In experimental analyses we evaluated the bit error rate (BER) of a standard TFF (Fig.2). A semiconducting control electronics provided a 40 kHz clock signal and monitored the output signal of the RSFQ circuit boosted by a semiconducting amplifier. The BER was measured depending on the bias current. The area of operation was passed trough with $1\mu A$ increment varying the value of the separated TFF bias current. For each step $10^3$ switching events were
Figure 6. a) A supposable equivalent circuit of a TFF composed of Josephson junctions and lumped element \( \pi \)-junctions b) A possible layout concept for an assumed SFS-technology

tested. In the transition area between correct function and malfunction the number of clock cycles was increased to \( 10^5 \). The collected data is displayed in Fig.7.

In theory the error rate and bias current \( (I_b) \) relation is well approximated by the error function

\[
BER = 0.5 + 0.5 \text{erf}(b_2(I_b - b_1)).
\] (4)

The parameter \( b_1 \) is the bias current where the error rate becomes 0.5 [18]. The slope of this function depends on parameter \( b_2 \) which can be determined by

\[
b_2 = \sqrt{\frac{R}{8k_BT}},
\] (5)

with the bandwidth \( B \) of the system, the resistance \( R \), the Boltzmann constant \( k_B \) and the Temperature \( T \). The fitting curves illustrated in Fig.7 are obtained by using Eq.(4). It is well known that the slope of both edges can be unequal, resulting in different values of \( b_2 \) [18] [19]. This corresponds with different effective temperatures for the rising and falling edge which diverge from the physical temperature.

We accomplished simulation studies on the equivalent circuit utilizing the circuit simulator program J-SIM [20] with the noise model implemented by Satchell [21]. We simulated 1000 clock cycles with a clock frequency of 10GHz. In case of a bit error rate smaller than 1% the number of clock cycles was increased to \( 10^4 \). Several different equivalent temperatures were estimated, finally we found the best match with the measured data by using \( T_1 = 12\text{K} \) for the falling and \( T_2 = 5\text{K} \) for the rising edge. The simulated data with these estimated effective noise temperatures are displayed in Fig.7.

5. Analyzing the TFF with intrinsic \( \pi \)-phase shifts

In [3] we have analyzed the influence of phase shifts on a separate storage loop. But a storage cell in RSFQ circuit is more complex, due to the redistribution currents between adjoining circuitry parts. Thus we accomplished the circuit simulations of TFF’s with phase shifting elements nested in a RSFQ environment. The phase shifting elements was modeled according to Tab.1. The utilized equivalent circuits contain reasonable values for parasitic inductances as well as additional elements caused by the characteristics of the technology. So we constricted the analyses to the flip-flops which are already realized. The bit error rate was used to compare the features of the TFF’s. To evaluate this parameter we assumed the effective noise temperatures which were identified in section 4. The resulting curves and the fitting curves based on Eq.(4) are illustrated in Fig.8.

The parameter \( b_2 \) of the fitted function is listed in Tab.2. The function was extrapolated to a BER of \( 10^{-12} \), which is estimated to be appropriate for digital applications. The margins for this
Figure 7. The DC bias dependence of the error rate of the standard TFF fabricated at FLUXONICS-Foundry [12]. The fitting curves are obtained by using Eq.(4).

Figure 8. The simulated DC bias dependence of the error rate of several TFF realizations. The fitting curves are obtained by using Eq.(4).

Table 2. Overview about the results of the analysis

|                     | standard TFF | TFF with π-rings | TFF with frozen flux |
|---------------------|--------------|------------------|----------------------|
| figure              | 2            | 4                | 5                    |
| $b_2$ falling edge  | 25           | 37               | 105                  |
| $b_2$ rising edge   | -36          | -69              | -120                 |
| margin for BER=10^{-12} | -7.5%       | -86.5%           | -76%                 |
| margin for BER=10^{-12} | +21%         | +81.5%           | +63.5%               |

error rate are also listed in Tab.2. The results of the simulations prove a significant improved dynamic reliability of the TFF’s with implemented phase shifting elements. The probability of a noise introduced switching error decreased drastically. Removing the bias current input (IB2 in Fig.2) is the main reason for the improved dynamic reliability. The utilized phase shifting elements are acting like a noiseless current source which does not perturb the decision process of the comparator inside the TFF core. Deviations between the TFF with different phase shifting elements were observed, but it can be assumed that they are the result of differing technology characteristics and do not depend on the source of the phase shift.

6. Conclusions

In this paper an overview about several concepts of realizing phase shifting elements was given with particular regard to the variability of the phase shifts and the requirements to the fabrication technology. Special technology features and restrictions which have to be considered during the design process were exemplified by a toggle-flip-flop. By experimental analysis the bit error rate dependent on the DC bias of a standard TFF was determined. Based on this data the effective noise temperatures were identified to be 12K for the falling and 5K for the raising edge of the BER function. These temperature values were the base for a simulation study of TFF’s containing phase shifting elements. A significant increased
region of function could be shown by a wide DC bias margin of at least ±63.5% with an error rate of 10^{-12}. The application of phase shifting elements as noiseless current sources which do not perturb the decision process of the adjoining comparator was mentioned to be the main reason for the improved dynamic reliability.

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