Solution processed fullerene (C$_{60}$) molecular floating gate layer has been employed in low voltage nonvolatile memory device on flexible substrates. We systematically studied the charge trapping mechanism of the fullerene floating gate for both p-type pentacene and n-type copper hexadecafluorophthalocyanine (F$_{16}$CuPc) semiconductor in a transistor based flash memory architecture. The devices based on pentacene as semiconductor exhibited both hole and electron trapping ability, whereas devices with F$_{16}$CuPc trapped electrons alone due to abundant electron density. All the devices exhibited large memory window, long charge retention time, good endurance property and excellent flexibility. The obtained results have great potential for application in large area flexible electronic devices.
F_{16}CuPc device trapped electrons alone with a memory window of 2 V. All the devices exhibited charge retention larger than 10^7 s with good cell-to-cell uniformity. The electrical performances of all the devices are well-maintained even after 500 programming/erasing cycles and did not degrade substantially upon bending.

**Results**

**Device structure and operation mechanism.** The overall fabrication of the memory transistor is illustrated schematically in Figure 1a. Atomic layer deposited aluminum oxide (Al₂O₃) was selected as the blocking dielectric layer on top of the silver (Ag) gate electrode on flexible poly(ethylene terephthalate) (PET) substrate. The atomic layer deposition technique allows for a high quality, defect-free dielectric layer with good barrier properties at low substrate temperature. Al₂O₃ has been demonstrated as a promising high-k dielectric candidate to minimize gate leakage current and achieve low voltage operation in thin film memory transistors. C₆₀ was spin-coated over the Al₂O₃ and then thermally annealed at 120°C for 10 min. A thin layer of poly(4-vinylphenol) (PVP) was then spin-coated onto the C₆₀ layer using orthogonal solvents in order to prevent the dissolution of the C₆₀ layer. A detailed description of the fabrication process is given in the experimental section. PVP possesses high resistivity and thermal stability, and has been demonstrated as a good polymer dielectrics. In our designed dielectric system, PVP has relatively low dielectric constant (4.7) compared with Al₂O₃ (7). According to the equation $E_1 = \frac{V_{g}}{d_1 + d_2 \left(\varepsilon_1/\varepsilon_2\right)}$, where $\varepsilon_i$ are the dielectric constants and $d_i$ are the thicknesses of the two dielectric layers, the applied electrical field in the PVP layer ($E_1$) is relatively stronger than in Al₂O₃ layer. Therefore, this system enables efficient charge transfer from the semiconductor layer to charge trapping layer through the tunnelling dielectric layer. Due to their good stabilities in ambient, pentacene and F₁₆CuPc were chosen as the p-type and n-type semiconductor to investigate the charging mechanism of the C₆₀ floating gate layer. Figure 1b illustrates the chemical structures of the organic small molecular materials used in this study. Figure 1c displays the atomic force microscopy (AFM) image of the C₆₀ film spin-coated at 1000 rpm. The C₆₀ film exhibited a surface morphology of separated islands, which is favorable for charge storage. The surface morphology of the C₆₀ film spin-coated through high speed is also analyzed and shows relatively low densities (see supporting information Figure S1). Previous studies have shown that the memory capacity is dependent on the charge trapping element density, while the memory window increases with enhanced trapping sites. Therefore, unless otherwise mentioned, all the memory devices are based on a C₆₀ layer resulting from the low spin-coating speed (1000 rpm).

**Electrical performance of p-type memory device.** To investigate the trapping capability of C₆₀ in the p-type memory device, we first fabricated a transistor with pentacene as the semiconductor layer. The schematic representation of the tunnelling of charge carriers in pentacene device is illustrated in Figure 2a. The holes are tunnelled through the PVP layer from the highest occupied molecular orbital (HOMO) of pentacene to C₆₀ layer while electrons are tunnelled from the lowest unoccupied molecular orbital (LUMO) of pentacene to C₆₀ trapping layer. It should be noted that intrinsic hole density is higher than electron density in pentacene. Figure 2b shows the electrical characteristics of the pentacene memory device before and after applying the negative gate pulses (–5 V for 100 ms). The electrical properties were found to be uniform by examining different devices. The memory transistors show a hole mobility of about 5 × 10⁻² cm² V⁻¹ s⁻¹ and current on/off ratio of about 10⁶ while the transistors without C₆₀ possess a mobility of about 0.1 cm² V⁻¹ s⁻¹. The slightly decreased mobility can be attributed to the increased surface roughness when introducing the C₆₀ layer under PVP. The applied electrical field is about 1.1 MV/cm in the tunnelling PVP layer, which is appropriate for efficient charge injection. The high mobility of C₆₀ can guide fast charge distribution and assist the charging process when the charge injection is non-uniform across the C₆₀ layer. The trend of the transfer curves reveals a typical hole trapping behavior indicating holes are injected from pentacene channel into C₆₀ Layer through PVP by the application of

![Figure 1](https://www.nature.com/scientificreports)

**Figure 1** | (a) Schematic diagram depicting the basic fabrication process of the molecular floating gate memory device. (b) Chemical structure of the molecules. (c) Tapping-mode AFM image of the C₆₀ layer.
the electric field. The trapped holes in C₆₀ layer screened the channel and resulted in decreasing the effective gate electric field. In order to analyze the charging effect of the dielectric system, we also fabricated the device without C₆₀ layer (see supporting information Figure S2). Almost negligible charging and discharging is observed in PVP/Al₂O₃ stack layers, therefore the charge carriers should mostly be trapped in C₆₀ Layer. The electrical characteristics of the memory devices before and after applying the positive gate pulses (5 V for 100 ms) are shown in Figure 2c. The results indicate that electron trapping also occurs using C₆₀ as the floating gate. In addition, pentacene has intrinsic electron mobility which makes them available to be trapped. This observation is interesting as most of the flash memory devices are based on single charge carrier trapping mechanism. At the same electrical field, the amount of stored holes is more than the electrons according to the equation Q = C × ΔVth where Q is the stored charges, C is the capacitance of the dielectrics and ΔVth is the threshold voltage shift. The V_th as a function of bias time is summarized in Figure 2d. The V_th shift increases with increased programming operation time, both in hole and electron charging process. Furthermore, V_th reach certain saturated values after long bias time, which is similar with metal nanoparticle floating gate memory. During the charging process, the charge carriers (holes or electrons) trapped in the C₆₀ layer can increase the capacitive coupling effect thus limited amount of trapped charge carriers are available at certain gate bias. In addition, the saturation rate of hole trapping process is observed to be quicker than electron trapping process. This may be attributed to the high hole mobility than electron mobility in pentacene.

With the property of trapping both holes and electrons, the memory window of the pentacene devices could be further enhanced. Figure 3a and 3b show the electrical characteristics of the two states (The state after positive gate bias 5 V for 1 s is denoted as ON state and the state after negative gate bias −5 V for 1 s is denoted as OFF state). The memory window (V_th shift) can reach about 4 V and the
maximum ON/OFF current ratio is about $1.5 \times 10^4$. This result is better than previously reported low voltage memory with conventional charge trapping layers such as evaporated metal layer and self-assembled nanoparticles. It should be noted that the memory window depends strongly on the applied gate bias and larger bias could lead to larger memory windows. Here we kept the applied voltage not exceeding 5 V to ensure the low voltage operation of the memory. The operation mode of the memory transistor has been reproducibly and reversely switched from one state to another state. The endurance properties of the pentacene device were studied by repeated application of gate bias pulses of $\pm 5$ V. Figure 3c illustrates the pulse sequence in the test. The ON and OFF state is well maintained for more than 500 cycles as shown in Figure 3d. In addition, we performed the data retention experiment on the devices and Figure 3e illustrates the test pulse sequence. In between the different measurement points, the devices are kept without applying any gate biases. The retention capability is shown in Figure 3f. The memory window is maintained at 82.1% for $10^4$ s, which is comparable with previously reported low voltage organic memory devices. In our device, the high energy barrier height of C$_{60}$ surrounded by PVP suppresses the charge transport between each C$_{60}$ island. At the same time, charge leakage from C$_{60}$ to the semiconductor channel is effectively prohibited by the PVP tunnelling layer. Therefore, the charge carriers (holes and electrons) are confined at the C$_{60}$ floating gate. Overall, both the positive part and negative part of the memory windows are suitable for the use as nonvolatile storage media.

**Electrical performance of n-type memory device.** We further explore the trapping capability of C$_{60}$ in n-type memory device, in which F$_{16}$CuPc is selected as the semiconductor layer. Figure 4a depicts the energy band diagram of charge carrier tunnelling in F$_{16}$CuPc based device. Figure 4b shows the electrical characteristics.

**Figure 3** | (a) Transfer curve ($I_{DS} - V_{GS}$) of the pentacene memory at ON and OFF state on log scale. (b) Transfer curve ($I_{DS}^{1/2} - V_{GS}$) of the pentacene memory at ON and OFF state on linear scale. (c) Test pulse sequence for the endurance test. (d) Endurance characteristics of the pentacene device as a function of bias cycles. (e) Test pulse sequence for the retention test. (f) Data retention capability as a function of time.
of F16CuPc memory device before and after applying a positive gate pulse (5 V for 100 ms). The electrons tunnelled from F16CuPc channel into the C60 Layer through PVP, resulting in a decreased effective gate electrical field. Such a destructive electrical field leads to a reduced channel conductance, and the transfer curves shift towards the positive direction. The F16CuPc device without C60 layer is also fabricated and almost no charging effect of the dielectric system is observed (see supporting information Figure S3). The memory transistors show an electron mobility of about $1.8 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ and current on/off ratio of about $10^2$ while the F16CuPc transistors without C60 show a mobility of about $3 \times 10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$. Further applying a negative gate pulse ($-5$ V for 100 ms) do not induce a negative shift of the transfer curves, which might be originated from the extremely low hole mobility of F16CuPc$^{50}$. It is understood that available minority carrier (hole) density in F16CuPc is much lower than the minority carrier (electron) density in pentacene. Therefore, we found both electron and hole trapping in pentacene based devices where as only electrons are trapped in F16CuPc based devices. The $V_{th}$ with respect to the bias time is summarized in Figure 4d. The $V_{th}$ shift towards more positive direction with prolonged bias, suggesting that additional charge carrier is brought to the molecular floating gate with increased bias time. The saturated level is also be observed here, demonstrating both trapped holes and electrons would cause capacitive coupling in the C60 floating gate.

Figure 5a and 5b show the electrical characteristics of the F16CuPc memory device at two states (The high conductance state is denoted as ON state and the low conductance state is denoted as OFF state). The memory window is about 2 V and the maximum ON/OFF current ratio is about $7 \times 10^2$. Continuous application of gate bias pulses of $\pm 5$ V for 1 s is carried out to measure the endurance properties as illustrated in Figure 5c. The ON and OFF state has been well maintained for more than 500 cycles as shown in Figure 5d. The test pulse sequence for the data retention test in F16CuPc device is illustrated in Figure 5e. The ON state and OFF state is well separated with respect to the elapsed time as shown in Figure 5f. About 19.2%

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**Figure 4** | (a) Energy band diagram of the F16CuPc based memory device. (b) Transfer characteristics of the memory transistor before and after positive gate bias. (c) Transfer characteristics of the memory transistor before and after negative gate bias. (d) Threshold voltage as a function of the gate bias time.
of the memory window is lost after a retention time of $10^4$ s. The storage ability of the memory is comparable to recently reported memory devices based on n-type semiconductors\textsuperscript{51,52}.

**Bending stability of the memory devices.** In addition to the reliable memory operations, the bending stability is another important parameter to examine the reliability of the flexible devices. The organic/inorganic bilayer dielectric structure used in our device can reduce the possibility of cracking or delamination during repetitive bending\textsuperscript{53}. Flexibility tests using cyclic bending were performed both in tensile and compressive mode with a bending radius of 10 mm. Figure 6a shows the schematic diagram of the bended device in a compressive state and Figure 6b illustrates the tensile state. The strain can be estimated from the equation $D/2R$, where $D$ is the thickness of the substrate and $R$ is the bending radius\textsuperscript{54}. The bending tests were done up to 500 times to confirm the flexibility of both the pentacene and F\textsubscript{16}CuPc devices. Figure 6c and 6d show the memory window as a function of compressive bending cycles. Figure 6e and 6f show the memory window as a function of tensile bending cycles. These results confirm that all the devices exhibit stable programmable properties with good mechanical flexibility.

**Discussion**

The high mobility of C\textsubscript{60} can guide fast charge distribution and assist the charging process when the charge injection is non-uniform across the C\textsubscript{60} layer. For the pentacene based p-type semiconductor devices, the trend of the transfer curves shows a typical hole trapping behavior indicating holes are injected from pentacene channel into C\textsubscript{60} Layer through PVP by the application of the electric field. Due to intrinsic electron mobility as minority carriers, electron trapping also occurs using C\textsubscript{60} as the floating gate in pentacene based devices.

![Figure 5](www.nature.com/scientificreports)

**Figure 5** | (a) Transfer curve ($I_{DS} - V_{GS}$) of the F\textsubscript{16}CuPc memory at ON and OFF state on log scale. (b) Transfer curve ($|I_{DS}|^{1/2} - V_{GS}$) of the F\textsubscript{16}CuPc memory at ON and OFF state on linear scale. (c) Test pulse sequence for the endurance test. (d) Endurance characteristics of the F\textsubscript{16}CuPc device with respect to the number of bias operations. (e) Test pulse sequence for the retention test. (f) Data retention capability with respect to the elapsed time.
addition, due to the high intrinsic hole mobility of holes than electrons in pentacene, the saturation rate of hole trapping process is observed to be quicker than electron trapping process. For the pentacene based devices, both the positive part and negative part of the memory windows are suitable for the use as nonvolatile storage media. On the other hand, for the devices based on n-type semiconductor F16CuPc, available minority carrier (hole) density is much lower than the minority carrier (electron) density in pentacene. Therefore, only electrons are trapped in F16CuPc based devices. The electrons tunnelled from F16CuPc channel into the C60 layer through PVP, resulting in a decreased effective gate electrical field which leads to a reduced channel conductance, and the transfer curves shift towards the positive direction. During the charging process, due to the increased capacitive coupling between the trapped charge carriers (holes or electrons) in the C60 layer limited amount of trapped charge carriers are available at certain gate bias for both pentacene and F16CuPc based devices.

Although metal nano-floating gate have been widely investigated as the charge trapping layer in flash memories, they are still suffering from poor processability to implement them in printing technology. The solution processed molecular materials should be a choice for large area printable electronics. On the other hand, unlike conventional metal or metal nanoparticle based memory device, the trapping capability of C60 will be of great importance to realize functional nonvolatile memory. Since molecular materials can be functionalized to obtain multifunctional properties, it is important to understand the working mechanism of such molecular floating gate devices. The C60 floating gates showed ambipolar trapping behavior in the pentacene based memories and unipolar trapping behavior in the F16CuPc based memories. The approach to trap both holes and electrons in memory devices is an important to achieve large memory window and other electrically variable properties.

Our fabrication methods including the fabrication of C60 molecular floating gate layer and PVP tunneling dielectric layer are solution-processed. The simplified fabrication steps and low temperature processing method is quite promising for flexible electronics. The successful adopting of this structure on flexible substrates demonstrates that this method is mass-producible to construct innovative large area electronics.

In conclusion, we have demonstrated that solution processed C60 could be an excellent candidate for molecular floating gate in flexible flash memories. By adopting C60 as the charge trapping layer in both pentacene and F16CuPc memory transistors, reliable p-type and n-type memory devices has been achieved. All these devices show large memory window, long retention time, good endurance properties and excellent mechanical flexibilities. More importantly, our results
show that the use of molecular floating gate for the realization of new organic flash memory devices offers a promising route for the future development of advanced organic electronics.

**Methods**

**Materials.** PVP (average Mw ~25,000), C60 (99.5%), pentacene (sulfonated grade) and F2,4CuPc (sulfonated grade) were purchased from Aldrich. PET substrates were cut from commercially available PET films. All chemicals and solvents were used without further purification in the experiment.

**Device fabrication.** PET substrate was cleaned in an ultrasonic bath with detergent, acetonitrile, and isopropanol prior to processing. 20 nm Ag film was thermally evaporated as the gate electrode: 40 nm Al2O3 layer was deposited using a Savannah 100 ALD system at a substrate temperature of 80 °C. C60 was dissolved in 1,2,4-trichlorobenzene (TCB) (10 mg ml\(^{-1}\) and spin-coated at different speeds on the Al2O3 layer with subsequent annealing for 1 min at 120 °C in a nitrogen environment. After that, the PVP film was fabricated by spin-coating the prepared solution (5 mg ml\(^{-1}\) in isopropanol). The resulting film was annealed at 100 °C for 1 h in a vacuum oven and the thickness was about 20 nm. 40 nm pentacene or 25 nm F2,4CuPc were thermally deposited as the semiconductor layer at a rate of 0.1 to 0.2 Å s\(^{-1}\). The substrate temperature was always kept at room temperature when depositing the p-type and n-type semiconductor films. Gold (Au) electrodes were employed as the source and drain contacts for both p-channel and n-channel memory transistors. 40 nm Au films were thermally evaporated through a shadow mask at a rate of 0.2 Å s\(^{-1}\), with a channel length to channel width ratio of 50 μm/1000 μm.

**Characterization.** The morphology of the C60 layer was investigated by AFM (Veeco Multi mode). The thicknesses of the deposited films were measured by an ellipsometer. The electrical characteristics of the memory transistors were measured using a Keithley 2412 source meter. All measurements were conducted in an atmospheric environment with a relative humidity of 60% and a temperature of 25 °C.

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Author contributions
Y.Z. performed the experiments and wrote the paper. S.T.H., Y.Y., L.B.H., L.Z. and J.H. assisted with the experiments, discussed the results and commented on the manuscript. V.A.L.R. supervised the project and finalized the manuscript.

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