Stream Processor Generator for HPC to Embedded Applications on FPGA-based System Platform

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Abstract—This paper presents a stream processor generator, called SPGen, for FPGA-based system-on-chip platforms. In our research project, we use an FPGA as a common platform for applications ranging from HPC to embedded/robotics computing. Pipelining in application-specific stream processors brings FPGAs power-efficient and high-performance computing. However, poor productivity in developing custom pipelines prevents the reconfigurable platform from being widely and easily used. SPGen aims at assisting developers to design and implement high-throughput stream processors by generating their HDL codes with our domain-specific high-level stream processing description, called SPD. With an example of fluid dynamics computation, we validate SPD for describing a real application and verify SPGen for synthesis with a pipelined data-flow graph. We also demonstrate that SPGen allows us to easily explore a design space for finding better implementation than a hand-designed one.

I. INTRODUCTION

Advancement of FPGA technologies has made custom computing machines more promising and feasible for a wide range of applications from high-performance computing (HPC) to embedded computing. Dedicated pipelines implemented on reconfigurable devices can achieve higher performance per power with efficient use of a limited bandwidth for external memories. In addition to the FPGA's prominent performance of non-arithmetic applications, e.g., pattern matching with regular expressions, state-of-the-art FPGAs overcome general-purpose microprocessors even for floating-point computations. It is announced that the next generation of FPGAs will have 10 GFlops [1], which is higher than that of a present GPU. Thus FPGAs are expected to bring a breakthrough even in supercomputing where conventional approaches with CPUs and GPUs are suffering from a low efficiency of bandwidth and power [14]. Furthermore, the tightly-coupled architecture with FPGA fabric and a hard-core ARM processor [2] also allows more flexible and all-in-one computation especially fit for embedded/robotics applications.

In our research project, we have developed an FPGA-based common system-on-chip (SoC) platform for power-efficient computation in the wide range of applications. The platform has a microprocessor, peripherals including a PCI-Express interface and network interfaces with remote DMA engines, and reconfigurable stream processors with their local DMA engines. The stream processors are application-specific computing pipelines to accelerate kernels of a target application. The microprocessor controls the DMA engines and the peripherals while it can also perform irregular and auxiliary computations. If the performance has to be scaled with multiple FPGAs, we can give the SoC platforms a dedicated network to directly connect FPGAs.

So far, we have demonstrated feasibility of the FPGA-based power-efficient computation with the SoC platform and stream processors for floating-point computations [8], [11], [12]. However poor productivity is still a big issue in developing application-specific pipelines. Implementation with a hardware description language (HDL) is not easy, requiring a sufficient skill and a long time. For example, development of the stream processor for fluid dynamics simulation [8], [12] required designing and implementing sub-modules each of which is for a part of an entire stream computation, a top module to connect the sub-modules with adequate delay insertion, and interface logics for the SoC platform. These steps are not only tedious and time-consuming, but also error-prone. To concentrate on algorithm design, we need a tool to generate an application-specific stream processor with high-level description.

In this paper, we present a stream processor generator, SPGen, which generates a stream processor for the SoC platform with high-level stream processing description, called SPD. In SPD, we simply write numerical equations and calls of user-defined hardware modules. SPGen gives the processor a stream interface to be used in embedding it into the SoC platform. We can specify a target frequency to change the pipeline depth for design space exploration under a trade-off between area and throughput. Contributions of this work are:

1) SPGen to generate a stream processor for floating-point computations with equations and user-defined modules,
2) domain-specific stream processing description (SPD),
3) verification and evaluation with practical computation.

This paper is organized as follows. Section II summarizes related work. Section III describes the FPGA-based SoC platform, a stream computing model, and a stream processor. Section IV presents SPGen after introducing the SPD format. Section V shows verification and evaluation of SPGen with an example of fluid computation based on the lattice Boltzmann method. Finally, Section VI gives conclusions and future work.

II. RELATED WORK

Recent advancement has allowed FPGAs to be programmed with high-level abstraction, by supporting conventional programming languages including C and Java with some extension or limitation. Tools or compilers such as Impulse-C [7], AutoPilot [15], Symphony [13], and a formal design framework [6] can be used to implement an IP core in high-level languages instead of describing RTL in HDL. Although their abstraction of description is useful, SPGen is more specific to a domain of stream computation with floating-point operators to easily develop high-throughput pipelines of numerical applications. We also leave the door open to extend a stream processor beyond just a computing pipeline.
DDRx Memory

 DMA

 Stream Computing

 Processor

 Data Interconnect

 Control Interconnect

 Micro-

 Memory

 RDMA

 NIC 1

 PCIe

 NIC m

 I/O

 Stream processor

 DMA

 PCIe

 RDMA

 NIC 1

 NIC m

 I/O

 Fig. 1. FPGA-based common system-on-chip platform.

 Fig. 2. Definition of a stream processor.

 and I/O modules. The PCIe is necessary if the FPGA operates as a slave of a host PC. The NICs are used to scale the system and the performance over multiple FPGAs directly connected by their dedicated network. The I/O modules are necessary for robotics applications receiving data from sensors and controlling actuators. Reconfigurability of FPGAs allows us to implement only necessary modules on the system under resource constraint.

 B. Stream computing model and stream processor

 We define data streams $S_i^{\text{in}}$ and $S_i^{\text{out}}$ as follows, which correspond to inputs and outputs of computation, respectively.

 $$ S_i^{\text{in}} \equiv \{ v_i^{\text{in}}, v_1^{\text{in}}, \ldots, v_i^{\text{in}}, v_n^{\text{in}} \} $$

 $$ S_i^{\text{out}} \equiv \{ v_i^{\text{out}}, v_1^{\text{out}}, \ldots, v_i^{\text{out}}, v_n^{\text{out}} \} $$

 where each element of these series is a vector: $v_i^{\text{in}} \equiv \{ v_i^{\text{in}}(1), v_i^{\text{in}}(2), \ldots, v_i^{\text{in}}(m) \}$ and $v_i^{\text{out}} \equiv \{ v_i^{\text{out}}(1), v_i^{\text{out}}(2), \ldots, v_i^{\text{out}}(m) \}$. With the input and output data-streams, the stream computation that we use is modeled by $v_i^{\text{out}} = f(v_i^{\text{in}}, v_1^{\text{in}}, \ldots, v_n^{\text{in}}, v_i^{\text{in}}(1))$, which means that the $i$-th output is obtained by computing with $(N+M+1)$ input vectors around the $i$-th input. If $v_i^{\text{out}}$ can be computed only with $v_i^{\text{in}}$, then $M = N = 0$. The function $f()$ can contain any numerical computations or other processing. A simple example with an input vector $v_i^{\text{in}} = \{ a, b, c, d \}$ and an output vector $v_i^{\text{out}} = \{ l(g, sm) \}$ is:

 $$ tmp1 = (a - b)/2, $$

 $$ tmp2 = tmp1 + c + d, $$

 $$ (l(g, sm)) = \begin{cases} (tmp2, tmp1), & (tmp1 < tmp2) \\ (tmp1, tmp2), & \text{(otherwise)} \end{cases} $$

 where $tmp1$ and $tmp2$ are temporal variables used internally.

 Fig. 2 shows a stream processor to compute $v_i^{\text{out}}$ with $v_i^{\text{in}}$. The inputs of $v_i^{\text{in}}$ for $k \neq i$ are obtained by using an internal buffer to hold input vectors for a certain number of cycles. The stream processor is a computing pipeline with a throughput of one. Vectors are input and output to/from the stream processor synchronously one by one every cycle. The computation takes $n$ cycles for $n$ pipeline stages. The more stages we have, the more computations can be performed at a constant throughput. Thus the higher computing performance can be achieved by unrolling a computing kernel to increase the number of operations in a pipeline.

 The stream processor has an interface to be embedded into the SoC platform of Fig. 1. We adopt an interconnection standard, called Avalon-ST, provided in Qsys system integration tool. Avalon-ST is simple and lightweight interface for data streaming, which includes data and control signals of valid, ready, start of packet (sop), end of packet (eop), and empty bytes in data. For Avalon-ST interface, the stream processor
is composed of the stream processing core and the other peripheral modules to handle the signals.

C. Conventional development flow of stream processors

So far, the following development flow has been required:
1) design a stream algorithm as a data flow graph (DFG)
2) design and implement modules of nodes in DFG,
3) connect modules with delays inserted for synchronization,
4) write a top module with Avalon-ST interface,
5) write a configuration file in tcl for Qsys.

Let’s suppose a simple stream processor of Fig.3 for Eqs.(3) to (5). In this example, the fundamental modules in DFG are the nodes: Eq.(3), Eq.(4), “Less-than” of Eq.(5) to compare for \( \text{tmp}1 < \text{tmp}2 \), and “Swap” of Eq.(5) to multiplex \( \text{tmp}1 \) and \( \text{tmp}2 \). In Step 2, we implement the modules for these nodes. We use FloPoCo tool [5] to generate an equation module as a pipeline with floating-point operators. For the other modules, called HDL modules, we write HDL codes. In Step 3, we connect the modules considering their delays. To synchronize data flowing through the DFG, we have to adequately insert delay modules as shown in Fig.4. Although less delays are preferable in terms of resource consumption, it is not easy to find the best delay insertion when a lot of nodes are connected. In Step 4, we write an HDL code for the top module containing the stream processing core of the DFG and peripheral modules for Avalon-ST interface. Finally, in Step 5, we need to write a tcl-based configuration file containing the module information for the Qsys system integration tool.

The example of Fig.4 is quite simple, however, for example, fluid dynamics computation requires a complex DFG connecting more nodes, resulting in a long development time. In addition to difficulty in finding adequate delay insertions, implementing and connecting a lot of modules are time-consuming and error-prone. To improve this poor productivity, we need a tool to automate Steps 2 to 5 and allow developers to concentrate on designing and exploring algorithms.

IV. SPGen: Stream Processor Generator

A. Overview of SPGen

We propose and develop a stream processor generator, called SPGen, to automate Steps 3 to 5 and a part of Step 2. Our requirements for SPGen are as follows:
1) Stream computing is given by its own simple and easy description with equations and module calls,
2) Users can write their own modules in HDL for non-numerical processing.
3) Users can control pipelining for design space exploration.
4) The output of SPGen is a core with Avalon-ST interfaces, which can be embedded into the SoC platform.

To easily describe stream computation for SPGen, we define a domain-specific stream processing description, called SPD. Although high-level descriptions like C language are not supported for now, we plan to develop code-to-code translation tools for them. In SPD, stream computation can be written with equations and module calls. SPGen generates equation modules by using the FloPoCo tool for equations. The combination of high-level equation description and low-level module-call description allows designers to easily implement a stream processor beyond just a floating-point (FP) pipeline.

SPGen is composed of a front-end and a back-end. In the following subsections, we describe the SPD format, the front-end, and the back-end.

B. Stream processing description (SPD) format

Fig.5 shows an SPD example of the stream processor for Eqs.(3) to (9). Each line follows a basic format of:

- Label \( \text{item1, item2, item3} \);
- The following labels are reserved for declaration or definition:
  - Name: defines a top-module name (string).
  - Input: declares input port variables (list with comma).
  - Output: declares output port variables (list with comma).
  - Param: defines a constant FP value (parameter = value).

If a label is not reserved word, the line declares a module by being interpreted as:

- (Module name) \( \text{item1, item2, item3} \);
  - where
    - \( \text{item1} \): delay cycles of the module (integer).
    - \( \text{item2} \): module type, which is “equ” or “HDL” (string).
    - \( \text{item3} \): an equation with “=” or a module call (string).

Line 9 in Fig.5 declares an equation module “eq1” with variables \( \text{tmp}1, a, b \), and a constant \( p1 = 0.5 \). An equation needs to be in a static single assignment form, where only a single variable can be written in the left-hand side. Since a pipeline delay is unknown before module generation, the delay cycles are ignored for an equation module.

Line 13 calls HDL module “less\_than” with an instance name “lsthan.” The delay cycle has to be given for an HDL module. Here, the “less\_than” module has 1 cycle delay. An HDL module can have multiple output variables, which are specified with a variable list: \( \text{var1, var2, ...} \). The input variables are also specified with a variable list in parentheses.
All variables in SPD description are basically 32-bit words, which are treated as IEEE754 single precision FP numbers for equation modules. We can use a bit range specification with [msb:lsb] for HDL modules. The used HDL module has to be prepared in advance. Developers can write their own modules while basic modules are available in a library.

C. Front-end and back-end of SPGen

The front-end reads an SPD file and generates a DFG with nodes of modules as an intermediate expression. For the SPD description of Fig.5, such a DFG as Fig.3 is generated. The front-end parses lines one by one, and registers definitions and declarations in an intermediate data structure if a label is a reserved word. If not, a new node is created and set as an equation module or an HDL module with information of its interface definitions, referenced HDL files, and so on. The ports names of module information, interface definitions, referenced HDL files, and so on.

The back-end generates HDL files of equation modules, inserts delay modules into the DFG, and lastly outputs a Verilog-HDL code of the top module and a module configuration file. The back-end generates equation modules by using the FloPoCo tool [5] with equation descriptions. The tool generates pipelined computing modules with FP operators and a single relaxation time. This delay insertion is performed based on obtained. Then the back-end inserts delay modules into a DFG and automatically-inserted delay modules.

After generating equation modules, their delay cycles are obtained. Then the back-end inserts delay modules into a DFG as shown in Fig.6, so that all the data inputs of each modules are synchronized. This delay insertion is performed based on the cumulative delays along paths from the top-module inputs. Because of the delay insertion algorithm, currently feed-back loops are not allowed in a DFG. Modules can have an initial interval other than 1, however, developers are responsible for data synchronization in stream computation. After delay insertion, a Verilog-HDL file of the top module is generated. The back-end outputs codes for top-module declaration with input and output ports, module instances, and wires to connect the modules. Since the input and output ports of the top module include the signals of Avalon-ST interface, codes for these signals are also generated. Finally, the back-end generates a configuration file for the stream processor to be embedded into the SoC platform of Fig.1. The file contains the descriptions of module information, interface definitions, referenced HDL files, and so on.

V. APPLICATION EXAMPLE AND EVALUATION

A. HPC application example

For verification and evaluation of SPGen, we designed and implemented a stream processor for the lattice Boltzmann method (LBM) [8], [12], which is one of the methods to compute fluid dynamics. We compare it with manually implemented one in [12]. Here we summarize computations of the LBM stream processor while more details are available in [12]. LBM models fluids with propagation and collision processes of fictive particles over a discrete lattice mesh [4]. Each lattice cell has a distribution function \( f_i \) for each of the nine particle speeds \( c_i = [(\cos \pi(i - 1)/4, \sin \pi(i - 1)/4)]i = 0, 1, ..., 8 \). LBM consists of a macroscopic physical quantity calculation stage (Macro), an equilibrium calculation stage (Equi), a collision calculation stage (Col), a translation stage (Trans), and a boundary calculation stage (Bound). With these stages, \( f_i(x) \) of a lattice cell at \( x \) is updated for a single time step. Computations of these stages are given for \( i = 0, ..., 8 \) by:

\[
\rho = \sum_{i=0}^{8} f_i(x), \quad V = \frac{1}{\rho} \sum_{i=0}^{8} c_i f_i(x),
\]

\[
f^\text{eq}_i = \rho \left( A_i + B_i (c_i \cdot V) + C_i (c_i \cdot V)^2 - D_i V^2 \right),
\]

\[
f^\text{col}(x) = f_i(x) - f^\text{eq}_i(x) / \tau,
\]

where \( \rho, V = (u, v) \), and \( \tau \) are fluid density, fluid velocity, and a single relaxation time. \( A_i, B_i, C_i \) and \( D_i \) are constants for \( i = 0, 1, ..., 8 \). Macro stage computes Eqs.(6). Equi, Col, and Trans stages computes Eqs.(7), (8), (9), respectively, for \( i = 0, 1, ..., 8 \). Then, boundary conditions are applied to \( f^\text{eq}_i \) for boundary cells, which are defined with attribute flags of each cell. We can compute boundary conditions for solid surfaces or fluid-incoming/outgoing with constant pressures. Details of boundary conditions are described in [12].

B. Implementation, validation, and productivity improvement

We wrote an SPD code for the LBM stream processor to compute Eqs. (6) to (9) and the boundary conditions. Fig.7 is an excerpt of the SPD code. Input and Output define the input and the output of the stream computation, respectively. The nine inputs of “if0” to “if8” are numerical values in IEEE754 floating-point format. The input of “iAtt_RAW.x” is an attribute of each cell, which contains flags for boundary processing. Here an Input/Output port name with “_RAW” is treated as non-numerical 32-bit words, and therefore an internal floating-point format converter between IEEE754 (32 bits) and FloPoCo (34 bits) is not inserted. The ports names with “_VLD_”, “_SOP_”, and “_EOP_” are internal signals of valid, start of packet, and end of packet for Avalon-ST interface. If HDL modules in SPD description use them, the above ports have to be explicitly written, and connected to the modules. If not, they can be omitted while their input signals are automatically connected to the output ports by SPGen.

In this design, we used HDL modules of a delay module “mDelay”, a multiplexer module “mMux”, and a translation...
module “mTrans.” In the case of HDL module declaration, a parameter list for a Verilog module instance can be added such as written for “mDelay” module. For example, we can change the lattice width to be computed by the stream processor for LBM by setting the parameters to the mTrans module.

We compiled the SPD code with SPGen. Fig.8 shows the DFG of the generated processor. The circles are the equation modules while the rectangulars are delay modules automatically inserted by SPGen. We embedded the stream processor into the top modules of the LBM stages required seven files, which totally contain 2720 lines. This means that the SPD format reduced the lines to only 83 lines for SPGen. For development of the hand-designed PE, we spent several months for the conventional design flow. On the other hand, it took only one or a few days to write and debug the SPD code, and run the design on FPGA. Although we cannot say that this is complete comparison for quantitative evaluation of productivity, these results show some of productivity improvement by SPGen. Consequently, we could optimize the equations of LBM by removing some redundant operations in the SPD code.

The LBM stream processor generated by SPGen has the same computing performance as that of the hand-designed one. Since the pipelining overhead for epilogue and prologue is ignorable for sufficiently large lattice data, we can obtain the sustained performance by multiplying an operating frequency F with the number of FP operations per cycle N_opc. In our system, F = 125 MHz and N_opc = 131 for 70 adders, 60 multipliers, and 1 divider in the stream processor. As a result, the sustained performance is FN_opc = 16.4 GFlops. Since at most three stream processors fit the Stratix IV FPGA, expected maximum performance is 16.4 × 3 = 49.2 GFlops.

![Fig. 7. SPD code of the stream processor for LBM (excerpt of original 83 lines without empty or comment lines).](image)

![Fig. 8. SPGen compiled results: DFG of the stream processor for LBM.](image)

![Fig. 9. Computed 2D sudden-expansion channel flow with a solid circle.](image)
TABLE I. RESOURCE CONSUMPTION FOR TARGET FREQUENCIES OF 125, 250, AND 500MHZ, AND COMPARISON WITH THE DESIGN BY HAND [12].

| Target frequency | Module     | Combinational LUTs | Registers | Block memory Kbits | 36-bit DSPs |
|------------------|------------|--------------------|-----------|-------------------|-------------|
|                  |            | %                  | %         | %                 | %           |
| 125 MHz          | Peripherals| 42758              | 23.4      | 43491             | 19.2        |
|                  | Stream processor | 44693              | 24.5      | 20745             | 11.4        |
| 250 MHz          | Peripherals| 42868              | 23.5      | 43525             | 23.9        |
|                  | Stream processor | 35411              | 19.4      | 33533             | 18.4        |
| 500 MHz          | Peripherals| 42931              | 23.5      | 42692             | 23.4        |
|                  | Stream processor | 45284              | 24.8      | 56001             | 30.7        |
| Design by hand   | Peripherals| 37942              | 20.8      | 41316             | 22.7        |
|                  | LBM PE     | 46889              | 25.7      | 38117             | 20.9        |

C. Resource consumption and design space exploration

By changing the number of pipeline stages of a stream processor with different target frequencies for the FloPoCo tool, we explore the design space to find one for minimum resource consumption. Table I shows the resource consumption for target frequencies of 125MHz, 250MHz, and 500MHz. “Peripherals” are for PCI-Express core, two DDR2 memory controllers, and four DMA cores. Here no microprocessor is implemented. The table shows that the higher frequency requires more registers for increased pipeline stages. Simultaneously, the higher frequency also consumes more block memory bits because more delays are inserted for a more deeply pipelined DFG. On the other hand, the target frequency of 250MHz gives the smallest number of LUTs against our expectations. This is because the FloPoCo tool uses smaller FP operators for the 250 MHz design. In any case, SPGen allows us to easily find the best design from pipelining choices.

We also compare resource consumption with the hand-designed PE, which is functionally identical. As seen in Table I, The 250MHz design has smaller consumption especially for LUTs and DSPs. Less LUTs are achieved mainly by the equation optimization where redundant operators are removed in the SPD code. Less DSP blocks are due to constant multipliers. In the hand-designed PE, we store parameters in registers to be read and computed. Therefore normal multipliers are generated for them. On the other hand, we use constant parameters directly in the SPD code, and change them when necessary. This is because SPGen allows us quick modification and synthesis of the design. As a result, many multipliers are generated as constant ones with smaller logics.

VI. CONCLUSIONS

This paper presents SPGen, a stream processor generator, which is based on the stream computing model and aims at assisting developers to design and implement high-throughput reconfigurable stream processor on an FPGA-based common SoC platform. We define a domain-specific description format, SPD, to easily define stream computation with equations and module calls. SPGen allows us to focus on designing stream algorithms and explore design space for different equations and frequencies. We demonstrate and validate SPGen and the SPD format with fluid dynamics computation based on LBM. SPGen reduces a development time from months to a few days. The generated stream processor works completely, and its performance and resource consumption are comparable to or better than those of the hand-designed one.

In our future work, we will evaluate SPGen with other applications of high-performance or embedded computation.

We will extend SPGen to version 2.0 so that it can generate a stream processor with interfaces for inter-processor communication other than data streaming.

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