Design of an Enhanced Reconfigurable Chaotic Oscillator using G⁴FET-NDR Based Discrete Map

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Abstract—In this paper, a novel chaotic map is introduced using a voltage controlled negative differential resistance (NDR) circuit composed of an n-channel and a p-channel silicon-on-insulator (SOI) four-gate transistor (G⁴FET). The multiple gates of the G⁴FET are leveraged to create a discrete chaotic map with three bifurcation parameters. The three tunable parameters are the gain of a transimpedance amplifier (TIA), top-gate voltage of p-channel and a voltage controlled negative differential resistance (VC-NDR) circuit consisting of two G⁴FETs and a transimpedance amplifier is used to build a novel chaotic map with three bifurcation parameters. Two methods are proposed for building chaotic oscillators using this discrete map. The effect of altering bifurcation parameters on chaotic operation is illustrated using bifurcation diagrams and Lyapunov exponent. A design methodology for building flexible and reconfigurable logic gate is outlined and the consequent enhancement in functionality space caused by the existence of three independent bifurcation parameters is demonstrated and compared with previous work.

Index Terms—Nonlinear dynamics, discrete chaotic map, chaos computing, SOI, G⁴FET, VLSI, NDR, hardware security

I. INTRODUCTION

As technology scaling has slowed down over the past decade, it has become increasingly difficult to integrate more transistors in a given area. Researchers are looking into new approaches to attain better performance without increasing the number of transistors. A possible solution is increasing the number of computations that a device can perform using chaotic operation [1]. The rich inherent dynamics of the chaotic circuits have been studied by researchers to build flexible and reconfigurable digital gates [2]. On the other hand, G⁴FET, a silicon-on-insulator (SOI) device with four independent gates, is also a promising candidate for accomplishing this goal since it has been used in various analog and digital applications with reduced transistor counts [3], [4]. In this work, we propose a scheme to combine the advantages of a multi-gate transistor with the large functionality space of chaotic circuits.

Traditional discrete chaotic maps such as logistic, tent, sine map, etc. are idealized mathematical functions that require a significant number of transistors for hardware implementation. In order to reduce the hardware cost, researchers have made an effort to come up with simpler transistor-level discrete maps with good chaotic properties [1], [5]. Recently, researchers have been exploring how to leverage the large functionality space provided by these discrete map chaotic circuits for security applications [6], [7]. Most chaotic maps have only one bifurcation parameter where the space is extended by increasing the number of iterations. However, due to the system’s susceptibility to noise, the reliability decreases with an increase in the number of iterations. Hence, it is highly desirable to develop a chaotic map with multiple independent control parameters which can reliably expand the functionality space with fewer number of iterations and relatively simple hardware implementation.

In this work, a voltage controlled negative differential resistance (VC-NDR) circuit consisting of two G⁴FETs and a transimpedance amplifier is used to build a novel chaotic map with three bifurcation parameters. Then two methods are proposed for building chaotic oscillators using this discrete map. The excellent property of the chaotic map is illustrated with the help of bifurcation diagram and Lyapunov exponent which are plotted for different values of control parameters. It is also shown that the availability of three independent bifurcation parameters can be used to exponentially increase the functionality space.

The paper is organized as follows: Section II introduces the proposed chaotic map built with G⁴FET NDR circuit. Section III elaborates on the design of chaotic oscillator and shows the resulting bifurcation diagrams and Lyapunov exponent. A methodology for generating logic functions from chaotic oscillator is shown in section IV and the resulting enhancement in design space are explored in section V. Finally, section VI concludes the paper.

II. PROPOSED CHAOTIC MAP USING G⁴NDR

A. G⁴FET

G⁴FET is a multigate SOI device [8] that is a potential candidate for designing innovative circuits with more functions and fewer transistors [3], [4]. It can be fabricated in partially/fully-depleted SOI process and the channel conductance can be modulated using four independent gates [9]. A conventional p-channel SOI MOSFET with two body contacts on the opposite sides of the channel can be converted into an n-channel G⁴FET. The structure and circuit symbol of an n-channel G⁴FET is shown in Fig. 1. The p+ doped source and drain of the traditional MOSFET now operate as junction gates. The function of the two lateral gates is similar to JFET gates and can be used to control the channel width. The operation of the top gate is
Fig. 1: a) 3-D device structure of an \( n \)-channel G\(^4\)FET, b) circuit symbol.

Fig. 2: Tunable NDR circuit using \( n \)- and \( p \)-channel G\(^4\)FET; (a) circuit schematic, (b) simplified symbol.

similar to the conventional MOS gate and the substrate is biased using the buried oxide layer which works as the bottom gate. The conductance of G\(^4\)FET is controlled by two MOSFET and two JFET gates that are biased independently. In this work, the bottom gates are grounded and not shown in the subsequent figures for simplicity.

B. G\(^4\)FET NDR

A tunable VC-NDR circuit using complementary G\(^4\)FETs was first proposed and experimentally verified in [3]. The G\(^4\)FET NDR is developed by substituting complementary JFETs with G\(^4\)FETs in a conventional lambda diode [10]. The schematic and simplified symbol are shown in Fig. 2 where both junction-gates of G\(^4\)FET are tied together and treated as a single gate. The G\(^4\)FET NDR is a four-terminal device where the additional two-terminals are the top-gates of the \( n \)- and \( p \)-channel G\(^4\)FETs and denoted by voltages \( V_N \) and \( V_P \), respectively. The dimensions of \( p \)- and \( n \)-channel G\(^4\)FET in this work are 0.35 \( \mu m \) / 1.2 \( \mu m \) and 0.35 \( \mu m \) / 3.4 \( \mu m \) respectively. All results are generated using the MOS-JFET macromodel [11].

C. G\(^4\)NDR Based Chaotic Map (GNM)

If a non-linear function, \( f \) transforms any point \( x_n \) from a closed interval \( l = [a, b] \) into some point \( x_{n+1} \) in the same interval i.e. \( f : l \rightarrow l \), then

\[
x_{n+1} = f(x_n)
\]

is called a discrete map of the interval \( l \) for \( n = 1, 2, ..., n \). Fig. 3 shows a schematic and a symbol of the chaotic map based on VC-NDR using complementary G\(^4\)FETs. When the resulting current is converted to voltage using a transimpedance amplifier (TIA) with a variable gain, \( R (\mu_1) \), we get a map circuit with transfer characteristic similar to a logistic map. However, common map functions (logistic, tent, sine etc.) are idealized mathematical functions which are expensive to implement in hardware and they provide only one bifurcation parameter. In contrast, the proposed chaotic map has three independently controllable bifurcation parameters. The transfer curve for the proposed chaotic map is shown in Fig. 4 where \( \mu_2 \) and \( \mu_3 \) are set at 0 V and \( \mu_1 \) is varied from 0 to 1 M\( \Omega \). The transfer curve displays differentiable unimodal characteristic which is suitable for chaotic operation.

III. CHAOTIC OSCILLATOR

The chaotic oscillator in Fig. 5a is made using the G\(^4\)FET NDR-based chaotic map (GNM), two sample-and-hold circuits

Fig. 3: G\(^4\)FET NDR based map (GNM) circuit with three bifurcation parameters; (a) circuit schematic, (b) simplified symbol.

Fig. 4: Transfer curve of the nonlinear map circuit.

Fig. 5: Chaotic oscillator using G\(^4\)FET NDR based chaotic map (GNM); a) feedback using buffer, b) feedback using another GNM instead of the buffer.
Fig. 6: (a) Bifurcation diagram and (b) Lyapunov exponent of the chaotic oscillator for varying $\mu_1; \mu_2 = 0 \text{ V}, \mu_3 = 0 \text{ V}$.

and a buffer. In Fig. 5b, we propose another design where the buffer in the feedback loop is replaced with another map. The initial input is applied to the oscillator using clock $\phi_3$. After the initial input has been applied, $\phi_3$ stops and the first output is fed back to the input using two complementary switches $\phi_1$ and $\phi_2$. The next output states are generated by alternating the on and off condition of the switches $\phi_1$ and $\phi_2$. When the system is in the chaotic region, a new analog voltage is generated at each iteration.

Lyapunov exponent, $\lambda$ is used to quantify the sensitive dependence of the chaotic oscillator on initial conditions. Positive values of $\lambda$ indicate chaotic operation whereas negative values imply periodic operation. For discrete-time chaotic maps, it is defined as,

$$\lambda = \lim_{n \to \infty} \frac{1}{n} \sum_{i=0}^{n-1} \ln |f'(x_i)|.$$  

The parameters, $\mu_1$, $\mu_2$ and $\mu_3$ control the behavior of the nonlinear dynamic system which is shown in the bifurcation diagrams Figs. 6a, 7a and 8a. In Fig. 6a, the steady-state output is plotted for varying $\mu_1$ while keeping $\mu_2$ and $\mu_3$ constant. The first 1000 iterations are ignored and the next 3000 iterations are plotted. We can clearly see the period-doubling phenomenon and chaotic regions. Similarly, Figs. 7a and 8a show the effect of $\mu_2$ and $\mu_3$, respectively while keeping the other two parameters constant. The corresponding Lyapunov exponents are shown in Figs. 6b, 7b and 8b. As can be seen from these figures, a positive value of Lyapunov exponent corresponds to a chaotic region whereas a negative value corresponds to non-chaotic (fixed/periodic) operating region.

Fig. 7: (a) Bifurcation diagram and (b) Lyapunov exponent of the chaotic oscillator for varying $\mu_2; \mu_1 = 1 \text{ M}\Omega, \mu_3 = 0 \text{ V}$.

Fig. 8: (a) Bifurcation diagram and (b) Lyapunov exponent of the chaotic oscillator for varying $\mu_3; \mu_1 = 1 \text{ M}\Omega, \mu_2 = 0 \text{ V}$.
TABLE I: Evolution of chaotic gate with different iterations ($\mu_1 = 0.95\; M\Omega, \mu_2 = 0\; V, \mu_3 = 0\; V, C_b = 0, V_{ref} = 1.25\; V$). Functions represented in decimal value.

| $x_n$(V) | $n = 1$ | $n = 2$ | $n = 3$ | $n = 4$ | $n = 5$ |
|----------|---------|---------|---------|---------|---------|
| 0.1(00)  | 0.46(0) | 1.02(1) | 1.34(0) | 1.89(1) | 0.34(0) |
| 0.757(01) | 1.98(1) | 0.23(0) | 1.93(0) | 2.43(1) | 0.36(0) |
| 1.314(10) | 1.01(0) | 1.86(1) | 0.34(0) | 1.83(1) | 1.20(0) |
| 2.071(11) | 0.19(0) | 0.82(0) | 1.98(1) | 0.24(0) | 1.01(0) |

**Func (dec)** | 4 | 10 | 1 (AND) | 14 (NAND) | 0 |

**IV. LOGIC FUNCTION GENERATION FROM Chaotic Oscillator**

The proposed chaotic oscillators can be used to build reconfigurable logic gates. A schematic for the logic gate is shown in Fig. 2. A digital-to-analog converter (DAC) converts the digital input bits to analog value which is used as the seed value ($x_0$) for chaotic oscillator. In order to enhance the design space, a control bus, $C_b$ is used along with the data bus, $I_b$. After each iteration, the analog output voltage is converted to digital voltage by using a comparator with a reference voltage, $V_{ref}$. The digital conversion is done using the following equation:

$$O_n = \begin{cases} 1, & \text{if } x_n > V_{ref} \\ 0, & \text{otherwise.} \end{cases}$$  

(3)

In this work, 2-input chaos-based digital gates along with 1 control bit is used. A 3-bit DAC is required for converting the digital input to analog voltage. The reconfigurable chaos-based logic gate can implement 16 different functions which are numbered in decimal starting from 0 (00000) to 15 (11111). Table II demonstrates the evolution of analog voltages with different iterations. The values of the control parameters are $\mu_1 = 0.95\; M\Omega, \mu_2 = 0\; V, \mu_3 = 0\; V, C_b = 0$ and $V_{ref} = 1.25\; V$. The functions vary with each iteration and they are represented in decimal format e.g. AND and NAND are represented by 1(0001) and 14(1110), respectively. As shown in Fig. 5, multiple configurations for implementing basic logic gates, enabled by nonlinear dynamics, can lead to obfuscation against power side channel attack. The proposed design can also be leveraged for the same goal. Three different configurations, distinguished by different combination of ($\mu_2, \mu_3$) are shown in Table II for implementing six common functions (AND, OR, XOR, NAND, NOR and XNOR). This design methodology is flexible i.e. the same logic function can be implemented in many different ways as well as reconfigurable i.e. the same circuit can be reconfigured to implement all the possible functions.

**V. ENHANCEMENT OF THE FUNCTIONALITY SPACE**

In this work we propose two new designs of chaotic oscillators (Fig. 5) which provide a significant increase in functionality space compared to existing works. In [12], there are three tuning parameters, bifurcation parameter ($\mu$), control bit ($C_b$) and number of iterations ($n$). Let, $N_{\mu}$ be the number of available levels in the chaotic region and $c$ is the number of control bits. The functionality space, $F(n)$ in the design can be written as,

$$F_1(n) = 2^c \times N_{\mu} \times n$$  

(4)

In [13], threshold is varied but control bit is not used. The bifurcation parameter was changed in each iteration to extend the functionality space. If we express $N_{v_{ref}}$ as the number of comparator reference voltage levels, the functionality space can be written as,

$$F_2(n) = N_{v_{ref}} \times N_{n} \times n$$  

(5)

In this work, we propose two new designs. For design 1, we use chaotic oscillator 1 from Fig. 5a with one chaotic map. There are six tunable parameters in this design: control bits ($C_b$), bifurcation parameters ($\mu_1, \mu_2$ and $\mu_3$), iteration number ($n$) and reference voltage ($V_{ref}$). If we allow the bifurcation parameter to change from iteration to iteration, the resulting functionality space can be written as,

$$F_3(n) = N_{v_{ref}} \times 2^c \times N_{\mu_1} \times N_{\mu_2} \times N_{\mu_3} \times n$$  

(6)

We can further extend the functionality space by using chaotic oscillator 2 from Fig. 5b. In this case, each of the forward path map and feedback path map has three independent bifurcation parameters and the functionality space can be written as,

$$F_4(n) = N_{v_{ref}} \times 2^c \times N_{\mu_1}^2 \times N_{\mu_2}^2 \times N_{\mu_3}^2 \times n$$  

(7)

The functionality spaces for equations (4)-(7) are shown in Fig. 10. This clearly shows that the functionality space of the proposed design is significantly larger compared to existing designs [12], [13] due to multiple bifurcation parameters. It should be noted that there are two more gates (bottom gates of $n$- and $p$-channel G$^2$FETs) that can also be used to further extend the design space.

The nonlinear dynamics inherent in a chaos-based design enables developing complex (e.g. multi-input, multi-output)
TABLE II: Three different configurations for six logic functions.

| Operation | Configuration 1 | Configuration 2 | Configuration 3 |
|-----------|-----------------|-----------------|-----------------|
| \( \mu \) | \( \mu_1(V_{REF}) \) | \( \mu_2(V_{REF}) \) | \( \mu_3(V_{REF}) \) |
| AND | 0.99 | 0 | 1 | 1.1 | 3 |
| OR | 0.99 | 0 | 1 | 1.6 | 0.3 |
| XOR | 0.99 | 0 | 0 | 0.6 | 4 |
| NAND | 0.99 | 0 | 0 | 0 | 6 |
| NOR | 0.99 | 0 | 1 | 0.6 | 6 |
| XNOR | 0.99 | 0 | 1 | 1.6 | 6 |

logic gates using the same circuit \([7]\). The possible functions for an \(n\)-input logic gate is \(2^n\). Hence, a 3-input gate will have 256 possible functions. For obfuscation applications, it is highly desirable to have a large functionality space so that multiple reliable configurations can be chosen for implementing a single function. This can be leveraged to ensure the security of chaos-based computing systems against side-channel power analysis based attacks \([7, 14]\). Previously, this was achieved using many iterations but this poses a problem since the resulting gate becomes increasingly unreliable. As shown in Fig. [10], the proposed design can achieve a very large functionality space using very few iterations.

Though a single chaos-gate has a larger overhead compared to conventional CMOS gates, this kind of multi-input arbitrary logic function can dramatically reduce the overhead of the overall design. For example, let’s consider a three input one output function, \( Y = ABC + \overline{AB}C + \overline{A}BC + \overline{A} \overline{B}C \). If we only use two-input logic gates, we have to use 14 gates whereas a single three-input one-output chaos gate can implement the same function. This approach can significantly reduce the overhead for implementing complex logic functions. Moreover, as shown in \([14]\), oftentimes we only have to replace a small percentage of total gates with chaos-based implementation to benefit from the resulting security advantages.

VI. CONCLUSION

In this paper, a novel nonlinear chaotic map circuit is introduced using a negative differential resistance circuit made of two complementary SOI four-gate transistors. Two novel chaotic oscillator designs are proposed and the resulting periodic and chaotic regions are demonstrated using bifurcation diagrams and Lyapunov exponent. A methodology for designing flexible and reconfigurable logic gate is outlined and three representative configurations for implementing basic logic gates are shown. Compared to earlier works, significant enhancements in functionality space have been demonstrated. The proposed designs can be utilized to reduce hardware overhead by reliably implementing complex logic functions. The enhanced space can be utilized for mitigating multiple hardware security problems.

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