On-CMOS High-Throughput Multi-Modal Amperometric DNA Analysis with Distributed Thermal Regulation

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Abstract—Accurate temperature regulation is critical for amperometric DNA analysis to achieve high fidelity, reliability, and throughput. In this work, a 9 × 6 cell array of mixed-signal CMOS distributed temperature regulators for on-CMOS multi-modal amperometric DNA analysis is presented. Three DNA analysis methods are supported, including constant potential amperometry (CPA), cyclic voltammetry (CV), and impedance spectroscopy (IS). In-cell heating and temperature sensing elements are implemented in standard CMOS technology without post-processing. Using proportional-integral-derivative (PID) control, the local temperature can be regulated to within ±0.5°C of any desired value between 20°C and 90°C. The two computationally intensive operations in the PID algorithm, multiplication, and subtraction, are performed by an in-cell dual-slope multiplying ADC in the mixed-signal domain, resulting in a small area and low power consumption. Over 95% of the circuit blocks are synergistically shared among the four operating modes, including CPA, CV, IS, and the proposed temperature regulation mode. A 3mm × 3mm CMOS prototype fabricated in a 0.13μm CMOS technology has been fully experimentally characterized. Each channel occupies an area of 0.06mm² and consumes 42μW from a 1.2V supply. The proposed distributed temperature regulation design and the mixed-signal PID implementation can be applied to a wide range of sensory and other applications.

Index Terms—Temperature regulation, mixed-signal IC, PID control, on-CMOS DNA analysis, circuit sharing

I. INTRODUCTION

Conventional optical DNA analysis methods typically require sample flushing, thus cannot be implemented in real-time [1]. Amperometric electrochemical DNA analysis supports real-time operation [2]. Recently, several CMOS system-on-chip (SoC) designs for amperometric electrochemical DNA analysis have been developed [3]–[7], [9]–[11]. On-CMOS DNA analysis permits advantageous high-density, low-noise, low-cost monolithic integration of various modules for sensing, signal processing, communication, and power management [8]. Fig. 1 illustrates the operating principles of amperometric DNA analysis. First, the surface of the working electrode (WE) is functionalized with probe DNA [3]. Then, a voltage is applied between the reference electrode (RE) and the WE. The voltage waveform is set to be a constant voltage for constant potential amperometry (CPA), a bidirectional ramp for cyclic voltammetry (CV), and a sinusoid for impedance spectroscopy (IS). The hybridization of the probe DNA with the target DNA alters the surface properties of the WE, such as the impedance or the surface charges. This variation will result in a waveform change of the redox current that indicates the kinetics and thermodynamics of the chemical reactions [12].

Temperature is a key constraint in all DNA analysis methods. Studies have shown that DNA hybridization is highly dependent on the temperature [13]–[15]. For a temperature increase of 10°C, the redox current will drop approximately by 10% [15]. Additionally, time-varying temperature control in the range of 20°C to 90°C is required for DNA multiplication through polymerase chain reaction (PCR). Therefore, a temperature regulation system is of great benefit for DNA sensing applications. In practice, off-array CMOS processing modules often cause temperature variation across the DNA analysis array, and do not scale well to large sensing arrays. Thus, distributed in-channel temperature sensing and regulation are necessary. In addition, a channel-level thermal regulation scheme permits the generation of spatial temperature gradients for advanced non-uniform DNA analysis [16], [17].

Several temperature regulation designs for chemical sensing applications have been reported [4], [6], [7], [9], [18]–[20]. These designs typically use resistive heating and sensing elements. Paper [18] presents a temperature sensing and reg-
Fig. 2. Four modes of operation of the proposed multi-modal DNA analysis SoC. (a) CPA configuration [27], (b) CV configuration [26], (c) IS configuration [28], and (d) temperature regulation configuration (the focus of this work). The blocks with a thick outline and highlighted in light green are synergistically shared in all modes, with over 95% of all area reused in each operating mode.

ulation microsystem for biological applications that achieves a single fixed temperature of 37°C on the backside of the chip, with an off-chip digital proportional-integral-derivative (PID) controller. Paper [19] presents a 3×3 micro-hotplate array for a protein-sensing application. In this design, the temperature of the chip is regulated up to 45°C with an off-chip digital PID controller. Paper [4] presents a 16-channel, frequency-shift CMOS magnetic biosensor array for a protein-sensing application. This design consists of an array of in-channel heaters, with a single temperature sensor and an off-chip analog PID controller. Paper [20] presents a digital CMOS micro-hotplate array architecture for a gas-sensing application. The array consists of 3×3 gas-sensing sites. Each site consists of a heater, a temperature sensor, and a delta-sigma modulated PID controller. The micro-hotplate achieves an operating temperature of up to 350°C. A 40-channel DNA analysis SoC based on ISFET sensors for rapid point-of-care DNA detection is reported in [5]. This design includes in-channel heaters, temperature sensing elements, and a dedicated ADC. A fully digital on-chip PID controller is utilized for temperature regulation. In summary, most existing closed-loop temperature regulation microsystems use off-chip controllers, with few exceptions [5], [7]. Conventional on-chip controller designs often require a large silicon area along with high power consumption, which is prohibitive for most on-chip electrochemical sensing applications.

In this work, we present a compact, distributed temperature regulator design implemented in 0.13µm standard CMOS technology. Fig. 1 depicts the block diagram of the proposed temperature-regulated electrochemical cell. It consists of a temperature sensor, a heater, a closed-loop regulator, a working electrode, a reference electrode, and a potentiostat. We chose the PID algorithm for the closed-loop regulation because of its high efficacy in temperature control systems [21], [22]. PID controllers have been implemented on-chip in analog [23], [24] and digital domains [25]. Here we introduced a novel mixed-signal design that yields a compact integration with low power dissipation. This design permits distributed temperature regulation in large-scale parallel sensing applications.

The presented temperature controller is a part of a highly-

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integrated multi-functional SoC that performs on-chip amperometric electrochemical DNA analysis. The overall SoC consists of 54 sensing channels with 600 gold microelectrodes. It performs label-free DNA analysis and pH sensing for prostate cancer detection. During the design, we synergistically share the circuits among different operation modes to achieve high integration and low resource overhead. We have previously reported on the cyclic voltammetry DNA sensing modality in [26]. We briefly discussed how the DNA sensing and the temperature control circuits are integrated in [27]. The impedance modality was introduced by us in [28]. In this paper, we presented a unified review of how all of these sensing modalities are implemented on the same IC with minimal overhead, and focus on presenting the details of the distributed mixed-signal temperature regulator, including the system architecture, algorithm design, circuit implementation, and experimental results. To the best of our knowledge, this work presents the first distributed temperature regulation design with on-chip PID control for DNA analysis. This design permits an accurate thermal control for compensating the temperature variation across the DNA analysis array while potentially enabling advanced temperature gradient generation. We developed a new way of implementing PID control using mixed-signal circuits (e.g., multiplying ADC), which avoids the computationally intensive multiplications of the PID algorithm in the digital domain, rendering compact silicon area and low power consumption. The proposed design is required for the three sensory modalities: CPA, CA, and IS, and reuses over 95% of their circuit implementation. It can be used in a wide range of applications beyond DNA analysis, including lab-on-chip designs, in-vitro systems, and implantable medical devices (e.g., retinal prosthesis array).

The rest of the paper is organized as follows. Section II overviews the multi-modal DNA analysis SoC. Section III provides background on temperature regulation principles. Section IV presents the VLSI architecture of the temperature controller. Section V details the circuit implementation. Section VI shows the experimental results obtained from the fabricated 0.13 μm CMOS prototype. Finally, Section VII concludes the paper.

II. Multi-modal DNA Analysis SoC with Synergistic Circuit Sharing

Fig. 2 shows an overview of the presented multi-modal DNA analysis SoC, which can be configured to perform CPA (Fig. 2(a) [27]), CV (Fig. 2(b) [26]), IS (Fig. 2(c) [28]), and temperature regulation (Fig. 2(d)).

The SoC includes a 9 × 6 array of low-power low-noise sensory circuit cells, a programmable waveform generator, on-chip SRAM memories, a shared PID controller, a digital PWM, an all-digital ultra-wideband (UWB) transmitter, and on-chip biasing and clock generation circuits. Each sensory cell includes a current-to-digital conversion channel, an array of DNA sensors, a pH sensor, several BJTs to generate the CTAT and PTAT currents, and a heater for temperature regulation. Each cell also integrates a bias voltage generator, clock generation circuitry, and SRAM memory that can be programmed individually.

Each current-to-digital conversion channel consists of either a transimpedance amplifier (TIA) or a current conveyor (CC) and a dual-slope multiplying ADC (MADC). The dual-slope MADC multiplies the sensor’s response with a set of digital coefficients, and outputs the corresponding digital word. The digital output of each channel is serialized on the chip and then wirelessly transmitted using the all-digital UWB transmitter [26].

The SoC reuses a number of blocks (denoted by bold outlines and light green color in Fig. 2) in different configurations. The circuit sharing design yields a significant saving in the integration area. Specifically, the circuits that occupy 95% of the in-cell area are shared with other modes of operation. For completeness, all key functionalities of the SoC are summarized in this section. For the detailed implementation of the CPA, CV and IS, please refer to our previous publications in [27], [26] and [28], respectively.

A. Constant Potential Amperometry (CPA) Mode

Fig. 2(a) shows the functional blocks for pH sensing using CPA analysis. Sensing pH is required as a part of DNA analysis. The in-channel pH sensor is implemented by a floating gate PFET, with the gate connected to the top metal layer for forming a floating gate electrode. The CMOS passivation layer is used as the pH-sensitive membrane, which gives a linear pH response with a sensitivity of about 56mV/pH, depending on the stoichiometry. The pH sensors are directly interfaced to the current recording channels, with gate voltage set by the on-chip reference electrode. In this configuration, both Vgs and Vds of the pH sensors are fixed. Changes in the pH level will affect the PMOS threshold voltage, resulting in the changes in the drain current, which is digitized by the recording channel. The chip temperature needs to be held at a constant value within ±0.5°C.

B. Cyclic Voltammetry (CV) Mode

Fig. 2(b) shows the functional blocks for CV analysis. In this mode, each channel is multiplexed among a bank of in-cell DNA sensors. The sensors are interrogated by the on-chip programmable waveform generator that is shared among all cells. The CC front-end is utilized in this configuration. The digital data representing the stimulation waveform properties are stored in the on-chip SRAM. The current-to-digital channel quantizes the input current and outputs the corresponding digital word. No computation is required in this case and the MADC digital multiplication coefficients are set to one. The chip temperature is held at a constant value within ±0.5°C.

C. Impedance Spectroscopy (IS) Mode

Fig. 2(c) shows the functional blocks for IS analysis. In this mode, a frequency response analysis (FRA) algorithm is used to extract the real and imaginary components of the biosensor impedance [28]. The computationally intensive operations required by the FRA algorithm are performed by the in-channel MADC in the mixed-signal domain. The waveform generator produces a variable frequency sinusoidal...
interrogation waveform for driving the reference electrode, and front-end TIA acquires the DNA sensor’s response. The MADC multiplies the sensor’s response with a set of digital FRA algorithm coefficients (stored in the multiplication coefficient SRAM). Next, the MADC accumulates the results over one period of the interrogation signal (integration) for extracting the impedance. In this mode, the cell temperature is held constant within ±0.5°C.

D. Temperature Regulation Mode

It is clear that each of the three sensory modes requires accurate temperature control. Thus, the temperature regulation function is the main focus of this paper. Fig. 2(d) shows the functional blocks. In this mode, the SoC utilizes the current-to-digital channels to measure temperature. The on-chip SRAMs are utilized to store PID coefficients and multiplication coefficients. The channel measures temperature by taking the ratio of a CTAT to PTAT currents as described in Section II. The measured temperature is fed to the on-chip PID controller. The PID controller regulates the 2D chip temperature profile by modulating the in-cell heaters. The multiplication and subtraction operations required by the PID algorithm are performed by the in-channel MADC in the mixed-signal domain, yielding a small silicon area and low power consumption.

III. TEMPERATURE CONTROL PRINCIPLES

A. Temperature regulation

The block diagram of the temperature regulation loop is shown in Fig. 4. It consists of a heater, a temperature sensor, a PID controller, and an actuator. The actuator uses digital pulse-width modulation (PWM) for controlling the heater.

![Block diagram of the PID control of the temperature regulation loop.](image)

The continuous-time representation of a PID controller is given by

\[
u(t) = K_p e(t) + K_i \int_0^t e(t) dt + K_d \frac{d}{dt} e(t) \tag{1}\]

where \(K_p\) is the proportional gain, \(K_i\) is the integral gain, \(K_d\) is the derivative gain, \(e(t)\) is the error value, and \(u(t)\) is the actuation value. A discrete-time representation of (1) in Z-domain is given by

\[
D(z) = \frac{u(z)}{e(z)} = K_p + K_i \frac{T_s}{2} z + 1 + K_d \frac{z - 1}{T_s} \tag{2}\]

where \(T_s\) is the sampling period. Eq. (2) can be implemented numerically as follows

\[
u(k) = u(k - 1) + c_0 e(k) + c_1 e(k - 1) + c_2 e(k - 2) \tag{3}\]

where \(k\) is the discrete time index, and \(c_0\), \(c_1\), and \(c_2\) are the PID control coefficients.

During the operation, the PID controller calculates the error value \(e(k)\) and attempts to minimize it by adjusting \(u(k)\), which sets the PWM duty cycle of the actuator.

B. Temperature sensing

Temperature can be measured by taking the ratio of two signals that are linearly dependent on it. In CMOS technologies, these signals can be derived from the base-emitter voltage of substrate pnp transistors [29]. These transistors use the p-substrate as the collector, the p⁺-diffusion as the emitter, and an N-well as the base. Fig. 3(a) shows the generation of two linearly temperature dependent signals. One is generated from the base-emitter voltage \(V_{BE}\) of a single pnp transistor, the other is generated from the difference between the base-emitter voltages \(\Delta V_{BE}\) of two pnp transistors biased at different collector current levels.

The temperature dependence of the \(V_{BE}\) can be derived from the exponential relation between the collector current \(I_C\) and the base-emitter voltage as follows.

\[
V_{BE}(T) = V_{g0}(1 - \frac{T}{T_r}) + \frac{T}{T_r} V_{BE} T_r - n \frac{KT}{q} \ln \frac{T}{T_r} + \frac{KT}{q} \ln \frac{I_C T}{I_T} \tag{4}\]

where \(V_{g0}\) is the extrapolated bandgap voltage at 0 Kelvin, \(n\) is a process-dependent constant, \(K\) is Boltzmann constant, \(q\) is the electron charge, and \(T_r\) is an arbitrary reference temperature [30]. As illustrated in Fig. 3(b), \(V_{BE}\) is complementary to absolute temperature (CTAT) with a typical slope of -2 mV/K. The nonlinearity is represented by the last two terms of (4), which is negligible in the temperature range of 20°C to 90°C required by DNA analysis.

The slope of the base-emitter voltage depends on the absolute value of the collector current. This dependence can
be used to generate a voltage that is proportional to absolute temperature (PTAT). The difference between the base-emitter voltages of two pnp transistors biased at two different collector currents can be expressed as follows

\[ \Delta V_{BE}(T) = V_{BE2}(T) - V_{BE1}(T) \]
\[ = \frac{KT}{q} \ln \left( \frac{I_{C2}}{I_{C1}} \right) \]

where \( I_{C1} \) and \( I_{C2} \) are the collector currents of the two pnp transistors.

Conventional temperature sensors measure the ratio of the PTAT signal to a temperature-independent reference signal. The temperature-independent reference signal can be generated by adding \( V_{BE} \) to a scaled version of \( \Delta V_{BE} \) \[29\]–\[33\]. The scaling factor \( \alpha \) is used to match the temperature dependence (with an opposite sign) of \( V_{BE} \) and \( \Delta V_{BE} \). However, the generation of the temperature-independent reference signal adds complexity to the circuit implementation, which is not suitable for a channel-level implementation. Although distributing a global temperature-independent signal is feasible, it places challenges in the signal routing if a voltage signal is used, and requires accurate matching or time multiplexing if a current signal is used. In this work, we eliminate these issues by directly taking the ratio of PTAT and CTAT signals, which have an approximately linear relationship with temperature within the range of 20°C to 90°C. The PTAT and CTAT voltages are converted to currents using resistors \( R_1 \) and \( R_2 \). The \( \alpha \Delta V_{BE}/R_2 \) is used as the reference the dual-slope MADC and the \( V_{BE}/R_1 \) is used as the input signal, as illustrated in Fig. 3(e). As a result, the dual-slope MADC inherently digitizes the ratio of \( \alpha \Delta V_{BE}/R_2 \) to \( V_{BE}/R_1 \) \[20\]. The digitized output number represents the temperature. The factor \( \alpha \), the resistance \( R_1 \) and \( R_2 \) are set such that both the input and the reference currents utilize the full dynamic range of the channel over the operating temperature range.

IV. VLSI ARCHITECTURE

The top-level VLSI architecture of the temperature regulation loop is shown in Fig. 5. The regulation loop consists of CTAT and PTAT BJTs, PTAT and CTAT current sources, a current-to-digital channel, a 7-bit SRAM bank with an adder, a 12-bit digital PWM, and an in-cell heater. The in-cell BJTs are interfaced sequentially to the current sources that generate \( I_{PTAT} \) and \( I_{CTAT} \). \( I_{CTAT} \) is used as the input to the channel, and \( I_{PTAT} \) is used as the reference current. The channel determines the ratio of \( I_{CTAT} \) to \( I_{PTAT} \). Both currents are scaled such that their magnitude fits within the channel dynamic range over the operating temperature range. The ratio of \( I_{CTAT} \) to \( I_{PTAT} \) results in a linear transfer characteristic (versus temperature) \[29\]. The channel dual-slope MADC performs three tasks. First, it computes the ratio of \( I_{CTAT} \) to \( I_{PTAT} \). Next, it multiplies this ratio by the PID coefficients, \( c_0, c_1, c_2 \), and finally it subtracts the results from the scaled version of the desired temperature, \( (c_0 t(k), c_1 t(k), c_2 t(k)) \). The result of these three operations is the computation of \( c_n e(k) \), as shown in Fig. 5. Next, these values are stored in the on-chip 7-bit SRAM bank. An on-chip adder adds the appropriate values according to Eq.(3) and computes \( u(k) \), which sets the duty cycle of the signal generated by the digital PWM. The duty cycle of this signal sets the amount of time that the in-cell heater is on, thus regulating the temperature. The in-cell heater was implemented by a PMOS transistor with a width and length of 100\( \mu \)m and 0.13\( \mu \)m, respectively, and a 15\( \Omega \) load.

The timing diagram of the PID regulation loop is shown in Fig. 6. The channel dual-slope MADC performs three conversion cycles during one cycle of the PID controller, thus eliminating the need for three parallel ADCs. As shown in Fig. 6 in the first conversion cycle of the PID controller, the ADC computes \( c_0 e(0), c_1 e(0), \) and \( c_2 e(0) \). Next, \( u(0) \) is calculated from these values, and the duty cycle of the digital PWM is set accordingly. Consecutive values of \( c_0 e(n), c_1 e(n), c_2 e(n), \) and \( u(n) \) are generated in the same manner.

V. CIRCUIT IMPLEMENTATION

A. CURRENT-TO-DIGITAL CONVERSION CHANNEL

The top-level VLSI architecture of the current-to-digital conversion channel is shown in Fig. 7. Each channel con-
After time $c_nT_1$, the voltage on the capacitor is held constant for a fixed time interval $T_{RD}$. During this time, the digital representation of the desired temperature that is scaled by the PID coefficients $c_n(t(k))$ is loaded into the counter. During time $c_nT_2$, the integrating capacitor is discharged with the PTAT current source. During time $c_nT_2$, the counter counts down, and the final value of the counter is available at the falling edge of $S_2$ signal. By counting down from $c_n(t(k))$ in the second phase of the conversion cycle, the MADC performs subtraction of $c_ny(k)$ from $c_n(t(k))$ (as shown in Fig. 5) thus computing the error signal $c_n(e(k))$.

The front-end bidirectional current conveyor is implemented by a PMOS and an NMOS transistor connected in the feedback of an OTA [36]. The negative feedback ensures a known potential at the working electrode is set by the voltage at the non-inverting input of the OTA. It also enables the current conveyor to source and sink an input current without the need for a DC offset current. The OTA is implemented as a folded-cascode amplifier with a PMOS input pair. Chopper-stabilization is utilized to reduce the OTA flicker noise and offset and dynamic element matching is utilized to reduce the output current mirrors mismatch [36].

The ADC comparator is implemented with three stages of pre-amplifiers with a total gain of 60dB, and a high-speed latch as the last stage. The first stage of the comparator is implemented as a cross-coupled diode-connected gain stage to provide a moderate gain with high bandwidth. Chopper-stabilization suppresses the input offset and ensures a 9-bit accuracy. The second and third stages are identical to the first one but with no chopping. The high-speed latch is implemented with an NMOS input pair gain stage and an NMOS-PMOS cross-coupled load to provide high accuracy, low offset and a high bandwidth [28].

### B. CTAT and PTAT Current Sources

A simplified circuit diagram of the CTAT current source is shown in Fig. 8a. To generate a digitally programmable base-emitter voltage $V_{BEtrim}$ (compensating for chip-to-chip variations), a PTAT current (generated by a separate on-chip biasing circuit) is passed through a 6-bit programmable resistor connected in series with the diode-connected pnp transistor $Q_1$. The current $V_{BEtrim}/R_1$ is generated by a voltage-to-current converter, as shown in Fig. 8a). A large resistor ($R_1 > 100 \text{M\Omega}$) is required to ensure that the CTAT current is kept relatively low (20nA) and stays within the dynamic range of the ADC. This would result in a large integration area. To reduce the size of the resistor, a current mirror with a 10:1 ratio is utilized. A 10:1 dynamic element matching is used to reduce the effect of the current mirror mismatch. In this work $R_1$ is set to 1.5M\Omega.

A simplified circuit diagram of the DTAT current source is shown in Fig. 8b. The $\Delta V_{BE}$ is generated by determining the difference between the $V_{BE}$ of the two substrate pnp transistors that are biased at 3:1 collector current ratio. The voltage-to-current converter consisting of OTA2 and the NMOS feedback transistor generates $\Delta V_{BE}$ across $R_2$ (split into $R_2/3$ and $2R_2/3$). In this work $R_2$ is set to 100k\Omega. This
results in the desired output current \( \Delta V_{BE}/R_2 \). The resistor \( R_2/3 \) is added in series with the base of the \( Q_3 \) transistor in order to ensure that the base current of the \( Q_3 \) does not affect the output current.

The main causes of inaccuracy in the current sources are the input offset and the flicker noise of OTAs and the mismatch of the bias current mirror. Internal OTA chopping is utilized to reduce the effect of flicker noise and input offset voltage \([37]\). OTA1 and OTA2 adopt the same circuit topology, as shown in Fig. 8(c). The transistor sizes are given in Table I.

| Transistor | W/L (µm)  |
|------------|-----------|
| \( M_{1,2} \) | 9 × 4/1   |
| \( M_{3,4} \) | 4 × 1.5/4 |
| \( M_{5,6} \) | 5 × 1.5/1 |
| \( M_{7,8} \) | 10 × 1.5/1|
| \( M_{9,10} \) | 4 × 1.5/4 |
| \( M_{11} \)  | 11 × 1.5/2|

The simulated input-referred noise of OTA1 in cases where the chopper is disabled and enabled is shown in Fig. 9. The integrated input-referred noise from 0.01Hz to 1kHz is 0.11pA when the chopper is disabled and 0.06pA when the chopper is enabled. The contribution of each transistor to the total input-referred noise is shown in Fig. 10. When the chopper is disabled, the main contributions to the input-referred flicker noise are from the OTA current mirror transistors \( M_5 \) and \( M_4 \), and from the input pair transistors \( M_1 \) and \( M_2 \). When the chopper is enabled, the current mirror transistors \( M_9 \) and \( M_{10} \) are the main contributors to the input-referred flicker noise.

C. Digital Pulse Width Modulator

In the temperature regulation loop, a digital PWM sets the duty cycle of the pulse for controlling the in-channel heater. The achievable discrete set of the duty cycle settings of the pulse depends on the digital PWM resolution. In this work, a 12-bit digital PWM architecture is selected. The design is based on a hybrid delay-line/counter architecture in \([38]\). The block diagram of the PWM is shown in Fig. 11.
architecture, a 7-bit counter and 32-stage ring oscillator are used to achieve the 12-bit resolution. At the beginning of a switching cycle, the output set-reset (SR) flip-flop is set, and the PWM output pulse goes high. The pulse that propagates through the ring at the oscillation frequency serves as the clock for the counter. At the time when the counter output matches the top most significant bits of the digital input \((n_c)\), and a pulse reaches the tap selected by the least significant bits \((n_d)\), the output flip-flop is reset, and the output pulse goes low.

**VI. Experimental Results**

**A. Chip Micrograph**

The micrograph of the fabricated multi-modal amperometric DNA analysis SoC is shown in Fig. 12. The 54 cells are arranged in a 9×6 array on a 3mm×3mm CMOS die. Each cell consists of a current conveyor, a dual-slope MADC, an in-cell bias and clock generator, a pH sensor, a heater, and temperature sensing BJTs. The PID controller, CTAT and PTAT current sources, and the digital PWM are located in the top section of the die. The electrodes are postprocessed with 2D and 3D Au top layers and several metal underlayers.

**B. Temperature Regulation Testing Results**

The output digital code of the ADC versus temperature, from 20°C to 90°C, is shown in Fig. 13. The temperature sensor archives a linear transfer function over the operating temperature range. Fig. 14 shows the measured temperature error of seven dies from one wafer, which operated at a supply voltage of 1.2V. After a one-point calibration for compensating for the BJT variation across channels, the temperature error across the seven dies was less than ±0.5°C within the temperature range of 20°C to 90°C.

![Fig. 13. Experimentally measured digital output of the ADC v.s. temperature.](image)

The digital PWM is characterized by sweeping the digital input code from 0 to 4095 and clocking the digital PWM at 2.5MHz. The experimental results of Fig. 15 show the measured duty ratio of the output pulses as a function of the 12-bits digital input. The minimum (4%) and the maximum (96%) duty ratios are set by design. The digital PWM achieves a linear transfer function over the programmable digital input code with a 0.82 percent maximum error. The digital PWM achieves a minimum duty cycle resolution of 0.1µS.

![Fig. 14. Temperature regulation error experimentally measured on seven dies from one wafer.](image)

An external heater was utilized to set the chip temperature at 50°C and the temperature at each channel was recorded to study the effect of channel-to-channel mismatch. Experimentally measured temperature from 54 channels in one chip is shown in Fig. 16. The mean digital output temperature and the corresponding standard deviation are 49.83°C and 0.20°C, respectively.

An example of the temperature regulation cycle in liquid (5mL 1M potassium phosphate buffer solution), with steps at 35°C, 45°C, 55°C, and 65°C, is shown in Fig. 17. The solid line is the chip temperature and the dashed line is the desired temperature. It takes roughly 10 seconds to achieve an increase.
Fig. 15. Experimentally measured transfer function of the pulse-width-modulator.

Fig. 16. Experimentally measured temperature from 54 channels in one chip.

Table II provides a summary of the experimentally measured characteristics of the system for temperature regulation.

C. Multi-modal Amperometric DNA Analysis Results

The dynamic performance of the cell was measured with a 15Hz sinusoidal input current at a full-scale current of 400nA. The ADC was clocked at 10MHz. A SNR of 56.9dB was measured, leading to an effective number of bits (ENOB) of 9.3. The distortion was limited by a -58.7dB HD2 due to the single-ended architecture of the ADC.

Fig. 17 shows the experimental characterization of pH sensing in the CPA mode. The 3σ error bars from 20 measurements are shown in the figure. The measured current leads to a linear response of 1.8nA/pH within ±2 relative to a pH of 7.

Fig. 18 shows the experimental measurements of prostate cancer DNA in the CV mode. On-chip gold electrodes were used for the CV scans, which were performed in a 20µM potassium ferrocyanide solution. Oxidation and reduction peaks are clearly visible in the CV scans using 5µM single stranded DNA modified electrodes. This is because of the negatively charged film created by thiolated DNA probes when they repel the negatively charged electrochemical reporter. Adding a 5µM non-complementary DNA target does not change the CV signal, which indicates that non-specific adsorption is
negligible. On the other hand, adding a 5µM complementary target to the chip leads to the creation of double stranded DNA on the biosensing electrode, which indicates additional negative charge and elimination of ferrocyanide’s redox peak. The error bars (from 3 chips) in the figure show a detection noise margin of around 4nA.

Fig. 21 shows the experimental measurements of prostate cancer DNA using the IS mode. The IS frequency was from 0.1Hz to 10kHz. The recordings of 20µM potassium ferrocyanide in the cases of 5µM single stranded DNA, addition of 5µM non-complementary DNA, and addition of 5µM complementary DNA target are shown. The 3σ error bars show 20 measurements from 3 chips. The impedance spectrum of DNA probe and non-complementary target are fairly similar as expected. The addition of the complementary DNA probe results in a change in the impedance spectrum.

Table III provides a comparative analysis of the presented design and existing temperature regulated biochemical sensory microsystems. The presented work supports advantageous multi-modal DNA analysis with the most flexible temperature regulation scheme. Our design also achieves a compact channel area, thanks to the synergistic circuit sharing design.

VII. CONCLUSIONS

A 9×6 cell array (54-channel) mixed-signal CMOS temperature-regulated distributed DNA-sensing SoC was developed. The SoC reuses circuitry to perform CPA, CA, IS, and temperature regulation. The on-chip, in-channel heating and temperature sensing elements were implemented in standard CMOS without any post-processing. Local temperature can be regulated to within ±0.5°C of any desired point between 20°C and 90°C using PID control. The overall design achieved a very low power consumption at 42µW per channel from a 1.2V supply. Each channel occupies a silicon area of only 0.06mm². This design can be used in a wide range of applications where temperature regulation is desirable. The proposed circuit sharing methodology can also be beneficial for future highly integrated SoC designs.

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## TABLE III
COMPARATIVE ANALYSIS OF TEMPERATURE-REGULATED BIOSENSORY MICROSYSTEMS

| Modes       | CPA 2010 [4] | JSSC 2017 [11] | JSSC 2019 [6] | TBioCAS 2020 [7] | TBioCAS 2020 [9] | This Work |
|-------------|--------------|----------------|--------------|-----------------|-----------------|-----------|
| Temp. Reg.  | Yes          | Yes            | Yes          | No              | No              | Yes       |
| IS          | No           | No             | No           | No              | No              | Yes       |
| CMOS Process| 0.13µm       | 0.25µm         | 0.25µm       | 0.18µm          | 0.6µm           | 0.13µm    |
| Power       | 165mW        | 118mW          | 256mW        | 2.7mW           | 1.242mW         | 0.35mW    |
| Supply Voltage| 1.2V         | 2.5V           | 2.5V         | 3.3V            | 5V              | 1.2V      |
| Chip Area   | 7.5mm²       | 63mm²          | 10.24mm²     | 15mm²           | 361mm²          | 9mm²      |
| Electrode Count | 16          | 1,024          | 1,024        | 1,225           | 16,064          | 600       |
| Electrode Type | 2D          | 2D             | 2D           | 2D              | 2D              | 3D        |
| Dynamic Range| 55dB         | 116dB          | 93dB         | N/A             | N/A             | 128dB     |
| Conversion Rate | N/A         | 50Hz           | 50Hz         | 17.06Hz         | 100kHz          | 10kHz     |
| Sensitivity | 0.3Hz        | 20A            | 280A         | N/A             | 42.8A           | 8.6pA     |
| Signal Generator | Yes        | Yes            | Yes          | Yes             | Yes             | Yes       |
| Signal Frequency | 1GHz        | N/A            | 50Hz         | N/A             | N/A             | 10kHz     |
| Wireless     | No           | No             | No           | No              | No              | No        |
| Channel      | 1            | 13             | 13           | 49              | 2               | 54        |
| Control Method | PID          | N/A            | N/A          | Off/On          | N/A             | PID       |
| Implementation | Off-chip     | Off-chip       | Off-chip     | On-chip         | Off-chip        | On-chip   |
| Signal Domain | Analog       | N/A            | N/A          | Digital         | N/A             | Mixed-signal |
| Accuracy     | 1°C          | 0.3°C          | N/A          | 1°C             | 0.5°C           | 20.5°C    |

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