Single Event Upset Hardened Design of SRAM Circuits
Xin HE*, Xu HUANG and Wu YANG
Sichuan Institute of Solid State Circuits, Chongqing, P.R. China
*Corresponding author

Keywords: Single Event Effects, Radiation hardened, SRAMs.

Abstract. As a very important component of integrated circuits, static memory is particularly sensitive to single event effects in outer space. In order to ensure the normal function of integrated circuits, radiation hardening of static memory is particularly important. The traditional reinforcement technology based on DICE structure has weak ability to resist dynamic SEU. A separated-bit-line structure is proposed to handle the DICE cells upset during reading and writing, and a double module redundancy method is presented to resolve the upset in the peripheral circuits. The results show these methods are effective to mitigate SEU from DICE cell based SRAMs.

Introduction

With the reduction of IC process size and the improvement of integration, the single event effect (SEE) has become more and more serious in outer space and nuclear explosion radiation environment. In the single event effect, the effect of single event upset (SEU) is particularly prominent. Single event flip refers to the abnormal change of the static memory unit caused by single event effect, which mainly affects the memory cells in digital integrated circuit system[1,2]. In a digital integrated circuit system, the proportion of memory cells is usually as high as 40%-70%, or even 90%. Moreover, as the size of the memory cell becomes smaller and smaller, and the integration degree increases continuously, the required power supply voltage decreases continuously, resulting in the critical charge of the circuit node state change greatly. Therefore, the memory circuit unit is particularly vulnerable to SEU in the application of outer space, making abnormal changes in the data in the memory, making the calculation results of the circuit system incorrect, and even possibly leading to the failure of the system function. Therefore, it is very important to harden the memory cell of digital integrated circuit system against single particle.

In order to solve the single SEU, and to reduce the complexity of the process and meet the requirements of radiation hardened performance, the design method of circuit-level radiation hardened reinforcement has been developed rapidly. At present, the common circuit-level anti SEU technologies include dual interlocked memory cell (DICE) technology, RC filter reinforcement, Muller-C unit reinforcement and so on. For memory circuits, the traditional DICE technology improves the anti SEU flip threshold and has the ability to reinforce the static SEU, but once a single event upset occurs, it can not be repaired, and the anti-dynamic SEU ability is weak. In this paper, based on the technology of double interlocking memory cell, we improve the ability of anti-dynamic SEU by combining the technology of dual modular redundancy to repair single bit upset.

Circuit Design

SRAM can be divided into memory cell array, address decoder, sensitive amplifier and input and output circuit modules. Among them, the memory cell array occupies most of the area of SRAM and is the most sensitive part of SEU. At present, DICE units with self-recovery capability are used to form memory cell arrays in SRAM based on DICE units to avoid SEU[3].

The 12-tube DICE structure unit is shown in Figure 1. Four-point redundant latches are adopted in the structure, and the four latch nodes are X1, X2, X3 and X4; P1, P2, P3 and P4 can be regarded as P-type single-transistor inverters; N1, N2, N3 and N4 can be regarded as N-type single-transistor inverters; N5, N6, N7 and N8 are NMOS transistors for reading and writing data. The single-transistor...
inverters in the structure constitute two relative feedback loops, the PMOS tube constitutes a
clockwise feedback loop, and the NMOS constitutes a counter-clockwise feedback loop. Four storage
nodes of DICE structure can store two complementary levels of data, such as "1010" or "0101",
which can represent 0 or 1 of a binary number respectively, and the four nodes are independent of
each other, but they restrict each other. When one of the nodes is upset by a single event, its level will
be restored by feedback from the adjacent nodes. If both adjacent nodes are upset at the same time, the
level of storage nodes will be upset. Because two adjacent nodes are incident by a single particle at the
same time and the probability of upset is very small, the memory cell based on this structure has better
anti SEU capability.

From the DICE cell structure of Figure 1, it can be seen that the SEU is unlikely to have a fatal
impact on the state of storage nodes under static holding. But in the process of reading and writing
data, DICE structure unit will expose some defects. We take writing data as an example. At this time,
the word line WL is high level, and the NMOS tubes N5, N6, N7 and N8 will be on at the same time.
Node X2 and X4 are connected through N6 and N8, node X1 and X3 are connected through N5 and
N7, then the SEU of one of the nodes will influence the other node of the interval through the on-line
NMOS transistor, thus destroying the self-recovery function of the DICE structure unit and causing
the permanent reversal of the storage unit data.

Figure 1. Traditional DICE structure. Figure 2. Separated-bit-line DICE structure.

Figure 2 shows the DICE structure memory unit with separated-bit-line. Its bit line input end is
increased from two of the traditional DICE structure to four of D0, /D0, D1, and /D1, which
effectively avoids the possibility of SEU occurring when the storage node is on-line in the process of
reading and writing data. At the same time, it can greatly reduce the adverse effects of single event
transient on memory cells. In order to better SEU of SRAM radiation hardened, often in the external
circuit is also adding reinforcement measures. For external circuits, dual mode redundancy or three
mode redundancy are generally adopted. In contrast, dual-mode redundancy occupies less resources
and is fast, but the disadvantage is that if the error occurs, it will output high resistance state, and if it
is not refreshed in time, it will lead to output error. The contents of latches in SRAM's write address
and output circuit will be refreshed in every cycle. Therefore, it is a better choice to use dual modular
redundancy for reinforcement.

Figure 3 is a traditional data writing circuit, where D is the input data signal and WEN is the write
enabling signal. When WEN = 0, the data is converted into two complementary signals to be latched
and sent to bit lines BL and BL_. The latch circuit used consists of a transmission gate controlled
by an internal clock GCLK and two cross-coupled inverters. Once the latch SEU occurs, it will cause
both BL and BL_ bit lines to discharge or not to discharge, so the data written will be an indefinite
value. The dual-mode redundancy hardened writing circuit is shown in Figure 4. Compared with the
original circuit, the improved circuit duplicates a pair of latches storing mutual anti-trust signals,
which will produce four bit-line signals of BL BL_ BL1 BL1_. On the one hand, it provides
redundant latch for data input, and on the other hand, it is compatible with the DICE unit of the
separation bit line. When one of the latches fails, the other three latches still provide the correct
signal. Considering the circuit structure of DICE unit, when three of its four bit lines are correct, the data written can be guaranteed to be correct.

Figure 3. Traditional write circuit.  Figure 4. Dual redundant hardened write circuit.

**Design and Implementation**

In this paper, Cadence's Spectre simulation software is used to simulate the DICE unit of the separated-bit-line and the peripheral circuit strengthened by dual-mode redundancy. In semiconductor integrated circuits, a large number of charges will be generated by single-particle bombardment, and pulse current will be formed under the action of electric field. Usually, the method of injecting a certain width of pulse current into sensitive nodes is used to simulate single-particle bombardment[4].

The traditional DICE unit and the DICE unit in this design are connected to the simulation environment respectively, and the flip pulse injected in 55ns is simulated. The simulation results are shown in Figure 5. In Figure 5, after injecting the pulse, the nodes of the storage unit of DICE flip over, which results in errors in readout data. In Figure 6, because the BL of the DICE structure is not directly connected to the storage node, the flip pulse on the BL has no effect on each node. The flip pulse on BL is temporary. When the pulse passes, the BL level returns to normal and the correct value is read out.

Figure 5. Traditional DICE data reading sequence.  Figure 6. Improved DICE data reading sequence.

At 10ns, the data is written to the memory unit under test, and the writing period is 5ns. Before the end of the writing period, the data bus is bombarded by a single particle, which generates a 1ns flip pulse. Figure 7 is a simulation of a traditional DICE bombarded by a single particle. Because BL and BL_flip simultaneously, four DICE storage nodes are exposed to the flipped BL and BL to connect with them at the same time, so the flip occurs. Figure 8 is a simulation of the improved DICE being bombarded by a single particle during the writing cycle. Unlike traditional DICE, when four nodes encounter flip pulses, only two nodes associated with BL and BL_flip, then recover under the feedback of the other two non-flip nodes, and finally write the correct value.

Based on the above technology and 0.13 um process, a RAM memory with 1024x16 bits capacity is designed and implemented. The storage array is divided into two sub-arrays. Each sub-array contains 128 rows and 64 rows of storage units, so that the load on the word and bit lines is roughly balanced.
Conclusions

By comparing and analyzing the simulation waveforms and experimental results, SRAM memory unit based on DICE structure with separated bit lines can achieve the read-write performance of traditional SRAM. Separated bit line makes SRAM memory cells have effective anti SEU characteristics in data holding and data reading and writing states. The dual-mode redundancy reinforcement structure of peripheral circuits also provides a more powerful guarantee for SRAM's anti-radiation ability.

References

[1] Rockett L R. Simulated SEU hardened scaled CMOS SRAM cell design using gated resistors[J]. IEEE Trans. Nucl. Sci. 1992, 39.

[2] Baumann R C. Radiation-Induced Soft Errors in Advanced Semiconductor Tech-nologies[J]. IEEE Transactions On Device and Materials Reliability, 2005, 5:305-316.

[3] Chen T H, Chen J H, Clark L T. Ultra- low power radiation hardened by design memory circuits[J].IEEE Trans. Nucl.Sci, 2007, 54: 2004-2011.

[4] Maru A, Shindou S, Ebihara T, et al. DICE based flip-flop with SET pulse discriminator on a 90nm bulk CMOS process[C]. Nuclear and Space Radiation Effects Conference, 2010.

[5] Amusan, L. W. Massengill, B. L. Bhuva, et al. Design techniques to reduce SET pulse widths in deep submicron combinational logic[J]. IEEE Trans. Nucl. Sci., 2007, 54:2060-2064