A Design and Realization of State Monitor Based on Avionics Core Processor

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Abstract. Based on the composition and the results of FMEA of Avionics Core Processor, this paper selects temperature, power and network for monitoring. Temperature monitoring for processor and high-power FPGA, current monitoring for power supply and network management and status collection. Next, the detailed design and implementation, information reporting and implementation process are discussed. Then the comprehensive diagnosis and system level state monitoring analysis are to be carried out in the next step.

Keywords: Avionics Core Processor; network management and status collection; comprehensive diagnosis.

1. Introduction
The Avionics Core Processor is the core processing system of the integrated modular avionics system and the core of the new generation of integrated modular avionics system. The integrated avionics system is the nerve center of modern aircraft. The high-performance avionics system has become the key factor to improve the comprehensive performance of military aircraft. With the improvement of the highly integrated degree of airborne equipment, the requirements for the reliability and stability of the Avionics Core Processor system are becoming higher and higher [1]. Therefore, it is particularly important to monitor the status of the Avionics Core Processor to ensure the normal operation of the platform.

Due to the high complexity of the Avionics Core Processor, it is obviously unrealistic to monitor all States of the platform. Therefore, based on the results of system failure mode impact and hazard analysis, it becomes a method to monitor the components or functions with high hazard or serious impact [2].

2. System composition and monitoring object

2.1. platform composition
The Avionics Core Processor is the core processing functional area of avionics system. Its internal and external communication design is based on the FC unified optical fiber network interconnection realized by non-blocking, real-time and fault-tolerant switching matrix switch. The internal hardware module design of the Avionics Core Processor will be classified and standardized, which is mainly...
composed of standard Line replaceable modules (LRM) such as power module, I/O module, general processing module, switch module and other functional modules [3]. The power module mainly realizes power conversion and power supply of the whole platform. The I/O module realizes the management and control of the whole avionics system, including application management and platform management. At the same time, it also provides I/O interface for the Avionics Core Processor. The switch module provides FC switching function between modules inside the core computing platform and other avionics systems. General processing and other functional modules mainly undertake application processing functions. Its specific composition is shown in Figure 1.

![Figure 1](image)

**Figure 1** the component of Avionics Core Processor

2.2. *platform status monitoring strategy*

Based on the existing FMECA results, the following factors must be considered in the condition monitoring of Avionics Core Processor:

(1) The Avionics Core Processor has high processing power to complete complex integrated processing tasks, which also brings very high power consumption. The power consumption of a single platform is expected to be at the kilowatt level; Due to the limited space, weight and the volume, the power consumption density per unit volume is very high. Therefore, the heat dissipation system of the Avionics Core Processor must be monitored to ensure the service life of the platform.

(2) COTS technology is widely used in the Avionics Core Processor, and some components may only be of industrial grade. Although it can work normally under airborne ambient temperature, long-term out of range operation will affect the service life of components; Therefore, we need to obtain the temperature and other parameters of each high heating component in the platform in real time to ensure its working environment;

(3) The Avionics Core Processor is the center of the whole avionics system, which has a direct impact on the normal operation of the whole avionics system. The transmission medium of FC network between the platform and other equipment is optical fiber, which has high requirements for connection accuracy. Therefore, monitoring and management of the whole network is also an important means to ensure the normal operation of the system;

(4) The power supply module in the Avionics Core Processor supplies power to other modules, which is the basis and premise for the normal operation of other modules in the platform. It is necessary to monitor the power supply operation status of the platform to carry out fault isolation, control platform power supply reconfiguration and emergency power supply configuration, to achieve the objectives of platform redundant power supply, fault monitoring and isolation;

Based on the above analysis, the Temperature, Power supply and Network status of Avionics Core Processor need to be monitored first.
3. State monitoring design

3.1. temperature monitoring

The devices with the highest thermal density in the Avionics Core Processor mainly include processor and FPGA. Temperature sensor and test circuit are designed for high-power devices such as processor in the platform to monitor the temperature state of high-power devices in real time, so as to ensure that the key high-power devices are within the reasonable working temperature range.

3.1.1. processor temperature monitoring. The processor of the Avionics Core Processor is mainly applied to the high-end chip of Freescale company. Temperature sensors are designed in the chip. The temperature sensor integrated with the chip can accurately measure the CPU temperature and save board level space.

ADT7461 is a dual channel digital temperature measurement circuit launched by ADI company. It can cooperate with the temperature measurement sensor integrated with CPU chip to realize real-time monitoring of remote temperature and local temperature. The chip provides great flexibility for users. The measurement range, conversion rate and operation stop can be controlled by reading and writing configuration registers. When the collected remote temperature or local temperature exceeds the temperature limit or the peripheral temperature measurement circuit is open, the alarm interrupt will be triggered. At the same time, the interconnection between CPU and ADT7461 is completed through I2C bus to realize the processor's control of ADT7461 and the readback of its own temperature [4]. The hardware design is shown in Figure 2.

![Figure 2](image)

**Figure 2** Temperature measurement system circuit diagram

3.1.2. FPGA temperature monitoring. The FPGA contains a system monitor located in the center of the die. The implementation of the system monitor is based on a 10 bit analog-to-digital converter (ADC) that can sample two hundred thousand instructions per second. By combining with a series of different on-chip memory sensors, ADC can be used to detect the physical operating characteristic parameters of FPGA, such as on-chip power supply voltage and core temperature. Figure 3 below shows the module structure of the system monitor.
The control logic of system monitor can realize some general monitoring, such as temperature monitoring[5]. The ADC can generate a complete 10 bit code according to the 1V differential input voltage of its external analog input. By reading the ADC code in the status register corresponding to the corresponding attribute, the actual value of the attribute to be monitored can be obtained through the calculation formula. Temperature monitoring can realize the temperature monitoring function from $-40^\circ C$ to $+125^\circ C$, and the temperature calculation formula is shown in formula (1).

$$\text{Temperature} (^\circ C) = \frac{\text{ADC code} \times 503.975}{1024} - 273.15$$

(1)

3.2. power monitoring

The power supply monitoring mainly carries out current monitoring. The function of the circuit is to detect the current passing through each switch array, generate voltage analog signal according to the current and provide it to the control unit for analog monitoring[6]. In order to reduce deviation and the power consumption of resistance and simplify the circuit design, the Hall effect current detection IC circuit based on linear current detection is selected in the design of Avionics Core Processor, and the current value is detected through the conversion relationship of detection voltage. The detection principle is that the output voltage $V_{out}$ of the current detection circuit is directly proportional and linear with the flowing current, and the detection current is calculated according to the conversion formula (2).

$$V_{OUT} = I_{SENSE} \times A_V$$

(2)

Where $I_{SENSE}$ is the detection current; $A_V$ is the device sensitivity conversion constant (185mV/A). Two thresholds are designed for current detection. One is to judge whether the power supply on each module of the later stage works in the current limiting state, The other is to judge whether the current of each switch exceeds the maximum set value. According to the actual working state of the Avionics Core Processor, the designed current detection range of the power management system is 0.5A ~ 6.2a. If it exceeds this range, it is judged to be abnormal and the switch will be closed automatically.

3.3. network monitoring

Network monitoring is mainly used to manage and monitor FC network. Network management is used to realize the functions of network initialization, operation control and communication configuration, which are core functions of network management. The testability of network management includes: function status monitoring of network remote terminal; Network system operation status monitoring; Online/offline control of network remote terminal; Network system operation structure reconfiguration.
process control; Remote terminal operation control of network system; Operation control of network switch; Protocol communication control function.

The overall design of network management is realized in two aspects: hardware and software. The hardware provides the sending and receiving scheduling mechanism of network management protocol data, configuration flash and hardware clock management mechanism. For software, ELS service based on FC protocol is adopted, and system network management operations are defined by user-defined fields open to the protocol (see Figure 4) [7], realizing the design of network management protocol and network control process. The implementation of network management includes the following parts: first, the definition of command format: use the frame format specified in FC protocol, use three types of services as the service type of network management protocol, and use LS_CMD of ELS at the same time and user defined FUNCTION_ID as a whole to form the definition of the network management command. The second is the process control method: the process of network management is based on the command/response mode to complete the whole control process.

4. monitoring information processing and reporting

4.1. record of monitoring information
The I/O module is usually defined as the system controller of the Avionics Core Processor, which undertakes the management and control of the whole platform. A large number of nonvolatile memories are configured on each functional module in the Avionics Core Processor to store the monitoring signal status information. These information can be sent to the input and output module according to the needs of the system; It can also be obtained by testing maintenance equipment under ground maintenance status. At the same time, there is a large capacity module specially responsible for recording, which can be used as a database to record the status monitoring information of the platform.

4.2. information reporting process
The status information collected in the Avionics Core Processor needs to be reported layer by layer and submitted to the upper layer for processing. The upper layer will process the collected status information according to the fault category and influence degree, such as stopping work, sending alarm, or comprehensive diagnosis.

Each LRM module in the platform collects the status information through the processor, reports it to the switch module through the FC communication interface, and forwards it to the I/O module. The status information of the switch module itself is directly forwarded to the I/O module[8]. The power module and other non FC cross-linked equipment are reported to the I/O module through other interfaces. The I/O module summarizes the status information and directly reports it to the upper level system. The reporting process is shown in Figure 5.
5. Summary
The status monitoring of the Avionics Core Processor has better completed the recording and monitoring of the key information of the platform, and played a good role in fault discovery and fault isolation of the platform. However, the following aspects need to be further strengthened:

(1) The Avionics Core Processor is a platform level product with high technical requirements and dense layout, which is difficult to support a large number of test circuit designs, so it is necessary to strengthen application testing and monitoring means;

(2) The Avionics Core Processor belongs to the bottom platform and only provides bottom module level and platform level monitoring. These bottom monitoring are independent of each other and have certain limitations, which is difficult to support the detection of complex modes. Therefore, it is suggested that the upper application should fully consider the design, make balanced selection in implementation, provide comprehensive diagnosis strategy and carry out system level monitoring analysis according to the monitoring information and results.

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