Hardware Design of an Image Acquisition Device for Target Observation and Tracking

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Abstract. In order to observe and track the separated targets in the air, this paper presents a hardware image acquisition platform based on three-way camera + FPGA + two-way DSP. Xilinx artix-7 series xc7a200t-2fbg676i FPGA is used as the main processor. It is mainly responsible for high-speed image acquisition, preprocessing, transmission and display. TMS320DM368 DSP of Texas Instruments is used as image compression processor. After receiving the image transmitted by artix-7 FPGA, the image H.264 is compressed. This architecture solves the delay problem of traditional image acquisition system in hardware architecture level, and realizes the real-time and high-speed image acquisition and processing. At the same time, the hardware has the basis of multi-channel image acquisition, multi-channel image compression, visible light and infrared camera acquisition data fusion.

1. Introduction

At present, image acquisition and processing [1] is one of the important issues in the field of machine vision [2] and artificial intelligence [3], and its key technology is high-speed image acquisition and processing at the source end [4]. Most of the traditional image acquisition and processing systems are based on PC architecture. The image acquisition and processing system based on PC architecture has the advantages of strong universality, strong expansibility and strong processing and computing ability. However, its large volume can only work on the ground, so it is difficult to install it on various small aerial unmanned aerial vehicles. And the hardware cost of the whole PC based architecture is high. For the aerial unmanned aerial vehicle (UAV), the fast dynamic characteristics and extremely high flight speed determine that the image acquisition system must have high real-time performance and high accuracy, and also have higher requirements for the size of the system. Although the high-speed image acquisition and processing board based on FPGA and DSP has appeared in the market, there is a lack of image acquisition and processing board with small size and multi-channel camera acquisition, including visible light camera [5,6] and infrared camera [7,8] and high-speed output of image H.264 compression [9].

2. Overall structure of the system

This paper presents an application of high real-time, high processing speed, small size and low power consumption system with three cameras and hardware architecture based on FPGA and DSP.
A hardware architecture of image acquisition device for aerial separation target observation is composed of imaging unit and main control unit. As shown in Figure 1.

The imaging unit is characterized in that it is composed of three cameras, two visible cameras and one infrared camera. In function, one visible camera and one infrared camera are used to observe the target, and the other visible camera is used to track the target. All three cameras are on the shelf products that can be purchased directly on the market.

The hardware architecture of the main control unit consists of one FPGA, two DSPs, power conversion module, clock generation module and external interface module. Among them, the FPGA uses Xilinx company artix-7 series xc7a200t-2fg676i as the main processor chip; external 2GB ddr3-1600 memory is used as image data buffer; 128MB nor flash is external connected. By configuring it into SPI mode, the application logic circuit can be solidified in NOR flash, and automatically slave nor by power on The FPGA expands one channel of Cameralink interface, uses TI company's ds90cr287 chip, the rate is 85 MHz, can test any channel of imaging unit video output; the FPGA and external communication leads out 4 channels of RS422 and one channel of 485 interface for users to use; the hardware structure of two DSP is the same, DSP adopts tms320dm368 of Texas Instruments Company. As a coprocessor chip, DSP is responsible for video compression processing. DSP is connected with 1GB ddr2-800 memory, which is used as the buffer of compressed image data; DSP is external connected with 2GB NAND flash, which is connected with DSP through EMIF interface to store application programs and algorithm programs. Users can automatically boot and store them in NAND flash programs through dial switch configuration; artix-7 FPGA is connected with two tms320dm368 DSP through common IO port.

The visible light (observation and tracking) camera in the imaging unit transmits the original image data to the artix-7 FPGA of the main control unit through the connector, and the FPGA transmits it to a tms320dm368 DSP. After the image is compressed by DSP, the compressed image data is transmitted back to artix-7 FPGA through SPI bus; the compressed image data received by artix-7 FPGA is transmitted to the outside world through RS422 and 485 interfaces. Similarly, the infrared camera in the imaging unit transmits the compressed image data to the outside world through RS422 and 485 interfaces through FPGA. The power conversion module converts the external power supply into the power supply required by each chip, and the clock generation module provides the working clock of each chip.

3. System hardware design
The hardware structure of the system is shown in Figure 2. Three cameras are connected to artix-7 FPGA for image acquisition; in addition, an external Cameralink interface is connected to artix-7
FPGA for testing and outputting any channel of camera image data display. When the image data is obtained by FPGA, the acquired image data is transmitted to DSP through IO interface for image compression processing, and the processed results are sent back to artix-7 FPGA through SPI interface. Finally, the image data processing results are transmitted to the outside world through RS422 and 485 interfaces by artix-7 FPGA.

3.1. Imaging unit

Two visible cameras are used 1080p@25Hz HD camera, infrared camera adopts long wave uncooled infrared 640 × 480@25Hz Camera;

3.2. Main control unit

(1) Xilinx's artix series xc7a200t-2fbg676i FPGA is used as the main processor chip, which is responsible for image acquisition, transmission and peripheral interface control;

(2) Tms320dm368 DSP of Texas Instruments Company is used as coprocessor chip, which is responsible for image compression processing;

(3) Artix-7 FPGA is connected with 2GB ddr3-1600 memory, which is used as the buffer of image data;

(4) Tms320dn368 external 1GB ddr2-800 memory is used as the buffer of compressed image data;

(5) Tms320dm368 is connected with 2GB NAND flash and connected with DSP through EMIF interface to store application program and algorithm program;

(6) Flash-1287 can be connected to flash-1287, and it can be automatically configured from the nor in the FPGA;

(7) The artix-7 FPGA extends one Cameralink interface, which can output any one of the three cameras for test;

(8) Four channels of RS422 and one channel of 485 interface are exported from artix-7 FPGA for users to use;

(9) The architecture adopts 5V / 4A DC power supply.

The three-way camera consists of two visible cameras and one infrared camera. One visible camera and one infrared camera are used for observation, and the other is for tracking. Xilinx's artix-7 FPGA is used as image acquisition, recognition, tracking and interface extension. Ti's tms320dm368 DSP is used for image H.264 compression processing. FPGA and DSP are connected through common IO ports. The system hardware architecture design mainly includes the following modules:

(1) Power module

It is powered by 5V / 10A DC power supply, and then converted to the desired voltage value through DC / DC circuit. The 3.3V, 1.8V, 1.2V, 1.0V power supply of artix-7 FPGA adopts ltm4644 (DC-DC) power chip, which can output 4-channel power supply at the same time. Each channel can stably output 4A current. The circuit is simple and can ensure the power and efficiency requirements. The 3.3V, 1.8V, 1.35v and 1.5V power supply of DDR3 in DSP are also implemented by ltm4644 power supply chip. The 0.75V reference voltage used in DDR3 is realized by using tps51200 chip of Ti, which has the advantages of small voltage difference and low noise.

(2) Clock module

FPGA uses active crystal oscillator as the clock generation device. The specific chips are sit1602 74.25mhz of sitime company and asfh150mhz of Abracon company. DDR3 uses differential crystal oscillator as the clock generation device. The specific chip uses sit9102 of sitime company, DSP uses passive oscillator as the clock generation device, and the specific chip uses abm3b 24MHz of Abracon company.

(3) Storage module

Artix-7 FPGA is used for image acquisition, processing and communication, so it has a large amount of logic resources. Using 128 MB SPI protocol nor flash has the characteristics of fast reading speed and large capacity. In order to match the bandwidth of image processing and data
communication, high-speed storage technology must be introduced. DDR3 memory is the most widely used and mature high-speed dynamic memory in high-end hardware system architecture. It has the technical characteristics of low power consumption, high density, high bandwidth, etc. In terms of transmission rate, it is obviously better than the traditional storage technology, while improving the storage performance, it also reduces the power consumption and further reduces the core voltage. In addition, DDR3 adopts point-to-point topology architecture to reduce the burden of address/command and control bus. In this invention, DDR3 storage technology is adopted, and a 1GBIT DDR3 1333 memory chip is configured for artix-7 FPGA. Tms320dm368 DSP uses an external memory, which is connected with a 2GB NAND flash through the EMIF interface.

(4) Communication link

The image data transmission between artix-7 FPGA and three cameras is directly input through ordinary FPGA IO port. There is image data transmission between artix-7 FPGA and tms320dm368 DSP. It is transmitted by ordinary IO and SPI protocol. The transmission between artix-7 FPGA and the outside world is through 4-channel RS422 and one channel 485 interface data.

(5) Application environment

The hardware architecture of an image acquisition device for aerial target observation and tracking is mainly used in UAV to observe and track separated targets in the air. The target is observed by a visible light camera and an infrared camera. The collected image is input to tms320dm368 through artix-7 FPGA. The image is compressed by DSP and then returned to FPGA. It is transmitted to external storage device through RS422 / 485 interface. The target is tracked by a visible light camera. The collected image is input to tms320dm368 through artix-7 FPGA. The image is compressed by DSP and then returned to FPGA, which is transmitted to the external attitude control system through RS422 / 485 interface, forming a closed loop with the attitude control system to complete the attitude control of the aircraft, so as to improve the accuracy of the observation and tracking of the target.

![Hardware structure of image acquisition device](image-url)

**Figure 2.** Hardware structure of image acquisition device
4. Experimental results
The design of the hardware system is shown in Fig. 3, with the size of 200mmx70mm, reaching the miniaturization size. After decoding and displaying the image quality of the upper computer through the dm368 video compression system, the high-definition video format can be transmitted and played smoothly without distortion and mosaic phenomenon. The delay time of the system is about 0.5 ~ 0.8s. The delay of the system is determined by video coding, packet forming, transmission and host computer decoding. The target can be tracked in the range of 5m ~ 300m.

Figure 3. Hardware picture of image acquisition device

5. Conclusion
This paper presents a hardware architecture of image acquisition device for observing and tracking aerial targets. On the one hand, three cameras (two visible cameras and one infrared camera) are used to observe and track the target, and the independent optical imaging unit is used to improve the reliability and stability of the system 1080p@25Hz High definition video H.264 compression, compressed image sequence without distortion, video smooth; with HD video target recognition and tracking capabilities, on the other hand, using FPGA is based on pure hardware logic, which has strong parallel processing ability, and tms320dm368 DSP has strong compression and processing ability of complex images, which makes the system architecture not only meet the real-time performance of the system, but also can ensure the high reliability of the system, and greatly reduce the power consumption of the system, so that the system has a stronger environmental adaptability. At the same time, the hardware has the basis of multi-channel image acquisition, multi-channel image compression, visible light and infrared camera data fusion.

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