New symmetric and planar designs of reversible full-adders/subtractors in quantum-dot cellular automata

Moein Sarvaghad-Moghaddam\textsuperscript{a} and Ali A. Orouji\textsuperscript{b}

Department of Electrical and Computer Engineering, Semnan University, Semnan, Iran

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Abstract. Quantum-dot Cellular Automata (QCA) is one of the emerging nanotechnologies, promising an alternative to CMOS technology due to a faster speed, smaller size, lower power consumption, higher scale integration, and higher switching frequency. In addition, power dissipation is the main limitation of all the nanoelectronics design techniques including the QCA. Researchers have proposed various mechanisms to solve this problem. Among them, reversible computing is considered as a reliable solution to reduce the power dissipation. On the other hand, adders are fundamental circuits for most digital systems. So, in this paper, the focus is on designing of reversible full-adders in logical and layout levels. For this aim, the first, a method for converting irreversible functions to reversible ones is investigated. Based on it, two novel designs of reversible full-adders/subtractors are presented. In another section, a new five-input majority gate is introduced. By using of this gate, a new reversible full-adder is designed. Finally, the proposed structures are extended to design three new 8-bit reversible full-adder/subtractors. The results are indicative of the outperformance of the proposed designs in comparison with the best available ones in terms of area, complexity, delay, reversible/irreversible layout, and also in logic level in terms of garbage outputs, control inputs, number of majority and NOT gates.

1 Introduction

Energy dissipation is one of the major issues in present-day technology. Landauer [1] has proved that irreversible computation will have $k_B T \ln 2$ joules of dissipated energy due to loss of single bit information. Here, $k_B$ and $T$ holds for Boltzmann’s constant and the computing temperature. In 1973, Bennett, showed that in order to avoid energy dissipation in a circuit it must be built from reversible circuits [2]. Reversible computing considers the relation between information dissipation and energy dissipation at the logical level. If a one-to-one mapping is established between the input and output vectors, the reversible computation would be achieved at the logical level [2]. The one-to-one mapping is called bijective property. In addition, fan-out is not possible in reversible systems. The unused outputs are used to maintain the reversibility of the circuits and are known as the garbage outputs. The constant inputs in the reversible circuits are called the ancilla.

Quantum-dot Cellular Automata (QCA) is a well-known technology which can be considered as a candidate for FET (Field Effect Transistor)-based devices on nanoscale [3–5]. Features of a more scalability, fast switching time and extremely low power into CMOS has caused QCA to become a very interesting topic of researches [6–8]. A QCA cell consists of four dots and two identical electrons. Each dot can be occupied by one of the two hopping electrons in a way that the electrons stay diagonally opposite due to Coulombic interaction. In QCA technology, the binary information is encoded with the arrangement of electrons rather than the current employed in CMOS. Two fundamental building blocks for QCA are the inverter and the majority gate [3]. In QCA logic, the clock is responsible for synchronization, control of information flow, and also it provides power to run the circuit [9,10].

However, it should be pointed out that the majority voting (MV) function is logically irreversible; but it has been shown in the literature that different clocking arrangements can be used for reversible computing in QCA. By using the clocking scheme is referred to as Bennett clocking can offer a practical realization of reversible computing in QCA. It has been shown by direct calculation which with Bennett clocking, energy dissipation per switching event is much less than $kT \ln 2$ for QCA circuits even with devices such as MV (which is irreversible function) and feature of fan-out (which is not a valid feature in the main definition of reversible functions) [11,12].

Adders are fundamental circuits for most digital systems and several adder designs in QCA had been proposed [13–16], and a performance comparison was presented [13]. In some of full adder designs, 3-input majority gates were employed [17,18] however recently 5-input ones had been
used in order to reduce the number of cells as well as the occupied area in designs [19–21]. In design proposed in [22], there are three 3-input majority gates, two inverters, and four clocking phases. In Azghadi et al. [23] a QCA full-adder was implemented only using three gates, two majority gates, and one inverter. In this design a five-input majority gate had been used that it has a simpler design scheme in comparison to another previous design [22]. Five-input majority proposed in Azghadi et al. [23] has a cubic structure, and maybe it is not simply feasible to fabricate. In Cho et al. [18] a new design for QCA full-adders was presented which revised the previous full-adder scheme. This design has only three clock phases.

Lent et al., proposed circuit design based on QCA in reversible logic [24]; then several authors proposed several reversible gates in QCA [25–28]. In Mohammadi and Mohammadi [29], designing of a one-bit full adder had been investigated using a QCA implementation of Toffoli and Fredkin gates. Then, a full adder design with reversible QCA1 gates had been proposed. Also, in Kianpour and Sabbaghi-Nadooshan [30], a novel 3 × 3 reversible gate that is universal and testable had been presented. By using this gate, a new 8-bit full-adder was designed. In this paper, the proposed design is even worse into work [29] in terms of complexity and area and delay. In this paper, innovation is divided into three sections. In the first section, a method for converting irreversible functions to a reversible one is presented. This method has advantages such as: converting of irreversible functions to reversible one directly and as optimal (so, in this method, sub-optimal methods which use conventional reversible blocks such as Toffoli and Fredkin, are not used), minimum number of garbage outputs. In addition, garbage outputs do not create any additional gates (majority and NOT gates). Then, Using the method, two new symmetric and planar designs of reversible full-adders are presented. In the second section, a new symmetric, planar and fault tolerant five-input majority gate is proposed. Based on the designed gate, a reversible full-adder is presented. Next, for this gate, a fault-tolerant analysis is proposed. In the third section, based on the proposed designs, three new 8-bit reversible full-adder/subtractor(s) is designed. In comparison with the best existing implementations, the proposed designs have demonstrated significant improvements in terms of area, complexity, delay, reversible/irreversible layout, and also in logic level in terms of garbage outputs, control inputs, number of majority and NOT gates.

The rest of the paper is organized as follows: Section 2 presents some related background materials. Section 3 introduces the proposed method in detail. Section 4 shows simulation results and comparison. Section 5 concludes the paper.

2 Background material

In this section, basic concepts in QCA technology such as Quantum-dot cellular automata and QCA devices are explained.

![Fig. 1. (a) Structure of a QCA cell with four quantum dots. (b) QCA cell with two different polarizations.](image-url)

2.1 Quantum-dot cellular automata

As shown in Figure 1a, a standard QCA cell is composed of four quantum-dots and two excess electrons located at the corners of a square. According to the existing Coulombic interaction between the electronic charges, they can occupy diagonal antipodal sites through tunneling junctions. Therefore, a single QCA cell can accept two completely polarized states called cell polarization $P = +1$ (binary “1” state) and $P = -1$ (binary “0” state) as shown in Figure 1b.

2.2 QCA logic devices

The fundamental QCA logic devices include a QCA wire, QCA inverter, and QCA majority gate. A 90° QCA wire is just a line of QCA cells. The wire is driven at the input cell by a cell with a fixed/held polarization [31]. The signal propagates along the wire from left to right when excited from the leftmost cell. A QCA wire can also be built with cells rotated by 45°. This kind of wire propagates the input signal in odd cells and inversion of the input signal in even cells [32,33]. A QCA majority gate can perform a three-input logic function as given in (1), where $A$, $B$, and $C$ are the three inputs.

$$M(A, B, C) = AB + BC + CA. \quad (1)$$

By forcing one of the three inputs of the majority gate to a constant logic “0” or a “1” the majority gate can be used to perform AND/OR operations as shown in the following equations:

$$M(A, B, 0) = AB, \quad M(A, B, 1) = A + B. \quad (2)$$

Figure 2 demonstrates a QCA wire in 90° and 45°, inverter gate, and majority gate, respectively.

In QCA, there are two crossover options. They are coplanar crossings and multilayer crossovers. In first way, one quantum wire with a 45° turn passes over a regular quantum wire without any interference. This approach is shown in Figure 3a. In the other approach, multi-layered structures are used for the passage of the quantum wires over each other. This structure is shown in Figure 3b.
2.3 Five-input majority gate

A five pins majority gate must have five inputs and one output. Figure 2e illustrates a schematic of the five-input majority gate. The majority voting logic function can be expressed in terms of the fundamental Boolean operator as shown in (3).

\[
M(A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE.
\]

(3)

A three-input AND gate and also a three-input OR gate can be implemented using this majority gate. These functions are as (4).

\[
M(A, B, C, 0, 0) = ABC,
\]
\[
M(A, B, C, 1, 1) = A + B + C.
\]

(4)

2.4 QCA clocking

In VLSI circuits, timing is controlled by a reference signal which is called clock but in QCA, the information storage and erasure in the cell are controlled by the clock. Clocking is required for QCA circuit to synchronize and information flow control. Two strategies have been considered for clocking QCA [11]: (1) Landauer clocking: has a logically irreversible “erase” operation (2) Bennett clocking: has a logically reversible “copy-then-erase” operation [34]. It has been shown that erasure without copying requires an amount of dissipated energy in the order of the signal energy. This scheme could offer a practical realization of reversible computing using QCA.

Generally, four multi-phase clocking signals applied as shown in Figure 4a is called Landauer type [35]. During a complete cycle, each zone goes through the four phases. These zones must follow a particular order namely \( C_0 \to C_1 \to C_2 \to C_3 \). Four phases are called Switch, Hold, Release, and Relax [10]. In switch phase, QCA cell is starting to move from un-polarized state to polarize state and the barriers of the dots is raised. The electrons are started tunnelling through dots as the dots are influenced by the electron of its neighbor cell. In Hold phase, barrier of the cell is in the high value, electron can’t tunnel through dots and cell maintains their current states i.e. fixed polarization. In release phase, barrier is lowered, electron can tunnel through dots and states of the cell become unpolarized. In relax phase barrier remains lowered and cell stay in un-polarized state. Another type of clocking signals for reversible circuit is Bennett-type clocking [34]. The waveform of Bennett clocking is shown in Figure 4b. The principle of this clocking is to first compute the results by latching the cell array from input to output and then uncompute by latching array to relax to an unpolarized state from output to input.

3 Proposed method

In this section, first, a method is introduced for converting multi-output irreversible functions to reversible ones. Then, according to it, new designs of reversible full adders are proposed. In addition, a new structure of five-input majority gate is presented that based on it, another design of reversible full adder is presented.

3.1 Method for converting multi-output functions to reversible functions

As stated in previous sections, in basic definition, a reversible function has the following features:

1- There is a one-to-one mapping between inputs and outputs.
2- Feedback is not allowed.
3- Fan-out is not allowed.

However, as stated in [11,12] features “2” and “3” is not necessary for creating reversible functions in QCA technology. So, for converting the multi-output functions to
the reversible functions, only, one to one mapping between inputs and outputs must be created. Also, it is not necessary that the number of inputs and outputs be same. To this end, first, equal states in outputs are marked, then, input columns are compared with outputs and through them, an input column is selected so that can make discrete the maximum number of the equal states in outputs. This column is added as a new column in output. This work is repeated until equal states in outputs is separated fully. By using this method, directly, anyone can create each type of reversible functions with minimum complexity, area, garbage outputs, control inputs and delay while other methods such as [29,30,36] have used well-known reversible blocks such as Toffoli and Fredkin gates for designing other reversible functions which these methods are not optimal. Our method has the minimum number of garbage outputs. As in this method, garbage outputs are added one to one for removing the maximum number of equal states. Another feature of this method is that garbage outputs do not create any additional gates (majority and NOT gates) for converting irreversible functions to reversible one. So, the number of majority gates are optimal. So, it has minimum complexity, delay, and area. Control inputs are redundancy inputs used for creating AND/OR gates. For a reversible function, these inputs must be minimum for reducing power consumption. In the next sections, we design new reversible functions using this method in QCA technology.

3.1.1 The proposed reversible full-adder

By using the proposed method for creating reversible functions, a new design of reversible full-adder is proposed. Specification function of this full-adder is shown in Table 1. As shown in this table, the first, equal states in outputs are determined (showed with gray color in Tab. 1). Two input columns \(a\) and \(b\) are added as output columns or garbage outputs. These two garbage outputs \(Gar_1\) and \(Gar_2\) are selected according to the maximum removing of equal states in specification function and create a one to one mapping between inputs and outputs. In this table, there are three equal states 01 and three equal states 10. By adding \(Gar_1\) output, that is same with column \(a\) in input \((Gar_1 = a)\), one equal state in 01 state and one equal state in 10 state are removed. Then, by adding \(Gar_2\) output as same with \(c_{in}\) column in input \((Gar_2 = c_{in})\), all equal states in output are removed and one to one mapping between input and output are created.

In the next step, for synthesizing each of outputs, the method in Sarvaghad-Moghaddam et al. [37] is used. As stated above, garbage outputs are same with inputs as the Control inputs.
Following:

\[
\begin{align*}
\text{Gar1} &= a, \\
\text{Gar2} &= c_{in}.
\end{align*}
\]  

(5)

\( C_{out} \) and \( \text{Sum} \) outputs can be synthesized as the following optimal forms with majority and NOT gates:

\[
\begin{align*}
\text{C}_{out} &= ab + bc_{in} + ac_{in} = M(a, b, c_{in}), \\
\text{Sum} &= abc_{in} + ab'c_{in}' + acb_{in}' + a'b'c_{in} \\
&= M(M(a, b, c_{in})', a, M(a', b, c_{in})).
\end{align*}
\]

(6)

In equation (6), common parts are underlined that as fan-out are used.

**Proof.** The proof of synthesis of \( \text{Sum} \) output also can be done as follows (similar to [38]):

Using the majority function of \( C_{out} \):

\[
C_{out}' = a'b' + b'c_{in}' + a'c_{in}' = M(a', b', c_{in}').
\]

Then, \( \text{Sum} \) output can be rewritten as:

\[
\begin{align*}
\text{Sum} &= abc_{in} + ab'c_{in}' + acb_{in}' + a'b'c_{in} \\
&= a'((bc_{in} + ab + ac_{in}) + (bc_{in} + ab' + ac_{in})) \\
&+ (ab + ac_{in})'((bc_{in} + ab + ac_{in}) + (bc_{in} + ab' + ac_{in})) \\
&+ (ab + ac_{in}')(bc_{in} + ab + ac_{in}) \\
&+ (ab + ac_{in}')(bc_{in} + ab') \\
&+ (ab + ac_{in}')(bc_{in} + a') \\
&+ (ab + ac_{in}')(bc_{in} + b') \\
&+ (ab + ac_{in}')(bc_{in} + a'c_{in}') \\
&+ (ab + ac_{in}')(bc_{in} + b'c_{in}').
\end{align*}
\]

Also equation (6) can be rewrite as two other equations as the following:

\[
\begin{align*}
\text{Sum} &= M(C_{out}', b, M(a, b', c_{in})), \\
\text{Sum} &= M(C_{out}', c_{in}, M(a, b, c_{in}')).
\end{align*}
\]  

(7)

Three another form for synthesizing \( \text{Sum} \) output can be proposed as the following:

\[
\begin{align*}
\text{Sum} &= M(M(a, b, c_{in}')', M(a, b', c_{in}'), a'), \\
\text{Sum} &= M(M(a, b, c_{in}'), M(a', b', c_{in}'), b'), \\
\text{Sum} &= M(M(a', b, c_{in}'), M(a, b', c_{in}'), c').
\end{align*}
\]  

(8)

**Proof.** The proof of synthesizing of \( \text{Sum} \) output in equation (8) is as follows:

\[
\begin{align*}
\text{Sum} &= abc_{in} + ab'c_{in}' + a'bc_{in}' + a'b'c_{in} \\
&= a'((bc_{in} + ab + ac_{in}) + (bc_{in} + ab' + ac_{in})) \\
&+ (ab + ac_{in})'((bc_{in} + ab + ac_{in}) + (bc_{in} + ab' + ac_{in})) \\
&+ (ab + ac_{in}')(bc_{in} + ab + ac_{in}) \\
&+ (ab + ac_{in}')(bc_{in} + ab') \\
&+ (ab + ac_{in}')(bc_{in} + a') \\
&+ (ab + ac_{in}')(bc_{in} + b') \\
&+ (ab + ac_{in}')(bc_{in} + a'c_{in}') \\
&+ (ab + ac_{in}')(bc_{in} + b'c_{in}').
\end{align*}
\]

Figure 5 shows the schematic of the proposed symmetric irreversible full adder according to equation (6) without garbage outputs. As shown in this figure, this topology is symmetric, and we use from this new schematic for improving QCA layout. According to Figure 5 and Table 1, the new layout of the proposed symmetric reversible full-adder is presented in Figure 6. Due to the symmetric structure in designing of this layout, three clock phase are used which this feature is caused circuit delay is reduced. Also, this layout is planar and in one layer is implemented.

### 3.1.2 The proposed reversible full-adder/subtractor

In this section, a new design of reversible full-adder/subtractor is presented according to the method proposed for converting irreversible functions to reversible one. Designing of specification function is shown in Table 2. In this table, outputs of \( C_{out} \), \( \text{Sum/Sub} \) and \( B_{out} \) are considered as the main outputs and Gar1 is garbage output that is added for reversibility. In fact, in this specification function instead of using of two redundant outputs (garbage outputs), one of garbage outputs
in Table 1 is used as the main output for doing subtraction operation. In the other words, we used garbage output for specific aims (subtractor) and increased the efficiency of reversible function. Also, in this design, outputs Sum and Sub is considered as one output and outputs \( C_{\text{out}} \) and \( B_{\text{out}} \) is considered as separate. So, this feature is caused that in this structure, operations of adding and subtracting is done simultaneously. As a result, in this stage, also, propagation delay is reduced. Then, equal states in output are specified (showed with gray color in Tab. 2). Then as comparing with input columns, a column with the maximum number of removing of equal states in output is selected. In this function, garbage output is selected as same with input column \( a \). With adding this column and reviewing of output states is determined which one to one mapping between input and output have been created. The next step is synthesizing of outputs. \( C_{\text{out}} \) and Sum/sub output are synthesized as equation (6). Outputs of \( B_{\text{out}} \) and Gar1 can be obtained as the following:

\[
B_{\text{out}} = M(a', b, c), \quad \text{Gar} = a,
\]

where \( B_{\text{out}} \) output is common with Sum in term \( M(a', b, c) \). Schematic of this block is shown in Figure 7a.

According to Table 2 and Figure 5, the layout of symmetric reversible full-adder/subtractor is presented in Figure 7b. As shown in this figure and equations (6) and (9), in this structure, the garbage outputs (redundant outputs) are used as the main output for the specific application (subtractor). Then for reducing the number of majority gates, we used Sub output as a fanout in Sum output. So, this output does not add any additional gate and the structure is optimal. In addition, in this layout, symmetric introduced in Figure 5 exist and this feature is caused which layout be optimal in terms of occupational area and cell count. Also, this layout is implemented in one layer similarly with layout shown in Figure 6.

3.2 A proposed symmetric five-input majority gate

In this section, a novel design of the symmetric and planar structure of 5-input majority gate is presented as shown in Figure 8. The gate is fault tolerant owing to its symmetric structure. Additionally, all input cells have an inverting effect on polarizations of device cells. The new five-input majority gate is composed of 10 cells, five input cells, one output cell, and four device cells.

A three-input AND gate and also a three-input OR gate can be implemented using this majority gate by fixing two of the five input cells to +1 or −1, respectively.

3.2.1 The proposed reversible full-adder using five-input majority gate

In this section, an efficient reversible QCA full adder is presented and implemented based on the proposed five-input majority gate. The schematic design and layout of the proposed irreversible full-adder is presented in Figure 9. In addition, Figure 10 illustrates the layout of the proposed reversible full-adder, which uses a planner five-input majority gate. In this figure, the layout is designed using Table 1 and schematic introduced in Figure 9a. Also, due to the symmetric structure, the three clock phase are used in this schematic. So, the delay is reduced.

In practical, for applying inputs from outside of the device to the inside of it, a method is using a multilayer crossing wire technique as shown in Figure 3b. So, the proposed layouts can easily be implemented in practice.

3.2.2 Fault tolerance analysis

A function of fault-tolerant QCA gate should work correctly in cases where one or more of the cells are misaligned or misplaced. The first fault is due to displacement of the cell from their intended location. The QCA cell displaced will be outside the radius of effect of its neighbor, so that no longer contributing to the interaction among the cells exists.

The interaction between cells exists up to typical maximum distance 40–60 nm. To assess displacement and misalignment tolerance [19–21], a 3-input AND gate based on our proposed gate is designed and cells A, B and C are displaced and misaligned in it. Figure 11 shows the possible defects which may occur for cell A (The green cells depict the possible locations of a displaced or misaligned A.). The obtained results are summarized in Table 3.

3.3 Reversible 8-bit full-adder/subtractor

In this section, three of the 8-bit full-adder/subtractor(s) are designed using adder/subtractor blocks proposed in the previous section. These circuits are a combinational circuit which performs arithmetic addition and subtraction with binary digits. This circuit is composed of eight reversible full-adder/subtractor blocks as series connections. Figures 12a and 12b show schematics of reversible 8-bit full-adder and reversible 8-bit full-adder/subtractor using adder blocks proposed in the previous section, respectively. For creating a reversible 8-bit

| Table 2. Designing of new reversible full-adder/subtractor. |
|-------------------------------------------------------------|
| \( a \) | \( b \) | \( c_{\text{in}} \) | \( C_{\text{out}} \) | Sum/Sub | \( B_{\text{out}} \) | Gar1 |
|------|------|-------|-------|--------|--------|------|
| 0    | 0    | 0     | 0     | 0      | 0      | 0    |
| 0    | 0    | 1     | 0     | 1      | 1      | 1    |
| 0    | 1    | 0     | 0     | 1      | 0      | 0    |
| 0    | 1    | 1     | 1     | 0      | 1      | 1    |
| 1    | 0    | 0     | 0     | 1      | 0      | 0    |
| 1    | 0    | 1     | 1     | 0      | 0      | 0    |
| 1    | 1    | 0     | 1     | 0      | 0      | 0    |
| 1    | 1    | 1     | 1     | 1      | 1      | 1    |

Figure 8. The gate is fault tolerant owing to its symmetric structure. Additionally, all input cells have an inverting effect on polarizations of device cells. The new five-input majority gate is composed of 10 cells, five input cells, one output cell, and four device cells.
full-adder/subtractor in Figure 12b, multiplexer blocks $2 \times 1$ are used for detecting the addition or subtraction operations in each time. With selecting state “zero”, add operation is done, and if state “one” is selected, the subtraction operation is done.

The three QCA layout of 8-bit reversible full-adder/subtractor(s) are shown in Figure 12. Figures 13a and 13b show the layout of 8-bit reversible-full adders using adder blocks proposed in Figures 6 and 10, respectively. Figure 13c show the layout of 8-bit reversible full-adder/subtractor using adder/subtractor block proposed in Figure 7. The proposed 8-bit reversible full-adders/subtractors consists of 570, 725, 1040 cells covering an area of 0.55, 0.68, 1.12 $\mu m^2$ in Figures 13a, 13b and 13c respectively.
Table 3. Results of cell displacement and misalignment of cell A (C) and B, separately.

| Cell  | C behaves mirrorly similar to cell A in all directions |
|-------|------------------------------------------------------|
| Move A to North | Move A to South | Move A to West | Move A to East |
| 0 ≤ d ≤ 5 | 0 ≤ d ≤ 8 | 0 ≤ d ≤ 6 | 0 ≤ d ≤ 10 |
| Normal function | Normal function | Normal function | Normal function |

Cell B

| Move B to North | Move B to South | Move B to West | Move B to East |
|----------------|----------------|----------------|---------------|
| 0 ≤ d ≤ 6 | 0 ≤ d ≤ 5 | 0 ≤ d ≤ 5 | Not possible |
| Normal function | Normal function | Normal function | Normal function |

Fig. 12. (a) Logic block of 8-bit reversible full-adder. (b) Logic block of 8-bit reversible full-adder/subtractor.

Fig. 13. QCA layout of (a) 8-bit reversible full-adder using structure proposed in Figure 6. (b) 8-bit reversible full-adder using structure proposed in Figure 10. (c) 8-bit reversible full-adder/subtractor using structure proposed in Figure 7.
Fig. 14. Simulation results. (a) Proposed reversible adder. (b) Proposed reversible adder/subtractor. (c) Proposed reversible adder with five-input majority.

Fig. 15. Simulation results. (a) Irreversible Adder proposed with five-input majority gate. (b) Three-input AND
Table 4. Settings of QCA designer.

| Parameter type                  | Value       | Parameter type                  | Value       |
|---------------------------------|-------------|---------------------------------|-------------|
| Cell size                       | 18 nm       | Clock high                      | 9.8e-22     |
| Number of samples               | 12800       | Clock low                       | 3.8e-23     |
| Convergence tolerance           | 0.001000    | Clock amplitude factor          | 2.000       |
| The radius of effect            | 65 nm       | Layer separation                | 11.5 nm     |
| Relative permittivity           | 12.9        | Maximum iterations per sample   | 100         |

Table 5. Comparison of QCA reversible full-adder designs.

| Reversible functions     | Constant inputs | Garbage outputs | Complexity (cell amount) | Area (µm²) | Clocking zones (delay) | Num of majority gates | Num of NOT gates | Control inputs |
|---------------------------|-----------------|-----------------|--------------------------|------------|------------------------|-----------------------|-----------------|----------------|
| Previous design [30]     | 0               | 2               | 399                      | 0.5        | 8                      | 9                     | 13              | 3              |
| Previous design [29]     | 0               | 3               | >300                     | 0.361      | 6                      | 6                     | 6               | 0              |
| Proposed QCA full-adder  | 0               | 2               | 48                       | 0.04       | 3                      | 3                     | 2               | 0              |
| Proposed full-adder/sub  | 0               | 2               | 48                       | 0.04       | 3                      | 3                     | 2               | 0              |
| Proposed full-adder with five-input majority gate | 0 | 2 | 58 | 0.04 | 3 | 2 | 2 | 0 |

Table 6. Comparison of QCA irreversible full-adder designs.

| Irreversible functions     | Complexity (cell amount) | Area (µm²) | Clocking zones (delay) | Layers |
|-----------------------------|--------------------------|------------|------------------------|--------|
| Previous design [22]        | 145                      | 0.17       | 5                      | 1      |
| Previous design [18]        | 86                       | 0.10       | 3                      | 2      |
| Previous design [20]        | 73                       | 0.04       | 3                      | 2      |
| Previous design [21]        | 52                       | 0.04       | 3                      | 2      |
| Proposed QCA full-adder     | 46                       | 0.04       | 3                      | 1      |
| Proposed full-adder/sub     | 46                       | 0.04       | 3                      | 1      |
| Proposed full-adder with five-input majority gate | 52 | 0.04 | 3 | 1 | 1 |

Table 7. Comparison 8-bit reversible adders/subtractors in QCA.

| Complexity (cell amount) | Area (µm²) | Clocking zones (delay) |
|--------------------------|------------|------------------------|
| Previous design (not reversible) [42] | 5786 | 10.47 | 109 |
| Previous design [30]     | 5489       | 10.07                  | 92           |
| Proposed QCA 8-bit reversible full adder (1) | 570 | 0.55 | 32 |
| Proposed QCA 8-bit reversible full adder (2) | 725 | 0.68 | 32 |
| Proposed QCA 8-bit reversible full adder/subtractor | 1040 | 1.12 | 42 |

4 Results

In this section, the first simulation results of the proposed circuits are presented. Then, in the next section, a comparison between the best-obtained results are done.

4.1 Simulation results

For the proposed circuit layouts and functionality checking, a simulation tool for QCA circuits, QCA Designer version 2.0.3 [37,39] is used in a bistable approximation [4,18,40,41]. QCA Designer is a tool used to create a layout and accurate simulation for QCA circuits that can run on most platforms. Parameters used in this software are shown in Table 4.

Simulation results of proposed reversible designs are shown in Figure 14. Also, Figure 15 depicts simulation results of irreversible adder and AND constructed using the five-input majority gate.

4.2 Comparison results

The proposed full-adders are compared with the previous works and the results are illustrated in Table 5. To demonstrate performance of proposed designs, we compare them with irreversible designs in Table 6. Also, the proposed 8-bit reversible full-adders/subtractors are compared in Table 7. It can be seen that the proposed reversible/irreversible full adders are more efficient in terms of area, complexity, delay, reversible/irreversible
layout, and also in logic level in terms of garbage outputs, control inputs, number of majority and NOT gates compared to the best previous works in reversible [29, 30] and irreversible [18, 20–22] and [30, 42] for 8-bit reversible full-adders/subtractors. In fact, Table 6 show which our results are even better when results of proposed reversible full-adders/subtractors are compared with the section of irreversible adders.

5 Conclusion

In this paper, three new design of reversible full-adder/subtractor(s) was introduced in QCA technology in logical and layout levels. one of the proposed structures was based on the new structure proposed for five-input majority gate. These structures have features such as planar, symmetric and fault-tolerant in layout level. A fault-tolerant analysis was presented for five-input majority gate. In continuing, based on proposed structures, three new 8-bit reversible full-adder/subtractors was designed. The layouts and functionality checks were done using QCA Designer and the designs was compared to the best previous QCA adder designs and shows considerable improvements in terms of area, complexity, delay, reversible/irreversible layout, and also in logic level in terms of garbage outputs, number of majority, NOT gates and power conception due to reversibility. These circuits can be used in processors with high operating speeds.

Author contribution statement

Moein Sarvaghad-Moghaddam contributed the idea and performed the simulations. Ali A. Orouji checked the simulations and supervised the general structure of the paper. All authors contributed to discussion and reviewed the manuscript.

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