MULTI LOOP SEPIC CONVERTER BASED POWER FACTOR CORRECTION WITH HYSTERESIS CURRENT CONTROL TECHNIQUE

A. John Britto¹, J. Jawahar Babu², R.Vinoth³, and K.Sujesh Kumar⁴

¹Assistant Professor, Department of Electrical and Electronics Engineering, Anna college of Engineering and Technology, Kumbakonam, India.
²Assistant Professor, Department of Electrical and Electronics Engineering, TRP Engineering College, Trichy, India,
³Assistant Professor, Department of Electrical and Electronics Engineering, Er. Perumal Manimekalai College of Engineering, Hosur, India.
⁴Kombolcha institute of technology (kiot,) Department of Electrical and Computer Engineering, Ethiopia.

Abstract—In this paper, multiloop interleaved control (MISEPIC converter) in SEPIC converter is proposed, and it is combined with conventional multiloop control and the interleaved pulse width modulation scheme. The average behavior of the interleaved three-level switch-mode rectifier (SMR) behaves similar to the conventional boost-type SMR even though two capacitor voltages are imbalanced. It implies that conventional Multiloop control can be applied to the interleaved three-level SMRs to achieve the desired power factor correction function and PI control is used to maintain the voltage to the load. The proposed MISEPIC converter is digitally implemented and verified in matlab simulation.

Keywords- SEPIC Converter, hysteresis controller, PI controller, MISEPIC converter.

I. INTRODUCTION

Power factor is the value of a system that reflects how much power is being borrowed from the power company for the system. Quantitatively, power factor ranges from zero to one and is the cosine of the difference in the angle between the current and voltage. Poor power factors are due to inductive loads such as the induction motors found in air conditioners and refrigerators. According to Pacific Gas & Electric Company, about 60% of all loads in the United States are electric motors. This fact in combination with the United States Energy Information Administration (EIA) statistic of only about 25,000 out of 200,000 manufacturing companies participating in power factor correction, illustrates a need for companies to implement power factor correction devices to improve efficiency and reduce energy waste. One incentive for companies to install power factor correction devices is the charges that many utility companies impose for falling below a certain power factor. For example, Ameren Illinois requires customers to install power factor correction devices on their system if the power factor falls below 0.85. If the customer does not install any devices then Ameren can actually come out to the customer’s property and install devices themselves and charge the customer a hefty rate for doing so.[1]. Pacific Gas & Electric (PG&E) charges 0.6% for each percentage point of power factor below 0.85 on a utility bill. So if a customer’s utility bill is $10,000 and has an average power factor of 0.83 for the month, the customer would be charged 1.2% of the total bill more because of that low power factor. PG&E also provides an incentive to maintain a power factor above 0.85 as well. If a customer has a power factor above 0.85 the customer receives a credit equal to the process described above instead of a charge. There are also a couple of reasons for power companies to be concerned with low power factor. One of the most important reasons they are concerned is the power losses that occur through their transmission lines or the “I squared R losses.” This is power that the customer never uses and is not charged for. This is a problem both for generating and distribution companies as a distribution company might be charged for running at a low power factor in their system by a generating company.[6]. These charges incurred are also important for keeping power companies’ rates low to remain competitive. With several power
companies offering incentives and most power companies charging some type of fee for falling below their specified power factor, some may wonder why companies do not actively pursue to improve their power factor. This can be due to several factors. One is that the companies’ administrators do not think the company will be able to recover costs from installing power factor correction devices. Another is that some companies might not have enough inductive loads to be concerned about power factor at all. Power factor correction acts to improve poor power factors by keeping a customer’s power factor above the level specified by the power company. The most common method of controlling power is by the use of switching capacitor banks and was the method implemented in this project. Capacitor banks generate “negative” reactive power or absorb the reactive power produced by inductive loads. However, it is possible to add too much capacitance to the system and still incur power company charges. This occurs when the amount of capacitance added is so much greater than the inductance of the system that the power factor goes below 0.85 leading. The goal of this project was to obtain a power factor as close to one as possible or to control the system power factor within a range that will avoid any power company charges possible.[7]

The attention devoted to the quality of the currents absorbed from the utility line by electronic equipment is increasing due to several reasons. In fact, a low power factor reduces the power available from the utility grid, while a high harmonic distortion of the line current causes EMI problems and cross-interferences, through the line impedance, between different systems connected to the same grid. From this point of view, the standard rectifier employing a diode bridge followed by a filter capacitor gives unacceptable performances. Thus, many efforts are being done to develop interface systems which improve the power factor of standard electronic loads. An ideal power factor corrector should emulate a resistor on the supply side while maintaining a fairly regulated output voltage. In the case of sinusoidal line voltage, this means that the converter must draw a sinusoidal current from the utility; in order to do that, a suitable sinusoidal reference is generally needed and the control objective is to force the input current to follow, as close as possible, this current reference. Hysteresis current control method is used due to its better performance in obtaining a sinusoidal input current. Its advantages are no need of compensation ramp and low distorted input current waveforms. According to this control technique, the switch is turned on when the inductor current goes below the lower reference and is turned off when the inductor current goes above the upper reference giving rise to a variable frequency control. The proposed control technique is adapted to the hysteresis current control technique. Unity power factor and tight output voltage regulation are achieved with the very well known two stage approach, shown in Fig. 1. Since the power stage is composed by two converters, size, cost and efficiency are penalized, mainly in low power applications. However, this is probably the best option for ac-dc converters due to the following reasons.

1) Sinusoidal line current guarantees the compliance of any Regulation.
2) It gives good performance under universal line voltage.
3) It offers many possibilities to implement both the isolation between line and load, and the hold-up time.
4) The penalty on the efficiency due to the double energy processing is partially compensated by the fact that the voltage on the storage capacitor is controlled. The fact of having a constant input voltage allows a good design of the second stage.

![Diagram](https://via.placeholder.com/150)

*Fig 1. Boost converter based PFC correction*
II. SEPIC CONVERTER

SEPIC converter is the Single-ended primary-inductor converter (SEPIC) is a type of chopper that has two inductors L1 & L2. Capacitors C1&C2 the diode D will protect the source from back emf. Similar to the buck boost converter it will do both buck and boost operation. The series inductor L1 will provides continuous input current, when the duty cycle is less than 0.5, it will works in discontinuous mode, that means buck mode so that the output voltage is less than input voltage. When the duty cycle is greater than 0.5, it is in continuous mode that means boost mode. So that output voltage is greater than input voltage.

![Fig 2. Single Ended Primary Inductance Converter](image)

The PWM pulse is control the output of the SEPIC converter. In this SEPIC converter the output voltage is non inverted so that it overcomes the drawbacks of buck boost and cuk converter. The input power factor becomes unity due to this continuous input current. The SEPIC converter have internal protection that has provided by the diode D, so it does not require any snubber protection.

III. THREE LEVEL SEPIC CONVERTER BASED PFC SCHEME

The single phase AC voltage is given to the diode bridge rectifier circuit. It will convert the AC voltage into uncontrolled DC voltage. This voltage is given to the proposed multiloop interleaved controller it will boost up the voltage and this constant voltage is given to the load.

The proposed MISEPIC converter shown in Fig. 4.2 combines the conventional multiloop control, the feed forward loop, and the interleaved PWM scheme. Both the voltage controller and the current controller are proportional–integral-type controllers. Two gate signals GT1 and GT2 are generated from the comparisons of control signal vcont3 and two unit saw tooth signals vtri1 and vtri2, respectively. It is noted that the two saw tooth signals have unit amplitude and identical period Ts; however, there is a 180° phase difference between them. Both duty ratios of switches SW1 and SW2 are equal to the MISEPIC converter control signal vcont3. Due to input inductor L and diodes D1 and D2 in the three level SMR, both switches are turned on at the same time. Therefore, there are four possible switching states in the operation of the interleaved three-level SMR, both switches turn on at switching state 1. Thus, inductor voltage vL3 in the three-level SMR equals the rectified input voltage vL3 = |vs|, and both capacitors supply energy to the load iC1 = iC2 = −id. At switching state 2 the upper switch turns on, and the lower switch turns off. The resulting inductor voltage vL3 = |vs| − vd2 equals the difference between the rectified input voltage |vs| and capacitor voltage vd2. Additionally, capacitor C1 supplies energy to the load iC1 = −id; however, capacitor C2 stores the energy from input source iC2 = iL3 − id. Similarly it is equal to the rectified input voltage minus the upper capacitor voltage vL3 = |vs| − vd1. At switching state 3, the upper capacitor C1 is charging iC1 = iL3 − id, but the lower capacitor C2 is discharging iC2 = −id. When both switches turn off in the resulting inductor voltage equals the rectified input voltage minus the output voltage,
The rectified input voltage $|v_s|$ supplies the load and charges both capacitors $iC_1 = iC_2 = iL_3 - id$. The analysis of the three-level converter can be divided into two conditions. One condition is $v_{cont3} > 0.5$, and the other condition is $v_{cont3} < 0.5$. When control signal $v_{cont3}$ is larger than 0.5, both duty ratios of the switches are larger than 0.5, and their conducting times are $v_{cont3}Ts$. However, there is a time difference $Ts/2$ between their turning-on instants. Therefore, the times taken by switching state 2 and switching state 3 are $(1 - v_{cont3})Ts$. The remaining time for switching state 1 is $(2v_{cont3} - 1)Ts$ because each switching period is $Ts$. By applying the average method, the average inductor voltage $v_{L3}$ in this condition can be expressed as

$$vL3 = |v_s| - vd = |v_s| - vd1 - vd2$$

(1)

where output voltage $vd$ is the sum of the two capacitor voltages

$$vd = vd1 + vd2.$$  

(4)

$v_{cont} < 0.5$: both duty ratios of the switches are smaller than 0.5, and both times taken by switching state 2 and switching state 3 are $v_{cont3}Ts$. Thus, the time for state 4 is $(1 - 2v_{cont3})Ts$. It follows that the average inductor voltage $v_{L3}Ts$ in this condition is $v_{L3}$

$$Ts = (|v_s| - vd1) v_{cont3} Ts + (|v_s| - vd2) v_{cont3} Ts + (|v_s| - vd) (1 - 2v_{cont3})Ts$$

(5)

From (11) and (12), it can be found that whether control signal $v_{cont3}$ is larger or smaller than 0.5, the average inductor voltage $v_{L3}Ts$ is always equal to $v_{L3}Ts = |v_s| - (1 - v_{cont3})vd$ even though two capacitor voltages are imbalanced $vd1 = vd2$. Additionally, the result $v_{L3}Ts = |v_s| - (1 - v_{cont3})vd$ is the same as the average inductor voltage, which shows that the three-level SMR behaves similar to a conventional boost-type SMR even though two capacitor voltages are imbalanced. Therefore, the conventional multiloop control can be integrated into the proposed MISEPIC CONVETRER to achieve the same PFC function for the three-level SMR. Due to the same average inductor voltage $v_{L3}Ts$, the control signal $v_{cont}$ by the multiloop control in can be extended to the MISEPIC CONVETRER control signal $v_{cont3}$, i.e.,

$$v_{cont3} = v_{cont} = 1 - Vs \left| \sin(2\pi f_t) \right|Vd.$$  

(6)

Fig 3. Proposed three level SEPIC converter based PFC correction
Fig 4. Modes of operation

The voltage ripple in capacitor voltage $v_{d1}$ is smaller than that in voltage $v_{d2}$, which shows that the waveforms are measured under the capacitance-mismatched condition. Capacitor voltage $v_{d1}$ quickly drops the voltage due to the connected resistor, and capacitor voltage $v_{d2}$ increases the voltage due to the voltage control loop. After removing the connected resistor, two capacitor voltages are gradually balanced. Therefore, the three-level SMR with the proposed MISEPIC converter possesses the ability to balance the capacitor voltages; however, it takes several seconds to balance the voltages. For the three-level SMR, the measured power loss, efficiency, and power factor. From
the three-level SMR yields less power loss than the conventional boost-type SMR, and the former possesses higher efficiency than the latter. It clearly shows that the three-level SMR possesses higher efficiency than the conventional boost-type SMR. In addition, the current ripple in the three-level SMR is smaller than that in the conventional SMR, and the power factor of the three-level SMR is higher than that of the conventional SMR. The results show that the proposed MISEPIC converter is able to work at high line voltages. From the provided simulation and experimental results, the proposed MISEPIC converter is able to achieve the PFC function without adding the voltage balancing control loop. The results show that the three-level SMR in ac/dc applications takes several seconds to automatically balance the capacitor voltages. Because the time taken to balance the voltages is several seconds in this case, adding the voltage balancing loop is sometimes required. Furthermore, some other simulations and experiments for the three-level boost converter in dc/dc applications had been done; however, the results show that the converter is not able to balance the capacitor voltages automatically without the voltage balancing control loop. Hence, the proposed simple MISEPIC converter cannot be extended to the three-level boost converter in dc/dc applications because the voltage balancing loop is still required.

**IV. SIMULATION RESULTS**

To verify the feasibility of the proposed strategy, simulations are carried out.

![Proposed system simulation](image-url)
Fig. 6 Proposed input AC voltage to the DBR

Fig. 7 Proposed input AC current due to the DBR

Fig. 8 Proposed system SEPIC converter input voltage waveform
Fig. 9 Proposed system SEPIC converter PWM pulse waveform

Fig. 10 Proposed system SEPIC converter output voltage waveform

Fig. 11 Proposed input AC current due to the SEPIC converter
The figure 12 shows the THD value, the SEPIC converter will reduce THD by providing constant voltage to the load.

V. CONCLUSION

In this project, the results show that the interleaved three-level SMR with the interleaved PWM scheme behaves similar to a conventional boost-type SMR. Its performance of the current shaping function does not degrade even when the two capacitor voltages are imbalanced. The MISEPIC converter for the three-level SMR in ac/dc applications has been first proposed. The proposed MISEPIC converter is implemented. The measured results show that the proposed MISEPIC converter is able to achieve the desired PFC function, and the capacitor voltages are automatically balanced without adding the voltage balancing loop. The commercial PFC ICs have the multiloop function but do not integrate the voltage balancing loop. However, based on this project, the commercial PFC ICs can be used in the three-level SMRs if the temporary voltage imbalance is acceptable during the system operation. The results are verified using matlab simulation.

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