A Fully-Integrated Ambient RF Energy Harvesting System with 423-µW Output Power

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Abstract: This paper proposes a 2.4-GHz fully-integrated single-frequency multi-channel RF energy harvesting (RFEH) system with increased harvested power density. The RFEH can produce an output power of ~423-µW in harvesting ambient RF energy. The front-end consists of an on-chip impedance matching network with a stacked rectifier concurrently matched to a 50 Ω input source. The circuit mitigates the “dead-zone” by enhancing the pumping efficiency, achieved through the increase of $V_{gs}$ drivability of the proposed internal gate boosting 6-stage low-input voltage charge pump and the 5-stage shared-auxiliary-biasing ring-voltage-controlled-oscillator (VCO) integrated to improve the start-up. The RFEH system, simulated in 180-nm complementary metal–oxide–semiconductor (CMOS), occupies an active area of 1.02 mm$^2$. Post-layout simulations show a peak power conversion efficiency (PCE) of 21.15%, driving a 3.3-kΩ load at an input power of 0 dBm and sensitivity of −14.1 dBm corresponding to an output voltage, $V_{out,RFEH}$ of 1.25 V.

Keywords: RF energy harvesting (RFEH); CMOS; RF-DC; DC-DC; charge pump; clock generator; ring-VCO; shared-dynamic-biasing

1. Introduction

Ubiquitous wireless sensor nodes (WSNs), body sensor nodes (BSN), and portable health monitoring devices will require energy harvesting (EH) to achieve battery-less or long-term battery-assist operation. RF Energy Harvesting (RFEH) [1–7] is gaining interest due to its continuous availability in urban environments compared to other renewable energy sources like solar, thermal, and piezo EH. In an indoor environment, the RF signal is concentrated, and in the outdoor environment the weather, season, and illumination have less impact around 0.0001 to 0.004 dB/m as propagation attenuation of EM waves [2]. In addition, the RFEH system conciliates well with existing wireless systems with a standard 50-Ω impedance matching network, requiring only an antenna as a transducer [8]. Most modern communication devices enable Wi-Fi or Bluetooth low-energy (BLE), hence, RF energy is abundant and the 2.4-GHz frequency band is of interest to achieve a small physical form factor as well as a low-cost solution for RFEH [8]. According to the International Telecommunication Union (ITU), global Wi-Fi growth increased by 80% after the first quarter of 2020 [9]. Hence, the power density of the wireless frequency in this channel [10] increased and we can drain it to overcome the limitation due to the low input power density of the RFEH in improving the system’s energy reliability. In complementing the RFEH, the
power consumption of various portable devices operates within the hundreds of μW range for the detection of symptomatic patterns in audio biological signals [11], ECG [12,13], and other health monitoring [14]. Table 1 shows the typical range of the power consumption of various electronic devices.

Table 1. The typical range of the power consumption of various electronic devices [15,16].

| Power    | 1 μW        | 10 μW       | 100 μW      | 1 mW  |
|----------|-------------|-------------|-------------|-------|
| Device   | 32 kHz Quarts oscillator | Wearable, Calculator, Passive RFID | Hearing Aid, Sensors [12,13] | Active RFID, Miniature FM receiver, Health monitoring [14] |

The usage of multi-channel RFEHS not only has the potential to improve the performance of the harvester but also increases the harvesting sensitivity [17], and supports a multiple-input multiple-output (MIMO) system [18,19]. Various multi-channel, multi-band RFEH systems adopting discrete elements require off-chip components [1,4,10,17–20], which include Schottky diodes [15] and rectenna [21]. Figure 1 presents the simple block diagram of the proposed RFEH system, which includes an on-chip impedance matching network (IMN), a stacked rectifier, and a charge-pump-based DC-to-DC converter with the developed shared-auxiliary-biasing ring-voltage-controlled-oscillator (SAB-RVCO). The array of antennas receives the available RF energy from the free space environment. The rectifier converts the time-varying electromagnetic RF signal to a DC voltage. The impedance matching network (IMN) interfaces the antenna (typically 50 Ω) and rectifiers to reduce impedance mismatch which in turn minimizes the power reflection. However, the physical form factor of the discrete components occupies a huge space, this limits the EH in the targeted WSN, BSN, and health care application. To overcome the aforementioned challenges, recent research directions changed towards solutions on-chip or with full integration. The primary scope of the proposed work is to increase the higher power density with higher power conversion efficiency and higher sensitivity for an on-chip solution.

Challenges of the on-chip IMN solution: IMN in RFEHS is built with capacitors and high Q-inductors for voltage amplification and maximum power transfer [22–28]. However, designing a high Q-inductor in complementary metal–oxide–semiconductor (CMOS) technology has its limitations and trade-offs in attaining maximum power conversion efficiency [29].

To overcome the aforementioned challenges of an on-chip IMN design, we present the following findings: (1) Through the investigation of the on-chip impedance matching technique for the RFEH system [30,31], this work proposes a design strategy that adopts the variation of the rectifier input impedance and devises a technique for the area reduction along with performance enhancement. (2) To increase the sensitivity of the RFEH system, we also put forward a low-power, non-overlap-clock shared-auxiliary-biasing ring-voltage-controlled-oscillator (SAB-RVCO) and the proposed internal gate biasing charge pump. By using a novel body-biasing technique, the SAB-RVCO can generate a non-overlap clock.
at low supply headroom and improve the pumping efficiency of the charge pump. The design of the proposed SAB-RVCO uses a dual-input RFEH system achieving single-chip integration and an overall low-power consumption for the harvester.

This paper reports a dual-channel fully-integrated RFEH system that consumes a total chip area of 1.02-mm² in 180-nm CMOS. With the proposed dual-channel scheme, the circuit exhibits a higher power density of 423 µW at 0-dBm input power. Section 2 describes the overview of the proposed fully-integrated RFEH system. Section 3 presents the IMN design strategy and circuit-level design of the SAB-RVCO along with the charge-pump circuits. We also discuss the control circuit adopted in the RFEHS. Section 4 highlights the post-layout simulation results of the RFEHS and Section 5 concludes the work.

2. System Architecture

Figure 2 outlines the conceptual block diagram of a fully-integrated dual-input RFEH system. Two differential antennas configured at the same frequency will scavenge RF power to increase the harvesting input density. The integrated rectifier has a highly-efficient differential drive similar to [32]. The proposed rectifier is cascaded in a $3 \times 3$ stage to achieve high efficiency and low input impedance. An on-chip differential LC-matching is adopted and realized in a fully-integrated system.

Figure 2. Block diagram of fully-integrated dual-input RF energy harvesting (RFEH) system.

The proposed system consists of two power paths controlled by the control unit incorporating two MOSFET switches, an inverter, and a common-gate input comparator. Figure 2 shows the primary power path (PPP) as well as the secondary power path (SPP) which harvests high power directly to the load unit and low power to the storage unit in
extending the lifetime of the battery. The comparator weighs the rectifier output voltage \( V_{\text{rec}} \) and the reference voltage \( V_{\text{ref}} \). As long as \( V_{\text{rec}} \) is greater than \( V_{\text{ref}} \), the comparator output voltage \( V_{\text{cmp}} \) is low and the inverter output will be high.

This activates the PPP in which the control unit selects switch \( S_1 \) (HIGH) to turn on and \( S_2 \) (LOW) to turn off. This in turn increases the PCE of the RFEH system during the high power mode. Similarly, if the comparator weighs in \( V_{\text{rec}} \) to be lower than the \( V_{\text{ref}} \), the voltage \( V_{\text{cmp}} \) becomes high and inverter output is low, hence the control unit switches \( S_1 \) to turn-off and \( S_2 \) to turn-on. This operation activates the SPP of the RFEHS. In short, this mode benefits in increasing the sensitivity of the RFEH system through the proposed charge pump.

3. Circuit Details

3.1. Rectifier

The proposed RFEH system uses a customized differential cross-coupled (DCC) [33] rectifier with three-stage series with three parallel stages to achieve impedance transformation, which is discussed in detail in Section 3.2. The proposed rectifier attains higher PCE at low input power compared to the conventional diode-connected single-ended rectifier topology. The rectifier is configured with the transistors \( M_{\text{DP1}}, M_{\text{DP2}}, M_{\text{DN1}}, \) and \( M_{\text{DN2}} \) which are actively biased with differential signals \( V_{\text{RF+}} \) and \( V_{\text{RF-}} \) as shown in Figure 3. When \( V_{\text{RF+}} \) is negative and \( V_{\text{RF-}} \) is in a positive cycle, the transistor \( M_{\text{DN1}} \) is forward biased due to the positive gate voltage from \( V_{\text{RF-}} \) which reduces the on-resistance of \( M_{\text{DN1}} \). Alternately, when \( V_{\text{RF+}} \) is positive and \( V_{\text{RF-}} \) is in a negative cycle, \( M_{\text{DN1}} \) is reverse biased by a decrease in the gate voltage, and thus reduces the reverse leakage current. Previously-reported work on the fully-integrated RFEHS adopts a single-ended rectifier due to the size constraint of the on-chip inductor. The proposed RFEH system in this work is the first to couple the DCC rectifier with an on-chip matching network. In order to reduce the switching losses, an optimal number of fixed rectifier stages are used instead of reconfigurable stages.

![Figure 3. RFEH front-end: (a,b) Operation of differential cross-coupled (DCC) rectifier and (c) Proposed 3x3 rectifier.](image-url)
3.2. Impedance Matching Network

The design of the IMN network aims to match the rectifier to a standard 50 Ω source impedance. The equivalent model of the IMN circuit is shown in Figure 4. The voltage source with an amplitude of $V_{\text{Ant}}$ is integrated with the antenna resistance $R_{\text{Ant}}$, and with an IMN that consists of inductor $L_{\text{M1}}$, $L_{\text{M2}}$, and capacitor $C_{\text{M1}}$. In addition to impedance transformation to attain maximum power transfer, the IMN is also utilized for passive voltage amplification.

![Figure 4. Equivalent circuit of the RFEH front-end.](image)

The proposed IMN network introduces an impedance reduction technique, which consequently improves the Q-factor of the inductor. The realization of the IMN is evaluated through the input reflection coefficient, $S_{11}$, which is defined as,

$$S_{11} (\text{dB}) = \Gamma = \frac{Z_{\text{Rec}} - Z_{\text{Ant}}^*}{Z_{\text{Rec}} + Z_{\text{Ant}}^*}$$

where $Z_{\text{Rec}} = R_{\text{Rec}} + X_{\text{Rec}}$ is the impedance of the rectifier and $Z_{\text{Ant}}^*$ is the complex conjugate of $Z_{\text{Ant}}$, where $Z_{\text{Ant}} = R_{\text{Ant}} + X_{\text{Ant}}$ is the impedance of the antenna or source. The amount of power reflected is calculated through Equation (2),

$$|\Gamma|^2 = \left| \frac{Z_{\text{Rec}} - Z_{\text{Ant}}^*}{Z_{\text{Rec}} + Z_{\text{Ant}}^*} \right|^2$$

The passive voltage gain $A_v$ is directly proportional to the $Q_L$-factor of the inductor [30],

$$A_v = \frac{1}{2} \sqrt{1 + Q_L^2}$$

Based on Equation (3), $Q_L$ is a defining factor for voltage gain, which is directly proportional to the PCE of the RFEH system. At the operating frequency of 2.4 GHz in the 180-nm CMOS platform, the inductor quality (Q) factor is in the range of 8 to 1 for 6 nH to 22 nH of inductance. The Q-factor is limited beyond the defined range of inductance with the silicon chip area increasing proportionally with the inductor value. The conventional IMN design strategy is based on the rectifier’s optimal number of stages, hence the rectifier input impedance is fixed. The balanced or symmetry impedance matching is used to derive the circuit with the same impedance and effect of the signal traveling in both directions of the port.

An on-chip LC-match IMN is adopted as shown in Figure 5. The value of $C_m$ and $L_m$ can be approximated by [34],

$$C_m = \frac{1}{\omega_{\text{RF}} Z_{\text{Rec}}} \sqrt{\frac{Z_{\text{Rec}}}{Z_{\text{Ant}}^*} - 1}$$
where $\omega_{RF}$ represents the input RF frequency. The ideal simulated input impedance of the 3-stage series rectifier is $16.12 - j492.03 \Omega$, with the respective on-chip IMN component value at 2.4 GHz calculated as $L_{M1} = L_{M2} = 17.089 \text{nH}$ at a $Q$ of 3.15, and the capacitance $C_{M1} = 1.923 \text{pF}$. The computed component value corroborates with Equation (3) and reduces $A_v$ and the PCE of the system. The proposed system aims to improve the voltage gain by increasing the $Q$ of the inductor. In the proposed RFEHS, a 3-stage series rectifier is connected in parallel to reduce rectifier impedance, thus reducing inductance and improving the $Q$ factor as well as the passive voltage gain which concurrently improves the PCE and achieves a smaller silicon area. Figure 5 shows the impedance reduction scheme with a single 3-stage series rectifier, 2-parallel-3-stage series rectifier, and 3-parallel-3-stage series rectifier. The input impedance of the rectifier with 2 and 3 parallel stages is $9.78 - j246.68 \Omega$ and $7.59 - j165.08 \Omega$, respectively. This reduction of impedance improves the inductor $Q$ value to $\sim 6$ for two parallel stage rectifiers and 8 for 3-parallel stage rectifiers in the technology of choice. Similarly, a two-channel symmetrical system is designed with an on-chip impedance matching network.

![Figure 5. Impedance reduction strategy of RF front-end: (a) 3-stage rectifier, (b) 2 parallel—3-stage rectifier, and (c) 3 parallel—3-stage rectifier.](image-url)

### 3.3. Proposed SAB-RVCO

A step-up DC-DC converter is an essential unit in attaining high sensitivity for RFEHS. The capacitive-based step-up DC-DC converter or charge pump (CP) is best suited for an on-chip implementation in contrary to the inductor-based DC-DC converter which requires bulky off-chip components which is unfavorable for miniaturization of the device. The monolithic ring-voltage control oscillator (R-VCO) is the main peripheral of the charge
pump, where low-power and low start-up will be the key performance parameter for the RFEHS [30].

The primary bottleneck in designing a charge pump for the EH system is to achieve a low-power, low-startup RVCO as well as a non-overlap clock unit. In addition, the RVCO must be able to operate with a minimum supply voltage (\(V_{DD,\text{min}}\)), lower than the threshold voltage (\(V_{th}\)) of the transistor. These limitations are dependent on the subthreshold swing (\(S_s\)) of the CMOS process. The range of \(S_s\) is between 70 to 100 mV/decade with the advanced CMOS process node can achieve nearer to the Meindl limits [35]. The oscillation of RVCO must exhibit a rail-to-rail output with higher current drivability to drive the pumping capacitor of the CP. However, when \(V_{rec}\) is less than \(V_{th}\), the device limits the current flow due to weak inversion between source and drain channel, reducing the RVCO drivability. In a higher process node technology, the \(V_{th}\) of the device decreases, however, this, in turn, increases the production cost. Alternatively, the body bias technique favorably reduces the \(V_{th}\) and increases the device inversion region in lower process technology.

The \(V_{th}\) of an N-channel metal-oxide-semiconductor (NMOS) is expressed as [36],

\[
V_{th} = V_{to} + \gamma \left( \sqrt{2|\phi_F| + V_{sb}} - \sqrt{2|\phi_F|} \right)
\]  

(6)

where \(\gamma\) is the body-effect coefficient, \(\phi_F\) is the Fermi potential, \(V_{th}\) and \(V_{th0}\) are the threshold voltage and threshold voltage at zero source-to-bulk voltage (\(V_{sb}\)), respectively.

The deep-well technology enables the body bias technique which varies the \(V_{th}\) and allows a low voltage headroom operation. To minimize the \(V_{th}\) of the transistor, the \(V_{sb}\) is sourced with a higher voltage than the \(V_{gs}\) for NMOS and alternately sourced with a lower voltage than the \(V_{dd}\) for a P-channel metal-oxide-semiconductor (PMOS) device. This reduces the depletion region and increases the near saturation region operation, which in turn increases the saturation current and concurrently reduces the propagation delay. The commonly used body biasing technique includes the dynamic threshold-voltage MOSFET (DTMOS) [37], swapped body bias (SBB) [38], and auxiliary transistor [39]. In the DTMOS configuration, the gate terminal is connected to the body or bulk of the PMOS and is similar to an NMOS transistor. Hence, the \(V_{th}\) of the transistor changes dynamically concerning the gate-source voltage (\(V_{gs}\)) of the inverter. Assuming a single-stage inverter with DTMOS applied between the supply voltage (\(V_{dd}\)) and ground, if \(V_{gs}\) is low, then the bulk of both PMOS and NMOS should be low. Hence, \(V_{bs}\) of the PMOS and NMOS are driven to forward bias (\(V_{bsp} = -V_{dd}\)) and zero-bias (\(V_{bsn} = 0\)), respectively. If \(V_{gs} = V_{dd}\), then the bulk of both the PMOS and NMOS should be high, hence \(V_{bs}\) of the PMOS and NMOS are driven to zero-bias (\(V_{bsp} = 0\)) and forward bias (\(V_{bsn} = V_{dd}\)), respectively. In the SBB configuration, the bulk of the PMOS are connected to ground whereas the bulk of the NMOS transistors are connected to \(V_{dd}\), so that \(V_{bs}\) of both the PMOS and NMOS are driven to forward bias with \(V_{bsp} = -V_{dd}\) and \(V_{bsn} = V_{dd}\), respectively.

In an auxiliary transistor body biasing configuration, the bulk of the PMOS and NMOS transistor is connected with the drain voltage of the auxiliary NMOS and PMOS, respectively. This achieves a higher biasing voltage magnitude compared to other body biasing techniques. However, the additional transistor increases the size as well as the effect of the inherent parasitic, which causes a mismatch in the phase shifters and tends to degrade the CP pumping efficiency at low voltage [40].

The architecture of the proposed SAB-RVCO is shown in Figure 6a. With \(n\) representing the stage number, the core circuitry of the RVCO shown in Figure 6b consists of the transistor \(M_{PN}\) and \(M_{NN}\), two-phase shifters comprising of \(M_{SPN}, M_{SNN}, M_{CPN}\), and \(M_{CNP}\), which generate two-phase clocks \(\phi_1, \phi_1\), and \(\phi_2\). In the transistor’s weak-inversion region, the parasitic dominates, and the clock signals (\(\phi_1\) and \(\phi_2\)) overlap, which degrades the CP performance. To overcome this problem, transistors \(M_{PN}\) and \(M_{NN}\) are integrated to establish bulk-biasing for the RVCO and phase shifters. The bulk-biasing through \(M_{PN}\) and \(M_{NN}\) ensures \(\phi_1\) and \(\phi_2\) are non-overlap clock signals which improve the pumping efficiency of the charge pump when \(V_{DD}\) is low. The minimum size of the
device is maintained to achieve lower $V_{th}$ in RVCO while the dimension of the buffer is maximized by a systematic transistor sizing strategy [41] to drive the CP pumping capacitance approximating to 60 pF as well to minimize the rise-time and fall-time edge of the clock generation.

Figure 6. Details of the proposed 5 stages (N = 1, 2, ..., 5) RVCO: (a) RVCO for energy harvesting, and (b) Shared- auxiliary-biasing ring-voltage-controlled-oscillator (SAB-RVCO).

Figure 7 shows the schematic of the SAB-RVCO with two parallel phase shifter circuits. The number of stages (N) of the RVCO is attained based on the study of an effective number of stages relations with the frequency ($f_{Osc}$) [42], power consumption ($P_c$) [43], and losses of CP [30]. The oscillation of frequency and power is given by [42,43],

$$f_{Osc} = \frac{1}{N \cdot 2 \cdot t_d}$$  

$$P_c = N f_{Osc} C_L V_{DD}^2$$  

where the N is inversely proportional to the frequency and directly proportional to the power consumption [42]. It is worth noting that the frequency is directly proportional to the power consumption. Based on the inference from [30], higher frequency causes switching losses in the CP circuit. It is worth noting that switching losses are inversely proportional to the conduction loss. Hence the optimal 5-stages of the proposed RVCO achieve lower startup and higher efficiency, with lower parasitics effect, where N is the odd number of inverters (N = 5). The oscillation frequency of the RVCO is dependent on the time delay of each inverter stage, where the operation is shown in Figure 8a. Referring to Figure 7, in the SAB-RVCO, the bulk terminal of $M_{P1}$ and $M_{N1}$ are biased by the drain voltage of the auxiliary transistor $M_{NB1}$ and $M_{PB1}$, respectively. $M_{NB1}$ provides the initial voltage for the parasitic capacitance of the transistor $M_{P1}$ ($C_{db-p1}$, $C_{sb-p1}$) and $M_{NB1}$ ($C_{gd-nb1}$, $C_{db-nb1}$), where the parasitics of MOSFET are descriptively shown in Figure 8b. When $V_g$ of $M_{P1}$ is low, the drain voltage of $M_{NB1}$ pulls $V_{b-p1(t)}$ to the ground. This satisfies the initial condition of the bulk of $M_{P1}$.

$$V_{b-p1(0)} = V_d(0) - V_{dd}$$
When $V_{d(t)}$ falls too low, $V_{b-p1(t)}$ reduces below zero and reaches a negative value due to the discharge of capacitance $C_{db-p1}$ and $C_{gd-nb1}$. Alternately, when $V_{d(t)}$ reaches a high value, then $V_{b-p1}$ increases from a negative voltage to zero due to the charging of capacitance $C_{db-p1}$ and $C_{gd-nb1}$. During the process of charging and discharging the internal capacitance, $V_{b-p1(t)}$ is lesser than the source voltage of $M_{NB1}$, and no current flows between drain to source of $M_{NB1}$, hence, $M_{NB1}$ acts as capacitor $C_{gd-nb1}$. $M_{PB1}$ provides the initial voltage for the parasitic capacitance of the transistor $M_{N1}$ ($C_{db-n1}$, $C_{sb-n1}$) and $M_{PB1}$ ($C_{gd-pb1}$, $C_{db-pb1}$). When $V_g$ of $M_{N1}$ is high, the drain voltage of $M_{PB1}$ drives $V_{b-n1(t)}$ to $V_{dd}$. This satisfies the initial condition of the bulk of $M_{N1}$.

$$V_{b-n1 (0)} = V_d (0) + V_{dd} \quad (10)$$

When $V_{d(t)}$ is high, $V_{b-n1(t)}$ increases above $V_{dd}$ and reaches a positive value due to the charging of $C_{db-n1}$ and $C_{gd-pb1}$. Alternately, when $V_{d(t)}$ reaches a low value, $V_{b-n1}$ reduces from a higher positive value to $V_{dd}$ due to discharging of capacitor $C_{db-n1}$ and $C_{gd-pb1}$. During the process of charging and discharging the internal capacitance, $V_{b-n1(t)}$...
is higher than the source voltage of \(M_{PB1}\) and there is no current flow between drain to source of \(M_{PB1}\), hence the transistor \(M_{PB1}\) acts as capacitor \(C_{gd-pb1}\).

The auxiliary transistor acts as a capacitor during the charging and discharging phase that provides \(|V_{bs-n1}| \geq V_{dd}\) and \(|V_{bs-p1}| \leq 0\) compared to DT莫斯 and SBB, then RVCO operates in the sub-threshold region, the transistor current has an exponential relation with \(V_{bs}\) and a linear relation concerning the aspect ratio. By reducing the aspect ratio, the subsequent stage of the transistor’s internal capacitance \((C_o)\) should be smaller, which requires less drain to the source current which assists to maintain low power dissipation.

The auxiliary transistor biasing technique shows improvement in the performance of the RVCO, phase shifter, and buffer circuit. However, the design technique doubles the area by the ratio of 1:1 (Primary transistor: Auxiliary transistor), increasing the parasitics and leading to mismatch at the phase of the clock which is unfavorable for low voltage CP below 250 mV [40,44]. To reduce the inherent parasite and improve the area efficiency of the clock generation unit, a single set of the auxiliary biasing transistors is shared between the parallel stage of inverters which operates with similar logic behavior in a configuration as the 3rd and 2nd stages of the phase shifter cell are connected with the 3rd stage of the RVCO inverter cell. Through this vertical sharing bias technique, our work achieves an area reduction in a ratio of 3:1 without compromising the functionality. In addition, the proposed SAB-RVCO achieves a similar drain to source current with lower input voltage due to the higher biasing voltage magnitude.

### 3.4. Charge-Pump Realization

The capacitive charge pump (CP) is well adapted for monolithic implementation compared to the bulky inductor-based boost converter. In addition, the capacitive CP has a good driving capability, minimal parasitic effect, and low complexity well fitted for energy harvesting applications. The CP performance at low voltage relies on the charge transfer switching resistance, particularly in the Dickson CP operation. The NMOS is driven in the triode region, and for a latched CP configuration, both the NMOS and PMOS transistor are driven in the triode region. For simplicity of the expression, the on-resistance \((R_{on})\) of the NMOS transistor is given neglecting the short channel effect, \(R_{on} = \frac{1}{\mu C_{ox} W} (V_{gs} - V_{th})\) (11) where \(\mu\) is the mobility of the electron/holes and \(C_{ox}\) is the oxide capacitance which is a technology-dependent parameter. The CP resistance can be reduced by increasing the gate-to-source voltage \((V_{gs})\). The internal gate enhances overdrive voltage [45] and external clock boosting topology can provide 2 folds [46,47] or 3 folds [48] of input voltage for low voltage CP application. However, in most cases, the clock signal is equal to \(V_{dd}\) therefore, increasing the \(V_{gs}\) to greater than \(V_{dd}\) is a tangible solution observed from Equation (9). The proposed CP provides clock amplitude equal to \(2V_{gs}\) and achieves the primary goal of a CP circuit.

Figure 9 shows the proposed 6-stage CP with the operation of each cycle described as follows. Each stage of the proposed CP consists of PMOS \((M_{P1i}, M_{P2i}, B_{P1i}, B_{P2i})\), NMOS \((M_{N1i}, M_{N2i}, B_{N1i}, B_{N2i})\), pumping capacitor \((CP)\), and the boosting capacitor or \((C_p)\) where “\(i\)” represents the number of stages \((i = 1, 2, \ldots n)\).

The bulk terminal of both the PMOS and NMOS transistors are connected to the respective source terminal to eliminate the body effect. The clock signals \((\Phi_1, \Phi_2)\) which have a clock amplitude up to \(V_{dd}\), are applied to the complementary CP pumping capacitors of branch 1 \((B_1)\) and branch 2 \((B_2)\). These branches are connected in parallel to the supply and output nodes. In response to \(\Phi_1\) and \(\Phi_2\) signals, the pumping capacitors in \(B_1\) and \(B_2\) charge alternately with \(V_{dd}\), in a repetitive process as the charges are stored in the capacitors and transferred to the output \(V_{OUT,CP}\).
Figure 9. Schematic of the proposed charge pump: (a) operation in Cycle 1 (b) operation in Cycle 2.

The gate voltages of (MN$_{12}$, BN$_{22}$), (MN$_{22}$, BN$_{12}$), (MP$_{12}$, BP$_{22}$), and (MP$_{22}$, BP$_{12}$) are connected to the boosting capacitor through the nodes N$_{23}$, N$_{13}$, N$_{21}$, and N$_{11}$, respectively. In stage 2, the NMOS transistors are connected with the output node N$_{23}$, N$_{13}$ of the next immediate stage of the CP, and PMOS transistors are connected with the output node N$_{21}$, N$_{11}$ of the previous stage CP. This pattern of connection continues to the ($n - 1$)th stage. In the first stage, the gate voltage of the PMOS transistor is connected to the clock from the output node N$_{21}$, N$_{11}$ complimentary branches, due to the absence of a former stage. Besides, the $n$th stage has an additional pair of transistors with minimally sized capacitance to provide gate voltage for the $n$th stage NMOS transistor. To reduce leakage in the higher stage, the last three stages of the CP is constructed with thick oxide transistors, and the first three stages adopt nominal transistor for better conduction.

A performance comparison with the prior art is shown in Figure 10 where the charge pump output voltage is plotted versus time. However, to justify the performance, the conventional cross-coupled charge pump (CCCP) and the transistor-based Dickson charge pump (DCP) are recreated and simulated under the same test conditions by using similar transistor sizing, pumping capacitance, and other design parameters. It is evident that the proposed solution achieves the highest performance in the adopted lower technology node.
3.5. Control Circuit

The control circuit design is mandatory in the proposed architecture due to the configuration of two power paths. $S_1$ and $S_2$ are controlled by the common-gate comparator [49,50] and an inverter where the comparator is the main block in the control unit, which is shown in Figure 11. Yet, under low power mode, the device works in the sub-threshold region, where the current has an exponential relation respective to $V_{\text{ref}}$, indicating that it is negligible. As the adopted 180-nm CMOS is enabled via the long-channel device, this feature favorably results in a lower current consumption deviating from the low-current conduction of the transistor.

4. Post-Layout Simulation Results and Comparison

The proposed stack rectifier technique implemented along with the SAB-RVCO and charge pump is adopted in a fully integrated dual-input RF energy harvesting system and implemented in a 180-nm CMOS process shown in Figure 12, where the post-layout simulation result includes parasitic extraction of the parasitic capacitance, parasitic resistance, and parasitic inductance to create an accurate model of the circuit. Table 2 shows the transistor

![Figure 10](image-url)  
**Figure 10.** The transient output voltage of the proposed charge pump with prior art at $V_{\text{dd}} = 200 \text{ mV}$.

![Figure 11](image-url)  
**Figure 11.** Common-gate comparator.
sizing of the proposed system. The active chip area of the entire system is 1.02 mm$^2$ while the proposed SAB-RVCO consumes an active silicon area of 0.037 mm$^2$.

Figure 12. Chip Layout of the proposed RFEH System.

Table 2. The transistor sizing of the proposed fully integrated RFEH system.

| Device Parameter | Rectifier | RVCO |
|------------------|-----------|------|
| MDP              | 12 μ    | MP/MS/MCP |
| MDN              | 6 μ     | MN/MS/MCN |
| Cc               | 2 pF    | MPB    |
| MP               | 4 μ     | MNB    |
| MN               | 2 μ     | 6 μ |
| CP               | 5 pF    | 3 μ |
| BP               | 2 μ     |      |
| BN               | 1 μ     |      |

The PCE of the RFEH system can be calculated as $PCE_{sys} (%)$, with the general formula given as:

$$PCE_{sys} (%) = \frac{P_{out,main}}{P_{in,imn}} \times 100 = \frac{V_{out,main}^2}{P_{in,imn}} \times 100$$  \hspace{1cm} (12)

where $P_{out,main}$ is the output power delivered to the load system, and $P_{in,imn}$ is the input power received at IMN. However, the PCE of the primary path is sufficient to benchmark with the other reported work.

In other words, the system PCE is predominantly determined by the efficiency of IMN ($\eta_{IMN}$), rectifier ($\eta_{rect}$), and PMU ($\eta_{PMU}$).

$$\eta_{System} = \eta_{IMN} \times \eta_{Rectifier} \times \eta_{PMU}$$  \hspace{1cm} (13)

The input power versus the load in the main path is shown in Figure 13a–e with the corresponding contour plots of $V_{out,rec}$, PCE, $P_{out}$, and transient response of the RFEH system. Figure 13a shows the contour plot of the primary power path output voltage respective to the load, $R_L$. A maximum $V_{out}$ of 1.64 V is observed at $P_{in}$ of 5 dBm and the optimal $V_{out}$ respective to the PCE is shown in the green band. Figure 13b shows the contour plot of PCE, where the proposed system achieves a peak PCE of 21.15% with a 3.3 kΩ load at 0 dBm of input power and obtains a 5 dB wide dynamic range with a PCE of over 16%. Figure 13c observes an output power of 423 μW at peak PCE and a maximum power of 1 mW at 5 dBm of input power. Figure 13d shows the reflection coefficient ($|S_{11}|$)
which yields an impedance matching at 2.4 GHz with the input power of 0 dBm. At low power, the secondary path produces a sensitivity of $-14.1$ dBm achieved by the improved voltage conversion efficiency (VCE) of the CP.

Figure 13. Post-layout Simulation results of RFEH: (a) $V_{out}$, (b) PCE, (c) $P_{out}$, (d) reflection coefficient ($|S_{11}|$) versus frequency, and (e) transient response.
The VCE of the CP can be expressed as,

\[
VCE (%) = \frac{V_{out, cp(\text{actual})}}{V_{out, cp(\text{ideal})}}
\]  (14)

where \(V_{out, cp(\text{actual})}\) is the actual output DC voltage of the CP and \(V_{out, cp(\text{ideal})}\) is the ideal output DC voltage of the CP. The CP pumping efficiency is 99.23\% at an input voltage of 0.2 V or \(V_{\text{rec}}\). This shows the proposed CP works well for lower supply voltage, which is preferred in a fully-integrated application. The proposed RVCO achieves a start-up at \(V_{\text{rec}} = 70\, \text{mV}\). The power consumption of RVCO is 953 pW at 0.2-V of input voltage and is well fitted for RF energy harvesting systems.

Table 3 summarizes the performance comparison with state-of-art RFEH systems [14,22–29]. The proposed fully integrated RFEH system has a unique feature that incorporates dual-channel on-chip IMN, rectifier, capacitive DC-DC converters, and PMU. This allows two separate power path operations, one is connected with the appropriate load and the other helps to provide battery assist operation. In addition, the proposed RFEH system has a higher output power of 423 \(\mu\text{W}\) at peak PCE, compared to other recent reported work in Table 3. The RFEHs in [22–24] have better PCE, but they require off-chip components, which increase the physical form factor to more than 10 times the size of the proposed system, and these bottlenecks in the miniaturization of the device. Further, the RFEH systems [24–26,28] require to be fabricated at a cost-ineffective higher process node such as 65 nm/130 nm. In comparison to the on-chip integrated RFEH solutions in [25–29], the proposed work achieves higher sensitivity, PCE, and output power.

Table 3. Performance benchmark with related State-of-Arts.

| Reference | This Work | [14] | [22] | [23] | [24] | [25] | [26] | [27] | [28] | [29] |
|-----------|-----------|------|------|------|------|------|------|------|------|------|
| CMOS Technology | 180-nm | 130-nm | 180-nm | 180-nm | 65-nm | 130-nm | 130-nm | 180-nm | 130-nm | 65-nm |
| Frequency (GHz) | 2.4 | 0.9 | 0.93 & 2.63 | 0.914, 2.4 | 2.45 | 2.4 | 1.3 | 3.85 | 2.4/5.8 | 0.9 |
| IMN Topology | LC | LC | LC | Transmission line | LC | TX | TX | TX | LC | TX |
| Type of IMN | On-chip | Off-chip | IPD | Off-chip | Off-chip | On-chip | On-chip | On-chip | On-chip | On-chip |
| Additional Technique | Rectifier stacking, Charge pump | Off-chip Inductor, PCB | Dual band, high-Q IPD passive components, RCN, PCB | DC-boostered gate | Switch NMOS | Voltage gain, reduce dead zone | - | Bond wire inductor | Step-up stacked transformer |
| Rectifier | 3 × 3 + 6 stage CP | 5 stage | 5 stage, Dickson topology | 3 stage | 2 stage | 5 + 4 stage rectifier | 18-stage Half wave rectifier | Dual half-wave rectifier | 5 stage Diode based | 5 stage |
| Sensitivity @1 V | −14.1 dBm | −12.3 dBm | −16.154 dBm | −16 dBm | −12 dBm | −10 dBm | −11 dBm | −12 dBm | −13 dBm | −16.5 dBm |
| Peak PCE | 21.15% @0 dBm* | 29.3% @0.2 dBm* | 23.3% @−1 dBm* | 43.1&36.5%* | 73.6% @−6 dBm* | 15.9% @60 dBm* | 0.03%* | 1.58%* | 14% @0 dBm* | <1% |
| Power at Peak PCE | 423 \(\mu\text{W}\)* | 307 \(\mu\text{W}\)* | 185 \(\mu\text{W}\)* | 43 \(\mu\text{W}\)* | 184.73 \(\mu\text{W}\)* | 159 \(\mu\text{W}\)* | - | - | 140 \(\mu\text{W}\)* | - |
| Size | 1.02 mm² | 0.17 mm²* | 11.6 mm²* | 6.1 × 3.24 cm² (FR4)* | 1 mm² (PCB)* | 2.08 mm² | 0.05 mm² | 0.04 mm² | 1.02 mm² | 0.28 mm² |

* On-chip IMN. * Off-chip IMN/non-CMOS.

5. Conclusions

We presented a fully integrated multi-channel RF energy harvesting implemented in 180-nm CMOS. It adopted a shared-auxiliary-biasing technique to obtain \(V_{\text{th}}\) reduction which yields an improved pumping efficiency of 99.23\% for the CP circuit. The CP contains a SAB-RVCO, a buffer, and a charge-pump circuit designed and implemented in an integrated dual-input RFEH system. This work proposed a rectifier stacking technique to reduce the impedance and concurrently improve the quality factor Q achieving a 2.4 GHz multi-channel fully integrated RFEH system with 423 \(\mu\text{W}\) output power at a peak PCE system of 21.15\% and a proposed charge pump support to reach a sensitivity of −14.1 dBm.
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References
1. Basim, M.; Khan, D.; Ain, Q.U.; Shehzad, K.; Shah, S.A.A.; Jang, B.-G.; Pu, Y.-G.; Yoo, J.-M.; Kim, J.-T.; Lee, K.-Y. A Highly Efficient RF-DC Converter for Energy Harvesting Applications Using a Threshold Voltage Cancellation Scheme. *Sensors* **2022**, *22*, 2659. [CrossRef] [PubMed]
2. Luo, Y.; Pu, L.; Wang, G.; Zhao, Y. RF energy harvesting wireless communications: RF environment, device hardware and practical issues. *Sensors* **2019**, *19*, 3010. [CrossRef] [PubMed]
3. Bouchouicha, D.; Dupont, F.; Latrach, M.; Ventura, L. Ambient RF energy harvesting. In Proceedings of the International Conference on Renewable Energies and Power Quality, Granada, Spain, 23–25 March 2010; pp. 2–6.
4. Piñuela, M.; Mitcheson, P.D.; Lucyszyn, S. Ambient RF energy harvesting in urban and semi-urban environments. *IEEE Trans. Microw. Theory Tech.* **2013**, *61*, 2715–2726. [CrossRef]
5. Chun, A.C.C.; Ramiah, H.; Mekhilef, S. Wide Power Dynamic Range CMOS RF-DC Rectifier for RF Energy Harvesting System: A Review. *IEEE Access* **2020**, *10*, 23948–23963. [CrossRef]
6. Martins, R.P.; Mak, P.L.; Chan, C.H.; Yin, J.; Zhu, Y.; Chen, Y.; Lu, Y.; Law, M.K.; Sin, S.W. Bird’s-eye view of analog and mixed-signal chips for the 21st century. *Int. J. Circuit Theory Appl.* **2021**, *49*, 746–761. [CrossRef]
7. Martins, R.P.; Mak, P.-I.; Sin, S.-W.; Law, M.-K.; Zhu, Y.; Lu, Y.; Yin, J.; Chan, C.-H.; Chen, Y.; Un, K.-F. Revisiting the Frontiers of Analog and Mixed-Signal Integrated Circuits Architectures and Techniques towards the future Internet of Everything (IoE) Applications. *Found. Trends Integr. Circuits Syst.* **2021**, *1*, 72–216. [CrossRef]
8. Xu, P.; Flandre, D.; Bol, D. Analysis, modeling, and design of a 2.45-GHz RF energy harvester for SWIPT IoT smart sensors. *IEEE J. Solid-State Circuits* **2019**, *54*, 2717–2729. [CrossRef]
9. ITU. Pandemic in the Internet Age: From Second Wave to New Normal, Recovery, Adaptation and Resilience. Available online: https://www.itu.int/myitu/media/Publications/2021-Publications/Pandemic-in-the-Internetage.pdf (accessed on 15 October 2021).
10. Zhang, Z.; Zhan, C.; Law, M.-K.; Jiang, Y.; Mak, P.-I.; Martins, R.P. A High-Efficiency Dual-Antenna RF Energy Harvesting System Using Full-Energy Extraction With Improved Input Power Response. *IEEE Open J. Circuits Syst.* **2021**, *2*, 436–444. [CrossRef]
11. Markandeya, H.S.; Roy, K. Low-power system for detection of symptomatic patterns in audio biological signals. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2016**, *24*, 2679–2688. [CrossRef]
12. Kim, H.; Kim, S.; Van Helleputte, N.; Artes, A.; Konijnenburg, M.; Huisken, J.; Van Hoof, C.; Yazicioglu, R.F. A configurable and low-power mixed signal SoC for portable ECG monitoring applications. *IEEE Trans. Biomed. Circuits Syst.* **2013**, *8*, 257–267. [CrossRef]
13. Bayasi, N.; Tekeste, T.; Saleh, H.; Mohammad, B.; Khandoker, A.; Ismail, M. Low-power ECG-based processor for predicting ventricular arrhythmia. *IEEE Trans. Very Large Scale Integ. (VLSI) Syst.* **2015**, *24*, 1962–1974. [CrossRef]
14. Liu, Z.; Hsu, Y.-P.; Fabs, B.; Hella, M.M. An RF-DC Converter IC With On-Chip Adaptive Impedance Matching and 307-µW Peak Output Power for Health Monitoring Applications. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2018**, *26*, 1565–1574. [CrossRef]
15. Kuhn, V.; Lahuec, C.; Seguin, F.; Person, C. A multi-band stacked RF energy harvester with RF-to-DC efficiency up to 84%. *IEEE Trans. Microw. Theory Tech.* **2015**, *63*, 1768–1778. [CrossRef]
16. Belleville, M.; Cantatore, E.; Fanet, H.; Fiorini, P.; Nicole, P.; Pelgrom, M.; Pignet, C.; Hahn, R.; Van Hoof, C.; Vullers, R. Energy Autonomous Systems: Future Trends in Devices, Technology, and Systems. 2009. Available online: https://pure.tue.nl/ws/portalfiles/portal/3259966/675451.pdf (accessed on 8 May 2022).
17. Kumar, P.K.; Ramiah, H.; Ahmad, M.Y.; Chong, G.; Rajendran, J. Analysis of a Single-Frequency Multi-Channel Ambient RF Energy Harvesting in CMOS Technology. In Proceedings of the 2019 IEEE Asia Pacific Conference on Circuits and Systems (APCAS), Bangkok, Thailand, 11–14 November 2019; pp. 97–100.
18. Kim, H.; Maeng, J.; Park, I.; Jeon, J.; Lim, D.; Kim, C. A 90.2% Peak Efficiency Multi-Input Single-Inductor Multi-Output Energy Harvesting Interface With Double-Conversion Rejection Technique and Buck-Based Dual-Conversion Mode. *IEEE J. Solid-State Circuits* **2020**, *56*, 961–971. [CrossRef]
19. Poo, C.M.; Chong, G.; Ramiah, H. A dual-input extended-dynamic-PCE rectifier for dedicated far-field RF energy harvesting systems. *Analog Integr. Circuits Signal Process.* 2021, 107, 567–573. [CrossRef]
20. Heo, B.-R.; Kwon, I. A Dual-Band Wide-Input-Range Adaptive CMOS RF–DC Converter for Ambient RF Energy Harvesting. *Sensors* 2021, 21, 7483. [CrossRef]
21. Song, C.; Huang, Y.; Carter, P.; Zhou, J.; Yuan, S.; Xu, Q.; Kod, M. A novel six-band dual CP rectenna using improved impedance matching technique for ambient RF energy harvesting. *IEEE Trans. Antennas Propag.* 2016, 64, 3160–3171. [CrossRef]
22. Li, C.-H.; Yu, M.-C.; Lin, H.-J. A compact 0.9–2.6-GHz dual-band RF energy harvester using SIP technique. *IEEE Microw. Wirel. Compon. Lett.* 2017, 27, 666–668. [CrossRef]
23. Nagaveni, S.; Kaddi, P.; Khandekar, A.; Dutta, A. Resistance compression dual-band differential CMOS RF energy harvester under modulated signal excitation. *IEEE Trans. Circuits Syst. I Regul. Pap.* 2020, 67, 4053–4062. [CrossRef]
24. Lau, W.W.Y.; Ho, H.W.; Siek, L. Deep neural network (DNN) optimized design of 2.45 GHz CMOS rectifier with 73.6% peak efficiency for RF energy harvesting. *IEEE Trans. Circuits Syst. I Regul. Pap.* 2020, 67, 4322–4333. [CrossRef]
25. Masuch, J.; Delgado-Restituto, M.; Milosevic, D.; Baltus, P. Co-integration of an RF energy harvester into a 2.4 GHz transceiver. *IEEE J. Solid-State Circuits* 2013, 48, 1565–1574. [CrossRef]
26. Gonçalves, H.; Martins, M.; Fernandes, J. Fully integrated energy harvesting circuit with—25-dBm sensitivity using transformer matching. *IEEE Trans. Circuits Syst. II Express Briefs* 2015, 62, 446–450. [CrossRef]
27. Soltani, N.; Yuan, F. A high-gain power-matching technique for efficient radio-frequency power harvest of passive wireless microsystems. *IEEE Trans. Circuits Syst. I Regul. Pap.* 2010, 57, 2685–2695. [CrossRef]
28. Lerdsitsomboon, W. Technique for integration of a wireless switch in a 2.4 GHz single chip radio. *IEEE J. Solid-State Circuits* 2010, 46, 368–377. [CrossRef]
29. Lian, W.X.; Ramiah, H.; Chong, G.; PC, K.K. A Differential RF Front-end CMOS Transformer Matching for Ambient RF Energy Harvesting Systems. In Proceedings of the 2021 IEEE Asia Pacific Conference on Circuit and Systems (APCCAS), Penang, Malaysia, 22–26 November 2021; pp. 133–136.
30. Churchill, K.K.P.; Chong, G.; Ramiah, H.; Ahmad, M.Y.; Rajendran, J. Low-voltage capacitive-based step-up DC-DC converters for RF energy harvesting system: A review. *IEEE Access* 2020, 8, 186393–186407. [CrossRef]
31. De Donno, D.; Catarinucci, L.; Tarricone, L. An UHF RFID energy-harvesting system enhanced by a DC-DC charge pump in silicon-on-insulator technology. *IEEE Microw. Wirel. Compon. Lett.* 2013, 23, 315–317. [CrossRef]
32. Moghaddam, A.K.; Chuah, J.H.; Ramiah, H.; Ahmadian, J.; Mak, P.-I.; Martins, R.P. A 73.9%-efficiency CMOS rectifier using a lower DC feeding (LDCF) self-body-biasing technique for far-field RF energy-harvesting systems. *IEEE Trans. Circuits Syst. I Regul. Pap.* 2017, 64, 992–1002. [CrossRef]
33. Kotani, K.; Sasaki, A.; Ito, T. High-efficiency differential-drive CMOS rectifier for UHF RFID. *IEEE J. Solid-State Circuits* 2009, 44, 3011–3018. [CrossRef]
34. Abouzied, M.A.; Sánchez-Sinencio, E. Low-input power-level CMOS RF energy-harvesting front end. *IEEE Trans. Micro. Theory Tech.* 2015, 63, 3794–3805. [CrossRef]
35. Zhai, B.; Blaauw, D.; Sylvester, D.; Flautner, K. The limit of dynamic voltage scaling and insomniac dynamic voltage scaling. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* 2005, 13, 1239–1252. [CrossRef]
36. Razavi, B. *Design of Analog CMOS Integrated Circuits*; Tsinghua University Press Co., Ltd.: Beijing, China, 2005.
37. Assaderaghi, F.; Sinitsky, D.; Parke, S.A.; Bokor, J.; Ko, P.K.; Hu, C. Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI. *IEEE Trans. Electron Devices* 1997, 44, 414–422. [CrossRef]
38. Narendra, S.; Tschanz, J.; Hofsheier, J.; Bloechel, B.; Vangal, S.; Hoskote, Y.; Tang, S.; Somasekhar, D.; Keshavarzi, A.; Erraguntla, V. Ultra-low voltage circuits and processor in 180 nm to 90 nm technologies with a swapped-body biasing technique. In Proceedings of the 2004 IEEE International Solid-State Circuits Conference (IEEE Cat. No. 04CH37519), San Francisco, CA, USA, 15–19 February 2004; pp. 156–158.
39. Chang, Y.; Chouhan, S.S.; Halonen, K. A novel forward body biasing technique for subthreshold ring oscillators. In Proceedings of the 2015 European Conference on Circuit Theory and Design (ECCTD), Trondheim, Norway, 24–26 August 2015; pp. 1–4.
40. Shirazi, N.C.; Jannesari, A.; Torkzadeh, P. Self-start-up fully integrated DC-DC step-up converter using body biasing technique for RF energy harvesting applications. *AEU-Int. J. Electron. Commun.* 2018, 95, 24–35. [CrossRef]
41. Lin, L.; Quang, K.T.; Alioto, M. Transistor sizing strategy for simultaneous energy-delay optimization in CMOS buffers. In Proceedings of the 2017 IEEE international symposium on circuits and systems (ISCAS), Baltimore, MD, USA, 28–31 May 2017; pp. 1–4.
42. Deen, M.J.; Kazemeini, M.H.; Naseh, S. Ultra-low power VCOs-performance characteristics and modeling. In Proceedings of the Fourth IEEE International Caracas Conference on Devices, Circuits and Systems (Cat. No. 02TH8611), Oranjestad, The Netherlands, 19–19 April 2002; p. C033.
43. Razavi, B. The ring oscillator [a circuit for all seasons]. *IEEE Solid-State Circuits Mag.* 2019, 11, 10–81. [CrossRef]
44. Jung, W.; Oh, S.; Bang, S.; Lee, Y.; Foo, Z.; Kim, G.; Zhang, Y.; Sylvester, D.; Blaauw, D. An ultra-low power fully integrated energy harvester based on self-oscillating switched-capacitor voltage doubler. *IEEE J. Solid-State Circuits* 2014, 49, 2800–2811. [CrossRef]
45. Ballo, A.; Grasso, A.D.; Palumbo, G. A high-performance charge pump topology for very-low-voltage applications. *IEEE Trans. Circuits Syst. II Express Briefs* 2019, 67, 1304–1308. [CrossRef]
46. Ballo, A.; Grasso, A.D.; Giustolisi, G.; Palumbo, G. Optimized charge pump with clock booster for reduced rise time or silicon area. *IEEE Trans. Circuits Syst. II Express Briefs* 2019, 66, 1977–1981. [CrossRef]

47. Pakkirisami Churchill, K.K.; Ramiah, H.; Chong, G.; Ahmad, M.Y.; Yin, J.; Mak, P.-I.; Martins, R.P. A 0.15-V, 44.73% PCE charge pump with CMOS differential ring-VCO for energy harvesting systems. *Analog Integr. Circuits Signal Process.* 2022, 111, 35–43. [CrossRef]

48. Yi, H.; Yin, J.; Mak, P.-I.; Martins, R.P. A 0.032-mm 2 0.15-V three-stage charge-pump scheme using a differential bootstrapped ring-VCO for energy-harvesting applications. *IEEE Trans. Circuits Syst. II Express Briefs* 2017, 65, 146–150. [CrossRef]

49. Lu, Y.; Dai, H.; Huang, M.; Law, M.-K.; Sin, S.-W.; Seng-Pan, U.; Martins, R.P. A wide input range dual-path CMOS rectifier for RF energy harvesting. *IEEE Trans. Circuits Syst. II Express Briefs* 2016, 64, 166–170. [CrossRef]

50. Khan, D.; Oh, S.J.; Shehzad, K.; Basim, M.; Verma, D.; Pu, Y.G.; Lee, M.; Hwang, K.C.; Yang, Y.; Lee, K.-Y. An efficient reconfigurable RF-DC converter with wide input power range for RF energy harvesting. *IEEE Access* 2020, 8, 79310–79318. [CrossRef]