Comparative analysis of switching losses and current ripple of continuous and discontinuous SVPWM strategies for unbalanced two-phase four-leg VSI Fed unsymmetrical two-phase induction motor

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Abstract
This paper presents a comparative analysis of the continuous space vector pulse width modulation and the discontinuous space vector pulse width modulation in terms of the switching losses and current ripple reduction for the unbalanced two-phase four-leg voltage source inverter fed unsymmetrical two-phase induction motor. The main function of both space vector pulse width modulation strategies is to produce unbalanced two-output voltages with constant phase shift of 90° for main and auxiliary windings. The discontinuous space vector pulse width modulation principle is modified from a traditional two-phase four-leg voltage source inverter by placement of the space vectors to alternatively eliminate zero space vector in each switching sequence. As a consequence, the proposed unmodulation region or clamping zone of the discontinuous modulation strategy has 180° all the time. The experimental results illustrate the modulation waveforms of both methods, output voltage spectrum, normalized switching losses, output current ripple and inverter efficiency at high modulation index. The evaluation of the normalized average switching losses and the current ripple of the discontinuous space vector pulse width modulation method can be reduced more than that of the continuous space vector pulse width modulation method.

1 | INTRODUCTION

Presently, there are many researches involving in single-phase motor drives since single-phase induction motors (SPIM) have been widely employed in household appliances and small industrial applications such as air pump, water pump, fan and others. Most of SPIM cannot be controlled its speed as well as three-phase induction motor. In order to achieve the variable speed drive, SPIMs need to modify as unsymmetrical type two-phase induction motors (U-TPIM) when energy saving is seriously concerned in [1–8]. U-TPIM is adapted from an existing single-phase capacitor start and run induction motor by removing two capacitors from main and auxiliary windings. Therefore, the unbalanced two-phase power supply with variable frequency fed U-TPIM provides better performance in terms of an increase in starting torque and balancing magnetic flux because backward torque is eliminated [1, 6–8].

In past decades, the balanced two-phase power supplies for TPIM were established from two-leg, three-leg and four-leg topologies with space vector PWM techniques in [5, 9, 10]. However, the principle of modulation still provides the balanced two-phase output voltages, which are not suitable for U-TPIM drives. Subsequently, the modulating function of unbalanced SVPWM for three-leg voltage source inverter (VSI) fed U-TPIM was proposed to define unbalanced two-phase output voltages of VSI [6]. For the performance enhancement of VSIs, several papers proposed discontinuous space vector pulses width modulation (DSVPWM) for a three-phase three-leg VSI and a two-phase three-leg VSI to reduce switching losses and current ripple at high modulation index.
For DSVPWM techniques of three-phase three-leg VSI, there are many different techniques depending on load power factor such as DPWM 0 and DPWM 2 suitable for the leading and lagging power factor load respectively [12].

There are not any publication analysing the switching loss characteristics and the current ripple for two-phase four-leg unbalanced output VSI fed U-TPIM with CSVPWM and DSVPWM techniques. The aims of this paper are to establish unbalanced two-output voltages using the four-leg VSI with CSVPWM and DSVPWM techniques to improve the performance of the U-TPIM drive. Many researches have been studied the comparative performance evaluation between two-leg, three-leg and four-leg VSIs [3–5]. Although, the four-leg VSI has more switching devices than two-leg and three-leg VSIs, the magnitude of two-output voltages of the four-leg VSI gives the highest DC bus utilization compared with three-leg and two-leg VSIs at the same DC bus voltage value and also provides the lowest two output current ripples [3, 5]. These are the advantages for choosing the four-leg VSI in this research. This paper focuses on the modulating function of unbalanced space vector PWM techniques providing unbalanced output voltages for the U-TPIM. In addition, the reduction of switching losses and current ripple are investigated. For verifying the validity of the proposed method, the experimental results of modulating waveforms, switching losses, current ripple

![FIGURE 1 Proposed two-phase four-leg VSI fed U-TPIM](image1)

![FIGURE 2 Conventional location of active space vectors in d-q plane and arbitrary output voltage](image2)

### TABLE 1 Switching states and corresponding output voltage of a two-phase four-leg inverter

| No. | $S_1$ | $S_3$ | $S_5$ | $S_7$ | $V_{ao}$ | $V_{bo}$ | $V_{co}$ | $V_{do}$ | $V_{ab}$ | $V_{cd}$ |
|-----|-------|-------|-------|-------|---------|---------|---------|---------|---------|---------|
| 1   | 0     | 0     | 0     | 0     | $-V_{dc}$ | $-V_{dc}$ | $-V_{dc}$ | $-V_{dc}$ | 0       | 0       |
| 2   | 0     | 0     | 0     | 1     | $-V_{dc}$ | $-V_{dc}$ | $-V_{dc}$ | $V_{dc}$  | 0       | $-2V_{dc}$ |
| 3   | 0     | 0     | 1     | 0     | $-V_{dc}$ | $V_{dc}$  | $-V_{dc}$ | $V_{dc}$  | 0       | $2V_{dc}$  |
| 4   | 0     | 0     | 1     | 1     | $-V_{dc}$ | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | 0       | 0       |
| 5   | 0     | 1     | 0     | 0     | $-V_{dc}$ | $V_{dc}$  | $-V_{dc}$ | $-V_{dc}$ | 0       | 0       |
| 6   | 0     | 1     | 0     | 1     | $-V_{dc}$ | $V_{dc}$  | $V_{dc}$  | $-2V_{dc}$ | 0       | 0       |
| 7   | 0     | 1     | 1     | 0     | $-V_{dc}$ | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | 0       | 0       |
| 8   | 0     | 1     | 1     | 1     | $-V_{dc}$ | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | 0       | 0       |
| 9   | 1     | 0     | 0     | 0     | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | 0       | 0       |
| 10  | 1     | 0     | 0     | 1     | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | 0       | 0       |
| 11  | 1     | 0     | 1     | 0     | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | 0       | 0       |
| 12  | 1     | 0     | 1     | 1     | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | 0       | 0       |
| 13  | 1     | 1     | 0     | 0     | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | 0       | 0       |
| 14  | 1     | 1     | 0     | 1     | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | 0       | $-2V_{dc}$ |
| 15  | 1     | 1     | 1     | 0     | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | 0       | $2V_{dc}$  |
| 16  | 1     | 1     | 1     | 1     | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | $V_{dc}$  | 0       | 0       |
TABLE 2  Switching states and corresponding active and zero space vectors [15]

| Location (degrees) | Switching states | Space vector magnitude (V) | Space vector |
|--------------------|------------------|-----------------------------|--------------|
| Origin             | 0000, 0011       | 0                           | $3V_0$       |
| 0°                 | 1000, 1011       | $2V_{dc}$                   | $3V_1$       |
| 45°                | 1010, -          | $\sqrt{2}(2V_{dc})$        | $3V_2$       |
| 90°                | 0010, 1110       | $2V_{dc}$                   | $3V_3$       |
| 135°               | 0110, -          | $\sqrt{2}(2V_{dc})$        | $3V_4$       |
| 180°               | 0100, 0111       | $2V_{dc}$                   | $3V_5$       |
| 225°               | 0101, -          | $\sqrt{2}(2V_{dc})$        | $3V_6$       |
| 270°               | 0001, 1101       | $2V_{dc}$                   | $3V_7$       |
| 315°               | 1001, -          | $\sqrt{2}(2V_{dc})$        | $3V_8$       |
| Origin             | 1111, 1100       | 0                           | $3V_0$       |

FIGURE 3  The desired output voltage vector, (a) phase leg reference voltages, (b) a circular trajectory for balanced target output voltage, (c) proposed elliptical trajectory for unbalanced target output voltage

FIGURE 4  The proposed location of active space vector of unbalanced SVPWM

FIGURE 5  The proposed overall location of the eight active space vectors and the elliptical trajectory of an arbitrary output voltage

TABLE 3  Space vector active times in four sectors

| Angular position | Space vector active times |
|------------------|--------------------------|
| Sector 1         | $T_{U1} = T_{SV1} = \frac{M|A|\sin\left(\frac{\pi}{4} - \phi - \theta\right)}{2\sin\left(\frac{\pi}{4} - \phi\right)}\Delta T$ |
| $0 < \theta < \frac{\pi}{4} - \phi$ | $T_{SV2} = \frac{M|B|\sin(\theta)}{2\sin\left(\frac{\pi}{4} - \phi\right)}\Delta T$ |
| Sector 2         | $T_{SV3} = \frac{M\sin\left(\frac{\pi}{4} - \theta + \phi\right)}{2\sin\left(\frac{\pi}{4} - \phi\right)}\Delta T$ |
| $\frac{\pi}{4} - \phi < \theta < \frac{\pi}{2}$ | $T_{SV4} = \frac{M|B|\sin(\frac{\pi}{4} - \theta)}{2\sin\left(\frac{\pi}{4} - \phi\right)}\Delta T$ |
|Sector 3          | $T_{SV5} = \frac{M\sin\left(\frac{3\pi}{4} - \phi + \theta\right)}{2\sin\left(\frac{\pi}{4} - \phi\right)}\Delta T$ |
| $\frac{\pi}{2} < \theta < \frac{3\pi}{4} + \phi$ | $T_{SV6} = \frac{M|A|\sin\left(\frac{3\pi}{4} + \theta - \phi\right)}{2\sin\left(\frac{\pi}{4} - \phi\right)}\Delta T$ |
| Sector 4         | $T_{SV7} = \frac{M|B|\sin(\frac{\pi}{4} + \theta - \phi)}{2\sin\left(\frac{\pi}{4} - \phi\right)}\Delta T$ |
| $\frac{3\pi}{4} + \phi < \theta < \pi$ | $T_{SV8} = \frac{M|A|\sin\left(\frac{3\pi}{4} + \theta + \phi\right)}{2\sin\left(\frac{\pi}{4} - \phi\right)}\Delta T$ |

reduction, and efficiency of the proposed DSVPWM and CSVPWM techniques are demonstrated.

2 TWOPHASE FOUR-LEG SVPWM TOPOLOGY

The proposed main power circuit topology of a two-phase four-leg VSI fed U-TPIM consisting of eight IGBTs as
FIGURE 6 Waveform of switching active times at $M = 2$ (a) balanced output voltage $|A| = 1$ (b) unbalanced output voltage $|A| = 0.6$

FIGURE 7 Symmetric pulse patterns of modulation process for sectors 1 and 2

Switching devices is shown in Figure 1. The terminal voltages, $V_{ac}$, $V_{bc}$, $V_{co}$, and $V_{do}$ are determined as phase-leg voltages. $V_{ab}$ and $V_{cd}$ are two voltages supplied to main and auxiliary windings of the U-TPIM, respectively. Eight IGBT power switching devices have 16 possible switching states as shown in Table 1. The upper switches, $S_1$, $S_3$, $S_5$, and $S_7$ are assigned with either “1” or “0” to turn-on and turn-off, respectively while the lower switches $S_2$, $S_4$, $S_6$, and $S_8$ have the opposite status [15].

According to the corresponding output voltages in Table 1, the half of the DC bus voltage is $V_{dc}$, and the DC bus voltage is $2V_{dc}$. For the switching states, there are switching states which are the same output voltages called zero voltage vectors such as status No. 1, 4, 13 and 16. There are twelve switching states called active voltage vectors such as status No. 2, 3, 5–12, 14 and 15. The selected switching states, corresponding to output voltages and space vector are shown in Table 2. There are eight possible active voltage vectors ($SV_1, SV_2, \ldots, SV_8$) and two zero voltage vectors ($SV_0, SV_9$) as illustrated in Figure 2.

In accordance with Table 2 and Figure 2, the active voltage vector is projected in a $d$–$q$ plane divided into eight sectors with 45°. The arbitrary output voltages ($\overline{V_o}$) can be displayed in the space vector plane. Four active voltage vectors ($\overline{SV_1}, \overline{SV_3}, \overline{SV_5}, \overline{SV_7}$) have a length of $2V_{dc}$ whereas four active vectors ($\overline{SV_2}, \overline{SV_4}, \overline{SV_6}, \overline{SV_8}$) have a length of $\sqrt{2}(2V_{dc})$. Due to the similar principle of the conventional three-phase three-leg and two-phase four-leg SVPWM [5, 12, 15, 16] the mathematical calculation of switching times for the two-phase four-leg SVPWM method can be dealt with in the same manner as for the conventional one. The desired output space vector voltage ($\overline{V_o}$) [6, 12, 15] can be expressed mathematically in terms of the average of a number of these space vectors within a switching period in each sector as,

$$\overline{V_o} = V_o \angle \theta = \frac{T_{U1}}{\Delta T/2} \overline{U_1} + \frac{T_{U2}}{\Delta T/2} \overline{U_2},$$  \hspace{1cm} (1)

where $\overline{U_1}, \overline{U_2}$ are two basic adjacent voltage vectors; $\theta$ is the sampled angular position; $T_{U1}, T_{U2}$ are the active space vector times for the two basic adjacent vectors; $T_{SV0}, T_{SV9}$ are the zero space vector times; $\Delta T$ is the carrier period.

Generally, for a symmetrical space vector pattern, the space vector time for each zero-switching state ($T_{SV0}, T_{SV9}$) is set to be equal. More detailed description for these quantities can be found in [12, 15]. From Equation (1) the relationship between space vector active times and the desired output voltage for the first sector can be expressed as,

$$\frac{T_{SV1}}{\Delta T/2} = \frac{V_o}{\sqrt{2}V_{dc}} \sin \left( \frac{\pi}{4} - \theta \right)$$  \hspace{1cm} (2)
According to Figure 2 and Equation (4), the condition for the maximum possible magnitude of arbitrary output voltage vector ($V_o$) is $2V_{dc}$, which can occur at $\theta$ equal to zero. Consequently, output voltage space vector ($V_o$) in vector form is rotated with a circular trajectory. Therefore, the maximum output voltage space vector can be expressed as,

$$V_o = 2V_{dc} \text{ or } MV_{dc},$$

where $M$ is the modulation index when $0 \leq M \leq 2$, and $V_{dc}$ is the DC voltage of the midpoint of the DC link. Two-phase balanced output voltages of the four-leg VSI can be expressed as,

$$V_{ab} = V_{cd} = MV_{dc} \left( \text{peak voltage} \right).$$

### 3 | PROPOSED UNBALANCED OUTPUT SVPWM FOR TWO-PHASE FOUR-LEG INVERTERS

The purpose of this research is to develop an unbalanced output voltage two-phase four-leg VSI using continuous and discontinuous SVPWM for U-TPIM drives. For scalar and flux vector control techniques of the U-TPIM drives, these
technology drives are necessary to supply the appropriate rated voltages depending on the turns ratio of the main and auxiliary windings. For increasing the starting torque and speed regulation improvement, the magnitude of the supplied voltage for

### TABLE 5

| Angular | Phase leg reference voltages position |
|---------|--------------------------------------|
| Sector 1 | $v_{d0}$ $V_{dc} = \frac{M}{\sin\left(\frac{\pi}{4} - \phi\right)} \left[|A| \sin\left(\frac{\pi}{4} - \phi - \theta\right) + |B| \sin(\theta) - 1\right]$ |
| $0 < \theta < \frac{\pi}{4} - \phi$ | $v_{b0}$ $V_{dc} = -1$ | $v_{c0}$ $V_{dc} = \frac{M|B| \sin(\frac{\pi}{4} - \phi)}{\sin\left(\frac{\pi}{4} - \phi\right)} - 1$ |
| Sector 2 | $v_{d0}$ $V_{dc} = -1$ | $v_{b0}$ $V_{dc} = -\frac{M|B| \sin\left(\frac{\pi}{2} - \phi\right)}{\sin\left(\frac{\pi}{2} + \phi\right)} - 1$ |
| $\frac{\pi}{4} - \phi < \theta < \frac{\pi}{2}$ | $v_{c0}$ $V_{dc} = \frac{M|B| \sin\left(\frac{\pi}{2} - \phi\right)}{\sin\left(\frac{\pi}{4} + \phi\right)} - 1$ | $v_{d0}$ $V_{dc} = -1$ | $v_{a0}$ $V_{dc} = -1$ |
| Sector 3 | $v_{d0}$ $V_{dc} = \frac{M|B| \sin\left(\frac{\pi}{4} + \phi\right)}{\sin\left(\frac{\pi}{4} + \phi\right)} - 1$ |
| $\frac{\pi}{2} < \theta < \frac{3\pi}{4} + \phi$ | $v_{b0}$ $V_{dc} = \frac{M}{\sin\left(\frac{3\pi}{4} - \phi\right)} \left[\sin\left(\frac{3\pi}{4} - \theta + \phi\right) + |B| \sin\left(\theta - \frac{\pi}{2}\right) - 1\right]$ |
| $v_{c0}$ $V_{dc} = -1$ | $v_{d0}$ $V_{dc} = -1$ |
| Sector 4 | $v_{d0}$ $V_{dc} = \frac{M}{\sin\left(\frac{3\pi}{4} - \phi\right)} \left[\sin\left(\frac{3\pi}{4} - \theta + \phi\right) + |B| \sin(\pi - \theta) - 1\right]$ |
| $\frac{3\pi}{4} + \phi < \theta < \pi$ | $v_{b0}$ $V_{dc} = \frac{M|B| \sin(\pi - \theta)}{\sin\left(\frac{\pi}{4} - \phi\right)} - 1$ |
| $v_{c0}$ $V_{dc} = -1$ | $v_{d0}$ $V_{dc} = -1$ | $v_{a0}$ $V_{dc} = -1$ |
The concept of the proposed unbalanced two-phase four-leg VSI is illustrated in Figure 3 the fundamental phase-leg output voltages referenced with respect to the DC bus centre tap are defined as $V_{ao}, V_{bo}, V_{co}$ and $V_{do}$. From the relationship of the four phasor voltages in Figure 3(a), it can be written as balanced and unbalanced two output voltages in a direct and quadrature reference frame as shown in Figure 3(b,c). $V_{ab}$ and $V_{cd}$ voltages are set to be the main and auxiliary winding voltages along the $d$-axis and $q$-axis, respectively, and the phase different angle is kept at $90^\circ$.

The output space vector $V_o$ in vector form of the balanced output voltage case is shown in Figure 3(b), which is a rotating vector with a dotted line circular trajectory. According to Figure 3(c), the concept of the proposed unbalanced output voltages, the magnitude of $V_{cd}$ is kept constant while the magnitude of $V_{ab}$ is resized by multiplying the unbalanced voltage factor $|A|$ in the range between 0–1. As a result, the arbitrary output space vector is rotated with an ellipse trajectory. Therefore, the unbalanced voltage factor $|A|$ can be dealt within the unbalanced output voltage as follows,

$$V_{ab} = |A| 2V_{dc}$$

When $0 < |A| < 1$.

The magnitude and location of the proposed SVPWM are obtained by scaling the magnitude of conventional ones by the unbalanced voltage factor $|A|$. As shown in Figure 4, by using a trigonometry relationship, two active vectors $SV_3$ and $SV_7$ representing the output voltage $V_{cd}$ are kept constant equal to $2V_{dc}$. In order to decrease the output voltage $V_{ab}$, two active vectors $SV_1$ and $SV_5$ are adjusted the scaling by reducing the unbalanced output voltage factor $|A|$. For the sector 1, the magnitude of $SV_1$ has a length equal to $2V_{dc} / |A|$. At the same time, the magnitude and location of $SV_2$ is changed. It has a length equal to $2V_{dc} / |A|$ resulting from a summation of active voltage vectors, $SV_1$ and $SV_3$. The location of the proposed active vector $SV_2$ is shifted from the conventional active voltage vector as shown in Figure 4, at which the active voltage vectors $SV_2$ and $SV_4$ are shifted from the conventional angle as phase angle $\phi$.

When considering Figure 4, by using the trigonometry and the relationship of $|A|$, $|B|$ and $\phi$, the magnitude and location of active voltage vectors in sectors 1, 2, 3 and 4 can be given by,

$$SV_1 = SV_5 = \frac{2V_{dc}}{|A|},$$

$$SV_2 = SV_4 = \frac{2V_{dc} |A|}{|A|},$$

$$SV_3 = SV_7 = \frac{2V_{dc}}{|A|}.$$
FIGURE 12 The example of switching waveform for unbalanced DSVPWM technique according to Figure (1) in phase-leg-a. (a) Carrier signal and reference voltage of phase of phase-leg-a, (b) voltage across switching device S1 (c) current flowing through switches S1 (d) voltage across switching device S2 (e) current flowing through switches S2 (f) load current (g) normalized average switching loss of phase-leg-a over a fundamental period

\[ SV_2 = SV_4 = \frac{2V_{dc}}{|B|}, \]

where,

\[ |A| = \frac{V_{ab}}{V_{cd}} \]

\[ |B| = \frac{1}{\sqrt{1 + (1/|A|)^2}} \]

\[ \phi = \frac{\pi}{4} - \left( \tan^{-1} |A| \right). \]

It is noted that, the balanced output voltage occurs at $|A| = 1$, and the unbalanced output voltage occurs at $|A| < 1$. The proposed overall location of active space vector in a $d-q$ plane and an arbitrary output voltage is shown in Figure 5.

3.1 Calculation of proposed unbalanced space vector active time

As the differences of magnitude and location of the proposed active voltage vectors were mentioned before, the unbalanced output voltages of the four-leg VSI are obtained by scaling the unbalanced voltage factor $|A|$ and $|B|$.

Because of the similar principle to the conventional balanced SVPWM, the magnitude and the location of active vectors in Figure 5 are used to calculate the switching active times for unbalanced SVPWM. As illustrated in sector 1, the space vector active times ($T_{SV_1}$, $T_{SV_2}$) in the function of $|A|$ and $|B|$ can be determined by the mathematical calculation as follows:

\[ T_{SV_1} = \frac{M|A| \sin \left( \frac{\pi}{4} - \phi - \theta \right)}{2 \sin \left( \frac{\pi}{4} - \phi \right)} \Delta T. \]
FIGURE 15 Experimental results of normalized phase-leg reference waveforms and PWM output voltages in each phase-leg of unbalanced CSVPWM at $|A| = 0.67$ and $M = 2$, (a) leg-a and leg-b (Ch.-1 = $v_{ao}$, Ch.-2 = $v_{bo}$, Ch.-3 = PWM voltage of $V_{ao}$ and Ch.-4 = PWM voltage of $V_{bo}$), (b) leg-c and leg-d (Ch.-1 = $v_{co}$, Ch.-2 = $v_{do}$, Ch.-3 = PWM voltage of $V_{co}$ and Ch.-4 = PWM voltage of $V_{do}$).

FIGURE 16 Measured voltage across and current flowing through switching device waveforms of unbalanced CSVPWM at $|A| = 0.67$ and $M = 2$.

FIGURE 17 Experimental results of normalized phase-leg reference waveforms and PWM output voltages in each phase-leg of unbalanced DSVPWM at $|A| = 0.67$ and $M = 2$, (a) leg-a and leg-b (Ch.-1 = $v_{ao}$, Ch.-2 = $v_{bo}$, Ch.-3 = PWM voltage of $V_{ao}$ and Ch.-4 = PWM voltage of $V_{bo}$), (b) leg-c and leg-d (Ch.-1 = $v_{co}$, Ch.-2 = $v_{do}$, Ch.-3 = PWM voltage of $V_{co}$ and Ch.-4 = PWM voltage of $V_{do}$).

FIGURE 18 Measured voltage across and current flowing through switching device waveforms of unbalanced DSVPWM at $|A| = 0.67$ and $M = 2$. 
The examples of calculation of the space vector active times for the sectors 1–4 are given in Table 3. The waveforms of the space vector active times over the one period of switching time at the modulation index of 2 for the balanced output voltage and unbalanced output voltages can be plotted as shown in Figure 6(a,b), respectively.

### 3.2 | Equivalent phase-leg reference voltages of CSVPWM method

In order to implement the carrier-based space vector PWM for the two-phase four-leg VSI, the equivalent phase-leg voltage of the continuous SVPWM technique is proposed. The equivalent phase-leg voltage signals are compared with a high frequency triangular carrier to obtain PWM signals for driving upper and lower switching devices.

The pulse patterns of the phase-leg voltages with respect to the midpoint of the DC bus voltage are shown in Figure 7, that the symmetric pulse patterns of the modulation process for sector 1 in over the time interval $\Delta T/2$ consisting of the switching status of space vector active time $T_{SV1}$ (1000), $T_{SV2}$ (1010) and null active vectors $T_{SV0}$ (0000), $T_{SV9}$ (1111) can be arranged in Figure 7(a). Similarly, with the same process, the switching time sequence of sector 2 are $T_{SV0}$, $T_{SV3}$, $T_{SV2}$ and $T_{SV9}$ in a half period of switching as shown in Figure 7(b).

As shown in Figure 7(a), phase-leg reference voltage of phase-leg-a in sector 1 can be calculated as,

$$v_{ao} = V_{dc} \left[ \frac{T_{SV1} \Delta T / 2}{\Delta T / 2} + \frac{T_{SV2} \Delta T / 2}{\Delta T / 2} \right].$$  \hspace{1cm} (15)

Substituting the space vector active times of Equations (13) and (14) in Equation (15), the equivalent reference voltage for phase-leg-a with respect to the midpoint of DC bus voltage can be written as,

$$\frac{v_{ao}}{V_{dc}} = \frac{M |B| \sin \left( \frac{\pi}{4} - \phi \right)}{2 \sin \left( \frac{\pi}{4} - \phi \right)} \left[ |A| \sin \left( \frac{\pi}{4} - \phi - \theta \right) + |B| \sin \theta \right].$$  \hspace{1cm} (16)

Similarly, according to the space vector active time in Table 3, with the same process, the examples of equivalent reference voltages of four phase-leg with respect to the midpoint of DC bus voltage for sectors 1–4 can be achieved as shown in Table 4. In addition, it can be seen that the phase-leg reference voltage equations in Table 4 correspond to unbalanced voltage factors $|A|$ and $|B|$, and modulation index($M$). The phase-leg reference voltage equations of the eight sectors can be plotted to be the waveforms as shown in Figure 8 when $v_{ao}$, $v_{bo}$, $v_{co}$ and $v_{do}$ in dashed lines are the fundamental voltage waveforms of phase-leg reference voltage in each phase-leg. Figure 8(a) shows the...
Figure 22 Normalized switching losses of unbalanced CSVPWM technique in each phase-leg

3.3 Equivalent phase-leg reference voltages of DSVPWM method

This section describes the proposed DSVPWM technique. The main purpose of this strategy is to reduce the switching losses and the output current ripple. Basically, the DSVPWM for two-phase four-leg VSI occurs when the zero space voltage vector of either $SV_0$ (0000) or $SV_9$ (1111) is selected resulting in the removal of zero voltage vector in successive half carrier intervals [13, 14]. For the proposed DSVPWM, the zero space vector time $SV_0$ is selected for all eight sectors as shown in the example pulse pattern of sector 1 and 2 in Figure 9. Note that the choosing of either $SV_0$ or $SV_9$ in the proposed DSVPWM gives the same results. The equation of zero space vector time $SV_0$ in

\[ V_{ab} = M |A| V_{dc} \text{ (main winding voltage)}, \quad (17) \]

\[ V_{cd} = MV_{dc} \text{ (auxiliary winding voltage)}. \quad (18) \]
Figure 23 Normalized switching losses of unbalanced DSVPWM technique in each phase-leg.

In the same calculation, the phase-leg average voltages normalized with the mid-point of DC bus voltage is,

$$\frac{v_{ao}}{V_{dc}} = \frac{M |A| \sin \left( \frac{\pi}{4} - \phi - \theta \right)}{\sin \left( \frac{\pi}{4} - \phi \right)} + \frac{M |B| \sin (\theta)}{\sin \left( \frac{\pi}{4} - \phi \right)} - 1. \tag{21}$$

In the same calculation, the phase-leg “a” reference voltage normalized with the mid-point of $v_{bo}, v_{co}, v_{do}$ and $\frac{v_{ao}}{V_{dc}}$ are,

$$\frac{v_{ao}}{V_{dc}} = \frac{v_{do}}{V_{dc}} = -1. \tag{22}$$
\[
\frac{v_{co}}{V_{dc}} = M |B| \sin (\theta) \sin \left( \frac{\pi}{4} - \phi \right) - 1.
\] (23)

Table 5 shows the examples of calculated phase-leg reference voltages of sectors 1–4. The waveforms of the normalized phase-leg reference voltages of eight sectors can be plotted as shown in Figure 10. The balanced output voltages at \(|A| = 1\) and unbalanced output voltages at \(|A| = 0.6\) are shown in Figure 10(a,b), respectively. It can be observed that the interval clamping time or unmodulated region of the proposed method is 180°. Hence, the reduction of switching losses does not depend on the load power factor. This is a main benefit of the proposed DSVPWM technique.

3.4 | Switching losses and current ripple reduction

It is known that the principle of DSVPWM technique has more advantages in terms of the switching power losses and current ripple reduction in switching devices at a high modulation index [12, 14, 15]. The results of switching losses reduction occur with zero space vector placement modulation strategies. As mentioned earlier, the zero space vector placement of the proposed DSVPWM is selected with \(T_{SV0}\). Consequently, the phase-leg reference voltage waveforms are clamped to \(-V_{dc}\) during 180° in an unmodulated region or a non-switching period as shown in Figure 10. For the switching loss reduction of the proposed DSVPWM compared with the CSVPWM method at the same carrier frequency, the DSVPWM principle provides greater the reduction in switching losses than the CSVPWM method. On the other hand, the DSVPWM principle provides an increase of output current ripple rather than CSVPWM principles. Therefore, to reduce the switching losses and output current ripple for the DSVPWM principle; it is necessary to increase the carrier frequency of DSVPWM to 1.5 times of CSVPWM [12, 14, 15]. However, the switching losses of the DSVPWM method must be less than the CSVPWM method. Many papers present the switching loss analysis of discontinuous modulation using normalized load current instead of the amount of real switching power loss in a power switching device [17–21]. As shown in Figure 1, considering the switching loss in IGBT-\(S_1\) (upper switch: \(S_1\)), total average switching losses in a switching period of switching device can be evaluated from [14],

\[
P_{SW,loss} = P_{on,avg} + P_{off,avg},
\] (24)

\[
P_{SW,loss} = f_{sw} I_{sw} (t_{on} + t_{off}) \frac{V_{dc}}{3},
\] (25)

where,

\(P_{SW,loss}\) is the total power switching losses in a switching period;

\(f_{sw}\) is the carrier frequency of CSVPWM method and 1.5\(f_{sw}\) for DSVPWM method;

\(I_{sw}\) is the magnitude of the current flowing though switching device;

\(t_{on}, t_{off}\) are the turn on and turn off times.

From Equation (25), the constant values of characteristic parameters of the switching device \(t_{on}, t_{off}\) are assumed, and the mid-point of DC bus voltage (\(V_{dc}\)) of both techniques is equal. Carrier frequency of DSVPWM is set as 1.5 times of that of CSVPWM technique. Therefore, the normalized power switching losses, including both upper and lower switching devices (S1 and S2) for phase-leg-a in overall fundamental period, of the proposed SVPWM methods depend on the current flowing switch (\(I_{sw}\)) in which the magnitude of \(I_{sw}\) varies with time and relates to the load current (\(I_{load}\)). Therefore, the normalized power switching losses of the proposed SVPWM methods depending on the absolute load current can be expressed as,

\[
\text{Normalized switching loss: (CSVPWM)} = \frac{|I_{load}|}{L_{sw}},
\] (26)
Figure 25 Measured output current and current ripple of unbalanced DSVPWM method with U-TPIM load at $M = 2$ and $|i| = 0.67$

Normalized switching loss: \( \text{(DSVPWM)} = 1.5 |i_{\text{load}}| \). \( (27) \)

When,

\[
|i_{\text{load}}| = \begin{cases} 
0; & \text{Unmodulated time,} \\
|i_{\text{load}}|; & \text{Modulated time.} 
\end{cases}
\]

From Equations (26) and (27), according to Figure 11, the normalized absolute load current waveform of CSVPWM is the same as a full-wave rectifier waveform, while that of DSVPWM is the same as a half-wave rectifier waveform because the clamping time or clamping zone of the DSVPWM method is 180°.

As a result, the average normalized absolute load current of CSVPWM and DSVPWM are 0.64 and 0.47, respectively. The DSVPWM method provides lower calculated average normalized total power switching losses than the CSVPWM method about 26.56%. For a conduction loss analysis for CSVPWM and DSVPWM techniques at high modulation index [22], an increase of the conduction losses under the variation of modulation index and switching frequency of both methods is insignificant whereas a change of the switching losses is significant. As a result, the conduction losses of the proposed DSVPWM are neglected [22].

In accordance with the main power circuit of the VSI fed U-TPIM as shown in Figure 1, the simulation results of the switching loss analysis for phase-leg-a in the discontinuous modulation strategy is shown in Figure 12. A control voltage or a phase-leg reference voltage of leg-a compared with a carrier waveform to be generated gate driver signals for the proposed DSVPWM method is presented in Figure 12(a). Voltage across switching device and its current flowing through switches $S_1$ and $S_2$ are shown in Figure 12(b, c). Main winding current or load current is shown in Figure 12(f). For the consideration of the switching loss analysis, the normalized average switching loss of phase leg-a for DSVPWM is calculated by Equation (27) and its normalized average switching loss waveform is shown in Figure 12(g). It can be seen that the interval time periods from $t_0 - t_1$, $t_2 - t_3$ and $t_4 - t_5$ are modulated times and $t_1 - t_2$ and $t_3 - t_4$ are the unmodulated times or clamping zone. The normalized switching loss waveform is equal to zero at the clamping zone, and the average of its values in the overall of the fundamental period is presented as dotted line in Figure 12(g).

4 | EXPERIMENTAL RESULTS

A diagram of the overall system for verifying the proposed CSVPWM and DSVPWM techniques is shown in Figure 13, and an experimental setup system is shown in Figure 14. The system is composed of an unbalanced two-phase four-leg VSI using IGBTs as switching devices, and modulation signals for driving eight IGBTs are calculated and generated by the TMS320F28335 DSP experiment kit with mathematical calculation by MATLAB/Simulink. The waveforms of experimental results are displayed by a digital oscilloscope. The single-phase
capacitor start and run induction motor with a rating of 370 W, 220 V, 50 Hz, 4 P and 1375 rpm modified as a U-TPIM is used for the test with the unbalanced voltage condition. Moreover, the more details of the U-TPIM parameters are presented in Appendix (Table A1).

To confirm the validity of both proposed SVPWM principles, the experiments are divided into 3 conditions as follows: (A) a test of the modulating signal generation and PWM output voltage waveform of CSVPWM and DSVPWM techniques, (B) a comparison of switching losses and output current ripple in each phase-leg of the CSVPWM and DSVPWM principles, (C) a comparison of an inverter efficiency of both techniques.

4.1 Modulating Signals and Output Voltage Waveforms

For the implementation of the unbalanced two-phase four-leg VSI fed U-TPIM, it is necessary to determine the appropriate voltage of the main winding voltage and auxiliary winding voltage so as to define the unbalanced voltage factor as mentioned in Equation (10). Using parameters of U-TPIM in Appendix (Table A1), the rated voltages of the main winding ($V_{ab}$) and auxiliary winding ($V_{cd}$) at the frequency of 50 Hz are equal to 311 V$_{peak}$ and 464 V$_{peak}$, respectively. Therefore, the calculated unbalanced voltage factor according to Equation (10) is 0.67. Substituting the modulation index ($M = 2$) and $|\Delta| = 0.67$ into Equation (17), the DC bus voltage is equal to 464 V.

The normalized phase-leg voltages of CSVPWM and DSVPWM techniques in Tables 4 and 5 are calculated and generated the gate driver signals by a TMS320F28335 DSP with MATLAB/Simulink. The carrier frequency of the proposed CSVPWM and DSVPWM methods are equal to 4 and 6 kHz, respectively.

Figure 15(a,b) illustrates experimental results of the normalized phase-leg reference waveforms and PWM output voltages in each phase-leg with respect to the mid-point of the DC bus voltage of the unbalanced CSVPWM case.

According to Figure 1, the experimental result waveforms of voltages across switching devices ($r_{S1}, r_{S5}$), and their currents flowing through switching device ($i_{S1}, i_{S5}$) waveforms at the rated load torque of the unbalanced CSVPWM method as shown in Figure 16. $r_{S1}$ and $i_{S1}$ are voltage across and current flowing through switching device of IGBT (S1), which is a part of the main winding branch circuit. Likewise, $r_{S5}$ and $i_{S5}$ are voltage across and current flowing through switching device of IGBT (S5) which is a part of the auxiliary winding branch circuit. For the experimental results of CSVPWM in Figure 16, the switching devices are switched on–off all the time.

Similarly, the experimental results of the unbalanced DSVPWM method, this proposed method can be seen that there is the unmodulated interval time corresponding with the phase-leg reference voltage waveforms as shown in Figure 17(a,b). Especially, voltage across and current flowing through switching devices of IGBT (S1 and S5) as shown in Figure 18 can confirm that the pulse patterns switch of DSVPWM have a unmodulating region or clamping time. As a result, the DSVPWM method can reduce the switching power losses lower than the CSVPWM method.

Figures 19 and 20 show PWM output voltages of the four-leg VSI (Ch.-1 = $V_{ab}$, Ch.-2 = $V_{cd}$; 1000 V/div) and the motor currents (Ch.-3 = $i_{main}$, Ch.-4 = $i_{aux}$; 2 A/div, 5 ms/div) with a phase difference of 90° at the rated load torque of 2.5 N m. For both motor currents, the peak currents of main and auxiliary windings are at 3 and 1.2 A, respectively. For the experimental results of the measured voltages harmonic spectrum of both the unbalanced CSVPWM and the unbalanced DSVPWM principles in terms of the mathematical analysis, the PWM output waveforms in Figures 19 and 20 are saved as CSV format by the digital oscilloscope, and analysed harmonics spectrum by MATLAB/Simulink as shown in Figure 21. A magnitude of the fundamental voltages for main and auxiliary windings for both CSVPWM and DSVPWM methods are equal to 311 and 464 V, respectively. It can be seen that the harmonic order of the first harmonic sideband of the CSVPWM method is about 80 in which the carrier and fundamental frequency are at 4 kHz and 50 Hz, respectively, while the harmonic order of the first harmonic sideband of DSVPWM method is about 120 in which the carrier and fundamental frequency are 6 kHz and 50 Hz, respectively.

4.2 Normalized switching losses and current ripple comparing

The proposed normalized switching power losses in each phase-leg of CSVPWM and DSVPWM techniques can be analysed as Figures 22 and 23. The measured data of the PWM output phase-leg voltages ($V_{a0}, V_{bo}, V_{co}$, and $V_{do}$) with respect to the mid-point of the DC bus voltage, of the normalized phase-leg reference voltage, and of the current flowing through the main winding of the motor ($i_{main}$) are used for mathematically calculating by using MATLAB/Simulink. To compare the switching losses and current ripple for both techniques, the DC bus voltage and unbalanced voltage factor $|\Delta|$ are defined at 464 V and 0.67, respectively. Figure 22 demonstrates the results of the normalized switching losses of the CSVPWM method in each phase-leg with the carrier frequency of 4 kHz when the modulation index is set at 2; therefore, the normalized switching loss waveform is similar to the absolute load current waveform. As shown in Figure 22(a–d), the unbalanced CSVPWM for each phase-leg-a, leg-b, leg-c and leg-d gives the normalized average values of the switching losses of 1.888, 1.889, 0.778 and 0.763, respectively.

Figure 23 shows the results of the normalized switching losses of the DSVPWM method in each phase-leg with the carrier frequency equal to 6 kHz, the modulation index setting at 2, and the normalized switching loss waveform, which is 1.5 times of the absolute load current waveform. As illustrated in Figure 23(a–d), the unbalanced DSVPWM for each phase-leg-a, leg-b, leg-c and leg-d gives the normalized average switching losses of 1.397, 1.418, 0.54 and 0.567, respectively. The average values of the normalized switching losses of each phase-leg of CSVPWM and DSVPWM can be compared in Table 6 that the
proposed DSVPWM method gives lower switching losses than the CSVPWM method about 27%.

Figures 24 and 25 show the output current and the comparison of the current ripple between the current flowing through the main and auxiliary windings of the CSVPWM and DSVPWM in the mean square values. The current ripples are extracted from current excluding fundamental component using MATLAB/Simulink. The DSVPWM gives current ripple lower than the CSVPWM as shown in Table 7.

4.3 Comparison of inverter efficiency for both SVPWM techniques

Inverter efficiency testing for continuous and discontinuous modulating techniques using the power meter analyser (WT1800 Precision power analyzer) as shown in Figure 13 is proposed. The U-TPIM is controlled by open loop scalar or constant voltage per Hertz control at the rated load torque. Therefore, in order to adjust the suitable voltages of both main and auxiliary windings of the U-TPIM, the voltage source inverter must be adjusted the proportion of the voltage per frequency so as to obtain constant magnetic flux of the motor. In the efficiency test condition, the fundamental frequency of the inverter is adjusted in a range between 40–50 Hz. The efficiency of the inverter for the rated voltage per Hertz adjusted is shown in Figure 26. Clearly, for a given range of the inverter frequency, the DSVPWM method gives higher efficiency than the CSVPWM about 1%.

5 CONCLUSION

This presented work has studied comparative analysis of switching losses and current ripple of the CSVPWM and DSVPWM techniques for the unbalanced two-phase four-leg VSI fed U-TPIM. A reduction of both normalized switching loss and current ripple parameters to improve the performance of four-leg voltage source inverter and U-TPIM drive was mainly focused. Based on the CSVPWM and DSVPWM techniques, the amplitudes of the two-phase voltage output can be controlled by the unbalanced voltage factor and the modulation index. For the unbalanced applied voltages for both windings of the U-TPIM, the main and auxiliary currents, giving the different angle at 90° were observed. Consequently, the starting torque and the speed regulation were improved. The values of the normalized switching losses and the current ripple obtained from the CSVPWM and DSVPWM techniques were compared. The DSVPWM gave the switching loss values lower than the CSVPWM for leg-a, leg-b, leg-c and leg-d equal to 26.01%, 25.33%, 30.68% and 25.65%, respectively. Furthermore, the reduction of the normalized average switching losses does not depend on a change in load current power factor (pf). The current ripple of the DSVPWM was lower than that of the CSVPWM for 5.73% of main current and for 7.75% of auxiliary current. The DSVPWM method gives higher inverter efficiency than the CSVPWM throughout a range of inverter frequency between 40–50 Hz. Both of the proposed SVPWMs can be applied for the variable speed drives of U-TPIM. For practical applications, the proposed unbalanced CSVPWM method is able to be employed with a range from low to middle speeds while the proposed unbalanced DSVPWM is able to be employed with the highest speed or rated speed.

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APPENDIX A

| TABLE A1 | Parameters of U-TPIM adapted from single-phase capacitor start and run induction motor |
|----------|----------------------------------------------------------------------------------------|
| Parameters                                      | Main winding | Auxiliary winding |
| Voltage ($V_{\text{Peak}}$)                     | 311 V        | 464 V            |
| Current ($I_{\text{Peak}}$)                     | 3 A          | 1.2 A            |
| Stator winding resistance                       | 6.8 $\Omega$ | 42.2 $\Omega$   |
| Stator leakage reactance                        | 13 $\Omega$  | 51.62 $\Omega$  |
| Rotor winding resistance                        | 14.68 $\Omega$ | 51 $\Omega$    |
| Rotor leakage reactance                         | 13 $\Omega$  | 51.62 $\Omega$  |
| Magnetizing reactance                           | 123.68 $\Omega$  | 598.17 $\Omega$ |