Model and performance evaluation of field-effect transistors based on epitaxial graphene on SiC

Martina Cheli, Paolo Michetti and Giuseppe Iannaccone
Dipartimento di Ingegneria dell’Informazione: Elettronica, Informatica, Telecomunicazioni, via Caruso
16, 56100 Pisa, Italy
email: {martina.cheli, paolo.michetti, g.iannaccone}@iet.unipi.it

Abstract

In view of the appreciable semiconducting gap of 0.26 eV observed in recent experiments, epitaxial graphene on a SiC substrate seems a promising channel material for FETs. Indeed, it is two-dimensional - and therefore does not require prohibitive lithography - and exhibits a wider gap than other alternative options, such as bilayer graphene. Here we propose a model and assess the achievable performance of a nanoscale FET based on epitaxial graphene on SiC, conducting an exploration of the design parameter space. We show that the current can be modulated by 4 orders of magnitude; for digital applications an $I_{on}/I_{off}$ ratio of 50 and a subthreshold slope of 145 mV/decade can be obtained with a supply voltage of 0.25 V. This represents a significant progress towards solid-state integration of graphene electronics, but not yet sufficient for digital applications.

I. INTRODUCTION

Epitaxially grown graphene on SiC provide potential for large scale integration of graphene electronics. The first challenge to the use of graphene as a channel material for FETs is to induce a reasonable gap for room temperature operation. Recently Zhou et al. [1] have experimentally demonstrated that a graphene layer, epitaxially grown on a SiC substrate, can exhibit a gap of about 0.26 eV, measured by angle-resolved photo-emission spectroscopy. The gap is probably due to symmetry breaking between the two sublattices forming the graphene crystalline structure, as also confirmed by recent density functional calculations [2], [3]. According to the authors of Ref. [1], this method of inducing a gap is very easy and reproducible; in addition, the thickness of graphite grown on SiC can be precisely controlled to be either single- or multiply layered depending on growth parameters [4]. From a manufacturability point of view it is also extremely promising, since it would be highly convenient to prepare an entire substrate of graphene on an insulator and then obtain single device and integrated circuit through patterning [5].

From its isolation [6], [7], graphene has attracted the attention of the scientific community due to its exceptional physical properties, such as an electron mobility exceeding more than 10 times that of silicon wafers [8], and in view of its possible applications in transistors [9] and in sensors [10]. To induce a gap in graphene structures, several methods have been used: lateral confinement in graphene ribbons [9], [11] carbon nanotubes [12], impurity doping [13], or a combination of single and bilayer graphene regions [14], [15], [16]. Unfortunately, they all face different problems.

Carbon nanotubes exhibit large intrinsic contact resistance and are difficult to pattern in a reproducible way; the inability to control tube chirality, and thus whether or not they are metallic or semiconducting, make solid state integration still prohibitive. Graphene nanoribbons [9], [11] allow to obtain a very interesting device behavior [17], but require extremely narrow ribbons with single-atom precision, since a difference of only one dimer line in the width may yield a quasi-zero gap nanoribbon. Bilayer graphene exhibits a gap in the presence of a perpendicular electric field, but the range of applicable bias can only induce a gap of $100 - 150$ meV, not sufficient to obtain a satisfactory behavior in terms of $I_{on}/I_{off}$ ratio [15]. Graphene on SiC can be a two-dimensional material, thus does not require extremely sophisticated lithography, and provides a higher energy gap: for the sake of comparison, a 0.26 eV energy gap would require an armchair nanoribbon of width smaller than 3 nm, or nanotubes with diameter smaller than 2 nm.

In this work we present a semi-analytical model of an FET with a channel of epitaxial graphene grown on a SiC substrate, where the band structure, the electrostatics, thermionic and band-to-band tunneling currents are carefully...
accounted for. On the basis of our model, we assess the achievable device performance through an exploration of the device parameter space, and gain understanding of the main aspects affecting device operation.

II. MODEL

We adopt the Tight Binding (TB) Hamiltonian for single layer graphene on SiC that was proposed by Zhou et al. [1]. The empirical TB valence (−) and conduction (+) bands of a single epitaxial layer of graphene on SiC, read:

\[
E_{\pm}(k_x, k_y) = \pm \sqrt{m^2 + t^2|f(k)|^2},
\]

where \( t \) is the in-plane hopping term (2.7 eV), \( m = 0.13 \) eV is an empirical potential energy shift between the two inequivalent graphene sublattices due to interaction with the SiC substrate, and \( f(k) \) is the off-diagonal element of the considered Hamiltonian [1]. In the six Dirac points of the graphene Brillouin zone, where \( f(k) \) is zero, there is a finite energy gap \( E_g = 2m \), corresponding to the channel conduction minimum \( E_{CC} = m - q\phi_{ch} \) and the channel valence maximum \( E_{VC} = -m - q\phi_{ch} \), where \( q \) is the electron charge and \( \phi_{ch} \) the self-consistent potential in the central region of the channel.

The device under consideration, depicted in (1a), is a transistor with a channel of epitaxial graphene on a SiC substrate of thickness \( t_{sub} \) = 100 nm, with a top gate separated by a SiO\(_2\) layer of thickness \( t_{ox} \). In (1b) we have sketched the band edge profiles along the transport direction \( \hat{x} \), where \( E_{Ci1} \) and \( E_{V1} \) respectively represent the conduction and valence band edges in the three different regions denoted by \( i=S, D, C \) (Source, Drain, Channel). Source and drain contacts are \( n^+ \) doped, with molar fraction \( \alpha_D \), which translates into an energy difference \( A \) between the electrochemical potential \( \mu_S (\mu_D) \) and the conduction band edge \( E_{CS} (E_{CD}) \) at the source (drain) contact. The potential is set to zero at the source and to \( V_{ds} \) at the drain contact. In the center of the channel \( \phi_{ch} \) is imposed by vertical electrostatics. We assume, as usual, complete phase randomization along the channel, which is particularly important because it allows us to neglect the effect of resonances in the presence of tunneling barriers.

Exploiting the Gauss theorem we can write the surface charge density in the central part of the channel as

\[
Q = -C_g (V_g - V_{FBi} - \phi_{ch}) - C_{sub} (V_{sub} - V_{FBb} - \phi_{ch}),
\]

where \( C_g = \epsilon_{SiO_2}/t_{ox} \) (\( C_{sub} = \epsilon_{SiC}/t_{sub} \)) is the capacitance per unit area between the channel and the top gate (back gate), \( V_g \) (\( V_{sub} \)) is the top gate (back gate) voltage, \( V_{FBi} \) (\( V_{FBb} \)) is the flat-band voltage of the top gate (back gate), which we set to \(-0.4 \) eV.

The transit time of the device in the channel has been estimated as \( \tau_t = \frac{Q_{th} L_C}{J_{th}} \approx 10^{-16} \) s where \( Q_{th} \) and \( J_{th} \) are the thermionic charge and current, respectively, \( L_C = 20 \) nm is the channel length.

In certain spectral regions, for example in the valence band when the device is in the off state, carriers are quasi confined by tunneling barriers, and can dwell in the channel for a much longer time and be subject to some degree of inelastic relaxation, even if transport in the conduction band is practically ballistic. To consider this effect, we have therefore included a degree of inelastic scattering that leads to energy relaxation.

In steady-state conditions, considering an infinitesimal element of area \( dk_x dk_y \) in the wave-vectors space, charge distribution in the channel is obtained as a balance between two types of charge exchange processes with the contacts: one elastic, and one inelastic.

We can write the electron charge in the channel as the sum of two contributions: \( N^+_{el} \) and \( N^-_{el} \). \( N^+_{el} = f^+_{L_C n_{2D}} \) \( (N^-_{el} = f^-_{L_C n_{2D}}) \) represents the density of forward (backward) going electrons, \( f^+_{L_C} (k_x, k_y) \) denotes the occupation factors of forward (+) and backward (−) states in the channel and \( n_{2D} (k_x, k_y) \) is the 2-dimensional density of states in the \( k \)-space. For each contribution we can write a rate equation in steady-state conditions:

\[
\frac{dN^+_{el}}{dt} = J^+_S - J^-_D + (1 - T_S) f^+_{el} v_x - (1 - T_D) f^+_{el} v_x + \frac{f^+_S - f^+_L}{\tau_S} L_C n_{2D} = 0
\]

\[
\frac{dN^-_{el}}{dt} = -J^-_S + J^+_D - (1 - T_S) f^-_{el} v_x + (1 - T_D) f^-_{el} v_x + \frac{f^-_S - f^-_L}{\tau_D} L_C n_{2D} = 0
\]

where: \( f^+_D, S = \frac{S}{2} \left( \frac{E_+}{E_+ - q\phi_{ch} - \mu_{D,S}} \right) \) is the occupation factor at the drain (D) and source (S) contacts, and \( \frac{S}{2} \) is Fermi-Dirac distribution function.

Let us focus on eq. (3) (similar considerations can be made for eq. (4)): \( J^+_S = T_S f^+_S v_x \) is the tunneling current component injected from source, \( J^-_D = T_D f^-_S v_x \) is instead the drain tunneling current component ejected to the
drain, $T_{S,D}$ are the transmission probabilities from source/drain contacts to channel and $v_x$ is the group velocity. $(1 - T_S) f^+_{e} v_x$ and $(1 - T_D) f^-_{e} v_x$ are the reflected current components from source and drain barriers, respectively. The last term of eqs. 5 and 6 is a thermalization process with the source and drain reservoirs, with characteristic times $\tau_S$ and $\tau_D$, respectively. The steady-state $f^+_{e}$ and $f^-_{e}$ can be obtained by solving eq. 5 and eq. 6

$$f^+_{e} = \frac{(T_D + \frac{1}{\tau_{DP}}) (1 - T_S) f^-_{D} + \left(\frac{1}{\tau_{DP}} + 1\right) \left(\frac{1}{\tau_{DP}} + 1\right) f^-_{S}}{\left(\frac{1}{\tau_{DP}} + 1\right) - (1 - T_S) (1 - T_D)}, \quad (5)$$

$$f^-_{e} = \frac{(T_S + \frac{1}{\tau_{DP}}) (1 - T_D) f^+_{D} + \left(\frac{1}{\tau_{DP}} + 1\right) \left(\frac{1}{\tau_{DP}} + 1\right) f^+_{S}}{\left(\frac{1}{\tau_{DP}} + 1\right) - (1 - T_S) (1 - T_D)}, \quad (6)$$

where $\nu = \frac{2\nu_{CS}}{v_x}$ is the inverse of the crossing time $\tau_t$. The same reasoning can be applied to derive the hole occupation factors in the channel $f^+_{h}$. The charge, to be self-consistently solved with eq[2] in order to obtain the channel potential $\phi_{ch}$, is computed
through the integration on the BZ

\[
Q = -\frac{q}{4\pi^2} \int_{BZ} (f^e_+ + f^e_-) \, dk_x dk_y + \frac{q}{4\pi^2} \int_{BZ} (f^h_+ + f^h_-) \, dk_x dk_y,
\]

where the total current density is expressed as [18]

\[
J_{tot} = -\frac{q}{4\pi^2} \int_{BZ} v_x (f^{e}_+ - f^{e}_-) \, dk_x dk_y + \int_{BZ} v_x (f^{h}_+ - f^{h}_-) \, dk_x dk_y
\]

(8)

The transmission probability \( T_S (T_D) \) of the interband barrier at source (drain) is zero in the source (drain) band gap and 1 when there is no barrier between source (drain) and channel. When a barrier is present \( T_S \) is computed analytically with the WKB approximation, assuming \( k_y \) conservation due translational invariance along the \( y \) direction:

\[
T_S(E, k_y) = \exp \left\{ -2 \int_{x_1}^{x_2} |\text{Im}(k^E_{x,k_y}(x))| \, dx \right\}.
\]

(9)

where \( x_1 \) and \( x_2 \) are the classical turning points, and \( E \) is the particle kinetic energy. The same approach is repeated for \( T_D \).

The potential profile between each contact and the central region of the channel is described by an exponential, with characteristic variation length \( \lambda \), obtained from evanescent mode analysis [19]. Assuming \( t_{sub} \gg t_{ox} > t_{ch} \) we obtain:

\[
\lambda \approx \left( t_{ox} + \frac{t_{ch}}{2} \right) \frac{2}{\pi},
\]

(10)

where \( t_{ch} \) is the effective separation between the interfaces of the SiO\(_2\) and SiC layers, for which we assume \( t_{ch} = 1 \) nm [9].

### III. Electrostatics

From analysis of the electrostatics we can gain a better insight of the device performance limitations. In fact gate voltage control upon the channel potential (of which the subthreshold slope \( S \) is a measure) is strictly limited by the quantum capacitance \( C_q \) of the channel. Device electrostatics can be schematized as in Fig. 2a). The differential capacitance seen by the gate is

\[
C_{tg} = C_q \left( 1 - \frac{\partial \phi_{ch}}{\partial V_g} \right)
\]

(11)
but, from Eq. (2a), $C_{tg}$ can also be expressed in terms of capacitances $C_g$, $C_{sub}$, and $C_q$:

$$C_{tg} = \frac{C_g (C_{sub} + C_q)}{C_g + C_{sub} + C_q}. \quad (12)$$

From Eqs. (11) and (12) we get the derivative of the channel potential with respect to the gate potential

$$\frac{\partial \phi_{ch}}{\partial V_g} = \frac{C_g}{C_g + C_{sub} + C_q}. \quad (13)$$

The expression of the sub-threshold slope $S$ then turns out to be

$$S = \left(1 + \frac{C_{sub} + C_q}{C_g}\right) \frac{kT}{q} \ln(10), \quad (14)$$

from which it is clear that $S$ is an increasing function of $C_q$, and therefore a large quantum capacitance severely limits device performance.

Fig. 2(b) shows the capacitance-gate voltage characteristics for $V_{ds} = 0, 0.1$ and $0.25$ V obtained by solving the Schrödinger equation self-consistently with Poisson equation. In the fully ballistic case the quantum capacitance is low for small $V_{ds}$, indicating a good control of the channel by the gate voltage, but, as soon as $V_{ds}$ increases, hole accumulation in the channel occurs and $C_q$ increases, rapidly degrading $S$ (2b)). In the inelastic case, instead, the hole accumulation process is slightly suppressed by inelastic injection from the source but the effect on the quantum capacitance is practically negligible. We have observed that for $\tau$ larger than $10^{-4}$ ns, the quantum capacitance basically does not change with respect to 2 on the other hand, for $\tau < 10^{-4}$ ns $C_q$ decreases with respect to the fully ballistic case, but the inelastic process becomes dominant and Eq. (14) loses validity.

IV. PERSPECTIVES FOR DEVICE OPERATION

In order to evaluate the possible performance of the SiC-graphene FET, we have computed the transfer characteristics by varying three device parameters: drain-source voltage $V_{ds} = (\mu_S - \mu_D)/q$, donor molar fraction at the contacts $\alpha_D$ (and therefore parameter $A$) and oxide thickness $t_{ox}$. We also account for different possible values of inelastic time $\tau$. First, in Fig. 3 we analyze the trend of the transfer characteristics for different $\tau$ for $V_{ds} = 0.25$ V, $t_{ox} = 1$ nm and $\alpha_D = 6.5 \times 10^{-4}$ (corresponding to $A = 0.01$ eV). We observe that for $\tau \geq 1$ ns the transfer characteristics are unaffected and identical to the ballistic case ($\tau \to \infty$). Reducing the relaxation time under 1 ns, the minimum current increases and the sub-threshold slope remains almost constant since the quantum capacitance of the channel does not change. The introduction of inelastic scattering process has mainly two effects in the transfer characteristics: one is a gradual change of the current in the sub-threshold region, the other is an increase

Fig. 3. Transfer-characteristics for $\tau = 10^{-2}, 10^{-3}, 10^{-4}, 10^{-5}, 10^{-6}$ ns, for $V_{ds} = 0.25$ V, $\alpha_D = 6.5 \times 10^{-4}$ and $t_{ox} = 1$ nm.
of saturation current for $\tau < 10^{-4}$ ns or when inelastic current becomes relevant. In the most favorable case a
sub-threshold slope of 140 mV/dec can be obtained.

In [4] we have highlighted the effect of $V_{ds}$ and of the doping level of contacts. As expected the main visible effect
of increasing $V_{ds}$ is a gradual degradation of the sub-threshold slope, both in the fully ballistic case (4(a)-(b)) and
in the case of relaxation time $\tau = 10$ ps (4(c)-(d)), from 84 mV/dec to 202 mV/dec. The reason is simply related to
the increased accumulation of holes in the channel with increasing $V_{ds}$, which implies a larger quantum capacitance
of the channel and therefore a reduced control of the channel potential from the gate voltage.

Increasing the doping causes an increase of both the maximum current, due to an improved capacity of the
source to inject electrons, and the minimum current. From [4] we draw the indication that by reducing doping at
the contacts we improve the current dynamics. As already noted, when the source-drain voltage exceeds the gap of
the semiconducting channel ($V_{ds} > 0.26$ V), the characteristics drastically degrade, since band-to-band tunneling
current becomes comparable with the thermionic current, and hole accumulation in the channel inhibits channel
control from the gate.

The increase of oxide thickness $t_{ox}$ has mainly two effects, which can be associated to a reduction of the capacitive
coupling between gate and channel: it increases the sub-threshold slope $S$ (as shown in [5(a)]), and the opacity
of tunneling barriers (i.e. a larger $\lambda$). The former effect is more evident for $V_{ds} = 0.25$ V, where the quantum
capacitance is larger, instead $S$ is almost constant at about 75 mV/dec for $V_{ds} = 0.1$ V and $\tau < 10^{-4}$ ns, instead
for smaller $\tau$, $S \sim 100$ mV/dec. [5(b)] represents the $I_{on}/I_{off}$ ratio as a function of $t_{ox}$ for $V_{ds} = 0.1$ V and
$V_{ds} = 0.25$ V, calculated for a gate voltage range $\Delta V_g = 0.25$ V for different values of $\tau$. Larger values of the
$I_{on}/I_{off}$ ratio are observed for $\tau \geq 1$ ns.

From our analysis of transfer characteristics, evaluated by varying three device parameters as $V_{ds}$, $\alpha_D$ and $t_{ox}$, we stress the important result that for small $V_{ds}$ and doping level (4(a)) current is modulated by more than 4 orders of
magnitude.

We have to stress also the main limitation of graphene on SiC: the energy gap of 0.26 eV coupled to a low
effective mass results in a high band-to-band tunneling current $V_{ds} > 0.26$ V and so in an increase of the minimum
current achievable. This limitation on $V_{ds}$ affects the perspectives for digital circuit operation: in that case we need
$V_{ds} \approx \Delta V_g$ and equal to the supply voltage. Even for optimized device parameters ($t_{ox} = 1$ nm, $\alpha_D = 4 \times 10^{-3}$),
a supply voltage of 0.25 V, we obtain an $I_{on}/I_{off}$ ratio of 50, as can been seen from [5(b)].
V. Conclusion

In this work we have investigated the performance of field-effect transistors based on epitaxial graphene on a SiC substrate with an analytical model. We have shown that, for small $V_{ds}$ and doping level, current is modulated by more than four orders of magnitude: this is a main improvement with respect to other graphene-based devices [20], [21], [16], [15]. Comparable results can be obtained only with carbon nanotubes or graphene nanoribbons, but only with post-selection of devices after fabrication (for proper chirality and/or width). In the case of graphene on SiC, lithography and device patterning are certainly not prohibitive. A steep subthreshold behavior ($S = 67$ mV/decade) can be obtained for small $V_{ds} = 0.1$ V, when the accumulation of holes in the channel is inhibited, and a larger current ratio, in excess of $10^3$, can be obtained for a gate voltage window of 0.25 V. For digital applications, the limiting factor is represented by the small voltage drop applicable to the channel, being limited by the energy gap (0.26 eV) of the semiconducting material. With optimized device parameters we have obtained a sub-threshold slope of $\approx 140$ mV/decade and an $I_{on}/I_{off}$ equal to 50, with a supply voltage of 0.25 V and $\tau = 1$ ns. This falls short of requirements of the International Technology Roadmap for Semiconductors, which requires $I_{on}/I_{off} \approx 10^4$ [22].

Finally, we believe that graphene on SiC is very promising as a channel material for FETs, and much attention has to be put on mechanisms capable to suppress hole injection also at larger $V_{ds}$, that would allow to improve the subthreshold swing and obtain a good $I_{on}/I_{off}$ also with a small applied voltage, and on its use in tunnel FETs, where its low gap and low effective mass can be turned into an advantage.

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