Selection of capacitance for stable operation of low power DC system with constant power loads

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Abstract
The connection of constant power loads (CPL) in a low power dc system leads to a reduction in the stability margin of the system. Most of the existing techniques increase the stability margin by modifying the controller for CPL or source converter at the cost of deterioration in the performance of converters. Few publications have suggested methods to determine the value of dc-link capacitance required for stable operation of dc microgrid with CPL. These methods do not necessarily give the minimum possible capacitance as a solution. This paper suggests a method to determine the lower bound on the value of capacitor, for stable operation of dc system. A dc system with both linear and CPL loads is considered. Detailed mathematical analysis is used to determine the range of capacitance to ensure the stability of equilibrium point. Further, this paper discusses the effects of variation in linear loads on the selection of capacitor. The procedure of capacitor selection for a low power dc system is included. Using the real-time digital simulator and a digital signal processor, controller hardware-in-loop based validation is carried out for the proposed approach.

1 | INTRODUCTION

The dc systems allow easy interconnection of storage elements, dc sources and dc loads. Further, due to absence of reactive power and development of protection techniques for the dc system, it is being considered as a potential technology to power low power systems, such as residential, telecom stations, electric vehicles, etc. [1–6]. Typically, these systems have a dc-bus where various sources and loads are connected [7–9]. The schematic of a low power dc system is shown in Figure 1. The system may include linear loads and loads connected to the dc-bus using various load side converters. The advantages offered by converter interfaced loads are reduction in weight, size, volume, efficiency, isolation, improved voltage regulation, flexibility in operation, capability of integrating of loads of different characteristics and capability to control power quality etc. Due to above mentioned advantages, the converter interfaced loads are becoming more popular in low power dc system [10, 11].

The sensitive loads connected across load side converters require constant voltage to be maintained across them. Therefore, the load side converters regulate their output voltages, thereby behaving as constant power loads (CPL) for the dc system [12–14]. The typical examples of CPLs used in low power dc system are telecom switches, wireless communications base stations, servers used in data centers, closed-loop electric drives used in electric vehicles, electronic loads (like laptops, mobile phones, compact fluorescent lamps, light emitting diode bulbs) etc. [15–17].

Voltage instability is an important issue considered in dc system. It occurs due to increased penetration of CPLs in the dc system. When the voltage across the CPL decreases/increases, the current through it increases/decreases. Due to constant power behaviour, the CPLs are nonlinear in nature. The nonlinear behaviour of CPLs may lead to energy imbalance between the powers supplied by the sources and demanded by loads during transient period. This energy imbalance resonate among the energy storing elements like capacitance and inductance connected in the system. Therefore, the nonlinear behaviour of CPL may lead to oscillations in dc-bus voltage and source currents and may even lead to voltage collapse [15, 18]. Linear loads present in the system, increase damping, and therefore compensate for the destabilizing effect of CPL to some extent [15].
Power drawn by linear and CPL loads vary over time and therefore system should be designed to ensure stable operation for the complete range of linear and nonlinear CPL loads. Some of the stability criteria used to study stability of dc systems with CPL are discussed in [19].

To compensate for the destabilizing effect of CPL, impedance compensation techniques are used [20–29]. These techniques modify or reshape the equivalent output impedance of source or input impedance of CPL converters to meet the stability criteria. Method to modify source impedance using passive components is discussed in [20]. Though, the method is capable of maintaining stability, it may lead to increased losses due to additional resistive components. This method also increases the cost and size of the system. Therefore, active methods based on the emulation of impedance are more popular in literature.

Three techniques for realizing active damping in the source side converter are presented in [21]. The suggested techniques modify the output impedance of voltage source converter which is used to interface ac system to the dc microgrid. Each technique has its advantages and limitations over another in reference to phase margin and voltage sensitivity, which is usually user-specific. The effectiveness of the suggested techniques is validated for a dc microgrid connected to ac system. To enhance the performance of the system, two virtual impedance loops in which one emulates impedance in series with intermediate converter and the other in series with capacitor filter of the intermediate converter are emulated [22]. However, it requires one additional converter called intermediate converter to implement the suggested methods, which may not necessarily be available in generic dc microgrids. Further, the implementation of suggested active damping method requires additional sensors, which increases the cost of the system. Virtual resistance is emulated in series with the source in [23]. This increases damping, but may increase error in power-sharing among different sources and deterioration of voltage regulation. To enhance the current sharing performance and stability margin of dc system, frequency dependent virtual impedance methods are suggested in [24–26]. In [24], a first order low pass filter is introduced in droop controller. By adjusting the cut-off frequency of low pass filter in range of oscillations produced by CPL, the instability due to CPL may be compensated. However, the performance of the suggested method deteriorates due to variation in parameters of dc system. The voltage regulation becomes poor at heavy loads. To minimize the effect of variation in system parameters on the active damping method and to improve voltage regulation at heavy loads, a virtual impedance including parallel $R–L$ branch is emulated in [25]. The virtual impedance is designed in such a way that during step variation in load demand, the behaviour of virtual $R–L$ branch enhances the damping of the system. During steady state, the virtual $R–L$ branch offers negligible impedance which improves the voltages regulation of sources. It is observed in [26] that the effect of delay caused due to digital control, sampling and switching operation in current control loop of source converters may deteriorate the bandwidth of current control loop and stability margin of the system may decrease. While evaluating the performance of virtual impedance methods discussed in [24, 25], the effect of delay is not considered. The delay may deteriorate the bandwidth of current control loop and stability margin of the system may decrease. To address this issue, a high frequency based virtual impedance based method is suggested in [26]. The suggested method improves bandwidth of current control loop and stability margin of voltage control loop. However, the implementation of suggested virtual impedance method discussed in [26] requires additional current sensors. To keep the performance of the source converter intact, active damping techniques are used to modify input impedance of CPL in [27–29]. Similar to electronics loads, the electric motor drives operating in speed regulated mode exhibit constant power behaviour at the input of dc-bus [27, 28]. In [27], negative input-resistance compensator is suggested to damp out oscillations in dc-link voltage during load transients in brushless dc motor drive. The controller reduces the value of dc-link capacitance required for stable operation of system. However, a trade off is observed between stability margin and load performance. Improvement in stability margin due to CPL may be compensated. However, the performance of system may deteriorate due to variation in parameters of dc system. To enhance the performance of system, two virtual impedance loops in which one emulates impedance in series with intermediate converter and the other in series with capacitor filter of the intermediate converter are emulated [22]. However, it requires one additional converter called intermediate converter to implement the suggested methods, which may not necessarily be available in generic dc microgrids. Further, the implementation of suggested active damping method requires additional sensors, which increases the cost of the system. Virtual resistance is emulated in series with the source in [23]. This increases damping, but may increase error in power-sharing among different sources and deterioration of voltage regulation. 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The suggested controller includes a simple and improved reference-voltage-based compensator (RVC) to compensate the negative impedance instability caused due to permanent magnet synchronous motor drive (PMSM). The simple RVC requires an extra current sensor used to sense dc-link capacitor current. To reduce the cost of system, improved RVC is used which requires sensing of dc-link voltage only. The suggested controller makes the operation of drive insensitive to the variation in dc-link capacitance. However, the effectiveness of the suggested controller is observed only for low speed PMSM drives. The deterioration in load performance
of the drive may not be acceptable for certain loads [18, 23]. Therefore, to improve the load performance, feedforward control based active damping technique is suggested in [29] which emulates virtual $R–C$ branch at the input of CPL. This method enhances stability margin of the system and damp out oscillations caused due to CPL. However, the stability of the system is affected by the cut off frequency of first order low pass filter used in feedforward controller. The tuning of this filter requires the accurate knowledge of parameters of $L–C$ filter. The methods suggested in [27–29] are based on input impedance shaping of CPL. Moreover, as the sources and CPL may be manufactured by different suppliers, practically it may be difficult to modify the controller of each source and CPL to ensure system stability. To resolve this issue, the best way to compensate CPL instability is to connect an external stabilizer in parallel with CPL. In [30], a positive smart resistor is emulated using active stabilization circuit (ASC) which successfully compensate negative impedance instability. The smart resistor reduces the size of dc-link capacitance and enhances fault endurance capability of the system. However, suggested method requires a separate ASC to be connected in parallel with each CPL. The cost of the system increases with increase in number of CPLs in the system. The reduction in dc-link capacitance is achieved at an additional cost of ASC.

To overcome the above-mentioned issues, simple design procedures for dc microgrid, with conventional sources and load controllers, are suggested in [15, 31–34]. These methods are based on establishing the stability conditions as functions of system parameters. In [31], the stability analysis of dc microgrid is studied using linearized reduced order model. In this study, it is established that droop gain should be less than the inverse of load conductance, to ensure stable operation of dc microgrid. However, the effect of the dc-link capacitor is not considered in the aforementioned study. Other possible methods to improve stability are addition in linear loads and curtailment of CPL [15]. However, these options are not generic and would not be viable for different dc systems. In [32], port Hamiltonian matrix method is used for electrical network connected with CPL and the necessary condition for the existence of equilibrium points is derived. However, the analysis for the stability of equilibrium points is not included. In [33], the condition for the existence of the equilibrium point and its stability for a dc network connected with CPLs is studied using linear matrix inequality (LMI). However, solving LMI for a dc microgrid having a large number of sources is computationally intensive. The approach discussed in [34], evaluates the capacitance value required for the stable operation of dc system. The value is determined based on the assumption that the system should be stable up to the loading, determined by maximum power transfer ($Z_{\text{line}} = \text{complex conjugate } Z_{\text{load}}$). However, usually rated power capability of systems is much lower than the maximum power transfer and is limited by thermal and operational capabilities, therefore the solution determined in [34] would ensure stable operation, but is sub-optimal. In this situation, the suggested approach results in a large value of capacitance. Therefore, the capacitance value must be evaluated as per the power demand by CPL. This will result in a reduction in the cost of the system.

To address the aforementioned issues, a design approach is proposed in this manuscript, which determines the lower bound on the values of dc-link capacitance for the stable operation of the dc system with nonlinear CPL. The proposed approach considers the variation in power demanded by linear loads and therefore gives a solution applicable for all range of load variations. Lower bound on capacitance is deduced by evaluating the stable operating region. A minimum value of capacitance is obtained for rated power demanded by CPL. If the rated CPL demand is lower than the maximum load of the system, the proposed technique results in significant reduction in capacitance value. Using the proposed technique, the stepwise procedure for selection of capacitor in perspective of a low power dc system is included.

Section 2 deals with the brief review of the problem and formulation of approach for evaluation of the stable region. The criteria for the selection of the minimum value of capacitance and design approach for a low power dc system are discussed in Section 3. Section 4 discusses the simulation results of a test system and its correlation with the analysis. Section 5 includes the controller hardware-in-loop (CHIL) results and Section 6 concludes the paper.

## 2 REVIEW OF [34] AND PROBLEM FORMULATION

This section gives a brief overview of the problem formulation. Further, the design approach of [34] and the reason for its conservativeness are discussed. Subsequent sections, utilize this problem formulation and discuss the proposed approach to determine the lower bound on the capacitance.

A low power dc system shown in Figure 1 includes multiple sources and loads interfaced to a dc-bus through power electronic converters. Some of the sources (such as solar photovoltaics (PV)) operate under maximum power point tracking (MPPT) mode [35]. For constant atmospheric conditions, solar PV source behaves as a constant power source. In MPPT mode, the PV source injects constant power into the low power dc system for variation in dc-bus voltage [22, 34, 36]. Sources integrating storage (battery) would usually be controlled by the droop controller and would share the load power proportionally [37]. Figure 2(a) shows the constant power sources and droop controlled sources. The constant power sources can be combined with constant power loads such that the effective load power is the difference between the two values.

The output voltage of droop controlled sources is given by,

$$v_{\text{out}}^j = V_{\text{vj}} - d_{ij}i_{ij}$$

(1)

where, $v_{\text{out}}^j$ is the converter output voltage, $V_{\text{vj}}$ is the nominal voltage, $i_{ij}$ is the source current and $d_{ij}$ is the droop gain of $j$th source. The CPL is a nonlinear load and is modelled as voltage-controlled current source [17, 23, 34]. The current drawn by $j$th
CPL is given by,

\[ i_{\text{CPL}} = \frac{P_{\text{CPL}}}{V_{\text{bus}}} \] (2)

Here, \( P_{\text{CPL}} \) represents the power drawn by \( j^{th} \) CPL and \( V_{\text{bus}} \) is the dc-bus voltage.

It is assumed that, \( V_s = V_{s1} = V_{s2} = \cdots = V_{sN} \) for each source and \( d_j = d_{j1}/L_{j1} = d_{j2}/L_{j2} = \cdots d_{jN}/L_{jN} \) for each cable. The droop controlled sources are represented by a Thevenin equivalent circuit, as shown in Figure 2(b). All the CPLs and constant power sources are combined and shown as a single CPL. The differential equations governing source current, \( i_j \) and dc-link capacitor voltage, \( v_{\text{bus}} \) are

\[ \frac{d i_j}{d t} = \frac{I_{s} - V_{\text{bus}}}{R_d} - R_d i_j \] (3)

\[ \frac{d v_{\text{bus}}}{d t} = \frac{1}{C} \left( i_j - \frac{V_{\text{bus}}}{R_d} - \frac{P_{\text{CPL}}}{v_{\text{bus}}} \right) \] (4)

where,

\[ R_d = \frac{I_{s} - V_{\text{bus}}}{I_{s} - V_{\text{bus}}} - R_d = \frac{1}{\sum_{j=1}^{\infty} L_{j}} \]

\[ d_{j} = \frac{1}{\sum_{j=1}^{\infty} d_{j}} - d_{j} = d_{j} + R_{j} \frac{1}{R} = \frac{1}{\sum_{j=1}^{\infty} R_{j}} \]

\[ P_{\text{CPL}} = \sum_{j=1}^{\infty} P_{\text{CPL}j} - \sum_{j=1}^{\infty} P_{\text{CPS}j} \frac{1}{C} = \sum_{j=1}^{\infty} \frac{1}{C} \frac{i_j}{L_{j}} \]

Here, \( P_{\text{CPS}j} \) is the power generated by \( j^{th} \) constant power source, \( R_j \) is the resistance and \( L_{j} \) is the inductance of \( j^{th} \) interconnecting cable, \( R_j \) is the resistance of \( j^{th} \) linear load, \( P_{\text{CPL}j} \) represents the power drawn by \( j^{th} \) CPL and \( C_j \) represents the dc-link capacitance in parallel with \( j^{th} \) CPL connected at dc-bus. The elements \( P_{\text{CPL}}, R \) and \( C \) represent the equivalent values of power demanded by CPL, linear load and dc-link capacitance corresponding to the circuit shown in Fig. 2(b).

The equilibrium points are identified from (3) and (4) by equating \( d i_j/dt \) and \( d v_{\text{bus}}/dt \) to zero. The two equilibrium points, \( e_1 \) and \( e_2 \) are given by \([34]\),

\[ e_1 = \left( V_{s1}^*, V_{s2}^*, \ldots, V_{sN}^* \right) \]

\[ e_2 = \left( V_{s1}^*, V_{s2}^*, \ldots, V_{sN}^* \right) \]

where, the value of \( q \) is given by the following expression:

\[ q = (R/2)^2 - 4P_{\text{CPL}}RR_d \]

Typically, \( R \) (linear load resistance) is much higher than \( R_d \) (Source Thevenin resistance including droop and cable resistance). Therefore, \( P_{\text{max}} \approx V_{s}^2/4R_d \). Since, \( R_d \) is small, \( P_{\text{max}} \) is usually much higher than the rated power of the system. This condition is usually satisfied in practical systems. Once the existence of equilibrium point(s) is ensured, the stability at the equilibrium points is evaluated as below. Equations (3) and (4) are linearized and represented in the state space form given below:

\[ \frac{\Delta i_j}{\Delta t} = J_e \Delta i_j + \left[ \begin{array}{c} 0 \\ 0 \\ -1 \\ -C \end{array} \right] \Delta P \] (10)

where, \( V_{\text{bus}}^* \) is the value of the dc-bus voltage at the equilibrium point \( e_k \) and \( \Delta P \) is a small change in the CPL. The system
matrix $J_k$ (also referred as Jacobian Matrix) evaluated at equilibrium points $e_1$ and $e_2$ is given by,

$$
J_k = \begin{bmatrix}
\frac{-R_j}{L_d} & \frac{-1}{L_d} \\
\frac{1}{C} & \frac{1}{C} (\frac{R_{PL}}{(V_{bus}^*)^2} - \frac{1}{R})
\end{bmatrix}
$$

(11)

where, $k = 1, 2$. The determinant of $J_1$ is always negative, which implies that one of the eigenvalues would be negative and other would be positive. Thus, $e_1$ is an unstable equilibrium point. The determinant of $J_2$ is simplified to,

$$
det(J_2) = \frac{2\sqrt{q}(R + R_d)}{CRL_d(RV_0 + \sqrt{q})}.
$$

(12)

Since $det(J_2)$ is always positive, eigenvalues may be complex conjugate, both negative or both positive. To ensure that the real parts of the eigenvalues are negative, the trace of the matrix $J_2$ should be negative. Thus,

$$
tr(J_2) = -\frac{R_j}{L_d} - \frac{1}{RC} + \frac{P_{CPL}}{C(V_{bus}^*)^2} < 0
$$

(13)

As derived in [34], by substituting the value of $V_{bus}^*$ from (7) in (13) and rearranging, the following two cases are possible which guarantee the stability of $e_2$.

**Case-1:** $C > \frac{L_d}{R_j}

The stability condition is given by,

$$
P_{CPL} < P_{max1}
$$

(14)

where, $P_{max1}$ is defined in (9).

**Case-2:** $C \leq \frac{L_d}{R_j}

The stability condition is given by,

$$
P_{CPL} < \frac{RL_dV_0^2(CR_dR + L_d)}{(CR_d^2R + 2R_dL_d + RL_d)^2} := P_{max2}
$$

(15)

**Existing Approach and Limitation**

As discussed in [34], selection of capacitance based on case-2 restricts $P_{CPL} < P_{max2}$, for stable operation. On the other hand for capacitance selection based on case-1, $P_{CPL} < P_{max1}$ is required. Since $P_{max1}$ is higher than $P_{max2}$, case-1 allows higher available range of $P_{CPL}$. Therefore, in [34], case-1 is used, which gives the minimum value of capacitance as $L_d/R_d^2$. However, for practical systems, the value of $P_{max1}$ is much more than the rated power of the system. Therefore, case-2 is also a viable option for determining the value of capacitance. This case allows the selection of lower capacitance, required for stable operation of the system. Therefore, unlike [34], this paper focuses on case-2 and discusses the viability of case-2 and its associated challenges in the selection of dc-link capacitance and solutions in subsequent sections.

### 3 | PROPOSED SELECTION METHOD

This section discusses the proposed approach for determining the value of capacitance for stable operation of the dc system. Section 3.1 discusses the variation in $P_{max2}$ over the range of linear loads. This would provide the worst-case condition (minimum value of $P_{max2}$). Further, it should be ensured that the operating $P_{CPL}$ should always be less than this worst-case $P_{max2}$. This is discussed in Section 3.2. This gives us a lower bound on the capacitance for stable operation of the system. In Section 3.3, steps for the determination of capacitance for a dc system are provided, which includes the relations derived in Sections 3.1 and 3.2.

### 3.1 | Determination of $P_{max2}$ over variation in linear load

Value of $P_{max2}$, given in (15), depends on system parameters ($R_d$, $L_d$, $C$) and variable (linear load, $R$). With the operation of the system, as the linear load changes, $R \in [R_{min}, R_{max})$, value of $P_{max2}$ also changes. The minimum value of $P_{max2}$ over the range of $R$ is important, as it represents the worst case limit on $P_{CPL}$, as shown in (15). To find the minimum value of $P_{max2}$,

$$
\frac{dP_{max2}}{dR} = \frac{V_0^2L_d^2(3CR_d^2 - L_dR + 2L_dR_d)}{(CR_d^2 + L_dR + 2L_dR_d)^3} = 0.
$$

(16)

This gives a single solution for $R$,

$$
R^* = \frac{2R_d}{1 - \frac{3CR_d}{L_d}}.
$$

(17)

The value of $\frac{d^2P_{max2}}{dR^2}$ is negative at $R^*$, which indicates that $P_{max2}$ achieves the maximum value at $R^*$. Figure 3 shows the variation of $P_{max2}$, with $R$, for different cases. For the case $R^* < R_{min}$, the min ($P_{max2}$), occurs at $R = R_{max}$, and for case the $R^* > R_{max}$, the min ($P_{max2}$), occurs at $R = R_{min}$. Hence, the minimum value of $P_{max2}$, will occur at the boundary values of $R$ (either at $R_{min}$ or $R_{max}$). Therefore, the value of $R$, at which the minimum value of $P_{max2}$ occurs is given by,

$$
R_{ct} := \begin{cases}
R_{max}, & \text{if } P_{max2} < P_{max2}, P_{min} < P_{max2} < P_{min} \\
R_{min}, & \text{if } P_{max2} > P_{max2} > P_{min}
\end{cases}
$$

(18)
Replacing $R$ with $R_{ct}$ in (15), the minimum values of $P_{\text{max}2}$ is given by,

$$\min\{P_{\text{max}2}\} = \frac{R_{ct}I_d V_o^2 (C R_d R_{ct} + I_d)}{(C R_d^2 R_{ct} + 2 R_d I_d + R_{ct} I_d)^2}$$  \hspace{1cm} (19)

### 3.2 Evaluation of lower bound on capacitance

For stable operation of system, condition given in (15) must be satisfied for all operating conditions. Therefore,

$$P_{\text{CPL}} < \min\{P_{\text{max}2}\}$$  \hspace{1cm} (20)

By substituting $P_{\text{max}2}$ from (19) in (20) and rearranging gives,

$$\rho(C) = C^2 + b_1 C + b_2 \leq 0$$  \hspace{1cm} (21)

where,

$$b_1 = \frac{I_d^2}{R_{ct}} \left( \frac{4}{R_d} + \frac{2}{R_{pl} R_d^2} \right), \quad b_2 = \frac{I_d^2}{R_{ct}} \left( \frac{4}{R_d^2} + \frac{1}{R_d^2} + \frac{4}{R_{pl} R_d^2} \right)$$

The roots of the quadratic equation $\rho(C)$ are given by $(-b_1 \pm \sqrt{b_1^2 - 4b_2})/2$. The expression for $b_1^2 - 4b_2$ is given by,

$$b_1^2 - 4b_2 = I_d^2 \left( \frac{V_o^4}{P_{\text{CPL}} R_d^2} - \frac{4 V_o^2}{P_{\text{CPL}} R_d^2 R_{ct}} - \frac{4 V_o^2}{P_{\text{CPL}} R_d^2 R_{ct}} \right)$$  \hspace{1cm} (22)

Using the expression for $q$, from (8) gives,

$$b_1^2 - 4b_2 = \frac{V_o^2 I_d^2 q^2}{P_{\text{CPL}}^2 R_d^2 R_{ct}^2}$$  \hspace{1cm} (23)

This shows that the value of $b_1^2 - 4b_2$ is non-negative and therefore the roots of $\rho(C)$, are always real. Further, the value of $b_1$, is evaluated by using the definition of $q$ as,

$$b_1 = \frac{-L_d}{P_{\text{CPL}} R_d R_{ct}} \left( q + 2 P_{\text{CPL}} R_d R_{ct} \right)$$  \hspace{1cm} (24)

Since, $b_1$, is always negative, at least one of the roots of $\rho(C)$, would be positive and real. Figure 4 shows the plot of $\rho(C)$ for sub-case (a), one of the roots ($C_1$) is positive and one positive ($C_2$) and, sub-case (b), both the roots ($C_1$ and $C_2$) are positive. These cases are further discussed below.

### Sub-case (a) ($C_1 < 0$ and $C_2 > 0$)

The product of the roots ($b_2$) would be negative for this case. Therefore, for sub-case (a), the range of capacitance for stable operation starts from zero value of capacitance. Using the expression for $b_2$, the inequality $b_2 < 0$, gives,

$$P_{\text{CPL}} < \frac{V_o^2 R_{ct}}{(R_d + 2 R_{ct})^2}$$  \hspace{1cm} (25)

Usually, the droop resistance $R_d$ would be much smaller then resistance of linear load ($R_{ct}$). Therefore, using $R_{ct} >> R_d$, the above expression becomes,

$$P_{\text{CPL}} < \frac{V_o^2}{R_{ct}}$$  \hspace{1cm} (26)

The physical significance of above result is that if the value of $P_{\text{CPL}}$ becomes less than linear load demand ($V_o^2 / R_{ct}$), the range of $C$ would start from negative value, and therefore, the system would be stable even with zero capacitance. However, in realistic sense, the zero value of $C$ means a very small value of $C$. The capacitance value cannot be zero as the analysis carried out in Section 2 of paper is valid only for non-zero value of dc-link capacitance. To keep the value of voltage ripples within a specified percentage of average value of dc-link voltage, a fixed minimum value of dc-link capacitance is still required [38, 39].

If the power demanded by nonlinear CPL load is more than the power demanded by linear load, then both roots would become positive and is discussed in next case.

### Sub-case (b) ($C_1 > 0$ and $C_2 > 0$)

Here the lower bound on capacitance for stable operation is given by,

$$C_{1|R_{ct}} = \frac{I_d}{R_d} \left[ -\frac{2}{R_{ct}} - \frac{1}{R_d} + \frac{V_o (V_o R_{ct} - \sqrt{q R_{ct}})}{2 P_{\text{CPL}} R_d R_{ct}} \right]$$  \hspace{1cm} (27)
As derived in appendix, the value of $C_1$ is less than $L_d/R_d^2$. This shows that the lower bound for this case would be given by $C_1$, which is less than $L_d/R_d^2$.

In summary, for $P_{CPL}$ less than the power of linear loads, the lower bound on capacitance for stable operation is zero, and in case of high penetration of CPL loads ($P_{CPL}$ > power of linear loads), low bound is given by $C_1$, which is less than $L_d/R_d^2$ (lower bound given in [34]). This section determines the lower bound on capacitance value. Once the range of capacitance for stable operation is known, the viability of proposed approach for a dc system is explored in subsequent sub-section.

3.3 | Capacitor Selection: System Perspective

This section discusses the selection of dc-link capacitor based on the expressions derived in the previous subsection. Typically, the load requirements are known. Using the composition of sources (solar PV and battery) and their locations would be determined based on available resources and technocommercial analysis. Subsequently, the interconnecting cables would be determined.

3.3.1 | Design of interconnecting cable and droop gain

The interconnecting cable is selected based on the desired current carrying capacity and allowable voltage drop across it. As discussed in [40], the required power handling capacity of the cable is determined by,

$$P_{\text{(cable)}} = \frac{\delta \eta V_{dc}^2}{2 \sigma L}. \tag{28}$$

where, $\delta$ is the desired voltage regulation of the system, $\eta$ is the overloading margin, $V_s$ is the nominal system voltage, $\sigma$ is the specific resistance at 80 °C, $S$ is area of cross section and $L$ is the length of the cable. Depending on the system voltage and power handling capacity, suitable cable is selected. Its parameters ($R_s, L_s$) as specified in cable data sheet supplied by manufacturer, would be used for further design process.

To ensure proportional power sharing among sources, they are controlled using droop controllers. The value of droop gain $d_i$ depends on the source power capacity and value of voltage as discussed in [41].

$$d_i = \frac{(V_s - V_{\text{out}}) V_{\text{out}}}{P_i}. \tag{29}$$

3.3.2 | Incorporation of tolerance limits

However, due to manufacturing imperfection and aging effect of capacitor, the capacitance value would be different from its nominal/designed value, which may affect local stability of equilibrium point [42, 43]. Tolerance in the value of capacitance, is defined as the permissible relative deviation from its rated value.

The tolerance limit $\pm \varepsilon_1\%$ and $\varepsilon_2\%$ represent the effect of manufacturing variations and the effect of aging, respectively. Correspondingly to $\varepsilon_1\%$ and $\varepsilon_2\%$, the modified nominal value of capacitor $C_{\text{new}}$, required for stable operation is,

$$C_{\text{new}} = \bar{C} \left(1 + \frac{\varepsilon_1}{100} + \frac{\varepsilon_2}{100}\right). \tag{30}$$

Incorporation of tolerance limits $\varepsilon_1\%$ and $\varepsilon_2\%$ compensates the effect of aging and manufacturing imperfection.

Once the system parameters are known, the design process, as shown in Figure 5 is followed:

i Calculate the droop gains of sources using (29). Using droop gains of sources ($d_i$) and cable parameters ($L_d$, $R_d$), determine the values of $R_d$ and $L_d$ using (5).

ii Check if power demand by nonlinear CPL is higher or lower than that of linear loads. If CPL power is lower than as discussed in section IIIC, minimum required capacitance is zero. Otherwise, use (27) to calculate the capacitance values $C_1 \mid R_{\min}$ and $C_1 \mid R_{\max}$. The value $\max\{C_1 \mid R_{\min}, C_1 \mid R_{\max}\}$ is the lower bound of capacitance required for stable operation of the system for all range of linear and nonlinear CPL loads.

iii Include the values of component tolerances $\varepsilon_1, \varepsilon_2$ in the selected values of $C$ to minimize the aging effect and effect of manufacturing imperfection.

3.3.3 | Other factors affecting dc-link capacitance

The boundary of value of dc-link capacitance, $C$ selected from (27) ensures the stable operation of dc system with CPL. However, use of reduced value of $C$ may lead to certain tech-
technical issues in dc system which are discussed in brief in this section. The reduction in the value of dc-link capacitance may increase the magnitude of ripples in dc-link voltage \[38,39,44\]. Due to reduction in the value of dc-link capacitance, the necessary energy required to open the protective devices is not provided by the dc-link capacitance which may deteriorate the fault detection and fault clearance performance of protection schemes used in dc systems \[15\]. To resolve above mentioned issues arising due to use of reduced value of dc-link capacitance, a higher value of dc-link capacitance is selected.

### 3.4 Selection of DC-link Capacitance using Detailed Model of DC System

In Section 2, the simplified model of dc system given by (11) is used to select the lower bound on the value of dc-link capacitance. In this model, the sources used in the low power dc system are modelled as ideal sources. However, the actual sources are provided with inner current and voltage controllers in addition to droop controller. The dynamics of these controllers may affect the value of lower bound on the value of dc-link capacitance. In this section, the selection of dc-link capacitance using detailed model of dc system is discussed. Further, the effect of these models on the selection of lower bound of dc-link capacitance is discussed.

#### 3.4.1 Detailed model of dc system

In this subsection, the value of \(C\) is evaluated using detailed model of low power dc system discussed in \[24\]. The low power dc system including sources and loads interconnected through cables is shown in Figure 6. Each source is connected to the dc-bus through bidirectional dc-dc boost converter as shown in Figure 6. The dynamical equations of \(j^{th}\) boost converter are

\[
\begin{align*}
\frac{di_{pj}}{dt} &= \frac{1}{L_{pj}}(V_{pj} - (1 - d_j)i_{pj} - R_{pj}i_{Lpj}) \quad (31) \\
\frac{dv_{pj}}{dt} &= \frac{1}{C_{pj}}((1 - d_j)i_{Lpj} - i_{pj}) \quad (32) \\
\frac{di_{pj}}{dt} &= \frac{1}{L_{pj}}(v_{pj} - v_{bus} - R_{pj}i_{pj}) \quad (33)
\end{align*}
\]

where, \(V_{pj}\) is the source input voltage, \(i_{Lpj}\) is the inductor current and \(d_j\) is the duty cycle of \(j^{th}\) dc–dc boost converter, respectively. The elements, \(L_{pj}\) and \(R_{pj}\) are inductance and resistance of input inductor coil and \(C_{pj}\) is the value of capacitance connected at the output of boost converter. The control scheme of \(j^{th}\) dc–dc boost converter is shown in Figure 7. The linear PI controllers are used to minimize error between the reference and actual quantity in voltage and current control loops. From the control scheme shown in Figure 7 for closed loop dc–dc boost converter, the state equations for output of voltage and current controllers are

\[
\begin{align*}
\frac{d\phi_{pj}}{dt} &= V_{oj} - d_{pj}i_{pj} - v_{oj} \quad (34) \\
\frac{d\phi_{pj}}{dt} &= K_{pPJ}(V_{pj} - d_{pj}i_{pj} - v_{oj}) + K_{iPJ}\phi_{pj} - i_{Lpj} \quad (35)
\end{align*}
\]

where, \(K_{pPJ}\) and \(K_{iPJ}\) are proportional and integral gains of PI controller used in voltage control loop and \(K_{pPJ}\) and \(K_{iPJ}\) are proportional and integral gains of PI controller used in current control loop of \(j^{th}\) dc–dc boost converter. Here, \(\phi_{pj}\) is the output of voltage controller, \(\phi_{pj}\) is the output of current controller.
and \( I_{j}^{ref} \) is the reference value of inductor current of dc-de boost converter. Using (34) and (35), the expression for duty cycle, \( d_j \) is given by,

\[
d_j = K_{p_j}[K_{p_j}(V_o - d_j - v_y) + K_{q_j}\phi - J_{L_j}I_j] + K_{q_j}\phi_j
\]

Linearizing (31), (32), (33), (34), (35) and (36) and simplifying, the small signal model of \( j \)th source converter is given by,

\[
\Delta\dot{x}_{ij} = A_{ij}\Delta x_{ij} + B_{ij}\Delta v_{bus}
\]

where, the state vector, \( \Delta x_{ij} = [\Delta x_{i}, \Delta x_{i}, \Delta x_{i}, \Delta \phi_{ij}, \Delta \phi_{ij}]^T \) and matrix \( B_{ij} = [0, 0, 0, 0, 0]^T \). The value of system matrix \( A_{ij} \) of \( j \)th converter is given by (38) in which, \( V_o \) and \( I_{L_j} \) are output voltage and inductor current corresponding to the operating point \( (V_o, I_{L_j}) \) of \( j \)th source converter.

\[
A_{ij} = \begin{bmatrix}
L_{ij}K_{p_j} & K_{p_j} & 1 & 0 & 0 \\
-C_{ij} & -C_{ij} & 0 & 0 & 0 \\
1-d_j & 1-d_j & 0 & 0 & 0 \\
-1 & 0 & 0 & 0 & 0 \\
-K_{p_j} & -K_{p_j} & 0 & 0 & 0
\end{bmatrix}
\]

Writing (37) for n-sources connected in dc system,

\[
\Delta\dot{x} = A\Delta x + B\Delta v_{bus}
\]

where, the state vector, \( \Delta x = [\Delta x_{1}, \Delta x_{1}, \Delta x_{1}, \Delta x_{2}, \Delta x_{2}, ..., \Delta x_{n}, \Delta x_{n}]^T \), \( A = \text{diag}[A_{11}, A_{22}, ..., A_{nn}] \) and \( B = [B_{11}, B_{22}, ..., B_{nn}]^T \).

Now assuming that, \( R_{L1}/L_{L1} = R_{L2}/L_{L2} = \cdots = R_{Lq}/L_{Lq} = R_{L}/L_{L} \), for each cable, the total source current, \( i \), is expressed as

\[
i = i_1 + i_2 + \cdots + i_j + \cdots + i_n = \sum_{j=1}^{n} i_j
\]

According to simplified model discussed in Section 2, all the CPLs and constant power sources are combined and represented as a single CPL. The dynamics of dc-bus voltage are represented in (4). In case of schematic of dc system shown in Figure 6, the differential equations governing dc-bus voltage, \( v_{bus} \) is

\[
\frac{dv_{bus}}{dt} = \frac{1}{C}\left(\sum_{j=1}^{n} i_j - v_{bus} - \frac{R_{PL}}{V_{bus}}\right)
\]

The meaning of symbols used in above relation are defined in Section 2. Linearizing above and writing in matrix form,

\[
\Delta i_{bus} = A_{bus}\Delta x + B_{bus}\Delta v_{bus}
\]

where, \( A_{bus} = \frac{1}{C}[0 0 0 0 0 0]^T \) and \( B_{bus} = \frac{1}{C}\left(\frac{P}{V_{bus}} - \frac{1}{V_{bus}}\right) \).

To check the stability of the dc system, the linearized small signal model of dc system is required. For this purpose, the state equations given by (39) and (42) are converted into standard state space form given below.

\[
\Delta\dot{x} = A\Delta x
\]

where, the state vector, \( \Delta x = [\Delta v_{bus}, \Delta i_{bus}]^T \) and the value of system matrix, \( A \) of low power dc system is given by,

\[
A = \begin{bmatrix}
A_{bus} & B_1 \\
A_{bus} & B_{bus}
\end{bmatrix}
\]

The small signal model represented by (43) represents the detailed model of dc system including dynamics of source converters and their controllers, interconnecting cables and loads.

### 3.4.2 Selection of dc-link capacitance

The theoretical value of dc-link capacitance required to ensure stable operation of dc system about the stable equilibrium point is evaluated from eigenvalues root loci plots. For this purpose, the eigenvalues of the dc system are determined using (43). For a given value of \( P_{CPL} \), the value of \( C \) is set to zero value. If any of the eigenvalues is in Right Half Plane (RHP), then gradually increase the value of \( C \) such that all the eigenvalues come to lie in the Left Hand Plane (LHP) from RHP. This is the minimum value of \( C \) required for the given value of \( P_{CPL} \). The same procedure is adopted for other values of \( P_{CPL} \).

### 4 STUDY OF A TEST SYSTEM

In this section, the procedure for evaluating dc-link capacitance is used for a test case system. The selection of dc-link
capacitance value for a low power dc system is explained in following subheadings.

### Configuration of Test Model

The test system has two sources connected to the dc-bus using dc-dc boost converters, one CPL and one linear load, as shown in Figure 8. System parameters are given in Table 1 and cable parameters are given in Table 2. The value of droop gain \( d \) of each source is set to 0.15 V/A for the value of voltage regulation of 5%. The power range for variation in linear load \( R \) is between 4 to 8 kW which corresponds to \( R_v \in (R_{\text{max}}, R_{\text{min}}) \) between 20 and 20 \( \Omega \).

#### TABLE 1 Parameters of source and load converter

| Parameter       | Source converter (boost converter) | CPL (buck converter) |
|-----------------|-----------------------------------|----------------------|
| Nominal output voltage | 400 V                            | 200 V                |
| Rated power     | 50 kW                             | 90 kW                |
| Switching frequency | 5 kHz                            | 5 kHz                |
| Inductor        | 100 \( \mu \)H                    | 100 \( \mu \)H       |
| Capacitor       | 1000 \( \mu \)F                   | 1000 \( \mu \)F      |
| Current controller (in pu) | 2.2 + 20/s | 6.1 + 10/s |
| Voltage controller (in pu) | 1.5 + 900/s | 0.5 + 1000/s |

#### TABLE 2 Interconnecting cable parameters [45]

| Parameter       | Cable-1 | Cable-2 |
|-----------------|---------|---------|
| Current rating  | 250 A   |         |
| Cable type      | 3 conductor Al-PVC 185 mm² |     |
| Resistance      | 105 m\( \Omega \)/km |   |
| Inductance      | 237 \( \mu \)H/km |   |
| Cable length    | 1000 m  | 1000 m  |

Figure 9 shows the plot of \( P_{\text{max}1} \) and \( P_{\text{max}2} \) corresponding to \( R_v = R_{\text{min}} = 20 \Omega \) with variation in the values of \( C \). For \( C = L_d/R_d \), the value of \( P_{\text{max}1} \) is equal to \( P_{\text{max}2} \). The region located below the \( P_{\text{max}1} \) curve is the region of existence of equilibrium point. The region located below the curve \( P_{\text{max}2} \) is the region of stability of equilibrium point \( e_2 \). The value of \( P_{\text{max}1} \) is 312 kW. The point of intersection of \( P_{\text{max}2} \) and \( R_{\text{CPL}} \) gives the value of \( C \) required for stabilization of dc system. In the simulation study, two cases are considered. In one case, the value of power demanded by CPL, \( P_{\text{CPL}} \), is less than the value of rated linear load demand \( (P_R) \), as shown in Figure 9(a). In the other case, the power demanded by CPL, is more than the rated linear power, as shown in Figure 9(b). In case-a, the value of linear load demand is \( P_R = 8 \) kW. The point \( Q \) shown in zoomed portion of Figure 9(a), represents the value of \( P_{\text{CPL}} \) which requires zero value of \( C \) for stabilization of dc system. The value of \( P_{\text{CPL}} \) corresponding to point \( Q \) is calculated from (25). The value of \( P_{\text{CPLQ}} \) for the parameters given in Table 1 is 7.8 kW which is nearly equal to \( P_{\text{min}} = 8 \) kW. However, the value of \( P_{\text{CPL1}} \) is 3 kW. The value of \( C \) required for stabilization lies on negative side of C-axis. This can be seen in the zoomed portion of Figure 9(a). This implies that for \( P_{\text{CPL}} < P_{\text{CPLQ}} \), system would be stable for any positive value of capacitance.

In case-(b), the rated value of \( P_{\text{CPL2}} \) is 90 kW. The \( P_{\text{CPL}} \) is more than the rated linear power \( P_R \), therefor the minimum capacitance required for stable operation is given by \( C_{\text{min}} = 0.60 \text{ mF} \). As shown in Figure 9(b), the value of \( P_{\text{max}1} \) is much higher than the \( P_{\text{CPL}} \) and \( P_R \) and therefore, there is no need to restrict capacitance value above \( L_d/R_d \). The proposed technique results in significant reduction in the value of \( C \). The points of intersection of \( P_{\text{CPL}} \) and \( P_{\text{max}2} \) gives the value of \( C_1 \) as shown in Figure 9(a),(b).

#### Selection of \( C \) using simplified model

In this section, the value of \( C \) is evaluated for the case, \( P_{\text{CPL}} > P_R \) using simplified model discussed in Sections 3.1, 3.2 and 3.3. Analytically, for the given range of \( R \), the value of \( C \) is evaluated using (27). The value of \( C|_{R_{\text{max}}} \) is calculated as 0.60 mF whereas \( C|_{R_{\text{min}}} \) is 0.58 mF. The value, \( \max \{0.58 \text{ mF}, 0.60 \text{ mF}\} = 0.60 \text{ mF} \), is the minimum value of capacitance required for stable operation of the system for all range of linear and CPL loads. This proves the effectiveness of the proposed methodology, which provide lower bound on capacitance for stable operation of the system.

Figure 10 shows the variation of \( P_{\text{max}2} \) with respect to variation in \( C_1 \) for the system parameters given in Table 1. The
FIGURE 9   Effect of variation of $C$ on $P_{max1}$ and $P_{max2}$ for case (a) and case (b)

expression for $P_{max2}$ is given by (15). The point of intersection of $P_{max2}$ and $P_{CPL}$ gives the value of $C$ required for stabilization of dc system. For a constant load power demand $P_{CPL} = 90 \text{kW}$, the minimum value of $C_1$ is 0.60 mF. The horizontal line (red colour) shows the selected value of $C_1$ using the approach suggested in [34], which gives the value of $C_1 = \frac{L_d}{R_d^2} = 7.30 \text{ mF}$. From the graph, it is clear that there is significant reduction in the value of $C_1$ if the value of $P_{CPL}$ is smaller than $P_{max1}$.

4.4 Selection of $C$ using Detailed Model

In Section 4.2, the value of dc-link capacitance is selected for the parameters of a low power dc system given in Table 1. The value of $C$ is selected using simplified modeling discussed in Sections 3.1, 3.2 and 3.3. In this subsection, the value of $C$ is evaluated using detailed model discussed in Section 3.4 for the parameters of low power system given in Table 1.

To determine the value of $C$ using detailed model of dc system, root loci plot for dominant eigenvalues given in Figure 11
is determined using (43). The value of constant load power demand is maintained at $P_{\text{CPL}} = 90$ kW and linear load demand, $P_{\text{Rmax}} = 4$ kW. The initial value of $C$ is set to $10 \mu F$. The value of $C$ is gradually increased in small steps. It is observed in Figure 11 that with increase in the value of $C$, eigenvalues starts moving towards the LHP. For a threshold value of $C_1 = 0.52$ mF, all the dominant eigenvalues migrate from RHP into the LHP. This threshold value of $C_1 = 0.52$ mF is regarded as the desired value of dc-link capacitance required to ensure the stable operation of dc system about the equilibrium point for $P_{\text{CPL}} = 90$ kW. The same procedure is repeated to determine desired values of $C$ for other values of $P_{\text{CPL}}$ using detailed model of dc system.

In the above mentioned case, the value of $C_1$ is evaluated using detailed model for a dc system having capacity of 100 kW and rated CPL demand $R_{\text{CPL}} = 90$ kW. Adopting the above mentioned procedure, the value of $C_1$ for other dc systems can be determined. As discussed in section 4.3, the Figure 10 shows the variation of $P_{\text{max2}}$ with respect to variation in $C_1$ for the system parameters given in Table 1. The point of intersection of $P_{\text{max2}}$ and $P_{\text{CPL}}$ gives the desired value of $C$ required for stabilization of dc system using simplified model. Using detailed model, the desired value of $C$ required for a given $C_1$ is mentioned above. The values of dc-link capacitances required for given values of constant load demands using the two models of dc system are plotted in Figure 12. For a rated constant load power demand $P_{\text{CPL}} = 90$ kW, the minimum value of $C_1$ required using simplified and detailed models are $0.60$ and $0.52$ mF, respectively. From Figure 12, it is observed that the values of $C_1$ determined using simplified and detailed model of dc system are in close agreement. This justifies the use of simplified model to evaluate the desired value of $C$ required to ensure stable operation of dc system for a specified value of rated CPL demand.

4.5 Simulation results

To validate the results in matlab/simulink, the simulation study of the system shown in Figure 8, is carried out. The parameters of the dc system are given in Table 1 of this manuscript. Depending upon the value of dc-link capacitance $C_1$, the following Matlab/Simulink results are included for capacitance value less than and more than its lower bound.

4.5.1 $P_{\text{CPL}} < P_{\text{R}}$ and $C_1 < C_{\text{min}}$

In this case, the constant load power demand, $P_{\text{CPL}}$ is maintained at a value which is less than the power demanded by linear load. The value of $P_{\text{CPL}}$ is 3 kW and the value of $P_{\text{Rmax}}$ is 4 kW. At $t = 1$ s, the step variation in linear load demand $P_{\text{R}}$ from 4 to 8 kW is applied. The value of dc-link capacitance, $C$ connected at the input of CPL is $20 \mu F$. The Figure 13 shows the waveforms of current supplied by source-1, source-2 and dc-bus voltage. From the waveform as shown in Figure 13, the operation of dc system remains stable. From these waveforms, it is clear that a stable operation of dc system is observed even for small value of $C$, which validates the findings discussed in Section 3.

4.5.2 $P_{\text{CPL}} > P_{\text{R}}$ and $C_1 < C_{\text{min}}$

In this case, the rated value of $P_{\text{CPL}}$ is 90 kW. The minimum value of $C_1$ required for stabilization dc system is $0.60$ mF. The initial value of $P_{\text{CPL}}$ demanded by buck converter connected at the dc-bus is $60$ kW. The dc-link capacitance having value of $C_1 = 0.40$ mF is connected at input of buck converter. As the linearized model of the converter is valid for small perturbations in load variations, therefore the constant power demand is gradually increased using variable resistance $R_L$ connected at the output of buck converter. Figure 14 shows the waveforms.
of current supplied by source-1 and source-2 interfaced to the dc-bus through dc-dc boost converters, dc-link voltage $v_{bus}$ and power demanded by CPL. The linear load demand is maintained at $P_{R_{min}} = 8$ kW. A step variation in $P_{CPL}$ from 60 to 70 kW is applied at $t = 1$ s. As shown in Figure 14(a), oscillations appear in $i_{d1}$ and $i_{d2}$, which increase without bounds and the operation of the dc system becomes unstable for $C_1 < C_{min}$.

4.5.3 \( P_{CPL} > P_R \) and \( C_1 > C_{min} \)

Now the value of $C_1$ is changed from $C_1 = 0.40$ mF to $C_2 = 0.80$ mF. The Figure 14(b) shows the waveforms of current supplied by source-1, source-2, dc-link voltage $v_{bus}$ and power consumed by CPL. From the responses of $i_{d1}$, $i_{d2}$, $v_{bus}$ and $P_{CPL}$, the stable operation of dc system is observed for $C_1 > C_{min}$.

4.5.4 \( (P_{CPL} > P_R \text{ and } C_1 = \frac{I_d}{R_d}) \)

Now the operation of dc system is observed with value of $C_1 = R_d/L_d^2$. The Figure 15 shows the operation of the dc system with value of $C_1 = R_d/L_d^2 = 7.30$ mF. The Figure 15 shows the waveforms of current supplied by source-1 and source-2, dc-link voltage $v_{bus}$ and power demanded by CPL, $P_{CPL}$. The linear load demand is maintained at $P_{R_{min}} = 8$ kW. A step variation in $P_{CPL}$ from 60 to 70 kW is applied at $t = 1$ s. The operation of dc system remains stable.

From Figs. 14(b) and Figs. 15, it is observed that the responses of dc system remains stable even for lower values of $C$ if dc-link capacitance is selected as per the CPL demand rather than selecting $C$ according to the method discussed in [34]. This validates the findings discussed in Section 3.

4.6 Evaluation of \( C_1 \) for sources having unequal ratings

The approach used to evaluate the value of dc-link voltage is applicable to the system including multiple sources of either equal or unequal ratings as discussed in Section 2. The analysis for the evaluation of value of $C$ remains same. From (5), the unequal values of droop gains of sources modify the average value of droop gain $d_{avg}$ which leads to modification in the value of effective droop gain $R_D$ of thevenin’s source. From (27), the minimum value of capacitance required for stable the operation is determined.

To validate the results, the simulation study of the low power dc system having two sources of unequal ratings as shown in The Figure 8, is carried out. The rating of source-1 is 70 kW, and that of source-2 is 30 kW. The cables used to connect the sources to the dc-bus are same as the previous case. The droop gain of source-1 is 0.109 V/A and that of source-2 is 0.253 V/A. For these values of droop gains, the value of $C$ evaluated using (27) to stabilize the operation of dc system against $P_{CPL} = 60$ kW and $P_{CPL} = 90$ kW are 0.30 and 0.50 mF. The initial value of $P_{CPL}$ demanded by buck converter connected at the dc-bus is 60 kW. The dc-link capacitance having value of $C = 0.40$ mF is connected at input of buck converter. The Figure 16(a) shows the waveforms of current supplied by source-1, source-2 and dc-link voltage $v_{bus}$ for $C = 0.40$ mF. The linear load demand is maintained at $P_{R_{min}} = 8$ kW. From the waveforms of the currents $i_{d1}$ and $i_{d2}$, supplied by source-1 and source-2, it is observed that the operation of dc system becomes unstable for a step variation in $P_{CPL}$ from 60 to 70 kW applied at $t = 1$ s. The Figure 16(b) shows the waveforms of current supplied by source-1, source-2 and dc-bus voltage $v_{bus}$ for $C = 0.80$ mF. From the waveforms of the currents $i_{d1}$ and $i_{d2}$, stable operation of dc system is observed for the step variation in $P_{CPL}$ from 60 to 70 kW.

5 CHIL BASED STUDIES AND VALIDATION

This section discusses the CHIL realization using real-time digital simulator (RTDS) and Texas Instruments made TMS320F28335, digital signal processor (DSP). The Figure 17 shows the overall scheme, implemented for this study. The parameters of source converter and CPL are given in Table 1. Each source and CPL is a dc-dc boost and buck converter along
FIGURE 14  Simulation results for sources having equal power ratings. Source currents, dc-bus voltage and power consumed by constant power load (CPL) for $P_{R_{min}} = 8$ kW: (Current: 200 A/div, voltage: 200 V/div, power: 20 kW/div and time-axis: 50 ms/div). (a) Waveforms of currents supplied by source-1 and source-2, dc-bus voltage and power consumed by CPL with $C = 0.40$ mF. (b) Waveforms of currents supplied by source-1 and source-2, dc-bus voltage and power consumed by CPL with $C = 0.80$ mF.

FIGURE 15  Simulation results for sources having equal power ratings. Source currents, dc-bus voltage and power consumed by constant power load (CPL) for $P_{R_{min}} = 8$ kW: (Current: 200 A/div, voltage: 200 V/div, power: 20 kW/div and time-axis: 50 ms/div). Waveforms of currents supplied by source-1 and source-2, dc-bus voltage and power consumed by CPL with $C = 7.3$ mF.

with inner voltage and current controllers as shown in Figure 8. The values of droop gains of boost converter, cable parameters and the dc-link capacitance are identical to those considered in previous section. The giga-transceiver analogue output and giga-transceiver digital input cards are used to interface the DSP (which includes controller for source and load converters) with RTDS (which includes the dc system and converters).

Depending upon the value of dc-link capacitance $C_1$, the CHIL results are considered for the following two cases.

5.1  |  Case-a ($P_{CPL} < P_R$)

In this case, the value of resistive load demand is more than the nonlinear CPL demand. As discussed in Section 3, for this case the stabilized operation of dc system can be achieved, even with very small value of $C$. For this case, $C$ having small value of 10 $\mu$F is connected at the input of CPL. The value of $P_{CPL}$ is 3 kW and the value of $P_{R_{max}}$ is 4 kW. At $t = 70$ ms, the step variation in linear load demand $P_R$ from 4 to 8 kW is applied. The Figure 18 shows the waveforms of current supplied by source-1, source-2 and dc-bus voltage. From the waveform as shown in Figure 18, the operation of dc system remains stable.

5.2  |  Case-b ($P_{CPL} > P_R$)

This case is further subdivided into three cases.
FIGURE 16  Simulation results for sources having unequal power ratings. Source currents, dc-bus voltage and power consumed by constant power load (CPL) for \( P_{R_{\text{min}}} = 8 \text{ kW} \): (current: 200 A/div, voltage: 200 V/div, power: 20 kW/div and time-axis: 50 ms/div). (a) Waveforms of currents supplied by source-1 and source-2, dc-bus voltage and power consumed by CPL with \( C = 0.40 \text{ mF} \). (b) Waveforms of currents supplied by source-1 and source-2, dc-bus voltage and power consumed by CPL with \( C = 0.80 \text{ mF} \).

5.2.1  Case-b1 \( (P_{\text{CPL}} > P_R \text{ and } C_1 < C_{\text{min}}) \)

In this case, the CPL demand is maintained more than the linear load demand. The rated value of \( P_{\text{CPL}} \) is 90 kW. The minimum value of \( C_1 \) required for stabilization dc system is 0.60 mF. The initial value of \( P_{\text{CPL}} \) demanded by buck converter connected at the dc-bus is 60 kW. The dc-link capacitance having value of \( C = 0.40 \text{ mF} \) is connected at input of buck converter. The Figure 19(a) shows the waveforms of current supplied by source-1, source-2 and dc-link voltage, \( n_{\text{bus}} \) by maintaining the linear load demand of \( P_{R_{\text{max}}} = 4 \text{ kW} \). A step variation in \( P_{\text{CPL}} \) from 60 to 90 kW is applied at \( t = 70 \text{ ms} \). As shown in Figure 19(a), the oscillations having large magnitude appear in the responses of \( i_{s_1}, i_{s_2} \) and \( n_{\text{bus}} \), and the operation of the dc system becomes unstable. Now the linear load demand is changed from \( P_{R_{\text{max}}} = 4 \text{ kW} \) to \( P_{R_{\text{min}}} = 8 \text{ kW} \). The Figure 19(b) shows the waveforms...
of current supplied by source-1, source-2 and dc-link voltage \(v_{\text{bus}}\) for the linear load demand of \(P_{\text{Rmin}} = 8\ \text{kW}\). The large oscillations in the responses of \(i_{\text{s1}}, i_{\text{s2}}\) and \(v_{\text{bus}}\) indicate the unstable operation of dc system.

### 5.2.2 Case-b2 (\(P_{\text{CPL}} > P_{\text{R}}\) and \(C_1 > C_{\text{min}}\))

Figs. 20(a) and 20(b) shows the waveforms of \(i_{\text{s1}}, i_{\text{s2}}\) and \(v_{\text{bus}}\) for \(P_{\text{Rmax}} = 4\ \text{kW}\) and \(P_{\text{Rmin}} = 8\ \text{kW}\), respectively. The value of \(C_1\) connected at the input of buck converter is 0.80 mF. A step variation in \(P_{\text{CPL}}\) from 80 to 90 kW is applied at \(t = 70\ \text{ms}\). As shown in Figure 20(a), damped oscillations appears in responses of \(i_{\text{s1}}\) and \(i_{\text{s2}}\). Due to increase in linear load demand \(P_{\text{L}}\) from 4 to 8 kW, oscillations are visible in \(i_{\text{s1}}\) and \(i_{\text{s2}}\), as shown in Figure 20(b).

### 5.2.3 Case-b3 (\(P_{\text{CPL}} > P_{\text{R}}\) and \(C_1 = \frac{L_s}{R_d^2}\))

The Figure 21(a),(b) shows the operation of the dc system with value of \(C = R_d/L_s^2 = 7.30\ \text{mF}\) for \(P_{\text{Rmax}} = 4\ \text{kW}\) and \(P_{\text{Rmin}} = 8\ \text{kW}\).
FIGURE 21 Controller hardware-in-loop (CHIL) results. DC-bus voltage and source currents with \( C = 7.30 \, \text{mF} \) for case-b3: (Voltage: 200 V/div, current: 80 A/div, time-axis: 50 ms/div). (a) Waveforms of dc-bus voltage and currents supplied by boost converters with \( P_{\text{Rmax}} = 4 \, \text{kW} \). (b) Bus voltage and currents supplied by boost converters with \( P_{\text{Rmin}} = 8 \, \text{kW} \).

8 kW respectively. From Figs. 20 and 21, it is clear that the operation of low power dc system is stable even with smaller values of dc-link capacitor selected using proposed approach and does not require large capacitance as discussed in [34].

6 | CONCLUSIONS

In this paper, a novel approach is proposed for the design of a low power dc system interfaced with nonlinear CPLs and resistive loads. The proposed approach helps in selecting the value of dc-link capacitance as per the CPL demand of the system. In the case where the CPL demand is greater than linear load, there exists a lower bound on the value of dc-link capacitance above which the stable operation is guaranteed. If the CPL demand is less than the linear load demand, the stable operation of low power dc system is observed even with very small value of dc-link capacitance. From the proposed approach, it is concluded that the stable operation of dc system is possible even with smaller values of dc-link capacitance and does not require large dc-link capacitance as discussed in the literature. The selection of capacitance for a low power dc system is also discussed in this paper. The value of capacitor, determined from the proposed methodology is validated using CHIL based setup. From the results included in Section 5, it is verified that the proposed method results in a significant reduction in the value of capacitance.

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To prove that $C_1 < L_d / R_d^2$, it is assumed that this inequality is true. Substituting the value of $C_1$ from (27) in inequality $C_1 < L_d / R_d^2$ and simplifying

$$\frac{L_d}{R_d} \left[ - \frac{2}{R_c} - \frac{1}{R_d} + \frac{V_d (V_c R_{cr} - \sqrt{q R_{cr}})}{2 P_{C_{PL}} R_d^2 R_{cr}} \right] < \frac{L_d}{R_d^2} \quad (A.1)$$

which on simplification gives,

$$\frac{V_d R_{cr}}{V_a} - \frac{4 P_{C_{PL}} (R_{cr} + R_d)}{V_a} < \sqrt{q R_{cr}} \quad (A.2)$$

squaring on both sides and simplifying

$$(V_d R_{cr})^2 > 4 P_{C_{PL}} (R_{cr} + R_d) \quad (A.3)$$

Since $q$ is non-negative quantity, the inequality (33) is true. Therefore the inequality given by (31) is also true. From above analysis, it is inferred that, $C_1 < L_d / R_d^2$ holds.