Neural networks on microcontrollers: saving memory at inference via operator reordering

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Abstract

Designing deep learning models for highly-constrained hardware would allow imbuing many edge devices with intelligence. Microcontrollers (MCUs) are an attractive platform for building smart devices due to their low cost, wide availability, and modest power usage. However, they lack the computational resources to run neural networks as straightforwardly as mobile or server platforms, which necessitates changes to the network architecture and the inference software. In this work, we discuss the deployment and memory concerns of neural networks on MCUs and present a way of saving memory by changing the execution order of the network’s operators, which is orthogonal to other compression methods. We publish a tool for reordering operators of TensorFlow Lite models and demonstrate its utility by sufficiently reducing the memory footprint of a CNN to deploy it on an MCU with 512KB SRAM.

1 Introduction

Deep learning can bring computational intelligence to personal and IoT devices. Using deep learning models directly on the edge devices allows for greater cost-efficiency, scalability and privacy for end-users, compared to relying on a remote server to carry out the processing. However, the development of lightweight neural networks, suitable for such underpowered hardware, is centred around mobile phones as the target platform.

Here, we venture further and explore a more resource-constrained platform—microcontroller units (MCUs). MCUs are cheap, widespread and are geared towards energy-efficient workloads. They offer an alternative to designing a purpose-built custom chip, allowing to save on development cost and time. However, a unit typically consists of a low-frequency processor and only several hundred kilobytes of on-chip memory, and thus severely underpowered compared to mobile devices.

Specially designed network architectures and inference software are required to cope with hardware constraints of MCUs. In this work, we: (a) discuss memory limitations of a microcontroller platform and how it affects neural network deployment; (b) devise a way to minimise the peak memory usage of a neural network by making inference software follow a particular execution order of its operations.

We implement our methodology as a tool for reordering operators within TensorFlow Lite models. We successfully apply it to a chosen convolutional neural network, reducing the memory footprint enough to make it fit within the on-chip memory of our microcontroller platform, which would not have been possible using the default provided operator execution order. Operator reordering is carried out only at inference and does not change the architecture or the output of a neural network, making it fully orthogonal to many other network compression methods.

1 Available for download at https://github.com/oxmlsys/tflite-tools

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2 Background

2.1 Neural network execution

A neural network can be thought of as a computation graph which expresses dependencies between individual operations (also called layers or operators). An operator, e.g. a 2D convolution or addition, takes one or more input tensors and produces a single output. Modern deep learning frameworks optimise the network’s computation graph for inference in advance by e.g. fusing adjacent operators and folding batch normalisation layers into preceding linear operations. The execution proceeds by evaluating one operator at a time in a topological order of nodes in the graph.

An operator requires buffers for its inputs and output to be present in memory before its execution can commence. Once the operator has finished executing, memory occupied by its inputs can be reclaimed (if not use elsewhere) and the output buffer will eventually be used as an input to other operators. We define a working set as a set of tensors that need to be kept in memory at any given point in execution. This comprises input and output tensors of a pending operator and other tensors that were already produced and need to be held back in memory for subsequent operators.

Classic neural network architectures, such as the original multilayer perceptron, AlexNet [2], VGG [3], consist of a linear sequence of layers, which are iteratively applied to transform the input. However, more recent architectures, such as ResNet [4], Inception [5], NasNet [6], introduce divergent processing paths where the same tensor can be processed by several layers, i.e. their computation graph is no longer linear and has branches. This means that the inference software may have multiple operators available for execution at any given step.

2.2 Resource scarcity of microcontroller hardware

A microcontroller unit that would be powerful enough to execute neural networks reasonably quickly (e.g. ARM Cortex M series) typically has a low-frequency RISC processing core (up to 400 MHz) and 128–2048KB of on-chip memory [1]. The memory is partitioned into read-write static RAM (SRAM) and read-only NOR-Flash memories, with the latter housing the executable code and static data. In contrast to mobile or desktop hardware, there are no intermediate levels in this memory hierarchy, although the set-up may have some backing storage. A backing storage, e.g. an SD-card, typically has a high capacity but is slow [7] and power-costly to access (≈100x more energy required to read a value outside of on-chip memory [8]).

The lack of intermediate memories forces applications to fit within the on-chip memory to remain fast. For neural networks, this makes aiming for a small peak working set size and parameter count (model size) an important goal in model design. Note that it’s not necessary to pursue the maximal memory saving—aiming just below the on-chip memory capacity is sufficient.

Memory requirements of a neural network can be directly mapped to the two types of on-chip memory. Parameters (trainable weights, constants) of a network are immutable and can be embedded into the executable code as static data stored in NOR-Flash. Any intermediate tensors that are dependent upon input (so-called activation matrices) are produced at runtime and would have to be stored in SRAM. Thus the model size and peak memory usage are constrained by the capacities of NOR-Flash and SRAM memories, respectively.

In Section 4, we show how choosing operator execution order affects which tensors reside in SRAM (are in the working set). We exploit this to minimise the peak working set size (peak memory usage).

3 Related work

The design of compact models is an active topic of deep learning research, albeit usually under less extreme constraints than those of microcontroller hardware. One can obtain a smaller neural network by using layer decomposition [9, 10], pruning [11][12], quantisation [13] and binarisation [14][15], distillation [16] or exploiting sparsity [17]. Popular mobile-friendly CNN architectures include MobileNet [18] and ShuffleNet [19]. MNasNet [20] and EfficientNet [21] develop architecture search algorithms to design a network within a certain floating-point operation count or memory budget. In particular, Fedorov et al. [22] incorporate the maximal working memory size of an operator into their optimisation goal.
A relatively underexplored set of methods include complex evaluation strategies for parts of the network to save memory at runtime. For example, authors of MobileNet \[18\] note that a building block of their model has a channel-wise operation, whose output is accumulated into another tensor, which allows processing the input tensor in parts. Also, Alwani et al. \[23\] propose not to materialise an output tensor of a large convolution operation in memory at all, and compute its individual output elements as needed by succeeding operators.

The development of low-power machine learning models is fostered by the TinyML Summit \[24\] and the Visual Wake Words competition \[25\], which looked for performant MCU-sized CNNs for person detection. Compact deep learning models have been built for use on wearables devices \[26\] and for keyword spotting \[27, 28\]. Concerns about the memory usage of neural networks and data movement during execution are also discussed in neural network accelerator chip design literature \[29–31\].

4 Methods and implementation

Neural networks whose computation graphs contain branches allow some freedom over the order of evaluation of their operators. When execution reaches a branching point, the inference software has to choose which branch to start evaluating next. This choice can affect which tensors need to be kept in memory (working set), so we can construct an execution schedule that minimises the total size of the working set at its peak (memory bottleneck).

To illustrate this, Figure 1 shows an example of a computation graph, adapted from a real-world CNN. Evaluating operators as numbered 1 through to 7 will result in peak memory usage of 5216, coming from operator #3 (input and output buffers + the output of operator #1 that is held back for operator #4). However, fully evaluating the rightmost branch first (execution order 1, 4, 6, 2, 3, 5, 7), would result in peak memory usage of 4960, coming from operator #2 (input and output buffers + output of operator #6 that is held back for operator #7). Appendix A gives a more detailed breakdown of the memory usage during computation, together with plots produced by our tool, for both default and optimised operator schedules.

We approach finding a memory-optimal execution schedule for an arbitrary computation graph by algorithmically enumerating all execution schedules and calculating their peak memory usage. To simplify the problem, we assume that no operator will be executed twice (this assumption is also made in TensorFlow). A computation graph is a directed acyclic graph (DAG) and any topological order of its nodes would produce a valid execution schedule; in general, enumerating all topological orders of a DAG is an explored problem in graph algorithms literature \[32\].

In Algorithm 1 (procedure MEM), we describe a dynamic programming algorithm that is concerned with the minimal peak memory usage required to produce (and keep in memory) a set of tensors $X$. It enumerates execution schedules recursively by trying to "undo" operators that produced each of the tensors in $X$. The algorithm should be invoked on a set of network’s output tensors and the optimal execution schedule can be traced by checking which recursive calls contributed to the answer.

To simplify the implementation, the algorithm begins by filtering out tensors that don’t have an operator that produced them (so-called constants), as those just contribute to memory usage and don’t affect the execution schedule. A restriction that no operator is evaluated twice is implemented by checking whether an operator is a predecessor to any of the remaining tensors, as this would require it to be executed at some point again in the schedule. Note that MEM($X$) may be invoked on the same set of tensors multiple times (from different execution paths), so it should be memoized (i.e. the output should be cached) to avoid recomputing the result.
Algorithm 1 Computing the minimal peak memory usage of a neural network. PARTITION function splits a set into two using a predicate; producer(x) denotes an operator that produced tensor x.

1: procedure MEM(X) ▷ Minimum amount of memory needed to compute tensors in X
2: ▷ Partition tensors into constants (no producer) and activation matrices
3: cs, as ← PARTITION(X, x : producer(x) is None)
4: if as is empty then
5:    return \(\sum_{c \in cs} |c|\) ▷ No operators left to order, report sizes of remaining constants
6: end if
7: m ← ∞
8: for x in as do
9:    \(rs \leftarrow as \setminus x\) ▷ Remaining tensors that need to be kept in memory
10:    is ← producer(x).inputs ▷ Tensors required to produce x
11:    if any(x is a predecessor of r for r in rs) then
12:        continue ▷ x is a predecessor to r, so producer(x) would have to be evaluated twice
13:    end if
14:    ▷ Peak memory usage will be determined by either the producer of x—i.e. memory used its input tensors (is), output tensor (x) and other tensors (rs)—or by other operators in the execution path (recursive case MEM(rs ∪ is))
15:    \(m' \leftarrow \max\{MEM(rs \cup is), \sum_{t \in rs \cup is \cup \{x\}} |t|\}\)
16:    \(m \leftarrow \min(m, m')\) ▷ Pick the execution path that gives minimal memory usage
17: end for
18: return \(\sum_{c \in cs} |c| + m\)
19: end procedure

We use a lightweight TensorFlow Light Micro inference engine [33] (henceforth micro-interpreter) to run the neural network on the MCU itself. At the time of writing [2], the software did not support reclaiming memory from tensors that were no longer needed, so we implement our own dynamic memory allocator for tensor buffers. Internally, TensorFlow Lite assumes that tensors reside in contiguous blocks of memory and cannot be fragmented. The memory allocator is only used by the micro-interpreter, which allows us to ensure that C/C++ pointers to memory blocks are not being remembered anywhere in the code. This enables us to move buffers in memory as needed for defragmentation. We adopt a very simple defragmentation strategy of moving all tensor buffers to the start of the memory region as much as possible after the execution of every operator.

5 Experiments

We deploy a neural network onto an MCU with both default and optimised operator schedules to exhibit the difference in memory usage. We use one of the winning submissions of the Visual Wake Words competition [25], called SwiftNet Cell [34, 35], as it has only 250KB of parameters and contains many branches, which enables us to showcase the benefits of reordering. The model is run using the modified micro-interpreter (as described above) on a NUCLEO-F767ZI prototyping board [36]. The board features a Cortex M7 processor, running at 216Mhz, and has 512KB of SRAM.

|                | SwiftNet Cell | MobileNet v1 |
|----------------|---------------|--------------|
|                 | Default order | Optimal order | Static alloc. | Dynamic alloc. |
| Peak memory usage (excl. overheads) | 351KB | 301KB | 241KB | 55KB (↓ 186KB) |
| Execution time  | N/A | 10243 ms | 1316 ms | 1325 ms (↑ 0.68%) |
| Energy use      | N/A | 8775 mJ | 728 mJ | 735 mJ (↑ 0.97%) |

Table 1: Peak memory usage, execution time and energy use of chosen models.

2 At the time of publication of this pre-print, a dynamic memory allocator has been implemented by maintainers of TensorFlow Lite Micro, making this change no longer necessary. However, we keep the description of our memory allocation strategy, as well as the power and latency measurements, as an illustrative example of memory management overheads.
Table 1 shows that optimised ordering was able to save 50KB of memory, compared to the order embedded in the model. Including the framework overhead (≈200KB for SwiftNet Cell, proportional to the number of tensors), this made a sufficient difference to make the model’s memory footprint fit within SRAM. We also check the overhead introduced by replacing a static memory allocator with a dynamic one by running MobileNet-v1-based person detection model (from the Tensorflow Lite Micro repository). Measurements show negligible (sub-1%) increase in execution time and energy used by the MCU and the memory footprint was decreased by 186KB. In general, latency and power consumption can be reduced with operator implementations that leverage processor capabilities well (SIMD, DSP instructions).

6 Discussion

The results show that employing a different operator execution order for neural network inference can make previously undeployable models fit within the memory constraints of MCU hardware. Reordering operators can be implemented just within the inference software, making it orthogonal to most other network compression approaches, which were likely to have been already used to create an MCU-sized model.

Unlike mobile and server platforms, MCU hardware often doesn’t have enough memory to statically pre-allocate all tensor buffers of the network, which requires the inference software to support dynamic memory allocation. We showed that a simple defragmentation strategy is a viable option with little overhead cost. However, when the execution schedule is known in advance, optimal tensor buffer placement in memory may be precomputed.

Having a way of precisely computing peak memory usage for models with complex computation graphs would benefit neural architecture search (NAS) procedures. The algorithm can be extended to support various memory saving tricks: for example, if one of the inputs to the addition operator is not used elsewhere, the result can be accumulated into it, eliminating the need for an output buffer.

7 Conclusion

Microcontrollers are a viable platform for running deep learning applications if the model designer can overcome constraints imposed by limited memory and storage. In this work, we describe how to minimise peak memory usage of a neural network during inference by changing the evaluation order of its operators. By applying our methodology, we were able to achieve sufficient memory savings to deploy the chosen CNN on a microcontroller with 512KB SRAM, which would not have been possible otherwise. Our tool for embedding optimal operator ordering into TensorFlow Lite models is available at https://github.com/oxmlsys/tflite-tools.

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Appendix A

Figure 2: Memory usage of the sample computation graph with default operator ordering.

Figure 3: Memory usage of the sample computation graph with optimised operator ordering.