LETTER

A Parasitic Elimination Bootstrapped Switch and A Fast Settling Residual Amplifier for High-Speed and High-Resolution Pipelined ADC

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Abstract This letter proposes a parasitic elimination bootstrapped switch and a fast settling residual amplifier to be used in multiplying digital-to-analog converter (MDAC) in order to improve the performance of pipelined ADC at high frequency. The parasitic elimination bootstrapped switch improves the sampling spurious free dynamic range (SFDR) by more than 6dB by shielding the nonlinear parasitic capacitance of the MOS transistor substrate. In addition, at high frequency, the negative zero point introduced by the later stage switch-capacitor circuit (which is easy to be ignored) will seriously deteriorates the settling time of residual amplifier in the former stage. A new zero-pole elimination technique is proposed, which greatly reduces the settling time of residual amplifier by nearly 11% and further improve the performance of MDAC. Simulated in 28nm CMOS technology, as the input signal is 1.38GHz, the former stage of the pipelined ADC implements high-speed high-resolution to obtain a SFDR of 75.77dB and a signal-to-noise-plus-distortion ratio (SNDR) of 68.05dB at a sampling frequency of 2.2GS/s.

Key words: pipelined ADC, bootstrapped switch, residual amplifier, MDAC

Classification: Integrated circuits

1. Introduction

Driven by wireless transceivers and mm Wave radios, high-speed and high-resolution analog-to-digital converters (ADC) [1, 2, 3] is widely used in broadband communication, digital phased array radar and other systems. Pipelined ADC can provide better trade-off in speed and resolution and is more attractive than other architectures, such as flash [4, 5, 6], folding [7, 8], successive approximation register (SAR) [9, 10, 11], sigma-delta [12, 13, 14] and so on. In recent years, many techniques have been proposed to improve the pipelined ADC core by the error calibration [15, 16, 17], but there were not much progress in reducing the error itself. This letter is focused on reducing the error of sampling switch and the settling time of residual amplifier of MDAC in high-speed and high-resolution pipelined ADC.

In high-speed and high-resolution pipelined ADC, the sampling switch must sample the input signal within a very short time and must ensure the accurate charging of sampling capacitor. The bootstrapped switch with deep n-well (DNW) is proposed and optimized in order to reduce distortion and improve the linearity of the sampling signal, but the linearity of the conventional bootstrapped switch deteriorates at high input frequency. Although various optimization techniques have improved the linearity of the bootstrapped switch [18, 19, 20], most of their purpose is to reduce the nonlinear parasitic capacitance of key nodes rather than find a way to shield it.

The settling time of residual amplifier [21, 22, 23] of MDAC block is another important factor that limits the performance of pipelined ADC. In general, when the current stage pipeline works in the hold phase, the switch-capacitor circuit (SC) circuit of the later stage pipeline works in the sampling phase as a load, as shown in Fig.1. In order to reduce the influence of thermal noise on signal-to-noise ratio (SNR), pipelined ADC usually adopts relatively large sampling capacitance. The on-resistance of the sampling switch and the sampling capacitor in series will introduce a negative zero point at the output of the residual amplifier. When the sampling rate of pipelined ADC is low, the residual amplifier needs a lower GBW. This negative zero is located at a relatively high frequency, which will not affect the settling of residual amplifier. Unfortunately, when the sampling rate of pipelined ADC reaches GS/s, the residual amplifier needs a considerable GBW to meet the requirements of high sampling rate. At this time, this negative zero is located at a relatively low frequency, which will seriously deteriorate the settling time of residual amplifier and deteriorate the performance of the pipelined ADC [24].

This letter introduces a bootstrapped switch with parasitic elimination technology to increase the sampling SFDR by adding source-bulk resistances at the key nodes of the conventional design. This technology basically has no hardware overhead. In addition, to push the sampling rate of a single channel pipelined ADC into GS/s rate region, high-speed high-bandwidth residual amplifier are required [25]. Considering the negative zero point introduced by the later stage SC circuit, a new zero-pole elimination technique is proposed to the former stage, which greatly improves the settling time of residual amplifier and improve the performance of MDAC.

The remainder of this paper is organized as follows. Section 2 introduces the parasitic elimination bootstrapped switch. Section 3 shows the details of the fast settling residual amplifier. Section 4 presents the simulation results. Section 5 draws the conclusions.

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2. The parasitic elimination bootstrapped switch

The Top-level block diagram of N-stage MDAC inside the pipelined ADC is shown in Fig. 1, in which two adjacent stages are shown in details. The linearity of the sampling switches, like \(\Phi_{s[i]}\) and \(\Phi_{s[i+1]}\) in Fig. 1, directly impact the total pipelined ADC’s performance. As ADC run faster with GS/s sampling rates, and the input frequencies rise up to the GHz range, the input sampling problem has become more challenging. The bootstrapped circuit used as each sampling switch is shown in Fig. 2. While the bootstrapped switch with DNW is applied for linear sampling [26, 27], its nonlinear signal-dependent on-resistance and parasitic capacitance become more pronounced at high input frequency, thus seriously degrade the linearity.

As an NMOS sampling switch, the on-resistance is

\[
R_m = \frac{1}{\mu_C \text{\L} \left( W_\text{Vgs} - V\text{th} \right)}
\]

In Fig. 2, according to the above formula, ideally, \(V\text{gs}\) and \(V\text{th}\) of the sampling transistor \(M_8\) is signal-independent in order to afford a constant switch on-resistance \(R_{DS}\). During the sampling phase, the internal node \(V_X\) rises to approximately \(V_m + VDD\) to boost the gate voltage of the sampling switch transistor by the bootstrapped capacitance \(C_b\). In order to prevent the \(V\text{th}\) change caused by the bulk effect of MOS transistors \(M_2\) and \(M_6\), their bulk terminals are connected to the source terminal instead of \(V\text{gs}\) and \(VDD\).

Although the source and bulk terminals of \(M_2\) and \(M_6\) are connected to eliminate the body effect, the parasitic capacitance between P-well and DNW \((C_{pw})\) and the parasitic capacitance between DNW and P-sub \((C_{p2})\) will introduce a low impedance path to \(VSS\) and deteriorate the linearity, especially at high frequencies. Simulations show that placing the MOS transistor in a P-well and connecting the transistor’s source to bulk offers no SFDR improvement. The contribution of the body effect elimination is cancelled by the increased loading from the nonlinear capacitance \((C_{p1}\) and \(C_{p2}\)) at the key nodes \(V_X\) and \(V_B\) [28]. Similar effect would occur in PMOS [29]. The nonlinear capacitance of \(V_X\) and \(V_B\) can be expressed as

\[
C_{p1} = \frac{C_{pw} C_{p2}}{C_{p1} + C_{p2}} + C_{p3}
\]

\[
C_{p2} = \frac{C_{pw}}{C_{p1} + C_{p2}}
\]

The bulk connecting \(M_2\), \(M_6\) and \(M_8\) adds a large nonlinear capacitance \(C_{p3}\) to the \(V_X\) and \(V_B\) nodes, which reduces the sampling linearity. This is due to voltage division between the bootstrapped capacitance \(C_b\) and the nonlinear capacitance \(C_{p3}\). Fig. 2(b) shows the equivalent circuit of the conventional bootstrapped switch during the sampling phase. The voltage transfer function from \(V_{in}\) to the \(V_G\) of \(M_i\) can be expressed as

\[
V_G = \frac{V_{in} \left( R_{C1}(C_{s} + C_{p3}) + C_b + C_{p3} + C_G \right)}{R_{C1}(C_{s} + C_{p3}) + C_b + C_{p3} + C_G}
\]

where \(R_{C1}\) is the on-resistance of \(M_8\) and \(C_G\) is the parasitic capacitance on the gate of \(M_4\). In order to simplify the expression and make the result more intuitive, we ignore the on-resistance of \(M_6\) and \(M_1\). The conventional bootstrapped switch’s phase shift from \(V_{in}\) to \(V_G\) can be expressed as

\[
\phi_{\text{conv}} = -\arctan \left( \frac{R_{C1}(C_s + C_{p3})\omega_{\text{in}}}{C_b + C_{p3} + C_G} \right)
\]

where \(\omega_{\text{in}}\) is the input frequency. Due to the nonlinear \(R_{C1}\) and \(C_{p3}\), \(\phi_{\text{conv}}\) inevitably becomes time-varying, thus distorting \(V_G\) [30]. The phase shift from \(V_{in}\) to \(V_G\) is the main cause of sampling nonlinearity. If \(C_b\) is much larger than \(C_{p3}\), \(C_{p3}\) can obtain almost all the voltage and improve the nonlinearity caused by \(C_{p3}\). A large \(C_b\) increases the turn-on time of the sampling switch, which is challenging under high-speed sampling.

To solve this problem, a technique to eliminate nonlinear parasitic capacitance is proposed, as shown in Fig. 3. A large resistor \(R\) is added between the source and bulk of the MOS transistor \(M2\), \(M6\) and \(M8\), respectively. At high frequency, the nonlinear parasitic capacitance at the key nodes \(V_X\) and \(V_B\) is invisible by \(R\). Then the impedance seen
from the MOS source terminal can be expressed as
\[ Z = R + \frac{1}{j\omega C_p} \approx R \] (6)

At the same time, the \( R \) can provide a stable voltage \( V_{\text{BS}} \) for the source terminal and bulk terminal of the MOS transistor. The constant \( V_{\text{BS}} \) of MOS transistor would not be affected by the nonlinear parasitic capacitance and hence the linearity is improved. This technology can be applied to input buffer and sampling switch to improve the linearity of output signal.

Fig. 3(b) shows the equivalent circuit of the parasitic elimination bootstrapped switch during the sampling phase. The voltage transfer function from \( V_{\text{in}} \) to \( V_O \) can be expressed as
\[ V_O = \frac{R C_s s}{(1 + R C_s s)(1 + R C_s s) + R C_G s} \] (7)

At high frequencies, \( |R C_s s| >> 1 \), formula (7) can be approximated as
\[ V_O = \frac{C_L}{R C_s C_s s + C_b + C_G} \] (8)

And the parasitic elimination bootstrapped switch’s phase shift from \( V_{\text{in}} \) to \( V_O \) can be expressed as
\[ \phi_{\text{prop}} = \arctan \frac{R C_s C_s \omega_n}{C_b + C_G} \] (9)

Comparing (5) with (9), we note that the nonlinear parasitic capacitance \( C_{\text{p}} \) is eliminated in the proposed circuit, which optimizes the linearity of \( V_O \), and thus improves the linearity of the sampling switch.

To demonstrate the effectiveness of the proposed solution, we simulate the conventional and proposed bootstrapped switches and compare their SFDR across the input frequency range. The size of the devices other than the source-bulk resistors are set the same between the two circuits for fair comparisons. Sampling at 2.2GHz, and with a sine wave input amplitude of 400 mV, simulations show that the conventional bootstrapped switch obtains an SFDR of about 114 dB and 93 dB with low- and high-frequency (94.5MHz and 5.6GHz) inputs, respectively, while the proposed bootstrapped switch obtains an SFDR of about 120 dB and 100 dB respectively. An average 6-dB improvement over the input frequency range is obtained. Here, we propose the parasitic elimination technique to improve the bootstrapped switch and this technique can be used standalone or in conjunction with the prior arts earlier.

3. The fast settling residual amplifier

While very fast switches, comparators and logic can be realized in 28nm CMOS technology, the ADC speed and power are primarily limited by the amplifiers. The output of the amplifier should settle within a specified tolerance of its steady-state value prior to the next sampling instant [31]. Therefore, the residual amplifier should have sufficient GBW to quickly complete the establishment of the output voltage. The GBW of the residual amplifier in the current stage of the pipelined ADC, using OPA, in Fig.1 as an example, can be expressed as
\[ \text{GBW} \geq \frac{f_s \sin \beta}{2^{N-M+1}} \] (10)

where \( f_s \) is the sampling frequency of the pipelined ADC, \( \beta \) is the feedback factor, \( N \) is the resolution of the pipelined ADC, \( M \) is the effective bits of the former-stage output (eg. Output of OPA in Fig.1). Formula (10) indicate that for a fixed feedback factor and the resolution of a pipelined ADC, GBW increases with the increase of sampling frequency.
When the pipelined ADC works normally, the SC circuit of the later stage acts as the load of the former-stage residual amplifier. Fig. 6 shows the equivalent circuit of the SC circuit as a load. The voltage transfer function from $V_{in}$ to $V_{out}$ can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{R_z + 1/sC_z}{Z_{out} + R_z + 1/sC_z}$$  \hspace{1cm} (11)

where $Z_{out}$ is the output impedance of the former-stage residual amplifier of MDAC, $R_z$ is the on-resistance of the sampling switch in later stage of SC circuit, $C_z$ is the sampling capacitance of the later stage of SC circuit. Formula 11 indicates that the SC circuit is used as the load. A negative zero point ($-1/R_z C_z$) is introduced into the system and the main pole of the original circuit is reduced (from $-1/Z_{out} C_z$ to $-1/(Z_{out} + R_z) C_z$). In order to achieve SNDR improvement and reduce layout area, the value of $C_z$ and $R_z$ should not be too small, especially in the former stages of pipelined ADC [32]. Therefore the negative zero will be at a lower frequency.

For a pipelined ADC with low sampling frequency, the residual amplifier has sufficient time to complete the establishment without high GBW. The negative zero introduced by SC circuit is much greater than 10 times of GBW, which will not affect the phase of the residual amplifier. At this time, the residual amplifier is still approximately a two pole system with no zero points. The negative zero will not worsen the settling time of the system. Unfortunately, for a pipelined ADC with a sampling frequency above GHz, the performance requirements of the residual amplifier are undoubtedly very harsh, requiring a large GBW to ensure the settling speed. At this time, the frequency of negative zero is less than 10 times GBW, the residual amplifier is approximately a two-pole system with a negative zero point at low frequency. This will significantly affect the magnitude- and phase-frequency characteristics of the residual amplifier, and further deteriorate the settling time of the residual amplifier and the SFDR of pipeline ADC.

To achieve quick settling speed, a residual amplifier with complementary telescopic cascode amplifier is used and shown in Fig. 7 in a MDAC configuration. The complementary topology nearly doubles the total transconductance of the amplifier without increasing power, leading to 2x improvements in DC gain and GBW. Gain boosters (A1, A2) are employed to provide high DC gain, which can simplify the digital correction. The residual amplifier is applied in each stage of the MDAC. During the hold phase, a relatively low frequency negative zero point ($-1/R_z C_z$) is introduced at node Y. Simulation AC responses of the residual amplifier is shown in Fig. 8.

To solve this problem, a residual amplifier with zero-pole elimination technique is proposed. A low-frequency pole point is introduced at node X by adding a resistor at the input of the residual amplifier to eliminate the low-frequency negative zero point generated above. According to Miller approximation, the frequency of pole point at node X can be expressed as

$$\omega_{p,x} = -\frac{1}{R[C_{g1} + 1 + g_{m1}(\frac{r_{d3}}{1 + g_{m1}(A_{aux} + 1)r_{d3}})C_{g1}]}$$  \hspace{1cm} (12)

where $R$ is the compensation resistance connected to the input of the residual amplifier, $A_{aux}$ is the gain of the auxiliary amplifier. The capacitance at node P1 is approximately

$$C_{p1} \approx [1 + g_{m1}(\frac{r_{d3}}{1 + g_{m1}(A_{aux} + 1)r_{d3}})r_{d3}]C_{g1}$$  \hspace{1cm} (13)

where the other parasitic capacitance are relatively small and ignored. The frequency of pole at node P1 can be expressed as

$$\omega_{p,p1} = -\frac{g_{m1}}{C_{g1}}$$  \hspace{1cm} (14)

In general, the frequency of pole at node P1 is much smaller than GBW, which can greatly reduce the settling error of the system. The frequency $\omega_{p,x}$ is often much larger than GBW, but $\omega_{p,p1}$ can be made smaller by changing the compensation resistance $R$.
higher than that at node X. Therefore, the pole at node X is optimized and shifted to the frequency of the negative zero point at node Y. Let formula (12) be equal to \(-1/R_c C_s\). The value of R can be expressed as

\[
R = \frac{R_c C_s}{C_{GS1} + \frac{1}{1 + g_{sa}(A_{in} + 1) R_c s}}
\]

(15)

The value of compensation R is obtained by formula (15). All other devices have the same sizes between the two designs. The compensation resistance at the input of residual amplifier successfully eliminates the negative zero point and the AC response curve is smoother.

- Fig. 8 Simulated AC responses without R and with R compensation
- Fig. 9 Simulated settling time after compensation of on-resistance of different sampling switch
- Fig. 10 The conceptual view of the settling time of residual amplifier before and after compensating negative zero point

which will further improve the performance of the MDAC.

4. Simulation results

The proposed bootstrapped switch and residual amplifier are applied to the MDAC inside a 7-stage pipelined ADC with a standard 28nm CMOS technology. In a pipelined ADC, the value of sampling capacitance and the GBW of residual amplifier decrease with the increase of pipelined stages. Therefore, the negative zero point introduced by SC circuit will seriously deteriorate the former stages of the pipeline. As an example, the 3rd stage of the pipelined ADC is simulated with an input frequency of 1.38GHz and a sampling frequency of 2.2GS/s.

The output spectrum of the conventional and proposed MDAC in the 3rd stage of pipelined ADC are shown in Fig. 11. The SFDR and SNDR of the conventional MDAC in the 3rd stage of the pipelined ADC are 56.44dB and 48.23dB, respectively, where 75.77dB and 68.05dB are achieved for the proposed design.

Fig. 12 plots the SFDR versus the input frequency at a sampling frequency of 2.2GS/s. An improvement of at least 12.88dB is achieved, which demonstrates the effectiveness of the proposed solution in MDAC.

5. Conclusion

In this letter, the parasitic elimination bootstrapped switch and a fast settling residual amplifier is proposed to improve the linearity of input signal and the performance of MDAC in pipelined ADC at high frequency. The parasitic elimination bootstrapped switch improves the sampling SFDR by more than 6dB by adding source-bulk resistances to shield the nonlinear parasitic capacitance of the MOS transistor substrate. The new zero-pole elimination
technology greatly reduces the setting time of residual amplifier by nearly 11% and further improves the performance of the MDAC. Simulated in 28nm CMOS technology, as the input signal is 1.38GHz, the 3rd stage of the pipelined ADC implements high-speed high-resolution which obtains SFDR of 75.77dB and SNDR of 68.05dB at a sampling frequency of 2.2GS/s. The proposed design can be widely applied in high-speed and high-resolution ADC designs.

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