Four-channel radio-frequency signal generator programmed by an open-source Arduino-based control system via single or quad Serial Peripheral Interface

Michele Sorelli\textsuperscript{a,b}, Marco Marchetti\textsuperscript{c}, Pietro Ricci\textsuperscript{a,b,d}, Domenico Alfieri\textsuperscript{c}, Vladislav Gavryusev\textsuperscript{a,b,*}, Francesco Saverio Pavone\textsuperscript{a,b,e}

\textsuperscript{a} University of Florence, Department of Physics and Astronomy, Sesto Fiorentino, 50019, Italy  
\textsuperscript{b} European Laboratory for Non-Linear Spectroscopy, Sesto Fiorentino, 50019, Italy  
\textsuperscript{c} L4T-Light4Tech, Sesto Fiorentino, 50019, Italy  
\textsuperscript{d} University of Barcelona, Department of Applied Physics, Barcelona, 08028, Spain  
\textsuperscript{e} National Institute of Optics, Sesto Fiorentino, 50019, Italy

vladislav.gavryusev@unifi.it ‘twitter: @VGavryusev’

Abstract

Radio-frequency (RF) signal generators are standard laboratory equipment and a wide-range of open-source and commercial devices exists to address their many applications. Nonetheless, only few expensive and proprietary solutions can be re-configured within a wide frequency band and triggered on a micro-second timescale. Such specifications are required for applications that use variable radio-frequencies to generate programmed mixed signals, to control processes or states and to precisely steer laser beams using acousto-optical devices, tasks often needed in industrial manufacturing, atomic and molecular physics or microscopy.

Here we present an open-source low-cost Arduino-based control system that can store up to millions of commands received from a computer and then perform reliable high-speed programming of an arbitrary device under its control (DUC) via a single- or quad-wire Serial Peripheral Interface. The software architecture operates as a real-time state machine, making it easily extensible and adaptable to any DUC. Each configuration change can be triggered either externally or internally, reaching \( \approx 1 \text{MHz} \) rates when using a Teensy 4.1 Arduino-compatible board. Leveraging this flexible system, we developed a programmable four-channel RF signal generator, based on an Analog Devices 9959 Evaluation board, and we demonstrated its capability and validated its performance.

Keywords
Low-cost; high-speed device control; Arduino; Teensy; radio-frequency signal generator; Serial Peripheral Interface
| Specifications table                                                                 |
|-------------------------------------------------------------------------------------|
| **Hardware name**                                                                     | Programmable four-channel radio-frequency signal generator |
| **Subject area**                                                                      | • Engineering and material science  
                                        | • Physics                                                        |
|                                                                                      | • Open source alternatives to existing infrastructure        |
| **Hardware type**                                                                     | • Electrical engineering and computer science               |
|                                                                                      | • External device control and programming                   |
| **Closest commercial analog**                                                         | Multi-channel programmable radio-frequency signal generators, such as Wieserlabs WL-FlexDDS-NG. |
| **Open source license**                                                               | CC-BY Attribution-ShareAlike 4.0 International (CC BY-SA 4.0) |
| **Cost of hardware**                                                                  | 641.79 €                                                     |
| **Source file repository**                                                            | Mendeley Data https://doi.org/10.17632/hvwy5yhh2.1           |
1. Hardware in context

Radio-frequency (RF) signal generators are devices designed to produce continuous and pulsed signals in the RF and microwave domains with defined and adjustable frequency, phase and amplitude. Often they provide one or several methods to modulate these properties in order to create a continuous-wave (CW) output, single pulses, pulse trains or more complex waveforms. These devices have a wide-range of applications, both in industrial, commercial and laboratory settings, spanning from wireless communication, automated test equipment, imaging and spectroscopy for healthcare to experiments in neuroscience [28, 32, 51], biophysics [22, 19], microscopy [44, 23], particle and nuclear physics [20], atomic and molecular physics [41, 21, 16], and quantum simulation and computing [14, 4, 5]. There is no single general purpose instrument that is able to cover such breadth of scopes and technical requirements, instead many open-source and commercial solutions have been developed to address one or several tasks, with their specific strengths, limitations and cost.

Recently, RF equipment has found vast application in industrial manufacturing, atomic physics and microscopy to precisely steer laser beams using RF-driven acousto-optical devices [23, 24, 43, 42] and to control processes or states of matter that are sensitive to this frequency domain [14], either directly through electromagnetic radiation emitted by an antenna or indirectly by driving electronic or opto-electronic equipment. Achieving a fine degree of control often requires to generate complex sequences of single RF tones, multi-frequency waveforms and rapid frequency sweeps that interleave on microsecond timescales and span a wide band of several hundreds MHz. Most often a single RF output is not sufficient and typically four channels or more have to be used concurrently, while respecting stringent phase-coherence and sub-µs synchronization conditions.

Arbitrary waveform generators (AWG) are a very flexible class of RF devices that can fulfill these demands. Commercial solutions [45, 46, 3] tend to have a substantial Cost Per Channel (CPC) in the range of 2000-3000 €, while laboratory developed solutions [15, 17, 25] are more affordable. These projects are based on field-programmable gate arrays (FPGA) that are very flexible and adaptable to changing requirements, but often their frequency bandwidth is limited to few tens of MHz. Besides, they present usability constraints because their software interfaces are often not trivial to program and integrate into existing laboratory control systems.

RF devices that employ Direct Digital Synthesis (DDS) to produce high spectral purity single-tones and frequency sweeps are a second valid class of solutions. Current state-of-the-art technology allows to manufacture DDS chips that can synthesize 1.4 GHz sine-waves, such as the Analog Devices (AD) AD9914 [10, 11], or even reach 4.2 GHz [52], but their CPC is rather high in the range of 800-1000 €. More affordable generators are built using one or several DDS chips that cost approximately 50 € each and can provide a 200 MHz to 400 MHz output, such as the four channel AD9959 [6, 7] and the single channel AD9910 [8, 9] chips. Many commercial products have been developed using these or similar DDS technologies and the most accessible multi-channel equipment [2, 36, 18, 1] has a CPC within 50-200 €, but is severely limited in the Output Reprogramming Rate (ORR ≤ 10 kHz). Higher speed RF drivers reach an ORR ≥ 1 MHz by leveraging a built-in memory that can store thousands of consecutive settings received from a computer, allowing output stabilization and amplification, and complex modulation schemes, with the downside of a significantly increased CPC ranging from 500 €34, 31, 27 to 2000-3000 €47, 48, 49, 50, 33. Several research groups have developed in-house DDS-based signal generators to reach an affordable CPC of 250-400 €, while preserving specifications comparable to the best commercial products or even adding customized functionality, such as digital input-output channels or a complete experiment timing and control system [41, 38, 40, 21, 16, 3]. Like for AWGs, FGPsAs have been used to program and control the DDS chips with ORR ≥ 1 MHz, sub-µs jitter triggering and providing a large command memory. Some designs have been presented without disclosing the implementation details [30, 29, 38, 21], while others have released all material as open-source [41, 16, 27]. Whilst complying with the license terms, the latter choice enables any user to reproduce, enhance and adapt the equipment to their own specific requirements way beyond what a proprietary solution can allow, while substantial economic savings may be obtained [37]. Furthermore, the original developers receive recognition for their work and may benefit from improvements contributed by the wider community of users.

Recently, the development of microcontroller units integrated into a development board (MCU) with ARM central processing units (CPU) running at clock rates of tens of MHz has paved the way to an alternative to FGPs for achieving negligible jitter, substantial command storage capacity and ORR ≥ 1 MHz. This approach presents several advantages: MCUs such as the broad Arduino-compatible family of devices [13] are
programmed in C++, instead of requiring knowledge of the more specialized VHDL and VERILOG languages, which lowers the usage barrier and vastly broadens the potential user community. Next, MCUs have longer product lifetimes than FPGAs and provide notably greater software and hardware compatibility between different product generations, including application programming interfaces, communication buses and even dimensional blueprints which even enable drop-in replacements or upgrades. This feature stimulates the creation and continued support of extensive software libraries that ease the firmware development and of interoperable off-the-shelf hardware plugins and extensions. Additionally, MCUs provide several standardized communication interfaces that may allow interacting with arbitrary devices under control (DUC) that present the same protocol, such as the Inter-Integrated Circuit (I2C) and Serial Peripheral Interface (SPI). Interestingly, this may obviate the need of realizing custom printed circuit boards (PCB) to pilot a DDS or another DUC. All together these aspects help to reduce development time and CPC expenditure.

This paper presents an open-source low-cost Arduino-based control system that can store millions of commands received from a computer (PC) via Universal Serial Bus (USB) and perform reliable high-speed programming of an arbitrary device under its control through a single- or quad-wire SPI. We use a Teensy 4.1 development board [39] as the MCU. The Teensy 4.1 is an Arduino-compatible development board with an ARM Cortex-M7 CPU running at 600 MHz, which grants it several times more computing power than provided by the 84 MHz ARM Cortex-M3 CPU of an Arduino Due [12]. The controller software architecture operates as a real-time state machine, making it easily extensible and adaptable to any DUC. Each configuration change can be triggered either externally or internally, with rates up to $\approx 200 \text{kHz}$ when using the standard SPI library. Outstandingly, if the standard single-wire SPI library is replaced by a custom implementation that benefits from port masking optimizations, the ORR rate doubles in single-wire SPI mode and reaches $\approx 1 \text{MHz}$ with quad-wire SPI communication, surpassing all prior MCU-based solutions [18, 2]. Leveraging this flexible system, we developed a low-cost programmable four-channel RF signal generator, based on an Analog Devices 9959 evaluation board [6, 7], and demonstrated its capability, validating its performance for all use-cases that require $\text{ORR} \leq 1 \text{MHz}$, low jitter and stand-alone operation with large command memory. The total system cost is currently $641.79 \text{ €}$, resulting in a notably low CPC of $160.45 \text{ €}$.

First, we present an overview of the hardware and software that composes our system. Then, all design files and materials are provided and discussed, along with build and operation instructions. Finally, we measure and validate the performance of our open-source programmable four-channel RF signal generator controlled by an Arduino-based MCU.

2. Hardware description

2.1 Overview

The design of the programmable four-channel RF signal generator that we developed is based on a general purpose and flexible architecture made of four main elements: the user determines on a PC the set of commands and settings that the MCU has to program into the DUC with precise timing supplied either internally or externally through a timing system. The MCU software implements a real-time state machine that can receive new settings and commands during run-time, store them in a fast internal memory, control the DUC and react to external events. The block diagram of the system is shown in Fig. 1 and its elements will be presented in detail in the following.

2.2 Hardware components

The central hardware element of our architecture is the MCU hosted on a development board because it interfaces the PC with the DUC and acts as a hardware and software abstraction layer, lifting from the user the need of knowing the technical details of the device to be controlled. Thanks to its built-in memory, the MCU can work both in tandem with the PC, receiving new commands during run-time, or standalone after storing the sequence of commands and settings to be applied to the DUC. Furthermore, it can be either externally triggered or perform timing functions itself since almost all microcontroller development boards provide many digital and some analog input and output (IO) channels.
We chose to use a Teensy 4.1 development board [39] as the MCU because it is currently the most powerful Arduino-compatible solution [13]. Its software is programmed in C++ (described in detail in the following Sec. 2.3), a language which many developers and researchers can work with, granting a large potential user community, instead of the more specialized VHDL and VERILOG languages that are required to operate most FPGAs. The Teensy has an ARM Cortex-M7 CPU with a float point math unit running at 600 MHz which provides several times more computing power than the 84 MHz ARM Cortex-M3 CPU of an Arduino Due [12]. This enables to process input data and IO communications with sub-µs timescale latency and jitter, both via USB 2.0 (with the PC) and SPI interfaces (with the DUC) or I²C. It has a total of 55 IO pins with different characteristics, making it capable of reacting to external events and providing precise triggering to the DUC. Several sets of four IO pins can be toggled together very quickly using a hardware-based port mapping optimization, a feature that we leveraged to implement a custom single- and quad-wire SPI that significantly increased the data rate with the DUC, as demonstrated in Sec. 7. Furthermore, this MCU has a large memory subsystem consisting of a 1024K random-access-memory (RAM), 7936K Flash, 4K EEPROM and with the option of QSPI memory expansion up to 16 MByte by soldering two extra RAM chips. Notably, the interaction with the PC can be realized not only via USB, but also through the Ethernet 10/100 Mbit interface. This option has not been implemented in our project, but should be easy to add through an existing library.

The computer has no special hardware requirements and can run any operating system that supports the Python Jupyter notebook software package and USB or Ethernet communication. The timing system has to provide five interrupts for the MCU and five triggers for the DUC (as shown in Fig. 3 and presented in detail in Sec. 5), totaling a requirement of ten digital transistor-transistor logic (TTL) channels, and can be either a standalone device or a board integrated in the PC, such as the National Instruments (NI) board PCI-6251 [35] that we used in our implementation. This PCI Multifunction I/O Device has 16 analog inputs (16-Bit, 1.25 MegaSamples/s), 2 analog outputs and 24 digital IO, out of which 8 can be timed up to 10 MHz. One of its TTL lines is logically combined through an OR gate circuit (Fig. 2(B)) with a TTL line from the MCU to generate a logic signal that triggers the output update on the DUC.
The MCU can be engineered and programmed to control any DUC that provides a supported interface, such as SPI and I²C. Since we aimed to realize an open-source low-cost programmable four-channel RF signal generator, we leveraged the capabilities of the Arduino-based control system to drive an AD9959/PCBZ evaluation board [7]. This off-the-shelf equipment uses an AD9959 DDS chip [6] which provides four synchronous RF outputs that can reach 200 MHz, generate single tones and linear frequency/phase/amplitude sweeps, and has independent frequency/phase/amplitude control. This RF source presents a narrow output spectrum with low phase-noise and it has 12 Hz or better frequency tuning resolution, 14-bit phase offset resolution and 10-bit output amplitude scaling resolution. To operate, it requires two supply voltages (+1.8 V DDS core and +3.3 V serial I/O) and a stable and spectrally narrow sinusoidal frequency reference that can be provided either by soldering on-board a crystal oscillator or supplying a clock signal externally. The clock signal is fed into a phase-locked loop (PLL) where a selectable 4× to 20× REF_CLK multiplier is applied to generate the internal clock signal that provides timing to all internal components of the DDS chip and determines the maximum RF frequency that can be generated without incurring in spectrum distortions, which is 40% of this rate. As clock signal source, we used an external 25 MHz temperature compensated crystal oscillator with a frequency stability of ±280 parts per billion, assembled following the schematic presented in Fig. 2(A).

The MCU is powered directly by the PC through the USB cable, while all other components of our programmable four-channel RF signal generator receive the required +3.3 V and +1.8 V supply voltages from the power supply circuit that consists of an AC/DC and a DC/DC converters, as depicted in Fig. 2(C).

2.3 MCU software

The MCU software loaded into the Teensy 4.1 board implements a real-time state machine able to listen to any incoming serial USB communication from PC, and to execute a set of predefined commands in response to external interrupt events. Here we will present its architecture in more detail.

The setup() function initializes the state machine when the software is first loaded into the MCU board and configures the digital pins needed to interact with the DUC and the external timing system. Moreover, upon setup a hard reset signal is issued to the DUC to force its internal registers to their default state. Next, depending on the selected reference clocking configuration, the internal PLL-based clock multiplier factor is optionally set by programming the Function Register 1 (FR1) of the DUC via SPI. Finally, the serial USB communication between the PC and the MCU board is initialized, and external interrupt requests (IRQs) are enabled.

The I/O block handling the reception of subsequent DUC settings from the PC is realized by two functions that are executed consecutively within the loop() function of the MCU sketch. Respectively, they read and parse incoming data strings, and push the received DUC configurations into the first in, first out (FIFO) buffers allocated for each of the four DDS channels. Similarly, there are separate sets of FIFO buffers designated for each specific channel register to be programmed into the DUC (refer to the AD9959 datasheet for a complete description of these registers). The size of the FIFO buffers was set to 4500 elements to maximize the usage of the dynamic memory normally accessible on the Teensy 4.1 board (RAM1). This size corresponds to the maximum number of output configurations that can be activated on the DUC without the need for a new USB communication when all four RF channels are simultaneously updated and operated in frequency sweep mode, which represents the most memory-consuming scenario. If such use-case would not be foreseen, the number of elements could be increased by adapting the software to the expected workload. Furthermore, this threshold may be heightened by exploiting the secondary RAM space (RAM2) through dynamic memory allocation via the malloc() function and by QSPI memory expansion, as mentioned in the previous subsection. Before writing data to these memory buffers, the received floating point frequency values (namely single-tone frequencies, frequency sweep limit frequencies and step sizes) are converted to the tuning data words to be programmed into the respective internal registers of the DUC. In fact, performing this conversion directly when receiving the data strings from the PC enables a faster refresh of the DUC, increasing the maximum achievable ORR.

External interrupt events are used to react asynchronously to specific user commands set on the PC and they are disabled during the USB and SPI communication sessions. They are activated on the rising edge of the toggling of the designated interrupt pins that are connected to the external timing lines, as presented in detail in Sec. 5. The interrupt service routines (ISRs) are the following:
• *initSingleSPI()*: enables the custom single-wire SPI communication mode (default), with the simultaneous control of the designated SDIO_0 and SCLK pins implemented via direct digital port manipulation;

• *initQuadSPI()*: enables the custom quad-wire SPI communication mode, which uses an efficient hardware implementation based on the fast simultaneous control of the designated SDIO pins via direct digital port manipulation;

• *softResetMCU()*: resets all MCU state variables to their default values, and clears the content of the FIFO buffers that store DDS tuning words previously received from the PC and not yet activated on the DUC;

• *hardResetDUC()*: issues a master reset pulse on the active-high reset pin of the DUC, reinitializing its internal registers to their default state. Afterwards, all channels are set to the single-tone mode of operation with their default 0x00 frequency tuning words, i.e. 0 MHz. Then, if required, the routine programs the PLL multiplier factor back to the user-set value;

• *updateDUC()*: this routine first retrieves and interprets a channel configuration byte header associated with each data string communicated to the MCU, properly adjusting the mode of operation (i.e., single-tone or linear frequency sweep) of the relevant channels which need to be updated. More specifically, the least significant nibble of this header points out the channels operating in frequency sweep mode, whereas the most significant one identifies the reprogrammed channels, in accordance with the structure of the DUC channel selection register, for a more efficient bit manipulation. Next, the ISR reads the new single-tone or sweep tuning words from the FIFO buffers of the channels which need to be updated, and transfers them to the DUC via SPI. In order to activate the received tuning words and effectively change the signal generator output, a trigger must be issued on the I/O update pin of the DUC after the SPI communication is complete. We implemented two options to generate this TTL: either the NI provides it, which requires careful synchronization with the execution of the update ISR, or the MCU itself supplies a pulse at the end of the data transfer. This latter approach, which we termed “auto update” mode, requires to activate a variable in the source code to be engaged, as described in item 7 of Sect. 6. Both options can work alternatively without hardware modification by using the digital logic OR gate circuit.

2.4 Computer software

The Jupyter notebook included in the software repository provides an easy-to-use user interface, written in Python 3.8, which allows to communicate to the MCU board the frequency settings to be consecutively activated on the DUC. All the functions included in the notebook are exhaustively documented, with docstrings complying with the PEP 257 convention.

As detailed in Section 6, users have only to edit the configuration lists within the “Input to AD9959 DDS” cell at the top of the notebook to customize the desired sequence of DUC settings. Whereas the specified single-tone frequency values can be directly transferred to the board, the generation of linear frequency sweeps by the AD9959/PCBZ evaluation board requires a conversion step of the user input. The desired positive or negative frequency slopes have to be translated into discrete time steps and intermediate frequency step sizes that are respectively applied when sweeping up or down the output frequency. This is performed by a dedicated block of chirp configuration functions which minimize the residual between the input chirp parameter and the slope of the linear sweep actually produced by the encoded sweep ramp rate and delta-tuning words, by iteratively selecting the adopted time step among a predefined list of increasing programmable values related to the DUC internal clock rate. Furthermore, also the transient phase leading to the maximum start frequency in the case of a falling frequency sweep, or back to the minimum frequency of a rising frequency sweep, must be similarly programmed. In the present implementation, this was accomplished so that the whole sweeping range was covered in the minimum time step allowed by the DUC, i.e. 8 ns at the peak 500 MHz clock rate, thus producing a quasi-instantaneous recovery of the user defined starting value.

The developed Jupyter notebook finally features a set of functions devoted to handling the USB communication with the MCU. These take the single-tone and frequency sweep data related to the user-defined consecutive configurations of the DUC output channels, generate the channel mode byte header described in Sect. 2.3, and composes the data strings which are finally encoded and transferred via USB to the MCU.
2.5 Device usefulness potential

In summary, the presented open-source programmable RF signal generator provides the following benefits:

- It has four outputs that can reach 200 MHz and operate in single-tone or frequency sweep modes.
- The generator output can be reprogrammed very quickly, up to \( ORR \approx 1 \text{ MHz} \).
- The hardware design and software are completely open-source, allowing easy extension and customization.
- All hardware components are off-the-shelf, for a total system cost of 641.79 € and a 160.45 € CPC, very competitive with commercial and lab-built RF generators with similar specifications and applications.
- The MCU software realizes a full control system that is adaptable to drive many other devices.

3. Design files summary

The design files are stored in the Mendeley repository and grouped in three folders:

- Software: it contains the MCU sketch and the PC to MCU communication code.
- Electronic Schematic: it contains the files describing the electronic design of the system.
- Documentation: it contains the datasheets for the components of the system.

The key design files necessary to build and operate the system are the following:

| Design filename         | File type            | Open source license | Location of the file           |
|-------------------------|----------------------|---------------------|--------------------------------|
| complete_code_pc_mcu.zip| code archive from GitHub [26] | MIT                | Mendeley/Software/             |
| python_pc.ipynb         | Jupyter notebook     | MIT                 | Mendeley/Software/python_pc/   |
| teensy_mcu.ino          | Arduino sketch       | MIT                 | Mendeley/Software/teensy_mcu/  |
| CircularBuffer-1.3.3    | Arduino library      | GNU GPL v3          | Mendeley/Software/teensy_mcu/lib/|
| BOM.ods                 | OpenDocument spreadsheet | CC BY-SA 4.0       | Mendeley/Electronic Schematic/ |
| Kicad_Circuits.zip      | Kicad project        | CC BY-SA 4.0        | Mendeley/Electronic Schematic/ |
| ElectronicSchematicsAll.pdf | PDF              | CC BY-SA 4.0        | Mendeley/Electronic Schematic/ |
| CircuitsClockORgatePWR.pdf | PDF         | CC BY-SA 4.0        | Mendeley/Electronic Schematic/ |
| PinConnections.pdf      | PDF                  | CC BY-SA 4.0        | Mendeley/Electronic Schematic/ |
4. Bill of materials summary

| Designator | Component | Number | Unit cost (€) | Total cost (€) | Source of materials | Material type |
|------------|-----------|--------|---------------|----------------|---------------------|--------------|
| MCU        | Teensy 4.1 development board | 1      | 31.53         | 31.53          | PJRC                | Other        |
| DUC        | AD9959/PCBZ | 1      | 494.80        | 494.80         | Analog Devices      | Other        |
| Clock      | CTS 535L250X2GT5 TCXO 25 MHz CLP SNW | 1      | 19.69         | 19.69          | Digi-Key            | Other        |
| OR         | SN74LVC1G3208DBVR AND/OR Logic gate | 1      | 0.38          | 0.38           | Digi-Key            | Other        |
| PWR1       | LRS-50-3.3 AC/DC Converter 3.3 V 33 W | 1      | 15.92         | 15.92          | Digi-Key            | Other        |
| PWR2       | TPS82671EVM-646 DC/DC Converter 1.8 V | 1      | 23.96         | 23.96          | Digi-Key            | Other        |
| ProtBoard  | SBBTH1506-1 prototype board | 3      | 1.09          | 3.27           | Digi-Key            | Other        |
| J1, J2, J3, J4 | RF2-04A-T-00-50-G SMA female jack through hole | 4      | 1.84          | 7.36           | Digi-Key            | Other        |
| CBsma      | Cable SMA-SMA male RG-316 0.5 m | 2      | 14.60         | 29.20          | Digi-Key            | Other        |
| CBusb      | Cable USB 2.0 A male to micro B male 5 m | 1      | 7.99          | 7.99           | Digi-Key            | Other        |
| C1         | Capacitor 10 nF 50 V | 1      | 0.19          | 0.19           | Digi-Key            | Ceramic      |
| C2, C4     | Capacitor 100 nF 50 V | 2      | 0.22          | 0.44           | Digi-Key            | Ceramic      |
| C3         | Capacitor 1 nF 50 V | 1      | 0.26          | 0.26           | Digi-Key            | Ceramic      |
| C5         | Capacitor 47 µF 25 V | 1      | 0.22          | 0.22           | Digi-Key            | Electrolytic |
| TVS        | SA7.0A-E3/54 Zener diode | 1      | 0.48          | 0.48           | Digi-Key            | Semiconductor |
| JP1, JP2   | SPC02SYAN jumper | 2      | 0.10          | 0.20           | Digi-Key            | Other        |
| CNm        | Header Connector 32 position 2.54mm through hole | 2      | 0.79          | 1.58           | Digi-Key            | Other        |
| CNf        | Receptacle Connector 32 position 2.54mm through hole | 2      | 2.16          | 4.32           | Digi-Key            | Other        |

The total cost of the components is 641.79 €, which leads to a CPC of 160.45 €.

5. Build instructions

In order to power the system we used the circuit depicted in Fig. 2(C), connected using common insulated wires. An AC/DC converter (PWR1) is directly wall powered and generates an output voltage of +3.3 V, which is filtered by capacitors C4 and C5 (electrolytic) and protected by the TVS Zener diode. For convenience, these three through hole components were soldered and linked on a ProtBoard perforated prototype board. A DC/DC converter (PWR2) is powered from the filtered +3.3 V line and produces a +1.8 V output when the
jumpers JP1 and JP2 are set in the pull-up position. The two voltage levels are necessary to power the DUC (AD9959/PCBZ evaluation board) via the TB1 connector. Additionally, both the OR gate and the clock source circuits adopted in the present application require a +3.3 V supply voltage.

The DUC requires an external 25 MHz stable clock reference to operate and reach its peak specifications. We selected a temperature compensated crystal oscillator (Clock) with a frequency stability of ±280 parts per billion and we assembled the schematic presented in Fig. 2(A) on a ProtBoard, soldering the through hole filtering capacitors (C1, C2, C3) and output SMA jack (J1). An SMA cable (CBsma) delivers the clock signal to the DUC via the J9 connector (REF CLK). In parallel, the W9 jumper had to be set to the REF CLK position. This reference clock was then brought to 500 MHz by employing the internal phase-locked loop-based reference clock multiplier of the DUC, as described in Section 6.

The logical OR gate circuit was soldered on the third ProtBoard, following the schematic presented in Fig. 2(B). The OR chip has its two inputs and single output wired to three SMA jacks (J2, J3, J4). The second SMA cable (CBsma) was cut in half and a two position connector (split-off either from the multi-position male header CNm or female receptacle CNf) was soldered on the loose end, with one pin attached to the inner signal line and the other to the outer shielding. The connector type (male or female) should be selected depending on the header type present on the MCU and DUC.

To power the MCU we opted to rely on the USB connector used for programming the board via the cable CBusb, instead of using an external power supply. Alternatively, 5 V may be supplied via the V_IN pin. However, for using the USB connection while employing an external power supply, the power provided by the USB cable should be properly isolated, so as to prevent the possibility of power flowing back to the PC. This can be accomplished by cutting apart the 5 V pads on the bottom side of the MCU board.

The MCU can control the DUC by establishing the connections illustrated in Fig. 3 to the I/O control headers. By default, the AD9959/PCBZ evaluation board is supplied with the USB communication enabled, a setting that disables these headers. To enact the external control of the DUC via the MCU, it is necessary to set the jumper W7 (PC_CTRL) to manual and remove those on W1, W2, W3 and W10 (highlighted with the blue dotted line in Fig. 3). Now, the MCU board must be connected to the header row (U2, U13) of the DUC, using, in particular, the PWR_DWN, RESET, IO_UPDATE and P0-3 (profile) pins, besides the pins related to the single/quad-wire SPI, i.e. chip select (CSB), serial clock (SCLK), SDIO_0, SDIO_1, SDIO_2 and SDIO_3. Since in the present application the DUC does not need to send a response back to the MCU board, a MISO
Figure 3: System assembly diagram. The positive power supply at 3.3 V and 1.8 V is shown in red, with the common ground of all devices shown in black. Digital inputs from the NI board are shown in orange, with dark orange indicating the IRQ lines connected to the MCU and light orange indicating the digital input lines to the DUC. Blue denotes the digital connections between MCU and DUC, with light blue indicating the shielded high-frequency transmission lines employed by the custom SPI developed in this work. The 25 MHz reference clock is shown in green, whereas the jumpers to be disconnected for enabling the manual DUC control and the external clock input are respectively highlighted in blue and green.
The ground pins next to these connections on the DUC header row must be coupled to the ground references on the MCU for avoiding ground loops. Similarly, the ground of the trigger generator used to control the operation timing must also be connected to the same ground reference. At both ends of each link, one or two position connectors split-off either from the multi-position male header CNm or female receptacle CNf and soldered to an insulated cable can be used to realize mechanically and electrically stable wiring.

The SPI communication between MCU and DUC was implemented in two alternative ways: via the standard single-bit SPI library or using custom functions performing single- or four-bit serial input operations. These functions use direct digital port manipulation for the fast simultaneous control of the designated SDIO and SCLK pins, in order to achieve improved serial transfer times with respect to the standard SPI library available in the Arduino platform. Specifically, all conventional SPI pins belong to the GPIO6 port of the MCU board; conversely, all the remaining pins indicated so far belong to different digital ports. Using these functions, we have verified the possibility of generating a SCLK having a frequency up to 120 MHz. However, clocking the SPI chip at this maximum rate could not guarantee a reliable communication, in view of the parasitic elements affecting our system. To mitigate this disturbance, SPI connections were made using shielded cables, grounding the shield at both ends. Adopting a working SCLK rate of 60 MHz by setting a clock divider equal to 2 in the custom SPI functions enabled a reliable communication between the MCU and DUC. The digital pin connections between them are summarized in Table 1.

| Function                     | Digital pins |
|------------------------------|--------------|
|                              | MCU | DUC |
| Power Control                | 2   | PWR_DWN |
| Master Reset                 | 3   | RESET |
| I/O Update                   | 5   | IO_UPDATE |
| Chip Select                  | 10  | CSB |
| Single/Quad-wire SPI Serial Clock | 40  | SCLK |
| Single/Quad-wire SPI SDIO    | 19  | SDIO_0 |
| Quad-wire SPI SDIO (second line) | 18  | SDIO_1 |
| Quad-wire SPI SDIO (third line) | 14  | SDIO_2 |
| Quad-wire SPI SDIO (fourth line) | 15  | SDIO_3 |

The last indispensable connections are related to the external timing system which can be any device capable of producing 10 +3.3 V TTL signals at rates ≥ 1 MHz. In our implementation, we used a National Instrument (NI) board (PCI-6251) to generate the interrupt trigger signals related to the commands described in Sect. 2.3, in addition to the pulses sent to the IO_UPDATE and P0-3 pins of the DUC, respectively required to activate the frequency configurations transferred via SPI, and to trigger the generation of the frequency ramps in frequency sweep mode. To meet the 3.3 V input voltage requirement of both the MCU and DUC boards, the 5 V output lines of the NI board were connected to a 5 V to 3.3 V voltage level translator (SN74LVC4245ADWR). As detailed in Section 2.3, we implemented two options to trigger the IO_UPDATE pin on the DUC: either directly from the NI after the SPI communication is completed or from the MCU if the “auto update” mode is engaged. To allow both options to work alternatively without hardware modifications, we use the digital logic OR gate.
circuit whose output goes to the DUC IO_UPDATE pin, while its inputs are connected to the I/O update pin of the MCU board (pin 5) and to the designated digital output line of the trigger generator.

6. Operation instructions

To operate the Arduino-based control system we developed an open-source software solution comprising two elements: the Arduino C++ sketch that constitutes the MCU program and the user interface implemented as a Python Jupyter notebook that runs on the PC and communicates with the MCU via USB. This notebook allows to compose and send the frequency configurations to be sequentially generated by the four-channel RF signal generator that we implemented as a demonstration of the MCU control system capabilities. The following procedure should be followed to operate the open-source software controlling the DUC:

1. Download the complete software package, comprising the Python 3 notebook and the C++ sketch to be loaded on the MCU board, either from the Mendeley repository or from the corresponding GitHub repository [26] for the latest version.

2. Download and install the Arduino integrated development environment (IDE) (Arduino Downloads).

3. Connect the MCU board to the PC via USB: this will power up the board.

4. Power up the DUC.

5. Open the C++ sketch using the Arduino IDE and, if required, modify the reference clock configuration of the DUC which is preset for an external 25 MHz clock source. In detail, after setting the frequency of the external reference clock (REF_CLK), set the global c.ClkMultiplier variable to false if clocking the DDS chip directly with a high frequency source. Otherwise, the internal phase-locked loop-based reference clock multiplier will be enabled; in this case, users must also specify the REF_CLK multiplier factor (c.PLLmul), that must be between 4 and 20. The internal clock rate of the DDS chip determines the maximum RF frequency that can be generated without incurring in spectrum distortions, which is 40% of this rate.

6. If desired, activate the sketch debug mode by setting g.debug to true and open the IDE serial monitor. When enabled, the MCU will output to this monitor several debugging messages that may help identifying issues in the supplied configurations or other problems.

7. If desired, activate the optional “auto update” mode (g.autoUpdate = true), discussed in Section 2.3.

8. Use the Arduino IDE to load the C++ sketch on the MCU board.

9. Open the Jupyter notebook user interface.

10. If required, adjust the value of the DUC system clock frequency (SYSCLK) within the “Setup Constants” cell at the top of the notebook.

11. Verify the number of the serial USB port used to communicate with the MCU board by selecting Tools > Port in the Arduino IDE menu.

12. In order to define the list of single-tone frequencies and/or linear frequency sweeps to be sequentially generated by the four DDS channels upon successive update interrupt events, edit the respective Python lists within the “Input to AD9959 DDS” cell. Specifically, whereas a simple floating-point value can be provided for the latter mode of operation, frequency sweeps are configured via Python dictionaries having as keys the start frequency, the chirp parameter (the slope of the frequency ramp, either positive or negative) and the sweep duration. Alternatively, a None keyword may be filled in whenever a particular channel should not be updated upon a specific step of the configuration sequence.
13. If desired, activate the notebook debug mode (debug = True) displaying the Unicode data strings encoded and sent to the board. Moreover, users may optionally disable the serial USB transfer (transfer = False) for validating the input to the MCU board without actually transferring the data strings.

14. Press the notebook’s “Run all” button to transfer the frequency configurations to the MCU board.

15. If the MCU debug mode is active, users may verify in the IDE serial monitor the frequency configurations received via USB and the programming progress of the DUC. Adopt long pulse periods (∼ ms) to allow the PC enough time to receive and display the MCU feedback messages.

16. Send a pulse train to the designated update interrupt pin of the MCU board for sequentially writing the transferred frequency configurations to the SPI buffers of the DUC. Once each setting is uploaded, the DUC waits for an I/O update pulse to reprogram and output the new set of RF signals. This pulse must be synchronized with the pulse train and delayed at least by the duration of the SPI transfer communication. It may originate either from another channel of the trigger source or from the MCU itself if the “auto update” mode of the C++ sketch has been enabled (item 7).

17. If linear frequency sweeps have been configured, following the I/O update pulse, these need to be externally triggered via transitions of the corresponding DUC profile pin logic state, i.e. from low to high for rising sweeps and vice versa, as detailed in the Linear Sweep Mode section of the AD9959 data sheet. Such logic state has to last for the entire duration of the frequency sweep (no-dwell mode disabled).

18. If required, users may toggle the designated external interrupt pins from low to high in order to trigger the execution of the commands implemented by the ISRs described in Sect. 2.3.

19. By repeating items 12-17, additional configuration lists can be defined, transferred to the MCU (appending them to the ones previously sent, if not yet executed) and activated on the DUC.

7. Validation and characterization

In order to validate the operation of the Arduino-based control system and of the four-channel RF signal generator that it powers, we first confirmed that the USB and SPI communication steps were error-free and we measured their data throughput rates. Then, we verified that the DUC was correctly programmed for all possible setting combinations and we characterized the RF output spectrum and verified that we could generate the desired combinations of RF single-tone signals and frequency sweeps.

We characterized the performance of the serial USB communication between the PC and MCU by evaluating the time required to transfer byte strings related to varying modes of operation of the four DDS channels, along with the time required to parse them and push incoming data into the designated memory buffers (Table 2). The data string byte size increases with the number of channels to be simultaneously activated, especially when operated in frequency sweep mode. We find that the relationship between the amount of transferred data and the incurred time is highly linear, as shown in Fig. 4, and from a linear fit we extract an USB transfer rate of 1.97 ± 0.01 MBytes⁻¹ and a data decoding rate of 4.29 ± 0.01 MBytes⁻¹, while the overheads are quite small, respectively 0.96(1) µs and 0.20(1) µs.

Next, we similarly assessed the achievable communication rate between the MCU and the DUC against different channel operation configurations, comparing the transfer times allowed by the standard single-wire Arduino SPI library with the ones obtainable with our custom single- or four-wire SPI implementation, which exploits direct port manipulation on the Teensy 4.1, a hardware optimization. A serial clock rate of 60 MHz was consistently adopted for the three SPI communication strategies, in order to establish a proper comparison.

These measures involved a subset of all possible channel programming combinations (i.e., an increasing number of single-tone signals or frequency ramps), and considered also the channel operation mode pre-programming needed when switching at least one of the four DDS channels from single-tone to frequency sweep mode and vice versa, requiring six additional bytes to be transferred in advance to the DUC. The measured transfer times are summarized in Table 3, and shown in Fig. 5 (channel mode pre-programming excluded). The standard single-wire SPI library provided a data rate of 3.38 ± 0.02 MBytes⁻¹, while our custom hardware-optimized
Figure 4: USB communication data rate between PC and MCU board, evaluated by linearly fitting the data reported in Table 2.

Table 2: PC-MCU USB communication properties against different channel configurations.

| Channels operation | Bytes | USB Transfer Time [µs] | Decoding Time [µs] |
|--------------------|-------|------------------------|-------------------|
| Single-tone Frequency Sweep |       |                        |                   |
| 1                  | 0     | 19                     | 8                 |
| 2                  | 0     | 29                     | 13                |
| 3                  | 0     | 39                     | 18                |
| 4                  | 0     | 49                     | 23                |
| 0                  | 1     | 51                     | 24                |
| 1                  | 1     | 61                     | 29                |
| 2                  | 1     | 71                     | 34                |
| 3                  | 1     | 81                     | 39                |
| 0                  | 2     | 93                     | 45                |
| 1                  | 2     | 103                    | 50                |
| 2                  | 2     | 113                    | 55                |
| 0                  | 3     | 135                    | 67                |
| 1                  | 3     | 145                    | 72                |
| 0                  | 4     | 177                    | 88                |

implementation reached 6.84 ± 0.07 MBytes⁻¹ in single-wire and 22.3 ± 0.3 MBytes⁻¹ in quad-wire modes. In all three cases the communication overhead and jitter was very small, respectively of 192(24) ns, 90(10) ns and 20(2) ns. These results highlight that our custom hardware-optimized SPI implementation delivers a considerable improvement of the DDS input data rate with respect to the standard SPI library, up to 6.6 times. As reported in Table 3, this in turn leads to an up to 6 times increase in the maximum allowed $ORR$ of the four DDS channels when using quad-wire custom SPI, with a minimum $ORR = 188$ kHz in the most data communication intensive case of four pre-programmed frequency sweeps, and a peak $ORR = 1.33$ MHz when only a single-tone setting is modified. This last result demonstrates that our four-channel RF signal generator reaches the desired performance specification and is competitive with other state-of-the-art solutions presented in Section 1.
Furthermore, we verified the correct activation of the frequency tuning words transferred via SPI, in order to validate the reliability of our custom single- and quad-wire solutions based on fast direct port manipulation.
Fig. 6 shows the spectrum of a 10 MHz RF signal generated by the DUC, as measured using the Fast Fourier Transform mathematical operation mode of a Rigol MSO5072 oscilloscope with a resolution bandwidth of 50 Hz. We found the measured spectrum to be consistent with the typical performance characteristics reported in the AD9959 data sheet [6]. The simultaneous refresh of two DDS channels is instead shown in Fig. 7, as captured with a Keysight Infinivision MSOX2024A oscilloscope: three subsequent update interrupt requests detected on the designated digital pin (magenta) trigger the SPI transfer of the data words sequentially stored in the FIFO buffers of the MCU. Following the SPI communication (yellow), an I/O update pulse (not shown) activates the new frequency values which are then generated by the respective DDS output channels after a fixed data latency of a few tens of SYSCLK periods. At the maximum SYSCLK rate of 500 MHz, these respectively correspond to $\sim 50 \text{ ns}$ and $\sim 80 \text{ ns}$ for DDS channels operated in single-tone and frequency sweep mode.

Figure 6: Typical RF spectrum of a single 10 MHz output of the DUC, measured using the Fast Fourier Transform mathematical operation mode of a Rigol MSO5072 oscilloscope.

8. Conclusion

The programmable Arduino-based four-channel RF signal generator that we have developed is an open-source and low cost solution that uses readily available components, like the 200 MHz AD9959/PCBZ [7] as the RF DDS source and the Teensy 4.1 [39] as the microcontroller unit. The total system cost is currently 641.79 €, resulting in a notably low cost per channel of 160.45 €, which makes it very competitive with respect to both commercial [18, 2, 34, 31, 27, 47, 48, 49, 50, 33] and lab-built RF generators [30, 29, 41, 38, 40, 21, 16, 3] that have similar specifications and applications. The internal software architecture has been designed to operate as a real-time state machine, allowing it to receive new commands and frequency settings from the PC via USB, store up to millions of them in its internal memory and to almost concurrently reprogram via SPI and activate the DDS outputs with sub-μs latency and jitter. We have validated the performance of our device, that surpasses all prior MCU-based solutions [18, 2], and demonstrated that it can generate single-tones or frequency sweeps in an externally or internally triggered arbitrarily programmed sequence. When using our custom quad-wire SPI implementation, that benefits from hardware optimizations, we have achieved high output change rates that depend only on the required amount of reconfiguration data, ranging from a minimum $\text{ORR} = 188 \text{ kHz}$ for four pre-programmed frequency sweeps and a peak $\text{ORR} = 1.33 \text{ MHz}$ when changing only a single-tone output. These rates were achieved while adopting a SCLK of 60 MHz and may be more than doubled if serial port I/O operations are conducted at the maximum speed of 200 MHz supported by the DUC. These characteristics make
Figure 7: Two-channel signal trace captured with a Keysight Infinivision MSOX2024A oscilloscope, displaying two sequences of three single-tone sinusoids of increasing frequency, activated in response to subsequent rising edges on the designated interrupt pin (UPDATE IRQ, shown in magenta) in “auto update” mode. The SCLK signal corresponding to the SPI communication between MCU and DUC is shown in yellow.

our RF signal generator suitable for a broad range of applications in biophysics, microscopy, quantum, atomic and molecular physics and industrial manufacturing, such as driving acousto-optical devices or controlling the state of processes or matter sensitive to this frequency domain.

By being open-source, state machine based and relying on standard interfaces for communication, the design of our RF generator is easily extensible and customizable for specific applications. Furthermore, the MCU architecture realizes a flexible and complete control system that is adaptable to many other devices. Likewise, the C++ software code presents a low skill barrier to be understood and modified using the Arduino IDE. Perspective improvements of our RF source would be the addition of amplitude and phase control which requires only additional software development, the enhancement of the SPI clock rate to further increase the ORR and the augmentation of command memory by 16 MByte by soldering two extra RAM chips. The functionality of the Jupyter notebook can be expanded to provide an iterative MCU communication method to supply configuration sequences whose length surpasses the MCU memory, to receive status information from the MCU and to provide IRQ functionality via USB, lowering the amount of required TTL timing lines. Finally, it should be possible to design a more general purpose MCU software code, lacking RF generator-specific functionality, that could ease the adaptation to another DUC type interfaced via SPI. Such future improvements and bug corrections will be made available in our GitHub repository [26].

CRediT author statement
Michele Sorelli: Software, Investigation, Validation, Visualization, Writing - Original Draft, Writing- Reviewing and Editing. Marco Marchetti: Software, Investigation, Validation, Writing - Original Draft. Pietro Ricci: Investigation, Validation, Visualization. Domenico Alfieri: Conceptualization, Funding acquisition, Project administration, Writing- Reviewing and Editing. Vladislav Gavryusev: Conceptualization, Methodology, Supervision, Software, Investigation, Visualization, Writing - Original Draft, Writing- Reviewing and Editing. Francesco Saverio Pavone: Funding acquisition, Project administration, Writing- Reviewing and Editing.
Declaration of Competing Interest
The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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