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Current Sharing Control of an Interleaved Three-Phase Series-Resonant Converter with Phase Shift Modulation

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Abstract: Recently, three-phase series-resonant converters (SRCs) have been proposed for high power applications. Three-phase SRCs can achieve zero-voltage-switching (ZVS) of the primary power switches and regulate the output voltage by pulse-frequency modulation. The interleaving technique is also a conventional method for DC-DC converters to achieve a high power level, reducing the output voltage ripples due to operating out of phase at the same frequency between the two converters. However, an interleaved three-phase SRC cannot easily synchronize switching instants between the two modules due to the component tolerances of circuits. In the proposed control method, phase shift modulation (PSM) is used to solve the output current imbalance caused by component tolerances. The power switches of the converter can also maintain synchronizing switching instants between the two modules. Therefore, the lower output voltage ripple can be achieved. A detailed analysis and design of this new control method for interleaved three-phase SRCs are described. Finally, prototype converters with a 2.4 kW total output were built and successfully tested to verify the feasibility of the current sharing modulation.

Keywords: current sharing; LLC-SRC; interleaved

1. Introduction

In the past decades, the resonant converter has been widely used in many applications such as laptop adapters, server power supply units and battery chargers. The reason for its wide use is its many advantages such as zero-voltage-switching (ZVS) at primary-side power switches, zero-current-switching at secondary-side rectifiers and a high conversion efficiency. However, the resonant converter is not suitable in high power and large output current applications because the secondary-side rectifiers do not use stored energy inductors such as an LLC resonant converter; thus, the secondary-side current is larger compared with other DC-DC converters. Therefore, many output capacitors are needed to parallel with the output side to satisfy the rated ripple voltage. The interleaved technique has been widely used for the high output power level. This technique can divide load current into each module and reduce output current ripple and voltage ripple. However, the conventional interleaving control for pulse-width modulation (PWM) cannot be directly applied to the resonant converters because they use pulse-frequency modulation (PFM) to regulate output voltage and the operational frequency of each module must be synchronized for the interleaved operations. However, when component tolerance occurs between the two modules, different gain characteristics will arise at a synchronized operational frequency. Thus, it will lose the advantage of interleaving control and will cause large output voltage ripples. Many studies have proposed an interleaving method of resonant converters. The influence of parameter mismatch of a resonant circuit and the improvement of current balancing are discussed in [1–11]. In [12], the output voltage of power-factor correction (PFC) was used to compensate for the parameter of the resonant circuit mismatch between the two modules. The PFC had to be placed in front of each
module of the resonant converters. In [13], the switch-controlled capacitor method was used to control output current sharing on each module. However, extra power switches had to be added, increasing the cost and volume of the converter. In [14], the current sharing method needed an additional power stage to regulate the output voltage but this method caused a lower conversion efficiency because the additional power stage caused other power losses. Three-phase series-resonant converters (SRCs) have been proposed for high power level applications. In comparison with other approaches, these SRCs can achieve better power loss distributions, excellent thermal distribution and much lower output voltage ripples. The three-phase SRC, three-phase LCC resonant converter and three-phase LLC resonant converter were proposed in [15–18]. These studies discussed the principle of operations about three-phase resonant converters. Similar to ordinary single-phase resonant converters, the output voltage of the three-phase SRC is regulated by a PFM control so that the interleaving technique is also difficult to use on three-phase SRCs.

In this paper, an interleaved structure of the three-phase SRC is proposed. In the proposed method, the three-phase SRC operates at a PFM control for regulated output voltage. Moreover, the influence of circuit parameter mismatch is compensated by a PSM control to achieve current balance. The proposed method does not require any auxiliary circuits and switching instants between modules can achieve synchronization. Section 2 describes the operation principle of an interleaved structure of a three-phase SRC with PSM. Section 3 provides an analysis and design for this proposed method. Section 4 demonstrates the experimental results of a 2.4 kW prototype. Section 5 concludes the paper.

2. Operation Principle of a Three-Phase Series-Resonant Converters (SRC)

The three-phase SRC schematic is shown in Figure 1. The circuit on the primary-side consists of three switch legs and three resonant tanks. The control signal is shown in Figure 2. Switches $S_1$–$S_6$ are controlled at a 0.5 duty ratio and three legs exhibit phase shifts at $0^\circ$, $120^\circ$ and $240^\circ$, respectively. The secondary-side transformers consist of three switch legs; switches $S_a$–$S_f$ are also controlled at a 0.5 duty ratio and three legs exhibit phase shifts at $120^\circ$ and $240^\circ$. The phase shift degree $\varphi$ between the primary-side and secondary-side is for output power control. Therefore, switches $S_1$ and $S_a$ represent phase shift degree $\varphi$, as do switches $S_3$ and $S_c$ as well as $S_5$ and $S_e$.

![Figure 1. Three-phase series-resonant converters (SRC) schematic.](image-url)
Figure 2. Power switch control signal.

Figure 3 shows the key waveforms of the three-phase SRC in one switching cycle. A complete half positive switching cycle comprises five states because the inductor current can be \( i_{Lrα} = i_{Lrβ} = i_{Lrγ} \) with phase shifts of 120° and 240°, which can only use one phase to analyze simplified calculations. The basic idea about the three-phase SRC has been discussed in many studies [19,20]. The resonant frequency \( f_r \) and the power transfer of a three-phase SRC has been expressed as:

\[
f_r = \frac{1}{2\pi \sqrt{L_r \times C_r}}, \tag{1}
\]

\[
P_o = 3 \cdot P_{\text{phase}} = \frac{n V_o V_{\text{in}} (\varphi - 30°)}{360 f_{\text{sw}} L_r}. \tag{2}
\]

Figure 3. Primary and secondary-side phase voltage and inductor currents of the one phase.

Equation (2) can explain the elements that can use the phase shift degree \( \varphi \) and switching frequency \( f_{\text{sw}} \) to regulate output power \( P_o \). Figure 4 depicts the relationship
between the phase shift degree $\phi$ and output power $P_o$. The phase shift degree $\phi$ must be limited between $30^\circ$ and $60^\circ$ to transform the power into the output load side. In addition, the specifications in Figure 5 are used except for frequency $f_{sw}$, which is defined as 125 kHz. To explain the relationship among the voltage gain, phase shift degree $\phi$ and switching frequency $f_{sw}$, the voltage gain is defined as $nV_o/V_{in}$ and Equation (3) can be derived from Equation (2) where $n$ is the turn ratio of the primary-side to the secondary-side of the transformers, assuming a voltage gain $nV_o/V_{in} = 0.56$, $V_{in} = 400$ VDC, $V_o = 48$ VDC and $I_o = 25$ A. Therefore, $R_L$ is equal to 1.92 $\Omega$, the resonant inductor $L_r$ is 18 $\mu$H, the resonant capacitor $C_r$ is 141 nF and the switching frequency $f_{sw}$ is limited between 100 and 200 kHz to normalize the frequency $f_{sw}$. The gain curve diagram is shown in Figure 5. The frequency $f_{sw}$ is normalized as $f_n$ by dividing the resonant frequency $f_r$, which is 100 kHz. As the color changes from blue to yellow, this indicates that the gain is from low to high. The output voltage can be regulated by the phase shift degree $\phi$ and normalized frequency $f_n$. Furthermore, when increasing the phase shift degree $\phi$ or decreasing the normalized frequency $f_n$, the voltage gain obviously rises.

$$Gain = \frac{nV_o}{V_{in}} = \frac{n^2 R_L(\phi - 30^\circ)}{360 f_{sw} L_r}$$

where $R_L = V_o/I_o$ and $n = N_p/N_s$.

![Figure 4. Transmission power curve.](image)

**Figure 4.** Transmission power curve.

![Figure 5. Gain curve.](image)

**Figure 5.** Gain curve.

3. Principle of an Interleaved Three-Phase SRC with PSM Current Sharing Control

3.1. Design of Phase Lagging Degree and Phase Shift Degree

The interleaved three-phase SRC schematic is shown in Figure 6. The SRC consists of two modules of a three-phase SRC, which are divided into modules A and B. $C_r$ is
the resonant capacitor. \( L_{rA} \) is the resonant inductor of module A and \( L_{rB} \) is the resonant inductor of module B. In ideal conditions, the \( L_{rA} \) and \( L_{rB} \) have equivalent values. The key waveforms of the interleaved three-phase SRC are shown in Figure 7. The phase shift degree \( \phi_A \) is module A between the primary- and secondary-sides. The phase shift degree \( \phi_B \) is module B between the primary- and secondary-sides. The phase shift degrees \( \phi_A \) and \( \phi_B \) are separately independent to control modules A and B for output power, respectively. Moreover, to achieve a minimum total output ripple current \( i_{o,pp} \), module B control signals will be lagging the \( \phi_{AB} \) degree of module A. The phase lagging degree \( \phi_{AB} \) can be calculated as

\[
i_{o,pp}(\phi_{AB}) = \begin{cases} \frac{\pi I_o}{3} \left[ 2 \cos \left( \frac{\phi_{AB}}{2} \right) \sin \left( \frac{\phi_{AB} + 60^\circ}{2} \right) - \sqrt{3} \right] & \text{for } 0^\circ \leq \phi_{AB} \leq 30^\circ \\ \frac{\pi I_o}{3} \left[ 2 \sin \left( \frac{\phi_{AB}}{2} + 60^\circ \right) + \sin \left( \phi_{AB} - 120^\circ \right) - \sqrt{3} \right] & \text{for } 30^\circ \leq \phi_{AB} \leq 60^\circ \end{cases}
\]

(4)

\[
i_{o,ppmax} = i_{o,pp}(0^\circ) = i_{o,pp}(60^\circ) = \frac{\pi I_o}{3} \left[ 2 \sin(60^\circ) - \sqrt{3} \right].
\]

(5)

Equation (4) is drawn in Figure 8, which is normalized by \( i_{o,ppmax} \). When the phase lagging \( \phi_{AB} \) is 30°, the converter will have a minimum total output ripple current \( i_{o,pp} \). Therefore, module B control signals will be set to lagging module A by 30°.
Figure 7. Operating principle of an interleaved three-phase series-resonant converters (SRC).

Figure 8. Current ripple comparison of lagging degree $\phi_{AB}$. 
3.2. Current Sharing Control of PSM

The digital control block diagram of the interleaved three-phase SRC is shown in Figure 9. To achieve output voltage stabilization and current sharing under all load ranges, the control method combines a PFM control to regulate the output voltage and a PSM control to achieve current sharing.

![Digital control block diagram](image)

**Figure 9.** Digital control block diagram. \(i_{oA}\): output current of ModuleA; \(i_{oB}\): output current of ModuleB; \(H_o(s)\); \(H_f(s)\); ADC: analog to digital converter; \(k\): sampled digital control cycle; \(V_d[k]\): digital value of \(V_d\); \(i_{oA}[k]\): digital value of \(i_{oA}\); \(i_{oB}[k]\): digital value of \(i_{oB}\); \(I_{ref}\): reference current; PI: proportional-integral controller; VCO: voltage-control oscillator; \(S_{A1}~S_{A6}\), \(S_{A3}~S_{A1}\), \(S_{B1}~S_{B6}\), \(S_{B6}~S_{B6}\): MOSFET signals.

\(H_o(s)\) and \(H_f(s)\) contain a voltage divider resistance and RC filter transfer circuit signals to a DC value under 3.3 V for ADC inputs. The ADC sample transfers analogue values to digital values such as \(V_d[k]\), \(I_{oA}[k]\) and \(I_{oB}[k]\). The error between the reference voltage \(V_{ref}\) and the sampled \(V_d[k]\) is entered into a compensator. The frequency is then controlled through a voltage-control oscillator as a PFM control. The error between reference current \(I_{ref}\), which is half of the total output current, and either \(I_{oA}[k]\) or \(I_{oB}[k]\) is entered into a compensator to control the phase shift angle \(\Delta \phi\) and as a PSM control. The initial phase angle \(\varphi_i\) is calculated through Equation (6) with \(I_{ref}\) and \(f_{sw}\). Finally, 12 enhanced pulse-width modulator (ePWM) modules with desired periods and phases are used to generate the 24 signals to control the circuit.

The program is implemented with a digital signal processor (DSP), namely, TMS320F28379. The main control flow chart is shown in Figure 10. The cycled steps of the proposed modulation are shown as follows.

- To achieve the above functions, three ADC inputs are needed to convert the sampled signals into digital values after interruption.
- The same operating frequency of modules A and B are determined by the output voltage feedback with a proportional-integral (PI) controller.
- For the \(\varphi_i\) calculation and average current sharing control, a reference current \(I_{ref}\) set as half of the total output current is needed.
- \(\varphi_i\) is calculated through Equation (6), which is derived from Equation (2) with \(I_{ref}\) and \(f_{sw}\).

\[
\varphi_i = 30^\circ + \frac{360 f_{sw} L_r I_{ref}}{n V_{in}}. \quad (6)
\]
• $I_{oA}$ and $I_{oB}$ are negative feedbacks to compare $I_{ref}$ with integral controllers. When output currents are balanced, $\Delta \phi$ and $-\Delta \phi$ are generated by the I-Loop compensation. Therefore, $\phi_A$ is equal to $\phi_i + \Delta \phi$; $\phi_B$ is equal to $\phi_i - \Delta \phi$.

![Figure 10](image.png)

**Figure 10.** Main control flow chart. (A/D: analog to digital; $I_{oA[k]}$: digital value of $i_{oA}$; $I_{oB[k]}$: digital value of $i_{oB}$; $I_{ref}$: reference current; PI: proportional-integral controller; $f_{sw}$: switching frequency; $L_r$: resonant inductor; $n$: turn ratio of the primary-side to the secondary-side of the transformers; $V_{in}$: input voltage; $\phi_A$: phase shift degree of ModuleA; $\phi_B$: phase shift degree of ModuleB).

### 3.3. Closed Loop Design

As the state-space averaging method can maintain an accuracy under $1/5$ of $f_{sw}$ [21], the simplified small-signal model of the proposed converter as shown in Figure 11 is used for the closed loop design [22]. The expressions of the small-signal value of the output current $i_o$ can be derived by taking the partial derivative of Equation (2) with respect to $f_{sw}$ and $\phi$ as follows.

\[
\tilde{i}_o = \frac{nV_{in}(\phi - 30^\circ)}{360f_{sw}L_r} \times f_{sw} + \frac{nV_{in}}{360f_{sw}L_r} \times \tilde{\phi}.
\]  

(7)

\[
\tilde{i}_o = \frac{nV_{in}}{360f_{sw}L_r}.
\]  

(8)

\[
\tilde{v}_o = \frac{nV_{in}(\phi - 30^\circ)}{360f_{sw}^2L_r} \times \frac{R_L}{1 + sR_LC_o}.
\]  

(9)

![Figure 11](image.png)

**Figure 11.** Simplified small-signal model of the proposed converter. ($C_o$: output capacitor; $R_L$: output load resistant; $i_o$: small-signal value of output current; $v_o$: small-signal value of output voltage).

As the digital sample and delay cause a phase margin drop, the crossover frequency needs to be designed smaller than analog. The PI controller is designed with a crossover frequency of 5 kHz and a phase margin of 96° for output voltage stabilization and a fast
load transient. The integral controllers are designed with a crossover frequency of 500 Hz and a phase margin of 91° for a current sharing feedback loop. The Bode plots of the compensated loop gain for both functions are shown in Figure 12.

![Bode Diagram](image)

**Figure 12.** Bode plots of the compensated loop gain for both functions.

### 3.4. Simulation Results of PSM Control

The combination of the single 1.2 kW module forming the interleaved three-phase SRC was designed and simulated for $V_{in} = 400$ V$_{DC}$, $V_o = 48$ V$_{DC}$ and $P_o = 2.4$ kW and the component values and specifications are listed in Table 1. In general, 130 kHz was the maximum limit of the switching frequency $f_{sw}$ for the power density and the high conversion efficiency. The phase shift degree $\varphi_A$ and $\varphi_B$ were limited to a maximum of 40° and the lagging degree $\varphi_{AB}$ was set at 30° for the minimum output ripple voltage. Equation (3) shows that the voltage gain was 0.56. The equivalent output resistances of the single module $R_L$ were 7.38 Ω at 25% load condition, 3.84 Ω at the 50% load condition and 1.92 Ω at the 100% load condition. Therefore, the resonant inductor followed Equation (1) and it could be obtained at approximately 18 µH.

| Parameter                        | Values                  |
|----------------------------------|-------------------------|
| Input voltage                    | 400 V$_{DC}$            |
| Output voltage                   | 48 V$_{DC}$             |
| Total output current (single module) | 50 A (25 A)           |
| Total output power (single module) | 2.4 kW (1.2 kW)        |
| Limit of switching frequency $f_{sw}$ | 120–130 kHz       |
| Limit of phase shift degree $\varphi_A$ and $\varphi_B$ | 30–40°                  |
| Lagging degree $\varphi_{AB}$    | 30°                     |
| Resonant inductors ($L_{rA}$, $L_{rB}$) | 18 µH ± 10%            |
| Voltage gain $nV_o/V_{in}$       | 0.56                    |
| Turn ratio of transformer $n = N_p/N_s$ | 14/3                    |

Figure 13 shows the simulation results of the ideal interleaved three-phase SRC. The resonant inductors $L_{rA}$ and $L_{rB}$ were equal to 18 µH. When the output load from 25%...
increased to the full load, modules A and B showed that switching frequency $f_{sw}$ changed from 130 kHz to 121 kHz and the phase shift degree $\varphi_A$ and $\varphi_B$ changed from 32.8° to approximately 40°. By contrast, the module cause of the imbalanced condition was the tolerance in the resonant inductor values of the converter. Generally, a 10% change in the magnetic component values could be expected, causing an imbalanced output current between modules A and B. Figures 14–16 show the simulation results of the imbalanced conditions when $L_{rA}$ was 20 $\mu$H and $L_{rB}$ was 16 $\mu$H. Figure 12 shows 25% output power load conditions. To maintain a voltage gain at 0.56 for regulated output voltage and interleaved operation, the switching frequency $f_{sw}$ of modules A and B operated at 130 kHz. The phase shift degree $\varphi_A$ of module A and the phase shift degree $\varphi_B$ of module B were 33.1° and 32.5°, respectively. In Figure 15, when the output load condition was at 50%, the switching frequency $f_{sw}$ operated at 127 kHz, the phase shift degree $\varphi_A$ of module A operated at 36.1° and the phase shift degree $\varphi_B$ operated at 34.9°. Figure 14 shows the output power at full load. The switching frequency $f_{sw}$ was at 121 kHz and the phase shift degree $\varphi_A$ and $\varphi_B$ operated at 41.7° and 39.3°, respectively.

Figure 13. Simulation results of the ideal interleaved three-phase SRC ($L_{rA} = L_{rB} = 18$ $\mu$H): (a) at a 25% output load ($V_o = 48$ V$_{DC}$, $I_o = 6.5$ A, $R_L = 7.38$ $\Omega$), (b) at a 50% output load ($V_o = 48$ V$_{DC}$, $I_o = 12.5$ A, $R_L = 3.84$ $\Omega$), (c) at 100% output load ($V_o = 48$ V$_{DC}$, $I_o = 25$ A, $R_L = 1.92$ $\Omega$).
Figure 14. Simulation results of switching frequency versus phase shift degree at a 25% output load: (a) module A with $L_{rA} = 20 \, \mu\text{H}$, (b) module B with $L_{rB} = 16 \, \mu\text{H}$.

Figure 15. Simulation results of switching frequency versus phase shift degree at a 50% output load: (a) module A with $L_{rA} = 20 \, \mu\text{H}$, (b) module B with $L_{rB} = 16 \, \mu\text{H}$.

Figure 16. Simulation results of switching frequency versus phase shift degree at a 100% output load: (a) module A with $L_{rA} = 20 \, \mu\text{H}$, (b) module B with $L_{rB} = 16 \, \mu\text{H}$.

Figure 17 shows the simulation results of the output current and output voltage ripple when the resonant inductors $L_{rA}$ and $L_{rB}$ were 20 and 16 $\mu\text{H}$ at full load conditions,
respectively. In Figure 17a, the gate signal $V_{gsBa}$ lagged $V_{gsAa}$ by approximately 30° so that the output ripple voltage $V_{oac}$ could be decreased. By contrast, because the PSM control was disabled, the phase shift degree $\varphi_A$ and the phase shift degree $\varphi_B$ were the same at 40.5° so the output current $I_{oA}$ and $I_{oB}$ were imbalanced. In Figure 17b, the PSM control was used for the output current balance. The switching frequency was approximately 121.2 kHz, the phase shift degree $\varphi_A$ was 41.8° and $\varphi_B$ was 39.2°. These simulation results corresponded with those in Figure 16.

4. Experimental Results

To verify the theoretical analysis, a 2.4 kW prototype was designed and built as shown in Figure 18. Its key parameters are shown in Table 1. The component values are listed in Table 2. The PQ-4040 core was used for isolation transformers $T_1$, $T_2$, $T_3$, $T_4$, $T_5$ and $T_6$, the resonant inductor core was CH330060 and the power switches were IPL60R199CP and IPB020N08N5.
The switching frequency was 130 kHz. Compared with Figure 13a, Figure 20 was identical to the simulation results.

Figure 19 shows the waveforms of the first bridge primary and secondary phase voltages and inductor currents at a 25% load. The power switch was turned on after the \( V_{ds} \) of the power switch dropped to a zero level, achieving ZVS.

Figure 20 shows the waveforms of ZVS.

Figure 19 shows the waveforms measured by the primary- and secondary-side power switches at a 25% load. The phase shift degree \( \phi_A \) was approximately 33° and the switching frequency was 130 kHz. Compared with Figure 13a, Figure 20 was identical to the simulation results.

Table 2. Summary of components.

| Component | Part Number |
|-----------|-------------|
| MOSFETs (primary-side) | IPL60R199CP |
| MOSFETs (secondary-side) | IPB020N08N5 |
| Transformer core (\( T_1 - T_6 \)) | PQ-4040 |
| Resonant inductor core (\( L_{rA}, L_{rB} \)) | CH330060 |
| DSP controller | TMS320F28379 |

Figure 18. 2.4 kW experimental setup.

Table 2. Summary of components.
Figure 21. Waveforms of phase shift of the primary- and secondary-sides.

Figure 20. Waveforms at a single module. The resonant inductor $L_{rA}$ was equal to 18 $\mu$H and had different output load conditions (6.25, 12.5, 18.75 and 25 A). The measured waveforms were the waveforms of $V_{gs2}$ and $V_{ds2}$ of the primary-side low-bridge switch $S_2$, the resonant inductor current $i_{LrA}$ and the $V_{gsb}$ of the secondary-side switch $S_b$.

Figure 21. Typical waveforms at (a) 25%, (b) 50%, (c) 75% and (d) 100% loads.

The values of resonant inductors $L_{rA}$ and $L_{rB}$ were set at different values to test imbalanced current conditions. $L_{rA}$ was designed as 20 $\mu$H and $L_{rB}$ was 16 $\mu$H. Figure 22 shows the output current waveforms of the two modules in parallel at a 25% load conduction. Figure 22a,b show without and with a current sharing control. When the function of the current sharing control was disabled, the current was imbalanced due to component mismatch. With a PSM control, the imbalanced current was improved. Both ripple current frequencies of $i_{rA}$ and $i_{rB}$ were six times larger than the switching frequency. Furthermore, with phase lagging $\varphi_{rAB}$ at 30°, the ripple current frequency of $i_r$ was twelve times larger than the switching frequency, achieving a minimum output ripple current $i_{o,pp}$. 
The trend of switching frequency and phase shift changing was the same as Figure 13 in that when the load was increased, the switching frequency \( f_{sw} \) decreased and the phase shift degree \( \varphi_A \) increased.

Figure 23 shows the current sharing waveforms of the two modules with the current sharing phase shift control at 50\%, 75\% and 100\% load conditions. The output currents were balanced at different loads. Table 3 shows the output current error of the two modules and the current sharing error ratio was under 3\%.

**Figure 23.** Output current waveforms of the two modules in parallel at (a) 50\%, (b) 75\% and (c) 100\% load.

| Load | \( I_{oA} \) (A) | \( I_{oB} \) (A) | \( I_o \) (A) | \( I_{Error} \) (%) |
|------|------------------|-----------------|---------------|-------------------|
| 25\% | 6.5              | 6.8             | 13.3          | 2.3               |
| 50\% | 12.4             | 12.4            | 24.4          | 1.6               |
| 75\% | 17.7             | 18.1            | 35.8          | 1.1               |
| 100\%| 24.2             | 24.3            | 48.5          | 0.2               |

\[ I_{Error} = \left| \frac{I_{oA} - I_{oB}}{I_o} \right| \]

Figure 24 shows the phase shift waveforms of modules A and B at different load conditions. The phase lagging was approximately 30°. When the load was increased, the
phase shift degree $\phi_A$ and $\phi_B$ increased and the switching frequency decreased to regulate the output voltage. In addition, the phase shift degree $\phi_A$ and $\phi_B$ operated in different degrees to balance the output current between modules A and B. The measurement results were identical to the simulation results in Figures 14–16.

![Phase shift waveforms of modules A and B at different loads](image)

**Figure 24.** Phase shift waveforms of modules A and B at (a) 25%, (b) 50%, (c) 75% and (d) 100% loads.

Figure 25 shows the output ripple voltage waveform at a 100% load and with the interleaved two modules, which achieved a minimum output ripple current $i_{o_pp}$ to reduce the volume of the output capacitor. In addition, Figure 26 shows the result of the dynamic load from 10 A to 50 A. The overshoot and undershoot of the output voltage were about 4 V. The efficiency curve of the converter was measured with a power meter and is shown in Figure 27. The highest efficiency could reach 94.5%.

![Output ripple voltage waveform at a 100% load](image)

**Figure 25.** Output ripple voltage waveform at a 100% load.
Figure 26. Dynamic load waveform from 10 A to 50 A.

Figure 27. Efficiency of an interleaved three-phase SRC with phase shift modulation.

5. Conclusions

To solve the current imbalance between two modules, this paper presented the PSM control for an interleaved three-phase SRC. The component mismatch of the resonant inductor was made to verify the validity of the proposed method. Using the proposed method achieved a current sharing function and synchronized switching frequencies. Thus, the proposed method is important in decreasing the output ripple voltage and equally distributing conduction losses between modules A and B. The experimental results on a 2.4 kW prototype were recorded to verify the theoretical analysis. The results showed that the PSM control could achieve the current sharing. The phase lagging of 30° could achieve the minimized output ripple voltage.

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