Current transport modeling and experimental study of THz room temperature ballistic deflection transistors

Vikas Kaushal†, Martin Margala‡, Qiaoyan Yu*, Paul Ampadu*, Gregg Guarino*, Roman Sobolewski*

†‡ Department of Electrical and Computer Engineering
*University of Massachusetts Lowell, MA, USA 01854
*University of Rochester, NY, USA 14627
vikas_kaushal@student.uml.edu

Abstract. In this paper, two different theoretical models, Comsol Multiphysics™ (a Finite Element Analysis tool), and a field solver Atlas/Blaze from Silvaco, are compared qualitatively to study the effect of the deflector position, its size and electric field on the charge transport and its distribution along the channel, resulting in current outputs and leakages in ballistic deflection transistors (BDT). Silvaco simulations and experimental results were then used to study the lateral charge transport as a result of variation in electric field distribution, which controls the charge current along the channel in BDT. The electric field dependence of gain is also studied with experimental and theoretical results.

1. Introduction
The future electronics depends significantly on the scalable solid state transistors with much higher speed than the III-IV FETs and lower energy dissipation than current CMOS transistors. The extensive scaling leads to increased leakages through gates, which motivates researchers to explore novel devices and structures. In the same context, ballistic devices have been proposed by many groups [1,2]. These devices have emerged as a prominent and practical device for high speed and high current handling applications. The current transport in these ballistic devices shows a unique behavior as all the charge is moving in a single 2DEG plane. The lateral charge density depends on the electric field distribution along the 2DEG plane, which leads to the variation in currents at various device terminals. Since, the device size is being scaled down aggressively and the scattering is only exhibit at the boundaries, the charge distribution also depends on its geometry and dimensions significantly.

In this paper, section one gives the overview of BDT, which is followed by the second section, which explains the theoretical simulations of current transport in BDT with two different modeling tools, Comsol Multiphysics™, an FEA software package and commercially available tool Atlas/Blaze from Silvaco. Third section explains the qualitative agreement between simulations and D.C. experimental results to describe the electric field distribution dependence of transconductance of BDT.

2. BDT operation and Structure
BDT, which is a 1-THz transistor, is proposed by our group in [3]. BDT is a low noise and low loss device which is based upon an electron steering and a ballistic deflection effect. The material system
chosen, provides a large mean free path and high mobility to support ballistic charge transport at room temperature. This transistor is unique in that no doping junction or barrier structure is employed. The theoretical value of $f_t$ obtained at room temperature is 1.02 THz for a specific geometry and dimension which can vary with dimension. Typical cross-section, SEM image and schematic of BDT are shown in Figure 1 (a), (b) and (c) respectively.

3. Modeling and Theoretical Results

Two different theoretical models are studied and compared qualitatively for the effect of deflector and electric field ($E$) on the charge transport along the planar channel, resulting in outputs and leakages. Two different selected simulations are Comsol Multiphysics™, a Finite Element Analysis (FEA) software package and commercially available tool Atlas/Blaze from Silvaco. For Comsol simulations, BDT was simulated using FEA, based on a simple conductive media model. The conductivity of the 2DEG was approximated based on a carrier density of $10^{12}$ cm$^{-2}$, and the InGaAs bulk electron mobility of 12,000 cm$^2$/V.s, giving a value of 0.00192 S. The effect of applied gate voltage was modeled as depletion of the channel on the side of the negative electrode. The depletion was assumed to advance laterally across the channel, as a linear function of a gate voltage, until complete pinch-off occurs at the max gate voltage.

The function of the triangular deflector in this FEA model was particularly of interest. Although it does not act as a deflector in the ballistic electron sense, it redirects the flow of current. Its shape and position influence the transport of output current between the top, left, and right electrodes. Top drain leakage ($I_{TD}$) has been a major source of leakage in the BDT [4]. Figure 2(b) shows $I_{TD}$ variation with applied differential gate voltage at different deflector positions ($k$). Deflector size ($h$) selected for this specific case is 75nm. “$k$” increases upwards as shown in Figure 1. This study shows that when deflector is placed at $k=230nm$, leakage rises and when deflector touches the top drain port, leakage
becomes negligible. Ideally, no current should pass through top drain but because of the fact that the electric field distribution is uneven and electron pull by top drain due to high electric field is much higher in the channel, electron current towards top drain counts for the leakage. It is observed that placing deflector at approximately 25% lower than the exact centre of the device reduces leakage significantly, which indicates the high deflector-electron interactions essentially creating a barrier for electron to move towards top drain [5].

Current distribution is also noticed with `h' and it can be seen from Table 1 that for \( h = 50 \text{nm} \), output obtained is maximum and leakage also reduced significantly. Table 2 shows a current distribution variation at different terminals with `k'. It is noticed that output rises with `k', and at the same time leakage also rises; leakage minimizes when deflector touches the top port. Fabrication with configuration of \( k = 325 \text{nm} \) is avoided because of the removal of the whole top channel in that case.

This effect of `k' is also studied with Silvaco simulations. The structure used for the simulations is the stacked lattice matched layers of InGaAs and InAlAs on InP substrate (Figure 1a). The Si-planar doping layer with a doping density of \( 2 \times 10^{12} \text{cm}^{-2} \) is used. Hall measurements of this structure yielded an electron sheet density of \( n_s = 9.832 \times 10^{11} \text{cm}^{-2} \) and electron mobility of \( \mu_n = 1.206 \times 10^4 \text{cm}^2/\text{Vs} \) at 300K. Physical models chosen are Boltzmann, thus a statistical approach. Mobility models chosen are \( \text{conmob} \) and \( \text{fldmob} \) where \( \text{conmob} \) uses simple power law temperature dependence and \( \text{fldmob} \) is used to model velocity saturation effects. Shockley-Read-Hall model is used because it uses fixed minority carrier lifetimes for numerical solutions. Fig. 2(b) shows the effects of applied gate voltage on \( I_{TD} \) at applied gate voltage. This study also showed that `k' is a significant in BDT and Silvaco simulations in qualitative agreement with Comsol modeling. Silvaco simulations confirm that for \( k = 230 \text{nm} \), leakage becomes maximum and becomes zero when deflector touches the top drain port (at \( k = 325 \text{nm} \)).

4. Theoretical and Experimental Results

Silvaco simulations are also used to study the current transport and distribution as a result of variation in electric field \( (E) \), which controls the flow of charge along the planar 2DEG channel. For this purpose, 2D Poisson equation is solved analytically for the entire high-field region. Electrostatic potentials between electrodes are differentiated to get \( E \). Figure 3(a) shows the theoretical variation of the \( E \) along the channel with drain voltage for a left gate bias of 0.3V. \( E \) increases along the channel, and reaches a maximum at a point between the gate and the drain as most of the applied drain potential appears across this narrow region of small conductance. The \( E \) is higher for higher values of \( V_{GS} \).

Figure 3(b), which is a D.C. experimental result, confirms it, which shows that the transconductance increases with \( V_{DS} \). It is also seen that the peak transconductance shifts to higher \( V_{GS} \) with increased \( V_{DS} \). This is easily understood since the voltage drop between the gate and the drains is much greater in the high-drain bias case, resulting in a high \( E \). Due to variation in the transport of the charges at different terminals, \( I_{TP} \) and \( I_{RD} \) appear as outputs and \( I_{TD} \) as leakage. BDTs with different dimensions are fabricated. Qualitatively, the results obtained are in agreement with the Silvaco simulations which confirm that \( E \) near drains is higher which leads to high conductivity inside the channel at these areas. Electron velocity \( (V_e) \) also plays a major role for the device performance. The \( V_e \) is significantly greater in the channel under high \( V_{DS} \) due to greater confinement of electrons within the 2D system. When the applied \( V_{DS} \) is low, the transistor is in linear operation regime, and the electron velocity is uniform. Electric field increases sharply due to velocity saturation. At this point, the average electron energy increases dramatically, leading to significant velocity overshoot.
Figure 3: (a) Variation of the electric field along the channel for different drain voltages. Each drain is kept same for single event. (b) IV characteristic of the left drain port as a function of differential gate voltage (in reference to the left gate), an increase in drain voltage increases the transconductance, near linearly for voltage beyond 1V.

Table 3: Comparison of theoretical and experimental results for output and leakage with 75nm deflector height.

| h=75(nm) | I_{LD}(A) | I_{RD}(A) | I_{TD}(A) |
|----------|-----------|-----------|-----------|
| Simulation | 1.9308E-08 | 1.9474E-08 | 2.4674E-08 |
| Experiments | 2.565E-06 | 2.4965E-06 | 9.2374E-07 |

Table 3 gives the current transport and distribution comparison between simulated results and experimental data. It is observed that the experimental results give good device performance but the leakage was high. These results can be used to define the electric field contour inside the device and thus the control on electric field distribution can be achieved for optimum device performance.

5. Conclusions

In this paper, two different modeling tools are used to study the current transport and its distribution inside the channel for various deflector positions and sizes. Geometry is optimized for reduced leakage and better device outputs. It is confirmed that placing deflector at k=185nm, which is 25% below the exact centre of the device, reduces leakage significantly. It is also observed that for the deflector size of 50nm, the outputs are at maximum and the leakage reduces significantly. Fabricated devices were tested for the electric field distribution comparison with Silvaco simulations. For each drain voltage of 2V, maximum electric field of the order of 352.675KV/cm is obtained, which indicates that with higher drain voltage, transconductance will increase. Output and leakage currents are compared in order to achieve the geometry optimization for future fabrications and experiments.

References
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