Implementation of True Random Number Generator based on Double-Scroll Attractor circuit with GST memristor emulator

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Abstract—The cryptographic security provided by various techniques of random number generator (RNG) construction is one of the developing researches areas today. Among various types of RNG, the true random bit generator (TRBG) can be considered as the most unpredictable and most secured because its randomness seed is generated from chaotic sources. This paper proposes a design of TRBG model based on double-scroll attractors circuits with GST memristor. After implementation and simulation of the chaotic circuit with GST memristor emulator, the chaotic behavior of the output voltage and inductor current were received. Moreover, their dependence on the input voltage revealed the close to double-scroll form. The randomness generated from the proposed circuit was tested by receiving Fast Fourier Transform (FFT) and Lyapunov exponents of the output voltage.

I. INTRODUCTION

THE Random Number Generator (RNG) is widely used subject in various technology spheres. Thus, it is one of the dominant tools in cryptographic security today and its importance gradually rises with the technological development. There are many different techniques to create RNGs based on their classification: true random number generator (TRNG), pseudo random number generator and hybrid number generator. As TRNG is generated from natural/non-deterministic and chaotic sources, its randomness seed can be considered as the most unpredictable and consequently most secured. One example of the non-deterministic source is the chaotic oscillator which generates double-scroll attractors [1], [2]. This chaotic oscillator is modeled by analogy of the circuit implemented by Chua in 1971, which is essentially oscillator with non-linear resistor for executing chaotic behavior inside [3]. Moreover, relatively new and full of potential memristive technology allows to replace non-linear resistor in the proposed chaotic circuit for TRNG because of its non-linear and distinctive electrical properties. Memristors are differed from each other and classified according to the technology of creation, materials and related features. In this paper we propose a design of TRNG circuit that is based on Phase- Change Memory device (Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>), which is known as GST memristor [4], [5], [6], [7]. For the present time there is no existing GST memristor model, that is why its characteristical equations and parameters should be investigated in order to create its emulator circuit. In order to reveal the effect of the addition of GST memristor emulator circuit, the theoretically and practically confirmed Chua’s circuit with non-linear resistor implemented as two diodes with different polarities and two pairs of resistors with different values should be also constructed [8], simulated and compared with studying circuit.

This paper is organized as follows. We first investigate the properties of GST memristor and construct its emulator circuit in LTSpice software. Then, mathematical calculations and analysis for GST memristor and other devices parameters are performed. After that, we analyze and compare the original Chua circuit with two diodes and the modified circuit with GST memristor model in order to receive double-scroll attractors and reveal the most efficient one.

II. GST MEMRISTOR EMULATOR CIRCUIT

The chaotic circuit constructed in this paper is based on the fundamental Chua’s circuit with non-linear resistor implementation. Initially, as it was proposed by Kennedy [8], the original circuit with non-linear resistor, which is implemented with two diodes with different polarities and two pairs of resistors of 3.3 kΩ and 47 kΩ values, and negative resistor, which consists of operational amplifier and three resistors of 290 Ω, 290 Ω and 1.2 kΩ values, is constructed. The designed original circuit is demonstrated on the Fig. 1.

![Chua circuit with two diodes and resistors implementing non-linear resistor behavior](image)

In order to implement new modified Chua’s circuit with GST memristor, the GST memristor’s emulator circuit with
3 different levels resistors and two capacitors was constructed because there is no already designed model of GST memristor. As it was suggested by Li et al. [9], the emulator circuit consisting of contact resistor of the electrodes \( R_s \) serially connected to parallel connection of pure resistor and capacitor of GST \( (R_p, C_p) \). In order to better represent equivalent behavior of the GST memristor two main sources of defect in crystalline grain and at grain boundaries should be considered. That is why, \( R_p \) and \( C_p \) are separated to \( R_g \) and \( C_g \) and \( R_{gb} \) and \( C_{gb} \), that corresponds to the first and second types of defects. The corresponding circuit of the GST memristor emulator can be observed on the Fig. 2.

![Fig. 2. GST memristor emulator circuit](image)

Thus, replacement of the non-linear resistor from the original circuit with the GST memristor emulator shown on the Fig. 2 leads to the design of the new Chua’s circuit with GST memristor emulator, as it can be seen from the Fig. 3.

![Fig. 3. Chua circuit with implemented GST memristor emulator circuit](image)

### III. MATHEMATICAL ANALYSIS

The mathematical analysis of the new chaotic circuit with the GST memristor emulator starts from revealing characteristic equations of the main device in the circuit - GST memristor emulator. The relationship between all components of the emulator circuit, which were described in the previous section, can be characterized by following equation for the total impedance of the circuit:

\[
Z = R_s + \frac{R_d}{1+jwR_gC_g} + \frac{R_{gb}}{1+jwR_{gb}C_{gb}} \tag{1}
\]

Based on the Eq. (1) generally the memristor emulator circuit was constructed (Fig. 2) and the corresponding values were selected, which will be discussed in the discussion section. Other important equations for characterization of the GST memristor were described by the Xiao et al [10], the characteristic equations for the GST memristor are [11]:

\[
II = M^{-1}V_M \tag{2}
\]

\[
M = f(V_M)\big[\theta\left(V_M\right)\theta\left(\frac{M}{R_1} - 1\right) + \theta(-V_M)\theta\left(1 - \frac{M}{R_2}\right)\big] \times \gamma(1 + W) \tag{3}
\]

\[
f(V) = -\beta V + \frac{\beta - \alpha}{2} \left(|V + V_L| - |V - V_R| + V_R - V_L\right) \tag{4}
\]

\[
W = W \times \phi(W)(W - W_i) \tag{5}
\]

Here, \( V_M \) and I are voltage and current passing through the memristor, \( M \) and \( W \) represents memristance and phase of GST, and \( V_L \) and \( V_R \) are threshold voltages. \( \theta() \) is the unit step function which limits memristance to the \( R_1 \) and \( R_2 \) values. Also, \( \alpha \) and \( \beta \) are characteristic rates of change of memristor, depending whether \( V_M \) is less or greater than threshold voltage, respectively. Moreover, \( \gamma \) is the correction factor for the variation of memristance because of phase transition, while \( W_i \) is the threshold of phase transition and \( \phi(W) \) is the mapping function of phase. The nature of these equations is still under the study.

Secondly, it is important to analyze the total chaotic circuit. After analysis of the chaotic circuit with HP memristor by Muthuswamy [13], the following characteristic differential equations for the circuit components without considering memristor effects were derived by him:

\[
\frac{d\phi}{dt} = V_i(t) \tag{6}
\]

\[
\frac{dV_1}{dt} = \frac{1}{C_1} \left[ \frac{V_2 - V_1}{R_1} - i(t) \right] \tag{7}
\]

\[
\frac{dV_2}{dt} = \frac{1}{C_2} \left[ \frac{V_1 - V_2}{R_1} - i_L(t) \right] \tag{8}
\]

\[
\frac{di_L}{dt} = \frac{V_2}{L} \tag{9}
\]

Taking into the account the memristor effect and using the above four equations the nonlinearity equation of the charge in chaotic circuit was derived and taken as cubic [13]:

\[
q = \theta \phi + \sigma \phi^3 \tag{10}
\]

From the Eq. (10) the next one for memductance can be derived using derivatives:

\[
W(\phi) = \frac{dq}{d\phi} = \theta + \sigma \phi^2 \tag{11}
\]
All the above equation can be related to our chaotic circuit with GST memristor, as the circuit is close to ours. All components from the HP memristor’s emulator circuit can be generally compared with the components of GST memristor’s emulator circuit. Therefore, \( \theta \) and \( \sigma \) values, which are constants from the Eq. 10 and Eq. 11 for GST memristor emulator circuit can be characterized with the following equations:

\[
\alpha = -\frac{1}{R_{\text{load}}} \tag{12}
\]

\[
\beta = \frac{1}{3} \left( \frac{R_g + R_{gb}}{R_{gb} * R_{\text{load}} * R_c} \right) \tag{13}
\]

Another important part of the chaotic circuit that must be analyzed is the negative resistor. In order to mathematically analyze the negative resistor circuit, which is designed with operational amplifier and three resistors (see Fig. 3), it is necessary to provide the small-signal analysis. Small-signal analysis is the method to express behavior of non-linear device in terms of linear equations. As it can be seen from the Fig. 3, the operational amplifier was replaced by voltage controlled voltage source, input and output resistors, which is basically the small-signal model circuit.

![Fig. 4. Chua circuit with implemented GST memristor emulator circuit and small-signal circuit for operational amplifier in the Negative Resistor](image)

From the nodal analysis of the circuit on the Fig. 5, it is clear that voltage at the node V+ represented by Eq. (14):

\[
V_+ = V_{\text{out}} i * R_{\text{plus}} = V_{\text{out}} V_s \tag{14}
\]

Where \( V_s \) is the voltage supplied by the source, in this case sinusoidal signal connected with memristor, and it is completely equal to the \( i \times R_{\text{plus}} \), because of infinitely large \( r_{in} \). And \( V_{\text{out}} \) is the output voltage of the operational-amplifier. On the other side of the open-circuit part the following equation at the node V- using Voltage divider principle can be derived:

\[
V_- = V_{\text{out}} \frac{R_{\text{minus}}}{R_{\text{minus}} + R_{\text{load}}} \tag{15}
\]

Due to the open circuit between V+ and V-, they can be considered as equal. Equalization of Eq. (14) and Eq. (15) leads to the following:

\[
V_{\text{out}} - V_s = V_{\text{out}} \frac{R_{\text{minus}}}{R_{\text{minus}} + R_{\text{load}}} \tag{16}
\]

Derivation of \( V_{\text{out}} \) from the:

\[
V_{\text{out}} = V_s (1 + \frac{R_{\text{minus}}}{R_{\text{load}}}) \tag{17}
\]

In order to find input current \( i \), the nodes V+ and Vout should be considered. As \( R_{\text{plus}} \) is the positive feedback resistance, input current goes from \( V_s \) to \( V_{\text{out}} \) through it:

\[
i = \frac{V_s - V_{\text{out}}}{R_{\text{plus}}} = \frac{V_s - V_s (1 + \frac{R_{\text{minus}}}{R_{\text{load}}})}{R_{\text{plus}}} = -\frac{V_s * R_{\text{minus}}}{R_{\text{plus}} * R_{\text{load}}} \tag{18}
\]

Consequently, resistance of the input source \( R_{\text{in}} \) is calculated simply by division of \( V_s \) to \( i \).

\[
V_{\text{out}} = \frac{V_s}{\frac{-V_s * R_{\text{minus}}}{R_{\text{plus}} * R_{\text{load}}}} = \frac{-R_{\text{plus}} * R_{\text{load}}}{R_{\text{minus}}} \tag{19}
\]

Hence, input resistance of the negative resistor circuit has negative value.

Secondly, the equation for the output resistance of the negative resistor circuit should be calculated. In order to find it
out, open circuit output voltage and short circuit current are required. Open circuit voltage can be calculated by considering node $V_{out}$ with $r_{in} = \infty$ and $r_{out} = 0$ conditions and using voltage divider technique.

$$V_{out} = A(V_+ - V_-) \frac{R_{load} + R_{minus}}{R_{load} + R_{minus} + r_{out}}$$  \quad (20)$$

Inserting equations (14) and (15) in (20):

$$V_{out} = A(V_{out} - V_s - V_{out}) \frac{R_{minus} \quad R_{load}}{R_{minus} + R_{load} \quad R_{load} + R_{minus} + r_{out}}$$  \quad (21)$$

After manipulations and solving for $V_{out}$ the following equation is received:

$$V_{out} = \frac{AV_s (R_{load} + R_{minus})}{R_{load}(1 - A) + R_{minus} + r_{out}} = V_{oc}$$  \quad (22)$$

Then, in order to find short-circuited current $i_{sc}$ the circuit on the Fig. 6 has to be analyzed.

![Fig. 6. Small-signal model for operational amplifier in Negative Resistor with open-circuited input resistance](image)

According to the Fig. 6 when the node $V_{out}$ is short-circuited, $V_{out} = 0$, the $V_-$ also becomes 0, as it was derived in (15). Therefore, the following equation is received after KCL technique:

$$i_{sc} = \frac{AV_s}{r_{out}} + \frac{AV_s}{r_{out} \quad r_{plus}} + \frac{V_s}{r_{out} \quad r_{plus}} = V_s \left(\frac{A}{r_{out} \quad 1} + \frac{1}{R_{plus}}\right)$$  \quad (23)$$

Finally, the division of (22) by (23) results in the following $R_{out}$ equation:

$$R_{out} = \frac{V_{oc}}{i_{sc}} = \frac{AV_s (R_{load} + R_{minus}) r_{out} R_{plus}}{(AR_{plus} + r_{out}) (R_{load}(1 - A) + R_{minus} + r_{out})}$$  \quad (24)$$

Considering the fact, that usually $A >> 1$ (large numbers) equation (24) can be approximated as:

$$R_{out} = \frac{(R_{load} + R_{minus}) \cdot r_{out} \cdot R_{plus}}{A \cdot R_{plus} \cdot R_{load}}$$  \quad (25)$$

IV. SIMULATION RESULTS

The simulation of this circuit with GST memristor emulator was done on the LTSpice software and the following results were received:

![Fig. 7. The Transient characteristic of output Voltage ($V_1$)](image)

![Fig. 8. The current of inductor $I_L$ and input voltage $V_2$ characteristic](image)

![Fig. 9. The output voltage $V_1$ and input voltage $V_2$ characteristic](image)
Fig. 10. The Fast Fourier Transform of output voltage $V_2$

Fig. 11. Power of the chaotic circuit with GST memristor emulator circuit implemented with resistors and capacitors

The constructed with GST memristor emulator Chua circuit has visually chaotic behavior for the voltage transient characteristic, as it can be seen from the Fig. 7. In order to demonstrate the randomness of the signal spectra, the FFT of output voltage was performed, as it can be seen on the Fig. 10. The significant variations in amplitude corresponding to different frequency values prove the randomness of the signal. However, the relationship of inductor current with input voltage and input-output voltages relationship plots do not have perfectly corresponding to theory double-scroll forms, but generally resembling double scrolls with chaotic relations with each other (Figs. 8|9). The power across the each component of GST memristor emulator circuit was found from the simulation and its power/time dependence across op-amp is shown on the Fig. 11.

V. DISCUSSION

In this paper we demonstrate the simulation for the Chua’s original chaotic circuit with non-linear resistor consisting of diodes and resistors together with modified circuit with GST memristor emulator circuit. This section aims to compare results of both circuits in order to reveal the effect of the memristor addition to the circuit.

A. Fast Fourier Transform

First of all, as it can be concluded from Fig. 10, where FFT of output voltage signals is illustrated, generally the output signal can be counted as random. As it was revealed during the research, the peak amplitude values for the original circuit attain approximately 600, while for the memristive circuit it reaches 700. Hence, deviations in voltage values for original circuit smaller than for circuit with memristor emulator, therefore the circuit with GST memristor emulator can be counted as better in terms of chaos.

B. Power analysis

Secondly, the general comparison of both circuits powers can be done in the following way. The original circuit requires 9V value for $V_{cc}$ and $V_{ee}$ for generating best chaotic output, while modified circuit requires only 3V. It means that second circuit has approximately 3 times less power dissipation. However, the real analysis revealed the following result. According to average calculation of data from each component in non-linear circuit of original chaotic Chua circuit the power is 5.02 mW. While the calculation of average power of each component in GST memristor emulator circuit of new chaotic Chua circuit gave 4.47 mW. It can be concluded, that the less power consumption of the Chua circuit with GST emulator is proved and the difference between it and the original circuit’s power is 0.55 mW. Also, from the Fig. 11 it can be visually seen that power in the circuit with GST memristor varies from about 1.20 mW to 1.80 mW, whereas in original circuit it varies from approximately 4 mW to 26 mW. In spite of receiving small variations in values, low power consumption of the circuit with GST memristor emulator is still big advantage.

C. Area analysis

Thirdly, another important comparison parameter is the area calculation. In order to calculate area of the original chaotic circuit with non-linear resistor circuit, the standard values of areas for diodes and resistors are taken. Diode 1N4148 dimensions are: 3.4×1.75 mm² for the cathode and 25.4x0.55 mm² for wires. Regular chip resistor dimensions are 0.6×0.3 mm². In total, the area of about 162 mm² will be occupied by the Chua circuit with non-linear resistor consisting of two different polarities diodes and resistors. For the chaotic circuit with GST memristor, assuming that the designed GST memristor model will be used, the total occupied area is assumed to be about 1x1 um², where the GST layer thickness is 150 nm, and for the electrodes is 100 nm, according to Li et al 9]. Hence, the area for the GST memristor model 162000 times smaller than the area for the non-linear resistor. If the emulator circuit is considered, standard dimensions for the chip capacitor are 0.51×0.25 mm². The overall area occupied by GST emulator circuit is approximately 1.155 mm², which is still 140 times lesser than the area of the non-linear resistor. Thus, in terms of area parameter it is proved that the advantage on the chaotic circuit with GST memristor side.
output of the chaotic circuit. The change is highly variable, it is difficult to observe it in the approximately 2 times and minimum of close to 0. Thus, as resistance is also chaotic and achieves the maximum of from the Fig. 13, difference between voltage values for different resistances is also chaotic and achieves the maximum of 40.9kΩ and Cgb=5pF parameters

D. Lyapunov exponents randomness test

Moreover, in order to better understand randomness in the constructed circuit, the Lyapunov exponents were generated in MatLab software. Corresponding $\theta$ and $\sigma$ values for the characteristic memductance equation of the memristor circuit calculated by Eq. [12] and Eq. [13] are $0.4 \times 10^{-3}$ and $1.35 \times 10^{-6}$ respectively. The Lyapunov exponents for the received $\sigma$ and $\theta$ parameters are shown on the Fig. 12. As it can be seen from the Fig. 12 there are two exponents that have similar pic values 4 but with different signs at the beginning. After few time firstly positive exponent (purple color) becomes negative and stable, while firstly negative exponent (yellow color) becomes fluctuating around x axis. Generally, both exponents are in close agreement and their sum (red color) is fluctuating negative exponent, which proves presence of the chaos in the circuit [13].

E. Values of components

Finally, the values of used parameters for the GST memristor emulator circuit are $R_a=100\Omega$, $R_g=25.9k\Omega$, $R_{gb}=2800\Omega$, as it is recommended in Li et al. [9], and capacitors values as $C_g=5\text{ pF}$ and $C_{gb}=30.6\text{ pF}$ are selected, as it is recommended by Li et al. [12]. Parameters for the rest circuit general elements are: $R_1=2k\Omega$, $C_2=100\text{ nF}$, $C_1=10\text{ nF}$, $L_1=18\text{ mH}$, $R_{plus}=250\Omega$, $R_{minus}=230\Omega$ and $R_{load}=2.5k\Omega$. Also, sinusoidal voltage source with 1kHz frequency and 11V amplitude is connected to memristor emulator circuit part. The variations of general elements in the circuit significantly influence on the output. That is why, these parameters are most appropriate to be used. On the same time, variations of GST memristor emulator parameters do not provide visual differences in the output. However, when the $R_g$ value is changed from 25.9kΩ to 40.9kΩ, the corresponding output data were collected and their difference was observed and plotted. As it can be observed from the Fig. 13, difference between voltage values for different resistances is also chaotic and achieves the maximum of approximately 2 times and minimum of close to 0. Thus, as the change is highly variable, it is difficult to observe it in the output of the chaotic circuit.

VI. CONCLUSION

This paper aimed to show that chaotic behavior can be achieved from the Chua’s oscillator circuit with GST memristor emulator. After construction and simulation on LTSpice software of the original Chua’s circuit with two diodes of different polarities and two pairs of different level resistors, which implements non-linear resistor functions, and of the modified Chua’s circuit with GST memristor emulator circuit results were received and compared. The chaotic output from the targeted memristive circuit was obtained, which is the expected result. Deviations in amplitude of randomness according to FFT for the new circuit to about 100 greater than in original circuit. Also, comparison in terms of area and power indicates the advantage of the Chua circuit with GST memristor emulator circuit. Additionally, Lyapunov exponents randomness test proved the presence of the chaos in the new Chua’s circuit with GST memristor emulator. More investigations of memristor emulator circuit and its parameters analysis are needed. It is recommended to study the addition of GST memristor emulator circuit to the chaotic circuits which generates N-scroll attractors, in order to receive more chaotic behavior.

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