Abstract—Traditional von Neumann architecture based processors become inefficient in terms of energy and throughput as they involve separate processing and memory units, also known as memory wall. The memory wall problem is further exacerbated when massive parallelism and frequent data movement are required between processing and memory units for real-time implementation of artificial neural network (ANN) that enables many intelligent applications. One of the most promising approach to address the memory wall problem is to carry out computations inside the memory core itself that enhances the memory bandwidth and energy efficiency for extensive computations. This paper presents an in-memory computing architecture for ANN enabling artificial intelligence (AI) and machine learning (ML) applications. The proposed architecture utilizes deep in-memory architecture based on standard six transistor (6T) static random access memory (SRAM) core for the implementation of a multi-layered perceptron. Our novel on-chip training and inference in-memory architecture reduces energy cost and enhances throughput by simultaneously accessing the multiple rows of SRAM array per precharge cycle and eliminating the frequent access of data. The proposed architecture realizes backpropagation which is the keystone during the network training using newly proposed different building blocks such as weight updation, analog multiplication, error calculation, signed analog to digital conversion, and other necessary signal control units. The proposed architecture was trained and tested on the IRIS dataset which exhibits $\approx 46\times$ more energy efficient per MAC (multiply and accumulate) operation compared to earlier classifiers.

Index Terms—In-memory computing, SRAM, artificial neural network, artificial intelligence, machine learning, classification.

I. INTRODUCTION

Artificial intelligence (AI) and machine learning (ML) algorithms are ubiquitous and integral part of contemporary computing devices, and significantly changing the way we live and interact with the world around us. Most of these computing systems are based on von Neumann architecture that involves separate processing and memory units where data need to be shuttled back and forth frequently between the processing and the memory units. Therefore, significant amount of the energy and time are consumed during data movement rather than actual computing, and this problem further exacerbated due to massive parallelism and data centric tasks such as decision making, object recognition, speech and video processing. This calls for a radical departure from the orthodox von Neumann approach to an unorthodox non-von Neumann computing architectures to carry out computations within the memory core itself, referred as to in-memory computing. Recently, hardware implementation of AI/ML algorithms based on in-memory computing has attracted huge attention because of unmatched computing performance and energy efficiency. In-memory computation overcomes the problem of frequent data movement between processing and memory units in the traditional von Neumann architecture based processors by carrying out computations within the memory core using its periphery circuitry.

Artificial Neural Network (ANN) is one of the most widely used tool for AI and ML based applications due to its very good resemblance and mimicking properties of human brain. It is used in a wide variety of AI/ML applications because of its self-learning ability to produce output that is not just limited to the input provided to them. Most of these AI/ML algorithms are software based and poses energy and delay optimization challenges for real time hardware implementation. The major limitations for hardware based solutions are large number of interconnections, massive parallelism, and time consuming calculations that requires huge data for training the networks and related algorithms. So, in-memory computation for such networks is one of the most preferred and efficient way for hardware realization of such complex networks. Researchers have come up with different in-memory implementations of popular machine learning networks and algorithms such as Convolution Neural Networks (CNNs)\cite{2,3,4}, Deep Neural Networks (DNNs)\cite{5,6} and machine learning classifiers \cite{7,8}. A large number of machine learning network architecture uses modified form of artificial neural networks such as in recurrent neural network (RNN), the fully connected layer of CNN, or in Deep Neural Networks (DNNs) which are the foundations of deep learning. There is a remarkable improvement in learning and predicting the complex pattern of a large data set which otherwise would have been very difficult even for the Graphic Processing Units (GPUs) that still require on-chip or off-chip memory access despite parallel computations for inference and training of these algorithms.

Most of the AI/ML algorithms require processing of a large data sets and the energy cost involved is mostly governed by the frequent access of memory\cite{9}, especially for dense networks such as DNNs\cite{10,11}. In DianNao\cite{11} and Eyeriss\cite{10}, the data reuse have been an efficient and highly effective solutions for saving energy, however, it still resulted in frequent on-chip memory access leading to 35% to 45% of total energy dissipation. Other techniques, such as reducing the precision of parameters to even 1-b during inference\cite{12,13,14} can address the energy and latency issues to a some extent but they will lead to accuracy trade-off. Further, implementation of architectures in digital domain using low power circuits have been employed such as power gating technique for speech recognition\cite{5}, RAZOR\cite{15} for Internet of Things (IoT) applications\cite{6}, and architectural designs such as dynamic-voltage accuracy frequency scalable CNN processor\cite{8} have been introduced earlier to reduce...
energy cost. They exploit the advantages of scalability and programmability of implementations in digital domain but they miss out the opportunities that lies in analog domain for implementation of AI/ML algorithms. This is due to the unique data flow of ANN during feedforward and backpropagation that can be exploited to design energy efficient and high throughput in-memory ANN architectures in analog domain.

Exploiting the opportunities available in analog domain for realizing in-memory AI/ML algorithms to reduce energy and delay cost, an in-memory inference processor based on deep in-memory architecture (DIMA)\cite{16, 17} have been presented earlier. The DIMA stores binary data in a column-major format as opposed to the row-major format employed in traditional Static Random Access Memory (SRAM) array organization. It reduces energy cost by simultaneously accessing multiple rows of the standard six-transistor (6T) SRAM cells per precharge cycle through the application of modulated pulse width signals to the word lines (WLs), and thus increases the throughput. Previously, DIMA is also used for AI/ML algorithms such as CNNs\cite{2} and its versatility was also established by mapping the ML algorithms for template matching\cite{18}, and architectures of sparse distributed memory\cite{19, 20}. A multifunctional in-memory inference processor\cite{16} based on DIMA have been presented earlier which achieves $53\times$ reduction in energy delay product (EDP) and supports four algorithms: support vector machine, $k$-nearest neighbour, template matching, and matched filter. But, the biggest disadvantage of DIMA was that it cannot be used for supervised learning algorithms which requires training of the network. This is because the underlying hardware of the DIMA does not support on-chip training of the network. Recent work on DNN\cite{21} deals with weight update but it requires additional buffers for storing the output before performing convolution at each stage which increases energy cost involved in frequent storage and access of data from these buffers which also increases latency.

In this paper, a DIMA based memory core is employed with proposed peripheral circuitry to realize in-memory ANN architecture. The memory read cost of the proposed architecture is reduced via DIMA functional read (DIMA-FR) process which access the multiple rows of SRAM bit cell arrays (BCA) per precharge cycle. Most of the hardware based AI/ML architectures do not support on-chip training and even if some of them does, then they do not able to avoid the frequent access to memory core during each iteration of training contributing to a large proportion in total energy and delay. To alleviate the memory access bottleneck, sampling capacitors have been used in the proposed architecture that store the weights temporarily and avoid the frequent memory access during each iteration. The proposed architecture provides on-chip hardware support for the feedforward (FF), backpropagation (BP), error calculation as well as weight updation. Further, it supports multilayered and scalable architecture by cascading the proposed single layered neural network. Each of these layer communicates with its preceding and next layer in the same way a neural network does. Moreover, a large variety of AI/ML algorithms can be implemented using the proposed architecture by just changing the activation function block and the number of memory banks in the architecture according to the requirements. Overall, the proposed architecture exactly mimics the way a neural network works and it is configurable to realize variety of neural networks based AI/ML algorithms. Simulation results demonstrate that the proposed architecture achieves $\approx 1.04\times$ reduction in energy delay product (EDP) and $\approx 46\times$ reduction is energy per multiply-and-accumulate (MAC) operation. In contrast to existing in-memory computing architectures, following are the key contributions of the proposed architecture:

1) **Hardware support for on-chip training**– Hardware support for feedforward and backpropagation process is designed in the periphery of SRAM bitcell array that mimics the way a neural network works. Further, the weight update mechanism has been developed without the need of intermediate buffers to avoid latency and energy cost involved in read/write mechanism of such buffers. Moreover, appropriate control signals have been designed for parallelizing weight update process of the whole network.

2) **On-chip error calculation**– An on-chip sum of squares of error calculating mechanism have been developed whose gradients with respect to weights are back propagated for network training.

3) **Signed flash ADC design**– The signed flash ADC is designed and presented to stored updated signed weights back inside SRAM memory core which follows $1’s$ complement conversion method for negative weights.

**II. BACKGROUND**

This Section discusses the pre-requisites for the development of artificial neural network\cite{22} and hardware implementation of deep in-memory architecture (DIMA)\cite{16, 17}.

**A. Neural Network**

The neural network is a complex network of neurons where each of the connections is characterized by synaptic weights. There are three basic elements of neuron:

1) **set of synapses or connecting links**– each characterized by a weight,

2) **an adder**– for summing the products of input signal and corresponding synapse weight, and

3) **an activation function**– typically sigmoid, tanh, or ReLU that limits the output of a neuron. Fig. 1 shows the generalized multilayered perceptron neural network exhibiting the signals at each layer during feedforward (in black colour) and backpropagation (in red colour). Both feedforward and backpropagation have been shown in the same network for a better understanding of signal flow during each of these two processes. In Fig. 1, $N_K$ (for $K \in W$, where $W$ denotes the whole number) corresponds to total number of neurons in the $K^{th}$ layer ($K = 0$ corresponds to the input layer). The $w^{[K]}_{ij}$ denotes weight of the synaptic connection to the $j^{th}$ neuron (of the $K^{th}$ layer) from the $i^{th}$ neuron (of its previous layer). In this paper, the subscripts $i, j, k,$ and $l$ (for $i, j, k, l \in W$) are used for indexing the properties/signals associated with a particular neuron and the superscript $[K]$ for indicating the layer to which it is associated with. Paired subscript, such as $‘ij’$ shows that the property is associated with the connection
of \(i^{th}\) neuron of any layer to the \(j^{th}\) neuron of its next layer. The training of the network takes place in two phases using the backpropagation algorithm\(^{22}\).

Forward Phase: In forward phase, the weights of the network are initialized and the input signals are propagated layer by layer through the entire network until they reach to the output layer. From Fig. 1, the output at the \(K^{th}\) layer is given by the following matrix multiplication and subsequently by the application of activation function on it as shown below:

\[
\begin{bmatrix}
    a^{[K]}_1 \\
    a^{[K]}_2 \\
    \vdots \\
    a^{[K]}_{N_K}
\end{bmatrix} = \varphi
\begin{bmatrix}
    w^{[K]}_{11} & w^{[K]}_{12} & \cdots & w^{[K]}_{1N_{K-1}} \\
    w^{[K]}_{21} & w^{[K]}_{22} & \cdots & w^{[K]}_{2N_{K-1}} \\
    \vdots & \vdots & \ddots & \vdots \\
    w^{[K]}_{N_{K-1}1} & w^{[K]}_{N_{K-1}2} & \cdots & w^{[K]}_{N_{K-1}N_{K-1}}
\end{bmatrix}
\begin{bmatrix}
    a^{[K-1]}_1 \\
    a^{[K-1]}_2 \\
    \vdots \\
    a^{[K-1]}_{N_{K-1}}
\end{bmatrix}
\]  

where \(\varphi(\cdot)\) is the activation function at the output of the neurons in the \(K^{th}\) layer.

Backward Phase: Once the final output is available during the forward phase, then the error is calculated by comparing the final output with the target (or intended) output. The error at any output neuron is calculated as \(e_l = t_l - y_l\), where \(y_l\) is the current output and \(t_l\) is the target (or intended) output at the \(l^{th}\) output neuron. For calculating the total error of the network there are many cost functions available of which the sum of squares of error is the most popular one which is given as:

\[
E = \frac{1}{2} \sum_{l=1}^{N_3} e_l^2
\]  

In Eq. 2 the square of error will be summed up for all the output neurons in Fig. 1. The resulting error is propagated through the network in the backward direction and successive weight adjustments/updates are made to the synaptic weights using gradient descent algorithm. The gradient descent algorithm states that weight should be moved in the direction of negative gradient of the error landscape to minimize the error of the network. Mathematically, the weight update of the synaptic connections to the \(K^{th}\) layer is given as:

\[
w^{[K]}_{jk} \leftarrow w^{[K]}_{jk} - \eta \frac{\partial E}{\partial w^{[K]}_{jk}} = w^{[K]}_{jk} + \Delta w^{[K]}_{jk}
\]  

where \(E\) is the error as calculated in Eq. 2 and \(\Delta w^{[K]}_{jk} = -\eta \frac{\partial E}{\partial w^{[K]}_{jk}}\) is the change in weight required to reduce the error of the network. Now, depending upon where the neuron is situated in the network, two cases arise. Firstly, when the neuron will be at the output layer of ANN. In this case, the desired response at each of the output node is supplied during training, making this case a straightforward way to handle from error calculation and weight updation point of view. Secondly, when the neuron is situated at any hidden layer. Hidden layer neurons are not directly accessible but they do share the responsibility for the total error of the network. At the same time their desired response is not known beforehand which makes the estimation of their contribution in total error even more difficult. Both cases are discussed in detail as follows:

- **CASE I: ‘K’ denotes an output layer**– The desired response at an output neuron is known in this case as
discussed earlier, so Eq. [2] (and Fig. [1]) can be used directly to calculate the weight change as:

$$\Delta w_{jk}^{[3]} = \eta (t_l - y_l) \varphi^{[3]}(h_k^{[3]}) a_k^{[2]} = \eta \delta_k^{[2]} a_k^{[2]}$$

(4)

where \( h_k^{[3]} = \sum_{l=1}^{N_2} a_k^{[2]} w_{kl}^{[3]} \) is the activation potential at the \( l^{th} \) neuron of the output layer, \( \delta_k^{[3]} = (t_l - y_l) \varphi^{[3]}(h_k^{[3]}) \) is the local gradient at the \( k^{th} \) neuron of the output layer of Fig. [1] and \( \varphi^{[3]}(\cdot) \) is the derivative of the activation function.

• **CASE II: ‘K’ denotes a hidden layer–** There is no specified desired response in this case, hence the error signal has to be determined recursively and working backward in terms of the error signals of all the neurons to which that hidden neuron is directly connected. Using Eq. [2] and applying chain rule the simplified result[22] can be obtained as:

$$\Delta w_{jk}^{[2]} = \eta \left( \sum_{l=1}^{N_3} \delta_l^{[3]} w_{kl}^{[2]} \right) \varphi^{[2]}(h_k^{[2]}) a_j^{[1]} = \eta \delta_k^{[2]} a_j^{[1]}$$

(5)

where \( \delta_k^{[2]} = \sum_{l=1}^{N_3} (\delta_l^{[3]} w_{kl}^{[2]} \varphi^{[2]}(h_k^{[2]})) \) is the local gradient at the \( k^{th} \) neuron of the \( 2^{nd} \) layer of the Fig. [1].

Similarly, the weight update for the \( 1^{st} \) layer is given as:

$$\Delta w_{jk}^{[1]} = \eta \delta_l^{[1]} a_j^{[0]}$$

(6)

This is how error is propagated backward in the network. This back propagation of error is shown in red color in Fig. [1]. The above derivations are described for a multilayered perceptron neural network with only two hidden layers, however, the same concept can be extended to any number of hidden layers.

**B. Basics of In-Memory Architecture**

The main and mature element of in-memory computing is the standard six transistor (6T) static random access memory (SRAM) cell/array, where most of the computations are performed in parallel and mixed-signal domain which results in significant improvement in throughput and energy efficiency. Recently, a 6T-SRAM based deep in-memory architecture (DIMA) has demonstrated very good energy efficiency for many intelligent and data intensive applications. Fig. [2] shows the conventional DIMA architecture. The DIMA uses the standard SRAM bit cell array (BCA) with read/write circuitry at the bottom and stores \( B_W \) bits of weight in a column-major format as opposed to the row-major format used in conventional SRAM cell. The DIMA consists of four processes that are executed sequentially.

1. **Multi-row Functional READ (FR)**– that performs digital to analog conversion of weights \( w \) (index \( i,j,k,l \) and \( [K] \) are omitted for simplicity) stored in standard 6T SRAM cell by fetching \( B_W \) bits of weight which is achieved by simultaneously reading \( B_W \) rows per pre-charge cycle.

2. **Bit Line Processing (BLP)**– calculates scalar distances (SDs) by carrying out mathematical operations (such as - addition, subtraction, multiplication, etc.) between weights stored in SRAM cells and the applied input signal.

3. **Cross BLP (CBLP)** – carries out the summation of scalar distances (SDs) via charge sharing across the required columns of the bit cell array to calculate the vector distances (VDs) such as dot product if SD is multiplication in BLP stage, or Manhattan distance if SD is absolute difference in BLP stage, and

4. **Analog-to-Digital Converter (ADC) and Residual Digital Logic (RDL)**– stage for realizing thresholding/decision function and carrying out analog to digital conversion of the results of previous analog computations.

Fig. [2]b shows the multi-row functional read process of the DIMA. The multi-row functional read stage yields a voltage discharge \( \Delta V_{BL} \) proportional to the weighted sum \( \bar{w} = \sum_{i=0}^{B_W-1} 2^i b_i \) of column-major stored digital data \( \{b_0, b_1, ..., b_{B_W-1}\} \) by applying binary-weighted modulated pulse width signal \( T_i \propto 2^i (i \in [0, B_W-1]) \) to \( B_W \) rows of SRAM array simultaneously, as shown in Fig. [2]b. The voltage drop on bitline (BL) as a function of weight \( w \) is given by:

$$\Delta V_{BL} = \frac{V_{PRE}}{R_{BL} C_{BL}} T_0 \sum_{i=0}^{B_W-1} 2^i b_i = \Delta V_{lb} \bar{w}$$

(7)

where \( \Delta V_{lb} = \frac{V_{PRE}}{R_{BL} C_{BL}} T_0, \) \( V_{PRE} \) is the precharge voltage on BL and its complement (BLB) lines, \( R_{BL} \) and \( C_{BL} \) are the discharge path resistance and capacitance respectively, \( \bar{w} \) is the decimal equivalent of \( 1 \)'s complement of weight stored in SRAM cell array in column-major format. Similarly, the voltage drop at the complement of BL (i.e. BLB) line can be expressed by simply replacing \( \bar{w} \) with \( w \) in Eq. [7] i.e.,:

$$\Delta V_{BLB} = \frac{V_{PRE}}{R_{BL} C_{BL}} T_0 \sum_{i=0}^{B_W-1} 2^i b_i = \Delta V_{lb} w$$

(8)

It is important to note that both Eqs. [7] and [8] are valid for \( T_i \ll R_{BL} C_{BL} \). A sub-ranged read technique[16] can be employed for improving the linearity of the FR process when \( B_W > 4 \) for which \( B_W/2 \) bits representing the most significant bits (MSB) and \( B_W/2 \) bits representing the least significant bits (LSB) of the weights stored in adjacent columns of the BCA. For this, the MSB and LSB BL capacitances \( C_M \) and \( C_L \) respectively, are required to be in the ratio \( 2 B_W/2 : 1 \). The MSB and LSB columns are first read separately and then merged by assigning more weights to MSB than LSB using ratioed capacitors \( C_M \) and \( C_L \).

However, the inference processor presented in ref. [16] supports four algorithms - Support Vector Machine, Template Matching, k-Nearest Neighbour, and Matched Filter which have been just mapped to them without discussing the way to train the network on the chip. Further, the peripheral circuits used around memory core in standard DIMA architecture lacks the hardware support for backpropagation algorithm and weight update mechanism which is a crucial part in training any neural networks. Also, frequent access to SRAM bitcell array during calculation of scalar distance (SD) at each iteration in conventional DIMA[16] architecture leads to a significant amount energy dissipation and latency. To realize hardware implementation of ANN along with addressing above discussed issues related to DIMA and other architectures discussed in introductory part of this paper, an in-memory ANN architecture is proposed in next Section.
III. THE PROPOSED IN-MEMORY ANN ARCHITECTURE

In this Section, the proposed In-Memory Artificial Neural Network architecture is presented. First, detailed architecture and working of a single layer of a neural network is discussed and then it is extended to the multilayered perceptron consisting of interconnections of many such layers. Fig. 2(c) shows a generalized block diagram of single DIMA-based memory bank. It is a basic building block of our proposed in-memory ANN architecture. Each memory bank corresponds to a single output neuron. As discussed in previous Section, the peripheral BCA circuitry of the traditional DIMA architecture is incapable of carrying out on-chip training of the network, therefore, we have incorporated the additional peripheral circuitry that facilitate the on-chip training and supports both feedforward and backpropagation processes for realizing the in-memory ANN. The proposed in-memory ANN architecture utilizes the last \( B_W \) rows of the BCA for storing weights (in column-major format) of the synaptic connections of an ANN and are accessed via multi-row FR process which yields the analog equivalent of stored weight as shown in Fig. 2(b). The rest of the memory space, i.e., \( \left[ N_{\text{col},K} \times (N_{\text{row}} - B_W) \right] \) bits of the BCA can be used as a general purpose digital storage medium.

Fig. 3 shows the proposed in-memory ANN architecture of any arbitrary layer of ANN. We have used \( M \) and \( N \) as general terms indicating the number of inputs and outputs, respectively, of the \( K^{\text{th}} \) layer. From Fig. 3 multi-bank division of the BCA have been done for parallelizing the computations involved in each layer of the ANN. Each bank is used to store weights of the connections from the outputs of the previous layer to the input of a neuron in the present layer. Each bank consists of \( M \) columns, for storing weights of the connection from \( M \) inputs to an output of this layer. Further, the number of such banks, \( N_{\text{bank},K} \), depends on the number of neurons at the output of this layer which is assumed to be \( N \) in our case. The FR process performs the analog to digital conversion of weights by discharging the BLB and BL lines.

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**TABLE 1**

| Notation | Description                                      |
|----------|--------------------------------------------------|
| ADC      | Analog to Digital Converter                      |
| ANN      | Artificial Neural Network                        |
| BCA      | Bit Cell Array                                   |
| BL       | Bit Line                                         |
| BLP      | Bit Line Bar                                     |
| \( B_W \) | No. of bits per weight                          |
| DIMA     | Deep In-Memory Architecture                      |
| FR       | Functional Read                                  |
| \( M = (N_{K-1}) \) | No. of inputs to the \( K^{\text{th}} \) layer |
| \( N = (N_{K}) \) | No. of output of the \( K^{\text{th}} \) layer   |
| \( N_{\text{bank},K} \) | No. of banks for the \( K^{\text{th}} \) layer   |
| \( N_{\text{col},K} \) | No. of columns per memory bank for the \( K^{\text{th}} \) layer |
| \( N_{\text{row}} \) | No. of rows in the bit cell array                |
| SA       | Sense Amplifier                                  |
| SWC      | Signed Weight Calculation                        |
| SM       | Signed Multiplier                                |
| \( MT \) lines | \( M \)-transmission lines                      |
| \( NT \) lines | \( N \)-transmission lines                      |
| WL       | Word Line                                        |
| WU       | Weight Updation                                  |

---

**FIG. 2.** (a) Conventional deep in-memory architecture (DIMA) [16]. (b) Memory access via functional read (FR) process of the DIMA for four bits per weight (\( B_W = 4 \)), (c) Generalized block diagram of the proposed architecture which employs FR of DIMA for accessing weights stored in last \( B_W \) rows of SRAM bitcell array (BCA).

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**FIG. 3.** Shows the proposed in-memory ANN architecture of any arbitrary layer of ANN. We have used \( M \) and \( N \) as general terms indicating the number of inputs and outputs, respectively, of the \( K^{\text{th}} \) layer. From Fig. 3 multi-bank division of the BCA have been done for parallelizing the computations involved in each layer of the ANN. Each bank is used to store weights of the connections from the outputs of the previous layer to the input of a neuron in the present layer. Each bank consists of \( M \) columns, for storing weights of the connection from \( M \) inputs to an output of this layer. Further, the number of such banks, \( N_{\text{bank},K} \), depends on the number of neurons at the output of this layer which is assumed to be \( N \) in our case. The FR process performs the analog to digital conversion of weights by discharging the BLB and BL lines.
by an amount proportional to their decimal equivalent \( w \) and its \( 1 \)'s complement \( \overline{w} \), and can be derived from Eqs. 8 and 7, respectively. Since, the weights can be either positive or negative, so a signed weight calculation (SWC) unit is designed for generating these weights in terms of proportional negative voltage (for negative weights) or positive voltage (for positive weights). The signed weights thus will be generated and sent to the weight updation (WU) unit where weights are updated in each iteration and then sent to the signed multiplier (SM) unit, these peripheral circuits are essential for on-chip training that makes our proposed approach energy efficient and real time.

The input vector \( X = [a_1, a_2, \ldots, a_M] \) (index \( i, j, k, l \) and \( [K] \) have been omitted to avoid confusion and \( [a_1, a_2, \ldots, a_M] \) is taken as the inputs to any general layer, i.e., the \( K^{th} \) layer) to this layer are fetched via \( M \)-transmission \((MT)\) lines each storing analog voltages proportional to the inputs to the layer, as shown in Fig. 3(a). These inputs are sent to the SM units where it is multiplied with signed weights, calculated via SWC units during feedforward process, to generate product of input and signed weight. To generate activation potential we need to sum these individual products at each of the output neuron, i.e., \( \sum_{j=1}^{M} a_j^{[K-1]} w_{jk}^{[K]} \) for which current based summation of weighted inputs is employed inside the activation potential block (discussed in upcoming sub-sections). The output of the activation potential block is sampled and stored in capacitor to avoid its regeneration during backpropagation where it will be used for weight update. This activation potential is fed to the activation function block from where the final output of the layer is obtained. The output of the layer are sent to the next layer through \( NT \) lines.

During backpropagation, the signals traverse through various components of the network and they will be governed by Eqs. 4, 5 and 6. The weighted sum of the local gradients (the weights applied to the local gradient are the weights of synaptic connections between the layer having the local gradients and its previous layer) of any layer are propagated backward to the previous layer which is multiplied with its input and learning rate for its weight update. Also, from Eqs. 4, 5 and 6 for generating local gradient at any neuron in the present layer, the weighted summation of the local gradient coming from the next layer is multiplied with the derivative of the activation function of the present layer neuron. In our proposed architecture, the weighted sum of the local gradients of any layer, i.e., the \( K^{th} \) layer is generated via current based summation which is employed inside the backpropagation block and is propagated to the previous layer through \( MT \) lines coming out, as shown in Fig. 3(a)). For the weight update, the local gradient of this layer is multiplied with input to this layer and sent to the weight updation (WU) unit. The learning factor \( \eta \) can be controlled by controlling the gain at the output of the multiplier going to WU unit. During feedforward and backpropagation processes, different signals need to be multiplied together which is controlled by control

\[
X = [a_1, a_2, \ldots, a_M]
\]

![Fig. 3. (a) Block diagram showing proposed in-memory multi-bank implementation of ANN. The T. lines (transmission lines) carrying forward propagating signals are shown in blue color, and the T. lines (transmission lines) carrying backpropagating signals are shown in red color. (b) A single DIMA based memory bank connected to \( M \) SWC & WU units.](image-url)
signal $s[1:0]$. Once the training of the network finishes, the WU unit will have all the trained weights stored in it. These trained weights need to be stored in BCA memory core since these weights are analog and susceptible to noise, weights may also drift due to noise/charge leakage then entire network will have to be trained again to avoid accuracy loss. To address weight drifting issue, signed flash ADC is designed and presented which will convert the signed weight to digital domain considering 1’s complement conversion for negative weights since the BL line have voltage discharge proportional to decimal equivalent of 1’s complement of weight which can be used to obtain absolute value of the negative weight during FR read process which can be further converted to proportional negative voltage. The output of signed flash ADC will be stored in SRAM BCA. The upcoming Subsections present detailed description of these blocks to support in-memory ANN essentials for on-chip training.

A. Signed Weight Calculation (SWC) Unit

Fig. 3(b) shows a single bank DIMA with SWC and weight updation (WU) units for generating signed and updating the weights, respectively. The weights of synaptic connections can either be negative or positive which will require a hardware circuitry that must be equipped with a suitable scheme to realize signed dot product. The signed dot product calculator has been proposed earlier in ref.[2] which has two rails: CBLP+ rail (for positive product) and CBLP− rail (for negative product) shared with multiple columns each corresponding to the output of a BLP block. The BLP block was used there to select the magnitude of weight and then calculate the product of input vector with weights stored in SRAM. These products were then shared with CBLP+ rail for positive weights and CBLP− rail for negative weights. These weights were accessed via DIMA FR process to get proportional analog equivalent of weight. These selection of BL or BLB lines for getting absolute value of weight and selection of CBLP+ or CBLP− rail depending on sign of product were done using control circuitry inside BLP block itself. These rails were then passed through the ADC and fed to the subtractor block which calculates the difference between them to get vector distance. However, this approach is inefficient for updating the weights during each iteration (on-chip training) because we are performing computations in analog domain to ease the process of weight updation by storing intermediate weights in capacitors (discussed in the next Sub-section). If computations were done in digital domain then it would have required additional registers/buffers to store intermediate weight during training consuming large silicon chip area for dense network involving a large number of weights.

Also, the methodology employed in ref.[2] for signed dot product cannot be used for our purpose since it uses the change in voltage of BLB and BL line which are proportional to the decimal equivalent of weight and its 1’s complement, respectively, which cannot be added/subtracted directly in the analog domain for performing addition/subtraction operation. Therefore, a signed weight calculation (SWC) unit is designed, as shown in Fig. 4. It works on the principle that one of the lines among BL (for negative weight) or BLB (for positive weight) will have voltage discharge proportional to the absolute magnitude of weight, as per from Eqs. 7 and 8. As we have assumed earlier that signed weight stored in BCA will follow 1’s complement scheme for negative weight. This magnitude has to be converted to proportional negative or positive voltage. For this, first the sign $S_W$ and $V_{mux}$ are generated with the help of circuitry shown in Fig. 4(a)), and corresponding expressions are:

$$S_W = \begin{cases} 0; & \text{for } V_{BLB} \geq V_{BL}, \text{ i.e., when } w \geq 0 \\ 1; & \text{for } V_{BLB} < V_{BL}, \text{ i.e., when } w < 0 \end{cases} \quad (9)$$

The output of MUX, $V_{mux}$ is selected from among the BL and BLB since one of them will have absolute value of weight in terms of voltage change on the line (from Eqs. 7 and 8). The selection is done using the sign of weights as the select line as:

$$|w| = \begin{cases} \sum_{k=0}^{Bw-1} 2^k b_k \propto \Delta V_{BLB}; & \text{if } S_W = 0 \\ \sum_{k=0}^{Bw-1} 2^k b_k \propto \Delta V_{BL}; & \text{if } S_W = 1 \end{cases} \quad (10)$$

Thus, the output voltage of MUX, $V_{mux}$ will contain the absolute value of weight as given by:

$$V_{mux} = V_{PRE} - \Delta V_{lsb} |w| \quad (11)$$

Thus the change in MUX voltage will be given by:

$$\Delta V_{max} = V_{PRE} - V_{mux} = \Delta V_{lsb} |w| \propto |w| \quad (12)$$

For calculation of signed weights the circuit in Fig. 4(b) is employed. It uses OPAMP for maintaining the voltage polarity based on value of $S_W$, can be seen from Fig. 4(c)-(d)). Thus, the output voltage at this stage will have positive or negative sign corresponding to positive or negative weights stored in the SRAM array and their magnitude will be proportional to the magnitude of corresponding weight, i.e., $|w|$.

B. Backpropagation and Weight Updation Units

Backpropagation and weight updation are the most important part of any neural network for learning by adjusting its weight for accurate prediction and decision making until error is reduced to a minimum possible value. These updated weights have to be accessed frequently during feedforward and backpropagation processes that incur high energy and delay cost during frequent access of SRAM BCA for storing and accessing the updated weights during each iteration of network training. However, for improved throughput, energy efficiency, and on-chip training, we have designed a dedicated circuitry that eliminates this requirement and makes the proposed in-memory ANN architecture suitable for various AI/ML applications, as shown in Fig. 4(e). In the proposed backpropagation and weight updation units, the generated signed weight $w_{jk}^{[k]}$ is first sampled using switched connection $\phi_S$ and stored in a sampling capacitor $C_S$ (shown in Fig. 4(e)) instead of storing them in SRAM BCA. The $C_S$ will be used to store all the intermediate weight corresponding to a single synaptic connection. The $M \times N$ such weight updation units of Fig. 4(e) will be required corresponding to the weights of all the $M \times N$ connections involved in the $K^{th}$ layer of the proposed architecture of the network, as shown in Fig. 3(a).
Generalizing from Eqs. 5-6, the change in weight $\Delta w_{jk}[K]$ required for weight update is generated via SM unit (discussed in the next Sub-section) and is sampled on another sampling capacitor $C_B$ via switched connection $\phi_B$, shown in Fig. 4(e).

The unity gain buffer is used to access the voltage stored in the sampling capacitors. The charge leakage problem of these unity gain buffers are applied at the two ends of the series combination of two resistors of equal magnitude $R$. Thus, the generated voltage at their common node $V_U$ will be proportional to the sum of voltages corresponding to weight and change in weight, i.e., $V_U = (w_{jk}[K] + \Delta w_{jk}[K])/2$. The output is then latched/stored on another sampling capacitor $C_L$ (via switched connection $\phi_L$) which will be used to update intermediate stage weights stored in sampling capacitor $C_S$. But the voltage $V_U$ have to be amplified by a factor of 2 to make the updated weight $wj_{jk}[K]$ exactly equal to the sum of original weight and change in weight required. This amplification can be done using any suitable scheme. One of them may be to use an OPAMP based non-inverting amplifier of gain 2 as shown in Fig. 4(e). The updated weight $w_{jk}[K]$ is then sent to the next unit for carrying out multiplication.

Weight update of the hidden layers is not a straightforward task as discussed in last section. Eqs. 5 and 6 can be generalized to state that the weighted sum of the local gradient, i.e., $\sum_k \delta_k w_{jk}[K]'$, is used by the $j^{th}$ neuron of the previous layer for its weight update. The hardware implementation for the backpropagation block is shown in Fig. 5(a). The product $\delta_k w_{jk}[K]'$ obtained from the signed multiplier (SM) unit corresponding to $j^{th}$ column of the $k^{th}$ bank is added over all the $k$'s, i.e., over all banks to generate the sum $S_j$, as shown in Fig. 5(a). The final output at each backpropagating line will be proportional to the weighted sum of local gradient which will be fed to the previous layer for its weight update. Once the local gradient of all the layers have been calculated via the backpropagation process, then the weight update process can be parallized by just changing the control signal to $S[1:0] = 10$ given in Table II and discussed in detail in next Sub-section.

C. Four Quadrant Analog Multiplier

As discussed, different signals need to be multiplied during feedforward and backpropagation processes. An accurate multiplier for the neural network is essential for better training and overall performance of the proposed in-memory ANN architecture. Fig. 5(b) shows the architecture of the proposed signed multiplier (SM) unit employed to carry out multiplication of different signals depending upon the 2-b control signal.
Fig. 5. (a) Proposed hardware for carrying out backpropagation. (b) Realization of SM (Signed Multiplier) unit. (c) Four quadrant analog multiplier used inside SM unit.

Fig. 6. Realization of pair of current sources used in Fig. 5(c).

$S[1:0]$ applied to it. Depending upon control signals, the proposed multiplier will select different pairs of signals for multiplication, as shown in Table III. Fig. 5(c) shows the hardware implementation of the four-quadrant analog multiplier which is the core of the proposed SM unit. In the proposed four-quadrant multiplier, the NMOS/PMOS work in the triode region to generate output proportional to the product of inputs $V_{in1}$ and $V_{in2}$.

For very small drain to source voltage, the drain current of NMOS in linear/triode region is given by [23]:

$$i_{Dn} = \mu_n C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_{Thn}) V_{DS}$$

(13)

where, $\mu_n$ is the electron mobility, $C_{ox}$ is the gate capacitance per unit area, $\left( \frac{W}{L} \right)$ is the aspect ratio, $V_{GS}$ and $V_{DS}$ are gate to source and drain to source voltages, respectively, and $V_{Thn}$ is the threshold voltage. Similarly, the drain current of PMOS is given by:

$$i_{Dp} = \mu_p C_{ox} \left( \frac{W}{L} \right) (V_{SG} - |V_{Thp}|) V_{SD}$$

(14)

where, $\mu_p$ is the hole mobility, $V_{Thp}$ is the threshold voltage of the PMOS, the rest of the quantities have the usual meaning as in Eq. 13. These Eqs. 13 and 14 will be valid for two sets of conditions: (i) $V_{GS} > V_{Thn}$ and $V_{DS} \ll V_{GS} - V_{Thn}$ for NMOS and; (ii) $V_{SG} > |V_{Thp}|$ and $V_{SD} \ll V_{SG} - |V_{Thp}|$
for PMOS. To satisfy these conditions, the pre-processing block is designed, as shown in Fig. 5(c)). Inside the pre-processing block, the voltage $V_{in2}$ is reduced in amplitude by an amount $A$ (reduction factor) that is sufficient enough to satisfy the necessary conditions on $V_{DS}$ (for NMOS) and $V_{SD}$ (for PMOS). There would be an obvious variation in multiplier output for different values of reduction factor, $A$, which are discussed in the next Section along with simulations results. Next, if $V_{GS} = V_{in1} + V_{Tn}$ (for NMOS) and $V_{GS} = V_{in1} - |V_{Pn}|$ (for PMOS) is applied to the gate of the MOSFETs (as shown in Fig. 5(c)) then, from Eqs. 13 and 14, the output current will be proportional to the product of input voltages. The above additions are performed inside the pre-processing block. Now, the outputs of the pre-processing block satisfies both necessary conditions (i) and (ii)) for the proposed multiplier to work properly. The outputs of the pre-processing block are fed to the multiplier, as shown in Fig. 5(c). The analog multiplier generates current that is proportional to the product of inputs voltages $V_{in1}$ and $V_{in2}$. Two current sources of equal gain $K_i$ are employed to generate the output current so that it could be used to drive the next stage. There are many ways to realize the pair of current sources used in Fig. 5(c). One of them can be to use a pair of OPAMP and an OTA (Operational Transconductance Amplifier) as shown in Fig. 6 which is used for simulations presented in next Section. The generated output current will be proportional to the product of input voltages within some offset error $\varepsilon_m$, i.e., $I_{mult} \propto (V_{in1}, V_{in2} \pm \varepsilon_m)$. The occurrence of error will be due to small deviation from the linear behaviour of the MOSFETs in the triode region. This is because I-V characteristics of the MOSFET will not be perfectly linear in the triode region. But the effect of non-linearity can be reduced by decreasing the drain to source voltage which can be achieved by increasing the value of reduction factor $A$ used in the pre-processing block in Fig. 5(c). Thus, the effect of error, $\varepsilon_m$, can be reduced by choosing a suitable value of the reduction factor $A$. The variations of $\varepsilon_m$ versus $A$ are shown in next the Section.

\section*{D. Activation Potential and Activation Function}

Fig. 7 shows the hardware implementation of activation potential and activation function for generating the output at any layer of perceptron. During feedforward, the product $I_{mult}(\propto \delta_l^{[K-1]}w_{jk}^{[K]})$ generated via SM unit and it is sent to the activation function block which carries out current based summation of input signals, as shown in Fig. 7(b). The total current $I_{TOT}$ will be proportional to the weighted sum of inputs, i.e., $I_{TOT} \propto \sum_j \delta_l^{[K-1]}w_{jk}^{[K]}$. But, we need output of the activation function in terms of voltage since the next layer requires input signal in the form of voltage instead of current. As input of multiplier requires signals in the form of voltage instead of current, a unity gain buffer is employed which converts the current through a resistor $R$ to a voltage, as shown in Fig. 7(b). The value of $R$ can be adjusted properly to make $I_{TOT}$ exactly equal to the weighted sum of inputs. This activation potential is stored in a capacitor $C$ and accessed via unity gain buffer. This is done to avoid its regeneration during backpropagation where it will be used for weight update. Activation functions perform a transformation on the input received, in order to keep values within a manageable range. There is a wide variety of activation functions available, such as linear, sigmoid, tanh, ReLU, etc. Out of these, the ReLU is the most popular and frequently used activation function for hidden layers. For the proposed in-memory ANN architecture, we have employed and designed the ReLU activation function and its output can be expressed as:

$$a_k^{[K]} = \varphi (h_k^{[K]}) = \max (0, h_k^{[K]})$$

where $h_k^{[K]}$ is the activation potential of the present layer and $a_k^{[K]}$ is the output of the present layer generated after applying activation function $\varphi$ on $h_k^{[K]}$. Its differentiation is also very simple as given:

$$\varphi'(h_k^{[K]}) = \begin{cases} 0, & \text{for } h_k^{[K]} \leq 0 \\ 1, & \text{for } h_k^{[K]} > 0 \end{cases}$$

Fig. 7(c) shows the hardware implementation of the ReLU function and its derivative. The MUX A1 performs the maximum operation as per Eq. 15 by selecting the maximum voltage based on comparator output. Another MUX A2 is used for generating the local gradient of this layer, which will be the product of differentiation of activation function and the weighted sum of the local gradient of the next layer, i.e.,

$$\delta_k^{[K]} = \left( \sum_j \delta_l^{[K+1]}w_{kl}^{[K+1]} \right) \varphi'(h_k^{[K+1]})$$

Using Eq. 16 the local gradient of this layer can be expressed as:

$$\delta_k^{[K]} = \begin{cases} 0, & \text{for } h_k^{[K]} \leq 0 \\ \sum_j \delta_l^{[K+1]}w_{kl}^{[K+1]}, & \text{for } h_k^{[K]} > 0 \end{cases}$$

The MUX A2 performs operation as per Eq. 17 based on the output of the comparator. But, ReLU is used only for the hidden layer. For output layer generally linear (for linear regression); sigmoid, tanh (for binary classification); or softmax (for multi-class classification) is used. The realization of linear activation function at the output is pretty much simple by just allowing the output to be equal to the input. Also, its derivative being equal to unity does not require any multiplier block for multiplying the error with derivative of activation function during backpropagation. But hardware realization of other non-linear activation function in the analog domain is quite complex. Instead, activation functions such as sigmoid, tanh, softmax and other non-linear activation functions can be easily realized in the digital domain using different approximation methods and/or look-up table (LUT) based methods. So, the incoming analog voltage corresponding to activation potential is first converted to the digital domain using ADC and then any of the above mentioned activation functions can be implemented digitally based on the requirement. In this paper, the softmax activation function have been employed and its output is converted back to the analog domain using DAC.

\section*{E. Multilayered Implementation Neural Network}

We have realized and discussed all the individual blocks needed for single layer of in-memory ANN architecture. However, for contemporary AI/ML applications, single layer
neural network needs to be extended for multilayered neural network along with on-chip training capability. Fig. 8(a) shows the multilayered perceptron model designed by cascading single-layered neural network. One of major advantages of the proposed neural network architecture is its scalability, as shown in Fig. 8(a), that is, any number of such architecture can be cascaded to design a multilayered perceptron with on-chip training capability. At the output layer, there will not be any further connections to the next layer but instead, there will be a mechanism for calculating the error of the network. The output of the sum of squares of error block is fed to the control signal block which controls the feedforward and backpropagation during the network training. The control signal block will stop the network training if the error $V_E$ has stopped decreasing. The error at any neuron is given as the difference between target/intended output and the current output. For this, an OPAMP subtractor circuit is used, as shown in Fig. 8(b) to calculate the difference $e_l (= t_l - y_l)$ at the $l^{th}$ neuron of the output layer. This difference is further sent to another two OPAMPs for calculating the difference $V_{Gn,l} (= V_{Tn} - e_l)$ and $V_{Gp,l} (= - |V_{Tp} - e_l|$) which is used for calculating the sum of squares of error in next stage, where, $V_{Gn,l}$ denotes the gate voltage of the NMOS at the $l^{th}$ output, similarly $V_{Gp,l}$ denotes the gate voltage of the PMOS at the $l^{th}$ output node.

Consider the MOSFET’s current in saturation region [23]:

$$I_D = \begin{cases} \\ \frac{1}{2} k_n (V_{GS} - V_{Tn})^2, & \text{for NMOS} \\ \frac{1}{2} k_p (V_{SG} - |V_{Tp}|)^2, & \text{for PMOS} \end{cases}$$

(18)

where, the parameters have usual meaning as mentioned in Eqs. 13 and 14. Now if $V_{Gn,l} (= V_{Tn} - e_l)$, generated via Fig. 8(b), is applied to the gate of NMOS then, for $e_l < 0$, \[ \sum_i \delta_i^{[K+1]} w_i^{[K+1]} \] \[ \sum_i \delta_i^{[K+1]} w_i^{[K+1]} \] \[ \sum_i \delta_i^{[K+1]} w_i^{[K+1]} \] \[ \sum_i \delta_i^{[K+1]} w_i^{[K+1]} \] \[ \sum_i \delta_i^{[K+1]} w_i^{[K+1]} \]
the drain current of the NMOS would be:

\[ I_{Dn,l} = \frac{1}{2} k_n (V_{Gn,l} - V_{Th})^2 = \frac{1}{2} k_n e_l^2 \quad (19) \]

For \( e_l > 0 \), no current will flow through the NMOS which will wrongly reflect that the error of the network has become zero although it has actually not. So an innovative mechanism consisting of a combination of NMOS and PMOS having equal transconductance parameter \( k (= k_n = k_p) \) is designed, as shown in Fig. 8(c) which will work even for \( e_l > 0 \). From Fig. 8(c), the gate to source voltage for PMOS will be \( V_{Gp,l} (= - |V_{Tp}| - e_l) \) which will be negative and less than \(- |V_{Tp}|\) for \( e_l > 0 \), hence PMOS will be in ON state. At any instant, either the NMOS or PMOS will be in ON state at the \( l^{th} \) output, thus, the square of the error will be easily generated. Another important observation is that for the square of the error to be generated correctly, i.e., for Eq. 18 to be satisfied the MOSFET must always be in saturation which will happen when \( V_{DS} \geq V_{GS} - V_{Th} \) (for NMOS) and \( V_{DS} \geq V_{SG} - |V_{Tp}| \) (for PMOS). For that, the same potential is applied to the drain and source, as shown in Fig. 8(c). This will ensure that the condition for the MOSFET to be in saturation is always satisfied. Next is the generation of the sum of square of errors, for which an OPAMP is employed to sum up the current flowing through each of the MOSFET as:

\[ I = \sum_{l} (I_{Dn,l} + I_{Dp,l}) = \frac{1}{2} k \sum_{l} e_l^2 \quad (20) \]

From above discussions, we can conclude for Eq. 20 that either of the \( I_{Dn,l} \) or \( I_{Dp,l} \) will always be zero since the hardware implementation in Fig. 8(c) is designed in such a way that only one of the MOSFETs (either NMOS or PMOS) will be ON at each of the output. Next, the final current flowing through OPAMP is converted to voltage \( V_E \) using resistor \( R_1 \) as shown:

\[ V_E = -IR_1 = -\frac{1}{2} k R_1 \sum_{l} e_l^2 \quad (21) \]

The negative sign is used since the voltage at the output of OPAMP will be negative when the current will flow in the conventional direction of NMOS as shown in Fig. 8(c). Negative polarity of voltage can be ignored since we are only interested in the magnitude of the error and our aim will be to make the magnitude of error as small as possible.

\( F: \) Signed Flash ADC

The trained weights have to be stored back in SRAM BCA to avoid training the network again and again. Since, the proposed architecture deals with negative/positive weights in the form of analog voltage so the general architecture of ADC
needs to be modified to meet our requirements for the proposed in-memory ANN architecture. Specifically, for negative updated weights we need an ADC that uses 1’s complement rule for analog to digital conversion. Therefore, a 4-bit signed flash ADC is designed and presented in Fig. 9(a). The flash ADC is chosen due to its speed and optimal silicon chip area for storing them back in SRAM BCA. In standard flash ADC, only positive reference voltage, i.e., $V_{REF}$ are used as opposed to the proposed implementation where both negative and positive reference voltage $V_{REF}$ and $-V_{REF}$ have been used. Further, comparison of both positive and negative analog voltages (corresponding to proportional negative and positive updated weights) have been performed using resistor ladder network. The outputs of the comparators are fed to priority encoder for generating final output which is the digital equivalent of the magnitude of the input voltage $V_{in}$. For negative $V_{in}$, the desired output is 1’s complement of the digital equivalent of the magnitude of voltage for which NOT gate is used at the output of the priority encoder corresponding to negative reference voltage of $-V_{REF}$ to generate its 1’s complement.

For signed conversion using 1’s complement, the positive number have MSB equals 0 and negative number have MSB equals 1. To incorporate it, the MSB is chosen as the output of the first comparator (U8) employed for comparing negative voltage, as shown in Fig. 9(a). This will ensure the MSB $b_3$ to be 0 for positive weights and 1 for negative weights lesser than $-V_{res}/2$, where $V_{res}$ is the resolution of the ADC in volts per step. Further, to reduce the output data line only one of the priority encoders is allowed to work at a time by applying $b_3$ as enable signal to the EN input of each of the priority encoders. Thus, for $b_3 = 0$ the priority encoder corresponding to positive reference voltage is enabled and for $b_3 = 1$ the priority encoder corresponding to negative reference voltage is enabled. Hence, the designed ADC works for both positive and negative weights. The reference voltage $V_{REF}$ decides the maximum swing of the ADC as well as the range of weights. The transfer function and value of the $V_{REF}$ of the proposed signed flash ADC are discussed in detail in the next Section.

G. Timing Diagram

Fig. 9(b) shows the timing diagram of the whole network. ‘P’ is the total number of epochs, ‘L’ is the total number of training samples presented to the network per epoch, ‘C’ is the total number of the layers. The notation: [0] → [1] denotes the forward propagation from input to the first hidden layer, and $[0] \leftrightarrow [1]$ denotes backpropagation from the first hidden layer to the input layer. With the same notation different index is used to indicate propagation between different layers. The working of the network starts with FR process of the SRAM BCA which fetches proportional analog equivalent of weights to the SWC units. Each SWC unit calculates the signed weight and sends the output to the WU unit. Once the FR process and SWC units have finish their work, then the whole training and testing procedure are controlled by $2 - b$ control signal $S[1:0]$. During feedforward, the control signal switches to ‘01’ and calculates the activation potential at each layer which is latched to sampling capacitor, via switched connection $\phi_{OUT}$, at the output of each layer. Next, the error of the network is calculated using the sum of squares of error cost function which is fed to the control block. If the error is still in reducing phase then the control block continues training the network otherwise the training is terminated. If the error has not stopped decreasing the next stage is the backpropagation phase ($S[1:0]=11'$) where the sum of local gradient is calculated inside the backpropagation block and...
is transmitted to previous layer via transmission lines. Once the backpropagation process completed then control signal switches to ‘10’ for weight updation. As training completes, the updated weights are stored back inside the SRAM BCA via signed flash ADC. Each of these major process is shown in timing diagram in Fig. 9(b). Further, each of these major process is further divided into smaller sub-process for a clear insight into the working of the network.

IV. SIMULATION RESULTS AND DISCUSSIONS

In this Section, the simulation results and working of the proposed architecture are presented. Simulations of all the peripheral computing blocks were performed with SPICE simulator using High-Performance 45nm PTM (Predictive Technology Model) models[27]. The design parameter chosen for simulation are summarized in Table III.

| Parameter          | Value  |
|--------------------|--------|
| Technology         | 45nm PTM HP |
| $V_{DD}$           | 1 V    |
| $V_{FR/RE}$ (of BL & BLB) | 1 V |
| W/L                | 2      |
| SRAM bit cell      | 6T     |
| $T_0$ (FR Read)    | 0.3 ns |
| $BW$               | 4      |
| $V_{REF}$          | 0.456 V |

TABLE III
DESIGN PARAMETERS FOR SIMULATION

Fig. 10. (a) Simulation result of magnitude of weight calculated via $\Delta V_{\text{max}}$ inside SWC unit and its deviation (in LSB) from ideal (expected) output for 4-b resolution. (b) 4-b weight dependent energy dissipation during FR read process. (c) Simulation result of updated weights for $\eta = 1$. (d) Transfer function of the proposed multiplier of Fig. 5(c).
or all one. As in this case either BL or BLB line will discharge completely and other will remain at a precharge voltage $V_{PRE}$ level. However, with magnitude of weight increases both BL and BLB lines discharge by some amount, as a result, either the number of discharge paths, the discharge time, or both of these increases. Hence, energy dissipation during the FR process increases with an increase in weight magnitude. The total energy dissipation during the FR process of the SRAM BCA can be modeled as:

$$E_{Total}(w) = \sum_{k} A_k(w) e^{-2\alpha_k \cdot f(w)}$$  \hspace{1cm} (22)$$

where, $\alpha = T_0/\tau_0$, $T_0$ is pulse width applied at the WL of the LSB row of DIMA, $\tau_0 = C_{BL}\cdot R_{BL}$ is the time constant of the circuit, $A_k(w)$ is the coefficient term that depends on the decimal equivalent of the weight stored in the SRAM BCA, and $f(w)$ is a linear function of decimal equivalent of weight $w$.

The maximum delay during FR read will be decided by the maximum time duration of the modulated pulse width WL signal applied to the MSB row which is 2.4 ns in our case for 4-b weights stored in SRAM BCA. Fig. 10(c) shows the variation of trained weight with signed weight (calculated in SWC unit) for different values of $\Delta w$, for $R = 1\ k\Omega$ and learning rate $\eta = 1$. The variation is found to be linear from simulation results as it is expected from Eq. 3.

Fig. 10(d) shows the transfer function of the proposed multiplier (see Fig. 5(c)). Designed multiplier employs a current controlled current source (CCCS) using a pair of OPAMP and an OTA, as shown in Fig. 6 (as discussed in previous Section). The desired output is effectively achieved within some error, as can be seen from simulation results for a current gain factor $K_i = 250$. The value of $R = 25 \\Omega$ and $G_m = 10$ (for CCCS used in Fig. 6) was used to make the current gain $K_i = G_m R$ equals 250 for simulation shown in Figs. 10(d) and 11(a). The error $\epsilon_m$ associated with the proposed multiplier can be reduced by increasing the reduction factor $A$ used in the pre-processing block of Fig. 5(c). For error analysis, multiplier output current was converted to a voltage by passing it through 1 k$\Omega$ resistance and measuring the voltage across

![Image](https://via.placeholder.com/150)

**Fig. 11.** (a) Energy dissipation in MOSFETs used inside multiplier of Fig. 5(c). (b) Worst case analysis of error, $\epsilon_m$, associated with multiplier output with reduction factor $A$ for different polarity of inputs $V_{in1}$ and $V_{in2}$ but each having equal magnitude of 1 V. (c) Transfer function and power dissipation of the proposed hardware for realizing ReLU activation function. (d) Simulation result of transfer function and energy dissipation of hardware (see Fig. 8(c)) used for realizing square of error. The simulation results are for a single neuron at the output layer, i.e., for $N_3 = 1$ in Fig. 8(c).
Gradient Descent

\[ E \approx \text{Sum of squares of error} \]

\[ \eta \approx \text{Learning rate} \]

\[ \text{Optimizer} = \text{Gradient Descent} \]

\[ \text{Activation Function} = \text{ReLU (for hidden layer)} \]

\[ \text{Softmax (for output layer)} \]

\[ \text{Dataset} = \text{Iris [28]} \]

\[ \text{Trainig Results on Iris Dataset} \]

\[ \text{Epochs} = 500 \]

\[ \text{Accuracy} \approx 99\% \]

\[ \text{Energy} \approx 0.84 \mu \text{J/epoch (} \approx 7.002 \text{ nJ/iteration}) \]

\[ \text{Delay} \approx 82.0352 \mu \text{s/epoch} \approx 0.685 \mu \text{s/iteration} \]

\[ \text{Testing Results on Iris Dataset} \]

\[ \text{Accuracy} \approx 96.67\% \]

\[ \text{Energy/Decision(pJ)} = 1.85 \]

\[ \text{Delay/Decision(ns)} = 680.6 \]

\[ \text{Decision/s} = 1.47 \text{ M} \]

\[ \text{EDP/Decision(J-s)} = 1.26 \times 10^{-18} \]

\[ \text{TABLE IV} \]

\[ N_{\text{col}} = \text{No. of input layer neurons} \]

\[ \text{No. of hidden layers} = 5 \]

\[ N_{\text{hid},1} = \text{No. of hidden layer neurons} \]

\[ N_{\text{hid},2} = \text{No. of hidden layer neurons} \]

\[ N_{\text{out},2} = \text{No. of output layer neurons} = 3 \]

\[ \text{Loss function} = \text{Sum of squares of error} \]

\[ \text{Optimizers} = \text{Gradient Descent} \]

\[ \text{Learning rate} (\eta) = 0.1 \]

\[ \text{Activation Function} = \text{ReLU (for hidden layer)} \]

\[ \text{Softmax (for output layer)} \]

\[ \text{Dataset} = \text{Iris [28]} \]

\[ \text{Trainig Results on Iris Dataset} \]

\[ \text{Epochs} = 500 \]

\[ \text{Accuracy} \approx 99\% \]

\[ \text{Energy} \approx 0.84 \mu \text{J/epoch (} \approx 7.002 \text{ nJ/iteration}) \]

\[ \text{Delay} \approx 82.0352 \mu \text{s/epoch} \approx 0.685 \mu \text{s/iteration} \]

\[ \text{Testing Results on Iris Dataset} \]

\[ \text{Accuracy} \approx 96.67\% \]

\[ \text{Energy/Decision(pJ)} = 1.85 \]

\[ \text{Delay/Decision(ns)} = 680.6 \]

\[ \text{Decision/s} = 1.47 \text{ M} \]

\[ \text{EDP/Decision(J-s)} = 1.26 \times 10^{-18} \]

\[ \text{TABLE IV} \]

\[ \text{Parameter} \]

\[ \text{Value} \]

\[ \text{N}_{\text{col}} = \text{No. of input layer neurons} \]

\[ 4 \]

\[ \text{No. of hidden layers} \]

\[ 5 \]

\[ \text{N}_{\text{hid},1} = \text{No. of hidden layer neurons} \]

\[ 5 \]

\[ \text{N}_{\text{hid},2} = \text{No. of hidden layer neurons} \]

\[ 5 \]

\[ \text{N}_{\text{out},2} = \text{No. of output layer neurons} \]

\[ 3 \]

\[ \text{Loss function} \]

\[ \text{Sum of squares of error} \]

\[ \text{Optimizer} \]

\[ \text{Gradient Descent} \]

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function which works better for classification task, i.e., our proposed architecture will work fine for regression task with square of error cost function but for classification problem other cost functions such as cross entropy works even better.

V. CONCLUSION

In-memory on-chip trainable and scalable artificial neural network was designed and developed for wide variety of data intensive AI/ML algorithms. The main focus of the presented architecture was to exploit the in-memory analog computations for realizing the of ANN with on-chip training facility. The proposed architecture is scalable and re-configurable to map a large variety of AI/ML algorithms by enabling different activation functions and cost functions. The main strength of the proposed architecture lies in the fact that each steps from training to inference can be performed on-chip without external computing resources. Further, it does not require temporary registers/buffers for storing intermediate results that makes our proposed approach energy and computationally efficient.

A neural network, being a complex interconnections of a large number of neurons, requires huge computations. Even some of the recently proposed architecture uses binary weights to reduce complexity but it may lead to accuracy issues since weights can have any real value (not necessarily only 0 and 1). Instead, in this paper, all the operations of a neural network are done in the analog domain which avoids such accuracy issues. However, some of the accuracy issues may arise during analog to digital conversion but that can be resolved using more number of bits/weight. Then the whole network was trained and tested on the iris dataset where the classification accuracy was estimated to be around $\approx 96.67\%$. Further, energy and delay analysis shows that the proposed work is $\approx 46\times$ energy efficient in MAC (multiply-and-accumulate) operation as compared to previous work which employs DIMA.

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