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Data-Driven Neuromorphic DRAM-based CNN and RNN Accelerators

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Abstract—The energy consumed by running large deep neural networks (DNNs) on hardware accelerators is dominated by the need for lots of fast memory to store both states and weights. This large required memory is currently only economically viable through DRAM. Although DRAM is high-throughput and low-cost memory (costing 20X less than SRAM), its long random access latency is bad for the unpredictable access patterns in spiking neural networks (SNNs). In addition, accessing data from DRAM costs orders of magnitude more energy than doing arithmetic with that data. SNNs are energy-efficient if local memory is available and few spikes are generated. This paper reports on our developments over the last 5 years of convolutional and recurrent deep neural network hardware accelerators that exploit either spatial or temporal sparsity similar to SNNs but achieve SOA throughput, power efficiency and latency even with the use of DRAM for the required storage of the weights and states of large DNNs.

There is currently interest from some mainstream AI communities in the relevance of neuromorphic engineering for artificial intelligence (AI). In particular, can Spiking Neural Networks (SNNs) bring benefits to the Deep Neural Network (DNN) architectures used in AI? These networks can be contrasted with conventional analog neural networks (ANNs) by their brain-inspired organization of interconnected spiking neurons to form DNNs. Around 2015, we strongly believed that SNNs were key to making progress in addressing the huge inefficiencies in power consumption of hardware AI accelerators. We still believe this, but with a more nuanced view of the realities of what silicon and current memory technologies can offer.

The main contribution of this paper is to summarize for a lay audience our findings over the last 5 years of work towards the aim illustrated in Fig. [1] We show that state-of-art (SOA) throughput, energy efficiency and latency can be achieved by convolutional and recurrent neural network (CNN and RNN) hardware accelerators that exploit data-driven synchronous architectures. We conclude by comparing hardware SNNs with ANNs.

Note: Our basic measure of computation (addition or multiplication) is the operation, or Op. When measuring DNN accelerator performance, a multiply-accumulate (MAC) or synaptic accumulation operation is counted as 2 Op.

I. SPARSITY IN THE BRAIN’S SPIKING NEURAL NETWORKS

Suppose we want to estimate the average spike rate $X$ of the brain’s network of spiking neurons consuming $Y \sim 10W$ power. We will assume that every spike leads to one synaptic activation per synapse (i.e. we ignore significant synaptic activation failures of probably more than 50%). If we multiply $X$ by the energy per synaptic activation, the number of synapses per neuron, and the number of neurons in the network, the result is the overall power consumption $Y$. (Metabolism accounts for only about half the brain’s energy consumption; about half is purely electrical [1].) The first interesting results from this calculation (shown in Fig. [2] is that the average spike rate $X$ is only about 1 Hz, which is about 2 orders of magnitude lower than typical sensor sample rates. In other words, most DNNs that infer the meaning of sensor input update every neuron much more frequently than 1 Hz.

This calculation should not be taken too literally. Spike rates for active biological sensory input and motor output neurons are higher than 1 Hz, and all the other numbers can be off by a factor at least 2. The main point is that most brain energy is consumed by synaptic events, and only when they occur.
We find two more interesting observations from this napkin estimate: First, the large fan-out of $10^4$ means that neurons are still getting input at an average rate of 10 kHz even with 1 Hz average spike rate. So they have the opportunity to spike with this much higher timing precision. Second, the fan-out of $10^4$ is not so much higher than well-known CNNs: For example, consider a CNN with 100 feature maps and 5x5 kernels. Then the fan-in to the next layer neurons will be 2500, which is not much less than $10^4$.

Fig. 2 also calculates that the energy per biological synaptic update is about 100 fJ, which equates to 10 TOps/s/W. Recent SRAM-based low-precision DNN accelerators are approaching this 10 TOps/s/W power efficiency, but the match to the number computed in Fig. 2 is a bit misleading for two reasons: Firstly, one must assume that in the brain, each spike is precious and so it is likely that each synaptic operation contributes useful information to a computation, while in conventional DNNs, the operations are carried out no matter what their importance is. Secondly, a biological synaptic event has complex dynamics that are certainly not present in a MAC. The neurons in the ANN are equivalent to a point neuron which ignores the complex and nonlinear dendritic tree of a real neuron, and which almost certainly has rich computational properties that are barely appreciated.

II. OUR FIRST HARDWARE SNNs

The fact that SNNs are inspired by the brain’s spiking networks and arguments like the preceding suggest significant advantages of SNNs compared with ANNs in that they access memory and compute only when needed. Computer demonstrations showed advantages such as lower operation count and quicker output, e.g. as in [2].

Our earliest developments of hardware SNN accelerators were in the CAVIAR project [3], a multi-chip, multi-partner project where one of the Spanish partners implemented the first convolutional SNN ASIC [4]. CAVIAR drove the development of the first DVS event camera [5], and it was also a breakthrough by its demonstration of a fully-hardware mixed-signal convolutional SNN vision sensor system, but it would have been impractical for production because of the large number of ICs that it would need. The only way to increase the size of the network it could run would be to add more chips.

Our subsequent implementation of an SNN accelerator was called Minitaur [6]. Minitaur was implemented on an FPGA and is our first event-driven digital implementation. It was based on the premise that the network weights and states are stored in DRAM and local SRAM is used to cache the recently-used values, so that they can be quickly and cheaply accessed when needed. But Minitaur could not deliver a high throughput. On admittedly a low-performance 50 MHz Spartan-3 FPGA, it could only handle input spike rates of up to a few kHz when implementing a small 2-layer fully-connected network with a few thousand units and about 100,000 weights. The basic problem is that we cannot use SRAM alone to hold the parameters of a large network, and to take advantage of sparsity, neurons should not need to fire repeatedly, but Minitaur relied on repeated firing to have high cache hit rate.

III. SNNs CAN BE ACCURATE

Minitaur led to a very useful outcome in that it shaped our later work on building DNN accelerators. It was the basis for an eventual successful proposal to an industry partner to explore SNNs and power-efficient ANNs. At the time, the partner strongly doubted if SNNs can achieve reasonable classification accuracy on a large dataset. We therefore undertook a study to investigate if SNNs could produce equivalent accuracy on the same classification task as ANNs. In this study, we first looked at a previously proposed method for converting a CNN using ReLUs to a spiking CNN [7], and then developed improved methods for converting continuous-valued CNNs and multi-layer perceptrons (MLPs) to equivalent-accurate SNNs [8]. We later showed that we can also train for low-latency, low-compute SNNs [2]. Our student Bodo Rueckauer took this on, and developed new conversion methods that improve on the classification accuracy of deeper SNNs. These methods show that larger pre-trained ANNs (e.g. VGG-16 and GoogLeNet Inception-V3) can be converted into equivalent SNNs that have the best SOA accuracy results at the time [9].

We also demonstrated that SNNs could be trained using backpropagation to SOA classification accuracy on MNIST [10]. Researchers are now exploring many interesting ideas for training SNNs using local learning rules, or approximations using spike rates during backprop.

IV. TWO PROBLEMS WITH SNNs

It turned out that there were two big problems with these results in relation to silicon implementation of SNNs:

1) Although we can convert pre-trained ANNs to equivalent SNNs to achieve almost equal accuracy as ANNs, the conversion equates activations to spike rates. The resulting SNN spike rates requires sending many spikes per activation value when the activation value is high. By contrast, a standard ANN sends just the activation value itself. The result was that the SNN was usually more costly to run than the ANN, i.e. required more synaptic operations than the MACs in the ANN.

2) As we will discuss in Sec. VIII, the resulting asynchronous unpredictable spikes made memory access unpredictable, which ruled out using DRAM memory, but only DRAM is affordable for scaling the hardware to big DNNs (SRAM is 20X more area than DRAM).

Since our observations of point 1, tools like [11] have enabled more people to train SNNs using backprop and were used to show that at least for shallow classifiers—where low precision activations provide sufficient accuracy—SNNs can achieve equivalent accuracy as ANNs with fewer synaptic
operations. But Minitaur and point \(^2\) stuck in our minds. We asked, would it possible to make use of sparsity in a synchronous DNN? Before going into these developments, we make a slight digression to review the architecture of DRAM.

V. DRAM ACCESS MUST BE PREDICTABLE

In dynamic random access memory, a bit is stored using a single transistor switch as charge on a capacitor. Since the charge leaks away, it must be periodically refreshed by reading and restoring the bit. DRAM architecture has two important features, one good and one bad.

Firstly, because a DRAM bit cell needs only a single transistor and a highly optimized cylindrical capacitor, it is very tiny and therefore cheap. By contrast, a static random access memory (SRAM) cell is constructed as a bistable latch circuit from a minimum of 6 transistors. It makes an SRAM cell area about 20X larger than a DRAM cell. Although the digital nature of SRAM state makes it very fast to write and read, it is costly compared with DRAM for storing large amounts of data.

Secondly, reading the bit of charge stored in a DRAM cell takes time, because it is done by putting a special type of metastable latch called a sense amplifier into its metastable point and then dumping the charge onto the latch’s input. Since the latch is large compared to a bit cell, and the sensing takes time, sensing the charge is done in parallel at the bottom of long columns of hundreds of DRAM bit cells. To read DRAM memory, you address with the ‘word line’ a row of cells. The sense amps connected to the column ‘bit lines’ then read the bits stored in the cells of that row. The sense amplifier digital outputs are then read out very fast using burst mode. If the DRAM reads and writes can be scheduled, then DRAM achieves high bandwidth. But reading DRAM memory randomly is much slower (e.g., 50X slower in the case of DDR3 DRAM) than reading it out row by row, at least in terms of throughput. This extreme asymmetry is illustrated in Fig. 3.

To summarize, accessing DRAM is only fast if the IO can be scheduled to consist of series of predictable pipelined burst transfers.

VI. ACCELERATING CNNS BY EXPLOITING SPATIAL ACTIVATION SPARSITY

Since we wanted an accelerator that could scale itself to any sized network, we needed to use DRAM, but this ruled out ‘pure’ asynchronous SNNs because of their unpredictable memory access. But we thought that it might still be possible to exploit activation sparsity.

Although the Rectified Linear Unit (ReLU) activation function sprang from neuroscience \([13]\), it was not until about 2010 \([14], [15]\) that the ReLU has widely been used in CNNs. Since ReLU output is zero anytime the input is non-positive, using it results in many zeros in feature maps. These zero pixels are like SNN neurons that are not spiking. They cannot have any downstream influence, so why bother to compute their MACs? But how many zeros are there in practice?

Fig. 4 show measurements of activation sparsity across layers in a classifier CNN. If the network is trained and run with floating point precision, the sparsity is about 50% \([16]\). While developing tools for quantizing weights, we discovered that if the network is trained to 16-bit weight and state precision by using a quantization technique called dual-copy rounding or Pow-2 ternarization \([17], [18]\), the average sparsity rises to nearly 80%. It means that 4/5 of the pixels are zero. It seems that the quantization training increases activation sparsity. Whatever the reason, in principle, we can skip over any sized network, we needed to use DRAM, but this ruled out ‘pure’ asynchronous SNNs because of their unpredictable memory access. But we thought that it might still be possible to exploit activation sparsity.

The first published CNN accelerator to exploit activation sparsity was the well-known EyeRiss \([19]\). Its dataflow architecture used each DRAM access for hundreds of MACs, but it did not take full advantage of ReLU sparsity because it decompressed and recompressed the run-length-encoded feature maps and just power-gated the MAC units.

Development of our NullHop CNN accelerator was started by postdoc H. Mostafa, and then taken over by our student Alessandro Aimar \([12]\). Nullhop is more efficient than Eyeriss by using several features illustrated in Fig. 5. It stores the feature maps using a sparsity map (SM) compression scheme.
The SM is a bitmap that marks non-zero feature map pixels with a ‘1’ bit, and stores the non-zero values in a non zero value list (NZVL). That way it uses only 1 bit for inactive pixels and the full precision of 16 bits in the NZVL, plus 1 SM bit for active pixels. The logic that processes the input feature maps to generate output feature maps never decompresses the feature maps and skips over all zero pixels without using any clock cycles. Its pooling-ReLU unit saves a lot of intermediate memory access when max-pooling feature maps.

Since the DRAM DDR3/4 memory interface IP block is too expensive for us, our reported NullHop results are from a 28nm process technology simulation and the System-on-Chip FPGA implementation. In 28nm technology, NullHop would achieve a core power efficiency of about 3 TOPs/W with area efficiency of about 100 GOp/s/mm². Factoring in DDR3 DRAM, the system level efficiency would be about 1.5 TOPs/W with area of about 6 mm² and throughput of about 500 GOPs. By exploiting the spatial activation sparsity, NullHop achieves an efficiency of almost 400% for large image classification networks, by skipping MACs for zero activations. 400% efficiency means that each MAC unit does the work of 4 MAC units that do not exploit sparsity.

The efficiency is worth comparing to the brain sparsity estimate from above. In contrast to the brain power efficiency estimate, where we only count actual synaptic operations, for accelerators that exploit sparsity, an operation is counted even if it is skipped. It is a fair comparison with accelerators that do not exploit data sparsity.

Fig. 5 compares CNN throughput versus power for a number of published and unpublished accelerators. The CNN accelerators that Aimar is currently developing, called Elements, include both kernel compression and flexible bit precision. The power reported in this chart does not include DRAM power for DRAM-based accelerators. The NullHop and Elements accelerators are labelled NPP. The ones labeled “SRAM/MRAM based” use only on-chip memory. They achieve high power efficiency but are either very limited (BinarEye [20]) or expensive (Lightspur). Aimar’s Elements modeling shows that including DRAM limits power efficiency to around 2 TOPs/W (based on DDR3 energies), and publications hint to similar limits. So, despite the impressive amortization of DRAM memory power by sharing the weights and activations across all the involved operations, CNN accelerators are hitting a memory bottleneck that is ultimately limited by DRAM energy itself.

VI. ACCELERATING RNNs BY EXPLOITING TEMPORAL ACTIVATION SPARSITY IN DELTA NETS

Nullhop was a step in the direction of an SNN-like synchronous accelerator, but it did not exploit any temporal sparsity. Was it possible to use this idea for CNNs, by making them stateful and only updating the units that change? Despite the publication of [27], we quickly discovered that in most cases it was not beneficial. Because a CNN is feedforward and stateless, it turns out that it is nearly always cheaper to completely compute the output of a layer by using the output of the previous layer, rather than propagating changes. To compute state changes, one would need to store each layer’s activations, and then read them before (possibly) updating them. It means that we would need to store, read, and write large parts of the entire network state rather than recreating it for each new input frame.

Stateless CNNs only benefit from exploiting temporal sparsity when this sparsity is very high, e.g. as in some surveillance applications [28], but the architectures that benefit hugely from exploiting temporal sparsity are RNNs. In contrast with CNNs, RNNs are stateful and the state space is rather small, since it generally consists of vectors representing e.g., in the input case, an audio spectrogram window or a set of low dimensional sensor signals. In contrast with CNNs, where each weight can be used many times, the big weight matrices in RNNs that connect the layers take a lot of memory bandwidth to read, and each weight is only used once per update. By using an RNN batch size > 1, or by processing multiple RNNs in parallel, it is possible to reuse weights, but we are mainly interested in real-time applications on embedded platforms where we get a new input sample and need to compute the RNN response to that sample as quickly as possible.

Thus we asked ourselves if it would be possible to propagate only significant changes through an RNN without losing...
accuracy. The answer came from our student Daniel Neil in our DeltaNet paper [29]. He showed that you can get away with only updating units downstream from those whose activity changes by more than \( \delta \) without huge accuracy loss. And if you include \( \delta \) in the forward pass during training, it helps the RNN to maintain higher prediction accuracy. The \( \delta \) is bit like a spike threshold, but it is evaluated synchronously in the DeltaNet, and the DeltaNet sends the full analog value of the activation to downstream units. Using these delta events requires storing the pre-activation states of the neurons rather than the usual post activation values, but the cost in memory or operations is not increased.

Using this DeltaNet principle reduces memory access by 5X-100X, depending on the input statistics. Thus a DeltaRNN sparsely computes in the temporal domain like a spiking neural network (SNN), but plays nice with DRAM by allowing a more predictable synchronous memory access.

Our student Chang Gao has implemented several generations of DeltaRNN on FPGAs. Fig. 7 shows a high level description of the blocks for the first published implementation [30]. It achieved a throughput of 1.2 TOp/s on wall plug power of about 15 W. This first implementation used FPGA block RAM (BRAM) rather than DRAM for the weights. His subsequent implementation for portable edge computing which we call EdgeDRNN [31] runs on a $89 FPGA board. It uses DRAM for the weights. Running a 2L-768H-DeltaGRU, it achieves a mean effective throughput of 20.2 GOp/s and a wall plug power efficiency of about 8 GOp/s/W which is higher by at least a factor of at least four compared to the NVIDIA Jetson Nano, Jetson TX2 and Intel Neural Compute Stick 2, for a batch size of 1. It is also at least six times quicker than these devices. Since more than 80% of EdgeDRNN power is for things like the ARM core processors, UART, and other support, the overall power efficiency is on the lower end of published RNN accelerators, but it remarkably achieves with 2.4 W wall plug power the same latency as a 92 W Nvidia GTX 1080 GPU.

Fig. 8 compares RNN throughput versus power for a number of published and unpublished accelerators. The ASIC publications omit DRAM and system power so they would be pushed way over to the right if these were included. Like for CNNs, RNN accelerators seem to be hitting an efficiency wall of a few hundred GOp/s/W that is determined by DRAM energy. It seems that MRAM-based RNN accelerators are an attractive target if fixed memory size is OK.

### VIII. Features and FOMs

Certain features make DRAM-based accelerators attractive, especially for system integration:

- **Flexibility in DNN size**, so it can run a range of networks, without much change in power efficiency, and so that the cost in memory is only enough to run the particular network.
- **Flexibility in DNN type**, so that can handle a tasks ranging from classification, detection, semantic pixel labeling, and video processing, requiring various levels of weight and especially state precision.
- **Cost sharing in a system environment**, e.g. ability to share existing memory and (and expensive) memory interface. An accelerator can be measured by a combination of figures-of-merit (FOMs) that rank how well it achieves certain objectives:

1. it must be cheap, i.e. have high Op/s/mm² area efficiency.
2. it must be fast enough, i.e. achieve sufficient Op/s throughput.
3. it must be cool enough at this throughput, i.e. achieve high Op/s/W power efficiency.

Synchronous CNN accelerators achieve throughput of about 1 TOp/s with area around 10 mm², i.e. area efficiency of 100 GOp/s/mm². High efficiency is achieved by high clock frequency and keeping the multipliers full of data.

Current DRAM-based CNN accelerator power efficiency seems to be asymptotically converging around few TOp/s/W, and more memory bound RNN accelerators are hitting about 100 GOp/s/W.
DRAM-based CNN accelerators achieve this high power efficiency by maximizing the reuse of the values fetched from DRAM: Kernels are kept in SRAM until the the entire layer has been processed. Activation values—typically from a patch across all the feature maps centered on a location in the image—are kept in SRAM until all the values are used to process the associated patch of output feature maps. That way, each value fetched from DRAM is used hundreds or thousands of times. This reuse amortizes the energy cost of the DRAM memory access so that it becomes similar to a local SRAM access. Once the layer pair has been processed, the kernels are not needed again for that frame of input. The result is that the arithmetic and memory access energy becomes comparable to that of SOA SNNs. It makes sense, because they use the same transistors and logic circuits to do the operations.

In a synchronous CNN accelerator, once a layer has been used to compute all its downstream targets, it can be discarded. It means that synchronous layer-by-layer CNN accelerators do not need to store the entire network activation state. A DRAM-based accelerator has the additional advantage that it can share the memory and its interface with other applications.

IX. Conclusion

Starting from SNNs, we found out that the key principles of data-driven sparse computing can equally benefit more flexible synchronous DNN accelerators. There is still potential in exploiting more data sparsity, not only in activations but also in the network connections. This area is very active in the mainstream accelerator community.

The availability of new memory technology could bring memory closer to computation, and even swap the roles: It is possible that memory itself will do the processing rather than the way we have it now [57]. But this step will require a huge change in system architectures and will probably require a compelling application for the required investment at all levels of the supply chain.

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REFERENCES

[1] S. B. Laughlin and T. J. Sejnowski, “Communication in neuronal networks,” Science, vol. 301, no. 5641, pp. 1870–1874, 2003.
[2] D. Neil, M. Pfeiffer, and S.-C. Liu, “Learning to be efficient: Algorithms for training low-latency, low-compute deep spiking neural networks,” in Proceedings of the 31st Annual ACM Symposium on Applied Computing (SAC’16), 2016, pp. 293–298.
[3] R. Serrano-Gotarredona, M. Oster, A. Linares-Barranco, R. Paz-Vicente, F. Gomez-Rodriguez, L. Camunas-Mesa, R. Berner, M. Rivas-Perez, T. Delbruck, S. Liu, R. Douglas, P. Hafliger, G. Jimenez-Moreno, A. Civit Ballcels, T. Serrano-Gotarredona, A. J. Acosta-Jimenez, and B. Linares-Barranco, “Caviar: A 45k neuron, 5m synapse, 12g connectic/s ler hardware sensoryprocessing learningagactuating system for high-speed visual object recognition and tracking,” IEEE Transactions on Neural Networks, vol. 20, no. 9, pp. 1417–1438, Sep. 2009.
[4] L. Camunas-Mesa, C. Zamarreno-Ramos, A. Linares-Barranco, A. J. Acosta-Jimenez, T. Serrano-Gotarredona, and B. Linares-Barranco, “An event-driven multi-kernel convolution processor module for event-driven vision sensors,” IEEE Journal of Solid-State Circuits, vol. 47, no. 2, pp. 504–517, 2012.
[5] P. Lichtsteiner, C. Posch, and T. Delbruck, “A 128×128 120 dB 15 µs latency asynchronous temporal contrast vision sensor,” IEEE Journal of Solid-State Circuits, vol. 43, no. 2, pp. 566–576, 2008.
[6] D. Neil and S.-C. Liu, “Miniatur, an event-driven FPGA-based spiking network accelerator,” IEEE Trans on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 12, pp. 2621–2628, 2014.
[7] Y. Cao, Y. Chen, and D. Khosla, “Spiking deep convolutional neural networks for energy-efficient object recognition,” International Journal of Computer Vision, pp. 1–13, 2014.
[8] P. U. Diehl, D. Neil, J. Binas, M. Cook, S.-C. Liu, and M. Pfeiffer, “Fast-classifying, high-accuracy spiking deep networks through weight and threshold balancing,” in International Joint Conference on Neural Networks (IJCNN), 2015, pp. 1–8.
[9] B. Rueckauer, I.-A. Lungu, Y. Hu, M. Pfeiffer, and S.-C. Liu, “Conversion of continuous-valued deep networks to efficient event-driven networks for image classification,” Frontiers in Neuroscience, vol. 11, 2017, https://www.frontiersin.org/article/10.3389/fnins.2017.00682.
[10] J. H. Lee, T. Delbruck, and M. Pfeiffer, “Training deep spiking neural networks using backpropagation,” Frontiers in Neuroscience, vol. 10, 2016.
[11] S. B. Shrestha and G. Orchard, “SLAYER: Spike layer error reassignment in time,” in Advances in Neural Information Processing Systems 31, S. Bengio, H. Wallach, H. Larochelle, K. Grauman, N. Cesa-Bianchi, and R. Garnett, Eds. Curran Associates, Inc., 2018, pp. 1412–1421. [Online]. Available: http://papers.nips.cc/paper/7415-slayer-spike-layer-error-reassignment-in-time.pdf
[12] A. Aimar, H. Mostafa, E. Calabrese, A. Rios-Navarro, R. Tapiador-Morales, I. Lungu, M. B. Milde, F. Corradi, A. Linares-Barranco, S. Liu, and T. Delbruck, “NullHop: A flexible convolutional neural network accelerator based on sparse representations of feature maps,” IEEE Transactions on Neural Networks and Learning Systems, pp. 1–13, 2018.
[13] R. H. Hahnloser, R. Sarpeshkar, M. A. Mahowald, R. J. Douglas, and H. Seung, “Digital selection and analogue amplification coexist in a cortex-inspired silicon circuit,” Nature, vol. 405, no. 6879, p. 947, 2000.
[14] K. Jarrett, K. Kavukcuoglu, M. Ranzato, and Y. LeCun, “What is the best multi-stage architecture for object recognition?” in 2009 IEEE 12th International Conference on Computer Vision, Sep. 2009, pp. 2146–2153. [Online]. Available: http://dx.doi.org/10.1109/ICCV.2009.5459469
[15] V. Nair and G. E. Hinton, “Rectified linear units improve restricted boltzmann machines,” in Proceedings of the 27th international conference on machine learning (ICML-10), 2010, pp. 807–814.
[16] M. B. Milde, D. Neil, A. Aimar, T. Delbruck, and G. Indiveri, “Adaption: Toolbox and benchmark for training convolutional neural networks with reduced numerical precision weights and activation,” arXiv preprint arXiv:1711.04713, 2017.
[17] E. Stromatias, D. Neil, M. Pfeiffer, F. Galluppi, S. B. Furber, and S.-C. Liu, “Robustness of spiking Deep Belief Networks to noise and reduced bit precision weights and activation,” IEEE Transactions on Neural Networks, vol. 24, no. 2, pp. 292–306, 2013.
[18] N. Cesa-Bianchi, and R. Garnett, Eds. Curran Associates, Inc., 2016.
[19] Y. H. Chen, T. Krishna, J. S. Emer, and V. Sze, “Eyriiss: An Energy-Efficient reconfigurable accelerator for deep convolutional neural networks,” IEEE J. Solid-State Circuits, vol. 52, no. 1, pp. 127–138, Jan. 2017. [Online]. Available: http://dx.doi.org/10.1109/JSSC.2016.2616357
[20] B. Moons, D. Bankman, L. Yang, B. Murmann, and M. Verhelst, “BinaryEye: An always-on energy-accuracy-scalable binary CNN processor with all memory on chip in 28nm CMOS,” in 2018 IEEE Custom Integrated Circuits Conference (CICC), 2018, pp. 1–4.
[21] Y.-H. Chen, T. Krishna, J. Emer, and V. Sze, “Eyriiss: An energy-efficient reconfigurable accelerator for deep convolutional neural networks,” in IEEE International Solid-State Circuits Conference, 2016.
[22] D. Shin, J. Lee, J. Lee, and H. Yoo, “14.2 DNPU: An 8.1TOPS/W reconfigurable CNN-RNN processor for general-purpose deep neural networks,” in 2017 IEEE International Solid-State Circuits Conference (ISSCC), Feb 2017, pp. 240–241.

[23] J. Lee, J. Lee, D. Han, J. Lee, G. Park, and H. Yoo, “LNPU: A 25.3 TFLOPS/W sparse deep-neural-network learning processor with fine-grained mixed precision of fp8-fp16,” in 2019 IEEE International Solid-State Circuits Conference - (ISSCC), Feb 2019, pp. 142–144.

[24] J. Lee, C. Kim, S. Kang, D. Shin, S. Kim, and H. Yoo, “UNPU: A 50.6 TOPS/W unified deep neural network accelerator with 1b-to-16b fully-variable weight bit-precision,” in 2018 IEEE International Solid-State Circuits Conference - (ISSCC), Feb 2018, pp. 218–220.

[25] S. Zhang, Z. Du, L. Zhang, H. Lan, S. Liu, L. Li, Q. Guo, T. Chen, and Y. Chen, “Cembricon-X: An accelerator for sparse neural networks,” in 2016 49th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), Oct 2016, pp. 1–12.

[26] Z. Du, R. Fasthuber, T. Chen, P. Jenne, L. Li, T. Luo, X. Feng, Y. Chen, and O. Temam, “ShiDianNao: Shifting vision processing closer to the sensor,” in 2015 ACM/IEEE 42nd Annual International Symposium on Computer Architecture (ISCA), June 2015, pp. 92–104.

[27] P. O’Connor and M. Welling, “Sigma delta quantized networks,” in ICLR, 2017.

[28] L. Cavigelli, P. Degen, and L. Benini, “Chinfier: Change-based inference for convolutional neural networks on video data,” in Proceedings of the 11th International Conference on Distributed Smart Cameras. ACM, 2017, pp. 1–8.

[29] D. Neil, J. Lee, T. Delbrück, and S. Liu, “Delta networks for optimized recurrent network computation,” in Proceedings of the 34th International Conference on Machine Learning ICML 2017, Sydney, NSW, Australia, 6-11 August 2017., 2017, pp. 2584–2593. [Online]. Available: http://proceedings.mlr.press/v70/neil17a.html

[30] C. Gao, D. Neil, E. Ceolini, S.-C. Liu, and T. Delbrück, “DeltaRNN: A power-efficient recurrent neural network accelerator,” in Proceedings of the 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, ser. FPGA ’18, New York, NY, USA, 2018, pp. 21–30. [Online]. Available: http://doi.acm.org/10.1145/3174243.3174261

[31] C. Gao, A. Rios-Navarro, X. Chen, T. Delbruck, and S.-C. Liu, “Edge-DRNN: Enabling low-latency recurrent neural network edge inference,” in IEEE Artificial Intelligence for Circuits and Systems (AICAS), 2019, submitted.

[32] F. Conti, L. Cavigelli, G. Paulin, I. Susmelj, and L. Benini, “Chipmunk: A systolically scalable 0.9 mm², 3.08 Gop/s/mW@ 1.2 mW accelerator for near-sensor recurrent neural network inference,” in 2018 IEEE Custom Integrated Circuits Conference (CICC), 2018, pp. 1–4.

[33] S. Han, J. Kang, H. Mao, Y. Hu, X. Li, Y. Li, D. Xie, H. Luo, S. Yao, Y. Wang et al., “ESE: Efficient speech recognition engine with compressed LSTM on FPGA,” in FPGA 2017, 2017.

[34] S. Wang, Z. Li, C. Ding, B. Yuan, Q. Qiu, Y. Wang, and Y. Liang, “C-LSTM: enabling efficient LSTM using structured compression techniques on FPGAs,” in Proceedings of the 2018 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, 2018, pp. 11–20.

[35] S. Han, X. Liu, H. Mao, J. Pu, A. Pedram, M. A. Horowitz, and W. J. Dally, “EIE: Efficient inference engine on compressed deep neural network,” in 2016 ACM/IEEE 43rd Annual International Symposium on Computer Architecture (ISCA). IEEE, 2016, pp. 243–254.

[36] S. Cao, C. Zhang, Z. Yao, W. Xiao, L. Nie, D. Zhan, Y. Liu, M. Wu, and L. Zhang, “Efficient and effective sparse LSTM on FPGA with bank-balanced sparsity,” in Proceedings of the 2019 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, 2019, pp. 63–72.

[37] A. Ankit, I. E. Hajj, S. R. Chalamalasetti, G. Ndu, M. Foltin, R. S. Williams, P. Faraboschi, W.-m. W. Hwu, J. P. Strachan, K. Roy et al., “Puma: A programmable ultra-efficient memristor-based accelerator for machine learning inference,” in Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems. ACM, 2019, pp. 715–731.