Low-distortion bandpass $\Sigma\Delta$ modulator using two-path double-sampling technique

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Abstract: A low-distortion bandpass (BP) sigma-delta ($\Sigma\Delta$) modulator with double-sampling technique is proposed. The proposed modulator is based on a double-delay switched-capacitor resonator which employs double-sampling technique to relax the requirements for circuits and reduce amplifier power consumption and chip area. The proposed architecture can be applied for other modulators. The full differential circuit using two-path technique is designed with a standard 0.18 µm CMOS technology. The power consumption is 6 mW with 1.8 V supply. The fourth-order single-bit BP modulator achieves a peak SNR (signal-to-noise ratio) of 86.6 dB and DR (dynamic range) of 90 dB with 200 kHz bandwidth centered at 20 MHz which are better than the conventional BP $\Sigma\Delta$ modulator.

Keywords: bandpass, sigma-delta, modulator, double-sampling

Classification: Integrated circuits

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1 Introduction

Broadband low power $\Sigma\Delta$ analog-to-digital (A/D) converters are becoming popular in wireless communication systems, high definition television and other applications [1], and for narrowband intermediate frequency wireless communication systems, BP $\Sigma\Delta$ modulator is an optimum approach for high resolution A/D conversion [2]. Most of previous works are focusing on the conventional architecture, while the low-distortion BP modulator has the potential to achieve better performance. Because the ideal distortion BP modulator utilizing a feedforward signal path which makes resonator only process the quantization noise has the potential to get better linearity specialties and is much less sensitive to resonator nonlinearity than the conventional one. Low-distortion architecture of BP $\Sigma\Delta$ modulator is firstly presented in [3], and a low-distortion fourth-order BP $\Sigma\Delta$ modulator circuit is implemented in [4]. However, the circuit in [4] needs two operational amplifiers (opamp) to realize the two delay cells and four for the two resonators, so the power dissipation is more than 60 mW at a 3.3 V power supply. In addition, the double-sampling technique doubles the oversampling ratio (OSR) effectively without increasing the clock frequency which relaxes the amplifier settling time [5]. The double-sampling technique is widely used in the low-pass $\Sigma\Delta$ modulator and conventional architecture of BP modulator, but not for the low-distortion architecture because the lack of available resonator [6, 7]. In this paper, a double-delay and double-sampling switched-capacitor resonator is presented which is suitable for the design of double-sampling low-distortion BP modulator. Based on the proposed double-delay and double-sampling resonator, a novel low-distortion fourth-order BP $\Sigma\Delta$ modulator circuit is given. The proposed full differential low-distortion BP modulator with double-sampling technique is absorbing in DR and power consumption which is suitable for low power A/D application.

2 Proposed architecture

Fig. 1 is the proposed fourth-order BP $\Sigma\Delta$ modulator where $f_1$ and $f_2$ are scaling coefficients, $f_3$, $f_4$ and $f_5$ are summation coefficients. The two paths work alternately at different clock phase (clk1, clk2) to reduce the sampling frequency for half without changing the equivalent sampling frequency, thus the settling requirement for the resonator is less strict.

The transfer functions of the signal and quantization noise in Fig. 1 are as follows:
The optimum set of coefficients is $f_1 = 0.5$, $f_2 = 1/3$, $f_3 = 0.3$, $f_4 = 0.4$, $f_5 = 0.3$, then the STF $(z)$ is not equal to unity any more as in [3]. Although it reduces the linearity of the modulator, the output swing of resonator is scaled down without increasing the capacitive loading which relaxes the requirements for the amplifier [8]. The fourth-order single-bit modulator is simulated using Simulink and the resonator output histograms are shown in Fig. 2. It is obvious that the proposed modulator achieves a much smaller resonator output swing than the conventional architecture and the low-distortion one presented in [3].

### 3 Circuit design and results

Fig. 3 presents the schematic diagram of the double-delay and double-sampling resonator which employs double-sampling technique and Fig. 4 shows the operational amplifier (opamp) circuit. During different phases, input signal is sampled by capacitor pairs $C_{sm}$ and $C_{sp}$, and the sampled input voltage is transferred to integrator capacitor pairs $C_{fm}$ and $C_{fp}$ after half a period. The scaling coefficients $f_1$ and $f_2$ in Fig. 1 are obtained by the ratio of
Cs and Cf, and it is insensitive to component variances. The output swing of the resonator can be scaled down without increasing the capacitive loading of the amplifier, so the voltage scaling technique makes it suitable for low power design.

The working process of resonator can be expressed as follows:

\[
\begin{align*}
V_{O+}(n-4)C_{fp1} &= V_{O-}(n-6)C_{fp1} + V_{I-}(n-6)C_{sm3} \\
V_{O+}(n-3)C_{fp2} &= V_{O-}(n-5)C_{fp2} + V_{I-}(n-5)C_{sm4} \\
V_{O+}(n-2)C_{fm1} &= V_{O-}(n-4)C_{fm1} + V_{I-}(n-4)C_{sm1} \\
V_{O+}(n-1)C_{fm2} &= V_{O-}(n-3)C_{fm2} + V_{I-}(n-3)C_{sm2}
\end{align*}
\]

(3)

Assuming \( C_{sm} = C_{sp} = C_s, C_{fm} = C_{fp} = C_f \), the transfer function is described as:

\[
H(z) = - \frac{C_s}{C_f} \frac{z^{-2}}{1 + z^{-2}}
\]

(4)

The sampling capacitance value depends on the SNR which is limited by the \( kT/C \) noise of the first resonator. To obtain a 14-bit BP modulator, the sampling capacitance value should satisfy:

\[
\frac{KT}{C_{s1} \times OSR} < \left( \frac{V_{pp}}{2^{N+1}} \right)^2
\]

(5)

where \( K = 1.38 \times 10^{-23} \text{J/K}, V_{pp} = 0.3 \text{V}, N = 14, OSR = 200, T = 300 \text{K} \), and the load of opamp should be as small as possible to reduce the power.
dissipation, then $C_{s1} = 0.8 \text{ pF}$. The sampling capacitance value of the second resonator is $0.2 \text{ pF}$.

Double-sampling technique is an effective method to relax the requirements for amplifier on the settling time, DC gain and bandwidth, therefore the requirement for the opamp is less strict. The opamp of the first resonator achieves an 85 dB DC gain with 226 MHz bandwidth for a 2 pF capacitor load, and the phase margin is 64°. The common mode input range is 0.1 V~1.5 V and the power dissipation is 2.8 mW at a 1.8 V supply. Fig. 5 shows the simulation result of the equivalent input noise, which presents 12.29 nV/sqrt(Hz) at 20 MHz. The opamp of the second resonator is less strict in load, bandwidth and DC gain, so the power dissipation is scaled down.

![Fig. 5. Simulation result of the opamp noise](image)

The proposed architecture of BP $\Sigma\Delta$ circuit is designed using a standard 0.18 $\mu$m CMOS technology and the full differential circuit principle is presented in Fig. 6. The two-path working mode is controlled by non-overlap clocks clk1 and clk2, and the two-path digital output sequences are rolled into one by the selector. The second resonator is relatively less critical than the first resonator. Therefore, the current and performance are scaled down to further reduce power consumption [9].

![Fig. 6. Proposed two-path fourth-order $\Sigma\Delta$ BP modulator circuit](image)
The BP modulator works at an equivalent sampling frequency of 80 MHz, and the maximum input signal is $-0.3$ dBFS centered at 20 MHz. The digital output sequences are calculated to get the PSD for the proposed fourth-order BP modulator shown in Fig. 7(a). The detail near the centre frequency is also presented. Fig. 7(b) shows the SNR against input signal amplitude for the proposed BP modulator. The performances comparison is listed in Table I in a fundamental FOM [10]. The proposed fourth-order $\Sigma\Delta$ BP modulator circuit achieves a better performance than other typical works.

![PSD for the proposed BP modulator](image1)

![Relation between input signal and SNR](image2)

**Fig. 7.** (a) PSD for the proposed BP modulator, (b) Relation between input signal and SNR

**Table I.** Performance comparison

| Reference | Power (mW) | Bandwidth (MHz) | FS (MHz) | DR (dB) | Peak SNR (dB) | \( FOM = \frac{4kT \times DR \times BW}{P} \times 10^{12} \) |
|-----------|------------|----------------|---------|---------|---------------|-------------------------------------------------|
| 2         | 11         | 0.2            | 42.8    | 82      | 80.14         | 24.69                                           |
| 7         | 13.5       | 0.27           | 80      | 85      | 82            | 28.15                                           |
| 11        | 56         | 0.27           | 80      | 84      | 80            | 6.71                                            |
| 12        | 27         | 0.2            | 80      | 87      | 85.5          | 10.67                                           |
| This work | 6          | 0.2            | 80      | 90      | 86.6          | 49.68                                           |

4 Conclusions

A high performance bandpass sigma-delta modulator is proposed. By employing double-sampling technique to relax the requirements for circuits, the proposed two-path architecture is advantageous in realizing a larger DR and lower power consumption than the conventional bandpass sigma-delta modulator. The proposed modulator is available for other low power applications.

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