The Core Diffusion-Drift Field-Effect Transistor Theory Including Quantum and Interface Trap Capacitances

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Abstract — We have decomposed the modeling of the field-effect transistors into the two independent parts: the current continuity based kinetics and the charge neutrality based electrostatics. The former part, that is universal for all FETs, leads to an explicit and closed form of I-V characteristics as a function of the total channel charge. The latter part, which is specific for a particular material and geometric configurations can be considered as an independent engineering task. The quantum capacitance and the interface trap density are consistently incorporated into the solution of the current continuity equation in the diffusion-drift approximation, providing a complete consistency in the current and the capacitance small-signal characteristics.

Index Terms— Field-effect transistor, MOSFET model, diffusion-drift, quantum capacitance, interface traps.

I. INTRODUCTION

The demands of advanced chip design in microelectronics is pushing the industry to develop new compact MOSFET models for design of advanced chip architectures [1]. A comparative analysis of different approaches to the MOSFET compact modeling was given in [2]. It is well-known the channel current in the field-effect transistors has in principle a diffusion-drift form due to fundamental non-uniformity of the charge distribution along the channel [3]. Despite this fact, most of the compact MOSFET models based anyway on a formal integration of the drift-like dependence \( I_D = GdV/dx \) [4, 5], where \( G \) is the channel conductance formally depending on the gate \( V_G \) and the drain \( V_D \) biases. This inconsistency leads often to a piecewise description of transistor operation in different modes, which is artificially corrected by formal interpolation procedures. We pointed in [6], that a consistent description of I-V characteristics in nonlinear electronic devices can be constructed on only the joint solution of the Poisson and current continuity equations. We argued that such theory, relying only upon the general principles of current continuity and electric neutrality along the channel (used instead of the exact solution of Poisson’s equation), is universal and can be used for any configurations of the field-effect transistors (FETs). A particular form of device geometry and material equations has to enter the theory only through the total node capacitances and through a dependence of the total channel charge \( Q_C \) on the external node biases. This point is very important since a use of the areal capacitance and the local charge density variables in the deeply scaled devices is problematic because of the fringing effects and non-uniformities in nanoscale devices. We consider a calculation of the full channel charge \( Q_C \) as a separate technical task, specific for different FETs. A particular form of \( Q_C (V_C) \) should be determined from electrostatic consideration, which is different for the different device configurations (bulk or SOI FETs, FinFETs, double gate FETs, etc.). The fundamental quantum capacitance and the parasitic interface trap capacitance should be consistently implemented into the structure of the core model.

We describe in this paper an advanced version of the diffusion-drift model [6] meeting these requirements and formulated in a general, consistent and physically transparent form.

II. DIFFUSION-DRIFT THEORY

A. Diffusion to drift current ratio

The diffusion-drift nature of the channel current implies a use of the electrochemical potential notion. The full diffusion-drift current is determined by the gradient of electrochemical potential \( \mu = \zeta - q\phi \)

\[
J = j_{diff} + j_{drift} = -\mu_n n_c \frac{d\mu}{dx} = -q\mu_n n_c \frac{d\phi}{dx} \left( 1 - \frac{d\zeta}{qd\phi} \right) = q\mu_n n_c E (1 + \kappa),
\]

where \( \mu_n \) is the carrier’s mobility, \( n_c \) is the channel electron density, \( E = -d\phi/dx \) is a lateral electric field. As shown in Ref. [6], the diffusion to the drift current ratio \( \kappa \) can be derived from the electric neutrality requirement along the channel of MOS structure in the gradual channel approximation

\[
\kappa = J_{diff} = -\left( \frac{\partial \zeta}{q\partial \phi} \right)_{V_c} = \frac{\left( \partial V_G / \partial \phi \right)_{V_c}}{q \left( \partial V_G / \partial \zeta \right)_{\phi}} = \frac{C_{ox} + C_D}{C_Q + C_T}, \tag{2}
\]

where \( C_{ox}, C_D, C_T \) are the total oxide (geometrical) capacitance, the total depletion layer and the interface trap capacitances, respectively. For convenience, we will denote the total charges and capacitances by the indices with the capital
letters. Notice, that only $C_{ox}$ and $C_{q}$ play a fundamental role in the field-effect device operation principle, whereas the interface trap and the depletion layer effects could be eliminated or minimized for ideal, or some particular device configurations.

The total inversion layer capacitance (referred often as a quantum capacitance [7]) $C_{q} = qdQ_{co}/d\zeta$ is closely related with the diffusion potential which is defined as a fundamental parameter of the generalized Einstein relation

$$\varphi_d = \frac{Q_{co}}{qdQ_{co}/d\zeta} = \frac{Q_{co}}{C_{q}} = \frac{D_0}{\mu_0},$$

where $D_0$ is the electron diffusivity, $Q_{co}$ is the total “equilibrium” channel charge at zero drain bias, which will be considered below as a known function of gate voltage. As well as the channel charge $Q_{co}$, the quantum capacitance $C_{q}$ varies over a very wide range, while the diffusion potential $\varphi_d$ varies only from the thermal potential $\varphi_t = k_BT/q$ in the subthreshold region to a few $\varphi_t$ (of order the Fermi energy) in the strong inversion.

The quantum capacitance is usually ignored in the MOSFET modeling. Actually, the quantum capacitance $C_{q}$ is very low in the subthreshold operation mode ($C_{q} << C_{ox}, C_{tr}, C_{pd}$) and extremely high in the strong inversion region ($C_{q} >> C_{ox}, C_{tr}, C_{pd}$). In the former case, $C_{q}$ is masked by the parasitic interface trap and the depletion layer capacitances. In the latter case, $C_{q}$ is typically insignificant in the silicon FETs (in contrast to graphene FETs) due to the series connection with the geometrical capacitance $C_{ox}$ (see, the inset in Fig. 1). Nevertheless, we will see below that the quantum capacitance is a key concept in the construction of the consistent MOSFET theory.

### B. I-V characteristics from the continuity equation solution

The key point of the original approach [6] is an explicit analytical solution of the continuity equation for the channel current density. The total diffusion-drift drain current $J_s = J_{dr} + J_{diff} \equiv (1+\kappa)J_{dr}$ has to be conserved along the channel in a quasi-static approximation. Assuming that the carrier’s mobility and $\kappa$ are coordinate-independent along the channel, we have the continuity equation in a form

$$-\frac{d}{dx}(n_c \frac{d\mu}{dx}) = (1+\kappa)\frac{d}{dx}(n_c E) = 0,$$

that yields the equation for the electric field distribution along the channel

$$\frac{dE}{dx} = \frac{\kappa}{\varphi_d} E^2.$$

Notice that this equation and electric field $E(x)$ have nothing to do with the built-in electric fields in generally non-uniform channels that can be calculated as a result of the Poisson’s equation even for zero drain-source bias. A direct solution of the ordinary differential equation Eq. 5 yields

$$E(x) = \frac{E(0)}{1-\kappa E(0)/\varphi_d},$$

where $E(0)$ is the electric field near the source, which should be determined from the condition imposed by a fixed source-drain electrochemical potential difference $V_d$

$$V_d = \int_0^L \left[ -\frac{d\mu(x)}{qdx} \right] dx = (1+\kappa)\int_0^L E(x) dx,$$

where $L$ is the channel length.

Based on (6) and (7), the explicit expression for $E(0)$ and electrochemical potential difference along the channel can be derived

$$\mu(x) - \mu(0) = \varphi_d (1+\kappa) \ln \left[ 1 - \frac{k_BT}{\varphi_d} \right].$$

Here, $\mu(0)$ the electrochemical potential (quasi-Fermi level) near the source ($\mu(L) - \mu(0) = qV_{ds}$), controlled by the gate-source bias $V_{gs}$. The chemical potential $\zeta$ and the electron density distributions along the channel can be also inferred in this way. According to a general rule, the total diffusion-drift drain current can be calculated as a gradient of the electrochemical potential taken in a suitable point, e.g., in the vicinity of the source [8]

$$I_D = -W\mu_0 n_c (0) \left[ \frac{d\mu}{dx} \right]_{x=0} = \frac{\mu_0 Q_{co}}{L} \left[ \frac{d\mu}{dx} \right]_{x=0}.$$

where $W$ is the FET width, $n_c(0)$ ($Q_{co} = qn_c(0)WL$) is electron density near the source.

Thus, the MOSFET drain current $I_D$ can be figured out in a closed explicit form as follows

$$I_D = \frac{D_0 Q_{co}}{L^2} \frac{1+\kappa}{\kappa} \left[ 1 - \exp \left( \frac{-\kappa}{1+\kappa} V_{ds} \right) \right].$$

Defining the electrostatic saturation drain bias as $V_{dsat} \equiv 2\varphi_d (1+\kappa)/\kappa$, we have

$$I_D = \frac{1}{2} G_s V_{dsat} \left[ 1 - \exp \left( -2 V_{ds} \right) \right].$$

where the channel conductance in the linear region is defined as follows

$$G_s \equiv \mu Q_{co}/L^2.$$

In view of (2) and (3), the direct calculation yields

$$V_{dsat} = 2\varphi_d \left[ 1 + \frac{C_{tr}}{C_{ox} + C_{d}} + \frac{2Q_c}{C_{ox} + C_{d}} \right].$$

We took into account in (13) that the electrostatic saturation regime corresponds to a non-uniform charge distribution in the channel. In contrast to $Q_{co}$, the total “nonequilibrium” channel charge $Q_c = Q_c(V_{gs},V_d)$ should also depend on the drain-source bias.
The formula (14) yields a convenient approximation for the self-consistent calculation of $Q_c(V_g,V_D)$ provided $Q_{co}$ is known

$$Q_c(V_g,V_D) = \frac{Q_{co}}{2} \left( 1 + \exp \left( -\frac{k V_D}{1 + \kappa \varphi_D} \right) \right) \approx \frac{Q_{co}}{2} \left( 1 + \exp \left( -\frac{(C_{ox} + C_D)V_D}{Q_{co}} \right) \right).$$

Note, that $Q_c(V_g,V_D=0) = Q_{co}$, $Q_c(V_g,V_D > V_{dsat}) \approx Q_{co}/2$, and $V_{dsat} \approx Q_{co}/(C_{ox} + C_D)$ in strong inversion. Thus, the equations (11-14) represent a closed, consistent and explicit analytical computational scheme for evaluation of the drain current as a function of $Q_{co}$.

It is notable that I-V characteristics of the field-effect transistors can be equivalently and self-consistently rewritten in an intuitively clear and concise form

$$I_D = \frac{Q_c}{\tau_{tr}},$$

where the transit time is defined as

$$\tau_{tr} = \frac{L^2}{\mu_V V_{dsat}} \coth \left( \frac{V_D}{V_{dsat}} \right).$$

The same relation for the transit time can be consistently obtained in the following way [9]

$$\tau_{tr} = \int_{0}^{L} \frac{dx}{\mu_V (1 + \kappa) E(x)},$$

where the lateral electric field in the channel $E(x)$ is an accurate solution of Eq.(5).

### III. APPLICATIONS

#### A. Inverse logarithmic slope and transconductance

Another important small-signal characteristics of the field-effect devices is the inverse logarithmic slope $S = I_D (dV_G/dI_D)$, which is a measure of the gate control over drain current, relating with the transconductance $g_m = dI_D/dV_G$ as follows

$$S = I_D (dV_G/dI_D) = I_D / g_m.$$  \hspace{1cm} (18)

This relation makes $S$ an extremely important parameter in the well-known $g_m/I_D$ sizing methodology in the analog CMOS circuits [10]. Fig. 1 illustrates the interrelation between $g_m$ and $S$ in (18) in a lucid graphic form.

Provided a weak dependence of the carrier’s mobility on gate voltage $V_G$, the logarithmic slope can be calculated as a function of the gate bias over many decades of drain current in the following way

$$S = Q_c \frac{dV_G}{dQ_c} = \varphi_D \left( 1 + \frac{C_D + C_T + C_G}{C_{ox}} \right) = \varphi_D \left( 1 + \frac{C_D + C_T}{C_{ox}} \right) + \frac{Q_c}{C_{ox}} \approx m \varphi_D + \frac{Q_c}{C_{ox}},$$

where $m$ is often referred to as an ideality factor. It corresponds to the well-known subthreshold slope measured in Volts per decade of the gate voltage

$$S_S = S \ln 10 \approx \varphi_T \ln 10 \left[ 1 + \left( C_D + C_{IT} \right) / C_{ox} \right] = m \varphi_T \ln 10.$$  \hspace{1cm} (20)

The inverse slope above the threshold is estimated as

$$S \equiv (V_G - V_T) / n \cdot (V_T \text{ is the threshold voltage), where } n = 1 \text{ in the linear regime and } n = 2 \text{ in the saturation}. \hspace{1cm} (19)$$

![Transfer I-V](image)

Fig. 1. Field-effect transistor transfer characteristics and graphical representation of the transconductance $g_m$ and the inverse logarithmic slope $S$.

Thus defined logarithmic slope describes in a unified way both the strong inversion and the weak inversion regions.

In contrast to the extensive transconductance (i.e., dependent on $W/L$), the inverse logarithmic slope $S$ (as well as $V_{dsat}$) is a thermodynamically intensive variable, i.e., independent of the channel size and shape. Comparing $V_{dsat}$ (13) and $S$ (19), one gets

$$V_{dsat} = \frac{2S}{1 + \eta},$$

where $\eta = C_D/C_{ox}$ is the substrate factor. In the strong inversion we have $V_{dsat} \equiv (V_G - V_T) / (1 + \eta)$. Then, the I-V characteristics becomes

$$I_D = \frac{G_m S}{1 + \eta} \left( 1 - \exp \left( -\frac{V_D}{S} (1 + \eta) \right) \right).$$

Taking into account (18), one obtains

$$g_m = \frac{G_m}{1 + \eta} \left( 1 - \exp \left( -\frac{V_D}{S} (1 + \eta) \right) \right) = \frac{2I_D}{(1 + \eta) V_{dsat}}.$$  \hspace{1cm} (23)

Another compact form of I-V characteristics

$$I_D = g_m \left( m \varphi_D + \frac{Q_c}{C_{ox}} \right).$$

$$\text{(24)}$$
B. Subthreshold current

The MOSFET drain current (22) in the subthreshold region \( (V_G < V_T, \ S \equiv m \phi_T) \) becomes

\[
I_D^{\text{sub}} = \frac{m \cdot D_Q}{1 + \eta} \cdot \frac{D_Q}{2L} \left[ 1 - \exp \left( -\frac{V_T}{m \phi_T} (1 + \eta) \right) \right] \equiv \frac{m \cdot D_Q}{1 + \eta} \cdot \frac{D_Q}{2L} \left( 1 - e^{-\frac{V_T}{m \phi_T} (1 + \eta)} \right), \quad (25)
\]

where \( Q_T \equiv C_D \phi_T \) is the channel charge at the threshold voltage.

C. Gate capacitance and channel capacitance

The low-frequency gate capacitance can be defined as a derivative of the total gate charge with respect to the gate voltage

\[
C_G = \left( \frac{\partial Q_G}{\partial V_G} \right) \equiv \frac{C_G + C_D + C_T}{C_G + C_D + C_T} \frac{C_G}{C_G + C_D + C_T} = \frac{1}{C_G + C_D + C_T} \left( 1 + \frac{C_D}{C_G} \right) \quad (26)
\]

We define the channel capacitance as follows [11]

\[
C_{CH} = \left( \frac{\partial Q_c}{\partial V_G} \right) \equiv \frac{C_G + C_D + C_T}{C_G + C_D + C_T} \frac{C_G}{C_G + C_D + C_T} = \frac{C_G}{1 + \kappa_{CH}} \left( 1 + \frac{C_D}{C_G + C_T} \right).
\]

Equation one can get the useful relations

\[
C_{CH} = \frac{C_G}{1 + \kappa_{CH}} = \frac{Q_C}{\phi_T \cdot m \cdot C_G + Q_C / C_{CH}}, \quad (28)
\]

\[
Q_C = \frac{C_{CH} V_{DSAT}}{2} \quad (29)
\]

In view of (26) and (27), the gate and the channel capacitances are related with each other

\[
C_G = \frac{C_G + C_D + C_T}{C_G + C_D + C_T} \frac{C_G}{C_G + C_D + C_T} = 1 + \frac{C_D}{C_G}. \quad (30)
\]

As can be seen directly from (30), the interface traps and depletion layer impair the gate control over the channel charge.

D. Transit time and field effect mobility

The transit time (see, equations (15-17)) can be expressed as a function of the channel capacitance and transconductance

\[
\tau_{TT} = \frac{Q_C}{g_m S} = \frac{C_{CH}}{g_m} \quad (31)
\]

Note that all variables are assumed to be non-linear functions of \( V_G \) and \( V_D \). The low-field transconductance \( g_m \) is closely related with the field-effect mobility \( \mu_{FE} \)

\[
g_m = \left( \frac{\partial I_D}{\partial V_G} \right)_{\gamma_G \to 0} = \frac{\mu_{CH} V_D}{g_{m2}} = \frac{\mu_{FE} C_{CH} V_D}{g_{m2}}. \quad (32)
\]

Then, using an operational definition of \( \mu_{FE} \) we get an explicit dependence of \( \mu_{FE} \) on the microscopic mobility \( \mu_0 \) and the small-signal capacitances

\[
\mu_{FE} \equiv \frac{g_{m2} L^2}{C_{ox} V_D} = \frac{g_m C_{CH}}{C_{ox}} = \frac{\mu_0}{1 + \frac{C_D + C_T}{C_G}}. \quad (33)
\]

The transit time in the linear regime is dependent only on microscopic mobility, and not on parasitic capacitances

\[
\tau_{TT} = \frac{C_{CH}}{g_m} \quad \frac{L^2}{\mu_{FE} V_D} C_{ox} = \frac{L^2}{\mu_{FE} V_D} \mu_{FE} V_D. \quad (34)
\]

E. Delay time and cut-off frequency in digital and analog circuits

The extrinsic cut-off frequency \( \omega_T \) in analog circuits is essentially determined by an external load capacitance \( C_L \) and parasitic interface trap and deletion layer capacitances

\[
\omega_T = \frac{g_m}{C_{CH} C_{CH} C_G + C_L} = \frac{1}{\tau_{TT} 1 + \frac{C_D}{C_G} + C_T + C_L} = \frac{1}{\tau_{TT} 1 + \frac{C_D}{C_G} + C_T + C_L} \frac{\phi_D}{\phi_D} = \frac{\tau_{TT} + \frac{C_D}{C_G} + C_T + C_L}{I_D} \phi_D. \quad (35)
\]

This expression is very similar to the extrinsic cutoff frequency for bipolar transistors [12].

Further, the node delay time metrics in digital circuits can be defined as follows [13]

\[
\tau_D = \frac{(C_L + C_G) V_{DD}}{I_{IN}}. \quad (37)
\]

where \( C_L \) is the load capacitance. Then, it could be estimated accurately

\[
\tau_D = \frac{g_m S}{\tau_{TT} C_{CH}} = \frac{C_L + C_G V_{DD}}{S} = \frac{\tau_{TT} + C_D + C_T + C_L}{I_{IN}} \frac{V_{DD}}{S}. \quad (38)
\]

Thus, the extrinsic delay time composed of intrinsic delay, intrinsic parasitic delay and the extrinsic parasitic delay.

This point shows a complete consistency in the description of the current and capacitance parameters in the context of our approach, which is impossible without a use of explicit quantum capacitance consideration.
We have developed a physical approach for construction of I-V characteristics in the field-effect transistors based on a consistent solution of continuity equation in diffusion-drift approximation. It was first shown that the quantum capacitance has to be an integral part of the FET theory that allows a continuous and consistent description of I-V characteristics. The fundamental channel quantum capacitance and parasitic interface trap density spectrum have been accurately and consistently implemented into the model structure.

The simulated FET I-V characteristics were shown can be represented accurately in different equivalent forms as functions of observable differential and large-signal parameters.

A key point is that the total channel charge is considered as a basic variable. This allows considering the geometric short-channel effects as a separate engineering task, bound by electrostatics of the specific device configuration.

Another crucial short-channel effect, the carrier velocity saturation, requires generally an accurate solution of the current continuity equation. The problem is the dependence of the drift velocity on the channel electric filed is generally unknown and often approximated phenomenologically in an inconvenient piecewise form [14]. This makes the exact analytical solution of the continuity equation meaningless since the choice of the mobility dependence approximation $\mu_c(E)$ strongly affects the functional form of the continuity equation solution [15]. An alternative phenomenological approach was proposed in [8, 16] where the electrostatic saturation voltage $V_{DSAT}$ in a basic equation (11) is replaced by a generalized saturation voltage $V_{SAT}$, defined as

$$V_{SAT} = \frac{2V_{max}}{\mu_c} \tanh \left( \frac{\mu_c V_{DSAT}}{2V_{max}L} \right),$$

(39)

that corresponds to $I_{DSAT} \equiv (1/2)G_0V_{DSAT} \propto (V_D - V_T)^2$ for the long-channel devices (square-law approximation), and the saturation current for the short channels $I_{DSAT} \equiv (1/2)G_0V_{SAT} \equiv \frac{V_{max}Q_G}{L}$ is determined by the maximum drift velocity $V_{max}$ of the channel carriers. This approach was validated on the extensive experimental data (see, e.g., [17]).

We believe that being based on the fairly general physical principles, the described approach can be the basis for the development of the universal compact models of the field-effect transistors of different types.

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