X Band Fin Resonant Body Transistors in 14nm CMOS Technology

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Abstract

Here we present the first demonstration and in-depth study of unreleased acoustic resonators in 14nm FinFET technology in the IEEE X band, which offer a zero-barrier-to-entry solution for high Q, small footprint, resonant tanks integrated seamlessly in advanced CMOS nodes. These devices leverage phononic waveguides for acoustic confinement, and exploit MOS capacitors and transistors inherent to the technology to electromechanically drive and sense acoustic vibrations. Sixteen device variations are analyzed across thirty bias points to discern the impact of phononic confinement, gate length, and termination scheme on resonator properties. The limiting factor in FinFET resonator performance among design variations tested is shown to be Back End of Line (BEOL) confinement, with devices with acoustic waveguides incorporating Mx and Cx metal layers exhibiting 2.2x higher average quality factor (Q) and peak amplitude, with maximum Q increasing from 115 to 181 and maximum amplitude scaling from 0.8 to 4.5 µS. A detailed analysis of biasing in the highest performing device shows good fit with a derived model, which addresses the velocity saturated piezoresistive effect for the first time in active resonant transistors. Peak differential transconductance that is dominated by changes in the silicon band-structure, as expected from an analysis that includes contributions from the piezoresistive effect, electrostatic modulation, and silicon bandgap modulation.

As demand for wireless services grows, so too does the demand for higher frequency radio communication where bandwidth is more plentiful. With 5G FR2 bands extending beyond 10 GHz and FR1 intra-band congestion growing, novel solutions are required to enable high performance, adaptable radios. As a key element of both the filters and voltage controlled oscillators used in radios, high frequency resonators represent an active area of research, with recent developments including thin film bulk acoustic resonators with novel ferroelectric materials, as well as high frequency Lamb and Lamé wave resonators using piezoelectric lithium niobate or aluminum nitride thin films [1–4]. To address band congestion, multiple-input-multiple-output (MIMO) arrays are becoming increasingly common as a way to multiplex transmissions between users in the same band, with large arrays allowing for increased performance across end-users sharing spectrum [5].

The beam-forming enabled by such an antenna array is particularly promising for higher frequency bands, where propagation conditions are less stable due to increased RF absorption. These RF front-ends of increasing complexity require many more analog components to be integrated in a compact form factor, leading to active research in RF integration into traditional digital processes. Many high performance technologies require integration in MEMS-first or MEMS-last process schemes [6,8], which provides space and power savings over off-chip RF integration. The use of phononic crystal confinement, however, opens the door for resonator integration directly into a standard CMOS process, potentially enabling larger MIMO arrays in a smaller footprint at lower power [9,10]. In addition to reducing parasitics from routing high frequency signals over long distances, this also provides the opportunity to use high performance transistors for active transduction, achieving potentially record-breaking performance [11]. Such an approach also opens the door for acoustic coupling between devices co-located on the same chip, reducing the need for power hungry phase locked loops and opening the door for exploration of highly scaled coupled oscillator systems for neuromorphic computing [12,13]. This paper continues the evolution of such technology by introducing the first CMOS FinFET-based resonators utilizing acoustic waveguiding confinement operating in the IEEE X band (8-12 GHz).

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1 Resonator Design

The designed resonator structure, shown in Fig. 1, is fully integrated in the GlobalFoundries 14LPP process and occupies a space of 9 µm x 15 µm [15]. The device is a four port network, with output of the resonator taken as the differential transconductance (Eq. 1), which is a function of three main items: the electrical to acoustic transduction efficiency in the drive transistors, the acoustic energy confinement and amplification in the resonance cavity, and the acoustic to drain current conversion in the output transistors. The first of these items, drive transduction, is electrostatic due to the 14 nm fabrication process used, although the potential for future piezoelectric drive using CMOS compatible thin film ferroelectrics exists [2,16,17]. The third of these, acoustic-to-drain current conversion, is also largely a function of the process and materials used in device fabrication. While this conversion will be examined utilizing a simplified model, the initial device design is focused on maximizing acoustic energy confinement by varying gate length, termination scheme, and back-end-of-line (BEOL) confinement conditions.

\[ g_{md} = \frac{i_d}{v_d} = Y_{dd21} - Y_{dd12} \]  

1.1 BEOL Phononic Confinement

Fig. 1(c) depicts a 3D unit cell of the resonator with a 14 nm wide FinFET at the front-end-of-line (FEOL) and periodically arranged metal blocks at the BEOL, categorized into Mx and Cx layers as shown based on thickness and minimum lateral feature sizes. The target resonant mode for the unreleased resonator is along the length direction of the fin transistors. To obtain lower insertion loss and higher quality factor, the radiated acoustic energy needs to be concentrated at the MOS capacitor drive transducers and the sensing transistors. Compared to more traditional suspended resonators, this represents a challenge in the unreleased resonant body transistor design in the commercial CMOS processes.

Integrating a phononic crystal (PnC) at the BEOL of the standard CMOS process and leveraging the mechanical bandgaps of such structures has proven to be an effective tool to confine the energy and boost resonance quality factor [2,10]. As shown by M1 in Fig. 1(b), these periodic metals are uniform along the length (y direction) of the transistor gates (orthogonal to the fin direction) within the resonant cavity.

In order to study and optimize the bandgap induced by the phononic crystals, several 2D simulations were performed in COMSOL Multiphysics. Specifically, by mapping the real coordinates to reciprocal coordinates and searching for the eigenmodes along the first irreducible Brillouin zone in the 2D reciprocal lattice, a 130 nm by 60 nm PnC (such as can be designed within the constraints of the Mx layers in the 14 nm process) yields a calculated bandgap from 8 GHz to 12 GHz (shown in Fig. 7(b)). To further confine the elastic energy, a separate PnC designed under Cx metal layer design rules is also considered for a subset of devices. The corresponding dispersion relationship is shown in Fig. 7(c). A mechanical bandgap is then obtained between 7.6 GHz and 10.7 GHz which overlaps with the bandgap induced by the Mx metal PnC. Together, these PnC designs indicate elastic waves with a frequency of 8 GHz to 12 GHz can be prohibited from propagating into the BEOL. If coupled with a waveguided mode with differential drive that exhibits a large momentum \( k_x = \pi/a \) at a frequency below the sound cone for the bulk silicon substrate, these modes can be confined laterally towards the driving/sensing transistors, with modes from 8 to 10.7 GHz showing the greatest confinement [10]. For an in-depth analysis on the acoustic modes in this device, readers are referred to [18].

1.2 Resonant Cavity Termination

While the PnCs in the main resonant cavity enhance energy confinement and wave reflection from the BEOL, there also exists wave scattering at the two ends of the resonator. Reducing this scattering further increases the horizontal confinement, reduces the insertion loss, and hence increases the Q. The adiabatic theorem in photonic waveguide design is leveraged here, which states that when the wave is propagated down the waveguide, scattering will vanish because of the limitation of sufficiently slow perturbation [19]. Therefore, the key to reduce this scattering is to introduce different units as terminations at the two ends for slower transitions. The unit cell for all the PnC structures in the major termination section throughout the paper is kept as 150 nm x 60 nm.
Figure 1: (a) Cross-section of one period of the FinFET resonator, modeled in COMSOL, with inset highlighting Si fin (dark green) and epitaxial raised source and drain with silicide (blue) [14]. Metal and contact layers highlighted in orange and dark gray and dielectric layers left uncolored (light gray). The target mode is defined primarily along the x-direction via the 180 degree phase constraint due to differential drive and sense. (b) Top down view of device shows the central sense transistors with five pairs of capacitors on either side allowing for differential drive, capped on either end by termination (ten gates in the actual devices, abbreviated to three in the figure) and surrounded by a ground ring. First level metal M1 is used for routing within the structure while higher level metals in Mx and Cx (not shown for clarity in this diagram) rest above this routing in either continuous plate or PnC form. The Kx layer represents higher level metal layers used for device to pad routing. (c) Resonator electrical test scheme with DC biasing provided by standalone SMUs, routed through internal PNA bias tees.
While all measured devices have ten terminating gates at each end of the cavity, two types of cavity termination spacings are explored to provide acoustic confinement in the lateral direction. These include abrupt and gradual termination schemes. The abrupt termination refers to the scenario where a terminating periodic array with constant pitch shifted from that of the resonance cavity array is immediately adjacent to the main resonance region. In this case, the gate length of the termination immediately transitions to the $L_{term}$ value given in Fig. 2(a) and stays constant until the end of the device. As such, the guided waves are abruptly transitioned from the main cavity towards the ends. In the gradual termination scenario, the main resonant cavity periodicity adiabatically transitions from $L_{gate}$ to the terminating array periodicity $L_{term}$, resulting in a termination gate length gradually transitioning from 80 to 140 nm. This serves to reduce scattering from the two ends and boost the Q\(^2\) [20]. These two schemes are depicted in Fig. 2(c).

## 1.3 FinFET Sensing

To understand the conversion from stress to drain current in the sense transistors, modulation of three separate FET properties is examined: oxide capacitance, channel mobility due to piezoresistivity, and silicon bandgap. For ease of visualization, an initial analysis is performed with the source-referenced simplified strong-inversion model with $\alpha = 1$ (the traditional "square-law model", or SPICE level 1)\(^1\):\(^2\)

$$ I_d = \mu C_{ox} \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) $$

where $I_d$ is the drain current, $\mu$ is the carrier mobility, $C_{ox}$ is the gate capacitance, $V_{DS}$ and $V_{GS}$ are the drain-to-source and gate-to-source bias, respectively, $W$ and $L$ are the channel width and length, and $V_T$ is the threshold voltage required for significant channel conduction.

Capacitance modulation in these devices is the same mechanism used in electrostatic drive of these devices, except that rather than sensing the gate current directly, the capacitance modulation is being amplified through transistor action into a change in drain current. The piezoresistive effect, whereby the semiconductor carrier mobility is modulated through stress in the transistor channel, likewise appears as a multiplier on the transistor drain current. Semiconductor bandgap modulation, on the other hand, largely affects the threshold voltage of the transistor. For a complete derivation of these effects, the reader is directed to the derivation in Appendix B. Modified to include the effects of stress on $\mu$, $C'_{ox}$, and $V_T$ (modeled as $\mu(\sigma) = \mu_0 + \Delta \mu$), the original expression for current in the linear region becomes the following:

$$ I_d(\sigma) = (\mu_0 C'_{ox0} + \mu_0 \Delta C'_{ox} + C'_{ox0} \Delta \mu + \Delta \mu \Delta C'_{ox}) \ast \frac{W}{L} \left( (V_{GS} - V_{T0}) V_{DS} - \frac{V_{DS}^2}{2} \right) $$

$$ - \Delta V_T V_{DS} \frac{W}{L} \left( \mu_0 C'_{ox0} + \mu_0 \Delta C'_{ox} + C'_{ox0} \Delta \mu + \Delta \mu \Delta C'_{ox} \right) $$

where

$$ \Delta I_d(\sigma) = (\mu_0 \Delta C'_{ox} + C'_{ox0} \Delta \mu + \Delta \mu \Delta C'_{ox}) \ast \frac{W}{L} \left( (V_{GS} - V_{T0}) V_{DS} - \frac{V_{DS}^2}{2} \right) $$

$$ - \Delta V_T V_{DS} \frac{W}{L} \left( \mu_0 C'_{ox0} + \mu_0 \Delta C'_{ox} + C'_{ox0} \Delta \mu + \Delta \mu \Delta C'_{ox} \right) $$

Likewise, in saturation

$$ I_{d0} = \mu C_{ox} \frac{W}{2L} \left( (V_{GS} - V_T)^2 (1 + \lambda [V_{DS} - (V_{GS} - V_{T0})]) \right) $$

where $\lambda$ represents the channel length modulation coefficient (0.05 to 0.25 typical) and

\(^1\)This model has only a handful of parameters to describe device operation, as opposed to the more advanced BSIM models used commonly in industry, which include many empirically fit parameters to give the best device models for commercial applications [21]. This simplified model is used with the understanding that the derivation, while not capturing a variety of short channel effects that influence modern transistor behaviour, will provide a more intuitive understanding into the basics of active FET sensing.
\[ \Delta I_d = (\mu_0 \Delta C_{ox} + C'_{ox0} \Delta \mu + \Delta \mu \Delta C'_{ox}) \ast \frac{W}{2L} (V_{GS} - V_T)^2 (1 + \lambda (V_{DS} - V_{GS} + V_T)) \]
\[ - \frac{W}{2L} (\mu_0 C_{ox0} + \mu_0 \Delta C_{ox} + C_{ox0} \Delta \mu + \Delta \mu \Delta C_{ox}) \left[ \Delta V_T \left[ \lambda (V_{GS} - V_{T0})^2 - 2(V_{GS} - V_{T0}) \ast \left(1 + \lambda [V_{DS} - (V_{GS} - V_{T0})]\right) \right] + \Delta V_T^2 \left[ \left(1 + \lambda [V_{DS} - (V_{GS} - V_{T0})]\right) - 2\lambda (V_{GS} - V_{T0}) \right] + \Delta V_T^3 [\lambda] \right] \] (6)

For modern sub-micron devices, carriers do not exhibit constant mobility but rather undergo velocity saturation at high fields. A simplified way to model this analytically is through a piece-wise equation
\[ v_d = \begin{cases} \frac{\mu |E_x|}{1 + |E_x|/E_{sat}}, & |E_x| < E_{sat} \\ v_{sat}, & |E_x| > E_{sat} \end{cases} \] (7)

which, solved at \( v_d = v_{sat} \), gives
\[ E_{sat} = \frac{2v_{sat}}{\mu} \] (8)

and leads to a modified expression for drain current
\[ I_d = \begin{cases} \mu C_{ox} \frac{W}{L} \left( \frac{1}{1 + \frac{V_{DS}}{E_{sat}L}} \right) (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} , & V_{DS} < V_{DS_{sat}} \\ C_{ox} W v_{sat} \frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_{sat}(L - \Delta L)} , & V_{DS} > V_{DS_{sat}} \end{cases} \] (9)

where
\[ V_{DS_{sat}} = \frac{(V_{GS} - V_T) E_{sat} L}{(V_{GS} - V_T) + E_{sat} L}. \] (10)

An important nuance for acoustic resonators is that both the saturation velocity and the change in mobility (piezoresistive effect) are related to the change in carrier effective mass caused by acoustic deformation of the crystal lattice - saturation velocity by \( m^* - \frac{1}{2} \) and mobility by a factor between \( m^* - \frac{1}{2} \) and \( m^* - \frac{5}{2} \), depending on doping (for a detailed analysis, see Appendix C). This relation means that, while DC current may saturate, the AC piezoresistive effect can still change drain current to an extent, even in the saturation region. For this reason, a compound model is utilized that incorporates velocity saturation in the calculation of DC drain current but allows mobility to vary freely. Under this approach, the contribution to RF output from both electrostatic forces and mobility modulation should scale linearly with drain current. The contribution from any threshold voltage shift is seen to be related to drain bias only in the linear regime and is scaled by the impact of mobility and capacitance changes. In the saturation regime, on the other hand, the threshold voltage shift is primarily a function of gate bias and is modified by drain bias only through channel length modulation. These expressions for \( \Delta I_d \) represent one half of the device transfer function \( g_{mdt} \), discussed in Eq. 4 with the other half being given by the voltage-to-strain conversion and subsequent strain confinement/resonance. While direct measurement of strain in the solid-state resonator in the front end of line poses a challenge, all three of these aspects are subsequently investigated using measured electrical results.
2 Results and Discussion

DC results, shown as an example for the 80 nm gate length device A1 in Appendix F, indicate that the sense transistors in all devices were working as intended. The large current values of approximately 2 mA when gate and drain are biased at $V_{dd}$ are due to the parallel DC connection of the two sense transistors and large effective width of the individual transistors, where 40 fins span the resonance cavity (in y-direction) and are electrically connected in parallel.

2.1 Analysis of Design Variations

While DC results were similar for all devices (outside expected differences due to gate length), resonance mode confinement was highly dependent on the design variations studied. A summary of all measured devices as well as a comparison of their differential transconductance spectra from 9.5 to 13.5 GHz are shown in Fig. 2. From these data, it is evident that phononic crystal confinement in the $M_x$ layers results in significantly improved quality factor and maximum transconductance. Also visible is the role the type of termination has in defining the center frequency of nearby spurious modes in the device.

These differences are quantified in Table 1, where the center frequency, quality factor, and height of resonant peaks in $g_{md}$ are compared for the three design splits after elimination of high-error peak fit ($\approx 5\%$ of data overall). For termination, this process is straightforward as there exists an abrupt and gradually terminated copy of every device. The resulting analysis indicates an increased transconductance in gradual transition devices (352 nS) vs. abruptly terminated ones (302 nS), with a corresponding increase in average quality factor (32 vs. 24). In addition to this enhancement, average resonance center frequency was shown to decrease slightly from 11.29 to 11.16 GHz, driven by the downward shift in the left-most peak of the high-Q cluster of modes seen in PnC-confined devices.

To investigate phononic crystal confinement, analysis was limited to designs with 80 nm gate length
Table 1: ANOVA Results for Peak Fits

|            | Frequency [Hz] | Height [nS] | Q               | Samples                  |
|------------|----------------|-------------|------------------|--------------------------|
|            | Mean           | Std. Error  | Mean            | Std. Error               |                          |
| PnC Confinement |               |             |                 |                          |                          |
| Mx, Cx     | 11.27 G        | 52.8 M      | 451.1           | 30.6                     | 44.32                    | 1.68                     | A1-A4, B0-B1 (L\textsubscript{gate}=80 nm) |
| Mx Only    | 11.22 G        | 55.9 M      | 379.4           | 32.5                     | 37.55                    | 1.78                     |                          |
| Plates     | 276            | 11.26 G     | 203.6           | 37.5                     | 19.88                    | 2.05                     |                          |
| Termination| Abrupt         | 11.16 G     | 33.4 M          | 301.6                    | 13.9                     | 24.21                    | 0.795                    | All                      |
| Gradual    | 11.29 G        | 35.4 M      | 352.4           | 14.7                     | 31.71                    | 0.843                    |                          |
| L\textsubscript{gate} | 80 nm         | 11.66 G     | 23.0 M          | 1.866                    | 153                      | 84.8                     | 4.40                     | A3-A6                    |
|            | 106 nm         | 10.71 G     | 23.0 M          | 1.651                    | 153                      | 87.1                     | 4.40                     |                          |

(A1-A4 and B0-B1) and the confinement treated as a three-level categorical factor. This analysis showed no significant change in center frequency of the modes, but it did show significantly improved transconductance (204, 379, 451 nS) and quality factor (20, 38, 44) with increasing layers of phononic crystal confinement. These trends are highlighted in Fig. 3 along with an example of the peak fitting results used for parameter extraction.

Compared to the other factors studied, L\textsubscript{gate} is unique in that it is the primary design variable for selecting center frequency due to the mode being defined by source/drain spacing. This means that the different values studied dramatically change the cavity shape and thus all peaks detected in the studied frequency span of 9.5 to 13.5 GHz cannot be used in the analysis, as they are not present in this range in all devices. To overcome this, a much smaller comparison of A3 and A4 (L\textsubscript{gate}=80 nm) to A5 and A6 (L\textsubscript{gate}=106 nm) was performed using only the prominent modes with transconductance above 500 nS and Q above 25 that were present towards the center of the spectra. The downside of this approach is that gate length is confounded with a change in phononic crystal design that is necessary for the different device geometries due to design rule challenges. Despite this, the fact that confinement method showed no significant change in center frequency for 80 nm devices points towards this shift being dominated by gate length as would be expected.

As the device with the highest performance, resonator A2 was selected for further analysis, with the maximum transconductance of the ≈11.75 GHz mode examined as a function of device biasing. This was done at a drive bias of V\textsubscript{dd}, as g\textsubscript{mdd} was seen to increase linearly with the increase in MOS capacitance at higher drive bias (see Appendix F). The dependence of g\textsubscript{mdd} on sense transistor biasing, shown in Fig. 4 highlights that device transconductance, as expected, is modulated in a manner consistent with piezoresistive and bandgap modulation. While transistor parameters are of the correct order of magnitude in the reported data fit, they vary slightly from real-world values due to the simplified model used. For example, the square law model does not accurately capture subthreshold (accumulation and weak inversion) behaviour, and thus the fit favors a slightly lower V\textsubscript{t} to more closely fit bias currents near zero. This, in turn, leads to an overestimation of current at higher biases, which is compensated by a lower than expected value for mobility and a slightly larger equivalent oxide thickness. On the AC side, the fit is hindered by the presence of a noise floor in the s-parameter measurements that may obscure lower peak levels. This, along with the poor near-threshold characteristics of the square law model, contributes to the fitting error at lower values of g\textsubscript{mdd}. Moving away from the square law model to a more advanced model such as that derived by Taur et al. that captures all regions of operation may decrease this error. Likewise, adopting band-structure simulations of silicon as a result of acoustic deformation could provide a unified source of mobility and threshold voltage changes in the transistor, at the expense of increased computation requirements.

For NMOS devices oriented in the 1\textsuperscript{110} direction, the negative piezoresistive coefficients ensure that the contribution of the threshold voltage shift and mobility is additive. If fRBT devices are implemented with PMOS devices or in processes with different fin orientations, care should be taken to ensure that the dominant stress-dependent effects do not compete against each other. This may not be as much of an issue for long channel RBT devices, as piezoresistive modulation dominates for long channel devices that are not supply voltage constrained.

The highest magnitude peak fit occurred in device A2 (L\textsubscript{gate} of 80 nm, gradually terminated, dual PnC) at 11.73 GHz with a differential transconductance of 4.49 µS and a Q of 69.8, for an f * Q product of 8.19*10\textsuperscript{13} at drain, gate, and drive biases of 0.6, 0.8, and 0.8 V, respectively. While previous unreleased
Figure 3: (a): Output of peak fit algorithm for one of the 392 individual measurements evaluated. Peak fits with error above 0.025 were filtered (120 out of 2554 peaks) and then design splits were evaluated by comparing means and performing ANOVA between appropriate samples. The most significant process variation, BEOL confinement, is shown in (b), with complete results given in Table 1. In addition to increasing average peak height and $Q$ across a range of drive and drain biases, it is also evident that an Mx-PnC greatly increases the maximum peak height, from under 1 $\mu$S to 4.5 $\mu$S for the highest-performing resonator. (c) shows $Q$ and amplitude of fit resonance peaks, filtered by a minimum $Q$ of 25 and height of 750 nS, with each dot indicating a peak of the correspondingly colored device under a single bias condition. Transconductance variations at the same frequency show the dependence of the resonance on electrical biases. Also evident is the change in center frequency due to gate length, and splitting from two to three distinct modes with gradual termination, as first shown in Fig. 2.
Figure 4: (a) Simulated contributions to $\Delta I_D$ from bandgap modulation (threshold voltage), piezoresistive modulation (mobility), electrostatic modulation (oxide capacitance), and cross-term. For short channel devices that are supply voltage constrained, bandgap and piezoresistive modulation are of similar magnitudes and dominate over electrostatic terms. (b) These two terms, along with the overall drain current modulation, are plotted against DC bias current of the sense transistor (X-axis) for simulated (top) and experimental (bottom) devices. Gate bias is shown by marker color (blue to yellow) and ranges from 0.4 to 0.8 by 0.1 V. Drain bias is represented with marker size, moving from small to large as bias increases from 0.1 to 0.8 by 0.1 V. The large cluster of points with equal gate biases and similar drain currents indicate saturation mode operation for those bias conditions with channel length modulation. The mobility term is linear with drain current, whereas the threshold voltage term due to bandgap modulation has both a flat (i) region in the linear regime with no $V_G$ dependence for constant $V_D$ and a slight $V_D$ dependence (ii) for constant $V_G$ in the saturation regime. Experimental data shows roughly linear dependence of drain current on gate voltage (a hallmark of velocity saturation vs. the $V_G^2$ dependence of the long channel model). Some deviation between the model fit and experimental results can be seen at high drain bias and low gate bias, which may be indicative of mobility degradation due to vertical fields, which is not modeled currently. Otherwise, experimental results show a similar shape to that of the simulated device, indicating the dominance of both piezoresistive and bandgap modulation in the experimental resonator. (c) Model fit to experimental results ($\mu = 79 \text{ cm}^2/\text{Vs}, \text{ equivalent oxide thickness}=1.6 \text{ nm}, V_t=0.206 \text{ V}, v_{sat}=1.83*10^7 \text{ cm/s}, \lambda=0.47, W = 3 \text{ um}, \text{ total stress}=1 \text{ MPa}$). A basin-hopping algorithm is used to find a global minimum fit for the DC transistor parameters, which are then fixed for the AC fit, achieved by varying stress.
Table 2: Comparison with Contemporaneously Reported X and K\textsubscript{u} Band Resonators

| Ref | \(f_0\) [GHz] | \(Q\) | \(f_0 \ast Q\) | Technology | Released | Area [\(\text{um}^2\)] |
|-----|----------------|-------|----------------|------------|----------|----------------|
| This Work | 11.7 | 69.8 | 8.2*10\textsuperscript{11} | 14LPP | No | 135 |
| 25 | 11.5 | 24 | 2.8*10\textsuperscript{11} | 32SOI | No | 15 |
| 26 | 8.8 | 750 | 6.6*10\textsuperscript{12} | Custom AlN | Yes | 6,500 |
| 4 | 11.1 | 615 | 6.8*10\textsuperscript{12} | Custom AlN | Yes | 675 |
| 27 | 13.0 | 282 | 3.7*10\textsuperscript{12} | Custom LiNbO\textsubscript{3} | Yes | 2,000 |
| 28 | 14.5 | 400 | 5.8*10\textsuperscript{12} | PCB Microstrip | - | 27,000,000 |

Resonators in the 32 SOI process have achieved an \(f \ast Q\) product of \(3.8 \ast 10^{13}\) with phononic confinement at 3.3 GHz, these 14 nm devices exhibit 50x higher transconductance and show an almost 3x improvement in \(Q\) over a similar frequency measured mode in 32 SOI devices. \(^{24, 25}\) Compared to some contemporary resonators in the X and adjacent K\textsubscript{u} (12-18 GHz) bands in Table 2, the unreleased devices in this work achieve moderate \(f \ast Q\) in a commercially available process in an area smaller than comparable released devices. This, combined with the fact that the devices are integrated in the front-end-of-line of a commercial CMOS advanced technology node, opens the door for tight logic integration with minimum routing (and associated parasitics). Additionally, if process design rule challenges can be overcome, this performance can be achieved across a band of frequencies by varying gate length and phononic crystal design.

3 Conclusion

This work provides an in-depth experimental investigation into the influence of several design parameters on the performance of unreleased Resonant Fin Transistors in standard 14nm FinFET technology. Phononic crystal confinement, shown experimentally here to be the most important variation in improving unreleased resonator performance (2.2x improvement on average), provides significant opportunity for integrating acoustic devices into standard CMOS platforms. The highest performing resonator, a gradually terminated 80 nm gate length device with both Mx and Cx phononic crystal confinement, shows a transconductance amplitude and \(Q\) of 4.49 \(\mu\)S and 69.8 respectively, with an \(f \ast Q\) product of \(8.19 \ast 10^{11}\). At the same time, an analytical model has been demonstrated that predicts resonator performance across sense transistor biasing conditions, utilizing a combined velocity saturated current at DC and unsaturated mobility variation at AC, where acoustic perturbation of carrier effective mass modulates saturation velocity and mobility simultaneously. This highlights the importance of understanding the assumptions that go into developing advanced electrical models for short channel transistors, which may not accurately depict effects present in active electromechanical devices. While creating these phononic confinement schemes in a standard process with strict design rules poses a unique challenge, we have established a methodical way to predict and design resonator performance across multiple CMOS platforms. This technology combined with parallel advancements in CMOS-compatible ferroelectric and piezoelectric thin films, presents the opportunity to develop compact, low-cost, CMOS-integrated, and electrically-controllable resonators with no additional packaging required, opening the door for acoustic processing alongside traditional electronics in advanced CMOS nodes.

A Characterization Methods

A.1 Device Measurement

S-parameter measurements were taken at room temperature and pressure, with an input power of -10 dBm using an Agilent Technologies N5225a PNA, with biasing provided by three Keithley 2400 SMUs as shown in Fig. 1a. All four devices were connected via GPIB and synchronized via published Python scripts. \(^{29, 30}\) WinCal software from Formfactor Inc. was used to facilitate pre-measurement calibration, with a Hybrid LRRM-SOLR performed utilizing an Impedance Standard Substrate (ISS 129-246). Infinity GSSG Probes
were used to allow for a compact biasing scheme, saving die real estate at the expense of increased cross-talk between adjacent signal lines. Gate bias for the sense transistors was provided via a separate DC needle probe.

A.2 Measurement Data Post-Processing

Acquired Touchstone files were first analyzed using Scikit-RF, which was used to transform the single-ended parameters collected into their mixed mode equivalent matrices [31]. From these, gmdd was extracted to allow for analysis of the designed differential mode. The magnitude of gmdd for each sample at a bias of V\text{drain} = 0.6, V\text{gate} = 0.8, and V\text{drive} = 0.8 V, was modeled as a collection of Gaussian peaks and fit via lmfit using the Levenberg-Marquardt algorithm with initial guesses for frequency and peak height provided via user input through matplotlib’s ginput method [32]. These preliminary fits were then used as initial conditions for the remainder of the 377 collected measurements taken at drain biases of 0.2, 0.4, and 0.6 V, drive biases of 0, 0.2, 0.4, 0.6, and 0.8 V, and sense FET gate biases of 0 and 0.8 V. These were again fit via lmfit and parallelized using dask [33]. Due to the noisy nature of the data, with varying spectra between devices, a number of constraints were added to improve fitting accuracy over all design variations. The fitting was weighted by gmdd amplitude to emphasize primary peaks over smaller spurious modes and background noise. Variation in the peak standard deviation between biases was constrained to two times the original standard deviation. Center frequency for each sample was constrained to a maximum of 5% deviation as a function of bias to improve fitting accuracy and reflect the fact that mode shape, and thus frequency of operation, is dictated primarily by device geometry.

Extracted peak properties were then analyzed in SAS JMP statistical discovery software to investigate the relationship between device design splits and variation in performance as a function of device bias [34]. The device splits, shown in Fig. 2, are not entirely orthogonal due to a variety of device design constraints related to the phononic crystals and gate lengths. Thus, one-way analysis of variance (ANOVA) was used on subsets of the experimental devices rather than trying to fit a multidimensional model to the entire sample set.

Examination of expected device performance using the derived analytical model was performed in Python. Contribution for each of the three components (bandgap, mobility, and capacitance modulation) was taken as the difference between the positive and negative stress components. Lmfit was used to perform the optimization routine, using a basinhopping algorithm to find a global minimum for the DC current. The fit of gmdd was performed using the Levenberg-Marquardt algorithm as this had less tendency to settle to a poor-fitting local minima. The simplified 1D model of a 3D transistor led to significant cross-correlation between stress directional components, however magnitude of the total stress remained relatively constant across fit iterations.

B FinFET Sensing: Electromechanical Conversion from Stress to Drain Current

To understand the conversion from stress to drain current in the sense transistors, modulation of three separate FET properties is examined: channel mobility due to piezoresistivity, oxide capacitance, and silicon bandgap.

B.1 Mobility

The piezoresistive effect is typically modeled as a linear change in resistivity (\(\rho\)) as a function of applied stress (\(\sigma\)) and the longitudinal and transverse piezoresistive coefficients (\(\pi\)):

\[
\rho = \rho_0 [1 + \pi_L \sigma_L + \pi_T \sigma_T].
\]  

(11)

Low-field mobility (\(\mu\)) is related to the resistivity as follows, where \(q\) is the elementary charge and \(N\) is the doping concentration per unit volume.

\[
\mu = 1/q \rho N
\]  

(12)
A stress-dependent mobility can be defined in terms of the initial mobility \( \mu_0 \),

\[
\mu(\sigma) = \frac{\mu_0}{1 + \pi_L \sigma_L + \pi_T \sigma_T}
\]  

and the initial value of mobility subtracted out to obtain the net change

\[
\Delta \mu(\sigma) = \mu_0 \left( 1 - \frac{1}{1 + \pi_L \sigma_L + \pi_T \sigma_T} \right) = \mu_0 \frac{-\pi_L \sigma_L - \pi_T \sigma_T}{1 + \pi_L \sigma_L + \pi_T \sigma_T}
\]  

### B.2 Oxide Capacitance

Oxide capacitance changes due to the physical thickness change of the oxide \( t_{ox} \) under strain. This strain \( \Delta t_{ox}/t_{ox0} \) is given by the applied stress divided by the Young’s modulus, \( E \), of the dielectric, assuming the film is stressed in the elastic regime. Such a relation results in the following expressions:

\[
C'_{ox}(\sigma) = \frac{\epsilon_{ox}}{t_{ox0} + \Delta t_{ox}} = \frac{\epsilon_{ox}}{t_{ox0}(1 + \sigma/E_{ox})}
\]  

\[
\Delta C'_{ox} = \frac{\epsilon_{ox}}{t_{ox0}} \left( \frac{1}{1 + \sigma/E_{ox}} - 1 \right) = C'_{ox0} \left( \frac{-\sigma/E_{ox}}{1 + \sigma/E_{ox}} \right)
\]  

### B.3 Bandgap Modulation

Strain dependence of the bandgap of silicon \( E_g \) is given by \[35\]:

\[
E_g(\xi) = E_{g0} + E_{1g} \xi
\]  

where \( E_{1g} \) represents the sensitivity of the bandgap to total strain \( \xi \), where

\[
\xi = \sum_{j=1}^{3} \frac{\sigma_{jj}}{E_{jj}}.
\]

Using this relation, the theoretical dependence of threshold voltage on strain can be derived using a typical expression for extrapolated threshold voltage that is referenced to the approximate onset of strong inversion \[22\]:

\[
V_T = V_{FB} + \phi_0 + \gamma \sqrt{V_{SB} + \phi_0}
\]  

where \( V_{SB} \) is the source to body voltage, \( V_{FB} \) is the flat-band voltage governed by the metal-semiconductor work function \( \phi_{ms} \) and effective oxide charge per unit area \( Q'_0 \), by

\[
V_{FB} = \phi_{ms} - Q'_0/C'_{ox}
\]  

\( \phi_0 \) is a value a few \( 2 < n < 5 \) typical) thermal voltages \( \phi_t \) above the onset of strong inversion

\[
\phi_0 = 2\phi_f + n\phi_t,
\]  

and

\[
\gamma = \sqrt{2q\epsilon_s N_A/C'_{ox}},
\]  

where \( \epsilon_s \) is the semiconductor permittivity \( N_A \) is the semiconductor acceptor doping per unit volume (assuming p-type substrate),

\[
\phi_{ms} = \phi_{ms} - \chi_s - E_g/2 - \phi_f,
\]  

\[
\chi_s = E_{vac} - E_c
\]  

\[12\]
and

$$\phi_f = kT \cdot \ln\left(\frac{N_A}{n_i}\right),$$  \hspace{1cm} (25)

with $n_i$ being the intrinsic carrier concentration in the semiconductor ($\approx 10^{10}$ in silicon at room temperature).

Combining all of this together,

$$V_T(\xi) = \phi_m - \chi_s(\xi) - E_g(\xi)/2 + \phi_f(\xi) - Q_0'(\xi)/C'_{ox}(\xi)$$

$$+ nkT + \frac{\sqrt{2q\epsilon_sN_A(\xi)}}{C'_{ox}(\xi)} \sqrt{V_{SB} + 2\phi_f(\xi) + nkT} \hspace{1cm} (26)$$

The dependence of $C'_{ox}$ on strain has already been discussed. The other terms, however, require further examination. Starting with the expression for $n_i$,

$$n_i = \sqrt{N_cN_v} \cdot \exp\left(\frac{-E_g}{2kT}\right)$$

where $N_{c/v}$ are related to the effective mass of carriers in the semiconductor conduction and valence band as follows:

$$N_{c/v} = 2^{s/2} \sqrt{\frac{2\pi m^{*}_{n/p}}{kT h^2}}$$  \hspace{1cm} (28)

Neglecting the change in $\sqrt{N_cN_v}$ since it will have less impact than the change in the exponential term,

$$n_i(\xi) \approx \sqrt{N_cN_v} \cdot \exp\left(\frac{-(E_g + \Delta E_g)}{2kT}\right) = \sqrt{N_cN_v} \cdot \exp\left(\frac{-E_g}{2kT}\right) \exp\left(\frac{-\Delta E_g}{2kT}\right)$$

$$= n_{i0} \cdot \exp\left(\frac{-\Delta E_g}{2kT}\right) \hspace{1cm} (29)$$

Carrier concentration exhibits a simple dependence on strain as the stretching/compression of the lattice merely changes the number of charges within a fixed volume. To a first order approximation,

$$N_A(\xi) = \frac{N_{A0}}{1 + \xi}$$  \hspace{1cm} (30)

These expressions, along with bandgap dependence on strain, are now inserted into the expression for $\phi_f$ to obtain

$$\phi_f(\xi) = kT \cdot \ln\left(\frac{N_{A0}}{n_{i0}} \cdot \frac{\exp(\Delta E_g/2kT)}{1 + \xi}\right) = \phi_{f0} + kT \cdot \ln\left(\frac{\exp(\Delta E_g/2kT)}{1 + \xi}\right)$$

where

$$\Delta \phi_f = kT \cdot \ln\left(\frac{\exp(\Delta E_g/2kT)}{1 + \xi}\right) = \Delta E_g/2 + kT \cdot \ln\left(\frac{1}{1 + \xi}\right) \hspace{1cm} (31)$$

Examining the change in threshold voltage as a function of gate dielectric stress and strain in the silicon substrate, the only term that does not have a well defined relation is $Q_0'$. This is because the term is the projection of all parasitic charges in the gate stack onto the semiconductor surface. Thus, while this term is itself an effective sheet charge, it in reality encompasses a mixture of sheet and volume charges which respond differently to strain, the ratio of which is not well defined. This term is thus left alone in the expression below, being defined as an initial ($Q_0'$) and change in ($\Delta Q_0'$) value. Substituting the derived relations into Eq. 26 and subtracting out the initial threshold voltage value gives the following expression for $\Delta V_T$:

$$\Delta V_T = -\Delta \chi_s + kT \cdot \ln\left(\frac{1}{1 + \xi}\right) + \left(\frac{\sqrt{2q\epsilon_sN_{A0}}}{C'_{ox}(1 + \sigma/E_{ox})}\right) \cdot \sqrt{2\left(\phi_{f0} + \Delta E_g/2 + kT \cdot \ln\left(\frac{1}{1 + \xi}\right)\right)} + V_{SB} + nkT$$

$$- \sqrt{2q\epsilon_sN_{A0}} \cdot \sqrt{V_{SB} + 2\phi_{f0} + nkT} - \left(\frac{\Delta Q_0' - Q_{00}'\sigma/E_{ox}}{C'_{ox}(1 + \sigma/E_{ox})}\right)$$

$$\hspace{1cm} (33)$$
B.4 Square Law Model

The source-referenced simplified strong-inversion model with $\alpha = 1$ gives the traditional square-law model [22]:

$$I_d = \mu C_{ox} \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$  \hspace{1cm} (34)

Modified to include the effects of stress on $\mu$, $C'_{ox}$, and $V_T$, this becomes the following:

$$I_d(\sigma) = (\mu_0 C'_{ox0} + \mu_0 \Delta C'_{ox} + C'_{ox0} \Delta \mu + \Delta \mu \Delta C'_{ox}) \ast \frac{W}{L} \left( (V_{GS} - V_{T0}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$- \Delta V_T V_{DS} \frac{W}{L} (\mu_0 C'_{ox0} + \mu_0 \Delta C'_{ox} + C'_{ox0} \Delta \mu + \Delta \mu \Delta C'_{ox})$$  \hspace{1cm} (35)

where

$$\Delta I_d(\sigma) = (\mu_0 \Delta C'_{ox} + C'_{ox0} \Delta \mu + \Delta \mu \Delta C'_{ox}) \ast \frac{W}{L} \left( (V_{GS} - V_{T0}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$- \Delta V_T V_{DS} \frac{W}{L} (\mu_0 C'_{ox0} + \mu_0 \Delta C'_{ox} + C'_{ox0} \Delta \mu + \Delta \mu \Delta C'_{ox})$$  \hspace{1cm} (36)

Likewise, in saturation

$$I_{d0} = \mu C_{ox} \frac{W}{2L} \left( (V_{GS} - V_T)^2 (1 + \lambda [V_{DS} - (V_{GS} - V_{T0})]) \right)$$  \hspace{1cm} (37)

and

$$\Delta I_d = (\mu_0 \Delta C'_{ox} + C'_{ox0} \Delta \mu + \Delta \mu \Delta C'_{ox}) \ast \frac{W}{2L} \left( (V_{GS} - V_T)^2 (1 + \lambda (V_{DS} - V_{GS} + V_T)) \right)$$

$$- \frac{W}{2L} (\mu_0 C_{ox0} + \mu_0 \Delta C_{ox} + C_{ox0} \Delta \mu + \Delta \mu \Delta C_{ox}) \left[ \Delta V_T \left[ \lambda (V_{GS} - V_{T0})^2 - 2(V_{GS} - V_{T0}) \ast \left( 1 + \lambda [V_{DS} - (V_{GS} - V_{T0})] \right) \right] \right.$$

$$\left. + \Delta V_T^2 \left[ 1 + \lambda [V_{DS} - (V_{GS} - V_{T0})] \right] - 2\lambda (V_{GS} - V_{T0}) \right]$$

$$+ \Delta V_T^2 \left[ \lambda [V_{DS} - (V_{GS} - V_{T0})] \right]$$  \hspace{1cm} (38)

Observing Eq. 4 combined with the expressions for change in mobility and capacitance (Eqns. 14 and 16), it can be seen that the initial values for mobility and capacitance can both be factored out of the non-$\Delta V_T$ term, resulting in a change in drain current as follows (for the linear regime):

$$\Delta I_d = I_{d0} \left( \frac{-\sigma/E_{ox}}{1 + \sigma/E_{ox}} + \left( -\pi L_\sigma L - \pi T_\sigma T \right) + \left( -\sigma/E_{ox} \right) \left( \frac{-\pi L_\sigma L - \pi T_\sigma T}{1 + \sigma/E_{ox}} \right) \right)$$

$$- \Delta V_T V_{DS} \frac{W}{L} \mu_0 C_{ox0} \left[ 1 + \left( -\sigma/E_{ox} \right) \left( \frac{-\pi L_\sigma L - \pi T_\sigma T}{1 + \sigma/E_{ox}} \right) + \left( -\pi L_\sigma L - \pi T_\sigma T \right) + \left( -\sigma/E_{ox} \right) \left( \frac{-\pi L_\sigma L - \pi T_\sigma T}{1 + \sigma/E_{ox}} \right) \right]$$  \hspace{1cm} (39)

with a similar expression likewise derivable for saturation.
C Mobility and Velocity Saturation Effects

In sub-micron devices with high lateral fields in the channel region, carrier drift velocity does not exhibit a linear dependence on electric field (constant mobility), but rather saturates as $V_{DS}$ increases [36]. The first notable deviation in velocity comes from phonon scattering, whereby carriers in motion lose energy to the lattice around them. This can be modeled via an effective temperature for the carriers, with drift velocity decreasing as the temperature differential increases [37]:

$$\frac{T_e}{T} = \frac{1}{2} \left[ 1 + \sqrt{1 + \frac{3\pi}{8} \left( \frac{\mu_0 E}{c_s} \right)^2} \right]$$  \hspace{1cm} (40)

$$v_d = \mu_0 E \sqrt{\frac{T}{T_e}}$$  \hspace{1cm} (41)

Once the field becomes sufficiently large, carriers may obtain enough energy ($E_p$) to emit optical phonons. When this kinetic energy is transferred to optical phonons, the carriers must subsequently accelerate again to regain kinetic energy [38]. The maximum rate at which they may travel is given by setting the kinetic energy equal to optical phonon energy and solving for velocity:

$$v_s = \sqrt{\frac{2E_p}{m^*}}$$  \hspace{1cm} (42)

To simplify modeling of velocity saturation in compact models, an empirical formula is typically used to encapsulate these effects into a simple equation:

$$v_d = \frac{\mu_0 E}{\sqrt{1 + (\mu_0 E/v_s)^5}}$$  \hspace{1cm} (43)

For simplicity in deriving an analytical equation for transistor operation with the presence of velocity saturation, a piece-wise approximation may also be utilized [22]:

$$v_d = \begin{cases} 
\frac{\mu |E_x|}{1 + |E_x|/E_{sat}}, & |E_x| < E_{sat} \\
|E_x|/E_{sat}, & |E_x| > E_{sat} 
\end{cases}$$  \hspace{1cm} (44)

which, solved at $v_d = v_{sat}$, gives

$$E_{sat} = \frac{2v_{sat}}{\mu}$$  \hspace{1cm} (45)

A comparison of these drift velocity models is shown in Fig. 5, with the understanding that the absolute values of these effects are influenced by doping, device orientation, strain engineering, temperature, and more. For silicon, the two most important phenomena limiting low-field mobility are acoustic-phonon interactions and ionized impurities, with overall mobility calculated as the harmonic mean (Matthiessen rule) of all individual contributions [36].

$$\mu_{ph} = \frac{\sqrt{8\pi q}\hbar^4 C_l}{3E_g^2 m_e^{5/2} (kT)^{3/2}}$$  \hspace{1cm} (46)

$$\mu_i = \frac{64\sqrt{\pi \varepsilon_i^2} (2kT)^{3/2}}{N_i q^3 m^*^{1/2}} \left[ \ln \left( 1 + \frac{12\pi \varepsilon_i kT}{q^2 N_i^{1/3}} \right) \right]^{-1}$$  \hspace{1cm} (47)

Of note is the fact that both mobility and optical phonon emission depend on effective mass, meaning the change in transistor current due to an effect that alters effective mass (such as acoustic deformation of the crystal lattice) will not be subject to velocity saturation like its DC component. Thus, the approach taken in this work is to use a compound model, with unsaturated long-channel expressions used to derive the relative AC change in transistor current and a saturation model, developed hereafter, to obtain the steady-state drain current used for the unstrained initial condition.
Figure 5: Representative curves for various mobility models. \( \mu = 300 \text{ cm}^2/\text{Vs}, c_s \approx 8400 \text{ m/s}, E_p = 63 \text{ meV}, m^* = 0.98, \kappa = 2 \).

Figure 6: Combination of phonon-limited mobility and impurity-limited mobility via Mattiessen rule results in a familiar shape for electrons in Si. Exact relations are presented in Equations 46 and 47. \( T = 300 \text{ K}, m^* = 0.98, C_l = 165 \text{ GPa}, \rho = 2329 \text{ kg/m}^3, \epsilon_s = 11.9 \epsilon_0, E_{ds} = -2.7 \text{ eV} \).
D Velocity Saturated Square Law Model

Utilizing the previously mentioned piece-wise model for carrier drift velocity leads to a modified version of the long channel model:

\[
I_d = \begin{cases} 
\mu C_{ox} \frac{W}{L} \left( \frac{1}{V_{DS}} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) \right), & V_{DS} < V_{DS\text{sat}} \\
C_{ox} W v_{sat} \left( \frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_{sat}(L - \Delta L)} \right), & V_{DS} > V_{DS\text{sat}} 
\end{cases}
\]  

(48)

where

\[
V_{DS\text{sat}} = \frac{(V_{GS} - V_T) E_{sat} L}{(V_{GS} - V_T) + E_{sat} L}.
\]  

(49)

In the long channel limit, \(V_{DS\text{sat}}\) tends towards \(V_{GS} - V_T\) and Equation 45 can be used to substitute in for \(v_{sat}\). Furthermore, linearizing the channel length modulation via Taylor expansion

\[
1 \left( 1 - \frac{\Delta L}{L} \right) \approx 1 + \frac{\Delta L}{L}
\]  

(50)

and taking

\[
\Delta L/L = \lambda (V_{DS} - V_{DS\text{sat}})
\]  

(51)

gives the original long channel expression, shown in Equation 37.

The end result of this is that the DC saturation current no longer scales quadratically with \(V_{GS} - V_T\) but rather linearly reduces the overall current. While the simultaneous change in mobility and saturation velocity with stress prevents AC current waveforms from clipping, this does reduce the magnitude of the mobility and oxide capacitance modulation terms that are linearly proportional to steady-state drain current.
E Model Fit Report

[[Model]]
Model( Id_DC_lmfit)
[[Fit Statistics]]
# fitting method = basinhopping
# function evals = 1309
# data points = 81
# variables = 6
chi-square = 6.2464e-08
reduced chi-square = 8.3285e-10
Akaike info crit = -1687.63316
Bayesian info crit = -1673.26646
## Warning: uncertainties could not be estimated:
eot: at initial value
eot: at boundary
Weff0: at boundary
[[Variables]]
u0: 0.00788908 +/- nan (nan%) (init = 0.03)
eot: 1.6054e-09 +/- nan (nan%) (init = 1e-09)
Vt0: 0.20593644 +/- 0.00395160 (1.92%) (init = 0.3)
vsat: 183092.801 +/- 19456.8380 (10.63%) (init = 200000)
clm: 0.47366497 +/- nan (nan%) (init = 0.3)
Weff0: 3.0000e-06 +/- nan (nan%) (init = 3.2e-06)

[[Model]]
Model(delId_vsat_lmfit)
[[Fit Statistics]]
# fitting method = leastsq
# function evals = 67
# data points = 81
# variables = 3
chi-square = 2.4219e-12
reduced chi-square = 3.1050e-14
Akaike info crit = -2516.41319
Bayesian info crit = -2509.22984
[[Variables]]
stressx: 1004021.25 +/- 1186898.72 (118.21%) (init = 1000000)
stressy: 10000.0691 +/- 1072828.08 (10728.21%) (init = 1000000)
stressz: 10000.0001 +/- 76609.1709 (766.09%) (init = 1000000)
[[Correlations]] (unreported correlations are < 0.100)
C(stressx, stressy) = -0.998
C(stressx, stressz) = -0.294
C(stressy, stressz) = 0.241
F Supplemental Figures

Figure 7: (a) Schematic of the unit cell for the periodic PnC structures, including the metal layer as well as inter-layer dielectric (ILD) films present between each metal layer. The orange region represents the metal whereas the surrounding layers are dielectric. (b) corresponding dispersion relationship with metal dimension of 130 nm with 60 nm gap (Mx). A complete bandgap is obtained between 8 GHz and 12 GHz. (c) highlights the dispersion relationship for PnC structures designed in Cx metal layers (80 nm metal, 80 nm gap). The corresponding bandgap is obtained between 7.6 GHz and 10.7 GHz.

Figure 8: Experimental (a) family of curves and (b) \( I_D - V_G \) DC bias currents for A1 resonator with 80 nm gate length. Drain currents reported are high due to the large width of the sense transistors, which comprise of 40 fins in parallel.
Figure 9: Trend in differential transconductance of largest mode ($\approx 11.75$ GHz) for A1 and A2 resonators (80 nm gate length, Mx and Cx phononic crystal confinement). $g_{mdd}$ (Y-axis) is plotted against DC bias current of the sense transistor (X-axis), tiled by device (X tiles) and drive bias (Y tiles). Gate bias is shown by marker color (blue to yellow), with gate biases of 0.3 V and below overlapping near zero drain current (subthreshold). Drain bias is represented with marker size, moving from small to large as bias increases. The large cluster of points with equal gate biases and similar drain currents indicate saturation mode operation for those bias conditions with channel length modulation. Peak $g_{mdd}$ increases as a function of drive bias and is largely dependent on drain current of sense transistor, although efficiency drops as gate voltage increases. Very low drain biases also tend to be less efficient than saturation mode biasing for a given device current.

Figure 10: Observed drive efficiency of resonators from the linear fits shown in Fig. 9 plotted alongside extracted capacitance from drive transducers vs drive bias on the X-axis indicating that transduction efficiency is dominated by the large change in capacitance in these devices over the small allowable voltage range.
Figure 11: Experimentally measured resonator impedance at input (ports 1 and 3) and output (ports 2 and 4), including input ESD diodes and device to pad routing.
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Author Contribution

J. Anderson performed device measurements, analysis, electrical modeling, and led manuscript preparation. Y. He wrote the sections on phononic confinement and cavity termination schemes and performed simulations related to device acoustic design. B. Bahr designed the devices and managed the tapeout of the resonators measured, as well as construction of an initial COMSOL model for device simulation. D. Weinstein provided feedback and guidance to the authors across device design, measurement, and manuscript preparation.

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