A temporal logic approach to modular design of synthetic biological circuits

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Abstract. We present a new approach for the design of a synthetic biological circuit whose behaviour is specified in terms of signal temporal logic (STL) formulae. We first show how to characterise with STL formulae the input/output behaviour of biological modules miming the classical logical gates (AND, NOT, OR). Hence, we provide the regions of the parameter space for which these specifications are satisfied. Given a STL specification of the target circuit to be designed and the networks of its constituent components, we propose a methodology to constrain the behaviour of each module, then identifying the subset of the parameter space in which those constraints are satisfied, providing also a measure of the robustness for the target circuit design. This approach, which leverages recent results on the quantitative semantics of Signal Temporal Logic, is illustrated by synthesising a biological implementation of an half-adder.

Keywords: Synthetic Biology, Parameter Synthesis, Temporal Logic.

1 Introduction

Synthetic Biology\textsuperscript{14} is an emerging discipline that aims at the rational design of artificial living systems with a predictable behaviour, either by creating new biological entities that do not exist in nature or by redesigning the existing ones. Even though important technological developments have been achieved in this field, the de-novo design of biological circuits implementing a desired behaviour results to be a very hard task, especially for large scale networks. Biological systems are complex to understand and to be engineered: the non-linear nature of interactions reflects in the emergence of systemic behavioural properties, not directly derivable from the knowledge of the individual parts. To model and control such systems we need to understand the relationships between the emergent behaviour and the topology of such complex interactions. A possible approach is to divide the whole system in “subunits” and to look at the structure of the interactions between them. This subdivision is often suggested by the way we describe (the components of) those systems. The idea is that compositionality at the specification level, to a certain extent, has to be reflected into compositionality at the behavioural level. This should depend on the properties satisfied by a single “sub-unit” and on the wiring between them. This way to approach the study of a system
is called modularity and the “subunits” of the system are called modules. Modularity can be effectively achieved in Synthetic Biology, combining a bottom-up \cite{31} and a top-down \cite{30} methodology. The former consists in the assembling of a set of well-characterised modules \cite{31} together to build sophisticated biological circuits and devices. The latter \cite{30} aims to identify and characterise the possible “subunits” and this is also helpful to understand real biological systems, for example to discover unknown structures or behaviours or to better understand and test current knowledge.

To unveil the system dynamics, it is important to correlate the denotation of a module with some of its specific behaviours, and understand how the global properties emerge from these local ones. This can be performed better if the emergent behaviours are specified in a formal language. We consider here a logical characterisation in terms of (linear) temporal logic formulae. In particular, we focus our attention on genetic regulatory circuits, seen as networks of interacting genetic modules (each representing, for instance, a logic gate). Each module has a set of inputs and outputs (usually transcription factors), and its local behaviour is specified by temporal logic properties.

In particular, we characterise the behaviour of logic gates with the addition of constraints on the response time. Logic gates are physical devices implementing a boolean function and they are the fundamental bricks upon which all the other logic circuits, including multiplexers, arithmetic logic units, memories and microprocessors, are built. They are primarily implemented using electronic transistors acting as electronic switches. In the last decade, genetic circuits acting as logic gates have been successfully identified and synthesised \cite{22}. This lead researchers to hope to engineer cells to turn them into miniature computers.

The main idea of this paper, sketched in Figure\[1\] is to translate the structural compositionality of networks of modules into compositionality of local behaviours, exploiting it to enforce a set of global behaviours to the network. This is realised by identifying a subset of parameters for which the truth of local properties implies the truth of the global specification, exploiting the modular structure of the network. We thus interpret the network of modules as a composition of their local properties, connecting the emergent behaviours with the topology of interaction of those local properties. The technical core of our approach is the quantitative semantics of Signal Temporal Logic \cite{20}, which can be seen as a measure of robustness of the satisfaction of a certain formula, and which comes with simulation-based methods to compute the robustness score and to identify a region of the parameter space in which the formula holds true.
The contributions of this paper are thus twofold: a design methodology for biological circuits based on a high level logical specification of behaviours and an algorithmic procedure exploiting compositionality to make parameter synthesis more effective, which gives as a byproduct a measure of robustness of the implementation.

The paper is structured as follows: in Section 2 we introduce the background material. In Section 3 we discuss the logical characterisation of the basic modules in terms of Signal Temporal Logic (STL). In Section 4 we sketch the algorithmic approach to parameter synthesis and in Section 5 we show an application to the design of an half-adder, a fundamental building block of microprocessors. The related works and the final discussion are in Section 6.

2 Background material

Modelling of Gene-Regulatory networks In this paper we consider deterministic models of gene regulatory networks, given by a set of non-linear Ordinary Differential Equation (ODE) [16]. For simplicity, we consider lumped models of gene expression, in which mRNA is not explicitly represented (cf. Remark 2 for a further discussion on this point). We assume to have \( n \) genes and proteins. Concentration of protein \( i \) at time \( t \), \( i = 1, \ldots, n \), is denoted by the variable \( x_i[t] \), while \( x = (x_1, \ldots, x_n) \) denotes the vector of concentration variables. The ODE for \( x_i[t] \) will then be of the form

\[
\frac{dx_i}{dt} = f_i(x) = f_i^+(x) - f_i^-(x),
\]

where \( f_i^+ \) is a function giving the net production rate of \( x_i \), while \( f_i^- \) is its degradation rate, which is usually a linear function of the form \( \mu_i x_i \), for some \( \mu_i > 0 \). The function \( f_i^+ \), instead, encodes the regulatory mechanism of gene \( i \), and is a combination of Michaelis-Menten or Hill functions [27].

Signal Temporal Logic Temporal logic [23] provides a very elegant framework to specify in a compact and formal way an emergent behaviour in terms of time-dependent events. Among the myriads of temporal logic extensions available, Signal Temporal Logic [20] (STL) is very suitable to characterise behavioural patterns in time series of real values generated during the simulation of a dynamical system. STL extends the dense-time semantics of Metric Interval Temporal Logic [1] (MITL), with a set of parametrised numerical predicates playing the role of atomic propositions. STL provides two different semantics: a boolean semantics that returns yes/no depending if the observed trace satisfies or not the STL specification, and a quantitative semantics that in addition returns a measure of robustness of the specification. Recently, Donze et. al [11] proposed a very efficient monitoring algorithm for STL robustness, now implemented in the Breach [8] tool. The combination of robustness and sensitivity-based analysis of STL formulae have been successfully applied in several domains, ranging from analog circuits [15] to systems biology [9, 10], to study the parameter space and also to refine the uncertainty of the parameter sets. In the following we recall [12] the syntax and the quantitative semantics of STL that will be used in the rest of the paper. The boolean
semantics can be inferred using the sign of the quantitative result (positive for true and negative for false).

**Definition 1 (STL syntax).** The syntax of the STL is given by

$$\varphi ::= \top | \mu | \neg \varphi | \varphi_1 \land \varphi_2 | \varphi_1 \mathcal{U}_{[a,b]} \varphi_2$$

where $\top$ is a true formula, conjunction and negation are the standard boolean connectives, $[a, b]$ is a dense-time interval with $a < b$ and $\mathcal{U}_{[a,b]}$ is the until operator.

The atomic predicate $\mu : \mathbb{R}^n \to \mathbb{B}$ is defined as $\mu(x) := (y(x) \geq 0)$, with $x[t] = (x_1[t], \ldots, x_n[t])$, $t \in \mathbb{R}_{\geq 0}$, $x_i \in \mathbb{R}$, and $y : \mathbb{R}^n \to \mathbb{R}$ a real-valued function.

The (bounded) until operator $\varphi_1 \mathcal{U}_{[a,b]} \varphi_2$ requires $\varphi_1$ to hold from now until, in a time between $a$ and $b$ time units, $\varphi_2$ becomes true. The eventually operator $F_{[a,b]} \varphi$ and the always operator $G_{[a,b]} \varphi$ can be defined as usual: $F_{[a,b]} \varphi := \top \mathcal{U}_{[a,b]} \varphi$, $G_{[a,b]} \varphi := \neg F_{[a,b]} \neg \varphi$.

**Definition 2 (STL Quantitative Semantics).**

$$\rho(\mu, s, t) = y(s[t]) \quad \text{where} \quad \mu \equiv y(s[t]) \geq 0$$

$$\rho(\neg \varphi, s, t) = -\rho(\varphi, s, t)$$

$$\rho(\varphi_1 \land \varphi_2, s, t) = \min(\rho(\varphi_1, s, t), \rho(\varphi_2, s, t))$$

$$\rho(\varphi_1 \mathcal{U}_{[a,b]} \varphi_2, s, t) = \max_{t' \in (t+[a,b])} \left( \min \left( \rho(\varphi_2, x, t'), \min_{t'' \in [t, t')} \rho(\varphi_1, x, t'') \right) \right)$$

where $\rho$ is the quantitative satisfaction function, returning a real number $\rho(\varphi, s, t)$ quantifying the degree of satisfaction of the property $\varphi$ by the signal $s$ at time $t$. Moreover, $\rho(\varphi, s) := \rho(\varphi, s, 0)$.

### 3 Logical characterisation of modules

The approach for the synthesis of biological circuits is based on the idea of combining simple genetic networks according to a specific design. These basic building blocks, or modules, are usually composed of a single or few genes, and express a specific transcription factor (or signal) in response to an input signal, generally the presence or absence of activators or repressors influencing the module behaviour. In most of the proposed approaches [27, 28], such modules are the biological equivalent of the logic gates of electronics, and as such they encode simple boolean functions, like AND, OR, or NOT, that can be combined together to build more complex circuits. Logic gates are usually described by their truth table. However, when moving from electronics to biology, the temporal dimension becomes much more relevant, and it cannot be neglected. Furthermore, biological modules considered in literature often produce more complex input/output (I/O) responses than a boolean I/O relationship, like pulses and oscillations [27]. For this reason, we find more convenient to describe the I/O behaviour of a module by a set of temporal logic properties.

More precisely, we define a module $\mathcal{M}$ to be a genetic network containing $n$ genes, that produce proteins whose concentration is indicated by $x = (x_1, \ldots, x_n)$. The genes
of $M$ are also regulated by additional $n_I$ external transcription factors, which are the inputs of the module. A subset of $n_O$ of the produced proteins constitutes the output of the module. The behaviour of such a module is characterised by a set of STL formulae of the form $\varphi_I \rightarrow \varphi_O$, expressing an I/O relationship, which can be arbitrarily complex. Here $\varphi_I$ depends only on the concentration of the input signals $x_I = (x_{I_1}, \ldots, x_{I_{n_I}})$ and $\varphi_O$ only on the concentration of the output signals $x_O = (x_{O_1}, \ldots, x_{O_{n_O}})$. Modules can be easily connected into a network, by using one output of a module as the input of another module (see Figure 2). Such networks can still have external inputs, while a subset of outputs of their modules will be identified as the output of the network. Furthermore, the network behaviour can also be characterised in terms of a temporal I/O relationship given by STL formulae of the form $\varphi_I \rightarrow \varphi_O$. In this sense, a network is nothing but a more complex module, which can then be used as a building block itself, resulting in a hierarchical compositional approach to circuit design.

**Example: Logic gates.** As an example, in this paper we consider modules corresponding to AND, OR, and NOT logic gates. For instance, a simple biological implementation of an AND gate can be obtained by a module in which a single gene, producing the output protein, is activated by two input signals, both required to start the gene expression. This requirement can be enforced directly at the level of the gene promoter [22] or by letting the complex formed by two input proteins activate the gene [19]. We stick to the first formulation. The truth table of the gate is shown in Table 1. To each input and output protein, we associate two thresholds, $\theta_+$ and $\theta_-$. The value true in the truth table corresponds to a concentration of the corresponding protein above $\theta_+$, while the value false corresponds to the concentration being below $\theta_-$. In the truth table we also provide a high level specification of the temporal behaviour of the gate, in terms of the maximum response time $\delta$ and the minimum duration $\lambda$ of the output signal. The former is an upper bound on the time needed by the gate to stabilise. The latter, instead, specifies for how long the output remains up or down. This in turn implies a constraint on the duration of the input signal: if we want the output to remain up for $\lambda$ units of time, then both inputs have to remain up for at least $\lambda + \delta$ units of time. We can easily turn such a truth table into a set of STL formulae, a formula for each row. For instance, the row four of Table 2 gives:

$$G_{[0,\lambda+\delta]}(x_A \geq \theta_{A+} \land x_B \geq \theta_{B+}) \rightarrow F_{[0,\delta]}G_{[0,\lambda]}(x_C \geq \theta_{C+}),$$

where $x_A$ and $x_B$ are the input signals and $x_C$ is the output. The mathematical model associated with this gate will be given by the non-linear ODE:

$$\dot{x}_C = H_{AND}(x_A, x_B, x_C, k) = k_{AB} \frac{x_A^n}{K_A^n + x_A^n} \frac{x_B^n}{K_B^n + x_B^n} - k_C x_C,$$

where $k = (k_{AB}, k_C, K_A, K_B, n)$ is a tuple of 5 parameters: $k_{AB}$, the maximum production rate (here we assume a zero basal expression rate), $k_C$, the degradation rate, $K_A$ and $K_B$, governing the Hill activation function, and $n$, governing the steepness of the Hill function.

The other basic logic gates can be modelled in a similar fashion [22]: the OR gate can be obtained from the AND gate by a non-collaborative activation of gene expression.
(e.g., replacing in the ODE model the product of Hill functions by a single Hill function depending on the sum of the two concentrations), while the NOT gate can be modeled by a gene whose production is repressed by the input protein. For actual biological implementations, see for instance the discussion in [22,27].

Example: XOR gate. Figure[2] shows how to build a XOR gate using AND, OR, and NOT gates. We stress here that the circuit architecture, seen as an implementation of a boolean function, can be obtained by classical techniques (e.g. by Karnaugh maps [17]). To fully specify the extended truth table of the XOR gate, like for the AND gate (cf. Table[1]), we need to specify additional information about the maximum response time and the minimal duration of the output signal for the network. These two quantities obviously depend on the corresponding ones of the constituent modules. Here we will specify a target temporal behaviour for the network and we will consequently constrain the temporal behaviour of modules.

Suppose we fix a maximum response time $\delta$ and a minimum duration $\lambda$ of the output signal for the XOR gate. Looking at Figure[2] we clearly see that the input signal to the XOR gate has to go through no more than three gates before influencing the output. Hence, if each gate has a maximum response time of $\delta/3$, we obviously obtain a response time for the XOR bounded by $\delta$. To enforce the constraint on the minimum duration of the output signal, we just need to make the output signals of internal gates last sufficiently long to trigger an output signal of the network of the target duration. This can be done by simply taking into account the maximum response delay of each gate. In the XOR example, we obtain that the AND gates need to have a minimal duration of $\lambda + \delta/3$, while the NOT gates of $\lambda + 2\delta/3$. Clearly, the input signal of the network needs to stay on for $\lambda + \delta$ units of time.

Constraints for arbitrary acyclic networks of logic gates. This simple compatibility analysis is easily generalised to arbitrary acyclic networks of logic gates, to which we restrict ourselves for the moment. Dealing with feedback loops is more complicated and is left to future investigation.

Consider a generic module/logic gate in an acyclic network, with target maximum delay $\delta$ and target output signal duration $\lambda$. For each module $\mathcal{M}$ of such a network, let $\ell_f(\mathcal{M})$ be the length of the longest path from $\mathcal{M}$ to an output module (i.e. a module producing one output of the network) and $\ell_b(\mathcal{M})$ be the length of the longest path from $\mathcal{M}$ to an input module (i.e. a module with an external input). Due to the acyclic nature of the network, both such quantities are finite and can be easily computed by a visit of the graph. Then the processing of an input signal passing from $\mathcal{M}$ has to go through at most $\ell_f(\mathcal{M}) + \ell_b(\mathcal{M}) + 1$ modules, so that a maximum delay of $\delta(\mathcal{M}) = \delta/(\ell_f(\mathcal{M}) + \ell_b(\mathcal{M}) + 1)$ guarantees the response time bound on the network. As for the minimum duration of the output for module $\mathcal{M}$, we can obtain it by the recursive relation $\lambda(\mathcal{M}) = \delta(\mathcal{M}) + \max\{\lambda(\mathcal{M}')\}$, where $(\mathcal{M},\mathcal{M}')$ is an edge of the network, i.e. $\mathcal{M}'$ is a module receiving as input an output of $\mathcal{M}$. These relationships are easily extended to modules with more than one output, defining a max response time constraint for each output.
We observe here that this compatibility analysis between delays and durations has a counterpart in the STL characterisation of module behaviours. The main idea is that we can express the consistency of the output-input links by the STL formulae like:

$$F_{[\nu_1, \nu_1 + \gamma_1]} G_{[0, \lambda_1]} (x \geq \theta_+) \rightarrow G_{[\nu_2, \nu_2 + \mu_2]} (x \geq \theta_+),$$

(3)

This formula states that if a variable is eventually expressed for $\mu_1$ units of time, starting between time $\nu_1$ and $\nu_1 + \gamma_1$, it is for sure expressed for $\mu_2$ units of time, starting at time $\nu_2$. If we set $\mu_1 = \lambda + \delta$, $\mu_2 = \lambda$, $\gamma_1 = \delta$, and $\nu_2 = \nu_1 + \delta$, with $\nu_1 \geq 0$, $\lambda$, $\delta > 0$ arbitrary, we obtain that the formula (3) is valid. According to the previous discussion, we need to choose $\lambda = \lambda(M)$ and $\delta = \delta(M)$.

Remark 1. In principle, we can consider more complex building blocks than logic gates, for instance modules acting as switches or oscillators. To this end, we need to generalise the technique for combining modules. More specifically, effective connection of modules is enforced by requiring the validity of formula (3), which is of the form $\varphi_O \rightarrow \varphi_I$. Such a formulation in terms of validity of STL formulae can be extended to more general output properties (or proper subformulae thereof). For instance, we can describe oscillations as signals being eventually above a high threshold for some time, and then falling below a low threshold for a subsequent period of time (this property holding globally). The subformulae describing these two behaviours can then be matched with input formulae of the kind considered in this paper.

### 4 Parameter synthesis

Consider a network composed by modules representing logic gates, fix a network specification in terms of an extended truth table/STL formulae, and consider an ODE model of the network, depending on a tuple of parameters $k$. We now tackle the problem of identifying parameters $k$ such that the network satisfies the specifications. According to the previous section, in order to satisfy the temporal constraints at the network level, we can simply enforce local constraints at the module level. The key intuition of our approach is that modularity can be further exploited, doing parameter synthesis for each module, with a guarantee that the so obtained parametrisation will satisfy the global specification at the network level. Furthermore, we will identify a set of compatible parameter values rather than a single point. Within the set, furthermore, we can identify

| Inputs | Output | Input\Output |
|--------|--------|--------------|
| max delays=$\delta$ | min. duration=$\lambda$ | STL Formula |
| pA | pB | pC |
| low | low | low | $G_{[0, \lambda + \delta]} (x_A \leq \theta_{A-} \land x_B \leq \theta_{B-}) \rightarrow F_{[0, \delta]} (x_C \leq \theta_{C-})$ |
| low | high | low | $G_{[0, \lambda + \delta]} (x_A \leq \theta_{A-} \land x_B \geq \theta_{B+}) \rightarrow F_{[0, \delta]} (x_C \leq \theta_{C-})$ |
| high | low | low | $G_{[0, \lambda + \delta]} (x_A \geq \theta_{A+} \land x_B \leq \theta_{B-}) \rightarrow F_{[0, \delta]} (x_C \leq \theta_{C-})$ |
| high | high | high | $G_{[0, \lambda + \delta]} (x_A \geq \theta_{A+} \land x_B \geq \theta_{B+}) \rightarrow F_{[0, \delta]} (x_C \geq \theta_{C+})$ |

Table 1. Extended truth table for the AND gate
an optimal parametrisation, by maximising the satisfaction level of the properties, according to STL quantitative semantics. We can also search a biological database, like BioBricks, to find genes with the synthesised kinetic constraints.

At the heart of the proposed approach resides the STL characterization of (the biological implementation of) logic gates. Essentially, we will restrict to a single gate, fixing the temporal constraints to those implied by the network requirements and by its structure, and find a subset of the parameter space in which the STL formulae characterising the gate behaviour hold true. This can be done algorithmically, using the simulation approach to parameter synthesis of [9], based on sensitivity analysis and STL quantitative semantics and implemented in Breach [8]. For the simple class of logic gates considered here, we can also do this analytically. Modularity is the key to the efficiency of our approach: as we treat independently each gate, we just need to explore a low dimensional parameter space, which makes the (computational) procedure feasible.

Modularity of parameter synthesis for logic gates. The main difficulty we have to solve is related to the fact that modules are connected in the network, hence they are not independent. Indeed, the expression of a gene is driven by the dynamical behaviour of its input transcription factors. The idea to get around this problem is to do a worst case analysis, showing that a specific parameter combination satisfies the properties for the “worst possible input signal”, and that this implies the satisfaction for all possible input signals compatible with the input constraints. This will result in a conservative, but computationally efficient, estimate. We can define the notion of “worst case input signal” in terms of the STL characterisation of module behaviour. Given an input signal $x_I[t]$ of a module $M$, $t \in [0, T]$, we denote with $x_{\hat{x}, k}[t]$ the trajectory of the module, with input $x_I[t]$ and parameters $k$.

**Definition 3.** An input signal $\hat{x}_I[t], t \in [0, T]$ is a worst-case input signal for the STL specification $\varphi_{Input} \rightarrow \varphi_{Output}$ of the behaviour of a module $M$ if and only if, for each parameter configuration $k$ such that $\rho(\varphi_{Input}, \hat{x}_I) \geq 0$ (and $\varphi_{Input}$ true) and $\rho(\varphi_{Output}, x_{\hat{x}, k}) > 0$, the following property holds:

- for each other input signal $x_I$ satisfying $\rho(\varphi_{Input}, x_I) \geq 0$ (and $\varphi_{Input}$ true), it holds that $\rho(\varphi_{Output}, x_{\hat{x}, k}) \geq \rho(\varphi_{Output}, x_{x_I, k})$.

The characterisation of such a “worst possible input signal” depends on the structure of the target STL formula and on the system of ODE describing a particular module. We provide now such a characterisation for the basic logic gate models considered in this paper and for the STL formulae associated with their extended truth tables.

Consider the property $G_{[0, \lambda + \delta]}(x_A \geq \theta_A^+ \land x_B \geq \theta_B^+) \rightarrow F_{[0, \delta]}(x_C \geq \theta_C^+)$, which describes a row of the extended truth table of an AND gate. This property is of the desired form $\varphi_{Input} \rightarrow \varphi_{Output}$. Now, $\varphi_{Input}$ identifies a subset of trajectories of the space of functions from $[0, \lambda + \delta]$ to $\mathbb{R}^2$, i.e. those that satisfy the inequality $x_A \geq \theta_A^+ \land x_B \geq \theta_B^+$ for all $t \in [0, \lambda + \delta]$. Among those functions, we consider $\hat{x}_A[t] \equiv \theta_A^+$ and $\hat{x}_B[t] \equiv \theta_B^+$, which satisfy $\varphi_{Input}$ but have quantitative satisfaction score equal to zero. Furthermore, for any other trajectory $x_A[t], x_B[t]$ that satisfies $\varphi_{Input}$, we have $x_A[t] \geq \hat{x}_A[t]$ for each $t \in [0, \lambda + \delta]$, and similarly for $x_B$. By monotonicity of Hill functions, this implies that the vector field of the AND gate satisfies...
\[ f_{\text{AND}}(x_A[t], x_B[t], x_C, k) \geq f_{\text{AND}}(\hat{x}_A[t], \hat{x}_B[t], x_C, k) \] for any \( x_C \geq 0 \). It then follows, by integrating the vector field, that \( x_C[t] \geq \hat{x}_C[t] \) for \( t \in [0, \lambda + \delta] \). Looking at the satisfaction function of \( \varphi_{\text{output}} \), defined by

\[ \rho(\varphi_{\text{output}}, x_C) = \max \left( \min_{t \in [0, \lambda]} (x_C[t] - \theta_{C^+}) \right), \]

it is easy to see that \( x_C[t] \geq \hat{x}_C[t] \) for \( t \in [0, \lambda + \delta] \) implies \( \rho(\varphi_{\text{output}}, x_C) \geq \rho(\varphi_{\text{output}}, \hat{x}_C) \). Hence, any configuration of parameters such that \( \rho(\varphi_{\text{output}}, \hat{x}_C) > 0 \) will imply the truth of \( \varphi_{\text{output}} \) for any input signal satisfying \( \varphi_{\text{input}} \), and therefore the truth of \( \varphi_{\text{input}} \rightarrow \varphi_{\text{output}} \). It follows that \( \hat{x}_A, \hat{x}_B \) is a worst-case input signal.

For the AND gate, a similar approach allows us to deal with the other three STL properties associated with the other rows of the truth table. In these cases, we need to find an upper bound for \( x_C[t] \), as we need to satisfy the output property \( F_{[0, \delta]} G_{[0, \lambda]} (x_C \leq \theta_{C^-}) \). To achieve this, we just need to set \( x_j[t] \) to \( \theta_{J^-} \), if the input \( J \) is false, and to \( \gamma_J \) if the input \( J \) is true, where \( \gamma_J \) is the maximum concentration level for the input \( x_j \), obtained by dividing maximum production rate by the degradation rate (here \( J = A, B \)).

In fact, in this way we maximise the production rate. All this analysis is easily extended to OR and NOT gates, and is captured in the following proposition.

**Proposition 1.** Let \( x_O \) be the output of a AND or OR logic gate and let \( x_j \) be a generic input. Fix the attention on a row of the extended truth table.

- If \( x_O \) is high, and \( x_j \) high, then \( \hat{x}_J = \theta_{J^+} \).
- If \( x_O \) is high, and \( x_j \) low, then \( \hat{x}_J = 0 \).
- If \( x_O \) is low, and \( x_j \) high, then \( \hat{x}_J = \gamma_J \).
- If \( x_O \) is low, and \( x_j \) low, then \( \hat{x}_J = \theta_{J^-} \).

Similarly, let \( x_O \) be the output of a NOT logic gate\(^6\) and let \( x_j \) be its input. Then

- If \( x_O \) is high, then \( x_j \) is low and \( \hat{x}_J = \theta_{J^-} \).
- If \( x_O \) is low, then \( x_j \) is high and \( \hat{x}_J = \theta_{J^+} \).

We stress that this proposition not only allows us to do parameter synthesis modularly, but also to find a lower bound on the robustness score of each parameterization.

**Remark 2.** The worst case analysis presented in this section relies on the monotonicity of the robustness score with respect to the input signal. This follows from the monotone dependence of the output on the input (in fact, \( \frac{\partial f}{\partial x} > 0 \)), and of the robustness score on the output. The construction of the worst case input is easily generalised to more complex scenarios satisfying a generalised monotonic property of the robustness score, following [20]. As an example, consider a model of the gene expression in which the gene produces the mRNA, and mRNA is in turn translated into the protein. In this case, for an AND gate, we have an ODE for mRNA similar to the one above, namely \( \frac{dx_m}{dt} = f_{\text{AND}}(x_A, x_B, m_C, k) \), while the ODE for the protein becomes \( \frac{dx_C}{dt} = f_C(m_C, x_C, k) = k_t m_C - k_d x_C \), with \( k_t \) the translation constant and \( k_d \) the

\(^6\) The difference between AND/ OR and NOT gates is in the fact that the input is an activator in the first two cases and a repressor in the last one.
protein degradation constant. The monotonic dependence of the robustness score (when both inputs are on) from inputs essentially follows because a larger input concentration will produce more mRNA, which in turn will result in a higher expression of the protein, giving a larger robustness degree (input/output properties are the same). If such a monotonic dependence fails, determining the worst case input can be more challenging. We will tackle this issue in our future work.

Sketch of the algorithm. Assuming the temporal constraints on the extended truth tables of modules have been derived from those of the network, the algorithm for parameter synthesis then work as follows: for any module/gate of the network, and any row in the extended truth table, fix the values of input signals to the worst case ones, and then do STL parameter synthesis to identify a subset of the parameter space in which the STL formula associated with the row is true. Take the intersection of these sets for each row in the truth table of each module. The STL parameter synthesis can be performed applying the sensitivity-based algorithm [9] implemented in the Matlab toolbox Breach [8]. This is a general approach, applicable to any module for which a worst-case input signal has been identified. However, for logic gates AND, OR, and NOT, we can further exploit their simplicity and characterise analytically a subset of parameters for which the STL specification is satisfied. This is due to the fact that, once the input signals are fixed, the non-linear model of the gate reduces to a linear set of ODEs, for which we can compute the solution in closed form. The details of the computation are reported in the Appendix.

5 Example: Half-Adder

The half-adder is a digital component that performs the sum of two bits A and B and provides two outputs, the sum (S) and the carry (C) signal representing an overflow into the next digit of a multi-digit addition. The value of the sum is $2C + S$. Figure 2 a) shows the simplest half-adder design and it incorporates a XOR gate for S and an AND gate for C. Figure 2 b) shows an alternative design using two NOT gates, two AND gates and one OR gate instead of a XOR gate. This is the design of the half-adder we intend to use, thus exploiting the characterisation of worst-case inputs for AND, OR, and NOT gates given in Proposition 1. Figure 2 c) shows the output of each component gate of the half-adder, for each pair of inputs.

We applied the algorithm discussed in the previous section to such a network layout, fixing the maximum total delay of the half-adder to 12 time units. Applying the method to enforce time constraints to each module, we obtain that all the gates that are part of the XOR gate must have a maximum time delay of 4 time units, while the AND gate whose output is C can have a maximum response time bounded by 12 time units. Before doing parameter synthesis, we also rescaled the concentration of each protein to the interval $[0,1]$. In this way, activation and deactivation thresholds are relative to the maximum steady state expression level of each protein. For

---

We use the convention that parameters not influencing a gate are set to their whole domain by the STL procedure.
Fig. 2. a) Half Adder implemented using two logic gates (XOR, AND), b) Half Adder implemented combining six logic gates, c) truth table for the Half Adder.

Fig. 3. The red curves represent the output signals of the Half-Adder gate, S and C, in the four different combination of the inputs A and B, one for each column; the horizontal lines are the threshold concentrations (θ⁺ in blue and θ⁻ in green); the yellow vertical line represents the time bound δ.

this example, we then arbitrarily fixed all the activation thresholds to θ⁺ = 0.75 and the deactivation thresholds to θ⁻ = 0.25, and then synthesised set of parameters consistent with the STL network specification and with such thresholds. We obtained the following bounds for parameters, with indices in the n and α parameters referring to the output variable and indices in the K parameters referring to the input and output protein, as from Figure 2 (b). AND gate: \( n_C, n_E, n_G \geq 3.2129, 0.3406 \leq K_{AC}, K_{BC}, K_{AE}, K_{DE}, K_{BG}, K_{FG} \leq 0.4228, \alpha_C \geq 0.3074, \alpha_E, \alpha_G \geq 0.9222 \). OR gate: \( n_S \geq 3.1681, 0.4050 \leq K_{ES}, K_{GS} \leq 0.5090, \alpha_S \geq 0.9222 \). NOT gates: \( n_D, n_F \geq 2.5372, 0.4192 \leq K_{AF}, K_{BD} \leq 0.4696, \alpha_D, \alpha_F \geq 0.9222 \). Constraints are similar for all gates of a given class (e.g. all AND gates) as a consequence of the rescaling of variables in [0,1]. Obviously, in a further step matching actual biological components to the circuit design, this rescaling has to be properly accounted for (for instance, by rescaling also the parameters of the biological components). Picking a value for each parameter consistent with the previous constraints, we can observe in Figure 3 that the dynamics of the network indeed satisfies the specifications of a half-adder.

We remark that, even if in this example we fixed the activation and deactivation thresholds and did parameter synthesis for the other parameters of the model, in the formal derivation we considered such threshold as parameters themselves.
6 Discussion

In this paper we focused on the design techniques for synthetic biological systems. We developed an approach based on two ideas: the specification of system properties in terms of signal temporal logic, and the exploitation of modularity to obtain an efficient procedure to identify a set of parameters for which the network satisfies its STL specification. In particular, we concentrated on the parameter synthesis problem for networks of logic gates, implemented as simple genetic networks. For acyclic networks, we are able to identify efficiently a set of parameters satisfying STL formulae encoding not only the desired boolean behaviour of the network, but also constraints on its response time.

Modularity allows us to synthesise parameters efficiently, processing each gate component independently. This is possible by isolating each module from the network assuming the worst possible input, which we formally characterised for the basic logic gates considered. We then showed the approach at work with a network implementing an half-adder.

The approach of this paper can be complemented by looking at databases of biological components, like BioBricks [18], for actual combinations of gene and promoters that satisfy the constraints on parameters. A delicate point for this plan is that we are implicitly requiring each module to produce different, non-interfering, output proteins, a not necessarily biologically realistic hypothesis. We will look at possible ways of relaxing this constraint, as in [32]. Other directions for future work include the generalisation of Proposition 1 to deal with more complex modules, for instance feed-forward networks implementing pulse generation or a low-pass filter. Moreover, we will consider the problem of dealing with more complex network topologies, having feedback loops. We expect to make some progress in this direction by suitably rephrasing parameter synthesis as the computation of a fixed point. Finally, we will also take into account the effects of stochasticity, for instance by exploiting moment closure techniques [29].

Related Work. De novo design of a synthetic biological circuit [7] implementing a desired behaviour is a very computational intensive task. The majority of the existing approaches relies on brute-force techniques running sophisticated optimization (i.e. evolutionary algorithms [13], simulating annealing [6]) algorithms to tune the kinetic parameters [5, 24, 28] values in order to match the desired behaviour.

These methodologies, lacking of compositionality, do not scale well and they are very computationally expensive for large networks. A more rational approach for automatic design was proposed by Marchisio and Stelling in [3, 21] where they show a workflow design taking as input a truth table and generating as output several possible circuit schemes, ranking them in the order of complexity. The choice of a truth table as a input specification for the target circuit design may be not enough when we need to guarantee that the result is produced after a proper delay. Additionally, the design needs to take in consideration the signal compatibility among the “wired” devices (a problem treated in [32]): the output signal of one device must match (in terms of low/high thresholds) with the input signal the other design. The novelty of our contribution is using signal temporal logic as specification language both for the target circuit and for the
available components, adding also time constraints in the design process. Furthermore, the device compatibility is rephrased in terms of a STL formula, of the form $\varphi_0 \rightarrow \varphi_1$, and the correct matching is elegantly obtained by requiring this formula to be valid.

Another related approach, is the one proposed by Batt et al. in [2], where the authors approximate the behaviour of genetic regulatory networks with piecewise multi-affine systems. In this class of models, the state-space is partitioned in hyper-rectangles exhibiting useful convexity properties [4] that allows to compute an over-approximation of the reachable sets. The authors exploit this characteristic to guide the parameter space partitioning in search of the intervals for which the gene networks is enforced to satisfy a particular behaviour expressed in a linear temporal logic formula. However, their approach is not modular, and only the rates of production and degradation of the proteins can be chosen as possible parameters. Furthermore, by using an over-approximation, the property usually expresses invariants and the parameter ranges found are very coarse, without discriminating trajectories with different time-constraints.

Finally, among the vast literature on combinatorial circuit design, we mention [25], where authors study the timing behaviour of a acyclic circuits by means of timed automata. Our approach is simpler and motivated by the inherent precision of delays in ODE models. However, the techniques of [25] could be helpful to relax the timing constraints we impose and to deal with intrinsic variability of biochemical systems.

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A Author’s contributions

L. Nenzi (PhD student at IMT, Lucca) developed the mathematical and the computational part. All authors contributed to brainstorming and to the writing.

B Half-Adder, system of ODEs

The full ODE system for the Half-Adder model is:

\[
\begin{align*}
\frac{dx_D}{dt} &= \frac{\beta_D}{1+(K_D+xB)^n} - \alpha_D \cdot x_D, \\
\frac{dx_E}{dt} &= \beta_E \cdot \frac{x_E^n}{1+(K_E+xB)^n} - \alpha_E \cdot x_E, \\
\frac{dx_F}{dt} &= \beta_F \cdot \frac{x_F^n}{1+(K_F+xB)^n} - \alpha_F \cdot x_F, \\
\frac{dx_G}{dt} &= \beta_G \cdot \frac{x_G^n}{1+(K_G+xB)^n} - \alpha_G \cdot x_G, \\
\frac{dx_S}{dt} &= \beta_S \cdot \frac{x_S^n}{1+(K_S+xB)^n} - \alpha_S \cdot x_S, \\
\frac{dx_C}{dt} &= \beta_C \cdot \frac{x_C^n}{1+(K_C+xB)^n} - \alpha_C \cdot x_C, \\
x_D(0) &= x_D^0, \\
x_E(0) &= x_E^0, \\
x_F(0) &= x_F^0, \\
x_G(0) &= x_G^0, \\
x_S(0) &= x_S^0, \\
x_C(0) &= x_C^0;
\end{align*}
\]

where \( A \) and \( B \) are the inputs of the whole system, \( D \) and \( F \) are outputs of NOT gates, \( E, G \) and \( C \) are outputs of AND gates and \( S \) is the output of an OR gate.

C Analytic characterisation of parameter synthesis for logic gates

If we fix the value of inputs signals, each gate (AND, NOT, OR) can be described by a linear ODE systems of the form

\[
\begin{align*}
\frac{dx}{dt} &= \beta \cdot K - \alpha \cdot x, \\
x(0) &= x_0;
\end{align*}
\]

where \( x \) is the concentration of the output, \( \beta > 0 \) is the production rate, \( \alpha > 0 \) the degradation rate and \( 1 \geq K \geq 0 \) is the Hill term. We can rescale the systems in \([0,1]\) observing that, for each \( t \), \( x(t) \leq \frac{\beta}{\alpha} \), the steady state value for \( K = 1 \), provided \( x_0 \leq \frac{\beta}{\alpha} \).

Calling \( \gamma = \frac{\beta}{\alpha} \), and \( \tilde{x} = x/\gamma \), we have:

\[
\begin{align*}
\frac{d\tilde{x}}{dt} &= \frac{d(x)}{dt} = \frac{\beta}{\gamma} \cdot K - \alpha \cdot \frac{x}{\gamma} = \alpha \cdot \tilde{K} - \alpha \cdot \tilde{x}, \\
\tilde{x}(0) &= \tilde{x}_0;
\end{align*}
\]

where \( \tilde{K} = \frac{\beta}{\alpha} \cdot K \).
The analytic solution of this equation, omitting the tilde for simplicity, is:

\[ x(t) = K + (x_0 - K) \cdot e^{-\alpha t}. \]  (4)

The constraints on the dynamics expressed by STL formulas, in the simple case of constant inputs, can be translated into a systems of inequalities. As an example, consider the AND gate and the STL formula obtained from the first row of the truth table, as discussed in Section 3. The analytic solution of the AND gate equation, with initial output concentration \( x_C(0) = 0 \), which is a lower bound on any solution with larger initial conditions, hence represents the worst case for the considered scenario is:

\[ x_C(t) = \frac{x_A^n}{K_{AC}^n + x_A^n} \cdot \frac{x_B^n}{K_{BC}^n + x_B^n}(1 - e^{-\alpha t}). \]  (5)

The STL formula for the fourth row is:

\[ G_{[0,\lambda+\delta]}(x_A \geq \theta_A^+ \land x_B \geq \theta_B^+) \rightarrow F_{[0,\delta]}G_{[0,\lambda]}(x_C \geq \theta_C^+). \]  (6)

If we fix \( x_A = \theta_A^+ \), \( x_B = \theta_B^+ \), \( x_C(0) = 0 \), the formula is satisfied if and only if

\[ F_{[0,\delta]}G_{[0,\lambda]}(x_C \geq \theta_C^+). \]

Now, the solution (5) is a monotonic increasing function converging to the steady state value \( x_C(\infty) = K \). It follows that if \( K \geq \theta_C^+ \) and \( x(\delta) \geq \theta_C^+ \), the STL formula is satisfied (the second condition guarantees that the threshold is crossed no later than \( \delta \) time units). In a similar way it is possible to derive a system of inequalities for all the other STL constraints considered.

**Bounding the degradation constant.** We first discuss how to bound the degradation constant. In particular, we will provide a generic bound, holding for all basic logic gates considered. Fix the thresholds \( \theta_+ \) (high concentration) and \( \theta_- \) (low concentration) for the output and the maximum time delay \( \delta \). We need to consider two cases:

- Case \( x_0 = 0 \) and \( x(\delta) \geq \theta_+ \). Here we want to upper bound by \( \delta \) the time at which \( x \) crosses the high concentration threshold \( \theta_+ \). Now, for the solution \( x(t) \) to eventually become bigger than the threshold \( \theta_+ \), we need \( K > \theta_+ \). We can enforce a stricter constraint by setting \( K \geq \theta_+(1 + p) \) for \( p > 0 \), which guarantees that the threshold is crossed in finite time. From equation (4) we get

\[ K(1 - e^{-\alpha \delta}) \geq \theta_+ \quad \text{for} \quad 1 \geq K \geq \theta_+(1 + p), \]

thus

\[ \alpha \geq \frac{1}{\delta} \log \left( \frac{K}{K - \theta_+} \right) \quad \text{for} \quad 1 \geq K \geq \theta_+(1 + p), \]

This inequality holds independently of \( K \) if and only if:

\[ \alpha \geq \frac{1}{\delta} \log \left( \frac{1}{p\theta_+} \right) \]
Case $x_0 = 1$ and $x(\delta) \leq \theta_-$. In this case, we want to upper bound by $\delta$ the time it takes for the solution to fall below the threshold $\theta_- < \theta_+$. In this case, we require $K \leq (1 - p)\theta_-, p > 0$, so that this time is bounded. From equation (4), we obtain:

$$K + (1 - K) \cdot e^{-\alpha \delta} \leq \theta_- \quad \text{for } 0 < K \leq (1 - p)\theta_-,$$

resulting in

$$\alpha \geq \frac{1}{\delta} \log \left( \frac{1 - K}{\theta_- - K} \right) \quad \text{for } 0 < K \leq (1 - p)\theta_-,$$

holding independently of $K$ if and only if:

$$\alpha \geq \frac{1}{\delta} \log \left( \frac{1}{p\theta_-} \right)$$

As $\theta_- < \theta_+$, intersecting the two conditions on $\alpha$ we obtain

$$\alpha \geq \frac{1}{\delta} \log \left( \frac{1}{p\theta_-} \right)$$

(7)

**AND gate.** We consider now the constraints specific to an AND gate. The ODE systems of the AND gate is:

$$\begin{cases}
\frac{dx_C}{dt} = \alpha_C \cdot \frac{x_A^n}{K_{AC}^n + x_A^n} \cdot \frac{x_B^n}{K_{BC}^n + x_B^n} - \alpha_C \cdot x_C, \\
x_C(0) = x_{C0};
\end{cases}$$

where $x_A$ and $x_B$ are the concentrations of the inputs $A$ and $B$, $K_{AC}$ and $K_{BC}$ are the concentration thresholds of $A$ and $B$ to activate the production of $C$, $n$ is the Hill coefficient.

According to the discussion of the paper, we will fix the value of $x_A$ and $x_B$ to a constant, either their activation thresholds $\theta_A^+$ and $\theta_B^+$, or their deactivation thresholds $\theta_A^-$ and $\theta_B^-$, or the maximum steady state level $\gamma_A$ and $\gamma_B$. We set $K_A^C = \frac{x_A^n}{K_{AC}^n + x_A^n}$, $K_B^C = \frac{x_B^n}{K_{BC}^n + x_B^n}$.

We fix the output concentration thresholds $\theta_{C+}$ and $\theta_{C-}$ and the maximum delay time $\delta$.

Invoking the same argument used for $\alpha$, we will consider new threshold $\hat{\theta}_{C+} = (1 + p)\theta_{C+}$ and $\hat{\theta}_{C-} = (1 - p)\theta_{C-}$, and use those to bound the steady state of the ODE system. This guarantees the existence of a lower bound for $\alpha$, independently of $K_{AC}$ and $K_{BC}$.

Now we introduce two methods to find the subspace of the parameters for which the AND gate module satisfies all the four STL formulae, associated with the four rows of the extended truth table. The first method is more intuitive and considers only hyper-cubic subspaces in the parameter space, at the price of discarding a lot of admissible values. This strong approximation is dropped in the second method, which results to be formally more accurate, but computationally more difficult.
Method 1: We treat the four STL conditions separately.

- Case 1 \((x_A = \theta_{A^+}, x_B = \theta_{B^+}, x_C(0) = 0)\). Notice that we fix \(x_C(0) = 0\) as, by monotonicity of the solution, the corresponding trajectory is a lower bound on the trajectories starting from \(x_C(0) > 0\). In this case, the steady state of the ODE, which is equal to \(K\), will be above the activation threshold if and only if

\[
K \geq \hat{\theta}_{C^+}.
\]

This corresponds to the following condition

\[
\theta^n_A + \theta^n_B - \hat{\theta}_{C^+} (K_{AC}^n + \theta^n_{A^+}) \cdot (K_{BC}^n + \theta^n_{B^+}) \geq 0,
\]

which can be rewritten as:

\[
(K_{AC}^n + \theta^n_{A^+}) \cdot (K_{BC}^n + \theta^n_{B^+}) \leq \frac{\theta^n_A}{\hat{\theta}_{C^+}} \cdot \frac{\theta^n_B}{\hat{\theta}_{C^+}}.
\]

Now, as all quantities involved are positive, the previous inequality holds if both

\[
(K_{AC}^n + \theta^n_{A^+}) \leq \frac{\theta^n_A}{\hat{\theta}_{C^+}}
\]

and

\[
(K_{BC}^n + \theta^n_{B^+}) \leq \frac{\theta^n_B}{\hat{\theta}_{C^+}}
\]

are true. We therefore obtain the following conditions on \(K_{AC}\) and \(K_{BC}\):

\[
\left\{ K_{AC}^n \leq \theta^n_A (1 - \hat{\theta}_{C^+}/(\hat{\theta}_{C^+}^2)), \quad K_{BC}^n \leq \theta^n_B (1 - \hat{\theta}_{B^+}/(\hat{\theta}_{C^+}^2)) \right\}
\]

- Case 2 \((x_A = \theta_{A^-}, x_B = \gamma_B, x_C(0) = 1)\). In this case, we chose \(x_C(0) = 1\) because this trajectory is an upper bound for all trajectories starting in \(x_C(0) < 1\). We need to impose the condition

\[
K \leq \hat{\theta}_{C^-},
\]

which is expanded as

\[
\frac{\theta^n_A}{K_{AC}^n + \theta^n_{A^-}} \cdot \frac{\gamma^n_B}{K_{BC}^n + \gamma^n_B} \leq \hat{\theta}_{C^-},
\]

Now, as \(\frac{\gamma^n_B}{K_{BC}^n + \gamma^n_B} \leq 1\), the previous condition is satisfied by requiring

\[
\frac{\theta^n_A}{K_{AC}^n + \theta^n_{A^-}} \leq \hat{\theta}_{C^-},
\]

which turns into the following condition for \(K_{AC}\):

\[
K_{AC}^n \geq \theta^n_A \frac{1 - \hat{\theta}_{C^-}}{\hat{\theta}_{C^-}}.
\]
- Case 3 \( (x_A = \gamma_A, x_B = \theta_B^-, x_C(0) = 1) \). In this case the condition is also \( K \leq \theta_C^- \). Reasoning symmetrically as in case 2, we then obtain:

\[
K_{BC}^n \geq \theta_B^- \frac{1 - \hat{\theta}_C^-}{\theta_C^-}
\]

- Case 4 \( (x_A = \theta_A^-, x_B = \theta_B^-, x_C(0) = 1) \). Here we also have to enforce \( K \leq \theta_C^- \), which however holds true if the condition for case 2 or that for case 3 holds.

**Intersection.** Intersecting the conditions from case 1 to 4, we get the following bounds on \( K_{AC} \) and \( K_{BC} \):

\[
\theta_A^- \left(1 - \frac{\hat{\theta}_C^-}{\theta_C^-}\right) \leq K_{AC} \leq \theta_A^+ \left(1 - \frac{\hat{\theta}_C^+}{\theta_C^+}\right)
\]

\[
\theta_B^- \left(1 - \frac{\hat{\theta}_C^-}{\theta_C^-}\right) \leq K_{BC} \leq \theta_B^+ \left(1 - \frac{\hat{\theta}_C^+}{\theta_C^+}\right)
\]

The previous constraints are not void if and only if:

\[
\theta_A^- \frac{1 - \hat{\theta}_C^-}{\theta_C^-} \leq \theta_A^+ \frac{1 - \hat{\theta}_C^+}{\theta_C^+}
\]

and

\[
\theta_B^- \frac{1 - \hat{\theta}_C^-}{\theta_C^-} \leq \theta_B^+ \frac{1 - \hat{\theta}_C^+}{\theta_C^+},
\]

giving the following constraint on \( n \):

\[
n \geq \frac{1}{\min\{\log(\theta_B^-/\theta_A^-), \log(\theta_A^+/\theta_B^-)\}} \log \left(\frac{\frac{\hat{\theta}_C^+}{\theta_C^+} \cdot 1 - \frac{\hat{\theta}_C^-}{\theta_C^-}}{\theta_C^- (1 - \frac{\hat{\theta}_C^+}{\theta_C^+})}\right).
\]

**Method 2:** We provide now more precise bounds for \( K_{AC} \) and \( K_{BC} \).

- Case 1 \( (x_A = \theta_A^+, x_B = \theta_B^+, x_C(0) = 0) \). We study the inequality:

\[
K \geq \theta_C^+,
\]

that is

\[
\frac{\theta_{AC}^n}{K_{AC}^n + \theta_{A+}^n} \cdot \frac{\theta_{BC}^n}{K_{BC}^n + \theta_{B+}^n} \geq \hat{\theta}_C^+.
\]

Note that, since \( \frac{\theta_{AC}^n}{K_{AC}^n + \theta_{A+}^n} \leq 1 \) and \( \frac{\theta_{BC}^n}{K_{BC}^n + \theta_{B+}^n} \leq 1 \), there exists a solution if and only if:

\[
\left\{ \frac{\theta_{AC}^n}{K_{AC}^n + \theta_{A+}^n} \geq \hat{\theta}_C^+, \frac{\theta_{BC}^n}{K_{BC}^n + \theta_{B+}^n} \geq \hat{\theta}_C^+ \right\},
\]

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i.e. if and only if
\[
\left\{ 0 \leq K_{AC} \leq \theta_{A^+} \left( \frac{1 - \hat{\theta}_{C^+}}{\theta_{C^+}} \right)^{\frac{1}{n}}, 0 \leq K_{BC} \leq \theta_{B^+} \left( \frac{1 - \hat{\theta}_{C^+}}{\theta_{C^+}} \right)^{\frac{1}{n}} \right\}
\]

Now, within this rectangle, we need to restrict to the region below the curve
\[
K_{AC} = \theta_{A^+} \left( \frac{\theta_{B^+}^n}{\theta_{C^+} (K_{BC}^n + \theta_{B^+}^n)} - 1 \right)^{\frac{1}{n}}.
\]

Hence, the set of parameters satisfying case 1 is characterised by
\[
\left\{ K_{AC} \leq \theta_{A^+} \left( \frac{1 - \hat{\theta}_{C^+}}{\theta_{C^+}} \right)^{\frac{1}{n}}, K_{BC} \leq \theta_{B^+} \left( \frac{1 - \hat{\theta}_{C^+}}{\theta_{C^+}} \right)^{\frac{1}{n}} \right\} \cap \left\{ K_{AC}^n \leq \theta_{A^+} \left( \frac{\theta_{B^+}^n}{\theta_{C^+} (K_{BC}^n + \theta_{B^+}^n)} - 1 \right)^{\frac{1}{n}} \right\}
\]

- Case 2 \((x_A = \theta_{A^+}, x_B = \gamma_B, x_C(0) = 1)\): We have to enforce the inequality:

\[
K \leq \hat{\theta}_{C^-},
\]

i.e.
\[
\frac{\theta_{A^-}^n}{K_{AC}^n + \theta_{A^-}^n}, \frac{\gamma_B^n}{K_{BC}^n + \gamma_B^n} \leq \hat{\theta}_{C^-}.
\]

First note that because \(\frac{\theta_{A^-}^n}{K_{AC}^n + \theta_{A^-}^n} \leq 1\) and \(\frac{\gamma_B^n}{K_{BC}^n + \gamma_B^n} \leq 1\), the truth of if \(\frac{\theta_{A^-}^n}{K_{AC}^n + \theta_{A^-}^n} \leq \hat{\theta}_{C^-}\) or \(\frac{\gamma_B^n}{K_{BC}^n + \gamma_B^n} \leq \hat{\theta}_{C^-}\) implies the satisfaction of the target inequality. Therefore
\[
\left\{ K_{AC} \geq \theta_{A^-} \left( \frac{1 - \hat{\theta}_{C^-}}{\theta_{C^-}} \right)^{\frac{1}{n}} \right\} \cup \left\{ K_{BC} \geq \gamma_B \left( \frac{1 - \hat{\theta}_{C^-}}{\theta_{C^-}} \right)^{\frac{1}{n}} \right\}
\]
is a subspace of the parameter space in which the inequality is true. In the remaining subspace
\[
\left\{ K_{AC} < \theta_{A^-} \left( \frac{1 - \hat{\theta}_{C^-}}{\theta_{C^-}} \right)^{\frac{1}{n}}, K_{BC} < \gamma_B \left( \frac{1 - \hat{\theta}_{C^-}}{\theta_{C^-}} \right)^{\frac{1}{n}} \right\},
\]

we need to restrict to the region above the curve
\[
K_{AC} = \theta_{A^-} \left( \frac{\gamma_B^n}{\theta_{C^-} (K_{BC}^n + \gamma_B^n)} - 1 \right)^{\frac{1}{n}}.
\]

Hence, the set of parameters satisfying case 2 is
\[
\left\{ K_{AC} \geq \theta_{A^-} \left( \frac{1 - \hat{\theta}_{C^-}}{\theta_{C^-}} \right)^{\frac{1}{n}} \right\} \cup \left\{ K_{BC} \geq \gamma_B \left( \frac{1 - \hat{\theta}_{C^-}}{\theta_{C^-}} \right)^{\frac{1}{n}} \right\} \cup
\]

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\[ \bigcup \{ K_{AC} < \theta_A - \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} , K_{BC} < \gamma_B \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} \}, \]

\[ K_{AC} \geq \theta_A - \left( \frac{\gamma_B}{\theta_C - (K_{BC}^n + \gamma_B^n)} - 1 \right)^{\frac{1}{\gamma}} \],

- Case 3 \((x_A = \gamma_A, x_B = \theta_B, x_C(0) = 1)\): this case is symmetric to case 2, just switching the role of input variables. We then obtain the following set of parameters

\[ \bigcup \{ K_{AC} \geq \gamma_A \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} \} \cup \{ K_{BC} \geq \theta_B - \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} \} \bigcup \]

\[ \bigcup \{ K_{AC} < \gamma_A \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} , K_{BC} < \theta_B - \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} \}, \]

\[ K_{AC} \geq \gamma_A \left( \frac{\theta_B^n}{\theta_C - (K_{BC}^n + \theta_B^n)} - 1 \right)^{\frac{1}{\gamma}} \],

- Case 4 \((x_A = \theta_A, x_B = \theta_B, x_C(0) = 1)\): A similar argument to case 2 can be used here to obtain the following parameter set

\[ \bigcup \{ K_{AC} \geq \theta_A - \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} \} \cup \{ K_{BC} \geq \theta_B - \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} \} \bigcup \]

\[ \bigcup \{ K_{AC} < \theta_A - \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} , K_{BC} < \theta_B - \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} \}, \]

\[ K_{AC} \geq \theta_A - \left( \frac{\theta_B^n}{\theta_C - (K_{BC}^n + \theta_B^n)} - 1 \right)^{\frac{1}{\gamma}} \].

**Intersection.** The intersection of the conditions of cases 2, 3, and 4 gives:

\[ \bigcup \{ K_{AC} \geq \theta_A - \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} , K_{BC} \geq \theta_B - \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} \} \bigcup \]

\[ \bigcup \{ K_{BC} < \theta_B - \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} \}, \]

\[ K_{AC} \geq \max \left( \theta_A - \left( \frac{\gamma_B}{\theta_C - (K_{BC}^n + \gamma_B^n)} - 1 \right)^{\frac{1}{\gamma}} , \gamma_A \left( \frac{\theta_B^n}{\theta_C - (K_{BC}^n + \theta_B^n)} - 1 \right)^{\frac{1}{\gamma}} \right) \bigcup \]

\[ \bigcup \{ K_{BC} \geq \theta_B - \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} , K_{AC} < \theta_A - \left( \frac{1 - \hat{\theta}_C}{\theta_C} \right)^{\frac{1}{\gamma}} \}, \]

\[ K_{AC} \geq \theta_A - \left( \frac{\gamma_B}{\theta_C - (K_{BC}^n + \gamma_B^n)} - 1 \right)^{\frac{1}{\gamma}} \].
Numerical example. Let \( \theta_+ = 2/3 \) and \( \theta_- = 1/3 \) for all species \( A, B, \) and \( C, \gamma_A = \gamma_B = 1 \) and \( p = 0.1. \) Applying the bounds of the first method, we obtain

\[
\frac{1}{\min\{\log(\frac{\theta_A^0}{\theta_A^-}), \log(\frac{\theta_A^0}{\theta_A^+})\}} \log \left( \frac{\theta_A^+}{\theta_A^-} \cdot \frac{1 - \theta_C^-}{1 - \theta_C^+} \right)
\]

\[
n \geq 3.798
\]

Then, setting for instance \( n = 4 \), we get

\[
0.4120 \leq K_{AC} \leq 0.4267
\]

and a similar value for \( K_{BC} \).
The second method gives us $n \geq 2.6818$.

If we set again $n = 4$, for comparison, the subspace of parameters for which the four STL properties are satisfied is given by the region delimited by the three following curves:

\[ K_{AC} = \theta_{A+} \left( \frac{\theta_B^n}{\theta_{C+}(K_{BC}^n + \theta_B^n)} - 1 \right)^{\frac{1}{n}} \]

\[ K_{AC} = \theta_{A-} \left( \frac{\gamma_B^n}{\theta_{C-}(K_{BC}^n + \gamma_B^n)} - 1 \right)^{\frac{1}{n}} \]

\[ K_{AC} = \gamma_A \left( \frac{\theta_B^n}{\theta_{C-}(K_{BC}^n + \theta_B^n)} - 1 \right)^{\frac{1}{n}} \]

This region is visually depicted in Figure 4. We can observe that the box identified by the first method is strictly included in the set provided by the second method.

![Figure 4](image-url)
If we set the thresholds to $\theta_+ = 3/4$ and $\theta_- = 1/4$, the first method gives us $n \geq 3.2129$, so that for $n = 4$, we obtain $0.3406 \leq K_{AC}, K_{BC} \leq 0.4228$, hence a larger interval. The validity domain found by the second approach, instead, is represented in Figure 5. Also in this case, the region is larger.

**Fig. 5.** The grey region inside the intersection of the curves $K_{AC} = \theta_A^+ \left( \frac{\theta_{n+} - \gamma B}{\gamma_B - (K_{BC} + \gamma B)} \right) - 1$ (in blue), $K_{AC} = \theta_A^- \left( \frac{\gamma B}{\gamma_B - (K_{BC} + \gamma B)} \right) - 1$ (in red) and $K_{AC} = \gamma_A \left( \frac{\theta_{n-} - \gamma_B}{\gamma_B - (K_{BC} + \gamma_B)} \right) - 1$ (in green) is the validity domain of the parameters $K_{AC}$ and $K_{BC}$ for $\theta_+ = 3/4$ and $\theta_- = 1/4$. The black region is the one identified by the first method.

Finally, we can compute the lower bound for the degradation constant $\alpha$, according to equation (7). For the thresholds $\theta_+ = 3/4$ and $\theta_- = 1/4$, we have $\alpha \geq \frac{3.4102}{3}$, while for $\theta_- = 1/3$ and $\theta_+ = 2/3$, we have $\alpha \geq \frac{3.6880}{5}$.

**NOT gate.** The differential equations for the NOT gate are

$$\begin{align*}
\frac{dx_D}{dt} &= \alpha_D K - \alpha_D \cdot x_D, \\
x_D(0) &= x_D(0),
\end{align*}$$

where

$$K = \frac{1}{1 + \left( \frac{\sigma B}{K_{BD}} \right)^n}$$
We fix the output concentration thresholds $\theta_{D^+}, \theta_{D^-}$ and the constant $p > 0$, and consider separately the two STL conditions. $\theta_{D^\pm}$ are defined as in the previous section.

1. Case 1 ($x_B = \theta_{B^-}, x_D(0) = 0$): Here we need to enforce the condition $K \geq \hat{\theta}_{D^+}$, which results in

$$K_{BD}^n \geq \frac{\hat{\theta}_{D^+} \theta_{B^-}^n}{1 - \theta_{D^+}}.$$ 

2. Case 2 ($x_B = \theta_{B^+}, x_D(0) = x_{D^0}$): The condition $K \leq \hat{\theta}_{D^-}$, gives us

$$K_{BD}^n \leq \frac{\hat{\theta}_{D^-} \theta_{B^+}^n}{1 - \theta_{D^-}}.$$ 

Taking the intersection, and imposing that the resulting set is non-void, we get

$$n \geq \frac{1}{\log(\theta_{B^-})} \log \left(\frac{\hat{\theta}_{D^+} 1 - \hat{\theta}_{D^-}}{\hat{\theta}_{D^-} 1 - \theta_{D^+}}\right)$$

and

$$\theta_{B^-} \left(\frac{\hat{\theta}_{D^+}}{1 - \hat{\theta}_{D^+}}\right)^\frac{1}{n} \leq K_{BD} \leq \theta_{B^+} \left(\frac{\hat{\theta}_{D^-}}{1 - \hat{\theta}_{D^-}}\right)^\frac{1}{n}.$$ 

**OR gate.** The ODE systems for the OR gate is:

\[
\begin{cases}
\frac{dx_S}{dt} = \alpha_S \cdot \frac{(xE_{KES})^n + (xG_{KGS})^n}{1 + (xE_{KES})^n + (xG_{KGS})^n} - \alpha_S \cdot x_S, \\
x_S(0) = x_{S_0},
\end{cases}
\]

with $K$ now defined as

$$K = \frac{(xE_{KES})^n + (xG_{KGS})^n}{1 + (xE_{KES})^n + (xG_{KGS})^n}.$$ 

We can obtain the constraints for the parameters using an approach similar to the one of the AND gate, for a fixed set of activation thresholds $\theta_{S^-}$ and $\theta_{S^+}$. Note that

$$K = \theta \text{ iff } (\frac{xE_{KES}}{K_{E}})^n + (\frac{xG_{KGS}}{K_{S}})^n = \frac{\theta}{1 - \theta}.$$ 

We have two possible methods also in this case, one stricter, giving an hyperbox, and one less strict, resulting in a curved region.

Remember that, due to Proposition II if the input $x_J$ is low and the output $x_O$ is high then the worst-case input signal is $\hat{x}_J = 0$; Hence, the analytic treatment of the corresponding cases is very simple.
Method 1. For the parameters $K_{ES}$ and $K_{GS}$ we obtain the following bounds:

$$\theta_E - \left(\frac{1}{2} - \hat{\theta}_S^-\right)^{1/n} \leq K_{ES} \leq \theta_E^+ \left(\frac{1}{2} - \hat{\theta}_S^+\right)^{1/n}$$

$$\theta_G - \left(\frac{1}{2} - \hat{\theta}_S^-\right)^{1/n} \leq K_{GS} \leq \theta_G^+ \left(\frac{1}{2} - \hat{\theta}_S^+\right)^{1/n},$$

resulting in the following constraint on $n$:

$$n \geq \min\{\log(\theta_G^+), \log(\theta_E^+)\} \cdot \log \left(\frac{\hat{\theta}_S^+}{\hat{\theta}_S^-} \cdot \frac{2 - 2\hat{\theta}_S^-}{1 - \hat{\theta}_S^-}\right).$$

Method 2. A more refined analysis gives us the following set of parameters:

$$\left\{ \theta^E - \left(\frac{1}{2} - \hat{\theta}_S^-\right)^{1/n} \right\}^\dagger \leq K_{ES} \leq \theta^E^+ \left(\frac{1}{2} - \hat{\theta}_S^+\right)^{1/n},$$

$$\theta^G - \left(\frac{1}{2} - \hat{\theta}_S^-\right)^{1/n} \leq K_{GS} \leq \theta^G^+ \left(\frac{1}{2} - \hat{\theta}_S^+\right)^{1/n},$$

$$K_{ES} \geq \theta^E - \left(\frac{1}{2} - \hat{\theta}_S^-\right)^{1/n} \left(\frac{1}{2} - \hat{\theta}_S^-\right)^{\pi/n}.$$ 

We also obtain the following constraint on the parameter $n$:

$$n > \min\{\log(\hat{\theta}_G^+), \log(\hat{\theta}_E^+))\} \cdot \log \left(\frac{\hat{\theta}_S^+}{\hat{\theta}_S^-} \cdot \frac{1 - \hat{\theta}_S^-}{1 - \hat{\theta}_S^+}\right).$$

In Figure 6 we compare the two validity sets for $\theta_S^- = 1/4$ and $\theta_S^+ = 3/4$, $p = 0.1$, $n = 3$.
Fig. 6. The grey region inside the intersection of the curves $K_{ES} = \theta_E - \left( \frac{1}{\theta_S - 1} - \frac{\tilde{\theta}_S - 1}{\tilde{\theta}_S - 1} \right)^{\frac{1}{n}}$ (in blue), $K_{GS} = \theta_G \left( \frac{1-\tilde{\theta}_S}{\tilde{\theta}_S} \right)^{\frac{1}{n}}$ (in green) and $K_{ES} = \theta_E + \left( \frac{1-\tilde{\theta}_S}{\tilde{\theta}_S} \right)^{\frac{1}{n}}$ (in red) is the validity domain of the parameters $K_{AC}$ and $K_{BC}$ for $\theta_+ = 3/4$ and $\theta_- = 1/4$. The black region is the one identified by the first method.