Optimal Design of Bidirectional PFC Rectifiers and Inverters Considering 2L and 3L Topologies with Si, SiC, and GaN Switches

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Power factor correction converters are widely used in industrial drive systems. Several different configurations and topologies exist for such converters and it is difficult to choose one. Therefore, in this work, a comprehensive selection of possible configurations are optimized and compared against each other. The analysis shows the important aspects of converter design and how the semiconductor technology used (Si, SiC, and GaN) affects the total converter volume. A sensitivity analysis of certain power semiconductor parameters is performed to highlight the benefit of possible future developments of components and materials. In addition, the differences between the rectifier stage, where an electromagnetic interference filter stage is necessary, and the inverter stage, where the harmonic motor losses are influenced by the modulation scheme, are presented.

Keywords: three-phase system, modulation strategy, power factor correction, EMC/EMI

1. Introduction

In industrial drive systems, bidirectional 3-phase boost Power Factor Correction (PFC) converters are widely used to supply electrical motors via a DC link from the mains (Fig. 1). The main goal of the converter is a power flow in both directions (i.e. accelerating and decelerating the motor).

The PFC rectifier has to ensure a high power factor and has to comply with harmonic regulations at low frequencies \(f \leq 700\) Hz, LF) and electromagnetic interference (EMI) regulations at high frequencies \(150\) kHz \(\leq f \leq 30\) MHz, HF) (1). Applying a suitable modulation scheme with a sufficiently high switching frequency ensures that the rectifier complies with the LF regulations. However, the HF noise has to be attenuated by an additional EMI filter, which has a considerable impact on the converter volume (2).

The design of a PFC rectifier can be focused on various aspects, for example on the EMI filter (3), the switching losses (4) or the common mode (CM) voltage generation (5). However, if the focus is only set on one of these aspects, it could worsen other aspects and the overall system design. Therefore, a comprehensive converter optimization analyses the impact of the topology and the modulation scheme on the total converter volume (i.e. the volume of the EMI filter, boost inductor, heat sink and DC link capacitors), including an analysis of the benefit of using SiC semiconductors (6). Also the benefit of using PCB embedded semiconductors has been analysed (7).

In this paper, the analysis will additionally include GaN devices and a sensitivity analysis on several semiconductor parameters to investigate the benefit on the system level of possible future developments of components and materials.

For the EMI filter, different damping topologies and CM configurations are analysed.

As the inverter stage use similar topologies and modulation schemes, the same considerations can be done, except for the EMI filter which is not necessary. However, not only the semiconductor losses have to be considered, but also the harmonic motor losses that depend on the applied modulation scheme (8) and the bearing currents which are a side effect of the generated CM voltage of the converter which can cause bearing failures (9). In this paper an optimization of the inverter will be proposed, regarding the aforementioned aspects.

Section 2 describes the investigated topologies and modulation schemes. In Sect. 3, the EMI filter design is outlined and Sect. 4 shows the optimization procedure. In Sect. 5, the models are validated with an experimental boost PFC rectifier and Sect. 6 presents the optimization results.

2. Topologies and Modulation Schemes

The topology and modulation scheme are the major design choices for a PFC converter. A controller sets an LF reference voltage of \(V_{\text{conv}}\) in the simplified differential mode (DM) equivalent circuit shown in Fig. 2 to ensure the control of bidirectional power (10). The choice of topology and
modulation scheme does not affect this LF voltage and therefore the controllability, but only the HF spectrum of the converter voltage, which has to be attenuated by the EMI filter (Sect. 3). In Sect. 2.1, the investigated topologies are presented, followed by Sect. 2.2 with an overview of the investigated modulation schemes.

2.1 Topologies

Figure 3 shows the investigated topologies. The respective advantages and disadvantages are discussed in the following.

2.1.1 2-level

The 2-level (2L) topology offers low conduction losses and low costs as the amount of power semiconductors is small. The disadvantage are high switching losses, only two voltage levels which affects the EMI filter volume considerably and a high power loss per power semiconductor device.

2.1.2 3-level Neutral Point Clamped

The 3-level Neutral Point Clamped (3L-NPC) topology has the lowest switching losses and a good loss distribution among the power semiconductor devices. The three voltage levels lead to a smaller EMI filter compared to the 2-level topology. The disadvantage are high conduction losses as there are always two power semiconductor devices conducting the current.

2.1.3 3-level T-Type

The 3-level T-Type (3L-TT) topology is a compromise between a 2-level topology and a 3-level NPC topology. The conduction losses are lower compared to the NPC topology as sometimes only one power semiconductor device is carrying the current, but the switching losses are higher as the switches $S_1/S_4$ have a higher voltage rating than in the NPC topology.

2.2 Modulation Schemes

Depending on the chosen topology, different modulation schemes can be applied. Figure 4 shows the space vector plane of a 2-level converter and sector I of the 3-level space vector plane. For the modulation scheme. For the 3-level converter even more degrees of freedom are present. In the following the investigated modulation schemes are shortly described in the space vector modulation (SVM) and the advantages and disadvantages are outlined.

2.2.1 2L Sinusoidal

In the 2L Sinusoidal ($2L$-Sin) modulation scheme, the phase voltages follow a sinusoidal reference (11). Translated into the SVM, the distribution of the space vectors $(ppp)$ and $(nnn)$ is chosen so that the average CM voltage over a switching period is zero. The main disadvantage of this modulation scheme are the high switching losses.

2.2.2 2L Clamping

In the 2L Clamping ($2L$-C) modulation scheme, the phase with the highest current is clamped to either positive or negative DC link voltage during one switching period (11). For the example reference vector given in Fig. 4(a) and for the assumption that phase 1 has the highest current, space vector $(nnn)$ would be omitted. On one hand this reduces the switching losses considerably, on the other hand the DM peak at the switching frequency is higher than in the $2L$-Sin modulation scheme (cf. Fig. 5), thereby increasing the EMI filter.

2.2.3 3L Sinusoidal

Similar to the $2L$-Sin modulation scheme, in the 3L Sinusoidal (3L-Sin) modulation scheme the phase voltages follow a sinusoidal reference and no CM voltage below the switching frequency is generated. However, the neutral point current $i_{np}$ (cf. Fig. 3) is not actively balanced, why a relatively big DC link capacitor is required (6).

2.2.4 3L Optimal Clamping

In the 3L Optimal Clamping (3L-OC) modulation scheme, the phase with the highest current is clamped, thereby reducing the switching losses (4). The disadvantage is the generation of a CM voltage below the switching frequency, a high DM peak at the switching frequency (cf. Fig. 5) and an unbalance of the neutral
point of the DC link, resulting in a big DC link capacitor.\footnote{10}

2.2.5 3L Clamping In the 3L Clamping (3L-C) modulation scheme, a controller for the neutral point voltage of the DC link decides if the phase with the highest or the second-highest current is clamped\footnote{12}, as these two possibilities either charge or discharge the neutral point of the DC link. Compared to the 3L-OC modulation scheme, the DC link capacitor volume is reduced at the price of increased switching losses.

2.2.6 3L Neutral-Point Balanced In the 3L Neutral-Point Balanced (3L-NPB) modulation scheme, the average current to the neutral point of the DC link $i_{\text{avg}}$ (cf. Fig. 3) is controlled to zero in the average of a switching period\footnote{13}. The switching losses are higher compared to the 3L-OC and 3L-C modulation scheme, but due to the DC neutral point balancing the DC link capacitor is smaller and the lower DM peak (cf. Fig. 5) reduces the EMI filter volume.

Based on the chosen topology and modulation scheme in combination with the EMI filter respectively the motor, the voltage and current forms can be calculated. For the rectifier, the EMI filter design (explained in Sect. 3) is optimized with respect to the total converter volume (cf. Sect. 4.1). For the inverter, the harmonic losses of the motor and the power semiconductor losses are evaluated as explained in Sect. 4.2.

3. EMI Filter

At the grid connection of the rectifier stage, the current has to be filtered in order to fulfill the EMI regulations. Section 3.1 describes the standards which are considered, Sect. 3.2 shows the investigated damping topologies for the DM filter and in Sect. 3.3 the investigated CM filter topologies are shown.

3.1 EMI Standards The EN 61000-3-12 standard is used for the LF and total harmonic distortion limits, while the CISPR 11 class A standard is used for the HF limits. In between, a logarithmic linear function is used as a standard in this medium frequency (MF) range could be expected in the future\footnote{1}. Figure 6 shows the applied limits.

Generally, the DM filter consists of a LCL structure as indicated in Fig. 7 in the equivalent circuit for one phase. One trade-off in the filter design is the value of the boost inductance $L_b$. The higher it is, the higher the boost inductor voltage becomes and the lower the other filter elements become and vice versa and is therefore optimized as explained in Sect. 4.1. The resonance frequency

$$\omega_0 = \frac{1}{\sqrt{L_b C_f}} \tag{1}$$

would lead to an unstable behaviour of the converter, therefore a damping network is required as explained in the next section.

3.2 Damping Topologies To avoid that the EMI filter affects the converter control, Middlebrook’s stability criterion\footnote{13,14} has to be fulfilled, i.e. the filter output impedance has to be smaller than the converter input impedance. The criterion has been extended to 3-phase systems\footnote{15}. Figure 8 shows the investigated damping topologies. These damping topologies have been analysed and it has been shown that the volume of the parallel-RL damping (Fig. 8(b)) leads always to a smaller volume than the serial-RL damping (Fig. 8(d)), while serial-RC and parallel-RC (Fig. 8(a) respectively c) lead to the same volume\footnote{16}. Therefore, only the parallel-RC and the parallel-RL damping are considered in this paper.

3.3 CM Filter Topologies Figure 9 shows the CM equivalent circuit of a three-phase boost PFC converter. The CM voltage source $V_{\text{conv,CM}}$ depends on the chosen topology and modulation scheme. $C_{\text{CM}}$ is the equivalent capacitance from the two DC link poles to ground and $C_{\text{CM}}$ is the parasitic capacitance from the power semiconductors to the grounded heat sink. The CM inductor $L_{\text{CM}}$ can either be placed on the grid or the converter side. If it is placed on the grid side, there are no HF DM currents which would generate additional losses. On the other hand if it is placed on the converter side, the CM damping is higher. The CM capacitor $C_{\text{CM}}$ can either be connected with the neutral point of the DC link or with ground. Therefore, four configurations are investigated:

3.3.1 CM Filter Topology 1 $L_{\text{CM}}$ is placed on the grid side (A-A2) and $C_{\text{CM}}$ is connected to the DC link midpoint (B-B1).
3.3.2 CM Filter Topology 2  $L_{CM}$ is placed on the converter side (A-A₁) and $C_{CM}$ is connected to the DC link midpoint (B-B₁).

3.3.3 CM Filter Topology 3 $L_{CM}$ is placed on the grid side (A-A₂) and $C_{CM}$ is connected to ground (B-B₂).

3.3.4 CM Filter Topology 4 $L_{CM}$ is placed on the converter side (A-A₁) and $C_{CM}$ is connected to ground (B-B₂).

3.4 Example Configuration Figure 10 shows the 3-phase equivalent circuit of the experimental setup in Sect. 5. It consists of a 3-level TT topology, a DM filter with parallel-RL damping and CM filter topology 1.

4. Optimization Procedure

Based on the chosen topology and power semiconductor devices, modulation scheme, damping topology and CM filter topology, the design parameters of the converter are optimized for maximal power density in order to derive the dependency of the converter volume on the switching frequency. Section 4.1 describes the optimization routine for the rectifier stage and Sect. 4.2 for the inverter stage. In Sect. 4.3 the volume estimation for the different converter components is explained.

4.1 Rectifier Optimization Procedure The considered optimization procedure shown in Fig. 11 has been presented in a previous work and is used to identify the switching frequency and CM and DM filter design parameters which lead to the lowest converter volume. The input of the optimization is the system specification which includes the AC and DC voltage, the output power, the inductor and capacitor materials and the topology including semiconductor devices and modulation scheme. For reducing the computing time, the optimization routine is implemented in a cascaded structure. The following DM filter design parameters are optimized:

1. The boost inductance value $L_b$ (trade-off between boost inductor volume and filter volume).
2. The filter resonance frequency $\omega_0$ (trade-off between filter volume and attenuation).
3. The frequency location of the maximum filter output impedance $\omega_m$ (trade-off between damping capability and volume of the damping element).
4. The maximum value of the filter output impedance $Z_m$ (trade-off between inductor and capacitor volume of the DM filter).

In addition, the following CM filter design parameters are optimized:

1. The CM filter resonance frequency $\omega_{cm}$ (trade-off between filter volume and attenuation).

(2) The maximum value of the CM filter output impedance $Z_{cm}$ (trade-off between inductor and capacitor volume of the CM filter).

Besides the EMI filter parameters, also the switching frequency $f_s$ is varied (trade-off between volume of the passive components, i.e. EMI filter and DC link capacitor, and heat sink volume).

4.2 Inverter Optimization Procedure The optimization for the inverter which is based on the procedure for the rectifier is shown in Fig. 12. In contrast to the rectifier optimization, no EMI filter has to be optimized. However, the harmonic motor losses are estimated as they are affected by the applied modulation scheme. They can be estimated via a power loss curve, defined by

$$P_{\text{motor, harmonic}} = \sum_n V_n^2 \left( \frac{A}{f_n} + \frac{B}{f_n^2} \right) \quad \cdots \quad (2)$$
where the high-frequency iron and copper losses are estimated via the experimentally derived parameters $A$, $B$, $\alpha$ and $\beta$(16).

**4.3 Volume Estimation** If a converter design complies with the EMI standards, the volumes of the various components are estimated (step 6 of Fig. 11). The capacitor volume is estimated with

$$V_C = k_1 \cdot C \hat{V}^2 + k_2 \hat{V},$$

(3)

The parameters $k_1$ and $k_2$ differ for the different capacitor types (DC link, DM filter, CM filter capacitor) and are shown in Appendix 1. The inductor volume is estimated with

$$V_L = k_1 \cdot (L I_i^2) + k_2 \cdot L I_i^2,$$

(4)

The parameters $k_1$ and $k_2$ are based on an inductor optimization(15) and are shown in Appendix 1 for the different inductor types (boost, DM filter and CM filter inductor).

The conduction and switching losses of the power semiconductors are calculated based on datasheet values. For the 3L-TT topology (cf. Fig. 3(b)) the switching losses have been scaled to the lower operating voltage. In addition, the switching losses differ from the data sheet as a diode with a lower voltage rating is used for the transition of the current. The datasheet curves have been adjusted linearly based on measured switching losses(17). The maximum allowed heat sink temperature is

$$T_{hs} = \min(T_{ac} - P_{chip,i} \cdot R_{th,i}, i = 1...N),$$

(5)

where $T_{ac}$ defines the maximal allowed junction temperature, $P_{chip,i}$ is the power loss of a single chip, $R_{th,i}$ its corresponding thermal resistance from junction to heat sink (including an insulation foil between semiconductor case and heat sink) and $N$ defines the number of semiconductors mounted on the heat sink. The heat sink is assumed to have a Cooling System Performance Index(18) $\text{CSPI} = 10 \text{W K}^{-1} \text{dm}^{-2}$ (forced air cooling) and therefore the volume can be calculated with

$$V_{hs} = \sum P_{chip} \cdot \text{CSPI} \cdot (T_{hs} - T_{amb}),$$

(6)

**5. Experimental Setup**

To verify the models used to calculate the currents and voltages of the rectifier system and the maximum estimation of an EMI test receiver, a 30kW prototype as shown in Fig. 13 has been built. Figure 14 shows the input voltages and currents as well as the output voltage and current with a 15kW load. Note that there is a 5th and 7th harmonic in the voltage input waveforms. This causes a 5th and 7th harmonic in the grid current of the converter but still meets the grid regulations. The critical frequency range is shown in Fig. 15, where the EMI measurements are compared to the model. The model predicts the maximum estimation of the test receiver with a good accuracy and the MF limits are met. In the MHz-range, the HF limits are violated, which could be corrected by a proper HF design of the converter components, which is not the scope of this work.

**6. Comparative Evaluation**

The optimization procedures described in Sect. 4 have been applied to a wide variation of topologies, modulation schemes, DM and CM topologies. The optimizations are performed for the rectifier stage (Sect. 6.1) as well as for the inverter stage (Sect. 6.2). Furthermore, a sensitivity analysis of the volume on the power semiconductor parameters is
performed in Sect. 6.3. Table 1 shows the assumptions and constraints of the optimization procedure. Note that changing these parameters would change the results. However, the optimization can be used for various parameters and the example provided in this paper gives a guideline which configurations of the converter are the most promising ones.

With this volume estimation equations the total volume of the converter can be optimized. The corresponding results are shown in Sect. 6.

6.1 Rectifier Optimization

The results for the rectifier stage are divided in different categories: In Sect. 6.1.1, the focus is put on the investigated modulation schemes. Section 6.1.2 analyses the impact of the chosen DM damping topology while Sect. 6.1.3 focuses on the CM topologies. Finally, in Sect. 6.1.4 the total rectifier volume for the different semiconductor technologies is analysed.

6.1.1 Modulation Scheme Comparison

Figure 16 shows the heat sink, DC link capacitor and EMI filter volume as a function of the switching frequency for the investigated modulation schemes. For this comparison, Si IGBTs are assumed and for 3L only the NPC topology is considered. The heat sink volume explains why with 2L topologies only a moderate switching frequency can be achieved. The DC link capacitor volume reveals the disadvantage of the 3L-OC modulation scheme: The volume is relatively big and does not decrease with a higher switching frequency, as the average neutral point current over a switching period is non-zero. The EMI filter volume shows that for the same switching frequency, the EMI filter volume of the 3L-NPB modulation scheme is lower than the one for other modulation schemes, as was predicted by the DM peak voltage (cf. Fig. 5).

To summarize, the 3L-NPB modulation scheme results in the smallest volume, due to the advantage of both a small DC link capacitor and a low EMI filter volume, which compensate for the higher switching losses compared to the clamping modulation schemes.

6.1.2 Damping Topology Comparison

Figure 17 shows the EMI filter volume for different damping topologies (cf. Sect. 3.2) and modulation schemes (cf. Sect. 2.2). For 3L the TT topology is considered and the CM filter is built with topology 1 and does not decrease with a higher switching frequency, as the average neutral point current over a switching period is non-zero. The EMI filter volume shows that for the same switching frequency, the EMI filter volume of the 3L-NPB modulation scheme is lower than the one for other modulation schemes, as was predicted by the DM peak voltage (cf. Fig. 5).

To summarize, the 3L-NPB modulation scheme results in the smallest volume, due to the advantage of both a small DC link capacitor and a low EMI filter volume, which compensate for the higher switching losses compared to the clamping modulation schemes.

6.1.3 DC Link Capacitor Comparison

Figure 18 shows the DC link capacitor volume as a function of the switching frequency for the investigated modulation schemes. For this comparison, Si IGBTs are assumed and for 3L only the NPC topology is considered. The DC link capacitor volume reveals the disadvantage of the 3L-OC modulation scheme: The volume is relatively big and does not decrease with a higher switching frequency, as the average neutral point current over a switching period is non-zero. The EMI filter volume shows that for the same switching frequency, the EMI filter volume of the 3L-NPB modulation scheme is lower than the one for other modulation schemes, as was predicted by the DM peak voltage (cf. Fig. 5).

To summarize, the 3L-NPB modulation scheme results in the smallest volume, due to the advantage of both a small DC link capacitor and a low EMI filter volume, which compensate for the higher switching losses compared to the clamping modulation schemes.
Fig. 18. EMI filter volume depending on the switching frequency for different CM topologies (cf. Sect. 3.3). The 3L-NPB modulation scheme is applied for a 3L TT topology using GaN transistors. For the DM filter a parallel-RL damping topology is used.

6.1.3 Common Mode Topology Comparison

Figure 18 shows the EMI filter volume depending on the switching frequency for different CM filter topologies (cf. Sect. 3.3). It can be seen that it is advantageous to place the CM inductor at the grid side (topology 1 and 3) as otherwise the HF harmonics of the DM current cause additional losses in the windings of the CM inductor and therefore would increase its volume. It is also advantageous to connect the CM capacitor to the DC link neutral point (topology 1 and 2), which has the additional benefit to reduce the currents to protective earth.

6.1.4 Semiconductor Technology Comparison

In Fig. 19, the total rectifier volume is shown for different semiconductor technologies and topologies. For the 2L topology, the 2L-OC modulation scheme is applied and for the 3L topology the 3L-NPB modulation scheme, according to the results in Sect. 6.1.1. For the damping topology, a parallel-RC topology is chosen (cf. Sect. 6.1.2) and the CM filter is built with CM topology 1 (cf. Sect. 6.1.3). The 2L topology with Si IGBTs could not be seen on the graph as the volume is very high - around 9 dm³. Either a change to new semiconductor technologies or a change to a 3L topology reduces the rectifier volume significantly. If both measures are combined, the rectifier volume is reduced further. The 3L NPC topology leads to the smallest volume. GaN semiconductor devices prove to be the best choice, as the switching frequency can be raised considerably, thereby reducing the volume of the EMI filter.

Keep in mind that the difference between the TT and NPC topology heavily depends on the used semiconductor devices (cf. Appendix 1).

6.1.5 Optimal Rectifier Design

Table 2 shows the components and their volume for the optimal rectifier design, which has a total volume of 2.8 dm³. Figure 20 shows the volume distribution of the converter. It can be seen that the heat sink and the boost inductors have the biggest share of the total rectifier volume. The EMI filter share (without the boost inductor) is approximately 20% of the total rectifier volume.

6.2 Inverter Optimization

The results for the

| Converter Topology | 3-Level NPC |
|--------------------|-------------|
| Modulation Scheme  | 3L-NPB      |
| Switching Frequency | 60.9 kHz    |
| Switches           | VisIC V22N65A |
| NPC Diodes         | Infineon IDW30G65CS |
| Heat Sink          | 1.1 dm³     |
| DC Link Capacitor C₆ | 2 x 14 µF    |
| Boost Inductor L₆  | 3 x 421.5 µH |
| Filter Inductor L₃ | 3 x 30.9 µH  |
| Filter Capacitor C₅ | 3 x 9.3 µF   |
| Damping Capacitor C₄ | 3 x 14.1 µF |
| Damping Resistor R₄ | 3 x 3.2 Ω   |
| CM Inductor L_CM   | 304.3 µH    |
| CM Capacitor C_CM  | 6.2 µF      |
| Total Volume       | 2.8 dm³     |

Keep in mind that the difference between the TT and NPC topology heavily depends on the used semiconductor devices (cf. Appendix 1).
inverter optimization are shown in Fig. 21 and 22. In contrast to the rectifier stage, there are less passive components which would benefit from a high switching frequency and a low DM voltage peak. This leads to three observations:

1. The 3L TT topology is preferred to the 3L NPC topology as the conduction losses are lower.

2. The 3L-C modulation scheme is preferred to the 3L-NPB modulation scheme as the lower switching losses outweigh the disadvantage of a higher DM peak voltage, as there is no EMI filter.

3. The considered SiC MOSFETs perform better than the GaN transistors as they result in lower conduction losses.

An additional benefit of the 3L topologies can be seen in Fig. 22: Due to the smoother output voltage, the harmonic losses of the motor can be considerably reduced. Furthermore, as the voltage steps of the winding voltages are reduced, the voltage stress on the insulation is reduced and the CM currents (which result in bearing currents) are reduced.

### 6.2.1 Optimal Inverter Design

Table 3 shows the components and their volume for the optimal inverter design, which has a total volume of 818 cm³. The ratio of heat sink to DC link capacitors is 83:17.

#### Table 3. Optimal inverter design with corresponding component volumes

| Converter Topology  | 3-Level TT |
|---------------------|------------|
| Modulation Scheme   | 3L-C       |
| Switching Frequency | 9 kHz      |
| Switches 1200 V     | Cree C2M0025120D |
| Switches 600 V      | Microsemi APT30SM70B |
| Heat Sink           | Si         |
| DC Link Capacitor C₀ | 2 x 74.9 µF |
| Heat Sink           | SiC        |
| DC Link Capacitor C₀| 2 x 70 cm³ |
| Heat Sink           | GaN        |
| DC Link Capacitor C₀| 2 x 74.9 µF |

Fig. 23. Volume reduction for different semiconductor improvements: reduced thermal impedance, reduced conduction losses or reduced switching losses.

### 6.3 Sensitivity Analysis

For all semiconductor technologies, different characteristics have been varied to analyze their impact on the total converter volume of the rectifier stage. A 3L NPC topology is considered and a 3L-NPB modulation scheme is applied. For the DM filter, a parallel-RC damping topology is considered and the CM filter is built with CM topology 1. Either the thermal impedance, the conduction losses or the switching losses have been reduced by 50%. The resulting volumes are shown in Fig. 23. As can be seen the biggest impact on the total converter volume is caused by reduced conduction losses, as these are the dominating semiconductor losses.

### 7. Conclusion

In this paper, various modulation schemes, topologies and EMI filter designs are analysed and compared against each other for bidirectional boost PFC rectifiers as well as inverters in terms of the volume. The 3L NPC topology has been shown to be the best topology for the rectifier stage, while for the inverter stage, the TT topology is to be the preferred one as the conduction losses are dominant there. For the same reason, GaN transistors are preferred for the rectifier stage, while SiC MOSFETs are advantageous for the inverter stage. In future research, the optimization of the rectifier and inverter stage could be combined to optimize the complete drive system.

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Appendix

1. Material Parameters

The used semiconductor devices are shown in Table 1. They have been chosen to have similar conduction losses to allow a fair comparison. Note that the current rating given by the manufacturers are considerably different despite similar conduction losses. The parameters for estimating the inductor and capacitor volumes are shown in Tables 2 and 3.

Jonas Wyss (Non-member) was born in Chur, Switzerland in 1987. He has studied Electrical Engineering at the Federal Institute of Technology in Zurich, Switzerland (ETH Zurich), focusing on drive systems and power electronics. In 2013, he received the master degree. His master thesis dealt with developing a multi-output rectifier. In April 2013 he joined the High Power Electronics Laboratory as a PhD student focusing on rectifier systems for drive systems.

Jürgen Biela (Non-member) received the Diploma (Hons.) degree from Friedrich-Alexander-Universität, Erlangen-Nuernberg, Nuremberg, Germany, and the Ph.D. degree from the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland, in 1999 and 2006, respectively. He dealt, in particular, with resonant dc-link inverters with the University of Strathclyde, Glasgow, U.K., and the active control of series-connected IGCTs with the Technical University of Munich, Munich, Germany, during his studies. In 2000, he joined the Research Department, Siemens Automation and Drives, Erlangen, Germany, where he was involved in inverters with very high switching frequencies, SiC components, and EMC. In 2002, he joined the Power Electronic Systems Laboratory (PES), ETH Zurich, for working to develop and optimize PFC, dcdc and multilevel converters with emphasis on passive components, and the design of pulsed-power systems and power electronic systems for future energy distribution.

app. Table 2. Parameters for estimating the volume of the inductors

| Component | Core Material | $k_1$ | $k_2$ |
|-----------|---------------|-------|-------|
| $L_s$     | METGLAS 2605SA1 | $266 \text{ cm}^3 \left( \text{H}^{-1} \text{A}^{-2} \right)^{-1}$ | 0 cm$^3$H$^{-1}$A$^{-2}$ |
| $L_{CM}$  | METGLAS 2605SA1 | $169 \text{ cm}^3 \left( \text{H}^{-1} \text{A}^{-2} \right)^{-1}$ | 64 cm$^3$H$^{-1}$A$^{-2}$ |
| $C_{f}$   | Vitroperm 500F | $39 \text{ cm}^3 \left( \text{H}^{-1} \text{A}^{-2} \right)^{-1}$ | 15 cm$^3$H$^{-1}$A$^{-2}$ |

app. Table 3. Parameters for estimating the volume of the capacitors

| Component | Series | $k_1$ | $k_2$ |
|-----------|-------|-------|-------|
| $C_{f}$   | EPCOS B3292x | 22.96 cm$^3$F$^{-1}$V$^{-2}$ | 2.24 cm$^3$ |
| $C_{f}$   | EPCOS B3265x | 55.54 cm$^3$F$^{-1}$V$^{-2}$ | 0.84 cm$^3$ |
| $C_{f}$   | EPCOS B3277x | 4.95 cm$^3$F$^{-1}$V$^{-2}$ | 4.24 cm$^3$ |

app. Table 1. Semiconductors considered in the optimization

| Type | Name |
|------|------|
| Si   | Infineon IW25N120T2 |
| Si   | Infineon IW30N65ES5 |
| SiC  | Infineon IDW30E65D1 |
| SiC  | Cree C2M0025120D |
| SiC  | Microsemi APT31350SM0B |
| SiC  | Infineon IDW30G65C5 |
| GaN  | VoIC VM40HB120D |
| GaN  | VoIC V22N65A |