Field effect devices with metal nanoparticles integrated by Langmuir-Blodgett technique for non-volatile memory applications

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Abstract. In this work, we demonstrate a hybrid silicon-organic nanocrystal floating gate memory device combining organic insulating materials, metal nanoparticles and Si MOSFET. The nanocrystals were organically passivated gold nanoparticles (Au-nps) forming a monolayer which was deposited by Langmuir-Blodgett (LB) technique. The FET device is fabricated on a Silicon-on-Insulator (SOI) substrate using conventional silicon processing. The nanoparticle layer is separated from the channel area of the FET with a 5 nm thermal SiO2 film and is isolated from the Al gate contact with a LB-deposited organic insulator layer. The memory effect is tested by means of threshold voltage shift measurements under different program/erase pulses. The nanocrystals can be charged either from the channel through the thermal oxide layer or from the gate through the organic insulator depending on the pulse applied pulse characteristics.

1. Introduction
Nanocrystal floating gate memory devices offer an alternative for nonvolatile floating-gate EEPROM devices with gate stack dielectrics. One challenging aspect remains the method of formation of the nanoparticles and its integration with silicon technology. Most of the research effort has focused on nanoparticle formation following high temperature CMOS compatible processes [1-3]. In this work we attempt to combine room temperature gold nanoparticle deposition and its use for a memory device demonstration. Along these lines a hybrid silicon-organic FET was used in a similar to EEPROM device architecture in order to probe the charge storage properties of the gold nanoparticles. Room temperature formation of nanoparticles might be considered as a critical step towards the fabrication of a low temperature processing memory device. The low temperature concept could find application in future 3-D memory architectures combined either with silicon or more probably with other low temperature processed materials like polymers. In addition, a hybrid silicon-organic approach, where organic materials are integrated with silicon devices, can provide a bridge between CMOS and organic technologies.

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2. Experimental procedure

The fabrication process began with a commercially available p-type SIMOX wafer with silicon over-layer thickness of 160 nm and a buried oxide thickness of 380 nm. After forming the Source and Drain (S/D) areas of the device a thermal oxide of 5 nm has been grown followed by the formation of Al contacts to S/D regions. Subsequently, the processed wafer was cut into small pieces each one of 2cm×2cm. Several samples are then fabricated: Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices with Al gate as reference sample (samples A), MISFET devices with the SiO₂ gate oxide coated with a 54 nm thick cadmium arachidate (Cd-AA) organic insulator by Langmuir-Blodgett (LB) technique and Al gate, as reference sample for the quality of the Cd-AA (samples B) and finally MISFET memory devices with the gold nanoparticle layer between the two insulating layers mentioned above (samples C). All these samples are described in figure 1a.

![Figure 1a](image1.png)

**Figure 1a.** The hybrid device structure. S, D and C are source, drain and the channel regions. The memory stack is made of a thermal SiO₂ layer (1), the gold nanoparticle layer (2) and the organic insulator on top (3). This sample is C as mentioned in the text. Referring again to the text, reference sample A includes only layer 1 and B includes layers 1 and 3.

The Au-nps were deposited on the SiO₂ substrates at room temperature by Langmuir-Blodgett technique using a Molecular Photonics LB700 trough. The subphase was purified water obtained from a reverse osmosis/deionisation/UV sterilization system; the film depositions were undertaken at a subphase pH of 5.8±0.2 and a temperature of 20±2 °C. These nanoparticles were of nominal diameter 10 nm passivated with tri-n-octylphosphine oxide/octadecylamine; a schematic diagram of their structure is shown in figure 1b. This capping makes the nanoparticles soluble in various organic liquids, but mainly insoluble in water; the Au-nps are thus suitable for LB deposition. More processing details can be found in [4] where a hysteresis in MIS capacitors has been also observed using the above film within the insulator stack.

Subsequently, Cd-AA films using the LB technique capped the gold nanoparticle layer. Cadmium arachidate films were obtained by spreading arachidic acid (Sigma, 99% purity) on a water subphase containing 2.5x10⁻⁴ M cadmium chloride (BDH, Analar Grade). The deposition pressure for these fatty acid salt films was 22 mN m⁻¹.

The fabrication of the device was completed with the Al gate electrode formation. Since the highest temperature for LB organic (CD-AA) films must not exceed 75°C, a new Al metallization process has been developed which has been described elsewhere [5].
3. Results and Discussion

A TEM micrograph is shown in figure 2. TEM image reveals that Au-nps possess a well-ordered, close-packed arrangement, and what appear to be twins can be seen in a number of the particles: Au is known to be very prone to twinning. The mean diameter of the particles is approximately 8 nm. Within the regions in which particles were present, the coverage was extremely dense. However, these regions only extended over distances of hundreds of nanometers, with the majority of the film being almost devoid of nanoparticles. This is most likely due to poor adhesion of the LB gold nanoparticle film on the TEM grid, which was coated by a carbon film.

The transfer characteristics (I_D-S−V_G-S) in the linear region (V_D-S=100 mV) have been compared for the three types of FET devices (A, B, C). A threshold voltage, V_th, variation is noted as the insulator stack configuration changes; this is mainly attributed to the presence of fixed charges in the organic insulator, already observed in other LB deposited insulators and explained as trapped charge at the interfaces between sequentially deposited layers [6]. Point defects observed by other researchers in LB deposited cadmium arachidate films could also result in fixed charges [7].

Au-nps devices exhibit good transistor (Fig. 3) and memory operation under different programming voltage pulse conditions. The final device exhibits clear memory window under different gate bias pulses of 1s duration. During this long pulse duration the charge exchange takes place between the nanocrystals and the metal gate electrode leading to counterclockwise hysteresis. Since no hysteresis is observed for a gate-voltage cycle for reference samples without Au nanocrystals (samples A and B) then we conclude that the charge storage is due to them. The application of pulses with shorter time duration, 300 ms, revealed the effect of nps charge exchange with the channel (Fig. 4). This takes place when the gate voltage does not exceed a value of 5 V. For higher pulse voltages the nanoparticles start to interact with the gate. It seems that two competitive conduction mechanisms exist, nc charging and
organic insulator leakage. A likely explanation might be the following: for low gate voltages \(V_{GS} \leq 5\) V during short pulses the electric field causes the fast interaction of the channel electrons with the nps and simultaneously the current leakage through control insulator is kept low. When the gate voltage increases the electric field increases also, resulting to the increment of the leakage current flowing from the ncs towards the gate through the organic insulator. This enhanced conduction masks the effect of channel charge exchange. According to Nabok and his co-workers [8] the conduction mechanism of LB insulating films is due (i) to direct tunneling through each LB bi-layer and (ii) thermally activated hopping within the plane of carboxylic head groups. In addition, it has been shown elsewhere that the 54nm LB Cd-AA film is more conductive than the SiO\(_2\) insulator [5]. So, the increase of electric field across the gate insulator stack with the applied gate voltages in order to inject charges into the nanoparticles enhances the conduction through the organic insulator.

4. Conclusions
We have demonstrated a hybrid silicon-organic EEPROM memory device fabricated on a SOI substrate using gold nanoparticles as charge storage elements deposited at room temperature by the Langmuir-Blodget technique [4]. Poor insulating properties of the Cadmium Arachidate organic insulator that separates the nanoparticle layer from the metal gate electrode results in fast degradation of this insulating film after about 70 cycles of write/erase operation. Replacement of the organic insulator used here with a less conductive material is underway in order to increase the endurance of the device.

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