A single-phase simplified DC-AC converter using DC-link capacitors and an H-bridge

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ABSTRACT

This paper introduces a simplified inverter circuit using a single dc source and an H-bridge with a least possible number of “switching devices”. This topology does not employ multiple “dc sources”, which enhances the reliability of the configuration. The topology consists of two parts, namely: “Level generation parts” as well as “Polarity generation parts”, it is the mixture of some of the switching devices, DC-link capacitor and a single DC source completes the part of level generation. The H-bridge in the proposed structure produces the polarity generation part. A detailed explanation of the modulation system and operating modes of the proposed framework are discussed. Finally, in the MATLAB/SIMULINK platform, the projected network topology is simulated and the outcomes are presented.

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1. INTRODUCTION

Single-phase DC-AC converters are predominant in several industrial and household applications like lathe machines, centrifugal pumps, uninterrupted power supplies, etc. Multilevel single-phase DC-AC converters are highly attractive than two-level inverters due to the advantages of higher power rating, improved power quality and higher reliability. In this context, cascaded converters are highly flexible and modular in the family of multilevel inverters. In this group, “cascaded H-bridge (CHB)” converters [1]-[4] are the classical and traditional types. CHB converters have the advantages of equal voltage stress in symmetrical configurations, easy to add/remove the H-bridges to increase/decrease the voltage levels in the output. MLI technology is spreading to several areas such as AC drives, static reactive compensators, micro-grid systems and renewable energy sources [5]-[8]. The “Flying capacitors clamped (FCC)”, “neutral point clamped (NPC)” and “CHB converters” [9]-[11] are established as normal topologies in the MLI family. In this configurations, the device count increases exponentially in reference to the increased in the voltage levels of output. The requirement of unequal voltage ratings of the clamping diodes, unequal capacitor size and a greater number of dc sources puts limitations on these topologies. Several new MLI configurations with the intention of avoiding the drawbacks in the standard topologies were proposed in the literature for several applications [12]-[16]. In recent times, cascaded converters are attracting attention from industries as well as
academia. Several such voltage source inverters (VSIs) were proposed in the literature by employing several combinations of switches, dc power supplies [17]-[20].

In this configuration, the converter has fewer components and lower blocking voltage across the switching devices, resulting in lower costs. The remain papers are organised as; section 2 describes the operating models, section 3 describes the modulation principles that is used to produced the essential "output voltage waveforms", section 4 describes the simulation results that were obtained for different kinds of modulation indices that were used to validate the proposed converter, and section 5 concludes the paper.

2. PROPOSED INVERTER

The recommended converter is depicted in Figure 1. It is used in single-phase alternating current output voltage. It is referred to as an inverter. The converter makes use of eight bidirectional switching devices, one direct current source, and three direct current link condensers. Despite the fact that the switching devices are bidirectional, they only block voltage in single route due to the existence of anti-parallel diode in the circuit. The proposed architecture can make use of three different dc sources, which can be attained from battery banks, photovoltaic systems, or rectifier circuit, respectively. Figures 2 (a) and 2 (b) depict the switchings state at negative and positive zero's output voltage crossing, correspondingly. \(V_{0}=0^+\) known as positive zero-crossing output voltage. \(V_{0}=0^-\) represents an output voltage with a negative zero-crossing voltage. All switches are subjected to the same amount of switching states in order to maintain a increased temperature.

![Figure 1. Schematic diagram of the proposed module](image)

![Figure 2. Operating methods through zero crossing: (a) \(V_{0}=0^+\), (b) \(V_{0}=0^-\)](image)

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Figure 3 represents the process of the projected converters to produce a positive levels voltage transversely to the output’s terminal. Figure 3 (a) generated $V_0=V_{dc}/3$, in this working modal, the control semiconducting material used in devices for IGBTs $S_2$, $S_4$, $S_5$ and $S_8$ conduct. Figure 3 (b) produces $V_0=2V_{dc}/3$, in these operating modes, the IGBTs $S_2$, $S_3$, $S_5$ and $S_8$ conduct. Figure 3 (c) shown the peak’s voltage of $V_0=V_{dc}$, in these operating modes, the IGBTs $S_1$, $S_3$ and $S_8$ manner. The working methods of the converters used to croped the adverse output voltages levels are shown in Figure 4. Figure 4 (a) generated $V_0=-V_{dc}/3$, in these operating models, the IGBTs $S_2$, $S_4$, $S_6$ and $S_7$ turn on. Figure 4 (b) provides the output voltage $V_0=-2V_{dc}/3$, during this period the IGBTs $S_2$, $S_3$, $S_6$ and $S_7$ turn on. Figure 4 (c) stretches the output voltages $V_0=-3V_{dc}$, throughout these periods the IGBTs $S_1$, $S_6$ and $S_7$ turn on.

![Diagram](image1)

Figure 3. Positive-level working methods, (a) $V_0=V_{dc}/3$, (b) $V_0=2V_{dc}/3$, (c) $V_0=V_{dc}$

![Diagram](image2)

Figure 4. Operating methods through negative voltage level, (a) $V_0=-V_{dc}/3$, (b) $V_0=-2V_{dc}/3$
3. MODULATION TECHNIQUE

In order to make it easier to describe Table 1 shows the switch states at numerous output voltage in the proposed converter, while showing the switch states at several output voltage in the proposed converter. The digits 1 and 0 are used to signify the on and off states of the IGBTs in Figure 1, as shown in the accompanying table: Table 1 the switches are all correctly positioned. $S_5, S_6, S_7$ and $S_8$ are better due to their lower switching frequencies. Figure 5 shows the modulation technique [21]-[23]. The concept will use it to create a gate pulse for IGBTs in the suggested system. Six triangular waveforms are used to produce a pure sinusoidal waveform. Both the sinusoidal wave and the triangular wave are known as reference and carrier waves, respectively. The reference waves interact with each carrier wave at specific time intervals, 1, 2, 3, 1', 2', and 3'. This explains why the subsequent pulses are $P_1-P_3$ and $N_1-N_3$. The output voltage is generated by logical gate circuits that efficiently use these pulses. The total number of output levels is based on the modulation index (M.I.), that is described as:

$$M.I. = \frac{V_{\text{peak}}}{3 \times V_{dc}}$$

(1)

![Figure 5. Sine-triangle comparison method](image)
Table 1. Inverter switching sequence

| Output voltage level ($V_0$) | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 |
|-------------------------------|----|----|----|----|----|----|----|----|
| $V_{dc}$                       | 1  | 1  | 0  | 1  | 0  | 0  | 0  | 1  |
| $2V_{dc}/3$                    | 0  | 1  | 1  | 0  | 0  | 0  | 0  | 1  |
| $V_{dc}/3$                     | 0  | 1  | 0  | 1  | 1  | 0  | 0  | 1  |
| $0^-$                          | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 1  |
| $0^+$                          | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  |
| $-V_{dc}/3$                    | 0  | 1  | 0  | 1  | 0  | 1  | 1  | 0  |
| $-2V_{dc}/3$                   | 0  | 1  | 1  | 0  | 0  | 1  | 1  | 0  |
| $-V_{dc}$                      | 1  | 0  | 0  | 0  | 0  | 1  | 1  | 0  |

4. SIMULATION RESULTS

The reproduction parameters [24], [25] are meant to result in an output voltage of 230 V and a frequency of 50 Hz, respectively. Table 2 contains a list of the extra parameters that will be considered in the simulation. The waveforms of the inverter current and output voltage for an M.I. of 0.9 and 0.6 are shown in Figures 6 (a) and 7 (a), respectively, for the inverter current and output voltage. For example, Figures 6 (a) and 7 (a) show the respective outputs voltage waveforms with currents, with the former representing seven levels and the latter representing five levels, respectively. As a result, when the M.I. is reduced, the peak voltage of the output will decrease as well ($V_{peak}$). Figures 6 (b) and 7 (b) show the FFT spectrums of the inverter output voltage at various levels of M.I., respectively. $V_{peak}$ can be seen that 323 V is modulated at the inverter at a rate of 0.9, with a entire harmonic distortion of 22.4%. This is illustrated in Figures 6 (b) and 7. The decreased in M.I. leads to an increased in THD by reducing the numbers of “output voltage level,” which is understandable in Figures 6 (b) and 7 (b).

Table 2. Configuration parameters

| Parameters                  | Values |
|-----------------------------|--------|
| $V_{dc}$                    | 240 V  |
| $P_{output}$                | 732 W  |
| $V_0$                       | 236 V  |
| $I_0$                       | 4.9 A  |
| Switching frequency ($f_{sw}$) | 4 kHz  |
| Fundamental frequency ($f_m$) | 50 Hz  |

Figure 6. Simulink result of the converters at $M.I.$=0.9; (a) converters voltage and current waveforms at the output, (b) FFT spectrum of $V_0$, (c) FFT analysis of $I_0$
Figures 6 (c) and 7 (c) represents each harmonics spectrum of the present output waveforms. At 0.9, the values of \(I_0\) peak is 4.9 A, whereas the total harmonic distortion (THD) is roughly 0.4%. The value of \(I_0\) peak decreases in response to the voltage reductions in M.I. The amount of \(I_0\) peak is diminished as 3.2 A and the THD is around 0.6%. Figure 8 depicts the performance of the shown in configuration to withstand the sudden changes in load. It can be observed in Figure 8 that the projected techniques is effective. The circuit can be produced the undistorted output w.r.t changes in the load.

**Figure 7.** Simulink result of the converters at M.I.=0.62; (a) converters voltage and current waveforms at the output, (b) FFT spectrum of V0, (c) FFT analysis of I0

**Figure 8.** Dynamic responded of the proposed formation for a step-change in load at \(m_a=0.9\)
5. CONCLUSION

This article features the simplified DC-AC MLI configuration. When it comes to creating the requisite number of output voltage levels for the inverter while employing the fewest number of components possible, a tri-tier circuit and an H-bridge are the most efficient methods available. The analyses and operating modes that were used to achieve zero, positive, and negative levels were discussed in depth in order to achieve these results. Without regard to the fundamental frequency, H-bridge switches in the projected network topology have a “lower switching frequency” when compared to other switches. With the suggested architecture, switching losses are more controlled, and as a result, total efficiency is increased. A sinusoidal PWM approach generates the firing pulses required by employing the most efficient technique available at the time. The findings of the MATLAB/SIMULINK system have been confirmed for MI of 0.9 and 0.6, correspondingly. As can be observed from the FFT output spectrum, the THD in the waveforms of the system meet with the IEEE 1547 standard.

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