Scaling Back-propagation by Parallel Scan Algorithm

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Abstract

In an era when the performance of a single compute device plateaus, software must be designed to scale on a massively parallel system for better runtime performance [9]. However, the commonly used back-propagation (BP) algorithm [27] imposes a strong sequential dependency in the process of gradient computation. Under model parallelism [19, 11, 16], BP has a theoretical step complexity of $\Theta(n)$ which hinders its scalability in a parallel computing environment, where $n$ represents the number of compute devices into which a model is partitioned. In this work, we restructure such dependency and reformulate BP into a scan operation which is scaled by our modified version of the Blelloch scan algorithm [3]. Our algorithm is able to achieve a theoretical step complexity of $\Theta(\log n)$. We perform an in-depth performance analysis and identify the challenges of deploying our algorithm in a practical setting, along with a variety of approaches to tackle such challenges. We demonstrate the scalability benefits of our algorithm in the use case of retraining pruned networks [10, 29, 14].

1 Introduction

The training of deep learning models demands more and more compute resources as the models become more powerful and complex with an increasing number of layers in recent years [20, 31, 30, 12, 15]. For example, ResNet can have more than a thousand layers [13] and take days to train on the state-of-the-art GPUs [4]. When the performance of a single compute device plateaus [9], training has to be designed to scale on a massively parallel system. Model parallelism [19, 11, 16] is one approach to scale training by partitioning a model and distributing its parts among multiple devices. This is the common approach when a model cannot fit into one device due to memory constraints (caused by, for example, deep network architecture, large batch size, or high input resolution [26, 33]). However, training under model parallelism does not scale well with the number of devices. The fundamental reason for such an scalability issue is that the back-propagation algorithm (BP) [27] imposes a strong sequential dependency between layers during the gradient computation, which effectively allows at most one device to be utilized at any given point in time. This dependency prevents BP from being efficiently deployed into a distributed computing environment. Therefore, we seek to address this fundamental limitation by restructuring the dependency so that BP can be scaled by parallel algorithms. In summary, we make several major contributions:

- We reformulate BP as a scan [3] operation, and modify the Blelloch scan algorithm [3] to efficiently scale BP in a distributed computing environment. Our method has a theoretical...
step complexity of $\Theta(\log n)$, where $n$ represents the number of devices into which a model is partitioned, compared to $\Theta(n)$ of the naïve implementation of model parallelism.

- We perform an in-depth runtime analysis of our algorithm, identify the challenges in applying it in a practical setting, and propose a new and efficient approach to tackle these challenges using sparse Jacobian matrices. We then develop routines to efficiently generate transposed Jacobian in sparse format for various operators.

- By projecting the performance of our method, we demonstrate that the retraining of pruned networks [10, 29, 14] is a practical use case where our method can achieve better scaling compared to the original BP.

2 Background and Prior Work

To increase the utilization of hardware resources with model parallelism, prior works (e.g., PipeDream [11] and GPipe [16]) propose to pipeline the computation in the forward and backward passes across devices. However, these solutions are not “silver bullets” to scalability for the following reasons. First, both PipeDream [11] and GPipe [16] require storing multiple versions of weights and activations for all mini-batches that enter the pipeline. Thus, the memory consumption grows linearly with the length of the pipeline. As a result, the maximum number of devices that can be supported is limited by the memory capacity of a single device (such as the GPU global memory). Second, if the parameter updates are not fully synchronized as proposed in PipeDream [11], staleness can be introduced. Although Harlap et al. argue that the staleness produced by their method does not affect the update step for a vanilla SGD optimizer [11], such argument would be invalid when combined with other techniques commonly used in first-order optimizers (such as momentum in Adam [17]). Otherwise, if the gradient updates are fully synchronized as proposed in GPipe [16], the “bubble of idleness” between the forward and backward passes increases linearly with the length of the pipeline, thus linearly reducing the hardware utilization and decimating the original purpose of pipelining.

Our approach fundamentally differs from these key prior works [11, 16] in the following ways. First, instead of following the dependency of BP, we reformulate BP so that scaling is achieved via the Blelloch scan algorithm [3] which is designed for parallelism. Second, the original BP is reconstructed exactly, so that estimation errors such as staleness do not exist; therefore, our method is agnostic to the exact first-order optimizer being used. Third, our approach becomes more advantageous as the number of devices increases, instead of diminishing returns or hitting scalability limits.

3 Problem Formulation and Proposed Method

We conceptualize a model as a vector function $f$ composed of sub-functions $\vec{x}_i = f_i(\vec{x}_{i-1}; \vec{\theta}_i)$:

$$f(\cdot; \vec{\theta}_1, \vec{\theta}_2, ..., \vec{\theta}_n) = f_1(\cdot; \vec{\theta}_1) \circ f_2(\cdot; \vec{\theta}_2) \circ ... \circ f_n(\cdot; \vec{\theta}_n)$$

where $\vec{\theta}_i, i \in \{1, ..., n\}$ are the parameters of the model. The model is evaluated by an objective function $l[f(\vec{x}_0; \vec{\theta}_i, i \in \{1, ..., n\})]$, where $\vec{x}_0$ is the initial input to the model. This formulation on convolutional neural networks can be visualized in Figure 1.

To train the model $f$, a first-order optimizer requires the gradients $\nabla_{\vec{\theta}_i} l$ which are derived from the gradients $\nabla_{\vec{\theta}_i} l$:

$$[\nabla_{\vec{\theta}_1} l, \nabla_{\vec{\theta}_2} l, ..., \nabla_{\vec{\theta}_n} l] \leftarrow [(\partial \vec{x}_1 / \partial \vec{\theta}_1)^T \nabla_{\vec{\theta}_1} l, (\partial \vec{x}_2 / \partial \vec{\theta}_2)^T \nabla_{\vec{\theta}_2} l, ..., (\partial \vec{x}_n / \partial \vec{\theta}_n)^T \nabla_{\vec{\theta}_n} l]$$

Figure 1: A visualization of the formulation in Section 3 on convolutional neural networks. Different parts of the model can be distributed to different devices (workers).
where \( \frac{\partial \vec{x}}{\partial i} \) is the Jacobian matrix of the output \( \vec{x}_i \) of \( f_i \) to its parameters \( \vec{i} \). To derive \( \nabla_{\vec{x}} l \) given \( \nabla_{\vec{x}} l \), BP solves the following recursive equation, from \( i = n - 1 \) to \( i = 1 \):

\[
\nabla_{\vec{x}} l \leftarrow (\frac{\partial f_{i+1}}{\partial \vec{x}_i})^T \nabla_{\vec{x}_{i+1}} l, \forall i \in \{n - 1, \ldots, 1\} \\
\]

(2)

where \( \frac{\partial f_{i+1}}{\partial \vec{x}_i} \) is the Jacobian matrix of the output \( \vec{x}_{i+1} \) of \( f_{i+1} \) to its input \( \vec{x}_i \). Equation 1 itself does not have dependency along \( i \); therefore, the computation of \( \nabla_{\vec{x}} l \) can be parallelized if \( \nabla_{\vec{x}} l \) are available. However, Equation 2 imposes a \text{strong sequential dependency} along \( i \) where the computation of \( \nabla_{\vec{x}} l \) can not begin until the computation of \( \nabla_{\vec{x}_{i+1}} l \) finishes, and therefore, hinders the scalability when multiple workers (as an abstraction of devices) are available.

### 3.1 Back-propagation as a Scan Operation

We define a \textit{binary}, \textit{associative} and \textit{non-commutative} operator \( A \odot B = BA \) whose identity value is the identity matrix \( I \), where \( A \) can be either a matrix or a vector and \( B \) is a matrix. Using operator \( \odot \), we can reformulate Equation 2 as calculating the following array:

\[
[\nabla_{\vec{x}} l, \nabla_{\vec{x}} l \odot (\frac{\partial \vec{x}_n}{\partial \vec{x}_{n-1}})^T, \nabla_{\vec{x}} l \odot (\frac{\partial \vec{x}_n}{\partial \vec{x}_{n-1}})^T \odot (\frac{\partial \vec{x}_{n-1}}{\partial \vec{x}_{n-2}})^T, \ldots, \nabla_{\vec{x}} l \odot (\frac{\partial \vec{x}_n}{\partial \vec{x}_{n-1}})^T \odot \ldots \odot (\frac{\partial \vec{x}_1}{\partial \vec{x}_0})^T ]
\]

(3)

Based on the definition proposed by Blelloch \cite{3}, Equation 3 can be interpreted as a \textit{scan (all-prefix-sums)} operation of \( \odot \) on the input array:

\[
[\nabla_{\vec{x}} l, (\frac{\partial \vec{x}_n}{\partial \vec{x}_{n-1}})^T, (\frac{\partial \vec{x}_{n-1}}{\partial \vec{x}_{n-2}})^T, \ldots, (\frac{\partial \vec{x}_1}{\partial \vec{x}_0})^T]
\]

(4)

### 3.2 Scaling Back-propagation with the Blelloch Scan Algorithm

#### Algorithm 1 Modified Blelloch Scan Algorithm

| Input: | \( a = [\nabla_{\vec{x}} l, (\frac{\partial \vec{x}_n}{\partial \vec{x}_{n-1}})^T, (\frac{\partial \vec{x}_{n-1}}{\partial \vec{x}_{n-2}})^T, \ldots, (\frac{\partial \vec{x}_1}{\partial \vec{x}_0})^T] \) | \( \nabla_{\vec{x}} l \) needed for Equation 1 computed \textit{in-place} |
| Output: | \( a = [I, \nabla_{\vec{x}} l, \nabla_{\vec{x}_{n-1}} l, \ldots, \nabla_{\vec{x}_1} l] \) | \( \nabla_{\vec{x}} l \) | |

1: for \( d \leftarrow 0 \) to \( \lceil \log(n + 1) \rceil - 2 \) do
2: for all \( i \leftarrow 0 \) to \( n - 2^{d+1} \) by \( 2^{d+1} \) do in parallel
3: \( (l, r) \leftarrow (i + 2^{d+1} - 1, \min(i + 2^{d+1} - 1, n)) \)
4: \( a[l] \leftarrow a[l] \odot a[r] \)
5: end for
6: end for
7: \( a[0] \leftarrow I \)
8: for \( d \leftarrow \lceil \log(n + 1) \rceil - 1 \) to 0 do
9: for all \( i \leftarrow 0 \) to \( n - 2^d \) by \( 2^d+1 \) do in parallel
10: \( (l, r) \leftarrow (i + 2^d - 1, \min(i + 2^d - 1, n)) \)
11: \( T \leftarrow a[l] \)
12: \( a[r] \leftarrow a[r] \odot T \)
13: end for
14: end for
15: end for

We can parallelize the computation of Equation 3 on multiple workers with the Blelloch scan algorithm \cite{3}, formally described in Algorithm 1 \cite{1}. The algorithm contains two phases: \textit{up-sweep} and \textit{down-sweep}. Figure 2 visualizes this algorithm applied on the convolution layers of VGG-11 \cite{30} with levels L0-L4 as the up-sweep and levels L5-L10 as the down-sweep. Only the up-sweep phase contains matrix-matrix multiplications. Due to the \textit{non-commutative} property of the operator \( \odot \), we have to reverse the operands of \( \odot \) during the down-sweep phase. This modification is reflected on line 13 of Algorithm 1 \cite{1} and visualized in Figure 4 \cite{4}.

### 3.3 Jacobian Matrices in Sparse Format

A full Jacobian matrix \( \frac{\partial \vec{x}_{i+1}}{\partial \vec{x}_i} \) of \( f_{i+1} \) can be too expensive to generate, store, and process. In fact, the Jacobian matrix of the first convolution operator in VGG-11 \cite{30} processing a \( 32 \times 32 \) image can occupy 768 MB of memory if it is stored as a full matrix, which is prohibitively large. Fortunately, Jacobian matrices of certain operators (such as convolution, ReLU, and max-pooling)
can be very sparse as shown in Figure 5. In our implementation, the transposed Jacobian matrices are represented in the Compressed Sparse Row (CSR) format due to existing support of CSR matrix multiplication routines in sparse matrix libraries such as cuSPARSE. Representing the data contained in the same Jacobian of the aforementioned convolution operator in CSR shrinks the memory consumption down to only 6.5 MB. Two types of zeros appear in an operator’s Jacobian: guaranteed zeros that are input invariant (e.g., zeros outside of the diagonal of the ReLU’s Jacobian); and possible zeros that are input dependent (e.g., zeros on the diagonal of the ReLU’s Jacobian). For any operator, the pattern of the distribution for guaranteed zeros (named as the sparsity pattern for brevity) in the Jacobian is deterministic with the model architecture and known ahead of time. Thus, this information can be used to build more efficient sparse matrix multiplication routines than the generic ones in conventional sparse matrix libraries (e.g., cuSPARSE). The sparsity of guaranteed zeros (defined as the fraction over all elements in a matrix) for various operators is listed in Table 1.

3.4 Generating Jacobian Matrix in CSR Analytically

To avoid impractically inefficient methods of generating the Jacobian of an operator one column at a time (either numerically or via automatic differentiation), we develop analytical routines to generate the transposed Jacobian directly into the CSR format.
Table 1: The sparsity of guaranteed zeros for various operators.

| Operator         | Filter/Kernel Size | Input Size | Output Size | Sparsity     | Examples† |
|------------------|--------------------|------------|-------------|--------------|-----------|
| Convolution      | $c_o \times c_i \times h_f \times w_f$ | $c_i \times h_i \times w_i$ | $c_o \times h_o \times w_o$ | $1 - \frac{h_f \times w_f}{h_i \times w_i}$ | 0.99157   |
| ReLU             | N/A                | $c \times h \times w$ | $c \times h \times w$ | $1 - \frac{c \times h \times w}{c \times h \times w}$ | 0.99998   |
| Max-pooling      | $h_f \times w_f$   | $c_i \times h_i \times w_i$ | $c_o \times h_o \times w_o$ | $1 - \frac{h_f \times w_f}{c_i \times h_i \times w_i}$ | 0.99994   |

† The examples of sparsity for the first convolution, ReLU and max-pooling operators of VGG-11 operating on $32 \times 32$ images are shown in the last column of the table. ‡ Approximation when $h_i$ and $w_i$ are much greater than the padding size.

Convolution For the transposed Jacobian of a convolution operator with a $3 \times 3$ filter and a padding size of 1 on all sides of the height and width, our methods of generating the CSR `indptr`, `indices` and `data` arrays [32] are formally described in Algorithm 2, Algorithm 3 and Algorithm 4 respectively.

Algorithm 2: Compute the CSR `indptr` array for the transposed Jacobian of a $3 \times 3$ convolution.

**Input:** input channels $c_i$, output channels $c_o$, input height $h_i$, input width $w_i$  
**Output:** `indptr ← malloc($c_i \times h_i \times w_i + 1$)`

```plaintext
1: for all $i ← 0$ to ($c_i \times h_i \times w_i$) do in parallel
2: \quad $a ← [i/h_i]$
3: \quad $b ← i \mod (h_i, w_i)$
4: \quad if $b < w_i$ then
5: \quad \quad `indptr[i] ← ac_o,(3w_i)(3h_i - 2)) + 6c_o b$
6: \quad else if $b < w_i(h_i - 1)$ then
7: \quad \quad `indptr[i] ← ac_o,(3w_i(3h_i - 2)) + 6c_o w_i + 9c_o (b - w_i)$
8: \quad else
9: \quad \quad `indptr[i] ← ac_o,(3w_i(3h_i - 2)) + 6c_o w_i + 9c_o (w_i(h_i - 2)) + 6c_o (b - w_i (h_i - 1))`
10: \quad end if
11: end for
```

Algorithm 3: Compute the CSR `indices` array for the transposed Jacobian of a $3 \times 3$ convolution.

**Input:** input channels $c_i$, output channels $c_o$, input height $h_i$, input width $w_i$, `indptr` computed from Algorithm 2

**Output:** `indices ← malloc((3w_i(3h_i - 2)c_i \times c_o)`)  

```plaintext
1: for all $i ← 0$ to ($c_i \times h_i \times w_i - 1$) do in parallel
2: \quad $r ← i \mod (h_i, w_i)$
3: \quad `base ← malloc(9c_o)`
4: \quad for all $k ← 0$ to ($c_o - 1$) do in parallel
5: \quad \quad `for all $k ← 0$ to 2 do in parallel`
6: \quad \quad \quad `base[9j + 3k : 9j + 3(k + 1)] ← ([-1,0,1] + (j h_i + k - 1) w_i + r) \mod (c_o \times h_i \times w_i)`
7: \quad \quad end for
8: \quad \quad end for
9: \quad \quad \quad `if r < w_i or r ≥ w_i(h_i - 1) then`
10: \quad \quad \quad \quad `row ← malloc(6c_o)`
11: \quad \quad \quad \quad `left, right) ← (3,9) if r < w_i; (0, 6) otherwise`
12: \quad \quad \quad \quad `for all $j ← 0$ to ($c_o - 1$) do in parallel`
13: \quad \quad \quad \quad \quad `row[6j : 6j + 6] ← base[9j + left : 9j + right]`
14: \quad \quad \quad \quad end for
15: \quad \quad end if
16: \quad \quad `row ← base`
17: \quad \quad end if
18: \quad \quad `indices[indptr[i] : indptr[i + 1]] ← sorted(row)`
19: \quad end for
```

ReLU Our methods of generating the CSR `indptr`, `indices` and `data` arrays [32] for the transposed Jacobian of a ReLU operator are formally described in Algorithm 5, Algorithm 6 and Algorithm 7 respectively.

Max-pooling Assuming the stride size and the window size are the same, and we can access a tensor (named as pool `indices` for brevity) which specifies the indices of the elements in the input tensor that are “pooled” for the output tensor (documented in [11]), our methods of generating the CSR `indptr`, `indices` and `data` arrays [32] are formally described in Algorithm 8, Algorithm 9 and Algorithm 10 respectively.
Algorithm 4 Compute the CSR data array for the transposed Jacobian of a $3 \times 3$ convolution.

Input: input channels $c_i$, output channels $c_o$, input height $h_i$, input width $w_i$, filter weights, indptr computed from Algorithm 2
Output: data ← malloc(3$w_i$(3$h_i$ - 2)$c_i$$c_o$)
1: for all $i ← 0$ to ($c_i$h_i$w_i$ - 1) do in parallel
2: $r ← i \mod (h_i, w_i)$
3: $m ← [i/(h_iw_i)]$
4: range ← (1::1) if ($r < w_i$); (2:0:-1) if ($r \geq w_i(h_i - 1)$); (2::1) otherwise
5: data[indptr[i]] = indptr[i + 1] ← flatten(weights[i, m, range, ::1])
6: Fix corner cases when ($i \mod w_i$) = 0 or ($i \mod w_i$) = ($w_i$ - 1).
7: end for

Algorithm 5 Compute the CSR indptr array for the transposed Jacobian of ReLU.

Input: size $d$ of the (flattened) input tensor $x$
Output: indptr ← malloc($d + 1$)
1: for all $i ← 0$ to $d$ do in parallel
2: indptr[i] ← i
3: end for

Algorithm 6 Compute the CSR indices array for the transposed Jacobian of ReLU.

Input: size $d$ of the (flattened) input tensor $x$
Output: indices ← malloc($d$)
1: for all $i ← 0$ to ($d - 1$) do in parallel
2: indices[i] ← i
3: end for

Algorithm 7 Compute the CSR data array for the transposed Jacobian of max-pooling.

Input: pool_indices, input height $h_i$, input width $w_i$, output height $h_o$, output width $w_o$, output channels $c_o$
Output: indptr ← malloc($c_i$h_i$w_i$ + 1), mapping ← malloc($c_i$h_i$w_i$)
1: for all $i ← 0$ to $c_i$h_i$w_i$ - 1 do in parallel
2: mapping[i] ← -1
3: end for
4: for all $c ← 0$ to $c_o - 1$ do in parallel
5: for all $h ← 0$ to $h_o - 1$ do in parallel
6: for all $w ← 0$ to $w_o - 1$ do in parallel
7: $i ← c_h w_i + pool_indices[c, h, w]$
8: $j ← (c_h h + h) w_o + w$
9: mapping[i] ← j
10: end for
11: end for
12: end for
13: ptr ← 0
14: for $i ← 0$ to ($c_i$h_i$w_i$ - 1) do
15: indptr[i] ← ptr
16: if mapping[i] ≠ -1 then
17: ptr ← ptr + 1
18: end if
19: end for
20: indptr[1] ← ptr

Algorithm 8 Compute the CSR indices array for the transposed Jacobian of max-pooling.

Input: mapping computed from Algorithm 5, input height $h_i$, input width $w_i$, output height $h_o$, output width $w_o$, output channels $c_o$
Output: indices ← malloc($c_i$h_i$w_i$)
1: indices_ptr ← 0
2: for $i ← 0$ to ($c_i$h_i$w_i$ - 1) do
3: if mapping[i] ≠ -1 then
4: continue
5: end if
6: indices[indices_ptr] ← mapping[i]
7: indices_ptr ← indices_ptr + 1
8: end for
Algorithm 10 Compute the CSR data array for the transposed Jacobian of max-pooling.

Input: output channels $c_o$, output height $h_o$, output width $w_o$
Output: data ← malloc($c_o h_o w_o$)

1: for all $i ← 0$ to $(c_o h_o w_o - 1)$ do in parallel
2: data ← 1
3: end for

4 Evaluation

We evaluate our method against two baselines: (1) the stronger baseline of PyTorch Autograd [24] which is a widely adopted implementation of BP; and (2) the weaker baseline of linear scan which is emulating BP by using the transposed Jacobian in CSR and multiplying with the gradient (as shown in Equation 2) explicitly via sparse matrix multiplication routines.

4.1 Convergence

Theoretically, our algorithm is a reconstruction of BP instead of an estimation, and hence, expected to reproduce the exact same outputs. However, in practice, numerical differences could be introduced due to the change in the order of matrix multiplications. We apply our algorithm to train LeNet-5 [22] on CIFAR-10 [18] to demonstrate that such numerical differences would not affect model convergence. We use a mini-batch size of 256 and the SGD [25] optimizer with a learning rate of 0.001 and a momentum of 0.9. The result plotted in Figure 6 shows that our algorithm has negligible impact on the convergence compared to the original BP.

4.2 Complexity Analysis

We leverage the following definitions to quantify the complexity of a parallel algorithm: (1) step complexity ($S$) which evaluates the number of steps on the critical path; (2) per-step complexity ($P$) which evaluates the runtime of a single step; and (3) work complexity ($W$) which evaluates the number of total steps executed by all workers. Assuming the system can be conceptualized as a parallel random-access machine (PRAM) [21], the number of workers is $p$ and the size of the input array in Equation 4 is $n + 1$, the step and work complexity of our algorithm can be derived as:

$$S_{Blelloch}(n) = \begin{cases} \Theta(\log n) & p > n \\ \Theta(n/p + \log p) & \text{otherwise} \end{cases}$$

$$W_{Blelloch}(n) = \Theta(n)$$

compared to $S(n) = \Theta(n)$, $W(n) = \Theta(n)$ of the linear scan (which has the same step and work complexity as BP). Therefore, in an ideal scenario where there is an unbounded number of workers with unit per-step complexity, our algorithm reduces the latency from $\Theta(n)$ to $\Theta(\log n)$. If, however, we consider the difference in per-step complexity between our algorithm ($P_{Blelloch}$) and the baseline
We prototype our algorithm with cuSPARSE [6] on a RTX 2070 GPU (Turing architecture) to perform sparse matrix-matrix multiplications, our algorithm has a latency of $\Theta(\log n) P_{\text{Baseline}}$ compared to $\Theta(n) P_{\text{Baseline}}$ in the baseline. There are two approaches to make our algorithm achieve a lower latency and better scaling than the baseline. First, we can reduce $P_{\text{Baseline}}$, which is reflected in leveraging the CSR sparse matrix multiplication routines analyzed in Section 4.3. Second, without a lower $P_{\text{Baseline}}$, our algorithm can still outperform the baseline if $P_{\text{Baseline}} / P_{\text{Baseline}} < \Theta(n / \log n)$. This can occur when $n / \log n$ grows larger than the dimension of $\vec{x}_i$. Possible use cases include computing inverse kinematics [23] of a long skeleton (such as simulating the movement of a snake) found in 3D animation.

4.3 Microbenchmark Analysis

We prototype our algorithm with cuSPARSE [6] on a RTX 2070 GPU (Turing architecture) to perform sparse matrix-matrix multiplications (csrgemm) and apply on the convolution layers of VGG-11 [30] (visualized in Figure 2) for training on CIFAR-10 [18]. The latency of every step (named \textit{per-step latency} for brevity) is derived by averaging the measurements via CUDA Events [5] from 50 trials after 5 warm-up runs. Each trial performs the backward pass for a single iteration of a single image sample. The goal is to reduce the per-step latency of our method to be below the maximum per-step latency of the baselines, which is measured under the same settings. Figure 7 shows the corresponding result. We can observe that many steps of sparse matrix-matrix multiplications meet the weaker baseline of the linear scan; however, a few have significantly higher per-step latencies.

Since the sparsity pattern can be determined ahead of time from the model architecture, the values in the CSR indptr and indices arrays [32] stay the same across batches and iterations. Therefore, the process of joining indptr and indices arrays in a generic csrgemm routine [2] could be omitted, and functions that transform the input data arrays to the output data array for each step can be generated and compiled \textit{a priori} before the training begins, potentially reaching better performance than cuSPARSE [6]. Considering the possibility of a better implementation, we project the lower bound of the per-step latency by measuring the number of floating-point operations (FLOP) performed on the CSR data arrays for each step and dividing it by the theoretical FP32 throughput of RTX 2070 [7]. The result is shown in Figure 7a from which we can observe that most steps meet the stronger baseline of PyTorch Autograd [24]; however, three matrix-matrix multiplications have latencies significantly higher than others. For every matrix-matrix multiplication, the number of non-zero elements (interpreted as $(1 - \text{sparsity})$ normalized by the size of the matrix) of the left and right operand matrices are plotted in Figure 8. We can observe that the sparsity helps reduce $P_{\text{Baseline}}$ as expected, and the three performance anomalies are caused by the loss of sparsity from the operands.

From Algorithm 4, we observe that the values in the Jacobian of a convolution operator only depend on the filter weights. Thus, pruning the weights can lead to a higher sparsity in the Jacobian, which would reduce the per-step latency of sparse matrix-matrix multiplications. Nevertheless, despite recent advances of network pruning algorithms [10] [29] [14], there is no existing widely adopted software or hardware platform that can capitalize on pruning, as most techniques are evaluated through "masking simulation" which leads to the same (if not worse due to masking) latency and memory usage. Therefore, we identify the \textit{retraining of pruned networks} as a strong use case that can benefit from our algorithm. We demonstrate such impact through an experiment on VGG-11 [30]: training on CIFAR-10 [18]; pruning away 97% of the weights in all convolution and linear operators using the technique proposed by See et al. [29], and retraining the pruned network. We choose this pruning percentage so that a similar validation accuracy can be reached (90.1% v.s. 88.9%) after retraining for the same number of epochs (100) as training. The lower bound projection on the per-step latency is derived via the same aforementioned method. Based on the result shown in Figure 7b, we can observe that all of the steps reach (with one anomaly that is close to) the stronger baseline of PyTorch Autograd [24].

5 Discussion

The runtime overhead added in the forward pass from generating the transposed Jacobian in CSR is not a primary concern because: for \textit{input-dependent} Jacobian (such as ReLU and max-pooling), the number of non-zero elements is at most the input size $\vec{x}_i$, which leads to extremely high sparsity and negligible overhead; and for \textit{input-invariant} Jacobian (such as convolution), the generation can be
Another approach to reduce the per-step complexity for sparse matrix-matrix multiplication is to use
Monte Carlo Approximate Matrix Multiplication \cite{8}. However, a trade-off between the convergence
rate and the per-step latency has to be made, as a lower per-step latency can be coupled with an
inaccurate matrix product which leads to noticeable errors in the resulting gradient vector \( \nabla_{x_i} l \).

The sparsity loss in the transposed Jacobian matrices comes from two possible sources. First, based
on Table\ref{tab:table1} when the ratio of \( \frac{h \times w_i}{h_i \times w_i} \) increases for convolutions, the sparsity of the Jacobian reduces.
This can occur when the activation \( x_i \) passes through max-pooling, and the height and width reduce
by the stride factor (half in the case of VGG-11 \cite{30}). This phenomenon is demonstrated in Figure \ref{fig:fig9a}
with the same experiment in Section 4.3. This issue is less limiting for retraining pruned networks
(Figure \ref{fig:fig9b}). Second, after the multiplication of two sparse matrices, the product matrix can have more
non-zero elements than the operand matrices. Therefore, the sparsity can reduce as the up-sweep
phase progresses to deeper levels. This can be observed from Figure \ref{fig:fig9b} by comparing \( L_3 \) with
previous levels. This challenge can be mitigated by balancing the number of levels that the up-sweep
phase progresses with the sparsity of the product matrices at each level.

Another approach to reduce the per-step complexity for sparse matrix-matrix multiplication is to use
Monte Carlo Approximate Matrix Multiplication \cite{8}. However, a trade-off between the convergence
rate and the per-step latency has to be made, as a lower per-step latency can be coupled with an
inaccurate matrix product which leads to noticeable errors in the resulting gradient vector \( \nabla_{x_i} l \).

Figure 7: Measuring or projecting the latency for each step. The orange and blue circles represent
matrix-vector and matrix-matrix multiplications respectively. A filled circle indicates that the step
is on the critical path. The red and blue dash lines represent the maximum per-step latency of the
linear scan and PyTorch Autograd baselines respectively. The x-axis represents the theoretical
complexity of the matrix-matrix or matrix-vector multiplications of the step if the transposed Jacob-
ians were full matrices. Each circle is annotated with the tag of the product corresponding to Figure 2.

Figure 8: The number of non-zeros in the (left, right) operands for all matrix-matrix multiplications and the corre-
sponding projected latencies.

Figure 9: Sparsity of all transposed Jacobian (inputs and intermediate results) in the up-sweep phase. Filled circle
represents the transposed Jacobian of convolutions. The x-axis represents the matrix tags corresponding to Figure 2.

Figure 8: The number of non-zeros in the (left, right) operands for all matrix-matrix multiplications and the corre-
sponding projected latencies.

Figure 9: Sparsity of all transposed Jacobian (inputs and intermediate results) in the up-sweep phase. Filled circle
represents the transposed Jacobian of convolutions. The x-axis represents the matrix tags corresponding to Figure 2.

Figure 8: The number of non-zeros in the (left, right) operands for all matrix-matrix multiplications and the corre-
sponding projected latencies.

Figure 9: Sparsity of all transposed Jacobian (inputs and intermediate results) in the up-sweep phase. Filled circle
represents the transposed Jacobian of convolutions. The x-axis represents the matrix tags corresponding to Figure 2.
6 Conclusion

This paper explores a new direction to scale BP. We reformulate BP into a scan operation which is scaled by our modified version of the Blelloch scan algorithm. While achieving superior scalability in terms of step complexity, per-step complexity increases due to multiplications of transposed Jacobian matrices during the up-sweep phase, as opposed to only multiplications of transposed Jacobian and gradient vectors in the baseline. We develop methods to efficiently generate the transposed Jacobian of various operators directly in CSR, and we leverage the CSR matrix multiplication routine (\texttt{csrgemm}) to reduce the per-step complexity. While \texttt{csrgemm} is an accessible tool for prototyping, we believe a more efficient implementation can be achieved since the sparsity pattern of the Jacobian is static and known ahead of time. We demonstrate that the retraining of pruned networks can potentially benefit from our algorithm. Future work includes investigating custom sparse matrix formats so that the per-step complexity can be reduced even further. We hope that our work will inspire radically new ideas and designs to improve distributed DNN training.

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