Realizable Reference Antiwindup Implementation for Parallel Controller Structures

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Abstract—Parallel controller structures are often used for the control of harmonic components in those power converters, including harmonic-compensation functions. The controlled signal can be distorted during the voltage saturation of the power converter output. This article proposes an implementation of the realizable reference antiwindup technique suitable for parallel controllers in multiple reference frames. The proposed implementation is simple and does not require a particular type of controllers nor special controller arrangements. The proposed implementation can be used for any kind of linear controller structure regardless of the variables being controlled. In the context of harmonic current controllers, the antiwindup implementation allows separating the harmonic controller outputs for canceling or decreasing them during steady-state saturation to improve the waveform quality. Different saturation options are analyzed for the inner loop current controller of grid-forming converter applications.

Index Terms—Current control, harmonic compensation, multifrequency, parallel controllers, saturation.

I. INTRODUCTION

DISTRIBUTED power generation systems (DPGSs) have increased their presence in the grid, especially those based on renewable energies, such as solar or wind energy [1]. Microgrids capable to operate independently of the grid are also increasing in size and quantity [2]. In both cases, there is a high percentage of nonlinear loads [3], injecting a significant amount of current harmonic content that eventually can distort the grid voltage. Therefore, requirements for harmonics content have been toughened up to improve general power quality [4]. Harmonic compensation can be implemented using dedicated units, as passive filters or centralized active filters [5], [6] are increasing the system cost. However, since the interface of DPGSs is generally based on power converters, this opens opportunities for harmonic compensation [6]. Harmonic compensation increases the voltage and current controller complexity requiring parallel structures [1]. The most used are those based on proportional-resonant (PR) controllers [7], also known as second-order generalized integrators (SOGI), and those based on synchronous proportional–integral (PI) controllers, implemented either in the synchronous or stationary reference frames [8], [9], also known as reduced-order generalized integrators (ROGIs).

Despite the controller type or design, there is always a maximum voltage available for compensation. Due to this, the current controller voltage demand can exceed the maximum available voltage under heavy load conditions, supply voltage drop, or if there is a sudden change of power demand. During a saturated state, two problems may arise: controller windup and harmonic distortion. Both situations can produce potentially dangerous overcurrents: windup can lead to a large overshoot in the controller response when the voltage is reestablished, and harmonic distortion can produce the loss of synchronization in grid-feeding applications, also leading to overcurrent.

There are different antiwindup methods for parallel controllers in the literature [10]–[16]. The controller windup can be avoided by individually saturating the parallel controllers to different preset values [10]. However, this solution does not ensure efficient voltage utilization and correct transition from the saturated state to the nonsaturated state. A backtracking algorithm with proportionally assigned gains for each controller has been proposed [11] to overcome this issue. Again, the need for preset saturation limits for each controller makes the solution inefficient in a general case. A state feedback antiwindup algorithm is proposed in [12]. This solution is essentially the same as [10] and [11] with a state-space formulation. A conditional cancellation of the multiple reference frame parallel controllers is proposed in [13]. It requires tuning of a voltage threshold to disable the controller integrators and the calculation of the control signal derivative to enable and disable the cancellation of the different controllers. The slow dynamic response of this solution makes it inefficient for continuously varying conditions. Moreover,
it requires a particular controller structure. An interesting
method has been recently proposed [16] for controllers in
the stationary reference frame. The antiwindup mechanism
locally applied to the different controllers in the parallel struc-
ture. The saturation limits for each controller are calculated at
every control sample following different strategies.

An effective realizable reference (RR) antiwindup technique
has been recently presented for stationary reference frame
parallel controllers [14], [15]. The implementation requires
a special formulation for the controller since it is efficiently
implemented as a single transfer function. Unfortunately, this
prevents manipulation of the individual parallel controllers’
outputs, which can be used to minimize harmonic distortion,
as will be discussed next. Moreover, the solution cannot be
used when different types of controllers are used or in different
reference frames.

Along with the windup problem, saturation also produces
waveform distortion in the controlled signals, and there have
different proposals to mitigate its effect [16]–[26]. A tra-
jectory analyzer is proposed in [17] and [18] to limit the
controller output in the case of saturation and avoid harmonic
injection. This analyzer is used to adapt the output voltage in
the stationary reference frame. The main drawback is that due
to its complexity, it is limited to fundamental and negative
sequence harmonic controllers. Moreover, the saturation is
considered with respect to the hexagon inner circle, limiting
the dc-link usage. A back-tracking scheme is proposed in [19]
for a parallel structure based on ROGI in multiple reference
frames. When output saturation is produced, the different
voltage components are adjusted in such a way that lesser
priority harmonics are removed from compensation. Although
simpler, this method does not entirely eliminate the distortion
and requires a particular controller structure. Harnefors et al.
[20] proposed a saturation scheme for a parallel structure
based on ROGI. When the output saturation is produced,
the different voltage components are adjusted following a
gain adjustment. The dynamic behavior of this method is
improved in [21], while it is extended to multiphase machines
in [22]. This proposal was further improved in [23], including
current limits to the control algorithm. The main drawbacks of
this method are the required tuning process and the dynamic
performance since the gain adjustment is driven by integral
controllers. In [24], a partial current harmonic compensation
for dual three-phase permanent magnet synchronous machines
(PMSMs) is proposed, based on manipulating the reference
signals for the current harmonics. Since this scheme is pre-
vented for an electric machine, torque production (fundamental
component) is favored over the current harmonics, whose
control is completely disabled if necessary. In this article, only
fifth and seventh harmonics are taken into consideration; the
partial compensation is based on finding the optimal compen-
sation level for each current harmonic \( \lambda_p \) based on a previous
commissioning process, which makes it impractical for general
application. Moriano et al. [25] proposed an instantaneous
method that calculates a trajectory that avoids overmodulation
at every time step to reduce the total harmonic distortion
(THD) maximizing the power injected to the grid. However,
this method is based on analytically solving nonlinear equa-
tions any time that a trajectory reduction is predicted, which
also increases the complexity as the number of harmonics to
compensate increases. In practice, the method maintains a low
THD of the injected current by decreasing the reactive power.
The computational burden of this method is reduced in [26].
Three saturation strategies intended for active power filters are
compared in [16]. The saturated voltage is calculated at every
control step in all cases.

This article generalizes the instantaneous RR algorithm
for application in parallel controller structures, which has
been initially drafted in conference paper [27]. The proposed
antiwindup implementation allows the proper saturation of
controllers in multiple reference frames, and it does not require
gain tuning. Furthermore, it is not restricted to any special type
of controllers, allowing to develop new controller types and
combine different controllers in different reference frames. It is
also noted that the proposed implementation can be applied to
any parallel controller structures regardless of the variables
being controlled.

The proposed antiwindup implementation is independent of
the strategy followed to reduce harmonic distortion during sat-
uration in current controllers. Cancellation or minimization of
the compensation of lower priority harmonics during saturation
is easily achieved. If required, any controller in the parallel
structure can be easily disabled by just setting its output to
zero. It can also be used in combination with the trajectory-
based methods proposed in the literature.

The antiwindup method is tested for proper saturation of
the inner loop current controllers of a grid forming application
although it is suitable for any application (e.g., grid support
and electric drives). In this regard, this article analyzes dif-
ferent options for the selection of the saturated voltage vector
to minimize current waveform distortion, recommending one
especially suited for grid-forming applications. In general,
researchers have focused on the concept of “distortion-free”
saturation methods [18]–[22], [25] for grid injection and
electrical machine current control. The main goal is preserving
the sinusoidal waveform shape of the currents injected to the
grid or electrical machines, rejecting harmonic distortion to
comply with grid codes or to minimize the torque ripple.
However, this always implies the reduction of the fundamental
component magnitude. This will reduce the injected power to
the grid or the fundamental torque component in electrical
machines. In the case of electrical machines, that strategy is
questionable but can still be useful for certain applications.
However, it will be shown that for grid-forming applications
in the presence of nonlinear loads, the saturation strategy goal
might be different since the preservation of the fundamental
component magnitude is the main requirement. This article
analyzes this extent.

This article is organized as follows. The RR anti-
windup implementation for parallel controllers is explained
in Section II. Different saturated voltage vector selection
strategies applied to the inner loop current controllers of grid
forming applications are described in Section III. The compari-
son of the proposed strategies is analyzed in Section IV, where
simulation results in open loop and closed loop are provided
with a special focus in grid-forming applications. Experimental
results are presented in Section V. Finally, a summary of the proposed ideas is found in Section VI.

II. RR FOR PARALLEL CONTROLLERS

A. Basic Concept

The transfer function of a discrete-time controller can be expressed as

\[ D(z) = \frac{u(z)}{e(z)} = \frac{b_0 + b_1 z^{-1} + \cdots + b_n z^{-n}}{1 + a_1 z^{-1} + \cdots + a_n z^{-n}} \]  

assuming that it has the same number \( n \) of poles as zeroes, where \( u \) is the controller output (i.e., inverter output voltage in a current controller); \( e \) is the error signal (i.e., current error in a current controller); and \( b_i \) and \( a_i \) (\( i = 1, 2, \ldots, n \)) are the polynomial coefficients. Note that \( u \) and \( e \) can be either scalar or complex vector quantities, as well as the polynomial coefficients.

The assumption of having the same number of poles as zeroes is not very restrictive since all continuous-time controllers discretized using the bilinear (Tustin), matched pole-zero, first-order hold, or backward Euler approximations will meet this condition. For the zero-hold, forward Euler, or modified matched pole-zero approximations, this condition is not necessarily met, resulting in discrete-time transfer functions that may have one more pole than zeroes. This can be circumvented by adding \((T/2)(z + 1)\) to the numerator of the controller, where \( T \) is the sampling period; the new controller exhibits a very similar response. Nevertheless, the discussion will be later extended to the case that the controller transfer function might have different numbers of poles than zeroes.

The difference equation needed for computer (e.g., microcontroller) implementation can be easily obtained as

\[ u[k] = \sum_{i=0}^{n} b_i e[k-i] - \sum_{i=1}^{n} a_i u[k-i]. \]  

(2)

The controller output must be limited to the actuator operating range to avoid controller windup. In the case of scalar output (i.e., using dc power source), a maximum and minimum voltage will be easily set

\[ u[k] = u_{sat} = \begin{cases} u_{max}, & \text{if } u[k] > u_{max} \\ u_{min}, & \text{if } u[k] < u_{min}. \end{cases} \]  

(3)

In the case of a complex vector output (i.e., using a three-phase inverter), more complicated expressions apply. Fig. 1(a) shows the maximum allowable voltage range using a three-phase inverter. It is given by a hexagon with radius \((2/3)V_{dc}\) and apothem \((V_{dc}/\sqrt{3})\), being \( V_{dc} \) the dc-link voltage. When the amplitude of a voltage command \( u \) surpasses the voltage hexagon limits, its amplitude must be limited or its phase distorted. In this case, multiple options exist. Commonly used options are shown in Fig. 1(a): \( u_{sat} \) keeps the original vector angle, \( u_{sat1} \) maximizes the \( q \)-axis component, and \( u_{sat2} \) maximizes the \( d \)-axis component. The hexagon limitation maximizes the inverter voltage utilization but brings implementation complexity, reference frame dependence, and the injection of additional harmonics when the voltage moves along the hexagon sides. To avoid this, the hexagon inscribed circle seen in Fig. 1(b) is often selected as voltage limit. To achieve those limits, either sinusoidal PWM (SPWM) with third harmonic injection or space vector modulation (SVM) is required.

Limitation of the digital controller output to the actuator limits prevents from windup but does not ensure a correct controller operation during the saturation state and a fast transition to normal operation when the saturation cause ceases. There exist different antiwindup mechanisms, as described in the introduction, the backcalculation or RR method \cite{28, 29} being the most effective and straightforward for digital implementation. It consists of calculating the error signal that would have made the controller to exactly produce the saturated output

\[ e_{sat} = \frac{1}{b_0} \left( u_{sat} - \sum_{i=1}^{n} b_i e[k-i] + \sum_{i=1}^{n} a_i u[k-i] \right). \]  

(4)

This value will be used as the previous step error signal in the next control period. This makes the controller always operate in the linear region, even under output saturation. Calculation of \( e_{sat} \) requires recalculating the last two terms on the right-hand side of (4) or storing those values during the controller computation. A simpler implementation is proposed next for the later extension to parallel controllers.

B. Efficient Implementation

The controller difference equation seen in (2) can be rewritten by extracting the first polynomial coefficient out of the summation

\[ u[k] = b_0 e[k] + \sum_{i=1}^{n} b_i e[k-i] - \sum_{i=1}^{n} a_i u[k-i]. \]  

(5)

In the case of saturation, the saturated controller output as a function of the realizable error (i.e., RR minus present output) can be calculated as

\[ u_{sat} = b_0 e_{sat} + \sum_{i=1}^{n} b_i e[k-i] - \sum_{i=1}^{n} a_i u[k-i]. \]  

(6)

By subtracting (5) from (6), a simpler expression only dependent on the last terms can be obtained

\[ u_{sat} - u[k] = b_0(e_{sat} - e[k]). \]  

(7)
Therefore, the realizable error can be easily calculated by only using the present period input and output of the controller

$$e_{sat} = e[k] + \frac{1}{b_0}(u_{sat} - u[k]). \quad (8)$$

C. Parallel Controllers in Stationary Reference Frame

In grid-forming, grid-connected, or active filter inverters, parallel controllers are often used for the control of the fundamental current (or voltage) and its harmonics. A structure using stationary reference frame parallel controllers can be seen in Fig. 2.

A backcalculation or RR antiwindup implementation has been proposed for a parallel structure composed of one proportional plus resonant harmonic controllers [14], [15] in a per phase scalar structure. The implementation in [14] and [15] allows the independent design of the fundamental and harmonic controllers and a straightforward antiwindup computation. The drawbacks are as follows: 1) it requires a special arrangement of the controllers; 2) the structure is limited to proportional plus resonant controllers; 3) individual controller outputs cannot be analyzed or limited; 4) it is only intended for controllers implemented in stationary reference frame; and 5) it is intended for scalar implementation. The antiwindup implementation proposed in this article overcomes those limitations.

The difference equation for the individual controllers is given as follows:

$$u_1[k] = b_{1,0}e[k] + \sum_{i=1}^{n_1} b_{1,i}e[k-i] - \sum_{i=1}^{n_1} a_{1,i}u_1[k-i] \quad (9a)$$

$$u_2[k] = b_{2,0}e[k] + \sum_{i=1}^{n_2} b_{2,i}e[k-i] - \sum_{i=1}^{n_2} a_{2,i}u_2[k-i] \quad (9b)$$

$$\vdots$$

$$u_x[k] = b_{x,0}e[k] + \sum_{i=1}^{n_x} b_{x,i}e[k-i] - \sum_{i=1}^{n_x} a_{x,i}u_x[k-i]. \quad (9c)$$

They are computed as $x$-independent controllers, where $u_j (j = 1, 2, \ldots, x)$ are the controller outputs, and $b_{j,i}$ and $a_{j,i} (i = 1, 2, \ldots, n)$ are the discrete-time controller coefficients. Please note that the error signal is common for all of them. The total controller output is the sum of the individual controller outputs

$$u_T[k] = \sum_{i=1}^{x} u_i[k]. \quad (10)$$

An identical result is obtained by summing the controller difference equations in (9), resulting in

$$u_T[k] = \sum_{i=1}^{x} b_{i,0}e[k] + \sum_{i=1}^{n_i} b_{i,i}e[k-i] - \sum_{i=1}^{n_i} a_{i,i}u_i[k-i]. \quad (11)$$

Similar to the single controller case, replacing the present output and error signal by their saturated counterparts gives

$$u_{sat} = \sum_{i=1}^{x} b_{i,0}e_{sat} + \sum_{i=1}^{n_i} b_{i,i}e[k-i] - \sum_{i=1}^{n_i} a_{i,i}u_i[k-i]. \quad (12)$$

Finally, subtracting (11) from (12) and after clearing $e_{sat}$ yield

$$e_{sat} = e[k] + \frac{1}{\sum_{i=1}^{x} b_{i,0}}(u_{sat} - u_T[k]). \quad (13)$$

The obtained result shows that the error backcalculation process is as simple as for a single controller. It must be remarked that (11) does not need to be computed; the parallel implementation [see (9) and (10)] is used instead. Finally, the fraction of saturation voltage corresponding to each parallel controller must be calculated

$$u_{i,sat} = u_i[k] + b_{i,0}(e_{sat} - e[k]) \quad \text{for } l = 1, 2, \ldots, x. \quad (14)$$

It is noted that only (13) and (14) must be computed for the antiwindup implementation once the saturated voltage ($u_{sat}$) is obtained. This implementation is advantageous since it allows disabling some harmonic controllers in the case of saturation as it will be discussed in Section III. Moreover, it mitigates rounding errors when combining large and small coefficients of the parallel controllers in a single controller implementation due to the numerical precision of the digital system [30].

In a general case, the parallel controllers can be designed and implemented in different reference frames. Therefore, an RR antiwindup implementation for multiple reference frames will be described next.

D. Parallel Controllers in Multiple Reference Frames

Different reference frames can be used for the design and implementation of the different controllers in the parallel structure, as can be seen in Fig. 3.

The error signal is first transformed into the different reference frames. Each controller produces an output in its
own reference frame; and finally, the outputs are transformed into a common reference frame (i.e., stationary) and added up. Superscript \( f_i \) (\( i = 1, 2, \ldots, x \)) is used to specify the different reference frames for the parallel controllers. The difference equations for the parallel controllers can be expressed as

\[
u_1^{f_1}[k] = b_{1,0}e^{f_1}[k] + \sum_{i=1}^{n_1} b_{1,i} e^{f_1}[k-i] - \sum_{i=1}^{n_1} a_{1,i} u_1^{f_1}[k-i] \tag{15a}
\]

\[
u_2^{f_2}[k] = b_{2,0}e^{f_2}[k] + \sum_{i=1}^{n_2} b_{2,i} e^{f_2}[k-i] - \sum_{i=1}^{n_2} a_{2,i} u_2^{f_2}[k-i] \tag{15b}
\]

\[\vdots\]

\[
u_x^{f_x}[k] = b_{x,0}e^{f_x}[k] + \sum_{i=1}^{n_x} b_{x,i} e^{f_x}[k-i] - \sum_{i=1}^{n_x} a_{x,i} u_x^{f_x}[k-i]. \tag{15c}
\]

After computation of the parallel controllers, the total output can be easily obtained

\[
u_T[k] = \sum_{l=1}^{x} \nu_l[k] = \sum_{l=1}^{x} u_l^{f_l}[k] e^{j\theta_l[k]} \tag{16}
\]

where \( \theta_l[k] \) is the angular position of the \( f_l \) reference frame in the present sampling period and “\( e^{j\theta} \)” is the Euler number.

Summing the difference equations in (15), after transforming them to a stationary reference frame, gives

\[
u_T[k] = \sum_{l=1}^{x} b_{l,0} e^{f_l}[k] e^{j\theta_l[k]} + \sum_{l=1}^{x} \left( \sum_{i=1}^{n_l} b_{l,i} e^{f_l}[k-i] \right) e^{j\theta_l[k]}
\]

\[\quad - \sum_{l=1}^{x} \left( \sum_{i=1}^{n_l} a_{l,i} u_l^{f_l}[k-i] \right) e^{j\theta_l[k]}. \tag{17}
\]

Writing the synchronous reference frame error signal in (17) in terms of the stationary reference frame error signal

\[e^{f_l}[k] = e[k]e^{-j\theta_l[k]} \tag{18}\]

results in

\[
u_T[k] = \sum_{l=1}^{x} b_{l,0} e[k] + \sum_{l=1}^{x} \left( \sum_{i=1}^{n_l} b_{l,i} e^{f_l}[k-i] \right) e^{j\theta_l[k]}
\]

\[\quad - \sum_{l=1}^{x} \left( \sum_{i=1}^{n_l} a_{l,i} u_l^{f_l}[k-i] \right) e^{j\theta_l[k]}. \tag{19}\]

This expression contains both the total controller output and the present error signal in the stationary reference frame.

Following the same thought process as in stationary reference frame, both the present voltage and error signals can be replaced by the saturated versions:

\[
u_{sat} = \sum_{l=1}^{x} b_{l,0} e_{sat} + \sum_{l=1}^{x} \left( \sum_{i=1}^{n_l} b_{l,i} e^{f_l}[k-i] \right) e^{j\theta_l[k]}
\]

\[\quad - \sum_{l=1}^{x} \left( \sum_{i=1}^{n_l} a_{l,i} u_l^{f_l}[k-i] \right) e^{j\theta_l[k]}. \tag{20}\]

By subtracting (19) from (20) and after clearing \( e_{sat} \), (13) is again obtained. Therefore, there is no difference in the calculation of the realizable error signal between the implementation in stationary or multiple reference frames. However, a final step is required in this case to provide the realizable error signal in each of the multiple reference frames

\[e_{sat}^{f_l} = e_{sat} e^{-j\theta_l[k]} \text{ for } l = 1, 2, \ldots, x. \tag{21}\]

The saturation voltage corresponding to each controller in the parallel structure can be then calculated similar to the stationary reference frame case

\[u_{f_{l,sat}}^{f_l} = u_{f_l}[k] + b_{l,0} \left( e_{sat}^{f_l} - e^{f_l}[k] \right) \text{ for } l = 1, 2, \ldots, x. \tag{22}\]

### E. Controllers With Different Numbers of Poles and Zeroes

As stated, the former expressions assume that each controller discrete-time transfer function has the same number of poles and zeroes. Note that this does not mean all the controllers in the parallel structure must have the same number of poles; it means that all the controller outputs are updated with the error value at the present instant. However, similar results can be obtained if the controllers have different numbers of poles than zeroes, while all of them have the same pole/zero difference

\[n_1 - m_1 = n_2 - m_2 = \cdots = n_x - m_x \tag{23}\]

where \( m_l \) is the number of zeroes of controllers, \( l = 1, 2, \ldots, x \). This means that all the controllers are updated with the same previous instant error value. Otherwise, a more complex and unpractical saturation scheme should be derived, in the case, the different controllers were updated with the error at different time instants. Although mathematically possible, this situation will not occur in practice.

### III. Saturation Strategies

Section II has demonstrated that the RR antiwindup technique can be easily implemented in the case of parallel controllers independently of the reference frame. This technique ensures a fast transition from saturated to nonsaturated state. However, this does not imply correct harmonic compensation or fundamental component realization during the saturated state. As it was described in Section I, several researchers [13], [16]–[21], [24], [25] have dealt with the problem of the voltage command adaptation during saturation. The use of the RR technique will further simplify the introduction of compensation mechanisms, but the fundamental component production and the harmonic distortion will depend on the selection of the saturated complex vector. As it was seen in Fig. 1, multiple saturation options exist when the controller output magnitude exceeds the hexagon limits. In the case of parallel controllers, an increased number of options exist. Fig. 4 shows the options analyzed in this article. It is considered that four parallel controllers would provide four voltage commands to exemplify the different analyzed options. The controllers are sorted (and numbered) in order of importance regarding fundamental component production and harmonic compensation, being \( u_1 \) the fundamental component.
Fig. 4. Saturation options analyzed. (a) Global. (b) Incremental-1. (c) Incremental-2. (d) Group (proposed method). (e) Trajectory. (f) Magnitude.

The distortion introduced by the different methods will depend both on the saturation level and the type of loads supported. The distortion can be minimized by using an appropriate saturation method. The methods can be categorized into three types: those that rely on the fundamental component, those that rely on the harmonic components, and those that use a combination of both.

The first type of method relies solely on the fundamental component. This type of method is simple to implement and requires no special treatment for the harmonic components. However, this type of method can result in high harmonic distortion.

The second type of method relies solely on the harmonic components. This type of method is more complex to implement and requires special treatment for the fundamental component. However, this type of method can result in low harmonic distortion.

The third type of method uses a combination of both the fundamental and harmonic components. This type of method is the most complex to implement and requires special treatment for both the fundamental and harmonic components. However, this type of method can result in the lowest harmonic distortion.

The choice of saturation method depends on the specific application and the desired level of harmonic distortion. The method that results in the lowest harmonic distortion may not be the most efficient in terms of voltage utilization. Therefore, a trade-off between harmonic distortion and voltage utilization must be considered when selecting a saturation method.
present in the system. A grid-forming scenario has been used to test the described alternatives. Fig. 5 shows a three-phase inverter with an output LC filter, an unbalanced three-phase linear load, and a nonlinear load. The main system parameters can be found in Table I. The linear and nonlinear loads draw about 40% and 35% of the rated power, respectively.

The inverter control goal is to obtain a balanced three-phase voltage at the filter output. The quality of this voltage will be used to benchmark the different methods. The typical grid-forming inverter control structure uses an outer voltage control loop controlling the capacitor voltage and an inner current control loop controlling the inverter currents. At steady state, the voltage controller will provide the adequate inverter current commands to achieve the desired voltage at the capacitors. To avoid the interaction of the voltage controllers in the analysis of the different saturation methods, the current commands at a steady state will be precalculated and not modified. Otherwise, the voltage controllers would react during saturation modifying the current commands and making the analysis very complex. The interaction with the voltage controllers is beyond the scope of this article.

The necessary current to achieve the desired capacitor voltage can be easily calculated by replacing the inverter and the filter inductor $L$ by an ideal three-phase source. Fig. 6(a) shows the current ($i_{id}$) needed to obtain the voltage trajectory at the filter capacitor ($u_{C_{id}}$) shown in Fig. 6(c). It is also possible to calculate the inverter voltage trajectory ($u_{id}$) to achieve both the inverter current and the capacitor voltage, as shown in Fig. 6(b).

An unrealistic bandwidth would be needed for the current controller to produce the trajectories shown in Fig. 6(a)–(c). Assuming a parallel controller structure composed of a fundamental current controller, a negative-sequence current controller, and five harmonic controllers, the modified trajectories shown in Fig. 6(d)–(f) are considered. They include the fundamental voltage at 50 Hz and harmonics at $-250, 350, -50, -550, 650, and -850$ Hz in decreasing order of magnitude. The resulting capacitor voltage shown in Fig. 6(f) has a small complex vector THD of $0.74\%$ and a magnitude error of $-0.01\%$. The magnitude error is defined as the difference between the magnitude of the fundamental component (i.e., 50-Hz component) of the capacitor voltage complex vector in steady state and the magnitude of the capacitor voltage command (i.e., ideal voltage) complex vector [see Fig. 6(c)]. The magnitude of the fundamental component is obtained by performing the fast Fourier transform (FFT) to the capacitor voltage complex vector. If only the fundamental component of the inverter voltage shown in Fig. 6(b) was injected, the THD would be $6.85\%$, the magnitude error is $-0.1\%$, and the phase-voltage unbalance is $0.58\%$.

If voltage saturation occurs, the previous trajectories will be distorted. The following discussion will analyze the resulting capacitor voltage trajectory when the different methods described in Section III are used. First, the open-loop analysis using the voltage trajectory shown in Fig. 6(e) will be carried out. This avoids the interaction on the current controller and the time to recover from saturation to better understand the different saturation options. Later, the closed-loop current control will be enabled to analyze the interaction of the current controller and the validity of the proposed RR implementation, as described in Section II. Three levels of saturation are imposed assuming dc-link voltages of 600, 570, and 540 V. The corresponding hexagon limits can be seen in Fig. 7.

### A. Open-Loop Analysis

The different saturation strategies described in Section III are analyzed in simulation. The simulations have been carried out using the Specialized Power Systems library of the MATLAB/Simulink Simscape Electrical toolbox. The control
routines have been coded in C language. The inverter shown in Fig. 5 is simplified by using a linear voltage source to speed up the simulations. The voltage trajectory in Fig. 7 is the inverter voltage command before saturation. The measured capacitor voltage THD, fundamental voltage magnitude error, the fundamental voltage phase angle, and the phase unbalance are taken as figures of merit for the different methods. The phase angle is given with respect to the nonsaturated capacitor voltage, whose trajectory is shown in Fig. 6(f). The phase unbalance is calculated as the difference between the fundamental peak of the highest and smallest phase voltages is normalized by the mean phase voltage.

Table II summarizes the obtained results. Focusing first in the direct saturation methods, it can be seen that the Group strategy [see Fig. 4(d)] gives both low THD and magnitude error. The Global strategy [see Fig. 4(a)] offers the second-best results for THD and magnitude errors and the best for angle phase distortion and unbalance; moreover, it has the benefit of being the simplest for computer implementation. The Incremental strategies [see Fig. 4(b) and (c)] do not provide good results; this, in addition to their increased complexity, discards them for the closed-loop analysis. All methods have been tested using both the hexagon and circle limits. As expected, a better THD is obtained in all cases with the circle limit but at the cost of a higher magnitude error and unbalance.

Voltage trajectories fitting the hexagon limit were synthesized from the original trajectory with three different strategies: decreasing the overall voltage (Global), canceling harmonics until the trajectory fits in the hexagon (Incremental-1 and 2), and reducing first the grouped harmonic components (Group). As can be seen in Table II, the Trajectory Global strategy preserves the original (i.e., unsaturated) THD, but the magnitude error is larger than in other methods. The small voltage margin left by the fundamental component makes the other two trajectory strategies to have worse THD than nontrajectory methods. The advantage of both the Trajectory Group and the Trajectory Incremental strategies over the Trajectory Global Strategy is that they better preserve the fundamental magnitude under light saturation and the fundamental voltage phase under deep saturation. It must be remarked that these are best-case results trying to resemble the behavior of trajectory-based methods. In practice, tracking the feasible trajectory is not straightforward, and worse results should be expected. The preservation of THD shown by the Trajectory Global method makes this strategy ideal for grid supporting applications, but grid forming applications require both harmonic quality and preservation of the fundamental voltage. A weighting algorithm could be implemented to trade-off THD and fundamental voltage reduction. However, that is far beyond the scope of this article.

The Magnitude strategy [see Fig. 4(e)] shows similar results to trajectory-based methods. However, in the case of the Global strategy, the worst voltage utilization by both using the circle limit and neglecting the component phases makes the fundamental magnitude error to be significantly higher.

B. Closed-Loop Analysis

The validity of the proposed antiwindup algorithm is analyzed in combination with some saturation strategies selected from the previous discussion. The Global and Group strategies are selected for their implementation simplicity and good results, respectively. The online adaptation of the current commands proposed by trajectory methods is beyond the scope of this article, and they have not been implemented.

The current trajectory shown in Fig. 6(d) is commanded to a current controller using a parallel structure (see Fig. 3) composed of seven complex vector PI controllers [31] for the fundamental, negative sequence, and main five harmonic components. Each controller is independently tuned in its reference frame. The measured capacitor voltage is used as a feedforward term for disturbance decoupling. This feedforward signal and the output of the fundamental current controller will be considered as the fundamental voltage component for the saturation strategy implementation. It is noted that the feedforward term can also contain harmonic content during transients and also in steady-state if low harmonic distortion is not achieved.

The capacitor voltage THD using this controller and assuming no saturation is 1.03%, the fundamental voltage component magnitude error is 0.1%, and the phase unbalance is 0.04%. Linear sources are first used in the simulation to separate the effects of the current controller bandwidth and antiwindup method from the inverter nonlinear behavior. When inverter voltage saturation is introduced, the results shown in Table III are obtained. Slightly increased THD and magnitude distortion values compared with those obtained for the open-loop inverter voltage are obtained. This is explained by the bandwidth limitation of the controllers. Nevertheless, the comparative results are similar to the case of open-loop voltage injection, meaning that the proposed antiwindup implementation is working as expected.

To prove the validity of the described antiwindup technique, the Group hexagon saturation strategy was also implemented without the proposed antiwindup algorithm in two cases: first, calculating the individual output voltages after saturation according to the given strategy (see “State saturation (SS)” in Table III); second, limiting only the global controller output according to the same strategy but not calculating the individual outputs (see “No SS” in Table III). The results are
### TABLE II
CAPACITOR VOLTAGDistortion Using Different Saturation Strategies for Open-Loop Inverter Voltage Command

| Method   | THD (%) | Mag. Error (%) | Angle (deg) | Unbal. (%) | THD (%) | Mag. Error (%) | Angle (deg) | Unbal. (%) | THD (%) | Mag. Error (%) | Angle (deg) | Unbal. (%) |
|----------|---------|----------------|-------------|------------|---------|----------------|-------------|------------|---------|----------------|-------------|------------|
| Global (circle) | 2.17    | 0.99           | 0           | 0.10       | 4.1     | 3.23           | 0.06        | 0.02       | 3.64    | 6.43           | 0           | 0.21       |
| Global (hexagon) | 2.17    | 0.99           | 0           | 0.10       | 4.1     | 3.23           | 0.06        | 0.02       | 3.64    | 6.43           | 0           | 0.21       |
| Incremental-1 (circle) | 4.47    | 1.27           | 0.25        | 0.11       | 6.0     | 6.43           | 0.53        | 0.04       | 6.32    | 6.44           | 0.13        | 0.57       |
| Incremental-1 (hexagon) | 4.47    | 1.27           | 0.25        | 0.11       | 6.0     | 6.43           | 0.53        | 0.04       | 6.32    | 6.44           | 0.13        | 0.57       |
| Incremental-2 (circle) | 3.04    | 1.96           | 0.24        | 0.37       | 4.38   | 4.34           | 0.53        | 0.14       | 6.32    | 6.44           | 0.13        | 0.57       |
| Incremental-2 (hexagon) | 3.04    | 1.96           | 0.24        | 0.37       | 4.38   | 4.34           | 0.53        | 0.14       | 6.32    | 6.44           | 0.13        | 0.57       |
| Group (circle) | 1.87    | 1.28           | 0.23        | 0.10       | 5.28   | 5.22           | 0.64        | 0.01       | 5.28    | 5.22           | 0.64        | 0.01       |
| Group (hexagon) | 1.87    | 1.28           | 0.23        | 0.10       | 5.28   | 5.22           | 0.64        | 0.01       | 5.28    | 5.22           | 0.64        | 0.01       |
| Trajectory Global | 0.74    | 0.15           | 0           | 0          | 0.74    | 0.14           | 0           | 0          | 0.74    | 0.14           | 0           | 0          |
| Trajectory Incremental | 0.74    | 0.15           | 0           | 0          | 0.74    | 0.14           | 0           | 0          | 0.74    | 0.14           | 0           | 0          |
| Magnitude Global | 0.74    | 0.15           | 0           | 0          | 0.74    | 0.14           | 0           | 0          | 0.74    | 0.14           | 0           | 0          |
| Magnitude Incremental | 0.74    | 0.15           | 0           | 0          | 0.74    | 0.14           | 0           | 0          | 0.74    | 0.14           | 0           | 0          |

### TABLE III
CAPACITOR VOLTAGDistortion Using Different Saturation Strategies for Closed-Loop Inverter Current Injection

| Method   | THD (%) | Mag. Error (%) | Angle (deg) | Unbal. (%) | THD (%) | Mag. Error (%) | Angle (deg) | Unbal. (%) | THD (%) | Mag. Error (%) | Angle (deg) | Unbal. (%) |
|----------|---------|----------------|-------------|------------|---------|----------------|-------------|------------|---------|----------------|-------------|------------|
| Global (circle) | 2.79    | 2.16           | -0.05       | 0.34       | 7.84    | 6.94           | 1.17        | 0.86       | 7.72    | 11.18          | -2.58       | 11.17      |
| Global (hexagon) | 3.14    | 1.54           | -0.03       | 0.56       | 6.28    | 6.24           | -0.53       | 1.08       | 9.46    | 10.81          | -1.51       | 1.52       |
| Group (circle) | 2.97    | 2.16           | -0.05       | 0.34       | 7.84    | 6.94           | 1.17        | 0.86       | 7.72    | 11.18          | -2.58       | 11.17      |
| Group (hexagon) | 3.14    | 1.54           | -0.03       | 0.56       | 6.28    | 6.24           | -0.53       | 1.08       | 9.46    | 10.81          | -1.51       | 1.52       |
| Trajectory Global | 0.74    | 0.15           | 0           | 0          | 0.74    | 0.14           | 0           | 0          | 0.74    | 0.14           | 0           | 0          |
| Trajectory Incremental | 0.74    | 0.15           | 0           | 0          | 0.74    | 0.14           | 0           | 0          | 0.74    | 0.14           | 0           | 0          |
| Magnitude Global | 0.74    | 0.15           | 0           | 0          | 0.74    | 0.14           | 0           | 0          | 0.74    | 0.14           | 0           | 0          |
| Magnitude Incremental | 0.74    | 0.15           | 0           | 0          | 0.74    | 0.14           | 0           | 0          | 0.74    | 0.14           | 0           | 0          |
| No state saturation | 8.30    | -6.73          | -3.34       | 1.16       | 9.78    | -0.48          | -0.64       | 1.18       | 9.78    | -0.48          | -0.64       | 1.18       |

The transient response was also analyzed through simulation before the experimental verification. Fig. 8(b) shows the current commands before and after the RR calculation. The Group saturation strategy is used. It is remarked the calculation of the RR is not strictly required in the implementation, but it better explains the technique behavior. Both commands are the same before 0.5 s since the controller output is not saturated. At $t = 0.5$ s, the dc-link voltage drops to 500 V (33% drop) [see Fig. 8(a)]. At this moment, the RR (continuous line) is calculated, differing from the nonsaturated command (dotted line). The actual currents follow the RRs as can be seen in Fig. 8(c). The RR reaches a steady state in one fundamental cycle, while the actual current needs around two cycles in this example. It is noted that the filter and load parameters for this simulation are the ones for the experimental setup, as shown in Section V.
**TABLE IV**

**Experimental System Parameters**

| Parameter          | Value  |
|--------------------|--------|
| Rated voltage $V_r$ | 400 Vrms |
| Rated current $I_r$ | 16 A rms |
| Filter $L$         | 2 mH   |
| Filter $C$         | 16 μF  |
| Linear load $R_t$  | 35 Ω   |
| Linear load $L_d$  | 2.4 mH |
| Linear load Unbalance | ±25% |
| Non-linear load $C_{nl}$ | 500 μF |
| Non-linear load $R_{nl}$ | 106 Ω |

**Fig. 10.** Current controller including RR antiwindup.

**Fig. 11.** Current commands and predicted voltage trajectories for the experimental system. (a) Inverter current. (b) Inverter voltage. (c) Capacitor voltage.

**V. EXPERIMENTAL RESULTS**

The experimental setup consists of an interleaving dc/dc converter and a grid-forming dc/ac converter manufactured by ELINSA. The dc/dc converter is intended to interface a LiFePO4 battery pack, but, in this work, it is used to force dc-link voltage variations. An $LC$ filter is used to smooth the output voltage to supply the loads, with the structure shown in Fig. 5. The experimental setup can be seen in Fig. 9. The converter control stage is based on a Texas Instruments TMS320F28335 digital signal controller board. The dc/ac converter switching and control frequency is 10 kHz.

The proposed RR antiwindup implementation along with the Group saturation strategy was experimentally tested. Due to laboratory power constraints, the inverter $LC$ filter and the load shown in Table I were resized to the values shown in Table IV to allow voltage saturation within the lab current limit. The linear load absorbs 41% of the rated power and the nonlinear load around 32%.

The current controller can be seen in Fig. 10. The controller is composed of eight complex vector PI controllers for the fundamental, dc component, negative sequence, and the main five harmonic components ($-250, 350, -550, 650, \text{and} 950 \text{ Hz}$). As in simulation, each controller is independently tuned in its reference frame. The measured capacitor voltage $u_{C_{dq}}$ is used as a feedforward signal for disturbance decoupling. The capacitor voltage feedforward term of the current controller creates a positive feedback loop for the dc component, giving rise to large dc offsets and even to controller output saturation. To avoid this, a dc component controller is added to the parallel structure. The sum of the feedforward signal and the fundamental and dc current controller outputs will be considered as the main voltage component for the Group saturation strategy.

The measured inverter current $i_{q_{d}}$ is compared with the current trajectory command, $i_{q_{d}}$, as shown in Fig. 11(a). This trajectory is obtained in simulation using the experimental setup parameters, as described in Section IV. Fig. 11(b) shows the corresponding theoretical nonsaturated inverter voltage trajectory, and Fig. 11(c) shows the resulting capacitor voltage when the described harmonics are injected. This must be taken as the best output voltage trajectory achievable by the implemented controller structure. The THD in the capacitor voltage is 3.28% due to the strong nonlinear load selected.
To decrease the THD below 1%, five additional parallel harmonic controllers would be required. Compensation of those additional harmonics would require the direct discrete-time design of the controllers [34] or delay compensation [35], which is out of the scope of this article. However, the THD is still below 8%, which is the limit recommended by the IEEE Standard 519-2014 [4] for voltages below 1000 V. The resulting voltage $u_{qg}$ from the control loop, after proper saturation, is commanded to the inverter using SVM.

The RR block (Real. Ref. in Fig. 10) is computed according to the flow diagram shown in Fig. 12. The function receives the present period controller error and outputs (i.e., voltage commands). According to the voltage limit selected, circle or hexagon, the maximum voltage available is calculated. This step is straightforward in the case of the circle limit, but it needs some computation time in the case of the hexagon. Once the limit is obtained, a magnitude comparison is done with the actual voltage command. Nothing is done if the voltage command does not exceed the limit. On the contrary, a voltage command replacement must be selected according to the trajectories described in Section III. Then, only by computing the equations in the blocks of Fig. 12 labeled as “RR antiwindup,” the antiwindup algorithm is performed.

The execution times of this algorithm using the 32-bit 150-MHz TMS320F28335 microcontroller are given in Table V for the controller structure used in this section (eight parallel controllers) and adding five additional harmonic controllers. The hexagon limit and the Group strategy are implemented. It is also included the time to compute the controllers, not included in the flow diagram in Fig. 12. It can be seen that the most demanding part of the algorithm is the calculation of the saturated voltage, but it is still affordable for medium performance microcontrollers. Circle limit strategies reduce this time. It is noted that the total time in the table does not include additional functions as AD converters reading, SVM, or protection functions.

Fig. 13 shows the trajectory of the actual nonsaturated inverter voltage command when the current trajectory seen in Fig. 11(a) is commanded. The differences with the theoretical trajectory shown in Fig. 11(b) are due to the inverter nonidealities. Voltage hexagon limits for dc-link voltages of 750, 570, and 500 V are also shown in Fig. 13. While
Fig. 15. Experimental. RR antiwindup performance during saturation and transition to nonsaturated state. (a) DC-link voltage (500 V → 750 V). (b) Phase currents (solid line) and current commands (dashed line). (c) Capacitor voltages. Blue: phase-a; red: phase-b; and black: phase-c.

A 750-V dc-link voltage ensures nonsaturated operation, both 570 and 500 V impose increasing levels of saturation. These dc-link voltage levels will be used to test the proposed method performance.

Fig. 14 compares the behavior of the proposed RR method versus a simple SS. In the latter case, when the controller output exceeds the voltage hexagon limits, it is also limited following the Group strategy, and the corresponding individual controller outputs are calculated, but the RR (i.e. error) is not computed. This prevents from windup [28], [29] but does not ensure a bumpless transition from the saturated to the nonsaturated state.

Fig. 14(a) shows a dc-link voltage transition from 570 to 750 V. Fig. 14(b) and (d) shows the inverter output current commands and actual phase currents. It can be observed that the current during saturation cannot accurately follow the command, but the distortion is small for RR, while, in the case of SS, there is noticeable distortion. Moreover, when the dc-link voltage is restored, the RR algorithm ensures a fast transition to the correct signal tracking (less than one fundamental cycle). SS transition is slower, needing seven fundamental cycles for complete recovery (not shown in the graph).

VI. CONCLUSION

This article develops and demonstrates a simple way of implementing the RR antiwindup technique for parallel controllers in multiple reference frames. The proposed implementation allows us to use any kind of controller and, if required, seamless modification of single controller outputs during saturation. The proposed antiwindup technique can be applied to any parallel linear controller structure, regardless of the variables being controlled. However, the choice of the saturated value will depend on the application.

Different saturation options are available and can be easily applied if this technique is used for current controllers. The
selection will depend on the final application (e.g., grid support and grid form). Grouping the harmonic controller outputs shows excellent results for the inner loop current controllers in grid-forming applications. Simulation and experimental results demonstrate the feasibility and performance of the proposed antwindup implementation in the current controllers of grid-forming inverters, even under deep dc-link voltage drop.

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