High Dielectric Constant Materials for Nanoscale Devices and Beyond

by Hiroshi Iwai, Akira Toriumi, and Durga Misra

The feature size of a metal oxide semiconductor field effect transistor (MOSFET), the driving force behind the silicon microchips, has approached the 10 nm range and below. The gate dielectric, being the critical constraint, has evolved significantly with the introduction of high dielectric constant (high-k) materials with metal gates and requires constant quality improvements to maintain the proper functioning of the transistors and memory devices in the 10-nm technology node. Many new devices such as nanowire devices, Ge, III-V semiconductors, graphene, 2D-semiconductor channel replacement devices, and tunnel FETs are emerging for the extension of complementary metal oxide semiconductor (CMOS) technology. Some of the most promising devices for beyond-CMOS technology that might replace silicon transistors include spin-FET, negative gate-capacitance FET and all-spin logic devices. All these devices will use high-k materials at some point or the other.

In 2005 an article was published in Interface in high-k dielectrics into CMOS technology for commercial production. It was predicted that high-k dielectric materials would be part of mainstream technologies. Even though many of the materials problems have been solved and many technologies have matured in the interim, many other challenges have also emerged. In this article, we provide a historical perspective of high-k dielectric development and discuss new understanding, applications and reliability aspects of high-k gate dielectrics for current and future nanoscale devices.

History of High-k Gate Insulator Development

Although successful operation of the MOSFET was achieved using a SiO₂ gate insulator in 1959, the SiO₂ gate film had problems of high defect density and a large amount of impurities, which caused significant yield and reliability issues in the 1960s. Several insulators, such as Si₃N₄, Al₂O₃, and even ZrO₂ were investigated to solve the problems. For example, it was found that Si₃N₄ and Al₂O₃ had the merit of better surface protection from contamination or impurity diffusion. However, the interfacial and bulk trap densities of these films were very high. These films were later used in nonvolatile memory structures such as MNOS (Metal Nitride Oxide Semiconductor) and MAOS (Metal Aluminum Oxide Semiconductor). Meanwhile, Ta₂O₅ and Al₂O₃ were used to replace the SiO₂ capacitor in DRAM (Dynamic Random Access Memory). Since the huge merits of the miniaturization or scaling of MOSFETs were recognized in early 1970s, the thickness of the SiO₂ gate films has been continuously decreased. However, in the past, it was predicted that the limit of the gate SiO₂ thickness would be 3 nm because of the onset of the direct-tunneling gate leakage current. It was demonstrated later, in 1994, that a small gate length transistor could still function well by using a 1.5 nm thick SiO₂ gate insulator. The direct-tunneling gate leakage current of the small channel gate area was still sufficiently negligible so as not to affect the I₅-V₅ characteristics. Thus, SiO₂ film with a small concentration of nitrogen with thickness less than 3 nm has been used for LSIs since then. However, the total gate leakage current at a chip level became an issue when the gate oxide thickness approached 1.0 nm.

To suppress the direct-tunneling gate leakage current, replacing the SiO₂ with a high-dielectric constant (or high-k) insulator was recognized as a solution. It was expected that similar magnitude of I₅-V₅ characteristics with suppression of the gate leakage current could be obtained using a physically-thick high-k gate film. Thus, it had been vaguely proposed that such sub-3 nm thick gate insulators would be necessary for sub-100 nm gate length generations. However, the development of high-k gate insulators for MOSFETs had not been seriously undertaken, because it was not known at all if such small (sub-100 nm) gate length MOSFETs could operate successfully, and also, because alternative dielectric films at that time were found to have a much poorer interface.

Therefore, the exploration of some high-k materials such as Si₃N₄, TiO₂, Ta₂O₅ and Y₂O₃ did not start seriously until the mid-1990s. In the early 1990s, the operation of the MOSFETs of gate length down to 25 nm was confirmed by performing Monte Carlo simulations. It was predicted that for a MOSFET with a gate length below 50 nm, the gate insulator materials should be high permittivity or high-k, in general, as shown in Fig. 1. Although the operation of 40 nm gate length transistors was verified by experiments in 1993, it was still based on the SiO₂ gate insulator as high-k technology was not available at that time.

Subsequently, sub-50 nm gate length MOSFETs were integrated in the scope of the industry, and the search for alternate gate dielectric materials applicable for future sub-50 nm gate length CMOS-LSIs became a challenge. Eventually, ZrO₂ and HfO₂, having similar characteristics, were considered as the most promising candidates because of the suitable dielectric constant, band offset values between the silicon and the dielectric, as well as thermal stability during the fabrication process. In the 1999 International Electron Devices Meeting (IEDM), MOSFETs with ZrO₂ or HfO₂ as gate insulators were reported for the first time by several groups. Later, it was found that HfO₂ had a better thermal stability than ZrO₂. However, there were still a number of issues, such as thermal stability, mobility degradation, threshold voltage control issue, and Fermi-level pinning, that needed to be resolved.

Then, HfO₂ high-k gate insulators with interfacial SiO₂ film were introduced into 45 nm CMOS technology in 2007. In the latest 14-10 nm CMOS technology, HfO₂-based oxide is still used but the interfacial SiO₂ layer has been removed to lower the EOT down to the sub-nanometer range. Figure 2 summarizes the issues in high-k/metal gate stack technologies. The issues have been solved for use for each generation of the scaling.

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New Understanding and Applications of High-k Dielectrics

HfO$_2$ has been used in advanced CMOS technology since 2007. High-k dielectrics keep the scaling equivalently, because the gate capacitance can be scaled down without physically reducing the oxide thickness. In the early stage of high-k research, high-k gate FET formation processes such as gate first or gate last processes have been intensively investigated. A number of challenges have arisen upon introducing high-k gate stacks. The direct HfO$_2$/Si interface was always worse than SiO$_2$/Si interface, and, as a result, the interface carrier mobility was degraded considerably. In addition to the enhanced Coulomb scattering due to the interface states and/or bulk trapped charges, a new type of scattering mechanism, remote phonon scattering, was proposed. Interlayer SiO$_2$ was introduced to improve the interface quality by avoiding direct contact with Si. This remains a fascinating topic from the device physics viewpoint.

Meanwhile, the FET threshold voltage in high-k gate stacks was different from that in SiO$_2$/Si. This was elegantly characterized by considering the dipole formation at the high-k/SiO$_2$ interface. Figure 3 shows the experimental evidence of the high-k/SiO$_2$ scavenging process. By taking account of the interface dipole, the threshold voltage should be described as follows:

$$V_{th} = \Phi_{AS} + \Phi_{dipole} + 2\phi_e + \frac{2\varepsilon_{Si} qN_F (2\phi_e)}{C_{ox}}$$

in which $\Phi_{dipole}$ is not included in SiO$_2$/Si gate stacks. This is interesting because an electric dipole is formed at insulator/insulator interfaces, and the dipole direction and magnitude are high-k-material dependent. Although the dipole formation mechanism is still under debate, our simple model that the dipole may be generated from the oxygen atom concentration difference at the interface can explain most experimental results. In addition, the interlayer SiO$_2$ between the high-k film and Si should considerably increase EOT (equivalent oxide thickness) in the ultra-thin EOT region. So, it was considered whether the interlayer could be scavenged by optimizing the PDA conditions of gate stacks. This interlayer SiO$_2$ scavenging process was also interesting to study both practically and theoretically. In particular, the Si kinetics in SiO$_2$ was mysterious in the scavenging process. We found that the scavenging was very sensitive to the substrate, which strongly suggested Si out diffusion from SiO$_2$ to HfO$_2$ due to the Si chemical potential gradient in the gate stack.

The dielectric constant of HfO$_2$ is ~18, and higher-k dielectrics will obviously be needed sooner or later to enhance the FET performance. It is technically important to decide whether a new higher-k material should be searched for or whether HfO$_2$ should be further used. We have been interested in the structural phase control of HfO$_2$ to enhance the dielectric constant, because 1st-principles calculation predict that high temperature phases of HfO$_2$ such as cubic or tetragonal phases have a higher-k than the amorphous or monoclinic phases. The monoclinic phase, however, is thermodynamically stable at Si processing temperatures, so usually cubic- or tetragonal-phase HfO$_2$ should be intrinsically unavailable. Nevertheless, significant enhancement of the dielectric constant in HfO$_2$ was actually demonstrated through the stabilization of the cubic or tetragonal phase. The key factor was the structural phase transformation by doping another metal-oxide onto HfO$_2$. The typical example was Y$_2$O$_3$-doped HfO$_2$. In fact, it had been well recognized in the ceramics community for a long time that Y$_2$O$_3$ doping could induce the oxygen vacancy in ZrO$_2$ to maintain the charge neutrality and more symmetric phase such as cubic or tetragonal than monoclinic.

Recently, ferroelectric HfO$_2$ was reported as shown in Fig. 4. We, very unfortunately, could not notice that HfO$_2$ ferroelectricity emerged upon doping with other oxides, though we had carried out the same type of experiments as described above. An interesting point in the ferroelectric HfO$_2$ is that the ferroelectric orthorhombic phase is not in the conventional phase diagram. Very recently, we found that ferroelectric HfO$_2$ can also be made by anion doping into HfO$_2$. The key is how to realize the non-centrosymmetric phase HfO$_2$ structure. The ferroelectric orthorhombic phase might lie between the monoclinic and tetragonal phases as a metastable state. This fact has made it more difficult to recognize such unexpected but advantageous functionality easily. In case of ferroelectric HfO$_2$, a couple of nanometers thick ferroelectric film is viable and its application is promising.

New semiconductor substrates such as III-V, Ge and 2D materials are now under investigation. In fact, the interface of high-k films with such substrates are quite different from that formed with Si. In case of Ge, for example, most of the studies have been interested in exploring interlayer GeO$_2$ on Ge by mimicking the SiO$_2$/Si case.
Reliability Issues in High-k Dielectrics

Reliability of high-k gate stacks has been a serious issue over several generations in the context of integrating high-k materials and its variations. Understanding the charge trapping behavior in the dielectric and at the interface has been the trend to evaluate its reliability. Furthermore, the gate stack’s response to electrical stress, especially the bias temperature instability (BTI), is another critical issue for threshold voltage shift (ΔVT) in nanoscale devices. Self-heating in FinFETs further adds to the problem of BTI.43 The other vital issue of reliability of high-k gate stacks is related to stress-induced dielectric breakdown. Studies of breakdown characteristics of high-k gate stacks are made complicated by the fact that the potential drop/electric field across interfacial and high-k layers are different due to the differences in the values of the dielectric constant and thickness.44,45 Once the EOT goes down below 0.7 nm for silicon devices, and when germanium is introduced as the channel material, the reliability problem can be exacerbated.

High-k gate dielectrics are known to have a much larger pre-existing intrinsic trap density compared to silicon dioxide. These traps, responsible for electron/hole trapping, can be classified into three groups46 according to their locations within the bulk high-k bandgap as shown in Fig. 5. Group A defect levels lie above the Si conduction band edge, ECB, and remain empty under “zero bias,” i.e., zero electric field and thermal equilibrium conditions. However, under “non-zero” gate bias such states facilitate the tunneling of electrons from ECB/gate through the thin interfacial layer (IL). Thus, they serve as the electron traps. Once the bias is removed, very fast (within μs) de-trapping to the substrate/gate occurs from these states. Hence, these shallow levels give rise to fast transient trapping of electrons, which is mostly responsible for hysteresis and mobility degradation. Group B defects lie within the Si bandgap range. Under “zero bias” conditions, carriers trapped in these deep states de-trap slowly to the substrate, depending on the physical distance from the substrate, and the activation energy w.r.t. to ECF, which gives rise to slow transient trapping. ΔVT due to trapping at these deep levels is the most critical reliability factor for the high-k dielectrics. Electrons trapped at levels below ECF (Group C) give rise to fixed oxide charges.

Since the introduction of HfO2 in mainstream technology its reliability has been extensively studied under different stress conditions.46,49 However, the negative bias temperature instability (NBTI) for p-channel MOSFETs and positive bias temperature instability (PBTI) for n-channel MOSFETs remain as serious degradation mechanisms when device temperature is increased.1 Interface state defect generation triggered by Si-H bond breaking at the interface is a point of major concern. One of the widely-used NBTI models is based on reaction-diffusion (R-D) theory, which basically focuses on time dependent net increase in the number of interface defects taking place during electrical stress at elevated temperatures. PBTI has become a concern for high-k devices even though it was not a serious concern for Si/SiO2 devices. Recent evidence of self-heating in FinFETs has also become a growing concern.44 Since the thermal resistance of these devices has increased from that of planar to bulk FinFET and into SOI FinFET, it is expected to increase even further in future devices like gate-all-around transistors. The impact of self-heating further enhances the NBTI or PBTI degradation process in these devices.50

High-k gate stacks are usually represented by a multi-layer structure that includes a high-k dielectric and a thin interfacial layer. Each of these layers, in turn, is affected by interlayer material interactions, in particular, a metal electrode may affect composition of the gate dielectric and a high-k film may change the stoichiometry of the underlying interfacial layer.46 Stress-induced degradation of the dielectric stack can originate from defect generation in both the high-k layer and in the interfacial layer, in which degradation is expected to be controlled by different mechanisms. The investigation of breakdown characteristics suggests that the breakdown of the gate stack is typically triggered by defect generation in the thin SiO2 interfacial layer.

Several intermediate treatments during the atomic layer deposition (ALD) process of Hf-based high-k dielectrics have been tried recently to enhance the quality of dielectrics and to downscale the EOT. Zr incorporation in HfO2 along with intermediate treatment like plasma exposure or plasma oxidation seems to be promising. The time dependent dielectric breakdown (TDDDB) characteristics suggest that the time to breakdown of Hf1-xZrO2 film on silicon increases with increasing Zr percentage when the dielectric is exposed to alternate inert plasma during cyclic ALD deposition. On the other hand, when Ge devices (p-Ge/Al2O3/ZrO2/TiN) were subjected to TDDDB, a rapid degradation of TDDDB characteristics was observed when a low-k GeO2 interfacial layer was formed during processing. Unlike SiO2, GeO2 seems to degrade easily. But when a comparatively thinner GeO2 interfacial layer is formed because of process control, better TDDDB characteristics were observed (Fig. 6).52,53 More reliability work is, therefore, necessary for high-k on Ge and other III-V and 2D materials to integrate these materials into mainstream commercial technologies.

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Fig. 4. P-E characteristics in Al-doped HfO2. A clear ferroelectric property is shown in 4.8 mol% Al-doped HfO2.46 (Reprinted from T. S. Böscke, et al., Appl. Phys. Lett. 99, 102903 (2011), with the permission of AIP Publishing.)
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About the Authors

HIROSHI IWAI is the professor emeritus at the Tokyo Institute of Technology, and vice dean and distinguished chair professor of National Chiao Tung University in Taiwan. After receiving BE and PhD degrees from the University of Tokyo, he worked at Toshiba Corporation for 26 years and then Tokyo Institute of Technology for 18 years. Iwai is highly recognized for his significant contributions for the development of dielectric films. Those contributions include the introduction of BPSG film reflow to integrated circuits, finding plasma induced damage on gate insulator, prevention of boron penetration of gate oxide by RTN gate SiO₂, and the introduction of 1.5 nm tunneling gate oxide to CMOS. Additionally, Iwai is the chair of the ECS Japan Section. He is the winner of Thomas Callinan Award from the Dielectric Science and Technology Division of ECS and has served as an organizer of many ECS symposia and has been a member of various Society committees. Iwai co-authored over 1,000 international and 500 domestic papers in journals and conferences. He may be reached at iwai.h.aa@m.titech.ac.jp.

Akiro Toriumi is a professor of Materials Engineering at The University of Tokyo, Japan. He received the B.S. degree in physics, the M.S. and Ph.D. degrees in applied physics from The University of Tokyo. He joined Research and Development Center of Toshiba Corporation and then he moved to The University of Tokyo. His current research interests include materials science and device physics of high-k dielectrics for both silicon and germanium FETs, and materials science and applications of functional oxides. He has authored more than 400 refereed journal/conference publications, and a couple of book chapters. He is a fellow of the Japan Society of Applied Physics and a fellow of the Institute of Electrical and Electronics Engineers. He may be reached at toriumi@material.t.u-tokyo.ac.jp.

Durga Misra is a professor in the Helen and John C. Hartmann Department of Electrical and Computer Engineering, New Jersey Institute of Technology, Newark, USA. His current research interests are in the areas of nanoelectronic/ optoelectronic devices and circuits; especially in the area of nanometer CMOS gate stacks and device reliability. He is a fellow of The Electrochemical Society. He received the Thomas Callinan Award from the Dielectric Science and Technology Division of ECS. He is also the winner of the Electronic and Photonic Division Award from ECS. He edited and co-edited more than 45 books and conference proceedings in his field of research. He has published more than 250 technical articles in peer reviewed journals and in international conference proceedings. He received the MS and PhD degrees in electrical engineering from the University of Waterloo, Waterloo, ON, Canada. He may be reached at dmisra@njit.edu. https://orcid.org/0000-0001-6844-6058

Summary

High-k gate dielectrics has become part of the mainstream CMOS technology, including advanced FinFET devices. We have discussed the historical evolution of this high-k gate dielectric through scientific and technological challenges over many decades until it was introduced into 45 nm CMOS technology in 2007 by replacing SiO₂. Interface and dipole issues were somewhat resolved through scientific understanding and technological innovation. Thanks to the step coverage advantage of atomic layer deposition process, high-k was easily migrated to FinFET technology. Reliability of devices with high-k was a significant problem in the beginning but over time it has been improved significantly. Use of high-k on new semiconductor substrates such as III-V, Ge and 2D materials is currently being investigated but faces many challenges. Recent discovery of ferroelectric properties of HfO₂ makes it viable for more potential applications.

Fig. 6. Statistical (Weibull) distribution of TDDB breakdown characteristics of a p-Ge/Al₂O₃/ZrO₂/TiN gate stack.

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