Decoding the Golden Code: a VLSI design

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Abstract

Multiple-input multiple-output (MIMO) systems are among the most promising transmission techniques to achieve high data rate and high reliability transmission over wireless channels. The recently proposed Golden code is an optimal space-time block code for $2 \times 2$ MIMO systems. The aim of this work is the design of a VLSI decoder for a MIMO system coded with the Golden code. The architecture is based on a rearrangement of the sphere decoding algorithm that achieves maximum-likelihood (ML) decoding performance. Compared to other approaches, the proposed solution exhibits an inherent flexibility in terms of QAM modulation size and this makes our architecture particularly suitable for adaptive modulation schemes. Relying on the flexibility of this approach two different architectures are proposed: a parametric one able to achieve high decoding throughputs ($>165$ Mbps) while keeping low overall decoder complexity (45 KGates), with respect to other proposed solutions; a flexible implementation able to dynamically adapt to the modulation scheme (4-,16-,64-QAM) retaining the low complexity and high throughput features. In addition, a deep analysis of finite precision effects on the performance is presented in this work for both 16 and 64 QAM.

Index Terms

VLSI, digital architectures, Golden code, MIMO, sphere decoding

I. INTRODUCTION

The hardware implementation of high data rate and high reliability wireless communication systems is one of the most widely investigated topics within the scientific community and has raised new engineering and research challenges for many years. Higher transmission reliability demands for higher levels of processing complexity in the mobile terminal, while faster data rates require increased throughput: both evolutive trends are strong driving forces for the search of novel efficient architectures implementing the most critical base-band processing functions. In particular new standards proposed to regulate Wireless Local Area Networks (WLAN) and
Metropolitan Area Networks (MAN) are significant examples of very challenging applications from the implementation point of view.

There are two main objectives on which research is actually focused. The first goal is to make wireless communication data rate comparable to that of wired communications: recent results show it is possible to approach 1Gb/s data rate [19], [27]. The second one is to improve reliability, by combating multipath, noise and interference effects. The recourse to multiple-input multiple-output (MIMO) systems seems to be one of the most promising solutions to reach both these results.

Traditionally, MIMO systems were conceived with the purpose of dealing with one of these two objectives, by means of transmit antenna diversity combined with space-time coding. More recently great efforts have been made in unifying both goals and some new space-time codes are now able to reach the best tradeoff between data rate and diversity gain, although they require more sophisticated detection schemes at the receiver [1], [4], [6], [15], [21], [26].

The main contribution of this work is in the hardware design of a decoder for this kind of codes, in particular for the decoding of a $2 \times 2$ MIMO signal coded with the *Golden code* [1]. Golden code is a recently proposed full-rate and full-diversity space-time block code, chosen for its good energy efficiency. The maximum-likelihood (ML) decoding algorithm for the Golden code is based on the *Sphere Decoder*, which has already been widely addressed in the literature also from a hardware implementation point of view [16]- [28].

Several architectures have been proposed for the efficient implementation of the sphere decoding architecture, but they are optimized for specific modulation schemes and do not support reconfigurability features. In [2, ASIC-I], in order to reach high throughput dedicated multipliers and parallel computations are used adopting a so called “one node per cycle” architecture. Other architectures instead take advantage of suboptimal algorithms: good examples of this approach are given in [2, ASIC-II], where the $L_{\infty}$-norm is implemented as an alternative to the more expensive $L_2$-norm, and in [11], where the K-Best algorithm allows for performance-complexity trade-offs. These choices lead to fully optimized architectures, achieving high throughput; however, they are not ML (the loss is about 1.4 dB in the case of [2, ASIC-II]) and have been proposed for specific modulation and transmission schemes, although in [2] the possibility to adapt the proposed solution to different modulations is also mentioned. In this work we overcome these limitations, proposing two novel architectures designed with VHDL as a reusable intellectual
property (IP) macrocell: the first one is parametrized with respect to the fixed-point representation of data and to the addressed modulation scheme; in order to enable comparisons with previous implementations, synthesis results are provided for this architecture in the case of 16 QAM. The second architecture is flexible, meaning that it can be dynamically configured to cover multiple modulation schemes. We note that both these hardware implementations can be equivalently used in a $4 \times 4$ uncoded MIMO system [27].

In Section II we briefly explain properties, construction and detection of Golden code, Section III is dedicated to reviewing the sphere decoding algorithm. In section IV the effects of fixed-point precision on the code performance are derived. A short introduction to the overall scheme of the MIMO receiver is given in Section V with particular attention to QR decomposition preprocessing unit; the detailed descriptions of the two hardware implementations are then carried out in VI and VII. In the last two sections results and conclusions are presented.

II. GOLDEN CODE

The Golden code is a space-time (ST) code for a $2 \times 2$ coherent MIMO channel, it was found independently by [1], [6], [26].

Number theoretical methods have been widely employed to construct full-rate and full-diversity codes for coherent MIMO systems. These methods are based on the rank and the determinant criteria. In a Rayleigh fading channel the pairwise error probability (PWEP) expression [22] shows that the error probability can be minimized operating mainly on two aspects: diversity and coding gain. In [22] it was proved that these parameters are related to the so called codeword difference matrix $D$, which is constructed as the difference between two codewords. In order to maximize the diversity gain, the space-time code must be designed so that the difference matrix between any two codewords is full rank (rank criterion). On the other hand, the coding gain, depends on the determinant of $DD^\dagger$ and high coding gain is achieved maximizing the minimum of this determinant over all codeword pairs (determinant criterion).

Golden code satisfies both the rank and the determinant criterion and in particular, differently from previously known codes, presents the non-vanishing determinant property, i.e., its minimum determinant is $1/5$ and does not depend on the size of the signal constellation. For this reason it can be successfully employed in systems with adaptive selection of the modulation.

Besides these properties, the Golden code has also the peculiarity to be energy efficient. It is
constructed using a rotated version of the $\mathbb{Z}[i]^{4}$ complex lattice, so that there is no loss due to shaping [1].

The codewords $X$ of the Golden code are $2 \times 2$ complex matrices of the following form

$$
X = \frac{1}{\sqrt{5}} \begin{bmatrix}
\alpha [a + b\theta] & \alpha [c + d\theta] \\
\sigma(\alpha)[c + d\sigma(\theta)] & \sigma(\alpha)[a + b\sigma(\theta)]
\end{bmatrix}
$$

(1)

where $a, b, c, d$ are the information symbols chosen in a $Q^2$-QAM=$(Q$-PAM)^2 constellation, $i = \sqrt{-1}$, $\theta = (1 + \sqrt{5})/2 = 1.618 \ldots$ (Golden number), $\sigma(\theta) = (1 - \sqrt{5})/2 = 1 - \theta$, $\alpha = 1 + i - i\theta = 1 + i\sigma(\theta)$, $\sigma(\alpha) = 1 + i - i\sigma(\theta) = 1 + i\theta$, [25].

A. The $2 \times 2$ MIMO System Model

In order to model the $2 \times 2$ MIMO channel, its impulse response can be used. Assuming $h_{ij}$ as the time-varying channel fading coefficients between the $j$-th transmit antenna and the $i$-th receive antenna, the MIMO channel is described through a $2 \times 2$ matrix:

$$
\mathbf{H} = \begin{bmatrix}
h_{11} & h_{12} \\
h_{21} & h_{22}
\end{bmatrix}
$$

(2)

where $h_{ij} \sim \mathcal{N}(0, 1)$. Assuming the “Block Fading” channel model, each transmitted codeword will be affected by an independently varying channel matrix $\mathbf{H}$. Then, the $2 \times 2$ received matrix is

$$
\mathbf{Y} = \mathbf{H} \mathbf{X} + \mathbf{Z}
$$

where $\mathbf{Z}$ is the additive white gaussian noise matrix with entries $\sim \mathcal{N}(0, N_0)$.

We note that each codeword is sent in two channel uses of the two transmit antennas, for a total of four component signals. It is convenient to represent the codeword $\mathbf{X}$ in vectorized form where, furthermore, real and imaginary components are separated, resulting in a $8 \times 1$ real vector $\mathbf{x}$. The channel matrix $\mathbf{H}$ can be consequently rearranged in a $8 \times 8$ real-valued matrix $\mathbf{H}$. It can be seen that $\mathbf{x} = \mathbf{G}s$, where $\mathbf{G}$ is a $8 \times 8$ orthogonal matrix ($\mathbf{G}^{-1} = \mathbf{G}^T$) and $s = (\mathbb{R}a, \mathbb{I}a, \mathbb{R}b, \mathbb{I}b, \mathbb{R}c, \mathbb{I}c, \mathbb{R}d, \mathbb{I}d)$ with entries from a $Q$-PAM constellation, [25].

The vectorized system model can so be expressed as:

$$
\mathbf{y} = \mathbf{H} \mathbf{x} + \mathbf{z} = \mathbf{H} \mathbf{G} \mathbf{s} + \mathbf{z}
$$

(3)
where \( \mathbf{y} \) is the \( 8 \times 1 \) received real vector and \( \mathbf{z} \) is a 8-dimensional i.i.d. (independent and identically distributed) zero mean gaussian noise real vector.

**B. Decoding the Golden code**

Decoding the Golden code is equivalent to decoding an 8-dimensional lattice with generator matrix \( \mathbf{M} = \mathbf{HG} \). Provided that \( \mathbf{H} \) is perfectly known at the receiver, the optimal detector for a MIMO channel, which minimizes the codeword error rate, is the maximum-likelihood (ML) detector. It solves the following equation:

\[
\hat{s} = \arg \min_{\mathbf{s} \in \mathcal{Q}^n} \| \mathbf{y} - \mathbf{M} \mathbf{s} \|^2
\]

where \( \mathcal{Q}^n \) is the cardinality of the search space and \( n = 8 \).

The above expression represents a discrete least-square (LS) minimization problem. Exhaustive search of the ML solution has exponential complexity and in this particular case it has \( 2^n \log_2 \mathcal{Q} \) possible solutions. Sphere decoding algorithms have then been proposed in order to decrease the decoder complexity.

**III. Sphere Decoding Algorithm**

*Sphere decoding algorithms* denote a family of algorithms, which aim at lowering the complexity of the minimization (4) by analyzing only a subset of the solution space [5]. These algorithms, in a certain range of parameters which is not too far from those of real systems, show a polynomial average complexity. Although other work [16] denies this theoretical proof, computer simulations still confirm the practical result. This behavior is due to the fact that \( \mathbf{y} \) is not an arbitrary vector, but it is given by the transmitted vector \( \mathbf{Hx} \) with a small offset due to additive noise \( \mathbf{z} \).

Sphere decoding algorithms look at the set of possible solutions as points of a lattice and try to find the closest point to the received vector. In particular, a hypersphere is constructed around the received vector and only points inside it are taken into account, since the others are actually too far. This constraint can be written as:

\[
\| \mathbf{y} - \mathbf{M} \mathbf{s} \|^2 \leq C_0
\]

where \( C_0 \) is the square radius of the hypersphere [9], [23], [24]. In the following we describe a method to easily compute distances between received signals and lattice points.
1) Tree construction: With a linear transformation of the matrix $M$, such as QR or Cholesky decomposition, it is possible to rewrite $M$ as a product of two matrices, one of which upper triangular [5]. In this work, QR decomposition has been employed so that, given $M = QR$, (4) can be rewritten as:

$$\arg \min_{s \in Q^n} \| y - QRs \|^2 = \arg \min_{s \in Q^n} \| Q^Ty - Rs \|^2$$

$$= \arg \min_{s \in Q^n} \| \tilde{y} - Rs \|^2$$

(6)

where we have exploited the orthogonality of $Q$ and $\tilde{y} = Q^Ty$ represents the zero-forcing (ZF) solution. The upper triangular structure of the factored matrix enables to take every component separately into account for the computation of the distance between the two points. The distance $d^2(s) = \| \tilde{y} - Rs \|^2$ can also be computed recursively as follows. Let us define the partial metric as in [2]

$$T(l)(s(l)) = \begin{cases} 
0 & \text{if } l = n + 1 \\
T(l+1)(s(l+1)) + |\tilde{y}_l - \sum_{j=l}^{n} R_{lj}s_j|^2 & \text{if } l = 1, \ldots, n \end{cases}$$

(7)

where $s(l) = [s_l \ s_{l+1} \ldots \ s_n]$, and

$$\psi_{l}^{(l+1)} = \tilde{y}_l - \sum_{j=l+1}^{n} R_{lj}s_j$$

(8)

with $\psi_{n}^{(n+1)} = \tilde{y}_n$. Then we can write $T(1)(s) = d^2(s)$.

One of the most interesting consequences of this interpretation is that the exploration of the lattice can be thought as a tree traversal. This tree has $n$ levels and every node at each level has $Q$ sons. At every level the radius constraint (5) must be verified and satisfied, otherwise the branch is pruned. Figure 1 depicts a two level tree for a QPSK modulation. $T(l)$ is the partial distance metric at level $l$ in (7); at the lowest level, final metrics are explicitly calculated for this simple case.

2) Tree exploration: Several algorithms have been studied in order to make the tree traversal efficient. First algorithm, proposed by Pohst in [9], needs to chose explicitly an initial radius. This is a very critical choice: if the radius is chosen too large, too many points fall into the
Fig. 1. Two level tree for QPSK modulation, where $a_1 = |\tilde{y}_2 + R_{22}|^2$, $a_2 = |\tilde{y}_2 - R_{22}|^2$, $b_1 = |\tilde{y}_1 + R_{12} + R_{11}|^2$, $b_2 = |\tilde{y}_1 + R_{12} - R_{11}|^2$, $b_3 = |\tilde{y}_1 - R_{12} + R_{11}|^2$, $b_4 = |\tilde{y}_1 - R_{12} - R_{11}|^2$.

hypersphere, while for a too small radius no points are left inside it. A more efficient algorithm has been proposed by Schnorr and Euchner (SE) [20]. The SE algorithm has intrinsically variable throughput and this makes it not very suitable for hardware implementation. The key to make this algorithm efficient or, at least, with predictable throughput, is to make an effective pruning. A lot of theoretical studies can be found in recent literature, which aim at finding techniques to reach this goal [28]. Although some of them give very interesting ideas, none of them seems to be effective nowadays, with a strong theoretical demonstration and a simple realization.

IV. FIXED-POINT ANALYSIS

The study of finite precision effects is a mandatory preliminary step in the design and hardware implementation of complex processing tasks. Although several implementations of the sphere decoding algorithm have been proposed, studies on finite precision effects are not available in literature. In this work, a wide range of simulations have been carried out in order to determine the effects of different fixed-point representations on the performance for both 16 and 64-QAM modulation schemes.

The main conclusion that can be derived from results reported in Figure 2 is that the required number of bits increases when higher-order modulations are used. There are two reasons for
this increase:

- with higher order modulations, Euclidean distances between constellation points decrease and a larger number of bits must be allocated in the fractional part to discriminate distances;
- signal amplitudes are higher in higher order modulations, thus more bits need to be allocated also in the integer part.

Simulation results show that a total of 12 bits lead to performance very close to the floating-point case for 16-QAM modulation, while 14 bits are necessary in the detection of 64-QAM signals.

![Graph showing BER vs SNR for different bit allocations for 16QAM and 64QAM modulations.]

Fig. 2. System bit error rate (BER) using 16 and 64-QAM: lowering the total number of bits.

Finally, Figures 3 shows that the fixed-point approximation does not affect significantly the number of visited nodes of the algorithm. The plot is given as a function of the codeword error rate.
V. PREPROCESSING

In this section we discuss the implementation issues related to pre-processing, which is required before the tree-search. This computation operates on the lattice generator matrix $M = HG$; since the code generator matrix is constant, the computation must be repeated at the channel estimation update frequency.

The update frequency for the channel estimation can change significantly according to the scenario, but it is generally one or two orders of magnitude lower than the signalling rate. Figure 4 depicts a block diagram of a MIMO system adopting the Golden code; dashed blocks implement modulation and demodulation functions in a generic MIMO-OFDM system. The Golden code decoding phase is made of three functions: QR decomposition, column reordering and tree search.
While column reordering is an optional operation able to reduce the tree-search complexity, QR decomposition is mandatory because it allows constructing the tree and finding the ZF solution, possible techniques to perform the QR decomposition in hardware are reviewed in order to estimate the overall complexity of the receiver.

A. QR decomposition

As already outlined, a linear transformation of the channel matrix $H$, such as QR or Cholesky decomposition is needed in order to construct the tree.

QR decomposition is a well studied numerical algorithm and widely used in many applications such as matrix inversion, adaptive beamforming and filtering. The QR decomposition based - Recursive Least Squares (QRD-RLS) methods are routinely adopted in applications such as multiuser detection in CDMA communications, adaptive equalization of radio channels etc. The method is well suited to VLSI realization and it can be implemented in a stable manner using relatively short word length arithmetic.

Hardware realization of this technique implies the choice between Householder transformation and Givens rotation based algorithms [10]. This second approach can be accomplished by a sequence of rotation operations to annihilate elements under the main diagonal of the matrix. Givens rotations require a larger number of flops compared to Householder method in order to compute QR decomposition, nevertheless they may be implemented using highly parallel systolic arrays and for this reason they are usually preferred for hardware implementation.

These arrays typically present linear, triangular, or square structure; the rotation angle is computed in boundary or diagonal processors and dispatched to other processors for rotation. The choice of the organization can be made on the basis of area and throughput considerations.
### TABLE I

**QR Decomposition: Different Array Organization Parameters - Number of Processing Elements (PE), Latency and Throughput**

| Architecture       | # of PEs                  | Latency of Single QR | Throughput             |
|--------------------|---------------------------|-----------------------|------------------------|
| Triangular         | $n(n+1)/2$                | $n(n+1)/2$            | $1/n$                  |
| Linear             | $n$                       | $2n^2 - n$            | $1/(2n^2 - n)$         |
| (2n - 1) + $(\frac{n}{2} - 1)(n + 1)$ | $\div$                      | $\div$                      | $1/[(2n - 1) + (\frac{n}{2} - 1)(n + 1)]$ |
| Single Element     | 1                         | $n^2(n+1)/2$          | $1/[n^2(n+1)/2]$       |

The main parameters of this architecture are listed in Table I for a $n \times n$ matrix: number of processing elements (PE), latency and throughput. It is assumed that every processing element takes one or more clock cycles to perform its computation.

Every single processing element must perform the angle calculation and the rotation to annihilate the matrix elements. Several alternatives exist to accomplish these two tasks, and the two main ones are:

1) *Sine* and *cosine* of the angle are computed by means of operations including also square root and division.

2) Direct calculation of the angle and then rotation using a CORDIC processor [12].

The main advantage of the first approach is that primitives can be optimized resulting in an efficient although expensive implementation. The second technique is less expensive, but outputs are generated with longer latencies and data-dependency between operations slows down the CORDIC algorithm. Many strategies have been adopted in order to alleviate the effects of data-dependencies, such as reordering look-ahead [3], [14], [17] or redundant arithmetic [8].

For lower data-rates, architectures that reuse the processing elements on different data have been proposed in [7], [13]. These architectures represent probably the best tradeoff for the applications addressed in this work.

### VI. First Hardware Implementation:
PARAMETRIZABLE SOLUTION

The tree-search algorithm is considered as the most computationally intensive processing block in a MIMO detector, although column reordering and QR decomposition can also be heavy processing tasks. However, since the rate of updating for channel estimation is usually one or two orders of magnitude lower than the signalling rate, design constraints tend to be more stringent for the tree-search unit than for column reordering and the QR decomposition. Thus the focus of this work is on the hardware realization of the tree-search algorithm.

As guidelines for the design of the architecture, two main objectives have been taken into account. The first requirement was a certain degree of flexibility in the choice of both modulation scheme. The second main design objective was a high decoding throughput, compliant with needs of modern wireless communication standards.

In the developed architecture, the datapath width, the size of the search tree and the modulation scheme are tunable parameters that can be statically configured to make the detector adaptable to different systems. Although the system is described with reference to the special case of the Golden code, it can be also used to decode a $4 \times 4$ uncoded MIMO scheme. The key elements of the developed architecture are described in the following paragraphs.

A. A flexible hardware solution

The key processing task in the tree exploration algorithm is given by (7), where we recall that $\psi_{l+1}^l = \tilde{y}_l - \sum_{j=l+1}^n R_{lj} s_j$, is the $l$-th entry of an $n$ elements vector $\psi^{l+1}$, where $l + 1$ is the tree level we are referring to. At level $l$, the generic $i$-th entry of this vector can be decomposed in a recursive manner through the following expression

$$
\psi_i^{(l)} = \begin{cases} 
\tilde{y}_i & \text{if } l = n + 1 \\
\psi_i^{(l+1)} - R_{il} s_l & \text{if } l = n, \ldots, 1
\end{cases}
$$

(9)

where $i$ is in the range $1, \ldots, n$ while the level $l$ decreases from $n + 1$ to 1.

The whole $\psi^{(l)}$ can therefore be updated by means of

$$
\psi^{(l)} = \psi^{(l+1)} - R_{ls_l} \quad l = n, \ldots, 1
$$

(10)

where $R_{s_l}$ is the $l$-th column of $R$ and the initial value is given by $\psi^{(n+1)} = \tilde{y}$.
In order to minimize the final metric $d^2(s)$ with a greedy algorithm, at each level of the tree the minimum $\psi^{(l+1)}_l - R_{ll}s_l$ value between all sons must be selected. More precisely, at each tree node, placed at level $l$, three main operations have to be accomplished:

1) the $s_l$ that minimizes the difference $|\psi^{(l+1)}_l - R_{ll}s_l|$ is selected
2) the partial metric $T^l(s^{(l)})$ is calculated according to (7).
3) for each $i = 1, \ldots, n$, $\psi^{(l)}_i$ is evaluated for the selected $s_l$ value, according to (9).

Thus the straightforward minimization of partial metrics $T^l(s^{(l)})$ requires the difference computation for all the possible values of $s_l$. This technique becomes increasingly expensive with high order modulations, due to the large number of required operations.

In the proposed architecture, the minimization of $T^l(s^{(l)})$ is rearranged in two steps. In the first processing step, the value of $s_l$ that minimizes the difference $|\psi^{(l+1)}_l - R_{ll}s_l|$ is directly selected by means of a division; the obtained $s_l$ is then used to generate $\psi^{(l)}_i$ amounts in (9), for all $i = 1, \ldots, n$. At the second step, (7) is finally evaluated to obtain the actual metric value $T^{(l)}$ for the selected son. Two functional blocks, $U_{\text{psi}}$ and $\text{Metric\_compute}$ units, are allocated to perform the indicated processing steps.

In order to find the value of $s_l$ able to minimize $|\psi^{(l+1)}_l - R_{ll}s_l|$, $U_{\text{psi}}$ unit (shown in Figure 5) receives as inputs the $\psi^{(l+1)}_l$ derived at the upper tree level, together with the $l$-th diagonal element of matrix $R$. The result of the division $\psi^{(l+1)}_l / R_{ll}$ is approximated to the closest odd integer. This approximation is equivalent to the selection of the closest point in a $Q$-PAM constellation.

The resulting value directly provides the desired $s_l$ for the analyzed node. The new $\psi^{(l)}_i$ values are then evaluated in parallel, to be used at the lower tree level.

Vector $\psi^{(l)}$ is stored in a dedicated memory, which will be later referred to as $\text{Psi memory}$ in the global architecture given in Figure 10.

The $\Delta$ output in Figure 5 is defined as

$$\Delta = s_l - \frac{\psi^{(l+1)}_l}{R_{ll}}$$

and it represents the correction term to be applied to the division result in order to take the closest point in the equivalent PAM constellation. The use of $\Delta$ will be described later in this Section.
The Metric compute unit realizes the second processing step, evaluating the new metric $T^{(l)}$ for the selected son. Figure 6 shows the block architecture: from the upper tree level, $T^{(l+1)}$ is received as input, together with the $\psi^{(l)}$ value generated by U_psi unit; the obtained $T^{(l)}$ is propagated to the lower tree level.

The described approach, and particularly the use of a division to obtain the optimal $s_l$, allows avoiding multiple metric computations; thus it offers low complexity and, at the same time, flexibility in terms of supported modulation schemes. As a matter of fact, a parallel architecture tailored on a given search tree is able to achieve high processing speed, while the sequential computation of a single metric at each cycle makes it easier for the decoder to adapt to different structures of the search tree, so providing support to multiple modulation schemes. Similarly to what is done in a software implementation, sequential operations compute a single metric at every cycle, so that the same processing platform can easily adapt to different structures of the search tree by simply varying the number of search steps in the tree.

On the other hand, differently from what was implemented in previous detectors, multiplications cannot be reduced to add and shift procedures since operands are not fixed and as a consequence general purpose multipliers have been allocated.
It is worth noting that, although the described technique introduces the division $\psi_l^{(l+1)}/R_{ll}$, only a few values of this ratio are of interest for the algorithm, those that correspond to the equivalent PAM constellation points $\pm 1, \pm 3, \ldots$. As a consequence, a general purpose hardware divisor is not necessary and the required operation can be executed by means of a simplified component able only to find the closest integer solution of this division and to determine if the approximation is by defect or by excess: the first $\log_2 Q$ steps of a successive subtraction divider [18] can be employed to this purpose, where $Q^2$ is the number of signals in the QAM constellation. This divider has a very simple architecture that employs only shifts and subtractions; although it tends to be very slow for a complete division, this solution can be effectively used when only a few shift and add steps are required. The divider employs a dichotomous process to find the requested value after $\log_2 Q$ steps. In the block diagram of Figure 7, the multiplexer selects the dividend at the first step and the subtraction result in the following ones; the $n$-bit variable shifter is used to shift the divider by a number of positions that changes from the initial value of $\log_2 Q - 1$ down to 0. The subtractor returns the result one bit per iteration, starting from the most significant one.
**B. Parallelism and pipelining**

The desired functional flexibility cannot be achieved at the expenses of processing throughput, but the final architecture must properly conjugate both features of flexibility and high data rates. Among effective techniques that can be used to increase throughput, parallelism and pipelining have been considered. In previous works, high throughput is obtained resorting to parallel architectures and two different kinds of parallelism are usually employed:

- Parallelism at the level of tree exploration
- Parallelism at the level of the metric computation for all sons of a given node and in the selection of the most probable son.

The first technique can be used only with some suboptimal algorithms [28] and it becomes unfeasible when optimal algorithms are adopted, since it requires large amounts of hardware resources. The second approach is feasible only with low order QAM modulation schemes as it implies many concurrent multiplications. Thus these techniques are not viable for the implementation of parametric architectures. As a consequence, in this work, the pipelining technique has been investigated.

In order to ensure that a new node is expanded at each clock cycle, a new, alternative metric must be available also after a pruning operation has taken place. As a consequence, when the metrics of a given father node are evaluated, two “candidate” nodes are concurrently computed: the first one is a direct son of the current node and it is processed by the \( U_{\psi} \) unit, while the alternative node, placed at a higher level in the tree, is concurrently computed by the \( U_{\psi,\text{step}} \) unit.
sub-circuit (see Figure 8). Both of them generate novel $\psi^{(l)}$ values for the next step in the tree traversal.

$U_{\psi}$ and $U_{\psi, \text{step}}$ units share a very similar architecture, however the latter does not need to perform the division, as the second best choice for $s_l$ (and thus for the alternative node) can be easily derived as follows. When $U_{\psi}$ unit computes the division, the result is approximated either by defect or by excess to the nearest PAM constellation point: the best choice for $s_l$ is given by (see Figure 9)

$$s_{l(1)} = \frac{\psi_l^{(l+1)}}{R_{ll}} + \Delta$$

where $\Delta$ is the correction term provided as output by the $U_{\psi}$ unit (Figure 5).

The sign of $\Delta$ is used by $U_{\psi, \text{step}}$ unit to take the second (and following) nearest point in the PAM constellation, according to the following rule, implemented in the top block of Figure 8

$$s_{l(k)} = s_{l(k-1)} - (-1)^k \text{sign}(\Delta) \cdot (k-1) \cdot A$$

where $A$ is the distance between two consecutive points and the initial value, $s_{l(1)}$, is the closest point given in equation (11).

Figure 9 shows the sequence of alternative nodes selected at a given tree level, after the occurrence of pruning. Depending on the values assumed by the father node metric, the algorithm
descends along the tree, reaching the son node, or it moves to the alternative node on the same level. It is worth noting that the computations of the $\psi^{(l)}$ values for both son and alternative nodes are performed concurrently with the elaboration of the $T_l$ metric for the father node. In other words, while the current metric is computed for the father node, the next node to be visited is identified choosing between the son and the alternative node. Additionally, the related $\psi^{(l)}_l$ value is computed to be used at the following step in order to obtain the proper metric $T_{l-1}$.

This approach also provides a significant speed-up to the inherently serial SE Sphere Decoding algorithm and has a limited impact on complexity.

C. Global architecture

The block scheme of the SE tree-traversal circuit showing the architecture derived from the design criteria outlined in previous paragraphs is depicted in Figure 10. Four fundamental processing blocks can be identified in this architecture:

- **U.psi unit**, which selects the most probable son of the current node and computes updated $\psi^{(l)}$ through expression (10) (see also Figure 5);
- **U.psi.step unit**, which selects the alternative node to be expanded and computes for this node the same amount;
- **Metric.compute unit**, which computes metric of the current node $T^{(l)} = T^{(l+1)}(s^{(l+1)}) + |\psi^{(l+1)}_l - R_l s_l|^2$, as in equation (7);
- **C.U., control unit** devoted to the proper selection of the tree search direction.

The C.U. constitutes the core of the tree traversal algorithm and it must also carry-out two further tasks: to verify the pruning condition and, on the basis of this verification, to properly
dispatch data between the other units. Symbols given in Figure 10 are related to the case of a node expanded in the depth-first mode, with no pruning: as a consequence, inputs of the \texttt{Metric compute} unit are fed with outputs provided by \texttt{U psi} block. When a pruning occurs, multiplexers are switched and metrics related to the alternative node are selected.

Finally, \textbf{Psi Memory} stores $\psi^{(l)}$ vectors from one step to the following one.

Fig. 10. \textit{Sphere decoder} block scheme (case of a node expanded in the depth-first mode, with no pruning).

\section*{VII. \textsc{Second Hardware Implementation: Flexible Modulation Solution}}

The capability of managing more than one modulation scheme in order to adaptively select the most efficient one according to user needs and channel conditions, is one of the most important requirements of modern wireless communications systems. The Golden code, thanks to the non-vanishing determinant property, is very well suited for such application since it achieves the best performance independently of the QAM size. In order to take full advantage of this Golden
code feature, an enhanced implementation has been realized to allow run-time choice of the modulation scheme.

This implementation relies on the same architecture described in the previous section, with an additional parameter that allows the run-time selection of the constellation. The requirement of supporting multiple modulation schemes basically impacts on the control logic, while the other architecture components remain the same as in the first hardware implementation.

At each level of the tree, the C.U., besides the pruning condition verification, also carries out a second verification task, related to the mapping constraint: it verifies if a certain value of $s_l$ still belongs to the specified constellation and uses this information to drive the processing.

This mapping constraint must also be taken into account in the division $\psi^{(l+1)} / R_{ll}$. As the number of acceptable values for this operation depends on the adopted modulation, the constellation parameter is used to dynamically drive the iterations of the dichotomic division algorithm.

Although the architecture deals with the implementation of the Golden Code where $n = 8$, it is also scalable in terms of $n$. Increasing the number of transmitting and receiving antennas: a larger value of the $n$ parameter can be set in the VHDL code to synthesize detectors for larger STBcodes. Of course a larger $n$ implies a more expensive architecture: particularly the value of $n$ mainly affects:

- the number of $\psi$ values to be evaluated in parallel in Figures 6 and 9
- the depth of the tree
- the size of $\psi$ memory.

The complexity of processing blocks in Figures 5 and 8 grows almost linearly with $n$; the memory size increases as $n^2$, because $n$ values of $\psi^{(l)}$ have to be stored for $n$ tree levels. Finally the throughput is expected to decrease with $n$, since the number of visited nodes grows, but this effect is strongly dependent also on the supported code.

VIII. SYNTHESIS RESULTS

The first proposed architecture, tailored to process the 16-QAM case, has been synthesized on both 0.13$\mu$m and 0.25$\mu$m CMOS Standard Cell technologies, using the Synopsys Version
Z-2007.03-SP1; synthesis on 0.13µm technology has been performed for the second flexible architecture. A commercial low-power library has been chosen.

In order to enable the direct comparison with existing hardware realizations [2], I and II ASIC, [11], a 16 bit datapath has been chosen and the overall decoder has also been simulated with the uncoded 4×4 MIMO system and throughput figures reported in Table II refer to this configuration.

The comparison of the described architectures to existing implementations tends to be quite difficult to carry out, because different approaches have been adopted: particularly, our solution implements the ML detection algorithm by means of a serial architecture, while the first ASIC in [2] maps the same algorithm onto a parallel structure and the second ASIC in [2] makes use of a serial scheme to realize a close to ML algorithm. These differences must be carefully evaluated while reading results in Table II.

### TABLE II

**SYNTHESIS RESULTS AND COMPARISONS (16 BITS)**

|                     | Reference | ASIC-I [2] | ASIC-II [2] | [11] | PARAMETRIZABLE IMP. | FLEXIBLE IMPL. |
|---------------------|-----------|------------|-------------|------|--------------------|----------------|
| **Antennas**        |           | 4×4        | 2×2 per two channel uses |     |                    |                |
| **Modulation**      |           | 16-QAM     | 16-QAM      | 16-QAM | 4,16,64-QAM       |                |
| **Detector**        |           | depth-first | sphere      | K-best | depth-first        |                |
| **BER Perf.**       |           | ML         | Close to ML | Close to ML | ML                |                |
| **Tech. [µm]**      |           | 0.25       | 0.25        | 0.35  | 0.25               | 0.13           |
| **Core Area [GE]**  |           | 117K       | 50K         | 91K   | 56K                | 45K            |
|                     |           | +preproc.  | +preproc.   | +preproc. | +preproc.         | +preproc.      |
| **Max. Clock**      |           | 51 MHz     | 71 MHz      | 100 MHz | 109 MHz           | 250 MHz        |
|                     |           |            |            |        |                    | 217 MHz        |
| **Throughput**      |           | 73 Mbps    | 169 Mbps    | 52 Mbps | 73 Mbps           | 167 Mbps        |
|                     |           | @SNR=20 dB | @SNR=20 dB |        | @SNR=20 dB        | @SNR=20 dB     |
Comparing the parameterizable architecture to parallel implementations in Table II, the solution described in [11] and the first ASIC presented in [2], it can be observed that a single metric computation is performed at each cycle, instead of multiple parallel metric computations. This characteristic justifies both the reduced complexity and the inherent flexibility of the proposed architecture. At the same time, thanks to the adopted pipelined architecture, a remarkable average decoding throughput is achieved without any highly specialized structure.

Implementation cost is slightly higher than for the second ASIC proposed in [2], where a serial approach is also adopted, in conjunction with a close to ML algorithmic approach.

On the other hand, the flexible implementation in the last column of Table II prove the limited complexity and performance overhead associated to the capability of dynamically adapting to different modulations (4-, 16- and 64-QAM).

Finally, the results presented in Section IV on the finite precision analysis of the decoding algorithm have been exploited to derive additional post synthesis figures for the flexible architecture: these results, referred to different datapath widths, are given in Table III. A total of 14 bits are enough for the 64-QAM modulation (6 bits for the integer part and 8 for the fractional one) and the two saved bits grant a complexity reduction of 8 K gates.

IX. CONCLUSIONS

A novel approach has been presented for the hardware implementation of a Sphere Decoder detector: the proposed solution uses a single metric computation per cycle and is well suited for pipelining, breaking the sequential nature of SD algorithm.

The main element of novelty of the described approach is in its inherent flexibility that makes it suitable for the implementation of an adaptive modulation scheme. Two different hardware
architectures have been designed: the first implementation is a parametrizable one, while the second is able to adapt on the fly to different modulation schemes.

The data representation format adopted in both implementations is based on exhaustive analysis of finite precision effects collected for 16 and 64 QAM modulations.

Final synthesis results of the proposed architectures are listed in Table III and show a significant complexity reduction (approx. 50% for 16 QAM modulation) with respect to parallel structures. This is mainly due to the single metric computation per cycle. A remarkable average decoding throughput can be achieved with both implementations, thanks to the pipelining technique, even if the hardware was not tailored on a single modulation scheme as all previously proposed solutions.

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