VPIC 2.0: Next Generation Particle-in-Cell Simulations

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Abstract—VPIC is a general purpose Particle-in-Cell simulation code for modeling plasma phenomena such as magnetic reconnection, fusion, solar weather, and laser-plasma interaction in three dimensions using large numbers of particles. VPIC’s capacity in both fidelity and scale makes it particularly well-suited for plasma research on pre-exascale and exascale platforms. In this paper we demonstrate the unique challenges involved in preparing the VPIC code for operation at exascale, outlining important optimizations to make VPIC efficient on accelerators. Specifically, we show the work undertaken in adapting VPIC to exploit the portability-enabling framework Kokkos and highlight the enhancements to VPIC’s modeling capabilities to achieve performance at exascale. We assess the achieved performance-portability trade-off through a suite of studies on nine different varieties of modern pre-exascale hardware. Our performance-portability study includes weak-scaling runs on three of the top ten TOP500 supercomputers, as well as a comparison of low-level system performance of hardware from four different vendors.

Index Terms—Simulation, Portability, Plasma Physics, Particle-in-Cell

1 INTRODUCTION

Many plasma physics phenomena can only be understood through the use of kinetic Particle-in-Cell (PIC) simulations. VPIC \cite{1,2} has been at the forefront of this research to study plasma physics phenomena including magnetic reconnection, fusion, solar weather, and laser-plasma interaction. VPIC was deployed to perform high performance multi-trillion particle simulations on over 2 million MPI processes on the Trinity supercomputer and other computing clusters at Los Alamos National Laboratory \cite{3,4}.

The original VPIC code (referred to throughout as VPIC 1.0) was built to minimize data movement and maximize performance; given a new HPC platform, the ad-hoc reengineering of the code had guaranteed the continuation of performance. However, the increasing heterogeneity of emerging exascale platforms makes it no longer practical to optimize the VPIC code for every available compute platform. A new multi-architectural VPIC code is needed to ensure portability and performance across exascale platforms, but there are three challenges to building this code. First, the build system complexity grows significantly with the number of architectures supported. Second, the code must allow usage of native hardware focused APIs and libraries. Hardware vendors and library developers put significant effort into optimizing common operations and function calls. Not allowing access to existing optimized libraries creates more work for the developers and reduces performance. The third, and probably the most tangible and difficult, challenge is loss in performance. Portable code comes at the cost of performance due to differences in parallelism approaches among platforms. Writing portable code requires forcing a single parallelism model onto many platforms. The mismatch between model and platform leads to a loss in performance.

There are multiple methods to overcome these challenges and to create a multi-architectural VPIC code while reducing long-term maintenance. These include pragma-based directives such as OpenMP and template-based library approaches such as Kokkos \cite{5} and Raja \cite{6}. Template-based library methods are particularly powerful because they can reduce the amount of code needed to support multi-architectural codes. Furthermore, frameworks like Kokkos and Raja can make architectural code-branching decisions at compile time while minimizing the architecture-dependent code required by the application developers. In this paper, we address the three challenges listed above to transformed the original VPIC code (VPIC 1.0), a CPU-only, platform-specific optimized code, into VPIC 2.0; a multi-architectural, portable code, with the support of the Kokkos abstraction layer. The single VPIC source code runs across a diverse range of modern hardware.

Transforming VPIC into a high performance portable code capable of running on emerging heterogeneous platforms requires several changes. Using Kokkos effectively involves changes to both VPIC’s data structures and user interfaces. VPIC 2.0 alters data storage to leverage the benefits of Kokkos Views (advanced multidimensional arrays). Using Views for storage allows us to automatically adjust the memory layout to best match the target hardware. Extending the user interface is required to maintain backwards compatibility and improve the performance of simulation diagnostics. Other transformations that we introduce focus on further improving the portability and performance of VPIC 2.0 through code restructuring and optimizations.
VPIC 2.0 scalability and portability is tested across nine platforms including the Sierra, Frontera, and Selene supercomputers. We demonstrate excellent weak scaling, especially the GPU-based platforms where we see less than 10% slowdown between 64 and up to 7,200 GPUs. The rise in GPU cache size opens up intriguing possibilities for super-linear speedup at tangible scientific scales, as shown in our strong scaling results. Our portability study demonstrates the effectiveness of VPIC 2.0 across all nine platforms and highlights both the challenges and strengths of portable code. VPIC 2.0 is easy to adapt and run on emerging hardware platforms with limited manual work. The portability of VPIC 2.0 enables the use of cutting edge accelerators for greater performance and facilitates longer simulations, more advance diagnostics, and faster turn around time. The contributions of this paper are as follows:

- An effective approach for performance portability
- The performance and portability study on nine platforms
- The study of weak and strong scaling across CPU and GPU platforms (including 3 top 10 machines)
- The analysis of the costs and benefits to portable code
- Insights on the impacts of VPIC 2.0 on future scientific discovery

The rest of this paper is structure as follows: Sec 2 presents key changes in modern computing and provides a overview of Kokkos; Sec 3 introduces the physics behind VPIC; Sec 4 presents our transformation to the VPIC code needed to achieve portability; Sec 5 shows performance and scalability results; Sec 6 describes the impact of the newly release VPIC on scientific discovery at exascale; Sec 7 cites related work; and Sec 8 summarizes this work.

2 BACKGROUND

2.1 Modern Heterogeneous Computing

Supercomputing has a rich history of exploring and exploiting different aspects of parallelism. From the first vector supercomputers in the 1970s, to the massive clusters of computers of today, accelerators have been used to offload time-consuming tasks from the primary compute unit(s). This was first seen with specific-purpose co-processors [7], [8], and later evolved to include generic purpose accelerator hardware [9] and GPUs [10] as the cornerstone of accelerator based computing.

Accelerators today provide a highly parallelized compute capacity. We have seen a few major approaches in accelerators in the last 10 years. The first, the GPGPU which uses hundreds of graphics cores that often only compute at single or half precision. The second modern accelerator type contains many general purpose cores which are generally slower than the primary compute unit. Some examples of this type are the Intel Knights Corner [11] and Sunway SW26010 [12] accelerators. Finally, while a large amount of SIMD capability now sits on the package of most modern CPUs, a third group of accelerators exists that provides additional vector capability, such as the NEC Vector Engine [13].

These characteristics and the accompanying execution models of modern accelerators create many challenges for maintaining and improving performance, which is the primary motivation for using accelerators in high performance computing. Porting an existing code base to a new accelerator architecture while maintaining performance can have many facets including; novel memory models; explicit concerns around data locality and data movement; unfamiliar execution models; and changes in the scale of parallelism. Any of these issues can be core to maintaining performance through an architecture change. Further compounding this complexity is that once a code base is ported to a new platform and is performant, there may now be a new branch or code variant to maintain.

2.2 Kokkos Overview

Kokkos [5] is a suite of libraries and abstractions for developing high performance C++ applications that are portable across many architectures, including all major CPUs and accelerators. Kokkos achieves high performance and portability by mapping its own programming model to various native backend parallel programming languages such as CUDA or HIP.

There are three major elements of the Kokkos ecosystem: the Kokkos kernels libraries, the Kokkos tools interface and the Kokkos core programming model. The Kokkos kernels libraries provide common linear algebra (e.g., BLAS, SparseBLAS) and graph algorithms. Kokkos tools are comprised of an interface and a set of utilities that connect to the Kokkos runtime and enable lightweight debugging and profiling. The Kokkos programming model enables developers to control memory layout, placement of data, parallel execution, and execution devices. Kokkos maps specified data characteristics and execution policies to the target hardware backends using a set of rules for automatically determining different hardware specific parameters, removing the user from the mapping task.

The Kokkos programming model abstractions manage common data structures and parallel execution as seen in Fig. 1. Kokkos data structures have three key extensions defining the memory space, layout, and traits. The memory space determines where the memory is allocated. This abstraction enables the use of different memory technologies (e.g., High Bandwidth Memory or HBM, DDR SDRAM, and Non-Volatile Memory). Memory layout controls the order in which memory is allocated and stored, affecting the memory access pattern. Kokkos includes the most common layouts (e.g., row/column major, strided, and tiled). These layouts are important for maximizing performance and interoperability with various linear algebra libraries. Kokkos also supports various memory traits that affect how memory is accessed (e.g., streaming, atomic, restricted) and offer the users fine grained control to be used to expose additional information or optimization opportunities. Kokkos Views are the most common data structure used in VPIC. Views are reference counted, multi-dimensional arrays with optional memory traits to control memory access. These memory traits, combined with hardware settings determined at compile time, enable Kokkos applications to operate on significantly different hardware platforms with a single code path needed to be written by the developer. For example, GPU applications generally require memory to be setup on the
host and copied to the device. Kokkos addresses this pattern by having a HostMirror View that acts as the host copy of a device View. Developers can use a deep_copy operation to move data between Views, including between a host and a device. If the target device is the same as the host, in the case of a CPU only build, any unnecessary deep_copy will change into a noop.

Kokkos’s parallel executions are defined via execution spaces, patterns, and policies. An execution space defines where an operation is to be run (e.g., CPU or GPU and execution mechanisms). The pattern of execution (or where an operation is to be run (e.g., CPU or GPU and spaces, patterns, and policies. An execution space defines portability [14].

Fig. 1: Core Kokkos abstractions for ensuring performance portability [14].

The PIC method solves the electromagnetic fields on a grid and moves particles continuously through space. The particles move in response to the fields according to the Lorentz force law, and deposit current on the grid. They do not directly interact with each other, unless collisions are modeled. The fields evolve according to Maxwell’s equations, Eqs. (1) including the current from the particles.

The plasma distribution function is represented by quasiparticles, also called simulation particles or macroparticles. Quasiparticles are single particles of a particular species in the simulation that represent a number of real particles given by their weight, \( w \). The PIC method thus samples the smooth distribution function \( f_s \), which is the ensemble average of the “ground truth” microscopic \( F_s \). Typically, \( w \gg 1 \).

Furthermore, quasiparticles have a shape (i.e., a distribution of mass charge over some spatial extent). For a given particle shape, \( \phi \), the distribution function is represented in PIC as

\[
f_s(\vec{x}, \vec{v}, t) = \sum_{i=1}^{N_s} w_i \phi(\vec{x} - \vec{x}_i(t)) \delta(\vec{v} - \vec{v}_i(t)).
\]

Typically, the particle shape functions are B-splines:

\[
b_0(\xi) = \begin{cases} 
1 & \text{if } |\xi| < 1/2 \\
0 & \text{otherwise}
\end{cases}
\]

\[
b_{n+1} = \int_{-\infty}^{\infty} b_0(\xi - \xi')b_n(\xi - \xi') d\xi',
\]

where \( \xi \) is the distance to the quasiparticle center normalized to the grid spacing. Zeroth order is called top-hat shape, and first is triangle. The 3D shape function is typically the tensor product of the 1D shape functions in each dimension. The field experienced by a quasiparticle with a finite spatial extent is

\[
\vec{E}_i = \int \vec{E} \phi(\vec{x} - \vec{x}_i) d\vec{x},
\]

\[
\vec{B}_i = \int \vec{B} \phi(\vec{x} - \vec{x}_i) d\vec{x}.
\]

Since the fields are defined on the grid, evaluating these integrals requires an interpolation scheme [24, 25], the details of which can be messy.

All PIC codes at their core consist of two coupled solvers: the particle pusher and the field solver. The particle pusher moves plasma particles freely through space based on surrounding EM fields and calculates currents arising from this motion. The field solver solves Maxwell’s equations on a fixed grid, accounting for the currents from the particles.
These core algorithms fully reproduce the behavior of collisionless, relativistic, kinetic plasmas. Additional physics, such as collisions and special boundary conditions, can be added with additional physics modules.

Maxwell’s equations are solved using the widely used finite-difference time-domain (FDTD) method [26] on the Yee staggered grid [27]. The staggered Yee grid allows for easily implemented centered, second order accurate derivatives. The particle pusher solves the relativistic equations of motion

$$\frac{dx}{dt} = \vec{v},$$

and

$$\frac{d(\gamma \vec{v})}{dt} = \frac{q}{m}(\vec{E} + \vec{v} \times \vec{B}).$$

VPIC uses the Boris pusher [28], a second-order accurate pusher that employs the leapfrog method, slightly modified to avoid cyclotron motion aliasing, similar to the method used in [29]. The Boris pusher splits the equations of motion into an acceleration from the $\vec{E}$ field and a rotation about the $\vec{B}$ field. A particle is first pushed a half-step, based on its previous momentum. The fields are interpolated to this half-step position, the momentum is updated with these fields, and the particle is moved the full step. Finally, the particle is moved to the three-halves position to calculate the current used by the field solver, and the three-halves position is discarded.

More formally, the difference equations are

$$\frac{p^n + \frac{1}{2} - p^{n-\frac{1}{2}}}{\Delta t} = \vec{v}^n,$$

and

$$\frac{p^{n+1} - p^n}{\Delta t} = q(E^{n+\frac{1}{2}} + \vec{v}^{n+\frac{1}{2}} \times B^{n+\frac{1}{2}}),$$

where $\vec{v} = \vec{p}/(m\gamma)$, and

$$\vec{v}^{n+\frac{1}{2}} = \frac{p^n + p^{n+1}}{2m\gamma^n + \frac{1}{2}}.$$

4 VPIC FOR HETEROGENEOUS PLATFORMS

4.1 Data Structure and Interface Transformations

Two components of the VPIC code need to be redesigned in order to deploy the Kokkos abstraction layer effectively: (1) the VPIC data structure elements and (2) the user interface.

4.1.1 VPIC Data Structure Elements

VPIC operates by defining a simulation space divided into a grid of cells, and modeling particle movement across these cells. In other words, particles are distributed across an n-dimensional (n-D) space that is decomposed into a n-D grid. Each simulated particle is a macroparticle with a defined weight (i.e., the number of real particles modeled by each macroparticle). There are four key data elements in VPIC that must be moved to Kokkos Views to ensure portability. They are the macroparticles, electromagnetic (EM) fields, interpolators, and current accumulators. Fig. 2a describes the original C++ definition of macroparticle storage in VPIC 1.0 before the Kokkos port. Each macroparticle is a 32-byte structure (i.e., 3 floats for voxel position $dx$, $dy$, and $dz$, 1 float for weight, and 1 integer for cell index).

The EM fields are represented in the original C++ VPIC 1.0 code as a 80-byte structure (i.e., 3 floats for the $E$ field, 1 float for the divergence of $E$ error, 3 floats for the $B$ field, 1 float for the divergence of $B$ error, 3 floats for free current, 1 float for charge density, 3 floats for the transverse current adjustment field, 1 float for the bound charge density, and 8 short integers for identifying the various materials at different places in the grid); interpolators are represented as 72-byte structure (i.e., 18 floats for the various interpolator values); and current accumulators are represented as 48-byte structure (i.e., 4 floats for the current in the $x$ direction, 4 floats for the $y$ direction, and 4 floats for the $z$ direction).

Porting VPIC to use Kokkos requires that we store the data structures in Kokkos Views. Care must be taken during the conversion to Kokkos Views because the conversion approach directly affects the memory layout. Memory layout is important for performance, with different hardware performing better with different layouts and parallelism techniques (i.e., thread parallelism and vector parallelism) [30]. In general there are two major memory layouts, array of structures (AoS) and struct of arrays (SoA). The AoS stores multiple instances of a struct in an array such that they are contiguous in memory. The SoA layout, on the other hand, stores multiple instances of a struct in a single struct with arrays for each structure member. Each member stores values in a contiguous array. Fig. 3 demonstrates the differences between the layouts using particle position coordinates as an example. The AoS layout has each coordinate ($dx$, $dy$, $dz$) in memory one after the other. The SoA layout has separate arrays for each dimension. The AoS layout is favored by traditional CPU hardware. The array

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is easily broken into chunks that each thread can operate on independently. Cache efficiency on CPUs also improves with the AoS layout due to the higher likelihood of fitting an entire struct in a single cache line. On the other hand, the SoA layout is preferred for hardware with small caches such as GPUs. On CPUs, many threads execute the same instruction. The small cache size and high memory access latency makes each memory operation very costly. The SoA layout ensures that memory is accessed in a contiguous manner. Accessing contiguous blocks of memory helps the GPU use its full memory bandwidth.

**Array of structs layout**
Preferred by traditional CPU architectures

\[
\begin{matrix}
  dx_0 & dy_0 & dz_0 & dx_1 & dy_1 & dz_1 & \ldots & dx_n & dy_n & dz_n \\
\end{matrix}
\]

**Struct of arrays layout**
Preferred by vector architectures

\[
\begin{matrix}
  dx_0 & dx_1 & \ldots & dx_n & dy_0 & dy_1 & \ldots & dy_n & dz_0 & dz_1 & \ldots & dz_n \\
\end{matrix}
\]

Fig. 3: Comparison of Struct of Arrays (SoA) and Array of Structs (AoS) memory layouts for storage position in 3D Cartesian coordinates.

Simply replacing arrays with Views may be inefficient as this decision limits memory layout and decreases performance when, for example, running VPIC on GPUs. Swapping arrays for Views restricts the data to a CPU favoring AoS layout. Instead of swapping, we use a 2D View to store data such that the layout is automatically chosen based on the target hardware (i.e., CPU or GPU). Fig. 2 shows the application of this principle when moving VPIC’s particle data to a Kokkos View. The original VPIC macroparticle code (VPIC 1.0) in Fig. 2a stores particles in an array of particles. Fig. 2b shows how the data is stored and accessed in a 2D Kokkos View in VPIC 2.0. The first and second index determine which particle and member variable to access respectively.

While converting structures to 2D Views, we consider two types of structures: structures with all members having the same member type and structures with multiple member types. Data with structures containing a single member type (e.g., only float) are simply moved to a 2D Kokkos View where the first dimension determines the View size while the second dimension corresponds to the different struct members. For data with structures containing multiple member types, such as the macroparticle in Fig. 2a, members of a given type are gathered in their own View and multiple Views are deployed. Fig. 2b shows how the particle cell index is separated into its own View due to having a different type than the other macroparticle items. Table 1 summarizes the types of members and Views for the four key VPIC data elements.

For convenience, we define an enum with numerals matching the original struct fields. An enum provides a clear definition for accessing struct fields stored in Views. Fig. 2 shows the difference in code for the particles. In Fig. 2a, the particle is defined using plain C++. Transforming the code with Kokkos results in the particle definition in

| Data Structure | Member Types | Transformation |
|----------------|--------------|---------------|
| Particles      | float and int| Multiple Views|
| EM Fields      | float and short int| Multiple Views|
| Interpolators  | float        | Single View   |
| Accumulators   | float        | Single View   |

Table 1: Member types and necessary code transformations for the four key data structures. Heterogenous data requires separate Kokkos Views for each member type. Homogeneous structures only need a single Kokkos View.

Fig. 2b Both the declaration and data access code for particle storage is similar to the original VPIC 1.0 code from the . This conversion approach provides a single interface to managing data across multiple platforms and allows domain experts to focus on scientific discovery.

4.1.2 User Interface
VPIC has several functions that allow the user to collect diagnostics and adjust the simulation. Users define their desired adjustments and diagnostics in C++ along with the frequency at which VPIC should call the functions. Porting VPIC to Kokkos requires changes to the user interface for backwards compatibility and performance.

VPIC data is stored in Kokkos Views with an explicit separation between host and device data. This separation is a requirement for parallel execution and needs changes to the code to maintain backwards compatibility with existing VPIC decks. The existing interface assumes all operations are done on the old data structures. Thus data must be copied between the old structures and Kokkos Views. The explicit split between host and device data requires that both structures are synchronized before and after any user diagnostics or adjustments. As a result, data must be copied from the device to the host and copied again to the original VPIC data structures. We add a set of flags for controlling data movement for user defined functions. By default, VPIC automatically handles data movement such that legacy codes run without changes.

Shuffling data among the host, device, and original structures is costly. Users can avoid the performance impact from moving data by writing their user functions with Kokkos. Functions written using the Kokkos API can directly operate on the data regardless of where it resides. Thus, unnecessary data movement is avoided. This feature also enables users to easily parallelize their code and integrate it into VPIC seamlessly. Under these circumstances, users need only to write their functions and set the appropriate flags.

4.2 Other Code Transformations
We perform additional code re-engineering to further improve portability and performance.

4.2.1 Improving Portability
There are two changes to the VPIC code that enable broader portability across platforms. The first, we move away from the vectorization formulation heavily deployed in VPIC 1.0. Second, we replace the explicit data duplication used for scatter-reduction patterns with the more portable Scatter-View container provided by Kokkos.
The original VPIC 1.0 code was designed to exploit vectorization with explicit SIMD code. While highly performing on CPUs, the formulation does not fit the GPU programming model and adds significant complexity. We re-engineer the code to match the Kokkos model instead; such a model generalizes well across both CPUs and GPUs. As the Kokkos project develops, we will improve the code to better expose vector parallelism.

A ScatterView is a helpful structure for concurrent reductions. Concurrent updates are implemented in two ways depending on the target hardware. On CPUs, each thread duplicates the data and operates locally before collecting updates from all threads and updating the data. This is done to avoid slow atomic operations and improve cache performance. On GPUs, caches are smaller and atomic operations are faster so updates are done with atomics. Electrical current accumulation in VPIC uses arrays of accumulators so that each thread can collect contributions independently before updating the EM fields. A ScatterView accomplishes the same goal, so we replace the accumulator arrays with a ScatterView that updates the current directly.

### 4.2.2 Improving Performance

For improving performance on GPU systems we integrate four optimizations in VPIC: restructuring code to keep data resident in the GPU; exploiting hierarchical parallelism; changing particle sorting order; and specializing the reduction code.

Data movement in Kokkos is done explicitly. In our first optimization, we restructure VPIC to avoid data transfers due to the high cost of data movement in modern systems. Data and simulation settings are set on the host CPU during initialization by default. Simulation data is then copied to the execution device and kept there throughout the simulation. Data movement between device and host is only done for communication and user diagnostics. On CPU-only platforms, where host and device are the same, data copies are eliminated automatically. This code structure ensures high performance on GPUs while Kokkos prevents any unnecessary data movement for CPU only systems.

Executing code in parallel introduces several tuning parameters for controlling how work is partitioned between the parallel threads of execution. The default settings determined by Kokkos achieve good performance and clean code. Still, performance can be further improved using hierarchical parallelism. Kokkos supports three levels of hierarchical parallelism: (1) thread teams, (2) individual threads, and (3) vector parallelism. In our second optimization, we apply hierarchical parallelism to the particle pusher as it is responsible for the majority of the computation. By explicitly defining the number of teams and threads per team, we exert more control over data access patterns and reuse. This optimization improves performance for the particle pusher and is easily applied to multiple target architectures.

Particle’s sorting is a performance optimization in VPIC that significantly speeds up the particle pusher. The particle pusher must load interpolation data based on the particle’s cell index. Current accumulation is also based on the cell index. Each cell must accumulate the generated current from all particles inside the cell. Thus keeping particles sorted based on cell index improves cache reuse. This feature is applied for CPU architectures as the GPU memory hierarchy requires a change in sorting order. The traditional sorting order results in many threads trying to access the same address which prevents the GPU from using the full memory bandwidth. In our third optimization, we address this issue by sorting the particles such that threads will access memory contiguously (e.g., thread 0 accesses entry 0 and thread 1 accesses entry 1). This implementation not only improves the memory access pattern but also reduces the number of simultaneous writes to the same memory location.

GPU memory and atomic operation performance varies greatly between different manufacturers and hardware generations. Our fourth and final optimization uses the interoperability capabilities of Kokkos to implement target specific thread team reductions on GPUs. In particular, we introduce specialized CUDA code using warp intrinsics to accelerate current accumulation and reduce the number of atomic writes. Performance improvements are hardware dependent. The specialized code provides significant performance improvements for GPUs.

### 5 Performance and Portability Study

Our study of the newly optimized VPIC 2.0 code’s performance and portability is executed on a diverse group of hardware platforms. For the performance, we consider both weak and strong scaling. For the portability, we present insights on the effectiveness of VPIC to run across multiple architectures.

#### 5.1 Hardware Platforms

We present results from five GPU-based platforms, and four CPU-based platforms. The architectures are sorted chronologically based on the year of release. The platform configurations are as follows.

#### 5.1.1 GPU Platforms

**NVIDIA Pascal P100 (2016)** experiments are run on the Kodiak computer at Los Alamos National Laboratory. This computer consists of 133 nodes each with an Intel Xeon E5-2695 v4 CPU with 256 or 512 GB of DRAM and four NVidia Tesla P100 GPUs on a Mellanox InfiniBand EDR Fat-Tree interconnect.

**NVIDIA Volta V100 (2017)** experiments are run on the Sierra supercomputer at Lawrence Livermore National Laboratory. Sierra is a 125 petaflop, IBM Power Systems AC922 hybrid architecture system comprised of 4320 nodes, each with two 44-core IBM Power9 processors running at 2.3–3.8 GHz with 256 GB of RAM and four NVIDIA V100 GPUs each with 16 GB of HBM2 DRAM.

**NVIDIA Turing RTX 5000 (2018)** experiments use the RTX partition of the Frontera cluster at the Texas Advanced Computing Center. This partition consists of nodes containing two Intel Xeon CPU E5-2620 v4 running at 2.10 GHz with 128 GB of RAM. Nodes are connected by Mellanox Infiniband FDR at 56 Gb/s configured in a fat-tree topology with a 4:1 oversubscription. Each node also contains four NVIDIA Quadro RTX 5000 GPUs with
16 GB of GDDR6 DRAM.

AMD Vega Radeon VII (2019) experiments are executed on a single node consisting of two AMD EPYC 7302 16-core processors with 64 GB of DRAM and four AMD Radeon VII GPUs with 16 GB of HBM2 DRAM each.

NVIDIA Ampere A100 (2020) experiments are completed on the NVIDIA DGX SuperPod [31], Selene, at NVIDIA. Each node within this system contains dual AMD EPYC 7742 CPUs with 64 cores per socket running at 2.25 GHz and 2 TB of DRAM. The nodes are connected together using Mellanox Infiniband HDR at 200 Gb/s within a fat-tree topology that is configured for a 5:4 oversubscription. Each node contains eight NVIDIA A100 GPUs with 80 GB of HBM2 DRAM each.

5.1.2 CPU Platforms

Intel Knights Landing (2019) experiments use the KNL partition of the Trinitite testbed at Los Alamos National Laboratory. This partition consists of 100 nodes of a Cray XC40 system configured with a 3D Aries Dragonfly interconnect. Each node contains one 68 core Knights Landing processor with 16 GB of high-bandwidth MCDRAM and 96 GB of DRAM.

AMD Zen 2 (2019) experiments are run on the Bell cluster at Purdue University [32]. Each node contains two AMD EPYC 7662 64 core processors operating at 2.0 GHz and 256 GB of DRAM. Each node is connected with Mellanox Infiniband HDR at 100 Gb/s in a fat-tree configuration that is oversubscribed 3:1.

Intel Cascade Lake (2019) experiments are executed on the Frontera cluster at the Texas Advanced Computing Center [33]. Each node in Frontera contains two Intel Xeon Platinum 8280 processors with 28 cores operating at 2.70 GHz and 192 GB of memory. The nodes are connected with Mellanox Infiniband HDR at 100 Gb/s. The interconnect is configured in a fat-tree topology with an oversubscription factor of 11:9.

Fujitsu A64FX (2020) experiments were ran on the Oakami cluster at Stony Brook University. Oakami is an HPE Apollo 80 system with 174 nodes. Each node contains a Fujitsu A64FX Arm processor [34] with 32 GB of high-bandwidth memory and a 512 GB SSD. Nodes are connected in a 2-level tree using non-blocking HDR-200.

5.2 Weak Scaling

For a test problem to study weak scaling, we adapt a large 3D simulation of stimulated Brillouin scattering (SBS) in a single laser speckle [19] relevant for inertial confinement fusion experiments. Running the full simulation to completion would be prohibitive in our scaling tests, so we modify the simulation to be much shorter while preserving the numerical properties of the full simulation. Instead of a single very long laser pulse with a slow ramp in intensity, we use two counter-propagating laser pulses that ramp up linearly in field strength (quadratically in intensity) from zero at the start to twice the intensity of [19] at the end of the simulation. The simulation is stopped just before the two pulses collide. This arrangement gets particles moving near the start of the simulation, and thus is computationally similar to the majority of a full length simulation, and less like the uninteresting uniform cold plasma of early time steps.

We simulate a fully ionized nitrogen plasma of temperatures $T_e = 600$ eV and $T_i = 150$ eV, with density $n_e = 0.05n_{cr}$, where $n_{cr} = m_e\omega_0^2/e^2$ is the critical density for a laser with angular frequency $\omega_0 = 2\pi c/\lambda_L$. The plasma fills a simulation volume of $80\mu m \times 20\mu m \times 20\mu m$. Two identical laser pulses are incident on the plasma from the positive and negative $x$ direction. Each pulse is a focused Gaussian beam of wavelength $\lambda_L = 527$ nm and beam waist $w_0 = 4\mu m$, focused at the center of the simulation volume. The pulses increase linearly in field strength over time to a maximum intensity $I_0 = 5 \times 10^{15}$ W/cm$^2$ at the end of the simulation, $t_{stop} = (80\mu m/2)/c$. The grid has resolution $6000 \times 1500 \times 1500$, for a cell size very near the Debye length, and a domain decomposition of $60 \times 15 \times 15$ across 13,500 GPUs. Tests smaller than this full scale simulate a proportional fraction of the volume and use only one laser pulse. Tests using 32 or fewer GPUs have an adjusted number of particles per cell to account for boundary conditions (there is a “buffer” region at the simulation boundary where particles cannot be placed to separate particle and field boundary conditions), making the maximum number of particles a rank has at initialization equal for all tests.

We run the weak scaling on three cutting-edge, GPU-based platforms (i.e., Sierra with Power 9 CPUs and V100 GPUs, Selene with EPYC 7742 CPUs and A100 GPUs, and the Frontera with Xeon E5-2620 v4 CPUs and RTX 5000 GPUs). The reported runtime is measured on up 7,200 GPUs on Sierra, 1,024 on Selene, and 256 on Frontera; the times are on to normalized to 64 GPU runs. Fig. 4 demonstrates the results from the three GPU-based platforms and their different GPUs, spanning both commercial and consumer grade cards. Runtime measurements for Frontera (RTX 5000) are the average of five runs with a standard deviation of 2.268. VPIC runtime in general is very consistent. Sierra (V100) and Selene (A100) measurements are from a single run. The weak scaling results show excellent performance across the GPU architectures considered. The best scaling performance is shown by the NVIDIA Volta (V100) hardware on the Sierra supercomputer. The tests on the Sierra’s 7,200 GPUs show only a 3.45% slowdown versus the 64 GPU run. This is a testament to the capability of VPIC 2.0 to preserve performance while gaining in portability. Other the platforms (i.e., Selene and Frontera) scale about half as well as Sierra on the configurations that were made available to us for our testing.

We demonstrate the ability of VPIC 2.0 to run on CPU-based architectures for two platforms: the Bell cluster at Purdue University using EPYC 7662 CPUs and the Frontera cluster with Xeon 8280 CPUs only (without the use of GPUs). Fig. 5 shows the weak scaling on the two platforms. The runtime values are the average of five runs and are normalized to the 64 CPU runs, as in the GPU-based testing. The presented runtimes are the average of five runs. For our tests, we run multiple MPI ranks per socket, thus the
Weak Scaling on three GPU-based platforms (i.e., Sierra with Power 9 CPUs and V100 GPUs, Selene with EPYC 7742 CPUs and A100 GPUs, and the Frontera with Xeon E5-2620 v4 CPUs and RTX 5000 GPUs). Runtime is normalized to the 64 GPU runs, below which boundaries cause a reduction in per GPU communication.

per socket communication is constant for 4 or more sockets. While these performance results are notably slower than the GPU runs in absolute terms, they still add a lot of value from the perspective of our portability study. Furthermore, as accelerators become the driving architectures for large scale simulations, the community gathering around VPIC is expected to use GPU-based platforms rather than CPU-only ones.

**5.3 Strong Scaling**

The cache increase on the A100 to 40 MB from 6 MB on the V100 has tangible implications for how these two cards are best utilized in VPIC 2.0. A significant part of the particle push is depositing the current generated from particle movement to grid points. VPIC 2.0 periodically sorts the particles by voxel such that the number of grid points being written to is minimal at any given time. Minimizing the number of grid points to write to, allows the grid points to be stored in cache, resulting in faster writes. The A100 raises the intriguing possibility of storing the entire grid in cache, obviating the particle sort, and possibly producing super-linear speedup behavior in a strong scaling test as the total available cache increases.

We investigate this feature with tests similar to the weak scaling tests above, but with particle sorting turned off and only using the two larger supercomputers (i.e., Sierra with the V100 and Selene with the A100). The number of particles is kept constant while grid size varies. Fig. 6 shows the number of particle pushes per nanosecond as a function of grid size. The figure confirms that there is indeed a grid size where particle push performance increases dramatically, both for V100 and A100. Performance peaks for the V100 with approximately 4 particle pushes per nanosecond at 13,824 grid points. On the other hand, the A100 reaches 6 particle pushes per nanosecond with a grid size of 85,184. Further more, the performance jump occurs at roughly 6 times more grid points for A100 vs. V100, similar to the increase in cache. If this increase is from cache effects, we should see super-linear speedup in the following strong scaling tests. We suspect the performance drop for very few grid points, and thus extremely high particles per cell, on A100 is a result of colliding atomic writes in the current deposition.

Carefully selecting the size of our grid to match the peak performance in Figure 6, we run strong scaling tests on Sierra with V100 GPUs (i.e., from 1 to 32 GPUs), as shown in Fig. 7 and on Selene with A100 GPUs (i.e., from 8 to 512 GPUs), as shown in Fig. 8. As suggested by Fig. 6, we do indeed observe super-linear scaling for both architectures. For V100, we observe a 25x speedup for an 8x increase of GPUs, from 1 to 8. Beyond 8, the GPUs are very empty and communication overhead starts to cancel out the super-linear speedup. On A100, we see a 19x speedup for an 8x increase in the number of sockets.
increase of GPUs, from 8 to 64. Unlike the V100, we see near-ideal scaling all the way to 512 GPUs, the largest allocation we were able to test.

Fig. 7: Strong scaling on the Sierra with V100 GPUs. As the number of GPUs increases, more of the grid is kept in cache; as a result we get super-linear speedup. Communication costs eventually catch up with more than 16 GPUs.

The super-linear speedup from storing the grid in the cache has practical applications for certain classes of problems. Simulations with fewer grid points or high particle per cell requirements (e.g., cross-beam energy transfer inertial confinement fusion simulations [20]) can cut their runtime down significantly.

Smaller, non-full-scale simulations also benefit significantly from the super-linear speedup. The faster runtime enables domain experts and developers to quickly iterate through test parameters and tune their simulations before moving on to full-scale runs.

5.4 Portability Study

Our portability study assesses how effectively VPIC 2.0, a single source code, can run across multiple architectures.

To show to achieved portability, we present performance of each architecture listed in Sec. 5.1 for VPIC 2.0.

Fig. 8 shows a comparison of the different runtime measurements in seconds for the GPU-based platforms when running on 8 GPUs, with 1 MPI rank per GPU. The total simulation time is shown and is predominately compute time, as communication time is minimal at 8 MPI ranks. For the NVIDIA-based platforms (i.e., P100, V100, RTX 5000, and A100) we see a large jump between P100 and V100, which can be explained by the increased atomic operation support in the V100. We attribute the further jump from V100 to A100 to the increase in both cache size and FP32 performance. The RTX 5000, while slower than the V100, performs admirably for a workstation card and proves itself very capable of single-precision scientific simulations. The AMD Radeon VII underperforms when compared to the RTX 5000, despite having similar theoretical compute performance and superior memory bandwidth. The difference in performance can be attributed to two factors: (1) the maturity of the Kokkos AMD backend; and (2) the fact that to date NVIDIA cards have been used as the development and testing platform for this work. The performance of VPIC 2.0 may further increase as Kokkos improves the AMD backend.

Fig. 9: Total simulation time for small scale GPU performance (8 cards). Results are ordered chronologically (based on the GPU releases).

Fig. 10 provides a comparison of CPU-based platforms, including chips from AMD, Intel, and ARM/Fujitsu. For test normalization we compare 8 sockets of each platform, which represents a regime where MPI costs are non-negligible. While it is an impressive feat that the same source code of VPIC 2.0 can run on such a diverse range of hardware, it is interesting to note that the AMD Zen 2 is the only platform that achieves performance comparable to that shown in the GPU study. We attribute the lower performance on CPU-based platforms to the limited vectorization support in the current version of Kokkos (version 3.3). For further optimizations, one could formulate the VPIC 2.0 code expression that is better able to vectorize. We do not address vectorization in this work as that introduces non-trivial code divergence, and the focus of this study is on achieving portability over platform specific performance. It
is our belief that for cutting-edge performance on a specific target platform, some level of specialization will always be required. In many cases the portability abstraction layer may be able to achieve this, but other times the burden will fall to the programmer.

![Figure 10: Compute and communication time for small scale CPU performance (8 sockets). Results are ordered chronologically (based on the CPU releases).](image)

With a portability study such as ours that relies on an underlying toolkit to facilitate the codes operation on a variety of platforms, it is somewhat inevitable that the performance results reflect the priorities and maturity of the framework, as well as reflecting the facets of the target hardware. It is clear from these results that the code, as written in its present state, maps best to GPU platforms. Proposals have been made to extend Kokkos SIMD support, and we look forward to being able to leverage these improvements for VPIC 2.0.

6 SCIENTIFIC IMPACTS OF VPIC 2.0

The ability for any code to readily deploy itself on a new machine, with limited manual refactoring effort, is a huge win that actively drives down the time to scientific discovery. As the heterogeneity of modern platforms continues to increase to meet the demands of exascale, effective use of these platforms translates directly to codes such as VPIC being able to run simulations at unprecedented scales, and opens the door to performing analysis and investigation which was previously intractable. Sec. 5.2 demonstrates that VPIC 2.0, by following the methodology laid out in this paper, is well prepared for the exascale challenge.

While enabling portability, VPIC 2.0 is also able to assure performance. The performance-portability trade-off allows simulations to complete quickly and without multiple restarts by using accelerators and emerging architectures; such platforms are not optimized or supported by the original VPIC code (VPIC 1.0). The reduction in execution costs when using accelerators, coupled with the portability presented in this paper, facilitate the following changes in VPIC simulations:

- Simulating more timesteps in fewer core-hours enables simulations which advance further in time, allowing us to set our sights towards performing longer fully resolved electromagnetic simulations than were previously possible.
- Advanced and expensive diagnostics can now be performed within the timestep that allows for more accurate analysis. The extensive analysis enables new fundamental insights to particle acceleration modeling at unprecedented scales.
- Previous simulations, which took considerable resources, can now be run multiple times to analyze stochastic variation in, for example, short-pulse laser experiments, which in turn can generate sufficient data for machine learning analysis.

The newly release VPIC code opens up new avenues of science, carrying the domain of plasma physics research to exascale level simulations.

7 RELATED WORK

While the computational characteristics of PIC codes are fairly well understood, much of the communities optimization and development efforts to date have been focused around platform and hardware specific optimization. As heterogeneity within leading supercomputers increases, it is no longer viable to periodically optimize for a single target platform, making portability more important than ever. Within the PIC community, portability is underexplored, and our work seeks to address this weakness. Example projects such as PIConGPU and the AMITIS project demonstrate the applicability of the PIC algorithm to GPU architectures, but do not make a concerted effort to address the portability issues presented by the increasing diversity of modern HPC platforms.

We leverage the Kokkos framework to address many aspects of the performance-portability trade-off. While Kokkos represents a fairly modern approach to code portability, it has already established itself as a key technology in the race for performance portability, and has successfully helped a variety of applications run on multiple large-scale platforms. These target applications span science domains including finite element analysis, computational fluid dynamics, and even deep neural networks. It is of particular note previous work by the molecular dynamics community to leverage Kokkos for performance portability. Molecular dynamics is an important workload for Sandia National Laboratory, the creators of Kokkos; and is also the best explored workload that shares computational similarities with the PIC method. Both methods are particle dominated, and rely on the fast processing of large amounts of particles to simulate the kinetic level behavior of a large system. It is important to note, however, that Kokkos is not the only project which seeks to address issues of performance-portable code development. These tools can be split into two types: high-level frameworks (such as Kokkos, RAJA, or HPX) and lower-level tools for which code can be generated (such as OpenMP, SYCL, or HIP). A comparison of these technologies has already been the subject of previous studies. Our selection of Kokkos to support VPIC’s portability is based on the fact that Kokkos allows for high-level programmability while still offering good low-level performance.
8 Conclusion
In this work we present a performance-portable version of VPIC, a kinetic Particle-in-Cell code that has been used to do some of the worlds largest plasma physics simulations. This version of VPIC (VPIC 2.0) relies on the Kokkos framework for portability. We capture the VPIC 2.0 performance on nine different platforms (including three of the top 10 Top500 systems) and scale our tests on up to 7,200 GPUs. We demonstrate super-linear strong scaling on the NVIDIA A100 architecture and provide insights on the scientific impacts of VPIC 2.0 on scientific discovery for the next generation exascale supercomputers.

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