On Actual Preparation of Dicke State on a Quantum Computer

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Abstract—The exact number of CNOT and single qubit gates needed to implement a Quantum Algorithm in a given architecture is one of the central problems of Quantum Computation. In this work we study the importance of concise realizations of Partially defined Unitary Transformations for better circuit construction using the case study of Dicke State Preparation. The Dicke States $|D_k^n\rangle$ are an important class of entangled states with uses in many branches of Quantum Information. In this regard we provide the most efficient Deterministic Dicke State Preparation Circuit in terms of CNOT and single qubit gate counts in comparison to existing literature. We further observe that our improvements also reduce architectural constraints of the circuits. We implement the circuit for preparing $|D_2^2\rangle$ on the “ibmqx2” machine of the IBM QX service and observe that the error induced due to noise in the system is lesser in comparison to the existing circuit descriptions. We conclude by describing the CNOT map of the generic $|D_k^n\rangle$ preparation circuit and analyze different ways of distributing the CNOT gates in the circuit and its affect on the induced error.

Index Terms—Quantum Computing, Quantum Circuit, Dicke States, IBMQ, CNOT, Noisy Computation.

I. INTRODUCTION

One of the most fundamental aspects of Quantum Mechanics is Quantum Computation. Quantum Computers enable Quantum Algorithms that can perform operations with even super exponential speed-ups in time over the best known classical algorithms. Any quantum algorithm can be defined as a series of unitary transformations and can be implemented as a Quantum Circuit. A quantum circuit has a discrete set of gates such that their combinations can express any unitary transformation with any desired accuracy. Such a set of gates is called a universal set of gates. We know from the fundamental work by Barenco et.al [1] that single qubit gates and the controlled NOT (CNOT) gate form a universal set of gates. We call these gates as elementary gates.

Quantum State Preparation is a topic within Quantum Computation that has gained interest in the past two decades due to applications of special quantum states in several fields of Quantum Information Theory. A $n$-qubit quantum state $|\psi_n\rangle$ can be expressed as the superposition of $2^n$ orthonormal basis states. In this work we look at $n$ qubit states as super position of the computational basis states $|x_1x_2...x_n\rangle$, $x_i \in \{0,1\}$, $1 \leq i \leq n$. The basis states in the expression of $|\psi_n\rangle$ with non zero amplitude are called the active basis states. Starting from the state $|0\rangle^\otimes n$ any arbitrary quantum state can be formed using $O(2^n)$ elementary gates, although for many $n$-qubit states preparation circuits with polynomial (in $n$) number of elementary gates is possible. The family of Dicke States $|D_k^n\rangle$ is one such example. $|D_k^n\rangle$ is the $n$-qubit state which is the equal superposition state of all $\binom{n}{k}$ basis states of weight $k$. For example $|D_1^2\rangle = \frac{1}{\sqrt{3}}(|001\rangle + |010\rangle + |100\rangle)$, Dicke states are an interesting family of states due to the fact that they have $\binom{n}{k}$ active basis states, which can be exponential in $n$ when $k = O(n)$ but need only polynomial number of elementary gates to prepare. Dicke states also have applications in the areas of Quantum Game Theory, Quantum Networking, among others. One can refer to [2] for getting a more in-depth view of these applications.

There has been several probabilistic and deterministic Dicke state algorithms designed in the last two decades [3], [4], [8]. In this paper we focus on the algorithm described by Bärtsci et.al [2] which gives a deterministic algorithm that takes $O(kn)$ CNOT gates and $O(n)$ depth to prepare the state $|D_k^n\rangle$. To the best of our knowledge this circuit description has the best gate count among the deterministic algorithms. Here it is important to note that the paper by Cruz et.al [5] describes two algorithms for preparing the $|D_k^n\rangle$ states, also known as $W_n$ states. Both the algorithms have better gate count than the description by Bärtsci et.al [2] and one of the algorithms has logarithmic depth. However, their work is restricted to $|D_1^n\rangle$ and has no implication on the circuits for $|D_k^n\rangle$, $2 \leq k \leq n - 2$. We further observe in Section [14] that the circuit obtained by us after the improvements for $|D_1^n\rangle$ is same as the linear $W_n$ circuit described in [5].

Because of the noisy behavior of current generation Quantum Computers the exact number of elementary gates needed and the distribution of the gates over the corresponding circuit become crucial issues which need to be optimized in order to prepare a state with high fidelity. An example of a very recent work done in this area is [7] which reduces the gate count of AES implementation. In this regard we discuss the following important problems in the domain of Quantum Circuit Design.

A unitary transformation acting on $n$ qubits can be expressed as a $2^n \times 2^n$ unitary matrix and can be decomposed into elementary gates in several ways. Therefore finding the decomposition that needs the least amount of elementary gates is a very fundamental problem, with [6], [9] being examples of work done in this area. It is crucial to minimize the number of gates while decomposing a unitary matrix as every gate induces some amount of error into the result. Especially reducing the number of CNOT gates is of importance due to the well known fact that it induces more error compared to single qubit gates.

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\[ D_{k}^{n} \]
In this work we first describe a fundamental problem that decomposition of matrix using a universal set of gates poses. Let there be a unitary transformation that is to be performed on a system of \( n \) qubits. This task can be represented as a unitary matrix \( U_n \) that works on the Hilbert Space \( H_n \) of dimension \( 2^n \). If we know the intended transformation for all the states of any orthonormal basis of \( H_n \), that completely defines the unitary matrix \( U_n \). Let us consider such a transformation for \( n = 1 \). If the transformation is defined for the two states in the computational basis \( |0 \rangle \) and \( |1 \rangle \) then the corresponding unitary matrix is completely defined. If the transformation is defined as \( |0 \rangle \rightarrow \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle) \) and \( |1 \rangle \rightarrow \frac{1}{\sqrt{2}}(|0\rangle - |1\rangle) \) then the corresponding matrix is the Hadamard matrix, expressed as \[
\begin{bmatrix}
\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\
\frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}}
\end{bmatrix}.
\] However if the transformation is only defined for one state, \( |0 \rangle \rightarrow \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle) \) and not defined for \( |1 \rangle \) then there can be uncountably many unitary matrices that can perform the said transformation. Specifically, any matrix of the form \[
\begin{bmatrix}
\frac{1}{\sqrt{2}} & \alpha \\
\frac{1}{\sqrt{2}} & -\alpha
\end{bmatrix}
\] can perform this task, where \( \alpha \in \mathbb{C}, |\alpha|^2 = \frac{1}{2} \).

There exists many quantum algorithms where at a step a particular transformation on \( n \) qubits is defined only for a a subset of the states of a orthonormal basis. This creates the possibility of there being uncountably many unitary matrices capable of such a transformation. The algorithm described in \[2\] contains such transformations that are not completely defined for all basis states. We call such a transformation a partially defined unitary transformation on \( n \) qubits. There are possibly multiple unitary matrices that can perform this transformation. In that case it becomes an important problem to find out which candidate unitary matrix can be decomposed using the minimal number of elementary gates.

Furthermore, the number of elementary gates needed to implement a well defined Quantum Circuit also varies with the architecture of the actual Quantum Computer. The architectures of current generation Quantum Computers do not allow for CNOT gates to be implemented between any two arbitrary qubits. This CNOT constraint may further increase the total number of CNOT and single qubit gates needed to implement a Quantum Circuit on a specific Quantum Architecture. Against this backdrop, let us draw out the organization of the rest of the paper along with our contributions.

A. Organization and Contribution

In Section \[II\] we first describe the preliminaries needed to support our work. We first define the concept of maximally partial unitary transformation. We then describe the the circuit in \[2\] for preparing Dicke States. We denote the circuit described in \[3\] for preparing \( |D^n_k \rangle \) as \( \mathcal{C}_{n,k} \).

We start Section \[III\] by showing that a transformation implemented in \( \mathcal{C}_{n,k} \) is in fact a partially defined construction. We then show that the unitary matrix used to represent the transformation is not optimal in terms of number of elementary gates needed to decompose it. We propose a different construction that indeed requires lesser number of elementary gates and we also argue its optimality w.r.t the Universal gate set.

In Section \[IV\] we use the construction to improve the gate count of the circuit \( \mathcal{C}_{n,k} \) in a generalized manner. We remove the redundant gates in the circuit and analyze the different partially defined transformations implemented in the circuit to further reduce the gate counts of the circuit. We denote the improved circuit for preparing any Dicke State \( |D^n_k \rangle \) as \( \hat{\mathcal{C}}_{n,k} \). To the best of our knowledge this is the most optimal implementation of a deterministic Dicke state preparation circuit for \( |D^n_k \rangle, 2 \leq k \leq n - 2 \).

Next in Section \[V\] we discuss the architectural constraints posed by the current generation Quantum Computers that are available for public use through different cloud services. We discuss the restrictions in terms of implementing CNOT gates between two qubits in an architecture and how it increases the number of CNOT gates needed to implement a circuit in an architecture. In this regard we show that the improvements described by us in Section \[IV\] not only reduces gate counts but also reduces architectural constraints.

We implement the circuits \( \mathcal{C}_{4,2} \) and \( \hat{\mathcal{C}}_{4,2} \) on the IBM-QX machine “ibmqx2” \[11\] and calculate the deviation in each case from ideal measurement statistics using a simple error measure. Next we show how two circuits with the same number of CNOT gates and the same architectural restrictions can lead to different expected error due to different CNOT distribution across the qubits. We analyze this by proposing modifications in the circuit \( \hat{\mathcal{C}}_{4,2} \) possible because partial nature of certain transformations and how it reduces the number of CNOT gates functioning erroneously on expectation in a fairly generalized error model. We finish this section by drawing out the general CNOT map of \( \hat{\mathcal{C}}_{n,k} \), shown as the graph \( C^{n,k} \) and observing that there in fact exists \( n - k - 1 \) independent modifications each leading to a different CNOT distribution.

We conclude the paper in Section \[VI\] by describing the future direction of work in this domain and also note down open problems in this area that we feel will improve our understanding both in the domains of partially defined transformations and architectural constraints.

II. Preliminaries

We first define some terminologies that we frequently use before moving onto some definitions and the preliminaries.

A. Notations

1) \( |v_2\rangle \): If we look at a system with \( n \) qubits then all the \( 2^n \) orthogonal states in the computational basis can be expressed as \( |b_1b_2...b_n\rangle \), \( b_i \in \{0,1\}, 1 \leq i \leq n \). In that case for representing the state \( |b_1b_2...b_n\rangle \) we treat it as a binary string and express it as \( |v_2\rangle \) where \( v = \sum_{i=1}^{n} b_i 2^{n-i} \).

2) \( R_y(\theta) \): The \( R_y \) gate is a single qubit gate defined as follows. \( R_y(\theta) = e^{-i\theta Y} = \begin{bmatrix} \cos(\frac{\theta}{2}) & -i\sin(\frac{\theta}{2}) \\ i\sin(\frac{\theta}{2}) & \cos(\frac{\theta}{2}) \end{bmatrix} \).

3) \( X \): This is a single qubit gate defined as \( X = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \).
4) \(CU_j^i\). While implementing a controlled unitary on a two qubit subsystem we use the following notations. Let there be a \(n\)-qubit system. \(CU_j^i\) represents a two qubit controlled unitary operation where the \(i\)-th qubit is the control qubit and the \(j\)-th qubit is the target qubit.

B. Maximally Partial Unitary Transformation

Let there be a unitary transformation that acts on \(n\) qubits. To perform this transformation we have to create a corresponding unitary matrix. If the transformation is defined for all \(2^n\) states of some orthonormal basis then the unitary matrix is completely defined. On the other hand if the transformation is defined for a single state belonging to the computational basis, only a single column of the corresponding \(2^n \times 2^n\) matrix is filled. The rest can be filled up conveniently, provided its unitary property is satisfied. In this regard we call a unitary transformation on \(n\) qubits to be maximally partial if it is defined for \(2^n - 1\) states of some orthonormal basis. That implies only a column of the matrix is not defined. In this paper we observe how corresponding to a maximally partial unitary matrix there can be multiple unitary matrices and how the minimal number of elementary gates needed to implement these matrices may vary.

We end this section by describing the structure of Dicke states and a circuit designed for its preparation.

C. The Dicke State Preparation Circuit \(C_{n,k}\)

The circuit \(C_{n,k}\) as described in \([2]\) works on the \(n\) qubit system \(|q_1 q_2 \ldots q_n\rangle\)). The circuit \(C_{n,k}\) is broken into \(n - 1\) blocks of the form \(SCS_k^n\) of which the first \(n - k\) blocks are of the form \(SCS_{n-t}^{n-k}\), \(n - t > k\) which is then followed by \(k - 1\) blocks of the form \(SCS_{t-1}^{1}\), \(k \geq i \geq 2\).

A block \(SCS_k^n\) consists of a two qubit transformation and \(k - 1\) three qubit transformations. The two qubit transformation works on the \(n - 1\) and \(n\)-th qubits and we denote it as \(\mu_n\). We describe the overall structure of the circuit again in Section [3]. The three qubit transformations are of the form \(M^i_{n,k}\), \(n - 1 \leq i \leq n - k + 1\) where \(M^i_{n,k}\) works on the qubits \(l - 1, l\) and \(n\). This construction is interesting in how the transformations \(\mu\) and \(M\) are partially defined which raises different implementation choices, with possibly different number of gates needed for elemental decomposition. We now describe these two transformations for reference. We denote by \(|ab\rangle_x\) the qubits in the \(x - 1\) and \(x\)-th position in a system.

\[
\begin{align*}
\mu_n: & 
|00\rangle_n \rightarrow |00\rangle_n \\
|11\rangle_n \rightarrow |11\rangle_n \\
|01\rangle_n \rightarrow \sqrt{\frac{1}{n}} |01\rangle_n + \sqrt{\frac{n - 1}{n}} |10\rangle_n 
\end{align*}
\]

The implementations of these transformations in \([2]\) is shown in Figures 1 and 2, respectively. The first transformation, \(\mu_n\), is in fact a maximally partial unitary transform. Because of the partially defined nature of the transformation the \(CR_y\) and \(CCR_y\) gates are also not fed all possible inputs. Instead the input to the \(CR_y\) gates is only from the subspace spanned by the computational basis states \(|00\rangle\), \(|10\rangle\) and \(|01\rangle\). Similarly the input to the \(CCR_y\) gate is only from the subspace spanned by the states \(|000\rangle\), \(|010\rangle\), \(|011\rangle\), and \(|110\rangle\).

Next in Section [3] we look how partially defined transformations can be implemented more efficiently, and argue the optimality of this improvement with respect to this particular building block. Then in Section [4] we reduce the gate count of the circuit \(C_{n,k}\) by removing redundancies and analyzing how the \(\mu\) and \(M\) transformations act only on a subset of the defined computational basis states in specific cases.

III. Example of Optimality for a Maximally Partial Unitary Transformation

We have described the two partially defined unitary transformations used in the circuit \(C_{n,k}\). The implementation of the first transformation, \(\mu_n\) is done using a controlled \(R_y\) gate and two \(CNOT\) gates. This \(CR_y\) gate only acts on the states \(|00\rangle\), \(|10\rangle\), \(|01\rangle\) and their superpositions and the transformation never acts on the \(|11\rangle\) state. If we take \(\theta = 2 \cos^{-1} \left( \sqrt{\frac{1}{n}} \right)\).

We denote the transformation implemented by the \(CR_y(\theta)\)
Theorem 1. \[6, \text{Theorem B}\]

1) For a controlled gate \( CU \) if \( \text{tr}(U X) = 0 \) \( \det(U) \neq 0 \), \( \det U = 1 \), \( U \neq \pm I \) then the minimal number of elementary gates needed to implement \( CU \) is 4.

2) For a controlled gate \( CU \) if \( \text{tr}(U) = 0 \), \( \det U = -1 \), \( U \neq \pm X \) then the minimal number of elementary gates needed to implement \( CU \) is 3.

3) For a controlled gate \( CU \) the minimal number of elementary gates needed to implement \( CU \) is less than three iff \( U \in \{e^{i\phi} I, e^{i\phi} X, e^{i\phi} Z\} \), \( 0 \leq \phi \leq 2\pi \).

Our lemma follows immediately.

Lemma 1. It takes minimum 4 elementary gates to implement the \( CR_y(\theta) \) gate.

**Proof.** We calculate the values of \( \det R_y(\theta) \) and \( \text{tr}(R_y(\theta) X) \) to confirm the minimal number of gates needed to decompose \( CR_y(\theta) \).

\[
\det R_y(\theta) = \sin^2\left(\frac{\theta}{2}\right) + \cos^2\left(\frac{\theta}{2}\right) = 1
\]

\[
R_y(\theta) X = \begin{bmatrix}
-\sin\left(\frac{\theta}{2}\right) & \cos\left(\frac{\theta}{2}\right) \\
\cos\left(\frac{\theta}{2}\right) & \sin\left(\frac{\theta}{2}\right)
\end{bmatrix} \implies \text{tr}(R_y(\theta) X) = 0
\]

The result (1) of Theorem 1 concludes the proof.

However the transformation \( T_1(\theta) \) can in fact be implemented using three elementary gates as follows.

\[
T_1(\theta) = \left( R_y\left(-\frac{\alpha}{2}\right) \otimes I_2 \right) \text{CNOT}_1 \left( R_y\left(\frac{\alpha}{2}\right) \otimes I_2 \right), \quad \frac{\alpha}{2} = \frac{\pi}{2} - \frac{\theta}{2}
\]

This decomposition has also been used by Cruz et al. [5] in the \( W_n \) (\( D_4^n \) state) preparation algorithm. However, the corresponding transformation is defined only for the states |00⟩ and |01⟩ and no insight into the optimality of the implementation is given.

We first derive the underlying \( 4 \times 4 \) unitary matrix \( U^{0}(\alpha) \) that describes this three gate transformation. Next we prove that \( U^{0}(\alpha) \) needs at least three gates to be implemented by verifying the conditions of result (2) of Theorem 1. We end this section by showing that the transformation \( T_1(\theta) \) needs at least three elementary gates (including one CNOT) to be implemented, proving the optimality of the \( U^{0}(\alpha) \) implementation.

**Theorem 2.** The gate \( U^{0}(\alpha) \) performs the partially defined unitary transformation \( T_1(\theta) \) where \( \alpha = \pi - \theta \) and needs minimum three elementary gates to be implemented.

**Proof.** We first study the transformation carried out by \( U^0 \) in the subspace of \( T_1 \).

\[
|00\rangle \rightarrow \left( \cos\left(\frac{\alpha}{4}\right) |0\rangle + \sin\left(\frac{\alpha}{4}\right) |1\rangle \right) |0\rangle
\]

\[
\text{CNOT}_1 \rightarrow \left( \cos\left(\frac{\alpha}{4}\right) |0\rangle + \sin\left(\frac{\alpha}{4}\right) |1\rangle \right) |0\rangle
\]

\[
|10\rangle \rightarrow \left( \cos\left(\frac{\alpha}{4}\right) \left( \cos\left(\frac{\alpha}{4}\right) |0\rangle - \sin\left(\frac{\alpha}{4}\right) |1\rangle \right) + \sin\left(\frac{\alpha}{4}\right) \left( \sin\left(\frac{\alpha}{4}\right) |0\rangle + \cos\left(\frac{\alpha}{4}\right) |1\rangle \right) \right) |0\rangle
\]

\[
= \left( \cos^2\left(\frac{\alpha}{4}\right) + \sin^2\left(\frac{\alpha}{4}\right) \right) |00\rangle = |00\rangle
\]

\[
|01\rangle \rightarrow \left( \cos\left(\frac{\alpha}{4}\right) \left( \cos\left(\frac{\alpha}{4}\right) |0\rangle + \sin\left(\frac{\alpha}{4}\right) |1\rangle \right) |1\rangle
\]

\[
\text{CNOT}_1 \rightarrow \left( \cos\left(\frac{\alpha}{4}\right) \left( \cos\left(\frac{\alpha}{4}\right) |0\rangle + \sin\left(\frac{\alpha}{4}\right) |1\rangle \right) |0\rangle
\]

\[
|01\rangle \rightarrow \left( \sin\left(\frac{\alpha}{4}\right) \left( \cos\left(\frac{\alpha}{4}\right) |0\rangle - \sin\left(\frac{\alpha}{4}\right) |1\rangle \right) + \cos\left(\frac{\alpha}{4}\right) \left( \sin\left(\frac{\alpha}{4}\right) |0\rangle + \cos\left(\frac{\alpha}{4}\right) |1\rangle \right) \right) |1\rangle
\]

\[
= \left( 2 \cos\left(\frac{\alpha}{4}\right) \sin\left(\frac{\alpha}{4}\right) |0\rangle + \cos^2\left(\frac{\alpha}{4}\right) - \sin^2\left(\frac{\alpha}{4}\right) |1\rangle \right) |1\rangle
\]

\[
= \left( \sin\left(\frac{\alpha}{2}\right) |0\rangle + \cos\left(\frac{\alpha}{2}\right) |1\rangle \right) |1\rangle
\]

Setting \( \alpha = \pi - \theta \) gives us the same transformation as defined by \( T_1(\theta) \).

Now we completely define the gate \( U^0 \) by studying the
transformation acted on the state $|11\rangle$.

\[
R_y(\frac{\pi}{4}) \text{ on } q_1 \mapsto \left( -\sin\left(\frac{\alpha}{4}\right) |0\rangle + \cos\left(\frac{\alpha}{4}\right) |1\rangle \right) |0\rangle
\]

\[
\text{CNOT}_2 \mapsto \left( \cos\left(\frac{\alpha}{4}\right) |0\rangle - \sin\left(\frac{\alpha}{4}\right) |1\rangle \right) |0\rangle
\]

\[
R_x(-\frac{\pi}{4}) \text{ on } q_1 \mapsto \left( \cos\left(\frac{\alpha}{4}\right) \left( \cos\left(\frac{\alpha}{4}\right) |0\rangle - \sin\left(\frac{\alpha}{4}\right) |1\rangle \right) \right) \left( \cos\left(\frac{\alpha}{4}\right) \left( \sin\left(\frac{\alpha}{4}\right) |0\rangle + \cos\left(\frac{\alpha}{4}\right) |1\rangle \right) \right) |0\rangle
\]

\[
= \left( \cos^2\left(\frac{\alpha}{4}\right) - \sin^2\left(\frac{\alpha}{4}\right) \right) |0\rangle - 2 \cos\left(\frac{\alpha}{4}\right) \sin\left(\frac{\alpha}{4}\right) |0\rangle |1\rangle
\]

\[
= \left( \cos\left(\frac{\alpha}{2}\right) |0\rangle - \sin\left(\frac{\alpha}{2}\right) |1\rangle \right) |1\rangle
\]

So the overall transformation provided by $U^0(\alpha)$ is:

\[
|00\rangle \rightarrow |00\rangle
\]

\[
|10\rangle \rightarrow |10\rangle
\]

\[
|01\rangle \rightarrow \left( \sin\left(\frac{\alpha}{2}\right) |0\rangle + \cos\left(\frac{\alpha}{2}\right) |1\rangle \right) |1\rangle
\]

\[
|11\rangle \rightarrow \left( \cos\left(\frac{\alpha}{2}\right) |0\rangle - \sin\left(\frac{\alpha}{2}\right) |1\rangle \right) |1\rangle
\]

Therefore the gate $U^0(\alpha)$ is a two qubit gate which can be expressed as a controlled gate $CU(\alpha)$ gate where $U(\alpha) = \begin{bmatrix} \sin\left(\frac{\alpha}{2}\right) & \cos\left(\frac{\alpha}{2}\right) \\ \cos\left(\frac{\alpha}{2}\right) & -\sin\left(\frac{\alpha}{2}\right) \end{bmatrix}$. Now $\text{tr}U(\alpha) = 0$ and $\det U(\alpha) = -1$ for all $\alpha$. Therefore we can conclude from the result (2) in Theorem 1 that this gate requires at least three gates to be implemented.

We finally show the optimality of this implementation for implementing the two qubit transformation $T_1(\theta)$. In this section we take $\alpha = \beta = \gamma = 0$ and $\theta = \beta = \gamma = 0$. Therefore $a = 0$, $b = 0$, $c = 0$, $d = 0$. Therefore $M_0$ is the identity matrix.

Lemma 2. The transformation $T_1(\theta)$ needs at least one CNOT and two single qubit gates to be implemented for $0 < \theta < \pi$.

Proof. The transformation $T_1(\theta)$ is only defined for the basis states $|00\rangle$, $|01\rangle$ and $|10\rangle$. Any matrix $M(\theta)$ that can carry out the transformation is of the form

\[
\begin{bmatrix}
1 & 0 & 0 & a \\
0 & \cos\left(\frac{\theta}{2}\right) & 0 & b \\
0 & 0 & 1 & c \\
0 & \sin\left(\frac{\theta}{2}\right) & 0 & d
\end{bmatrix}
\]

where $a$, $b$, $c$, $d$ are complex unknowns. However since $M(\theta)$ is unitary we have $M(\theta)M(\theta)^\dagger = I$. Therefore $1 + aa^\ast = 1 \Rightarrow a = 0$. If $c = 0$, $d = 0$, $e = 0$, $f = 0$.

Now we use our observations to improve the gate count of the circuit $C_{n,k}$.

IV. IMPROVED GATE COUNTS FOR CIRCUITS OF $|D^n_k\rangle$

We first count the number of CNOT and single qubit gates in $C_{n,k}$ by reviewing the circuit. The circuit is composed of $n - 1$ blocks of gates called $SCS$. There are $n - k - 1$ blocks of the form $SCS^t_{k'}, k < t \leq n$ and $k - 1$ blocks of the form $SCS_{k+1}^{t+i}$, $1 \leq i \leq k - 1$.

Each block $SCS^t_{k'}$ consists of one two qubit transformation $\mu_t$ which is implemented on the qubits $t - 1$ and $t$ and $k - 1$ three qubit transformations of the type $M_{k'}^t$, $t - 1 \leq t \leq k - 2$. Here $\mu_t$ is implemented on the $t - 1$ and $t$-th qubit and $M^t_{k'}$ is implemented on the $l - 1$, $l$ and $l$-th qubit, as described in Section III. Each transformation of type $\mu$ is decomposed into two CNOT and a $T_1(\theta)$ transformation which is implemented as a $CR_y$ gate by adjusting the value of $\theta$. We have shown in Lemma 1 that a $CR_y$ transformation needs minimum 4 gates to implement. In fact it needs at least two CNOT gates. Therefore each $\mu$ transformation needs four CNOT and two single qubit gate. The number of transformations of type $M^{t}_{k'}$ is

\[
(n-k)(k-1) + \sum_{i=1}^{k-2} i = nk - n + k - k^2 + \frac{(k-1)(k-2)}{2}
\]

\[
= nk - k(k+1) - n + 1.
\]

Each $M_{k'}^t$ transformation is shown to require six CNOT and four single qubit gates. However one CNOT gate of each $M_{k'}^t$ transformation can be canceled by rearranging the first two CNOT gates of the next transformation.

The total number of CNOT gates and single qubit gates used to prepare the state $|D^n_k\rangle$ is shown in Table I.

| CNOT gates | $5(nk - \frac{k(k+1)}{2} - n + 1) + 4(n-1)$ |
| single qubit gates | $4(nk - \frac{k(k+1)}{2} - n + 1) + 2(n-1)$ |

TABLE I: Gates needed to prepare $|D^n_k\rangle$ as in \[2\].

Figure 5 shows the circuit $C_{0,3}$ in terms of CNOT, $CR_y$ and $CCR_y$ gates.

We show the circuit of $|D^2_3\rangle$ formed according to this construction method in Figure 5.

We now improve the gate counts of the circuit $C_{n,k}$ in the following ways.

Replacing $CR_y$ with $CU$

We first use the $CU$ gate shown in Section III to implement the transformation $T_1$ corresponding to each $\mu$ transformation which needs one CNOT and two single qubit gates to be implemented. Therefore each $\mu$ transformation needs three CNOT and two single qubit gates. Since there are $n - 1$ $\mu$ transformations this reduces the number of CNOT by $n - 1$ for any $|D^n_k\rangle$.

Next we observe that some of the $\mu_n$ and $M^n_{k'}$ transformations act as identity transformation, which we count as a function of $k$ for any $|D^n_k\rangle$.

The $\mu$ and $M$ transformations that act like Identity

Let there be a $n$ qubit system in some state $|\phi\rangle$. This state can be uniquely represented as a superposition of all $2^n$ (computational) basis state. The amplitude of a particular basis
state may or may not be zero depending on the description of $|\phi\rangle$. We call a basis state with non zero amplitude an active basis state. The affect of a unitary transformation $T$ on this state can be completely described by observing how it transforms the active basis states of $|\phi\rangle$. If the $k$-th qubit is in the zero (one) state in all the active basis states and the transformation $T$ doesn’t act on the $k$-th qubit in non trivial way on any of those basis states then the $k$-th qubit in all the active basis states of $T|\phi\rangle$ will also be in the zero(one) state. Using this simple fact we prove the following theorem using induction.

**Theorem 3.** If the $n$ qubit system is expressed as superposition of computational basis states after the block $SCS^{n-t}_{k}$ has acted then it can be expressed as

$$
\sum_{a=0}^{2^{t+1}-1} \sum_{b=0}^{2^{t+1}-1} \alpha_{a,b} \left( |0\rangle \otimes_{n-k-1} (\bigotimes_{i=1}^{t+1} |a_{i}^{bin}\rangle) \right),
$$

Thus the first $n-k-1$ qubits are all in the state $|0\rangle$ and the $(n-k+1)$-th qubit and the next $k-1$ qubits are all in the $|1\rangle$ state in all active basis states of the system. This concludes the base case.

Now assume that our statement holds true for some $t-1 < k-2$ we show that the statement also holds for $t$. The $SCS^{n-t}_{k}$ block is composed of the transformations $\mu_{n-t}, \mathcal{M}_{n-t}^{i}, n-t-1 \leq t \leq n-k+1$. The $n$ qubit system is in the state

$$
|\psi_{t-1}\rangle = \sum_{a=0}^{2^{t-1}-1} \sum_{b=0}^{2^{t-1}-1} \alpha_{a,b} \left( |0\rangle \otimes_{n-k-t} (\bigotimes_{i=1}^{t} |a_{i}^{bin}\rangle) \right).
$$

That is, the first $n-k-t$ qubits are in the state $|0\rangle$ in all active basis states and the $n-k+1$ and the next $k-t$ qubits are in the state $|1\rangle$. These are the first qubits to the transformations $\mu_{n-t}, \mathcal{M}_{n-t}^{i}, n-t-1 \leq i \leq n-k$. This implies the $\mu$ transformation and the $(k-2-t) \mathcal{M}$ transformations act as identity transformations on all active basis states.

The next $t \mathcal{M}$ transformations may get the $|0\rangle$ state to the first qubit and therefore the $n$-qubit system before the last $\mathcal{M}$ has been applied is in the state

$$
|\psi_{t-1}\rangle = \sum_{a=0}^{2^{t-1}-1} \sum_{b=0}^{2^{t-1}-1} \alpha_{a,b} \left( |0\rangle \otimes_{n-k-t} (\bigotimes_{i=1}^{t} |a_{i}^{bin}\rangle) \right).
$$

Finally the last three qubit transformation of the block $SCS^{n-t}_{k} \mathcal{M}_{n-t-1}^{n-t+1}$ acts on the system. Now since the $(n-t-k)$-th qubit is in the state $|0\rangle$ in all active basis states, the $\mathcal{M}$ gate may only trivially act on it and the $(n-t)$-th qubit. This results in the state

$$
|\psi_{t}\rangle = \sum_{a=0}^{2^{t+1}-1} \sum_{b=0}^{2^{t+1}-1} \alpha_{a,b} \left( |0\rangle \otimes_{n-k-t-1} (\bigotimes_{i=1}^{t+1} |a_{i}^{bin}\rangle) \right).
$$

This completes the proof. It is important to note that there may be many basis states in the expression of $|\psi_{t}\rangle$ with zero amplitude. However our focus is on qubits that are definitely going to be either in the zero state or in the one state in all active basis states.
This proof also shows that the \( \mu \) transformation and the \( k-2-t \) \( M \) transformations in the block \( SCS_{k-1}^{n-t} \), \( t < k-1 \) act as identity transformations and therefore can be removed from the circuit, which is the second improvement. Therefore the number of \( \mu \) transformations omitted is \( k-1 \) and the number of \( M \) transformation omitted are \( \frac{k-2(k-1)}{2} \). This removes \( 3(k-1) + \frac{5(k-2)(k-1)}{2} \) CNOT and \( 2(k-1) + \frac{4(k-2)(k-1)}{2} \) single qubit gates.

**The first non identity \( M \) transformation in \( SCS_{k}^{n} \)**

Having removed the \( \mu \) and \( M \) transformations we now look at the first transformation of the block \( SCS_{k}^{n-t} \), \( t < k-1 \) which is \( M_{n-t}^{n-1} \). This transformation depends on the states of the \( n-k \)-th and \( n-t \)-th qubits and affects the state of the \( (n-k) \)-th and \( (n-t) \)-th qubit. At this stage the \( n \) qubit system is at the state

\[
\sum_{a=0}^{2} \sum_{b=0}^{2} a_{n,k} |0\rangle^{\otimes n-k-t} \left( \bigotimes_{i=1}^{t} |a_{1n}^{b_{in}}\rangle \right) |1\rangle^{\otimes k-t} \left( \bigotimes_{j=1}^{t} |b_{jn}^{j_{jn}}\rangle \right).
\]

Therefore in all the active basis states both the \( n-k \)th and the \( n-t \)th qubits are in the state \( |1\rangle \). Therefore the three qubit transformation applied by \( M_{n-t}^{n-1} \) can be expressed as follows substituting \( t = n-k+1 \):

\[
|11\rangle |1\rangle_{n-t} \rightarrow |11\rangle |1\rangle_{n-t}
\]

\[
|01\rangle |1\rangle_{n-t} \rightarrow \sqrt{\frac{n-t-l+1}{n-t}} |01\rangle |1\rangle_{n-t} + \sqrt{\frac{l-1}{n-t}} |11\rangle |0\rangle_{n-t}.
\]

This is in-fact can be implemented as a two qubit transformation of the form \( \mu \) as in the \( (n-k-1) \)-th qubit is in the \( |1\rangle \) state in all the active basis states.

The transformation acts on the \( (n-k) \)-th and \( (n-t) \)-th qubits as \( M_{n-t}^{n-k-1} \equiv (CNOT_{n-k-t} \theta) (\theta) \), where \( \theta = 2\cos^{-1} \left( \sqrt{\frac{n-t+1}{n-t+k}} \right) \). We know that the \( CU \) gate requires one CNOT and two \( R_{y} \) gates to be implemented therefore \( M_{n-t}^{n-k-1} \) requires only three CNOT and two \( R_{y} \) gates. This improvement is reflected for all \( SCS_{k}^{n-t} \) such that \( n-t \geq n-k+2 \) that is for \( 0 \leq t \leq k-2 \). Therefore it reduces the number of CNOT gate in the circuit by further \( 2(k-1) \) and the number of single qubit gates by \( 2(k-1) \) as well.

Additionally for \( |D_{k}^{n}\rangle \), \( k > 1 \) when \( SCS_{k}^{n} \) is applied the \( n \)-qubit system is in the state \( |0\rangle^{\otimes n-k} |1\rangle^{\otimes k} \) and therefore the transformation \( M_{n-t}^{n-k-1} \) only acts on the basis state \( |01\rangle \).

The corresponding transformation is

\[
|01\rangle_{n-k+1} |1\rangle_{n} \rightarrow \frac{\sqrt{k}}{n} |01\rangle_{n-k+1} |1\rangle_{n} + \sqrt{\frac{n-k}{n}} |11\rangle_{n-k+1} |0\rangle_{n}.
\]

This can be implemented using a \( R_{y} \left( \frac{\pi}{2} \right) \) on the \( (n-k) \)-th qubit followed by a CNOT gate CNOT_{n-k} which removes further two CNOT and one single qubit gate.

We denote this circuit by \( \tilde{C}_{n,k} \). Combining the results we get the following count of CNOT and single qubit gates in the improved circuit. We now calculate the total improvement in the CNOT and single qubit gate counts for the \( |D_{k}^{n}\rangle \), \( k > 1 \) preparation circuit \( \tilde{C}_{n,k} \).

- The total number of CNOT gates removed = \( n - 1 + \frac{3(k-2)(k-1)}{2} + 2(k-1) + 2 \).
- The total number of single qubit gates removed = \( 2(k-1) + \frac{4(k-2)(k-1)}{2} + 2(k-1) + 1 \).

Therefore the total number of CNOT gates present in the circuit is

\[
5(nk - \frac{k(k+1)}{2}) - n + 1
\]

\[
- \left( n - 1 + \frac{3(k-2)(k-1)}{2} + 2(k-1) + 2 \right)
\]

\[
= 5nk - 5k^2 - 2n
\]

The number of single qubit gates present in the circuit is

\[
4(nk - \frac{k(k+1)}{2}) - n + 1
\]

\[
- \left( 2(k-1) + \frac{4(k-2)(k-1)}{2} + 2(k-1) + 1 \right)
\]

\[
= 4nk - 4k^2 - 2n + 1
\]

For \( k = 1 \) we get the number of CNOT as \( 3n - 3 \) (from \( n-1 \) \( \mu \) transformations) and the number of single qubits gate as \( 2n + 2 \). However, one CNOT gate can be further removed from each \( \mu \) gate as the active basis states in input to the \( \mu \) transformations are only \( |00\rangle \) and \( |01\rangle \). The resultant circuit is identical to the linear \( W_{n} \) preparation circuit in [5] and contains \( 2n - 2 \) CNOT and \( 2n - 2 \) single qubit gates and thus we don’t elaborate it further.

We know that the state \( |D_{k}^{n}\rangle \) can be prepared by first forming the state \( |D_{n-k}^{n}\rangle \) and then applying a \( X \) gate to each qubit. On that note it is interesting to observe that after the improvements the Circuits for \( |D_{k}^{n}\rangle \) and \( |D_{n-k}^{n}\rangle \) require the same number of CNOT gates.

| \( n \) | \( 4 \) | \( 5 \) | \( 6 \) | \( 7 \) |
|---|---|---|---|---|
| 2 | 22.12 | 31.20 | 40.28 | 49.36 | 58.44 |
| 3 | 27.7 | 41.20 | 55.33 | 69.46 | 83.59 |
| 4 | 46.10 | 65.28 | 84.46 | 103.64 |
| 5 | 70.13 | 94.36 | 118.59 |
| 6 | 99.16 | 128.44 |
| 7 | 133.19 |

**TABLE II: CNOT gate count of the pair \( C_{n,k}, \tilde{C}_{n,k} \)**

| \( n \) | \( 4 \) | \( 5 \) | \( 6 \) | \( 7 \) |
|---|---|---|---|---|
| 2 | 14.9 | 20.15 | 26.21 | 32.27 | 38.33 |
| 3 | 18.5 | 28.15 | 38.25 | 48.35 | 58.45 |
| 4 | 32.7 | 46.21 | 60.35 | 74.49 |
| 5 | 50.9 | 68.27 | 86.45 |
| 6 | 72.11 | 94.33 |
| 7 | 98.13 |

**TABLE III: Single qubit gate count of the pair \( C_{n,k}, \tilde{C}_{n,k} \)**
Table II and III show the number of CNOT and single qubit gates needed to implement the states $|D_k^Q\rangle$ for $4 \leq n \leq 8$, $1 \leq k \leq n-1$, respectively.

In the next section we show that our observations not only reduces the gate counts of the circuit but also reduces its architectural constraints.

V. ACTUAL IMPLEMENTATION AND ARCHITECTURAL CONSTRAINTS

A. Architectural Constraints

We are at the stage where quantum circuits can be implemented on actual quantum computers using cloud services, such as IBM Quantum Experience, also known as IQX [11]. However the architecture of the individual back-end quantum machines pose restrictions to implementation of a particular circuit. The most prominent constraint is that of the CNOT implementation. In this regard we use the terms architectural constraint and CNOT constraint interchangeably. Every quantum machine poses restrictions to implementation of a particular circuit due to CNOT on expectation without a reduction in the number of CNOT gates. Given a circuit it is crucial to find it’s minimal architectural needs in terms of the CNOT map without increasing the CNOT gate count. The IBM-Q systems mapping solutions show the modified circuit as the transpiled circuit given any circuit as input, although its solutions are not always optimal. In this paper we first consider the system “ibmqx2” ($Q_1$) of IQX. The CNOT map of $Q_1$ is shown in the Figure 7.

![CNOT map of Q1](image)

Against this backdrop we observe the CNOT constraints of the circuit $C_{4,2}$, implemented to prepare $|D_1^Q\rangle$. Then we implement the circuit $\hat{C}_{4,2}$ which is the result of the improvements shown in Section IV. We observe that the improvement proposed by us not only reduces gate counts but also reduces CNOT constraints. We implement these circuits in the system $Q_1$ and compare the measurement statistics of the two circuits by measuring the deviation from the ideal measurement statistics and find that the results of $\hat{C}_{4,2}$ is much more closely aligned with the ideal results. We end this section by showing how some changes in the circuit $\hat{C}_{4,2}$ possible because of partially defined transformations can lower the error in the circuit due to CNOT on expectation without a reduction in number of CNOT gates or change in the CNOT constraints.

B. Implementation and Improvement for $|D_1^Q\rangle$

We start by constructing the circuit $C_{4,2}$. We implement every $CR_y$ gate using two CNOT gates and two $R_y$ gate as we know that the $CR_y$ gate needs at least 4 gates to be implemented and every three qubit $M_n^t$ transformation using five CNOT and four $R_y$ gates (as given in the description...
of \( \mathcal{C}_4,2 \). The resultant circuit \( \mathcal{C}_4,2 \) is shown in Figure 8. This circuit contains 22 CNOT gates. We use the notation \( \theta_k^y \) to denote the angle \( 2 \cos^{-1}\left(\frac{R}{y}\right) \).

The CNOT map of the circuit is shown in Figure 9.

![Fig. 9: The CNOT map of \( \mathcal{C}_4,2 \)](image)

We then implement \( \hat{\mathcal{C}}_{4,2} \) by making the following changes to \( \mathcal{C}_4,2 \).

1) Implement the \( CU^o \) gate instead of \( CR_y \) gates.
2) Remove the Redundant \( \mu \) and \( \mathcal{M} \) transformation.
3) Reduce the gate count in implementation of \( \mathcal{M}_{n-k+1} \) type transformations.

This brings the total number of CNOT gates in the circuit to 12. We name the circuit at this stage \( \hat{\mathcal{C}}_{4,2} \).

These steps not only reduce the CNOT gates in the circuit but also reduces the CNOT constraints of the circuit. Figure 10 shows the circuit at this stage and the reduced CNOT map \( \hat{G}_{\hat{\mathcal{C}}}_{4,2} \) as shown in the Figure 11.

![Fig. 11: The CNOT map \( \hat{G}_{\hat{\mathcal{C}}}_{4,2} \) corresponding to the circuit \( \hat{\mathcal{C}}_{4,2} \)](image)

In fact the Graph \( \hat{G}_{\hat{\mathcal{C}}}_{4,2} \) can be shown to be a subgraph of \( G_A^3 \) under several mappings of qubits. Therefore this circuit can be implemented in the “ibmqx2” (\( Q_1 \)) machine with 12 CNOT. However the CNOT constraints of the circuits corresponding to even \( D^{(n)}_{k} \), \( k > 1 \) cannot be met by any IBM-Q architecture at this stage. Now we compare the results of the circuits \( \mathcal{C}_{4,2} \) which is due to \( \mathcal{C}_4 \) and \( \hat{\mathcal{C}}_{4,2} \) which is what we obtained after the reductions and modifications.

**Comparison of Measurement Statistics of \( \mathcal{C}_{4,2} \) and \( \text{Cir}^3_{4,2} \)**

The output by an ideal Quantum Computer would produce the state \( \sqrt{\frac{1}{2}} \sum_{\text{wt}(x)=w} |i_2 \rangle \) on a correct \( |D^n_w \rangle \) preparation circuit. We first verify the resultant state vectors to of the two circuits to see that they both ideally produce \( \sqrt{\frac{1}{2}} (|0011\rangle + |0110\rangle + |1011\rangle + |1100\rangle) \) and then use a primary error measure based on measurement in computational basis to estimate the closeness of the states formed by the two circuits from the ideal state \( |D^2_2 \rangle \).

We run both the circuits for the maximum possible shots (8192) and use the measurement statistics to estimate the closeness to the desired state using the following error measure. We define our error measure \( EM_{n,w} \) for the Dicke state \( |D^n_w \rangle \) as follows. Let \( p_i \) be the percentage of times the measurement of the circuit \( \mathcal{C} \) yields the result \( i_2 \). Then we have

\[
EM_{n,w}(\mathcal{C}) = \frac{1}{2} \left( \sum_{j,w(t(j)=w)} |p_j - \frac{1}{w}| + \sum_{j,w(t(j)\neq w)} p_j \right)
\]

An \( EM \) value of 0 signifies that the measurement statistics are exactly aligned with the expected ideal results while the \( EM \) value can at maximum be 1. We have calculated the \( EM \) values for results of different mappings for the circuit \( \mathcal{C}_{4,2} \).

It is very interesting to see that under different mapping of logical qubits to physical qubits in \( Q_1 \) from the user end the IQX mapping solution provided different transpiled circuits. We know that the number of CNOT in \( \mathcal{C}_{4,2} \) is 22. The transpiled circuits for \( \mathcal{C}_{4,2} \) had a minimum of 25 CNOT gates and were as high as 31 in some cases. The corresponding transpiled circuit contains 25 CNOT gates which is the least of all the transpiled circuits. Figure 12 shows the measurement statistics corresponding to the circuit with the minimum \( EM \) value, which is equal to 0.4088.

Next we look at the measurement statistics of the circuit \( \hat{\mathcal{C}}_{4,2} \). There are many mappings between logical and physical qubits in this case such that the CNOT constraint of the circuit is met. Let such a map be \( M : \{q_0,q_2,q_3,q_4\} \rightarrow \{0,1,2,3,4\} \). Then if there is a CNOT between \( q_i \) and \( q_j \) then there is an edge \( M(q_i) \leftrightarrow M(q_j) \) in graph \( G_A^{Q_1} \). In such mappings the IQX mapping solution didn’t implement any modification in the transpiled circuit as expected.

Here we present the result for the following map \( M_1 \)

\[
M_1 : \ q_0 \rightarrow 3, \ q_1 \rightarrow 2, \ q_2 \rightarrow 4, \ q_3 \rightarrow 0.
\]

Figure 13 shows the measurement statistics corresponding to this mapping and the resultant \( EM \) value is 0.282103. These results show that the circuit \( \mathcal{C}_{4,2} \) needs more than the specified number of CNOT while being implemented on “ibmqx2” and the measurement statistics of \( \hat{\mathcal{C}}_{4,2} \) is much more closely aligned with the ideal measurement statistics compared to \( \mathcal{C}_{4,2} \).

**C. Modifications leading to different CNOT error distributions**

We now discuss how we can in fact use partially defined transformations to further fine tune the circuit \( \hat{\mathcal{C}}_{4,2} \) depending on the specifications of the architecture. We consider a four qubit architecture \( A_4 \) with the same CNOT connectivity as \( \mathcal{C}_{4,2} \) and only differs in CNOT error distribution. We then observe how further modifying the circuit \( \hat{\mathcal{C}}_{4,2} \) can lead to lower CNOT error on expectation against some error distributions in the architecture \( A_4 \). We assume every edge in the CNOT map of \( A_4 \) is bidirectional, as is the case with all currently publicly available IBM-Q machines.

The CNOT error rate when applying a CNOT between qubits \( i \) and \( j \) (such that the edge \( i \leftrightarrow j \) is present in \( G_A \)) is denoted as \( e_{ij} \).

Figure 15 shows the CNOT map of the architecture.
**CNOT error model:** In this regard we define our error model to calculate CNOT error on expectation of a circuit implemented in the architecture $A_4$. The probability of a CNOT placed between qubits $i$ and $j$ acting erroneously in a circuit is dependent on the error rate of the corresponding CNOT coupling in the architecture. We call this CNOT error. We denote this probability with $f_e : [0, 1] → [0, 1]$. We do not assume the exact nature of $f_e$, but only that it is directly proportional to error rate (i.e. an increasing function) which is by definition.

Next we define the following Bernoulli random variables to calculate the number of CNOT acting erroneously on expectation when a circuit is applied on this architecture. We define a variable $x_k$ corresponding to each CNOT used in a circuit. The variable is assigned zero if the $k$-th CNOT is applied correctly while executing a circuit, and one otherwise.

Let us suppose the $k$-th CNOT is applied between qubits $i$ and $j$. Then we have $Pr(x_k = 1) = f_e(e_{ij})$ and The expected error while applying the CNOT is $E(x_k) = f_e(e_{ij})$. Therefore the CNOT error on expectation while implementing a circuit $C$ on the architecture is

$$E(C) = \sum_{ij} e_{ij} f_e(e_{ij}).$$

Having described the error model we look at the CNOT
distribution of the circuit $\hat{C}_{4,2}$ as a weighted graph $G_f$. The vertices and the edges of this graph is same as that of $G^{\hat{C}_{4,2}}$. The weight of an edge $q_i \leftrightarrow q_j$ is the number of CNOT gates applied between the two qubits in the circuit. The graph $G_f$ is shown in Figure 14.

Now we implement the circuit $\hat{C}_{4,2}$ on the architecture $A_4$ so that all CNOT constraints can be met. We observe that only the qubit 1 has degree 3 and therefore $q_1$ is mapped to the physical qubit 1. Then we can have the following maps which satisfies all the CNOT constraints.

1) $q_1 \rightarrow 1$, $q_0 \rightarrow 0$, $q_2 \rightarrow 2$, $q_3 \rightarrow 3$.
2) $q_1 \rightarrow 1$, $q_0 \rightarrow 2$, $q_2 \rightarrow 0$, $q_3 \rightarrow 3$.

Then the expected CNOT error of the circuit $\hat{C}_{4,2}$ when applied on the architecture $A_4$ is

$$E(\hat{C}_{4,2}) = 5f_e(e_{01}) + 3f_e(e_{02}) + 3f_e(e_{12}) + f_e(e_{13}).$$

We now show the circuit $\hat{C}_{4,2}$ (described in Figure 10) can be further modified using partially defined transformations so that the CNOT error in the circuit on this architecture will reduce on expectation under some error distribution conditions.

![Graph $G_f$ corresponding to $G^{\hat{C}_{4,2}}$.](image)

Fig. 14: Graph $G_f$ corresponding to $G^{\hat{C}_{4,2}}$.

![CNOT map of the architecture $A$.](image)

Fig. 15: CNOT map of the architecture $A$.

The first $R_y$ gate that acts on the second qubit of $\hat{C}_{4,2}$ is followed by the CNOT gates CNOT$^3_2$ and CNOT$^2_2$. The combined transformation $T_3$ of these two CNOT is defined only for two basis states on 4 qubits $|0011\rangle \rightarrow |0011\rangle$ and $|0111\rangle \rightarrow |0100\rangle$.

We use the partial nature of the transformation to modify the circuit as follows. Note that transformation $T_3$ is the first transformation that acts on $q_3$. Then if we start the circuit from the state $|0010\rangle$ instead of $|0011\rangle$ then we can define the transformation $T_4^1$ such that

$$T_4^1 \equiv (I_2 \otimes \text{CNOT}_2^3 \otimes I_2)(I_2 \otimes I_2 \otimes \text{CNOT}_2^2)$$

resulting in the same output states as $T_4$ for all the computational basis states for which $T_4$ is defined. It is important to note that this implementation would not have been possible if the transformation was defined for all the 8 basis states of the second third and fourth qubits.

We denote this circuit as $\hat{C}'_{4,2}$ and it is drawn in Figure 17. We denote the weighted CNOT map of the circuit $\hat{C}'_{4,2}$ as $G'_f$ and it is shown in Figure 16.

We now see that in $G'_f q_2$ has degree three and therefore any map that meets all the CNOT constraints will have $q_2 \rightarrow 1$. Therefore we can have the following maps that satisfies all the CNOT constraints.

1) $q_2 \rightarrow 1$, $q_0 \rightarrow 0$, $q_1 \rightarrow 2$, $q_3 \rightarrow 3$.
2) $q_2 \rightarrow 1$, $q_0 \rightarrow 2$, $q_1 \rightarrow 0$, $q_3 \rightarrow 3$.

The CNOT error on expectation for both the circuits is

$$E(\hat{C}'_{4,2}) = 5f_e(e_{02}) + 3f_e(e_{01}) + 3f_e(e_{12}) + f_e(e_{13}).$$

Now we calculate the conditions when $E(\hat{C}'_{4,2})$ is less than $E(\hat{C}_{4,2})$.

$$E(\hat{C}'_{4,2}) < E(\hat{C}_{4,2})$$

$$\Rightarrow 5f_e(e_{02}) + 3f_e(e_{01}) + 3f_e(e_{12}) + f_e(e_{13}) < 5f_e(e_{01}) + 3f_e(e_{02}) + 3f_e(e_{12}) + f_e(e_{13})$$

$$\Rightarrow f_e(e_{02}) < f_e(e_{01})$$

$$\Rightarrow e_{02} < e_{01}.$$  

This gives us an insight into how different CNOT distributions in a circuit may lead to better results without reduction in the number of CNOT gates or a reduction in the architectural constraints. We conclude this section by describing the architectural constraint of the circuit $\hat{C}_{n,k}$.

### D. The CNOT map of $\hat{C}_{n,k}$

The CNOT gates in the circuit $\hat{C}_{n,k}$ are due to implementation of the $\mu$ and $\mathcal{M}$ transformation of the different $SCS^n_k$ blocks. $\mu_n$ forms an edge in the CNOT map of the form $n-1 \leftrightarrow n$, where as $\mathcal{M}_n^l$ forms the edges $(l-1) \leftrightarrow n$ and $l \rightarrow (l-1)$. However in the circuit $\hat{C}_{n,k}$ the transformations $\mathcal{M}_n^{l-k+1}$ do not have a CNOT between the neighboring qubits $n-k$ and $n-k+1$.

We divide the edges into two groups. One corresponding to CNOT gates between neighboring qubits and one where the positions of the qubits differ at least by two. We calculate the edges of each of these types.

- The neighboring qubits with CNOT connections are the qubits $(n-k+1-i)$ and $(n-k-i)$ where $i$ varies from 0 to $n-k-1$. The other neighboring qubits do not have CNOT connections due to removal of identity transformations form those qubits. This results in $n-k$ edges.
Figure 18 and 19 show the CNOT maps $G_{n,k}$ that the number of CNOT gates between the qubits change are same they are not isomorphic. Moreover the Graph $G_{n,k}$ note that although the number of edges in $G_{n,k}$ the total number of edges in $M_{n,k} - 1$ + 1 $\leq k \leq n - k + 1$ the edge $n \rightarrow (n - k)$ is not present. Figure 18 and 19 show the CNOT maps $G_{6,2}^6$ and $G_{6,3}^6$ respectively.

- Now we consider the second kind of connections. These connections are formed between $l - 1$ and $t$ th qubit for any $M_{i}$ transformation. There are $n - k$ SCS$_k^t$ blocks with originally $k - 1$ $M$ transformations in $C_{n,k}$ which forms the edges:

  $(n-t) \leftrightarrow (n-t-2-i), \ 0 \leq i \leq k-2, 0 \leq t \leq n-k-1$.

  Then there are $k - 1$ blocks of SCS$_t^{n+1}$ with $i - 1$ $M$ transformations which forms the edges:

  $(k-t) \leftrightarrow (k-t-2-i), \ 0 \leq i \leq k-t-2, 0 \leq t \leq k-2$.

  However in $C_{n,k}$ there are no $M$ transformations of the type $M_{y,z,k+1}$, $x > 0$. Removing such edges $n - k + x \leftrightarrow y$ gives us the complete description of the CNOT map of $C_{n,k}$, which we denote by $G_{n,k}$. Additionally, in the transformation $M_{n,k} - 1$ the edge $n \rightarrow (n - k)$ is not present.

Figure 18 and 19 show the CNOT maps $G_{6,2}^6$ and $G_{6,3}^6$ respectively.

Fig. 17: Circuit description of $\hat{C}_{4,2}$

Fig. 19: The CNOT map $G_{6,3}^6$

Fig. 18: The CNOT map $G_{6,2}^6$

We now count the number of edges in $G_{n,k}$. The number of edges present due to $M$ transformations is $nk - \frac{k(k+1)}{2} - n + 1 - \frac{(k-1)(k-2)}{2} = nk - n - k^2 + k$. There are further $n - k$ edges due to the $\mu$ transformations. Which brings the total number of edges in $G_{n,k}^6$ to $nk - k^2$. It is important to note that although the number of edges in $G_{n,k}^6$ and $G_{n,n-k}^6$ are same they are not isomorphic. Moreover the Graph $G_{n,k}^3$ is not a subgraph of $G_{n,i+1}^6$.

Finally we observe that the circuit $\hat{C}_{n,k}$ can be modified so that the number of CNOT gates between the qubits change for certain cases, although the total number of CNOT gates and the overall CNOT map does not change. We call these different instances as different CNOT distributions of $\hat{C}_{n,k}$.

Different CNOT distributions for $\hat{C}_{n,k}$

We know from the description of $\hat{C}_{n,k}$ [2] that the number of CNOT gates in the three qubit transformation $M$ is reduced from 6 to 5 by canceling the last CNOT of every transformation by rearranging the first two CNOT gates of the next transformation. Figure 20 shows the original layout as per the algorithm and Figure 21 shows the reduction due to [3].

Now let us consider the last transformation $(k-th)$ of each SCS$_k^t$, $0 < i < n - k$ block, $M_{n-i-k+1}^n$. This transformation acts on the qubits $n - i - k, n - i - k + 1$ and $(n - i)$. This is in fact the first transformation that affects the qubit $(n - i - k)$ and thus the qubit is in the state $|0\rangle$. If we do not cancel the last CNOT of the preceding $M$ transformation ($CNOT_{n-i-k}$) this then enables us to remove of the CNOT gate ($CNOT_{n-i-k}$), changing the CNOT distribution of the circuit without a change in CNOT map or number of CNOT gates. This leads to the implementation shown in Figure 22. Since there are $n - k - 1$ such transformations, this leads to a total of $2^{n-k-1}$ different CNOT distributions. However, these modifications do not alter the CNOT map of the circuit due to the fact that there are other CNOT gates applied between these qubits, which is evident from the circuit description. As we have observed in Section [V-C] such different CNOT distributions may lead to different number of CNOT gates acting erroneously on expectation and thus affect the overall error induced in the circuit.
Vi. Conclusion

In this paper we have explored the domain of optimal circuit implementation in terms of CNOT and single qubit gates. In this regard we have concisely realized partially defined unitary transformations to improve the gate count of the most optimal deterministic Dicke state ($\hat{D}_{n,k}$) preparation circuit ($C_{n,k}$). We have improved the implementation of one such transformation and have also proven the optimality of our implementation. We have further improved the Dicke State preparation circuit by removing redundant gates and modifying implementations of certain partially defined unitary transformations depending on the active basis states that that act as input to these transformations. We have then shown that these improvements not only reduce the number of CNOT and single qubit gates but also reduces the architectural constraints of the circuit using the case of $[D^2_{n,k}]$. The resultant circuit is the deterministic Dicke State ($[D^2_{n,k}], 2 \leq k \leq n - 1$) Preparation Circuit with the least number of elementary gates to the best of our knowledge. We have implemented the circuits $C_{4,2}$ and the improved circuit $\tilde{C}_{4,2}$ on the IBM-Q machine “ibmqx2” and observed that the deviation from ideal measurement statistics is significantly lesser in case of $\tilde{C}_{4,2}$. Furthermore, we have shown that how different CNOT distributions can help a circuit without changing the number of gates or the architectural constraints by comparing the expected CNOT error of two such distributions against a fairly generalized error model. We have concluded by describing the CNOT map of the circuit $\tilde{C}_{n,k}$ and observe the exponential number of different CNOT distributions that can be derived by modifying the circuit to complete our generalization.

We observed that even the circuits for $[D^2_{n,k}]$ could not be implemented in the IBM back end machines without adding further CNOT gates to our description. This is because of incompatibility of the architecture and circuit CNOT maps. Therefore it is of all the more importance to form the circuit for an algorithm in the most concise way possible. Against this backdrop we have shown how optimally realizing partially defined unitary transformations can lead to better implementation results. In conclusion we note down the following optimization problems that will help us implement algorithms more efficiently in the current scenario.

1) Given a maximally partial unitary transformation what is the corresponding unitary matrix that can be decomposed using the least number of elementary gates?

2) Given two circuits corresponding to an algorithm with isomorphic CNOT maps and the same number of CNOT gates, but different CNOT distribution across the qubits, which circuit will produce less erroneous outcome?

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