Double Sliding-Surface Multiloop Control Reducing Semiconductor Voltage Stress on the Boost Inverter

Oswaldo López-Santos and Germain Garcia

1 Facultad de Ingeniería, Universidad de Ibagué, Carrera 22 Calle 69 Barrio Ambalá, 730001 Ibagué, Colombia
2 LAAS-CNRS, Université de Toulouse, CNRS, INSA, 31077 Toulouse, France; garcia@laas.fr

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Abstract: Sliding-mode control (SMC) has been successfully applied to boost inverters, which solves the tracking problem of imposing sinusoidal behavior to the output voltage despite the coupled or decoupled operation of both boost cells in the converter. Most of the results reported in the literature were obtained using the conventional cascade-control structure involving outer loops that generate references for one or two sliding surfaces defined using linear combinations of inductor currents and capacitor voltages. As expected, all proposed methods share the inherent robustness and insensitivity to the uncertainties of SMC, which are the reasons why one of the few comparison criteria between them is the simplicity of their implementation that is evaluated according to the required measurements and mathematical operations. Furthermore, the slight differences between the obtained dynamic performances do not allow a clear distinction of the best solution. This study presents a new SMC approach applied to a boost inverter in which two boost cells are independently commutated. Each of these boost cells integrates an outer loop, enforcing the tracking of harmonic-enriched waveforms to the capacitor voltage. Although this approach increases by two the number of measurements and requires multiloop controllers, it allows effective alleviation of the semiconductor voltage stress by reducing the required voltage gain. A complete analytical study using harmonic balance technique allows deducing a simplified model allowing to obtain a PI controller valid into to the whole set of operation conditions. The several simulation results completely verified the potential of the control proposal and the accuracy of the employed methods.

Keywords: boost inverter; harmonic balance; sliding mode control

1. Introduction

The DC–AC boost converter, boost inverter, differential boost inverter or dual boost inverter, as it has been called by different authors in the literature, was introduced by Caceres and Barbi in the 1990s [1]. The potential that allowed this converter to attract the interest of researchers in the following decades was its ability to overcome the most restrictive limitations of the conventional and well-established full-bridge inverter. This is mainly related to the possibility of generating AC voltages with amplitudes larger than the input DC voltage without requiring more than one conversion stage or increasing the number of power semiconductors. This interesting topology is composed of two identical cells using symmetrical bidirectional boost DC–DC converters that share a back-to-back or bridge connection and differentially provide the output voltage between their outputs. This feature is characterized by a reduced common-mode noise but can be affected by DC current circulation in the load if the bias component of the output voltage of the cells is not correctly equalized [2].

Although the aforementioned features of the boost inverter are very attractive, these can only be achieved by developing more complex controllers or applying more complex methods to synthesize the required controllers. Compared with its counterpart, i.e., the full-bridge inverter, the highly nonlinear
dynamic behavior of the output voltage as a function of the operating duty cycle makes devising an effective control solution difficult. The higher the required gain to generate the output voltage is, the higher is the effect of nonlinearity on the dynamic behavior causing that linear controllers cannot guarantee a proper operation. Further, we need to mention that the approach performance based on linear control is directly affected by the non-minimum phase nature of the output voltage to control the transfer function of each boost cell.

Sliding-mode control (SMC) was practically the first approach in the reported literature applied to control a boost converter in the context of a stand-alone operation. In [1], Caceres and Barbi defined a sliding surface for each boost cell using a linear combination of current and voltage errors. Although the required voltage references were nothing more than two DC-biased sinusoidal waveforms with a 180° phase shift between them, the current references were difficult to synthesize because it depended on the input voltage and load current. Hence, the current-error component of the surfaces was obtained by measuring the high-frequency component of the inductor currents by assuming perfect tracking of the references in the stationary state. This approach was implemented using hysteresis comparators that then generated a variable switching frequency. This first proposal could be classified into a set of double-surface SMC (DS-SMC) approaches. A second method that employed SMC was introduced by Cortes et al. in [3] in which the control of both boost cells were correlated by complementarily coupling the commutation of the switches in the boost cells. In that work, a unique sliding surface was defined that involved the difference between the inductor currents and the proportional and integral actions that both operated under an output–voltage error. This second proposal, which could be classified as a single-surface SMC, was implemented using a single hysteresis comparator and required one less measurement because the voltage of the capacitors were not separately controlled. Furthermore, in the selected sliding surface, identifying the form of the well-known indirect control applied to regulate the output voltage of DC–DC converters was possible using an outer proportional–integral (PI) controller and a current inner loop. More recently, Flores-Bahamonde et al. have reemployed the same technique by preserving the coupled control action between the converter cells and applying an equivalent control technique to provide an analytical solution for synthesizing the outer voltage controller [4]. From the perspective of that work, the converter was controlled by imposing a periodic reference to the difference between the input currents of the cells, which in turn was generated by a PI outer loop that was configured to enforce the desired shape on the output voltage. That work also employs a hysteresis comparator for implementation. Finally, from a different perspective of the SMC application in this field and using a constant-frequency modulator, Wai et al. developed an adaptive fuzzy-neural-network control (AFNNC) in combination with a total sliding-mode controller [5]. To design the controller, an additional loop, called as curbing controller, allowed modification of the sliding surface to cope with unpredictable disturbances, whereas the AFNNC modified the sliding-surface parameters to ensure permanent stability. Naturally, despite the achieved good performance, the required implementation was considerably complex compared with that in [4]. In addition, SMC has been applied to the control of boost inverters in grid-connected applications, which is similar to the work reported in [6] in which a boost-inverter-based hybrid energy-storage system (HESS) integrates both batteries and supercapacitors to the grid using two sliding-mode controllers. A particular aspect to consider regarding this work is the fact that the system can be considered as two boost inverters that share the connection to the cell capacitors and then share the AC-side differential connection. The complexity of the control in this approach then comes from the power control used to inject apparent power into the grid (both active and reactive power), the control used to impose the charge–discharge regimes of the storage devices and the compact configuration of the HESS.

More recently, following the interest in systems involving batteries and fuel cells, researchers have paid more attention to the input–current behavior of the boost inverter mainly because of the scientific results that demonstrate that the ripple content exerts an important negative effect on the lifetime of storage devices. In a stand-alone case, to adequately shape the output voltage, the control must minimize the ripple content of the input current, which constitutes an important control objective.
As expected, the simultaneous accomplishment of these two functions results in new stationary behavior in the inner variables, which is reflected in their harmonic content. In [7], Jha et al. presented a cascade-control approach based on the use of a linearization function that evolved depending on the load and input–voltage operating conditions. A particular feature of this proposal was the use of three voltage measurements that shared the same reference and that no current measurement was required. Similarly, Zhu et al. proposed in [8] a waveform control using a cascade controller with two loops: one that shaped the voltage of the capacitors of the boost cells and the other that shaped the overall output voltage. These two controllers exhibited the characteristic of avoiding the use of current measurements.

In the grid-connected case, the control of the inverter forces the shape of not only the output voltage, but also the current to inject the generated power into the grid. This application of the boost inverter was explored by Angelidis and Vassilos et al. in [9] using a cascade-control scheme that involved a loop compensation of the nonlinear gain of each boost cell and then provided the reference of the inner loops that affected the inductor currents. Similar to the stand-alone case, the enforcement of the input current to be simultaneously constant with the primary control objective implies an adjustment of the stationary behavior of the converter variables. A rule-based cascade controller that determined a component to be added to the voltage references in order to cancel the second-order harmonic of the input current was developed in [10]. The proposed scheme required the measurement of the ripple component of the input current to compute the amplitude and phase of the voltage references of the cascade loops that included a voltage outer loop and a current inner loop per boost cell. The innovative feature of this controller was the use of a perturb and observe algorithm that computed the amplitude and phase of the required additional components. Again, a similar cascade-control scheme was proposed in [11] where an additional outer loop generated the added components from the measurement of the AC component of the input current. The proposed loop separately determined the AC components to avoid undesired phase shifts. The common feature of these last three controllers was the use of harmonic-enriched references in the capacitor-voltage control loops, which increased the ability of the control system to perform a second function in addition to the tracking of the output voltage or current. Other interesting works that improved the control of boost inverters can be found into battery-charging [12,13] and fuel-cell-based applications [14,15].

This study presents an alternative DS-SMC approach that is applied to a boost inverter in which the boost cells are independently commutated using one cascade controller per cell, thereby enforcing tracking of harmonic-enriched reference waveforms to shape the capacitor voltage. Second- and fourth-order terms are introduced to reduce the instantaneous-voltage gain of the cells, which results in the alleviation of the voltage stress of the switches throughout the period of the output voltage, as previously assessed in [16] where the same converter was modified by introducing additional power semiconductors and using half-cycle rectified voltage references. In contrast to the SMC approach developed in [4], the proposed control requires two additional voltage measurements, one additional hysteresis comparator and a complementary reference generator to produce the two required harmonic components. Although this last aspect supposes an increment in terms of cost of the solution, the three required voltage measurements share the same electric reference which suppose no need of isolation. Furthermore, since isolation is preferred for increased values of nominal power of the inverter, the cost of the additional electronics will become irrelevant. Beside this, complexity of the system is not really affected because the control philosophy is the same (hysteresis comparison and PI outer loop). The size of the electronic circuit or the computational cost increase depending on the type of implementation, but this aspect is not comparable with the considerable reduction of the semiconductor voltage stress.

The rest of the study is organized as follows: The boost converter operation and the fundamentals of the performance improvement are presented in Section 2. After that, in Section 3, the ideal sliding motion is analyzed for the entire range of operation conditions using the harmonic balance technique. The constraints to ensure asymptotic stability when tracking the required periodic behavior are provided as well as a simplified model of the inner loop dynamics. The fundamentals for synthesis
and implementation of the outer controllers are also explained. Comparative simulation results demonstrate the feasibility and advantages of the proposed control in Section 4. Finally, conclusions and future work are presented in Section 5.

2. Fundamentals of the Performance Improvement

The boost inverter depicted in Figure 1 is a fourth order DC–AC converter which is composed by two conventional boost converter cells. The sub-indices $x = \{1, 2\}$ were defined to differentiate left and right sides of the converter, respectively. Each cell is integrated by one inductor ($L$), one capacitor ($C$) and two controlled switches ($S_{x1}$: high-side and $S_{x2}$: low-side). The two switches into a cell assemble a bridge leg and then the complete circuit topology is quite similar to the conventional full-bridge inverter. The input voltage $v_{in}$ is applied to the inputs of the two cells and the output voltage ($v_o$) is obtained as the difference between the voltages of the output capacitors of the cells ($v_1$ and $v_2$). The study is developed considering a resistive load $r_o$.

![Figure 1. Schematic diagram of the boost inverter circuit.](image)

Stand-alone applications demand that inverter produces a pure sinusoidal signal from a DC input voltage which in the case of the boost inverter can be lower that the amplitude of the desired output. Then consider the following output voltage:

$$v_{oe} = V_m \sin \omega t = 2V_{s1} \sin \omega t \quad (1)$$

being $V_m$ the desired amplitude and $\omega = 2\pi f$, for $f$ being the desired output frequency. To obtain this voltage, majority of control proposals define as objective the tracking of DC-biased sinusoidal references in the capacitor voltages. These references have the form:

$$v_{1e} = V_{dc} - V_{s1} \sin \omega t \quad (2)$$

$$v_{2e} = V_{dc} + V_{s1} \sin \omega t \quad (3)$$

Considering that Equation (1) is obtained from the difference between Equations (3) and (2), it is easy to note that the same result can be produced using references $v_{1e}$ and $v_{2e}$ with enriched harmonic content as follows:

$$v_{1e} = V_{dc} - V_{s1} \sin \omega t + V_{s1} \cos \omega t + \sum_{n=2}^{\infty} V_{sn} \sin n\omega t + V_{cn} \cos n\omega t \quad (4)$$

$$v_{2e} = V_{dc} + V_{s1} \sin \omega t + V_{s1} \cos \omega t + \sum_{n=2}^{\infty} V_{sn} \sin n\omega t + V_{cn} \cos n\omega t \quad (5)$$

As it was developed in [16], the voltage stress of the semiconductors in the boost inverter is directly related with the shape of the capacitor voltages. Then, that work shows how enforcing a DC-biased half-wave rectified sinusoidal is optimal to alleviate the switching losses improving the
efficient of the converter. However, in that work, the desired behavior is obtained by using two additional switches increasing the number of semiconductors and the required auxiliary circuitry. Then, the concept developed in this study consists of enforcing the desired shape in the capacitor voltages through independent controllers for each boost cell of the inverter simultaneously ensuring an output voltage of high quality. Then, two objectives are defined: (a) generating the adequate voltage references and (b) guaranteeing a robust tracking of these references.

Consider that references are defined to enforce the DC-biased half-wave rectified sinusoidal shape in the capacitor voltages as follows:

\[ v_{1e} = V_{dc} - V_{s1} + 2V_{s1} \sin \omega t [1 + \text{sign}(\sin \omega t)] \]  
\[ v_{2e} = V_{dc} + V_{s1} + 2V_{s1} \sin \omega t [1 + \text{sign}(\sin \omega t)] \]  

Although references Equations (6) and (7) can be easily produced, they can introduce negative effects into the control loop because of the discontinuity of their derivatives. Then, it is proposed to build approximate, but smooth references by adding one or two harmonic components to Equations (2) and (3). To sake of simplicity, analysis is shown only for reference signal \( v_{2e} \), as follows:

\[ v_{2e} = V_{dc} - V_{s1} + V_{c2} + V_{c4} \sin \omega t - V_{c2} \cos 2\omega t \]  
\[ v_{2e} = V_{dc} - V_{s1} + V_{c2} + V_{c4} \sin \omega t - V_{c2} \cos 2\omega t - V_{c4} \cos 4\omega t \]

Figure 2 depicts a comparison between signals obtained from numeric evaluation of Equations (7)–(9). Although a higher number of harmonics can improve the results, solutions given by Equations (8) and (9) are acceptably good. As it can be observed, for Equation (8) the signal remains below the pure sinusoidal by a considerable margin while the difference with respect to the signal Equation (9) is slight, but also important.

Deduction of the amplitude of the added components is constrained to obtain a reference which maximum and minimum values be the same of the pure sinusoidal. A numeric analysis allows deduce that for Equation (8), \( V_{c2} = 0.256V_{s1} \) is optimal, while for Equation (9), \( V_{c2} = 0.36V_{s1} \) and \( V_{c4} = 0.036V_{s1} \) are optimal.

Figure 2. Comparison of possible waveforms for \( v_2 \) constraining the voltage excursion.

The minimum limits of the waveforms in the graphic comparison are the same because \( V_{dc} = 0 \) for Equation (7), \( V_{dc} = 0.75V_{s1} \) for Equation (8) and \( V_{dc} = 0.676V_{s1} \) for Equation (9). Consequently, the value of \( V_{dc} \) into the references must be defined adequately to ensure that this limit be always higher that the instantaneous input voltage.
3. Control of the Inverter

In this work, the adopted control scheme is a classical cascade control structure. The two inner loops, one for each boost cell, are current control loops. Due to its great flexibility and ease of implementation, a sliding mode control strategy was retained. The outer loops, one for each boost cell, are voltage control loops based on saturated PI controllers whose outputs provide an adequate current reference for the inner loop controllers. The need of saturated PI controllers will be justified later. An important step for the success of the adopted control strategy is the generation of appropriate voltage references considering the performance improvements discussed and proposed in Section 2. These voltage references are determined by a harmonic balance method applied to a power balance which constitutes a constraint imposed by the inverter structure. Figure 3 depicts the overall controlled system. Note that the sliding modes controllers are implemented by using simple hysteresis comparators leading to inner controls expressed as:

\[
    u_x = \begin{cases} 
    0 & \text{if } S_x(x) > \delta \\
    1 & \text{if } S_x(x) < -\delta 
    \end{cases} \quad x = 1, 2
\]

where \(\delta\) is a small positive number defined to constrain the maximum switching frequency of the converter and \(S_x(x)\) are the sliding surfaces introduced in a next paragraph. Note that possible variations of the input source voltage is considered in the proposed strategy to modify the DC-component of the voltage references. This aspect is covered by taking measure of \(v_{in}(t)\) and using a low-pass (LP) filter to smooth the effect of ripple content. The cutoff frequency of the LP filter must be selected accordingly with the output frequency (three or four times is enough).

![Figure 3. Block diagram of the complete control proposal: reference-generation and control.](image)

### 3.1. Model of the Inverter

The model of the inverter is deduced from the four circuit structures presented in Figure 4. Introducing the control signals \(u_1\) and \(u_2\), corresponding to \(u_x = 0\) if \(S_{x1}\) is on and \(S_{x2}\) is off and conversely \(u_x = 1\) if \(S_{x1}\) is off and \(S_{x2}\) is on, \(x = 1, 2\), the converter circuit can be modeled by means of the following state equations:

\[
\frac{di_1(t)}{dt} = \frac{1}{L}v_{in}(t) - \frac{1}{L}u_1v_1(t)
\]

(10)

\[
\frac{di_2(t)}{dt} = \frac{1}{L}v_{in}(t) - \frac{1}{L}u_2v_2(t)
\]

(11)

\[
\frac{dv_1(t)}{dt} = \frac{1-u_1}{C}i_1(t) + \frac{1}{r_0C}v_0(t)
\]

(12)

\[
\frac{dv_2(t)}{dt} = \frac{1-u_2}{C}i_2(t) - \frac{1}{r_0C}v_0(t)
\]

(13)
\[ v_o(t) = v_2(t) - v_1(t) \]  

where \( u_1 \) is the control signal of the left-side boost cell and \( u_2 \) is the control signal of the right-side cell.

\[ (a) \quad (b) \quad (c) \quad (d) \]

**Figure 4.** Circuit structures of the boost inverter operating in DS-SMC. (a) Cell 1 state 0, (b) cell 1 state 1, (c) cell 2 state 0 and (d) cell 2 state 1.

### 3.2. Inner Current Control Loops

To enforce a sliding mode regime, the switches of the boost inverter can be operated using two different commutation techniques which have in common the complementarity between the states of the high-side and low-side switches of each boost cell, i.e., when one of them is turned on, the other is turned off. A brief description of features distinguishing these techniques can be summarized below:

- The single surface sliding mode control (SS-SMC) produces two circuit structures and is obtained when the high-side switch of one boost cell is turned on and turned off simultaneously with the low-side switch of the other boost cell and the same for the other switches. In that case, it is possible to reduce the number of control signals. One control signal \( u_1 \) is sufficient to describe the circuit behavior. The corresponding model is obtained replacing \( u_2 \) by \( 1 - u_1 \) in the previous model. The use of this coupled operation of the switches in the control law allows to use only the measurement of the output voltage and both inductor currents to ensure the desired behavior. Furthermore, only one hysteresis comparator enforces the sliding regime tracking the inner reference given by an outer controller which in turn enforces a pure sine-waveform behavior in the output voltage. Although optimal in terms of implementation and computational cost, this commutation method is limited to guarantee a single control objective: provide a high quality output voltage.

- The double surface sliding mode control (DS-SMC) produces four circuit structures and is obtained when the switches of one boost cell commutate completely independent of the switches of the other cell. This signifies that control of the cells is independent although the cells are interconnected through the load and share the connection to the input DC voltage. This is the common way to configure the control loops although it requires measurement of both capacitor voltages and both inductor currents. In addition, one hysteresis comparator is required per boost cell to track the reference given by the outer compensator operating on the capacitor voltage error. Although two
DC biased pure sine-waves are normally used as references, as discussed in the previous section, enriching their harmonic content allows considerably reducing the voltage stress of the switches. Therefore, this control approach is adopted to develop the contribution of this study.

Consider the following sliding surfaces

\[
S(x) = \begin{bmatrix} S_1(x) \\ S_2(x) \end{bmatrix} = \begin{bmatrix} i_1(t) - i_{1e}(t) \\ i_2(t) - i_{2e}(t) \end{bmatrix}
\]

(15)

where \(i_{1e}(t)\) and \(i_{2e}(t)\) are given current signals. By applying the invariance conditions \(S(x) = 0\) and replacing in Equations (9) and (10), the equivalent controls are given by:

\[
1 - u_{i_{1q}} = \frac{v_{in}(t) - L \frac{di_{1e}(t)}{dt}}{v_1(t)} > 0 \Rightarrow \frac{di_{1e}(t)}{dt} < \frac{v_{in}(t)}{L}
\]

(16)

\[
1 - u_{i_{2q}} = \frac{v_{in}(t) - L \frac{di_{2e}(t)}{dt}}{v_2(t)} > 0 \Rightarrow \frac{di_{2e}(t)}{dt} < \frac{v_{in}(t)}{L}
\]

(17)

Replacing Equations (16) and (17) in Equations (12) and (13) and because on the surface \(i_1(t) = i_{1e}(t)\) and \(i_2(t) - i_{2e}(t)\), the following equations are obtained defining the ideal sliding dynamic of the inverter:

\[
\frac{dv_1}{dt} = \frac{1}{C} \left( v_{in} - \frac{v_1}{v_1} \right) + \frac{1}{r_0C} \left( v_2 - v_1 \right) - \frac{L}{Cv_1} \frac{di_{1e}}{dt}
\]

(18)

\[
\frac{dv_2}{dt} = \frac{1}{C} \left( v_{in} - \frac{v_2}{v_2} \right) - \frac{1}{r_0C} \left( v_2 - v_1 \right) - \frac{L}{Cv_2} \frac{di_{2e}}{dt}
\]

(19)

Now, consider that converter variables has incremental variations around one instantaneous operation point \(v_1 = V_1 + \bar{v}_1, v_2 = V_2 + \bar{v}_2, i_{1e} = I_{1e} + \bar{i}_{1e}, i_{2e} = I_{2e} + \bar{i}_{2e}, \frac{di_{1e}}{dt} = \frac{d\bar{i}_{1e}}{dt}, \frac{di_{2e}}{dt} = \frac{d\bar{i}_{2e}}{dt}\), \(v_{in} = V_{in} + \bar{v}_{in}\) and \(r_0 = R_0 + \bar{r}_0\). By following the conventional linearization procedure preserving only first-order terms, it is obtained that:

\[
\frac{d\bar{v}_1}{dt} = W_{11} \bar{i}_{1e} - LW_{12} \bar{i}_{2e} - (CW_{11} W_{12} + b) \bar{v}_1 + b \bar{v}_2 + W_{12} \bar{v}_{in} - W_3 \bar{r}_0
\]

(20)

\[
\frac{d\bar{v}_2}{dt} = W_{21} \bar{i}_{2e} - LW_{22} \bar{i}_{2e} - (CW_{21} W_{22} + b) \bar{v}_1 + b \bar{v}_2 + W_{22} \bar{v}_{in} + W_3 \bar{r}_0
\]

(21)

\[
W_{11} = \frac{1}{Cv_1} \left( V_{in} - LI_{1e} \right) \quad W_{12} = \frac{L}{Cv_1} \quad b = \frac{1}{r_0C} \quad W_{21} = \frac{1}{Cv_2} \left( V_{in} - LI_{2e} \right) \quad W_{22} = \frac{L}{Cv_2} \quad W_3 = \frac{V_{in} - \bar{v}_1}{R_0C}
\]

(22)

By applying the Laplace transform to Equations (20) and (21), Equations (23) and (24) are obtained with which the linear model of whole system can be represented using the block diagram in Figure 5. Transfer functions are defined using the polynomial Equations (25)–(30) considering \(G_1(s) = B_1(s)/A(s), G_2(s) = B_2(s)/A(s), H_{12}(s) = C_1(s)/A(s), H_{21}(s) = C_2(s)/A(s), H_{01}(s) = D_1(s)/A(s), H_{02}(s) = D_2(s)/A(s), H_{41}(s) = E_1(s)/A(s)\) and \(H_{42}(s) = E_2(s)/A(s)\).

\[
V_1(s) = G_1(s) I_{1e}(s) + H_{12}(s) I_{2e}(s) + H_{41}(s) V_{in}(s) - H_{1}(s)R_0(s)
\]

(23)

\[
V_2(s) = G_2(s) I_{2e}(s) + H_{21}(s) I_{1e}(s) + H_{42}(s) V_{in}(s) + H_{2}(s)R_0(s)
\]

(24)

\[
(s) = s^2 + [C(W_{11} W_{12} + W_{21} W_{22}) + b]s + C^2 W_{11} W_{12} W_{21} W_{22} + bC(W_{11} W_{12} + W_{21} W_{22})
\]

(25)

\[
B_1(s) = -L W_{12} s^2 + [W_{11} - L W_{12} (C W_{21} W_{22} + b)]s + W_{11} (C W_{21} W_{22} + b)
\]

(26)

\[
B_2(s) = -L W_{22} s^2 + [W_{21} - L W_{22} (C W_{11} W_{12} + b)]s + W_{21} (C W_{11} W_{12} + b)
\]

(27)
Harmonic balance technique facilitating the synthesis of the simplest controller.

As it can be noted, the parameters of the plant transfer functions $G_1(s)$ and $G_2(s)$, have a high dependence not only on the operation point defined by the input voltage and the load, but also on the shape of the converter waveforms. In order to accurately model the behavior of these parameters, the inductor currents and their derivatives are analyzed in the next section through application of harmonic balance technique facilitating the synthesis of the simplest controller.

![Figure 5. Block diagram of the outer voltage controllers.](image)

### 3.3. Analysis of the Dynamic Behavior using Harmonic Balance

From the analysis in Section 2, the reference required to enforce the desired shape in the capacitor voltages has the following form:

\[
v_{1e} = V_{dc} - V_{s1} \sin \omega t + V_{c2} \cos 2\omega t + V_{c4} \cos 4\omega t
\]

\[
v_{2e} = V_{dc} + V_{s1} \sin \omega t + V_{c2} \cos 2\omega t + V_{c4} \cos 4\omega t
\]

The corresponding time derivatives are given by:

\[
\frac{dv_{1e}}{dt} = -\alpha V_{s1} \cos \omega t - 2\alpha V_{c2} \sin 2\omega t - 4\alpha V_{c4} \sin 4\omega t
\]

\[
\frac{dv_{2e}}{dt} = \alpha V_{s1} \cos \omega t - 2\alpha V_{c2} \sin 2\omega t - 4\alpha V_{c4} \sin 4\omega t
\]

Now, suppose that the stationary periodic behavior of the inductor currents can be approximated, in a satisfactory way by means of the following waveforms and its derivatives:

\[
i_{1e} = I_{dc} - I_{s1} \sin \omega t - I_{c1} \cos \omega t + \sum_{n=2}^{4} (-1)^{n+1} [I_{sn} \sin n\omega t + I_{cn} \cos n\omega t]
\]

\[
i_{2e} = I_{dc} + I_{s1} \sin \omega t + I_{c1} \cos \omega t - \sum_{n=2}^{4} [I_{sn} \sin n\omega t + I_{cn} \cos n\omega t]
\]
\[
\frac{di_{c1}}{dt} = a_1l_{c1} \sin \omega t - a_1l_{c1} \cos \omega t + \omega \sum_{n=2}^{4} n\left[(-1)^n l_{c1} \sin n \omega t + (-1)^{n+1} l_{c1} \cos n \omega t \right]
\] (37)

\[
\frac{di_{c2}}{dt} = -a_1l_{c1} \sin \omega t + a_1l_{c1} \cos \omega t + \omega \sum_{n=2}^{4} n\left[l_{c1} \sin n \omega t - l_{c1} \cos n \omega t \right]
\] (38)

On the other hand, expressions Equations (18) and (19) can be interpreted as power balance constraints for the boost inverter cells. Then, they can be rewritten as follows:

\[
Li_{c1} \frac{di_{c1}}{dt} + Cv_{c1} \frac{dv_{c1}}{dt} - \left(v_{in} i_{c1} + \frac{v_{in} \omega}{r_0} \right) = 0
\] (39)

\[
Li_{c2} \frac{di_{c2}}{dt} + Cv_{c2} \frac{dv_{c2}}{dt} - \left(v_{in} i_{c2} - \frac{v_{in} \omega}{r_0} \right) = 0
\] (40)

Summing Equations (39) and (40), the power balance equation for the complete inverter can be written as:

\[
L\left(i_2 \frac{di_{c2}}{dt} + i_3 \frac{di_{c3}}{dt}\right) + C\left(v_{c2} \frac{dv_{c2}}{dt} + v_{c3} \frac{dv_{c3}}{dt}\right) - \left[v_{in}(i_{c1} + i_{c2}) - \frac{v_{in} \omega}{r_0}\right] = 0
\] (41)

By replacing Equations (31)–(38) into Equation (41) and applying the harmonic balance technique, it is obtained a set of nonlinear algebraic equations, whose unknowns are the amplitudes of the harmonic components of the currents. It can be compactly written as:

\[
F_B(i_{dc}, i_{s1}, i_{s2}, i_{s3}, i_{s4}, i_{c1}, i_{c2}, i_{c3}, i_{c4}, v_{dc}, v_{s1}, v_{s2}, v_{c1}, v_{c2}, v_{c3}) = 0
\] (42)

where the components of \( F_B \) are expressed by:

\[
F_{dc} = 2V_{in}i_{dc} - \frac{2V_{dc}^2}{r_0}
F_{s1} = \omega L\left(i_{s1}^2 - i_{s1}^2 + 4i_{s2}i_{s2} + 2i_{s1}i_{s3} + 2i_{s1}i_{s4} - 2i_{s2}i_{s4} - 2i_{s2}i_{s4}\right) + \omega C\left(V_{c3}^2 - 4V_{dc}V_{c2} - 2V_{dc}V_{c4}\right) + 2Vi_{in}l_{c2}
F_{s2} = 2\omega L\left(i_{s1}i_{s3} - 2i_{s2}i_{s2} + 2i_{s1}i_{s3} + 2i_{s3}i_{s1} - 2i_{s3}i_{s4} - 2i_{s4}i_{s3}\right) - \left(-2V_{in}i_{c2} + \frac{2V_{c3}^2}{r_0}\right)
F_{s3} = 2\omega L\left(i_{s3}^2 - i_{s2}^2 - 2i_{s3}i_{s3} + 2i_{s3}i_{s3} + 4i_{s4}i_{c4}\right) + 2\omega C\left(-V_{c2}^2 - 4V_{dc}V_{c4}\right) + 2Vi_{in}l_{c4}
F_{c1} = 4\omega L\left(i_{c2}i_{c2} - i_{c3}i_{c1} - i_{c4}i_{c1} + 2i_{c4}i_{c4}\right) + 2Vi_{in}l_{c4}
F_{c2} = 3\omega L\left(i_{s3}^2 - i_{s2}^2 + 2i_{s4}i_{c4} - 2i_{s2}i_{c4}\right) - 6\omega CV_{c2}V_{c4}
F_{c3} = 6\omega L\left(i_{s3}i_{c3} + i_{s4}i_{c4} + i_{c2}i_{c2}\right)
F_{c4} = 7\omega L\left(-i_{c3}i_{c4} + i_{c4}i_{c4}\right)
F_{c5} = 7\omega L\left(-i_{s3}i_{c4} - i_{c4}i_{c4}\right)
F_{c6} = 4\omega L\left(i_{c2}^2 - i_{c4}^2\right) - 4\omega CV_{c4}^2
F_{c7} = 8\omega L_{c4}i_{c4}
\] (43)

Numerical evaluation of this nonlinear equation system for the entire range of \( v_{in} \) and \( r_0 \) allows to obtain the shape of the inductor currents and their derivatives which beside to the desired voltage references allow to analyze the dynamic behavior of the system. Solutions are obtained by using the function \textit{lsqnonlin} of MATLAB considering the input–output ranges listed in Table 1 and parameters in Table 3. For the subsequent analysis, recall that harmonic components of the capacitor voltages for a given amplitude \( V_m \) of the desired output voltage \( v_0(t) \) are expressed by \( V_{s1}0.5V_m, V_{s2}0.18V_m \) and \( V_{c4}0.018V_m \). The dC component of the voltage references is computed some volts higher than the minimum permissible value: \( V_{dc} = V_{in} + 0.338V_m + V_{+} \).
Table 1. Range of operation of the converter used for numeric analysis.

| Parameter                              | Symbol | Minimum   | Maximum   | Unities |
|----------------------------------------|--------|-----------|-----------|---------|
| Input voltage                          | \( v_{in} \) | 125%–25% | 125 + 25% | V       |
| Output voltage amplitude (Std. 1)      | \( v_m \) | 120 \( \sqrt{2} \) | V         |         |
| Output frequency (Std. 1)              | \( f \) | 60        | Hz        |         |
| Output power (Std. 1)                  | \( P_o \) | 24        | 240       | W       |
| Resistive load (Std. 1)                | \( r_o \) | 600       | 60        | \( \Omega \) |
| Output voltage amplitude (Std. 2)      | \( v_m \) | 220 \( \sqrt{2} \) | V         |         |
| Output frequency (Std. 2)              | \( f \) | 50        | Hz        |         |
| Output power (Std. 2)                  | \( P_o \) | 22        | 220       | W       |
| Resistive load (Std. 2)                | \( r_o \) | 2200      | 220       | \( \Omega \) |
| Parameter Symbol Minimum Maximum Unities |

By evaluating the periodic terms of Equations (16) and (17), it is possible to observe that their values are always lower than any value of the input voltage in the range of operation of the converter. Figure 6 shows three cycles of these terms evaluated for 30 coordinates into the range of input voltage and output load including extreme values. A coincidence of the produced waveforms around zero is recognized. From these results, it is easy to conclude, that operating with constant voltage and load, this condition will never be violated. However, during transient response to input voltage or power load disturbances, the value of the derivative can considerably increase enforcing the loss of the sliding regime. As we will see later, maintaining the system in the sliding regime can be ensured saturating the derivative of the currents.

![Figure 6](image_url)

**Figure 6.** Evaluation of three cycles of the waveforms of the inductor voltages for the entire range of input voltage at full load. (a) Standard 220 V @ 50 Hz and (b) standard 120 V @ 60 Hz.

Figure 7 depicts the inductor current waveforms evaluated for the same 30 coordinates into the set of operation conditions of the converter. As it can be observed, when the inductor current of one cell takes negative values, the current in the other one takes positive values. In some few cases and for short intervals close to the end of each half-period, both currents can take negative values simultaneously. A coincidence around zero is also observed for this variable.
Figure 7. Evaluation of three cycles of the waveforms of the inductor currents for the entire ranges of input voltage and output load. (a) Standard 220 V @ 50 Hz and (b) standard 120 V @ 60 Hz.

Figure 8 shows the capacitor voltage waveforms evaluated for the whole range of input voltage of the converter. Please note that impose these voltage waveforms is one of the control objectives and then the shape of the voltages must be independent of the power load. It is possible to observe how independent of the output frequency, the waveforms show coincidence at the end of each half-cycle taking values in the vicinity of $2V_{in}$.

![Figures 7 and 8](image)

Figure 8. Evaluation of three cycles of the waveforms of the capacitor voltages for the entire range of input voltage at full load. (a) Standard 220 V @ 50 Hz and (b) standard 120 V @ 60 Hz.

From the results of the previous analysis, it seems to be reasonable to evaluate the parameters of the polynomial Equations (25) and (27) to obtain $G_2(s)$ around the average point Equation (44) which results in the reference current to capacitor voltage transfer functions given by Equation (45).

\[
\begin{align*}
\left(i_{1r}, i_{2r}, v_1, v_2, L \frac{di_{1r}}{dt}, L \frac{di_{2r}}{dt}, v_{in}, r_0\right) &= (0, 0, 2V_{in}, 2V_{in}, 0, 0, V_{in}, R_0) \\
G_1(s) &= \frac{s+b}{2C(s+2b)s} \\
G_2(s) &= \frac{s+b}{2C(s+2b)s}
\end{align*}
\]  \hspace{1cm} (44)  \hspace{1cm} (45)

The resulting model shows that system dynamics is not asymptotically stable nor unstable. Around the linearization point, an integral effect can be observed, but this effect diminishes as we move away from it. The following as conclusions can be considered for the controller design stage.

1. Without an outer loop, having that the average value of the currents is positive, the voltages of the capacitors will increase until the permitted physical limits;
2. Using a proportional controller, the stability is ensured, but the references cannot be accurately tracked. The error is greater for instantaneous operation points furthest from linearization point;
3. A proportional-integral (PI) controller with adequate parameters can provide an accurate tracking of the periodic references for all operation points;
4. The resulting transfer functions in Equation (45) show no effect of the input and output voltages but include the term \( b \) which represents the influence of the power load.

### 3.4. Outer Voltage Controllers

The tracking of the voltage references is guaranteed by the outer loops with PI voltage compensators defined by:

\[
\begin{align*}
    s_x(t) &= \text{sat}_{u_0}\left\{ K_p \left[ \frac{d(v_x(t) - v_{xe}(t))}{dt} + \alpha (v_x(t) - v_{xe}(t)) \right] \right\} \\
    i_{xe}(t) &= \int_{-\infty}^{t} s_x(\tau) d\tau \quad x = 1, 2
\end{align*}
\]

where \( \text{sat}_{u_0}(x) \) is the classical symmetrical saturation function [17] having \( u_0 = \frac{v_m(t)}{L} \) defining its limits. \( K_p \) and \( \alpha \) are positive design parameters, \( K_p \) being the proportional gain and \( \alpha K_p \) the integral gain. When the signal \( s_x(t) \) does not saturate, the controller is a classical PI controller whose expression is:

\[
i_{xe}(t) = K_p (v_x(t) - v_{xe}(t)) + \alpha K_p \int_{-\infty}^{t} (v_x(\tau) - v_{xe}(\tau)) d\tau, \quad x = 1, 2
\]

The presence of saturation function ensures that the overall controlled system is asymptotically stable. This can be deduced from the stability result developed in the previous section, simply by noting that functions \( a_x(t), x = 1, 2 \), remain positive if condition Equation (15) is satisfied, that is, if:

\[
\frac{di_{xe}(t)}{dt} < \frac{v_{in}(t)}{L}, \quad x = 1, 2
\]

Equation (15) being also a necessary condition for the existence of a sliding regime. In such situation, for all positive \( K_p \) and \( \alpha \), we will have:

\[
\lim_{t \to \infty} v_1(t) = v_{1e}(t) \quad \text{and} \quad \lim_{t \to \infty} v_2(t) = v_{2e}(t)
\]

For ease implementation of the proposed controller, we can remark that an expression of the outer control can be formulated with a saturation function whose limit is constant and equal to a positive real number \( s_0 \) (i.e., independent of time) chosen to facilitate the controller implementation. An alternate expression with such a property could be:

\[
\begin{align*}
    s_x(t) &= \frac{v_{xe}(t)}{L} \text{sat}_{s_0}\left\{ \frac{Ls_p}{L_p} K_p \left[ \frac{d(v_x(t) - v_{xe}(t))}{dt} + \alpha (v_x(t) - v_{xe}(t)) \right] \right\} \\
    i_{xe}(t) &= \int_{-\infty}^{t} s_x(\tau) d\tau \quad x = 1, 2
\end{align*}
\]

Figure 9 represents the block-diagram of the proposed saturated PI controller.

To simplify the controller structure and then its implementation, if there exists a value \( v_{in_{\text{min}}} > 0 \) such that for all \( t \), \( v_{in}(t) > v_{in_{\text{min}}} \), it is possible to drop the measurement of \( v_{in}(t) \) and replace it by \( v_{in_{\text{min}}} \) in the control expression. It is also possible to use a non-saturated PI controller if the converter was adequately designed to track the reference signals of interest (i.e., in a way guaranteeing that the control never saturates).

To end with the outer loop, the choice of constants \( K_p \) and \( \alpha \) have an influence on the transient behavior of the controlled system, but asymptotic stability is always ensured. Even if asymptotic stability is a necessary condition, it is not sufficient in practice. A good performance level is often needed. The parameters \( K_p \) and \( \alpha K_p \) can be selected as done classically for a nonsaturated PI controller. However, it is important to remark that while the stability will be preserved, the performance associated
with such a choice will only be guaranteed in the zone of linearity of the saturated PI controller. When the controller will saturate, except stability, no performance level can be guaranteed.

\[
\begin{align*}
&\text{Proportional gain } K_p \\
&\text{Integral gain } aK_p \\
&\text{Saturation limit } s_0 \\
&\text{Hysteresis band width } 2b \\
&\text{Cutoff frequency LPF } f_{c1}
\end{align*}
\]

### Table 2. Control parameters used in simulations.

| Parameter               | Symbol | Value (60 Hz) | Value (50 Hz) | Unities |
|-------------------------|--------|---------------|---------------|---------|
| Proportional gain       | \(K_p\) | 0.3           | 0.2           |         |
| Integral gain           | \(aK_p\) | \(25 \times 10^{-6}\) | 20 \times 10^{-6} |         |
| Saturation limit        | \(s_0\) | \(500 \times 10^3\) | 500 \times 10^3 | A/s     |
| Hysteresis band width   | \(2b\) | 2             | 2             | A       |
| Cutoff frequency LPF    | \(f_{c1}\) | 240           | 200           | Hz      |

### Table 3. Parameters of the power converter in simulations.

| Element   | Manuf./Reference | Parameter               | Symbol | Value | Unities |
|-----------|------------------|-------------------------|--------|-------|---------|
| Capacitors | KEMET [19]       | Capacitance             | C      | 9     | \(\mu F\) |
|           |                   | Series resistance       | \(R_C\) | 8.3   | m\(\Omega\) |
| Inductors | Bourns [20]      | Inductance              | \(L\)  | 120   | \(\mu H\) |
|           |                   | Series resistance       | \(R_L\) | 28    | m\(\Omega\) |
| MOSFETs   | ROHM [21]        | On-resistance           | \(R_M\) | 196   | m\(\Omega\) |

In both simulation tests, five points are enforced to assess the stationary and transient behavior. Selected conditions and time intervals are listed in Table 4. Sudden transitions are enforced during the load changes while ramp type transitions with intervals of 3 ms are applied for input voltage changes.
4.1. Simulation Test 1 (American Standard 120 V @ 60 Hz)

Figure 10 presents the waveforms at the output of the converter (voltage and current), the capacitor voltages and the inductor currents for the simulation test 1. As it can be observed, the output signal accurately track the high quality sinusoidal in both stationary and transient regimes. After disturbances, the AC component of the capacitor voltages remains unchanged while its average value adapts to the input voltage. Table 5 summarizes the obtained THD (lower than 1%) and RMS error (lower than 0.2%) demonstrating the high performance of proposed control in the five selected operation points.
Table 5. Output voltage quality for simulation test 1 (120 V @ 60 Hz).

| Convention          | Time Interval | THD (%) | RMS Error (%) |
|---------------------|---------------|---------|---------------|
| Operation condition 1 | 0.10–0.15 s   | 0.70    | 0.06          |
| Operation condition 2 | 0.15–0.20 s   | 0.70    | 0.06          |
| Operation condition 3 | 0.20–0.25 s   | 0.71    | 0.07          |
| Operation condition 4 | 0.25–0.30 s   | 0.71    | 0.08          |
| Operation condition 5 | 0.30–0.35 s   | 0.66    | 0.10          |

Figure 11 shows a comparison between the DS–SMC approach developed in this work and the SS-SMC approach developed in [4]. As it can be noted, the voltage of the capacitors which is the same voltage applied to open semiconductors in each boost cell is always lower for the DS-SMC. It is relevant to mention that two features of the proposed control are responsible of the improvement: (a) the harmonic content included in the capacitor voltages and (b) their average component. The DC component cannot be accessed using the SS-SMC approach while using the proposed DS-SMC this component allows to enforce the minimum value of the output capacitors to be almost equal to the input voltage. In this simulation test $V_{dc} = V_{in} + 0.338V_m + V_+$, being $V_+$ settled to 5 V.

Figure 12. Simulated semiconductor voltages comparing SS-SMC and DS-SMC for simulation test 1.

4.2. Simulation Test 2 (European Standard 220 V @ 50 Hz)

Figure 13 presents the waveforms at the converter for the simulation test 2. It is possible to confirm that the output signal accurately track the high quality sinusoidal. Table 6 summarizes the obtained THD and RMS error which show values lower than 1% and 0.2%, respectively. It is worth mentioning that the required voltage gain increases around 50% without affecting the performance of the control which use the same parameters.

Table 6. Output voltage quality for simulation test 2 (220 V @ 50 Hz).

| Convention          | Time Interval | THD (%) | RMS Error (%) |
|---------------------|---------------|---------|---------------|
| Operation condition 1 | 0.10–0.16 s   | 0.76    | 0.08          |
| Operation condition 2 | 0.16–0.22 s   | 0.76    | 0.10          |
| Operation condition 3 | 0.22–0.28 s   | 0.76    | 0.08          |
| Operation condition 4 | 0.28–0.34 s   | 0.77    | 0.09          |
| Operation condition 5 | 0.34–0.40 s   | 0.74    | 0.11          |
Equal to the previous test, the DS–SMC and SS–SMC approaches were compared. Again, the voltage applied to semiconductors is always lower for the DS–SMC. The expression $V_{dc} = V_{in} + 0.338V_m + V_+$ being $V_+$ settled to 5 V is used to define input voltage. In addition, similar to the previous case, the alleviation of the semiconductor voltage stress is at least of 30 V and becomes up to 100 V. A more accurate analysis is presented in the next subsection.

4.3. Semiconductor Voltage Stress Comparison

A further analysis was done by reviewing the maximum, minimum and average semiconductor voltage stress for inverter operating with the two studied standards using the same simulations producing Figures 11 and 13. In addition to the two methods compared in these figures, the proposed control without adding the harmonic components in the voltage references is also assessed. In Table 7, the minimum voltage corresponds with intervals in which the input voltage is minimum (125 V–25%), the maximum voltage corresponds to the intervals in which the input voltage is maximum (125 V + 25%) and the average is computed considering the complete simulation interval for both standards.
or he boost cells to alleviate semiconductors considering the complete simulation interval
(b) minimize the required voltage gain in the boost cells to alleviate semiconductor voltage stress.
The objectives are accomplished by means of two independent multiloop controllers involving an inner
loop which is also an innovative feature of the proposed control scheme. The obtained
technique. A PI controller with saturation of the output derivative allowed to ensure the sliding regime
the converter was developed to obtain a simple model of its dynamics by using the harmonic balance
further reduce the required gain in the converter cells. A complete study of the stationary behavior of
the average value of the capacitor voltages, an adaptive feed-forward loop was integrated helping to
the tracking of harmonic enriched references. Additionally, having a degree of freedom to modify
loop of sliding mode control implemented using hysteresis comparators and PI compensators ensuring
the capacitors are enforced to have additional optimal values of double and fourth harmonic terms.

Figure 13. Simulated semiconductor voltages comparing SS-SMC and DS-SMC for simulation test 2.

| Control Method                  | Standard 1 (120 V @ 60 Hz) | Standard 1 (220 V @ 50 Hz) |
|--------------------------------|----------------------------|----------------------------|
|                               | Min (V) | Max (V) | Avg (V) | Min (V) | Max (V) | Avg (V) |
| SS-SMC [4]                    | 136     | 418     | 254     | 120     | 533     | 290     |
| DS-SMC (Sine references)      | 97      | 331     | 209     | 97      | 472     | 285     |
| DS-SMC (Modified references)  | 97      | 331     | 182     | 97      | 472     | 235     |

Results demonstrate how the voltage stress of the semiconductors reduces considerably by
employing the DS-SMC proposed in this study (Separate voltage control loops minimizing the
DC-bias of the references) even without additional harmonic components into the voltage references.
Beyond that, results also demonstrate conclusively how the addition of the two harmonic components
in the references further improve this feature.

5. Conclusions

In this study, the sliding mode control technique was effectively applied to accomplish two
main objectives in the operation of the boost inverter: (a) provide a high quality output voltage and
(b) minimize the required voltage gain in the boost cells to alleviate semiconductor voltage stress.
Different from all previously published works related to the control of this converter, the voltage of
the capacitors are enforced to have additional optimal values of double and fourth harmonic terms.
The objectives are accomplished by means of two independent multiloop controllers involving an inner
loop of sliding mode control implemented using hysteresis comparators and PI compensators ensuring
the tracking of harmonic enriched references. Additionally, having a degree of freedom to modify
the average value of the capacitor voltages, an adaptive feed-forward loop was integrated helping to
further reduce the required gain in the converter cells. A complete study of the stationary behavior of
the converter was developed to obtain a simple model of its dynamics by using the harmonic balance
technique. A PI controller with saturation of the output derivative allowed to ensure the sliding regime
of the inner loop which is also an innovative feature of the proposed control scheme. The obtained
THD is lower than 0.8% and the regulation of the RMS value is lower than 0.2% in the entire range of
operation of the converter for both standards used as case study. The alleviation of the semiconductor
voltage stress is very important also for both analyzed standards.
From the results of the present work, a new control scheme is being developed using a multiple input multiple output perspective of the problem, this allowing a better action on the coupling dynamics of the boost cells. Prospective work involves experimental validation using a laboratory prototype.

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