Fast Successive-Cancellation Decoding of Polar Codes With Sequence Nodes

Yang Lu*, Ming-Min Zhao*, Member, IEEE, Ming Lei, Member, IEEE, and Min-Jian Zhao, Senior Member, IEEE

Abstract—Due to the sequential nature of the successive-cancellation (SC) algorithm, the decoding of polar codes suffers from significant decoding latencies, which hinders its application in low-latency communication scenarios. Fast SC decoding is able to speed up the SC decoding process by implementing parallel decoders at the intermediate levels of the SC decoding tree for some special polar constituent subcodes (special nodes) with specific information and frozen bit patterns. To further improve the parallelism of SC decoding, this paper presents a new class of special nodes composed of a sequence of rate one or single-parity-check (SR1/SPC) nodes, which can be easily found especially in high-rate polar code and is able to envelop a wide variety of existing special node types. Then, we analyze the parity constraints associated with the SC decoding algorithm. Due to the polarization theory, polar codes under SC decoding are theoretically proved to have capacity-achieving capabilities under binary-input memoryless channels [2]. Due to the capacity-achieving error-correction performance and low-complexity successive cancellation (SC) based algorithm, polar codes are adopted in the control channel of the enhanced mobile broadband (eMBB) use case in the latest 5G cellular standard [3]. However, there are two main drawbacks associated with the SC decoding algorithm. First, according to the polarization theory, polar codes under SC decoding can achieve the channel capacity only when the code length tends toward infinity. As a result, SC decoding falls short in providing a reasonable error-correction performance for practical moderate code lengths. Second, the sequential bit-by-bit nature of SC decoding leads to high decoding latency and low throughput in terms of hardware implementation, which hinders its application in low-latency communication scenarios.

The first drawback mentioned above is mainly due to the fact that SC decoding is suboptimal with respect to maximum-likelihood (ML) decoding. To partially compensate for this sub-optimality, SC list (SCL) decoding algorithm was presented in [4]. By maintaining a list of candidate codewords, the SCL decoder is able to reduce the performance gap between SC and ML decoding at the cost of increased implementation complexity [5]. By concatenating polar codes with simple cyclic redundancy check (CRC), it was observed that the performance of the SCL decoder can be significantly improved [6]. With a large list size, the decoding performance provided by the CRC-aided SCL (CA-SCL) decoder can approach that of the ML decoder, which makes polar codes competitive with the other state-of-the-art channel codes, such as low-density parity-check (LDPC) and turbo codes [7].

The second drawback stems from the sequential nature of SC decoding. To tackle this issue, many fast decoding schemes have been developed for polar codes [8], [9], [10], [11], [12], [13], [14], [15], [16], [17]. The main idea behind these schemes is to decode polar constituent subcodes (special nodes) at the intermediate levels of the SC or SCL decoding tree, instead of the leaf nodes. As for the intermediate decoders tailored for the special nodes, they usually have much higher degrees of parallelism while providing promising performance, making them compatible with the plain SC decoding. Since these node-based decoding schemes highly depend on the SC decoding process, they inevitably inherit the sequential nature. Although true parallelism is unrealistic, node-based fast SC decoding schemes are still promising as they are able to yield the same error-correction performance as SC decoding, with much lower decoding latency. In particular, it was shown in [8] that ML decoding of the intermediate nodes can be employed to parallelize the SC decoding. However, this scheme is only suitable for nodes with short lengths. On the contrary, the work [9] proposed a low-complexity simplified SC (SSC) decoding algorithm for two types of special nodes with certain information and frozen bit patterns, i.e., rate-zero (Rate-0) and rate-one (Rate-1) nodes that contain no information and frozen bit, respectively. In particular, the ML codeword of a Rate-0
node is always an all-zero vector, while the ML codeword of a Rate-1 node is the hard-decision output of the log-likelihood ratio (LLR) vector at the node root. Likewise, single-parity-check (SPC) and repetition (REP) nodes along with their fast decoding techniques were proposed in [10], which is known as the fast SSC (FSSC) decoding algorithm. Furthermore, the work [11] advanced the studies in [9] and [10] by proposing fast decoders for five new types of special nodes, namely the Type I-V nodes, which further reduces the SC decoding latency. In [12], a generalized REP (G-REP) node and a generalized parity-check (G-PC) node were proposed to reduce the latency of SC decoding even further. Moreover, the identification and utilization of the aforementioned special nodes were also extended to SCL decoding [13], [14], [15], [16]. However, all these works require the design of a separate decoder for each class of nodes, which inevitably increases the implementation complexity. Recently, a class of more general nodes, i.e., the sequence Rate-0/REP (SR0/REP) node, was proposed in [17] to provide a unified description of most of the existing low-rate special nodes. With the introduction of fast SC and SCL decoding algorithms for SR0/REP nodes, higher degrees of parallelism can be achieved without degrading the error-correction performance [17], [18].

This work is an extension of our work in [1], where a new fast SC decoding algorithm was initially proposed. In this paper, we further present a simplification technique which incurs almost no error-correction performance loss. Our contributions are summarized as follows. First, a new class of sequence nodes is introduced, which is composed of a sequence of Rate-1 or SPC (SR1/SPC) nodes, and thus provides a unified description of a wide variety of existing high-rate special nodes. The proposed SR1/SPC node is typically found at higher levels of the decoding tree, thus a higher degree of parallelism can be exploited as compared to the existing special nodes. Then, we investigate the impact of the frozen bits contained in the proposed SR1/SPC node, which leads to two types of parity constraints that are imposed on the decoded codeword. Furthermore, inspired by ML decoding, a simple and efficient decoding algorithm is proposed to decode the proposed SR1/SPC node, which can achieve quasi-ML performance with higher degree of parallelism. By combining the proposed SR1/SPC nodes with other types of special nodes, such as the SR0/REP nodes [17], we show that the overall decoding latency can be reduced by 43.8% and 62.9% as compared to the state-of-the-art SC decoder and the renowned FSSC decoder [10], respectively.

The remainder of this paper is organized as follows. Section II reviews the backgrounds on polar codes, SC decoding, and fast SC decoding techniques. In Section III, we introduce the SR1/SPC node, and then analyze the induced parity constraints. Fast SC decoding of the proposed SR1/SPC node is presented in Section IV. Section V provides simulation results to evaluate the decoding latency, complexity and performance. Finally, conclusions are drawn in Section VI.

Notations: Scalars, vectors, and matrices are respectively denoted by lower case, boldface lower case, and boldface upper case letters. For an arbitrary vector \( \mathbf{a} \), \( a[i : k : j] \) represents a subvector of \( \mathbf{a} \) which is constructed by \( \{ a[i], a[i + 1], \ldots, a[i + m]\} \), where \( k \) is the step size and \( m = \lfloor (j - i)/k \rfloor \). If \( k = 1 \), \( a[i : k : j] \) is simply written as \( a[i:j] \). \( \text{sgn}(a) \) denotes the sign of a scalar \( a \) and \( \min(a) \) returns the minimum element in a vector \( a \). Besides, \( \mathbf{I}_N \) and \( \mathbf{0}_N \) denote the \( N \times N \) identity matrix and the \( N \times N \) all-zero matrix, respectively. For a matrix \( \mathbf{A} \), \( (\mathbf{A})_i \) represents its \( i \)-th column vector. In addition, \( \{\cdot\} \) denotes a set, \( [\cdot] \) and \( [\cdot] \) denote the round-up and round-down operations, respectively. \( \oplus \) denotes the bitwise XOR operation and \( \otimes \) denotes the Kronecker product. \( A^\otimes n \) denotes the \( n \)-th Kronecker power of \( A \).

II. Preliminaries

A. Polar Codes

A polar code with code length \( N = 2^n \) and information length \( K \) can be represented as \( P(N, K) \), which has a code rate of \( R = K/N \). The transmitted polar codeword \( \mathbf{x} = (x[1], x[2], \ldots, x[N]) \) is obtained by \( \mathbf{x} = \mathbf{u} \mathbf{G}_N \), where \( \mathbf{u} = (u[1], u[2], \ldots, u[N]) \) is the message vector and \( \mathbf{G}_N = \mathbf{F}^{\otimes n} \) is the generator matrix with \( \mathbf{F} = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \) being the base polarizing matrix. The message vector \( \mathbf{u} \) is constructed by choosing \( K \) bit-channels with high reliability to transmit information bits, while the remaining \( N-K \) bits are frozen to some fixed values (usually set to 0). With the help of an indicator vector \( \mathbf{e} = (c[1], c[2], \ldots, c[N]) \), we are able to distinguish information and frozen bit-channels according to

\[
c[k] = \begin{cases} 
1, & \text{if } k \in \mathcal{A} \\
0, & \text{if } k \in \mathcal{A}^c,
\end{cases}
\]

where \( \mathcal{A} \) and \( \mathcal{A}^c \) denote the sets of information and frozen bits indices, respectively, which are both known to the encoder and decoder. The codeword vector \( \mathbf{x} \) is then modulated and transmitted over the channel. Throughout this paper, we consider binary phase shift keying (BPSK) modulation and additive white Gaussian noise (AWGN) channel.

B. SC Decoding

SC decoding originated in [2] is a greedy search algorithm for decoding polar codes, and only the best decoding result is reserved in each decoding step. The decoding procedure of SC can be interpreted as a binary tree search process that starts from the root node to the leaf node and from the left branch to the right. At the \( p \)-th \((0 \leq p \leq n)\) level of the decoding tree, each parent node, referred as \( \mathcal{N}_p^i \), has a left child node \( \mathcal{N}_{p-1}^{2i-1} \) and a right child node \( \mathcal{N}_{p-1}^{2i} \), where \( 1 \leq i \leq 2^{n-p} \). There are two types of messages, i.e., the soft LLRs \( \alpha_p^i[1 : 2^p] \) that are propagated from the parent node to their child nodes, and the hard codeword \( \beta_p^i[1 : 2^p] \) that is propagated from the child nodes to their parent node in return. The \( 2^{p-1} \) LLRs of the left child node \( \alpha_p^{2i-1}[1 : 2^{p-1}] \) and those of the right child node \( \alpha_p^{2i}[1 : 2^{p-1}] \) can be respectively obtained by

\[
\alpha_p^{2i-1}[k] = \text{sgn}(\alpha_p^i[k]) \cdot \text{sgn}(\alpha_p^i[k + 2^{p-1}]) \cdot \min([\alpha_p^i[k], \alpha_p^i[k + 2^{p-1}]]),
\]

\[
\alpha_p^{2i}[k] = \alpha_p^i[k + 2^{p-1}] + (1 - 2\beta_p^{2i-1}[k])\alpha_p^i[k].
\]
Besides, the hard codeword of $N_p^j$, i.e., $\beta_p^j[1 : 2^p]$, is calculated based on the hard codewords of $N_{p-1}^{2^{j-1}}$ and $N_{p-1}^{2^j}$ as follows:

$$\beta_p^j[k] = \begin{cases} 
\beta_{p-1}^{j-1}[k] \oplus \beta_{p-1}^j[k], & \text{if } 1 \leq k \leq 2^{p-1}, \\
\beta_{p-1}^{j-1}[k], & \text{otherwise}
\end{cases}, \quad (4)$$

at the leaf level $p = 0$, bit $u[k]$ can be estimated by performing hard decision on $\alpha_0^j[1]$ according to

$$\hat{u}[k] = \beta_0^j[1] = \text{HD}(\alpha_0^j[1]) = \begin{cases} 
\frac{1 - \text{sgn}(\alpha_0^j[1])}{2}, & \text{if } k \in A_c, \\
0, & \text{if } k \in A_c^c.
\end{cases} \quad (5)$$

where $\hat{u}[k]$ is the estimate of $u[k]$ and HD(·) is the hard decision function.

### C. Fast SC Decoding

The sequential nature of SC decoding, i.e., each bit estimate depends on all previous ones, results in high decoding latency. The decoding speed can be accelerated by implementing decoders that can output multiple bits in parallel without traversing the bottom of decoding tree. Based on this idea, the work [8] presented a highly parallel ML decoder to estimate the codeword of node $N_p^j$, i.e.,

$$\beta_p^j[1 : 2^p] = \arg \max_{\beta_p^j[1 : 2^p] \in \mathcal{B}_p^j} \sum_{k=1}^{2^p} (-1)^k \beta_p^j[k] \alpha_p^j[k], \quad (6)$$

where $\mathcal{B}_p^j$ is the set of all codewords associated with node $N_p^j$. However, the complexity of solving (6) can be very high, especially for nodes with long lengths. Therefore, the work [10] proposed the FSSC decoding algorithm, based on the discovery that the calculation of (6) can be significantly simplified for some nodes with special information and frozen bit patterns. In particular, four types of special nodes, i.e., Rate-0, Rate-1, REP and SPC, are considered in the FSSC decoder, and their structures are described as follows:

- **Rate-0**: all bits are frozen bits, $c = \{0, 0, \ldots, 0\}$.
- **Rate-1**: all bits are information bits, $c = \{1, 1, \ldots, 1\}$.
- **REP**: all bits are frozen bits except the rightmost one, $c = \{0, 0, \ldots, 1\}$.
- **SPC**: all bits are information bits except the leftmost one, $c = \{1, 0, \ldots, 1\}$.

Moreover, the work [11] further improved the FSSC decoding speed by investigating five additional special nodes along with their efficient SC decoders. The five additional special nodes are summarized as follows:

- **Type I**: all bits are frozen bits except the rightmost two, $c = \{0, 0, 0, 1, 1\}$.
- **Type II**: all bits are frozen bits except the rightmost three, $c = \{0, 0, 0, 0, 0, 1, 1\}$.
- **Type III**: all bits are frozen bits except the leftmost two, $c = \{0, 0, 0, 1\}$.
- **Type IV**: all bits are information bits except the leftmost three, $c = \{0, 0, 0, 1, 0, 1\}$.
- **Type V**: all bits are frozen bits except the rightmost three and the fifth-to-last, $c = \{0, 0, 0, 1, 0, 1, 0, 1\}$.

In [12], two types of generalized fast decoding techniques for G-REP and G-PC nodes were introduced. G-REP is a node at level $p$ with all its descendants being Rate-0 nodes, except the rightmost one at a certain level $q < p$, which is a generic node of rate $C$ ($0 \leq C < 1$). Similarly, G-PC is a node at level $p$ having all its descendants as Rate-1 nodes except the leftmost one at a certain level $q < p$, which is a Rate-0 node.

Recently, the work [17] proposed a new class of multi-node information and frozen bit patterns, namely SR0/REP node, which includes most of the existing special nodes as special cases. For an SR0/REP node at level $p$, all its descendants are Rate-0 or REP nodes except the rightmost one at level $q$, which is a generic source node. The general structure of the SR0/REP node is depicted in Fig. 1, where $N_q^{R_0}$ denotes the source node at level $q$ with $R_q = 2^p - q$. Note that an SR0/REP node will reduce to a G-REP node if all its descendants except the source node are Rate-0 nodes.

An SR0/REP node can be decoded based on the codeword of its source node. Let $s_l = \{s_l[1], \ldots, s_l[2^p-1]\}$ denote the repetition sequence given by

$$s_l = (\eta_q, 1) \otimes (\eta_{q+1}, 1) \otimes \cdots \otimes (\eta_{p-1}, 1),$$

$$l \in \{1, 2, \ldots, |S|\}, \quad (7)$$

where $S$ denotes the set containing all possible $s_l$, and $\eta_q$ denotes the rightmost bit value of the descendant Rate-0/REP node $N_{l}^{R_0-1}$ at level $r$, i.e.,

$$\eta_q = \begin{cases} 
1, & \text{if } N_{l}^{R_0-1} \text{ is a Rate-0 node} \\
1 - 2 \beta_q^{R_0-1}[2^q], & \text{if } N_{l}^{R_0-1} \text{ is an REP node}.
\end{cases} \quad (8)$$

Note that $s_l$ can be pre-determined based on the SR0/REP node structure before decoding. Let $\alpha_{q}^{R_0}[1 : 2^p]$ represent the LLR vector of the source node associated with $s_l$, then in order to decode an SR0/REP node, the LLRs of the source node are first calculated as

$$\alpha_q^{R_0}[k] = \sum_{m=1}^{2^p-q} \alpha_p^j[(m-1)2^q + k] s_l[m],$$

$$k \in \{1, 2, \ldots, 2^q\}, \quad (9)$$
Then, the optimal decoding path index $\hat{l}$ can be selected according to

$$\hat{l} = \arg \max_{l \in \{1, \ldots, |\mathcal{S}|\}} \sum_{k=1}^{2^q} |\alpha^R_{q_l}[k]|.$$  \hspace{1cm} (10)

Subsequently, the source node is decoded to obtain $\beta^R_{q_l}[k]$ using $\alpha^R_{q_l}[1 : 2^p]$. In particular, fast decoding techniques can be utilized if the source node has a special structure, otherwise the plain SC decoding is used. Finally, the decoding result of the SR0/REP node is obtained by

$$\beta^R_{p_l}[k : 2^q : 2^p] = \beta^R_{q_l}[k] \oplus s_i, \quad k \in \{1, 2, \ldots, 2^q\}. \hspace{1cm} (11)$$

Compared with the plain SC decoding, all of the aforementioned fast SC decoding algorithms can preserve the decoding performance with reduced latency by exploiting the special structure of the nodes at intermediate levels of the decoding tree. As a result, if the level of the special node to be decoded is higher, the decoding speed would be faster, but the decoding algorithm might be more difficult to be conducted since the associated bit pattern is more complicated.

III. SEQUENCE RATE-1 OR SPC NODES

In this section, we introduce a new special node, known as the SR1/SPC node, which is characterized by a source node combined with a sequence of Rate-1 or SPC nodes. Then, we characterize the parity constraints induced by the proposed special node that should be satisfied in order to facilitate fast decoding without performance degradation.

A. Node Structure

Similar to the SR0/REP node [17], the proposed SR1/SPC node is defined as any node at level $p$ whose right descendants at level $q \leq r < p$ are all Rate-1 or SPC nodes, except the leftmost one at a certain level $q$, where $0 \leq q < p$. The leftmost node is referred as the source node, which is a generic node of Rate-C. For illustration purpose, the structure of the SR1/SPC node is depicted in Fig. 2.

Given an SR1/SPC node, its node structure, denoted by $\text{NS}(p, q, \mathcal{L})$, is characterized by three key parameters, where $p$ is the root node level, $q$ is the source node level, and $\mathcal{L}$ represents a level index set which consists of the level indices of each descendant SPC node, i.e., $\mathcal{L} = \{r | X_{q+1}^p \text{ is an SPC node}, q \leq r < p\}$ with $L_r = 2^q - r(i - 1) + 1$. Note that the decoding latencies of the existing fast SC decoding algorithms increase linearly with $p - q$, therefore we define $d = p - q$ as the node depth to reflect the parallelism of the SR1/SPC node. Besides, without loss of generality, we assume that the level indices are sorted in ascending order. For instance, a $\mathcal{P}(32, 27)$ polar code with

$$c = \{\text{REP}, \text{SPC}, \text{SPC}, \text{Rate-1}\}$$

can be represented as an SR1/SPC node with $\text{NS}(5, 2, \{2, 3\})$.

Since the source node can be any generic node, the proposed SR1/SPC node can envelop various kinds of special nodes. As shown in Table I, most of the existing special nodes can be viewed as special cases of the SR1/SPC node. However, the existing special nodes either have smaller node depth (parallelism), or are rarely distributed (see Table II), which both lead to limited decoding latency reduction. Note that the case of $\mathcal{L} = \emptyset$ or $\mathcal{L} = \{q, q + 1, \ldots, p - 1\}$, an SR1/SPC node will reduce to a sequence Rate-1 (SR1) or a sequence SPC (SSPC) node, respectively. Besides, it is worth mentioning that exploring other types of descendant node types may lead to the discovery of more special node types that can be decoded efficiently, however further exploration is left for future work.

B. Induced Parity Constraints

As pointed out in [12], each frozen bit at the leaf level of the decoding tree will impose a parity constraint on the possible codewords at the intermediate levels. This means that the codeword at the node root need to satisfy the parity constraints to ensure its validity, otherwise there would be decoding performance loss. For instance, the decoding of the RG-PC node introduced in [12] ignored the parity constraints brought by the frozen bits in the descendant nodes, which leads to significant performance degradation at high SNR scenarios. In the following, we analyse the parity constraints imposed on the root of the SR1/SPC node.
For an arbitrary SR1/SPC node, the parity constraints induced by the frozen bits in the source node can be obtained as follows:

**Theorem 1:** For an SR1/SPC node $N_{p}^{q}$, the source node at level $q$ will impose the following $2^{q}$ parallel parity constraints (P-PC) on the root node at level $p$:

$$2^{d} \bigoplus_{j=1}^{\beta_{p}^{q}[j-1]} \beta_{p}^{q}[2^{q} + k] = \beta_{q}^{p}[k],$$

$$k \in \{1, 2, \ldots, 2^{q}\}.$$

**Proof:** Please see Appendix A. ■

For an SR1 node, since there is no other frozen bit except for those in the source node, we do not need to consider other parity constraints except the P-PCs in (12). However, for a general SR1/SPC node, each of its descendant SPC node will induce an additional parity constraint on its root node, which is given by

$$2^{d} \bigoplus_{j=1}^{2^{p-r-1}} \bigoplus_{k=1}^{2^{r}} \beta_{p}^{q}[(2^{r} - 1)2^{r} + k] = 0. \quad (13)$$

**Proof:** Please see Appendix B. ■

According to Theorems 1 and 2, in order to decode an SR1/SPC node, the aforementioned two types of parity constraints, i.e., P-PCs and S-PCs, derived from the source and descendant SPC nodes, should both be taken into consideration. For illustration purpose, we use two notations to represent the bits with respect to different parity constraints, which are listed as below:

- For the $k$-th P-PC, the bits $\beta_{p}^{q}[k : 2^{2} : 2^{p}]$ constitute an SPC subcode with index $k$, which has a special parity check $\beta_{q}^{p}[k]$.
- The bits $\beta_{p}^{q}[j-1]2^{q} + 1 : j2^{q}$ constitute a segment with index $j$.

According to Theorem 1, each P-PC involves the root bits that are equally spaced in $\beta_{p}^{q}[1 : 2^{p}]$, and these bits compose an SPC subcode that should satisfy the parity check $\beta_{q}^{p}[k]$. On the other hand, the bits involved in the S-PCs are located in different segments of the root node. In Fig. 3, we depict all the P-PCs and S-PCs of a specific SR1/SPC node denoted by NS(5, 2, {2, 3}). It can be observed that the source node with length 4 imposes 4 P-PCs on the root node, while the descendant SPC nodes at levels 2 and 3 introduce two separate S-PCs. To summarize, the P-PCs and S-PCs depend on the SPC subcodes and segments, respectively.

## IV. Fast Decoding of SR1/SPC Nodes

In this section, we first provide an overview to unveil the decoding rules that will lead to promising quasi-ML performance. Then, we present the proposed decoding algorithm for the SR1/SPC nodes, which is divided into two stages. Finally, a simplification technique is further proposed to reduce the computational complexity.

### A. Overview

In general, our proposed decoding algorithms are designed based on two decoding rules originated from the ML decoding. Specifically, by revisiting the ML decoding shown in (6), we summarize two decoding rules for SR1/SPC nodes, which are listed as below:

- All the P-PCs and S-PCs are satisfied simultaneously (validity rule)
- Ensure that the decoded codeword has the least Euclidean Distance with the hard-decision codeword (ML rule)

The first rule, denoted as the validity rule, is to make sure that the estimated codeword is within the space of valid code-word set $\mathcal{B}_{p}^{q}$. Thanks to the analysis of the imposed parity constraints on SR1/SPC nodes, i.e., the P-PCs and S-PCs, we are now able to keep the validity by correcting all the parity checks that are unsatisfied. Conversely, if the codeword of an SR1/SPC node fails to fulfill all the P-PCs and S-PCs simultaneously, the final SC decoding output must be wrong due to the sequential decoding nature, which will degrade the performance. Then, we present the proposed decoding algorithm for the SR1/SPC nodes, which is divided into two stages. Finally, a simplification technique is further proposed to reduce the computational complexity.

### B. Algorithm

The proposed decoding algorithm for SR1/SPC nodes is divided into two stages:

1. **Stage 1:** Validity Check
   - For each P-PC, check if the corresponding parity check is satisfied. If any P-PC fails, the decoding process is stopped.
   - For each S-PC, check if the corresponding parity check is satisfied. If any S-PC fails, the decoding process is stopped.

2. **Stage 2:** ML Decoding
   - Use the valid codeword obtained from Stage 1 as the input for ML decoding.
   - The output of ML decoding is the estimated codeword.

### C. Complexity Analysis

The proposed decoding algorithm has a lower computational complexity compared to the conventional ML decoding. Specifically, the complexity of the proposed algorithm is $O(2^{d})$, while the complexity of the conventional ML decoding is $O(2^{2d})$. The main reason is that the proposed algorithm reduces the number of computations by exploiting the parity constraints.

### D. Simulation Results

To verify the performance of the proposed decoding algorithm, we conduct simulations on various scenarios. The results show that the proposed algorithm achieves a significant performance gain compared to the conventional ML decoding, especially in low SNR regimes. Additionally, the proposed algorithm is more robust to channel errors compared to the conventional ML decoding.
decoding performance. For the latter rule, the Euclidean distance between the estimated codeword and the hard-decision codeword should be as small as possible, which is known as the ML rule.

Following the aforementioned decoding rules, we then design our decoding algorithms for SR1/SPC nodes. First of all, inspired by the ML rule, we propose to directly flip the hard-decision codeword bits to satisfy all the parity constraints. However, each S-PC is dependent on the P-PCs and other S-PCs due to the bits in common, which makes it difficult to develop an efficient decoding algorithm since flipping one bit may impact the parity checks of both P-PCs and S-PCs. To tackle this issue, we propose to progressively satisfy the P-PCs and S-PCs with two stages. In the first stage, the P-PCs are corrected by temporarily ignoring the S-PCs, and in the second stage, the S-PCs are corrected without violating the P-PCs, such that all the parity check constraints are satisfied simultaneously. Specifically, we utilize Wagner decoding to correct the P-PCs and present a flip coordinate set to further correct the S-PCs, such that a list of candidate codewords can be obtained. Furthermore, a penalty metric based on the ML rule is introduced to measure the reliability of each candidate codeword, with which the least penalised codeword is selected as the decoding output. As the decoding rules are originated from the ML decoding, a quasi-ML decoding performance is thus expected. Note that existing highly-parallel ML decoding variants, such as the guessing random additive noise decoding algorithm [20] and the syndrome-check decoding algorithm [21] can also achieve quasi-ML performance, but are usually computational-unfriendly.

In the following, we will introduce the proposed decoding algorithm for SR1/SPC nodes in two stages, and then a simplification technique is further proposed to reduce the computational complexity.

B. Correcting the P-PCs

First, we divide both the LLRs and codeword of the SR1/SPC node into $2^q$ parts such that

$$
\alpha_p^\text{P-PC} [1 : 2^d] = \alpha_p[k : 2^q : 2^p], \\
\beta_p^\text{P-PC} [1 : 2^d] = \beta_p[k : 2^q : 2^p], \\
q \in \{1, 2, \ldots, 2^q\},
$$

(14)

where $\alpha_p^\text{P-PC}[1 : 2^d]$ denotes the LLRs of the $k$-th SPC subcode, and $\beta_p^\text{P-PC}[1 : 2^d]$ represents the corresponding codeword of $\alpha_p^\text{P-PC}[1 : 2^d]$. Then, the LLR vector $\alpha_q^{L_q}[1 : 2^d]$ of the source node can be obtained by

$$
\alpha_q^{L_q}[k] = \prod_{j=1}^{2^d} \text{sgn}(\alpha_k^\text{P-PC}[j]) \min \left( |\alpha_k^\text{P-PC} [1 : 2^d]| \right), \\
q \in \{1, 2, \ldots, 2^q\}.
$$

(15)

Subsequently, the source node is decoded either by plain SC decoding, or by fast decoding techniques if it has a special pattern, to obtain the codeword $\beta_q^{L_q}[1 : 2^d]$. According to Theorem 1, each SPC subcode should satisfy the parity check $\beta_q^{L_q}[k]$, and we employ Wagner decoding to decode these SPC subcodes [22]. For the $k$-th SPC subcode, the parity check of the $k$-th P-PC, denoted by $\gamma_p^\text{P-PC}[k]$, and the least reliable position for bit-flipping, denoted by $\rho[k]$, are respectively determined by

$$
\gamma_p^\text{P-PC}[k] = \bigoplus_{j=1}^{2^d} \text{HD}(\alpha_k^\text{P-PC}[j]) \oplus \beta_q^{L_q}[k], \\
\rho[k] = \arg \min_{j \in \{1, 2, \ldots, 2^q\}} |\alpha_k^\text{P-PC}[j]|.
$$

(16)

(17)

Fig. 3. Parity constraints of an SR1/SPC node NS(5, 2, {2, 3}).
Algorithm 1: Correcting the P-PCs

Input: LLR vector $\alpha_p^t[1 : 2^p]$ of the SR1/SPC node $N_p^t$, node parameters $NS(p, q, L)$

Output: Codeword vector $\beta_p^t[1 : 2^p]$ of $N_p^t$

1 if $N_q^{L_q}$ is a Rate-0 node then
2 \[ \beta_q^t[1 : 2^q] = 0; \]
3 else
4 Calculate $\alpha_q^{L_q}[1 : 2^q]$ using (15);
5 Obtain $\beta_q^{L_q}[1 : 2^q]$ by decoding $N_q^{L_q}$ using $\alpha_q^{L_q}[1 : 2^q]$;
6 Obtain $\beta_p^t[1 : 2^p]$ according to (18);
7 return $\beta_p^t[1 : 2^p]$

Finally, the codeword of the SR1/SPC node with all P-PCs satisfied is obtained by applying bit-flipping operations on the hard-decision codeword, which is shown as follows:

\[ \beta_{p-\text{PC}}[j] = \begin{cases} \text{HD}(\alpha_{p-\text{PC}}[j]) \oplus \gamma_{p-\text{PC}}[k], & \text{if } j = \rho[k] \\ \text{HD}(\alpha_{p-\text{PC}}[j]), & \text{otherwise} \end{cases} \]

(18)

The procedure of correcting P-PCs is summarized in Algorithm 1. Note that the identification of the source node can be performed offline before decoding. In Algorithm 1, the source node is decoded according to its node type (lines 1-5). In particular, in case it is a Rate-0 node, its codeword can be obtained directly (line 2) since there is no information bit to be estimated. Otherwise, LLR calculation is performed (line 4), followed by a specific decoding procedure to obtain the codeword of the source node (line 5). Since the source node might be composed of one or several special nodes, the fast decoding techniques in [8], [9], [10], [11], [12], [17], can be applied. Finally, in line 6, $2^q$ parallel Wagner decoders are implemented to decode the root node according to (18). Note that the SR1 node can be directly decoded by Algorithm 1 since it contains no S-PC.

C. Correcting the S-PCs

Similar to (14), the LLRs and codeword of the SR1/SPC node are divided into $2^d$ parts such that

\[ \alpha_{k-\text{PC}}^{S-\text{PC}}[1 : 2^d] = \alpha_p^t(k-1)2^q + 1 : k2^q], \]
\[ \beta_{k-\text{PC}}^{S-\text{PC}}[1 : 2^d] = \beta_p^t(k-1)2^q + 1 : k2^q], \]
\[ k \in \{1, 2, \ldots, 2^d\}, \]

(19)

where $k$ denotes the segment index, $\alpha_{k-\text{PC}}^{S-\text{PC}}[1 : 2^d]$ denotes the LLR subvector associated with the $k$-th segment, and $\beta_{k-\text{PC}}^{S-\text{PC}}[1 : 2^d]$ represents the corresponding codeword of $\alpha_{k-\text{PC}}^{S-\text{PC}}[1 : 2^d]$. For the SR1/SPC node of depth $d$, let $\gamma_{S-\text{PC}}[1 : d]$ denote the S-PC parity check vector, which can be calculated based on Theorem 2 as follows:

\[ \gamma_{S-\text{PC}}[t] = \begin{cases} 2^{q-r-1} + 1, & \text{if } N_{L+1}^{L+1} \text{ is an SPC node} \\ 2^{q-r-1} + (2j - 1)2^r + k, & \text{if } N_{L+1}^{L+1} \text{ is a Rate-1 node} \end{cases} \]

(20)

where $-1$ indicates that the descendant node $N_{L+1}^{L+1}$ has no S-PC as it is a Rate-1 node. Note that $\gamma_{S-\text{PC}}[t]$ is also able to indicate whether the $t$-th S-PC is satisfied or not, since a satisfied S-PC leads to an even check and an unsatisfied one leads to the opposite. Besides, for an arbitrary even numbers of segments, the $m$-th bits in these segments should be flipped to maintain the $m$-th P-PCs $(m \in \{1, 2, \ldots, 2^q\})$. Thus, let $E = \{k_1, k_2, m\}$ denote a flip coordinate set, which indicates a pair of bit positions to be flipped, i.e., $\beta_{k_1}^{S-\text{PC}}[m]$ and $\beta_{k_2}^{S-\text{PC}}[m]$, where $k_1, k_2 \in \{1, 2, \ldots, 2^d\}$ are segment indices and $k_1 < k_2$. For simplicity, we drop the bit index $m$ and $E = \{k_1, k_2\}$ is simply written as $E = \{k_1, k_2\}$ in the following. Based on $E$, we are able to determine the feasible flip coordinates and flipping the corresponding bits can correct the S-PCs with odd checks without violating the P-PCs.

As mentioned above, a feasible flip coordinate should correct the odd S-PC checks while maintain the even ones. Therefore, for a feasible flip coordinate $E = \{k_1, k_2\}$, only one of the two segment indices should be involved in the S-PCs with odd checks. Besides, $k_1$ and $k_2$ should both be involved or not involved by the remaining S-PCs such that the remaining S-PC checks can be maintained. For simplicity, we say two segments are equivalent if they are both involved or not involved in the $t$-th S-PC. On the contrary, two segments are not equivalent if only one of them is involved in the $t$-th S-PC. From (20), we can readily determine whether a segment is related to the $t$-th S-PC or not. Specifically, segments with indices in

\[ I_t = \{2^t+1, 2^{t-1}+2, \ldots, 2^t, \ldots, (2j-1)2^t+1, (2j-2)2^t+2, \ldots, 2^d-2^t-1+1, 2^d-2^t-1+2, \ldots, 2^d\}, \]

(21)

are involved in the $t$-th S-PC, whereas those with indices in

\[ I'_t = \{1, 2, \ldots, 2^t-1, \ldots, (j-1)2^t-1+1, \ldots, (j-1)2^t-1+2, \ldots, 2^d-2^t-1+1, 2^d-2^t-1+2, \ldots, 2^d\}, \]

(22)

are not involved, where $j \in \{1, 2, \ldots, 2^d-t\}$. By identifying the segments that impact each S-PC, we can obtain the following theorem to determine whether two segments are equivalent or not.

**Theorem 3:** For the $t$-th S-PC, segments $k + \mu2^j$ with $\mu \in \{[-k/2^j], \ldots, [(2^d - k)/2^j]\} \setminus \{0\}$ are equivalent to segment $k$. Besides, segments $k + (2v - 1)2^j$ with $\nu \in \{[-k/2^j + 1/2], \ldots, [(2^d - k)/2^j + 1/2]\}$ are not equivalent to segment $k$.

**Proof:** Please refer to Appendix C.
Theorem 3 implies that applying bit-flipping on the coordinate \( \{ k, k + \mu 2^t \} \) is able to maintain the \( t \)-th S-PC, while performing bit-flipping on \( \{ k, k + (2v-1)2^{t-1} \} \) changes the \( t \)-th S-PC. For the special case that \( \gamma_{S-PC}[1 : d] = (0, \ldots, 0, 1) \), the feasible flip coordinates can be determined by resorting to the following lemma.

**Lemma 1:** For SR1/SPC nodes, the feasible flip coordinates associated with \( \gamma_{S-PC}[1 : d] = (0, \ldots, 0, 1) \) are

\[
E = \left\{ k, k + 2^{d-1} \right\}, \quad k \in \{ 1, 2, \ldots, 2^{d-1} \}. \quad (23)
\]

**Proof:** A feasible flip coordinate must contain the indices of two equivalent segments in order to maintain the S-PCs with even checks from \( t = 1 \) to \( t = d - 1 \). Besides, if the parity check of the \( d \)-th S-PC is odd, then it must be corrected by flipping two inequivalent segments. Starting from \( t = 1 \), the indices of involved and uninvolved segments can be respectively obtained as \( I_1 = \{ 2, 4, 6, \ldots, 2^d \} \) and \( I^c_1 = \{ 1, 3, 5, \ldots, 2^d - 1 \} \) according to (21) and (22). Thus, we can infer that for any feasible flip coordinate, the interval between two segment indices must be even, thus the set of feasible intervals can be determined by \( \{ 2, 4, 6, \ldots, 2^d \} \). Then, for the case of \( t = 2 \), we can see that all the intervals with values \((2v-1)2^{t-1}\) are infeasible based on Theorem 3, which reduces the set of feasible intervals to \( \{ 4, 8, 12, \ldots, 2^d \} \). Meanwhile, \( \{ 4, 8, 12, \ldots, 2^d \} \) is valid since two segments with intervals \( \mu 2^t \) are equivalent according to Theorem 3. Furthermore, for the case of \( t = 3 \), this set becomes \( \{ 8, 16, 24, \ldots, 2^d \} \) by resorting to Theorem 3 again. Repeat the above procedure multiple times until \( t = d - 1 \), we can obtain that the only feasible interval is \( 2^{d-1} \). Finally, for the case of \( t = d \), it can be readily proved that the segments with interval \( 2^{d-1} \) are inequivalent according to Theorem 3. This thus completes the proof.

Lemma 1 only provides the feasible flip coordinates for the special case of \( \gamma_{S-PC}[1 : d] = (0, \ldots, 0, 1) \). Next, we will construct the feasible flip coordinates for more general cases via induction. Given an depth-\((d - 1)\) SR1/SPC node and a feasible flip coordinate \( E = \{ k_1, k_2 \} \) associated with \( \gamma_{S-PC}[1 : d - 1] \), let us consider an extended SR1/SPC node of depth \( d \), whose left child node is the original SR1/SPC node of depth \( d - 1 \) and the right child node is a Rate-1 or an SPC node, which introduces an additional S-PC with parity check \( \gamma_{S-PC}[d] \). Then, the feasible flip coordinates for the new SR1/SPC node of depth \( d \) can be constructed based on the original one of depth \( d - 1 \), which are shown as follows:

**Lemma 2:** For SR1/SPC nodes, given a feasible flip coordinate \( E = \{ k_1, k_2 \} \) and \( \gamma_{S-PC}[1 : d - 1] \) associated with \( \gamma_{S-PC}[1 : d - 1] \), we define four new flip coordinates \( \bar{E}_1 = \{ k_1, k_2 \}, \bar{E}_2 = \{ k_1 + 2^{d-1}, k_2 + 2^{d-1} \}, \bar{E}_3 = \{ k_1 + 2^{d-1}, k_2 + 2^{d-1} \}, \bar{E}_4 = \{ k_1, k_2 + 2^{d-1} \} \) determined by \( E \), then the following flip coordinates associated with \( \gamma_{S-PC}[1 : d] \) are feasible for different cases of \( \gamma_{S-PC}[d] \):

- \( \bar{E}_1, \bar{E}_2 \), if \( \gamma_{S-PC}[d] = 0 \),
- \( \bar{E}_3, \bar{E}_4 \), if \( \gamma_{S-PC}[d] = 1 \),
- \( \bar{E}_1, \bar{E}_2, \bar{E}_3, \bar{E}_4 \), if \( \gamma_{S-PC}[d] = -1 \).

**Proof:** Firstly, for the case of \( \gamma_{S-PC}[d] = 0 \), the two segment indices in a feasible flip coordinate should be equivalent, while keeping the parity checks of the other S-PCs unchanged. It can be observed from (21) and (22) that \( k_1 \) and \( k_2 \) are both not involved in the \( d \)-th S-PC, while \( k_1 + 2^{d-1} \) and \( k_2 + 2^{d-1} \) are both involved, thus \( \bar{E}_1 = \{ k_1, k_2 \} \) and \( \bar{E}_2 = \{ k_1 + 2^{d-1}, k_2 + 2^{d-1} \} \) can maintain the \( d \)-th S-PC. Besides, according to Theorem 3, segments \( k \) and \( k + 2^{d-1} \) are equivalent for the \( t \)-th S-PC with \( t \leq d - 1 \), which means that \( \bar{E}_2 = \{ k_1 + 2^{d-1}, k_2 + 2^{d-1} \} \) will not violate the other S-PCs.

Next, if \( \gamma_{S-PC}[d] = 1 \), the two segment indices in a feasible flip coordinate should be inequivalent, while keeping the parity checks of the other S-PCs unchanged. It can be observed from (21) and (22) that \( k_1 \) and \( k_2 \) are both not involved in the \( d \)-th S-PC, while \( k_1 + 2^{d-1} \) and \( k_2 + 2^{d-1} \) are both involved, thus \( \bar{E}_3 = \{ k_1 + 2^{d-1}, k_2 \} \) and \( \bar{E}_4 = \{ k_1, k_2 + 2^{d-1} \} \) can correct the parity check of the \( d \)-th S-PC. Besides, according to Theorem 3, segments \( k \) and \( k + 2^{d-1} \) are equivalent for the \( t \)-th S-PC with \( t \leq d - 1 \), which means that both \( \bar{E}_3 = \{ k_1 + 2^{d-1}, k_2 \} \) and \( \bar{E}_4 = \{ k_1, k_2 + 2^{d-1} \} \) will not violate the other S-PCs.

Finally, since the additional descendant node imposes no S-PC on the codeword of the SR1/SPC node for the case of \( \gamma_{S-PC}[d] = -1 \), a feasible flip coordinate associated with \( \gamma_{S-PC}[1 : d] \) only needs to keep all S-PC checks unchanged. As proved above, segments \( k \) and \( k + 2^{d-1} \) are equivalent for the \( t \)-th S-PC with \( t \leq d - 1 \), thus applying this equivalence to either one or both of the elements in \( E = \{ k_1, k_2 \} \) results in four new feasible flip coordinates as shown in (26), which completes the proof.

The results in Lemma 2 indicates a splitting procedure to construct feasible flip coordinates, as shown in Fig. 4 for an example with \( d = 3 \) and \( \gamma_{S-PC}[1 : d - 1] = (0, 1) \). In Fig. 4, each box represents a segment, boxes with dashed lines represent the segments involved in a particular S-PC. Besides, a box marked with a colour represents a flipped segment, and each flip coordinate is represented by two connected boxes marked with different colours. Note that one can determine whether the parity check of a certain S-PC is correct through the number of involved flipped segments, i.e., flipping an even numbers of segments involved by an S-PC can maintain the corresponding parity check, otherwise the parity check is changed. Given \( d = 3 \) and \( \gamma_{S-PC}[1 : d - 1] = (0, 1) \), a feasible flip coordinate can be determined as \( E = \{ 1, 3 \} \) according to Lemma 1. It is observed that with \( E = \{ 1, 3 \} \), the parity checks of the S-PCs in the depth-\((d - 1)\) SR1/SPC node are corrected. Then, \( E \) is split into new feasible flip coordinates, which are determined based on the value of \( \gamma_{S-PC}[d] \), as shown in Fig. 4 (a), (b) and (c), respectively. If \( \gamma_{S-PC}[d] = 0 \) (Fig. 4 (a)), the splitting procedure follows (25) in Lemma 2, which leads to \( \bar{E}_1 = \{ 1, 3 \} \) and \( \bar{E}_2 = \{ 5, 7 \} \). If \( \gamma_{S-PC}[d] = 1 \) (Fig. 4 (b)), \( E = \{ 1, 3 \} \) is split into \( \bar{E}_3 = \{ 3, 5 \} \) and \( \bar{E}_4 = \{ 1, 7 \} \) according to (26). Otherwise, for the case of \( \gamma_{S-PC}[d] = -1 \) (Fig. 4 (c)), four flip coordinates \( \bar{E}_1 = \{ 1, 3 \} \), \( \bar{E}_2 = \{ 5, 7 \} \), \( \bar{E}_3 = \{ 3, 5 \} \) and \( \bar{E}_4 = \{ 1, 7 \} \) are generated according to (26). For the extended SR1/SPC node of depth \( d \), it can also be observed that all the S-PCs are not violated, which validates
the correctness of flip coordinates derived from the splitting procedure.

Based on Lemmas 1 and 2, we present in Algorithm 2 the procedure to construct the flipping set $\mathcal{F}_{S_\text{PC}}$ that contains all feasible flip coordinates for SR1/SPC nodes. From Algorithm 2, it can be observed that there is a boundary condition under which $\mathcal{F}_{S_\text{PC}}$ can be obtained directly, which is shown in line 2. Lines 3-6 determine $\mathcal{F}_{S_\text{PC}}$ according to Lemma 1. In lines 8-24, a splitting procedure is performed based on Lemma 2, where $\mathcal{F}_{S_\text{PC}}$ is constructed based on $\mathcal{F}$ associated with $\gamma_{S_\text{PC}}[1 : d - 1]$.

Algorithm 2 provides a number of possible flip coordinates for correcting S-PCs, and performing bit-flipping on these bit positions will not violate the P-PCs. Considering the ML rule in (6), we introduce a penalty metric $\lambda_{E}$ associated with the flip coordinate $E \in \mathcal{F}$ based on Lemma 2, where

$$\lambda_{E} = (1 - 2\beta_{k_1}^{S_\text{PC}}[m])\alpha_{k_1}^{S_\text{PC}}[m] + (1 - 2\beta_{k_2}^{S_\text{PC}}[m])\alpha_{k_2}^{S_\text{PC}}[m].$$

(27)

Then, we select the optimal flip coordinate that has the least penalty metric for bit-flipping, i.e.,

$$E_{\text{opt}} = \arg \min_{E \in \mathcal{F}_{S_\text{PC}}} \lambda_{E}.$$  

(28)

Finally, for the codeword obtained from Algorithm 1, bit-flipping operations are performed on the pair of bit positions determined by $E_{\text{opt}}$, which are shown as follows:

$$\beta_{k_1}^{S_\text{PC}}[m] = \beta_{k_1}^{S_\text{PC}}[m] \oplus 1,$$

$$\beta_{k_2}^{S_\text{PC}}[m] = \beta_{k_2}^{S_\text{PC}}[m] \oplus 1.$$  

(29)

D. Decoding of SR1/SPC Nodes

Based on Algorithms 1 and 2, the overall decoding procedure of SR1/SPC nodes is summarized in Algorithm 3. As can be seen, an SR1/SPC node is first decoded using Algorithm 1 (line 1) to obtain the codeword $\beta_{p}^{S_1}[1 : 2^p]$, and at this point the P-PCs of the SR1/SPC node are satisfied. Then, the parity checks of the S-PCs $\gamma_{S_\text{PC}}[1 : d]$ are calculated (line 2). In case that all the S-PCs are satisfied (depending on the channel conditions), which indicates that the current codeword $\beta_{p}^{S_1}[1 : 2^p]$ is optimal, then the whole algorithm is terminated. Otherwise, bit-flipping operations on $\beta_{p}^{S_2}[1 : 2^p]$ are required to correct the odd S-PC checks (lines 3-8), i.e., flipping a pair of bits on $\beta_{p}^{S_2}[1 : 2^p]$ associated with the flip coordinate. All the feasible flip coordinates are contained in the flipping set which can be determined using Algorithm 2 (line 4). Note that by taking all possible values of $\gamma_{S_\text{PC}}[1 : d]$ into consideration, all the flipping sets associated with $\gamma_{S_\text{PC}}[1 : d]$ can be generated offline before decoding. Thus, for a specific vector consists of the S-PC checks, the corresponding flipping set can be determined instantly during decoding. For each feasible flip coordinate in the flipping set, we evaluate its penalty metric according to (27) (lines 5-6). Then, the optimal flip coordinate is selected by comparing these penalty metrics (line 7). Finally, the pair of bits indicated by the optimal flip coordinate are flipped to obtain the final codeword vector (line 8). By identifying the proposed SR1/SPC nodes, Algorithm 3 can be incorporated into the existing fast decoding algorithms, which further reduces the decoding latency.

To select the optimal codeword, the penalty metrics of each flip coordinate from the flipping set should be calculated and compared, resulting in high computational complexity. For a flip coordinate $E = \{k_1, k_2, m\}$, we say $E$ is corrupted if $\beta_{k_1}^{S_\text{PC}}[m] \neq \text{HD}(\alpha_{k_1}^{S_\text{PC}}[m])$ or $\beta_{k_2}^{S_\text{PC}}[m] \neq \text{HD}(\alpha_{k_2}^{S_\text{PC}}[m])$,
Algorithm 2: Generate Flipping Set $F_{\gamma_S:PC}$ for SR1/SPC Nodes

**Input:** Parities for checking S-PCs $\gamma_{S:PC}[1 : p-q]$

**Output:** Flipping set $F_{\gamma_S:PC}$

1. $F_{\gamma_S:PC} = \emptyset$
2. if $\gamma_{S:PC}[1 : d] = (0, \ldots, 0, 1)$ then
   3. for $k = \{1, 2, \ldots, 2^{d-1}\}$ do
   4. $\mathcal{E} = \{k, k + 2^{d-1}\}$
   5. $F_{\gamma_S:PC} = \{F_{\gamma_S:PC}, \mathcal{E}\}$
   6. return $F_{\gamma_S:PC}$
   else
5. Obtain $\mathcal{F}$ associated with $\gamma_{S:PC}[1 : d-1]$ using Algorithm 2;
6. if $\gamma_{S:PC}[d] = 0$ then
7. foreach $\mathcal{E}$ in $\mathcal{F}$ do
8. $\mathcal{E}_1 = \{k_1, k_2\}$, $\mathcal{E}_2 = \{k_1 + 2^{d-1}, k_2 + 2^{d-1}\}$
9. $F_{\gamma_S:PC} = \{F_{\gamma_S:PC}, \mathcal{E}_1, \mathcal{E}_2\}$
10. return $F_{\gamma_S:PC}$
else if $\gamma_{S:PC}[d] = 1$ then
11. foreach $\mathcal{E}$ in $\mathcal{F}$ do
12. $\mathcal{E}_3 = \{k_1 + 2^{d-1}, k_2\}$, $\mathcal{E}_4 = \{k_1, k_2 + 2^{d-1}\}$
13. $F_{\gamma_S:PC} = \{F_{\gamma_S:PC}, \mathcal{E}_3, \mathcal{E}_4\}$
14. return $F_{\gamma_S:PC}$
else
15. foreach $\mathcal{E}$ in $\mathcal{F}$ do
16. $\mathcal{E}_1 = \{k_1, k_2\}$, $\mathcal{E}_2 = \{k_1 + 2^{d-1}, k_2 + 2^{d-1}\}$
17. $\mathcal{E}_3 = \{k_1 + 2^{d-1}, k_2\}$, $\mathcal{E}_4 = \{k_1, k_2 + 2^{d-1}\}$
18. $F_{\gamma_S:PC} = \{F_{\gamma_S:PC}, \mathcal{E}_1, \mathcal{E}_2, \mathcal{E}_3, \mathcal{E}_4\}$
19. return $F_{\gamma_S:PC}$

Algorithm 3: Decoding of SR1/SPC Nodes

**Input:** LLR vector $\alpha_p^i[1 : 2^p]$ of the SR1/SPC node $N_p^i$, node parameters $N(p, q, \mathcal{L})$

**Output:** Codeword vector $\beta_{p}^i[1 : 2^p]$ of $N_p^i$

1. Obtain $\beta_p^i[1 : 2^p]$ using Algorithm 1;
2. Calculate $\gamma_{S:PC}[1 : d]$ using (20);
3. if $\exists t \in \{1, 2, \ldots, d\}, \gamma_{S:PC}[t] = 1$ then
4. Generate $F_{\gamma_S:PC}$ using Algorithm 2;
5. foreach $\mathcal{E}$ in $F_{\gamma_S:PC}$ do
6. Calculate $\lambda_{\mathcal{E}}$ using (27);
7. Choose $E_{opt}$ according to (28);
8. Perform bit-flipping operations on $\beta_p^i[1 : 2^p]$ using (29);
9. return $\beta_p^i[1 : 2^p]$

V. SIMULATION RESULTS

In this section, the node distribution, average decoding latency, computational complexity, and error-correction performance of the proposed decoding algorithms are investigated, and comparison with the state-of-the-art fast SC decoding algorithms is provided. We consider polar codes with length $N \in \{512, 1024, 4096\}$. When $N \leq 1024$, polar codes are constructed according to the 5G standard [3], while for $N = 4096$, the Gaussian Approximation (GA) method [23] is utilized for code construction. Furthermore, the FSSC decoder proposed in [10], which takes Rate-0, Rate-1, REP and SPC nodes into consideration, is selected as the baseline. Other state-of-the-art fast SC decoders that presented in [11], [12] and [17], namely FSC1, FSC2 and FSC3, are also considered for comparison, which progressively applied the decoding of Type-I-IV nodes, G-REP and G-PC nodes, and SR0/REP nodes to the FSSC decoder, respectively. To evaluate the effects of the proposed SR1/SPC nodes on the decoding speed, the decoding of Rate-0, Rate-1, REP, SPC and SR0/REP nodes is combined with the decoding of the proposed SR1/SPC node in Algorithm 3, and the resulting fast SC decoder with sequence nodes, abbreviated as SN-FSC, is used for comparison. In order to gain further speedup, we also present a relaxed fast SC decoder with sequence nodes, namely the SN-RFSC decoder, where SR1/SPC nodes are decoded as RG-PC nodes by ignoring the frozen bits in the SR1/SPC descendant nodes, as done in [12]. Specifically, the SN-RFSC chooses to skip the operations in lines 3-8 of Algorithm 3 when decoding SR1/SPC nodes. To summarize, the considered special nodes of different decoders are listed as follows:

- **FSC [10]:** Rate-0 + Rate-1 + REP + SPC.
- **FSC1 [11]:** FSC + Type I-V.
- **FSC2 [12]:** FSC + G-REP + G-PC.
- **FSC3 [17]:** FSC + EG-PC + SR0/REP.
- **SN-FSC:** FSC + SR0/REP + SR1/SPC.
- **SN-RFSC:** FSC + SR0/REP + RG-PC.
Following the decoding tree depicted in Fig. 2, the source node other existing special nodes when employing other decoders. As the proposed special node is a highly parallel node, it needs to be decomposed into the total number of time steps can be calculated by adding required by the check-node operations. Specifically, the LLR decoding latency of these nodes and the additional latency of the existing fast SC decoders. Therefore, decoded using separate fast decoding algorithms. Therefore, and the descendant Rate-1 or SPC nodes should be serially located at higher levels of the decoding tree, and thus the number of such nodes is smaller. Besides, although the proposed SR1 node a generalized version of the EG-PC node, they have almost the same distribution in a practical polar code, which means that the source node in the SR1 node is usually Rate-0 or REP. However, other types of SR1/SPC nodes are shown to be more frequently distributed as compared to the EG-PC nodes, leading to significant overall latency reduction. We also note that the implementation complexity can be significantly reduced by using the proposed decoder, since we do not need to develop a dedicated decoder for each special node type shown in Table I. In particular, 5G polar codes with $N = 128$ can be represented by only SRO/REP and SR1/SPC nodes.

### A. Node Distribution

Table II shows the numbers of EG-PC and SR1/SPC nodes contained in a particular polar code with different code lengths $N$ and code rates $R$. It can be seen that generally, the number of SR1/SPC nodes increases with the increasing of the code length $N$, i.e., more latency savings can be achieved for longer polar codes. When $R > 1/2$, it is observed that the total number of SR1/SPC nodes is smaller, but the node depth is larger as the code length $N$ increases. This is because as the code rate increases, the proposed SR1/SPC nodes tend to be located at higher levels of the decoding tree, and thus the number of such nodes is smaller. Besides, although the proposed SR1 node a generalized version of the EG-PC node, they have almost the same distribution in a practical polar code, which means that the source node in the SR1 node is usually Rate-0 or REP. However, other types of SR1/SPC nodes are shown to be more frequently distributed as compared to the EG-PC nodes, leading to significant overall latency reduction. We also note that the implementation complexity can be significantly reduced by using the proposed decoder, since we do not need to develop a dedicated decoder for each special node type shown in Table I. In particular, 5G polar codes with $N = 128$ can be represented by only SRO/REP and SR1/SPC nodes.

### B. Decoding Latency and Computational Complexity Analysis

In this subsection, the decoding latency of our proposed fast SC decoders is compared with that of the state of the arts. In particular, we analyse the required number of time steps to decode the proposed SR1/SPC node, where the same unlimited-resource assumptions as in [9], [11], [17] are utilized, which are shown as follows:

- Addition/subtraction of real numbers and check-node operations can be performed in one time step.
- Bit operations can be carried out instantly.
- Wagner decoding consumes one time step.

Based on these assumptions, the number of required time steps to decode the existing nodes is listed in Table III.

For SR1/SPC nodes, we first present the decoding latency of the existing fast SC decoders. As the proposed special node is a highly parallel node, it needs to be decomposed into other existing special nodes when employing other decoders. Following the decoding tree depicted in Fig. 2, the source node and the descendant Rate-1 or SPC nodes should be serially decoded using separate fast decoding algorithms. Therefore, the total number of time steps can be calculated by adding the decoding latency of these nodes and the additional latency required by the check-node operations. Specifically, the LLR calculation for the left child node at each level consumes one time step, resulting in $d$ time steps to traverse to the source node. Next, the decoding of the source node requires $T_{SN}$ time steps, where the value of $T_{SN}$ depends on the considered decoding algorithms. After decoding the source node, the hard codeword is passed back to the parent node to calculate the LLRs for the descendant Rate-1 or SPC nodes. As such, check-node operations are performed at each level, leading to $d$ time steps in total. Besides, the descendant nodes are decoded using their corresponding decoding algorithms [10], which account for additional $|L|$ time steps (0 for Rate-1 nodes and 1 for SPC nodes). Finally, the total number of time steps required to decode an SR1/SPC node is $T_{SN} + 2d + |L|$, when using the existing fast SC decoders.

On the other hand, if the proposed SN-FSC decoder is used, then the decoding latency of SR1/SPC can be calculated according to the following analysis. Let $T_1$ and $T_2$ denote respectively the corresponding required time steps of the first stage and second stage in Algorithm 3. First, we analyse $T_1$, i.e., the number of required time steps to perform Algorithm 1. As can be seen, the decoding in the first stage depends on the source node structure. In case that the source node is Rate-0, its codeword can be obtained immediately. Otherwise, calculating the LLRs and decoding the source node require one $T_{SN}$ time steps, respectively. Moreover, applying Wagner decoding to the root node requires one time step. Therefore, $T_1$ can be expressed as

$$T_1 = \begin{cases} 1, & \text{if the source node is Rate-0} \\ T_{SN} + 2, & \text{otherwise} \end{cases} \quad (30)$$

Subsequently, we can see that calculating the parity checks of the S-PCs in line 2 of Algorithm 3 can be performed instantaneously since it only involves XOR bit operations. Note that the flipping set can be generated offline, thus conducting line 4 incurs no latency. The calculation of the penalty metrics in lines 5-6 only involves addition operations and can be executed in parallel, which requires one time step. The following selection of the optimal flip coordinate in line 7 is based on a comparison tree, and thus consuming another one time step. Finally, performing bit-flipping operations (line 8) requires no time step, since only XOR bit operations are involved as shown in (29). As a result, $T_2$ is given by

$$T_2 = \begin{cases} 2, & \text{if } \exists t \in \{1, 2, \ldots, d\}, \gamma_{S-PC}[t] = 1 \\ 0, & \text{otherwise} \end{cases} \quad (31)$$

As can be seen, $T_2$ is a variable depending on $\gamma_{S-PC}[1 : d]$, which is further dependent on the channel conditions. To summarize, the total numbers of time steps required to decode SR1, SSPC and SR1/SPC node are respectively

| Rate-0 | 0 | Rate-1 | 0 | REP | 1 | SPC | 1 | Type I | 1 | Type II | 2 | Type III | 1 | Type IV | 2 |
|-------|---|--------|---|-----|---|-----|---|-------|---|-------|---|----------|---|-------|---|
| Type V | 1 | G-PC | 2 | G-REP | 1 | EG-PC | 2 | SRO/REP | $T_{SN} + 3$ | SR1/SPC | $T_{SN} + 2d + |L|$ |

$*$ When the SR1/SPC node is decoded by the proposed SN-FSC decoder.  
$^\dagger$ When the SR1/SPC node is decoded by the existing fast SC decoders.

TABLE III

**NUMBER OF REQUIRED TIME STEPS TO DECODE DIFFERENT SPECIAL NODES**

| Rate-0 | 0 | Rate-1 | 0 | REP | 1 | SPC | 1 | Type I | 1 | Type II | 2 | Type III | 1 | Type IV | 2 |
|-------|---|--------|---|-----|---|-----|---|-------|---|-------|---|----------|---|-------|---|
| Type V | 1 | G-PC | 2 | G-REP | 1 | EG-PC | 2 | SRO/REP | $T_{SN} + 3$ | SR1/SPC | $T_{SN} + 2d + |L|$ |

$*$ When the SR1/SPC node is decoded by the proposed SN-FSC decoder.  
$^\dagger$ When the SR1/SPC node is decoded by the existing fast SC decoders.
given by

\[ T_{SR1} = T_1, \]
\[ T_{SSPC} = T_{SR1}/SPC = T_1 + T_2. \]  

(32)

Furthermore, the lower and upper bounds of \( T_{SR1}/SPC \), denoted by \( T_{LB} \) and \( T_{UB} \), respectively, are given by

\[ T_{LB} = T_1 + \min(T_2) = T_1, \]
\[ T_{UB} = T_1 + \max(T_2) = T_1 + 2. \]  

(33)

Consequently, for a given polar code, the overall, minimum and maximum numbers of decoding time steps can be calculated based on (32) and (33).

For a fair comparison, we compare the decoding latency when a single SR1/SPC node is decoded by the existing fast SC decoders and the proposed one. As can be seen from Table III, the decoding latency of the existing decoders increases linearly with the node depth \( d \), while \( T_{SR1}/SPC \) is upper bounded by \( T_{UB} = T_1 + 2 \). As a result, the speedup stems from the saving of tree traversal and decoding of the descendant nodes, which means that a higher degree of parallelism can be achieved as the node depth \( d \) increases.

In Table IV, we further compare the decoding latency of the state-of-the-art and the proposed fast SC decoders for the whole polar codes, where two code lengths \( N \in \{512, 4096\} \) and five code rates \( R \in \{1/6, 1/3, 1/2, 2/3, 5/6\} \) are considered. The decoding latency of the proposed SN-FSC decoder is measured by the average number of time steps at \( E_b/N_0 = 0.0,1.0,2.0,3.0,4.0 \) dB, since the required time steps of decoding SR1/SPC nodes \( T_{SR1}/SPC \) is an variable affected by the channel condition, while those of the baseline algorithms are fixed. Besides, the minimum and maximum numbers of required time steps are also presented, which are denoted by ‘LB’ and ‘UB’, respectively. For the proposed SN-FSC decoder, the maximum speedup over the state-of-the-art FSC3 decoder is also provided for comparison. As can be seen, the decoding of SR0/REP node [17] mainly incurs addition operations, which is caused by LLR calculation of a list of repetition sequence patterns, and it was shown in [24] that adopting the SR0/REP node increases the computational resource consumption. Similar to the SR0/REP node, the decoding of the proposed SR1/SPC nodes requires more CS operations to correct the P-PCs and S-PCs, which also increases the number of overall arithmetic operations. However, we can observe from Table V that the arithmetic operations required by the proposed plain SN-FSC decoder is only slightly increased as compared to other fast SC decoders and still significantly lower than the original SC decoder. In addition, with the proposed simplification technique, the SN-FSC decoder can achieve lower computational complexity as compared to the FSC3 decoders.

### Table IV

| \( N \) | \( R \) | FSSC | FSC1 | FSC2 | FSC3 | SN-FSC | SN-RFSC |
|---|---|---|---|---|---|---|---|
| 1/6 | 89 | 63 | 55 | 36 | 34.86 | 34.29 | 34.06 | 34.01 | 34.00 | 34 | 36 | 34 | 5.5 |
| 1/3 | 128 | 85 | 86 | 63 | 47.94 | 48.87 | 49.09 | 49.05 | 43.00 | 43 | 51 | 43 | 31.7 |
| 1/2 | 126 | 89 | 101 | 70 | 59.27 | 57.32 | 54.63 | 54.09 | 54.01 | 54 | 64 | 54 | 22.9 |
| 2/3 | 129 | 87 | 103 | 74 | 58.12 | 56.87 | 53.54 | 50.50 | 50.03 | 50 | 60 | 50 | 32.4 |
| 5/6 | 88 | 64 | 72 | 38 | 38.40 | 37.88 | 37.84 | 35.14 | 32.61 | 32 | 40 | 32 | 44.8 |

| \( E_b/N_0 \) (dB) | 0.0 | 1.0 | 2.0 | 3.0 | 4.0 |
|---|---|---|---|---|---|
| LB | 184.03 | 184.00 | 255.25 | 255.00 | 255.00 |
| UB | 184 | 255 | 255 | 255 | 255 |

The above latency analysis of Algorithm 3 is based on the unlimited-resource assumption where operations can be parallelly executed in a single time step. In the other extreme, i.e., the case of a fully serial implementation, the number of arithmetic (including add and compare) operations can also be employed to measure the average computational complexity. Table V compares the number of arithmetic operations required by the considered decoders, for \( P(1024, 512) \). Herein, we assume that the least reliable bit (see 17) and the optimal flipping coordinate (see 28) are both obtained through a compare-and-select (CS) tree that compares data in pairs with pipelined comparators. Given that \( X \) is the number of input data (usually a power-of-two integer), CS tree operations will require \( \frac{X}{2} + \frac{X}{4} + \ldots + 1 = X - 1 \) comparisons to obtain the maximum/minimum data. For the proposed SN-FSC decoder, the two numbers on each row/column in Table V provide the numbers of arithmetic operations required by the plain decoder and the simplified decoder, respectively. As can be seen, the decoding of SR0/REP node [17] mainly incurs addition operations, which is caused by LLR calculation of a list of repetition sequence patterns, and it was shown in [24] that adopting the SR0/REP node increases the computational resource consumption.
Fig. 5. FER performance comparison of the SC, SCL, SN-FSC and SN-RFSC decoders for SR1/SPC nodes.

Table V

| # Operations   | SC | FSSC | FSC1 | FSC2 | FSC3 |
|----------------|----|------|------|------|------|
| Add            | 5120 | 3110 | 3056 | 3110 | 5379 |
| Compare        | 5120 | 3080 | 2964 | 2958 | 2611 |
| Total          | 10240 | 6190 | 6020 | 6068 | 7990 |

Fig. 6. FER performance comparison of the SC, SN-FSC and SN-RFSC decoders, for 5G polar codes with length $N = 1024$ and $R = \{1/3, 1/2, 2/3\}$.

C. Memory Overhead Analysis

In this subsection, we discuss the memory overhead caused by generating the flipping set offline by Algorithm 2. Basically, the flipping sets are determined by the node structure and further by the whole polar code. As shown in Algorithm 2, the determination of the flipping set depends on $\gamma_{S,PC}[1 : d]$. By considering all possible values in $\gamma_{S,PC}[1 : d]$, the resultant collection of all flipping sets, referred to as flipping collection, is only dependent on the node depth $d$. This indicates that different SR1/SPC nodes can share the same flipping collection given that they have the same node depth. Therefore, although various nodes are contained in a specific polar code (as shown in Table II), most of them share the same flipping collection and thus a large amount of memory consumption can be saved. Based on this discovery and given a maximum node depth $D$, all flipping collections with node depths $1 \leq d \leq D$ can be pre-determined and stored in the memory. Therefore, for any polar codes with arbitrary code lengths and rates, the required flipping set can be read from this memory. As a result, the flipping set is rate-compatible for a practical polar decoder.

Next, we analyse the memory consumption to store flipping collections with different node depths $d$. Let $i$ and $j$ denote respectively the indices of the first ‘1’ and ‘−1’ in $\gamma_{S,PC}[1 : d]$, such that $\gamma_{S,PC}[1 : d] = (i-1, j-i-1, d-j+1, 0, \ldots, 0, 0/1, \ldots, 0/1, -1, \ldots, -1)$, where $1 \leq i \leq d$ and $i + 1 \leq j \leq d + 1$. According to the recursion procedures in Algorithm 2, the size of the flipping set with node depth $d$ is...
determined by its initial size and will be doubled or quadruple every splitting procedure, where the size of the initial flipping set is $2^{i-1}$, and will be doubled $(j - i - 1)$ times and quadrupled $(d - j + 1)$ times. Therefore, the size of the flipping set with node depth $d$ is $(2^{i-1}2^{j-i-1}4^{d-j+1})$. Since there are $2^{j-i-1}$ flipping sets for each $i$ and $j$ pair, the total number of flip coordinates contained in the flipping collection with node depth $d$, denoted by $M_d$, can be expressed as

$$M_d = \sum_{i=1}^{D} \sum_{j=i+1}^{d+1} (2^{i-1}2^{j-i-1}4^{d-j+1})2^{j-i-1} = (d-1)2^{2d-1} + 2^{d-1}. \quad (34)$$

Moreover, each flip coordinate is composed of two segment indices and storing each one of them requires $d$ bits. Finally, the overall memory overhead, denoted by $M$, can be estimated by

$$M = \sum_{d=1}^{D} 2dM_d = \left(\frac{3}{4}D^2 - \frac{20}{9}D + \frac{32}{27}\right)4^D + (D-1)2^{D+1} + \frac{22}{27} \text{ (bits)}. \quad (35)$$

For polar codes with length $N = 512$, the maximum node depth can be determined as $D = 6$ according to Table II, therefore the memory overhead would be 61474 bits. Since the node depth is not very large in practice, the memory overhead caused by storing all the flipping sets will not be overwhelming.

Another promising approach to achieve rate compatibility is to determine the flipping set online using custom-tailored circuits. Since the flipping set is fixed for a given code length/rate, it only needs to be re-determined once the code length/rate is changed. In practice, online determination of the flipping set can be performed in parallel with other modules in the receiver before decoding, such as synchronization, demodulation and equalization, etc., and this will not lead to extra memory overhead and latency. However, the design of the corresponding circuits are usually considered by VLSI oriented papers, which is beyond the scope of this paper.

### D. Error-Correction Performance Comparison

To avoid costly computations, an SCL decoder with list size 32 is implemented to get close-to-ML decoding performance. In Fig. 5, we compare the frame error rate (FER) performance of different decoders, when decoding the SR1/SPC nodes that can be found in a GA polar code with $N = 4096$. Note that the other state-of-the-art decoders (those shown in Table IV) exhibit the same performance as the conventional SC decoder, and thus the comparison is omitted here. First, it can be observed from Fig. 5 (a) that for an SR1 node with NS$(5, 2, \emptyset)$, SC, SCL (with list size 32) and the proposed decoders exhibit the same decoding performance, which means that both SC and the proposed decoding algorithms can obtain ML performance when decoding SR1 nodes. Besides, the SN-RFSC decoder incurs no performance loss as there is no S-PC contained in SR1 nodes, and thus the decoding is optimal once all the P-PCs are corrected. However, the SN-RFSC decoder causes severe performance degradation (larger than 1 dB) when decoding other SR1/SPC special cases (see Fig. 5 (b) and Fig. 5 (c)), which means that it is necessary to take the validity rule into consideration to preserve the error-correction performance. Furthermore, as can be seen from Fig. 5 (b) and Fig. 5 (c), although the performance of the proposed decoder is inferior to that achieved by the SCL decoder when decoding other SR1/SPC special cases, it still outperforms the conventional SC decoder. In essence, SC decoding is locally optimal as it estimate bits at the leaf level, and any wrong choice makes the entire estimated codeword incorrect, thus it is inferior to ML decoding when the channels are incompletely polarized (i.e., when the code length is finite). On the other hand, the proposed decoding algorithms stem from ML decoding, where the codeword is estimated at the node level, based on the aforementioned two decoding rules. Due to the global selection of the best codeword, a slight improvement in terms of error-correction performance can thus be observed. Besides, the slight performance gap between ML decoding and the proposed SN-RFSC decoder is mainly due to the following reasons. First, the proposed decoding algorithms are divided into two stages to progressively satisfy all the parity checks, which is sub-optimal as compared to the globally optimal ML result. Second, since SC decoding is employed to decode the source node, the obtained source node codeword is only locally optimal. Thus, the resulting codeword space for the entire special node is narrowed and the ML codeword may fall out of this space. Therefore, our proposed decoding algorithms can only obtain quasi-ML performance under certain code lengths and rates.

A similar phenomenon can also be observed from Fig. 6, where the proposed decoder is shown to outperform the conventional SC decoder for a $N = 1024$ polar code with $R \in \{1/3, 1/2, 2/3\}$. Note that this is an important advantage of the proposed decoder since the performance of previous fast SC decoders cannot exceed that of the conventional SC decoder. Besides, Fig. 6 also shows that the employment of the proposed simplification technique incurs no performance loss, yet with reduced computational complexity.

### VI. Conclusion

In this work, we introduced a new class of multi-node information and frozen bit patterns, namely the SR1/SPC nodes, and proposed the corresponding fast SC decoding algorithm. The proposed SR1/SPC node can be identified by a sequence of Rate-1 or SPC nodes, and it provides a unified description of a wide variety of special nodes. Moreover, the decoding rules for the proposed SR1/SPC nodes were derived from ML decoding to facilitate fast SC decoding, with which a higher degree of parallelism can be obtained. The proposed decoding algorithm was compared with the state-of-the-art fast SC decoding algorithms, in terms of decoding latency and error-correction performance. Simulation results showed that by combining the existing special nodes with the proposed SR1/SPC nodes, we can achieve much lower decoding latency.
as well as noticeable performance improvement. Besides, note that the proposed SR1/SPC nodes are very promising as they can also be adopted in the SCL decoder, which is left for future work.

**APPENDIX A**

**Proof of Theorem 1**

Given the codeword of each node at level \( q \), the codeword of the root node at level \( p \) can be derived based on the bit recursion formula in (4), i.e.,

\[
\beta_p^q[1 : 2^p] = \beta_q^p (F \otimes d \otimes I_{2^q}),
\]

where \( \beta_q^p = (\beta_q^{L_q}[1 : 2^q], \beta_q^{L_q+1}[1 : 2^q], \ldots, \beta_q^{R_q}[1 : 2^q]) \).

Then, using the identity \((A \otimes B) \otimes C = A \otimes (B \otimes C)\) with \( A = B = F \) and \( C = I_{2^q} \), (36) can be rewritten as

\[
\beta_p^q[1 : 2^p] = \beta_q^p (F \otimes d - 1 \otimes (F \otimes I_{2^q})).
\]

Repeating the above procedures \( d \) - 1 times leads to

\[
\beta_p^q[1 : 2^p] = \beta_q^p (G'_{2d}^q),
\]

where \( G'_{2d} \) is obtained by replacing the 0 and 1 elements in \( G_{2d} \) by \( 0_{2^q} \) and \( I_{2^q} \), respectively. Then, for any \( k \in \{1, 2, \ldots, 2^q\} \), we have

\[
\bigoplus_{j=1}^{2^q} \beta_p^q((j-1)2^q + k) = \bigoplus_{j=1}^{2^q} (\beta_q^p (G'_{2d}^q)(j-1)2^q + k)
\]

\[
= \beta_q^p \bigoplus_{j=1}^{2^q} (G'_{2d}^q)(j-1)2^q + k
\]

\[
= \beta_q^p \begin{pmatrix}
I_{2^q} & 0_{2^q} & \cdots & 0_{2^q}
\end{pmatrix}^T
\]

\[
= \beta_q^p \begin{pmatrix}
k - 1 & 0 & \cdots & 0 & 0 & \cdots & 0
\end{pmatrix}^T
\]

\[
= \beta_q^p[k] \overset{(b)}{=} \beta_q^{L_q^p}[k],
\]

where (a) is based on the property of the generator matrix, i.e., \( \bigoplus_{j=1}^{2^q} (G_{2d}^q)j = (1, 0, \ldots, 0)^T \), and (b) is due to the definition of \( \beta_q^p \). This thus completes the proof.

**APPENDIX B**

**Proof of Theorem 2**

Similar to the proof of Theorem 1, the following equality can be obtained:

\[
\bigoplus_{j=1}^{2^{2^r}} \beta_p^q((2j - 1)2^r + k)
\]

\[
\overset{(a)}{=} \beta_r \bigoplus_{j=1}^{2^{2^r}} (G^r)(2j - 1)2^{r+k}
\]

\[
\overset{(b)}{=} \beta_r \begin{pmatrix}0_{2^r}, I_{2^r}, 0_{2^r}, \ldots, 0_{2^r}\end{pmatrix}^T
\]

\[
= \beta_r \begin{pmatrix}2^{r+k-1} & 2^{r+k-1} & \cdots & 2^{r+k-1} & 0_{2^r} \end{pmatrix}^T
\]

\[
= \beta_q^p[2^r + k] = \beta_q^{L_q^p+1}[k],
\]

where (a) is based on (38) and (b) is because \( \bigoplus_{j=1}^{2^{2^r-1}} (G_{2^r-1})_j = (0, 0, \ldots, 0)^T \). Since \( \mathcal{N}_{r+1}^{L_r} \) is an SPC node, its corresponding codeword should satisfy [10]

\[
\bigoplus_{k=1}^{2^r} \beta_q^{L_q^p+1}[k] = 0.
\]

By replacing \( \beta_q^{L_q^p+1}[k] \) on the left-hand-side of (41) by (40), (13) can be readily proved.

**APPENDIX C**

**Proof of Theorem 3**

First, we prove the equivalence of segments \( k \) and \( k + 2^t \), \( \mu = \{[-k/2^t], \ldots, [(2^d-k)/2^t]\} \). Starting from \( \mu = 1 \), if segment \( k \) is involved in the \( t \)-th S-PC, i.e., \( k \in \mathcal{I}_t \), the range of \( k + 2^t \) can be accordingly determined by

\[
k \in \mathcal{I}_t \Rightarrow (2j - 1)2^t + 1 + 2^t \leq k + 2^t \leq j2^t + 2^t
\]

\[
\Rightarrow (2(j - 1)2^{t-1} + 1 + 2^t) \leq k + 2^t \leq (j + 1)2^t
\]

\[
\Rightarrow k + 2^t \in \mathcal{I}_t.
\]

By viewing \( j + 1 \) as a new \( j \), it can be observed from (21) that segment \( k + 2^t \) is also involved in the \( t \)-th S-PC. Likewise, if segment \( k \) is not involved in the \( t \)-th S-PC, i.e., \( k \in \mathcal{I}_t^c \), the range of \( k + 2^t \) can be determined based on (22), given by

\[
k \in \mathcal{I}_t^c \Rightarrow (j - 1)2^t + 1 + 2^t \leq k + 2^t \leq (2j - 1)2^{t-1} + 2^t
\]

\[
\Rightarrow j2^t + 1 \leq k + 2^t \leq (2(j - 1)2^{t-1} + 2^t
\]

\[
\Rightarrow k + 2^t \in \mathcal{I}_t^c
\]

which shows that segment \( k + 2^t \) is not related to the \( t \)-th S-PC. Therefore, segments \( k \) and \( k + 2^t \) are equivalent for \( j = 1 \). Then, following a similar procedure, it can be proved that segment \( k + 2^t \) is equivalent to segment \( k + 2 \times 2^t \) and the latter is further equivalent to \( k + 3 \times 2^t \), etc. To sum up, we can prove that segment \( k \) is equivalent to segments \( k + \{[-k/2^t], \ldots, [(2^d-k)/2^t]\} \), which thus proves that segments \( k + \mu 2^t \), \( \mu = \{[-k/2^t], \ldots, [(2^d-k)/2^t]\} \) are equivalent with each other.

Then, we prove that segments \( k \) and \( k + (2^t - 1)2^t \) are inequivalent (\( \nu = \{[-k/2^t+1/2], \ldots, [(2^d-k)/2^t+1/2]\} \)). Let \( \nu = 1 \), depending on whether segment \( k \) is involved in the \( t \)-th S-PC or not, the ranges of \( k + 2^{t-1} \) can be respectively obtained as follows based on (21) and (22):

\[
k \in \mathcal{I}_t
\]

\[
\Rightarrow (2j - 1)2^{t-1} + 1 + 2^{t-1} \leq k + 2^{t-1} \leq j2^t + 2^{t-1}
\]

\[
\Rightarrow j2^t + 1 \leq k + 2^{t-1} \leq (2j + 1)2^{t-1}
\]

\[
\Rightarrow k + 2^t \in \mathcal{I}_t^c
\]

Authorized licensed use limited to the terms of the applicable license agreement with IEEE. Restrictions apply.
As can be seen, only one of the two segments \( k \) and \( k + 2t - 1 \) is involved in the \( t \)-th S-PC. Therefore, for the \( t \)-th S-PC, segments \( k \) and \( k + 2t - 1 \) are inequivalent, which proves the case of \( \nu = 1 \). Then, since segments \( k + 2t - 1 \) and \( k + 2t - 1 + \mu 2^{t} \) are equivalent based on the above proof, we can conclude that segment \( k \) is also inequivalent to segment \( k + (2t-1)2^{t-1} \) with \( \nu \in \{\lceil -k/2^{t} + 1/2 \rceil, \ldots, \lceil (2^{d} - k)/2^{t} + 1/2 \rceil \} \).

This thus completes the proof.

**REFERENCES**

[1] Y. Lu, M.-M. Zhao, M. Lei, and M.-I. Zhao, “Fast decoding of sequence rate-1 or SPC nodes for polar codes,” in *Proc. IEEE Int. Conf. Commun. (ICC)*, Rome, Italy, May 2023, pp. 125–131.

[2] E. Arikan, “Channel polarization: A method for constructing capacity-achieving codes for symmetric binary-input memoryless channels,” *IEEE Trans. Inf. Theory*, vol. 55, no. 7, pp. 3051–3073, Jul. 2009.

[3] “NR: multiplexing and channel coding (release15),” 3GPP, Sophia Antipolis, France. 3GPP Rep. TS 38.212V15.2.0 (2018–06). Jan. 2018. [Online]. Available: http://www.3gpp.org/ftp//Specs/archive/38_series/38.212/38212--f20.zip.

[4] I. Tal and A. Vardy, “List decoding of polar codes,” *IEEE Trans. Inf. Theory*, vol. 61, no. 5, pp. 2213–2226, May 2015.

[5] F. Ercan, C. Condo, S. A. Hashemi, and W. J. Gross, “On error-correction performance and implementation of polar code list decoders for 5G,” in *Proc. 55th Allerton Conf. Commun. Control Comput. (Allerton)*, Oct. 2017, pp. 443–449.

[6] K. Niu and K. Chen, “CRC-aided decoding of polar codes,” *IEEE Commun. Lett.*, vol. 16, no. 10, pp. 1668–1671, Oct. 2012.

[7] A. Balatsoukas-Stimming, P. Giard, and A. Burg, “Comparison of polar decoders with existing low-density parity-check and turbo decoders,” in *Proc. IEEE Wireless Commun. Netw. Conf. Workshops (WCNCW)*, Mar. 2017, pp. 1–6.

[8] G. Sarkis and W. J. Gross, “Increasing the throughput of polar decoders,” *IEEE Commun. Lett.*, vol. 17, no. 4, pp. 725–728, Apr. 2013.

[9] A. Alamdar-Yazdi and F. R. Kschischang, “A simplified successive-cancellation decoder for polar codes,” *IEEE Commun. Lett.*, vol. 15, no. 12, pp. 1378–1380, Dec. 2011.

[10] G. Sarkis, P. Giard, A. Vardy, C. Thibeault, and W. J. Gross, “Fast polar decoders: Algorithm and implementation,” *IEEE J. Sel. Areas Commun.*, vol. 32, no. 5, pp. 946–957, May 2014.

[11] M. Harif and M. Ardakani, “Fast successive-cancellation decoding of polar codes: Identification and decoding of new nodes,” *IEEE Commun. Lett.*, vol. 21, no. 11, pp. 2360–2363, Nov. 2017.

[12] C. Condo, V. Bioglio, and I. Land, “Generalized fast decoding of polar codes,” in *Proc. IEEE Glob. Commun. Conf. (GLOBECOM)*, Dec. 2018, pp. 1–6.

[13] G. Sarkis, P. Giard, A. Vardy, C. Thibeault, and W. J. Gross, “Fast list decoders for polar codes,” *IEEE J. Sel. Areas Commun.*, vol. 34, no. 2, pp. 318–328, Feb. 2016.

[14] S. A. Hashemi, C. Condo, and W. J. Gross, “A fast polar code list decoder architecture based on sphere decoding,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 12, pp. 2368–2380, Dec. 2016.

[15] S. A. Hashemi, C. Condo, and W. J. Gross, “Fast and flexible successive-cancellation list decoders for polar codes,” *IEEE Trans. Signal Process.*, vol. 65, no. 21, pp. 5756–5769, Nov. 2017.

[16] M. R. Ardakani, M. Harif, M. Ardakani, and C. Tellambura, “Fast successive-cancellation-based decoders of polar codes,” *IEEE Trans. Commun.*, vol. 67, no. 7, pp. 4562–4574, Jul. 2019.

[17] H. Zheng et al., “Threshold-based fast successive-cancellation decoding of polar codes,” *IEEE Trans. Commun.*, vol. 69, no. 6, pp. 3541–3555, Jun. 2021.

[18] Y. Ren, A. T. Kristensen, Y. Shen, A. Balatsoukas-Stimming, C. Zhang, and A. Burg, “A sequence repetition node-based successive cancellation list decoder for 5G polar codes: Algorithm and implementation,” *IEEE Trans. Signal Process.*, vol. 70, pp. 5592–5607, Oct. 2022.