DC-AC Inverter with Tap Changing Transformer

Mustafa H Mohsin 1, Nabil K Al-Shamaa 2

1 MSc. student in power engineering /electrical engineering technical college /middle technical university /Baghdad – Iraq.
2 Electrical engineering technical college /middle technical university /Baghdad – Iraq.

Abstract. In this paper a new single phase seven and eleven level inverter based on a tap changer transformer is developed to generates seven and eleven non-equal voltage levels from two DC sources. The model of inverter thus presented does not suffer from voltage balancing issues. The DC sources are connected to the primary side of the tap changer transformer with the help of a microcontroller circuit (Arduino UNO), with several semiconductor switches offering sequential modality. At the secondary side of transformer, the output voltage is generative, and Proteus/Software manipulation is performed. This technique reduces the Total Harmonic Distortion (THD) of the output voltage significantly.

1. Introduction

An inverter was introduced at the desired frequency and output voltage to convert power from DC to AC [1]. For high power low voltage applications, a multilevel inverter (MLI) plays a key role in the managing power electronics [2, 3] in terms of minimizing the Total Harmonic Distortion (THD), lower voltage impact on switches, and high voltage alienability, contributing to high performance applications and reducing switching losses. Such advantages recommend the use of MLI compared to the classic inverter [4, 5].

The principle of operation of a tap changer transformer is the same as for a normal transformer with the exception of the process being moved out from the anode situated between where the two ends of the lapping distributing transformer tap are connected. Where one side of the transformer, whether primary or secondary, contains more than one coil, this is known as a multicoil [6].

In this paper DC-AC conversion is done using a tap changer transformer. To generate non equal output voltage levels, the DC source is placed on the primary side of the tap changer transformer in sequential modality. An Arduino UNO is used to switch the relevant switches alternately on the primary side of transformer. Controlling the amplitude of the output voltage on the secondary side of transformer means that the output voltage is generative.

2. Sequential operation

Two DC sources for input are used, along with switches BDX54, BDX53; filter tap changer transformer; and load, as shown in figures 1 and 2.

The seven-level model uses six switches and three taps in the primary side of the transformer:
The eleven-level model uses ten switches and five taps in the primary side of the transformer, as shown in figure 2:

3. Operating principles for seven levels

3.1 Upper switches:

The microcontroller (Arduino UNO) sends the switches (throw 2N222 Drivers) S1 up to S3 gate pulses to shape a positive half cycle. At the secondary side of transformer, the output voltage thus increases. Switch S1 has the minimum output voltage as S1 connects to the DC source at the maximum primary turns of the transformer, given by

\[ V_2 = V_1 \frac{N_2}{N_1} \]  

where: \( V_2 \) is the output voltage and \( V_1 \) is the input voltage
In a similar manner, when S2 switches on, the output voltage increases as the primary turns of the transformer decrease. To complete the positive half cycle switching sequence, after S2, S3 is triggered and then S2 followed by S1. The output voltage reaches a maximum value as the minimum primary turns of the transformer are connected.

3.2 Lower switches:

The microcontroller (Arduino UNO) sends the switches (throw 2N222 Drivers) S4 up to S6 gate pulses to shape a negative half cycle. At the secondary side of the transformer, output voltage increases. Trigger S4 has the minimum output voltage because S4 connects the DC source at the maximum primary turns of the transformer. In a similar manner, when S5 switches, the output voltage increases as the primary turns of the transformer decrease. To complete the negative half cycle the switching sequence after S5 is S6, then S5 and then S4. The output voltage reaches the maximum value as the minimum primary turns of the transformer are connected.

The operating principles for seven levels resemble the operating principles for eleven levels, though in the latter, the number of switches in each batch extend from S1 to S5 for the upper switching pattern and from S6 to S10 for lower switching pattern.

4. Proteus /software

In the Proteus program, the tap changer inverter is presented as a tap changer transformer. BDX54 and BDX53 represent the switches, with 2N222 acting as drivers. An Arduino UNO is used as the microcontroller circuit, and the dc-ac circuit is as shown in figure 3.

![Figure3](image)

Figure3. Design for a seven-level dc-ac inverter.

The primary side of the transformer contain three taps, each connected with the middle of two switches (upper and lower). Figure 4 shows the pulses that shape the two half cycles.
Figure 4. The pulses from upper and lower switches before the seven-level primary transformer.

The secondary side of the transformer produces the output voltage, as illustrated in figure 5 (without filter):

Figure 5. Output voltage without filter for seven levels.
The output voltage with filter for the secondary side of transformer at 50Hz for seven levels is shown in figure 6:

Figure 6. Output voltage after filter for seven levels.

In the 11-level Proteus program, the tap changer inverter is presented as a tap changer transformer. BDX54 and BDX53 represent the switches with 2N222 drivers. The Arduino UNO represents the microcontroller circuit in the dc-ac circuit shown in figure 7.

The primary side of the transformer contain five taps, each of which is connected with the middle of two switches (upper and lower switches). Figure 8 shows the pulses which go out to shape the two half cycles.

The secondary side of transformer produces the output voltage, as illustrated in figure 9, with a rest period of 0.5 ms without filter. The matching output voltage with filter at 50Hz for eleven levels is shown in figure 10.
Figure 7. Design for an eleven-level dc-ac inverter.

Figure 8. Pulses from upper and lower switches before the eleven level primary transformer.
Figure 9. Output voltage without filter for eleven levels.

Figure 10. Output voltage after filter for eleven levels.

To illustrate the reduction of harmonics, a Fast Fourier Transform (FFT) analysis was done, as shown in figure 11.
5. Difference between models

In the seven-level model, six switches are used with three tap transformer and three low pass filters, to achieve three non-equal output voltages, while in the eleven level model, ten switches, five tap transformers, and five low pass filters are used to get five non-equal output voltages.

6. Conclusion

This paper simulated a novel DC-AC multilevel inverter using ISIS Proteus software. Frequency switching was found to reduce power losses and thus to increase the efficiency of the introduced topology. Compared with other topologies of multilevel inverters, the control offered by this technique is simple. The increase in tap transformer-generated voltage levels leads to the output voltage developing a sinusoidal signal, reducing in harmonics of the output voltage, as shown by FFT analysis.

7. References

[1] Butichi G, Lorenzani E, Franceschini G 2013 A five –level single phase grid –connected converter for renewable distributed systems (IEEE Trans Ind Electronics) vol 60 pp 906-16

[2] Ashan S H and Monfared M 2016 design and comparison of nine- level single- phase inverters with a pair of coupled inductors and two dc sources. J. IET. On Power electronics. 9 pp 2271-81

[3] Ashan S H and Monfared M 2015 Generalized single- phase N- level voltage- source inverter with coupled inductors. J. IET. On Power electronics.8 pp 2257-64

[4] Nguyen N V, Nguyen B X and Lee H H 2011 An optimized discontinuous PWM method to minimize switching loss for multilevel inverters (IEEE Trans Ind Electronics) vol 58 pp 3958-66
[5] Nguyen N V, Tu Nguyen T k, Lee H H 2015 A reduced switching loss PWM strategy to eliminate common-mode voltage in multilevel inverters (IEEE Trans Ind Electronics) vol 30 pp 5425-38

[6] Faiz J and Siahkolah B 2011 Electronic tap-changer for distribution transformers (London/New York: springer) p 1