Multiobjective Optimization of an Operational Amplifier by the Ant Colony Optimization Algorithm

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Abstract The Ant Colony Optimization (ACO) algorithm is used as a multi-objective optimization technique to size a most popular analog circuit, the CMOS operational amplifier (Op-Amp). The work consist of finding the more convenient transistors sizes, including the channel widths and lengths, in order to meet or reach the specified requirements such as the voltage gain $A_v$, the Common Mode Rejection Ratio CMRR, the die area A, the power consumption $P$ and the Slew Rate $SR$. SPICE simulations are used to strengthen and to validate the obtained sizing/performances.

Keywords Ant Colony Optimization, Multi-objective optimization, CMOS, Op-Amp

1. Introduction

Over the past decade, significant progress has been realized with the appearance of a new generation of powerful and approximate optimization methods, known as metaheuristics[1]. Such methods are used to solve real-world problems within a reasonable amount of time. They always offer ‘good’ approximation of the ‘best’ solutions for optimization problems[2]. One of the incoming problems to be resolved in the nearer future is the sizing of electronic circuits given the continuous increase of the integration densities. So, the designers and electronic engineers had a good and exciting challenge to reach, that is to find a technique, which can easily determine the components sizing, taken into account a well determined specifications. Some (meta-) heuristics were proposed in the literature and were used by some designers to optimize the sizing of the analog components automatically, such as Tabu Search[3,4], Genetic Algorithms (GA)[5], local search (LS)[6], Wasp Nets (WN)[7], Bacterial Foraging Optimization (BFO)[8], Particle Swarm Optimization (PSO)[9] and recently Ant Colony Optimization (ACO)[10, 11].

These algorithms have often dealt with single-objective optimizations; however, the optimization of analog circuits is generally a multi-objective problem. They are always formed by at least two conflicting performance functions.

That means that improving one performance results automatically into the degradation of another one. In this way a set of several meta-heuristics algorithms have been developed, such as Multi-objective Optimization Genetic Algorithm (MOGA)[12], Multi-objective Optimization Particle Swarm Optimization (MOPSO)[13].

In the domain of meta-heuristic methods, an important interest has been paid to the Ant Colony Optimization algorithm. The basic idea is to imitate the cooperative behaviour of ant colonies in order to solve combinatorial optimization problems within a reasonable amount of time, The ACO is actually recognized as one of the most successful strands of swarm intelligence[14]. Some ACO-based algorithms have been proposed such as the multi-objective optimization problems MOACO[15], the Multiple Objective Ant-Q Algorithm (MOAQ)[16], the Pareto-Ant Colony Optimization (P-ACO)[17] and the Ant Algorithm for Bi-criterion Optimization Problems[18].

In a previous work, we have adapted and used the MOACO algorithm for a two objectives electronic circuit optimization namely the Second Generation Current Conveyors[19]. At the present we propose to use the same algorithm in order to optimize the sizing of the CMOS Op-Amp, which is a more popular analog circuit requiring many highly interdependent performances.

Thus the subsequent section will present an overview of the ACO technique followed by with a presentation of the proposed adaptation of the ACO technique for analog circuits optimization and introduces the MOACO. The third deals with the optimal sizing of the CMOS Operational Amplifier (Op-Amp) and presents the main results and simulations. Finally, the paper will be concluded in the final section.

2. Algorithm Presentation

2.1. Ant Colony Optimization

The ACO technique is inspired by the collective behavior
of deposition and monitoring of some traces as it is observed in insect colonies [20,21], such as ants. It is for example well known that ants deposit pheromone on the ground in order to mark some favourable paths that should be followed by other members of the colony. Fig. 1 shows an illustration of the ability of ants to find the shortest path between food and their nest. Ants communicate indirectly through dynamic changes in their environment (pheromone trails).

\[ \eta_{ij} = \frac{1}{d_{ij}} \]  

(2)

Where \( d_{ij} \) is the distance between vertices \( i \) and \( j \).

The pheromone rate values are updated during each iteration by all the m ants that have built a solution in the iteration itself. The pheromone rate \( \tau_{ij} \), which is associated with the edge joining vertices \( i \) and \( j \), is updated as follows:

\[ \tau_{ij} = (1 - \rho) \cdot \tau_{ij} + \sum_{k=1}^{m} \Delta \tau_{ij}^k \]  

(3)

where \( \rho \) is the evaporation rate, \( m \) is the number of ants, and \( \Delta \tau_{ij}^k(t) \) is the quantity of pheromone laid ‘deposited, or dropped of’ on edge \((i,j)\) by ant \(k\):

\[ \Delta \tau_{ij}^k = \begin{cases} Q(t) / L_k & \text{if ant } k \text{ used edge } (i,j) \text{ in its tour, otherwise} \\ 0 & \end{cases} \]

The ACO approach attempts to solve an optimization problem by iterating the following two steps:

- The Candidate solutions are constructed using a pheromone model, that is, a parameterized probability distribution over the solution space;
- The candidate solutions are used to modify the pheromone values in a way that is deemed to bias future sampling toward high quality solutions.

2.2. Adaptation

The main idea consists of constructing a graph that imitates the movement of the ants[28,29]. Then, we construct a graph composed of the discretized variable vectors, corresponding to the graph vertices. Thus, each ant will construct its path by a random displacement from a variable value to another, as it is shown in Fig. 2; \( V_1, V_2, V_3 \ldots V_N \) constitute the discrete variable vectors.

\[ P_{ij}^k = \begin{cases} \tau_{ij}^k \cdot (\eta_{ij})^\alpha \cdot \eta_{ij}^\beta & \text{if } j \in J_i^k \\ \frac{1}{\sum_{i \neq k}^i \tau_{ij}^k \cdot (\eta_{ij})^\alpha \cdot \eta_{ij}^\beta} & \text{if } j \not\in J_i^k \\ \frac{1}{\sum_{i \neq k}^i \tau_{ij}^k \cdot (\eta_{ij})^\alpha \cdot \eta_{ij}^\beta} & \end{cases} \]

(1)

where \( J_i^k \) is the set of neighbours of the vertex \( i \) of the \( k \)th ant, \( \tau_{ij}^k \) is the amount of pheromone trail on the edge \((i,j)\), \( \alpha \) and \( \beta \) are weightings that control the pheromone trail \( \tau_{ij}^k \) and the visibility value, \( \eta_{ij} \) given by:

In short, each ant \( k \) will randomly chose a path (values of
In the multi-objective optimization problem, a set of non-dominated solutions form the Pareto frontier. An example is shown in Figure 3, where the solid (filled) circles represent the non-dominated solutions which form the Pareto frontier, while the open circles represent the dominated solutions. This result corresponds to a two-objective optimization problem, where the goal was the minimization of the two objectives, i.e. to search for the non-dominated solutions located along the Pareto frontier.

To resolve the multiobjective problems, we proposed the algorithm shown in Figure 4. In the initialization phase: Ants are generated each starting with a set $X$, the objective weights $P_k$ is determined randomly for each ant. In the construction phase of the algorithm, each ant tries to construct a feasible set $X$ by using a pseudo-random proportional rule. After a set has been constructed, its feasibility and efficiency is determined. Pheromone updating is performed by using the best solution $X_k$ of the current iteration for each objective $k$.

### 3. Operational Amplifier Optimization

The two-stage CMOS operational amplifier (Op-Amp) shown in Figure 5, is considered as an example for the validation of our proposed algorithm. In fact the design of the Op-Amp continues to pose a challenge as transistor channel lengths scale down with each generation of CMOS technologies.

Performances of an Op-Amp are evaluated via several parameters such as:

- The open-loop voltage gain $A_v$:
  \[
  A_v = \frac{2C_{sw}}{(\lambda_n + \lambda_p)} \sqrt{\frac{\mu_n \mu_p}{L}} \left(\frac{W}{L}\right)_b
  \]
  (5)

- The power dissipation $P$:
  \[
  P = (V_{dd} - V_{ss})(I_{bias} + I_3 + I_7)
  \]
  (6)
The Common Mode Rejection Ratio CMRR:

\[ CMRR = \frac{2C_{ox}}{(\lambda_n + \lambda_p)A_p} \left( \frac{\mu_n\mu_p}{4I_s^2} \right) \left( \frac{W}{L} \right)_s \]  

(7)

The die Area A:

\[ A \approx \sum_{i=1}^{k} W_iL_i \]  

(8)

The Slew Rate SR:

\[ SR = \min \left[ \frac{2I_s}{C_{c} + C_{C} + C_{TL}} \right] \]  

(9)

Those expressions (5) and (7), were obtained by considering the small signal equivalent transistor’s models. \( V_{dd} \) and \( V_{ss} \) are respectively the positive and the negative supply voltages; \( W_1-W_8 \) and \( L_1-L_8 \) are the gates widths and the channels lengths of the transistors \( M_1-M_8 \) respectively. \( I_{bias} \) is the bias current. \( g_m \) refers to the transconductance of the MOS transistor, \( C_{ox} \), \( \lambda_n \), \( \lambda_p \), \( \mu_n \) and \( \mu_p \) are technological parameters. \( C_C \) is a compensation capacitor and \( C_{TL} \) is the total capacitance at the output node which can be expressed as:

\[ C_{C} = C_{gd1} + C_{gd2} \]  

(10)

\( C_{gd1} \) and \( C_{gd2} \) denote to the parasitic grid to drain capacitance for transistor \( M_6 \) and \( M_7 \) respectively.

Determining the optimal dimensions of the transistors for a specific design involves a tradeoff among all these performance measures. Each transistor must be in saturation. Expressions (11)-(14) give the corresponding constraints, that have to be satisfied when computing optimal sizes of the transistors \( M_1 \) and \( M_2 \), \( M_3 \), \( M_4 \), \( M_5 \), \( M_6 \) and \( M_7 \) respectively.

\[ V_{out,\min} - V_{ss} - V_{TP} - V_{TN} \geq \frac{2I_s}{\mu_nC_{ox}\left( \frac{W}{L} \right)_s} \]  

(11)

\[ V_{dd} - V_{cm,\max} + V_{TP} \geq \frac{2I_s}{\mu_nC_{ox}\left( \frac{W}{L} \right)_s} + \frac{2I_s}{\mu_pC_{ox}\left( \frac{W}{L} \right)_s} \]  

(12)

\[ V_{out,\min} - V_{ss} \geq \frac{2I_s}{\mu_nC_{ox}\left( \frac{W}{L} \right)_s} \]  

(13)

\[ V_{dd} - V_{out,\max} \geq \frac{2I_s}{\mu_pC_{ox}\left( \frac{W}{L} \right)_s} \]  

(14)

where \( I_s = \frac{W}{L}_s I_{bias} \), \( I_f = \frac{W}{L}_f I_{bias} \), and \( I_t = \frac{I_s}{2} \) while respecting the expression (15):

\[ \frac{W}{L}_s \left( \frac{W}{L}_f \right)_s = \frac{1}{2} \frac{W}{L}_s \left( \frac{W}{L}_f \right)_s \]  

(15)

where, \( V_{pp} \) and \( V_{nn} \) are the PMOS and the NMOS threshold voltages, respectively.

This optimization belongs to the family of NP hard problems; in fact, there are 11 design parameters to optimize for the two-stage Op-Amp, the widths and lengths of all transistors, \( (W_1-W_8 \) and \( L) \), the bias current \( I_{bias} \) and the value of the compensation capacitor \( C_C \), in addition to the various constraints of the problem. Note that all the channel length \( L \) is considered the same for all the transistors.

The considered optimization problem is a typical multi-objective one, consisting of minimizing two objective functions (the die area and the consumed power), and maximizing the other performances.

| Table 1. Parameters of ACO algorithm |
|--------------------------------------|
| Number of iterations | 10000 |
| Number of ants (m) | 50 |
| Number of projects | 100 |
| Evaporation rate (\( \rho \)) | 0.1 |
| Quantity of deposit pheromone by the best ant (Q) | 0.2 |
| Phenomone factor (\( \alpha \)) | 1 |
| Heuristics factor (\( \beta \)) | 1 |

| Table 2. Optimal device sizing and performances |
|-----------------------------------------------|
| \( W_1 \) (\( \mu m \)) | 102.31 | 100.00 | 115.43 | 100.00 | 107.37 |
| \( W_2 \) (\( \mu m \)) | 75.22 | 84.98 | 74.48 | 82.38 | 78.12 |
| \( W_3 \) (\( \mu m \)) | 15.24 | 18.27 | 18.81 | 13.61 | 17.21 |
| \( W_4 \) (\( \mu m \)) | 105.41 | 119.02 | 115.87 | 109.18 | 123.54 |
| \( W_5 \) (\( \mu m \)) | 10.68 | 12.80 | 14.63 | 09.01 | 13.60 |
| \( W_6 \) (\( \mu m \)) | 15.07 | 17.98 | 14.48 | 19.95 | 20.13 |
| \( L \) (\( \mu m \)) | 0.82 | 0.95 | 0.88 | 0.90 | 0.92 |
| \( I_0 \) (\( \mu A \)) | 50.53 | 32.11 | 80.00 | 10.00 | 24.43 |
| \( C_C \) (\( fF \)) | 0.0848 | 0.1256 | 0.1500 | 0.0542 | 0.0810 |
| CMRR (dB) | 94.58 | 98.21 | 88.13 | 105.29 | 101.24 |
| \( P \) (mW) | 1.37 | 0.87 | 2.57 | 0.23 | 0.33 |
| SR (V/\( \mu m \)) | 112.40 | 13.28 | 112.40 | 115.87 | 119.02 |

| Table 3. SPICE performance results |
|------------------------------------|
| \( A_{\mu m} \) | 28.12 | 32.11 | 34.58 | 101.24 | 123.54 |
| CMRR(dB) | 1.37 | 0.87 | 2.57 | 0.23 | 0.33 |
| \( P \) (mW) | 103.44 | 95.46 | 86.07 | 103.44 | 99.31 |
| \( C_{\mu m} \) (\( \mu m \)) | 0.82 | 0.95 | 0.88 | 0.90 | 0.92 |
| SR (V/\( \mu m \)) | 112.40 | 72.33 | 241.45 | 1.37 | 0.87 |

Figure 6. Spice simulation results for Gain
The MOACO algorithm when applied to our optimization problem, using the parameter values given in Table 1, gives 43 optimal parameter designs. Table 2 present five of these parameter designs and their corresponding performances. Also, it is to be noted that the computing time equals 184s.

SPICE simulation results performed, using AMS 0.35μm technology, Voltage power supply is $V_{dd}/V_{ss}=+2.5 V/-2.5 V$, are presented in the Table 3; they show the good agreement with the expected ones.

Figure 6 shows SPICE simulation results for the five optimal designs, of the gain. The choice between the sets of the determined optimal parameters, given by this MOACO algorithm, will depend on the desiderata of the designer.

4. Conclusions

The presented work proposes an adaptation of the ant colony optimization technique to the optimal sizing of analog circuits. We show the practical applicability of the ACO to optimize performances of electronics integrated circuits and its suitability for solving a multiobjective optimization problem. The proposed algorithm is validated by the Operational Amplifier performances optimization. Viability of the technique was proved via SPICE simulations.

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