Principles towards Real-Time Simulation of Material Point Method on Modern GPUs

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Physics-based simulation has been actively employed in generating offline visual effects in the film and animation industry. However, the computations required for high-quality scenarios are generally immense, deterring its adoption in real-time applications, e.g., virtual production, avatar live-streaming, and cloud gaming. We summarize the principles that can accelerate the computation pipeline on single-GPU and multi-GPU platforms through extensive investigation and comprehension of modern GPU architecture. We further demonstrate the effectiveness of these principles by applying them to the material point method to build up our framework, which achieves 1.7×–8.6× speedup on a single GPU and 2.5×–14.8× on four GPUs compared to the state-of-the-art. Our pipeline is specifically designed for real-time applications (i.e., scenarios with small to medium particles) and achieves significant multi-GPU efficiency. We demonstrate our pipeline by simulating a snow scenario with 1.33M particles and a fountain scenario with 143K particles in real-time (on average, 68.5 and 55.9 frame-per-second, respectively) on four NVIDIA Tesla V100 GPUs interconnected via NVLinks.

CCS Concepts: • Computing methodologies → Physical simulation.

Additional Key Words and Phrases: material point method, GPU

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1 INTRODUCTION

Cinematic narratives in modern games and other real-time applications (e.g., virtual production, avatar live-streaming, and cloud gaming) are becoming increasingly extensive, causing a great demand for more refined visual effects production. Creating an atmosphere that meets the plots’ requirements for natural scenery may require realistic snow, sand, and water simulations.

On the other hand, using physical simulation to generate large-scale, plausible natural or character-related effects has become a standard in the production of films. Material point method (MPM) [Sulsky et al. 1994] is widely used due to its quantitative accuracy [Gaume et al. 2018] and strong generalization capability, enabling the plausible simulation of various complex materials and the coupling between them [Hu et al. 2019b; Jiang et al. 2016]. However, the computations required for high-quality scenarios are generally immense, deterring its adoption in real-time applications. Recently, to make the MPM more efficient, Gao et al. [2018] developed MPM on a graphics processing unit (GPU), and Wang et al. [2020] developed MPM on multiple GPUs. At the same time, Hu et al. [2019a] also revealed the Taichi framework, which is more convenient for developing MPM on the GPU.

Compared to MPM implementations on the CPU, these methods or frameworks have significantly improved the performance. However, there is still a gap between the achieved performance and the performance required by real-time applications. Besides, these works mainly focus on optimizing performance in the case of large numbers of particles. Few works have been done to minimize the extra cost of memory access or synchronization, which are critical for real-time applications that usually require a small number of particles but with a much tighter temporal budget.

In order to further improve the performance of GPU-MPM to reach the requirements of real-time applications, we provide four contributions:

(1) optimization strategies that significantly improve the performance of MPM on single or multiple GPUs, providing excellent scaling on a multi-GPU platform even when the number of particles is relatively small (e.g., less than 100K);
(2) ablation tests of various performance optimization strategies on GPU, proposed in either this article or previous works. Besides, we provide analysis in the aspects of hardware architecture and GPU instruction sets;
(3) choices of different strategies based on these test and analysis results, and a more efficient implementation for simulations at different scales, which achieves 1.7×–8.6× speedup on single-GPU and 2.5×–14.8× acceleration on four GPUs compared with the state-of-the-art [Wang et al. 2020]; and
(4) principles that summarize our choices to inspire further optimization of the performance of MPM and other similar methods.

2 RELATED WORKS

2.1 Material Point Method

The material point method (MPM) is a comprehensive simulation framework proposed by Sulsky et al. [1994]. MPM uses both Lagrangian and Eulerian representations and has been used in many
In this work, we adopt the material point method and focus on its code optimization on the GPU. Our optimization principles apply to MPM and also can be helpful to other similar frameworks using a mixed Lagrangian-Eulerian representation (e.g., fluid simulation with an implicit pressure solver [Bridson 2015]).

works in mechanics [Zhang et al. 2017] as well as computer graphics [Hu et al. 2019b; Jiang et al. 2016] to simulate complex phenomena including fluids, solids, and coupling between different materials. In this work, we adopt the material point method and focus on its code optimization on the GPU. Our optimization principles apply to MPM and also can be helpful to other similar frameworks using a mixed Lagrangian-Eulerian representation (e.g., fluid simulation with an implicit pressure solver [Bridson 2015]).

Fig. 1. Top: Sand Blocks. Blocks of sand with different sizes are dropped into a static, frictionless box, where particles simulated with different GPUs are colored differently. Bottom (from left to right): Timing per frame (in milliseconds, averaged over 60 frames) comparison between our implementation and Wang et al. [2020]’s, the latter’s percentage of additional costs per frame compared with ours, and the comparison of four-GPUs’ efficiencies computed through equation (1) from the averaged timings.
2.2 GPU Based Real-Time Physical Simulation

With the rapid development of computing architectures and software stacks, GPU has become a powerful tool in real-time physical-based simulation. GPU has the benefits of better energy efficiency and higher per-dollar performance. However, migrating a CPU simulation algorithm to the GPU without significant performance degradation is nontrivial. The GPU has SIMD architecture and unique memory models that require special treatment on memory access and program design.

Single GPU Simulation. Most research works focus on acceleration on a single GPU. Recently, there are research works using a single GPU to accelerate MPM solvers [Gao et al. 2018], Finite Element Methods (FEM) solvers [Bernstein et al. 2016; Wang and Yang 2016], Eulerian fluids solvers [Chentanez and Müller 2011; Cohen et al. 2010], pure-Lagrangian fluid solvers [Amada et al. 2004; Chen et al. 2015; Goswami and Neyret 2017; Macklin et al. 2014; Winchenbach et al. 2016], thin-film solvers [Vantzos et al. 2018], cloth solvers [Tang et al. 2016, 2018; Wang 2021; Wu et al. 2020], and other hybrid Eulerian-Lagrangian solvers [Chentanez et al. 2015; Wu et al. 2018]. Additionally, Hu et al. [2019a] proposed a framework where the user may write efficient simulation code on the GPU more easily.

Multiple GPU Simulation. A common expectation is that multiple GPUs can provide higher computational power and performance than a single GPU. However, physical simulation with multiple GPUs is more challenging than a single one due to the limited communication bandwidth. Besides, the overhead of launching a CUDA API (e.g., cudaMallocAsync) increases along with the number of CPU-GPU pairs due to the required sophisticated locking mechanism used in these APIs [Abe et al. 2014]. The overhead brought by multiple GPUs becomes even more significant when pursuing real-time simulation. The computational scale is usually tiny for real-time cases, and most time can be spent on communication if the code is not well optimized. Among the recent research, Herman et al. [2010] introduced a cooperative framework for interactive physical simulation using both multi-GPU and multi-CPU. They use a multiple-GPU abstract layer to handle memory transfer between different GPUs and handle job splitting dynamically. Junior et al. [2012] implemented an architecture for simulation of real-time fluid using the multi-GPU SPH method. They used a domain splitting method to distribute jobs to multiple GPUs and approached a 1.19×–1.8× speed up on two GPUs. For MPM, Wang et al. [2020] implemented a multi-GPU MPM, which mainly focuses on simulations with tens of millions of particles. More recently, Li et al. [2020] presented a multi-GPU cloth solver, which focuses on simulations with millions of triangles.

Most prior works focus on accelerating MPM simulation performed in a large-scale, off-line environment. This paper shows that a real-time MPM simulation may have different considerations, and we attempt to push multi-GPU acceleration to the real-time domain. We proposed several principles, with which a real-time four-GPU MPM simulation with 55K particles can be 14.8× faster than the state-of-the-art, and 2.5× faster for off-line simulation with 12M particles.

3 PRINCIPLES ON MODERN GPU

This section summarizes and briefly discuss the principles and leaves the elaborated study to later sections. For real-time high-quality physics-based simulation, we would like to assume that the graphics cards we used to have a large GPU memory size with NVLink connectivity [Foley and Danskin 2017] between each pair of them. While all principles are proposed for designing a highly efficient simulator (e.g., applying them to an incompressible fluid solver), in this work, we mainly focus on optimizing the pipeline of the explicit material point method to demonstrate their efficacy.

3.1 Single GPU

We summarize the principles for the computation on a single GPU as follows:

- Avoiding intrinsic functions without native hardware support.
- Reducing memory reallocation once the simulation starts;
- Minimizing the number of CUDA kernels executed within a single time step;
- Minimizing the synchronization between GPU and CPU;
- Fine-tuning the CUDA block size and the usage of on-chip memory.

The first three principles strongly impact the performance, from which the schemes derived contribute more than half of the performance improvement. A detailed ablation study is presented in §6.2.

Fig. 2. Top: A didactic kernel function adding a scalar atomically into shared and global memory; Bottom: The SM_70 disassembly (or Streaming ASSembl, SASS) of the compiled binary code. The (non-native) shared atomic add is emulated with a loop and an atomic compare-and-swap instruction (ATOMS.CAS), which are far more expensive than a single (native) global atomic add instruction (RED.E.ADD.F32.FITZ.RN). More details about the SASS instructions can be found in the instruction set reference [NVIDIA 2021a].

We begin our discussion of these principles with the intrinsic functions. Some of the intrinsic functions are not directly mapped to a single hardware instruction. Instead, they are emulated by dozens of instructions. We name these functions as non-native functions for brevity. For example, prior works [Gao et al. 2018; Hu et al. 2019a; Wang et al. 2020] rely heavily on atomic operations applied...
to floating-point shared memory variables. These operations are non-native and will be translated into complex instructions, e.g., branching and looping instructions (Fig. 2), which can be more expensive. We demonstrate in §4.3 that enforcing this principle by carefully redesigning the pipeline could deliver a substantial performance boost.

The second principle is straightforward, and some prior works (e.g., Tarjan et al. [2009]) have also emphasized this. More specifically, in scenarios with a small number of particles, without an optimized memory reallocation strategy, the memory reallocation (and the implicit synchronizations) would consume a longer time (Fig. 3) than the computational kernels themselves. Besides, it would also make the frame rate unstable and thus impact the user experience in interactive applications. However, it is also impractical to predict the necessary memory accurately or reserve all available memory for simulation. To minimize memory reallocation, we implement a GPU container similar to standard C++'s vector [Stroustrup 2013] that would automatically allocate memory with $4 \times$ of the requested size when it is half-filled.

To maximize the performance, we minimize the number of CUDA kernels executed within a single time step, where two different ways can be applied. The first way is merging smaller kernels into a larger one. This idea is not new and has been discussed in Wang et al. [2020]. The second way is less evident than the first. We can divide the kernels per time step into two groups: the essential and non-essential groups. While the former is inevitable, kernels in the latter group are unnecessary to be conducted every step. In the context of MPM, we show in §4.2.1 that the kernels rebuilding the mapping between particles and grid nodes are non-essential and can be invoked with a much lower frequency to achieve significant computational savings.

For most kernels, GPU and CPU work asynchronously. Issuing a kernel on the CPU usually takes much less time than executing it on the GPU, leading to a temporal difference between the invocation and execution. However, there are cases where a CPU-GPU synchronization is necessary. When there is a CPU-GPU synchronization, the time gap accumulated from the previous asynchronous executions would suddenly appear, causing the GPU to stall: the gap makes the GPU idling before the subsequent kernel execution (also known as a pipeline bubble, Fig. 4). We put as much work as possible on GPU. Besides, the necessary data transfer from GPU to CPU mostly happens when building data structures. For example, when building the particle-node mapping, the CPU code needs to know the number of particle blocks to determine how many CUDA threads need to be launched for the following kernels or if the memory needs to be reallocated. To reduce CPU-GPU synchronizations, we eliminate the rebuilding of such data structures as many as possible.

On a streaming multiprocessor (SM), the register file and shared memory size are limited. The more a CUDA block (containing several warps of threads) uses shared memory or the more each thread uses registers, the less number of CUDA blocks will be simultaneously active on the SM. As a result, the SMs will be less occupied, leading to worse efficiency. Therefore, we fine-tune the number of CUDA blocks used for each kernel and the balance between registers and shared memory usage. It is a common practice to cache data with shared memory. However, it is less well-known that spilling some registers into shared memory in a complex kernel (that may use too many registers by default) also helps increase occupancy (and thus efficiency). In the context of MPM, we spill the B-spline weights (nine floats for each thread) by storing them into the shared memory (instead of registers), although none of them is shared between threads. This choice increases performance, particularly when the number of threads is large (§6.2.5).

3.2 Multiple GPUs

Our principles proposed for a single GPU also apply to the case when simulated on multiple GPUs. For example, frequent memory reallocations cause even more severe overhead in a multi-GPU environment (§6.3.1). Nevertheless, there are additional considerations for performance optimization in a multi-GPU environment. Unbalanced work distribution among GPUs would detriment the performance. GPUs with less workload may stay idle while other GPUs keep busy, wasting the overall computing power. In the ideal case, the workload would be dynamically divided into even slices and redistributed to GPUs every few steps. For example, in a smoke simulation, the workload covers several spatial blocks that change every step as the smoke rises, so the slices must be recalculated every few steps. For MPM, as the computational workload is closely related to the number of particles, we divide the initial set into pieces with the equivalent number of particles based on their initial position. We then assign each piece of particles to one GPU and keep this partition unchanged throughout the simulation. We demonstrate that this simple partitioning scheme provides a balanced workload for scenes used in this paper. However, dynamic particle partitioning should be introduced for extreme cases where particles from different GPUs can get evenly mixed, e.g., by rotating a paddle in the middle of a container. We leave it as future work.

We propose a few principles that maximize the performance of real-time applications on multiple GPUs. The first and most important principle is that one should always try to make each GPU process independently and only transfer information between different GPUs when inevitable. We further categorize all these principles into what and how to transfer among multi-GPUs for a more straightforward interpretation. A detailed ablation study on the impact of these principles is presented in §6.3.

- Minimizing the number of transfers and synchronizations between GPUs;
- What to transfer?
  - Minimizing the amount of data transferred between the GPUs and the subsequent computations;
- How to transfer?
  - Using in-kernel peer-to-peer (P2P) read/write operations for inter-GPUs communications;
  - Overlap P2P data transfer and computation through warp-interleaved execution when using NVLinks

The inter-GPU communications always appear with inter-GPU synchronizations. Communications are accomplished via either reading or writing between GPUs. When a GPU writes to some other GPUs, a post-write synchronization would be necessary to
Fig. 3. A screenshot of Nsight System analysis of an MPM simulation with 55K particles. Memory reallocations can take up a large proportion of a time step (even much larger than the actual computations), which is more likely to occur when the particles get stretched and cause the particle-node mapping to be rebuilt.

Fig. 4. A screenshot of Nsight System analysis of an MPM simulation with 55K particles. A GPU-CPU synchronization performed through cudaEventSynchronize waits for a G2P transfer to complete on the GPU, delaying the later kernel invocations on the CPU. As a result, a gap between the invocation and execution (or a pipeline bubble) appears.

ensure the receivers get the information from the sender. Similarly, when a GPU reads from some other GPUs, a pre-read synchronization would help it know that all the data to be collected are in place. Concurrent reading and writing from/to the same address among GPUs should be avoided.

The inter-GPU synchronizations usually involve locks between multiple streams and contexts which create pipeline bubbles on the GPUs, i.e., causing GPUs to stall. Thus, in general, the number of synchronizations between GPUs should be minimized. When synchronization is unavoidable, a common choice is directly using the cudaMemcpy API. However, as this API relies on sequential CPU mutexes to avoid deadlock, the cost would quadratically increase w.r.t. the number of GPUs. Furthermore, it would be unacceptably expensive for scenes less than 100k particles since the computations would not cover the cost. We instead implement inter-GPU synchronization by creating a barrier across different GPUs via system atoms over NVLinks (or effectively, a spin lock), and it does not need to have the CPUs involved. As shown in Fig. 5, while the two schemes provide similar performance with a large number of particles, ours delivers much better efficiency with around 50k particles.

The second principle emphasizes that the amount of data transferred between GPUs should be minimized. Each thread is in charge of a particle in the particle-grid transfer (P2G) of MPM. When threads from different GPUs write to the same set of nodes, the values of these nodes held by each GPU need to be combined to get the final values.

There are two ways to combine the values from different GPUs. One way is to duplicate the data on particles and transfer them among GPUs before P2G. Then each GPU can process both the particles from itself and the transferred as usual without interfering with the other GPUs. Another way is to apply a simple reduction with the other GPUs. In this way, the tagging scheme used in the second option is much more lightweight and brings much less overhead.

Fig. 5. Top: A GPU spin lock kernel for the synchronization between different GPUs. The kernel is executed with a single thread on each GPU, the GPU id, number of GPUs, and a pointer to integer-sized device memory as the parameters. Bottom: Timing (in milliseconds) comparison between our implementation and the one with cudaMemcpyAPI, as well as the percentage of additional costs incurred by the latter.
The last set of principles consists of two aspects about how exactly the inter-GPU transfers should be achieved. For transferring data among GPUs, specifically for scenes with a small number of particles, in-kernel peer-to-peer (P2P) accesses should be preferred than dedicated copy engines such as a bunch of cudaMemcpy-s or the NCCL library [Jaegye 2017], as the latter brings in an extra invocation cost. Furthermore, SMs on modern GPUs can efficiently switch between executing warps waiting for a P2P transfer and warps conducting computations. Therefore, we fuse the P2P copying with some computations into a single kernel and rely on GPU’s interleaved warp execution to overlap data transfer and computations.

Remark: The last one seems to be controversial as it is almost a standard way in high-performance computing (HPC) to hide device-to-device communication costs via manually splitting data transfer as an independent stream and overlapping it with computations [Wang et al. 2020]. However, multiple streams would work best if the communications consume roughly the same amount of time as the computations or within specific copy engines that have logic control units running in parallel with the computational units (e.g., MPI for a CPU-GPU heterogeneous framework [Dominguez et al. 2013]). For (nearly) real-time simulations, the situation is different. The total amount of data on each GPU is much smaller than the amount that needs to be considered in HPC applications in the first place. Furthermore, only a tiny portion of it needs to be transferred between GPUs, making the communication cost only a tiny fraction of computational cost. The P2P data transfer, although very efficient, also occupies SMs. Thus, manually splitting a kernel into two kernels, i.e., a P2P kernel and a computation kernel, would not be beneficial.

### 4 MATERIAL POINT METHOD ON A SINGLE GPU

![Timing comparison chart](image)

**Fig. 6.** Left: Timing (in milliseconds) comparison between our implementation and the one where mapping between particle and grid are rebuilt every step. Right: The percentage of additional cost incurred by rebuild-mapping per step.

Some prior works [Gao et al. 2018; Hu et al. 2019a; Wang et al. 2020] also focus on optimizing the material point method on GPUs. All of them share a similar procedure that contains the following phases for each time step:

1. **Rebuild-mapping**: building up the mapping between particles and background grid blocks;

2. **Sort-particle**: sorting particles to the appropriate level of granularity: the level of cells [Gao et al. 2018] or the level of blocks [Hu et al. 2019a; Wang et al. 2020];

3. **Transfer-particle-to-grid**: transferring particle momenta and masses to grid nodes and computing nodal forces;

4. **Update-grid**: updating nodal velocities and resolving collisions on grid nodes;

5. **Transfer-grid-to-particle**: transferring new velocities back to particles from grid nodes and advecting particles.

The rebuild-mapping phase consists of several substeps. First, we compute particle codes from particle positions, and we adopt a simplified version of (GPU) SPGrid [Gao et al. 2018; Setaluri et al. 2014] that interleaves the three-dimensional 32-bit indices of particles into a 64-bit offset. The higher bits encode the block information (block code) while the lower bits encode the cell information (cell code). With the particle codes, we construct a hash table to record all blocks in which particles reside (named as a geometric block [Gao et al. 2018], or gblock). Next, we update the hash table by recording all the $3 \times 3 \times 3$ neighboring blocks of each geometric block. These blocks, including the gblocks and their neighboring blocks, cover all the nodes the particles may talk to through B-spline quadratic weighting functions. We name this group of blocks as physical blocks (pblock), of which the gblocks are a subset. These pblocks are sparsely populated in space while they are consecutively stored and indexed in memory. In this work, the block code would have a sense of space while the block index is used to record the block’s memory location; and we update the mapping between them during the rebuild-mapping phase.

As the shared memory has a limited size on streaming multiprocessors, prior works [Gao et al. 2018; Hu et al. 2019a; Wang et al. 2020] require that the particles handled by a CUDA block should come from the same particle block so that the amount of shared memory allocated to each CUDA block can be reasonably small. To achieve this, Gao et al. [2018] partition the particles from the same particle block into a few CUDA blocks and name such CUDA blocks as “virtual blocks” (or vblock). In contrast, as our pipeline gets rid of shared memory (refer to §4.3 for details), we divide particles by the warps. We only require the particles in the same warp are originated from the same particle block in the rebuild-mapping phase, and each CUDA block can handle warps from different particle blocks.

There are several choices of algorithms for sorting particles. Radix-sort using particle codes as keys is the simplest. However, as discussed by Gao et al. [2018], a histogram-sort performs more efficiently, where the keys are computed through concatenating the block index and the cell code. Therefore, we adopt the latter for sorting particles. Unlike prior works [Hu et al. 2019a; Wang et al. 2020] that only sort the particles to the granularity of blocks, in this work, we sort the particles to the granularity of cells. There are two benefits of this choice. First, processing particles that are sorted w.r.t. cells during the P2G and G2P transfer is more efficient since we can read from or write to consecutive memory (see §6.2.3 for validation). Second, it enables using the warp-level reduction before atomically writing data to nodes [Gao et al. 2018] for expedited particle-to-grid (P2G) transfers, which leads to much less atomic operations compared with works using block-level sorting.
The P2G kernel also computes each particle’s plasticity, stress, and body force before conducting the actual P2G transfer. After P2G, the computations on the grid nodes take the collisions with boundaries into consideration to update the nodal velocities. Then the final grid-to-particle (G2P) phase transfers the velocities back to particles.

4.1 Merge Kernels

The key benefit of merging kernels is that specific global memory accesses can be avoided for the variables that are not part of the system state. For example, the stresses computed on particles are temporary states used to compute the nodal forces and do not need to be stored in the global memory for the next step, and therefore, we can compute the stresses with P2G in the same kernel.

This idea of merging kernel is not new and first employed by Hu et al. [2019a] that they postpone the update of deformation gradient at the end of G2P to the beginning of P2G to avoid the redundant write operations. Wang et al. [2020] move one step further to merge quite a lot of kernels into a single large kernel - the G2P2G kernel.

Nevertheless, a complicated kernel may also introduce additional costs or limitations in certain situations. For example, it would be challenging to simulate Lagrangian MPM models (e.g., hair or cloth [Fei et al. 2021; Guo et al. 2018; Jiang et al. 2017]) with a G2P2G kernel, as some of these models require sophisticated modifications to the particles’ velocities before P2G. Also, operations such as the addition and deletion of particles are not easily supported in G2P2G as they usually happen between G2P and P2G, forbidding particle sources or dynamic particle boundaries [Huang et al. 2021; Stomakhin and Selle 2017]. In the result section, we have also conducted one experiment to illustrate that combining G2P2G with our current pipeline would only deliver better performance when the number of particles is relatively small. We observed that the compiled SASS code of G2P2G is extended and contains some long-distance jumps. When there are many particles so that there are many warps to be executed, the execution between warps can vary, requiring a large instruction cache. Because the latter is limited, a dramatic increase of instruction cache miss is observed, which can be justified by a noticeable rise of stall no instruction in Nsight Compute analysis.

To avoid these drawbacks of G2P2G, we separate the two transfer phases unless there are no particle additions or deletions and the number of particles is small (e.g., less than 100K in this work). However, we merge all computations on particles, i.e., singular value decomposition, plasticity projection, stress computation, into a single P2G phase.

Another benefit that is less discussed is that by merging small kernels into an appropriate size, the stream multiprocessors (SMs) can overlap memory accesses with computations for better performance through warp scheduling. The latter is efficient and costs only one cycle to switch between two warps [Jia et al. 2019]. For example, the P2G kernel overlaps the writing operations at its end with the computations at its beginning.

Besides, when the simulation resolution is small, there are only a limited number of thread blocks. The SM groups thread blocks into a specific size (known as a wave) and execute the thread blocks wave by wave. Without merging kernels, the thread blocks would not have enough computations; the limited number of threads in the last wave makes SM idling, wasting a large portion of computational power. Such inefficiency is also known as the tail effect [Micickevicius 2012]. With merging, these trivial computations can be executed and overlapped with other heavier computational or memory operations, eliminating the tail effect and drastically improving the overall performance.

4.2 Minimize nonessential computations

As mentioned in the previous section, the computations per time step can be divided into two groups. Specifically, for the five phases of the material point method, we regard the first two as the nonessential ones and the other three as the essential ones. While the essential phases would always stay in place, the nonessential phases can sometimes be removed to save the cost of performing them. One may naively remove them to ignore rebuild-mapping and use a dense background grid or remove the particle sorting not to concern the performance of the memory operations. Such naive ways, however, would always bring some other side effects that impact the overall performance.

Instead, in this work, we develop a new method that vastly reduces the frequency of these two nonessential phases to achieve substantial computational savings without bringing other side effects. In other words, instead of running them every time step, we can now conduct them once every few time steps with appropriate modifications.

4.2.1 Rebuild-Mapping. We start with the scheme proposed in Gao et al. [2018] to rebuild mapping between the particles and nodes: particles are initially divided/sorted into non-overlapping particle blocks. As shown in Fig. 4 of Gao et al. [2018], a particle block is shifted by half-\(dx\) w.r.t grid block, such that the particles assigned to this particle block will touch and will only touch the nodes of its \(2 \times 2 \times 2\) neighboring blocks. A particle’s assigned block can then be found by right-shifting its code only to keep the higher bits, and the neighboring blocks can also be retrieved either via the hash table or via an explicitly stored vector. In the next step, as particles advect, some may end up with positions outside their original particle block and need to talk to the nodes that are not tracked. Thus, rebuilding the mapping between particles and grid blocks is inevitable.

We observe that the aim of rebuild-mapping is not to find the grid block in which a particle resides but rather to provide the memory addresses of the neighboring \(27\) nodes with which the particle will interact through a quadratic kernel. If the moving range of a set of particles is known and fixed in a few steps, one may find all nodes that possibly interact with these particles and build the mapping between them once for all these steps.

In this work, we allow the particles to move within a \((10dx)^3\) range (named as a free zone, see Fig. 8 for an illustration) without triggering rebuild-mapping. Instead of \(2 \times 2 \times 2\) neighboring blocks, we divide particles into blocks with a negative-half-\(dx\) shifting and keeping track of its \(3 \times 3 \times 3\) neighboring blocks. As long as the particles move in the free zone, they are free from rebuild-mapping.

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1When the simulation resolution is large, the tail effect will fade out as the number of waves becomes large. Hence, the discussion here only applies to the case where simulation resolution is small.
In other words, all grid nodes with which the particles communicate are known, and their addresses can be computed from the blocks’ codes.

Our scheme can substantially reduce the frequency of rebuild-mapping. The CFL condition usually prevents particles from traveling a distance longer than the cell size \( dx \) within a time step, and thus using a free zone with \( 10dx \)-width may potentially reduce the frequency of rebuild-mapping from every step to per four steps (assuming the extreme case, e.g., a particle on the edge of a dual block moves away from the block with one \( dx \) per step). In our test case where each frame contains 36 steps (§6), however, we observed the rebuild-mappings happen only every 10–30 steps, and each frame only needs 1–4 rebuild-mappings.

Wang et al. [2020] proposed a similar idea to allow transferring particle properties to grid nodes after advection within the G2P2G step as it is impossible to rebuild the mapping inside a kernel. However, they still conduct the rebuild mapping every time step. They use \( 2 \times 2 \times 2 \) blocks with one-and-half \( dx \) shifts, while our free zone is designed with a larger size to reduce further the frequency of rebuilding. One can push to use more neighboring blocks than we do, and the extreme would end up with a dense background grid, where the rebuild mapping can be removed entirely.

Our scheme takes a longer time to hash more neighboring blocks. However, the hashing only happens during rebuild-mapping. Because we only rebuild mapping over a few steps, the cost of the entire rebuilding is amortized to these steps and becomes negligible. Additionally, to avoid handling more physical blocks, we mark the physical blocks that are not touched by any particles and skip them during the grid computations. In our experiments (Fig. 6), when the number of particles is small, i.e., 55.3k, the rebuild-mapping itself is the bottleneck, and our free zone scheme alone brings 3.7x acceleration.
4.2.2 Particle Sorting. In the particle-to-grid step, particles in the vicinity could simultaneously write to the same grid nodes, leading to writing conflicts. The simplest way to enforce correctness is to use CUDA atomic operations; however, the performance can be severely compromised without careful treatment. Two different types of solutions have been proposed to reduce the total number of atomics at any instant. Prior works [Hu et al. 2019a; Wang et al. 2020] either leave particles unsorted at the cell level or adjust their order with shuffling or binning strategies, such that particles within the same warp would have a smaller chance to conflict. On the contrary, Gao et al. [2018] sort particles into cells and then apply a warp-level reduction to fuse multiple atomic operations into one. We adopt the second way as it is more robust towards extreme scenarios. For example, when particles get tightly compressed into one cell, the first method would fail to alleviate conflicts.

In a CUDA warp, 32 threads handle 32 particles in parallel. When particles are randomly ordered, the 32 threads would have a better chance to write to different grid nodes at one instant. However, as we sort the particles into cells, several subgroups usually exist among the 32 particles; threads inside each subgroup write to the same node. Reductions are independently conducted per subgroup, and then the first thread in each subgroup is responsible for writing the reduced result back to the grid node. In this way, each subgroup ends up with only one atomic operation.

A complete particle sorting can be divided into two phases: sort the particles w.r.t. particle blocks and then sort w.r.t. cells. We modify the first one to be compatible with the free zone, i.e., as long as the particles stay inside the free zone, there is no need to sort the particles into blocks.

Furthermore, as the reduction only helps to lessen the atomic operations within each warp, instead of sorting w.r.t. cells every time step, we can perform it only when rebuild-mapping happens. Between two rebuild-mappings, we conduct radix sort in each warp before the reduction in P2G transfer. This arrangement splits sorting w.r.t. cells further into two substeps: sorting in each warp and then sorting between warps, and the latter can be avoided in most time steps. Notice that instead of using 32 bits for warp-level radix sort, we only need 10 bits for better efficiency as our free zone spans a domain with (10dx)3.

Our new scheme may present a less optimal particle ordering, e.g., particles in the same cell can be distributed to several warps, resulting in several atomics instead of one. However, this performance loss can be compensated well when particle density is not extremely high in each cell. We avoid the complete particle sorting, which may possess quite a fraction of the whole pipeline, leading to 8%−17% acceleration across different resolutions.

4.3 Avoid non-native intrinsics

Prior works [Gao et al. 2018; Hu et al. 2019a; Wang et al. 2020] adopt two types of atomic operations in the P2G step. Values such as weighted momenta transferred from particles to grid nodes are first added up in the shared memory by non-native atomics (Fig. 2) to get intermediate results. They are then written back to global memory through native atomics to reach the final results. However, non-native atomics are much slower than the native ones as they are not supported by the (latest generation of) hardware. Atomics of floating-point numbers performed on shared memory are emulated by a read-modify-write (RMW) operation using the atomicCAS instruction.

Furthermore, the adoption of shared atomics also imposes constraints that may contradict our rebuild mapping scheme. The shared memory needs to be sufficiently large to store the data of all nodes with which the particles in a block may interact. However, as the streaming multiprocessor (SM) has a limited size of shared memory, kernels using a large shared memory will be executed with fewer active CUDA blocks. To make the required shared memory size acceptable, prior works [Gao et al. 2018; Hu et al. 2019a; Wang et al. 2020] limits the size of neighboring blocks as 3 × 2 × 2 and require each CUDA block only to handle particles from a specific grid block. Instead, our rebuild mapping scheme uses 3 × 3 × 3 neighboring blocks, which would require a shared memory size that significantly reduces the number of active CUDA blocks, leading to a dramatic performance loss.

Following the principle of avoiding non-native atomics, we directly write back to global memory via native atomics when computing transfers from one particle to one grid node. We achieve 3×−5× acceleration (Fig. 10). Besides, 3 × 3 × 3 blocks are now compatible with the free zone without fretting the memory size limitation. The multiprocessor occupancy is also improved by allowing a CUDA block to handle warps from different particles blocks. Furthermore, there is no need to synchronize threads before writing from scratchpad to global memory anymore. Warp that finish their work sooner would not need to stall but immediately switch to new tasks. Similarly, we also get rid of the shared memory in the G2P step.

Besides atomic functions, some other non-native intrinsics should also be avoided when possible. In CUDA, by default, the floating-point operations like \( \frac{\sin(x)}{x} \), \( \sinf(x) \) and \( \logf(x) \), are designed to match IEEE 754 precision standard [IEE 2019]. To achieve this precision, the compiler will map these math functions to dozens of instructions. In cases where precision is not critical, the _use_fast_math compile flag can be used to utilize native intrinsic functions, which can save a lot of instructions and register costs (refer to §6.2.9 for detailed comparisons). In Fig. 11, we compare the stress computed with and without fast-math intrinsics over 60 frames in the case with 3.1M falling sand particles (refer to Fig. 1). The error brought by fast-math intrinsics is negligible (the absolute error is at most 0.12dyne/cm²), especially when the stress itself has a considerable magnitude. In practice, we did not observe any noticeable visual difference between the two simulations.

5 MATERIAL POINT METHOD ON MULTIPLE GPUs

In multi-GPU applications, the efficiency is defined as [Kraus 2019]

\[
e = \frac{t_1}{n \times t_n}
\]

where \( t_1 \) and \( t_n \) are the time consumed with only one GPU and with \( n \) GPUs respectively. In general, we have \( e \leq 1 \). \( e \) only reaches 1 (or 100%) in the ideal case, where \( n \)-GPUs produce \( n \)-times performance scaling, making \( t_n = t_1/n \). The closer \( e \) gets to 1, the better a multi-GPU implementation/algorithm would be. As the first effort
of optimizing MPM on multiple GPUs, Wang et al. [Wang et al. 2020] build up a working pipeline from scratch and deliver good performance. Following the principles proposed in §3.2, we adopt several new schemes that successfully push the efficiency of our pipeline closer to the ideal case, as shown in Fig. 1.

5.1 Tag shared and non-shared blocks

Wang et al. [2020] tagged a block into three different types, assigned blocks in which particles reside, transferred block to which the particles may write, and advected blocks to which particles may advect. Based on this tagging, they also identify the "halo regions" containing overlapping blocks on two or more cards. Instead of using such a sophisticated scheme, in this work, we adopt a much simpler scheme that is far less time-consuming.

We tag blocks into two types: blocks shared by other GPUs and blocks not shared by any GPUs. Blocks with the latter type can be processed similarly as blocks on a single GPU, while shared blocks also need a pass of data reduction after P2G transfer. To identify the shared blocks, we maintain a list storing all the block codes on each GPU during the construction of the hash table. An inter-GPU synchronization is enforced right before the tagging to guarantee that the code lists from all GPUs are in place. Then each GPU reads block codes from other GPUs via peer-to-peer (P2P) read operation, computing their spatial indices through block codes. For each incoming block, we then check whether its code already exists in the local hash table: if so, both its source GPU id and memory address are recorded for later reduction. As we adopt P2P read, on each GPU, our tagging step is entirely independent of all other GPUs, i.e., after the tagging step, each GPU can move forward without a second inter-GPU synchronization that may stall the devices.

Wang et al. [2020] conducted tagging by copying data through cudaMemcpy both between GPU and CPU and between GPUs along with multiple CPU-GPU and inter-GPU synchronizations. On the contrary, our method is relatively lightweight and only requires one inter-GPU synchronization, leading to 5× acceleration per step as shown in Fig. 16. Due to our free-zone scheme (§4.2.1), this tagging step is conducted only when rebuild-mapping happens (while transfers among GPUs are still performed every time step), which tremendously reduces the cost per frame as demonstrated in Fig. 17.

5.2 Compute the reduce sum on shared blocks

For each time step, as the values on the nodes of shared blocks are distributed to different cards, a reduction operation has to be applied across multi-GPUs to get the correct nodal values. By following the
multi-GPU principles, we propose a method that is both lightweight and quite efficient.

For collecting nodal values stored on shared blocks from different GPUs, we synchronize all GPUs right after the P2G step as peer-to-peer read operation will be used in the reduction step. This operation is the only inter-GPU synchronization required in each step if the rebuild mapping is not initiated. We further fuse the reduction with the original nodal computations (i.e., updating nodal velocities and resolving collisions) into a single kernel to overlap the inter-GPU communications and local computations through warp scheduling, which provides better performance (refer to §6.3.2 for statistical details).

To ensure each GPU proceeds independently and avoid data race, we adopt a double-buffering strategy to isolate the local reduction on each GPU. Specifically, we allocate two buffers for the P2G transfer and inter-GPU reduction. We store the results from each GPU’s P2G on the second buffer. For each shared block, we then read the copies of this block from other GPUs’ second buffer via P2P-reads, add

**Remark.** Our method effectively conducts multiple reductions for the same shared pblock. An alternative is to compute and store on a single GPU while directly writing the values to other GPUs via P2P-atomics, which removes the need for an additional buffer. However, inter-GPU atomics with a large portion of data may need many (implicit) synchronizations between GPUs [Abe et al. 2014], which can be very ineffective (§6.3.4).
some of them may seem to be controversial. While the final pipeline delivers quite a massive boost in performance compared to state-of-the-art [Wang et al. 2020], a thorough ablation study would help researchers understand the effect of every single modification.

The machine we use to run the benchmarks is an NVIDIA DGX-1. While there are eight Tesla V100 GPUs in total, they are divided into two groups, and only the GPUs in the same group have fully connected NVLinks. As a result, we test up to four GPUs in the same group. The DGX-1 has two Intel Xeon Platinum 8255C CPUs running at 2.50GHz, and each of them has 24 logical cores and 48 threads. The operating system is CentOS 7, the GPU driver version is 460.32.03, and the CUDA version is 11.2. We turn on the compiler option –use_fast_math to use native intrinsics by default.

We begin our profilings with a highly dynamic scenario containing several Sand Blocks (Fig. 19). With the cell size being fixed, one, four, or sixteen cubic boxes of sand particles are dropped into a container so that the particles collide with the frictionless boundary and with each other to generate energetic dynamics. We simulate 60 frames, and each frame has a duration of 1/48 seconds. We fix the time step size to $5.787 \times 10^{-4}$ seconds such that each frame consists of 36 time-steps. We report the average cost per frame across the entire 60 frames. For the multi-GPU profilings in this scenario, we compute the longest axis of the particle cluster and sort the particles along with this axis. Then we divide the particles by their indices and distribute them evenly onto four GPUs.

### 6.1 Compare with state-of-the-art

Our final pipeline is compared with the one proposed in Wang et al. [2020]. As shown in Fig. 1 (bottom), their implementation consumes much more time than ours, ranging from 96% to 1385%. Our pipeline is exceptionally faster than Wang et al.’s when the number of particles on each GPU is small.

We also compare the four-GPU efficiencies (the capability of scaling) between our final pipeline and the one proposed in Wang et al. [2020]. We compute the efficiency $\varepsilon$ through equation (1) from the averaged timings. Our multi-GPU pipeline almost reaches the ideal case (i.e., $\varepsilon = 1$) when the number of particles is large (96.3% for 12.6M) and keeps an acceptable efficiency when the number of particles is small (38.8% for 55.3K). On the contrary, Wang et al.’s efficiencies drop to less than 25% when the simulation contains less than 389.3K particles, indicating too much overhead in their multi-GPU pipeline, making their four-GPU simulation even slower than their 1-GPU simulation.

**Remark:** In this subsection, we adopt G2P2G when the number of particles per GPU is less than 100K (with either multiple GPUs or a single GPU) as the instruction miss rate is still tolerable.

### 6.2 Ablation study on a single GPU

In the following sections, we perform an ablation study on our final pipeline. We roll back and remove a single scheme derived from our principles and compare its performance with our final pipeline. We adapt from the open-source code that the authors released on GitHub, https://github.com/penn-graphics-research/claymore, commit 4a6b0cf on Nov. 21, 2020, adding our benchmark scenario and the neo-Hookean sand model from Yue et al. [2018].
6.2.1 Reduce memory reallocation. In Fig. 20 we show that our memory allocation scheme effectively reduces the need for reallocation and dramatically eliminates overhead. We compare with other schemes that are commonly adopted. For example, suppose we only allocate to the required size (in other words, we never allocate more than necessary). In that case, the overhead is 15%–136% for simulation on a single GPU. On the other hand, if we always reallocate by each step, regardless of the allocation size, the overhead would increase up to 161% on a single GPU. More discussion about memory reallocation for multiple GPUs can be found in §6.3.1.

6.2.2 Minimize rebuilding mappings. Our new scheme only rebuilds the mapping between particles and the background grid every 10–30 time steps (across all the test cases’ frames). When running with multiple GPUs, a standard rebuild-mapping step consists of more than ten CUDA kernels, CPU-GPU synchronizations, and inter-GPU synchronizations. In Fig. 6, we show that without our scheme, i.e., rebuilding the mapping every time step, the computational cost would increase by 42.5%–266.1% per frame.

6.2.3 Keep particles sorted with cheaper sorting. In our pipeline, a complete sort-particle step, i.e., sorting particles to cells, only occurs with the rebuild-mapping step. A warp-level radix sorting is used to help reduce the number of atomics in other time steps. Nevertheless, we adopt four warps per block since this choice performs better than the others in most cases.

We adopt Yue et al. [2018]’s neo-Hookean sand model for all the cases. In Fig. 20 we show that our implementation uses four warps per block; in other schemes that are commonly adopted. For example, suppose we always re-allocating regardless of sizes (always realloc). Right: The percentage of additional costs incurred by different schemes other than ours. The second
we can observe (through Nsight Compute) the amount of warp stall barriers doubles. Such barriers prevent the warps from switching to handle another block of particles. As a consequence, the cost dramatically increases by 48.0%–120.6% per frame (Fig. 10, vblock w. final sync).

Furthermore, there do not exist native GPU instructions that support atomic addition for floating-point numbers on shared memory in most recent NVIDIA graphics cards. The compiler would translate the shared atomic into loops and atomic compare-and-swap as shown in Fig. 2. Such a translation would increase the number of instructions by 38% and impact the computational performance. Fig. 10, vblock w. shared atoms, shows there is 131.1%–247.1% additional cost when using both virtual blocks and shared atoms.

Finally, as the size of the shared memory in each CUDA block is relatively large in MPM, the GPU occupancy becomes much lower than our implementation. Increasing the number of threads per block may help increase the occupancy but would not improve the performance. When the virtual block has a larger size, more threads stay idle for the particle blocks that do not have enough particles. Fig. 10, vblock w. sh. a. + occu., shows the situation deteriorates when increasing the number of threads per block from 128 to 256.

Fig. 21. Comparison between assigning a CUDA block to particles in mixed physical blocks (top) and assigning to a unique virtual block, each of which only holds particles from a single physical block (bottom). The latter scheme, proposed by Gao et al. [2018], may have more CUDA blocks being launched and less efficient utilization of threads when the size of physical blocks varies. Here we have three physical blocks holding 50, 150, and two particles, respectively. A solid box indicates a CUDA warp with 32 threads, and a dashed box indicates a CUDA block with four warps.

We adopt a complete sort-particle step every time step and introduces 11.3%–24.8% additional cost (P2G w. full sorting).

6.2.4 Avoid reduction on shared memory. Two kinds of methods have been designed to handle the write conflicts in the P2G steps. Gao et al. [2018] adopt three levels of reductions: first, a warp-level reduction reduces the number of atomics within each warp; second, each warp writes the sums into the shared memory via shared atomics; and a syncthreads function synchronizes the threads in the CUDA block before the final reduction is applied to write to the global memory. Wang et al. [2020] and Hu et al. [2019a] avoid the first reduction, and they shuffle particles such that there would be minimum conflicts within each warp. On the contrary, we eliminate the second reduction, which relies on the non-native shared atomics of floating-point numbers, to follow the proposed principle. In other words, after the warp-level reduction, we directly write to the global memory via global atomics without using the shared memory as the scratchpad. In Fig. 10, we conduct extensive comparisons between different schemes to show that our scheme manifests the best efficiency.

Compared with our scheme, partitioning particles into virtual blocks not only needs extra computations (6.4%–27.0% additional cost as in Fig. 10, vblock), but also introduces workload imbalance (Fig. 21) as virtual blocks would have many more idle threads. Notice that virtual blocks from the same particle block will write to the same global memory addresses, potentially increasing the number of conflicts.

Reducing to the shared memory also requires an additional in-block synchronization which turns out to be quite expensive. Putting an extra synchronization at the end of our implementation of P2G,
cacheline, two read operations are required instead of one, leading to less efficiency. AoSoA packs data into small 32× channel packets, and thus the memory access pattern of AoSoA is well aligned to the cacheline. In contrast, SoA has less aligned requests and needs 8%–18% more sectors (and thus more data) sent/received than AoSoA.

Furthermore, at the end of P2G, when threads in the same warp write to different grid nodes, SoA presents a less coalesced pattern, i.e., accessing addresses within the same warp can be wildly different from AoSoA, leading to 16% more accesses.

6.2.7 Merge small kernels. In Fig. 7, we show that merging small kernels into appropriate size boosts the performance as certain global memory operations, e.g., writing and then reading intermediate variables, can be removed. Compared with our final pipeline, computing stress with an individual kernel before P2G transfer (indiv. comp. stress) induces 4.7%–11.7% additional cost per frame; resolving boundary condition separately after updating nodal velocities (indiv. resolv. b. c) induces 0.2%–4.4% additional cost per frame; and clearing nodal buffers with an individual kernel before P2G transfer (indiv. buffer clearing) brings in as much as 4.3% additional cost per frame. While the small kernels cannot fully utilize the SM (also known as the tail effect [Mickeyevic et al. 2012]), the SM has to finish execution of these kernels before executing any other larger kernels afterward. By integrating these small kernels into the larger kernels following them, the limited computation or memory operations can be overlapped with other heavier computations or memory operations through interleaved warp scheduling, reducing the tail effect with small kernels.

In Fig. 23 we show that merging P2G and G2P transfer into a single G2P2G transfer, as suggested by Wang et al. [2020], is only beneficial when the number of particles is small as the instruction cache miss rate is still tolerable.

6.2.8 Tune the size of CUDA blocks. Our pipeline divide particles into warps, and each CUDA block handles four warps. In Fig. 18, we compare the performance with a different number of warps per CUDA block. The number of simultaneously active blocks on one SM is limited. Thus, when the number of particles is extensive, using 1 or 2 warps per CUDA block would lead to a large number of blocks, and some of them have to stay inactive. On the other hand, CUDA blocks with many warps would need too many registers, resulting in low occupancy.

6.3 Ablation study on multiple GPUs

6.3.1 Reduce memory reallocation. The principle for reducing memory reallocation proposed in §6.2.1 also applies to multi-GPU environment. However, in contrast to single-GPU scenarios, for multi-GPU, when one card reallocates the memory, it also needs to update information with other GPUs and thus inter-GPU synchronizations are enforced. As a result, we can observe much more overhead with frequent memory reallocation in a multi-GPU environment. As shown in Fig. 20, when simulating with four GPUs without pre-allocating more memory than requested, the overhead can be up to 396%. If we trivially reallocate every time step, the overhead is up to 533%.

One less obvious case is that libraries such as Thrust [Bell and Hoberock 2012] and CUB [Merrill 2015] that provide implementations of parallel algorithms need scratch memory to store the intermediate results. Implicitly re-allocating the scratch memory each time these algorithms execute impacts the performance and in Fig. 13 we show that it introduces 4.4%–9.2% additional cost when simulating with four GPUs.

6.3.2 Overlap computation and inter-GPU data transfer with interleaved warp scheduling. In our pipeline, the inter-GPU communications and the computations on the grid nodes are merged into one kernel, and thus in one stream. And we rely on the interleaved warp scheduler to automatically overlap the memory accesses and the computations. The alternative is to overlap the two of them with two different streams manually. In Fig. 14, we show that the two-stream implementation induces 3.8%–13.6% additional cost. As revealed in the analysis of Nsight System, the extra cost comes from the synchronization between the two different streams, while there is almost no difference in performance between the two schemes.

6.3.3 Lightweight block tagging. In Fig. 15 we show our tagging scheme is lightweight and occupies only up to 2.9% of the overall cost per frame even when the number of particles is small (55.3K). In contrast, the prior work [Wang et al. 2020] consumes much more time per step in tagging (Fig. 16). Furthermore, with our free zone
scheme, both the rebuild-mapping and the tagging only occur every 10–30 steps, leading to tremendous performance gain per frame (Fig. 17).

\[ \begin{align*}
\text{Left: } & \text{Timing (in milliseconds) comparison between our implementation and the one uses only a single buffer and writes nodal data directly through inter-GPU atomics. Right: The percentage of additional costs incurred with the latter scheme. Four GPUs are used in all scenarios.} \\
& \text{6.3.4 Isolate P2P reads and local reduce sum with double-buffering. After the P2G step, each card needs to read values on the shared grid blocks from other cards and then applies a local reduce operation to get the sums. We adopt a double-buffering scheme such that within one card, the P2P read requests from other cards and the local reduce sum are isolated. A simple alternative is to complete the reduction via P2P atomics directly. While it only requires one buffer and thus consumes less memory, this method turns out to be much less efficient than ours as P2P atomics are much more costly than P2P reads and writes, bringing 326.5%–2743.2% additional cost as shown in Fig. 25.} \\
& \text{6.3.5 Inter-GPU barriers. In Fig. 5 our spinlock scheme is compared with a more standard one that uses the CUDA API cudaStreamWaitEvent for an inter-GPU barrier. In cases with a small number of particles (e.g. 13.8K per card in our test), cudaStreamWaitEvent causes latency on the CPU that consumes \( \sim 1.38 \text{ms per frame, while the P2G transfer only takes 0.63ms.} \) We also observe cudaStreamWaitEvent costs in \( O(m^2) \) where \( m \) is the number of GPUs, which indicates the delay can be more severe for computation with eight cards.} \\
& \text{6.4 Fountain} \\
& \text{Our pipeline can also be applied to scenarios where new particles are generated every frame, which can be difficult for pipelines adopting G2P2G. We simulate a fountain (Fig. 26) similar to the one in Fei et al. [2021], and profile two different scales: one that can be simulated in real-time (55.9 frames per second on average with four GPUs) with maximal 143.5K particles (Fig. 27), and another one that is simulated offline with maximal 3.6M particles (Fig. 28). Each simulated frame is \( \frac{1}{60} \text{second.} \) In both two cases, we adopt the ASFLIP integrator [Fei et al. 2021] and a weakly-compressible material [Tampubolon et al. 2017] with bulk modulus \( 1.0 \times 10^5 \text{dyne/cm}^2 \). The ball-shaped water source is resampled at each frame with 27 particles per cell. We adopt a cell size 0.66cm for the interactive case and 0.25cm for the offline case. The time-step sizes are automatically deducted [Fang et al. 2018] \( (6.13 \times 10^{-4} \text{ on average for the interactive case; and } 1.78 \times 10^{-4} \text{ on average for the offline case).} \) In this scenario, particles spray and travel rapidly, and thus the rebuild-mappings are performed more frequently (11.77 steps on average between two rebuild-mappings). As a result, the number of particles used to keep the simulation running at an interactive rate is relatively low. Even in this case, the four-GPU efficiency of our pipeline is around 52%. And it can further boost to 89% when the number of particles increases to larger than one million.}

\[ \begin{align*}
& \text{6.5 Crawling in Snow} \\
& \text{We also profile our pipeline in a scenario with a more complicated animated boundary. We simulate a man crawling in the snow (Fig. 29). The animation of the man-shaped triangular mesh is converted to a sequence of levelsets during the precomputation. We model the snow as an NACC material [Wolper et al. 2019], with bulk modulus \( k = 5.00 \times 10^5 \), Poisson ratio \( \nu = 0.3 \), friction coefficient \( M = 0.8 \), cohesion coefficient \( \beta = 0.9 \), and hardening coefficient \( \xi = 5.0 \) (refer to Wolper et al. [2019] for the notations). We adopt a cell size 1.35cm. The time-step size is automatically deducted [Fang et al. 2018] \( (5.46 \times 10^{-4} \text{ on average).} \) The snow dynamics are relatively slow, which allows rebuild-mappings to be performed less frequently (84.36 steps on average between two rebuild-mappings). As a result, the performance is much better than the Fountain and it allows us to simulate 1.33M particles in real-time, i.e., \( \geq 60 \text{ frames per second with each simulated frame being } \frac{1}{60} \text{second (Fig. 30). And our pipeline achieves a significant four-GPU efficiency (on average 77%).} \)

\[ \begin{align*}
& \text{7 LIMITATION AND FUTURE WORK} \\
& \text{We introduce principles for optimizing MPM on both single-GPU and multi-GPUs and demonstrate that by following these principles our new pipeline achieves a dramatic performance boost compared to the state-of-the-art. However, we believe there is still room for improvement in many aspects and we list some of them as follows.} \\
& \text{Workload (re)-balancing. With multi-GPUs, we partition and distribute the particles evenly on each GPU during initialization. The partition pattern is pre-decided and its impact on the performance is not thoroughly studied. Neither do we consider dynamic workload re-balancing during simulation. When particles from different GPUs are randomly mixed, e.g., a paddle spinning in the sand may mix the sand from different GPUs, each physical block may be shared by all the GPUs and the inter-GPU communication would become the new bottleneck. Dynamic re-partition of the particles across multiple cards is still an open problem. Furthermore, transporting particles between GPUs during the simulation also brings additional costs.} \\
& \text{Adaptive, hierarchical data structure.} \text{ We only consider the simulation of MPM with a single level of the (sparse) background grid and all particles are of the same size. Gao et al. [2017] present an MPM simulation with a multi-level grid that supports adaptive refining and coarsening of different regions. It can be even more challenging to optimize on multiple GPUs for adaptive MPM.}
Validation on different devices. We only test our pipeline on Tesla V100 GPUs which is based on NVIDIA Volta architecture. There are many other GPU architectures (e.g., NVIDIA Turing, NVIDIA Ampere, and AMD and Intel GPUs) that have different on-chip memory designs (e.g., different sizes of register files and caches) and instruction sets [Jia et al. 2019]. Hence, our pipeline and principles may need to be tweaked and validated on GPUs with other architectures.

REFERENCES

2019. IEEE Standard for Floating-Point Arithmetic. IEEE std 754-2019 (Revision of IEEE 754-2008) (2019), 1–84. https://doi.org/10.1093/IEEEESTD.2019.8766229

Yuki Abe, Jason Aurimiller, Takuya Azumi, Masato Edahiro, Yusuke Fujii, Tsyoshi Hamada, Masaki Iwata, Shinpei Kato, Marcin Koscielniicki, Michael Methrow, Martin Peres, Hiroshi Sasaki, Yusuke Suzuki, Hisashi Usuda, Kaibo Wang, and Hiroshi Yamada. 2014. Gdev: Open-Source GPGPU Runtime and Driver Software. https://github.com/shinpei0208/gdev.

Takashi Amada, Masataka Imura, Yoshihiro Yasumuro, Yoshisugu Manabe, and Kuniharu Chihara. 2004. Particle-based fluid simulation on GPU. In ACM workshop on general-purpose computing on graphics processors, Vol. 41. Citeseer, 42.

Nathan Bell and Jared Hoberock. 2012. Thrust: A productivity-oriented library for CUDA. In GPU computing gems Jade edition. Elsevier, 359–371.

Gilbert Louis Bernstein, Chunmayee Shah, Cristian Lemure, Zachary Devito, Matthew Furse, Philip Levis, and Pat Hanrahan. 2016. Ebb: A DSL for Physical Simulation on CPUs and GPUs. ACM Trans. Graph. 35, 2, Article 21 (May 2016). 12 pages. https://doi.org/10.1145/2892632

Robert Bridson. 2015. Fluid simulation for computer graphics. CRC press.

Zhi Liu, Byungmoon Kim, Daichi Ito, and Huamin Wang. 2015. Waterbrush: GPU-based 3D painting simulation at the bristle level. ACM Transactions on Graphics (TOG) 34, 6 (2015), 1–11.

Nuttapong Chentanez, Matthias Müller, and Tae-Yong Kim. 2015. Coupling 3D Eulerian, Heightfield and Particle Methods for Interactive Simulation of Large Scale Liquid Phenomena. IEEE Transactions on Visualization and Computer Graphics 21, 10 (2015), 1116–1128. https://doi.org/10.1109/TVCG.2015.2449303

Nuttapong Chentanez and Matthias Müller. 2011. Real-time Eulerian water simulation using a restricted tall cell grid. In ACM Siggraph 2011 Papers. 1–10.

Jonathan M Cohen, Sarah Tariq, and Simon Green. 2010. Interactive fluid-particle simulation using translating Eulerian grids. In Proceedings of the 2010 ACM SIGGRAPH symposium on Interactive 3D Graphics and Games. 15–22.

Jose Ricardo Da Silva Junior, Mark Joselli, Marcelo Zamith, Marcos Lage, Esteban Chua, Eduardo Soluri, and Nullpointer Tecnologia. 2012. An architecture for real time fluid simulation using multiple GPUs.

José M Dominguez, Alejandro JC Crespo, Daniel Valdez-Balderas, Benedict D Rogers, and Moncho Gómez-Gesteira. 2013. New multi-GPU implementation for smoothed particle hydrodynamics on heterogeneous clusters. Computer Physics Communications 184, 8 (2013), 1848–1860.

Yu Fang, Yuanming Hu, Shi-Min Hu, and Chenzhuang Jiang. 2018. A temporally adaptive material point method with regional time stepping. In Computer graphics forum, Vol. 37. Wiley Online Library, 195–204.
Crawling in Snow. A man crawls forward in the snow. This simulation has 1.33M particles and can be simulated in real-time (≥ 60 frames per second) with four Tesla V100 GPUs. At the bottom, particles simulated with different GPUs are colored differently.

Fig. 30. Left: Timing (in milliseconds) per frame of Crawling in Snow with 1.33M particles over different frames; Right: four-GPU Efficiency over different frames.

Yuanming Hu, Tzu-Mao Li, Luke Anderson, Jonathan Ragan-Kelley, and Frédéric Durand. 2019a. Taichi: a language for high-performance computation on spatially sparse data structures. *ACM Transactions on Graphics (TOG)* 38, 6 (2019), 1–16.

Yuanming Hu, Xinxin Zhang, Ming Gao, and Chenfanfu Jiang. 2019b. On hybrid lagrangian–eulerian simulation methods: practical notes and high-performance aspects. In *ACM SIGGRAPH 2019 Courses*. 1–246.

Libo Huang, Ziyin Qu, Xin Tan, Xinxin Zhang, Dominik L. Michels, and Chenfanfu Jiang. 2021. Ships, Splashes, and Waves on a Vast Ocean. *ACM Trans. on Graph. (TOG)* 40, 6 (2021), 1–15.

Sylvain Jeaugey. 2017. NCCL 2.0. In *GPU Technology Conference (GTC)*.

Zhe Jia, Marco Maggioni, Jeffrey Smith, and Daniele Paolo Scarpazza. 2019. Dissecting the NVidia Turing T4 GPU via microbenchmarking. arXiv preprint arXiv:1903.07486 (2019).

Chenfanfu Jiang, Theodore Gast, and Joseph Teran. 2017. Anisotropic elastoplasticity for cloth, knit and hair frictional contact. *ACM Trans. on Graph. (TOG)* (2017).

Chenfanfu Jiang, Craig Schroeder, Joseph Teran, Alexey Stomakhin, and Andrew Selle. 2016. The material point method for simulating continuum materials. In *ACM SIGGRAPH 2016 Courses*. 1–52.

Gergely Klár, Theodore Gast, Andre Pradhana, Chuyuan Fu, Craig Schroeder, Chenfanfu Jiang, and Joseph Teran. 2016. Drucker-prager elastoplasticity for sand animation. *ACM Trans. on Graph. (TOG)* 33, 4 (2016), 1–12.

Jiri Kraus. 2019. Multi GPU Programming Models. In *GPU Technology Conference (GTC)*.

Miles Macklin, Matthias Müller, Nuttapong Chentanez, and Tae-Yong Kim. 2014. Unified Particle Physics for Real-Time Applications. *ACM Trans. on Graph. (TOG)* 33, 4, Article 153 (July 2014), 12 pages. https://doi.org/10.1145/2601097.2601152

Duane Merrill. 2015. Cub. NVIDIA Research (2015).

Paulius Maciukievicius. 2012. GPU performance analysis and optimization. In *GPU Technology conference*, Vol. 3. NVIDIA. 2021a. CUDA Binary Utilities: Instruction Set Reference. https://docs.nvidia.com/cuda/cuda-binary-utilities/index.html.

NVIDIA. 2021b. Kernel Profiling Guide. https://docs.nvidia.com/cuda/kernel-profiling-Guide.pdf.

Rajakhar Setaluri, Mridul Aanjaneya, Sean Bauer, and Efthychios Sifakis. 2014. SPGrid: A sparse paged grid structure applied to adaptive smoke simulation. *ACM Transactions on Graphics (TOG)* 33, 6 (2014), 1–12.

Alexey Stomakhin, Craig Schroeder, Chenfanfu Jiang, Lawrence Chai, Joseph Teran, and Andrew Selle. 2014. Augmented MPM for phase-change and varied materials. *ACM Trans. on Graph. (TOG)* 33, 4 (2014), 1–11.

Alexey Stomakhin and Andrew Selle. 2017. Fluxed animated boundary method. *ACM Trans. on Graph. (TOG)* 36, 4 (2017), 1–8.

Bjarne Stroustrup. 2015. The C++ Programming Language. Pearson Education.

Deborah Sulsaky, Zhen Chen, and Howard L Schreyer. 1994. A particle method for history-dependent materials. *Computer methods in applied mechanics and engineering* 118, 1-2 (1994), 179–196.

Andre Pradhana Tampubolon, Theodore Gast, Gergely Klár, Chuyuan Fu, Joseph Teran, Chenfanfu Jiang, and Ken Museth. 2017. Multi-species simulation of porous sand and water mixtures. *ACM Trans. on Graph. (TOG)* 36, 4 (2017), 1–11.

Min Tang, Haomin Wang, Le Tang, Ruofeng Tong, and Dinesh Manocha. 2016. CAMA: Contact-aware matrix assembly with unified collision handling for GPU-based cloth simulation. In *Computer Graphics Forum*, Vol. 35. Wiley Online Library, 511–521.

ACM Trans. Graph., Vol. 1, No. 1, Article . Publication date: November 2021.
Min Tang, Tongtong Wang, Zhongyuan Liu, Ruofeng Tong, and Dinesh Manocha. 2018. I-Cloth: Incremental collision handling for GPU-based interactive cloth simulation. ACM Transactions on Graphics (TOG) 37, 6 (2018), 1–10.

David Tarjan, Kevin Skadron, and Paulius Micikevicius. 2009. The art of performance tuning for cuda and manycore architectures. Birds-of-a-feather session at SC 9 (2009).

Orestis Vantzos, Saar Raz, and Mirela Ben-Chen. 2018. Real-Time Viscous Thin Films. ACM Trans. Graph. 37, 6, Article 281 (Dec. 2018), 10 pages. https://doi.org/10.1145/3272127.3275086

Huamin Wang. 2021. GPU-based simulation of cloth wrinkles at submillimeter levels. ACM Transactions on Graphics (TOG) 40, 4 (2021), 1–14.

Huamin Wang and Yin Yang. 2016. Descent methods for elastic body simulation on the GPU. ACM Transactions on Graphics (TOG) 35, 6 (2016), 1–10.

Xinlei Wang, Yuxing Qiu, Stuart R Slattery, Ya Fang, Minchen Li, Song-Chun Zhu, Yuxin Zhu, Min Tang, Dinesh Manocha, and Chenfanfu Jiang. 2020. A massively parallel and scalable multi-GPU material point method. ACM Transactions on Graphics (TOG) 39, 4 (2020), 30–1.

Rene Wincherbach, Hendrik Hochstetter, and Andreas Kolb. 2016. Constrained neighbor lists for SPH-based fluid simulations. In Proceedings of the ACM SIGGRAPH/Eurographics Symposium on Computer Animation. 49–56.

Joshua Wolper, Yu Fang, Minchen Li, Jiecong Lu, Ming Gao, and Chenfanfu Jiang. 2019. CD-PM. Continuum damage material point methods for dynamic fracture animation. ACM Trans. on Graph. (TOG) 38, 4 (2019), 1–15.

Kui Wu, Nghia Truong, Cem Yüksel, and Rama Hoetzlein. 2018. Fast Fluid Simulations with Sparse Volumes on the GPU. Computer Graphics Forum 37, 2 (2018), 157–167. https://doi.org/10.1111/cgf.13350 arXiv:https://onlinelibrary.wiley.com/doi/pdf/10.1111/cgf.13350

Longhua Wu, Botao Wu, Yin Yang, and Huamin Wang. 2020. A Safe and Fast Repulsion Method for GPU-based Cloth Self Collisions. ACM Transactions on Graphics (TOG) 40, 1 (2020), 1–18.

Yonghao Yue, Breannan Smith, Peter Yichen Chen, Maytee Chantharayukhontorn, Ken Kamrin, and Eitan Grinspun. 2018. Hybrid grains: adaptive coupling of discrete and continuum simulations of granular media. ACM Trans. on Graph. (TOG) (2018).

Fan Zhang, Xiong Zhang, Kam Yim See, Yanping Lian, and Yan Liu. 2017. Incompressible material point method for free surface flow. J. Comput. Phys. 330 (2017), 92–110. https://doi.org/10.1016/j.jcp.2016.10.064