Graphical modelling of carbon nanotube field effect transistor

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Abstract. Carbon nanotube Field Effect Transistors (CNTFET) are found to be one of the most promising successors to conventional Si-MOSFET. This paper presents a novel modelling for planar CNTFET based on curve fitting method. The results obtained from the model are compared with the simulated results obtained by using the nanohub simulator. Finally the accuracy of the model is discussed by calculating the normalized root mean square difference between the nanohub simulation results and those obtained from the proposed model.

1. Introduction
Among many different potential applications of carbon nanotubes (CNT), we have focused on its use in CNTFET, which is found to be one of the most promising alternatives for current field effect transistors. The first CNTFET was reported in 1998 [1] and after that different types of structures are proposed for CNTFET [2-9], out of which we have chosen the planar CNTFET. Further different models are also developed to study the characteristics of different CNTFETs [10-12]. In this paper we have presented a model for planar CNTFET which reproduces almost same results as obtained from the simulation which is done by using the nanohub simulator [13-15]. The main aim is to report a simple model which produces the results very similar to that obtained through very rigorous methods.

The paper is organized as follows. Characterization of planar CNTFET is done based on the simulation results which are discussed in section 2. After that the developed model is presented in section 3. Section 4 is devoted for results and discussions and finally a conclusion is given in section 5.

2. Characterization of CNTFET
The planar CNTFET structure is almost the same as the conventional Si-MOSFET, the only difference being the use of a CNT in the channel region, inside which the carriers move from source to drain. Different CNTFETs having planar structure were simulated to understand how the characteristic curves depend on different tube parameters, like the length of the tube and its chirality. This simulation was done by using the nanohub simulators [13-15]. First of all a CNTFET was simulated in which a (10,0) CNT is used as the channel. For this simulation we have kept all other parameters fixed and changed the channel length as well as the top gate length proportionally. For the second phase of simulation, the diameter of the CNT was changed by changing the chirality, and the channel length was kept constant. The basic characteristic curves for a planar CNTFET based on the above simulation results are shown in figure 1 (a) and 1 (b). Further a (10,0) CNT is considered as the channel and the channel length is taken to be 10 nm. A (10,0) CNT was chosen because the band gap for this is comparable with that of silicon. The range of drain voltage for the output characteristic curves, as shown in figure 1 (a), is 0V - 0.4V and the different curves in the plot are for gate voltages from
0.225V to 0.4V in steps of 0.025V. The drain current is very small for the first plot which is for a gate voltage 0.225V, as this gate voltage is just above the threshold voltage. Moreover, the current increases with applied gate voltage. Figure 1 (b) shows the transfer characteristic curves for drain voltages 0.2V, 0.3V and 0.4V respectively. As the saturation is achieved well before these drain voltages, we have same drain current for all the three drain voltages for any applied gate voltage and hence all the three curves coincide.

![Figure 1: (a) Vd~Id plot and (b) Vg~Id plot for planar CNTFET.](image)

3. Modeling of CNTFET

For the modeling we have first obtained the simulation results from the nanohub simulator as discussed in the previous section. The simulation was repeated for different planar CNTFETs with different physical dimensions (length and diameter) to study the dependence of drain current on those parameters. In the next step we have developed certain empirical relations between the drain current \(I_d\), drain voltage \(V_d\) and the applied gate voltage \(V_g\), that we have obtained, based on the previous simulation results, using the best-fit method. In this we have used a best-fit schemes based on exponential fit, where the functional relation is chosen to be an exponential function. The best fit is in the sense of minimal root-mean-squared (RMS) difference between the function chosen and the simulation data. This has been done for planar CNTFETs, over the entire range of \(V_d\) & \(V_g\) values chosen. In order to check the closeness of the fits, we have calculated the root-mean-squared difference (RMSD) and normalized-root-mean- squared differences (NRMSD).This fit also includes the length modulation of the CNT forming the channel and the chirality of the CNT is chosen as \((10,0)\). The choice of a particular chirality fixes the diameter of the CNT used in the channel. The exponential function chosen is:

\[
I_d = f(V_g, L) \times \left(1 - e^{d(V_g)V_g}\right)
\]

(1)

Here \(d\) is a function of gate voltage only but \(f\) is a function of both gate voltage \(V_g\) and the length of CNT \(L\) which are given as:

\[
f(V_g, L) = a_1V_g^a
\]

(2)

\[
d = d_1V_g^2 - d_2V_g - d_3
\]

(3)

Further the coefficients \(a_1\) and \(a\) in \(f\) are considered as functions of length and modeled as:

\[
a = c_1 \exp(c_2L) + c_3 \exp(c_4L)
\]

(4)
where $c_1$, $c_2$, ..........., $c_8$ are different fitting parameters, which, in the present calculation, have been taken to be constants. However, these coefficients can be modeled further to include dependency on other parameters like diameter, doping, dielectric constants etc.

4. Results and Discussions

The output characteristic curves, obtained with the above fit, for different planar CNTFETs with different lengths of CNT are shown in figure 2 and the results are compared with the simulation results obtained from the nanohub simulator. Figure 2(a)-(d) are for different lengths of the CNT used as the channel. Further for each length of the CNT we have plotted the characteristic curves for different applied gate biases. In the figures the dotted lines are for the results obtained from the nanohub simulator and the solid lines represent the result obtained from our model equations. As can be seen from the graphs, we are getting very similar result as the previous simulation results. We have also calculated the NRMSE for each curve to have a quantitative measure of the error, which are listed in table 1.

Figure 2: Comparison between the results obtained from the nanohub simulator and our model: (a) $L = 5$nm, (b) $L = 10$nm, (c) $L = 15$nm and (d) $L = 20$nm.
Table 1. Calculated NRMSE for different applied gate voltage and different length of the CNT used in the channel of the device.

| L_{CNT} in nm | Vg in volt(V) | NRMSE | L_{CNT} in nm | Vg in volt(V) | NRMSE |
|---------------|---------------|-------|---------------|---------------|-------|
| 5nm           | 0.275         | 0.1444| 15nm          | 0.275         | 0.0603 |
|               | 0.3           | 0.0600|               | 0.3           | 0.0284 |
|               | 0.325         | 0.0167|               | 0.325         | 0.0342 |
|               | 0.35          | 0.0384|               | 0.35          | 0.0479 |
|               | 0.375         | 0.0806|               | 0.375         | 0.0398 |
|               | 0.4           | 0.0399|               | 0.4           | 0.0233 |
| 10nm          | 0.275         | 0.2157| 20nm          | 0.275         | 0.2793 |
|               | 0.3           | 0.1219|               | 0.3           | 0.1276 |
|               | 0.325         | 0.0433|               | 0.325         | 0.0108 |
|               | 0.35          | 0.0133|               | 0.35          | 0.0292 |
|               | 0.375         | 0.0533|               | 0.4           | 0.1594 |

Using our model equations as given in equation (1), the transfer characteristic curves are also plotted for two different lengths of the CNT used in the channel region. The plots are shown in figure 3, in which the dotted lines are for the results obtained using our model and the solid lines show the results obtained from the nanohub simulator. The drain voltage considered for both the cases is equals to 0.3V. From the figures it is clearly seen that the fits are quite good.

Figure 3: Transfer characteristic curves for planar CNTFETs with CNTs of length (a) 10 nm and (b) 15 nm.

5. Conclusion
This paper presents some model equations which reproduces output as well as transfer characteristics, for planar CNTFET, very close to some earlier results. Both qualitative as well as quantitative comparisons are done which show the accuracy of the results obtained from the proposed model equations.

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