Process for integration of energetic porous silicon devices

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Abstract. We have developed new procedures for etching porous silicon (PSi) which allow PSi devices to be more easily integrated with other devices used for controlling or utilizing the output of the PSi devices. The output from energetic PSi devices may be used for MEMS actuation or energy harvesting applications. Initial proof-of-concept energy harvesting with a macro-scale, piezo cantilever has been demonstrated. Of the 2 etch processes developed, the sacrificial electrode process is the simplest, but it produces an inhomogeneous PSi thickness across the wafer and introduces surface topography due to electropolishing. By using the anchored electrode method, which incorporates a dielectric layer, more controllable etch depths and patterned devices are obtained. However, a proximity effect is observed where features closer to the electrode etch more rapidly. A simple voltage divider model can be used to predict these relative etch depths, but more work is required to develop a quantitative model.

1. Introduction

Porous silicon (PSi) devices have been investigated for a number of applications including chem/biosensors, optoelectronics, and solar cells [1] as well as for energetic devices such as micro-thrusters [2]. Here, we describe a metal-assisted etch process [1, 3] that will facilitate integration of PSi with other devices. The difficulty in such integration stems from the aggressive etch solution (3:1 HF:ethanol with 2.4% H$_2$O$_2$). The new process, where the metal electrode and the Si to be etched are on the same side of the wafer, permits etchant sensitive devices on the other side of the wafer to be protected during the etch. This is important as it provides significantly more flexibility for integrating PSi with other devices on the same wafer or chip.

PSi is most commonly formed by anodic etching of a silicon (Si) wafer in an etch solution containing a high concentration of HF [1]. We have focused on using a metal-assisted etch, also referred to as a galvanic etch, which is a simplified etch procedure that does not require a potentiostat or external wires to the wafer. In this approach, a metal, typically platinum (Pt) is deposited on 1 side of a Si wafer, and this metallized wafer is immersed in a HF, hydrogen peroxide (H$_2$O$_2$), and ethanol etch solution. The H$_2$O$_2$ reacts with hydrogen ions from the HF at the catalytic metal surface to become water molecules while liberating electron-hole (h+) charge carriers into the metal/wafer. These h+ charge carriers traverse the wafer to the other side where they induce the exposed Si to react with the HF to produce a soluble dihydrogen silicon hexafluoride product [3]. In this arrangement, the HF and H$_2$O$_2$ concentrations control the electrochemical current, and therefore reaction rate, without any external instrumentation. In addition, the Pt to Si surface area ratio also affects the etch rate, as the etch current is proportional to the area of exposed Pt, and the area of exposed Si determines the resultant etch current density. If the current density at the Si surface becomes too large, the etch transitions from producing PSi to an electropolishing regime where the Si is completely etched away [1]. Two approaches were taken for using same-side Pt electrodes. In the first approach, Pt electrodes
were deposited directly on the Si wafer to be etched. This approach is termed the sacrificial Pt electrode approach since the PSi etch etches the Si underneath the Pt, eventually releasing the Pt from the wafer. In the second approach, termed the anchored Pt electrode approach, the Pt electrodes are deposited onto a Si wafer that is covered with a silicon nitride (Si$_3$N$_4$) layer which is patterned to expose the Si to the etchant, and to allow electrical contact between the Pt electrodes on top of the Si$_3$N$_4$ and the Si.

2. Experimental

In this study, 1–10 Ω p+ Si wafers were used as they produce nanoporous Si, which is desired for our energetic PSi applications. These wafers have 500 nm of Si$_3$N$_4$ on both sides as received from Rogue Valley Microdevices. In the case of the sacrificial Pt electrodes, the Si$_3$N$_4$ is removed from 1 side of the wafer while, in the case of anchored Pt electrodes, photolithographically defined windows are etched in the Si$_3$N$_4$ to expose Si areas for etching and for electrical contact to the Pt. These Si$_3$N$_4$ etches are carried out using a Unaxis VLR 700 reactive ion etch system.

After the Si$_3$N$_4$ has been removed as desired, the wafer is etched for 2 min in 6:1 H$_2$O:HF to remove any native oxide prior to being sputter cleaned for 30 s in a Unaxis Clusterline 200 sputter deposition system. Without breaking vacuum, the samples are then transferred to the Pt sputter chamber where 170 nm of Pt is sputter deposited at a sample temperature of 250 °C. This Pt layer is then patterned using photolithography and a 4Wave Inc. 4W-PSIBE ion mill etch system. The resulting wafers, which have patterned Pt electrodes and exposed Si, are then etched with a HF, ethanol, and peroxide mixture. The ethanol reduces the viscosity/surface tension of the etch solution so that it can penetrate into the small pores being formed. A typical etch composition is 3:1 HF:ethanol with 2.4% peroxide.

The etch results were characterized using scanning electron microscope (SEM) cross-section micrographs obtained with a Hitachi S4500 SEM. Etch depth measurements were also made, after removing the PSi with a 1 molar potassium hydroxide (KOH) etch, using a Wyko NT1100 optical profilometer. In order to measure the combustion rates of the PSi, bridge wires were photolithographically deposited onto the wafers, prior to the PSi etching, using a lift-off approach with metal deposited using a CHA Industries e-beam evaporator [2]. In order to burn the PSi an oxidizer is applied to the PSi in the form of a 3 M sodium perchlorate in methanol solution. After drying for 30 min, the PSi is ignited by passing 20 V/1 A of current across the bridge wire. This is done while synchronously triggering a Photon Devices Inc, high-speed camera used to measure the PSi burn rate.

An energy harvesting experiments was performed by mounting PSi device, made using backside electrodes [2], onto a macro-scale piezoelectric cantilever model V22B obtained from Mide. Upon ignition of the PSi, the output of the piezo was put into a Mide model EH20W rectifier circuit with the output stored on a capacitor. The piezo signal and the charging of the capacitor were monitored with an oscilloscope.

3. Results

3.1. Sacrificial Pt Electrodes

The sacrificial Pt approach was investigated because it is the simplest approach to same-side Pt electrodes as it requires only a Pt deposition and patterning process before the PSi etch. Figure 1 is a drawing showing the sample structure and associated etch process. The sacrificial Pt electrodes were designed to be at least as wide as the desired etch depth so that the Pt would not be completely undercut until the desired etch depth had been achieved. In practice, the PSi etching under the Pt edges enables the Pt to detach from the Si surface. As a result, the Pt peels back from the etch-front producing greater lateral than vertical etching as shown in figure 2. This delamination results from current crowding [4] at the edge of the Pt/Si interface which increases the local etch current density into the electropolishing regime [1] which removes all of the Si. This Pt delamination and electropolishing limits the PSi thickness, results in PSi thickness inhomogeneity, and produces surface
topography. It may be possible to reduce the deleterious electropolishing by reducing the etch solution concentrations and the Pt:Si ratios. However, this is likely to adversely affect the quality of the PSi for many applications, and the PSi thickness will still be non-uniform across the sample surface.

**Figure 1.** Cross-sectional diagram of the sacrificial electrode PSi etch showing that the etch undercuts the Pt electrode.

**Figure 2.** SEM cross-sectional image showing a Pt electrode peeling back from the PSi etch-front resulting in greater lateral etching under the Pt than the vertical etching into the Si surface.

### 3.2 Anchored Pt Electrodes

In order to achieve thicker PSi films along with better control over the PSi pattern on the wafer, the anchored Pt approach was developed. In this approach, the Pt is deposited onto Si$_3$N$_4$ which is patterned to expose the Si to be etched, and to allow electrical contact between the Pt and Si, as shown in figure 3. The Si$_3$N$_4$ performs 2 important functions for this etch approach. As before, its resistance to the PSi etchant allows it to be used to define where the PSi will be etched. In addition, its dielectric nature prevents electropolishing induced delamination at the edge of the Pt electrodes.

**Figure 3.** Cross-sectional drawing of the anchored electrode structure and etch process showing the PSi etch undercutting the Si$_3$N$_4$, and that the Pt is isolated from the PSi etch front.

**Figure 4.** SEM cross-sectional image showing signs of electropolishing early in the etch, with better PSi formed as the etch-front area grows, thus lowering the etch current density.

Even away from the Pt contact, electropolishing of the exposed Si can still occur if the H$_2$O$_2$ concentration is too high or if the Pt:Si ratio is too large. Figure 4 shows an example of a line of etched
PSi where the initial etching was near the electropolishing regime leading to broken and isolated pieces of PSi. As the etch progressed, the area of Si at the etch-front increased so that the etch current density decreased to below the electropolishing regime so that better quality PSi was formed.

There can also be variations in etch rates as a function of distance from the Pt electrode. This proximity effect results in features closer to the Pt having different PSi etch depths and properties from features further from the Pt. A quantitative measure of the proximity effect was made by etching a number of lines at various distances from a Pt electrode. Figure 5a-b shows plots of etch depths for 5 lines at different distances from Pt electrodes. These depths were measured using optical profilometry after removing the PSi. It can be seen that there is a greater proximity effect when the PSi lines are close to the Pt electrode (figure 5a). In this case, the etch depths range from 22.4 to 11.8 microns when the lines were from 2.1 to 3.9 mm from the Pt contact point, respectively. In the second sample (figure 5b), the etch depths vary from 7.3 to 6.5 microns for lines 20.1 to 21.9 mm from the Pt contact point, respectively. The additional resistance between the Pt electrode and the etched lines in this sample results in more uniform etching as well as reduced etch rates.

A simple voltage divider model serves as a first-order approximation for this effect, and it could be used to design electrodes for minimizing or utilizing differences in etch depth across the wafer. Normalizing the voltage divider model output to match the etch depth of the line closest to the Pt electrode produces the results shown in figure 6 for the sample showing more variation in etch depth. Figure 6 shows a less than perfect fit between the model and experimental results. More experimental measurements need to be made before a more accurate model can be developed.

Figure 5. Optical profilometry of PSi line depths at various distances from a Pt electrode (which are to the right of the plots). (A) lines etched at 2.1, 2.55, 3.0, 3.45, and 3.9 mm from their electrode. (B) lines etched at 20.1, 20.55, 21.0, 21.45, and 21.9 mm from their electrode.

Figure 6. Plot of etch depth versus distance from the electrode data from figure 5a compared to predictions using a simple voltage divider model scaled to the deepest etch depth.

Long straight line devices were made in order to characterize the burn properties of PSi produced with anchored Pt same-side electrodes. By filming the burning of a 0.5-mm-wide, 23-mm-long, and approximately 18-micron-thick PSi device, a flame speed of 3.6 m/s was measured when using sodium perchlorate as the oxidizer. This is comparable to similar PSi etched using the standard backside electrode process, which produces m/s to km/s burn rates [5].
Since the energy density of PSi is very high, it would be useful if it could be converted to electrical energy. A proof of concept energy harvesting demonstration was performed by mounting a 2 mm diameter PSi device [2] onto a macro-scale piezo cantilever. Upon ignition, the force deflected the cantilever which oscillated producing an AC signal which was rectified and used to charge a capacitor (see figure 7). By using force measurements and equations for strain energy in a cantilevered beam, we can estimate that amount of harvestable mechanical energy for these devices is on the order of 1 µJ, much lower than the expected 250 µJ of mechanical energy from the PSi [2]. While initial system efficiencies are low, there is significant opportunity to improve them. For example, the need to excite the proper oscillation modes in the cantilever was observed. This may be done through tuning the burn rate of the PSi to match the harmonics of the cantilever, and by placing the sample at the harmonic nodes of the cantilever.

![Image](image_url)

Figure 7. (A) Photograph of a PSi device being ignited while attached to a piezoelectric cantilever. (B) Output of cantilever during oscillation.

4. Conclusions

We have developed new procedures for etching PSi while potentially only exposing 1 side of the sample to the etch solution. This allows PSi devices to be more easily integrated with existing devices on a wafer or chip. These other devices may be used for initiating or utilizing the mechanical force, gases, light, or thermal energy from energetic PSi devices for MEMS actuation or energy harvesting applications. Of the 2 processes developed, the sacrificial electrode process is the simplest, but it produces an inhomogeneous PSi thickness across the wafer and introduces surface topography due to electropolishing. The anchored electrode approach, which includes an etch-resistant dielectric layer, produces more controllable etch depths and makes patterned devices possible. One complication is a proximity effect is where features closer to the electrode etch more rapidly. However, a simple voltage divider model can be used to predict the relative etch rates, and therefore, develop electrode patterns that will produce the desired results. Proof-of-concept energy harvesting with a macro-scale, piezo cantilever has been demonstrated.

5. References

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