Abstract—With the rise in Internet of Things (IoT) devices, home network management and security are becoming complex. There is an urgent requirement to make smart home network management efficient. This work proposes an SDN-based architecture to secure smart home networks through K-Nearest Neighbor (KNN) based device classifications and malicious traffic detection. The efficiency is further enhanced by offloading the computation-intensive KNN model to Field Programmable Gate Arrays (FPGA), which offers parallel processing power of GPU platforms at lower costs and higher efficiencies, and can be used to accelerate time-sensitive tasks. The proposed parallelization and implementation of KNN on FPGA are achieved by using the Vivado Design Suite from Xilinx and High-Level Synthesis (HLS). When optimized with 10-fold cross-validation, the proposed solution for KNN consistently exhibits the best performances on FPGA when compared with four alternative KNN instances (i.e., 78% faster than the parallel Bubble Sort-based implementation and 99% faster than the other three sorting algorithms). Moreover, with 36,225 training samples, the proposed KNN solution classifies a test query with 95% accuracy in approximately 4 milliseconds on FPGA compared to 57 seconds on a CPU platform.

Index Terms—FPGA, smart home, IoT, security, HLS, KNN

I. INTRODUCTION

The Internet of Things (IoT) marketplace has experienced an exponential increase over the past few years. The current estimate projects that 43 billion IoT devices will be in circulation by 2025, a threefold increase from 2018 [1]. Further, the investment in IoT technology is projected to grow at 13.6% per year through 2022 [1]. One important IoT application is a smart home, whose market is expected to reach $121 billion by 2022 [2].

Existing security solutions are becoming inadequate to manage smart home IoT devices due to the following reasons. Firstly, IoT devices’ explosive growth has led to pervasive device heterogeneity and various communication protocols, which require comprehensive network management. Secondly, IoT devices generate massive amounts of data, resulting in heavy computational complexity for data-driven security analysis. However, the access points (APs) in most smart homes are far from adequate to handle such complex network management and analysis. Thus, an efficient and scalable security solution is required.

To combat growing difficulties in smart home security, Software Defined Networking (SDN) technology is leveraged in this paper as an effective centralized solution. With the decoupling of the control plane and data plane, resource-limited home APs can focus mainly on simple switch functionalities on the data plane while offloading the complex control tasks. This enables SDN to provide an effective and efficient networking management system. Given the resource-constrained nature of home gateways and routers, the proposed solution uses flow statistics as features because they are less computationally expensive than packet-by-packet statistics. Furthermore, Machine Learning (ML) models can be utilized to identify devices and malicious behaviors in a network. In particular, the K-Nearest Neighbors (KNN) algorithm is chosen in this work due to its effectiveness and simplicity.

Despite the benefits of using ML and SDN, the capacity of SDN controllers is still limited. With rapid increases in the number of IoT devices in a smart home and their significant amount of traffic data, the computational overhead of running ML models is also dramatically increasing, causing challenges in real-time secure home network management. Field Programmable Gate Arrays (FPGAs) is proposed in this paper to enhance system efficiency. They are highly flexible and can perform ML workloads with significantly reduced latency due to a fundamentally different execution paradigm than traditional CPU-based systems. Although they can be challenging to program and utilize, FPGAs promise to enhance SDN scalability by performing auxiliary SDN tasks faster, especially those required by ML. The proposed solution is implemented using high-level synthesis (HLS) and optimized for an FPGA workflow while comparing it to existing FPGA and parallel KNN implementations. It is further compared to CPU-based solutions executed on a single controller to show the advantages of leveraging the network programmability of FPGA architecture to reduce the latency of ML applications on SDN.

Our contributions are listed as follows. First, we propose a SDN-based architecture to secure a smart home network using device classification and Distributed Denial of Service (DDoS) detection and accelerate this decision-making process for real-time security via FPGA. Second, we propose a novel KNN parallelization and implementation on FPGA using HLS. Third, comprehensive experimental results on both FPGA and CPU platforms validate that the proposed KNN instance outperforms other existing KNN instances in achieving the minimum latency.

The rest of this paper is organized as follows. We present the proposed SDN-based architecture for smart home security and data collection setup in Section [1]. The overview of the KNN's implementation using HLS for device classification and DDoS
detection is presented in Section III. Next, the in-depth results are discussed in Section IV. Finally, the related works are discussed in Section V, followed by a conclusion in Section VI.

II. AN ARCHITECTURE FOR SMART HOME SECURITY

A. Proposed Architecture

We propose a SDN-based, FPGA-accelerated smart home architecture in Figure 1. The data plane comprises Open vSwitch (OVS). The OVS is responsible for forwarding packets as flow data to the controller received from connected devices, including IoT devices and attack devices. Further, the controller extracts features for offloading and sends them to the FPGA, where the specialized KNN implementation executes. The controller is a Raspberry Pi (RPI) running RYU controller software. The FPGA then forwards the device classification and DDoS detection class to the RPI controller to update OVS rules. Currently, the FPGA is an Artix-7 and is separated from the controller. However, this can also be realized in a single heterogeneous system that provides programmable FPGA logic and a CPU (as in the Xilinx 7000 series chips), reducing the communication lag between the FPGA and CPU and providing a complete System on Chip (SoC) that is fully integrated.

B. Smart Home Testing Environment

We establish a smart home testbed to collect benign and DDoS attack data by adopting various hardware and software tools. Four popular IoT devices, including Google Home, Amazon Echo, Nest Camera, Ring Camera, and one Android phone, are adopted. Three Linux machines are configured to act as WiFi AP, sniffer, and attacker, respectively. The hostapd is configured on the AP. hostapd is a user-space daemon that helps to create an isolated environment for data collection. We configure tshark on the sniffer to collect benign and attack traffic. tshark is a command-line tool that reduces the graphical user interface (GUI) overhead on Linux machines. Further, hping3 is installed on the attacker, which helps to change the IP source addresses, IP destination addresses, attack types, and attack duration dynamically.

The IoT devices and Android phone connect to the AP using WiFi. The AP, sniffer, and attacker connect to the Ethernet switch. We interact with IoT devices for 24 hours to collect benign traffic while the sniffer captures the traffic in pcap files. These interactions include various real-time activities that can occur during regular device usage.

We launch three types of DDoS attacks against IoT devices, namely ICMP, TCP-SYN, and UDP floods. While the sniffer records the attack traffic’s pcap files, the attacker launches each type of attack for 10 minutes against the individual IoT device. This process produces a dataset of 3,066,585 packets, composed of 1,264,392 malicious packets and 1,802,193 benign packets.

To confirm the machine learning model’s robustness, we also adopt the UNSW dataset consisting of 802,580 benign packets. The dataset consists of the following ten smart home devices — Wemo Motion Sensor and Power Switch, Samsung and Netatmo Camera, TP-Link Plug, Hue Bulb, Amazon Echo, Chrome Cast, iHome, and Lifx lightbulb. We combine both benign datasets, i.e., our dataset (SIOTLAB) and UNSW lab. Further, the DDoS traffic is joined with the benign dataset. In our previous work, we identified 20 seconds as the optimal polling interval when KNN achieves accuracy greater than 95% for device identification and DDoS detection using the following novel feature set. (1) Protocol percentage: for each flow data, ICMP, TCP, and UDP percentage is calculated for both benign and DDoS traffic. (2) IP diversity ratio: calculated as the number of unique IP addresses divided by the total packets sent by a device. (3) Packet count and size.

III. KNN IMPLEMENTATION ON FPGA

A. KNN

KNN is simple and easy to implement for the following reasons. Firstly, during the training phase, the data is stored in memory, so there is no need to build the model. Second, KNN has one hyperparameter to tune. However, KNN gets significantly slower as the dataset size increases. To overcome this challenge, we identify the minimum training samples necessary to achieve accuracy greater than 95%.

An instance of KNN calculates distances from each of the elements in an input training dataset to a query from the testing dataset and classifies the query by returning the mode of the sorted k nearest neighbors, where k is the hyperparameter. A query is classified by finding the mode or most common nearest neighbor. This process can be described by several tasks: calculating all of the neighbors’ distances, finding the closest neighbors, and evaluating the mode of these neighbors.

The closest neighbors are determined based on a distance metric evaluated on the query against each of the training data points. We utilize the Manhattan distance metric to avoid computationally intense operations such as square roots. Next each data points is sorted based on the distance from the query. This step is the most computationally-intensive task of KNN because it may require sorting the entire input dataset. This results in an algorithmic complexity that is linear with the size of the data multiplied by the number of features.

FPGAs have the potential to greatly reduce the run time of KNN by running the tasks in parallel. Pipelining and unrolling the distance calculations for the training data points and sorting
Algorithm 1: K-Min Sorting Algorithm for KNN

Input: The training data train, their labels train_labels, and a test query query.
Output: The classification of the test query.

distances[k] ← {∞};
labels[k] ← {l};
foreach e ∈ train and l ∈ train_labels do
    tmp_dist ← distance(e, query);
    tmp_max ← max(distances);
    if tmp_dist < distances[tmp_max] then
        distances[tmp_max] ← tmp_dist;
        labels[tmp_max] ← l;
end
return mode(labels);

the k nearest neighbors, it is possible to drastically shorten the classification process.

B. Sorting Algorithms used by KNN

In order to thoroughly test the extent of current FPGA optimization techniques, we implement the KNN algorithm using High Level Synthesis (HLS) and evaluate the performance of several common sorting algorithms including Bubble Sort, Merge Sort, Odd-Even Sort, and Enumeration Sort. These sorting algorithms are compared against the proposed custom algorithm (K-Min Sort).

1) Bubble Sort: The Bubble Sort produces a partially sorted array in order to take advantage of the limited number of neighbors required to produce a high accuracy using KNN, and only sort the minimum number of values defined by k. This is done by implementing k comparison steps or bubbles. Since the bubbles that traverse the input array only compare adjacent elements, each comparison bubbles can run independently of another, and can sort elements simultaneously. The small bubble count and easy parallelism makes this implementation of Bubble Sort an effective option for FPGA platforms.

2) Merge Sort: There exist several Merge Sort variations that are known to be effective when run on parallel platforms. While some combine the design concepts of other sorting techniques like bitonic sort or quick sort, their function is necessarily the same and reflects the basic Merge Sort model. Resource utilization can be high for parallel Merge Sort algorithms, but their speed makes them effective for certain applications, including time-sensitive edge computing IoT systems for example DDoS detection. The Merge Sort variation implemented here follows the traditional model. The incoming data is continually bisected and each of the resulting parts is sorted and merged to produce the desired fully sorted array.

3) Enumeration Sort: Enumeration sort has the potential to be a good fit for the parallel structure of the FPGA fabric. This algorithm determines data points’ positions in a final sorted array by comparing each element to every other. Memory accesses can be minimized since elements are not swapped or moved multiple times, making this sorting algorithm easily parallelizable.

4) Odd-Even Sort: Odd-even sort has the potential to reduce memory accesses and improve performance for KNN. This algorithm consists of two phases, an even phase and an odd phase, in which pairs of elements in a dataset are compared and swapped. By alternating between even and odd pairs of data each comparison step can be parallelized. However, arranging Odd-Even Sort in this manner increases its space complexity greatly, making area the primary limitation with this algorithm.

5) The proposed K-Min Sort: In order to outperform the previous algorithms, we propose a custom sorting algorithm called K-Min Sort. As seen in Algorithm 1, the distances between the test query and each element of the training data are calculated and evaluated in the same loop iterations. Of these distances only k are recorded, which reduces the sorting task while maintaining KNN’s accuracy, and the input dataset only needs to be traversed once. By combining the distance metric and sorting steps we minimize the run-time complexity and number of memory accesses required to retrieve and store the data and distances. This combined step can be additionally pipelined on the FPGA as another performance benefit. In place of a separate sorting step, Algorithm 1 only compares the distance of each training data point to the furthest of the recorded neighbors at a given point in time. As such, the number of comparison operations is minimized, proportional to the size of the input dataset.

Despite their similarities, K-Min sort performs fewer comparisons and memory accesses than the Bubble Sort algorithm since it does not perform swap operations on each element of the input dataset. Both algorithms traverse the training distances dataset, only sort k distance, and can be parallelized in a similar manner, but K-Min sort does so with a lower resource overhead. The Merge, Enumeration, and Odd-Even algorithms each sort all of the training data point distances in order to select the k values necessary for KNN after, but by parameterizing k K-Min and Bubble Sort avoid this excess computation.

C. HLS Simulation

High-level synthesis (HLS) interprets and implements high level language algorithms in register transfer language (RTL) for specific hardware platforms. HLS is capable of efficiently optimizing algorithms for particular hardware systems, enabling developers to work at a high level of abstraction. This work makes use of the HLS system in the Vivado Design Suite. Since we accelerate KNN using an FPGA, we need to be able to control the HLS synthesis process to make the most of the available resources on the low-cost hardware platform. To this end, Vivado provides tools for kernel optimization, function inlining, pipelining, loop unrolling and optimization, and array optimization. Finally, our results are extracted in a physical implementation as well as simulation results from HLS.
IV. RESULT AND DISCUSSION

We utilize the KNN implementation in the Scikit-learn Python library to generate test and train datasets with various size at 1%, 5%, 10%, 30%, 50%, 70%, 90% splits. The same tool is used to run a 10-fold cross validation (CV). The 10-fold CV accuracy is presented in Figure 2 along with the test accuracy for both the default value (i.e., \( k = 5 \)) and optimized values. Figure 2 shows that as the training dataset size increases, the 10-fold CV and test accuracy increases. Further, as seen in Figure 2, the accuracy exceeds 95% at the 50% dataset split for the default \( k \) value, and is maintained with the reduced, optimal \( k \). By optimizing \( k \), the amount of calculations required by KNN are minimized without a loss in accuracy. The optimized \( k \) value for the different dataset sizes is then implemented and tested in HLS on the FPGA platform. Figure 2(a) and 2(b) show the ranges of execution times of KNN for the 5 tested sorting algorithms. The data is gathered from HLS C synthesis reports, which approximate each algorithm’s latency with high accuracy as the train-test split percentage changes. The algorithms in Figure 3(a) are compiled in HLS with the default \( k = 5 \), while Figure 3(b) is compiled in HLS using optimal values for \( k \).

When an HLS C synthesis report is generated, the Vivado system evaluates the critical path of an implementation and determines its latency from the known execution times of common operations, including data manipulation, memory accesses, and movement. However, HLS does not attempt to calculate latency values when a single critical path cannot be isolated, which may occur as a result of embedded loops and memory dependencies. Nevertheless, the `loop_tripcount` pragma enables HLS to estimate the minimum and maximum latencies when a critical path cannot be immediately found by the compiler. Our work provides HLS simulation times combined with FPGA execution times in an Artix-7 FPGA. The HLS Simulation results are shown in Figure 3 and the resource utilization for the algorithms and the FPGA resource consumption are shown in Tables 1 and 2. Furthermore, our results are compared to CPU execution times for a x86 processor with two cores and four threads on a 2017 MacBook Air to compare performance in Table 3. The small embedded Artix-7 is able to achieve significant increases in performance even against a multi-core and multi-threaded CPU implementation.

As Figure 3(a) shows, the K-Min KNN solution performs very well with a minimum latency of \( 6.5 \times 10^3 \) clock cycles at the 1% dataset size and \( 580 \times 10^3 \) at 90%. It lies just above the minimum latency of the Merge Sort algorithm at each dataset size, differing by a few percent. The HLS synthesis performance report lists the same value for this algorithm’s minimum and maximum latencies at each percentage because it is well suited to the FPGA platform and is parallelized easily in HLS. In Figure 3(b), we see that the K-Min sorting solution exhibits a 33% improvement in performance when the \( k \) parameter is optimized. This places the K-Min algorithm just below the minimum latency of Merge Sort at each dataset size. We see a similar case in Figure 3(a) when looking at Bubble Sort. Like the K-Min solution, Bubble Sort is highly parallelizable and its performance is proportional to the size of the input dataset, so its minimum and maximum latencies are equivalent. At a 1% dataset size, it takes \( 30 \times 10^4 \) clock cycles, and \( 3 \times 10^6 \) at 90%. Bubble Sort lies closer to the K-Min solution in Figure 3(b) and experiences a 53% increase in performance, a greater increase than all the other algorithms.

In Figure 3(b), we observe that the best performing algorithm according to minimum latencies is the K-Min solution while Bubble Sort follows in third. The Bubble Sort algorithm performs more slowly than the K-Min solutions as a result of the comparison and swap operations it requires. Bubble Sort stores more input data in memory than the K-Min solution, and the greater number of memory accesses that occur as a result slows down the KNN algorithm. This limitation of memory accesses and storage is one of the primary factors that the K-Min solution sought to remedy.

When looking at the performance of Merge Sort in Figure 3(a) and 3(b), we see that optimizing \( k \) does not have a significant impact on this algorithm, reflecting a change of less than 0.1%. The minimum and maximum latencies at the 1% dataset size are around \( 4 \times 10^3 \) and \( 3 \times 10^5 \) clock cycles in both figures, and are \( 8 \times 10^6 \) and \( 6 \times 10^{10} \) clock cycles at the 90% dataset size. The HLS C synthesis report provides a range of latencies due to the complexity of the algorithm.

The latency data for Odd-Even Sort is similar to that of Merge Sort; as seen in Figure 3(a) and 3(b), optimiza-


| Sorting Algorithm | CPU (ms) | FPGA (ms) |
|-------------------|----------|-----------|
| Odd-Even          | 1927200  | 297615    |
| Enumeration       | 1209000  | 281750    |
| Merge             | 150000   | 6024      |
| Bubble            | 34811    | 13.041    |
| Proposed K-Min    | 32519    | 3.913     |

| Sorting Algorithm | BRAM | DSP | FF | LUT |
|-------------------|------|-----|----|-----|
| Odd-Even          | 258  | 5   | 4084 | 3844 |
| Enumeration       | 642  | 5   | 3957 | 4204 |
| Merge             | 514  | 5   | 4372 | 4447 |
| Bubble            | 258  | 7   | 3880 | 3628 |
| Proposed K-Min    | 4    | 5   | 3886 | 3663 |

**TABLE I**

**TABLE II**

The performance gains of the other sorting algorithms is as expected. Due to the customization of the K-Min algorithm for an FPGA workload, our solution is able to obtain extremely optimized millisecond level performance, several orders of magnitudes faster, while only consuming 2.67% of the total Block Random Access Memory (BRAM), 4.17% of the DSP slices, 5.96% of the total Flip Flops (FF), and 11.24% of the total Look Up Table (LUT) space as seen in Table II. Therefore, this implementation is not only extremely fast, but also utilizes minimum resources on the FPGA to provide an optimal design achieving 95% accuracy at 3.9 millisecond speed.

V. RELATED WORK

FPGA platforms are cost effective and versatile for IoT and edge computing applications [12]. They are suitable for these tasks because they maintain steady throughput regardless of workload, have a high capacity for spatial and temporal parallelism, and are very energy efficient [13].

In existing work we see robust FPGAs used in large scale server-side applications to supplement network security. FPGA’s speed makes them useful for real-time network intrusion detection and device identification in closed critical industrial networks [14]. For example, a proposed k-means k-modes clustering architecture in [15] implements highly configurable input parameters with interconnected blocks to reduce the need for reconfiguration. [16] allows network parameters to specify pruning, data quantization, and precision without reconfiguration at run-time.

Acceleration techniques can be refined by evaluating KNN variations to find the most suitable for certain applications, but there is a lack of existing work comparing parallel KNN variations on FPGAs. This lack of exploration is similarly seen
of other prevalent ML algorithms whose acceleration could benefit IoT applications. The range and variety of optimization techniques made available by the parallelism of FPGAs and HLS reinvigorates KNN, whose improvements may benefit other algorithms as well.

Device identification has been accelerated with the use of fixed-point arithmetic [17] by using 16 and 8 bit precision to reuse hardware and reduce space and resource consumption. This also improves memory access efficiency for algorithms on FPGAs; it allows distant neighbors to be discarded early in KNN [18]. This modification is particularly useful for handling large datasets on FPGAs with few memory resources.

While these existing parallel acceleration techniques are informative, they are not designed for fast, real-time edge computing applications, but rather for server applications and the workloads of large scale data centers [19]. This absence of research regarding KNN for edge computing and IoT applications extends to the parallelization of sorting algorithms [5] [20]. Only niche applications of KNN acceleration exist for TCP/IP packet inspection [21], NIC outlier filtering [22], and flow-based network traffic attack detection [23].

This work expands on existing research, and accelerates the computationally intensive sorting and selecting task of KNN with a low-cost FPGA suitable for edge computing platforms. Traditional sorting algorithms like Merge [6] and Bubble Sort [5] are not feasible on small FPGAs. Therefore, to get the best performance and efficiency out of our low-cost system, we make use of several acceleration techniques with a custom sorting algorithm to develop a KNN solution that is well-suited to small-scale IoT networks.

VI. CONCLUSION

The proliferation of IoT devices requires increased flexibility for home network management and more lightweight and robust security solutions. Software-Defined Networking (SDN) and Machine Learning (ML) have been proposed as efficient solutions to provide device classification and malicious traffic detection. However, Field Programmable Gate Arrays (FPGAs) can further enhance this efficiency due to their fine-grained parallelism and parallel processing efficiency. This is demonstrated by the proposed FPGA-based KNN algorithm classifying a network flow with 95% accuracy in 4 milliseconds compared to the required 57 seconds on a CPU-based platform. This stark performance difference is indicative of the potential of FPGAs to benefit other ML algorithms which would otherwise be dismissed on CPUs due to the constraints of serial processing platforms. Our work hopes to encourage further research in using FPGA technology in edge networking applications due to its speed and energy efficiency.

REFERENCES

[1] “Cisco annual internet report - cisco annual internet report (2018–2023) white paper.” Cisco White Paper, 2020.

[2] A. Bujari, M. Furini, F. Mandreoli, R. Martoglia, M. Montangero, and D. Ronzani, “Standards, security and business models: key challenges for the iot scenario,” Mobile Networks and Applications, vol. 23, no. 1, pp. 147–154, 2018.

[3] H. Gordon, C. Batula, B. Tushir, B. Dezfuli, and Y. Liu, “Securing smart homes via software-defined networking and low-cost traffic classification,” arXiv preprint arXiv:2104.00296, 2021.

[4] N. Moustafa and J. Slay, “Unsw-nb15: a comprehensive data set for network intrusion detection systems (unsw-nb15 network data set),” in 2015 Military Communications and Information Systems Conference (MILCOM), 2015, pp. 1–6.

[5] Y. Pu, J. Peng, L. Huang, and J. Chen, “An efficient knn algorithm implemented on fpga based heterogeneous computing system using opencl,” in IEEE 22nd Annual International Symposium on Field-Programmable Custom Computing Machines, 2015, pp. 167–170.

[6] J. Lobo and S. Kuwelkar, “Performance analysis of merge sort algorithms,” in International Conference on Electronics and Sustainable Communication Systems (ICESC), 2020, pp. 110–115.

[7] Yasuura, Takagi, and Yajima, “The parallel enumeration sorting scheme for vlsi,” IEEE Transactions on Computers, vol. C-31, no. 12, pp. 1192–1201, 1982.

[8] A. Hematian, S. Chuprat, A. A. Manaf, and N. Parsazadeh, “Zero-delay fpga-based odd-even sorting network,” in IEEE Symposium on Computers Informatics (ISCII), 2013, pp. 128–131.

[9] “Vivado design suite.” [Online]. Available: https://www.xilinx.com/products/design-tools/vivado.html

[10] F. Pedregosa, G. Varoquaux, A. Gramfort, V. Michel, B. Thirion, O. Grisel, M. Blondel, P. Prettenhofer, R. Weiss, V. Dubourg et al., “Scikit-learn: Machine learning in python,” the Journal of machine Learning research, vol. 12, pp. 2825–2830, 2011.

[11] S. Rampersaud, L. Mashayekhy, and D. Grosu, “Computing nash equilibria in bimatrix games: Gpu-based parallel support enumeration,” IEEE Transactions on Parallel and Distributed Systems, vol. 25, no. 12, pp. 3111–3123, 2014.

[12] T. Gomes, S. Pinto, T. Gomes, A. Tavares, and J. Cabral, “Towards an fpga-based edge device for the internet of things,” in IEEE 20th Conference on Emerging Technologies Factory Automation (ETFa), 2015, pp. 1–4.

[13] S. Biookaghazadeh, F. Ren, and M. Zhao, “Are fpgas suitable for edge computing?” 04 2018.

[14] J. Kang, T. Kim, and J. Park, “Fpga-based real-time abnormal packet detector for critical industrial network,” in IEEE Symposium on Computers and Communications (ISCC), 2019, pp. 1199–1203.

[15] L. Andrade Maciel, M. Alcantara Souza, and H. Cota de Freitas, “Reconfigurable fpga-based k-means/k-modes architecture for network intrusion detection,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 8, pp. 1459–1463, 2020.

[16] L. Ioannou and S. A. Fahmy, “Network intrusion detection using neural networks on fpga socs,” in 29th International Conference on Field Programmable Logic and Applications (FPL), 2019, pp. 232–238.

[17] K. Alrawashdeh and C. Purdy, “Reducing calculation requirements in fpga implementation of deep learning algorithms for online anomaly intrusion detection,” in IEEE National Aerospace and Electronics Conference (NAECON), 2017, pp. 57–62.

[18] X. Song, T. Xie, and S. Fischer, “A memory-access-efficient adaptive implementation of knn on fpga through lfsrs,” in IEEE 37th International Conference on Computer Design (ICCD), 2019, pp. 177–180.

[19] D. Danopoulos, C. Kachris, and D. Soudris, “Fpga acceleration of approximate knn indexing on high-dimensional vectors,” in 14th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), 2019, pp. 59–65.

[20] L. Liu and M. A. S. Khalid, “Acceleration of k-nearest neighbor algorithm on fpga using intel sdk for opencl,” in IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS), 2018, pp. 1070–1073.

[21] S. Ponnamaraj, R. Rashmi, and M. V. Anand, “Lds based network security architecture with tcp/ip parameters using machine learning,” in International Conference on Computing, Power and Communication Technologies (GUCON), 2018, pp. 111–114.

[22] A. Hayashi and H. Matsutani, “An fpga-based in-nic cache approach for lazy learning outlier filtering,” in 25th Euromicro International Conference on Parallel, Distributed and Network-based Processing (PDP), 2017, pp. 15–22.

[23] L. Chen, S. Gao, B. Liu, Z. Lu, and Z. Jiang, “Few-ann: A fuzzy entropy weighted natural nearest neighbor method for flow-based network traffic attack detection,” China Communications, vol. 17, pp. 151–167, 05 2020.