An Absolute-value Detector with Threshold Comparing for Spike Detection in Brain-machine Interface

Mingzheng Yuan*
Miami College, Henan University, Kaifeng 475000, China
*Corresponding author e-mail: 1838020028@vip.henu.edu.cn

Abstract. This research designs an absolute-value detector with the function of threshold comparing. Specifically, it is an essential device in the spike detection of the brain-machine interface. The optimized design in the research can accomplish the main functions in spike detection and has good performance in both delay and energy consumption. It comes up with two types of design at the beginning. To make the design reliable and comprehensive, it decides to discuss both methods in this paper. The first design is using a full adder, multiplexer and comparator. The concept of its logic circuit is adding the logic one to the input when the given input data is negative, keeping the original information as the given input data is positive. To achieve the function of adding, this study chooses the full adders. The primary purpose of using multiplexers is to select from the processed input and original input, and the choice depends on the most significant bit (MSB) of the input data. To compare the absolute value of the input data with a given threshold, this research used a multi-bit comparator. The second design is based on the fundamental algorithms of calculating total numbers. It indicates that this study can operate it with the threshold value through a subtractor when the input is negative. On the contrary, an adder can be used when the information is positive. Based on the concept of logic optimization, this study chooses to use the only subtractors, and it just needs to focus on the borrow bit, which can indicate the more significant number. By connecting the MSB of the input with the subtractors through XOR gates, the selection can be achieved without using any multiplexer. In the process of removing and replacing the devices, it reached the optimization of the design. Then, this paper compared the minimum delay by calculating each stage’s size and finding that the second design is better. Finally, based on the dual design, this essay computed the energy consumption in the circuit and implement $V_{DD}$ optimization to obtain the minimum energy.

1. Introduction
The human brain is one of the most significant components in the human body, and it is responsible for most human activities. The human brain consists of billions of neurons and they are communicating with each other through electrochemical processes. Based on the electro-chemical properties, this research can obtain practical information by processing and analyzing the neural signals. The neurons in the human brain can excite the action potentials, and this mechanism allows neurons to reliably transmit information over long distances without transmission attenuation. Additionally, the action potentials can be detected as spikes when exceeding a specific threshold value. However, it is inevitable that the extracted signals may have multiple components, including background noise signals and specific neural signals. To obtain accurate signals and describe correct neural activities, it is essential to introduce spike sorting, which separates the electrical activity of individual neurons from noisy recorded signals [1].
The Spike-sorting algorithms have gained much interest in the research community with the recent advancements in neural signal acquisition systems. Considering the existence of the background noise signals and chaotic spike activities, it is essential for researchers to detect the accurate and effective neural signals. However, farfarrigous methods are applied to accomplish spike detection in current studies. This research is to design one of the commonly used spike-detection algorithms, a 4-bit threshold-value comparator with absolute-value detection.

The logic function of this design mainly includes two parts, one is to detect and process the absolute value of the signal, and the other is to compare the processed signal with the specific threshold value. To achieve these logic functions, it comes up with two types of designs. The first design uses full adders to add logic when the value of neural signal is negative, which is actually the function of absolute-value detection. In addition, multiplexers are used to choose between the processed neural signal and the original neural signal. The second design abandons full adders and multiplexers for better performance of the circuit as adders and multiplexers can lead to more significant energy consumption and longer delay. However, to make this research effective and comprehensive, it analyzes both of the designs. This study finds the critical paths of these two circuits and calculated the corresponding delay of the two critical paths. After calculating the minimum delay of each critical path, it can be illustrated from the results that the second design has better performance. Based on the second design, this research implements further analysis, including computing the minimum energy consumption and discussing the relationship between delay and energy consumption.

2. Spike Detection

Brain-machine interface (BMI) is a direct connection path established between human or animal brain (or brain cell cultures) and external devices. In a one-way brain-machine interface, the computer either accepts commands from the brain or sends signals to the brain. In the early stages of research in the field, recognizing user’s intentions through a BMI was exploited mainly in the communications domain [2]. However, more recently, researchers have opened up new directions for BMI, especially in the field of brain-controlled robotic devices [3]. This technique also has many vital applications in biological, medical and other academic fields. Considering the practical value of BMI technique in multidisciplinary areas, it has become one of the most valuable interdisciplinary techniques in the current research.

Figure 1 demonstrates the working principle of a classic BMI through a block diagram. Firstly, the activities of neurons are detected by microelectrode arrays which can accurately separate the electrical signals of a single cell, and record the signs of almost all neurons in the sample. Using the current technique of the CMOS-based high-density microelectrode arrays (HD-MEAs), the neurites of brain cells can be drawn, and electrical signals of substructures such as cell bodies and axons can be detected as well [4]. Then after amplifying and filtering, the neural signals are still combined with background noise signals. On account of this, the spike sorting is implemented to eliminate the surrounding noise, and it can also regulate and cluster the processed signals. Finally, the decoded signals can issue specific instructions and commands to external devices to achieve corresponding control.

However, this research focuses on spike detection, which is mainly responsible for eliminating ambient noise. Spike detection is commonly used in two stages, pre-emphasis and thresholding. The neural signals are processed for the pre-emphasis by detecting the absolute value at first [5]. As the neural signals are emitted and received through a discrete waveform, this study has to implement the non-linear energy operator (NEO) and discrete wavelet transform (DWT) as the processes of neural signals [6,7]. The next step is thresholding. The main idea is to compare the neural signal, or the pre-emphasized signal, to a threshold value. A spike is detected when the neural signal crosses an assumed threshold [8]. Figure 2 is the overall procedure for constructing the design that achieves the functionality needed. It can be seen from this figure that this design is mainly divided into two stages, detecting and thresholding. However, this procedure has formed the overall idea and framework of the design. At the next stage of this research, it focuses on two main steps, including the absolute-value detection and thresholding comparison.
3. Circuits and Topology

This section concludes the crucial algorithms for constructing an absolute-value detector. Then two types of designs are introduced to fulfill the implementation of the absolute value detection and comparison. After that, it discusses both methods by calculating the delay and energy consumption of the critical path. Based on the calculation results, this part is able to choose the optimal one and do further research and analysis.

3.1. Algorithms of Absolute-value Detector

For constructing a design that can detect the absolute values of neural signals and compare them with specific thresholds, it is essential to sort its key algorithms and main ideas [9,10]. For the absolute-value detector, the most significant algorithm is adding a logic “1” to the inverted input number when the input is negative. To achieve the function of inverting and adding, this study has to introduce the fundamental algorithm which is the magnitude of 2’s complement number. In the 2’s complement representation of binary numbers, the most significant bit (MSB) is represented as the flag bit to determine positive and negative input numbers. Then it can determine the magnitude of the 2’s...
complement number by checking the best bits of the input numbers. On account of this, it can decide on the optimal design, and further analysis can be implemented based on it.

3.2. First Design
To accomplish the functions of absolute-value detection and thresholding comparison, this paper arises two types of designs at the early stage of constructing circuits and topology. First design chooses to use the devices including full adder, invertor, multiplexer and comparator. As shown in Figure 3, this research separates the input neural signals into two parts, MSB and magnitude. What is mentioned above is that the volume has to be inverted, and added “1” for the input is negative, and it remains still for the positive input. Thus, this study uses inverters and full adders when processing the input data. Then the processed data and original data are presented as the input data of the multiplexer, and the MSB is acting as the select signal, which can determine whether it is a positive signal or a negative signal. Finally, the output of the multiplexer is sent to a comparator and compared with a specific threshold.

![Figure 3: Basic Flow Chart of the First Design](image)

This research assumes that the input neural signal is a 4-bit binary number and is given in 2’s complement format. In this case, it needs a 3-bit full adder (Figure 4) to add the magnitude part of the input data. To do the addition operation of the 3-bit number bit by bit, the carry bits also have to be considered. The 3-bit full adder consists of six input signals which include three bits of the input neural signal (A0, A1, A2) and three bits of the adding number “1” (B0, B1, B2). In addition to the sum of two numbers in the home position, this research has to consider adding the rounding from the lower part, which are the carry bits (C0, C1, C2, C3). Lastly, the S0, S1, S2 are represented as the output data of this 4-bit adder [11].

![Figure 4: A 3-Bit Full Adder](image)

Multiplexers are used to choose between the processed input signal and the original signal, which is called absoletion-value detection. To obtain the correct output, choices made by the multiplexers depend on the Most Significant Bit (MSB) of the input data. When the MSB of the input data is “1” which indicates the input data to be harmful, the processed input signal is selected by the corresponding multiplexer. Otherwise, the original signal is determined by the multiplexer as the MSB of the input data.
is “0”. Thus, this research builds a 2-to-1 multiplexer, and its logic circuits schematic is shown in Figure 5.

![Figure 5: A 2-to-1 Multiplexer](image)

After the multiplexer processes the input data, the output data is directly compared with the given threshold in the comparator which is described in Figure 6. This figure demonstrates the logic circuit schematic of a 3-bit comparator, and the data processed previously become the input of this comparator. A single-port output of the comparator presents the result. If the magnitude of the input signal is greater than the threshold, its output should be a “1” (high logic value), otherwise the production should be a “0” (low logic value) [12].

![Figure 6: A 3-Bit Magnitude Comparator](image)

Based on the devices above, this paper designs an absolute-value detector with the function of threshold comparison. Figure 7 is the complete logic circuit schematic of the first design, and it is apparent that it is divided into three main parts: full adder, multiplexer, and comparator. When the input neural signals are applied, the multiplexers read the MSB of inputs and select corresponding branches, which allow the absolute-value data to transmit. Meanwhile, the absolute-value data are processed in the 3-bit full adder before being determined by the multiplexers. Finally, the outputs of multiplexers are compared with the given thresholds in a 3-bit magnitude comparator.
3.3. Second Design

Previous part has accomplished the logic circuit schematic of the first design and described the main components. However, as it reviewed the schematic of the first design, a large number of gates and logic devices are used. Consequently, the performance of this design may be affected negatively as gates increase delay and energy consumption. On account of this, it comes up with another type of design based on logic optimization.

Firstly, this essay reviews the basic idea of the design. In calculating the absolute-value numbers in the fundamental algorithm, it denotes the threshold and the input by $T$ and $A$. Thus, differencing these two numbers (information is in the form of absolute value) it has the equation expressed in (1).

$$T - |A| = \begin{cases} T - (-A) = T + A \\ T - A \end{cases}$$

Therefore, this study compares the input with the given threshold by determining the difference between them. It can be seen in Figure 8 that this paper uses subtractor and adder to do the calculations above. Similar to the first design, it utilizes a multiplexer to implementing the selection between positive input and negative input. Finally, it can accomplish the comparison by checking out the difference between input and threshold.

Based on the concept of logic optimization [13], this research puts more emphasis in optimizing the circuit in the second design. By comparing the adder and subtract, this study finds the only difference is
that one is counting a borrow bit and another is counting a carry bit. For threshold is removed by input data, the borrow bit of the highest bit exists when the input data is greater than the threshold. On account of this, this study chooses to use only subtractor and it just needs to focus on the borrow bit which can indicate the greater number. Moreover, by connecting the input with the subtractors through XOR gates, it can achieve the judging without using any multiplexer. In the process of moving and replacing devices, this paper performs the optimization of the design.

![Figure 9: The Logic Circuit Schematic of the Second Design](image)

4. Critical Path Analysis
In the last stages, it has come up with two types of design and described them in detail. To discuss and compare both designs, this paper analyzes their critical paths respectively which means the single path with the worst slack [14]. The critical approach of a circuit reflects the overall performance in delay and energy consumption. Therefore, it performs the critical path analysis for both of the designs.

![Figure 10: The Critical Path of the First design and the Second Design](image)

To calculate and analyse the critical path delay, this research performed derivation of relevant algorithms at first.

\[ f^* = N \sqrt{PathEffort} \]  \hspace{1cm} (2)
\[ f^N = \prod g \cdot h = PathEffort \quad (3) \]

Therefore, the study starts with the last stage of the schematic and derives the sizing of each stage from back to front.

\[ C_{in} = g \frac{C_{out}}{f^*} \quad (4) \]

Based on the parameters above, this paper can have the derivation of the minimum path delay which is the critical parameter it is looking for. And the minimum path delay is expressed as Equation (5).

\[ D_{min} = \sum (g_i \cdot h_i + p_i) = N \cdot f^* + P \quad (5) \]

However, it still needs to calculate and analyse the energy consumption of the critical path circuit based on the delay time. For the calculations above, “delay” refers to the worst-case propagation delay. The energy this research is about to compute refers to the total energy drawn from \( V_{DD} \) for a given input probability distribution. To find the optimal \( V_{DD} \), this study has to derive from the relation between minimum delay and energy. It can be assumed that the delay is proportional to \( V_{DD} \) as Equation (6) to find optimal \( V_{DD} \) at minimum energy consumption. While \( V_{DD}^{M delay} \) is the \( V_{DD} \) at minimum delay. Finally, the energy consumption can be solved by the Equation (7).

\[ \frac{V_{DD}^{Opt}}{(V_{DD}^{Opt} - V_T)^2} \]

\[ \frac{V_{DD}^{M delay}}{(V_{DD}^{M delay} - V_T)^2} \]

\[ P = C_L \times V_{DD}^2 \times (W_p + W_N) \quad (7) \]

5. Results

Based on the derivations in the previous analysis, this study can compute the specific numbers and elicit the result of this research. To specify the calculation and rationalize the research findings, this research declares the conditions and constraints of this design. It is assumed that the \( C_{parasitic}/C_{gate} \) equals to 1 and \( V_T \) equals to 0.2V. Moreover, the input signal is a 4-bit number represented in 2’s complement format. The threshold value (3-bit binary) is fixed and you can assume a mid-range value for this Threshold. Assume that each bit of the input has an equal probability of being 0 or 1 and the bits are mutually independent. The input capacitance of all inputs (A0-A3) is less than or equal to 2-unit sized inverters (see below for the definition of the unit-sized inverter). For design purposes, the inputs to adder are driven by a unit sized buffer (chain of two-unit sized inverters). The delay is measured as the delay after the input driver (2 inverters) to before the load (32 times unit sized inverters). The output bit is loaded with CL = 32 unit-sized inverters. \( V_{DD} \) is 1V when the minimum delay is applied. Lastly, it is assumed that the unit-sized inverter is \( W_p = 650nm, W_N = 430nm, Lp = Ln = 100nm \).

For the minimum delay of both designs, this paper has the result as follows. Sizes of each stage is shown in Table 1. The minimum delays are presented in Table 2, and it finds that the second design has better performance in delay. Thus, the further computations and analysis are based on the dual design. The \( V_{DD} \) at the minimum energy consumption and the minimum energy consumption are presented in Table 3. Each logic gate in Table 3 is labelled in order from the end of the critical path to the beginning.
| Gates in the 1st Design | Size | Gates in the 2nd Design | Size |
|------------------------|------|------------------------|------|
| \( C_{in15} \)        | 41.92| \( C_{in10} \)        | 27.28|
| \( C_{in14} \)        | 30.51| \( C_{in9} \)         | 18.60|
| \( C_{in13} \)        | 22.20| \( C_{in8} \)         | 15.86|
| \( C_{in12} \)        | 12.90| \( C_{in7} \)         | 10.82|
| \( C_{in11} \)        | 5.63 | \( C_{in6} \)         | 9.22 |
| \( C_{in10} \)        | 4.10 | \( C_{in5} \)         | 6.29 |
| \( C_{in9} \)         | 2.39 | \( C_{in4} \)         | 5.36 |
| \( C_{in8} \)         | 4.17 | \( C_{in3} \)         | 3.66 |
| \( C_{in7} \)         | 7.30 | \( C_{in2} \)         | 1.87 |
| \( C_{in6} \)         | 5.30 | \( C_{in1} \)         | 3.83 |
| \( C_{in5} \)         | 3.08 |
| \( C_{in4} \)         | 2.24 |
| \( C_{in3} \)         | 1.30 |
| \( C_{in2} \)         | 2.31 |
| \( C_{in1} \)         | 1.01 |

Table 2: Minimum Delay for Both Designs

| Minimum Delay for the 1st Design | 81.35 |
|---------------------------------|-------|
| Minimum Delay for the 2nd Design| 48.5  |

Table 3: Minimum Energy Consumption for the 2nd Design

| \( V_{DD} \) at the Minimum Energy Consumption | Minimum Energy Consumption |
|-----------------------------------------------|---------------------------|
| 0.7754                                        | 2076                       |

6. Conclusion

This research comes up with two types of design at the beginning. To make the design reliable and comprehensive, it decided to discuss both designs in this paper. The first design is using full adders, multiplexers and a comparator. The concept of this circuit is adding the logic one to the input when the given input data is negative, and keeping the original input as the given input data is positive. To achieve the function of adding, this study chose the full adders. The main purpose of using multiplexers is to choose from the processed input and original input, and the choice depends on the most significant bit (MSB) of the input data. To compare the absolute value of the input data with a given threshold, it used a multi-bit comparator. The second design concept is based on the fundamental algorithms of the calculation of the absolute numbers. It means when the input is negative, this study can operate it with the threshold value through a subtractor. On the contrary, it can use an adder when the input is positive. By comparing the adder and subtractor, this research found the only difference is that one is counting a borrow bit and another is counting a carry bit. On account of this, it decided to use the only a subtractor, so that can delete the borrow bits when it does not need to consider the borrow bits. By connecting the input with the subtractors through XOR gates, this paper can achieve the judging without using any multiplexer. In the process of moving and replacing devices, it reached the optimization of this design. Finally, this essay compared the minimum delay by calculating each stage’s sizing and finding that the second design is better. Based on the second design, it calculated the energy consumption in the circuit and do \( V_{DD} \) optimization to get the minimum energy consumption.


References

[1] Lewicki M S. A review of methods for spike sorting: the detection and classification of neural action potentials[J]. Network, 1998.
[2] Birbaumer N, Ghanayim N, Hinterberger T, et al. A spelling device for the paralysed. [J]. Nature, 1999, 398(6725):297-298.
[3] Noninvasive Brain–Machine Interfaces for Robotic Devices[J]. Annual Review of Control Robotics and Autonomous Systems, 2021, 4(1).
[4] Single-Cell Electrical Stimulation with CMOS-based High-Density Microelectrode Arrays[J]. Frontiers in Cellular Neuroscience, 2018, 12: -.
[5] Obeid I, Wolf P D. Evaluation of spike-detection algorithms for a brain-machine interface application. [J]. Biomedical Engineering IEEE Transactions on, 2004, 51(6):905-911.
[6] Kaiser J F. On a simple algorithm to calculate the 'energy' of a signal[C]. International Conference on Acoustics. IEEE, 2002.
[7] Kim K H, Kim S J. A wavelet-based method for action potential detection from extracellular neural signal recording with low signal-to-noise ratio. [J]. IEEE transactions on bio-medical engineering, 2003, 50(8):999-1011.
[8] D Valencia, Alimohammad A. Neural Spike Sorting Using Binarized Neural Networks[J]. IEEE Transactions on Neural Systems and Rehabilitation Engineering, 2020, PP(99):1-1.
[9] Sikandar Kumar,Subha P. Eswaran. Improved Spectrum Sensing Schemes Using Prewhitening and Weights Under Spatially Correlated Noise[J]. Wireless Personal Communications,2020,115(prepublish).
[10] M. Hirata,S. Nagashima,T. Cho,J. Kohagura,M. Yoshida,H. Ito,S. Tokioka,T. Numakura,R. Minami,Y. Nakashima,T. Kondoh,K. Yatsu,S. Miyoshi. A Novel Electrostatic Ion-Current Absolute-Value Detector Under Circumstances with Simultaneous Electron Incidence by The Use of a Proposed “Self-Collection” Method for Secondary Electron Emission[J]. Fusion Science and Technology,2003,43(1T).
[11] S. Prema. Comparative Analysis of Different Full Adder Circuits[J]. Programmable Device Circuits and Systems,2013,5(2).
[12] Efstatious Constantinos,Kitsos Paris. Efficient majority logic magnitude comparator design[J]. Microprocessors and Microsystems,2021,82.
[13] Lee Seong Bong, Chong Jong Wha. A Rule-Based System for VLSI Gate-Level Logic Optimization[J]. Journal of the Korean Institute of Telematics and Electronics,1989,26(1).
[14] Chang-Lin Li,Hyun Joong Kim,Seo Weon Heo,Tae Hee Han. Voltage and Frequency Tuning Methodology for Near-Threshold Manycore Computing using Critical Path Delay Variation[J]. Journal of Semiconductor Technology and Science,2015,15(6).