A 0.6V high-swing gate-switching charge pump for PLL with current self-matching technique in 28nm CMOS

Dezheng Zhu1, Chao Chen2, Yan Zhao2, Chenglei Peng1 and Zhikuang Cai3

Abstract This letter presents a low voltage high-output-swing gate-switching charge pump (CP) used in phase-locked loops (PLL). The current self-matching technique is proposed to dynamically bias the gate of the current source transistors corresponding to output voltage fluctuation, keeping charging and discharging currents constant. To overcome the voltage margin issues under low supply voltage, a master-slave rail-to-rail operational trans-conductance amplifier (OTA) structure is proposed as the error amplifier of the negative feedback loop. The current mismatch of less than 2% is realized in the voltage range from 0.05V to 0.55V. A prototype of the proposed CP is designed and fabricated in TSMC 28nm CMOS process under a 0.6V supply voltage. Charging and discharging currents are designed to be identical during the entire reset impulse. The measured reference spur is less than -59.4 dBc.

key words: charge pump, PLL, CMOS, self-matching technique
Classification: Analog Circuits, frequency Synthesizers

1. Introduction

Supply voltage shrinkage is a prevalent approach in RF transceiver design for lowering the power consumption of portable wireless devices, in which a long charging cycle is a primary goal among all the performances [1–8]. Furthermore, a lower supply voltage is inevitable due to breakdown issues in modern deep-submicron processes [9, 10]. Unfortunately, the threshold voltage is not much reduced in consideration of current leakage. This brings great difficulties to assign adequate voltage headroom for conventional analog circuits [9].

For a typical charge pump (CP) used in the frequency synthesizer, negative feedback loops are employed to guarantee the charging and discharging current matching [10, 11, 12]. Unfortunately, it can't work properly under low supply voltage below 0.7 V since numbers of stacked transistors are used inside of the operational trans-conductance amplifier (OTA) [13]. Some previous works use open-looped source switching structures as expediency [14, 15, 16]. However, it is inferior in current matching and reference spurs. Meanwhile, the voltage drop on the source switches consumes a non-neglectable portion of the available output swing which is valued in low voltage design. For regular voltage designs, various techniques are proposed by previous works to improve the reference spurs [17–28]. However conventional techniques such as cascode and negative feedback can hardly work under low supply voltage because of the deficient voltage margin. To save voltage headroom for the CP's output swing, gate switching CP [29, 30] is a more promising solution than the source switching and drain switching structures, as shown in Fig.1(a). The efficient output voltage range is between $V_{DSATN}$ and $V_{DD}-V_{DSATP}$, which are the overdrive voltage of the charging and discharging transistors. However, the open-looped structure results in poor current matching and reference spurs. In this letter, a novel gate-switching CP with the current self-matching structure based on master-slave OTA is proposed. With gate-voltage dynamically compensated the current variation due to output voltage fluctuations, the charging and discharging current keep constant for a wide output range from 50 mV to $V_{DD}$-50 mV. Simulation and measurement results also indicate less than 2% current mismatching and less than -59.4 dBc reference spur are realized.

2. Circuit Design

The schematic of the proposed gate-switching CP is shown in Fig.1(b). Charging and discharging currents are provided by P1 and N1 respectively, which are controlled by digital impulse signals CPP and CPN. The impulse generator is powered by 1V $V_{DD}$ to guarantee fast switching speed and low on-resistance. With error amplifiers A1 and A2 which are rail-to-rail master-slave OTA shown in Fig.2, the current of P1 copies P2 and the current of N1 copies N2. A2 makes the drain terminal of the input reference current source equal to the core Vdd of 0.6V, keeping the reference current constant. More importantly, A2 controls the gate of N1/2, making its

1 School of Electronic Science and Engineering, Nanjing University, Nanjing 210023, China
2 National ASIC Center, Southeast University, Nanjing 210096, China
3 School of Electronic and Optical Engineering, Nanjing University of Posts and Telecommunication, Nanjing 210023, China
a) pcl@nju.edu.cn

DOI: 10.1587/elex.18.20200441
Received December 22, 2020
Accepted December 25, 2020
Publicized January 08, 2021

This article has been accepted and published in J-STAGE in advance of copyediting. Content is final as presented.
current equal to the reference current all the time. A1 tracks the output voltage and dynamically changes the gate voltage of P1/2, compensating the current variation caused by the output voltage fluctuations. The charging and discharging current can be set constant even if N2 and P2 being forced into the triode region. Smoothing capacitor C1 and C2 are to provide charges for the charging and discharging switches, which helps to achieve steep on-edges in time-domain. In high-speed operation, the charging and discharging current are highly consistent under different output tuning voltages, which is the key for rejecting reference spurs. The branch of P2 and N2 is one of the output branches of the bandgap reference, which is powered by 1V $V_{DD}$. With the output terminal of the reference branch being fixed to the 0.6V core supply voltage, the currents of P2 and N2 are always constant.

A low voltage rail-to-rail OTA is also proposed in this letter to act as the error amplifiers in the CP, as shown in Fig. 2. Complementary gm stages are applied and their currents are superimposed by the common-gate stage. The master-slave structure compresses the $V_{DS}$ of current tails, saving the voltage margin for input common-mode voltage and eliminating the dead zone near half of the supply voltage. Here taking the PMOS input stage to explain the principle of the master-slave structure, the first stage acts as a slave stage that consists of the tail current transistor ($M_3$), the differential pair ($M_{1a}$ and $M_{1b}$), and the current-mirror load ($M_{1a}$ and $M_{1b}$). The master stage replicates the tail current source and the trans-conductance transistor of the slave stage, which means $M_{2a}$, $M_{2b}$, and $M_4$ are the copies of $M_{1a}$, $M_{1b}$, and $M_3$ respectively. To save voltage margin, both $M_3$ and $M_2$ are biased in the near-linear region. The drain-source voltage of $M_{2a}$ is defined as $V_{DSL}$, which is tens of mV. The minimum supply voltage, therefore, is $V_{TH} + 2 \cdot V_{OV} + V_{DSL}$. The drain terminals of $M_{2a}$ and $M_{2b}$ are connected to the drain terminal of the current source $M_5$ and the gate of the $M_4$, forming a negative feedback loop. When the input voltage of the OTA changes, the negative feedback loop automatically adjusts the gate voltage of $M_5$ to make its current equals the current source of $M_3$. Since the master stage accurately replicates the slave circuit, the current flowing through $M_3$ remains constant.

Fig. 3 shows the simulated static charging and discharging current versus output voltage of the proposed CP(solid lines) and the conventional switching-gate CP(dashed lines).
tracks the output voltage and dynamically controls the gate voltage of P1 & N1 to make charging and discharging current constant in almost the entire voltage range between V\textsubscript{DD} and GND. The current mismatch is less than 2% in the voltage range from 0.05V to 0.55V.

In the PFD, a reset impulse of 0.5 nS width is designed to eliminate the dead-zone. During this phase, the charging and discharging currents must always be identical to avoid reference spurs. Fig.4 shows the simulated charging and discharging current during the reset impulse of the proposed CP. It is shown that the current curves almost coincide during the entire reset impulse.

**3. Measurement results**

Fig.5 shows the micrograph of the proposed CP, which is part of a low voltage frequency synthesizer for BLE application in TSMC 28nm CMOS process. The reference frequency is 24MHz and the active area is 320μm×280μm including all of the decoupling capacitors. Fig.6 shows the output spectrum of the frequency synthesizer. Thanks to the precise current matching, the reference spur of the frequency synthesizer is -59.4dBc as indicated in the spectrum.

**6. Conclusion**

This letter presents a low voltage high-output-swing gate-switching CP with the current self-matching technique. To extend the output swing range under low supply voltage, a master-slave rail-to-rail operational trans-conductance amplifier (OTA) is employed to form the negative feedback loop. A prototype of the proposed CP is designed and fabricated in TSMC 28nm CMOS process under a 0.6V supply voltage. Charging and discharging currents are designed to be identical during the entire reset impulse. The measured reference spur is less than -59.4 dBc.

**Acknowledgments**

This work was supported in part by the National Natural Science Foundation of China under Grant 61376075 and Grant 41412020201 and in part by the Key Research and Development Program of Jiangsu Province under Grant BE2015153.

**References**

[1] Zhai, Bo , et al. “Theoretical and practical limits of dynamic voltage scaling.” Proceedings. 41st Design Automation Conference, (2004) 1. (DOI: 10.1145/996566.996798).

[2] H. Kaul et al., “A 320 mV 56 μW 411 GOPS/Watt Ultra-Low Voltage Motion Estimation Accelerator in 65 nm CMOS,” IEEE J. Solid-State Circuits, 44 (2009)107.(DOI:10.1109/JSSC.2008.2007164).

[3] R. G. Dreslinski, M.Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, “Near-threshold computing: Reclaiming Moore’s low through energy efficient integrated circuits,” Proc. IEEE, (2010) 253. (DOI:10.1109/JPROC.2009.2034764).

[4] H.-H. Hsieh, C.-T. Lu, and L.-H. Lu, “A 0.5-V 1.9-GHz low-power phase locked loop in 0.18-μm CMOS,” Proc. IEEE, (2010) 164. (DOI:10.1109/VLSIC.2007.4342999).

[5] T.-S. Chao, Y.-L. Lu, W.-B. Yang, and K.-H. Cheng, “Designing ultra low voltage PLL using a bulk-driven technique,” Proc. IEEE, (2009) 388. (DOI: 10.1109/ESSCIRC.2009.5325983).

[6] A. Yu and P. Kinget, “A 0.65-V 2.5-GHz fractional-N synthesizer with two-point 2-Mb/s GFSK data modulation,” IEEE J. Solid-State Circuits, 44 (2009) 2411 (DOI: 10.1109/JSSC.2009.2023156).
[7] W.-H. Chen, W.-F. Loke, and B. Jung, “A 0.5-V, 440-μW frequency synthesizer for implantable medical devices,” IEEE J. Solid-State Circuits, 47 (2012) 1896 (DOI: 10.1109/JSSC.2012.2196315).

[8] B. Xiang, et al.: “A 0.5V-to-0.9V 0.2GHz-to-5GHz Ultra-Low-Power Digitally-Assisted Analog Ring PLL with Less Than 200ns Lock Time in 22nm FinFET CMOS Technology,” IEEE Custom Integrated Circuits Conference (CICC) (2020) 1 (DOI: 10.1109/CICC484029.2020.9075897).

[9] A. Shirane, et al.: “A low voltage 0.8V RF receiver in 28nm CMOS for 5GHz WLAN,” 43rd IEEE European Solid-State Circuits Conference (ESSCIRC) (2017) 328 (DOI: 10.1109/ESSCIRC.2017.8094592).

[10] N. Joram, et al.: “High swing PLL charge pump with current mismatch reduction,” Electronics Letters, 50 (2014) 661 (DOI: 10.1049/el.2014.0804).

[11] R. R. Manikandan and B. Amrutur: “A zero charge-pump mismatch current tracking loop for reference spur reduction in PLLs,” Microelectronics J. 46 (2015) 422 (DOI: 10.1016/j.mejo.2015.03.004).

[12] P. Qin, et al.: “A fast and efficient automatic frequency calibration technique for 10 GHz PLLs,” IEICE Electron. Express 11 (2014) 20140845 (DOI: 10.1587/elex.11.20140845).

[13] Z. Zhang, et al.: “Source-switched charge pump with reverse leakage compensation technique for spur reduction of wideband PLL,” Electronics Letters 52 (2016) 1211 (DOI: 10.1049/el.2016.1036).

[14] M. Jalalifar and G. Byun: “Near-threshold current charge pump circuit using dual feedback loop,” Electronics Letters 49 (2013) 1436 (DOI: 10.1049/el.2013.1304).

[15] A. Paidimarri, et al.: “A 0.68V 0.68mW 2.4GHz PLL for ultra-low power RF systems,” IEEE Radio Frequency Integrated Circuits Symposium (RFIC) (2015) 397 (DOI: 10.1109/RFIC.2015.7337789).

[16] Xi, Na.: “A low reference spur phase-locked loop realized with dynamic current injection charge pump,” IEICE Electronics Express (2019). (DOI: 10.1587/exel.16.20190095).

[17] D. Mandal, et al.: “Prediction of reference spur in frequency synthesizers,” IET Circuits Dev. Syst. 9 (2015) 131 (DOI: 10.1049/iet-cds.2014.0019).

[18] S.-W. Hsiao, et al.: “Phase-locked loop design with SPO detection and charge pump trimming for reference spur suppression,” IEEE 32nd VLSI Test Sy.

[19] D. Biswas and T. K. Bhattacharyya: “Charge pump with reduced current mismatch for reference spur minimization in PLLs,” Analog Integr. Circuits Signal Process. 95 (2018) 209 (DOI: 10.1007/s10470-018-1163-z).

[20] M. M. Elsayed, et al.: “A spur-frequency-boosting PLL with a ~74 dBc reference-spur suppression in 90 nm digital CMOS,” IEEE J. Solid-State Circuits 48 (2013) 2104 (DOI: 10.1109/JSSC.2013.2266865).

[21] D. Park, et al.: “A 14.2 mW 2.55-to-5 GHz cascaded PLL with reference injection and 800 MHz delta-sigma modulator in 0.13-μm CMOS,” IEEE J. Solid-State Circuits 47 (2012) 2989 (DOI: 10.1109/JSSC.2012.2217856).

[22] D. Zhong, et al.: “A perfectly current matched charge pump with wide dynamic range for ultra-low voltage applications,” IEICE Electron. Express 11 (2014) 20140993 (DOI: 10.1587/elex.11.20140993).

[23] C. Hangmann, et al.: “Stability analysis of a charge pump phase-locked loop using autonomous difference equations,” IEEE Trans. Circuits Syst. I, Reg. Papers 61 (2014) 2569 (DOI: 10.1109/TCSI.2014.2333331).

[24] J. Choi, et al.: “A spur suppression technique using an edge interpolator for a charge-pump PLL,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 20 (2012) 969 (DOI: 10.1109/TVLSI.2011.2129602).

[25] Y. W. Chen, et al.: “A 0.18-μm CMOS dual-band frequency synthesizer with spur reduction calibration,” IEEE Microw. Wireless Compon. Lett. 23 (2013) 551 (DOI: 10.1109/LMWC.2013.2279113).

[26] P. Agarwal, et al.: “Zero-power feed-forward spur cancelation for supply-regulated CMOS ring PLLs,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 26 (2018) 653 (DOI: 10.1109/TVLSI.2017.2788882).

[27] A. M. K. Kuppalath and B. J. Kailath: “Nonlinear PFD free of glitches and blind zone for a fast locking PLL with reduced reference spur,” IEICE Electron. Express 13 (2016) 20160328 (DOI: 10.1587/elex.13.20160328).

[28] Y. Lee, et al.: “A low-jitter and low-reference-spur ring-VCO based switched-loop filter PLL using a fast phase-error correction technique,” IEEE J. Solid-State Circuits 53 (2018) 1192 (DOI: 10.1109/JSSC.2017.2768411).

[29] K. Cheng, et al.: “A 0.5-V 0.4–2.24-GHz Inductor less Phase-Locked Loop in a System-on-Chip,” IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I) 58 (2011) 849 (DOI: 10.1109/TCSI.2010.2089559).

[30] J. Moon, et al.: “A 0.4-V, 90–350-MHz PLL With an Active Loop-Filter Charge Pump,” IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II) 61 (2014) 319 (DOI: 10.1109/TCSI.2014.2312800).