Demonstration of Superconducting Optoelectronic Single-Photon Synapses

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Abstract

Superconducting optoelectronic hardware is being explored as a path towards artificial spiking neural networks with unprecedented scales of complexity and computational ability. Such hardware combines integrated-photonic components for few-photon, light-speed communication with superconducting circuits for fast, energy-efficient computation. Monolithic integration of superconducting and photonic devices is necessary for the scaling of this technology. In the present work, superconducting-nanowire single-photon detectors are monolithically integrated with Josephson junctions for the first time, enabling the realization of superconducting optoelectronic synapses. We present circuits that perform analog weighting and temporal leaky integration of single-photon presynaptic signals. Synaptic weighting is implemented in the electronic domain so that binary, single-photon communication can be maintained. Records of recent synaptic activity are locally stored as current in superconducting loops. Dendritic and neuronal nonlinearities are implemented with a second stage of Josephson circuitry. The hardware presents great design flexibility, with demonstrated synaptic time constants spanning four orders of magnitude (hundreds of nanoseconds to milliseconds). The synapses are responsive to presynaptic spike rates exceeding 10 MHz and consume approximately 33 aJ of dynamic power per synapse event before accounting for cooling. In addition to neuromorphic hardware, these circuits introduce new avenues towards realizing large-scale single-photon-detector arrays for diverse imaging, sensing, and quantum communication applications.

1 Introduction

Developing the next generation of artificial intelligence is an interdisciplinary endeavor, building upon advancements in computer science, neuroscience, and hardware. Two general lessons have emerged simultaneously from both engineering pursuits and naturalistic inquiry: (1) a neural system’s performance typically improves with increasing number and connectivity of processing primitives, both in biology [1, 2, 3] and artificial intelligence [4, 5]; and (2) analog processing with spiking communication in systems exhibiting complex temporal dynamics is both physically efficient and computationally powerful, again in the biological [6, 7, 3] or artificial domain [8, 9]. The circuits presented in this work are designed to embrace both of these ideas by implementing synapses that receive single-photon communication events and perform analog computation with superconducting electronics.

Spiking neural networks inspired by biological systems are particularly intriguing for their exploitation of the temporal domain and suitability for efficient implementation in analog hardware. With recent advances in training algorithms [10, 11, 12], spiking networks are increasingly competitive with conventional neural networks and have been argued to be optimal in at least some respects [13, 14]. Implementing sophisticated spike-based process-
ing in large, highly interconnected networks desired for the highest-performance applications remains daunting for current hardware. While biological neurons are capable of directly fanning out to tens of thousands of synapses, present-day electronic systems struggle with physical fan-out greater than a few and typically resort to digital multiplexing [15]. Multiplexed communication systems inevitably introduce trade-offs between network size and latency. Direct connections between neurons are therefore desirable but require novel hardware. Our proposed solution is to avoid multiplexed communication through the use of integrated optical receivers and transmitters, which do not suffer from charge-based parasitics and can achieve dedicated connections from each neuron to thousands of synaptic recipients. Dense photonic waveguide networks [16, 17] enable high fan-out neurons with light-speed communication. We have argued elsewhere that superconducting hardware is uniquely promising for realizing large-scale spiking neural networks with sophisticated processing units [18, 19, 20]. Superconducting single-photon detectors (SPDs) enable the optical communication of synaptic events at the physical limit of energy efficiency, while the speed, nonlinearity, and low power of Josephson junctions (JJs) make them highly attractive for implementing neural behavior, as recognized by many authors for decades [21, 22, 23, 24, 25, 26, 27, 28].

SPDs and JJs are combined in this study to realize the first superconducting optoelectronic synapses for large-scale neuromorphic hardware. The synapses are demonstrated to detect single-photon events and implement analog signal weighting in the electronic domain. In addition to these minimum synaptic-processing requirements, the synapses perform leaky integration of events over time, and the non-dissipative nature of superconductivity allows leak rates to be chosen over a wide range of timescales (hundreds of nanoseconds to milliseconds are demonstrated here). This capability is promising for leveraging temporal dynamics over many orders of magnitude in complex, adaptive networks. Synaptic circuits are also shown to inductively couple to neuronal and dendritic circuit blocks for further non-linear processing in a manner that has been shown theoretically to enable high fan-in [29]. Taken together and recognizing the synapse as the fundamental computational element of neural systems [30], these results are a major advancement towards the development of large-scale superconducting optoelectronic networks. To our knowledge, the present work is the first demonstration of monolithic integration of superconducting nanowire single photon detectors with JJs, which will also find application in a variety of other scientific and technological fields.

2 The Synaptic Circuit

The basic synaptic circuit is shown in Fig. 1(a) and is discussed in detail in Refs. 18, 31, and 32. Example behavior shown in Figs. 1(b)-(j) was calculated with the circuit model described in Appendix A. The circuit comprises an SPD receiver at the left and a signal integrator at the right. We refer to the integrator as the synaptic integration (SI) loop. Each time the SPD detects one or more photons, current \( I_{sy} \) is added to the SI loop, and the amount of current added is independent of the number of photons detected, yielding binary photonic communication. This current is added in discrete increments called fluxons [33, 34] by the JJ circuit. In the quiescent state, the bias \( I_{sy} \) is chosen so that the current flowing through the first junction \( J_1 \) is below that junction’s critical current, \( I_c \), and the junction provides a superconducting path to ground. Upon detection of a photon, the SPD transitions to a resistive state and diverts current \( I_{spd} \) into \( J_1 \). When \( I_{sy} + I_{spd} \) exceeds \( I_c \), \( J_1 \) will produce a train of fluxons that propagates through a Josephson transmission line and accumulates in the SI loop. The synapse makes use of passive reset, as supercurrent will return to the SPD with a time constant set by \( L_{spd}/r_{spd} \approx 40 \text{ ns} \). The number of fluxons added to the SI loop per photon-detection event depends on the duration of time \( J_1 \) is driven above \( I_c \). This behavior is illustrated in Fig. 1(b), where \( I_{sy} + I_{spd} \) is plotted for two different values of \( I_{sy} \). The dashed horizontal line in Fig. 1(b) represents the junction \( I_c \). Fluxons are produced for as long as \( I_{sy} + I_{spd} \) remains above \( I_c \). For the low value of \( I_{sy} \), the combined currents exceed \( I_c \) only briefly, while the high value drives \( J_1 \) above \( I_c \) for nearly the entire duration of the SPD pulse. Additionally, the rate of fluxon production increases with the current flowing through the junction. Example fluxon trains for the two synaptic weights are shown in Fig. 1(c) and Fig. 1(d), and their corresponding contributions of current to the SI loop are illustrated in Fig. 1(e) and Fig. 1(f). Only a brief subsection of the fluxon train is shown in the high weight case. The difference in fluxon rates is evident, as seven fluxons are produced within 3 ns by the weak synaptic weight, while only 200 ps is required to produce seven fluxons for the high synaptic weight. The total number of fluxons added to the SI loop in the case of the synapse event with high synaptic weight is 1346.

The role of fluxon trains has a direct analogy with biological synapses, where the strength of synaptic connections is determined by the number of synaptic vesicles containing neurotransmitters that are passed across the synaptic cleft. In our synapses, the strength of synaptic connections is determined by the number of fluxons passed into the SI loop. As with biology, this low-level, discrete picture can often be disregarded in favor of a simpler, essentially analog description of high level synaptic operation.

Figures 1(g)-(j) concern the integration of multiple photon-detection events in the SI loop. Figure 1(g) shows presynaptic spike trains of photon-detection events at two different frequencies. Each photon-detection event adds current to the SI loop, and the integrated current in the SI loop decays with a time constant set by \( \tau_{si} = L_{si}/r_{si} \). We
Figure 1: Synapse concept. Refer to Appendix A for details of the circuit model. (a) Synaptic circuit diagram showing four main circuit blocks. (b) Simulation of the current flowing into $J_1$ upon detection of a photon for two different values of $I_{sy}$. A train of fluxons is produced for as long as these traces exceeds the critical current $I_c$ of the junction. (c)-(f) Fluxon trains for the two synaptic weights and their corresponding additions to the SI loop. The high synaptic weight case, (d) and (f), only shows a brief fraction of the pulse train. (g) SPD response to a train of single-photon pulses at different frequencies. (h) SI current in response to the two photonic pulse trains shown in (g). The higher frequency input pulse train results in a higher current in the integration loop. (i) The peak value of SI current (normalized by the JJ critical current) as function of the number of pulses in a pulse train, demonstrating the emergence of steady-state behavior and synaptic weighting capability. (j) The maximum SI current as a function of the frequency of a pulse train, illustrating the saturating behavior of the SI loop. (i) and (j) use time-accelerated SPDs to reduce numerical simulation time.

will show that the passive elements $L_{si}$ and $r_{si}$ can be engineered over many orders of magnitude. In this way, the SI loop exhibits leaky-integrator behavior desired of spiking neural computational primitives, shown in Fig. 1(h). In Figs. 1(g)-(j) $\tau_{si}$ is 250 ns, and for these figures the model used an accelerated-time synapse with 5 ns SPD recovery to facilitate numerical efficiency. The slower of the two input photonic pulse trains displayed in Fig. 1(g) is 4 MHz ($1/\tau_{si}$), while the faster input train is at twice this frequency. Figure 1(h) shows that the higher-frequency series of 10 pulses results in appreciably larger integrated signal, a feature that will be prominent in the measured data shown in Sec. 4. The magnitude of current stored in the SI loop is thus a record of recent synaptic activity that can be used in subsequent computations, including in local weight update circuits.
The synapse as a whole can be modeled with a leaky integrator equation of the form

$$\frac{dI_{si}}{dt} = I_{iq} R_{iq}(t) - \frac{I_{si}}{\tau_{si}},$$

(1)

where $I_{iq} = \Phi_0 / L_{sq}$ is the current of a single flux quantum entering the integration loop, and $R_{iq}(t)$ is the rate of flux-quantum production. At a fixed frequency of input photonic pulses, current will accumulate in the SI loop. Yet during each inter-spike interval some of this signal will decay exponentially with time constant $\tau_{si}$. A quasi-steady state is reached when the signal added with each photonic pulse counters the signal decay between pulses. Here, we use “quasi-steady state” to refer to the circumstance where the time-averaged signal between evenly spaced incident photon pulses is constant from one photon pulse to the next. In this case, the time average of $dI_{si}/dt = 0$, and Eq. 1 informs us that $I_{si} = \tau_{si} I_{iq} R_{iq}$, with $I_{si}$ and $R_{iq}$ indicating time averages. The time-averaged rate at which fluxons are produced depends on the synaptic weight, the rate at which photons are incident, and the value of $I_{si}$. The emergence of steady state behavior is illustrated in Fig. 1(i) and its frequency and synaptic weight dependence is illustrated in the transfer function of Fig. 1(j). This behavior is experimentally validated in Sec. 4.

The SI loop is also inductively coupled to a superconducting quantum interference device (SQUID) to implement non-linear transfer functions and transduce $I_{si}$ into a measurable voltage. We refer to this SQUID as the dendritic receiving (DR) loop. The DR transfer function in the present study results in a roughly sigmoidal response. We now discuss the fabrication process before presenting measured data.

3 Fabrication

A 14-layer fabrication process was developed for this demonstration and supports Nb/aSi/Nb JJs [35] externally shunted with PdAu resistors and MoSi SPDs [36, 37]. The high kinetic inductance of the MoSi thin film was also leveraged in conjunction with Au resistors to realize the leaky integrating loops. Electron-beam lithography was used for the SPD step, while all other patterning was accomplished with photolithography using a 365 nm i-line stepper. A complete process flow can be found in Appendix B. In brief, the MoSi SPD/high-kinetic-inductance layer is deposited and patterned on a pristine oxidized-silicon surface. Contact is made from this layer to Nb. The SPD layer is separated from the JJ layers by an SiO$_2$ insulator and an Nb ground plane. Contact is made from the SPDs to the JJs with etched and backfilled vias. An additional Nb wiring layer is included above the JJs to enable the transformers that couple synapses to SQUIDs. The PdAu and Au resistor layers are patterned last.

A synapse layout and microscope images of key components are shown in Fig. 2. Five synapse designs were fabricated with different synaptic time constants and storage capacities. Synapse areas range from 0.32 mm$^2$-0.52 mm$^2$ excluding wiring pads, although no effort was made to make the circuits compact in this work. In a mature process, various device layers will be placed atop one another with planarization performed between. Previous analysis found similar synapses will fit in 30 µm × 30 µm [20]. The results presented here are from the first wafer run with this process. The immediate yield is suggestive that the process will be robust.

4 Experimental Characterization

Measurements were performed between 800 mK and 900 mK in a closed-cycle sorption pump 4He cryostat. Due to wiring limitations, each synapse was measured during a separate cool-down. A fiber-coupled, 780 nm pulsed laser source was used to flood illuminate the chip and serve as the presynaptic input. The laser pulse width was approximately 480 ps. This is much shorter than the SPD recovery time, so multiple detection events per pulse are unlikely, as supported by synapse count rate measurements shown in Appendix D. Although each optical pulse contains multiple photons to guarantee detection for each presynaptic event in this free-space configuration, we confirmed the synapses’ ability to detect single photons with a linearity measurement under very low light-levels (Appendix D). The detector response is also independent of photon number [38], so the fact that more than one photon was used as synaptic input for these measurements is ultimately how the detectors are intended to behave in a network context, and identical dynamics should be expected for few-photon pulses in future waveguide-integrated circuits. As we have argued elsewhere, it may be advantageous for presynaptic spikes to arrive with an average of seven photons to ensure 99% successful communication despite unavoidable Poisson variability [19, 20].

The voltage across the DR loop, $V_{eq}$, [Fig. 1(a)] is on the order of 10 µV and is read out with a room-temperature amplifier. Two different amplifiers (40 dB and 60 dB voltage gain) were used to accommodate the wide range of
timescales under investigation. Averaging was required on most traces to counteract low-frequency line noise disturbing the microvolt signals. An unaveraged trace is shown in Appendix F. All biases were generated outside the cryostat and were tuned individually for each synapse to maximize signal amplitude and account for device variation. Refer to Fig. 8 in Appendix C for an exhaustive list of experimental parameters used in the presented data.

Figure 3 presents the characterization of a single synapse designed with a time constant of 6.25 µs and inductance of 2.5 µH. Measurements suggest actual values of 8 µs and 3.2 µH. The cause of the increased inductance is described in Appendix B. Synaptic weighting is shown in Fig. 3(a), where the response to a single optical pulse is plotted for different values of $I_{sy}$. The DR response was tuned to be approximately linear over this relatively small signal range, allowing the current in the SI loop, $I_{si}$, to be estimated from $V_{sq}$ (Appendix E). The inset to Fig. 3(a) compares the measured data with the circuit model of Appendix A and shows that the weighting function measured experimentally agrees with the prediction of our theoretical model. $I_{sy}$ is shown to modulate the height of $V_{sq}$ in response to a single optical pulse by at least a factor of 28, and the ability to resolve small weights was limited by noise.

Figure 3(b) shows the integrating capability of the synapse in response to a pulse train of fixed frequency and pulse number for five values of synaptic weight. For sufficiently long pulse trains, the synapse reaches a steady state that can be tuned with $I_{sy}$, and depends also on the frequency of the input pulse train. We refer to such operation as the “rate-coding” domain. Figure 3(c) demonstrates an activity level that is better regarded as the “burst-coding” domain [39]. Here, the synaptic weight is fixed and the different traces correspond to different numbers of pulses as the steady-state is approached. Figure 3(d) shows the synaptic response to 10 pulses at three different frequencies, analogous to the theoretical traces of Fig. 1(h). Figures 3(e) and 3(f) summarize these behaviors by plotting the maximum value of $V_{sq}$ as a function of photonic pulse number and frequency respectively for several values of synaptic weight in a manner analogous to the theoretical traces of Fig. 1(i) and (j). Figure 3(e) shows the transition from the burst-coding regime for low numbers of pulses to the rate coding regime where $I_{si}$ reaches a steady-state level. Figure 3(f) displays the desired roll-over behavior with pulse frequency discussed in Sec. 2. Both figures also demonstrate the ability of $I_{sy}$ to tune synaptic response over a wide range. Sigmoidal fits for these plots are presented in Appendix F. While the pulse number and frequency transfer functions capture the essential analog computation for the burst- and rate-coding domains, these synapses could be used with spike timing as well [32] and make use of the extremely low jitter (picoseconds) of superconducting nanowire detectors [40].

The synaptic transfer functions can be engineered over
Figure 3: Detailed characterization of 6.25 µs, 2.5 µH synapse. (a) Response of $I_{si}$ to a single optical pulse for different values of $I_{sy}$. Inset shows comparison to the model of Appendix A. (1000 averages.) (b) Response to an 800 kHz train of 20 pulses for different synaptic weights. (c) Response at fixed $I_{sy}$ to 400 kHz pulse trains containing different numbers of pulses. (d) Response at fixed $I_{sy}$ to pulse trains at three different frequencies. Compare to Fig. 1(h). (e) Transfer function versus number of pulses in pulse train at different synaptic weights and fixed frequency (1 MHz). Compare to Fig. 1(i). (f) Transfer function versus pulse train frequency at different synaptic weights for 100 pulses. Compare to Fig. 1(j).

A wide range of timescales, as illustrated in Fig. 4. Figure 4(a) shows the temporal response of synapses with four different time constants to a single photonic pulse. Moderate synaptic weights were chosen for each synapse. We see that the temporal dynamics range from the submicrosecond to several milliseconds. Dotted lines show exponential fits on the semi-logarithmic plot. Figures 4(b) and (c) show integrating behavior for the fastest (271 ns) and slowest (5.83 ms) time constant synapses respectively, demonstrating no degradation in the leaky-integrating behavior at either extreme. Figures 4(d)-(f) show the frequency response functions for those same two synapses as
Figure 4: Comparison of synapses with varying time constants. (a) Response to a single optical pulse at moderate synaptic weight for synapses with four different designed time constants (250 ns, 1.25 µs, 6.25 µs, and 5 ms). Dotted lines show exponential fits with extracted time constants. (b) 250 ns synapse response to seven optical pulses at three different megahertz-range frequencies. (c) 5 ms synapse response to seven optical pulses at three different sub-kilohertz frequencies. (d)-(f) Frequency transfer function at varying synaptic weights and fixed number of pulses (100, 100, and 10 respectively). Parts (d)-(f) are labeled with the designed time constants, and those measured are given in parentheses.

well as one with an intermediate time constant designed to be 6.25 µs and measured to be 8.06 µs. We once again see similar behavior across the timescales and observe that the onset of integration can be tuned from 100 Hz to almost 10 MHz. Figure 4 also illustrates the interplay between parameters fixed in hardware ($L_{si}$ and $r_{si}$) and those that can be reconfigured dynamically ($I_{sy}$).

The vast parameter space (pulse frequency, pulse number, $I_{sy}$, $\tau_{si}$, and $L_{si}$) exhibited by these synapses is promising for fostering complex dynamics in large-scale networks. Figure 5 captures the synaptic response across a large range of this space. The temporal traces of Figures 3 and 4 are once again reduced to single data points corresponding to the maximum change in voltage recorded for each trace, as in the transfer functions. For fixed $I_{sy}$, these values of $V_{sq}$ are plotted as 2D heat maps with the
Figure 5: Heat maps of synaptic response. (a) Sample map at fixed synaptic weight showing frequency and number axes (fixed for all plots in this figure). (b) Color bars showing the change in $V_{sq}$, normalized for each synapse. (c) Grid showing the evolution of synaptic response with $I_{sy}$ (increasing vertically) for five different synapses.

graph frequency of a pulse train along the $x$-axis and the number of pulses in a train along the $y$-axis [Fig. 5(a)]. Both $x$ and $y$ axes are spaced with a geometric progression. This data is presented for six different values of $I_{sy}$ (rows) and five different synapses (columns) in Fig. 5(c), and the color bars in Fig. 5(b) give the scale for each column. Due to the use of different amplifiers and different bias conditions on synapses measured on different cool downs, the variation in color axis was unavoidable. Synapses are labeled by their designed time constant and SI loop inductance. Comparisons between different synapses (columns) should be taken somewhat qualitatively given fabrication and biasing variations. Nonetheless, we can clearly see great diversity in behavior, and several notable trends can be observed. The turn-on frequency increases inversely with $\tau_{si}$, as expected for an $LR$ filter. Both the frequency and number responses can be broadly adjusted with synaptic weight. The 250 ns synapse responds far more strongly to frequencies greater than 1 MHz, and this is striking in comparison to the microsecond synapses that successfully integrate at much lower frequencies.

The third and fourth columns show two synapses with the same designed time constant, but two different values of $L_{si}$. $L_{si}$ sets the amount of current added to the SI loop per fluxon. This is a different weighting mechanism than $I_{sy}$, which sets the number of fluxons added per photon detection. Larger $L_{si}$ corresponds to less current added to the loop per fluxon, so the apparently slower turn on of the 2.5 $\mu$H synapse with $I_{sy}$ is expected. However, we caution that some of this discrepancy may be from different biasing conditions including a reduced SPD bias on the 2.5 $\mu$H synapse to account for a lower SPD $I_c$. Investigating the effect of different values of $L_{si}$ is intriguing because it sets the ultimate number of events that can be stored by the
SI loop, but full analysis requires further study.

The millisecond synapse in the far right column is a curious case, as it is independent of frequency over this measured range (100 kHz - 10 MHz). The current in the SI loop does not have time to decay between pulses, making this synapse essentially a photon-counting device over this range. This slow-leak behavior is illustrated in Fig. 6, where the millisecond synapse is shown responding to pulse trains of 500 kHz, 1 MHz, and 1.5 MHz. Each pulse train is identical in length (15 events). We see that the final magnitude of $V_{eq}$ is independent of frequency, but is instead determined only by $I_{sy}$ and the number of pulses in the train. We anticipate this regime to be useful in long-term plasticity mechanisms for modulating the behavior of faster synapses, as well as for applications in SPD imaging arrays.

5 Discussion

Through monolithic integration of SPDs with JJs we have demonstrated tunable single-photon optoelectronic synapses with numerous temporal filtering properties of utility for spiking neural systems. The presented synapses are responsive to presynaptic spiking events encoded as single-photon signals, positioning them for use in large-scale networks that embrace direct optical connections between neurons. Unlike electrical communication, optical signals are immune to the parasitics that pose challenges for electronic fan-out. Direct communication is superior to multiplexed systems for large, highly interconnected networks, as latency is essentially decoupled from network complexity. Latency in this system is limited only by the time it takes light to travel between nodes.

These synapses are not mere variable attenuators as many hardware synapse implementations, but also perform temporal integration and other analog computational primitives observed in biology. A system with integrating synapses (and dendrites) is vastly more dynamic than one in which only the neurons perform integration. The synapses presented here thus make full use of the temporal advantages of spiking networks. The great diversity in demonstrated decay times (hundreds of nanoseconds to several milliseconds) is another advantage of this hardware. We can now imagine networks that are matched to applications of a wide range of different timescales—from accelerated simulations and precise control systems to interactions with humans. The millisecond synapse achieves a biologically relevant timescale, which has been a major area of research in analog CMOS implementations [41, 42]. Mixing synapses with different time constants in the same network may also be advantageous, as networks with time constants spanning orders of magnitude may be more apt to develop temporal dynamics with power-law statistics—the signature of critical behavior that has been studied for its important role in cognition [43, 44, 45]. Integrating behavior is also useful for plasticity mechanisms that rely on the recent history of synaptic activity to update weights, such as spike-timing-dependent plasticity [46, 47]. We envision local plasticity circuits coupled to the SI loop at every synapse. Many of these plasticity (or homeostatic) mechanisms will also be desired to operate at timescales significantly longer than that of the synapses themselves, which this data suggests is imminently feasible.

This study represents the first demonstration of superconducting optoelectronic synapses, and ample room for improvement remains. The temperature of operation is a prime candidate. The current fabrication process should be commensurate with operating temperatures up to 2.7 K, but other SPD materials (likely NbTiN) may prove better suited for operation at 4 K where liquid helium immersion cooling can be utilized. This would not only improve energy efficiency, but would also significantly simplify the measurement apparatus and remove compressor noise. Energy efficiency of the devices themselves also stands to be improved. The main source of energy consumption here is through the discharging of the detector inductance. Free space operation necessitated relatively large detector areas, and thereby large inductance ($\approx 825$ nH). This energy ($\frac{1}{2}L^2I^2$) corresponds to 33 aJ per event (33 fJ if a factor of one thousand is included for cooling overhead). A low-inductance waveguide-integrated synapse would improve this metric by an order of magnitude [16]. Optical communication is still likely to dominate power consumption even in this case, so thousands of fluxons can be produced per synaptic operation before computational power begins to dominate over communication. Another major deficiency is the use of an external bias to provide the synaptic weight. A local memory would be superior. One possibility is to store the weight as persistent current in another superconducting loop that is inductively coupled to the $I_{sy}$ bias line [18]. Such memory should be achievable without any changes to the process flow. Both unsupervised Hebbian-based learning [12, 48] and recently developed supervised algorithms for local gradient descent [11, 49] could be implemented with local analog plasticity circuits that adjust the current stored in such memory loops. In the near term, the synapses could be interfaced with bias-generator circuits for either hardware-in-the-loop training or for implementing a fixed network in inference tasks. Further work remains to combine these synapses with light-emitting neuron circuits. Significant progress in cryogenic integrated light sources [50, 51] and superconducting optical transmitter circuits [52] has occurred, indicating that full superconducting optoelectronic neurons may not be far in the future.

While this platform was designed for high-performance neuromorphic computing, there are many other application areas that stand to benefit from this first demonstration of monolithic SPD-JJ integration. The exact synaptic circuits we have presented can be used as single-photon integrating pixels for advanced imaging applications. Large-scale SPD arrays have thus far been limited by readout technologies, but the integrating character of these circuits...
allows photon-detection events to be stored and read out at later convenience. The demonstrated millisecond retention times are particularly amenable to large arrays. Single-photon to single-fluxon transduction with long integration times should be feasible, enabling accurate photon counting similar to Ref. 53. The fabrication process should also be applicable to Josephson circuits incorporating single-flux-quantum logic, presenting the possibility of digital processing of single photon events [54, 55] for applications including qubit control or post-processing of images acquired with SPD arrays. Thus, we expect the monolithic SPD-JJ integration to offer new opportunities in fields as diverse as quantum information and communication, biomedical imaging, and broad-spectrum astronomical observations [56], potentially engendering an entirely new field of integrated superconducting optoelectronic hardware.

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\[ \frac{d^2 \delta}{d\tau^2} = \frac{1}{\beta}\left(i - \sin \delta - \frac{d\delta}{d\tau}\right). \] (3)

There are three JJs in the circuit, each obeying the second-order Eq. 3, and two additional first-order equations from Eqs. 2. This system can be represented as eight coupled first-order ODEs which we solve with the Scipy function `solve_ivp`. The other currents in the circuit can be obtained from
\[ i_1 = \frac{1}{\beta_{L,11}} (\delta_2 - \delta_1) + i_{sy} + i_{s2}, \]
\[ i_3 = \frac{1}{\beta_{L,12}} (\delta_2 - \delta_3) - i_{si} + i_{sc}, \]
\[ i_2 = i_{sy} + i_{j1} + i_{sc} + i_{s2} - i_1 - i_3 - i_{si}. \] (4)

**B Fabrication Details**

The fabrication of the SPD-JJ synaptic circuits combines previously developed SPD and JJ fabrication processes. The MoSi SPDs have been described in Refs. 36, 37, and the Nb JJs have been described in Refs. 58, 35. The process began with a thermally oxidized silicon wafer. Thin Nb contacts (45 nm) were deposited via sputtering, and a liftoff process was employed to realize a very shallow sidewall angle. This defined the first metal layer, M1. Next MoSi was sputtered to a thickness of 5 nm and capped with a 2 nm amorphous silicon layer. This defined the superconducting thin film layer, STF. The Nb liftoff process was used for M1 so the thin MoSi layer could make superconducting contact. In a mature fabrication it will be desirable to deposit Nb wires with a damascene process followed by chemical-mechanical planarization. The MoSi would be deposited on the planarized surface and would make contact to the planarized Nb. In the present work we avoided this planarization step as it is non-trivial in the NIST cleanroom. We have performed experiments with MoSi deposited on planarized oxidized wafers with less than 0.5 nm root-mean-square roughness and measured less than 0.2 K change in the film critical temperature as compared to a film deposited on a thermally oxidized substrate.

The SPDs were defined on the STF layer through ebeam lithography. The wires defining the SPDs were 200 nm wide on the mask with 50% fill factor, resulting in wire widths near 180 nm on the wafer. A 100 kV column and 2 nA beam current were used in patterning. The inductors comprising the SI loops were formed from the same STF superconducting thin film layer, STF. The Nb liftoff process was used for M1 so the thin MoSi layer could make superconducting contact. In a mature fabrication it will be desirable to deposit Nb wires with a damascene process followed by chemical-mechanical planarization. The MoSi would be deposited on the planarized surface and would make contact to the planarized Nb. In the present work we avoided this planarization step as it is non-trivial in the NIST cleanroom. We have performed experiments with MoSi deposited on planarized oxidized wafers with less than 0.5 nm root-mean-square roughness and measured less than 0.2 K change in the film critical temperature as compared to a film deposited on a thermally oxidized substrate.

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Following M1 and STF, the first SiO2 insulator (I1) was deposited using electron cyclotron resonance plasma-enhanced chemical vapor deposition. I1 was 200 nm thick,
as were all insulating layers. The first via layer (V1) was etched through I1, terminating on the Nb contacts formed in M1. V1 was etched with CHF3 chemistry with O2 added to increase the sidewall slope to facilitate via formation without a damascene process. M2 was then deposited by sputtering Nb, and wires were formed with i-line photolithography and dry etching using an inductively coupled plasma with SF6 chemistry. M2 serves as the superconducting ground plane for the circuits. I2 was then deposited using the same process as V1. V2 was opened using the same process as V1.

The JJs were fabricated next using an Nb/a-Si/Nb trilayer. The lower electrode Nb layer (JJ1) made contact with M2 through V2. The a-Si tunneling barrier was approximately 5 nm thick. Self-shunted JJs with Nb doped Si barriers have been previously used in SFQ circuits [35]. However, in this work undoped a-Si barriers and external shunts were used as JJ area was not a concern in these circuits. The target critical current density of the trilayer was 1 kA/cm2, but the resulting value was more than twice as large due to an unidentified change in the process. Subsequent wafers have returned to the previous value. The fact that the synaptic circuits remained highly functional when the critical currents of all JJs on the wafer were more than twice as large as designed is evidence for the robustness of the circuit concepts. The JJ top electrode (JJ2) and tunneling barrier were dry etched with SF6 chemistry, stopping on JJ1 to leave a metal wiring layer. The JJ1 layer was also used as the SQUID washer body, which served as the pickup component of the transformer between the SI and DR loops. I3 was then deposited at 200 nm with the same SiO2 as the other insulators, and V3 was etched to contact the JJ top and bottom electrodes.

Upper Nb metal M3 was then deposited and etched just as M2. This wiring layer was used for superconducting interconnects and to form the input coil for the transformer from the SI loop to the DR loop. M1 was also employed in this transformer to cross under JJ1. All SQUIDs on this wafer leveraged quadrupole designs [Fig. 2(g) and (h)] to avoid sensitivity to stray uniform magnetic fields. Some SQUIDs on a diagnostic chip included resistors coupled to the washer to damp LC resonances. However, for the SQUIDs employed to interface with the synapses, an abundance of caution drove us to omit those resistors to our detriment. LC resonances driven by the room-temperature amplifier had deleterious effects on the SQUID response curves (Appendix E), limiting the dynamic range we were able to for the measurements.

The JJ shunt resistors were formed from PdAu due to that material’s low residual resistivity ratio, while the resistors used in the SI loops to set the leak rate were formed from Au due to its low resistivity. These two layers were deposited in separate liftoff steps. Again, a mature foundry would be able to straightforwardly adapt these steps to a damascene process. A final insulator was deposited just as the others, and large vias were opened to enable wire bonding to the top Au layer.

In addition to the JJ tunneling barrier being thinner than desired leading to higher Isq than designed, one other processing step was sub-optimal. Before depositing I1 over STF, an RF clean was conducted in the deposition chamber. This plasma clean slightly thinned the STF film resulting in suppressed critical temperature and increased inductance. All circuits were designed to operate at 2.7 K, with the MoSi film having a critical temperature above 5.5 K, but this film degradation required operation below 1 K to support the designed SPD Ic values. The increased inductance is likely the cause of the SI loop inductances being larger than design. This issue has since been resolved by depositing a slightly thicker a-Si capping layer on STF.

All data presented in this paper were acquired from the first wafer fabricated with this combined SPD-JJ process.

C Experimental Details

A schematic of the experimental set-up is presented in Fig. 9. Each synapse requires seven coaxial connections for I/O. Four current biases are required by the synaptic block (Ispd, Isy, Ijtl, and Iwc) as shown in Fig. 7. The DR block requires a bias for the SQUID (Idr), an “addflux” bias (Iad) for tuning the operating point of the DR loop, and a line for reading the voltage (Vsq) across the loop. Fabrication variation between synapses required each of the six current biases to be adjusted to maximize signal amplitude. Due to current sharing on the JJs between the biases, there are many possible biasing conditions that behave in a qualitatively similar manner. To maintain consistency, the biases Isy, Ijtl, and Iwc were chosen with similar values when possible. The addflux line was chosen so that Vsq just started to increase with Isi, except for where more linear operation was desired, such as in Figs. 3(a) and 4(a). The biases for every figure in the main text are provided in Fig. 8.

All measurements were performed between 800 mK and 900 mK in a closed-cycle sorption pump 4He cryostat. Two concentric cylindrical mu-metal shields reduce external magnetic noise. An optical fiber was positioned to flood illuminate the entire chip. A function generator triggered the 780 nm laser to produce bursts of pulses of a given number and frequency. Idr was supplied by a commercially available current source, while all other current biases came from resistors in series with isolated voltage sources. Two different amplifiers were used in these experiments to read Vsq. One was a home-built amplifier with 40 dB voltage gain and 1 MHz bandwidth. The other was a commercial amplifier with 60 dB gain and 10 MHz bandwidth. Amplifier bandwidth limitations are visible for the 250 ns synapse [Fig. 4(b)]. Time traces were recorded with a 1 GHz oscilloscope triggered by the function generator.
**Figure 8**: Parameters used for all data shown in the main text.

| Parameter   | Value  |
|-------------|--------|
| $\tau_{g}$  | 6.25 µs |
| $L_{g}$     | 2.5 µH  |
| $I_{sp}$    | 7.2     |
| $V_{g}$     | 87.0 - 91.9 N/A |
| $I_{g}$     | 90      |
| $I_{j}$     | 90      |
| $I_{sc}$    | 486     |
| $I_{af}$    | 510     |
| Pulse Frequency | 800 kHz |
| Pulse Number | 100     |
| Averages    | 1000    |

**Figure 9**: Measurement setup. The voltage sources are used to generate currents through fixed resistors between 100 Ω and 100 kΩ.

**D Characterization of Single-Photon Detectors**

The SPDs are MoSi superconducting-nanowire single-photon detectors [37]. A typical detector response to a photon pulse train is shown in Fig. 10(a) and a zoom-in of a single pulse is shown in Fig. 10(b). The decay time is approximately 37.5 ns. The SNSPD is unresponsive to photons when in the resistive or recovery state, so this response time sets the maximum frequency (tens of MHz) of presynaptic events for this hardware. The inset of Fig. 10(b) shows the IV curve of the detector, demonstrating a critical current of approximately 12 µA. Figure 11 shows count rate as a function of bias current for pulse trains of various frequencies for both the 250 ns synapse (a) and a stand-alone “monitor” SPD (b). Such a monitor SPD was fabricated adjacent to each synapse for diagnostic purposes. The pulse frequency is kept below the onset of integration for the synapse so that individual counts could be well-defined. We observe a large plateau region from 6 µA-12 µA where the photon detection efficiency is largely independent of bias (and bias noise). The synapse
exhibits a large increase in dark counts near $I_c$ likely due to relaxation oscillations between the SPD and the Josephson junctions [59]. Fortunately, this phenomenon only occurs for a small range of biases, and is easily avoidable by biasing elsewhere in the plateau. SPD biases in this work were $9 \mu$A for all synapses except the 6.25 µs, 2.5 µH synapse where 7.2 µA was used to account for a reduced SPD critical current.

The single-photon operation of the detectors and synapses is confirmed in Fig. 12(c). Under very low optical illumination, single photon events are expected to dominate optical inputs, as opposed to multi-photon events wherein more than one photon is absorbed in the detector within the $\approx 200$ ps rise time of the SPD pulse. For optical pulses with $\lambda$ photons per pulse, the probability of detection is proportional to the Poisson probability of a single photon in a pulse, $P(k = 1) = \lambda e^{-\lambda}$. For $\lambda \ll 1$, Taylor expansion shows that the count rate should be proportional to $\lambda$, and therefore to the optical power. Taking the logarithm of both sides implies that the logarithm of count rate versus the logarithm of power should be a line with a slope of positive one. This is confirmed in Fig. 12(c), where linear fits to the logarithm of count rate versus attenuation show slopes very near the expected value of negative one for both the synapse and monitor SPD. If two-photon events were required for detection, the slope would be negative two.

### E Characterization of Josephson Junctions and Superconducting Quantum Interference Devices

Sample JJ IV curves are presented in Fig. 13. The JJs used in the synaptic block all had diameters of 2.59 µm [Fig. 13 (a)], while the JJs used in the DR block had diameters of 4.09 µm [Fig. 13 (b)], corresponding to critical currents of about 95 µA and 263 µA respectively. This varied considerably across the wafer, as evidenced by the range in biases used for the synapses in Fig. 8. The critical current density, $J_c$, of the fab process was measured to be approximately 1.7 kA/cm$^2$.

The response of stand-alone SQUIDs (essentially the DR loop without the synaptic block attached) are shown in Fig. 14 under several measurement conditions. The $x$-axis is the current sent through a wire inductively coupled to the SQUID loop, mimicking the current in the SI loop of a synapse. Figure 14(a), which lacks an amplifier and has a resistive shunt on the SQUID to limit LC resonance effects, shows the results closest to the expected output of an asymmetric SQUID. The synaptic circuits were un-
Figure 12: Count rate dependence on optical power level. 
(a) Count rate for the 250 ns synapse as a function of SPD bias current. (b) Count rate for the monitor SPD as a function of bias. (c) Confirmation of single-photon sensitivity for both the monitor SPD and the synapse.

Figure 13: JJ IV curves. The SI circuit block used 2.59 µm junctions with $I_c \approx 95 \mu A$ (a), while the DR loop used 4.09 µm junctions with $I_c \approx 263 \mu A$ (b).

shifted with a second tuning coil carrying $I_{af}$. This ability was used throughout data collection to maximize signal amplitude by cancelling the effects background flux in the loop. The addflux coil was also essential for estimating the SI current from $V_{sq}$, as shown in the inset of Fig. 3(a). $I_{af}$ was increased from other measurements on this synapse (see entries for the 6.25 µs, 2.5 µH synapse in Fig. 8) to ensure an approximately linear transfer function between $I_{si}$ and $V_{sq}$. The transfer function of a DR Loop coupled to a given synapse was measured by fixing the synaptic bias currents and sweeping the addflux bias. Measurements of the period of the SQUID response provided experimental values for mutual inductance between the DR loop and both the SI loop and the addflux coil. Together, these measurements permit the extraction of the SI current from $V_{sq}$.

Fortunately saddled with the worst scenario [Fig. 14(d)]: no shunt resistor and an amplifier to resolve small signals. We see that a variety of undesirable abrupt features were introduced in this case, which we think are related to noise coupled in by the amplifier driving $LC$ resonances, where the inductance is due to the SQUID washer and input coil of the transformer, and the capacitance is between the washer and the input coil. A synapse-dendrite combination embedded in a neuron would have a response most similar to Fig. 14(a), with the addition of a shunt resistor and without the need for a readout amplifier.

Figure 15 shows how the SQUID response could be
Figure 14: Stand-alone (diagnostic) SQUID response as a function of current in what would be the SI loop. The SQUIDs used in the DR loops for the measured synapses correspond to the case shown in (d), but (a) is the device that will be used in for future systems.

Figure 15: SQUID response at a fixed bias current for different values of $I_{af}$, demonstrating the ability to tune the phase of the SQUID response.
F Additional Data from Synapses

Here we show additional data from various synapses that may be of interest to readers with high stamina. Figure 16 shows a single time trace taken from a synapse wherein no averaging was performed.

Figure 17 shows time traces from the 250 ns synapse with bursts of one through seven photonic pulses incident. The frequency of the input pulse train varies across the columns from 2 MHz to 8 MHz showing how integration begins to occur above the \( L/r \) cutoff frequency. The three rows show the behavior with three different synaptic bias currents applied.

Figure 18 shows data similar to Fig. 17, except for the 6.25 µs, 500 nH synapse. The frequencies have been shifted lower by an order of magnitude to demonstrate the same temporal integration crossover effect.

Figures 19 and 20 investigate the 6.25 µs, 2.5 µH synapse. Figure 19 shows integrating behavior. The three columns show three frequencies while the three rows show different numbers of pulses in the incident photonic pulse train. Within each panel, several values of synaptic weight are shown. As the pulse train is shifted to higher frequency, weaker synaptic weights are sufficient to bring the integrated signal above the noise.

Figure 20 shows the transfer functions measured from this synapse, just as in Fig. 3(e) and (f), but here we have included fits to the data. In Fig. 20(a) fits to a sigmoidal functional form are shown as dotted lines. The sigmoid functional form is given by

\[
V_{sq}(N_{ph}) = (A - A_0) \left[ 1 - \left( e^{(N_{ph} - N_0)/w} + 1 \right)^{-1} \right] + A_0,
\]

where \( A, A_0, N_0 \) and \( w \) have been fit using the Scipy curve_fit function. Figure 20(b) shows the transfer functions versus the frequency of photonic pulses. In this case, the sigmoid form of Eq. 5 provides a reasonable fit of the roll-over section of the curves (dotted lines), while the initial turn-on section is better fit with a linear function.

Figure 16: Example unaveraged time trace from the 250 ns synapse.
| Frequency | Integrate Time | Current (μA) |
|-----------|----------------|-------------|
| 2 MHz     | 250 ns         | 81.89       |
| 4 MHz     | 250 ns         | 82.67       |
| 8 MHz     | 250 ns         | 83.83       |

Figure 17: 250 ns synapse integrating behavior with different frequency pulse trains (columns), different values of $I_{syn}$ (rows), and different numbers of pulses (colors).
Figure 18: 6.25 μs, 500 nH synapse integrating behavior with different frequency pulse trains (columns), different values of $I_{sy}$ (rows), and different numbers of pulses (colors).
Figure 19: 6.25 µs, 2.5 µH synapse integrating behavior with different frequency pulse trains (columns), different numbers of pulses in a burst (rows), and different synaptic weights (colors).
Figure 20: Fits to the transfer functions of the 6.25 ns, 2.5 µH synapse. (a) Sigmoidal fits to the burst transfer functions for the same cases as Fig. 3(e). (b) Fits to the frequency transfer functions for the same cases as Fig. 3(f). In (b) the dashed-dotted lines are linear fits that capture the behavior well for the initial turn-on segment, and the dotted lines are sigmoidal fits that capture the behavior as the curves roll over.