Training Progressively Binarizing Deep Networks Using FPGAs

Corey Lammie, Wei Xiang, and Mostafa Rahimi Azghadi
College of Science and Engineering, James Cook University, Queensland 4814, Australia
Email: {corey.lammie, mostafa.rahimiazghadi, wei.xiang}@jcu.edu.au

Abstract—While hardware implementations of inference routines for Binarized Neural Networks (BNNs) are plentiful, current realizations of efficient BNN hardware training accelerators, suitable for Internet of Things (IoT) edge devices, leave much to be desired. Conventional BNN hardware training accelerators perform forward and backward propagations with parameters adopting binary representations, and optimization using parameters adopting floating or fixed-point real-valued representations—requiring two distinct sets of network parameters. In this paper, we propose a hardware-friendly training method that, contrary to conventional methods, progressively binarizes a singular set of fixed-point network parameters, yielding notable reductions in power and resource utilizations. We use the Intel FPGA SDK for OpenCL development environment to train our progressively binarizing DNNs on an OpenVINO FPGA. We benchmark our training approach on both GPUs and FPGAs using CIFAR-10 and compare it to conventional BNNs.

Index Terms—Deep Learning, Binarized Neural Networks, Progressive Binarization, Deep Neural Networks, Convolutional Neural Networks, CIFAR-10

I. INTRODUCTION

BINARIZATION has been used to augment the performance of Deep Neural Networks (DNNs), by quantizing network parameters to binary states, replacing many resource-hungry multiply-accumulate operations with simple accumulations [1]. It has been demonstrated that Binarized Neural Networks (BNNs) implemented on customized hardware can perform inference faster than conventional DNNs on state-of-the-art Graphics Processing Units (GPUs) [2], [3], while offering notable improvements in power consumption and resource utilizations [4]–[6]. However, there is still a performance gap between DNNs and conventional BNNs [7], which binarize parameters deterministically or stochastically. Moreover, the training routines of conventional BNNs are inherently unstable [8].

During backward propagations of conventional BNN training routines, gradients are approximated using a Straight-Through Estimator (STE) as the signum function is not continuously differentiable [1]. The gap in performance, and the general instability of conventional BNNs compared to DNNs, can be largely attributed to the lack of an accurate derivative for weights and activations in BNNs, which creates a mismatch between binary and floating- or fixed-point real-valued representations [9].

The training routines of DNNs that utilize continuously differentiable and adjustable functions in place of the signum function, which we denote Progressively Binarizing NNs (PBNNs), transform a complex and non-smooth optimization problem into a sequence of smooth sub-optimization problems. Such training routines that progressively binarize network parameters, were first used to binarize the last layer of DNNs to yield significant multimedia retrieval performance on standard benchmarks [10]. Since, various works have detailed training routines of complete PBNNs [11]–[13]. However, efficient customized hardware implementations of PBNNs are yet to be explored.

In this paper, we use the Intel FPGA SDK for OpenCL development environment to implement and train novel and scalable PBNNs on an OpenVINO FPGA, which progressively binarize a singular set of fixed-point network parameters. We compare our approach to conventional BNNs and benchmark our implementations using CIFAR-10 [14]. Our specific contributions are as follows:

• We implement and present the first PBNNs using customized hardware and fixed-point number representations;
• We use a Piece-Wise Linear (PWL) function for binarization and activations with a constant derivative to simplify computations;
• We demonstrate compared to training BNNs deterministically or stochastically on CIFAR-10, PBNNs yield a marginal, yet consistent, increase in classification accuracy, and decrease both resource and power utilizations.

II. PRELIMINARIES

A. Conventional BNNs

The training routines of conventional BNNs binarize parameters either deterministically or stochastically after performing parameter optimizations. Deterministic binarization is performed as per Eq. (1).

\[ \theta_b = \begin{cases} -1 & \text{if } \theta \leq 0 \\ +1 & \text{if } \theta > 0, \end{cases} \]  

(1)

where \( \theta_b \) denotes binarized parameters and \( \theta \) denotes real-valued full-precision parameters. Stochastic binarization is performed as per Eq. (2), where \( \sigma \) is the hard sigmoid function described in Eq. (3).

\[ \theta_b = \begin{cases} +1 & \text{with probability } \rho = \sigma(\theta), \\ -1 & \text{with probability } 1 - \rho \end{cases} \]  

(2)
σ(θ) = clip(\(\frac{\theta + 1}{2}, 0, 1\)) = \max(0, \min(1, \frac{\theta + 1}{2}))  \tag{3}

During backward propagations, large parameters are clipped using \(t_{\text{clip}}\), as per Eq. (4), where \(J\) denotes the objective function.

\[
\frac{\partial J}{\partial \theta} = \frac{\partial J}{\partial \theta_b} \mid_{\theta \leq t_{\text{clip}}}  \tag{4}
\]

**B. Progressively Binarizing DNNs**

PBNNs use a set of constrained real-valued parameters \(\theta_l\) at each layer \(l\), which are not directly learnable, but are a function of learnable parameters \(P\) at each layer [11], [12]. The shape of \(\theta(P)\) evolves during training, to closely resemble the signum function once training is complete. The hyperbolic tangent function is commonly used to relate \(\theta\) and \(P\), as described in Eq. (5).

\[\theta(P) = \tanh(v \cdot P), \tag{5}\]

where \(v\) is an adjustable scale parameter, which is used to evolve the shape of Eq. (5). The derivative of Eq. (5) is described in Eq. (6).

\[
\frac{\partial \tanh(v \cdot P)}{\partial P} = v \cdot (1 - \tanh^2(v \cdot P)). \tag{6}\]

As \(v\) increases, the shape of Eq. (5) better mimics that of the signum function. During training, parameters, denoted using \(P\), are optimized to minimize a loss function, while \(v\) is progressively increased. After training is completed, \(v\) is sufficiently large that the parameters, \(\theta\), are very close to \(\in [-1, 1]\), as depicted in Fig. 1. The final binary parameters can simply be obtained by passing \(\theta(P)\) through the signum function.

**III. IMPLEMENTATION DETAILS**

**A. Our Progressive Binarization Training Routine**

We employ a PWL function to approximate the hyperbolic tangent function, described in Eq. (7) and depicted in Fig. 2.
to simplify computations. In addition to reducing a non-linear function to a linear function, the derivative of Eq. (7), when bounded, is constant and does not depend on $P$. Consequently, when all activations are computed simultaneously, the output of each layer during forward propagations, $a_l[n]$, does not need to be stored in memory to determine gradients during backward propagations.

$$\theta(P) = \begin{cases} -1 & \text{if } P < -1 \\ v \cdot P & \text{if } -1 \leq P \leq 1 \\ +1 & \text{if } P > 1 \end{cases} \quad (7)$$

Algorithm 1 provides a high-level overview of our progressive binarization training routine. Trained binary parameters can be computed after each training epoch to determine performance on the test set during training. Here, $a_l[n]$ denotes the output of the $l$th layer at the $n$th epoch. As $v \gg 1$ the sign of the output of Batch Normalization (BN) is reformulated to reduce computation as per Eq. (8) [12].

$$\text{sign}(a_l[n]) = \text{XNOR}(I > T; \gamma > 0), \quad (8)$$

**Algorithm 1** The training routine adopted by all of our progressively-binarizing DNNs.

**Input:** Network hyperparameters (the learning rate schedule, $\eta$, scale parameter schedule, $v$, batch size, $B$, gradient optimizer, loss function, $J(\theta, y_i'(a_{l-1}), y_i)$, and the number of training epochs).

**Output:** Trained binary weights and biases, $\theta_b$.

```plaintext
for each training epoch do
    1. Forward Propagation
       $\eta; v = \eta[\text{epoch}], v[\text{epoch}]$
       for each training batch do
          for each layer do
            Determine $a_l[n] = \theta_l[n-1](P_l[n-1])$
          end for
       end for
    2. Backward Propagation
       Determine $J(\theta, y_i'(a_{l-1}), y_i)$
       for all other layers do
         Determine $\frac{\partial J}{\partial a_{l-1}[n]}$ using $\frac{\partial J}{\partial a_l[n]}$ and $\theta_l[n-1]$
       end for
    3. Parameter Optimization
       for each layer do
         Determine $\frac{\partial J}{\partial a_l[n]}$ using $\frac{\partial J}{\partial a_l[n]}$
         Determine $\theta_l[n]$ using $\frac{\partial J}{\partial \theta_{l-1}[n]}$ and $\eta$
       end for
    4. Determine the Trained Binary Parameters
       $\theta_b = []$
       for each layer do
         $\theta_b = \text{concat}(\theta_b, \text{sign}(\theta_l))$
       end for
end for
```

WHERE $T$ is defined in Eq. (9). $I$ denotes the input, $\beta$ and $\gamma$ are parameters that define an affine transform, and $u_l$ and $\sigma_l$ are the running mean and standard deviation of the feature maps that pass through them.

$$T = \mu_l - \sigma_l \cdot \frac{\beta}{\gamma} \quad (9)$$

We trained all networks until improvement on the test set was negligible (for 50 epochs) with a batch size $B = 8$. This is the largest possible batch size that makes comparison across devices possible. The initial learning rate was $\eta = 1 \times 10^{-3}$, which was decayed by an order of magnitude every 20 training epochs, i.e. when mod($\eta$, 20) = 0.

During training, each network’s scale parameter, $v$, was increased logarithmically, from 1, at the first epoch, to 1000, at the final epoch. Eq. (8) was used to determine the output of all batch normalization layers when $v \geq 500$. Adam [15] was used to optimize network parameters and Cross Entropy (CE) [16] was used to determine network losses. After the trained binary parameters were determined, for all our implementations, a conventional OpenCL BNN inference accelerator was used to perform inference on the CIFAR-10 test set.

### B. Network Architecture

The network architecture, previously used in [17], was used in all of our DNNs. This architecture is a variant of the VGG [18] family of network architectures. It is summarized in Table I. For each convolutional and pooling layer, $f$ denotes the number of filters, $k$ determines the filter size, $s$ is the stride length, and $p$ denotes the padding. Here, $N$ is the number of output neurons for each fully connected layer. All convolutional and fully connected layers are sequenced with batch normalization and activation layers. The last fully connected layer adopts real-valued representations.

### C. Hardware Architecture

All of our implementations are described using the heterogeneous OpenCL [20] framework, in which multiple OpenCL kernels are accelerated using either FPGAs or GPUs that are controlled using C++ host controllers. For FPGA implementations a SoC is used as the host controller, whereas for GPU implementations a CPU is used. We note that the

| Layer          | Output Shape | Binarized |
|----------------|--------------|-----------|
| Convolutional, $f = 128, k = 3, s = 1, p = 1$ | $(128 \times 32 \times 32)$ | ✓         |
| Convolutional, $f = 128, k = 3, s = 1, p = 1$ | $(128 \times 32 \times 32)$ | ✓         |
| Max Pooling, $k = 2, p = 2$ | $(128 \times 16 \times 16)$ | ✓         |
| Convolutional, $f = 128, k = 3, s = 1, p = 1$ | $(128 \times 16 \times 16)$ | ✓         |
| Convolutional, $f = 256, k = 3, s = 1, p = 1$ | $(256 \times 16 \times 16)$ | ✓         |
| Max Pooling, $k = 2, p = 2$ | $(256 \times 8 \times 8)$ | ✓         |
| Convolutional, $f = 256, k = 3, s = 1, p = 1$ | $(256 \times 8 \times 8)$ | ✓         |
| Convolutional, $f = 512, k = 3, s = 1, p = 1$ | $(512 \times 8 \times 8)$ | ✓         |
| Max Pooling, $k = 2, p = 2$ | $(512 \times 4 \times 4)$ | ✓         |
| Fully Connected, $N = 1024$ | $(1024)$ | ✓         |
| Fully Connected, $N = 1024$ | $(1024)$ | ✓         |
| Fully Connected, $N = 10$ | $(10)$ | ✓         |
TABLE II: Implementation results obtained using the CIFAR-10 dataset for GPU and FPGA accelerated networks. \(^1\)The mean and standard deviations reported for the Training Time per Epoch (s) metric are determined over 50 training epochs. \(^2\)Similarly to conventional networks, the unbounded ReLU [19] activation function was used instead of Eq. (7) for the real-valued FP-32 baseline implementation on GPU. \(^3\)The same test set accuracy was achieved for GPU and FPGA implementations.

| Training Routine | Total Kernel Power Usages (W) | Total Training Time (s) | Training Time per Epoch (s) | Test Set Accuracy (%) |
|------------------|-------------------------------|-------------------------|-----------------------------|-----------------------|
|                  | FPGA                          | GPU                     | FPGA                        | GPU                   |
| 8-bit Fixed Point|                               |                         |                             |                       |
| Stochastic       | 8.06                          | 133.9                   | 1,592.7                     | 31.85 ± 0.21          | 52.27 ± 0.37          |
|                  |                               |                         |                              |                       | 85.91                 |
|                  |                               |                         |                              |                       | 85.91                 |
| Deterministic    | 7.95                          | 133.0                   | 1,523.17                    | 30.46 ± 0.18          | 49.95 ± 0.31          |
|                  |                               |                         |                              |                       | 85.56                 |
|                  |                               |                         |                              |                       | 85.56                 |
| Progressive      | 7.60                          | 130.3                   | 1,383.17                    | 27.66 ± 0.17          | 46.31 ± 0.32          |
|                  |                               |                         |                              |                       | 86.28                 |
| 16-bit Fixed Point|                               |                         |                              |                       |
| Stochastic       | 10.19                         | 134.2                   | 1,989.25                    | 39.78 ± 0.17          | 62.94 ± 0.31          |
|                  |                               |                         |                              |                       | 86.45                 |
|                  |                               |                         |                              |                       | 86.45                 |
| Deterministic    | 10.03                         | 132.8                   | 1,907.17                    | 38.14 ± 0.19          | 58.19 ± 0.36          |
|                  |                               |                         |                              |                       | 86.16                 |
|                  |                               |                         |                              |                       | 86.16                 |
| Progressive      | 9.27                          | 130.5                   | 1,729.32                    | 34.58 ± 0.22          | 53.70 ± 0.34          |
|                  |                               |                         |                              |                       | 86.94                 |
| FP32 Baseline    |                               |                         |                              |                       |
| Real-valued\(^2\) | —                            | 137.1                   | —                           | 50.48 ± 0.35          | —                     |
|                  |                               |                         |                              |                       | 86.77                 |

power consumption of our FPGA implementations could be further decreased by realizing them using Hardware Description Language (HDL), removing the host controller, however, this would make fair comparisons between GPU and FPGA implementations difficult [21].

IV. IMPLEMENTATION RESULTS

In order to investigate the performance of our progressively binarizing training routine, CIFAR-10 was used. Prior to training, the color channels of each image were normalized using mean and standard deviation values of \((0.4914, 0.2023), (0.4822, 0.1994),\) and \((0.4465, 0.2010),\) for the red, green, and blue image channels, respectively. This normalization was performed because it has demonstrated significant performance on the ImageNet dataset [22]. We compare FPGA implementations adopting 16-bit and 8-bit fixed-point real-valued representations, as a large degradation in performance was observed when using smaller bit widths.

To compile OpenCL kernels for the OpenVINO FPGA, the Intel FPGA SDK for OpenCL Offline Compiler (IOC) was used, as part of the Intel FPGA SDK for OpenCL and Quartus Prime Design Suite 18.1. For our GPU implementations, a Titan V GPU was used to execute OpenCL kernels and an AMD Ryzen 2700X @ 4.10 GHz Overclocked (OC) CPU was used to drive the host controller. We used version 430.50 of the Titan V GPU driver to launch compute kernels. We report all GPU and FPGA implementation results in Table II.

From Table II it can be observed that our progressive training routine consumed the least power and had the smallest total training time on FPGA. Moreover, when adopting 16-bit fixed-point real-valued representations during training it achieved the largest test set accuracy. We believe that, similarly to [1], this can be attributed to the additional regularization that binarized parameters introduce. We note that the total training times of our GPU and FPGA implementations are not indicative of those with larger batch sizes, and that the available resources on the FPGA used, restricted us to use \(3 = 8\) across all devices.

The device utilization of our FPGA implementations is presented in Table III. Our progressive binarizing training routine consumes notably less Adaptive Logic Modules (ALMs) and Flip Flops than deterministic and stochastic routines for both 16- and 8-bit fixed-point representations. Digital Signal Processor (DSP) utilization is similar to deterministic and stochastic routines, and is only decreased marginally when 8-bit fixed-point real-valued representations are adopted.

V. CONCLUSION

We proposed and implemented novel and scalable PBNNs on GPUs and FPGAs. We compared our approach to conventional BNNs and real-valued DNNs using GPUs and FPGAs and demonstrated notable reductions in power and resource utilizations for CIFAR-10. This was achieved through approximations and hardware optimizations, as well as using only one set of network parameters compared to conventional BNNs.

We leave further hardware-level dissemination, upscaling, hyperparameter optimization, and tuning to future works.

TABLE III: Comparison of device FPGA utilization for various binarization training approaches. The numbers are extracted from acl_quartus_report.txt, generated by Quartus Prime Design Suite 18.1.

| Training Routine | Deterministic | Stochastic | Progressive |
|------------------|---------------|------------|-------------|
| Device           | Intel FPGA    | OpenVINO   | CIFAR-10    |
| Dataset          |               |            |             |
| 8-bit Fixed Point| 63.19         | 66.42      | 62.95       |
| ALMs (%)         | 81.38         | 84.87      | 76.92       |
| DSPs (%)         | 100.00        | 100.00     | 93.20       |
| 16-bit Fixed Point| 96.06         | 98.43      | 91.96       |
| ALMs (%)         | 90.40         | 94.31      | 85.54       |
| DSPs (%)         | 100.00        | 100.00     | 100.00      |
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