Research on Technology of Finger Vein Pattern Recognition Based on FPGA

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Abstract. Finger vein patterns recognition as a new type of biometric recognition technology, the existing pattern of the finger vein recognition has registered and verified the disadvantage of slow speed. Therefore, in this paper, a finger vein feature extraction and matching recognition algorithm suitable for FPGA is proposed, and the hardware system of finger vein recognition is designed and implemented, including three modules: finger vein image acquisition device, image processing module and matching display module. Finally, the key algorithm is simulated and analyzed. It speeds up the registration and recognition of mobile phone veins.

1. Introduction
As a new biometrics identification technology, finger vein pattern recognition has the advantages of being hard to steal, high precision and convenient[1]. Of course, there are some problems with the current finger vein recognition technology, such as slow registration and verification of recognition. Therefore, this paper will focus on the design and implementation of finger vein image recognition system with FPGA as the main control chip, and strive to contribute to the acceleration of finger vein image registration and its recognition speed.

2. Imaging principle of finger vein veins
As an internal feature of fingers, veins can hardly be acquired by image acquisition device under visible light environment. Through medical research, it has been proved that near-infrared irradiation will deoxidize the hemoglobin contained in human venous blood, and then the hemoglobin will further absorb the near-infrared light with wavelength of 700nm and 1000nm[2]. This makes infrared light through the veins of the fingers very rare. Therefore, 850 nm infrared light and the corresponding photosensitive camera will be used to illuminate fingers and image veins in this paper. The specific working principle is shown in Figure 1.

Figure 1. Imaging principle diagram of finger vein veins
3. Study on identification technology of finger veins

In this paper, based on the FPGA algorithm ideas of finger vein recognition as shown in Figure 2, finger vein pattern recognition system is divided into five processing steps:

- The pattern of the finger vein image acquisition.
- Preprocess finger vein images (mainly including filtering and denoising and image enhancement) in order to enhance the difference between venous area and non-venous area.
- Segmentation of finger vein veins to separate finger vein area from non-venue area.
- Expand and corroded the segmented finger vein images to obtain the global features of finger veins;
- Compare the extracted user's finger vein characteristics with the samples, and finally complete the matching recognition.

4. Structural design of finger vein pattern recognition system based on FPGA

The finger vein pattern recognition system proposed in this paper consists of three modules: image acquisition, FPGA image processing and matching display. FPGA is directly connected with USB 2.0 controller chip CY7C68014A. Recognition system using Omni Vision OV5640 CCD image sensor. Video data of CCD module is processed by FPGA and then sent to USB chip, and finally matched and recognized on computer to display the final result. Its hardware design structure is shown in Figure 3.

4.1. Image acquisition module

In this paper, the data of the system is taken by using high-resolution CCD module. The FPGA chip is connected by two wires through the IIC interface of CCD module.

4.2. FPGA image processing module

In terms of real-time image processing technology, FPGA’s parallel processing characteristics and reconfiguration are more universal than DSP systems, which are more suitable for modular design[3]. In addition, compared with other fields, FPGA has a shorter development cycle, and is easy to maintain and expand. Meanwhile, it can also process implementation signals and image data at a high speed, so it can meet real-time requirements. Therefore, this paper adopts FPGA to implement the system designed.

4.3. Communication between FPGA and computer

USB (Universal Serial Bus) is a common communication interface, which is generally used to connect PC and peripheral devices for high-speed communication. Compared with other buses, USB shows unique advantages: easy to connect, easy to use by inserting socket, high transmission efficiency and automatic detection or configuration of peripheral devices[4]. Therefore, the display system of this paper adopts USB chip CY7C68014A developed by Cypress. The method includes writing firmware program and driver program.
5. Implementation of key algorithm for finger vein pattern recognition based on FPGA

Applying the hardware description language Verilog HDL to implement the main curvature algorithm for feature extraction is the focus and difficulty of this paper. Due to space limitations, other parts will not be described in detail.

5.1. FPGA implementation of the main curvature algorithm

5.1.1. Principle and implementation. Since the image is stored in the form of digital image in the computer, the differential is used to replace the differential in the continuous signal for the gradient of the digital image.

Sobel operator is mainly used for edge detection, but technically, it is a discrete difference operator used to calculate the approximation of grayscale of image brightness function[5]. The convolution formula is as follows:

\[ g = f \ast h \]

\[ g(i, j) = \sum \sum f(i-k, j-l)h(k, l) = \sum \sum f(k, l)h(i-k, j-l) \]  \hspace{1cm} (2)

The following \( G_x \) and \( G_y \) are the convolution factors of sobel, which is the approximation of the gradient in the x direction and y direction. The convolution of these two factors with the original image is as follows. As shown in the figure below:

\[ G_x = \begin{bmatrix} -1 & 0 & +1 \\ -2 & 0 & +2 * A \\ -1 & 0 & +1 \end{bmatrix} \]

\[ G_y = \begin{bmatrix} +1 & +2 & +1 \\ 0 & 0 & 0 * A \\ -1 & -2 & -1 \end{bmatrix} \]  \hspace{1cm} (3)

Get the horizontal and vertical gray values \( G_x \) and \( G_y \) of each point in the image. In general, \( G \) is equal to the sum of the squares of \( G_x \) and \( G_y \), as shown in the following formula:

\[ G = \sqrt{G_x^2 + G_y^2} \]  \hspace{1cm} (5)

However, in order to improve efficiency, the approximation without square root is usually used, and the following is used:

\[ |G| = |G_x| + |G_y| \]  \hspace{1cm} (6)

Although this would lose precision, it would be convenient to implement on FPGA. The design thought of using parallel pipeline to calculate the Sobel operator, can increase the calculation of the whole module.

The port of Sobel operator module designed in this paper is shown in Figure 4. Clken is the completion signal received by the serial port, and the received eight-bit data is input. After the calculation of Sobel operator, the single-bit data is extended to sixteen bits of output.

![Figure 4. Sobel operator module port](image)

Process simulation is shown in Figure 5. The generated 3*3 matrix is used to convolve with Sobel operator, and the current direction gradient of target pixel is finally obtained.
Similarly, Gaussian filtering and adaptive threshold binarization and corrosion expansion are similar processing methods, but the convolution factor is different according to different filtering. I won’t repeat it here.

5.1.2. FPGA implementation of the main curvature algorithm. In this paper, principal curvature refers to the larger eigenvalue of the two eigenvalues of the image Hessian matrix. However, it is not necessary to solve the eigenvalue of Hessian matrix. I’m going to calculate it directly from the formula[6]:

$$\lambda = \frac{1}{2} \left( h_{xx} + h_{yy} + \sqrt{h_{xx}^2 + h_{yy}^2 - 2h_{xx}h_{yy} + 4h_{xy}^2} \right)$$  \hspace{1cm} (7)

Where, \( h_{xx} \) represents the special second-order partial derivative \( g_{xx} \) of a particular point in the image. There will also be gradient normalization, and threshold processing. Therefore, \( g_{xx} \) can be obtained by using the \( G_x \) convolution factor in Sobel’s implementation in the previous section. Only the convolution operation of a specific point with \( G_x \) convolution factor is needed twice.

This kernel is only meaningful for grayscale images, so this paper selected gray vein images, tested them in pipeline mode, and compared them with the results processed by MATLAB, as shown in Figure 7:

![Figure 6: Comparison diagram](image)

The original figure is on the left, the HDL function simulation results in pipeline mode are in the middle, and the software simulation results are on the right.

Finally realizes the relationship with the window size is large, color bits wide of 8, the window size of 3 situation is analyzed, according to Vivado generated report, the main resource costs such as Table 1.

| Slice LUTs* | Slice Registers |
|-------------|-----------------|
| 208         | 210             |

Meanwhile, according to the timing sequence report, the maximum Data Path Delay is 2.085ns, that is, FMax= 479.61mhz, while the mean value of PSNR is the maximum, which is equivalent to the software and can reach a very high FMax.

6. Summary
Finger vein pattern recognition has occupied an important position in the second generation of biometrics in just a few years. In order to improve the speed of finger vein registration and recognition, according to the design of FPGA characteristics, this paper proposed an algorithm of finger vein feature extraction and matching recognition suitable for FPGA implementation, and carried out simulation test and analysis on MATLAB to verify the effectiveness of the system. The hardware recognition system of finger vein veins is designed based on FPGA. Some key algorithms of finger vein feature extraction and matching recognition are implemented on FPGA.
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