Optimization of BDD-based Approximation Error Metrics Calculations

Vojtech Mrazek
Brno University of Technology, Faculty of Information Technology
Brno, Czech Republic
mrazek@fit.vutbr.cz

Abstract—Software methods introduced for automated design of approximate implementations of arithmetic circuits rely on fast and accurate evaluation of approximate candidate implementations. To accelerate the evaluation of circuit error, we propose four novel algorithms for the exact worst-case and mean absolute error analysis based on Binary Decision Diagrams. As these algorithms do not compute any absolute values in the characteristic function, which basically compares a candidate approximate circuit with a golden circuit, the error evaluation is significantly faster than the standard BDD-based error analysis. On average, the proposed algorithms are three times faster (in some cases, 30 times faster) than the baseline for 8- to 32-bit approximate adders. These results were obtained from more than 49 thousand runs with different configurations of the method. The proposed error evaluation algorithms are available as an open-source software https://github.com/ehw-fit/bdd-evaluation.

Index Terms—approximate computing, error calculation, binary-decision diagrams

I. INTRODUCTION

Minimizing power consumption is one of the most significant objectives for current digital circuit design. In many applications, such as image or signal processing, the users are also often willing to accept certain errors if they are accompanied by reduced power consumption or other improvements. This paradigm, called approximate computing [1], systematically tries to find the best trade-offs between the quality of output and hardware parameters such as area, power consumption, or latency. One of the most widely used methods is replacing the standard arithmetic circuits with approximate implementations [1]. The circuit approximation techniques can be classified as manual (e.g., [2]) and automated (e.g., [3], [4]). From a broader perspective, the automated methods usually provide better trade-offs between the error and other circuit parameters. These methods typically start with an exact circuit and modify it using the following iterative scheme: (i) generate candidate approximate circuits, (ii) evaluate these circuits, and (iii) select the best candidate for the next iteration. As many candidate circuits are usually generated, it is essential to quickly analyze their error [4].

Let \( f : \mathbb{B}^n \rightarrow \mathbb{B}^m \) be an \( n \)-input \( m \)-output Boolean function that describes the correct functionality (the accurate function) and \( f' : \mathbb{B}^n \rightarrow \mathbb{B}^m \) be an approximation of it with error \( \varepsilon \), formally \( \forall x \in \mathbb{B}^n : f(x) \approx f'(x) ; f'(x) = f(x) + \varepsilon(x) \). If there is no analytical model of the error function \( \varepsilon \) (which can, in fact, be easily derived only for a few approximation techniques such as bit-truncation), the error of \( f' \) has to be determined for all possible input combinations, i.e. \( |\mathbb{B}^n| = 2^n \).

The evaluation time grows exponentially with \( n \), but can effectively be reduced by parallel circuit simulation [5] or formal verification techniques such as SAT, BDDs or algebraic solvers [4], [6].

The formal verification techniques achieve very good performance for the error evaluation [4]. However, some of them do not scale for some types of circuits or error metrics. For example, SAT solving is applicable for determining the worst-case error but useless for the mean error. BDD-based methods are not applicable to structurally complex circuits such as multipliers.

In this paper, we deal with efficient error analysis methods using BDDs. The calculation is based on the so-called characteristic function \( |f - f'| \) represented as a Boolean equation [7]. Keszez [6] introduced a technique that does not need to compute the absolute value which represents the performance bottleneck. On the other hand, this algorithm assumes that \( \forall x : f'(x) \leq f(x) \) and can produce only such solutions that satisfy this assumption. However, this assumption is not realistic general-purpose approximation engines (such as [4]) in which arbitrary candidate approximations must be evaluated.

This paper aims to propose new algorithms for the exact error analysis that further simplify the characteristic function without postulating any specific constraint on the evaluated function \( f' \).

We propose four error calculation algorithms (two for the worst-case error and two for the mean-absolute error). These algorithms omit the absolute value calculation while the average error evaluation time is reduced \( 3 \times \) compared to the standard BDD-based approach. Moreover, they also reduce the memory complexity, and in some cases, the speedup is \( 10 - 30 \times \).

The proposed error analysis algorithms were employed in a circuit approximation method based on CGP, which is inspired in [4]. In our experiments, the error evaluation was executed for billions of adders. The resulting approximate adders exhibit better trade-offs than the approximate adders published in the EVOApprox library [8]. All approximate implementations are available for download (TBD). The C++ implementation of the error analysis algorithms is provided as an open-source software https://github.com/ehw-fit/bdd-evaluation.

II. APPROXIMATE COMPUTING

Approximate computing aims to introduce an error into a software or hardware implementation. It can be done on
various levels: algorithmic, functional, or physical. We focus on the functional approximation (i.e., modification of Boolean functions describing the logic behavior of digital circuits) of arithmetic circuits that may be used as basic building blocks in complex systems.

A. Error metrics

There are various application-independent error metrics used in the literature [2]. The worst-case arithmetic error, sometimes denoted as error magnitude or error significance, is defined as

\[ e_{\text{wce}}(f, f') = \max_{x \in \mathbb{B}^n} |\text{int}(f(x)) - \text{int}(f'(x))|, \]

where \( \text{int}(x) \) represents a function \( \text{int} : \mathbb{B}^m \rightarrow \mathbb{Z} \) returning an integer value of the \( m \)-bit binary vector \( x \). Typically, a natural unsigned binary representation is considered, i.e., \( \text{int}(x) = \sum_{i=1}^{m} 2^{i-1} x_i \). The worst-case error represents the fundamental metric that is useful to guarantee that the approximate output differs from the correct output by at most the error bound \( e \).

The average-case arithmetic error (also known as mean absolute error) is defined as the sum of absolute differences in magnitude between the original and approximate circuit, averaged over all inputs:

\[ e_{\text{mac}}(f, f') = 2^{-n} \sum_{x \in \mathbb{B}^n} |\text{int}(f(x)) - \text{int}(f'(x))|. \]

Note that the values produced by the “absolute” error metrics \( e_{\text{mac}} \) and \( e_{\text{wce}} \) can be very high. Hence, these values can be expressed relatively to the output range, using division by \( 2^m - 1 \), i.e., the maximal output value.

In the metric error formulas, the enumeration of all possible input vectors is present. For \( n \) greater than approx. 24, it is not feasible to enumerate \( \mathbb{B}^n \) in a reasonable time even when a highly parallel circuit simulator is employed.

This issue can partly be eliminated by utilizing a formal verification approach for the error calculation. Formal techniques typically construct a virtual miter circuit to compute the characteristic function. Reduced Ordered Binary Decision Diagrams (BDD) or SAT solving-based methods were employed in the area of approximate circuits. ROBDDs are suitable for the formal error analysis of less complex circuits (such as adders) for which the BDD does not grow exponentially with \( n \). SAT solving can effectively handle determining the worst-case error for up to 32-bit multipliers but does not provide suitable results for other error metrics. Details of BDDs are elaborated in Section II-C.

B. Automated design techniques

The automated approximation algorithms iteratively modify a given accurate circuit to achieve the best trade-off between the error and other circuit parameters. The most recent algorithms use various approaches for circuit representation and error evaluation. Soeken et al. proposed an algorithm that directly modifies the BDD [6], [7]. This algorithm satisfies the assumption of the fast error evaluation, but its design space is limited. Another approach is to use some internal circuit representation. Hashemi et al. divided the original circuit into subcircuits and approximated each of them. Finally, the error was evaluated for many candidate solutions [3]. A specific internal circuit representation is used in Cartesian Genetic Programming (CGP) [4] which is a heuristic design-space exploration algorithm. Candidate circuits are represented as directed acyclic graphs in a fixed grid of nodes. The algorithm randomly changes the connections between nodes and the nodes’ functions. It uses the following fitness function for a given error metric \( e \) (e.g., \( e_{\text{mac}} \) or \( e_{\text{wce}} \) ) and the acceptable error threshold \( \tau \)

\[ F(f') = \begin{cases} \text{size}(f') & \text{if } e(|f - f'|) \leq \tau \\ \infty & \text{otherwise} \end{cases} \]

This algorithm starts with an accurate solution and reduces its size while keeping the error constraint satisfied. The result of the search is the smallest circuit satisfying the constraint \( \tau \).

C. BDDs

This work exploits the Reduced Ordered Binary Decision Diagrams (ROBDDs, also referred to as BDDs). ROBDD is a canonical rooted acyclic graph-based representation of a Boolean function, where each node represents either an input variable or terminal node, and the edges represent the value assignment. There are two terminal nodes – true and false. ROBDDs have been traditionally used to solve the equivalence checking problem due to their canonical property (i.e., the ROBDDs of two logic functions are isomorphic if the functions are functionally equivalent and the input variables have the same order). The tools, developed for constructing and manipulating ROBDDs, can exactly answer the following questions: (1) whether a variable (signal) in the circuit is satisfiable, i.e., whether an input vector exists which generates a true value of the signal; and (2) the probability that a selected variable is true. Although these questions are answered fast (by finding some paths in the ROBDD), the construction of the ROBDD is not trivial, and in some circuits such as multipliers, the ROBDDs grow exponentially with \( n \).

Since there is no significant difference in the performance of major tools operating with ROBDDs [9], we selected BuDDy and CUDD tools, which also support dynamic variables re-ordering for evaluation. In these tools, the BDD node is represented by a structure. Starting with an input node, these tools allow adding new nodes by applying logical operations (\( \neg, \land, \lor, \oplus, \ldots \)) to two existing nodes. Therefore, one can construct an arbitrary Boolean function.

1) Conventions and notations: Henceforth, we denote an \( n \)-input \( m \)-output Boolean function as \( f \). Without loss of generality the functions can be represented by the BDDs \( f = (f_n, f_{n-1}, \ldots, f_1) \) where each output bit \( f_i \) is a BDD node. For integer functions, \( f_{\text{sign}} \) denotes the sign bit \( f_n \).

For one-output function (i.e., BDD node) the tools can provide the probability that a selected node \( f_i \) is true

\[ \#\text{SAT}(f_i) = 2^{-n} \cdot |\{x : f_i(x) = \text{True}\}| \]
and a Boolean value $\text{SAT}(f_i)$ answering whether the node $f_i$ becomes $\text{true}$ for any input.

We also implemented two arithmetic Boolean functions as BDDs. The Addition function $\text{add}(a, b)$ creates a Ripple-carry adder with output nodes of functions $a$ and $b$ as inputs. Similarly, subtraction function $\text{subtract}(a, b)$ is constructed in the same way, but the $b$ outputs are inverted, and the carry input is set. Note that the input vectors must be (sign-) extended to handle both signed and unsigned variants of $a$ and $b$.

2) Existing algorithms (BASELINE): In [7], Soeken et al. proposed the error analysis based on calculating characteristic both signed and unsigned variants of $a$ way, but the MAE without the characteristic function. This algorithm is constructed in the same way, which is captured by a signed function $\varepsilon$, and the absolute value is obtained (unsigned $r$). The absolute value has to deal with the two’s complement and increments the value if the result is negative (ln. 4). The binary search starts with the MSB, computes the worst-case error $wce$ and also the function $\mu: \mu(x) = 1$ if and only if $r(x) = wce$.

Algorithm 1: Baseline WCE calculation using two’s complement

```plaintext
Input : Functions $f$ and $f'$ as ROBDDs
Output: Worst-case error (wce)
1 $\varepsilon \leftarrow \text{subtract}(f, f')$; // subtract results
2 for $i \leftarrow 1$ to $|\varepsilon| - 1$ do
3 \hspace{1em} $r_i \leftarrow \varepsilon_i \oplus \varepsilon_{\text{sign}}$; // absolute value
4 \hspace{1em} $r \leftarrow \text{add}(r, \{\varepsilon_{\text{sign}}\})$; // two’s complement
5 $\mu \leftarrow \text{True}$;
6 $wce \leftarrow 0$;
7 for $i \leftarrow |r|$ to 1 do // binary search
8 \hspace{1em} if $\text{SAT}(\mu \land r_i)$ then
9 \hspace{2em} $wce \leftarrow wce + 2^{i-1}$;
10 \hspace{1em} $\mu \leftarrow \mu \land r_i$;
11 return $wce$;
```

The average (mean absolute error) is calculated (Alg. 2) with the same characteristic function $r$. The weighted sum of positive-bit probabilities is computed. Finally, the sum is divided by $2^n$ while $n$ is the number of inputs of functions $f$ and $f'$.

Keszocze showed that the subtraction and absolute value calculation are the most time-consuming parts of the evaluation [6]. He also proposed a fast algorithm for determining the MAE without the characteristic function. This algorithm needs to satisfy a condition that $\forall x : f'(x) \leq f(x)$. Automated iterative approximation algorithms typically cannot satisfy this condition, therefore, we are not able to employ this algorithm in a CGP-based approximation engine.

III. PROPOSED MAE AND WCE CALCULATION

We present improvements of the baseline error evaluation algorithms to omit the absolute value calculation. We propose two approaches — one replaces the absolute value by approximation in ones’ complement, the second one handles the positive and negative branches separately.

A. Ones’ complement (ONES’)

In the baseline Algorithms 1,2 (ln. 4), the increment of $r$ vector by a sign bit is needless. In the proposed algorithm (Alg. 3), we omitted this addition. We obtain the exact $wce$ for positive $r$; and $wce$ decreased by 1 if the maximal error is in the negative $r$. Because this condition is expressed in the MSB node of $\varepsilon$, the error can be compensated (ln. 10 - 11).

Algorithm 2: Baseline MAE calculation using two’s complement

```plaintext
Input : Functions $f$ and $f'$ as ROBDDs
Output: Mean absolute error (mae)
1 $\varepsilon \leftarrow \text{subtract}(f, f')$; // subtract results
2 for $i \leftarrow 1$ to $|\varepsilon| - 1$ do
3 \hspace{1em} $r_i \leftarrow \varepsilon_i \oplus \varepsilon_{\text{sign}}$; // absolute value
4 \hspace{1em} $r \leftarrow \text{add}(r, \{\varepsilon_{\text{sign}}\})$; // two’s complement
5 $\text{mae} \leftarrow 0$;
6 for $i \leftarrow 1$ to $|r|$ do
7 \hspace{1em} $\text{mae} \leftarrow \text{mae} + 2^{i-1} \cdot \#\text{SAT}(r_i)$;
8 return $\text{mae}$;
```

A similar approach is used in the average error calculation (Alg. 4). The error by 1 can be corrected by adding the proportion of negative numbers $\varepsilon$, i.e. $\#\text{SAT}(\varepsilon_{\text{sign}})$ (ln. 7).

B. Omitting the absolute values (NOABS)

The second proposed approach exploits the fact that we can build two BDD trees for the resulting vector $\varepsilon$ — one for the positive part $\neg \varepsilon_{\text{sign}} \land \varepsilon_i$ and one for the negative part $\varepsilon_{\text{sign}} \land \varepsilon_i$. The worst-case error calculation is shown in Alg. 5. Since the absolute error is calculated using XOR operations which
make the resulting BDDs more complex, the WCE value is calculated directly from the signed result of subtraction $\varepsilon$. If the sign bit is negative, a binary search of the maximal value is performed as $wce_p$. On the other hand, the negative part is transformed to searching the minimal value $wce_n$. The subtraction result $\varepsilon$ is expressed as two’s complement. Therefore, the negative $wce_n$ is incremented by 1, and the maximal value is returned (ln. 14).

```
Algorithm 5: Proposed WCE calculation without the absolute value (NOABS)

Input : Functions $f$ and $f'$ as ROBDDs
Output: Worst-case error ($wce$)
1 $\varepsilon \leftarrow \text{subtract}(f, f')$; // subtract results
2 /* positive error */
3 $\mu_p \leftarrow \neg \varepsilon_{\text{sign}}$;
4 $wce_p \leftarrow 0$;
5 for $i \leftarrow |\varepsilon| - 1$ to 1 do // binary search
6 if SAT($\mu_p \land \varepsilon_i$) then
7 $wce_p \leftarrow wce_p + 2^{i-1}$;
8 $\mu_p \leftarrow \mu_p \land \varepsilon_i$;
9 /* negative error */
10 $\mu_n \leftarrow \varepsilon_{\text{sign}}$;
11 $wce_n \leftarrow 0$;
12 for $i \leftarrow |\varepsilon| - 1$ to 1 do // binary search
13 if SAT($\mu_n \land \neg \varepsilon_i$) then
14 $wce_n \leftarrow wce_n + 2^{i-1}$;
15 $\mu_n \leftarrow \mu_n \land \neg \varepsilon_i$;
16 return max($wce_p, wce_n + 1$);
```

The mean average error calculation (Alg. 6) employs two BDD trees — for the positive part anded with the unset sign bit $\neg \varepsilon_{\text{sign}}$ and for the negative inverted anded with a set sign bit $\varepsilon_{\text{sign}}$. The negative part introduces an error by one, which can easily be compensated by adding the probability at line 6.

All the proposed algorithms follow the scheme of WCE and MAE calculation introduced by Soeken et al. [7] However, the absolute value calculation is partially (in ones’) or totally (in noabs) transformed from the BDD function to mathematical corrections.

IV. EXPERIMENTS

A. Experimental setup

To evaluate the quality of the proposed error calculation algorithms, we employed them in the CGP-based approximation of adders (both signed and unsigned). The overall scheme of the approximation engine is given in Figure 1. In the search loop, tens of thousands of candidate approximate adders were generated and their errors calculated. We collected all results and analyzed them statistically.

```
Algorithm 6: Proposed MAE calculation using ones’ complement

Input : Functions $f$ and $f'$ as ROBDDs
Output: Mean absolute error ($mae$)
1 $\varepsilon \leftarrow \text{subtract}(f, f')$; // subtract results
2 $mae \leftarrow 0$;
3 for $i \leftarrow |\varepsilon| - 1$ do
4 $mae \leftarrow mae + 2^{i-1} \cdot \#\text{SAT}(\varepsilon_i \land \neg \varepsilon_{\text{sign}})$;
5 $mae \leftarrow mae + 2^{i-1} \cdot \#\text{SAT}(\neg \varepsilon_i \land \varepsilon_{\text{sign}})$;
6 $mae \leftarrow mae + \#\text{SAT}(\varepsilon_{\text{sign}})$; // complement corr.
7 return mae;
```

```
Algorithm 4: Proposed MAE calculation using ones’ complement

Input : Functions $f$ and $f'$ as ROBDDs
Output: Mean absolute error ($mae$)
1 $\varepsilon \leftarrow \text{subtract}(f, f')$; // subtract results
2 $mae \leftarrow 0$;
3 for $i \leftarrow |\varepsilon| - 1$ do
4 $mae \leftarrow mae + 2^{i-1} \cdot \#\text{SAT}(\varepsilon_i \land \neg \varepsilon_{\text{sign}})$;
5 $mae \leftarrow mae + 2^{i-1} \cdot \#\text{SAT}(\neg \varepsilon_i \land \varepsilon_{\text{sign}})$;
6 $mae \leftarrow mae + \#\text{SAT}(\varepsilon_{\text{sign}})$; // complement corr.
7 return mae;
```

The key component of the calculation is the BDD library, which provides an abstraction to BDD trees. It implements the functions deciding the satisfiability SAT($d$) and calculating the probability #SAT($d$). We compared two state-of-the-art libraries — BuDDy and CuDD. The cache memory of BuDDy was set to 10^7 according to the documentation. Similarly, default size of CuDD cache (2^{18} = 262,144) was used.

The maximal allowed MAE and WCE errors that are the key parameters of CGP exponentially vary from 2 to 0.2 \cdot 2^{n+1} (20% of the output range). As a CGP seed, three adder types are considered: carry-look-ahead, carry-skip, and ripple-carry adders, unsigned and signed versions, for bit-widths 8 to 32 (of each operand). Since the CGP approximation is a

![Fig. 1. Experimental setup of CGP-based search engine employing the proposed error calculation algorithms.](image-url)
stochastic approach, 5 independent runs are executed for each setup. Finally, the best adders are synthesized using Synopsys Design Compiler with 45 nm technology.

All experiments were executed on a computer cluster with nodes having 2 CPU Intel Xeon E5-2670 2.6 GHz, 16-core, 20 MB cache, and 64 GB RAM. Each run was a single thread (with 2 GB of memory), and 32 runs were executed on the node. In total, 49,716 independent runs were performed to evaluate the above-mentioned setups.

B. CGP Approximation with BDD-based error evaluation

Table I shows that BuDDy library leads to a faster error evaluations than CuDD, except the baseline algorithm for 32-bit adders. The results are aggregated over all the error thresholds. On average, CuDD is 2x slower than BuDDy. The addition of 8 inputs ($n$) leads to a 4-20x slow down for both libraries.

![Table I](image)

Henceforth, only the BuDDy library is used in the following experiments. Table II shows the average evaluation time for different error evaluation algorithms. Both proposed implementations achieve significant speedup compared to the baseline implementation. On the average, the ones’ implementation performs better for MAE calculation, but WCE calculation is executed faster without the absolute value (noabs). We can see an enormous speedup for 20-bit and 24-bit adders for MAE and WCE, respectively. This is caused by the fact that the proposed algorithms produce smaller BDD trees that can fit the cache. Increasing the cache size could move this peek for larger sizes, but we are also limited by CPU caches and RAM.

We separately analyzed the impact of signed and unsigned versions of adders. The signed adders need the subtractor in the characteristic function to be extended by one bit. This extension slows down the error calculation by 3 - 17% for the proposed algorithms.

C. Error characterisation of 16-bit adders

We analyzed the behavior of the proposed error calculation algorithms in the design of 16-bit approximate adders in greater detail. The average evaluation time depends on the selected error analysis algorithm, error threshold, and the seed circuit. Figure 2 shows the average evaluation time for different error thresholds. The slowest evaluations are in the middle part of thresholds regardless of the evaluation algorithm. It is caused by the following: (i) For small thresholds, the BDDs representing $f$’s are not much different from the golden circuits $f$. (ii) For large thresholds, BDDs representing $f$’s are simplified (because of the approximation), and their sizes are reduced. We can see the proposed algorithms achieved significantly faster evaluations than the baseline.

![Figure 2](image)
The resulting approximate adders are synthesized to obtain hardware parameters (we focus on energy). Both error metrics are evaluated. Figure 5 shows trade-offs between $e_{wce}$ and the energy. In addition to the area estimation in the fitness function (eq. 3), we also used CGP with the area-delay product (ADP) in the fitness function. However, this setup did not improve the results in terms of energy. The resulting approximate adders outperform relevant approximate adders published in the EvoApproxLib library [8]). Moreover, we designed larger approximate adders, including the signed and unsigned variants that are not included in the library. These circuits were introduced to the new version of EvoApproxLib.

D. Synthesis and comparison to SoA

We proposed new BDD-based algorithms for the fast error evaluation of approximate adders and subtractors. Compared with the baseline implementation, these algorithms reduced the evaluation time 3x times on average. Moreover, they do not need any assumption about $f'$. These algorithms enabled us to accelerate the approximate circuit design process. Our future work will be devoted to adapting the principle for different arithmetic error metrics and the application of the proposed circuits.

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V. CONCLUSION

We proposed new BDD-based algorithms for the fast error evaluation of approximate adders and subtractors. Compared with the baseline implementation, these algorithms reduced the evaluation time 3x times on average. Moreover, they do not need any assumption about $f'$. These algorithms enabled us to accelerate the approximate circuit design process. Our future work will be devoted to adapting the principle for different arithmetic error metrics and the application of the proposed circuits.

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