A Ka-band GaAs MMIC Quadrupler with High Dynamic Range and Efficient Harmonics Rejection

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Abstract: We report a Ka-band monolithic frequency quadrupler with high dynamic range and harmonics efficient rejection based on 0.15 μm GaAs PHEMT process in this letter. The quadrupler is constructed a drive power amplifier, a one-stage active quadrupling part, a high-pass filter, and a three-stage power amplifier of the fourth harmonic. Efficient harmonics rejection is realized by harmonic restrain structure inside the quadrupling part and the filter between the quadrupling part and the output amplifier. According to the measured results, the output power reaches 20 dBm when input power ranges from -5 dBm to 1 dBm at an input frequency of 8.5 GHz. The harmonics rejections are larger than 40 dBc. The overall chip size is 3×2.2 mm².

Keywords: quadrupler, conversion gain, amplifier, harmonic, MMIC.

Classification: Microwave and millimeter wave devices, circuits, and systems

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Introduction

Frequency multiplier are widely used in millimeter-wave (MMW) system due to their advantages of highly spectral purity and stability [1-2]. With the increasing requirement of compact circuits, Microwave Monolithic Integrated circuits (MMIC) frequency multipliers up to hundreds GHz have been studied. However, the dynamic range and harmonic rejection of high-order MMIC multiplier (i.e. Quadrupler) is still unsatisfied in millimeter-wave band.

A wide variety of methods have been used in the past to perform frequency quadrupling. The methods can be catalog into active or passive, single-ended or balanced, and cascading or single-stage. Compared with passive multipliers, the active multipliers have the advantage of providing possible conversion gain. Cascading two frequency doublers is also generally used [3-4], but the suppression of the second harmonic is usually unsatisfactory. Balanced configuration is considered because it provides an efficient rejection of the fundamental and odd-harmonic frequency, and it is appropriate for implementation of a balanced VCO at the input [3-6]. As a basic topology of multiplier MMIC, single frequency multiplier circuit structure is relatively simple, flexible and convenient design which is often used by designers [7], and cascading amplifier and band-pass filter can effectively compensate for the lack of conversion gain and harmonic suppression.

In this paper, the design based on 0.15μm GaAs PHEMT process and performance of a frequency quadrupler comprised of a one-stage input power amplifier, a one-stage single-ended frequency quadrupler, a microstrip high-pass filter, and a three-stage output power amplifier is presented. Due to the chosen configuration, the quadrupler achieves high conversion gain and high output
power level with, at the same time, excellent suppression of undesired harmonics. Furthermore, the size of the MMIC is limited to 3×2.2 mm².

2. Circuit design:

The block diagram and chip layout is shown in Fig. 1. The configuration consists of an 8.5 GHz one-stage input power amplifier, a 8.5-34 GHz quadrupling part, a high-pass filter, and a 34 GHz three-stage output power amplifier. The input power amplifier supplies exactly the proper power that the quadrupling part needs to realize relatively low conversion loss. Furthermore, a high-pass filter is designed between the quadrupling part and the output power amplifier. Thus, the MMIC performs well in conversion gain and unwanted harmonics’ suppression.

![Figure 1. Block diagram (a) and chip layout (b) of the MMIC quadrupler.](image)

2.1 Quadrupling Part

This part is the core of the whole design, whose schematic diagram is shown in Fig. 2. WIN’s PHEMT standard 2×50μm MS transistor working in class-B condition is used in this part. In order to reduce the dc power consumption and generate the fourth harmonic signal the transistor is biased near the pinch off region [8], where the non-linearity of transconductance is used for frequency multiplying.

The length of T2, T3, and T7 is shown in (1). \( \lambda_0 \) is the wavelength of the fundamental, and \( f_0 \) is the frequency of the fundamental. As shown in Fig. 2., at the gate of the transistor, open-stub for \( 4 \times f_0 \) and open-stub for \( 2 \times f_0 \) (T2 and T3) supply a short circuit for the fourth harmonic and the second harmonic respectively to ensure the input signal avoiding interference of even harmonics. Two stubs (stub1 and T7) at the drain of the transistor are designed to suppress second harmonic, sixth harmonic and fundamental, third harmonic, fifth harmonic respectively. Considering that \( \lambda_0/4 \) is too long, lumped elements instead of a long transmission line are used at stub1 [2][7]. In order to improve stability of the circuit, resistors R1,
R2 and R3 are used at the dc bias stub. Input and output matching structures are thoroughly investigated to bring the least transition loss for fundamental and the fourth harmonics respectively.

\[ l_1 = l_2 = \lambda_0/8 \quad l_2 = \lambda_0/16 \]  

(1)

**Figure 2.** Schematic diagram of the EM-simulation of the quadrupling part.

Fig. 3. Shows the output spectrum when input power of this part is 12.42 dBm at 8.5 GHz. According to the simulation result, undesired harmonic suppression can reach 13.3 dBc. The rejection of the third harmonic is about 27 dBc.

**Figure 3.** Simulation result of the quadrupling part.

2.2 8.5 GHz Drive Power Amplifier

Fig. 4. Shows the schematic diagram of the 8.5 GHz drive power amplifier. In order to drive the quadrupling part, standard 2×75 um MS transistor is used in this part. The input-matching network has transmission lines T1, T2 and T3. Capacitor C3 can expand bandwidth to a certain extent, and also takes part in the input-matching. R2 and C4 can reduce low frequency gain and improve stability at low frequencies. R1 is a current limiting resistor. At drain, T4 and L play the role of output-matching. R3 brings down the gain, but can guarantee the stability.

**Figure 4.** Schematic diagram of the EM-simulation of the 8.5 GHz drive power amplifier.
2.3 34 GHz Output Power Amplifier

Due to conversion loss of the second part, the output power of the quadrupler is about -1 dBm. Thus, an output power amplifier is designed to improve the conversion gain of the whole MMIC and so enough output power that the application of the quadrupler is much more convenient. The output power amplifier not only increases the output power of the quadrupler, but also plays a role in rejection of other harmonics.

Schematic diagram of the three-stage 34 GHz output power amplifier is presented in Fig. 5. Gate width of three transistors are respectively 2×50 um, 2×50 um, 4×50 um. Matching structures and dc bias circuits of each stage are designed quite similar. L-type microstrip matching structure is adopted at each gate and drain of the transistors. In order to reduce gain and improve the stability, a series resistance is added to the gate of each transistor. Capacitors are cascaded between stages in order to isolate biases. Resistors and capacitors used in the bias structures reduce the low frequency gain and improve the stability at low frequencies.

![Figure 5. Schematic diagram of the part of 34 GHz output power amplifier.](image1)

2.4 High-pass Filter

In order to realize higher suppression of lower harmonics, a high-pass filter is designed between the quadrupling part and the output power amplifier. Its schematic diagram is shown in Fig. 6. The filter is structured by transmission line cascaded with two capacitance paralleled with an open stub. Function of high-pass is formed by the capacitance, and the open stub shown in Fig. 6 generates a resonance point of the third harmonic. Simulation result of this part is shown in Fig. 7.

![Figure 6. Schematic diagram of the part of the high-pass filter.](image2)
Figure 7. Simulation result of the high-pass filter.

3 Measured MMIC performance:
The test board shown in Fig. 8 is designed. The testing work is done on probe station for that RF signal is still added and received through GSG probes.

Figure 8. Test board and the picture of the MMIC.

Figure 9. Measured output power of the quadrupler in comparison with the simulation result as a function of input power at an input frequency of 8.5 GHz.

Fig. 9. presents the measured output power of each harmonic (from fundamental to the forth harmonic) of the quadrupler in comparison with the simulation result as a function of input power at an input frequency of 8.5 GHz. The quadrupler delivers 20 dBm when it gets saturated at an input power of about -5 dBm. Compared with simulation result, measured result is a little worse. We can judge
from the graph that the rejection of fundamental is beyond 55 dBc, the rejection of the second harmonic is beyond 54 dBc, and for the worst, the rejection of the third harmonic is beyond 40 dBc. The total working current of the quadrupler is less than 150 mA. The quadrupler performs quite similar when input frequency ranges from 8.4 GHz to 8.6 GHz. The flatness of output power of the quadrupler is 0.5 dBpp from 33.6 GHz to 34.4 GHz.

**Figure 10.** Measured $S_{11}$ and $S_{22}$ of the quadrupler in comparison with the simulation results.

Fig. 10. shows the measured result of $S_{11}$ and $S_{22}$ compared with the simulation ones. We can judge with this result that the measured S-parameter offsets down from the simulation one. The offset increases with the increase of frequency. It’s obvious that the offset is about 2 GHz at 25.5 GHz which is the frequency of third harmonic. This conclusion may cause offset of the simulation result of the filter shown in Fig. 7. Which is the reason of the distinguish of output harmonics between test and simulation shown in Fig. 9.

Table. 1. Summarizes some of the characteristics of the published MMIC quadruplers or the products of major microwave or RF corporations. The performances of the quadrupler designed in this paper is mentioned at the bottom of the table for comparison. To my knowledge, such significant performance in conversion gain and undesired harmonic suppression of this work has never shown up in former works.

| Ref. | Type | $P_{out}$ (dBm) | $F_{reqout}$ (GHz) | Reject. (dBc) | Conv.G. (dB) | Size (mm$^2$) | $P_{DC}$ (mW) |
|------|------|----------------|-------------------|--------------|-------------|--------------|--------------|
| [2]  | 2 sing.$\times$2 | 1.4 | 12-12.8 | - | 4.4 | 1.69 | 35 |
| [3]  | 2 bal.$\times$2 | 19.4 | 36-40 | 30 | 16.4 | 2.76 | 1596 |
| [4]  | 2 bal.$\times$2 | 0 | 27-34 | 30 | -5 | 6.75 | 163 |
| [6]  | bal.$\times$4 | -2.5 | 30 | 30 | -7.5 | 3 | 54 |
| [7]  | sing.$\times$4 | -5 | 59 | - | -5 | 2.38 |
| [8]  | sing.$\times$4 | 6.9 | 56-64 | 40(for fundamental) | 6.9 | - | - |
| [9]  | $\times$4 | 0 | 14.4-16.4 | 22 | -5-15 | Packaged | 275 |
| [10] | $\times$4 | 7 | 11.4-13.2 | 25 | 2-17 | Packaged | 300 |
| [11] | 2$\times$2 | 11 | 36-40 | 15 | -1 | 2.25 | 280 |
| [th] | sing.$\times$4 | 20 | 32.4-35.6 | 40 | 19-25 | 6.6 | 705 |
4. Conclusion:

The design of a Ka-band GaAs MMIC quadrupler with high conversion gain and efficient rejection of undesired harmonics is discussed in this publication and the chosen configuration realizes a remarkable performance as shown in the measured result. With a chip size of $3 \times 2.2 \text{ mm}^2$, the MMIC performs that the conversion gain ranges from 25 dB to 19 dB and correspondingly the output power reaches 20 dBm when input power ranges from -5 dBm to 1 dBm at an input frequency of 8.5 GHz. Meanwhile, the rejection of fundamental is 55 dBC and rejection of unwanted harmonic is 54 dBC for the second harmonic, and 40 dBC for the third at an input power of -2 dBm, frequency of 8.5 GHz.