A Sigma-Delta modulator circuit using correlated double sampling

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Abstract. This paper presents a 14-bit ΔΣ analog-to-digital converter (ADC) with 2.35 kHz BW, while operating from a 3.3V supply. Correlated double sampling (CDS) are used to mitigate the ADC’s offset and 1/f noise, especially at low frequencies.

1. Introduction
In the oversampling ΔΣ analog-to-digital converter, the oversampling, feedback, digital filter and other technologies are used to effectively reduce the noise in the baseband of the system, so that the Sigma-Delta converter has an accuracy of at least 14-bit. The circuit structure is widely used in digital audio circuits and ADSL (Asymmetric Digital Subscriber Line) systems [1-2].

In order to meet the requirements of high precision and low noise with low-frequency input signal, this paper designs a Sigma-Delta converter based on correlated double sampling technology. The Sigma-Delta analog-to-digital converter circuit adopts a third-order, single-loop structure and a quantized output. The feedforward structure improves the stability of the modulator loop, reduces the output swing of the integrator, and relaxes the requirements for operational amplifier characteristics and improves linearity [3]. The modulator is realized by a fully differential switched capacitor, the sampling frequency is 3.2 MHZ, the input signal frequency is 781.25 HZ, the common mode voltage is 1.65V and the amplitude is a sine wave of 100 mV.

The SMIC 0.18um CMOS process is used to design each sub-module circuit in the modulator, including integrator, operational amplifier, adder, comparator, reference and bias circuit, two-phase non-overlapping clock, etc [4]. The overall layout design of ADC is completed. Signal-to-noise ratio of ADC under different process corners is simulated. The final experimental results show that the optimized ADC has 14-bit accuracy with bandwidth of 2350 Hz, where the FFT result is achieved with 2\textsuperscript{14}-points.

2. Adc architecture and implementation
Fig.1 shows the block and timing diagram of the ADC. It is based on a single-loop single-bit 3rd-order SC ΔΣ Modulator with an energy-efficient feedforward architecture, three operational-transconductance-amplifiers (OTAs), and a SC summing network.
Four inner set of switches together with two-phase non-overlapping clock clk1d_in and clk2d_in, implement a correlated double sampling (CDS) scheme that mitigates the effect of offset and 1/f noise of the 1st OTA. During clk1d_in, the input signal, Vin, and the OTA offset are sampled on the 0.8pF input capacitors, Cs. During clk2d_in, the cross-coupled switch reverses the input and thus transfers a charge packet proportional to 2•Cs•Vin to the integration capacitors, Cint. This cross-coupled sampling scheme ensures that the only components exposed to the input CM voltage are the capacitors Cs and capacitively coupled switches. Each switch is controlled by non-overlapping clock signals clk1d_in or clk2d_in, generated by standard 3.3 V logic. The two-phase non-overlapping clock and comparator control levels are shown in Fig.1 (b). The first-stage integrator is shown in Fig.2. For the Delta Sigma modulator with the third-order structure, the first-stage integrator plays a vital role. It needs a larger gain and bandwidth to suppress the noise and offset of the latter-stage integrator; at the same time, the first-stage integrator It has requirements on the noise and offset of the system. The requirements of the system for the second and third stage integrators are lower. Because the noise contribution and offset of the second and third stage integrators to the system are small, the sampling capacitance and integral capacitance of the latter two-stage integrators are smaller than those of the first-stage integrator. The operational amplifiers in the three-stage integrator all adopt the same structure, but the tail current value will be adjusted proportionally with the sampling and integration capacitance value of the integrator, then the sampling and integration capacitance of the three-stage integrator is in turn: 0.8 pF, 4.8 pF; 0.5 pF, 2 pF; 0.5 pF, 2.5 pF.

The Z-domain transfer function of the integrator is shown below:

\[ H(Z) = \frac{z^{-1} C_s}{1 - 2^{-1} C_{int}} \]  

(1)

The gain of the integrator is determined by the ratio of the sampling capacitor Cs and the integrating capacitor Cint. The above transfer function is obtained under ideal conditions. In fact, the gain of the operational amplifier is not infinite, and the integral circuit will leak.
Assuming that the gain multiple of the operational amplifier is \( A \), Fig. 1(a) shows the implementation of the integrator in the modulator:

\[
C_{\text{int}}V_{\text{out}}(nT+T)(1+\frac{1}{A}) = C_s[V_{\text{IP}}(nT)-V_{\text{out}}(nT)-V_{\text{IN}}(nT+\frac{T}{2})-\frac{V_{\text{out}}(nT)}{A}]
\]  

This equation can be expressed in the z domain as:

\[
V_{\text{out}}Z(1+\frac{1}{A}) = \frac{C_s}{C_{\text{int}}}[V_{\text{IP}}-V_{\text{out}}-\frac{ZV_{\text{IN}}}{Z}]
\]  

After finishing, get the integrator transfer function:

\[
\frac{V_{\text{out}}}{V_{\text{IP}}-Z^2V_{\text{IN}}} = \frac{C_s}{C_{\text{int}}Z[1+\frac{1}{A}]+C_s(1+\frac{T}{2})}
\]  

All integrators are built around folded-cascode OTAs. The 1st integrator achieves 98dB DC gain and draws 640.68 uA. Setting \( C_{s1}=0.8\text{p} \) ensure that the ADC is thermal noise limited. The 2nd and 3rd integrators are scaled down by 2x to improve power efficiency. The comparator consists of a pre-amplifier and a dynamic latch. The output of three integrators are summed by a passive SC adder.

### 3. Layout completion and simulation results

The modulator is implemented in a SMIC 180nm CMOS process and occupies 2.48mm\(^2\) (Fig. 2). The chip draws 4.45mA from a 3.3V supply: 2.42mA by the three integrators & comparator & current mirror & buffer, and 2.03mA by the clock generator.

In the time domain, the integrator integrates the difference between the input and output of the modulator, and the result of the integration is used as the input of the quantizer. Negative feedback reduces the difference between the input and output of the modulator as much as possible. As a result, the average value of the output signal follows the input signal, as shown in Fig. 3. It can be seen from Fig. 3 that the ΔΣ modulator modulates the input signal with pulse width, and the average value of its output follows the input. Fig. 3(a) shows a simplified diagram of the input and output signals with one input signal period, and Fig. 3(b) presents a detailed diagram of the output signal with a period from 100 to 200 μs.
Fig 3. Input and output of Delta-Sigma modulator. (a) Sketch map of modulator input and output signal with one period of input signal (b) Detail diagram of modulator output signal (100us-200us)

After using the correlated double sampling structure, the flicker noise of the modulator at low frequencies remains at a low level. $2^{14}$-point FFT results of the ΔΣ modulator with and without CDS is shown in Figure Fig. 4. The red line is the FFT result without CDS technology. The signal-to-noise ratio (SNR) is given by:

$$SNR = 10 \log \left( \frac{2^{2L+1} OSR^{2L+1}}{n^{2L}} \times (2^N - 1)^2 \right)$$  \hspace{1cm} (5)

Where $N$ is the number of quantization bits, the order of the modulator is $L$. 


As shown in Fig. 4, the input signal is a sin wave with a peak to peak voltage of 200 mV, and the frequency is 781.25 HZ. The low-frequency (from 0 to 200 Hz) noise of the modulator is significantly lower than the modulator without using CDS. At the same time, under the 2.35 KHz bandwidth, the SNR is 88.8 dB, SNDR is 86.7 dB and the ENOB is 14.1 bits.

In order to simulate the modulator with CDS has a lower noise at low frequency, a mismatch-size input pairs for OTA in the 1st integrator is used to obtain an equivalent offset of 1.5 mV in this design. As shown in Fig. 5, the ΔΣ modulator with CDS has a lower value at low frequency (from 0-200 Hz) than the modulator without CDS. ΔΣ modulator with CDS achieves a SNR of 91.9 dB and ENOB is 15 bits.

In addition, the offsets in the 2nd and the 3rd integrator can be equivalent to the offset of 1st integrator. Fortunately, they can be significantly reduced by a high-pass transfer function that is an inverse of the integrator’s transfer function, where the integrator’s transfer function is a low-pass filter.

Fig4. Simulated 2^{14}-point FFT results of the ΔΣ modulator output.

Fig5. Measured 2^{14}-point FFT of the ΔΣ modulator output (The input differential pair of the first stage integrator op amp has a deviation of 1.5mV from the gate)

4. Conclusion
This article designs a ΔΣ ADC based on correlated double sampling technology. The ΔΣ ADC explained the role of correlated double sampling technology, and disassembled the specific circuits of each module.
of the modulator. And with this technology, the system structure is optimized, and the ratio of the sampling capacitor to the integrating capacitor is adjusted, so as to obtain better low-frequency characteristics, and the low frequency band of 1/f noise below 200 HZ is significantly reduced. The simulation results show that it also has some suppression on the offset of 1st OTA.

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