MAC-DO: Charge Based Multi-Bit Analog In-Memory Accelerator Compatible with DRAM Using Output Stationary Mapping

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ABSTRACT

Deep neural networks (DNN) have been proved for its effectiveness in various areas such as classification problems, image processing, video segmentation, and speech recognition. The accelerator-in-memory (AiM) architectures are a promising solution to efficiently accelerate DNNs as they can avoid the memory bottleneck of the traditional von Neumann architecture. As the main memory is usually DRAM in many systems, a highly parallel multiply-accumulate (MAC) array within the DRAM can maximize the benefit of AiM by reducing both the distance and amount of data movement between the processor and the main memory. This paper presents an analog MAC array based AiM architecture named MAC-DO. In contrast with previous in-DRAM accelerators, MAC-DO makes an entire DRAM array participate in MAC computations simultaneously without idle cells, leading to higher throughput and energy efficiency. This improvement is made possible by exploiting a new analog computation method based on charge steering. In addition, MAC-DO innately supports multi-bit MACs with good linearity. MAC-DO is still compatible with current 1T1C DRAM technology without any modifications of a DRAM cell and array. A MAC-DO array can accelerate matrix multiplications based on output stationary mapping and thus supports most of the computations performed in DNNs. Our evaluation using transistor-level simulation shows that a test MAC-DO array with 16 x 16 MAC-DO cells achieves 188.7 TOPS/W, and shows 97.07% Top-1 accuracy for MNIST dataset without retraining.

1. INTRODUCTION

Following the emergence of “Internet of Things” (IoT), demand for processing a large amount of data efficiently in edge devices keeps increasing [1, 2, 3]. In order to more accurately process those massive data collected from IoT devices, numerous artificial neural networks (ANN) such as deep neural networks (DNN) are widely used. Deep neural networks have been proved for its effectiveness for diverse classification problems, image processing, video segmentation, and speech recognition [4, 5, 6, 7, 8, 9, 10, 11], but they require a vast amount of network parameters and multiply-accumulate (MAC) operations in return. In a traditional computer architecture called von Neumann architecture, processing a huge amount of data may be inefficient due to a bottleneck between the cpu and memory as shown in Figure 1-(a). GPUs can mitigate the bottleneck problem since it computes MAC operations parallelly and reuses the data many times once it is read from the memory. However, it still has several limitations such as high cost and energy consumption [12].

Accelerator-in-memory (AiM) architectures can minimize the cost for data movement and avoid the memory bottleneck by performing computations within a memory [13, 14, 15, 16, 17, 18, 19]. One of the key design points for AiM architectures is how efficiently and effectively it can process a great amount of data under a restricted area around the memory. Accordingly, many different types of memory arrays such as SRAM and ReRAM have been actively investigated for AiM architectures [20, 21, 22, 23, 24, 25]. Though SRAM based accelerators have been proved for its potential for computations [20, 21, 26], it still has a limitation of large cell area. ReRAM based accelerators also have superior computation ability, but may suffer from intrinsic data retention issues [27, 28]. Due to these limitations, network parameters are usually stored in the main memory and a small portion of it is temporarily copied to these AiM arrays and used. Therefore, the overall performance of SRAM and ReRAM based AiMs is limited because they require long distance of data movement between the main memory and the arrays as shown in Figure 1-(b).
On the other hand, DRAM based AiM accelerators can be placed close to the main memories of many computing systems and minimize the distance and amount of data movement between the processor and the main memory. Actually, many near-DRAM accelerators have been developed and used in industry, including Google TPUs (HBM memories are used since TPUv2 [29]), UPMEM PIM-DRAM [30]. Although the distance of data movement is shorter than SRAM and ReRAM based accelerators, most of the near-DRAM accelerators still require frequent data movement between individual DRAMs and data processing chips, which costs much more than on-chip data movement.

Monolithic integration of processing blocks and data storage in a single chip is one of the most power-efficient solutions. [31] used embedded DRAMs (eDRAMs) for such integration using a CMOS logic process technology, but the capacity of an eDRAM in a logic process is not as good as a modern DRAM. Also, many in-DRAM data processing techniques and architectures like Figure 1-(c) have been presented recently [32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43]. However, they require a large amount of data movement between the accelerator and DRAM arrays since their data reuse rate is low because of destructive read operation in DRAM. In addition, they can only perform simple logic operations such as NOR and NOT in a computation cycle and require many cycles for more complex operations, such as multi-bit MAC operations. Besides, only a few cells in each DRAM column participate in a computation and remaining cells sit idle, leading to low array utilization, throughput and energy efficiency. It may be enough for accelerating some data-intensive tasks that memory bandwidth is a bottleneck, but accelerating compute-intensive tasks, e.g. convolutions comprising over 90% computations and runtime of CNN operations [44], is limited due to the low array utilization and throughput.

In order to solve those limitations of DRAM based accelerators, this paper presents an analog MAC based in-memory accelerator architecture like Figure 1-(d), named MAC-DO. In contrast with many previous DRAM based accelerators, a MAC-DO cell supports a single-cycle MAC operation with multi-bit precision input and weight, using two 1T1C cells in a DRAM array. For this, MAC-DO adopts a new analog computing mechanism based on charge steering, which was originally proposed for high-speed analog and mixed-signal circuits [45]. It is basically a discrete-time analog amplifier with a voltage gain $A_v$ between a $V_{in}$ and a $V_{out}$, and its voltage gain is decided by the ratio of two capacitance values. Hence, the voltage gain is stable since capacitors are less influenced by PVT variation than transistors [46], as well as easily controllable by changing the size of one capacitor. This allows multiplication of two arbitrary numbers, regarding a differential analog signal $V_{in}$ as an input multiplicand and the voltage gain $A_v$ as the other.

In addition, MAC-DO is compatible with modern DRAM arrays and does not require any modifications of a DRAM cell and array for MAC operations. A MAC-DO cell requires only two 1T1C DRAM cells and all DRAM cells in an array can participate in parallel computations at a time without an idle cell by employing an output stationary mapping [47, 48, 49]. Also, MAC-DO has much increased throughput and better energy efficiency than previous DRAM based accelerators, even using a very small portion of banks and mats in a DRAM chip. Thus, the overall chip cost of MAC-DO is expected to be low and can extend the range of AI applications to low-cost and low-power edge devices [50].

The main contributions of this paper are listed as follows:

- This paper presents an analog MAC based in-memory accelerator which implements charge-based MAC operations between multi-bit signed inputs and weights. It ensures higher linearity than current-based accelerators since capacitors are less susceptible to PVT variation.

- A MAC-DO cell exploits charge steering technique that was originally used for analog and mixed-signal applications only. This paper first proves its applicability in highly parallel analog computing by proposing a 2-D array architecture, control methods, and error compensation schemes that are supported by extensive transistor-level simulation data. MAC-DO can take advantages of charge steering, including high-speed operation, good linearity and reliability, for analog computing as well.

- MAC-DO is compatible with modern DRAM array directly without any changes of DRAM cells. Hence, the overall integration cost of MAC-DO would be low.

- To the best of our knowledge, MAC-DO is the only architecture that can utilize every DRAM cell in an array for MAC operations for a computation cycle. Previous DRAM based accelerators activate only a few rows for computations and other rows remain idle. On the other hand, MAC-DO makes all DRAM cells participate in MAC operations simultaneously and each of them makes a different partial sum for MAC results. As a result, MAC-DO can greatly improve both the throughput and energy efficiency.

The rest of this paper is organized as follows. Section 2 introduces the background of previous DRAM based accelerators and outer product for MAC operations. Section 3 describes charge-steering topology for MAC-DO, actual MAC-DO circuits and its operation. Section 4 demonstrates digital and analog correction for negative weight and non-linear effects. Section 5 explains the evaluation methodology for performance test. Section 6 presents the evaluation results of MAC-DO. Section 7 concludes this paper.

2. BACKGROUND

2.1 DRAM and Its Operation

A DRAM chip consists of multiple banks connected by a global shared bus. Each bank is composed of subarray groups and each of them includes several cell matrices (mat), which is the basic unit of the DRAM chip. Each mat has its own independent sense amplifier (SA) row, a word-line (WL) decoder and a DRAM array. A SA amplifies the signal on a bit-line (BL) and quantizes it. A WL decoder controls WLs to write or read data. There are numerous DRAM cells inside a DRAM array and each cell consists of an access transistor.
and a cell capacitor, called a 1T1C cell as shown in Figure 2. The access transistors are exploited to write data into each cell capacitor or to read the data stored in each cell through WLs and BLs. For example, when writing data ‘1’ into a cell, the corresponding WL is activated and the cell capacitor is charged to a high voltage through the corresponding BL. On the other hand, if the cell capacitor is discharged, the cell stores data ‘0’. In a read process, a row of access transistors is activated and the stored data are read through the SAs.

2.2 Conventional In-DRAM Accelerator

Many in-DRAM accelerators recently have been presented to reduce data movement cost between the processor and the main memory. Ambit (Figure 3-(a)) uses Triple Row Activation (TRA) for a logic operation through charge sharing on BLs [33]. DRISA’s 1T1C (Figure 3-(b)) adds digital logic gates outside a DRAM array and it performs a logic operation by activating two rows sequentially. DRISA’s 3T1C (Figure 3-(c)) modifies a 1T1C DRAM cell into a 3T1C DRAM cell and activates a few rows for a logic operation [38]. Though they reduce the distance of data movement more than SRAM and ReRAM based AIsM, they can perform only simple logic operations such as NOR and NOT for a computation cycle, still requiring a lot of overall data access and data movement for multi-bit MAC operations, and it may worsen the power efficiency. Besides, they require additional data movement cost for copying the stored data \((D_i, D_j, D_k)\) into other DRAM arrays before a computation because DRAM read process is destructive. Also, their throughput is limited since only a few row cells out of the entire DRAM array participate in operations while most of the cells are not activated for a computation cycle as shown in Figure 4-(a). Lastly, they are not suitable to modern DRAM technology because they require logic gates or modifications of a 1T1C DRAM cell for computations.

2.3 Outer Product

For higher DRAM array utilization throughout operations (Figure 4-(b)), output stationary data mapping can be used. It basically multiplies two matrices \(A\) and \(B\) through iterative outer products between columns of \(A\) and rows of \(B\) [51] (Fig-
Figure 6: Convolutions

Figure 7: The operation of a charge-steering amplifier

3. MAC-DO AND ITS OPERATION

3.1 Charge-Steering Amplifier

MAC-DO is based on a charge-steering topology [45]. Charge steering can be used for a discrete-time analog amplifier, offering high-speed and low-power amplification compared with traditional current-steering amplifiers. As shown in Figure 7, the charge-steering amplifier operates in two phases: reset phase and amplification phase. In the reset phase (Figure 7-(a)), two capacitors at the output terminals (C_P) are precharged to V_DD using two precharge (PREC) switches, while the tail capacitor C_T is reset to zero by turning on the RESET switch. At the same time, the two transistors M_1 and M_2 are turned off in order to block charge flow between the capacitors. In the amplification phase (Figure 7-(b)), the PREC and RESET switches are turned off, and both transistors M_1 and M_2 are turned on with a differential input signal V_in = V_{in(+)} - V_{in(-)}. The tail capacitor C_T is connected to the differential pair M_1 and M_2 through a switch enabled by the clock signal CK. During the amplification phase, charges in output capacitors are discharged to the tail capacitor for a certain period, and the relative amount of discharge from two output capacitors are controlled by the differential input signal. Therefore, a differential voltage gain A_V is mainly determined by the ratio between the capacitance of C_T and C_D [45], with little dependence on the common mode voltage of V_in as

$$ A_V \approx \frac{2C_T}{C_D}. $$

Hence, a differential output signal V_out is written as

$$ V_{out} = A_V \times V_{in}. $$

where the V_out is the differential output voltage between the V_Q and V_QN. Here, V_{Q} = V_{DD} - A_VV_{in(+)} and V_{QN} = V_{DD} - A_VV_{in(-)}, so that V_{out} = A_V(V_{in(+)} - V_{in(-)}). Consequently, multilevel V_out voltages can be generated depending on various V_{in} signals and A_V values.

The charge-steering amplifier has two advantages over a traditional current-steering amplifier. First, its discrete operation is compatible with other digital circuits and helps save unnecessary power consumption. Secondly, it maintains stable operation even at high operating frequency up to a few GHz domains [52, 53]. As a result, the charge-steering topology is suitable for analog MAC operations where both the power efficiency and speed are required.

3.2 Mapping a Charge-Steering Amplifier onto Two IT1C Cells

A DRAM array can be reorganized into an array of charge-steering amplifiers. Figure 8-(b) shows a modified charge-steering amplifier mapped on a DRAM array, which consists of two access transistors and two cell capacitors (two IT1C DRAM cells). The tail node of the differential pair M_1 and M_2 in the charge-steering amplifier corresponds to the bit-line of the two IT1C DRAM cells. The two PREC switches in the original charge-steering amplifier can be combined with M_1 and M_2 with an extra PREC switch at the tail node, or the corresponding bit-line as shown in Figure 8-(b). In this modified charge-steering amplifier, V_Q and V_QN are precharged to V_DD by turning on M_1, M_2, and PREC. M_1 and M_2 transistors need to be turned on by a voltage higher than V_{DD} + V_{TH} in order to fully precharge two DRAM cell capacitors to V_DD. During amplification, two WLs of the modified charge-steering
amplifier receive $V_{in(+)}$ and $V_{in(-)}$ voltages composing a differential input $V_{in}$. Since the charge-steering amplifier and the modified charge-steering amplifier are identical except the position and the number of PREC switches that are only activated during reset phase, the modified charge-steering amplifier follows the same amplification phase as discussed in Section 3.1. As a result, a differential output signal $V_{out}$ is generated from the two DRAM cells, at $V_Q$ and $V_{QN}$.

### 3.3 A MAC-DO Cell for a Series of Multi-Bit MAC Operations

In order for the modified charge-steering amplifier to perform MAC operations with multi-bit input and weight data, $V_{in}$s and $A_v$s must be controllable by the input and weight data. It requires modifications on wordline and bitline drivers to the DRAM array MAC-DO cells are mapped on. In addition, a series of accumulations for an output stationary data flow involves a small change of operation phases.

A MAC-DO cell and WL/BLS drivers: A MAC-DO cell consists of two DRAM cells as shown in Figure 9 and carries out multi-bit MAC operations inside the cell. A multi-bit digital input is converted into a differential input signal $V_{in}$ for $M_1$ and $M_2$ through a digital to analog converter (DAC). A multi-bit digital weight controls effective capacitance of the tail capacitor $C_T$ by enabling a part of parallel tail capacitors through a thermometer code decoder, and therefore controls the gain of the amplifier, $A_v$. Here, only a MAC-DO cell is located inside a DRAM array and the other circuits are in the array periphery. Each multiplication result is accumulated at the $V_Q$ and $V_{QN}$ as a differential signal $V_{out}$ without additional precharge phases. This innate accumulation process necessitates an output stationary data flow for the array control since the MAC-DO cell is optimized for accumulating MAC outputs instead of storing input and weight data. The detailed MAC operation consists of 3 phases as follows.

1. Reset and precharge phase: In the first phase, the MAC-DO cell is prepared for following MAC operations as shown in Figure 10-(a). The PREC switch, $M_1$ and $M_2$ are turned on, so that two cell capacitors are fully precharged to $V_{DD}$, resulting in $V_{out}=V_{QN}$. At the same time, the $RESET$ switch and all tail switches are turned on to reset all tail capacitors. These two operations are independent and both are carried out in this phase.

2. Multiply-accumulate (MAC) phase: In this phase, the PREC and $RESET$ switches are turned off first. Then, a differential $V_{in}$ signal corresponding to a multi-bit input is applied to $M_1$ and $M_2$ through a DAC. The $A_v$ value is adjusted according to a multi-bit weight by controlling the tail switches through a thermometer code decoder. As a result, the MAC-DO cell performs multiplication of multi-bit input and weight and generates a differential output voltage $V_{out}$ as

$$V_{out} = V_{in} \times \sum_{i=1}^{N} 2C_i \frac{C_D}{2C_D}$$

(4)

, and this first multiplication result is accumulated at two cell capacitors as a differential voltage. Here, $N$ determines the ratio of $\frac{C_T}{C_D}$ and hence the differential gain $A_v$. For example, if $N$ is 2, two tail switches are turned on as shown in in Figure 10-(b) and it leads to $V_{out} = V_{in} \times \frac{2C_1+C_2}{2C_D}$. Higher $N$ increases $A_v$ and is used for greater weights. With a proper conversion between the analog and digital domains, the Equation (4) can be transformed as

$$OUT = I \times W$$

(5)

where $OUT$, $I$ and $W$ corresponds to $V_{out}$, $V_{in}$ and $\sum_{i=1}^{N} 2C_i \frac{C_D}{2C_D} = A_v$, respectively. Both the input ($I$) and weight ($W$) can be easily converted to corresponding analog values ($V_{in}$ and $A_v$) by using a DAC for $V_{in}$ and a bank of tail capacitors for $A_v = \sum_{i=1}^{N} \frac{2C_i}{C_D}$.

3. Standby phase: After a MAC operation is performed in the MAC phase, $M_1$ and $M_2$ are turned off. Accordingly, the MAC result $V_{out}$ is stored at two cell capacitors as a differential analog value (Figure 10-(c)). Meanwhile, all tail switches and the $RESET$ switch are turned on to reset all tail capacitors and prepare for the next MAC operation.

A final MAC result is obtained by repeating the MAC phase and the standby phase alternately without additional precharge phase. For instance, when second input and weight data are applied after the first standby phase, the second multiplication is performed without precharging the DRAM cell capacitors (Figure 10-(b)). The second multiplication result is accumulated in the same capacitors (at $V_Q$ and $V_{QN}$) with the previous result from the first multiplication. Output voltages stored in the cell capacitors barely affect the new
\[ OUT_{FINAL} = \sum_i OUT_i = \sum_i I_i \times W_i \] (6)

which is the same equation as a vector dot product operation, or a series of multiply-accumulate (MAC) operations.

Figure 10: MAC operation phase of MAC-DO

Figure 11: A MAC-DO array structure

Figure 12: Matrix multiplications in a MAC-DO array for convolution

Figure 10-(d) shows the detailed timing diagram for MAC operations of MAC-DO. Since the MAC-DO cell recycles the stored charge from the first precharge phase for remaining MAC operations, it features an outstanding energy efficiency.

3.4 Array Structure

Multiple MAC-DO cells in Figure 9 are combined and reorganized into an array for computing highly parallel MAC operations such as convolutions in CNN. A MAC-DO array is basically same as a DRAM array as shown in Figure 11. An input activation \( I \) is converted into a differential input voltage \( V_{in} \) and shared across a row of MAC-DO cells using two WLs. Similarly, a weight \( W \) controls a capacitor bank (=Weight Block) added to a bit-line and \( A_i \), which is shared across a column through the bit-line. Thanks to these input and weight broadcasting, the MAC-DO array can calculate the outer product of two matrices \((I \times W)\) as explained in Section 2.3 and accumulate the results in the array for every cycle. For input and weight matrices with proper sizes, every MAC-DO cell inside the array can be engaged in an individual MAC operation without leaving an idle cell. Therefore, the
MAC-DO array architecture has a high utilization ratio of up to 100% and high throughput compared to bit-line charge-sharing-based accelerators [33, 34, 35].

3.5 Outer Product to a MAC-DO Array

Since each MAC result keeps accumulated in each MAC-DO cell, the MAC-DO array is controlled for an "output stationary" data flow [47, 48, 49]. For matrix by matrix multiplication, \( I(0) \sim I(i) \) and \( W(0) \sim W(j) \) matrices in Figure 6 are reshaped as an input matrix \( I \) and a weight matrix \( W \) as shown in Figure 12. Then, the two matrices perform outer product on the MAC-DO array. Each outer product multiplication result is mapped on the MAC-DO array and keeps accumulated in each MAC-DO cell for every computation cycle as explained in Section 3.3 like

\[
\sum OUT(i, j) = \sum_{k=0}^{C \times R \times R - 1} I(i)_k \times W(j)_k
\]

where \( i \) and \( j \) mean the row and column number of the MAC-DO array, respectively, and \( k \) means the \( N \)’th computation cycle. The outer product is completed after the \( C \times R \times R \) cycles, and every MAC-DO cell stores an individual MAC result simultaneously. With the matrix by matrix multiplication, MAC-DO can perform various convolution operations such as depth-wise convolution.

3.6 Reading out MAC Results

Since each MAC-DO cell in a MAC-DO array stores an individual MAC result at its two cell capacitors as a differential analog voltage, MAC-DO requires an analog to digital converter (ADC) to convert the analog MAC results into digital values for reading out. A row of differential ADCs used for quantizing the differential analog voltage is connected to the MAC-DO array through the corresponding BLs and quantizes the analog MAC results (Figure 13). Throughout the reading out process, only a row of the MAC-DO array involves in the ADC conversion at a time while other rows are deactivated. One of two WLs of the row is activated first and analog voltages stored at \( V_{ODS} \) nodes are sampled on a row of \( C_a \) capacitors and held (S/H). Next, the other WL is activated to sample the other part of differential voltages at \( V_{VNS} \) on a row of \( C_b \) capacitors for a differential pair. Lastly, each ADC quantizes each differential analog voltage sampled on two capacitors \( (C_a \) and \( C_b \) as shown in Figure 13. After a row of MAC results is read out, other rows go through the same readout process row by row. The ADC overheads such as area and cost are significantly increasing as ADC bit resolution grows [54]. However, the overheads would account for a small portion of MAC-DO’s overall overheads since MAC-DO targets low resolution inference. In addition, the overheads can be minimized by sharing one ADC with multiple BLs through multiplexers at the expense of longer readout latency.

3.7 Supporting Signed Number Operations

Signed input: Because an input activation is translated into a differential analog voltage, MAC-DO easily supports negative activation by flipping its polarity. This requires only a few additional switches as shown in Figure 14. The circuit is unchanged when \( S_1 \) switches are on. On the other hand, when \( S_2 \)s are on, the polarity of the differential input signal \( V_{in} \) is inverted inside the corresponding MAC-DO cells and a multiplication with negative input

\[
OUT = -I \times W
\]

occurs in the MAC-DO cells. This adds an extra sign bit for input and increases the bit precision.

Signed weight: The charge-steering circuit always discharges from the DRAM cell capacitors, so a MAC-DO cell itself cannot handle negative or zero weight data. Also, because of the innate tail capacitance offset arising from parasitic capacitors at the BL and capacitor bank, the weight term (W) in Equation (5) is biased and needs correction. In order to resolve both issues, a digital offset is added to weights before going into the array. So, the Equation (6) for MAC operation is modified as

\[
\sum OUT = \sum I \times (W + W_o + 2^{N-1})
\]

where \( W_o \) is the offset from parasitic capacitors, \( N \) is the weight bit-precision including a signed bit and \( 2^{N-1} \) is a digitally added value for shifting negative weights into positives.
4. MISMATCH CORRECTION METHODS

4.1 Mismatch Effect of MAC-DO Cells

Since every access transistor in a MAC-DO array performs analog MAC operations, the mismatch among the access transistors affects MAC operations in a real chip. As a result, outputs generated in two MAC-DO cells can be different even with the same input and weight data. In order to minimize such mismatch effects in MAC operations, three methods are used in MAC-DO circuit design and operation. First, the size of cell transistors is increased to reduce the mismatch. Even though this has largely increased the power consumption for driving cell transistors, it still maintains good energy efficiency. Secondly, the mismatch effect is further diminished by adopting a common centroid layout technique. For the common centroid layout, each MAC-DO cell is copied and placed symmetrically about both axes of symmetry x and y as shown in Figure 15. All the copied cells can be placed in a DRAM array without altering the original DRAM array structure. These copied cells are activated at the same time with the same data. For example, 4 cells of 'E' in Figure 15 are placed symmetrically inside a DRAM array and operate simultaneously. This technique may reduce the effect of spatial mismatch gradient with less cell area increase. Despite those two solutions for reducing the mismatch effect, it is not fully removed in reality. With the mismatch effect, the Equation (9) is expressed as

$$\sum OUT = \sum (I + I_m) \times (W + W_c) \quad (10)$$

where $I_m$ represents the offset mismatch of each MAC-DO cell. Thus, MAC-DO requires additional correction techniques to cancel the offset terms ($I_m$ and $W_c$) to acquire an actual MAC result, which is expressed as $\sum I \times W$.

4.2 Digital Correction

To get the desired MAC result $\sum I \times W$, the left and right sides of Equation (10) are transposed as

$$\sum I \times W = \sum OUT - I_m \sum W - W_c \sum I - \sum I_m W_c \quad (11)$$

so the offset effects included in $\sum OUT$ need to be subtracted to get the desired MAC result. The offset constants of $I_m$ and $W_c$ are obtained by applying the test data composed of '1' and '0' and by solving the equation above. For this correction, MAC-DO needs additional accumulations of input and weight data in digital domain, but its overhead is not critical in the entire system, since the offset constants can be reused once they are obtained and other accumulation results can also be shared across many cells in a row or column.

4.3 Analog Correction

In addition to the digital correction, MAC-DO can use an analog offset cancellation technique such as chopping. For this, MAC-DO performs an additional MAC operation with negated input and weight after a normal MAC cycle. The two MAC operation results, $OUT$ and $OUT'$, are

$$OUT = (I + I_m) \times (W + W_c)$$

$$OUT' = (-I + I_m) \times (-W + W_c), \quad (12)$$

and they add up to

$$OUT + OUT' = 2(I \times W + I_m \times W_c). \quad (13)$$

Therefore, the desired MAC result is expressed as

$$\sum I \times W = (\sum OUT + OUT' - \sum I_m W_c) / 2 \quad (14)$$

Now the MAC result has only one constant subtraction term that can be easily found and computed; It no longer requires accumulation of input nor weight data.

5. EVALUATION METHODOLOGY

5.1 Overall System Architecture for Testing MAC-DO

To verify the performance of MAC-DO, an overall system architecture including test circuits has been designed as shown in Figure 16. The test focuses on accelerating compute-intensive convolutions in inference which are the largest bottleneck in CNN layers (>90% computations, runtime). The MAC-DO for accelerating convolutions consists of five blocks: a MAC-DO array, a row controller, an R-string DAC block, a column controller, and an analog to digital converter (ADC) block.

For convolutions, input and weight data are stored outside of MAC-DO, which would be DRAM arrays. Those data go through a data-reshaping step and are prepared as a matrix form to perform the outer product like Figure 12. Then, the row controller receives the input matrix through input buffers and controls the R-string DAC to generate differential analog input voltages for corresponding rows of MAC-DO cells. The column controller receives the weight matrix through weight buffers and manipulates the tail switches of the capacitor banks in weight blocks. After a series of MAC operations
inside the array, the ADCs convert the differential analog output voltages stored at each MAC-DO cell into digital values row by row. Data pre-/post processing and running other layers such as pooling and activation are performed with the help of software using the host CPU because they are rather data-intensive and can be easily performed using conventional in-/near-DRAM processing techniques. We skip the detailed explanation of the software system because it is out of the scope of this paper.

5.2 Parameters of MAC-DO Circuits

Table 1: Design Parameters of MAC-DO Test Circuit

| Parameter                        | Value                  |
|----------------------------------|------------------------|
| Technology                       | 65nm CMOS logic process |
| Supply voltage ($V_{DD}$)        | 1.2V                   |
| Clock frequency                  | 12.5 MHz               |
| An access transistor size (W/L)  | 800/560 (nm)           |
| Cell capacitance                 | 100fF                  |
| Noise at cell capacitors         | 264.3μV, <0.13% error  |
| Each tail capacitance            | 6.8f~9.6f (f)          |
| A MAC-DO cell size               | 221.21 (μm²)           |
| An array size                    | 16 × 16                |
| Input/weight precision           | 4bit/4bit integer      |
| # of maximum MAC operations in a MAC-DO cell | 200                  |

MAC-DO has been simulated in transistor level by using Cadence Spectre Simulator [55] under a 65nm CMOS process. The MAC-DO array (16 x 16 MAC-DO cells or 32 x 16 1T1C DRAM cells), row controller (including switch blocks), R-string DAC and column controller have been designed in transistor level. For ADC analysis, we use data from a survey of recent ADC circuits [56] and scaled an ADC data to 65nm process, 1.2V supply voltage and 6bit output precision for fair comparison with other works. The test focuses on accelerating convolutions of a neural network. The 4bit quantized input and weight data at each convolution layer are extracted through PyTorch [57] and they are transferred into the Spectre simulator by using a Verilog-A block modeling a data bus [58]. After a simulation is finished, differential analog output voltages of the simulated array are directly observed. These are rather data-intensive and can be easily performed using conventional in-/near-DRAM processing techniques. We skip the detailed explanation of the software system because it is out of the scope of this paper.

5.3 Circuit Implementation

MAC-DO’s computation accuracy has been tested in the same way as [61] by measuring the Top-1 accuracy drops when MAC-DO performs MAC operations for a convolution layer of LeNet-5 [60] neural network for MNIST dataset [59]. Other layers such as non-linear function have been supported by using software. The detailed network parameters of LeNet-
Table 2: LeNet-5 Neural Network for Circuit Simulation

| Dataset       | MNIST [59] |
|---------------|------------|
| Network       | LeNet-5 [60] |
| Batch size    | 32         |
| Layers        | Network Parameters |
| Conv1(C1), BatchNorm, Tanh | Input Feature : 1 x 32 x 32, Weight Filter : 6 x 1 x 5 x 5 |
| Conv3(C3), BatchNorm, Tanh | Input Feature : 6 x 14 x 14, Weight Filter : 16 x 6 x 5 x 5 |
| Conv5(C5), BatchNorm, Tanh | Input Feature : 16 x 5 x 5, Weight Filter : 120 x 16 x 5 x 5 |
| FC1, Tanh     | Input Feature : 120 x 1, Weight Filter : 84 x 120 |
| FC2           | Input Feature : 84 x 1, Weight Filter : 10 x 84 |

Table 3: Benchmarking Top-1 Accuracy for MNIST Dataset in LeNet-5

| I/W precision | full-precision | 4b/4b | 3b/3b | 2b/2b |
|---------------|----------------|-------|-------|-------|
| Top-1 Accuracy| 99.075%        | 98.973%| 98.595%| 84.767%|

5 is shown in Table 2. In order for benchmarking, the LeNet-5 network for MNIST dataset is pre-trained with full precision operations and batch size 32 using PyTorch, and the Top-1 accuracy shows 99.075%. Also, a convolution layer in LeNet-5 has been digitally computed after 4bit, 3bit and 2bit quantization to compare with analog computation using MAC-DO. For these tests, the pre-trained network in full precision domain has been reused without retraining and a digital correction is performed using PyTorch. The accuracy for the each case is shown in Table 3.

6. EVALUATION RESULTS

6.1 Accuracy of Multiplication Results of A MAC-DO Cell

Figure 17 shows the accuracy of multiplication results of a MAC-DO cell. Figure 17-(a) shows the accuracy of repetitive MAC operations in a MAC-DO cell. For example, the plot with square markers shows the accumulation results ($V_{out}$) of a series of 15(I)×15(W) multiplications. Results with W = 0, show that non-zero multiplication results keep accumulating because of the weight offset arising from parasitic capacitors in weight blocks. However, this unwanted offset can be removed by aforementioned correction techniques. Figure 17-(b) shows the multiplication results for all 256(4b×4b) combinations of inputs and weights, after 50 times of accumulation in a MAC-DO cell. Figure 17-(c) and (d) shows the absolute (mV) and relative errors (%) of the data in Figure 17-(b) from the ideal values. The maximum error levels among the 256 results are 1.19mV and 4.06%, respectively. Table 4 shows the relative error after digital and analog correction with mismatch effects. Analog correction requires doubled MAC cycles but shows much better correction performance.

Figure 18: Area breakdown of MAC-DO architecture

The area of each block in the MAC-DO test circuit has been estimated based on the transistor-level circuit design and layout. The total area is estimated 0.0771mm² and Figure 18 shows the area breakdown. Currently, most of the area is for the 16×16 array (80.15%), mainly due to areas for cell capacitors. The area for the weight blocks accounts for 4.08% of the total area, which is also dominated by the tail capacitors. The area of switch blocks accounts for 4.23% and the area of row controller is 8.78% of the total area because of a lot of switches in row periphery. The overall area of the MAC-DO architecture can be further decreased by using DRAM technology. Also, the switch transistors in the row controller can be much smaller by using normally
sized access transistors (∼10× smaller even with common centroid cell mapping) in the array because smaller access transistors require less driving force for the switches.

6.3 Average Power Breakdown

![Average power breakdown of three convolution layers (C1, C3 and C5)](image)

Figure 19: Average power breakdown of three convolution layers (C1, C3 and C5)

Figure 19 shows the average power breakdown of the MAC-DO test circuit for running three convolution layers C1, C3 and C5 of LeNet-5. The total power for C1, C3 and C5 layers are 34.46 μW, 33.96 μW and 35.63 μW, respectively. The power consumption for precharging cell capacitors is dominant in the array power because MAC operations in MAC-DO are performed by discharging cell capacitors that were precharged once at the precharge phase. The array power consumption in the C1 layer is smaller than in the C3 and C5 layers because it requires the fewest accumulation cycles for a convolution (5×5 = 25 cycles). The R-DAC shows the largest power consumption in the MAC-DO test circuit because it drives a lot of big access transistors (∼40× bigger than usual), so it can be further reduced by optimizing the size of access transistors. In addition, since the size of a cell capacitor is smaller in actual DRAM process, the size of tail capacitors can also be scaled down, and so does the power consumption of the column controller (Col_C) and the MAC array in a real DRAM based chip.

6.4 Performance Analysis and Comparison

Figure 20 summarizes the performance numbers from the circuit simulation results of the MAC-DO test circuit on three convolution layers (C1, C3, C5) of LeNet-5. Figure 20-(a) shows the total energy consumption for executing an array operation (a part of convolution that fits in the 16 x 16 array). Figure 20-(b) shows the average array utilization (used MAC-DO cells / total MAC-DO cells) for each convolution layer, which marks high (∼ 93.75%) utilization except for the C1 layer with unusually few numbers of input and output channels (1 and 6, respectively). Figure 20-(c) shows the throughput in terms of images per second. Figure 20-(d) shows the energy efficiency (TOPS/W), where 1 MAC operation is regarded as 2 operations (1 multiply + 1 accumulate). Since C1 has the lowest array utilization, its energy efficiency is the lowest among the three layers. Figure 20-(e) shows inference time for a batch of images (=32 images). If a part of image data can be processed with the next image using scheduling, the array utilization can increase to 100% for C3 layer, because the number of its output channels (=16) is a multiple of the number of columns (=16) in the MAC-DO array. In this case (=C3*), the energy efficiency and inference time for a batch of images show 1.12× and 0.893× improvement over when without scheduling, respectively.

![Performance comparison among convolution layers](image)

Figure 20: Performance comparison among convolution layers

![Performance comparison at faster speeds](image)

Figure 21: Performance comparison at faster speeds

Figure 21 shows the performance summary for faster clock frequency settings. The throughput increases linearly to clock frequency because the time for precharging cell capacitors does not affect precharging numbers due to the small array size. Also, it shows better energy efficiency at faster speeds as excessive energy dissipation during too long evaluation periods is reduced, even though the average power is increased.

6.5 Performance Estimation for a Real DRAM Based Array

In this section, we estimate MAC-DO architecture’s performance when it is used with a real DRAM array size. The array size is scaled to a typical DRAM MAT size (256 × 512 MAC-DO cells, or 512 × 512 1T1C DRAM cells [64]). Our estimation is based on the average power breakdown of C3...
layer (Figure 19-(b)) and the size of cell capacitors and access transistors are unchanged. Then, we assume the average power is linear to the number of circuit blocks because most power dissipation is due to the dynamic power consumption, which is basically proportional to the size of parasitic capacitors. Overheads for controlling complicated row and column peripheral circuits are amortized over more number of MAC-DO cells, so the estimated performance of MAC-DO marks 2.22x energy efficiency improvement over the 16 × 16 test circuit (Table 5) with 3.26 TOPS of throughput over when the array size is 16 × 16.

6.6 Accuracy

The accuracy of MAC-DO analog computation results has been tested with C3 layer of LeNet-5. For the test, C3 convolution layer is executed by the MAC-DO test circuit using transistor-level simulation for 448 test set images from the MNIST dataset, and the Top-1 accuracy is calculated from the collection of the final results. Other layers have been executed with full precision using software in the similar way as [61]. In order to dequantize the analog MAC results, we use four images as training data to find proper dequantization parameters. The Top-1 accuracy is 97.07% with a standard deviation of 0.2507%, (without network retraining, the four images for training dequantization parameters are not included). To estimate an effective bit precision of this analog computing, the Top-1 accuracy is compared to the accuracy results when the same C3 layer only has been executed after quantization into 2-, 3-, 4-bit data (Table 3). The Top-1 accuracy drop of 1.903% from the MAC-DO analog computing is most similar to that of digital operation with 3-bit quantized data. The accuracy number can be further improved by retraining the LeNet-5 network with MAC-DO circuits or performing additional analog corrections.

6.7 Comparison with Other Works

Figure 22 compares the results with a common GPU and other accelerators [26, 31, 37, 38, 44, 62, 63], and Table 6 shows their baseline descriptions for the comparison. For fair comparison, we include ADC overheads estimated from [56] after scaling to 65nm process. We assume 16 ADCs (=# of columns) are used and each ADC area is 0.00116mm$^2$ with 0.89 (pJ) per 6bit conversions. The ADC overheads account for a small portion of MAC-DO’s performance because MAC-DO targets low-resolution inference in edge devices, reducing the ADC design complexity. Since MAC-DO array size is 16 × 16, the test chip has a low throughput, but in a real chip, it can be easily scaled to several TOPS as shown in Table 5. Figure 22-(a) compares computational density (GOPS/mm$^2$) with other works. MAC-DO shows 2.55x computational density improvement over a recent DRAM based AiM [37] thanks to high array utilization. In addition, the computational density will be further increased when MAC-DO is designed using DRAM technology. Figure 22-(b) shows that MAC-DO is at least minimum 29.7x more energy efficient than other compared works, even including SRAM based accelerators. Figure 22-(c) compares the FoM (energy efficiency(TOPS/W) × input precision × weight precision), and MAC-DO also marks the best with > 9.7x difference with previous works.

7. CONCLUSION

Recently presented in-DRAM accelerators can perform only simple logic operations because an efficient way to accelerate MAC operations suitable to DRAM technology has not been presented so far. Also, the energy efficiency and throughput of those previous works are limited because of low array utilization. To resolve this issue, MAC-DO performs analog multi-bit precision multiply-accumulate operations directly using the 1T1C DRAM array and can achieve 100% array utilization by exploiting a very compact, charge-steering based analog multiplication mechanism. MAC-DO’s core MAC operation happens inside each 2T2C MAC-DO cell and does not involve complex digital circuits so it is well suited to DRAM technologies. The output stationary data flow allows easy task mapping on the MAC-DO array and efficient data reuse for all types of data, leading to the improvement of throughput and energy efficiency for most convolution lay-
ers. Thanks to the high array utilization, MAC-DO shows $>2.55 \times$ higher computational density than previous in-DRAM accelerators and $>29.7 \times$ energy efficiency and $>9.7 \times$ over all compared accelerators.

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