Hybrid Three-Phase Transformer-Based Multilevel Inverter with Reduced Component Count

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ABSTRACT This paper proposes a novel three-phase transformer-based multilevel inverter (MLI) topology to maximize the output voltage levels for high-power high-voltage applications while reducing component counts as compared to its transformer-based counterparts. The proposed hybrid topology is formed by connecting a three-level T-type module with full H-bridge cells through single-phase transformers. The T-type module is fixed while the full H-bridge cell can be repeated for enlarging the output voltage levels without increasing the voltage stress on switches. Key features of the proposed topology include low part count, capacitor-free, diode-free, voltage boosting, simple control, and modularity. Within the framework, a simple low-frequency pulse width modulation (LFPWM) switching scheme is used to control the output voltage, and the working principle is detailed for seven-, nine-, and N-level operation. The operability and performance of the proposed topology are numerically verified and experimentally validated at different loads. Moreover, its conversion efficiency is experimentally examined. Finally, a comparative study with existing transformer-based MLI circuits is conducted to prove its key merits.

INDEX TERMS Cascaded-transformer multilevel inverter (CTMI), DC-AC converter, hybrid multilevel inverter (MLI), multilevel inverter topology.

I. INTRODUCTION

Multilevel inverters (MLIs) concept has become a mature technology, being deployed in medium- and high-power DC-AC conversions. The MLIs have gained popularity due to their unique merits of producing high voltages at high quality, namely low THD value, low dv/dt, low electromagnetic interference (EMI), high conversion efficiency, voltage scalability, and reliability while using low-voltage semiconductor devices and low switching frequency [1-5]. The conventional MLIs include three topologies, being known as cascaded H-bridge (CHB) [6], neutral point clamped (NPC) [7, 8], and flying capacitor (FC) [9, 10]. The CHB, NPC, and FC MLIs can produce output voltages with N levels, requiring huge counts of DC sources, clamping diodes, and capacitors, respectively. For example, producing nine-level three-phase voltages requires 48 switches, twelve DC sources in CHB inverters, 168 clamping diodes in NPC inverters, and 92 capacitors in FC inverters, increasing inverter size, cost, losses, failure rate, and complexity. As argued in [11], increasing the number of voltage levels is a desirable necessity to enhance the MLI performance. Therefore, many MLIs are intensively developed to increase the output voltage levels with reduced component counts [11-22]. Among them, transformer-based MLIs have received great attention with key features of reducing DC source count and maximizing the output voltage [18-22]. Their structure, merits and demerits are briefly discussed hereafter.

The cascaded-transformer multilevel inverter (CTMI) in [18] comprises two stages: voltage generator stage (VGS) and polarity changer stage (PCS). Half-bridge modules are the building block in the VGS, thus adding more half-bridge modules enlarges the voltage level count. The PCS employs full H-bridges to bipolarize the generated unipolar multilevel voltages from the VGS stage. Producing three-phase voltages requires three single-phase transformers to couple the PCS outputs with the load. This CTMI requires three power
transformers, \(3N+9\) switches, and \(0.5N-0.5\) DC voltage sources for generating \(N\) voltage levels. It can eliminate flying capacitors, clamping diodes and reduce the DC source count as compared to FC, NPC, and CHB inverters, respectively. However, using three H-bridge cells to produce bipolar voltages is a conspicuous drawback because of linking the switch blocking voltage to the output voltage level count. For example, the total standing voltage of PCS switches is \(6V_{\text{DC}}(N-1)\), where \(V_{\text{DC}}\) is the voltage rating of each DC source in the DC-link, limiting the modularity of this CTMI and other associated features such as THD and dv/dt.

To tackle the drawbacks of the CTMI in [18], a hybrid nine-level inverter (H9LI) is proposed in [19], which can produce bipolar voltages without a polarity changer with a lower part count. It employs twenty-four switches, nine capacitors, six power diodes, one DC source, and three single-phase transformers. It saves twelve switches and three DC sources as compared to the CTMI when producing nine-level voltages. However, the reduction of DC sources and switches requires higher numbers of power diodes and capacitors, decreasing the inverter efficiency, reliability, and life span. Further, during startup, the H9LI requires pre-charging circuits for three capacitors, as suggested by the authors in [19].

To reduce or eliminate capacitors in the H9LI, two transformer-based topologies were presented in [21, 22]. The modified active-neutral point-clamped (MANPC) topology in [21] uses thirty switches, five capacitors, three single-phase transformers, and one DC source to produce nine voltage levels. The MANPC topology has a lower part count than H9LI in [19]. Both circuits use the same count of transformers and DC sources, but MANPC topology eliminates the six power diodes in H9LI. Further, it uses only five capacitors instead of nine in H9LI, simplifying control algorithms and improving inverter reliability. However, using additional six switches is a disadvantage of the MANPC as compared to the H9LI. A transformer-based cascaded H-bridge (TB-CHB) topology in [22] can reduce the switch count to only twenty-four, being the same switch count as H9LI, and lower than MANPC by six switches. Furthermore, it can remove all capacitors in MANPC and H9LI inverters. For constructing each inverter leg in the TB-CHB topology, several full H-bridge cells sharing a single DC-link are cascaded through single-phase transformers. A nine-level operation, it requires one DC source, twenty-four switches, and six single-phase transformers. Modularity, capacitor-free, diode-free, and reduced switch count are its key merits. However, using six transformers is the main drawback, increasing the size and cost of the inverter.

To address the disadvantages of the aforementioned transformer-based inverters, namely high counts of DC sources in CTMI [18], power diodes and capacitors in H9LI [19], switches in MANPC [21], or transformers in TB-CHB [22], this study proposes a novel three-phase transformer-based MLI topology, which can reduce the total part count while preserving the key features of being capacitor-free, diode-free, and low counts of DC sources, switches, and transformers. Further, the proposed circuit allows for increasing the voltage level count without increasing the voltage stress across the switches, being a good option for high-power high-voltage applications. This MLI topology is proposed as part of work carried out for the research in [23].

Section II details the working principle, symmetrical and asymmetrical operation modes, generalized configuration of the proposed topology, and suggests its applications. A switching modulation scheme based on low-frequency pulse width modulation (LFPWM) is given in Section III. Section IV presents and discusses the simulation and experimental verification of the proposed inverter. A comparative assessment between the proposed topology and recently developed transformer-based inverters is drawn in Section V. Finally, Section VI concludes the finding of this paper.

II. PROPOSED TRANSFORMER-BASED MLI TOPOLOGY

A. CIRCUIT CONFIGURATION

The circuit configuration of the proposed transformer-based inverter is shown in Fig. 1. It is a hybrid three-phase topology, being formed by connecting three T-type legs to three H-bridge inverters through three single-phase transformers. The proposed topology consists of two DC sources \(E_1\) and \(E_2\), three transformers \(T_A, T_B, \) and \(T_C\), and twenty-four switches \((S_{1A}-S_{12})\). The twenty-four switches are used to implement eighteen unidirectional switches and three bidirectional switches. The proposed topology does not require any clamping diodes or flying capacitors in its operation. It can produce different voltage level counts \(N\), according to the selected transformer turns ratio \(\beta\). For example, it produces seven voltage levels and nine voltage levels when selecting \(\beta\) to be 1 and 1.5, respectively. The proposed topology configuration keeps the maximum blocking voltage of the switches either below or equal to \(E\), where \(E\) is the input DC-link voltage. The switches \(S_1, S_{11}, S_{12}, S_{19}\), and \(S_{20}\) have a voltage stress of \(0.5E\). Alternatively, the switches \(S_1, S_2, S_3-S_{10}, S_{13}-S_{18}\), and \(S_{21}-S_{24}\) withstand a voltage stress of \(E\).

B. OPERATING CONCEPT

The operating concept can be explained based on the pole voltage generation. The pole voltages are the voltage differences between the three load points \((A, B, \) and \(C)\) and the reference point \(0\), being labelled as \(V_{A0}, V_{B0}, \) and \(V_{C0}\), respectively. Considering \(V_{A0}\) as an example, it is synthesized by adding two voltage components: \(V_0\) and \(V_1\), as shown in (1) and Fig. 2. The \(V_0\) is the voltage between the midpoint of the T-type leg and the reference point \(0\), and \(V_1\) is the secondary voltage of transformer \(T_A\). Both two voltage components can have three different voltage levels, \(V_0\) has \(0.5E, 0, -0.5E\), and \(V_1\) has three levels of \(\beta E, 0, \) and \(-\beta E\). \[
V_{A0} = V_0 + V_1 \tag{1}
\]

The transformer turns ratio \(\beta\) can have different values: A) Case A, \(\beta =1\), producing three voltage levels of \(E, 0, \) and \(-E\) in
the voltage component \( V_1 \), B) Case B, \( \beta = 1.5 \), producing three voltage levels of \( 1.5E, 0 \), and \(-1.5E \) in \( V_1 \). Although both cases keep producing the same number of voltage levels, the maximum reachable voltage in the case B is higher than that in the case A. Accordingly, the pole voltage can have different voltage level counts: seven levels in the case A (i.e., \( 1.5E, E, 0.5E, 0, -0.5E, -E \), and \(-1.5E \)) and nine levels for the case B (i.e., \( 2E, 1.5E, E, 0.5E, 0, -0.5E, -E, -1.5E \), and \(-2E \)).

Fig. 3 shows seven different operating modes of the proposed topology to produce seven voltage levels in the pole voltage \( V_{A0} \) when \( \beta \) is equal to 1. For instance, in Fig. 3 (a), mode I describes the required ON/OFF switches for producing \( 1.5E \) in \( V_{A0} \), in which the switches \( S_1, S_4, S_5, \) and \( S_8 \) must be ON while \( S_2, S_3, S_6, \) and \( S_7 \) are OFF. The remaining six voltage levels can be achieved by following the operating modes II to VII, as shown in Figs. 3(b) to (g), respectively. It is worth noting that the mentioned operating modes are selected to produce the targeted voltage level without causing a short-circuit across the input DC sources. Therefore, some combination of switches cannot be set ON. For example, in phase leg A, the following combinations are not used in the modulation control of the proposed topology: \( (S_i, S_j) \), \( (S_i, S_k, S_l) \), \( (S_2, S_3, S_4) \), \( (S_5, S_6, S_7) \), and \( (S_7, S_8) \).

C. N-LEVEL CONFIGURATION

The proposed topology can be extended to produce \( N \) voltage levels by adding more H-bridge cells in each phase leg, being connected through transformers, as shown in Fig. 4. The blocking voltage of the switches is not a function of the voltage levels count, so increasing the voltage level count does not increase the voltage stress across the switches. All H-bridge cells contribute to the pole voltage. For example, the pole voltage \( V_{A0} \) is synthesised by adding all the cell voltages \( V_1 \), \( V_2 \), …, and \( V_6 \) to the base voltage \( V_0 \) as expressed in (2).

\[
V_{A0} = V_0 + \sum_{i=1}^{6} V_i
\]  

(2)

The \( N \)-level configuration of the proposed inverter generates different voltage level counts according to the transformer turn ratio \( \beta \) while keeping the same component count. The generalized configuration has three cases, depending on \( \beta \): A) symmetrical turns ratio (where \( \beta_1 = \beta_2 = \ldots = \beta_n = 1 \), B) asymmetrical binary turns ratio (where \( \beta_1, \beta_2, \beta_3, \ldots \) are 1, 2, 4, …), C) asymmetrical ternary turns ratio (where \( \beta_1, \beta_2, \beta_3, \ldots \) are 1.5, 4.5, 13.5,…). The relationships between the transformer count \( N_{\text{trf}} \), switch count \( N_{\text{SW}} \), and the voltage level count \( N \) are presented in (3-4), (5-6), and (7-8), for symmetrical, binary asymmetrical, and ternary asymmetrical turn ratios, respectively. For example, using six transformers (two per phase leg) produces eleven, fifteen, twenty-seven voltage levels in the pole voltage for symmetrical, binary asymmetrical, ternary asymmetrical turn ratios, respectively. The component counts in (3)-(8) represent the total count in the three legs.

1) SYMMETRICAL RATIOS: \( \beta_1 = \beta_2 = \ldots = \beta_n = 1 \)

\[
N = \frac{4N_{\text{trf}}}{3} + 3
\]

(3)

\[
N_{\text{SW}} = 3N + 3
\]

(4)

2) ASYMMETRICAL BINARY RATIOS: \( \beta_1, \beta_2, \beta_3, \ldots \) are 1, 2, 4, …

\[
N = \frac{N_{\text{trf}} + 1}{3}
\]

(5)

\[
N_{\text{SW}} = 12 \left( \frac{\ln(N+1) - 1}{\ln(2)} \right)
\]

(6)

\[
N_{\text{trf}} = 3 \left( \frac{\ln(N+1) - 2}{\ln(2)} \right)
\]

(7)

(8)
3) **ASYMMETRICAL TERNARY RATIOS:** $\beta_1, \beta_2, \beta_3, \ldots$ are 1.5, 4.5, 13.5, \ldots

$$N = \frac{3^{\frac{N_{SW}}{\ln(3)}}}{3^{\frac{N_{Trf}}{\ln(3)}}}$$

$$N_{SW} = 12 \left( \left\lfloor \frac{\ln(\frac{N}{3})}{\ln(3)} \right\rfloor + 1 \right)$$

$$N_{Trf} = 3 \left( \left\lfloor \frac{\ln(\frac{N}{3})}{\ln(3)} \right\rfloor + 1 \right)$$

The H-bridge cells can enlarge the output voltage level count and the output power without increasing the switches blocking voltage. Therefore, from application point of view, the proposed circuit is best suitable for high-power high-voltage applications, in which the component count and inverter footprint are more important than the isolation feature. Other recommended applications for the proposed topology are in constant-frequency applications, including dynamic voltage restorers (DVR), uninterruptible power supplies (UPS), etc. To avoid transformer saturation, like in other transformer-based MLI, the proposed topology is not suitable for applications where a wide range of frequencies is required, such as motor drives with wide speed ranges.


III. MODULATION STRATEGY

The low-frequency pulse width modulation (LFPWM) scheme is selected to control the proposed topology output voltage due to its simplicity. However, other modulation schemes can be used as well, and selecting the best modulation is outside the scope of this study. Table I lists the switching states when $\beta$ is 1, generating seven voltage levels in the pole voltage. Alternatively, nine voltage levels are generated when $\beta$ is 1.5, as described in Table II. The LFPWM scheme is based on these two tables. Moreover, Tables I and II list the switching states of leg-A switches ($S_1$-$S_6$) and the corresponding output voltages $V_o$, $V_1$, and $V_{so}$.

Fig. 5 shows the generation of the switching signals for the leg-A switches when $\beta$ is 1. To produce the seven-level pole voltage as shown in the last trace of Fig. 5, a sinusoidal reference signal $V_{refA}$ and six offset signals ($\pm R_1$, $\pm R_2$, and $\pm R_3$) are required. The reference signal can be varied from 0 to the maximum of $V_T$, while the offset signals can be expressed as in (9) [16].

\[
\pm R_1 = V_p \sin(\theta_1), \\
\pm R_2 = V_p \sin(\theta_2), \\
\pm R_3 = V_p \sin(\theta_3)
\]

(9)

where $\theta_1$-$\theta_3$ are the transition angles between voltage levels as marked in the pole voltage waveform in Fig. 5. These transition angles can be calculated using (10) [16]. Further, equation (10) can be used for computing the transition angles of any number of voltage level produced by the $N$-level configuration in Fig. 4. In other words, Fig. 5 can be extended for producing the required switching pulses for $N$ voltage levels by using (10) to determine $N$-1 offset signals ($\pm R_1$, $\pm R_2$, $\pm R_3$, ...and $\pm R_{(N-1)2}$).

\[
\theta_m = \sin^{-1} \left( \frac{2m - 1}{N} \right) \\
m = 1, 2, ..., \frac{N-1}{2},
\]

(10)

Six primary signals ($X_1$-$X_6$) are derived when comparing the reference signal $V_{refA}$ with six offset signals. These six primary signals are the inputs for the Boolean operators in (11)-(14), being used to achieve the switching states in Table I.

\[
S_1, \overline{S_1} = X_1 + (\overline{X}_3 \times X_4) \\
S_2, \overline{S_2} = X_4 + (\overline{X}_3 \times X_6)
\]

(11)

(12)

| TABLE I | OUTPUT VOLTAGES AND THE CORRESPONDING SWITCHING STATES WHEN $N$ IS 1: LEG A |
|---------|--------------------------------------------------------------------------|
| $S_1$  | $S_2$  | $S_3$  | $S_4$  | $S_5$  | $S_6$  | $V_o$  | $V_1$  | $V_{so}$ |
| 1      | 0      | 0      | 1      | 1      | 1      | 0.5E   | E      | 1.5E     |
| 0      | 0      | 1      | 1      | 1      | 0      | 0.5E   | 0      | E        |
| 1      | 0      | 0      | 1      | 0      | 1      | 0.5E   | 0      | 0.5E     |
| 1      | 0      | 0      | 1      | 1      | 0      | 0.5E   | 0      | 0.5E     |
| 0      | 1      | 1      | 0      | 1      | 0      | -0.5E  | E      | 0.5E     |
| 0      | 0      | 1      | 1      | 1      | 0      | 0      | 0      | 0        |
| 0      | 0      | 1      | 1      | 0      | 1      | 0      | 0      | 0        |
| 0      | 1      | 1      | 0      | 1      | 1      | 0      | -0.5E  | -E       |
| 0      | 1      | 1      | 0      | 1      | 1      | 0      | -0.5E  | -E       |
| 0      | 0      | 1      | 1      | 0      | 1      | 0      | -0.5E  | -E       |
| 0      | 0      | 1      | 1      | 0      | 1      | 0      | -0.5E  | -E       |
| 1=ON, 0=OFF |

| TABLE II | OUTPUT VOLTAGES AND THE CORRESPONDING SWITCHING STATES WHEN $N$ IS 1.5: LEG A |
|----------|-----------------------------------------------------------------------------|
| $S_1$   | $S_2$  | $S_3$  | $S_4$  | $S_5$  | $S_6$  | $V_o$  | $V_1$  | $V_{so}$ |
| 1      | 0      | 0      | 1      | 1      | 0      | 0      | 0.5E   | 1.5E     |
| 0      | 0      | 1      | 1      | 1      | 0      | 0      | 1.5E   | 1.5E     |
| 0      | 1      | 1      | 0      | 1      | 0      | 1      | 0.5E   | 1.5E     |
| 1      | 0      | 0      | 1      | 1      | 1      | 1      | 0.5E   | 0.5E     |
| 0      | 0      | 1      | 1      | 1      | 0      | 1      | 0.5E   | 0.5E     |
| 0      | 0      | 1      | 1      | 1      | 1      | 0      | 0      | 0        |
| 0      | 1      | 1      | 0      | 1      | 1      | 0      | -0.5E  | -E       |
| 0      | 1      | 1      | 0      | 1      | 1      | 0      | -0.5E  | -E       |
| 0      | 0      | 1      | 1      | 0      | 1      | 1      | -0.5E  | -E       |
| 0      | 0      | 1      | 1      | 0      | 1      | 1      | -0.5E  | -E       |
| 0      | 1      | 1      | 0      | 1      | 1      | 0      | -0.5E  | -E       |
| 0      | 1      | 1      | 0      | 1      | 1      | 0      | -0.5E  | -E       |
| 0=ON, 0=OFF |

![FIGURE 5] Switching signals generation and the leg-A pole voltage $V_o$ when producing seven voltage levels at $\beta$ of 1.
\[ S_x, S_y = X_z \] (13)

\[ S_x, S_y = X_z \] (14)

The required switching signals for producing nine voltage levels in the pole voltages can be generated by using the same procedures as described in Fig. 5. In this case, eight offset signals are used instead of six. Comparing the eight offset signals and the modulation signals produces eight primary signals \( Y_1-Y_8 \). The adequate switching signals are derived by applying the Boolean operations in (15)-(18) on \( Y_1-Y_8 \) signals. In (11)-(18), symbols "+" and "\( \times \)" correspond to the logical operators "OR" and "AND", respectively.

\[ S_1, S_2 = (Y_5 \times Y_3) + (Y_3 \times Y_1) \] (15)

\[ S_1, S_2 = (Y_5 \times Y_3) + (Y_3 \times Y_1) \] (16)

\[ S_3, S_4 = Y_5 \] (17)

\[ S_3, S_4 = Y_5 \] (18)

IV. SIMULATION AND EXPERIMENTAL VALIDATION

This section presents a numerical verification and experimental validation of the proposed topology. The circuit configuration in Fig. 1 is used to evaluate the circuit operation, and Table III lists the used system parameters in simulation and experimental tests. Fig. 6 shows the experimental setup, consisting of two programmable DC voltage sources (Chroma, 62024P-100-50), one DC source for control circuits (Rohde & Schwarz, HMP4040), three single-phase transformers (Triad Magnetics, VPM240-20800), dSPACE MicroLabBox controller, current and voltage probes, digital oscilloscope (Yokogawa, DL850EV), resistive-inductive loads, and the inverter prototype. The inverter prototype is constructed using twenty-four IGBT modules (SEMIKRON, SKM300GA12E4) associated with gate-driver boards (SEMIKRON, SKHI 10/12 R).

A. SIMULATION RESULTS

The transformer turns ratio \( \beta \) affects the output voltage level count. The proposed inverter can produce seven and nine voltage levels at \( \beta \) of 1 and 1.5, respectively. Figs. 7-10 show the voltage waveforms of the proposed inverter when changing the turns ratio \( \beta \) from 1 to 1.5. Figs. 7(a) and 9(a) illustrate the synthesized pole voltage \( V_{AB} \), being obtained by adding \( V_I \) to \( V_o \). Figs. 7(b) and 9(b) show the three pole voltages \( V_{AB}, V_{BC}, \) and \( V_{CA} \), respectively. The output line voltages \( V_{AB}, V_{BC}, \) and \( V_{CA} \), are presented in Figs. 7(c) and 9(c). Fig. 7(c) shows that the line voltages can have fourteen different voltage levels of 0, ±0.5\( E \), ±1.5\( E \), ±2\( E \), ±2.5\( E \), and ±3\( E \) at \( \beta \) of 1. Alternatively, when \( \beta \) is 1.5, seventeen voltage levels of 0, ±0.5\( E \), ±1.5\( E \), ±2\( E \), ±2.5\( E \), ±3\( E \), ±3.5\( E \), and ±4\( E \) are generated in the line voltages as depicted in Fig. 9(c). The depicted line voltages in Fig. 9(c) have better THD than those in Fig. 7(c) because of having a lower level count, the THD value is 7.14% instead of 8.52%. Further, Figs. 8(a) and 10(a) show the load currents when connecting a resistive load (R) of 50 \( \Omega \) to the inverter outputs, where the line voltage \( V_{AB} \), phase voltage \( V_{AN} \), and load current \( I_{AN} \) appear in the first, second, and the third trace, respectively. Figs. 8(b) and 10(b)

| TABLE III | EXPERIMENTAL SYSTEM SPECIFICATIONS |
|-----------|-----------------------------------|
| Description | Value | Unit |
| DC-link voltage (\( E \)) | 100 | V |
| Load resistor (R) | 50 | \( \Omega \) |
| Load inductor (L) | 100 | mH |
| Output frequency (\( f_o \)) | 50 | Hz |
| Sampling frequency (\( f_s \)) | 50 | kHz |
| Number of transformers (\( N_{Trf} \)) | 3 | – |

![FIGURE 6 Experimental setup of the proposed topology.](image)
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show the waveforms of $V_{AB}$, $V_{AN}$, and $I_{AN}$ when feeding power to a resistive-inductive (R-L) load ($R=50\ \Omega$ and $L=100\ \text{mH}$).

**B. EXPERIMENTAL RESULTS**

The simulation findings are experimentally validated by the in-house inverter prototype in Fig. 6. The proposed topology is tested with one case of $\beta$ ($\beta=1$) since we do not have transformers with a turn ratio of 1.5. All the remaining parameters are kept as same as in the simulation verifications. Fig. 11(a) presents the leg-A pole voltage $V_{A0}$ and its two voltage components $V_{0}$ and $V_{1}$. By setting 100 V as the input voltage of the inverter ($E$), the waveforms of $V_{0}$ and $V_{1}$ have voltages of (0 and $\pm 50\ \text{V}$) and (0 and $\pm 100\ \text{V}$), respectively, resulting in a seven-level pole voltage as shown in the first trace of Fig. 11(a). Further, Fig. 11(b) shows the seven-level pole voltages of the three inverter legs $V_{A0}$, $V_{B0}$, and $V_{C0}$. These pole voltages having phase shifts of 120° produce three balanced line voltages of thirteen levels, as depicted in Fig. 11(c). Figs. 12(a) and (b) provide the obtained results when connecting resistive and resistive-inductive loads to the inverter outputs, respectively. The experimental results well validate and confirm the simulations and theoretical analysis of the proposed topology.

The efficiency of the proposed topology is measured experimentally. Fig. 13 shows the obtained values at different output powers while keeping all other system parameters constant. The efficiency increases from 92.69% to 97.76% when increasing the load power from 0.2 KW to 1.5 KW in a step of 0.1 KW. Using low frequencies ($\leq 150\ \text{Hz}$) in the employed switching scheme reduces switching losses and increases the overall efficiency.
The proposed topology is compared to recent developed transformer-based MLIs at nine-level operation in this section. The proposed topology aims to maximize the output voltage level count while reducing the required components. Therefore, a quantitative comparison is carried out between the transformer-based counterparts and the proposed topology based on component counts: namely DC voltage source count \(N_{DC}\), transformer count \(N_{Trf}\), switch count \(N_{SW}\), power diode count \(N_{D}\), and capacitor count \(N_{Cap}\).

For a fair comparison, the following aspects are considered:

A) generating nine levels in the three pole voltages. B) synthesizing pole voltages \(V_{A0}, V_{B0}, V_{C0}\), and \(V_{A0}\), \(V_{B0}\), and \(V_{C0}\), and \(V_{AB}, V_{BC}, \) and \(V_{CA}\).

V. COMPARATIVE ASSESSMENT OF THE PROPOSED TOPOLOGY

The proposed topology is compared to recent developed transformer-based MLIs at nine-level operation in this section. The proposed topology aims to maximize the output voltage level count while reducing the required components. Therefore, a quantitative comparison is carried out between the transformer-based counterparts and the proposed topology based on component counts: namely DC voltage source count \(N_{DC}\), transformer count \(N_{Trf}\), switch count \(N_{SW}\), power diode count \(N_{D}\), and capacitor count \(N_{Cap}\).

For a fair comparison, the following aspects are considered:

A) generating nine levels in the three pole voltages. B)
TABLE IV

| Topology | $N_{DC}$ | $N_{C}$ | $N_{SW}$ | $N_{D}$ | $N_{Tr}$ |
|----------|----------|---------|----------|---------|---------|
| $T_1$ [18] | 4 | 0 | 0 | 0 | 0 |
| $T_2$ [19] | 0 | 0 | 1 | 0 | 0 |
| $T_3$ [20] | 0 | 0 | 1 | 2 | 0 |
| $T_4$ [21] | 0 | 0 | 1 | 2 | 0 |
| Proposed MLI | 2 | 0 | 0 | 0 | 0 |

* The applied voltage across the primary windings, the load current is assumed to be the same for all topologies.

VI. CONCLUSION

This paper proposes a novel three-phase transformer-based nine-level inverter with a reduced component count, having the key features of being capacitor-, diode-free, and low counts of DC sources, switches, and transformers. The proposed circuit can increase the voltage level count to $N$ levels without increasing the voltage stress across the switches, being a promising candidate for high-power high-voltage applications. Further, it has beneficial features of modularity, voltage boosting and simple structure. The working principle of the proposed topology was theoretically demonstrated, numerically verified, and experimentally validated through the in-house setup. Finally, the advantages of the proposed topology, in terms of component counts, are highlighted by a comparative study.

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REFERENCES

[1] P. R. Bana et al., “Recently developed reduced switch multilevel inverter for renewable energy integration and drives application: topologies, comprehensive analysis and comparative evaluation,” IEEE Access, vol. 7, pp. 54888-54909, 2019.
[2] M. Vijej et al., “A general review of multilevel inverters based on main submodules: structural point of view,” IEEE Transactions on Power Electronics, vol. 34, no. 10, pp. 9479-9502, 2019.
[3] M. N. Raju et al., “Modular multilevel converters technology: a comprehensive study on its topologies, modelling, control and applications,” IET Power Electronics, vol. 12, no. 2, pp. 149-169, 2019.
[4] A. Salem et al., “Voltage source multilevel inverters with reduced device count: topological review and novel comparative factors,” IEEE Transactions on Power Electronics, vol. 36, no. 3, pp. 2720-2747, 2021.
[5] H. P. Venuganti et al., “A survey on reduced switch count multilevel inverters,” IEEE Open Journal of the Industrial Electronics Society, vol. 2, pp. 80-111, 2021.
[6] R. H. Baker and L. H. Bannister, “Electric power converter,” U. S. Patent 3867643, 1975.
[7] R. H. Baker, “Switching circuit,” U. S. Patent 4210826, 1980.
[8] A. Nabae, I. Takahashi, and H. Akagi, “A new neutral-point-clamped PWM inverter,” IEEE Transactions on Industry Applications, vol. IA-17, no. 5, pp. 518-523, 1981.
[9] T. A. Meynard and H. Foch, “Multi-level conversion: high voltage choppers and voltage-source inverters,” in Proc. 23rd Annu. IEEE Power Electron. Spec. Conf., 1992, pp. 397-403.
[10] J. P. Lavieille, P. Carrere, and T. Meynard, “Electronic circuit for converting electrical energy, and a power supply installation making use thereof,” U. S. Patent 5 668 711, 1997.
[11] C. Phanikumar, J. Roy, and V. Agarwal, “A hybrid nine-level, 1-phase grid connected multilevel inverter with low switch count and innovative voltage regulation techniques across auxiliary capacitor,” IEEE Transactions on Power Electronics, vol. 34, no. 3, pp. 2150-2170, 2019.
[12] S. Pal et al., “A cascaded nine-level inverter topology with T-type and H-bridge with increased DC-bus utilization,” IEEE Transactions on Power Electronics, vol. 36, no. 1, pp. 285-294, 2021.
[13] K. Wang et al., “Topology and capacitor voltage balancing control of a symmetrical hybrid nine-level inverter for high-speed motor drives,” IEEE Transactions on Industry Applications, vol. 53, no. 6, pp. 5563-5572, 2017.
[14] A. Edpuganti and A. K. Rathore, “Optimal low switching frequency pulsewidth modulation of nine-level cascade inverter,” *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 482-495, 2015.

[15] A. M. Mahfuz-Ur-Rahman et al., “Model predictive control for a new magnetic linked multilevel inverter to integrate solar photovoltaic systems with the power grids,” *IEEE Transactions on Industry Applications*, vol. 56, no. 6, pp. 7145-7155, 2020.

[16] N. Sandeep and U. R. Yaragatti, “A switched-capacitor-based multilevel inverter topology with reduced components,” *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5538-5542, 2018.

[17] B. S. Naik et al., “A hybrid nine-level inverter topology with boosting capability and reduced component count,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 1, pp. 316-320, 2021.

[18] M. M. Hasan, A. Abu-Siada, and M. S. A. Dahidah, “A three-phase symmetrical DC-link multilevel inverter with reduced number of DC sources,” *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8331-8340, 2018.

[19] W. Lin et al., “Hybrid nine-level boost inverter with simplified control and reduced active devices,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 2, pp. 2038-2050, 2021.

[20] S. N and U. R. Yaragatti, “Design and implementation of active neutral-point-clamped nine-level reduced device count inverter: an application to grid integrated renewable energy sources,” *IET Power Electronics*, vol. 11, no. 1, pp. 82-91.

[21] N. Sandeep and U. R. Yaragatti, “Operation and control of a nine-level modified ANPC inverter topology with reduced part count for grid-connected applications,” *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4810-4818, 2018.

[22] J. Lee et al., “Combination analysis and switching method of a cascaded H-bridge multilevel inverter based on transformers with the different turns ratio for increasing the voltage level,” *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4454-4465, 2018.

[23] A. M. S. Ali, “Multilevel inverters with reduced component count for energy systems,” Ph.D. Dissertation, Faculty of Engineering and Science, University of Agder, Grimstad, 2021. Accessed on: February 25, 2022. [Online]. Available: https://uia.brage.unit.no/uia-xmflui/handle/11250/2787318.