Fast Encoding and Decoding of Flexible-Rate and Flexible-Length Polar Codes

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Abstract—This work is on fast encoding and decoding of polar codes. We propose and detail 8-bit and 16-bit parallel decoders that can be used to reduce the decoding latency of the successive-cancellation decoder. These decoders are universal and can decode flexible-rate and flexible-length polar codes. We also present fast encoders that can be used to increase the throughput of serially-implemented polar encoders.

Index Terms—Polar codes, domination contiguity, maximum a posteriori, maximum likelihood, minimum distance, systematic codes, non-systematic codes.

I. INTRODUCTION

POLAR codes are capacity-achieving block codes that are recently introduced by Arıkan [1]. Due to their provable capacity-achieving performance with low-complexity encoding and decoding, they have gained significant interest [2], [3]. In particular, polar codes can be encoded and decoded in a recursive fashion, which results in encoding and decoding complexities of $O(N \log_2 N)$, where $N$ is the code length [1].

One of the main challenges associated with polar codes is their high decoding latency and low throughput [2], [4]. Since the serial nature of decoding bottlenecks fast implementation of polar coding, researchers have introduced novel ways to reduce the decoding time [2]–[6]. For example, [5] introduces the notion of rate-zero and rate-one nodes to reduce the decoding depth of the successive cancellation (SC) decoder. The resulting simplified SC (SSC) decoder reduces the decoding latency up to 20 times [6]. The decoding latency can further be improved by identifying single-parity-check (SPC), repetition (REP) and REP-SPC nodes in the decoding tree of polar codes and implementing their fast decoders [2].

The key idea behind the above-mentioned strategies is to increase the decoding speed by reducing the decoding depth and implementing fast parallel decoders for some particular frozen-bit sequences. As such, these schemes work only on specific codes. In particular, the decoding tree of a given rate and length polar code is first constructed, and then the aforementioned nodes are identified and implemented in hardware. Changing the code length or rate will necessitate re-identification of these nodes. As such, these schemes are not suitable for variable-rate and/or variable-length polar codes.

The new radio access technology will use a variable rate and length polar code for downlink control information to fully utilize the physical resources [7]–[9]. As such, implementing fast polar decoders that work for any rate and length is of practical interest. One such decoder, that reduces the decoding depth by one was proposed in [10]. In particular, the authors proposed to decode two bits in parallel by implementing four decoders corresponding to all frozen-bit sequences. The same authors then extended this concept to larger power of 2 block sizes in [11], [12], but the extension results in huge hardware cost as the number of all frozen-bit sequences grows exponentially with the block size. Secondly, their decoding methodology does not identify and utilize the code structure for different frozen-bit sequences to reduce the hardware area or computational complexity.

In this paper, we present fast decoders for variable-rate and/or variable-length polar codes. In particular, we borrow the idea presented in [10]–[12] of implementing $R$-bit ($R = 2, 4, 8, 16$) parallel decoders at the last stage. But, unlike [10]–[12], we do not implement $2^R$ parallel decoders for decoding each contiguous block of $R$ bits. Rather, we rely on a key characteristic of properly-designed polar codes, domination contiguity of the set of good bit-channel indexes [3], to significantly reduce the required number of parallel decoders for each block. Additionally, we use the minimum distance of the polar code corresponding to each domination-contiguous set to further reduce the number of required decoders. For example, we implement only 21 instead of $2^{16}$ parallel decoders for $R = 16$, which implies that the required number of decoders is reduced by 99.97% compared to a simple application of ideas presented in [11], [12].

Achieving hardware-area reduction is not the only aim of our proposed decoding strategy. We also reduce the decoding complexity by relying on specific structure of the polar code corresponding to each bit-channel index set. We aim to minimize computationally-intensive operations, such as check-node operations, while ensuring that the proposed parallel decoders do not tangibly alter the performance of the SC decoder.

Unlike decoding, which is serial in nature, encoding of polar codes can be done in parallel. In fact, the seminal work on polar codes presented a fully-parallel encoding architecture for non-systematic polar codes [1]. Although very high encoding speed can be achieved by implementing a fully-parallel encoder, such an implementation is highly disadvantaged due to large memory size and number of XOR gates, especially for long polar codes. As such, folded or serial implementations of polar-code encoders are implemented to reduce the hardware area [13]. Moreover, systematic polar codes, as proposed in [14], are serial by nature.

Like decoding, the serial implementation of polar encoder results in higher encoding latency. Similar to our proposed decoding strategy, we can increase the encoding speed by implementing $R$-bit parallel encoders at the last stage. Such an implementation is particularly helpful for flexible-rate and/or
flexible-length systematic polar codes as they are non-trivial to be parallelized due to their bidirectional information transfer \[2, 3, 14\].

Our main contributions are summarized in the following.

1) We present fast parallel decoders for variable-rate and variable-length polar codes. In particular, we detail 9 (instead of 2^8) decoders for 8-bit parallel decoding and 21 (instead of 2^16) decoders for 16-bit parallel decoding of polar codes. These decoders accommodate all frozen-bit sequences that can occur in a block of 8 or 16 bits.

2) Secondly, our scheme improves the encoding speed of serially-implemented variable-rate or variable-length polar codes. Our scheme is particularly useful for flexible-rate or flexible-length systematic polar codes as their encoding is hard to be parallelized.

In the following, we first provide a background on polar codes in Section II, primarily to establish some notations and explain the challenges associated with variable-rate polar codes. We also review the domination contiguity of the set of good bit-channel indexes in Section II. We then present our proposed R-bit parallel encoder/decoders in Section III. Afterwards, we present some numerical results for corroboration of our proposed scheme, which will be followed by concluding remarks in Section IV.

Although we will be focusing mainly on the systematic polar codes (due to their superior performance and difficulty in parallelization \[3, 14\]), similar results and conclusions can be drawn for non-systematic polar codes with little or no modifications.

II. BACKGROUND

A. Encoding Polar Codes

Polar codes defined on the binary field, \(\mathbb{F}_2\), are block codes, which can be mathematically described as

\[
x = uG_N,
\]

where \(x \in \mathbb{F}_2^N\) is the codeword of length \(N = 2^n\), \(u \in \mathbb{F}_2^N\) is the input vector comprising information and frozen bits, and \(G_N \in \mathbb{F}_2^{N \times N}\) denotes the generator matrix. The matrix \(G_N\) for non-reversed polar code is \(G_N = F^\otimes n\), where \(F^\otimes n\) is the \(n\)th tensor power of \(F\) defined as

\[
F^\otimes n = \begin{bmatrix}
F^{\otimes (n-1)} & 0 \\
F^{\otimes (n-1)} & F^{\otimes (n-1)}
\end{bmatrix},
\]

with \(F^\otimes 0 = 1\). Denoting the left and right halves of \(u\) (\(x\)) by \(u_0\) and \(u_1\) (\(x_0\) and \(x_1\)), respectively. \[2\] implies \(x_1 = u_1G_{N/2}\) and \(x_0 = u_0G_{N/2} + x_1\). Consequently, a message vector of length \(N\) can be encoded by encoding two message vectors of length \(N/2\) each. Repeating this process \(n\) times results in encoding \(N\) message bits individually. As such, polar codes have a low encoding complexity of \(O(N \log_2(N))\).

For the sake of exposition, we consider only non-reversed polar codes as similar conclusions can be drawn for reversed-polar codes with proper permutation.

B. Constructing Polar Codes

Polar codes rely on the phenomenon of channel polarization, which constructs \(N\) polarization bit channels out of \(N\) independent copies of a given binary memoryless channel, \(W\). In particular, \(N\) copies of \(W\) are combined and then split to a set of \(N\) binary-input channels, \(W^{(i)}_N\), where \(i = 0, 1, \ldots, N - 1\), such that the symmetric capacity of \(W^{(i)}_N\) tends towards either 0 or 1 as \(N\) becomes large. Bit channels having near-symmetric capacity are identified as ‘good’ channels, whereas the others are classified as ‘bad’ channels and are frozen to zero \[1\]. Mathematically, denoting the set of ‘good’ and ‘bad’ bit-channel indexes by \(A\) and \(A^c\), respectively, \(u_{A^c} = \left(u_i : i \in A^c\right) = 0\).

C. Decoding Polar Codes

Since a polar code can be encoded recursively, it can be represented by a binary tree, where each node represents a codeword \[2, 3\]. Fig. 1(a) shows such a tree corresponding to a polar code of length 16, where the white and black leaves correspond to frozen and information bits, respectively.

![Decoding trees corresponding to the (a) SC, (b) SSC, (c) fast-SSC, (d) proposed (R = 8), and (e) proposed (R = 16) decoding algorithms.](image)

We explain different decoding algorithms using the tree representation as follows. In the SC decoder \[1\], the root node receives \(y\), the channel log-likelihood ratios (LLR). Denoting the left and right halves of \(y\) by \(y_0\) and \(y_1\), respectively, the root node sends the outputs of check-node operations between \(y_0\) and \(y_1\) to its left child. Mathematically, the left child receives \(\tilde{y}_0 = y_0 \oplus y_1\), a vector of \(N/2\) real numbers whose \(i\)th element, \(\tilde{y}_{0i}\), is computed as

\[
\tilde{y}_{0i} = y_{0i} \oplus y_{1i} = 2 \tanh^{-1} \left[ \tanh \left( \frac{y_{0i}}{2} \right) \tanh \left( \frac{y_{1i}}{2} \right) \right],
\]

where \(y_{0i}\) and \(y_{1i}\) are the \(i\)th element of \(y_0\) and \(y_1\), respectively.

Afterwards, the left child performs decoding on \(\tilde{y}_0\) (which we will explain later) and returns a binary vector, \(\tilde{x}_0\), to the root node. The root node then computes \(\tilde{y}_1\) and sends it to the right child. The \(i\)th element of \(\tilde{y}_1\), \(\tilde{y}_{1i}\), is computed as

\[
\tilde{y}_{1i} = (1 - 2\tilde{x}_{0i}) y_{0i} + y_{1i},
\]
where $\bar{x}_{0i}$ is the $i$th element of $\bar{x}_0$. The right child then performs decoding similar to the left child and returns a binary vector, $\bar{x}_1$, to the root node. The root node then returns an estimate of the codeword based on $\bar{x}_0$ and $\bar{x}_1$ as

$$\hat{x} = [\bar{x}_0 + \bar{x}_1 \ | \ \bar{x}_1],$$

(5)

where the vector addition is performed in $\mathbb{F}_2^{N/2}$.

For non-systematic polar codes, the left and right children also return $\bar{u}_0$ and $\bar{u}_1$, respectively, to the root node. These binary vectors are estimates of the left and right halves of the input, $\bar{u}$. The root node, in addition to computing $\hat{x}$, computes an estimate of $\bar{u}$ as $\bar{u} = [\bar{u}_0 \ | \ \bar{u}_1]$.

Since each child of the root node can be considered as the root node of a subtree, each child performs exactly the same operation of its parent node. This process continues until the leaf nodes do not have any child, they either send 0 or hard-decision estimates based on the received LLRs to their parents depending on the frozen-bit sequence.

The decoding latency of the SC decoder depends on the computation time of the check-node operation and the decoding-tree depth. The SSC decoder [5] improves the latency by identifying and removing descendants of rate-0 and rate-1 nodes in the code tree as shown in Fig. 1(b). Here, instead of traversing (which involves performing check-node operations) the subtree rooted in a rate-0 node, an all-zero vector is sent to its parent node. Similarly, a rate-1 node computes and sends the binary vector(s) to its parent node without traversing its descendants.

The fast-SSC decoder [2] further prunes the decoding tree by identifying the SPC, REP and REP-SPC nodes in the tree. For example, in Fig. 1(c), the subtrees of two SPC nodes are removed from the tree resulting in the decoding depth of only two.

As clear from Fig. 1, both the SSC and fast-SSC decoders require identification of some special nodes based on the frozen-bit sequence, which can be used to eliminate corresponding subtrees in the code tree. In polar codes with flexible rate or length, the frozen-bit sequence changes with the code rate and length (see Fig. 2). Hence, these algorithms are not directly applicable.

For variable-rate or variable-length polar codes, $R$-bit parallel decoders as proposed in [10]–[12] can be used to improve the decoding speed, where $R = 2^4, 8, \cdots$. Fig. 2 shows such a case where a 16-bit parallel decoder is implemented to decode a variable-rate polar of length $N = 64$. Here, the frozen-bit sequence is represented in hexadecimal notation. For example, when the frozen-bit sequence is FFFE, all bits except the last one are frozen to zero in a block of 16 bits.

Observe that, unlike Fig. 1(b) and (c), the code-tree structure remains the same regardless of the code rate. Secondly, the code tree is also complete, i.e., all nodes except the leaf nodes have two children. A similar observation can be made about Fig. 1(d) and (e), where 8-bit and 16-bit parallel decoders are used to improve the decoding speed, respectively.

The $R$-bit parallel decoders must be able to decode all the frozen-bit sequences that can occur in a block of $R$ bits. One way to satisfy this requirement is to implement $2^R$ parallel sub-decoders and select the appropriate one corresponding to the frozen bit sequence as proposed in [10]–[12]. Unfortunately, this solution becomes impractical even for small values of $R$. However, we can reduce the required number of decoders by using a key characteristic of properly-designed polar codes, domination contiguity, as described below.

### D. Domination Contiguity

Let $\{N\}$ denote the set $\{0, 1, \cdots, N-1\}$, where $N = 2^n$, and $n$ is a positive integer. For $i \in \{N\}$, we use $\langle i \rangle_2$ to represent the $n$-bit binary representation of $i$, i.e., $\langle i \rangle_2 = i_n i_{n-1} \cdots i_1$, where $i_n$ is the most-significant bit. For $i, j \in \{N\}$, $i$ is said to binary dominate $j$, denoted by $i \geq j$, if and only if $i_k \geq j_k$ for all $1 \leq k \leq n$, where $i_k$ and $j_k$ are the $k$th least-significant bits in the binary representations of $i$ and $j$, respectively. A set, $S \subseteq \{N\}$, is domination contiguous if $h, j \in S$ and $h \geq i \geq j$ implies $i \in S$.

For a properly-designed polar code, the set of good bit-channel indexes, $A$, must be domination contiguous [3]. Since not all subsets of $\{N\}$ are domination contiguous, the cardinality of the set of all possible frozen-bit sequences of a properly-designed polar code is less than $2^N$. In the following, we will explain how this key characteristic can be used to significantly reduce the number of required decoders from $2^R$ for $R$-bit parallel decoders.

### III. Proposed Encoder/Decoder Structure

The proposed encoders/decoders rely on parallel encoding/decoding of $R$ bit channels simultaneously, where $R = 2^t$, and $t$ is a positive integer. Specifically, we divide $N$-bit $\bar{u}$ into $N/R$ consecutive groups each containing $R$ bits, i.e., $\bar{u} = [u_0 \cdots u_{N/R-1}]$. Then we encode/decode $R$ bits in each group simultaneously to reduce the encoding/decoding depth of the code tree by $t$ levels.

Quite intuitively, the greater the value of $R$, the faster the encoder/decoder will be. On the downside, we require more hardware to implement all the encoders/decoders for a block size of $R$. Theorem 11 describes inheritance of domination contiguity of $A$ to the domination contiguity in each block...
of $R$ bits, which will be used later to optimize the number of required encoders/decoders for an $R$-bit parallel decoder.

**Theorem 1.** Let $\hat{A}_i$ denote the set of good bit-channel indexes corresponding to $u_i$, $i = 0, 1, \ldots, N/R - 1$. For a properly-designed polar code, $\hat{A}_i$ is domination contiguous.

**Proof:** Observe that all elements of each $\hat{A}_i$ have the same $n-t$ most-significant bits, where $n = \log_2(N)$, and $t = \log_2(R)$. Further, the $n-t$ most-significant bits corresponding to each $\hat{A}_i$ differ in at least one bit from that of $\hat{A}_j$, where $j = 0, 1, \ldots, N/R - 1$, and $j \neq i$. Domination contiguity of $A$ implies that if $h, j \in \hat{A}_i$, and $h \geq k \geq j$ then $k \in \hat{A}_i$. But $h$ and $j$ have the same $n-t$ most-significant bits. As such, $h \geq k \geq j$ implies that $k$ also has the same $n-t$ most-significant bits. Therefore, $k \in \hat{A}_i$.

An immediate consequence of the domination contiguity of $\hat{A}_i$’s is that the number of required encoders/decoders can be reduced from $2^R$ to each block of $S$.

**Theorem 2.** Let $U_R^\circ = \{\hat{A}_i\}$ denote a universal set containing all the good bit-channel indexes of the $i$th R-bit block, $u_i$, for $i = 0, 1, \ldots, N/R - 1$. Denoting the cardinality of a set $S$ by $|S|$, the ratio $|U_R^\circ|/2^R$ is a decreasing function of $R$, and in the limit as $R$ goes to infinity, the ratio $|U_R^\circ|/2^R$ goes to zero.

**Proof:** Without loss of generality, we consider the first $R$-bit block ($i = 0$). Furthermore, we let $P_R = |U_R^\circ|$ and split the elements of any $\hat{A}_0 \in U_R^\circ$ into two sets, $S_0$ and $S_1$, where $S_0$ contains those elements of $\hat{A}_0$ that are less than $R/2$, and $S_1$ contains the remaining.

Theorem 1 asserts that the domination contiguity of $\hat{A}_0$ begets domination contiguity of $S_0$ and $S_1$. Consequently, $U_R^\circ \subseteq B$, where $B = \{B : B = B_0 \cup B_1\}$, $B_0 \subseteq U_{R/2}^\circ$, $B_1 = \{b_i : (b_i - R/2) \in \hat{B}\}$, and $\hat{B} \subseteq U_{R/2}^\circ$. Clearly, $|B| = P_{R/2}^\circ$ and as such, $|U_{R/2}^\circ| = P_{R/2} < P_{R/2}^\circ$.

Moreover, if $\hat{A}_0 \neq \emptyset$ then $R - 1 \in \hat{A}_0$. Equivalently, $\hat{A}_0 \neq \emptyset$ implies $S_1 \neq \emptyset$. Conversely, if $S_1 = \emptyset$ then $\hat{A}_0 = \emptyset$ and $S_0 \neq \emptyset$. But $B$ contains those sets which correspond to $S_1 = \emptyset$ and $S_0 \neq \emptyset$. Therefore, $U_R^\circ \subset B$, and $P_R < P_{R/2}^\circ$.

Lastly, we define a sequence $a_t = P_R/2^R = P_{R/2}^\circ/2^t$, where $t = \log_2(R)$, and $t = 1, 2, \ldots$. Using the fact that $0 < a_t < 1$ and $a_{t+1} < a_t^2$, we get $\lim_{t \to \infty} a_t = \lim_{t \to \infty} a_t^2 = 0$.

**Theorem 2** shows that the ratio $P_R/2^R$ is a decreasing function of $R$. But it does not imply that $P_R$ does not increase rapidly. In fact, $P_R$ can be shown to be equal to $2, 3, 6, 20, 108$, and $7581$ for $R = 1, 2, 4, 8, 16$, and $32$, respectively. Clearly, implementing $P_R$ parallel decoders to increase the decoding speed becomes impractical even for moderate block lengths. Fortunately, we can reduce the number of required decoders further by eliminating some frozen-bit sequences depending on the minimum distance of the corresponding code and the position of frozen bits in the sequence as explained below. Note that the minimum required number of encoders/decoders corresponding to each block of $R$ bits is $R + 1$ because the number of frozen bits in a block of $R$ bits can vary from 0 to $R$. Hence, at least $R + 1$ encoders/decoders are needed.

In the following, we present encoders for all the 20 cases corresponding to $A_i$ for $R = 8$. Later, we reduce this number to the minimum, i.e., 9, based on the position of frozen bits and the minimum distance of the polar code corresponding to each frozen-bit sequence. To do so, we define the notion of max-frozen set, which will be used to eliminate some candidate sets.

Let $\pi_n : \{N\} \to \{N\}$ denote a bit-permutation function that maps $j \in \{N\}$ to $\pi_n(j)$ such that the bits in $(\pi_n(i))_2$ are a permutation of the bits in $(i)_2$. Further, for $D \subseteq \{N\}$, we define $\pi_n(D) = \{\pi_n(d) : d \in D\}$. For example, the bit-reversal permutation $[1]$ for $N = 4$ maps $j$ to $\pi_2(j)$, where $(\pi_2(j))_2 = j_2j_1, \text{and } (j)_2 = j_2j_1$. Likewise, if $D = \{0, 2, 3\}$ then $\pi_2(D) = \{0, 1, 3\}$.

**Lemma 1.** If $D$ is domination contiguous then so is $\pi_n(D)$.

**Proof:** Let $\pi_n^{-1}()$ be the inverse permutation function, i.e., $\pi_n^{-1}(\pi_n(j)) = j$. Further, let $h, j \in \pi_n(D)$ and $h \geq k \geq j$. As such, $\pi_n^{-1}(h), \pi_n^{-1}(j) \in D$. Also, we observe that binary domination is invariant to bit permutations, i.e., $h \geq k \geq j$ implies $\pi_n^{-1}(h) \geq \pi_n^{-1}(k) \geq \pi_n^{-1}(j)$.

Since domination contiguity of $D$ implies $\pi_n^{-1}(k) \in D$, $k \in \pi_n(D)$. Therefore, $\pi_n(D)$ is domination contiguous.

Let $P_N = [e_{\pi_n(0)} \cdots e_{\pi_n(N-1)}]$ denote the permutation matrix corresponding to the bit-permutation function $\pi_n(\cdot)$. Here, $e_i$ denotes a column vector whose $i$th element is 1 and the remaining $N-1$ elements are 0. It was shown in $[15]$, $[16]$ that $P_NG_N = G_NP_N$. Therefore, $uP_NG_N = xP_NG_N$. Denoting $uP_N = u_{\pi_n}$ and $xP_N = x_{\pi_n}$, we get $u_{\pi_n}G_N = x_{\pi_n}$. Consequently, if $x$ is a polar code for input $u$ then permuting the bit positions of $u$ permutes $x$ in the same manner. We refer to these codes as the *conjugates* of the original code. Observe that the set of good bit-channel indexes of a conjugate polar code is $\pi_n(A)$.

**Lemma 1** confirms that, similar to $A$, $\pi_n(A)$ is domination contiguous. Further, when $\pi_n(A)$ differs $A$, the SC decoding shows worse performance $[16]$. However, the SC decoder can be modified to decode in the permuted order $[15]$, $[16]$ to achieve the same performance. Consequently, for a given decoding order, only one set of good bit-channel indexes will show the best performance. Quite intuitively, the set which results in early ‘decoding’ of the most frozen bits will outperform others $[17]$ Section 7.4.3]. We call this set the *max-frozen set*. As such, for a given decoding order, the number of required decoders can be reduced by implementing decoders only for the max-frozen sets and ignoring their distinct bit-permuted sets.

In the following, we present encoders and decoders for $R = 8$. For the sake of clarity, we will drop the subscript $i$ from $A_i$. Also, the set of frozen bit-channel indexes will be represented by $A^f$. Lastly, we will consider the natural-order decoding of polar codes to eliminate all the bit-permuted sets of the max-frozen set.


A. Block Size 8 Encoders/Decoders

Table I enlists all the 20 frozen-bit sequences, \( f \), that can occur in a block of 8 consecutive bit channels of a properly-designed polar code. The \( i \)th component of \( f \) is 1 if the \( i \)th bit channel is frozen and is 0 otherwise. These sequences are grouped into 9 different cases depending on the number of information bits in the block of 8 bits. The corresponding set of good bit-channel indexes are also tabulated. Observe that all the sets are domination contiguous. Lastly, the systematic polar code, \( x \), corresponding to each frozen-bit sequence is also mentioned along with its minimum distance, \( d_{\text{min}} \). As we explain below, the code structure and its corresponding frozen-bit sequence and \( d_{\text{min}} \) will be used to further reduce the number of possible cases from 20 to 9. For the sake of brevity, we have used the notation \( x_{abc} \) to denote \( x_a + x_b + x_c \).

In the following, we discuss each individual case and explain why a particular frozen-bit sequence is kept in each case.

1) Case 0: This case corresponds the rate-0 node introduced in [5], and the optimal decoder assigns an all-zero vector to the output.

2) Case 1: This is an (8, 1) repetition code, and the optimal maximum-likelihood (ML) decoder will add the LLRs of all the channel outputs and perform threshold detection on the sum [18]. The same decoder is used in [2], where they have outlined some low-latency decoding strategies for improving the decoding speed.

3) Case 2: All the three cases are (8, 2) repetition codes and are conjugates of one another. For the SC decoder with natural-order decoding, the first case is the max-frozen set. Consequently, other cases will not occur. The optimal decoder, like Case 1, will add the LLRs of four outputs to estimate \( x_7 \) and other four LLRs to estimate \( x_6 \).

4) Case 3: These codes are concatenated (8,4) repetition and (4,3) single parity-check (SPC) codes and are conjugates of one another. Since \( \hat{A} = \{5, 6, 7\} \) is the max-frozen set, only the first case will occur in practice. The decoding can be carried out by first adding the LLRs of the outputs corresponding to the same bits. As such, we are left with the LLRs of a (4,3) SPC code. The optimal ML decoder of the SPC codes, Wagner decoder [19], makes hard-decision estimates of \( x_i \)'s and flips the least-reliable bit if the parity check is not satisfied.

5) Case 4: The number of good bit-channel indexes, \( \hat{A} \), is 4 when \( k = 4 \). Amongst them, three correspond to (8,4) repetition codes. As such, their \( d_{\text{min}} = 2 \). In only one case, \( \hat{A} = \{3, 5, 6, 7\} \), the minimum distance turns out to be 4. Since code performance heavily depends on \( d_{\text{min}} \), only this case will occur in practice. In fact, this is an extended Hamming code [20] and is equivalent to the repetition-SPC code introduced in [2]. Although the optimal ML decoder for such a code can be implemented easily [18], a low-complexity decoder of this code was mentioned in [2]. Furthermore, the bit-error rate (BER) performance of the code is not considerably altered by implementing the low-complexity decoder instead of the optimal decoder [2]. For completeness, we briefly mention the low-complexity decoder below.

First, observe that \( (x_0 + x_4, x_1 + x_5, x_2 + x_6, x_3 + x_7) \) constitute a (4,1) repetition code, while \( (x_4, x_5, x_6, x_7) \) is a (4,3) SPC code. The repetition code can easily be decoded by adding the LLRs, resulting in \( \hat{x}_8 \), a hard-decision estimate of \( x_8 = x_3 + x_7 \). Afterwards, additional LLRs for \( (x_4, x_5, x_6, x_7) \) are trivially computed either by keeping or switching the sign of the LLRs of \( (x_0, x_1, x_2, x_3) \) depending on the value of \( \hat{x}_8 \). After adding the LLRs of \( (x_4, x_5, x_6, x_7) \), we are left with a
Case 2, we can find hard-decision estimates of $u$, which can be used to decode the input, $x$. Coders can be used to find a hard-decision estimate of $u$, and de- 

For non-systematic codes, exactly the same de-

Remark 3. Implementing the proposed low-complexity de-

$\hat{x} \in \{0, 1\}$, which can be used to find a hard-decision estimate of $x$. The decoding latency can be reduced by implementing a cycle-free Tanner graph of $\tilde{x}$, which can be used to find estimates of $(x_0, x_1, x_2, x_3)$. The decoding latency can be reduced by implementing two parallel decoders depending on the actual value of $\tilde{x}$. As such, compared with the SC decoder, where 12 check-node operations are used and are carried out sequentially, the proposed decoders require less check-node operations and are faster as these operations can be implemented in parallel.

B. Block Size 16 Encoders/Decoders

Having discussed all the possible cases for $R = 8$, we now consider polar codes for $R = 16$. Similar to $R = 8$ case, we can significantly reduce the required number of parallel encoders/decoders (from 168 to just 21). Table [I] lists these 21 cases along with the $d_{\text{min}}$ of the corresponding codes. Here, we have used hexadecimal indexes for the sake of brevity. The appendix provides a detailed description of the proposed decoders for the cases tabulated in Table [II].

It is worth noting that at least 17 encoders/decoders are required for encoding/decoding flexible-rate polar codes. So only four extra encoders/decoders are needed to ensure that the polar codes designed for any rate, length and channel can be encoded/decoded. The following theorems assert that the polar codes designed for a BEC, encoders/decoders for $f = \text{FFC0}$, $f = \text{FF80}$, $f = \text{FFC0}$, and $f = \text{FC0C}$ are not required when polar codes are designed for a binary-eraser channel (BEC) or by Huawei formula [7].

Theorem 3. If polar codes are constructed for a BEC, encoders/decoders for $f = \text{FFC0}$, $f = \text{FF80}$, $f = \text{FFC0}$, and $f = \text{FC0C}$ are not required.

Proof: This assertion can be proved by noting that, regardless of the value of erased probability, the aforementioned four cases do not occur when $N = 16$. The result immediately follows by noting that the frozen-bit sequence for each of 16-bit block is generated for a BEC [1].

Recently, in 3GPP RAN1 #87 meeting, an agreement was reached to use variable-rate polar codes for uplink control channel [7], [9]. Since polar-code design is channel dependent, and the location of frozen bits varies with the channel conditions, Huawei presented a channel-independent reliability metric for constructing polar codes [7]. In particular, each polarized bit-channel, $W_{N}^{(j)}$, is assigned a reliability metric, $Q_j$, computed as

$$Q_j = \sum_{k=1}^{n} j_k^{k + \frac{1}{k}}.$$ (6)
TABLE II
FROZEN-BIT SEQUENCES AND THE CORRESPONDING OUTPUTS FOR R = 16.

| k  | f (Hex) | Output: x | $d_{\text{min}}$ |
|----|---------|-----------|-----------------|
| 0  | FFFF    | 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0 | - |
| 1  | FFEF    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 16 |
| 2  | FFCC    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 8 |
| 3  | FFF8    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 8 |
| 4  | FFE8    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 8 |
| 5  | FE8E    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 8 |
| 6  | FFC0    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 4 |
| 7  | FF80    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 4 |
| 8  | FE80    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 4 |
| 9  | FCC0    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 4 |
| 10 | FC80    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 4 |
| 11 | F880    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 4 |
| 12 | E880    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 2 |
| 13 | E800    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 2 |
| 14 | C800    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 2 |
| 15 | E000    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 2 |
| 16 | E000    | x, x, x, x, x, x, x, x, x, x, x, x, x, x, x, x | 2 |

where $j_k$ is the $k$th least-significant bit in the $n$-bit binary representation of $j$, i.e., $j_2 = j_0j_1j_2\cdots j_{n-1}$.

The following theorem asserts that the extra cases are not required when polar codes are constructed by Huawei formula.

**Theorem 4.** If polar codes are constructed by using Huawei formula, the four extra case ($f$ = FFC0, $f$ = FF80, $f$ = FCC0, and $f$ = C0C0) do not occur at all.

**Proof:** Observe that

$$Q_j = \sum_{k=1}^{n} j_k 2^{k-1} = \left[ \frac{4 j_1 2^{-1}}{T_1} + \sum_{k=5}^{n} j_k 2^{k-1} \right],$$

(7)

Next, we partition $\mathbb{N}$ into $N/16$ consecutive groups, each containing 16 numbers. By denoting them with $G_i$, where $i = 0, 1, \cdots, N/16 - 1$, we have $G_0 = [16]$ and $G_i = \{16i + g : g \in G_0\}$. Further, observe that $Q_j$ of all the elements in $G_i$ have exactly the same value of $T_2$. As such, inclusion of $j \in G_i$ in $A_i$ depends solely on $T_1$, or the last four bits of $(j)_2$. Letting $j$ denote the decimal number corresponding to the last 4 bits of $j$, we observe that the values of $T_1$ decreases monotonically when $j$ takes on values from $Q_0^{15} = (15, 14, 13, 11, 7, 12, 10, 9, 6, 5, 3, 8, 4, 2, 1, 0)$ left to right. As such, for Case $k$ ($k = 0, 1, \cdots, 16$), the first $k$ bit-channel indexes are selected in $Q_0^{15}$ for information transfer, and the rest are frozen to zero. Consequently, only 17 unique cases will occur, and the afore-mentioned four extra cases will not occur.

![Fig. 4. BER performance of systematic and non-systematic rate-1/2 polar codes of length $N = 256$ in additive-white-Gaussian noise channel with the signal-to-noise ratio of $E_c/N_0$ when decoded by conventional SC decoder and the proposed decoders for $R = 8$.](image)

**IV. RESULTS**

In this section, we compare the proposed decoding strategy with the SC decoder in terms of the bit-error-rate and decoding latency performances.

**A. BER Performance**

Fig. 4 compares the BER performance of the proposed 8-bit parallel decoders with that of the SC decoder. Both optimal
and low-complexity sub-optimal decoders are implemented for the proposed decoders. Here, the polar codes are constructed for the binary-erasure channel with the erasure probability of $e^{-1} \simeq 0.37$ [22], [23].

Some interesting observations can be made by analyzing the figure. First, the proposed decoders do not deteriorate the performance of the SC decoder. Second, the performance gap between the optimal and the sub-optimal decoders is negligibly small, which implies that the low-complexity decoders can be used instead of the optimal ones. Last, the proposed schemes can be used for both systematic and non-systematic polar codes.

B. Decoding Latency

One way to approximate the decoding latency of different polar decoders is as follows. We presume that bit operations and addition/subtraction of real numbers can be carried out in one clock cycle, whereas a check-node operation takes $T_c$ and finding the minimum of a list takes $T_m$ clock cycles. Note that finding a minimum requires significantly less computations than performing a check-node operation [24].

For a block of $R$ bits, the SC decoder performs $R/2$ check-node operations in each of $\log_2(R)$ stages. But all the check-node operations can be performed in parallel in the first stage, whereas the last stage requires all check-node operations to be performed in a sequential manner. In general, the number of parallel check-node operations performed in the $m$th stage is $R/2^m$, where $m = 1, 2, \ldots, \log_2(R)$. Consequently, a decoding latency of $T_c(R/2 + R/4 + \cdots + 1) = (R - 1)T_c$ cycles is incurred in performing check-node operations for the SC decoder. Similarly, the number of binary and real additions involved in decoding $R$ bits can be shown to be $1$ and $R - 1$, respectively. Therefore, an SC decoder will take $R + (R - 1)T_c$ clock cycles to decode a block of $R$ bits. Note that this decoding latency is fixed regardless of the frozen-bit sequence.

For the proposed schemes, the decoding latency varies depending on the frozen-bit sequence. For example, for $R = 8$, Case 0 can be executed instantaneously, whereas Case 4 incurs the highest decoding latency of $1 + \max \{T_c, T_m\}$ cycles, which is calculated as follows. The check-node operations are performed in parallel, so they take only $T_c$ cycles for execution. Meanwhile, two outputs can be generated corresponding to $x_8 = 0$ and 1 by two Wagner decoders ($T_m + 1$ clock cycles), and, depending on the value of $x_8$ (computation time is 1 cycle), one of the outputs is selected. Therefore, the decoding latency for Case 4 is $\max \{1 + T_c, 1 + T_m\}$.

Observe that even the highest decoding latency of the proposed decoders is much smaller than that of the SC decoder. Hence, our proposed scheme will significantly improve the decoding speed of variable-rate polar codes.

Table III shows the decoding latency, $L$, of the proposed low-complexity decoders for blocks of length $R = 8$ and $R = 16$ bits. Observe that the proposed decoders have significantly less decoding latency compared to the SC decoder, which has the decoding latency of $R + (R - 1)T_c$ cycles for all the cases.

V. Conclusion

In this work, we presented fast 8-bit and 16-bit parallel decoders that can reduce the decoding-tree depth of the decoding tree of variable-rate and variable-length polar codes. They can reduce both the decoding latency and hardware complexity without deteriorating the bit-error-rate performance of the successive-cancellation decoder.

APPENDIX

Block Size 16 Decoders

This appendix details the proposed low-complexity parallel decoders for the cases tabulated in Table III.

1) Case 0: The optimal decoder assigns an all-zero vector to the output.

2) Case 1: This is a repetition code, and the optimal decoder makes a hard decision on the sum of the LLRs of the received bits.

3) Case 2: This is a (16,2) repetition code, and the optimal ML estimates of $x_k$ and $x_{k+1}$ can be found by making hard-decisions on the LLR sums of even-indexed and odd-indexed bits, respectively.

4) Case 3: This is a (4,3) SPC code concatenated with a (16,4) repetition code. The optimal decoder will first add the LLRs of the received bits corresponding to $x_0, x_1, x_2,$ and $x_3$ before finding their hard estimates with the Wagner decoder.

5) Case 4: This is an (8,4) extended Hamming code concatenated with a (16,8) repetition code. Decoders mentioned in Case 4 for $R = 8$ can be used after adding the LLRs of the first half to the second's.

6) Case 5: Although an exhaustive-search based ML decoder can be implemented, we can reduce the decoding complexity by introducing a new variable, $z = x_7 + x_9$. By noting that $x_0 + x_8 = x_1 + x_9 = \cdots = x_7 + x_9 = z$, we first find $\hat{z}$, a hard-decision estimate of $z$. Specifically, we add $y_0 \oplus y_8, y_1 \oplus y_9, \ldots, y_7 \oplus y_9$ to get an LLR for $z$ and make a hard decision on the LLR to compute $\hat{z}$.

Afterwards, the decoder computes $y_0 \pm y_8, y_1 \pm y_9, \ldots, y_7 \pm y_9$, where addition is performed when $\hat{z} = 0$, and subtraction otherwise. These values are then input to one of the decoders of Case 4 for $R = 8$ to get estimates of $x_8, x_9, \ldots, x_{16}$. Lastly $\hat{z}$ is added to $x_8, x_9, \ldots, x_{16}$ to compute $\hat{x}_8, \hat{x}_9, \ldots, \hat{x}_{16}$.

Implementing two parallel decoders corresponding to $\hat{z}$ equalling 0 and 1 and choosing an appropriate output after computing $\hat{z}$ can reduce the decoding latency.

7) Case 6: For the first case, $f = \text{FFC}0$, an optimal decoder can be implemented by noting that the codeword comprises two concatenated (4,5) SPC and (8,4) repetition codes. Two separate Wagner decoders can be used to find hard estimates of the transmitted bits after adding the LLRs of the repeated bits.

For the second case, $f = \text{FEE}0$, the decoder presented in Case 5 ($R = 16$) can be used to decode the received LLRs with the exception that the decoder of Case 4 ($R = 8$) is replaced with the low-complexity decoder of Case 5 ($R = 8$).
8) Case 7: The first case, \( f = FF80 \), corresponds to a concatenated (8,7) SPC and (16,8) repetition code. Therefore, the code can be decoded optimally by adding the LLRs of \( x_0, x_1, \ldots, x_7 \) to that of \( x_8, x_9, \ldots, x_{15} \) and finding hard estimates by the Wagner decoder.

For the second case, \( f = FEC0 \), the decoder presented in Case 5 (\( R = 16 \)) can be used to decode the received LLRs with the exception that the low-complexity decoder of Case 6 (\( R = 8 \)) replaces the decoder of Case 4 (\( R = 8 \)).

9) Case 8: For the first case, \( f = FE80 \), the decoder presented in Case 5 (\( R = 16 \)) can be used to decode the received LLRs with the exception that the Wagner decoder is used instead of the decoder of Case 4 (\( R = 8 \)).

For the second case, \( f = FCC0 \), the even-indexed and the odd-indexed bits constitute two separate (8,4) extended Hamming codes. Therefore, the decoders for Case 4 (\( R = 8 \)) can be used to decode the received code vector.

10) Case 9: A low-complexity decoder can be implemented by defining \( z_0 = x_6 + x_8 \) and \( z_1 = x_7 + x_9 \). Observe that \( x_0 + x_8 = x_2 + x_A = x_4 + x_C = x_6 + x_E = z_0 \), and \( x_1 + x_9 = x_3 + x_A = x_5 + x_D = x_7 + x_F = z_1 \). The proposed decoder makes hard decisions on \( y_0 \oplus y_A \oplus y_C \oplus y_E \) and \( y_1 \oplus y_B \oplus y_D \) and respectively assigns them to \( z_0 \) and \( z_1 \), hard estimates of \( z_0 \) and \( z_1 \), respectively. Afterwards, additional LLRs for \( x_8, x_9, \ldots, x_{15} \) are computed by using \( z_0 \) and \( z_1 \). For example, the additional LLR of \( x_8 \) is \( y_0 \) when \( z_0 \) is 0 and \( -y_0 \) otherwise. After adding the additional LLRs to \( y_0, y_B, \ldots, y_{15} \), Wagner decoder is used to find hard estimates of \( x_8, x_9, \ldots, x_{15} \), which along with \( z_0 \) and \( z_1 \) are used to estimate \( x_0, x_1, \ldots, x_7 \).

The decoding latency can be reduced by implementing four Wagner decoders (corresponding to four possible values of \( z_i, z_i' \)) and using the computed value of \( (z_0, z_1) \) to select the output of corresponding Wagner decoder.

11) Case 10: A low-complexity decoder can be implemented by defining four variables: \( z_0 = x_0 + x_8 = x_4 + x_9 \), \( z_1 = x_1 + x_9 = x_5 + x_C \), \( z_2 = x_2 + x_A = x_6 + x_D \), and \( z_3 = x_3 + x_8 = x_7 + x_F \). The decoder will first compute \( z_i \)'s, hard estimates of \( z_i \)'s, where \( i = 0, 1, 2, 3 \), from the LLRs obtained by adding LLRs of the output of check-node operations. For example, LLR of \( z_0 \) is computed by adding \( y_0 \oplus y_8 \) and \( y_4 \oplus y_9 \), where \( y_i \) denotes the LLR of \( x_i \). Depending on the value of \( z_i \)'s, additional LLRs for \( x_8, x_9, \ldots, x_{15} \) are obtained from \( y_0, y_1, \ldots, y_7 \). For example, additional LLR for \( x_8 \) is \( y_0 \) when \( z_0 = 0 \) and \( -y_0 \) when \( z_0 = 1 \). After adding the additional LLRs to the received LLRs, the decoder finds hard estimates of \( x_8, x_9, \ldots, x_{15} \) using Wagner decoder. Finally, these hard estimates are used along with \( \hat{z}_i \)'s to estimate \( x_0, x_1, \ldots, x_7 \).

12) Case 11: A low-complexity decoder can be implemented by observing that \( z_0, z_1, \ldots, z_7 \) constitute an (8,4) extended Hamming code, where \( z_0 = x_0 + x_8, z_1 = x_1 + x_9, \ldots, z_7 = x_7 + x_F \). As such, the decoders of Case 4 for \( R = 8 \) can be used to find \( \hat{z}_i \)'s, estimates of \( z_i \)'s for \( i = 0, 1, \ldots, 7 \). Then, depending on the values of \( \hat{z}_i \), additional LLRs for \( x_8, x_9, \ldots, x_{15} \) are obtained from \( y_i \)'s, where \( i = 0, 1, \ldots, 7 \). For example, the additional LLR for \( x_8 \) is \( y_0 \) if \( \hat{z}_0 = 0 \) and \( -y_0 \) otherwise. After adding the LLRs, Wagner decoder is used to compute estimates of \( x_8, x_9, \ldots, x_{15} \). The decoded bits along with \( \hat{z}_0, \hat{z}_1, \ldots, \hat{z}_7 \) are then used to compute estimates of \( x_0, x_1, \ldots, x_7 \).

13) Case 12: For the first case, \( f = E800 \), the decoder of Case 11 can be used to decode the received LLRs, with the exception that the Wagner decoder is not used at all. Rather, hard decisions are made on the updated LLRs of \( x_8, x_9, \ldots, x_{15} \).

In the second case, \( f = C0C0 \), the code word consists of four separate (4,3) SPC codes, which can be individually decoded by the Wagner rule.

14) Case 13: Introducing a new variable, \( z = x_3 + x_7 + x_9 + x_F \), results in a cycle-free Tanner graph as shown in Fig. 5. As such, a non-iterative optimal MAP decoder can easily be implemented for this case.

A low-complexity decoder can also be constructed for this code. For example, making a hard decision on \( z \) results in four separate SPC codes, which can be decoded by the Wagner rule.

15) Case 14: This code consists of two (8,7) SPC codes, which can be optimally decoded by two Wagner decoders.

16) Case 15: This is a (16,15) SPC code, and Wagner decoder can be used to decode the received LLRs optimally.

17) Case 16: The optimal decoder will make hard decisions on the LLRs of the received bits.

### Table III

| Case | Latency, \( R = 8 \) | Latency, \( R = 16 \) | Latency, \( R = 16 \) |
|------|---------------------|---------------------|---------------------|
| 0    | 0                   | 0                   | 1 + max \( T_c, T_m \) |
| 1    | 1                   | Case 1              | 1 + max \( T_c, T_m \) |
| 2    | 1 + \( T_m \)       | Case 3              | 3 + \( T_c + T_m \) |
| 3    | 1 + max \( T_c, T_m \) | Case 4              | 2 + max \( T_c, T_m \) |
| 4    | 1 + \( T_c \)       | Case 5              | 3 + max \( T_c, T_m \) |
| 5    | \( T_m \)           | Case 6              | \( 1 + T_m \) |
| 6    | \( T_m \)           | Case 7              | 3 + \( T_c \) |
| 7    | 0                   | Case 8              | 1 + \( T_m \) |
| 8    | 2 + \( T_m \)       | Case 9              | \( T_m \) |
| 9    | 2 + \( T_m \)       | Case 10             | \( T_m \) |
| 10   | 0                   | Case 11             | 0                   |
| 11   | 0                   | Case 12             | 0                   |
| 12   | 0                   | Case 13             | 0                   |
| 13   | 0                   | Case 14             | 0                   |
| 14   | 0                   | Case 15             | 0                   |
| 15   | 0                   | Case 16             | 0                   |
Fig. 5. Tanner graph for the systematic-polar code corresponding to $f = E000$.

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