From FPGAs to Obfuscated eASICs: Design and Security Trade-offs

Zain UI Abideen, Tiago Diadami Perez, Samuel Pagliarini
Centre for Hardware Security, Tallinn University of Technology (TalTech), Estonia
{zain.abideen, tiago.perez, samuel.pagliarini}@taltech.ee

Abstract—Threats associated with the untrusted fabrication of integrated circuits (ICs) are numerous: piracy, overproduction, reverse engineering, hardware trojans, etc. The use of reconfigurable elements (i.e., look-up tables as in FPGAs) is a known obfuscation technique. In the extreme case, when the circuit is entirely implemented as an FPGA, no information is revealed to the adversary but at a high cost in area, power, and performance. In the opposite extreme, when the same circuit is implemented as an ASIC, best-in-class performance is obtained but security is compromised. This paper investigates an intermediate solution between these two. Our results are supported by a custom CAD tool that explores this FPGA-ASIC design space and enables a standard-cell based physical synthesis flow that is flexible and compatible with current design practices. Layouts are presented for obfuscated circuits in a 65nm commercial technology, demonstrating the attained obfuscation both graphically and quantitatively. Furthermore, our security analysis revealed that for truly hiding the circuit’s intent (not only portions of its structure), the obfuscated design also has to chiefly resemble an FPGA: only some small amount of logic can be made static for an adversary to remain unaware of what the circuit does.

Index Terms—Hardware Obfuscation, Secure ASIC Design, CAD, Reconfigurable obfuscation, Reverse engineering

I. INTRODUCTION

Shipment of semiconductor devices is forecast to surpass one trillion units in the year 2021, the third time this mark is surpassed in a calendar year since 2018 [1]. The majority of those devices are being manufactured by foundries that subscribe to the fab-for-hire model. A rogue element within the foundry can mount fabrication-time attacks, i.e., the foundry and its employees are considered potential adversaries. Many potential threats regarding third-party foundries have been studied in recent years, include tampering, counterfeiting, reverse engineering, and overproduction [2]. On the other hand, many techniques have been devised to mitigate threats from untrusted fabrication. Countermeasure techniques to increase the IC security against not only third-party foundries but also from the end-user have been recently demonstrated. Notable examples include IC Camouflaging [3]–[5], Logic Locking [6]–[8], and Split Manufacturing [9], [10].

Generally speaking, all of the aforementioned countermeasures attempt to “hide” the design from adversaries and can be classified as obfuscation techniques. Unfortunately, none of these techniques is currently adopted in large-scale production of ICs, for reasons that include (lack of) practicality [9] and insufficient security guarantees [11]. Another approach towards obfuscation is the use of an FPGA (or FPGA-like) design, where the configuration bitstream serves as a key to unlock the functionality of the circuit [12]. Our paper too explores this possibility. The fabric in an FPGA contains reconfigurable elements, but this flexibility incurs a limited performance. On the other hand, ASIC requires one-time placement, it is static (non-reconfigurable), but it provides best-in-class performance. As shown in Fig. 1, performance increases if we move from right to left. Contrarily, area, obfuscation, and flexibility increase if we move from left to right. However, we argue that neither extremes of the spectrum are a good design point for circuits that have stringent security and performance constraints. An intermediate solution is a better trade-off and this is precisely the motivation for our work. We term our in-between solution an “embedded ASIC” (eASIC).

Design obfuscation concept: In this work, we propose to obfuscate a design by exploiting the best of both worlds. The generated device is a hybrid which includes reconfigurable elements (analogous to the FPGA) and also includes ASIC cells as static elements, i.e., gates with fixed functionality after fabrication. Previous research on obfuscation by reconfigurable elements has focused on keeping the reconfigurable portion as small as possible [13], [14], which is logical if the goal is to keep overheads under control. However, we later show that true hiding of the circuit’s intent requires a high degree of obfuscation that is usually not explored in the state of the art. Thus, our eASIC device is largely non-functional until it is programmed. Our main contribution is a tool for automatically obfuscating a design in the form of eASIC, where the obfuscation range can be from 0 to 100%. Furthermore, its physical synthesis flow is standard-cell based that is compatible with current design and fabrication practices.

II. A CAD FLOW FOR eASIC

Our CAD flow is centered around a tool named Tuneable Design Obfuscation Technique using eASIC, or TOTe for short. This section explains the CAD flow of eASIC and TOTe’s main features. TOTe generates a hybrid design with static and reconfigurable elements, which we refer to as eASIC. For the reconfigurable elements, we implement the logic utilizing the notion of programmable LUTs (Look Up Tables) - same as in FPGAs. The complete TOTe design flow for generating an eASIC is shown in Fig. 2 and it consists of three phases.

In the first phase of our flow, the design under obfuscation, described in register-transfer level (RTL) form, is synthesized using a commercial FPGA synthesis tool. As a result, the netlist contains all typical FPGA primitives, i.e., FFs, MUXs, and LUTs. The input
Algorithm 1: Tunable Obfuscation Technique using eASIC

Input: \( L \) (list of LUTs), \( P \) (list of paths), \( \text{obf_c} \) (obfuscation criterion)

Output: \( e\text{ASIC} \leftarrow f(\text{input}) \)

1. \( L_{ST} \leftarrow \emptyset \)
2. \( L_{RE} \leftarrow L \)
3. while \( \text{SIZE} \_\text{OF} \ (L_{ST}) \leq \text{obf_c} \) do
   4. \( \text{path} \leftarrow \text{FIND}\_\text{CRITICAL}(P) \)
   5. \( \text{lut} \leftarrow \text{FIND}\_\text{SLOWEST}(\text{path}) \)
   6. if \( \text{lut} \in L_{RE} \) then
      7. \( \text{INSERT}(\text{lut}, L_{ST}) \)
      8. \( \text{UPDATE}\_\text{TIMING}(\text{lut}, P) \)
   9. else
      10. \( \text{REMOVE}(\text{path}, P) \)
11. end
12. for each \( \text{lut} \in L_{RE} \) do
13. \( \text{GEN}\_\text{CASE}_0\_1(\text{lut}) \)
14. \( e\text{ASIC} \leftarrow L_{ST} \cup L_{RE} \)

In the third and final phase, the obfuscated netlist from TOTe is synthesized using any commercial ASIC CAD tool and implemented using an also commercial physical synthesis tool where traditional P&R, CTS, DRC, LVS, etc. steps are executed. Finally, the tapeout database is sent to the foundry for fabrication. Once the fabricated parts are delivered, they have to be programmed (i.e., using a bitstream as in FPGAs) for the eASIC design to be completed and functional.

III. EXPERIMENTAL RESULTS USING TOTe

This section reports the analysis of security versus performance, security versus area for selected designs and reports the results for numerous designs after obfuscation. For all experimental results that follow, FPGA synthesis was executed in Vivado and the targeted device is Kintex-7 XC7K325T-2FFG900C, which contains only 6-input LUTs. For the ASIC flow, the implementations are done using a commercial 65nm PDK with three standard cell flavors (LVT/SVT/HVT) and tools from Cadence suite (i.e., Genus and Innovus). However, we emphasize that TOTe is agnostic with respect to PDKs, libraries, and tools. In the experiments that follow, we prevent the FPGA synthesis from inferring any BRAM or instantiating any DSP cells. This choice makes for very clear trade-offs when obfuscating the logic. Nevertheless, if a given design requires memory cells, TOTe has the capability to translate the inferred BRAMs into compiled SRAMs for the specific ASIC technology utilized.

A. Custom standard-cell based LUTs

The premise of eASIC is to have reconfigurable and static elements that can be integrated transparently. For this reason, we have designed our own custom LUTs (LUT1, LUT2,..., LUTn) by following VPR’s template [15]. Different from FPGAs that generally implement only one LUT size, for eASIC we have the flexibility to implement more than one size because our design intent will not change. By doing
this, we preserve area and potentially increase the performance of eASIC. The layouts for LUT1, LUT2, and LUT6 macros are shown in Fig. 3. These blocks are highly compact since the main design goal for them was area/density. Each LUT has its own registers for storing the configuration, a functionality that is enabled by including three extra configuration pins (\texttt{serial\_in, serial\_out, and enable}). The LUTs are connected to one another in a daisy chain that is analogous to a scan chain. We chose a flip-flop based implementation to make our framework easily portable between technologies, and also, make the floorplan and placement almost effortless. Using SRAM for storing those bits, on the other hand, can save area and power but requires extra effort during implementation since memories need special power routing and have to be strategically placed to achieve the best performance.

### B. Design Space Exploration in TOTe

For our first experiment, we selected a small but representative design which covers all possible FPGA primitives: a schoolbook multiplier (SBM), which is a bit-serial polynomial multiplication circuit. For a SBM design that is synthesized targeting a very high frequency, the \textsl{CP} and \textsl{sumCP} become, as calculated by TOTe’s timing engine, 0.490 ns and 16088.69 ns, respectively. These values correspond to a design obfuscated at 100\%, i.e., the design has only reconfigurable logic. The absolute accuracy of these values is not relevant since final timing analysis is performed using a commercial physical synthesis engine later.

While the SBM design is an interesting motivational example, it showed that \textsl{CP} tends to saturate while the \textsl{sumCP} continues to improve as the obfuscation is reduced. Next, we wanted to determine if the same saturation trend appears for other designs and the results are reported in Table I. From these experiments, it is possible to conclude that the performance of numerous designs saturates incredibly fast as we decrease the obfuscation level, even when the obfuscation range is limited to 86-100\%. Moreover, the results for AES-128 [16], RISC-V, and SHAKE-256 have been depicted in Fig. 4. Several other designs, including ISCAS’85 benchmarks and known opencores, have been evaluated. The complete set of results can be found in our git repository [17]. Concerning runtime, TOTe requires only a few minutes for big designs. Then, commercial CAD tools require a considerable amount of time for logic and physical synthesis (same as conventional ASIC flow). In summary, TOTe does not become a bottleneck in the design flow.

### IV. SECURITY ANALYSIS

As compared to conventional logic locking, the LUTs introduced in eASIC are the key-gate equivalents. In principle, a single LUT\textsubscript{s} ought to be equivalent to 2\textsuperscript{n} XOR/XNOR key-gates. In practice, the LUT logic has similarities to a run of key-gates (see [7]) due to the \textit{n}-to-1 multiplexing nature of it, which reduces the search space and may possibly make eASIC vulnerable to well-known oracle-based attacks (e.g., SAT). However, notice that we are considering designs with target obfuscation rates higher than 86\%, which results in bitstreams with thousands of bits. Even for a small and combinational design as the ISCAS'85 c7552, 50\% of obfuscation requires a bitstream with approximately 11k bits. The SAT attack is not able to find the correct key, even running for more than 60 hours. On the other hand, the same circuit with 10\% of obfuscation and a bitstream in the order of 1k bits, the SAT attack was successful, requiring less than a minute to retrieve the correct key. In general, the high obfuscation percentages obtained in eASIC discourage an adversary from performing SAT attacks. Similar findings were reported in [13], [14], [18]. However, our proposed eASIC design \textit{potentially} creates attack vectors that other approaches do not since a portion of the design is exposed (from an adversary point of view). We will focus on these attacks in the text that follows.

#### A. Threat Model

In our considered threat model, the primary adversary is the \textit{untrusted foundry}. We make no distinction whether the adversary is institutional or a rogue employee. Assuming the security of an eASIC design is a function of its static logic (fully exposed) and reconfigurable logic (protected by a bitstream that serves as a key), we make the following assumptions:

- The main adversarial goal is to reverse engineer the design in order to pirate its IPs, overproduce the IC, or even to insert

\begin{table}[h]
\centering
\caption{Detailed results for selected designs using TOTe}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline
Design & \textbf{Obs. (%)} & \textbf{sumCP (ns)} & \textbf{CP (ns)} & \textbf{Area-RE (\square mm\textsuperscript{2})} & \textbf{Area-ST (\square mm\textsuperscript{2})} & \textbf{LUT (RE)} & \textbf{LUT (ST)} \\
\hline
SBM & 98 & 16088.690 & 0.490 & 13190.04 & 29 & 0 & 0 \hline
95 & 15895.826 & 0.484 & 12792.00 & 21.40 & 28 & 1 & 1 \hline
92 & 15877.962 & 0.464 & 12547.80 & 12.11 & 27 & 2 & 2 \hline
89 & 15145.506 & 0.461 & 12438.72 & 37.56 & 26 & 3 & 3 \hline
86 & 15370.682 & 0.459 & 12234.52 & 48.27 & 25 & 4 & 4 \hline
\hline
PID & 98 & 2517.581 & 0.756 & 445590.0 & 2816.82 & 896 & 18 \hline
95 & 2466.254 & 0.642 & 432340.9 & 9441.36 & 869 & 45 & 45 \hline
92 & 2391.963 & 0.592 & 421365.9 & 14928.84 & 841 & 73 & 73 \hline
89 & 2348.613 & 0.568 & 407273.7 & 21794.94 & 814 & 100 & 100 \hline
86 & 2322.462 & 0.543 & 392454.6 & 29439.0 & 787 & 127 & 127 \hline
\hline
SHA-256 & 98 & 7425.731 & 0.962 & 1313150.7 & 12091.86 & 2195 & 44 \hline
95 & 7354.593 & 0.871 & 1275984.0 & 25875.24 & 2128 & 111 & 111 \hline
92 & 7322.155 & 0.871 & 1233448.5 & 50412.96 & 2060 & 179 & 179 \hline
89 & 7301.945 & 0.871 & 1197083.6 & 77029.92 & 1992 & 246 & 246 \hline
86 & 1644.025 & 0.871 & 1123979.6 & 103967.46 & 1925 & 313 & 313 \hline
\hline
FPU & 98 & 2909.063 & 0.707 & 1031676.8 & 1250.028 & 2487 & 50 \hline
95 & 2734.008 & 0.650 & 1003223.6 & 2572.586 & 2412 & 126 & 126 \hline
92 & 2572.952 & 0.650 & 966671.20 & 4498.11 & 2336 & 202 & 202 \hline
89 & 2478.732 & 0.650 & 935060.0 & 60808.68 & 2259 & 279 & 279 \hline
86 & 2410.211 & 0.650 & 893050.56 & 8183.592 & 2183 & 355 & 355 \hline
\end{tabular}
\end{table}

Fig. 4: Obfuscation results for AES-128, RISC-V and SHAKE-256 using TOTe.
sophisticated hardware trojans. For this goal, the adversary must recreate the bistream.

- The adversary goal might also be to identify the circuit intent, even in the presence of obfuscation. For this goal, the adversary does not need to recreate the bistream.
- The adversary has access to the GDSII file of the eASIC design. He or she is skilled in IC design and has no difficulty in understanding this layout representation. The adversary enjoys access to state-of-the-art CAD tools for this end.
- The attacker can recognize the standard cells, thus the gate-level netlist of the obfuscated circuit can be easily recovered [19].
- We assume that the attacker can differentiate between design inputs and reconfiguration pins [11], [20], thus being able to effortlessly identify all LUTs and their programming order.
- We assume the adversary can group the standard cells present in the static logic and convert them back into reconfigurable logic (i.e., LUT representation)\(^1\).

In order to evaluate the security hardness of eASIC, we propose two different attacks: one based on the structure of design and another based on the composition of known different circuits. Being so, we believe that the adversary can learn and extract information by exploiting the static portion of the design, including: (1) the frequency of masking patterns (2) the composition of different designs.

**B. Structural Analysis Attack**

**Goal:** by statistical analysis means, decrease the key search space and attempt to recover the bistream.

We recall again that the obfuscation engine of TOTe utilizes six variants of LUTs (\(\text{LUT}_1, \text{LUT}_2, \ldots, \text{LUT}_6\)) during the obfuscation phase. However, the majority of the LUTs are \(\text{LUT}_6\) due to the packing algorithm executed during FPGA implementation. Therefore, let us assume without loss of generality, that any FPGA-synthesized circuit contains only instances of \(\text{LUT}_{6x}\) for our security analysis.

As we mentioned before, the key search space is \(2^{64}\) for a single \(\text{LUT}_6\). But this assumption only holds if the FPGA synthesis is actually capable of exercising the entire key search space, which our results reveal that is far from possible. We have synthesized a large number of representative designs (>30) and counted how many unique \(\text{LUT}_6\) masking patterns appear in the corresponding netlists. Designs of varied complexity, size, and functionality where added until the combined number of unique masking patterns appears to settle, forming a set of \(m = 3376\) elements. This result alone, albeit being empirical, reduces the global search space from \(L_1\) to \(L_2\) as illustrated in Fig. 5.

\(^1\)This is a very generous concession since the static logic is repeatedly optimized during logic and physical synthesis. Nevertheless, we err on the side of caution and assume the adversary can achieve a perfect reconstruction of LUTs, which by itself is a reverse engineering problem.

In the next step, we targeted two processor designs in our statistical analysis: MIPS and RISC-V. For each circuit, we utilize tuples of \(\langle\text{pattern}, \text{frequency}\rangle\) for tracking how often masking patterns repeat. The tuples are referenced by integer identifiers and ordered by frequency. Our analysis reveals that the MIPS netlist has 776 unique LUTs and that there are very few outliers that occur more than 50 times. Similarly, for RISC-V, there are 628 unique LUTs and only 3 occur more than 100 times. In practice, if the attacker could know for a fact that the obfuscated circuits are indeed MIPS and RISC-V, the search space would shrink further. The shrunk search spaces are labeled \(L_3\) in Fig. 5. The question then becomes whether the static portion of the circuit is large enough for the adversary to be confident that the circuit under attack can be labelled as circuit \(C_1\), \(C_2\), or \(C_6\). We investigate this possibility by further analysing the behaviour of the frequency of masking patterns, as depicted in Fig. 6.

For this, we utilized polynomial trendlines for a portion of identifier of masking pattern, considering netlists generated by TOTe at 98\%, 95\%, 92\%, 89\%, and 86\% obfuscation levels. It is noteworthy that the trendlines become better frequency predictors as the obfuscation level is decreased. For RISC-V, in particular, the adversary can guess a small number outliers and the best guess (when obfuscation is 86\%) is far from the original frequencies (>100).

**C. Composition Analysis Attack**

**Goal:** identify the circuit by correlation to known circuits. This attack also exploits the frequency of the LUTs, but here we correlate entire designs (instead of pattern-frequency tuples) based on their composition. We consider that the attack is successful if the adversary is able to identify the circuit (see Threat model, 2nd bullet). Breaking the key is not necessary for this attack.

In this experiment, we performed correlation analysis for the well-known SHA-256 crypto core as shown in Fig. 7. The objective of this experiment is to analyze the leaked information from the static part of an obfuscated design against a database\(^2\) of circuits that are known to the attacker. We have obfuscated SHA-256 in the 70-100\% range and then correlated the static portion of the design with the database of known circuits. In Fig. 7, we show the results where the x-axis shows the obfuscation percentage and the y-axis shows correlation (right) and number of unique LUTs (left). For this circuit, three regions of

\(^2\)We assume the adversary can obtain samples of open source cores from repositories and execute FPGA synthesis on them with his tool of choice.
TABLE II: Results for the implementation of SHA-256 for different obfuscation levels

| Obfuscation | Density | Area (μm²) | Freq. (MHz) | Leakage (mW) | Dynamic Power (mW) | Total Power (mW) | # LUT | # Buffer | # Comb. | # Inv. | # Sequential |
|-------------|---------|------------|-------------|--------------|-------------------|-----------------|-------|----------|--------|--------|--------------|
| FPGA        | 100%    | --         | 77          | 158          | 33                | 191             | 2238  | --       | --     | --     | 1830         |
| TOTe        | 100%    | 46%        | 1412227.08  | 166.7        | 17.01             | 257.23          | 274.24 | 2238     | 623.4  | 82756  | 4686         | 103128       |
| TOTe        | 90%     | 45%        | 1274690.16  | 179.6        | 15.34             | 246.87          | 262.21 | 2015     | 5411   | 83452  | 4188         | 94876         |
| TOTe        | 85%     | 46%        | 1215328.32  | 200          | 14.62             | 263.20          | 277.82 | 1904     | 5249   | 79626  | 3972         | 90420         |
| TOTe        | 80%     | 54%        | 1135752.20  | 200          | 13.93             | 248.84          | 262.77 | 1792     | 7699   | 74000  | 3755         | 83790         |
| ASIC       | 0%      | 71%        | 43097.40    | 500          | 0.525             | 6.405           | 6.93   | 0        | 119    | 3165   | 128         | 1806          |
| ASIC       | 0%      | 71%        | 60563.52    | 769          | 0.862             | 32.69           | 33.55  | 0        | 336    | 3165   | 128         | 1806          |

Fig. 7: The correlation of SHA-256 versus numerous other designs.

interest can be defined: 97-100% (no correlation), 86-96% (strong correlation to another circuit), and 70-85% (correlation to itself).

This attack reveals that if the adversary goal is solely to identify the circuit’s intent, eASIC can be as vulnerable as an ASIC design. To mitigate this undesirable effect, obfuscation levels should remain relatively high. Otherwise, if the obfuscation lies between 70 and 84%, the search space would shift from L3 to L4 as shown in Fig. 5. This is a key finding of our manuscript and will guide our design choices when implementing the physical synthesis of eASIC designs in the section that follows.

V. PHYSICAL SYNTHESIS FOR EASIC

This section contains the physical implementation results for an obfuscated SHA-256 core. We have selected SHA-256 as it is popular and widely used in cryptography. The variants of the design with different obfuscation levels are implemented with the aid of the LUTs defined in Section III-A. The results obtained after implementation are focused on performance vs. area trade-offs for the 80-100% obfuscation range as determined by the security analysis of Fig. 7. Initially, we synthesized and implemented the SHA-256 core on FPGA. This implementation achieves a frequency of only 77 MHz (for reference, the Kintex-7 family is produced on a 28nm CMOS technology). To start the analysis, we select 100% obfuscation as a baseline design because it is fully reconfigurable and somewhat analogous to an FPGA design.

The implementation results for 0%, 80%, 85%, 90%, and 100% obfuscation are listed in Table II. These are obtained after physical synthesis and are for the worst process corner (SS) and a nominal temperature of 25°C. It is noteworthy that the performance of the design is increasing as we decrease the level of security. This behaviour is clearly depicted in the fourth column of Table II and matches the goal we set from the beginning: to trade-off power for security. Here we also show that performance saturates rather quickly, as predicted by TOTe in Section III-B. The area of the design is proportional to the obfuscation level which means that increasing the security of design will cause area overhead. As we only exploit LUT primitives for promoting obfuscation, the number of LUTs increases with the obfuscation level. In the same manner, leakage and dynamic power figures are proportional to security as reconfigurable logic is less efficient than static logic. The results obtained from the physical synthesis justify trade-offs and the last five columns of Table II show the resource requirements.

The first three panels (a, b and c) of Fig. 8 illustrate the layouts for 80%, 85% and 90% obfuscation levels. The dimensions of the layouts are indicated on the bottom and left sides of each panel. All the six variants of LUTs are highlighted with different colors and the static logic part of eASIC is highlighted in red – notice that, as expected, the design remains primarily a sea of LUTs - the reconfigurable logic part. The majority of those LUTs are LUT6, thus the layouts appear to be dominated by yellow boxes. The placement of LUTs is done by the ASIC placement tool. For this, we modified the LUT macros to behave as regular standard cells. Then, the placer exploits its optimization strategies to place each LUT efficiently. From a magnified view, the mixed structure of LUT macros and standard cells clearly depicts the placement pattern, and that spaces between macros are usually filled with standard cells (static logic part). Notice how the LUT macros align with the standard cell rows, allowing for the entire design to have a uniform power rail and power stripe configuration.

VI. COMPARISON AND DISCUSSION

From the many results, we conclude that obfuscation levels should be relatively high to achieve a considerable security, thus the majority of the eASIC logic should be reconfigurable logic (i.e., LUTs). Having a large portion of reconfigurable logic provides an opportunity to correct the issues/bugs that could be easily fixed during the reconfiguration phase. Naturally, there are limitations since a portion of the system consists of static logic and cannot be modified. This limitation could be eased if the eASIC layout were to include spare LUTs. These same spare LUTs could serve as decoy LUTs for preventing the composition attack described in Section IV-C, but at a cost in area, power, and likely timing as well. To some degree, those spare LUTs could also be used to make side-channel attacks less successful. These possibilities are not studied in this manuscript but remain promising concepts for future work.

Our eASIC device presents a largely regular structure upon visual inspection. This effect can be modulated if it proves to be effective against a reverse engineering adversary. For instance, we could have mapped LUTs of all sizes to LUT6, which would increase the layout regularity (i.e., making it only red and yellow). Similarly, LUTs could have been laid out in a perfect grid fashion. These two design choices are relatively simple to implement in physical synthesis but carry overheads that we deemed not advantageous, even if they make perfect sense for an FPGA device.
A recent trend in obfuscation research is the use of embedded FPGA (eFPGA) [21], [22]. A very similar approach is also found in [23], where authors perform obfuscation with transistor-level granularity. While there are advantages to this practice, it has been used selectively to only protect key portions of a design and therefore keep the performance penalty as low as possible. The challenge is in determining which portions of the circuit merit protection and which ones do not. Our eASIC approach bypasses this question almost completely by only revealing (portions of) critical paths when they are selected to become static logic, which we consider an advantage if the ASIC-equivalent performance can be sacrificed. In [24], the authors present a top-down methodology to implement ASICs with eFPGAs. Their designs share many of the advantages of our eASIC solution while presenting more regularity than our designs (they make use of logic tiles as in commercial FPGAs). Our tile-free design trades this regularity for performance as evidenced by the layout in Fig. 8.

VII. CONCLUSIONS

In this paper, we have developed a custom tool (TOTe) that obfuscates a design and transforms it into an eASIC device. Our eASIC solution contrasts with the current practice of eFPGA for obfuscation and this is not by coincidence: our experimental results show that obfuscation rates have to be high to protect not only the bitstream but also the design’s intent. This is a key finding of our research which we hope can help to steer current obfuscation practices in the literature. Our findings are also validated in a commercial physical synthesis tool with industry-strength timing and power analysis, from which we confirm that TOTe’s trade-off analysis is sufficiently accurate. Our future research will focus on the ideas put forward in our discussion, where we argue that eASIC has many benefits beyond obfuscation.

REFERENCES

[1] IC Insights, “Semiconductor units forecast to exceed 1 trillion devices in 2021.” [Online]. Available at: https://www.icinsights.com/news/bulletins/Semiconductor-Units-Forecast-To-Exceed-1-Trillion-Devices-Again-In-2021/.

[2] S. M. Ben, “Security challenges and requirements for industrial control systems in the semiconductor manufacturing sector,” 2012. [Online]. Available: https://csrc.nist.gov/CSRC/media/Presentations/Security-Challenges-and-Requirements-for-Control-S/images-media/presentation-3_salem.pdf

[3] M. Yasin et al., “Removal attacks on logic locking and camouflaging techniques,” IEEE Transactions on Emerging Topics in Computing, vol. 8, no. 2, pp. 517–532, 2020.

[4] R. P. Cocchi et al., “Circuit camouflage integration for hardware ip protection,” in DAC, 2014, pp. 1–5.

[5] M. Li et al., “Provably secure camouflaging strategy for ic protection,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 38, no. 8, pp. 1399–1412, 2019.

[6] K. Zamiri Azar et al., “Threats on logic locking: A decade later,” in GLSVLSI ’19, 2019, p. 471–476.

[7] M. Yasin et al., “On improving the security of logic locking,” IEEE TCAD, vol. 35, no. 9, pp. 1411–1424, 2016.

[8] J. Sweeney et al., “Latch-based logic locking,” in 2020 IEEE HOST, 2020, pp. 132–141.

[9] T. D. Perez et al., “A survey on split manufacturing: Attacks, defenses, and challenges,” IEEE Access, vol. 8, pp. 184013–184035, 2020.

[10] J. Rajendran et al., “Is split manufacturing secure?” in 2013 DATE, 2013, pp. 1259–1264.

[11] P. Subramanyan et al., “Evaluating the security of logic encryption algorithms,” in 2015 IEEE HOST, 2015, pp. 137–143.

[12] B. Liu et al., “Embedded reconfigurable logic for asic design obfuscation against supply chain attacks,” in 2014 DATE, 2014, pp. 1–6.

[13] H. Mardani Kamali et al., “Lut-lock: A novel lut-based logic obfuscation for fpga-bitstream and asic-hardware protection,” in 2018 IEEE ISVLSI, 2018, pp. 405–410.

[14] S. D. Chowdhury et al., “Enhancing sat-attack resiliency and cost-effectiveness of reconfigurable-based circuit obfuscation,” in 2021 IEEE ICCAS, 2021, pp. 1–5.

[15] K. E. Murray et al., “Vtr 8: High-performance cad and customizable fpga architecture modelling,” ACM Transactions on Reconfigurable Technology and Systems, vol. 13, no. 2, 2020.

[16] H. Hsing, “Aes-128,” 2013. [Online]. Available: https://opencores.org/projects/tiny_aes

[17] Z. U. Abideen et al., “TOTe (Tuneable Design Obfuscation Technique using eASIC),” 2021. [Online]. Available: https://github.com/Centre-for-Hardware-Security/eASIC

[18] G. Kolhe et al., “Security and complexity analysis of lut-based obfuscation: From blueprint to reality,” in 2019 IEEE ICCAD, 2019, pp. 1–8.

[19] R. Torrance et al., “The state-of-the-art in ic reverse engineering,” in CHES 2009, C. Clavier et al., Eds., 2009, pp. 363–381.

[20] M. Yasin et al., “Provably-secure logic locking: From theory to practice,” in Proceedings of the 2017 ACM SIGSAC Conference on Computer and Communications Security, 2017, p. 1601–1618.

[21] B. Hu et al., “Functional obfuscation of hardware accelerators through selective partial design extraction onto an embedded fpga,” in GLSVLSI ’19, 2019, p. 171–176.

[22] J. Chen et al., “DECOY: DEflection-Driven HLS-Based Computation Partitioning for Obfuscating Intellectual Property,” in 2020 IEEE DAC, ser. DAC ’20, IEEE Press, 2020.

[23] M. M. Shihab et al., “Design obfuscation through selective post-fabrication transistor-level programming,” in 2019 DATE, 2019, pp. 528–533.

[24] P. Mohan et al., “Top-down physical design of soft embedded fpga fabrics,” in The 2021 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, 2021, p. 1–10.