A High Step-Up PWM Non-Isolated DC-DC Converter With Soft Switching Operation

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ABSTRACT A high step-up PWM non-isolated dc–dc converter with soft switching is proposed in this paper. The converter has minimum auxiliary elements to achieve high power density and high voltage gain. The ZVS operation of the main power switch results in negligible capacitive turn-on losses. Since the duty cycle of the auxiliary switch is narrow and its operation is under ZCS condition, the losses that the auxiliary circuit imposes are not significant. Also, all the diodes are operated under soft-switching conditions solving the reverse recovery problem. All the inductors are coupled on only one magnetic core, reducing size and conduction losses. Compared to the hard switched counterpart, the electromagnetic interference of the proposed converter is reduced. Furthermore, the output voltage of the proposed converter is controlled by an integral sliding mode control strategy during the load variations. Also, the proposed integral sliding mode control strategy has been compared with the PI control strategy, improving the transient response and the robustness under load variations while the switching frequency is constant. The effectiveness and accuracy of the proposed converter are verified by practical laboratory results which are obtained from a 250W prototype.

INDEX TERMS High step-up, soft-switching, ZVT, ISMC, PWM, photovoltaic, renewable energy, solar systems.

I. INTRODUCTION

Recently, the massy usage of fossil fuels effects on the environment. This is an important issue which causes to find renewable energy sources to generate electrical energy [1], [2]. The solar system is one of the suggestive players in renewable energy sources because of the emission-free and clear quality [3]–[6]. One of the exciting topics is to employ the new power electronic circuits whose high power density, high efficiency, and broad conversion ratio are their trends [7]. The development of high step-up converters has become critical for converting the low voltage of photovoltaic (PV) panels to a desired voltage level for grid-connected applications. Generally, many high step-up converters are famous for being used in electronic devices such as renewable energy sources like photovoltaic and fuel cell systems. Moreover, the high-intensity-discharge (HID) lamps, the fuel cells, the uninterruptible power supply (UPS), and the communication power system’s front-end stage are some of the applications that high power-density and high step-up non-isolated converters are used [8], [9].

To obtain the high voltage gain by using the conventional boost converter, the high duty cycle should be used for the power switch. Therefore, the current level through the converter rises, so the voltage drop increases which decrease the efficiency of the converter. Moreover, the high-priced power switches should be chosen. In order to solve these problems and achieve high voltage gain, many techniques are introduced, such as the coupled inductors, switched-capacitors, and multiplier circuits. Nevertheless, in the switched-capacitors and the multiplier circuits, the number of capacitors and the semiconductors are high, so the conduction losses and the switching losses in these topologies increase. Also, the power density of the converter is reduced. The coupled inductor technique, which is used in the proposed converter, is one of the most popular methods to increase the voltage gain, but by using more than one core, the size and volume of the converter are increased [10], [11].

In the switching converters, the size and the weight of the reactive components should be downgraded to reduce the costs of the converter [10], [11]. To achieve this, the
operation should be on high switching frequency [12]; therefore, in high-frequency hard-switched converters, the losses of switching and the EMI are increased, resulting in lower efficiency in comparison with the soft switched converters due to the sudden changes of voltage and current of the switches [11], [13]. To overcome these drawbacks, various passive [14], [15] or active [16], [17] soft switching techniques are proposed. The resonant converters are a kind of soft switched converters in which no auxiliary switch added to the structure. But for controlling the output power in these converters, the switching frequency should not vary, so cannot achieve the optimum design of the magnetic elements. The active clamp technique makes the power switches operate under ZVS conditions with no capacitive turn-on losses. However, in the active clamp circuit, the circulating current in the auxiliary circuit is high, so the conduction losses rise; thus, the efficiency decreases. Moreover, the Zero-Current-Transition (ZCT) and the Zero-Voltage-Transition (ZVT) are two commonly used methods of the soft switching active techniques, in which an auxiliary circuit with at least one power switch is attached to the converter to provide soft transition conditions [18]–[20]. In the ZVT technique, which used in the proposed converter, an auxiliary circuit is added to the converter, after the main switch, in parallel with the structure. The ZVT circuit in the proposed converter consists of a switch, a diode, an inductor, and a coupled inductor. Using the ZVT circuit makes the main switch operates under the ZVS soft-switching condition with no capacitive turn-on losses for the main switch. Also, there are no switching losses for the MOSFETs because of the soft-switching conditions. Furthermore, because of the inductor, which series with the auxiliary switch, the auxiliary switch operates under the ZCS condition. The ZCS operation of the MOSFET leads to narrow switching losses of the converter. Further, the circulating current and conduction losses of the auxiliary circuit is reduced due to the low duty cycle. Moreover, using the ZVT technique makes the converters operate similar to the regular Pulse-Width-Modulation (PWM) converters [13] which the designation of their controller is simple.

In this paper, a new PWM high step-up converter is presented, which illustrated in Fig. 1. In this structure, the soft-switching conditions is obtained for all the semiconductors by using the ZVT circuit while there are no extra stresses on the MOSFETs. The soft-switching conditions are also achieved for all the diodes, solving the reverse recovery problem and decreasing the power losses. The high voltage conversion of 30-500V makes the circuit suitable for photovoltaic applications. In order to improve the efficiency, all the inductors are coupled on only one magnetic core, as shown in Fig. 2. Also, a higher power density is achieved compared to other converters, which have more than one magnetic core.

To guarantee the stability and adjust the output voltage to the required value under the load variations, the output voltage of the proposed converter can be controlled by Sliding Mode Control (SMC) technique, which is more attractive than regular PWM controllers used in [11] and [14]. The advantages which make the SMC family more suitable compared to the proportional-integral (PI) controller are the stability against parameter variations, disturbances rejection, fast dynamic responses, and inherent robustness of tracking control [21], [22]. On the other hand, there are also disadvantages. One of the crux disadvantages of applying SMC on dc-dc converters is design filter circuit difficulty due to the operation frequency variation [21]. To achieve constant frequency operation, the PWM converters are used in the related applications, but the Steady-State Error (SSE) are increased. Another disadvantage of the SMC is need a high-switching frequency for control action which results in the so-called chattering effect [23], [24]. In order to solve these drawbacks, a kind of SMC called Integral Sliding Mode Control (ISMC) is proposed [22] and [24]. The ISMC has strong robustness under load variations. This property caused to fix the output voltage level of the converter to the desired value. In this paper, an ISMC strategy is used for adjusting the output voltage of the proposed converter to the required value under the load variations. To validate the analysis, a practical prototype is implemented on a SPARTAN-6 XC6SLX9 FPGA chip which its clock manager is developed in comparison with the SPARTAN-3 FPGA chip which used in [21] and [23], so the processing speed has been improved and resulted in less chattering effects.

Firstly, the main contribution of the proposed converter is the modular ZVT auxiliary circuit which there is no need for new auxiliary circuit for the converter with extra phases. Secondly, the circulating current in the proposed auxiliary circuit is low because the short turned on time of the auxiliary switch. According to the soft-switching
condition which is provided for the auxiliary switch and the auxiliary diode operation, there is no significant losses of the auxiliary circuit imposing to the proposed converter. Moreover, in order to create a voltage source on the auxiliary circuit, a tertiary coupled inductor is applied on the main core of the proposed converter which decreases the volume and increases the power density. Moreover, the soft-switching condition is achieved for a wide range of the load variations.

In the following, the proposed converter and the soft switching operating principles are presented in section II. Section III has explained the ISMC design and its comparison with the PI controller. Moreover, section IV presents the experimental results that verified the soft-switching conditions, the fixed output voltage on load variations, and the conduction EMI comparison between the soft switched converter and the hard-switched counterpart. Finally, the conclusion is written at the end of the paper in section V.

II. OPERATING PRINCIPLES AND DESIGNATIONS

A high step-up PWM non-isolated DC-DC converter with soft switching operation is proposed. The converter comprised a ZVT circuit, a clamp circuit, and a charge-pump capacitor. The ZVT auxiliary circuit includes an auxiliary switch (S_a), an auxiliary diode (D_a), an auxiliary inductor (L_a), and a tertiary inductor (L_3). This auxiliary circuit is added to the converter in parallel. A clamp circuit is used identically in the output, after the ZVT circuit, which solves most efficiency issues. The clamp circuit includes two diodes named D_1 and D_2 and a clamp capacitor named C_c. Eventually, the charge-pump capacitor (C_{cp}) is located crosswise to the coupled inductors (L_1, L_2), which increases the voltage gain. Further, the primary inductor (L_1) current is continuous because of adding this charge-pump capacitor. So, the Continuous-Conduction-Mode (CCM) is available for this converter. Also, according to Fig. 2, the L_1 inductor, added by the auxiliary circuit, is on the magnetic core, which contains the two primary and secondary inductors (L_1 and L_2). Using only one magnetic core decreases the total volume and the power losses of the converter, which leads to higher power density and efficiency, in comparison with other converters which contain more than one core.

A. OPERATING PRINCIPLES

The operation is on eight modes for every switching cycle at full-load. Each mode expresses the proposed converter’s accurate performance. Figure 3 and Fig. 4, illustrate the theoretical waveforms and the counterpart circuit for each mode, respectively. In Fig. 3, the “V_{GS(Sm)}” is the gate-source pulse of the main switch, the “V_{GS(Sa)}” is the gate-source pulse of the auxiliary switch, the “I_{Sm}, V_{Sm}” is the drain-source current and voltage of the main switch, and the “I_{Sa}, V_{Sa}” is the drain-source current and voltage of the auxiliary switch. Also, the current and voltage of the D_1, D_2, and D_0 diodes were also illustrated in Fig. 3 by “I_{D1}, V_{D1}”, “I_{D2}, V_{D2}”, “I_{Do}, V_{Do}” respectively.

If the N_1 through N_3 be the turn’s number of L_1 through L_3, respectively, the turns ratio n and m are equal to:

\[
\begin{align*}
  n &= \frac{N_2}{N_1} \\
  m &= \frac{N_3}{N_1}
\end{align*}
\]  

Prior to the first mode, all the MOSFETs are turned off, and the snubber capacitor’s voltage is reached to its maximum. Also, only the output diode is conducting, and the other diodes are off. For the analysis, it is considered that:

- All the semiconductors are assumed to be ideal.
- Output and clamp capacitors are chosen spacious; so, their voltages are constant during the switching cycle.

1) MODE 1 [t_0, t_1]

Prior to turn on the main switch, S_m, the auxiliary switch, S_a, should be turned on for discharging the snubber capacitor C_c. Therefore, this mode commences, and the S_a turns on with the ZCS condition because of the L_1 inductor series. The auxiliary switch S_a current can be calculated as follows, where D is the duty cycle of the S_m:

\[
  i_{sa}(t) = \frac{m V_{in}}{(1 + n) L_a} \frac{4 + 2 n - (1 + n) D}{1 - D} (t - t_0)
\]
When the $S_a$ is turned on, the $D_a$ diode turns on with the ZCS condition too. Also, the $L_a$ inductor’s current increases, and the output diode $D_o$ current decreases, both linearly, so the ZCS turn-off for output diode $D_o$ is provided. The current of the $D_o$ diode reaches zero and this mode ends.

2) MODE 2 $[t_1, t_2]$

The output diode turns off, and the snubber capacitor $C_s$ is discharged via resonance with the $L_a$ inductor. Therefore, the voltage of $C_s$ is decreased resonantly to zero, so the ZVS condition is obtained for turning the main switch on is
provided. The resonantly decreased voltage of the snubber capacitor $C_s$ can be derived as below, where $\omega$ is the angular frequency.

$$V_{Cs}(t) = V_{Cs'} \max \cos(\omega(t - t_0))$$ (3)

$$V_{Cs'} \max = \frac{V_{out}}{n + 2}$$ (4)

$$\omega = \frac{1}{\sqrt{L_aC_s}}$$ (5)

Then, the body diode of the main switch becomes forward biased and clamps its voltage to zero level, and this mode ends.

3) MODE 3 [$t_2$, $t_3$]

The body diode becomes forward biased, this mode begins, and then the $S_m$ could be turned on under ZVS condition. Because of the constant voltage difference between the two ends of $L_m$, which is defined as “$nV_{in}$”, the current of $L_m$ is decreased linearly. Then, the body diode current is moved to the main switch.

4) MODE 4 [$t_3$, $t_4$]

The current of the main switch $S_m$ rises linearly to magnetizing current and the main switch is turned on with the ZVS condition. Also, the $L_a$ inductor’s current reduces gradually to zero, and the $D_a$ diode turns off with the ZCS condition. Afterward, the auxiliary switch $S_a$ can be turned off under ZCS condition, too.

5) MODE 5 [$t_4$, $t_5$]

The output diode $D_o$ is off, and the main switch $S_m$ is on. Thus, the magnetizing inductor, $L_{m}$, is charged. The voltage of the $L_2$ inductor can be calculated as:

$$V_{L_2} = nV_{in}$$ (6)

Moreover, the output current is supplied by the capacitor $C_o$ while the $D_2$ diode conducts under ZCS condition, and the capacitor $C_{cp}$ is charged from the paths of main switch $S_m$, clamp capacitor $C_c$ and $D_2$ diode. This mode continues until the main switch $S_m$ turns off.

6) MODE 6 [$t_5$, $t_6$]

The main switch ($S_m$) is turned off. Also, its voltage rises gradually due to the snubber capacitor paralleled with it. Thus, the main switch $S_m$ turns off with the ZVS condition. The voltage of the main switch can be derived as:

$$V_{Cs}(t) = V_{Sm}(t) = \frac{i_{Lm}}{C_s}(t - t_0)$$ (7)

$$V_{Sm'} \max = V_{Cs'} \max = \frac{V_{out}}{n + 2}$$ (8)

where $i_{Lm}$ is the magnetizing current. Also, the $D_2$ diode’s current is reduced to zero, then the clamp diode, $D_1$, turns on, and this mode ends.

7) MODE 7 [$t_6$, $t_7$]

The $D_1$ turns on with the ZVS condition. Then, the $L_a$ inductor’s energy is moved to the clamp capacitor $C_c$. The $L_a$ inductor’s voltage is derived as below:

$$V_{L_a} = V_{in} \left(\frac{2}{1 - D} \right)$$ (9)

where $D$ is the main switch duty cycle.

The $D_2$ diode turns off under the ZVS condition, and the $D_o$ turns on with the ZCS condition. Also, the current of the output diode $D_o$ is as follows where $D$ is the main switch duty cycle, and $i_{Lm}$ is the magnetizing current:

$$i_{D_o}(t) = \frac{V_{in}}{L_a} \left(\frac{2}{1 - D} \right) (t - t_0)$$ (10)

Furthermore, the magnetizing inductor’s energy is discharged in the output, and the $D_1$ turns off with the ZCS condition.

8) MODE 8 [$t_7$, $t_8$]

The $D_1$ diode is turned off. The magnetizing inductor’s energy moves from the output diode $D_o$ to output. This mode continues until the auxiliary switch $S_a$ is turned on.

B. DESIGN PROCEDURE

The converter’s voltage gain is acquired by a KVL between the output, clamp capacitor, and the secondary inductor as follow, where $D$ is the duty cycle, and $k$ is the effect of the leakage inductor.

$$Gain = \frac{V_{out}}{V_{in}} = \frac{2}{1 - D} + D(1 - k)(n - 1)$$ (11)

Without considering the leakage inductance energy, the voltage gain is calculated as follow:

$$Gain = \frac{V_{out}}{V_{in}} = \frac{2 + n}{1 - D}$$ (12)

To obtain the snubber capacitor ($C_s$) value, the converter is checked in Mode 2 when the $C_s$ capacitor is discharged via resonance with the $L_a$ inductor. The $C_s$ capacitor must be spacious enough to decrease the stresses of the main switch $S_m$. The designation of the $C_s$ capacitor in this paper is like a regular snubber capacitor, where the main switch voltage’s rise time and the magnetizing inductor current are named by $t_s$ and $i_{Lm}$, respectively. The snubber capacitor $C_s$ value can be acquired as below:

$$C_s = \frac{i_{Lm}t_s}{2V_{es} - V_{in}}$$ (13)

As well as the $C_s$ capacitor is attained, the $L_a$ inductor is calculated by the angular frequency (5), where $f_{sw} = 1/T$ is the switching frequency.

$$L_a = \frac{(2\pi f_{sw})^2}{C_s}$$ (14)
Moreover, the $C_{\text{cp}}$ is a charge-pump capacitor whose voltage value can be derived by a KVL between the charge-pump capacitor, the clamp capacitor, and the secondary inductor in Mode 5 operation. The $C_{\text{cp}}$ voltage is calculated as:

$$V_{C_{\text{cp}}}(t) = \frac{V_{\text{in}}(nk + 2 + D(1 - k)(n - 1))}{2(1 - D)} \quad (15)$$

Moreover, the clamp capacitor voltage is also computed by this KVL as follow:

$$V_{C_{\text{c}}}(t) = \frac{V_{\text{in}} + D(1 - k)(n - 1)}{1 - D} \quad (16)$$

The characteristics of the presented converter are provided in Table 1 compared to the other related converters. According to this table, the proposed structure has fewer components and MOSFETs in comparison with the converters in [26], [29], [30], and [32], reducing weight, size, and cost, and improving the power density of the converter. Also, the voltage gain of the proposed converter is higher than the converters in [25] and [26]. Although the converters in [27], [28], and [32] have a higher voltage gain in comparison with the proposed structure, the converter presented in [29] operates under ZCS condition.

The ZCS condition applied to the power switches of the converters in [25] and [29] raises the capacitive turn-on losses of the converter. Further, the converters in [27], [28], and [30] operate under hard-switching condition. The converters in [27] and [30] have 18 total component counts resulting in less power density and higher costs compared to the proposed structure. Moreover, although the voltage gain of the converter in [32], which has three voltage multiplier stages, is higher than that of the proposed converter, the proposed converter has fewer components. Furthermore, the active clamp technique is used for the converter in [32] for making the MOSFETs operate with the ZVS condition. Also, this technique increases the current flow and the current stress of the main switches, while its experimental results illustrate the current of the main switch is almost 50A for the 500W prototype. In addition, the switching operation in the converter [28] is hard-switching, so the switching losses and the EMI of the converter are high. It is noted that the A in Table 1 is $n(2 - d)(M - 1 - d(M - k) + (1 - d)$. The $M$ is the number of stages and $k = 1$ is the number of the diode-capacitor Voltage Multiplier (VM) stages of the converter.

Moreover, the voltage and current stresses of the proposed converter and the converters introduced in [25]–[30] and [32] are written in Table 2. The voltage stress of the converters in [25] and [26] is higher than the voltage stress of the proposed converter, while the current stress of the proposed converter is lower than that of the converters in [27]–[32]. It is noted that the ESR in Table 2 is the equivalent series resistance of the capacitors. For better understanding, the comparison between the voltage gains of the converters in [25]–[32] is plotted in Fig. 5.

### Power Losses

This section presents the effects of the non-ideal components of the proposed converter on the total losses. By considering the non-ideal components, the conduction losses of the MOSFETs and the diodes, the conduction losses of the coupled inductors, and the conduction losses of the capacitors are calculated. Because of the ZVS condition provided for the main switch, it has no capacitive turn-on losses. However,
the capacitive turn-on losses of the auxiliary switch are considered. The core losses are few enough, which is ignored. The conduction losses of the power switches depend on the drain-source on resistance and the root-mean-square (RMS) current of the switches. The conduction losses of the MOSFETs are calculated as:

$$P_{\text{Conduction}} = R_{DS} \left( I_{\text{RMS}} R_{\text{Sm}}^2 + I_{\text{RMS}} R_{\text{Sa}}^2 \right) = (8 \times 10^{-3} (7^2 + 0.9^2) = 0.4W$$

Because of the ZVS condition, which is provided for the main switch, its capacitive turn-on losses equal zero, and there are only the capacitive turn-on losses of the auxiliary switch, which are calculated as follows:

$$P_{\text{C.T.O.Sa}} = \frac{1}{2} C_{\text{out.Sa}} V_{\text{out.Sa}}^2 I_{\text{sw}} = \frac{1}{2} \times 400 \times 10^{-12} \times 440^2 \times 100 \times 10^{-3} = 3.872W$$

The conduction losses of all the diodes depend on their forward voltage drops and average currents flowing through them, which are obtained as follows:

$$V_f (I_{\text{avg.D1}} + I_{\text{avg.D2}} + I_{\text{avg.Da}}) = (975 \times 10^{-3}) \times (0.7 + 1 + 0.9) = 2.535W$$

$$P_{\text{Conduction}}' = V_f I_{\text{avg}}' D = 2.4 \times 0.6 = 1.44W$$

The conduction losses of the inductors are also considered because they have parasitic resistances. The losses of the inductors are calculated as follows:

$$P_{\text{Inductors}} = \frac{1}{2} L_1 I_{\text{RMS}} L_1^2 + \frac{1}{2} L_2 I_{\text{RMS}} L_2^2 + \frac{1}{2} L_3 I_{\text{RMS}} L_3^2$$

$$+ \frac{1}{2} L_4 I_{\text{RMS}} L_4^2 = 0.13 + 0.05 + 0.13 + 0.003 = 0.313$$

The capacitors losses are considered, which depend on their resistance and current, as follows:

$$P_{\text{Capacitors}} = R_{C1} I_{\text{RMS}} C_1^2 + R_{C2} I_{\text{RMS}} C_2^2 + R_{C1} I_{\text{RMS}} C_0^2 = 0.13 + 0.20 + 0.32 = 0.65W$$

According to the above calculations, the total calculated power losses of the proposed converter is 9.21W for the 250W full-load prototype. Thus, 96.32% of calculated efficiency is achieved.

### D. AUXILIARY CIRCUIT DERIVATION

A new ZVT auxiliary circuit is applied to the proposed converter, which contains the minimum number of elements to provide soft-switching conditions for the power switches. A new ZVT auxiliary circuit is applied to the proposed converter which contains the minimum number of elements to provide soft-switching conditions for the power switches. The leakage inductance of the tertiary coupled inductor which is located on the ZVT auxiliary circuit series with the La inductor, so there is resonance between the inductors and the snubber capacitor. Thus, the ZVS operation for the main switch is provided. Further, the auxiliary switch of the converter is operated under ZCS condition because of the La inductor, which is series with it. So, the auxiliary circuit does not impose significant losses to the proposed converter because of the short duty cycle of the auxiliary switch and the soft-switching operation of both power switches.

The proposed auxiliary circuit has a simple operation. As analyzed in section II, to turn the main switch on under ZVS condition, the auxiliary switch should turn on sooner than the main switch. So, the auxiliary inductor La resonances with the snubber capacitor. The voltage of the main switch reduces gradually to zero; then the main switch can be turned on under ZVS condition. The auxiliary inductor of La, which series with the auxiliary switch, increases and decreases their current slowly. So the ZCS condition for turning on and off instants is provided for the auxiliary switch.

The proposed ZVT auxiliary circuit could apply to other related high step-up converters (single-phase and double- phases). For instance, in Fig. 6, a double phases (Fig. 6(a)) and a single-phase (Fig. 6(b)) high step-up converters are presented, which have the higher voltage gain and lower voltage stress on the switches compared to the proposed converter. However, the total component count of these converters is high, reducing the power density and increasing the total cost, weight, and size of the converter. This paper,
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III. ISMC DESIGN

In this section, a controller is designed based on ISMC to adjust the output voltage of the proposed converter to the required level under load variations. The power switches’ duty cycles are changed with the controller while the load varies. The ISMC strategy has more benefits compared with the PI system. Some of these advantages are fast response, guarantee stability, and robustness in the face of uncertainties and environmental situations. Moreover, the proposed control method operates on the wide range of the quiescent point, while the PI controller operation depends on the quiescent point strongly. The tuning of the coefficients of the PI controller is also complicated. Furthermore, the chattering effect and the steady-state error is minimized by this controller ability. In the following, the design procedure of the proposed control method is explained.

A. SLIDING SURFACE

To design the proposed controller based on ISMC strategy, sliding surface \( s \) is considered as:

\[
\begin{align*}
  s &= e(t) + K \int e(t) dt + e(0), \quad K > 0 \quad (23) \\
  e &= V_{\text{ref}} - V_{\text{out}} \quad (24)
\end{align*}
\]

where \( e = V_{\text{ref}} - V_{\text{out}} \) is the voltage error. Also, \( V_{\text{ref}} \) and \( V_{\text{out}} \) are the reference and the actual value of the converter’s output voltage, respectively. \( K \) is the positive constant gain suitable for the system transient requirement. The \( s = 0 \) represents the accurate tracking of the converter’s voltage. Moreover, the system states attain the sliding surface and then slide along the surface. Thus:

\[
  s = \frac{ds}{dt} = 0
\]

Based on (25), derivatives of \( s \) equal zero, which gives:

\[
  \frac{de}{dt} = -Ke
\]

The aforementioned equation ensures the voltage error converges to zero. Since (23) equals zero initially, the converter’s output voltage gathers asymptotically to the base with a time constant of \( 1/K \).

B. SMC LAW

The SMC design is employed in the systems to force the state variables to the surface. In the proposed control method, the output voltage reference of the converter is generated as the input of the PWM module.

To derive the conditions on the control law, a candidate Lyapunov function is employed, which drives the state to the sliding surface. The “\( W \)” is the Lyapunov function which is introduced as:

\[
  W = \frac{1}{2} s^2 > 0
\]

Time derivative of the candidate Lyapunov function (27) is obtained:

\[
  \frac{dW}{dt} = s \frac{ds}{dt}
\]

With differentiating \( s \) by (23), the motion projections of the system (12) on sliding surface \( s \) are derived, as:

\[
  \frac{ds}{dt} = \frac{de}{dt} + Ke = -\frac{dV_{\text{out}}}{dt} + K (V_{\text{ref}} - V_{\text{out}})
\]

According to (12), \( dV_{\text{out}}/dt \) is calculated as:

\[
  \frac{dV_{\text{out}}}{dt} = -\frac{(2 + n)}{(1 - D)^2} V_{\text{in}} = -\frac{V_{\text{out}}}{(1 - D)}
\]

Substituting (30) into (29) yields:

\[
  \frac{ds}{dt} = F + QV_{\text{out}}
\]

where, \( F = K V_{\text{ref}} \) and \( Q = (1/(1 - D)) - K \).

The switch control law is chosen to form \( dW/dt < 0 \) for \( S \neq 0 \). Therefore, the control law is introduced by (32) as:

\[
  u = -Q^{-1}[F + U^*]
\]

where,

\[
  U^* = K_c \text{sat}(s)
\]

The \( K_c \) is the positive control gain.
C. THE STABILITY PROOF

For making the sliding surfaces stable, the time derivative of the Lyapunov function (28) must be a negative-definite function:

\[
\frac{dW}{dt} = -s(K_c \text{sat}(s))
\]  

(34)

Since \(s\text{sat}(s)\) is positive, \(dW/dt\) is absolutely negative. Since \(W > 0\) and \(dW/dt < 0\), \(s\) reaches zero asymptotically. Accordingly, the proposed controller is stable.

D. THE ROBUSTNESS PROOF

In terms of practicable application, the disturbances of the system include the sample errors of analog-digital converting, the noises, and the parameter variations that could affect the sliding surface, \(s\). Consequently, (31) is rewritten:

\[
\frac{ds}{dt} = F + QV_{\text{out}} + H
\]  

(35)

where \(H\) is the disturbance term. Thus, (28) is rewritten as:

\[
\frac{dW}{dt} = -s(H - K_c \text{sat}(s))
\]  

(36)

The \(dW/dt\) is undoubtedly negative. If the positive control gains satisfy the conditions, named \(K_c > |H|\). Hence, the ISMC emphasizes strong robustness.

The proposed control method block diagram is illustrated in Fig. 7. Consequently, the proposed converter’s output voltage is driven to the referenced level, and the instantaneous errors of the reference and the output voltages of the proposed converter are employed as the input of the ISMC. Moreover, the discrete-time nature of the simulation and implementation on a FPGA chip resulted in finite amplitude and “zigzag” motion of the frequency due to the imperfection in the sign function implementation [24]. This effect, named chattering, maximizes the output voltage ripple. To remove the chattering effect, the saturation function is used and makes the ISMC suitable for controlling the converter’s output voltage with minimum chattering and steady-state error.

IV. EXPERIMENTAL RESULTS

A. SOFT SWITCHING EXPERIMENTAL RESULTS

To prove the proposed converter proficiency, a prototype has been implemented. Also, to find the exact design specifications, Table 3 is presented. According to Table 3, the converter’s input voltage is 30V, and its output voltage is designed 500V. The switching frequency is 100 kHz, and the output power is 250W. The proposed converter’s practical prototype photo and the FPGA board of the controller are
The semiconductor elements’ practical waveforms on full-load are shown in Fig. 9. As maintained by this figure, the soft-switching conditions are verified for all semiconductors. It is observed by Fig. 9(a) that the main switch $S_m$ is turned on and off under ZVS condition. In addition, the maximum voltage of the $S_m$ is curbed to less than 150V. In addition to that, the conduction losses could be downgraded. Besides, Fig. 9(b) shows the ZCS condition on the auxiliary switch for turn on and off instance due to the slow increase and decrease of its current. According to the Fig. 9(b), the drain-source capacitor of the auxiliary switch resonates with the $L_a$ inductor resulting a ringing on the voltage of the auxiliary switch at the turn off instance. As illustrated in Figs. 9(c) and (d), the soft-switching operation is obtained for $D_1$ and $D_2$ diodes. The $D_1$ diode is turned on and turned off under ZVS and ZCS conditions, due to the gradually decrease of voltage and current respectively. Also, the $D_2$ diode is turned on under ZCS and turned off under ZVS conditions. Moreover, the waveforms of the $D_o$, depicted in Fig. 9(e), illustrates the output diode turns on and off under ZCS condition. Also, there is a resonance on the output diode voltage at the turn off instance because of the parasitic capacitor of the output diode which resonates with the leakage inductance of the coupled inductors.

The measured efficiency of the proposed converter and its hard-switched counterpart is plotted in Fig. 10(a) under 100W loads to full-load. As a result, the full-load measured efficiency of the proposed converter is 96.32% which is higher than that of the hard-switched counterpart. In addition, the losses distribution of the proposed converter is illustrated in Fig. 10(b). In this figure, the semiconductor devices losses and the inductors losses are considered. According to this chart, the majority of losses are associated to power switches. Also, the conduction losses of the diodes significantly affect the converter’s efficiency. The total losses can be declined by choosing the MOSFETs with low $R_{DS(on)}$. Also, to improve the converter’s efficiency, more coppers are recommended.

**TABLE 3. Significant design specifications.**

| Symbol       | Component     | Specification |
|--------------|---------------|---------------|
| $V_{in}$     | input voltage | 30V           |
| $V_{out}$    | output voltage| 500V          |
| $P_{out}$    | output power  | 250W          |
| $f_{sw}$     | switching frequency | 100kHz        |
| $C_p$        | charge-pump capacitor | 100µF         |
| $C_z$        | clamp capacitor | 22µF          |
| $C_{out}$    | output capacitor | 47µF          |
| $S_m, S_o$   | switches      | IRFP4668pf    |
| $D_1, D_2, D_o$ | diodes         | MUR820        |
| $D_o$        | output diode  | MUR880        |

**B. PI AND ISMC PRACTICAL WAVEFORMS**

Both of the controllers are implemented on a SPARTAN-6 XC6SLX9 FPGA chip to compare the experimental results of the PI and ISMC. The implementation process is as follows, which is similar for both controllers. The presented
converter’s output voltage is conveyed to analog to digital converter (ADC) pins of the FPGA board; the design calculations of the controller are done, then a PWM signal at 100 kHz is directly generated to control the duty cycle of the power switches.

In order to make a good challenge for the proposed control method and adjust the output voltage of the proposed converter to the desired value (500V), the proposed converter’s output power is changed over time. The practical results of the output voltage and current over power variations are shown in Fig. 11. In this scenario, the output power of the proposed converter is changed from half-load to full-load at \( t = 0.26 \)s, and full-load declined to half load at \( t = 0.91 \)s (the timing range accords to \( t = 0.26 \)s and \( t = 0.91 \)s are assumed from the beginning of these waveforms in Fig. 11(a) and (b)). The experimental results of the output voltage and current of the proposed converter by using the conventional PI and the proposed controllers are presented in Fig. 11(a) and (b), respectively. As can be simply found from Fig. 11(a), the output voltage response sustains a constant value. The earliest transient of the CH2 at \( t = 0.26 \)s illustrates the output voltage undershoot, which its amplitude is approximately 50V, and the next transient at \( t = 0.91 \)s shows the output voltage overshoot which is also about 50V. The settling time of the output voltage by the PI controller shows the controller’s response time is about 50ms for both of the power alterations. Additionally, in Fig. 11 (b), the experimental results of the proposed controller are shown. The earliest transient of CH2 at \( t = 0.23 \)s and the next one at \( t = 0.91 \)s match the output voltage undershoot and overshoot respectively, which are approximately 20V, and about 13ms settling time shown for both of the power alterations of 50% to 100% and vice versa. Also, the steady-state error which is shown in Fig. 11(a), is eliminated by the ISMC controller. As a conclude, the output current alteration in Fig. 11(b) shows the faster response time of the proposed controller compared with the PI controller, which is shown in Fig. 11(a).

C. PRACTICAL RESULT OF THE CONDUCTED EMI

For measuring the conducted EMI, a setup consisting of a CISPR22 LISN, and a GWINSTEK GSP-830 spectrum analyzer is used. The proposed converter’s EMI at full-load and the hard-switching counterpart’s EMI is measured. The conditions and the components of both converters are the same. Also, the LISN is positioned between the power supply.
with 30V, and the input of the converter and the spectrum analyzer is located on RS [17]. The major contribution of common-mode noise to differential-mode noise is achieved on peak detect mode. Figure 12 illustrates the total conducted EMI of the hard-switched counterpart and the proposed converter. Under CISPR 22 standard, the frequency range of the conducted EMI is bounded from 150 kHz to 30MHz by the horizontal axis [10], [11]. The vertical axis shows the electromagnetic interference value which is limited between 20dBµV and 100dBµV. Figure 12(a) illustrates the EMI of the hard-switched counterpart with 80dBµV and the Fig. 12(b) shows the EMI of the proposed converter. It is understood by Fig. 12 that the proposed converter’s EMI peak is approximately 8dBµV less than the hard-switching counterpart.

V. CONCLUSION

In the presented paper, a high step-up PWM non-isolated DC-DC converter with soft switching operations is proposed. The converter’s diodes and MOSFETs are operated under soft switching conditions, which improve the reverse recovery problem, the efficiency, and the conducted EMI of the proposed converter. The main switch operates under ZVS condition. Thus, the capacitive turn-on losses is ignored. Moreover, a control method based on ISMC is presented, which regulates the converter’s output voltage during the load variations. The presented theoretical analysis is confirmed through experimental tests under full-load for soft switching conditions and under half-load and full-load for the controller strategy. The experimental results show the soft-switching conditions for all the semiconductors, and the proposed controller has about 37ms faster transient response and approximately 30V less over/undershoot peak compared to the conventional PI controller. Furthermore, based on the EMI experimental results, the proposed converter has 8dBµV less EMI than the hard-switched counterpart in peak detect mode. In addition, compared to the hard-switched counterpart, the measured efficiency of the proposed converter is improved by 6.31%.

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