Enabling The Feed-Forward Design Model in OpenCL Using Pipes

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ABSTRACT
Over the past few years, there has been an increased interest in using FPGAs alongside CPUs and GPUs in high-performance computing systems and data centers. This trend has led to a push toward the use of high-level programming models and libraries, such as OpenCL, both to lower the barriers to the adoption of FPGAs by programmers unfamiliar with hardware description languages (HDLs), and to allow to seamlessly deploy a single code on different devices. Today, both Intel and Xilinx (now part of AMD) offer toolchains to compile OpenCL code onto FPGA. However, using OpenCL on FPGAs is complicated by performance portability issues, since different devices have fundamental differences in architecture and nature of hardware parallelism they offer. Hence, platform-specific optimizations are crucial to achieving good performance across devices.

In this paper, we propose using the feed-forward design model based on pipes in order to improve the performance of OpenCL codes running on FPGA. We show the code transformations required to apply this method to existing OpenCL kernels, and we discuss the restrictions to its applicability. Using popular benchmark suites and microbenchmarks, we show that the feed-forward design model can result in higher utilization of the global memory bandwidth available and increased instruction concurrency, thus improving the overall throughput of the OpenCL implementations at a modest resource utilization cost. Further concurrency can be achieved by using multiple producers and multiple consumers.

KEYWORDS
OpenCL, FPGA, high-level synthesis, compiler techniques, pipes, performance optimization

1 INTRODUCTION
Over the past several years, there has been an increasing trend toward using heterogeneous hardware in single machines and large-scale computing clusters. This trend has been driven by demands for high performance and energy efficiency. Initially, heterogeneity has mostly involved the use of GPUs and Intel many-core processors alongside multi-core CPUs [6]. More recently, due to their compute capabilities and energy efficiency, the trend has evolved to include Field Programmable Gate Arrays (FPGAs) [18] in high-performance computing clusters and data centers. Today, Microsoft Azure and Amazon Web Services include FPGA devices in their compute instances [3][1].

Hardware heterogeneity involves significant programmability challenges. Without a unified programming interface, not only are users required to become familiar with multiple programming frameworks, but they also need to understand how to optimize their code to various hardware architectures. To address this challenge, the Khronos group has introduced a unified programming standard called OpenCL, which is intended for accelerated programming across different architectures [4]. This programming model initially targeted CPUs and GPUs. At the same time, programming FPGAs using low-level hardware description languages (HDLs) has traditionally been considered a specialized skill. To facilitate the adoption of FPGAs, vendors have spent substantial resources on the design and the development of OpenCL-to-FPGA toolchains, including runtime libraries and compilers allowing the deployment of OpenCL code on FPGA. Intel and Xilinx, two major FPGA vendors, are now providing their own OpenCL-to-FPGA development toolchain and runtime system [5][10].

Although OpenCL increases portability and productivity, there is often a significant performance gap between an OpenCL and a hand-optimized HDL version of the same application [14]. Bridging this performance gap while limiting the development effort requires exploring existing OpenCL-to-FPGA optimizations and designing new ones. Several papers have aimed to improve the efficiency of existing OpenCL code (often tailored to GPUs) on FPGA through platform-agnostic and specific compiler optimizations and scheduling techniques [15][11][9][20].

Performance portability is one of the major issues when using OpenCL-to-FPGAs SDKs, especially for applications originally encoded for a different device (e.g., a GPU). It has been shown that OpenCL code tailored to one platform often performs poorly on a different platform [21]. The origin of the performance portability issues between GPUs and FPGAs lies in the different architectural characteristics of these two platforms. Specifically, there are three fundamental factors that affect the performance portability between GPUs and FPGAs. First, the form of parallelism that these devices offer. FPGAs leverage deep pipelines to exploit parallelism across OpenCL work-items, while GPUs rely on concurrent, SIMD execution of threads (or work-items). Second, the off-chip memory bandwidth of current FPGA boards is much lower than that offered by high-end GPUs, which results in inefficient memory operations and lower overall application performance. Third, while GPUs provide relatively efficient support for synchronization primitives like
In this work, we explore and evaluate the use of the feed-forward design model to improve the performance of OpenCL code on FPGA. The proposed model splits each kernel into two kernels - a memory kernel and a compute kernel - connected through pipes. At a high level, the model aims to increase the memory bandwidth utilization, reduce the memory units’ congestion, and maximize the instructions concurrency within the application. We show that the feed-forward design model allows the offline compiler to generate designs with more efficient memory units and increased instruction parallelism, leading to better performance with a low resource utilization overhead. A simplified version of this scheme has been explored in [22] on simple micro-kernels, in most cases leading to performance degradation over the original single work-item version of the code. In this work we show that, when generalized and applied to more complex and less regular kernels, this technique can achieve up to a 65× speedup over the single work-item version of the code, and an average 20× speedup across a set of diverse applications from popular benchmark suites [8][7].

Our exploration is structured as follows. First, based on recommendations from Intel’s OpenCL-to-FPGA documentation [2], we convert SIMD-friendly code into serial code (i.e., a single work-item kernel). Second, using the the feed-forward design model, we split each kernel into two kernels (memory and compute kernels), thus separating global memory reads from the rest of the instructions inside the kernel. In order to minimize the data communication latency, we connect these two kernels through pipes. Lastly, we explore increasing the concurrency by having multiple versions of the feed-forward design model, and in this work we show that, when generalized and applied to more complex and less regular kernels, this technique can achieve up to a 65× speedup over the single work-item version of the code, and an average 20× speedup across a set of diverse applications from popular benchmark suites [8][7].

In summary, this work makes the following contributions:

- Showing how the feed-forward programming model can improve performance of OpenCL codes on FPGA by addressing one fundamental performance bottleneck for single work-item kernels, namely, memory bandwidth utilization;
- Proposing a systematic method to use the feed-forward design model in OpenCL kernels;
- Identifying limitations of the explored design model;
- Exploring optimizations enabled by the feed-forward design model.

The rest of the paper is organized as follows. In Section 2, we provide background information on OpenCL for FPGA. In Section 3, we discuss the feed-forward design model, we show how it can be applied to existing OpenCL code, and we discuss its applicability and limitations. In Section 4, we present an experimental evaluation covering micro-benchmarks and applications from popular, open-source benchmark suites [8][7]. In Section 5, we discuss prior work in this area. In Section 6 we conclude our discussion.
2.2 OpenCL Memory Model

In order to better understand how different compiler or scheduling techniques and optimization can improve the performance of an OpenCL kernel on FPGAs, it is crucial to have a comprehensive knowledge of the OpenCL memory model and how they map on the system. The Memory model that defines the hierarchy of memory sections used by OpenCL applications consists of five sections. Figure 1 shows the hierarchy between these five sections. First is the host machine’s global memory, which is directly accessible by the host processor and is used to store the data that will further be transferred to or read from the device(s). The second one is the device’s global memory. This region is accessible to both the host processor and all the work-groups and work-items of the kernel and coordinates the data transfer between host and device memory. The third region is the constant global memory which is the section of the system memory that the host code carries read and write access to it, while the kernels only have read access. The device’s global and constant memories are usually memory chips connected to the FPGA device. However, in some cases it might also include distributed memories within FPGA fabric [21] [5]. The last two regions are high-throughput and low-latency memory regions known as local and private memory regions. The former region is shared and accessible among work-items inside a single work-group. The latter region is only visible to each work-item executing within an OpenCL processing element. These two memory regions are often implemented using BlockRAMs or registers in the FPGA fabric.

Many of the previous works, such as [16][23], aimed to reduce the performance limitations resulting from the external memory bandwidth of FPGA boards. In order to better understand the effect of compiler optimizations and scheduling techniques on memory operations, it is essential to know how OpenCL-to-FPGA compilers implement memory operations using load/store units (LSU). For the rest of the paper, we refer to Intel’s OpenCL-to-FPGA SDK as the offline compiler. The offline compiler can instantiate one of several types of LSUs depending on the inferred memory access pattern of the memory operations. Whether the accesses are to/from global or local memory, and which types of LSUs are available on the target FPGA platform are the parts of the information that the offline compiler uses to choose the most efficient available LSU type. For non-atomic memory operations on the global memory region, the offline compiler often instantiates from one of the multiple LSU types.

First LSU type used by the offline compiler is the burst coalesced LSU. The offline compiler often uses burst coalesced LSU as the default type. This type of LSU is the most resource-hungry memory module, designed to buffer memory requests until the largest possible burst of data read/write request can be sent to the global memory. Second, known as prefetching LSU, leverages a FIFO to read large blocks of data from global memory and tries to keep the buffer full of valid data. This type best fits the memory operations with a sequential memory access pattern. Further, for the memory operations on the local region, the offline compiler instantiates a pipelined LSU, which submits memory accesses in a pipeline manner as soon as they are received. The offline compiler can also use pipelined LSU as an alternative for global memory accesses, resulting in slower but more resource-efficient memory units.

3 IMPLEMENTING THE FEED-FORWARD DESIGN MODEL

As we mentioned in the background section, different LSU modules can result in a different hardware implementation with different resource utilization and throughput. Moreover, memory operations on global memory are known to be one of the main throughput bottlenecks for kernels implemented on FPGAs. While sometimes the offline compiler allows the programmer to control the type of the LSU, there is a lack of underlying hardware and implementation knowledge from programmers to leverage these customizations. Moreover, the offline compiler takes a relatively conservative approach regarding loop carried dependencies for global memory operations, resulting in a sub-optimal global memory bandwidth utilization. Programmers can verify this by checking the early stage analysis report file generated by the offline compiler.

Hence, there are two primary outcomes of the offline compiler memory analysis that significantly affect the kernel’s final performance. The first one is the type and setting of each LSU assigned to one or multiple global memory instruction(s). Moreover, the second is the presence of loop carried dependencies through global memory. In their presence, the offline compiler serializes the execution of loops with loop carried dependencies, resulting in a high initial interval (II) and low throughput for that specific loop. Initial interval is the number of clock cycles between the launch of successive loop iterations calculated for each loop in the design. This infers that the better the offline compiler understands the memory access patterns and behavior of global memory instructions inside the kernel, the more optimized the offline compiler will generate the final implementation.

Wang et al. [17] measured the memory bandwidth for sequential and random memory accesses for different variable types and concluded that kernels containing random memory accesses will suffer from low memory bandwidth drastically. Also, many OpenCL for FPGA baseline designs they used in their work had sub-optimal throughput due to severe lock overhead or memory bandwidth overhead. Through this work, we realized that programmers could help the offline compiler better understand the different characteristics of memory operations and dependencies by isolating the memory operations. For instance, using the feed-forward design model indicates that there is no loop carried dependencies between load and store instructions from/to global memory pointers. Providing this information to the offline compiler can significantly improve the performance in different applications. After converting the ported design to FPGA from the NDRange programming model to a single work-item programming model, using this technique can result in synchronization-free kernels with high memory bandwidth utilization.

In this design model, the resulting kernel responsible for loading values from global memory (memory kernel) should connect to the second kernel (compute kernel) through a hardware mechanism that does not involve using global memory. This restriction results in a second kernel that is free of global memory load instructions.
Therefore, in this design, it is not possible to use the local memory objects for this data sharing abstract because they are separate kernels. However, the OpenCL standard provides a concept of a memory object that is an ordered sequence of data items called pipes. Pipes are the primary mechanism for passing data between kernels, enabling concurrent execution of multiple kernels using pipeline parallelism across multiple kernels.

Each pipe has a write and read endpoint, which allows a single OpenCL kernel to write to one endpoint of the pipe and another kernel to read from the read endpoint of the pipe. It is worth mentioning that, in an OpenCL programming model host and device(s) can also have dynamic communication through pipes which is not the focus of this paper. Following the OpenCL specifications, Intel provides an OpenCL extension called channels and introduces it as a mechanism for data communication between kernels which can also help kernels synchronize efficiently [2]. This extension will allow concurrently running kernels to communicate without getting the host processor or device’s global memory involved.

Programmers can define the depth of the channels as an input attribute. At the same time, the offline compiler considers this input to be the minimum depth of that specific channel. The offline compiler may increase the depth if there is a need to balance the reconverging paths through multiple kernels or to achieve a lower initial interval for the loops inside the kernel [2]. In an OpenCL kernel written for Intel FPGAs, channels can be used in two formats: blocking and non-blocking. The blocking channel operations (read/write) will stall the kernel until the operation returns successfully. In contrast, non-blocking channel operations return the results of the operation as successful or failed through an additional flag immediately.

Intel recommends FPGA programmers use the single work-item programming model to design their OpenCL kernel. This programming model can maximize the throughput in applications that require fine-grained data sharing among parallel work-items. Moreover, Intel suggests using single work-item kernels over NDRange kernels when designing an application using channels/pipes while creating the feed-forward data path between the two kernels connected using pipes.

Using channels for concurrent kernel execution can improve the efficiency of the design. In this case, the host code launches the kernels concurrently, and kernels communicate through channels where applicable. Programmers can exploit this improved efficiency using the feed-forward design model with a producer-consumer approach in which one or multiple producer kernels send the data to one or multiple consumer kernels. In the feed-forward design model, a manager module and synchronization mechanism are required to ensure the design’s functionality is maintained while chasing performance improvement. In cases where synchronization is needed, programmers can use blocking channels to implement a synchronization mechanism among producer, consumer, and manager kernels. Our approach in this work follows the same feed-forward design. We use the host code and hard-coded sections in the producer and consumer kernel to address the need for a manager kernel between the producer and consumer kernel. This approach simplifies the design and reduces the number of busy waits between kernels. For the rest of the paper, we call the producer memory kernel and the consumer compute kernel.

```
1. for (int tid = 0; tid < num_nodes; tid++)
2. if(c_array[tid] == -1) {
3.   *stop = 1;
4.   int start = row[tid];
5.   int end;
6.   if ((tid + 1 < num_nodes)
7.     end = row[tid + 1];
8.   else
9.     end = num_edges;
10.  float min = BISNUM;
11.  for(int edge = start; edge < end; edge++) {
12.    if (c_array[col[edge]] == -1) {
13.      if (node_value[col[edge]] < min)
14.       min = node_value[col[edge]];
15.     }
16.   }
17.  min_array[tid] = min;
18. }
19. }
```

(a) The feed-forward design model example baseline

```
1. for (int tid = 0; tid < num_nodes; tid++)
2. if(c_array[tid])
3.   write_channel_intel(c0, c_array);
4. if(c_array == -1) {
5.   int start = row[tid];
6.   write_channel_intel(c1, start);
7.   int end;
8.   if ((tid + 1 < num_nodes)
9.     end = row[tid + 1];
10.  else
11.   end = num_edges;
12.  write_channel_intel(c2, end);
13.  for(int edge = start; edge < end; edge++) {
14.    int c_arr1 = c_array[col[edge]];
15.    write_channel_intel(c3, c_arr1);
16.    if (c_arr1 == -1) {
17.      write_channel_intel(c4, node_value[col[edge]]);
18.    }
19. } }
20. }
```

(b) The feed-forward design model resulted memory kernel

```
1. for (int tid = 0; tid < num_nodes; tid++)
2. int c_arr = read_channel_intel(c0);
3. if(c_arr == -1) {
4.   *stop = 1;
5.   int start = read_channel_intel(c1);
6.   int end = read_channel_intel(c2);
7.   float min = BISNUM;
8.   for(int edge = start; edge < end; edge++) {
9.     int c_arr1 = read_channel_intel(c3);
10.    if (c_arr1 == -1) {
11.       float node_val = read_channel_intel(c4);
12.      if(node_val < min)
13.       min = node_val;
14.    }
15. }
16.  min_array[tid] = min;
17. }
18. }
```

(c) The feed-forward design model resulted compute kernel

Figure 2: The feed-forward design model example
Channels have been used in the past mostly to connect kernels in order to explore intra-kernel optimization space [12] or to explore data partitioning and memory bandwidth limitation on simple hand-written kernels [22][17]. However, the performance advantage is usually limited in these kernels due to global memory bandwidth limitations. This work focuses on transforming kernels from various programming model domains with or without control-flow divergence to a producer/consumer base implementation using channels. This transformation involves managing global read instructions in a separate kernel and reducing the unnecessary control-flow divergence due to the kernel’s behavior.

While focusing on this design model, it is crucial to understand the limitations of our suggested design. To have an easier understanding of these limitations, we use the single work-item version of kernels as the baseline to check whether this approach is feasible to be implemented or not. Assuming the kernel is in NDRange form like the baseline implementation of the benchmarks in [7] and [8], programmers can construct the single work-item version by embedding the body of the NDRange baseline kernel within a nested loop. The outer and inner loops must have the work-group and work-item sizes as the loop iteration count, respectively. Analyzing the single work-item kernel, if the programmers identify true loop carried dependencies that involve global memory operations inside the kernel, a simple feed-forward design model cannot be applied. This shortcoming is due to the lack of a well-defined technique to introduce global intra-kernel synchronizations between concurrent kernels in OpenCL to FPGA toolchains. We will elaborate on loop carried dependencies later in this section.

While having this information regarding efficient OpenCL kernel design, Figure 2 shows an example of how programmers can leverage the Channels extension (OpenCL pipes) to convert a complex single work-item baseline kernel into the feed-forward design model implementation. In what follows we explain this process step-by-step and match each step with the provided example in Figure 2 (in the example in Figure 2 we used notations from Intel OpenCL to FPGA SDK).

(1) Remodeling the kernel to a single work-item programming model if the baseline is in NDRange format.

(2) Identifying instructions that read from a global memory pointer (lines 2, 7, 12, and 13 from the baseline in 2a).

(3) Check the kernel to make sure no MLCDs are presented in the kernel.

(4) If there are no kernel inside the application that include MLCD(s), move to the next step. Otherwise, this form of feed-forward design model is not feasible for those specific kernel(s), but programmers can still apply it to the rest of the kernels inside the application.

(5) Allocating a local variable for load instructions inside a conditional or loop statement to increase the clarity of data transfers (lines 2 and 14 on the Figure 2b).

(6) Copying the baseline kernel (Figure 2a) into two different kernels, namely memory kernel (Figure 2b) and compute kernel (Figure 2c).

(7) Defining a pipe for each load instruction using the proper data type.

(8) Adding a write to pipe instruction for each read from global memory pointers in the memory kernel (lines 3, 6, 12, 15, 17 on Figure 2b).

(9) Replacing instances of reading from a global memory pointer with a read from the assigned pipe inside the compute kernel (lines 2, 5, 6, 9, 11 from the Figure 2c).

(10) Removing any arithmetic computation, store to global memory pointers, or local memory object from the memory kernel which will not affect the control flow paths containing a load instruction or their indices.

(11) Cleaning both kernels from empty control flow paths and values not further used (i.e., applying dead code elimination pass (DCE)).

(12) Instantiating memory kernel and compute kernel multiple times to have a multiple producers/consumers implementation and adjust the main loop trip counts accordingly. In the case of multiple kernels, due to the resource utilization overhead, we only instantiate multiple versions of producer and consumer only for the kernel(s) which dominate the application's execution time.

(13) Checking the control flow statements conditions inside each kernel again and simplifying them if possible (i.e., running the second DCE pass)

(14) Replacing the baseline kernel Enqueue inside the host code with the Enqueue of all memory and compute kernels on separate queues.

Limitations - Recall that as we mentioned earlier, while converting the NDRange kernel into a single work-item programming model in case the conversion results in loops with true loop carried dependencies through global memory, the kernel is not suitable for this design model. Using this design model for kernels with this characteristic will result in inaccurate outputs generated by the application due to the concurrency of dependent load and store instructions.

Our proposed technique can improve the kernels’ performance due to optimizing the following characteristics of the kernel.

loop carried dependencies - In order to better understand the impact of the loop carried dependencies (LCD) on the performance of different kernels, it is crucial to understand different types of LCD and how the offline compiler deals with them. Typically LCD can be in the form of memory loop carried dependency (MLCD) or data loop carried dependency (DLC).

MLCD applies when a single value or vector data stored in the global memory in one iteration of a for loop inside the kernel is further requested by a later iteration of the same loop. This data dependency implies that the device needs to schedule the read and write operations serially to ensure the correctness of the results generated from the kernel. Figure 3(a) shows an example of MLCD in which the operation in line 4 has a global memory loop carried dependency to the operation in line 2. The offline compiler will serialize such a loop to ensure that the correctness is guaranteed. While converting NDRange kernels to single work-item kernels, the results from the offline compiler report files indicate that the offline compiler takes a more conservative approach and considers MLCD where it cannot determine whether there is one or not. We realized that this would result in a significantly higher execution time for different benchmarks throughout our experiments. For
each MLCD that the offline compiler implies, it will serialize the whole loop to ensure the correctness of the kernel results, which drastically increases the initial interval (II) of the loop and results in the performance degradation, as mentioned earlier.

```
1. for (int tid = 1; tid<num_nodes; tid++) {
2.   a = output[tid-1];
3.   b = input[tid];
4.   output[tid] = a * b;
5. }
```

(a) Memory loop carried dependency

```
1. for (int tid = 5; tid<num_nodes; tid++) {
2.   r = 0;
3.   for (int iter=0; iter<num_nodes; iter++) {
4.     a = input[tid-iter];
5.     r += a;
6.   }
7.   output[tid] = r;
8. }
```

(b) Data loop carried dependency baseline

```
1. for (int tid = 5; tid<num_nodes; tid++) {
2.   r = 0;
3.   for (int iter=0; iter<num_nodes; iter++) {
4.     a = input[tid-iter];
5.     r += a;
6.   }
7.   write_channel_intel(c8, a);
8. }
```

(c) Data loop carried dependency Memory kernel

```
1. for (int tid = 5; tid<num_nodes; tid++) {
2.   r = 0;
3.   for (int iter=0; iter<num_nodes; iter++) {
4.     a = read_channel_intel(c8);
5.     r += a;
6.   }
7.   output[tid] = r;
8. }
```

(c) Data loop carried dependency Compute kernel

Figure 3: Loop carried dependencies

While we propose this technique to help programmers write more efficient and optimized codes for FPGAs, we believe that programmers should have such knowledge regarding cases of MLCD inside their application. Programmers must only use this design model when they can guarantee that there is no true MLCD involved in the algorithm or application they are implementing. This design model ensures the offline compiler that there is no true MLCD in the application. The offline compiler can generate an implementation with substantial performance benefits compared to the baseline code. For instance, while applying the feed-forward design model on Maximal Independent Set (MIS) application from Pannotia, removing the false MLCDs results in improving the maximum global memory bandwidth utilization from 208 MB/s to 2116 MB/s and results in 6.35x speedup over the single work-item baseline.

DLCD is another form loop carried dependencies which results in the serialization of the loops by the offline compiler. Figure 3(b) shows an example of DLCD in which the operation on line 5 implies a loop carried dependency for the loop on line 3, and the offline compiler will serialize the load and arithmetic instruction in this example. This serialization will result in an initial interval higher than one for the loop, which has a significant negative effect on the performance of the kernel. This serialization will also result in a lower memory bandwidth utilization for load instruction in the loop, especially load instructions with regular memory access patterns. However, after applying our technique to the baseline kernel, this DLCD is moved to the compute kernel which is free of memory operations. This will allow the offline compiler to schedule load instructions in the Memory kernel earlier since now these instructions are in a loop with no DLCD. Figure 3(c) and 3(d) show how the DLCD in the loop in Figure 3(b) is moved only to the compute kernel and the offline compiler can schedule the memory instructions in memory kernel in a pipeline manner.

Simplified control flow for load instructions - While applying this technique, the memory kernel can have a more simplified control flow graph (CFG) compared to the original baseline. A less complex CFG for the kernel with memory operations can result in less stall for read instruction on global memory, hence higher memory bandwidth utilization. Consequently, improved global memory bandwidth utilization can improve the overall performance of the implementation as respectively.

Enabling feed-forward design model with multiple producers and consumers - The most significant advantage of our proposed technique is enabling using the feed-forward design model to increase the memory bandwidth utilization for load instruction by increasing concurrency among memory operations. In the feed-forward design model, data traverses from the producer to the consumer in one or multiple words. For each word written on a channel by the producer kernel, the consumer will process the data and free up the memory space assigned to the channel. The producer kernel can reuse this memory region further to transfer the following word(s) of data to the producer kernel. Having multiple producers and consumers in the design could potentially increase the maximum global memory bandwidth achieved by design.

Having multiple producers and consumer kernels require the programmer to make various decisions regarding their number, the load balancing mechanism, and buffer management. Having more replications adds concurrency while increasing the complexity of the design and the use of channels to implement data transfers between producers and consumers. Intel recommends limiting the number of channels used in the design, as they can add complexity and limit overall performance. Also, having a large number of kernels to read data from global memory concurrently can increase global memory congestion and result in poor global memory bandwidth utilization. In our experiments across benchmarks, we did not find significant performance improvements beyond two producers and two consumers. By limiting the use of channels and the global memory contention, this setting allows for increasing the performance of the design at a limited resource utilization overhead. Moreover, we explored using a single producer and multiple consumers during our experiments on a limited number of benchmarks. However, results indicated that having separate producer kernels will result in higher concurrency compared to the case with one producer and multiple consumer kernels.

Programmers can use different load balancing mechanisms to implement their programs using one or multiple producer/consumer
### Table 1: Base Characteristics of Rodinia and Pannotia benchmarks used in this work and used datasets

| Suite | Benchmark                      | Dwarves                  | Memory Access Pattern | Dataset Description |
|-------|--------------------------------|---------------------------|-----------------------|---------------------|
| Rodinia | Breadth-First Search (BFS) | Graph Traversal | Irregular             | #nodes=2M           |
|        | Hotspot                        | Structured Grid          | Regular               | Size=8192           |
|        | k-Nearest Neighbors            | Dense Linear Algebra     | Regular               | Size=8.3M           |
|        | Hotspot 3D                     | Structured Grid          | Regular               | Size=8192           |
|        | Needleman-Wunsch               | Dynamic Programming      | Regular               | Size=8192           |
|        | Back Propogation               | Unstructured Grid        | Regular               | Size=12.8M          |
| Pannotia | Floyd-Warshall (FW)           | Graph Traversal          | Irregular             | Size=512            |
|        | Maximal independent set (MIS) | Graph Traversal          | Irregular             | G3_circuit          |
|        | Graph Coloring (CLR)           | Graph Traversal          | Irregular             | G3_circuit          |

kernels. These mechanisms can be classified as either static or dynamic. Unlike dynamic algorithms, a static load balancing algorithm does not take into account the state of the system to make decisions regarding the distribution of tasks. Many of the dynamic load balancing algorithms require busy-wait or feedback mechanism implementations involving more than two kernels by polling on non-blocking channels. This form of busy wait can result in sub-optimal performance for the designs on FPGA. We use static load balancing to connect producer and consumer kernels in this work. However, static load balancing will simplify the design and avoid using busy waits or non-blocking channels, which also increases the resource utilization of the design. By following this method, programmers can further improve the execution time of the feed-forward design model up to 93% by improving the global memory bandwidth utilization and concurrency among instructions/increased performance number for Hotspot application from Rodinia by increasing the global memory bandwidth utilization from 7340 MB/s to 13660 MB/s.

Moreover, programmers can use a single memory location or a FIFO buffer to manage data transfer between kernels. From our experiments with the feed-forward design model, we concluded that the channel’s depth does not significantly affect the performance improvement or degradation. Hence, we use a single memory location for data transfer between each producer and consumer kernel. Moreover, we designed a set of automatically generated microbenchmarks to explore the baseline kernel features that would impact the design speedup by using the feed-forward design model. We will discuss the characteristics of these microbenchmarks in the Section 4.

### 4 EXPERIMENTAL EVALUATION

#### 4.1 Experimental Setup

**Hardware** - We ran our experiments on an Intel programmable acceleration card (PAC) with an Arria® GX FPGA. The PAC board contains two 4 GB DDR-4 SDRAMs memory banks with a maximum bandwidth of 34.1 GB/s and 128 MB of flash memory. This FPGA includes 65.7 Mb of on-chip memory, 1150k logic elements (ALUTs), and 3036 digital signal processing (DSP) blocks. On the host side, the machine is equipped with an Intel Xeon® CPU model E5-1607 v4 with a maximum clock frequency of 3.1 GHz. Also, on the host machine, we used Intel FPGA SDK for OpenCL version 19.4 with Ubuntu 18.04.6 LTS.

**Performance Metrics** - For performance, we measure and report the speedup over the original single work-item version of each benchmark. For resource utilization comparison, we exhibit the increase in logic utilization and use of block RAMs (BRAMs) in the transformed version compared to the single work-item version. Logic utilization represents an estimation of how many half ALMs (adaptive logic modules) the compiler used to fit the design. The compiler presents this number as a percentage of total half ALMs on the FPGA board. ALMs are the basic building blocks in an FPGA. The simplified version of ALMs contain a lookup table (LUT) and an output register. The compiler can use ALMs to build different Boolean logic on the board.

**Benchmarks** - In this work, we first started by evaluating our design on widely used open-source benchmarks from Rodinia [8] and Pannotia [7] benchmark suites from different domains. We use table 1 to summarize the main characteristics of these applications in addition to resource utilization and execution time of the baseline codes.

#### 4.2 Experimental Result

In what follows, we will discuss the kernels’ main characteristics, which have gained the most speedup from our proposed technique, in two steps. First, we will discuss which benchmarks benefit from the transformation of the base kernel to the feed-forward design, and later we will discuss how these kernels can benefit from increased concurrency by having multiple producers and consumers.

**Feed-forward model comparison with the baseline** - Table 2 shows the speedup impact of transforming the single work-item baseline of each benchmark to the feed-forward design model. In all cases, we used the naive code without any optimizations in order to isolate the impact of this design model in the final results. Moreover, we obtained the best result from running the same experiments with channels having three different depths of one, 100, and 1000 in the design. We should recall that the offline compiler considers channel depth input as the minimum depth of that specific channel and may increase if there is a need to balance the reconverging paths through multiple kernels or achieve a lower initial interval for the loops inside the kernel. During our experiments, we realized that the depth of the channel does not significantly affect the speedup for the feed-forward design, and there is no
Table 2: Resource utilization and throughput comparison of the feed-forward design model with the baseline

| Benchmark | Baseline Execution Time (ms) | Feed-forward Design Speedup over Baseline | Baseline Logic Utilization (%) | Feed-forward Design Logic Utilization (%) | Baseline BRAM | Feed-forward Design BRAM |
|-----------|-----------------------------|------------------------------------------|-------------------------------|-------------------------------------------|---------------|--------------------------|
| BFS       | 6422                        | 13.84                                    | 18.62                         | 20.00                                     | 578           | 596                      |
| PageRank  | 8430                        | 0.96                                     | 20.43                         | 22.52                                     | 703           | 709                      |
| FW        | 41760                       | 64.95                                    | 16.21                         | 16.47                                     | 482           | 465                      |
| MIS       | 2166                        | 6.47                                     | 21.77                         | 24.44                                     | 803           | 807                      |
| Color     | 453                         | 1.02                                     | 17.78                         | 19.48                                     | 651           | 656                      |
| Hotspot   | 22553                       | 0.85                                     | 16.14                         | 17.25                                     | 517           | 522                      |
| Hotspot3D | 31967                       | 0.88                                     | 16.45                         | 17.95                                     | 542           | 536                      |
| BackProp  | 140601                      | 44.54                                    | 24.67                         | 26.68                                     | 674           | 646                      |
| NW        | 26036                       | 50.95                                    | 16.10                         | 18.86                                     | 506           | 407                      |

Figure 4: M2C2 speedup and resource utilization overhead compared to the feed-forward design baseline

notable trend for increase/decrease in any specific metric using channels with higher or lower depth. As shown in table 2, among the benchmarks we explored, Breadth-First Search (BFS), Floyd-Warshall (FW), Back Propagation, Maximal independent set (MIS), and Needleman-Wunsch (NW) benefit drastically from converting the single work-item baseline to the feed-forward model. In all these benchmarks, the main driver for the speedup is removing false loop carried dependency between operations on the device’s global memory region.

For Floyd-Warshall (FW), the false LCDs detected by the offline compiler results in a large initial interval (II) of 285 for the main loop inside the kernel. In similar cases, the offline compiler often uses burst coalesced LSU type for memory operation involving global memory and results in low memory bandwidth for operations with regular memory access patterns. Using the feed-forward design model will result in resolving those dependencies while converting the same loop to a fully pipelined loop with an II of one. It will also enable the offline compiler to use a prefetching LSU for one of the three global load operations with a regular memory access pattern and increases the maximum global memory bandwidth of the kernel from 630 MB/s to 3130 MB/s. These changes will result in up to 65X speedup compared to the single work-item baseline.

Following the same trend, the Back Propogatation benchmark benefits from this design in the same way. The main loop that degrades the performance of the kernel in the single work-item version with II of 416 will transform to a pipelined loop with II of one. This decrease in the II will increase the maximum global memory bandwidth used by the kernel and result in a significant speedup of 44X over the single work-item baseline.

Other three benchmarks also benefit from this model in the same way. Here, we should notice that the baseline version of the Needle-Wunsch (NW) benchmark carries a true MLCD inside the main loop of the kernel. However, this LCD is for a read memory operation that in iteration K which is dependent on the write memory operation in the iteration K-1. In this case, this LCD can be resolved in the baseline kernel using a local variable in the private memory of the device. Storing the dependency value at the end of each iteration can remove the existed loop carried dependency with the global memory operations. Hence, the kernel can read the same value at the beginning of the next iteration (except the first iteration). Adding this private variable will result in a single work-item baseline kernel with no MLCD. Then we can apply the feed-forward design model to get up to 50X speedup by decreasing the II of the main loop and increasing the global memory bandwidth of the application.

While the feed-forward design model enables removing MLCDs and increasing the maximum global memory bandwidth of the kernel. It also enables using multiple producers/consumers to increase the concurrency among the instructions in the application. However, a resource utilization overhead is associated with this increase in concurrency. Hence, it is crucial to analyze the profiling data before increasing the number of producers and consumers.

In this work, we use the Intel OpenCL-to-FPGA profiler to analyze the throughput and execution time of each kernel. In order to avoid high resource utilization overhead, we only instantiate multiple versions of the producer and consumer kernels for the kernel with the dominant execution time in the application. This rules out kernels commonly used for initialization only once at the beginning of application execution. We also tried multiple values...
as the number of producers and consumers in multiple applications. Results from these experiments indicated that having more than two producers and two consumers per kernel in the design will result in high resource utilization overhead and either non-significant speedup or even throughput degradation due to memory congestion among concurrent memory instructions.

Figure 4 shows the speedup from having two memory and two compute kernels (M2C2) alongside resource utilization overhead. In this part, we only duplicate the memory and compute kernel for the kernels that dominate the execution time of the application in the feed-forward design model. We compare the speedup to the feed-forward design baseline, which indicates that the M2C2 version is much faster than the single work-item baseline model in most applications. Results show an average of 39% speedup over the feed-forward design model baseline with a 31% average increase in logic utilization and a 26% average increase in the number of BRAMs used by the implementation also compared to the feed-forward design baseline. In the case of Pagerank and Back propagation benchmarks, the profiling data from the feed-forward design baseline indicates highly optimized memory operations with high global memory bandwidth utilization. This characteristic of these applications hinders further performance improvement from using multiple memory and compute kernels.

Moreover, it is worth mentioning that analyzing the results from different sections of the experiments indicates no obvious increase/decrease trend for the maximum frequency of the final implementation for different versions of each application.

A case study with vector variable type - While using pipes to enable the feed-forward design model, we also tried to improve the memory bandwidth utilization by using vector type operations. Using vector-type operations can potentially decrease the number of memory read and write requests and data transfers. The speedup from using vector type variable is highly dependent on the memory access pattern of memory operations and the utilized memory bandwidth of the design. For instance, using vector type operations, we were able to improve the throughput of the FW benchmark by 3× while it degraded the performance of the MIS benchmark significantly. Unfortunately, we could not explore this optimization more on all of our experimental benchmarks due to an internal flaw in the Intel OpenCL-to-FPGA SDK. This flaw will result in an internal error while using the feed-forward design with pipe and vector type memory operations and data transfers. We informed Intel about this compiler flaw and received confirmation.

Microbenchmarks - In the last part of this work, we designed two sets of automatically generated microbenchmarks to explore the impact of two features in the baseline kernel on the performance of the feed-forward design model. The first one is the access pattern of the kernel’s load instructions, and the second one is the divergence among different iterations of the main loop in the single work-item kernel.

The first set of microbenchmarks is designed to target memory access patterns. We use two kernels with no divergence among main loop iterations, eight load instructions from global memory, and eighty arithmetic operations (i.e., arithmetic intensity of 10). These two kernels only differ in the behavior of their load instructions. The first benchmark in this set, called MAI10 R, has load instructions with regular memory access patterns, and the second one, called MAI10 IR, has load instructions with irregular memory access patterns.

The second set of microbenchmarks targets the divergence among different iterations of the main loop in a single work-item kernel. To this end, we designed two kernels with the same characteristics as the first set; however, we added a for loop with a different trip count for each iteration of the main loop alongside one if statement inside to add divergence to the first set of microbenchmarks. To further show the impact of the feed-forward design model on kernels with DLCD, we also added a reduction operation inside the inner loop to add data dependencies among different iterations of the inner loop. We also decreased the number of arithmetic operations inside the kernels to increase the divergence’s impact on the kernel’s total execution time. Like the first set of microbenchmarks, one microbenchmark, called MAI6 for-if R, has load instructions with regular, and another, called MAI6 for-if IR, with irregular memory access patterns.

Table 3 shows the impact of the feed-forward design model with two producers and two consumers on these sets of microbenchmarks. From the memory access pattern point of view, the results suggest that kernels containing load instructions with regular memory access patterns would often benefit more from the feed-forward design model than those containing irregular load instructions. This is due to a higher memory contention for concurrent irregular load instructions in the feed-forward design with multiple producers, which leads to a lower memory bandwidth utilization.

Moreover, the feed-forward design model benefits kernels with divergence and DLCD more than the first set of microbenchmarks. The baseline version of these microbenchmarks has a lower memory bandwidth utilization due to a more complex control flow graph and the presence of a DLCD compared to the first set of microbenchmarks. Using the feed-forward design model removes the DLCD from the producer kernel and increases the concurrency among memory instructions by having two producer and two consumer kernels. These changes will result in significantly higher memory bandwidth utilization and, hence, better execution time.
5 RELATED WORK
Zohouri et al. [21] and Nourian et al. [13] studied several optimization techniques on different applications from Rodinia benchmark and finite automata traversal respectively while focusing on performance evaluation and power consumption. Their analysis confirms the performance portability gap while porting a GPU-optimized OpenCL implementation to FPGA and indicates a critical need for FPGA-specific optimizations to reduce this gap. Kromydas et al. [11] performed a similar analysis on several OpenCL kernels investigating pipeline parallelism on single work-item kernels, manual and compiler vectorization, static coalescing, pipeline replication, and inter-kernel channels. Hassan et al. [9] explored FPGA specific optimizations in their work. Their benchmarks were chosen from irregular OpenCL applications suffering from unpredictable control flows, irregular memory accesses and work imbalance among work-items. In their work, they exploit parallelism at different levels, floating-point optimizations, and data movement overhead across the memory hierarchy.

Several previous works have tried to leverage channels to improve the performance of their implementations by increasing the concurrency among the instructions. Sanaullah et al. [15] proposed an empirically guided optimization framework for OpenCL to FPGA. They leveraged channels to convert a single kernel implementation to multiple kernels, each working as a separate processing element. In their work, they used channels for data communication among kernels. However, their analysis indicates that using channels in their implementation can result in lower performance, mainly due to the data dependency among kernels and the need for synchronizing data paths. Wang et al. [19] leveraged using task kernels and channels to design a multi-kernel approach to reduce the lock overhead. Mainly their work was focused on data partitioning workload. Yang et al. [17] used channels to implement a specific molecular dynamic application.

In a more recent work, Liu et al. [12] proposed a compiler scheme to optimize different types of multi-kernel workloads. They introduced a novel algorithm to find an efficient implementation for each kernel to balance the throughput of a multi-kernel design. Additionally, they explored bitstream splitting to separate multiple kernels into more than one bitstream to enable more optimizations for individual kernels.

6 CONCLUSION
In this work, we proposed guidelines for using a feed-forward design model based on pipes in order to improve the performance of OpenCL codes running on FPGA. We showed the code transformation steps to convert OpenCL kernels to a feed-forward design model and introduced the limitations of its applicability. By analyzing the results from our experiments, we realized that this design could improve the performance of the single work-item kernels potentially up to 86x if multiple producers and consumer kernels are instantiated.

To continue this work in future, we are planning to look into more automatically generated microbenchmarks to identify different baseline kernel features that affects the speedup of the feed-forward design model.

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