Area optimized design of tetrad flip-flop using new tetrad value logic gate's

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Abstract. Logic levels in digital systems are predefined voltage and current range and a defined difference in voltage and current value signify binary information's in digital systems. There are many logic families available to define binary data. In binary logic, there are two logic levels 1 and 0. This paper defines a new tetrad value logic (TVL) which can have four logic levels 0, 1, 2 and 3. This work presented novel designs of tetrad value logic NOT gate, AND gate and OR gate. With the help of these tetrad logic gates, a tetrad logic Flip-flop has been designed and tested on Tanner Electronic Design Automation (EDA) tool. The proposed tetrad flip-flop is a memory cell of tetrad Value Logic (TVL) which can store Logic 0, Logic 1, Logic 2, and Logic 3 when the input clock is off, and on the positive edge of the input clock, it can change the past stored logic with new input logic. This work discusses the possible application of tetrad logic. Simulation of tetrad logic gates and flip flop performed with help of tanner tool and verifies expected output correctly for all possible test cases. Parameters like Voltage levels, power consumption, noise margin, MOS count, propagation time, fan-out, noise margin, clock frequency, sink, source current, setup and hold time, are analyzed for proposed tetrad logic gates and flip flop. The S-edit 9.0 is used for the schematic design and T-spice 9.0 is used for parameter setting and design technology selection and W-edit 9.0 is used for simulation observation. The obtained results have been compared with other similar work and found better.

Keywords. Tetrad Value Logic (TVL), N value logic (NVL), Quad logic, Fan-out, Binary logic, MOSFET, Flip-flop, Noise margin.

1. Introduction

Natural signals are analog and require complex computation when they process in electronic systems. To simplify the computational complexity of analog signals, binary logic introduced. It uses only two logic state 0 and 1 which reduces the complexity of computations[1]. In binary logic one wire carries only two logic levels and when big data needs to communicate a collection of wires needed[1]. A binary flip flop can store only 0 or 1 logic. Quad or tetrad logic can reduce the numbers of wires to communicate information also tetrad logic can store four logic levels in one flip flop. The applications of tetrad value flip-flop are as below:

- To store any decimal value range between 0 to 255, 8 binary logic flip-flops will be required, however, the same number can be store by only four tetrad logic flip flop.
- In Simple UART Serial data transmission to transmit any decimal value stored in 8 binary bit register, 8 clock cycles will be required, however in case of tetrad logic the same decimal number can be store in four tetrad flip-flop only hence only four clock cycles will be required.
Figure 1(a) below shows the interfacing of 256x8 memory with binary logic requires 8-bit address bus and 8-bit data bus needed however with tetrad value same memory will required 4-bit address bus and 4-bit data bus needed.

![Diagram showing memory interfacing with binary and tetrad logic](image)

**Figure 1.** (a) 256-byte memory Interfacing with binary number system (b) 256 byte Memory interfacing with the Tetrad number system

Concept of a fuzzy flip flop was defined in 1989 [2]. Kaoru's [2] J-K flip-flop was capable of storing min and max logics and performing negation operation. Multivalue full functioning flip flop with 27 types of function transformation described in 1991 [3]. the weighted fuzzy flip-flop is constructed by weighted AND/OR elements in 1995 [4]. A new strategy for optimization of storage in flip flop using the same elements of the same array as for elements of different arrays describe in 1997 [5]. A concept of fuzzy logic-based J-K flip-flops and fuzzy complementation operations was presented in 1998 [6], their fuzzy Flip flop was based on bounded product and bounded sum. A resistive fault model for real defects describe in 2000 [7]. Amir's fuzzy logic techniques [7] was used for fault simulation. Fuzzy logic can be used for multi-value logic (MVL) which can have more logic between true and false as described in 2001 [8]. In binary logic more wires required so more connectors and more power but if multiple (i.e. N-logic) logic used every wire in N value logic (NVL) [9] can carry N logic levels hence the need of wires will directly reduce by (logN/log2) times so fewer connectors and less power. Ugur's Multiple valued static CMOS memory cell [9] design was developed in 2001 and they configure their flip flop for quad-level and perform simulation and validation. Later a new modified fuzzy memory cell and a new fuzzy logic AND logic and OR logic gate defined in 2007 [10], Ben's fuzzy cell [10] were capable to store any two values between zero to one. [11] presented an alternative logic level known as multi-level logic (MLL) in place of binary logic level in 2011. Quadruple valued logic (QVL) based flip-flop design presented in 2017[12] with quad states true, partially known, partially unknown, and false. [13] develops a nonvolatile flip-flop which was based on Spin Transfer Torque (STT) method and it offers normally-off and sudden-on computing features to minimize leakage.

Fuzzy logic represents logic levels between zero and one, but the issue is that fuzzy logic does not define fix range for mid logic level and its define boundaries sometimes overlap, hence to have significant noise margin is not possible in fuzzy logic based logic gates and so in fuzzy logic based flip flops [2-4,6-8]. N value logic (NVL) [9] can have N-2 fix numbers of logic levels between 0 and 1, but in NVL the reference voltage varies with N, hence NVL cannot be standardized. Ben's [10] Fuzzy memory cell was developed for quad logic in their work generalized inverter is used for complement quad logic, the generalized inverter requires 11 CMOS which enhances the area. Quadruple valued logic (QVL) [12] based flip-flop has a fan-out capacity of two only. Spin Transfer Torque (STT) based
four value flip-flops can be further optimized in terms of area and as the STT requires additional hardware.

This paper presents a tetrad value logic (TVL) flip-flop which can store four logic levels 0, 1, 2 and 3 with a better fan-out capacity of 10 also a better noise margin of 1 volt. The Tetrad inverter is designed with one CMOS only where the reference voltages vary. Apart from better fan-out and noise margin, the challenge is to design a tetrad logic flip-flop which is more area optimized as compare with two binary logic flip-flop and the maximum speed of tetrad logic flip flop must not be less than double of a maximum speed of binary logic flip-flop. Tetrad logic must be simple as binary logic and it must perform computations simply as binary logic. In binary logic noise margin is significant but to maintain a similar noise margin with tetrad logic in another challenge. This work design resolves the challenges above with the new design of Tetrad logic Gates.

2. Methodology

Tetrad-value input and output voltage and current levels shown in table 1, the total voltage range is 0 to 6 volt and the noise margin [14,18] between two levels is 1 volt. 1-volt noise margin is considered good when buses and connectors are of good quality. sink current [14,18]capacity is of 16mA and Fan-Out [14,18] is 10, so total ten another tetrad logic gates can be run from one tetrad logic gate. Binary logic can perform computation easily because it uses Boolean algebra and binary logic gates [14]. To make tetrad-value logic simple the Boolean equation of tetrad logic Gates are also defines.

| Table 1. Input and output voltage and current levels of Tetrad logic gates |
|-----------------------------|-----------------------------|
| **Input Voltage Levels**     | **Output Voltage Levels**    |
| Logic '3' 6v                 | 6v                          |
| Logic '3' 4.5v               | 5v                          |
| Logic '3' 40 μA              | 400 μA                      |
| Logic '3' 4.5-6 volt Logic 3 | 5-6 volt Logic 3            |
| Logic '2' 4.5v               | 4.5-5 v                     |
| Logic '2' 300 μA             | 3.5-4.5 volt Logic 2        |
| Logic '2' 3v                 | 3 mA                        |
| Logic '2' 3-4.5 volt Logic 2 | 3.5-4.5 volt Logic 2        |
| Logic '1' 3v                 | 2.5 - 3.5 v                 |
| Logic '1' 1.25 mA            | 1.5-2.5 volt Logic 1        |
| Logic '1' 1.5-3 volt Logic 1 | 1.5v                        |
| Logic '0' 1.5v               | 1.5v                        |
| Logic '0' 1.6 mA             | 16 mA                       |
| Logic '0' 0-1.5 volt Logic 0 | 0-1 volt Logic 0            |
| Logic '0' 0v                 | 0v                          |

Figure 2 below shows the tetrad logic Not Gate symbol and table 2 shown below is the truth table of proposed tetrad logic NOT gate. Designing of tetrad logic NOT gate is the same as of binary logic NOT gate only difference is the power supply used in tetrad logic is different.

![Tetrad logic NOT gate symbol](image)

Equation (1) shows the mathematical relation between input and output in tetrad logic. The observed output of the tetrad logic NOT gate can be understood from Table 2. Tetrad logic NOT truth table verified on Tanner W-Edit simulator.
Table 2. Tetrad logic NOT gate truth table

|       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|
| Vref=0v, Vref+=2V | x | Y | x | Y | x | Y | x | Y |
| 0     | 1     | 0    | 2    | 0    | 3    | 0    | 2 |
| 1     | 0     | 1    | 0    | 1    | 3    | 1    | 2 |
| 2     | 0     | 2    | 0    | 2    | 0    | 2    | 1 |
| 3     | 0     | 3    | 0    | 3    | 0    | 3    | 1 |
| Vref=2v, Vref+=6V | x | Y | x | Y |
| 0     | 3     | 0    | 3   |
| 1     | 3     | 3    | 3   |
| 2     | Uncertain | 2 | 0 |
| 3     | 0     | 3    | 0   |

Table 3 shown below shows the truth table of proposed Tetrad logic AND gate. The output of tetrad logic AND is minimum out of two inputs. Figure 3 shown below is the logical circuit of the proposed Tetrad-logic AND gate. Tetrad logic AND truth table output logic verified on the Tanner W-Edit simulator.

Table 3. Tetrad logic AND gate truth table

| Input | Output | Input | Output |
|-------|--------|-------|--------|
| 0     | 0      | 2     | 0      |
| 0     | 1      | 2     | 1      |
| 0     | 2      | 2     | 2      |
| 0     | 3      | 2     | 3      |
| 1     | 0      | 3     | 0      |
| 1     | 1      | 3     | 1      |
| 1     | 2      | 3     | 2      |
| 1     | 3      | 3     | 3      |

Figure 3. Tetrad logic AND gate and Proposed symbol for Tetrad AND logic

\[ \text{OUT} = \sim[(IN1 \land IN2)_{0}^{14}]_{t^{4}} \sim[(IN1 \land IN2)_{0}^{2}]_{t^{2}} \ldots \ldots (2) \]

\[ \text{OUT} = \sim[(IN1 \land IN2)]_{t} \ldots \ldots (3) \]
Equation (2) above shows input and output relation in tetrad AND login gate and equation (3) shows the proposed symbol for tetrad logic and gate.

\[ O_U^T = ~IN^1 \lor IN^2 \]  \hspace{1cm} \text{(4)}

\[ OUT = IN1 \cup IN2 \]  \hspace{1cm} \text{(5)}

Figure 4 shown above is the logical circuit of the proposed Tetrad-logic OR gate. Equation (4) above shows input and output relation in tetrad OR login gate and equation (5) shows the proposed symbol for tetrad logic and gate. Table 4 shown below is the truth table of the proposed 4 logic OR gate. The output of tetrad logic OR is maximum out of two input Tetrad logic OR truth table output logic verified on Tanner W-Edit simulator.

**Table 4.** Tetrad logic OR gate truth table

| Input | Output | Input | Output |
|-------|--------|-------|--------|
| 0     | 0      | 2     | 0      |
| 0     | 1      | 2     | 1      |
| 0     | 2      | 2     | 2      |
| 0     | 3      | 2     | 3      |
| 1     | 0      | 3     | 0      |
| 1     | 1      | 3     | 1      |
| 1     | 2      | 3     | 2      |
| 1     | 3      | 3     | 3      |

Table 5 shown is the tetrad logic flip flop truth table. It similar to D flip flop only set and reset is possible in proposed flip flop. Figure 5 shown below is the logical circuit of the proposed tetrad logic flip flop. The design uses tetrad logic NOT gates, tetrad logic AND gates, and tetrad logic OR gates.

**Table 5.** Tetrad Flip flop Truth table

| Clock     | Input | Old state O/P | New state O/P | State      |
|-----------|-------|---------------|---------------|------------|
| No event  | X     | 0             | 0             | No Change  |
| No event  | X     | 1             | 1             | No Change  |
| No event  | X     | 2             | 2             | No Change  |
| No event  | X     | 3             | 3             | No Change  |
Figure 5 below is proposed Tetrad flip flop memory cell that can store four logic levels as was defined in table 1.

\[
Q_{t+1} = ( \{ \sim clk \land Q_t \} \lor (CLK \land IN) \} \lor Q_t ) \land \{ (\sim clk \land Q_t) \lor (CLK \land IN) \} \lor \sim Q_t \]

\[
\sim Q_t \land \sim clk \land Q_t \lor (CLK \land IN) \]

… (6)

Equation 6 shows the tetrad flip-flop Clock, input, old and new output state relationship. The next value will be change only if a positive edge on the clock \( Q_{t+1} = IN \) and if the clock is off no change \( Q_{t+1} = Q_t \).

Figure 5. Tetrad logic flip flop

3. Results
Tanner Electronic device Automation (EDA) version 9.0  S-edit [15] used for layout schematic design, T-Spice [16] used for MOS parameter setting, and W-edit [17] used for verification of the Simulation results. Figure 6 below shows the Schematic design of CMOS Not gate with \( V_{ref-} = 2V \) and \( V_{ref+} = 4V \).

Figure 6. Tetrad NOT logic gate Schematic
Figure 7. W-Edit simulation obtain for Tetrad logic NOT gate when $V_{ref-} = 2V$ and $V_{ref+} = 4V$

Figure 7 shows simulation obtained for Tetrad logic NOT gate shown in figure 6. In figure 7 green line shows the input provided and the yellow line shows the output, it may be observed that for input logic 0 output is logic 2, for input logic 1 output is logic 2, for input logic 2 output is logic 1, and for input logic 3 output is logic 1. Similarly, all other tetrads NOT logic gates have been designed and results are verified with Table 2 and found correct.

Figure 8. Tetrad logic AND gate schematic

Figure 9. W-Edit simulation obtain for Tetrad logic AND gate
Figure 8 shows the schematic design of Tetrad logic AND gate and figure 9 shows simulation obtained for Tetrad logic AND gate shown in figure 8. In figure 9 the green and the yellow line shows the inputs provided and the sky-blue line shows the output, the output results of tetrad logic AND gate is verified with Table 3 and found correct.

Figure 10. Tetrad logic OR gate Schematic

Figure 11. W-Edit simulation obtain for Tetrad logic OR gate

Figure 10 above shows the schematic design of the tetrad logic OR gate and figure 11 shows simulation obtained for Tetrad logic OR gate shown in figure 10. In figure 11 the green and the yellow line shows the inputs provided and the sky-blue line shows the output, the output results of tetrad logic OR gate is verified with Table 4 and found correct.

Figure 12. Schematic design of proposed Tetrad logic flip flop
Figure 13. W-Edit simulation obtain for Tetrad logic Flip flop

Figure 12 above shows the schematic design of the proposed tetrad logic flip-flop gate and figure 13 shows simulation obtained for Tetrad logic flip-flop shown in figure 12. In figure 13 the green line is the clock signal, the yellow line shows the inputs provided by the user and the sky-blue line shows the output, it can be observed that the results are same as was expected and discussed in table 5. The proposed tetrad logic flip flop is capable of storing four logic levels and it is positive edge triggered, from simulation results it may be seen that the output of flip flop changes only when the positive edge of the clock appears and for storing anyone out of four logic we just need to stop the clock signal. In figure 13 it can be observed that between 400 to 500ns no clock provided and logic 3 gets store in flip flop. Figure 13 shows the proposed design of 4 logic ‘0’, ‘1’, ‘2’ and ‘3’ flip flop design which is capable of storing four logic instead of 2 logic as was in the binary system, Proposed four logic flip flop will need 2ⁿ less numbers of a binary flip flop for storing any number. Voltage levels, noise margin, Fan-out, sink & source current of TVL logic are defined in table1. The parameters of table1 have been verified on tanner EDA with DC and transient analysis. Table 6 below shows the result parameters observe on the simulation statics report generated on T-spice 9.0 for the proposed TVL designs.

Table 6. Results of proposed tetrad logic designs

| Design          | MOS count | Average power consumed | Transient time | Setup time |
|-----------------|-----------|------------------------|----------------|------------|
| Tetrad logic NOT| 2         | 1.57 mw                | 60 ns          | 10 ns      |
| Tetrad logic AND| 18        | 2.34 mw                | 400 ns         | 10 ns      |
| Tetrad logic OR | 18        | 2.21 mw                | 200 ns         | 10 ns      |
| Tetrad logic Flip Flop | 130 | 3.95 mw | 657 ns | 30 ns |

Table 7 shows the comparative results in comparison with MVL proposed work TVL uses less power and it has high fan-out then MVL. In comparison with QVL proposed TVL has better noise margin
and high fan out. In comparison with NVL proposed TVL has a better noise margin however TVL uses 2 extra MOS in comparison with NVL.

Table 7. Comparative Results of Flip flop design

|                      | N-Value Logic (NVL) [9] | Quad Value Logic (QVL)[12] | Multi-Value Logic (MVL) [13] | Tetrav Value Logic (TVL) This work |
|----------------------|-------------------------|----------------------------|-----------------------------|----------------------------------|
| MOS count            | 128                     | -                          | -                           | 130                              |
| Average power consumed| -                       | 3.96 mw                    | 4.2255 mw                   | 3.95 mw                          |
| Noise Margin         | 0.8 v                   | 0.9 v                      | 1 v                         | 1 v                              |
| Fan out              | 10                      | 2                          | 6                           | 10                               |
| Setup/Hold time      | 30 ns                   | -                          | -                           | 30 ns                            |

4. Conclusion

This work is a design of tetrad logic flip flop with help of new design of tetrad logic AND gate, tetrad logic NOT, and tetrad logic OR gate. It can be concluded that the proposed tetrad logic flip-flop requires less power, better fan-out, and good noise margin. Tetrad logic uses half numbers of flip-flops in comparison with binary logic for storing any number also the number of wires to carry signals are also half. All modules are simulated and verified successfully. The design was done using the Tanner S-Edit Schematic capture tool design parameter and command given on T-Spice, W-edit waveform generator is been used for observing and verifying the results. The tetrad value logic (TVL) can be used in future technology and near future tetrad flip flop can be used as a new energy-efficient technique for data storage.

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