A Non-linear GPU Thread Map for Triangular Domains

Cristóbal A. Navarro\textsuperscript{a,}\textsuperscript{*}, Benjamín Bustos\textsuperscript{b}, Nancy Hitschfeld\textsuperscript{b}

\textsuperscript{a}Instituto de Informática, Universidad Austral de Chile.
\textsuperscript{b}Departamento de Ciencias de la Computación, Universidad de Chile.

Abstract

There is a stage in the GPU computing pipeline where a grid of thread-blocks, in parallel space, is mapped onto the problem domain, in data space. Since the parallel space is restricted to a box type geometry, the mapping approach is typically a $k$-dimensional bounding box (BB) that covers a $p$-dimensional data space. Threads that fall inside the domain perform computations while threads that fall outside are discarded at runtime. In this work we study the case of mapping threads efficiently onto triangular domain problems and propose a block-space linear map $\lambda(\omega)$, based on the properties of the lower triangular matrix, that reduces the number of unnecessary threads from $O(n^2)$ to $O(n)$. Performance results for global memory accesses show an improvement of up to 18\% with respect to the bounding-box approach, placing $\lambda(\omega)$ on second place below the rectangular-box approach and above the recursive-partition and upper-triangular approaches. For shared memory scenarios $\lambda(\omega)$ was the fastest approach achieving 7\% of performance improvement while preserving thread locality. The results obtained in this work make $\lambda(\omega)$ an interesting map for efficient GPU computing on parallel problems that define a triangular domain with or without neighborhood interactions. The extension to tetrahedral domains is analyzed, with applications to triplet-interaction n-body applications.

Keywords: block-space mapping, data re-organization, triangular domain

1. Introduction

GPU computing has become a well established research area since the release of programmable graphics hardware and its programming platforms such as CUDA and OpenCL. In the CUDA GPU programming model there are three constructs that allow the execution of highly parallel algorithms; (1) thread, (2) block and (3) grid. Threads are the smallest elements and they...
are in charge of executing the instructions of the GPU kernel. A block is an intermediate structure that contains a set of threads organized as an Euclidean box. Blocks provide fast shared memory access as well as local synchronization for all of its threads. The grid is the largest construct of all three and it keeps all blocks together spatially organized for the execution of a GPU kernel. These three constructs play an important role when mapping the execution resources to the problem domain.

For every GPU computation there is a stage where threads are mapped onto the problem domain. A map, defined as \( f : \mathbb{R}^k \rightarrow \mathbb{R}^p \), transforms each \( k \)-dimensional point \( x = (x_1, x_2, ..., x_k) \) of the grid into a unique \( p \)-dimensional point \( f(x) = (y_1, y_2, \cdots, y_p) \) of the problem domain. Since the grid lives in parallel space, we have that \( f(x) \) maps the parallel space onto the data space. In GPU computing, a typical mapping approach is to build a bounding-box (BB) type of parallel space, sufficiently large to cover the data space and map threads using the identity \( f(x) = x \). Such map is highly efficient for the class of problems where data space is defined by a \( p \)-dimensional box, such as vectors, lists, matrices and box-shaped volumes. For this reason, the identity map is typically considered as the default approach.

There is a class of parallel problems where data space follows a triangular organization. Problems such as the Euclidean distance maps (EDM) [6, 7, 8], collision detection [9], adjacency matrices [10], cellular automata simulation on triangular domains [11], matrix inversion [12], LU/Cholesky decomposition [13] and the n-body problem [14, 15, 16], among others, belong to this class and are frequently encountered in the fields of science and technology. In this class, data space has a size of \( D = n(n+1)/2 \in \mathcal{O}(n^2) \) and is organized in a triangular way. This data shape makes the default bounding-box (BB) approach inefficient as it generates \( n(n-1)/2 \in \mathcal{O}(n^2) \) unnecessary threads (see Figure 1).

**Figure 1**: The BB strategy is not the best choice for a td-problem.

For each unnecessary thread, a set of instructions must be executed in order to discard themselves from the useful work, leading to a performance penalty that can become notorious considering that fine-grained parallelism usually produces thousands of threads with a small amount of work per thread. In this
context, it is interesting to study how one can reduce the number of unnecessary threads to a marginal number and eventually produce a performance improvement for all problems in this class. Throughout the paper, this class will be referred as the **triangular-domain** class or simply **TD**.

This work addresses the problem depicted in Figure 1 and proposes a block-space map $\lambda(\omega)$ designed for the TD class that reduces the number of unnecessary threads to $o(n^2)$, making kernel execution up to 18% faster than the BB approach in global memory scenarios and up to 7% faster in shared memory tiled scenarios. The rest of the paper includes a description of the related works (Section 2), a formal definition for $\lambda(\omega)$ (Section 3), an evaluation of square root implementations (Section 4), a performance comparison with the related works (Section 5) and an extension of the strategy to tetrahedral domains with its potential performance benefit (Section 6).

2. Related Work

In the field of distance maps, Ying *et. al.* have proposed a GPU implementation for parallel computation of DNA sequence distances [17] which is based on the Euclidean distance maps (EDM). The authors mention that the problem domain is indeed symmetric and they do realize that only the upper or lower triangular part of the interaction matrix requires computation. Li *et. al.* [7] have also worked on GPU-based EDMs on large data and have also identified the symmetry involved in the computation.

Jung *et. al.* [18] proposed packed data structures for representing triangular and symmetric matrices with applications to LU and Cholesky decomposition [13]. The strategy is based on building a *rectangular box strategy* (RB) for accessing and storing a triangular matrix (upper or lower). Data structures become practically half the size with respect to classical methods based on the full matrix. The strategy was originally intended to modify the data space (i.e., the matrix), however one can apply the same concept to the parallel space.

Ries *et. al.* contributed with a parallel GPU method for the triangular matrix inversion [12]. The authors identify that the parallel space indeed can be improved by using a *recursive partition* (REC) of the grid, based on a **divide and conquer** strategy.

Q. Avril *et. al.* proposed a GPU mapping function for collision detection based on the properties of the upper-triangular map [9]. The map, referred here as **UTM**, is a thread-space function $u(x) \rightarrow (a, b)$, where $x$ is the linear index of a thread $t_x$ and the pair $(a, b)$ is a unique two-dimensional coordinate in the upper triangular matrix. Their map is accurate in the domain $x \in [0, 100M]$, with a range of $(a, b) \in [0, 3000]$.

The present work is an extended and improved version of a previous conference research by Navarro and Hitschfeld [21].
3. Block-space triangular map

3.1. Formulation

It is important to distinguish between two possible approaches; (1) thread-space mapping and (2) block-space mapping. Thread-space mapping is where each thread uses its own unique coordinate as the parameter for the mapping function. The approach has been used before in the work of Avril et. al. [9]. On the other hand, block-space mapping uses the shared block coordinate to map to a specific location, followed by a local offset on each thread according to the relative position in their block. This approach has not been considered by the earlier works and it has been chosen as it can give certain advantages over thread-space mapping specially on memory access patterns.

For a problem in the TD class of linear size $n$, its total size is $n(n+1)/2$. Let $m = \lceil n/\rho \rceil$ be the number of blocks needed to cover the data space along one dimension and $\rho$ the number of threads per block per dimension, or dimensional block-size (for simplicity, we assume a regular block). A bounding-box mapping approach would build a box-shaped parallel space, namely $P_{BB}$, of $m \times m$ blocks and put conditional instructions to cancel the computations outside the problem domain. Although the approach is correct, it is inefficient since $m(m+1)/2$ blocks are already sufficient when organized as:

$$D = \begin{bmatrix}
0 & 2 & & & \\
1 & 3 & 4 & 5 & \\
& \cdots & \cdots & \cdots & \cdots \\
\frac{m(m-1)}{2} & \frac{m(m-1)}{2} + 1 & \cdots & \cdots & \frac{m(m+1)}{2} - 1
\end{bmatrix} \quad (1)$$

We define a balanced two-dimensional parallel space $P_\Delta$ (see Figure [2]) of size of $m' \times m'$ blocks where $m' = \left\lceil \sqrt{m(m+1)/2} \right\rceil$. This setup reduces the number of unnecessary threads from $n(n-1)/2 \in O(n^2)$ to $\frac{\rho(\rho-1)}{2} \lceil n/\rho \rceil < \frac{\rho^2}{2} \lceil n/\rho \rceil \in o(n^2)$ threads, with $\rho \in O(1)$.

**Figure 2:** parallel space $P_\Delta$ is sufficient to cover the problem domain.
Spaces $P_\Delta$ and $D$ are both topologically equivalent, therefore the map has to be at least a homeomorphism from block coordinates to unique two-dimensional coordinates in the triangular data space.

**Theorem 3.1.** There exists a non-linear homeomorphism $\lambda : \mathbb{Z}^1 \rightarrow \mathbb{Z}^2$ that maps any block $B_{i,j} \in P_\Delta$ onto the TD class.

**Proof.** Let $\omega$ be the linear index of a block, expressed as

$$\omega = \sum_{r=1}^{x} r \quad (2)$$

From expression (2), one can note that the index of the first data element in the row of the $\omega$-th linear block corresponds to the sum in the range $[1, i]$, where $i$ is the row for the $\omega$-th block. Similarly, the index of the first block from the next row is a sum in the range $[1, i+1]$. Therefore, for all $\omega$ values of the $i$-th row, their summation range is bounded as

$$\sum_{r=1}^{i} r \leq \lambda = \sum_{r=1}^{i+x} r < \sum_{r=1}^{i+1} r \quad (3)$$

with $\epsilon < 1$. With this, we have that $x \in \mathbb{R}$ and most importantly that $i = \lfloor x \rfloor$. Since $\sum_{r=1}^{x} r = x(x+1)/2$, $x$ is found by solving the second order equation $x^2 + x - 2\omega = 0$ where the solution $x = \sqrt{1/4 + 2\omega} - 1/2$ allows the formulation of the homeomorphism

$$\lambda(\omega) = (i, j) = \left(\left\lfloor \sqrt{\frac{1}{4} + 2\omega} - \frac{1}{2} \right\rfloor, \omega - i(i + 1)/2 \right) \quad (4)$$

which is non-linear since $\exists \omega_1, \omega_2 \in P_\Delta : g(\omega_1 + \omega_2) \neq g(\omega_1) + g(\omega_2)$, e.g., $\omega_1 = 4, \omega_2 = 3 \implies g(7) = (3, 1) \neq g(4) + g(3) = (4, 1)$.

If the diagonal is not needed, then $\lambda(\omega)$ becomes:

$$\lambda(\omega) = (i, j) = \left(\left\lfloor \sqrt{\frac{1}{4} + 2\omega} + \frac{1}{2} \right\rfloor, \omega - i(i + 1)/2 \right) \quad (5)$$

There are three important differences when comparing $\lambda(\omega)$ with the UTM map [9]: (1) $\lambda(\omega)$ maps in block-space and not in thread-space as in UTM, allowing larger values of $n$, (2) thread organization and locality is not compromised, making nearest-neighbors computations efficient for shared memory and (3) $\lambda(\omega)$ uses fewer floating point operations than in UTM since it uses a lower-triangular approach.

### 3.2. Bounds on the improvement factor

The reduction of unnecessary threads from $O(n^2)$ to $O(n)$ may suggest that the improvement could reach a factor of up to $2 \times$. For this to be possible, one
would need to measure just the mapping stage, so that necessary and unneces-
sary threads do similar amount of work, and assume that the mapping function
\( \lambda(\omega) \) is as cheap as in the BB strategy. In the following analysis we analyze
the improvement factor considering a more realistic scenario where \( \lambda(\omega) \) has a
higher cost than the BB map, due to the square root computation involved.

The performance of \( \lambda(\omega) \) strongly depends on the square root which in theory
costs \( O(M(n)) \) [20] where \( M(n) \) is the cost of multiplying two numbers of \( n \)
digits. Considering that real numbers are represented by a finite number of
digits (i.e., floating point numbers with a maximum of \( m \) digits), then all basic
operations cost a fixed amount of time, leading to a constant cost \( M(m) = C_s \in O(1) \).
All other computations are elemental arithmetic operations and can be taken as an
additional cost of \( C_a \in O(1) \). The total cost of \( \lambda(\omega) \) is
\( \tau = C_s + C_a = O(1) \) for each mapped thread. On the other hand, the BB
strategy uses the identity map and checks for each thread if \( B_j < B_i \) in order
to continue or be discarded, leading to a constant cost of \( \beta \in O(1) \). It is indeed
evident that \( \beta \) is cheaper than \( \tau \), therefore \( \tau = k\beta \) with a constant \( k \geq 1 \). The
improvement factor \( I \) can expressed as

\[
I = \frac{\beta|P_{BB}|\rho^2}{\tau|P_{\Delta}|\rho^2} = \frac{2\beta N_B^2}{\tau N_D^2 + \tau N_D} = \frac{2\beta [n/\rho]^2}{\tau ([n/\rho]^2 + [n/\rho])}
\]

For large \( n \) the result approaches to

\[
\lim_{n \to \infty} I = \frac{2\beta}{\tau}
\]

Using the relation \( \tau = k\beta \) in (7) we have \( I \approx 2/k \) for large \( n \) and since \( k > 1 \),
the final range for \( I \) becomes

\[
0 < I < 2
\]

The parameter \( k \) can be interpreted as the penalty factor of \( \lambda(\omega) \), where the
lowest value is desired. In practice, a value \( k \approx 1 \) is too optimistic. Given how
actual GPU hardware works, one can expect that the cost of the square root
will dominate the \( k \) parameter.

4. Implementation

This section presents technical details on choosing a proper square root
implementation for \( \lambda(\omega) \) as well as a general description of the related works chosen
for performance comparison later on.

4.1. Choosing a proper square root

The performance of map \( \lambda(\omega) = (i, j) \) depends, in great part, on how fast
the square root from eq. (4) is computed. Three versions of \( \lambda(\omega) \) have been
implemented, each one using a different method for computing the square root.
Results from each test are computed as the improvement factor with respect to
the BB strategy. The first implementation, named $\lambda_X$, uses the default $\text{sqrtf}(x)$ function from CUDA C and it is the simplest one.

The second implementation, named $\lambda_N$, computes the square root by using three iterations of the Newton-Raphson method \[20, 19\] which is available from the implementation of Carmack and Lomont. This square root implementation has proved to be effective for applications that allow small errors. The initial value used is the magic number “0x5f3759df” (this value became known when ‘Id Software’ released Quake 3 source code back in the year 2005). Adding a constant of $\epsilon = 10^{-4}$ to the result of the square root can fix approximation errors in the range $N \in [0, 30720]$.

The third implementation, named $\lambda_R$, uses the hardware implemented reciprocal square root, $\text{rsqrtf}(x)$:

$$\sqrt{x} = \frac{x}{\sqrt{x}} = x \cdot \text{rsqrtf}(x)$$

In terms of simplicity, $\lambda_R$ is similar to $\lambda_X$, with the only difference that it adds $\epsilon = 10^{-4}$ at the end to fix approximation errors, just like in $g_2$.

For each implementation a performance improvement factor was obtained with respect to BB strategy, by running a dummy kernel that computes the $i, j$ indices and writes the sum $i+j$ to a constant location in memory. It is necessary to perform at least one memory access otherwise the compiler can optimize the code removing part of the mapping cost. Figure 3 shows the improvement factor as $I = BB/\lambda(\omega)$ using the three different implementations, running on three different Nvidia Kepler GPUs; GTX 680, GTX 765M and Tesla K40.

Figure 3: Performance of the different square root strategies.

From the results, we observe that $\lambda_X$ is slower than BB when running on the GTX 680 and GTX 765M, achieving $I_{680} \approx 0.87$ and $I_{765M} \approx 0.83$, respectively. For the same two GPUs, $\lambda_X$ achieves an improvement of $I_{680} \approx 1.025$ and
\( I_{765M} \approx 0.96 \) which is practically the performance of BB. Lastly, \( \lambda_R \) achieves improvements of \( I_{680} \approx 1.15 \) and \( I_{765M} \approx 1.1 \). From these results, we observe that using the inverse square root is the best option for the GTX 680 and GTX 765M. For the case of the Tesla K40, we observe that all three implementations achieve an improvement of \( I_{K40} \approx 1.08 \), allowing to have the precision of \( \lambda_X \) with the performance of \( \lambda_R \).

4.2. Implementing the other strategies

The strategies from the relevant works, including the default one from CUDA, were implemented as well: bounding-box (BB), rectangle-box (RB), recursive-partition (REC) and upper-triangular-matrix (UTM) following the details provided by the authors [18, 19, 12]. To each implementation the following restriction was added: the map cannot use any additional information that grows as a function of \( N \). This means no auxiliary array such as lookup tables are allowed, only small constants size data if needed. The purpose of such constraint is to guarantee that GPU memory is dedicated to the application problem.

For the bounding box (BB) strategy, blocks above the diagonal are discarded at runtime, without needing to compute a thread coordinate as it can be done by checking if \( B_i > B_j \) is true or not in the kernel. Threads that got a true result from the conditional proceed to compute their global coordinate and do the kernel work. The condition \( i > j \) is still performed to discard threads on blocks where \( B_i = B_j \). It is important to note that this implementation of BB is faster than computing the thread coordinate first and filtering afterwards.

The rectangular box (RB) takes a sub-triangular portion of the threads where \( t_x > N/2 \), rotates it counter-clock-wise (CCW) and places it above the diagonal to form a rectangular grid (see Figure 4, left).

![Rectangular Box (RB)](image1)

![Recursive Partition (REC)](image2)

**Figure 4:** On the left, the rectangular-box (RB). On the right, the recursive-partition (REC).

The original work was actually a memory packing technique in data space, but the principle can be applied to the parallel space as well. For this, the lookup texture is no longer used and instead the mapping coordinates are computed at runtime. All threads below the diagonal just need to map to \( i = t_y - 1 \), while \( j \) remains the same, and threads in or above the diagonal map to \( i = \)
An important feature of the RB map is that the number of unnecessary threads is asymptotically $O(1)$.

The recursive partition (REC) \cite{12} strategy was originally proposed for matrix inversion problem. In this strategy the size of the problem is defined as $N = m2^k$ where $k$ and $m$ are positive integers and $m$ is a multiple of the block-size $\rho$. The idea is to do a binary bottom-up recursion of $k$ levels (see Figure 4, right), where the $i$-th level has half the number of blocks of the $(i-1)$-th level, but with doubled linear size. This method requires an additional pass for computing the blocks at the diagonal (level $k = 0$ is a special one). More details of how the grid is built and how blocks are distributed are well explained in \cite{12}. In the original work, the mapping of blocks to their respective locations at each level is achieved by using a lookup table stored in constant memory. In this case, the lookup table is discarded and instead the mapping is done at runtime.

The upper-triangular mapping (UTM) was proposed by Avril et. al. \cite{9} for performing efficient collision detection on the GPU. Given a problem size $N$ and a thread index $k$, its unique pair $(a, b)$ is computed as $a = \lfloor \frac{(2n+1)+\sqrt{4n^2-4n-8k+1}}{2} \rfloor$ and $b = (a+1) + k - \frac{(a-1)(2n-a)}{2}$. The UTM strategy uses the idea of mapping threads explicitly to the upper-triangular matrix, making it a thread space map.

5. Performance Results

The experimental design consists of measuring the performance of $\lambda(\omega)$ and compare it against the bounding box (BB), rectangular box (RB) \cite{18}, the recursive partition (REC) \cite{12} and upper-triangular mapping (UTM) \cite{9}. Three tests are performed to each strategy; (1) the dummy kernel, (2) EDM and (3) Collision detection. Test (1) just writes the $(i, j)$ coordinate into a fixed memory location. The purpose of the dummy kernel is to measure just the cost of the strategy and not the cost of the application problem. Test (2) consists of computing the Euclidean distance matrix (EDM) using four features, i.e., $(x, y, z, w)$ where all of the data is obtained from global memory. Test (3) consists of performing collision detection of $N$ spheres with random radius inside a unit box. The goal of this last test is to measure the performance of the kernels using a shared memory approach.

The reason why these tests were chosen is because they are simple enough to study their performance from a GPU map perspective and use different memory access paradigms such as global memory and shared memory. Based on these arguments, it is expected that the performance results obtained by these three tests can give insights on what would be the behavior for more complex problems that fall into one of the two memory access paradigms. Furthermore, the tests have been ran on three different GPUs in order to check if the results vary under older or newer GPU architectures. The details on the maximum number of simultaneous blocks (sblocks) for each GPU used are listed in Table \ref{table:1}.

Performance results for the dummy kernel, 4D-EDM and collision detection in 1D/3D are presented in Figure 5. Graphic plots the performance of all four
Table 1: Hardware used for experiments.

| Device | Model       | Architecture | Memory | Cores | sblocks |
|--------|-------------|--------------|--------|-------|---------|
| GPU1   | GeForce GTX 765M | GK106        | 2GB    | 768   | 80      |
| GPU2   | GeForce GTX 680 | GK104        | 2GB    | 1536  | 128     |
| GPU3   | Tesla K40   | GK110        | 12GB   | 2880  | 240     |

strategies as different dashed line colors, while the symbol type indicates which GPU was chosen for that result. The performance of each mapping strategy is given in terms of its improvement factor $I$ with respect to the BB strategy (i.e., the black and solid horizontal line fixed at $I = 1$). Values that are located above the horizontal line represent actual improvement, while curves that fall below the horizontal line represent a slowdown with respect to the BB strategy.

For the dummy kernel test the plots shows that the RB strategy is the fastest one achieving up to 33% of improvement with respect to BB when running on the GTX 765M. Map $A(\omega)$ comes in the second place, achieving a stable improvement of up to 18% when running on the GTX 680. The REC and UTM strategies performed slower than BB for the whole range of $N$. We note that this test running on the Tesla K40 does not show any clear performance difference.

Figure 5: Improvement factors for the dummy kernel, Euclidean distance matrix and collision detection.
among the mapping strategies once $N > 15000$, as they all converge to a 7% of improvement with respect to BB.

For the EDM test, RB is again the fastest map achieving an improvement of up to 28% with respect to BB when running on the Tesla K40 GPU. In second place comes $\lambda(\omega)$ with a stable improvement of 18% and third the REC map with an improvement that reaches up to 12% for the largest $n$. The performance of the UTM strategy was lower than BB and unstable for all GPUs. It is important to consider that UTM was designed to work in the range $n \in [0, 3000]$, where it actually does perform better than BB offering up to 4% of improvement over BB. For this test, performance differences among the strategies did manifest for all GPUs, including the Tesla K40.

For the 3D collision detection test only $\lambda(\omega)$ manages to perform better than BB, offering an improvement of up to 7%. Indeed, the performance scenario changes drastically in the presence of a different memory access pattern such as shared memory; the RB strategy, which was the best in global memory, now performs slower than BB. The case is similar with the REC map which now performs much slower than BB. It is important to mention that the UTM map is the only strategy that cannot use a 2D shared memory pattern because the mapping works in linear thread space. At low $n$, UTM achieves a 100% of improvement because of the different memory approach used, thus it cannot be taken as a practical improvement. Furthermore, as $n$ grows, its performance is over passed by the rest of the strategies that use shared memory. For the case of 1D collision detection, results are not so beneficial for the mapping strategies and in the case of $\lambda(\omega)$ it is in the limit of being an improvement. The 1D results show that in low dimensions the benefits of a mapping strategy can be not as good as in higher ones.

6. Extension to 3D Tetrahedrons

In this section, the potential benefit of $\lambda(\omega)$ is considered for 3D cases as an extension of the 2D approach. The three-dimensional analog of the 2D triangle corresponds to the 3D discrete tetrahedron, which may be defined by $n$ triangular structures stacked and aligned at their right angle, where the $r$-th triangular layer contains $T^{2D}_r = r(r+1)/2$ elements. The total number of elements for the full structure can be expressed in terms of the $n$ layers:

$$T_n = \sum_{r=1}^{n} T^{2D}_r = \sum_{r=1}^{n} \frac{r(r+1)}{2}$$

(10)

The sequence corresponds to the tetrahedral numbers, which can be defined by

$$T_n = \left(\frac{n+2}{3}\right) = \sum_{r=1}^{n} T^{2D}_r = \frac{n(n+1)(n+2)}{6}$$

(11)

Similar to the 2D case, a canonical map $f(x) = x$ with a box-shaped parallel space leads to an inefficiency as the number of unnecessary threads is in the order of $O(n^3)$ as illustrated by Figure 6.
A more efficient approach can be formulated by considering how block indices can map onto the tetrahedron. More precisely, it is possible to redefine $\lambda$ as a map $\lambda(\omega) : \mathbb{N} \rightarrow \mathbb{N}^3$ that works on the tetrahedral structure without loss of parallelism (see Figure 7).

The approach takes advantage of the fact that when using a linear enumeration of blocks on the tetrahedron, the $\omega$ index of the first element of a 2D triangular layer corresponds to a tetrahedral number $T_x$. Similar to the previous two-dimensional row analysis, now that data elements that reside in the same layer obey the following property

$$\sum_{r=1}^{k} r(r+1)/2 < \omega = \sum_{r=1}^{x} r(r+1)/2 < \sum_{r=1}^{k+1} r(r+1)/2.$$

When expressing $\omega$ as the tetrahedral number

$$\omega = \sum_{r=1}^{x} r(r+1)/2 = \frac{x(x+1)(x+2)}{6},$$

the $k$ component of the $(i, j, k)$ coordinate of block $\omega$ can be obtained by solving
the third order equation

\[ x^3 + 3x^2 + 2x - 6\omega = 0 \] (14)

and extracting the integer part of the root

\[ x = \frac{3\sqrt[3]{729\omega^2 - 3 + 27\omega}}{2} + \frac{1}{\sqrt[3]{3\sqrt[3]{729\omega^2 - 3 + 27\omega}}} - 1 \] (15)

Once the value \( k = \lfloor x \rfloor \) is computed, the \( \omega_{2D} \) linear coordinate

\[ \omega_{2D} = \omega - T_k \] (16)

can be obtained as well, where \( T_k = k(k+1)(k+2)/6 \) is the tetrahedral number for the recently computed \( k \) value. With \( \omega_{2D} \) computed, the \( i \) and \( j \) values of the block can be computed using the two-dimensional version of \( \lambda(\omega) \). Combining all three sub-results, the tetrahedral map \( \lambda(\omega) \) becomes

\[ \lambda(\omega) \mapsto (i, j, k) = \left( \omega_{2D} - T_y^{2D}, \left\lfloor \sqrt[1/2]{1 + 2\omega_{2D} - \frac{1}{2}} \right\rfloor, \lfloor v \rfloor \right) \] (17)

The blocks in parallel space can be organized on a cubic grid of side \( \lceil \sqrt[3]{n} \rceil \) in order to balance the number of elements on each dimension, producing \( n^2 \rho^3 \in o(n) \) unnecessary threads. The potential improvement factor of the block-space map with respect to the bounding box is

\[ I = \frac{\alpha n^3 / \rho^3}{\gamma T_n / \rho^3} = \frac{6\alpha n^3}{\gamma (n^3 + 3n^2 + 2n)} \] (18)

where \( \alpha \) is the cost of computing the block coordinate using the box approach, while \( \gamma \) is the cost of mapping blocks onto the tetrahedral map. In the infinite limit of \( n \), the potential improvement becomes

\[ I_{n \to \infty} \sim \frac{6\alpha}{\gamma} \] (19)

and tells that in theory the tetrahedral map could be close to 6 \times more efficient for large \( n \). However, such improvement can only be possible if \( \gamma \sim \alpha \), i.e., if the square and cubic roots can be computed fast enough to be comparable to the cost of the bounding-box approach, which is very unlikely to happen in practice. Nevertheless, there still can be valuable improvement as long as \( \gamma < 6\alpha \).

7. Conclusions

The mapping technique studied in this work may be a useful optimization for GPU solutions of parallelizable problems that have a triangular or tetrahedral domain. The map proposed in this work, namely \( \lambda(\omega) \), proved to be the fastest strategy (with 7\% of improvement over the bounding-box) when dealing
with shared memory scenarios that require locality, which is a computational pattern often found in scientific and engineering problems where information of nearest neighbors is accessed. Since the map is performed in block-space, thread locality is not compromised allowing to integrate the optimization with other optimization techniques such as block-level data re-organization or coalesced data sharing among threads. The implementation of $\lambda(\omega)$ is short in code and totally detached from the problem, making it easy to adopt it as a self-contained function with no side effects.

The performance of the map varies depending on which GPU is used and on the way the map computations are performed. It is of high interest to study even more optimized square root routines as they have a great impact on the performance of $\lambda(\omega)$.

Extensions to the 3D tetrahedron are worth inspecting in more detail as they have the potential of being up to 6× more efficient regarding parallel space. This improvement can traduce to a performance increase only if the cost of cubic and square root computations is low enough to the same order of the bounding box approach. Although tetrahedral domain problems are less frequently found, they are still important in science when solving triplet-interaction n-body problems. An interesting approach for the implementation of the 3D map would be to reconsider relaxing the condition of allowing extra data and introduce a type of succinct lookup table of $o(T_n)$ combined with coordinate computations in order to balance and overlap the use of numerical and memory operations.

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