The DAQ and control system for JadePix3

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ABSTRACT: The silicon pixel sensor is the core component of the vertex detector for the Circular Electron Positron Collider (CEPC). The JadePix3 is a full-function large-size CMOS chip designed for the CEPC vertex detector. To test all the functions and the performance of this chip, we designed a test system based on the IPbus framework. The test system controls the parameters and monitors the status of the pixel chip. By integrating the jumbo frame feature into the IPbus suite, the block read/write speed is further extended in order to meet the specifications of the JadePix3. The robustness, scalability, and portability of this system have been verified by pulse test, cosmic test and laser test in the laboratory. This paper summarizes the DAQ and control system of the JadePix3 and presents the first results of the tests.

KEYWORDS: Data acquisition concepts; Control and monitor systems online; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases)

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1 Introduction

The CEPC has been proposed as a Higgs factory to measure the Higgs boson properties and explore new physics [1]. It is designed to run with a center mass energy of about 240 A GeV. To meet the stringent physics requirements, it is necessary to design and construct high efficiency and precision charged particle tracking and vertex detectors. The silicon pixel detector is the core component of the vertex detector.

A prototype sensor, namely JadePix3, has been developed for the vertex detectors. The goals of the JadePix3 project are to study the designs of high spatial resolution, low power consumption, modest readout speed and small-size front-end circuits. Figure 1 shows the diagram of the JadePix3 design and the layout of the chip. The JadePix3 is a CMOS pixel sensor designed based on TowerJazz CIS 180 nm. The total size of the chip is 10.4 × 6.1 mm² (512 × 192 pixels), the minimal size of the pixel is 16 × 23.11 µm².
Rolling shutter readout structure is adopted for its simple structure, there are more possibilities to reduce the pixel size. The main circuit structure of the rolling shutter mode is the row address decoder, which is located on the periphery of the pixel array. The working mode of rolling shutter is to read one row at a time, turn on the output switch of one row through the control line of the row distribution, and reset the register of the previous row at the same time. The JadePix3 uses a weak inversion current comparator to amplify and discriminate the signals in the pixel. The threshold signal is stored in the register in the pixel and to be read out by row-by-row scanning. The scanning speed is 192 ns per row, and the time to complete a frame is 98.3 μs.

![Figure 1: The layout and design diagram of the JadePix3.](image)

The JadePix3 test system needs to verify all the modules of the JadePix3, including sensing diode, analog front-end, a digital circuit in the pixel, rolling shutter, zero compression and data buffering, serializer and serial output, DAC module, SPI module, and two independent design verification modules, LVDS and bandgap reference source.
2 System implementation

2.1 Overview

An overview of the JadePix3 test system is shown in Figure 2. The test system includes the chip to be tested, the FPGA readout board, the daughter board, and the control and data acquisition system based on the IPbus framework.

Figure 2: Overview of the DAQ and control system of the JadePix3 pixel detector.

2.1.1 Readout board

The test system of the JadePix3 has been developed using a commercial FPGA board[2] (Xilinx, KC705) as the Read Out Board (ROB). The industry-standard FPGA Mezzanine Connectors (FMC) on KC705 allows scaling and customization with daughter cards. It provides numerous Input/Output (IO) ports (single-ended and differential), and the IO level is compatible with 1.8 V and 2.5 V. The HPC FMC connector provides ten serial transceiver pairs, 160 single-ended signals (or 80 differential pairs) and clock signals. The high-density FMC interface on KC705 can meet the connection requirements of all IO ports on JadePix3. The KC705 evaluation board has 1 GB of DDR3 memory and a network transmission bandwidth of up to 1000 Mbps, which can provide sufficient data buffering and sending and receiving capabilities. Figure 3 shows the KC705 used in the test system.

Figure 3: The readout board adopted in the test system.
2.1.2 Daughter board

A daughter board contains a JadePix3 chip was designed for testing. Besides the JadePix3 chip, low voltage (LV) power supplies, a digital to analog converter (DAC70004) and an FMC connector are also mounted on the daughter board. The LV power supplies provide 1.8 V to the JadePix3 and 3.3 V to the DAC70004. The DAC70004 output test signals (analog pulse, reset) to the JadePix3 chip. The readout board controls all these chips via the FMC connector. Figure 4 is the front view of the daughter board.

Figure 4: The daughter board designed for the test system.

2.1.3 IPbus protocol and suite

The IPbus software and firmware suite were developed for the level one trigger upgrade for the CMS experiment. A high-performance control link is implemented based on the IPbus protocol for particle physics. The typical usage of IPbus is reading and modifying memory-mapped resources within FPGA-based IP-aware hardware devices.

The IPbus protocol defines the following operations: Read, Write, Read-Modify-Write bits, Read-Modify-Write sum. For each operation, the IPbus client sends a request to the IPbus device, then the device sends back a response message containing an error code and returns data in case of a reading operation. User Datagram Protocol (UDP) is a very simple protocol, and can be easily implemented in software and firmware. Though it is not unreliable compared to Transmission Control Protocol (TCP), the packet loss on a dedicated network is in reality very low, hence it can be adopted in many applications. So UDP is selected as the transport protocol[3]. In addition, the IPbus 2.0 protocol can correct UDP packet loss, re-ordering or duplication automatically by using the IPbus reliability mechanism.

The IPbus suite consists of the following components: IPbus firmware, ControlHub and µHAL. The IPbus firmware is a module that implements the IPbus protocol within end-user hardware. The ControlHub is a packet-handling software to allow separation of hardware and control networks. Hence, the IPbus suite can form a large-scale system base on the communication between multiple ControlHubs and the communication between ControlHubs and devices. Though the minimum configuration is used in the test system, the readout architecture can be easily expanded by considering multi-chip readout situations, such as beam test. Figure 5 shows the topology of an example large-scale IPbus control system, with many IPbus devices, and the control/monitoring applications spread across many computer nodes.
Figure 5: The topologies of a large-scale IPbus control system.

The ControlHub implements the IPbus reliability mechanism for the UDP packets traveling between the ControlHub and the IPbus target devices. µHAL is the micro Hardware Access Library providing C++/Python API for IPbus operations defined in the IPbus protocol.

2.1.4 IPbus jumbo frame feature

In most cases, the IPbus framework is applied to slow control systems, mainly based on its design purpose and the limitation of readout speed. So far, IPbus supports up to 1G Ethernet transmission. The single-word read/write latency for one device and one software client is approximately 250 ms, and the block read/write throughput for payloads larger than 1 Mbyte is above 0.5 Gb/s[4]. Though the IPbus suite is usually adopted as a slow control system, the data transmission capacity is also possible enough for a small-scale detector testing system. The readout speed specified in the CEPC Conceptual Design Report (CDR) is in the range of 1–100 µs [5]. The goal of the JadePix3 design is 100 µs based on the research purpose. The maximum data rate will be \(\approx 10.9 \text{ hit} \cdot \text{cm}^{-2} \cdot \text{µs}^{-1}\). With these indicators, we can calculate the maximum hit number in each frame.

\[
Hit_{\text{Max}} = DataRate \times ChipSize \times FramePeriod = 10.9 \times \frac{10.4 \times 6.1}{100} \times 98.316 = 680 \quad (2.1)
\]

The rate of raw data is \(DataRate_{\text{raw}} = \frac{680 \times 32}{98.316} \text{Mbps} \approx 221 \text{Mbps}\). If the multiplicity parameter is considered, an event may generate 3 data (according to the beam current test results of similar sensors), then the transmission speed of the data link needs to reach 663 Mbps. Therefore, the readout ability of IPbus needs to be improved if we want to implement the JadePix3 DAQ system by the IPbus framework.

In order to improve the speed of block read/write operation, the jumbo frame feature has been added to the IPbus suite. IEEE 802.3 Ethernet standard only supports 1500 byte frame maximum transmission unit (MTU), with a total frame size of 1518 bytes, jumbo frames can carry up to 9000 bytes of payload. The usage of jumbo frames can reduce overheads and CPU cycles, make the performance of Gigabit Ethernet fully play and increase the data transmission efficiency.
To achieve this feature, the number and depth of FIFOs Ethernet module of IPbus firmware need to be increased, the number is increased from 16 to 32, and the FIFO depth is increased from $2^{11}$ to $2^{13}$. At the same time, the underlying protocol parameters of the IPbus µHAL also need to be modified accordingly, including Maximum Send Size, Maximum Reply Size and Reply Memory Size in TCP and UDP protocols. With the changes mentioned above, an IPbus packet can now carry data with a size of 8140 bytes. By continuously filling the FIFO with data to form a continuous large data stream (0.5 MB payload), the block read speed reaches 750 Mbps. With this feature implemented, the IPbus block read/write speed and efficiency are improved and can be used as a small-scale readout framework. Through discussion and testing with the IPbus development team, this feature has been integrated into the new version of the IPbus software[6].

2.2 The IPbus framework of the JadePix3 test system

Figure 6 shows how the IPbus is structured in the JadePix3 readout firmware. Four slave devices are developed according to controlling needs. Device 0 is used for system reset logic, reset (global, partial) functions are implemented. Device 1 is used to manage the DAC70004, this digital to analog converter (DAC) will supply test signals for the chip. Device 2 is an ipbus-spi master, this slave device is designed based on an open core spi project[7]. It’s a high-performance and highly customizable IP core. Some import parameters of the pixel sensor, like the bandgap voltage and the PLL settings, are controlled via the SPI interface. The parameters of the chip (DAC, PLL, etc) are stored in a 200 bits register. To configure the chip, we need to write this register through the SPI interface, and then send a enable signal to load the configuration. The maximum variable length of transfer is extended from 128 bits to 256 bits to meet the requirement of the chip design. Device 0 to device 2 are designed based on the IPbus register read/write option. Device 3 is a more complex salve, it not only sets the working mode and parameters of the JadePix3 and monitors the status of the chip, but also writes the configuration of each pixel and readout the detector data via two FIFOs (WFIFO, RFIFO).

Figure 6: The IPbus slaves in firmware.
The JadePix3 software is developed based on µHAL Python API. Based on the encapsulation of IPbus basic communication functions (read/write operation of registers and memory), script commands for high-level operations are realized. Users only need to change the parameters of commands in one Python script to operate the entire test system. According to the function division, we have designed a Python module for each function, such as the DAC70004 module, the on-chip SPI module, the rolling shutter module, the global shutter module, and so on. The layout of IPbus device is specified by Extensible Markup Language (XML) file. The XML node can be a register, memory (FIFO, RAM) or a collection of them.

Figure 7 shows an example of how the DAC70004 is controlled via the test system. The software sets the parameters of DAC by the DAC70004 nodes defined in the XML file. There are three register nodes (two control registers and one status register) defined in the DAC7004 XML file. While the DAC70004 device in firmware received the IPbus commands, the control timing will be generated, then the DAC70004 outputs the desired voltage.

```python
ipbus_link = IPbusLink()
dac70004_dev = Dac70004Device(ipbus_link)
dac70004_dev.soft_reset()
dac70004_dev.soft_clr()
dac70004_dev.w_power_chn(DAC70004_PW_UP, 0xf)
dac70004_dev.w_ana_chn_update_chn(DAC70004_CHN_A, 1.2)
```

![Figure 7](image.png)

**Figure 7**: The diagram of DAC70004 controlling. The python software initial an IPbus link, and a DAC70004 module. All control operations can be done through the methods in the module.

### 2.3 Firmware

The diagram of the working states and transitions is shown in Figure 8. The states used in the firmware are idle (IDLE), configuration mode (CFG), global shutter mode (GS), and rolling shutter mode (RS). The initial and default state is IDLE when the system is configured.

#### 2.3.1 Pixel configuration

For debugging and testing, each pixel has two configuration D-latches, MASK and PULSE. The PULSE D-latch sets the output of the pixel, and the MASK D-latch decides whether the output is masked. After the row and column address select the corresponding pixel unit, it is judged by CON_SEL/P to write the state of CON_DATA into the corresponding D-latch. To configure the registers, all configuration data will be sent to the FIFO in the FPGA firmware from the PC, and after all the configurations are received, the FPGA will start to configure the chip automatically. Figure 9 shows the flow chart of configuring the pixel array parameters. The timing of pixel configuration is shown in Figure 10.
**Figure 8:** Block diagram of the working states and transitions.

**Figure 9:** The flow chart of configuring the pixel array parameters. The pixel settings are generated by a pattern generator in the software.

**Figure 10:** The timing of pixel configuration. The system clock period is 12 ns. T0: Address and data settle time, 24 ns. T1: D-latch settle time, 144 ns. T2: Address and data hold time, 24 ns.

### 2.3.2 Rolling shutter and global shutter

The rolling shutter transmits data to the end of a column through the column-level data line, and reads the signal through the data processing logic at the end. In order to ensure that the peripheral digital logic sees a stable signal within a cycle time window, a buffer structure is designed at the
end of the column data line, and the stable data is sampled and stored through an appropriate clock signal.

To verify the digital logic of the pixel array and save pad sources, multiplexed column output can be captured (HITMAP[15:0]). It’s selected by selected by corresponding column address (0d340 to 0d351). The parameters of this debugging function are setting by the software in the rolling shutter mode. The output of the buffer structure can be controlled through external input (cache_bit), it can produce different hit patterns, which is useful to verify the correctness of the back-end digital logic. The basic unit of the cache structure uses the D flip-flop in the standard digital library, which is triggered by a rising edge and has the function of asynchronous reset. The timing diagram of the rolling shutter is shown in Figure 11.

![Rolling shutter timing diagram]

**Figure 11**: Rolling shutter timing diagram. T0: Row Address settle time, T1: Column bus settle time, T2: Column bus hold time, T3: Row reset asserts time, T4: Row reset de-assert time, T5: Col Address assert time, T6: HITMAP settle time.

The software will set how many frames the pixel array will be scanned, and when the number of scanned frames reaches the set value, the state machine will go to IDLE state. A total of $2^{30} - 1$ rolling shutter frames can be set. Listing 1 shows how we set the parameter and run the RS operation.

```python
from lib.ipbus_link import IPbusLink
from lib.jadepix_device import JadePixDevice
ipbus_link = IPbusLink()
jadepix_dev = JadePixDevice(ipbus_link)

jadepix_dev.rs_config(cache_bit=0x0, hitmap_col_low=340, hitmap_col_high=351, hitmap_en=False, frame_number=400000)
jadepix_dev.reset_rfifo()
jadepix_dev.start_rs()
data_mem = jadepix_dev.read_data(safe_mode=True)
jadepix_dev.write2txt(rs_outfile, data_mem)
```

Listing 1: The example code of how to set the parameters of rolling shutter and read out the data from chip to the data file.

All sensor pixels "expose" simultaneously and readout afterwards at global shutter mode. Figure 12 shows the timing diagram of the global shutter. The exposure time is set by software, and its maximum value can reach $2^{34} - 1$ system clock cycles (12 ns). The software can choose to do Analog Pulse (APLSE) test or Digital Pulse (DPLSE) test during exposure. The analog output can be selected by column address during exposure. After the exposure is over, the firmware will enter the RS mode, and then the whole pixel array will be scanned once.
Figure 12: Global shutter timing diagram. T0: PULSE DELAY, range in $0 \sim 6.12 \mu s$, T1: PULSE WIDTH, range in $24 \text{ ns} \sim 103.079 \text{ s}$, T2: PULSE de-assert, range in $0 \sim 6.12 \mu s$, T3: GSHUTTER de-assert, range in $0 \sim 6.12 \mu s$.

2.4 Data readout

Figure 13 shows the block diagram of the JadePix3. The Jadepix3 design uses zero-compression logic at the end of the pixel array to achieve data compression. The zero-compression logic sends a reset signal after reading the data in the buffer. The row and column information are encoded and stored in the FIFO. The write-enable signal of the FIFO is sent outside the chip for the FPGA to monitor the data flow. In this way, the FPGA can exactly know the amount of data written into each FIFO, and allows to study the optimization readout scheme among the 4 FIFOs. The finite state machine (FSM) selects whether to send data or FIFO state, or K28.5 code according to the INQUIRY signal. The pixel array is divided into four sectors (sector 0 to sector 3), every 48 columns are used as one sector, each sector has one FIFO ($48 \times 16$) for caching data. The four data buffers take turns occupying the serializer channel and the CML serial port to output data under the control of the multiplexer. The data is sent to the serial transmitter after 8b/10b conversion, and finally transmitted to the outside of the chip through LVDS. For the purpose of testing, data can also be output in parallel, which is also the current test system solution.

Figure 13: The block diagram of the zero compression module, data caching module, serializer, and serial transmitter.
Figure 14 shows the structure of the JadePix3 readout firmware, which needs to steer the data flow in the JadePix3. The FIFO_READ_EN and BLK_SELECT[1:0] control signals allow FPGA to control the reading of data from any FIFO. The FIFO monitor module in the firmware can monitor the FIFO status (valid counter, overflow counter) in the chip by these signals. A ring buffer will record the frame number, the row number and the value of their corresponding FIFO counters. In addition, the overflow information of the ring buffer itself will also be recorded. If there is no data in the entire row, there will be no write operation in the ring buffer. The FPGA will start to read the FIFO in the chip according to the valid counter value in the ring buffer.

Figure 14: Block diagram of the JadePix3 data readout firmware. The readout port of FIFO is 8 bits wide. The low 8 bits of 16-bit hit information are read out first, and the high 8 bits are read out later. Each FIFO can store 48 hit information.

Currently, the data is written into the RFIFO by order of sector 0 to sector 3. Four types of data will be encoded and stored: 1. Frame Head, which contains the status information of four FIFOs on-chip and overflow information of ring buffer; 2. Data frame, overflow count and on-chip FIFO data; 3. Frame Tail, the frame number; 4. Error, overflow count of the RFIFO. The RFIFO has three XML nodes, RFIFO_DATA, RFIFO_LEN and RVALID_LEN. RFIFO_DATA is used to store data, RFIFO_LEN stores the number of valid data in the FIFO, and RVALID_LEN stores the number of how many data is read. When the state is RS or GS, the software will continuously query the value of the RFIFO_LEN node, and read out the same amount of data from the RFIFO. There are three data buffer structures in the entire data link, the first is the internal FIFO of the chip, the second is the Ring buffer of the FPGA, and the third is the IPbus RFIFO. Their overflow status is very important for monitoring the system’s status, so the overflow counts of the three buffers will be put into the data stream.
3 System tests in the laboratory

The test system has been deployed in the laboratories at the Institute of High Energy Physics (IHEP) and Central China Normal University (CCNU). The test setups are shown in Figure 15. Three

![test setups at CCNU and IHEP](image)

**Figure 15:** The photograph of test setups at CCNU and IHEP. (a) Test setup for the pulse and cosmic signals at CCNU. (b) Laser test setup at IHEP.

test input signals include pulse, cosmic and laser have been used to verify the DAQ’s stability and performance.

### 3.1 Pulse test

The pulse test is carried out according to the following steps: 1. Set the DAC70004 to adjust the high and low voltage of the pulse (PULSE_HI, PULSE_LO); 2. Through the SPI interface, configure a 200-bit width register inside the chip to control the on-chip DAC and change the bandgap reference source voltage (BANDGAP_ALT); 3. Configure the pixel array register (PULSE, MASK) to make a test pattern; 4. In the global shutter mode, observe the analog output signal (AOUT) or the array output signal (HITMAP). 5. Archive data as ROOT/TXT file, and check whether the result is the same as expected.

Usually, to verify that the entire pixel is working, we randomly select individual pixels and continuous pixels and block region in each of the four sectors. Figure 16 shows the pulse test results. We can verify whether the module in the pixel works through this test, including the analog and digital parts of the pixel, the on-chip DAC, the pixel configuration register, and the SPI interface. In addition, some related functions of the firmware and software have also been verified, including chip control, pixel configuration, global shutter mode and small-scale data acquisition. For the special test pattern, the “CEPC”, since the period of the test pulse is different from the scan period, and the two signals are not synchronized, the "CEPC" image should be incomplete in most cases, and the entire image will be truncated into two adjacent frames. The test results are in line with expectations.

The stability of the readout system is verified under a pulse test. After setting the readout system and chip parameters, we injected pulses of various frequencies into the chip. Test Pattern is four columns(4 × 512 pixels) of pixel array (one column for each sector). By analyzing the obtained
Figure 16: The pulse test conditions: PULSE_HI is 1.7 V, PULSE_LO is 1.2 V; BANDGAP_ALT is 1.2 V. (a) Global shutter readout mode. The analog output is enabled, the analog waveform can be observed at AOUT with a APULSE input (250 mV). (b) Rolling shutter mode, frame_num is 400000, input pulse period is 200 µs. This figure is a plot of one frame data with special test pattern, the "CEPC".

data files, verifying whether there are data loss and errors, and the overflow situation seen in various parts, it proves that the system has very reliable stability. In order to verify the specific value of the system speed bottleneck, we tested the overflow flag of the critical data buffer stage under different input conditions. The overflow of the on-chip FIFO is measured by changing the test pattern. The overflow of the ring buffer is measured by changing the frequency of the input pulse. Figure 17 shows some of the test results.

Figure 17: Hit number per each event = 2048, frame number = 400000. (a) The status of data accumulation and system overflow status. Event interval = 110 µs. The data throughput is $595.8 \text{Mbps} \times 39.3s$, no overflow is found. (b) The data count in the sectors at different pulse periods.
3.2 Cosmic test

We can verify the function of the chip and the readout system by the cosmic ray test. Tests were carried out at two angles (the chip is placed vertically or horizontally on the ground plane, respectively) to observe the track, shape and frequency of the cosmic rays. The sensor data is read out in rolling shutter mode. The frame number is set to 400000, so the scanning time is \( 400000 \times 98.3 \mu s \approx 40 \) s. The mean number of the event is 4.5, the cosmic rate is \( 4.5 \div (40 \times 10.4 \times 6.1) \approx 0.177 \, \text{cm}^{-2} \, \text{s}^{-1} \). Figure 18 shows the plots of the cosmic ray signal captured.

\[ \begin{array}{ll}
\text{Figure 18:} & \text{The cosmic ray test conditions: BANDGAP_ALT=1.2 V, frame_num=400000. (a) The chip is parallel to the ground. This figure is one of the five captured signals. (b) The chip is perpendicular to the ground. This figure is one of the four captured signals.} \\
\end{array} \]

3.3 Laser beam test

A laser beam test system is built for measuring the position residual and single point resolution of the JadePix3. The laser test system consisted of a laser generator, an optical fiber, a collimator, a focusing lens, and a 3D linear motion platform[8]. The laser intensity and the distance from the laser emitting point to the chip need to be adjusted to allow one hit at a time. Then the laser position is moved to perform one-dimensional scanning of the chip. Figure 19 shows the result of a 1-D scan of laser position.

3.4 Rolling shutter speed verification

The integration time (the speed of RS) is a very important design parameter for the JadePix3. The timing of the RS is precisely controlled by FPGA, and integration time should be \( (512 \times 16 + 1) \times 12 \mu s = 98.316 \mu s \). We use two pulse tests to calculate the RS speed from the data. The period of the first test pulse signal is 10 s, and the period of the second test pulse signal is 500 \( \mu s \). By calculating the number of frames between two adjacent pulses, the period of the RS can be obtained. The test results are shown in Figure 20, the integration time is in line with expectations.
Figure 19: 1-D scan of laser position. The laser wavelength is 1064 nm, the scan direction is from pixel0 to pixel 1, and the scan step is 1 µm.

Figure 20: The pulse test conditions: BANDGAP_ALT=1.2 V, frame_num=400000. (a) Pulse period=10 s, RS period=98.315 426 µs. (b) Pulse period = 500 µs. RS period=98.315 360 µs

4 Conclusion

The JadePix3 test system is developed based on the IPbus framework. This system is reliable and flexible for chip testing. The system has tested almost all the chip modules, and the stability and portability of the system have also been verified under different test conditions. The jumbo frame feature has been integrated into the IPbus suite for meeting the readout speed requirement of the experiment. The speed bottleneck of the system has also been tested and verified. This system has been successfully applied to the testing of the JadePix3 and it has great potential to be applied to similar readout architecture pixel chips.

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