Robust and Resource-Efficient Quantum Circuit Approximation

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ABSTRACT

We present QEst, a procedure to systematically generate approximations for quantum circuits to reduce their CNOT gate count. Our approach employs circuit partitioning for scalability with procedures to 1) reduce circuit length using approximate synthesis, 2) improve fidelity by running circuits that represent key samples in the approximation space, and 3) reason about approximation upper bound. Our evaluation results indicate that our approach of “dissimilar” approximations provides close fidelity to the original circuit. Overall, the results indicate that QEst can reduce CNOT gate count by 30-80% on ideal systems and decrease the impact of noise on existing and near-future quantum systems.

1 INTRODUCTION AND MOTIVATION

We begin by providing a brief relevant background of quantum computing, followed by motivation for QEst, and summarize the approach and contributions of QEst.

1.1 Quantum Computing: A Brief Background

The unit of information in quantum computing is the qubit. This is a two-level abstraction, whose state is represented by \( |\psi\rangle = \alpha |0\rangle + \beta |1\rangle \), which is a superposition of the \( |0\rangle \) and \( |1\rangle \) states. When this qubit is measured, its superposition collapses and it can be measured in state \( |0\rangle \) with probability \( \|\alpha\|^2 \) and in state \( |1\rangle \) with probability \( \|\beta\|^2 \), such that \( \|\alpha\|^2 + \|\beta\|^2 = 1 \). Similarly, an \( n \)-qubit entangled quantum system can be represented as a superposition of \( 2^n \) states: \( |\psi\rangle = \sum_{k=0}^{2^n-1} \alpha_k |k\rangle \), such that \( \sum_{k=0}^{2^n-1} \|\alpha_k\|^2 = 1 \).

Under Deutsch’s computational model, a quantum program can be represented as a circuit of operations [9]. A quantum system can be put into a desired superposition state using quantum gates or operations. For example, a one-qubit NOT operation can be used to rotate the state of qubit \( (|0\rangle \rightarrow |1\rangle \) or vice versa), while a two-qubit controlled-NOT or CNOT operation can be used to entangle two qubits and apply a NOT gate to the “target” qubit if the “control” qubit is in the \( |1\rangle \) state. When these operations are applied in succession to one another, they form a “quantum circuit” that represents and executes the corresponding “quantum algorithm.” Note that all quantum algorithms can be represented as a sequence of one-qubit rotation gates and two-qubit CNOT gates.

1.2 Motivation for QEst

Existing quantum systems and projected near-term future quantum systems suffer from a pack of different types of errors [20, 32]. These include state-preparation and measurement (SPAM) errors and qubit state decoherence errors. These near-term intermediate-scale quantum (NISQ) devices also suffer from errors related to applying one-qubit and two-qubit gates to a qubit. These errors get compounded over the course of a quantum circuit, as a circuit runs many quantum operations. The two-qubit (CNOT) operation error rate (1-3%) tends to be an order of magnitude above one-qubit operation error rate.

This makes it difficult to run long quantum circuits with many CNOT gates on near-term quantum computers as the CNOT gates have a high application error as well as take longer to apply, causing decoherence errors. Previous works have proposed several techniques that focus on circuit compilation and mapping to hardware in a manner that reduces the CNOT gate count of the circuit as well as reduces the impact of the errors. These include reducing gate count by collapsing adjacent gates, deleting gate operations using commutativity and unitary laws, reducing the number of CNOT and SWAP operations (implemented using three CNOT gates) by performing layout-aware mapping of the quantum circuit to the hardware, and performing noise-aware mapping to ensure that more noisy qubits and operations are avoided as much as possible [21, 26, 27, 35, 37, 39, 42, 44, 45]. Qiskit [25], IBMQ’s python-based quantum compiling package has these state-of-the-art compilation techniques implemented as optimization passes, whereby...
the optimizations are applied one after another. While these compilation and mapping passes are effective in some cases, they are not able to reduce the gate count to a degree that is able to reduce the noise sufficiently.

As an instance, Fig. 1(a) and (b) show the output of the TFIM (Transverse Field Ising Model) and Heisenberg quantum algorithms, respectively, in the ideal (ground truth) scenario vs. the case in which they are on run on the real IBMQ Manila quantum computer [6]. TFIM outputs the time evolution of the average magnetization (energy) of a four-spin physical system with only the $z$ Hamiltonian interaction component, while Heisenberg outputs the time evolution of a four-spin system with $x$, $y$, $z$ Hamiltonian interaction components [3]. Even though the IBMQ Manila computer is a relatively low-error NISQ device and all of the Qiskit compiler optimizations are applied when running the circuit on the computer, the output is far from the expected ideal output. The error is large enough for the output to be not provide meaningful insights. For example, with TFIM, the output does not remain consistent across the timesteps (even though it should according to the ground truth output), not does it have the same magnetization amplitude as the ground truth.

### 1.3 Approach and Contributions of QEST

Overall, the compilation and mapping passes employed by the state-of-the-art approaches cannot reduce the output error sufficiently. Therefore in this work, we present QEst, a technique that focuses on delivering a large reduction in CNOT gate count to reduce the effect of noise.

QEst is built on are a few key observations and opportunities. A quantum circuit can be mathematically represented as a unitary matrix. A unitary matrix can have multiple mathematically close “approximations”. These approximated unitaries can represent the original circuit’s functionality. QEst leverages this property to demonstrate that it is possible to use approximations to our advantage to improve the output fidelity of complex quantum programs on erroneous NISQ devices.

While the idea of approximating circuits appears promising, it poses multiple challenges not solved by prior works before it can be realized in practice. First, approximating a complex quantum circuit requires calculating approximate circuits of a large unitary matrix. Unfortunately, the calculation of how mathematically approximate a circuit is to its original circuit is computationally infeasible for quantum programs beyond four-five qubits. QEst employs circuit partitioning to make the problem tractable: QEst applies approximations on small-size partitions (blocks) and then, combines these approximate blocks to produce an approximate full circuit for the original circuit. While this is the only way to produce approximations for large circuits, it poses two primary challenges.

1) First, when we combine multiple approximate circuit blocks to produce a full approximate circuit, there is no existing knowledge or mechanism to understand how these approximations interact and affect the overall quality of the full approximate circuit. QEst overcomes this hurdle by providing a theoretical proof to guarantee that the quality of the approximation of the full circuit can be bounded by controlling the quality of the approximations of blocks. This allows QEst to combine the approximate blocks and guarantee that the overall approximation is of an acceptable quality.

2) The second challenge is that the quality of a circuit approximation is expressed as the difference between the unitary matrix of the original circuit and unitary matrix generated after approximation; this measure of approximation does not have strict ordering or direct analytical relationship with the output fidelity. Thus, different “similar” approximate circuits can potentially produce different program outputs (and hence, output fidelities). QEst overcomes this challenge by devising a novel apriori selection and combination strategy to indirectly control the overall output fidelity by choosing a set of “dissimilar” approximate circuits that have low CNOT gate counts. QEst’s method is effective in achieving higher output fidelity by controlling the approximations for individual circuits.

### The main contributions of this work are as following:

- QEst leverages the approach of circuit synthesis, a technique to generate a mathematically equivalent circuit for a given quantum circuit [8, 13, 14, 23, 34], and approximates it to generate low-CNOT-gate-count circuits that deliver a large reduction in noise.
- QEst defines an apriori approximation selection criterion that enables it to select approximations with fewer CNOT gates in a manner that the effect of the approximations does not manifest in the output of the circuit.
- We provide a theoretical proof to bound the distance of the approximations from the original circuit, which enables QEst to partition the circuit for synthesis and scale up.
- QEst’s evaluation demonstrates a 30-80% reduction in the CNOT gate count of circuit while ensuring that the output does not deviate from the output of the original circuit on an ideal quantum system. On a noisy system, QEst reduces the output error by up 30% points.
- Using real materials simulation algorithms like TFIM and Heisenberg, QEst demonstrates its ability to track algorithm-specific output even on existing quantum computers due to careful selection of low-error approximations.

### 2 QEST-RELEVANT TERMS AND DEFINITIONS

Before we present our technique in Sec. 3, below we introduce some terms and definitions that are used in this paper.

A quantum algorithm (or transformation) is a procedure (or computation) that takes a system from an initial state into a final state, as prescribed by its developer. There are multiple formalism spaces in which we can reason about quantum program behavior: 1) process metrics [18], and 2) domain-specific or standard output metrics [5, 11, 30].

First, at the fundamental level, each program is represented by a unitary matrix $U$. For a $n$-qubit system in initial state $|\psi\rangle$, the effect of the program is computed as $U |\psi\rangle$, where $U$ is a $2^n \times 2^n$ unitary matrix. In general, synthesis algorithms use norms to assess the solution quality, and their goal is to minimize $\|U - U'\|$, where $U$ is the unitary that describes the transformation and $U'$ is the computed solution. This norm is referred to as process distance. Intuitively, process distance metrics compare how alike are two
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Figure 2: QEst’s methodology of partitioning the circuit into smaller blocks, generating multiple approximate solutions for each block, and selecting “dissimilar” circuits from the block search space while minimizing the CNOT gate count.

3 DESIGN AND IMPLEMENTATION OF QEST

In this section, we provide an in-depth description of how QEst addresses the problem of reducing the number of CNOT gates in a circuit. We begin by providing an overview of the end-to-end design of QEst.

3.1 Overview of QEst Design

As shown in Fig. 2, QEst first partitions the large circuit into multiple smaller circuits called “blocks” to ensure a scalable solution. Next, it generates approximate circuit solutions with low CNOT gate counts for individual blocks using approximate synthesis. Approximate synthesis is a procedure whereby an approximate circuit can be produced by reducing the process distance between the unitary matrices of the approximate and original circuits. Once the synthesized blocks are generated for each block, they are combined to form the approximate full circuit, which now has a lower CNOT gate count than the original circuit.

However, because the circuit is approximate, the output of the circuit can be different from the original circuit. To overcome this issue, QEst’s makes use of its key insight: multiple different approximate full circuits can be generated because the block instances can be combined in different ways. QEst uses a dual annealing engine to search the block instance search space in a manner that it selects multiple low-CNOT-gate-count full circuit approximations that are mathematically “dissimilar” to each other. This ensures that when the outputs of the approximations are averaged, it produces the same output as the original full circuit, but by using circuits that have fewer CNOT gates. We also provide a theoretical proof that bounds the full circuit’s approximation distance, without the need to calculate it directly as it is computationally infeasible, to avoid coarse approximations.

Next, we describe each of these steps in detail, starting with a description of circuit synthesis.

3.2 Overview and Challenges of Circuit Synthesis

Quantum circuit synthesis is the technique used to find a circuit for a quantum algorithm that is mathematically close (referred to in this paper as “exact” synthesis) to the original algorithm circuit. Recall that an n-qubit quantum algorithm can be represented as an N × N unitary matrix, where N = 2^n. This unitary matrix can be calculated by taking a product of all the operations run by a
A solution to the problem of scaling the circuit synthesis approach is to partition the circuit into blocks of smaller sizes [1]. Fig. 3 shows how this can be achieved for an example circuit of four qubits. Assuming that we can computationally synthesize circuits that are up to three qubits in size, if we partition the four-qubit circuit into two blocks of three-qubits, we can synthesize the two blocks separately to generate circuits equivalent to their corresponding unitaries: $U_1$ and $U_2$. The blocks are formed such that there are no connections in terms of two-qubit CNOT gates between the two blocks. Otherwise, they may be entangled and cannot be synthesized separately.

In terms of our example circuit, the unitary $U_1$ is synthesized such that $1 - \frac{||\text{Tr}(U_1^2)||}{N_1} < \epsilon_1$ and the matrix $U_2$ is synthesized such that $1 - \frac{||\text{Tr}(U_2^2)||}{N_2} < \epsilon_2$. When the synthesized circuits are obtained for $U_1$ and $U_2$, they are put together to form the full synthesized circuit. Note that this approach is scalable because we limit the block size to what is computationally possible. Synthesizing in this manner does not require generating the target unitary for the full circuit, nor does it require calculating the process distance for the entire circuit’s unitary. However, this approach also has several challenges, which we discuss in the following section.

### 3.4 Challenges with Exact Synthesis of Blocks

An exact solution that minimizes the process distance might not necessarily minimize: 1) the CNOT gate count, and 2) the output distance: how far the output of the synthesized circuit is from the output of the original circuit. As for 1), exact synthesis solutions provide a small reduction in the number of CNOT gates due to the strict process distance threshold requirements (more layers have to be added to the circuit during synthesis to allow for more degrees of freedom).

With regard to 2), the output distance cannot be used as a metric of mathematical exactness during synthesis because the state of a quantum system can only be represented using its unitary. Moreover, when the circuit is partitioned, each block cannot be optimized using an output distance metric because individual blocks have no output of their own. Only the full circuit has an output and it can only be measured after execution. Thus, while the process distance is required for synthesis, the output distance comes into play when the output of the algorithm needs to be interpreted.

However, circuits with similar process distances can have different output distances and CNOT gate counts. Fig. 4 demonstrates the relationship between the number of CNOT gates and the TVD for several exactly synthesized solutions of a four-qubit Variational Quantum Eigensolver (VQE) circuit. All solutions
have a similar process distance of less than $10^{-5}$ (exact solution threshold) and yet have TVDs in a large range. The solution with the minimum number of CNOT gates has one of the highest TVDs, while the solution with only 10% more CNOT gates than the minimum (1.1 factor) has a lower TVD. This small-scale example shows that it is not always advisable to select the exact solution with the fewest number of CNOT gates. Thus, QEst breaks away from the notion of having an exact synthesized solution by designing an approximate synthesis approach.

### 3.5 STEP 2: Generate Approximate Circuits for Blocks

QEst employs an approximate synthesis procedure that generates multiple low-CNOT-gate-count circuit approximations in a manner that minimizes the output distance between the synthesized circuits and the original circuit of a block.

The key to achieving this reduction is realizing that different types of circuits can be synthesized such that they have process distance below a certain threshold. Recall that synthesis is performed using numerical optimization building layer-by-layer. The qubits that these layers are placed on and the rotation angles that are assigned to them during the process distance minimization procedure affects the final synthesized circuit that is produced. Multiple different approximate circuits can be produced by varying these factors.

To achieve this, QEst modifies the Leap compiler [36] to return the best $M$ circuits with the lowest process distance at each layer of the compiler tree. The compiler constructs a circuit tree one layer at a time as shown in Fig. 5. Each layer consists of at least one CNOT gate between two qubits followed by two rotation gates on both the qubits. It attempts this layer on all allowed two-qubit combinations and optimizes the rotation angles to minimize the unitary process distance. As more layers are added, the tree expands due to the increased number of layer permutations. Every few layers, it picks the branch with the least process distance and starts reconstructing the tree from there to reduce the number of optimization evaluations. QEst uses the compiler to generate multiple approximations at each layer of the tree (a tree layer roughly corresponds to one CNOT gate). This enables the generation of approximate circuits of different qualities in terms of process distances for each block at different CNOT gate counts. All approximate solutions are generated until the tree exceeds the CNOT gate count of the original circuit. As more layers are constructed and the tree becomes deeper, the process distance decreases. However, because we would like to have multiple solutions for a block, including the ones with higher CNOT gate counts than the minimum CNOT gate count solution, we collect all solutions of different CNOT gate counts.

![Figure 5: Leap compiler builds the circuit layer-by-layer.](image)

### 3.6 STEP 3: Putting Together Approximate Blocks

How can these low-CNOT-gate-count approximations be used to reduce the output distance? Fig. 6 demonstrates a visual example of how selecting multiple synthesized circuits can help ensure that the output distance is reduced. The figure is read from left to right, with the first circle showing when one approximate circuit sample is used and the last circle showing when six samples are used. The red cross shows the output of the original circuit in Hilbert space, the boundary circle around it demarcates the boundary of the process distance threshold used for approximate synthesis (this threshold is larger than used with exact synthesis so as to generate low-CNOT-gate-count solutions). The blue squares show the output samples of the approximate synthesized circuit and the dark blue diamond shows the average of the samples. We make two points:

1) If only the circuit with the fewest number of CNOT gates is selected, it can result in a high output distance as shown in the first circle. While the circuit with the lowest CNOT gate count might also coincidentally have a low output distance for some algorithms, this cannot be established analytically as it assumes knowing the ground truth output. Instead, averaging over $M$ low-CNOT-gate-count circuits can help us regulate and control the output distance with more robustness than simply choosing one circuit. The trade-off here is between the CNOT gate count and the output distance. If multiple circuits are not selected, we do not have a way to control and reduce the output error. On the other hand, if the CNOT gate count is high, it defeats the purpose of synthesis.

2) It is also not sound to just have many random approximations. If the approximations are mathematically similar (e.g., if the six samples in the third circle were in the same region of the circle), their output cannot average out to reduce the output distance. Thus, QEst must ensure that the approximations are “dissimilar,” while also having a low CNOT count.

QEst achieves this balance by using a dual-annealing-based minimization algorithm [33] shown in Algorithm 1 to minimize an objective function that places equal weight on CNOT-gate count and the dissimilarity of the approximations: $\min f = \frac{1}{2} \times \text{CNOT Count} + \frac{1}{2} \times \text{Dissimilarity}$.

The CNOT count in this objective function is simply the normalized CNOT gate count of the approximation compared to the original circuit. The approximation dissimilarity is calculated as the fraction of already selected circuit samples with similarity to the new sample. Consider two approximate circuit samples, $S_1$ and $S_2$. If the process distance between the two samples $(\langle S_1, S_2 \rangle_{HS})$ is less
than the maximum of their process distances to the original circuit \((\max\{\langle S_1, O \rangle_{HS}, \langle O, S_2 \rangle_{HS}\})\), then the two samples are considered similar: \(\langle S_1, S_2 \rangle_{HS} \leq \max\{\langle S_1, O \rangle_{HS}, \langle O, S_2 \rangle_{HS}\}\). Intuitively, in the visualization shown in Fig. 6, this means that both samples are in the same region of the circle. If the process distance between the two is greater than the maximum of their process distances to the original circuit, then the two circuits are on the opposite side of the circuit; thus, their output can be averaged out. The first sample has an approximation dissimilarity of zero (since there are no already selected circuits), and the objective function will select the approximate circuit with the lowest CNOT gate count. As more samples are selected, the approximation dissimilarity gains more significance as it becomes increasingly difficult to find dissimilar approximations. However, the equal weight on CNOT count ensures that approximations that have too many CNOTs are not selected.

While this objective function works well for non-partitioned circuits, it requires a tweak to accommodate large partitioned circuits. Calculating if two full circuit approximations (constructed by putting together block approximations) are similar should not require the computationally infeasible use of the full circuit unitaries. Instead, QEst uses the metric “fraction of all circuit blocks that are similar” in the objective function as it is a scalable alternative that works well in practice. As an instance, for two approximations of a full circuit consisting of ten blocks, if three of the blocks are mathematically similar, the two approximations receive a similarity score of 0.3. Next, we discuss a major challenge when approximating large partitioned circuits.

### 3.7 A Challenge of Approximating Full Circuits

While for individual blocks it can be ensured that the approximations are not too coarse by eliminating ones with a high output distance (Lines 6-7 in Algorithm 1), a major challenge of partitioned synthesis is to ensure that when the approximate blocks are put back together, the process distance of the full circuit approximation is not violated. Blocks cannot be combined without the knowledge of how their process distances accumulate. For example, the process distance may compound multiplicatively when the blocks are combined to form the full circuit. Without having a theoretical bound on the process distance of the full circuit, the process distance thresholds of its blocks may have to be kept unnecessarily small to be on the safe side. This means that the synthesized blocks likely end up being longer than they need to be as more layers are typically required during the numerical optimization process if the distance threshold is very small. Overcoming this problem can help us synthesize shorter circuits with fewer CNOT operations. To this end, next we provide a theoretical proof to bound the full circuit process distance based on the process distances of its blocks without the need to directly calculate the process distance of the full circuit. This will help us ensure that the full circuit approximations that are too coarse can be eliminated during the dual annealing minimization procedure.

### 3.8 Theoretical Upper Bound on Process Distance

We prove the theoretical upper bound for a circuit partitioned into two blocks without any loss of generality (e.g., the one shown in Fig. 3), and it can then be extended to a circuit partitioned into \(K\) blocks.

We want the process distance of the unitary \(U\) of the full circuit to be bounded without performing synthesis on the full circuit due to the lack of scalability: \(\sqrt{1 - \frac{\|\text{Tr}(U (U^\dagger U'))\|^2}{N^2}} < \epsilon\). \(U\) is an \(N \times N\) matrix, where \(N = 2^n\), where \(n\) is the number of qubits in the full circuit. We choose the \(\sqrt{1 - \frac{\|\text{Tr}(U (U^\dagger U'))\|^2}{N^2}}\) metric for process distance as it is a reasonable metric to measure unitary equivalence, it is computationally efficient, and it gives us the ability to prove a bound on it without calculating it directly. The \(\epsilon\) bound needs to be derived based on the process distances of its circuit blocks. Recall that the partitioned blocks are small enough to be efficiently synthesizable and therefore, have known process distances. The example circuit has two blocks and these blocks have the below two process distance bounds by construction (synthesis is performed in a manner that ensures that these bounds are met).

\[
\sqrt{1 - \frac{\|\text{Tr}(U_1 (U_1'))\|^2}{N_1^2}} \leq \epsilon_1, \quad \sqrt{1 - \frac{\|\text{Tr}(U_2 (U_2'))\|^2}{N_2^2}} \leq \epsilon_2
\]

Here, \(N_1\) and \(N_2\) are the dimensions of \(U_1\) and \(U_2\), respectively. For the example circuit, we have \(U = (I \otimes U_2)(U_1 \otimes I) = U_2 U_1\). The notation \(U_{11}\) refers to the unitary \((U_1 \otimes I)\), representing the Kronecker product of the \(U_1\) operation with the identity operation on the remaining qubits (no operation can be represented as the identity operation). Similarly, \(U_{22}\) refers to the unitary \((I \otimes U_2)\). The post-synthesis approximations of these unitaries can be represented as \(U' = (I \otimes U'_2)(U'_1 \otimes I) = U'_2 U'_1\). Also, \(N = N_1 \times N_2 = N_2 \times N_1\).

As a first step, we prove the process distance bound when a unitary representing a partitioned block is extended to the remaining qubits in the full circuit, i.e., we determine the process distance of \(U_1 \otimes I\) matrix given the process distance of the \(U_1\) matrix. We begin
by rearranging the terms in Eq. 1 to isolate for \( \| \text{Tr} (U_1^t U_1') \|_F \), as is shown below.

\[
\sqrt{1 - \frac{\| \text{Tr} (U_1^t U_1') \|^2}{N_1^t}} \leq \epsilon_1 \Rightarrow \frac{\| \text{Tr} (U_1^t U_1') \|^2}{N_1^t} \geq 1 - \epsilon_1^2
\]

\[ (2) \]

Next, we show how \( \text{Tr} (U_{1H}^t U_{1H}') \) is related to \( \text{Tr} (U_1^t U_1') \):

\[
\text{Tr} (U_{1H}^t U_{1H}') = \text{Tr} [(U_1^t \otimes I)(U_1' \otimes I)] = \text{Tr} [(U_1^t \otimes I')(U_1' \otimes I)]
\]

\[ = \text{Tr} [(U_1^t \otimes I)(U_1' \otimes I)] = \text{Tr} (U_1^t U_1' \otimes I) = \text{Tr} (U_1^t U_1') N_1
\]

Substituting Eq. 2 into Eq. 3, we get that \( \| \text{Tr} (U_1^t U_1') \| \geq N_1 \sqrt{1 - \epsilon_1^2} \), as shown below.

\[
\| \text{Tr} (U_1^t U_1') \| = \| \text{Tr} ((U_1^t U_1') N_1) \| = \| \text{Tr} (U_1^t U_1') \| N_1
\]

\[ \geq N_1 \sqrt{1 - \epsilon_1^2} N_1 = N_1 N_1 \sqrt{1 - \epsilon_1} = N_1 \sqrt{1 - \epsilon_1}
\]

\[ (4) \]

If we rearrange the terms in Eq. 4 (similar to the rearranging in Eq. 2, but in reverse order), we get \( \sqrt{1 - \frac{\| \text{Tr} (U_1^t U_1') \|^2}{N_1^t}} \leq \epsilon_1 \). Thus, the process distance of a block unitary that does not span the full size (number of qubits) of a circuit remains bounded by the same threshold when the unitary is extended to the size of the circuit. Therefore, using a similar procedure, we can also show that for the second block, \( U_2 \), \( \sqrt{1 - \frac{\| \text{Tr} (U_2^t U_2') \|^2}{N_2^t}} \leq \epsilon_2 \).

We now have the tools to bound the process distance of the full circuit. Recall that the process distance for the full circuit is \( \sqrt{1 - \frac{\| \text{Tr} (U^t U') \|^2}{N^t}} \). Substituting \( U = U_2 U_1 \), we obtain the following:

\[
\sqrt{1 - \frac{\| \text{Tr} (U^t U') \|^2}{N^t}} = \sqrt{1 - \frac{\| \text{Tr} [U_2 U_1 (U_1^t U_1') N_1] \|^2}{N^t}}
\]

\[ \leq \sqrt{1 - \frac{\| \text{Tr} (U_1^t U_1') \|^2}{N_1^t}} + \sqrt{1 - \frac{\| \text{Tr} (U_2^t U_2') \|^2}{N_2^t}} \leq \epsilon_1 + \epsilon_2
\]

\[ (6) \]

Combining Eq. 5 and Eq. 6, we get \( \sqrt{1 - \frac{\| \text{Tr} (U^t U') \|^2}{N^t}} \leq \epsilon_1 + \epsilon_2 \). This proof can be extended to circuits partitioned into \( K \) blocks by providing the proof for two blocks at a time, combining the two into a single unitary and providing the proof again for the two unitaries (combined unitary and the third unitary), and so on and so forth, iteratively. Therefore, for a circuit partitioned into \( K \) blocks, we have that \( \sqrt{1 - \frac{\| \text{Tr} (U^t U') \|^2}{N^t}} \leq \sum_{k=1}^{k=K} \epsilon_k \). The process distance of the full circuit is theoretically upper bounded by the sum of the process distances of all of its partitioned blocks.

While the relationship between the derived process distance upper bound and the actual process distance cannot be directly/theoretically proven as it algorithm specific and varies depending on how the algorithm circuit is constructed and partitioned, we demonstrate this relationship using real algorithm examples. Fig. 7 shows the relationship between the process distance upper bound and the actual process distance for different algorithms. The results indicate that the derived upper bound is respected across all samples and a relatively tight bound is obtained for different algorithms and process distance values. Therefore, the upper bound enables us to confidently bound the process distance of the full circuit (without the need to calculate it directly) simply by ensuring that its partitioned blocks are combined by the dual annealing engine in a manner that the sum of their process distances is within an acceptable threshold.

Putting it together. In summary, QEst enables reduction in the CNOT gate count by partitioning the circuit into smaller blocks and generating multiple approximate circuits for the blocks. It then puts back together the block approximations in a manner that reduces the CNOT gate count as well as generates dissimilar approximations to reduce the output distance using its dual annealing engine. It is aided by the theoretical upper bound to eliminate coarse approximations in a scalable manner. In the next section, we evaluate the effectiveness of QEst for different algorithms after providing details about the experimental setup and methodology.

4 EVALUATION

4.1 Experimental Setup and Methodology

Comparative Techniques. We compare against the original circuit as a baseline circuit (referred to as the Baseline) in terms of the CNOT gate count, ground truth output, as well as the error observed in a noisy environment. We also compare to the circuit generated when all the Qiskit compiler optimizations are applied to this Baseline circuit. These compiler optimizations are simply
Table 1: Algorithms and benchmarks used to evaluate QEst.

| Algorithm | Description |
|-----------|-------------|
| Adder     | Quantum adder circuit [7] |
| Heisenberg| Time-independent Heisenberg Hamiltonian [3] |
| HLF       | Hidden linear function [4] |
| QFT       | Quantum Fourier transform [28] |
| QAOA      | Quantum alternating operator ansatz [10] |
| Multiplier| Quantum multiplier circuit [12] |
| TFIM      | Transverse field Ising model [3] |
| VQE       | Variational quantum eigensolver [24] |
| XY        | XY quantum Heisenberg model [3] |

referred to as Qiskit. When these compiler passes are applied to the approximate circuits produced by QEst, the results generated by the produced circuits are referred to as QEst + Qiskit.

Experimental Setup. The partitioning, approximate synthesis, and dual annealing components of QEst are run on our local computer cluster consisting of 2.4 GHz Intel E5-2680 v4 CPUs. A maximum block size of four qubits is used to partition the circuits using the scan partitioner available as part of the open-source BQ SKit package [1]. It forms partitions by traversing the circuit left to right and creating four-qubit blocks. Note that some blocks may be of a smaller size if need be. A maximum block size of four qubits is used as it synthesizes efficiently and yields good results. When an algorithm has multiple blocks, the approximate synthesis step is run on different blocks in parallel on up to ten compute nodes. Leap compiler [36], which is also a part of the BQSKit package, is modified and used for synthesis as described in Sec. 3. The Python-based SciPy package is used to run the dual annealing engine [15]. The process distance threshold to eliminate coarse approximations in the annealing engine is set proportional to the number of blocks in the circuit and up to 16 approximations are generated for each algorithm. A balanced weight of 0.5 is used for CNOT gate count and approximation dissimilarity in the objective function that the dual annealing engine minimizes. The ground truth results are obtained by running the Baseline circuit in an ideal quantum simulation environment using the Qiskit unitary simulator [25], which is part of the Aer package. We perform noisy simulations on circuits up to 16 qubits (it was not possible to run noisy simulations on larger circuits) using the IBMQ QASM simulator available via the IBM quantum experience cloud. A Pauli noise model is used for all the qubits with noise levels of 1%, 0.5%, and 0.1% to simulate how QEst will perform for future NISQ computers as the noise level decreases. We run circuits up to five qubits on the IBMQ Manila quantum computer in order to demonstrate how the technique performs on existing quantum computers. We use 8192 experimental trials (maximum allowed) per experiment. Each circuit run on a quantum computer takes 10-12 seconds for all trials.

Algorithms and Benchmarks. We use the algorithms and benchmarks listed in Table 1 to evaluate QEst. Adder and Multiplier are standard quantum arithmetic circuits, while QAOA and VQE are quantum variational algorithms. Heisenberg, TFIM, and XY are time-evolving Hamiltonian algorithms for material simulations.

The Heisenberg model has non-zero strength for the coupling interaction between nearest neighbor spins for all three axes (x, y, z), TFIM does for z, and XY does for x and y. We evaluate circuits of size 4-32 qubits.

Evaluation Metrics. In terms of output distance, we use the Total Variation Distance (TVD) and the Jensen-Shannon Divergence (JSD) as defined in Sec. 2. These are general metrics that are typically used to define the output distance across all algorithms. To calculate the output distance from the Baseline for QEst, the output probability distributions of all of its approximate circuits are averaged to generate one probability distribution. In addition to these metrics, we also study algorithm-specific output distances as necessary. For example, for TFIM and Heisenberg algorithms, we study the differences in the magnetization at different time steps.

4.2 Results and Analysis

The QEst reduces the CNOT gate count over all algorithms compared to the Baseline circuits as well as the Qiskit optimizations applied on the Baseline circuits. The number next to the algorithm name indicates the number of qubits.

Figure 8: QEst reduces the CNOT gate count across all algorithms compared to the Baseline circuits as well as the Qiskit optimizations applied on the Baseline circuits. The number next to the algorithm name indicates the number of qubits.

When the Qiskit compiler optimizations are added on top of the approximate circuits produced by QEst, there can be a slight improvement or degradation in CNOT count depending on the algorithm. For example, QEst + Qiskit performs better than QEst for the eight-qubit Heisenberg circuit, but it performs worse for the four-qubit XY circuit. Nonetheless, for most algorithms we observe that it does not diminish the gains of QEst and so we use the QEst + Qiskit configuration for evaluation results going forward.
QEst ensures low output distance from the ideal output while delivering a reduction in CNOT gate count.

QEst’s approximations result in a low output distance even in the ideal quantum computing scenario. We now evaluate if the approximate circuits produced by QEst are resulting in the correct output (close to ground truth results) even in the absence of noise. This can help us understand if the approximate circuits are closely emulating the expected output of the Baseline circuit. Fig. 9(a) and (b) show the TVD and JSD, respectively, between the ground truth output of the Baseline circuit and the approximated noiseless output of QEst. The figure shows that both the output distance metrics have low values across all algorithms. Given the corresponding reduction in CNOT gate count, these results signify the usefulness of circuit approximations even in a fault-tolerant environment. As both metrics have similar trends, we use only the TVD going forward for brevity.

QEst delivers a significant reduction in TVD on a real NISQ machine. Next, we evaluate the performance of QEst on IBMQ Manila, one of the most recent and least error quantum computers available via IBMQ open access for algorithms which were possible to run. Fig. 10 shows the TVD from the ground truth when the algorithms are run with just the Qiskit optimizations vs. when they are run with QEst + Qiskit. While the raw TVD numbers are large for most algorithms due to the high noise of the current state-of-the-art quantum computers, QEst + Qiskit reduces the TVD by over 0.3 or 30% points in some cases. For example, for the four-qubit TFIM circuit, the TVD drops from 0.35 to 0.08.

QEst delivers a significant reduction in TVD even for larger circuits and as hardware noise is decreased in a quantum simulation. We now present larger circuits run in a noisy simulation environment with noise levels of 1%, 0.5%, and 1% in Fig. 11(a), (b), and (c), respectively. The figures show the percentage reduction in TVD compared to when the Baseline circuit is run with a noisy simulation for Qiskit and QEst + Qiskit. We see that across the board, QEst + Qiskit reduces the TVD even as the hardware noise is reduced. This demonstrates the usefulness of circuit approximations even when projected on to the future when the noise is reduced by 10× (0.1% compared to the current average noise of over 1%). QEst incurs one-time cost for building approximate circuits to yield meaningful output quality for circuits with a large number of CNOT gates. QEst’s approximate circuit building process consists of three steps: (1) partitioning, (2) synthesis, and (3) dual-annealing engine. Fig. 12(a) and (b) show absolute time required for different circuit and relative contribution from each step. Overall, for most circuits QEst can be completed within a few hours. The only exception is TFIM 32 which takes almost a full day. Partitioning takes up most of the time due to TFIM circuit structure. Synthesis and dual-annealing engines are not major contributors.

While this one-time cost is non-negligible, it has potential for significant reduction (e.g., all blocks can be synthesized in parallel). But, we did not need to focus on reducing this overhead because of the feedback provided by the domain scientists and physicists who are actively working and improving the two major target applications. They assessed this cost is hidden in the code development and improvement cycle, and hence, wanted this effort to focus on obtaining meaningful output quality. For example, the magnetization curve for the Heisenberg application should match the ground truth curve. QEst achieved these algorithmic and science goals, as confirmed by our case study on TFIM and Heisenberg over their entire time evolution landscape (discussed below).

Also, we note that this overhead is not incurred each time the program needs to be compiled with Qiskit and executed. This is because QEst produces full approximate circuits as one-time output. This one-time output can be compiled with Qiskit (in the order of seconds) whenever needed for optimally mapping the approximate circuit on physical qubits.

4.3 TFIM and Heisenberg: A Case Study

QEst + Qiskit is able to more closely track the ground truth output than just Qiskit optimizations due to the larger reduction in the number of CNOT gates. Fig. 13 shows the time evolutions of the four-spin TFIM and Heisenberg circuits with ground truth, and the Qiskit circuit, and QEst + Qiskit approximate circuits when run on the IBMQ Manila computer. Each step in the time evolution is a different circuit that is separately run with QEst. For the TFIM algorithm, the QEst + Qiskit magnetization line is more stable and closer in magnitude to the ground truth than is the Qiskit magnetization.
Figure 11: Noisy simulations with different levels of noise indicate that QEst can reduce TVD even for future NISQ devices.

Figure 12: The execution time overhead of QEst and its division among the different steps varies for different algorithms.

Figure 13: QEst achieves closer to the ground truth output on the IBMQ Manila machine than the Baseline.

For Heisenberg, QEst very closely tracks the ground truth magnetization, while Qiskit produces meaningless results.

In fact, Fig. 14 plots the simulation results with noise levels 1%, 0.5%, and 0.1%, and the figure shows that projected reduction in hardware errors can further reduce the output distance for TFIM and Heisenberg. This is due to the large reduction in the CNOT gate count of both the algorithms.

Fig. 15(a) shows that circuit structure of the TFIM algorithm at the 100th timestep with Baseline and one of the approximations generated using QEst. Similarly, Fig. 15(b) shows the circuit structure of the Heisenberg algorithm at the 50th timestep. The figures illustrate the large reduction in CNOT gate count. For example, for the Heisenberg algorithm, the gate count reduced from 900 CNOTs to just 11 CNOTs with approximate circuits. This reduction enables fewer operations errors and lower decoherence errors due to faster execution.
QEst’s design decisions of using process distance upper bound threshold and dissimilar approximations yields good results. Fig. 16(a) and (b) shows the output of TFIM and Heisenberg algorithms for different process distance thresholds. Recall that if the threshold is set too high, the dual annealing engine is likely to select coarse approximations selecting more circuits with fewer CNOT gate count than selecting ones with dissimilar characteristics (approximations with low process distances among them). The figures shows that this can lead to a large error in the output distance for both algorithms. Thus, careful selection of the threshold is required to ensure beneficial results. However, it also does not have to be tuned exhaustively because as the figure shows, QEst performs well for a wide range of values. Therefore, we set the threshold to be proportional to the number of blocks in the circuit and it works well across all algorithms in practice.

5 RELATED WORK

Quantum Circuit Compiling and Mapping. There has been a large focus on attempting to leverage compiler-based passes and quantum computing rules to reduce CNOT and SWAP gate counts and perform noise- and layout-aware mapping of the qubits to the hardware [21, 26, 27, 35, 37, 39, 42, 44, 45].

For example, in the circuit mapping space, previous efforts have exploited the diverse error characteristics of different qubits to map the same baseline circuit in different ways expecting the output distances to reduce [31, 38]. But these works do not target reducing the CNOT count considerably by employing approximate synthesis to systematically generate dissimilar circuits and thus, have large output distances.

Quantum Circuit Synthesis. QEst employs synthesis as one of the steps in its procedure to generate approximate circuits. Previous synthesis works have attempted to synthesize circuits with only specific gates (e.g., only CNOTs) or universal circuits as exactly as possible with as few CNOT gates as possible [8, 13, 14, 17, 23, 29, 34, 36, 43]. We use a modified version of the Leap synthesis tool for QEST as it performs better than previous approaches [36].

Despite the potential of approximations, not many procedures to generate resource efficient approximations using synthesis have existed before QEst. Madden et al. [22] describe generative procedures using synthesis, but these procedures are non-scalable and lack any apriori criteria for selecting approximations across different algorithms. Amy et al. [2] describe a more scalable direct synthesis algorithm, but the approach leads to very long circuits, sometimes by orders of magnitude compared to other synthesis tools. In comparison, QEst defines a clear criterion for selecting dissimilar approximate circuits apriori, provides a theoretical proof to bound process distance, and generates circuits with few CNOTs.

6 CONCLUSION

In this work, we present QEst, a technique to reduce CNOT gate count of quantum circuits using approximate synthesis and distance-based approximation selection. We provided a theoretical derivation to bound the process distance of approximations as well as a dissimilarity criterion to select approximations in a manner that reduces the output distance. QEST achieves a CNOT gate reduction of 30-80% across algorithms while maintaining a low output distance from the output of the original circuit. While QEst’s contributions are beneficial in the NISQ era for minimizing the impact of noise, they are also useful for fault-tolerant quantum computers.

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