Black Start Operation using a MMC based HVDC system

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Abstract. Blackouts could occur due to various faults and in order to keep the power stations running constantly to avoid consumers losing power a backup plan is necessary. Black start is the process of restoring power to the electric power stations. The Modular Multilevel Converter (MMC) topology has been propitious technology in High Voltage DC (HVDC) system. The research in MMC technology has significantly increased. The MMC based HVDC system has many advantages when compared to the other technology based HVDC system. In this paper, Black Start Operation using a MMC Based HVDC system is proposed to provide continuous power to the load for a certain period of time within which alternative methods of power generation can be made ready. The paper also provides a mathematical model of a continuous equivalent circuit of the MMC Phase Leg. The efficiency of the proposed idea has been verified by MATLAB/Simulink Software and discussed.

Keywords—Black Start, Fault, High Voltage Direct Current (HVDC), Modular Multilevel Converter (MMC), MOSFET, Grid.

1. Introduction
The Black start [1] is a process that is generally performed in power stations or a particular part of the electrical grid where alternative methods are used to cope up with the lack of external power transmission that occurred due to a partial or complete shutdown. The power stations usually use small diesel generators to restore the energy in the grid. In the recent times, there has been tremendous expansions in modern power systems. Hence it has become a necessity to ensure the safety and reliability of these large-scale power systems. Blackouts are caused due to various reasons and pose potential threats to the power systems. Thus, black start methods are used to immediately restore power systems during a blackout. For the successful restoration of power to the power systems during black out, the blackout unit should have an adequate capacity which satisfies the plant’s total load and the needs of the start-up process should be met by its dynamic performance. During the black start, the power supply, with respect to black out unit’s capacity, should be studied and to ensure the voltage and power flowing through stay in an operational limit, the largest motor should be started. Traditional black start methods faced various issues such as self-excitation of the generator, maintain the fundamental frequency of the voltage, surges during the switching, frequency and voltage stability,
etc. The VSC-HVDC [13] is a better means of performing black start operation and various research has been taking place in this method of black start.

High voltage DC (HVDC) power transmission system [12] has a lot of practical importance. It has a lot of advantages like it costs lesser for a long-distance power transmission, no stability issues, lower losses than the High Voltage AC (HVAC). Studies on HVDC transmission system for black start operation suggests that it plays an important role in the recovery of the load, the grid and the power supply and it enhances the recovery process. For successful black start operation, a sufficient amount of back-up power is required to initialize the start-up power capability. There are three efficient methods that can act as source for black start operation. The first two methods focus on high voltage DC transmission (HVDC) system. The Line Commutated Converter (LCC) [4] and Voltage Source Converter (VSC) [8] based HVDC are the two methods. The micro grid is being the modern and third method that acts as a source for black start capability. LCC based HVDC system requires a network for commutation and also absorbs reactive power. These limitations in this system increase the cost of the system while using as a source in black start operation. The micro-grids [5] make uses of renewable energy [10] sources such as Bio-Diesel fed synchronous generators [7], solar and wind systems. The micro grid is capable of self-starting during black outs. The self-starting capability of micro grids is very low in terms of capacity which again has limitations while using as a source for black start operation. VSC based HVDC system is capable of operating at higher power ratings and these are more stable when compared with micro grids and LCC based HVDC system. It is capable of controlling the reactive and active power independently even in black start operation. HVDC transmission and MMC [14] together have immense potential in power electronics application.

Modular Multilevel Converter (MMC) [6] is one of the most ground-breaking power converter topologies in HVDC power transmission. It can produce pure sinusoids at high or medium voltages. Therefore, it is used for high power medium voltage applications. This converter has high modularity, redundancy and fault tolerant [2], [11] capacity. Its efficiency is as high as 99 percent and above. It has numerous sub-modules connected in cascade or series. The submodule consists of a switch and a capacitor voltage which acts as a DC source. The switch is also called as a cell. The dc links of these cells are isolated. The MMC has high structural scalability and can theoretically offer any level of current and voltage. The same converter can be used as an AC-DC converter or a DC-AC [9] converter by altering the algorithm of the device. Since the MMC is made up of a large number of modules which gives multilevel of voltage therefore filters are unnecessary for producing sinusoidal waveforms. It also has a good transient response. The MMC has great potential in power electronics application like HVDC transmission, Flexible AC transmission system (FACTS), high power motor drive application, etc. In the three-phase line-to-ground fault, all the three lines gets shorted and comes in contact with the ground. Due to this, all the power directly flows to the ground, therefore the magnitude of the current is drastically increased causing major damage in the power system.

This paper proposes a black start operation model to tackle the triple line-to-ground fault using a MMC based HVDC system and the proposed idea has been realized using MATLAB/Simulink software and its respective results have been discussed. The paper has been organized into six subsections respectively. The section two details about the system and its specifications. The section three describes about the working of the MMC. The mathematical modelling of the MMC has been discussed in section 4. In section 5, the simulation and its respective analysis has been given. The work gets concluded by section 6.

2. System Specifications

2.1 Block Diagram

The proposed block diagram in Figure 1 is an open loop system of a black start operation model using a MMC based HVDC system. The three-phase AC supply from the generation station is fed to the MMC through a circuit breaker that is triggered to open circuit condition during a fault. The MMC in the transmission substation performs the function of a rectifier by converting HVAC to HVDC which is then
transmitted over a distance greater than 500 kilometers. The HVDC is then converted back to HVAC by the MMC at the receiver substation and is tapped to the load.

![Figure 1. Block Diagram of the Proposed system.](image)

2.2 Simulation Specifications

The proposed system has been subdivided into three major blocks. The primary block being the source side block containing the three-phase source, three-phase fault along with three-phase breaker. The secondary block which is MMC block contains the MMC basic elements being capacitors, MOSFET’s and pulse generators. The final block being load side block contains the load and low power LC filter. The Table 1 shows the simulation specifications of the source side block. Similarly, Table 2 and Table 3 depicts the simulation specifications of MMC block and load side block respectively.

| Parameters                  | Specification                  |
|-----------------------------|--------------------------------|
| **Three-Phase source**      |                                |
| Configuration               | Y-g (Star-Ground)              |
| Phase-to-phase $V_{rms}$     | 122474.4871                    |
| Phase angle in degrees      | 0° for phase A                 |
| Frequency (Hz)              | 50                             |
| Resistance offered by source ($\Omega$) | $892.9 \times 10^{-3}$      |
| Inductance offered by source (H) | $16580 \times 10^{-6}$      |
| **Three-Phase Fault**       |                                |
| Initial status              | 0                              |
| Switching time (sec)        | 0.325                          |
| Fault resistance ($\Omega$) | $1 \times 10^{-3}$             |
| Ground resistance ($\Omega$) | $10 \times 10^{-3}$           |
| **Three-Phase Breaker**     |                                |
| Initial Status              | Open                           |
| Switching time (sec)        | 0.325                          |
| Breaker resistance ($\Omega$) | $10 \times 10^{-3}$         |
Table 2. Simulation specifications of MMC block

| Parameters                  | Specification   |
|-----------------------------|-----------------|
| **Capacitances**            |                 |
| DC link (F)                 | 0.01            |
| Capacitance (in Sub-Modules) (F) | 100*10^6       |
| **MOSFET**                  |                 |
| FET Resistance (Ω)          | 100*10^3        |
| Diode Resistance (Ω)        | 10*10^3         |
| Snubber Resistance (Ω)      | 100000          |
| Snubber Capacitance (F)     | infinity        |
| **Pulse Generator**         |                 |
| Pulse Type                  | Time based      |
| Amplitude                   | 1               |
| Period (secs)               | 20*10^3         |
| Pulse width                 | 50%             |
| Phase Delay                 | Varies according to logic |

Table 3. Simulation specifications of load side block

| Parameters                | Specification   |
|---------------------------|-----------------|
| **Load**                  |                 |
| Resistance (Ω)            | 1000            |
| **Low Power LC Filter**   |                 |
| Inductance (H)            | 200*10^3        |
| Capacitance (F)           | 50*10^6         |

3. Modular Multilevel Converter (MMC)

The Modular Multilevel Converter (MMC) was proposed by Rainer Marquardt in the year 2001 in Germany. It is one of the newest members of the multilevel family and has immense potential for various power electronics application even though its potential wasn’t realized immediately. The principle of the series connection of the low voltage cells in order to produce high voltage is applicable for the MMC technology.

3.1. MMC and its Cells

The Figure 2 shows basic structure of the MMC. It has three phases called as legs and each leg has two arms; positive and negative arms. The arm is made up of several cells. Each cell is made up of two Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) complimentary to each other to prevent
the shorting of the DC bus which is formed by a capacitor and an anti-parallel free-wheeling diode makes up a Half Bridge Circuit Model (HBCM) as whole. If ‘n’ number of these cells are cascaded or connected in series, we can get 2’n’+1 levels of voltages and the maximum amplification of the voltage is ‘n’ times of the input/source voltage. The same converter can be used as both AC-DC converter and DC-AC converter by changing the control logic. The positive and negative arms produce voltages with either different polarities or same polarity.

3.2. AC to DC MMC Converter
The Three-Phase AC to DC based MMC has two arms in each of the three phases; upper arm and lower arm. Each of these arms contain ‘n’ number of Half Bridge Sub Module (HBSMs) connected in series. The HBSM, as shown in the Figure 3, contains a capacitor with voltage across it Vc, two MOSFETs S1 and S2, each of them having anti-parallel diodes D1 and D2 respectively. It also has a protective thyristor T and a switch S across the MOSFET to bypass the faulty power modules to help the converter to function irrespective of the faulty module. By controlling the states of the MOSFETS S1 and S2, one Sub Module can generate two levels of voltages; 0 and Vc. In the Figure. 1, the DC voltage can be produced at side B from an available AC voltage from side B by making the polarities of the upper and the lower arm in the same direction, i.e., either both upwards or downwards.

3.3. DC to AC MMC Converter
The DC to Three-Phase AC based MMC has the same features as mentioned in the AC-DC MMC Converter as the same converter can be used as both. In the Figure 2, the AC voltage can be produced
at side A from an available DC voltage source at side B by making the polarities of the upper and the lower arm in the opposite direction. Inductors may be introduced in the arm to suppress the high-frequency components and to avoid the peaks in the arm current.

4. Mathematical modelling of MMC

Assuming that the converter has a switching frequency of infinity and each multivalve has infinite submodules. These assumptions help us in building a continuous model. For abbreviations used in modelling, Table 4 have been provided respectively.

From the Fig. 4, the following equations [14] can be analyzed by using Kirchhoff’s current law. The equation (1) is realized by using KCL from fig.4. The equations (2), (3) are the sub equations of (1).

\[ i_{umv} + i_{lmv} = i_v \]  \hspace{1cm} (1)
\[ i_{umv} = I_{S1} + I_d \]  \hspace{1cm} (2)
\[ i_{lmv} = I_{S2} - I_d \]  \hspace{1cm} (3)

Substituting (2) and (3) in (1), equation (4) can be framed.

\[ i_v = I_{S1} + I_d + I_{S2} - I_d = I_{S1} + I_{S2} \]  \hspace{1cm} (4)

The difference between the upper multivalve and lower multivalve current is given by (5).

\[ i_{umv} - i_{lmv} = I_{S1} + I_d - (I_{S2} - I_d) = I_{S1} + I_{S2} + 2I_d \]  \hspace{1cm} (5)

Considering each multivalve to have ‘n’ submodules. \( n_m = 0 \) indicates that all the ‘n’ submodules in the multivalve are bypassed and \( n_m = 0 \) indicates that all the submodules are inserted.

The sum of all the inserted capacitor voltage is given by (6).

\[ V_{cm} = n_m V \sum_{cm} \]  \hspace{1cm} (6)
Where $V_{\sum_{cm}}$ is multivalve total capacitor voltage.

From the Fig. 4, using Kirchhoff's voltages law, equations (7) and (8) have been given.

$$\frac{V_{dp}}{2} - n_{umv} \sum_{cumv} - V_0 = 0$$  \hspace{1cm} (7) \\
$$-\frac{V_{dp}}{2} + n_{lmv} \sum_{clmv} - V_0 = 0$$  \hspace{1cm} (8)

The sum of the intersection index is kept equal to 1. $(n_{umv} + n_{lmv} = 1)$

On subtracting (7) and (8), equation (9) can be framed.

$$V_{dp} - n_{umv} \sum_{cumv} - n_{lmv} \sum_{clmv} = 0$$  \hspace{1cm} (9)

On adding (7) and (8), equation (10) can be framed.

$$2V_0 = n_{lmv} \sum_{clmv} - n_{umv} + t \sum_{cumv}$$  \hspace{1cm} (10)

During a perfect balance $\sum_{cumv} = \sum_{clmv} = V$.

Due to imbalances in the multivalve voltages, the circulating currents develops. $i_d$ will become zero as the deviation from $V$ becomes zero.

Assuming:

$$I_{S1} = I_{S2} = \frac{i_v}{2}$$  \hspace{1cm} (11)

Substituting (11) in (2) and (3) and adding them result in (12).

$$i_d = \frac{i_{umv} - i_{lmv}}{2}$$  \hspace{1cm} (12)

This indicates that the outer voltage is only dependent on the difference between the upper and lower multivalve voltages. This voltage is considered as an inner alternating voltage denoted by $e_v$. The respective value has been given by (13) respectively. Table 4 depicts the abbreviations that are used in modelling of MMC

$$e_v = n_{lmv} \sum_{clmv} - n_{umv} \sum_{cumv}$$  \hspace{1cm} (13)

From (10) and (13), equation (14) can be analyzed

$$V_0 = \frac{e_v}{2}$$  \hspace{1cm} (14)

### Table 4. Abbreviations used in mathematical modelling.

| Denotations | Abbreviations |
|-------------|---------------|
| $i_{umv}$ | Current flowing in upper multivalve |
| $i_{lmv}$ | Current flowing in lower multivalve |
| $i_v$ | Output (AC) current |
| $i_d$ | Current circulating in the multivalve |
| $V_{dp}$ | DC voltage (pole to pole) |
| $V_{\Sigma_{Cumv}}$ | Sum of the upper multivalve capacitor voltage |
| $V_{\Sigma_{Clmv}}$ | Sum of the lower multivalve capacitor voltage |
| $V_{ia} = (n_{umv} V_{\Sigma_{Cumv}} - n_{lmv} V_{\Sigma_{Clmv}})/2$ | Inner alternating voltage |
| $n_{umv}$ | Multivalve (upper) insertion index in [0,1] |
5. Simulation Analysis

The simulation Figure 5 has been simulated using MATLAB/Simulink and its respective results have been discussed in this section. The overall simulation Figure has been given by Figure 5 respectively. The section can be divided into mainly four sections.

5.1 Proposed module
5.2 Source side analysis
5.3 MMC converter analysis
5.4 Load side analysis

5.1. Proposed Model

The Figure 5 represents the complete proposed model of Black Start Operation using a MMC based HVDC System in MATLAB/Simulink Software. The source is a three-phase star-grounded AC source providing 10 MW of power which delivers to the AC to DC MMC based converter through a circuit breaker which receives the negation of the fault command. The fault introduced in the system is a L-L-L-G fault which is introduced at 3.325 seconds. The power delivered to the AC to DC converter will be stored in the capacitances rated 0.01 Farad. The mid-terminal of the two capacitors has been grounded to prevent the peaks of the DC current damaging the MMC Modules. The stored DC is then converted to AC by a DC to AC MMC based converter. The MMC converters can be realized as nine-level module and each of the phases has a positive and a negative arm. Each of these arms has eight modules. The output of the DC to AC converter can be directly given to the load if the levels are increased to 40 or above as the MMC with large number of levels doesn’t require harmonic filters. The simulated circuit contains MMC with nine level output, therefore it requires low power LC filter to filter out the harmonics. The load is rated at 1 MW power, 82 A and 82000 V. The Figure 6, a small part of the positive and negative arms has been shown. Each of the modules in the arm contains 2 MOSFETs along with a capacitor. The pulse generating block, P1_9, supplies its signal to the first MOSFET of the first and the ninth module and the negation of the signal is supplied to the second MOSFET of the first and the ninth module. Similarly, the P2_10 pulse generating block supplies to the second and the tenth module and its negated pulse to the respective MOSFETs, the pulse width supplied to the 1st MOSFET of the 9th module is the same for the 2nd MOSFET of the 1st module.

![Figure 5. Simulation Figure of the Proposed system.](image-url)
5.2. Source Side Analysis
The Figure 7 shows the voltage across the three-phase AC source. As the source voltage is independent of the faults in the circuit, it remains constant throughout the entire time spectrum and therefore maintaining its voltage at 10 KV. The Figure 8 shows the current flowing through the system at the source before, during and after the fault. The current before the fault is very small, 1000A, compared to the current during and after fault, 100 MA, when the fault is introduced in the system at 0.325s. It can be inferred that

\[ V_{rms} = 100000 \sqrt{2} = 70710.67 \text{ V}, V_{il} = V_{rms} \times \sqrt{3} = 122.47 \text{ KV}, I_{rms} = 10000000 \sqrt{2} = 70.7 \text{ MA} = I_{lin} \text{ respectively}. \]

Figure 9 represents the circuit breaker command signal which toggles from High to Low when the fault is introduced at t = 0.325 secs.

5.3. MMC Converter Analysis

5.3.1. Converter One Results
The Figures in this section are related to the converter-1 leg-3 i.e., phase C. The same results would be applicable for phase A and phase B with 120-degree phase shift with respect to each other. The modules 1 is directly connected to the positive terminal of the capacitance. While module 16 is connected to the negative terminal. At the junction of Module 8 and 9 there is a connection to the AC
source, therefore, observations of Module 9 have been taken. Figure 10 represents the voltage profile of Converter 1 – Leg 3 – Module 1 – MOSFET 2 – Voltage. The voltage is maintained with a Peak value of 13500V before the fault. Peak value during the fault (introduced at 0.325s) =13000V. Peak value after the fault is 12000V. Figure 11 represents the current profile of Converter 1 – Leg 3 – Module 1 – MOSFET 2 – current. The current is maintained with a Peak value of 100000A before the fault. Peak value during the fault (introduced at 0.325s) =100000A. Peak value after the fault is 1000A. As the current before and after fault have a lot of difference in its magnitude, the current after fault looks like zero. Figure 12 represents the voltage profile of Converter 1 – Leg 3 – Module 16 – MOSFET 2 – Voltage. The voltage is maintained with a Peak value of 14000V before the fault. Peak value during the fault (introduced at 0.325s) =13000V. Peak value after the fault is 15500V. Figure 13 represents the current profile of Converter 1 – Leg 3 – Module 16 – MOSFET 2 – current. The current is maintained with a Peak value of 100000A before the fault. Peak value during the fault (introduced at 0.325s) =100000A. Peak value after the fault is 1000A. As the current before and after fault have a lot of difference in its magnitude, the current after fault looks like zero. Figure 14 represents the voltage profile of Converter 1 – Leg 3 – Module 9 – MOSFET 2 – Voltage. The voltage is maintained with a Peak value of 14500V before the fault. Peak value during the fault (introduced at 0.325s) =7500V. Peak value after the fault is 15000V. Figure 15 represents the current profile of Converter 1 – Leg 3 – Module 9 – MOSFET 2 – current. The current is maintained with a Peak value of 1000A before the fault. Peak value during the fault (introduced at 0.325s) =15000A. Peak value after the fault is 13000A. As the current before and after fault have a lot of difference in its magnitude, the current after fault looks like zero. Figure 16 represents the PWM pulse supplied to Converter 1 – Leg 3 – Module 16 – MOSFET 1. The amplitude of the PMW pulse is 1V and the frequency is 50Hz. Figure 17 represents the PWM pulse supplied to Converter 1 – Leg 3 – Module 16 – MOSFET 2. This is the negation of the PMW pulse in the Figure 16 with amplitude of 1 V and frequency 50 Hz.
5.3.2. DC-Link Results

The Figures in this section are related to the DC-link capacitance results respectively. Figure 18 represents the voltage in DC Link Capacitor C1 which remains at 110KV peak before the fault. After the fault at 0.325 secs the voltage across the Capacitance C1 starts to drop as it supplies the power to load. Figure 19 represents the average voltage in DC Link Capacitor C1 which remains at 100KV peak before the fault. After the fault at 0.325 secs the average voltage across the Capacitance C1 starts to drop as it supplies the power to load. Figure 20 represents the voltage in DC Link Capacitor C2 which remains at 110KV peak before the fault. After the fault at 0.325 secs the voltage across the Capacitance C2 starts to drop as it supplies the power to load. Figure 21 represents the average voltage in DC Link Capacitor C2 which remains at 110KV peak before the fault. After the fault at 0.325 secs the average voltage across the Capacitance C2 starts to drop as it supplies the power to load. Figure 22 represents the DC Link Current with peak value of 185 KA at before the fault. After the fault at 0.325 secs the Current flowing drops to 1000A which seems to be almost a zero compared to the large values of current before the fault.
5.3.3. Converter Two Results

The figures in this section are related to the converter-2 leg-3 i.e., phase C. The same results would be applicable for phase A and phase B with 120-degree phase shift with respect to each other. The modules 1 is directly connected to the positive terminal of the capacitance. While module 16 is connected to the negative terminal. Figure 23 represents the voltage profile of Converter 2 – Leg 3 – Module 1 – MOSFET 2 – Voltage. The voltage is maintained with a Peak value of 1450V before the fault. Peak value during the fault (introduced at 0.325s) =1300V. Peak value after the fault is 1300V. Figure 24 represents the current profile of Converter 2 – Leg 3 – Module 1 – MOSFET 2 – Current. The current is maintained with a Peak value of 13 KA before the fault. Peak value after the fault is 13 KA. Figure 25 represents the voltage profile of Converter 2 – Leg 3 – Module 16 – MOSFET 2 – Voltage. The voltage is maintained with a Peak value of 41 KV before the fault. Peak value during the fault (introduced at 0.325s) = 39 KV. Peak value after the fault is 42 KV. Figure 26 represents the current profile of Converter 2 – Leg 3 – Module 16 – MOSFET 2 – Current. The current is maintained with a Peak value of 12 KA before the fault. Peak value after the fault is 12.5 KA. Figure 27 represents the PWM pulse supplied to Converter 2 – Leg 3 – Module 16 – MOSFET 1. The amplitude of the PWM pulse is 1V and the frequency is
50Hz. Figure 28 represents the PWM pulse supplied to Converter 2 – Leg 3 – Module 16 – MOSFET 2.

5.4. Load Side Analysis

The Figure 29 shows the profile of load voltage during the simulation run. The Figure 30 is the zoomed version of Figure 29 and Figure 31 shows the profile of load current during the simulation run. The Figure 32 is the zoomed version of Figure 31. It can be seen that the waveforms have been at constant variations till $t = 0.32$ seconds, after 0.32 seconds the load profiles have some fluctuation which are due to the fault where high amount of current is flowing for few seconds as seen in Figure 32 and load being resistive the same profile have been followed by load voltage. As circuit breaker opens its states after few milli seconds of fault, the current and the voltage gets stabilized. From the Figure 30 and Figure 32, the peak voltage is 82000V and peak current is 82A. $V_{p} = \frac{82000}{\sqrt{2}} = 57982.75 V$, $V_{l} = V_{p} \times \sqrt{3} = 100.43 kV$, $I_{rms} = \frac{82}{\sqrt{2}} = 57.98 A = I_{l}$. It can be seen in the Figure 33 and Figure 34, that there are 3 phase A B C, and in each phase, it can be observed that there are nine levels in both voltage and current waveform. Figure 33 shows the load voltage without any rated LC filter and Figure 34 depicts the load current profile without LC filter. It can be observed from Figure 35 that the 10 MW power has been delivered to the load till 0.32 sec, due to rise in the peak values of current and voltage, the power also rises for 0.02 ms as seen in the
above simulated graph. Later on, as the capacitor starts discharging, the load power also starts decreasing. Usage of the highest level MMC powers the load constantly for some more time.

Figure 29. Load Voltage in volts.

Figure 30. Zoomed version of Load Voltage in volts.

Figure 31. Load Current in Amps.

Figure 32. Zoomed version of Load Current in Amps.

Figure 33. Load Voltage in Volts without LC filter.

Figure 34. Load Current in Amps without LC filter.

Figure 35. RMS Load Power in watts.

6. Conclusion
A black start operation model has been discussed to tackle the triple line-to-ground fault using a MMC based HVDC system. The MMC has high structural scalability and can theoretically offer any level of current and voltage. The MMC is a highly versatile device which can be used for both AC-DC conversion and DC-AC conversion by just altering the algorithm of the device. Since the MMC is made up of a large number of modules which gives multilevel, filters are unnecessary for producing sinusoidal waveforms. It also has a good transient response. The MMC has great potential in power
electronics applications like HVDC transmission, Flexible AC transmission systems (FACTS), high power motor drive application, etc. The simulation for the proposed system has been done and its respective results have been discussed. At time t=0.325 sec the L-L-L-G fault has been introduced in the system and the MMC based HVDC technology is able to power the load continuously even when the circuit breaker has been opened during the fault detection. The system has been proven well working for the critical loads for continuous power flow during black outs.

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