ChewBaccaNN: A Flexible 223 TOPS/W BNN Accelerator

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Abstract—Binary Neural Networks enable smart IoT devices, as they significantly reduce the required memory footprint and computational complexity while retaining a high network performance and flexibility. This paper presents ChewBaccaNN, a 0.7 mm² sized binary CNN accelerator designed in global-foundsries 22 nm technology. By exploiting efficient data re-use, data buffering, latch-based memories, and voltage scaling, a throughput of 233 GOPS is achieved while consuming just 1.2 mW at 0.4V/154MHz for the inference of binary CNNs with 7x7 kernels, leading to a core energy efficiency of 223 TOPS/W. This is up to 4.4x better than other specialized binary accelerators while supporting full flexibility in kernel configurations. With as little as 3.9 mJ, using an 8-fold ResNet-18, a Top-1 accuracy on ImageNet of 67.5% can be achieved, which is just 1.8% less than using the full-precision ResNet-18.

Keywords—Binary Neural Networks, Hardware Accelerators

I. INTRODUCTION

CONVOLUTIONAL neural networks have revolutionized the machine learning field in recent years, outperforming humans in image recognition [1] and advancing the state-of-the-art for a wide range of applications [2]. Most of these networks require billions of multiply-accumulate operations per frame and millions of trained parameters. This is incompatible with hundreds of KB of on-chip memory and the limited energy available on battery-powered, low-cost IoT sensor nodes. A common approach is to analyze the data in the cloud for ease of deployment and to avoid the performance limitations of edge devices. However, transmitting the data comes with a high energy cost, introduces privacy concerns, requires expensive infrastructure, and has a high latency. Thus, the focus has shifted to analyze the data near the sensor, which has given rise to research into hardware accelerators [3]. Besides data flow optimizations and data reuse to improve the throughput and energy efficiency of convolution operations, particular focus has been put on reducing off-accelerator data transfers [4], [5], memory accesses and the operation complexity through architectural improvements, reduced-precision operands [6], skipping zero-multiplications [7], and on-the-fly feature map and model compression [8].

Furthermore, the research community has proposed several algorithmic advances to enable inference at the edge reducing the number of operations by choosing smaller kernel sizes [9], reducing input channels [9], increasing the number of skippable operations [10], weight sharing [11], decompose 2D convolutional layers into 2 sequential 1D (depth-wise and/or spatial) convolutional layers [12], limiting inter-channel dependency by channel grouping [13], and using quantized fixed-point arithmetics (e.g., [14]).

In particular, arithmetic precision scaling has shown significant potential, due to its inherent reduction in memory requirements (i.e., feature maps and weights), and computational complexity. CNNs have been proven to be robust to quantization down to 16-bit without retraining [15], and 8 bits with retraining [16]. Binary Neural Networks push the idea of quantization to the limit and quantize weights, and feature maps to a single bit representing the values -1 and 1. XNOR-Net extends the stochastic gradient descent algorithm (commonly used to train NNs) by quantizing the weights and activations in the forward path and scales the feature maps to matrix norm of the weight kernels [17]. On the challenging ImageNet Large Scale Visual Recognition Challenge, Rastegari et al. achieved 51.2% using a binarized ResNet-18, which was a significant drop of -18.1%. Courbariaux et al. achieved then state-of-the-art results with 99.04 on MNIST (+0.34%), 97.47 on SVHN (-0.09%), and 89.85% CIFAR-10 (-0.46%), but these datasets are much simpler than ImageNet [18]. Recent research has been focusing mainly on minimizing the quantization error (e.g., scaling feature maps in XNOR-Net), improving the loss function, and reducing the gradient error [19], [20]. Recently, the accuracy gap between BNNs and their full-precision equivalent have been brought down to 12% (DoReFaNet on AlexNet [21]). This accuracy gap can be reduced by using multiple binary layers (i.e., weight bases) in parallel and binarizing around multiple thresholds (i.e., activation bases). Using 3 weight bases, Lin et al. [22] have achieved 69.3%/89.2% (Top-1/Top-5, -8.3%/–6.0% vs. ResNet-18) and Zhuang et al. reached 72.8%/90.5 (Top-1/Top-5, –3.2%/-2.4% vs. ResNet-50) using 8 weight bases [23]. Using multiple bases directly impacts the throughput and energy per inference for any given hardware accelerator, negating some of the benefits of BNNs. However, it provides the opportunity to smoothly scale from a highly efficient, less accurate network to almost full accuracy inference.

Several BNN hardware accelerators have shown an energy efficiency gain of around two orders of magnitude is achievable compared to quantized neural network accelerators. By reason of avoidance of off-chip data transfers and the exploiting of the extreme reduction in arithmetic complexity where full-precision multiply-accumulate becomes binary xnor-poopcount. In [24], Conti et al. presents a 46TOPS/W BNN accelerator tightly-connected to a general-purpose processor (without considering off-accelerator memory and I/O costs), UNPU is a stand-alone accelerator for flexible weights (i.e., 1-16 Bits) and feature maps and reaches 51 TOPS/W for fully-binary NN [25], and BinarEye presents a full-custom accelerator for BNN fully-

1 composed of more than 1 million images of 1000 different object classes
specialized with 64 channels and only $2 \times 2$ kernels, achieving a peak core energy-efficiency of 230 TOPS/W.

In this paper, we present ChewBaccaNN, a binary CNN accelerator designed in GlobalFoundries 22 nm FDX technology, exploiting the reduced arithmetic complexity using xnor-gates and efficient popcount adder trees, energy-efficient latch-based memories, and voltage scaling. ChewBaccaNN supports the main primitives of CNNs such as pooling, (batch) normalization, and ReLU activation and is configurable for kernel sizes from $1 \times 1$ to $7 \times 7$. Due to the significant reduction of the memory requirements, all feature maps can be stored on-chip without incurring unnecessary accesses to external storage devices. ChewBaccaNN is the 2nd generation of XNORBIN [26] (in UMC 65 nm), exploiting the more advanced, lower power 22 nm FD-SOI technology node. SRAMs have been replaced with much more energy-efficient latch-based memories; furthermore, power-gating of unused memory banks, silencing of unused compute units, and extending the voltage range have been introduced. Additionally, we have extended ChewBaccaNN to support pooling on the binary activations, average pooling, and support for residual paths through the Near-Memory Compute Unit (NMCU), enabling inference on SoA binary ResNets. The energy efficiency at 0.4 V has been increased by 2.3× from 95 to 223 TOPS/W at roughly the same throughput/frequency of 244 GOPS/156 MHz and 2.3× lower power consumption (i.e., 2.6 to 1.13 mW) compared to XNORBIN at its lowest-voltage operating point (0.8 V). Additionally, we present in detail algorithmic optimizations that can be used to exploit fully-binary neural network acceleration. Then, we evaluate the top SoA networks on ChewBaccaNN, demonstrating flexibility combined with leading-edge energy efficiency.

II. BNN AND RELATED HW OPTIMIZATION

In BNNs, the weights and intermediate feature maps are quantized to a single bit: $X \in \{-1,1\}^{n_{in} \times h \times w}$, $W \in \{-1,1\}^{n_{out} \times n_{in} \times k_h \times k_w}$. After the multiplication, which is reduced to a xnor operation, these products and a bias value are accumulated in full-precision followed by re-binarizing the product, thus replacing the activation function and are accumulated in the feature maps. By merging the number of accumulated contributions, by merging the number of accumulated contributions, by merging the number of accumulated contributions, and rearranging, the formula can be turned into the same form as in Eq. 1, where multiplications within the convolutions are replaced by xnor operations indicated by $\otimes$:

$$o_k = \text{sgn} \left( C_k + \sum_{n=0}^{n_{in}-1} \left( 2 \cdot i_n \otimes w_{k,n} - k_y k_x \right) \right)$$

The (-32)-term compensates for the 32 parallelly calculated input channel contributions. Even though the weights and feature maps stay binary, the accumulation itself and the learned bias/scaling factors for batch normalization are still represented in non-binary form:

$$\hat{o}_k = \text{sgn} \left( \hat{C}_k + \hat{\alpha}_k \sum_{n=0}^{n_{in}-1} \left( i_n \otimes \hat{w}_{k,n} - \mu_k \right) \right)$$

In the implementation, $\mu_k$, $C_k$, $\alpha_k$ and $\sigma_k$ can be absorbed into a single threshold $\theta_k = \frac{C_k \alpha_k}{\sigma_k} + \mu_k$ applied on the sum of products:

$$o_k = \begin{cases} -1, & \sum_{n=0}^{n_{in}-1} i_n \otimes w_{k,n} < \theta_k \\ 1, & \text{else} \end{cases}$$

Pooling is applied after convolution, scaling, and batch normalization, but before the re-binarization and, therefore, in the non-binary domain. However, due to the monotonicity and commutativity, the pooling function can be calculated as a Boolean operation (e.g., max/min-pooling becomes AND/OR and average-pooling becomes Boolean majority voting).

$$\text{Pool}(o_k(x,y)) = \begin{cases} -1, & \max_{m,n \in [0,1]} \left( o_k(2x+m, 2y+n) \right) < \theta_k \\ 1, & \text{else} \end{cases}$$

$$= \begin{cases} -1, & \min_{m,n \in [0,1]} \left( o_k(2x+m, 2y+n) \right) < \theta_k \\ 1, & \text{else} \end{cases}$$
III. ARCHITECTURE

The architecture of ChewBaccaNN is illustrated in Fig. 1 and its components are explained as follows:

Each Basic Processing Unit (BPU) performs a 1D convolution of an input image row with a kernel row from 16 input channels at a time, by employing \( xnor \)-sum units consisting of 16 \( xnor \)-gates each and a popcount adder tree.

The \( xnor \)-sum unit is replicated 7 times to produce outputs corresponding to a window size of at most 7 input feature map pixels in a row. Outputs from all units are accumulated together with a second stage adder tree to create 1D inner product, shown in Fig. 2. 7 BPUs are instantiated in order to support kernel sizes up to \( 7 \times 7 \). The outputs of all these instances are pipelined to increase throughput and are then added up in a third stage adder tree to produce 2D inner product. Each of the \( xnor \)-sum instances is fed with the input activations and weight data through a controlled shift-register to enable data reuse. The same BPU array datapath is reused to perform binary max-pooling operation, where the 2\(^{nd} \) and 3\(^{rd} \) stage adder trees are flanked by a 1 bit comparator (AND gate) tree.

ChewBaccaNN comes with a Feature Map Memory (FMM) and data buffering. The FMM stores the feature maps and the partial sums of the convolutions. The memory is divided into two blocks, where one serves as the data source (i.e., current input feature maps), and the other serves as data sink (i.e., partial or final output feature maps). They are swapped after each layer. If the FMM is dimensioned to fit the largest intermediate FMs, no energy-costly off-chip memory accesses are needed during inference. To conceal the weight loading latency, the PB is enriched with a double buffering feature. The Parameter Buffer (PB) stores the weights, the binarization thresholds, and the configuration parameters. In the optimal case, it stores all the weights of the network to avoid I/O for weight loading. If the parameters are too many to fit on-chip, the PB can be reused to buffer off-chip accesses. The Row Banks are used to buffer rows of the input feature maps for frequent accesses. It also contains rows of filter weights corresponding to the batch of output channels calculated in parallel. Since these row banks need to be rotated when shifting the convolution window down, they are connected to the BPU array through a crossbar. The crossbar connects the registers inside the BPUs, the controlled shift registers (L1) (CSRs) containing kernel input feature map elements, and the filter weight elements. These are shifted when the convolution window is moved forward. The DMA moves data independently from FMM and PB into (via Row Banks) and out of the BPU array. Scheduler: According to a given layer configuration of a CNN, the scheduler controls the crossbar on how and when to route feature map and weight data from the Row Banks to the BPUs in order to compute row-wise partial sums for each member in the batch. The Near Memory Compute Unit (NMCU) is illustrated in Fig. 3 and is used for on-the-fly computation when writing back to the main memory. This includes partial sum calculations from the BPU array, accumulating residual paths from the FMM, the binarization, and storing back to the FMM in a packed format (i.e., 16 activations).

To maximize kernel-level reuse, filter weights are retained in BPUs while streaming selected image rows through BPUs, and partial sums are computed concurrently for a batch of output feature map tile to maximize row-level image reuse. The resulting integer value that is produced from the BPU array in each cycle as a result of a horizontally sliding convolution window is forwarded to the DMA controller via the Near-Memory Compute Unit (NMCU). The CU accumulates the partial results by means of a read-add-write operation. After the final accumulation of partial results, the unit also performs the thresholding/re-binarization operation (i.e., activation and batch normalization). The binary results are packed into 16-bit words and written back to the memory by the DMA unit. The scheduling is determined with the objective of maximizing the data reuse at different levels of the memory hierarchy. The scheduling algorithm and mapping of operations to BPU units are explained in Alg. 1 based on the filter dimensions \( k_w \) and \( k_h \), the spatial input dimensions \( i_w \) and \( i_h \), the depths (i.e.,
Algorithm 1 High-level scheduling of 1 BNN layer

Require: \( k_w, k_h, i_w, i_h, c_i, c_o, \hat{c}_i, \hat{c}_o \)
1: \( \text{for } n_o \leftarrow 0 \text{ to } c_o/\hat{c}_o \text{ do} \)
2: \( \text{for } n_i \leftarrow 0 \text{ to } c_i/\hat{c}_i \text{ do} \)
3: \( \text{for } n_{row} \leftarrow 0 \text{ to } i_h \text{ do} \)
4: \( \text{for } b_o \leftarrow 0 \text{ to } \hat{c}_o \text{ (per BPU array in parallel) do} \)
5: \( \text{pass kernels of channel } b_o \text{ to Bank memory} \)
6: \( \text{for } k_{row} \leftarrow -(k_h/2) \text{ to } (k_h/2) \text{ (parallel) do} \)
7: \( \text{for } k_{col} \leftarrow -(k_w/2) \text{ to } (k_w/2) \text{ (parallel) do} \)
8: \( \text{for } b_i \leftarrow 0 \text{ to } \hat{c}_i \text{ (HW parallel) do} \)
9: \( \text{pass input feature map pixel } (b_i, n_{row}, n_{col}) \text{ and weight } (b_o, b_i, k_{col}, k_{row}) \text{ to BPU array } b_o \)
10: \( \text{calculate xnor-popcount and accumulate} \)
11: \( \text{end for} \)
12: \( \text{end for} \)
13: \( \text{Binarize final partial sums} \)
14: \( \text{Pool operation (if applicable)} \)
15: \( \text{end for} \)
16: \( \text{end for} \)
17: \( \text{end for} \)

Fig. 4: Throughput vs. Core Energy Efficiency for various timing constraints at 0.4 V supply voltage and FMM=4 kB.

Fig. 5: Floorplan of ChewBaccaNN core

IV. RESULT

A. Physical Implementation

ChewBaccaNN has been implemented with a 7.5 track standard-cell libraries in Globalfoundries 22nm FDX technology, synthesized with Synopsys Design Compiler 2018.06. Cadence Innovus 18.11 was used for back-end design and power simulation, and Questa Modelsim 10.6b has been used for verification and extraction of switching activities for power simulation. To reach the highest energy efficiency, we operate at VDD=0.4 V with 0.1 V forward body-biasing. To scale the voltage down to this level and to reduce the energy cost per memory access by 3.5×, we use standard-cell memories (SCMs) instead of SRAMs. The SCMs are designed with hierarchical clock gating and address/data silencing mechanisms, thus when a bank is not accessed the whole latch array consumes no dynamic power [6]. The SCMs are composed of multiple banks of 256 words \( \times \) 32 bit (1 kB). The FMM is dimensioned to fit the two largest consecutive layers of the network, which has to be supported without tiling. We have selected them to be either 16 and 32 SCM banks (48 kB) for AlexNet or 2 \( \times \) 73 banks (146 kB) for both AlexNet and ResNet-18; the parameter buffer 2 banks (3.5 kB) and the 7 row bank memories consist of 1 SCM bank each (i.e., 3.5 kB in total). The final floorplan is shown in Fig. 5. It can be seen that a large part of the chip (i.e., 97%) are memories, whereas the compute units just occupy 1% of the total chip area of 0.7 mm\(^2\). The power consumption has been evaluated with back-annotated post-layout simulation. The stimuli vectors, including weights, input feature maps, and configuration is generated from the network model in Torch by a custom compiler written in Python, and streamed to the accelerator through the input interface. I/O energy has been estimated with 21 pJ/bit based on LPDDR3 memory access cost evaluation [4].

B. Throughput to Energy Trade-Off

We have synthesized (i.e., same color for same timing constraints) and run back-ends at various timing constraints, to explore out the energy-efficiency to throughput trade-off at 0.4 V. The results are shown in Fig. 4. Due to the lower density of the SCM memories compared to SRAMs, the chip reports high leakage (i.e., dashed line represents energy efficiency limit...
based on leakage power), which limits the core energy efficiency to 185/100/39.0 TOPS/W with 48kB FMM (i.e., same size as XNORBIN) at a throughput of 241/123/44.4 TOPS and a core power consumption of 1.3/1.2/0.90 mW for the full-utilization case of \(7^2/5^2/3^2\) kernel sizes. Fortunately, most of the FMM banks stay unused and can, therefore, be power-gated. Thus, with 4 active banks (4 kB) the energy consumption reduces to 1.08/0.99/0.68 mW and the energy efficiency can be increased up to 223/124/65 TOPS/W. UNPU supports CNN inference with \(3 \times 3\) and \(5 \times 5\) kernels, ChewBaccaNN is \(2.0\times\) more energy-efficient than UNPU [25]. For \(7 \times 7\) kernels ChewBaccaNN outperforms UNPU even \(4.4\times\). The highest efficiency value has been reported by BinarEye with 230 TOPS/W, but BinarEye can handle only 64 channels and is limited to uncommon \(2 \times 2\) kernels, and is \(2 \times\) larger (1.4 mm\(^2\)) than ChewBaccaNN.

C. Accuracy and Energy-Efficiency for Various BNNs

In this section, we compare several published BNNs and how efficiently they map to ChewBaccaNN in Tab. I. The first two BNN networks have been used in embedded applications. Rusci et al. trained and implemented a VGG-like network on the CIFAR-10 dataset which does image recognition on \(32 \times 32\) colored images with 10 classes, and achieves an accuracy of 86.6\% (4.6\% less than FP32 baseline) [28]. Cerutti et al. presented a BNN for Sound Event Detection on the Freesound database with 28 classes [29]. The audio data is converted to a Mel-frequency cepstral spectrogram and fed to a binary CNN with \(5 \times 3\) layers with \(3 \times 3\) kernels, followed with \(3 \times 3\) kernels with \(1 \times 1\) kernels. They achieve 77.9\% of accuracy (i.e., a drop of 7.9\% with respect to full-precision). Both networks have been implemented on the low-power Gapuino board featuring the GAP8 multi-core processor, with \(8 \times 1\) energy-optimized RISC-V cores implementing the RISC-V RV32IMC ISA and the Xpulp ISA extensions (i.e., supporting bit-manipulation, popcount, hardware-loop, post-increment load/stores, ...) [30]. In Cerutti et al.’s network, we tile the input FM in 2 tiles with an overlap of 20 columns to fit in the 146 kB FMM. Running these networks on ChewBaccaNN has an actual energy consumption of 3.9/296\(\mu\)J/frame, a 195/86\(\times\) improvement over the embedded GAP8 implementation.

Furthermore, we evaluate the SoA BNN networks on the challenging ImageNet image classification challenge. DoReFaNet with the smallest reported Top-1 accuracy gap of 12.3\% [21], XNOR-Net++ with the best Top-1 accuracy with standard BNNs [31], and the two multi-base binary networks ABC-Net [22] and Zhuan et al. [23]. DoReFaNet was evaluated with 48 kB FMM, and the others with 76 kB FMM. ABC-Net extends ResNet-18 with 3 parallel BNN layers per original full-precision layer (i.e., 3 weight bases) and reaches an accuracy of 61.0\% (-8.5\%) requiring 1.46 mJ and Zhuan et al. 67.5\% (-1.8\%) with \(8 \times\) bases with a 3.9 mJ energy cost per frame. XNOR-Net++ can be run at an energy cost of 487\(\mu\)J at 61\% Top-1 accuracy and a throughput of 23 GOPS.

| TABLE I: Real network performance on SoA BNNs. Gap shows the perf. difference to the full-precision baseline net. |
|---|---|---|---|---|---|---|---|---|---|---|
| Acc. | Gap | Util.% | Core Eff. | Dev. Eff. | P | En. | Throughput |
| % | Δ% | % TOPS/W | TOPS/W | mW | mJ | TOPS/W | GOPS | FPS |
| CIFAR-10 | 10 classes, 3\(\times\)32\(\times\)32 |
| [28] VGG | 86.8 | -4.6 | 54.3 | 24.5 | 7.5 | 3.2 | 1.4 | 23.9 | 2.3k |
| Freesound, Sound Event Detection with 28 classes, 1\(\times\)400\(\times\)64 MFCC Spectrograms |
| [29] 5C\(\times\)5, 3C\(\times\)1 | 77.9 | -7.9 | 18.9 | 10.6 | 7.7 | 3.2 | 296 | 16.8 | 7.2 |
| ImageNet | 1'000 classes, 3\(\times\)224\(\times\)224 |
| [21] AlexNet | 43.6 | -12.3 | 45.3 | 27.8 | 13.8 | 2.1 | 141 | 28.5 | 14.7 |
| [31] ResNet-18 | 57.1 | -12.2 | 52.0 | 14.6 | 6.5 | 3.5 | 487 | 23.0 | 7.2 |
| [22] 3\(\times\) ResNet-18 | 61.0 | -8.3 | 52.0 | 14.6 | 6.5 | 3.5 | 1462 | 23.0 | 2.4 |
| [23] 8\(\times\) ResNet-18 | 67.5 | -1.8 | 52.0 | 14.6 | 6.5 | 3.5 | 3900 | 23.0 | 0.9 |

V. CONCLUSION

We have described a best-in-class BNN accelerator that achieves an energy efficiency of up to 223 TOPS/W, while keeping the flexibility of running a wide range of BNNs, an improvement of 4.4x over the closest competitor UNPU, which reaches 51 TOPS/W. We can run state-of-the-art BNNs such as XNOR-Net++ or the one by Zhuang et al., reaching a Top-1 accuracy of 61.0\% and 67.5\% on ImageNet at merely 1.46 and 3.9 mJ/frame, respectively.

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