Abstract

We propose a flexible framework that can be easily customized to enforce a large variety of information flow properties. Our framework combines the ideas of secure multi-execution and map-reduce computations. The information flow property of choice can be obtained by simply changes to a map (or reduce) program that control parallel executions.

We present the architecture of the enforcement mechanism and its customizations for non-interference (NI) (from Devriese and Piessens) and some properties proposed by Mantel, such as removal of inputs (RI) and deletion of inputs (DI), and demonstrate formally soundness and precision of enforcement for these properties.

1 Introduction

Information flow properties define the acceptable behaviours of computer programs with respect to allowed and forbidden flows of information. The most well-known information flow property is non-interference (NI), which roughly requires that the input data classified as confidential (also called secret, or high) should not influence the public (low) outputs [7, 6].

By weakening or strengthening the definition of NI in order to address some of its problems, security researchers have proposed different information flow properties [15, 16, 9, 17, 26]. For instance, the definition of NI in [7] is based on an assumption that if there is no high input, then there is no high output. This assumption does not always hold. In [17], the generalized non-inference (GNF) property is defined for systems that generate high outputs even if there are no high inputs.

Different information flow properties led to different enforcement techniques. To the best of our knowledge, there is no proposal in the literature with a unified approach to the enforcement of multiple information flow properties. The existing enforcement mechanisms (e.g. [6, 5, 25, 14, 20, 5]) can be configured to accommodate different information flow policies that identify what is confidential and what is public, and what are the authorized flows in the security lattice [6, 21], and, sometimes, they can as well enforce declassification
Tab. 1: Enforcement mechanisms for the selected information flow properties

| Property                  | Section | Components | MAP   | REDUCE | $T_M$/$T_R$ |
|---------------------------|---------|------------|-------|--------|-------------|
| Removal of inputs [15]    | § 5.1   | Fig. 10a   | Fig. 10b | Fig. 10c | Fig. 10d    |
| Deletion of inputs [15]   | § 5.3   | Fig. 17a   | Fig. 17b | Fig. 17c | Fig. 17d    |
| Termination (in)sensitive | § 5.2   | Fig. 14a   | Fig. 14b | Fig. 14c | Fig. 14d    |
| non-interference [6]      |         |            |        |        |             |

Yet, the adaptation of an existing enforcement mechanism (for example, for NI) to enforce another property (for instance, GNF) is not straight-forward.

We aim to fill this gap by providing an enforcement framework that can be extended by different information flow properties. The framework is inspired by the MAP-REDUCE approach explored by Google [12]; and generalizes the secure multi-execution (SME) technique proposed by Devriese and Piessens in [6] so that it can enforce other information flow properties, e.g. properties from [15].

The main idea is to execute multiple “local” instances of the original program, feeding different inputs to each instance of the program. The local inputs are produced from the original program inputs by the MAP component, depending on the set of security levels defined in the framework and the input channels available. Upon receiving the necessary data (for instance, after each individual program instance is terminated), the REDUCE component collects the local outputs and generates the common output, thus ensuring that the overall execution is secure. MAP and REDUCE are customizable and by changing their programs the user can easily change the enforced property. Two simple tables ($T_M$ and $T_R$) tell MAP and REDUCE what they should do when receiving respectively input and output requests from local executions on a channel.

In this report we present the following contributions:

- The architecture of this flexible enforcement framework.
- A set of simple instructions for programming the framework components, such as a “clone” instruction to spawn new processes.
- The instantiation of the framework’s configuration for non-interference (NI) from [6], Removal of Inputs (RI) and Deletion of Inputs (DI) from [15]. The components are summarized in Tab. 1. We prove formally soundness and precision of these enforcement mechanisms with respect to the corresponding properties for a model programming language with simple I/O instructions.
- An example on how a simple change to the configuration can lead to the enforcement of new information flow properties.

The rest of the paper is organized as follows. §2 gives an overview of the idea behind our approach and the architecture of the enforcement framework. The

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1These policies are required when one needs to disclose information that depends on confidential data in some way, see e.g. [15] [22] for details.
Fig. 1: Architecture of enforcement mechanisms

2 Overview

Fig. 1 depicts the general architecture of the enforcement mechanism for an information flow property on a program $\pi$. It is composed by a stack $EX$ of local executions ($\pi[0], \ldots, \pi[TOP]$, where $TOP$ is the index of the top of the stack), global input and output queues, the MAP and REDUCE components, and the tables $TM$ and $TR$.

Local executions (instances of the original program that are executed in parallel and are unaware of each other) are separated from the environment input and output actions by the enforcement mechanism. A local execution has its own input and output queues. The local input (resp. output) queue of a local execution contains the input (resp. output) items that can be freely consumed (resp. generated) by this local execution. MAP and REDUCE are responsible for respectively the global input queue containing the input items from the external environment (received from the user or other input channels), and the global output queue containing the output items filtered by the enforcement mechanism to the environment.

When a local execution needs an input item that is not yet ready in its local input queue, it will request the help of MAP by emitting an interrupt signal (or just signal for short). When different local executions request values from the same channel, there will be only one actual input action performed by the enforcement mechanism. After the value is read, MAP will distribute it to local executions, replacing the actual value by the default (fake) one, if necessary. Similarly, when a local execution generates an output item, the output item will be handled by REDUCE.

MAP and REDUCE can also autonomously send and, respectively, collect items from local queues. For example, upon receiving an input item from the environment, MAP can send it to all local executions that satisfy a predicate.
\[ \pi ::= \text{instructions} : \]
\[
\mid x := e \quad \text{assignment} \\
\mid \pi; \pi \quad \text{sequence} \\
\mid \text{if } e \text{ then } \pi \text{ else } \pi \quad \text{if} \\
\mid \text{while } e \text{ do } \pi \quad \text{while} \\
\mid \text{skip} \quad \text{skip} \\
\mid \text{input } x \text{ from } c \quad \text{input} \\
\mid \text{output } e \text{ to } c \quad \text{output} \\
\]

Fig. 2: Language instructions

The parallel broadcast and parallel collection to and from local processors are the characteristic features of MAP-REDUCE programs \[12\]; this explains our choice for the name of the enforcement mechanism.

The actions of MAP (respectively REDUCE) on an input (output) request from a local execution depend on the configuration information in the table \[T_M (T_R)\]. These components of the enforcement mechanism are customized depending on the desired information flow property. The framework components configured to implement the chosen information flow properties are listed in Tab. 1 (for each selected property the table contains pointers to the actual component configurations).

The configuration of input and output actions of local executions is based on two privileges: ask (a) and tell (t). If a local execution has the ask privilege on the input channel \(c\), then MAP can fetch the input item from the environment upon receiving the interrupt signal from a local execution. If a local execution has the tell privilege on the input channel \(c\), then this local execution can get the real value from the channel \(c\) when MAP broadcasts the input item to local executions, otherwise it will get a default value. If a local execution has the ask privilege on the output channel \(c\), then REDUCE will actually ask the execution for the real value that it wished to send to \(c\). Otherwise, REDUCE will just replace it with a default value. If a local execution has the tell privilege on the output channel \(c\), it can invoke REDUCE to send the values generated by itself to \(c\).

Notice that an execution may have only one privilege. For example, an execution with the ask but not the tell privilege in \(T_R\) will provide the real value to REDUCE, but will not be able to invoke REDUCE to put the value in the external output. It will have to wait for somebody else with the tell privilege on the channel to produce an output.

### 3 Semantics of Controlled Programs

Our model programming language is close to the one used in the SME paper \[6\]. Valid values in this language are boolean values (T and F) or non-negative integers. A program \(\pi\) is an instruction composed from the terms described in Fig. 2. In this figure, \(\pi\), \(e\), \(x\), and \(c\) are meta-variables for respectively instruc-
Table 2: Labels and their semantics

| Label | Semantics |
|-------|-----------|
| prg   | Program executed by the component |
| mem   | Memory of the component |
| in    | Input queue of the component |
| out   | Output queue of the component |
| top   | Index of the top of the stack |
| stt   | State of a local execution |
| int   | Interrupt signal sent by a local execution |
| tm    | Table $T_M$ |
| tr    | Table $T_R$ |
| map   | MAP component |
| red   | REDUCE component |

tions, expressions, variables, and input/output channels. Since a program is just a sequence of instructions (i.e. a complex instruction itself), we will use program and instruction interchangeably when referring to complex instructions.

We model an input (output) item as a vector and define input (output) of program instances as queues. We use vectors of channel to accommodate forms in which multiple fields are submitted simultaneously but are classified differently (e.g. credit card numbers vs. user names).

**Definition 3.1.** An input vector $\vec{v}$ is a mapping from input channels to their values, $\vec{v} : C_{in} \rightarrow \Sigma \cup \{\bot\}$, where the value $\bot$ is the special undefined value. An output vector $\vec{v}$ is a mapping from output channels to their values, $\vec{v} : C_{out} \rightarrow \Sigma \cup \{\bot\}$.

Given a vector $\vec{v}$ and a channel $c$, the value of the channel is denoted by $\vec{v}[c]$. The symbol $\bot$ denotes an output vector mapping all channels to $\bot$. To simplify the formal presentation, in the sequel w.l.o.g. we assume that each input and output operation only affect one channel at a time. Thus, for each vector, there is only one channel $c$ such that $\vec{v}[c] \neq \bot$.

Let queue $Q$ be a sequence of elements $q_1 \ldots q_n$. We denote the addition of a new element to the queue $Q$ as $Q.q$, or $q_1 \ldots q_n.q$; the removal of the first element from the queue $Q$ is denoted by $q_2 \ldots q_n$. By $\epsilon$ we denote an empty queue.

To define an execution configuration, we use a set of labelled pairs. A labelled pair is composed by a label and an object and in the form $label:object$. The label is attached to the object in order to differentiate this object from others, so each label occurs only once. For example, $tm:T_M$ is the configuration table for MAP. A summary of labels and their semantics used in this report is in Tab. 2.

**Definition 3.2.** An execution configuration of a program is a set $\{prg: \pi, mem: m, in: I, out: O\}$, where $\pi$ is the program to be executed, $m$ is the memory (a function mapping variables to values), $I$ (resp. $O$ respectively) is the queue of input (resp. output) vectors.

The operational semantics of the language is described in Fig. 3. The conclusion part of each semantic rule is written as $\Delta, \Gamma \Rightarrow \Delta, \Gamma'$, where $\Delta$ denotes the
\[
\begin{align*}
\text{ASSG} & : \quad \pi = x := e \quad m(e) = \text{val} \\
\text{COMP} & : \quad \begin{array}{c}
\text{prg} : \pi_1, \text{mem} : m, \text{in} : I, \text{out} : O \to \text{prg} : \pi_1', \text{mem} : m', \text{in} : I', \text{out} : O' \\
\text{prg} : \pi_2, \text{mem} : m, \text{in} : I, \text{out} : O \to \text{prg} : \pi_2', \text{mem} : m', \text{in} : I', \text{out} : O'
\end{array}
\end{align*}
\]

\[
\begin{align*}
\text{IF-T} & : \quad \pi = \text{if } e \text{ then } \pi_1 \text{ else } \pi_2 \quad m(e) = T \\
\text{IF-F} & : \quad \pi = \text{if } e \text{ then } \pi_1 \text{ else } \pi_2 \quad m(e) = F \\
\text{WHIL-T} & : \quad \pi = \text{while } e \text{ do } \pi_{\text{loop}} \quad m(e) = T \\
\text{WHIL-F} & : \quad \pi = \text{while } e \text{ do } \pi_{\text{loop}} \quad m(e) = F \\
\text{SKIP} & : \quad \pi = \text{skip} \\
\text{INP} & : \quad \pi = \text{input } x \text{ from } c \quad I = \vec{v}, I' \quad \vec{v}[c] \neq \bot \\
\text{OUTP} & : \quad \pi = \text{output } e \text{ to } c \quad \vec{v} = \overline{\vec{v}}[c \mapsto m(e)]
\end{align*}
\]

Fig. 3: Semantics of instructions of controlled programs

The semantics of the comma "\(\)," in the expression \(\Delta, \Gamma\) is the disjoint union of \(\Delta\) and \(\Gamma\). We abuse the notation of the memory function \(m(\cdot)\) and use it to evaluate expressions to values. When an output command sends a value to the channel \(c\), an output vector \(\vec{v} = \overline{\vec{v}}[c \mapsto \text{val}]\) is inserted into the output queue, where \(\vec{v}\) is the vector with all undefined channels, except \(c\) that is mapped to \(m(e)\), so \(\vec{v}[c'] = \bot\) for all \(c' \neq c\) and \(\vec{v}[c] = m(e)\).

**Definition 3.3.** An execution of the program \(\pi\) is a finite sequence of configuration transitions \(\gamma_0 \to \gamma_1 \to \ldots \to \gamma_k\), where \(\gamma_0 = \{\text{prg} : \pi, \text{mem} : m_0, \text{in} : I, \text{out} : O\}\) is the initial configuration, \(m_0\) is the function mapping every variable to the initial value, and \(k\) is the number of transitions.

The transition sequence can be also written as \(\gamma_0 \to^{*} \gamma_k\), or \(\gamma_0 \to^{*} \gamma_k\) if the exact number of transitions does not matter, or \((\pi, I, \epsilon) \to^{*} (\pi^k, I^k, O^k)\), where \(\gamma_k = \{\text{prg} : \pi^k, \text{mem} : m^k, \text{in} : I^k, \text{out} : O^k\}\). All sequences have the form

\[
\begin{align*}
\Delta, \text{prg}(\pi), \text{mem}(m) \to \Delta, \text{prg}(\pi'), \text{mem}(m')
\end{align*}
\]
, where \( \text{INST}_1 \) is ASSG, WHIL-F, INP, or OUTP; \( \text{INST}_2 \) is IF-T, IF-F, or WHIL-T; and \( \text{INST}_3 \) is ASSG, INP, OUTP, or SKIP.

An infinite sequence is written as \( \gamma_0 \rightarrow \gamma_1 \rightarrow \ldots \).

**Definition 3.4.** The program terminates if there exists a configuration \( \gamma_f = \{ \text{prg: skip, mem: m, in: } \epsilon, \text{out: O} \} \) such that \( \gamma_0 \rightarrow^* \gamma_f \). We denote this whole derivation sequence by \((\pi, I) \Downarrow O\) using the big step notation.

## 4 Semantics of the Enforcement Mechanism

**Definition 4.1.** A configuration of an enforcement mechanism is a set \( \{ t_m: T_M, t_r: T_R, \text{top: TOP, map: M, red: R, in: } I, \text{out: } O, \bigcup_i \text{LECS}_i \} \), where \( T_M \) and \( T_R \) are configuration tables for respectively MAP and REDUCE, TOP is the index of the top of the stack of configurations of local executions \( EX \), \( M \) and \( R \) are configurations of respectively MAP and REDUCE components, \( I \) and \( O \) are respectively the input and output queues of the enforcement mechanism, and \( \text{LECS}_i \) is the configuration of the \( i \)-th local execution.

We denote the enforcement mechanism on \( \pi \) by \( \text{EM}(\pi) \). For the initial configuration, all local input and output queues will be empty, all local executions will be in the executing state, and skip is the only instruction in MAP and REDUCE programs. The enforcement mechanism is terminated when all local executions, MAP and REDUCE programs are terminated, and the global input queue is consumed completely.

**Definition 4.2.** The enforcement mechanism terminates if there exists a configuration \( \gamma_f = \{ t_m: T_M, t_r: T_R, \text{top: TOP, map: M, red: R, in: } I, \text{out: } O, \bigcup_i \text{LECS}_i \} \) such that \( \gamma_0 \rightarrow^* \gamma_f \), where \( \text{EX}[i].\text{prg: skip} \) for all \( i \), \( \text{map.prg: skip} \), and \( \text{red.prg: skip} \). We denote this whole derivation sequence by \((\text{EM}(\pi), I) \Downarrow O\) using the big step notation.

We now specify the semantics of the enforcement mechanism components: local executions, the programs of MAP and REDUCE. The general approach is that execution of parallel programs is modeled by the interleaving of concurrent atomic instructions [13] so each transition rule either by a local execution, by MAP, or by REDUCE is a step of the enforcement mechanism as a whole.

### 4.1 Local Executions

Each local execution is associated with a unique identifier \( i \), that is its number on the stack \( EX \). A local execution can be in one of the two states: \( \text{E} \) (Executing) or \( \text{S} \) (Sleeping). Initially, the state of all local executions is \( \text{E} \). A local execution moves from \( \text{E} \) to \( \text{S} \) when it has sent an interrupt signal to require an input item
LINP1. \[ \pi = \text{input } x \text{ from } c \quad \Delta, EX[i].prg, EX[i].mem \Rightarrow \Delta, EX[i].prg, EX[i].mem[x \mapsto \text{val}], EX[i].in \]

LINP2. \[ \pi = \text{input } x \text{ from } c \quad \Delta, \}v\text{ from } Q \quad \text{.dequeue}(I, c) = (\text{val}, I') \]

LOUTP. \[ \pi = \text{output } e \text{ to } c \quad \Delta, EX[i].mem = m \Rightarrow \Delta, EX[i].prg, EX[i].out : O \]

Fig. 4: Semantics of the input and output instructions of \( \pi[i] \)

that is not ready in its local input queue, or to signal that it has generated an output item. A local execution moves from \( \text{S} \) to \( \text{E} \) when it is awakened by the \( \text{MAP} \) component (the input item it required is ready) or by the \( \text{REDUCE} \) component (its output item is consumed).

Definition 4.3. An execution configuration of a local execution is a set \( \text{LECS}_i \triangleq \{EX[i].stt, EX[i].int: \text{signal}, EX[i].prg: \pi, EX[i].mem: m, \text{EX}[i].in: I, \text{EX}[i].out: O\} \), where \( \text{EX} \) is the global stack of local execution, \( i \) denotes the \( i \)-th execution, \( \text{stt} \) is the state of the local execution, \( \text{signal} \) is the interrupt signal sent by the local execution, \( \pi \) is an instruction to be executed, \( m \) is the memory, and \( I \) and \( O \) are queues of input and output vectors respectively.

We define the dequeue operator \( \text{deque}(Q, c) \) on a queue \( Q \) and a channel \( c \) that returns \( (\text{val}, Q') \), where the value of \( \text{val} \) is \( \{v \mid c \} \), where \( v \) is the first vector, such that \( \{v \mid c \} \neq \perp, \) and \( Q' \) is obtained by removing \( v \) from \( Q \); otherwise (there is no vector \( v \) in \( Q \), where \( \{v \mid c \} \neq \perp \)), \( \text{val} = \perp \) and \( Q' = Q \).

The semantics of local executions for assignment, composition, if, while, and skip instructions is essentially identical to the one described in Fig. 3. The only difference is the explicit condition that the local state must be \( \text{E} \). We do not present these rules in the paper. We provide the rules for input and output instructions in Fig. 4. When the input instruction is executed and the input item required is in the local input queue, this item will be consumed (rule LINP1). Otherwise, the local execution emits an input interrupt signal \( c \) and moves to the sleep state (rule LINP2). The output interrupt signal \( c \) is generated when the output instruction is executed (rule LOUP).

The initial configuration of the \( i \)-th local execution is \( \{EX[i].stt: \text{E}, EX[i].int: \perp, EX[i].prg: \pi, EX[i].mem: m, EX[i].in : I, EX[i].out : O\} \). A local execution is terminated if there is only the skip instruction to be executed.

4.2 MAP

A MAP program is normally composed of three steps: the input retrieval step, the value distribution step and the wakeup step. In the first step, an input
item is fetched by performing an actual input action from the specified channel, or by using the default value (val_{def}). In the second step, a real input item or the default item is sent to local executions. These two steps depend on the configuration in $T_M$. In the third step, local executions are waken up if a certain condition is satisfied, e.g., these local executions were waiting for input items and they have received the input items they required.

In addition to the instructions in Fig. 2 (except the output instruction that is replaced by the map instruction), the program $\pi_M$ is also composed by the instructions described in Fig. 5, where $PRED[\ ] \triangleq \lambda x.\text{Pred}(x)$ is a meta-variable for predicates. The evaluation of the predicate $PRED[\ ]$ on the configuration of the local execution $\pi[i]$ is denoted as $PRED[i]$. The execution of map, wake, or clone instruction is applied simultaneously to all local executions $\pi[i]$ such that $PRED[i]$ is true as follows. First, the value of the expression $e$ is sent to the input queues of all local executions. The value sent is considered as a value from the channel $c$. Then all local executions $\pi[i]$ are awaken and the interrupt signals generated by those local executions (if there were some) are removed. The execution of the clone instruction clones the configuration of each local execution $\pi[i]$. The new program and the overall configuration will be appended to the local executions stack. The state of the new executions is $S$. The privileges of the new local executions are copied from the lists of privileges $PRIV_{TM}$ and $PRIV_{TR}$. The list $PRIV_{TM}$ (respectively $PRIV_{TR}$) is an input (resp. output) privilege configuration template which varies depending on the enforced property. We give an example of such templates in §5.3, where the enforced property requires cloning.

**Definition 4.4.** A configuration of the MAP component is a set \{map, prg: $\pi_M$, map, mem: m\}, where $\pi_M$ is the instruction to be executed, and $m$ is the memory.

The semantics of instructions of assignment, sequence, if, while, and skip of MAP is almost the same as the semantics presented in Fig. 3. The output instruction is not used in $\pi_M$. The semantics of input and map is described in Fig. 6. For the map, wake, and clone instructions, if there is no $i$ such that $PRED[i]$ holds, then the execution of these instructions makes all local executions move from their current configurations to themselves.

The bijective function $assignIndex() : S \rightarrow \{1, \ldots, |S|\}$ assigns and returns an unique index of the element $i$ in the set $S$ (the index starts from 1). The function $fork(LECS_i, j)$ makes a copy of the local execution $\pi[i]$; the new execution can be referred as $EX[j]$. The function $assign(TM, TR, TOP, TOP', PRIV_{TM}, PRIV_{TR})$
\[
\pi_M = \text{input } x \text{ from } c \quad I = \vec{v}, I' \quad \vec{v}[c] \neq \perp
\]
\[
\Delta, \text{map.prg}; \pi_M, \text{map.mem}; \text{in} I \Rightarrow \Delta, \text{map.prg}; \text{skip}, \text{map.mem}; [x \mapsto \vec{v}[c]], \text{in} I'
\]
\[
\pi_M = \text{map}(e, c, \text{PRED}[i]) \quad S = \{i \in \{0, \ldots, \text{TOP}\} : \text{PRED}[i]\}
\]
\[
\text{LECS} = \bigcup_{i \in S} \{\text{EX}[i], \text{in} I\} \quad \vec{v} = \vec{v} \downarrow [c \mapsto m(e)] \quad \text{LECS}' = \bigcup_{i \in S} \{\text{EX}[i], \text{in} I', \vec{v}\}
\]
\[
\text{MAP} \quad \Delta, \text{map.prg}; \pi_M, \text{LECS} \Rightarrow \Delta, \text{map.prg}; \text{skip}, \text{LECS'}
\]
\[
\pi_M = \text{wake}(\text{PRED}[i]) \quad S = \{i \in \{0, \ldots, \text{TOP}\} : \text{PRED}[i]\}
\]
\[
\text{LECS} = \bigcup_{i \in S} \{\text{EX}[i].\text{int}; \text{signal}, \text{EX}[i].\text{stt}; S\}
\]
\[
\text{LECS}' = \bigcup_{i \in S} \{\text{EX}[i].\text{int}; \perp, \text{EX}[i].\text{stt}; E\}
\]
\[
\text{WAKM} \quad \Delta, \text{map.prg}; \pi_M, \text{LECS} \Rightarrow \Delta, \text{map.prg}; \text{skip}, \text{LECS'}
\]
\[
\pi_M = \text{clone}(\text{PRED}[i], \text{PRIV}_T, \text{PRIV}_R)
\]
\[
S = \{i \in \{0, \ldots, \text{TOP}\} : \text{PRED}[i]\}
\]
\[
\text{LECS} = \bigcup_{i \in S} \text{LECS}_i
\]
\[
\text{LECS}' = \text{LECS} \cup \bigcup_{i \in S} \text{fork}([\text{LECS}_i, \text{TOP} + \text{assignIndex}(i)])
\]
\[
\text{CLON} \quad (T'_M, T'_R) = \text{assign}(T_M, T_R, \text{TOP}', \text{TOP}', \text{PRIV}_T, \text{PRIV}_R)
\]
\[
\Delta, \text{tm}; T_M, \text{tr}; T_R, \text{top}; \text{TOP}, \text{map.prg}; \pi_M, \text{LECS}
\]
\[
\Rightarrow \Delta, \text{tm}; T'_M, \text{tr}; T'_R, \text{top}; \text{TOP}', \text{map.prg}; \text{skip}, \text{LECS}'
\]
\[
\text{MACT} \quad \text{map.prg}; \text{skip} \quad S = \{i \in \{0, \ldots, \text{TOP}\} : \text{WAIT}[i]\}
\]
\[
S \neq \emptyset \quad \pi = \text{pick}(S) \quad \text{EX}[i].\text{prg} = \text{input } x \text{ from } c; \pi
\]
\[
\Delta, \text{EX}[i].\text{int}; c, \text{map.prg}; \text{skip}, \text{map.mem}\n\]
\[
\Rightarrow \Delta, \text{EX}[i].\text{int}; \perp, \text{map.prg}; \pi_M(i, c), \text{map.mem}; \emptyset_0
\]

Fig. 6: Semantics of instructions of MAP

modify tables \(T_M\) and \(T_R\) by adding new columns for the newly cloned processes and the corresponding values for the privileges from \(\text{PRIV}_T\) and \(\text{PRIV}_R\) for the input and output channels for these processes.

The initial configuration of MAP is \(\{\text{map.prg}; \text{skip}, \text{map.mem}; \emptyset_0\}\). The execution of MAP is terminated if skip is the only instruction in the MAP program.

We define the predicate \(\text{WAIT}[i]\) that indicates whether a local execution is waiting for an input item or not. The function \(\text{pick}(S)\) returns an element from the non-empty set \(S\). The selection of an element in a non-empty set \(S\) can be non-deterministic or in the round-robin way.

\[
\text{WAIT}[i] \triangleq \lambda x. \text{EX}[x].\text{stt} = S \land \exists c \in \text{C}_{in} : \text{EX}[x].\text{int} = c \land \text{EX}[x].\text{prg} = \text{input } y \text{ from } c; \pi
\]

The MAP component activation is presented in Fig. 5 (the rule MACT).
\[ \pi_R ::= \ldots \]

\[ \text{retrieve } x \text{ from } (i, c) \text{ retrieve} \]

\[ \text{clean}(c, \text{PRED}[\ ]) \text{ clean} \]

Fig. 7: REDUCE instructions

MAP can be activated when there is only the skip instruction in the MAP program, and there is an interrupt signal \( c \) from the local execution \( \pi[i] \), the state of this local execution is sleeping (S), the instruction to be executed is an input instruction. The activation of MAP on a signal on channel \( c \) from \( \pi[i] \) will remove the signal from configuration of \( \pi[i] \).

4.3 REDUCE

The REDUCE component controls the output actually generated by the enforcement mechanism. A REDUCE program \( \pi_R \) can ask an item from a local execution, send an item to the external output, clean local output queues of local executions and wake local executions up.

Definition 4.5. A configuration of the REDUCE component is a set \( \{ \text{red.prg: } \pi_R, \text{red.mem: } m \} \), where \( \pi_R \) is the instruction to be executed, and \( m \) is the memory.

Except for the input instruction that is replaced by the retrieve instruction, in addition to the instructions in Fig. 3 and the wake instruction, the program of the REDUCE component may contain the instructions described in Fig. 7. The execution of the retrieve instruction reads the value from the output queue of \( \pi[i] \) and stores it into \( x \). The execution of the clean instruction is applied to all local execution \( \pi[i] \) such that \( \text{PRED}[i] \) is true. This instruction removes the first vector \( \vec{v} \) of the output queue \( O \) of \( \pi[i] \), where the value of \( \vec{v}[c] \) is different from \( \perp \).

The semantics of the retrieve, output, wake, and clean instructions is described in Fig. 8 where the function \( \text{remove}(O, c) \) removes the first vector \( \vec{v} \) in \( O \) where \( \vec{v}[c] \neq \perp \).

The initial configuration of REDUCE is \( \{ \text{red.prg: } \text{skip}, \text{red.mem: } m_0 \} \). Similar to the execution of MAP, the execution of REDUCE is terminated if skip is the only instruction in the REDUCE program.

We define the predicate \( \text{WAITO[ ]} \) indicating whether a local execution is sleeping on an output instruction.

\[
\text{WAITO[ ] } \triangleq \lambda x. \text{EX}[x].\text{stt} = \text{S} \land \exists c \in C_{out} : \text{EX}[x].\text{int} = c \land \text{EX}[x].\text{prg} = \text{output } e \text{ to } c; \pi
\]

In Fig. 8 we present the REDUCE activation rule (RACT). Similarly to MAP, REDUCE can be activated when there is only the skip instruction in the REDUCE program, and there is an interrupt signal \( c \) from the local execution \( \pi[i] \), the state of this local execution is sleeping (S), the instruction to be executed is an
\[ \pi_R = \text{retrieve } x \text{ from } (i, c) \]
\[ \Delta, \operatorname{red.prg} \pi_R, \operatorname{red.mem} m \Rightarrow \Delta, \operatorname{red.prg} \text{skip}, \operatorname{red.mem} m[x \mapsto \text{val}] \]

\[ \pi_R = \text{output } e \text{ to } c \quad \text{red.mem} = m \quad \vec{v} = \overrightarrow{c \mapsto m(e)} \]
\[ \Delta, \operatorname{red.prg} \pi_R, \text{out} O \Rightarrow \Delta, \operatorname{red.prg} \text{skip}, \text{out} O \vec{v} \]

\[ \pi_R = \text{wake}([\text{PRED}[]]) \quad S = \{i \in \{0, \ldots, \text{TOP}\} : \text{PRED}[i]\} \]
\[ \text{LECS} = \bigcup_{i \in S} \{\text{EX}[i].\text{int.signal}, \text{EX}[i].\text{stt}S\} \]
\[ \text{LECS}' = \bigcup_{i \in S} \{\text{EX}[i].\text{int} \perp, \text{EX}[i].\text{stt}E\} \]

\[ \Delta, \operatorname{red.prg} \pi_R, \text{LECS} \Rightarrow \Delta, \operatorname{red.prg} \text{skip}, \text{LECS}' \]

\[ \pi_R = \text{clean}(c, [\text{PRED}[]]) \quad S = \{i \in \{0, \ldots, \text{TOP}\} : \text{PRED}[i]\} \]
\[ \text{LECS} = \bigcup_{i \in S} \{\text{EX}[i].\text{out} O\} \quad \text{LECS}' = \bigcup_{i \in S} \{\text{EX}[i].\text{out} \text{remove} O, c\} \]

\[ \Delta, \operatorname{red.prg} \pi_R, \text{LECS} \Rightarrow \Delta, \operatorname{red.prg} \text{skip}, \text{LECS}' \]

\[ \text{red.prg} \text{skip} \quad S = \{i \in \{0, \ldots, \text{TOP}\} : \text{WAITO}[i]\} \quad S \neq \emptyset \]
\[ i = \text{pick}(S) \quad \text{EX}[i].\text{prg} = \text{output } e \text{ to } c; \pi \]
\[ \Delta, \text{EX}[i].\text{int} c; \text{red.prg} \text{skip}, \text{red.mem} m \]
\[ \Rightarrow \Delta, \text{EX}[i].\text{int} \perp; \text{red.prg} \pi_R(i, c), \text{red.mem} m_0 \]

output instruction. The activation of \text{REDUCE} on a signal on channel \( c \) from \( \pi[i] \) will remove the signal from configuration of \( \pi[i] \).

## 5 Configurations for the Selected Properties

In [15], Mantel proposes a uniform framework to define possibilistic information flow properties and he proves that existing possibilistic information flow properties can be expressed as a predefined basic security predicate (BSP) or conjunction of these BSPs. A BSP is generally defined in the framework of Mantel based on removal of some high inputs and events.

In the next sections, we will demonstrate configurations of our framework for enforcement of two BSPs, RI and DI, and the SME-style NI. It might not be obvious whether these properties are actually different in our model. We resolve possible doubts of the attentive reader in Sec. 9.

**Definition 5.1.** Let \( \text{COND}[\vec{v}] \triangleq \lambda \vec{v}.\text{Cond}() \) be a predicate and \( \text{COND}[\vec{v}] \) be the result of the evaluation of \( \text{COND}[\vec{v}] \) on \( \vec{v} \). We define the restriction operator

![Fig. 8: Semantics of instructions of \text{REDUCE}](image-url)
\textbf{Fig. 9: Running Example Program}

on the queue $Q$ with $\text{COND}[]$ as follows:

\[ Q|_{\text{COND}[\ ]} \triangleq \begin{cases} 
\epsilon, & \text{if } Q = \epsilon; \\
\vec{v}.Q'|_{\text{COND}[\ ]}, & \text{if } Q = \vec{v}.Q' \text{ and } \text{COND}[\vec{v}] = T; \\
Q'|_{\text{COND}[\ ]}, & \text{if } Q = \vec{v}.Q' \text{ and } \text{COND}[\vec{v}] = F.
\end{cases} \]

We will use the notation $Q|_l$, the restriction on security level $l$, if $\text{Cond}(l) \triangleq \lambda \vec{v}.\exists c : \vec{v}[c] \neq \bot \land \text{LVL}[c] = l$; and the notation $Q|_c$, the restriction on channel $c$, if $\text{Cond}(c) \triangleq \lambda \vec{v}.\vec{v}[c] \neq \bot$.

In the sequel, we will use the program described in Fig. 9 to illustrate how the enforcement mechanism works for different information flow properties. The program has two high input channels $cH1$, $cH2$, and one high output channel $cH3$. With the execution of instructions at lines 3, 4, 7, and 8, the secret values from $cH1$ (line 1) and $cH2$ (line 8) can influence the value sent to the low output channel $cL3$ (line 10). In addition, the sequences of high input items are affected by the low input (line 7 and 8); for example, if the value of $l1$ is $T$, an input item from $cH2$ will be consumed.

We consider the execution of the program with the input sequence ($cH1 = T$) ($cL1 = F$) ($cL2 = m$) ($cH2 = M$).

### 5.1 Removal of Inputs

The property of removal of inputs \cite{15} requires that if a possible trace is perturbed by removing all high input items, then the result can be corrected into a possible trace.

\[ \forall t \in \text{Tr}. \exists t' \in \text{Tr}. t|_L = t'|_L \land t'|_{H1} = \epsilon \]

In our notation, if all high input items in an input queue are replaced by default items or removed, the input queue can be modified to an input such that the program will be terminated when executing on this input and the output generated will be equivalent at the low level with the original output.

**Definition 5.2.** A program $\pi$ satisfies the property of removal of inputs iff

\[ \forall I, \forall \text{values of } \text{val}_{\text{def}} : (\pi, I) \downarrow O \implies \exists I' : I'|_L = I|_L \land I'|_H = (d')^* \land \land \forall c \in C_{in}, \parallel I'|_c \parallel \leq \parallel I|_c \parallel \land (\pi, I') \downarrow O' \land O'|_L = O|_L, \]
if $a \in T_M[i][c]$ then
input $x$ from $c$
map($x, c, \text{canTell}(c)$)
map(val_{de,f}, c, \neg \text{canTell}(c))
wake(isReady(c))
else
skip

$x := \text{val}_{de,f}$
if $a \in T_R[i][c]$ then
retrieve $x$ from $(i, c)$
if $t \in T_R[i][c]$ then
output $x$ to $c$
clean(c, identical(i))
wake(identical(i))

RI prevents attackers from inferring what high input items have been read, since the removal and the replacement of high input items with fake ones have no effect on what is visible to attackers. Only the low execution in the enforcement mechanism can output to low channels. MAP can perform input actions for all requests from the low execution. The low execution can only receive default values for high input items.

Fig. 10: Configuration for the enforcement mechanism of RI

where the vector $\vec{df}$ contains the default value, and $\|Q\|$ returns the length of $Q$.

The enforcement mechanism of the RI property on the program $\pi$ only needs two parallel programs: the high ($\pi[0]$) and the low ($\pi[1]$). We specify the full configuration of the local executions in Fig. 10. The high execution can receive (real) input values from $L$ and $H$ channels, while the low execution can receive only (real) input values from $L$ channels. The high execution can write output values only to $H$ channels, the low execution can write values only to $L$ channels. If the interrupt signal is from $\pi[1]$, or the interrupt signal is from $\pi[0]$ and the level of channel $c$ is $H$, then the input action will be performed. Otherwise, the local execution keeps sleeping.

The program of MAP is described in Fig. 10a. The function $\text{canTell}(c)$ indicates whether the local execution $\pi[i]$ can receive real values from MAP:

$$\text{canTell}(c) \triangleq \lambda x.t \in T_M[x][c]$$

If a local execution that is sleeping and waiting for an input item from a channel has received the input item required, this local execution is ready to be waken up:

$$\text{isReady}(c) \triangleq \lambda x.\text{EX}[x].\text{stt} = S \land \text{EX}[x].\text{prg} = \text{input } y \text{ from } c; \pi \land \\land \text{EX}[x].\text{in} = I \land \text{dequeue}(I, c) = (\text{val}, I') \land \text{val} \neq \perp$$

When there is an interrupt signal on channel $c$ from $\pi[i]$ on an output instruction, the program REDUCE provided in Fig. 10b is activated. If the local execution $\pi[i]$ can send items to channel $c$ ($T_R[i][c] = 1$), the output action is performed. Otherwise, there is no output action. After that, the output
queue of $\pi[i]$ is cleaned and only $\pi[i]$ is waken. Since the execution of the wake instruction wakes only $\pi[i]$ up, the function $\text{identical}(i)$ is defined as

$$\text{identical}(i) \triangleq \lambda x. x = i$$ (3)

**Example.** We consider the tables $T_M$ and $T_R$ of the enforcement mechanism of RI for the program described in Fig. 9. In Figure 11a we show the $T_M$ instantiation for the given set of channels. Following Fig. 10c on the channels $cH1$ and $cH2$ we assign the “at” permissions for the high execution $\pi[0]$, but only the “a” permission to the low execution $\pi[1]$. We also assign the permission “t” on the low channels $cL1$ and $cL2$ for the high execution $\pi[0]$, while we set “at” for the low execution $\pi[1]$. The table $T_R$ in Fig. 11b is configured similarly, following Fig. 10d.

Examples of executions of the high execution $\pi[0]$ and the low execution $\pi[1]$ are shown in Fig. 12. Here, we assume that the high execution runs faster. At line 1, $\pi[0]$ sends a request to MAP and moves to the state $S$. MAP is activated and the code from line 1 to line 5 in Fig. 10a is executed, since the permission “a” is in $T_M[0][cH1]$. Line 2 reads the value $T$ from the global queue; line 3 sends $T$ to the local input queue of $\pi[0]$, since $\text{canTell}(c)$ returns $T$ with $\pi[0]$; line 4 sends the default value $F$ to the local input queue of $\pi[1]$; line 5 wakes $\pi[0]$ up, since $\text{isReady}(cH1)$ returns $T$ with $\pi[0]$. The high execution $\pi[0]$ is waken up and it continues to execute at line 1. At this time, since there is a value from $cH1$ in the local input queue, the execution of the input instruction follows the rule LINP1. Next, line 2 in Fig. 12a is executed. The high execution moves to the state $S$ and waits for an input item from $cL1$.

The low execution starts executing. The execution of line 1 follows the rule LINP1 since there is an item (with default value) from $cH1$ in the local input queue. The execution of line 2 moves the low execution to the state $S$. MAP is activated, and it consumes $F$ from $cL1$ (line 2), sends $F$ to both local input queues (line 3), and wakes the low execution $\pi[1]$ up (line 5). The execution of line 3 does nothing since there is no local execution that can make $\neg\text{canTell}(cL1)$ be true. After that, the low execution keeps executing.

Because values of $h1$ and $l1$ are respectively $T$ and $F$, the high execution executes instructions at lines 3, 5, 6, 7, 9, and 10. At line 9 the high execution moves to the state $S$ and then REDUCE is activated. The program described in Fig. 10b is executed. Since the permission “at” is in $T_R[0][cH3]$, REDUCE retrieves the value generated by the high execution (line 3), sends the value to the global output queue (line 5), cleans the output queue of $\pi[1]$ (line 6), and wakes the high execution $\pi[0]$ up (line 7).
\begin{verbatim}
1. input h1 from cH1 //Get T from cH1.
2. input l1 from cL1 //Use F read by the public execution.
3. if !h1 then
4.   l1 := !l1 //This instruction is skipped since the value of h1 is T.
5. input l2 from cL2 //Use m read by the public execution.
6. h2 := 0
7. if l1 then
8.   input h2 from cH2 //This instruction is skipped since l1 is F.
9.   output l2 + h2 to cH3 //Send m to cH3.
10. output l2 + h2 to cL3 //The output is ignored.
\end{verbatim}

(a) The high execution π[0]

\begin{verbatim}
1. input h1 from cH1 //The default value (F) is used.
2. input l1 from cL1 //Get F from cL1
3. if !h1 then
4.   l1 := !l1 //Value of l1 is T
5. input l2 from cL2 //Get an input from cL2
6. h2 := 0
7. if l1 then
8.   input h2 from cH2 //A default value (∗) is used.
9.   output l2 + h2 to cH3 //The output is ignored.
10. output l2 + h2 to cL3 //Send ∗+m to cL3.
\end{verbatim}

(b) The low execution π[1]

Fig. 12: Executions of local copies for RI

Since the value of both h1 and l1 is F, the instructions at lines 3, 4, 6, 7, 9 and 10 of the low execution π[1] are executed. At line 3 the low execution moves to the state S and MAP is activated. Because the permission “a” is in T_M[1][cH2], MAP reads M from the global input queue, sends M and a default value (∗) to the local input queues of the high and the low execution respectively, and wakes the low execution up. When executing the output instruction at line 9 the low execution moves to the state S, and REDUCE is activated. Since neither of the permissions “a” and “t” is in T_R[1][cH3], REDUCE does not retrieve any item from the local output queue of the low execution and does not send any value to the global queue. REDUCE cleans the output generated by π[1] and wakes π[1] up. The execution of the output instruction at line 10 is similar to the execution of the output instruction at line 9 of the high execution.

We describe the global input, output queues, and local input, output queues in Fig. 13. The global input queue is consumed completely by the execution of the enforcement mechanism. The values sent to cH3 and cL3 are respectively m and ∗+m. Each column in the table corresponds to an input/output operation. Input and output tables should be read from left to right; columns describe the input/output to each channel at time \( t = 0, t = 1 \), etc.

5.2 Non-Interference

The enforcement mechanism configured in this section mimics the SME-style enforcement of non-interference \cite{6} from Devriese and Piessens, and therefore
The input to MAP:

| Channel | Time | 0 | 1 | 2 | 3 | MAP |
|---------|------|---|---|---|---|-----|
| cH1     | T    | ⊥ | ⊥ | ⊥ |   |     |
| cH2     | ⊥    | ⊥ | ⊥ | ⊥ | M |     |
| cL1     | ⊥    | F | ⊥ | ⊥ |   |     |
| cL2     | ⊥    | ⊥ | m | ⊥ |   |     |

Local Executions:

The high execution \( \pi[0] \):

| The local input: | The local output: |
|------------------|-------------------|
| cH1              | T                 |
| cH2              | ⊥                 |
| cL1              | ⊥                 |
| cL2              | ⊥                 |

The low execution \( \pi[1] \):

| The local input: | The local output: |
|------------------|-------------------|
| cH1              | F                 |
| cH2              | ⊥                 |
| cL1              | ⊥                 |
| cL2              | ⊥                 |

REDUCE \( \Rightarrow \)

| Channel | Time | 0 | 1 | 2 | 3 | 4 | 5 |
|---------|------|---|---|---|---|---|---|
| cH3     | ⊥    | ⊥ | ⊥ | ⊥ | m | ⊥ |   |
| cL3     | ⊥    | ⊥ | ⊥ | m | ⊥ |   |   |

Fig. 13: Example of input and output queues for RI

inherits also the limitations of SME formal guarantees.

Informally, a program satisfies the termination-insensitive non-interference (TINI) property if given two arbitrary inputs that are equivalent at the low level and the executions of the program on these two inputs are terminated, then the outputs generated are indistinguishable to the users at the low level. In other words, the high input items in these two inputs have no effect on what observable is to users at the low level. Termination-sensitive non-interference (TSNI) additionally requires that the secret input items do not influence the termination of the program [3].

**Definition 5.3.** A program \( \pi \) satisfies the property of **termination-insensitive non-interference** iff

\[
\forall I, I': I|_L = I'|_L \implies O'|_L = O|_L,
\]

where \((\pi, I) \downarrow O\) and \((\pi, I') \downarrow O'\).

**Definition 5.4.** A program \( \pi \) satisfies the property of **termination-sensitive non-interference** iff

\[
\forall I, I': I|_L = I'|_L \land (\pi, I) \downarrow O \implies (\pi, I') \downarrow O' \land O'|_L = O|_L
\]
1: if \( a \in T_M[i][c] \) then
2: input \( x \) from \( c \)
3: \( \text{map}(x, c, \text{canTell}(c)) \)
4: \( \text{map}(\text{val}_\text{def}, c, \neg\text{canTell}(c)) \)
5: \( \text{wake}(\text{isReady}(c)) \)
6: else
7: if \( t \notin T_M[i][c] \) then
8: \( \text{map}(\text{val}_\text{def}, c, \text{identical}(i)) \)
9: \( \text{wake}(\text{identical}(i)) \)
10: else
11: skip

(a) MAP for SME for input from \( c \) requested from \( \pi[i] \)

1: \( x := \text{val}_\text{def} \)
2: if \( a \in T_R[i][c] \) then
3: \( \text{retrieve} \ x \ from \ (i, c) \)
4: if \( t \in T_R[i][c] \) then
5: \( \text{output} \ x \ to \ c \)
6: \( \text{clean}(c, \text{identical}(i)) \)
7: \( \text{wake}(\text{identical}(i)) \)

(b) REDUCE for SME for an output to \( c \) from \( \pi[i] \)

\[
\begin{array}{|c|c|c|}
\hline
\text{LVL}_c & \pi[0] & \pi[1] \\
\hline
H & at & - \\
L & t & at \\
\hline
\end{array}
\]

(c) \( T_M \)

\[
\begin{array}{|c|c|c|}
\hline
\text{LVL}_c & \pi[0] & \pi[1] \\
\hline
H & at & - \\
L & - & at \\
\hline
\end{array}
\]

(d) \( T_R \)

NI prevents attackers from inferring high input items, since all executions on inputs that are low-equivalent will generate low-equivalent outputs. The low execution \( \pi[1] \) cannot ask values from high input channels or be told real value from these channels. MAP will not perform any input actions on requests for high inputs items from the low execution. \( T_R \) and the program of REDUCE are the same as in the enforcement mechanism of RI.

Fig. 14: Configuration for the enforcement mechanism of NI

To implement the SME approach [6], we use the following configuration. The high execution \( \pi[0] \) can only read high input items, but it can consume both high and low ones. For low input items this local execution needs to wait for the values read by the low execution \( \pi[1] \). The low execution \( \pi[1] \) can read and consume only low items. If the low execution requires a high input item, the default value will be used.

The configuration tables \( T_M \) and \( T_R \) and the program for MAP, and REDUCE to enforce the SME-style NI are presented in Fig. 14. Compared to the program for MAP in the enforcement mechanism of RI, the program for MAP is different, as shown in Fig. 14a. The functions \( \text{canTell}(c) \), \( \text{isReady}(c) \) and \( \text{identical}(i) \) are defined in respectively Eq. 1, 2 and 3 in § 5.1.

**Example.** The contents of the tables \( T_M \) and \( T_R \) for the enforcement mechanism of NI for the running example program in Fig. 9 follow the patterns described in Fig. 14c and Fig. 14d respectively.

The executions of the high execution and the low execution are described in Fig. 15. The execution of the high program is similar to the execution of the high program in RI. The execution of the low execution is almost the same as the execution of the low execution in RI, except for handling the input instruction at line 8.

When the input instruction at line 8 is executed, the low execution moves to the state S and sends a signal to MAP. When MAP is activated on this
input h1 from cH1 //Get T from cH1.
input l1 from cL1 //Use F read by the low execution.
if !h1 then
  l1 := !l1 //This instruction is skipped since the value of h1 is T.
input l2 from cL2 //Use m read by the low execution.
h2 := 0
if l1 then
  input h2 from cH2 //This instruction is skipped since l1 is F.
output l2 + h2 to cH3 //Send m to cH3.
output l2 + h2 to cL3 //The output is ignored.

(a) The high execution π[0]

input h1 from cH1 //A default value is used.
input l1 from cL1 //Get F from cL1
if !h1 then
  l1 := !l1
input l2 from cL2 //Get an input from cL2
h2 := 0
if l1 then
  input h2 from cH2 //A default value is used.
output l2 + h2 to cH3 //The output is ignored.
output l2 + h2 to cL3 //Send * + m to cL3.

(b) The low execution π[1]

When the low execution π[1] asks MAP an item from cH2, MAP does not perform any input operation and sends a default value to the local input queue of the low execution

Fig. 15: Executions of local copies for NI

signal, the instructions at lines 1, 7, 8, 9 in the program described in Fig. 14a are executed. MAP sends a default value to the local input queue of the low execution (line 5), and wakes this local execution up (line 9).

We describe the global input, output queues, and local input, output queues in Fig. 16. Compared to the execution of the enforcement mechanism of RI, the execution of the enforcement of NI consumes only three input items. The fourth input item is kept in the figure for the illustrative purposes and in order to make a comparison with the enforcement of RI. The local input queue of the high execution contains only three input items; these are two low input items requested by the low execution and one high input item requested by the high execution. The local input queue of the low execution π[1] contains four input items, where the last one is the default item generated and sent by MAP.

5.3 Deletion of Inputs

The property of deletion of inputs (DI) requires that if we perturb a possible trace t (where \( t = \beta.e.\alpha \) and there is no high input event in \( \alpha \)) by deleting the high input event \( e \), then the result can be corrected into a possible trace \( t' = \beta'.\alpha' \). The parts \( \beta \) and \( \beta' \) are equivalent on the low input events and the high input events. In other words, the low input events and the high input events in \( \beta \) and \( \beta' \) must be the same. The parts \( \alpha \) and \( \alpha' \) are also equivalent on
The input to MAP:

(The last input item is not consumed.)

| Channel | Time | 0 | 1 | 2 | 3 |
|---------|------|---|---|---|---|
| cH1     | T    | ⊥ | ⊥ | ⊥ | ⊥ |
| cH2     | ⊥    | ⊥ | ⊥ | M | ⊥ |
| cL1     | ⊥    | F | ⊥ | ⊥ | ⊥ |
| cL2     | ⊥    | ⊥ | m | ⊥ | ⊥ |

MAP

Local Executions:

The high execution π[0]:

| Channel | Time | 0 | 1 | 2 | 3 |
|---------|------|---|---|---|---|
| cH1     | T    | ⊥ | ⊥ | ⊥ | ⊥ |
| cH2     | ⊥    | ⊥ | ⊥ | ⊥ | ⊥ |
| cL1     | ⊥    | F | ⊥ | ⊥ | ⊥ |
| cL2     | ⊥    | ⊥ | m | ⊥ | ⊥ |

The local input: The local output:

The low execution π[1]:

| Channel | Time | 0 | 1 | 2 | 3 |
|---------|------|---|---|---|---|
| cH1     | F    | ⊥ | ⊥ | ⊥ | ⊥ |
| cH2     | ⊥    | ⊥ | ⊥ | * | ⊥ |
| cL1     | ⊥    | F | ⊥ | ⊥ | ⊥ |
| cL2     | ⊥    | ⊥ | m | ⊥ | ⊥ |

The local input: The local output:

REDUCE

The output by REDUCE:

| Channel | Time | 0 | 1 | 2 | 3 | 4 | 5 |
|---------|------|---|---|---|---|---|---|
| cH3     | ⊥    | ⊥ | ⊥ | ⊥ | m | ⊥ | ⊥ |
| cL3     | ⊥    | ⊥ | ⊥ | ⊥ | ⊥ | ⊥ | *+m|

Fig. 16: Example of input and output queues for NI

the low events and the high input events. Since there is no high input events in \( \alpha \), there is also no high input events in \( \alpha' \).

\[
\forall t \in T, \forall \alpha, \beta \in E^*, \forall e \in E, (e \in HI \land t = \beta.e.\alpha \land \alpha|_{HI} = e) \implies (\exists t' \in T, t'|L = t'|L \land t' = \beta'.\alpha' \land \alpha'|_{LIHI} = \alpha|_{LIHI} \land \beta'|_{LIHI} = \beta|_{LIHI})
\]

In our notation, if we have an input queue \( I = I_1, \vec{v}, I_2 \), where \( \vec{v} \) contains a value from a high channel and in \( I_2 \) there are either no high input items or only high input items with default values, then this input queue can be changed by replacing \( \vec{v} \) by the default vector. The obtained input queue can be sanitized by removing existing default high input items in \( I_2 \) or adding other default high input items to \( I_2 \). The sanitized queue can be consumed completely by a clone of the original program and the output should still be equivalent at the low level to the original output generated with the input \( I \).
A program $\pi$ satisfies the property of deletion of inputs $\text{DI}$ iff

$$\forall I, \forall \text{ values of } \text{val}_{df}: I = I_1 \vec{v} I_2 \land LVL[c] = H \land I_2 | H = (\vec{d}f)^* \land (\pi, I) \Downarrow O$$

$$\implies \exists I': I' = I_1' I_2' \land I'_L = I_L \land I_2' | H = (\vec{d}f)^* \land (\pi, I') \Downarrow O' \land O'| L = O_L,$$

where $\vec{v}[c] \neq \bot$ and the vector $\vec{d}f$ contains a default value.

DI is enforced with the idea that whenever the high execution requests a high input item, the high execution will be cloned and the clone can only receive default values for high input items. When receiving a request from the low execution for a high input item, MAP will return the default value. The program of REDUCE is the same as in the enforcement mechanism of RI.

**Definition 5.5.** A program $\pi$ satisfies the property of deletion of inputs $\text{DI}$ iff

$$\forall I, \forall \text{ values of } \text{val}_{df}: I = I_1 \vec{v} I_2 \land LVL[c] = H \land I_2 | H = (\vec{d}f)^* \land (\pi, I) \Downarrow O$$

$$\implies \exists I': I' = I_1' I_2' \land I'_L = I_L \land I_2' | H = (\vec{d}f)^* \land (\pi, I') \Downarrow O' \land O'| L = O_L,$$

where $\vec{v}[c] \neq \bot$ and the vector $\vec{d}f$ contains a default value.

DI is enforced with the idea that whenever the high execution requests a high input item, this execution will be cloned and the clone will not receive real values from high channels. Components configured to implement the enforcement mechanism of DI are presented in Fig. 17. The program of REDUCE is identical to the program used in the enforcement mechanism of RI.

The enforcement mechanism of DI requires more than two local executions. Only the high execution $\pi[0]$ can ask for and get the high input items, other local executions will only use default values. Each time the high execution is cloned the new execution is inserted into the stack of local executions. The configuration of the clones for input (respectively, output) is presented in Fig. 17(c) (respectively, 17(d)) in the column $\pi[i] > 1$; this is the privilege configuration template $\text{PRIV}_{T_M}$ ($\text{PRIV}_{T_R}$, respectively). In addition, only the low execution
\[ \pi[0], \pi[1], \pi[2] \]

\[
\begin{array}{ccc}
\text{ch1} & \text{at} & a & a \\
\text{ch2} & \text{at} & a & a \\
\text{cl1} & t & at & t \\
\text{cl2} & t & at & t \\
\end{array}
\]

(a) \( T_M \)

\[
\begin{array}{ccc}
\pi[0] & \pi[1] & \pi[2] \\
\text{ch3} & \text{at} & - & - \\
\text{cl3} & - & at & - \\
\end{array}
\]

(b) \( T_R \)

Fig. 18: Example tables \( T_M \) and \( T_R \) for DI

\( \pi[1] \) can ask for low input items and generate low output items; other local executions will reuse the low input items retrieved by the low execution.

**Example.** Fig. 18 depicts \( T_M \) and \( T_R \) of the DI enforcement mechanism for the program described in Fig. 9 that are instances of the tables described in Fig. 14c and Fig. 14d respectively. When the enforcement mechanism starts executing, there are only two columns (\( \pi[0] \) and \( \pi[1] \)) in each table. The third column is appended when the corresponding local execution is created. Following Fig. 17c, the new execution has the “a” permission on high input channels (ch1 and ch2) and the “t” permission on low input channels (cl1 and cl2). The permissions of the new local execution on output channels are configured in a similar way from the column \( \pi[i] > 1 \) in Fig. 17d.

The executions of local executions are described in Fig. 19. When line 1 of the high program is executed, the high execution moves to the state S: the program of MAP in Fig. 17a is activated (the contents of PRIV\( T_M \) and PRIV\( T_R \) used at line 2 are from the columns \( \pi[1] > 1 \) in Fig. 17c and Fig. 17d respectively). Line 2 creates a new clone of \( \pi[0] \), which is referred to as \( \pi[2] \). After that, MAP consumes T from the global input queue (line 5), sends T to the local input queue of the high execution \( \pi[0] \) (line 6), broadcasts F to the local input queues of \( \pi[1] \) and \( \pi[2] \) (line 7), and wakes \( \pi[0] \) and \( \pi[2] \) up (line 8).

When line 2 of \( \pi[0] \) is executed, the high execution moves to the state S and waits for the corresponding input item to be requested by the low execution. After the low execution executes the input instruction at line 2 and F is received from cl1, the high execution is waken up. Next, the instructions at lines 3, 5, 7, 9, and 10 are executed.

The execution of the low execution \( \pi[1] \) is the same as the execution of the low program in NI. The execution of \( \pi[2] \) follows the same pattern as the execution of \( \pi[1] \), with the only difference that also the result of the output instruction at line 10 is ignored by REDUCE.

The input consumed and the output generated by the enforcement mechanism, the local input and output queues of the high execution \( \pi[0] \) and the low execution \( \pi[1] \) are the same as the ones in the enforcement mechanism of NI in Fig. 16. The local input and output queues of the other local execution \( \pi[2] \) are the same as respectively the input and output queues of the low execution.
1. input h1 from cH1 //Get T from cH1.
2. if !h1 then
3.  l1 := !l1 //This instruction is skipped since the value of h1 is T.
4. input l2 from cL2 //Use m read by the low execution.
5. h2 := 0
6. if l1 then
7.  input h2 from cH2 //This instruction is skipped since l1 is F.
8. output l2 + h2 to cH3 //Send m to cH3.
9. output l2 + h2 to cL3 //The output is ignored.

(a) The high execution \( \pi[0] \)

1. input h1 from cH1 //A default value is used.
2. input l1 from cL1 //Use F read by the low execution.
3. if !h1 then
4.  l1 := !l1
5. input l2 from cL2 //Get an input from cL2
6. h2 := 0
7. if l1 then
8.  input h2 from cH2 //A default value is used.
9. output l2 + h2 to cH3 //The output is ignored.
10. output l2 + h2 to cL3 //Send * + m to cL3.

(b) The low execution \( \pi[1] \)

1. input h1 from cH1 //The default value (F) is used.
2. input l1 from cL1 //Use F read by the public execution.
3. if !h1 then
4.  l1 := !l1
5. input l2 from cL2 //Use m read by the public execution.
6. h2 := 0
7. if l1 then
8.  input h2 from cH2 //A default value is used.
9. output l2 + h2 to cH3 //The output is ignored.
10. output l2 + h2 to cL3 //The output is ignored.

(c) The other execution \( \pi[2] \)

The execution \( \pi[2] \) is created when the high execution requests the first high input item. When the low execution \( \pi[1] \) (or the other execution \( \pi[2] \)) asks MAP for an item from cH2, MAP does not perform any input operation, but it sends a default value to the local input queue of the low execution (respectively, the other local execution).

Fig. 19: Executions of local copies for DI

6 Soundness

In this section we formalize the soundness property of an enforcement mechanism, and postulate the theorem on the security guarantees that the enforcement mechanisms configured earlier ensure with respect to the corresponding properties.

Definition 6.1. *An enforcement mechanism is sound with respect to a property*
For all programs $\pi$ the enforcement mechanism executed on $\pi$ satisfies $P$.

**Theorem 6.1** (Soundness of Enforcement). Each enforcement mechanism in Tab. 1 is sound with respect to the corresponding property, except for TSNI.

In order to prove soundness, we state two basic properties specifying the behaviour of MAP on receiving requests for low input items and the behaviour of REDUCE when receiving an output request from a local execution. For the actual proof of the theorem, we perform a case-based reasoning showing that at the end, the output is what we expect. In this respect an important assumption is that the program to be enforced is deterministic. For RI, we need an additional preliminary property showing the relationship between the execution of a controlled program and the corresponding local execution. For DI, we need another preliminary property about the input items that can be consumed by $\pi[i]$ where $i > 1$. Figure 20 sketches the proof strategy for soundness.

We first prove the soundness theorem for NI. To this extend, we first need two simple propositions on the I/O behaviour of the enforcement components.

**Proposition 6.1** (Input items consumed by enforcement mechanisms and input items sent to local input queues of local executions). Consider the enforcement mechanisms of information flow properties, it follows that:

- MAP will only ask low input items from the environment for low input requests from the low execution. The low execution can only receive default values for high input items. This local execution can receive real values for low input items.
- For the enforcement mechanism of NI and DI, MAP will only ask high input items from the environment for high input requests from the high execution.
- For the enforcement mechanism of RI, MAP will ask high input items from the environment for high input request from any local execution.
- The high execution can receive real values for low and high input items.
Proof. The proposition is obvious from the configurations of the corresponding enforcement mechanisms, where all input items in local input queues are sent by MAP; and only MAP can get input items from the environment.

The proposition is proven by using the induction technique on the number of times of activation of MAP on input requests from local executions. Let $k$ be the number of times of activation of MAP on the input request.

Base case: $k = 0$. The proposition holds vacuously.

Induction hypothesis: Assume that the proposition holds for the case that $k < n$. We now prove that the proposition holds for $k = n$. We consider the $n$-th activation of MAP on a request from $\pi[i]$ on channel $c$. The following holds:

- Each instruction of MAP, REDUCE, and local executions is executed atomically,
- The execution of the MAP program does not interfere with the execution of the REDUCE program and vice-versa,
- The execution of a local execution does not interfere with the execution of the MAP (REDUCE) program,

Therefore, we have:

- Case 1: $i = 0$
  - Case 1.1: $LV L[c] = L$: For RI, the instructions at lines 1 and 7 in Fig. 10a are executed. For NI, the instructions at lines 1 and 11 in Fig. 14a are executed. For DI, the instructions at lines 1, 3 and 13 in Fig. 17a are executed. MAP does not perform any input action. This activation does not influence the items received by the low execution.
  - Case 1.2: $LV L[c] = H$: For RI, the instructions from line 1 to 5 in Fig. 10a are executed. For NI, the instructions from line 1 to 5 in Fig. 14a are executed. For DI, the instructions from line 1 to 8 in Fig. 17a are executed. MAP performs an input action and sends a default value to the local input queue of the low execution, and the real value to the local input queue of the high execution.

- Case 2: $i = 1$.
  - Case 2.1: $LV L[c] = L$: The instructions executed are the same as the ones in Case 1.2, except for the clone instruction at line 2 in Fig. 17a that is not executed. The real value is sent to the local input queues of $\pi[1]$ and $\pi[0]$.
  - Case 2.2: $LV L[c] = H$: We check the instructions of the corresponding MAP programs. MAP does not perform an input action on low channels in this case. For NI, (respectively DI), the default value is sent to the local input queue of $\pi[1]$ by the execution of the instruction at line 8 in Fig. 14a (resp. line 10 in Fig. 17a). For RI, an input operation is performed (line 2 in Fig. 10a). However, a default value is sent to the local input queue of $\pi[1]$ (line 3), while the real value is sent to the local input queue of $\pi[0]$ (line 5).
• Case 3: \( i > 1 \) (only for the enforcement mechanism of DI)
  
  - Case 3.1: \( LVL[c] = L \): MAP does not perform any input actions. MAP does not send any input item to the local input queue (line 10 in Fig. 17a).
  
  - Case 3.2: \( LVL[c] = H \): MAP will send only a default input item to the local input queue of \( \pi[i] \) (line 10 in Fig. 17a).

  The proposition holds for \( k = n \). Therefore, the proposition holds for all \( k \geq 0 \).

**Proposition 6.2** (Outputs of enforcement mechanisms). Concerning the output of an enforcement mechanism for an information flow property, it follows that:

- For the enforcement mechanism of RI, NI, and DI, only the high execution \( \pi[0] \) sends output items to high output channels.
- For the enforcement mechanism of RI, NI, and DI, only the low execution \( \pi[1] \) can send output items to low output channels.
- For the enforcement mechanism of DI, the output items generated by the local execution \( \pi[i] \) with \( i > 1 \) are ignored.

**Proof.** The proposition is proven by using the induction technique on the number of times of activation of REDUCE on output requests from local executions. The proof is similar to the proof of Prop. 6.1.

Now we proceed to the proof of soundness of the enforcement mechanism for NI.

**Proof of Theorem 6.1 for NI.** Let us consider two executions: \( \langle EM(\pi), I \rangle \Downarrow O \) and \( \langle EM(\pi), I' \rangle \Downarrow O' \), where \( I|_L = I'|_L \).

The following holds:

1. The low input items consumed by the enforcement mechanism depends only on the low execution (by Prop. 6.1).
2. The low executions in the runs of the enforcement mechanism on \( I \) and \( I' \) always consume default values for high input items (by Prop 6.1).
3. The low executions in these two runs consume the same low input items and same high output items. (By 1, 2 and \( \pi \) be deterministic).
4. These low executions generate the same outputs (By 3 and the fact that \( \pi \) is deterministic).
5. The output items sent to low output channels are always generated by the low executions (by Prop 6.2).
6. \( O|_L = O'|_L \) (by 4 and 5).

This concludes the proof.

For the proof of the soundness of the enforcement mechanism for RI, we need an property stating the relationship between the controlled program and a local execution. We also need another simple property showing how MAP handles the high input requests from local executions.
Proposition 6.3 (Controlled programs and local executions). Let $I_1$ and $I_2$ be two input queues, such that for all input channels $c$, $I_1|_c = I_2|_c$. Then we have:

for all programs $\pi$,

$$\forall I: (\pi, I_1, \epsilon) \rightarrow^k (\pi_k, I_{1k}, O_k) \implies \forall I: \forall c \in C_{in}: I_1|_c = I_2|_c : (\pi, I_2, \epsilon) \rightarrow^k (\pi, I_{2k}, O_k)$$

and $I_{1k}|_c = I_{2k}|_c$ for all $c$.

And we have:

$$\forall I: (\pi, I_1, \epsilon) \rightarrow^k (\pi_k, I_{1k}, O_k) \implies \exists I: \forall c \in C_{in}: I_1|_c = I_2|_c : (\pi, I_2, \epsilon) \rightarrow^k (\pi, I_{2k}, O_k)$$

and $I_{1k}|_c = I_{2k}|_c$ for all $c$.

**Proof.** The proposition is proven by using the induction technique on $k$ and the length of the input queue $I_1$, along with the fact that controlled programs and the local executions are deterministic.

Next, we prove the soundness of the enforcement mechanism for RI.

**Proof of Theorem 6.1 for RI.** Let $I_{rc}^1$ be the input consumed by the low execution in the run $(\text{EM}(\pi), I) \Downarrow O$, and $k$ be the number of high input items in $I$.

**Base case:** $k = 0$. The theorem holds for RI (in this case $I' = I$).

**Induction hypothesis:** Assume that the theorem holds for $k < n$ for RI.

We now prove that the theorem holds for $k = n$. The following holds:

1. $I_{rc}|_L = I|_L$ (by Prop. 6.1).
2. $I_{rc}|_H = (\vec{df})^*$ (by Prop. 6.1).
3. There exists $I^*$ such that $(\pi, I^*) \Downarrow O^*$, and $I^*|_c = I_{rc}|_c$ for all $c$ (by Prop. 6.3).
4. $I^*|_L = I_{rc}|_L$ (by [3], Prop. 6.1 and the fact that $\pi$ is deterministic).
5. $I^*|_L = I|_L$ (by [1] and [3]).

If we used $I^*$ as an input for the enforcement mechanism and the high execution is run only after the low execution is terminated:

6. The low execution will consume all input items in $I^*$ and is not stuck (by Prop. 6.1).
7. Both the high and the low executions will consume with the same input (by [2] and [9] and Prop. 6.1).
8. Both the high and the low execution are terminated (by [6] and [7]).
9. The output items are generated by the low execution (by Prop. 6.2).

From [4], [8] and [9], we have there exists $I^*$, such that $(\text{EM}(\pi), I^*) \Downarrow O^*$ and $O^*|_L = O|_L$. Let $I \triangleq I^*$, it follows that the theorem for the enforcement mechanism of RI holds for the case $k = n$. Thus, the theorem holds for RI.

To prove the soundness of DI, we need a proposition showing the influence of local execution $\pi[i]$ (with $i > 1$) on the input consumed by the enforcement mechanism.

27
Proposition 6.4. For the enforcement mechanism of DI, a local execution $\pi[i]$ with $i > 1$ has no effect on the input consumed by the enforcement mechanism.

Proof. The proof is obvious from the configuration of the enforcement mechanism.

Proof of Theorem 6.1 for DI. The idea of the enforcement mechanism of DI is that when the high execution requests a high input item, the high execution will be duplicated and the newly duplicated execution will receive the default values for high input items. If we replace the last high input item in the original input $I$ with a default item, then there exists another input queue satisfying the definition of DI. Such an input queue is the input consumed by $\pi[\text{TOP}]$.

Let $I$ be an input, such that $(\text{EM}(\pi), I) \Downarrow O$. The proof of soundness of the enforcement mechanism of DI is based on the induction technique on the number of high input item in $I$.

Base case: If there is no high input item in $I$, the theorem holds vacuously.

Induction Hypothesis: The theorem holds for all $I$, such that the number of high input items is smaller than $n$. We now prove that the theorem also holds for the case when the number of high input items is equal to $n$. Now $I$ can be written as $I_1, v_1, \ldots, I_n, v_n, I_{n+1}$.

Based on the configuration of the enforcement mechanism, $\pi[\text{TOP}]$ is created when the high execution requests the last high input item. Let $I^*_{\text{TOP}}$ be the input consumed by $\pi[\text{TOP}]$, $I^*_L$ be the input consumed by $\pi[1]$. We have:

1. $I^*_\text{TOP} = I_1, v_1, \ldots, I_n, \bar{d}f, I'_n, I_{n+1}$, where $I'_n, I_{n+1} = (\bar{d}f)^*$.
2. $I^*_L = I^*_L$.

Let $I^*$ be an input queue, such that $I^* = I_1, \ldots, I_n, v_1, \ldots, v_{n-1}, \bar{d}f, I^*_{n+1}$, where $I^*_{n+1} = I^*_{n+1}$. Assume that the order of executing local executions is first $\pi[1]$, then $\pi[0]$. We have:

3. $I^*_L = I^*_L$.
4. The low execution will consume the part $I_1, \ldots, I_n, I_{n+1}$ for low input items and default values for high input items (by Prop 6.1).
5. The high execution $\pi[0]$ will consume $v_1, \ldots, v_{n-1}, \bar{d}f, I^*_{n+1}$ (by 4 and Prop 6.3).
6. For every $i$, such that $1 < i \leq \text{TOP}$, the execution of the local execution $\pi[i]$ is terminated and it does not effect the input consumed by the enforcement mechanism (by the assumption that $(\text{EM}(\pi), I) \Downarrow O$ and Prop. 6.4).

7. $I^*$ is consumed completely by the enforcement mechanism (by 3 and 5).
8. The high execution is terminated (by the assumption that $(\text{EM}(\pi), I) \Downarrow O$).
9. $(\text{EM}(\pi), I^*) \Downarrow O^*$ (by 3, 7, 8).
10. $O^*_{\text{L}} = O_{\text{L}}$ (by Prop 6.2).

From 5, 8 and 10, the theorem holds for the case of the number of high input item in $I$ is $n$. Therefore, the theorem holds for the enforcement mechanism of DI.

□
7 Precision

The notion of precision for enforcement of a property is taken from [6, 8]. The intuition is that the enforcement mechanism does not change the visible behavior of a program that is already secure with respect to the chosen property (and in particular each I/O on specific channels). Devriese and Piessens separated by construction the input queues of each channel. Since in our formulation the channels are merged into a global stream, our definition of precision must make explicit that the partial order of input items on a channel is preserved. This observation applies also to the order of output items in output queues. In our framework, the local executions are executed in parallel with no specific order. Therefore, the total order of input items consumed by the enforcement mechanism can be different from the total order of input items in the input queue consumed by the controlled program that already obeys the desired property. However, the partial order of input items on a channel is preserved. This observation applies also to the order of output items in output queues.

**Definition 7.1.** An enforcement mechanism is precise with respect to a property, if for any program \( \pi \) that satisfies the property, and for every input \( I \), where \( (\pi, I) \Downarrow O \), regardless of the order of executing local executions, the input \( I^* \) and \( O^* \) of the enforcement mechanism will be such that \( I^*|_c = I|_c \), \( O^*|_c = O|_c \) for every channel \( c \), and \( (EM(\pi), I^*) \Downarrow O^* \).

**Theorem 7.1** (Precision of Enforcement). Each enforcement mechanism in Tab. 7 is precise with respect to the corresponding property, except for TINI.

Figure 21 shows the proof strategy for precision. The proof of precision is more complex than the proof of soundness. At first, we need to prove a number of simple properties on the correct handling of interrupt signals and the
equivalence between the semantics of controlled programs and the semantics of local executions.

**Proposition 7.1** (Local executions and local input queues). For a local execution, when the input instruction is executed, if the input item required is in its local input queue, this item will be consumed. Otherwise, an interrupt signal is generated.

*Proof.* Proof follows obviously from the semantics of local executions. 

**Proposition 7.2** (The wake of local executions). The following facts hold:

1. If a local execution is sleeping on an input instruction that required an input item from the channel \(c\), this local execution will be waken up when the input item is ready and the instruction of \(\pi_M\) executed is the wake instruction. In addition, when a local execution is awaken, there is no interrupt signal in its configuration.

2. A local execution is not awakened when the input item required is not ready or when the input item required is ready, but the instruction executed of \(\pi_M\) is not the wake instruction.

*Proof.* Proof follows by induction on the length of the derivation sequence of the enforcement mechanism.

Next we show that from \(\pi[0]\)'s input, we can reconstruct the original global input.

**Proposition 7.3** (Global input and local inputs). Let \(k\) be the number steps of derivation of the execution of the enforcement mechanism of RI, DI, or NI. Assume that we have \((EM(\pi), I, \epsilon) \Rightarrow^k (EM(\pi), I_k, O_k)\), and \(I^0_{rc}\) is the queue of the input items that have been received by \(\pi[0]\), then it follows that:

- \(I^0_{rc}.I_k = I\)

*Proof.* The lemma is proven by using the induction technique on the length of the global input queue and the length of the derivation sequence of the enforcement mechanism, along with the fact that the execution of the controlled program and the executions of local executions are deterministic.

At this point, we have all that is needed to present the key lemma for the proof of precision for NI that shows that all inputs have been processed and there is nothing left within the enforcement mechanism.

**Lemma 7.1** (Inputs of a controlled program and inputs consumed by the corresponding enforcement mechanism). Let \(\pi\) be a program satisfying TSNI and \((\pi, I) \Downarrow O\). Regardless of the order of executing local executions, if the low execution consumes the same low input items as in \(I\), and the high execution consumes high input and low input items as in \(I\), then it follows that the execution of the enforcement mechanism is terminated, and the input consumed by the enforcement mechanism is \(I^*\), where \(I^*|c = I|c\) for all \(c\).
Proof. The proof of this lemma is based on the proposition of equivalence between semantics of controlled programs and semantics of local executions (Prop. [6.3]) and the proposition of the relationships between the global input queue and local input queues (Prop. [7.3]).

According to the semantics of the enforcement mechanism of NI, the high execution does not influence the termination of the low execution, the input consumed and the output generated by the low execution. Therefore, regardless of the order of executing local executions, if the low execution consumes the same low input items as in \( I \), then the input consumed by the low execution is \( I | L \).

We next prove that \( I_a \neq \epsilon \) and the low execution is terminated.

- Assume that \( I_a \neq \epsilon \). This means there exists an input \( I' \), where \( I'|_L = I|_L, I_a \) and \( I'|_H = (\vec{df})^* \), and \( (\pi, I') \rightarrow \ldots \). Since \( \pi \) satisfies TSNI, this case cannot happen.

- Assume that \( \pi[1] \) is not terminated. However, this leads to the conclusion that \( \pi \) does not satisfy TSNI.

We now prove that the high execution is also terminated and does not request any high input item that is not in \( I \).

- Case 1: Assume that the high execution is stuck on a request for low input items. If the high input execution needs a low input item, the enforcement mechanism will behave accordingly to Prop. [7.1] and Prop. [7.2]. The high execution is stuck on low input items when it requests for an input item that is never requested by the low execution. Since the low input items consumed by the low execution is \( I|_L \), the stuck of the high execution leads to the conclusion that \( \pi \) is non-deterministic.

- Case 2: The high execution requests a high input items that is not in \( I \). Regarding this assumption, because of Prop. [7.3] there are two instances of \( \pi \) that consume some input items, but at some point run in different paths of execution. In other words, \( \pi \) is non-deterministic.

- Case 3: The high execution receives all input items it needs, but is in an infinite loop. This case also leads to the conclusion that \( \pi \) is non-deterministic.

Therefore both local executions are terminated. Let \( I'_0 \) be the input queue received by \( \pi[0] \). Since \( \pi[0] \) does not request any other input items that are not in \( I \), then \( I'_0|_c = I|_c \). From Prop. [7.3] we have \( I^* = I'_0 \). Thus \( I^*|_c = I|_c \) and \((EM(\pi), I^*) \Downarrow O^*\).

We have now all that is needed for the main theorem.

**Proof of Theorem [7.1] for NI.** Let \( I \) be an input queue, such that \((\pi, I) \Downarrow O\). We need to prove that regardless of the order of executing local execution, the input \( I^* \) and output \( O_j \) will be such that \( I^*|_c = I|_c, O^*|_c = O|_c \), and \((EM(\pi), I^*) \Downarrow O^*\).

The proof of precision of the enforcement mechanism of NI is based on Lem. [7.1] and Prop. [6.2] We have:
Regardless of the order of executing local execution, the input $I^*$ and output $O^*$ will be such that $I^*|_c = I|_c$, and $(\text{EM}(\pi), I^*) \Downarrow O^*$ (by Lem. 7.1).

$O^*|_c = O|_c$ (by Prop. 6.2 and $\pi$ satisfying TSNI).

Therefore, the theorem holds for the enforcement mechanism of NI.

For the RI property, the structure of the proof is similar. We can directly state the main lemma since we have already stated the key propositions.

**Lemma 7.2.** Let $\pi$ be a program satisfying RI and $(\pi, I) \Downarrow O$. Regardless of the order of running local executions, if the low execution consumes the same low input items as in $I$, and the high execution consumes high input and low input items as in $I$, then it follows that the execution of the enforcement mechanism is terminated, and the input consumed by the enforcement mechanism is $I^*$, where $I^*|_c = I|_c$ for all $c$.

**Proof.** The proof is similar to the proof of Lem. 7.1. According to the semantics of the enforcement mechanism of RI, the high execution does not influence the termination of the low execution and the output generated by the low execution. The high execution also does not influence the input consumed by the low execution, since $\text{MAP}$ can ask all input items for the low execution, and the low execution only consumes default high input items.

Therefore, regardless of the order of executing local executions, if the low execution consumes the same low input items as in $I$, then the input consumed by the low execution is $I|_L$. $(\vec{df})^* \cdot I_a$, where $I_a$ contains only low input items.

The proofs that $I_a = \epsilon$, the low execution is terminated, the high execution does not request any other low input items not in $I$ are similar to the proofs in Lem. 7.1.

We now prove that all the high input items in $I^*_rc$ are consumed by $\pi[0]$. Assume that there exists a high input item $\vec{v}$ in $I^*_rc$ ($\vec{v}|c \neq \bot$) that is not consumed. From Prop. 7.2 and Prop. 7.1 the existence of such a high input item means that the low execution requested a high input item that was not required by $\pi[0]$. In other words, $|| I^*_rc \cdot \vec{v}|c \neq \bot || I^*_rc \cdot ||. However, since $\pi$ satisfies RI, this case cannot happen.

Let $I^*_rc$ be the input queue received by $\pi[0]$. Since $\pi[0]$ does not request any other input items that are not in $I$, then $I^*_rc|c = I|c$. From Prop. 7.3 we have $I^* = I^*_rc$. Thus $I^*|c = I|c$ and $(\text{EM}(\pi), I^*) \Downarrow O^*$.

**Proof of Theorem 7.1 for RI.** We next prove the precision of the enforcement mechanism of RI. Let $\pi$ be a program satisfying RI, and $I$ be an input queue, such that $(\pi, I) \Downarrow O$. We have:

- Regardless of the order of executing local execution, the input $I^*$ and output $O^*$ will be such that $I^*|_c = I|_c$, and $(\text{EM}(\pi), I^*) \Downarrow O^*$ (by Lem. 7.2).

$O^*|_c = O|_c$ (by Prop. 6.2 and $\pi$ satisfying RI).

Therefore, the theorem holds for the case of RI.

**Proof of Theorem 7.1 for DI.** The proof for DI follows the same structure.
8 Further Properties

Our framework can capture other properties. Other BSPs from [15] can also be enforced. Removal of events (RE) requires that if there is no high input, there is no high output. To enforce RE, when receiving an output request for a high channel from the high execution, REDUCE needs to check whether there are any other high input items different from the default values and affecting the output generated by the high execution. Enforcement of strict removal of inputs (SRI) is similar to the enforcement of RI, but only the low execution can generate output items for both high and low channels. Strict deletion of inputs, deletion of events, and backward strict deletion can be enforced by using the clone instruction and the REDUCE check mentioned above.

In [24] Sutherland defines the notion of non-deducibility (ND) under the assumption that attackers have knowledge about the program, i.e. they know all possible executions of the program. ND can be enforced in our framework by running three local executions: the low, the high and the normal execution. Configuration of the low execution is similar to the low execution in the enforcement mechanism for NI. The normal execution will be privileged to use only input items read by other executions, and to output to high output channels. The high execution will read high input items and consume default low input items. In this way the attackers cannot deduce which execution occurred since there are other executions that can generate the same low behaviour. If an attacker based on his observations tries to construct a set of all possible executions that are low-equivalent, he cannot deduce which sequence of high events did not occur since the set he constructed contains all possible sequences of high events.

By modifying the privileges of local executions or modifying the MAP or REDUCE programs, we can enforce new properties. A possible modification is shown in Fig. [27] where the configuration of $T_M$ is the same as the configuration of $T_M$ for NI, and the MAP program is the same as the one for RI. The low execution needs to wait for high input items requested by the high execution even though the low execution can only consume default values. This option
Fig. 23: A configuration of $T_R$, in which the low execution can send output to high channels

| $LVL[c] = H$ | $\pi[0]$ | $\pi[1]$ |
|------------|--------|--------|
| $LVL[c] = L$ | $-$ | $at$ |

leads to a novel strict property, which we have called substitution-deletion of inputs (SubDI). SubDI requires that when all high input items in an input $I$ are substituted by a default item or deleted, then the remaining input items can be corrected to $I'$, which preserves the low prefixes of high input items in $I$. A program that satisfies RI, but not SubDI, is described in Fig. 22c therefore these properties are actually different.

The configuration of $T_R$ also leads to discovery of new properties. A possible configuration of $T_R$ is described in Fig. 23 in which the low execution can send output items to high channels.

9 Relationships among the properties enforced

We have defined enforcement mechanisms for several information flow properties, but it might be unclear whether these properties are actually different (in our notation). Further we demonstrate that the properties that we have investigated are not the same.

The relationship between RI and NI. The RI property is stricter than the property of TINI, because the RI property requires that if a real value is replaced by a default one, then the other real values are either also replaced by the default ones, or will not appear in the input queue at all. Actually, if a program satisfies the RI property, then it also satisfies the NI property. However, the opposite is not true.

A program, which satisfies NI, but not RI, is shown in Fig. 24a. In this example the level of the channels $cH1$, $cH2$ and $cH3$ is high, while the level of
The channels $cL1$ and $cL2$ is low. This program satisfies the NI property, since the output item on the channel $cL5$ is independent from the secret values from confidential channels. However, this program does not satisfy the RI property. The reason is that the execution of the program with the input $(cH1 = T)(cL1 = val)(cH2 = val)$ is terminated, but if we apply the procedure of perturbation and correction on this input, the results are inputs with which the execution of the program will be error.

The relationship of DI and RI  A program satisfying RI, but not DI, is shown in Fig. 24b. In this example, $I = (cH1 = T)(cH2 = T)(cL1 = val)$ is an input and the execution of the program on $I$ generates the output $O = (cL2 = val)$. If we replace all high inputs with the default values, we obtain another input $(cH1 = F)(cH2 = F)(cL1 = val)$, such that the program in Fig. 24b will produce an output low equivalent with $O$. However, if we replace the last high input event by the default value, then the new input is $I^* = (cH1 = T)(cH2 = F)(cL1 = val)$, and the execution of the program with $I^*$ is not terminated. Therefore, the DI property does not hold for the program.

10 Limitations

Currently, the enforcement mechanism is not independent from the choice of the default values $(val_{df})$. We prove soundness and precision of enforcement with respect to all possible choices of the default values, and we assume that for each channel it is possible to determine a suitable (“non-leaking”) default value.

The definition of DI in our notation requires that high items in $I'_2$ are default ones. This constraint is enough to prevent attackers from deducing whether the value of the last high input is default or not. However, we can put another constraint on $I'_2$, i.e., $\|I'_2|_c\| \leq \|I_2|_c\|$ for all $c$. Regarding this additional constraint, the relationship between DI and RI as shown in [13] is preserved.

Our enforcement mechanism in §5.2 inherits the limitations of the SME mechanism [6]. SME can soundly enforce TINI, but not TSNI. This happens in the case when the low execution is terminated but the high execution is not, and thus the whole enforcement mechanism is not terminated. Respectively, SME (and our enforcement mechanism for NI) can precisely enforce TSNI, but not TINI.

In [11] Kashyap, Wiedermann and Hardekopf evaluate the security guarantees of SME for the termination covert channel; they have proposed to mediate the security problems of SME related to this channel with more sophisticated schedulers. In our approach we do not schedule the order of local executions, therefore, we cannot immediately adapt their suggestions. However, our framework can be extended to control the order of executing local executions by specifying a new rule to control the start of local executions, and the predicate $isReady()$ used in the wake instruction.

We see one of the main limitations of our current proposal in the absence of a practical implementation. It is still an open question, whether the memory and performance overhead will be acceptable, especially for complex properties, such as DI. Devriese and Piessens in the original SME paper [6], as well as Bielova et al. in [4] and De Groef et al. in [8] report on complications while
instrumenting SME for real browsers, which we will have to address. A working implementation is our next target.

11 Related Work

The information flow policies enforcement is a deeply investigated field. We will briefly recall the developed approaches for information flow policies enforcement and discuss the most relevant techniques in more details.

Static analysis techniques for information flow security inspect the program code in order to check whether there is any unwanted information flow. We refer the interested reader to the survey by Sabelfeld and Myers [21] with an excellent overview of static language-based approaches for information flow security.

In contrast to the static verification techniques, dynamic analysis for information flow enforcement tracks propagation of confidential information when a program is executed; an extensive review on the dynamic approach can be found in [14]. The trade-offs between static and dynamic analysis approaches are evaluated by Russo and Sabelfeld in [19].

Our choice of using the multi-execution approach, despite its performance overhead, was dictated by its advantages over the static and dynamic information flow analysis techniques. Static analysis can fall short in scenarios when the program can be composed dynamically, such as in the case of JavaScript; dynamic runtime monitoring for information flow can suffer from impossibility to account for the branch of execution that was not taken, and can leak the control flow details [21], e.g. introduce information leaks through the halting behaviour of the program.

Secure multi-execution [6] has inspired many researchers to push further investigation of this technique. Jaskelioff and Russo in [10] describe their adaptation of SME to Haskell and provide an SME implementation in a handy library. SME is applied to a reactive model of a browser in [4], and is implemented as a fully functional web browser FlowFox that embeds an SME-based runtime enforcement mechanism in [8]. FlowFox is a modification of Firefox, it introduces a noticeable memory and performance overhead, but works with most of the existing web sites. We plan to learn from [8] how to implement a fully working solution and how to evaluate the usability.

Barthe et al. [2] achieve the effects of SME through static program transformation instead of modifying the runtime environment. The transformation technique, which provides sound and precise enforcement of non-interference, is based on the main SME idea: a program is transformed into the sequential composition of the same code paired with a security level ranging from low to high. The program instances on higher levels reuse the inputs of the low instances through global buffers of inputs. We achieve the same security with our enforcement mechanism configuration for NI.

In [11] the authors analyse SME with respect to timing and termination covert channels and propose a variety of schedulers for SME to close these channels. Our framework can be extended with a scheduler to orchestrate the local executions order of executions; we plan to apply the subtleties of timing- and termination-sensitive non-interference identified by the authors and improve our framework by closing these covert channels.

Instead of having multiple different executions, in [1] non-interference is
achieved by using faceted values (pairs of two values containing low and high information). This allows to effectively simulate multiple executions on different security levels while in fact running a single-process execution (the projection property). The authors also introduce enforcement of declassification policies with their technique. Our enforcement mechanism for NI ensures the same security as the faceted values approach; however, our framework currently does not include support for declassification. Yet, enforcement of such property as DI seems infeasible for the faceted values approach in its current state, as significant changes in the semantics for treatment of faceted values are required.

Capizzi et al. in [5] propose the shadow execution technique, with the main goal to prevent confidentiality leaks of the user information in an operating system setting. Shadow execution, which idea is similar to SME, consists of replacing the original program with two copies. The private copy (the high execution) receives the confidential data, but is prevented from accessing the network. The public copy (the low execution) receives fake data, but can access the network; the results from the network are supplied also to the private copy. In this way the private copy can avail any network related functionality without leaking the confidential data. Our framework can be configured to fully simulate the shadow execution technique, by using the configuration for enforcement of NI and regulating the network connectivity of the program copies.

With respect to the body of work on the SME technique, we do not push further the security guarantees offered by the SME paper [6]; for the non-interference property we do not improve the SME drawbacks and do not close the reported covert channels. However, our goal is different. We aim at creating an enforcement framework which can be easily configured to accommodate different information flow properties; and multi-execution is just the technique we have chosen for achieving our goal. Other techniques (e.g. the faceted values approach) can also be considered.

12 Conclusion

We have presented an architecture of an extensible framework for enforcement of information flow properties. To the best of our knowledge, this is the first enforcement mechanism capable to accommodate more than one property. The main idea behind our approach is to run several local instances of a program in parallel, following the idea of secure multi-execution [6], and carefully orchestrate processing of input and output operations of the enforced program through two components (MAP and REDUCE), and two tables ($T_M$ and $T_R$).

To support our claims on the extensibility of the framework we have provided a set of configurations of the enforcement framework for enforcement of non-interference and several properties from the framework of Mantel [15]. The framework component programs for each of these properties are quite simple. For these properties we have formally proven soundness and precision of enforcement.

Our approach to enforcement allows the users to define and enforce novel information flow properties, only by fine-tuning the settings. This characteristics of our framework has huge potential. We plan to continue studying new properties that appear due to fine-tuning the components of the framework, and to research configurations for combinations of several properties.
One may argue whether it is actually easy to configure the enforcement in order to add a new property. Of course, we do not expect that an average user might be interested in defining his own property; we only aim to provide such a user with a checkbox selection of a desired information flow property. However, more security-aware users and the security researchers with a desire to investigate some information flow property will be able to obtain the enforcement mechanism by customizing our framework with simple programs for MAP and REDUCE, and defining the tables $T_M$ and $T_R$, instead of hacking their browsers.

Our next steps include the investigation the patterns of $T_M$, $T_R$, $\pi_M$, $\pi_R$ and the property to be enforced; a proof-of-concept implementation (we have chosen to implement our framework for a web browser; however, our approach can be suitable to any platform), and extension of the framework with more properties and options for declassification.

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