AnySeq/GPU: A Novel Approach for Faster Sequence Alignment on GPUs

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1 INTRODUCTION
Computing alignments of genomic sequences is a core algorithmic component in bioinformatics. With the development of next-generation sequencing (NGS) technologies, increasing amounts of high throughput sequencing read datasets are produced, which establishes the need for highly optimized alignment implementations.

Pairwise alignment of two given genomic sequences aims to identify an optimal order-preserving mapping of their characters while allowing insertions of gaps. Needleman-Wunsch [21], Smith-Waterman [29] and their variants are frequently used algorithms to compute optimal local, global, or semi-global pairwise alignments, respectively, by means of dynamic programming (DP). However, their time complexity is proportional to the product of sequence lengths, thus making them highly time consuming for typical NGS datasets which either consist of many short reads (of a few hundred base-pairs in length for Illumina platforms) or long reads (varying between a few thousands to hundreds of thousand base-pairs in length for the PacBio and ONT platforms).

Consequently, a variety of parallelized implementations and libraries have been developed for computing pairwise sequence alignments in recent years on CPUs [5, 19, 25, 31], GPUs [1, 2, 6, 11, 13, 17, 23, 27], and FPGAs [15, 22, 26]. However, existing GPU implementations are limited by inefficient memory access schemes and thus cannot fully exploit the performance of modern GPUs. Furthermore, they are not performance portable to highly varying sequence lengths and different alignment types needed in NGS bioinformatics workflows. In addition, they are only optimized for certain types of (CUDA-enabled) GPUs. Thus, there is an urgent need for a flexible alignment library that reaches close-to-peak performance on modern GPUs from various vendors.

We address this need by presenting AnySeq/GPU—a highly efficient GPU-based extension of the AnySeq 1 [20] library for batched pairwise alignments of short and long sequencing reads. Our implementation uses the AnyDSL compiler framework [14] which is

CCS CONCEPTS
• Applied computing → Bioinformatics; Computational genomics; • Computing methodologies → Massively parallel algorithms; • Software and its engineering → Compilers.

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based upon the concept of partial evaluation [3, 8, 28] and allows for compilation of different variants of the DP algorithm that are highly optimized for specific alignment types, scoring schemes, and hardware targets.

1.1 Contributions
This paper makes the following contributions:

- We present the design of a novel fine-grained parallelization strategy based on warp intrinsics for sequence alignment targeting massively parallel GPU architectures. We introduce a DP matrix partitioning scheme that supports batches with highly varying sequence lengths (see Section 3.1).
- We showcase how AnySeq/GPU uses state-of-the-art DSL technology which makes it possible to implement large parts of AnySeq/GPU in a hardware-independent way and instantiate these parts with highly-optimized kernels for AMD and NVIDIA GPUs (see Section 3.2).
- We demonstrate that our implementation can achieve over 80% of the available peak performance on modern GPUs from both NVIDIA and AMD for single- and half-precision arithmetic. For various types of alignments (local, global, semi-global, with/without traceback), gap penalties (linear, affine), and different NGS technologies (Illumina, PacBio) AnySeq/GPU achieves speedups of at least 3.6x and a median speedup of 19.2x over state-of-the-art GPU codes (GASAL2, ADEPT, NGBIO, AnySeq 1) executed on the same hardware (see Section 4).

2 BACKGROUND

2.1 Sequence Alignment
Let \( Q = (q_1 q_2 \ldots q_m) \) and \( S = (s_1 s_2 \ldots s_n) \) be two genomic sequences over the alphabet \( \Sigma = \{A, C, G, T\} \). For each pair \((q_i, s_j)\) of characters the DP algorithm decides if these characters should be aligned or if a gap should be inserted and records a corresponding score in a matrix \( H \). This is illustrated in Fig. 1, where light gray cells are initialization cells and dark gray cells indicate the ancestral subproblems of the currently active cell in black. Formally, we define \( H \) as a recurrence relation:

\[
H(i, j) = \max\begin{cases}
H(i - 1, j - 1) + \sigma(q_i, s_j) \\
E(i, j) \\
F(i, j)
\end{cases} \quad 1 \leq i \leq m \\
\quad 1 \leq j \leq n \tag{1}
\]

where

- the first row and column of \( H \) are given as initialization,
- \( E \) and \( F \) determine the gap penalty scheme (linear or affine),
- \( \nu \) and the initialization model determine the alignment type (local, global, or semi-global).

This yields the optimal alignment score \( H(i, j) \) of the prefixes \((q_1 \ldots q_i)\) and \((s_1 \ldots s_j)\) where \( \sigma \) is a substitution function over \( \Sigma \times \Sigma \) that determines the score of aligning two characters.

Linear Gap Penalty. For this gap penalty scheme, we just use a gap penalty \( \alpha \):

\[
E(i, j) = H(i - 1, j) - \alpha \tag{2}
\]

\[
F(i, j) = H(i, j - 1) - \alpha \tag{3}
\]

Affine Gap Penalty. For this variant, we penalize a gap of length \( k \) by \( \alpha + (k - 1) \cdot \beta \), where \( \alpha \) is the cost of the first gap (opening) and \( \beta \) the cost of each subsequent gap (extension):

\[
E(i, j) = \max\begin{cases}
E(i - 1, j) - \beta \\
H(i - 1, j) - \alpha
\end{cases} \tag{4}
\]

\[
F(i, j) = \max\begin{cases}
F(i, j - 1) - \beta \\
H(i, j - 1) - \alpha
\end{cases} \tag{5}
\]

Local Alignments. These compute an alignment with the highest score starting at any position \((q_i, s_j)\) and ending at any other position \((q_k, s_l)\) with \( i \leq k \leq m, j \leq l \leq n \). The parameter \( \nu \) in Eq. 1 is set to 0. The DP matrices are initialized as follows:

\[
\begin{align*}
H(0, 0) &= 0 & H(i, 0) &= 0 & H(0, j) &= 0 \\
E(0, 0) &= -\infty & E(i, 0) &= -\alpha - \beta(i - 1) & E(0, j) &= -\infty \\
F(0, 0) &= -\infty & F(i, 0) &= -\infty & F(0, j) &= -\alpha - \beta(j - 1)
\end{align*}
\]

Global Alignments. These always start at position \((0, 0)\) and end at position \((m, n)\). Hence, their optimal score is always stored in cell \( H(m, n) \). The variable \( \nu \) in Eq. 1 is set to \(-\infty\). The DP matrices are initialized as follows:

\[
\begin{align*}
H(0, 0) &= 0 & H(i, 0) &= -\alpha - \beta(i - 1) & H(0, j) &= -\alpha - \beta(j - 1) \\
E(0, 0) &= -\infty & E(i, 0) &= -\alpha - \beta(i - 1) & E(0, j) &= -\infty \\
F(0, 0) &= -\infty & F(i, 0) &= -\infty & F(0, j) &= -\alpha - \beta(j - 1)
\end{align*}
\]

Semi-global Alignments. These do not penalize gaps at the beginning and the end. This leads to the same specifications as for local alignment but the optimal score is determined as the maximal value in the last row or column of \( H \).

Traceback. Score-only computations can be performed in linear space \( O(\min(m, n)) \) and quadratic time \( O(m \cdot n) \). Actual alignments producing this value can be determined by tracing back the predecessor information in the DP matrices. A divide-and-conquer approach [10] consumes linear instead of quadratic space by recursively determining optimal midpoints of the DP matrix—at the cost of doubling the amount of computed DP cells in the worst case.

2.2 GPU Computing
We briefly highlight a number of relevant features for GPU computing.

NVIDIA GPUs. These execute kernels with a number of independent thread blocks. Each thread block is mapped onto exactly one streaming multiprocessor (SM) and consists of a number of warps. Each warp contains 32 threads that are executed in lockstep—similar to vector instructions of SIMD units on CPUs. GPUs contain several types of memory:

- large but high latency off-chip global memory and
- fast but small on-chip shared and constant memory.
Nevertheless, the fastest way to access data is through usage of the thread-local register file.

**AMD GPUs.** These GPUs exhibit a similar general structure. They schedule kernels as a collection of independent *workgroups* onto the *workgroup processors (WGP)* of the GPU. Each workgroup contains multiple *wavefronts*. A wavefront is AMD’s counterpart to a warp. This means that all *work-items* within a wavefront are also executed in lockstep. The most notable difference to NVIDIA GPUs is the number of threads executed in lockstep: Starting with RDNA, wavefronts can be 32 or 64 threads wide, while previous architectures had a fixed wavefront width of 64.

**Warp Shuffles.** These operations are crucial features of our approach. They allow for low latency communication and minimization of memory traffic. In particular, we take advantage of the warp-level collectives `__shfl_sync()`, `__shfl_down_sync()` and `__shfl_up_sync()`. For example, the intra-warp communication operation

```c
R1 = __shfl_up_sync (0 xFFFFFFFF , R0 , 1, 32);
```

moves the contents of register R0 in thread i within each warp to register R1 in thread $i + 1$ for $0 \leq i < 31$.

### 2.3 The AnyDSL Compiler Framework

**AnySeq/GPU** is implemented in AnyDSL [14]. AnyDSL is a framework for staging domain-specific languages using partial evaluation (PE). AnyDSL provides several benefits for the implementation of high-performance domain-specific languages:

*Implementing DSLs without Writing a Compiler.* The programmer implements the domain-specific language as higher-order library functions in the AnyDSL host language Impala. The DSL program is essentially a nested function call to these library functions. By means of partial evaluation, the overhead of these nested calls is entirely removed: The result is highly-optimized code that looks as if a programmer had manually specialized all these functions. Technically, this a combination of the first Futamura projection [7] and a so-called *tagless interpreter* [4].

Implementing DSLs this way typically promotes a more functional style of programming which allows for abstraction from concerns such as hardware dependence by separating these issues into dedicated functions that are passed to the core algorithms as high-order arguments. While functional programming is often associated with slower execution, AnyDSL has demonstrated that the potential overhead of functional programming is succinctly eliminated using partial evaluation [20, 24].

**Compilation to Heterogeneous Hardware.** The AnyDSL compiler infrastructure provides code generators for a variety of heterogeneous hardware targets: multi-core CPUs with vector instruction sets, NVIDIA and AMD GPUs, as well as different kinds of FPGAs. AnyDSL exposes code generation to accelerators via compiler-known, higher-order functions that the programmer can use to map a certain piece of code to, say, a GPU. This way, hardware-independent code is reusable for different targets and will be later on specialized with hardware-dependent code. Therefore, when implementing a domain-specific library in AnyDSL, the implementer can readily choose among these code generators and is not bothered with implementing their own code generators. In turn, every DSL implemented in AnyDSL directly benefits from potential improvements of these code generators in the AnyDSL compiler.

**Partial Evaluation.** AnyDSL hinges strongly on partial evaluation and AnySeq/GPU makes use of partial evaluation in the way described above but also in several other ways that are described in Section 3.2 to elegantly optimize code even further. Therefore, we briefly introduce the most important features of AnyDSL’s partial evaluator. Programmers control the partial evaluator via so-called *filters*. These are Boolean expressions of the form @*(expr)* that annotate function signatures. Each call site instantiates the callee’s filter with the corresponding argument list. If the expression evaluates to ttrue, the call is *guaranteed* to be specialized. Additionally, the expression ?expr yields ttrue, if expr is known at compile time; the expression $expr$ is never considered constant by the evaluator. For example, the following @*(?)n* filter will only specialize calls to pow if n is statically known at compile time:

```c
fn ?(n) pow(x: int, n: int) -> int { /* ... */ }
```

Thus, the call `pow(x, 5)` produces a loopless sequence of multiplications, `pow(3, 5)` evaluates to 243 while `pow(x, 5)` remains untouched. The fact that the specialization behavior is determined for each call site independently is called *polyvariance*. As syntactic sugar, ? is available as shorthand for @*(true)*. This causes the partial evaluator to always specialize the annotated function. Finally, Impala automatically annotates higher-order parameters for specialization.

### 3 METHODS

We base our parallelization scheme on computing an independent alignment per warp, a group of synchronized threads that are executed in lockstep and communicate via collective operations such as shuffles or votes. Threads in a warp thus can compute DP matrix cell values in a cooperative fashion. In order to unlock the full potential of modern GPUs for alignment, we apply the following techniques:

- Full in-register computation of the DP recurrence relations.
• Low latency communication of neighboring DP cells between threads through warp shuffles.
• Reduction of frequent sequence character loading from memory by employing an intra-warp communication scheme based on warp shuffles.
• Efficient scheme for substitution table lookups \(\sigma(q_i, s_j)\).
• DP matrix partitioning scheme for long sequences.
• Optional traceback in linear space.

3.1 Mapping Matrix Cells and Sequences to Threads

Each warp in a thread block (a group of \(p\) threads \(T_0, ..., T_{p-1}\) where \(p = 32\) for NVIDIA, \(p = 64\) for AMD) executed in lockstep, computes the score for aligning a (query) sequence \(Q\) to a (subject) sequence \(S\). Assume \(Q\) of length \(m\) and \(S\) of length \(n = k \cdot p - 1\). We use register tiling to assign \(k\) columns of the DP matrix to be calculated by each thread (see Fig. 2). Computation proceeds along a wavefront in \(m + p\) iterations. In iteration \(i\), thread \(T_i\) computes \(k\) adjacent cells of the DP matrix row \(i - t\). The maximum possible value of \(k\) depends on the number of available registers and used data type.

According to the recurrence relations Eq. 1–5 of all pairwise comparisons of each thread (see Fig. 1). All cells of the current and previous iteration are stored in thread-local registers. Thread \(T_i\) obtains the rightmost value of thread \(T_{i-1}\) computed in the previous iteration by using a low-latency warp shuffle-up instruction.

At the beginning each thread \(T_i\), \(0 \leq t < p\) loads \(k\) characters of the subject sequence \(S\) from global memory. Note that the characters of \(S\) remain the same for each column of the DP matrix while the required characters from \(Q\) vary. The loaded subject characters are used to create a scoring profile in shared memory; i.e., a lookup table that stores the resulting substitution score \(\sigma\) of all pairwise comparisons of each subject character with all characters of the alphabet \(A, C, G, T\). In subsequent steps, this profile is used to obtain scores for the pairwise comparisons of subject and query sequence characters. This approach avoids branch divergence associated with handling cases of mismatching character pairs differently from matching ones. Furthermore, a 4-character-wide data type allows for looking up 4 neighboring cells in the substitution table with a single shared memory access to the scoring profile. Note that creating the scoring profile requires only one linear pass over the input sequence which results in a negligible runtime compared to the subsequent DP matrix computation which is quadratic in the input sequence length.

In order to avoid repeated, expensive reading from global memory, we only load new query characters every \(p\) iterations and otherwise exchange them between threads via warp shuffles with two registers \(c_q0\) and \(c_q1\) per thread. Register \(c_q0\) stores the query character \(Q_{i-t-1}\) needed for the current computation by thread \(t\) in iteration \(i\) while register \(c_q1\) stores the character needed for the next computation. At the start of each iteration, thread \(0\) copies the current value of \(c_q1\) to \(c_q0\). Afterwards, a warp shuffle-up and a warp shuffle-down update \(c_q0\) and \(c_q1\), respectively, with characters from neighboring threads. Only in iterations \(0 \leq i < m + p\) with \(i \mod p = 0\) each thread \(t\) loads a new query character \(Q_{i+t}\) from memory and stores it in \(c_q1\).

To compute the current matrix row, each thread first looks up the \(k\) substitution scores \(\sigma(c_q0, S_j)\) for \(x = t+kj+1\) for \(x \geq 0, 0 \leq j \leq k\) from the scoring profile and subsequently computes the recurrence relations Eq. 1–5. This involves several maximum, addition, and subtraction operations.

On modern GPUs from both NVIDIA and AMD the maximum number of registers per SIMD unit is limited to 255 and 256, respectively. This restricts the maximum number of columns \(k\) that are computable by one thread. In order to overcome this limitation, we partition the workload into \(l\) non-overlapping submatrices of size \((m + 1) \times \frac{p}{l}\) that are computed by a thread group in \(l\) stages from left to right. DP cells in the right column of thread \(T_{p-1}\) are stored in shared memory or global memory (depending on the sequence length) and loaded by thread \(T_0\) in the next stage. In order to avoid repeated, expensive accesses to global memory, these values are only loaded/written every \(p\) iterations and otherwise exchanged between threads via warp shuffles in a similar way to reading query sequence characters as explained above.

Listing 1 shows Impala pseudo-code of our kernel that computes global alignments with a linear gap scoring scheme using a single warp and a single stage, i.e., for a subject sequence that has at maximum \(p \cdot k\) characters. \(\text{update_matrix}(\cdot)\) computes \(k\) DP cells per thread (red cells in Fig. 2) using thread-local in-register computation and shared memory lookups to the scoring profile. Required communication to access neighboring DP cells \(\text{shfl\_up\_sync}(H, \text{read}(k), 1)\) or neighboring query sequence characters \(\text{shfl\_up\_sync}(c_q0, 1)\), \(\text{shfl\_down\_sync}(c_q1, 1)\) occur outside this function using low latency warp shuffles (dashed arrows in Fig. 2). Within the for-loop, global memory is only accessed every \(p\) iterations \(i\) to load new query characters (green values in Fig. 2) in a coalesced fashion that are stored in thread-local registers (variable \(c_q1\)). Prior to the for-loop \(\text{init\_profile}(\cdot)\) initializes scoring profiles from subject sequences in shared memory.

3.2 GPU Kernel Variants

We employed AnyDSL’s user-guided partial evaluation to generate GPU kernels that are tailored to different hardware requirements, alignment schemes, maximum input sequence lengths as well as scoring schemes with their associated penalty values, which are often known at compile time.

Data views are used to abstract the memory access to different parts of the input sequence batch, scoring profile storage, storage for intermediate scores and storage for the final scores. All reading and writing data accesses are hidden behind accessor functions whose calling overhead is fully eliminated by PE. Furthermore, since functions are first-class citizens in Impala, one can easily change data access schemes by assigning different functions to members of “data view” structs. This allows us to implement code in a data-source-agnostic way and also enables easy exploration of different data layouts during development. We obtain optimized kernels for the alignment of sequences with a known maximum length by setting this value in the corresponding data view and feeding it to the partial evaluator.

In a similar manner, we specialize most parameters of the alignment and scoring scheme by selecting appropriate functions that...
provide the desired behavior at compile time. Such functions are
grouped in structs and are used to determine the substitution func-
tion \( \sigma \), the strategy for initializing cells in the leftmost column and
topmost row of the DP matrix, and the lookup and tracing of the
optimum score. Scoring strategies for linear and affine gap penalties
are factored out to separate kernels as the need to perform addi-
tional computations on matrices \( E \) and \( F \) leads to a significantly
altered code structure throughout a scoring function. Partial eval-
uation combines these kernels with the desired scoring function
without performance overhead.

In addition to the alignment score we also implemented the
full traceback of the actual alignment. For sequences with a total
length of up to 128 characters we explicitly store the optimum cell
predecessors which leads to quadratic memory overhead. We use
Hirschberg’s traceback algorithm \[10\] for longer sequences as it
only requires linear memory overhead at the expense of doubling
the amount of total score computations.

Maximum performance is only achieved if the arrays for the
matrix cell values associated with a thread are all stored in registers.
Unlike objects of fundamental or aggregate type, arrays defined in
a CUDA kernel’s scope are not always guaranteed to be stored in
registers and may be put in much slower constant memory instead.
The compilers by NVIDIA or AMD usually decide this based on
heuristics without providing guarantees to the developer. However,
using AnyDSL we defined an unrolled array type that is usable
like an ordinary array while its elements are actually put into
scalar registers—combining the convenience of index-based access
with the performance of register variables. The size of an unrolled
array is fixed at compile time and access to elements is done by
mapping array indices to variables using recursive conditions that
are partially evaluated at compile time.

Score computation requires several smaller loops, e.g., over all
4 possible DNA characters. According to our observations such
loops often benefit from loop unrolling. Using Impala’s for-loop
abstraction, we simply exchange a regular range-based loop iterator
with an unrolling one. Unlike traditional compiler pragmas which
are non-binding requests, AnyDSL guarantees that unrolling takes
place when desired, because the unroll iterator is implemented
using partial evaluation filters (see Section 2.3). This allows for
easy, step-by-step tuning of kernels guided by reliable performance
experiments.

All score computations exclusively use floating-point arithmetic
since we observed that it consistently leads to higher throughput
on all our test systems compared to integer arithmetic. In addition,
we also employed half-precision arithmetic instructions supported
by NVIDIA A100 and AMD MI100 accelerators that allow for the
simultaneous execution of one operation on two half-precision val-
ues. Besides instructions for packing (extracting) 2 single-precision
values into (from) a pair of half-precision values, we used addition
and maximum\(^1\) operations that operate on pairs of half-precision
values to compute the DP recurrence relations. We compute two
independent alignments at the same time in the lower and the up-
per part of a packed pair of half-precision values thus effectively
doubling the number of cells computed per thread.

Note that there are no rounding issues since the actual values of
the computation are always integer. Furthermore, the limited range

\(^1\)The required \texttt{half2max} comparison function is supported on A100 and MI100 but
not on the utilized GV100 and RTX3090 GPUs.
We compared AnySeq/GPU to three GPU alignment libraries: NVBIO 1.1, GASAL 2 and ADEPT, to the established CPU sequence alignment library SeqAn 2.4.0, and to AnySeq 1 executed on both CPU and GPU.

We evaluated the experiments on the following systems:

1. Dual Intel Xeon Gold 6130 (Skylake) CPUs, 192 GB of DDR4 RAM, 2 NVIDIA GV100.
2. Dual Intel Xeon E5-2683, 256 GB RAM, NVIDIA RTX3090.
3. NVIDIA DGX-A100 with 8 A100 GPUs, Dual AMD Rome 7741, 2 TB RAM.
4. Dual Intel Xeon Gold 6130, 128 GB RAM, AMD MI100.

CPU-based alignment experiments with AnySeq 1 and SeqAn were run on System 1 using 32 threads. GPU experiments were conducted on one of the GPUs in each of the systems. AnySeq/GPU was compiled with the AnyDSL version from March 2021 which is based on LLVM 10.0. The GPU alignment libraries GASAL 2, ADEPT and the relevant parts of NVBIO were compiled with nvcc 10.2 with g++ 9.3.0 as host compiler for CUDA-enabled GPUs and compiled for use with the MI100 GPU using the HIPIFY tool that is part of AMD’s ROCm 4.3.1 developer tool suite. Benchmark programs that use SeqAn were compiled with g++ 9.3.0.

We computed global, semi-global and local alignments using both a simple scoring scheme with +2 for a match, −1 for a mismatch and a linear gap penalty of 1 and an affine scoring scheme using the same match and mismatch penalties and gap penalties $\alpha = 2$ and $\beta = 1$. AnySeq 1, SeqAn, NVBIO and GASAL offer optimized implementations for all combinations of alignment types and gap penalty schemes while ADEPT is primarily optimized for local alignments using an affine gap penalty scheme.

We evaluated the alignment speed for two common tasks that are major runtime contributors in many bioinformatics pipelines:

- pairwise alignment of short DNA snippets (called sequencing reads), and
- alignment of long sequencing reads against a longer genomic sequence.

Speeds are reported by measuring runtimes (excluding PCIe data transfers) and converting them into the number of DP matrix cell updates that are performed per second in GCUPS or TCUPS, i.e., billions (giga) or trillions (tera) of cell updates per second.

All read data sets were created from human chromosome 10 sequence GRCh38_chr10 using simulator tools. We generated a total of six sets each consisting of 3536 Illumina short to medium-size reads with lengths of 125, 250, 512, 1024, 2048 and 4096 characters using Mason 2.0.9 with default settings. For each combination of short read data set, system, alignment library and alignment scheme the resulting alignment speed was obtained as the median speed of 10 runs (arithmetic mean of the 5th and 6th decile value) where each run computed all 3536 ± 12.5 million pairwise alignments of the reads in a set.

As long read sequencing technologies have been gaining importance in recent years, we also included a set of PacBio long reads simulated using PBSIM 1.0.3. Individual read lengths in our Pacbio read set vary from 4,442 to 57,571 characters with an average length of 21,223 and a standard deviation of 6,482. The Pacbio reads were aligned against the original genomic sequence from which they were created. As for the short reads, each speed result reported is the median speed of 10 runs.

4 EVALUATION

4.1 Experimental Setup

We compared AnySeq/GPU to three GPU alignment libraries: NVBIO 1.1, GASAL 2 and ADEPT, to the established CPU sequence alignment
Detailed information about the usage of the two simulators (MA-SON and PBSIM) and the constructed datasets are also provided on the AnySeq/GPU repository (https://github.com/AnyDSL/anyseq).

Note that due to the quadratic time complexity, PCIe transfers are typically negligible; e.g., for the 512bp Illumina dataset used in our tests, data transfers only take 0.36 ms. That compares to a computation time of around 866 ms for global alignment with linear gaps on an MI100. Furthermore, PCIe data transfers can be overlapped with computation using batching. Similar values hold for the transfer of the results back to the CPU (note that in many scenarios this is not even required since the results could be further processed on the GPU).

4.2 Efficiency Analysis

We first analyze if our approach is able to effectively remove overheads occurred by memory accesses by modeling the theoretical peak performance (TPP) in terms of cell updates per second (CUPS) of the utilized GPU hardware as:

\[
TPP = \frac{\#\text{Cores} \times \text{Clock}}{\text{Cycles}_{\text{per cell update}}}
\]

Cycles_{per cell update} in Eq. 6 models the maximum attainable performance constrained by the algorithm structure. In our case it refers to the minimal number of clock cycles needed by an individual FP32-core of the utilized GPU to calculate one DP matrix cell.

We use global alignment with affine gap penalties with Illumina reads as case study to analyze to what extend AnySeq/GPU makes optimal use of the hardware. The number of required arithmetic operations in our implementation to calculate a single DP cell is 7 (i.e. 4 maximum instructions and 3 additions/subtractions). These values are determined by Eq. 1 (1 add, 2 max)\textsuperscript{3} and optimized versions of Eq. 4 and 5 (2 sub, 2 max)\textsuperscript{4}. This leads to 7 required clock cycles per cell update (when using single-precision arithmetic on GV100 and RTX3090) and 3.5 required clock cycles (when using half2 arithmetic on A100 and MI100). Note that we disregard the lookup operation \(\sigma(q_i, s_j)\) since it can in principle be performed concurrently to computation. Table 2 shows that AnySeq/GPU is able to achieve efficiencies of over 80% on all utilized GPUs, which shows that our approach is able to effectively minimize overheads from memory accesses.

4.3 Performance Comparison

Table 1 shows the median speeds in GCUPS for computing global alignments using a linear gap penalty scheme with and without performing a full traceback for the different libraries (AnySeq/GPU, GASAL 2, NVBIO, SeqAn, AnySeq 1) and three different read sets (125bp, 512bp, PacBio). Computing only the global alignment score with a linear penalty scheme is the scenario for which all libraries deliver their maximum performance on all four test systems. This is to be expected since no additional DP cells for affine gap penalties have to be maintained and the currently best local score does not need to be tracked.

AnySeq/GPU clearly outperforms all other tested GPU libraries in each test case. When aligning short reads of length 125bp AnySeq/GPU achieves a minimum speedup of 4.4\times and a median speedup of 9.3\times over all other tested GPU libraries on the same hardware and a minimum speedup of 3.6\times and a median speedup of 7.6\times when also computing the traceback. The difference becomes even more pronounced for reads of length 512bp where AnySeq/GPU outperforms the other GPU libraries by a minimum factor of 7.1 and a median factor of 34.5 for score computation using the same hardware setup and at least a factor of 6.2 and a median factor of 27.9 when also computing the traceback. Again using the same hardware setup, the performance advantage over the other GPU libraries for aligning long Pacbio reads with a high length variance is of similar magnitude, where AnySeq/GPU is at least 5.8 times faster with a median speedup of 28.2\times for score computation and at least 3.9\times faster with a median speedup of 18.3\times when performing a full traceback. Summarizing, AnySeq/GPU provides a minimum speedup of at least 3.6\times and a median speedup of 19.2\times across all tested alignment scenarios and hardware setups compared to GASAL 2, NVBIO and AnySeq 1.

State-of-the-art CPU-based alignment libraries like SeqAn or AnySeq 1 can outperform or closely match the performance of the fastest currently available GPU libraries for the same alignment task when running on a modern workstation CPU. However, for the first time, AnySeq/GPU provides a clear benefit of using a costly GPU accelerator over a workstation CPU. It outperforms both tested CPU libraries running with 32 threads and using AVX512 SIMD instructions by at least a factor of 4.3 with a median speedup of 5.9\times using the slowest tested GV100 GPU and a factor of at least 9.8 with a median speedup of 13.2\times on an MI100 which was the fastest GPU in our benchmarks.

Aligning short reads against other short reads is one of the most prevalent tasks in bioinformatics pipelines. Fig. 3 gives an overview of speeds achieved for the pairwise alignment of 125 bp Illumina short reads for different combinations of alignment schemes (global, semi-global, linear), gap penalty scheme (linear or affine) and result type (score only, traceback). These results reveal that AnySeq/GPU’s GPU implementation consistently outperforms all tested competitors. The setup in which all libraries perform worst is computing the traceback of local alignments with affine gap penalties, yet AnySeq/GPU is able to achieve up to 757 GCUPS on an A100 GPU in this scenario while the fastest competitor GASAL 2 achieves only 124 GCUPS on the same GPU and the fastest CPU implementation achieves only 82 GCUPS.

We performed several experiments with varying read lengths in order to investigate its influence on the resulting speed in batched alignment scenarios on the GPU. On the newer RTX3090, A100 and MI100 GPUs AnySeq/GPU shows a continuous increase in speed up to a read length of 512 bp for all score-only pairwise alignment scenarios including the fastest setup (global alignment, linear gaps) as well as the slowest setup (local alignment, affine gaps) as shown in Fig. 4a–c. Global alignments on the GV100 GPU are fastest for reads of length 1024 bp while affine alignments are fastest for reads of length 256 bp. Across all tested setups, AnySeq/GPU aligns reads of up to 4096 bp no more than 20% slower than its best performance at 256 or 512 bp. This shows the effectiveness of our partitioning scheme for different sequence lengths.
a) global alignment, linear penalties; b) global alignment, affine penalties; c) local alignment, affine penalties.

Figure 4: Median speed in GCPUS achieved for pairwise score computation using AnySeq/GPU for reads of varying lengths for a) global alignment, linear penalties; b) global alignment, affine penalties; c) local alignment, affine penalties.
Table 1: Median speeds in GCUPS for global alignments using a linear gap penalty scheme for a) 12.5 million pairwise alignments of 125 bp short reads, b) 12.5 million pairwise alignments of 512 bp short reads and c) alignments of long Pacbio reads (21223 ± 6482 bp) against a long genomic sequence (∼135 million bp). CPU experiments were run on System 1. Best values per column are indicated in bold.

Table 2: Efficiency of AnySeq/GPU for global alignment with affine gap penalties on different GPUs. Achieved TCUPS is the maximal performance of AnySeq/GPU in Fig. 4b. (TPP = theoretical peak performance.)

5 RELATED WORK
Parallelization of pairwise sequence alignment has been investigated mainly in the context of two types of application scenarios:

(1) computing a single alignment of two very long DNA sequences (typically whole genomes or chromosomes), and

(2) computing batches of different alignments of shorter length.

Widely adopted parallelization schemes are *inter-sequence* (computes DP matrix cells of a number of independent alignment tasks in parallel), *intra-sequence* (computes DP matrix cells of a single alignment in parallel), and their hybrid combination.

5.1 CPU Implementations
Approaches on CPUs for processing NGS data where a large number of alignments needs to be computed typically combine SIMD vectorization with multi-threading [5, 19, 25, 31]. For the alignment of a single pair of long genomic sequences, most approaches employ wavefront parallelism for intra-sequence parallelization [12, 16, 26]. This approach takes advantage of the dependency relationship in the recurrence relation: each cell depends on its left, upper, and upper-left neighbor. An additional level of coarse-grained parallelism (e.g. on CPU/GPU clusters) has been proposed based on speculative execution or compensation-based parallelism [6, 11, 18].

5.2 GPU Implementations
Existing GPU-based approaches often compute an independent alignment per CUDA thread block whereby threads compute cells along a minor diagonal of the DP matrix in parallel. Data between neighboring diagonals is communicated via shared memory. Early implementations have been optimized for specific alignment types and use cases [13, 17, 27]. More recent GPU approaches provide more flexible libraries and APIs, which are required for processing high-throughput NGS data such as GASAL 2 [1], ADEPT [2], and NVBIO [23]. Wang et al. [30] attempted to replace shared memory accesses in DP computation by warp shuffles between registers but only achieved very moderate improvements due to an ineffective partitioning scheme. In addition, AnySeq [20] demonstrates that using PE and AnyDSL it is possible to build an alignment library based on higher-order abstractions that can specialize on a variety of architectures (CPUs, GPUs, and FPGAs).

This work, AnySeq/GPU, replaces the less efficient GPU kernels in AnySeq 1. It computes one alignment per warp thereby allowing for fast communication between thread-local registers by means of warp shuffles in systolic fashion. This new parallelization with its associated partitioning scheme minimizes memory access overheads and achieves over 80% of the theoretical peak performance of modern NVIDIA and AMD GPUs. It outperforms GASAL2, ADEPT, NVBIO, and the old AnySeq 1 implementation by a factor of at least 3.6 and achieves a median speedup of 19.2× over these tools across different alignment scenarios and sequence lengths.
6 CONCLUSION

The continually increasing volume of genomic sequencing data has resulted in a growing demand for high-throughput sequence processing pipelines in recent years. Sequence alignment is an important algorithmic part of many bioinformatics applications and a major contributor to their overall runtime.

We have presented AnySeq/GPU, a high performance sequence alignment library that makes use of a new approach for implementing high-throughput DP algorithms on modern GPU architectures based on warp shuffles and half-precision arithmetic. AnySeq/GPU’s implementation achieves over 80% peak performance on modern GPUs and outperforms state-of-the-art GPU-based competitors such as GASAL 2, NVBIO and ADEPT by at least a factor of 6.6 and achieves a median speedup of 30× compared to these tools when running on the same hardware. AnySeq/GPU is also at least 3.6 times faster than the old AnySeq 1 GPU implementation and achieves a median speedup of 7.6× compared to it (taking into account different alignment schemes, traceback and all tested read lengths). Furthermore, AnySeq/GPU offers a clear advantage over state-of-the-art AVX512-enabled CPU libraries. Using an AMD MI100 it outperforms SeqAn and AnySeq 1 running on a dual-CPU workstation with 32 physical threads by at least 9.8× with a median speedup of 13.2×.

Our results show that prior GPU approaches have not been able to unlock the full potential of GPUs for alignment and only achieve a fraction of the available peak performance. As a consequence, they cannot provide significant speedups compared to current CPU-based approaches since they are bottlenecked by inefficient memory access schemes. Our approach thus changes the standing of GPUs in sequence alignment significantly. We demonstrate a GPU implementation that has close-to-peak performance on modern GPUs and a (median) 30-fold performance increase in terms of GCUPS compared to the best performing existing GPU codes for a variety of sequence lengths (ranging from 125 to 4,096 for Illumina reads, and 4,442 to 57,571 for PacBio reads). Our partitioning scheme allows for even longer sequence lengths while requiring only linear memory consumption. Thus, GPUs can be efficiently used for typical problem sizes used in practice for processing large-scale NGS datasets in bioinformatics.

Our parallelization scheme is in general not limited to pairwise alignment but is applicable to a wider range of DP-based algorithms with similar dependency relationships such as the Viterbi algorithm for finding a most likely sequence of hidden states in a hidden Markov model. It would thus be interesting to evaluate the performance of our approach when adapted to different DP algorithms. Related speed advantages might become even more pronounced on upcoming GPUs such as the recently announced NVIDIA Hopper architecture by taking advantage of new DPX instructions for accelerating DP algorithms [9].

Our implementation makes use of the AnyDSL compiler framework and is written in its functional front-end language Impala. The partial evaluation guarantees provided by AnyDSL enable convenient higher-order abstractions for separating computation into common generic parts and parts that are optimized for specific hardware architectures. Program parametrization for different alignment variants, scoring schemes and mappings to different architectures are achieved through simple function composition instead of complicated and hard-to-debug metaprogramming. Performance tuning was greatly enhanced by the ability to trigger guaranteed specializations like loop unrolling instead of relying on unpredictable compiler heuristics. For the development of AnySeq/GPU, AnyDSL was particularly helpful to implement abstractions that made the creation and exploration of several algorithmic variants and parameter sets very easy. In a conventional setting, all these variants would have to be implemented manually. Using AnyDSL, they are generated automatically using PE without any runtime overhead.

AnySeq/GPU is open source software and can be downloaded at https://github.com/AnyDSL/anyseq.

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