Abstract—We propose the theory of Cayley graphs as a framework to analyse gate counts and quantum costs resulting from reversible circuit synthesis. Several methods have been proposed in the reversible logic synthesis literature by considering different libraries whose gates are associated to the generating sets of certain Cayley graphs. In a Cayley graph, the distance between two vertices corresponds to the optimal circuit size. The lower bound for the diameter of Cayley graphs is also a lower bound for the worst case for any algorithm that uses the corresponding gate library. In this paper, we study two Cayley graphs on the Symmetric Group $S_n$: the first, denoted by $I_n$, is defined by a generating set associated to generalized Toffoli gates; and the second, the hypercube Cayley graph $H_n$, is defined by a generating set associated to multiple-control Toffoli gates. Those two Cayley graphs have degree $n2^{n-1}$ and order $2^n$. Maslov, Dueck and Miller proposed a reversible circuit synthesis that we model by the Cayley graph $I_n$. We propose a synthesis algorithm based on the Cayley graph $H_n$, with upper bound of $(n-1)2^n+1$ multiple-control Toffoli gates. In addition, the diameter of the Cayley graph $H_n$ gives a lower bound of $n2^{n-1}$.

Index Terms—circuit synthesis, quantum complexity, Cayley graphs.

I. INTRODUCTION

An important feature of the circuit model of quantum computation is reversibility. This is a consequence of the evolution postulate of quantum mechanics, which states that the time-evolution of the state of a closed quantum system is described by a unitary operator [1]. Therefore, the theory of reversible computation is one of the foundations of quantum computation. In any reversible circuit—classical or quantum—the output contains sufficient information to reconstruct the input, i.e., no input information is erased [2]. This aspect of reversible computation has important physical consequences. For instance, it is well established that conventional logic gates lead to at least $kT \ln 2$ energy dissipation per irreversible bit operation, where $k$ is Boltzmann’s constant and $T$ is the absolute temperature of the circuit [3]. Therefore, logical circuits with almost zero power dissipation will only be possible if they are built from reversible gates [4]. Thus, reversible computers can be economically more interesting for low-power design than a computer with conventional circuits. The field of reversible computing also draws motivation from several sources, such as signal processing, cryptography, computer graphics, nano and photonic circuits, just to mention a few [5].

A set of reversible gates is needed to design reversible circuits. Group Theory has recently been employed as a tool to analyse reversible logic gates and investigate generators for the group of reversible gates [6], [7]. In this work, we study Cayley graphs associated to the Symmetric Group $S_n$ in order to analyse reversible circuit synthesis methods. Each method has been proposed by considering different libraries whose gates are associated to the generating sets of certain Cayley graphs.

Several properties of these Cayley graphs—such as degree, distance and diameter—are considered. The degree of the Cayley graph is exactly the size of the generating set, which in turn corresponds to the size of the gate library. The distance between two vertices corresponds to the optimal circuit size—each gate produces an edge of the Cayley graph, so the circuit size corresponds to the distance. Finally, an important property of Cayley graphs is that the lower bound for their diameter is also a lower bound for the worst case of any algorithm that uses the corresponding gate library.

Our goal is to analyse reversible circuit synthesis based on Cayley graphs. We present two Cayley graphs on the Symmetric Group $S_n$: the first, denoted by $I_n$, is defined by a generating set associated to generalized Toffoli gates (G-Toffoli); the second, the hypercube Cayley graph $H_n$, is defined by a generating set associated to multiple-control Toffoli gates (MC-Toffoli). Maslov, Dueck and Miller [8], [9] proposed a reversible circuit synthesis that we model by the Cayley graph $I_n$. We propose a synthesis algorithm based on the Cayley graph $H_n$ with upper bound of $(n-1)2^n+1$ multiple-control Toffoli gates. In addition, the diameter of the Cayley graph $H_n$ gives a lower bound of $n2^{n-1}$.

This paper is organized as follows. In Section 2, we introduce notation and review some basic concepts on circuits and group theory that will be necessary throughout the paper. We also describe two algorithms for circuit synthesis: the first, based on G-Toffoli gates; and the second, based on MC-Toffoli gates. In Section 3, we present the analysis of the circuit synthesis based on G-Toffoli gates, which we model by Cayley graph $I_n$. In Section 4, we present the analysis of the circuit synthesis based on MC-Toffoli gates, which we model by Cayley graph $H_n$. In Section 5, we present our conclusions.
II. PRELIMINARIES

A. Graph Theory and Cayley Graphs

Let \((G, \cdot)\) be a finite group with identity element denoted by \(\iota\). A subset \(C\) of this group is a generating set if every element of \(G\) can be expressed as a finite product of elements in \(C\). We also say that \(G\) is generated by \(C\).

**Definition 1.** Let \(C\) be a generating set for a group \(G\). We say that a directed graph \(\Gamma(V, E)\) is a Cayley graph associated to a group with generating set \((G, C)\), if there exists a bijection mapping every vertex \(v \in V\) to a group element \(g \in G\), such that group elements \((g, h) \in G\) are connected by a directed edge \((g, h) \in E\) if and only if exists \(c \in C\) such that \(h = c \cdot g\).

If \(\iota \notin C\), then there are no loops (i.e., edge between a same element) in \(\Gamma\), which we define as the identity free property. If \(c \in C\) implies \(c^{-1} \in C\), then for every edge from \(g\) to \(g \cdot c\), there is also an edge from \(g \cdot c\) to \((g \cdot c) \cdot c^{-1} = g\), which we define as the symmetry condition. The Cayley graph with identity free property and symmetry condition is an undirected graph. In this paper, we only consider undirected graphs.

Let \(A\) be a finite set and \(f : A \rightarrow A\) a bijective function, i.e., a permutation. For example, \(\pi = [1 \ 3 \ 2 \ 0]\) is a permutation over \(\{0, 1, 2, 3\}\) where \(\pi[0] = 1\), \(\pi[1] = 3\), \(\pi[2] = 2\) and \(\pi[3] = 0\). The set of all \(n!\) permutations on \(A = \{0, 1, \ldots, n - 1\}\) with function composition operation forms the Symmetric Group \(S_n\) on \(A\).

**Definition 2.** The distance \(d(u, v)\) between the vertices \(u\) and \(v\) in a graph is the number of edges in a shortest path connecting them.

**Definition 3.** The diameter \(D\) is the largest distance among all pairs of vertices.

In Cayley graphs, the problem of finding the distance among all pairs of vertices, is equivalent to finding the minimum length sequence that creates the element \(p\) from \(\iota\), see [10]. So, in order to find the diameter, it is sufficient to calculate the greatest distance between the identity vertex and all other vertices.

**Definition 4.** Let \(\pi_b\) and \(\sigma_b\) be the binary representations of permutations \(\pi\) and \(\sigma\), respectively. Hamming distance \(d_H(\pi, \sigma)\) is the number of positions in \(\pi_b\) and \(\sigma_b\) with different bits.

For example, the elements \((0, 1, 1)\) and \((1, 1, 1)\) have Hamming distance 1.

B. Reversible and quantum circuits

A logic circuit consists of interconnected logic gates. A classical logic gate is a function \(f : \{0, 1\}^n \rightarrow \{0, 1\}^m\) with \(n\) input bits and \(m\) output bits. We define combinational circuit or irreversible circuit as an acyclic logic circuit, which means that each instance of the logic gate is used only once.

When a function \(f\) is bijective, it has an inverse function. Therefore, there is a circuit where, for each output value \(y\) of \(f\), it produces the value \(x\) such that \(f(x) = y\). In this case we say that the circuit is reversible. A reversible \(n\)-gate realizes a bijective function over \(\{0, 1, \ldots, 2^n - 1\}\). For any reversible gate \(g\), the gate \(g^{-1}\) implements the inverse transformation.

A generalized Toffoli gate or G-Toffoli gate \(C^n NOT(x_1, x_2, \ldots, x_n)\) keeps the first \(n - 1\) lines, called control lines, unchanged. This gate flips the \(n\)-th line, target line, if and only if each control line carries the 1 value. For example, Figure 1 shows a \(C^4 NOT(a, b, c, d)\) gate. For \(n = 0, 1, 2\) the gates are named \(NOT\), \(CNOT\), and Toffoli, respectively (see Figure 2). These three gates compose the CNT library [2], which is a universal set of gates for the classical reversible computing.

![Fig. 1. G-Toffoli gate representing \(C^4 NOT(a, b, c, d)\). The top line denotes the less significative bit.](image1)

![Fig. 2. Circuit representation for the CNT gate library. The top line denotes the less significative bit.](image2)

Observe that a reversible \(n\)-gate applied in a specific position realizes a permutation of \(S_{2^n}\). For example, using decimal notation, the \(NOT\) gate over one line realizes the permutation \([1 \ 0]\). If the \(NOT\) gate is applied over the most significative bit in a 2-line circuit, then the associated permutation is \([2 \ 3 \ 0 \ 1]\). The \(CNOT\) gate over the 2-line circuit realizes the permutation \([0 \ 1 \ 3 \ 2]\) or the permutation \([0 \ 3 \ 2 \ 1]\), depending on the position of the control bit.

The concatenation of gates in a circuit is equivalent to realizing the composition of permutations associated to each gate of the concatenation in the same order.

**Definition 5.** Let \(L\) be a reversible gate library. An \(L\)-circuit is a circuit composed only of gates from \(L\). A permutation \(\pi \in S_{2^n}\) is \(L\)-constructible if it can be realized by an \(L\)-circuit.

**Theorem 1** (Shende et al. [11]). Every permutation is \(CNT\)-constructible with at most one line of temporary store.

**Definition 6.** \(L_I\) is the reversible gate library formed only by generalized Toffoli gates.
A multiple-control Toffoli gate or MC-Toffoli gate $C^n \text{NOT}(x_1, x_2, \ldots, x_n)$ keeps the first $n-1$ lines, called control lines, unchanged. This gate flips the $n$-th line, target line, if and only if each positive (or negative) control line carries the 1 (or 0) value. We indicate the line which is the negative control with \textsuperscript{-} after control. See Figure 3 for an example of a $4 \times 4$ multiple-control Toffoli gate with a negative-positive-negative pattern of control lines and target on the last line, which can be denoted by $C^4(a', b, c', d)$.

$$\begin{array}{c}
a & a \\
b & b \\
c & c \\
d & d' \\
\end{array}$$

Fig. 3. MC-Offoli gate representing $C^4 \text{NOT}(a', b, c', d)$. The top line denotes the less significative bit.

**Theorem 2** (Toffoli [2]). Any invertible finite function of order $n$ is obtained by the composition of multiple-control Toffoli gates.

**Definition 7.** $L_H$ is the reversible gate library formed only by multiple-control Toffoli gates.

In the quantum circuit synthesis, a small set of primitive gates are used as elementary building blocks with an assumed unit cost [12]–[14]. A standard set of universal gates is composed by Hadamard, phase, CNOT and $\pi/8$ gates [1]. In the context of our work, it is also reasonable to include in this set the NOT gate, the controlled-V gate, and the controlled-$V^\dagger$ gate, with $V$ defined as the square root of NOT, i.e., a unitary operator such that $V^2$ is equal to the NOT operator. Each Toffoli gate, $G$-Toffoli gate, or $MC$-Toffoli gate can be decomposed into a sequence of quantum gates from the above mentioned set, following the pattern of Figures 4 and 5.

$$\begin{array}{c}
\text{U} \\
\text{V} \\
\text{V}^\dagger \\
\text{V} \\
\end{array} = \begin{array}{c}
\text{V} \\
\text{V}^\dagger \\
\text{V} \\
\text{V} \\
\end{array}$$

Fig. 4. Decomposition of two-control quantum gate into a sequence of single-control quantum gates. An analog decomposition pattern is possible for quantum gates with more than two controls [1].

The number of gates has been used to evaluate nearly all synthesis approaches in literature so far. For an arbitrary circuit $C$ consisting of a sequence $g_1, g_2, \ldots, g_k$ of $k$ quantum gates, the gate count metric is defined as $gc(C) \equiv k$. We also refer to the notion of quantum cost to measure the implementation cost of quantum circuits. More precisely, quantum cost is defined as the number of elementary quantum operations needed to realize a gate. For an arbitrary quantum gate $g$ that can be decomposed into $k$ elementary quantum gates, its quantum cost metric is defined as $gc(g) \equiv k$. The quantum cost for a circuit $C$ is defined as $gc(C) = \sum_{g \in C} gc(g)$. Table I shows the quantum cost for all the reversible gates used in this paper, with $m$ denoting the amount of negative controls on the $MC$-Toffoli gate.

In Figure 5, we have an example of how to decompose a MC-Offoli gate of size $n = 6$ into Toffoli gates, with $n - 3$ ancilla (garbage) bits, by using a synthesis method based on [15], [16]. Quantum cost, in this case, is the gate count multiplied by 5.

$$\begin{array}{c}
a & a \\
b & b \\
c & c \\
d & d \\
e & e \\
0 & 0 \\
0 & 0 \\
f & f' \\
f' & f' \\
\end{array}$$

Fig. 6. Implementation of MC-Offoli for $n = 6$ and 3 garbage based on [15], [16].

In Figure 7, we have an example of how to decompose a
MC-Toffoli gate of size $n = 6$ into Toffoli gates, with $n-3$ garbage bits, by using a synthesis method based on [12], [13]. Notice that in this case, we do not need to initialize the garbage bits with zeros.

In Figures 8 and 9, we have an example of how to decompose a MC-Toffoli gate of size $n = 8$ into Toffoli gates, with one garbage bit, by using a synthesis method based on [12], [13].

C. Circuit synthesis using generalized Toffoli gates

We show below the reversible circuit synthesis using generalized Toffoli gate, which we call Basic Algorithm. The Basic Algorithm was proposed by Maslov, Dueck and Miller [8], [9], and is reproduced in Algorithm 1. It considers a reversible function specified as a mapping over $\{0, 1, \ldots, 2^n - 1\}$, i.e., a truth vector. It writes a function $f(i)$, where $i$ is an integer in the range $0 \leq i \leq 2^n - 1$, meaning that the function argument $i$ is a vector giving the binary expansion of the integer $i$. The result of the function application to an integer argument $i$, $f(i)$, is treated as an integer as well. The Basic Algorithm works by assigning Toffoli gates at the output end of the cascade. The Toffoli gates are chosen so that the output part of the specification is progressively transformed to match the input part. When a cascade of Toffoli gates transforming the total specification into the identity permutation is found, then reading this cascade in reverse order will transform the input to the required output, thus realizing the target function.

Table II illustrates the application of the Basic Algorithm. Notice that the gates are identified in order from the output side to the input side. The corresponding network is showed in Figure 11.

Using the Basic Algorithm, it is possible to find a permutation for any $n$ that requires at most $(n - 1)2^n + 1$ generalized Toffoli gates. The Basic Algorithm finds the permutation $[7 1 4 3 0 2 6 5]$ for $n = 3$ and the permutation
Algorithm 1: Basic Algorithm [8], [9]

begin
Step 0: If \( f(0) \neq 0 \), invert the outputs corresponding to 1-bits in \( f(0) \). Each inversion requires a NOT gate. The transformed function, written as \( f^+ \), has \( f^+(0) = 0 \).
Step i: Consider each \( i \) in turn for \( 0 \leq i \leq 2^n - 1 \) letting \( f^+(i) \) denote the current reversible specification. If \( f^+(i) = i \), no transformation and, hence, no Toffoli gate is required for this \( i \). Otherwise, gates are required to transform the specification to a new specification \( f^{++} \) with \( f^{++}(i) = i \). The required gates must map \( f^+(i) \rightarrow i \).

Let \( p \) be the bit string with 1s in all position where the binary expansion of \( i \) is 1, while the expansion of \( f^+(i) \) is 0. These are the 1 bits that must be added in transforming \( f^+(i) \rightarrow i \). Conversely, let \( q \) be the bit string with 1s in all positions where the expansion of \( i \) is 0, while the expansion of \( f^+(i) \) is 1. \( q \) identifies the 1 bits to be removed in the transformation.

For each \( p_j = 1 \), apply the Toffoli gate with control lines corresponding to all outputs in positions where the expansion of \( i \) is 1 and whose target line is the output in position \( j \). This will increase the lexicographical order of \( f^+(i) \). Then, for each \( q_k = 1 \), apply the Toffoli gate whose target line is the output in position \( k \), and with control lines corresponding to all outputs in positions, except \( k \), where the expansion of \( f^+(i) \) is 1. This second operation decreases the lexicographical order, but not below \( i \).

| Algorithm | Number of permutations |
|-----------|------------------------|
| 1         | 1                      |
| 2         | 14                     |
| 3         | 92                     |
| 4         | 380                    |
| 5         | 1113                   |
| 6         | 2468                   |
| 7         | 4311                   |
| 8         | 6083                   |
| 9         | 7044                   |
| 10        | 6754                   |
| 11        | 577                    |
| 12        | 10253                  |
| 13        | 17049                  |
| 14        | 1922                   |
| 15        | 8921                   |
| 16        | 3549                   |
| 17        | 2468                   |
| 18        | 625                    |
| 19        | 102                   |
| 20        | 12                     |
| 21        | 1                      |
| 22        | 1                      |
| avg. gates | 8.67                  |

Table III shows the results of applying version of Algorithm 1 over all \( 8! = 40320 \) permutations when \( n = 3 \). We show the number of functions for each gate count and the average number of gates required.

TABLE II

| \( n \) | \( \pi \) | \( \pi' \) |
|--------|--------|--------|
| 2      | \( [0, 1, 2] \) | \( [0, 1, 2] \) |
| 3      | \( [0, 1, 2, 3] \) | \( [0, 1, 2, 3] \) |
| 4      | \( [0, 1, 2, 3, 4] \) | \( [0, 1, 2, 3, 4] \) |
| 5      | \( [0, 1, 2, 3, 4, 5] \) | \( [0, 1, 2, 3, 4, 5] \) |
| 6      | \( [0, 1, 2, 3, 4, 5, 6] \) | \( [0, 1, 2, 3, 4, 5, 6] \) |

D. Circuit synthesis using multiple-control Toffoli gates

We present below the reversible circuit synthesis using multiple-control Toffoli gates, denoted by hypercube method. Each permutation is a sequence of \( n2^n \) bits. The application of a multiple-control Toffoli gate over one permutation \( \pi \) generates a permutation \( \pi' \), with change over two bits, i.e., \( d_H(\pi, \pi') = 2 \). Regarding the identity permutation \( \iota \), we have three cases for the Hamming distance: i) \( d_H(\pi_b, \iota_b) = d_H(\pi'_b, \iota_b) - 2 \), when the gate places two bits in their correct positions; ii) \( d_H(\pi_b, \iota_b) = d_H(\pi'_b, \iota_b) \), when the gate places one bit in its correct position and misplaces one bit in a wrong position; iii) \( d_H(\pi_b, \iota_b) = d_H(\pi'_b, \iota_b) + 2 \), when the gate misplaces two bits in wrong positions.

The hypercube method for reversible circuit synthesis uses the \( L_H \) gate library. This method, presented in the Algorithm 2, uses consecutive applications of multiple-control Toffoli gates in order to organize the bits. The proposed method takes the binary representation of the permutation elements—each one is composed of \( n \) bits—and carries out at most \( n \) changes. Those changes use the multiple-control Toffoli gate in order to put the permutation element in its correct position. See example in Table IV. The corresponding reversible circuit is given in Figure 12.

For instance, Table IV shows the hypercube method that transform the permutation \( \pi = [7 4 1 0 3 2 6 5] \) into the identity permutation \( \iota = [0 1 2 3 4 5 6 7] \).

a
\[ \begin{array}{cccccccc}
  \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\
 a & b & c & a' & b' & c' & a & b'
\end{array} \]

Fig. 12. Reversible circuit that transforms permutation \( \iota \) into \( \pi \), according to example taken from Table IV.
Algorithm 2 makes the reversible circuit synthesis using multiple-control Toffoli gates and reads the permutation from right to left order. We call it the \textit{right order}. One can change the line 4 of Algorithm 2 to read the permutation from left to right order. In that case, we call it the \textit{left order}. Denoted by unidirectional if Algorithm 2 runs right order or left order. Denoted by bidirectional if Algorithm 2 runs right order and left order.

The hypercube method has the following property in the change of permutation and it is used to prove the correctness of Algorithm 2.

\textbf{Property 1.} When \(i < k\) in the external for loop in Algorithm 2, let \(\pi\) be any permutation and let \(\pi[k]\) be a component of permutation \(\pi\), where \(i < k \leq 2^n - 1\). Then we have that \(\pi[k] = k\).

\textbf{Theorem 3.} Algorithm 2 returns a reversible circuit using multiple-control Toffoli gates.

\textbf{Proof:} We will prove by induction the correctness of the Algorithm 2 by showing that in the application of each multiple-control Toffoli gate, at least one bit changes or stays in its correct place. The induction hypothesis: In the step \(i = k\) and \(j = l\), we have \(\pi[k'] = k'\) and \(\pi_b[k][l'] = \omega_b[k][l']\) for \(k' > k\) and \(l' > l\), or in other words, the elements greater than \(k\) and all less significative bits than \(\pi[k][l]\) of \(\pi[k]\) stay in their correct positions.

When \(i = N - 1\), it is only possible to change \(\pi[i]\) with \(\pi[k']\), where \(k' < N - 1\), warranting the satisfiability of the basis of induction.

The induction is guaranteed if we show that the gate application, in the step \(i = k\), does not affect any element \(\pi[k']\), with \(k' > k\).

In the step \(i = k\) and \(j = l\), if \(\pi_b[k][l] = \omega_b[k][l]\) then no change is needed. Otherwise, \(\pi[k]\) must change the \(l\)-th bit with \(\pi[m]\) such that

\[\pi_b[m][p] = \begin{cases} \pi_b[k][p] & \text{if } p \neq l \\ \pi_b[k][p] & \text{if } p = l, \end{cases}\]

where \(l\) is 1 if \(x = 0\) or 0 in otherwise.

If \(\pi_b[k][l] = 1\) then the change (1 to 0) is made to a value \(\pi[m] < \pi[k]\), consequently, by induction hypothesis, to a value less than \(k\). If \(\pi_b[k][l] = 0\) then the change is made to a value greater than \(\pi[k]\). We must show that the \(\pi[m] < k\).

Take the most significative bit \(l'\) of \(\pi[k]\) such that \(\pi_b[k][l'] \neq \omega_b[k][l']\). We can separate in two cases: (i) \(l' = l\) (ii) \(l' > l\). In the case (i), the bits more significative than \(l\) of \(\pi[k]\) are correct and by induction hypothesis, the bits less significative than \(l\) of \(\pi[k]\) are correct and \(\pi[k'] = k'\) for \(k' > k\), hence if \(m > k\) then \(\pi[m] = k\) and \(\pi[m] = k\), that is possible. In the case (ii), if \(m > k\) then \(\pi_b[m][l'] = 1\), but \(\pi_b[m][l'] = \pi_b[k][l']\) when \(l' \neq l\), thus \(\pi[k] > k\) that is contrary to induction hypothesis.

\textbf{Theorem 4.} The reversible circuit returned by Algorithm 2 has size less than or equal to \((n - 1)2^n + 1\) multiple-control Toffoli gates.

\textbf{Proof:} Notice that each gate application changes at least one bit to its correct place. Therefore, Algorithm 2 terminates.
after applying a maximum of \(n2^n\) multiple-control Toffoli gates. In order to prove an upper bound, we construct a worst-case function for this algorithm.

The first \(2^{n-1}\) input patterns match the input, so the most significant bit of the output patterns has been completely dealt, \(2^{n-1}\) zeros are in the upper part of the truth table, the lower \(2^{n-1}\) must then by definition be 1. Therefore, starting from this step, the most significant bit is fixed. Starting from step \(2^{n-1}\), flip only the remaining \(n-1\) unspecified bits of the output.

Similarly, at step \(2^{n-1}+2^{n-2}\) of the algorithm, the second most significant bit will be completely specified. In general, at step \(2^{n-1}+2^{n-2}+\ldots+2^{i-1}\), the \(i\) most significant bits are completely specified. Thus, the maximum number of multiple-control Toffoli gates produced by the Algorithm 2 becomes:

\[
n2^n + (n-1)2^{n-2} + \ldots + n - (n-1)2^{n-2} = (n-1)2^n + 1.
\]

Therefore, \((n-1)2^n + 1\) is an upper bound for the circuit size obtained by Algorithm 2.

Using Algorithm 2, it is possible to find a permutation for any \(n\) that requires at most \((n-1)2^n + 1\) multiple-control Toffoli gates. If Algorithm 2 runs on right order, then we find the permutation \([5 \ 2 \ 7 \ 4 \ 1 \ 6 \ 3 \ 0]\) for \(n = 3\) and the permutation \([5 \ 10 \ 7 \ 4 \ 9 \ 14 \ 11 \ 8 \ 13 \ 2 \ 15 \ 12 \ 1 \ 6 \ 3 \ 0]\) for \(n = 4\). If Algorithm 2 runs on left order, then we find the permutation \([7 \ 4 \ 1 \ 6 \ 3 \ 0 \ 5 \ 2]\) for \(n = 3\) and the permutation \([15 \ 12 \ 9 \ 14 \ 3 \ 0 \ 13 \ 2 \ 7 \ 4 \ 1 \ 6 \ 11 \ 8 \ 5 \ 10]\) for \(n = 4\).

Table V shows the results of applying version of Algorithm 2 over all \(8! = 40320\) permutations when \(n = 3\). We show the number of functions for each gate count and the average number of gates required.

### Table V

| Size | Number of permutations |
|------|------------------------|
|      | Algorithm 2 unidirectional | Algorithm 2 bidirectional | optimal results |
| 17   | 1                      |                         | 8.67           |
| 16   | 14                     |                          | 7.71           |
| 15   | 92                     |                          | 8.50           |
| 14   | 380                    |                          |                |
| 13   | 1113                   |                          |                |
| 12   | 2468                   |                          |                |
| 11   | 4311                   |                          |                |
| 10   | 6083                   |                          |                |
| 9    | 7044                   |                          |                |
| 8    | 6754                   |                          |                |
| 7    | 5379                   |                          |                |
| 6    | 3549                   |                          |                |
| 5    | 1922                   |                          |                |
| 4    | 839                    |                          |                |
| 3    | 286                    |                          |                |
| 2    | 72                     |                          |                |
| 1    | 12                     |                          |                |
| 0    | 1                      |                          |                |
| avg. gates | 8.67 | 7.71 | 8.50 |

III. ANALYSIS OF A CIRCUIT SYNTHESIS BASED ON CAYLEY GRAPH \(I_n\)

In this section, we present the Cayley graph \(I_n\) associated to G-Offoli gates. These gates are used in the method for circuit synthesis proposed by Maslov, Dueck and Miller [8], [9], as we described in Sec. II-C.

**Definition 8.** \(C_1\) is the subgroup of \(S_{2^n}\), such that all permutations \(c \in C_1\) are \(L_1\)-constructible, with only one gate.

**Lemma 1.** The subgroup \(C_1\) is a generating set of \(S_{2^n}\).

Let \((S_{2^n}, \cdot)\) be a finite Symmetric Group with a generating set \(C_1\) given by generalized Toffoli gates.

We denote by \(I_n(V, E)\) the Cayley graph associated with \((S_{2^n}, \cdot, C_1)\). The Cayley graph \(I_n\) has degree \(n2^{n-1}\) and order \(2^n!\). Notice that in this case, the corresponding circuits have \(n\) gates \(N\), \(n(n-1)\) gates \(C\) and \(n(n-1)(n-2)/2\) gates \(T\). Also, for \(i \geq 3\) there are \(\binom{n}{i}\) generalized Toffoli gates. Therefore,

\[
\sum_{i=1}^{n} i \binom{n}{i} = 1 \binom{n}{1} + 2 \binom{n}{2} + 3 \binom{n}{3} + \ldots + n \binom{n}{n} = n2^{n-1}.
\]

**Theorem 5.** The upper bound for the diameter of the Cayley graph \(I_n\) is \((n-1)2^n + 1\).

**Proof:** Follows directly from Algorithm 1, by construction.

**Lemma 2.** The Cayley graph \(I_n\) is not a bipartite graph.

**Proof:** We show that the graph \(I_n\) has an odd cycle. Let \([3 \ 1 \ 0 \ 2], [3 \ 1 \ 2 \ 0], [1 \ 3 \ 0 \ 2], [0 \ 2 \ 1 \ 3]\) and \([0 \ 2 \ 3 \ 1]\) be the five vertices of the Cayley graph \(I_2\). By definition of generating set, we can apply the following changes: \((2, 3)\), that corresponds to \(C^2\text{CNOT}(a, b)\) with target in \(b\); \((0, 1)(2, 3)\), that corresponds to \(C^1\text{CNOT}(a, b)\) with target in \(a\); \((0, 2)(1, 3)\), that corresponds to \(C^1\text{CNOT}(b, c)\) with target in \(b\); \((2, 3)\), that corresponds to \(C^2\text{CNOT}(a, b)\) with target in \(a\); \((0, 2)(1, 3)\), that corresponds to \(C^1\text{CNOT}(b, c)\) with target in \(b\). Therefore, we have an odd cycle and the Cayley graph \(I_n\) is not a bipartite graph.

**Table VI** summarizes our analysis of quantum cost for the synthesis based on Cayley graph \(I_n\), showing its relation to an upper bound for the diameter of the same graph. The first column indicates the amount of garbage (ancilla) qubits. The second column indicates the gate cost, which is upper bound for the diameter of Cayley graph \(I_n\). The third column indicates the quantum cost for the synthesis based on Cayley graph \(I_n\). This quantum cost is obtained by multiplying the diameter of the graph by the corresponding gate count.

IV. ANALYSIS OF A CIRCUIT SYNTHESIS BASED ON CAYLEY GRAPH \(H_n\)

In this section, we present the Cayley graph \(H_n\) associated to MC-Toffoli gates. These gates are used in the hypercube method for circuit synthesis, the we introduced in Sec. II-D.
Table VI

| garbage | gate count (gc) | quantum cost (qc) |
|---------|----------------|------------------|
| 0       | $2n \times 1$  | $(n - 1)2^{n+1}$ |
| 1       | $2n \times 1$  | $(n - 1)2^{n+1} + 1$ |
| n-3     | $2n \times 1$  | $((n - 1)2^{n+1} + 1)(24n - 88)$ |

Definition 9. $C_H$ is the subgroup of $S_{2^n}$, such that all permutations $c \in C_H$ are $L_H$-constructible, with only one gate.

Corollary 1. The subgroup $C_H$ is a generating set of $S_{2^n}$.

Let $(S_{2^n}, \cdot)$ be a finite Symmetric Group with a generating set $C_H$ given by multiple-control Toffoli gates.

We denote by $H_n(V, E)$ the Cayley graph associated with $(S_{2^n}, \cdot, C_H)$. Notice that the Cayley graph $H_n$ has degree $2^{n-1}$ and order $2^n!$, the multiple-control Toffoli $C_H \text{NOT}(x_1, x_2, \ldots, x_n)$ have values $n$ target lines and $0 \leq k \leq 2^{n-1} - 1$, where $k$ is a decimal value that represent the lines control. So, we have $2^{n-1}$ elements in $C_H$.

The Cayley graph $H_n$ has a generating set of the same size and numbers of vertices of the Cayley graph $I_n$, but those Cayley graphs are not isomorphic.

Lemma 3. The Cayley graph $H_n$ is a bipartite graph.

Proof: Let $x = \{ x_1, x_2, \ldots, x_k, x_1, \ldots, x_m, x_n, \ldots, x_{n2^n-1} \}$ be any vertex of the Cayley graph $H_n$ in binary. Let $y = \{ y_1, y_2, \ldots, y_l, y_1, \ldots, y_k, \ldots, y_{n2^n-1} \}$ and $z = \{ z_1, z_2, \ldots, z_m, z_1, \ldots, z_k, \ldots, z_{n2^n-1} \}$ be neighbors of $x$ in binary, where for all $1 \leq i < 2^n$, $x_i = y_i$ and $x_i = z_i$, except $i = m$, $i = n$, $i = k$ and $i = l$, in which cases $x_m = y_m$, $x_n = y_n$, $x_k = z_k$ and $x_l = z_l$. If $m = k$ and $n = l$, then $y = z$. If $m = k$ and $n \neq l$, the Hamming distance between $y$ and $z$ is 3, then there is not an edge. If $m \neq k$ and $n \neq l$, the Hamming distance between $y$ and $z$ is 4, then there is not an edge. Therefore, the Cayley graph $H_n$ does not have odd cycles and $H_n$ is bipartite.

Theorem 6. The Cayley graph $H_n$ is not isomorphic to the Cayley graph $I_n$.

Proof: It follows directly from Lemmas 2 and 3.

Table VII summarizes our analysis of quantum cost for the synthesis based on Cayley graph $H_n$, showing its relation to an upper bound for the diameter of the same graph. The first column indicates the amount of garbage $H_n$, showing its relation to an upper bound for the diameter of the same graph. The second column indicates the gate count, which is an upper bound for the diameter of Cayley graph $H_n$. The third column indicates the quantum cost for the synthesis based on Cayley graph $H_n$. This quantum cost is obtained by multiplying the diameter of the graph by the corresponding gate count.

Table VII

| garbage | gate count (qc) | quantum cost (qc) |
|---------|----------------|------------------|
| 0       | $(n - 1)2^{n+1}$ | $((n - 1)2^{n+1} + 1)(2^{n-3} + 2m)$ |
| 1       | $(n - 1)2^{n+1}$ | $((n - 1)2^{n+1} + 1)(24n - 88)$ |
| n-3     | $(n - 1)2^{n+1}$ | $((n - 1)2^{n+1} + 1)(10n - 23)$ |

V. CONCLUSIONS

Since reversibility is an essential aspect the circuit model of quantum computers, we must have efficient methods for designing and analysing reversible circuits. Group Theory provides an unified framework for the development and analysis of methods for reversible circuit synthesis. In this work, we studied two Cayley graphs, $I_n$ and $H_n$, that can be applied to the synthesis of reversible circuits.

Maslov, Dueck and Miller [8], [9] proposed an algorithm to reversible circuit synthesis using generalized Toffoli gates...
that we modeled by the Cayley graph $I_n$. The framework of the theory of Cayley graphs enabled us to prove that the diameter of $I_n$ is less than $(n - 1)2^n + 1$ and the number of vertices is $2^n!$. These bounds are consistent with the gate count and quantum cost complexity of the circuit synthesis using G-Toffoli gates.

We presented an algorithm to reversible circuit synthesis using multiple-control Toffoli gates. The proposed circuit synthesis is based on the hypercube Cayley graph $H_n$. The diameter of the Cayley graph $H_n$ is at most $(n - 1)2^n + 1$ and is at least $n2^{n-1}$. Since the number of vertices of $H_n$ is $2^n!$, we have that the number of vertices is a factorial on the diameter. We proved that Cayley graph $H_n$ is not isomorphic to Cayley graph $I_n$, so the corresponding synthesis algorithms are different. These bounds are consistent with the gate count and quantum cost complexity of the circuit synthesis using MC-Toffoli gates.

We may expect Cayley graphs to be an attractive and versatile framework for analysing reversible circuit synthesis.

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