Principle and Topology Derivation of Single-Inductor Multi-Input Multi-Output DC–DC Converters

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Abstract—Single-inductor multi-input multi-output (SI-MIMO) dc–dc converters are attractive in the engineering applications due to the advantage of high power density and low cost. In order to explore as many as possible SI-MIMO topologies, this article proposes a simple and effective topology derivation principle that only requires three steps. First, three basic cells consisting of a single inductor and multiple sets of unidirectional switches as well as inputs/outputs are proposed. Second, integrate the mentioned three basic cells with the inductor branch of the typical single-input single-output converters. Finally, implement the topology simplification by removing unnecessary switches/diodes. Based on the proposed principle, a large number of SI-MIMO topologies are derived from buck, boost, buck–boost, and noninverting buck–boost converters in this article. With more topology choices having different performance characteristics, it is very beneficial for engineers to gain an optimized design that a preferred one can be selected out after comprehensive comparison. As an example, topology comparison and selection among a family of single-inductor single-input dual-output converters is also conducted in this article. Besides, performance analysis, design considerations, and simulation/experiment results of the selected optimum topology are demonstrated in detail to verify its advantages.

Index Terms—Multi-input multi-output (MIMO), principle, single inductor (SI), topology derivation.

I. INTRODUCTION

In many industrial applications, such as photovoltaics [1], [2], electric vehicles [3], data processing centers [4], personal computers [5], and so on [6]–[8], multiple ports with various voltage levels are demanded. In order to achieve the voltage regulation as well as the power control among different ports, multiple independent single-input single-output (SISO) converters can be simply employed. However, owing to the large number of components, high overall cost and large system volume will be incurred. To address this problem, two types of integrated multiport dc–dc converters have been proposed, in which the number of semiconductor devices and inductors is effectively reduced, and so that both the cost and power density are improved.

Based on the typical buck [9], [10], boost [11], and buck–boost [12] converters, integrated N-port converters with semiconductor devices multiplexed were proposed, which only need N switches/diodes. In comparison with the conventional solution with independent SISO converters, including 2N−2 switches/diodes, the number of semiconductor devices is N−2 reduced, and hence lower cost can be achieved. Aiming to explore more favorable topologies, a systematic synthesis method was further proposed in [13]. However, because the magnetic components accounting for a very large proportion in the overall volume and weight are not optimized, the improvement of power density is limited in the integrated multiport converters with semiconductor devices multiplexed.

Fortunately, the inductor can also be multiplexed, and only one inductor is employed in the single-inductor multi-input multi-output (SI-MIMO) converter. The inductor functions as a common power flowing path for different ports. Consequently, high power density is achieved in the SI-MIMO converters, which attract increasing attention in the recent years. In general, researches of SI-MIMO converters mainly focus on two aspects, new control and new topologies, to improve converter performance. In terms of the control strategy, there are three common modulation strategies, discontinuous conduction mode (DCM), continuous conduction mode (CCM), and pseudo-CCM/DCM. In [14], the converter is designed to work in DCM with multiple energizing cycles per switching period. It functions similarly as multiple independent SISO converters, and thus good dynamic response is achieved. However, under heavy load conditions,
the peak inductor current will become large, which deteriorates both the current stresses and conduction losses. In order to alleviate this problem, the SI-MIMO converters can work in CCM with one energizing cycle per switching period. Nevertheless, because the power transfer among different ports are dependent on a common inductor, severe cross-regulation problem will be caused. Based on this, multiple new control schemes had been figured out in the past researches, aiming to achieve reduced cross regulation. Besides the CCM and DCM, the SI-MIMO converters can also work in pseudo-CCM/DCM with an extra switch connected between the inductors [15], [16]. It makes a compromise between the current stresses and the cross-regulation problem. In a word, control strategies of SI-MIMO converters have been widely studied in the past.

On the other hand, in terms of the topology configurations, only several SI-MIMO dc–dc converters have been proposed in the existing researches. Six types of single-inductor single-input dual-output (SI-SIDO) topologies based on buck [17]–[19], boost [17], [20], buck–boost [17], or noninverting buck–boost [17], [21], [22] converters were presented, and four types of single-inductor multiple-input single-output topologies based on buck [23], boost [24], buck–boost [23], and noninverting buck–boost [25] converters were proposed. In addition, their counterpart MIMO converters were developed in [26]–[32] by simply connecting multiple additional input/output branches in parallel. Although the existing topologies can provide favorable performances for the specified applications, they cannot always be the best choices for various applications with different system requirements. For example, for the applications having several inputs/outputs with different voltage/power levels, the direct parallel connection of additional input/output branches is usually not a good solution. Actually, in order to effectively select a preferred converter for an engineering application, as many viable topologies as possible should be provided and compared. However, until now, the principle to derive SI-MIMO topologies is kept unclear, and only a limited number of topologies is available.

From the abovementioned information, SI-MIMO converters have the advantages of low cost and high power density, which are attractive in the engineering applications. Their control strategies have been widely discussed in the relevant researches to improve the dynamic characteristics. But for the topology configurations, only several ones are available, and more viable topologies are desired so that a preferred one can be selected out after comprehensive comparison. With this demand, a novel principle of deriving a large number of SI-MIMO topologies from typical buck, boost, buck–boost, and noninverting buck–boost SISO converters is proposed in this article. Only three steps are needed, and thus it is simple to be implemented. To gain a better understanding, a family of SI-SIDO, single-inductor dual-input single-output (SI-DISO), and single-inductor dual-input dual-output (SI-DIDO) topologies are derived and demonstrated, including the ones presented in [17]–[22]. Besides, the obtained SI-SIDO boost converters are taken as an example to be compared, and an optimum one is finally chosen for a specific application, whose performance analysis, design considerations, and simulation/experiment verification are also illustrated in detail.

II. PRINCIPLE AND TOPOLOGY DERIVATION

In this section, the principle and topology derivation of SI-MIMO converters from the typical buck, boost, buck–boost, and noninverting buck–boost SISO converters in Fig. 1 will be depicted in detail, which only needs three steps and thus can be implemented easily. Besides, some of the derived topologies can be further simplified under appropriate working conditions to obtain reduced number of semiconductor devices.

A. Principle

First, three basic MIMO cells (MIMO_1, MIMO_2, and MIMO_3) with p outputs and q inputs are proposed in Fig. 2, according to the fundamental operation principle and topology structure of the existing SI-MIMO converters. By connecting multiple inputs/outputs and unidirectional switches with the outflow, inflow, or both ports of inductor, as shown in Fig. 2(a)–(c), the current \( i_L \) will be multiplexed and will flow into different inputs/outputs during the time interval when their corresponding switches conduct.

Second, integrate the MIMO cells shown in Fig. 2 with the inductor branch of buck, boost, buck–boost, and noninverting buck–boost converters. In order to achieve a unified topology derivation process, the inductor branch of four typical SISO converters are expressed in a general form, as shown in Fig. 3(a). According to Fig. 1, the values of \( m \) and \( n \) are either 1 or 2. Then, the integration of one MIMO cell and the inductor branch is depicted in Fig. 3(b)–(d). For the MIMO_1 cell, it is added at the outflow port of inductor, and an extra unidirectional switch is added in each original branch \( B_{o1}−B_{on} \). These additional
switches along with the switches in MIMO_1 cell are used to ensure that inductor current $i_L$ can only flow into one path at any time. The integration is similar for the MIMO_2 cell, as shown in Fig. 3(c), whereas it is a little different for the MIMO_3 cell. From Fig. 3(d), only an extra unidirectional switch is needed for the integration of MIMO_3 cell, because it is parallel connected with the inductor. Moreover, two or three different MIMO cells can also be simultaneously integrated with the SISO converters in a similar manner, as shown in Fig. 4. It is noted that the extra unidirectional switch consisting of a MOSFET and a diode as $v_s$. If it is larger than or equal to zero all the time, the diode will always be forward biased, and thus it can be removed. On the other hand, if $v_s$ is always less than or equal to zero, the parallel diode of MOSFET conducts all the time, and it can also be removed.

B. Topology Derivation

With the abovementioned principle, various SI-MIMO converters can be easily derived. Taking the combination of boost converter and MIMO_3 cell with one output branch ($p = 1$, $q = 0$) as an example, its detailed topology derivation process is demonstrated in Fig. 6. After integrating MIMO_3 cell with the boost converter in Fig. 6(a), the extra unidirectional switches are moved to connect in series with switch $S_1$ and diode $D_s$, as shown Fig. 6(b). According to the simplification shown in Fig. 5, the reduplicated MOSFET and diode are deleted in Fig. 6(c). Then, by turning ON the switch $S_1$, $S_2$ and $S_3$ one-by-one, the inductor current $i_L$ will flow into a different path in a switching period. When $S_1$ is OFF, the voltage across $D_{s1}$ and $S_1$ is equal to $V_{o1}$ plus $V_{i1}$ in the interval with $S_2$ and $S_3$ ON, respectively. Therefore, it is always larger than zero, and the diode $D_{s1}$ can be further removed. Finally, a viable SI-SIDO topology is derived in Fig. 6(d). To the best knowledge of the authors, this topology has not been reported in previous researches.

In addition, Tables I and II also summarize a family of SI-SIDO and SI-DISO converters derived from typical buck, boost,
TABLE I
FAMILY OF SI-SIDO CONVERTERS DERIVED FROM BUCK, BOOST, BUCK–BOOST, AND NONINVERTING BUCK–BOOST CONVERTERS

| (i) buck | (ii) boost | (iii) buck-boost | (iv) non-inverting buck-boost |
|----------|------------|------------------|-----------------------------|
| ![Diagram](image1) | ![Diagram](image2) | ![Diagram](image3) | ![Diagram](image4) |

According to Fig. 1, except for the two nodes of inductor, there are two other nodes in the buck, boost, and buck–boost converter, and hence two corresponding topologies can be respectively obtained for them by integrating one MIMO_1 or MIMO_2 cell.

It is noted that the SI-SIDO/SI-DISO buck–boost topologies consisting of MIMO_1 or MIMO_2 cells are the same, because its outflow and inflow ports of the inductor are equivalent. For the noninverting buck–boost converters, there are three other nodes, and likewise, three topologies are derived with MIMO_1 or MIMO_2 cell. In these SI-SIDO/SI-DISO topologies, several ones have been presented in [17]–[22], and the rest are first found with the proposed principle in this article. Because their performance characteristics are different, engineers can select a preferred one for a specified application after comprehensive comparison, which is very beneficial for the practical design.

Moreover, with the increasing number of ports, more viable SI-MIMO topologies can be developed. Taking the SI-DIDO topologies based on a boost converter as an example, it has 25 viable topologies in total, which can be classified into 6 types in terms of the different MIMO cells. An example topology is respectively demonstrated in Fig. 7. In Fig. 7(a)–(c), two same MIMO cells are added in the boost converter simultaneously, whereas two of three cells are combined in Fig. 7(d)–(f). In comparison with the SI-MIMO converters that have multiple additional inputs/outputs only connecting in parallel [26]–[31], the characteristics of additional ports in the newly obtained buck–boost, or non-inverting buck–boost converters using the proposed topology derivation method. 5, 5, 3, and 7 viable SI-SIDO/SI-DISO topologies are respectively obtained, among which there is always one including MIMO_3 cell.
SI-MIMO topologies are diverse and thus can be a better solution for the application with different inputs/outputs.

C. Further Discussion

Actually, some of the above derived SI-MIMO topologies can be further simplified if they work under appropriate voltage conditions. According to Fig. 5, the MOSFET or diode will become useless in their series-connected structure if its voltage is always positive or negative and, thus, can be deleted. Taking the SI-SIDO converters based on boost converter in Table I(ii) as an example, topologies presented in (b), (c) and (e) can be, respectively, simplified into the ones presented in Figs. 8–10, when the corresponding relationships among $V_{i1}$, $V_{o1}$, and $V_{o2}$ are satisfied. After simplification, the number of required semiconductor device is reduced and so is the conduction losses.

III. TOPOLOGY COMPARISON AND PERFORMANCE ANALYSIS

A. Topology Comparison

After deriving various SI-MIMO topologies, their performance characteristics will be compared and then an optimum one could be selected out for a specified application. As an example, the obtained SI-SIDO topologies based on a boost converter presented in Table I(ii) and Figs. 8–10 will be detailed compared in this section. Afterward, topology selection is conducted for a specific application with input voltages $V_{i1} = 18–30$ V, output voltages $V_{o1} = 60$ V, $V_{o2} = 24$ V. Because $V_{o2}$ is always smaller than $V_{o1}$ and $V_{o1} - V_{i1}$, the SI-SIDO boost converters presented in Table I(ii)-(a) and -(d) and Figs. 8(a), 9(a), and Fig. 10(a) can be employed. Their comparison results in terms of the average inductor current $I_L$, the working condition, and the semiconductor devices are summarized in Table III.

For the topologies presented in Table I(ii)-(a) and Fig. 8(a), their average inductor currents are smaller, which is equal to the input currents $I_{i1}$, and the number of active semiconductor devices in conduction is also smaller. However, their working conditions are limited. The output current $I_{o2}$ must be less than $I_{o1}$ in Table I(ii)-(a), and the relationship between $I_{o1}$ and $I_{o2}$ is restricted under the condition with $V_{o2} < V_{i1}$ in Fig. 8(a), e.g., $I_{o1}$ cannot be no-load with $V_{o2} < V_{i1}$, otherwise the inductor will be always charged. In a word, although the topologies presented in Table I(ii)-(a) and Fig. 8(a) are favorable in terms of the average inductor current and semiconductor devices, they
Fig. 7. SI-DIDO topologies based on boost converter with different MIMO cells. (a) MIMO_1 + MIMO_1. (b) MIMO_2 + MIMO_2. (c) MIMO_3 + MIMO_3. (d) MIMO_1 + MIMO_2. (e) MIMO_1 + MIMO_3. (f) MIMO_2 + MIMO_3.

Fig. 8. Further simplification of the SI-SIDO boost converter in Table I(ii)-(b) with voltage relationships. (a) \( V_{o1} > V_{o2} \). (b) \( V_{o1} < V_{o2} \).

Fig. 9. Further simplification of the SI-SIDO boost converter in Table I(ii)-(c) with voltage relationships. (a) \( V_{o2} < V_{o1} - V_{i1} \). (b) \( V_{o2} > V_{o1} - V_{i1} \).

Fig. 10. Further simplification of the SI-SIDO boost converter in Table I(ii)-(e) with voltage relationships. (a) \( V_{o2} < V_{o1} - V_{i1} \). (b) \( V_{o2} > V_{o1} - V_{i1} \).

Fig. 11. Proposed SI-SIDO converter and its equivalent circuits in different working stages. (a) Converter. (b) \([t_0, t_1]\) in both DCM and CCM, \([t_3, t_4]\) in DCM. (c) \([t_1, t_2]\) in both DCM and CCM. (d) \([t_2, t_3, t_5, t_6]\) in DCM. (e) \([t_4, t_5]\) in DCM, \([t_2, t_3]\) in CCM.

Table III

| Topology | \( I_L \) | Working Condition | Semiconductor Devices |
|----------|----------|-------------------|-----------------------|
| Table 1 (ii)-(a) | \( I_{o1}, I_{o2} \) | \( I_{o1}, I_{o2} > I_{i1}, I_{i2} \) | 2S2D 1S+1D+1S1D |
| Fig. 8(a) | \( I_{o1}, I_{o2} \) | \( I_{o1}, I_{o2} > I_{i1}, I_{i2} \) | 2S2D 1S+1D+1S1D |
| Fig. 9(a) | \( I_{o1}, I_{o2} \) | \( I_{o1}, I_{o2} > I_{i1}, I_{i2} \) | 2S2D 1S1D+1S1D+2D |
| Table 1 (ii)(d) | \( I_{o1}, I_{o2} \) | \( I_{o1}, I_{o2} > I_{i1}, I_{i2} \) | 2S2D 2S+2D+1S1D+1S1D |
| Fig. 10(a) | \( I_{o1}, I_{o2} \) | \( I_{o1}, I_{o2} > I_{i1}, I_{i2} \) | 2S2D 1S+1D+1S1D |

Note. S: switch, D: diode

are not suitable for the specific application due to the restricted working conditions. The undesired restriction is avoided in the topologies presented in Fig. 9(a), Table I(ii)-(d), and Fig. 10(a). And \( I_L \) is equal to \( I_{o1} + I_{o2} \) in all these three converters. Their differences mainly lie in the number of active semiconductor devices in different working stages. From Table III, all working stages have two active semiconductor devices in the topologies presented in Fig. 9(a) and Table I(ii)-(d), whereas only one stage has two and the rest two stages have one in the topology presented in Fig. 10(a). Therefore, thanks to the smaller number of active semiconductor devices in conduction and consequently lower conduction losses, the topology presented in Fig. 10(a) is chosen for the specific application.

B. Operation Analysis

The proposed SI-SIDO topology shown in Fig. 10(a) is redepicted in Fig. 11(a). It can operate in DCM, as shown in Fig. 12(a), or CCM, as illustrated in Fig. 12(b). \( v_{gs1} \) and \( v_{gs3} \) are the drive signals of \( S_1 \) and \( S_3 \), respectively. \( i_{L1}, i_{s1}, i_{s3}, \) and \( i_{D2} \) are the inductor current, drain-to-source currents of \( S_1, S_3 \), and current of \( D_{s2} \), respectively. The corresponding equivalent
Stage 4 ($t_3$-$t_4$): At $t_3$, switches $S_1$ and $S_3$ are turned on. The operation in this stage is the same as that of stage 1.

Stage 5 ($t_4$-$t_5$): At $t_4$, switch $S_1$ is turned off. Because $S_2$ is on and $V_{o2} + V_{t1}$ is smaller than $V_{o1}$, the diode $D_{s3}$ will turn to be forward biased, and the inductor current $i_L$ commutes to output $V_{o2}$, as shown in Fig. 11(e). In this stage, inductor $L$ is discharged by $-V_{o2}$, and thus the inductor current $i_L$ decreases. The diode $D_{s2}$ and switch $S_1$ are, respectively, clamped by $V_{o1} - V_{t1} - V_{o2}$ and $V_{t1} + V_{o2}$.

Stage 6 ($t_5$-$t_6$): At $t_5$, the inductor current $i_L$ decays to zero, which is the same as that of stage 3.

From above, the proposed SI-SIDO converter shown in Fig. 11(a) operates as a typical boost and buck-boost converter in turn during different half switching periods $T_s/2$. Then, the voltage relationships among $V_{o1}$, $V_{o2}$, and $V_{t1}$ can be correspondingly obtained in (1). From (1), by adjusting the duty cycles $D_1$ and $D_2$, the output voltages $V_{o1}$ and $V_{o2}$ can be independently controlled. In addition, the power $P_{o1}$ and $P_{o2}$ of two outputs $V_{o1}$ and $V_{o2}$ are calculated in (2), which can also be, respectively, controlled by the duty cycles $D_1$ and $D_2$.

\[
\begin{align*}
V_{o1} &= \left(1 + \frac{1}{1 + \frac{2D_2 T_s R_3}{L}}\right) V_{t1} \\
V_{o2} &= \sqrt{\frac{R_2 T_s}{2L D_2}} V_{t1} \\
P_{o1} &= \frac{V_{o1}^2 V_{t1}}{2(L(V_{o1} - V_{t1}))} D_1^2 \\
P_{o2} &= \frac{V_{o2}^2 T_s}{2L} D_2^2
\end{align*}
\]

(1)\(\quad\) (2)

where $R_1$ and $R_2$ are the output resistances of $V_{o1}$ and $V_{o2}$, respectively.

2) CCM Operation: According to Fig. 12(b), a switching period $T_s$ includes three stages $[t_0, t_1]$ in CCM. The stages $[t_1, t_2]$, $[t_2, t_3]$ and $[t_3, t_4]$ of CCM are, respectively, similar to the stages $[t_0, t_1]$, $[t_1, t_2]$, and $[t_2, t_3]$ of DCM, except that the inductor current $i_L$ is continuous instead of discontinuous. The inductor current flows to the first output $V_{o1}$ during the stage $[t_1, t_2]$ and flows to the second output $V_{o2}$ during the stage $[t_2, t_3]$. Then, with the neglect of inductor current ripple, equation $i_L = V_{o1}/R_1/(1 - D_3) - V_{o2}/R_2/(D_3 - D_1)$ is derived. In addition, the inductor is charged by $V_{t1}$ in the stage $[t_0, t_1]$ and is discharged by $V_{t1} - V_{o1}$ and $-V_{o2}$ in the stage $[t_1, t_2]$ and $[t_2, t_3]$, respectively. Then, equation $D_1 V_{t1} = (1 - D_3)(V_{o1} - V_{t1}) + (D_3 - D_1)V_{o2}$ can be obtained according to the flux balance of inductor. With the abovementioned two equations, the voltage relationship between $V_{o1}$, $V_{o2}$, and $V_{t1}$ is calculated in (3). From (3), both $V_{o1}$ and $V_{o2}$ are determined by $D_1$, $D_3$, $R_1$, and $R_2$. Therefore, severe cross-regulation problem will be incurred under load variation. In order to improve the dynamic response, the existing proposed solutions, such as control loop decouple [33], [34], multivariable control [35], predictive control [36]-[38], and deadbeat control [39], can be employed, but with increased complexity.

\[
\begin{align*}
V_{o1} &= \left(1 + \frac{1}{1 + \frac{2D_3 T_s R_2}{L}}\right) V_{t1} \\
V_{o2} &= \sqrt{\frac{R_2 T_s}{2L D_2}} V_{t1} \\
P_{o1} &= \frac{V_{o1}^2 V_{t1}}{2(L(V_{o1} - V_{t1}))} D_1^2 \\
P_{o2} &= \frac{V_{o2}^2 T_s}{2L} D_2^2
\end{align*}
\]

(3)
Fig. 13. Design considerations in DCM. (a) Inductance L. (b) Duty cycles D1 and D2. (c) iL(t1), iL(t4), and iL_rms. (d) I_{s1_rms} and I_{s3_rms}.

| Parameter          | Value          | Parameter          | Value          |
|--------------------|----------------|--------------------|----------------|
| Input Voltage V_{i1} | 18–30 V       | Inductance L_{i1}  | 30 µH/DCM     |
| Output Voltage V_{o1} | 60 V          | Switches S_{i1,3}  | IPP530N15N3   |
| Rated Output Current I_{o1_{\text{rat}}} | 0.5 A       | Diodes D_{o2}      | MBR20200CT    |
| Output Voltage V_{o2} | 24 V          | Switching Period t_{s} | 40 µs     |
| Rated Output Current I_{o2_{\text{rat}}} | 0.5 A       |                   |               |

Table IV

| Parameter | Value |
|-----------|-------|
| L_{o}     | 30 µH |
| L_{i1}    | 1.4 mH |
| L_{i2}    | 1.4 mH |

IV. DESIGN AND EXPERIMENT VERIFICATION

In order to verify the theoretical analysis, a prototype circuit of the proposed SI-SIDO converter, shown in Fig. 11(a), with system parameters, presented in Table IV, is built. In this section, its design considerations in both DCM and CCM are explained first. Then, the simulation and experiment results under input voltages V_{i1} = 18 and 30 V are demonstrated.

A. Design Considerations

In DCM, the peak inductor current i_{L}(t_1) and i_{L}(t_4) are obtained in (4) from the performance analysis in previous section. Then, according to the average output current I_{o1} = i_{L}(t_1) \times (t_2 - t_1)/2 and I_{o2} = i_{L}(t_2) \times (t_5 - t_4)/2, the values of t_2-t_1 and t_5-t_4 are calculated in (5), and they should be less than T_s/2. Based on this requirement, the available inductance L is calculated in (6) and is depicted in Fig. 13(a) with the aforementioned system parameters. The available inductance varies with different input voltages V_{i1}, for example, L \leq 74 µH for V_{i1} = 30 V, whereas L \leq 37 µH for V_{i1} = 18 V. Because the DCM operation is demanded to be guaranteed under whole input voltage range, the smallest range of inductance L should be selected, i.e., L \leq 37 µH. Besides, with the consideration of margin and nonideal parameters in the practical circuit, the inductance L is finally designed as 30 µH. Then, the duty cycles D_1 and D_2 are derived in (7) from (1) and are also demonstrated in Fig. 13(b). They decrease with the increment of input voltage V_{i1}. Afterward, substituting (7) into (4), the peak inductor currents i_{L}(t_1) and i_{L}(t_4) as a function of V_{i1} are illustrated in Fig. 13(c), which, respectively, obtain maximum value 7.48 A and 5.66 A at V_{i1} = 18 V. Moreover, according to Fig. 12, the root-mean-square (rms) value of inductor current I_{L_{rms}} and drain-to-source current I_{s1_{rms}} and I_{s3_{rms}} are obtained in (8). Their maximum values 3.57, 2.89, and 1.37 A are also obtained at V_{i1} = 18 V, as shown in Fig. 13(c) and (d). And from Fig. 11(a), the average current I_{DS2/3} of D_{s2/3} is equal to the average currents I_{o1} and I_{o2}, respectively. On the other hand, the maximum drain-to-source voltages of S_1 and D_2 are V_{o1} and V_{o2}, and the voltage stresses of S_3 and D_3 are V_{o1} - V_{i1} - V_{o2} and V_{i1} + V_{o2}, respectively. Based on aforementioned analysis, a ferrite core EI-28 with 12 turns is employed to implement the inductor L, MOSFET IPP530N15N3 is chosen as switches S_1 and S_3, and MBR20200CT is employed as diode D_{s2} and D_{s3} in the prototype circuit

\[
\begin{align*}
I_{L_{rms}} &= \frac{V_{o1}^2 V_{o2}^2}{8 V_{o1}^2 I_{o1}^2} \left( \frac{D_{s2}}{2T_s R_1} \right)^2, \quad D_2 = \frac{V_{o2} + V_{o2}^2}{V_{i1} + V_{o2}^2} \left( \frac{2L}{R_2 T_s} \right) \quad (7) \\
I_{s1_{rms}} &= \frac{D_{s1}}{3} i_{L}(t_1)^2 + \frac{D_{s2}}{3} i_{L}(t_4)^2, \\
I_{s3_{rms}} &= \frac{I_{s1_{rms}} - I_{s2_{rms}}}{3 T_s} i_{L}(t_4)^2
\end{align*}
\]

In CCM, the required inductance is different from that in DCM, whose value is designed to ensure that the ripple current \Delta i_L of inductor in (9) is less than 20% of its average value I_{L}. Similarly, according to the system parameters presented in Table IV, the inductance is designed as 1.42 mH. In addition, the voltage stresses of semiconductor devices are the same as that in DCM, whereas their current stresses are decreased due to the smaller ripple current. Hence, the MOSFET IPP530N15N3 and diode MBR20200CT are still used

\[
\begin{align*}
\Delta i_L &= \frac{V_{i1} D_{s1} T_s}{L}, \\
I_L &= \frac{V_{o1} I_{o1} + V_{o2} I_{o2} + V_{i1} I_{o2}}{V_{i1}} \quad (9)
\end{align*}
\]
In addition, according to Fig. 16, the steady voltage stresses $v_{s3}$ and $v_{D2}$, which are, respectively, decreased and increased with the increase in $v_{11}$. It is noteworthy that the oscillation of $v_{s3}$, $v_{D2}$, $v_{s3}$, and $v_{D3}$ during the interval when $i_L$ = 0 is caused by the resonance of the inductor $L$ and the parasitic capacitors of semiconductor devices.

Fig. 17 also depicts the measured efficiencies of the proposed converter at different input voltages $v_{11}$. Because there are two conducting switches/diodes in only one stage while one switch/diode conducts in the rest two stages, the number of active semiconductor devices in the proposed converter is small. Therefore, low conduction losses are achieved, contributing to high efficiencies. In Fig. 17, the minimum efficiency is 0.919, and the maximum efficiency is 0.98. It is noteworthy that the practical efficiencies would be a little decreased with the consideration of the loss of drive circuits.

Likewise, experiment waveforms of the proposed converter in Fig. 11(a) working in CCM are also illustrated in Figs. 18–20, which are in well coincidence with the theoretical analysis. Unlike the discontinuous currents in DCM, the inductor current is continuous in CCM. Hence, the oscillation of $v_{s1}$, $v_{D2}$, $v_{s3}$, and $v_{D3}$ would not appear, as shown in Fig. 20. However, because of the hard-switching operation of switches and the reverse-recovery process of diodes, spike turn-off/on voltage and currents are incurred in Figs. 19 and 20.

Besides, the dynamic response under load variation in DCM and CCM are shown in Fig. 21(a) and (b), respectively. In DCM, the two outputs are independently controlled and thus the variation of $i_{o1}/i_{o2}$ only has an influence on $v_{o1}/v_{o2}$. Also, the simulation results of dynamic response under input voltage variation in DCM are also shown in Fig. 22, which is similar.
Fig. 19. Experimental waveforms of inductor current $i_L$, drain-to-source currents $i_{s1}$ and $i_{s3}$, and diode current $i_{D2}$ at different $v_{i1}$ in CCM. (a) $v_{i1} = 18$ V. (b) $v_{i1} = 30$ V.

Fig. 20. Experimental waveforms of drain-to-source voltages $v_{s1}$ and $v_{s3}$ and diode voltages $v_{Ds2}$ and $v_{Ds3}$ at different $v_{i1}$ in CCM. (a) $v_{i1} = 18$ V. (b) $v_{i1} = 30$ V.

Fig. 21. Experimental waveforms of dynamic response under load variation. (a) DCM. (b) CCM.

Fig. 22. Simulation waveforms of dynamic response under input voltage variation in DCM.

Fig. 23. Photograph of prototype SI-SIDO converter shown in Fig. 11(a).

V. CONCLUSION

In this article, a simple principle of deriving SI-MIMO topologies from typical buck, boost, buck–boost, and noninverting buck–boost converters with only three steps was revealed. And as an example, a family of SI-SIDO, SI-DISO, and SI-DIDO topologies was derived and demonstrated in detail. With the proposed principle and the obtained SI-MIMO topologies, more choices are available and then an optimum one can be selected out for an engineering application. In addition, a family of SI-SIDO boost converters were also taken as an example to be compared under input voltages $V_{i1} = 18$–30 V and output voltages $V_{o1} = 60$ V and $V_{o2} = 24$ V, and a preferred one with lower conduction losses was finally selected, analyzed, and validated experimentally.

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