Research and optimization design of voltage divider biasing circuit based on PSpice

Jincheng Wu*, Jingrui Sun, Mingcheng Liu

College of Electronic and Communication Engineering, Tianjin Normal University, Tianjin, China

*Corresponding author e-mail: wdxywjc@tjnu.edu.cn

Abstract. Based on the practical characteristics of the basic course of electronic technology, a new method of optimizing the circuit by using the parameters scanning function of PSpice simulation technology is proposed, which is to perform basic transient scanning on the circuit to meet the basic functions of the amplifying circuit. After discovering the unreasonable technical parameters, the parameters of the circuit are scanned and modified. After correcting the incorrect parameters, the optimized analyze design module is used to optimize the circuit design. The optimal design process and simulation results of the voltage-divided bias amplifier circuit by this method are presented. The experimental results show that the optimal design of the amplifying circuit can not only meet the performance parameters required by the constraints and target conditions but also reduce the number of optimization iterations and simulation execution by adjusting the performance specifications of the circuit, thus improving efficiency and accuracy of the optimization design. At the same time, it also verifies the effectiveness and feasibility of optimizing the circuit and design through the simulation.

1. Introduction

In the teaching of basic courses of analog electronic technology, the small signal analog amplifier circuit is a fundamental and difficult to understand the circuit, even if the circuit parameters designed according to the requirements are completely correct, the transistor parameters are caused by the aging of components and temperature changes. The change will cause the instability of the quiescent operation point, resulting in unstable circuit output, because the quiescent operation point not only determines whether the circuit will produce nonlinear cutoff and saturation distortion but also affects the AC dynamic parameters such as voltage amplification and input resistance. Among the factors that cause unstable power supply voltage fluctuations, component aging, peripheral component parameter mismatch and temperature variation at the quiescent operation point, the influence of temperature and circuit peripheral component mismatch on the internal parameters of the transistor is the most important. The voltage-dividing bias circuit with negative feedback overcomes the variation of the transistor parameters due to parameters such as temperature variation and component mismatch and increases the stability of the Q point through the negative feedback circuit, thereby making the circuit output more stable[1].
2. Circuit working principle and parameter setting

2.1. The working principle of voltage divider biasing circuit

According to the basic design idea and requirements of the voltage-dividing bias circuit shown in Fig. 1[2], for the silicon transistor, $I_{R_{B2}}=(5\sim10) I_B$ can generally be selected in the estimation, but the $I_{R_{B2}}$ cannot be too large. Too large, $R_{B2}$ will become smaller, causing the input resistance to become smaller, which increases the power loss. Select $V_B=(5\sim10) U_{BE}$. If $V_B$ is too large, $V_E$ will increase accordingly, causing $V_{CE}=V_{CC}-I_{RC}\cdot V_E$ to be too small, and the output voltage dynamic range will become too small.

![Figure 1. Schematic diagram of voltage division bias circuit.](image)

The circuit parameters designed according to the above requirements are not subject to changes in the external environment, such as temperature and other parameters. If there is no simulation circuit, the parameters such as $V_B$, $I_{R_{B2}}$, $I_B$, and $V_{CE}$ are taken point by point by observing the oscilloscope or by manually changing the $R_{B1}$ or $R_{B2}$ values, insufficient precision, it also takes a lot of time, because these parameters change, mutual constraints and influence each other, it is very difficult to complete, and using the simulation software PSpice can very quickly follow the design requirements through the parameter scanning and optimization function is very good complete the circuit design [3].

2.2. Quiescent operation point $Q$ value obtained by transient scanning

When $R_{B1}=R_{B2}=10k$, $\beta=37.5$. Through the DC simulation as shown in Fig.2, it is found that $V_{CE}=7.155-4.984=2.171V$, close to the saturation region, resulting $\beta=I_C/I_B=2423/69.38=34.92$ and the original value $\beta$ is also somewhat different, the distortion-free dynamic range is very small. For the analysis of an amplifying circuit composed of transistors, it is first necessary to determine the operating state of the transistor. If it is in the amplification area, the parameters such as the magnification of the calculation circuit are meaningful. Otherwise it has no meaning. When the transistor is switching, it ensures that the transistor operates in the non-linear region to be turned off and saturated.

![Figure 2. Transient scanning voltage and current value](image)
2.3 Get the best dynamic range by parameter scanning

Through the formula $V_{cc} \approx V_{cc} - I_C (R_C + R_e)$ analysis, this is because the $V_{ce}$ caused by the $I_C$ is too small, and because $I_C = \beta I_B$, so the $I_B$ current should be reduced, then only increase the $R_{B1}$ value, through the simulation software, the parameter scanning function is very convenient [4]. It sets the $R_{B1}$ value as a parameter. When the $R_{B1}$ value is changed to the corresponding $V_{ce}$ and changes to approximately equal to $1/2V_{cc}$, as shown in Fig.3, the waveform is selected as $V_{cc} = V_{cc}/2 = 6V$. The corresponding $R_{B1}$ value is approximately $20k\Omega$. Just as the circuit works in Class A mode, it is also the desired output dynamic range.

As shown in Fig.2, the setting parameter scan $R_{B1}$ is changed from $5k$ to $30k$, and when the simulation output waveform as shown in Fig.3 is observed, when $V_{CE} = V_{CC}/2$, $R_{B1} = 20k$, the parameter scan is selected as shown in Fig.4, $I_{RB2} \approx (5 \sim 10) I_B$, $V_B \approx (5 \sim 10) U_{BE}$, the values are shown in Table 1;

![Figure 3. Parameters setting the scanning waveform](image)

![Figure 4. Corresponding voltage and current value](image)

### Table 1. The relative voltage and current value.

| $R_{B1}(k \Omega)$ | $I_{RB2}/I_B$ | $V_B/V_{BE}$ | $V_{CE}(V)$ | $V_B(V)$ |
|---------------------|----------------|--------------|-------------|----------|
| 6.36                | 5              | 10           | 0           | 6.75     |
| 18                  | 8.9            | 6            | 5.41        | 4        |
| 20                  | 9              | 5.7          | 6           | 3.73     |
| 24.3                | 9.4            | 5            | 6.85        | 3.25     |
| 30                  | 10             | 4.32         | 7.8         | 2.79     |
Observe by Table 1 when $R_{B1}=18\text{K} \sim 20\text{KΩ}$, $V_{CE}=5.41 \sim 6\text{V}$, $I_{RB2} \approx 9I_B$, $V_B=5.7U_{BE}$; meet the design requirements.

According to the specific design requirements, according to Table 1, the corresponding adjustments can be made within the required range of the circuit.

The theoretical calculation of the voltage divider biasing amplifying circuit formula (1) ~ (5) corresponds to the static value in the simulation shown in Fig.5, the error positive and negative $\leq 6.9\%$ meet the qualitative analysis and quantitative estimation requirements [4].

$$
U_E \approx \frac{V_B - V_E}{R_E} = \frac{4 - 0.7}{2K} \approx 1.65mA 
$$

(2)

$$
I_B = \frac{I_E}{1 + \beta} = \frac{1.65mA}{1 + 37.5} \approx 43\mu A
$$

(3)

$$
I_C = \beta I_C = 37.5 \cdot 43\mu A \approx 1.6mA
$$

(4)

$$
V_{CE} = V_{CC} - I_C (R_C + R_E) = 12 - 1.6(2K + 2K) \approx 5.6V
$$

(5)

3. Circuit AC parameter scanning and calculation

3.1. Parameter scanning of amplitude

After the circuit design is completed, the amplitude of the input signal $u_i$ should not be too large to avoid the working range of the amplifying circuit exceeding the linear range of the characteristic curve.
The amplitude is set as a parameter, and the parameter input is used to observe when the $u_i$ input is 1mv ~ 15mv when the increase is 3mv, observe the maximum undistorted output voltage. By scanning the amplitude parameter, when the input voltage is at most 10 mv as shown in Fig.6, the corresponding output 696 mv is not distorted. When the input is greater than 10mv, the output is distorted. On this basis, it can also be subdivided by parameter scanning until the best is correct. As shown in Fig.7, when $u_i$=10 mv, $u_o$=696 mv, the output voltage is 180 degrees different from the input voltage phase.

![Figure 7. Input and corresponding output voltage waveforms](image)

### 3.2 Simulation of AC parameters

The input resistance 594 ohm and the voltage amplification factor $A_U(\text{max}) = \frac{u_o}{u_i} = 58$ to 82 as shown in Fig.8 is shown by the AC scanning of the circuit; the output resistance $R_o = 1.93$ k ohm is shown in Fig.9. And use the formula to calculate $r_i = R_B1 \parallel R_B2 \parallel r_{be} = 20k \parallel 10k \parallel 0.85k = 0.75k$ ohm; $r_o = R_C = 2k$ ohm; $A_U(\text{max}) = -\beta(\frac{R_C}{R_L})/r_{be} = -37.5 \times (2k // 6k)/0.85k = -66$, meeting the estimation requirements;

![Figure 8. Input resistance and amplitude frequency characteristic curve](image)

![Figure 9. Output resistance waveform](image)

### 3.3 Parameter scanning of bypass capacitor $C_E$

The lower limit cutoff frequency can be changed by changing the emitter bypass capacitor $C_e$. When $C_e$ is 50uF, $f_L = 212.194$hz, $f_H = 18.933$Mhz is observed by scanning.
The pass band \( B_W = f_H - f_L = 18.9328 \text{ Mhz} \). If the value of the emitter bypass capacitor \( C_e \) is adjusted by parameter scanning, as shown in Fig.10 at \( C_1 = C_2 = 10 \mu \text{F}, R_E = 2 \text{ K ohm} \), the lower limit cutoff frequency of the circuit is adjusted, and the corresponding values are shown in Table 2.

### Table 2. The effect of \( C_e \) change on frequency response.

| \( C_e (\mu \text{F}) \) | IF voltage gain (dB) | \( f_L \) (Hz) | \( f_H \) (Mhz) |
|--------------------------|----------------------|----------------|---------------|
| 40                       | 38.34                | 252.23         | 18.76         |
| 50                       | 38.34                | 206.77         | 18.76         |
| 60                       | 38.34                | 176.43         | 18.76         |

#### 3.4. Optimized design of bypass capacitor \( C_e \)

After completing the above circuit design, it is observed through the parametric scanning simulation that as the emitter bypass capacitor \( C_e \) becomes larger, the lower limit cutoff frequency becomes smaller, and the design requirements are met, but if the designed circuit is to be optimally designed. At this time, the PSpice Optimizer module is called to automatically adjust the current design value of the emitter bypass capacitor \( C_e \), so that the circuit lower limit frequency \( f_L \) is accurately improved, and the circuit is optimized[7]. The optimization module amplification circuit is shown in Fig.11.

#### Figure 11. Optimization module amplifying circuit

When the current design index is \( C_e = 50 \mu \text{F} \), the lower limit frequency is about 206.73Hz. According to the requirements of the optimization accuracy \( f_L = 210 \pm 1\% \text{ Hz} \), the capacitor \( C_e \) can be used as an adjustable component. The setting of the component parameters to be adjusted is implemented by executing the PSpice/Place Optimizer Parameters subcommand, and the setting constraint \( C_e \) changes from 40\( \mu \text{F} \) to 60\( \mu \text{F} \) with an accuracy of 10\%. The output of the optimization
module is shown in Fig.12. The system undergoes 3 iterative operations, 5 circuit simulations, and the lower limit of the design index when $C_e=49.1227\mu F$ is to be adjusted. The frequency $f_L=210Hz$ meets the optimization design requirements.

![Image of the output of the module]

**Figure 12.** Optimizes the output of the module

4. Conclusion

The PSpice simulation software is used for the comprehensive research and design of the voltage divided bias amplifier circuit by the functions of transient, AC scanning, parameter scanning, and optimization. By using the calculation method of qualitative analysis and quantitative estimation of an electronic circuit, it is proved that the computer simulation software is used to simulate and analyze the circuit, which saves time. From the intuitive output waveform, a large amount of experimental data is processed, which can be a very good application to the analysis and design of the actual circuit [7]. Using this software, students can be motivated to learn interest and enthusiasm. Before doing specific experiments, they can be simulated first. If the design function is not up to or is unreasonable, it can be easily and repeatedly modified on the computer until it is correct. In this way, before the experiment, there will be a certain understanding of the experimental results, so that the experiment has a deep and broad understanding of the experiment, so as to achieve the purpose of the experiment and the future to the society.

Acknowledgments

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