Faster Schrödinger-style simulation of quantum circuits

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ABSTRACT
Recent demonstrations of superconducting quantum computers by Google and IBM and trapped-ion computers from IonQ fueled new research in quantum algorithms, compilation into quantum circuits, and empirical algorithmics. While online access to quantum hardware remains too limited to meet the demand, simulating quantum circuits on conventional computers satisfies many needs. We advance Schrödinger-style simulation of quantum circuits that is useful standalone and as a building block in layered simulation algorithms, both cases are illustrated in our results. Our algorithmic contributions show how to simulate multiple quantum gates at once, how to avoid floating-point multiplies, how to best use instruction-level and thread-level parallelism as well as GPU cache, and how to leverage these optimizations by reordering circuit gates. While not described previously, these techniques implemented by us supported published high-performance distributed simulations up to 64 qubits. To show additional impact, we benchmark our simulator against Microsoft, IBM and Google simulators on hard circuits from Google.

1 INTRODUCTION
Quantum computation was first developed theoretically to accelerate computational bottlenecks using quantum-mechanical phenomena [1]. Among several promising quantum models of computation, quantum circuits have been implemented in several technologies, for which end-to-end programmable computation has been demonstrated at intermediate scale [2]. In 2019, Google claimed quantum-computational supremacy [3, 4] by scaling quantum computation to the point where simulating it becomes exceptionally challenging even on supercomputers. The significance of quantum design automation tools has been appreciated for many years, to the point where IBM and Microsoft have developed extensive toolchains (Qiskit and QDK respectively), which include language support, compilation, optimization, and a variety of execution back-ends for physical quantum computers and circuit simulators. Just like in conventional Electronic Design Automation, such software allows one to validate prototype designs before building the hardware. Quantum circuit simulation in general is inherently difficult due to the exponential growth in the number of internal parameters and complexity-theoretic reasons [5, 6]. We distinguish several categories and uses of quantum-circuit simulation:

(1) Polynomial-time simulation of "easy" special-case quantum circuits — those using Clifford gates [7], many instances of Grover’s algorithm [8], and circuits with small tree-width [9]. Such simulation is used to (i) rule out quantum speed-up in specific algorithms, and (ii) for limited initial testing of quantum computers in the lab and debugging of failed tests.

(2) Best-effort simulation of unrestricted “small” quantum circuits up to 40 qubits, illustrated in Section 6. Such simulation is used (i) for broad testing and routine debugging of quantum computers, (ii) to verify local quantum circuit transformations and whole circuits, as well as (iii) to evaluate new quantum algorithms, quantum error-correcting codes and device architectures [10]. In particular, VQE algorithms common for quantum-chemistry applications run numerous quantum circuits in a sequence, their development particularly benefits from fast simulation.

(3) Distributed quantum-circuit simulation on clusters and supercomputers [11, 12, 14–18], including the world’s largest [19]. Such expensive and scarce resources are used to verify quantum computation and set performance baselines when claiming quantum-computational supremacy [3, 4, 17]. Whereas other uses entail repeated on-demand simulations on readily available computing hardware, this category targets a small number of “expensive” one-off simulations.

All three categories of quantum-circuit simulation are in demand today, but high-performance simulation of unrestricted quantum circuits in Categories 2 and 3 is challenging and motivates algorithmic improvements of the type we propose. Using fast simulation to evaluate, verify, test and debug larger quantum circuits and algorithms facilitates the development of many applications. Schrödinger-style simulation is the mainstream technique for general-case simulation of quantum algorithms, circuits and physical devices. It represents a quantum state (wave function) by a vector of complex-valued amplitudes and modifies this vector in place by applying quantum transformations (quantum gates, laser pulses, algorithm modules, etc). Schrödinger simulation

- scales linearly with computation (circuit) depth but exponentially with the number of qubits, or width (Section 6.3);
- is popular for small and mid-size quantum-circuit and device/technology simulations because its unoptimized variants are relatively straightforward to implement;
- dominates supercomputer-based quantum circuit simulations because it can leverage distributed memory, fast interconnect, GPUs, etc [11–16, 18, 19];
- has been extended for better scalability via layered simulation [18, 20, 21]. For example, combining Schrödinger simulation with Feynman path summation enables scaling tradeoffs between circuit depth and width [5] and orders-of-magnitude resource savings in important cases [21].
Our work accelerates both pure Schrödinger simulation and layered algorithms that use it, as we illustrate empirically for Schrödinger-Feynman simulation from [21]. Our algorithmic insights and innovations offer both constant-time implementation speed-ups and algorithmic speed-ups that scale with qubit count:

- Careful selection of the floating-point type backed by numerical accuracy improvements and checks, so as to reduce memory footprint and memory bandwidth.
- Avoiding most floating-point multiplications, in favor of faster additive and bitwise instructions.
- Batched simulation of diagonal quantum gates that significantly reduces expensive memory traversals and the overall runtime, while exposing thread-level parallelism.
- Encoding sets of same-type diagonal gates by bitmasks (Figure 6), simulating them with bitwise and mod-p CPU instructions, as well as leveraging Gray codes in such simulation.
- Encoding sets of same-type single-qubit (not necessarily diagonal) gates by bitmasks (Figure 6) and simulating them using a recursive FFT-like algorithm that improves cache locality and exposes thread-level parallelism.
- The insight that some quantum gates (implemented in superconducting quantum computers) are easier to simulate in pairs because this simplifies matrix elements and benefits from batched load/store operations.
- Gate clustering by type, contrasted with the common gate fusion that clusters heterogenous gates that share qubits. We develop a reordering-based clustering algorithm that finds larger homogenous clusters (Figure 6).
- Implementing our algorithms with extensive use of AVX-2 instructions that improves productivity per instruction.

Our empirical results start with comparisons on smaller circuits where software from IBM and Microsoft can be used, then study the scalability of our techniques and explain how they enrich layered simulation methods. On a MacBook Pro laptop with 16GiB RAM, we simulate circuits with a 5×5-qubit array to any depth, with 20× and 12× speedups over simulators from Microsoft QDK and IBM Qiskit/QASM, respectively. Our simulator Rollright uses 3.27× and 1.7× less memory respectively and can also simulate 6×5-qubit circuits of any depth. On a mid-range server, we simulate up to 6×6-qubit circuits and the illustrate Schrödinger-Feynman simulation [21] that assembles results of multiple half-sized Schrödinger simulations, benefits from our techniques, and shows 700−4000× speedups over QDK and Qiskit. Additional comparisons to the Qsim simulator currently under development at Google help estimating the impact of specific innovations in our work.

The remaining part of the paper is structured as follows. In Section 2 we review minimal background in quantum circuits and introduce relevant quantum gates. Section 3 introduces basic ideas behind Schrödinger-style simulation. Our algorithmic framework is presented in Section 4, including key design decisions and some of the performance optimizations. Section 5 describes several ways in which we leverage the CPU architecture and available hardware resources. Empirical results and scalability studies are reported in Section 6, followed by conclusions in Section 7. Key concepts are illustrated by examples.

## 2 BACKGROUND

A quantum circuit on n qubits is a sequence of quantum gates that act on quantum states represented by 2ⁿ-dimensional complex-valued vectors [1]. The computation usually starts with the basis vector (1, 0, …, 0) which sets each qubit in the |0⟩ state rather than the |1⟩ state. Quantum gates transform this initial n-qubit state into a superposition of 2ⁿ basis vectors (where each vector is labeled by some n-bit binary number j and participates with the complex amplitude αj). Quantum measurements are traditionally performed at the end to stochastically read out non-quantum bits, while destroying the quantum state. The probabilities of measurement outcomes depend on the values αj. In this work, we assume that there is enough memory to represent all of these values, in which case simulating measurements is straightforward. Thus, our task is to find the final values of all αj, also known as strong simulation.

The types of quantum gates used by industry quantum computers include a handful of one- and two-qubit gates. In quantum computers based on superconducting technologies, qubits are often arranged in a planar grid, and two-qubit gates are restricted to nearest-neighbor qubits. Yet, our methods directly handle two-qubit gates acting on any pair of qubits (as in ion-trap computers).

Specific quantum gates are defined by 2×2 or 4×4 unitary matrices [1]. Single-qubit quantum gates include

\[
\text{NOT} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, \quad H = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}, \quad \text{and } Z = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix},
\]

where NOT negates the state of the qubit, H sets the qubit into a superposition of |0⟩ and |1⟩, while Z shifts the phase of the qubit. Multiple qubits can be coupled using the Controlled-NOT (CNOT) and Controlled-Z (CZ) gates:

\[
\text{CNOT} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \end{bmatrix}, \quad \text{CZ} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \end{bmatrix}.
\]

Example 2.1. Figure 1 illustrates a two-qubit circuit with two Hadamard gates around a CNOT gate, followed by measurements on each qubit. The three-gate circuit is equivalent to a CZ gate:

\[
(I \otimes H) \text{CNOT} (I \otimes H) = \text{CZ},
\]

where ⊗ represents the Kronecker product and I represents the identity matrix of appropriate dimension. Given that the CZ gate is diagonal, it maps |11⟩ into −|11⟩ and the remaining three basis vectors to themselves. Therefore, if the circuit starts with any basis vector, the measurement will deterministically produce this vector. In general, diagonal operators/gates do not create superpositions. In many circuits, one-qubit gates create separable superpositions, which diagonal gates then turn into entangled superpositions.

Quantum circuits with only the gates introduces so far (along with P = Z²ⁿ) can be simulated in polynomial time by a compact algorithm, hence they do not offer quantum computational advantage [7]. Among additional gates supported by Google Bristlecone and Sycamore chips [3, 4, 25]

\[
X^{1/2} = \frac{1}{2} \begin{bmatrix} 1 + i & 1 - i \\ 1 - i & 1 + i \end{bmatrix}, \quad Y^{1/2} = \frac{1}{2} \begin{bmatrix} 1 + i & 1 + i \\ -1 - i & 1 - i \end{bmatrix}, \quad T = \begin{bmatrix} 1 & 0 \\ 0 & e^{\pi i/4} \end{bmatrix}.
\]

A similar equation expresses CNOT via CZ and two H gates.

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1. A similar equation expresses CNOT via CZ and two H gates.
Figure 1: Quantum circuit diagrams for equivalent circuits

\( |q_0\rangle \xrightarrow{Z} |q_0\rangle \quad |q_1\rangle \xrightarrow{H} |q_1\rangle \)

\( |q_1\rangle \xrightarrow{H} \)

Fast Schrödinger simulation. For a q-bit gate defined by its \( 2^q \times 2^q \) matrix and circuit qubits \( i_0, \ldots, i_{q-1} \) to which it is applied, a typical simulation algorithm modifies the \( 2^q \)-dimensional state-vector in-place. Such a simulation traverses the state-vector and enumerates all \( 2^{n-q} \) disjoint sets of \( 2^q \) amplitudes, to which the gate can be applied in-place. To specify these sets, we turn to the binary (n-bit) representations of amplitude indices. Each set exhibits all \( 2^q \) combinations of bits indexed \( i_0, \ldots, i_{q-1} \), whereas the remaining \( n-q \) bits are common and form a set id.

Since some gates modify only a fraction of amplitude sets, additional speedups are available by skipping the remaining sets.

Example 3.1. CZ gates are commonly used in circuit design and favored because they are qubit-symmetric and because a CNOT can be expressed via CZ and H gates. To simulate a single CZ gate acting on qubits \( i_0 \) and \( i_1 \), note that it flips the sign of amplitude \( \alpha_j \) when \( j \) has 1s at binary positions \( i_0 \) and \( i_1 \), but otherwise leaves \( \alpha_j \) unchanged.\(^3\) Hence, the simulation traverses all amplitudes, and for each \( \alpha_j \) decides whether to flip the sign based on the bits of \( j \). Such simple linear memory passes benefit from standard CPU caching and prefetching policies.

Universal quantum gate libraries often complement the CZ gate with one-qubit gates [22, 23]. Therefore, a minimal circuit-simulation framework can be completed with an algorithm to simulate an arbitrary one-qubit gate acting on qubit \( i_0 \) (simulating measurements is straightforward from the definition when all amplitudes are available). Diagonal one-qubit gates, such as \( Z \) and \( T \) can be simulated similarly to how we simulate CZ, except that only one bit of the amplitude index \( j \) needs to be considered.

Example 3.2. NOT gates are not diagonal and swap pairs of amplitudes whose indices differ at bit \( i_0 \). One simulates a NOT gate in one pass over the state vector as follows: for each \( j \), if bit \( i_0 \) is zero, swap \( \alpha_j \) with \( \alpha_{j'} \), where \( j' \) differs from \( j \) at bit \( i_0 \) only.

Example 3.3. A generic one-qubit gate can be simulated by isolating the gate action to pairs of amplitudes whose indices differ in one bit only, such as \( 46=b101110 \) and \( 38=b100110 \). Rather than swap these amplitudes (as for NOT gates), it applies the \( 2 \times 2 \) gate matrix. Figure 2 illustrates this with our C++ code, which additionally exploits bitwise instructions for efficiency. To scale this code beyond 64 qubits, our simulator redefines \( \text{idx}_\text{size} \).

4 OUR ALGORITHMIC FRAMEWORK

We now introduce key techniques and optimizations for advanced Schrödinger-style simulation. First, we show how to achieve sufficient numerical accuracy with the 32-bit float type and outline the benefits this brings. Second, we introduce a new gate-clustering approach that forms clusters of gates of a kind. Then we focus on optimizations for each gate type, and point out that clustering can be improved by circuit reordering. To be specific, we use the gate library from Section 2, but the framework supports other common gates too, e.g., by re-expressing them via the gates we consider.

In this context, we emphasize that the runtime of our simulation algorithms scales linearly with the number of gates, regardless of gate type.
4.1 Data type selection and numerical accuracy

Given that state vectors consist of complex-valued amplitudes, the code in Figure 2 assumes a complex-valued type, and we need to choose a floating-point type to implement it. The two basic alternatives on modern computers are the 32-bit float and the 64-bit double. Higher-precision types are also available and have been used for quantum simulation, but significantly increase the computational load. Our choice of the 32-bit float ensures a reduced memory footprint and not only helps to simulate more qubits with limited memory, but also improves memory throughput, which happens to be a bottleneck after simulation algorithms are properly optimized. Most other simulators rely on double, which handicaps them in memory and runtime (see Section 6).

To make our use of float feasible, we need to maintain numerical accuracy during simulation in the face of potential underflows. Among our gates, NOT, Z, CZ, and even T gates do not significantly change the magnitudes of α values, but H, X\(^{1/2}\) and Y\(^{1/2}\) include 1/√2 or 1/2 factors which, after hundreds of gates are applied, can lead to numerous underflows. To avoid underflows, we maintain a global power of 1/√2 to accumulate contributions from individual gates. Specifically, we store a single integer value (starting with 0) and increment it whenever we encounter a factor of 1/√2 (and increment twice for 1/2). This value can be accounted for when reading off α values at the end of the simulation, but that sometimes leads to very large values. Therefore, we “flush” accumulated (1/√2)p when p > 100, back into α. We use a similar counter s for global phase i\(^s\), but it cycles through only four possible values. By inspecting gate matrices in Section 2, one can see that, after factoring out 1/√2, all gates can be simulated without floating-point multiplies to improve both speed and accuracy.

**Example 4.1.** To simulate a T gate without floating-point multiplies, note that the only nontrivial multiplication involves \(\exp(\pi i/4) = (i + 1)/\sqrt{2}\). This multiplication can be realized by first incrementing the p count and then using \((i + 1)z = iz + z = (\text{Re}(z) - 1)z + i(\text{Re}(z) + 1)m(z)\). In other words, add a complex number z to its product by i, the latter computed by swapping the real and imaginary parts and negating the real part. Also see Example 5.1.

As explained in Section 4.2, our simulator rarely deals with T gates one by one, but rather clusters them and simulates entire clusters, eliminating not only floating-point multiplies, but also most floating-point additions and subtractions (using integer arithmetic and bit-parallel instructions instead).

When relying on the compact float type, it is important to explicitly check for accuracy loss. Since quantum states are represented by norm-one vectors, we compute the norm before measurement and check how close it is to 1. In practice, the norm computation itself can introduce greater errors than our simulation, unless done carefully. Indeed, small contributions of individual amplitudes \(α_j\) are accumulated in a much larger running sum. Adding a very small number to a much larger number exposes mantissa limitations. This pitfall can be avoided by representing the running sum during the norm computation by the higher precision double type and/or by representing the running sum with a pair of floating-point values — a common technique for robust arithmetic in numerical analysis [26].

Using pairs of compact float values to represent complex amplitudes offers an additional, less obvious benefit: four pairs of complex numbers can be added by one AVX-2 instruction (see Section 5).

4.2 Gate clustering and bitmask encoding

Prior quantum simulators [14] typically cluster adjacent gates acting on the same qubits (when this is possible) up to 5 qubits, multiply out gate matrices up to \(32 \times 32\), and then optimize matrix-vector multiplication with SIMD multiply-accumulate instructions [14]. Given that we have eliminated most floating-point multiplies for individual gates, adopting this approach would be a step back. However, simulating one gate at a time requires expensive memory traversals. We propose a new gate clustering that considerably reduces memory traversals by forming larger clusters yet still avoids floating-point multiplies and MAC instructions. This is accomplished by clustering adjacent gates of a kind — diagonal gates \((T\) and \(CZ\)) separately from one-qubit non-diagonal gates \((H, X^{1/2}, Y^{1/2})\). While the decision on how to cluster gates (Figure 6) may not seem particularly insightful, it enables bitmask encodings and downstream optimizations with profound impact on simulation performance, as we show in the rest of the paper.

Clustering diagonal gates together and one-qubit gates together brings a number of benefits. Here we rely on the fact that diagonal gates act on individual \(α\) values without permuting or mixing these values. In particular, the order in which diagonal gates are applied (within the cluster) does not matter. Along these lines, the order of one-qubit gates acting on different qubits does not matter. For each type of one-qubit gate, such as T gates, we encode circuit gates in each cluster using bitmasks.

**Example 4.2.** In Figure 6, the four-qubit circuit on the right contains a cluster of T gates on qubits 0-3. This cluster can be represented by the bitmask 15=b1111, neglecting the order in which these gates were listed in the circuit. The same encoding is used for \(X^{1/2}\) gates \((7=b0111)\) and \(Y^{1/2}\) gates \((14=b1110)\).

A single bitmask cannot encode multiple T gates on one qubit, but such gates can be separated into adjacent layers (cycles) and captured using one bitmask per layer. Bitmap encodings of CZ gates are more involved and discussed in Section 4.3.

So far, we explained which gates we cluster and outlined the logic behind the approach. As will be seen in Section 4.3, our use of bitmasks significantly reduces the number of floating-point operations by (i) first consolidating the phases contributed by CZ and T gates to each amplitude index \(j\), and (ii) applying the resulting phases to the amplitudes \(α_j\), when the phases are \(≠ 1\). Additionally, simulating all diagonal gates in one memory pass over amplitudes \(α_j\) reduces memory traffic that is often the main limiting factor when large amounts of memory are used.

Optimizations for non-diagonal gates are covered in Section 4.4. For algorithmic details on gate clustering see Section 4.5.

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\(^{4}\)Clustering gates of a kind helps find hidden gate cancellations. Such gate cancellations sometimes appear in compiled circuits, but not in well-designed simulation benchmarks such as the ones we use in this work [3, 24].

\(^{5}\)The benchmarks used in this work [3, 24] do not include repeated gates.
/ * Returns the 8 phases affected by a set of CZ gates on 8 consecutive amplitudes */
unsigned char GetCZPhaseInBlockUsingGrayCodesAndBitmask(
    idx_size num_qubits,
    // one bitmask per qubit
    idx_size* __restrict__ c_z_bitmasks,
    idx_size block_idx /* block of 8 floats */)
{
    // gc : gray codes
    idx_size prev_GC = (block_idx - 1) * (block_idx - 1) >> 1;
    gc0 = prev_GC, gc4 = (block_idx + 4) * (block_idx + 4) >> 1);
    const idx_size gc[2] = {gc0, gc0, gc0, gc0, gc0, gc0, gc0, gc0} ;
    gc[2] = gc[1] | gc[0] |
    gc[2] = gc[2] ^ 1, gc[2] ^ 3, gc[2] ^ 2, gc[2] ^ 1, gc[2] ^ 3, gc[2] ^ 2);
    unsigned char z_phase_result = 0u;
    // In blocks of 4, indices 0,1,0 capture the application of CZ on the least-sig qubit. */
    const idx_size bit_idx[4] = (__builtin_ctzl(gc[0] ^ prev_GC), 0, 1, 0, __builtin_ctzl(gc[1] ^ prev_GC));
    const idx_size bit_idx[8] = (__builtin_ctzl(gc[4] ^ prev_GC), 0, 1, 0, __builtin_ctzl(gc[5] ^ prev_GC), 0, 1, 0);
    // Get CZ parity for the prev. set of 1-bit indices
    idx_size gate_count = 0;
    for (idx_size i = 0; i < num_qubits; ++i)
        if (((prev_GC & (1ull << i)) == (1ull << i)) && (prev_GC & c_z_bitmasks[i]))
            gate_count += __builtin_popcountll((prev_GC & c_z_bitmasks[i]));
    if (gate_count & 2) z_phase_result |= 1;
    // Update CZ gate state by calculating the new parity in the current block */
    for (int i = 0; i < 8; ++i)
        if (__builtin_popcountll(gc[i] & c_z_bitmasks[i]) == 1)
            z_phase_result |= z_phase_result & (1 << i);
    return z_phase_result
}

Figure 3: Our optimized algorithm for simulating a bitmask-encoded cluster of CZ gates on a block of consecutive amplitudes. It performs a loop-unrolled Gray-code traversal on a block of 8 consecutive indices. The 8 returned phase values determine whether or not to negate each amplitude in the wave function. Compiler intrinsics are explained in Table 1.

4.3 Optimizations for diagonal gates
For a cluster of T and CZ gates, we traverse the entire state vector once. For each amplitude \( \alpha_j \), we calculate the new value after all gates in the cluster are applied. For each gate in the cluster, the task is simple. For example, a T gate acting on qubit \( i_0 \) leaves unchanged those \( \alpha_j \) values where the binary form of \( j \) has 0 at bit position \( i_0 \), and multiplies the remaining \( \alpha_j \) by \( \exp(i\pi/4) \). A CZ gate acting on qubits \( i_0 \) and \( i_1 \) negates \( \alpha_j \) when \( j \) has bit 1 at positions \( i_0 \) and \( i_1 \).

The handling of diagonal clusters can be optimized further. We form \( n \)-qubit layers of T gates, where each layer has at most one gate on any given qubit and can thus be encoded by a bitmask \( m \), where each gate location is represented by a 1 bit. Bitmasks are formed before the memory pass. For each amplitude \( \alpha_j \), each bit of each bitmask may contribute a factor of \( \exp(i\pi/4) \) or a factor of 1. The nontrivial contribution occurs when a 1-bit in bitmask \( m \) matches a 1-bit in index \( j \).

Example 4.3. To count pairs of matching 1-bits between an amplitude index \( j \) and a T-gate bitmask \( m \), two single-cycle CPU instructions suffice: popcount\((m \& j)\). See Table 1 for more details.

Since \( 2^8 = 8 \), the number of matching bits above can be taken mod-8. Applied as a power to \( \exp(i\pi/4) \), this integer yields eight possible values: \( \pm 1, \pm i, (\pm 1 \pm i) / \sqrt{2} \). We multiply by these values using increments of the \( p \) counter, floating-point negations, and swaps of real and imaginary parts (Section 4.1).

To leverage fast bit-based CPU instructions, bitmasks are stored in 64-bit integers when simulating \( \leq 64 \) qubits. Processing dozens of T gates in a cluster by several bit-based operations per amplitude is much more efficient than simulating gates one by one.

To simulate CZ gates, each CZ gate can be encoded by a bitmask \( m \) with two nonzeros, such bitmasks stored in a list (as long as the number of CZ gates). Then for each \( \alpha_j \) and each CZ gate, we can check if \( m \& j \equiv m \) bitwise, in which case we increment a counter of contributions. Since each CZ gate can contribute only a factor of 1 or -1, contributions can be aggregated and then we can either apply the resulting -1 or do nothing (saving a memory write).

When dealing with large clusters of CZ gates on \( n \) qubits, a more efficient approach is to use (up to \( n - 1 \)) bitmasks that can capture multiple gates each. For qubit \( k > 0 \), the bitmask \( m_k \) represents (qubits \( k < j \) of) CZ gates that also act on qubit \( k \). To each \( \alpha_j \), these gates can cumulatively contribute phase 1 or -1, which we determine by aggregating parity\((1\ll j)\) over all \( k \) such that \( j \& (1\ll k) \neq 0 \).

Example 4.4. Consider a cluster of six CZ gates that couple all pairs of four qubits. This cluster is encoded by the following set of bitmasks (one per qubit): \( m_1 = \{1000, 1100, 1100, 1100\} \). Note that there are exactly six nonzero bits total across these bitmasks.

A further optimization uses Gray codes. Specifically, we traverse \( \alpha_j \) in a Gray code order, so that \( j \) changes one bit at a time to minimize necessary updates. In this work, we use the more-common reflected Gray code that can be produced from a regular counting sequence \( k = 0, 1, 2, 3, \ldots \) with bit operations \( j = k \oplus (k \gg 1) \).

Example 4.5. The three-bit reflected Gray code uses codewords \( \{000, 001, 011, 010, 110, 101, 100, 011, 010, 110, 101, 100\} \). Note that this code is cyclic — the first and the last values differ in one bit. It can be obtained from its first half by setting the most significant bit to 1 and reflecting the first half.

Given a pattern of CZ gates in a bitmask-encoded cluster, we precompute which CZ gates become active (-1) or inactive (1) when each bit switches. When processing blocks of indices, instead of index calculations from scratch, we incrementally update the “state” from the previous block. This technique reduces the complexity of amplitude updates from \( O(n) \) to \( O(1) \) time, after initialization.

Figure 3 implements the ideas above, using advanced CPU instructions via compiler intrinsics (Table 1). The code works with
 bitmask-encoded CZ gates and finds the implied Z phase changes for a block of 8 amplitude indices. Returned as a byte, these 8 bits determine if respective amplitudes must be negated. The function can be used in a thread-parallel traversal of the wave function in conjunction with aligned memory reads (see Section 5).

Other common diagonal gates can be simulated natively or by expressing them via supported gates, e.g., $P = T^2$ and $Z = T^4$.

### 4.4 Optimizations for non-diagonal gates

Recall that all non-diagonal gates in our gate library are one-qubit gates. If one wanted to simulate a CNOT gate, it can be re-expressed using a CZ gate and two $H$ gates on the sides. Thus, we are now simulating the following gates (leading factors extracted):

$$H' = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}, \quad X' = \begin{bmatrix} 1+i & 1-i \\ 1-i & 1+i \end{bmatrix}, \quad Y' = \begin{bmatrix} 1+i & 1 \\ -1-i & 1+i \end{bmatrix}$$

When different gate types are applied on the same qubit, their order matters. However, gates applied on different qubits can be reordered. Thus, we cluster gates of each kind into layers, and represent each layer by a bitmask $m$. Since applying gates one at a time is inefficient, we apply them two at a time. While this requires fetching more data at a time, the resulting matrices

$$H' \otimes H' = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix}, \quad Y' \otimes Y' = \begin{bmatrix} i & 1 & 1 & 1-i \\ i & 1 & 1-i & 1 \\ 1 & 1-i & i & 1 \\ 1-i & 1 & i & i \end{bmatrix}$$

use mostly $\pm 1$ and $\pm i$ as their entries and can be multiplied by without floating-point multiply and MAC instructions. For example,

```c
template<typename function>
void Apply2QGates(cmplx* __restrict w, // wave function 
                 size_t gate_qubits, int num_qubits,
                 function& gate_func, idx size collected_amps /* = 4 
when gate_func is in AVX-256 */) {
  const size_t num_idxs = 4, w_size = 1ull << num_qubits,
  gate_bitmask = (1ull << ((num_qubits - 1) - 
                  __builtin_ctzl(gate_qubits))) |
  (1ull << ((num_qubits - 1) - (63 - 
                  __builtin_clzl(gate_qubits))));

  array<size_t, num_idxs> starting_idxs;
  /* Get starting indices into the wave function to 
  start applying the gates on */
  GetFirstSetOfIndicesInWToApplyGate(num_qubits,
  starting_idxs.data(), gate_qubits);

  w = (cmplx*)__builtin_assume_aligned(w, 64);
  size_t iters = 0, idx = 0;
  array<size_t, num_idxs> temp_idxs;

  const size_t num_iters = w_size / num_idxs;
  while (iters < num_iters) {
    /* Skip block where the gate has already been 
    applied. This is where the bits in the wave 
    function index are 1 at the position of the 
    qubit value. */
    if (!((idx & gate_bitmask)) {
      iters += collected_amps;
      /* Increase the starting indices by idx to 
      progress through the wave function */
      for (idx size i = 0; i < num_idxs; ++i)
        temp_idxs[i] = starting_idxs[i] + idx;
      gate_func(w, temp_idxs.data());
      idx += collected_amps;
    } else idx += (idx & gate_bitmask);
  }
}
```

Figure 4: Our algorithm for extracting the first set of indices of the wave function to apply a generic $k$-qubit gate on qubits specified by the bitmask. Other sets of indices are obtained by shifting the first set, as shown in Figure 5. See Table 1 for compiler intrinsics.
multiplying a complex value $a_k$ by the imaginary $i$ entails a swap of the real and imaginary parts and one negation. Using such observations, we have developed several algorithms in the spirit of Figure 2. A common pattern in these algorithms is that the two-qubit gate combination acts each time on four amplitudes whose indices differ by two bits. To extract such indices, we find the first set using the code in Figure 4 and obtain the remaining sets by shifting the indices as shown in Figure 5.

Our first implementation uses a generic gate_func as in Figure 2, but is not limited to one-qubit gates. As shown in Figure 5, it extracts sets of amplitude indices, then for each set loads the amplitudes from the wave function, applies gate_func to them and saves the result back into the wave function. Our second implementation in Section 5.3 uses the same index-extraction mechanism, but increases instruction-level parallelism via custom code for each pair of one-qubit gates (hence, no generic gate function is passed).

### 4.5 Gate clustering by reordering

To perform clustering outlined in Section 4.2, we assume a quantum circuit specified by a list of gates given by their matrices and qubits on which they act (Section 2). The gates are ordered so that gate $g_k$ whose output qubit acts as input to gate $g_l$ appears before $g_k$, but parallel gates can be ordered either way. Such topologically sorted orders are generally not unique. Moreover, diagonal gates can always be reordered without affecting circuit functionality. Google benchmarks [3, 24] additionally pack parallel gates into numbered “cycles”, but we ignore this additional structure.

When gates of a kind are adjacent in the given gate ordering, they form a natural cluster. However, we also find non-adjacent gates of a kind that can be reordered to form larger clusters. The search proceeds from the beginning of the circuit in topological order. Start with a gate $g_k$ that cannot be in a cluster formed before (such as the first gate in the circuit) and assume that no gates after it can be in a cluster formed before (or else they would have been reordered). The inner loop of the algorithm (for a fixed $g_k$) finds gates that cluster with $g_k$ and reorders them accordingly. The outer loop goes over all yet-unclustered gates $g_k$. The state of the inner loop designates each qubit as unobstructed (initially) or obstructed. An obstructed qubit prevents a gate of the same type as $g_k$ from being reordered to be adjacent to $g_k$.

The inner loop scans (traverses) gates after $g_k$, classifies each gate $g_l$ in one of three categories and performs the following actions:

1. a gate of the same kind as $g_k$ — if all of the gate’s qubits are unobstructed, then reorder the gate toward $g_k$ to form a larger cluster, else mark all of the gate’s qubits obstructed;
2. a gate $g_l$ of a different kind that can be reordered with $g_k$ — do not change qubit designations because gates of the same kind as $g_k$ can be reordered past $g_l$ towards $g_k$;
3. a gate that cannot be reordered with a $g_k$ — mark all of the gate’s qubits as obstructed.

The scan from $g_k$ continues until all qubits are marked as obstructed or all gates have been scanned. Upon the completion of the scan, all qubits are reset to unobstructed, and the next iteration of the outer loop focuses on to the next gate not in a cluster. This algorithm is guaranteed to put each gate in the circuit into a cluster (single-gate clusters are allowed).

**Example 4.6.** The circuit in Figure 6 starts (and ends) with a cluster of Hadamards, unchanged during reordering. When the outer loop focuses on the $CZ$ gate on qubits 0-1, it reorders the other $CZ$ gate to be adjacent. This step relies on the fact that $CZ$ and $T$ gates are both diagonal, and so can always be swapped. The second iteration clusters $T$ gates. Subsequent iterations cluster $X^Y$ and $Y^Y$ gates.

The reordering-based clustering is performed once at the beginning of simulation with negligible impact on runtime. Striving for larger clusters, we put $X^Y$ and $Y^Y$ gates into the same clusters (consider them gates of a kind), especially that $X^Y \otimes Y^Y$ is as simple to multiply by as other Kronecker products above.

### 5 LEVERAGING THE CPU ARCHITECTURE

Additional efficiencies are available by enhancing memory locality, optimizing algorithms for the CPU cache size (“blocking”), leveraging instruction-level parallelism, and using multiple CPU threads.

#### 5.1 Memory locality and CPU cache blocking

Given that we have eliminated most floating-point multiplies and simulate large groups of diagonal gates with fast CPU instructions, performance bottlenecks shift towards memory operations. Notable performance losses are due to cache misses, especially when...
Table 1: Compiler intrinsics used to accelerate simulation of specific gate types.

| Instruction Type               | Compiler Intrinsics | Use in Simulation |
|--------------------------------|---------------------|-------------------|
| Aligned read/write            | mm256_load_ps      | For all gates, loads/stores amplitudes between RAM & registers. |
|                               | mm256_store_ps     |                   |
| Packed 32-bit float arithmetics | mm256_add_ps       | Used with $X^{1/2}$, $Y^{1/2}$, and $H$ gates. AVX multiplication with $T$ gates. |
|                               | mm256_sub_ps       |                   |
|                               | mm256_mul_ps       |                   |
| Multiply 32-bit floats, then add/subtract | mm256_fadd_ps     | Optional with $T$ gates. |
|                               | mm256_fsub_ps      |                   |
| Bitwise opd on packed 32-bit floats | mm256_xor_ps      | With $X^{1/2}$, $Y^{1/2}$, $H$ gates. |
|                               | mm256_or_ps        |                   |
| Packed 32-bit floats swizzle  | mm256_shuffle_ps   | Used to rearrange real and imaginary parts of complex amplitudes for arithmetic optimizations. |
|                               | mm256_permute_ps   |                   |
| Assume aligned                | builtin_assume_aligned | In most kernels lets the compiler optimize for aligned vectors. |
| Count trailing, leading 0-bits | builtin_ctzl       | Used to extract indices and apply bitmasks. |
|                               | builtin_clzl       |                   |
| Count 1-bits                  | builtin_popcountll | Used with $CZ$ and $T$ gates, also to extract data from bitmasks. |
| Parity of 1-bit count         | builtin_parityll   | Used with $Z$ and $CZ$ gates, with Gray codes. |

Applying one-qubit gates (diagonal gates require a small number of linear memory passes). To improve memory locality, we take special care when forming pairs of one-qubit gates. First, the gates of each kind in a layer are sorted by the qubits they act upon. Then, we form pairs in order, so that paired up gates act on as close qubits as possible. This reduces memory strides when simulating gate pairs acting on less significant bits.

A more sophisticated optimization is blocking. Rather than apply pairs of one-qubit gates in separate passes, such pairs acting on different qubits can be reordered and even applied partially in different orders. Simulating gates that act on more significant bits still suffer from long memory strides and frequent cache misses. To also address those gates, we developed a recursive FFT-like algorithm for simulating layers of one-qubit (non-diagonal) gates of a kind. Shown in in Figure 7, this algorithm starts with the most significant qubits and simulates gates acting on those qubits (if they exist), after which it partitions the state vector into equal-sized chunks and recurses to individual chunks. Chunks are chosen to have the smallest size such that the most significant one-qubit gate

const int kRT = 8 * sizeof(idx_size) + 1;
inline int GetNextUsedQubitIndex (const idx_size bitmask) {
    return bitmask ? __builtin_ctzl(bitmask) : kRT;
}
*/

size X_bitmask, idx_size Y_bitmask, int num_qubits, int num_threads) {
    
    const int idx_increment = 4; idx_size i_phase = 0;
    if (X_bitmask & 1 || Y_bitmask & 1) {
        idx_size gates_bitmask = 0;
        // Move the bitmask so the next two qubits are the least significant and find whether to apply XX, XY, YX, YY.*

        int gate_type = UpdateXYBitmask(X_bitmask, Y_bitmask, gates_bitmask, i_phase);
        Apply2QGates(w, gate_type, gates_bitmask, num_qubits, idx_increment);}

    const int k = min(GetNextUsedQubitIndex(Y_bitmask),
                      GetNextUsedQubitIndex(X_bitmask));
    // Base condition : end-case when qubit index == 65.
    // RT only supported for up to 64 bits indices here.
    if (k != kRT) {
        const idx_size iters = 1ull << k,
        stride = 1ull << (num_qubits - k);
        X_bitmask >> k; Y_bitmask >> k;
        idx_size temp_i = 0;
        for (idx_size i = 0; i < iters; ++i)
            temp_i += XYFastTransform(w + (i * stride),
                                        X_bitmask, Y_bitmask, num_qubits - k, num_threads);
        i_phase += temp_i / iters;
    }
    return i_phase % 4;
}

Figure 7: Our recursive transform (RT) algorithm illustrated by applying combinations of $X^{1/2}$ and $Y^{1/2}$ gates.

left can be applied within a chunk. Upon recursion, the algorithm applies multiple non-overlapping pairs of one-qubit gates to each chunk and moves on to the next chunk. When each chunk fits in L2 cache, cache misses are reduced and performance is improved.

5.2 Thread-level parallelism

The recursive FFT-like algorithm has the added benefit of exposing data parallelism after simulating gates that act on the most significant qubits. Therefore, different branches of recursion can be processed by different CPU threads. Additionally, memory traversals used when simulating diagonal gates expose significant data parallelism. We invoke parallel threads using OpenMP pragmas.
with our C++ code, so that the code runs sequentially when pragmas are ignored. In practice, this brings a 3-4x speedup with 8 threads, after which threads become memory-starved.

5.3 Instruction-level parallelism

Major performance gains are achieved in our work with aligned memory reads and writes. Such CPU instructions fetch 256 bits of data (four complex numbers), but require data alignment to sufficient powers of two. To unlock these optimizations, we had to give up the use of C++ STL vector classes and instead resorted to C-style arrays whose memory positioning can be controlled more precisely. Fortunately, all large arrays in quantum circuit simulation are sized at large powers of two, and can therefore be perfectly aligned using a small amount of address arithmetic. When simulating diagonal gates, each pass becomes faster because the number of reads and writes is reduced (here we use Gray codes only within each 256-bit block). When simulating pairs of one-qubit gates, our memory traversal pattern is enhanced by cache blocking via the recursive FFT-like algorithm in Figure 7. Recall that pairs of one-qubit gates are applied to four amplitudes at a time, but those four amplitudes are not contiguous in general. Therefore, we load an entire cache line for each, so that four aligned reads provide data for applying two gates to four sets of amplitudes.

With data loaded in chunks (typically cache lines), we made a concerted effort to leverage wide arithmetic operations from the AVX-2 instruction set. Relevant CPU instructions accessed through compiler intrinsics are listed in Table 1. In order to prepare registers for AVX-2 arithmetics, 32-bit values may need to be shuffled using several types of bit permutations. CPU cycles can be reduced by optimizing data shuffles and by reducing the number of arithmetic operations. The latter is facilitated by common sub-expression elimination and matrix factorizations.

Example 5.1. Our AVX-2 kernel used to simulate paired $X^{1/2}$ gates is illustrated in Figure 8. The diagonal of the $X^{1/2} \otimes X^{1/2}$ matrix (Section 4.4) implies multiplication by $1-i$. Figure 8 shows how to implement such multiplies with fast permutation and XOR instructions. In particular, _mm256_permute_ps and _mm256_xor_ps execute in a single cycle on Intel CPUs, whereas multiplication takes 3-5 cycles depending on the CPU. Without method, the four amplitudes would have to be multiplied by $(1-i)$ each and then four more loads would be required to complete the add and subtract operations with the original amplitudes. Our approach saves at least twelve CPU cycles for a pair of $X^{1/2}$ gates. The add and subtract AVX-2 instructions in Figure 8 complete in 24 cycles.

Customizing (to each gate type) such permutations, arithmetic instructions and read-write instructions is a very laborious process that requires careful optimization and testing. In particular, we have studied assembly code generated from our compiler intrinsics to understand how to perform the same work with fewer CPU cycles. These efforts are justified by serious performance benefits. In addition to better arithmetic performance, aligned memory reads and writes improve memory bandwidth and help keep more CPU threads supplied with data.

```c
void ApplyXX12GateAVX(cmplx* __restrict w, // wave function
                       const float* __restrict t_w =
                       // temp wave function
                       float* __restrict t_w =
                       // Permute real and imaginary numbers
                       t2 = _mm256_permute_ps(t2, 0b10110001);
                       t3 = _mm256_permute_ps(t3, 0b10110001);
                       a0 = _mm256_add_ps(t0, t2);
                       a1 = _mm256_add_ps(t0, t3);
                       a2 = _mm256_add_ps(t0, t2);
                       a3 = _mm256_add_ps(t0, t3);
                       _mm256_store_ps(t_w + 2*target[0], a0);
                       _mm256_store_ps(t_w + 2*target[1], a1);
                       _mm256_store_ps(t_w + 2*target[2], a2);
                       _mm256_store_ps(t_w + 2*target[3], a3);
```

Figure 8: Optimized AVX-2 code to apply the $X^{1/2} \otimes X^{1/2}$ gate on four amplitudes loaded onto CPU registers. Code for the $Y^{1/2} \otimes Y^{1/2}$ gate is simpler due to its simpler matrix, as seen in Section 4.4. Compiler intrinsics are explained in Table 1.

6 SIMULATION COMPARISONS

This work targets circuits that run on NISQ computers [2] and are therefore limited in the number of qubits. Among such circuits, many well-known examples are fairly easy to simulate [8]. Therefore, we focus on recent quantum-supremacy circuits from Google [24] that were designed to ensure difficulty of simulation [25]. The average-case difficulty of their simulation has since been proven analytically [6], and the benchmarks have been revised [21, arxiv:1807.10749] to remove unintended simulation shortcuts. On the other hand, our Schrödinger simulator does not exploit some of the well-known features of these benchmarks that simplify simulation, such as their planar-grid qubit layout with nearest-neighbor qubit couplings, or the knowledge of specific gate patterns. Table 2 shows characteristics of the benchmarks, including their large T-gate counts, which defeat stabilizer-based simulation techniques.
| Circuit depth | Gates all | Gates 2-q | T | Microsoft QDK time | Microsoft QDK mem MiB | QISKit-Terra QASM time | QISKit-Terra QASM mem MiB | Rollright time | Rollright mem MiB | Ratios QDK/RR time | Ratios QDK/RR mem MiB | Ratios QISkit/RR time | Ratios QISKit/RR mem MiB |
|---------------|----------|----------|----|-------------------|-----------------------|------------------------|--------------------------|---------------|----------------|-----------------|---------------------|-----------------|---------------------|
| 16q           | 274      | 78       | 68 | 2.34              | —                     | 1.59                   | —                        | S < 0.1       | —              | —               | —                   | —                | —                   |
| 24q           | 417      | 123      | 99 | 16.64             | 463                   | 9.87                  | 176.34                  | S 0.88       | 128            | 18.91           | 3.63                | 11.22            | 1.38                |
| 25q           | 435      | 130      | 105| 28.72             | 972                   | 18.3                 | 432.36                  | S 1.45       | 256            | 19.81           | 3.80                | 12.62            | 1.69                |
| 30q           | 524      | 161      | 119| —                 | OOM                   | —                     | OOM                      | S 58.8       | 8192           | —               | —                   | —                | —                   |
| MacBook Pro 2017 – MacOS High Sierra: 16 GiB, Intel Core i7-7700HQ (2.80GHz) 4 cores 8 threads |
| 16q           | 524      | 161      | 119| 1213.16           | 23959                 | 212.25                | 15925                   | —            | —              | —               | —                   | —                | —                   |
| 24q           | 524      | 161      | 119| 1213.16           | 23959                 | 212.25                | 15925                   | —            | —              | —               | —                   | —                | —                   |
| 30q           | 524      | 161      | 119| 1213.16           | 23959                 | 212.25                | 15925                   | —            | —              | —               | —                   | —                | —                   |
| 32q           | 560      | 168      | 168| 1213.16           | 23959                 | 212.25                | 15925                   | —            | —              | —               | —                   | —                | —                   |
| 32q           | 560      | 168      | 168| 1213.16           | 23959                 | 212.25                | 15925                   | —            | —              | —               | —                   | —                | —                   |
| 36q           | 633      | 195      | 144| —                 | OOM                   | —                     | OOM                      | —            | —              | —               | —                   | —                | —                   |
| Server – Ubuntu Linux: 144 GiB, Intel Xeon Platinum 8124M (3.00GHz) 18 cores, 72 threads |

Table 2: Comparisons of our simulator Rollright to the simulator from Microsoft QDK v0.11.2006.403 and IBM QISkit-Terra v0.5.7 benchmarks from Google (v2) [3, 24] with up to 36 qubits, performed on a laptop and a mid-range server. Memory usage is the increase in max resident memory versus the baseline 16-qubit simulation, to exclude code-segment size.

6.1 Validation and basic performance

We implemented proposed algorithms in C++17 in a package called Rollright and compiled the codes with Clang v11.0.3. As described in Section 5.3 we use AVX-2 instructions that are commonly available on commodity and server CPUs. Results reported in this paper do not use GPUs, but use SIMD and thread parallelism.

To ensure correctness of simulation results, we saved all amplitudes of final states (for several circuits with 20-25 qubits) and compared them to amplitudes produced by several industry and academic simulators. For circuits with 30-36 qubits, we saved a small number of amplitudes and cross-checked them against results obtained by the authors of Google benchmarks independently.

Software development and some of the experiments were performed on a MacBook Pro 2017 laptop with 16 GiB RAM, where our baseline Schrödinger simulation completes a 30-qubit circuit with depth 1 + 26 + 1 in 72 s using a little over 8 GiB of RAM (1+ and +1 denote initial and final layers of Hadamard gates as in Figure 6). On the laptop, we use a single CPU process with eight threads. For simulations on a mid-range server with ample memory (Tables 2 and 3) we use multiple CPU processes (with eight threads each) to leverage available hardware threads.

In terms of actual performance, Rollright spends negligible time on I/O and circuit pre-processing, i.e., gate reordering and forming clusters. Most of the runtime is spent simulating clusters of diagonal and non-diagonal gates. For runtime profiling, we distinguish non-diagonal gates acting on the more and the less significant qubits. To illustrate, consider a 5 × 6-qubit Google circuit of depth 1 + 26 + 1, where simulating X1/2 and Y1/2 gates on the more significant qubits took > 75% of runtime. CZ, T gates, along with remaining X1/2, Y1/2, and H gates took only 14.4% runtime.

In addition to pure Schrödinger simulation, our techniques can be used to accelerate layered simulation algorithms [18, 20, 21] that handle a greater variety of circuits. For example, divide-and-conquer algorithms leverage Schrödinger simulation of n = 32-qubit blocks to simulate 2n = 64-qubit circuits [21]. Tables 2 and 3 show results for both pure Schrödinger and Schrödinger-Feynman simulation [21] with our optimizations included.

6.2 Comparisons to Microsoft, IBM and Google

We compared our simulator to the Microsoft Quantum Development Kit (QDK) v0.2.1806.3001 and IBM QISKit-Terra v0.5.7. Microsoft QDK includes a back-end circuit simulator and front-end support for the Q# language, integrated with Microsoft Visual Studio and available on Windows, MacOS and Linux. IBM QISKit includes several simulators, and we found the QASM simulator to be faster than the state-vector simulator on quantum-supremacy circuits [3, 24]. We performed empirical comparisons to our simulator Rollright on circuits of depth 1 + 26 + 1 with up to 36 qubits, as shown in Table 2. To exclude code segments from memory comparisons, we first measured max resident memory for each simulator on the 16-qubit benchmark and then used those measurements as baselines. Differences in memory usage are on the order of 2× and are mostly explained by our use of single-precision floats. Rollright’s runtime advantage is much greater and grows with the number of qubits.

Given that for 30-qubit circuits Microsoft and IBM simulators required > 16 GiB memory available (Rollright used a little over 8 GiB), we also used a multicore Linux server with sufficient memory and observed that the Microsoft and IBM simulators used all available threads. The optimizations proposed in this work apply to both Schrödinger and Schrödinger-Feynman simulation, therefore we evaluated Rollright in both modes. Clearly, the Schrödinger-Feynman simulation offers a much greater advantage in both runtime and memory on circuits of depth 1 + 26 + 1. The 32-qubit circuit uses the oblong 4 × 8 qubit array, and the Schrödinger-Feynman mode of our simulator is able to exploit this shape. Therefore, we also show results for Schrödinger-Feynman simulation on an even-sided 6 × 6 qubit array. Our comparisons to software from IBM and Microsoft have been presented in person at these companies.

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6 The runtime of simulation with Rollright is consistent among different circuits of similar size, which makes concerns about benchmark post-selection moot.
We also compared our simulator to the Qsim simulator under development at Google (https://github.com/quantumlib/qsim), which we compiled using the same compiler we used for Rollright. According to the authors, Qsim clusters one-qubit gates to nearby two-qubit gates and uses AVX-2 instructions to simulate resulting generic two-qubit gates one by one. Qsim lacks our optimizations for diagonal and one-qubit gates, as well as the FFT-like algorithm that optimizes memory access. Following our prior collaboration with Google [21], Qsim supports the same simulation modes as Rollright — Schrödinger and Schrödinger-Feynman, — which facilitates more detailed apples-to-apples comparisons. Runtimes in Table 3 (shared with Qsim authors) were collected on the same server as for the lower half of Table 2. While Google Qsim outperforms IBM Qiskit and Microsoft QDK on Google benchmarks, Rollright remains ahead, confirming the impact of our proposed methods.

### 6.3 Scalability studies and use models

The results in Table 2 show massive advantage of Schrödinger-Feynman simulation, but pure Schrödinger simulation remains attractive for deep quantum circuits, e.g., in quantum chemistry applications [10] and/or when supercomputing resources are available [11–16, 18, 19]. Simulating 40-qubit circuits this way would require servers with >8 TiB (now available from Microsoft Azure and Amazon AWS). In the Schrödinger-Feynman mode, memory usage can be kept low (see details in [21]) by serializing the computation, but if massive parallel resources are available, using greater peak memory can decrease the latency of simulation. In the meantime, runtime grows as $2^n_{\text{num qubits}}/2^{n_{\text{depth}}} C$ for a large $C > 0$. Figure 9 uses larger supremacy benchmarks from Google to illustrate these differences between Schrödinger and Schrödinger-Feynman simulation by plotting memory usage and runtime for varied qubit counts and circuit depth. The linear runtime scaling of Schrödinger simulation vs. circuit depth (regardless of gate types) contrasts with the semi-exponential scaling of Schrödinger-Feynman simulation.

While this paper focuses on single-server experiments, distributed Schrödinger-Feynman simulations with Rollright using Google Cloud [21] show that our methods are directly useful to simulate bounded-depth 56- and 64-qubit circuits. Alternatively, our techniques can be directly used in supercomputer-based Schrödinger simulations [19] that are not limited by circuit depth. To this end, results in [20] show how to reduce the simulation of wide but shallow circuits (those with many qubits but low depth) to narrow but deep circuits, where pure Schrödinger simulation does well.

### 7 CONCLUSIONS

Many near-term intermediate-scale quantum (NISQ) computers [2] are currently operating with less than 64 functional qubits, including a recent demonstration of quantum-computational supremacy by Google [4] with 53 qubits. Quantum circuits that run on such computers support a plethora of science experiments [10] and motivate circuit optimization tasks, most of which require support in the form of simulation on conventional computers. For example, recent developments in quantum chemistry offer synthesis methods for quantum circuits that model molecular configurations and help computing their energy levels. While these circuits are intended for NISQ computers, quantum-circuit simulation on conventional computers is crucial to develop and validate advanced quantum technologies, such as quantum-on-quantum simulators [10].

Among the simulation algorithms available, this work focuses on Schrödinger simulation that can be used independently or within layered simulation algorithms [18, 20, 21] that handle a greater variety of circuits. Our algorithmic optimizations collectively provide a hefty speed-up over quantum simulators from Microsoft and IBM on hard circuits from Google. This speedup is not limited by a constant factor, but grows with the number of qubits.

Some of our optimizations are generic and some are tuned to gates used by Google benchmarks [3, 24]. It should be clear that other gates can be natively supported using our techniques and/or by expressing them in terms of the gates we explored. While our evaluation focuses on medium-size circuits which industry
simulators can handle, our contributions are directly useful when simulating circuits with many more qubits as shown in [20, 21]. Our techniques can directly benefit supercomputing simulations, especially those using the same types of circuits and simulation frameworks [19]. However, supercomputers do not support the needs of frequent on-demand simulation during practical work with quantum algorithms, quantum error-correcting code, and/or NISQ hardware. For such uses, better approaches include smaller-scale Schrödinger simulation on single high-mem servers and distributed Schrödinger-Feynman simulation in commercial clouds [21].

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