Klessydra-T: Designing Vector Coprocessors for Multi-Threaded Edge-Computing Cores

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Abstract—Convolutional computation kernels are fundamental to today’s edge computing applications. Interleaved-Multi-Threading (IMT) processor cores are an interesting approach to pursue the highest energy efficiency and lowest hardware cost in edge computing systems, yet they need hardware acceleration schemes to deal with heavy computational workloads like convolutional algorithms. Following a vector approach to accelerate convolutions, this study explores possible alternatives to implement vector coprocessing units in IMT cores, showing the application-dependence of the optimal balance among the hardware architecture parameters.

Since the beginning of computer design history, many processor architecture innovations have pursued maximizing the average number of executed instructions per cycle (IPC). Multiple-issue Out-of-Order (OOO) processors implement complex dynamic scheduling schemes in hardware to improve IPC [8], and with the advent of multi-threaded software applications, the OOO architecture schemes have been adapted to support simultaneous multithreading, dynamically scheduling instructions from different threads on the functional units of the core [8]. A different approach, known as interleaved multithreading (IMT) or barrel-processing [1,3,4], alternates instructions belonging to different execution threads in the stages of a single-issue in-order processor pipeline. In this way, while the maximum throughput remains IPC = 1, no instruction with data dependence on the result of a previous one needs to be executed before that result is available in the register file, thus avoiding instruction stalls without any hardware overhead. As long as the workload of the application can be programmed as multiple independent threads, the IMT approach can sustain IPC = 1 with relatively high clock frequency and high energy efficiency, thanks to the hardware simplicity, which is a desirable goal in embedded edge-computing processors.

To execute computationally heavy applications on the edge, any kind of core needs the additional support of hardware acceleration to sustain the desired performance. In the context of hardware acceleration, two broad classes of approaches exist: hardware units that can autonomously execute entire computation kernels upon memory-mapped commands from the processor core, and instruction acceleration units, sometimes referred to as coprocessors, that take over complex instructions for the processor core and thus are directly sequenced by the core instruction stream. Coprocessors have significantly less communication overhead with the core, yet they can be efficiently exploited only within Instruction Set Architectures that allow extensions dedicated to particular computation domains, such as the RISC-V instruction set architecture [2]. This work addresses the introduction of coprocessor acceleration in IMT cores for edge-computing, targeting energy efficiency and performance. In this context, we specifically address supporting accelerated vector operations to execute convolutional computation kernels, due to their ubiquity in the broad area of deep neural algorithm applications currently found in edge computing [6]. A typical and very general scenario is the execution of multiple...
convolution kernels as multiple-threads, on different portions of input data. In this study, we designed, implemented and evaluated a whole taxonomy of different coprocessor acceleration schemes analyzing them for performance, area efficiency, and energy efficiency.

BACKGROUND
Many previous works reported the design of hardware accelerated microcontroller cores in edge-computing applications. In [7], the PULP project team describes a RISC-V processor with DSP hardware support, targeting near-threshold voltage operation. Also the Diet-SODA design implements a simple approach by running its DSP accelerator in near-threshold regime, and then speed-up the computation by increasing Data Level Parallelism (DLP) through very wide SIMD lanes [9]. Our study is agnostic with respect to supply or bias voltage tuning, purely relying on DLP and TLP for energy efficiency, thus targeting any physical implementation including soft-cores on commercial FPGA devices, as shown in our results. Another work, based on OpenRISC cores, introduced a hardware convolution engine for image processing [12], focusing on identifying the optimal buffer size to store a selected portion of the input image. Our study adopts a different approach based on coprocessors equipped with scratchpad memories, coupled with an IMT processor, to hide memory latency. Also in [10,11], energy efficient accelerators were designed to be efficient by making highly parallel hardware units and minimizing off-chip data movements by reusing on-chip loaded data. In these works, the architectural concept is a subset of those covered in our study. Our work builds on the activity reported in [5], that was an initial effort into designing a mathematical accelerator for a RISC-V core, and in [4], that addressed the best performing pipeline organization for an IMT RISC-V core.

THE KLESSYDRA-T IMT ARCHITECTURE
The processing core discussed in this article, named Klessydra-T13, is a parametric design implementing an IMT four-stage-pipeline RISC-V processor. It supports the RV32IMA instruction set [2], augmented by a custom extension composed of a small subset of mathematical vector instructions. The Klessydra-T13 core (Figure 1) implements a pure IMT paradigm as defined by the following points:

- Thread context switch at each clock cycle
- in-order, single issue instruction execution
- feed-forward pipeline structure (no hardware support for branching-hazard and data-hazard handling)
- bare metal execution (RISCV M mode)

The core interleaves three hardware threads (harts [2]) in its four-stage instruction pipeline. For multi-threading support, the register file, program counter, and CSR unit are replicated per hart. A hardware context counter (hartc) switches between the program counters of the three harts on a rotating basis to fetch instructions from the program memory. The three harts in the four pipeline stage provide a register file access fence, such that it is never possible for any two

![Figure 1 Klessydra T13 block organization](image-url)
instructions to manifest a dependency hazard in the pipeline. The T13 core includes multiple units in the execution stage, namely a Load/Store unit (LSU), a scalar execution unit (EXEC) and a vector-oriented multipurpose functional unit (MFU), which implements the coprocessing features. At the instruction level, the T13 architecture supports the superscalar execution of instructions of different types, belonging to the same hart. The LSU works in superscalar mode when executing memory store instructions, that cannot cause a write-back conflict on the register file. The MFU is allowed to read operands from the register file but can only write its results to local scratchpad memories (SPMs). Data transfers to/from the data memory from/to the SPMs are managed by the LSU via dedicated instructions.

| Assembly syntax | Short description |
|-----------------|------------------|
| knemld (rd), (rs1), (rs2) | load vector into scratchpad region |
| knenstr (rd), (rs1), (rs2) | store vector into main memory |
| kadddv (rd), (rs1), (rs2) | adds vectors in scratchpad region |
| kauubv (rd), (rs1), (rs2) | subtract vectors in scratchpad region |
| kvmul (rd), (rs1), (rs2) | multiply vectors in scratchpad region |
| kved (rd), (rs1), (rs2) | reduce vector by addition |
| kdotp (rd), (rs1), (rs2) | vector dot product into register |
| ksavadss (rd), (rs1), (rs2) | add vector + scalar into scratchpad |
| ksavadstr (rd), (rs1), (rs2) | add vector + scalar into scratchpad |
| ksvmulc (rd), (rs1), (rs2) | multiply vector + scalar into scratchpad |
| ksvmulfr (rd), (rs1), (rs2) | multiply vector + scalar into register |
| kdotpps (rd), (rs1), (rs2) | vector dot product and post scaling |
| kslv (rd), (rs1), (rs2) | vector logic shift within scratchpad |
| ksav (rd), (rs1), (rs2) | vector arithmetic shift within scratchpad |
| krelu (rd), (rs1) | vector ReLu within scratchpad |
| kveil (rd), (rs1), (rs2) | compare vectors and create mask vector |
| kveilr (rd), (rs1), (rs2) | compare vector scalar and create mask |
| kvecp (rd), (rs1) | copy vector within scratchpad region |

The MFU executes vector arithmetic instructions, whose latency is proportional to the vector length. A hart requesting access to the busy MFU executes a self-referencing jump until the MFU becomes free, avoiding unnecessary stalls of other harts in the pipeline, which are independent from the MFU being busy.

The custom instruction extension supported by the MFU and LSU is summarized in Table 1. The instructions implement vector operations without relying on a vector register file, but rather on a memory space mapped on the local SPMs, for maximum flexibility. The programmer can move vector data in any point of the SPM address space with no constraint except the total capacity of the SPMs, which in turn is a parameter of the microarchitecture design. The vector length applied by MFU operations is encoded in a user accessible custom control/status register (CSR) named MVSIZE.

The instructions supported by the coprocessor subsystem are exposed to the programmer in the form of very simple intrinsic functions, fully integrated in the RISC-V gcc compiler toolchain.

**HARDWARE ACCELERATION SCHEMES**

The parametric coprocessor architecture in T1.3 cores is comprised of the MFU and the SPMs, that are accessed through a Scratchpad-Memory Interface (SPM), as detailed in Figure 1. The user can configure the number of parallel lanes \( D \) in the MFU, the number of MFUs \( F \), the SPM capacity, the number of SPMs \( N \), the number of SPMs \( M \), as well as the way the MFUs and SPMIs are shared between harts. A typical vector arithmetic operation in the coprocessor takes from 4 to 8 cycles to process one line of data coming from the SPM, an initial latency that is usually hidden by other instructions executing in parallel. The MFU is the engine that accelerates vector computations. It can operate on different integer data element widths (8, 16, 32-bit) in subword-SIMD fashion, and also in element-SIMD fashion when \( D \) is configured to multiply the execution lanes for DLP.

A mapping unit directs the data to the appropriate functional unit inside the MFU. There are five functional units in the MFU: adder, multiplier, shifter, accumulator, and Rectifier Linear Unit (ReLu). The MFU runs a hardware loop that continuously fetches data elements from the SPMs until the vector length is reached, with automatic increment of indices. Each SPM has one read and one write port. The parameter \( D \) that defines the MFU lanes also corresponds to the number of SPM banks; all the banks of an SPM are accessed together as a single SPM line. When the MFU executes a vector operation, in every clock cycle it fetches an entire SPM data line, composed of multiple vector elements, through the SPMI. A bank read rotator aligns the source operands coming from the SPM line, and a bank write rotator aligns the destination data to the correct banks in an SPM line. When the LSU fills the SPM banks with data from the 32-bit data memory port, a bank interleaver switches between the banks. The reader may refer to [5] for internal details of the units inside the MFU and SPMs.

Furthermore, the coprocessor can be configured to implement the following different schemes of interaction with harts:

**Shared coprocessor**: A single MFU/SPM subsystem is shared by all the harts. In case of busy MFU, any hart wanting to access it is stalled until the MFU becomes free. In this approach, superscalar execution is limited to occur only between coprocessor and non-coprocessor instructions. Yet, the MFU/SPM may exploit pure DLP acceleration, by multi-lane SIMD execution.
Thread-Dedicated coprocessors: A complete MFU/SPM subsystem is appointed to each hart, eliminating coprocessor contention. Stalls can only happen if the next instruction of the same hart that is using the MFU requests MFU operation. This approach can still exploit DLP by multi-lane SIMD execution, and also TLP by fully symmetric MIMD execution, allowing multiple vector instructions to execute in parallel.

Thread-Dedicated SPMI / Shared MFU: a dedicated SPM address space is kept for each hart, while the harts share one MFU at the functional unit level. This scheme still allows inter-hart superscalar execution of coprocessor instructions, provided they use different internal functional units of the MFU (e.g., adder, multiplier). Harts that request a busy internal unit in the MFU will be stalled until the contended unit becomes free. This scheme can exploit DLP by multi-lane SIMD execution, and also TLP in the form of a heterogeneous MIMD execution.

The explored design parameters and corresponding configurations, whose names will be used as references in reporting performance results, are the following:
- $M=1, F=1, D=1$: SISD
- $M=1, F=1, D=2,4,8$: Pure SIMD
- $M=3, F=3, D=1$: Symmetric MIMD
- $M=3, F=3, D=2,4,8$: Symmetric MIMD + SIMD
- $M=3, F=1, D=1$: Heterogenous MIMD
- $M=3, F=1, D=2,4,8$: Heterogenous MIMD + SIMD

In our application benchmarks, the parameter N is set to 2.

Finally, we refer to the T13 microarchitecture configured with no hardware acceleration as Klessydra T03.

PERFORMANCE RESULTS

A set of convolution tests were run on the T13 implemented with the coprocessor schemes introduced in the previous section. Here we refer to convolutions adopting the widely used 3x3 filter size, on matrix sizes of 4x4, 8x8, 16x16, and 32x32 elements. The element width was kept 32 bit in fixed-point representation. Table 2 summarizes the performance and synthesis results of the different configurations.

Total cycle count: With small matrix convolutions such as 4x4, the coprocessor support reached up to 3X speed-up over a RV32IM IMT core without acceleration (Klessydra T03), and 2X speed-up when compared to the single-threaded, DSP-extended RISCY core [7]. Regarding the accelerated implementations, increasing the DLP gives a boost of up to 29% when going from SISD to 8-way SIMD. Increasing the TLP gives a boost of up to 44% when switching from SIMD-only to symmetric MIMD coprocessor.

As expected, large matrix convolutions such as 32x32 exhibit larger advantage when comparing vector-accelerated cores to the non-accelerated cores, quantified in 13X speed-up relative to Klessydra T03, 9X relative to the RISCY core and 19X relative to ZeroRiscy.

Figure 2 shows the contribution of DLP and TLP for different matrix sizes. For small vectors, TLP exhibits better contributions to the speed than DLP, while as the matrix sizes grows, the DLP boost becomes higher than the TLP boost. Lastly, implementations exploiting both TLP and DLP performed greatly better in bigger matrix convolutions. A key outcome of this study is that a single core IMT processor can exploit both DLP and TLP and follow the grey curve, while a single-threaded core exploits only DLP and its speed-up trend follows the blue curve.

An important outcome of figure 2, the heterogenous MIMD coprocessor, that decreases by 3 times the number of functional units in the core, employed only 1% to 7% more cycles than the fully symmetric MIMD scheme. This shows that, in convolutional kernels, functional unit contention is much less impacting than SPM contention.

![Figure 2 DLP and TLP cycle-count performance boost](image)

Maximum clock frequency: All the cores under analysis were implemented as FPGA soft-cores. The clock speed exhibited the sharpest drops as the DLP grew larger. In the heterogeneous MIMD scheme, the crossbar mapping the SPMI output data on the shared MFU units becomes the critical path $D=4,8$. Pipelining the crossbar to reduce the critical path, introduces hardware overhead, compromising the area advantage of the heterogeneous MIMD configuration.

Absolute execution time: Figure 3 summarizes the comparison of total time to execute the convolutions when each core operates at its maximum frequency. In small matrix convolutions such as 4x4, increasing the DLP by going from SISD to SIMD actually increased the total time, because the drop in the clock frequency was more significant than the cycle count decrease.
This effect is not visible with larger matrices. Exploiting pure TLP, by going from a SISD to symmetric and heterogenous MIMD, decreased the total time in all cases, due to modest frequency drops. Thanks to exploiting both TLP and DLP, the symmetric MIMD + SIMD schemes exhibit the lowest execution times.

The non-accelerated Klessydra-T03, while employing a higher cycle count than RISCY due to the absence of DSP and hardware-loop extensions, exhibits an absolute performance advantage over RISCY thanks to a more than double frequency attained by the pure IMT microarchitecture. When compared to ZeroRiscy, T03 exhibits both lower cycle count and higher frequency.

**Hardware Resource Utilization:** In cost-constrained applications, the T13 area overhead due to DLP and TLP exploitation imposes to find an optimal balance between speed-up and area overhead. The heterogenous MIMD + SIMD scheme with $D = 2$ resulted to be a possible best balance between speed and area. The non-accelerated T03 exhibits only a slightly greater footprint than the tiny ZeroRiscy core, despite the replicated register file to support multi-threading, thanks to the LUTRAM implementation of the registers.

**Energy Efficiency:** The average energy per algorithmic operation (multiplications and additions) is a general measure of the energy efficiency attained by a processor core in implementing an algorithm.

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**Table 2 – Summary of performance results and synthesis results**

| Core              | Configuration     | DLP | 4x4 | 8x8 | 16x16 | 32x32 | Element Utilization | Max Freq. [MHz] |
|-------------------|-------------------|-----|-----|-----|-------|-------|---------------------|-----------------|
|                   |                   |     |     |     |       |       | FF | LUT | BRAM | DSP | LUT-RAM |     |
| Klessydra T03     | SISD              | 1   | 1105| 3060| 9727  | 34201 | 2488 | 6982 | 6    | 11  | 264     | 144.38 |
|                   | SIMD              | 2   | 895 | 2245| 6261  | 20374 | 2627 | 8400 | 6    | 15  | 264     | 145.96 |
|                   | Sym. MIMD         | 4   | 824 | 1768| 4607  | 13444 | 3301 | 11366| 6    | 23  | 264     | 137.23 |
|                   |                   | 8   | 824 | 1613| 3692  | 10069 | 4800 | 17331| 12   | 39  | 264     | 137.72 |
|                   | Sym. MIMD + SIMD  | 2   | 629 | 1190| 3123  | 8681  | 4712 | 15943| 18   | 31  | 264     | 131.67 |
|                   |                   | 4   | 560 | 1190| 2543  | 7148  | 6753 | 25089| 18   | 55  | 264     | 120.00 |
|                   |                   | 8   | 560 | 1152| 2543  | 6006  | 10854| 43419| 36   | 103 | 264     | 105.10 |
|                   | Het. MIMD         | 1   | 663 | 1521| 4153  | 13565 | 3012 | 10182| 18   | 11  | 264     | 117.16 |
|                   |                   | 2   | 638 | 1274| 3280  | 9167  | 3871 | 15577| 18   | 15  | 264     | 128.88 |
|                   |                   | 4   | 573 | 1213| 2688  | 7473  | 5015 | 23282| 18   | 23  | 264     | 122.01 |
|                   |                   | 8   | 573 | 1079| 2580  | 6285  | 7325 | 42944| 36   | 39  | 264     | 108.57 |
| Klessydra T03 (IMT, no accel) | 1819 | 5737| 20714| 79230| 1418 | 4281 | 0    | 7    | 176 | 221.14 |
| RISCY (single th. DSP ext) | 1377 | 4247| 15088| 57020| 2527| 7674 | 0    | 6    | 0   | 91.36 |
| ZeroRiscy (single th., no accel) | 2510 | 8111| 29583| 113793| 1933 | 5275 | 0    | 1    | 0   | 117.23 |

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Figure 3 Absolute execution time in different cores executing convolution algorithms (Log scale)
computation. Figure 4 reports the outcome of this analysis, referring to the soft-core implementations. While the most energy efficient designs resulted to be the T13 symmetric MIMD configurations, the heterogeneous MIMD approach exhibited an almost complete overlap in energy consumption. The pure SIMD schemes, despite having the smallest area footprint, resulted in a larger energy consumption, due to low exploitation of TLP.

Larger Filters: Table 3 shows how the speed-up and energy consumption trends continue as the filter dimensions grow larger. The matrix being convoluted is 32x32 elements in this analysis. The symmetric and heterogeneous MIMD+SIMD schemes, with $D=2$, maintain very similar performance and energy results throughout the analyzed cases. Comparing the MIMD+SIMD schemes with pure SIMD schemes, we see that an IMT core capable of MIMD acceleration increasingly performs better than a single-thread SIMD acceleration. Lastly, comparing to the non-accelerated cores, higher order filters show the evident benefits of vector coprocessors, such that the maximum 17X performance and 6X energy boost obtained with 3x3 filters grows to 35X and 13X, respectively, when using 11x11 filters.

**CONCLUSIONS**

Being convolutions highly parallel in nature, as well as extremely important in a variety of edge computing applications, they serve as a prime example to demonstrate the exploitation of IMT processors. MIMD + SIMD vector coprocessor schemes enabled tuning the TLP and DLP contribution, reaching the highest performance and energy efficient metrics when $D = 2$ for 3x3 filters, while still utilizing a limited area footprint. Higher DLP implementations showed to be faster and more energy efficient in higher order filters, thus making the optimal DLP choice to be application oriented. Furthermore, the heterogeneous MIMD approach was capable to maintain very similar results as the symmetric MIMD approach, but at a lower hardware cost. Both the approaches exhibited better

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**Figure 4 Average energy [nJ] per algorithmic operation in different cores executing convolution algorithms**

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**Table 3 Higher Order Filter Evaluation Results for Cycle Count, Total time at max frequency and Energy**

| Core     | DLP | Filter (5x5) | Filter (7x7) | Filter (9x9) | Filter (11x11) |
|----------|-----|--------------|--------------|--------------|---------------|
|          | Cycle Cnt X1000 | T (us) | E [uJ] | Cycle Cnt X1000 | T (us) | E [uJ] | Cycle Cnt X1000 | T (us) | E [uJ] | Cycle Cnt X1000 | T (us) | E [uJ] |
| T13 SIMD  | 2   | 52.7 | 362 | 50.6 | 101.2 | 694 | 97.1 | 165.8 | 1136 | 159.1 | 246.5 | 1689 | 236.6 |
| T13 SIMD  | 8   | 24.6 | 179 | 34.4 | 46.1 | 335 | 64.5 | 74.7 | 543  | 104.7 | 110.6 | 803  | 154.8 |
| T13 Sym MIMD | 2  | 19.5 | 148 | 26.9 | 35.8 | 272 | 49.4 | 57.4 | 436  | 79.2  | 84.4  | 641  | 116.5 |
| T13 Sym MIMD | 8  | 11.8 | 113 | 28.9 | 19.2 | 183 | 46.9 | 29.8 | 284  | 72.7  | 42.9  | 408  | 104.7 |
| T13 Het MIMD | 2  | 20.5 | 159 | 28.3 | 37.5 | 291 | 51.8 | 60.2 | 467  | 83.1  | 88.5  | 687  | 122.1 |
| T03 (no accel.) | -   | 247 | 1120 | 215.5 | 514.8 | 2328 | 447.9 | 881.2 | 3985 | 766.6 | 1369 | 6191 | 1191.1 |
| RISCY    | -   | 180 | 1971 | 252.0 | 385.3 | 4218 | 539.4 | 662.5 | 7252 | 927.5 | 1000.2 | 10949 | 1400.3 |
| ZeroRiscy | -   | 318.9 | 2721 | 226.4 | 674.5 | 5754 | 478.9 | 1129.7 | 9637 | 802.1 | 1697.8 | 14482 | 1205.4 |
results than pure SIMD acceleration, showing how an IMT microarchitecture can benefit from TLP and DLP acceleration in a single core, while a single-thread core can only benefit from DLP acceleration with less effective results.

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The Klessydra-T parametric cores are available as open source designs on the GitHub platform at https://github.com/klessydra/T13x.