T-count and Qubit Optimized Quantum Circuit Design of the Non-Restoring Square Root Algorithm

EDGARD MUÑOZ-COREAS AND HIMANSHU THAPLIYAL, University of Kentucky, USA

Quantum circuits for basic mathematical functions such as the square root are required to implement scientific computing algorithms on quantum computers. Quantum circuits that are based on Clifford+T gates can easily be made fault tolerant but the T gate is very costly to implement. As a result, reducing T-count has become an important optimization goal. Further, quantum circuits with many qubits are difficult to realize, making designs that save qubits and produce no garbage outputs desirable. In this work, we present a T-count optimized quantum square root circuit with only $2 \cdot n + 1$ qubits and no garbage output. To make a fair comparison against existing work, the Bennett’s garbage removal scheme is used to remove garbage output from existing works. We determined that our proposed design achieves an average T-count savings of 43.44%, 98.95%, 41.06% and 20.28% as well as qubit savings of 85.46%, 95.16%, 90.59% and 86.77% compared to existing works.

CCS Concepts: • Hardware → Quantum computation; Emerging architectures; Arithmetic and datapath circuits;

Additional Key Words and Phrases: Quantum arithmetic circuit, Quantum gate, Non-restoring division, Resource optimization

ACM Reference Format:
Edgard Muñoz-Coreas and Himanshu Thapliyal. 2010. T-count and Qubit Optimized Quantum Circuit Design of the Non-Restoring Square Root Algorithm. ACM J. Emerg. Technol. Comput. Syst. 9, 4, Article 39 (March 2010), 16 pages. https://doi.org/0000001.0000001

1 INTRODUCTION

Among the emerging computing paradigms, quantum computing appears promising due to its applications in number theory, encryption, search and scientific computation [7] [4] [19] [31] [24] [30] [12] [29] [13]. Quantum circuits for arithmetic operations such as addition, multiplication, square root and fractional powers are required in the quantum circuit implementations of many quantum algorithms [10] [9] [4] [6] [7]. For example, arithmetic circuits for the square root can be used in the circuit implementation of quantum algorithms such as those for computing roots of polynomials, evaluating quadratic congruence and the principal ideal problem [12] [29] [13]. Quantum square root circuits also reduce the resources needed in the circuit implementations of higher level functions computing the natural logarithm [6]. An efficient quantum circuit of the natural logarithm has use in quantum algorithms such as those for Pell’s equation and the principal ideal problem [13]. The design of quantum circuits for arithmetic operations such as addition and multiplication have received notable attention in the literature. However, the design of quantum circuits for crucial arithmetic functions such as the square root is still at an initial stage.
Reliable quantum circuits must be able to tolerate noise errors [32] [33] [21] [23]. Fault tolerant quantum gates (such as Clifford+T gates) and quantum error correcting codes can be used to make quantum circuits resistant to noise errors [1] [17] [2] [15] [22] [8]. However, the increased tolerance to noise errors comes with the increased implementation overhead associated with the quantum T gate [1] [22] [33] [8]. Because of the increased cost to realize the T gate, T-count has become an important performance measure for fault tolerant quantum circuit design [1] [11]. Further, existing quantum computers have few qubits and large-scale quantum computers are difficult to realize [14] [18]. As a result, the total number of qubits required by a quantum circuit is an important performance measure. Quantum circuits have overhead called ancillae and garbage output that add to the total number of qubits of a quantum circuit. Any constant inputs in the quantum circuit are called ancillae. Garbage output exist in the quantum circuit to preserve one-to-one mapping. Garbage output are not primary inputs or useful outputs. Minimizing the overhead from ancillae and garbage output is a means to reduce overall qubit cost of a quantum circuit.

The design of quantum circuits for the calculation of the square root has only recently begun to be addressed in the literature. A design for the calculation of the square root based on the Newton approximation algorithm is presented in [6]. While an interesting design, the implementation requires $5 \cdot \lceil \log_2(b) \rceil$ multiplications and $3 \cdot \lceil \log_2(b) \rceil$ additions (where $b$ is the number of bits of accuracy in the solution and $b \geq 4$) [6]. This arithmetic operation cost translates into significant T gate and qubit cost. The design in [26] presents a quantum circuit for calculating the square root based on the non-restoring square root algorithm. This design requires only $\frac{n}{2}$ additions or subtractions making the design far more efficient than the design in [6] in terms of qubits and T gates. However, the design in [26] does not include the additional ancillae and T gate costs required for removing garbage outputs. Additional recent quantum circuit designs for calculating the square root root presented in [3] also require only $\frac{n}{2}$ controlled subtraction operations. The designs in [3] are based on the non-restoring square root algorithm. Thus, the designs presented in [3] also offer more efficient alternatives to the design in [6] in terms of qubits and T gates. One of the designs presented in [3] has been optimized for gate count further reducing its T-gate cost. Both designs presented in [3] produce significant garbage output. In [3] for both designs the qubit and T gate cost associated with removing this garbage output was not considered in the circuit cost calculations. Thus, the quantum square root circuits in [26] and [3] have significant overhead in terms of T-count and qubits. To overcome the limitations of existing designs, we present the design of a quantum square root circuit that is garbageless, requires $2 \cdot n + 1$ qubits and is optimized for T-count. The quantum square root circuit based on our proposed design is compared and is shown to be better than the existing designs of quantum square root circuit in terms of both T-count and qubits.

This paper is organized as follows: Section 2 presents background information on the Clifford+T gates. In Section 3 we present the design of our proposed quantum square root circuit. In Section 4 our proposed design is compared to the existing work.

## 2 BACKGROUND

### 2.1 Fault Tolerant Quantum Circuits

The fault tolerant Clifford+T gate set is used in fault tolerant quantum circuit design. Table 1 shows the gates that make up the Clifford+T gate set. The quantum square root circuit proposed in this work is composed of the quantum NOT gate, Feynman (CNOT) gate, inverted control CNOT gate, SWAP gate and Toffoli gate. Table 1 illustrates that the CNOT gate and NOT gate are Clifford+T gates. The Clifford+T implementation of the inverted control CNOT gate, SWAP gate and Toffoli gate are shown in Figure 1. In this work, we use the Clifford+T implementation of the Toffoli gate presented in [2]. The inverted control CNOT gate and the SWAP gate are 2 input, 2 output logic gates that...
Table 1. The Clifford + T gates

| Type of Gate                  | Symbol | Matrix                              |
|------------------------------|--------|-------------------------------------|
| NOT gate                     | $X$    | $\begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$ |
| Hadamard gate                | $H$    | $\begin{bmatrix} \frac{1}{\sqrt{2}} & 1 \\ 1 & -\frac{1}{\sqrt{2}} \end{bmatrix}$ |
| $T$ gate                     | $T$    | $\begin{bmatrix} 1 & 0 \\ 0 & e^{i\frac{\pi}{4}} \end{bmatrix}$ |
| $T$ gate Hermitian transpose | $T^\dagger$ | $\begin{bmatrix} 1 & 0 \\ 0 & e^{-i\frac{\pi}{4}} \end{bmatrix}$ |
| Phase gate                   | $S$    | $\begin{bmatrix} 1 & 0 \\ 0 & i \end{bmatrix}$ |
| Phase gate Hermitian transpose | $S^\dagger$ | $\begin{bmatrix} 1 & 0 \\ 0 & -i \end{bmatrix}$ |
| CNOT gate                    | $C$    | $\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix}$ |

**Fig. 1.** The fault tolerant Clifford + T implementations of quantum logic gates used in this work. The Toffoli gate shown has a T-count of 7 and a T-depth of 3.

have the mapping $A, B$ to $A, \overline{A} \oplus B$ and $A, B$ to $B, A$ respectively. The Toffoli gate is a 3 input, 3 output logic gate and has the mapping $A, B, C$ to $A, B, A \cdot B \oplus C$.

Fault tolerant quantum circuit performance is evaluated in terms of T-count and T-depth because the implementation costs of the T gate is significantly greater than the implementation costs of the other Clifford+T gates [1] [22] [33] [8] [11]. **T-count is the total number of T gates or Hermitian transposes of the T gate in a quantum circuit.** As illustrated in Figure 1, the inverted control CNOT gate and the SWAP gate both have a T-count of 0 while the Toffoli gate has a T-count of 7. **T-depth is the number of T gate layers in the circuit, where a layer consists of quantum operations that can be performed simultaneously.** As illustrated in Figure 1, the inverted control CNOT gate and the SWAP gate both have a T-depth of 0. The Toffoli gate has a T-depth of 3 because the most T gate layers encountered by any qubit in the Toffoli gate is 3.
3 DESIGN OF THE PROPOSED QUANTUM SQUARE ROOT CIRCUIT

The proposed quantum square root circuit calculates the square root by implementing the non-restoring square root algorithm. The non-restoring square root algorithm is illustrated in Figure 2 (Algorithm 1). Researchers have demonstrated the correctness of the non-restoring square root algorithm through functionally correct circuit implementations such as those in [26] [3] and [25]. A specific example illustrating how Algorithm 1 calculates the square root of a number $a$ is available in Appendix A.

We now present the design of our proposed quantum square root circuit. The proposed method is garbageless and requires fewer qubits than existing designs. The proposed circuit also has a lower T-count compared to existing designs. Consider the square root of the number $a$. We represent $a$ as a positive binary value in 2’s complement that has an even bit length $n$. $a$ is stored in quantum register $|R\rangle$. Further, let $|F\rangle$ be a quantum register of size $n$ initialized to 1 and let $|z\rangle$ be a 1 qubit ancillae set to 0. At the end of computation, quantum register locations $|F_{2} + 1\rangle$ through $|F_{2}\rangle$ of $|F\rangle$ will have the value $Y (\sqrt{a})$. In addition, quantum register $|R\rangle$ that initially stored $a$ will have the remainder from the calculation of $\sqrt{a}$. Lastly, quantum register $|z\rangle$ and the remaining register locations $|F_{n-1}\rangle$ through $|F_{2} + 2\rangle$ and $|F_{1}\rangle$ through $|F_{0}\rangle$ of $|F\rangle$ are restored to their initial values at the end of computation.

The proposed methodology is generic and can design a quantum square root circuit of any size. The steps involved in the proposed methodology are presented for finding the square root of the value $a$. The proposed quantum square root circuit is divided into three parts: (i) Part 1: Initial Subtraction, (ii) Part 2: Conditional Addition or Subtraction, and (iii) Part 3: Remainder Restoration. A quantum circuit is generated for each part of the design. Each part implements the following portions of the non-restoring square root algorithm shown in Algorithm 1.

- **Part 1: Initial Subtraction** This part executes the statements before the FOR loop in Algorithm 1. Also, this part executes the first iteration of the FOR loop in Algorithm 1.
- **Part 2: Conditional Addition or Subtraction** This part executes the remaining $\frac{n}{2} - 2$ iterations of the FOR loop in Algorithm 1. Thus, Part 2 will be iterated a total of $\frac{n}{2} - 2$ times.
- **Part 3: Remainder Restoration** This part implements the IF statement that follows the FOR loop in Algorithm 1.

Figure 3 shows a generic example of how the parts of our quantum square root circuit are combined to implement Algorithm 1. The detailed quantum circuit designs of Part 1, Part 2, and Part 3 required to implement Algorithm 1 are explained as follows:

3.1 Part 1: Initial Subtraction

This part only occurs once. The quantum circuit for Part 1 takes quantum registers $|R\rangle$, $|F\rangle$ and $|z\rangle$ as inputs. Part 1 has six steps. Figure 4 illustrates the generation of Part 1 with an example of a 6 bit square root circuit.

- Step 1: At location $|R_{n-2}\rangle$ apply a quantum NOT gate.
- Step 2: At locations $|R_{n-1}\rangle$ and $|R_{n-2}\rangle$ apply a CNOT gate such that the location $|R_{n-2}\rangle$ is unchanged while location $|R_{n-1}\rangle$ now has the value $|R_{n-2} \oplus R_{n-1}\rangle$ (where $R_{n-2} \oplus R_{n-1} \equiv Y_{2} - 1$). Step 1 and Step 2 implement lines 2 through 4 of Algorithm 1.
- Step 3: At locations $|R_{n-1}\rangle$ and $|F_{1}\rangle$ apply a CNOT gate such that the location $|R_{n-1}\rangle$ is unchanged while location $|F_{1}\rangle$ now has the value $|R_{n-2} \oplus R_{n-1} \oplus F_{1}\rangle$. If $|R_{n-1}\rangle = 1$, this step partially implements line 11 of Algorithm 1 because the value at location $|F_{1}\rangle$...
Algorithm 1: Non-restoring square root algorithm

Requirements: $a$ must be a positive binary value in 2's complement that has an even bit length $n$
Input: $a$. $a$ is incrementally loaded into $R$ starting from the most significant bit.
Outputs: $\sqrt{a}$ and the remainder from calculating $\sqrt{a}$. The $\sqrt{a}$ is an $\frac{n}{2}$ bit value in $F$.
We will use the variable $Y$ to represent the $\sqrt{a}$. $R$ will have the $n$ bit remainder.

Function Non-Restoring($a$)

1. $R = 0^{n-2}a_{n-1}a_{n-2}$ //where $0^{n-2}$ are $n-2$ zeros. $a_{n-1}$ is the most significant bit of $a$.
2. $F = 0^{n-2}01$ //where $0^{n-2}$ are $n-2$ zeros.
3. $R = R - F$
4. 

For $i = \frac{n}{2}$ to 1

If($R < 0$)

5. $Y_i = 0$
6. $R = 0^{2-i-2}R_{n-1-2,i} \cdots R_0a_{2,i-1}a_{2,i-2}$ //where $0^{2-i-2}$ are $2 \cdot i - 2$ zeros.
7. //Values $R_{n-1-2,i}$ through $R_0$ of $R$ are shifted and reused.
8. $F = 0^{i+\frac{n}{2}-2}Y_{\frac{n}{2}-1}Y_{\frac{n}{2}-2} \cdots Y_{i+1}Y_i11$ //where $0^{i+\frac{n}{2}-2}$ are $i + \frac{n}{2} - 2$ zeros.
9. //$Y_{\frac{n}{2}-1}$ is the most significant bit of $Y$.
10. $R = R + F$
11. 

Else

12. $Y_i = 1$
13. $R = 0^{2-i-2}R_{n-1-2,i} \cdots R_0a_{2,i-1}a_{2,i-2}$ //where $0^{2-i-2}$ are $2 \cdot i - 2$ zeros.
14. //Values $R_{n-1-2,i}$ through $R_0$ of $R$ are shifted and reused.
15. $F = 0^{i+\frac{n}{2}-2}Y_{\frac{n}{2}-1}Y_{\frac{n}{2}-2} \cdots Y_{i+1}Y_i01$ //where $0^{i+\frac{n}{2}-2}$ are $i + \frac{n}{2} - 2$ zeros.
16. //$Y_{\frac{n}{2}-1}$ is the most significant bit of $Y$.
17. $R = R - F$
18. 

End

If($R < 0$)

19. $Y_0 = 0$
20. $F = 0^{\frac{n}{2}-2}Y_{\frac{n}{2}-1}Y_{\frac{n}{2}-2} \cdots Y_1Y_01$ //where $0^{\frac{n}{2}-2}$ are $\frac{n}{2} - 2$ zeros.
21. //$Y_{\frac{n}{2}-1}$ is the most significant bit of $Y$.
22. $R = R + F$
23. 

Else

24. $Y_0 = 1$
25. $F = 0^{\frac{n}{2}-2}Y_{\frac{n}{2}-1}Y_{\frac{n}{2}-2} \cdots Y_1Y_01$ //where $0^{\frac{n}{2}-2}$ are $\frac{n}{2} - 2$ zeros.
26. //$Y_{\frac{n}{2}-1}$ is the most significant bit of $Y$.
27. 

End

Return: $R, F$.

Fig. 2. The non-restoring square root algorithm. The algorithm has been adapted from the presentation shown in [25].

\[
\left(\overline{R_{n-2}} \oplus R_{n-1} \oplus F_1\right) \text{ simplifies to } |1\rangle. \text{ Otherwise this step helps to implement line } 18 \text{ of Algorithm 1 because the value at location } |F_1\rangle \left(\overline{R_{n-2}} \oplus R_{n-1} \oplus F_1\right) \text{ simplifies to } |0\rangle \text{ when } |R_{n-1}\rangle = 0.\]
Fig. 3. Example of the complete proposed square root circuit.

Fig. 4. Circuit generation of Part 1 of the proposed quantum square root circuit: Steps 1-6. To keep Figures compact quantum register locations (such as $|F_5\rangle$ through $|F_4\rangle$) are represented as a single line and labeled accordingly (such as with $|F_{5,4}\rangle$) where possible.

- Step 4: At locations $|R_{n-1}\rangle$ and $|z\rangle$ apply an inverted control CNOT gate such that the location $|R_{n-1}\rangle$ is unchanged while location $|z\rangle$ now has the value $\overline{R_{n-2} \oplus R_{n-1} \oplus z}$ which simplifies to $R_{n-2} \oplus R_{n-1} \oplus z \equiv Y_{\frac{n}{2}-1}$. This step prepares register $|z\rangle$ for use in subsequent steps.
- Step 5: At locations $|R_{n-1}\rangle$ and $|F_2\rangle$ apply an inverted control CNOT gate such that the location $|R_{n-1}\rangle$ is unchanged while location $|F_2\rangle$ now has the value $\overline{R_{n-2} \oplus R_{n-1} \oplus F_2}$ which simplifies to $R_{n-2} \oplus R_{n-1} \oplus F_2$ (where $R_{n-2} \oplus R_{n-1} \oplus F_2 \equiv Y_{\frac{n}{2}-1}$). If $|R_{n-1}\rangle = 1$ this step completes execution of line 11 of Algorithm 1 and quantum register $|F\rangle$ will have the value: $|0\rangle \cdots |0\rangle |Y_{\frac{n}{2}-1}\rangle |1\rangle |1\rangle$. Conversely, if $|R_{n-1}\rangle = 0$ this step completes execution of line 18 of Algorithm 1 and quantum register $|F\rangle$ will have the value: $|0\rangle \cdots |0\rangle |Y_{\frac{n}{2}-1}\rangle |0\rangle |1\rangle$. 

ACM Journal on Emerging Technologies in Computing Systems, Vol. 9, No. 4, Article 39. Publication date: March 2010.
• Step 6: this step has two sub-steps.
  - Step 1: At locations $|R_{n-1}\rangle$ through $|R_{n-4}\rangle$ of register $|R\rangle$ and locations $|F_3\rangle$ through $|F_0\rangle$ of register $|F\rangle$ apply the quantum conditional addition or subtraction (ADD/SUB) circuit such that locations $|F_3\rangle$ through $|F_0\rangle$ are unchanged while locations $|R_{n-1}\rangle$ through $|R_{n-4}\rangle$ will hold the results of computation.
  - Step 2: At location $|z\rangle$ apply the quantum ADD/SUB circuit such that the operation of the circuit is conditioned on the value at location $|z\rangle$. Location $|z\rangle$ is unchanged.

After this step, if $|R_{n-1}\rangle = 1$, the quantum register $|R\rangle$ will equal $|R\rangle + |F\rangle$ (line 13 of Algorithm 1). If $|R_{n-1}\rangle = 0$, the quantum register $|R\rangle$ will equal $|R\rangle - |F\rangle$ (line 20 of Algorithm 1).

### 3.2 Part 2: Conditional Addition or Subtraction

This part is repeated a total of $\frac{n}{2} - 2$ times. The quantum circuit for each iteration of Part 2 takes quantum registers $|R\rangle$, $|F\rangle$ and $|z\rangle$ as inputs. Part 2 has seven steps. Figure 5 illustrates the generation of Part 2 with an example of a 6 bit square root circuit. We show the steps for iteration $i$ where $2 \leq i \leq \frac{n}{2} - 1$.

- Step 1: At locations $|z\rangle$ and $|F_1\rangle$ apply an inverted control CNOT gate such that the location $|z\rangle$ is unchanged while location $|F_1\rangle$ now has the value $|z\rangle \oplus |F_1\rangle$. This step restores $|F_1\rangle$ to its initial value such that $|F\rangle$ has the value: $|0\rangle \cdots |0\rangle |Y_{\frac{q}{2}}^{-1} \cdots |Y_{\frac{q}{2}-i+1}^{-1}|0\rangle|1\rangle$.
- Step 2: At locations $|F_2\rangle$ and $|z\rangle$ apply a CNOT gate such that the location $|F_2\rangle$ is unchanged while location $|z\rangle$ now has the value $|F_2\rangle \oplus |z\rangle$ which reduces to 0. Steps 1 and 2 prepare $|z\rangle$ and $|F\rangle$ for iteration $i$ of the FOR loop in Algorithm 1.

![Quantum Circuit Diagram](image-url)
3.3 Part 3: Remainder Restoration

This part only occurs once. The quantum circuit for Part 3 takes quantum registers \(|R\rangle, |F\rangle\) and |z\rangle as inputs. Part 3 has nine steps. Figure 6 illustrates the generation of Part 3 with an example of a 6 bit square root circuit.

- Step 1: At locations |z\rangle and |F_i\rangle apply an inverted control CNOT gate such that location |z\rangle is unchanged while location |F_i\rangle now has the value |z \oplus F_i\rangle. This step restores |F_i\rangle to its initial value such that |F\rangle has the value: |0\rangle \cdots |0\rangle |Y_{2^{-i-1}}\rangle \cdots |Y_{2^{-i}}\rangle|0\rangle|Y_i\rangle\rangle. Thus, this step completes line 20 of Algorithm 1.

- Step 2: At locations |F_i\rangle and |z\rangle apply a CNOT gate such that location |z\rangle now has the value |z \oplus F_2 + z\rangle (where R_{n-1} \oplus F_2 \circ z \equiv Y_{2^{-i}}). This step prepares register |z\rangle for use in subsequent steps.

- Step 3: At locations |F_i\rangle and |F_{i+1}\rangle apply an inverted control CNOT gate such that location |F_{i+1}\rangle is unchanged while location |F_i\rangle now has the value |F_{i+1}\rangle \oplus F_i\rangle (where R_{n-1} \oplus F_{i+1} = Y_{2^{-i}}). If |R_{n-1}\rangle = 1 this step continues execution of line 11 of Algorithm 1 and quantum register |F\rangle will have the value: |0\rangle \cdots |0\rangle |Y_{2^{-i}}\rangle \cdots |Y_{2^{-i+1}}\rangle|0\rangle|1\rangle. Conversely, if |R_{n-1}\rangle = 0 this step continues execution of line 18 of Algorithm 1 and quantum register |F\rangle will have the value: |0\rangle \cdots |0\rangle |Y_{2^{-i-1}}\rangle \cdots |Y_{2^{-i}}\rangle|0\rangle|1\rangle. This step completes the execution of line 11 of Algorithm 1 or line 18 of Algorithm 1 depending on the value of |R_{n-1}\rangle.

- Step 7: This step has two sub-steps.
  - Step 1: At locations |R_{n-1}\rangle through |R_{n-2-i-2}\rangle of register |R\rangle and |F_{2+i-1}\rangle through |F_0\rangle of register |F\rangle apply the quantum conditional addition or subtraction (ADD/SUB) circuit such that locations |F_{2+i-1}\rangle through |F_0\rangle are unchanged while locations |R_{n-1}\rangle through |R_{n-2-i-2}\rangle will hold the results of computation.
  - Step 2: At location |z\rangle apply the quantum ADD/SUB circuit such that the operation of the circuit is conditioned on the value at location |z\rangle. Location |z\rangle is unchanged. After this step, if |R_{n-1}\rangle = 1, the quantum register |R\rangle will equal |R\rangle + |F\rangle (line 13 of Algorithm 1). If |R_{n-1}\rangle = 0, the quantum register |R\rangle will equal |R\rangle - |F\rangle (line 20 of Algorithm 1).
T-count and Qubit Optimized Quantum Circuit Design of the Non-Restoring Square Root Algorithm

Fig. 6. Circuit generation of Part 3 of the proposed quantum square root circuit: Steps 1-9. Quantum circuit and graphical representation are shown. To keep Figures compact quantum register locations (such as $|R_{4:0}\rangle$ through $|R_{0}\rangle$) are represented as a single line and labeled accordingly (such as with $|R_{4:0}\rangle$) where possible.

- Step 3: At locations $|R_{n-1}\rangle$ and $|z\rangle$ apply an inverted control CNOT gate such that location $|F_2\rangle$ is unchanged while location $|z\rangle$ now has the value $R_{n-1} \oplus F_2 \oplus z \equiv Y_0$. This step prepares register $|z\rangle$ for use in subsequent steps.
- Step 4: At locations $|R_{n-1}\rangle$ and $|F_{\frac{n+1}{2}}\rangle$ apply an inverted control CNOT gate such that location $|R_{n-1}\rangle$ is unchanged while location $|F_{\frac{n+1}{2}}\rangle$ now has the value $R_{n-1} \oplus F_{\frac{n+1}{2}} \equiv Y_0$. If $|R_{n-1}\rangle = 1$, this step continues execution of line 26 of Algorithm 1 and if $|R_{n-1}\rangle = 0$, this step continues execution of line 31 of Algorithm 1. Quantum register $|F\rangle$ will have the value: $|0\rangle \cdots |0\rangle |Y_0\rangle |Y_{\frac{n-1}{2}}\rangle \cdots |Y_1\rangle |0\rangle |1\rangle$.
- Step 5: At location apply $|z\rangle$ apply a quantum NOT gate. The value of $|z\rangle$ is now $|R_{n-1} \oplus F_2 \oplus z\rangle$ (where $R_{n-1} \oplus F_2 \oplus z \equiv Y_0$). This step prepares $|z\rangle$ for subsequent computations.
- Step 6: This step has the following two sub-steps.
  - Step 1: Apply quantum registers $|F\rangle$ and $|R\rangle$ to a quantum CTRL-ADD circuit such that $|F\rangle$ is unchanged while $|R\rangle$ will hold the result of computation.
  - Step 2: At location $|z\rangle$ apply a quantum conditional addition (CTRL-ADD) circuit such that the operation of the quantum CTRL-ADD circuit is conditioned on the value at location $|z\rangle$. After this step, if $|R_{n-1}\rangle = 1$, the quantum register $|R\rangle$ will equal $|R\rangle + |F\rangle$ (line 28 of Algorithm 1). If $|R_{n-1}\rangle = 0$, the value in quantum register $|R\rangle$ is unchanged. After this step, $|R\rangle$ will contain the remainder from calculating $Y$ (or $\sqrt{a}$).
The proposed design methodology reduces the T-count by incorporating T gate efficient implementations of quantum CTRL-ADD circuits and quantum ADD/SUB circuits. Garbageless and T gate optimized quantum ADD/SUB and CTRL-ADD circuits in the literature such as the designs in [27] [16] and [20] can be used in our proposed quantum square root circuit. The T-count of the proposed quantum square root circuit that correctly implements the non-restoring square root algorithm.

4 Cost Analysis

4.1 T-count Cost

The proposed design methodology reduces the T-count by incorporating T gate efficient implementations of quantum CTRL-ADD circuits and quantum ADD/SUB circuits. Garbageless and T gate optimized quantum ADD/SUB and CTRL-ADD circuits in the literature such as the designs in [27] [16] and [20] can be used in our proposed quantum square root circuit. The T-count of the proposed quantum square root circuit is illustrated shortly for each part of the proposed design.

4.1.1 Part 1: Initial Subtraction.
- Steps 1 through 5 do not require T-gates.
- Step 6 requires 42 T gates. We use a quantum ADD/SUB circuit of T-count $14 \cdot n - 14$ in this step (where $n = 4$).

4.1.2 Part 2: Conditional Addition or Subtraction. The steps in this part are repeated $\frac{n}{2} - 2$ times. We show the T-count for the $i$th iteration of Part 2 where $2 \leq i \leq \frac{n}{2} - 1$
- The $i$th iteration of 1 through 6 do not require T-gates.
- The T-count for the $i$th iteration of Step 7 is $14 \cdot (2 \cdot (i + 1)) - 14$ which simplifies to $28 \cdot i + 14$.
  - We use a quantum ADD/SUB circuit of T-count $14 \cdot n - 14$ in this step (where $n = 2 \cdot (i + 1)$).

4.1.3 Part 3: Reminder Restoration.
- Steps 1 through 5 do not require T-gates.
- The T-count for Step 6 is $21 \cdot n - 14$. We use a quantum CTRL-ADD circuit of T-count $21 \cdot n - 14$ in this step.
- Steps 7 through 9 do not require T-gates.

4.1.4 Calculation of T-count. To calculate the total T-count we add the total T-count for each part of the design. The total T-count for Part 1 is 42 (or $14 \cdot n - 14$ where $n = 4$). The total T-count for Part 2 is given as $\sum_{i=2}^{\frac{n}{2}-1} 28 \cdot i + 14$ and the total T-count for Part 3 is given as $21 \cdot n - 14$. Combining
the total T-count for each part of the proposed quantum square root circuit results in the following expression:

\[
\left( \sum_{i=1}^{\frac{n}{2} - 1} 28 \cdot i + 14 \right) + 21 \cdot n - 14
\]  

(1)

The expression for the T-count (expression 1) can be simplified into the following expression:

\[
\frac{7}{2} \cdot n^2 + 21 \cdot n - 28
\]  

(2)

4.2 T-depth Cost

We now calculate the T-depth for our proposed design. Our proposed design is based on T-depth efficient designs of quantum ADD/SUB circuits and quantum CTRL-ADD circuits. We determined that garbageless and T gate optimized quantum ADD/SUB circuits in the literature such as the design in [27] have a T-depth that is constant and independent of the circuit size \(n\). Thus, these ADD/SUB circuits have T-depth of order \(O(1)\). We determined as well that CTRL-ADD circuits in the literature such as the design in [20] scale as a function of circuit size \(n\). Thus, these CTRL-ADD circuits have a T-depth of order \(O(n)\). The T-depth of the proposed quantum square root circuit is illustrated shortly for each part of the proposed design.

4.2.1 Part 1: Initial Subtraction.

- Steps 1 through 5 do not require T-gates.
- Step 6 has a constant T-depth of 10. This T-depth is seen by locations \(|R_{n-2}\rangle\) and \(|R_{n-3}\rangle\) of quantum register \(|R\rangle\). We use a quantum ADD/SUB circuit in this step. The ADD/SUB circuit has a constant T-depth 10 that is independent of the circuit’s size.

4.2.2 Part 2: Conditional Addition or Subtraction. The steps in this part are repeated \(\frac{n}{2} - 2\) times.

We show the T-count for the \(i\)th iteration of Part 2 where \(2 \leq i \leq \frac{n}{2} - 1\)

- The \(i\)th iteration of 1 through 6 do not require T-gates.
- Step 7 has a constant T-depth of 10. This T-depth is seen by locations \(|R_{n-2}\rangle\) through \(|R_{n-2,i-1}\rangle\) of quantum register \(|R\rangle\). We use a quantum ADD/SUB circuit in this step. The ADD/SUB circuit has a constant T-depth 10 that is independent of the circuit’s size.

4.2.3 Part 3: Reminder Restoration.

- Steps 1 through 5 do not require T-gates.
- Step 6 has a T-depth of \(2 \cdot n\). This T-depth is seen by quantum register \(|z\rangle\). We use a quantum CTRL-ADD circuit of T-depth \(2 \cdot n\) in this step.
- Steps 7 through 9 do not require T-gates.

4.2.4 Calculation of T-depth. We now illustrates the steps we use to determine the total T-depth for the proposed quantum square root circuit:

- Step 1: Calculate the T-depth for Part 1. Part 1 has a T-depth of 10. This T-depth is seen by locations \(|R_{n-2}\rangle\) and \(|R_{n-3}\rangle\) of quantum register \(|R\rangle\).
- Step 2: Calculate the T-depth for Part 2. Part 2 has a T-depth of \(10 \cdot \left( \frac{n}{2} - 2 \right)\) because Part 2 requires \(\frac{n}{2} - 2\) quantum ADD/SUB circuits. The total T-depth \(10 \cdot \left( \frac{n}{2} - 2 \right)\) simplifies to \(5 \cdot n - 20\). This T-depth is seen by locations \(|R_{n-2}\rangle\) and \(|R_{n-3}\rangle\) of quantum register \(|R\rangle\).
- Step 3: Calculate the T-depth for Part 3. Part 3 has a T-depth of \(2 \cdot n\). This T-depth is seen by quantum register \(|z\rangle\).
Step 4: Determine which qubits see the most T gate layers. We find after comparing all the qubits in our proposed design quantum register \(|z\rangle\) and quantum register locations \(|R_{n-2}\rangle\) and \(|R_{n-3}\rangle\) of \(|R\rangle\) see the most T gate layers.

Step 5: Determine the total number of T gate layers seen by quantum register \(|z\rangle\) in the proposed design. Quantum register \(|z\rangle\) will see a total of \(2 \cdot n\) T gate layers because in Part 1 and Part 2, no T gates operate on quantum register \(|z\rangle\).

Step 6: Determine the total number of T gate layers seen by quantum register locations \(|R_{n-2}\rangle\) and \(|R_{n-3}\rangle\) of \(|R\rangle\) in the proposed design. Quantum register locations \(|R_{n-2}\rangle\) and \(|R_{n-3}\rangle\) will see a total of 10 T gate layers from Part 1, \(5 \cdot n - 20\) T gate layers from Part 2 and 13 T gate layers from Part 3. The total T-depth for locations \(|R_{n-2}\rangle\) and \(|R_{n-3}\rangle\) is \(5 \cdot n + 3\). Quantum CTRL-ADD circuits in the literature such as the design in [20] present a constant T-depth to locations \(|R_{n-2}\rangle\) and \(|R_{n-3}\rangle\) of quantum register \(|R\rangle\) when \(|R\rangle\) is supplied as an input. We use a quantum CTRL-ADD circuit that presents a constant T-depth of 13 to locations \(|R_{n-2}\rangle\) and \(|R_{n-3}\rangle\).

Step 7: Determine which qubits see the most T gate layers. We determined that locations \(|R_{n-2}\rangle\) and \(|R_{n-3}\rangle\) see more T gate layers than register \(|z\rangle\) because \(5 \cdot n + 3 > 2 \cdot n\). The number of T gate layers on qubits with the most T gate layers will determine the T-depth for the proposed quantum square root circuit.

Thus, our proposed design has a T-depth of \(5 \cdot n + 3\) and this T-depth is seen by locations \(|R_{n-2}\rangle\) and \(|R_{n-3}\rangle\) of quantum register \(|R\rangle\).

Table 2. Comparison of quantum square root circuits

| design | T-count | T-depth | qubits |
|--------|---------|---------|--------|
| 1      | \(7 \cdot n^2 + 14 \cdot n\) | \(3 \cdot n + 8\) | \(\frac{1}{4} \cdot n^2 + 6 \cdot n - 2\) |
| 2      | \(420 \cdot n^2 + 168 \cdot n - 364\) | NA | \(\approx 42 \cdot n + 10\) |
| 3      | \(\frac{21}{4} \cdot n^2 + \frac{105}{2} \cdot n - 42\) | NA | \(\approx \frac{1}{2} n^2 + 7 \cdot n + 2\) |
| 4      | \(\frac{21}{4} \cdot n^2 + \frac{7}{2} \cdot n - 14\) | NA | \(\approx \frac{1}{2} n^2 + 3 \cdot n + 4\) |
| proposed | \(\frac{7}{2} \cdot n^2 + 21 \cdot n - 28\) | \(5 \cdot n + 3\) | \(2 \cdot n + 1\) |

1 is the design by Sultana et al. [26]
2 is the design by Bhaskar et al. [6]
3 is the first design by AnanthaLakshmi et al. [3]
4 is the second design by AnanthaLakshmi et al. [3]
Table entries are marked NA where a closed-form expression is not available for the T-depth.

4.3 Cost Comparison

The comparison of the proposed quantum square root circuit with the current state of the art is illustrated in Table 2. To compare our proposed square root circuit against the existing designs by Sultana et al. [26] and AnanthaLakshmi et al. [3], we implemented the designs with Clifford+T gates. We also apply the Bennett’s garbage removal scheme (see [5]) to remove the garbage output from the designs by Sultana et al. and AnanthaLakshmi et al. The total qubit cost for each design by AnanthaLakshmi et al. are calculated by summing the garbage output produced by the controlled subtraction circuits and the circuit outputs.
We calculated that our design achieves improvement ratios ranging from $\mathcal{O}(b)$ multiplications and $\mathcal{O}(b)$ additions (where $b$ is the number of bits of accuracy of the solution). We use an implementation that has the lowest possible accuracy and thus let $b = 4$. This is because the T gate and qubit costs increases as a function of solution accuracy. Thus, the square root circuit based on the design by Bhaskar et al. requires 10 multiplications and 6 additions. Bhaskar et al. did not specify a quantum adder or multiplier design for use in their square root quantum circuit design. Therefore, to have a fair comparison against our work we use the quantum adder presented in [28] and the quantum multiplier shown in [20]. The quantum adder has a T-count of $14 \cdot n - 7$, a qubit cost of $2 \cdot n + 1$ and produces no garbage output. Further, the quantum multiplier has a T-count of $21 \cdot n^2 - 14$, a qubit cost of $4 \cdot n + 1$ and produces no garbage output. We assume that given two inputs on quantum registers $|a\rangle$ and $|b\rangle$, the quantum multiplier will produce the product of $|a\rangle$ and $|b\rangle$ on $2 \cdot n + 1$ ancillae. The inputs $|a\rangle$ and $|b\rangle$ will maintain the same value at the end of computation. Consequently, at the end of computation, the square root circuit based on the design by Bhaskar et al. will have garbage outputs. We apply the Bennett’s garbage removal scheme to remove the garbage output from the quantum circuit implementation of the design by Bhaskar et al.

4.3.1 Cost Comparison in Terms of T-count. The T-count cost of the proposed quantum square root circuit and the designs by Sultana et al., Bhaskar et al. and AnanthaLakshmi et al. are of order $\mathcal{O}(n^2)$. We compared the T-count cost of our proposed design methodology to the designs presented by Sultana et al., Bhaskar et al. and AnanthaLakshmi et al. for values of $n$ ranging from 4 to 512. We calculated that our design achieves improvement ratios ranging from 33.33% to 49.61%, 98.41% to 99.16%, 33.84% to 55.56% and 0.00% to 32.64% compared to the designs by Sultana et al., Bhaskar et al. and AnanthaLakshmi et al.

4.3.2 Cost Comparison in Terms of Qubits. Table 2 also shows that our proposed design and the design by Bhaskar et al. have a qubit cost of order $\mathcal{O}(n)$ while the qubit cost for the designs by Sultana et al. and AnanthaLakshmi et al. are of order $\mathcal{O}(n^2)$. We also compared the qubit cost of our proposed design methodology to the designs presented by Sultana et al., Bhaskar et al. and AnanthaLakshmi et al. for values of $n$ ranging from 4 to 512. We calculated that our proposed design methodology achieves improvement ratios ranging from 65.38% to 98.51%, 94.94% to 95.24%, 76.32% to 99.24% and 62.50% to 99.23% compared to the designs by Sultana et al., Bhaskar et al. and AnanthaLakshmi et al.

4.3.3 Cost Comparison in Terms of T-depth. Table 2 illustrates how T-depth and qubit cost are linked and that minimizing one will result in an increase in the other resource cost measure. Table 2 shows that the T-depth of our proposed design and the design by Sultana et al. are of order $\mathcal{O}(n)$. Table 2 illustrates the trade-off between the T-depth and number of qubits. However, the design by Sultana et al. is only able to achieve a constant factor of T-depth improvement against the proposed work at the expense of having a qubit cost of order $\mathcal{O}(n^2)$. Our proposed design achieves a qubit cost of order $\mathcal{O}(n)$. Thus, we significantly reduced the number of qubits in our proposed circuit and maintained a T-depth of the same order ($\mathcal{O}(n)$) as the work by Sultana et al.

5 CONCLUSION

In this work, we present a new design of a quantum square root circuit. The proposed design has zero overhead in terms of garbage output. The proposed design also requires fewer T gates and less qubits than the current state of the art. The proposed quantum square root circuit has been formally verified. The proposed quantum square root circuit could form a crucial component in
the quantum hardware implementations of scientific algorithms where qubits and T-count are of primary concern.

ACKNOWLEDGMENTS

The authors would like to thank the reviewers for their proposed suggestions that helped in further saving of T gates.

REFERENCES

[1] M. Amy, D. Maslov, and M. Mosca. 2014. Polynomial-Time T-Depth Optimization of Clifford+T Circuits Via Matroid Partitioning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 33, 10 (Oct 2014), 1476–1489. https://doi.org/10.1109/TCAD.2014.2341953

[2] M. Amy, D. Maslov, M. Mosca, and M. Roetteler. 2013. A Meet-in-the-Middle Algorithm for Fast Synthesis of Depth-Optimal Quantum Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 32, 6 (June 2013), 818–830. https://doi.org/10.1109/TCAD.2013.2244643

[3] A.V. AnanthaLakshmi and Gnanou Florence Sudha. 2017. A novel power efficient 0.64-GFlops fused 32-bit reversible floating point arithmetic unit architecture for digital signal processing applications. Microprocessors and Microsystems 51, Supplement C (2017), 366 – 385. https://doi.org/10.1016/j.micpro.2017.01.002

[4] S Beauregard. 2003. Circuit for Shor’s algorithm using 2n+3 gubits. QUANTUM INFORMATION & COMPUTATION 3, 2 (MAR 2003), 175–185.

[5] C. H. Bennett. 1973. Logical Reversibility of Computation. IBM J. Res. Dev. 17, 6 (Nov. 1973), 525–532. https://doi.org/10.1147/rd.176.0525

[6] M. K. Bhaskar, S. Hadfield, A. Papageorgiou, and I. Petras. 2016. Quantum Algorithms and Circuits for Scientific Computing. QUANTUM INFORMATION & COMPUTATION 16, 3–4 (MARCH 2016), 197–236.

[7] Donny Cheung, Dmitri Maslov, Jimson Mathew, and Dhiraj K. Pradhan. 2008. Theory of Quantum Computation, Communication, and Cryptography: Third Workshop, TQC 2008 Tokyo, Japan, January 30 - February 1, 2008. Revised Selected Papers. Springer Berlin Heidelberg, Berlin, Heidelberg, Chapter On the Design and Optimization of a Quantum Polynomial-Time Attack on Elliptic Curve Cryptography, 96–104.

[8] S. J. Devitt, A. M. Stephens, W. J. Munro, and K. Nemoto. 2013. Requirements for fault-tolerant factoring on an atom-optics quantum computer. Nature Communications 4, Article 2524 (Oct. 2013), 2524 pages. https://doi.org/10.1038/ncomms3524

[9] Dave Wecker et. al. 2016. Language-Integrated Quantum Operations: LIQUi|> Available at: https://www.microsoft.com/en-us/research/project/language-integrated-quantum-operations-liqui/.

[10] Peter Selinger et. al. 2016. The Quipper System. Available at: http://www.mathstat.dal.ca/ selinger/quipper/doc/.

[11] David Gosset, Vadym Kliuchnikov, Michele Mosca, and Vincent Russo. 2014. An algorithm for the T-count. QUANTUM INFORMATION & COMPUTATION 14, 15-16 (2014), 1261–1276. http://www.rintonpress.com/xxqic14/qic-14-1516/1261-1276.pdf

[12] Su Guodong, S. Shenghui, and X. Maozhi. 2014. Quantum Algorithm for Polynomial Root Finding Problem. In 2014 Tenth International Conference on Computational Intelligence and Security. 469–473. https://doi.org/10.1109/CIS.2014.40

[13] Sean Hallgren. 2007. Polynomial-time Quantum Algorithms for Pell’s Equation and the Principal Ideal Problem. J. ACM 54, 1, Article 4 (March 2007), 19 pages. https://doi.org/10.1145/1206035.1206039

[14] IBM. 2017. Quantum Computing - IBM Q. Available at: https://www.research.ibm.com/ibm-q/.

[15] N. Cody Jones, Rodney Van Meter, Austin G. Fowler, Peter L. McMahon, Jungsang Kim, Thaddeus D. Ladd, and Yoshihisa Yamamoto. 2012. Layered Architecture for Quantum Computing. Phys. Rev. X 2 (Jul 2012), 031007. Issue 3. https://doi.org/10.1103/PhysRevX.2.031007

[16] Igor L. Markov and Mehdi Saedee. 2012. Constant-optimized quantum circuits for modular multiplication and exponentiation. QUANTUM INFORMATION & COMPUTATION 12, 5-6 (2012), 361–394. http://www.rintonpress.com/xxqic12/qic-12-56/0361-0394.pdf

[17] D. Michael Miller, Mathias Soeken, and Rolf Drechsler. 2014. Mapping NCV Circuits to Optimized Clifford+T Circuits. In Reversible Computation, Shigeru Yamashita and Shin-ichi Minato (Eds.), Lecture Notes in Computer Science, Vol. 8507. Springer International Publishing, 163–175.

[18] C. Monroe, R. Raussendorf, A. Ruthven, K. R. Brown, P. Maunz, L.-M. Duan, and J. Kim. 2014. Large-scale modular quantum-computer architecture with atomic memory and photonic interconnects. Phys. Rev. A 89 (Feb 2014), 022317. Issue 2. https://doi.org/10.1103/PhysRevA.89.022317

[19] A. Montanaro. 2014. Quantum pattern matching fast on average. ArXiv e-prints (Aug. 2014). arXiv:quant-ph/1408.1816

[20] E. Muñoz-Coreas and H. Thapliyal. 2017. T-count Optimized Design of Quantum Integer Multiplication. ArXiv e-prints (June 2017). arXiv:quant-ph/1706.05113
Algorithm 39:15

The square root of \( T \)-count and Qubit Optimized Quantum Circuit Design of the Non-Restoring Square Root Algorithm

[21] A. Paler and S. J. Devitt. 2015. An introduction into fault-tolerant quantum computing. In 2015 52nd ACM/EDAC/IEEE Design Automation Conference (DAC). 1–6. https://doi.org/10.1145/2744769.2747911

[22] Alexandru Paler, Ilia Polian, Kae Nemoto, and Simon J Devitt. 2017. Fault-tolerant, high-level quantum circuits: form, compilation and description. Quantum Science and Technology 2, 2 (2017), 025003. http://stacks.iop.org/2058-9565/2/i=2/a=025003

[23] I. Polian and A. G. Fowler. 2015. Design automation challenges for scalable quantum architectures. In 2015 52nd ACM/EDAC/IEEE Design Automation Conference (DAC). 1–6. https://doi.org/10.1145/2744769.2747921

[24] J Proos and C Zalka. 2003. Shor’s discrete logarithm quantum algorithm for elliptic curves. QUANTUM INFORMATION & COMPUTATION 3, 4 (JUL 2003), 317–344.

[25] S. Samavi, A. Sadrabadi, and A. Fanian. 2008. Modular array structure for non-restoring square root circuit. Journal of Systems Architecture 54, 10 (2008), 957 – 966. https://doi.org/10.1016/j.sysarc.2008.04.004

[26] S. Sultana and K. Radecka. 2011. Reversible implementation of square-root circuit. In

[27] Himanshu Thapliyal. 2016. Mapping of subtractor and adder-subtractor circuits on reversible quantum gates. In Transactions on Computational Science XXVII. Springer, 10–34.

[28] Himanshu Thapliyal and Nagarajan Ranganathan. 2013. Design of Efficient Reversible Logic-based Binary and BCD Adder Circuits. J. Emerg. Technol. Comput. Syst. 9, 3, Article 17 (Oct. 2013), 31 pages. https://doi.org/10.1145/2491682

[29] W. van Dam and S. Hallgren. 2000. Efficient Quantum Algorithms for Shifted Quadratic Character Problems. eprint arXiv:quant-ph/0011067 (Nov. 2000). arXiv:quant-ph/0011067

[30] W. van Dam and G. Seroussi. 2002. Efficient Quantum Algorithms for Estimating Gauss Sums. eprint arXiv:quant-ph/0207131 (July 2002). arXiv:quant-ph/0207131

[31] Wim van Dam and Igor E. Shparlinski. 2008. Classical and Quantum Algorithms for Exponential Congruences. Springer Berlin Heidelberg, Berlin, Heidelberg, 1–10.

[32] Paul Webster, Stephen D. Bartlett, and David Poulin. 2015. Reducing the overhead for quantum computation when noise is biased. Phys. Rev. A 92 (Dec 2015), 062309. Issue 6. https://doi.org/10.1103/PhysRevA.92.062309

[33] Xinlan Zhou, Debbie W. Leung, and Isaac L. Chuang. 2000. Methodology for quantum logic gate construction. Phys. Rev. A 62 (Oct 2000), 052316. Issue 5. https://doi.org/10.1103/PhysRevA.62.052316

A EXAMPLE OF THE NON-RESTORING SQUARE ROOT ALGORITHM

In this section, we present an example of Algorithm 1. We shall illustrate the calculation of the square root of 26. We represent 26 as a 6 bit positive binary number in 2’s complement \((a = 011010)\). The square root of 26 is 5 with a remainder of 1. At the end of computation, \(R\) will have the remainder (1) from calculating the square root of 26 and bit positions \(F_4\) through \(F_2\) of \(F\) will contain the square root value \(\bar{Y}\) (where \(Y = 5\)).

| R     | F     | Operations                                                                 |
|-------|-------|----------------------------------------------------------------------------|
| 000001| 000001| \(\text{Assign } R = 0^4a_5a_4\text{ and } F = 0^401\). Where 0^4 are 4 zeros.                               |
| 000000| 000000| \(\text{Calculate } R = R - F\)                                                                                   |
| 000110| 000101| \(i = 2\text{ and } R \geq 0\text{ so } Y_2 = 1\)                                                                 |
| 111101| 000101| \(\text{Assign } R = 00R_1R_0a_5a_2\text{ and } F = 0^3Y_201\). Where 0^3 are 3 zeros. Locations \(R_1R_0\) in \(R\) are shifted and reused. |
| 110110| 001011| \(i = 1\text{ and } R < 0\text{ so } Y_1 = 0\) \(\text{Assign } R = R_3R_2R_1R_0a_5a_0\text{ and } F = 00Y_2Y_111\) Locations \(R_3\) through \(R_0\) in \(R\) are shifted and reused. |
| 000001| 001011| \(\text{Calculate } R = R + F\)                                                                                   |
| 000001| 010101| \(R \geq 0\text{ so } Y_0 = 1\) \(\text{Assign } F = 0Y_2Y_1Y_001\)                                               |
| 000001| 010101| \(\text{Return } F\) and \(R\)                                                                                  |
As expected $R = 000001$ which is the binary representation of the remainder 1. Bit positions $F_4$ through $F_2$ of $F$ contain the values 101 which is the binary representation of the number 5 (the calculated square root value of 26).

Received February 2007; revised March 2009; accepted June 2009