Single-Stage Three-Phase Grid-Tied Isolated SEPIC-Based Differential Inverter With Improved Control and Selective Harmonic Compensation

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ABSTRACT The simple circuit based on DC-DC converters is the main attractive feature of the differential inverter topologies. It has a single-stage and provides modularity and scalability. However, the Negative Sequence Harmonic Component (NSHC) generated at the output terminal may hinder its practical applications. This paper presents a single-stage three-phase isolated differential inverter based on three High-Frequency Link (HFL) transformer-based DC-DC SEPIC converters. The utilized SEPIC converters perform voltage step-up/down capability with galvanic isolation, which is essential for Renewable Energy Sources (RES). It mitigates the Common-Mode Voltage (CMV) and Electro-Magnetic Interference (EMI). Moreover, this paper proposes a two-loop based d-q synchronous frame grid-current control to mitigate its NSHC. A Type-II compensator and simple NSHC detection circuit are proposed to enhance the inverter’s stability and compensate phase-delay of the utilized SEPIC converters. NSHC detection is developed using three cascaded Low Path Filters (LPFs). A 1.6kW inverter prototype was set to validate the performance of the proposed inverter and its control. The control is implemented by the MWPE3 C6713A Expert III DSP board. The proposed topology has a maximum efficiency of 89.744 at 700W output power and 86.4% at full power. The proposed control decreases the NSHC from 40.6% to 1.614%, which shows its accuracy and precision. Furthermore, THD is reduced from 35.61% to 4.087% and satisfy the recent grid codes (<5%).

INDEX TERMS Differential inverter, grid-current control, low-order harmonics, NSHC, HFL transformers, SEPIC converters.

I. INTRODUCTION

The fast penetration of RES, such as Photovoltaics (PVs), increases the popularity of DC-AC power converters at grid-connected applications [1]–[5]. However, the new PV architectures have independent PV modules with low input voltages [6]–[9]. Moreover, the partial shading scenarios force this voltage to be time-variant [8], [10]. This characteristic makes the traditional VSI and CSI have some limitations due to voltage gain property because VSI and CSI are a buck and boost inverter topologies, respectively [3], [8]–[10].

Therefore, inverter topologies with buck/boost features are the modern PV architectures trend with additional functionalities such as voltage isolation, modularity, scalability, and bi-directional power capability [8], [10].

Generally, PV modules are directly connected to the utility grid. The issues related to leakage current and grid-operators safety have been increased. Isolated topologies are recommended to cut the leakage currents, decrease CMV, and EMI to maintain human safety [8], [10]. Also, defining the number of connected PV modules with the utilized inverter topology needs a modular inverter to increase the system’s flexibility and optimize it for further extension in the future [8]. Furthermore, increasing the battery systems at the current...
utility grids, especially the advanced Electric Vehicles (EVs) and charging/discharging stations, put a new direction by optimizing DC-AC inverters with bi-directional power competence [11], [12].

Traditionally, a DC-DC boost converter or isolated DC-DC converters such as flyback, Cuk, and SEPIC converters were added to traditional VSIs to step up the low DC input voltage and generate a buck-boost inverter [13]–[17]. This topology processes the power twice (two-stage inverters), which are extensively studied and adds many limitations for the component count and the control complexity. During the last decade, many topologies have been introduced using the same approach, such as switched-capacitor based inverters [18]–[24], Z source inverters [25]–[29], and multi-level inverters [30]–[32].

In the first topology, a switched-capacitor circuit is used instead of the boost converters [22], [24]. This circuit can charge and discharge in parallel and series to boost the input DC voltage. However, this topology has many component counts, especially at the three-phase systems [18]–[21], and lacks galvanic isolation and modular construction [23]. Also, it has many issues related to the capacitors’ mismatch and their self-voltage balancing [24]. On the other hand, the Z source inverter utilizes Z-network before the VSI stage. This network has many features, such as boosting ability, no dead-time operation, and continuous input current [25]. Although there was an extensive literature for this topology, isolated topologies still need more improvements to reduce the component counts and the size of utilized HFL transformers [8]. Finally, current topologies of multi-level inverters have voltage boosting. However, it is suitable for multi-input inverter topologies rather than single-input inverter topologies [34].

Motivated by this, Single-Stage Buck-Boost Inverter (SSBB-I) topologies become a more important trend. It has one single-stage with a low number of components, such as differential inverters [34]–[54] and split-source inverters [55]–[57]. In between, differential inverter topologies replace every leg of traditional VSI with a DC-DC converter [34]. This new configuration gives many properties such as single-stage, modularity, and isolation using isolated DC-DC converters [51]. The connection of one DC-DC converter per phase provides the unique operation of the differential inverter. It facilitates the power extension (power scalability) by adding parallel converters for every phase without adding control complexity [52]. They have voltage gain with buck-boost features and bi-directional power ability [54].

On the other hand, for control performance [35]–[42], differential inverters incorporate a low number of switches (only six switches for buck-boost DC-DC converters), resulting in uncomplicated gate-driver circuits and simple PWM strategies. The similarity between differential inverters and the traditional VSI inverter expedite the control function, where VSI control was well-known and studied extensively for a long time [42], [53]. Also, it has illustrous programming codes with a small computational burden. The configuration of differential inverters, based on DC-DC converters, is imperative because the DC-DC converters implement small passive elements and improve the stability of the developed control. Finally, the dependency of the differential inverters on DC-DC converters opens the way to improve their performance by benefiting from the tremendous studies applied for DC-DC converters such as dynamic behavior, converter modeling, and stability studies. Using this direction, upgrade their applications and enlarge their accessibility for recent step-up/down three-phase inverter applications [8], [10], and [40]–[50].

However, the differential connection, of step-up/down DC-DC converters, introduces significant low-order harmonic components. It results from the circulating currents between them in addition to their dynamics [42]–[45], [51]–[53]. The current circulation results because the AC grid output voltage is larger than the DC input voltage. Moreover, there is a reverse relationship between these harmonics and passive components of associated DC-DC converters. Although huge passive components damp it a little bit, this solution is not accepted. It adds more size, weight, and cost for the differential inverters and hinders its practical applications.

These low-order harmonics of differential inverter were studied in many papers and covered many buck-boost DC-DC converters such as Cuk, SEPIC, and flyback converter [42]–[54]. For all, these harmonics resulted from two sources and given as:

- Second-order Negative Sequence Harmonic Component (NSHC).
- Other low-order harmonics higher than NSHC such as third-order, fourth-order, and fifth-order components.

For low-order harmonic components, higher than NSHC, the differential inverters’ variable duty cycle was achieved using a sinusoidal duty cycle in many traditional PWM strategies [43]. Using this modulation introduces a mismatch between the actual output voltage and its reference signal for the utilized DC-DC converters. The source of this mismatch is the dynamic behavior of the passive elements (inductors and capacitors), used in the DC-DC converters, toward this modulation. Therefore, many linearization strategies have been developed in many works to mitigate this issue. In [41], [42], a linearization method, for five three-phase buck-boost based differential inverter topologies, was proposed by emerging the voltage ratio of utilized buck-boost converters in the duty cycle calculations. In [43], a Linearization strategy, between the static gain of differential inverter and its output voltage, is proposed for the buck-boost converters. In [44], a static linearization block has emerged at three-phase and single-phase Cuk based differential inverter with input DC voltage feedforwarding. However, these methods successfully reduced low-order harmonics beyond the second-order NSHC.

To inject current free from NSHC, the main loop, introduced for grid-current control, is not enough to mitigate NSHC even at previous static linearization strategies. Therefore, adding a control loop for NSHC mitigation is presented for Cuk differential inverter in [41]. In this loop, a band-path filter is used to extract NSHC from the output.
This paper presents the proposed isolated SEPIC-based differential inverter, as shown in Fig. 1. This inverter has many features such as compact size, low cost, and high power density. Also, this work has developed a generalized mathematical model for NSHC. It is found that the NSHC generates from the differential inverter connection, the unipolar operation of the utilized DC-DC converter, and the variable duty cycle. Then, for the first time, the developed model is used to investigate its concerning effects on the DC source, the SEPIC converters, and the grid. The third part of this work has presented the proposed improved control technique for grid-current control and NSHC mitigation. The first loop of the proposed control has achieved control of the grid-current using type-II compensator. This compensator has enhanced control performance by improving steady-state error, stability, and THD. This control is better than the PID compensator, which developed in previous work. Moreover, this work has developed a general- mathematical model for NSHC. It is found that the power density. Also, this work has developed a general-

voltage and modulate it using a Proportional Resonance (PR) compensator. The same approach is implemented for grid-connected differential inverter topologies based on five different DC-DC buck-boost converters, as presented in [42]. Unlike the continuous modulation scheme (CMS) proposed in [41–42], [51–54], single-phase and three-phase Cuk-based differential inverters using Discontinuous Modulation Scheme (DMS) were presented in [44–45] and [46, 47], respectively. This modulation has decreased the circulating currents between different Cus in both topologies, and thereby, circulating power loss in addition to NSHC. However, the DMS modulation scheme does not remove the whole NSHC but decreases its amplitude and still needs an additional loop. Also, it adds odd harmonics (third-order) that need additional control loops and complicates overall control performance [45].
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**TABLE 1.** Isolated SEPIC converter components with its operational voltages, current and ripple components.

| Component | Voltage | Current | Ripple component |
|-----------|---------|---------|------------------|
| $L_{rx}$  | --      | $n_{lx}d_{rx}$ | $d_{rx}(t)V_{dc}$ |
| $L_{mx}$  | --      | $n_{lx}$ | $-d_{rx}(t)V_{dc}$ |
| $C_{ox}$  | $V_{dc}$ | --      | $\frac{L_{mx}f_{sw}}{n_{lx}d_{rx}(t)}$ |
| $C_{ox}$  | $v_{ox}$ | --      | $\frac{L_{mx}f_{sw}}{i_{gx}(t)}$ |
| $S_{mx}$  | $V_{dc} + v_{ox}$ | $n_{lx}$ | $1 - d_{rx}$ |
| $S_{rx}$  | $V_{dc} + n_{vx}$ | $n_{lx}$ | $\frac{L_{mx} + i_{mx}(t)f_{sw}}{d_{gx}(t)V_{dc}}$ |

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converter, its components ratings and, the total weight of the SEPIC-based differential inverter.

**B. MATHEMATICAL MODELING OF SEPIC DIFFERENTIAL-BASED INVERTER**

For the convenience of analysis, the balanced three-phase voltages at the grid side, shown in Fig 1, are expressed as:

\[
\begin{bmatrix}
    e_{ou}(t) \\
    e_{ov}(t) \\
    e_{ov}(t)
\end{bmatrix}
= e_m \begin{bmatrix}
    \sin (\omega t) \\
    \sin (\omega t - \frac{2\pi}{3}) \\
    \sin (\omega t + \frac{2\pi}{3})
\end{bmatrix}
\]  

(2)

where \(e_m\) is the peak phase voltage and, \(\omega\) is the angular frequency. Time-variant output voltage on each SEPIC converter can be generated using variable duty cycle as portrayed in Fig. 2. The duty cycles are displaced with a 120° phase shift angle to generate three-phase voltages. Therefore, the duty cycle of the SEPIC converters is formulated as:

\[
\begin{bmatrix}
    d_u(t) \\
    d_v(t) \\
    d_w(t)
\end{bmatrix}
= \frac{n * M(1 + K)}{n * M(1 + K) + 1}
\]  

(3)

where \(M\) represents the actual static gain of the differential inverter, see Fig. 2, and the term \(k\) presents the behavior of the grid and given as:

\[
K = \begin{bmatrix}
    \sin (\omega t) \\
    \sin (\omega t - \frac{2\pi}{3}) \\
    \sin (\omega t + \frac{2\pi}{3})
\end{bmatrix}
\]  

(4)

It’s interesting to notice that equation (3) considers the static linearization without any feedforward signals and mitigates low-order harmonics higher than NSHC. The output voltages of the SEPIC converters \(v_{ou}, v_{ov}, v_{ov}\) as shown in Fig 1 and 2, have two different components; a line-frequency sinusoidal component \(e_m\), synchronized with the grid side and a DC offset component \(v_{do}\), which generated due to the variable duty cycle and the unipolar operation of the SEPIC converters. They are expressed as follows:

\[
\begin{bmatrix}
    v_{ou}(t) \\
    v_{ov}(t) \\
    v_{ov}(t)
\end{bmatrix}
= v_{do} + e_m \begin{bmatrix}
    \sin (\omega t) \\
    \sin (\omega t - \frac{2\pi}{3}) \\
    \sin (\omega t + \frac{2\pi}{3})
\end{bmatrix}
\]  

(5)

Owing to the differential connection of SEPIC modules at the grid side as presented in Fig 1, these DC offsets cancel each other at the line-to-line terminal voltages, and in turn, decouple the DC offset voltage from three-phase grid voltages. Since both components results from SEPIC converters, the output voltages of SEPIC converter, derived at (5) can be expressed as:

\[
\begin{bmatrix}
    v_{ou}(t) \\
    v_{ov}(t) \\
    v_{ov}(t)
\end{bmatrix}
= nMV_{dc} + nMV_{dc} \begin{bmatrix}
    \sin (\omega t) \\
    \sin (\omega t - \frac{2\pi}{3}) \\
    \sin (\omega t + \frac{2\pi}{3})
\end{bmatrix}
\]  

(6)

It’s worth noticing that, according to equation 6, \(v_{do}v_{do}\) equals \(e_m\) and, the voltage gain of the differential inverter depends on static gain \(M\) and the turn’s ratio of HFL transformer \(n\).

**C. MATHEMATICAL MODELING OF NSHC**

The output current of the differential inverter is distorted with NSHC even at static linearization that outlined in equation (3). This section describes the modeling of the NSHC and it’s concerning effects on the internal components of the proposed isolated SEPIC converters. For this purpose, the grid current of the SEPIC-based differential inverter is assumed as:

\[
\begin{bmatrix}
    i_{su}(t) \\
    i_{sv}(t) \\
    i_{sw}(t)
\end{bmatrix}
= i_m \begin{bmatrix}
    \sin (\omega t) \\
    \sin (\omega t - \frac{2\pi}{3}) \\
    \sin (\omega t + \frac{2\pi}{3})
\end{bmatrix}
\]  

(7)

+ \(i_h \begin{bmatrix}
    \sin (2\omega t) \\
    \sin (2\omega t - \frac{2\pi}{3}) \\
    \sin (2\omega t + \frac{2\pi}{3})
\end{bmatrix}\)

where, \(i_m, i_h\) represent the maximum current of grid-current and the maximum amplitude of the NSHC, respectively. Multiplying the voltage ratio of SEPIC converters, outlined in equation (6), and the assumed grid current in equation (7) generates the input current of the SEPIC converters. It expressed as:

\[
\begin{bmatrix}
    i_{inu}(t) \\
    i_{inv}(t) \\
    i_{inv}(t)
\end{bmatrix}
= 0.5nMi_m + nMi_m \begin{bmatrix}
    \sin (\omega t) \\
    \sin (\omega t - \frac{2\pi}{3}) \\
    \sin (\omega t + \frac{2\pi}{3})
\end{bmatrix}
\]  

+ 0.5nMi_h \begin{bmatrix}
    \cos (\omega t) \\
    \cos (\omega t - \frac{2\pi}{3}) \\
    \cos (\omega t + \frac{2\pi}{3})
\end{bmatrix}

- 0.5nMi_m \begin{bmatrix}
    \cos (2\omega t) \\
    \cos (2\omega t - \frac{4\pi}{3}) \\
    \cos (2\omega t + \frac{4\pi}{3})
\end{bmatrix}
Moreover, this effect continues to the input current of the DC modules are affected according to equations (7, 8). The practical input current of the SEPIC converters that equals the inductor current \( L_\alpha \) includes the following components:
- DC offset current component, representing the shared average current of each SEPIC module from the DC source.
- Line frequency component, representing the fundamental sinusoidal waveform imposed on the DC component and declares the injected current injection in the grid side.
- Second-order component, representing the circulating currents at reverse power operation and generates the NSHC imposed on grid current.
- Third-order component, representing the component that generates from the current interaction between the reflected NSHC and the circulating currents.

With NSHC, the input and the output current of SEPIC modules are affected according to equations (7, 8). The current of switches, inductors, and HFLs depends on them. Moreover, this effect continues to the input current of the DC source based on the following expression:

\[
I_{dc} = i_{inu} + i_{inv} + i_{invu}
= \frac{3}{2}nMi_h + \frac{3}{4}nMi_h \cos(3wt)
\]  (9)

According to (9), the DC input current is distorted with a third-order component which has many harmful effects, especially for RES. Moreover, this equation proves that no additional loop are desired for this harmonics because NSHC compensation on grid side is enough. In the next sections, the details of the proposed control are presented, which mitigates NSHC and its concerned effects.

### III. LOSS ANALYSIS OF PROPOSED INVERTER

The proposed SEPIC-based differential inverter has three identical SEPIC converters with equal power. Although there is a 120-degree phase shift between them, they have similar duty cycle modulation over one complete cycle with the same peak, average, and valley value [52]. Therefore, the power loss distribution is also the same. This section shows the loss distribution of one SEPIC converter. It has split among the following components.

\[
\begin{bmatrix}
\sin(2wt) \\
\sin(2wt - \frac{4\pi}{3}) \\
\sin(2wt + \frac{4\pi}{3})
\end{bmatrix}
\]

\[
\begin{bmatrix}
\cos(3wt) \\
\cos(3wt - \frac{6\pi}{3}) \\
\cos(3wt + \frac{6\pi}{3})
\end{bmatrix}
\]

(8)

From (8), since the second-order NSHC at the grid current, the practical input current of the SEPIC converters equals the inductor current \( L_\alpha \) includes the following components:

A. **SWITCHES**

As shown in Fig 2 and 3, the main switch \( S_{mx} \) and body diode of the synchronous switch \( S_x \) process the inverter power in the first half of line-frequency cycle \( T_L/2 \) or \( 0 - \pi \) and produce conduction and switching loss. On the other hand, the synchronous switch \( S_x \) and the body diode of the main switch \( S_{mx} \) process the power in the second half \( T_L/2 \) or \( \pi - 2\pi \). To ease the power loss calculation, the conduction and switching loss are calculated based on the switching-frequency \( T_s \). Then the power loss is averaged over the line-frequency \( T_L \).

The conduction loss over one switching cycle \( T_s \) of the MOSFET switch is obtained from equation (10) and can be given as [58]:

\[
P_{cond} = R_{dson}d(t)[I_{D}^2 + \Delta I_D^2/12] \quad (10)
\]

where, \( R_{dson} \) is the on-resistance of the switch, \( d(t) \) is the duty cycle at this instant. \( I_D \) is average drain current over one cycle, and, \( \Delta I_D \) is the ripple component of switch current. Also, the switching loss can be obtained as [59]:

\[
\begin{align*}
P_{sw} &= P_{swon} + P_{swof} + P_{coss} \\
P_{swon} &= \frac{1}{6}t_{rise} F_{sw} V_{ds} \left[ I_D - \frac{\Delta I_D}{2} \right] \\
P_{swof} &= \frac{1}{6}t_{fall} F_{sw} V_{ds} \left[ I_D + \frac{\Delta I_D}{2} \right] \\
P_{coss} &= 0.5 C_{oss} V_{ds}^2
\end{align*}
\]  (11)

In 11, \( t_{rise}, f_{fall}, C_{oss} \) are the rise time, fall time and drain source capacitance of the switch, respectively. All previous parameters were found in the datasheet of the switch. Moreover, the conduction loss of the body diode can be obtained as:

\[
P_{cond} = d(t) I_F V_F \quad (12)
\]

The switching loss of body diode can be obtained as:

\[
\begin{align*}
P_{sw} &= P_{swon} + P_{swof} + P_{Qrr} \\
P_{swon} &= t_{dead} F_{sw} V_F \left[ I_F - \frac{\Delta I_F}{2} \right] \\
P_{swof} &= t_{dead} F_{sw} V_F \left[ I_F + \frac{\Delta I_F}{2} \right] \\
P_{coss} &= 0.5 V_{ds} F_{sw} Q_{rr}
\end{align*}
\]  (13)

In 12 and 13, \( I_F \) is average forward current over \( T_s \), \( V_F \) is the forward voltage of the body diode, \( \Delta I_F \) is the ripple component of diode current, \( t_{dead} \) is the dead time between main and synchronous switch of the SEPIC converter, and \( Q_{rr} \) is the reverse recovery charge of the diode. Table 2 shows the previously calculated parameters of switches and their body diodes and their connected operating period.

### B. INPUT INDUCTOR

The inductor losses are divided to winding conduction losses and magnetic core losses. The winding conduction loss is a function of DC resistance of inductor wire \( R_{dcr} \) and AC...
resistance $R_{acr}$ that indcating the proximity effect of inductor wire at switching-frequency. This loss can be obtained as [60]:

$$P_{cond} = I_i^2 R_{dcr} + \frac{1}{12} \Delta I_i^2 R_{acr} \tag{14}$$

Generally, $R_{dcr}$ and $R_{acr}$ of inductor can be determined using inductor test at switching frequency. Moreover, average inductor current and ripple component are shown in Table 1.

The magnetic core loss of inductor $P_{core}$ depends on the peak ac flux density $B$, the operating switching frequency $F_{sw}$ and the volume of the core and usually obtained by Steinmetz equation to be [61]:

$$P_{core} = k f^\alpha B^\beta A_m l_m \tag{15}$$

where, $A_m$ is the cross-sectional area of the core, $l_m$ is the core mean magnetic path length, $\alpha$, $\beta$ are constants and obtained from the datasheet of the utilized core.

### C. HFL TRANSFORMER

The losses of the HFL transformers are separated into conduction losses and core losses. The conduction losses produce from the primary and secondary resistances of the HFL transformer wires $R_{pri}, R_{sec}$[61]. They are calculated as

$$P_{cond} = \left[ \frac{V_{pri} I_{pri}(t)}{(L_{mx} + L_{pri}) F_{sw}} \right] R_{pri} + \left[ \frac{V_{sec} I_{sec}(t)}{(L_{mx} + L_{sec}) F_{sw}} \right] R_{sec} \tag{16}$$

where, $V_{pri}, V_{sec}$ are the primary and secondary voltages of the transformer, $L_{pri}, L_{sec}$ are the primary and secondary winding inductances of the HFL transformer. Moreover, the core losses can be obtained using equation (15).

### D. COUPLING AND OUTPUT CAPACITORS

From (17), (18), the power losses of both capacitors are obtained as:

$$P_{clas} = \frac{1}{12} \left[ \frac{ni_l d_i(t)}{C_{x} F_{sw}} \right]^2 R_{esr} \tag{17}$$

$$P_{class} = \frac{1}{12} \left[ \frac{ni_s d_i(t)}{C_{x} F_{sw}} \right]^2 R_{esr} \tag{18}$$

where, $R_{esr}$ is the ESR resistance of the capacitor. Finally, the losses of other components such as control circuit, snubber circuit of HFL transformer and connecting wires can be obtained from [58]–[61].

### IV. PROPOSED CONTROL TECHNIQUE

The first step in developing precise control is using a specific open-loop transfer function. The developed SEPIC converter dynamic transfer function derived at [62] is used in this paper. This model considers all interesting parameters needed at the proposed inverter. It expressed as:

$$G_{vd}(s) = \frac{V_{vd}(s)}{d(s)} = \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{19}$$

where, $G_o$ is the dc gain of SEPIC converter, $a_0 \ldots a_3$ represent the constants of its zeros, and $b_0 \ldots b_3$ are the constants of its poles.

The simulation parameters of the utilized SEPIC converter, shown in Table 3, is used to draw the open-loop transfer function and define the exact location of poles and zeros and also decide the stability range of the converter. Using high switching-frequency, $F_{sw} = 50$ kHz enhances the overall size of the SEPIC-based differential inverter by implementing small passive elements. It worth noticing that, the high switching frequency also improves the performance of the closed-loop control because its effect on the line-frequency response is neglected, especially over the entire range of the variable duty cycle $d_x = 0 \ldots 0.8$. This inverter processes 1.6kW active power from a 100V DC source. Finally, table 3 covers the specifications of the grid.

![Proposed control diagram with NSHC compensation circuit.](image)

The CMS operation of the differential inverter produces a second-order NSHC. Therefore, the proposed control has two loops; the first loop for grid-current control. The second loop mitigates the NSHC. Both loops realize their function, as shown in Fig. 4, in the rotating d-q frame. This is based on the grid voltage phase-angle and the use of Clark transformation to obtain currents in the d-q axis. The errors $e_d, e_q$ between the fundamental values of actual and reference currents ($i_d, i_q$ and $i_{refd}, i_{refq}$) are the input of proposed Type-II compensator. This compensator is realized as...
The transfer function of the LPF has formulated as follows:

\[ G_c(s) = G_{co} \frac{(1 + \frac{s}{w_1})}{(1 + \frac{s}{w_2})(1 + \frac{s}{w_3})} \]  

The gain of Type-II, \( G_{co} \), increases the DC gain of the open-loop transfer function of the SEPIC converter, and improves the steady-state error. Zero of the control path, \( w_1 \), boosts the phase delay of the SEPIC converter and enhance the overall inverter stability by expanding the system bandwidth. Therefore, the first pole \( w_1 \) at low frequency flattens the DC gain and increases the control accuracy. The frequency of the second pole \( w_2 \) is high, close to switching frequency, to damp the switching harmonics and eliminate it’s concerning resonance effects from the control path. The compensator outputs \((M, M_q)\), which indicate the static gain of differential based inverter, are then transferred to ABC frame using inverse Clark transformation, representing the first component of the modulation index of each SEPIC converter.

The second loop is disconnected.

In the second loop, the proposed detection circuit of NSHC is based on three cascaded low-pass filters (LPFs). The output sensors of the grid current have delivered to the proposed LPFs. These LPFs accurately mitigate all low-order harmonics and obtain fundamental components of grid currents. Then, the output of LPFs is extracted from the actual grid currents to detect the second-order NSHC, as shown in Fig. 4. The transfer function of the LPF has formulated as follows:

\[ G_s(s) = \frac{1}{(1 + \frac{s}{w_1})^3} \]

This transfer function of LPFs has -60DB per decade response due to the located three poles. In addition to pole of Type-II, there are four poles in the system and, all damp the switching harmonics and the resonance produced between capacitors and inductors of SEPIC converter. The Clark transformation achieves the operation between ABC frame and d-q frame at the angular frequency \((-2omega)\). Then, the cascaded integrator attenuates the errors of the NSHC loop by modulating the duty cycle of each SEPIC converter. Finally, the dynamic behavior of integrators in the second loop is slow to prevent any distortion on the first loop.

The closed-loop transfer function of SEPIC-based differential inverter that uses the proposed control is then expressed as follows:

\[ T(s) = G_{vd}(s) \ast G_R(s) \ast G_{c2}(s) \ast d_s(s) \]  

Here \( G_{c2}(s) \) is the total transfer function of both loops, \( G_R(s) \) is the transfer function of grid side inductance, shown in Fig. 1. \( d_s(s) \) represents the transfer function of static linearization function based on equation (3). At frequency domain, it is expressed as:

\[ d_s(s) \approx \frac{m(s) + m(s)K}{m(s) + m(s) + 1} \]

where, \( m(s) \) is the small signal component of static gain of differential inverter. According to the proposed control, the bandwidth of the closed-loop transfer function of the SEPIC converters is 590Hz. The DC gain and the phase margin are 98DB and 38.2, respectively, as shown in Fig. 5.

### Simulation Parameters of Proposed Isolated SEPIC-based Differential Inverter

| component                  | value | Unit |
|----------------------------|-------|------|
| Rated Power, P             | 1600  | W    |
| Input DC Voltage, \( V_{dc} \) | 100   | V    |
| Grid Voltage, \( V_g \), \( \omega \) | 200, 2\pi * 60 | V, rad/sec |
| Switching Frequency, \( F_{sw} \) | 50    | kHz  |
| Input inductor, \( L_x \)  | 180   | uH   |
| HFL transformer inductance, \( L_{ms} \) | 500   | uH   |
| HFL transformer turns ratio \( n \) | 1     | --   |
| Coupling capacitor, \( C_x \) | 14    | uF   |
| Output capacitor, \( C_{ox} \) | 14    | uF   |
| Grid inductance, \( L_{gs} \) | 4     | mH   |

### V. SYSTEM RESULTS AND DISCUSSION

Simulation and experimental results have been conducted in this section to verify the effectiveness of the proposed control technique and the theoretical assumptions. To consider the mathematical analysis of NSHC, two case studies have been provided as:

- Case 1: This case discusses the effect of NSHC on the SEPIC converters, DC source, and grid. The control task includes Type-II compensators in the first loop. The second loop is disconnected.
- Case 2: This case shows the features of the proposed NSHC strategy using the proposed LPFs. The control task includes the Type-II compensator in the first loop as well as LPFs and integrators in the second loop.

Both cases have performed using PSIM 11.1.3 software and MWPE3 C6713A Expert III DSP board. MWPE3 FPGA board is used to generate the gate pulses of switches. Fig. 6 shows the experimental setup of the proposed SEPIC-based differential inverter with modified grid-current control. In this setup, three HFL transformers is designed and
implemented using ferrite cores and litz wires to get high performance. Fig. 7 shows the implemented PCB board of one SEPIC converter. The SEPIC converters are designed and implemented on separate PCP boards to provide modularity and plug and play operation [52]. Only five sensors are used (two for line-line voltages and three for grid currents). Table 4 demonstrates the experimental parameters of the inverter setup.

A. CASE 1: NSHC ISSUE

Fig. 8 and 9, show the simulation and experimental results of proposed isolated SEPIC-based differential inverter at case 1. The proposed Type-II compensator has achieved grid-current control and injected active power. However, the grid current in both have distorted with NSHC even at applying static linearization. These findings of simulation and experimental results match the theoretical assumptions and the literature work of differential inverters. This NSHC component is reflected in SEPIC converters and DC voltage source, as shown in the input currents and the DC current. Again, these results are matched with our assumptions derived at equations (7, 8, and 9). Moreover, the reflection of NSHC on the DC source current generates a third-order component that complies with equation (9).
parasitic of SEPIC converters, such as DC resistances of the PCB boards and connecting wires, are the source of this difference. This difference also introduced at the FFT harmonic spectrum of the grid-current (simulation and experimental results), as presented in Fig. 10. It shows that the percentage of second-order NSHC is about 25.81% and 40.6% for simulations and experiments. For the THD, the proposed inverter has 23.45% and 35.61% from simulations and experiments. Practically, Table 5 illustrates the percentage of other low-order harmonics. It's shown that the proposed static linearization strategy eliminates the other components, and there is a reflection of NSHC on input current of the SEPIC converter. This harmonic violates the IEC-61000 grid standards [65] and hinders the differential-based inverter’s practical applications, as shown in Fig. 11. Finally, all previous results have shown the serious deformation of NSHC on the proposed differential inverter and the ultimate need for additional loop for NSHC mitigation.

### FIGURE 10. FFT harmonic spectrum of grid-current at case 1.

#### TABLE 4. Experimental parameters of proposed isolated SEPIC-based differential inverter.

| component       | specifications |
|-----------------|----------------|
| Input Inductor  | \(L_x\) 181.9\(\mu\)H |
|                 | \(R_{acr}\) 200m\(\Omega\) |
|                 | core EER-94 |
| No. of turns    | 37 |
| HFL transformer | \(L_{ecl}\) 493.28\(\mu\)H |
|                 | \(R_{pri}\) 50m\(\Omega\) |
|                 | \(R_{sec}\) 65m\(\Omega\) |
|                 | core EER-94 |
| Turns ratio 1:n | 1:1 |
| No. of turns (primary) | 15 |
| Switches        | \(R_{agon}\) 40m\(\Omega\) |
|                 | \(V_F\) 1.8v |
|                 | \(t_{rise}\) 52ns |
|                 | \(t_{fall}\) 34ns |
| Capacitors      | \(C_x\) C4AE0BW5140A3JJ |
|                 | \(C_{ox}\) C4AE0BW5140A3JJ |
|                 | \(R_{exr}\) 5.4m\(\Omega\) |
| Grid inductance | \(L_{gx}\) 4m\(\Omega\) |
|                 | \(R_{gx}\) 0.2\(\Omega\) |

#### TABLE 5. Low-order harmonic components percentages of proposed inverter at case 1.

| Current/ Harmonic Order | 2 | 3 | 4 | 5 |
|-------------------------|---|---|---|---|
| Grid current \(i_{gw}\) | 25.81 | 0.204 | 0.605 | 0.235 |
| Input Current \(i_{inw}\) | 27.32 | 10.55 | 0.902 | 0.312 |

**B. PROPOSED CONTROL AND NSHC COMPENSATION STRATEGY**

Fig. 12 and 13 show the simulation and experimental results of case 2 that consider the proposed HSHC compensation circuit. In both, the proposed control technique injects sinusoidal current to the grid at unity power factor. Compared with case 1, the proposed control technique successfully eliminates the NSHC from the grid current.

Moreover, it reduces the distortion of the three input inductor currents of SEPIC converters and their mismatch. It eliminates the third-order component from the DC source due to the successful elimination of the NSHC of grid-current. Fig. 14 shows the FFT harmonic spectrum of the injected grid current at case 2 for simulation and experimental results.
The percentage of second-order NSHC reduced from 25.81% to 0.278% in the simulations. Also, it reduced from 40.6% to 1.6143% at the experiments. The successful mitigation of NSHC forces the third-order harmonics at the input of SEPIC converters to reduce from 17.54% to 2.13% in the experimental results. The simulations results also have the same improvements, as illustrated in Table 6. The maximum regulation limit of the harmonic components in case 2 is reduced from 150% to 70% as shown in Fig. 15. It confirms that the differential-based inverter using proposed control meets the standard limits of IEC-61000.

### TABLE 6. Low-order harmonic components percentages of proposed inverter at case 2.

| Harmonic order | 2 | 3 | 4 | 5 |
|---------------|---|---|---|---|
| Grid current $i_{sw}$ | 0.278 | 0.575 | 0.06 | 0.169 |
| Input Current | 35.05 | 1.08 | 0.175 | 0.191 |

### C. POWER LOSS DISTRIBUTION AND EFFICIENCY

The power loss distribution for the proposed inverter topology has been carried out based on the mathematical calculation derived in section III. The semiconductor devices, inductors, HFL transformer, and capacitors are modeled using their datasheets. Table 7 gives the power loss of all components for one SEPIC converter together with the calculated efficiency with an output power of 533 W. Then the power of proposed inverter equal to 1.6 kW using one SEPIC converter per phase.
FIGURE 15. IEC-61000 standards compared with FFT spectrum of experimental grid-current at case 2.

TABLE 7. Calculated power loss distribution of one SEPIC converter at proposed inverter topology.

| component                        | $P_{cond}$ | $P_{Sw}$ | total |
|----------------------------------|------------|----------|-------|
| Main Switch $S_{mx}$             | 6.351      | 3.666    | 10.017|
| Body diode of main Switch $S_{mx}$| 2.310      | 1.335    | 3.645 |
| Synchronous Switch $S_{xx}$      | 1.558      | 1.429    | 2.987 |
| Body diode of Synchronous        | 4.739      | 1.884    | 6.623 |
| Switch $S_{xx}$                  |            |          |       |
| Input Inductor $L_{S}$           | 10.250     | 8.000    | 18.250|
| HFL transformer $N_{H}$          | 11.235     | 8.184    | 19.417|
| Coupling capacitor $C_{x}$       | 0.007      |          |       |
| output capacitor $C_{ox}$        | 0.002      |          |       |
| Snubber circuit                  | 2.2        |          |       |
| Grid inductance                  | 3.07       |          |       |
| Control and gate drives          | 0.883      |          |       |
| Total power loss and output      | 67.121     | 533      |       |
| Power W Efficiency               |            |          | 87.406%|

FIGURE 16. Efficiency vs output power of the proposed inverter.

Moreover, the variation of efficiency against injected output power with loss calculation using mathematical, simulation and experimental measurements are shown in Fig. 16. The maximum experimental efficiency of the proposed inverter has a value of 89.744% at the output power of 700W. As the output power increases, the efficiency decreases to 86.4% at full rating of the proposed inverter 1.6kW. It’s worth noticing that the drop is low and the difference between calculated, simulated and experimentally measured efficiency is small due to the accuracy of loss modeling derived at section III.

D. DISCUSSION, COMPARISON AND EVALUATION

In Table 8, comparative evaluation between the proposed inverter and state of the art topologies have been carried out in terms of topology, voltage gain, voltage step-up/down ability, different components count and power rating. Also, it includes the feasibility of the topologies for modularity, galvanic isolation, and power efficiency. The proposed inverter requires low number of switches (six switches like the traditional VSI) which is less than the proposed topologies in [22], [24], [26], and [33]. Furthermore, it does not need any diodes like topology proposed in [25]. Another exciting benefit of the proposed topology is the galvanic isolation using HFL without any additional switches. Finally, it has an excellent potency to be modular and scale the power for over extension.

The switched-capacitors inverters still need improvements in terms of switches, where topologies in [22] and [24] have 8 and 27 switches with many gate drive circuits. It does not have a modular configuration, and the HFL integration is still not investigated. For Z source inverter topologies, the buck-boosting ability is excellent. However, the Z network’s size is still substantial (they have inductors in mH range) [25]. Again, it needs additional components to implement galvanic isolation and modularity. For multi-level inverters, the efficiency is generally high. However, the number of switches is very high and needs large filters due to low switching-frequency.

In contrast, Table 8 gives a quantitative comparison between the proposed inverter and similar differential inverter topologies. The proposed topology based on SEPIC converters has only three inductors, which is lower than the Cuk topologies (six inductors). Furthermore, the utilized inductors have small values that improve the inverter size. Although the measured efficiency of the proposed topology is close to proposed one in [44], it has many advantages to enhance it in the future.

Table 9 summaries the literature work, which eliminates NSHC at differential inverters. The proposed control design provides grid-current control and excludes NSHC by using two control loops. NSHC can be decreased partially by using DCM operation, as reported at [44]. However, this will add higher-order harmonic components (i.e., third, fourth, and extra) that disturb THD, and need extra loops. The DCM Cuk-based differential inverter at [44] needs more loops to decrease THD to acceptable values, as outlined at [45]. Moreover, the utilization of second loop from the perspective of input current distortion. It is imperative to exclude the third loop, which adds complexity and a computational burden for utilized DSP board.

Unlike [42], the proposed control eliminates the third-order components using the second loop from the perspective of input current distortion. As the output power increases, the efficiency decreases to 86.4% at full rating of the proposed inverter 1.6kW. It’s worth noticing that the drop is low and the difference between calculated, simulated and experimentally measured efficiency is small due to the accuracy of loss modeling derived at section III.

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Moreover, it provides accurate mathematical modeling for its association with NSHC. Also, this behavior has been verified using simulations and experiments.
VI. CONCLUSION

This paper has presented a single-stage three-phase HFL transformer SEPIC-based differential inverter with a new mathematical model and control technique to minimize the NSHC of the grid injected current. This model successfully demonstrates the source of NSHC. In the proposed control, the Type-II compensator successfully enhances SEPIC converters’ stability and achieves grid current control with a small steady-state error. In the second loop, a simple NSHC detection circuit, constructed from three cascaded Low Path Filter (LPFs), is proposed to improve the quality of the grid current by mitigating the NSHC. The proposed LPFs have extra poles that damp the switching harmonics in addition to the poles of Type-II and gives better performance. The proposed control injects sinusoidal current to the grid at a unity power factor that meets the permissible limits for all harmonic contents of IEC61000 standards. The validity of the proposed control techniques is investigated in simulation and experiments using PSIM software and laboratory prototype of 200V, 1.6kW, 50 kHz, and achieving THD of 4.087% for the grid current with the proposed compensation technique. The maximum measured efficiency of the proposed inverter is 89.744% at the output power of 700W and 86.4% at full power. Finally, the proposed inverter is modular and can be extended by adding new SEPIC converters without additional complexity for the control.

Table 10 demonstrates the performance of proposed control techniques with our previous work [52]. It worth noticing that both controllers provide high performance. Moreover, the proposed improved control has low execution time that improves the computational burden of the DSP board. The NSHC is less than 1.6143% that enhances the THD (less than 5%). Finally, these findings achieve the standards of recent grid codes.

### TABLE 8. Comparison between proposed inverter and similar topologies.

| Topology | Topology | Voltage gain | Power (KW) | Capacitors% inductors | Switches Diodes | Modular CMV | HFL& Application | Measured efficiency |
|----------|----------|--------------|------------|----------------------|-----------------|-------------|-----------------|---------------------|
| Ref[22]  | Switched | Buck-Boost   | NA         | 2                    | 8               | No          | No              | Three-phase         | 97.4                |
|          | Capacitor|              |            | 0                    | 2               |             |                 |                     |                     |
| Ref[24]  | Switched | Buck-Boost   | NA         | 2                    | 27              | No          | No              | Three-phase         | NA                  |
|          | Capacitor|              |            | 0                    | 0               |             |                 |                     |                     |
| Ref[25]  | Z source | Buck-Boost   | 0.45       | 2                    | 6               | No          | No              | Three-phase         | NA                  |
|          |          |              |            | 2                    | 1               |             |                 |                     |                     |
| Ref[26]  | Z source | Buck-Boost   | 1          | 2                    | 6               | No          | No              | Three-phase         | 97.1                |
|          |          |              |            | 2                    | 1               |             |                 |                     |                     |
| Ref[33]  | Multi-level | Buck | 1.1       | 5                    | 8               | Yes          | No              | Single-phase        | 96.3                |
|          |          |              |            | 0                    | 6               |             |                 |                     |                     |
| Ref[37]  | Differential | Buck-Boost | 1.4       | 3                    | 6               | Yes          | No              | Three-phase         | NA                  |
|          |          |              |            | 3                    | 0               |             |                 |                     |                     |
| Ref[38]  | Differential | Buck-Boost | 0.5       | 3                    | 4               | Yes          | No              | Single-phase        | 97                  |
|          |          |              |            | 4                    | 2               |             |                 |                     |                     |
| Ref[41]  | Differential | CUK     | 2.5       | 6                    | 6               | Yes          | No              | Three-phase         | NA                  |
|          |          |              |            | 2                    | 6               |             |                 |                     |                     |
| Ref[42]  | Differential | CUK     | 2.5       | 6                    | 6               | Yes          | Yes             | Three-phase         | NA                  |
|          |          |              |            | 2                    | 6               |             |                 |                     |                     |
| Ref[43]  | Differential | Boost    | 0.5       | 2                    | 4               | NO           | No              | Single-phase        | NA                  |
|          |          |              |            | 2                    | 0               |             |                 |                     |                     |
| Ref[44]  | Differential | CUK     | 0.5       | 6                    | 6               | Yes          | yes             | Three-phase         | 91%                 |
|          |          |              |            | 6                    | 0               |             |                 |                     |                     |
| Ref[47]  | Differential | Buck     | 0.4       | 3                    | 4               | Yes          | No              | Three-phase         | NA                  |
|          |          |              |            | 3                    | 0               |             |                 |                     |                     |
| proposed | Differential | SEPIC | 1.6       | 6                    | 6               | Yes          | yes             | Three-phase         | 89.744              |
|          |          |              |            | 3                    | 0               |             |                 |                     |                     |

Table 10 demonstrates the performance of proposed control techniques with our previous work [52].
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