Quantum Error Correction on Linear Nearest Neighbor Qubit Arrays

Austin G. Fowler\textsuperscript{1}, Charles D. Hill\textsuperscript{2} and Lloyd C. L. Hollenberg\textsuperscript{1}

\textsuperscript{1}Centre for Quantum Computer Technology, School of physics
\textsuperscript{2}University of California, Berkeley, California 94720, USA.

(Dated: October 31, 2018)

The field of quantum computation deals with the manipulation of 2-state quantum systems called qubits. Many different physical systems are being investigated in the race to build a scalable quantum computer \textsuperscript{1} 2 3 4 5. Due to the fragility of quantum systems, one property a scalable architecture must possess is the ability to implement quantum error correction (QEC) \textsuperscript{6} 7 8. This requirement arises with and without QEC are presented. The paper is organized as follows. Firstly, the canonical decomposition used to construct efficient two-qubit gates is discussed in brief. Details of the method used can be found in \textsuperscript{31}. The Kane architecture \textsuperscript{11} has been used to construct explicit decompositions, but the methods described apply to any architecture. The 5-qubit QEC scheme is then discussed and the LNN circuit presented. Following this, simulations of quantum data storage with and without QEC are presented. The paper concludes with a summary of all results.

The canonical decomposition enables any 2-qubit operator $U_{AB}$ to be expressed (non-uniquely) in the form $V_A^\dagger \otimes V_B^\dagger U_{d} U_A \otimes U_B$ where $U_A$, $U_B$, $V_A$ and $V_B$ are single qubit unitaries and $U_d = \exp[i(\alpha_x X \otimes X + \alpha_y Y \otimes Y + \alpha_z Z \otimes Z)]$ \textsuperscript{30}. Moreover, any entangling interaction can be used to create an arbitrary $U_d$ up to single qubit rotations \textsuperscript{31}. These two facts allow the construction of very efficient composite gates on any physical architecture. Fig. 1b shows the form of such a decomposed controlled-NOT (CNOT) on a Kane quantum computer \textsuperscript{1} 32. The 2-qubit interaction corresponds to $\alpha_x = \alpha_y = \pi/8$, and $\alpha_z = 0$. Z-rotations have been represented by quarter, half and three-quarter circles corresponding to $R_z(\pi/2)$, $R_z(\pi)$, and $R_z(3\pi/2)$ respectively. Full circles represent $R_y$-rotations of angle dependent on the physical construction of the computer. Square gates 1 and 2 correspond to X-rotations $R_x(\pi)$ and $R_x(\pi/2)$. Fig. 1a shows an implementation of the composite gate Hadamard followed by CNOT followed by swap (HCNOTS). Note that the total time of the compound gate is significantly less than the CNOT on its own.

The implication of the above is that the swaps inevitably required in an LNN architecture to bring qubits together to be interacted can be incorporated into other gates without additional cost. Indeed, in certain cases LNN circuits built out of compound gates are actually faster. With careful planning, general quantum circuits can be implemented on an LNN architecture with asymptotically the same number of gates as that required on an architecture that allows any pair of qubits to be interacted.

5-qubit quantum error correction schemes are designed to correct a single arbitrary error. No single error correction scheme can use less than 5 qubits \textsuperscript{20}. A number of 5-qubit QEC proposals exist \textsuperscript{2} 3 8 9 29 35 36. Fig. 2a shows a circuit optimized for an LNN architecture implementing the encode stage of the QEC scheme proposed in \textsuperscript{29}. For reference, the original circuit is shown in fig. 2b. Note that the LNN circuit uses exactly the same number of CNOTs and achieves minimal depth. The two extra swaps required do not significantly add to the total time of the circuit. Fig. 2b shows an equivalent physical circuit for a Kane quantum computer. Note that this circuit uses the fact that if two 2-qubit gates share a qubit then two single-qubit unitaries can be combined as shown in fig. 2d. The decode circuit is simply the encode circuit run backwards. All 5-qubit QEC schemes are only useful for correcting a single arbitrary error. No single error correction scheme can use less than 5 qubits 20. A number of 5-qubit QEC proposals exist 2 3 8 9 29 35 36. Fig. 2a shows a circuit optimized for an LNN architecture implementing the encode stage of the QEC scheme proposed in 29. For reference, the original circuit is shown in fig. 2b. Note that the LNN circuit uses exactly the same number of CNOTs and achieves minimal depth. The two extra swaps required do not significantly add to the total time of the circuit. Fig. 2b shows an equivalent physical circuit for a Kane quantum computer. Note that this circuit uses the fact that if two 2-qubit gates share a qubit then two single-qubit unitaries can be combined as shown in fig. 2d. The decode circuit is simply the encode circuit run backwards. All 5-qubit QEC schemes are only useful for data storage due to the difficulty of interacting two logical qubits. Fig. 2c shows a full encode-wait-decode-measure-correct data storage cycle. Table 1 shows the range of possible measurements and the action required in each case.

When simulating the QEC cycle, the circuit of fig. 2b was used to keep the analysis architecture independent. Each gate was modeled as taking the same time, allowing the time $T$ to be made an integer such that each gate takes one time step. Gates were furthermore simulated as though perfectly reliable and errors applied to each
FIG. 1: Decomposition into physical operations of a.) CNOT gate b.) Hadamard, CNOT then swap. Note that the Kane architecture has been used for illustrative purposes. In addition to the clear speed advantage when implementing compound gates, the decomposed CNOT gate is faster than its adiabatic equivalent (26\(\mu\)s) [33].

\[ H_1 = R_x(\pi/2) \]

\[ = R_y(\pi) \]

\[ \Phi = R_z(\pi/2) \]

\[ \Phi = R_z(\pi) \]

\[ \Phi = R_z(3\pi/2) \]

\[ \Phi = R_z(\pi) \]

\[ n = e^{|i\pi(XX+YY)/n} \]

FIG. 2: a.) 5-qubit encoding circuit for general architecture b.) equivalent circuit for linear nearest neighbor architecture with dashed boxes indicating compound gates. CNOT gates that must be performed sequentially are numbered.
\( \epsilon_{\text{step}} \) and the reduction in error \( \epsilon_{\text{step}}/p \) versus \( p \) for discrete errors. Table II shows the corresponding data for continuous errors. Note that, in the continuous case, the single qubit \( p \) has been obtained via 1-qubit simulations and a 1-qubit version of equation \( 3 \).

An enormous range of threshold error rates \( p \) exist in the literature. These start at a very pessimistic \( p = 10^{-8} \) and go up to a very optimistic \( p = 2 \times 10^{-3} \) \( 37 \). The first thing that can be noted from the discrete simulation data of Table I is that the LNN threshold \( p = 1.6 \times 10^{-3} \) is comparable to the most optimistic previous estimate
which was made using 7-qubit fault tolerant QEC with errors applied only after gate operations and not to idle qubits. The error rate $p = 1.6 \times 10^{-3}$ should not however be thought of as the allowable operating error rate of a physical quantum computer as precisely no improvement in error rate is achieved when using QEC. If an error rate improvement of a factor of 10 or 100 is desired when using QEC then $p = 10^{-5}$ or $p = 10^{-7}$ is required respectively. Further work is required to determine the error rate improvement required to allow robust implementation of large scale quantum algorithms with a reasonable number of error correction qubits.

For continuous errors, there is no true threshold. Even for very large random unitary rotations an improvement is still gained by using the LNN QEC circuit. In this case, provided gates can be implemented such that the angles associated with the continuous error model are of order $10^{-2}$, an improvement in error rate of at least a factor of 10 can be achieved.

Further work is required to determine whether the discrete or continuous error model or some other model best describes errors in physical quantum computers.

In conclusion, we have presented an efficient circuit for 5-qubit QEC on an LNN architecture and simulated its effectiveness against both discrete and continuous errors. It was found that, for the discrete error model, if error correction is to provide an error rate reduction of a factor of 10 or 100, the physical error rate $p$ must be $10^{-5}$ or $10^{-7}$ respectively. For the continuous error model, it was acceptable for error angles to have a standard deviation of up to $10^{-2}$ radians as using QEC still gives an error rate improvement better than a factor of 100.

Further simulation is required to determine the error thresholds associated with 1- and 2-qubit LNN error-corrected gates.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig5.png}
\caption{A complete encode-wait-decode-measure-correct QEC cycle.}
\end{figure}
[38] C. Zalka, quant-ph/9612028 (1996).