The concept of PICaboo

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The concept of PICaboo: from individual building blocks to complex photonic integrated circuits for future access and metro networks

Giannis Kanakis1,*, Maria Spyropoulou2, Giorgos Brestas3, Weiming Yao4, Jos J G M van der Tol5, Alessio Miranda6, Kolsoom Mehrabi7, Dhiman Nag8, Christophe Caillaud9, Vladyslav Vakarin1, Jordi Soler Penades1, Inigo Artundo1, Rene Bonk1, Robert Borkowski1, Despoina Petousi6, Pablo Castro Ayala1, Michael Eisel1 and Hercules Avramopoulos1

1 Photonics Research Communications Laboratory, School of Electrical and Computer Engineering, National Technical University of Athens, Athens, Greece
2 Institute of Photonic Integration, Technical University of Eindhoven, Eindhoven, The Netherlands
3 III-V Lab, Palaiseau Cedex, France
4 VLC Photonics Sociedad Limitada, Valencia, Spain
5 NOKIA Solutions and Networks GmbH & Co. KG, München, Germany
6 ADV A Optical Networking SE, Meiningen, Germany
* Author to whom any correspondence should be addressed.
E-mail: giankan@mail.ntua.gr

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Abstract
The immense growth of data traffic that traverses modern networks, calls for immediate solutions to tackle the challenges that arise in terms of speed, capacity, cost and energy efficiency. This manuscript outlines the key technological aspects of the PICaboo project, that aims to develop novel building blocks and photonic integrated circuits for the next generation of optical metro and access networks enhanced with optical signal processing functionalities exploiting the generic foundry model approach.

1. Introduction

Telecom operators are standing at a critical crossroads. While the quest for higher capacity at a lower cost per bit is ubiquitous, modern needs are pushing traffic towards the edge of the network; mobile users demand access to bandwidth hungry applications such as ultra-high-video streaming, online gaming and the metaverse, while at the same time a significant portion of the consumer traffic is shifted towards the home to support small office home office and entertainment. Furthermore, the adoption of 5G and the Internet of things (IoT) imposes stringent latency constraints and high availability to satisfy massive machine-type communication. Meanwhile, this immense traffic volume that originates from the access segment of the network, has a knock-on effect on the optical metro and dictates an upgrade of the existing transport equipment. This tremendous volatility of the networking landscape highlights the necessity for a paradigm shift [1].

Photonic integration is considered a key enabling technology leading to the development of new products and services with substantial economic benefits. The global photonics market has gained significant momentum in various segments including information and communication technology, light sources, displays, medical technology and life sciences [2] and it is expected to turn into a multi-billion Dollar market by 2024 [3]. Indium phosphide (InP) has played a key role in the development and commercialization of high-performance optical components and optoelectronic devices due to its demonstrated capabilities for efficient amplification, high speed modulation and detection, low propagation loss and compact chip area. InP photonic integrated circuit (PIC) technology has been the workhorse for the development of optical transceivers for metro/core and access networks due to its high-speed operation potential and its capability for large scale monolithic integration [4–6]. Despite its high-performance characteristics e.g. large
electro-optic bandwidth and ultra-fast response it is considered inherently an expensive technology compared to silicon photonics which relies on low cost CMOS processes. Significant efforts towards decreasing development costs and lowering the boundaries for fast prototyping is pursued via JePPIX pilot line, the EC manufacturing pilot line project for photonic integrated circuits based on InP, through open access to multi-project-wafer runs from its foundries [7]. European InP foundries have specific process design kit (PDK) libraries including building blocks which can be used by designers in order to develop application-specific PICs with predictable performance. This means that the processes used for the development of a building block with certain performance do not affect the performance of a neighbouring building block.

The aggregation of multiple functionalities on a single chip is very important for bandwidth-hungry cloud and IoT applications considering that transceiver capacity can easily be increased via channel parallelization and multiplexing of the optical wavelengths, yielding in tandem significant cost benefits due to the reduced assembly complexity and its associated costs. Moreover, scaling to larger capacities usually implies the need for stronger digital signal processing (DSP) both at the transmitter and at the receiver side, which in turn increases the overall power consumption and dictates stricter requirements for cooling and airflow management at the front panel of digital switches. Optical signal processing has been extensively researched in the past decades towards the realization of transparent all-optical networks via complex functionalities like all-optical regeneration, all-optical switching etc. [8, 9] but the advent of coherent technologies, after 2010 widely deployed in metro and longhaul networks, addressed most of these by means of electronic DSP. In the access networks, simple intensity modulated/direct detection (IMDD) technologies have been widely deployed at low speed (GPON, XGS-PON). However, this scenery will rapidly change considering the fast uptake of 5G and 6G services.

In this communication, we report on the technological advancements that the European H2020 project PICAST envisions in order to tackle the challenges that arise in modern metro and access networks, as well as to overcome the economical and technological barriers that the vertical fabs’ paradigm is creating towards the vast development of photonic components.

2. The PICaboo concept and approach

2.1. The generic foundry model approach

The generic foundry model allows for decoupling between PIC design and fabrication and enables designers to create new circuits with the freedom to place building blocks to suit circuit needs across markets and product generations [10]. Besides, it fosters innovation through early adoption of the technology by end-users and through fast prototyping, yielding the development of innovative commercial products. Additionally, integration platforms offer a fast-track to custom integration for the ultimate performance with high-volume products. The co-integration of multiple building blocks on the generic platform requires precise control of the fabrication steps. Within PICaboo the InP PIC platforms of TU/e and III-V Lab will be enhanced via the development of new building blocks to keep pace with the high speed, low power and enhanced functionality requirements dictated by application roadmaps. The developed building blocks will bring significant advancements to the InP PIC platforms of the two fabs compared to the current state-of-the-art. Technology development will rely on the generic process flow rules which are specific to each PIC platform. This means that every novel or performance-enhanced building block that will be developed will follow a standardized procedure in order to be included in the generic PDK of the respective platform. For each new building block that will be developed, compact models will be generated and will be continuously updated based on the obtained measurement data from every fabrication cycle.

In more detail, TU/e will enrich its InP PIC platform with respect to three main pillars: (a) uniform component performance across a wide wavelength range: the passive and active building blocks to be developed will exhibit ultra-wideband operation across 100 nm over the S- and C- bands to enable multi-band WDM applications; (b) increase the platform speed capabilities to keep up with the capacity requirements of modern applications: high-speed photodetectors and photodetector arrays capable of 50 Gbaud operation will be developed and integrated into coherent optical receiver PICs; (c) harness the signal polarization on-chip: accurate polarization handling is a critical functionality for many photonic applications but is currently not available in PICs. Within PICaboo, an integrated polarization controller will be developed permitting the conversion of the input signal’s polarization to any output state. The controller will comprise a polarization rotator, a polarization splitter and a polarization phase shifter with excellent performance to ensure polarization conversion with minimum losses.

In parallel, III-V Lab will transfer its InP semi-insulated buried heterostructure (SIBH) platform to the O-band operating range and develop novel passive and active building blocks which will be then co-integrated in novel PICs. The SIBH technology reduces the parasitic effects and enhances the speed
capabilities of the InP PIC platform, while significantly improving the thermal behavior of the developed structures. III–V Lab will (a) scale the speed performance of its actives to 100 Gbaud: high-speed EAMs, distributed feedback (DFB) lasers with a circular mode profile and gain sections will be developed for the first time on the O-band semi-insulating buried heterostructure (SIBH) platform, (b) fabricate critical low-loss passive structures: high-transparency waveguides, multi-mode-interference optical couplers/splitters with negligible optical loss and ultra-compact optical ring filters will be developed, (c) introduce SAG technology to its InP SIBH platform towards large scale cointegration of actives and passives building blocks, yielding the first InP generic O-band band PIC platform in Europe and (d) leverage all-optical signal processing on chip that will compensate for bandwidth limitations and transmission impairments on high-speed applications.

2.2. Coherent receiver PIC with all-optical DSP functions for low-cost metro and DCI applications

Discussions among industry suggest that coherent technologies are expected to penetrate the datacenter environment even at short distances [11]. While PAM4 IMDD comprises a cost-efficient solution compared to coherent technologies which employ high power DSPs and costly low linewidth lasers, it requires optical dispersion compensation and additional optical amplification increasing the power consumption and the overall cost. The 400 ZR implementation agreement [12] defines the use of coherent technologies with low-power DSPs for distances up to 80–120 km. PICaboo will fabricate a coherent optical receiver capable of reducing the power consumption of coherent DSP systems and the overall receiver cost. The use of the novel integrated polarization phase shifter and polarization controller sub-circuits will enable migration of complex signal processing functions typically performed at the digital domain to the optical domain. Nearly all of this signal processing relies on a binary representation of the sampled received signal. However, most of this signal processing, like separating the signals of the two orthogonal polarizations and tracking the frequency and phase of the signal with respect to the local oscillator, concern the signal in its optical state. In PICaboo, these signal processing steps will be performed in the optical domain introducing novel functionalities at the photonic receiver chip.

Two coherent receiver PIC demonstrators will be developed, a single and a dual polarization coherent receiver with phase and polarization control operating at 100 Gb s\(^{-1}\) and 400 Gb s\(^{-1}\), respectively, that target to satisfy the requirements for 80–120 km metro/DCI use cases and to offer a competitive alternative for short DCI links within the 10–40 km range. The simplified block diagram of the single polarization coherent receiver that will be developed within PICaboo, is depicted in figure 2. The state of polarization of the received signal is rotated to stably match the polarization of the local oscillator. This requires a phase shifter capable of introducing a phase difference between the two orthogonal polarizations, followed by a rotation of the resulting polarization. Since the polarization changes stochastically over time during the propagation of the signal in the fiber, the phase difference will be dynamically controlled by the novel endless phase shifter that will be developed. This structure can continuously change the phase of the optical signal without the need for any reset operation [13]. Maintaining a fixed output polarization of this stage, the power variations due to the polarization effects in the transmission fiber are eliminated.

Moreover, to be able to separate the orthogonal phases (or quadratures) of the received signal, a constant phase relation between the local oscillator and the data signal must be maintained. This requires a frequency and phase control of the local oscillator laser, to match the respective characteristics of the data signal laser.
Figure 2. The PiCaboo single polarization coherent receiver with phase and polarization control.

Figure 3. The PiCaboo EAM-IQM with all optical pre-equalization on-chip.

The continuous phase control is based on feedback from the output ports of the optical hybrid, where the beating between the local oscillator and the signal can be observed. The coherent receiver ensures that the data signal is recovered with simplified PAM4 DSP implementations, which are also employed in IMDD schemes, yielding an overall cost reduction of the coherent receiver device. The PICs will be assembled on appropriate interposers for feeding the RF and DC signals. The receiver modules will be based on an appropriately designed package or in the form of evaluation boards. Commercially available trans-impedance amplifiers will be used, with analog bandwidth of 35 GHz.

2.3. EAM-based MachZehnder modulator transmitter PIC with all-optical signal equalization for current and future PON applications

To close the gap between 10 Gbit s\(^{-1}\) XGS-PON and future 50 G-PON implementations, the 25 GS-PON specification has been defined [14] which constitutes a cost-effective solution based on IMDD schemes, that can also meet the needs of the mobile 5G era and large-scale enterprises, where symmetrical connections become increasingly important. The path towards 50/100 Gb s\(^{-1}\) and beyond PON systems can follow two directions, either by increasing the line rate per wavelength, or by increasing the overall system capacity by means of channel bonding. PiCaboo leverages both trends by developing a single transmitter PIC technology that scales the line rate per wavelength to 100 Gb s\(^{-1}\) and 200 Gb s\(^{-1}\) and at the same time adding more wavelengths exploiting also novel all-optical processing functionalities.

In more detail, two generations of electro-absorption modulators (EAMs) will be developed, targeting 50 Gbaud and 100 Gbaud operation respectively, employed in a MachZehnder interferometer (MZI) configuration to achieve better signal quality performance through higher dynamic extinction ratio. The differentially-driven EAM-based MZ modulator will exhibit higher transmission tolerance to chromatic dispersion owing to the chirp cancelation between the two MZI arms enabling the achievement of low dispersion penalty. The PiCaboo EAM-MZI transmitters, comprising also the developed DFBs, gain sections and passive elements, will enable the downstream operation over the required PON reach of up to 40 km or even beyond using standard DSP. Despite the fact that the MZI-based layout will occupy larger chip area compared to a typical single EML transmitter, it consumes a much smaller chip area compared to traditional MZMs relying on the electro-optic effect which are based on a long travelling wave electrode design in order to achieve high speed operation. The chip area is of high importance especially for PON applications because the optical module size should be as small as possible to enable a large port-density at the optical line terminal -side. Moreover, a coherent based IQ transmitter prototype (figure 3) and an array of four coherent IQ EAM-MZIs will be fabricated on a single chip exploiting the developed passive and active components and exploiting a different design, scaling the overall transmitter capacity to 400 Gb s\(^{-1}\) and 1.6 Tb s\(^{-1}\) respectively. In PONs, optical signal processing can be used at the transmitter to apply pre-emphasis to the signal. The Tx-side circuit will leverage all-optical signal equalization functionality by developing a tapped delay line signal processing circuit that will be monolithically cointegrated with the EAM-IQM transmitters aiming operation at 100 Gbaud and allowing for: (a) pre-compensation of signal impairments and (b) mitigation of bandwidth limitations at the optical network unit receiver offloading DSP requirements and unleashing the vast potential of PIC technology. The output of the tapped-delay-line optical-predistortion circuit comprises a weighted sum of delayed copies of the input signal using the critical building blocks that will be developed on the SAG-SIBH platform of III–V Lab. The abovementioned
PICs will be assembled on a suitable high-speed interposer carrying 67 GHz RF lines based on a flip chip bonding process and a DC interposer will also be used to supply the necessary currents/voltages to the integrated Mach-Zehnder phase shifters, the DFBs and the EAMs. Compatible high speed InP-HBT drivers which will be provided externally will be co-packaged with the transmitter PICs close to each other on appropriate evaluation boards to achieve the best performance possible.

3. Impact

PICaboo is fully aligned with the vision of the generic foundry model and targets to develop PDK-compatible libraries including the compact models of all building blocks which will be developed within the project. Since these libraries will be readily integratable into the generic PDK of TUe and III–V Lab after the project end, will enhance the platforms’ capabilities offered to end users and maximize the exploitation potential of the developed building blocks. Designing PICs by making use of the building blocks in the PDK libraries will reduce design and test time by an estimated 30% and reduce the cycle count of iterations by at least one full round, due to the availability of the already validated building blocks, paving the way for fast prototyping. Moreover, PICaboo technologies will tackle a wide range of application areas bringing significant benefits in terms of performance, cost and energy consumption.

The coherent receiver PICs make a perfect fit for near-term exploitation in 100 Gb s$^{-1}$ systems based on 28 G DP-QPSK and 200 Gb s$^{-1}$ systems based on 28 G DP-16QAM or 50 Gbaud DP-QPSK. Considering that sales of 400 GbE transceivers are gaining momentum, PICaboo coherent receiver will comprise an attractive technology based on 50 Gbaud DP-16QAM with long term exploitation potential. The dual polarization coherent receiver PIC demonstrator will reduce the overall transceiver power consumption by more than 30% with concurrent cost benefits of 3,600× compared to standard coherent transceivers. PICaboo EAM-based transmitters are aligned with industry trends for upgrading PON capacity: (a) high speed single channel and (b) channel bonding via wavelength multiplexing. The single EAM-MZM transmitter targets the 25 G/50 G-PON and 100G-PON markets employing NRZ and PAM4 modulation on a single channel. The EAM-IQM transmitter targets up to 400 Gb s$^{-1}$ capacity exploiting single channel and coherent 16QAM modulation, and the four-array EAM-IQM can offer up to 1.6 T comprising a future-proof and scalable solution for emerging 6G fronthaul applications. The single EAM-MZM transmitter and the coherent EAM-IQM transmitter PICs will leverage power consumption reduction of 50% and 65% respectively, compared to 50G EML-based solutions and will both demonstrate an overall cost reduction by almost 20%. Although a standard form factor or a Co-Packaged Optics approach are not considered within PICaboo, the developed PIC demonstrators will be assembled and packaged appropriately to enable system-level evaluation and exhibit the expected performance.

4. Conclusions

The PICaboo project has a twofold ambitious mission: (a) to develop novel building blocks, sub-circuits and PICs that will address a wide range of application areas and markets and (b) to reduce the overall research and development costs of advanced PICs aligning with the vision of the generic foundry model. This concept paper outlines the approach that PICaboo adopts to tackle these challenges.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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ORCID iDs

Giannis Kanakis https://orcid.org/0000-0003-0364-4090
Maria Spyropoulou https://orcid.org/0000-0002-4851-791X

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