Robust formation of quantum dots in GaAs/AlGaAs heterostructures for single-electron metrology

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Abstract
The robust and reproducible formation of a quantum dot is key for the development of tunable barrier single-electron pumps as a future quantum current standard. We investigate the fabrication process and perform electrical characterizations at cryogenic temperatures of quantum dots realized in a GaAs/AlGaAs heterostructure with lateral potential confinement by a combination of a shallow-etch technique and metallic top-gates. Stable geometric parameters of the lithography (5% deviation) in combination with a homogeneous heterostructure resulted in the robust and reproducible quantum dot formation for 37 out of 39 tested devices.

Keywords: quantized current source, single-electron pumps, GaAs/AlGaAs heterostructure based quantum dots, robustness of Coulomb blockade

(Some figures may appear in colour only in the online journal)

1. Introduction
Non-adiabatic single-electron pumps capture and transmit single electrons in a dynamic quantum dot (QD) formed each frequency period by modulating one of the tunnel barriers connecting the QD to the leads [1]. Recently, such devices realized in GaAs/AlGaAs heterostructures reached a current quantization better than 1 ppm, establishing these pumps as promising candidates for a direct realization of the new definition of the SI unit ampere [2–5]. The probability for capturing electrons while the QD is being isolated from the electronic environment essentially determines the achievable accuracy and can be described as a cascade of back-tunneling events [6]. The empirical figure-of-merit for a prediction of current quantization, \( \delta_2 = \ln \Gamma_1 \frac{E_c}{\Delta_{ptb}} \), depends on the tunnel barrier dynamics and charging energy (represented by decay rates \( \Gamma_n \), QD level shift \( \Delta_{ptb} \) during the capture process and the charging energy \( E_c \)) [7]. While the properties of the dynamic QD during pumping operation are inaccessible to dc transport measurements, the basic QD formation can be tested by Coulomb blockade measurements. Empirically, we find for the typical range of parameters of this device type the observation of Coulomb blockade to be linked to the generation of quantized currents in the dynamically driven system, indicating that a stable formation of Coulomb blockade is a necessary but not a sufficient condition for realizing a single-electron pump. The robust formation of quantum dots with a reproducible charging energy and tunnel barriers is therefore key for any metrological application, especially for a possible device parallelization in order to achieve larger currents in the nA range.

Quantum dots serve as basic building blocks for a variety of nanoscale devices, for example as spin qubits [8, 9]. Surprisingly, there are only very few studies targeting device yield of mesoscopic devices in GaAs/AlGaAs heterostructures. The manual fabrication of prototype devices and the measurements at cryogenic temperatures make these device characterizations time-consuming and challenging. Therefore most studies of device characteristics are based on very few
or even only on single samples. One of the simplest structures showing quantum coherence phenomena is the split-gate transistor. Yang et al [10] studied over 500 quantum point contacts (QPC) and found a surprisingly low yield, citing local fluctuations of the 2DEG potential and the QPCs large sensitivity to those as probable reasons in addition to the limited fabrication yield. To overcome the testing limitations induced by the cryogenic measurement environment, Al-Taie et al [11, 12] developed an on-chip multiplexer to test 256 split-gate devices in one cooldown, resulting in a device yield of about 55%. More complex devices, such as surface-gate defined quantum dots in the few electron regime investigated for Coulomb blockade, showed a yield of less than 50% [13].

In contrast to a purely gate defined QPC or QD, the lateral, electrostatic confinement of the electrons in our device is achieved by a combination of mesa structuring with a shallow-etch technique and two metallic top-gates (see figure 1(b)). The shallow-etch technique implies that only the upper n-doped AlGaAs layer and not the undoped AlGaAs spacer layer is removed by the chemical wet etch (see figure 1(a)) [14]. The main advantage of this approach is the reduction of sidewall depletion and electron transport disturbances by local impurities, because the electron channel is not directly bounded by an etched surface. The tunable barriers are realized by two Schottky-barrier type metal gates on top of the channel. This method of confinement for a QD was first shown by Nagamune et al and promises quantum dots of a very small size [15].

The robust and reproducible formation of a QD is essentially dependent on geometric deviations and the overall yield of lithography, therefore a systematic investigation of the manual fabrication process is presented in the first part of this report. Second, basic electrical properties at low temperatures, such as resistance and gate control of the conducting channel, are investigated in order to identify faulty devices and to verify a reproducible confining potential. Coulomb blockade measurements and the evaluation of charging energy and capacitive gate coupling were conducted to test for a successful QD formation and will be presented in the last part of the report.

2. Sample fabrication

Devices were fabricated on 2” MBE grown wafers consisting of an n-type modulation doped GaAs/AlGaAs heterostructure with a two-dimensional electron gas (2DEG) at a measured depth of 82 nm and a typical electron density in the range of $n_e = 2.6 \times 10^{11}$ cm$^{-2}$ and $\mu_e = 1 \times 10^6$ cm$^2$ V$^{-1}$ s$^{-1}$. The pumps were aligned parallel to the main flat ([011] crystal direction in EJ notation), unless stated otherwise.

After a careful pre-lithographic surface treatment with a diluted NH$_4$OH solution, the mesa structure was patterned by e-beam lithography in a negative tone resist system. In contrast to the dry-etching process technology, chemical wet etching has the ability to cause nearly no surface damage that can degrade electronic properties, but is on the other hand a challenging task in terms of process control and reproducibility (e.g. etch rates and mask undercut) [16]. In order to achieve good process control of various etch depths between 20 nm and 90 nm, an etching speed of 0.5 nm s$^{-1}$–1 nm s$^{-1}$ was chosen. A highly diluted phosphoric based etch (volume ratios: H$_3$PO$_4$:H$_2$O$_2$:H$_2$O (1:4:495)), with an etch rate of 0.52 nm s$^{-1}$–0.58 nm s$^{-1}$ yields a nearly isotropic etch profile [17]. Due to the manual composition of the etching solutions, the etching has to be calibrated with a test sample.

The two key factors for shallow-etch defined channels are the minimal etching depth ($z$) to establish a confining potential and the resulting sidewall depletion inside these channels, limiting the minimal lithographic channel width ($w$) in dependency of channel length ($l$). A series of test samples revealed a minimum etching depth of about 30 nm for a successful confinement. Taking into account that slight deviations in the manually handled wet-etching process can occur, a value of 38 nm–42 nm for etching depth was chosen for all devices. The channel length was set to a minimum value of 600 nm,
limited by the geometry of the top-gates and a small offset compensating slight alignment errors between the different lithographic steps of mesa structure and top-gates. Several different channel widths were tested at cryogenic temperatures, resulting in a minimal width of about 350 nm for the chosen channel length of 600 nm. To compensate fluctuations in electron density and other slight deviations of the fabrication process, a target value of 450 nm–470 nm was chosen for all devices.

The ohmic contacts (Ni/Ge/Au/Ni/Au) and gate structures (7 nm Cr and 28 nm Au) were fabricated by a metal lift-off process with a PMMA system as lithography mask. In order to validate the channel conductance (range of some kΩ) in a two terminal setup, a stable and low resistance ohmic contact is necessary. The contact resistance was evaluated by testing transmission line structures at 1.5 K, revealing a stable value of 19 Ω ± 0.6 Ω (standard deviation for n = 10 samples) with a reproducible linear current–voltage characteristic.

3. Characterization of the fabrication process in terms of reliability and reproducibility

The geometry of the confinement potential, the surface quality of the etched structures and the stability of the 2DEG parameters all determine the electron transport characteristic of the QD. In order to distinguish between variations induced by the fabrication process and intrinsic fluctuations (e.g. disorder potential), a careful investigation of these parameters was conducted to estimate the variation within one produced wafer to ensure the reproducibility of the fabrication process.

The wafer quality and homogeneity was tested by quantum Hall measurements over a sample batch of 7 wafers, which had been grown in the MBE in direct sequence without interruptions. At a temperature of 1.5 K, these measurements showed an electron density of $n_e = 2.64 \times 10^{11} \text{cm}^{-2} \pm 2.4\%$ and a mobility of $\mu_e = 1.04 \times 10^6 \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \pm 5.3\%$ ($n = 4$ samples, Hall bar parallel to main flat, $[0 \bar{1} 1]$ crystal direction), and $0.91 \times 10^6 \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \pm 7.1\%$ ($n = 3$, Hall bar perpendicular to main flat, $[0 1 1]$ crystal direction), respectively. To study possible effects of an inhomogeneous modulation doping, two quarter pieces of one 2" wafer were fabricated with Hall bar structures evenly distributed from center to the outer circumference, with a safety distance of 2 mm to the outer border. The electron density showed a nearly stable value of $n_e = 2.64 \times 10^{11} \text{cm}^{-2} \pm 1.6\%$ ($n = 12$) and only a slightly larger deviation for the mobility $\mu_e = 0.89 \times 10^6 \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \pm 4.4\%$ ($n = 7$, Hall-bar perpendicular to main flat) and $1 \times 10^6 \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \pm 1.5\%$ ($n = 5$, Hall-bar parallel to main flat), respectively.

The etch depth strongly influences the charge carrier density and sidewall depletion in the channels. Despite a stable overall etch depth from wafer to wafer, the uniformity on a single wafer is also important for a reproducible device fabrication. Over a whole quarter wafer piece the etch depth at mesa steps horizontal and perpendicular to the main wafer flat showed a standard deviation of less than ± 1.5 nm ($n = 14$), nearly independent of the crystal axis, all verified in atomic force microscopy (AFM) measurements with an estimated statistical error of ± 1 nm. For different production runs a reproducibility of ± 2 nm ($n = 5$) of the desired etch depth was achieved. Due to careful pre- and post-etch treatment with a diluted NH$_4$OH solution, the areal surface roughness ($S_q = \text{root mean square height, ISO 25178}$) showed only minor fluctuations on a low base level ($S_q = 0.56 \text{ nm} \pm 0.12 \text{ nm}$ measured on 5 different positions on one wafer piece). It was possible to closely reproduce these values over 5 different production batches ($S_q = 0.5 \text{ nm} \pm 0.13 \text{ nm}$). A typical AFM image for an etch depth and surface roughness measurement can be seen in figure 2. Samples with improper surface treatment (e.g. $S_q = 1.8 \text{ nm}$) fabricated outside the scope of this study showed strong random telegraph noise and were unsuitable for single-electron transport measurements.
An inspection performed by scanning electron microscopy (SEM) showed an overall yield of 95% for the lift-off process and mesa etch. The geometry of the confinement potential is essential for the reproducibility of the QD formation, therefore special attention was paid on the reproducibility of channel width and gate geometry. Every device used for the electrical characterization in section 4 was therefore inspected afterwards individually by SEM, resulting in a channel width of 469 nm ± 8 nm (n = 30). The gate distances showed a maximum deviation of ±5 nm (n = 30) to their designed target values in the range from 115 nm up to 300 nm. The gate width was determined to 81 nm ± 4 nm (n = 60). The systematic error for SEM distance measurement using cross sections was estimated to ±5 nm for mesa structures and ±2 nm for metallic structures.

The evaluated geometry variance is therefore sufficiently small in order to test for the reproducibility of the confinement potential in the following electrical characterizations.

4. Electrical characterization

While potential basic device faults are identified by probing the channel conductivity at room temperature (here zero devices), the investigation of the static QD properties required cryogenic temperatures. Dc characterization techniques provided information about the confining potential induced by the shallow-etched channel and the two top-gates. Transport spectroscopy measurements of Coulomb blockade were used to determine the charging energy of the QD and the capacitive coupling of the gates to the QD. These measurements also revealed information about the geometric position of the QD between the gates and the potential existence of a double QD, possibly induced by a charge trap which can strongly influence single-electron pumping performance.

The cooldown speed has been proven to be crucial for reproducibility. A high cooldown speed can cause an uncontrolled formation of the mesa confined 2DEG, resulting in a high conductance or non-conducting channels. The cooldown speed was therefore closely monitored for each of the samples and especially adjusted in the region between 150 K–50 K to values of no more than 2 K min⁻¹. Applying positive voltages to the gates during cooldown is a common method to suppress random telegraph noise, however to ensure a comparable electrical characterization, all samples were grounded during cooldown [18].

To identify damaged or defect samples that can falsify the data evaluation, SEM images were taken after every cooldown for each sample to check for possible deviations in the geometry and for electrostatic discharge damage (ESD) of the metallic gate structures. Devices destroyed by ESD which show no gating effect, are excluded from the data analysis (in total 12 devices). Two cases, where the electrical characterization indicates internal damage are discussed in the final section, leaving in total 30 devices of batch (A) for the dc characterization in the following section.

4.1. Dc characterization at cryogenic temperatures

The spatial, macroscopic homogeneity of charge carrier density across the whole wafer was probed by a two-point differential conductance measurement of the mesa structured channels. The calculated mean value for the resistance of 30 devices is $R = 4.1 \, \text{k}\Omega \pm 0.6 \, \text{k}\Omega$ at $T = 300 \, \text{mK}$ (see figure 3(a)). The narrow constriction of the 2DEG due to the shallow-etch dominates the conductance, with the 2DEG and ohmic contacts typically being in the order of 100 $\Omega$–200 $\Omega$. The relative homogeneity of the resistance indicates also a stable sidewall depletion.

Figure 3. (a) Histogram of channel resistances with a bin size of 0.25 kΩ. (b) Histogram of gate pinch-off voltages with a bin size of 5 mV, indicating a symmetric but not unimodal distribution around the mean value of $-154.7 \, \text{mV}$. 

The electrostatic potential of the channels can be locally modified by the top-gates in a typical transistor gate configuration. The sample design also included a varying gate distance $d$ between 115 nm up to 300 nm to check for the influence of the gate design onto QD capacitance. The pinch-off voltages were measured to a mean value of $V_p = -154.7 \, \text{mV} \pm 23.2 \, \text{mV}$ (n = 60), showing 15% standard deviation of the mean (see figure 3(b)).
\( \Delta V_{g1} = \frac{\Delta V_{g2}}{\Delta V_{g1}} = 2.1 \) indicates a very symmetric position of the QD between the gates. No additional resonances deployed by a second QD are observed. (b) Conductance measurement of the same device under variation of bias voltage and gate 1. The dotted lines indicate the shape of the Coulomb diamond used for evaluation of charging energy and gate lever-arms.

Despite the small spread of the geometric channel confinement in our devices, a typical deviation of 15% in channel resistance and subsequently an almost identical deviation in gate pinch-off can be observed, very comparable to values reported in literature. A significant improvement of this deviation was only achieved by testing all devices in a single cooldown.

4.2. Transport properties in the Coulomb blockade regime

To obtain information about the relative capacitive coupling strength of the gates, \( m = \Delta V_{g1}/\Delta V_{g2} \), and the location of the QD between the two gates, a charge stability diagram was measured for each device, showing the current through the QD under low bias voltage (100 µV) as a function of both gates (see figure 4(a)). For 30 devices the relative gate coupling was evaluated to a mean value of \( m = 1 \pm 0.07 \), indicating a very symmetric capacitive coupling. A statistical error due to the manual fitting process was estimated to a value of \( \pm 0.02 \). There were no evident signs of a double QD in any device.

The main energy scale to describe electronic transport through a weakly coupled QD in the constant-interaction model (CI) is the charging energy \( E_c = e^2/C_{QD} \), directly related to the overall capacitance of the QD \( C_{QD} \). The capacitive coupling of a particular gate onto the electrochemical potential of the QD is defined by a proportional factor \( \alpha = C_g/C_{QD} \) (lever-arm). These parameters are obtained from conductance measurements under variation of bias voltage and plunger gate by the evaluation of the Coulomb diamond shape. For these measurements, the devices were all tuned to a similar current range and equivalent barrier transparency for a constant coupling strength and therefore enabling comparable measurements between individual devices.

All devices showed a clear diamond-shape like pattern, resulting in charging energies \( E_c \) ranging from 0.98 meV up to 1.75 meV depending on gate distance (see figure 4(b)). A systematic error of \( \pm 0.05 \) meV was estimated for manual fitting errors. Seven devices with a similar gate distance of \( d = 116.2 \) nm \( \pm 3 \) nm showed a mean value for the charging energy of \( E_c = 1.61 \) meV \( \pm 0.13 \) meV. A direct comparison with other published results is difficult and nearly impossible due to a very wide parameter space, for example fabrication technology, device design and 2DEG properties, even if often reported values for QDs in comparable GaAs/AlGaAs heterostructures are typically in a similar range between 0.5 meV and 3 meV [15]. The observed dependency between gate distance and charging energy (see figure 5) indicates how a lower areal spacing results in a reduced capacitance and higher charging energy, even if the exact physical parameter dependency between electronic environment and QD...
capacitance in relation to gate distance is not trivial. It should be noted, that a stable Coulomb blockade was observed for all gate distances down to the design dependent limit of 115 nm. Four tested devices with a gate distance of 105 nm ± 3 nm, fabricated in a second production run on the same wafer material (not part of batch A), showed a non-symmetric Coulomb blockade locating the QD beneath one of the gates. Therefore, a gate width of 115 nm is estimated to be the lower limit for our confinement geometry on wafers with the previously mentioned 2DEG properties.

Another point of interest is the evaluation of the capacitive coupling of the gates onto the QD. The lever-arms for the gates can be evaluated to an overall mean value of $\alpha = 0.23 \pm 0.02$ ($n = 60$). A statistical error due to the manual fitting process was estimated to a value of ±0.01. A correlation between lever-arms and gate distance was not observed. The values of the gate lever-arms indicate a very reproducible and symmetric coupling to the electrochemical potential of the QD, being a necessary pre-requisite for a reliable operation as a single-electron pump with tunable barriers.

As previously mentioned in section 4, two devices showed remarkable deviations in pinch-off voltages and relative gate coupling (e.g. $m = 0.2$ and $m = 1.51$) in contrast to the typical expected values. It should be noted, that these devices were also able to form a QD, resulting in unexceptional values for the charging energy and drawing the conclusion that the full set of device characterization measurements is necessary to clearly identify faulty devices.

All these results were also validated by additional measurements on 7 devices with the same design approach, fabricated in a second batch (B) on another wafer with nearly the same properties for electron density and mobility. For a gate distance of 150 nm, a mean value of $E_c = 1.69$ meV ± 0.15 meV ($n = 4$) was evaluated for the charging energy, the larger gate distance of 250 nm resulted in a lower charging energy of $E_c = 1.16$ meV ± 0.07 meV ($n = 3$), as expected.

The relative gate coupling was also nearly constant, showing a mean value of $m = 0.99 \pm 0.07$ ($n = 7$), again indicating a very symmetric position of the QD without another second QD. The lever-arms were evaluated to a mean value of $\alpha = 0.22 \pm 0.02$ ($n = 14$), in good agreement with our previous results.

5. Conclusion

In comparison to devices realized in GaAs/AlGaAs heterostructures, an alternative and widely regarded approach for quantized charge pumping are silicon based devices. One main advantage is the existence of a highly developed fabrication technology promising reproducible device characteristics [22–24]. But so far, there are no known studies of reproducibility for such silicon based devices, but especially

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**Figure 5.** Left axis: charging energy $E_c$ as function of gate distance $d$ with error bars for manual fitting routine. Right axis: level-arms $\alpha$ as a function of gate distance $d$, the error bars are not visible due to small values.

**Table 1.** Key parameters and results for two batches.

|                  | Batch (A)        | Batch (B)        |
|------------------|------------------|------------------|
| Electron density | $2.68 \times 10^{11}$ cm$^{-2}$ | $2.68 \times 10^{11}$ cm$^{-2}$ |
| Mobility $\mu_e$ | $1.1 \times 10^{6}$ cm$^2$ V$^{-1}$ s$^{-1}$ | $0.99 \times 10^{6}$ cm$^2$ V$^{-1}$ s$^{-1}$ |
| Fabricated      | 208              | 208              |
| devices          |                  |                  |
| Gate distances   | 115 nm ... 300 nm | 150 nm; 250 nm   |
| Tested devices   | 44               | 7                |
| Damaged ESD      | 12 (+2)          | 0                |
| Functional       | 30               | 7                |
| Charging         | 0.98 meV ... 1.75 meV | 1.11 meV ... 1.85 meV |
| energy $E_c$     |                  |                  |
| Relative gate    | $1 \pm 0.07$     | $0.99 \pm 0.07$  |
| coupling $m$     |                  |                  |
| Gate lever-arm $\alpha$ | $0.23 \pm 0.02$ | $0.22 \pm 0.02$ |
the formation of single-traps will be a challenging task for a reliable production. 

In this report, we have demonstrated the ability to fabricate lateral QD devices based on GaAs/AlGaAs heterostructures in a narrow range of geometric parameters with only minor deviations in the range below 5% to their mean values. In combination with a reproducible and homogeneous heterostructure, the basic electrical properties showed a standard deviation of about 15% for the conductance and gate pinch-off at cryogenic temperatures. The characterization of the static QD properties showed a smaller maximum deviation in charging energy of 8% for a fixed gate distance and 9.7% for all lever-arms independent from gate distance. Measurements of identically designed samples on a second wafer fabricated in a different batch demonstrated the reliability and reproducibility of our fabrication process (see table 1).

In total 37 out of 39 and therefore the significant majority of devices showed reproducible QD formation within small tolerances. Even if the overall yield may not be an appropriate and easy to define term for a manual fabrication process and single device testing, the Coulomb blockade realized in GaAs/AlGaAs heterostructures devices is sufficiently robust and underlines the suitability of this material system for mesoscopic devices in metrology.

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References

[1] Kaestner B and Kashcheyevs V 2015 Non-adiabatic quantized charge pumping with tunable-barrier quantum dots: a review of current progress Rep. Prog. Phys. 78 103901
[2] Giblin S P, Kataoka M, Fletcher J D, See P, Janssen T J B M, Griffiths J P, Jones G A C, Farrer I and Ritchie D A 2012 Towards a quantum representation of the amperes using single electron pumps Nat. Commun. 3 930
[3] Stein F et al 2015 Validation of a quantized-current source with 0.2 ppm uncertainty Appl. Phys. Lett. 107 103501
[4] Bae M-H, Ahn Y-H, Seo M, Chung Y, Fletcher J D, Giblin S P, Kataoka M and Kim N 2015 Precision measurement of a potential-profile tunable single-electron pump Metrologia 52 195–200
[5] Stein F et al 2017 Robustness of single-electron pumps at sub-ppm current accuracy level Metrologia 54 S1–8
[6] Kashcheyevs V and Kaestner B 2010 Universal decay cascade model for dynamic quantum dot initialization Phys. Rev. Lett. 104 186805
[7] Kashcheyevs V and Timoshenko J 2014 Modeling of a tunable-barrier non-adiabatic electron pump beyond the decay cascade model 29th Conf. on Precision Electromagnetic Measurements (IEEE) pp 536–7
[8] Loss D and DiVincenzo D P 1998 Quantum computation with quantum dots Phys. Rev. A 57 120–6
[9] Hanson R, Kouwenhoven L P, Petru J R, Tarucha S and Vandersypen L M K 2007 Spins in few-electron quantum dots Rev. Mod. Phys. A 79 1217–65
[10] Yang Q-Z, Kelly M J, Farrer I, Beere H E and Jones G A C 2009 The potential of split-gate transistors as one-dimensional electron waveguides revealed through the testing and analysis of yield and reproducibility Appl. Phys. Lett. 94 033502
[11] Al-Taie H, Smith L W, Xu B, See P, Griffiths J P, Beere H E, Jones G A C, Ritchie D A, Kelly M J and Smith C G 2013 Cryogenic on-chip multiplexer for the study of quantum transport in 256 split-gate devices Appl. Phys. Lett. 102 243102
[12] Al-Taie H, Smith L W, Lesage A A J, Griffiths J P, Beere H E, Jones G A C, Ritchie D A, Kelly M J and Smith C G 2015 Spatial mapping and statistical reproducibility of an array of 256 one-dimensional quantum wires J. Appl. Phys. 118 035703
[13] Yang Q-Z, Jones G A C, Kelly M J, Beere H and Farrer I 2008 Fabrication and characterization of GaAs/AlGaAs lateral quantum dot developed by ultrasonic agitation Semicond. Sci. Technol. 23 055018
[14] van Houten H, van Wees B J, Heijman M G J and André J P 1986 Submicron conducting channels defined by shallow mesa etch in GaAsAlGaAs heterojunctions Appl. Phys. Lett. 49 1781–3
[15] Nagamune Y, Sakaki H, Kouwenhoven L P, Mur L C, Harmans C J P M, Motohisa J and Noge H 1994 Single electron transport and current quantization in a novel quantum dot structure Appl. Phys. Lett. 64 2379–81
[16] Baca A G and Ashby C I 2005 Fabrication of GaAs Devices (London: The Institution of Electrical Engineers) p 117
[17] Mori Y and Watanabe N 1978 A new etching solution system, H₃PO₄−H₂O−H₂O, for GaAs and its Kinetics J. Electrochem. Soc. 125 1510–4
[18] Pioro-Ladrière M, Davies J H, Long A R, Sachrajda A D, Gaudreau L, Zawadzki P, Lapointe J, Gupta J, Wasilewski Z and Studenikin S 2005 Origin of switching noise in GaAs/AlGaAs lateral gated devices Phys. Rev. B 72 115331
[19] Nixon J A and Davies J H 1989 Potential fluctuations in heterostructure devices Phys. Rev. B 40 7929–32
[20] Smith L W et al 2014 Statistical study of conductance properties in one-dimensional quantum wires focusing on the 0.7 anomaly Phys. Rev. B 90 045426
[21] Kouwenhoven L P, Austing D G and Tarucha S 2001 Few-electron quantum dots Rep. Prog. Phys. 64 701–36
[22] Tettamanzi G C, Wacquez R and Rogge S 2014 Charge pumping through a single donor atom New J. Phys. 16 063036
[23] Clapera P et al 2017 Design and operation of CMOS-compatible electron pumps fabricated with optical lithography IEEE Electron Device Lett. 38 414–7
[24] Yamahata G, Giblin S P, Kataoka M, Karasawa T and Fujiwara A 2017 High-accuracy current generation in the nanoampere regime from a silicon single-trap electron pump Sci. Rep. 7 45137