The properties of bipolar junction transistors (BJTs) are known to vary in terms of their parameters. In this work, an experimental approach, including pattern recognition concepts and methods such as principal component analysis (PCA) and linear discriminant analysis (LDA), was used to experimentally investigate the variation among BJTs belonging to integrated circuits known as transistor arrays. It was shown that a good deal of the devices variance can be captured using only two PCA axes. It was also verified that, though substantially small variation of parameters is observed for BJT from the same array, larger variation arises between BJTs from distinct arrays, suggesting the consideration of device characteristics in more critical analog designs. As a consequence of its supervised nature, LDA was able to provide a substantial separation of the BJT into clusters, corresponding to each transistor array. In addition, the LDA mapping into two dimensions revealed a clear relationship between the considered measurements. Interestingly, a specific mapping suggested by the PCA, involving the total harmonic distortion variation expressed in terms of the average voltage gain, yielded an even better separation between the transistor array clusters.

I. INTRODUCTION

Bipolar transistors are at the root of modern electronics, but the variability of their parameters remains an important phenomenon with important theoretical and practical implications. Perhaps as a consequence of the adoption of negative feedback in promoting circuit invariance to transistor parameters, the variability of transistor behavior has received relatively little attention in the literature more recently. There have been several works addressing this problem at a larger integration and processing scales (e.g. [1]), typically considering digital applications, but relatively fewer works have addressed discrete device variance in analog electronics. Yet, a better understanding of transistor variability at the individual level remains an important issue because it can help, in a number of ways, the design of better electronic circuits (e.g. [2]). Ultimately, all large scale integration systems are composed by a massive number of individual transistors. For instance, the knowledge of the current gain of an individual (or a lot of) BJT provides valuable subsidies for deciding how much gain can be sacrificed to negative feedback in exchange for circuit improvements. In addition, recent findings [3] suggest that the latter technique may have limited effects in ensuring transistor parameter invariance, motivating further related research, as well as design procedures that take into account the specific characteristic curves and parameters of each individual device.

Interestingly, though important issues such as transistor parameter dependency have been addressed in semiconductor physics, it usually does not go to the level of probing industrialized devices, so there is substantial space for research aiming at bridging this gap. Fortunately, many advances in instrumentation [4], signal analysis techniques [5, 6], powerful multivariate statistical [7, 8] and pattern recognition [9, 10] methods have paved the way to devising experimental approaches that can contribute to our understanding of industrialized transistor variability. In a recent study [3], we showed that discrete BJTs variance is relatively constrained within each transistor type, but much larger among different types of transistors. These differentiating variabilities are such that well-defined clusters of transistors could be identified, each of such clusters corresponding to respective transistor types. However, the intra-cluster variance resulted markedly distinct for different types, resulting in clusters of different sizes and shapes. One of the important consequence of such findings, at least for the considered devices and configurations, is that transistor variability is not as large as to prevent statistical methods to be applied to characterize specific types. It was also shown that the variability of BJTs is mostly a two-dimensional phenomenon, in the sense that two linear combinations of traditional transistor characteristics was found to be enough to account for 88% of the variability of the considered BJTs. Despite such interesting findings, an important question remained unanswered mainly concerning the possible causes of BJT variability. More specifically, it would be interesting to investigate to what an extent such a variance depends on transistors sharing or not the same substrate. After all, devices sharing the same substrate have been exposed to almost identical fabrication conditions.

Here, we resort to pattern recognition concepts and methods, including principal component analysis (PCA) and linear discriminant analysis (LDA), to investigate transistor arrays, namely integrated circuits containing several BJTs in a common substrate, therefore providing an interesting laboratory to study transistor variability. Such types of ICs were produced during the 80’s and 90’s for several applications, such as buffering, driving, power control, audio, among other possibilities. One of the advantages of such arrays, as indicated in the respective datasheets, would be more controlled device characteristics as a consequence of the common substrate and fabrication conditions shared by the devices. However, to our knowledge, few (or no) systematic experimental data is available in the literature regarding the characteristics of
transistor arrays.

So, transistor arrays constitute an interesting resource to complement our previous investigations of transistor variability. More specifically, here we experimentally obtain characteristic curves for 6 devices in 50 transistor arrays, totaling 300 BJTs. Voltage and current gains, as well as Total Harmonic Distortion (THD) measurements were obtained respectively to a modified common emitter class A configuration. Several features of each transistor were then numerically estimated, and several modern pattern recognition concepts and methods — including PCA and LDA — were used to investigate clustering and variability of individual transistors. Several interesting results are reported. First, we have that, as expected, the parameter variability among transistors in a same array is much smaller (by an approximate factor of 20 with respect to current gain) compared to the overall variability among transistors from all arrays. The overall distribution of parameters was analyzed using PCA and subsequent density estimation, and found to be possibly distributed between two main peaks, suggesting the existence of two prototypes, at least for the considered BJT samples and conditions. The variation among the arrays was found not to be negligible, indicating that more critical analog projects involving more than one array may justify acquiring and taking into account the experimental characteristics of the used devices. Further analysis by using LDA revealed an improved segregation between the transistor arrays, as well as a clear relationship between the measurements. An even better separation between the transistor arrays was achieved by mapping the THD in terms of a combination of measurements derived from the PCA. The obtained results indicate that a good deal of transistor parameter variation may stem from different substrates, probably as a consequence of residual doping variations or other industrial processing events.

The current article is organized as follows. First, we present how the experimental data was obtained and processed in order to estimate the respective electrical features. Then, we show the results obtained by using PCA and LDA, leading to the conclusion that the BJTs in each transistor array are indeed much more similar one another than devices devices from distinct ICs.

II. MATERIALS AND METHODS

A customized stimuli generator and data acquisition was designed and implemented for the purpose of the reported experiments. It consists of a modular 16-bit microprocessor system, with separated digital and analog parts. All supplies are thoroughly decoupled. The analog inputs are sample-and-held and buffered into 4 channels, while the analog outputs are buffered by voltage followers. A precision reference source is used for DA conversion, taking place over 4 independent channels. Acquired data is buffered to ensure real-time sampling, and then transferred to SD cards. The characteristics curves are obtained by subsequent fixed $V_{cc}$ scans. A modified version of the fixed bias, class A common emitter configuration [11] (shown in Figure 1) is used for such purposes, using $R_b = 11900\Omega$ and $R_c = 67\Omega$. By modified we mean the use of the base resistor $R_b$ as a current limiter to the input signal, used fixed instead of emitter biasing.

In order to estimate the properties of the considered transistors (please refer to Figure 1), we start by organizing their characteristic curves in terms of isolines with fixed $V_{bb}$. Next, we select a representative contiguous set of isolines defined by a range in $I_c$. This is done so that the influence from the saturation region over the transistor parameters is reduced. Figure 2(a) illustrates a typical set of isolines obtained for BJT transistors. The figure also shows a possible choice for the region of interest corresponding to isolines far away from the saturation region as well as from the cutoff. The reported experiments adopted $I_{c,min} = 2mA$, $I_{c,max} = 4mA$ and $V_{cc} = 6V$.

The total current gain $\beta$, defined as $dI_c/dI_b$, can be estimated directly from the obtained isolines. The inset of Figure 2 illustrates the procedure to obtain $\beta$. For a chosen $V_{cc}$ far from the saturation region, and for given reference $V_{bb}$ isoline, we estimate $\beta(V_{bb})$ as

$$\beta(V_{bb}) \approx \frac{\Delta I_c}{\Delta I_b} \quad (1)$$

where $\Delta I_c$ and $\Delta I_b$ corresponds respectively to the changes of $I_c$ and $I_b$ between two isolines: one sequentially before and another after the reference isoline. Such a procedure yields a distribution of $\beta$ along $V_{bb}$ from which we can obtain statistics such as the average, $\mu_\beta$, and standard deviation, $\sigma_\beta$.  

![FIG. 1: The modified, fixed bias, class A common emitter configuration adopted in the reported experiments.](image)
The voltage gain $A$ is the ratio between the input voltage and the resulting output voltage, i.e., $A = dV_c/\Delta V_{bb}$. Observe that such an adopted voltage gain differs from the more commonly used $A_c$ derived from emitter biased configuration, consider the base voltage directly instead of the voltage at the incoming lead of $R_b$ in the adopted configuration shown in Figure 1. Such a property can be estimated by means of the transfer functions $V_c(V_b)$. Such transfer functions can be retrieved from the characteristic curves by taking the values of $V_b$ along a load line, which in turn are defined by $V_{cc}$ and $I_{bb}$. More specifically, $A(V_{cc})$ can be estimated as the negative of the slope of each transfer curve corresponding to values of $V_{cc}$. Figure 2(b) illustrates typical transfer functions obtained for BJTs. Minimum least squares approximation can be used to fit the transfer curves to straight lines and recover the slope. Similarly to $\beta$, we also considered a distribution of the values for the voltage gain, however in this case, by varying $V_{cc}$. Therefore, we can define the average, $\mu_A$, and standard deviation, $\sigma_A$, of the voltage gain.

Another important characteristic usually expected from transistor and respective circuits is linearity. This property can be quantified by the so-called total harmonic distortion (THD) [12]. This property is calculated as follows. A pure sinusoidal function with frequency $f$ is applied to the system. Then, the amplitudes of the fundamental ($V_f$) as well as of the harmonics generated on the output ($V_{2f}, V_{3f}, \text{etc}$) are measured. The THD can then be calculated as:

$$THD(f) = \frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + \cdots}}{V_f}$$

(2)

If the system contains only resistive components, the THD does not depend on the input frequency. For calculating the THD, we consider the range of load lineas as shown in Figure 2. From such a distribution, we estimate the average, $\mu_{THD}$, and standard deviation, $\sigma_{THD}$, of THD.

Throughout the discussion, we also consider the average of the measurements for a given array. Such averages are indicated by a bar above the respective measurement. For instance, regarding the average, $\mu_\beta$, and standard deviation, $\sigma_\beta$, of individual transistors, the overall averages of these properties for all transistors in a given array are respectively represented as $\bar{\mu}_\beta$ and $\bar{\sigma}_\beta$.

Since we consider many properties to characterize the devices (i.e. the mean and standard deviation of $\beta$, $A$ and THD), it is useful to reduce the complexity of the data in order to aid the interpretation of the results. Such a task can be accomplished by using Principal Component Analysis (PCA) [7]. Given a dataset containing $m$ features, PCA can be used to define a new, smaller, set of features $PCA_1, PCA_2, \ldots, PCA_k$ providing optimal preservation of the data variance. The first component ($PCA_1$) contains the largest variance of the data, followed by $PCA_2$ and so on. The amount of variance retained by each new feature can be calculated from the normalized $i$-th eigenvalue of the covariance matrix obtained from the data. This quantity, here represented as $E_i$ for $PCA_i$, is defined in the range $[0\%, 100\%]$.

While PCA implements a projection so as to optimize the data variability along the first axes, there are other projection schemes that optimize other properties. Linear Discriminant Analysis [13] (LDA) is one of such schemes, which optimizes the linear separation between groups being, therefore (and unlike PCA), a supervised method.
III. RESULTS AND DISCUSSION

In this section, we present several analysis of the experimentally obtained characteristics of the arrays and respective BJTs. We follow a progression from a simpler measurement-by-measurement characterization, to LDA, passing by PCA approaches.

Measurement-by-Measurement Analysis

Figure 3 shows the averages and standard deviations of the several considered measurements within each array. The x-axes are organized in monotonically decreasing order.

Regarding the average current gain ($\mu_\beta$) values, shown in Figure 3(a), we have that the group average range from 50 to 140, which are typical of BJTs. Small variations of such averages are observed, except for a few cases. The group average of $\sigma_\beta$, shown in Figure 3(b), range from 3 to 8, which is very small considering the respective average values, suggesting that BJTs from a same chip are remarkably coherent regarding $\beta$. The averages of the voltage gain properties, $\mu_A$ and $\sigma_A$, in common-emitter configuration are depicted in Figures 3(c) and 3(d). The former varies from -0.40 to -0.15. Figures 3(e) and 3(f) show the group average of $\mu_{\text{THD}}$ and $\sigma_{\text{THD}}$. The averages range from 0.007 to 0.016, while the standard deviations go from 0.0005 to 0.0015. All in all, these results suggest a remarkably small parameter variation within each array.

Figure 4 shows the Pearson correlation coefficients between the several adopted measurements. It is clear from this figure that most measurements are cross-correlated, except mainly for the standard deviation of THD and voltage gain, which are much more independent in this respect. The most intense correlation results between the two gains, $\mu_\beta$ and $\mu_A$. Observe that the voltage gain is often negatively correlated with the other measurements.

PCA and Density

In addition to understanding the variability, in absolute manner, of the several measurements, it is also interesting to infer what is the effective dimensionality of the overall variability of the measurements after completely eliminating the correlation between them. This can be readily achieved by using PCA. Figure 5 shows the PCA projection of the 300 BJT samples considered in our experiments.

Several interesting findings can be derived from such a result. First, the total variation explanation for the two first axes, respectively equal to 64% and 15%, indicate that the greatest part of the variation of the transistor parameters can be accounted for by nearly just two degrees of freedom, corresponding to respective random variables defined by linear combinations of the adopted measurements. This result is in agreement with previous experiments [3] suggesting that BJT variability has a low dimensionality.

Another important result concerns the fact the BJTs belonging to the same array tend to appear near one another, defining respective groups in the PCA space. As shown in the projections respective to each of the PCA axes, the separation between arrays is much more definite along the first axis than for the second. These projections were obtained by normally individually fitting each group (corresponding to each transistor array) and then mapping into the first and second PCA axes. The dispersion of each group, as indicated in the first axis projection, tends to increase along that axis.

It is also clear that the parameter variance within each IC is substantially smaller than the variance considering all devices. Henceforth, we quantify the variance of a group of individuals by taking the trace of the respective covariance matrix, giving rise to the total variation measurement. A measurement of how effectively the parameter variation can be minimized by adopting transistors from a same IC can therefore be expressed in terms of the ratio between the total variation for all devices divided by the total variation averaged among the IC clusters. This value was obtained as being nearly 5 for the first PCA component.

It is also clear from Figure 5 that the overall distribution of BJTs is skewed, with a stronger peak at the left-hand side and a secondary, less compact, peak to the right. The first peak is characterized by $\text{PCA}_1 \approx -1.8$, and the second by $\text{PCA}_1 \approx 2.1$.

The weights of each considered measurement on each axis are given in Table I. The first axis is strongly related to the average THD, voltage gain, and current gain, as well as the standard deviation of current gain. Actually, we have from Figure 4 that these four variables are strongly correlated. In the case of the second axis, the major contribution is from the standard deviation of THD. Such results suggest to use the average voltage gain and standard deviation of THD in order to summarize the first and second axes, respectively. The respectively obtained scatter plot is shown in Figure 6. Remarkably, the arrays resulted very compact and segregated along the average voltage gain, with a gain factor of about 20 in parameter variation along the gain axis (observe that the current and voltage gain resulted highly correlated).

LDA

The LDA analysis of the 300 BJTs yielded the two-dimensional projection shown in Figure 7. At the expense of a less effective minimization of variance along the first two axes, LDA provided a new projection that maximizes the separation of groups according to scatter matrices dispersions. At the same time, the dispersion within each group became much more uniform and constrained, to the point of defining a narrow relationship.
between the two axes, which can be summarized by the dashed line. In order to try obtaining a functional relationship between the adopted measurements, we applied generalized mean least square fitting [14, 15] while rotating the two-dimensional LDA projection and seeking for the smallest fitting residual. For this, we used a second degree polynomial as the template for the fitting. In order to avoid the effect of the varying density of samples in the LDA space, windowed weighting of one axis in terms of the other was applied for each rotating configuration. Figure 8 shows the obtained optimal fitting.

The obtained fitting coefficients for the first two LDA components resulted in the following approximate relationship between LDA1 and LDA2:

\[
\text{LDA}^2 + \text{LDA}(-2.723 - 1.961 \times \text{LDA}2) + (40.93 + 0.9612 \times \text{LDA}2) \times \text{LDA}2 = 138.2, \quad (3)
\]

which can also be written approximately in terms of the
FIG. 4: The Pearson correlation coefficients between the 6 considered BJT measurements. Most measurements are correlated one another, except mainly for the standard deviation of the voltage gain.

TABLE I: The weights (or strengths) of each of the considered measurements on the first and second axes of the PCA and LDA. The larger the magnitude of such weights, the larger its effect in defining the respective axis, which are linear combinations of the original measurements.

| Axis     | \( \mu_\beta \) | \( \sigma_\beta \) | \( \mu_A \) | \( \sigma_A \) | \( \mu_{THD} \) | \( \sigma_{THD} \) |
|----------|------------------|-------------------|-------------|------------|-----------------|-------------------|
| PCA1     | 0.49             | 0.47              | 0.49        | -0.26      | 0.44            | 0.21              |
| PCA2     | 0.01             | -0.01             | 0.00        | 0.52       | -0.11           | 0.85              |
| LDA1     | -6.86            | 0.19              | 17.81       | 0.22       | 0.03            | 0.00              |
| LDA2     | -12.92           | 0.1               | 11.77       | -0.13      | 0.39            | -0.17             |

considered transistor parameters as

\[
11 \mu_A + \mu_A^2 - 0.112 \mu_A \mu_{THD} - 13 \mu_\beta \\
+ 1.85 \mu_A \mu_\beta - 0.104 \mu_{THD} \mu_\beta + 0.857 \mu_\beta^2 \\
+ 0.11 \mu_A \sigma_A + 0.103 \mu_\beta \sigma_A - 0.177 \sigma_{THD}
\]

\[= 3.516 \quad (4)\]

IV. CONCLUSIONS

Although at the core of modern electronics, the issue of transistor variability has received relatively little attention as a consequence of the effectiveness of negative feedback in controlling such an effect. However, recent studies [3] have suggested revisions of such a perspective in the sense that BJTs of a given type can have relatively consistent features (small variations), capable of defining clusters by transistor type. In other words, BJTs from the type can cluster in characteristic, distinctive groups. The current work has investigated BJT variability further, now considering transistor arrays, where the devices share the substrate and other fabrication effects. As it could be expected, the variability of BJTs inside the same IC was found to be much smaller (by a factor of 20 in the case of current gain, for the considered devices and configuration) than between BJTs from different arrays. This confirms the improved control of transistor properties when built into the same IC. At the same time, larger variations were observed among BJTs from different arrays.

It should be emphasized that, though in principle expected, the reduced variability of industrially produced BJTs inside a same chip has been rarely (if ever) systematized in the literature. The obtained results make it clear, at least for the considered array samples, that a substantial gain in standardization of BJT parameters can be achieved by using transistor arrays. However, critical projects large enough to involve multiple arrays may require the consideration of the individual characteristics of the used devices, as a consequence of the larger variation of parameters among BJTs from distinct arrays. The obtained results corroborated the potential of integrated analog design for increasing parameter uniformity. In addition, when the data was mapped in terms of the scatterplot defined by the THD variation and the voltage gain (as suggested by the strength of these measurements respectively to the two PCA axes), an even better separation was obtained between the transistor arrays, showing most of the clusters clearly segregated one another along the latter axis, while similar distributions were observe in the former axis.

Further analyses by using LDA showed an even better separation between the clusters corresponding to respective transistor arrays. Interestingly, the LDA mapping revealed a clearly defined relationship between the considered measurements, probably related to the Early effect [11, 16]. This result, as well as all the others in the current work, are respective to the considered transistor arrays samples and circuit configuration, so that further investigations are required in order to validate and further generalize them.

Perhaps as a consequence of well-established design practices, some important issues in analog electronics have been somewhat overlooked. It is, therefore, interesting to revisit such issues in the light of state-of-the-art pattern recognition and statistical analysis concepts and methods. It would be particularly interesting, for instance, to complement the currently reported study by considering other IC families (e.g. FET, MOSFET) and alternative circuit configurations, as well as to compare parameter variability between NPN and PNP devices.

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FIG. 5: PCA obtained from the experimental measurements of the 50 samples of transistor arrays, as well as the individual clusters normally fitted and projected along both axes. BJTs from a same array are shown by the same color. The estimated density of cases is shown as a cloud, from which two peaks can be observed: a more compact group to the left-hand side, and a less compact to the right-hand side.

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FIG. 6: Scatterplot obtained by plotting the variation of the THD in terms of the average of the voltage gain, also showing normally fitted individual clusters along both axes. Such a mapping, defined by two measurements suggested by the PCA, yielded a remarkable separation between the transistor arrays, especially along the average voltage gain axis. The average variation of such individual clusters was verified to be nearly 20 times smaller than the overall BJT variance considering all the clusters.
FIG. 7: LDA of the 300 BJTs, as well as normally fitted individual clusters along each axis. A good separation of the groups is obtained, and the mapping also revealed a clear functional relationship between the two respective axes.

FIG. 8: Generalized (quadratic) least mean square fitting of the LDA results, after rotation optimizing the fitting residue.