Read-out analog channel with interpolator for signal peak finding

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Abstract. A prototype of an analog channel with a digital processing system for reading signals from GEM detectors is presented. Each channel consists of a charge-sensitive amplifier, a shaper, a switch, an amplifier and a 10-bits ADC. The data from the ADC is processed by the digital system based on an interpolator to find signal peaks. The interpolator uses a 6th order Lagrange polynomial. It maintains peak detection accuracy within 1.1 LSB at 25 MHz ADC sampling rate and 270 ns shaper peaking time.

1. Introduction
Traditionally, an analog peak detector or digital peak detector are used to determine the maximum of a signal in the analog channel [1, 2]. In case the digital peak detector is used, the error in determining the maximum will depend on the ratio of the shaper peaking time and the sampling frequency of the ADC. If the signal at the channel output during the ADC sampling period changes more than by 1 LSB, then the peak detector will introduce an error determining the maximum. Figure 1 shows the error versus sampling frequency for different peaking times and orders of shaper.

![Figure 1. Maximum error of peak determination vs. ADC sampling frequency for a shaper of 2-nd and 4-th order with peaking time of 100 ns, 200 ns and 300 ns](image-url)
Therefore, the ADC sampling frequency is to be high enough. However, it is problem for design of a low power analog channel. In this paper an approach based on the use of an interpolation to increase the signal sampling rate and reduce of the peak determination error is proposed.

2. Channel Structure

The designed analog channel is intended for processing signals from the GEM detector [3] of both polarities, with an amplitude of no more than 100 fC and parasitic capacitances up to 100 pF. The channel has a differential structure and consists of a charge-sensitive amplifier, a shaper amplifier, a switch for changing signal polarities, an additional buffer amplifier and a 10-bits ADC. The channel structure is shown in Figure 2.

The charge-sensitive amplifier is implemented in a telescopic cascade architecture with an additional (boosting) amplifier to increase the open loop gain. To increase the tolerance to spikes and digital noise, the channel has differential structure starting from charge-sensitive amplifier output. Thus, the amplifier has a pseudo-differential output. The charge-sensitive amplifier followed by a 2-nd order shaper. The shaper has a peaking time of 270 ns. The switch is required to change differential signals when polarity is reversed. An additional amplifier provides amplification to increase the signal swing at the ADC input.

The equivalent noise charge of the channel is about 1000 electrons at a parasitic detector capacitance of 50 pF. The power consumption of the analog part of the channel is less than 4 mW. The ADC is built using the MCS (Merged Capacitor Switching) architecture [4, 5]. The use of MCS architecture allows to shorten the conversion time by 1 cycle and reduce the area of the ADC matrix by 2 times in comparison with the traditional architecture. The ADC has differential input, 10 bits resolution and sampling rate of 25 MHz. The power consumption of the ADC is 1 mW. Conversion is started by an external signal. Digital signals from the ADC output go to the interpolator input.

3. Interpolator

Interpolation allows to find the fit curve function, which passes through a given set of points. Knowing function, it is possible to calculate the intermediate values near the expected signal peak. In order to select an interpolation algorithm several known approaches were considered. Figure 3 shows interpolation curve for Lagrange and spline methods [6]. Both interpolation algorithms provide acceptable accuracy, but Lagrange interpolation is easier to implement in hardware. This is due to the simplification of the algorithm when working with points which evenly distributed over time axis.

The interpolation of Lagrange polynomials has been chosen for implementation. The interpolator uses the 6-th order Lagrange interpolation polynomial [7].

The data coming from the ADC to the interpolator is synchronized and written to a 6-word ring buffer. If the data matches the signal amplitude ratio pattern: $PTS[0]<PTS[1]<PTS[2]≥PTS[3]>PTS[4]>PTS[5]$, where $PTS[i]$ is the ADC counts, the interpolator calculates values at intermediate points, between samples $PTS[1]$ and $PTS[3]$. To achieve the required level of accuracy of one LSB, the values are calculated at three intermediate points between adjacent samples. This allows to increase the actual sampling rate of the ADC by 4 times. Further in the cycle, the calculated value is compared with the previous maximum, and in case the current value is less than the previous one, the maximum is fixed, and cycle stopped. Figure 4 shows the output of the shaper (ADC input) with the indicated samples, which are taken to calculate the maximum signal amplitude by the interpolator.
Figure 3. Interpolation curve fit near peak

Figure 4. Shaper output signal

Figure 5. Error of maximum determination
The interpolator has a 12-bit output with a 10-bit ADC to improve system resolution. An additional function of the interpolator is to determine the time of reaching the maximum, by which the time of arrival of the signal can be calculated in the remote system, since the time constant of the amplifier-shaper is known. The time stamp resolution is 10 ns (1 / (ADC sampling rate * 4)). The power consumption of the interpolator is 4 mW.

Figure 5 shows the error of peak determination versus the shift of the signal peak relatively to the ADC start of conversion signal for digital peak detector and interpolator. For shaper signal with peaking time equal to 270 ns, the maximum error in determining the peak without using the interpolator is 6.1 LSB, whereas with the interpolator − 1.1 LSB. This data was obtained by transistor level simulation.

The analog channel and interpolator were designed in UMC 180 nm CMOS MMRF process.

4. Conclusion
The read-out analog channel with interpolator for signal peak finding was studied. Using of the interpolator improves the accuracy of determination of the maximum in the developed analog channel to 1.1 LSB at 25 MHz ADC sampling frequency and 270 ns peaking time of the 2-nd order shaper.

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