Single electron Sensitive Readout (SiSeRO) X-ray detectors:
Technological progress and characterization

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ABSTRACT

Single electron Sensitive Read Out (SiSeRO) is a novel on-chip charge detector output stage for charge-coupled device (CCD) image sensors. Developed at MIT Lincoln Laboratory, this technology uses a p-MOSFET transistor with a depleted internal gate beneath the transistor channel. The transistor source-drain current is modulated by the transfer of charge into the internal gate. At Stanford, we have developed a readout module based on the drain current of the on-chip transistor to characterize the device. Characterization was performed for a number of prototype sensors with different device architectures, e.g. location of the internal gate, MOSFET polysilicon gate structure, and location of the trough in the internal gate with respect to the source and drain of the MOSFET (the trough is introduced to confine the charge in the internal gate). Using a buried-channel SiSeRO, we have achieved a charge/current conversion gain of $>700$ pA per electron, an equivalent noise charge (ENC) of around 6 electrons root mean square (RMS), and a full width half maximum (FWHM) of approximately 140 eV at 5.9 keV at a readout speed of 625 Kpixel/s. In this paper, we discuss the SiSeRO working principle, the readout module developed at Stanford, and the characterization test results of the SiSeRO prototypes. We also discuss the potential to implement Repetitive Non-Destructive Readout (RNDR) with these devices and the preliminary results which can in principle yield sub-electron ENC performance. Additional measurements and detailed device simulations will be essential to mature the SiSeRO technology. However, this new device class presents an exciting technology for next generation astronomical X-ray telescopes requiring fast, low-noise, radiation hard megapixel imagers with moderate spectroscopic resolution.

Keywords: SiSeRO, readout, X-ray detector, Digital filtering, RNDR, Instrumentation

1. INTRODUCTION

X-ray Charge Coupled Devices (CCDs) [1, 2] have been the primary detector technology for soft X-ray instrumentation for more than three decades in X-ray astronomy. The low noise performance ($<4$ e\textsubscript{RMS}), broad energy response up to tens of keV, high spatial and moderate energy resolution made them an obvious choice for the X-ray spectro-imagers in missions such as ASCA, Chandra, XMM-Newton, Swift, Integral, Hitomi, and AstroSat. Chandra, in particular, has been extremely successful in revealing the detailed properties of X-ray astronomical sources by combining the high angular resolution imaging with the excellent detection properties of CCDs.

Next generation X-rays CCDs, with higher readout speed and improved noise performance, also hold the potential to support future astronomical missions such as the Lynx Observatory [3], proposed earlier to NASA's
2020 Decadal Survey, and AXIS probe class mission∗, which will have order-of-magnitude larger collecting areas to probe deeper into the high redshift, faint X-ray universe. Noise performance as low as 1 e_{RMS} and associated improvements in low energy response (<500 eV) will also be highly beneficial to fully utilize these observatories. MIT Lincoln Laboratory (MIT-LL), MIT and Stanford University (SU) have together made substantial improvements in X-ray CCD technology in recent years [4, 5, 6], and in the development of fast, low noise readout electronics to support these detectors [7, 8, 9, 10]. In parallel, MIT-LL has been developing a unique Single electron Sensitive readout stage (hereinafter SiSeRO) for CCDs, intended to provide even greater responsivity and significantly better noise performance even at readout speeds >2 MHz.

In Chattopadhyay et al. 2022 [11], we discussed the working principle of SiSeROs and demonstrated the first results from these devices using a readout module developed at SU. The working principle of SiSeROs is similar in some respects to DEPFET detectors [12, 13] and draws on earlier work on floating-gate amplifiers described in Matsunaga et al. 1991 [14]. SiSeRO devices employ a p-channel metal-oxide-semiconductor field-effect transistor (MOSFET) straddling the n-channel of the CCD. When a charge packet is transferred to the internal channel beneath the p-MOSFET, it modulates the transistor drain current, which can be sensed directly. For our first generation prototypes, we obtained an equivalent noise charge (ENC) of 15 e_{RMS}. In this paper, we update the characterization test results for a new SiSeRO device (CCID93) with a buried-channel p-MOSFET transistor, obtaining highly encouraging results. We have also developed techniques to suppress 1/f correlated noise using an optimized digital filter when measuring the charge signal in the pixels. In addition, we have for the first time demonstrated Repetitive Non-Destructive Readout (RNDR) in these detectors, wherein the charge signal is measured multiple times by moving the charge back and forth non-destructively. In principle this can reduce the noise well below the 1/f barrier and into the sub-electron regime. In future work, we plan to continue to mature the SiSeRO design and further optimize the digital filtering and RNDR.

In Sec. 2, we give a brief introduction to the SiSeRO amplifiers. This is followed in Sec. 3 by a short description of the characterization test stand, readout module and the new test results for the CCID93 buried-channel SiSeRO. In Sec. 4 and Sec. 5, we discuss the new analysis techniques, namely the digital filtering and RNDR techniques respectively. The results are summarized along with future plans in Sec. 6.

2. OVERVIEW OF SISERO DEVICES

In this section, we give a brief overview of the SiSeRO devices we are testing. Details of the working principle can be found in [11]. The SiSeRO amplifier, shown in Fig. 1, is a floating-gate amplifier, where a P-MOSFET gate (‘S’, ‘G’, and ‘D’ in the figure refer to Source, Gate, and Drain respectively) sits above the CCD channel. When a CCD charge packet is transferred beneath the gate, it modulates the drain current of the transistor, which is proportional to the source signal strength. The signal is brought directly out of the package through the source or drain of the transistor, enabling the device to be operated in a drain-current readout mode. Once the charge is readout, the internal channel is emptied by the resetting the channel to reset drain (‘RD’) using reset gate (‘RG’) switch. The ‘Sg’ and ‘OG’, in the figure refer to the last serial clock register and output gate respectively. The output gate is normally connected to a small positive DC bias to shift the charge from the serial register to the internal channel.

For current readout devices like SiSeROs, the noise of the output stage depends on the conversion gain, $G_q$ (pA/electron) and the transconductance, $g_m$ (µS) of the transistor. From first principles, it can be estimated that the device output stage noise can be as low as 1 e_{RMS} for a $G_q$ of 1400 pA/e and $g_m$ of around 20 µS for 1 MHz of readout speed. In the case of SiSeROs based on a single polysilicon MOSFET, the internal gate minimizes parasitic capacitance on the sense node, resulting in a high conversion gain and minimized noise. Further, MOSFETs show larger transconductance per unit area than JFETs (used in CCDs) and especially small MOSFETs can achieve very high signal speeds. SiSeROs also offer the potential for RNDR: since the charge packet in the internal gate is unaffected by the read out process, it can be moved around like any charge packet in a CCD. This can in principle reduce the noise below the 1/f barrier and deep into the sub-electron regime. Together, these properties identify SiSeROs as a device class with the potential for sub-electron noise and very high-speed performance.

∗https://axis.astro.umd.edu/
In Chattopadhyay et al. 2022 [11], we used the first generation prototype SiSeRO devices to demonstrate its working principle and presented the first results using a drain current readout module. We estimated a charge conversion gain of 700 pA/e and around $20 \mu S$ of transconductance, obtaining an ENC of $15 e_{RMS}$ and a full width at half maximum (FWHM) spectral resolution of 230 eV at 5.9 keV. These first prototypes used surface channel transistors in which we expect the Si interface states to capture and release mobile carriers, causing excess noise that is multiple times that of the theoretical lower limit. In this paper, we characterize a new SiSeRO device that uses a buried transistor channel. In absence of trapping and de-trapping of the charge carriers from the Si interface states, we can expect improved noise performance from these devices. Details of the experiment and results are given in the next sections.

3. CHARACTERIZATION OF A CCID93 DEVICE (BURIED-CHANNEL SiSeRO)

3.1 Experiment Test Stand

The test stand, along with the readout module (also known as the ‘Tiny Box’, see [15] for details) and the X-ray detector are shown in Fig. 2a. A compact (13 cm $\times$ 15 cm $\times$ 6.5 cm) aluminum vacuum chamber houses the X-ray detector. The detector is mounted in the middle of the chamber on an aluminum cold block (or cold finger) and faces upward towards the top flange (not shown here). An X-ray entrance window on the top flange allows X-ray photons to illuminate the detectors. A thermo-electric cooler (TEC) is used to cool down the detectors. A liquid plate on the back of the bottom flange removes the heat deposited by the TEC. We use a Proportional-Integral-Derivative (PID) algorithm to control the temperature of detectors with better than 0.1°C accuracy.

For this experiment, we used a CCID93 detector (see Fig. 2a), a prototype X-ray CCD with a buried-channel SiSeRO at the output stage. The test device, developed by MIT-LL, is fabricated in an n-channel, low-voltage, single-poly process. The device active area is $\sim 4 \text{ mm} \times 4 \text{ mm}$ in size with a $512 \times 512$ array of 8 $\mu \text{m}$ pixels. The test detector, used in the experiment, is a front-illuminated device. The readout module consists of a preamplifier board (the green circuit board in Fig. 2a) and an Archon controller (the black box in the figure). The preamplifier uses a drain current readout where an I2V amplifier first converts and amplifies the...
SiSeRO output and a differential driver, at the second stage, converts the output to fully differential signal at the input of the differential ADCs in the Archon controller. In Chattopadhyay et al. 2022 [11], we discuss the schematic of the preamplifier chain along with LTspice simulations* for the transient and ac performance of the circuit. The simulation results suggest a low noise yield from the readout circuit. The Archon [16], procured from Semiconductor Technology Associates, Inc (STA†), provides the necessary bias and clock signals to run the detector, digitize the output signal and perform correlated double sampling (CDS) to generate 2D images.

3.2 Results

Figure 2b shows the digital video waveform sampled at every 10 ns as obtained from the Archon controller. The readout speed of the detector is set at 625 kpixel/s (each pixel is 1600 ns long). The change from the baseline (denoted by the two blue dashed lines) to the signal level (denoted by the two dashed red lines), after the charge packet is transferred from the output gate to the internal channel (see Fig. 1), is directly proportional to the amount of charge transferred. The signal amplitude is extracted by taking the difference between these two levels (CDS) for each pixel, which are then used to generate the 2D images. Read noise is estimated from the distribution of charge in the overclocked pixels (an array of over-scanned pixels with no physical existence). An example of such distribution in ADU (Analog to Digital Unit), obtained from one of the dark frames at 250 K (-23°C), is shown in Fig. 3a. The distribution is fitted with a Gaussian (shown in red dashed line) to quantify the RMS of the distribution. From the known conversion gain of the system, the read noise is estimated to be around 6.44 $e^{-RMS}$. An ENC of 6.44 $e^{-RMS}$ in the buried channel SiSeROs shows a significant improvement in the noise performance compared to the surface channel p-MOSFET SiSeROs, where we estimated the noise to be around 15 $e^{-RMS}$ [11].

The spectral performance of the device was evaluated using a $^{55}$Fe radioisotope. The X-ray images are first corrected for bias (using the over-scan region) and dark current (using the dark frames). We generate an event list of 9-pixel islands around each X-ray event. We then apply a secondary ADU threshold to grade the events and generate spectra for each of the event grades. An X-ray spectrum showing Mn K$_{\alpha}$ (5.9 keV) and Mn K$_{\beta}$

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*https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html
†http://www.sta-inc.net/archon/
Figure 3: (a) Distribution of charge in ADU from the over-scan region. The red dashed line is a Gaussian fit to the distribution. The read noise is estimated be around $6.44 \epsilon_{RMS}$ (b) A spectrum showing the Mn K$_\alpha$ (5.9 keV) and K$_\beta$ (6.4 keV) lines from a $^{55}$Fe radioactive source for single-pixel (grade 0) events. The FWHM is estimated to be 147 eV at 5.9 keV.

(6.4 keV) lines from the radioactive source is shown in Fig. 3b. The spectrum is generated using single-pixel events (grade 0 events). The red lines are Gaussian fits to the Mn K$_\alpha$ (5.9 keV) and Mn K$_\beta$ (6.4 keV) lines in the spectra. We calculate a FWHM of 147 eV at 5.9 keV. As expected, the energy resolution, in the case of buried-channel SiSeROs, has improved significantly from the previous results of 230 eV at 5.9 keV for the surface channel SiSeROs. We also calculated the conversion gain ($G_q$) of the system to be around 800 pA per electron. The transconductance ($g_m$) of the device is estimated to be around 25 µS.

4. 1/F CORRELATED NOISE AND DIGITAL FILTERING

From the estimated conversion gain of 800 pA per electron and transconductance of 25 µS, the thermal noise in these SiSeRO devices is expected to be around $2.5-3 \epsilon_{RMS}$ at a readout speed of 625 kpixel/s. We have observed a large 1/f noise in the frequency spectrum of these detectors with a 1/f corner frequency close to the typical readout rate of the detectors (625 kpixel/s in this case). The Archon uses a default box filter in the CDS of the digital waveform. Although a box filter is preferred in cases where the total noise is dominated by the thermal white noise, it is not ideal when the total noise is dominated by both thermal and 1/f noise. Papers [17] and [18] discuss new digital filtering techniques to reduce the 1/f noise in the sensors. Stefanov et al. 2015 [17] discuss a filter optimized for low frequency correlated noise suppression. On the other hand, Cancelo et al. 2012 [18] estimates the low frequency correlated noise in the waveform and subtract it. Both techniques are shown to provide significant improvement in the overall noise performance.

In our test setup, we have the flexibility to save the raw waveform for the pixels, which allows us to explore digital filtering techniques. Here, we discuss the effect of an optimized filter (hereafter ‘cusp’) for digital CDS on the noise performance. In Fig. 4, the black solid lines show the weights of the cusp filter in the baseline and signal regions of the waveform (shown in red solid line). The baseline samples multiplied by the positive filter weights and the signal samples multiplied by the negative filter weights are added together to calculate the charge in each pixel. In case of a box CDS, the filter weights are equal along the baseline and signal samples. Because of the correlated low frequency noise embedded in the waveform, the baseline and signals are affected by a small but unequal amount in ADU amplitude, which leads to additional noise after the CDS. To minimize this effect, we apply higher filter gain near the charge transfer, as shown in Fig. 4. The noise performance depends on multiple factors including the weights, sampling region etc. While more samples are useful to average out the white thermal noise, the filter peak frequency (highest gain in frequency domain) shifts to a lower frequency...
Figure 4: Digital filtering: the black lines (plotted against the left axis) show the weights of the CDS cusp filter used here. The waveform of the SiSeRO is shown in the red line plotted against the right axis. With this filtering technique, the read noise is improved to $6 \sigma_{\text{RMS}}$ (varies roughly as $1/N_{\text{sample}}$) and deeper into the 1/f domain. Therefore, it is important to optimize the sample size and weight ratios simultaneously to achieve best noise performance with this technique. The read noise was improved by 6-7% to $6 \sigma_{\text{RMS}}$ by the cusp filtering from the default box CDS. We expect further improvements in the noise performance by estimating the 1/f correlated noise across a series of pixels, interpolating at the time of the signal for each pixel, and then use this to correct the pixel baseline. This work is currently in progress and will be reported at a later date.

We also attempted a new digital filtering technique where we include the baseline samples from the adjacent pixel to calculate the baseline for CDS. The advantage of this technique is that, while with more samples from the adjacent pixel the average thermal noise is expected to decrease, this sampling does not also allow the filter peak frequency to shift into the low frequencies, resulting in no excess 1/f noise. The read noise with this technique is estimated to be around $5.2 \sigma_{\text{RMS}}$. Figure 5 shows a single pixel spectrum obtained from this technique from a $^{55}$Fe radioactive source. The FWHM at 5.9 keV Mn K\text{\textalpha} line is estimated to be around 130 eV.

5. REPETITIVE NON-DESTRUCTIVE READOUT (RNDR)

Since in SiSeROs, the charge packet remains unaffected in the readout process (not transferred to a doped node like in CCDs), we tried to explore the possibility to utilize RNDR by moving the charge packet multiple times between the internal channel and the adjacent output gate. This technique has been demonstrated for DEPFET devices with sub-electron read noise yield [19] and related efforts have been demonstrated on Skipper CCDs [20]. An advantage of repetitive readout of the same charge signal is that the non-white noise (1/f noise) can be significantly attenuated, resulting in extremely low noise.

In Fig. 6a, we show the waveform for one pixel in RNDR readout. Here we implemented nine repetitive readout cycles which results in an increase in the readout time by nine times (overall readout rate is $\sim$63 kpixel/s). For each repetitive cycle, we first move the charge from the internal channel back to the output gate (OG, see Fig.1) by applying a positive clock potential (>channel potential which is around 2 V) to the OG. Note that in normal applications, OG is connected to a positive DC bias (0.5 V). However, in RNDR, to move the charge back and forth, we clock OG between 0.5 V (OGLow) and 4 V (OGHigh). The last serial clock (Summing Well or SW in CCID93) is then made high and OG is made low simultaneously to move the charge to SW. As OG settles down to OGLow, this introduces the individual baselines (from B$_2$ to B$_9$ in Fig. 6a) that we see in the waveform. The charge packet is then moved back to the internal channel by changing the SW potential to SWLow (<OGLow). This introduces the individual signal regions (from S$_2$ to S$_9$ in Fig. 6a) in the waveform.
Figure 5: An example spectrum obtained using the digital double baseline CDS filter which improves the read noise to $5.2 \, e_{RMS}$ (see text for more details). It shows the Mn K$_\alpha$ (5.9 keV) and K$_\beta$ (6.4 keV) lines from a $^{55}$Fe radioactive source for single-pixel (grade 0) events. The FWHM is estimated to be around 130 eV at 5.9 keV.

In Fig. 6b, we show the nine individual (blue squares) and consecutively averaged read noise measurements (red circles). The individual cycles yield similar noise measurements (shown by the blue dashed line fitted to the individual measurements), suggesting that the transfer of the signal charge into and out of the back gate of the transistor is perfect. The red dashed line ($N_{RNDR}^\alpha$) is a fit to the averaged measurements with a best fit value of -0.505 for $\alpha$. We achieved a read noise as low as 2 $e_{RMS}$ at the end of the 9th RNDR cycle.

Figure 6c shows a preliminary spectrum of for Mn K$_\alpha$ (5.9 keV) and K$_\beta$ (6.4 keV) lines generated from the single-pixel events. The FWHM at 5.9 keV is estimated to be around 121 eV. Note that the Fano limit for Silicon at 5.9 keV is 119 eV. We plan to refine this technique further such that it helps to reach sub-electron noise levels. The RNDR technique is also relevant to the gain calibration of X-ray detectors [21].

6. SUMMARY AND FUTURE PLANS

At SU, we are developing fast low noise readout electronics for the next generation X-ray CCDs for future X-ray astronomy missions. The SiSeRO amplifier, developed by MIT Lincoln Laboratory, is a novel technology for the output stage of X-ray CCDs that can provide very low noise and high speed performance. In this paper, we discussed the working principle of the SiSeROs and characterization test results for a buried-channel SiSeRO device. In our previous paper [11], we used the first generation prototype devices for characterization for which we obtained a read noise of 15 $e_{RMS}$ and a FWHM energy resolution of 230 eV at 5.9 keV. These earlier prototypes used surface channel transistors, where trapping and de-trapping of charge carriers from the Si interface states degrades the overall noise performance. In the current paper, we characterized a new SiSeRO device with a buried transistor channel. We obtained significant improvements in the noise (around 6 $e_{RMS}$) and spectral performance (around 150 eV at 5.9 keV). We also demonstrated preliminary results for 1/f correlated noise suppression by using an optimized filter in the digital CDS instead of a default box filter. We have already achieved significant improvement in the noise performance with the use of the new tools: with optimization of the digital filtering, the spectral resolution was improved to 130 eV at 5.9 keV.

For the first time with such devices, we have explored the RNDR technique. Because the charge packet can be moved back and forth non-destructively between the internal channel and adjacent output gate in the output stage of the SiSeRO, it is possible to apply the RNDR technique to lower the noise significantly, well below the 1/f barrier. In our preliminary analysis, the noise was found to improve from 6 $e_{RMS}$ to around 2 $e_{RMS}$ by
Figure 6: Preliminary RNDR results: (a) Waveform for one pixel in RNDR readout process. Here we implemented nine repetitive readout cycles. (b) Read noise from RNDR analysis. The blue points show the individual read noise measurements from 9 individual repetitive measurements whereas the red data points are obtained when we average out the consecutive measurements. The red data points are shown to follow the expected $1/\sqrt{N}$ trend. (c) The final spectrum obtained from RNDR analysis showing the Mn K$_\alpha$ (5.9 keV) and K$_\beta$ (6.4 keV) lines from a $^{55}$Fe radioactive source for single-pixel (grade 0) events. The FWHM is estimated to be around 121 eV at 5.9 keV. The Fano limit for Silicon at 5.9 keV is 119 eV. The read noise for this measurement is $2 e^{-RMS}$. 
applying 9 RNDR iterations. The final energy resolution is estimated to be around 121 eV FWHM at 5.9 keV, approaching the Fano limit of Silicon at these energies.

The results shown here are extremely encouraging. In future work, we plan to mature the digital filtering tools and develop techniques to accurately estimate the 1/f correlated noise and subtract it from the waveform. These new techniques are expected to improve the noise performance of the devices even further. With the 1/f noise subtraction and further improvements in RNDR, it might be possible to achieve sub-electron noise performance with even first generation SiSeRO devices. One of the goals of our ongoing SiSeRO development program is to characterize larger arrays of SiSeROs with multiple parallel readouts; the first examples will be fabricated in the near future. We have developed an ASIC-based readout system at SU to enable parallel readout of these devices, the details of which can be found in [8] and other papers submitted in this conference [10]. Apart from the improvements in the readout electronics and analysis software, we plan to continue testing the buried-channel devices in combination with detailed device simulations to mature the SiSeRO technology.

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