Hierarchical Temporal Memory using Memristor Networks: A Survey

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Abstract—This paper presents a survey of the currently available hardware designs for implementation of the human cortex inspired algorithm, Hierarchical Temporal Memory (HTM). In this review, we focus on the state of the art advances of memristive HTM implementation and related HTM applications. With the advent of edge computing, HTM can be a potential algorithm to implement on-chip near sensor data processing. The comparison of analog memristive circuit implementations with the digital and mixed-signal solutions are provided. The advantages of memristive HTM over digital implementations against performance metrics such as processing speed, reduced on-chip area and power dissipation are discussed. The limitations and open problems concerning the memristive HTM, such as the design scalability, sneak currents, leakage, parasitic effects, lack of the analog learning circuits implementations and unreliability of the memristive devices integrated with CMOS circuits are also discussed.

Index Terms—Hierarchical Temporal Memory, Spatial Pooler, Temporal Memory, Memristor, Spin-neuron, Crossbar.

I. INTRODUCTION

Hierarchical temporal memory (HTM) is a neuronsorphic machine learning algorithm that emulated the performance of the human brain neocortex. The main characteristics of HTM are sparsity, hierarchy and modularity. HTM consists of two main parts: the HTM Spatial Pooler (SP) and the HTM Temporal Memory (TM). The HTM SP converts the inputs to sparse binary patterns and produces Sparse Distributed Representation (SDR) of the input data. This process also refers to the encoding of the information, which is performed throughout the HTM SP. The HTM TM is the HTM part responsible for the learning process.

Algorithmic implementations of the HTM on software revealed great potential of this machine learning method for large variety of applications. The increase in the edge computing devices in the Internet of things era drives the need for hardware acceleration for near sensor processing and computing. The computational considerations of the processing speed and possibility for the real-time realization pushed for transition of the originally purely software based algorithm to the hardware implementation. As a result, hardware design of HTM became a highly attractive topic for the last few years that already produced some promising results.

In this work, we provide a comprehensive review of the analog memristive HTM implementations, which are derived and modified from the original HTM algorithm. We present the state-of-the-art studies involving the implementation of memristive HTM. We draw a comparison between the HTM digital solutions and analog memristive HTM implementations and analyze the advantages, drawbacks and open problems. We describe and compare the existing HTM solutions in relation to various applications, comparing the performance accuracy, on-chip and power dissipation. We discuss the scalability issues, the possibility and drawbacks of real memristive HTM implementation. We provide a summary of the open problems concerning memristive HTM implementation that should be addressed.

This paper is organized into 6 sections. Section II describes the HTM theory and introduces the mathematical framework for the HTM SP and TM algorithms. Section III provides the comprehensive review of the hardware implementations of HTM with the focus on the mixed-signal and purely analog implementations based on the memristive circuits. Section IV represents the survey on the HTM applications including HTM performance, power and area calculations and overview of the system level HTM implementation process. Section V provides the explicit discussion of the advantages of the memristive HTM, limitations of the hardware design and open problems. Section VI concludes the paper.

II. HTM THEORY

A. HTM Overview

HTM is a machine learning algorithm that is inspired by the biological functionality of the neocortex [6]. This algorithm attempts to reproduce the following characteristics of the neocortex: processing and representation of the information in the sparsely distributed manner, encoding of the sensory data in real time [7], consideration of the temporal changes of the input data and ability to make predictions based on the history of previous events [8].

The implementation of HTM requires consideration of two modules: Spatial Pooler (SP) and Temporal Memory (TM). The studies on functionality of HTM revealed that SP alone is able to learn and classify the data sets that are related to the numbers, pixels and letters [9]. This was validated on the practical applications related to the biometric recognition, object categorization [4], face recognition [10], [11], [12], speech

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recognition [11], gender classification [13], handwritten digits recognition [14], [9], [15] and natural language processing [16]. The purpose of SP in HTM is to train the system to recognize certain patterns of the input data such that for different inputs that possess similar characteristics particular attributes in the output are activated [6]. In other words, SP generates the sparse distributed representation (SDR) from the given input data. While SP considers the common patterns in the spatial domain, TM looks for the temporal patterns. It examines the temporal changes of the input data and makes predictions based on previous experience of having certain patterns being followed by particular types of other patterns [17].

The 3-level hierarchical structure of HTM is shown in Fig. 1 (top left). The fundamental elements within the hierarchy are cells that are grouped together to form a column. The cells in the hierarchy of HTM are the basic processing units that are used to emulate the functionality of the pyramidal neurons, where the output depends not only on the feedforward input, but also feedback and contextual information learned from previous inputs (Fig. 1, top right). The group of columns defines a region within the HTM hierarchy. Although 3-level hierarchy in Fig. 1 (top left) illustrates a single region within each of the levels, depending on the application there might be several regions. The level that is higher in the hierarchy uses the patterns from the lower levels, which usually represents more details and consequently requires more regions for the processing of these details. The 3-level hierarchy in Fig. 1 (top left) also illustrates an idea of how the analog data is transformed to the activation of certain cells in the regions of HTM.

The realization of SP requires implementation of four phases, which are initialization, calculation of overlap value, inhibition and learning process [6], [18]. During initialization phase certain number of columns within the HTM regions are selected. The selected columns are considered to receive the input data. The connection between the input and the column is established through the dendrite segment with several potential synapses. The initialization of the weight values of the potential synapses (permanence values) is performed randomly. Those potential synapses that obtained the permanence value greater than threshold are said to be connected. The activity of the synapse is related to the input whether it is active (high input) or not. The aim of the overlap phase is to compute the number of active connected synapses [7]. The frequency of the column being active with respect to its neighbors is considered by the boosting factor that is used to multiply with the active synapses. During the inhibition phase the columns that are inside of the same inhibition region having k-th highest activations become active, while others are inhibited. During the learning phase the rule for the Hebbian learning is used to update the weights of the synapses. The phases of overlap, inhibition and learning are then repeated.

The outputs that are collected from SP are used as inputs to TM. The active columns of SP produces the so-called feedforward inputs. The first step for the TM implementation is to activate the cells that are in the predictive state within the columns that won during the inhibition stage (active columns). In case if there are no cells that are in predictive state, all of the cells within the column are activated. For each of the dendrite segments the number of the synapses that are connected to the active cells is computed. If the number of the synapses is higher than the given threshold the segment is considered being active. The cells that are related to the activated dendrite segment are settled to the predictive state. The prediction in TM is based on consideration of the cells that in the predictive state. The weights of the potential synapses that are within the
activated dendrite segment are updated based on the activity of the cell. The active cell leads to the increase in the permanence value. This is considered to be a temporal change that is applied only if the feed-forward activation of the cell is correct. In case if the cell makes incorrect prediction on the feed-forward activation of the other cell, the temporal changes are removed and permanence value of the synapse being active is reduced.

### B. Mathematical Framework

1) **Spatial Pooler:** An arrangement of the input space and the output space of the HTM SP and its main steps are shown in Fig. 1 where \( x_j \) refers to the \( j \)-th input neuron in the input space. The outputs are topologically arranged into mini-columns, where \( y_i \) is the \( i \)-th output SP mini-column in the output space. The mini-column \( y_i \) is connected to the part of the input space, which is called potential connections. The synapse referring to the \( i \)-th SP mini-column is located in a hypercube of the input space with the center in \( x_i^c \) and edge length \( \gamma \). If the synaptic permanence of the synapse is greater than the threshold value, the synapse is connected. Eq.7 represents the potential input connections \( PI(i) \) to the input space and \( i \)-th mini-column [17], [12].

\[
PI(i) = \{ j | (x_j, x_i^c, \gamma) and (z_{ij} < \rho) \}
\]

where, \( (x_j, x_i^c, \gamma) = 1, \forall x_j \in (x_i^c, \gamma), \) and \( z_{ij} \sim U(0,1) \), \( z \) is selected randomly from the uniform distribution \( U \) having range \([0,1]\). The parameter \( \rho \) denotes the fraction of inputs that are potential connections within the hypercube of the input space. The uniform distribution is used for the synaptic performances to ensure that all of the synapses have equal probability of being connected [19].

The set of connected synapses are represented as a binary matrix \( B \) in Eq.2. The synapses are considered to be connected, if their value is above the threshold value \( \theta_c \).

\[
B_{ij} = \begin{cases} 
1 & \text{if } S_{ij} \geq \theta_c \\
0 & \text{otherwise}
\end{cases}
\]

The threshold parameter \( \theta_c \) refers to the percentage of connected synapses. For instance, \( \theta_c = 0.4 \) indicates that 40\% of the potential synapse are connected. The synaptic permanence from the \( j \)-th input to the \( i \)-th SP mini-column is represented by the matrix \( S_{ij} \in [0,1] \) shown in Eq.3.

\[
S_{ij} = \begin{cases} 
U(0,1) & \text{if } j \in PI(i) \\
0 & \text{otherwise}
\end{cases}
\]

Next, the local inhibition part of the HTM SP is executed through the local inhibition mechanism that implies the SP mini-columns in a particular neighborhood inhibit each other. This neighborhood \( N_i \) of the \( i \)-th SP mini-column is defined by Eq.4 where, \( ||y_i - y_j|| \) determines the Euclidean distance between the mini-columns \( i \) and \( j \) and the parameter \( \phi \) is used to control the inhibition radius.

\[
N_i = \{ j | ||y_i - y_j|| < \phi, i \neq j \}
\]

The parameter \( \phi \) is useful when the inputs are also topologically arranged to the mini-columns to ensure that all the inputs are affected by the inhibition process. If the receptive field size increases, the parameter \( \phi \) also increases. To determine \( \phi \), the average number of connected input spans of all the SP mini-columns are multiplied by the number of mini-columns per inputs. If the dimensions of SP inputs and mini-columns are same, \( \phi \) is set equal to \( \gamma \).

The measure that determines the activation of SP mini-columns for a given input pattern \( Z \) is called input overlap. The input overlap shown in Eq.5 is calculated as a feed-forward input to each mini-column.

\[
\alpha_i = \beta_i \sum_j B_{ij} Z_j
\]

The parameter \( \beta_i \) represents the boosting factor that controls the excitability of each SP mini-column. The appropriate value of the boosting factor is either selected initially or modified during training and learning phase of the HTM SP.

The activation of the SP mini-column depends on two main conditions: the input overlap is greater than a stimulus threshold \( \theta_s \) and is among the top \( s \) percentile \((prctile)\) of its neighborhood. Eq.6 refers to the active column selection, where \( \alpha_i \) is the activity of the SP mini-columns, and \( NO(i) = \{ o_j | j \in N(i) \} \) with \( s \) being the target activation density. This activation rule refers to the implementation of the \( k \)-winners-take-all computation within a local neighborhood.

\[
\alpha_i = 1, \text{if } (\alpha_i \geq prctile(NO(i),1-s)) \text{ and } (\alpha_i \geq \theta_s)
\]

In the original algorithm, the parameter \( k \), can be adjusted to regulate the desired number of winning columns [17]. However, to simplify the algorithm for the circuit level implementation, the value of the desired activity level is limited to 1 because the the inhibition phase is implemented by the Winner-Takes-All (WTA) circuits [10], [11].

In the learning phase of the HTM SP, feed-forward connections are learned using Hebbian rule and the boosting factor is updated considering the last \( T \) inputs in time. The reinforcement of input connections is performed by the increasing of the permanence value \( \rho \) by \( \rho^+ \). Whereas, the permanence of inactive connections is decrease by \( \rho^- \). It should be noticed that the permanence values are kept within the boundaries of from 0 to 1.

The update process of the boosting factor depends on the time-average activity and the recent activity of the SP mini-columns [17]. The parameter \( \alpha_i(t) \) refers to the time-average activation level in time \( t \) considering \( T \) previous inputs and current activity \( \alpha_i(t) \) of the \( i \)-th mini-column shown in Eq.7.

\[
\alpha_i(t) = \frac{(T-1) \times \alpha_i(t-1) + \alpha_i(t)}{T}
\]

The calculation of the recent activity \( <\alpha_i(t)> \) of the mini-columns in a particular neighborhood in time \( t \) is shown in Eq.8.

\[
<\alpha_i(t)> = \frac{1}{|N(i)|} \sum_j \alpha_i(t)
\]
The update process of the boosting factor is shown in Eq.[3] where the parameter \( \eta \) controls the adaptation effect in the HTM SP.

\[
\beta_i(t) = e^{-\eta(\sigma_i(t)-\bar{\sigma}_i(t))}
\]

(9)

2) Temporal Memory: HTM TM implementation and sequence learning process is illustrated in Fig. [1]. The predictive state of the cells in the HTM TM is shown in Eq.[10] where \( A^t \) is the activation matrix of size \( N \times S \) referring to \( N \) columns and \( S \) neurons per column with elements \( a_{ij}^t \) of \( A^t \) denoting the activation state of the \( i \)-th cell and \( j \)-th column at the time point \( t \). The permanence of the \( d \)-th segment of \( i \)-th cell in the \( j \)-th column is denoted as \( D_{ij}^d \). The parameter \( \tilde{D}_{ij}^d \) corresponds to connected synapses, and \( \theta \) refers to the segment activation threshold value [20].

\[
\pi_{ij}^t = \begin{cases} 
1 & \text{if } \exists d \left\| \tilde{D}_{ij}^d \cdot A^t \right\|_1 > \theta \\
0 & \text{Otherwise}
\end{cases}
\]

(10)

The calculation of the activation state is shown in Eq. [11] where, \( W^t \) refers to the top \( s1 \) percentage of column that has largest number of synaptic inputs. Typically \( s1 \) is set to \( 1\% \) to \( 2\% \) [20]. The cell in the winning column is activated, if it was in the predictive state in the previous time step.

\[
a_{ij}^t = \begin{cases} 
1 & \text{if } j \in W^t \text{ and } \pi_{ij}^{t-1} = 1 \\
1 & \text{if } j \in W^t \text{ and } \sum_i \pi_{ij}^{t-1} = 0 \\
0 & \text{Otherwise}
\end{cases}
\]

(11)

The dendrite segment activations and the learning of lateral connections is preformed using a Hebbian-like rule. Eq. [12] represents the reinforcement of the depolarized cell in a segment that subsequently become active, where \( \tilde{D}_{ij}^d \) is a binary matrix representing only positive elements of \( D_{ij}^d \), and the small values \( \rho^- \) and \( \rho^+ \) are for negative reinforcement of inactive synapse and positive reinforcement of active synapse in dendrite segments, respectively.

\[
\Delta D_{ij}^d = \rho^+ \tilde{D}_{ij}^d \cdot A^{t-1} - \rho^- \tilde{D}_{ij}^d \cdot (1-A^{t-1})
\]

(12)

Eq.[3] refers to the long term that is introduced by including a small decay to the active segments that did not become active, where \( \alpha_{ij}^t = 0 \) and \( \left\| \tilde{D}_{ij}^d \cdot A^{t-1} \right\|_1 > \theta \), with \( \rho^- << \rho^+ \) [20], [12].

\[
\Delta D_{ij}^d = \rho^- \tilde{D}_{ij}^d
\]

(13)

The research study [20] states that the Hebbian-like learning rule can be replaced by the gradient descent method on the cost function, such as prediction error, which could lead to the better accuracy results. However, the number of studies of the HTM implementation with backpropagation with gradient descent for weight update is limited, and the performance accuracy comparison of these two methods has not been done yet.

The Algorithm [1] summarizes the original HTM structure and illustrates the main processing steps. Lines 1-34 represents the HTM SP implementation, while lines 35-48 refer to the HTM TM processing. Lines 1-19 refer to the initialization stage and local inhibition calculations. Line 20 refers to the

\[\text{Algorithm 1 HTM algorithm}\]

1. Define the size of input neighborhood with potential connections, \( x_i, \gamma, \rho, \eta, \theta_s \), size of the local inhibition region, \( \theta_s \)

2. Determine \( \phi \) by multiplying the average number of connected input spans of all the SP mini-columns by the number of mini-columns per inputs.

3. if size (inputs)=size(mini-columns) then
   4. \( \phi = \gamma \)
   5. \( z_{ij} \sim U(0,1) \)
   6. if \( \forall x_j \in \{x_i^c, \gamma\} \) then
      7. \( t(x_j, x_i^c, \gamma) = 1 \)
      8. for \( (x_j, x_i^c, \gamma) \) and \( (z_{ij} < \rho) \) do
         9. \( PI(i) = j \)
      10. if \( j \in PI(i) \) then
          11. \( S_{ij} = U(0,1) \)
          12. else
              13. \( S_{ij} = 0 \)
          14. if \( S_{ij} = \theta_s \) then
              15. \( B_{ij} = 1 \)
          16. else
              17. \( B_{ij} = 0 \)
          18. for \( |y_i - y_j| < \phi, i \neq j \) do
              19. \( N_i = j \)
              20. \( a_i = \beta_i \sum B_{ij} Z_j \)
          21. for \( j \in N(i) \) do
              22. \( NO(i) = a_j \)
          23. if \( (a_i \geq \text{prctile}(NO(i), 1 - s)) \) and \( (a_i \geq \theta_s) \) then
              24. \( \alpha_i = 1 \)
          25. else
              26. \( \alpha_i = 0 \)
          27. if input connections are active then
              28. \( \rho = \rho + \rho^+ \)
          29. else if input connections are inactive then
              30. \( \rho = \rho + \rho^- \)
          31. for time period t do
              32. \( \bar{\sigma}_i(t) = \frac{(T-1)\bar{\sigma}_i(t-1) + \sigma_i(t)}{T} \)
              33. \( <\bar{\sigma}_i(t)> = \frac{1}{|N(i)|} \sum_{j \in N(i)} \bar{\sigma}_i(t) \)
              34. \( \beta_i(t) = e^{-\eta(<\bar{\sigma}_i(t)>-\bar{\sigma}_i(t))} \)
          35. Define \( N, S, \theta \)
          36. if \( \exists d \left\| \tilde{D}_{ij}^d \cdot A^t \right\|_1 > \theta \) then
              37. \( \pi_{ij}^t = 1 \)
          38. else
              39. \( \pi_{ij}^t = 0 \)
          40. for \( j \in W^t \) and \( \pi_{ij}^{t-1} = 1 \) then
              41. \( a_{ij}^t = 1 \)
          42. else if \( j \in W^t \) and \( \sum_i \pi_{ij}^{t-1} = 0 \) then
              43. \( a_{ij}^t = 1 \)
          44. else
              45. \( a_{ij}^t = 0 \)
          46. \( \Delta D_{ij}^d = \rho^+ \tilde{D}_{ij}^d \cdot A^{t-1} - \rho^- \tilde{D}_{ij}^d \cdot (1-A^{t-1}) \)
          47. if \( a_{ij}^t = 0 \) and \( \left\| \tilde{D}_{ij}^d \cdot A^{t-1} \right\|_1 > \theta \), with \( \rho^- << \rho^+ \) then
              48. \( \Delta D_{ij}^d = \rho^- \tilde{D}_{ij}^d \)

\(\triangleright\text{HTM SP}\)

\(\triangleright\text{HTM TM}\)
overlap calculations. The lines 21-26 represent the inhibition stage of HTM SP. Lines 27-30 includes the learning stage of the HTM SP, where reinforcement of active connections and suppression of inactive connections is performed. Lines 31-34 correspond to the update of boost factor. The HTM TM processing starts at line 35, where the number of columns and number of neurons per column is initialized the threshold $\theta$ is defined. Lines 36-39 refer to the determination of predictive state of the cells. The calculation of the activation function state is performed in lines 40-45. Finally, the reinforcement of depolarization cell corresponds to line 46, and the long-term depression is shown in lines 47-48.

III. HARDWARE IMPLEMENTATION

A. Mixed-signal HTM Implementation

The mixed signal implementation of HTM is represented in [14]. The HTM architecture is based on the memristive crossbar arrays combined with spin-neuron devices, spin-neuron based successive approximation register analog-to-digital converters (SAR ADCs) and Winner-Takes-All (WTA) circuits. The analog part of HTM comprised of dot-product multiplication is performed using the memristive crossbars during the inference stage to perform the pattern classification problem. The digital part of HTM involves the offline training stage, which is performed using external software. In the inference stage, the digital inputs are fetched into the crossbar and the analog crossbar outputs are converted back into digital signals.

The overall system architecture is shown in Fig. 2. The system is tested for the handwritten digits recognition. The implemented HTM architecture is hierarchical and modular. Each level of hierarchy involves both analog and digital processing. This modular architecture is tested on handwritten digits recognition, where the parts of the patterns are fetched into the separate HTM node.

B. Analog Implementation

1) Memristor-CMOS Hybrid Implementation of SP: One of the first works that presented the analog implementation of Spatial Pooler is based on memristor-CMOS hybrid circuit [10]. Similar to any neural circuit, SP design requires implementation of the synapse that allows for communication between the neurons. Based on this requirement, the work in [10] demonstrates the design for the single synapse circuit. This design is then used to construct the column of SP that consists of $S$ number of such synapses.

The circuit design for the single synapse is illustrated on the Fig. 4. The input stage of the circuit is presented by the current mirror. The input in the form of the current pulses allows for reduced impedance as compared to the cases when the current greater than the certain threshold is flowing through it. In the SAR ADC, the digital values stored in the approximation register are converted into analog currents using DTCS DAC. These currents are compared to the currents from the memristive crossbar. Then, a special latch is used to detect the output stage. Next, the SAR ADC digital outputs are fetched into the HTM TM RCNs having the same operating principles as HTM SP RCN. Finally, the digital output of HTM TM RCNs are fetched to the WTA circuit, which identified the winning index. If the HTM node is the highest in the hierarchy, the identified winning index refers to the class of the pattern. Otherwise, it represents the index of a particular temporal group.
Figure 3. RCN and SAR ADC architectures. RCN involves DTCS DAC and memristive crossbar. SAR ADC works as a current comparator and involves spin-neuron devices [14].

Figure 4. Design of single synapse circuit for the HTM architecture [10].

Figure 5. WTA circuit [23] for realization of inhibition phase of SP.

Figure 6. High-level block diagram of the SP implementation [11].

The proposed design was verified through the face recognition practical problem, where the simulations using AR database resulted in the accuracy of 80%.

2) Memristive array based implementation of SP: Another design for the SP was presented in the paper of [11]. The circuit design is based on the memristive crossbar architecture. The validation of the proposed design was performed for the face and speech recognition problems. The proposed systems allows to use SP for extraction of the most important spatial features from the input image. The block diagram of the method being used for implementation of the SP by [11] is presented in Fig. 6. The input image is divided into inhibition regions that in turn subdivided into smaller blocks that combine several pixels of the image. Fig. 6 demonstrates an example of image being divided into 4 inhibition regions with each having 4 small blocks. Single small block in the example contain 9 pixels. During the initialization stage the pixel values are normalized and the weights are randomly distributed across the memristive devices in the crossbars. Several crossbar slices are used in parallel and hence two types of columns are differentiated. Within a single crossbar there is \( N \) number of serial columns that are equal to the number of inhibition regions. The number of crossbar slices is related to the number of small blocks inside of inhibition region, which results in \( C \) number of parallel columns. Within a single column there are \( S \) number of synapses, which is related to the number of pixels being grouped by a single small block.

Circuit design of the single crossbar slice is presented on the Fig. 7. It constitutes of memristive crossbar structure,
read and write circuitry, circuit for the single synapse overlap calculation and circuit for the calculation of the total overlap of the column.

NMOS and PMOS switches allows for transition from read to write mode of the crossbar through the $V_{\text{ReadEn}}$ and $V_{\text{WriteEn}}$ enabling voltages, respectively. Read and write operations are performed for the single column at a time within a single crossbar slice. For this to be implemented, the control voltage is applied to the selected column, while all of the other columns are forced to be connected to the ground. Although this increases the time required for the processing of the single array, consideration of the single column at a time avoids the sneak path problems in the design [24]. During the read mode of the crossbars a single serial column within each of the parallel crossbar slices is activated and the voltage is read through the $M_{\text{readout}}$ memristor. This voltage is used to calculate the overlap values of each of the synapses in the column ($\alpha_{1,j}, \ldots, \alpha_{S,j}$). The summing amplifier $\text{SumAmp}$ is used to calculate the total overlap value of the column $\alpha_j$. This total overlap values of all of the parallel columns are passed through the WTA circuit [23] to determine the winning column. As a result the pixel values that are related to the column that wins among the other columns within the same inhibition region get the value of 1, while others a set to 0. This way the important features of an image could be distinguished.

![Circuit implementation of the memristive crossbar based architecture for overlap calculation stage of SP.](image)

The output from the proposed SP system is the binarized input image with the features being labeled as important and unimportant. The paper [11] suggests that the resulted features could be used for the pattern matching and classification applications. For this purpose the 2-bit memristive XOR pattern matcher was realized. The circuit design and explanations for the pattern recognizer will be presented together with the paper on memristive implementation of SP and TM [12].

3) Memristive HTM System: The analog implementation of the overall HTM system for face recognition is proposed in [25]. The system involves the input data controller, HTM SP, HTM TM, output data controller and pattern matcher. The overall architecture is shown in Fig. 8. The input data controller performs the pre-processing of the input data and selects the data samples. The HTM SP is used for the feature extraction. The HTM SP hardware are the same as in [11]. The HTM SP is followed by HTM TM processing, which is performed on software. However, the HTM TM analog outputs are saved using memristive multilevel analog memory unit shown in Fig. 9. The overall architecture of the applied memristive memory array with multilevel discrete analog memory cells is represented in [13]. The memory cell architecture can consists of 3 or 4 branches with programmable memristors. By applying different write voltage to $V_W$ node, each memristor can be programmed to a particular state. The values of the resistors are different in each branch: $R_1 \neq R_2 \neq R_3$. In this case, it is possible to store up to 256 analog values with the average error less than 10 % and up to 1024 values with the average error of approximately 20 %. The circuit involved HP TiO$_2$ memristor and the simulations with the Pickett models proposed in [26] were modified for large-scale simulations [27], [28].
4) Memristor Logic Circuit for Analog SP and Analog TM:

Recent research illustrated the modified implementation of the analog HTM SP and analog hardware design of the HTM TM [12]. Comparing to the previous works [10], [11], [25], the modified HTM SP analog circuit level implementation is more scalable and introduces randomization process, which is more accurate and closer to the original HTM SP algorithm. The overall modified HTM SP architecture is illustrated in Fig. [10]. The main modification of the HTM SP circuit is that it involves the calculation of the mean value in inhibition block instead of the traditional maximum. This brings the significant difference to the circuit level implementation of the HTM SP. In comparison to the HTM implementation in [11], the WTA and summation stage in the HTM SP is not required and replaced by the memristive averaging circuit. Also, the complete randomization of the HTM SP input weight is added. To perform the randomization phase, the set of averaging circuits with random initial weights are included to the receptor block processing in Fig. [10]. The weights represented by the resistance of the memristors refer to the synaptic connection. The synapse is either connected, which refers to the $R_{on}$, or disconnected, which is represented by memristors with $R_{off}$. The receptor block output $RB$ represents the calculation of the overlap value of the HTM SP column.

The threshold calculation block performs the calculation of the average value of all overlaps, which represents the threshold for accepting important features and rejection of irrelevant features. This selection is performed by the inhibition block involving the threshold comparison circuit consisting of the comparator and inverter. If the receptor block output is greater than the threshold value, the output of the inhibition block corresponding to this receptor block becomes 1, otherwise inhibition block output is 0. This allows to perform feature encoding with the HTM SP using analog memristive circuits.

The analog circuit level implementation of the HTM TM circuits for a single pixel is illustrated in Fig. [11]. The HTM TM circuit consists of the comparator, summing amplifier, thresholding circuit and discrete analog memristive memory array. The class template is stored in the memristive analog memory array introduced in [13]. During the training stage, the data from the HTM SP is fetched to the comparator consisting of two inverters. The second inverter has an underdrive voltage $V_{DD}$, where $V_{DD} = \rho^+$ and $V_{SS} = \rho^-$. For the comparator inputs 0 or 1, the comparator outputs are $\rho^-$ and $\rho^+$, respectively. Then, this comparator output is summed up with the stored template of the particular class using summing amplifier circuit. The summing amplifier consists of the averaging circuit and amplification stage. The averaging circuit calculates the average value between the comparator output and the stored pattern; while, the amplification circuit is used to double the average circuit results. This is equivalent to the sum of two inputs. After this, the memory array is updated and obtained results from the summing amplifier is stored. When the training phase is finished, the thresholding circuit, equivalent to the thresholding circuit in the modified HTM SP, is used to binarize the output of the HTM TM. This final binary pattern represents the final result after the training stage corresponding to a particular class, which is further used in the inference stage to perform recognition process.

The recognition process in this HTM-based system involves the memristive pattern matcher circuit shown in Fig. [12]. The matching circuit is based on the XNOR threshold logic gates [29]. The memristive XNOR gate consists of the memristive XOR gate and inverter. The memristive XOR gate includes the memristive NOR gate comprising three parallel memristors, where two of the memristors are connected to the two input signals that are required to be compared and the third memristor is connected to the control signal $V_c$. The variation of the control signal allows to control the variation of the NOR gate threshold. The XOR gate involves the memristor $R_{XOR}$ that controls the performance and threshold level of the gate. The XOR gate output is inverted to obtain the XNOR gate output. Finally, the output of all memristive XNOR gates for the input pattern are averaged with memristive averaging circuit and the final similarity score. In the inference stage, the same is performed for the different pattern class samples to compare the current input pattern with all pattern classes obtained after the HTM TM processing. Finally, the pattern matcher outputs of all classes are compared using the WTA.
The analog circuit level implementation of the HTM TM involving comparator, summing amplifier, thresholding circuit and discrete analog memristive memory array. The presented circuit is equivalent to the HTM TM processing of a single input [12].

The extension of the modified HTM SP approach from [12] is proposed in [30]. The traditional HTM SP random weight distribution approach is compared to the rule based weight assignment. In this method, the initial weights for the HTM SP are selected based on the local mean intensity of the input pattern within a particular neighborhood. The system level simulation results show that this approach allows to preserve feature sparsity and increase for recognition accuracy for face recognition problems. The hardware implementation of [30] is shown in [31]. Comparing to the HTM SP implementation in [12], modified HTM SP receptor block involves memristive mean calculation circuit, CMOS comparator and CMOS analog switch.

C. Weight update process

In all HTM implementations [12], [30], [13], [11], [10], [25], the HTM weights are programmed as particular resistive states of the memristor. As the memristor is a device that can exhibit various resistive states between $R_{ON}$ and $R_{OFF}$ and possesses a non-volatility property, it can be programmed applying a pulse of a certain duration and amplitude across the memristor. The amplitude of the pulse should be greater than its threshold voltage. The duration and amplitude of the pulse depends on the memristor characteristics, such as switching threshold, set time, reset time, $R_{ON}$ and $R_{OFF}$ parameters. The parameters vary based on the memristor material and size of the device. The number of possible resistive states depends on the memristor properties [32]. In the architectures with single synapses that are not connected to each other, the memristors are easier and faster, while in a crossbar architectures and accurate switching between crossbar rows and columns is required and the update process is slower.

D. Comparison of the memristive HTM designs

Each memristive HTM design has particular advantages and drawbacks. The mixed signal design presented in [14] calculates a dot product in HTM SP and HTM TM using memristive crossbar, where less CMOS components are required and total area and power consumption are reduced, comparing to the analog HTM implementations and equivalent FPGA implementation [14]. The efficient method of dividing a large image into smaller crossbars is applied, which allows to avoid common scalability issues related to the crossbar implementation. However, in this approach the training of weights is done offline on the software, and only inference phase is performed on hardware, which make it impossible to be used for near-sensor edge computing applications. In addition, as the emerging spin-neuron devices are used, the compatibility with CMOS/memristive circuits should be investigated further.

The memristive HTM design in [10] represents only a single synapse circuit for HTM cell and it is one of the earliest
IV. Applications of Memristive HTM

A. Overall approach for system level simulation of HTM

The example of HTM system level processing for face recognition application is shown in Fig. 13. The pre-processing phase including filtering and image normalization is not included to this example. The images are processed in a hierarchical manner starting from the HTM SP processing involving the image block processing and inhibition region processing. After the HTM SP, the sparse binary representation of the input image is formed. Fig. 13 shows the example of the processing of testing image and comparison of it to 2 training classes. In the training phase, the training image template is formed by the HTM TM combining all intra-class training patterns. The training phase includes the update of the weights of HTM synapses using Hebbian learning rules and backpropagation algorithm to minimize the recognition error. Next, in the testing phase, these trained weights are used. The test image is compared with the training templates of all classes and the similarity score for each class referring to each feature in the image (called local similarity) is calculated. The global similarity score for each class is calculated combining all local similarity scores of the same class by either summation or averaging operation. Finally, the global similarity scores are compared by the WTA function that selects the winning class. Fig. 13 illustrated the example of 2 training image in the HTM TM. If the number of training images is larger, the class template representing a particular pattern class is updated in time. Fig. 14 illustrates this process. Each training image is initially processed by the HTM SP before fetching to the HTM TM. The class template evolves with time during the training process with the HTM TM.

The parameters of the HTM SP and HTM TM vary depending on the application. Such parameters as number of cells, layers, columns per HTM region are selected experimentally and adjusted according to the application. For example, the parameters of HTM for NPL related problems [16] are different from the image classification problems [12], [11]. In research works [12], [25] and [11], the authors select the number of columns and number of regions experimentally performing system level simulations in Matlab simulations and verifying the best possible accuracy for particular applications and databases. In addition, even for the same application the number of columns can vary for different databases, and the optimum parameter for particular application can be selected based on experimental verification of the maximum possible accuracy for all databases [13]. Depending of the number of cells, layers and columns in HTM, the complexity of the circuits varies. For example, in modified HTM [12], the number of regions in HTM affects the total power consumption and on-chip area, while the number of columns effects only on-chip area. In [12], the trade-off between the accuracy variation with the number of columns and corresponding on-chip area and power consumption for particular image classification application is discussed.

The system level algorithm for the HTM system implementation is shown in Algorithm 2. The system is divided into four phases: pre-processing, HTM SP, HTM TM and
Algorithm 2 System level implementation of HTM

1: \( x = \text{grayscale}(x) \) ▷ PRE-PROCESSING
2: \( x = \text{filtering}(x) \)
3: for \( p \) inhibition regions do ▷ HTM SP
4: for \( k \) image blocks do
5: for \( j \) iterations do
6: \( W = \text{random}(S,S) \)
7: for all \( i \in W \) do
8: if \( W(i) \geq \theta \) then
9: \( W(i) = 1 \)
10: else
11: \( W(i) = 0 \)
12: end if
13: image.block\((j) = \text{mean}(W(j) \times \text{image.block}(j)) \)
14: image.block\((k) = \text{mean}(\text{all.image.blocks}(j)) \)
15: threshold.block = \text{mean}(y.image.blocks)
16: for \( y \) image blocks do
17: if \( \text{image.block}(y) > \text{threshold.block} \) then
18: inhibition.region\((y) = 1 \)
19: else
20: inhibition.region\((y) = 0 \)
21: end if
22: end for
23: if training phase then ▷ HTM TM
24: for \( c \) training classes do
25: for \( t \) training images do
26: if \( x(j) = 1 \) then
27: class.t\((c,j) = \text{class.t}(c,j) + \rho^+ \)
28: else if \( x(j) = 0 \) then
29: class.t\((c,j) = \text{class.t}(c,j) + \rho^- \)
30: end if
31: end for
32: end for
33: end if
34: else if testing phase then ▷ RECOGNITION
35: for \( c \) classes do
36: for \( j \) image pixels do
37: score\((c) = \text{sum}(\text{XOR(class.t}(c,j), x(j)))) \)
38: class = class\((\text{min(score)}) \)

The inference phase varies with the application of HTM. For prediction making applications, HTM TM is involved in inference phase and the predictions are made based on the learned training sequences. For the pattern recognition applications, inference phase involves only recognition and classification process shown in lines 34-38. All features of the input image \( x(j) \) are compared with the corresponding pixels of the class templates \( \text{class.t}(j) \) of each class \( c \) using the \( \text{XOR} \) function. Then, the similarity score \( \text{score}(c) \) for each class \( c \) is calculated. Finally, the class is determined by minimum similarity score corresponding to the minimum distance to the class template.
B. HTM Applications

The applications of the HTM algorithm and hardware implementation include face, speech and gender recognition, natural language processing (NLP) and recognition of handwritten digits. Table I presents a comprehensive comparison analysis of the different hardware implementations of HTM that were discussed in the survey. The designs are compared in terms of technology being used for the implementation, resulted recognition/classification accuracy, area and power requirements and practical application to which proposed system could be applied.

1) Face Recognition: Most of the analog HTM implementations focus on the face recognition problems. The examples of the HTM application for face recognition are shown in [10], [11], [12], [25], [13], [30]. The works involve the application of AR [33], Yale [34] and ORL databases [35]. The HTM processing face images usually involves the conversion of the RGB images into gray scale and filtering using standard deviation filter. The possible accuracy of the recognition varies from approximately 63% up to 98% for different configurations of HTM.

2) Speech Recognition: The speech recognition involving HTM is represented in [13], [12], [11]. The speech recognition is performed using TIMIT database [36]. The speech sequences are transferred into the pattern matrices and then processed as the images. The maximum speech recognition accuracy that can be achieved using HTM is approximately 95%.

3) Handwritten Digits Recognition: The digital and mixed-signal HTM implementations focus mostly on handwritten digits recognition represented in [15], [14]. The maximum recognition accuracy for the digital HTM implementation for handwritten digits recognition is 95% and 92% for mixed-signal and digital implementation, respectively.

4) Gender Classification: The HTM was also tested for gender classification problem [13]. The gender classification is similar to the face recognition and performed using [37]. For the gender recognition the HTM SP with TM performed better than the single HTM SP. The average accuracy achieved for the gender classification is approximately 71% and 63 %, respectively.

5) HTM for Natural Language Processing: The recently proposed HTM application for NLP is represented in [16]. It involves the sequence learning for detecting patterns of any natural language that is represented as a system containing several levels of symbols. It has been proposed to apply HTM for correction misspelled words on hardware level. However, the simulation results or circuit level implementation of the HTM for this purpose has not been presented yet.

V. DISCUSSION

A. Advantages of the Memristive Implementation of HTM

To discuss the advantages of the memristor based circuit realizations of HTM over the other attempted approaches, a brief overview of the non-memristive digital implementations is required. Recent publications on the digital implementation of HTM modules include FPGA platforms [9], [15] and VLSI design [39]. The circuit design for non-volatile architecture for HTM implementation using VHDL implemented in [15] requires 104.26mm$^2$ of area footprint and 64.394mW of power for an 8-channel based SP model and demonstrates classification accuracy of 91.89% for the MNIST database. The FPGA implementation of HTM [9] allows to speed up the training process and produce the accuracy of 91% for MNIST and 90% for EUNF [40] databases even with the presence of noise. While the accuracy of approximately 95% can be achieved for prediction making using HTM algorithm [39].

Comparing to the digital implementations of the HTM algorithm [9], [15], [39], the advantages of the analog memristive HTM implementations that were presented in this paper are related to the processing speed, small on-chip area and adjustable power dissipation. The full analog circuit level implementation of HTM would allow to process visual data faster, in contrast to the digital implementations that are limited by the processing frequency of FPGAs and the sampling rate of analog-to-digital and digital-to-analog converters.

The memristive devices used in the HTM design for various components, such as amplifiers, pattern matcher and averaging circuits, ensure the reduction of the on-chip area of the HTM, in comparison to the implementation that are based on resistors or fixed digital FPGAs and VLSI implementations. Also, while the digital HTM implementations have fixed area and power dissipation, the analog circuit for HTM can be adjusted. For example, the high power components, such as operational amplifiers, can be replaced by the circuit components with lower power dissipation. In addition, the other advantage of using memristors, comparing to the CMOS transistors and resistors, is low leakage currents within the device.

B. Limitations of Memristive HTM Hardware Implementation

The HTM SP algorithm is simplified to implement it using analog hardware. Such parameters as more than 1 active columns after overlap calculation, update of the boosting factor, complete Hebbian-based learning have not been implemented yet. In recently proposed studies [10], [12], [11], [25], the number of winning columns in the overlap phase of HTM SP is limited to 1 because of the overlap parameter is selected using the traditional WTA circuits. However, in the original algorithm the desired number of winning columns can be selected. To improve this limitation, the implementation of the HTM SP with adjustable number of outputs in the WTA circuit is required.

In addition, in most of the implementations the boost factor parameter is not taken into account or represented as 1. This is appropriate for the visual data processing applications [10], [12], [11], [25]. However, the original HTM algorithm implies that the boosting factor should be updated [17]. The analog circuit level implementation of the boosting factor update may open the possibility of the successful application of HTM not only for the pattern recognition and visual data processing, but also the other applications, such as prediction making.

The existing circuit level implementation of the HTM TM proposed in [12] is not scalable. The HTM TM circuit is presented for a single pixel implementation. The real time
implementation of such hardware circuits involves the consideration of the trade-offs between the parallel and sequential processing of the input data. For the parallel processing of the HTM TM circuits, the on-chip area and power is large and it is difficult to scale the architecture. However, the processing speed of such circuit is high, comparing to the implementation of the equivalent digital circuits or sequential processing of the input data using the same HTM TM design. The sequential processing requires the additional sequence control circuit.

### C. Open Problems

One of the most important problems in the hardware implementation of HTM is the continuous hardware training, learning and parameter update process. The research study [17] states that the boosting factor in the HTM SP should be updated based on the average-activity of the mini-columns considering $T$ previous inputs. The appropriate number of $T$ is selected to be 1000, which means that 1000 update cycles in analog hardware is required. Considering that the learning and update process in [12] is performed using analog memristive memories [13], the real on-chip implementation of the stable multilevel memristive memory with the long lifetime is one of the challenges in the analog circuit level implementation of the memristive HTM. Therefore, the robust analog circuit level implementation for online learning and training and of HTM is required. The fully analog learning circuit for the HTM will remove the necessity of the offline software-based or FPGA-based training process, which would improve the processing speed. Also, the implementation of the efficient and robust analog memory unit is necessary to achieve the maximum processing speed and efficient temporal data storage. The implementation of the on-chip analog memory unit for the memristive HTM will remove the necessity to have the separate storage unit, which will improve the processing speed and reduce required on-chip areas and power consumption.

The implementation of HTM with backpropagation learning has not been fully investigated in software implementations of HTM, and the circuit implementation of HTM with backpropagation has not been proposed yet. Even though theoretical HTM works mention that the backpropagation with gradient descent is one of the possible ways to update HTM weights [20], the HTM with backpropagation remains an open problem. The implementation of such circuit can increase the accuracy of the results and decrease the number of iterations in the training stage, because the weight update is much accurate in backpropagation learning comparing to the simple Hebbian rule. The Hebbian learning rule involve a simple update by $\pm \Delta$ value depending on the sign of error, while the backpropagation with gradient decent considers the gradient

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### Table I

| Papers | Specifications | Technology | Application | Accuracy | Area | Power |
|-------|----------------|------------|-------------|----------|------|-------|
| [14]  | Memristive crossbar, HTM SP and TM | Mixed-signal design: Ap-5 memory and spin-neuron devices | Handwritten digits recognition | up to 95% | NA | NA |
| [10]  | Memristor-CMOS hybrid design, HTM SP | Analog design: 90nm IBM CMOS, Yakobek memritor model [23] | Face recognition | 80% (AR database) | 56.19$\mu m^2$ (9x9 array) | 4.79$\mu W$ |
| [11]  | Memristive crossbar, HTM SP | Analog design: 180nm IBM CMOS, Biolek memritor model [27] | Face recognition | 86.42% (AR database), 86.67% (Yale database), 70% (Average for speech) | 12.51$\mu m^2$ (9x9 array) | 31.56$\mu W$ |
| [25]  | Memristive crossbar with analog memristive memory array , analog HTM SP, HTM TM on software | Analog design | Face recognition | HTM SP: 76.54%, HTM SP and TM: 83.48% | NA | NA |
| [13]  | HTM with analog memristive memory array, analog HTM SP, HTM TM on software | Analog design: 180nm IBM, Modified Pickett model [38] | Face recognition , Gender Classification | HTM SP: 76.54%, HTM SP and TM: 83.48%, HTM SP:63.06%, HTM SP and TM: 71.17%, HTM SP:up to 70%, HTM SP and TM: up to 90% | NA | NA |
| [12]  | Memristive-CMOS design involving analog memory and memristive pattern matcher, analog HTM SP and TM | Analog design: 180nm TSMC, Biolek memritor model [27] | Face recognition, Speech recognition | 87.21% up to 95% | HTM SP (1 x 4): 19.96$\mu m^2$, HTM TM (1 x 1): 23.85$\mu m^2$, Pattern matcher (1 x 1): 1.18$\mu m^2$ | HTM SP (1 x 4): 365.88$\mu W$, HTM TM (1 x 1): 442.26$\mu W$, Pattern matcher (1 x 1): 69.44$\mu W$ |
| [30], [31] | Algorithm modification of HTM SP with hardware testing [12] | Analog HTM SP modified design of modified algorithm in hardware testing [31] | Face recognition | up to 98% | Single receptor block: 13.31$\mu m^2$ | 135$\mu W$ |
of error in each update and the updates in each weight are different depending on the amount of error. The analog circuit implementation of such algorithm may lead to the decreased number of required iteration, which insures less endurance issues and longer lifetime of the memristive weights. However, the time required for update process may increase, especially in a crossbar, where each weight has to be updated separately. In addition, the complexity of the circuits, on-chip area and power consumption also increase, because additional CMOS components are required for the implementation.

To solve the analog HTM scalability problems, the analysis of the parasitics, sneak currents and leakage currents of the large memristive CMOS circuits is required. As in most of the cases gateless memristive arrays are used, which allows to avoid additional leakage current comparing to the gated arrays with CMOS transistors, the sneak path problems of such arrays for HTM applications should be investigated. The scalability of the memristive crossbar array for analog HTM design should be tested and the limitations of the number and side of the HTM input should be identified. Also, the performance of the memristive HTM SP and TM in terms of recognition and classification accuracy should be tested on the real memristive crossbars considering influence of the parasitic effects and sneak currents on the HTM performance.

The realistic implementation of memristive HTM circuits required at least the involvement of the large scale circuits containing the devices that induce the memristive behavior, such as resistive switching memories. However, all existing memristive devices have a limitations in terms of the number of possible memristive states. For example, the analog implementations of the memristive pattern matcher and low voltage amplifier involving the memristors that replace the resistors in the circuits [12] are practically very difficult to implement with the existing memristive devices. As the implementation of these circuits require the memristors to be programmed to exact level of resistance, the implementation of such circuits with the existing two state memristive devices is complex. One of the possibility is to use the set of memristive devices with $R_{on}$ and $R_{off}$ states connected in parallel and in series. However, the real behavior of such configuration should be tested considering parasitics, leakage and sneak currents, because the parallel and series connection of the memristors is different than in the resistors. The current flow in memristors should be considered. Memristive analog HTM implementation can involve the resistive switching memories that have been used for the implementations of the neural networks [42], however the HTM behavior will not be accurate due to the limited number of memristive states.

One of the possibility to achieve multiple resistive states is to use $GST$ memristors with 16 resistive levels [43]. However, the area of such memristors is larger and $GST$ memristor technology is not always compatible with the CMOS technology. The possibility to achieved 64 resistive levels using $SiO_2$-based memristor with $Si$ diodes is illustrated in [44]. The overall size of such device is $41 \times 19 \mu m^2 + 21.9 \times 21.9 \mu m^2$. However, the set and reset voltage of such device is very large for the HTM applications and designed circuits, because the minimum reset voltage can reach up to $17V$ with the time pulse of $1000\mu s$. The recent works illustrate the possibility of implementation of multilevel states with the use $SiN_x$-based memristor, which is compatible with the CMOS technology, can be used in a crossbar array and suppresses the issue of sneak path currents [45]. The switching time of such memristors is $100ns-200ns$, which is relatively fast comparing to HP $TiO_2$ memristors [46]. However, the switching voltage is large (greater than $5V$ [45]). In addition, the memristor has not been tested for HTM applications. The HTM circuits have to be adjusted to use with $SiN_x$-based memristors, because the read pulse for HTM circuits was set to $1V$, while the read pulse for $SiN_x$-based memristors is $0.2V$ [45].

In addition, the real memristive devices are not always accurate and involve the problem of switching stochasticity. Two real memristors of the same technology can react differently to the same voltage applied across the memristor for the switching [47]. The switching time and level may vary or, according to the theories of probabilistic behavior of the memristor, the switching may not occur. Such behavior of memristive devices may effect the performance accuracy of the HTM SP and HTM TM significantly. For example, in the HTM TM more training images and training cycles may require to achieve the same accuracy and system level HTM performance due to these variabilities in the behavior of the memristor.

VI. Conclusion

In this work, the comprehensive survey on the memristive HTM has been presented. The existing HTM digital, analog and mixed signal implementations have been reviewed and their advantages and drawbacks have been identified. The architectures of memristive HTM have been compared in terms of accuracy, on-chip area and power. In addition, the applications of HTM, including face, speech and handwritten digits recognition, gender classification and NLP, and proposed hardware solutions were reviewed.

The analog memristive HTM implementation has an advantage in terms of processing speed, small on-chip area and possibility to adjust to total power consumption of the HTM circuit by replacing the conventional elements with low power circuit configurations. However, the analog hardware limitations do not allow the implementation of the traditional HTM algorithm and impose several modifications of the original HTM algorithm. The open problems in the memristive HTM implementation include the scalability of the analog circuits and memristive crossbars, the limitation in the number of states and unpredictable behavior of real memristive devices and a lack of full circuit level implementation of the robust analog memory unit and learning algorithm for the weight update process in the HTM SP and TM.

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