Nonlinearity-Induced Spurs in Fractional-N Frequency Synthesizers

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Abstract—Fractional-N frequency synthesizers are characterized by unwanted periodic components in their frequency spectra called spurs. In communications applications, spurs reduce the signal to noise ratio of the system; in clocking they add jitter; in radar and imaging, they can present ghost targets. Some spurs are due to parasitic electromagnetic coupling between components and can be mitigated by careful circuit layout. Others are inherent in the mathematics that describe the system and are best tackled using mathematical approaches. This brief considers spurs that are introduced directly by the divider controller and those that result from distortion of the control signal by nonlinearity in the synthesizer. It summarizes the state of the art in terms of divider controllers that are themselves spur-free and divider controllers that do not produce spurs when used in synthesizers with memoryless polynomial nonlinearities.

Index Terms—Frequency synthesizer, digital delta-sigma modulator, fractional-N phase locked loop, nonlinearity.

I. INTRODUCTION

Frequency synthesizers are used throughout modern electronic systems to produce signals at precise frequencies. These signals are typically used as clocks in wired systems and as modulation and carrier signals in wireless communications. The most common way to synthesize a frequency is by indirect synthesis [1]. A phase locked loop (PLL), which incorporates a frequency divider, is used to lock the output of the synthesizer to an accurate reference frequency, as shown in Fig. 1. The reference signal \( f_{\text{ref}} \) is normally a squarewave derived from crystal oscillator. The output signal is produced by a controlled oscillator (CO). This signal is divided by a frequency divider in the feedback path of the PLL that outputs one falling edge for every \( N \) falling edges of the output signal. The time difference between a falling edge of the reference signal \( f_{\text{ref}} \) and that of the divided signal \( f_{\text{out}} \) produces an error \( e \) that, after filtering, controls the CO. When the PLL is locked, the output frequency \( f_{\text{out}} \) is a multiple of the reference frequency \( f_{\text{ref}} \).

Specifically, when the division ratio is \( N \), the output frequency is locked to \( N \) times the reference: \( f_{\text{out}} = N f_{\text{ref}} \). When \( N \) is an integer, frequencies that are spaced by \( f_{\text{ref}} \) can be generated.

This is called the integer-N (int-N) mode of operation and is used in applications such as clocking of digital systems where a small number of widely spaced frequencies is required.

The process of measuring the time difference once per cycle of the reference clock introduces a periodic disturbance in the loop, that manifests itself as a periodic spurious tone (spur) at an offset of \( f_{\text{ref}} \) from the output frequency; this is called the reference spur [2]. If the reference frequency is much higher than the bandwidth of the PLL, the reference spur can be attenuated significantly by lowpass filtering. Spurs that arise at frequencies closer to \( f_{\text{out}} \) are typically more problematic.

In applications such as wireless communications, the synthesizer is usually required to generate many frequencies that are spaced more closely than \( f_{\text{ref}} \). If \( N \) is expressed as the sum of an integer \( N_{\text{int}} \) and a rational number \( \alpha \), where \( 0 \leq \alpha < 1 \), then

\[
f_{\text{out}} = (N_{\text{int}} + \alpha)f_{\text{ref}},
\]

and the frequency spacing is a fraction of \( f_{\text{ref}} \); this is called fractional-N (frac-N) mode [3].

Fractional division is achieved by toggling a multimodulus divider between integer values. For example, an average division ratio of 41.25 can be achieved by dividing by 41 with a probability of 0.75 and by 42 with a probability of 0.25. The frequency divider is controlled by a divider controller, the purpose of which is to fix the average while randomizing the instantaneous division ratio. If the randomization is inadequate, periodic patterns may appear in the controller output and subsequently the time difference signal \( e \). This, in turn, causes periodic modulation of the loop and spurious tones appear at the output that are caused directly by the divider controller [4], [5]. For example a simple periodic pattern of

Fig. 1. Block diagram of a PLL-based indirect frequency synthesizer.

Manuscript received February 6, 2022; revised April 5, 2022; accepted April 11, 2022. Date of publication April 21, 2022; date of current version May 27, 2022. This work was supported in part by the Science Foundation Ireland under Grant 13/IA/1979 and Grant 20/FFP-A/8371, and in part by Enterprise Ireland under Grant TC-2015-0019. This brief was recommended by Associate Editor E. Bonizzoni. (Corresponding author: Michael Peter Kennedy.)

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSII.2022.3169224.

Digital Object Identifier 10.1109/TCSII.2022.3169224

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Fig. 2. Power spectra of different divider controllers: undithered MASH 1-1-1, MASH 1-1-1 with first-order least significant bit (LSB) dither and undithered HK-MASH. In each case, the input and initial state are even.

| Architecture     | Initial state | Dither | Cycle length |
|------------------|---------------|--------|--------------|
| MASH 1-1-1 [16]  | even          | N      | 4            |
| MASH 1-1-1 [16]  | odd           | N      | 2M           |
| MASH 1-1-1 [18]  | even          | Y      | 4 × Lsd      |
| MASH 1-1-1 [18]  | odd           | Y      | 2M × Lsd     |
| HK-MASH [23]     | even          | N      | M²           |

In the frequency synthesizer application, spurs within the bandwidth of the loop are problematic as they cannot be attenuated. Additive pseudorandom dither increases the length of the cycle [17]–[20] and thereby attenuates the associated fractional spur. When first-order shaped LSB dither is introduced into the MASH 1-1-1, its spectrum (the solid curve in Fig. 2) is smooth and spur-free. The additional noise contribution due to the shaped dither manifests itself as a 20 dB/decade slope at low frequencies. Qualitatively, mitigating spurs normally involves adding dither or higher order noise shaping, both of which result in higher low frequency noise [13].

Additional ways to mitigate fractional spurs introduced by the divider controller itself include restricting to odd-valued inputs, choosing odd initial conditions, adding feedback and feedforward paths, and/or using a prime modulus M [6], [8], [21], [22].

Table I summarizes the guaranteed shortest cycle lengths for several architectures. M is the modulus of the controller and Lsd is the period of the pseudorandom binary dither signal [18]. In the worst case, an undithered MASH 1-1-1 can produce a cycle with a length (period) of just 4 [16]; therefore, dithering is normally used in practice [7]. The HK-MASH variant [23], which behaves as if its modulus were a prime number, has an extremely long cycle for all inputs and for all initial conditions, making it effectively spur-free, even without dithering, as shown dashed in Fig. 2.

Many other spur-free divider controllers have been developed in recent years. For the remainder of this brief, therefore, we will assume that the divider controller is spur-free.

While a spur-free divider controller output is necessary to eliminate fractional spurs, it is not sufficient, because interaction with nonlinearity in the PLL causes nonlinearity-induced spurs [9], [10].

Fig. 3 shows contributions of various divider controllers to the output phase noise spectrum of a synthesizer without and with a cubic nonlinearity. All three divider controllers are themselves spur-free, and classical linear analysis [24] suggests that their contributions to the output phase noise can be spectrally masked by the phase noise of the oscillator itself, as shown in Fig. 3(a). However, for two of these examples—the dithered MASH 1-1-1 and the undithered HK-MASH—the synthesizer exhibits spurs when their outputs are distorted by the nonlinearity, as shown in Fig. 3(b).

In the next section, we will consider such spurs that are caused by interaction between the signal introduced by the divider controller and nonlinearity in the synthesizer loop. We will describe architectures that are spur-free both before and after nonlinear distortion.
III. SPURS DUE TO INTERACTION BETWEEN THE DIVIDER CONTROLLER AND NONLINEARITY IN THE LOOP

Mitigating spurs caused by nonlinearity in the PLL is a difficult problem because the nonlinearity is usually unknown. Nevertheless, key nonlinearities in charge-pump PLLs (CPPLLs) can be modelled by a truncated memoryless power series [25], [26]. Furthermore, stochastic signal processing can be used to define performance bounds and inspire architectural innovations that can mitigate spurs [26]–[31]. Familier and Galton proved that it is possible to design divider controllers that are immune to polynomial distortion up to a given order [28]. As an existence proof, they elaborated successive requantizer (SR) architectures that are optimal with respect to spurious tone immunity in the sense that they have the highest possible order of immunity to polynomial nonlinearity [26]–[29].

A. Periodic Nonlinearity Noise

An intuitive explanation of the spur production mechanism shows how one may determine the locations and amplitudes of the spurs in a frac-N synthesizer by calculating the so-called periodic nonlinear noise (PNN) [32].

Samples of the phase error \( e_{acc} \) introduced by a divider controller in fractional-N mode with a constant input lie on a number of parallel tracks \( \tau_k \) that have a characteristic sawtooth shape, as shown in Fig. 4(a). Samples of \( e_{acc} \) are distributed over the tracks \( \tau_k \) with a probability distribution \( P(\tau_k) \). Each track \( \tau_k \) is distorted by the nonlinearity, denoted \( N(\cdot) \), yielding distorted tracks \( \hat{\tau}_k \), as shown in Fig. 4(c). Samples of \( e_{acc}^{NL} \) lie on the distorted tracks.

The PNN, which is the instantaneous average of \( e_{acc}^{NL} \), is calculated as a weighted sum of the distorted tracks:

\[
\text{PNN}[n] = \sum_k \hat{\tau}_k[n]P(\tau_k[n]),
\]

where the number of tracks depends on the architecture of the divider controller. Further details of the PNN and its applications can be found in [30], [32].

If the PNN is time-varying, the synthesizer exhibits fractional spurs; if it is constant, the nonlinearly distorted contribution from the divider controller to the output phase noise of the synthesizer is spur-free [30]. This method has been used to show that a synthesizer with a MASH 1-1-1-1 divider controller is spur-free in the presence of cubic distortion and explains why the corresponding spectrum (marked with \( \times \)) in Fig. 3(b) is spur-free. Furthermore, it has inspired the design of the enhanced nonlinearity-induced noise performance (ENOP) DDSM architecture [31] that is also optimal in the sense of Familier and Galton.

Fig. 5 shows PNN waveforms for MASH 1-1-1, MASH 1-1-1-1, and ENOP controllers interacting with the same cubic nonlinearity. The PNN for the MASH 1-1-1 is close to sinusoidal. This indicates a strong fractional spur, as seen in Fig. 3(b). By contrast, the PNNs for the MASH 1-1-1-1 and ENOP are constant, indicating no spurs.

Table II summarizes levels of spur immunity for some representative divider controller architectures interacting with memoryless polynomial nonlinearities. It has been hypothesized that an \( l \)th order MASH is immune to spurs following

Fig. 3. Contributions of various divider controllers—MASH 1-1-1 with first-order LSB dither, undithered HK-MASH and MASH 1-1-1-1 with first-order LSB dither—to the output phase noise output spectrum: (a) with no nonlinearity, (b) after interaction with a cubic nonlinearity.
Fig. 5. PNN waveforms for MASH 1-1-1, MASH 1-1-1-1, and ENOP divider controllers and a cubic nonlinearity.

TABLE II
ORDER OF POLYNOMIAL SPUR IMMUNITY

| Architecture       | Output range | Noise shaping order | Spur immunity order |
|--------------------|--------------|---------------------|--------------------|
| MASH 1-1-1 [30]    | [3,4]        | 3                   | 2                  |
| MASH 1-1-1-1 [30]  | [7,8]        | 4                   | 3                  |
| SR [29, Fig. 6]    | [7,8]        | 2                   | 3                  |
| ENOP [31, P1]      | [2,3]        | 2                   | 3                  |

Fig. 6. Contributions from representative divider controllers to the output phase noise of a fractional-N synthesizer with a cubic nonlinearity: first-order dithered MASH 1-1-1-1, successive requantizer, ENOP.

The polynomial distortion of order up to \((l - 1)\) [30]. The SR and ENOP are capable of optimum spur immunity [27], [28], [31].

Fig. 6 shows simulated phase noise contributions from MASH 1-1-1-1, SR and ENOP divider controllers to a fractional-N synthesizer with a third order polynomial nonlinearity. Consistent with Table II, all three modulators are spur-free after cubic distortion. Note that they produce differing levels of excess inband noise. The MASH 1-1-1-1 and the SR have the largest output range and exhibit a high level of folded noise. The ENOP produces the least nonlinearity-induced noise of these three.

B. Stochastic Divider Controllers

Stochastic divider controllers such as the successive requantizer [26] come in many varieties, including the probability mass redistributor [33], time-invariant probability modulation [34], and probability density shaping [35]. They have been used in CP-PLLs, bang-bang (BB-PLL), sampling and all-digital PLLs (ADPLLs) to achieve record levels of spur mitigation. Table III summarizes reported worst case inband fractional spurs for a selection of architectures.

In fractional-N CP-PLLs, quantization noise is introduced only by the divider controller and the dominant source of nonlinearity is the phase-frequency detector and charge pump in the time difference measurement block. By contrast, digital-intensive architectures typically use time to digital converters (TDCs) for time difference measurement and a finite state machine, such as a dithered DDSM, to drive a digitally-controlled oscillator. These introduce additional sources of quantization noise and hard nonlinearities that worsen the fractional spur problem [39]. Although CP-PLLs have historically led the field in terms of fractional spur performance, the use of digital to time converters (DTCs) to minimize the instantaneous time difference to be measured and stochastic divider controllers to mitigate residual nonlinearities have enabled significant recent advances for digitally-assisted [37], [40] and all-digital PLLs [35], [38]. There is further scope for improvement in digital-intensive architectures in terms of their spur performance [41].

C. Wandering Spurs

In addition to fixed spurs, fractional-N frequency synthesizers can exhibit a type of spur that moves about in the spectrum [42]. The phenomenon is normally observed on a spectrum analyzer and manifests itself in different ways, depending on the configuration of the instrument. The spectrum can jump up and down or spurs can appear to “walk” or “march” across the screen from one sweep to the next. Therefore, the phenomenon goes by many colloquial names, including walking, marching, traveling and wandering spurs.

Recently, the wandering spur phenomenon has been explained in detail [43]–[46]. Wandering spurs result from the double integration of a constant, leading to a parabolic quantization error signal within the divider controller. When accumulated and subsequently distorted, a component related to this parabolic structure causes chirp modulation of the CO. Note that fixed and wandering spurs can coexist.

While the phenomenon has no obvious structure when viewed with a conventional swept spectrum analyzer, a clear pattern emerges when a spectrogram is plotted using a real-time spectrum analyzer. Fig. 7 shows a simulated spectrogram of wandering spurs. The horizontal axis is frequency while the vertical axis is time; the amplitude is indicated by the color. Spurious tones move linearly in frequency towards the output frequency and then away from it.

Table IV summarizes the wander rate and period between events for a synthesizer with a MASH 1-1-1 divider controller [44]. The fraction \(\alpha\) is expressed in the form \(\alpha = \frac{X}{M}\) with \(X = \frac{4kM}{D} + X',\) where \(X, M, k, D\) and \(X'\) are integers. The
Fig. 7. Simulated spectrogram showing wandering spurs events (centered on the dashed red lines) around which the spurs move towards and away from the carrier (along black dashed line).

| Input Condition | Wander rate | Period |
|-----------------|-------------|--------|
| \( k = 0, X = X' \) | \( f_{FPD} \frac{2}{M} \) | \( \frac{1}{f_{FPD} M X' X} \) |
| \( k \neq 0, X' \neq 0 \) | \( f_{FPD} \frac{1}{M} \) | \( \frac{1}{f_{FPD} M^2 X X'} \) |

Fig. 8. Measured spectrograms of a fractional-N synthesizer with wandering spur mitigation (a) disabled and (b) enabled [48].

First line of the table corresponds to the case when the fraction \( \alpha \) is close to zero. In the special case when \( X' = 0 \), the wandering spur pattern also depends on the initial condition of the divider controller [45].

A hardware solution to the wandering spur problem in a fractional-N frequency synthesizer with a MASH 1-1-1 divider controller has been demonstrated [46]–[48]. Fig. 8 shows experimentally measured spectrograms from a fractional-N synthesizer integrated circuit without and with wandering spur mitigation.

D. Fixed Spurs That Depend on the Initial State

In addition to fixed fractional spurs whose positions are determined by the fraction \( \alpha \), frac-N synthesizers can also exhibit spurs at locations that depend on the initial state of the divider controller. Consider the phase noise plot shown in Fig. 9. As expected, it contains a fractional spur at \( \omega_{ref} \) (approximately 2.2 MHz in this example). Note that, in addition, the passband contains a large number of pairs of spurs, the lowest frequency pair of which are at approximately 24 kHz. These are called “horn spurs” [49]. They can be problematic in applications because they can lie inband and contribute to jitter [50]. Their locations depend explicitly on the initial state of the system. Horn spurs and techniques to mitigate them are described in detail in [49].

IV. Conclusion

Fractional-N frequency synthesizers necessarily exhibit spurs due to the fact that the output frequency is not an integer multiple of the reference. Modulation of the division ratio by the divider controller introduces quantization noise that, when distorted by nonlinearities in the loop, gives rise to spurs at the output. We have described techniques to ensure that the output of the divider controller itself is spur-free, and divider controller architectures that do not produce spurs when they interact with specified classes of nonlinearities. Finally, we have described some less studied phenomena including time-varying wandering spurs and horn spurs that depend explicitly on the initial state of the divider controller.

Much progress has been made in the past decade in this field but many challenges remain, especially in digital-intensive architectures that contain hard nonlinearities and multiple quantizers.

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