Analysis of Discrete-Time Switched Linear Systems under Logic Dynamic Switching

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Abstract

The control properties of discrete-time switched linear systems (SLS) with switching signals generated by logical dynamic systems are studied using the semi-tensor product (STP) approach. With the algebraic state space representation (ASSR), the linear modes and the logical generators are aggregated as a hybrid system, leading to the criteria of reachability, controllability, observability, and reconstructibility of the SLSs. Algorithms for checking these properties are given. Then, two kinds of realization problems concerning whether the logical dynamic systems can generate the desired switching signals are investigated, and necessary and sufficient conditions for the realizability of the required switching signals are given with respect to the cases of fixed operating time switching and finite reference signal switching.

Key words: Discrete-time switched linear system; logical control network; semi-tensor product of matrices; hybrid system.

1 Introduction

A switched linear system (SLS) is a dynamical system consisting of a finite number of linear subsystems (or modes) and a logical rule that controls the activating subsystem during operation time. SLSs can be either continuous-time or discrete-time and can be discretized if the unit switching time is known. Due to the flexibility of mode selection, SLSs offer superior performance and can perform a wider range of tasks than any single subsystem, making them a popular choice for analysis and control. In the last three decades, there have been many advances in the study of SLSs, including stability and stabilization [1,2,3,4,5,6,7], reachability and controllability [8,9,10,11,12], observability and reconstructibility [8,13,14,15,16], and more.

In most of the existing literature on SLSs, the logical rules that generate the switching signals are usually freely chosen or determined by the range of the physical state $x(t)$, i.e. the rules are given as piecewise constant maps from each switching time to the index set of the subsystems or state-feedback switching (for example, the mixed logical-dynamical systems [17]), rather than as outputs of some logical-dynamical processes. This means that one cannot consider an SLS as a true hybrid system containing both physical and logical states, but must split it into regulatory and operational parts. Perhaps this is not surprising given the following facts:

- It is well known that modeling logical dynamical systems is not an easy task.
- Assuming that the logical rules are somehow modeled, it is also meaningless if you cannot aggregate the obtained model with the linear subsystems.
This paper presents a novel approach to the study of discrete-time SLSs where the switching signals are generated by logical dynamic systems. This approach is inspired by the work in [7] and differs from the existing literature, such as [8,9,10,11], which considers SLSs with freely chosen switching signals. The system diagram is shown in Figure 1, where the top layer (supervisor or mode changer) is a logical control network with output $\sigma(t)$, generated by logical state $\gamma(t)$ and logical input $\theta(t)$, controlling the modes of the bottom layer, i.e. the discrete-time SLS.

![Fig. 1. System diagram](image)

The proposed model is applicable to systems that contain a multi-layered structure and hybrid states, such as the cyber-physical systems (CPS) [21,22,23,24,25]. Recently, with the development of computer science, CPS has become a hot topic in the fields. A CPS has both computational and physical components and is therefore capable of performing well-defined tasks. It has been assessed by the US National Science Foundation that “the CPSs of tomorrow will far exceed those of today in terms of adaptability, autonomy, efficiency, functionality, reliability, security, and usability”. As pointed out in the title of [21], the design problems of CPSs are still challenging today, and one of the several reasons is the “lack of temporal semantics and adequate concurrency models in computing”. Another example is Game-Based Control Systems (GBCS) [26,27,28], which have been proposed to address control problems in “social, economic, and now rapidly evolving “intelligent” systems. In a GBCS, there is a hierarchical decision structure in which a regulator makes his decision first, and then the agents make their strategies to pursue an optimal payoff. Understandably, the regulator makes its policy using a logical dynamic process, and the agents are modeled by linear/nonlinear dynamical systems.

Although temporal logic still lacks a general modeling method, the logical dynamic systems of propositional logic have already been well studied with the STP approach and can be used as the computational part of a CPS. Since the birth of STP of matrices (see [29,30]), modeling logical dynamical systems is no longer a problem. Using the algebraic state-space representation (ASSR) method based on the STP approach, a logical dynamical system can be described as a linear-like system, and one can then gain insight into the system through a structure matrix. Using the STP approach, many unsolved problems, not only in logical dynamical systems but also in finite games and other applications, have been easily solved. For example, stability and stabilisation [31,32,33,34,35], controllability [36,37,38,39], observability [40,41,42,43,44,45,46], bisimulation [47,48,49], output tracking [50,51,52], identification [53,54] and many other control problems of logical dynamical systems.

Using the ASSR method, the structures of the logical control networks and the discrete-time SLSs are unified to form a linear-like hybrid system. When analyzing the discrete-time SLSs, the advantages of the ASSR method are twofold:

- The algebraic model of logical control networks in discrete-time SLSs can be embedded in the commonly used state-space model and then considered as a whole system with hybrid states.
- The properties of logical control networks, together with the limitations of switching signals inherited from the structure of logical control networks, do not need to be considered separately.

Based on the derived hybrid system, this paper first discusses the problems of reachability, controllability, observability, and reconstructibility of discrete-time SLSs under logic dynamic switching, and then provides criteria for the system realization problems. The corresponding necessary and sufficient conditions for the four properties are obtained, as well as an algorithm that provides an easy way to verify the control problems.

On the other hand, when the constraints on the switching signals of an SLS take the form of dynamical systems, we are interested in whether the logical network is able to generate the desired switching signals. Such problems are crucial for evaluating the performance of switching systems. This paper provides criteria for the solvability of the realization of logical control networks with respect to two cases of constraints on the switching signals: fixed-operating-time switches, where the time of
the signal to stay in each state is fixed; finite reference-signal switches, where the signals should follow a given reference signal sequence.

Using the ASSR method, in [7], the authors constructed logical control networks for different requirements of the generated switching sequences. Based on this, to solve the above realization problems from a different perspective, this paper provides a new set controllability and observability, and reconstructibility problems for discrete-time SLSs under logic dynamic switching are studied. The system realization problems based on two cases of switching signal restrictions are considered in Section 4 with the newly-introduced $\ell$-step input-space reachability method. An illustrative example is provided in Section 5. Section 6 contains the concluding remarks.

The rest of this paper is organized as follows: Section 2 recalls the STP-based mergence of discrete-time SLSs. In Section 3, the reachability, controllability, observability, and reconstructibilility methods for discrete-time SLSs under logic dynamic switching are studied. The system realization problems based on two cases of switching signal restrictions are considered in Section 4 with the newly-introduced $\ell$-step input-space reachability method. An illustrative example is provided in Section 5. Section 6 contains the concluding remarks.

The notations used in the text are listed below:

- $\mathcal{M}_{m \times n}$: the set of $m \times n$ real matrices.
- $\text{Col}(A)$ (Row($A$)): the set of columns (rows) of $A$.
- $\text{Col}_i(A)$ (Row$_i(A)$): the $i$-th column (row) of $A$.
- $D_k := \{1, 2, 3, \ldots, k\}$.
- $\delta_n^i$: the $i$-th column of identity matrix $I_n$.
- $\Delta_n := \{\delta_n^1, \delta_n^2, \ldots, \delta_n^n\}$.
- $[A]_{i,j} := \text{Row}_i(\text{Col}_j(A))$.
- $L_{m \times n}$: the set of $m \times n$ logical matrices, that is, $\text{Col}(L) \in \Delta_m$.
- $B_{m \times n}$: the set of $m \times n$ Boolean matrices, that is, $[B]_{i,j} \in \mathcal{D} := \{0, 1\}$.
- $\delta_{m}[i_1, i_2, \ldots, i_n] := [\delta_{m}^{i_1}, \delta_{m}^{i_2}, \ldots, \delta_{m}^{i_n}] \in L_{m \times n}$.
- $I_n := [1, 1, \ldots, 1]^T$.
- $\land, \lor, \neg$: the conjunction, disjunction, and negation operators.
- $A \oplus B$: the Boolean addition of $A, B \in B_{m \times n}$ that is, $[A \oplus B]_{i,j} = [A]_{i,j} \lor [B]_{i,j}$.
- $A \otimes B$: the Boolean product of $A \in B_{m \times n}, B \in B_{n \times p}$, and $[A \otimes B]_{i,j} = 0$ if $[AB]_{i,j} = 0$, $[A \otimes B]_{i,j} = 1$ if $[AB]_{i,j} > 0$.
- $A \otimes B$: the Kronecker product of $A$ and $B$.
- $A \ast B$: the Khatri-Rao product of $A \in M_{m \times n}$ and $B \in M_{q \times n}$, that is $i = 1, 2, \ldots, n$, $\text{Col}_i(A \ast B) = \text{Col}_i(A) \otimes \text{Col}_i(B)$.
- $A \ast B := [A \ast B]_{i,j} = [A]_{i,j} \otimes [B]_{i,j}$.
- $W_{m,n} = [I_n \otimes \delta_{m}^1, I_n \otimes \delta_{m}^2, \ldots, I_n \otimes \delta_{m}^n]$; the swap matrix, that is, for $x \in \Delta_m, y \in \Delta_n$, $W_{m,n}x \otimes y = y \otimes x$.
- $\Phi_n := \delta_n^11, n + 2, 2n + 3, \ldots, (n - 2)n + (n - 1), n^2$ is the power-reducing matrix. It follows that $\forall x \in \Delta_n$, $\Phi_n x = x^2$.

- $|S|$; the cardinality of a set $S$.
- $[a, b] := \{a, a + 1, \ldots, b\}$, where $a, b \in \mathbb{Z}, a < b$.
- $\text{Im}(A)$: the image of a matrix $A$.

The main mathematical tool used in this paper is the STP of matrices, denoted by “$\ast$”, which is omitted if there is no confusion. For details, please refer to Appendix.

## 2 STP-Based Mergence

We consider linear discrete-time switched systems where the switching signals are generated by logic dynamical systems. The following equations depict the model:

$$\begin{align*}
x(t + 1) &= A_{\sigma(t)} x(t) + B_{\sigma(t)} u(t), \\
y(t) &= C_{\sigma(t)} x(t),
\end{align*}$$

(1)

$$\begin{align*}
\theta_1(t + 1) &= f_1(\theta_1(t), \ldots, \theta_k(t); \gamma_1(t), \ldots, \gamma_l(t)), \\
\theta_2(t + 1) &= f_2(\theta_1(t), \ldots, \theta_k(t); \gamma_1(t), \ldots, \gamma_l(t)), \\
&\vdots \\
\theta_k(t + 1) &= f_k(\theta_1(t), \ldots, \theta_k(t); \gamma_1(t), \ldots, \gamma_l(t)), \\
\sigma(t) &= h(\theta_1(t), \ldots, \theta_k(t); \gamma_1(t), \ldots, \gamma_l(t)),
\end{align*}$$

(2)

where $x(t) \in \mathbb{R}^n, u(t) \in \mathbb{R}^m, y(t) \in \mathbb{R}^p$ are the state, input, and output, respectively; $\sigma(t) \in [1, q]$ is the switching signal; $(A_i, B_i, C_i), i \in [1, q]$ are the subsystems, also known as the modes, of the discrete-time SLS (1); (2) is a (mixed-value) logical control network with $\theta(t) \in \Delta_N, i \in [1, k]$ being the logical states, $\gamma_j(t) \in \Delta_{M_j}, j \in [1, l]$ being the logical inputs and $\sigma(t) \in \Delta_q$ being the switching signal. $f_i : \prod_{i=1}^{k} \Delta_{N_i} \times \prod_{j=1}^{l} \Delta_{M_j} \rightarrow \Delta_{N_i}, i \in [1, k], j \in [1, l], \quad h : \prod_{i=1}^{k} \Delta_{N_i} \times \prod_{j=1}^{l} \Delta_{M_j} \rightarrow \Delta_q, i \in [1, k], j \in [1, l]$ are logical functions.

The ASSR of the logical control network (2) can be obtained by resorting to the STP approach (please refer to Appendix for the details on the transformation process between the algebraic and vector forms of the logical variables) as follows:

$$\begin{align*}
\tilde{\theta}(t + 1) &= L \times \tilde{\gamma}(t) \times \tilde{\theta}(t), \\
\tilde{\sigma}(t) &= R \times \tilde{\gamma}(t) \times \tilde{\theta}(t),
\end{align*}$$

(3)

where $\tilde{\theta}(t) \in \Delta_N, N := \prod_{i=1}^{k} N_i, \tilde{\gamma}(t) \in \Delta_M, M := \prod_{j=1}^{l} N_j, \tilde{\sigma}(t) \in \Delta_q$ are the overall logical state, overall
logical input, and switching signal in vector forms; \( L \in \mathcal{L}_{N \times MN} \) and \( R \in \mathcal{L}_{N \times MN} \) are the structure matrix and signal-generating matrix of (3). \( L \) is often written as \([L_1, L_2, \cdots, L_M]\), where \( L_i \in \mathcal{L}_{N \times N} \).

Using the STP approach, equation (1) can be rewritten as

\[
x(t+1) = A \otimes \delta(t) \otimes x(t) + B \otimes \delta(t) \otimes u(t),
\]

\[
y(t) = C \otimes \delta(t) \otimes x(t),
\]

where \( A := [A_1 \ A_2 \ \cdots \ A_q], \ B := [B_1 \ B_2 \ \cdots \ B_q], \) and \( C := [C_1 \ C_2 \ \cdots \ C_q] \).

Letting \( z(t) := \bar{\theta}(t) \otimes x(t) \in \mathbb{R}^{Nn} \), the STP-based merger of systems (4) and (3) is derived as follows [7]:

\[
z(t+1) = \bar{\theta}(t+1) \otimes x(t+1)
= L\gamma(t)\bar{\theta}(t)[A\delta(x(t) + B\delta(t)u(t))]
= L\gamma(t)\bar{\theta}(t)A\gamma(t)\bar{\theta}(t)x(t)
+ L\gamma(t)\bar{\theta}(t)B\gamma(t)\bar{\theta}(t)u(t)
= G\gamma(t)z(t) + H\gamma(t)\bar{\theta}(t)u(t),
\]

where \( G := L[I_{MN} \otimes (AR)]\Phi_{MN} \in \mathcal{M}_{Nn \times Nn}, \ H := L[I_{MN} \otimes (BR)]\Phi_{MN} \in \mathcal{M}_{Nn \times Nn}. \)

Since \( \gamma(t) \in \Delta_M \), based on the properties of the STP, the merged system (5) can be rewritten as:

\[
z(t+1) = [G_1 \ G_2 \ \cdots \ G_M]\gamma(t)z(t)
+ [H_1 \ H_2 \ \cdots \ H_M]\gamma(t)\bar{\theta}(t)u(t),
\]

where

\[
G_i = \begin{bmatrix}
G_{1,1}^i & G_{1,2}^i & \cdots & G_{1,N}^i \\
G_{2,1}^i & G_{2,2}^i & \cdots & G_{2,N}^i \\
\vdots & \vdots & \ddots & \vdots \\
G_{N,1}^i & G_{N,2}^i & \cdots & G_{N,N}^i
\end{bmatrix},
\]

and

\[
H_i = \begin{bmatrix}
H_{1,1}^i & H_{1,2}^i & \cdots & H_{1,N}^i \\
H_{2,1}^i & H_{2,2}^i & \cdots & H_{2,N}^i \\
\vdots & \vdots & \ddots & \vdots \\
H_{N,1}^i & H_{N,2}^i & \cdots & H_{N,N}^i
\end{bmatrix},
\]

each submatrix \( G_{\alpha,\beta}^i \in \mathcal{M}_{nxn} \) and \( H_{\alpha,\beta}^i \in \mathcal{M}_{nxn} \), \( \alpha, \beta \in [1, N] \). We call the above matrices the block form of \( G_i \) and \( H_i, \ i = 1, \cdots, M \).

Using the merged system (6), we formally eliminated the constraint that the switching signals \( \sigma(t) \) must be produced by the logical control network (3). One can see that the logical inputs \( \gamma(t) \), which can be selected arbitrarily, are the “switching signals” of the system (6), and the original switching signals \( \sigma(t) \) are implicit at present.

**Remark 1** In the subsequent sections, the logical state and input variables \( \theta \) and \( \gamma \) appear as the overall variables unless otherwise specified. For example, \( (\gamma_1, \gamma_2, \cdots, \gamma_T) \) represents a logical input sequence but not a series of logical input nodes.

### 3 Main Results

#### 3.1 Reachability Problem

**Definition 2** Consider the switched linear system (1) in which the switching signal is generated by the logical control network (3).

(1) A state \( x \in \mathbb{R}^n \) is reachable, if there exists a positive integer \( T < \infty \), a logical input sequence \( (\gamma_0, \gamma_1, \cdots, \gamma_{T-1}) \), and an input sequence \( (u_0, u_1, \cdots, u_{T-1}) \), such that for \( \forall \theta_0 \in \Delta_N \),

\[
x_0 = 0, \quad x_T = x.
\]

(2) The system is reachable if all states in \( \mathbb{R}^n \) are reachable.

**Definition 3** Consider the merged system (6). Define the reachable set of state \( x = 0 \) with \( T \)-length logical input sequence \( (\gamma_0, \gamma_1, \cdots, \gamma_{T-1}) \) and initial logical state \( \alpha \in [1, N] \) as

\[
\mathcal{R}_T^\alpha(\gamma_0, \gamma_1, \cdots, \gamma_{T-1}) :=
\begin{align*}
&\mathbb{1}_N^T \left[ \text{Im}(G_{\gamma_{T-1}}G_{\gamma_{T-2}} \cdots G_{\gamma_1}H_{\gamma_0} \delta_N^0) \right] \cup \\
&\mathbb{1}_N^T \left[ \text{Im}(G_{\gamma_{T-1}}G_{\gamma_{T-2}} \cdots G_{\gamma_1}H_{\gamma_0} \delta_N^0) \right] \cup \\
&\vdots \\
&\mathbb{1}_N^T \left[ \text{Im}(H_{\gamma_{T-1}}L_{\gamma_{T-2}} \cdots L_{\gamma_1}L_{\gamma_0} \delta_N^0) \right] \\
&\mathbb{1}_N^T \left[ \text{Im}(H_{\gamma_{T-1}}L_{\gamma_{T-2}} \cdots L_{\gamma_1}L_{\gamma_0} \delta_N^0) \right].
\end{align*}
\]

Now we are ready for the following result.

**Theorem 4** The switched linear system (1) is reachable under the logically generated switching signal (3), if and only if there exists a logical input sequence \( (\gamma_0, \gamma_1, \cdots, \gamma_{T-1}) \), such that the reachable set of the
merged system (6) satisfies

$$\bigcap_{\alpha=1}^{N} \mathcal{R}_T^\alpha(\gamma_0, \gamma_1 \cdots, \gamma_{T-1}) = \mathbb{R}^n. \quad (8)$$

**Proof:** Before proving Theorem 4, we first have a closer look into the structures of \( \mathbf{G} \) and \( \mathbf{H} \).

From equation (5), one has

\[
\mathbf{G} = L \begin{bmatrix}
\mathbf{AR} & \cdots & \mathbf{AR} \\
\vdots & \ddots & \vdots \\
\mathbf{AR} & \cdots & \mathbf{AR}
\end{bmatrix} \begin{bmatrix}
\delta_{(MN)^2}^1 \\
\vdots \\
\delta_{(MN)^2}^1
\end{bmatrix} = L A_1 \delta_{(MN)}^1 = L A_1^{\delta_{(MN)}^1} = \begin{bmatrix}
\text{Col}_1(L) A_{\sigma_1} & \cdots & \text{Col}_M(L) A_{\sigma_M}
\end{bmatrix}.
\]

where \( A_\sigma := A_{\sigma | \sigma = \text{Col}_1(L)} \).

Then it is straightforward that

\[
\mathbf{G}_1 = \begin{bmatrix}
\text{Col}_1(L) A_{\sigma_1} & \cdots & \text{Col}_N(L) A_{\sigma_N}
\end{bmatrix},
\]

\[
\mathbf{G}_2 = \begin{bmatrix}
\text{Col}_{N+1}(L) A_{\sigma_{N+1}} & \cdots & \text{Col}_2(L) A_{\sigma_2}
\end{bmatrix},
\]

\[
\vdots
\]

\[
\mathbf{G}_M = \begin{bmatrix}
\text{Col}_{(M-1)N+1}(L) A_{\sigma_{(M-1)N+1}} & \cdots & \text{Col}_N(L) A_{\sigma_N}
\end{bmatrix}.
\]

Since \( L \) is a logical matrix, \( \text{Col}(L) \subset \Delta_N \), in the block form of \( \mathbf{G}_i \), there is only one nonzero block in each column. Furthermore, when we compress each nonzero block into 1, zero block into 0, and denote the compressed matrix by \( \tilde{G}_i \), then \( \tilde{G}_i = L_i \) and consequently, \( \mathbf{G} = L \). It is obvious that \( \mathbf{H} \) also has the above properties. Now we are ready for the proof.

From the structure of \( \mathbf{G} \) and \( \mathbf{H} \), we know that \( G_{\gamma_{T-1}} G_{\gamma_{T-2}} \cdots G_{\gamma_1} H_{\gamma_0} \) also has the block form where each column has only one nonzero block, so do the other matrices in similar forms on the right side of equation (7).

We first analyse the term

\[
1^T_N \left[ \text{Im}(G_{\gamma_{T-1}} G_{\gamma_{T-2}} \cdots G_{\gamma_1} H_{\gamma_0} \delta_N) \right]
\]

in equation (7). In the \( \alpha \)-th column of the block form of \( G_{\gamma_{T-1}} G_{\gamma_{T-2}} \cdots G_{\gamma_1} H_{\gamma_0} \delta_N \), \( \alpha \in [1, N] \), the nonzero block has the following form:

\[
G_{\gamma_{T-1}}^{\alpha T} G_{\gamma_{T-2}}^{\alpha T} \cdots G_{\gamma_1}^{\alpha T} H_{\gamma_0}^{\alpha T} = A_{\sigma_{T-1}} A_{\sigma_{T-2}} \cdots A_{\sigma_1} B_{\sigma_0},
\]

where \( (\gamma_0, \gamma_1, \ldots, \gamma_{T-1}) \) is the logical input sequence, \( (\alpha, \beta, \kappa, \ldots, \xi, \epsilon, v) \) and \( (\delta_0, \delta_1, \ldots, \delta_{T-1}) \) are the corresponding logical state trajectory and switching signal trajectory, respectively (one should notice that the length of the logical trajectory is \( T + 1 \)). To be precise, \( \sigma_{T-1} = \sigma_N^{(\gamma_{T-2}+1)+\epsilon} \sigma_{T-2} = \sigma_N^{(\gamma_{T-1}+1)+\xi} \cdots, \delta_0 = \sigma_N^{(\gamma_0-1)+\alpha} \). Thus,

\[
\text{Im}(G_{\gamma_{T-1}} G_{\gamma_{T-2}} \cdots G_{\gamma_1} H_{\gamma_0} \delta_N) = \text{Im}(\delta_0^N A_{\sigma_T} A_{\sigma_{T-1}} \cdots A_{\sigma_1} B_{\sigma_0}) \subset \{ \delta_N^N \} \times \mathbb{R}^n.
\]

It is obvious that

\[
1^T_N \left[ \text{Im}(G_{\gamma_{T-1}} G_{\gamma_{T-2}} \cdots G_{\gamma_1} H_{\gamma_0} \delta_N) \right] = \text{Im}(A_{\sigma_{T-1}} A_{\sigma_{T-2}} \cdots A_{\sigma_1} B_{\sigma_0}).
\]

The other terms in equation (7) have similar results. Then it means that with the initial logical state \( \alpha \), there is a switching signal trajectory \( (\sigma_0, \sigma_1, \ldots, \sigma_{T-1}) \), such that

\[
\text{Im}(A_{\sigma_{T-1}} A_{\sigma_{T-2}} \cdots A_{\sigma_1} B_{\sigma_0}) \cup \text{Im}(A_{\sigma_{T-1}} A_{\sigma_{T-2}} \cdots A_{\sigma_1} B_{\sigma_0}) \cup \cdots \cup \text{Im}(A_{\sigma_{T-1}} B_{\sigma_{T-2}}) \cup \text{Im}(B_{\sigma_{T-1}}) = \mathbb{R}^n,
\]

which means that starting from \( x(0) = 0 \) and \( \delta_0 = \delta_N^N \), with certain input sequence \( (u_0, u_1, \ldots, u_{T-1}) \),

\[
x(T) = A_{\sigma_{T-1}} A_{\sigma_{T-2}} \cdots A_{\sigma_1} B_{\sigma_0} u_0 + \cdots + A_{\sigma_{T-1}} B_{\sigma_1} u_{T-1}
\]

can reach anywhere in \( \mathbb{R}^n \).

The above analysis is based on the initial logical state \( \alpha \). To eliminate this constraint, \( \alpha \) should be any possible value. Otherwise, the logical input sequence \( (\gamma_0, \gamma_1, \ldots, \gamma_{T-1}) \) is not feasible for some initial logical states such that the vector space \( \mathbb{R}^n \) cannot be spanned by the corresponding switching signal sequences. Now the proof is completed. \( \square \)

**Remark 5** In Theorem 4, one may not have to take all \( \alpha \in [1, N] \) into the computation. If there is a \( \beta \in [1, N] \) such that equation (8) holds, then one does not have to check the states that can be controlled to \( \beta \), because, for these states, one can first drive them to \( \beta \) and then
solve the problem. To be precise, the number of the to-be-checked states is the number of the disjoint control attractors (i.e., the attractors whose attract basins are disjoint) of the logical system (3).

It should be pointed out that Theorem 4 in its present form can hardly serve as an easily verifiable criterion for controllability, because one may find it difficult to check the existence of the logical input sequences required by (2). Thus, in the following, we provide an algorithm to overcome such difficulty.

By the proof of Theorem 4 and Remark 5, the following algorithm gives the feasible logical input sequences.

Algorithm 1 Computing the feasible logical input sequences.

Step 1: Set $k := 1$, go to Step 2.
Step 2: Compute

$$G_k := \left( \sum_{i=1}^{M} G_i \right)^k,$$

then go to Step 3.

%here is the symbolic computation on the block form

Step 3: Compute $G_k$, where $G_k$ is the $k$-th column of $G(k)$ is nonzero):

$$G_{v,\alpha}^k G_{v,\xi}^{k-1} \cdots G_{\beta,\alpha}^0 + G_{v,\alpha}^{k-1} G_{v,\xi}^{k-2} \cdots G_{\beta,\alpha}^0 + \cdots.$$

Go to Step 4.

Step 4: Take each alternative logical input sequence $(\gamma_0^j, \gamma_1^j, \cdots, \gamma_{k-1}^j)$ and its corresponding logical state trajectory $(\alpha, \beta^j, \cdots, \xi^j, \gamma^j, v^j)$ into equation (8).

If (8) holds for all the initial logical states which are control attractors (see Definition 31 of Appendix, and only one logical state in a control cycle needs to be checked), then $(\gamma_0^j, \cdots, \gamma_{k-1}^j)$ is the desirable logical input sequence, stop. Otherwise, set $k := k + 1$, and go to Step 2.

Remark 6 In Algorithm 1, an alternative logical input sequence $(\gamma_0, \gamma_1, \cdots, \gamma_{T-1})$ only needs to be checked for a few control attractors whose attract basins compose the whole state space. Because for the other states, the corresponding logical input sequences can be obtained by adding the segments $(\gamma_{-1}, \gamma_{-1+1}, \cdots, \gamma_{-1})$, which can drive them to the control attractors, to the left side of the checked logical input sequence.

Remark 7 From the proof of Theorem 4, we can see that the criterion (8) for the reachability of the merged system (6) is equivalent to the Kalman-type rank condition for the reachability of the system (1), that is, the system is reachable, if and only if there exists a switching signal sequence $(\sigma_0, \sigma_1, \cdots, \sigma_{T-1})$ generated by the system (3), such that

$$\text{rank}[B_{\sigma_{T-1}}, A_{\sigma_{T-1}}, B_{\sigma_{T-2}}, \cdots, A_{\sigma_{T-1}} A_{\sigma_0}] = n.$$

But one should notice that without the proposed approach, the Kalman-type rank condition cannot be applied to the studied hybrid systems because the system (6) which contains both physical and logical states, is not a linear system. Besides, one cannot guarantee whether the switching signal sequence $(\sigma_0, \sigma_1, \sigma_{T-1})$ can be generated by the logical control network. Hence, the Kalman-type rank condition is not feasible for solving the problems considered in this paper.

3.2 Controllability Problem

Definition 8 Consider the switched linear system (1) in which the switching signal is generated by the logical control network (3).

(1) A state $x \in \mathbb{R}^n$ is controllable, if there exist a positive integer $T < \infty$, a logical input sequence $(\gamma_0, \gamma_1, \cdots, \gamma_T)$, and an input sequence $(u_0, u_1, \cdots, u_T)$, such that for $\forall \theta_0 \in \Delta_N$,

$$x_0 = x, \quad x_T = 0.$$

(2) The system is controllable if all the states in $\mathbb{R}^n$ are controllable.

Theorem 9 The switched linear system (1) is controllable under the logically generated switching signal, if and only if there exists a logical input sequence $(\gamma_0, \gamma_1, \cdots, \gamma_T)$, $T < \infty$, such that starting from any logical state $\alpha$ in $[1, N]$, the merged system (6) satisfies

$$1^T_N [\text{Im}(G_{\gamma_{T-1}} G_{\gamma_{T-2}} \cdots G_{\gamma_0})] \subset \mathbb{R}^n_{\gamma}(\gamma_0, \gamma_1 \cdots, \gamma_{T-1}).$$

Proof: By equation (6), if the system is controllable, then there exists $T < \infty$ such that the following equation holds:

$$z(T) = G_{\gamma_{T-1}} \cdots G_{\gamma_0} z(0) + G_{\gamma_{T-1}} \cdots G_{\gamma_1} H_{\gamma_0} \hat{\theta}(0) u(0) + G_{\gamma_{T-1}} \cdots G_{\gamma_2} H_{\gamma_1} \hat{\theta}(1) u(1) + \cdots + G_{\gamma_{T-1}} H_{\gamma_{T-2}} \hat{\theta}(T-2) u(T-2) + H_{\gamma_{T-1}} \hat{\theta}(T-1) u(T-1) = 0.$$
Then for some initial logical state denoted by \(\delta_N^\alpha\), one has
\[
G_{\tau T - 1} \cdots G_{\gamma_0} \delta_N^\alpha x(0) = -(G_{\tau T - 1} \cdots H_{\gamma_0} \delta_N^\alpha u(0) + \cdots \\
+ G_{\tau T - 1} H_{\tau T - 2} \cdots L_{\tau T - 3} \cdots L_{\gamma_0} \delta_N^\alpha u(T - 2) \\
+ H_{\tau T - 1} L_{\tau T - 2} \cdots L_{\gamma_0} \delta_N^\alpha u(T - 1)).
\]

According to the proof of Theorem 4, the term
\[
G_{\tau T - 1} \cdots G_{\gamma_0} \delta_N^\alpha
\]
has only one nonzero block. Without loss of generality, we assume that it is the \((\nu, \alpha)\)-th block:
\[
G_{\tau T - 1} \cdots G_{\gamma_0} \alpha \beta \gamma
\]
Then starting with logical state \(\alpha\), the controllability is guaranteed if and only if for all \(x_0 \in \mathbb{R}^n\),
\[
(G_{\nu, \alpha} G_{\tau T - 2} \cdots G_{\gamma_1} G_{\beta, \alpha}^T)x_0 \in \mathcal{R}^n(\gamma_0, \gamma_1, \cdots, \gamma_{T - 1}),
\]
which coincides with (9). Similar with the argument in the proof of Theorem 4, equation (9) should be valid on all \(\alpha \in [1, N]\).

**Remark 10** (1) When checking if equation (9) holds for all \(\alpha \in [1, N]\), one can also simplify the computation using Remark 5.
(2) It is obvious that when the system (1) is reversible, i.e., \(A_i\) is non-singular for all \(i \in [1, q]\), Theorems 4 and 9 are equivalent.

**Remark 11** We may borrow the result in [8] to obtain the upper bound of \(T\) in Theorems 4 and 9, that is, \(T \leq n\). This upper bound is also feasible for the results in the subsequent subsection.

### 3.3 Observability and Reconstructibility Problems

**Definition 12** Consider the switched linear system (1) where the switching signal is generated by the logical control network (3). The system is observable (reconstructible), if there exists a positive integer \(T < \infty\) and a logical input sequence \((\gamma_0, \gamma_1, \cdots, \gamma_{T - 1})\), such that the input sequence \((u_0, u_1, \cdots, u_{T - 1})\) and output trajectory \((y_0, y_1, \cdots, y_T)\) can uniquely determine the initial state \(x_0\) (the current state \(x_T\)), regardless of the value of the initial logical state \(\theta_0\).

Now we build a dual system as
\[
\ddot{x}(t + 1) = \tilde{A} \times \dot{x}(t) + \tilde{C} \times \dot{u}(t),
\]
where \(\tilde{x} \in \mathbb{R}^n\), \(\tilde{u} \in \mathbb{R}^p\), \(\tilde{A} = [\tilde{A}_1 \tilde{A}_2 \cdots \tilde{A}_q] := [A_1^T \ A_2^T \cdots A_q^T], \tilde{C} = [\tilde{C}_1 \tilde{C}_2 \cdots \tilde{C}_q] := [C_1^T \ C_2^T \cdots C_q^T],
\]

The logical control network remains the same as (3).

Similar with the construction of system (5), we build a merged system using systems (10) and (3):
\[
\ddot{z}(t + 1) = \tilde{g}(t + 1) \ddot{z}(t + 1) \\
= L_{\gamma}(t)\tilde{b}(t) [\tilde{A} \tilde{C}(t) \dot{z}(t) + \tilde{C} \tilde{C}(t) \dot{u}(t)] \\
= L_{\gamma}(t)\tilde{b}(t) [\tilde{A} \tilde{C}(t) \dot{z}(t) + \tilde{C} \tilde{C}(t) \dot{u}(t)] \\
= L_{\gamma}(t)\tilde{b}(t) [\tilde{A} \tilde{C}(t) \dot{z}(t) + \tilde{C} \tilde{C}(t) \dot{u}(t)] \\
= \tilde{G}_{\gamma}(t) \ddot{z}(t) + \tilde{H}_{\gamma}(t)\tilde{b}(t)\dot{u}(t),
\]
where
\[
\tilde{G} := L_{\gamma}(t) \otimes (\tilde{A} \tilde{C}) \in \mathcal{M}_{nN \times nMN}, \tilde{H} := L_{\gamma}(t) \otimes (\tilde{C} \tilde{C}) \in \mathcal{M}_{nN \times nMN},
\]

System (11) can also be rewritten as
\[
\ddot{z}(t + 1) = [\tilde{G}_1 \tilde{G}_2 \cdots \tilde{G}_n] \tilde{G}(t) \ddot{z}(t) \\
+ [\tilde{H}_1 \tilde{H}_2 \cdots \tilde{H}_M] \tilde{H}(t)\dot{u}(t),
\]

where
\[
\tilde{G}_1 = \begin{bmatrix} \tilde{G}_1 \ 1 \ 1 \ \cdots \ \tilde{G}_1 \ n \ 1 \\ \tilde{G}_1 \ 2 \ \tilde{G}_2 \ 2 \ \cdots \ \tilde{G}_2 \ n \ 2 \\ \vdots \ \vdots \ \cdots \ \vdots \ \vdots \\ \tilde{G}_1 \ 1 \ n \ \tilde{G}_2 \ n \ \cdots \ \tilde{G}_n \ n \ n \end{bmatrix}
\]
and
\[
\tilde{H}_1 = \begin{bmatrix} \tilde{H}_1 \ 1 \ 1 \ \cdots \ \tilde{H}_1 \ 1 \ n \ 1 \\ \tilde{H}_1 \ 2 \ \tilde{H}_2 \ 2 \ \cdots \ \tilde{H}_2 \ n \ 2 \\ \vdots \ \vdots \ \cdots \ \vdots \ \vdots \\ \tilde{H}_1 \ 1 \ n \ \tilde{H}_2 \ n \ \cdots \ \tilde{H}_n \ n \ n \end{bmatrix}
\]
with each submatrix \(\tilde{G}_{\alpha, \beta}  \in \mathcal{M}_{nN \times nN}\) and \(\tilde{H}_{\alpha, \beta}  \in \mathcal{M}_{nN \times p}, \alpha, \beta \in [1, N]\). We call the above matrices the block form of \(\tilde{G}_i\) and \(\tilde{H}_i, i = 1, \cdots, M\).

**Definition 13** Consider the merged system (11). Define the reachable set of state \(\tilde{z}\) with \(T\)-length logical input sequence \((\gamma_0, \gamma_1, \cdots, \gamma_{T - 1})\) and initial logical state \(\alpha \in [1, N]\).
[1, N] as
\[
\tilde{\mathcal{R}}_T^\alpha(\gamma_0, \gamma_1 \cdots, \gamma_{T-1}) := \\
1_N^T \left[ \text{Im}\left( \tilde{G} \gamma_0 \tilde{G} \gamma_1 \cdots \tilde{G} \gamma_{T-1} \tilde{L}_0 \tilde{L}_{T-2} \cdots \tilde{L}_{n_0} \tilde{N}_0 \right) \right] \cup \\
1_N^T \left[ \text{Im}\left( \tilde{G} \gamma_0 \tilde{G} \gamma_1 \cdots \tilde{G} \gamma_{T-2} \tilde{L}_n \tilde{L}_{T-3} \cdots \tilde{L}_{n_0} \tilde{N}_0 \right) \right] \cup \\
\vdots \cup 1_N^T \left[ \text{Im}\left( \tilde{G} \gamma_0 \tilde{H} \gamma_1 L_0 \delta_N \right) \right] \\
\cup 1_N^T \left[ \text{Im}\left( \tilde{H} \gamma_0 \delta_N \right) \right].
\]
(13)

By the duality principle, the following theorem is obtained.

**Theorem 14** The switched linear system (1) is observable under the logically generated switching signal, if and only if there exists a logical input sequence \((\gamma_0, \gamma_1, \cdots, \gamma_{T-1})\), such that the reachable set of the merged system (11) satisfies
\[
\bigcap_{\alpha=1}^N \tilde{\mathcal{R}}_T^\alpha(\gamma_0, \gamma_1 \cdots, \gamma_{T-1}) = \mathbb{R}^n.
\]
(14)

**Proof**: Using the proof of Theorem 4, one can conclude that criterion (14) is equivalent to that for the system (10), there exists a switching signal sequence \((\sigma_0, \sigma_1, \cdots, \sigma_{T-1})\), which is generated by the system (3) with initial state \(\alpha\), such that
\[
\text{Im}\left( \tilde{A}_{\sigma_0} \tilde{A}_{\sigma_1} \cdots \tilde{A}_{\sigma_{T-1}} \tilde{C}_{\sigma_{T-1}} \right) \cup \\
\text{Im}\left( \tilde{A}_{\sigma_0} \tilde{A}_{\sigma_1} \cdots \tilde{A}_{\sigma_{T-2}} \tilde{C}_{\sigma_{T-2}} \right) \cup \\
\vdots \cup \text{Im}\left( \tilde{A}_{\sigma_0} \tilde{C}_{\gamma_1} \right) \cup \text{Im}\left( \tilde{C}_{\sigma_0} \right) = \mathbb{R}^n,
\]
which implies that
\[
\text{rank}\left( \begin{array}{c}
C_{\sigma_0} \\
C_{\sigma_1} A_{\sigma_0} \\
\vdots \\
C_{\sigma_{T-2}} A_{\sigma_{T-3}} \cdots A_{\sigma_0} \\
C_{\sigma_{T-1}} A_{\sigma_{T-2}} \cdots A_{\sigma_0}
\end{array} \right) = n.
\]

From the relationship between reachability and controllability of the switched linear systems, we have the following results resorting to the duality principle.

**Theorem 15** The switched linear system (1) is reconstructable under the logically generated switching signal, if and only if there exists a logical input sequence \((\gamma_0, \gamma_1, \cdots, \gamma_{T-1})\), \(T < \infty\), such that staring from any logical state \(\alpha \in [1, N]\), the merged system (12) satisfies
\[
1_N^T \left[ \text{Im}\left( \tilde{G} \gamma_0 \tilde{G} \gamma_1 \cdots \tilde{G} \gamma_{T-1} \tilde{N}_0 \right) \right] \subset \tilde{\mathcal{R}}_T^\alpha(\gamma_0, \gamma_1 \cdots, \gamma_{T-1}).
\]
(15)

**Remark 16** Similar with the argument in Remark 10, for the merged system (6) whose linear subsystem (1) is reversible, Theorems 14 and 15 are equivalent.

## 4 System Realization Problem

In the previous section, we investigated four fundamental control properties of discrete-time SLSs where the switching signals are generated by logical control systems. Now it is natural to ponder the following problem: under what condition(s) can the logical system produce a desirable sequence such that the linear system’s performance reaches our goal?

A straightforward result is as follows.

**Proposition 17** Consider the logical control network (3). If each state \(\theta \in \mathcal{D}_N\) is one-step controllable from all the states, which in the vector form is
\[
[L_{1_M}]_{\alpha, \beta} > 0, \quad \forall \alpha, \beta \in [1, N],
\]
then the four properties of the switched linear system (1) with constrained switching signals are reduced to the unconstrained cases.

One should notice that the condition (16) is rather strict for a logical control network. In the following, we will probe some feasible conditions.

We consider two kinds of logical regulating methods:

- **Case 1**: Generating the switching signal sequences that guarantee the fixed operating times (FOTs) for the subsystems.
- **Case 2**: Generating the switching signals aligned with a finite reference sequence.

### 4.1 \(\ell\)-Step Input-State Set Reachability

In this subsection, we introduce the \(\ell\)-step input-state set reachability of logical control networks, which is used hereafter.
Consider the logical control network (2) and its ASSR (3). Denote the input set by $\mathcal{U} := \{1, 2, \ldots, M\}$ and the state set by $\mathcal{X} := \{1, 2, \ldots, N\}$, then $\Omega \in \mathcal{2}^{\mathcal{U} \times \mathcal{X}} \setminus \{\emptyset\}$ is an input-state subset. Now we denote $V(\Omega) \in \mathcal{B}_{MN \times 1}$ the index vector of $\Omega$, which is defined as

$$[V(\Omega)]_i := \begin{cases} 1, & i \in \Omega; \\ 0, & i \notin \Omega. \end{cases}$$

One can see that $V(\Omega) = \sum_{(\gamma, \theta) \in \Omega} \tilde{\vartheta}$.

For a class of initial state subsets $\Omega^0 := \{\Omega^0_1, \Omega^0_2, \ldots, \Omega^0_n\}$ and a class of terminal state subsets $\Omega^d := \{\Omega^d_1, \Omega^d_2, \ldots, \Omega^d_n\}$ ($\alpha, \beta \in \mathbb{Z}_+$ are the numbers of the subsets), define their index matrices as

$$P^0_{\Omega} := \left[ V(\Omega^0_1) V(\Omega^0_2) \cdots V(\Omega^0_n) \right] \in \mathcal{B}_{MN \times \alpha},$$

$$P^d_{\Omega} := \left[ V(\Omega^d_1) V(\Omega^d_2) \cdots V(\Omega^d_n) \right] \in \mathcal{B}_{MN \times \beta}.$$

Now we are ready to give the concept of input-state set reachability of logical control networks.

**Definition 18** Consider the logical control network (3) with a class of initial state subsets $\Omega^0 = \{\Omega^0_1, \Omega^0_2, \ldots, \Omega^0_n\}$ and a class of terminal state subsets $\Omega^d = \{\Omega^d_1, \Omega^d_2, \ldots, \Omega^d_n\}$.

1. The system is $\ell$-step input-state reachable from $(\gamma^0, \theta^0)$ to $(\gamma^d, \theta^d)$ if, there exists at least a logical input sequence $$(\gamma(0), \gamma(1), \ldots, \gamma(\ell)),$$ where $\gamma(0) = \gamma^0$ and $\gamma(\ell) = \gamma^d$, such that $(\gamma^0, \theta^0)$ can be steered to $(\gamma^d, \theta^d)$.
2. The system is $\ell$-step input-state reachable from $\Omega^0_j$ to $\Omega^d_i$ if, for some $(\gamma^0, \theta^0) \in \Omega^0_j$ and some $(\gamma^d, \theta^d) \in \Omega^d_i$, there exists at least a logical input sequence $$(\gamma(0), \gamma(1), \ldots, \gamma(\ell)),$$ where $\gamma(0) = \gamma^0$ and $\gamma(\ell) = \gamma^d$, such that the system is reachable from $(\gamma^0, \theta^0)$ to $(\gamma^d, \theta^d)$.
3. The system is $\ell$-step input-state reachable at $\Omega^0_j$ if, the system is set reachable from $\Omega^0_j$ to $\forall \Omega^d_i \in \Omega^d$.
4. $\Omega^d_i$ is global $\ell$-step input-state set reachable if, the system is set reachable from $\forall \Omega^0_j \in \Omega^0$ to $\Omega^d_i$.
5. The system is $\ell$-step input-state set reachable from $\Omega^0_j$ to $\Omega^d_i$ if, for $\forall \Omega^0_j \in \Omega^0$ and $\forall \Omega^d_i \in \Omega^d$, the system is $\ell$-step input-state set reachable from $\Omega^0_j$ to $\Omega^d_i$.

Define the input-state matrix of the logical control network (3) as

$$L := 1_M L = \left[ L^T L^T \cdots L^T \right]^T. \quad (17)$$

Given $\Omega^0$ and $\Omega^d$, we have the $\ell$-step input-state set reachability matrix of the system (3) as

$$C_\ell := (P^0_{\Omega})^\ell \times B L^\ell \times B P^d_{\Omega}, \quad (18)$$

the $\ell$-step input-state set reachability can be verified by the following conditions.

**Proposition 19** Consider the logical control network (3) with a group of initial state subsets $\{\Omega^0_1, \Omega^0_2, \ldots, \Omega^0_n\}$ and terminal input-state subsets $\{\Omega^d_1, \Omega^d_2, \ldots, \Omega^d_n\}$.

1. The system is $\ell$-step input-state set reachable from $\Omega^0_1$ to $\Omega^d_1$, if and only if $|C_\ell|_{i,j} = 1$.
2. The system is $\ell$-step input-state set reachable at $\Omega^0_j$, if and only if $\operatorname{Col}_i(C_\ell) = \mathbf{1}_\alpha^T$.
3. $\Omega^d_i$ is global $\ell$-step input-state set reachable, if and only if $\operatorname{Row}_i(C_\ell) = \mathbf{0}^\ell$.
4. The system is $\ell$-step input-state set reachable, if and only if $C_\ell = \mathbf{1}_{\beta \times \alpha}$.

**Proof:** Given $\gamma(0) = \gamma^0$ and $\theta(0) = \theta^0$, one has

$$L \times B \tilde{\gamma}(0) \tilde{\theta}(0) = 1_M \times B L \tilde{\gamma}(0) \tilde{\theta}(0) = \sum_{i=1}^m \delta^*_M \tilde{\theta}(1) := \tilde{\vartheta}(1),$$

where $\tilde{\vartheta}(t)$ denotes the Boolean sum of all possible input-states $\tilde{\gamma}(t) \tilde{\theta}(t)$ at time $t$, starting from the initial input-state $\tilde{\gamma}(0) \tilde{\theta}(0)$. Then one has

$$L^{(t)} \times B \tilde{\gamma}(t) \tilde{\theta}(t) = L^{(t-1)} \times B \tilde{\vartheta}(1) = L^{(t-2)} \times B \tilde{\theta}(2) = \cdots = L \times B \tilde{\vartheta}(t) = \tilde{\vartheta}(t),$$

which deduces the following recursion

$$\tilde{\vartheta}(t + 1) = L \tilde{\vartheta}(t) \quad t \geq 1.$$
Then it can be easily concluded that
\[
\begin{pmatrix}
\gamma^d 
\end{pmatrix}^T L \begin{pmatrix}
\gamma(0) 
\end{pmatrix}^T \tilde{\theta}(l) = \begin{pmatrix}
1 
\end{pmatrix} \iff (\gamma^d, \theta^d) \text{ is reachable from } (\gamma^0, \theta^0);
\begin{pmatrix}
0 
\end{pmatrix} \iff (\gamma^d, \theta^d) \text{ is not reachable from } (\gamma^0, \theta^0).
\]

According to the structure of the index matrices, the criteria in Proposition 19 are proved. \hfill \Box

**Corollary 20** From the proof of Proposition 19, one sees easily that letting the Boolean product be the conventional product and then compute \( \tilde{C}_t \), i.e.,
\[
\tilde{C}_t := (P_{ \Omega_t}^d)^T \times L^t \times P_{ \Omega_t}^o,
\]
the results in Proposition 19 will be quantitative but not qualitative. That is,

1. The number of the \( \ell \)-length paths that from \( \Omega^d_t \) to \( \Omega^d_j \)
is \([\tilde{C}_t]_{i,j}\).

2. The system is \( \ell \)-step input-state set reachable if and only if \( \text{Col}_j(\tilde{C}_t) > 0 \), and each element of \( \text{Col}_j(\tilde{C}_t) > 0 \) represents the number of the \( \ell \)-length paths that end in the corresponding input-state sets.

3. \( \Omega^d_t \) is global \( \ell \)-step input-state set reachable if and only if \( \text{Row}_i(\tilde{C}_t) > 0 \), and each element of \( \text{Row}_i(\tilde{C}_t) > 0 \) represents the number of the \( \ell \)-length paths that start in the corresponding input-state sets.

4. The system is \( \ell \)-step input-state set reachable if and only if \( \tilde{C}_t > 0 \).

Using the structure matrix \( L \), one can draw the input-state dynamic graph of the logical control network (3). An illustrative example is given below to provide an intuitive understanding of input-state set reachability, where the logical control network was originally proposed in [55].

**Example 21** Consider a logical control network (A.4), where the structure matrix \( L = \delta_3[1 \ 1 \ 2 \ 4 \ 4 \ 4 \ 3 \ 3] \). Its input-state dynamic graph is shown in Fig. 2. From Fig. 2, we can observe all the transitions among the input-state variables.

To extract the set reachability, we should first assign the input-state subsets. For instance, let the three layers of nodes be partitioned into three input-state subsets:

\[
\Omega_1 := \{2 \times (1, 2), 1 \times (2, 2)\},
\Omega_2 := \{2 \times (2, 1), 2 \times (2, 2), 2 \times (1, 1)\},
\Omega_3 := \{1 \times (2, 1), 1 \times (1, 2), 1 \times (1, 1)\}.
\]

Then the index vectors are

\[
V(\Omega_1) = [0 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0]^T,
V(\Omega_2) = [0 \ 0 \ 0 \ 1 \ 0 \ 1 \ 1]^T,
V(\Omega_3) = [1 \ 1 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0]^T.
\]

Letting \( \Omega^d := \{\Omega_1, \Omega_2, \Omega_3\} \), we can obtain that

\[
\tilde{C}_1 = \begin{bmatrix} 2 \\ 0 \end{bmatrix}, \quad \tilde{C}_2 = \begin{bmatrix} 4 \\ 2 \end{bmatrix}.
\]

This result can be observed from Fig. 2 that the nodes on the uppermost layer have two 1-length paths that can reach the nodes on the middle layer: \( (2 \times (1, 2)) \rightarrow (2 \times (2, 2)), \ (1 \times (2, 2)) \rightarrow (2 \times (2, 2)) \), while the nodes on the middle layer have two 1-length paths to the nodes on the nethermost layer: \( (2 \times (2, 1)) \rightarrow (1 \times (2, 1)), \ (2 \times (2, 2)) \rightarrow (1 \times (2, 1)) \), but there is no 1-length path from the uppermost to the nethermost layer.

One can also find the 2-length paths from Fig. 2 and the number of the paths coincide with the corresponding elements of \( \tilde{C}_2 \):

1. **4 paths from the uppermost layer to the middle layer:**
   \( (2 \times (1, 2)) \rightarrow (1 \times (2, 2)) \rightarrow (2 \times (2, 2)), \ (2 \times (1, 2)) \rightarrow (2 \times (2, 2)) \rightarrow (2 \times (2, 1)), \ (1 \times (2, 2)) \rightarrow (2 \times (2, 1)), \ (1 \times (2, 2)) \rightarrow (1 \times (2, 2)) \rightarrow (2 \times (2, 2)) \);

2. **2 paths from the uppermost layer to the nethermost layer:**
   \( (2 \times (1, 2)) \rightarrow (2 \times (2, 2)) \rightarrow (1 \times (2, 1)), \ (1 \times (2, 2)) \rightarrow (2 \times (2, 2)) \rightarrow (1 \times (2, 1)) \).

### 4.2 Fixed Operating Time Switching

In Case 1, without loss of generality, assume that the FOTs of the corresponding subsystems are positive. Then we have the following conditions.

**Theorem 22** Consider system (1) in which the switching signal is generated by the system (3). Denote by \( d_1, d_2, \ldots, d_q \in \mathbb{Z}_+ \cup \{\infty\} \) the FOTs of the subsystems \( \Sigma_1, \Sigma_2, \ldots, \Sigma_q \). The switching signal sequences, which ensure the FOTs, can be generated by the system (3) under some logical inputs, no matter what the initial logical state is, if and only if
(1) For the subsystem $\Sigma_i$ whose FOT $d_i = 1$, there exists at least one logical input $\gamma \in [1, M]$, such that the switching signal $\sigma = i$ can be transferred to other values.

(2) For the subsystem $\Sigma_i$ whose FOT satisfies $1 < d_i < \infty$, there exists at least one logical input $\gamma \in [1, M]$, such that the switching signal $\sigma = i$ can be transferred to other values; and exists at least one logical input $\gamma \in [1, M]$, such that the switching signal $\sigma = i$ can keep still.

(3) For the subsystem $\Sigma_i$ whose FOT satisfies $d_i = \infty$, there exists at least one logical input $\gamma \in [1, M]$, such that the switching signal $\sigma = i$ can keep still.

Proof: The value of the FOT $d_i$ for the subsystem $\Sigma_i$ can be $d_i = 1$, $1 < d_i < \infty$, or $d_i = \infty$, and for an initial logical state, the initial switching signal must correspond to the subsystem according with one of the three situations.

- For the case of $d_i = 1$, once the system is started with $\Sigma_i$ at $t = 0$ (or switched to $\Sigma_i$ at time $t = \tau$), the subsystem $\Sigma_i$ should be transferred to the other subsystems immediately at time $t = 1$ (or $\tau + 1$) using a logical input $\gamma_1$ (or $\gamma_{\tau+1}$).

   If there is no such logical input, then it means that once the system is switched to subsystem $\Sigma_i$, the system will always run in this mode, which is forbidden by the FOT.

- For the case of $1 < d_i < \infty$, once the system is started with $\Sigma_i$ at $t = 0$ (or switched to $\Sigma_i$ at time $t = \tau$), the logical system (3) should have the ability to 1) let $\sigma = i$ stay if $t < d_i$ (or $t < \tau + d_i$), and 2) steer to the other values when $t = d_i$ (or $t = \tau + d_i$). Thus, there should exist at least two logical inputs, such that one can keep $\sigma = i$ still and the other can steer $\sigma$ to other values. Otherwise, the subsystem cannot reach or will exceed the FOT.

- For the case of $d_i = \infty$, which means that once the system is started with $\Sigma_i$ at $t = 0$ (or switched to subsystem $\Sigma_i$ at time $t = \tau$), it should operate in this mode at $t > 0$ (or $t > \tau$). Thus there should exist at least one logical input such that $\sigma = i$ holds. Otherwise, the mode will be changed to other subsystems at $t = 1$ (or $t = \tau + 1$).

The proof is thus completed.

Let $\mathcal{I} := \{i \mid d_i = 1\}$, $\mathcal{J} := \{i \mid 1 < d_i < \infty\}$, and $\mathcal{K} := \{i \mid d_i = \infty\}$. Define a series of input-state subsets as $\mathcal{O}_i := \{\delta_{MN}^{O_i} \mid \delta_{MN}^{O_i} = \delta_i\}$, and define the singleton version of $\mathcal{O}_i$ as $\hat{\mathcal{O}}_i := \{\delta_{MN}^{O_i} \mid \delta_{MN}^{O_i} = \delta_i\}$. Now using Proposition 19, we can obtain the following result.

Theorem 23 The switching signal sequence which guarantees the FOTs of the switched linear system (1) can be generated regardless of the initial logical state of the logical control network (3), if and only if

(1) $\forall i \in \mathcal{I}$, the system is 1-step input-state set reachable from every singleton in $\hat{\mathcal{O}}_i$ to $\Delta_{MN} \setminus \mathcal{O}_i$, that is,

$$P^{T}_{\{\Delta_{MN} \setminus \mathcal{O}_i\}} \times_{B} L \times_{B} P_{\mathcal{O}_i} = 1^{T}_{\mathcal{O}_i}. \quad (19)$$

(2) $\forall i \in \mathcal{J}$, the system is 1-step input-state set reachable from every singleton in $\hat{\mathcal{O}}_i$ to both $\Delta_{MN} \setminus \mathcal{O}_i$ and $\mathcal{O}_i$, that is,

$$\begin{cases} P^{T}_{\{\Delta_{MN} \setminus \mathcal{O}_i\}} \times_{B} L \times_{B} P_{\mathcal{O}_i} = 1^{T}_{\mathcal{O}_i}, \quad \text{if } \sigma = 1 \\ P^{T}_{\{\mathcal{O}_i\}} \times_{B} L \times_{B} P_{\mathcal{O}_i} = 1^{T}_{\mathcal{O}_i}. \end{cases} \quad (20)$$

(3) $\forall i \in \mathcal{K}$, the system is 1-step input-state set reachable from singleton in $\hat{\mathcal{O}}_i$ to $\mathcal{O}_i$, that is,

$$P^{T}_{\{\mathcal{O}_i\}} \times_{B} L \times_{B} P_{\mathcal{O}_i} = 1^{T}_{\mathcal{O}_i}. \quad (21)$$

where $L = 1_M L = [L^T, L^T, \ldots, L^T]^T$ is the input-state matrix of the logical control network (3).

To avoid frequent switches of the subsystems, the concept of minimum dwell time is usually used when studying switched systems. It can be easily seen that the minimum dwell time is a special case of the FOT. To be specific, we have the following result.

Corollary 24 If the switching signal sequence is asked to align with a minimum dwell time $d_i \in \mathbb{Z}_+$ assigned to each subsystem $\Sigma_i$, then it is obvious that the logical control network (3) has the ability to generate the required switching signal sequences if condition (2) in Theorem 22 (equivalent to condition (2) in Theorem 23) is satisfied for $\forall i \in [1, q]$.

4.3 Finite Reference Signal Switching

A finite reference signal sequence is given in Case 2. The key point of this problem is checking whether the required signal sequence can be generated by the logical control network (3). In [51], the authors studied the finite horizon output tracking of Boolean control networks, which provides us with a way to solve the problem. We first generalize the concept of finite horizon output tracking to $\sigma$-tracking of the logical control network (3).

Definition 25 Consider the logical control network (3) with an initial state $\theta_0$. The reference signal sequence $(\sigma_0, \sigma_1, \ldots, \sigma_\tau)$ is called trackable if there exists a logical input sequence $\Gamma := (\gamma_0, \gamma_1, \ldots, \gamma_\tau)$ such that

$$\sigma(t, \theta_0, \Gamma) = \sigma_t, \quad t = 0, 1, \ldots, \tau.$$
For a given reference signal sequence \((\sigma_0, \sigma_1, \ldots, \sigma_\tau)\), we define a series of input-state subsets as
\[
O_{\sigma_t} := \{ \delta^i_{MN} \mid R\delta^i_{MN} = \sigma_t \}, \; t = 0, 1, \ldots, \tau.
\]

Then using the input-state set controllability method and the results in [51], we have the following theorem.

**Theorem 26** Consider the logical control network (3) with an initial state \(\theta_0\). The reference signal sequence \((\sigma_0, \sigma_1, \ldots, \sigma_\tau)\) is trackable, if and only if
\[
P_{\{O_{\sigma_t}\}}^T L \bar{\theta}(t - 1) > 0, \; t = 1, 2, \ldots, \tau, \tag{22}
\]
where
\[
\bar{\theta}(t) = \begin{cases} 
\bar{\theta}(0) = L_{\theta_0} \bar{\theta}(0) \wedge P_{\{O_{\sigma_0}\}} \ 
\bar{\theta}(t) = (L \times_B \bar{\theta}(t - 1)) \wedge P_{\{O_{\sigma_t}\}}.
\end{cases}
\]

**Proof:** It is clear that the tracking problem has a solution if and only if there is an input-state sequence \(\{(\gamma_0, \theta_0), (\gamma_1, \theta_1), \ldots, (\gamma_\tau, \theta_\tau)\}\), where \(\theta_0\) is given, such that
\[
R_{\gamma_t} \bar{\theta}_t = \bar{\sigma}_t, \; t = 0, 1, \ldots, \tau,
\]
where \(\bar{\theta}_{t+1} = L_{\gamma_t} \bar{\theta}_t, \; t = 0, 1, \ldots, \tau - 1\). That is, the input-state sequence satisfies the following condition:

- For \(t = 1, 2, \ldots, \tau\), \(\gamma_t \bar{\theta}_t\) is 1-step reachable from \(\gamma_{t-1} \bar{\theta}_{t-1}\), where \(\gamma_t \bar{\theta}_t \in O_{\sigma_t}\) for \(t = 0, 1, \ldots, \tau\).

**Sufficiency:** Using Proposition 19 and its proof, one sees easily that in equation (22), \(\bar{\theta}(t)\) is the sum of all the possible input-states that can generate \(\bar{\sigma}_t\) at the \(t\)-th step. If (22) holds, then there is an input-state path such that the above condition is ensured.

**Necessity:** If equation (22) does not hold for at least one \(t \in [1, \tau]\), then by Proposition 19 we know that \(\gamma_t \bar{\theta}_t \notin O_{\sigma_t}\), which contradicts the above condition. \(\Box\)

With the above results, the system realization solvability condition is obtained.

**Theorem 27** Consider the switched linear system (1) where the switching signal is generated by the logical control network (3). The signal sequence, which aligns with the reference sequence \((\sigma_0, \sigma_1, \ldots, \sigma_\tau)\), can be generated by the system (3) starting from an initial logical state \(\theta_0\), if and only if the reference sequence is \(\sigma\)-trackable by the system (3).

5 **Illustrative Example**

**Example 28** Consider the SLS
\[
x(t + 1) = A_{\sigma(t)} x(t) + B_{\sigma(t)} u(t),
\]
\[
y(t) = C_{\sigma(t)} x(t), \tag{23}
\]
whose switching signals \(\sigma(t) = \{1, 2\}\) are generated by the following logical control network
\[
\bar{\theta}(t + 1) = L \times \bar{\gamma}(t) \times \bar{\theta}(t),
\]
\[
\bar{\sigma}(t) = R \times \bar{\gamma}(t) \times \bar{\theta}(t), \tag{24}
\]
where
\[
A_1 = \begin{bmatrix} 1 & 2 & -1 \\ 0 & 1 & 0 \\ 1 & -4 & 3 \end{bmatrix}, \quad B_1 = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}, \quad C_1 = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix},
\]
\[
A_2 = \begin{bmatrix} -2 & 2 & 1 \\ 0 & -2 & 0 \\ 1 & -4 & 0 \end{bmatrix}, \quad B_2 = \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix}, \quad C_2 = \begin{bmatrix} 0 & 1 & 0 \end{bmatrix},
\]
\[
L = \delta_4[1, 1, 2, 4, 4, 4, 3, 3],
\]
\[
R = \delta_2[2, 2, 1, 1, 1, 2, 2, 1].
\]

With equation (5), one has
\[
G = \begin{bmatrix} G_1, G_2 \end{bmatrix},
\]
Using Algorithm 1, we have

\[ \Delta = \delta_1 \]

The transition 7 in [52], we know that all the logical states are control attractors, and the attractor basins of the logical network (24). Using Proposition 1, we first check the control attractors, as well as their attractor basins of the logical network (24). We then check if equations (14), and (15) hold for all the 3-length logical input sequences except (2, 2, 2).

### 6 Conclusion

This paper presents a novel approach to studying the control properties of SLSs with logic dynamic switching. The proposed approach combines the ASSR method and merged hybrid systems to analyze the reachability, controllability, observability, and reconstructibility of such systems. Additionally, two types of system realization problems are investigated by introducing the concept of input-state set reachability. The proposed methods can be extended to continuous-time linear systems.

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Appendix

A Semi-Tensor Product of Matrices

We briefly introduce the mathematical tool used in this paper, that is, the semi-tensor product (STP) of matrices and the algebraic state-space representation (ASSR) method of logical control networks.

Definition 29 ([29]) Let $A \in \mathcal{M}_{m \times n}$, $B \in \mathcal{M}_{p \times q}$, and the least common multiple of $n$ and $p$ be $t = \text{lcm}(n, p)$ (the least common multiple of $n$ and $p$). The STP of $A$ and $B$, denoted by $A \times B$, is defined as

$$ (A \otimes I_{t/n})(B \otimes I_{t/p}). \quad (A.1) $$

From Definition 29, one sees that the STP is a generalization of the conventional matrix product because they are equivalent when $n = p$. Hence, we do not need to deliberately distinguish them, and in this paper, if it will not cause misunderstanding, the symbol “$\times$” is omitted.

Consider an $n$-node $\kappa$-value logical control system whose logical evolutionary dynamics is

$$ \begin{aligned}
\theta_1(t + 1) &= f_1(\theta_1(t), \ldots, \theta_n(t); \gamma_1(t), \ldots, \gamma_m(t)), \\
\theta_2(t + 1) &= f_2(\theta_1(t), \ldots, \theta_n(t); \gamma_1(t), \ldots, \gamma_m(t)), \\
&\vdots \\
\theta_n(t + 1) &= f_n(\theta_1(t), \ldots, \theta_n(t); \gamma_1(t), \ldots, \gamma_m(t)), \\
\end{aligned} \quad (A.2) $$

where $\theta_i(t) \in \mathcal{D}_\kappa$, $i \in [1, n]$ are the state nodes, $\gamma_j(t) \in \mathcal{D}_\kappa$, $j \in [1, m]$ are the input nodes, $f_i : \mathcal{D}_{\kappa^{n+m}} \rightarrow \mathcal{D}_\kappa$ are logical functions.

Identifying $\alpha \sim \delta^\alpha$ and $\beta \sim \delta^\beta$ for $\alpha, \beta \in [1, \kappa]$, $\theta_i$ and $\gamma_j$ can be expressed into their vector forms as

$$ \begin{aligned}
\bar{\theta}_i := \delta^\alpha \theta_i, & \quad i \in [1, n] ; \\
\bar{\gamma}_j := \delta^\beta \gamma_j, & \quad j \in [1, m].
\end{aligned} $$

Denote by $\bar{\theta} = (\bar{\theta}_1, \bar{\theta}_2, \ldots, \bar{\theta}_n) \in \mathcal{D}_\kappa^n$ and $\bar{\gamma} = (\bar{\gamma}_1, \bar{\gamma}_2, \cdots, \bar{\gamma}_m) \in \mathcal{D}_\kappa^m$ the overall state variable and overall input variable. Their vector form expressions are

$$ \begin{aligned}
\bar{\theta} := \kappa^{m+1}_{i=1} \bar{\theta}_i \in \Delta_{\kappa^n}, \\
\bar{\gamma} := \kappa^{m+1}_{j=1} \bar{\gamma}_j \in \Delta_{\kappa^m}.
\end{aligned} $$

The following proposition is borrowed from [29] and [30].

Proposition 30(i) Let $f : \mathcal{D}_{\kappa^{n+m}} \rightarrow \mathcal{D}_\kappa$, expressed by

$$ \zeta = f(\theta_1, \theta_2, \cdots, \theta_n; \gamma_1, \gamma_2, \cdots, \gamma_m), $$

be a logical function. Then there exists a unique logical matrix $M_f \in \mathcal{L}_{\kappa^{n+m} \times \kappa^{n+m}}$, called the structure matrix of $f$, such that in vector form the logical function can be expressed by

$$ \bar{\zeta} = M_f \bar{\gamma} \bar{\theta}. \quad (A.3) $$

(ii) Let $M_i$ be the structure matrix of the logical function $f_i$, $i = 1, 2, \cdots, n$. Then there exists a unique logical matrix $M \in \mathcal{L}_{\kappa^{n+m} \times \kappa^{n+m}}$ such that in vector form, logical control network (A.2) can be expressed by

$$ \bar{\theta}(t + 1) = L \bar{\gamma}(t) \bar{\theta}(t), \quad (A.4) $$

where $L = M_1 * M_2 * \cdots * M_n$ is called the structure matrix of the logical control network (A.2).

Equation (A.4) is called the ASSR of the logical control network (A.2).

Definition 31 [52] Consider the logical system (3). Given a state subset $V \subset \Delta_N$:

1. A state $\bar{\theta}^* \in V$ is a control fixed point in $V$, if there exists an input $\bar{\gamma} \in \Delta_M$ such that $L \bar{\gamma} \bar{\theta}^* = \bar{\theta}^*$.
2. A state subset $\{\theta(0), \theta(1), \cdots, \theta(\ell - 1)\} \subset \Delta_N$ is called a control cycle in $V$, if there exists an input sequence $(\gamma(0), \gamma(1), \cdots, \gamma(\ell - 1))$ such that
   - $\bar{\theta}(t + 1) = L \bar{\gamma}(t) \bar{\theta}(t)$, $t \in [0, \ell - 2]$;
   - $\bar{\theta}(0) = L \bar{\gamma}(\ell - 1) \bar{\theta}(\ell - 1)$.
3. The control fixed points and control cycles are collectively referred to as the control attractors; the union of all the control fixed points and control cycles in $V$ is called the control attractor set of $V$.
4. For a control attractor, its attract basin is the set of all the states that can be steered to the control attractor.

* For 2-value logical networks (i.e. Boolean networks), the domain is usually defined as $\{1, 0\}$, which is equivalently defined as $\{1, 2\}$ in this paper, just for simplicity of expression.