Tunneling FET Calibration Issues: Sentaurus vs. Silvaco TCAD

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Abstract. In this paper, a comprehensive comparison of TFET simulations using two TCAD simulators, Sentaurus and Silvaco TCAD, is presented. The comparison is fully cover various types of TFETs, either from the structure geometry or the materials point of view, which proved a framework for TFET designs and simulations. For Sentaurus TCAD, a dynamic nonlocal BTBT model is used for all simulations as it is proved a good calibration for experimental data or full quantum data taken from the literature. The BTBT model’s parameters are determined for different material and hetero-junctions structures where they can be used directly for any design or structure calibration. For the Silvaco simulator, a nonlocal BTBT model is utilized for calibration and its parameters are also provided. The study offers quick parameters data to be used directly, utilizing various materials without being involved in calibration difficulties.

1. Introduction

Tunneling field-effect transistors (TFETs) has been innovated as an alternative to tackle some challenges of traditional MOSFET transistors [1, 2]. The current in TFET is mainly due to band-to-band tunneling (BTBT) phenomena rather than thermionic emission in MOSFET [3, 4]. TFET can operate well at low supply voltage providing low OFF current [2, 5]. However, TFETs face a low ON current [2], am-bipolarity of current, and implementation difficulties [6].

Performance enhancement of TFETs is done to acquire mainly a higher ON current and to overcome other TFET obstacles [7]. In this regard, different structures are investigated, such as multi-gate [1] or gate all around (GAA) [8] structures, which can be entirely fabricated by CMOS technology and reduce short-channel effects. Hetero structures may also be used to enhance the TFET characteristics where the source material is replaced by a smaller bandgap material i.e. Ge or Mg₂Si [2, 9]. Using such low bandgap materials results in a reduction of the tunneling resistance, so the ON current, in turn, is improved. Other III-V materials may completely replace Si to provide a good
tunneling probability like InAs [10], which has a direct bandgap instead of the indirect bandgap of Silicon.

Many studies have been done on TFET fabrications [11, 12]. Others utilized the simulation results to predict, design, and optimize the TFETs performance [13, 14]. Many simulator tools are used such that Sentaurus [15] and Silvaco [16] TCAD simulators, which provide efficient BTBT models. Regarding TCAD environments, four models are equipped to track the BTBT phenomena [15]: Kane model, Hurkx model, Schenk model, and the nonlocal model. Among them, the nonlocal BTBT model is found to be the most accurate model to simulate tunneling in TFETs [15-17].

In Silvaco, the nonlocal BTBT model has to be accompanied by a fine quantum meshing around the expected tunneling area. On the other hand, in Sentaurus, the nonlocal model gives a dynamic path of tunneling starting from the Valence band (VB) to the Conduction band (CB) or vice versa in the direction of the electric field [15], so it is called dynamic nonlocal BTBT model. Both models show the right way to calibrate the experimental and full quantum simulation results.

In this work, extensive calibrations of different device structures with homo and heterojunctions using various materials are reported by using both Sentaurus and Silvaco TCAD Tools. The calibration results are compared to experimental and full quantum results available in the literature. The BTBT parameters for both simulators are given for the various TFET structures, which could facilitate the calibration process and expedite the TFET design utilizing different materials and structures.

2. Device structures and materials

Different TFET structures and materials are used in the following simulations. Fig. 1(a) shows a multi-gate TFET [18], which is used to allow TFET’s implementation using standard FinFET processing techniques. Fig. 1(a) illustrates the actual 3D structure while Fig. 1(b) demonstrates the 2D representation used in the simulation. Fig. 1(c) shows a 3D Gate-all-around (GAA) silicon nanowire (NW) TFET [8] while Fig. 1(d) shows the 2D structure used for simulation where simulation is done by what is called cylindrical coordinates [16]. Further, Fig. 1(e) shows the third structure in which the source is formed of Ge instead of Silicon as a heterostructure to reduce the effective barrier height [6]. A hetero-dielectric-gate is also used in this structure with source overlap to confine tunneling inside Ge. Furthermore, Fig. 1(f) and (g) demonstrate the fourth structure used. The structure is a GAA TFET and the Silicon is wholly replaced by InAs material [19]. InAs is an III-V compound semiconductor that has a smaller bandgap than Silicon (having a bandgap of \( E_{g_{\text{InAs}}} = 0.37 \text{ eV} \)). Finally, Fig. 1(h) shows the last structure used in simulations. In this structure, MgSi (having a bandgap of \( E_{g_{\text{MgSi}}} = 0.77 \text{ eV} \)) is introduced as a new material for the source [20]. All the structures parameters and material properties used are summarized in Table 1.
3. Results and discussion

Firstly, the calibration is performed for a multi-gate TFET structure. Fig. 2 (a) shows the simulation results where the calibration is done vs experimental data available in [18]. To perform the calibration, the dynamic nonlocal BTBT model in Sentaurus is activated with the parameters’ values for phonon-assisted of $A_{\text{path}} = 2.2 \times 10^{17} \text{cm}^3\text{s}^{-1}$ and $B_{\text{path}} = 8.2 \times 10^6 \text{Vcm}^{-1}$ and for direct of $A_{\text{path}} = 4.8 \times 10^{17} \text{cm}^3\text{s}^{-1}$ and $B_{\text{path}} = 6.45 \times 10^6 \text{Vcm}^{-1}$ [21]. For the low voltage values of $V_{\text{GS}}$, the Hurkx Trap-assisted Tunneling (TAT) model is used. The result in [18] is divided by $25 \times 10^{-3}$ to account for the third gate. Regarding Silvaco TCAD, the effective tunneling masses of the nonlocal BTBT model are tuned to get the best fit. Electron and hole effective masses are found to be 0.11 and 0.17, respectively. These effective masses values are compatible with those found in the literature for a similar double gate n-type TFET structure [22-24]. The BTBT parameters for both Sentaurus and Silvaco are found to be used in all simulations concerning Silicon material. So, the same parameters will be used for the next case study which involves Silicon material.

Further, Fig. 2 (b) shows both experimental and simulation results of the Gate-all-around Silicon nanowire TFET structure [8]. To calibrate this structure in Sentaurus, the same model of multi-gate TFET is used. Also, Silvaco tunneling masses used in the previous structure are applied as stated above. To calibrate the OFF current when using Silvaco, the SRH (Shockley Read Hall) recombination and TAT (Trap Assisted Tunneling) models should be incorporated as the BTBT model.
is not suitable to fit this region because the tunneling width is increased and thermionic current dominates. To get the best fit, the adjusted values of the lifetimes are found to be $\tau_{\text{min}} = 0$ for both electron and holes and $\tau_{\text{max}} = 1 \times 10^5$ s for electron and $\tau_{\text{max}} = 3 \times 10^6$ s for holes, for TAT models, Electron and hole effective masses are found to be 0.11 and 0.17, respectively.

Furthermore, Fig. 2 (c) shows the simulation results of Ge-source hetero-dielectric TFET [6]. As can be seen from the results, the ON current has improved with a decline in the OFF current compared to silicon TFET. To calibrate the full quantum simulation results, the direct BTBT model is used with $A_{\text{path}} = 1.465 \times 10^{20}$ cm$^3$s$^{-1}$ and $B_{\text{path}} = 6.03 \times 10^6$ Vcm$^{-1}$ [6] and the phonon-assisted model is used with $A_{\text{path}} = 4 \times 10^{14}$ cm$^3$s$^{-1}$ and $B_{\text{path}} = 1.9 \times 10^7$ Vcm$^{-1}$. Regarding Silvaco, the electron and hole tunneling masses are adjusted as 0.12 and 0.18, respectively. It should be pointed out here that the adjustment of the tunneling masses is straightforward and needs little effort to reach the best fit. This is also valid for all materials, as will be shown hereafter.

Moreover, Fig. 2 (d) and (e) shows the calibration results of all InAs GAA TFET. The results show an improvement in ON current compared to silicon TFET while the OFF current is degraded. The data used in calibration is based on a full quantum simulator. However, this simulator proved to be compatible with measurements [19, 26, 27]. To calibrate the results in Sentaurus, the pre-factor value is found to be $A_{\text{path}} = 2 \times 10^{20}$ and the exponential factor $B_{\text{path}} = 2.24 \times 10^6$ Vcm$^{-1}$ as mentioned in [28]. The simulation shown in Fig. 2 (d) is done also with the same parameters in 3D using Sentaurus.

Regarding Silvaco TCAD, the simulation is done for the 2D case only as the BTBT model used in Silvaco is not enabled in 3D structures, which is a disadvantage of this simulator. Silvaco nonlocal BTBT model is only constrained to modeling 1D and 2D TFET geometries. It can be used to model a 3D TFET structure if the structure is cylindrical and can be divided into two symmetric parts. In this regard, half the device is considered and the meshing option of cylindrical is enabled as done in the case of GAA. Silvaco’s fitting parameters of electron and hole tunneling masses are adjusted to 0.15 and 0.18, respectively, to get the best fit.

Finally, Fig. 2 (f) shows the simulation results of Mg$_2$Si-source TFET. Like Ge-source TFET, the Mg$_2$Si-source TFET shows an enhancement in ON current, and the OFF current is reduced compared to all-silicon TFET. Comparing Mg$_2$Si-source TFET with Ge-source TFET, the Mg$_2$Si-source TFET shows better ON current. As there is no experimental or full quantum data are available for this new material, we used the same effective masses used in Silicon for Silvaco simulation while for Sentaurus simulation the parameters’ values for phonon-assisted are adjusted to $A_{\text{path}} = 9 \times 10^{17}$ cm$^3$s$^{-1}$ and $B_{\text{path}} = 1.9 \times 10^7$ Vcm$^{-1}$ and for direct of $A_{\text{path}} = 2 \times 10^{21}$ cm$^3$s$^{-1}$ and $B_{\text{path}} = 2.06 \times 10^7$ Vcm$^{-1}$. These results are compatible with the first published work for a TFET regarding this material [29].

Table 2. Calibrated parameters for Sentaurus and Silvaco Simulators ($A_{\text{path}}$ and $B_{\text{path}}$ are in units of cm$^3$s$^{-1}$ and Vcm$^{-1}$, respectively)

| TFET Structure       | Sentaurus Parameters | Silvaco Parameters |
|----------------------|----------------------|--------------------|
|                      | Phonon-assisted | Direct | $m_e$ | $m_h$ |
| Multi-gate Si        | $2.2 \times 10^{17}$ | $8.2 \times 10^6$ | $4.8 \times 10^6$ | $6.45 \times 10^6$ | 0.11 | 0.17 |
| GAA Si NW            | $2.2 \times 10^{17}$ | $8.2 \times 10^6$ | $4.8 \times 10^6$ | $6.45 \times 10^6$ | 0.11 | 0.17 |
| Ge-source hetero-dielectric | $4 \times 10^{14}$ | $1.9 \times 10^7$ | $1.465 \times 10^{10}$ | $6.03 \times 10^6$ | 0.12 | 0.18 |
| All InAs GAA         | $2 \times 10^{20}$ | $2.24 \times 10^6$ | $2 \times 10^{20}$ | $2.24 \times 10^6$ | 0.15 | 0.18 |
| Mg$_2$Si-source      | $9 \times 10^{17}$ | $1.9 \times 10^7$ | $2 \times 10^{14}$ | $2.06 \times 10^7$ | 0.11 | 0.17 |

Table 2 summarizes the calibrated parameters used in the nonlocal BTBT models of both Sentaurus and Silvaco simulators. As can be depicted from the previous simulations and the reported values given in Table 2, we can highlight the following. Although Sentaurus provides a wide range of parameters to be tuned when calibrating its dynamic BTBT model, which could be an advantage, it
may lead to different parameters used from research to another. Meanwhile, Silvaco limits the calibration of the nonlocal BTBT model only on two parameters, which are easier to be fitted even manually.

![Graphs and images](image-url)

Figure 2. Calibration of (a) multi-gate Silicon TFET. (b) Gate-all-around Silicon nanowire TFET. (c) Ge-source hetero-dielectric TFET. (d) All InAs GAA TFET (3D case) (e) All InAs GAA TFET (2D case) (f) Simulation results of Mg2Si-source TFET.

4. Conclusion

In this work, a brief flow of TFET calibration using Sentaurus and Silvaco TCAD tools is presented. The calibration is done using experimental and full quantum data. Different structures including multi-gate Silicon, Gate-All-Around Si nanowire, Ge-source, MgSi-source, and all InAs TFETs are used in this calibration study to find the BTBT parameters, for both Sentaurus and Silvaco simulators, that
best fit the data. The simulation results could provide a good source in investigating numerous TFET structures with different materials either for Sentaurus or Silvaco TCAD environments.

References
[1] Leonelli, D., Vandooren, A., Rooyackers, R., Verhulst, A.S., De Gendt, S., Heyns, M.M. and Groeseneken, G., 2010. Performance enhancement in multi gate tunneling field effect transistors by scaling the fin-width. Japanese Journal of Applied Physics, 49(4S), p.04DC10.
[2] Kim, S.H., Kam, H., Hu, C. and Liu, T.J.K., 2009, June. Germanium-source tunnel field effect transistors with record high $I_{ON}/I_{OFF}$. In 2009 Symposium on VLSI Technology (pp. 178-179). IEEE.
[3] Sajjad, R.N., Chern, W., Hoyt, J.L. and Antoniadis, D.A., 2016. Trap assisted tunneling and its effect on subthreshold swing of tunnel FETs. IEEE Transactions on Electron Devices, 63(11), pp.4380-4387.
[4] Gopi, C. and Chauhan, S.S., 2016, April. Double-gate Ge, In As-based tunnel FETs with enhanced ON-current. In 5th International Conference on Communication and Signal Processing (ICCSIP) (pp. 0639-0641). IEEE.
[5] Jain, P., Rastogi, P., Yadav, C., Agarwal, A. and Chauhan, Y.S., 2017. Band-to-band tunneling in $\Gamma$ valley for Ge source lateral tunnel field effect transistor: thickness scaling. Journal of Applied Physics, 122(1), pp.014502.
[6] Poorvasha, S. and Lakshmi, B., 2018. Influence of structural and doping parameter variations on Si and Si$_{1-x}$Ge$_x$ double gate tunnel FETs: An analysis for RF performance enhancement. Pramana, 91(1), p.2.
[7] Chen, Z.X., Yu, H.Y., Singh, N., Shen, N.S., Sayanthan, R.D., Lo, G.Q. and Kwong, D.L., 2009. Demonstration of tunneling FETs based on highly scalable vertical silicon nanowires. IEEE Electron Device Letters, 30(7), pp.754-756.
[8] Madan, J., Dassi, M., Pandey, R., Chaujar, R. and Sharma, R., 2020. Numerical analysis of Mg$_2$Si/Si heterojunction DG-TFET for low power/high performance applications: Impact of non-idealities. Superlattices and Microstructures, 139, p.106397.
[9] Pala, M.G. and Esseni, D., 2013. Interface traps in InAs nanowire tunnel-FETs and MOSFETs—Part I: Model description and single trap analysis in tunnel-FETs. IEEE transactions on electron devices, 60(9), pp.2795-2801.
[10] Bhuwalka, K.K., Sedlmaier, S., Ludsteck, A.K., Tolksdorf, C., Schulze, J. and Eisele, I., 2004. Vertical tunnel field-effect transistor. IEEE Transactions on Electron Devices, 51(2), pp.279-282.
[11] Bhuwalka, K.K., Born, M., Schindler, M., Schmidt, M., Sulima, T. and Eisele, I., 2006. P-channel tunnel field-effect transistors down to sub-50 nm channel lengths. Japanese journal of applied physics, 45(4S), p.3106.
[12] Verhulst, A.S., Vandenbergh, W.G., Maex, K. and Groeseneken, G., 2008. Boosting the on-current of an-channel nanowire tunnel field-effect transistor by source material optimization. Journal of Applied Physics, 104(6), p.064514.
[13] Toh, E.H., Wang, G.H., Samudra, G. and Yeo, Y.C., 2008. Device physics and design of germanium tunneling field-effect transistor with source and drain engineering for low power and high performance applications. Journal of Applied Physics, 103(10), p.104504.
[14] Sentaurus Device User Guide, Version H-2013.03, 2013
[15] Silvaco TCAD User Guide version 2015
[16] Kampen, C., Burenkov, A. and Lorenz, J., 2011, September. Challenges in TCAD simulations of tunneling field effect transistors. In 2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC) (pp. 139-142). IEEE.
[17] Der Agopian, P.G., Martino, M.D.V., dos Santos Filho, S.G., Martino, J.A., Rooyackers, R., Leonelli, D. and Claeys, C., 2012. Temperature impact on the tunnel FET off-state current components. Solid-state electronics, 78, pp.141-146.
[18] Luisier, M. and Klimeck, G., 2009. Atomistic full-band design study of InAs band-to-band tunneling field-effect transistors. IEEE Electron Device Letters, 30(6), pp.602-604.

[19] Wu, Y., Kakushima, K. and Takahashi, Y., 2017, June. Formation of magnesium silicide for source material in Si based tunnel FET by annealing of Mg/Si thin film multi-stacks. In 2017 17th International Workshop on Junction Technology (IWJT) (pp. 83-84). IEEE.

[20] Shaikh, M.R.U. and Loan, S.A., 2019. Drain-engineered TFET with fully suppressed ambipolarity for high-frequency application. IEEE Transactions on Electron Devices, 66(4), pp.1628-1634.

[21] Shaker, A., El Sabbagh, M. and El-Banna, M.M., 2017. Influence of drain doping engineering on the ambipolar conduction and high-frequency performance of TFETs. IEEE transactions on electron devices, 64(9), pp.3541-3547.

[22] Shaker, A., ElSabbagh, M. and El-Banna, M.M., 2019. Impact of nonuniform gate oxide shape on TFET performance: A reliability issue. Physica E: Low-dimensional Systems and Nanostructures, 106, pp.346-351.

[23] Boucart, K. and Ionescu, A.M., 2007. Double-gate tunnel FET with high-κ gate dielectric. IEEE transactions on electron devices, 54(7), pp.1725-1733.

[24] Shaker, A., Maged, A., Elshorbagy, A., AbouElainain, A. and Elsabbagh, M., 2020. Source-all-around tunnel field-effect transistor (SAA-TFET): proposal and design. Semiconductor Science and Technology, 35(2), p.025007.

[25] Luisier, M., Schenk, A., Fichtner, W. and Klimeck, G., 2006. Atomistic simulation of nanowires in the sp’d’s* tight-binding formalism: From boundary conditions to strain calculations. Physical Review B, 74(20), p.205323.

[26] Luisier, M., Schenk, A. and Fichtner, W., 2007. Atomistic treatment of interface roughness in Si nanowire transistors with different channel orientations. Applied Physics Letters, 90(10), p.102103.

[27] Madan, H., Saripalli, V., Liu, H. and Datta, S., 2012. Asymmetric tunnel field-effect transistors as frequency multipliers. IEEE electron device letters, 33(11), pp.1547-1549.

[28] Wu, Y., Hasegawa, H., Kakushima, K., Ohmori, K., Watanabe, T., Nishiyama, A., Sugii, N., Wakabayashi, H., Tsutsui, K., Kataoka, Y. and Natori, K., 2014. A novel hetero-junction Tunnel-FET using Semiconducting silicide–Silicon contact and its scalability. Microelectronics Reliability, 54(5), pp.899-904.