Abstract

Particulate detection, which is based on lock-in amplifier technology, requires a phase-shift signal generator with wide frequency range and high phase shift precision. Since the current phase-shift signal generator has a deficiency of low precision in high frequency range, the author designed a phase-shift generator which adopts direct digital frequency synthesis technology, and expresses hardware design principles of the system. This paper focuses on the design of hardware and software concerning high precision phase shift and amplitude closed-loop control. The experimental results indicate that the output signals have a high accuracy in phase difference, frequency and amplitude under a wide frequency range and this system achieves the requirements of particulate detection.

Keywords: phase shift signal generator; AD9852; lock-in amplifier; particulate detection

1. Introduction

Air pollution is an important factor to affect human health and airborne particulates are the main components of pathogenic factors. How to effectively detect particulates has long been a major research subject to domestic environmental monitoring researchers [1]. The light extinction measurement is commonly used in particle detection [2]. However, the effective signals are always submerged in the background field [3]. The lock-in amplifier detection is an effective method to improve this problem [4], but it needs to manually adjust the phase shift of reference channel. It could not guarantee the phase shift
precision, and cause the DC output unstable which affect the accuracy. Nowadays, digital phase shift signal generator was also put forward which did not need manually adjustment. However, the frequency and phase-shifting precision were difficult to meet the demand for particulate detection which needs 1Hz~5MHz frequency range and 0.1° phase-shifting precision at least.

In order to meet the particulate detection, the paper describes a design of phase shift signal generator which adopts direct digital frequency synthesis technology.

2. Principle of particulate detection

Its principle of lock-in amplifier technique is shown in Fig.1. Signal source generates a sinusoid excitation signal with fixed frequency for light source modulation. The modulated light rips into the air chamber after been coupled into the optical system. The output signal from air chamber is received by PIN photoelectric detector after been propagated through the fiber, and is converted to electronic signal. The electronic signal after been processed by signal processing circuit, performs multiplication with reference channel signal, and finally through the low pass filter (LPF) for DC signal which is related to particulate size and quantity.

Supposing \( X(t) = U_1 \sin(\omega t + \phi) + n(t) \) is the signal which was pre-processed by signal processing circuit, \( Y(t) = U_2 \sin \omega t \) is reference channel signal. \( U_1, U_2 \) are amplitude of signal, \( \omega \) is angular frequency, \( \phi \) is phase difference between \( X \) and \( Y \), \( n(t) \) is noise. According to the principle of lock-in amplifier detection, the final output DC signal can be described as [5]

\[
V_{DC} = \frac{1}{2} U_1 U_2 \cos \phi
\]  

(1)

Fig. 1. The sketch of airborne particulates detection based on lock-in amplifier technique

It indicates that the DC output \( V_{DC} \) is proportional to the amplitudes of the two input signals when \( \phi \) becomes zero. As a result, the relationship between \( V_{DC} \) and particulate size and concentration could be concluded by scaling. When taking measurement, the MCU changes the \( \phi \) continuously in auto scaling mode until it gets the maximum value of \( V_{DC} \).

3. Hardware design

As shown in Fig.2, the system is mainly composed of AD9852, LPC2212, clock circuit, low pass filter, programmable amplifier and driver output. AD9852 is a Direct Digital Frequency Synthesizer which highly integrated with adjustable module such as frequency, phase and amplitude. The highest internal clock of the chip is 300MHz. It has 12 bit DAC, 48 bit programmable frequency register and 14 bit programmable phase register.

For signal output, the system firstly writes frequency, phase and amplitude control words into AD9852 register through LPC2212, then enable external update clock. Two channels of sinusoidal signal with phase difference are generated after LPF, programmable amplifier and driver output Circuit.

The frequency and phase difference of the two channels can be calculated by Eq.(2) and Eq.(3):

\[
V_{DC} = \frac{1}{2} U_1 U_2 \cos \phi
\]
\[ f_{out} = f_{MCLK} \times \frac{FREG}{2^{18}} \]  
\[ \Delta P = 2\pi \times \frac{PREG1 - PREG2}{2^{14}} \]  

where FREG is frequency control word. PREG1, PREG2 are phase control words of AD9852 respectively. It can be concluded that the phase difference resolution between the two channels is 0.22°.

The system also realized the square wave output, which was generated by AD9852’s internal comparator since the smoothed sinusoidal signal was connected to VINP, VINN pin.

2.1. Phase control and synchronization

Phase control and synchronization of the two AD9852 chips was the key point of the system. For phase control, firstly reset the AD9852 so that the phase register is zero and always keep the phase of one AD9852 at zero, then change the phase value of the other to adjust phase difference. For high precision phase difference adjustment, measures for phase synchronization of the two chips were carried out:

1. Do keep the phase difference between the two AD9852 chips’ input reference clocks as small as possible. As shown in Fig.2, the active crystal oscillator’s clock signal was injected to zero delay buffer chip CY2305. And then make one of the synchronization output clocks from CY2305 as the input clock of D trigger, the other synchronization output clock was converted into differential clock for AD9852’s reference clock by MC100LEVEL16.

2. After the frequency control word write into AD9852 data buffer, it must be activated by an update clock (UD CLK) for signal output. The reference clock (REFCLK) and UD CLK should be satisfied timing sequence as Fig.3a shown. That is, the rising edge of UD CLOCK should be generated in effective area. To meet this requirement, active crystal oscillator was connected to D trigger, and makes the output signal Q of D trigger as reference clock of the UD CLOCK.

3. When PLL-based reference clock multiplier in AD9852 is used, the number of system clock sent into phase accumulator is uncontrollable and difficult to synchronization. So the multiplier function was bypassed to allow direct clocking for AD9852 from an external active oscillator with 30MHz frequency to meet the frequency range and avoid the phase unsynchronized.
2.2. Closed loop programmable amplification design

Programmable amplifier was needed since the maximum output voltage of DAC was limited at 0.5V. As shown in Fig. 3b, the output signal from low pass filter was scaled up to 10 V by OPA603 and realized 0-10 V regulation by digital potentiometer MAX5451. The gain of low pass filter is not constant in passband and will fluctuate with the change of the frequency. For accurate amplification, the MAX5451 was used for error correction.

For correction, adjust MAX5451(2)’s wiper to make its output equal to the preset value, and also make it as the reference voltage for negative input of comparator LMH7220. Since the reference voltage may not be accurate enough, the reference voltage was sampled by LPC2212 internal ADC for adjustment. Sinusoidal signal amplified by OPA603 was sent into positive input of LMH7220 after been adjusted by MAX5451(1), and was compared with reference voltage for final equivalence. The comparison result was acquired by Q and /Q output, which were connected to EINT0 and EINT1 pins of LPC2212 respectively. The MAX5451 contains two independent resistor arrays each with 255-resistive elements which were connected in series. So the minimum resolution of 10V reference voltage can reach 0.00153V precision.

4. Software design

The software include user interface, control word calculation, phase shift control unit and so on. Phase shift control unit in scanning phase mode is the key point of the software design, and the program flow is illustrated in Fig.4. After reset, change the default internal update clock to external one, write the phase and frequency control words into the register and update it. For first output signal, the program judges whether to output square wave. If it needs to output square wave in one channel, connect corresponding signal from LPF to AD9852 internal comparator which can output square wave. If not, connect corresponding signal from LPF to closed loop programmable amplification for amplitude adjustment, and finally output the sinusoid signal. For phase shift signal output thereafter, all need to do is calculate the step phase control word, write it into the corresponding register and update it.
5. Experimental results

To confirm the precision of the system, experiments for phase difference, amplitude ($V_{pp}$) and frequency were carried out. We used USB-6251 produced by NI for phase difference, amplitude measure and PM6671 for frequency measure. The result was shown in table 1. It could be concluded that the performance of the system can meet the demand of high precision airborne particulates detection.

Table 1. (a) Phase difference measure results (10 MHz); (b) Amplitude ($V_{pp}$), frequency measure results

| Preset/° | Measure/° | Preset/° | Measure/° | $V_{pp}$ Set/ V | Measure/ V | Freq Set/ Hz | Measure/ Hz |
|----------|-----------|----------|-----------|----------------|------------|--------------|-------------|
| 0.000    | 0.000     | 150.018  | 150.015   | 0.50           | 0.501      | 10           | 10.0000009  |
| 30.800   | 30.801    | 180.004  | 180.005   | 2.00           | 1.999      | 1k           | 1000.0017   |
| 60.016   | 60.014    | 270.006  | 270.003   | 5.00           | 5.002      | 100k         | 100000.04   |
| 90.003   | 90.003    | 300.014  | 300.011   | 8.00           | 8.001      | 1M           | 10000000M   |
| 120.012  | 120.012   | 330.000  | 330.001   | 10.00          | 9.999      | 10M          | 10.000001M  |

6. Conclusions

The system can output two channels sine or square wave signals. The frequency of each channel is $0 \sim 10$ MHz, the amplitude is $0 \sim 10$ V and the phase shift is $0 \sim 360$°. The system can set parameters arbitrarily and has the function of sweep frequency or phase automatically. The minimum frequency sweep step rate is 0.01 Hz and the minimum phase sweep step is 0.22°.

The phase shift signal generator based on AD9852 has advantage in resolution, conversion rate and reliability. It has wide application prospect in impedance measurement, gas concentration detection, and bioelectrical parameter measurement and so on.

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