JCI-CAC: An Efficient Crosstalk Avoidance Code Considering Joint Capacitive and Inductive Effects

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ABSTRACT
Capacitive coupling and inductive coupling are the two main factors in the occurrence of crosstalk fault in the communication bus. Among the various methods for reducing crosstalk fault, Crosstalk Avoidance Codes (CAC) codes are effective. However, with technology scaling, CACs are not able to prevent inductive effects. The proposed CACs methods are mainly based on capacitive coupling and do not consider inductive effects. To overcome this issue, a coding method is presented to avoid crosstalk fault called Joint Capacitive and Inductive CAC (JCI-CAC). The JCI-CAC coding reduces crosstalk faults by removing patterns of inductive coupling as ‘11111’ and ‘00000’ and capacitive coupling as ‘10101’ and ‘01010’. The JCI-CAC offers a new method to generate a new numerical system for data encoding that has a low computational overhead so that it can be used for any desired width of the communication bus. The simulation results of the proposed JCI-CAC mechanism are investigated in different criteria of delay, power consumption and area overhead. The simulation results provide less power consumption in JCI-CAC than other recent approaches. There have also been improvements in overhead area and critical paths in JCI-CAC coding. The main novelty of this paper is to provide a new numerical system and a new coding algorithm with minimum cell area overhead and power consumption, considering inductance coupling in addition to capacitive coupling. Based on simulation results, power consumption of JCI-CAC in the 8-bit and 16-bit bus is reduced by up to 20% compared to SOTA and FPF (PS-Fibo, S2AP, Improved Fibo-CAC, Fibo-CAC) codings. Also, cell area overhead in JCI-CAC compared to SOTA coding in an 8-bit bus is reduced by 4.8%.

INDEX TERMS
Reliability, crosstalk fault, crosstalk avoidance code, capacitive coupling, inductive coupling, crosstalk avoidance coding mechanism.

I. INTRODUCTION
In recent years, the very large-scale integration technology (VLSI) has advanced a lot, which has led to an increase in the number of different units on a chip. In fact, the presence of different components (processing and input/output) creates a complex hardware system on the chip so that it has high processing power [1]. But this steady increase has made a major challenge for designers due to the connecting cores using buses [2]. Based on ITRS projection, as the number of units on the chip increases, the number of processing cores on the chip will also increase, so that in 2025 this number will reach 7,000 chips [3]. In other words, the connection between these cores is an important challenge that significantly affects the system’s performance. Reliability is introduced as a measure to determine the performance of the system [4]. Therefore, the reliability of the data on the communication bus is important, which is compromised by the crosstalk fault between the wires of buses [5]. Crosstalk fault affects the reliability of the system by an fault in the signal of the data sent on the communication bus [6].

To increase the reliability of the communication bus between the various components on the chips, methods at different levels of renewal have been proposed. Crosstalk...
avoidance coding techniques significantly help to reduce the delay caused by crosstalk faults. Therefore, they are effective in improving the reliability of the communication bus.

To better understand the problem, one of the most important components of SoCs is the communication bus between its components. The performance of the communication bus is an important factor in ensuring the accuracy of the transmitted data. As mentioned earlier, the crosstalk fault is one of the important factors that compromises the reliability of the data on the communication bus, which leads to the error in the data that is sent over the communication bus. These faults occur in long wires adjacent to each other [7]. As a result, delays due to crosstalk faults in the transmission of the packets lead to the system bottleneck [4]. The most important cause of crosstalk fault is the formation of couplings that occur due to unwanted transition on the communication bus wires [8].

There are two types of effects between communication bus wires: capacitive coupling and inductive coupling [9]. Capacitive and inductive couplings lead to the effect of communication bus wires on each other. In other words, the transitions of the communication bus wires affect the data signal of each wire. This phenomenon is called crosstalk fault that causes an unwanted change in the data signal of adjacent wires on communication bus [7].

To solve the problem, Crosstalk Avoidance Code (CAC) is presented to prevent prohibited transitions from occurring on the communication bus which results in preventing crosstalk faults. Crosstalk Avoidance Code (CAC) has an efficient performance in increasing the systems-on-chip performance. Adding to it, in the previously presented methods, the communication bus is modeled as three-wire or five-wire. Five-wire methods are more accurate due to considering the effects of more adjacent wires [10]. Among these methods, again Crosstalk Avoidance Codes (CACs) have the best performance to deal with crosstalk faults.

Given the importance of inductive coupling in the future, it is necessary to investigate its effects on the communication bus on the chip [9]. Therefore, a coding method to prevent interference errors has been introduced, which is termed as Joint Capacitive and Inductive CAC (JCI-CAC). Next, the JCI-CAC mechanism is analyzed, evaluated, and compared with other state-of-the-art methods. Finally, our experimental results are reviewed and it is shown that the JCI-CAC method reduces power consumption, critical path overhead, and computational overhead compared to the recently studied methods.

The works presented in this paper are as follows:

1) A recursive formula is provided to produce a complete and unambiguous numerical system at all bus widths in mapping algorithm.

2) A coding algorithm for joint elimination of capacitive and inductive coupling patterns using the corresponding numerical system is presented.

3) To eliminate induction pair patterns (directional transitions), a formula is provided to calculate the determination of the smallest code word that can be sent.

The rest of the paper presents the necessary background and motivations for the importance of crosstalk faults and coding against crosstalk faults on the chips communication bus. In the following, previous works in the literature are reviewed, then the proposed method for crosstalk avoidance coding is presented. Finally, the simulation results of the proposed method are compared and analyzed in comparison with other recent CACs methods in various aspects including delay, power consumption, area overhead, and occurrence of forbidden transition patterns.

II. MOTIVATION AND RELATED WORK

The two main factors of crosstalk fault on the communication bus are: capacitive coupling and inductive coupling [9]. When two wires are adjacent to each other, an unwanted capacitor is created between them; Which is called the coupling capacitor [11]. On the other hand, changes in the magnetic field around the wires lead to inductive coupling. Capacitive and inductive coupling between adjacent wires leads to the mutual interaction of the communication wires [9]. The phenomenon of energy exchange between two wires is called crosstalk fault [7].

A communication bus with 3 wires is shown in Figure 1. Each wire is represented as a cylindrical that is used to transmit a bit of data. Five electrical capacitors are formed next to each bus wire in this way: the capacitor with the substrate is shown as $C_{g1}$, the capacitor with the symbol $C_{g2}$ that is formed between the wire and the side plates of the wire, the capacitors between adjacent wires are shown with $C_c$ [11].

In addition to the capacitive coupling, inductive coupling also occurs between the bus wires. The cause of inductive coupling changes in the magnetic field around the wires. Also, with increasing clock frequencies in the size of GHz, the changes of the magnetic field around the bus wires intensify. As a result, each wire has significant inductive effects on the surrounding wires.

To consider inductive coupling along with capacitive coupling in a communication bus on-chip, an electrical model for a 5-bit bus is presented. Each wire $b_i$ in the bus has a capacitor $C_{IG}$ (equal to the sum of capacitors $C_{g1}$ and $C_{g2}$ in Figure 1), resistance $R_i$ and inductor $L_i$. Capacitors $C_{(i,i+1)}$ and $C_{(i,i−1)}$ are considered to represent the effect of capacitive

![FIGURE 1. 3-bit communication bus capacitors.](image-url)
coupling and capacitors $I_{i-2,i}$, $I_{i-1,i}$, $I_{i,i+2}$ and $I_{i,i-1}$ are considered to show the inductive coupling impact [12].

According to research in the transition to deep fabrication technologies, wire height (shown with $T_{int}$ in Figure 1) decreases at a lower rate than wire width ($W_{int}$) and distance between adjacent wires ($S_{int}$) [13]. To have a closer look, the transition voltage generated by capacitive coupling and inductive coupling raises the signal level by up to 20% above the supply voltage [14]. Therefore, the capacitor coupling decreases at a lower rate than the substrate capacitor and the rate of occurrence and crosstalk faults increase with the transition to deep sub-micron technologies. In addition, with increasing clock frequency to GHz, inductive coupling becomes important and greatly affects the signals on the bus.

Crosstalk Avoidance Codes (CACs) are effective methods in avoiding/reducing crosstalk faults in the subject literature. The proposed CACs methods are mainly based on capacitive coupling and do not consider inductive coupling [15]. However, due to the increase in the length of the wires on the chip and the increase in frequency in the future, the inductive coupling becomes very important. The most important cause of crosstalk faults is the formation of couplings that occur due to unwanted transitions on the communication bus wires. There are two types of capacitive coupling and inductive coupling between the communication bus wires. Capacitors and inductive coupling cause the wires in the communication bus to interact with each other. In other words, the data signal of each wire in the communication bus is affected by the signals passing through the other wires. Unwanted data signal impact of adjacent wires is called crosstalk fault.

The construction of nano-scale VLSI has led to an increase in the growth rate of crosstalk faults [3]. In many communication systems, such as in-chip connections and quantum systems, system and environment interventions generally affect system performance [3]. On the other hand, increasing the parallel and long lines of the communication bus is directly related to increasing the length of the bus wires. According to the forecast, the total length of the wires on the chip will reach about 15,000 square meters per square meter in 2025, and the corresponding increase will be significant [3]. Figure 2 shows the predicted amount of wire length on the chip. Due to the growing trend of wire lengths, the delay due to compliance forms becomes the bottleneck of the system [16].

According to the graph in Figure 3, the number of processing cores in systems-on-chip is increasing. Due to the growth rate of the number of cores on the chip, the communication of the communication bus becomes more complex and extensive. Therefore, improving system performance and increasing reliability are significant. Also, reducing the delay of communication buses between the cores leads to improve performance [14], [17].

Thus, inductive effects cannot be ignored in the design of high-performance circuits nowadays, especially for global connections such as clock wires and signal buses [15]. Also, the worst patterns due to inductive coupling are quite different from capacitive coupling patterns, which makes the previously proposed coding schemes inefficient. Therefore, considering the effects of RLC to develop coding schemes to reduce bus delay is very important, because inductive in the design of high-performance circuits cannot be ignored [15].

When the signals of adjacent wires change in opposite directions, the worst-case transmission pattern delay occurs due to capacitive coupling. In contrast, the worst-case transition patterns are due to the effect of the inductive coupling, which occurs by changing adjacent wires in one direction. Therefore, considering inductive coupling is very important for the development of encryption schemes to reduce bus delay because today, inductive coupling can not be ignored in the design of high-performance circuits.

To investigate the effect of inductive coupling in this section, a classification of transition patterns is introduced which is based on the general magnetic inductive on the middle wire ($k$-th wire). The specified value in Eq (1) is defined to measure inductive coupling [9]:

$$W_k = \left| \sum_{i=k}^{i=k+\frac{1}{2}} \frac{1}{2} W_i \right|$$

(1)
In Eq. (1) in which $\Delta$ is equal to the number of adjacent wires considered for the mutual inductive effect, $w_i$ is equal to 1 for the transition $\uparrow$, $-1$ for transition $\downarrow$, and 0 for no transition. It should be noted that the symbol $\uparrow$ means the transition from bit 0 to 1 and the symbol $\downarrow$ means the transition from bit 1 to 0. If the transition does not change the bit, it is indicated by $-\text{symbol}$. It is also considerable that for $w_i$ equal to 1 or $-1$, the most inductive coupling is observed. Instead of considering two adjacent wires to determine capacitive coupling, the number of additional wires ($\Delta$) can be selected to consider inductive coupling. To classify transitions based on inductive coupling in a 5-bit bus, the effect of four adjacent wires on the middle wire is considered, and then patterns with close delay are placed in a class. Therefore, the third wire is considered as the middle wire ($k = 3$) and $\Delta = 4$. Since the 5-bit bus is considered, the amount of inductive coupling is calculated based on the value $W_3 = |\sum_{i=1}^{5} w_i|$. Due to the transition $\uparrow$ on the middle wire, there are $3^4 = 81$ different transition patterns which are shown in Table 1. By inverting all the patterns $\downarrow$ to $\uparrow$ and vice versa in Table 1, a similar classification can be obtained to transfer $\downarrow$ on the middle wire. The classification of unchanged patterns on the middle wire is shown in Table 2.

Also, according to the unchanged transitions on the middle wire in Table 2, the highest rate of inductive coupling in the directional transitions occurs in the wires adjacent to the middle wire. According to Table 1 and Table 2, when the adjacent wires change in one direction, the maximum amount of inductive effect exists. While in the capacitive effect, the worst case is showed up when the changes are in the opposite directions [19]. Due to the importance of inductive effects in the future, 5-wire classification with capacitive and inductive effects is more accurate.

Previous works on crosstalk fault reduction can be divided into physical level, transistor level, and register transfer level. Wire sizing and spacing [20], shielding [20], and repeater insertion [21] are the samples of physical level mechanisms. The skewing transition is part of the transistor level [20]. The approaches of physical level and transistor-level have more power consumption and area overhead than register transfer approaches. In the register transfer level, Error checking and correction (ECC) methods and Crosstalk Avoidance Codes (CACs) to avoid compliance are introduced. In [22], [23] and [24], some ECC-based methods are discussed. Among the coding methods CACs effectively are used to reduce the delay of crosstalk fault.

CACs prevent transition patterns to reduce the crosstalk delay. For this purpose, CACs encode a data word into a code word that lacks prohibition transitions. In one sense, CACs can be classified into two types of CACs with memory and memoryless. In memory-base CACs have to store all code words of codebooks because the encoding needs to the previously sent code word. In contrast, memoryless CACs encoding just belongs to the data word. Thus, the implementation of memoryless CACs is simpler [9]. The previous approaches like Forbidden Overlap Code (FOC) [25], Forbidden Transition Code (FTC) [26], Forbidden Pattern Code (FPC) [27], [28], [29], [30], [31], [32], One Lambda Code (OLC) [28] and Improved OLC (IOLC) [10] are memoryless CACs. FPC methods that do not have forbidden transition patterns are also called Forbidden Pattern Free (FPF). The [27] method is based on the fibonacci series numeral system. S2AP method provides another numerical system to prevent the occurrence of forbidden transition patterns in the 3-wire model, so that it is complete and unambiguous [29]. The PS-Fibo method provides another numerical system based on the fibonacci series of forbidden transition patterns in the 3-wire model [30]. ST-CAC coding is a numerical system-based method that uses ternary coding instead of binary coding and only considers the effects of capacitive coupling [33]. In [34], a Crosstalk Avoidance based Integer Coding (CAIV) technique is presented. The optimal mapping of data words and code words along with selective inversion of input signals minimizes the error rate in this coding technique.
These CACs consider only the capacitance coupling effect. However, in Same and Opposite Transitions Avoidance (SOTA) coding the effects of inductive coupling are considered alongside the effect of simultaneous capacitive coupling [9].

Some CACs are numerical based system methods. In these CACs, the data word is mapped to a code word without forbidden transitions/patterns using a numerical system. Prohibited transition patterns lead to crosstalk, so crosstalk fault can be avoided by preventing them. In numerical system-based CACs, the code word \((d_m d_{m-1} \ldots d_1)\) is generated in a \(m\)-bit communication bus using the numeric sequence \(\{f_i\}_{i=1}^m\) as \(\sum_{i=1}^{m} d_i f_i\). The data message sent by \(v\) can be in the range \([0, \sum_{i=1}^{m} f_i]\). Two features of a complete and unambiguous numerical system are important. The complete numerical system has one equivalent code word for each data word, so that all data can be encoded in it. They are also non-ambiguous, meaning that there is only one code word for each data word.

IOLC coding is a numerical system based method. Most previous work has focused on the effect of capacitive coupling. Meanwhile, IOLC coding is more accurate due to the use of the 5-wire model. Since the inductance is important in the design of high-performance circuits, coding has been adopted that considers the effects of inductive coupling as well as capacitive coupling. SOTA coding is also a method based on a numerical system that considers the effect of capacitive coupling and inductive coupling at the same time. SOTA coding for generating the code word depends on the input parameter \(P\) [9]. Also, the production of the numerical system in SOTA coding depends on several functions and therefore increases the amount of computational overhead in the encoder and decoder.

In the subject literature, approaches without a numerical system have also been presented to avoid crosstalk faults. In [35] and [36], encodings without a numerical system take into account the effects of capacitive coupling and prevent the occurrence of transitions with the greatest switching change which have used the 3-wire model. Therefore, the accuracy of these methods is lower than 5-wire models.

In this paper, a 5-wire model is used to increase the accuracy of coding, and a coding algorithm is proposed to avoid directional and opposite transitions so that by avoiding directional transition patterns the inductance coupling is avoided, and by avoiding opposite transitions capacitive coupling is prevented. For this purpose, a formula for calculating the smallest amount of code word without directional and opposite transition patterns is provided. Also, a positive non-decremental numerical system is presented that can be generated recursively from previous sequence numbers. The simulation results prove that the proposed coding algorithm using the proposed numerical system has a lower overhead area and less power consumption than the SOTA method. Since the proposed method jointly considers capacitive coupling and inductive coupling, it is called Joint Capacitive and Inductive CAC, JCI-CAC for short.

**III. PROPOSED METHOD: JOINT CAPACITIVE AND INDUCTIVE CAC (JCI-CAC)**

Numerical System coding methods for crosstalk fault avoidance that are employed for preventing the occurrence of forbidden transition patterns, map the transmitted data words to the code words which are free from forbidden transitions [27]. For this purpose, the transmitter requires an encoder circuit to map the data word as \(v\) to the code word as \((d_m, \ldots, d_2, d_1)\) where \(m\) is the width of the communication bus. The generated code word is obtained based on the numerical system \(\{U_i\}_{i=1}^m\) by the coding algorithm. The receiver requires a decoder circuit to perform inverse mapping. The decoder obtains the transmitted data word by obtaining the sum of the base coefficients in the code word as \(\sum_{i=1}^{m} d_i U_i\). The encoding/decoding process is shown in Figure 4. In Figure 4, the input/output is shown as a parallelogram and processing/operation is shown as a rectangle. The whole process from the start to the end is related to the encoding and decoding process. In Figure 4, the first rectangle shows the encoding process and the second rectangle shows the decoding process. Both encoder and decoder sides have the \(\{U_i\}_{i=1}^m\) numerical system and use it to perform encoding/decoding operations.

In CAC methods, to send data in the communication bus, they must be encoded so that the sent code word has no forbidden transitions. Forbidden transition patterns are determined by the transition classification model. It is necessary to determine the model of transition classification to design a coding method in the CAC algorithm. A CAC is presented in the 5-wire model, considering the effects of capacitive coupling and the effects of inductive coupling between communication bus wires. By directional transitions avoidance, inductive coupling is avoided. On the other hand, by opposite transitions avoidance, capacitive coupling is avoided. Therefore, the accuracy of this method is higher than other crosstalk avoidance coding. The inductance impact is also considered between the wires in the communication bus. As a result, code words generated in the provided CAC do not have the patterns 00000, 11111, 01010, and 10101. According to Table 2, patterns 00100 and 11011 also causes much severe inductance coupling effect. However, these patterns are not considered as forbidden patterns because they are in Class 4, while patterns 11111 and 00000 are in Class 5 as the worst cases delay.

To encode a data message, first, a numerical system is provided and then a coding algorithm using the corresponding numerical system is proposed so that each code word has no directional or reverse directional patterns. Encoder and decoder at the source and destination use a numerical system to encode/decode data word. Since the auxiliary functions in calculating the proposed numerical system have been omitted, the proposed method is called Joint Capacitive and Inductive CAC, JCI-CAC for short. JCI-CAC numerical system has two main features: completeness and unambiguity. JCI-CAC numerical system is complete so that all data words in display data range can be encoded with it.
meaning that there must be an equivalent code word for each data word. Also, it is unambiguous, meaning that there is only one equivalent code word for each data word. Using these two features, JCI-CAC numerical system has high accuracy in encoding data. It should be noted that the mapping algorithm provided by the relevant numerical system can be used to obtain complete code words in any width of the communication bus.

A mathematical relation is needed to generate the basis of JCI-CAC numerical system, which can be used to obtain the numerical system at different bus widths. All data sent in the communication bus is mapped to code words without any forbidden transition patterns using this numerical system. To reduce the computational overhead, a method for obtaining a numerical system in the m-bit bus as Eq (2) is proposed. According to Eq (2), auxiliary functions are no longer needed to compute the numerical system, and the proposed numerical system can be recursively generated by using series \( \{U_i\}_{i=1}^m \) such that \( m \) is the width of the communication bus.

\[
U_i = \begin{cases} 
1, & i = 1 \\
1, & i = 2 \\
2, & i = 3 \\
i, & i = 4 \\
U_{i-1} + U_{i-3}, & i = 5 \text{ and } m > 5, \\
U_{i-1} + U_{i-2} + U_{i-5}, & i = m \neq 5 \neq 7, \\
U_{i-1} + U_{i-2} + U_{i-4}, & i = m = 5 \text{ or } i = m = 7, \\
U_{i-2} + U_{i-3}, & \text{otherwise.}
\end{cases}
\tag{2}
\]

JCI-CAC numerical system can be generated recursively at different widths of the communication bus by Eq (2). The numerical system generated by Eq (2) in 5-bit to 10-bit bus is shown in Table 3. For example, according to Eq (2), the proposed numerical system for \( m = 8 \) (8-bit bus width) is \(147543211\) from the most valuable bit to the least valuable bit from left to right. It should be noted that the U numerical system in the mapping algorithm can be used to generate word ambiguous and complete code so that it lacks forbidden patterns.

In a binary numerical system as \( \sum_{i=d_i}^{m} d_i f_i \) where \((d_m, \ldots, d_2, d_1)\) is a binary string and \(f_m, \ldots, f_2, f_1\) is a basis set, the sent message can be represented as \(v \in [0, \Sigma_{i=m}^{m} f_i]\).

To prevent directional transitions, it is not possible to send a code word with all bits 0 or all bits 1 on the communication bus. Since all zero and all one patterns have been removed in this encoding, the minimum data word that can be sent in the \(k\)-bit bus, indicated by the \(P\) parameter, must be found. In this way, the value of \(P\) is added to data message \(v\) and the resulting number is encoded. Therefore, the range of the transmitted data is changed to \([P, P + \Sigma_{i=m}^{m} f_i]\) so that the parameter \(P\) is the first code word without the same direction and opposite direction patterns. Consider \(Min\) and \(Max\) functions to find the minimum and maximum data sent as Eq (3) and Eq (4), respectively, without the same-direction and opposite-direction transition patterns.

\[
Min_n = \begin{cases} 
(00011)_k, & n = 5k, \\
(00011)_k.0, & n = 5k + 1, \\
(00011)_k.00, & n = 5k + 2, \\
(00011)_k.000, & n = 5k + 3, \\
(00011)_k.00001, & n = 5k + 4,
\end{cases}
\tag{3}
\]

![FIGURE 4. General process of operation in numerical system based Crosstalk Avoidance Codes (CACs).](image-url)
As explained above, \(P\) value is added to solve the problem of sending all zero bits, therefore, to calculate it, the smallest acceptable code word must be obtained across each bus width. According to the \(Min\) function, \(P\) value in each \(m\)-bit bus can be calculated based on Equation (5). In this case, to calculate \(P\) value, \(Min\) function and \(g\) are calculated and added to the encoder and decoder. Using the \(Min\) function, the smallest transmissible data can be calculated as a \(P\) parameter. Where \(g(c_m) = \Sigma_{i=1}^{m} c_i U_i\). Therefore, \(P\) value is not an input of the encoding algorithm and prevents manual calculations and errors in its determination.

\[
P = g(\text{Min}_m)
\]  

(5)

After obtaining the \(\{U_i\}_{i=1}^{m}\) numerical system, it is necessary to encode the data word in the mapping algorithm in order to generate unambiguous code words without prohibited patterns using this numerical system in the algorithm. That is, by using the \(\{U_i\}_{i=1}^{m}\) numerical system in the algorithm, the code words without patterns 11111, 00000, 01010 and 10101 have been generated. In the following, the JCI-CAC coding algorithm is based on the relational calculations of Eq (6-9). Algorithm (1) is used to encode the transmitted message as \(d_m d_{m-1} \ldots d_1\). Based on Eq (6-9), \(\gamma_k\), \(\Theta\), \(\alpha_k\) and \(\beta_k\) values can be calculated [9].

For example, in a 5-bit bus, the minimum value of the transmitted data is \(P = 2\) according to Eq (6). The code words generated by Algorithm (1) are shown in Table 4. According to Table 4, none of the code words contain the forbidden patterns 10101, 01010, 11111 and 00000, and there is only one equivalent code word for all data words as \(v \in \{P, P + \Sigma_{i=1}^{m} U_i\}\). According to Table 4, none of the code words contain the forbidden patterns '10101', '01010', '11111', '00000'. Also, for all sendable data, \(v\) is there only one equivalent code word, which means that the generated code words generated from the numerical system and mapping algorithm are complete and unambiguous.

\[
\begin{align*}
\gamma_k &= U_k, \\
\Theta &= g(\text{Min}_{m-1}) + U_m, \\
\alpha_k &= g(\text{Max}_{k-1}) + 1, \\
\beta_k &= g(\text{Min}_{k-1}) + U_k
\end{align*}
\]  

(6), (7), (8), (9)

**Algorithm 1 Coding Dataword in JCI-CAC Method**

**Require:** code length \(m\), data message \(v\)

**Ensure:** \(d_m d_{m-1} \ldots d_1\)

1: \(P = g(\text{Min}_m)\)
2: \(v = v + P\)
3: \text{for} \(k = m\) down to 2 \text{do}
4: \text{if} \(k = m\) then
5: \quad \text{if} \(v \geq \Theta\) then
6: \quad \quad \(d_m = 1\)
7: \quad \text{else}
8: \quad \quad \(d_m = 0\)
9: \text{end if}
10: \(\gamma_m = v - d_m U_m\)
11: \text{else}
12: \quad \text{if} \(\gamma_{k+1} \geq \alpha_k\) then
13: \quad \quad \(d_k = 1\)
14: \quad \text{else if} \(\gamma_{k+1} < \beta_k\) then
15: \quad \quad \(d_k = 0\)
16: \quad \text{else}
17: \quad \quad \(d_k = d_{k+1}\)
18: \quad \text{end if}
19: \quad \(\gamma_k = r_{k+1} - d_k U_k\)
20: \text{end if}
21: \text{end for}
22: \(d_1 = \gamma_2\)

**Table 4. 5-bit codebook of JCI-CAC.**

| dataword \((v)\) | \(v + P\) | codeword |
|----------------|-----------|---------|
| 0              | 2         | 00011   |
| 1              | 3         | 00110   |
| 2              | 4         | 00111   |
| 3              | 5         | 01100   |
| 4              | 6         | 01110   |
| 5              | 7         | 10001   |
| 6              | 8         | 10011   |
| 7              | 9         | 11000   |
| 8              | 10        | 11010   |
| 9              | 11        | 11100   |

**IV. EXPERIMENTAL RESULTS**

In this paper, the Modelsim simulator tool [37] is used to verify the performance of the encoder and decoder in JCI-CAC method. Next, the Design Compiler [38] is used to synthesize encoder and decoder to generate related hardware. As a result, critical path delay, power consumption, and area overhead are measured in encoder and decoder units. In this section, the proposed methods are implemented and analyzed using Modelsim and Design Compiler tools and the evaluation results are presented.

This section evaluates the JCI-CAC coding method compared to other coding methods including SOTA, FPF, and IOIC codings. Both methods have been modeled using Verilog language to compare JCI-CAC method with SOTA coding and show the accurate assessment of area overheads, delay, and power consumption. In this step, the correct operation of the encoder and decoder is ensured. After ensuring
the correctness of the algorithm, with the help of Synopsys Design Compiler tool in 45nm technology, the encoder and decoder circuits have been modeled in both methods. To test both methods, 500 random data packets were generated to obtain the exact amount of delay, power consumption, and overhead of the encoder/decoder area. Since the numerical systems used in the JCI-CAC and SOTA methods are the same, their delay is reported to be the same. According to different simulation results, JCI-CAC method has improved area overhead and power consumption better than SOTA [9] coding method. In the following, each of these overheads is reviewed and compared.

### A. CRITICAL PATH DELAY OVERHEAD

As stated earlier, the numerical system is the same in both encoding methods. Therefore, it was predictable that the delay per encoder/decoder unit would be the same in both methods. The latency of the bus with different widths of 8-bit, 16-bit, and 32-bit is shown in Table 5.

### B. POWER CONSUMPTION OVERHEAD

In this section, the power consumption of JCI-CAC, SOTA, and FPF CACs is compared. Different FPF CACs called PS-Fibo [30], S2AP [29], Improved Fibo-CAC [28] and Fibo-CAC [27] have been studied. Simulation results in different widths are shown in Table 6. Due to the changes applied to the encoder and decoder to calculate the numerical system for encoding data packets, power consumption has been improved in JCI-CAC method.

According to Table 6, power consumption of JCI-CAC in the 8-bit and 16-bit bus is reduced by up to 20% compared to SOTA and FPF (PS-Fibo, S2AP, Improved Fibo-CAC, Fibo-CAC) codings. It also shows 42% reduction in power consumption in the 32-bit bus. The power consumption graph is also shown in Figure 5. A comparison of JCI-CAC power delay product (PDP) concerning SOTA, and FPF (PS-Fibo, S2AP, Improved Fibo-CAC, Fibo-CAC) codings is shown in Figure 6. Due to the high value of PDP in FPF(PS-Fibo, S2AP, Improved Fibo-CAC, Fibo-CAC) codings, the diagram in Figure 6 is drawn as two vertical values. The improvement of JCI-CAC PDP compared to SOTA CACs in 8-bit, 16-bit and 32-bit busses is 23%, 22%, and 46%, respectively.

### C. AREA OVERHEAD

Area overhead is one of the measurement criteria of CAC method. The area overhead is actually the area related to CAC, the amount of which has been checked in the proposed method compared to other CAC methods in different widths of the communication bus. Since CAC methods can be used in the communication bus with different widths, the area overhead has been measured in 8-, 16- and 32-bit widths.

In this section, the cell area overhead of JCI-CAC, SOTA, and FPF (PS-Fibo, S2AP, Improved Fibo-CAC, Fibo-CAC) methods is compared. The synthesis results of cell area overhead in JCI-CAC, SOTA, and FPF (PS-Fibo, S2AP, Improved Fibo-CAC, Fibo-CAC) codings are shown in Table 7. According to Table 7, cell area overhead in JCI-CAC compared to SOTA coding in 8-bit bus is reduced by 4.8%. On the other hand, cell area overhead has increased in the width of the communication bus by up to 3% in the 32-bit bus. It can be concluded that JCI-CAC performs better in lower width busses. A comparison diagram of cell area overhead in SOTA and JCI-CAC is shown in Figure 7. According to the experimental results of JCI-CAC compared to SOTA coding, in the 32-bit bus despite a minimum reduction of 20% in power consumption, 3% increase in cell area overhead is negligible.

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**TABLE 5. Critical delay(ns) overhead rate of JCI-CAC, SOTA, and FPF (PS-Fibo, S2AP, Improved Fibo-CAC, Fibo-CAC) codings.**

| Coding/Bus width | 8-bit | 16-bit | 32-bit |
|------------------|-------|--------|--------|
| JCI-CAC          | 0.1   | 0.1    | 0.1    |
| SOTA             | 0.1   | 0.1    | 0.1    |
| PS-Fibo          | 3.77  | 11.83  | 48.97  |
| S2AP             | 3.8   | 12.1   | 50.4   |
| Improved Fibo-CAC| 4.3   | 13.7   | 53.9   |
| Fibo-CAC         | 4.49  | 14.13  | 55.8   |

**TABLE 6. Power consumption (uW) overhead of JCI-CAC, SOTA, and FPF (PS-Fibo, S2AP, Improved Fibo-CAC, Fibo-CAC) codings.**

| Coding/Bus width | 8-bit | 16-bit | 32-bit |
|------------------|-------|--------|--------|
| JCI-CAC          | 131.96| 404.68 | 2430.14|
| SOTA             | 162.15| 489.19 | 2463.16|
| PS-Fibo          | 363.6 | 1089.5 | 1109.9 |
| S2AP             | 610.2 | 1518.2 | 11181.4|
| Improved Fibo-CAC| 660.33| 3343.3 | 15714.1|
| Fibo-CAC         | 691.65| 3454.8 | 15712.8|

**TABLE 7. Cell Area Consumption (mm²) of JCI-CAC, SOTA and FPF (PS-Fibo, S2AP, Improved Fibo-CAC, Fibo-CAC) codings.**

| Coding/Bus width | 8-bit | 16-bit | 32-bit |
|------------------|-------|--------|--------|
| JCI-CAC          | 241.33| 765.81 | 5532.01|
| SOTA             | 253.23| 763.15 | 5367.61|
| PS-Fibo          | 653.45| 1993.83| 9669.84|
| S2AP             | 668.45| 2008.83| 9664.84|
| Improved Fibo-CAC| 677.50| 2401.50| 10829.60|
| Fibo-CAC         | 685.2157| 2414.74 | 10529.60|

**FIGURE 5. Power consumption of codec in the presence of JCI-CAC concerning SOTA, and FPF (PS-Fibo, S2AP, Improved Fibo-CAC, Fibo-CAC) codings.**

**FIGURE 6. Cell area consumption of JCI-CAC, SOTA and FPF (PS-Fibo, S2AP, Improved Fibo-CAC, Fibo-CAC) codings.**

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The code rate on an \( m \)-bit bus is the number of \( k \) bits that can be displayed on \( m \) wire. The number of bits used in each bus width requires the size of CAC codebook. Consider \( C(m) \) the set of code words generated in each CAC as a codebook. Hence the code rate in the \( m \)-bit communication bus can be calculated according to \( k/m \). The cardinality of JCI-CAC can be displayed as Eq. (10). In the case without coding, it is possible to send \( 2^k \) data words on the communication bus with \( m \) wire. Due to the removal of prohibited patterns in CACs, some code words are not passed over the bus. As the cardinality of CAC increases, the number of code words that can be sent over the communication bus increases, which leads to a reduction in the extra wires to display the given data words \( 2^k \). Therefore, reducing redundant wires leads to a reduction in crosstalk fault on the wires.

\[
C_m = \begin{cases} 
10, & m = 5, \\
14, & m = 6, \\
18, & m = 7, \\
C_{m-2} + C_{m-3}, & m \geq 8, 
\end{cases} \tag{10}
\]

Figure 8 shows a comparison of code rate in JCI-CAC and IOLC codings. From the comparison, if \( m \) is small, the code rates difference between JCI-CAC and IOLC codings is quite small, and their area overhead is close to each other. In JCI-CAC, the number of bits that can be displayed on the \( m \) wire has increased as the communication bus width increases. This means that more wire usage is used to display more code words, which reduces the redundant wire.

D. INVESTIGATING THE OCCURRENCE OF INDUCTANCE CLASS PATTERNS

To investigate the effect of the proposed numerical system on reducing crosstalk fault effects, a simulation environment has been developed. According to the explanations of the previous sections, analysis of power consumption and wire delay is important, because these factors are affected by crosstalk fault. Various applications have been applied to generalize the results. As a result, the simulation is checked on real data. To examine the proposed method on real data, three standard criteria video streaming of the foreman, football2, and mobile3 have been used to obtain real repetitive patterns and transmission factors. A comparison of the occurrence rates of each pattern class on the 6 video input files mentioned is shown in Figure 9.

The occurrence of 5-wire transition patterns on 6 input files in two modes encoded by JCI-CAC and without encoding is shown in Figure 9. The delay of the class patterns increases from \( 0C \) to \( 5C \), respectively, from left to right of the diagrams in Figure 9. According to the diagrams, the incidence of \( 2C \) to \( 5C \) class patterns in JCI-CAC is zero due to the removal of patterns 00000 and 11111. Based on Figure 9, the incidence of Class patterns \( 2C, 3C, \) and \( 4C \) in JCI-CAC has been reduced by up to 26%, 11%, and 3% compared to
the uncoded method, respectively. The worst case 5C class patterns in JCI-CAC are reduced by about 0.15% compared to the codeless method.

The simulation results in the communication bus with different widths of 8-, 16-and 32-bits show that the delay rate of the JCI-CAC is the same as the SOTA. The delay of JCI-CAC is improved by 90% compared to FPF coding methods. The power consumption of JCI-CAC in the 8-bit and 16-bit bus is reduced by up to 20% compared to SOTA and FPF (PS-Fibo, S2AP, Improved Fibo-CAC, Fibo-CAC) codings. It also shows 42% reduction in power consumption in the 32-bit bus. The improvement of JCI-CAC PDP compared to SOTA CACs in 8-bit, 16-bit and 32-bit busses is 23%, 22%, and 46%, respectively.

According to the synthesis results, the cell area overhead in JCI-CAC compared to SOTA coding in 8-bit bus is reduced by 4.8%. On the other hand, cell area overhead has increased by increases in the width of the communication bus by up to 3% in the 32-bit bus. According to the experimental results of JCI-CAC compared to SOTA coding, in the 32-bit bus despite a minimum reduction of 20% in power consumption, 3% increase in cell area overhead is negligible. According to the simulation results, the occurrence of inductance class patterns the occurrence of class patterns 2C, 3C, and 4C in JCI-CAC is reduced by 26%, 11%, and 3%, respectively, compared to the uncoded method. The worst-case patterns of the 5C class in JCI-CAC are reduced by about 0.15% compared to the uncoded method.

According to the evaluation results, the power consumption of JCI-CAC framework has improved by at least 20% compared to SOTA coding. Therefore, imposed area overhead of 3% can be ignored due to the increase in coding calculations. Also, the reduction of the PDP criterion is at least 22% compared to the SOTA method.

One of the limitations of the proposed method is its equal delay compared to the SOTA method. However, due to the reduction of cell area overhead and power consumption compared to existing methods, it has valuable results.

V. CONCLUSION

Connection between chips become an important bottleneck in performance and energy consumption in chip design, when the design scale is reduced to nanometers. System performance is introduced under the reliability factor. Since the occurrence of errors and defects due to the crosstalk is one of the issues that jeopardize the reliability of chips and data in communication bus, it needs to be carefully studied. The proposed methods for crosstalk lead to delay, power consumption, and area overloads in the communication bus on the chip. Therefore, the imposed overhead on the chip is one of the important issues studied in the field of reliability. By reducing the scale of the devices to the nanometers, an important bottleneck in performance and power consumption in the chip design is the connection between the chips. In this regard, communication buses consume large energy and have high propagation delays in the design of deep
sub-micron on the chip. Hence, performance and energy consumption are affected by limiting factors such as physical connections on the chip. Today, various methods are offered to increase the reliability of chips, and coding methods to avoid crosstalk have efficient performance.

As a result, designers must look for methods with minimal overhead in order to achieve better performance in increasing reliability. In this paper, the following items were done to reduce the crosstalk fault: -Attempts to reduce computational overhead, power consumption, and area in the crosstalk avoidance coding methods, -Present an algorithm to generate a numerical system in the coding method, -Introduce a new algorithm to reduce computational overhead, -Analysis and evaluation of various overheads of new methods using Mod- elsim and Design Compiler tools.

The innovative idea of the proposed method is to provide a new numerical system and a new coding algorithm with minimum area overhead and power consumption, taking into account inductance coupling in addition to capacitive coupling. Considering the importance of inductance coupling in the future, its effects cannot be ignored. Since in the subject literature, few methods have addressed the effects of inductance coupling along with capacitive coupling, the results obtained in the proposed method are significant.

VI. FUTURE WORK

This research can be used to provide a suitable platform for sending data in different versions of the communication bus between the chips with the minimum overhead delay, power consumption, and area. Here are some other suggestions for this line of research:

- Check negative numbers to create a numerical system in presenting CACs.
- Encryption of transmitted data by adding control bit to eliminate transition patterns with maximum delay.
- Presenting solutions to avoid crosstalk faults in 3D chips.

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