Low-temperature activation under 150°C for amorphous IGZO TFTs using voltage bias

Heesoo Lee, Ki Soo Chang, Young Jun Tak, Tae Soo Jung, Jeong Woo Park, Won-Gi Kim, Jusung Chung, Chan Bae Jeong and Hyun Jae Kim

aSchool of Electrical and Electronic Engineering, Yonsei University, Seoul, Republic of Korea; bDivision of Scientific Instrumentation, Korea Basic Science Institute, Daejeon, South Korea

ABSTRACT

Proposed herein is a new technique of activation for the backplane of low-temperature amorphous indium gallium zinc oxide thin-film transistors (a-IGZO TFTs) by applying a bias voltage to gate, source, and drain electrodes and simultaneously annealing them at 150°C. This ‘voltage bias activation’ can be an effective method of reducing the backplane processing temperature from 300°C to 150°C. Compared with the reference a-IGZO TFTs fabricated at 300°C, the a-IGZO TFTs fabricated through voltage bias activation showed sufficient switching characteristics: 10.39 cm²/Vs field effect mobility, 0.41 V/decade subthreshold swing, and $3.65 \times 10^7$ on/off ratio. These results were analyzed thermodynamically using infrared micro-thermography. In the case of the positive gate voltage bias condition, the maximum temperature of the a-IGZO channel increased to 48°C, and this additional annealing effect and activation energy lowering compensated for the insufficient thermal energy of annealing at a low temperature (150°C). With this approach, a-IGZO TFTs were successfully fabricated at a low temperature.

ARTICLE HISTORY

Received 30 November 2016
Accepted 10 April 2017

KEYWORDS

Voltage bias; InGaZnO thin-film transistors; Joule heating; activation; flexible display

1. Introduction

Amorphous indium gallium zinc oxide thin-film transistors (a-IGZO TFTs) have gained international attention for the backplane technologies of the next-generation flexible displays since Hosono et al. first published a paper about ‘In-Ga-Zn-O TFTs’ in 2004 [1]. This is because a-IGZO TFTs are promising alternatives to the hydrogenated amorphous silicon (a-Si:H) TFTs due to their many advantages, such as a lower deposition temperature and higher field effect mobility compared to those of the a-Si TFTs [2–4].

The a-IGZO TFTs fabricated by the sputtering process, however, have an issue: defect sites can be generated in oxide films by high-energy target ions and the incorporation of Ar+ ions during the sputtering process [5–8]. To alleviate the defect sites of a deteriorated film and to obtain sufficient switching properties, a-IGZO TFTs have required an annealing activation process at a high temperature over (300°C) after the deposition of a-IGZO active layers [9,10].

The thermal treatment at a high temperature, however, is not suitable for the formation of a-IGZO TFTs on a flexible polymer substrate, which generally has a low glass transition temperature [11,12]. Therefore, it is essential to develop a low-temperature fabrication process to solve the problem and to ultimately realize ideal flexible electronics.

Demonstrated herein is a low-temperature activation technique for a-IGZO TFTs by applying voltage bias to electrodes under 150°C. The electrical characteristics of a-IGZO TFTs activated with voltage bias are also investigated. Furthermore, the mechanisms of voltage bias activation are discussed based on the thermodynamic analysis of the a-IGZO TFTs using infrared micro-thermography.

2. Experiments

2.1. Fabrication of a-IGZO TFTs

a-IGZO TFTs with an inverted staggered structure were fabricated on a heavily doped p-type Si wafer with 120-nm-thick thermally grown SiO2. The a-IGZO active layer was deposited through radio frequency sputtering on a cleaned Si substrate using an IGZO target ($\text{In}_2\text{O}_3\cdot\text{Ga}_2\text{O}_3\cdot\text{ZnO} = 1:1:1$ mol%) at room temperature for 5 min, and the thickness of the resulting a-IGZO
The active layer was 40 nm. 200-nm-thick aluminum source and drain electrodes were deposited via thermal evaporation. The channel region was defined with a width (W) of 1000 μm and a length (L) of 150 μm.

Figure 1(a) shows the schematic of the a-IGZO TFTs with an inverted staggered structure and voltage bias activation. For the fabrication of the conventional thermally activated a-IGZO TFTs that were used for reference, the devices were annealed at 300°C for 1 h in ambient air after the deposition of an active layer and source/drain electrodes. In the case of voltage bias activation, constant DC voltages were applied to the gate, source, and drain electrodes of the a-IGZO TFTs, respectively. The samples were annealed at 150°C with different gate voltage (V_G) bias conditions: V_G = −100, 0, and +100 V. The source voltage (V_S) and drain voltage (V_D) were fixed: V_S = 0 V and V_D = 10.1 V, respectively. A photograph of the voltage bias activation process is shown in Figure 1(b).

2.2. Electrical measurements

The electrical characteristics of the devices were measured in a dark box under ambient conditions, using a semiconductor parameter analyzer (HP 4156C; Hewlett Packard, Palo Alto, CA). a-IGZO TFT measurements were carried out by inducing a gate voltage (V_GS) sweep from −30 to +30 V and a drain voltage (V_DS) of 10.1 V. High-resolution infrared micro-thermography analysis was performed to study the local-heating effect of a-IGZO TFTs.

3. Results and discussion

3.1. Electrical and infrared micro-thermography analysis of the voltage-bias-activated TFTs

Figure 2(a) shows the transfer characteristics of the a-IGZO TFTs annealed at various temperatures (100, 150, 200, 250, and 300°C) for 1 h. The reference a-IGZO TFT annealed at 300°C shows sufficient transfer characteristics (e.g., field effect mobility (μ_FET), on/off current ratio) as it is recognized that thermal annealing at a high temperature (~300°C) is important to control the properties of a-IGZO TFTs.

Figure 2(b) shows the transfer characteristics of the a-IGZO TFTs fabricated with voltage bias activation. The optimized sample shows similar electrical characteristics in spite of a lower process temperature (150°C) compared to the reference one (300°C), and the optimized conditions were V_G = +100 V and time = 1 h. The electrical parameter values of the reference and optimized samples, including the μ_FET, on/off current ratio, V_on, subthreshold swing (SS), and maximum trapped charge density (N_{max}), are arranged in Table 1. The μ_FET was obtained from the I_DS − V_DS curves in the saturation

Figure 2. Transfer characteristics of the a-IGZO TFTs (a) annealed at 100, 150, 200, 250, and 300°C on a hot plate for 1 h; (b) with V_G = −100, 0, and +100 V.
Table 1. Summary of the device electrical parameters, including the $\mu_{\text{FET}}$, on/off current ratio, $V_{\text{on}}$, SS, and $N_{\text{max}}$, for the reference and voltage-bias-activated a-IGZO TFTs.

| Sample         | Annealing temperature (°C) | Process time (h) | $V_G$ (V) | $V_S$ (V) | $V_D$ (V) | $\mu_{\text{FET}}$ (cm$^2$/Vs) | $I_{\text{on}}/I_{\text{off}}$ ratio | $V_{\text{on}}$ (V) | SS (V/decade) | $N_{\text{max}}$ (cm$^{-3}$) |
|----------------|-----------------------------|------------------|-----------|-----------|-----------|-------------------------------|---------------------------------|--------------------|----------------|----------------|
| Reference      | 300                         | 1                | –         | –         | –         | 9.59                          | 1.61 x 10$^7$                  | –1.40              | 0.39           | 9.85 x 10$^{11}$ |
| Voltage bias   | 150                         | 1                | +100      | 0         | +10.1     | 10.39                         | 3.65 x 10$^7$                  | 0.20               | 0.41           | 1.05 x 10$^{12}$ |

region ($V_{DS} \geq V_{GS} - V_T$) using the equation below.

$$I_{\text{DS}} = \frac{w}{2L} C_i \mu_{\text{FET}} (V_{GS} - V_T)^2,$$  \hspace{1cm} (1)

where $C_i$ and $V_T$ denote the gate capacitance and threshold gate voltage, respectively.

In the case where $V_G$ is $-100$ V, insufficient carriers were accumulated in the a-IGZO channel because of the repulsive force between the negative $V_G$ and the electron carriers. If $V_G$ is 0 V, it cannot attract as many electron carriers to the a-IGZO channel as when $V_G$ is +100 V. A +100 V $V_G$, however, can attract sufficient electron carriers in the a-IGZO channel through the attractive force between the positive $V_G$ and the electron carriers. The sufficient electron carriers generate Joule heating at the a-IGZO channel region during voltage bias activation [13–15] because heat is produced when an electric current flows through a conductor, which is known as Joule heating, and because the amount of heat is proportional to the current flowing according to Joule’s first law [16].

A +100 V $V_G$, however, can attract sufficient electron carriers in the a-IGZO channel through the attractive force between the positive $V_G$ and the electron carriers. The sufficient electron carriers generate Joule heating at the a-IGZO channel region during voltage bias activation [13–15] because heat is produced when an electric current flows through a conductor, which is known as Joule heating, and because the amount of heat is proportional to the current flowing according to Joule’s first law [16].

The aforementioned electrical analysis results are in agreement with the infrared micro-thermography analysis results, as shown in Figure 3 [17]. When voltage bias was applied, the maximum temperature increase ($\Delta T_{\text{max}}$) of the a-IGZO channel differed depending on the polarity of $V_G$. As shown in Figure 3(b), $\Delta T_{\text{max}}$ increased up to 48°C with $V_G = +100$ V. In contrast, as shown in Figure 3(c), $\Delta T_{\text{max}}$ was only 12°C when $V_G = -100$ V. It was clearly observed that $\Delta T_{\text{max}}$ decreased along with $V_G$. This was because the amount of Joule heat increased with the drain current, which originated from $V_G$ in accordance with Equation (1). A more positive $V_G$ attracts more electron carriers and generates more Joule heat. When $V_G = 0$ V, it does not attract electron carriers, resulting in less Joule heat compared to the positive $V_G$. A negative $V_G$ repulses electrons and generates the minimum Joule heat among the positive, zero, and negative $V_G$.

The effect of voltage bias activation, however, cannot be explained by Joule heating alone because in this study, the Joule heating increased the $\Delta T_{\text{max}}$ of the a-IGZO channel to 48°C, and the 198°C total thermal energy that resulted from the simultaneous annealing at 150°C was insufficient to activate a-IGZO TFTs, as shown in Figure 2(a).

The a-IGZO film is composed of many electrons, protons, and ions of indium, gallium, zinc, and oxygen. The charged particles experience attractive or repulsive forces from the applied voltage bias according to the Coulombic interaction. It is generally known that the energy states of atoms and molecules are unstable, and that the probability of reaction increases when an external electric-field is induced in the oxide system [18]. The initial energy state of the a-IGZO film increases, and the film is likely to react and improve its weak chemical bonds by overcoming the activation energy barrier. In this situation, relatively lower thermal energy is required to overcome the activation energy barrier compared to the conventional activation process. That is, the voltage bias is not

![Figure 3](image-url) Infrared micro-thermography results. (a) Optical-microscope image of an a-IGZO TFT. Temperature distribution of an a-IGZO TFT applying voltage bias under (b) $V_G = +100$ V and (c) $V_G = -100$ V.
only the carrier source for Joule heating but is also the activation promotion process even at a low temperature (198°C) by driving the electric-field-induced molecules or atoms. Therefore, the voltage bias activation in this study can be achieved by Joule heating and by lowering the activation energy.

4. Conclusion
A new technology was developed to activate the a-IGZO TFTs at 150°C using electrical and thermal energy. In this study, with voltage bias, concurrent electrical and thermal treatment activated the a-IGZO TFTs at a low temperature, and caused it to exhibit superior electrical characteristics. By controlling $V_G$, the electron carriers in the channel and drain currents can be controlled. Joule heating occurs with the drain current flow, and the $\Delta T_{\text{max}}$ of the a-IGZO channel increases along with $V_G$. In addition, the applied voltage bias reduces the activation energy. The electrical energy compensates for the insufficient thermal energy at a low temperature (150°C), and the annealing temperature was decreased without degrading the electrical characteristics compared to the reference TFTs.

Disclosure statement
No potential conflict of interest was reported by the authors.

Funding
This work was supported by Samsung Display and Korea Evaluation Institute of Industrial Technology (KEIT) funded by the Ministry of Trade, Industry, & Energy (MOTIE, Korea) [grant no. 10063038].

Notes on contributors
Heesoo Lee is currently pursuing a Ph.D. degree at the School of Electrical and Electronic Engineering of Yonsei University in Seoul, South Korea. She has been researching on thin-film transistors and the resistive random access memory based on metal oxide materials.

Ki Soo Chang received his Ph.D. degree from Gwangju Institute of Science and Technology in 2007. He is currently a principal researcher at the Division Scientific Instrumentation, Korea Basic Science Institute. His current research interests include the development of a thermal imaging microscope for semiconductor device applications and nano-biophotonic imaging systems for biomedical applications.

Young Jun Tak is currently pursuing a Ph.D. degree at the School of Electrical and Electronic Engineering of Yonsei University in Seoul, South Korea. He has been researching on thin-film transistors and the resistive random access memory based on metal oxide materials.

Tae Soo Jung is currently pursuing a Ph.D. degree at the School of Electrical and Electronic Engineering of Yonsei University in Seoul, South Korea. He has been researching on thin-film transistors based on metal oxide materials.

Jeong Woo Park is currently pursuing a Ph.D. degree at the School of Electrical and Electronic Engineering of Yonsei University in Seoul, South Korea. He has been researching on thin-film transistors based on metal oxide materials.

Won-Gi Kim is currently pursuing a Ph.D. degree at the School of Electrical and Electronic Engineering of Yonsei University in Seoul, South Korea. He has been researching on thin-film transistors based on metal oxide materials.

Jusung Chung is currently pursuing an M.S. degree at the School of Electrical and Electronic Engineering of Yonsei University in Seoul, South Korea. He has been researching on thin-film transistors based on metal oxide materials.

Chan Bae Jeong received his M.S. Optoelectronics & Physics degree from Ulsan University, Ulsan, South Korea in 2015. He is currently a researcher at Korea Basic Science Institute. He has been conducting research on infrared micro-thermography, photothermal deflection spectroscopy, and local heat distribution analysis in the research center.

Hyun Jae Kim received his Ph.D. degree from the Department of Materials Science and Engineering of Columbia University in New York, NY, USA in 1996. He has been a professor at the School of Electrical and Electronic Engineering of Yonsei University in Seoul, South Korea since 2005.
References

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, Nature. 432, 488 (2004).
[2] S.J. Heo, D.H. Yoon, T.S. Jung, and H.J. Kim, J. Inf. Disp. 14, 79 (2013).
[3] M. Nag, R. Muller, S. Steudel, S. Smout, A. Bhoolokam, K. Myny, S. Schols, J. Genoe, B. Cobb, A. Kumar, G. Gelinck, Y. Fukui, G. Groeseneken, and P. Heremans, J. Inf. Disp. 16, 111 (2015).
[4] K.M. Kim, W.H. Jeong, D.L. Kim, Y.S. Rim, Y. Choi, M.-K. Ryu, and K.-B. Park, H.J. Kim, IEEE Electr. Dev. Lett. 32, 1242 (2011).
[5] Z.W. Zheng, C.H. Cheng, and Y.C. Chen, ECS J. Solid State Sci. Technol. 2, N179 (2013).
[6] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, and H. Kumomi, Appl. Phys. Lett. 89, 112123 (2006).
[7] R.C. Ross and R. Messier, J. Appl. Phys. 52, 5329 (1981).
[8] H.-K. Noh, K.J. Chang, B. Ryu, and W.-J. Lee, Phys. Rev. B 84, 115205 (2011).
[9] Y.J. Tak, S.P. Park, T.S. Jung, H. Lee, W.-G. Kim, J.W. Park, and H.J. Kim, J. Inf. Disp. 17, 73 (2016).
[10] T. Kamiya, K. Nomura, and H. Hosono, J. Disp. Technol. 5, 468 (2009).
[11] C. Wang, D. Hwang, Z. Yu, K. Takei, J. Park, T. Chen, B. Ma, and A. Javey, Nat. Mater. 12, 899 (2013).
[12] T. Sekitani and T. Someya, Adv. Mater. 22, 2228 (2010).
[13] J.-S. Ro and W.-E. Hong, Jpn. J. Appl. Phys. 45, L1142 (2006).
[14] W.-E. Hong, J. Chung, D. Kim, S. Park, and J.-S. Ro, Appl. Phys. Lett. 96, 052105 (2010).
[15] D.H. Kim, W.E. Hong, W.S. Ro, S.H. Lee, and S. Park, Vacuum 85, 847 (2011).
[16] A.M. Prokhorov, Joule–Lenz law. Great Soviet Encyclopaedia (1972).
[17] K.S. Chang, S.C. Yang, J.-Y. Kim, M.H. Kook, S.Y. Ryu, H.Y. Choi, and G.H. Kim, Sensors 12, 4648 (2012).
[18] J.S. Langer, Ann. Phys. 54, 258 (1969).