ABSTRACT

As the application of deep learning continues to grow, so does the amount of data used to make predictions. While traditionally, big-data deep learning was constrained by compute performance and off-chip memory bandwidth, a new constraint has emerged: privacy. One solution is homomorphic encryption (HE). Applying HE to the client-cloud model allows cloud services to perform inference directly on the client’s encrypted data. While HE can meet privacy constraints, it introduces enormous computational challenges and remains impractically slow in current systems.

This paper introduces Cheetah, a set of algorithmic and hardware optimizations for HE DNN inference to achieve plaintext DNN inference speeds. Cheetah proposes HE-parameter tuning optimization and operator scheduling optimizations, which together deliver 79$\times$ speedup over state-of-the-art. However, this still falls short of plaintext inference speeds by almost four orders of magnitude. To bridge the remaining performance gap, Cheetah further proposes an accelerator architecture which, when combined with the algorithmic optimizations, approaches plaintext DNN inference speeds. We evaluate several common neural network models (e.g., ResNet50, VGG16, and AlexNet) and show that plaintext-level HE inference for each is feasible with a custom accelerator consuming 30W and 545mm$^2$.

Table 1: Generalization of privacy-preserving techniques.

| Solution | Security   | Limitation                           |
|----------|------------|--------------------------------------|
| Local    | System     | Edge performance; leaks model        |
| TEE      | System     | Performance; side-channels            |
| DP       | Statistical| Applications; utility-privacy tradeoff|
| MPC      | Cryptographic| Communication bandwidth               |
| HE       | Cryptographic| Compute                              |

deliver security via system implementation or mathematical guarantees. Implementation-based methods include (i) moving computation to edge devices, i.e., local computation [54,68], and (ii) trusted execution environments (TEEs), e.g., SGX [10,15,59]. Both methods achieve security by monitoring and restricting data usage via a combination of software and hardware implementations. In contrast, methods offering provable mathematical guarantees provide a theoretically-quantifiable level of privacy. Such solutions include (i) differential privacy (DP) [4,13,18,21], (ii) secure multi-party compute (MPC) [32,36,48,49], and (iii) homomorphic encryption (HE) [7,28,31,53]. Table 1 summarizes the techniques and limitations associated with each with respect to wide-scale deployment.

Each of the above solutions have differing limitations. Local execution offers individual users improved security, but there is risk of sensitive information leaking or being stolen through the model, plus model-privacy concerns for service providers [60]. TEEs have been shown to be vulnerable to side-channel attacks [15]. DP offers statistical privacy levels quantified via privacy loss $\epsilon$ but imposes an abstruse trade-off between $\epsilon$ and data utility [20]. Moreover, while DP has seen success in training [12,45], its application to inference is an open question. MPC also delivers cryptographically-strong privacy guarantees. However, MPC performance is limited by communication bottlenecks [36,40,49], which require consideration of network-protocol and technology levels, or reformulating the algorithm itself to alleviate.

This paper focuses on homomorphic encryption (HE) to enable privacy-preserving deep learning inference, or HE inference. The key strength of HE is that it offers cryptographically-
strong privacy guarantees, but these guarantees come at the cost of massive computational overheads. These overheads are so high that existing state-of-the-art implementations of HE inference [28][31][53] are still five to six orders of magnitude slower than plaintext inference. To put this in perspective, the current state-of-the-art HE inference solution (Gazelle [32]) takes 800ms for a single MNIST inference. These computational overheads are so extreme that prior research has yet to consider modern datasets and models, e.g., ImageNet and ResNet50, as even MNIST is currently beyond the realm of feasibility. In this paper, we propose a three-part algorithm-hardware co-design to demonstrate that the six order-of-magnitude performance gap in the state-of-the-art can be overcome.

High-performance HE inference requires addressing three key challenges. First, at the algorithmic level, HE has configurable parameters that trade performance (i.e., HE operator latency) and “computational budget,” canonically known as the noise budget in HE literature. This HE noise budget limits the amount of computation (i.e., number of HE operations) that can be applied to encrypted data while still allowing correct decryption. Aggressive HE parameter setting improves performance by reducing the cost of each operation (e.g., using smaller data types), but if set too aggressively, the noise budget can be exceeded and cause the computation (i.e., decryption) to fail. The second challenge is how computations are scheduled and mapping to HE primitives. HE only supports a limited set of operators (e.g., add and multiply) that applications must be expressed as, and each operator increases noise differently. Therefore, noise-aware operator schedules can significantly improve performance by reducing accumulated noise, enabling more aggressive HE parameters to be used. The final challenge is the sheer number of computations HE inference entails. As we show, this challenge requires hardware acceleration and leveraging the extreme degrees of parallelism in both DNNs and HE operators to maximize performance.

Key Contributions: To address these challenges, this paper presents Cheetah, a framework (Figure 1) to enable practical HE-based privacy-preserving machine learning inference by combining algorithm optimization and custom hardware acceleration. We assume Gazelle [32] as our state-of-the-art baseline. Our contributions are as follows:

First, we propose HE-PTune (Section 4), which is an analytical model that tunes HE parameters at the algorithm level. HE-PTune automatically identifies the highest-performance HE parameter settings that satisfy noise-budget constraints by tuning HE parameters based on the needs of each layer in a deep neural network model. HE-PTune’s parameter tuning yields up to 11.7 × for VGG16 and 5.5 × for ResNet50 performance benefit over state-of-the-art.

Second, we propose a new schedule for dot product operations called Sched-PA to minimize consumption of the noise budget and improve performance in HE. Sched-PA is a partial-aligned dot product schedule, which exploits the key insight that the order of HE operations significantly impacts performance and noise budget. This allows Sched-PA to achieve a maximum additional speedup of 10.2 × (5.20 × harmonic mean) and a combined speed using HE-PTune of 79.6 × (13.5 × harmonic mean) over state-of-the-art.

Third, we propose a custom hardware accelerator architecture that combines these algorithmic optimizations to approach plaintext speeds for privacy-preserving HE inference given the abundance of parallelism and opportunities for specializations. To do this, we first conduct hot kernel profiling of an HE software implementation [55] to derive the speedups necessary to achieve plaintext inference speeds using parameters identified by HE-PTune and Sched-PA. We also identify the amount of application inter-kernel and intra-kernel parallelism available in hot kernels. We then use these profiling results to implement a custom accelerator architecture for HE inference and conduct design space exploration for each HE kernel to measure speedups afforded by exploiting exposed parallelism.

By combining algorithmic optimizations with large-scale custom hardware acceleration, Cheetah approaches speeds comparable to plaintext deep learning inference. Compared to Gazelle, our system is five to six orders of magnitude faster. For ResNet50, we find accelerator hardware requirements on the order of 545mm² and 30W in a 5nm technology node (Section 7). More importantly, we find that the accelerator area and power resources required to support HE inference at these speeds is within practical (albeit still high) resource requirements which is still on the order of a large datacenter-class GPU or similar coprocessor.

2. OVERVIEW AND ASSUMPTIONS

2.1 System Setup

A typical deep learning system setup is shown in the gray box of Figure 1. A client generates data and sends it to the cloud. The cloud performs inference and the result is returned to the client. The most direct way to apply HE is for the client to encrypt the data, the cloud processes the entire inference using HE, and the encrypted result is returned to the client. Unfortunately, this approach has two drawbacks: (1) HE cannot readily process nonlinear functions (without incurring prohibitively large penalties) and (2) many computations in DNNs requires a relatively large HE noise budget, which necessitates larger encryption parameters, resulting in poor performance. This effect is exacerbated by deeper networks.

A recently proposed system, called Gazelle [32], shows how multi-party computation (MPC) can resolve the aforementioned nonlinear and HE noise budget challenges. The
main performance improvement of Gazelle over HE-only solutions comes from the observation that widely used activation functions in deep learning such as ReLU or MaxPool can be represented efficiently using Boolean circuitry, securely computed using Yao’s garbled circuits (GC) that incur small computational overhead [5][66].

In Gazelle, the client encrypts data to be processed and sends it to the cloud. The cloud applies a single linear layer (e.g., convolution) to the input using HE. ReLU and pooling functions are computed on the client using a GC. The GC is configured by the client and sent to the client along with the encrypted linear layer outputs. The client then decrypts the outputs and processes them using the GC. Note that allowing the client to observe the original outputs after decryption can leak the cloud’s private model weights (knowing the inputs and outputs of a linear function would make it trivial to steal the cloud’s model). To prevent this, the cloud obscures the actual activation values (both input and output) by adding random numbers to each, i.e., the client receives encrypted activation input also obfuscated with random numbers. After decryption, the client runs the GC, which includes a subtraction circuit to remove the added random numbers securely (recovering original values), an activation unit (ReLU or pooling), and finally and additionally to obscure the plaintext output value and protect model weights. Once GC evaluation completes, the masked output is re-encrypted by the client and sent to the cloud. On the cloud, the random numbers added to the activation are removed via HE subtraction and the following linear layer is computed (using HE). The HE-MPC cycle repeats for each layer of the deep network.

Note that in homomorphic encryption, decryption resets the HE noise budget. Therefore, the Gazelle system addresses both issues associated with nonlinear computation and limitations of HE noise budget. However, the computational overheads of HE—the focus of this paper—remain prohibitive. Gazelle is an instance of a more general class of privacy-preserving solutions combining multiple techniques (e.g., [36][40][44][52]). Gazelle addresses the HE compute bottleneck, which is an architecture/hardware problem, but the proposed optimizations for HE are more generally applicable to other solutions beyond Gazelle. Solving the communication/network bottleneck is beyond the scope of this paper. We expect contributions on the algorithmic (e.g., different MPC protocols [23][41][44]) and technology (e.g., 5G) front to help.

### 2.2 Threat Model

The threat model assumed by Cheetah is the same as in Gazelle [52], and similar to other two-party compute (2PC) solutions including DeepSecure [49], MiniONN [36], and SecureML [40]. This model assumes the client/user and cloud are honest but curious, i.e., each agent follows the protocol precisely but may try to infer information. Under this assumption, Cheetah optimizes the protocol preserving the privacy of both the clients’ data and cloud’s model weights. For more details, see [52].

Note that the protocol does leak some information about the model. Because ReLU and pooling layers are performed by the client, the client can learn the number and shape of each layer. The model weights values, however, are not leaked. It is possible to obscure this information (e.g., pad tensor dimensions and add null layers), but they are not considered here and left as future work. Cheetah focuses on improving users privacy while protecting the cloud’s models (considered IP today [67]) from model-stealing attacks [60].

### 3. BACKGROUND

This section provides a brief introduction to HE and the BFV [22] construction used by Cheetah. For a complete technical description see [8][22].

#### 3.1 Homomorphic Encryption: The Basics

HE is a privacy-preserving encryption technique that enables computation over encrypted data, which was first shown to be possible by Gentry [24]. Since its discovery, many algorithmic improvements have been made to improve performance [6][8][9][22][25][26][27]. Modern HE schemes such as BFV allow adds and multiplies between encrypted data and derive security from the hardness of the Ring Learning With Error (RLWE) problem [37]. In BFV, noise is added during plaintext encryption and accumulates over successive ciphertext computations. If the aggregate noise exceeds a noise budget threshold, decryption fails. This noise budget is a function of the HE parameters and defines how many computations can occur before decryption fails. HE schemes of this type are called Leveled HE (LHE). In contrast, fully homomorphic encryption (FHE) schemes enable an arbitrary number of computations. FHE schemes can be built from LHE schemes via bootstrapping [22][24]. Bootstrapping reduces the noise in the ciphertext but is expensive to implement, so most applications focus on LHE.

#### 3.2 BFV: Relatively Efficient HE

BFV [22] is a relatively efficient LHE scheme; Figure 2 shows an overview of the process. In BFV, data is encoded
TABLE 3: Impact on Noise of basic BFV operations.

| Noise (w) in fresh ct₀ | HE_Add (ct₀, ct₁) | HE_Mult (pt, ct₀) | HE_Rotate (ct₀) |
|------------------------|------------------|------------------|-----------------|
| 2ⁿ²⁺² (8 = 6σ)        | ν₀ + ν₁ (additive) | n⁻¹l₀W_{dcmp}ν₀/2 (multiplicative) | ν₀ + l₀A_{dcmp}B₀/2 (additive) |

as a plaintext polynomial that is then encrypted as a pair of ciphertext polynomials. Ciphertexts are then input to addition and multiplication during evaluation. The resulting ciphertexts from evaluation are decrypted to plaintext and finally decoded to individual scalars. Polynomials are implemented as integer vectors, where the vector length (polynomial degree) and bit-width (coefficient size) are set by HE parameters. BFV parameters (listed in Table 2) must be carefully tuned as they affect computational efficiency and security.

Core BFV Parameters (n, t, q): Plaintext polynomials are elements of the ring: $Rₙ = \mathbb{Z}_q[x]/(x^n + 1)$, where the degree of the polynomial is less than $n$ (a power of 2). Polynomial coefficients are integers in $\mathbb{Z}_t$ (integers in the range $(-\frac{t}{2}, \frac{t}{2})$). $t$ is called the plaintext modulus as all HE operations are taken modulo $t$ in the plaintext space. Setting $t$ requires profiling the application to ensure enough bits are used for correctness and no more, as over provisioning causes unnecessary slowdown.

Similarly, two polynomials of a ciphertext are in $R_q = \mathbb{Z}_q[x]/(x^n + 1)$, where $q$ is the ciphertext modulus. The ratio between $q$ and $t$ determines the noise budget, which sets the number of HE operators that can be computed per ciphertext before decryption fails. The ratio between $n$ and $q$ for a given variance ($σ^2$) of Gaussian noise added for encryption sets the security strength of the HE scheme (see 22 for details).

Encoding (Packing) Data to Polynomial: When proper HE parameters are used (i.e., $t$ is prime and $t \equiv 1 \mod 2n$), a property of the ring $Rₙ$ enables a form of algorithmic parallelism. Here, each plaintext polynomial in $Rₙ$ and, hence, the ciphertext, can be packed with $n$ data. This means that each HE addition or multiplication can actually perform an $n$-way parallel element-wise computation. With packing, each scalar data is tied to a slot, and slots can be thought of as individual elements in the integer array. Packing significantly improves HE performance; $n$ is typically on the order of thousands and the benefits of packing are proportional 58.

Polynomial Representations: Polynomials are represented in two spaces—coefficient and evaluation. The coefficient representation is how polynomials are typically represented, e.g., $\sum_{i=0}^{n-1} α_{i}x^i$. The evaluation space is analogous to the frequency domain of time-domain signals. Similar to FFT, efficient conversion between the two is done via the Number Theoretic Transform (NTT) 59,58. Cheetah keeps polynomials in the evaluation space and converts to coefficient space only as needed for operations like decomposition (see below). Using the evaluation space as a default representation reduces the number of NTTs needed for homomorphic CNN/FC. Note that applying NTT to ciphertexts does not affect noise.

3.2.1 Operations of BFV

BFV consists of three operators: HE_Add, HE_Mult, and HE_Rotate. Recall that the HE_Add and HE_Mult operate on vectors of packed data, so they are effectively SIMD-add and SIMD-multiply operations. Note that the underlying implementations of HE_Add and HE_Mult consist of many modular arithmetic calculations, different from a single cycle integer add or multiply computation. Table 3 shows the amount of noise introduced by each operator which depend on BFV parameters. $B$ is the bound of the noise added during encryption while $v$ represents the noise in ciphertext $ct$.

The remaining parameters ($l_w$, $l_{ct}$, $W_{dcmp}$, and $A_{dcmp}$) are for decomposition, defined in Section 3.2.2.

HE_Add: Two ciphertexts can be added homomorphically by summing each ciphertext coefficient followed by a modulo operation. I.e., a resulting coefficient outside the range $\mathbb{Z}_q$ is reduced to be in $\mathbb{Z}_q$. Reduction is implemented as a comparison and subtraction to keep the performance overhead low. Each HE_Add operation increases noise additively.

HE_Mult: BFV supports both ct-ct and pt-ct multiplication. Cheetah uses pt-ct multiplication to multiply plaintext weights by encrypted activations. Pt-ct multiplication is achieved by multiplying evaluation space ciphertext polynomials by the evaluation space plaintext polynomial containing weights on a per-element basis. Performance is limited by the modular reduction required for each polynomial coefficient of output. Cheetah uses Barret reduction (details in Section 4.1). HE_Mult operations increase noise by a multiplicative factor.

HE_Rotate: BFV supports slot rotation within a packed polynomial to enable computation between data in different slots. Since HE_Add and HE_Mult are element-wise operations, computations like dot products require HE_Rotate to align partial products and implement the reduction (see Section 5.1). HE_Rotate is computationally expensive with many steps, and increases noise additively. We refer the reader to [9, 62] for details.

3.2.2 Polynomial Decomposition

Decomposition is used to segment polynomials into multiple components with smaller-valued coefficients. The key idea is that HE operations over smaller coefficient polynomials reduces noise growth. To enable this, Cheetah has two parameters for polynomial decomposition: $W_{dcmp}$ and $A_{dcmp}$ (Table 2), which defines the base that polynomials are decomposed to. Decreasing decomposition base increases the number of decomposed polynomials which decreases operator noise growth but increases the total amount of compute. Once decomposed operators complete, resulting segments are re-combined (i.e., summed) to get the final result.

HE_Rotate requires ciphertext decomposition, otherwise a single operation can exceed the noise budget. The decomposition base $A_{dcmp}$ is used to factor ciphertext polynomials into multiple, smaller-magnitude polynomials when HE_Rotate is applied. We denote $l_w \approx \log_{A_{dcmp}}(q)$ as the number of polynomials with base $A_{dcmp}$ resulting from the de-
composition. Since HE_Rotate noise increase is additive, with decomposition noise increase by an additive factor proportional to \( A_{\text{dcmp}} \) and the increase in number of polynomial operations \( l_d \).

HE_Mult also benefits from decomposition to reduce noise. For neural networks, we use HE_Mult with decomposition to compute the partial products since weights are presented in plaintext. Using a decomposition base \( W_{\text{dcmp}} \), the plaintext polynomial can be decomposed into \( I_{pl} \approx \log_{W_{\text{dcmp}}} (t) \) polynomials. The resulting HE_Mult with decomposition requires \( I_{pl} \) polynomial multiplications to implement but reduces noise growth by a factor of around \( t/(I_{pl} W_{\text{dcmp}}) \).

### 4. HE-PTUNE: MODELS & PARAMETER TUNING

Parameter selection is a major source of complexity in HE (i.e., \( n,l,q,W_{\text{dcmp}}, A_{\text{dcmp}} \)). The key challenge is striking a balance between noise budget and performance. A higher noise budget enables greater computational depth per ciphertext but slower HE operators. Existing solutions rely on over-provisioning noise budgets, resulting in suboptimal performance. This section proposes HE-PTune: analytical performance and noise models for deep learning operators in HE to maximize performance via fine-grained parameter tuning. An evaluation of Cheetah’s HE parameters found using HE-PTune shows up to a 11.7 \( \times \) speed up over the state-of-the-art.

### 4.1 Performance Modeling

HE-PTune’s performance model is based on analytically deriving the total number of underlying integer-multiplication operations that need to take place per layer. (Recall that the HE operator HE_Mult consists of many underlying multiplications.) Empirical studies show most HE operators resolve to multiplication and ones that do not have run-times either strongly correlated or dominated by those that do. Therefore, a high-level model multiplicity count is sufficient to model performance (as validated below). Performance models for CNN and FC layers are built by first modeling HE and transformation (i.e., NTT) operations. Next, modeled operations are reduced to the total number of underlying integer-multiplication operations.

#### 4.1.1 Modeling CNNs

CNN layers are parameterized as \((w, f_w, c_i, c_o)\), where \( w^2 \) and \( f_w^2 \) represent the size of input image and weight filter, and \( c_i \) and \( c_o \) denote the number of input and output channels, respectively. Encryption parameters follow the notation defined in Table 2. Effective modeling of HE_Mult and HE_Rotate counts require consideration of two cases: 1) the ciphertext slot count is greater than an input image (i.e., \( n > w^2 \)), 2) the ciphertext slot count is less than an input image (i.e., \( n < w^2 \)). Let \( c_o \) denote the number of input image channels per ciphertext (i.e., \( n/w^2 \)) in the first case and inversely the number of ciphertexts per input image channel (\( w^2/n \)) in the second case. Both cases count the number of HE operations per CNN layer (see Table 4).

#### 4.1.2 Modeling FCs

A similar process is repeated to model FC layers. The only difference is the change in the number of HE_Mult and HE_Rotate counts. The required number of integer multiplications per HE_Mult and HE_Rotate operations is the same in both CNN and FC. Here, an FC layer is parameterized as \((n_i, n_o)\), where \( n_i \) and \( n_o \) represent the number of input and output activations, respectively. The required number of HE_Mult and HE_Rotate for all possible cases, conditioned on the input-output ratio, are summarized in Table 4.

### 4.2 Noise Modeling

CNN and FC layers are implemented with HE operations (see Section 5.1), so with an understanding of HE operator noise growth (see Table 3), we developed a model for layer noise as a function of both HE \((n,l,q,W_{\text{dcmp}}, A_{\text{dcmp}})\) and FC/CNN \((f_w, w, c_i, c_o)\) for CNN and \( n_i, n_o \) for FC) parameters. If we directly used values from Table 5 the model would estimate worst case noise, causing excessively slow HE parameters to be used. Fortunately, the worst case is extremely rare. Here we develop practical-noise estimations for HE operators and provide a theoretical analysis of the failure rate. We also note that all prior work on high-performance HE \([11,28,32]\) set HE parameters using heuristics, proving high-likelihoods for success but not guaranteeing it.

Cheetah builds a theoretically-motivated, empirically-driven noise model that minimizes computational overheads with a targeted probability of success. We use the fact that the noise added for encryption is sampled from an independent bounded discrete Gaussian (IBDG) distribution with variance \( \alpha^2 \), and if \( X_1 \)'s are IBDG with variance \( \alpha^2 \), then \( \sum \alpha X_i \) is also IBDG with variance \( \sum \alpha_i^2 \). As the noise grows multiplicatively in HE_Mult and additively in HE_Add and HE_Rotate, we can compute the variance of the output noise after each linear operation under independence assumption (i.e., noise coefficients in ciphertexts are independent), validated in [19]. Then, since the output noise, say \( Y \), is IBDG with standard deviation, say \( \sigma_y \), the probability of incorrect decryption is bound by \( \Pr(|Y| \geq q/(2r)) \leq \)

| Table 5: Noise models for CNN and FC layer |
|-------------------|-------------------|
| **CNN** | **Output Noise** |
| \( n \geq w^2 \) | \( f_w^2 c_i \eta_0 w + \eta_0 c_i (f_w^2 - 1 + (c_o - 1)/c_o) \) |
| \( n < w^2 \) | \( (2f_w - 1)f_w c_i \eta_0 w + \eta_0 c_i (2f_w + 1)/(f_w - 1) \) |

| **FC** | **Output Noise** |
|-------------------|-------------------|
| \( n \geq n_i \) | \( n_i \eta_0 w + \eta_0 (n_i - 1) \) |
| \( n < n_i \) | \( n_i \eta_0 w + \eta_0 (n_i - 1)/n \) |
2 \exp \left(-\frac{q^2}{4r^2 \sigma_T^2} \right)$. We use the above facts to derive an output noise threshold given a probability of correct decryption. Therefore, instead of using worst-case bounds and guaranteeing correct decryption, our noise model uses the scaled expressions given in Table 5. The scaling factor $c$ was chosen for a decryption failure rate of less than $10^{-40}$, which is much lower than the model’s misclassification rate. Empirically, our experiment show $c \approx 0.001$ for the tested HE parameters (e.g., $n \geq 2048$).

The output noise variance for CNN and FC layers are tabulated in Table 5. Here, $v_0$ is the initial noise for the input ciphertext, $\eta_q$ is the noise due to HE_Mult, and $\eta_A$ is the growth factor from HE_Rotate. By dividing $\frac{v_0}{2}$ by the output noise (and take the log), the remaining noise budget in bits is given. When the budget is negative, computation fails; when positive, it fails with probability $\leq 10^{-10}$.

### 4.3 HE Parameter Space Exploration

Using a single set of HE parameters for all DNN layers results in unnecessarily poor performance. This is because HE parameters must provision for the worse case noise across different layers which may have different dimensions and hyperparameters. Using HE-PTune’s models for noise and performance, parameters can be tuned on a per-layer basis. HE-PTune takes layer hyperparameters as input and outputs optimal HE parameters found via a design space exploration. Because the model is analytical, a vast (nearly exhaustive) parameter space can be explored in a matter of minutes.

An example of HE parameter space exploration are given in Figure 3 using the ImageNet dataset and AlexNet model. Each blue dot is unique set of HE parameters modeled with HE-PTune to estimate computation and remaining noise budget. Red stars indicate parameters used by Gazelle and green stars show the optimal point found using HE-PTune. Gazelle uses the same sets of HE parameters for all layers. Of all layers in the model, Layer 5 has the smallest remaining noise budget, and it follows that the speedup between Gazelle and Cheetah is the lowest for this layer (see bars in Figure 3).

Using HE-PTune, empirical results show using a single set of parameters is inefficient and unnecessary. The highest Cheetah speedup is in Layer 0, where Gazelle has an excess noise budget of 4.6 bits whereas HE-PTune finds a configuration leaving only 1 bit of noise budget. Improvements come from tailoring the parameters precisely for unique characteristics of each layer; e.g., Layer 5 is FC and Layer 0 is CNN, the computational demands between them vary by over 100x.

In addition to performance, HE-PTune eases the complex task of identifying working HE parameter settings in the first place. Recall that any point with a negative margin fails decryption as the noise budget is exceeded. Of all the points evaluated in the design space search, over 99% have a negative remaining noise budget and will not work if used. Finding HE parameters is difficult for non-experts, and further motivating HE-PTune.

We validate the parameter sets from HE-PTune using different CNN and FC layers used across commonly used deep learning models. We evaluate the following deep learning models: LeNet-300-100 and LeNet5 for MNIST [35], and AlexNet [34], VGG16 [57], and ResNet50 [30] for ImageNet [51]. Each layer is tested using a variety of HE parameters, with no consideration of noise budget to explore the parameter space. Execution times are collected by implementing each CNN/FC layer in the SEAL HE library [55] and measuring its performance using a Xeon server. The remaining noise budget is collected after each run using SEAL’s internal measuring capability and API. Overall, we find that due to the randomness in the noise, the noise model shows slightly larger error than the performance model. However, this is acceptable as the worst-case errors are within 1 bit in the low-remaining noise budget region of the space. This implies the model is fast enough to tell whether a set of HE parameters will allow correct computation of a given layer.

### 5. PARTIAL-ALIGNED SCHEDULING

This section introduces a new dot product schedule - Sched-PA - to enable high-performance HE for the FC and CNN layers. Recall that each HE primitive has different run-time and additive noise trade-offs (Section 3) and the overheads of different primitive schedules are not associative so order of operations matters. Operation orderings with less noise are beneficial as it enables higher-performance via more computationally efficient HE parameters. As a result, our Sched-PA dot product schedule optimization provides a performance benefit of up to $10.2 \times$ compared to Gazelle’s dot product schedule which is prior state-of-the-art.

#### 5.1 Sched-PA: Partial-Aligned Dot Products

The key challenge for implementing HE dot products is optimizing how data is packed into polynomial slots and the relative order of operations. Computing a dot product in HE requires all three primitives: HE_Mult, HE_Add, and HE_Rotate. First, each partial product is computed using one full HE_Mult operation between a ciphertext (encrypted activation) and a plaintext (model weights). Each partial is then accumulated using a series of HE_Add operations to reduce the final output. The problem is that HE operations
Recall that in the context of HE for deep learning in the
This means that when polynomial A and B are multiplied
Sched-PA dot product first rotates
then
HE_Rotate
v
aligned such that the partial slot matches the correct output
compute the final value.
The post-rotation ciphertext and plaintext are
ations involved, weights must simply be arranged in a plain-
cloud the activations are assumed to be encrypted as cipher-
Prior work aligns the input data before performing mul-
In partial-aligned dot products, the initial input cipher-
text is kept in its original order, never rotated. Weights are
weights are
only support computation between aligned polynomial slots. This means that when polynomial A and B are multiplied (resulting in C), C[i] = A[i] • B[i], ∀i ∈ {0, n). To properly reduce each of the partials of a dot product, the slots in C must be aligned to use the correct values.

Prior work aligns the input data before performing multiplication, referred to here as an input-aligned dot product schedule (Sched-IA) [29,32]. In input-aligned dot products, the input ciphertext is first aligned, i.e., rotated, to the correct output slot, and plaintext weights are packed appropriately. (Recall that in the context of HE for deep learning in the cloud the activations are assumed to be encrypted as ciphertext and the weights in plaintext. Re-arranging plaintext data in polynomials is cheap as there is no encryption or HE operations involved, weights must simply be arranged in a plaintext vector.) The post-rotation ciphertext and plaintext are then multiplied, resulting in a dot product partial (ciphertext). Resulting partial ciphertexts can be readily accumulated to compute the final value.

Cheetah proposes a new dot product implementation called Sched-PA (see Figure 4,5). The key insight of the implementation is that HE_Mult increases noise by a multiplicative factor ηM (≤ nlpdWtemp/2) whereas HE_Rotate is additive ηA. In partial-aligned dot products, the initial input ciphertext is kept in its original order, never rotated. Weights are again packed into a plaintext polynomial and aligned with ciphertext slots to compute the correct partial product via HE_Mult. Finally, resulting partial ciphertexts are aligned such that the partial slot matches the correct output slot. Figure 5 also shows Sched-PA compared to the other approach.

The benefit stems from noise accumulation in chained HE operations. Recall that v0 and vA represent the initial input ciphertext noise and additive noise from HE_Rotate, respectively. Thus, a dot product using the partial aligned schedule experiences a noise growth of ηMv0 + ηA. In contrast, the Sched-IA dot product first rotates then multiplies, resulting

Figure 4: How Cheetah implements CNNs using Sched-PA. Sources of inter-kernel parallelism (IKP) are labeled.

Figure 5: Sched-IA (input-aligned) versus Sched-PA (partial-aligned) dot product schedules. Cheetah uses Sched-PA to improve performance of CNN and FC layers.

5.2 Implementing Low-Noise Convolution
Figure 6 shows an example of how CNNs are implemented in HE using Sched-PA. FC layers are implemented following precisely the same steps as CNNs, as the core primitives are also dot products. First, the input activation ciphertext (Acts) is packed/encoded by placing adjacent pixels from the client’s image sequentially in polynomial slots. This ordering eases partial ciphertext alignment. Next, CNN filter weights (Filter) are packed/encoded into plaintext polynomials. Each activation-weight polynomial is multiplied with HE_Mult, resulting in a ciphertext of dot product partials. The resulting partial polynomials are then rotated to align partial slots to the proper output-neuron slot. Finally, with all partials computed and aligned, the ciphertexts are summed with HE_Add to perform partial reduction. Note how polynomial slots allow multiple output neurons to be computed in single ciphertext. This algorithmic parallelism provides substantial performance and memory savings for HE as without it, each thousand degree polynomial would only compute a single output neuron, resulting in thousands of factors of slowdown.

The zeros found in weight plaintext slots (e.g., PT0) ensure the correct computation of convolution operation. For example, the red slot in Figure 4 shows how accumulation works. After f0 is multiplied to D6 in the first HE_Mult, the result is rotated right 6 times to be accumulated in the red slot (C12 in the output). When this rotation is performed, D19 aligns to slot 0, however f0D19 should not be accumulated for the convolution output of slot 0 (i.e., C0). Selectively adding zeros in the plaintext slots avoids this boundary cases.

5.3 Evaluation Results
The effectiveness of Sched-PA is evaluated using five standard CNN models. HE-PTune is employed to maximize

Figure 6: Per-benchmark speedup achieved by Cheetah using HE-PTune and Sched-PA. Speedup is relative to Gazelle [32], in noise growth of ηM(v0 + vA), which is significantly larger than the partial-aligned schedule. Saving noise enables HE-PTune to identify higher performance HE parameter settings, ultimately resulting in performance benefit.
Figure 7: Profiling results for ResNet50 and speedup needed by each kernel to match plaintext inference latency.

benefits using the same method from Section 4 where HE parameters are tuned on a per-layer basis. Multiple experiments are run to show the benefits of HE-PTune with and without Sched-PA relative to Gazelle 32.

The results for each model are shown in Figure 6. Overall, the Cheetah optimizations substantially outperform Gazelle. Using the harmonic mean, 2.98× speedup comes from HE-PTune alone (5.25× ignoring MNIST). Sched-PA provides an additional mean speedup of 5.20× (6.11× ignoring MNIST) for a total mean performance improvement of 13.5× and maximum of 79.5× over Gazelle (30.3× mean without MNIST).

Significant performance overheads are incurred by Gazelle as the high-noise, input-align schedule requires substantial ciphertext and plaintext decomposition. Each time a polynomial is decomposed to reduce operation noise, the number of polynomials that must be computed grows proportionately. In ResNet50, Cheetah’s optimizations result in a ciphertext decomposition base of 8 to 16 more bits. A higher ciphertext decomposition bases result in fewer decomposed polynomials for HE_Rotate, and substantial performance improvements. Using Sched-PA, Cheetah avoids all plaintext decomposition.

6. PROFILING HE INFERENCE

Algorithmic optimizations like HE-PTune and Sched-PA significantly improve the performance over the state-of-the-art 32, e.g., 55.6× for ResNet50. However, with algorithm optimizations alone HE inference is still impractically slow - 3-4 orders of magnitude slower than plaintext inference. To better understand performance limitations and bottlenecks, we profile a high-performance software implementation of HE inference and measure the speedups needed from hardware acceleration.

We implement ResNet50 HE using the SEAL library 55. Leveraging Cheetah to tune parameters and maximize performance, a single inference takes 970 seconds running on an Intel Xeon E5-2667 server. For reference, a single plaintext inference implemented in Keras 14 running on the same server takes 100 milliseconds. Since SEAL only supports CPUs, we perform profiling on the CPU platform. Later we also consider GPU optimization focusing on NTT kernel.

Profiling results are summarized in the pie chart of Figure 7. Notice that only a few kernels dominate performance (HE_Mult, HE_Add, HE_Rotate, and NTT). HE_Rotate in Figure 7 does not include NTT as this is shown separately. Of the four, NTT is the primary bottleneck taking 55.2% (535 seconds) of the run time. The SEAL profile also contains a long-tail of small functions as well (labeled as "Other" in Figure 7). A deeper investigation reveals that most of the time in

Figure 8: NTT GPU speedup over CPU.

"Other" functions is construction and destruction overhead.

Using the profile results, we compute the speedup needed from each kernel to achieve plaintext HE inference. Figure 7 shows the results from this limit study of how various speedup factors impact overall run time. The x-axis shows the speedup factor applied to each labeled kernel function (note log scale); the final speedup factor for each kernel is the speedup needed (e.g., 16,384 for NTT). The y-axis shows absolute latency. From left to right, the plot shows how the total inference latency decreases as each theoretical speedup factor is applied to each function. Kernel speedup is applied successively where the run time from the most aggressive speedup factor is taken as the base for the next function as well as the starting point for the client. The horizontal red line is the 100ms plaintext inference time taken as a latency target.

Speeding up HE with GPUs: One way to improve kernel performance is with GPUs. For HE, GPUs provide large improvements over CPUs but still fall short of the four orders of magnitude compared to plaintext inference. To understand the limitations of HE on GPUs, we benchmark NTT, which is the main HE bottleneck, using the cuHE library 16 on an NVIDIA 1080-Ti GPU. We report GPU speedup for different NTT transform batch sizes (1 to 1024) and vectors lengths n = 16K, 32K, and 64K (Figure 8). We note that some vector lengths are unnecessarily large for efficient BFV implementations, but we included them to show the speedup limits. For larger batch size, the speedup saturates at about 120× for batch sizes 512 and 1024. Profiling results using nvpprof for batch size 512 show that the GPU is highly utilized, achieving 70% occupancy and 85% warp execution efficiency. We also observe shared memory bank conflicts resulting in only 43% of average shared memory efficiency.

Other first order limitations to performance likely derive from (a) non-native, long integer data types requiring emulation, (b) modular arithmetic, which adds branch instructions and over 10 compute instructions per multiplication. Despite the speedups, GPUs fall well short of the improvements required to reach native CPU speed. Finally, we note the reported GPU speedup is optimistic as it ignores bit-reversal (needed for HE inference), which we implement.

7. ACCELERATING HE INFERENCE WITH CUSTOM HARDWARE

This section proposes a general accelerator architecture for HE inference to bridge the remaining performance gap.

7.1 Accelerator Architecture

The proposed accelerator architecture is shown in Figure 9. At a high level, it is composed of ciphertext (CT) processing engines (PEs) that receive data from a PCIe-like streaming interface and buffer intermediary results in SRAMs (Figure 9a).
The partial reduction network is configured based on the number of partials computed in parallel (i.e., number of Lanes). Input CT SRAMs are provisioned with enough capacity to hold all the inputs with sufficient bandwidth to feed all Lanes. The partial reduction network is composed of the individual HE operators. In Figure 9c, HE processors a single ciphertext of output neurons at a time and all compute/memory resources necessary for the output remain local to the PE; the number of PEs is an architecture parameter. When there are more output neurons per layer (parallel Output CTs) than physical PEs, we time multiplex the computation across multiple PE executions. The PEs are connected to input and output buffers used to route data to and from the client. As the accelerator is output-stationary, these buffers only handle communication, all state and intermediates are local to PEs and, therefore, constitute small SRAMs.

The internals of the PE contain partial processing lanes and partial reduction networks. Each PE contains an Input CT buffer to store a copy of all activation CTs locally, a relatively small SRAM for weights, a set of parallel processing lanes (hardware threads), a partial reduction network, and output CT SRAM to interface with the controls to send the results back to the client. Each Lane is capable of processing a unique dot product partial; the number of lanes is parameterizable. Lanes within a PE operate in lockstep to enable aggressive reuse of twiddle factor SRAMs required for NTTs. The partial reduction network is configured based on the number of partials computed in parallel (i.e., number of Lanes). Input CT SRAMs are provisioned with enough capacity to hold all the inputs with sufficient bandwidth to feed all Lanes.

7.1.2 Lanes: Partial Engines

Each lane forms the backbone of the computation and is composed of the individual HE operators. In Figure 9b, HE

kernel blocks are denoted in red, which we build in HLS. Intermediary SRAMs, shown in blue, are used to store results between HE kernels. We use SRAMs instead of off-chip DRAM for intermediary results because of the high internal bandwidth required within NTT modules to support aggressive parallelism. Each NTT kernel at worst requires roughly 13 GB/s of combined internal read/write bandwidth; each lane contains multiple NTTs and each PE contains many lanes. Aside from the NTT kernels that require a butterfly data access pattern, all operations within a Lane can be made streaming (i.e., no SRAMs needed after kernels). This allows the architecture to save SRAM resources. The NTT activation decomposition factor \( A_{\text{dcmp}} \) introduces a parametrizable degree of inter-NTT parallelism, which otherwise does not impact overall latency. For high-performance, we allocate the maximum number of lanes so that they can execute in parallel for all partials.

Recall that in BFV each ciphertext is two polynomials. The lane architecture shows the datapath and dependencies to compute a single partial dot product. Both input polynomials (CT[0] and CT[1]) are first multiplied by plaintext weights using the HE_Mult operator outputting partial polynomials. However, the datapaths diverge due as the BFV formulation splits the compute asymmetrically between partial[0] and partial[1]. HE_Rotate is applied to perform polynomial/vector slot alignment (refer to Section 5). The swap unit reorders each partial’s coefficients. For partial[1], inverse NTT (INTT), decomposition, NTT, and composition units are applied. The datapath for partial[1] splits after the INTT computation in order to implement ciphertext decomposition. Recall that decomposition reduces noise growth; however, the trade-off manifests here as additional compute requirements. Fortunately, the additional computation can be parallelized (NTTs and SIMDmults). The decomposed polynomials are then converted back to the evaluation domain and combined with swapped partial[0] to produce the aligned partial that is fed to the partial reduction network in the PE, which consists of more SIMDadd units.

8. DESIGN SPACE EXPLORATION

This section presents design space exploration results of our architecture. It shows that, when combined with application optimizations, we can achieve plaintext-level HE inference speed.
8.1 Methodology

Design space exploration consists of sweeping different kernel implementation parameters. Each kernel (HE_Mult, HE_Add, and HE_Rotate—which is split into Swap, INTT, Decompose, NTT, and Compose) is built using Catapult HLS 10.3d [1] and synthesized with a commercially-available 40nm standard cell library targeting 400 MHz. We sweep hundreds of design points per kernel to explore different kernel design spaces and identify optimal implementations. Each design is parameterized by memory bandwidth (or IO in the case of streaming kernels), datapath parallelism (i.e., hardware loop unrolling), pipelining (i.e., initiation-interval), and clock frequency. To check correctness, each kernel was validated against equivalent SEAL implementations. We measure the power, performance, and area of these results using the Catapult RTL generation and power estimation flows. To estimate SRAM power and area, we use a commercial SRAM compiler to compile each SRAM dimension used across different design points due to different memory tiling factors. Based on these design sweeps, we identify the Pareto optimal points and use them to identify optimal power and area accelerator designs.

The overall performance of a full inference is modeled on a per-layer granularity; this is because after each layer’s linear computations, activations are sent to ReLU and Pooling. Architecturally, we assume 32K PEs and 16K lane instances per PE to exploit the abundant application parallelism available. Lanes per PE is swept from 4 to 192. Each layer of a DNN is expressed as a series of output neuron computations; from this, we compute the total number of partial products per output neuron ciphertext. Given a set of hardware resources, we execute as many in parallel as is supported and time multiplex computation as needed for larger workloads. The power, area, and performance estimates are derived using lane estimates as well as additional overheads such as data ingestion time over the I/O interface. SRAM capacities and bandwidth are derived using HE, DNN, Kernel, Lane, and PE parameters. SRAM is always allocated for the worst case, supporting the maximum capacity and bandwidth necessary to keep compute resources fully utilized.

To estimate the benefits of technology scaling, we report power and area estimates for 5nm using foundry-reported scaling factors. Specifically, we use 0.2× power and 0.22× area to scale from 40nm to 16nm, based on [12, 34, 43, 51, 61]. From 16nm to 5nm, the power and area scaling factors are 0.32× and 0.17×, using [50] and recent data from [65]. Together, the power and area scaling factors (40nm to 5nm) are 0.056× and 0.038×, respectively.

8.2 Evaluation Results

This section evaluates inter-kernel and intra-kernel speed ups to determine whether plaintext HE inference is possible.

8.2.1 Intra-Kernel Parallelism

We measure the Pareto optimal design speed ups for HE kernels achieved by the energy-optimal point from the power-latency Pareto frontier. An example design space Pareto frontier for NTT is shown in Figure 10. Recall that these frontiers are used as the cost model for the larger architecture, whose sweeps consider the performance-latency tradeoffs of each kernel. We normalize our speedups to the SEAL library implementation on a 3GHz Intel Skylake Xeon processor.

Overall, we see modest speedups of individual kernels up to 40× speedup (average ≈10× speedup) with hardware acceleration. The HE_Add and HE_Mult kernels provide substantial parallelism as the underlying computation consists of element-wise modular additions and multiplications which can be easily parallelized. In the case of HE_Rotate (Swap, Decompose, Compose) and NTT, parts of the underlying computations occur sequentially while others can be parallelized such as the element-wise multiplications and butterfly computations. The key result is that intra-kernel parallelism can reduce HE overhead by roughly one order of magnitude.

8.2.2 Inter-Kernel Parallelism

Fortunately, neural networks contain abundant application-level parallelism that results in the majority of computation being embarrassingly parallel. With the exception of kernel dependencies within a Lane and the reduction of partial products in PEs, partials and output neurons can be executed in parallel by allocating more hardware resources.

For example, consider CNN Layer6 in ResNet50 (\(f_u = 3\), \(w = 64\), \(c_i = c_o = 64\)). If each ciphertext contains a single input channel (\(n = 4096\)), then all partial products can be computed with 36,864 HE_Mult and HE_Rotate parallel kernel invocations. The partial products for these layers cannot be parallelized since HE_Mult must be performed before HE_Rotate in partial-aligned scheduling. In HE_Rotate, domain conversion from evaluation to coefficient using INTT must be done before polynomial decomposition, but the remaining NTT to convert the domain of decomposed polynomials can be parallelized. As a result, we find that the degree of parallelism that can be exploited at the Lane and PE level is on the order of thousands for ResNet50. The key result is that application inter-kernel parallelism can expose two to three order of magnitude improvement.

8.2.3 Lane and PE DSE
Table 6: Performance of running VGG16 and AlexNet on PT-ResNet50 accelerator. Prt is partials per output CT.

| Model      | Lat(ms) | Increase | PEs-Lanes | Out CT μ | (K)Prt μ |
|------------|---------|----------|-----------|-----------|-----------|
| ResNet50   | 100     | 0%       | 8-512     | 147       | 50.5      |
| VGG16      | 215     | 59%      | 16-256    | 422       | 595       |
| AlexNet    | 77      | 28%      | 16-128    | 475       | 337       |

When combined, inter-kernel and intra-kernel parallelism can bridge the remaining 9000× speedup required to achieve plaintext inference speeds on top of Cheetah’s algorithmic optimizations. We now identify whether the design is of practical size and power by conducting a design space exploration to run each inference model at plaintext speed. Figure 11 shows the results from the design space exploration of ResNet50. The power-latency Pareto points identified in the left-most subplots are the ideal architectures when designing an accelerator tuned only for the model. The Pareto frontiers provide insight into the hardware cost-per-ms tradeoff of inference latency. The ResNet50, we find that the Pareto optimal design point to achieve plaintext inference speeds requires around 30W for ResNet50 and 545mm², which is within feasible (albeit high) resource usage for datacenter servers. The extremely low power density is due to aggressive SRAM tiling to meet aggressively high internal bandwidth targets for NTT units. Upon further analysis, we find that the 128×60 bit SRAM sizes have a bit density that is ≈2.5× worse than larger 1024×60 SRAMs, which ultimately results in low power density. We also note that the 400 MHz clock target is low for a 5nm technology, further reducing power density.

To understand the limitations to efficiency and performance of each Pareto design point, Figure 11 shows the Pareto optimal design result for ResNet50 (AlexNet, VGG16, and MNIST exhibit similar trends). Figure 11a shows six design points on the Pareto frontier. Figure 11b and Figure 11c show the breakdown of run time and area respectively for these six design points. For extreme low-latency designs (Pareto points 0 and 1), results show that most of the design area goes into small SRAMs which are required to support the enormous internal bandwidth required by NTT units (discussed next). As a result, this leads to impractically large area overheads.

Overall, our results in Figure 11 confirm NTT and reduction (HE_Add) generally dominate HE accelerator computation. Recall NTT is data intensive and have many small internal SRAMs, which at extreme design points result in high power and area usage. This is compounded by the sheer number of NTT units that operate in parallel, making NTT computations the largest area component of the accelerator overall. And even for the largest design, NTT compute remains the primary latency bottleneck and IO utilization is only at 12%. Moreover, we find that the input and output SRAMs in the architecture do not incur as high of a power and area cost. This means that the input duplication into each PE to support output-stationary computation is relatively inexpensive.

8.2.4 Accelerator Generality

Fabricating a single fixed-size accelerator for each DNN model is impractical. Instead, the accelerator can be programmed to support different-sized networks by multiplexing compute logic (PEs and Lanes) to handle different DNN tensor shapes. To quantify the loss associated with the underutilized units and imperfect dimension matching, we quantify the performance loss of running different ImageNet models (AlexNet and VGG16) on the HE accelerator optimized for ResNet50 from Figure 11 (i.e., Point 3).

The performance results are summarized in Table 6. We find both AlexNet and VGG16 experience considerable slowdown relative to their ideal architectures for real-time inference as seen in the Increase column of the table. This is due to the choice of PE and Lane allocations and the differences in layer dimensions. As the table shows, AlexNet and VGG16 layers have a higher average number of output CTs per layer than ResNet50, and the cost of multiplexing PEs outweighs the cost of poor Lane utilization given the granularity of work (a partial versus an entire output CT). The average number of partials per ciphertext is also much higher. However, ResNet50 is very structured given its use of bottleneck layers many of which have partials per output ciphertext that are divisible by or less than 512, yielding high utilization. Conversely, VGG16’s partials per output CT tend to fall just above or below factors of 512, (e.g., 34, 687, 1086) resulting in lower utilization.

9. RELATED WORK

A growing interest in privacy and machine learning has resulted in a body of related work on developing cryptographic solutions. Techniques can be categorized into two groups: HE only [11, 28, 31, 53], or multiparty computation (MPC)-based [32, 36, 48, 49]. While each has significantly advanced the field all suffer from either accuracy loss due approximation or high communication/computation overheads.

HE only techniques must address evaluating non-linear functions (e.g., ReLU, MaxPool) using only available addition and multiply operations. CryptoNets [28], CryptoDL [31], and LoLa [11] propose replacing ReLU with low-order polynomials that can readily be computed with HE primitives. However, even with square activations [11], this requires very large HE parameters (e.g., q ≈ 1000 [28], 440 bits [11], while Cheetah uses 60) for an appropriate noise budget. Moreover, approximate activation functions require re-training [11] and can degrade accuracy [28]. Others propose accelerating HE kernels with accelerators. NTT has been ported to FPGAs [46, 50] and GPUs [2, 3, 17] to speedup polynomial multiplication. Raizi et al [47] propose HEAX to accelerate HE kernels with FPGAs but only reports two orders of magnitude speedup. While related, the results of HEAX are orthogonal to the contributions of this paper; HEAX uses CKKS (Cheetah uses BFV), focuses on ciphertext-ciphertext multiplication (Cheetah uses plaintext-ciphertext), and mostly targets kernel acceleration (Cheetah focus on the end-to-end application of DNN inference and general chip architecture).

MPC-based schemes provide an alternative to approximation by combining HE with other security solutions, typically garbled circuit (GC) [32, 36, 40, 44, 48, 49]. Among them, Gazelle is considered the state-of-the-art [32]. Gazelle uses HE for linear layers in the cloud and GC for ReLU and MaxPool on the client. This can significantly improve the latency for small models but results in a severe computational
bottleneck in deep models (e.g., ResNet50). Cheetah takes Gazelle as a baseline and focuses on reducing the significant computational overheads of HE.

Other work assumes different threat models with non-private solutions. E.g., [10, 59] use TEEs to isolate private data from untrusted software. Others have looked at limiting information leakage by adding noise (similar to DP) [39]; this provides increased average-case privacy with negligible loss in accuracy.

10. CONCLUSION

This paper makes progress on fundamental roadblocks to adoption of HE machine learning inference by proposing Cheetah. First, HE-PTune automatically identifies the HE parameter with minimal computational overhead. By fine-grained tuning of HE parameters per each layer, HE-PTune’s parameters yield up to $11.7 \times$ performance benefit over the state-of-the-art. Next, Cheetah proposes Sched-PA which yields 10.2 $\times$ speedup for dot products in FC and CNN layers in HE. Finally, we propose a custom accelerator architecture to exploit the high application inter- and intra-kernel parallelism. We evaluate the tradeoffs between inference latency and hardware costs and show that combining application level parameter tuning with specialized hardware acceleration can bring HE inference down to practical plaintext speeds.

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