FPGA-based Performance Evaluation of FEC Codes for an Advanced ISDB-T

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Abstract We are developing an advanced Integrated Services Digital Broadcasting-Terrestrial (ISDB-T) system for the next generation of digital terrestrial television broadcasting. The advanced ISDB-T provides 4K8K terrestrial broadcasting service for fixed reception and 2K service for mobile reception simultaneously within one channel. New technologies such as Low-Density Parity-Check (LDPC) code are used for expanding the transmission capacity and for improving the spectral efficiency. The LDPC codes designed for the advanced ISDB-T have two code lengths and 13 code rates for each code length. The code length and code rate can be selected in consideration of the transmission latency requirement or the link budget. Meanwhile, although the LDPC codes have good bit error rate (BER) performance approaching the Shannon limit, a small number of error bits cause an error floor even if the $E_s/N_0$ is high enough. The error floor may cause serious issues such as block noise in video and mute in audio because broadcasting is a real-time service without any feedback. To deal with this problem, Bose-Chaudhuri-Hocquenghem (BCH) code is concatenated as outer code to the LDPC codes as inner codes. We conducted a simulation using a field programmable gate array (FPGA) instead of a computer to evaluate the BER performance. An FPGA simulation is 1000 times faster than a computer simulation, so the BER performance can be evaluated quickly with an adequate number of measurement bits. As a result, it was confirmed that LDPC codes perform as designed both in the water-fall and error-floor regions and that the BCH codes correct the small number of error bits after the LDPC decoder.

Key words: LDPC codes, BCH codes, an advanced ISDB-T

1. Introduction and overview

4K8K satellite broadcasting services using the Integrated Services Digital Broadcasting for Satellite, 3rd generation (ISDB-S3) system1) were launched in Japan in 2018. For the next generation of digital terrestrial television broadcasting, NHK is developing an advanced Integrated Services Digital Broadcasting-Terrestrial (ISDB-T)2) system for simultaneously providing 4K8K terrestrial broadcasting service for fixed reception and 2K service for mobile reception over a 6 MHz bandwidth in the UHF band3). The advanced ISDB-T will use new technologies such as low-density parity-check (LDPC) codes for expanding the transmission capacity and for improving the spectral efficiency. Our previous studies evaluated the transmission performance in computer simulations, laboratory experiments, and field experiments using prototype hardware4).

The LDPC codes of the advanced ISDB-T include two different code lengths, i.e., a 69120-bit code called middle code and a 17280-bit code called short code5). The longer code than the middle one, called long code, does not exist yet because the advanced ISDB-T is not standardized but still under consideration. Since it is well known that the longer code works better, the target performance, complexity, and specifications of the long code will be discussed. Two code lengths and 13 code rates can be selected in consideration of various requirements such as the link budget of each service and the transmission latency. For example, the middle codes will be used for the fixed reception layer in consideration of the need for higher spectral efficiency, while the short codes will be used for the mobile reception layer in consideration of the need for lower latency. Meanwhile, although LDPC codes have excellent error correction performance approaching the Shannon limit in the water-fall region, some error bits cannot be corrected in the error-floor region. On the other hand, terrestrial broadcasting systems require a robust transmission capability, since they are real-time services without any feedback and error bits cause serious issues with video
and audio content. For example, the ISDB-T system used in current television broadcasting requires a bit error rate (BER) of less than $1 \times 10^{-11}$ after Reed-Solomon decoding. This is equivalent to one error hit every few hours considering that the bit rate of the service is about 18 Mbps. Since the advanced ISDB-T is assumed to require the same robustness as ISDB-T, the error floor may be a serious issue. To deal with this problem, Bose-Chaudhuri-Hocquenghem (BCH) code is concatenated as outer code with LDPC codes as inner codes. When the LDPC codes of the advanced ISDB-T were designed, the BER performance in the water-fall region was evaluated in computer simulations. However, these evaluations did not treat either the error-floor region or its BCH code performance because of the long calculation time it entailed.

This paper describes the BER performance of LDPC codes of the advanced ISDB-T in both the water-fall and error-floor regions and BCH code performance in simulations using a field programmable gate array (FPGA) instead of a computer, i.e., a central processing unit (CPU). By using the FPGA, we succeeded in calculating the BER performance of LDPC codes with an adequate number of measurement bits in the error-floor region within a realistic calculation time. Next, we measured error bits that were not corrected in the LDPC decoder and verified whether the BCH codes work as designed. In addition, by using FPGA simulations with a huge number of measurement bits, we confirmed that the BER of each code has low error-floor characteristics and the BCH codes perform as expected.

The performance of iterative decoding schemes such as LDPC codes is well-known to suffer from the error-floor problem. Richardson presented a numerical technique for the prediction of the error-floor of an LDPC code with BPSK modulation over the AWGN channel. Also, the prediction method of the error-floor of LDPC coded bit-interleaved coded modulation (BICM) was reported. These techniques do not consider a concatenated code such as LDPC and BCH code used in various broadcasting standards. Other international standards of terrestrial broadcasting, such as DVB-T2 and ATSC 3.0, also use LDPC codes and BCH codes.

In this paper, section II briefly introduces the features of the LDPC codes and BCH codes for the advanced ISDB-T. Section III explains the method and parameters of the performance evaluation and the FPGA simulation results. Section IV is the conclusion of this paper and mentions future work.

2. Features of FEC codes

2.1 LDPC codes of the advanced ISDB-T

Fig. 1 shows the structure of the forward error correction (FEC) frame. As in DVB-T2 and ATSC 3.0, LDPC codes and BCH codes are concatenated. $N, K, M_b,$ and
Table 1: Specifications of LDPC codes

(a) Middle codes

| R   | PCM | N   | K   | M₀  | M₁₁ | M₂ |
|-----|-----|-----|-----|-----|-----|-----|
| 2/16| MET | 69,120 | 8,448 | 192 | 1,800 | 58,680 |
| 3/16| MET | 69,120 | 12,768 | 192 | 1,800 | 54,360 |
| 4/16| MET | 69,120 | 17,088 | 192 | 1,800 | 50,040 |
| 5/16| MET | 69,120 | 21,408 | 192 | 1,800 | 45,720 |
| 6/16| MET | 69,120 | 25,728 | 192 | 1,800 | 41,400 |
| 7/16| MET | 69,120 | 30,048 | 192 | 4,680 | 34,200 |
| 8/16| IRA | 69,120 | 34,368 | 192 | 34,560 | - |
| 9/16| IRA | 69,120 | 38,688 | 192 | 30,240 | - |
| 10/16| IRA | 69,120 | 43,008 | 192 | 25,920 | - |
| 11/16| IRA | 69,120 | 47,328 | 192 | 21,600 | - |
| 12/16| IRA | 69,120 | 51,648 | 192 | 17,280 | - |
| 13/16| IRA | 69,120 | 55,968 | 192 | 12,960 | - |
| 14/16| IRA | 69,120 | 60,288 | 192 | 8,640 | - |

(b) Short codes

| R   | PCM | N   | K   | M₀  | M₁₁ | M₂ |
|-----|-----|-----|-----|-----|-----|-----|
| 2/16| MET | 17,280 | 1,592 | 168 | 1,800 | 13,320 |
| 3/16| MET | 17,280 | 3,072 | 168 | 1,440 | 12,600 |
| 4/16| MET | 17,280 | 4,552 | 168 | 1,080 | 11,880 |
| 5/16| MET | 17,280 | 5,032 | 168 | 720 | 11,160 |
| 6/16| MET | 17,280 | 6,512 | 168 | 720 | 10,080 |
| 7/16| IRA | 17,280 | 7,392 | 168 | 9,720 | - |
| 8/16| IRA | 17,280 | 8,472 | 168 | 8,640 | - |
| 9/16| IRA | 17,280 | 9,552 | 168 | 7,560 | - |
| 10/16| IRA | 17,280 | 10,632 | 168 | 6,480 | - |
| 11/16| IRA | 17,280 | 11,712 | 168 | 5,400 | - |
| 12/16| IRA | 17,280 | 12,792 | 168 | 4,320 | - |
| 13/16| IRA | 17,280 | 13,872 | 168 | 3,240 | - |
| 14/16| IRA | 17,280 | 14,952 | 168 | 2,160 | - |

M₁ respectively mean the code length, data length, BCH parity length, and LDPC parity length. Table 1 shows the specifications of the LDPC codes of the advanced ISDB-T. N is a constant value that does not depend on the code rate $R = (N - M₁)/N$. The length of the short code is a quarter that of the middle code. While in case of a middle $R > 7/16$ and short $R > 6/16$, the parity check matrix (PCM) has an irregular repeat accumulate (IRA) structure\(^{(1)}\). In the case of a middle $R \leq 7/16$ and short $R \leq 6/16$, the PCM has a multi-edge type (MET) structure\(^{(1)}\). According to the related paper\(^{(2)}\), MET structure performs better than the IRA one for low LDPC code rates, especially rates less than a half. For this reason, both the advanced ISDB-T and ATSC 3.0 adopt not only IRA but MET structure in order to provide wide range of LDPC code rate. In the case of MET structure, the LDPC parity length is divided into two parts, denoted $M₁₁$ and $M₁₂$. The total LDPC parity length is calculated using Eq.(1).

$$N - (K + M₀) = M₁₁ + M₁₂ \quad (1)$$

The PCM of each structure is shown in Fig. 2, where A, C, and D are $\{M₁ + M₁₁\} \times (K + M₀)$, $M₁₂ \times (K + M₀)$, and $M₁₁ \times M₁₂$ matrices, respectively.

M₂ is an $\{M₁ \times M₁₂ \times \{M₁₁ \times M₁₁\}\}$ dual diagonal matrix. E is an $M₁₁ \times M₁₂$ identity matrix. Z is the zero matrix. Both PCMs have a quasi-cyclic(QC)-LDPC structure in consideration of the hardware complexity of the decoder. As can be seen in Fig. 2, the matrix is divided into segments whose size is L. The parity-check is arranged randomly in the first column of the segment. The parity-check in the second column is placed at the q-bit shift of each address in the first column. q in the IRA structure obeys Eq.(2).

$$q = \frac{M₁}{L} \quad (2)$$

In this way, the parity-check on the n-th column(1 ≤ n ≤ L) is placed on the q-bit shift of each address in the (n-1)-th column. L for the advanced ISDB-T is 360. On the other hand, $q₁$ and $q₂$ are defined in accordance with the MET structure. $q₁$ is used in part A, and $q₂$ is used in parts C and D. $q₁$ and $q₂$ obey Eq.(3).

$$\begin{align*}
q₁ &= \frac{M₁₁}{L} \\
q₂ &= \frac{M₁₂}{L}
\end{align*} \quad (3)$$

The matrix structure and its design method are detailed in the previous related paper\(^{(12,20)}\).

When the LDPC codes of the advanced ISDB-T were first designed, the BERs in the error-floor region were required to be under $1.0 \times 10^{-7}$, and a software simulation confirmed that there was no measurable error floor at a BER $> 1.0 \times 10^{-7}$. However, it was difficult to find the error floor at a BER of $1.0 \times 10^{-7}$ or lower.

### 2.2 BCH codes of the advanced ISDB-T

BCH code uses a 16th degree primitive polynomial for the middle codes and 14th degree one for the short codes, as does DVB-T2 and ATSC 3.0. Table 2 shows the parameters of the BCH codes. The length of each BCH code is a constant value, and its data length is shortened in consideration of the data length of LDPC code $(K + M₀)$.

### 3. Performance evaluation

#### 3.1 Simulation method

Fig. 3 shows a block diagram of the simulation implemented in the FPGA. Pseudo-random noise (PN)
binary signals are generated and input to the BCH encoder and LDPC encoder in turn. Both encoders attach parity data to the input binary data. After that, the input data are modulated with a quadrature phase shift keying (QPSK) signal $x$. $x$ represents a complex baseband signal. In the channel simulator, $x$ is multiplied by a complex signal $c = a + jb$. In the case of an additive white Gaussian noise (AWGN) channel, $(a, b)$ is always $(1, 0)$. In the case of an i.i.d. (independent and identically distributed) Rayleigh channel, $a$ and $b$ are randomly generated from a Gaussian whose average is 0 and variance is 0.5. After the channel simulator, AWGN noise signal $n$ is randomly generated from Gaussian noise of average 0 and variance $\sigma^2/2$ using the Box-Muller method and added to the signal. The received signal $y$ is described as follows.

$$y = cx + n$$  \hspace{1cm} (4)

The log likelihood ratio (LLR) of each bit is then calculated. The $i$-th LLR $\lambda_i$ is

$$\lambda_i = \ln \frac{\sum_{k \in S^0_i} \exp \left(-\frac{|y - cx_k|^2}{\sigma^2_i}\right)}{\sum_{k \in S^1_i} \exp \left(-\frac{|y - cx_k|^2}{\sigma^2_i}\right)}$$ \hspace{1cm} (5)

Here, $\sigma^2_i$ is the noise variance of the $i$-th bit, $x_k$ and $k$ represent a transmitter replica signal and index of it, and $S^b_i$ is the set of $b = \{0, 1\}$ in the $q'$-th bit. In this simulation, the channel state information (CSI), i.e., $c$ and $\sigma^2$, is known to the receiver. The LLRs are input to the LDPC decoder and BCH decoder. The BERs are measured before and after the BCH decoder.

The bit depth setting in the FPGA-based simulation is shown in Table 3. The whole simulation architecture is implemented in a single XILINX Vertex-7 (XC7VX1140T-FLG1930C), and its clock speed is 100 MHz. In a LLR calculation, the bit assignments of the decimal part, integer part, and sign are 3, 4, and 1. The degradation from a floating number calculation is less than 0.1 dB.

### 3.2 Simulation parameters

Table 4 shows the parameters of the simulation. The LDPC decoding algorithm is the offset min-sum method. This method has lower complexity and a little lower performance than that of the sum-product (SP) algorithm. Another popular decoding algorithm is the normalized min-sum method. In our previous study, the offset min-sum method works a little better than the normalized min-sum method in the case of higher order modulation scheme such as 4096QAM. Since the modulation scheme of the advanced ISDB-T includes up to 4096QAM, the offset min-sum method is used in this paper. The maximum number of measurement bits in the FPGA simulation is $1.0 \times 10^{13}$, about 1000 times as many as in the software simulation. It is equivalent to 4 days’ worth of transmitted data assuming that the transmission bit rate in the 6 MHz bandwidth is 30 Mbps.

### 3.3 Simulation results

1. **LDPC codes**

   Fig. 4 and 5 show the BER performance for each code length and code rate in AWGN and i.i.d. Rayleigh channels. The BERs in the error-floor region are suppressed to under $1.0 \times 10^{-7}$, which is the upper limit in the error-floor region when the LDPC codes were designed for the advanced ISDB-T. Moreover, the BER performance of middle and short codes in the i.i.d. Rayleigh channel is lower than that in the AWGN channel because of the slightly higher $E_s/N_0$.

   The threshold of $E_s/N_0$ is defined if each BER is equal to $1.0 \times 10^{-7}$ in order to compare the performance of middle and short codes. The gain, that is, the difference between the thresholds for middle and short code, is plotted for each code rate in Fig. 6. In case of $R \geq 8/16$, all the matrices are IRA structure, and the difference between the middle and short codes is less than 0.2 dB in the AWGN channel and less than 0.4 dB in the i.i.d. Rayleigh channel. In the case of
Fig. 4: BER performances in AWGN channel

Fig. 5: BER performances in i.i.d. Rayleigh channel

Fig. 6: Gain of middle codes from short codes

Fig. 7: Error bit counts

$R < 8/16$, the difference between the middle and short codes is less than 0.6 dB in both channels. These results show that the BER performance of the middle code in the water-fall region is better than that of the short code, because it is longer. Fig. 6 also shows that the gain in the i.i.d. Rayleigh channel is a little larger than that in the AWGN channel, and the gain of the lower code rate is a little larger than that of the higher code rate.

Fig. 7 shows the error bit counts in a false FEC frame with $R = \{4, 7, 12\}/16$ at a constant $E_s/N_0$. Each constant $E_s/N_0$ is determined in the error-floor region, referred in Fig. 4 and 5. These results show the distribution of error bits after the LDPC decoder. There are not only many random errors of 1 or 2 bits, but also
burst errors up to 12 bits. In all cases, no burst errors over 13 bits were measured. This means that the BCH code can correct all the error bits occurring after the LDPC decoder.

(2) LDPC+BCH codes

For example, Fig. 8 shows the BER performances of LDPC codes and LDPC+BCH codes, whose code length is middle and code rate is 9/16. A small number of error bits remain after the LDPC decoder, and the BCH code performs well. The BER after the BCH decoder is less than $1.0 \times 10^{-12}$ when the BER before the BCH decoder is $3.0 \times 10^{-10}$. The concatenated BCH code performance should be verified with simulations because the LDPC codes do not mathematically determine the error correction ability. The relationship between the BER performances before and after the BCH decoder is shown in Fig. 9 and 10. Each BER performance plot shows that the BCH code corrected every error bit in the error-floor region. These results indicate that $t = 12$ error correction bits of BCH code is enough for the advanced ISDB-T. For example, if the bit rate for the fixed reception service is 30 Mbps, 1 bit error per hour means $BER = 9.2 \times 10^{-12}$. The BER performance of the LDPC and BCH concatenated code is less than 1 bit error per hour in all cases.

Tables 5 and 6 show the BER before the BCH decoder and after the BCH decoder at a constant $E_s/N_0$(dB). The average BER of all code rates is listed at the bottom of each table. The average BER in the i.i.d. Rayleigh channel is a little lower than that in the AWGN channel because of the slightly higher $E_s/N_0$. In both channels, all BERs before the BCH decoder are under $4.0 \times 10^{-9}$ in the error-floor region. On the other hand, all BERs after the BCH decoder are zero. This means that no error events occurred in the AWGN and i.i.d. Rayleigh channels during the $1.0 \times 10^{13}$ bit measurement. These results indicate that all the LDPC codes of the advanced ISDB-T perform excellently.

4. Conclusion

This paper described a performance evaluation of LDPC codes and BCH codes that were designed for the advanced ISDB-T. Previously, it was difficult to measure the BER performance before and after the BCH decoder in the error-floor region using a CPU simulation because of the long calculation time. Since the error floor may cause a serious issue in the digital terrestrial broadcasting service, the BER performance in the error-floor region needs to be evaluated. In this study, an FPGA simulation instead of a CPU simulation was performed in an attempt to evaluate the BER.
BCH codes were evaluated. The relationship between cause the error floor, were measured. After LDPC decoding, not only ran-
less than 0.6 dB. It was also found that the gain of an 
gain of the middle code from the short code, is 
short code are suppressed to under 
short code, is 
less than 0.6 dB. It was also found that the gain of an 
i.i.d. Rayleigh channel is a little higher than that of an 
AWGN channel. After LDPC decoding, not only random errors but also burst errors up to 12 bits, which 
cause the error floor, were measured.

Next, the performances of concatenated LDPC and 
BCH codes were evaluated. The relationship between 
the BER performances before and after the BCH de-
coder was revealed. It was found that $t = 12$ error 
correction bits of BCH code is enough for the advanced 
ISDB-T. Furthermore, by transmitting a huge amount 
of data, the BER performances of all code rates and 
code lengths were evaluated. All BERs of the code 
rates in the error-floor region were found to be under 
$4.0 \times 10^{-9}$. As a result, it was confirmed that all the 
LDPC codes of the advanced ISDB-T work as designed 
in both the water-fall and error-floor region, and the 
concatenated BCH codes work perfectly. Our future 
work will be to use the FPGA to evaluate the perfor-
mance of not only the LDPC codes but also the bit-
interleaved coded modulation(BICM). Also, these sim-
ulation results will be the basis for a quasi-error free 
(QEF) reference and a measurement guideline of the 
advanced ISDB-T.

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