An FPGA cached sparse matrix vector product (SpMV) for unstructured computational fluid dynamics simulations

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Abstract

Field Programmable Gate Arrays generate algorithmic specific architectures that improve the codes’ FLOP per watt ratio. Such devices are re-gaining interest due to the rise of new tools that facilitate their programming, such as OmpSs. The computational fluid dynamics community is always investigating new architectures that can improve its algorithms’ performance. Commonly, those algorithms have a low arithmetic intensity and only reach a small percentage of the peak performance. The sparse matrix-vector multiplication is one of the most time-consuming operations on unstructured simulations. The matrix’s sparsity pattern determines the indirect memory accesses of the multiplying vector. This data path is hard to predict, making traditional implementations fail. In this work, we present an FPGA architecture that maximizes the vector’s re-usability by introducing a cache-like architecture. The cache is implemented as a circular list that maintains the BRAM vector components while needed. Following this strategy, up to 16 times of acceleration is obtained compared to a naive implementation of the algorithm.

1 Introduction

Power constraints are pushing the High-Performance Computing (HPC) community towards the search for more efficient computing architectures that can cope with the exascale’s challenges [1]. One of the current trends consists of

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using accelerators as co-processors that increase the Floating-point operations (FLOP) per watt ratio in the systems. The Graphic Processor Units (GPUs) are the most common accelerators utilized in the leading edge supercomputers \cite{2}. Its adoption has been supported by the impulse in markets such as videogames, cryptocurrency, and deep learning. Those markets are focused on dense computations that do not always reflect the algorithms’ needs in computational fluid dynamics (CFD). Consequently, CFD codes are accelerated but can only exploit a small percentage of the peak performance \cite{3,4}. The results are even more dramatic when dealing with simulations based on unstructured meshes. In that case, the parallel algorithms are characterized by sparse algebra operations and low arithmetic intensity.

Field Programmable Gate Arrays (FPGAs) are accelerators capable of reconfiguring their circuit logic. The chip consists of an array of configurable logic blocks interconnected by a programmable network. Those logic blocks are supported by an internal memory called Block Random Access Memory (BRAM). Also, the blocks can include non-configurable computing engines dedicated to specific tasks. The FPGAs’ advantage is their ability to use problem-specific information to create customized architectures that efficiently map the data path and algorithmic logic. By doing so, the chip is entirely devoted to specific tasks, increasing the power efficiency in comparison with general-purpose architectures (CPUs and GPUs). For years, the developers viewed the FPGAs as complex devices that require in-depth computing architecture knowledge with unreasonable long developing cycles. This fact has been improved by the utilization of high-level synthesis (HLS) tools such as Vivado HLS. This tool allows to abstract from the detailed low-level knowledge of computer architecture, relying on automatic optimization mechanisms that interpret the high-level clauses inserted in the code. In our implementation, an extra layer of abstraction exists due to a directive-based programming model. OmpSs \cite{5} is developed at the Barcelona Supercomputing Center (BSC) and allows to engage the FPGAs just by adding pragma clauses in the code. At compilation time, OmpSs converts the code into an intermediate code interpreted by the Vivado HLS, simplifying the code writing to the scientific application experts.

CFD codes can profit the FPGAs for generating a customized architecture that can improve its performance per watt ratio. Early attempts \cite{6,7} of porting part of finite element method (FEM) codes have been tested successfully. Our work is based on a portable implementation method presented in \cite{8}. The idea consists of implementing the CFD as a concatenation of sparse algebra operations. The primary function is the sparse matrix-vector multiplication (SpMV), and therefore it is the focus of attention in this paper.

The SpMV is widely studied due to its importance in many scientific applications. Storage formats are used to avoid storing the zero elements of the sparse matrix. Consequently, the multiplying vector accesses are indirect and determined by the sparsity pattern of the matrix. The matrices arisen from the discretization over unstructured meshes have a very scarce sparsity pattern, making difficult the data reuse. Regarding the SpMV in FPGAs, different implementation strategies have been studied in the past. An implementation based
on using block structures present in the sparsity pattern of FEM matrices was proposed in [9]. A column-wise implementation was presented by [10]. The idea consists of avoiding the multiplying vector’s indirect accesses, while the resulting vector can be stored in a dense local structure. Another strategy, developed in [11], is based on performing a lossless compression of the non-zero elements of the matrix for reducing the memory bandwidth occupancy. A cache vector strategy was presented in [12] and later utilized in [13], the caching scheme aims at maximizing the data reuse of the multiplying vector by performing a preprocess that determines the cache misses that later work as an input for the algorithm. The cache misses have also been treated by fully transferring the multiplying vector into the BRAM [14]. These works aim to be efficient in a broad set of matrices that does not profit the problem information of the sparsity pattern in our CFD matrices.

Therefore, we propose an FPGA SpMV algorithm that borrows some of the developments mentioned above while incorporating information from the CFD matrices. A cache vector is implemented as a circular list for maximizing the memory reuse and concurrently compress part of the matrix data. The matrix is stored using a sliced ELLPACK format [15] following a column-wise order.

The rest of the paper is organized as follows. In the next section, we present the CFD simulations’ application context to understand the importance of the SpMV. In Section 2 we present an overview of the hardware architecture and software components of the FPGA utilized in this paper. Section 3 describes the general considerations for implementing the SpMV. Then, in Section 4 the proposed algorithm for the FPGA cache SpMV is explained in detail. Afterward, in Section 6 the performance of the new algorithm is compared with the naive implementation and with a general-purpose implementation found in the literature. Finally, we summarize our contributions in Section 7.

2 Application Context

Our application context are the CFD simulations based on the solution of the Navier Stokes equations for incompressible turbulent flows:

\[
\nabla \cdot \mathbf{u} = 0, \tag{1}
\]

\[
\frac{\partial \mathbf{u}}{\partial t} + (\mathbf{u} \cdot \nabla) \mathbf{u} = -\nabla p + \nu \nabla^2 \mathbf{u} \tag{2}
\]

where \( \mathbf{u} \) is the three-dimensional velocity vector, \( p \) is the kinematic pressure scalar field, and \( \nu \) is the fluid’s kinematic viscosity.

The standard strategy to discretize the equations is using stencils. Those operations aim at choosing a path to sweep the data maximizing its reuse. The data reuse is possible due to the geometrical topology in the structured grids. However, unstructured meshes lack the geometrical support to detect data reutilization zones, and therefore, do not profit from the stencil implementation. In such cases, an alternative portable implementation based on algebraic operators has been presented in [16] [17].
In an operator-based formulation, the finite-volume spatial discretization of these equations reads

\begin{align*}
\mathbf{M} \mathbf{u}_c &= \mathbf{0}_c, \\
\Omega \frac{d\mathbf{u}_c}{dt} + \mathbf{C}(u_s)\mathbf{u}_c + \mathbf{D}\mathbf{u}_c + \Omega\mathbf{G}p_c &= \mathbf{0}_c,
\end{align*}

where \( \mathbf{u}_c \) and \( p_c \) are the cell-centered velocity and pressure fields, \( \mathbf{0}_c \) is the discrete collocated field with zero in each component, \( u_s \) is the velocity field projected to the faces’ normals, \( \Omega \) is a diagonal matrix with the sizes of control volumes, \( \mathbf{C}(u_s) \) and \( \mathbf{D} \) are the convection and diffusion operators, and finally, \( \mathbf{M} \) and \( \mathbf{G} \) are the divergence and gradient operators, respectively.

Note that \( \Omega, \mathbf{M} \) and \( \mathbf{G} \) are linear operators, so they can be implemented as sparse matrices. In practice, the coefficients of the convective term are stored in a one-dimensional array of dimension \( N_e \), where \( N_e \) is the number of non-zero entries in \( \mathbf{C}(u_s) \). The arrangement of this array depends on the storage format chosen for the operator. Under these conditions, we define the evaluation of \( \mathbf{C}(u_s) \) as a linear operator \( \mathbf{E}_C : \mathbb{R}^{N_s} \rightarrow \mathbb{R}^{N_e} \), such that:

\[ \mathbf{C}(u_s) \equiv \mathbf{E}_C u_s. \]

This strategy permits us to transform the non-linear operators into a concatenation of linear operators represented by sparse matrices. Consequently, the time-integration step of the CFD simulation is a concatenation of few algebraic operations. In this work, we focus our attention on the SpMV that is the most time-consuming operation (78%) from the linear solver and the matrix assembly when using the portable implementation [8] according to Figure 1.

The SpMV is a memory bounded operation dominated by the indirect accesses of the multiplying vector. Those accesses are determined by the matrix’s sparsity pattern, which in our simulations is derived from the discretization method and the connection of the unstructured mesh cells. For instance, a second-order discretization scheme derives in a matrix in which rows have up to five non-zero components on a mesh of tetrahedra. A CFD matrix typically has thousands of rows, leading to a very scarce sparsity pattern. This data path generally leads to low resource utilization and compute efficiency in modern architectures [18]. Figure 2 depicts the sparsity pattern of a matrix arisen from 100 tetrahedral cells using the mesh generator’s numbering. Note that the matrix is symmetrical due to the discretization scheme. In this work,
we focus on matrices arisen from incompressible flow problems. In that case, the matrices remain constant during the simulation. This fact facilitates heavy pre-processing techniques since its relative cost would be negligible compared to the full simulation time.

3 System overview

3.1 Computing resources

The Field Programmable Gate Arrays can adapt the circuit logic to the algorithm that it is running on them. A configuration with an optimal number of computing gates and RAM blocks is possible, leading to an improvement in
power consumption. In this work, we use the FPGA ADM-PCIE-7V3 of Xilinx that features two independent channels of DDR3 memory capable of 1333MT/s (fitted with two 8GB SODIMMs). Moreover, it consists of a BRAM of 52.9MB, FFs 886k, LUTs 693k, DSP3600.

The FPGA is connected with a CPU through the PCI-express. Moving data into the FPGA can become a bottleneck since it needs to be transferred from the RAM of the node to the FPGA RAM. From there, it has to be transferred to the on-chip memory (BRAM) when processing the SpMV. A scheme with the node configuration is shown in Figure 3. This work assumes that the matrix data fit in the device’s RAM and is transferred only at the simulation’s preprocess. Therefore the memory transfers between CPU and FPGA RAMs are not considered.

Figure 3: Node configuration diagram.

3.2 Software stack

High-level synthesis (HLS) has facilitated the FPGA implementations during the last years. It has abstracted the complex process of re-programming the FPGAs using the Register-Transfer Level (RTL) design and a Hardware Description Language (HDL). Standard code is complemented with FPGA-specific directives that aim to explain the desired behavior and create digital hardware that maps such action. Vivado HLS is the tool used by the Xilinx to perform the synthesis. In recent years, the HLS has been incorporated in directive-based programming models such as OmpSs.

In the OmpSs@FPGA programming model, programmers write a single source programs in C/C++ that run on heterogeneous systems with CPUs and FPGAs. OmpSs follows an approach similar to OpenMP with some extensions to offload tasks onto the FPGAs.

OmpSs programs are annotated with two types of directives:

- #pragma omp task in(...) out(...) inout(...) are applied to function prototypes, indicating that the invocations to such function are to be spawned in parallel. Additionally, the input-output clauses (in, out,
and inout) tell the data that needs to be available to the task. And also, indicate if the data is consumed, produced, or both. For example, this is the typical annotation for the sparse matrix multiplication:

```c
#pragma omp task in ([NNZ]A, [NNZ] cols , [N] x), inout ([N] b)
void spmv(double *A, int * cols , double* x, double *b);
```

- `#pragma omp target device(fpga)` is attached to a task to indicate that the code of the function will be transferred to a separate output file to be compiled with the Xilinx Vivado HLS tool, thus getting the bitstream to configure the FPGA. Accordingly, the complete annotation becomes:

```c
#pragma omp target device(fpga)
#pragma omp task in ([NNZ]A, [NNZ] cols , [N] x), inout ([N] b)
void spmv(double *A, int * cols , double* x, double *b);
```

This approach allows generating code for Xilinx FPGAs, from Zynq 7000, and Zynq Ultrascale+, to the new PCI-Express attached ALveo boards. The structure of the compilation environment is shown in Figure 4. Code annotated with `target device(fpga)` is interpreted by Mercurium compiler to generate a Vivado HLS file. This file is sent to the AutoAIT tool and compiled with Vivado HLS (right side of the figure). A bitstream is generated from the OmpSs IP blocks with support to the task management tool. On the other hand, Standard C/C++ code for the CPUs is compiled with the native system compiler (GCC in the left of the figure) and linked with the Nanos++ runtime system. This runtime provides the threading and tasking services managing the parallelism, data transfers, and the execution of the FPGA tasks.

In this work, we use OmpSs combined with Vivado HLS to design our algorithm. However, the algorithm itself does not depend on them and could be reused in any other language.

Figure 4: OmpSs@FPGA workflow.
4 General Considerations

4.1 Matrix Reordering

A Cuthill-McKee algorithm \[19\] is applied to reordering the unknowns of the system. The sparsity pattern of the matrix is transformed into a band matrix. The maximum difference between column indexes of the same row is known as the width of the band. The reordering aims at reducing this width by applying a variant of a breath-first search of graph theory. The algorithm has proven to be efficient for CPU and GPU execution since it minimizes the cache misses produced by indirect memory accesses of the multiplying vector \[8\]. Figure 5 shows the changes in the sparsity pattern of the same matrix with 100 tetrahedra cells after applying the reordering. Note that the algorithm does not alter the matrix coefficients nor the sense of the equations. In practical terms, the matrix is still stored contiguously in memory, permitting it to be read efficiently. Moreover, the reordering is applied to the full CFD simulation, so its application is needed only once at the start of the simulation.

![Sparsity pattern of the same matrix arisen from tetrahedral mesh (100 elements) after applying the Cuthill-McKee reordering.](image)

4.2 Storage Format

The sliced ELLPACK format \[15\] is the most appropriate for the matrices arisen from our CFD discretization \[8\]. The format consists of dividing the matrix into slices with a similar number of non-zero elements per row. The number of rows per slice is a parameter defined as $S$. For each slice, the maximum number of non-zero components per row is calculated, and zeros are padded in the rows with fewer elements than the maximum. This scheme permits maintaining the regularity within each slice. Finally, each slice is stored using a column-wise order. By doing so, accessing the rows is performed independently and
contiguously. This storage adapts better to our matrices in which the slices may represent different geometrical elements. Figure 6 shows an example of the storage format when selecting a slice size four. In CFD, the array \( Val \) contains double-precision matrix coefficients to conserve the accuracy of the simulation. The array \( col \) contains the column indexes in a 4-byte integer representation.

4.3 Naive implementation

The primary difficulty in the SpMV is reading the multiplying vector. The matrix's column index, stored as an integer, needs to be read beforehand to determine the vector's required component. This dependency adds an overhead while reading the multiplying vector. In a matrix derived from a tetrahedral mesh, each of the vector components is read on average five times. However, the reuse of the elements not necessarily takes place between two adjacent rows. Consequently, in a naive implementation, each vector component is read up to five times from global memory following an irregular pattern.

5 FPGA SpMV for CFD using unstructured meshes

5.1 Cache-like data structure

The band matrix reordering provides a data path for accessing the multiplying vector that exposes the reusing of its components. As the algorithm moves through the matrix’s rows, the multiplying vector elements are being reused until a point in which the elements are not needed anymore.

Due to the banded pattern, the matrix is divided into slices of \( S \) rows. \( S \) is the optimal number of rows needed to hide the latency of pipelining them on the FPGA. For each slice \( i \), the first and last vector components needed are obtained from the sparsity pattern and named \( col_{start} \) and \( col_{end} \), respectively. The two values determine the range of the vector components required by the slice \( i \). When solving two adjacent slices, the necessary elements overlap, setting the basis for data reuse. Then, each IP core is implemented to operate on a block of \( B \) adjacent slices executed in order. In each block execution, the multiplying vector components needed by the first slice are loaded into a cache vector stored...
in BRAM (local memory). The next slices upload only the members of the multiplexing vector that are not already in the cache. Load operations are performed in chunks of memory, so-called *wordsize*. For simplicity, the *wordsize* is equal to the number of rows in a slice (*S*).

The cache vector is a circular list in which the new components are stored consecutively. When the end of the cache vector is reached, the new components are saved from the beginning, thus, erasing the older cached elements. The cache vector’s optimal size is calculated from the width of the band obtained from the Cuthill-McKee reordering.

The matrix’s storage format needs two additional parameters: 1) the number of the words needed from the multiplying vector that are not currently in the cache vector, and 2) the position of the multiplying vector where the block needs to start the reading process. The number of components read by block*_{i} is obtained from the \( colend_{i} - colend_{i-1} \). And \( offset_{i} \) is equal to \( colend_{i-1} \).

Finally, the column indexes are rewritten as their relative position within the cache vector. By doing so, the indexes vary in the range between zero and the cache vector length. This size is much smaller than the multiplying vector’s total size, and therefore the column indexes can be stored as short integers saving 2-bytes per component read. This compression reduces part of the overhead of reading the components. During the multiplication, the cache vector is still accessed indirectly. However, the memory now is within the BRAM, which is much faster.

### 5.2 Adapted ELLPACK FPGA cached-SpMV

The matrix is stored using an ELLPACK format with a constant number of non-zero entries per row. This number is defined by the geometry of the unstructured meshes and the discretization order. For a tetrahedral mesh, a constant number of five non-zero entries per row. Note that in the case with less connectivity, such as boundary conditions, zeros are padded to enforce the size. This format has proven to be the most efficient in our matrices \(^{[8]} \). In each BLOCK, the rows are stored using a column-wise order that permits the execution of all the rows’ calculation concurrently.

Each instance of our SpMV executes a block of many slices, and each one performs three steps:

- Load the words needed that are not in the cache vector.
- Load matrix and solve the multiplication of each row of the slice.
- Copy the result back to the CPU.

The code is implemented using a combination of OmpSs and Vivado HLS.

### 6 Numerical Results

The matrices used in the numerical experiments were generated using the Laplacian operator and a second-order discretization applied on cells of tetrahedral
meshes. Table 1 shows the characteristics of those matrices.

Table 1: Characteristics of the matrices used in the numerical results

| Charac. | \( C50K \) | \( C100K \) | \( C200K \) | \( C400K \) | \( C800K \) |
|---------|------------|------------|------------|------------|------------|
| rows    | 49,336     | 97,521     | 187,078    | 398,000    | 775,058    |
| nnz     | 243,504    | 481,855    | 928,184    | 1,975,128  | 3,851,840  |

6.1 Comparison with a naive approach

First, we have compared our algorithm with the naive approach discussed in Section 4. Note that the naive SpMV IP has lower BRAM requirements since the multiplying vector is not cached. Therefore, up to 32 instances can be generated and executed concurrently on the FPGA. On the other hand, the optimal version of the cache SpMV has been found when using the number of rows per slice, \( S \), equal to 512. The wordsize is equal to the parameter \( S \). A cache vector of 16,384 entries (32 words) is allocated in the BRAM. With these constraints, only four IPs of the cache SpMV can be instantiated and executed concurrently. The results for both executions are shown in Table 2.

Table 2: Comparison with the naive format

| Method      | \( C50K \) | \( C100K \) | \( C200K \) | \( C400K \) | \( C800K \) |
|-------------|------------|------------|------------|------------|------------|
| Naive       | 0.138      | 0.277      | 0.545      | 1.183      | 2.335      |
| cached SpMV | 0.017      | 0.025      | 0.036      | 0.074      | 0.142      |
| Speedup     | 8.19       | 10.95      | 15.19      | 15.87      | 16.41      |

The comparison shows that the caching strategy outperforms the naive version up to 16 times. The acceleration grows with the matrix size since the multiplying vector’s indirect accesses are more distanced.

6.2 Comparison with an open library

The next step consisted of comparing the results with an open library of the SpMV in FPGAs [14]. The library implements a stream version of the SpMV in the traditional CSR format. The full multiplying vector is loaded once into the BRAM. By doing so, the indirect accesses are produced inside of a memory that is much faster. The drawback of following this approach is that much more BRAM is needed. Large matrix sizes are prohibited, or fill the BRAM with only one instance. Table 3 show the results for both executions. First, we have
compared our algorithm with the naive approach discussed in Section 4. Note that the naive SpMV IP has lower BRAM requirements since the multiplying vector is not cached. Therefore, up to 32 instances can be generated and executed concurrently on the FPGA. On the other hand, the optimal version of the cache SpMV has been found when using the number of rows per slice, $S$, equal to 512. The wordsize is equal to the parameter $S$. A cache vector of 16,384 entries (32 words) is allocated in the BRAM. With these constraints, only four IPs of the cache SpMV can be instantiated and executed concurrently. The results for both executions are shown in Table 2.

Table 3: Comparison with an open library

| Method      | Matrices |        |        |        |        |
|-------------|----------|--------|--------|--------|--------|
|             | $C50K$   | $C100K$| $C200K$| $C400K$| $C800K$|
| stream CSR  | 0.112    | 0.221  | 0.424  | 0.902  | 1.757  |
| cached SpMV | 0.017    | 0.025  | 0.036  | 0.074  | 0.142  |
| Speedup     | 6.64     | 8.73   | 11.83  | 12.11  | 12.35  |

The comparison shows that the caching strategy outperforms the library version up to 12 times. The acceleration grows with the matrix size since the indirect accesses of the multiplying vector are more distanced. The $C800K$ was the last matrix size that the library could solve.

7 Conclusions

The SpMV has proven to be a complex problem to be solved by FPGAs. Its difficulty relies on the indirect memory accesses of the multiplying vector. The sparsity pattern in the matrices arisen from unstructured CFD simulations is scarce, adding an extra layer of complexity. This work shows how applying some pre-processing algorithms tuned an optimal SpMV FPGA execution. An implementation of the SpMV using cache is proposed. The promising results show that using the cache version outperforms the naive implementation up to 16 times. Moreover, the cache SpMV has also been compared against a library that implements a strategy of caching the full multiplying vector into the BRAM. In this case, our implementations are up to 12 times faster, proving their potential to be used in future CFD simulations.

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