Overlap junctions for superconducting quantum electronics and amplifiers

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Due to their unique properties as lossless, nonlinear circuit elements, Josephson junctions lie at the heart of superconducting quantum information processing. Previously, we demonstrated a two-layer, submicrometer-scale overlap junction fabrication process suitable for qubits with long coherence times. Here, we extend the overlap junction fabrication process to micrometer-scale junctions. This allows us to fabricate other superconducting quantum devices. For example, we demonstrate an overlap-junction-based Josephson parametric amplifier that uses only 2 layers. This efficient fabrication process yields frequency-tunable devices with negligible insertion loss and a gain of ~30 dB. Compared to other processes, the overlap junction allows for fabrication with minimal infrastructure, high yield, and state-of-the-art device performance.

Superconducting electronics have experienced rapid growth over the last decade. Advances in quantum information processing based on superconducting qubits has fueled much of this growth. Improvements in design, materials, and fabrication of quantum-limited amplifiers, and the implementation of low-loss superconducting components are some of the pillars supporting progress in the field.

Fundamental building blocks of superconducting quantum circuitry include discrete components, e.g., capacitors, inductors and Josephson junctions (JJs), as well as distributed elements resonators. Modern microfabrication technology allows for the realization of these circuit elements with infrastructure that typically includes optical lithography techniques and metal/dielectric deposition. The JJs, formed by two superconducting electrodes separated by a thin tunnel barrier, play a central role in superconducting quantum circuits. The lossless, nonlinear inductance is the most salient property of these JJs, which render JJs as indispensable circuit elements for superconducting qubits as well as quantum-limited amplifiers.

There are various methods to realize JJs. These include subsequent layer removal of deposited superconductor-insulator-superconductor (SIS) tri-layers (i.e., the “trilayer process”) by shadow evaporation (e.g., the Dolan-Bridges and Manhattan geometries),4 and the overlap-junction technique.5–7 The trilayer process, typically used for superconducting electronics, involves many steps and significant infrastructure for different etches and both metal and dielectric deposition/patterning. On the other hand, shadow evaporation has become the norm for qubit JJs because they can be made very small with a single electron beam (e-beam) lithography step. This minimizes infrastructure and has enabled generations of researchers to make nano-scale quantum devices at the cost of scalability. However, with modern optical lithography that extends down to nanometer dimensions, this has become a moot point. Overlap junctions now allow access to full range of simple fabrication from micro- to nano-scale dimensions. This opens efficient wafer-level fabrication of JJs with high dimensional control and a wide range of applications.

Here, we develop low-critical-current JJs and demonstrate a simple process for micrometer-scale junctions. We describe the process bias and measure the current-voltage (I-V) characteristics of the resulting junctions. This enables the realization of a wide range of superconducting devices. In particular, we demonstrate the fabrication and characterization of important devices for the field, Josephson parametric amplifiers (JPAs), that use only two steps of photolithography.

As shown in Fig. 1 the process is started by depositing ~200 nm Al onto a 76 mm (3 in) intrinsic Si wafer with native oxide in an e-beam evaporation chamber at a base pressure of ~2.7 × 10^{-5} Pa. In the first step of photolithography, the desired pattern for the bottom-electrode (BE) layer is formed using a positive photoresist (PR) on the Al deposited wafer. The pattern is exposed through a photomask, i.e., reticle, in a 5:1 reduction stepper and developed in a tetramethylammonium hydroxide (TMAH) based solution (Fig. 1(a)). The pattern is then transferred onto the Al film by agitating the wafer in an etching solution heated to ~50 °C (Fig. 1(b)). An over-etch of ~10 s ensures complete removal of Al in developed regions (unprotected by the PR).

In the second photolithography step, a metal lift-off resist (LOR) process was used (Fig. 1(c–i)). An imaging PR layer on top of the LOR layer comprises the bi-layer PR stacking. Since TMAH etches Al, a ~200 nm thick polymethyl methacrylate (PMMA) protective layer was applied, before the bi-layer PR stacking, to protect the BE Al layer from the PR developer. This process yields an undercut profile of ~0.7 µm after photo-exposure and development, resulting in a clean metal lift-off.

The subsequent steps shown in Fig. 1(d–f) are critical for the precise definition of the tunnel barrier area. Before the wafer is loaded into the high vacuum e-beam evaporator, it is subjected to room-temperature O2 plasma ash (100 W for 3 min) at a pressure of ~67 Pa (Fig. 1(d)). This step removes PMMA and other organic residues in the developed regions of the wafer. Next, the wafer is loaded into the high vacuum de-
FIG. 1. Fabrication steps for micrometer-scale overlap junction process. (a) 3D sketch of the Si substrate after deposition of the bottom Al layer followed by patterning the PR layer. (b) After etching of Al bottom layer with etchant and stripping of the PR layer. A native surface oxide forms on the bottom Al electrode. (c) After coating with thin protective PMMA layer. (d) A bi-layer of PR/LOR is patterned in a second lithography step to define the pattern of the TE. The thin protective PMMA layer is removed by O$_2$ ashing at room temperature. (e) The native oxide on the bottom Al electrode surface is removed by Ar RF-plasma cleaning. (f) Ultrahigh-purity grade low pressure O$_2$ is used to form a controlled AlO$_x$ tunnel barrier. (g) The TE is formed by subsequent Al evaporation. (h) Metal-liftoff in solvent completes the overlap junction process. (i) A cross-section view of the junction along the dashed line in panel (h) of this figure.

position chamber and argon RF-plasma cleaning is employed to remove the native oxide on the patterned bottom Al layer as described in an earlier work. This cleaning is carried out by applying RF power to an electrically isolated wafer holder that is water cooled. Typically 50 W RF power is applied for $\sim$1 min at room-temperature; the argon pressure is maintained at $\sim$ 1.3 Pa (Fig. 1(e)). AlO$_x$ tunnel barrier is formed by controlled oxidation of the cleaned Al surface. (Fig. 1(f)). The oxidation is carried out by pumping out and sealing the chamber, then introducing ultra-high purity grade (99.999%) O$_2$ into the chamber. The oxidation dose is tuned by adjusting the oxidation time and the oxidation pressure. The overlap junction is completed by depositing $\sim$ 350 nm Al as the top-electrode (TE) using e-beam deposition (Fig. 1(g)). The TE is created by lift-off in solvent with ultrasonic agitation (Fig. 1(h-i)).

An important step in fabricating tunnel junctions is the oxidation step (Fig. 1(f)). In our studies, we explored three different oxidation doses to vary the Josephson tunnel junction resistance (hence critical current) by nearly two orders of magnitude. The oxidation doses explored were 4 min at $\sim$ 40 Pa, 36 min at $\sim$ 40 Pa, and 36 min at $\sim$ 100 Pa.

In order to design wafer-scale lithography patterns, it is necessary to understand the dimensional process biases and apply those to the drawn dimensions. In addition, for devices that are oxidized in-situ after argon cleaning, it is also necessary to include intrinsic process bias. These may be due to, e.g., inhomogeneous junction cleaning, oxidation, and extended edge profiles. To accomplish this, we plot and fit the room-temperature junction resistance $R$ as a function of both the drawn and the measured dimensions of the junctions. Making use of optical microscopy, we determined that the fabrication process yields actual dimensional biases of $a = +0.47 \pm 0.03 \mu m$ and $b = -1.92 \pm 0.05 \mu m$ for the TE and BE, respectively. These reflect the fact that the top layer is additive and the bottom is subtractive. For the $R$ vs. electrode width fits, we start from $R \times A = c$ (where $A$ is the junction area and $c$ is a constant dependent on oxidation dose). To fit using the drawn areas, we can write:

$$R = \frac{c}{(W_T^{\text{drawn}} + a) \times (W_B^{\text{drawn}} + b)}$$

Here $a$ and $b$ correspond to only dimensional bias, and $W_T^{\text{drawn}}$ ($W_B^{\text{drawn}}$) is the drawn width of top (bottom) electrode. The dimensional bias may be expected to correspond with the optically measured values if there is no intrinsic bias. However, as shown in Table 1 and discussed below, we see that the fit bias for the BE is significantly smaller than the measured value, while they match fairly well for the TE. A fit using the measured dimensions helps to understand this; since the actual widths of the TE and the BE are known, we can fit it using only two parameters,
FIG. 2. Room temperature junction characterization. (a) Optical microscope image of a typical micrometer-scale overlap junction is shown on the left of the panel. A drawing of the cross-section is presented on the right side. (b) Junction resistance $R$ vs $W_B$ at different oxidation doses as indicated on the plot. (c) Junction Resistance $R$ vs $W_T$.

$$R = \frac{c}{W_T^{\text{Measured}} \times (W_B^{\text{Measured}} + 2\lambda)}$$  \hspace{1cm} (2)$$

where again $c$ is the oxidation constant while the parameter $\lambda$ includes intrinsic effects.

Resistance data was acquired for the three different oxidation doses and plotted vs. electrode widths, where first the $W_B$ was varied with fixed $W_T$ and then the $W_T$ is varied with fixed $W_B$ (Fig.2). For Fig.2(b) and (c), data for drawn vs. measured widths are plotted using solid and open symbols, respectively. Each data point in Fig.2(b–c), represents the statistical average of 10 individual resistance measurements of nominally identical junctions across a die. Measurements from two dies across the wafer are included for a given oxidation dose. For the various oxidation doses, we performed fits where $W_B$ is varied in Fig.2(b) and $W_T$ is varied in Fig.2(c). The dashed and solid lines in Fig.2(b–c) show the fits using models based measured (Eq.2) and drawn (Eq.1) electrode dimensions, respectively. The fitting results are summarized in TableI.

For the resistance vs. measured width fits, we see that the intrinsic process bias on the bottom electrode, $2\lambda \sim 2 \mu m$, accounts for the missing process bias in the parameter $b$ in the fit for the drawn dimensions. This could explicitly be accounted for in Eq.1 by using:

$$b \rightarrow b + 2\lambda$$  \hspace{1cm} (3)$$

Note that $\lambda$ is significantly larger than the BE thickness. Two possible explanations for this are (a) the edge profile is curved due to wet etching, which yields a length that is longer than the BE thickness and (b) RF plasma cleaning is localized towards the film edges, hence the edges are more electrically transparent than the top surface. This is by no means detrimental to the fabrication process and is easily accounted for in process bias or by extending the RF clean cycle time.

The fitting parameter $c$ is a measure of normal resistance of the junction and is therefore proportional to the effective oxidation dose, given as $c \alpha \times P^\beta$, where $\alpha$ and $P$ are oxidation time and pressure, respectively. From the results presented in TableI $\alpha = 0.58$ and $\beta = 0.40$ ($\alpha = 0.48$ and $\beta = 0.44$) based on measured (drawn) dimensions. This result is in good agreement with accepted values in recent studies, illustrating that the oxidation process is not significantly altered by the air exposure and subsequent RF plasma cleaning step.

We next discuss the low temperature (40 mK) characteristics of the micrometer-scale overlap JJs. The current-voltage (I-V) characteristics are measured by driving current from a low-noise current source and measuring the voltage across the junction with a voltage pre-amplifier.

The JJs display I-V characteristics with no discernible hysteresis (Fig.3). We acquire I-V curves of three representative junctions with $R_N$ values of 4.0, 8.6 and 17.7 $\Omega$, with $W_B^{\text{measured}} = 2.18 \mu m$. We calculate a superconducting gap $\Delta/e = 335 \mu V$, in agreement with values expected for Al. Critical currents, $I_c$, for each junction were 22, 10, and 4 $\mu A$. These measured $I_c$’s are significantly lower than expected, by about a factor of 1/3, from the Ambegaokar-Baratoff (A-B) formula at $T = 0 K$. This is not surprising because the A-B formula is derived for an ideal uniform tunnel barrier, and

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**TABLE I. Oxidation dose and fitting results for models based on measured and drawn dimensions**

| Oxidation Dose | Drawn Dimensions Model | Measured Dimensions Model |
|----------------|------------------------|--------------------------|
| $P$ (Pa) | $t$ (min) | $c$ ($\Omega \mu m^{-2}$) | $a$ ($\mu m$) | $b$ ($\mu m$) | $c$ ($\Omega \mu m^{-2}$) | $\lambda$ ($\mu m$) |
| 100 | 36 | $1634 \pm 45$ | $0.40 \pm 0.03$ | $-0.11 \pm 0.09$ | $1727 \pm 42$ | $0.96 \pm 0.05$ |
| 40 | 36 | $1087 \pm 55$ | $0.34 \pm 0.06$ | $-0.19 \pm 0.17$ | $1198 \pm 38$ | $1.01 \pm 0.07$ |
| 40 | 4 | $382 \pm 20$ | $0.70 \pm 0.08$ | $0.28 \pm 0.19$ | $333 \pm 9$ | $0.92 \pm 0.07$ |
sets an upper limit for the maximum critical current. However, for an actual JJ, defects due to interface roughness, crystal and grain structures, impurities, and processing conditions all may lead to suppression of the critical current.15–17

As a concrete and useful application of these JJs, we designed and fabricated JPAs around the overlap process. This process offers a method for making overlap JPAs (O-JPAs) reliably and with far fewer resources than are typically employed. Early research on JPAs dates back several decades.15–17 More recently, JPAs are employed as indispensable tools for quantum information processing due to their ability to amplify small microwave signals with ultralow added noise. We refer to literature for various implementations and design aspects of JPAs.18–21

Here, we implement an O-JPA design, which is comprised of a capacitive element in parallel with a non-linear inductor (Fig. 4(a)). The inductance is provided using a tunable superconducting quantum interference device (SQUID) array with inductance \( L_j \) that is grounded on one end. For this device, 8 nominally identical SQUIDs, with junction inductance \( L_j \approx 0.5 \text{ nH} \), provide a minimum \( L_j^{\text{min}} = 2.05 \text{ nH} \) (inset of Fig. 3(a)). An interdigitated shunt-capacitor, \( C_s = 396 \text{ fF} \), is connected in parallel with the SQUID array to ground. The resulting lumped-element resonator is coupled to a coplanar waveguide (CPW) transmission line with a coupling capacitor \( C_r = 90 \text{ fF} \). The capacitors were made by etching a 2 \( \mu \text{m} \) wide trench between metal fingers.

The O-JPA is designed to have an unbiased resonance frequency of \( f_{\text{res}} \approx 5.05 \text{ GHz} \) with a quality factor of \( Q_{\text{Total}} \approx 32.22 \). It is operated as a single port device in reflection mode. A circulator is used to separate the input signals (strong RF pump and weak RF signal) from the reflected output signals (idlers and amplified RF signal).

Initial tests of the O-JPA in an adiabatic demagnetization refrigerator (\( T < 100 \text{ mK} \)) are shown in Fig. 4 with the resonant frequency vs. SQUID bias in the inset of panel (b). The inductance of the SQUID array is tuned by applying an external magnetic flux to the SQUID loops by running a DC current through a coil placed nearby. This provides frequency tunability \( \sim 3-5 \text{ GHz} \). A gain of more than 25 dB with about 7 MHz bandwidth is centered at 5.06 GHz. It is possible to engineer a wider bandwidth at the expense of lower gain.

Cavity decay measurements at the base temperature of a dilution fridge (23 mK) allowed the initial estimate of the noise in O-JPAs.23 The decay of an ultra-high finesse cavity at 5 GHz was measured using an O-JPA, operated at 17 dB gain. The O-JPA was followed by a high-electron-mobility-transistor (HEMT) amplifier with 2.4 K thermal noise. The signal-to-noise ratio improved by 11 dB when the O-JPA is turned on, allowing the placement of a lower bound of half a photon added noise due to the O-JPA.

In conclusion, we developed a simple two-step process to realize micrometer-scale overlap JJ devices. The process requires minimal infrastructure compared to typical processes. The geometry, process, and oxidation dose are outlined and we show how to determine the process bias. We characterized the I-V curves of the JJs. We used this information to design and fabricate an ultra-low noise O-JPA with over 25 dB of gain.

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1. M. Gurvitch, M. A. Washington, and H. A. Huggins, Applied Physics Letters 42, 472 (1983).
2. M. Weides, R. C. Bialczak, M. Lenander, E. Lucero, M. Mariantoni, M. Neeley, A. D. O’Connell, D. Sank, H. Wang, J. Wernner, T. Yamamoto, Y. Yin, A. N. Cleland, and J. Martinis, Superconductor Science and Technology 24, 055005 (2011).
3. G. J. Dolan, Applied Physics Letters 31, 337 (1977).
4. A. Potts, P. R. Routley, G. J. Parker, J. J. Baumberg, and P. A. J. de Groot, Journal of Materials Science: Materials in Electronics 12, 289 (2001).
5. M. Steffen, M. Ansmann, R. McDermott, N. Katz, R. C. Bialczak, E. Lucero, M. Neeley, E. M. Weig, A. N. Cleland, and J. M. Martinis, Phys. Rev. Lett. 97, 050502 (2006).
6. J. Braumüller, J. Cramer, S. Schlör, H. Rotzinger, L. Radtke, A. Lukashenko, P. Yang, S. T. Skacel, S. Probst, M. Marthaler, L. Guo, A. V. Ustinov, and M. Weides, Phys. Rev. B 91, 054523 (2015).
7. X. Wu, J. L. Long, H. S. Ku, R. E. Lake, M. BäI, and D. P. Pappas, Applied Physics Letters 111, 032602 (2017).
8. L. J. Zeng, S. Nik, T. Greibe, P. Krantz, C. M. Wilson, P. Delsing, and E. Olsson, Journal of Physics D: Applied Physics 48, 395308 (2015).
9. A. W. Kleinasser, R. E. Miller, and W. H. Mallison, IEEE Transactions on Applied Superconductivity 5, 26 (1995).

10. Argon RF-plasma cleaning at 50 W and 10 mTorr are applied for 75 seconds for these devices. Since then we increased the RF cleaning time to at least 3 minutes to remove the oxide on top of the BE completely.
11. C. Kittel, Introduction to Solid State Physics, 5th ed. (John Wiley & Sons, Inc, New York, 1976).
12. V. Ambegaokar and A. Baratoff, Phys. Rev. Lett. 10, 486 (1963).
13. T. Imanura, T. Shiota, and S. Hasuo, IEEE Transactions on Applied Superconductivity 2, 1 (1992).
14. T. Shiota, T. Imanura, and S. Hasuo, IEEE Transactions on Applied Superconductivity 2, 222 (1992).
15. N. Calander, T. Claeson, and S. Rudner, Applied Physics Letters 39, 650 (1981).
16. A. Smith, R. Sandell, J. Burch, and A. Silver, IEEE Transactions on Magnetics 21, 1022 (1985).
17. B. Yurke, L. R. Corruccini, P. G. Kaminsky, L. W. Rupp, A. D. Smith, A. H. Silver, R. W. Simon, and E. A. Whittaker, Phys. Rev. A 39, 2519 (1989).
18. M. A. Castellanos-Beltran, K. D. Irwin, G. C. Hilton, L. R. Vale, and K. W. Lehnert, Nature Physics 4, 929 (2008).
19. M. Malnou, D. A. Palken, L. R. Vale, G. C. Hilton, and K. W. Lehnert, Phys. Rev. Applied 9, 044023 (2018).
20. M. Hatridge, R. Vijay, D. H. Slichter, J. Clarke, and I. Siddiqi, Phys. Rev. B 83, 134501 (2011).
21. H.-S. Ku, Generating and Verifying Entangled-Itinerant Microwave Fields, Ph.D. thesis, University of Colorado Boulder, Boulder, CO (2015).
22. We used high-frequency electromagnetic software for simulations.
23. A. Romanenko, R. Pilipenko, S. Zorzetti, D. Frolov, M. Awida, S. Belomestnykh, S. Posen, and A. Grassellino, Phys. Rev. Applied 13, 034032 (2020).