Failure Analysis of a Circuit with AC Noise in the Output Signal

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Abstract—A failure analysis process of a circuit with AC (alternating current) noise in the output signal was presented. To find out the root of the failure, the circuit principle and the layout of the circuit were analyzed, and it was found that the layout design was not unreasonable. Specifically, the output signal wire is too close to the clock signal wire, which results in the coupling crosstalk. To eliminate the coupling crosstalk, several measures including the filter design, replacement of resistor, and layout optimization were adopted. This work has reference significance for the anti-interference design of circuits.

1. INTRODUCTION
In recent years, the failure analysis of electronic components has become increasingly important for the manufacture and usage of products [1-4]. By determining the failure location and finding out the failure cause, failure analysis can provide a guide for the designer to improve the reliability of the product during the design stage. Signal anti-interference design is one of the most important reliability issues in circuit design. Generally, an excellent anti-interference design requires both knowledge and experience. In this paper, through the failure analysis of a circuit with AC noise in the output signal, we give an example of anti-interference design.

2. FAILURE PHENOMENON
The failure event occurred on a signal processing circuit fabricated using multi-chip thick film technology. The signal of output pin (pin 1) of the circuit was found to be corrupted by a 100kHz AC noise. The peak-to-peak value of the output signal was about 200mV, while the required value by the user should be less than 10mV.

Inspect the appearance of the faulty circuit, pins 1–8 are connected with a bundle of connecting wires, and the rest are free from any abnormality. After communicating with the user and simulating the user's application environment, manual test was carried out on the signal of output pin (pin 1) of faulty circuit. It was found that the signal of output signal pin (pin 1) had a large AC noise with a peak-to-peak value about 170mV, and the frequency of the AC noise was 100kHz, as shown in Figure 1. The phenomenon was consistent with the user. The difference cannot be excluded because of the inconsistent test environment between the tested peak-to-peak value of 170mV and the user tested 200mV.
3. FAILURE ANALYSIS

3.1 Working principle
To figure out the failure cause, it is necessary to study the circuit principle in the first step. The faulty circuit is a signal processing circuit designed to demodulate the sensing signal from the sensor. Figure 2 shows the functional block diagram of the circuit, and one can see that it is mainly composed of oscillation, differential capacitance detection, signal conditioning, power drive, and voltage reference modules. The function of the main pins is summarized in Table 1. From Table 1, we noted that the frequency of the AC noise falls in the frequency range of the clock output.

![Functional block diagram of the circuit.](image)

Table 1. The main Pin description.

| Pin | Symbol | Description                                      |
|-----|--------|--------------------------------------------------|
| 1   | V4     | The fourth test port                            |
| 2   | V2     | The second test port                            |
| 3   | V-     | Negative power supply -15V                     |
| 4   | V+     | Positive power supply +15V                     |
| 5   | GND    | Ground                                          |
| 6   | VN     | The test port for VN                            |
| 7   | VT     | The test port for VT                            |
| 8   | fclock | Clock output, clock frequency 95~105kHz         |
| 9   | VREF(5V)| Voltage reference 5V                           |
3.2 Reason analysis

Because the frequency of AC noise is close to that of the clock signal, it is probably that the noise is related to the clock. The pins 1~8 of the faulty circuit returned by the user were connected by connecting wires, so this failure can be caused by either peripheral connection wires or the quality problem of the circuit itself.

1) The external reason

In order to exclude the influence of connecting wires, we cut the connecting wires one by one while monitoring the signal of output pin (pin 1). We found that the peak-to-peak value of the AC noise decreased from 170mV to 150mV, as shown in Figure 3, when the wire connected to pin 8 was cut. The connecting wire of pin-8 has an impact on the noise, but it is not the root as the peak-to-peak value of AC noise is still much higher than 10mV required by the user.

2) The internal reason

Since the clock signal is suspected, we check the internal routing of the clock in the first step. The layout of the circuit is shown in Figure 4 (a). It can be seen that a portion of the internal wire of pin 8 (red) is parallel to the green one which is connected to pin 7, and the distance between them is relatively small. Due the long coupling length and small distance between the wires, theoretically, there may be large distributed capacitance and inductance. When high-frequency clock signal propagates on the red wire, it may cause an unexpected voltage or current noise interference on green wire. Similarly, due to the distributed capacitance and inductance formed by other wires, it is easy to generate the capacitive and inductive coupled crosstalk simultaneously [5-6]. The interior of faulty circuit is shown in Figure 4 (b). Therefore, the 8-pin clock port of the faulty circuit has great interference to the routing of the rest pins in the circuit.

Figure 3. The signal of output pin (pin 1) after cutting the wire connected to pin 8.
4. IMPROVEMENT OF THE FAULTY CIRCUIT

To reduce the noise interference, the layout of the circuit was redesigned. The improved layout is shown in Figure 5 (a) and its area remains unchanged. The distance between the clock wire (red) and the test voltage wire (green) is enlarged. To further increase the anti-interference capability, a 0.22μF filter capacitance is added between the power to the ground. Moreover, the 0603 package of some resistors is replaced by smaller 0402 package to adapt to the filter capacitance. The final improved circuit is shown in Figure 5 (b).

A test was carried out to check the performance of the improved circuit. The test result is shown in Figure 6, and one can see that the peak-to-peak value of the AC noise of pin 1 is less than 10mV, indicating the modified circuit has eliminated the internal interference from the clock signal. This result
already meets the requirement of the user. One may find that there is still a small AC noise interference, this is the result of lack of the electromagnetic shielding of the pin 8. Because the pin 8 will produce a strong AC signal, it will lead to the crosstalk on the other pins of the circuit from external propagation of electromagnetic field [7]. Therefore, it is suggested that pin 8 should be shielded from the other pins.

Figure 6. The signal of output pin (pin 1) of the improved circuit.

5. CONCLUSION
In this paper, the failure phenomenon of a circuit with AC noise in the output signal is analyzed, the root cause of the failure of a circuit is found, and a corresponding improvement scheme is proposed. By redesigning the layout and verifying, the same phenomenon has not happened again in the improved circuit. The crosstalk of the AC signal should be carefully considered when designing the layout of the circuit. The routing of the clock wire should be kept far from the key signal wires. This work can offer a reference for the anti-interference design of similar circuits.

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