A high input impedance chopper amplifier using negative impedance converter for implantable EEG recording

Zhiming Liang\textsuperscript{1}, Bin Li\textsuperscript{1}, a), Zhaohui Wu\textsuperscript{1, b)}, and Yunfeng Hu\textsuperscript{2}

Abstract Negative impedance convertor is introduced to build a high input impedance chopper IA for implantable EEG recording. The compensation theory is analyzed in detail to reveal the characteristics of the impedance boosting method. The proposed chopper IA achieves very high input impedance of 18.9 GΩ and 18.5 GΩ at DC and 100 Hz respectively. It can reach 5.8 GΩ even at 1 kHz. With the common-mode feedback loop, up to 600 mVpp common-mode interference tolerance and 97 dB CMRR are achieved. The amplifier is implemented in a 0.18 μm standard CMOS process and takes a power consumption of 1.34 mW with a 1.2 V supply. The mid-band input referred noise PSD is 130 nV/√Hz and an NEF of 4.89 is obtained.

Keywords: chopper amplifier, negative impedance convertor, impedance boosting, high impedance, EEG recording

Classification: Devices, circuits and modules for IoT and biomedical applications

1. Introduction

EEG is an essential component in the evaluation of epilepsy and other nervous system diseases. It provides important information about background EEG and epileptiform discharges and is required for the diagnosis of specific electroclinical syndromes \([1, 2]\). The accurate location of epileptic focus is of great significance in surgical treatment, which includes two stages. First, the scalp electrodes are used for rough positioning. Then, the implanted electrodes are used for obtaining the precise locations. Therefore, implantable EEG recording plays an important role in the treatment of epilepsy \([3, 4, 5, 6, 7]\). In order to obtain high-quality biopotential signal, the front-end amplifier must meet several performance challenges, such as low power, low noise, high CMRR and high input impedance. Biopotential from bioelectrodes is usually low frequency weak signal. In the biosensor amplifier implemented by CMOS technology, the chopper capacitive feedback instrumentation amplifier (CC-FIA) is the most conventional amplifier structure, so as to reduce the in band 1/f noise as well as the DC offset \([8, 9, 10, 11, 12]\). When chopping technique is introduced, the input impedance of the amplifier falls down arising from the switched capacitor (SC) resistor formed by the input chopper and input or parasitic capacitances. In this case, the conventional input impedance can be expressed as \(Z_{in} = 1/(4f_{ch}C_{in})\), where \(C_{in}\) is the equivalent differential capacitance across the output terminals of the input chopper. Determined by the input capacitors and the chopping frequency, typical input impedance of the conventional CC-FIA is always within mega ohms \([13, 14]\). Several techniques have been proposed to boost the input impedance of the CC-FIA, such as using pre-charge technique \([15, 16]\), negative capacitance circuit \([17]\), positive feedback loop \([12, 18]\) and dynamic element matching approach \([19]\). However, the increase in impedance is limited to a few giga-ohms. In order to obtain higher input impedance, a fully integrated chopper IA using three-OTA fully differential structure and negative impedance convertor (NIC) for impedance boosting is proposed in this letter \([20, 21, 22]\).

2. Structure design and analysis of the chopper IA

Fig. 1 gives the schematic of the proposed chopper IA, which is consisted of two amplifier stages. The first stage is a dual-OTA fully differential chopper stage made up of two OTAs of \(A_{1,2}\) and two choppers of \(CH_{1,2}\) to suppress the low frequency flicker noise. The OTA \(A_3\) is placed behind the chopper stage as the linear stage to ensure the open-loop voltage gain. Negative feedback loop, composed of

\textsuperscript{1} School of Microelectronics, South China University of Technology, Guangzhou 510640, China
\textsuperscript{2} Zhongshan Institute, University of Electronic Science and Technology of China, Zhongshan 528402, China

\textsuperscript{a}) phlibin@scut.edu.cn
\textsuperscript{b}) phzhwu@scut.edu.cn

DOI: 10.1587/elex.17.20200238
Received July 8, 2020
Accepted July 13, 2020
Publicized July 28, 2020
Copyedited September 10, 2020
C_{fb1,2} and C_{fb3,4} is used to obtain a definite and accurate closed-loop voltage gain, which can be calculated as $A_v = C_{fb3,4}/C_{fb1,2} + 1$.

The NEF of the amplifier, defined in [27], expresses the noise current trade-off metrics to quantify the performance of these amplifiers. The Noise Efficiency Factor (NEF) is well-known in the design of such amplifiers for physiological sensing applications. The NEF, defined in [27], expresses the noise current trade-off and is given as

$$NEF = \frac{1}{2} \frac{I_{tot}}{U_T \cdot 4kT \cdot \pi \cdot BW}$$

where $I_{tot}$ is the total current drawn by the amplifier, $BW$ is its bandwidth, and $v_{nRMS}$ is its input-referred noise. For the proposed chopper IA and considering the chopper stage only, the NEF can be estimated as

$$NEF_{IA, chopper \ stage} = \sqrt{\frac{32\gamma}{kT}} \approx 3.8$$

Here the technology dependent noise coefficient $\gamma$ takes a value of 1. High gain accurate and low signal distortion of the chopper IA working in close-loop state requires a large open-loop gain. Therefore, in biomedical applications, a linear stage is needed to provide sufficient open-loop gain. After taking into account the closed-loop operating stability, output voltage swing and voltage gain, the chopper IA in this letter uses a fully differential symmetric OTA as the linear stage, which is shown in Fig. 2(b). Considering the phase delay caused by the nondominant pole, the size ratio of M19 and M20 is set as 2:1, and the W/L of M20 is 16/2/2/1.2.

Fig. 3 Open-loop characteristics of the proposed chopper IA

Fig. 3 shows the open-loop characteristics simulation result of the proposed chopper IA. Open-loop DC gain of the chopper IA is about 86.5 dB, which is higher enough to form an accurate close-loop gain. The chopper IA will be designed to operate at a closed-loop gain of 40 dB, while a phase shift of $-114^\circ$ occurs and a phase margin of $66^\circ$ is obtained.

3. Design and analysis of impedance boosting circuits

The input impedance of the proposed chopper IA will be approximately 100 times higher than the input impedance of a nonchopper amplifier. The proposed chopper IA will be designed to operate at a closed-loop gain of 40 dB, while a phase margin of $66^\circ$ is obtained.

$$V_{x1,2} = \frac{V_t + V_c}{2} - \frac{1}{g_{m1}} |r_{o1}| + \frac{1}{g_{m1}}$$

The drain voltage of M1 is obtained as follows.


\[ V_{d1} = -(V_s - V_{cs1,2}) \frac{g_{m1}}{g_{m5}} \]  

(6)

Basing on the Miller’s theorem, the capacitance of non-inverse input terminal of \( G_{m1} \) can be calculated as

\[ \frac{1}{Z_{g1}} = C_{gb1} + C_{gs1} \left( 1 - \frac{V_{cs1,2}}{V_s} \right) + C_{gd1} \left( 1 - \frac{V_{d1}}{V_s} \right) \]  

(7)

When biased in subthreshold region, the gate-source and gate-drain capacitance of a MOS transistor are the same and proportional to the channel width, that is \( C_{g1} = C_{gd1} = W_1C_{ov} \). From Eq. (5) to (7), when the chopper IA shows a very high open-loop gain, the \( C_{g1} \) can be computed as

\[ \frac{1}{Z_{g1}} = C_{gb1} + W_1C_{ov} + W_1C_{ov} \frac{1}{\frac{1}{g_{m1}} \left| r_{g1} + \frac{1}{g_{m5}} \right|} \]  

(8)

Compared with the conventional CCFIA, the original input capacitance of the proposed chopper IA is much smaller, and it can originally obtain very high input impedance around hundreds of megaohms without using boosting technique [28]. In order to obtain higher input impedance, a negative impedance converter (NIC) is introduced to generate a negative impedance device (NID) to compensate the negative impedance convertor (NIC) is introduced to generate a negative impedance device (NID) to compensate the negative impedance convertor (NIC). In the NIC, \( R_{n1} \) and \( R_{n2} \) provide DC feedback for two OTAs, while \( R_{n3} \) and \( R_{n4} \) are designed to balance the AC positive and negative feedback of them. \( C_{d1} \) and \( C_{d2} \) are DC blocking capacitors, whose AC impedance at chopping frequency is negligible compared with the pseudo resistors in series. Assuming that \( A_6 \) and \( A_6 \) are ideal OTAs, the negative impedance generated by the NIC with a connected positive impedance \( Z_{pos} \) is

\[ Z_{neg} = -\frac{Z_{cn1} + Z_{rn1}}{Z_{cn2} + Z_{rn2}} Z_{pos} = k Z_{pos} \]  

(9)

where, \( Z_{cn1} \) and \( Z_{cn2} \) are impedance of capacitors \( C_{n1} \) and \( C_{n2} \), \( Z_{rn1} \) and \( Z_{rn2} \) are the impedance of \( R_{n1} \) and \( R_{n2} \) [20]. When the impedance conversion coefficient \( k \) is \( -1 \), and the equivalent impedance of the \( Z_{pos} \) is the same as that of \( Z_{in,ori} \), the original input impedance of chopper IA can be neutralized by the negative impedance generated by the NIC. That is to say, theoretically, an infinite input impedance can be obtained. In this case, to get a conversion coefficient of \(-1\), capacitors \( C_{n1} \) and \( C_{n2} \) will be designed to the same value. Fig. 4(b) shows the circuit structure of the positive impedance \( Z_{pos} \) used for negative impedance conversion. The pseudo resistors \( R_{n5,6} \) and chopper \( CH_4 \) are used to match the \( R_{n1,2} \) and the input chopper \( CH_1 \) respectively. The \( C_{d3} \) and \( C_{d4} \) are DC blocking capacitors, which are used to avoid the DC coupling of the pseudo resistors \( R_{n5,6} \) and chopper \( CH_4 \) to the inverse input terminal of the OTAs \( A_5 \) and \( A_6 \). Fig. 5 shows the schematic diagram of the negative impedance compensation principle. The original input impedance \( Z_{in,ori} \) and the positive impedance \( Z_{pos} \) for conversion are placed on the left and right respectively.

\[ Z_{in,ori} = Z_{chopper}(2Z_{prex})(2Z_{c1}) \]  

(10)

\[ Z_{pos} = Z_{chopper}(2Z_{prex})(Z_{c23}) \]  

(11)

Therefore, in order to obtain the best impedance compensation, the values of \( Z_{c1} \) and \( Z_{c23} \) should be equal. As shown in Fig. 4(b), when only source followers with the diode connected PMOS transistors are considered, the gate to ground capacitance of NMOS transistor of M23 or M24 can be calculated as

\[ C_{g23} = C_{gb23} + W_{23}C_{ov} + W_{23}C_{ov} \frac{1}{\frac{1}{R_{m23}} \left| r_{o23} + \frac{1}{g_{m23}} \right|} \]  

(12)

Compared Eq. (3.) with the expression of \( C_{g1} \) in Eq. (9), if the M23 and M29 are designed to the same size of the M1 and M5 respectively and work in the subthreshold region, the values of \( C_{g1} \) and \( C_{g23} \) will be very close. In practical application, due to the non-idealization of the OTAs, the negative impedance generated by the NIC cannot completely match the original input capacitance. Left part of Fig. 6 is half of the NIC used to computed the negative impedance conversion theory under this non-ideal factor. There will be input capacitance at the input terminals of non-ideal OTA. The capacitance at inverse input terminal will be paralleled with half of the positive impedance to be converted \( Z_{pos}/2 \), and the input capacitance at the non-inverse input terminal will be paralleled with half of the original input impedance.
of the chopper IA $Z_{in,ori}/2$. If asymmetric differential to single ended current source is used as the loads of the input differential pairs, the input capacitance of the inverse and non-inverse input terminals will be inconsistent, resulting in the mismatch of positive and negative impedance. Therefore, symmetrical OTAs are used in the NIC to ensure that the inverse input impedance can match the non-inverse input impedance after being converted into negative impedance, as shown in the right part of Fig. 6. In the analysis of circuit principle, due to the symmetry of NIC circuit, $Z_{pos}/2$ will be used in the calculation. Thus, the converted negative impedance will also be $Z_{neg}/2$ with half of the NIC. As shown in Fig. 6, $Z_o$ and $Z_L$ are the internal and external equivalent load of the OTA at chopping frequency, $Z_n$ is the parallel impedance of $C_{in}$ and $R_{in}$. $C_{29}$ and $C_{30}$ are the inverse and non-inverse input capacitors of the symmetrical OTA, which show the same impedance of $Z_{ci}$ at the chopping frequency. Assuming that chopping response of the OTA is $A(f_{chop})$, voltage applied to the NID is $V_{in}$, current from voltage $V_{in}$ to the NID is $I_{in}$, the following equations can be obtained.

$$V_o = (V_{in} - V_o)A(f_{chop})$$  \hspace{1cm} (13)

$$V_{in} = \frac{Z_{pos}/2}{Z_{ci}} V_o$$  \hspace{1cm} (14)

$$I_{in} = \frac{V_{in} - V_o}{Z_n} + \frac{V_{in} - V_o}{Z_{ci}}$$  \hspace{1cm} (15)

$$Z_{neg} = \frac{2V_{in}}{I_{in}}$$  \hspace{1cm} (16)

$$Z_{in,boost} = Z_{in,ori}/||Z_{neg}|=|Z_{pos}/||Z_{neg}|$$  \hspace{1cm} (17)

By solving the Eq. (13) to (17), the boosted input impedance can be revealed.

$$Z_{in,boost} = \frac{2}{Z_n} \left[ Z_j \frac{Z_n}{Z_o} + Z_j + \left( \frac{Z_j}{Z_n + Z_j} \right)^2 A(f_{chop}) \right] Z_n$$  \hspace{1cm} (18)

where $Z_j = (Z_{pos}/2)||Z_{ci}$. From Eq. (18), it can be seen that the boosted impedance is a function of the $Z_n$ and $A(f_{chop})$.

In order to further evaluate the effect of impedance boosting, the $A(f_{chop})$ will be computed by calculating $Z_L$ according to Miller’s theorem.

$$Z_L = \frac{Z_n}{1 - \frac{V_{in}}{V_o}}$$  \hspace{1cm} (19)

$$A(f_{chop}) = G_{m5}(Z_n)||Z_L$$  \hspace{1cm} (20)

$Z_L$ and $A(f_{chop})$ can be solved by combining Eq. (13), (14), (19) and (20).

$$Z_L = \frac{Z_n + \frac{1}{G_{m5}}}{\frac{Z_n}{Z_n + Z_j} - \frac{1}{G_{m5}Z_o}}$$  \hspace{1cm} (21)

$$A(f_{chop}) = \frac{1 + G_{m5}Z_n}{Z_n + Z_j} + \frac{Z_n}{Z_o}$$  \hspace{1cm} (22)

The partial derivative of $Z_{in,boost}$ with respect to $Z_n$ can be calculated as

$$\frac{\partial Z_{in,boost}}{\partial Z_n} = 2Z_n^2 \left[ a(Z_n + Z_j)^2 + b + c \right] \frac{dZ_n}{d^2}$$  \hspace{1cm} (23)

where $a = 1 - G_{m5}Z_o$, $b = 2(Z_n + Z_j)$, $c = G_{m5}Z_o Z_j(Z_n + Z_j)$, $d = (Z_n + Z_j)(2Z_n + Z_o + Z_j)$.

Making the derivative of $Z_{in,boost}$ equal to zero and solving the equation, the maximum value of $Z_{in,boost}$ can be reached at

$$Z_n = \frac{(Z_o + Z_j)}{Z_o} + \frac{1}{2} \left( \frac{G_{m5}Z_o Z_j}{Z_o + Z_j} + \frac{Z_n Z_n}{Z_o + Z_j} \right)$$  \hspace{1cm} (24)

It is easy to prove that the value on the right side of the above formula is greater than $Z_j$. Therefore, $[0, Z_j]$ is the increasing interval of function $Z_{in}$. Then the maximum value can be calculated as

$$Z_{in,boost} = \left[ 1 + \frac{1}{2} \left( \frac{G_{m5}Z_o Z_j}{Z_o + Z_j} \right) \right] Z_j$$  \hspace{1cm} (25)

The above formula reveals that the maximum boosting multiple is about one quarter of the voltage gain of the OTAs at the chopping frequency. Fig. 7 shows the simulation curve of input impedance varying with feedback capacitance $C_{61-4}$ at 100 Hz input frequency. It can be seen that the input impedance reaches a maximum value of 33.2 GΩ when the feedback capacitance is 22 fF. This is consistent with the theoretical calculation and analysis results. Taking into account of the matching accuracy and boosting effect, value of the feedback capacitors is designed as 80 fF, where the input impedance of about 20.5 GΩ can be obtained.

![Input impedance varying with feedback capacitance](image)

**4. Layout and results**

The proposed chopper IA was designed using a 0.18 μm standard CMOS process. In the layout design, it is very important that, because the input impedance of the amplifier is very high, the chopper clock interconnects near the inputs and outputs of the input chopper should be shielded with ground metal to reduce the coupling effect of the chopper clock. Fig. 8 shows the layout capture of the proposed chopper IA, the area is about 300 μm × 200 μm. The ripple-reduction-loop (RRL) is also designed to suppress the output ripple, which is not introduced in this letter [29, 30, 31].

The proposed chopper IA is powered by 1.2 V and works at 20 kHz chopping frequency. Fig. 9 shows the input impedance characteristics of pre-simulation, post-simulation and pre-simulation with no NIC. The pre-simulation and post-simulation DC input impedance are about 21.0 GΩ and 18.9 GΩ respectively. Because of the parasitic capacitance, the input impedance of post simulation is a little lower than that of the pre-simulation. The input impedance can still reach 18.5 GΩ and 5.8 GΩ at 100 Hz and 1 kHz respectively. The pre-simulation DC input
impedance with no NIC is 0.88 GΩ, which demonstrate an impedance boosting effect of about 24 times when the NIC is applied. Monte Carlo simulation is carried out to represent and analyze risk and uncertainty caused by process error and mismatch. Under the 725 sampling points, the average input impedance is about 17.85 GΩ and the standard deviation is 1.42 GΩ, as shown in Fig. 10. It reveals that the input impedance is stable and high enough under the process error and mismatch.

Monte Carlo simulation is carried out to represent and analyze risk and uncertainty caused by process error and mismatch. Under the 725 sampling points, the average input impedance is about 17.85 GΩ and the standard deviation is 1.42 GΩ, as shown in Fig. 10. It reveals that the input impedance is stable and high enough under the process error and mismatch.

Fig. 8  Layout capture of the proposed chopper IA

Fig. 9  Input impedance characteristics of pre-simulation, post-simulation and pre-simulation with no NIC

Fig. 10  Monte Carlo simulation results of input impedance

Fig. 11 shows the AC and noise characteristics of the proposed chopper IA. The passband gain is 41 dB with a 3 dB bandwidth of 6.5 kHz. The mid-band input referred noise power spectral density (PSD) is 130 nV/√Hz and the equivalent input noise is 9.7 μVrms integrated from 1 Hz to 6.5 kHz. The total current consumption is about 1.12 mA, thus the power consumption is 1.34 mW, and then the NEF can be calculated to be 4.89. The CMRR and PSRR at 50 Hz are 97 dB and 112 dB respectively, as shown in Fig. 12(a). Stimulated under a 1 mV, 1 kHz differential-mode signal with 600 mVpp, 50 Hz common-mode signal superimposed on it, the single port output spectrum of the chopper IA is shown in Fig. 12(b). It is indicated that the chopper IA can work properly with large common-mode interference. Compared with the previous works on chopper amplifier in Table I, the input impedance of the proposed architecture is much higher than the others, especially when the input frequency rising.

5. Conclusion

Using negative impedance convertor, basing on three-OTA instrumentation amplifier structure with chopping technique, a high input impedance fully integrated chopper IA is proposed in this letter. The negative impedance compensation theory is computed and analyzed in detail, through which the characteristics of this impedance boosting method is obtained. The proposed chopper IA is realized using 0.18 μm
standard CMOS process. The post-simulation results show that the input impedance of the amplifier is 18.9 GΩ at DC input, and it can still reach 5.8 GΩ at 1 kHz. Owing to chopping technique, mid-band input noise spectral density of 130 nV/√Hz, equivalent input noise of 9.7 μVrms integrated from 1 Hz to 6.5 kHz and NEF of 4.89 are obtained. With the common-mode feedback circuit block, common-mode input voltage tolerance of 600 mVpp and CMRR of 97 dB are achieved. It is indicated that the chopper IA is suitable for low-frequency sensor applications, such as biomedical, which require high input impedance, low noise and low power consumption.

Acknowledgments

This work was supported by Key-Area Research and Development Program of Guangdong Province (2019B010145001) and the National Natural Science Foundation of China (grant no. 61571196).

References

[1] C. Qian, et al.: “A micropower low-noise neural recording front-end circuit for epileptic seizure detection,” IEEE J. Solid-State Circuits 46 (2011) 1392 (DOI: 10.1109/JSSC.2011.2126370).

[2] F. Furbass, et al.: “An artificial intelligence-based EEG algorithm for detection of epileptiform EEG discharges: validation against the diagnostic gold standard,” Clinical Neurophysiology 131 (2020) 1174 (DOI: 10.1016/J.CNPH.2020.02.052).

[3] F.T. Sun, et al.: “Responsive cortical stimulation for the treatment of epilepsy,” Neurotherapeutics 5 (2008) 68 (DOI: 10.1016/J.NURT.2007.10.069).

[4] N. Jrad, et al.: “Automatic detection and classification of high-frequency oscillations in depth-EEG signals,” IEEE Trans. Biomed. Eng. 64 (2017) 2230 (DOI: 10.1109/tbme.2016.2633391).

[5] G. Buzsáki and A. Draguhn: “Neuronal oscillations in cortical networks,” Science 304 (2004) 1926 (DOI: 10.1126/SCIENCE.1099745).

[6] I. Akita and M. Ishida: “A current noise reduction technique in chopper instrumentation amplifier for high-impedance sensors,” IEICE Electron. Express, Vol.17, No.17, 1–6 (DOI: 10.1587/ELEX.2017.7530957).

[7] T. Denison, et al.: “A 2 μW 100 nV/√Hz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials,” IEEE J. Solid-State Circuits 42 (2007) 2934 (DOI: 10.1109/JSSC.2007.8997189).

[8] I.H. Stevenson and K.P. Kording: “How advances in neural recording affect data analysis,” Nature Neuroscience 14 (2011) 139 (DOI: 10.1038/NN.2731).

[9] Y. Masui, et al.: “Low power and low voltage chopper amplifier without LPI,” IEICE Electron. Express 5 (2008) 967 (DOI: 10.1587/ELEX.5.967).

[10] M. Somok and D.A. Hall: “A 13.9-nA ECG amplifier achieving 0.86/0.99 NEF/PEF using AC-coupled OTA-OTA-rocketing,” IEEE J. Solid-State Circuits 55 (2020) 414 (DOI: 10.1109/JSSC.2019.2957193).

[11] C.J. Lee and J.-J. Song: “A chopper stabilized current-feedback instrumentation amplifier for EEG acquisition application,” IEEE Access 7 (2019) 11565 (DOI: 10.1109/ACCESS.2019.2892502).

[12] D. Luo, et al.: “A low-noise chopper amplifier designed for multichannel neural signal acquisition,” IEEE J. Solid-State Circuits 54 (2019) 2555 (DOI: 10.1109/JSSC.2019.2913101).

[13] J. Zheng, et al.: “Chopper capacitively coupled instrumentation amplifier capable of handling large electrode offset for biopotential recordings,” IEEE Trans. Circuits Syst. 64 (2017) 1392 (DOI: 10.1109/TCSII.2017.2741348).

[14] Q. Fan, et al.: “A capacitively-coupled chopper operational amplifier with 3pV offset and outside-the-rail capability,” IEEE ESSCIRC (2012) 73 (DOI: 10.1109/ESSCIRC.2012.6341259).

[15] H. Chandrakumar and D. Marković: “An 80-mVpp linear-input range, 1.6-GΩ input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to 650-mVpp common-mode interference,” IEEE J. Solid-State Circuits 52 (2017) 2811 (DOI: 10.1109/JSSC.2017.2753824).

[16] A. Samiei and H. Hashemi: “A chopper stabilized, current feedback, neural recording amplifier,” IEEE Solid-State Circuits Lett. 2 (2019) 17 (DOI: 10.1109/LSSC.2019.2916754).

[17] M. Saad, et al.: “A chopper capacitive feedback instrumentation amplifier with input impedance boosting technique,” IEEE MWSCAS (2016) (DOI: 10.1109/MWSCAS.2016.7870153).

[18] W. Bai, et al.: “A 64.8 μW > 2.2 GΩ DC-AC configurable CMOS front-end IC for wearable ECG monitoring,” IEEE Sensors J. 18 (2018) 3400 (DOI: 10.1109/JSEN.2018.2809678).

[19] F. Butti, et al.: “A chopper instrumentation amplifier with input resistance boosting by means of synchronous dynamic element matching,” IEEE Trans. Circuits Syst. I, Reg. Papers 64 (2017) 753 (DOI: 10.1109/TCSI.2016.2633384).

[20] H. Yang, et al.: “Non-Foster matching of a resistively loaded Vee dipole antenna using operational amplifiers,” IEEE Trans. Antennas Propag. 64 (2016) 1477 (DOI: 10.1109/TAP.2015.2513090).

[21] J.G. Linvill: “Transistor negative impedance converters,” Proc. IRE 46 (1956) 5 (DOI: 10.1109/PROC.1956.2742151).

[22] P.V. Ananda Mohan, “On actively compensated amplifiers using negative impedance converters,” IEEE Trans. Circuits Syst. 67 (2020) 640 (DOI: 10.1109/TCSII.2019.2925094).

[23] E.M. Spinelli, et al.: “AC-coupled-front-end for biopotential measurements,” IEEE Trans. Biomed. Eng. 50 (2003) 391 (DOI: 10.1109/TBME.2003.808826).

[24] J.W. Huang, et al.: “A ECG offset cancelling readout circuit using a current mode feedback loop technique,” IEICE Electron. Express 15 (2018) 1 (DOI: 10.1587/ELEX.14.20170891).

[25] Y.-Y. Qian, et al.: “A high gain and high CMRR instrumentation amplifier for biomedical applications,” ICIIM (2019) 61 (DOI: 10.1109/ICIMC48536.2019.8977189).

[26] S. Monda and D.A. Hall: “An ECG chopper amplifier achieving 0.92 NEF and 0.85 PEF with AC-coupled inverter-stacking for noise efficiency enhancement,” IEEE ISCAS (2017) 1 (DOI: 10.1109/ISCAS.2017.8050957).

[27] M.S.J. Steyaert and W.C.M. Sansen: “A micropower low-noise monolithic instrumentation amplifier for medical purposes,” IEEE J. Solid-State Circuits 22 (1987) 1163 (DOI: 10.1109/JSSC.1987.1052869).

[28] Z. Liang, et al.: “A fully integrated chopper IA for implantable multichannel EEG recording without impedance boosting circuits,” IEEE APCCAS (2018) 143 (DOI: 10.1109/APCCAS.2018.8605664).

[29] T. Ling, et al.: “Chopping-out-of-band (COOB) for reducing ripple in chopper amplifiers,” IEICE Electron. Express 12 (2015) 1 (DOI: 10.1587/ELEX.12.20141226).

[30] C. Zhang, et al.: “A design of readout IC with capacitively-coupled chopper current-feedback instrumentation amplifier in a 0.18 μm CMOS process,” Analog Integrated Circuits and Signal Processing 102 (2020) 309 (DOI: 10.1007/S10470-019-01559-Y).

[31] F.H. Noshahr, et al.: “Multi-channel neural recording implants: a review,” Sensors 20 (2020) 904 (DOI: 10.3390/S2003904).