The relationship between the single event upset and the order of sensitive transistors in flip-flop layout

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Abstract. Traditionally, it is believed that only reverse biased PN junctions can collect ionized electron-hole pairs. Therefore, only the drain of the transistor in the off-state can be considered as a sensitive node, which is easy to absorb charge and cause upset. This paper finds that on-state transistors can also become sensitive nodes. This paper studies the relationship between SEU and the order of transistors in the flip-flop layout. It is found that the adjacent placement of on-state sensitive transistors can promote the occurrence of SEU, and a targeted hardened plan is proposed. The results of this paper are helpful for the design of the radiation-resistant layout of the flip-flop.

1. Introduction
As the size of devices shrinks, flip-flops are becoming more and more sensitive to single event upset (SEU) [1]. The lower supply voltage and reduced node capacitance reduce the critical charge that causes SEU. As technology develops, the close proximity of transistors leads to charge sharing among multiple nodes. Standard Dual Interlock Storage Cell (DICE) has been applied to flip-flops in deep submicron planar Complementary Metal Oxide Semiconductor (CMOS) technology to achieve low SEU rates [2,3]. However, DICE can only be immune to SEU caused by one node charge collection. The multi-node charge collection caused by charge sharing increases the SEU sensitivity of the DICE flip-flop. Some works have reported that the error rate of traditional DICE flip-flops is reduced by 30%-50% compared with the unreinforced flip-flop design using 40 nm technology [4]. In addition, the advantage in the 28 nm bulk silicon process is even smaller [1]. In order to better use DICE flip-flop in the future, it is necessary to analyze and strengthen its SEU-resistance performance. Based on the 28 nm bulk silicon process, this paper studies the DICE flip-flop and discovers the new characteristics of SEU related to the arrangement of transistors in layout. Through Technology Computer Aided Design (TCAD) simulation, the SEU characteristics of two different arrangements were compared, an abnormal upaet phenomenon was found, and hardened measure was proposed.

2. DICE flip-flop structure analysis
The traditional DICE flip-flop circuit structure is shown in Figure 1(a). The master stage and the slave stage are connected through C2MOS to avoid the mutual influence between the master and slave stages when affected by a single event, and it has good upset-resistant performance. As shown in Figure 1(b), the flip-flop layout can generally be divided into 4 parts: MP1/MN1, MP2/MN2, SP1/SN1 and SP2/SN2. The structure of MP1/MN1 and MP2/MN2 is roughly the same, SP1/SN1 and SP2/SN2 is roughly the same. In the layout design, the ordering method of the transistors in each part will affect its upset-resistant ability. There are two main sorting methods, the difference lies in the placement of the main
transistors (M0/M2/S0/S2 node transistors). The following focuses on comparing the two placement methods, as shown in Figure 2, where (a) the master and slave stages use different sorting methods, named Array A, (b) the master and slave stages use the same sorting method, which named Array B. In Array A, due to the different sorting methods, the two larger sensitive transistors in the box are placed next to each other. Although the two belong to the master and slave stages, and the C2MOS connection between the master and slave stages can avoid reverse conduction. But adjacent placement may affect each other and change the overall charge collection situation. In Array B, the master and slave stages use the same sorting method, so that the sensitive nodes are uniformly distributed in the layout, which helps to improve the charge sharing situation.

Figure 1. (a) The circuit diagram of C2MOS structure flip-flop, (b) layout of flip-flop.

Figure 2. (a) The layout of the Array A method, (b) the layout of the Array B method.

3. TCAD simulation

In our previous work, TCAD simulation is an effective means to study the physical mechanism of single event effects [5,6]. In this paper, we use the TCAD tool to validate our method. The PMOS and NMOS transistors in each TCAD model are calibrated to match the electrical characteristics obtained from the standard compact model of the corresponding commercial 28 nm bulk silicon technology. The power supply voltage is set to 0.9V, and the Linear Energy Transfer (LET) value is set to 40 MeV·cm²/mg. The physical models used in the simulation include Fermi-Dirac statistics, band gap narrowing effect, Auger recombination and doping dependent, electric field dependent, and carrier-carrier scattering mobility models. Unless otherwise specified, the default models and parameters provided by TCAD tools are used. In four different input conditions (D=0, CK=0, D=0, CK=1, D=1, CK=0 and D=1, CK=1), the
drain centers of the 16 transistors are struck in the vertical direction. The results of the strike are shown in Table 1.

Table 1. Upset results in TCAD simulation.

| Layout type | Input condition | Upset node |
|-------------|-----------------|------------|
| Array A     | D=1, CK=0       | S0 PMOS    |
|             | D=1, CK=1       | S0 PMOS    |
| Array B     | All the four conditions | No upset |

4. Discussion and improvement

4.1. Discussion on the effects of the two layout methods

Traditionally, it is believed that only reverse-biased PN junctions can collect ionized electron-hole pairs. Therefore, only the drain of the transistor in the off-state can be considered as a sensitive node, and it is easy to absorb charge and cause upset. In Array A, when D=1, CK=0 and D=1, CK=1, the strike of S0 PMOS produced upset. The S0 PMOS is in the on-state during the strike, which is different from traditional cognition. Analyze the voltage and current after the strike. Take D=1, CK=0, strike the center of the S0 PMOS drain in Array A as an example. As shown in Figure 3, after the strike, the S1 node is closer to the strike node, and the holes that have diffused are collected immediately, and the S3 node is farther away, and the holes are collected after a period of time. The PMOS at the S2 node is turned on, but the NMOS is driven by the S1 node, and the node potential is reduced to a certain extent. After the S3 node potential rises, the PMOS is turned off with its control, and then the node potential becomes 0. Under the influence of the upset of the three nodes, the potential of the S0 node begins to drop, but there are still a large number of electron-hole pairs at the node PMOS, and the PMOS drain will continue to absorb holes to delay the upset. After the excess holes are consumed, the potential eventually drops to 0.

Figure 3. (a) The voltage distribution after the strike, (b) the current distribution after the strike.

At the same time, the source of two adjacent transistors at the strike node is analyzed. The source hole currents are shown in Figure 4(a), the S0 node PMOS source hole current is first negative and then positive, which means that after the strike, the source first absorbs a small amount of holes and then releases a large amount of holes. The M2 node PMOS source also releases a lot of holes. The overall potential is shown in Figure 4(b). The top is the strike moment, and the bottom is 100ps after the strike. It can be found that after the strike, the generated electrons and holes cause the potential disturbance between the N well and the P substrate, which turns on the PNP bipolar transistor of PMOS drain-N well-P substrate. As shown in Figure 4(c), it is the hole current section of the S0 node PMOS source, the
left is the strike moment, and the right is 100ps after the strike. The source injects holes, diffuses to the P substrate through the N well, and is absorbed by the substrate contact. When the bipolar transistor is turned on, the N-well will actively inject and diffuse holes continuously, affecting other nearby transistors.

Comparing the result of strike the M2 PMOS drain center in Array B, as shown in Figure 5, (a) is the hole current distribution at the time of strike, (b) is the hole current at 100 ps after the strike. It can be found that after separating the two larger-sized transistors, the strike cannot generate enough electron-hole pairs, and the potential disturbance of the well is small. The bipolar amplification effect may be generated locally, and the duration is short, and the impact is small. As shown in Figure 5(c), the two sources connected to VDD on the left and right of the strike point generate small hole current. A small amount of holes is not enough to cause a multi-node upset.
4.2. Hardened method

The comparison shows that placing two larger sensitive PMOS transistors adjacent to each other will increase the electron-hole pairs generated by strike, aggravate the well potential perturbation, enhance the bipolar amplification effect, and inject more holes into the N-well, increasing the probability of upset. To strengthen it, the transistors can be folded to form a "source-drain-source" structure, reduce the volume of the sensitive area, increase the distance between the transistor and the P substrate, and increase the distance between the sensitive transistors. As shown in Figure 6, the transistors at nodes M0, M2, S0, and S2 are folded in a "source-drain-source" manner. Simulation was performed after folding, and no upset was found. When D=1 and CK=0, the result of striking the drain center of S0 PMOS in Array A is shown in the Figure 6. Similar to the above-mentioned separate transistor, the strike produces fewer electron-hole pairs, and the two sources of S0 PMOS do not release holes, indicating that there is no obvious bipolar amplification effect, and the S3 node is almost unaffected.
5. Conclusion

In this paper, we have studied the relationship between the SEU and the transistor ordering of flip-flops when the layout is implemented. It was discovered for the first time that the proximity of an on-state sensitive transistor would worsen the single event effect, enhance the bipolar amplification effect, and promote the occurrence of SEU. The proposed method of folding the transistor can enhance the SEU-resistant ability of the flip-flop. The findings in this paper are a further explanation of the upset phenomenon of the flip-flop, which is helpful for the design of the radiation-hardened layout of the flip-flop. The proposed hardened method can also be widely applied to various radiation-hardened circuits.

References

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