MEMORY-EFFICIENT SPEECH RECOGNITION ON SMART DEVICES

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ABSTRACT
Recurrent transducer models have emerged as a promising solution for speech recognition on the current and next generation smart devices. The transducer models provide competitive accuracy within a reasonable memory footprint alleviating the memory capacity constraints in these devices. However, these models access parameters from off-chip memory for every input time step which adversely affects device battery life and limits their usability on low-power devices.

We address transducer model’s memory access concerns by optimizing their model architecture and designing novel recurrent cell designs. We demonstrate that i) model’s energy cost is dominated by accessing model weights from off-chip memory, ii) transducer model architecture is pivotal in determining the number of accesses to off-chip memory and just model size is not a good proxy, iii) our transducer model optimizations and novel recurrent cell reduces off-chip memory accesses by $4.5 \times$ and model size by $2 \times$ with minimal accuracy impact.

Index Terms— RNN-T, ASR, Recurrent Transducer, Automatic Speech Recognition, On-device Inference

1 Introduction
Speech is a natural interface for the “smart” devices around us – especially the emerging class of keyboard-/screen-less devices such as assistant, watch, glass amongst others. Given the tremendous growth and adoption of these new devices, we expect speech to be primary mode of interaction for humans with their devices going forward. As a result, there is a lot of interest in building on-device speech recognition to improve their reliability and latency as well as address user data privacy concerns. While the previous attempts at building on-device ASR involved scaling down traditional, memory-heavy multi-model system [1, 2] (acoustic/pronunciation/language models), recent work on Recurrent Transducer models [3] (originally described in [4]) have shown promise for the general problem of speech recognition using an end-to-end neural model. Their compact size addresses the memory capacity constraints while providing accuracy comparable to the larger server-side models.

While the recurrent transducer models address the memory capacity constraints, their execution still relies on fetching weights from off-chip memory for every input speech frame. This repeated access of weights from off-chip memory makes the model inefficient because the cost of accessing memory is significantly higher than accessing on-chip buffers as well as performing computations (Figure 1). Transducer model’s memory heavy behavior can limit their ability to run on low-end devices with slow off-chip memory. In this work, we significantly reduce off-chip memory accesses by redesigning transducer model such that it can access model parameters primarily from on-chip buffers. We find that the number of off-chip memory accesses is not just proportional to the model size but rather depends on the per-layer parameter count as well as how we schedule across time steps and layers. This work makes the following contributions:

• **Efficient Transducer model architecture** that reduces the number of off-chip memory accesses for model parameters.
• **Novel recurrent cell design** that models the cell state as a matrix instead of a vector. This gives us more flexibility in terms of sizing a layer to fit within on-chip buffers.
• **Memory-efficient Model**: We reduce memory accesses by $4.5 \times$ and model size by $2 \times$ without loss in accuracy.

2 Recurrent Transducer Model
This section presents an overview of Recurrent Transducer networks [3, 4] and challenges in deploying them on low-end smart devices. The recurrent transducer network (Figure 2) consists of three components — encoder works on the input audio stream, prediction uses the previously predicted symbols to guide the next symbol and joint network combines the two networks to produce the probability distribution of the next symbol. Encoder is the largest component of the transducer network and also executes the most often because the number of input speech frames are much higher than the output word pieces. We focus on encoder in this work.
2.1 Encoder Network Architecture

Encoder accepts as input the audio stream preprocessed into features and runs them through a multi-layer LSTM [8] (Figure 2) network to produce feature representation. Our encoder uses unidirectional LSTMs to target the streamlining behavior.

**Compute Building Block:** LSTMs take as input vector for current time step \( x_t \) and hidden state from previous time step \( h_{t-1} \). It uses three gates – input \( i \), forget \( f \) and output \( o \) to update the cell memory \( c \) and produce new hidden state vector \( h_t \) for the next time step. Current day networks typically stack multiple layers of the LSTM cells where the hidden state output of a layer is fed as input to the next layer as input \( x_{t+1} \). To aid with training stability and efficiency, speech models such as RNNT [3] use LayerNorm [9] (shown as \( ln \) in equations) within the LSTM to normalize the cell, gate and output calculations.

\[
\begin{align*}
    f_t, i_t, c_t, o_t &= ln(W_f, W_i, W_c, W_o) \cdot [h_{t-1}, x_t]^T \\
    f_t, i_t, o_t &= \text{sigmoid}(f_t, i_t, o_t) \\
    c_t &= \text{tanh}(c_t) \\
    o_t &= \text{tanh}(c_t) \\
    h_t &= o_t \ast \text{tanh}(c_t)
\end{align*}
\]

**Time Reduction Layer:** This layer merges features from neighboring time steps into a single embedding vector – a common reduction technique being concatenation. This layer is motivated by the observation that there are many more input speech frames (one every 10 ms or so) than the number of output tokens (word pieces). Time reduction helps address this imbalance which improves the training stability [10].

2.2 Encoder Computation Scheduling

**Execute one speech utterance per encoder inference:** The basic scheduling would run the whole encoder network for every new speech frame. In this scheme, we will fetch all the model parameters from off-chip memory every time step.

**Batch “B” time steps:** An alternative would be to wait for \( B \) speech frames and execute encoder on all of them. By doing so, we fetch weights for the input-to-hidden path \( W_{ih} \) in Figure 2 only once for “B” time steps. However, we still need to fetch weights for hidden-to-hidden path \( W_{hh} \) in Figure 2 “B” times from off-chip memory because of the sequential dependence between each time step calculation.

In either scheme, we need to fetch model parameters from off-chip memory for each input speech frame. Section 3 discusses how to optimize away this need for repeated off-chip memory access of model parameters.

2.3 Deployment challenges

While LSTM-based encoder models achieve high accuracy for streaming speech recognition [3], there are many challenges in deploying them on smart devices.

**Repeated access to model parameters:** These models need to access model parameters at each input time step as shown in Section 2.2.

**Large memory footprint:** An LSTM layer has \( O(8d^2) \) parameters where \( d \) is the dimension of the input:hidden

2.4 Efficient RNNT Variations

Prior work has looked at addressing these RNNT inefficiencies by using LSTM variants such as CIFG [11, 12, 13]. While model size is a popular target metric for optimization, we instead use expected memory access efficiency by appropriately designing RNN-T model. Our work focuses on developing novel LSTM variants and sizing them appropriately so that we can maintain speech model accuracy while improving its memory access efficiency. We demonstrate that there is scope for large, non-linear improvements in memory access efficiency by appropriately designing RNN-T model.
3 Optimizing Transducer Models

We inspect various components of the transducer encoder and propose variations to improve model efficiency. In particular, we optimize layer normalization, time reduction, simplify multi-layer stacking and allow reducing layer size without hurting its cell memory size. We show our modified cell equation and highlight the changes with a box.

3.1 Layer Normalization

Layer Normalization (ln) helps stabilize training by normalizing the output of the compute layers. The original implementation normalizes values across all the gates (i, f, o gate) and cell state (c). Given the very different downstream usage of gates and cell state, it is not clear why they should be normalized together. An alternative would be normalizing them separately [14], but that makes it hard for gates to be all small or large needed to mostly forget or carry over past state.

We use layer normalization only to normalize cell state computation. In our experiments, we see that this provides similar training stability while being more efficient at inference time because we can skip normalization of gates.

\[
fp_t, ip_t, cp_t, o_t = ([W_f, W_i, W_c, W_o] \cdot [h_{t-1}, x_t]^T)
\]

\[
f_t, i_t, o_t = \text{sigmoid}(fp_t, ip_t, op_t)
\]

\[
\hat{c}_t = \text{tanh}(\text{ln}(cp_t))
\]

\[
c_t = \ln(f_t \cdot c_{t-1} + i_t \cdot \hat{c}_t)
\]

\[
h_t = o_t \cdot \text{tanh}(c_t)
\]

3.2 Internally Stacked Recurrent Cells

This technique simplifies layer stacking and reduces its cost. The current approach for multi-layer stacked recurrent networks stack another LSTM layer on top. Our approach explores stacking internal to the recurrent cell by just building a deeper network for cell memory and hidden state computation. This provides a network designer additional knobs in terms of achieving extra depth with minimal increase in parameters and network complexity.

\[
fp_t, ip_t, cp_t, o_t = ([W_f, W_i, W_c, W_o] \cdot [h_{t-1}, x_t]^T)
\]

\[
f_t, i_t, o_t = \text{sigmoid}(fp_t, ip_t, op_t)
\]

\[
\hat{c}_t = \text{tanh}(\text{ln}(cp_t))
\]

\[
c_t = \ln(f_t \cdot c_{t-1} + i_t \cdot \hat{c}_t)
\]

\[
h_t = o_t \cdot \text{tanh}(c_t)
\]

3.3 Two-dimensional Cell Memory

We extend the traditional LSTM cells with two-dimensional cell memory instead of a vector which is single dimensional. The motivation is as follows - when we reduce the LSTM layer size by reducing the hidden-state size, we also reduce the memory capacity of the layer since cell memory size and hidden state is proportional to the hidden size. In our approach, we model cell memory as \(h \times v\) matrix where \(h\) is the hidden state size and \(v\) is the number of cell memory vectors in the recurrent cell. By doing so, we can reduce the hidden state size without reducing the cell memory by increasing \(v\).

\[
fp_t, ip_t, cp_t, o_t = ([W_f, W_i, W_c, W_o] \cdot [h_{t-1}, x_t]^T)
\]

\[
f_t, i_t, o_t = \text{sigmoid}(fp_t, ip_t, op_t)
\]

\[
Cm_t = \text{ln}(W_{ch} \cdot cp_t).\text{view}(h, v)
\]

\[
\hat{c}_t = \text{tanh}(Cm_t)
\]

\[
C_t = \ln(f_t \cdot C_{t-1} + i_t \cdot \hat{c}_t)
\]

\[
Hm_t = o_t \cdot \text{tanh}(C_t)
\]

\[
h_t = Hm_t.\text{view}(h \times v)
\]

3.4 Time Reduction Layer

To reduce the number of tokens flowing through the encoder network, a common time reduction layer step is using concatenation [3]. This does come at the cost of an increase in number of parameters. We simplify the time reduction step by replacing concatenation to mean. By doing so, we can i) reduce the model size without impacting accuracy, ii) reduce the number of memory accesses and compute in a pretrained model by changing number the time reduction factor without any change to network weight shape. This allows us to quickly adapt a trained model to smart device’s memory constraints without having to train a new model.

4 Results

In this section, we demonstrate that i) model size is a poor proxy to approximate it’s expected off-chip memory accesses, ii) our transducer architecture optimizations and novel recurrent cell reduces the encoder size by 2.5× and iii) we achieve super-linear savings in off-chip memory access of 4.5× demonstrating that model size is not proportional to off-chip memory access. To demonstrate the above points, we construct and train the following model variations (Table 1):

B This is our baseline network based on RNNT paper [3] that uses multi-layer stacked LSTMs. We scale the model size down to below 40 MB. This model’s encoder has two time reductions layers that each reduce the token count by 2×.

E1 We change time reduction operator from concatenation to mean with no impact on accuracy.

E2 We build a deeper variant of the network where each layer is skinnier (1.78× smaller). However, it does not converge.

E3 Replacing LSTM with its residual [15] variant helps the network converge and recover the original accuracy.

E4 Replacing LSTMs with CIFG [11] helps us achieve further reduce model size for a very modest accuracy hit.

E5 Adding greater depth via internal stacking (IS) following the time reduction layer helps us recover accuracy with almost no increase in parameter count.

E6 Replacing CIFG with our novel two-dimensional cell memory (2D) allows us to reduce hidden dimension from 480 to 256 with minimal accuracy impact. Our novel design reduces the hidden dimension of the recurrent cell without reducing the cell memory size.

E7 We further reduce the model size by building a deeper model with skinnier cells (200 hidden state).
Significant Model Size Reductions

We would like to highlight the following observations:

- learning rate of 0.0004 and polynomial scaling by factor of 4.2
- ADAM optimizer for 75 epochs with 61 epochs on a constant

We train the model variations on Librispeech [16] – we use

4.1 Optimizing Off-chip Memory Accesses

We start by demonstrating that designing a model to be on-
chip buffer aware is critical. For this discussion, we focus on
one LSTM layer with hidden state size H and say it can work
on T input samples at once (for streaming use cases T can be
4 - 16 incurring 100 - 200 ms model latency). As shown in
Figure 3 when a layer’s recurrent path (Whm in Figure 2) can
fit on-chip (Memory-Opt), then it accesses off-chip memory
much less often (up to 8× lower) than the baseline scenario
where the layer needs to fetch weights from off-chip mem-
ory for every speech utterance. Since off-chip memory ac-
cesses dominate Transducer’s execution (Figure 1), replacing
them with on-chip memory accesses enables efficient speech
recognition on low-end devices.

To realize the above gains, each layer should be small
enough to fit within on-chip buffers. In the next section, we
show how our optimizations can reduce the per-layer size by
more than 3× with minimal accuracy impact.

4.2 Accuracy Evaluation

We train the model variations on Librispeech [16] – we use ADAM optimizer for 75 epochs with 61 epochs on a constant
learning rate of 0.0004 and polynomial scaling by factor of 0.8. Table 1 shows the results from the various configurations.
We would like to highlight the following observations:

- Significant Model Size Reductions: Our model and layer
optimizations can reduce the model size by 2× with minimal
accuracy impact. Furthermore, we spread the smaller
model size across a greater number of layers which reduces
on average per-layer size by more than 3×. This makes the
design amenable to utilizing on-chip buffers for each layer.

- LayerNorm on Cell state is enough: Experiments from E5-
E7 only use layer normalization for the cell state and we did
not see any network training stability issues.

- Internal Stacking is Efficient (E4 → E5): Using internal
stacking to increase depth by 2 improves accuracy with
negligible increase in the model size.

- 2D cell state allows hidden-state reduction (E5 → E7):
We can reduce the hidden state dimension significantly
(E6 and E7) with modest accuracy impact accuracy by re-
presenting the cell memory and hidden state as a 2D matrix.
This allows us to reduce a layer’s parameter count without
impact its representation power.

4.3 Efficiency Evaluation

This section discusses the improvement in execution effi-
ciency from our model optimizations. For this analysis, we
assume a mobile system with a modest resource of ~512 KB
on-chip buffer. Table 2 shows reduction in off-chip memory accesses – we reduce it to 0.57× by optimizing the
transducer model architecture (E3) and to 0.22× by using our
novel recurrent cells. We also note that reduction in memory
accesses are higher than the reduction in the model size re-
forcing our observation that the savings come from a more
efficient model design and not just from model size reduction.

5 Discussion and Future Directions

Our work significantly reduces the memory traffic in a speech
model inference without compromising on the accuracy. We
believe this will be critical in providing high-quality speech
support on the next generation devices such as smart-watch,
AR-glass among others that will have limited memory re-
sources as well as severe power constraints. Further efficiency
gains are possible by combining our approach with pruning,
quantization and neural architecture search. Another related
line of work would be post-training adaptation of a trained
speech recognition model for deployment on different target
devices, since the memory traffic overhead on a phone, watch
and glass will vary substantially. Our technique of using mean
in the time-reduction layer instead of concat enables adapting
a model post-training. For example, by increasing the time-
reduction factor we can reduce the memory accesses by more
than 20% while recovering much of the accuracy with quick
fine-tuning. This in combination with other techniques such as
LayerDrop [18] can provide significant deployment flexi-
bility and reduce the need to train many different models.

6 Conclusion

We propose an optimized transducer model architecture built
with a novel recurrent cell design that reduces its off-chip
memory accesses by 4.5× and model size by 2.5×. With
our architecture optimizations, we can enable high accuracy
speech recognition support on low-end smart devices.
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