Supporting information

Highly Reliable Flexible Device with Charge Compensation Layer

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Figure S1. The initial electrical characteristics of the Devices. (a) Device A (a-IGZO TFTs as SiO$_2$ barrier layer over the glass substrate). (b) Device B (a-IGZO TFTs as SiO$_2$ barrier layer over the PI substrate). (c) Device C (a-IGZO TFTs as SiO$_2$/SiCOH barrier layer over the PI substrate).

Figure S1 presents the results of the initial electrical parameters of a-IGZO TFTs. The $V_{th}$, hysteresis voltage, and field effect mobility were extracted from five samples for each type of TFTs and compared in a box plot.
Figure S2. Vertical cross-sections by SEM to measure the thicknesses of MIM capacitor dielectrics. (a) PI thickness of MIM A with an Al/SiO$_2$/PI/Al structure. (b) Enlarged image of MIM A to measure the SiO$_2$ thickness. (c) Measured PI thickness of MIM B with Al/SiO$_2$/SiCOH/PI/Al. The measured PI thickness was similar to the measured PI in MIM A. (d) Enlarged image of MIM B to measure the thickness of SiO$_2$ and SiCOH. Total barrier thickness was controlled to 300 nm for both MIM A and MIM B.
Figure S3. C–V plots before and after NBTS of MIM capacitors. (a) C–V plot of MIM A with increasing applied voltage. (b) C–V plot of MIM B with increasing applied voltage. Voltage of −10 V, −20 V, and −30 V were applied to the top electrode of the MIM capacitor, and C–V measurements were taken at 70 °C. The change in capacitance under the bias stress was larger in MIM A than in MIM B.

Figure S3 presents the results of the C–V measurement of MIM capacitors with different structures. Changes in capacitance were conducted by applying voltages of −10 V, −20 V, and −30 V at 70 °C to the top electrode of the MIM capacitors. In the MIM A capacitor with the SiO$_2$ barrier layer, the change in capacitance increased as the voltage increased, but the MIM B capacitor with the SiO$_2$/SiCOH bilayer showed no change in the capacitance even with increased voltages.
Figure S4. I–V plot before/after NBTS of MIM capacitors. (a) I–V plot of MIM A with increasing applied voltage. (b) I–V plot of MIM B with increasing applied voltage. Voltages of −10 V, −20 V, and −30 V were applied to the top electrode of the MIM capacitor, and I–V measurements were taken at 70 °C. The change in current under the bias stress was larger in MIM A than in MIM B.

Figure S4 depicts the I–V plots of the MIM capacitors according to the applied voltage stress at 70 °C. The I–V results show the leakage currents of MIM A and MIM B with the applied voltage; however, MIM B showed fewer fluctuations in the leakage current according to the applied voltage. Two main reasons are possible for the increase in the leakage current of the MIM capacitors under bias. First, the bonds of the molecular chains inside the PI were broken by the injected electrons, resulting in defect generation, which increases the leakage current. The second reason is related to the density of the insulator, including the barrier layers. If the density of the layer is low, the leakage current path increases by the accumulated voltage stress. However, it can be assumed that the first reason is the main cause of leakage current fluctuations because the density of SiO$_2$ is much larger than that of SiCOH as a barrier layer.
Figure S5. The electric field after a NBTS of the MIM capacitor, extracted from the changing capacitance amount of PI as a function of the applied voltage.

After NBTS, the amount of change in capacitance was obtained through the C–V curve of MIM capacitors, and the charge change in Coulombs ($\Delta Q$) value was extracted from the equation $\Delta Q = \Delta C \times V$. To confirm whether it can affect the a-IGZO TFT active area fabricated on the PI substrate, the extracted charge can be converted into an electric field ($E = V/d$) that affects the actual active layer in the PI/barrier/a-IGZO TFT structure. Figure S5 shows the accumulated electric field in the interface between the PI and barrier layer as a bar graph.
Figure S6. KPFM analysis principles and sample preparation process for measurement. (a) Energy level of the sample and tip when separated by a certain distance \(d\) in the absence of an electrical contact. (b) The energy level between the sample and the tip during electrical contact. (c) Compensation by externally applying the same DC bias as \(V_{CPD}\). (d) Sample preparation process for KPFM. Step 1: In the MIM structure, cut the top electrode in half along the red line in the figure. Step 2: To apply voltage to the top and bottom electrodes during KPFM measurement, wire both the top electrode and bottom electrodes and then mold with resin. Step 3: Polish the resin until the cut top electrode is exposed for KPFM measurements. Step 4: Apply KPFM before and after applying voltage stress. The voltage stress can be applied through the wires connected to the top and bottom electrode.

KPFM is an AFM-based technique used to study the electronic properties of nanoscale materials and devices. KPFM detects the electrostatic force and measures the CPD between the AFM probe and the sample surface, which is caused by the difference in the work function of the material itself, the surface charge, and non-equilibrium charging, such as dipole and photo-induced charge separation\(^1\)\(^2\). The probe and sample form an effective capacitor, and the stored energy is expressed by:

\[
U_{cap} = \frac{1}{2}C(\Delta V)^2
\]

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where $C$ is the capacitance between the probe and the sample and $\Delta V$ is the difference in charge potential between the probe and the sample surface. The force acting on the probe can be obtained at this time by differentiating the energy of the above equation by the distance $d$ between the probe and the sample surface:

$$\frac{\partial U_{\text{cap}}}{\partial d} \equiv F_{\text{cap}} = -\frac{1}{2\varepsilon_0} \frac{\partial C}{\partial d} (\Delta V)^2$$

and $\Delta V$ can be expressed as:

$$\Delta V = \Delta V_{\text{DC}} + \Delta V_{\text{AC}} \sin \omega \Phi \sin \omega K_P t$$

where $\omega K_P$ is the vibration frequency of the Kelvin probe. Also, $\Delta V_{\text{DC}}$ can be expressed as a separate equation, in which $\Delta V_{\text{DC,cap}}$ is the difference in the DC potential energy of the capacitor, $\Delta \Phi_S$ is the difference in the surface potential between the probe and the sample surface, and $\Delta \Phi_S = eV_{\text{CPD}}$. $V_{\text{CPD}}$ can be expressed as:

$$V_{\text{CPD}} = \frac{\Phi_s - \Phi_t}{\varepsilon}$$

Figure S6a–c shows the principle of KPFM. This is based on the alignment of the Fermi level when two conductive or semiconducting materials are in electrical contact. One material represents the sample, while the other is the conductive AFM tip with work functions of $\Phi_s$ and $\Phi_t$, respectively (Figure S6a). In Figure S6b, when an electrical contact occurs between the tip and the sample, the sample and the Fermi level of the tip are aligned as electrons flow from the sample to the tip. This in turn causes a contact potential difference ($V_{\text{CPD}}$) between the tip and the sample. In KPFM, $V_{\text{CPD}}$ is compensated at each point of the scan by applying a DC bias ($V_{\text{DC}}$) that equals $V_{\text{CPD}}$, as shown in Figure S6c.

Figure S6d shows the sampling procedure for KPFM analysis of a MIM capacitor and consists of 4 steps. Step 1: The MIM capacitor structures are cut across the top electrode along the red line marked in the figure. Step 2: Wires are connected to the bottom electrode and the cut part of the top electrode to apply voltage stress during KPFM measurement, and then the samples are packaged with resin. Step 3: The cut side of samples are polished until the electrode and dielectric are exposed to allow the measurement tip to scan the MIM capacitor vertically. Step 4: A potential profile using KPFM along the top to bottom electrode of the MIM capacitor structure is measured before and after voltage stress through the wires.
Figure S7. A flexible OLED display image-sticking evaluation method and driving circuit. (a) Three steps of the method for evaluating the image-sticking of the panel progressed in the chess pattern. (b) Images-sticking (image retention) on the flexible display panel. (c) A pixel-driving circuit of a panel composed of six transistors and one capacitor (Cst). (d) Change in panel luminance according to the $\Delta V_{th}$ change of each TFT. When the $V_{th}$ of the T1 and T3 TFTs is shifted positively, the luminance decreases, and when the $V_{th}$ is shifted negatively, the luminance increases.

Image-sticking, which is an indicator of display quality, is a phenomenon in which the previous screen affects the next screen. Figure S7a shows the method for evaluating image-sticking in a display panel\textsuperscript{3,4}. The methods consists of three main steps. The first step is to measure the luminance of the center of the panel in the state of 64 gray patterns. The next step is to perform aging for a certain period of time in a chessboard pattern of an alternating grid of white and black squares. The last step is to measure the luminance again in the area where the luminance was initially measured in the 64-gray-patterns state on the panel. After aging, the degree to which the luminance exceeds a certain level compared to the initial luminance is defined as an image-sticking time value. The flexible display currently being manufactured on the PI substrate has an afterimage phenomenon, as shown in Figure S7b, in which the luminance decreases in the aging region of the black pattern.

Image-sticking may be caused by a $V_{th}$ shift of a specific TFT in the pixel circuit. Because OLED display panels are manufactured on a large substrate, the $V_{th}$ distribution is not optimal. As shown in Figure S7c, a Vth
compensation circuit is applied and used to supply a constant current to the driving TFT. Figure S7d provides the results of a simulation testing whether the $V_{th}$ of six TFTs constituting a pixel circuit changes from $-5$ V to 5 V to cause a change in panel luminance. The results confirm that the change in $V_{th}$ of the TFT (T3) serving as the compensation circuit causes a panel luminance deviation, and that the luminance increases or decreases according to the direction of the $V_{th}$ shift.
Table S1. Electrical properties of a–IGZO TFT before and after NBTS.

| Parameter                  | Device A | Device B | Device C |
|----------------------------|----------|----------|----------|
| $V_{th}$ (V)               | 1.36     | 1.43     | 1.31     |
| $\mu_{FE}$ (cm$^2$/V·s)   | 24.9     | 24.9     | 25       |
| $\Delta V_{HYS}$ (V)       | 0.06     | 0.06     | 0.06     |
| $S.S$ (V/dec)              | 0.11     | 0.12     | 0.12     |
| $\Delta V_{th}$ (V) after NBTS | -0.36    | 0.45     | -0.25    |
| $\Delta S.S$ (V/dec) after NBTS | 0.047    | 0.018    | 0.022    |

Table S2. Material parameters extracted from the SEM and C–V measurement.

|               | PI       | SiO$_2$  | SiO$_2$/SiCOH |
|---------------|----------|----------|---------------|
| Thickness (µm)| 5        | 0.3      | 0.15/0.15     |
| Dielectric constant | 3.92 | 3.9 | -             |
| Capacitance (F) | $3.72\cdot10^{-11}$ | $8.13\cdot10^{-12}$ | $1.40\cdot10^{-12}$ |
Supporting Information References

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