An experimental evidence-based computational paradigm for new logic-gates in neuronal activity

R. Vardi1, S. Guberman1,2, A. Goldental2 and I. Kanter1,2

1 Gonda Interdisciplinary Brain Research Center, and the Goodman Faculty of Life Sciences, Bar-Ilan University Ramat-Gan 52900, Israel
2 Department of Physics, Bar-Ilan University - Ramat-Gan 52900, Israel

received 19 August 2013; accepted 13 September 2013
published online 25 September 2013

PACS 64.60.aq – Networks
PACS 87.18.Sn – Neural networks and synaptic communication
PACS 05.45.Tp – Time series analysis

Abstract – We propose a new experimentally corroborated paradigm in which the functionality of the brain’s logic-gates depends on the history of their activity, e.g. an OR-gate that turns into a XOR-gate over time. Our results are based on an experimental procedure where conditioned stimulations were enforced on circuits of neurons embedded within a large-scale network of cortical cells in vitro. The underlying biological mechanism is the unavoidable increase of neuronal response latency to ongoing stimulations, which imposes a non-uniform gradual stretching of network delays.

Introduction. – This year we are celebrating the 70th anniversary of the publication of the seminal work by McCulloch and Pitts “A logical calculus of the ideas immanent in nervous activity” [1]. They suggested that the brain is composed of threshold units, neurons, composing reliable logic-gates similar to the logic at the core of today’s computers. This suggested computational framework had a tremendous impact on the development of artificial neural networks [2] and machine learning theory [3]. Nevertheless, it is fair to conclude that the concept of simplified neurons had a limited impact on neuroscience, as measurements indicated that neurons exhibit much richer spatial and temporal dynamics, which are far from pure Boolean elements [4].

The long-lasting rejection of this simplified neuronal framework left the fundamental concept of the computational abilities of the nervous system unclear [5]. In the present study, we propose a new experimentally corroborated paradigm in which the logical operations of the brain differ from the logic of computers. Unlike a burned gate on a designed chip that consistently follows the same truth table, here the functionality of the brains logic-gates depends on the history of their activity, i.e. the truth tables are time dependent. Our results are based on an experimental procedure where conditioned stimulations were enforced on circuits of neurons embedded within a large-scale network of cortical cells in vitro (i.e. if neuron A is driven by neuron B in the neuronal circuit, then conditioned to an evoked spike of A, we stimulate B after a predefined time delay) [6,7]. We demonstrate that the underlying biological mechanism is an unavoidable increase of neuronal response latency [8–10] to ongoing stimulations, which imposes a non-uniform gradual stretching of delays associated with the neuronal circuit [11]. We anticipate that our results will lead to a better understanding of the suitability of this computational paradigm to account for the brains functionalities. In addition, this paradigm will require the development of new systematic methods and practical tools beyond traditional Boolean algebra methods [12] which have been observed and exemplified for some neuronal configurations [13,14].

Elastic response latency — single neuron. – At the single-neuron level, one of the most significant time-dependent features is the neuronal response latency that measures the elapsed time between the beginning of the stimulation and the evoked spike. The latency is typically on the order of several milliseconds [9,11] which reflects the neuronal internal dynamics [15]. To exemplify this neuronal feature, experiments with a stimulation rate of 10 Hz (fig. 1(a)) were conducted on cultured cortical neurons that were functionally isolated from their network using a cocktail of synaptic blockers (“Methods” section). The stimulated neuron typically responded to each and every...
μ per evoked spike, which introduces a finer time scale, (fig. 1(a)). The results indicate a stretching of a few by a few ms over a few hundreds of repeated stimulations stimulus with high reliability and the latency increased by a few ms over a few hundreds of repeated stimulations (fig. 1(a)). The results indicate a stretching of a few μs per evoked spike, which introduces a linear time scale, μs, of cortical dynamics [11]. Specifically, for the first several stimulations the stretching per spike is typically a few dozen μs followed by a fast decay to a roughly linear stretching of only several μs per spike until the neuron enters an intermittent phase, characterized by relatively large fluctuations of the latency around an average value (fig. 1(a)). This fully reversible phenomenon of neuronal response stretching occurs for stimulation rates exceeding ~5 Hz and is typically enhanced with the increase of stimulation rates [9,11].

Fig. 1: (Color online) Stretching of the neuronal response latency to ongoing stimulations. (a) An extracellular stimulation of a single neuron at 10 Hz. The relative time gap between a stimulation (red bar) and its recorded evoked spike (voltage minima), the neuronal response latency, is exemplified for several stimulations. The graph (right) summarizes the latency over 1600 stimulations. (b) A two-neuron chain where neuron A is stimulated at a rate of 10 Hz, and the initial effective delay between evoked spikes of neurons A and B is set to \( \tau_{AB} = 80 \text{ ms} \). Several recorded spikes from neurons A and B are exemplified. The graph (right) summarizes the ~2 ms increase in \( \tau_{AB} \) over ~270 stimulations. (c) Similar to (b) with a five-neuron chain, and a ~6 ms increase in \( \tau_{AE} \) which accumulates the stretching of all four (B–E) neuronal response latencies.

Elastic response latency —circuit level. – To analyze the impact of dynamic neuronal response latency at the circuit level, we artificially generated conditioned stimulations of a circuit of neurons embedded within a large-scale network of cortical cells in vitro (“Methods” section). Assuming a directed chain of two neurons, A and B, we define \( \tau_{AB} \) as the time gap between consecutive evoked spikes from neurons A and B. Initially this time gap is set to \( \tau_{AB} = 80 \text{ ms} \) (fig. 1(b)). Hence, the initial delay time between an evoked spike of neuron A and the corresponding stimulation to neuron B is set to \( 80 - L_B(0) \text{ ms} \), where \( L_B(0) \) stands for the initial latency of neuron B. After ~270 stimulations of neuron A at a rate of 10 Hz, the latency of neuron B increases by ~2 ms, thus resulting in an increase of the delay, \( \tau_{AB} \approx 82 \text{ ms} \). The stretching of the delay of a neuronal chain is accumulative (fig. 1(c)). For a chain consisting of five neurons, the increase in the effective delay, \( \tau_{AE} \), (between evoked spikes of neurons A and E) is the accumulation of the latency increases of neurons B, C, D, E. After ~270 stimulations of neuron A, a stretching of ~6 ms in \( \tau_{AE} \) was measured (fig. 1(c)). This unavoidable accumulated stretching is the key feature of the underlying experimentally corroborated paradigm presented below, which enables the brain to implement new types of dynamic logic-gates.

AND-gate. – The first experimentally examined dynamic logic-gate is an AND-gate consisting of 5 neurons and weak/strong stimulations represented by dashed/full lines. (a) Schematic of an AND-gate consisting of five neurons and weak/strong stimulations represented by dashed/full lines. (b) The delays are initially set to \( \tau_{BE} = 80 \text{ ms} \) and \( \tau_{AE} \sim \tau_{BE} - 1.6 \text{ ms} \). Applying simultaneous stimulations at ~10 Hz to the input neurons, the two delays become the same and later reverse roles where \( \tau_{AE} \sim \tau_{BE} + 1 \text{ ms} \), as presented by the blue dots as a function of stimulation number. Unified longer stimulations were given for events where \( |\tau_{AE} - \tau_{BE}| < 100 \mu s \) and are presented by zero-time-lag open blue dots. The probability of an evoked spike of neuron E over a sliding window of 10 stimulations is presented by the purple line.

Fig. 2: (Color online) Dynamic logic operating modes of an AND-gate. (a) Schematic of an AND-gate consisting of five neurons and weak/strong stimulations represented by dashed/full lines. (b) The delays are initially set to \( \tau_{BE} = 80 \text{ ms} \) and \( \tau_{AE} \sim \tau_{BE} - 1.6 \text{ ms} \). Applying simultaneous stimulations at ~10 Hz to the input neurons, the two delays become the same and later reverse roles where \( \tau_{AE} \sim \tau_{BE} + 1 \text{ ms} \), as presented by the blue dots as a function of stimulation number. Unified longer stimulations were given for events where \( |\tau_{AE} - \tau_{BE}| < 100 \mu s \) and are presented by zero-time-lag open blue dots. The probability of an evoked spike of neuron E over a sliding window of 10 stimulations is presented by the purple line.
BE (fig. 2(b)). For a time lag $|\tau_{AE} - \tau_{BE}|$ greater than $\sim 0.5$ ms the logic-gate operates as a NULL-gate indicating a lack of evoked spikes independent of the input stimulation, whereas in the intermediate region it operates typically as an AND-gate. Hence, this neuronal gate exhibits NULL $\rightarrow$ AND $\rightarrow$ NULL dynamic logic operation transitions (table 1, 1st row). The maximal time lag between two weak stimulations generating an evoked spike varies across different experiments and stimulation types and increases even beyond a millisecond. This phenomenon of the time-dependent operation of the AND-gate is robust to population dynamics, cell assembly (see the “Population dynamics” section).

**OR-gate.** – The experimental setup of the OR-gate is similar to the AND-gate (fig. 2(a)); however, all stimulations are now strong (fig. 3(a)). As a result of simultaneous stimulations given to the input neurons, the relative stretching of the two input chains, $|\tau_{AF} - \tau_{BF}|$, exceeds $\sim 5$ ms. The output neuron, F, generates two evoked spikes when the time lag between the two incoming stimulations is large enough (compared to the refractory period), typically greater than 4 ms (fig. 3(b)). This dynamic logic-gate exemplifies an entry from a region of typically two evoked spikes into an OR mode (a single output spike is produced in response to $in_1$ or $in_2$) and back to a mode of two evoked spikes (table 1, 2nd row).

**NOT-gate.** – The logic operation of the NOT-gate consists of a single input. Its implementation is similar to the previous ones (figs. 2(a) and 3(a)), but includes an inhibitory stimulation from neuron D to E (fig. 4(a)) and an outer stimulation, $in_2$, given independently of $in_1$.

This inhibition, conditioned to the stimulation given to neuron A, blocks the stimulation coming from neuron B for a limited time interval. The inhibitory mechanism cannot be achieved by shaping the stimulations amplitude or its sign. Using a different cocktail of synaptic blockers which mainly suppresses the excitatory synapses (“Methods” section) enables the use of inhibitory stimulations. For low stimulation rates, stretching of neuronal response latencies can be ignored and the logic operation of the gate was measured independently for each relative delay between excitation and inhibition, $\tau_{BE} - \tau_{AD}$ (fig. 4(b)). The inhibition is almost absolute for stimulations given 5 ms or less prior to an excitatory stimulation and its effectiveness deteriorates for larger time gaps, until it vanishes around 10 ms. For a high stimulation rate a time-dependent logic operation is demonstrated as a relatively fast transition from a reliable relay of an arriving spike to an absolute blocker, a NOT-gate (fig. 4(C2)) and vice versa. Hence, 1-NOT-1 logic operating modes are anticipated (table 1, 3rd row).

Table 1: (Color online) Experimentally examined logic-gates and their dynamic operations. The first column lists the logic-gates. The second column details the truth table, the input/output relations. The third column presents a schematic of the confirmed dynamic transitions among different logic operating modes, as a gate was repeatedly stimulated. The symbols $0/1$ stand for a non-evoked/evoked spike, NULL indicates a non-evoked output spike independent of the inputs and IF($in_i$) represents an output identical to the $i$-th input. The order of IF($in_1$) and IF($in_2$) in the second row indicates the timing of their effects on the output unit.

| Logic-gate | Truth table | Dynamic logic operation |
|------------|-------------|------------------------|
| AND        | 0 0 0       | NULL $\rightarrow$ AND $\rightarrow$ NULL |
| OR         | 0 0 0       | IF($in_1$) $+$ IF($in_2$) $\rightarrow$ OR $\rightarrow$ IF($in_1$) $+$ IF($in_2$) |
| NOT        | 0 1 1       | 1 $\rightarrow$ NOT $\rightarrow$ 1 |
| XOR        | 0 0 0       | OR $\rightarrow$ XOR $\rightarrow$ OR |

Fig. 3: (Color online) Dynamic logic operating modes of an OR-gate. (a) Schematic of an OR-gate consisting of a four-neuron input chain (green) and a one-neuron input chain (orange), where all stimulations are strong. (b) Independent experiments for fixed time lags $\tau_{BF} - \tau_{AF}$ (purple dots connected with a dashed guideline). The probability for neuron F to respond by two spikes was averaged over several tens of input stimulations. (c) Input stimulation at a rate of 10 Hz resulting in dynamic changes of $\tau_{BF} - \tau_{AF}$ from 8 to 3 ms (blue dots). A dynamic transition from the region of typically two output spikes to an OR operating mode (similar to the entry on (b)) occurs after $\sim 30$ input stimulations. Missed evoked spikes resulting in only one stimulation to neuron F are marked as blue dots on the x-axis. (d) Similarly to the entry in (b), $\tau_{AF} - \tau_{BF}$ increases from $\sim 2.5$ to $7$ ms (blue dots) and a dynamic exit from the OR region to the region of typically two evoked spikes occurs after $\sim 60$ input stimulations.
XOR-gate. — The implementation of the XOR-gate is similar to the OR-gate setup, but requires two inhibitory stimulations (red in fig. 4(d)). For low stimulation rates, the neuronal response latencies remain unaffected and the logical operation of the XOR-gate was measured independently for each relative delay between excitation and inhibition, $\tau_{BE} - \tau_{AC}$. Figure 4(e) exemplifies XOR→OR operating modes. Clearly, for negative $\tau_{BE} - \tau_{AC}$, the excitation arrives before the inhibition, and the gate operates as an OR-gate. Hence, as $\tau_{BE} - \tau_{AC}$ varies in time, OR→XOR→OR transitions are expected. We note that the synaptic delays can be shortened to several ms, a realistic cortical time scale, using long synfire chains. Moreover, the few hundred stimulation periods of operating logic modes can be significantly shortened. Long synfire chains increase the stretching linearly with the number of their relays and, in addition, the neuronal response latencies increase significantly faster (by one order of magnitude) in the initial spiking activity (fig. 1(a)).

Population dynamics. — The robustness of the dynamic logic-gates to population dynamics is exemplified for the AND-gate in fig. 5, where populations A, B and C are comprised of 40 Hodgkin-Huxley neurons (fig. 5(a)). Each neuron in population C receives a drive from 10% of population A’s neurons as well as from 10% of population B’s neurons, all randomly selected, resulting on the average in 8 stimulations to each neuron in population C. These diluted population-population stimulations represented by the dashed arrows, are weak stimulations; thus, to generate a spike in an output neuron, almost all stimulations from both populations at a sufficiently small time lag are required. The initial time delays from the stimulation of the neurons in the two input populations to the stimulation of the neurons in the output population are

Fig. 4: (Color online) Dynamic logic operating modes of a NOT-gate and a XOR-gate. (a) Schematic of NOT-gate consisting of five neurons, with one inhibition (red). A NOT-gate has one input (table 1, 3rd row), where $in_2$ stands for an outer stimulation which is always given, independently of $in_1$. (b) Independent experiments for a fixed time lag $\tau_{BE} - \tau_{AD}$ (purple dots connected with a dashed guideline) and $\tau_{BE} = 80$ ms. Neurons A and B are simultaneously stimulated at 1 Hz. (c) Input stimulations at a rate of 10 Hz resulting in dynamic changes in $\tau_{BE} - \tau_{AD}$ as shown by time segments $C_1$, $C_2$ and $C_3$ in (b) averaged over a sliding window of 20 stimulations. (d) Schematic of a XOR-gate containing two inhibitory stimulations (red). (e) Input neurons are simultaneously stimulated at 1 Hz. Independent experiments where $\tau_{BF} - \tau_{AC}$ is varied; a fixed time lag $\tau_{AE} - \tau_{BD} = 3$ ms was selected to inhibit the stimulation from neuron A, $\tau_{AE} \sim 100$ ms, $\tau_{BF} \sim 50$ ms and $\tau_{AC} - \tau_{BC} = 150$ ms were performed (dots connected with a dashed guideline). The conditional probabilities of an evoked spike of neuron G are presented by the three colored dashed lines.

Fig. 5: (Color online) Population dynamics implementation of an AND-gate. (a) Schematic of an AND-logic-gate in population dynamics. (b) For a simultaneous stimulation to all neurons in populations A and B, the firing probability of the output neurons is presented as a function of the time lag $\gamma$ between $\tau_{AC}$ and $\tau_{BC}$, as detected in a simulation. (c) A similar setup as in panel (a), containing a synfire chain from B to E. Each population is comprised of 40 neurons, each neuron receives a drive from 4 randomly chosen neurons of the preceding population. The neuronal latency increase is taken to be $\Delta = 0.04$ ms per spike. (d) The difference $|\tau_{AE} - \tau_{BE}|$ is presented as a function of the stimulation number, simultaneously given to all neurons in populations A and B, together with the firing probability of the output population.
τ_{AC} = \text{unif}[9.5, 10.5] \text{ ms}, \text{ and } τ_{BC} = \text{unif}[9.5, 10.5] + \gamma \text{ ms} \ (\text{unif stands for uniform distribution}). \ The \ population \ gate \ was \ simulated \ using \ Hodgkin-Huxley \ neurons \ with \ parameters \ similar \ to [16] \ and \ q_{max} = 0.0648 \text{ ms/cm}^2. \ For \ a \ simultaneous \ stimulation \ to \ all \ neurons \ in \ populations \ A \ and \ B, \ the \ firing \ probability \ is \ defined \ as \ the \ fraction \ of \ firing \ neurons \ in \ the \ output \ population. \ This \ probability \ is \ presented \ as \ a \ function \ of \ the \ time \ lag \ \gamma \ \text{between} \ τ_{AC} \ \text{and} \ τ_{BC}, \ as \ detected \ in \ a \ simulation \ where \ each \ \gamma \ \text{was averaged over 50 different initial conditions. In the range} \ \text{where} \ \gamma \ \text{is less than 1 ms, an increased firing probability of population C is detected and the functionality of an AND-logic-gate is maintained. In fig. 5(c) we demonstrate a similar setup as in fig. 5(a), containing a synfire chain from B to E. Each population is comprised of 40 neurons, each receiving a drive from 4 randomly chosen neurons of the preceding population. A neuron in population E receives 8 weak stimulations (from A and D), represented by the dashed arrows similar to those in fig. 5(a). The initial time delays (including the initial neuronal latencies) between the stimulation of the neurons in the two input populations to the stimulation of the neurons in the output population are τ_{AE} = \text{unif}[31.5, 32.5] \text{ ms}, \text{ and } τ_{BE} = \text{unif}[29.5, 30.5] \text{ ms}. \ The \ neuronal \ latency \ increase \ is \ taken \ to \ be \ Δ = 0.04 \text{ ms per spike (to reduce computation complexity). The difference} |τ_{AE} − τ_{BE}| \ \text{is presented as a function of the stimulation number, simultaneously given to all neurons in populations A and B, together with the firing probability of the output population. Initially, the difference} |τ_{AE} − τ_{BE}| \ \text{is \sim 2 ms, therefore no output spikes are expected. As the neuronal delays increase,} |τ_{AE} − τ_{BE}| \ \text{shrinks to zero and grows again, resulting in dynamic transitions, NULL→AND→NULL.} \ 

Discussion. – It is evident that the variety of possible dynamic logic-gates is much larger than the above-mentioned examples. Specifically, one can go beyond simultaneous stimulations to the input neurons or a single frequency to each input neuron as well as a scenario with several input chains to the output neuron. This computational horizon was examined (not shown) using a simplified theoretical framework based on the following assumptions: The increase in the neuronal response latency per spike is a constant, identical for each neuron comprising the gate and is independent of its current latency. In addition, strong excitatory stimulation always generates an evoked spike. Using these assumptions, complex gates with multiple transitions between basic types of logic operations can be achieved. In addition, the confirmation of the dynamic logic operating transitions for the XOR-gate requires much longer neuronal chains and was examined using this analytical approach.

For recurrent networks, the complexity is expected to be enhanced as the timings of the input stimulations are a function of the activity of the entire network. One of the open theoretical questions is the number of different possible logic operations for N interconnected gates, where each one has, for instance, two operating modes. The upper bound for different operating logic-states of the network is 2^N, but it is unclear how many of them are realizable.

On mathematical grounds, the time-dependent logic-gates raise the following key questions. Does this type of recurrent network dynamics lead to a new kind of computation paradigm which might go beyond the universal Turing machine [5,17] and if not what are its advantages with respect to the implementation of the brains functionalities?

Methods. – Cortical neurons were obtained from newborn rats (Sprague-Dawley) within 48 h after birth using mechanical and enzymatic procedures (see refs. [7,8]). Rats were euthanized according to protocols approved by the National Institutes of Health. The cortex tissue was digested enzymatically with 0.05% trypsin solution in phosphate-buffered saline (PBS) (Dulbecco’s PBS) free of calcium and magnesium, supplemented with 20 mM glucose, at 37 °C. Enzyme treatment was terminated with heat-inactivated horse serum (Biological Industries, Beit-Haemek, Israel), and cells were then mechanically dissociated. The neurons were plated directly onto substrate-integrated multi-electrode arrays and allowed to develop functionally and structurally mature networks over a time period of 2–3 weeks in vitro, prior to the experiments. Variability in the number of cultured days in this range had no effect on the observed results. The number of plated neurons in a typical network is of the order of 130000, covering an area of about 380 mm².

The preparations were bathed in MEM supplemented with heat-inactivated horse serum (5%), glutamine (0.5 mM), glucose (20 mM), and gentamicin (10 g/ml), and maintained in an atmosphere of 37 °C, 5% CO₂, and 95% air in an incubator as well as during the electrophysiological measurements. All experiments were conducted on cultured cortical neurons that were functionally isolated from their network by a pharmacological block of glutamatergic and GABAergic synapses. Experiments were conducted in the standard growth medium, supplemented with 10 μM CNQX (6-cyano-7-nitroquinoxaline-2,3-dione) and 80 μM APV (amino-5-phosphonovaleric acid). 5 μM Bicuculline was added only in experiments where no inhibitory stimulations were used (figs. 1, 2, 3). This cocktail of synaptic blockers made the spontaneous network activity sparse. At least one hour was allowed for stabilization of the effect.

An array of 60 Ti/Au/TiN extracellular electrodes, 30 μm in diameter, and spaced either 200 or 500 μm from each other (Multi-ChannelSystems, Reutlingen, Germany) were used. The insulation layer (silicon nitride) was pre-treated with polyethyleneimine (Sigma, 0.01% in 0.1 M borate buffer solution). A commercial setup (MEA2100-2 × 60-headstage, MEA2100-interface board, MCS, Reutlingen, Germany) for recording and analyzing data from two 60-electrode MEAs (microelectrode arrays) was used, with integrated data acquisition from 120 MEA...
electrodes and 8 additional analog channels, integrated filter amplifier and 3-channel current or voltage stimulus generator (for each array of 60 electrodes). Mono-phasic square voltage pulses (100–500 µs, −100–900 mV) were applied through extracellular electrodes. Each channel was sampled at a frequency of 50k sample/s. Action potentials were detected on-line by threshold crossing. For each of the recording channels a threshold for a spike detection was defined separately, prior to the beginning of the experiment.

Each logic-gates node was represented by a stimulation source (source electrode) and a recording electrode (target electrode). The pair of electrodes (source and target) were selected as the ones that evoked well-isolated and well-formed spikes and reliable response with high signal-to-noise ratio. This examination was done with stimulations of electrode \(k\) given to each one of the 60 extracellular electrodes. The initial step to identify a pair of electrodes for an inhibitory stimulation was to pinpoint an excitatory node by its source and target electrodes (a stimulation of the source electrode, \(i\), results in a detection of a well-isolated spike in the target electrode, \(j\)). In the next step a stimulation was given to each one of the 60 extracellular electrodes (electrode \(k\)) a few ms prior to the stimulation of the source electrode, \(i\), while the activity of the target electrode, \(j\), was recorded. This procedure was repeated 5 times for each of the 60 electrodes. This examination was performed under different time lags between stimulations of an electrode \(k\) \((k = 1, 60)\) and the stimulation of the source electrode, \(i\). In the case of an inhibitory stimulation (neuron \(k\) inhibits neuron \(j\)), a stimulation given to electrode \(k\) several ms prior to the stimulation of the source electrode, \(i\), results in no neuronal response in the target electrode, \(j\). When the time lag between the stimulations of electrode \(k\) and the source electrode \(i\) is relatively long \((e.g., 15\, ms)\), the inhibitory effect gradually disappears, and a spike will be detected in the target electrode, \(j\).

We thank Moshe Abeles and Eytan Domany for fruitful discussions and comments on the manuscript, as well as the computational assistance by Mathias Mahn, Igor Reidler, Yair Sahar, Alexander Kalmanovitch and Haya Brama. The authors thank Hana Arnon for invaluable technical assistance. This research was supported by the Ministry of Science and Technology, Israel.

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