Computer Redundancy Management Technology Based on Non-Similar Platform

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Abstract. In order to study an efficient and reliable platform management computer, a non-similar platform management computer technology is designed. According to the structural characteristics of the computer management platform, a redundancy management strategy is developed. The redundancy management strategy of processor is studied. Then the priority order and voting strategy of four processors are determined, and several typical failure modes in practical work are discussed in detail. In order to verify the correctness of the synchronization strategy and redundancy management strategy, the principle prototype was tested, including the test of synchronization accuracy, typical debugging results and double redundant bus switching effect. The results show that the system runs stably and the four processor has good synchronization. It can achieve two fault works and three fault safeties, and it can realize bus switching.

1. Introduction

The security and reliability of computer systems are one of the key factors for computer applications in all fields, especially in aerospace systems. Embedded computer is the core component of the whole system, and its reliable operation is the security guarantee of the whole system. Minor faults can lead to disastrous consequences. Therefore, the research of high reliability embedded computer has been paid more and more attention. In order to improve the reliability of embedded computer, the traditional method is to choose components with high reliability. By improving the process structure and controlling the aging and screening of the components, the reliability of the components can be improved directly. Moreover, the current reliability index of the components cannot meet the high reliability requirements of aerospace systems (Wienhold, 2016). Obviously, this method cannot reduce the failure rate of the system very well. Therefore, another important way to improve reliability is to develop redundancy technology (Pandiaraj, 2015).

Compared with the conventional triple-modular redundant computer, the non-similar dual redundant platform management computer eliminates the common-mode fault, and its reliability is further enhanced. Compared with the traditional dual redundant structure, its resource utilization is improved, but the management difficulty will be increased accordingly. The redundancy management and related technologies of platform management computer are deeply studied.
2. Computer overall design

2.1. Dual redundant structure with conventional self-monitoring

The redundant technique is an important means to improve the safety and reliability of the computer system. Through redundant technology, components with lower reliability are combined into a highly reliable system to reduce the system failure rate. In the redundant technique of fault-tolerant computer, the fault-tolerant computer can be divided into the similar redundancy computer and the non-similar redundancy computer according to the structure characteristic of the system (Gomes, 2016). The similar redundancy structure adopts a simple method of resource duplication, and its hardware and software are exactly the same. The structure of hardware and software of non-similar redundancy structure is different (Buckley, 2016).

The characteristics of dual redundant structures with conventional self-monitoring can be summarized as follows: First, the composition of hardware and software of the two channels is exactly the same, and they are all in constant power supply and hot standby state. One is the main channel, which is responsible for providing the various functions of the platform management computer, and implementing external control. The other is a backup channel that runs the same software as the main channel, but it does not perform external controls. Second, each channel has two processors (Tian, 2015). The two processors within the channel interact with each other via the cross-channel data link (CCDL). There is usually no interaction between the two channels of processors (Stewart, 2015).

2.2. System composition of a platform management computer

Improvement of conventional triple-modular redundant computer: the triple-modular redundant computer consists of three computer modules with the same type but it is independent of each other. The three modules receive three identical inputs, respectively, then processing the data and sending their processing results to the voting device. After voting, the correct result is output by the voter. The conventional trumpet redundant computer has the following disadvantages: When a failure occurs, the conventional trumpet redundant computer can continue to work. But it will enter a safe state in next time. Meanwhile, the common redundancy structure is adopted, which results in the common mode failure risk of the processor. In this topic, the platform management computer adopts the design method of non-similar redundancy to improve the reliability of the platform management computer.

Improvement of dual redundancy computer with conventional self-monitoring: In this structure, when one channel fails, the control is switched from one channel to another (Norman, 2015). Therefore, it is possible to have another processor in the channel., and the processor resource utilization is not high. Through the analysis of the dual-redundancy structure with conventional self-monitoring, it is found that the two processors within the same channel can interact with each other. There is no information interaction between processors in different channels (Dao, 2016).

3. Design of redundant management technology

The platform computer management system of non-similar dual redundancy is composed of two parts: hardware and software. The execution speed of hardware system is fast, but the relative difficulty is great and the cost is expensive. Meanwhile, the FPGA design of the dual redundancy bus is introduced, and the cross control of the function module by the processor system is realized.

3.1. FPGA platform design

In the four processor systems, the interface of the FPGA module is exactly the same as the specific program design. The FPGA modules in each system are equipped with three channels of synchronous serial port receiving and three serial synchronous serial port sending interface. The information interaction channels of each processor system are independent of each other, and are implemented through backplane routing. Thus, the location relationship between the different processor systems is determined. Each identifier is determined by its position in the slot, which is independent of the
processor itself. Each processor system FPGA module has the I2C bus interface, and the physical connection with the I/O module is also realized through the backplane wiring.

Each processor system is equipped with synchronous serial protocol control module, synchronization module and I2C protocol control module. The function module FPGA is equipped with I2C protocol control module and DART serial transceiver module. Through synchronous serial ports, four processors can exchange information between them. The processor is selected according to the voting strategy, and the processor on duty controls the I2C bus. The shift processor outputs the result to the function module and outputs the result through the DART asynchronous serial port.

Both the CPU board and the I/O board FPGA use separate clocks. Four CPU board clocks and I/O board are provided by 20MHz crystal oscillator. FPGA selects the A3P1000-PQG208 chip produced by Actel company, and the integrated environment for development is Libero IDE 8.5. VHDL programming language is used to design FPGA.

3.2. Platform software design
Hardware synchronization cannot meet the design requirements of the system. The design of non-similar platform management computer system consists of two parts: software and hardware. The system realizes task level synchronization, fault diagnosis and downgrade. In software design, the method of executing single task by cycle is adopted. The software design flow will be described below.

The first step is to turn on the machine at the same time. Then a millisecond counter is used to determine the time base for the four processors to start working. The timer of the periodic task begins to produce a synchronous signal that interrupts the existing task of the processor. At the entry of each task program, the four processor systems begin to perform tasks at the same time as they wait for the task to start.

Second, after the completion of the task, three working modes need to be judged, respectively four machine mode, three machine mode and two machine mode. In each mode, each normally operating processor sends data to the rest of the normal processor. The rest of the normal processor's data is received and saved. Once the data exchange is completed, the system can determine whether all the processors are synchronized. If all of them are synchronized, the output results are compared, and a processor for data processing errors is voted out. After this information interaction, each processor has a judgment of the state of the other processors and determines the correct output.

Third, after the synchronous operation of four, each processor sends its own state voting results to the rest of the processor, and receive the results of the rest of the normal processor. Based on the principle of subordination of the minority to the majority, the fault processor and the processor on the shift are selected. The correct results are output to the I/O module by the processor on duty by I2C.

4. Test results and analysis
The program is downloaded through four CPU boards and I/O board FPGA, while synchronization control, synchronous serial port transceiver and internal bus control functions are completed. Software synchronization, data exchange, state voting and downgrade as well as the control programs for I/O can be run in the VxWorks operating system. Each module has been working properly after debugging. In the test, the operating frequency of the two BM3 803 processors is set at 64MHz, and the operating frequency of the two PC8245 processors is set at 247.5MHz. At this frequency, the module runs stably, the frequency of the input clock on the four CPU board FPGA is 50MHz and the frequency of input clock on the I/O board FPGA is 20MHz. The four processor systems perform the same task and the task cycle is set to 400ms. An oscilloscope WS3034 is used to capture the operating status of other signals, such as synchronization. The prototype of the platform management computer is shown in figure 1.
4.1. Mode migration implementation

In practical work, there may be many kinds of faults. Eventually, however, there are differences between four processor paths or data interactions. Several typical cases of the state and main behaviors of the processor system consisting of four processors are simulated. The structure of the fault can be injected into the wrong method by software, that is, change the value of the variable in the shell command window in the Tornado environment. It can also be implemented by means of a communication link that carries out information interaction with the four processor system.

In testing, according to the position of the four CPU boards in the slot, the A, B, C, and D processor bits are represented in binary terms, followed by 00, 01, 10, and 11. Taking processor A as an example, the processor A communicates with D through synchronous serial port 0, and it communicates with B through synchronous serial port 1, and it communicates with C through synchronous serial port 2. The position relation has been determined.

Table 1. CCDL communication link relationships between four processor systems

| Processor system | synchronous serial port 0 | synchronous serial port 1 | synchronous serial port 2 |
|------------------|----------------------------|---------------------------|---------------------------|
| A                | D                          | B                         | C                         |
| B                | D                          | A                         | C                         |
| C                | D                          | A                         | B                         |
| D                | C                          | A                         | B                         |

4.2. Migration analysis of different modes

The four machine mode: In this mode, each processor will receive data sent by the other three processors via a synchronous serial port when there is no fault. At this point, the machine on duty outputs the result. The information interaction in the normal four machine mode is shown in table 2.

Table 2. Information interaction of normal four mode

| Processor system | synchronous serial port 0 | synchronous serial port 1 | synchronous serial port 2 | output result |
|------------------|----------------------------|---------------------------|---------------------------|---------------|
| A                | 2D                         | 2D                        | 2D                        | 2D            |
| B                | 2D                         | 2D                        | --                        | --            |
| C                | 2D                         | 2D                        | --                        | --            |
| D                | 2D                         | --                        | --                        | --            |

The three machine mode: Table 3 shows the information interaction between the four processor systems. Enabling the processor A to perform task timeouts can enable interactive processes. At this point, the processor A cannot be synchronized with the other three processors. Processor B, C, and D cannot receive data from A. The A is no longer sending data to the A by exchanging views with the processor. As a result, A can no longer receive data, which has been isolated from the system. The results is output by machine B on duty.

Table 3. Unsynchronized information interaction

| Processor system | synchronous serial port 0 | synchronous serial port 1 | synchronous serial port 2 | error CPU | output result |
|------------------|----------------------------|---------------------------|---------------------------|-----------|---------------|
| A                | --                        | --                        | --                        | --        | --            |
5. Conclusions

Through the improvement of the conventional self-monitoring and the triple-modular redundant computer, the non-similar platform management computer and the corresponding synchronization and redundant management strategies are developed. Through the software and hardware combination method, the strategy is implemented and verified. The shortcomings of the two types of computers are analyzed. In order to eliminate the effects of common mode failures and improve resource utilization, a non-similar and dual redundancy platform management computer structure was proposed. The CCDL is implemented between four processor systems using FPGAs, enabling the four processors to exchange synchronization status information in real time. Several typical mode migration cases are simulated and analyzed by software simulation fault and hardware simulation fault method. The test results of all kinds of cases coincide with the theoretical analysis. The system can achieve two normal operations and three fault safeties. To sum up, the synchronization of the system is realized. The degree of asynchronism is controlled in hundreds of microseconds to meet mission requirements. The study of computer synchronization techniques for non-similar redundancy is not as good as that of triple-modular redundant computers. The system synchronization accuracy needs to be further improved.

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