PERFORMANCE IMPROVEMENT OF A MODIFIED CARRY SELECT ADDER

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Abstract – This paper contains various performance improvement techniques of a modified architecture of carry select adder. The conventional Carry Select Adder is first designed and then modification is done to improve performance parameters such as delay reduction, power dissipation, power Delay Product. We simulated these designs along with a modified design in cadence VIRTUOSO environment in 180nm CMOS technology and compared their performance parameters are compared.

Keywords – CMOS Logic, Carry Select Adder, GDI Approach, High Performance

I. INTRODUCTION

Adder is one of the most useful building blocks of any processor. Any High speed application needs to be operated faster than any other application. In order to make our calculation faster we definitely need an addition technique which takes very less time to execute. So a faster adder is always preferred in high performance application [1].

But along with this increasing need of portable devices such as cellular mobile phones, different processors, the need for low power dissipating VLSI circuits also have become necessarily increased. As we all know reduction in delay will give rise to power dissipation. As a VLSI Designer one should take care of power dissipation also[2]. So basically a low power fast algorithm is needed in order to make a design efficient. There are several fast addition techniques discovered in last decades. Carry Select adder is one of the fastest addition techniques. We first design a conventional Carry Select Adder and then further modification done by replacing ripple carry adder block by Kogge Stone adder. Use of Kogge Stone adder gave a significant improvement in performance parameters. We then use Multiple Threshold techniques over it to reduce the static power dissipation[3]. Then we modified the architecture for kogge stone based Carry Select adder by the use of GDI technique. Using of GDI Approach subsequently reduces the power dissipation as the transistor count become less than conventional CMOS logic and gives us a moderate speed of operation.

II. CARRY SELECT ADDER

Carry Select Adder is one of the fastest algorithms for addition of two numbers. In this method first we do the lower nibble operation using the input bits and carry in signal. Then the upper bit calculation is done assuming two different carry in signal i.e. either 0 or 1. We use a Multiplexer in order to get exact sum bits. The operation of Carry Select Adder can be well understood from the diagram below[4].

Figure 1. Conventional Carry Select Adder

Figure 2. 8 bit Conventional Carry Select Adder

Performance Improvement Of A Modified Carry Select Adder
The internal sum is calculated using 2 bit Ripple carry Adder and Each Ripple Carry adder consists of two 28T full adder.

III. KOGGE STONE BASED CARRY SELECT ADDER

This is a modified Carry Select Architecture which has significantly improved performance parameters. In this adder the Ripple Carry Adder Block is replaced by 2bit Kogge Stone Adder[5-6]. Due to use of Parallel Prefix adder the delay of overall modified Carry Select Adder become very less Compared to the conventional one[10].

IV. MTCMOS TECHNIQUE

Reduction of Power dissipation is one of the greatest challenges in modern VLSI Design. Among several low power techniques, Multiple Threshold CMOS Technique is one of the major Low Power methodologies in terms of reduction of static power dissipation[7]. MTCMOS technique is a variation of CMOS chip technology which has transistors with multiple Threshold voltage in order to optimize power.

V. GDI APPROACH

GDI technique or gate Diffusion input technique is suitable for designing fast and low power circuits using reduced number of transistor count compared to traditional CMOS and pass Transistor logic. Instead of using two bulk NMOS and PMOS, in GDI technique we use three different inputs. The basic diagram of GDI technique is shown below[8-9].

VI. MODIFIED TECHNIQUE

The Kogge Stone based Carry Select Adder is then further modified by use of GDI technique. In this process we first design 2 bit kogge stone adder using GDI approach and after that we use this modified kogge stone adder in place of Ripple Carry Adder Block inside the Carry Select Adder. Due to lesser transistor count of GDI technique, the 2 bit kogge stone adder will dissipate lesser power than the previous and hence the overall power dissipation of modified carry select adder become less.

VII. RESULTS & DISCUSSIONS

All the above described adder architectures are designed for 8bit operation in cadence VIRTUOSO environment in 180 nm CMOS technology and their performance parameters are shown below.

Table 1. Performance parameter of four adder
From the above table we can see that all the modified architecture has improved performance parameters than conventional Carry Select Adder. In 8bit operation, delay reduced in kogge stone based Carry Select adder is 0.036ns compared to 0.22ns in basic Carry Select adder i.e. 83.63% increment in speed and power dissipation also reduced to 84.75% than the conventional one.

When we go for further power dissipation in that modified architecture by use of MTCMOS technique the delay increased to 0.778ns but power reduces drastically from 916.8 μw to 253.2 μw i.e. 72.38% reduction in power dissipation.

Now after using GDI technique inside the Kogge Stone architecture will again decrease the delay and power both. The delay will be reduced by 79.54% and power dissipation is significantly reduced by 96.61% which in turns produce a better power delay product of $13.2 \times 10^{-15}$ joule than the others.

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**Table 2. Different modification technique with total transistor count**

| DESIGN                                      | Transistor Count |
|---------------------------------------------|------------------|
| Carry Select adder (8 bit)                  | 446              |
| Kogge-Stone based Carry Select Adder (8 bit) | 698              |
| with MTCMOS technique                      | 702              |
| With GDI Approach (8 bit)                  | 256              |

**VIII. CONCLUSION**

High speed application is always desired in modern VLSI design. On the other hand lower power dissipation is also a primary goal of any circuit design. Based on the Experimental data shown in table 1 we can say that among all the modified architecture described in above section, kogge stone based carry select adder gives a significant reduction on power dissipation and also gives a decent speed of operation than both the conventional Carry select adder and kogge stone based Carry Select adder. This kogge stone based carry select adder with GDI approach can be used in high speed as well as in low power applications.

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