Exceedingly High Performance Top-Gate P-Type SnO Thin Film Transistor with a Nanometer Scale Channel Layer

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Abstract: Implementing high-performance n- and p-type thin-film transistors (TFTs) for monolithic three-dimensional (3D) integrated circuit (IC) and low-DC-power display is crucial. To achieve these goals, a top-gate transistor is preferred to a conventional bottom-gate structure. However, achieving high-performance top-gate p-TFT with good field-effect mobility (μFE) and large on-current/off-current (ION/IOFF) is challenging. In this report, coplanar top-gate nanosheet SnO p-TFT with high μFE of 4.4 cm²/Vs, large ION/IOFF of 1.2 × 10⁵, and sharp transistor’s turn-on subthreshold slopes (SS) of 526 mV/decade were achieved simultaneously. Secondary ion mass spectrometry analysis revealed that the excellent device integrity was strongly related to process temperature, because the HfO₂/SnO interface and related μFE were degraded by Sn and Hf inter-diffusion at an elevated temperature due to weak Sn–O bond enthalpy. Oxygen content during process is also crucial because the hole-conductive p-type SnO channel is oxidized into oxygen-rich n-type SnO to demote the device performance. The hole μFE, ION/IOFF, and SS values obtained in this study are the best-reported data to date for top-gate p-TFT device, thus facilitating the development of monolithic 3D ICs on the backend dielectric of IC chips.

Keywords: monolithic 3D; 3D brain-mimicking IC; SnO TFT

1. Introduction

Metal-oxide Thin film transistors (TFTs) [1–35] have drawn considerable attention due to their high mobility, low fabrication temperature, and simple fabrication process, making them suitable for advanced display [1–6] and monolithic three-dimensional (3D) integrated circuit (IC) [15–21] on amorphous inter-metal-dielectric (IMD) of a Si chip. To reach low DC power consumption, both high performance n- and p-type TFTs are necessary to form the complementary metal-oxide-semiconductor (CMOS) logic. Although high-performance n-TFTs with high field-effect mobility (μFE), sharp subthreshold swing (SS), and large on-current/off-current (ION/IOFF) values [12–15] have been reported, achieving reasonable performance p-TFTs is much more challenging [16,17,36,37]. Moreover, a top-gate structure is more suitable than a conventional bottom-gate device for high integration density and easy fabrication [24–26]. Previously, we have reported the bottom-gate SnO p-TFT, which has higher μFE than Cu₂O p-TFT [16,17]. In the current study, we further used the SnO channel to fabricate top-gate coplanar nanosheet p-TFT. Because the gate insulator was deposited after the SnO layer, the deposition and post-annealing conditions are crucial to device performance. This is because the p-type SnO is highly sensitive to oxygen partial pressure (Opp) and annealing temperature, and can be easily oxidized into oxygen-rich Sn₂O₃, Sn₃O₄, or SnO₂ [27–29]. Moreover, the weak Sn–O bond enthalpy [38] facilitates Sn diffusion into high-dielectric-constant (high-k) HfO₂ insulator at elevated temperature,
thus degrading device performance. In this study, the above challenges were successfully overcome, and high-performance top-gate nanosheet SnO p-TFT was achieved with high \( \mu_{FE} \) of 4.4 cm\(^2\)/Vs, large \( I_{ON}/I_{OFF} \) of \( 1.2 \times 10^5 \), and sharp \( SS \) of 526 mV/decade, indicating a high potential for future monolithic 3D and brain-mimicking IC applications [15,17–21].

2. Materials and Methods

The coplanar top-gate nanosheet SnO p-TFTs were fabricated on the Si wafer with a 500-nm-thick SiO\(_2\) IMD layer on Si wafer. The 7-nm-thick nanosheet SnO layer was deposited through reactive sputtering with 50 W DC power from a Sn target under \( O_2 \) power of 14.2%, 25%, and 33.3% ambient, respectively. All the SnO p-TFT samples were annealed under 200 \(^\circ\)C in N\(_2\) ambient for 45 min. Next, 40-nm high work-function Ni was deposited using an e-gun evaporator for the Schottky-barrier source and drain electrodes [39,40]. Subsequently, 50-nm HfO\(_2\) gate dielectric was deposited by e-beam evaporation with a rate of 0.2 Å/sec. HfO\(_2\) post-annealing was performed in N\(_2\) ambient at 100 \(^\circ\)C and 200 \(^\circ\)C. Finally, 50-nm gate electrode Al was deposited and patterned. The transistor’s length and width were 50 and 400 \( \mu\)m, respectively. The current-voltage characteristics of top-gate SnO p-TFT were measured through the HP4155B parameter analyzer and a probe station. The field-effect mobility values (\( \mu_{FE} \)), subthreshold slope (\( SS \)) and on-current/off-current (\( I_{ON}/I_{OFF} \)) values were extracted at a standard and small \( V_{DS} = -0.1 \) V. The cross-sectional image of device structure was obtained from FEI Talos F200X high-resolution transmission electron microscope (TEM). The surface roughness of HfO\(_2\) films were obtained via Atomic Force Microscope (AFM) using DIMENSION 3100. The X-ray photoelectron spectroscopy (XPS) analyses of HfO\(_2\) films and SnO films were executed by Thermo Nexsa. The secondary ion mass spectrometry (SIMS) depth profiles of Sn, Hf and O atoms were obtained by CAMECA IMS-6fE7.

3. Results

Figure 1a illustrates the top-view photograph of top-gate nanosheet SnO p-TFT, where the light-reflective Al metal-gate is on the top of the device. Figure 1b depicts the cross-sectional transmission electron microscope (TEM) image of the device structure with top Al-metal-gate, HfO\(_2\) gate-dielectric, and p-type channel SnO on SiO\(_2\) IMD. The thickness of Al, HfO\(_2\), and nanosheet SnO is 50, 50, and 7 nm, respectively.

![Figure 1. (a) top-view photograph and (b) cross-sectional TEM image of the top-gate nanosheet SnO p-TFT device. The “white”-color gate on top of the device is due to the light-reflective Al metal.](image-url)
The $O_{pp}$ is critical for top-gate nanosheet SnO p-TFT, where the SnO channel was made by sputtering from a metal Sn target under different $O_{pp}$ conditions. This is because the SnO can be oxidized into oxygen-rich SnO$_2$ [16]. The $O_{pp}$ can be expressed as follows:

$$O_{pp} = \frac{P_{O_2}}{P_{O_2 + P_{Ar}}} \times 100\%,$$

where $P_{O_2}$ and $P_{Ar}$ are the pressures of $O_2$ and $Ar$ in a sputtering system, respectively. For comparison, the $O_{pp}$ values were adjusted to 14.2%, 25% and 33.3% during sputtering. Figure 2a,b show the drain-source current versus gate-source voltage ($|I_{DS}| - V_{GS}$) and $\mu_{FE}$-$V_{GS}$ characteristics of top-gate nanosheet SnO p-TFT devices, respectively, under different $O_{pp}$ values. The top-gate p-type SnO device exhibits the highest $I_{ON}$ and the lowest leakage $I_{OFF}$ at the 25% $O_{pp}$ condition. The device with the best $I_{ON}$ and $I_{OFF}$ is also consistent with the highest $\mu_{FE}$. The $\mu_{FE}$ values were 1.5, 4.4 and 2.6 cm$^2$/Vs at $O_{pp}$ of 14.2%, 25% and 33.3%, respectively. Here the $\mu_{FE}$ values were obtained at the standard and a small $V_{DS}$ of $-0.1$ V. Such abnormal $\mu_{FE}$ on $O_{pp}$ is ascribed to the following reasons. The device $\mu_{FE}$ increases with the increase in $O_{pp}$ from 14.2% to 25% due to the increased oxygen content in SnO$_x$ with $x \leq 1$, and device performance degrades at a high $O_{pp}$ of 33.3% owing to the formation of oxygen-rich SnO$_x$ with $x > 1$. Under high $O_{pp}$, SnO$_x$ becomes n-type electron-conductive SnO$_2$ [12-14], which lowers the hole $\mu_{FE}$ under negative $V_{GS}$.

![Figure 2](image-url)

**Figure 2.** (a) $|I_{DS}| - V_{GS}$ and (b) $\mu_{FE}$-$V_{GS}$ characteristics of top-gate nanosheet SnO p-TFTs with SnO channel deposited at different $O_{pp}$ conditions. The SnO layer was annealed at 200 °C and HfO$_2$ layer was annealed at 100 °C.

The device integrity in top-gate nanosheet SnO p-TFT is also dependent on HfO$_2$ annealing temperature. To avoid plasma damage to the SnO channel layer, the high-$\kappa$ HfO$_2$ gate dielectric was deposited using an e-beam evaporator and subjected to post-annealing at 100 and 200 °C for 30 min under N$_2$ ambient. Here the SnO layers were deposited under 25% $O_{pp}$ and annealed at 200 °C under N$_2$ ambient. Subsequently, the HfO$_2$ were deposited and annealed at 100 °C or 200 °C under the N$_2$ ambient. The $|I_{DS}| - V_{GS}$ and $\mu_{FE}$-$V_{GS}$ characteristics of SnO p-TFTs with 100 and 200 °C post-annealing are shown in Figure 3a, b, respectively. The $I_{ON}/I_{OFF}$ and $\mu_{FE}$ values of the SnO p-TFT at 100 °C post-annealing are $1.2 \times 10^5$ and $4.4$ cm$^2$/Vs, respectively, which are much better than those obtained at 200 °C: $4.6 \times 10^5$ and 1.44 cm$^2$/Vs, respectively. The $I_{ON}/I_{OFF}$ is even better than previous bottom-gate SnO p-TFT [16] possibly due to the thinner SnO channel used in this study, which slightly degrades the $\mu_{FE}$. A thin channel layer is needed to fully deplete the conductive oxide semiconductor SnO, similar to the low $I_{OFF}$ using ultra-thin body Si-on-Insulator (SOI) and Fin field-effect transistor (FinFET). However, the small sub-10
nm-scale channel thickness can increase the interface roughness scattering and decrease the mobility.

To investigate the mechanism of such annealing temperature dependence, Figure 4a,b plot the $I_{DS}$ versus drain-source voltage ($I_{DS}$-$V_{DS}$) and the gate-source current versus gate-source voltage ($I_{GS}$-$V_{GS}$) characteristics of top-gate SnO p-TFTs, respectively, at annealing temperatures of 100 and 200 °C. The p-TFT device at 100 °C annealing shows higher $|I_{DS}|$ than that at 200 °C annealing, corresponding to the higher $\mu_{FE}$ (Figure 3b). In normal case, a high post-annealing temperature of high-κ gate dielectric is necessary to reduce the gate leakage current and improve the device performance. However, the measured $|I_{GS}|$ of HfO$_2$/SnO p-TFT annealed at 200 °C shows one order of magnitude higher gate leakage than that in the device annealed at 100 °C. The as-deposited HfO$_2$ layer without annealing has too high gate leakage current due to defect conduction [41] and unsuitable for device application. To decrease the defect-conductive leakage current, even higher annealing temperature is required for metal-gate/high-κ/Si CMOS [39,42,43].

To further inspect the unusual annealing temperature dependence on device performance, material analysis of atomic force microscope (AFM), X-ray photoelectron spectroscopy (XPS), and secondary ion mass spectrometry (SIMS) were performed. In Figure S1, the surface roughness of the 50 nm HfO$_2$ films annealed at 100 °C, 200 °C and 400 °C were analyzed through AFM. The root mean square values of surface roughness show slightly decrease along with the increasement of the annealing temperature. The HfO$_2$ dielectric
with different annealing temperatures were also analyzed by XPS. As shown in Figure S2, the binding energies of Hf-O and non-lattice O were 530 eV and 531.3 eV, respectively. The peak intensity of non-lattice O was related to the defects in HfO2 dielectric, which decreased with increasing post-annealing temperature. From the AFM and XPS analysis, the good device performance at 100 °C annealing is not related to the tiny difference of HfO2 layer.

To further investigate the $O_{pp}$ effect on chemical composition of the SnO layer, the XPS analyses on channel SnO were performed at the $O_{pp}$ of 14.2%, 25% and 33.3%. The HfO2 layer of HfO2/SnO stack was etched before the XPS analysis. The XPS data are depicted in Figure 5. The XPS spectra can be deconvolved into three curves from the Sn$^{2+}$O, Sn$^{4+}$O2 and Sn$^{0}$ signals, with their corresponding energies of 486.8, 486 and 484.4 eV, respectively. The composition x values of SnO$_x$ deposited at $O_{pp} = 14.2\%$, 25% and 33.3% were 0.8, 0.95 and 1.3, respectively, which explains well the measured electrical data in Figure 2.

![Figure 5. The Sn 3d$_{5/2}$ spectra of SnO films deposited at $O_{pp}$ of (a) 14.2%, (b) 25% and (c) 33.3%.

Figure 6a–c show the SIMS profiles of Hf, Sn and O atoms from the HfO2/SnO device structure annealed at 100, 200 and 400 °C, respectively. Increasing the annealing temperature from 100 to 400 °C led to significant Sn diffusion into SnO into HfO2. This is attributed to the weak Sn–O band enthalpy [38], even though it also leads to high hole mobility [15,16]:

$$\text{SnO} \rightarrow \text{Sn}^{2+} + \text{O}^{2-}$$

(2)

![Figure 6. SIMS depth profiles of HfO2/SnO stack annealed at (a) 100, (b) 200 and (c) 400 °C N2 ambient.

The charged Sn$^{2+}$ can diffuse into HfO2, create vacancies at elevated temperatures, and, together with charged O$^{2-}$ ions, allow HfO$_x$ diffusion into the SnO layer at 200 °C annealing temperature. The inter-diffusion of Sn and Hf atoms and the formed vacancies and charged ions further degrade the HfO$_2$ gate-dielectric and HfO$_2$/SnO interface that
cause poor $I_{GS}$, $\mu_{FE}$, $I_{ON}$, and $I_{OFF}$. The amount of Hf diffusion into the SnO layer at 400 °C annealing temperature can be calculated by the area within SnO layer in Figure 6c, which is 1.15 times higher than the HfO$_2$/SnO annealed at 200 °C. The Sn atoms diffused into HfO$_2$ layer at 400 °C were 1.14 times more than the HfO$_2$/SnO annealed at 200 °C. Thus, the higher post-annealing temperature will cause more inter-diffusion between HfO$_2$ and SnO.

The diffused Sn$^{2+}$ can behave as trap states in HfO$_2$ gate dielectric, provide extra transport paths for the carriers, and lead to higher gate leakage current (Figure 4b). To understand the conduction mechanism of gate leakage current, the measured data were fitted with various mechanisms. As shown in Figure 7a, the measured $I_{GS}$-$V_{GS}$ fits well with the hopping conduction $[44-47]$, under an electric field ($E$) of <0.25 MV/cm, for 100 and 200 °C annealed top-gate SnO p-TFTs, where the slope of $ln(|I_{GS}|)$-$E$ is 5.72 and 4.91, respectively. The hopping conduction mechanism is expressed as $[45]$:

$$|J| = \frac{q^2n}{kT} \times \exp \left[ \frac{qaE}{kT} - \frac{E_a}{kT} \right],$$  (3)

where $J$, $q$, $a$, $n$, $v$, and $E_a$ are the current density, electron charge, mean hopping distance, carrier concentration, thermal vibration frequency of carriers at trap states, and activation energy, respectively. The hopping distances of 100 and 200 °C annealed devices calculated from Equation (3) are 1.48 and 1.27 nm, respectively. The smaller hopping distance is ascribed to the Sn diffusion in HfO$_2$, which increases the gate leakage $I_{GS}$. The mechanism of poor gate leakage current and interface at high annealing temperature is depicted schematically in Figure 7b. The trap-induced hopping conduction causes high $I_{GS}$. The degraded interface by Sn and Hf inter-diffusion and created vacancies increase the hole scattering from the source to drain, thus lowering the important $I_{ON}$ and $\mu_{FE}$. The created vacancies also increase the $I_{OFF}$ through defect conduction. The device performance can be further evaluated by the $I_{DS}$-$V_{GS}$ hysteresis curves. The defect density formed by hysteresis curves, under forward and reverse sweep between 0 to $-3$ V, are $1.5 \times 10^{12}$ and $5.4 \times 10^{12}$ cm$^{-2}$ for device annealed at 100 and 200 °C, respectively. This result is consistent to our conclusion: the higher post-annealing temperature creates more defects in the HfO$_2$/SnO gate capacitor, which leads to higher gate leakage current, lower hole mobility, and poorer hysteresis than the one annealed at lower 100 °C temperature.

![Figure 7](image)

**Figure 7.** (a) $I_{GS}$-$V_{GS}$ characteristics of top-gate nanosheet HfO$_2$/SnO p-TFTs annealed at 100 and 200 °C. (b) Schematic diagram to show gate leakage and inter-diffusion of top-gate SnO TFT device annealed at 200 °C.

The sub-threshold slope is related to interface trap, which can be calculated $[48]$:

$$SS = \frac{KT}{q} \times ln10 \times \left(1 + \frac{C_{dep} + C_{it}}{C_{ox}}\right),$$  (4)
where the $C_{\text{dep}}$, $C_{\text{it}}$, and $C_{\text{ox}}$ are the depletion capacitance, interface trap capacitance and gate dielectric capacitance, respectively. The interface trap density ($D_{\text{it}}$) is $2.5 \times 10^{13}$ eV$^{-1}$cm$^{-2}$ that is higher than the metal-gate/high-$\kappa$/Si CMOS. Therefore, the hump of sub-threshold $|I_{\text{DS}}| - V_{\text{GS}}$ curve in Figure 2 is due to the charge modulation from the interface traps [49].

In comparison with SnO atomic density of $2.9 \times 10^{22}$ atoms/cm$^3$ or sheet atomic density of $9.4 \times 10^{14}$ atoms/cm$^2$, the $D_{\text{it}}$ is only 2.7% of the sheet atoms of SnO. Thus, the electronic measurement is highly sensitive to defects compared with other measurements.

The $\mu_{\text{FE}}$ data increase to a peak value and decrease with increasing gate field. The detailed physical analysis in oxide semiconductor transistor is not reported yet. However, such hole mobility dependence is generally observed in SiO$_2$/Si [50], high-$\kappa$/Si [51–53], SiO$_2$/SiGe [54], high-$\kappa$/SiGe [55] and high-$\kappa$/Ge [56] p-MOSFETs. Because the Si, SiGe, Ge and SnO are all semiconductors and have the similar valance band structure, the decreased mobility at high electric field may be due to the similar mechanisms of phonon and interface roughness scatterings [57].

The La$_2$O$_3$ can achieve the excellent performance of low leakage current and high-$\kappa$ value [55,58,59], but the moisture degradation is stronger than the HfO$_2$ and ZrO$_2$. The ZrO$_2$ [60] has a higher $\kappa$ value than HfO$_2$ once crystallized, which is widely used for dynamic random-access memory (DRAM) capacitor. For gate dielectric application, orientation-independent amorphous material like conventional SiO$_2$ is needed [61]. The TiO$_2$ has the highest $\kappa$ value but suffers from the small energy bandgap and high leakage current [62]. Thus, the TiO$_2$ is generally added to other high-$\kappa$ dielectric to increase the overall $\kappa$ value [63]. The Al$_2$O$_3$ has been used for gate dielectric due to its excellent stability [40], but suffers from relatively lower $\kappa$ value than HfO$_2$. Therefore, the HfO$_2$ is used for CMOS application and also for this work.

To inspect the stability of the top-gate SnO TFT devices, the devices were measured at as-fabricated and after retention in air ambient for two months, as depicted in Figure 8. In comparison with the conventional bottom-gate structure, such top-gate device shows huge stability improvement after retention in air [32], which is due to fully covered channel layer by metal-gate and gate-dielectric. Therefore, both the 100 and 200 °C annealed top-gate transistors show only slight degradation after exposure in air for two months. The top-gate HfO$_2$/SnO p-TFT has slightly lower hole $\mu_{\text{FE}}$ of 4.4 cm$^2$/Vs than our previously reported 7.6 cm$^2$/Vs of bottom-gate HfO$_2$/SnO device, which is attributed to the HfO$_2$/SnO inter-diffusion. Because of the larger SS of top-gate device than the bottom-gate one with the same HfO$_2$ and SnO, the HfO$_2$/SnO interface degradation is confirmed from Equation (4).

Table 1 presents a comparison of the essential device characteristics of top-gate SnO p-TFTs [11,33–35] The merits of this work are the highest $\mu_{\text{FE}}$ of 4.4 cm$^2$/Vs, largest $I_{\text{ON}}$/I$_{\text{OFF}}$ of $1.2 \times 10^5$, and sharpest SS of 526 mV/decade reported to date at fabrication temperatures of only 100–200 °C. This device thus has high potential to be integrated into the IMD layer of Si chips for monolithic 3D and brain-mimicking IC applications.

Table 1. The device performances of various top-gate SnO p-TFTs.
reported 7.6 cm²/Vs of bottom-gate HfO₂/SnO device, which is attributed to the HfO₂/SnO inter-diffusion. Because of the larger SS of top-gate device than the bottom-gate one with the same HfO₂ and SnO, the HfO₂/SnO interface degradation is confirmed from Equation (4).

![Figure 8](https://www.mdpi.com/2079-4991/11/1/92/s1, Figure S1: The surface roughness analysis of HfO₂ annealed at (a) 100 °C, (b) 200 °C and (c) 400 °C through AFM. Figure S2: The O₁s spectra of HfO₂ films annealed at (a) 100 °C, (b) 200 °C and (c) 400 °C.

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