1 Introduction

The recent development of Deep Neural Networks (DNNs) has made machine learning based smart solutions more relevant and accessible to the general public. We have seen that some DNN technologies have been integrated into our daily applications to provide high-quality inference services, such as image recognition, natural language processing, self-driving cars, and augmented and virtual reality [1,2,3,4], which have made our lives more convenient and our work more efficient. A significant number of these machine learning applications leverage edge devices and need to be deployed onto resource-constrained embedded systems, such as cell phones, cameras, and unmanned aerial vehicles (UAVs). They require not only higher inference accuracy to achieve intelligent responses but also aggressive inference speed, throughput, and energy efficiency to meet real-life demands.

As DNNs become more complicated, developing and serving the DNN-enabled applications requires more compute and memory resources, longer latency, and greater energy consumption. For example, the computation demands for DNN training have risen by over 300,000 times between AlexNet [5], the champion model of the 2012 ImageNet competition, and the AlphaGo Zero [6], the AI player proposed by DeepMind.
in 2017 for the board game Go with superhuman skills [7]. By checking the image recognition models, there is a 16 times increase in model complexity from AlexNet with 85% top-5 accuracy to ResNet-152 [2] with 95% top-5 accuracy.

Such exponentially increasing compute and memory demands have created challenges and difficulties for DNN deployment on hardware, especially when targeting edge embedded devices with strictly limited compute and memory resources and tight power budgets [8, 9]. Although cloud computing can alleviate the burden of edge computing by taking over computationally intensive tasks, it is not always feasible when dealing with various real-life scenarios. Primary reasons for sticking to edge embedded devices come from the unique requirements of the edge applications, which typically require real-time decision-making and reduced reliance on network communication and accessibility. They typically cannot tolerate the extra latency caused by network data transfer due to the real-time response requirements. In addition, private information, such as personal and sensitive data, should not be uploaded to the cloud without permission. It means that the edge devices are required to deliver not only high inference accuracy from DNNs, but also aggressive inference speed, throughput, and energy efficiency to meet various real-life demands. In summary, the challenges of deploying machine learning workloads on edge embedded devices mainly come from three aspects: 1) DNN models are getting complicated and may fail to run efficiently, especially when targeting the low-power edge devices with scarce compute and memory resources; 2) Mapping DNN onto existing hardware or building domain-specific hardware is tedious and time-consuming; 3) Additional challenges come from inefficient optimization strategies that focus only on hardware or software optimizations alone but lack software/hardware co-design or cross-system stack design methods that can potentially deliver better overall solutions.

Despite the aforementioned challenges, there has been continuous progress in recent studies to explore various optimization strategies for edge machine learning solutions. In this chapter, we present comprehensive design methodologies to face and overcome the challenges and enable efficient DNN applications on embedded systems. These methods include efficient DNN model designs in Sec. 3, accelerator design and workload mapping technologies in Sec. 4, and cross-stack optimization strategies in Sec. 5.

2 Background and Related Works

2.1 Efficient DNN designs

DNN is one of the most recent breakthroughs to enable machine intelligence in many of our daily applications. A DNN includes multiple intermediate layers between the input and output layers, and each intermediate layer consists of artificial neurons for transforming the input information (e.g., input feature maps) following the predefined network connection. In general, a DNN contains millions of parameters and
requires billions of operations during inference. To successfully deploy DNNs onto hardware with desired performance, developers focus on network compression to reduce network complexities and lower the compute and memory demands. Recent research has demonstrated the possibility of using quantized data to represent original floating-point parameters, such as using 8-bit quantization or even binary and ternary data representation \[10,11,12,13,14,15\]. These solutions are intended to replace the hardware-intensive floating-point multiplications by logical operations so that DNNs can be more efficient on hardware platforms.

Another method to compress DNN is network pruning, which aims to reduce the redundancy of DNN structures \[16,17,18\]. According to the published pruning strategies, the less essential connections between DNN layers are discarded, and network retraining is then performed to regain accuracy. Significant reductions can be achieved on the classic DNNs, such as AlexNet \[5\] and VGG-16 \[19\]. Since the major benefit of network compression comes from the fully-connected (FC) layers, to continuously have effective pruning results for latter DNNs (e.g., GoogleNet \[20\] and ResNet \[2\]) with fewer FC layers, more sophisticated algorithms are required to achieve effective network pruning, such as using evolutionary algorithms \[21\], alternating direction method of multipliers \[22\], and iterative pruning \[23\].

As most of the computations happen inside the convolutional (Conv) layers, previous works also attempt to reduce the computational complexity by using depth-wise separable Conv layers \[24\]. The depth-wise separable structure can effectively reduce the number of operations and provide more compact DNN designs for resource-constrained hardware. To further improve the DNN deployment on hardware, layer fusion is proposed in \[25\] to minimize data movements between on-chip and off-chip memory.

### 2.2 Efficient accelerator designs and DNN mapping methods

Building domain-specific hardware accelerators is another popular approach for efficient DNN deployment. These accelerators attempt to take advantage of customized or specialized hardware and software designs, such as adopting acceleration libraries on CPUs \[26\], exploring kernel optimization on GPUs \[27\], and building customized accelerators on FPGAs \[28,29,30\] and ASICs \[31,32,10\] to improve the speed and efficiency of DNN inference and training processes. Among these accelerator designs, FPGA- and ASIC-based designs can be fully customized to implement the neural network functionality with improved latency, throughput, and energy consumption compared to CPU- and GPU-based designs.

Still, developing customized accelerators present significant challenges, such as the tedious hardware design process, the intricate hardware verification problems, and the time-consuming design space exploration during DNN deployment. To alleviate these challenges, recent investigations have started focusing on techniques including high-level synthesis \[33,34,35\] and end-to-end design frameworks for fast DNN accelerator design and efficient workload deployment \[36,30,37,38\]. They
support high abstraction inputs, such as Python-based DNN descriptions used by popular machine learning frameworks (e.g., Caffe [39], TensorFlow [40], PyTorch [41]), so DNNs can be directly imported without manual code conversions and be parsed and then mapped onto hardware. These frameworks, such as DNNBuilder [30] and HybridDNN [37] also integrate design space exploration (DSE) engines to perform effective and systematical explorations and deliver highly optimized accelerators to meet the user-specific requirements.

2.3 Efficient co-design optimization

Recent research also focuses on cross-stack co-design optimizations to enable successful DNN deployment on embedded systems [42]. Instead of independently optimizing hardware and software components, researchers proposed algorithm/accelerator co-design and co-search to solve the edge AI challenges: DNNs are designed to satisfy accuracy demands and must be aware of the hardware constraints with rational network configurations. At the same time, the accelerators need to provide extensive support for different DNN components without introducing too many restrictions on network design and guarantee performance to meet the specifications. The authors in [43] proposed the concept of DNN/accelerator co-design for the first time, which aims to consider software and hardware metrics simultaneously to “automatically generate both DNN models and their corresponding implementations as pairs”. This concept is then demonstrated by winning the competitive System Design Contest for low power object detection in the 56th IEEE/ACM Design Automation Conference (DAC-SDC) [44].

Many follow-up works continued investigating the co-design opportunities between different AI algorithms and hardware devices [45, 46, 47, 48, 49, 50, 51, 52]. These co-design approaches have been studied with remarkable achievements by combining multiple optimization techniques across both hardware and software. For example, while neural architecture search (NAS) has been largely successful in designing high-quality DNN models [53, 54], hardware-aware NAS is drawing increasing attention, which aims at delivering high-accuracy models with hardware efficiency as well (e.g., FBNet [55] and MnasNet [56]). Other machine-learning algorithm/hardware co-design works include FNAS [57], NAIS [48], EDD [58], and NASAIC [59]. Driven by the success of such a co-design strategy, other types of co-design methods are also proposed recently, including software/compiler co-design [60, 61, 62, 63], compiler/hardware co-design [64, 65, 66], etc.

3 Efficient Machine Learning Model Designs

Machine learning applications require not only high inference accuracy but also aggressive inference speed, throughput, and energy efficiency to meet real-life de-
mands. They rely on hardware-efficient DNN designs, especially when targeting edge scenarios with limited hardware resources. In this section, we introduce ELB-NN [12] and VecQ [14] to deliver hardware-efficient DNNs for embedded systems.

3.1 The ELB-NN

ELB-NN (Extremely Low Bit-width Neural Network) is proposed to enhance energy efficiency when running image classification on an embedded FPGA. It is one of the first hybrid low-bit-width designs that supports arbitrary DNN quantization. This subsection presents the hybrid quantization feature of the ELB-NN and its corresponding hardware accelerator design on embedded systems.

3.1.1 Hybrid quantization scheme

Hybrid quantization means that different quantization schemes are involved for the network’s parameters and activations. The quantization scheme can go all the way down to binary. To better adapt the hybrid quantization, we first investigate their impacts on the network inference accuracy. We follow Eq. 1 to calculate the binary weights. Here $\tilde{w}$ represents the full precision weights after back propagation, while $E(|\tilde{w}|)$ represents the mean of all the full-precision weights as a scaling factor. For the ternary training, the $w_t$ (representing ternary parameters) can be calculated following Eq. 2. Here we set the threshold $w_{ihres} = 0.7 E(|\tilde{w}|)$ and calculate the scaling factor $E$ as suggested in [67]. We also apply relatively high precision using 8- or 4-bit fixed-point representation. We then use AlexNet [5] to perform quantitative analysis when applying hybrid quantization.

$$w_b = \text{sign}(|\tilde{w}|) \times E(|\tilde{w}|)$$

$$w_t = \begin{cases} 
\text{sign}(\tilde{w}) \times E & |w_t| > w_{ihres} \\
0 & |w_t| \leq w_{ihres}
\end{cases}$$

Fig. 1 Network representation when using hybrid quantization

In this analysis with AlexNet, we focus on the impact of 1) the quantized parameters of the convolutional (CONV) and fully-connected (FC) layer, and 2) the
quantized activations. We use mid-CONV to denote all the CONV layers except the first CONV layer and mid-FC to denote all the FC layers except the last FC layer. The naming rule of the proposed hybrid precision network can be referred to Fig. 1.

| Network precision            | Accuracy (Top-1) |
|------------------------------|------------------|
| Alexnet with float32         | 55.9%            |
| Alexnet-8-8888                | 54.6%            |
| Alexnet-8-8228                | 53.3%            |
| Alexnet-8-8218                | 52.6%            |
| Alexnet-8-8118                | 51.1%            |
| Alexnet-4-8218                | 49.3%            |
| Alexnet-2-8218                | 46.1%            |
| Alexnet-4-8218 (w/o g.)      | 53.2%            |
| Alexnet-4-8218 (ext.)        | 54.5%            |

In Table 1 the 8-bit design (Alexnet-8-8888) only reduces the accuracy by 1.3% compared to the original float32 version. The accuracy is still promising after using ternary (Alexnet-8-8228) and binary (Alexnet-8-8218) parameters for mid-CONV and mid-FC layer. It means that the network is relatively robust to the precision of parameters. On the contrary, the precision of activations significantly impacts classification accuracy. Compared to the Alexnet-8-8218, we observe 3.3% and 6.5% accuracy drop when activations move to 4 bits (Alexnet-4-8218) and 2 bits (Alexnet-2-8218). To further investigate, we disable the group function, which was originally proposed to handle the limited GPU memory issue. As a result, we capture an 80% computation increase and a 3.9% accuracy improvement in Alexnet-4-8218 (w/o g.). We further increase the channel number for the five CONV layers in Alexnet-4-8218 (ext.) and achieve 1.3% accuracy gain by affording extra 61% computation compared to Alexnet-4-8218 (w/o g.). By increasing the model complexity, we can bring back the accuracy. These observations are insightful for hybrid DNN quantization as parameters can be quantized more aggressively than activations.

### 3.1.2 Hardware accelerator for ELB-NN

To handle ELB-NN, we propose a parameterized Computation Engine (CE) in [12] with flexible support of low bit-width quantization and configurable parallelism during execution. As shown in Fig. 2 it contains a four-input-parallel CE as an example, where four inputs can be processed simultaneously (including binary/ternary operations and accumulation) and then followed by batch normalization (BN) and activation function. The precision of the accumulator is adjustable, which is intended to allow more flexible quantization designs and maintain the output accuracy. For a larger number of inputs, an adder tree will be used before the accumulator for timing enclosure.
To demonstrate the hardware efficiency of ELB-NN, we adopt the accelerator with the proposed CE and accelerate different quantized versions of the AlexNet and VGG16 using an embedded platform called ZC706 (with an ARM CPU and a Xilinx Kintex-7 FPGA). Results are shown in Table 2. ELB-NN can achieve throughput performance up to 10.3 TOPS, which outperforms previous designs in [69, 70, 71].

Table 2 ELB-NN performance evaluated on an embedded platform (Xilinx ZC706) [12].

| Network                  | Utilization | Batch size | Bandwidth (GBs/s) | Complexity (GOP) | Images/s | Perf. (TOPS) |
|--------------------------|-------------|------------|-------------------|------------------|----------|--------------|
| Alexnet-8-8888           | 862 (39%)   | 513 (48%)  | 201 (64%)         | 808 (83%)        | 2        | 10.8         |
| Alexnet-8-8218           | 1015 (47%)  | 901 (41%)  | 43 (89%)          | 558 (61%)        | 5        | 4.35         |
| Alexnet-4-8218           | 1056 (48%)  | 941 (46%)  | 64 (92%)          | 1369 (69)        | 8        | 13.5         |
| Alexnet-4-8218 (w/o g.)  | 1273 (58%)  | 1033 (80%) | 43 (91%)          | 1198 (59)        | 7        | 4.30         |
| Alexnet-4-8218 (ext.)    | 1243 (57%)  | 1015 (61%) | 48 (94%)          | 592 (22)         | 7        | 4.22         |
| VGG16-4-8218             | 1129 (52%)  | 993 (99%)  | 80 (93)           | 1107 (3)         | 2        | 5.85         |
| VGG16-2-8118             | 1379 (63%)  | 1132 (82%) | 49 (99)           | 332 (2)          | 3        | 6.67         |

3.2 The VecQ

Vectorized Quantization (VecQ) is a training quantization framework that is based on a novel quantization loss measurement metric called vector loss. It is proposed to provide flexible bitwidth support with minimal quantization loss to achieve higher model accuracy. In this subsection, we present the detailed definition of vector loss and the VecQ quantization framework.
3.2.1 Quantization with Vector Loss

We use the square of the Euclidean distance of the data before and after quantization to represent quantization loss. It is also called Square 2-norm or L2 distance. Minimizing the L2 loss during the model training is proved to be adequate in providing higher model accuracy [72, 73, 74, 68, 75]. However, due to the non-convex characteristic of optimization for L2 loss under a constrained bitwidth requirement, the quantization easily falls into sub-optimal solution space. In addition, adopting the L2 distance collects the loss of each quantized data individually and neglects the distribution and correlations among these data points in a kernel or a layer.

Focusing on the limitations above, in VecQ, we first flatten and reshape the weight set $W_f(l)$ for a layer of the DNN and reshape them as a vector $w_f(l)$ with the dimension of the size of the elements. For example, it will be a $N \times M \times K^2$-dimensional vector for a CNN layer with $N$ input channel, $M$ output channel and $K$ size of filter kernel. The quantized weight vector is denoted as $w_q(l)$.

![Fig. 3 The attributes of a vector and the quantization angle of $w_f$ and $w_q$.](image)

There are two attributes of a vector, as shown in Fig. 3: orientation and modulus. We define a quantization angle representing the intersection angle between the original weight vector and the quantized vector. So, the vector distance between the weight vector before and after quantization is determined by the quantization angle and the vector's modulus. We then define a vector loss, denoted as $J_v$, and compose it with the orientation loss $J_o$ and the modulus loss $J_m$.

$$J_v = J(w_f, w_q) = J_o(w_f, w_q) + J_m(w_f, w_q)$$ (3)

Where $J_o$ and $J_m$ are computed as:
\[ J_o = 1 - \cos \theta, \quad \cos \theta = \frac{\alpha w_q \cdot w_f}{|\alpha w_q||w_f|} \]
\[ = 1 - e_v e_{w_f} \]
\[ = 1 - \sum_{i=1}^{d} (e_{v_i} e_{w_{f_i}}) \]
\[ J_m = ||w_f - \alpha w_q||^2 \]

here, the \( e_v \) and \( e_{w_f} \) represent the unit vector for \( v \) and \( w_f \). \( w_f \) is a weight vector of a layer of a DNN containing \( d \) weights.

With these approaches, the orientation loss \( J_o \) indicates the optimized quantization angle and the modulus loss \( J_m \) indicates the optimized scale at this angle. Therefore, our quantization takes two stages to minimize the two losses independently, which are defined as steering stage and driving stage as shown in Fig. 4. In the steering stage, we adjust the orientation of the weight vector to minimize the orientation loss. Then, we fix the orientation and only scale the modulus of the vector at the driving stage to minimize the modulus loss.

Fig. 4 The overall flow of quantization process, including both steering and driving stage [14].

3.2.2 Framework integration

Fig. 5 Integrated quantization process in DNN training [14].
The VecQ quantization is integrated into the DNN training flow for both the weight data and the activation data. As shown in Fig. 5, for weight data, taking a layer $l$ as an example, during the forward propagation, the weights $w_f(l)$ represented in floating-point is quantized into $w_q(l)$, then use the quantized weights to compute the output of this layer. To simplify the computing process, the weight is treated as normally distributed and an interval $\lambda$ is used regarding the given bitwidth constraint. During the backward propagation, the gradient is calculated with $w_q(l)$ instead of $w_f(l)$ and propagated. In the final update process, the gradient $g(l)$ of $w_q(l)$ is updated to $w_f(l)$ [68].

For the activation output of a layer, during the training, we compute a distribution parameter of the activation outputs $p(t)$ and update it with Exponential Moving Average. During the inference, the distribution parameter is employed as a linear factor to the activation function [76]. The $A(l)$ is the activation output of layer $l$, and $Activation(\cdot)$ is the non-linear activation function following the convolution or fully-connected layers, such as Sigmoid, Tanh, ReLU.

We evaluate VecQ on image classification task with the popular models and compare the results to the state-of-the-art quantization solutions with the same DNN model and bitwidth configurations. The state-of-the-art quantization solutions include BWN [11], TWN [67], TTQ [77], TSQ [78], INQ [79] and ENN [80]. Note here, not all of these quantization solutions provide bitwidth support from 1 to 8 bits. As shown in Fig. 6, our VecQ quantization outperforms most of the solutions with the same bitwidth configurations, and VecQ provides a wider range of bitwidth coverage as well. It only loses the advantage when comparing to the solutions specifically designed for binary weights.

Fig. 6 Comparison with state-of-the-art solutions.
4 Efficient accelerator design and workload mapping

As discussed before, there exists an ever-widening barrier between fast DNN model design in software and slow hardware accelerator implementation. To bridge the hardware-software gap, in this section, we introduce DNNBuilder [30] and PyLog [38] to provide efficient solutions for automatically generating high-performance hardware accelerators for DNN workload deployments.

4.1 DNNBuilder

DNNBuilder is an end-to-end automation framework that can transform DNN designs from popular deep learning frameworks to highly optimized hardware deployment on customized accelerators implemented on FPGAs. Users are no longer required to design and optimize accelerators manually but can enjoy the auto-generated hardware accelerators for desired AI workloads. DNNBuilder introduces two major architecture innovations: the fine-grained layer-based pipeline architecture and the column-based cache scheme, which achieve 7.7× and 43× reduction of latency and on-chip memory usage, respectively. This subsection presents the novel designs introduced by DNNBuilder and showcases its promising edge AI performance.

4.1.1 An end-to-end automation flow

DNNBuilder produces customized DNN accelerators in three steps as Design, Generation, and Execution (Fig. 7). During the Design step, a DNN is designed and trained using deep learning frameworks, which in general employ CPUs and GPUs. After training, network definition files and trained parameters are passed to the next step. To ensure design freedom specified by users, the proposed flow supports hybrid
quantization schemes, where different quantization schemes can be applied to the parameters and activations of different network layers, to explore tradeoffs among inference accuracy, resource utilization, performance, etc. One important feature of this step is the feedback function that provides hardware metrics estimation. If the current DNN runs slower or consumes more resources than expected, users could update their network designs, such as adjusting quantization schemes or modifying network layers to meet performance and resource requirements. This function also makes the hardware-software co-design possible.

In the Generation step, network parsing is launched to decompose the input models. Different network layers, e.g., CONV, Pooling, and FC layers, are decomposed and then mapped to our pre-built RTL IPs, which are the basic building blocks of the generated accelerator. The computational intensive nested loops are captured by parameterized compute engines. Then, automated optimization works for exploring the hardware design space and provides configuration guidelines so that the generated accelerator can achieve maximum performance. Following these guidelines, network construction is responsible for building DNN implementations with the pre-built RTL IPs, dataflow controller, and memory instances, which are highly configurable to ensure the adaptability and scalability for various DNNs. After that, code generation generates accelerator related files for FPGA-based instances.

In the Execution step, the DNN accelerator is instantiated in FPGA with unified interfaces, including a FIFO-like data input/output interface and a weight access interface connecting the off-chip memory controller. In this final step, the DNN accelerator is ready for eventual deployment.

4.1.2 Architecture novelties

Fig. 8 Latency comparison between the proposed fine-grained (left) and conventional (right) pipeline when handling the same object detection DNN model with a ZC706 embedded FPGA [30].

We propose a fine-grained layer-based pipeline to deliver high throughput performance and promising real-time response. Each major neural network layer, such as CONV or FC layer, in the targeted DNN model, is handled by one pipeline stage,
as major layers dominate computation and memory consumption. The rest of the layers, such as batch normalization (BN), scale, and activation layers, are aggregated to their neighboring major layers so that we reduce the number of pipeline stages for lower latency. In addition, DNNBuilder enables pipeline stage overlapping to overcome the long initial latency, which is frequently encountered by conventional pipelines. We demonstrate the proposed fine-grained layer-based pipeline by accelerating an object detection DNN model called YOLO \cite{81} and show the results in Fig. 8. DNNBuilder can effectively hide the data transmission delay and generate outputs even when the first input frame is still loading. It helps achieve a 7.7\times smaller startup latency (9.92ms) compared to the conventional pipeline design (411.99ms).

![Figure 9: The proposed column-based cache scheme \cite{30}.](image)

The other novel design is the column-based cache scheme, which reduces on-chip memory utilization during DNN inference and supports high-definition image input for resource-constrained embedded systems. By following the pipeline architecture, intermediate results between pipeline stages are stored on-chip to guarantee seamless pipeline operations. However, feature maps can be enormous when inputs become large in real life and become impossible to be held on-chip entirely. The column-based cache scheme is designed to address this problem as it only keeps a subset of the input feature map on chip. Fig. 9 shows an example when DNNBuilder processes a convolution layer (with kernel size=3 and stride=1). Since slices 1~3 contribute to the first sliding window operation (from top to bottom), we name the first three slices as column 1. Similarly, column 2 represents the amount of data for the second sliding window operation, so that slices 2~4 constitute column 2. DNNBuilder caches at least two columns before starting computing, which allows the kernel to perform the second vertical sliding window operation immediately after finishing the first one. Delay caused by data shortage will not happen by caching one more column.
Meanwhile, slice 5 will start buffering to form the next column (with slices 3~5) after releasing the room taken by slice 1. By serving the same objection detection AI model (YOLO with high-definition inputs), the proposed column-based cache can significantly reduce 43× on-chip memory usage compared to the accelerator without this technology [30].

4.1.3 State-of-the-art performance

We demonstrate our design by accelerating popular AI workloads on an embedded platform (ZC706). As shown in Table 3, our DNNBuilder generated design reaches the best performance (524 and 262 GOPS in Fix8 and Fix16 quantization schemes) and power efficiency (72.8 GOPS/Watt in Fix8 and 36.4 GOPS/Watt in Fix16). We also extend our comparison to the embedded GPU (TX2) in Table 4. The DNNBuilder-generated design can deliver higher efficiency than the TX2-based solution even without using batch processing (batch size = 1), and it can achieve up to 47.2 image/Second/Watt.

| Table 3 | Comparison with existing embedded FPGA-based DNN accelerators [30]. |
|---------|---------------------------------------------------------------|
| Reference | FPGA chip | Frequency | Network | Precision | DSPs (used/total) | DSP Efficiency | Performance (GOPS) | Power Efficiency (GOPS/W) |
| DNNBuilder | Zynq XC7Z045 | 150 MHz | VGG | Fix16 | 780/900 | 44.0% | 137 | 14.2 |
| [29] | Zynq XC7Z045 | 100 MHz | VGG | Fix16 | 824/900 | 69.6% | 230 | 24.4 |
| [82] | Zynq XC7Z045 | 200 MHz | VGG | Fix16 (Fix8) | 680/900 | 96.2% | 262 (524) | 36.4 (72.8) |

| Table 4 | Alexnet inference comparison on embedded GPU and FPGA platforms [30]. |
|---------|---------------------------------------------------------------|
| Platform | Precision | Batch | Throughput (img/S) | Power (W) | Efficiency (img/S/W) |
| DNNBuilder (ZC706) | Fix16, Fix8 | 1, 2 | 170, 340 | 7.2 | 23.6, 47.2 |
| GPU-TX2 [83] | Float16 | 2 | 250 | 10.7 | 23.3 |

4.2 PyLog: A Python-based FPGA Programming Flow

The fast-growing complexity of new applications and new use scenarios poses serious challenges for computing systems. Embedded hardware accelerator systems
have demonstrated great flexibility, performance, and efficiency in many different applications and scenarios. However, as system complexity and application complexity grow rapidly, programming and optimizing embedded accelerator systems require great manual efforts and consume a lot of time. Compiling and optimizing a general application specified in high-level programs like Python are becoming common tasks in creating embedded accelerator designs.

4.2.1 PyLog Flow Overview

PyLog \cite{38} is a Python-based high-level programming flow for FPGAs. It allows users to create FPGA accelerators with Python code using PyLog high-level operators and Python syntax. PyLog presents a unified programming model for host and accelerator logic with consistent Python-based syntax and semantics. This seamless host-accelerator programming model enables agile system design, convenient functional simulation, and flexible design space exploration.

Fig. 10 shows the overall PyLog at high level. PyLog flow allows users to create efficient FPGA accelerators and program host system with Python. The input to the PyLog flow is Python code, where the FPGA kernel function is decorated with the \texttt{@pylog} decorator. The PyLog flow contains an accelerator synthesis flow and a runtime flow.

![PyLog Flow and Example System Architecture](image)

In the accelerator synthesis flow, the \texttt{@pylog} decorator calls the PyLog compiler to compile the kernel function into optimized high-level synthesis (HLS) C code,
which is then compiled into efficient FPGA IPs with HLS flow, and integrated into a complete accelerator system by PyLog system generator. Beside the PyLog kernel function, the rest of the PyLog program is interpreted by the standard Python interpreter running on the host CPU side, which supports all Python libraries and language features. This part of PyLog program naturally becomes the host program of whole accelerator system. After the accelerator system is generated by the synthesis flow, the system can be deployed at the target FPGA platform using the generated FPGA bitstream configuration file, and runs with support from the PyLog runtime flow. During runtime, PyLog runtime can prepare input data, launch accelerator, and collect results according to the host code. Host CPU and the FPGA accelerator interactions are handled automatically by the PyLog runtime and the underlying Xilinx PYNQ library [84].

4.2.2 PyLog Features

PyLog has several unique features that help users to create FPGA accelerators more efficiently.

(i) **High-Level Operators.**

In addition to commonly used Python standard language features, PyLog also supports several built in high-level operators and NumPy operators that allow users to express computation patterns at high level and enable better compiler optimizations. Table 5 summarizes the language features supported in PyLog, including PyLog high-level operators, NumPy operators, and standard Python features. Listing 1 demonstrates a few example usages of PyLog map and dot operators.

| Category          | Operators                           |
|-------------------|-------------------------------------|
| PyLog high-level operators | map, dot, user-defined ops          |
| NumPy operators   | argmax, argmin, max, min, matmul, convolve, sort |
| Python features   | list, functions, calls, lambda, for, while, if...else..., slice, subscript, attribute, bin_op, unary_op, return |

1 # Vector add
2 out = map(lambda x, y: x + y, vec_a, vec_b)
3
4 # 1D convolution
5 out = map(lambda x: w0*x[-1]+w1*x[0]+w2*x[1], vec)
6
7 # Inner product
8 out_vec[i] = dot(matrix[i,:], in_vec)
9
10 # Square matrix multiplication
11 out = map(lambda x,y: dot(x[:,i], y[i,:]), ma, mb)
Listing 1  PyLog map and dot examples. [38]

These operators not only simplify programming for users, they also pass more information on computation to the compiler (e.g., computation patterns, data flow information, data/task parallelism, etc.), compared to programming in C/C++, and thus allows compilers to perform more optimizations and choose the optimal code generation.

Fig. 11 shows an example of generating multiple hardware implementations from a PyLog map operation. The compiler generates HLS C implementations in different styles, which corresponds to different hardware structures, e.g. shift registers, systolic arrays, etc. Depending on the context and constraints, the optimal implementation will be chosen.

(ii) Type Inference and Type Checking.

Python is a dynamically typed languages and there is no explicit type declaration in the Python code. PyLog has a built-in type inference and type checking engine that can infer the type and shape information of code objects in the PyLog kernel functions. This type inference engine is critical in PyLog since same operators may have completely different meanings when applied to operands with different types or shapes. With this type inference engine, PyLog users do not need to provide explicit type annotations or hints in PyLog program.

(iii) Compiler Optimizations.

PyLog provides a set of compiler optimizations that improve the design quality of generated accelerators. PyLog uses its own PyLog intermediate representation (PLIR) as the internal representation of the input code. PyLog code analysis and transformation passes work on PLIR to perform a sequence of optimizations including high-level operator lowering, loop transformation, HLS pragma insertion, etc. The internal PLIR is capable of expressing different design options and can therefore form a design space that not only covers low-level design
parameter tuning, but also high-level design pattern selection, which has not been explored in previous tools.

4.2.3 PyLog Evaluation Results

We evaluate the performance of PyLog in terms of expressiveness and accelerator performance, using real-world applications.

(i) **Expressiveness.** We evaluated the expressiveness of PyLog by comparing the number of lines of code to implement a benchmark using PyLog and HLS C. For the benchmarks evaluated, on average PyLog only needs around 30% of the code length of HLS C. This indicates that PyLog provides good expressiveness compared with HLS C and allows users to describe their computation with fewer lines of code.

(ii) **Accelerator Performance.** We evaluated the performance of the accelerators generated by PyLog using real-world benchmarks. Evaluation was done on Amazon EC2 F1 f1.2xlarge instance. The evaluated benchmarks are from different domains and have various computation patterns. They are representative FPGA workloads, including linear algebra, data analytics, stencil, sparse operations, etc. Amazon EC2 F1 f1.2xlarge instance is a cloud computing platform that has an 8-core Intel Xeon E5-2686 v4 CPU and a Xilinx Virtex UltraScale+ XCVU9PFPGA. Table 6 shows the evaluation results. The table lists the FPGA resource utilization as well as the accelerator execution time. We compared the PyLog accelerator execution time against the optimized CPU time as well as the execution time of accelerators generated from [85]. On average, PyLog accelerators achieve around $3.17 \times$ and $1.24 \times$ speedup over CPU baseline and manually optimized accelerators [38].
Table 6 Accelerator Performance Evaluation on AWS F1 Instance

| Benchmark | LUT | FF | BRAM | DSP | $f$ (MHz) | $P$ (W) | $T_{CPU}$ | $T_{HCL}$ | $T_{PyLog}$ | $T_{CPU}$ | $T_{HCL}$ | $T_{PyLog}$ |
|-----------|-----|----|------|-----|---------|-------|---------|---------|-----------|---------|---------|-----------|
| KNN       | 109276 | 74889 | 425 | 0  | 256.40  | 37.222 | 0.48 | 0.45 | 0.26 | 1.85 | 1.73 |
| K-means   | 10829 | 17604 | 3  | 7  | 273.97  | 37.429 | 38.16 | 4.24 | 4.45 | 8.58 | 0.95 |
| Jacobi    | 93925 | 111144 | 96 | 304 | 268.73 | 36.011 | 11.31 | 8.25 | 5.19 | 2.18 | 1.59 |
| Seidel    | 47304 | 57854 | 30 | 304 | 268.03 | 37.341 | 21.37 | 8.22 | 5.16 | 4.14 | 1.59 |
| Gaussian  | 56580 | 75846 | 48 | 688 | 147.15 | 37.783 | 23.63 | 7.34 | 5.19 | 4.55 | 1.41 |
| GEMM      | 12868 | 63759 | 655 | 1024 | 250.00 | 39.657 | 60.34 | 8.13 | 13.05 | 4.62 | 0.62 |
| SpMV      | 8294  | 12787 | 25 | 21  | 273.97 | 37.225 | 0.29 | -    | 0.24 | 1.21 | -    |
| Histogram  | 4096  | 7647  | 13 | 0   | 273.97 | 37.327 | 5.85 | -    | 2.07 | 2.83 | -    |

Geometric Mean 3.17, 1.24

$T_{CPU}$: Execution time on CPU; $T_{HCL}$: Execution time on HeteroCL [85] generated accelerator; $T_{PyLog}$: Execution time on PyLog generated accelerator; All time values are in milliseconds (ms); '-' means the implementation is not publicly available.

5 Efficient Optimizations

With a great number of efficient optimization techniques, in this section, we introduce three key optimization techniques: hardware-aware NAS, FPGA/DNN co-design, a specialized approach for FPGA/DNN co-design [45], and a unified differentiable co-design approach, across different platforms [58].

5.1 Hardware-aware Neural Architecture Search (NAS)

Neural Architecture Search (NAS) refers to the automated process of neural architectural design [88]. It has been largely successful in producing many state-of-the-art networks. Typically, a NAS process requires three distinct components:

1. **Search space.** A search space includes all possible network architectures that follow a predefined template. For example, the networks can be sequential layer-wise architecture [89, 90], cell-based architecture [54], and hierarchical architecture [56].

2. **Search algorithm.** NAS search algorithms usually sample child networks from the search space. Given the prohibitively large search space, the search algorithm can greatly influence the efficiency of the search and the effectiveness of the final network architecture. Generally, search algorithms can be classified into two categories: super-net-based search [91, 55] and sampling-based search [89, 92, 93].

3. **Network evaluation.** Network evaluation is the key for efficient NAS, since fast evaluation is required to estimate the quality of individual networks to guide the search algorithm to choose top-performing architectures from the search space. Network evaluation can be prohibitively expensive due to network training.
so that various approximation approaches have been proposed to expedite the evaluation such as few-shot and one-shot training \cite{94, 95} and using proxy tasks \cite{96}.

5.1.1 HW-aware NAS Formulation

In recent years, driven by the need of deploying power-hungry DNNs into resource-constrained devices, hardware-aware NAS (HW-NAS) has emerged as one of the most promising techniques \cite{97}. There is a great amount of hardware-aware work, each of which often adopts a specific hardware device (CPU, GPU, embedded/mobile device) and requires a different hardware-cost metric (e.g., prioritizes latency or energy). For example, FBNet \cite{55} develops a differentiable neural architecture search (DNAS) framework and discovers state-of-the-art DNNs balancing both accuracy and hardware efficiency, by incorporating a loss consisting of both the cross-entropy loss that leads to better accuracy and the latency loss that penalizes the network’s latency on a target device. To provide more integrated co-optimization solutions, EDD \cite{58} fuses the design space of DNN architecture and hardware accelerator and formulates the DNN and hardware design as a co-search problem. EDD aims to discover the most suitable combination of DNN and hardware within the co-search space and maximize software and hardware metrics given the targeted edge AI application. Once for All (OFA) \cite{98} is the first work that proposes an elastic training scheme for supernet. By training the supernet, high-accuracy architectures is directly searched by selecting from the OFA network without additional training.

One of the classic search method for HW-NAS is to first define a template based search space, and then incorporate hardware performance into the loss function:

\[
L = L_T + L_{HW} \quad \text{or} \quad L = L_T \cdot L_{HW}
\]

where \(L_T\) is the task-specific loss of NAS, such as cross-entropy loss for classification tasks or Mean squared error (MSE) loss for regression tasks. \(L_{HW}\) is the hardware performance loss, such as measured or estimated execution latency of the network architectures on the target device.

5.2 FPGA/DNN Co-design

Hao and Chen first proposed the concept of accelerator and DNN co-design in an invited paper titled “Deep Neural Network Model and FPGA Accelerator Co-design: Opportunities and Challenges” \cite{43}, where they advocated “automatically generate both DNN models and their corresponding implementations as pairs”. Later, based on the proposed co-design method, we implemented the first simultaneous FPGA/DNN co-design framework \cite{45}. It has two major components, as shown in Fig. \ref{fig1} (1) a hardware-oriented bottom-up DNN model design, named Auto-DNN, which is
an efficient search engine to explore DNN candidates under hardware resource and performance constraints; (2) a DNN-driven top-down FPGA accelerator design, named Auto-HLS, which is a fast board-level design generator to automatically map DNNs onto FPGAs.

5.2.1 The key to co-design: Bundle

Fig. 14 The key to co-design: Bundle – the common basic building block to both DNN design and accelerator design [45].
The key to achieve co-design, i.e., to execute Auto-DNN and Auto-HLS simultaneously, is to propose basic building blocks that can be used to construct both DNNs and their accelerators at the same time. We call such building blocks Bundles, the common building block of both DNN architectures as well as their hardware implementation, as shown in Fig. [4] The benefits of Bundles are two-fold. First, a DNN can be constructed by replicating a bundle for a certain number of layers with pooling layers inserted, which is a common and effective way to construct high-quality DNNs, such as the residual block in ResNet [2], the Inception block in GoogLeNet [20], meanwhile, many NAS approaches follow such cell-based strategy [54, 56, 91]. Second, an accelerator can be constructed by building a hardware module for the certain bundle and reusing it for different DNN layers, given that the DNN is built by replicating the bundle; this can significantly reduce the resource usage of the accelerator by resource sharing and shorten the hardware development cycle. As an example, a Bundle can be a set of DNN layers including: one $3 \times 3$ convolution, one batch normalization, one activation, one $1 \times 1$ convolution, and one activation. Meanwhile, the hardware accelerator will need one instance for the $3 \times 3$ convolution, one instance for the $1 \times 1$ convolution, and so on.

5.2.2 Progressively reducing search space

It is non-trivial to select an optimal Bundle given the large design space and the prohibitively long DNN training time. Therefore, it is essential to narrow down the search space as early as possible. Our approach is in a three-step progressive way, by filtering out unfavourable Bundles at early stage and conducting detailed search at later stage using promising ones. The three steps are as follows.

**Step 1.** Analytical models for performance and resource estimation for bundles and DNNs. Denoting a Bundle as $bund_i$, the resource of $bund_i$ is computed as:

$$Res_{bund_i}^r = \sum_{p_j} Res_{j}^r + \Gamma_{i}^r$$  \hspace{1cm} (6)

where $Res_{j}^r$ is the resource usage of instance $p_j$ of resource type $r$ (including DSP, LUTs, FF and BRAM), $\Gamma_{i}^r$ represents other resource overhead such as LUTs consumed by control logic and multiplexers.

The latency of a Bundle is estimated as:

$$Lat_{bund_i} = \alpha_i \cdot \sum_{p_j} Comp_j + \frac{\beta_i \cdot \Theta(Data_i)}{bw}$$  \hspace{1cm} (7)

where $Comp_j$ is the computation latency of instance $p_j$, and $\Theta(Data_i)$ is the data amount processed by $bund_i$. $bw$ represents the off-chip memory bandwidth. Denote the latency of one execution of $p_j$ as $lat_j$, and the total number of reuses of $p_j$ as $reuse_j$, the computation latency $Comp_j$ is estimated as:

$$Comp_j = \sum_{1 \leq j \leq n} reuse_j \cdot lat_j$$  \hspace{1cm} (8)
can be computed by the input/output dimensions of the data processed by the IP and the data dimensions of $p_j$’s interface. The parameter $\alpha_i$ in Eq. 7 describes how much computation is overlapped because of IP pipelining, and $\beta_i$ describes how much data transfer is overlapped during computations. $\alpha_i$, $\beta_i$, and $\Gamma_i$ will be determined for each $bund_i$ using Auto-HLS sampling.

The overall DNN latency based on $Lat_{bund_i}$ in Eq. 7 is estimated as:

$$Lat_{DNN} = \sum_{i=1}^{N} Lat_{bund} + \phi \cdot Lat_{DM}$$

where $N$ is the number of Bundle repetitions of the DNN, and $\phi \cdot Lat_{DM}$ represents the inter-bundle data movement latency. For overall DNN resource utilization, we have:

$$Res_{DNN} = Res_{bund} + \gamma \cdot Res_{ctl}$$

where $Res_{bund}$ is the resource of $bund_i$, and $Res_{ctl}$ is additional control logic overhead, e.g., finite state machine and multiplexers. $\phi$, $\gamma$, $Lat_{DM}$ and $Res_{ctl}$ will be decided and calibrated through actual hardware synthesis and implementation.

**Step 2.** Bundle evaluation and selection. In this step, we evaluate the latency, resource, and accuracy metrics for each Bundle, as defined in Step 1. Since we cannot evaluate the accuracy for a single Bundle, we replicate a Bundle for $n$ times to build a DNN and train it for a small number of epochs (20 in the experiment). We plot Pareto curves for the Bundles to examine the tradeoff between DNN accuracy and resource utilization, and the Bundles on the Pareto curve will be selected for detailed search in the next step.

**Step 3.** DNN construction using Bundles and training. After selecting top-$N$ promising Bundle candidates, We search DNN models under resource and latency constraints. For each Bundle, $K$ initial DNNs are generated and are progressively updated by adjusting the number of channels, pooling layer positions, etc., until the latency target is met. Then, we perturb the initial DNNs by changing three variables: the number of Bundle replications, down-sampling configurations between bundles, and channel expansion configuration. We adopted Stochastic Coordinate Descent (SCD) algorithm for perturbation, while other heuristic or evolutionary algorithms can be applied as well. The goal of the search algorithm is to find the DNN architecture which meets the performance constraints with highest accuracy.

### 5.2.3 Evaluation results

To evaluate the effectiveness of the co-design framework, we apply it on a low-power object detection competition [99], and compare to the top-3 winners for both FPGA and GPU categories. The results are shown in Table 7. We make comparisons in: (1) the Intersection over Union (IoU); (2) the latency for processing one frame and the overall frame per second (FPS); (3) the board power; (4) the energy consumption for all testing data; and (5) the energy efficiency per frame (J/pic). The results are collected from the board-level implementations on Pynq-Z1. The latency refers to
Table 7 Performance Comparisons (FPGA and GPU competition data are obtained from [99])

| Model | IoU | Latency (ms) | FPS | Power | Energy | Efficiency |
|-------|-----|--------------|-----|-------|--------|------------|
| Ours  |     |              |     |       |        |            |
| DNN1  | 68.6% | 80.0 (100 MHz) | 12.5 | 2.2W  | 8.80 KJ | 0.18 J/pic |
|       | 57.4 (150 MHz) | **17.4** | **2.5W** | **7.18 KJ** | **0.14 J/pic** |
| DNN2  | 61.2% | 62.6 (100 MHz) | 16.0 | 2.2W  | 7.50 KJ | 0.15 J/pic |
|       | 44.1 (150 MHz) | 22.7 | 2.4W  | 5.51 KJ | 0.11 J/pic |
| DNN3  | 59.3% | 47.8 (100 MHz) | 20.9 | 2.2W  | 5.74 KJ | 0.11 J/pic |
|       | 33.7 (150 MHz) | **29.7** | **2.4W** | **4.04 KJ** | **0.08 J/pic** |
| 1st in FPGA SSD | 62.4% | 84.6 (150 MHz) | 11.96 | 4.2W  | 17.56 KJ | 0.35 J/pic |
| 2nd in FPGA – | – | 49.2% | 38.5 (150 MHz) | 25.97 | 2.5W  | 4.81 KJ | 0.10 J/pic |
| 3rd in FPGA – | – | 57.3% | 136.1 (150 MHz) | 7.35 | 2.6W  | 17.69 KJ | 0.35 J/pic |
| 1st in GPU Yolo | 69.8% | 40.7 (854 MHz) | 24.55 | 12.6W | 25.66 KJ | 0.51 J/pic |
| 2nd in GPU Tiny-Yolo | 69.1% | 39.5 (854 MHz) | 25.3 | 13.3W | 26.28 KJ | 0.53 J/pic |
| 3rd in GPU Tiny-Yolo | 68.5% | 42.3 (854 MHz) | 23.64 | 10.3W | 21.79 KJ | 0.44 J/pic |

the execution time for a single frame in millisecond, while FPS is measured using total run-time for the 50K images including image loading, preprocessing, and DNN inference.

Compared to the 1st-place winner of the FPGA category, we achieve 6.2% higher IoU, 40% lower power, and 2.5× better energy efficiency, which we attribute to the effectiveness of an automated co-search instead of manual designs. Compared to GPU-based designs, our DNN1 model is more accurate than the 3rd-place design and only 1.2% lower IoU than the 1st-place GPU design. Regarding the energy efficiency, ours is 3.6× better than the 1st-place GPU design with 40% longer latency despite a nearly 6× slower clock frequency.

5.3 EDD: Efficient Differential DNN Architecture Search

On top of the FPGA/DNN co-design introduced in Sec. 5.2, we further develop co-design to a more generalized and unified approach, i.e., fully simultaneous neural architecture and implementation co-search, targeting arbitrary hardware platforms. Neural architecture and implementation co-search (NAIS) [48] is the first work that stylized design methodology targeting both FPGAs and GPUs, while EDD [58] is a fully simultaneous, efficient differentiable DNN architecture and implementation co-search methodology. The overall architecture of EDD is presented in Fig. 15.

5.3.1 Fused co-design space

The key technology is to fuse the design space of DNN architecture search and hardware implementation search. We collectively denote the variables used in DNN search and implementation search as $A$ and $I$, respectively, and the fused space of co-search is $\{A, I\}$. To carry out both DNN architecture and hardware accelerator co-search in the fused DNN/accelerator space as described in E.5 we minimize the following loss function:
\[
\min : \mathcal{L} = \text{Acc}_{\text{loss}}(A, I) \cdot \text{Per}_{\text{loss}}(I) + \beta \cdot C^{\text{RES}(I)-\text{RES}_{\text{ub}}}
\] (11)

In the above equation, \(\text{Acc}_{\text{loss}}\) is the DNN accuracy loss; \(\text{Per}_{\text{loss}}\) is the hardware performance loss such as end-to-end inference latency, throughput, energy, DNN model complexity, etc.; multiple performance metrics can be optimized simultaneously by defining a single weighted loss. \(\text{RES}\) is the resource utilization and \(\text{RES}_{\text{ub}}\) is resource upper bound. Apparently, \(\text{Acc}_{\text{loss}}\) is a function of \(A\) and \(I\); \(\text{Per}_{\text{loss}}\) and \(\text{RES}\) are functions of \(I\). Resource upper-bound \(\text{RES}_{\text{ub}}\) is expressed in an exponent term to introduce large penalty when being violated. Worth noting, in the existing hardware-aware NAS approaches, only \(A\) is searched while \(I\) is fixed during NAS. In our proposed co-search formulation, \(I\) is variable, and \(A\) and \(I\) are fused as one design space \([A, I]\).

**NAS design space.** In the search space, each DNN is composed of \(N\) basic building blocks in a single-path fashion without branches \([100]\). Inside each block, there are \(M\) candidate operations. We adopt the most commonly used DNN blocks in NAS approaches, called MBConv \([50]\), which is composed of sequential layers of \(\text{conv-1} \times 1, \text{duconv-k} \times k\) and \(\text{conv-1} \times 1\), where \(k\) is the kernel size. Between \(\text{conv-1} \times 1\) and \(\text{duconv-k} \times k\), the number of channels expands/shrinks by a ratio of \(c_{\text{ch}}^m\) for operation \(op^m\). The output of each block is calculated based on the outputs of its \(M\) candidate operations. Specifically, we adopt the Gumbel-Softmax function in \([53]\), where each operation \(op^m\) will be sampled from a sampling parameter \(\theta_{i,m}\) following Gumbel-
Table 8: Comparisons with existing NAS solutions [58].

| Baseline Models       | Test Error (%) | GPU Latency | FPGA Latency |
|-----------------------|----------------|-------------|--------------|
|                       | Top-1 | Top-5 | Titan RTX | ZCU102 | ZCU102 |
| GoogleNet [103]       | 30.22 | 10.47 | 27.75 ms | NA    | NA    |
| MobileNet-V2 [103]    | 28.1  | 9.7   | 17.87 ms | 10.85 ms|
| ShuffleNet-V2 [104]   | 30.6  | 11.7  | 21.91 ms | NA    | NA    |
| ResNet18              | 30.2  | 10.9  | 9.71 ms  | 10.15 ms|
| Hardware-aware NAS Models |      |        |           |        |        |
| MnasNet-A1 [56]       | 24.8  | 7.5   | 17.94 ms | 8.78 ms|
| FBNet-C [55]          | 24.9  | 7.6   | 22.54 ms | 12.21 ms|
| Proxyless-cpu [105]   | 24.7  | 7.6   | 21.34 ms | 10.81 ms|
| Proxyless-Mobile [105]| 25.4  | 7.8   | 21.23 ms | 10.78 ms|
| Proxyless-gpu [105]   | 24.9  | 7.5   | 15.72 ms | 10.79 ms|
| EDD-Net-1             | 25.3  | 7.7   | 11.17 ms | 11.15 ms|
| EDD-Net-2             | 25.4  | 7.9   | 13.00 ms | 7.96 ms |

Softmax distribution, which converts the discrete non-differentiable sampling to continuous differentiable sampling. The sampled operations form a complete DNN, which can be evaluated for accuracy and implementation performance.

**Implementation search space** We let each candidate operation \( o_p^m \) has its own implementation variables, forming an implementation search space \( I^m \). The primary implementation variable is quantization \( q \), i.e., data precision, since it has a large impact on DNN accuracy, implementation performance and hardware resource. Rather than using a train-and-quantize approach, the quantization shall be searched together with DNN structure to provide implementation performance feedback. Besides quantization, other implementation variables can also be integrated into the framework, such as accelerator parallelism, loop tiling factors, batch size, etc.

### 5.3.2 Differentiable performance and resource formulation

The key technology is how to formulate the loss function differentiable with respect to the search space \( A \) and \( I \). Since NAS search space \( A \) is discrete, differentiable formulation requires continuous relaxation. DARTS [91] is the first work that uses softmax for relaxation, while FBNet uses Gumbel-softmax [101] by sampling from the discrete space. Such relaxation has been demonstrated to be GPU-hours efficient with appealing model accuracy [91, 55, 93]. Motivated by FBNet, a similar technique using Gumbel-softmax can be applied to differentiable implementation \( I \) to convert the discrete implementation search space into continuous. Therefore, by descending the loss function on validation set, \( (A, I) \) can be learned simultaneously.

### 5.3.3 State-of-the-art results

We demonstrate the results on a subset of ImageNet dataset randomly sampled from 100 classes and target three hardware architectures, each with a searched DNN
model, called EDD-Net: (1) low-latency oriented GPU (EDD-Net-1); (2) folded FPGA architecture (EDD-Net-2), where a single processing element (PE) will be reused by all layers; (3) pipelined FPGA architecture (EDD-Net-3), where each layer has its own PE, and all PEs work simultaneously. Each model is produced through EDD within a 12-hour search on a P100 GPU.

For GPU-targeted EDD-Net-1, the results are as shown in Table 8, where the GPU latency is tested on Titan RTX. It shows that EDD-Net-1 reaches similar or better accuracy comparing with the state-of-the-art DNN models and other NAS approaches while achieving the shortest inference latency. Table 9 shows the accuracy and latency tradeoff of different precisions of EDD-Net-1 on Nvidia 1080 Ti GPU.

For FPGA-targeted EDD-Net-2, the latency values are collected by running DNN models with CHaiDNN accelerators on ZCU102 FPGA as shown in Table 8. It shows that EDD-Net-2 delivers the shortest latency on FPGA among all the DNNs. FPGA-targeted EDD-Net-3 is searched targeting a pipelined FPGA accelerator. As shown in Table 10, EDD-Net-3 achieves higher throughput with a much higher accuracy comparing with the state-of-the-art.

### 6 Conclusion

Emerging DNN-based AI applications are challenging for embedded systems as these applications come with high computation and memory demands as well as diverse application-specific requirements, such as real-time responses, high-throughput performance, and reliable inference accuracy. This chapter introduced a series of effective design methods to overcome these challenges to enable embedded AI solutions. These methods can be categorized into efficient machine learning algorithms, accelerator and compiler designs, and various co-design and optimization strategies. We first proposed ELB-NN and VecQ to strengthen the AI model’s hardware efficiency by enabling extremely low bit-width quantization during model training and inference. Then, we proposed DNNBuilder and PyLog for customized hardware accelerator design and DNN workload mapping to such accelerators. At last, we introduced efficient co-design strategies, including FPGA/DNN co-design and EDD, when deploying AI workloads on embedded systems.
We believe embedded AI solutions will involve more effective and comprehensive design methods in the future, covering AI algorithms, customized accelerators, and co-design and co-optimization strategies between algorithm and hardware. For example, our efficient AI algorithm designs, such as ELB-NN and VecQ, can adopt more advanced quantization schemes to minimize network compression loss. Future works will consider more diverse network architecture and layer-wise data distribution features. To facilitate a smoother accelerator design process, we will extend DNNBuilder and PyLog to create frameworks and tools for hardware design, synthesis, and workload compilation. Major directions include 1) heterogeneous computing support, which intends to enable system-level design and optimization for heterogeneous AI systems, and 2) dynamic computational graph scheduling, which enables the generation of runtime adaptive accelerators for future AI applications. Our future works will also cover more advanced software/hardware co-design for emerging AI models running on heterogeneous systems, which contains a much larger design space and is thus more challenging. For example, multi-modal multi-task (MMMT) models and customized hardware designs working for autonomous driving have demonstrated the importance of heterogeneity in AI model and hardware designs. The co-design and co-optimization methods must be developed for such heterogeneous scenarios.

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References

1. Yann LeCun, Yoshua Bengio, and Geoffrey Hinton. Deep learning. *Nature*, 521(7553):436–444, 2015.
2. Kaiming He, Xiangyu Zhang, Shaoqing Ren, et al. Deep residual learning for image recognition. In *IEEE Conf. Comput. Vis. Pattern Recog.*, 2016.
3. Ashish Vaswani, Noam Shazeer, Niki Parmar, et al. Attention is all you need. In *Neural Inform. Process. Syst.*, 2017.
4. Stephen Lombardi, Jason Saragih, Tomas Simon, and Yaser Sheikh. Deep appearance models for face rendering. *ACM Trans. Graph.*, 37(4):1–13, 2018.
5. Alex Krizhevsky, Ilya Sutskever, and Geoffrey E Hinton. Imagenet classification with deep convolutional neural networks. *Neural Inform. Process. Syst.*, 25, 2012.
6. David Silver, Julian Schrittwieser, Karen Simonyan, Ioannis Antonoglou, Aja Huang, Arthur Guez, Thomas Hubert, Lucas Baker, Matthew Lai, Adrian Bolton, et al. Mastering the game of go without human knowledge. *Nature*, 550(7676):354–359, 2017.
7. OpenAI. AI and compute. 2018.
8. Shengkui Zhao, Saima Ahmed, Yun Liang, et al. A real-time 3d sound localization system with miniature microphone array for virtual reality. In *Conf. Industrial Electronics and Applications*, 2012.
9. Deming Chen, Jason Cong, Swathi Gurumani, et al. Platform choices and design demands for iot platforms: cost, power, and performance tradeoffs. *IET Cyber-Physical Syst.: Theory & Applications*, 1(1):70–77, 2016.

10. Norman P Jouppi et al. In-datacenter performance analysis of a tensor processing unit. In *Int. Symp. Comput. Architecture*, 2017.

11. Mohammad Rastegari, Vicente Ordonez, Joseph Redmon, and Ali Farhadi. Xnor-net: Image-net classification using binary convolutional neural networks. In *Eur. Conf. Comput. Vis.*. pages 525–542. Springer, 2016.

12. Junsong Wang, Qiuwen Lou, Xiaofan Zhang, Chao Zhu, Yonghua Lin, and Deming Chen. Design flow of accelerating hybrid extremely low bit-width neural network in embedded FPGA. In *Int. Conf. Field Programmable Logic and Applications*, pages 163–1636. IEEE, 2018.

13. Dibakar Gope et al. Ternary hybrid neural-tree networks for highly constrained iot applications. In *Conf. Machine Learning Syst.*, 2019.

14. Cheng Gong, Yao Chen, Ye Lu, Tao Li, Cong Hao, and Deming Chen. Vecq: Minimal loss dnn model compression with vectorized weight quantization. *IEEE Trans. Comput.*, 2020.

15. Yao Han et al. T-DLA: An open-source deep learning accelerator for ternarized DNN models on embedded FPGA. In *IEEE Comput. Society Annual Symp. VLSI*, 2019.

16. Song Han et al. Learning both weights and connections for efficient neural network. In *Neural Inform. Process. Syst.*, 2015.

17. Song Han et al. Deep compression: Compressing deep neural networks with pruning, trained quantization and huffman coding. In *Int. Conf. Learn. Represent.*, 2016.

18. Jian-Hao Luo et al. Thinlet: A filter level pruning method for deep neural network compression. In *Int. Conf. Comput. Vis.*, 2017.

19. Karen Simonyan and Andrew Zisserman. Very deep convolutional networks for large-scale image recognition. *arXiv preprint arXiv:1409.1556*, 2014.

20. Christian Szegedy, Wei Liu, Yangqing Jia, et al. Going deeper with convolutions. In *IEEE Conf. Comput. Vis. Pattern Recog.*, 2015.

21. Xiaoliang Dai et al. Nest: A neural network synthesis tool based on a grow-and-prune paradigm. *IEEE Trans. Comput.*, 68(10):1487–1497, 2019.

22. Ao Ren et al. ADMM-NN: An algorithm-hardware co-design framework of dnns using alternating direction methods of multipliers. In *Int. Conf. Architectural Support for Programming Languages and Operating Syst.*, 2019.

23. Xiaohan Ding et al. Auto-balanced filter pruning for efficient convolutional neural networks. In *AAAI*, 2018.

24. Andrew G Howard, Menglong Zhu, Bo Chen, Dmitry Kalenichenko, Weijun Wang, Tobias Weyand, Marco Andreetto, and Hartwig Adam. Mobilenets: Efficient convolutional neural networks for mobile vision applications. *arXiv preprint arXiv:1704.04861*, 2017.

25. Manoj Alwani et al. Fused-layer CNN accelerators. In *Int. Symp. Microarchitecture*, 2016.

26. Bryan Brown. Intel® math kernel library for deep learning networks. 2018.

27. Dustin Franklin. NVIDIA Jetson AGX Xavier delivers 32 tera ops for new era of AI in robotics. *NVIDIA Accelerated Computing| Parallel For all*, 2018.

28. Chen Zhang et al. Optimizing FPGA-based accelerator design for deep convolutional neural networks. In *Int. Symp. FPGAs*, 2015.

29. Jian Tao Qu et al. Going deeper with embedded FPGA platform for convolutional neural network. In *Int. Symp. FPGAs*, 2016.

30. Xiaofan Zhang, Junsong Wang, Chao Zhu, Yonghua Lin, Jinjun Xiong, Wen-mei Hwu, and Deming Chen. DNNBuilder: An automated tool for building high-performance DNN hardware accelerators for FPGAs. In *Int. Conf. Comput. Aided Design*, pages 1–8. IEEE, 2018.

31. Yu-Hsin Chen et al. Eyeriss: An energy-efficient reconfigurable accelerator for deep convolutional neural networks. In *Int. Solid-State Circuits Conf.*, 2016.

32. Song Han, Xingyu Liu, Huizi Mao, Jing Pu, Ardavan Pedram, Mark A Horowitz, and William J Dally. ElIE: Efficient inference engine on compressed deep neural network. In *Int. Symp. Comput. Architecture*, 2016.
33. Alexandros Papakonstantinou, Karthik Gururaj, John A Stratton, et al. FCUDA: Enabling efficient compilation of CUDA kernels onto FPGAs. In Symp. Application Specific Processors, 2009.

34. Kyle Rupnow, Yun Liang, Yinan Li, et al. A study of high-level synthesis: Promises and challenges. In Int. Conf. ASIC, 2011.

35. Xinliang Liu, Yao Chen, Tan Nguyen, et al. High level synthesis of complex applications: An H. 264 video decoder. In Int. Symp. FPGAs, 2016.

36. Chen Zhang et al. Caffeine: Toward uniformed representation and acceleration for deep convolutional neural networks. IEEE Trans. Comput. Aided Design of Integrated Circuits and Syst., 38(11):2072–2085, 2018.

37. Hanchen Ye, Xiaofan Zhang, Zhize Huang, Gengsheng Chen, and Deming Chen. Hybridnn: A framework for high-performance hybrid dnn accelerator design and implementation. In Design Automation Conf., pages 1–6. IEEE, 2020.

38. Sitao Huang, Kun Wu, Hyunmin Jeong, Chengyue Wang, Deming Chen, and Wen-Mei Hwu. PyLog: An algorithm-centric Python-based FPGA programming and synthesis flow. IEEE Trans. Comput., 70(12):2015–2028, 2021.

39. Yangqing Jia et al. Caffe: Convolutional architecture for fast feature embedding. In ACM Int. Conf. Multimedia, 2014.

40. Martin Abadi et al. Tensorflow: A system for large-scale machine learning. In USENIX Symp. OSDI, 2016.

41. Adam Paszke, et al. Pytorch: An imperative style, high-performance deep learning library. In Neural Inform. Process. Syst., 2019.

42. Cong Hao, Jordan Dotzel, Jinjun Xiong, Luca Benini, Zhiru Zhang, and Deming Chen. Enabling design methodologies and future trends for edge ai: specialization and codesign. IEEE Design & Test, 38(4):7–26, 2021.

43. Cong Hao and Deming Chen. Deep neural network model and fpga accelerator co-design: Opportunities and challenges. In Int. Conf. Solid-State and Integrated Circuit Technol., pages 1–4. IEEE, 2018.

44. Xiaofan Zhang, Haoming Lu, Cong Hao, Jiachen Li, Bowen Cheng, Yuhong Li, Kyle Rupnow, Jinjun Xiong, Thomas Huang, Honghui Shi, et al. Skynet: a hardware-efficient method for object detection and tracking on embedded systems. Conf. Machine Learning Syst., pages 216–229, 2020.

45. Cong Hao, Xiaofan Zhang, Yuhong Li, Sitao Huang, Jinjun Xiong, Kyle Rupnow, Wen-mei Hwu, and Deming Chen. Fpga/dnn co-design: An efficient design methodology for 1ot intelligence on the edge. In Design Automation Conf., pages 1–6. IEEE, 2019.

46. Yifan Yang, Qijing Huang, Bichen Wu, et al. Synetgy: Algorithm-hardware co-design for convnet accelerators on embedded fpgas. In Int. Symp. FPGAs, 2019.

47. Kaiyuan Guo, Shulin Zeng, Jincheng Yu, Yu Wang, and Huazhong Yang. A survey of fpga-based neural network inference accelerators. ACM Trans. Reconfigurable Technol. and Syst., 12(1):1–26, 2019.

48. Cong Hao, Yao Chen, Xinheng Liu, Atif Sarwari, Daryl Sew, Ashutosh Dhar, Bryan Wu, Dongdong Fu, Jinjun Xiong, Wen-mei Hwu, et al. NAIS: Neural architecture and implementation search and its applications in autonomous driving. arXiv preprint arXiv:1911.07446, 2019.

49. Weiwen Jiang, Lei Yang, Edwin H-M Sha, Qingfeng Zhuge, Shouzhen Gu, Sakyasingha Dasgupta, Yiyu Shi, and Jingtong Hu. Hardware/software co-exploration of neural architectures. IEEE Trans. Comput. Aided Design of Integrated Circuits and Syst., 2020.

50. Junsong Wang, Xiaofan Zhang, Yubo Li, et al. Exploring HW/SW co-optimizations for accelerating large-scale texture identification on distributed GPUs. In Int. Conf. on Parallel Processing, pages 1–10, 2021.

51. Xiaofan Zhang, Yuan Ma, Jinjun Xiong, et al. Exploring HW/SW co-design for video analysis on CPU-FPGA heterogeneous systems. IEEE Trans. Comput. Aided Design of Integrated Circuits and Syst., 2021.

52. Yonggan Fu, Yongan Zhang, Chaojian Li, et al. A3C-S: Automated agent accelerator co-search towards efficient deep reinforcement learning. In Design Automation Conf., 2021.
53. Thomas Elsken, Jan Hendrik Metzen, and Frank Hutter. Neural architecture search: A survey. *The Journal of Machine Learning Research*, 20(1):1997–2017, 2019.

54. Barret Zoph, Vijay Vasudevan, Jonathon Shlens, and Quoc V Le. Learning transferable architectures for scalable image recognition. In *IEEE Conf. Comput. Vis. Pattern Recog.*, pages 8697–8710, 2018.

55. Bichen Wu, Xiaoliang Dai, Peizhao Zhang, Yanghan Wang, Fei Sun, Yiming Wu, Yuandong Tian, Peter Vajda, Yangqing Jia, and Kurt Keutzer. Fbnet: Hardware-aware efficient convnet design via differentiable neural architecture search. In *IEEE Conf. Comput. Vis. Pattern Recog.*, pages 10734–10742, 2019.

56. Mingxing Tan, Bo Chen, Ruoming Pang, Vijay Vasudevan, Mark Sandler, Andrew Howard, and Quoc V Le. Mnasnet: Platform-aware neural architecture search for mobile. In *IEEE Conf. Comput. Vis. Pattern Recog.*, pages 2820–2828, 2019.

57. Weiwen Jiang, Xinyi Zhang, Edwin H-M Sha, Lei Yang, Qingfeng Zhuge, Yiyu Shi, and Jingtong Hu. Accuracy vs. efficiency: Achieving both through fpga-implementation aware neural architecture search. In *Design Automation Conf.*, pages 1–6, 2019.

58. Yuhong Li, Cong Hao, Xiaofan Zhang, Xinheng Liu, Yao Chen, Jinjun Xiong, Wen-mei Hwu, and Deming Chen. Edd: Efficient differentiable dnn architecture and implementation co-search for embedded ai solutions. *Design Automation Conf.*, 2020.

59. Lei Yang, Zheyu Yan, Meng Li, Hyouthun Kwon, Liangzhen Lai, Tushar Krishna, Vikas Chandra, Weiwen Jiang, and Yiyi Shi. Co-exploration of neural architectures and heterogeneous asic accelerator designs targeting multiple tasks. *Design Automation Conf.*, 2020.

60. Xiaolong Ma, Fu-Ming Guo, Wei Niu, Xue Lin, Jian Tang, Kaisheng Ma, Bin Ren, and Yanzhi Wang. Pconv: The missing but desirable sparsity in dnn weight pruning for real-time execution on mobile devices. In *AAAI*, pages 5117–5124, 2020.

61. Wei Niu, Xiaolong Ma, Sheng Lin, Shihao Wang, Xuehai Qian, Xue Lin, Yanzhi Wang, and Bin Ren. Patdnn: Achieving real-time dnn execution on mobile devices with pattern-based weight pruning. In *Int. Conf. Architectural Support for Programming Languages and Operating Syst.*, pages 907–922, 2020.

62. Shaoqian Liu, Bin Ren, Xipeng Shen, and Yanzhi Wang. Cocopie: Making mobile ai sweet as pie—compression-compilation co-design goes a long way. *Communications of ACM*, 2020.

63. Ji Lin, Wei-Ming Chen, John Cohn, Chuang Gan, and Song Han. Mecnet: Tiny deep learning on ioi devices. In *Neural Inform. Process. Syst.*, 2020.

64. PULP - An Open Parallel Ultra-Low-Power Processing-Platform. [http://iis-projects.ee.ethz.ch/index.php/PULP](http://iis-projects.ee.ethz.ch/index.php/PULP).

65. Angelo Garofalo, Giuseppe Tagliavini, Francesco Conti, Davide Rossi, and Luca Benini. Xpulpnn: accelerating quantized neural networks on risc-v processors through isa extensions. In *Design, Automation & Test in Euro. Conf. & Exhibition*, pages 186–191. IEEE, 2020.

66. Angelo Garofalo, Manuele Rusci, Francesco Conti, Davide Rossi, and Luca Benini. PULPNN: accelerating quantized neural networks on parallel ultra-low-power risc-v processors. *Philosophical Trans. the Royal Society A*, 378(2164):20190155, 2020.

67. Fengfu Li, Bo Zhang, and Bin Liu. Ternary weight networks. *arXiv preprint arXiv:1605.04711*, 2016.

68. Shuchang Zhou, Yuxin Wu, Zekun Ni, Xinyu Zhou, He Wen, and Yuheng Zou. Dorefa-net: Training low bitwidth convolutional neural networks with low bitwidth gradients. *arXiv preprint arXiv:1606.06160*, 2016.

69. Richie Zhao, Weinan Song, Wentao Zhang, Tianwei Xing, Jeng-Hau Lin, Mani Srivastava, Rajesh Gupta, and Zhiru Zhang. Accelerating binarized convolutional neural networks with software-programmable FPGAs. In *Int. Symp. FPGAs*, pages 15–24, 2017.

70. Y. Umuroglu et al. Finn: A framework for fast, scalable binarized neural network inference. In *Int. Symp. FPGAs*. ACM, 2017.

71. N. Eriko et al. Accelerating binarized neural networks: Comparison of FPGA, CPU, GPU, and ASIC. In *Int. Conf. Field-Programmable Technol.*, 2016.

72. Iuy Hubara, Matthieu Courbariaux, Daniel Soudry, Ran El-Yaniv, and Yoshua Bengio. Binarized neural networks. In *Neural Inform. Process. Syst.*, pages 4107–4115, 2016.
73. Matthieu Courbariaux, Yoshua Bengio, and Jean-Pierre David. Binaryconnect: Training deep neural networks with binary weights during propagations. In Neural Inform. Process. Syst., pages 3123–3131, 2015.

74. Zhouhan Lin, Matthieu Courbariaux, Roland Memisevic, and Yoshua Bengio. Neural networks with few multiplications. In Int. Conf. Learn. Represent., 2016.

75. Canran Jin, Heming Sun, and Shinji Kimura. Sparse ternary connect: Convolutional neural networks using ternarized weights with enhanced sparsity. In Asia and South Pacific Design Automation Conf., pages 190–195, 2018.

76. Sergey Ioffe and Christian Szegedy. Batch normalization: Accelerating deep network training by reducing internal covariate shift. In Int. Conf. Machine Learning, pages 448–456, 2015.

77. Chenzhuo Zhu, Song Han, Huizi Mao, and William J Dally. Trained ternary quantization. In Int. Conf. Learn. Represent., 2017.

78. Peisong Wang, Qinghao Hu, Yifan Zhang, Chunjie Zhang, Yang Liu, and Jian Cheng. Two-step quantization for low-bit neural networks. In IEEE Conf. Comput. Vis. Pattern Recog., pages 4376–4384, 2018.

79. Aojun Zhou, Anbang Yao, Yiwen Guo, Lin Xu, and Yurong Chen. Incremental network quantization: Towards lossless cnns with low-precision weights. In Int. Conf. Learn. Represent., 2017.

80. Cong Leng, Zesheng Dou, Hao Li, Shenghuo Zhu, and Rong Jin. Extremely low bit neural network: Squeeze the last bit out with admm. In AAAI, 2018.

81. Joseph Redmon and Ali Farhadi. Yolo9000: better, faster, stronger. In IEEE Conf. Comput. Vis. Pattern Recog., 2017.

82. Qingcheng Xiao et al. Exploring heterogeneous algorithms for accelerating deep convolutional neural networks on FPGAs. In Design Automation Conf., 2017.

83. Dustin Franklin. NVIDIA Jetson TX2 delivers twice the intelligence to the edge. NVIDIA Accelerated Computing| Parallel For all, 2017.

84. PYNQ. http://www.pynq.io/.

85. Yi-Hsiang Lai, Yuze Chi, Yuwei Hu, Jie Wang, Cody Hao Yu, Yuan Zhou, Jason Cong, and Zhiru Zhang. HeteroCL: A multi-paradigm programming infrastructure for software-defined reconfigurable computing. In Int. Symp. FPGAs, pages 242–251, 2019.

86. George Kyriakides and Konstantinos Margaritis. An introduction to neural architecture search for convolutional networks. arXiv preprint arXiv:1805.03648, 2018.

87. Barret Zoph and Quoc V Le. Neural architecture search with reinforcement learning. arXiv preprint arXiv:1611.01578, 2016.

88. Bowen Baker, Otkrist Gupta, Nikhil Naik, and Ramesh Raskar. Designing neural network architectures using reinforcement learning. arXiv preprint arXiv:1611.02167, 2016.

89. Yiyang Zhao, Linnan Wang, Yuandong Tian, Rodrigo Fonseca, and Tian Guo. Few-shot neural architecture search via regression. Neural Inform. Process. Syst., 34, 2021.

90. Hongyang Li, David Eigen, Samuel Dodge, Matthew Zeiler, and Xiaogang Wang. Finding task-relevant features for few-shot learning by category traversal. In IEEE Conf. Comput. Vis. Pattern Recog., pages 1–10, 2019.
97. Hadjer Benmeziane, Kaoutar El Maghraoui, Hamza Ouarnoughi, Smail Niar, Martin Wistuba, and Naigang Wang. A comprehensive survey on hardware-aware neural architecture search. arXiv preprint arXiv:2101.09336, 2021.
98. Han Cai, Chuang Gan, Tianzhe Wang, Zhekai Zhang, and Song Han. Once-for-all: Train one network and specialize it for efficient deployment. arXiv preprint arXiv:1908.09791, 2019.
99. Xiaowei Xu et al. DAC-SDC low power object detection challenge for UAV applications. arXiv:1809.00110, 2018.
100. Dimitrios Stamoulis, Ruizhou Ding, Di Wang, Dimitrios Lymberopoulos, Bodhi Priyantha, Jie Liu, and Diana Marculescu. Single-path nas: Device-aware efficient convnet design. arXiv preprint arXiv:1905.04159, 2019.
101. Eric Jang, Shixiang Gu, and Ben Poole. Categorical reparameterization with gumbel-softmax. arXiv preprint arXiv:1611.01144, 2016.
102. CHaiDNN. [https://github.com/Xilinx/CHaiDNN].
103. Mark Sandler, Andrew Howard, Menglong Zhu, Andrey Zhmoginov, and Liang-Chieh Chen. Mobilenetv2: Inverted residuals and linear bottlenecks. In IEEE Conf. Comput. Vis. Pattern Recog., pages 4510–4520, 2018.
104. Ningning Ma, Xiangyu Zhang, Hai-Tao Zheng, and Jian Sun. Shufflenet v2: Practical guidelines for efficient cnn architecture design. In Eur. Conf. Comput. Vis., pages 116–131, 2018.
105. Han Cai, Ligeng Zhu, and Song Han. Proxylessnas: Direct neural architecture search on target task and hardware. arXiv preprint arXiv:1812.00332, 2018.
106. Cong Hao and Deming Chen. Software/hardware co-design for multi-modal multi-task learning in autonomous systems. In Int. Conf. Artificial Intelligence Circuits and Syst., pages 1–5. IEEE, 2021.
107. Emil Talpes, Debjit Das Sarma, Ganesh Venkataramanan, Peter Bannon, Bill McGee, Benjamin Floering, Ankit Jalote, Christopher Hsiong, Sahil Arora, Atchuthy Gorti, et al. Compute solution for tesla’s full self-driving computer. Micro, 40(2):25–35, 2020.