A non-isolated high step-up DC–DC converter using magnetic coupling and voltage multiplier circuit

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Abstract
This paper introduces a new DC–DC structure with a high voltage gain. The proposed structure can achieve higher voltage gain by using magnetic coupling and voltage multiplier circuit (VMC). The VMC is also used as a clamp circuit to suppress the voltage spike through the switch which leads to increase the overall system efficiency. Moreover, the peak voltage through the semiconductors of the proposed converter is low. The existence of soft-switching such as zero-current switching (ZCS) in OFF-state and zero-voltage switching (ZVS) in ON-state of diodes is another merit of the proposed converter. The recommended structure uses one power MOSFET with low on-state resistance ($R_{DS-ON}$) that leads to decrease the conduction loss. For demonstrating the proficiency of the proposed structure, technical analysis, mathematical survey, and comparison results with other similar previous structures are carried out. Finally, laboratory results with 200 W output power and 50 kHz switching frequency are provided, which prove the usefulness of the suggested converter. The proposed converter's efficiency in 200 W output power is 96.98%. Also, the voltage gain, maximum voltage stress across the power switch and diodes for $n$ (turn-ratio) = 2 and $D$ (duty-cycle) = 0.6 are equal to 10, 0.25, and 0.75, respectively.

1 | INTRODUCTION

The photovoltaic source is one of the most significant energy systems in the world and by 2040 will have the largest contribution of electricity generation among all renewable energy candidates. Because this energy is a renewable electricity generation technology with no emission of venomous gasses and has high performance [1–3]. PV power plant is an effective method to obtain energy from the sun and directly convert it to electrical form. Unfortunately, the PV panels’ voltage level is very low, and for high voltage applications, these panels should be connected in series and parallel configurations. Consequently, with this procedure, the PV power systems’ cost is increased [4, 5]. High step-up DC–DC converters can be used to reduce the system’s cost and enhance the voltage level of the PV panels [6–8]. Also, the input current ripple of the converter should be low to reduce the oscillation of the PV panel’s output power. The low input current ripple can increase the lifetime of the PV panel.

On the other hand, the PV panels have low efficiency. Thus, to enhance the PV system efficiency, a high-efficiency DC–DC converter should be used. In the conventional high step-up DC–DC converters such as PWM boost converter, the duty cycle of switches should be notably increased to achieve a high voltage gain, which increases the power losses and decreases the efficiency of the converter. Also, the voltage stress of the switch in the conventional boost converter is equal to the output voltage [9–11]. In order to overcome the above-mentioned drawbacks of the conventional boost converter, many high step-up topologies were presented. There are numerous types of high step-up DC–DC converters, which can be categorised in non-isolated/isolated, bidirectional/unidirectional, the voltage fed/current fed, and hard switched/soft switched classes [12, 13]. Non-isolated step-up converters can be implemented with low cost and elements. But in isolated converters, high volume and cost transformers should be used. Accordingly, the non-isolated high step-up converters have lower volume and price.
than the isolated converters [14, 15]. Usually, common ground between input and output ports is obtained in non-isolated converters. This advantage leads to reduce the Electromagnetic interference (EMI) effects. On the other hand, in these topologies, the coupled inductor can enhance the voltage gain by changing its turn ratio number. Also, by using a coupled inductor, one core can be used for two windings which lead to reduce converter volume. There are other methods for voltage boosting such as a switched inductor, voltage multiplier, and switched capacitors [16, 17]. In order to improve the operation of the high step-up converters in terms of voltage gain and efficiency, many structures have been presented in the literature. In [18], a high step-up DC–DC converter with the coupled inductor and switched capacitor has been presented. By using switched inductor, a non-isolated buck-boost converter was reported in [19], which the input current ripple of the converter was very high. In [20], to reduce the input current ripple, a non-isolated bidirectional DC–DC converter has been represented, which has the capability of (ZVS), but this converter suffers from low voltage gain and low efficiency in the high power range. By using coupled inductor and voltage lifting cells, an improved boost DC–DC converter was suggested in [21]. This structure has some disadvantages such as high voltage stress on diodes and low efficiency even in mediocre output power rate. In [22], integrated autotransformer and coupled inductor was used to enhance the voltage boosting. This converter operates in discontinuous conduction mode (DCM). As a result, this converter is not suitable for PV and fuel cell applications. An interleaved step-up DC–DC converter has been suggested in [23], which uses two coupled inductors. Although it has high voltage gain, but the voltage stress on diodes is very high. Also, the high number of semiconductors is used in this structure, which leads to increase the cost and volume of the converter. By using coupled inductor and voltage multiplier cell, a modified SEPIC converter has been represented in [24]. The benefit of this converter is high voltage gain with low voltage stress across semiconductors and its disadvantage is low efficiency in all load power ranges. In [25], high step-up converters have been reported based on voltage multiplier cells, which used a large number of elements in its structure. Consequently, these topologies suffer from high cost and low efficiency. The proposed converter in [26] use three capacitors clamp circuit to reduce the voltage stress across power switch. Also, coupled inductor is used to increase the voltage gain. In [27], an isolated DC–DC converter is proposed with soft switching feature. However, in this topology two high volume transformer is used, which increases the volume of the converter. An interleaved boost converter with VMC and coupled inductors is proposed in [28]. This topology is suitable for renewable applications such as PV and fuel cell. However, it suffers from lack of common ground between input and output ports. In [29], using asymmetric coupled inductor and VMC a high step-up DC–DC converter is suggested with high efficiency, low voltage stress across semiconductors, low input current ripple and soft switching, and common ground features. Also, dynamic analysis and output voltage controller design in provided in [29]. A step-up converter using dual cross-coupled inductors and VMC is proposed in [30] for electric vehicles. This structure benefits from ultra-high voltage gain with reduced voltage stress across semiconductors and low components count, where only one magnetic core is used. Also, parallel connection of the input port provides a low input current ripple. But lack of common ground is the disadvantage of this topology. A non-isolated high step-up converter using coupled inductor and VMC is proposed in [31]. This topology benefits from high voltage gain. But it has a high input current ripple and high number of components. In [32], analysis and control of a step-up converter with winding cross-coupled inductor technique is presented for DC microgrid applications. This converter has ultra-large gain with low voltage stress across semiconductors. The used passive clamp circuit recycle the leakage energy. The main drawback of this structure is high number of power diodes and capacitors. A trans-inverse coupled inductor-based semi SEPIC converter is proposed in [33]. Wide control rage, continuous input source current are the main benefits of this topology. But it has a low voltage gain than the other similar converters. In [34], a novel soft-switched converter with high voltage gain, recycled leakage energy, and reduced voltage stress across switches and diodes. However, it has higher input current ripple. Using three winding coupled inductor and VMC, a single switch ultra-high step-up DC–DC converter is proposed in [35]. Low reverse recovery of diodes, low operating duty cycle, and high efficiency are the main benefits of this topology. But it suffers from high input current ripple and for solving this problem a RC low pass filter is used.

In this paper, a novel structure of non-isolated DC–DC converter with high voltage conversion ratio and high efficiency is introduced with the following specifications:

- The input current is continuous, which leads to increase the input source's lifetime.
- The output voltage rate of the proposed converter can be increased by selecting the proper turn ratio of the coupled inductor.
- VMC technique has been utilised for further improving the voltage gain. Moreover, the nominal peak voltage throughout the semiconductors is decreased by considering the VMC as a snubber circuit.
- Less number of active and passive elements such as inductors and semiconductors are utilised in the presented structure.
- The zero-current switching (ZCS) in OFF-state and the zero-voltage switching (ZVS) in ON-state of the diodes are other advantages of the suggested converter which improve the efficiency of the proposed structure by decreasing diodes reverse recovery losses.

Thus, due to the above-mentioned features, the presented converter has a useful structure and can be used in renewable energy applications with high efficiency.

In Section 2 the operation analysis of the proposed structure has been carried out. Section 3 presents the steady state analysis of the suggested converter. Section 4 explains the design considerations of the components. In Section 5 the efficiency analysis has been carried out. Section 6 proposes the comparison study. The dynamic model and controller method of the
proposed paper has been presented in Section 7. Section 8 indicates the experimental results of the suggested converter. Finally, Section 9 presents the conclusion of the proposed paper.

2 | OPERATIONAL ANALYSIS OF THE PROPOSED STRUCTURE

The equivalent power circuit and time waveforms of the suggested DC–DC converter are illustrated in Figures 1 and 2, respectively.

The proposed structure includes an input inductor \( L_{in} \), a power switch \( S \), a coupled inductor (CL), four capacitors \( (C_1, C_2, C_3 \) and \( C_o) \) and three diodes \( (D_1, D_2 \) and \( D_o) \). \( C_3 \) is a passive clamp capacitor, which suppresses the peak voltage across the switch \( S \). Diodes \( D_1 \) and \( D_2 \) with \( C_3 \) are elements of VMC. The VMC enhances the voltage gain and decreases the passing current from the power switch. It is located on the secondary side of the CL and provides a high voltage gain without needs to increase the CL turns ratio. Furthermore, to simplify the steady-state analysis of the suggested converter, six assumptions are considered as follows:

1. The proposed high step-up structure operates in continuous conduction mode (CCM).
2. All semiconductor elements \( (S, D_1, D_2 \) and \( D_o) \) are ideal.
3. Capacitors are sufficiently large. \( S \_o \) the voltages across them are constant pending switching period \( (T_s) \).
4. Line is large enough and the input current can be ignored.
5. The CL is modelled as an ideal type transformer, which has a turns ratio \( n = n_2 / n_1 \), leakage \( (L_k) \), and magnetising \( (L_m) \) inductors.
6. The voltage of the first side of the coupled inductor \( (V'_{in}) \) and the voltage of the magnetising inductor \( (VLm) \) are same.

Figure 2 shows the current and voltage waveforms of the presented converter components during one switching cycle. In one switching cycle, five operation modes are attained as shown in Figure 3.

Mode 1 \( [t_0 < t < t_1] \): This interval is a transition mode. At \( t = t_0 \), switch \( S \) is turned ON. \( L_{in} \) obtains energy from the input source \( (V_{in}) \). \( S_o \) its current is linearly increased. Diodes \( D_1 \) and \( D_2 \) are reverse biased, but diode \( D_o \) is turned ON. The energy of CL is passing from the secondary side of CL to output through diode \( D_o \). Also, \( C_3 \) is charged by using input inductor \( L_{in} \) and the capacitor \( C_1 \). The equivalent circuit of mode 1 is shown in Figure 3(a). The voltage and current equations of this mode are obtained as follows:

\[
\begin{align*}
v_o &= v_{C_2} + v_{n_2} & (1) \\
i_o &= i_{L_2} - i_{n_2} & (2) \\
i_{L_k} &= i_{m} & (3) \\
i_{L_2} &= i_{n_2} & (4)
\end{align*}
\]

Mode 2 \( [t_1 < t < t_2] \): At \( t = t_1 \), the switch \( S \) is still ON and diode \( D_2 \) is turned ON at ZVS condition. Meanwhile, the output diode \( D_o \) is turned OFF. The equivalent circuit of mode 2 is shown in Figure 4(a). The following relations can be written for this mode.

\[
\begin{align*}
v_L &= v_{in} - v_{L_m} & (5) \\
v_{L_m} &= v_{C_3} - v_{C_1} & (6) \\
v_{L_m} &= v_{C_3} - v_{C_1} & (7) \\
v_{n_2} &= \frac{v_{C_3}}{n} - v_{C_2} & (8) \\
i_t &= i_{m} - i_{n_2} & (9) \\
i_{D_2} &= i_{n_2} & (10)
\end{align*}
\]

Mode 3 \( [t_2 < t < t_3] \): In this mode, diodes \( D_1 \) and \( D_o \) are turned ON and diode \( D_2 \) is turned OFF in ZCS condition. Also, at the beginning of this transition mode, the resonance between \( L_m \), \( C_1 \) and \( C_2 \) is finished. The equivalent circuit of mode 3 is shown in Figure 3(b). As can be seen, the capacitor \( C_3 \) is charged through diode \( D_1 \) and its current is \( i_{D_1} = -i_{C_1} \). The following equations are obtained in this mode:

\[
\begin{align*}
v_{C_3} &= 0 & (11) \\
v_t &= i_{in} + i_{C_1} & (12) \\
i_t &= i_{m} - i_{D_1} - i_{D_2} & (13)
\end{align*}
\]

Mode 4 \( [t_3 < t < t_4] \): At the beginning of this mode, the switch \( S \) is turned OFF. Stored energy in \( CL \) and \( C_2 \) is transferred to the output through the diode \( D_o \). Also, the capacitor \( C_3 \) is charged by \( C_1 \) and the input inductor \( L_{in} \). The current direction of mode 4 is depicted in mode 4 (b). In this subinterval, the following equations are achieved:

\[
\begin{align*}
v_o &= v_{C_3} + v_{C_2} - v_{n_2} & (14) \\
v_L &= v_{in} - v_{L_m} - v_{C_3} = v_{in} + v_{C_1} - v_{C_3} & (15)
\end{align*}
\]

The problems related to these converters are voltage spikes through the power switches due to the leakage inductance of the coupled inductor. In order to solve this problem in this mode,
the diode $D_1$ with capacitor $C_3$ can make the clamp circuit that leads to suppress the voltage spike through the switch. This can achieve by providing another path for flowing the leakage inductor current ($i_{Lm}$) through the diode $D_1$ and capacitor $C_3$, when the switch is in OFF-state.

**Mode 5 $[t_4 < t < t_5]$**: In the start of this mode, diode $D_1$ is turned OFF in the ZCS condition. The input current and magnetising inductance current is linearly decreased. In this mode, only diode $D_o$ is conducting. The current direction of mode 4 is depicted in mode 4 (c). Also, the voltages across diode $D_1$ and power switch $S$ are clamped by the capacitor $C_3$. In this mode, we have:

$$v_o = v_{C3} - v_{C1} - v_{Lm} + v_{C2} - v_{n2} \quad (16)$$

$$i_{Do} = i_{C3} + i_o \quad (17)$$
FIGURE 3  The operation modes of the proposed high step-up converter, (a) mode 1, and (b) mode 3

3  |  STEADY STATE ANALYSIS OF THE SUGGESTED CONVERTER

3.1  |  Voltage gain

Modes 1 and 3 are ignored because these two time-intervals are very short compared with other modes. By using the volt-second balance law for the magnetising and input inductors, Equations (18)–(20) are obtained for capacitor $C_1$, $C_2$, and $C_3$ as follows:

\[ V_{C_1} = DV_{C_3} = \frac{D}{1-D} V_{in} \]  (18)

\[ V_{C_2} = n \left( \frac{1-D}{1-D} \right) + \frac{1}{1-D} V_{in} \]  (19)

\[ V_{C_3} = \frac{1}{1-D} V_{in} \]  (20)

By using Equation (14), the voltage gain is achieved as follows:

\[ M = \frac{V_o}{V_{in}} = \frac{n+2}{1-D} \]  (21)

The coupling coefficient ($k$) of the coupled inductor is defined as follows:

\[ k = \frac{L_{m}}{L_{m} + L_{k}} \]  (22)

FIGURE 4  The operation modes of the proposed high step-up converter, (a) mode 2, (b) mode 4, (c) mode 5 and (d) DCM mode

The voltage gain by considering the coupling coefficient ($k$) is calculated as follows:

\[ M = \frac{V_o}{V_{in}} = \frac{n + nD(K-1) + 2}{1-D} \]  (23)

Thus, in Equation 18, if the coupling coefficient ($k$) is 1, the obtained equation in (21) can be achieved. According to Equation (21), by increasing the turn’s ratio and duty cycle, the voltage gain of the proposed converter is enhanced. Figure 5, indicates that the relation between the voltage gain with different duty cycles and different turns ratio. It
has to be mentioned that the proposed structure has a high voltage gain for various turns ratio of CL.

3.2 DCM operation

The operation time waveform of the suggested converter has been indicated in Figure 2(b). From this figure, it is apparent that the DCM has three operation modes. Modes 1 and 2 of DCM are same as the mode 2 and 4 of CCM. In mode 3 of DCM only diode \( D_1 \) is conducting and the other semiconductor elements are in OFF-state. In this mode, the second side of the coupled inductor current \( i_{s2} \) reaches zero. Regarding Figure 4(a), the following equations can be written for the first mode of DCM:

\[
\begin{align*}
\nu_{s1} &= V_{C3} - V_{C1} \\
\nu_{s2} &= V_{C2} - V_{C3} \\
\nu_{\text{Lin}} &= V_{\text{in}} + V_{C1} - V_{C3}
\end{align*}
\]

The second mode equations of DCM can be obtained as follows related to Figure 4(b):

\[
\begin{align*}
\nu_{s1} &= -V_{C1} \\
\nu_{s2} &= V_{C2} + V_{C3} - V_o \\
\nu_{\text{Lin}} &= V_{\text{in}} + V_{C1} - V_{C3}
\end{align*}
\]

The third mode of DCM has been indicated in Figure 4(d). In this mode, the stored energy in the second side of the coupled inductor is completely depleted. The third mode equations are expressed as follows:

\[
\begin{align*}
\nu_{s1} &= -V_{C1} \\
\nu_{s2} &= 0 \\
\nu_{\text{Lin}} &= V_{\text{in}} + V_{C1} - V_{C3}
\end{align*}
\]

The volt-second-balance low for the inductor in DCM mode, can be defined as follows:

\[
\int_{0}^{DT_s} \nu_{\text{Lin}}(1)\,dt + \int_{0}^{(D+D')T_s} \nu_{\text{Lin}}(2)\,dt + \int_{0}^{T_s} \nu_{\text{Lin}}(3)\,dt = 0
\]

\[
\int_{0}^{DT_s} \nu_{s1}(1)\,dt + \int_{0}^{(D+D')T_s} \nu_{s1}(2)\,dt + \int_{0}^{T_s} \nu_{s1}(3)\,dt = 0
\]

\[
\int_{0}^{DT_s} \nu_{s2}(1)\,dt + \int_{0}^{(D+D')T_s} \nu_{s2}(2)\,dt + \int_{0}^{T_s} \nu_{s2}(3)\,dt = 0
\]

The voltage gain in DCM can be derived as follows:

\[
M_{\text{DCM}} = \frac{V_o}{V_{\text{in}}} = \frac{n(D + D') + 2}{1 - D}
\]

where \( D' \) is expressed as follows:

\[
D' = \frac{V_o(1 - D) - (nD + 2)V_{\text{in}}}{nV_{\text{in}}}
\]

The peak current of the secondary side of the coupled inductor is equal to

\[
I_{s2} = \frac{nDT_s}{I_{s2}} V_{\text{in}}
\]

It is obvious that the average current of the capacitors in steady-state operation is equal to zero. Therefore, the average current of diodes will be equal to the average current of the output. Thus, the following equations can be written:

\[
I_{D1} = I_{D2} = I_{Dn} = I_o = \frac{1}{2}D'I_{s2}
\]

By substituting Equations (37) and (38) into Equation (39), and by knowing that \( I_o = V_o/R_i \), the voltage conversion ratio in DCM \( (M_{\text{DCM}}) \) can be achieved as follows:

\[
M_{\text{DCM}} = \frac{D(2 + nD)}{D(1 - D) - 2k_{s2}}
\]

The parameter \( k_{s2} \) is defined as follows:

\[
k_{s2} = \frac{2I_{s2}}{RT_s}
\]
3.3  BCM (boundary condition mode) operation

The BCM is occurred when the voltage conversion ratio in CCM is equal to voltage conversion ratio in DCM. The \( k_{n2_{\text{crit}}} \) should be defined for BCM operation which can be find as follows:

\[
M_{\text{CCM}} = M_{\text{DCM}} \tag{42}
\]

By substituting \( M_{\text{CCM}} \) and \( M_{\text{DCM}} \) in Equation (42) the \( k_{n2_{\text{crit}}} \) can be fined as follows:

\[
k_{L,n2_{\text{crit}}} = \frac{nd(1 - d)^2}{2(n + 2)} \tag{43}
\]

The \( k_{n2_{\text{crit}}} \) curve versus duty-cycle for \( n = 2 \) has been indicated in Figure 6. From this figure, when \( k_{n2} \) is higher than the \( k_{n2_{\text{crit}}} \), the recommended converter will be operated in CCM.

3.4  Voltage and current stresses

The maximum voltage across the semiconductors includes power switch \( S \) and diodes \( D_1, D_2 \) and \( D_o \) versus output voltage are calculated as follows:

\[
V_{DS} = V_{D1} = V_{C3} = \frac{1}{n+2} V_o \tag{44}
\]
\[
V_{D2} = V_{D_o} = \frac{n+1}{n+2} V_o \tag{45}
\]

Also, the maximum currents passing through power switch \( S \) and diodes \( D_1, D_2 \) and \( D_o \) versus output current are obtained as follows:

\[
i_{D1} = \frac{n+2}{1-D} I_o \tag{46}
\]
\[
i_{D2} = i_{D_o} = \frac{1}{1-D} I_o \tag{47}
\]
\[
i_s = 2MI_o = \frac{2(n+2)}{1-D} I_o \tag{48}
\]

Figure 7(a,b), indicate the voltage and current stresses on all the semiconductors. As shown in Figure 7(a), the voltage stress on diode \( D_1 \) with power switch \( S \) and \( D_2 \) with \( D_o \) are equal. Furthermore, the maximum current passes through diodes \( D_2 \) and \( D_o \) are equal. Related to Figure 7, it can be noted that the peak voltage and the peak current throughout the semiconductors are low, which leads to decrease the conduction losses and subsequently increase the system efficiency. The maximum voltage value of the power switch is constant for all power ranges (variable input source amplitude). In other words, the normalised voltage stress across the power switch will be decreased by increasing the turn’s ratio value. In fact, the output voltage value will increase for higher turns ratio values, but the maximum voltage stress of the power switch will remain constant. Therefore, a switch with constant nominal values can be used for all power levels. Also, this is caused to decrease the overall cost and increase the overall efficiency of the proposed converter.

4  DESIGN CONSIDERATIONS

4.1  The coupled inductor design

The magnetising inductor is designed with an assumption as follows:

\[
\Delta i_m \geq 20\%I_m \tag{49}
\]
On the other hand, the relation between voltage and current of an inductor can be written as follows:

\[ V_{I_m} = L_m \frac{dI_m}{dt} \]  

(50)

Therefore, the value of \( L_m \) can be obtained from Equation (31):

\[ L_m \geq \frac{DV_{I_m}}{20\% I_{m,f_s}} \]  

(51)

The average current of \( L_m \) is calculated as follows:

\[ I_{I_m} = I_m = M I_o = \frac{n + 2}{1 - D} I_o \]  

(52)

By replacing Equation (52) into Equation (51), the following equation can be obtained:

\[ L_m \geq \frac{D(1 - D) V_{I_m}}{20\% (n + 2) I_o f_s} \]  

(53)

The related equations for designing the size of the core, turn ratio and the wire size is completely discussed in [33]. The coupled inductor is designed related to maximum current of the magnetising inductances. Therefore, the magnetising inductance should be defined, which is indicated in Equation (53). The maximum current of the magnetising inductance current is equal to:

\[ I_{M,max} = I_M + \Delta I_M \]  

(54)

The root mean square (RMS) of the winding current of the coupled inductor can be obtained as follows:

\[ I_{tot} = \frac{n_1}{I_{I_m}} + \frac{n_2}{I_{I_m}} \]  

(55)

In order to design the coupled inductor in detail the following steps are utilised [33]:

1. Determine core size \( k_g \geq \frac{\rho I_M I_{I_m} M_{I_m} \times 10^{8}}{B_{max} A_{max}} \)
2. Determine the air gaps are neglected
3. Determine the winding number of the first side of the coupled inductor \( n_1 = \frac{I_M I_{I_m} M_{I_m} \times 10^{8}}{B_{max} A_{max}} \)
4. Determine the winding number of the second side of the coupled inductor \( n_2 = \frac{A_{w1}}{A_{w2}} \)
5. Evaluate fraction of window area allocated each winding \( (a_1 = \frac{n_1 I_{i,m}}{I_{I_m}}, a_2 = \frac{n_2 I_{i,m}}{I_{I_m}}) \)
6. Evaluate the wire size \( A_{w1} \leq \frac{a_1 k_1 W_1}{A_{w1}}, A_{w2} \leq \frac{a_2 k_2 W_2}{A_{w2}} \)

It has to be mentioned that in order to design the coupled inductor, the EPCOS B66344 (Ferrite core EE60) model is utilised. The magnetising inductance \( (L_m) \) is chosen 100 \( \mu \)H. For the coupled inductor with \( L_m = 100 \mu H \), the number of the first side of the coupled inductor winding is 34 turns and also the number of the second side of the coupled inductor winding is 68 turns. Regarding Eq. 54, if we consider the coupling coefficient about 0.98 and \( L_m = 100 \mu H \) in the experimental result, the leakage inductance \( (L_k) \) can be calculated as follow:

\[ K = \frac{L_m}{L_m + L_k} \]  

(56)

By solving Equation (54), the leakage inductance \( (L_k) \) is obtained about 2 \( \mu H \). Extreme care has been taken in the design of the coupled inductor to have a low leakage inductance.

### 4.2 Coupled inductor turns ratio

Using (21), the turn’s ratio of the used coupled inductor can be calculated as:

\[ n = M (1 - D) - 2 = \frac{V_o}{V_i} (1 - D) - 2 \]  

(57)

According to Equation (34), the value of the selected duty cycle affects the number of coupled inductor’s turn’s ratio.

### 4.3 Capacitors

Susceptibility on the voltages of the capacitors will reduce the output voltage quality, so the capacitors are considered to preserve the voltage constant. The output capacitor is calculated based on the output current and output voltage as follows:

\[ C_o = \frac{2D^2 I_o}{\Delta V_{C_o} I_s} \]  

(58)

Finally, the minimum values of the capacitors \( C_1, C_2, C_3, \) and \( C_o \) are obtained by Equations (59)–(62), respectively:

\[ C_1 \geq \frac{(n + 2)^2 I_o}{2\% V_o (1 - D) f_s} = \frac{(n + 2)^2}{2\% (1 - D) R_o f_s} \]  

(59)

\[ C_2 \geq \frac{D (n + 2)}{2\% (1 - D) n R_o f_s} \]  

(60)

\[ C_3 \geq \frac{D (n + 2) (n + 4)}{2\% (1 - D) R_o f_s} \]  

(61)

\[ C_o \geq \frac{D I_o}{2\% V_o f_s} = \frac{D}{2\% R_s f_s} \]  

(62)

### 4.4 The input filter design

In DC–DC converters which are utilised in renewable energy systems, the input current ripple is the main factor to determine the lifetime of the input sources. Renewable energy
systems such as solar cells have a pulse current. Therefore, the main requirement of such a DC–DC converter, which are
used as interfacing converter, is that the ripple of input current
should be low. Thus, the input inductor $l_{in}$ of the suggested
converter is given by:

$$l_{in} = \frac{DV_{in}}{f_s \Delta i_{in}}$$  \hspace{1cm} (63)

The input current ripple is considered 10–20% of the average
input current, which is acceptable in DC–DC converters.

5  |  EFFICIENCY ANALYSIS

Power losses of the proposed converter include power losses of
switch $S$ (conduction and switching losses), diodes conduction
losses, capacitors ESR losses, and magnetic components losses
(ohmic and core losses). In the proposed converter, due to the
ZCS condition of diodes $D_1$ and $D_2$, the reverse recovery losses
of the mentioned diodes can be ignored. The efficiency of the
proposed converter can be calculated as:

$$\eta = \frac{P_o}{P_{in}} = \frac{P_o - P_{Loss}}{P_{in}}$$ \hspace{1cm} (64)

Considering the above-mentioned situations, the total power
losses can be expressed as follows:

$$P_{Loss} = P_{Loss}^{Switch} + P_{Loss}^{Diodes} + P_{Loss}^{Capacitors} + P_{Loss}^{Magnetics}$$ \hspace{1cm} (65)

The power losses in switch $S$ are obtained by using Equation
(66):

$$P_{Loss}^{Switch} = P_{Loss}^{Conduction} + P_{Loss}^{Switching}$$ \hspace{1cm} (66)

$$P_{Loss}^{Switch} = r_{DS} \left( I_{rms}^{D1} \right)^2 + \frac{1}{2} V_{gs} \sqrt{f_s \left( t_{on} + t_{off} \right)}$$ \hspace{1cm} (67)

It should be noted that the diodes power losses are dependent
on voltage drop and conduction resistance in the turn-on mode,
as follows:

$$P_{Loss}^{Diodes} = V_{Forward} \left( I_{rms}^{D1} + I_{rms}^{D2} + I_{rms}^{D3} \right) + ESR_{D1} \left( I_{rms}^{D1} \right)^2$$

$$+ ESR_{D2} \left( I_{rms}^{D2} \right)^2 + ESR_{D3} \left( I_{rms}^{D3} \right)^2$$ \hspace{1cm} (68)

The power losses of the used capacitors due to ESR values
are given by:

$$P_{Loss}^{Capacitors} = ESR_{C1} \left( I_{rms}^{C1} \right)^2 + ESR_{C2} \left( I_{rms}^{C2} \right)^2$$

$$+ ESR_{C3} \left( I_{rms}^{C3} \right)^2 + ESR_{C0} \left( I_{rms}^{C0} \right)^2$$ \hspace{1cm} (69)

The magnetic components of power losses include ohmic
losses and core loss as follows:

$$P_{Loss}^{Magnetics} = P_{Loss}^{Ohmic} + P_{Loss}^{Core}$$ \hspace{1cm} (70)

The total ohmic losses consist of input inductor and coupled
inductor winding losses, as follows:

$$P_{Loss}^{Ohmic} = r_{in} \left( I_{rms}^{in} \right)^2 + r_{c1} \left( I_{rms}^{in} \right)^2 + r_{c2} \left( I_{rms}^{in} \right)^2$$ \hspace{1cm} (71)

The core losses of magnetic devices are obtained as:

$$P_{Loss}^{Core} = P_{Loss}^{in} + P_{Loss}^{CL} = k \beta_1 \beta_2 W_{in} + k \beta_3 \beta_4 W_{CL}$$ \hspace{1cm} (72)

where $k$ is the inductors eddy current losses coefficient and is
0.005, $\beta$ is the core magnetic flux. $W_i$, the mass (kg) of cores, is
0.1, $\beta = 1.2$ and $\alpha = 2.12$ are constant and depend on the type
of cores.

As given in Equations (67)–(71), RMS value for the current of
the switch $S$, all diodes, capacitors, and magnetic devices and the
average current of the power switch $S$ should be calculated. The
average and RMS values for the current of switch $S$ is obtained
as follows:

$$I_{avg}^S = \frac{n + 2 \sqrt{D \left( n + 2 \right) V_o}}{1 - D}$$ \hspace{1cm} (73)

$$I_{rms}^S = \frac{2 \sqrt{D \left( n + 2 \right) V_o}}{1 - D}$$ \hspace{1cm} (74)

Equations (75)–(77) are used for obtaining RMS current of
diodes $D_1$, $D_2$, and $D_3$, respectively:

$$I_{rms}^{D1} = \frac{n + 2 \sqrt{D \left( n + 2 \right) V_o}}{1 - D}$$ \hspace{1cm} (75)

$$I_{rms}^{D2} = \frac{2 \sqrt{D \left( n + 2 \right) V_o}}{1 - D}$$ \hspace{1cm} (76)

$$I_{rms}^{D3} = \frac{2 \sqrt{D \left( n + 2 \right) V_o}}{1 - D}$$ \hspace{1cm} (77)

RMS current of capacitors $C_1$, $C_2$, $C_3$ and $C_0$ are obtained as
follows:

$$I_{rms}^{C1} = \frac{n + 2 \sqrt{D \left( n + 2 \right) V_o}}{n}$$ \hspace{1cm} (78)

$$I_{rms}^{C2} = \frac{n + 2 \sqrt{D \left( n + 2 \right) V_o}}{n}$$ \hspace{1cm} (79)

$$I_{rms}^{C3} = \frac{2 \sqrt{D \left( n + 2 \right) V_o}}{n}$$ \hspace{1cm} (80)

$$I_{rms}^{C0} = \frac{\sqrt{D \left( n + 2 \right) V_o}}{n}$$ \hspace{1cm} (81)
Furthermore, RMS current of the input and coupled inductor is given by:

\[
I_{\text{rms}}^{\text{input}} = \frac{(n + 2) V_o}{R_o} \sqrt{1 + D - D^2} \quad (82)
\]

\[
I_{\text{rms}}^{\text{D}} = \frac{V_o}{n R_o} \sqrt{\frac{D}{(1 - D)^3}} \quad (83)
\]

61 COMPARISON STUDY

In this section, a comparison between the proposed non-isolated high step-up converter and some similar converters with the same family under the same condition is provided based on voltage gain, voltage stress across switches, maximum peak voltage through the diode, input current ripple, the number of components, and soft-switching feature. Among the compared converters in Table 1, in the represented converters in [7], [10], and [20] two power switches were used. However, in the rest of the converters, only one power switch was used.

Figure 8 shows the comparison results between the voltage gain of the proposed converter and other reported converters in Table 1 versus the duty cycle and coupled inductor turns ratio. According to Figure 8, the proposed converter has a higher voltage gain than other converters. As a result, for an equal output voltage, the presented structure can be operated in a low duty cycle in comparison with other converters as given in Table 1. Thus, in such conditions, the efficiency of the suggested converter will be higher than the other mentioned converters. It can be noticed that the voltage gains of the converters in [1] is equal with [10], in [8] is equal with [18] and in [4] is equal with [6], [11], [12], and [17]. Noted that the voltage gains in Figure 8, is obtained for the coupled inductor turn ratio equal to 1 (\(n = 1\)). It is obvious that by increasing the turn ratio of the coupled inductor, the voltage gain is increased exponentially, and subsequently the maximum voltage through the switch is decreased.

In terms of converters efficiency, it can be mentioned that the converters represented in [4], [7], [8], [9], [12], and [17] suffer from lack of soft-switching feature, so the efficiency of these converters are lower than the other introduced structures in Table 1. In addition, in the suggested structure with the wide voltage conversion ratio and soft-switching conditions, it is possible to reduce the duty cycle and coupled inductor turns ratio. Therefore, the losses in the power switch and magnetic components can be reduced. As a result, the proposed converter has

\[I_{\text{rms}}^{\text{input}} = \frac{(n + 2) V_o}{R_o} \sqrt{1 + D - D^2} \]

\[I_{\text{rms}}^{\text{D}} = \frac{V_o}{n R_o} \sqrt{\frac{D}{(1 - D)^3}}\]

| Converter | CI* | I* | S* | D* | C* | M_{\text{CGM}} | \(V_{\text{s}}/V_o\) | \(V_{\text{D}}/V_o\) | Input current ripple | Soft switching |
|-----------|-----|----|----|----|----|----------------|----------------|----------------|-------------------|---------------|
| [1]       | 1   | 1  | 1  | 2  | 2  | \(\frac{2}{1 + D}\) | \(\frac{1}{a} = 0.5\) | 1               | Low              | Yes            |
| [4]       | 1   | 0  | 1  | 3  | 3  | \(\frac{1}{1 + D}\) | \(\frac{1}{a} = 0.33\) | 1               | High             | No             |
| [6]       | 1   | 0  | 1  | 3  | 3  | \(\frac{1}{1 + D}\) | \(\frac{1}{a} = 0.5\) | \(\frac{1}{a + 1} = 0.66\) | Low              | Yes            |
| [7]       | 1   | 0  | 2  | 5  | 3  | \(\frac{2 - D}{1 + D}\) | \(\frac{1}{2(2-D)} = 0.17\) | \(\frac{1}{2-D} = 0.71\) | Low              | No             |
| [8]       | 1   | 1  | 1  | 4  | 3  | \(\frac{1 + D}{1 + D}\) | \(\frac{1}{1 + D} = 0.45\) | \(\frac{1}{1 + D} = 0.9\) | High             | No             |
| [9]       | 1   | 1  | 1  | 2  | 2  | \(\frac{2 + D}{1 + D}\) | \(\frac{1}{2 + D} = 0.29\) | \(\frac{1}{2 + D} = 0.65\) | High             | No             |
| [10]      | 1   | 1  | 2  | 2  | 3  | \(\frac{1}{1 + D}\) | \(\frac{1}{a} = 0.5\) | 1               | Low              | Yes            |
| [11]      | 1   | 1  | 1  | 3  | 4  | \(\frac{1}{1 + D}\) | \(\frac{1}{a} = 0.33\) | \(\frac{1}{a + 1} = 0.66\) | High             | Yes            |
| [12]      | 1   | 1  | 1  | 3  | 3  | \(\frac{1}{1 + D}\) | \(\frac{1}{a} = 0.33\) | \(\frac{1}{a + 1} = 0.66\) | Low              | No             |
| [17]      | 1   | 0  | 1  | 4  | 5  | \(\frac{1}{1 + D}\) | \(\frac{1}{a} = 0.33\) | \(\frac{1}{a + 1} = 0.66\) | High             | No             |
| [20]      | 1   | 0  | 2  | 0  | 4  | \(\frac{1}{1 + D}\) | \(\frac{1}{a} = 0.45\) | -               | High             | Yes            |
| Proposed  | 1   | 1  | 1  | 3  | 4  | \(\frac{1}{1 + D}\) | \(\frac{1}{a} = 0.25\) | \(\frac{1}{a + 1} = 0.75\) | Low              | Yes            |

*S = switch, *D = diodes, *C = capacitors, *CI = coupled inductor, *I = inductor.
higher efficiency than the other reported converters due to high voltage gain, a smaller number of components, and the soft-switching capability of diodes $D_1$ and $D_2$.

Figure 9(a,b) depicts comparison results of the peak voltage through the switches and diodes versus coupled inductor turn ratio, respectively. As illustrated in Figure 9(a), for all mentioned converters, the peak voltage on power switches is proportionally decreased with increasing of coupled inductor turn ratio. It has to be noticed that only the converter in [7] has lower voltage stress on the switch than the presented converter. However, this converter has low voltage gain with high input current ripple, the high number of components, and lower efficiency with no soft-switching capability compared to the proposed structure.

According to Figure 9(b), the represented converters in [6], [9], [11], [12] and [17] have lower voltage stress on diode than the proposed high step-up converter. However, the converters in [9], [11], and [17] have high input current ripple than the proposed converter and also, there is no soft-switching capability in [9], [17], and [12], and also the efficiency is low in [12], too. Although, the converter represented in [6] has lower peak voltage than the suggested structure, but it operates in DCM with lower voltage gain and higher peak voltage through the switch in compared to the suggested converter. Therefore, this converter is not suitable for renewable energy applications. Noted that the presented voltage stress in Figure 9(a,b), are obtained for duty cycle is equal to 0.6 ($D = 0.6$).

The obtained content result of Table 1 is implemented by considering $n = 2$ and $D = 0.6$ for all converters for a better realisation of the superiority of the proposed converter among other reported structures in the same family. Due to this table, it can be concluded that the presented structure has the merits of high voltage gain with soft-switching capability, low voltage stress through the semiconductors, and high efficiency with a smaller number of components in the same condition. With regard to comparison results, it has to be noticed that the proposed structure can be a suitable candidate for sustainable energy applications such as PV power plants.

## 7 Dynamic Model and Controller Method

It should be noticed that the industrial loads typically contain inductance as well as resistance. Moreover, the inductance characteristic of the load can affect the dynamic behaviour of the converter. In order to control the proposed converter, the load is assumed as RL. In the first step, the dynamic model of the suggested structure is described as follows:

$$ x = Ax + Bu, \quad y = Cx + Du \quad (84) $$

where $x$ is the space state vector, $u$ is the input vector, and $y$ is the output vector:

$$ x = \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \\ v_{C_3} \\ v_{C_4} \end{bmatrix}, \quad y = \begin{bmatrix} i_{L_1} \\ i_{L_2} \end{bmatrix}, \quad u = \begin{bmatrix} v_o \\ f_o \end{bmatrix} \quad (85) $$

Also, matrix $A$, $B$, $C$ and $D$ are obtained as follows:

$$ A = \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L_1} & 0 & -\frac{1}{L_2} & 0 \\ 0 & 0 & 0 & -\frac{1}{L_1} (1+\alpha)(1) & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{L_1} (1+\alpha) & 0 & 0 \\ 0 & -\alpha \frac{1}{L_1} (1+\alpha) & 0 & 0 & 0 & 0 & 0 \\ -\alpha \frac{1}{L_2} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\alpha \frac{1}{L_2} (1+\alpha) & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (86) $$

$$ B = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \quad C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad D = \begin{bmatrix} 0 \end{bmatrix} \quad (87) $$

FIGURE 9 Voltage stress comparison between the proposed and the other converters in Table 1, (a) voltage stress on switches, and (b) voltage stress on diodes.
In the next step, to obtain the small signal-model of the proposed converter, the nonlinear space state equations are linearised by assuming the Equation (88):

\[
\begin{cases}
    d = D + \hat{d} \\
    \hat{v}_m = V_m + \hat{v}_m \\
    X = X + \hat{X}
\end{cases}
\]  

(88)

Where, \(D\), \(V_m\), and \(X\) are the steady-state components. \(\hat{d}\), \(\hat{v}_m\), and \(\hat{X}\) are small AC variations. Substituting Equation (88) into Equation (85) and neglecting steady-state terms, the linear small-signal equations are achieved as follows:

\[
L_m \frac{d\hat{i}_{m}}{dt} = \hat{v}_m + \hat{i}_C - \hat{i}_C
\]

(89)

\[
(1 + n) L_m \frac{d\hat{i}_{m}}{dt} = \hat{i}_C (1 + nD) + n\hat{d}V_C_1
\]

\[
+ \hat{i}_C (1 - D) - \hat{d}V_C_2 + \hat{i}_C (1 + nD) + n\hat{d}V_C_3
\]

(90)

\[
L_m \frac{d\hat{i}_C}{dt} = \hat{i}_C - R\hat{d}I_v
\]

(91)

\[
\frac{d\hat{v}_{C_1}}{dt} = \hat{i}_m (1 - 2D) - 2\hat{d}I_v + C_1 \hat{i}_r + \hat{d}I_v - \hat{i}_r (1 - D) + \hat{d}I_v
\]

(92)

\[
\frac{d\hat{v}_{C_2}}{dt} = \hat{i}_m (1 + (n - 1) D) + \frac{\hat{d} (n - 1) I_m}{C_1}
\]

(93)

\[
\frac{d\hat{v}_{C_3}}{dt} = \hat{i}_m (1 - 2D) - 2\hat{d}I_v + \hat{i}_m \frac{(n + 1) D}{C_1 C_2}
\]

\[
+ \frac{(n + 1) \hat{d} I_m - \hat{i}_r (1 - D) + \hat{d}I_v}{C_1 C_2}
\]

(94)

\[
\frac{d\hat{v}_{C_3}}{dt} = \hat{i}_m (1 - D) - \hat{d}I_v + \hat{i}_r (1 - 2D) - 2\hat{d}I_v
\]

(95)

By applying the Laplace transformation on Equations (89)–(95) and neglecting \(\hat{v}_m\), the output voltage-to-duty ratio transfer function is obtained as follows:

\[
G_d (s) = \frac{\hat{v}_o (s)}{\hat{d} (s)} = \frac{K_1 W_1 + (1 - D) W_2}{(1 - D) W_3 + K_2 W_4 C_0 \delta}
\]

(96)

Where, \(K_1, K_2, W_1, W_2, \) and \(W_3\) are given by Equations (97)–(101):

\[
K_1 = 2I_{m_1} + I_{m_2}
\]

(97)

\[
K_2 = \frac{(1 - 2D)}{C_0 \delta (L_{m_0} + R_C)}
\]

(98)

\[
W_1 = \frac{I_1 - V_o - V_C_3}{Z_1}
\]

(99)

\[
W_2 = \frac{(u V_C_1 + n V_C_3 - V_C_2) + Z_4 - Z_5}{Z_1}
\]

(100)

\[
W_3 = \frac{Z_6 + Z_7 - Z_8}{Z_1}
\]

(101)

Parameters \(Z_1, Z_2, \) and \(Z_3\) are summarised in Table 2. The open-loop bode diagram of the proposed converter is shown in Figure 10. As can be seen that, GM is positive and PM of the system is more than 45 degrees. Therefore, the closed-loop control of the suggested converter, the PI controller is used, which does not add a positive phase to the system but it can obtain better steady-state performance. The closed-loop control system is shown in Figure 11. The transfer function of the used PI controller is given as:

\[
G_C (s) = 0.6 \left(1 + \frac{15.7 \times 10^3}{s}\right)
\]

(102)

Finally, the bode diagram of the proposed converter after closed-loop control is shown in Figure 12. According to this figure, after closed-loop control PM is more than 45 degrees, and the GM of the system is positive. So, a stable situation is obtained.

### Table 2 parameters \(Z_1, Z_2, \) and \(Z_3\)

| Parameter | Expression |
|-----------|------------|
| \(Z_1\)  | \( (1 + n)L_m \) |
| \(Z_2\)  | \( \frac{2(1 + nD)I_m + 2Z_5 - Z_4}{C_0 \delta} \) |
| \(Z_3\)  | \( \frac{2(1 + nD)I_m - Z_4}{C_0 \delta} \) |
| \(Z_4\)  | \( \frac{2(1 + nD)I_m + Z_5}{C_0 \delta} \) |
| \(Z_5\)  | \( \frac{(1 - D)^2 + (1 - D)^2}{L_m (L_m + R_C)} \) |
| \(Z_6\)  | \( \frac{(1 + nD)I_m + 2Z_5 - Z_4}{C_0 \delta} \) |
| \(Z_7\)  | \( \frac{(1 + nD)I_m + 2Z_5 - Z_4}{C_0 \delta} \) |
| \(Z_8\)  | \( \frac{(1 + nD)I_m + 2Z_5 - Z_4}{C_0 \delta} \) |

### 8 EXPERIMENTAL RESULTS

A hardware prototype with 200 W output power has been built and tested in the laboratory to confirm the theoretical equations and analysis of the suggested converter, which is illustrated in Figure 13. In order to control the power switch of the suggested converter, the microcontroller (ATMEGA16) has been utilised. The characteristics of the circuit components of the prototype are indicated in Table 3. Also, the operation details of the proposed structure are illustrated in Table 4.

The main experimental waveforms are depicted in Figures 14–16. Figure 14 demonstrates the input, output, and capacitor’s voltage waveforms. As shown in Figure 14(a), the input \(V_{in}\) and output \(V_o\) voltages are 20 V and 195 V, respectively. This figure confirms the obtained voltage gain in Equation (20). On the other hand, the output voltage ripple is low and can be neglected. Furthermore, Figure 14(b–d) shows the voltages across capacitors \(C_1, C_2\), and \(C_3\), respectively. According to these figures, the
voltage across capacitor $C_f$ is about 28.8 V and confirms the Equation (17). Moreover, the voltages across capacitors $C_2$ and $C_3$ are approximately 89 and 49 V, which confirm Equations (18) and (19), respectively. The voltage and current waveforms of switch $S$ and diodes $D_1$, $D_2$ and $D_o$ are demonstrated in Figure 15(a–d), respectively. Figure 15(a) shows that the voltage and current of switch $S$ are nearly 49 V and 18.5 A. As this figure shows, the maximum voltage across the power switch $S$ is smaller than the output voltage, which verifies Equation (21). The measured values of the diode $D_1$ voltage and current are about 49 V and 9.9 A, which is shown in Figure 15(b). According to Figure 15(a,b), the peak voltage across the power switch $S$ and diode $D_1$ are equal, which are smaller than the output voltage. Besides, diode $D_1$ turns off at ZCS that leads to decrease in the reverse recovery loss. The maximum voltage and maximum current of diode $D_2$ are indicated in Figure 15(c), which are almost 145 V and 2.4 A. In this figure, ZVS in on-state and ZCS in off-state are specified. Regarding Figure 15(b,c), before the switching off or switching on process of the diodes $D_1$ and $D_2$, the resonance was performed to produce the ZCS and ZVS conditions. Therefore, it can be said that the suggested converter is operated in quasi-resonant operation. The peak voltage and current of diode $D_o$ are equal with diode $D_2$ as shown in Figure 15(d). Figure 16(a–d) demonstrates the waveforms of the inductor $L_{in}$, primary, and secondary windings current of the coupled inductor, respectively. The maximum and minimum of input inductor current ($I_{in}$) are almost 9.1 and 9.5 A, respectively. Therefore, the proposed structure has a very low input current ripple (about 4.3%), which leads to the lifetime increasing of the input source of the proposed topology. Related to Figure 16(c–d), it can be seen that the currents ripple contents of the coupled inductor are acceptable for a high step-up DC–DC converter. The operational analysis of the suggested converter such as magnetic components current charge and discharge (Figure 2) can be verified related to the gate-source voltage and the magnetic current waveforms.

The voltage stress on the switch in experimental results for a different range of duty-cycle is measured and indicated in Figure 17. From this figure, it can be found that the voltage stress throughout the switch is lower than the output voltage for all duty-cycles that leads to higher efficiency achieving for such converter.

### TABLE 3 List of the circuit components of the prototype

| Element | Specification |
|---------|---------------|
| Power switch $S$ | IRF260N (200 V /50 A), $R_{DS(ON)} = 0.04 \Omega$ |
| $D_1, D_2, D_o$ | MUR2060 (600 V /20 A)MUR1560 (600 V /15 A) |
| $C_1, C_2, C_3$ | 220 V/200 \(\mu\) F |
| $C_o$ | 400 V/400 \(\mu\) F |
| $L_{in}$ | 100 \(\mu\) H, $\eta_1 = 1 m\Omega$, $\eta_{12} = 3 m\Omega$, $\eta_2 = 2 m\Omega$ |
| Coupled inductor | Ferrite EE60 core with $L_{in} = 100 \mu H$, $\eta_1 = 3 m\Omega$, $\eta_2 = 3 m\Omega$, $L_k = 2 \mu H$ |

### TABLE 4 Specification of the experimental prototype of the proposed converter

| Parameters | Value |
|------------|-------|
| Rated output power | 200 W |
| Input voltage | 20 V |
| Output voltage | 200 V |
| Turns ratio of the coupled inductor ($n$) | 2 |
| Switching frequency ($f_s$) | 50 kHz |
The transient response of the proposed converter for step-change about 10% in input voltage is illustrated in Figure 18(a) for RL load. Based on this figure, it is clear that the proposed converter has a good dynamic response for the step-change in the input voltage. Besides, the transient response for the sudden load variations is indicated in Figure 18(b). Due to Figure 18, it can be found that the suggested converter has an appropriate dynamic response for the step-change in load and input voltage.

Table 5 is provided to assess the analysis and also illustrating the comparison of the measured and calculated circuit variables in both theoretical and experimental results. It has to be mentioned that there is a little difference between the values of each section because, in practice, the elements are not ideal and have conduction losses.

The proposed converter's experimental and theoretical efficiency versus output power and the power losses diagrams are illustrated in Figure 19(a–b), respectively. As illustrated in this figure, due to the ZCS condition, high efficiency is achieved at output power equal to 200 W by decreasing the conduction losses. According to theoretical analysis and laboratory results, it can be concluded that the suggested structure can be an acceptable choice for renewable energies such as PV panels because of high efficiency and lower peak voltage through the semiconductors. Also, Figure 19(c) shows a comparison between the proposed converter’s efficiency and other introduced converter in Table 1. According to this figure, the presented structure has higher efficiency at 200 W output power. It should be noted that the 200 V converter is built in the laboratory in order to confirm the correctness of the proposed converter operation analysis and the mathematical calculation. The experimental results of this sample are designed to use low rating elements that lead to reduce the cost of the proposed converter.

Related to the theoretical analysis, comparison survey, and laboratory result, it is clear that the used semiconductor elements in the proposed topology have presented at a low peak voltage, which results in lower cost and higher efficiency of the converter. Besides, it has been shown that in the proposed
FIGURE 14  The experimental measurement of (a) $V_{C1}$, (b) $V_{C2}$, (c) $V_{C3}$ and (d) $V_{o} - V_{a}$.

FIGURE 15  The experimental measurement of (a) $V_{sw} - I_{sw}$, (b) $V_{D1} - I_{D1}$, (c) $V_{D2} - I_{D2}$ and (d) $V_{Do} - I_{Do}$.
structure, efficiency is flexible and higher than 95% that shows the suggested converter can operate in high power rating in industry application. Therefore, by using high power rating elements in the laboratory prototype, the proposed converter can be utilised in low power and high-power applications such as PV systems, fuel cells, and LED lamps.
FIGURE 19  Efficiency and losses of the proposed converter, (a) efficiency versus output power, (b) proportion of losses at power = 200 W, $D = 0.6$, $V_{in} = 20$ V and (c) comparison of the proposed converter’s efficiency with the introduced converters in Table 1
9 | CONCLUSION

In this paper, a novel single switch non-isolated DC–DC converter with a high voltage conversion ratio was proposed. The benefits of this converter include: (1) high voltage gain; (2) low input current ripple with operation in continuous conduction mode; (3) low peak voltage across power switch and diodes, and (4) existence of ZCS and ZVS conditions for diodes. The coupled inductor and VMC technique have been utilised to enhance the voltage conversion ratio. To decrease the peak voltage across the active switch, the VMC operates as a clamp circuit. The ZCS condition leads to high efficiency by decreasing the reverse recovery losses of diodes. Also, using only one power MOSFET with lower ON-state resistance provides the simple control circuit for the suggested topology. To demonstrate the performance of the proposed structure, the principle of the operation modes, comparison results, dynamic behaviour analysis, and control method were given. Finally, experimental results with a 200W power level at 50 kHz operating frequency show the validity of the design. According to the presented converter specification, it can be concluded that the suggested topology can be used in power conversion applications such as sustainable energy systems, LED drivers etc.

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