Tuning supercurrent in Josephson field effect transistors using h-BN dielectric

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The transparent interface in epitaxial Al-InAs heterostructures provides an excellent platform for potential advances in mesoscopic and topological superconductivity. Semiconductor-based Josephson Junction Field Effect Transistors (JJ-FETs) fabricated on these heterostructures have a metallic gate that tunes the supercurrent. Here we report the fabrication and measurement of gate-tunable Al-InAs JJ-FETs in which the gate dielectric in contact with the InAs is produced by mechanically exfoliated hexagonal boron nitride (h-BN) followed by dry transfer using a van der Waals-mediated pick up process. We discuss the fabrication process that enables compatibility between layered material transfer and Al-InAs heterostructures to avoid chemical reactions and unintentional doping that could affect the characteristics of the JJ-FET. We achieve full gate-tunability of supercurrent by using only 5 nm thick h-BN flakes. We contrast our process with devices fabricated using a conventional AlO\textsubscript{x} gate dielectric and show that h-BN could be an excellent competing dielectric for JJ-FET devices. We observe that the product of normal resistance and critical current, I\textsubscript{n}R\textsubscript{n}, is comparable for both types of devices, but strikingly higher R\textsubscript{n} for the h-BN-based devices indicating that the surface is doped less compared to AlO\textsubscript{x} gate dielectric.

Understanding and engineering JJ-FETs fabricated on semiconductors with highly transparent contacts can yield a gate-controllable supercurrent \cite{1,9}. Tuning the conductivity of the semiconductor part of a JJ-FET affects superconducting properties. For example, JJ-FETs fabricated on Al-InAs have been used for tunable superconducting qubits, the so-called “gatemon”, where the qubit frequency, which depends on the value of the supercurrent, can be tuned in-situ with an applied electric field \cite{10}. Furthermore, since InAs has large spin-orbit coupling, Al-InAs system can host topological superconductivity and Majorana bound states \cite{11,14}. In this work we discuss a novel fabrication process for gating semiconductor-based JJ-FETs and study their behavior via quantum transport measurements \cite{15}.

JJ-FET devices on III-V materials above the superconducting critical temperature behave practically like a III-V transistor. Historically, performance enhancement of these devices has been achieved through shrinking the gate length of transistors. However, the constant electrostatic scaling started to deviate as the gate lengths of transistors were pushed into the nanoscale. The advent of high-k dielectrics offered a solution and also opened up the opportunity for exploring III/V materials which should also be able to provide sufficiently low density of charge traps for reliable device operation. While the standard atomic layer deposition of the gate dielectric used for FET or JJ-FET is a high-k oxide such as AlO\textsubscript{x} or HfO\textsubscript{x} \cite{16,19}, the challenge continues to develop high performance devices with lowest density of charge traps.

The ability to replace this layer with an ultrathin insulator with no chemical bonding to the InGaAs/InAs channel can modify and enhance the efficiency of the junctions. Two-dimensional (2D) materials are, in principle, excellent candidates for both their fundamental properties and their flexibility in fabrication techniques. In 2D material device studies, thin layers of h-BN have served diverse device functions including dielectric substrates \cite{20}, proton transport membranes \cite{21}, encapsulation layers \cite{15,22}, and tunneling barriers \cite{23,24}. Properties of h-BN leading to superior device performance include an atomically flat and dangling-bond-free surface, low density of charge traps, high surface optical phonon frequency, and low microwave absorption \cite{25,29}. In this letter we introduce h-BN as a gate dielectric for epitaxial Al/InAs JJ-FETs.

Figure 1(a) illustrates the material stack grown on a semi-insulating InP (001) substrate. A layer of InAs with 4 nm thickness is grown on a 6 nm
layer of In$_{0.81}$Ga$_{0.19}$As to form a quantum well on a step-graded buffer of In$_X$Al$_{1-X}$As. To couple the two-dimensional electron gas (2DEG) to the superconductor, a finite charge distribution at the semiconductor/metal interface is required. A layer of In$_{0.81}$Ga$_{0.19}$As with the thickness of 10 nm satisfies this condition while producing an optimal interface with relatively high 2DEG mobility [16, 30]. A voltage ($V_G$) applied to the graphite top gate (gray in Fig. 1(a)) controls the carrier density in the semiconductor region.

Figure 1(b) shows a scanning electron microscope image of the superconductor/semiconductor/superconductor device. The JJ fabrication process is performed by electron beam lithography using polymethyl methacrylate (PMMA) as the resist. Device mesas are defined and etched using Transene type D Al etchant followed by a III-V etch solution ($C_6H_8O_7 (1M)$ 18.3: $H_3PO_4 (85\%)$ 0.43: $H_2O_2 (30\%)$ 1: $H_2O$ 73.3). In the active region of the junction, the mesa is 4 $\mu$m wide. In a second step, the gap between superconducting contacts of the JJ was patterned by selective etching of Al over InGaAs/InAs using Transene type D. All presented samples have a gap of $\sim 100$ nm.

During initial device fabrication attempts, a stamp made of a thin polycarbonate (PC) film on polydimethylsiloxane (PDMS) was used to construct the graphite/h-BN stack and transfer it onto aluminum contacts. However, the chloroform used to remove the PC after transfer etched the aluminum contacts and destroyed the Al/InAs junctions, likely because of a small concentration of HCl created in the chloroform by its ethanol stabilizer. To eliminate chloroform from the fabrication process, a modified version of this technique was used to create stamps with polypropylene carbonate (PPC), which was dissolved in anisole.

Here, we focus on two JJ devices A and B fabricated on nominally identical heterostructures. The 2DEGs in these heterostructures were characterized separately by magneto-resistance measurements in van der Pauw geometry. Both samples have density of $7 \times 10^{11}$ cm$^{-2}$. They also have an estimated mean free path $\ell_e$ of 200 nm. As a consequence with superconducting electrode gap of $L = 100$ nm both samples are expected to be close to the ballistic regime $L < \ell$. The superconducting gap of the Al was estimated to be about 210 $\mu$eV from the critical temperature of the film in both samples ($T_c \sim 1.4$ K). In both samples, the Thouless energy $E_{\text{Thouless}} = \frac{\hbar v_F \ell_e^2}{L^2}$, with $v_F$ the Fermi velocity and L the gap of the JJ, is larger than 1 meV, which implies that our junctions are in the short limit ($\Delta \ll E_{\text{Thouless}}$).

Figure 2a shows differential resistance (dV/dI) vs. measured d.c. bias current as a function of applied top gate voltage at 30 mK. We observed that the critical current remains nearly unchanged above $V_G > 1$ V while it decreases below this value similar to JJ-FET devices with AlO$_x$ as the gate dielectric [31]. As we tune the gate voltage toward more negative values, the window with zero resistance state...
FIG. 2: (a) Differential resistance (dV/dI) of the JJ as a function of bias current and gate voltage. (b) Two line traces of panel (a) at V_G = 1 and -1.5 V shown in blue and red, respectively.

(dark blue) becomes narrower and reaches zero at V_G = -3 V. Figure 2b shows the differential resistance as a function of bias current extracted from panel (a). The line traces in blue and red are for V_G = 1 V and -1.5 V, respectively. The critical current shows hysteresis behavior. For example, at V_G = 1 V exhibiting -2 μA on the hot branch and 2.7 μA on the cold branch. We observe several peaks and valleys in the region above the critical current that are interpreted as multiple Andreev reflection processes [32, 33]. These observations verify a nearly ballistic transport in the exposed semiconductor region and a high transparency boundary with the superconducting contacts. In each Andreev reflection, two electrons are transferred across the junction and contribute to the current to drop the resistance, with peaks in resistance corresponding to transitions between successive orders of reflection processes in the high-transparency limit [32]. These reflections are observed across the whole range of gate voltages and only disappear around V_G = -2.5 V, just above when supercurrent in the JJ ceases, V_G = -3 V.

Figure 3a shows the d.c. transport measurement of voltage versus bias current as a function of top gate voltage. This V-I characteristic demonstrates an unperturbed JJ behavior due to h-BN. As the gate is used to deplete the 2DEG, by tuning the gate voltage from 3 V to -2 V in 1 V steps, (b) I_c,cold R_n as a function of gate voltage for samples A (c) R_n as function of gate voltage for sample A with h-BN and sample B with AlO_x dielectrics. (d) I_c,cold as function of gate voltage for samples A with h-BN, and sample B with an AlO_x dielectrics.
the $I_c R_n$ products for sample A. The trend is very similar to JJ devices with AlO$_x$ dielectrics [31].

For comparison we provide data from sample B with 40 nm of AlO$_x$ dielectric. Figure 3c makes a comparison between gate dependence of normal resistance (at high current bias) of two JJ-FETs with h-BN (sample A) and AlO$_x$ (sample B) dielectric. Sample B shows a smaller normal resistance compared to Sample A which suggests a higher density for Sample B. There is growing evidence that AlO$_x$ increases the density of a bare sample by 20-30% compared to ungated van der Pauw devices [36]. We interpret this increase as originating from additional carriers at the surface due to a chemical reaction of the AlO$_x$ dielectric with III/V compound materials [37].

The gate efficiency of the device can also be evaluated by plotting supercurrent as a function of electric displacement field (to normalize for different thicknesses and dielectric constants of h-BN and AlO$_x$) which is shown in Fig. 3d. Although the supercurrent is smaller in h-BN devices, the overall $I_c R_n$ are comparable due to higher $R_n$ in h-BN devices as discussed above. Another feature here is that using h-BN the supercurrent can be turned off faster, requiring nearly half the electric displacement field compared to a standard AlO$_x$ dielectric, despite the much smaller relative permittivity of h-BN. This efficiency is advantageous for low power cryogenic electronics as well as tunable quantum circuits in which the coupling is controlled by tuning the frequency of the resonators or qubits [38][39].

By applying an external magnetic field to the junction, the critical current of the junction is found to follow a characteristic Fraunhofer pattern. As illustrated in Fig. 4 for sample A, the differential resistance oscillates as a function of the out-of-plane magnetic field. The pattern is periodic with a double-width central lobe, which suggests that the current is distributed uniformly in the junction and is not affected by distortion or wrinkles in the h-BN dielectric. We observe a slight increase of the period with the magnetic field which we attribute to the reduction of the field focusing effect caused by the Al contacts. Similar observations have been reported in Ref. [40] and can be attributed to the large width of our contacts.

In conclusion, we have demonstrated the gate tunability of Al-InAs JJ-FET using a 2D material gate stack. We have used h-BN as the gate dielectric with a graphite gate. Through a van der Waals mediated pick-up fabrication process, we have successfully transferred mechanically exfoliated thin films with minimal interfacial contamination. These JJ-FETs exhibit $I_c R_n$ values comparable to those gated by AlO$_x$ dielectric with higher $R_n$ values, suggesting minimal perturbation of the InAs 2DEG by the gate dielectric through unintentional doping and surface chemical reactions. These results demonstrate that h-BN provides a superior gate dielectric compared to AlO$_x$ for JJ-FET devices with applications in superconducting logic [41] and quantum information technologies.

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