Capacitances Extraction for Multilayer Conductor Interconnect In Integrated Circuits

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Abstract: The incessant evolution towards greater densities of circuit integration, with faster signals, reduced noise margins, numerous levels of interconnections have opened up possibilities for integration. The topology of the tracks obtained by masking or laser engraving implies the need to treat a wide range of interconnections, which, always with the aim of increasing the integration density, have their geometric dimensions reduced along the axis of their width. With the technological evolution towards small dimensions, the surfaces each other between interconnections become proportionately larger. The parasitic capacitances between the conductors are thus reinforced. The present paper deals with the analysis approach for capacitance extraction for multilayer conductor interconnect. In this study, we design three geometry for conductor transmission lines interconnect we have identified the potential distributor and we computed the capacitance and inductance matrix using the finite element method then compare the results with some methods in previous publication.

Keywords: Interconnects, Transmission line, Capacitance, Inductance, Multiconductor

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1. Introduction

When designing and implementing integrated circuits, consideration should be given to the existence of parasitic capacitances between the interconnection lines and to providing methods for sufficiently reducing the influence of capacitive coupling either in led or radiated and improve their insensitivity to attacks from outside, to ensure safe operation, in all cases of use [1]. The modeling of all high performance systems, such as the design of integrated circuits is based on numerical capacitance and inductance field calculation methods; capacitance calculation has drawn the attention of IC designers to the complexity of interconnection networks. The simulation tools must make it possible to define an overall specification of the system to be studied, but the difficulty lies in passing on the noise margins on the system [2]. Transmission interconnect lines have been investigated for many years. In [3] starting from several reasonable approximations, closed-from expression for the mutual impedance per unit length of coupled IC interconnects with silicon substrate have be proposed [4], analysis of multiconductor quasi-TEM transmission lines and multimode waveguide is done. We can mention, finite difference methods (FDM) [5], Variational method [6], the method of moment [7], the Green’s function approach [8], the Galerkin method [9], Finite Element Method [10].

In this work, we design two deferent geometry of line interconnect in two dielectric region. The models are designed in 2D using finite element method in order to compare our results with some of the other available methods.

2. Materials and Methods

The capacitance coefficients for a system of parallel microstrip lines are defined as follows, it is convenient to write [11]:

\[ Q_i = \sum_{j=1}^{n} C_{sj} V_j \]  \hspace{1cm} (1)

Where \( V_j \) is the voltage of \( j \) th conductor with reference to the ground plane, \( Q_i \) is the charge per unit length, \( C_{sj} \) is the short circuit capacitance between \( i \) th and \( j \) th conductor. The short circuit capacitances can be obtained either from measurement or from numerical computation [12-13]. We obtain:

\[ C_{ij} = \sum_{j=1}^{n} C_{sj} \]  \hspace{1cm} (2)

\[ C_{ij} = -C_{si}, i \neq j \]  \hspace{1cm} (3)

Where \( C_{ij} \) is the capacitance per unit length between the \( i \) th conductor and the ground plane. The coupling capacitances are illustrated in Figure 1.

The capacitance can be calculated as follows

\[ C = \frac{2W_e}{V^2} \]  \hspace{1cm} (4)

Where \( W_e \) is the dielectric energy given by:
\[ W_c = \iint \varepsilon_0 \varepsilon_r |E|^2 \, dx \, dy \]  \hspace{1cm} (5)

![Diagram](image1.png)

Fig.1. The per unit length capacitances of general n conductor

The matrix \([c]\) capacitance for n conductor is given by

\[
C = \begin{bmatrix}
C_{11} & -C_{12} & \ldots & -C_{1n} \\
-C_{21} & C_{22} & \ldots & -C_{2n} \\
\vdots & \vdots & \ddots & \vdots \\
-C_{n1} & -C_{n2} & \ldots & C_{nn}
\end{bmatrix}
\]  \hspace{1cm} (6)

\[
[L] = \mu_0 \varepsilon_0 [C_0]^{-1}
\]  \hspace{1cm} (7)

Where,

\([L]\) = Inductance matrix.

\([C_0]^{-1}\) = the inverse matrix of the capacitance of multiconductor transmission line when all dielectric constants are set equal to one.

\(\mu_0\) = permeability of space or vacuum.

\(\varepsilon_0\) = permittivity of free space or vacuum.

The characteristic impedance and capacitance per unit length are related as follows:

\[
Z = \sqrt{\frac{[L]}{[C]}}
\]  \hspace{1cm} (8)

The electrical parameters are:

Capacitance per unit length matrix (\([C]\) in pF/m), inductance per unit length (\([L]\) in nH/m), impedance ([Z] in \(\Omega\)).

To illustrate and validate the new proposed formulation, in the first section we consider a planar interconnects line including four strips, Figure (2) shows the geometry of the model.

This microstrip coupled interconnects have the following geometrical parameters:

- \(w_1 = w_2 = w_3 = w_4 = 20 \mu m, S = 20 \mu m, h = 40 \mu m, t = 5 \mu m, \varepsilon_1 = 11.7, \varepsilon_2 = 3.9\)

![Diagram](image2.png)

Fig.2. Symmetric microstrip coupled interconnect

The figure 3 show mesh by finite element, the basic approach of the finite element method is to subdivide the field of study into finite numbers of subdomains called elements. The approximation of the unknown is done in each element of the interpolation functions. The interpolation function is also defined according to the geometry of the element that is chosen beforehand and coincides with the nodes of this element relative to the values of the unknown.

![Diagram](image3.png)

Fig.3. Mesh of four strip conductor system

![Diagram](image4.png)

Fig.4. Surface potential distribution of four strip conductors system
The capacitance per unit length of the multistrip transmission lines are related as follows:

\[
C = \begin{bmatrix}
0.968 & -0.328 & -0.08 & -0.01 \\
-0.328 & 1.126 & -0.325 & -0.08 \\
-0.08 & -0.325 & 1.126 & -0.328 \\
-0.01 & -0.08 & -0.328 & 0.968
\end{bmatrix}
\]

Table 1 shows the FEM results for the self capacitance per unit length of the fourth conductor transmission lines interconnect with two dielectric layer. They are compared with Galerkin method.

Table 1. Capacitance matrix of the model in figure 2

| Capacitance (10^{-10} F/m) | Galerkin method | Our work |
|----------------------------|----------------|----------|
| C_{11}                    | 0.475          | 0.968    |
| C_{12}                    | -0.582         | -0.328   |
| C_{13}                    | -0.114         | -0.08    |
| C_{14}                    | -0.062         | -0.01    |
| C_{22}                    | 0.289          | 1.112    |

The inductance per unit length matrix is:

\[
L = \begin{bmatrix}
0.1063 & 0.0381 & 0.0220 & 0.0117 \\
0.0381 & 0.1025 & 0.0387 & 0.0219 \\
0.0220 & 0.0387 & 0.1025 & 0.0381 \\
0.0117 & 0.0219 & 0.0381 & 0.1062
\end{bmatrix}
\]

The impedance per unit length matrix is:

\[
Z = \begin{bmatrix}
0.3846 & 0.3182 & 0.2699 & 0.2160 \\
0.3166 & 0.3957 & 0.3287 & 0.2706 \\
0.2683 & 0.3286 & 0.3963 & 0.3198 \\
0.2144 & 0.2702 & 0.3196 & 0.3884
\end{bmatrix}
\]

In the second parts we consider a planar interconnects line including four strips with two levels systems, Figure (5) shows the geometry of the model.

Table 2. Capacitance matrix of the model in figure 5

| Capacitance (10^{-12} F/m) | MoM | Our work |
|----------------------------|-----|----------|
| C_{11}                    | 7.158 | 6.921    |
| C_{12}                    | -1.284 | -1.251   |
| C_{13}                    | -1.296 | -1.312   |
| C_{14}                    | -2.224 | -2.104   |
| C_{22}                    | 8.732  | 8.602    |
| C_{23}                    | 13.39  | 12.86    |
| C_{44}                    | 14.11  | 14.01    |
Table 2 shows the FEM results for the self capacitance per unit length of the fourth conductor transmission lines interconnect with two dielectric layers. They are compared with Moment method.

The inductance per unit length matrix is:

\[
L = \begin{bmatrix}
0.2125 & 0.1016 & 0.0683 & 0.0676 \\
0.1016 & 0.2619 & 0.1226 & 0.1019 \\
0.0683 & 0.1226 & 0.1473 & 0.0599 \\
0.0676 & 0.1019 & 0.0599 & 0.1245 \\
\end{bmatrix}
\]

The impedance per unit length matrix is:

\[
Z = \begin{bmatrix}
0.7629 & 0.7553 & 0.6077 & 0.5786 \\
0.7553 & 0.9686 & 0.7539 & 0.6942 \\
0.6077 & 0.7539 & 0.6359 & 0.5479 \\
0.5786 & 0.6942 & 0.5479 & 0.5533 \\
\end{bmatrix}
\]

In this part we have to demonstrate the effect of the geometry of the interconnection track on the values of parasitic capacitance. We consider the same geometry for the figure (2) and figure (5). The calculation of the matrix \([C]\) for the given cut is made by making varies some parameters. The parameters studied are:

- \(t\), thickness of the track varying from 5 to 10 \(\mu\)m
- \(h\), height of the oxide, ranging from 40 to 100 \(\mu\)m

Table 3. The values of the parameters, five case were simulated

| Parameters (\(\mu\)m) | Case   |
|-----------------------|--------|
|                       | 1  | 2  | 3  | 4  | 5  |
| \(w\)                 | 20 | 20 | 20 | 20 | 20 |
| \(s\)                 | 60 | 60 | 60 | 60 | 60 |
| \(t\)                 | 5  | 10 | 5  | 10 | 5  |
| \(h\)                 | 40 | 40 | 80 | 80 | 100|

All abilities decrease with distance to the ground plane. This evolution can be explained by the fact that we combine the increase of the distance between the track, in order to locate an optimum layer thickness corresponds to the thickness for which the parasitic capacitance-to-capacitance ratio mass is the lowest.

3. Conclusion

In this paper, we have identified the potential distribution of different geometries of the interconnection lines and the capacity matrix and the inductance for each of the geometries have been calculated. Some geometric parameters have also been varied in order to remedy the problems of parasitic capacitances. We have found that as the thickness of the dielectric layer increases, parasitic capacitances between tracks increase with interconnect levels, and the higher the interconnect level, the lower the capacitances towards the ground plane.
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