Deployment Architectures for Cyber-Physical Control Systems

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Abstract—We consider the problem of how to deploy a controller to a (networked) cyber-physical system (CPS). Controlling a CPS is an involved task, and synthesizing a controller to respect sensing, actuation, and communication constraints is only part of the challenge. In addition to controller synthesis, one should also consider how the controller will work in the CPS. Put another way, the cyber layer and its interaction with the physical layer need to be taken into account.

In this work, we aim to bridge the gap between theoretical controller synthesis and practical CPS deployment. We adopt the system level synthesis (SLS) framework to synthesize a state-feedback controller and provide a deployment architecture for the standard SLS controller. Furthermore, we derive a new controller realization for open-loop stable systems and introduce four different architectures for deployment, ranging from fully centralized to fully distributed. Finally, we compare the trade-offs among them in terms of robustness, memory, computation, and communication overhead.

Notation and Terminology: Let $\mathcal{RH}_\infty$ denote the set of stable rational proper transfer matrices, and $z^{-1}\mathcal{RH}_\infty \subset \mathcal{RH}_\infty$ be the subset of strictly proper stable transfer matrices. Lower- and upper-case letters (such as $x$ and $A$) denote vectors and matrices respectively, while bold lower- and upper-case characters and symbols (such as $u$ and $\Phi_u$) are reserved for signals and transfer matrices. Let $A_{ij}$ be the entry of $A$ at the $i$th row and $j$th column. We define $A^*$ as the $i$th row and $A^{*j}$ the $j$th column of $A$. We use $\Phi_u[r]$ to denote the $\tau$th spectral element of a transfer function $\Phi_u$, i.e., $\Phi_u = \sum_{r=0}^{\infty} z^{-r} \Phi_u[r]$.

We briefly summarize below the major terminology:

- **Controller model**: a (linear) map from the state vector to the control action.
- **Realization**: a control block diagram/state space dynamics based on some controller model.
- **Architecture**: a cyber-physical system structure built from basic components.
- **Synthesize**: derive a controller model (and some realization).
- **Deploy/Implement**: map a controller model (through a realization) to an architecture.

I. INTRODUCTION

We consider a linear time-invariant (LTI) system with a set of sensors $s_i, i = 1, \ldots, N_x$ and a set of actuators $a_k, k = 1, \ldots, N_u$, with plant dynamics

$$x[t + 1] = Ax[t] + Bu[t] + d_x[t]$$

where $x[t] \in \mathbb{R}^{N_x}$ is the state vector, $u[t] \in \mathbb{R}^{N_u}$ is the control, and $d_x[t] \in \mathbb{R}^{N_x}$ is the disturbance. Suppose the system is open-loop stable, i.e., $(zI - A)^{-1} B \in \mathcal{RH}_\infty$. The goal of this paper is to address how a state-feedback controller can be deployed to this system and what the corresponding cyber-physical structures and trade-offs are.

A model-based approach to control design involves two phases: the synthesis phase and the deployment phase, as illustrated in Fig. 1. In the synthesis phase, the control engineer derives the desired controller model by some synthesis algorithm based on a model of the system dynamics, a suitable objective function, and operating constraints on sensing, actuation, and communication capabilities. The optimal controller in the model-based sense is thus the model achieving the best objective value.

Synthesizing an optimal controller for a cyber-physical system is, in general, a daunting task. Recently, a framework named system level synthesis (SLS) was proposed to facilitate distributed controller synthesis for large-scale (networked) systems [1]–[3]. Instead of designing the controller itself, SLS directly synthesizes desired closed-loop system responses subject to system level constraints, such as localization constraints [4] and state and input constraints [5]. Using the closed-loop system response, SLS derives the optimal linear controller model, which admits multiple (mathematically equivalent) control block diagrams/state space realizations (or simply realizations) [2], [6].

On the other hand, the deployment phase (often referred to as implementation) is concerned with how to map the derived controller model/realization to the target system. We can usually implement one controller realization by multiple different deployment architectures (or simply architectures). Although all architectures lead to the “optimal” controller,
they can differ in aspects other than the objective, for example; memory requirements, robustness to failure, scalability, and financial cost. Therefore, it is important to consider the trade-offs among those architectures, in order to deploy the most suitable architecture.

Approaches to deployment vary greatly in the literature. In the control literature, most work gives the controller design at the realization level and implicitly relies on some interface provided by the underlying CPS for deployment [7], [8]. Providing the appropriate abstraction and programming interface is itself a design challenge [9]–[12]. Some papers also examine the deployment down to the circuit level [13], [14]. The networking/system community, on the other hand, mostly adopts a bottom-up instead of a top-down approach to system control. It usually involves some carefully designed gadgets/protocols and a coordination algorithm [15]–[17].

In this work we take an alternative approach to deployment, which lies between the realization and the circuit level. Rather than binding the design to some specific hardware, we advocate for a modular approach, which lies between the realization and the circuit level. This approach is particularly well suited to modular architectural components, which can be easily mapped our architectures to the real CPS – as long as the system supports all basic functions. It is the flexibility of the SLS approach which makes such a process possible.

The paper is organized as follows. In Section II, we briefly review system level synthesis, propose a new, simpler control realization, and show it is internally stabilizing. With this realization, we propose four different partitions and their corresponding deployment architectures in Section III, namely, the centralized (Section III-B), global state (Section III-C), naive and memory conservative distributed (Section III-D) architectures. Then, in Section Section IV we discuss the trade-offs made by the architectures on robustness, memory, computation, and communication. Finally, we conclude the paper with possible future research directions in Section V.

II. SYNTHESIS PHASE

We briefly review the SLS method for the distributed control synthesis phase. Then we describe two “standard” SLS controller realizations and draw attention to their respective architectures for the deployment phase. Finally, we derive a new controller realization for open-loop stable systems which we will show in later sections has many favorable properties in the deployment stage.

A. System Level Synthesis (SLS) – An Overview

To synthesize the state-feedback closed-loop controller for the system described in (1), SLS introduces the system response \( \{ \Phi_x, \Phi_u \} \) transfer matrices. The system response is the closed-loop mapping from disturbance \( d_X \) to state \( x \) and control action \( u \), under the feedback policy \( u = K x \). Compactly this is written as

\[
\begin{bmatrix}
    x \\
    u
\end{bmatrix} =
\begin{bmatrix}
    \Phi_x \\
    \Phi_u
\end{bmatrix} \begin{bmatrix}
    d_x
\end{bmatrix},
\]

where \( \{ \Phi_x, \Phi_u \} \) have the realizations \( \Phi_x = (zI - A - BK)^{-1} \) and \( \Phi_u = K(zI - A - BK)^{-1} \). It was shown in [2] that the set of all achievable internally stabilizing controllers is parametrized by an affine subspace.\(^3\) Using this property, system level synthesis problem takes the form:

\[
\begin{align*}
\text{minimize} & \quad g(\Phi_x, \Phi_u) \\
\text{s.t.} & \quad [zI - A - B] \begin{bmatrix}
    \Phi_x \\
    \Phi_u
\end{bmatrix} = I \\
& \quad \Phi_x, \Phi_u \in z^{-1}RH_\infty \\
& \quad \begin{bmatrix}
    \Phi_x \\
    \Phi_u
\end{bmatrix} \in S.
\end{align*}
\]

As long as \( g \) is a convex functional, and \( S \) defines a convex set, the SLS problem (2) is convex. For details on how classical optimal control problems can be formulated in this manner, as well as many other aspects of SLS, the reader is referred to [3, §2.2]. The constraint set \( S \) is used to provide spatial and temporal locality to the closed-loop response. This is typically done by enforcing sparsity on the spectral components of \( \{ \Phi_x, \Phi_u \} \) and making them finite-impulse-response (FIR) filters. Full details can be found in [3], [4].

With (2) solved, a stabilizing controller is readily obtained from the system response:

\[
K = \Phi_u \Phi_x^{-1}.
\]

The controller above is useful for theoretical purposes. However, inverting \( \Phi_x \) is undesirable in most cases as it is heavily dependent on conditioning, and all the structure that \( \Phi_x \) has will likely be lost. Indeed, a controller realization based on the block diagram in Fig. 2 is more suitable for distributed control. In state space, it takes the form:

\[
\begin{align*}
\hat{x}[t+1] &= \sum_{\tau \geq 1} \Phi_x[\tau] \delta[t + 1 - \tau], \\
u[t] &= \sum_{\tau \geq 2} \Phi_u[\tau] \delta[t + 2 - \tau],
\end{align*}
\]

where \( -\hat{x} \) is the output of the \( I - z\Phi_x \) block. This controller is a disturbance-rejection controller as the signal \( \delta \) estimates the disturbance signal \( d_x \). From a realization perspective, this is better than realizing (3) by a single block. Unlike (3), which inverts \( \Phi_x \), any structure imposed on \( \{ \Phi_x, \Phi_u \} \) is inherited by the two blocks in Fig. 2, i.e., closed-loop constraints are passed on to the controller. One of the main contributions of this paper is to show that there is another controller realization, which, from a deployment perspective, may be more economical to implement whilst maintaining the desirable properties of (4).

B. A Simpler SLS Controller Realization

We have seen in the previous section how the distributed controller obtained form \( \Phi_x \) and \( \Phi_u \) can be realized. To give a bit more insight into this design, observe that

\[
K = \Phi_u \Phi_x^{-1} = (z\Phi_u)(z\Phi_x)^{-1}.
\]

\(^3\)Recent work has shown the equivalence between the SLS closed-loop parameterization and the well-known Youla parameterization [18].
The realization in Fig. 2 then follows by putting \( z\Phi_u \) in the forward path and realizing \((z\Phi_x)^{-1}\) as the feedback path through the \( I - z\Phi_x \) block.

Although the design in Fig. 2 is straightforward, and certainly preferable to direct implementation via (3), we note that two convolutions are required to construct \( u[t] \). Furthermore, the memory required to hold the convolution kernels grows rapidly with horizon length (of the FIR constraint in \( S \)) and number of system states \([6]\). We will show that when the plant is open-loop stable, we can simplify the design by replacing a convolution with two matrix-multiplies as in Fig. 3. In Section III-B we carry out an explicit cost comparison between the architectures resulting from Fig. 2 and Fig. 3.

**Theorem 1.** Let \( A \in \mathbb{R}^{N_x \times N_x} \) in (1) be Schur stable. The dynamic state-feedback controller \( u = Kx \) realized via

\[
\begin{align*}
\delta[t] &= x[t] - Ax[t - 1] - Bu[t - 1], \\
u[t] &= \sum_{\tau \geq 1} \Phi_u[\tau] \delta[t + 1 - \tau],
\end{align*}
\]

is internally stabilizing and is described by the block diagram in Fig. 3.

**Proof.** To derive block diagram in Fig. 3, observe that any feasible \( \{\Phi_x, \Phi_u\} \) pair satisfies (2), which implies

\[
\Phi_x = (zI - A)^{-1}(I + B\Phi_u).
\]

In other words, the information of \( \Phi_x \) is already encoded in \( \Phi_u \). Substituting (6) into the transfer function \( K = \Phi_u\Phi_x^{-1} \), we have

\[
K = \Phi_u(I + B\Phi_u)^{-1}(zI - A) = (z\Phi_u)(I + z^{-1}B(z\Phi_u))^{-1}(I - z^{-1}A).
\]

The block diagram follows immediately from (7). The time domain dynamics (5) are obtained from an inverse z-transform.

To prove internal stability, additional perturbations are added to the closed-loop, and it is shown that they decay with time. Consider the plant and controller connected in feedback as in Fig. 4. It is sufficient to examine how the internal states \( x, u, \) and \( \delta \) are affected by those external signals. The signals are related via the following equations:

\[
\begin{align*}
zx &= Ax + Bu + dx, \\
u &= (z\Phi_u)d + du, \\
\delta &= -z^{-1}B(z\Phi_u)d + (I - z^{-1}A)x + d\delta,
\end{align*}
\]

which, after rearranging, gives

\[
\begin{bmatrix} x \\ u \\ \delta \end{bmatrix} = \begin{bmatrix} \Phi_x \\ \Phi_u \\ I + \Phi_uB \\ z\Phi_u \end{bmatrix} \begin{bmatrix} (zI - A)^{-1}B(z\Phi_u) \\ I \end{bmatrix} \begin{bmatrix} dx \\ du \\ d\delta \end{bmatrix},
\]

where \( \Phi_x = (zI - A)^{-1}(I + B\Phi_u) \). If all nine entries in the transfer matrix above are stable, then the (bounded) injected signals \( dx, du, \) and \( d\delta \) produce bounded signal \( x, u, \) and \( \delta \), which implies internal stability. By assumption, \((zI - A)^{-1}B\) is stable, and (2) constrains \( \Phi_x, \Phi_u \) to \( z^{-1}R\mathcal{H}_\infty \). It is then easy to verify stability of all nine entries, thus proving the system is internally stable.

The advantage of Fig. 3 is that it uses only one convolution \( z\Phi_u \). Also, when \( \Phi_u \) has finite impulse response (FIR) with horizon \( T \), we have

\[
u[t] = \sum_{\tau = 1}^{T} \Phi_u[\tau] \delta[t + 1 - \tau]
\]

regardless of whether \( \Phi_x \) is FIR or not.

We remark that it is possible to internally stabilize some open-loop unstable systems by the controller in Theorem 1 (Fig. 3). Consider a decomposition of the system matrix such that \( A = A_u + A_s \) where \( A_u \) is unstable and \( A_s \) is Schur stable. Then using the robustness results from \([19]\), the controller designed for \((A_s, B)\) will stabilize \((A, B)\) if \( \|A_u\Phi_x\| < 1 \) for any induced norm.

**III. DEPLOYMENT ARCHITECTURES**

We now explore the controller architectures for the deployment phase. The crux of our designs centers on the partitions of the controller realization described in Theorem 1 and illustrated in Fig. 3. We first introduce the basic components. Using those components, we propose the centralized, global
state, and distributed architectures accordingly. As long as
the real system is capable of providing the basic components
(or some equivalent parts), mapping the architectures into
the system is straightforward.

A. Basic Components

We assume that the nodes in the target system are capable
of performing the functions shown in Fig. 5. These functions
cover variable storage, arithmetic computation, and commu-
nication. Below we describe these functions in details.

The essential component is a buffer. A buffer is where
the system keeps the value of a variable. It can be a memory
device such as a register or merely a collection of some buses
(wires). On the other hand, a delay buffer is the physical
implementation of $z^{-1}$ in a block diagram, which keeps the
variable received in the current time step and releases its
value in the next time step.

For computation, a multiplier with a matrix $A$ senses the
variable in a targeted buffer and multiplies it by $A$ as the
output. An adder performs entry-wise addition of two vectors
or matrices of compatible dimensions. Although an adder is
a two-input component, we can merge cascaded adders into
a multiple-input adder in practice.

A node can also communicate with other nodes through
dissemnator-collector pairs. A disseminator sends some
parts of a variable to designated nodes. At the receiving
side, a collector assembles the received parts appropriately
to reconstruct the desired variable.

B. Centralized Architecture

The most straightforward deployment architecture is the
centralized architecture, which partitions the block diagram
as in Fig. 6. It packs all the control functions into one
node, the centralized controller. The centralized controller
maintains communications with all sensors and actuators to
collect state information and dispatch the control signal.

Fig. 7 shows the architecture of the centralized controller.
For each time step $t$, the controller first collects the state
information $x_i[t]$ from each sensor $s_i$ for all $i = 1, \ldots, N_x$.
Along with the stored control signal $u$, the centralized con-
troller computes $\delta[t]$ as in (5a), $\delta[t]$ is then fed into an array
of delay buffers and multipliers to perform the convolution
(5b) and generate the control signals. The control signals
$u_k[t]$ are then sent to each actuator $a_k$ for all $k = 1, \ldots, N_u$.

Deploying a synthesized solution to the centralized archi-
tecture is simple: We take the spectral components $\Phi_u[\tau]$ of
$\Phi_u$ from $\tau = 1, 2, \ldots$ and insert them into the array of the
multipliers. Also, $A$ and $B$ are adopted directly from the
system model.

We can compare the centralized architecture of Fig. 3 with
the architecture of the original block diagram Fig. 2, which
is shown in Fig. 8. As mentioned in Section II, the original
architecture (Fig. 8) is expensive both computationally and
storage-wise. Specifically, when both $\Phi_x$ and $\Phi_u$ are FIR
with horizon $T$, the original architecture depicted in Fig. 8
performs
\[
\frac{(T-1)N_x^2 + TN_x N_u }{ \Phi_x[\cdot]\delta[\cdot] } \quad \text{scalar multiplications per time step and needs}
\]
\[
\begin{array}{c}
\Phi_x[\cdot] \\ \Phi_u[\cdot] \\ \Phi_u[\cdot] \\ \Phi_u[\cdot] \\ \Phi_u[\cdot] \\
\end{array}
\]
\[
\delta[\cdot], \ x[t], \ -\bar{x}[t+1], \text{ and } u[t]
\]
scalar memory locations to store all variables and multipliers.
On the other hand, Fig. 7 performs
\[
\begin{array}{c}
N_x^2 + N_x N_u + \frac{T}{\Phi_u[\cdot]} \\
-A x[t] \quad \text{and} \quad -B u[t]
\end{array}
\]
\[
\frac{1}{\Phi_u[\cdot]\delta[\cdot]}
\]

\[
(8)
\]
C. Global State Architecture

To avoid overloading the centralized controller, we can offload the computations to the nodes in the system, which results in the global state architecture. Fig. 9 shows the partitions of the block diagram. We have a centralized global state keeper (GSK) which keeps track of the global state \( \delta[t] \) instead of the raw state \( x[t] \) at each time step \( t \). Rather than directly dispatching the control signals \( u[t] \) to the actuators, GSK supplies \( \delta[t] \) to the actuators and relies on the actuators to compute \( u[t] \).

We illustrate the details of each node in Fig. 10. GSK collects \( \delta_i[t] \) from each sensor \( s_i \). To compute \( \delta_i[t] \), each \( s_i \) stores a column vector \( -A^* \). Using the sensed state \( x_i[t] \), \( s_i \) computes \( -A^{ij} x_j[t] \) and sends it to \( s_j \). Meanwhile, \( s_i \) collects \( -A^{ij} x_j[t] \) from each \( x_j \) and \( -B^{ik} u_k[t] \) from each \( a_k \). Together, \( s_i \) can compute \( \delta_i[t] \) by

\[
\delta_i[t] = x_i[t] - A^{ij} x_j[t+1] - B^{ik} u_k[t+1] = x_i[t] - \sum_j A^{ij} x_j[t+1] - \sum_k B^{ik} u_k[t+1].
\]

The \( \delta'[t] \) term is then forwarded to each actuator by GSK. The actuator \( a_k \) can compute the control signal using the multiplier array similar to the structure in the centralized architecture. The difference is that each actuator only needs to store the rows of the spectral components \( \Phi_k[\tau] \) of \( \Phi_u[\tau] \). After getting the control signal \( \delta_k[t] \), \( a_k \) computes \( -B^{ik} u_k[t] \) for each sensor \( s_i \).

One outcome of this communication pattern is that \( s_i \) only needs to receive \( -A^{ij} x_j[t] \) from \( s_j \) if \( A^{ij} \neq 0 \). Similarly, only when \( B^{ik} \neq 0 \) does \( s_i \) need to receive information from \( a_k \). This property tells us that the nodes only exchange information with their neighbors when a non-zero entry in \( A \) and \( B \) implies the adjacency of the corresponding nodes (as shown in Fig. 14(b)). Notice that this property holds for any feasible \( \{\Phi_k, \Phi_u\} \), regardless of the constraint set \( S \).

The global state architecture mitigates the computation workload of the centralized architecture and hence improves the scalability. However, this architecture is subject to a single point of failure – the GSK. Therefore, we explore some decentralized architectures in the following subsection.

D. Distributed Architectures

To avoid the single point of failure, we can either reinforce the centralized unit by redundancy or deconstruct it into multiple sub-units, each responsible for a smaller region. Here we take the latter option to an extreme: We remove GSK from the partitions of the control diagram (Fig. 9) and distribute all control functions to the nodes in the network.

A naive way to remove GSK from the partitions is to send the state \( \delta'[t] \) directly from the sensors to the actuators,

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Fig. 9. The partitions of the block diagram for the global state architecture.
\[ \delta_i[t] \text{ from each } s_i \rightarrow \delta[t] \rightarrow \text{ to each actuator} \]

(a) The architecture of the global state keeper (GSK).

\[ -A^{\gamma}x_i[t] \]
\[ -A^{\gamma}x[t] \]
\[ -B^{\gamma}u[t] \]

(b) The architecture of each sensor \( i (s_i) \).

\[ \delta[t] \text{ from each } s_j \rightarrow \delta(t-1) \]
\[ \vdots \]
\[ \Phi_{\gamma}^1[t] \]
\[ \Phi_{\gamma}^2[t] \]
\[ \Phi_{\gamma}^3[t] \]
\[ \text{⋯} \]
\[ -B^{\gamma}u_k[t] \text{ from each } a_k \]

(c) The architecture of each actuator \( k (a_k) \).

At the actuator \( a_k \), the control signal \( u_k[t] \) is given by the sum of the convolution results from each sensor:

\[ u_k[t] = \sum_{\tau \geq 1} \Phi_{\gamma}^k[\tau] \delta_i[t + 1 - \tau] \]

\[ = \sum_i \sum_{\tau \geq 1} \Phi_{\gamma}^k[\tau] \delta_i[t + 1 - \tau]. \]

To confirm that Fig. 12 is more memory efficient than Fig. 11, we can count the number of scalar memory locations in the corresponding architectures. Since both architectures store the matrices \( A, B, \Phi_u \) in a distributed manner, the total number of scalar memory locations needed for the multipliers is

\[ N_x^2 + N_x N_u + TN_x N_u. \]  

(10)

We now consider the memory requirements for the buffers. Suppose \( \Phi_u \) is FIR with horizon \( T \) (or, there are \( T \) multipliers in the \( z\Phi_u \) convolution). In this case Fig. 11 has the same architecture as Fig. 10 without the GSK. Therefore, the
total number of stored scalars (buffers) is as follows:

At each \( s_i: N_x + 4 \),
At each \( a_k: (T + 1)N_x + 1 \),

Total: \( N_x(N_x + 4) + N_u((T + 1)N_x + 1) \)
\[ = (T + 1)N_xN_u + N_x^2 + 4N_x + N_u. \quad (11) \]

On the other hand, the memory conservative distributed architecture in Fig. 13 uses the following numbers of scalars:

At each \( s_i: N_x + N_u + T + 3 \),
At each \( a_k: N_x + 1 \),

Total: \( N_x(N_x + N_u + T + 3) + N_u(N_x + 1) \)
\[ = 2N_xN_u + N_x^2 + (T + 3)N_x + N_u. \quad (12) \]

In sum, the memory conservative distributed architecture requires fewer scalars in the system, and the difference is \( (T - 1)N_x(N_u - 1) \), which is non-negative since \( T, N_x, \) and \( N_u \geq 1 \).

Future work will look at specializing the above computation/memory costs to specific localization constraints. The above expressions serve as upper bounds that are tight for \((d, T)\)-localization defined in [4]). For systems localizable to smaller regions, the actuators only collect local information, and hence we don’t need every sensor to report to every actuator.

IV. Architecture Comparison

As mentioned at the beginning of Section III, different architectures implementing the same controller model allow the engineer to consider different trade-offs. Here we compare the proposed architectures and discuss their differences. Our findings are summarized in Table I.

In terms of robustness, the centralized and the global state architectures suffer from a single point of failure, i.e., the loss of the centralized controller or the GSK paralyzes the whole system. This also makes the system vulnerable from a cyber-security perspective. On the contrary, the distributed architectures can still function with some nodes knocked out of the network.\(^2\)

For information storage, the centralized controller uses the fewest buffers, and the global state architecture stores the most variables (because its GSK has to relay \( \delta(t) \)). We remark that although the centralized scheme achieves the minimum storage usage at the system level, the single node memory requirement is high for the centralized controller. Conversely, the other architectures store information in a distributed manner, and a small memory is sufficient for each node.

We evaluate the computational load at each node by counting the number of performed multiplication operations. The centralized architecture aggregates all the computation at the centralized controller, while the other architectures perform distributed computing. For distributed settings, the computation overhead is slightly different at each node. The global state and naive distributed scenarios let the actuators compute the convolution. Instead, the memory conservative distributed architecture puts the multiplier arrays at the sensors.

Finally, we discuss the communication loading of the architectures. In Fig. 14, we sketch the resulting cyber-physical structures of each scheme. The centralized architecture ignores the underlying system interconnection and installs a centralized controller to collect information and dispatch control actions. Under this framework, the sensors and the actuators only need to recognize the centralized controller, but the centralized controller must keep track of all the nodes in the system, which limits the scalability of the scheme.

The global state architecture also introduces an additional node into the system, the GSK, with which all nodes should be contact with. Meanwhile, the sensors and actuators also communicate with each other according to the matrices \( A \) and \( B \). In other words, if two nodes are not directly interacting with each other in the system dynamics, they don’t need to establish a direct connection.

Similarly, in the distributed architectures, the sensors and the actuators maintain connections according to \( A \) and \( B \). Additionally, direct communications, which are governed by the structure of \( \Phi_u \), are added to replace the role of GSK. Although it would be slightly more complicated than having a GSK as the relay, we can localize \( \Phi_u \) at the synthesis phase to have a sparse communication pattern.

Besides the centralized architecture, the physical structure has a direct influence on the cyber structure in all other architectures. As such, we believe further research on the deployment architectures of SLS would lead to better cyber-physical control systems.

V. Conclusion and Future Directions

A new internally stabilizing state-feedback controller was derived for systems that are open-loop stable. The controller was shown to have a block diagram realization that is in some ways simpler than the “standard” SLS state-feedback controller.

We considered various architectures to deploy this controller to a real CPS. We illustrated and compared the memory and computation trade-offs among four different deployment architectures: centralized, global state, naive distributed, and memory conservative distributed architectures.

Future work involves removing the open-loop stability requirement and considering the output-feedback setting. Also, as pointed out in Section III-D, there are still many decentralized architecture options left to explore. For example, in addition to the distributed schemes, one can install multiple local controllers to form clustered architectures and employ localization constraints to limit information exchange among clusters.

References

\(^2\)The system operator might need to update \( \Phi_u \) to maintain performance – such a re-design is well within the scope of the SLS framework.

[1] J. C. Doyle et al., “System level synthesis: A tutorial,” in Proc. IEEE CDC, 2017.
TABLE I
COMPARISON AMONGST THE PROPOSED ARCHITECTURES

| Property                        | Centralized (Fig. 6) | Global State (Fig. 9) | Naive Distributed (Fig. 11) | Memory Conservative Distributed (Fig. 12) |
|---------------------------------|-----------------------|-----------------------|-----------------------------|------------------------------------------|
| Single Point of Failure         | yes                   | yes                   | no                          | no                                       |
| Overall Memory Usage            | lowest (see (9))      | highest (equal to (10)+11)+N_x) | second highest (equal to (10)+11) | second lowest (equal to (10)+12)         |
| Single Node Memory Usage        | high                  | low (actuator needs more memory) | low (actuator needs more memory) | low (sensor needs more memory)          |
| Single Node Computation Loading | high (see (8))        | low (actuator performs convolution) | low (actuator performs convolution) | low (sensor performs convolution)        |
| Single Node Communication Loading | sensor/actuator: low controller: high | sensor/actuator: medium GSK: high | sensor/actuator: high, but localizable | sensor/actuator: high, but localizable |

Fig. 14. The cyber-physical structures of the proposed architectures. The horizontal dashed line separates the cyber (top) and the physical (bottom) parts of the system. Each solid node represents a computation unit, and the arrow links are the communication channels. The dotted lines associate the computation units with their locations. The cyber structure of the centralized architecture is ignorant about the underlying physical system, while the other architectures manifest some correlations between the cyber and the physical structures. The distributed architectures (naive and memory conservative) replace GSK by direct communications, which can be trimmed by imposing appropriate localization constraints on $\Phi_{\mathbf{A}}$ during the synthesis phase.

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