STBPU: A Reasonably Safe Branch Predictor Unit

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Abstract—Modern processors have suffered a deluge of dangerous side channel and speculative execution attacks that exploit vulnerabilities rooted in branch predictor units (BPU). Many such attacks exploit the shared use of the BPU between unrelated processes, which allows malicious processes to retrieve sensitive data or enable speculative execution attacks. Attacks that exploit collisions between different branch instructions inside the BPU are among the most dangerous. Various protections and mitigations are proposed such as CPU microcode updates, secured cache designs, fencing mechanisms, invisible speculations. While some effectively mitigate speculative execution attacks, they overlook BPU as an attack vector, leaving BPU prone to malicious collisions and resulting critical penalty such as advanced micro-op cache attacks. Furthermore, some mitigations severely hamper the accuracy of the BPU resulting in increased CPU performance overhead. To address these, we present the secret token branch predictor unit (STBPU), a branch predictor design that mitigates collision-based speculative execution attacks and BPU side channel whilst incurring little to no performance overhead. STBPU achieves this by customizing inside data representations for each software entity requiring isolation. To prevent more advanced attacks, STBPU monitors hardware events and preemptively changes how STBPU data is stored and interpreted.

I. INTRODUCTION

Over the last few decades, a large number of protection techniques against software attacks have been introduced making exploitation of traditional attack vectors such as code injection or return-oriented programming challenging. With a decreasing number of available targets for software attacks, the attention of adversaries is more frequently drawn to exploitable weaknesses in hardware. Although hardware attacks such as microarchitectural side channels [1], [3], [6], [19], [26], [44], [56], [57], covert channels [17], [24], [49], [54], and power analysis [2], [34], [48], [50], [55] have been known for a long time, only recently did researchers demonstrate the true power of microarchitectural attacks with newly discovered speculative execution attacks, such as Meltdown [42], [73] and Spectre [13], [32], [33], [35], [47], [67]. These attacks are based on speculative (transient) execution, a performance optimization technique present in nearly all of today’s processors. While this technique improving CPU performance, with a carefully crafted exploit, it completely undermines memory protection, giving unauthorized users the ability to read arbitrary memory [33], [42] and disable crucial protections [32].

Microarchitectural attacks are possible because performance optimizations such as caches, prefetchers, and various predictors were not traditionally designed with security in mind. For example, data structures used to implement these mechanisms are commonly shared, making various conflicts possible. Some conflicts result in leakage of sensitive data. One such mechanism is the branch predictor unit (BPU). Substructures within the BPU are typically shared, and the stored data is compressed, prone to various branch collisions. [15], [64]. This enables attacks such as side channels [2], [16], [18] that are capable of leaking encryption keys or bypassing ASLR, and the recently introduced speculative execution attacks [32], [33]. At the same time, shared BPUs are beneficial for performance. They allow high utilization of hardware structures to reduce the cost and enable efficient branch history accumulation. [52]. Therefore, naïve protections which disable sharing or flush BPU structures have high performance overhead. Recent Intel microcode updates introduced as a countermeasure against Spectre attacks [27] demonstrated that the overhead from naïve protections can be as high as 440% [58], [71].

Despite significant efforts directed towards designing other secure microarchitectural components e.g., caches [14], [31], [43], [63], [76], [78], [80] and memory buses [4], [40], [66], secure BPU designs remain a handful of attempts [20], [38], [77]. More importantly, none of existing approaches completely eliminate BPU vulnerabilities, such as recent µop caches attacks [65]. We propose Secret-Token Branch Prediction Unit (STBPU), a safe BPU design aimed to protect against collision-based BPU attacks and eliminate BPU side channels. STBPU prevents collision-based side channel and speculative execution attacks by disallowing software entities from creating controlled branch instruction collisions and thus affecting each other in an unsafe way. This is done by customizing the branch representation for each software entity in the form of address mappings and by encrypting data stored in BPU. In STBPU, each software entity is provided with a unique, randomly-generated secret token (ST) that customizes data representations. STBPU constantly monitors active attacks with hardware events and re-randomizes STs to prevent attackers from reverse-engineering the ST tokens.

This paper makes the following contributions:

- We propose, STBPU, a safe BPU design protects against speculative execution attacks including fast algorithm attacks, provides strong isolation guarantees to eliminate to BPU side channels, and incurs low overheads.
- We provide insight on how to adapt the STBPU design, invalidating the recent µop cache attacks which can bypass mitigations e.g., invisible speculation and fencing.
- We design an automated frame to create lightweight ST-dependent remapping functions and validate STBPU with in-depth security analysis.
We evaluate STBPU performance on advanced prediction mechanisms e.g., TAGE_SC_L and Perceptron and show low overhead even with extreme security settings.

II. BACKGROUND & RELATED WORKS

A. STBPU’s motivation and scope

Figure 1 lays two main groups of BPU-centered speculative execution attacks: collision-based e.g., spectre-w2 and history-based e.g., spectre-v1 utilizing different BPU properties. The first group exploits branch collisions (aliasing) that appear when two branch instructions located at different addresses map into the same BPU entry and affect each other’s behavior (target). As depicted in Figure 1 in dotted circles, existing secure BPU designs and enhancements tend to resolve these attacks but all have incomplete protection coverage or unsupported performance. We provide detail in §II-D.

The second group exploits the most fundamental property of BPU, to record branch’s statistics and then activate speculative execution based on such statistics. This makes BPU trainable by attackers via providing branch execution history. These attacks are often mitigated by non-BPU protections, including secured cache designs [60], [79], [81]; shadow structures to hide the effects of erroneous speculative executions [30], [82]; tracking speculative data flow for invisible speculations [41], [61], [84] and offline gadget detectors [21], [53], etc.

Depicted as solid square in Figure 1 non-BPU protections trying to cover both groups of attacks often introduce high costs on performance and resource. More importantly, they overlook BPU as an attack vector i.e., BPU is still prone to collisions, resulting critical penalty in security. For instance, researchers recently discovered micro-op cache (also called decoded stream buffer, DSB) as disclosure primitive [65]. Depicted as lightest grep area in Figure 1. This new timing channel can leverage BPU for more powerful transient execution attacks that do not require implicit or explicit data access, bypassing several existing mitigations such as STT [84] and context-based fencing [72] and voiding their security guarantee on both spectre-v1 and spectre-v2.

The incompleteness in protection motivates us to propose STBPU, a safe BPU design that is immune to collision-based attacks and BPU side channels and lifts non-BPU protections’ inherent overhead towards all-around security. As depicted as the dash-dotted circle, STBPU focuses on protecting collision-based attacks but is not limited to it. The aforementioned new µop-cache attacks are interesting cases, showing the STBPU design can mitigate more powerful spectre-v1 variant.

In i see dead µop attack variant 2 [65], an attacker first prime certain micro-op cache sets and performs Spectre-v1 type of mis-training on a authorization check and a followed transmitting indirect branch instruction in a victim method. Next, attacker enters untrusted input. The authorization check will fail. If enabled, non-BPU mitigations such as fencing or speculative data flow control will restrict the followed instructions from dispatch or being visible. However, they do not prevent this secret-dependent indirect branch from being speculatively fetched, further leaving a footprint in the micro-op cache. As a result, the attacker can probe the micro-op cache set and infer the secret. On the other hand, such attacks become inapplicable with the STBPU design of DSB. This is due to ST remapping makes DSB indexing non-deterministic. As a result, on both priming and probing stage, the attacker loses the control on both the entry branch address and DSB set mapping even within the same address space.

DSB caches stream decoded micro-ops from multiple decoders after the branch prediction stage, making it naturally applicable to use ST remapped address for its own indexing without additional latency. As DSB is enabled only through branch [28], a consistent isolation can be maintained via ST remapping and ST re-randomization. We analyze similar mechanism with more complicated BPU attacks in §VI. Since STBPU substructure modification will be detailed in §IV, we omit the DSB discussion detail as it is similar and simpler.

History-based attack such as Spectre-v1 leverages the correlation between the natural consequence of prediction and the unsafe follow-up front-end acceleration. Thus, we believe Spectre-v1 mitigation should be outside of BPU such as by existing non-BPU protections, an orthogonal safe speculative execution control, or a safe loop stream detection (LSD) unit. STBPU benefits these protections by largely reduce their surface of enforcement, granting better performance.

The rest of this paper will focuses on collision-based attacks and BPU side-channels. Evidenced by a large number of well-documented dangerous exploits, they are responsible from critical data leakage to speculatively executed arbitrary code. We categorize dangerous exploits and their mechanisms in §II-C and analyze the security STBPU against them in §VI.

B. BPU Baseline Model

Below we present a baseline BPU as an example to illustrate our STBPU design in practice. The baseline reflects the branch predictor (including structure sizes) used in Intel Skylake microarchitecture. Derived based on recent reverse-engineering works [16], [18], [33], [36], [46], [85], it represents a generalization of mechanisms used in modern Intel processors. STBPU can be applied to different branch predictors, e.g., [68], [69], as it adds security guarantees without altering any prediction principles. We demonstrate this by adapting the STBPU to protect several advanced predictors such as...
TAGE-SC-L [70] and Perceptron [29] and show negligible performance overheads in their STBPU-protected alternatives (with STP prefixes) in §VII.

The BPU consists of the following main structures: shift registers such as the global history register (GHR) and branch history buffer (BHB), branch target buffer (BTB), pattern history table (PHT), and return stack buffer (RSB). Different structures are used in combination to generate predictions dependent on specific branch types. Figure 2 depicts how these structures are utilized during a BPU lookup with highlighted components that are modified by STBPU. The figure also shows several important functions which are referenced later.

**Shift registers** such as GHR and BHB are used in the BPU as a low-cost way of retaining complex branch history. GHR stores the global history of taken/not-taken branches. BHB is used by the indirect predictor to store compressed branch address history for indirect branches. It is used as part of BTB access to predict targets that depends on both branch virtual address and branch context (of previously executed branches). When a branch is executed, its virtual address is folded using XOR and mixed with the current state of BHB [33].

**BTB** serves the purpose of caching target addresses of branch instructions. It is implemented as an 8-way, 4096-entry table. Each entry stores a truncated address of the 32 least significant address bits of the target. Function 5 is then utilized to convert a 32-bit entry into a 48-bit virtual address during prediction by combining 16 higher bits from the branch instruction pointer with 32 lower bits from BTB. While the BTB is used to store targets for all branch types, it has two addressing modes. In mode one, the virtual address of a branch instruction is used to compute an index and tag. In mode two, in addition to virtual address, the BHB is used to perform a lookup. Mode two is only used when predicting indirect branches, and serves as a fall-back mechanism for predicting returns. This addressing enables storing multiple targets for a single indirect branch depending on the context [16], [33], [85].

**PHT** is a large (16k entry) table consisting of n-bit (e.g. 2-bit) saturating counters; each counter implements a simple FSM with states ranging from strongly non-taken to strongly-taken. This structure is used as a base predictor to predict the direction of conditional branches. Previous studies [7], [18], [25], [85] indicated presence of mechanism similar to gshare [83] with two modes of addressing: the simple 1-level mode where virtual address of branch is used to find a PHT entry, and a more complex 2-level mode where the branch virtual address is hashed with global history register (GHR) enabling accurate prediction complex patterns.

**RSB** is used to predict return instructions. The RSB is implemented as a fixed size (16-entry) hardware stack [36], [46]. A call instruction pushes a return address on the RSB and a return instruction pops it. Similarly to the BTB, RSB stores only 32 bits of the target. Due to limited capacity, the RSB can underflow. In this case, returns are treated as indirect branches, and the indirect predictor is utilized for prediction.

**C. BPU Centered Attacks**

We detail the entire collision-based attack surface in Table I. First, we classify attacks by where adversarial effect takes place, either within the attacker’s code (home effect) or in the victim’s code (away effect). Secondly, we classify by the kind of the effect. A collision in BPU structures results in either data placed by another software entity being reused, or such data is evicted and replaced. We refer to these as reuse-based and eviction-based attacks. The table summarizes attacks caused by BPU collisions and their steps. Please note that there can be different adversarial effects enabled by same type of collision. For instance, a collision in BTB between two different branches can result in 1) BTB-data reuse, 2) BTB-eviction and 3) activating malicious speculative execution. While 1) and 2) results in side channel leakage of branch-related information 3) is used as part of speculative execution attack to reveal victim’s memory contents. As can be seen from the table, there is a diverse range of dangerous collision-based attacks. STBPU, while eliminating collision-based BPU attacks, can substantially improve security properties of microprocessors.

There are two BPU features that are present in nearly all CPUs that make collision-based attacks possible. First, the BPU data structures are shared among all software executed on a CPU core, enabling branch collisions between different processes. Second, the BPU operates with compressed virtual addresses. For instance, out of 48 bits of branch virtual address, only 30 are utilized. Then, these bits are further compressed [33]. This allows branch collisions within the same virtual address space such as collisions between different branches in kernel and user process [16]. The deterministic nature of the BPU makes it possible for an attacker to controllably trigger collisions. Our proposed solution aims at eliminating such determinism to prevent attacks.

**D. Existing Protections Against BPU Attacks**

Branch predictor collision-based attacks can be mitigated in several ways. While some protections may be more specific and cover only certain attack scenario, others may provide protection from multiple attacks. For instance to avoid leaking secret key bits from RSA secret key operation, one can rewrite the exponentiation calculation code to avoid secret-key dependent branches [5]. If branch predictor is flushed on context switch attacks such as Spectre v2, Jump-over-ASLR and others can be fully mitigated.
Intel has proposed a set of microcode-based protections which aim to mitigate speculative execution attacks on legacy CPUs by restricting BPU structure sharing. These protections include Indirect Branch Restricted Speculation (IBRS), Indirect Branch Prediction Barrier (IBPB), and Single Threaded Indirect Branch Prediction (STIBP) [27]. IBRS prevents higher level processes from speculating with entries provided by lower level processes by flushing. IBPB provides protection by flushing the contents of the BPU on context switches. While effectively removing the interference from the branch prediction on other processes, flushing the BPU removes useful history, resulting in high performance reduction [58], [71]. Additionally, recent research demonstrated exploitable branch collisions within same address space [65], [85]. Therefore enforcing security only during context switch is not complete. STIBP logically segments the BPU so that branch prediction of on the same physical assemblage does not interfere with each other. In contrast, STIBP works regardless of context switch activity. We choose to compare performance of STBPU to protection mechanisms derived from such protections as they, when properly activated, can provide strong BPU isolation.

Figure 1 shows that existing secure BPU designs are limited in protection surface and performance support. Brb [77] stores and reloads the entire history of the directional predictor for each process which only defends against BranchScope. Exynos security enhancement [20] also utilizes XOR-based encryption on branch predictor. However, this approach only protects/encrypts target information and only on indirect branches and returns that not only allows both high-efficiency branch poisoning and BPU side-channel attacks. Although, Exynos generates CONTEXT_HASH via multiple entropy sources, the computation is deterministic and requires levels of hashing and iterative entropy spreading, which not only leaves rooms for offline replay attacks but introduces a latency of multiple cycles. BSUP [38] first encrypts the PC and then encrypts the entries of BPU. This design is not applicable to SMT scenario, and it differs from our work as we create new remapping functions to prevent separate software entities from interfering with each other. In addition, the key randomization schemes in BSUP and Exynos lack in consideration of critical kinds of adversarial effects, making both of them vulnerable to many attacks [2], [12], [59], [61], [65].

| Attack steps | Home effect (HE) | Away effect (AE) | Home effect (HE) | Away effect (AE) |
|--------------|-----------------|-----------------|-----------------|-----------------|
| BTB:         | 1: V; jmp s → d; BTB ← (s, d) | 1: V; jmp s → d; BTB ← (s, d) | 1: A; jmp s → d; BTB ← (s, d) | 1: A; jmp s → d; BTB ← (s, d) |
| PHT:         | 1: V; jnt s → d; PHT ← (s, t) | 2: V; jnt s → d; PHT ← (s, t) | 2: V; jnt s → d; PHT ← (s, t) | 2: V; jnt s → d; PHT ← (s, t) |
| RSB:         | 1: V; call s → d; RSB ← (s + 1) | 2: V; call s → d; RSB ← (s + 1) | 2: V; call s → d; RSB ← (s + 1) | 2: V; call s → d; RSB ← (s + 1) |
| A sees misprediction | 3. V speculatively executes d | 3. V speculatively executes d | 3. V speculatively executes d | 3. V speculatively executes d |

**TABLE I:** Attack surface classification for BPU collision-based attacks by event and adversarial effect types

### III. Threat Model

We assume a powerful attacker that has a complete understanding of all hardware components and structures in the STBPU. The attacker has access to normal reverse engineering recourses, such as time measurements and performance counters, and has access to a wide variety of hardware covert channels. The STBPU design calls for new special purpose registers as detailed in Figure 4, the adversary is assumed to be unable to read/modify the contents of these registers. Such role is delegated to a privileged software entity (OS, hypervisor) which attacker does not control.

We consider attacks presented in Table I including both side channel attacks in which victim executes a sensitive data dependent branch branch as well as speculative execution attacks where victim is forced to speculatively execute leakage gadget code. We assume the following two attack scenarios:

**Sensitive Process as Victim** In this scenario, an attacker tries to learn sensitive data from a victim process by manipulating the BPU state and recording observations. The attacker has control over user-level process co-located on the same CPU core and is capable of performing activities that are normally allowed to untrusted process such as accessing fine grain hardware timers via rdtscp instructions. We assume the victim and attacker can either execute on two virtual cores within same physical core or share the same logical core with time-slicing. This scenario also includes recently introduced transient trojans [85] where collisions occurring within the same memory segments are exploited.

**Kernel/VMM as Victim** The attacker takes a form of a software entity with lower privilege level, i.e. untrusted user process. The attacker tries to learn sensitive data owned by a higher privileged entity (OS kernel or VMM) by manipulating with BPU state and recording observations. Here, victim and
attacker share same contiguous virtual address space. Attacker is restricted from executing privilege instructions.

IV. STBPU DESIGN

As discussed in [II], BPU attacks are possible due to deterministic mapping mechanisms, allowing attackers to create branch collisions. STBPU aims to stop these attacks by replacing these deterministic mechanisms with key remapping mechanisms which prevent branch collision construction. The design philosophy of STBPU is to create different data representations for separate software entities inside BPU data structures. Each software entity requiring isolation is assigned a unique secret token (ST), which is a random integer that controls how branch virtual addresses are mapped into BPU structures. This ST is also used to encrypt/decrypt stored data. Compared to naïve protections based on flushing or partitioning, our approach has a number of benefits.

Consider a protection scheme where branch target poisoning is prevented by flushing the BTB on context switches. Invalidating the entire branch target history will negatively affect performance in cases where context switches are frequent. Similarly, to protect from target collisions between kernel and user branches, BTB must be flushed on mode switches (e.g. all syscalls). Partitioning hardware resources reduces the effective capacity of BPU structures resulting in a higher miss rate and lower prediction accuracy. Instead, a customized mapping approach allows separate software entities to co-exist in the BPU with minimal performance overhead; performance evaluated in [VII]. STBPU utilizes two key approaches to enable safe resource sharing. First, we ensure that collision creation is challenging by ensuring all remapping functions are dependent upon both branch address and ST. Second, STBPU detects when a potential attacker process has recovered sufficient information that enables deterministic collision creation by monitoring hardware events. The ST of the current process in the BPU is rerandomized once certain (OS controlled) thresholds are reached. Note that in STBPU design, the OS is trusted and is responsible for setting parameters such as re-randomization threshold. This is a common assumption for systems protecting against microarchitectural attacks since compromising OS gives the attacker full control over system making the side channel attack non-necessary. STBPU can be also adapted for systems with OS not trusted (e.g. SGX), then another system component, such as enclave entering routine can be given access to ST. Alternatively simple logic of ST management in STBPU should also enable hardware only implementation. Re-randomizing ST effectively resets the customization the BPU data representation for that process. Although branch history is lost in this case (by making it unusable), our analysis indicates that such events are infrequent. Re-randomizing the ST of one process does not remove the stored history of a process with a different ST. This is the key difference comparing to flushing-based approaches. We derive the re-randomization thresholds through the analysis in [VI].

While potentially dangerous, branch history sharing between programs can benefit performance. Consider a server application which spawns a new process for each incoming connection. Since each process executes the same code, data accumulated in the BPU can be used by the newly spawned process; this allows the new process to avoid costly BPU training because the history of the parent process was retained. STBPU permits selective history sharing by allowing OS to provide multiple threads of the same program to utilize the same ST value. However, when sharing is not desired, each thread (or child process) can be assigned its own ST.

A. Hardware Mechanisms and Interfaces

To design a secure BPU having comparable performance and hardware cost, we restrict ourselves to only modifying BPU mapping mechanisms, adding registers, and encrypting stored targets. The minimalistic nature of proposed changes will facilitate adaptation of our approach. In our design, each logical (hyperthreaded) core is provided with an extra register to store the ST of the current process. Only the OS is allowed to read/modify these registers, and these registers are inaccessible in unprivileged CPU mode. As such, the OS facilitates history retention across context/mode switches by loading the appropriate STs. We also add several MSRs that store thresholds and counters for automatic ST re-randomization. These MSRs monitor the events that indicate an active attacker process. We monitor two events: 1. branch mispredictions which includes incorrectly predicted direction of conditional branches and targets of any branch, and 2. BTB evictions. In [VI], we explain how these events are utilized to deter BPU attacks. Initially, the counter values are set to their respective threshold values. When an event is observed, the corresponding counter is decremented. When a counter reaches zero, the current ST is re-randomized, and the CPU reset the counter with the threshold value. The OS treats these registers as a part of software context saving, and recovering their values on context/mode switches. Modern CPUs have embedded high performance pseudo-random number generators [45]. We propose using these for efficient ST re-randomization.

The ST register is a 64-bit register divided into two 32-bit chunks, $\psi$ and $\varphi$. The first chunk $\psi$ acts as a key for a keyed remapping functions making BPU mapping unique for each process. We replace functions 1, 2, 3 and 4 in Figure 2 with STBPU remappings $R_{1\ldots4}$ accordingly. We add functions $R_t$ and $R_p$ that are used for STBPU implementation with TAGE and Perceptron predictors. Both baseline and STBPU remapping functions reduce input data (address, BTB, GHR bits) into fixed size index, tag, and offsets used by the BPU to perform lookups. [V-B] describes how $R_{1\ldots4,t,p}$ were selected.

| Baseline input | STBPU input | Output | Function |
|---------------|-------------|--------|----------|
| $s$           | $\psi, 48$  | $t$    | $R_{1(80 \rightarrow 22)}$ |
| $58$ bits     | $32, 48$    | $8$    | $R_{2(90 \rightarrow 8)}$ |
| $32$          | $32, 48$    | $14$   | $R_{3(90 \rightarrow 14)}$ |
| $18$ GHR, $32$| $32, 48$    | $14$   | $R_{3(90 \rightarrow 14)}$ |
| $32$, $L(GHR)$| $32, 48$, $L(GHR)$ | $0/15$ | $R_{4(80 \rightarrow 25)}$ |
| $48$          | $32, 48$    | $10$   | $R_{5(80 \rightarrow 10)}$ |

\(L(GHR)\) — represents geometric series of global history lengths

| TABLE II: I/O bits for baseline and STBPU functions |
Additionally, these functions utilize the entire 48-bit virtual address unlike legacy functions that use truncated address bits as inputs. This is crucial in order to prevent same address space attacks. Table II summarize all input/output bit changes between the baseline and STBPU models.

We use a XOR scheme to encrypt data stored in BPU structures to stop attackers from redirecting execution to a desired speculative gadget even if collisions occur. Instead, speculative execution will be redirected to a random (and likely invalid) address. In STBPU, every entry stored in BTB and RSB is XORed with \( \varphi \) of the current process. Note that the baseline BPU stores only 32 bits of target addresses, so the 32-bit \( \varphi \) is sufficient for encrypting all stored bits. We use simple XOR encryption for two reasons: 1. XOR operations are extremely fast with trivial hardware implementation, and 2. re-randomization of STs makes a simple XOR encryption an effective attack mitigation (discussed in §VI). To decrypt data in BTB and RSB, we modify function \( \mathcal{S} \), which XORs target bits with \( \varphi \) before extending them to 48-bit address.

V. DEVELOPMENT AND OPTIMIZATION OF REMAPPING

In §V we defined remapping functions \( R_{1,4,t,p} \) which replace the methods of calculating indices, tags, and offsets for lookup purposes in the baseline BPU model. Remapping functions \( R_{1,4,t,p} \) can be thought of as non-cryptographic hash functions. Given the size constraints of the BPU structures, collisions between different inputs to functions \( R_{1,4,t,p} \) will occur; this fact prevents functions \( R_{1,4,t,p} \) from providing cryptographic security, regardless of implementation. This inherent weakness is remedied with periodic re-randomization of STs; the security of such re-randomizations are discussed in §VI. The mapping functions used in the baseline model are not fully re-engineered, but we can safely assume some fast compression functions are used with delays of no more than 1 clock cycle. Using performance and security as our guides, we placed several important constraints upon functions \( R_{1,4,t,p} \):

C1 The compute delay for \( R_{1,4,t,p} \) must not exceed \( C \) clock cycles, where \( C \) may vary from CPU to CPU. For our purposes, we chose \( C \) to be 1 clock cycle. We enforce this by limiting transistor critical path of each function.

C2 The outputs of \( R_{1,4,t,p} \) should be uniformly distributed across their respective output spaces. (uniformity)

C3 The outputs \( R_{1,4,t,p} \) must appear to be pseudo-random, and the relationship between inputs and outputs should be non-linear. (avalanche effect \( [23] \))

A. STBPU Remapping v.s. Existing Ciphers

We analyzed existing hardware supported hashing mechanisms, but found none that satisfied our specific requirements for three main reasons: 1) Using stronger ciphers does not directly translate into better security. Existing ciphers are primarily designed to withstand known plaintext/ciphertext attacks. However, STBPU threat model is much different as attackers never observe encrypted addresses (ciphertext) nor partially matched plaintext/ciphertext. They only observe collisions (not knowing with their own or victim’s branch) and need to reverse-engineer the rest of the address bits. Besides, knowing their own STs does not provide immediate access to collision creation or simplifies collision-based attacks. In §VI we show that the number of mispredictions and evictions attackers must incur to successfully infer a ST (to deterministically poison BTB) far exceeds the thresholds that will trigger ST re-randomization. Thus, encrypting with a more advanced cipher would not increase the level of security. 2) On the other hand, more sophisticated encryption schemes introduce significant delays in CPU frontend. For instance, we explored using PRINCE-64 \( [11] \) to encrypt stored targets. While fast, PRINCE-64 will still consume multiple clock cycles and consume more energy due to higher number of gates compared to a simple subsingle-cycle XOR operation. 3) Moreover, different input/output bit requirements for various BPU mechanisms make it challenging to utilize a single hash.

Therefore, we propose a automated remapping function generation and optimization approach, enabling STBPU to compose \( R_{1,4,t,p} \) with all suitable properties.

B. Automation of Remapping Development

Automated Remap Generation Algorithm. Designing these remapping mechanisms is a multi-variable optimization problem. Therefore, we use a weighted randomization algorithm to generate possible remapping functions. Our algorithm takes in a list of hardware constraints, and generates remappings that satisfied the supplied constraints. The algorithm contains a predetermined pool of primitives to use for construction of potential remapping mechanisms. Each remapping function is iteratively generated and tested one layer at a time, where a layer is a block of these primitives. After a layer is added, the current function is tested against the supplied constraints. There are three possible scenarios that occur during each round of testing. 1) The current design satisfies all constraints, and subsequently stored for later optimization. 2) The current design violates one or more constraints, and is discarded. 3) The current design does not outright violate the constraints, but is incomplete. In case 3, our algorithm changes the weights used for primitive selection during the creation of the next layer to better improve the current design.

Constraint Selection of \( C_1 \). Our algorithm requires an input of several variable constraints for the generated remapping functions to satisfy \( C_1 \). These constraints are: the maximum count of transistors along the critical path, the maximum number of transistors in parallel (breadth), the maximum number of total transistors for the design, the number of input and output pins, the maximum number of functional layers (blocks) the design can have, and the maximum number of wires an arbitrary wire can cross over.

Modern processors are designed to perform 15-20 gate operations in a single cycle \( [60] \), which translates to roughly 30-45 transistors along the critical path. The delay incurred by each transistor in the critical path is relatively independent of the CPU clock cycle; therefore, the faster the CPU’s clock cycle, the smaller the number of transistors that can be completed within 1 clock cycle. Therefore, 45 transistors
is the absolute maximum number of transistors we allow in the critical path with preference set for shorter critical paths. **Primitive Selection.** Much research has been conducted into cryptographic hash primitives [9], [10], [57], [86], [87] that provide building blocks for hash functions with strong properties. We leverage these primitives from SPONGENT [10] and PRESENT [9] hashes. Out of those S-boxes (establishing non-linearity by substations) are perhaps most critical. To increase the simplicity of remapping function generation, we separate primitives into two categories: non-invertible compression primitives and mixing primitives.

Non-invertible primitives tend to employ XOR logic gates to obfuscate the relationship between input and output. For many such primitives, multiple inputs generate the same, smaller output which makes reverse-engineering difficult. Combining multiple non-invertible layers increases complexity of attacks aiming to pair a known output to an unknown input. These primitives compress input size $|m|$ to an output size $|n|$ where $|m| > |n|$. Table II shows the disparity between the input and output sizes for $R_{1, 4, t, p}$ functions, and indicates the need for optimized compression primitives. Mixing primitives are primarily used to introduce non-linearity to a hash design which makes deterministically changing the output by varying the input difficult. These primitives are primarily composed of $|m| \rightarrow |n|$ sized S-boxes and P-boxes (performing permutations). Since the hardware complexity of S-boxes increases superlinearly with the size of $|m|$, we limit our S-boxes to a maximum of 4 input/outputs. These S-boxes can be implemented efficiently with combinatorial logic or transistor/diode matrices. P-boxes are constrained by the maximum wire crossover set for the algorithm.

**Validation of Uniformity (C2) and Avalanche Effect (C3)**

Remappings that satisfy the hardware constraints are then tested against constraints C2 and C3. We first employ the balls and bins analysis and compute the coefficient of variation (CV) of bins to approximate the uniformity (C2) of the output space [62], [23] is satisfied when a remapping adheres to a strict avalanche criterion. To quantify the avalanche effect of $F$, for each input $\lambda$, we generate a set of unique inputs, $S$, where each input in $S$ differs from $\lambda$ by a single bit flip. We then compute the hamming distance between $F(\lambda)$ and $F(S_i)$, for all inputs in $S$. Using these hamming distances, we determine the CV of the hamming distances for a particular $\lambda$. We test each $F$ with 1 million random inputs and compute the average hamming distance for all inputs. The ideal case occurs when: i) the average hamming distance over 1 million random inputs is roughly 50%. ii) For all inputs, the CV of the average hamming distance for each input is 0. iii) For all bit positions of an output of $F$, the difference between the min and max hamming distances for a bit flip in any bit position is 0.

**C. Optimization and Remapping Selection**

The final selection of remapping functions $R_{1, 4, t, p}$ is primarily based upon the results of the previous tests. The result is a multiobjective optimization problem where the ideal state for different desired metrics may be maximized or minimized. To make all metrics comparable, we normalized each metric so that the optimal value is 0. We then considered this to be a simple weighted optimization problem where we seek functions that yield the lowest sum of all metrics recorded when testing for uniformity and the avalanche effect. Let $F$ be a particular function in the group of potential functions $G$ for remapping function $R_i$, for $i \in R_{1, 4, t, p}$.

$$\min \sum_{i} w_i \cdot g(F), F \in G$$

All weights were set to 1 to avoid prioritizing one metric over another. Further prioritizing then can be done by hardware developers for a specific CPU design. For space reasons, we do not show the designs for all of $R_{1, 4, t, p}$ since they share many similar characteristics. Instead, we show the chosen design for $R_1$ in Figure 3 where stages 1, 3, and 5 are substitution layers using $4 \rightarrow 4$ and $3 \rightarrow 3$ S-boxes. For space reasons, not all types of S-boxes are shown. Under the design of $R_1$, we show the logical mappings for S-boxes used by PRESENT and SPONGENT. P-boxes are $n \rightarrow n$ in size with the pin mappings generated randomly by our remap function generator. C-S boxes are compression structures that map $|m|$ bits to an output size of $|n|$ bits where $|m| > |n|$. This design of $R_1$ has a critical path length of 36 transistors, so it is capable of being computed within a single clock cycle.

**VI. Security Analysis**

Introduced in §III an attacker has a complete working knowledge of all STBPU remapping functions, a full control of execution flow, and being capable of executing branches to/from any address in the attacker’s address space. The goal of the attack is to enable a malicious branch instruction collision that allows to mount one of the attacks presented in §II. STBPU makes collisions non-deterministic forcing the attacker to either rely on brute force approach to find collisions or to reverse-engineer the ST value. We assume attacker utilizing recently proposed fast attack algorithms such as GEM [61] and PPP [59], designed to attack randomized caches.

An attacker possessing knowledge of their ST ($\psi/\phi$) voids the security provided by the STBPU because they can deterministically generate outputs with any of the remapping
functions used by the STBPU. Table III shows which attacks benefit from knowledge of ST. Table IV consists of a few terms used in the analysis. Branch collisions are unavoidable due to the extreme compression required by $R_{1..4..t,p}$. This weakness is alleviated with periodic rerandomization of ST for individual processes. Several important axioms to consider:

A1 Attacker do not know the numerical outputs of $R_{1..4..t,p}$.
A2 Due to $\mathbf{A1}$ all the current state of the STBPU must come from detection of mispredictions and evictions.
A3 Attacker does not have inherent knowledge or control of ST of any process.

A. STBPU Attacks

The attacks described in [II] become considerably more complex to execute without knowledge of ST used during execution of the attacker or the victim. These attacks can be mitigated with targeted rerandomization of ST after a certain number of mispredictions or evictions in the BPU have occurred due to $\mathbf{A2}$.

1) Target Injection Attacks: Recall that we encrypt the targets stored in the STBTB and STRSB through the following means: $E_A = \varphi_a \oplus \tau_A$. With Spectre V2, the attacker supplies a malicious $\tau_A$ using branch $A$ that collides with the victim’s branch $V$ causing $V$ to speculate with $\tau_A$. With the SpectreRSB, the attacker places a malicious return address $\tau_A$ on the stack that the victim speculates with. In both cases, the target the victim will use from the STBTB or STRSB is determined by $\tau_A$. If there is a Spectre gadget located in the victim’s address space at address $G$, the attack is successful if $\tau_V = G$. Due to $\mathbf{A2}$, the attacker does not have control of $\varphi_a$ or $\varphi_v$; consequently, the only variable the attacker can change is the address of $\tau_A$ on the stack that the victim speculates with. In both cases, the target the victim will use from the STBTB or STRSB is determined by $\tau_A$.

2) Reuse-based Attacks: Address mappings are randomized so that there is only a probability that an arbitrary $A$ and $V$ will collide in the STBPU. Even though $A$ and $V$ are mapped with $R_{1..4..t,p}$, the probability that attacker branch $A$ collides with victim branch $V$ in the STBTP-STPHT is not bound by birthday complexity because $V$ is a static, specific address. The probability of collision is $P(A \Rightarrow V) = \left(\frac{1}{2}\right)^{1/2\cdot\sqrt{\tau_A}}$. Note, we break up the probability that $A$ and $V$ are in the same set vs. the probability that $A$ and $V$ have matching tag and offsets because tag/offset comparisons are only done if $A$ and $V$ are in the same set. This adds uncertainty for reuse-based side channels where the attacker wishes to determine the direction of $V$ since a lack of misprediction by $A$ or $V$ could mean that $A$ and $V$ do not collide, or that $V$ was not taken. To increase the probability that an arbitrary $A$ collides with a static $V$, the attacker can execute a set of branches $S_B = \{b_1, ..., b_n\}$ where $n$ is large so that one branch in $S_B$ might collide with $V$. The probability that one of the branches in $S$ collides with $V$ is $P(S_B \Rightarrow V) = \sum_{i=1}^{n} P(S_{b_i} \Rightarrow V)$. However, noise is added using this method because it is possible that branches in $S_B$ will collide with each other. The probability that two branches in $S_B$ collide can be approximated with birthday complexity because the branches in $S_B$ are arbitrary.

In order to ensure that no branches in $S_B$ collide with any other branch in $S_B$, the attacker execute the following steps: 1) Use $b_{new}$ as new address in attacker’s address space. 2) For every branch $b_i$ in $S_B$, execute $b_i$ and $b_{new}$. 3) If no MISP, between $b_i$ and $b_{new}$, $S_B = S_B \cup \{b_{new}\}$. In order to achieve a 50% probability of collision between $A$ and a branch in $S_B$, the size of $S_B$ must be $\frac{ITO}{2}$. The number of MISPs $M$ and evictions $E$ generated whilst generating $S_B$ of size $n = \frac{ITO}{2}$ can be approximated as follows:

$$M \approx \sum_{i=0}^{n} \sum_{j=0}^{i=1} \frac{1}{\sqrt{2}^2} \cdot \frac{1}{\sqrt{2}^2} = \frac{n(n + 1)}{2\sqrt{2}^2} \cdot \sqrt{2}^2$$

$$E \approx \frac{ITO}{2} - IW$$

Note the reuse-based side channel attacks on PHT do not generate evictions. The size of the STBTP is $IW$ which is significantly smaller than $\frac{ITO}{2}$, so entries in the STBTP will constantly be evicted as the attacker grows $S_B$.

Attacks such as BranchScope [18] and BlueThunder [25] are viable against processors using hybrid directional predictors largely in part due to the inclusion of a base directional predictor in these hybrid BPU’s. Due to the complexity of TAGE tables and Perceptron weights, it is significantly easier to maliciously modify the base directional predictor than the complex TAGE/Perceptron structures. Since the remapping mechanisms used in our TAGE/Perceptron structures are different than the remapping functions used for the base directional predictor, little information is gained by an attacker observing mispredictions from both the base and complex directional components. Due to $\mathbf{A1}$, an attacker will not know which TAGE bank or Perceptron weight set produced a prediction. The thresholds for rerandomization stemming from mispredictions from the directional predictor are based on the least complex attack on the directional predictor so as to also protect against more complex directional predictor attacks.

3) Same Address Space Attacks: Recently discovered same address space attacks [8] are classified as target injection attacks, but in this case both $A$ and $V$ are located inside the attacker’s address space. As such, encrypting the target of $A$ with $\varphi_a$ provides no security because $V$ will decrypt $\tau_A$ with $\varphi_a$. However, due to $R_v$, there is only a probability

| (Name: Description) | (i) Branch in attacker(A)’s address space |
|---------------------|------------------------------------------|
| Wstruct | Number of ways |
| V struct | Branch in victim(V)’s address space |
| Tstruct | Number of sets (indices) |
| $\omega_{AV}$ | AV R(1) 32-bit token |
| Tstruct | Entry tag bit entropy |
| $\varphi_A$ | AV target encryption token |
| Bstruct | Entry offset bit entropy |
| $\varphi_B$ | Target of arbitrary branch $Q$ |
| Estruct | Entry target bit entropy $Q$ |

TABLE IV: Useful IDs and Descriptions
that $A$ and $V$ will collide; this probability is the same as in \textsection VI-A2. Therefore, the number of mispredictions and evictions generated while performing a same address space attack are also approximated by Equation (2).

4) Eviction-based Attacks: The attacker cannot deterministically create STTBT eviction sets without knowing $\psi_a$ since address mappings change when $\psi_a$ is rerandomized. With $W_{stbtb}$ ways, detecting an eviction in an arbitrary set requires $W_{stbtb} + 1$ colliding branches (same index, different tag and/or offset). The attacker wants to fill STTBT sets so that if $V$ is executed, it disturbs one of the attacker’s primed sets. To increase the chances that $V$ will enter a primed set, the attacker must prime as many sets as possible. Assuming the ideal case when the attackers do not have conflicts between their own branches, they need to cover $P \cdot I$ sets to achieve $P$ probability of a successful attack. For example, the probability that $A$ enters the same set as a static $V$ is $\frac{1}{2}$, so to have a 50% chance of priming the set $V$ enters, the attacker must prime $\frac{I}{2}$ sets. Naively, the probability of randomly guessing $W_{stbtb}$ branches to form a single set of branches $S_c$ that enters the same STTBT set is:

$$P(S_c) = \frac{1}{W_{stbtb}^{I-1}} \quad (3)$$

Since this probability is not favorable, the attacker could apply a fast algorithm GEM \cite{59} to construct every eviction set. The attackers uses GEM because bottom-up strategies like PPP becomes less efficient without a partitioned randomized structure \cite{59}. We assume the ideal scenario for the attacker is when most of the branches tested follow a perfect uniformity. In this case, given a particular branch, the probability to have $W$ branches belonging to the same set is directly related to the total number of test entries. For instance, there is a 50% probability that in a group of $\frac{LW}{2}$ branches that at least $W$ branches share the same index. Thus, in order to achieve $P$ attack rate, the attacker needs to test at least $PIW$ branches as the initial set since the total attack lines in $L$ in GEM. ($L$ should be larger than 44 according the GEM). With the origin setting in GEM, the attacker sets the group size $G = W + 1$ and start to eliminate group of branches. Although the total branch accesses will be approximately $2.3 \cdot W \cdot L$, the total eviction number will be less as the majority of the probe during each iteration will be hit. Since the probability that each group will produce an eviction is approximately equal to $1 - \frac{1}{e}$. The evictions generated by testing will be negligible as $(W + 1) \cdot 1 - \frac{1}{e} \cdot n$ since the total rounds $n$ for GEM converge on the list of conflicting lines are relatively small. However, when first placing $L$ branches, the attacker has to trigger the same amount of evictions. Summarizing the procedure to construct required eviction sets above, we can now approximate evictions numbers generated whilst building sets for $P$ attack rate as follows:

$$E \approx PI \times (PIW + (W + 1) \times (1 - \frac{1}{e} \times 3) \quad (4)$$

5) Thresholds for Baseline Model: STBPU has the same parameters as the baseline Intel Skylake+ BPU. The STTBT has 8 ways and 512 sets. The stored entries have a compressed 8-bit tag and a 5 bit offset. The STPHT has 1 way and 214 sets. Using Equation (2) the number of mispredictions and evictions an attacker will likely generate to perform a successful STTBT RB side channel attack is $6.9 \times 10^8$ and $2^{31}$, respectively. Correspondingly, for an STPHT RB side channel, the number of triggered mispredictions is $\approx 838 000$. For an STTBT EB side channel, the average number of evictions required needs to be found is $\frac{1}{2}$ or $5.3 \times 10^5$ per Equation (2). For Spectre V2 and SpectreRSB, the number of mispredictions generated is $\approx 2^{31}$. To prevent attacks we use the lowest misprediction and eviction thresholds as the upper bounds for rerandomization of ST when evaluating the performance of STBPU.

B. Support for Future Attacks and Defenses

Retaining flexibility in STBPU is not only essential to keep up with evolving attacks in the security arms race but also important to improve performance with advanced defensive additions. Thus, we designate the role of ST management to system software (OS) while providing basic hardware support such as automatic even counter and ST re-randomization. The OS is responsible for setting re-randomization thresholds of each software entity, enabling it to adjust the level of security. For instance, if a process does not require BPU isolation, the OS can disable event counting. Should more optimal BPU attacks be discovered or weaknesses found in other components, the OS can reduce the thresholds forcing more frequent rerandomizations to neutralize new threats. In the extreme case, the OS can set threshold to 0 to forcing re-randomization after every BPU event. Moreover, we suggest to combine STBPU with external hardware attack detectors \cite{53}. This can further reduce STBPU cost by updating event counters only when unique attack patterns are detected.

In threat models where OS is not trusted, such as in case of SGX enclaves, the role of ST management is given to the enclave entrance routine. In this case, the code running in SGX mode is given permissions to access ST and threshold registers. Before entering the enclave and after exiting it, the ST register is zeroed out. This prevents a rogue OS from reading enclave’s ST as well as malicious enclave from spying on ST of other processes. At the same time the enclave can retain ST state between enclave activations improving performance and if necessary, re-randomize the token.

VII. Evaluation of STBPU Design

Realistically evaluating BPU design is a challenging task. First, sharing BPU resources creates various possibilities for branch conflicts affecting prediction accuracy. Moreover, in BPU designs with safety mechanisms (e.g., IBRS, IBPB), normal system activity may drastically affect performance. For instance, to avoid BPU state leakage between user processes and kernel, BPU resources need to be flushed upon context/mode switches. As a result, programs that cause frequent mode or context switches may experience worse performance comparing to standard benchmark suits that are composed of computation bound applications. Thus, a good evaluation
order to evaluate microarchitectural performance effects, we implemented the STBPU mechanisms inside gem5\cite{gem5} and conducted simulations in gem5 syscall-emulation (SE) mode using DerivO3CPU model with configurations that mimics a modern Skylake processor. The detailed specification is shown in Table\cite{table}. All gem5 simulations were performed with simulating 110 million instructions with a warm-up of 10 million instructions. We evaluate performance effects of STBPU on two simulators. We use trace-based simulator to capture system wide effects and then validate our results using detailed cycle accurate simulator. This approach provides a good coverage evaluating various performance effects.

A. Rerandomization Threshold Optimization

In §VI we demonstrate the misprediction and eviction thresholds for ST rerandomization when various STBPU attacks have \(P\) attack success rate. For BranchScope, to have a 50\% chance of success, the number of mispredictions generated is \(\approx 838\,000\). For an STBEB EB side channel, the number of evictions generated is \(\approx 5.3 \times 10^5\). These are the lowest numbers for mispredictions and evictions generated by the attacks discussed in this paper. Indeed, we would like to rerandomize ST well before the attacker has a reasonable probability of a successful attack. To do so, we utilize results from previously discussed security analysis and derive the rerandomization thresholds as follows: We first denote the attack complexity \(C\) as the least number of evictions or mispredictions that the attack needs to trigger in order to succeed the attack with 50\% chance. Please note, we use 50\% probability rather than 100\% (full brute-force) since on average the attacker will succeed with half the number of attempts needed for the full exhaustive key search. Let the variable \(r\) be the attack difficulty factor, and \(\Gamma\) be the rerandomization threshold. As such, \(\Gamma = r \cdot C\). An attack has a 50\% success rate when \(r = 1\). For instance, if \(r = 0.1\), the rerandomization thresholds for mispredictions and evictions are 83\,000 and 53\,000, while 41\,500 and 26\,500 when \(r = 0.05\). We set \(r\) to 0.05 and derive rerandomization from this value since it offers strong security guarantees with low performance impact.

B. STBPU Performance Evaluation

1) Prediction Accuracy with real branch trace: Here, we evaluate the impact on BPU accuracy from STBPU mechanisms and compare it to existing naïve protections modeled
after microcode protections and based on flushing or partitioning BPU resources. It avoids simulating the complex state of microarchitectural components. Instead, it is designed to allow a rapid testing of BPU models adopted with the STBPU design against a variety of real-world scenarios.

Each instance of simulation collected from an Intel Core i7-8550U machine captures traces from a live physical core and include any OS/library code executed including naturally occurring context, mode switches and interrupts. This allows a realistic simulation of complex cross-process BPU effects and assessing of how flushing or ST rerandomization affects performance. For single task centralized scenarios, we collect 23 SPEC CPU 2017 traces. In addition, we capture traces from user and server applications, including Apache2 workloads under different prefork settings and Google Chrome traces of running single or multiple browser workloads, etc.

Introduced in §II-B our baseline BPU model combines recent reverse-engineering insights of Intel processors [16], [18], [33], [36], [46], [85]. We applied the ST protections from [IV-A] to the baseline model for STBPU implementation. We also created two models that mimic the baseline model with Intel’s microcode-based protections namely µcode protection 1 and 2, modeling IPBP+IBRS protection with and without STIBP. Please note that microcode-based protections cannot prevent branch collisions occurring within same context. To prevent such collisions, more structural BPU changes are required. In particular, instead of storing compressed and truncated addresses in BTB, the full 48-bit address must be stored. As a result, a number of entries the BTB is capable of storing must be reduced (assuming unchanged hardware budget). We refer to such model as conservative, which fully prevents any known collision-based BPU attack by flushing or partitioning. Please note that STBPU achieve same security level, but via customizing data representations inside BPU achieving significantly better performance results.

The result from simulating the above five models is demonstrated in Figure 6 where we aggregate all the effective predictions into a single metric: overall accuracy effective (OAE) which counts a branch correctly predicted if all necessary predictions are correct (target and direction), otherwise it’s counted as mispredicted. Figure 4 shows the overall accuracy of the various BPU models against the SPEC2017 benchmarks and user applications. Combined, STBPU incurred an overall effective prediction accuracy penalty of less than 1.3%. For comparison, the microcode and the conservative BPU models suffer at least around 12% overall accuracy loss and have multiple single cases of nearly 30% reductions. With this, we conclude that microcode protections using flushing or partitioning of the BPU are too heavy-handed [22], [74], [75], and significantly reduce BPU accuracy.

2) Cycle Accurate Evaluation using gem5: Our next evaluation focuses on the comprehensive impact of STBPU on Out-of-Order (OoO) CPU in terms of cycle accurate performance, protecting advanced branch predictors, and SMT performance.

We tested three advanced BPU models: TAGE_SC_L_8KB, TAGE_SC_L_64KB [70], and PerceptronBP [29]. To demonstrate the consistency of accuracy between gem5 and our previous evaluation, we also ported and tested our baseline model in [VII-B] as SKLCond model. We compared the direction prediction accuracy between SKLCond in gem5 with our previous baseline model results on the same SPEC 2017 workloads. We observed below 5% direction prediction difference on average which validates our simulator’s consistency.

We treated the aforementioned four BPU models and implemented four STBPU models. In single process evaluations, we simulated each pair of STBPU models and their non-ST counterparts across 18 SPEC2017 workloads. Figure 5 illustrates the reduction of direction / target predictions rate and the normalized IPC between STBPU designs and their non-secure counterparts. We observe all 4 STBPU designs can achieve less than 2% reduction on average target prediction rate and less than 1.3% reduction on average of direction prediction rate. The less than 4% average IPC reduction demonstrates the high effectiveness of STBPU designs.

We used the same eight BPU models in our gem5 SMT simulations. Instead of running a single workload at a time, we...
mixed all compatible SPEC workloads in pairs and simulated together with SMT enabled. In order to fairly evaluate the STBPU impacts on overall throughput, we calculated the Harmonic means (Hmeans) of IPCs as we equally value each workload. Figure 6 displays the overall IPC and accuracy impacts. In particular, we observed the ST_SKLcond models suffers the most when SMT scenarios introduces more ST rerandomizations while it can still achieve less than 2% throughput reduction. We believe this is because ST_SKLcond model does not have a separate threshold register as TAGE models do for TAGE-table mispredictions. This results in more direction mispredictions as shown in the first chart of Figure 6 which further affect the overall performance. On the other hand, the advanced models retain their efficiencies with minimized accuracy reductions and throughput drop-downs.

3) ST Rerand. Overhead v.s. Future Attacks: Protections need to be prepared for future challenges. In microarchitecture security, such an arms race involves advanced algorithms and new hardware vulnerabilities, potentially improving attack rates by orders of magnitude. Although STBPU can maintain security by adjusting ST rerandomization frequencies (using smaller r settings), at what performance cost can be an interesting question. To explore this trade-off, we broaden the STBPU evaluation with a range of aggressive ST rerandomization thresholds, assuming any future attacks increase the efficiency to 10 times, 100 times, and even more. To demonstrate an extreme instance, we select an advanced BPU sensitive to branch history and test it under SMT scenarios that are more prone to mispredictions and evictions. Figure 7 shows the STBPU-protected Tage_SC_L BPU can retain performance above 95% until the re-randomization thresholds triggers ST update every few hundreds of mispredictions or evictions, which practically shuts down any BPU training.

We argue that the C2 constraint (uniformity) of remapping prevents STBPU from interfering with the nature of BPU’s and applications having high interference rates. On the other hand, without uncovering both attacker and victim’s STs, an attacker tends to pollute his own program with deliberately generated events like evictions, resulting in more frequent ST updates.

VIII. CONCLUSIONS & ACCESSIBILITY

We presented the STBPU, a safe branch prediction design that defends against BPU side channel and speculative execution attacks. We performed an systematization of BPU related attacks and provided a detailed security analysis of STBPU against the most recent advanced attacks. While retaining security, we demonstrate the STBPU’s high efficiency with both real-world traces and advanced BPU models. We plan to release our simulation tool, gem5 modifications, and more details in STBPU design, evaluations, and hw estimation.

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