Research on Net Weighting Schemes in Performance Driven Global Routing

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Abstract— In today’s VLSI technology nodes, interconnect delay plays an important part in deciding the performance of the chip designs. Various methods are introduced at the level of placement and routing to address this problem. To address this problem at the level of global routing, net weighting methods are being explored in the industry and academia. We investigate four methods for weighting the critical nets during performance driven global routing. This paper presents a comparative study conducted on the four methods for net weighting proposed by us in our previous works.

Keywords: FPGA Routing, Net Weighting Methods.

1. INTRODUCTION

According to Moore’s law the gate count increases twice every year. As more and more cells are added to the design, placement and routing complexity of the design increases many folds. This is primarily due to the fact that the interconnect delay becomes significant. The efficient placement and routing of the design decides the performance of the final chip. Many methods have been proposed in the literature at the level of placement of the design and also at the global routing level to address this issue. In this paper, we focus on methods to perform efficient timing driven global routing for FPGA based designs.

Timing optimization algorithms have been traditionally applied to placement problems. There are two types of approaches in the placement and routing methods, 1) Path based and 2) Net based. In path-based approaches, the critical path of the design under consideration are analyzed and optimized. These approaches are complex to analyze and difficult to implement which is primarily due to exponential number of paths in a design. Net based methods are easy to implement compare to path-based approaches and hence are very popular. Weights of nets are computed based on the criticality of the net in the design, and then these weights are applied during the run of the routing tool.

Resources present in FPGA routing architecture use segments of various lengths. Due to this reason, the traditional (as in ASIC) methods of route length estimation do not apply. Timing driven routing becomes even more difficult under such scenario.

In this paper we investigate the net weighing schemes for FPGA based designs. Our approach in this paper is based on application of weights to the critical nets during the global routing flow. We use VPR tool for our experiments with a number of FPGA designs.

Peishan Tu et al.[1] proposed a novel timing driven routing tree construction method for tradeoff between wirelength and timing. Their approach is based on shortest path trees and minimum spanning trees.

Dongsheng Wang et al.[2], proposed a method in which graph connectivity of graph is obtained at first which is based on observing Elmore delay model. This graph is known as DCG (directed connectivity graph) which describes connectivity of all the edges of the graph. They also propose a C-Tree algorithm which is a timing-driver Steiner tree routing approach.

Dongsheng Wang et al.[3] propose a new algorithm called MCM/IC multilayer routing algorithm, named MLR, which is timing driven and considers the Elmore delay as a performance issue. It also consider number of layers, total wirelength and the vias. Based on layer assignment problem, this algorithm assigns all the nets into the routing layers in a layer-pair by later-pair fashion.

Jin-Tai Yan et al.[4], proposes a simulated-annealing based approach, wherein, the input is an initial routing tree. They consider routing flexibility in a SRT and flexibility of the Steiner-point in one Y-type wire. The flexibility of the points is timing constrained. The simulated-annealing-based approach obtains a better timing-constrained flexibility-driven SRT by performing reassignment of the possible locations of the Steiner points in a SRT.

Tsung-Yi Ho et al.[5], propose a new framework for rapid multilevel routing considering performance optimization and crosstalk. To optimize performance-driven routing, they have proposed a new method of minimum-radius minimum-cost spanning tree algorithm which is applied in global routing. To reduce the crosstalk problem, they have added an intermediate stage of layer/track into their routing framework.

Fang-Jou Liu et al.[6] propose a novel timing model which is based on the layout of the design. This is based on Asymptotic Waveform Evaluation (AWE) which helps in analysis of timing paths during global routing. This computation of moments of the interconnect tree are enabled...
by this model in a bottom-up fashion, and can be integrated global router without much effort. This integration helps in layout optimization in an incremental manner, i.e., routing and timing analysis are performed simultaneously, along with exchange of information between them.

Jong Hu et al. [7], propose a method for global routing that can optimize routing delay, routing congestion, and number of bends. This approach solves problems which are competing objectives. Based on the timing constraints, routing flexibilities are obtained and used to reduce congestion given the timing constraints.

Kaushik Roy et al. [8], proposes a solution for the problem of place and route in field programmable gate arrays (FPGA’s) targeted for low power dissipation constrained by critical path delays. There is a capacitive loading for each net of the large number of unprogrammed anti-fuses present in the routing architecture. Due to signal transitions happening at the output of logic gates, a substantial amount of power gets dissipated in the routing architecture. The signal transitions within internal nodes of the circuit are estimated based on primary input signal distributions.

Jucemar Monteiro et al. [9], proposed an algorithm in which both routing metrics and timing are considered during detailed placement. They also present a detailed analysis of a score for the timing quality and the number of routing overflows. They also provide a trade-off between them and experiment their algorithm on the International Conference on Computer Aided Design (ICCAD) 2015 timing-driven contest benchmarks.

Hsiao-Ping Tseng et al. [10], propose a crosstalk and timing driven router for the task of VLSI design which is used for detailed and global routing. This method targets to process the timing constraints and crosstalk by tuning wire spacing and by performing ordering of nets and by quantitative analysis. This novel heuristic fits for detailed routing and global routing along with the flow of layout design.

Takahiro Deguchi et al. [11], present a method for performance driven routing. This method is based on a multi-layer routing model. The use linear programming in this method by considering buffer insertion and wire sizing under timing constraints. The routes for each net are determined in a hierarchical level.

Sung-Woo Hur et al. [12], this paper performs the study of the performance driven objective of maze routing. They adopt a graph model appropriate for applications to global and detailed routing. This model captures blockages naturally, limits the routing layer assignment and wire-sizing resources. The perform annotation of each edge in the graph with capacitance and resistance values pertaining to the particular wire segment. The objective is to find low resistance-capacitance delay paths or obtains a tradeoff between total capacitance and resistance-capacitance delay.

Jin-Tai Yan et al. [13], present a method for performance driven routing which is based upon the concept of assignment of hidden Steiner points and insertion of sharing buffer. This is achievable for input graph where a set of connecting nodes of a net are given. They construct a rectilinear Steiner tree which is performance driven by inserting Steiner points and sharing buffers into all possible positions that given a better performance.

Christophe Alexandre et al. [14], propose a routing tool called TSUNAMI, which is more of a platform based on an C++ database. All the tools interact with this database consistently and collaborate on the problems at hand. A timing driven global routing and a timing driven placement tool has been developed on this platform.

In Section 2, we discuss the implementation aspects of the proposed routing tool. Experiments are presented in Section 3. Finally, we present the results of our approach in Section 3 which is followed by Conclusion in Section 4.

2. IMPLEMENTATION OF THE ROUTER

We implement timing driven routing for FPGA routing architecture. A typical FPGA routing architecture is show in Figure 1.

![Figure 1: Typical FPGA Resources](image)

Algorithm 1 Method A for weighting nets

1: for All nets n do
2: for All pins p of net n do
3: pin crit = max(Criticality - net slack(p)) / Tcrit, 0
4: pin crit = pow(10, pin crit)
5: pin critical(p) = pin crit
6: end for
7: end for

Figure 2: Method A

In method B, as shown in Figure 3, in line 1 we assign Pincrit to be equal to Pincrit raised to the power of 10. After this we choose the maximum of Maxcrit and Pincrit.

Algorithm 2 Method B for weighting nets

1: for All nets n do
2: for All pins p of net n do
3: pin crit = max(Criticality - net slack(p)) / Tcrit, 0
4: pin crit = pow(10, pin crit)
5: pin critical(p) = pin crit
6: end for
7: end for
In method C, as shown in Figure 3, we traverse through all the nets of the design, which is followed by traversal for all the pins for each net. Initially, we compute the \( \text{Pin}_{\text{crit}} \) for each pin which is maximum of the ratio of net slack divided by time period of the critical path of the design. Next, we assign \( \text{Pin}_{\text{crit}} \) to be equal to \( e \) raised to the power of \( \text{Pin}_{\text{crit}} \). After this we choose the maximum of \( \text{Max}_{\text{criticality}} \) and \( \text{Pin}_{\text{crit}} \).

In method D, as shown in Figure 4, we traverse through all the nets of the design, which is followed by traversal for all the pins for each net. Initially, we compute the \( \text{Pin}_{\text{crit}} \) for each pin which is maximum of the ratio of net slack divided by time period of the critical path of the design. Next, we assign \( \text{Pin}_{\text{crit}} \) to be equal to \( \text{Pin}_{\text{crit}} \) raised to the power of \( e \). After this we choose the maximum of \( \text{Max}_{\text{criticality}} \) and \( \text{Pin}_{\text{crit}} \).

### 3. EXPERIMENTS AND RESULTS

We carry out our experiments on twenty FPGA designs. The experiments are run on a 64-bit MAC running on UNIX operating system. We used VPR version 2.4 from internet. The results obtained by using method A and method are shown in Table 1 and Table 2 respectively. As shown in Table 1, the third column represents the time period for each design, and column 4 and column 5 represent the time period obtained in timing analysis after running the router VPR and the proposed methods respectively. The comparison of time periods obtained for VPR and proposed method (Method A and Method B) are shown in Figure 4 and Figure 5 respectively. Note that while extracting the results for VPR we have used criticality exponent as 0.01 for VPR.

### Table 1 Comparison of time period between VPR and proposed for Method A

| Index | Design | Clock Period in nanosecond | Period VPR in nanosecond | Period MethodA in nanosecond | % Improvement of Slack |
|-------|--------|-----------------------------|--------------------------|------------------------------|------------------------|
| 1     | bluf   | 92.00                       | 146.491                  | 110.43                       | 43.97683               |
| 2     | apen2  | 130.00                      | 165.168                  | 126.73                       | 17.26                  |
| 3     | apen4  | 150.00                      | 144.419                  | 121.38                       | 14.95963               |
| 4     | edkey  | 100.00                      | 144.95                   | 141.22                       | 2.73                   |
| 5     | cicnu  | 300.00                      | 252.266                  | 253.611                      | 12.885                 |
| 6     | der    | 120.00                      | 151.944                  | 118.99                       | 27.495                 |
| 7     | defeq  | 100.00                      | 98.4009                  | 99.2141                      | 8.7474                 |
| 8     | diph   | 85.00                       | 98.50863                 | 83.45                        | 23.28682               |
| 9     | elicte | 150.00                      | 215.927                  | 182.579                      | 22.232                 |
| 10    | ext010 | 189.00                      | 324.846                  | 247.515                      | 40.90688               |
| 11    | extp   | 150.00                      | 136.444                  | 98.34                        | 25.42076               |
| 12    | fritec | 150.00                      | 234.588                  | 165.839                      | 43.82567               |
| 13    | mica   | 120.00                      | 131.223                  | 106.322                      | 20.75083               |
| 14    | pdc    | 380.00                      | 315.524                  | 238.912                      | 20.16105               |
| 15    | sfo    | 250.00                      | 237.595                  | 198.24                       | 15.8876                |
| 16    | sfo041 | 125.00                      | 260.179                  | 177.33                       | 65.8729                |
| 17    | sfo081 | 91.00                       | 150.017                  | 101.1                         | 53.75495               |
| 18    | seq    | 140.00                      | 153.597                  | 126.938                      | 19.04214               |
| 19    | sphi   | 120.00                      | 212.304                  | 155.31                       | 64.16167               |
| 20    | sphi2  | 80.00                       | 84.2235                  | 90.0419                      | -7.272                 |

**Average** 25.85931
4. RESULTS & DISCUSSIONS

As shown in Table 1, Table 2, Table 3 and Table 4, the routing Method C works the best on Design Apex4. We list down the pin criticality for design Apex4 considering for Methods A, B, C and D in Table 5. As show in Figure 6, the value of weights for Method C are the highest, which is the reason for best improvement in slack for the design Apex4 using method C.
To thank Department of Electronics and Communication Engineering, Cambridge Institute of Technology, Bangalore for providing the resources to conduct the experiments.

5. CONCLUSION

Timing driven routing is a well-studied problem and important problem considering the impact of routing to performance of the design after fabrication. In this paper we present a comparative analysis of timing driven routing algorithms. We present four methods for weighing the nets of critical path of a design and provide a comparative analysis of these methods. The methods A, B, C and D proposed in this work, show an improvement of 14.65 %, 26.85 %, 17.18 % and 22.35 % improvement in slack when compared with a well-known routing algorithm VPR.

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