Multilayer Structure of a New Portable, Low-Cost and Reversible Arithmetic and Logic Unit using High-Speed and Low-Power “QCA” Technology with Good-Scalability.

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Abstract. All nano-technologies including “QCA” (Quantum-dot Cellular Automata) is widely used in today’s world to reduce the power dissipation, area and delay. “QCA” is a magnify technology with huge advantages such as: high-speed, high-density, faster-switching and higher clock-frequency which is rapidly used for Integrated-Circuit (“IC”) design. Quantum-dot Cellular Automata is an useful and appropriate alternative of the “CMOS-technology” because of its various advantages such as: its high-frequency, less power leakage and less required area. An “ALU” (arithmetic and logic unit) is applying for all types of arithmetic-logical performances and it widely used in digital circuits for all types of arithmetic and logical operations. The reversible-Logic an authentic solution in low-power and low-cost technology. This paper presents a latest 3-D or multilayer structure of ALU using reversible-computing and also non-reversible logic which gives a comparative outcome with low supply-power and delay. The complexity of the formation and the engrossed size of this model is low. ‘AND-Gate’, ‘OR-Gate’, ‘XOR-Gate’ and the reversible ‘TSG-Gate’ and also the non-reversible model of ‘Full-Adder’ are used to design the suggested model of this paper through the “QCA Designer” software (for simulation). This design reduce the size of the model up to 0.11 μm² with three layers which is also compared to the formation in the “Xilinx” software.

Keywords: Arithmetic-logic performance, High-Speed, Multilayer or 3-D Structure, ‘TSG-Gate’, ‘QCA Designer’, “Xilinx”.

I. INTRODUCTION

Nowaday “nano-technology” world the “QCA” technique can be accepted as a suitable replacement of “CMOS” Design. Binary-Operation of this proposed technique depends on the location change of free electrons at different quantum-dot of the cell [1-5]. This paper mainly focus on the reversibility, scalability, leakage-power reduction with room temperature and speed improvement of the suggested device by applying reversible-logic in “QCA Designer” where the forward and also backward running can be doing in a proper way with less chances of information losses or we can say this process is a proper way to decrease the amount of dissipated-power.

In this paper a novel reversible, scalable, flexible, high speed and fault tolerant 3-D formation of “ALU” design is suggested using reversible ‘AND’ and ‘OR’ gate and Reversible ‘TSG-Gate’ which can be used as ‘full-adder’ and reversible-XOR gate to the KTln2 energy/bit required for irreversible gate in “QCA” [6].

This paper also represents the “RTL schematic” and the “technology schematic” of the “ALU” design using “VHDL code” in “Xilinx” software and the outputs of these two software are compared which is presented through a table in this paper.

II. BACKGROUND OF “QCA” CELL STRUCTURE AND CLOCK-MECHANISM

Two steady ground-states which are located on the of the “QCA” cell are responsible for two logic levels (‘0’ and ’1’) in digital-circuits. The basic “QCA” cell-design and two types of polarized cells (‘+1’ for binary ‘1’ and ’-1’ for binary ‘0’) are presented in “FIGURE” 1(a), 1(b) and 1(c) respectively. The coulombic interaction between electrons of nearby cells is occurred to form the binary wire (“FIGURE” 2) in “QCA” design [7-8].

![FIGURE 1(a).Basic cell-design of QCA 1 (b).Binary ‘1’ cell-design of QCA 1(c). Binary ‘0’ cell-design of QCA](image)

When first cell is forced it applies the same force to the next neighboring-cell through coulombic-repulsion. In another process for 45 degree cells opposite polarized-cells (‘+1’ and ’-1’) are located one after another which are used for signal-transmission process. The equations of “three input majority gate”, ‘OR-Gate’ and ‘AND-Gate’ are represented in this paper in equation (1), (2) and (3) respectively (Let A, B and C are the three inputs ).
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\[ M(A, B, C) = AB + BC + AC \]  
(1)

\[ M(A, B, I) = AB + B.1 + A.1 = A + B \]  
(2)

\[ M(A, B, 0) = AB + B.0 + B.0 = A.B \]  
(3)

FIGURE 2. Wiring process using 90-degree (A) and 45-degree (B) cell [8]

The truth table and “QCA” lay-out of “5-input majority gate” and “Inverter gate” (single layer and multilayer) are represented here in “Table” 1 and “FIGURE” 3 and 4 respectively [8-9].

| \( \Sigma (A, B, C, D \text{ and } E) \) | Maj (A, B, C, D, E) |
|--------------------------------------|-------------------|
| 0                                   | 0                 |
| 1                                   | 0                 |
| 2                                   | 0                 |
| 3                                   | 1                 |
| 4                                   | 1                 |
| 5                                   | 1                 |

Table 1: Truth Table of “5-input majority gate” [9]

FIGURE 3. “QCA” lay-out of “5-input majority gate” [9].

FIGURE 4.A. Standard inverter, B. 2-Effective cell inverter, C. Inverter using 2-layers [8]

Four clock-zones 1, 2, 3 and 4 are experienced by quantum cells which are represented here in “FIGURE” 5.

FIGURE 5. Clock-Mechanism of quantum cell design [9].

III. RELATED PAPER-WORKS

In this section of this paper the review of different proposed designs (year-wise) are summarized and represented through different figures. In “FIGURE” 6 a suggested formation of a four-bit “ALU” with non-reversibility and non-fault tolerance [10] is represented here and this formation was a 3-layered (“3-D”) formation with 420 numbers of cells which is occupied 0.85\( \mu m^2 \) area. This year also formed a simple “12-Arithmetic Logic Unit” having twelve inputs of signal dependence.

In the year “2008”, a “16-Arithmetic Logic Unit” formation using ‘vector-pair’ with above disadvantages[11] was proposed and in ‘2012’ a novel “ALU” structure with reversibility was formed, where the logic-unit and the arithmetic-unit were designed in separate portion with reversible-criteria [12], but the large size and higher number of clock-zones were the markable drawbacks of the selected structure. Its block-diagram is shown this paper in “FIGURE” 7.

A multi-layered (3-layers)“ALU” formation using ‘4’“self-testing” [13] adder (“FIGURE” 8)and another “ALU” design using ‘Naghibzadeh Hoshmand Gate’ (“FIGURE” 10) were formed in ‘2017’ [15] with 670 number of quantum cells.

In ‘2018’ three layered 1-bit “ALU-design” with ‘OR-Gates’, ‘XOR-Gates’ and “Full-adder” was formed [14] applying 464 quantum cells and three ‘clock-zones’ delay (“FIGURE” 10).
This year also a reversible QCA based design of ALU using ‘AND-Gate’, ‘OR-Gate’, ‘XOR-gate’ and “Full adder” with fault tolerance was formed and due to this design the delay of the circuit can be reduced (“FIGURE”11).

IV. PRESENTED DESIGNS

In a Digital-circuit an “Arithmetic and Logic Unit” is used to execute any computer-programs (mainly arithmetic and logical operations). So, it is very important to design a low power and high-speed “ALU” structure with high scalability and high-density. In our proposed “ALU” formation we use the logic-gates with reversibility for doing the arithmetic and logical operations which are discussed below and the outcomes are presented by using a design of a “4:1 MUX”.
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A. Designs Of A Reversible Logic-Gates And “FULL-ADDER” Using “QCADESIGNER”

In this paper a reversible ‘XOR-Gate’ using ‘AND ,OR’ gate and ‘NAND & NOR’ gate are designed by “QCA” (in “FIGURE” 14,15 and 16 respectively)and also the design of a non-reversible and a reversible “Full-Adder” using “TSG-Gate” are presented in “FIGURE” 17 and 18.

FIGURE 12. Logic-diagram of “Double-feynman-Gate”[8]

FIGURE 13. Logic-diagram of “TSG-Gate” as a ‘Full-Adder’ [6].

FIGURE 14. Reversible ‘AND & OR’ gate.

FIGURE 15. Reversible ‘NAND and NOR’ gate.

FIGURE 16. “Double-feynman-Gate” as a reversible ‘XOR-Gate.’

FIGURE 17. “Full-Adder” formation using “3 and 5-input majority gates”.

FIGURE 18. “Full-Adder “formation using reversible “TSG-Gate”. 
B. Design Of “4:1 MUX” Using “QCADESIGNER”

The suggested formation of “ALU” requires a “4:1 MUX” structure which includes four inputs (A, B, C and D), two select lines such as S₀ and S₁ and one output (F). The logic-diagram, truth-table and “QCA” design of the selected device are represented in “FIGURE” 19, 20 and “Table” 2 respectively. 3 inverter-gates, 6 “AND-Gates” and 3 “OR-Gates” are applied to form this multiplexing circuit formation. In this paper the “4:1 MUX” is used to select the outputs of the “ALU” by two select-lines and it is designed in the 3rd layer of the “ALU” structure by using four clock-zones in ‘critical-path’.

![Logic-diagram of “4:1 MUX” in “ALU”](image)

**FIGURE 19.** Logic-diagram of “4:1 MUX” in “ALU” [8].

| S₀ | S₁ | A | B | C | D | F |
|----|----|---|---|---|---|---|
| 0  | 0  | X | X | X | 0 | 0 |
| 0  | 0  | X | X | X | 1 | 1 |
| 0  | 1  | X | X | 0 | X | 0 |
| 0  | 1  | X | X | 1 | X | 1 |
| 1  | 0  | X | 0 | X | X | 0 |
| 1  | 0  | X | 1 | X | X | 1 |
| 1  | 1  | 0 | X | X | X | 0 |
| 1  | 1  | 1 | X | X | X | 1 |

**Table 2: Truth-table of “4:1 MUX”** [8]

V. SIMULATION-RESULTS AND COMPARISON

This paper represents ‘OR-Gate’ with reversibility using “Double-Feynman-Gate” and “TSG-Gate”. All the required parameters for the simulation are listed here in “Table” 3. The size of thefts-Gate” is less than the other using reversible gates and also it directly works as a “Full-Adder” circuit. “TSG” when acts as “Full-Adder”, it has four inputs (A, B, Cin, 0) and outputs (P, Q, R, S) which are shown below in eq. (1), (2), (3), (4).

\[ P = A \] (1)
\[ Q = A \oplus B \] (2)
\[ R = AB + BC + CA \] (3)
\[ S = \text{XOR}(A, B, \text{Cin}) \] (4)

The proposed “ALU” structure is formed by using 3 layers (3-D design). The first-layer shows the “Full-Adder” design using “TSG-Gate”. The transmission line is represented in the next layer and the third-layer presents the structure of proposed “4:1 MUX” using “QCA Designer” which is given in “FIGURE” 21. The occupation-area of the proposed reversible quantum dot design is minimized by using multiple layers and also this technique is able to reduce used clocking-zones of “QCA” technology.

**FIGURE 20.** “4. 1 MUX” structure for “ALU”.

![3 layers of presented “ALU”](image)

**FIGURE 21.3 layers of presented “ALU”.

This paper presents the simulated results of “Full-Adder” using “TSG-Gate” in “FIGURE” 22, reversible ‘AND-OR’ gate and ‘NAND-NOR’ gate in “FIGURE” 23 and 24 respectively. These two figures are also follows the “1:1 input / output” technique of reversibility. Here two inputs are given and from this design we get two different logical representations and these are the two different outputs. One output presents ‘AND’ gate’s outputs and another is ‘OR’ gate’s output in “FIGURE” 23. “FIGURE” 24 uses same phenomenon for the outputs of ‘NAND’ and ‘NOR’ gate. The outputs of the “4:1 MUX” and proposed structure of “ALU” are presented in this paper in “FIGURE” 25 and 26 respectively.
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The outcome of simulating “ALU” presents the “TSG” gate outputs and the output of “4:1 MUX” in differently. The outcome of “4:1 MUX” follows the truth-table of this device.

FIGURE 22. Result of the simulating “Full-Adder”.

FIGURE 23. Result of the simulating reversible ‘OR-AND’ gate.

FIGURE 24. Result of the simulating reversible ‘NOR-NAND’ gate.

FIGURE 25. Output of the simulating “4:1 MUX”.

FIGURE 26. Output of the simulating 3-D structure of “ALU”.

This paper compares the proposed circuits to the outcomes of “Xilinx” software. The circuits are formed in “Xilinx” by ‘VHDL’ coding and the “technology schematic” and “RTL-Schematic” of the suggested “ALU” figure is presented in this paper in “FIGURE” 27 and 28 respectively from which the logic-diagram of different parts of the proposed structure can be achieved properly. But the occupation-area, delay and power of the simulated design through “Xilinx” can be minimized effectively by using “QCA” simulator. So, the required area, power and delay of the discussed simulators are enlisted in “Table” 4. This paper also represents the graphical-representation of supply-power vs. junction-temperature in “FIGURE” 29 which shows the exponential growth of supply-power with the increment of junction-temperature.
Table 4. Comparison table between “Xilinx” and “QCA Designer” software.

| Name of the designs | IOB (No. of gates in “Xilinx”) | Delay in “Xilinx” (ns) | Power in “Xilinx” (mW) | Area in “QCA Designer” (m²) | Delay in “QCA Designer” (cycles) | Number of layer in “QCA Designer” |
|---------------------|--------------------------------|-----------------------|------------------------|-----------------------------|---------------------------------|---------------------------------|
| ALU with 4 input and 2 select lines | 8 | 0.2 | 0.08 | 320 | 2.2 | 3 |

The size and clock-zones of suggested designs are presented in the table. This proposed reversible design of this unit able to reduce the number of required quantum-cells, cell-size, required area, delay and cost (area X latency²) than the previous referred design of paper [8] and in this proposed design 4 clock-zones are applied in the critical path. The outcomes of some referred papers are compared with the presented design of this paper and all the values are shown in “Table” 5.

Table 5. The compared outcomes of “QCA” designs.

| “ALU” Design in different papers | Number of quantum-cells | Occupied area (µm²) | Layer-Number | Latency (Clock-cycles) | Reversible or not |
|----------------------------------|-------------------------|--------------------|--------------|-----------------------|------------------|
| [10]                             | 420                     | 0.85               | 3            | 3                     | No               |
| [11]                             | 35,596                  | 11.37              | 1            | 9                     | No               |
| [12]                             | 2857                    | 4.44               | -            | 6                     | Yes              |
| [13]                             | 1069                    | 2.34               | 1            | 2                     | Yes              |
| [14]                             | 464                     | 0.78               | 3            | 3                     | No               |
| [17]                             | 670                     | 0.92               | 3            | 4                     | Yes              |
| [8]                              | 332                     | 0.38               | 3            | 3                     | Yes              |
| Proposed                         | 139                     | 0.1                | 3            | 0.25                  | Yes              |

VI. CONCLUSION

A new multilayer reversible low-cost “ALU” is designed in our paper-work by using reversible “Full-Adder” design and reversible “4:1 MUX” design and applying cell-size reduction process through “QCA Designer” to minimize the occupied area, delay, cost and leakage-power than other previously discussed formations and also this paper presents a comparison between the outcomes of “QCA Designer” and “Xilinx” where the advancement of “Quantum-dot Cell Automata” with the logic of reversibility and multiple-layer technique over “Xilinx” technology is proved. This proposed structure is able to ignore information-loss due to reversible nature and the occupied area and latency of the proposed design are reduced 73% and 91% than previous paper [8]. The supply power of this proposed design are changes with junction-power increment up to “85°C”.

In future work these proposed designs can be improved more by optimizing the required layers and by using this structure for another circuits and by designing more advance device with the delay, cell-size, dot-diameter, required quantum cell-number reduction and improvement of fault-tolerance and better supply-power calculation.
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