Strategic Review on Different Materials for FinFET Structure Performance Optimization

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Abstract. In this paper, the strategic review of different materials that are used in FinFET structure is studied. This is achieved by using carefully designed source/drain spacers and doped extensions to mitigate the off-current, typically high in narrow band-gap materials, as part of a CMOS compatible replacement-metal gate process flow. FinFETs are promising substitutes for bulk complementary metal oxide semiconductor. FinFETs are dual-gate devices and Good electrostatic characteristics which are obtained in a wide range of device dimensions. The simulations provide further insights into device functionality and about the dominant off-state leakage mechanisms. The GaAs material was examined by scanning transmission electron microscopy (STEM) and the epitaxial structures showed good crystal quality. In this various types of materials are used and studied they are FinFET based Dual KK-structure, InGaAs-on-Insulator FinFET, Double Gate based n-FinFET using Hafnium oxide, SOI-FinFETs, MosFET (Multi gate), Deeply Scaled CMOS, FinFET, Selective Epitaxial Si Growth in FinFET and Atomic Layer Deposition (ALD) in FinFET. Furthermore, we demonstrate a controlled GaAs digital etching process to create doped extensions below the source-drain spacer regions.

1. Introduction
The first FinFET transistor type was invented in the year 1989 and it was called as "Depleted Lean-channel Transistor" or "DELTA" transistor. The first FinFET was fabricated in Japan by Hitachi Central Research Laboratory's Digh Hisamoto, Toru Kaga, Yoshifumi Kawamoto and Eiji Takeda [5][7][8]. A double-gate transistor can have each side connected to two different terminals or contacts. This type of FinFET is known as split transistor. A fin field-effect transistor (FinFET) is a multigate device, a MOSFET (metal-oxide-semiconductor field-effect transistor) built on a substrate where the gate is placed on two, three, or four sides of the channel or wrapped around the channel, forming a double gate structure. These devices have been given the generic name "finfets" because the source and drain region forms fins on the silicon surface. The FinFET devices have significantly faster switching times and higher current density than planar CMOS (complementary metal-oxide-semiconductor) technology. Compound semiconductors dependent on arsenides (In1−xGaxAs) are viewed as promising possibility to substitute silicon in nFETs for cutting edge and ultra-scaled CMOS innovation hubs [5]. These materials offer a noteworthy preferred position as far as electron portability contrasted with silicon and are reasonable for low-power applications. Aspect-ratio trapping (ART) strategy, for example, expects to channel precious stones which proliferates the channel effects [1].
FinFET technology emerged with numerous advantages when compared to bulk CMOS are listed below:

- Higher current drive capability with high speed,
- Lower threshold leakage,
- Lower power consumption,
- No random dopant fluctuation,
- Better mobility and
- Scaling of the transistor beyond 28nm.

We have recently built up a combination approach called template-assisted selective epitaxy (TASE), in which view of the development of various III-V materials inside discretionarily molded oxide is done. Due to developing current and short-channel issues of customary planar MOSFET transistors, it is beyond the realm of imagination to expect to proceed with further downsizing the element sizes of the planar transistors. FinFET transistors have been presented as an elective arrangement, which has the important attributes to additionally recoil the innovation [13]. The term FinFET was first referenced to depict the non-planar Double Gate transistor. It was shown as a potential trade for regular planar innovation [2]. Afterward, FinFETs were utilized in numerous distributions to depict transistors worked with new non-planar multi-Gate design.

The characteristics of the FinFET transistor is that its directing channel comprises of slight vertical silicon Fins encompassed by Gate terminals [12][24]. This prompts a superior control of the channel and better electrostatic properties, consequently decreasing current in the off state [3-4]. Because of their 3D structure, FinFETs have a few focal points including: controlled Fin body thickness, low edge voltage variety, decreased changeability and lower working voltage. The entirety of this empowers structures that can work quicker with less force. Because of the critical force and execution benefits, FinFET planning and assembling may present extra difficulties.

The novelty of the innovation and the normal increment in assembling cost make it worth investigating abandons that could influence item quality and yield. This is a nontrivial task, given that even recollections planned ahead of time planar innovations can be influenced by various imperfection types. Every one of which is ordered as a remarkable issue model. It is basic to build up a far reaching yet streamlined set-up of test calculations that identify these deformities, while keeping test cost low. Albeit a considerable lot of the imperfection types influencing recollections dependent on planar transistors additionally influence FinFET-based recollections, new deformities do happen because of the interesting FinFET structure [5].

In multi-gate field-effect transistors (MuGFET), which are constructed corresponding to one another, the quantity of blades is expanded, improving the short channel impact. The measure of charging bearers spilling out of more noteworthy potential to diminished potential is additionally expanding as the quantity of blades rises. The rate at which the bearers stream besides speeds up more quickly. Better Gate command over the leading channel is the essential advantage of different blades. With these lines, the current leakage and the dispersal of vitality are decreased. This achieves high on-state drive current. The demonstrating of 2D nFinFET has been done in simulation software. FinFET gadget comprises of source, channel, Double Gate, oxide layer and four nitride spacers. Here N-type FinFET was made at both 22nm and 20nm innovation [26]. The source and channel were doped with Ntype material like Phosphorous. The Channel was doped with P-type material like Boron. The doping convergence of source/channel and channel is 1e+18 and 1e+20.

The silicon material is utilized for source, channel and channel district. Four spacers are utilized so as to improve the ON current. The spacers were comprised of nitride material Dual material spacers and triple material spacers can likewise be brought into utilization for additional improvement in gadget execution. The work capacity of both front and back Gate shifts dependent on various Gate material. So as to improve the channel flow, the high k dielectric material called hafnium oxide was utilized in the oxide layer. The tallness of the FinFET is 10nm. The two-dimensional schematic perspective on double gate n-FinFET in simulation of 2D views of the n-FinFET double gate in the Fig.1.
FinFET based recollections are additionally less compared to specific deformities that would cause disappointments in planar-based recollections. Given these distinctions, the issue models and recognition strategies produced for planar transistors are not adequate to cover FinFET abandons in implanted recollections [14]. With creation of FinFET-based (recollections utilizing FinFET transistors), the issue of installed memory test and fin is basic, as the issue models and test calculations utilized for regular recollections may not cover the entire part of potential imperfections in FinFET-based recollections. In spite of the significance of the issue, generally few explorations examine have been directed around there during the ongoing years [15]. A ultra-thin Si fin in a FinFET system frames a directing divert in which the electrons stream from source to deplete. This leading channel is encased by a Gate that provisions the information voltages. Along these lines, controlling electrons stream even in off-state current. There is regularly an expansion in the amount of charging carriers and the speed at which they stream, driving in the breakdown of the single-blade leading channel. This obstructs the current progression of electrons from source to deplete. The figure (2) gives the 3D View of FinFET structure which is shown below. This FinFET structure consists of thin (vertical) fin of silicon body on a substrate. The gate is wrapped around the channel providing excellent control from three sides of the channel. This structure is called the FinFET because its Si body resembles the back fin. The fins are the 3D channel between the source and the drain.

2. Literature Survey
For exchanging gadgets and advanced hardware field-effect transistors (FETs) with ordinarily off qualities are attractive [2]. In this manner, cubic AlxGa1-xN/GaN without unwanted parasitic piezoelectric and unconstrained polarization fields and with equivalent electrical properties for all Gate directions and has a critical vehicle favorable circumstances, and is being utilized widely in research as
channel materials for forthcoming exceptionally flaky gadgets. Further the cubic nitrides would permit utilizing a similar innovation for regularly on and ordinarily off gadgets. Yet, larger part of III-V materials have impressively littler band hole when contrasted with silicon, prompting inordinate band-to-band burrowing current flows, which in as far as possible their versatility past 22 nm innovation length of gate node (LG).

In HEMT (High Electron Mobility Transistor) gadgets, the gate leakage current and support current are significant variables constraining its presentation and unwavering quality. Thusly, the utilization of a Gate oxide assists with improving Gate contact shaping a MOS-HEMT (Metal Oxide Semiconductors High Electron Mobility Transistor), lessen the Gate current and increment channel current, nonetheless, it somewhat decreases the trans conductance as a result of a bigger Gate to-channel detachment. The measure of transistors in a coordinated circuit duplicates like clockwork, as indicated by Moore's law. A few methodologies to downsize the size of CMOS innovation have been created. The multi-Gate transistor is one such methodology. MOSFET is alluded to as a multi-Gate transistor with more than one Gate in a solitary gadget.

FinFET is a multigate structure and a transistor that is non-planar. It has front and back Gates that give better control to the effect of the short channel. Double gate devices are thusly most appropriate for low-power frameworks as they permit critical decrease in reserve power along with improved effectiveness. FinFET is portrayed by the wrapping of the leading channel around a dainty silicon film that shapes the gadget's body. The material size decides the device productive channel length and Gate width. Because of the float of electron highlights in the direct and the move in limit voltage inferable from the contracting channel length, the concise channel impacts happen. The meager silicon film in the SOI gadget restrains the off-state current. The silicon film thickness must be short of what one fourth of the length of the channel.

For standard bulk MOSFETs, the raised fixation punch through plug results in current corruption and serious drivability in the Gate controls the force hindrance among source and channel. Due to the short channel impact, one self adjusted Double Gate MOSFET configuration has a major sub-edge swing. FinFET is the fruitful apparatus that doesn't make up for the gadget's size past the cutoff and productivity. Utilizing high k dielectric, the current flow is diminished. MOSFET Double Gate is most appropriate for low-force or elite gadgets later on. Assembling MOSFET Double Gate gadgets is more than assembling single Gate gadgets. Fig.3. shows the schematic view of FinFET with the geometrical boundary, for example, Gate length (Lg). It very well may be construed that, a metal Gate and high k dielectric gives a decent exhibition in nanometer run. In this work, area 2 portrays the reproduction of n-FinFET in TCAD programming with a Gate length of 22nm and 20nm innovation. Distinctive Gate materials like aluminum, molybdenum and gold were utilized. For each Gate metal outcomes have been acquired and the exchange attributes for each Gate metal were then plotted and an examination was made between them.

![Figure 3. Schematic view of FinFET device](image)

3. Review of Different Materials That Are Used in Finfet
Initially, MOSFET is introduced with multi gates but it has shot channel effects. To overcome this deeply scaled CMOS structure is implemented. But this structure has leakage issues. Now, at last to overcome all this issues, FinFET is introduced. FinFET is a gate that is self-aligned and can be fabricated with a single lithography process [9]. FinFET will have high aspect of ration and fin widths of about 10nm.
FinFET have high durability per unit chip area. Basically, low power & high frequency of FinFet structure performance is improved with RF/Analog Figure of Merit. Asymmetric drain extension Dual-KK structure plays very important role in FinFet structure. The asymmetric drain extension regions are improved by taking the parameters of cutoff frequency ($f_T$) and maximum oscillation frequency ($f_{\text{max}}$). The parameters that are improved in asymmetric drain extension of Dual-KK are given below:

- $g_m$ (trans conductance) - ~ 9.09%
- $g_{ds}$ (output conductance) - ~ 13.04%
- $f_T$ (cutoff frequency) - ~ 12.91%

Compared to the dual-k structure, the asymmetric drain extension dual-KK structure improves the efficiency. Next another important material of FinFet is In-GaAs-on-Insulator [10-11]. This material is optimized based on the on/off trade-off showing record performance. Using this technology, the gate length is expanded up to 20nm and width is up to 10nm. This is achieved by carefully designing source/drain spaces and doped extensions to migrate the off-current [23]. Double gate-based n-FinFET is designed and simulated at 22nm and 20 nm technology. The leakage current in this design is reduced by using the Hafnium oxide [26]. Generally, Hafnium oxide has high-K dielectric constant as gate dielectric. Hence the combination of Gold gate metal hafnium oxide has larger $I_{\text{ON}}/I_{\text{OFF}}$ Ratio than Aluminium.

In the Silicon-On-Insulator (SOI) FinFET structure, fully depleted nMOS and pMOS FinFET’s have been demonstrated. This demonstrated FinFET’s have fin width down to 5nm, 65nm tall fins. In this lithography process is introduced for optimizing the dry etch & hard mask trimming conditions. To reduce the resistance in FinFET’s selective epitaxial Si growth is implemented. This will improve the performance in effective way. In this 300mm SOI wafers with 145nm buried SiO$_2$ & 65nm crystalline (C-Si) is used a material.

| Material used in FinFET | Improvement |
|-------------------------|-------------|
| FinFET based Dual KK-structure | 1) $g_m$ (trans conductance) - ~ 9.09%  
2) $g_{ds}$ (output conductance) - ~ 13.04%
3) $f_T$ (cutoff frequency) - ~ 12.91%
4) Maximum oscillating frequency |
| InGaAs-on-Insulator FinFET | Improvement in the length of gate and sources of drain |
| Double Gate based n-FinFET using Hafnium oxide | Reduces the leakage current |
| SOI-FinFETs | Improvement in the fin width |
| MosFET (Multi gate), Deeply Scaled CMOS, FinFET | Short channel effects are obtained and Leakage Issues are obtained. Improvement in chip area and high performance |
| Selective Epitaxial Si Growth in FinFET | Repairs the fin outer surface |
| Atomic Layer Deposition (ALD) in FinFET | Improvement in threshold voltage ($V_t$) |
4. Conclusion
Hence, in this paper review is given on different FinFET materials. FinFET based Dual KK-structure, InGaAs-on-Insulator FinFET, Double Gate based n-FinFET using Hafnium oxide, SOL-FinFETs, MosFET (Multi gate), Deeply Scaled CMOS, FinFET, Selective Epitaxial Si Growth in FinFET and Atomic Layer Deposition (ALD) in FinFET review are studied. Generally, FinFETs are promising substitutes for bulk complementary metal oxide semiconductor. FinFETs are dual-gate devices and Good electrostatic characteristics which are obtained in a wide range of device dimensions. The simulations provide further insights into device functionality and about the dominant off-state leakage mechanisms. From this study, it can observe that Transfer characteristic of InGaAs FinFET device, and Representative transfer characteristic of a planar InGaAs device is continually increasing. Therefore, GaAs material was examined structures by showing its good crystal quality.

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