Energy efficient quaternary capacitive DAC switching scheme using sar analog to digital converter

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Abstract: This article shows the outline of successive approximation register- ADC used to convert the signals obtain from the brain into electrical signal. Quaternary capacitive exchangin vitality conspires (QCS) within the execution of (C-DAC) is utilized which makes the vitality utilization in the C-DAC free of the yield advanced output code. This method accomplishes a 50% diminishment within the normal vitality utilization. The design is actualized in 0.25nm technology using complementary metal-oxide semiconductor (CMOS).

1. Introduction:
We need to note document the readings of brain neural action as it is imperative to analyze the neurological clutters such as seizure disorder, sadness, and Parkinson’s illness. To document the brain’s neural movement there’s extraordinary request to scale down fixed coordinates microsystems. Numerous past works have appeared advance toward planning moo control Microsystems [1]-[5].

The Figure 1 appears the square graph of neural prosthetic BMI framework. This neural prosthetic BMI framework regularly comprises of documenting and incitement routing. The incitement route bargains with the final essential of the BMI and controls the development of the diverse parts of body. The documenting route bargains with the basic requirement of the BMI and basically called as NRF conclusion. The most part of NRF conclusion is to sense, intensify, and convert into digital neural signals extricated from the neurons without undermining it with electronic clamor. The NRF conclusion regularly comprises of a multi electrode cluster for recording the neural movement, taken after by a group of moo commotion intensifiers (LNAs), and A to D converter to digitally convert the neural data recorded.

Figure 1. Implantable framework for BMI framework.
An A/D converter is exceptionally critical piece within the NRF conclusion plan. Lots of work has to be done within the planning of a vitality productive A/D converter. Persuaded by the requirement for vitality productive arrangements for analog to computerized conversion, we display an arrangement for ADC in this paper. NR framework ordinarily employments a progressive estimation register (SAR) analog to computerized digital converter (ADC) due to direct determination (7-10 bits) and tall vitality effectiveness. To execute the successive approximation register-ADC we require the ability to compete between the input values with base input levels and check these base levels depending on the past measured values. Figure 2 appears the piece chart of a customary SAR-ADC.

Figure 2. Block diagram for customary Successive Approximation Register

The paper is divided into following sections, namely: Section II introduces the design for four-bit successive approximation register analog to digital converter. Area 2A displays the circuit usage of comparator circuit. Segment 2B clarifies the vitality proficient DAC exchanging strategy, quaternary capacitive switching scheme-digital to analog converter. Area 2(C) discuss regarding approximately the Non concurrent dynamic estimation select computerized basis module utilization. Segment III presents what the measured reenactment comes about.

Architecture of SAR-ADC

Figure 3 appears the proposed design of four bit successive approximation register-ADC with quaternary CDAC and mirror image components to change the digital to analog output yield for inverted contrast between two DAC yields.

Figure 3. Architecture of successive approximation register -ADC
A comparator circuit is utilized to measure input $V_{\text{in}}$ with $V_{\text{dac}}$ (Adacp or Adacm) base value. The details regarding the comparator circuit is discussed in section-III. For delivering the base levels the analog to digital converter (DAC) is utilized. Diverse sorts of digital to analog circuits can be utilized in successive approximation register-ADC but C-DAC is transcendently utilized due to the benefit of no dormant control scrambling. Imperativeness utilization inside the DAC may well be a basic parcel of include up to essentialness utilization inside the ADC and an vitality successful course of action of the ADC have to be endeavor to diminish the essentialness utilization inside the ADC. In this work, we have tried to introduce a unique imperativeness profitable DAC trading strategy [6]-[7].

2. Comparator:

The circuit of the comparator circuit is shown within the figure 4. The comparator circuit comprises of two parts namely, simple latch and a pre-amplifier. Here the clamor and input alluded balanced is observed as to be the restricting components of the determination, which are also the execution measurements of comparator. The pre-amplifier is utilized is favored for counterbalanced and feedback clamor moderation. The preamplifier in successive approximation register-ADC increase the leftover distinction between the digital to analog voltage and supply voltage fair sufficient for the discovery of the sign by the lock by utilizing the strobe signal which is created within the successive approximation register rationale piece.

![Pre-amplifier diagram](image1.png)

**Figure 4a. Diagram for Pre-amplifier**

![Latch circuit diagram](image2.png)

**Figure 4b. Diagram for the latch circuit**

An enhancer comprises of double combined transistors each for $V_{\text{in}}$ and gain of digital to analog converter. The utilization of transistor having W2 width gives a fractional input which decreases the viable yield conductance(G) and the comparator circuit can speedily move forward. The width of stack transistor (W1) which is kept more prominent than the W2 width of the
transistor giving halfway criticism to anticipate the compelling yield conductance from getting to be negative, indeed within the nearness of jumble.

3. Quaternary Capacitive Switching Scheme:

The analog to digital circuit works on the principle of twofold look calculation. On the basis of the comparative result obtained, the parallel look calculation advances to compete with high or low voltage values i.e if either moves up or have a down move for the upcoming competing. But the output obtain shows that, the down transition move devours more vitality than up move [8] amid the next competing process within the execution of binary search tree.

The vitality expended in down transition moves contrast with respect to the vitality devoured amid that of up moves. It occurs due to the obstructions of higher most significant bitcapacitors while extracting the less significant bits. The process has the vitality utilization within the C-DAC subordinate on the code obtained. The most significant bitcapacitors meddled after the less significant bits obtained consequently debases the vital utilization amid the down moves.

![Figure 5. Proposed switching technique with Quaternary Switching Capacitors](image)

In figure 5 appears the parallel weighted capacitive digital to analog converter for exchanging plot for four-bit successive approximation register-ADC. The figure appears to be the proposed conspire, where after the output bit is obtained, the successful capacitance decreases by coasting the final most significant bits capacitors. Subsequently the most significant bits capacitors don’t influence the vitality utilization amid the extracting process of the leftover less noteworthy bits. The sum of vitality conveyed by the base to the CDACis at that point as it were subordinate on the capacitance to be exchanged from Vcm to base voltage level (Vref). The introduced vitality proficient exchanging conspire diminishes the vitality concluded from the base by lessening an exchanging capacitance, compared to routine exchanging plans. As the most significant bit capacitors are not present amid the estimation of low significant bits, the design conspire utilizes the energy within the capacitive digital to analog converter autonomous of the yield computerized code[8].
Figure 5c and figure 5d shows up and down procedure required individually for the estimation the moment most significant bits. To implement this process we begin with most significant bit capacitor (8C) is made to drift who empowers exchanging of as it were 2C for step change of V/8 within the capacitive digital to analog converter yield compared to 3C in [9]. The vitality obtained by the base value is ¾.CV2 for both up and down moves in this part. The vitality utilization for these steps in [10] are Eup=1/2.CV2 and Edown=5/2.CV2, i.e. Eavg =1.5*CV2. Hence the proposed strategy accomplishes a 50% decrease within the normal vitality utilization for thisstep. Essentially figure e to figure h appears that coasting the 2nd most significant bit capacitor which requires exchanging of as it were 0.5C with respect to 2C in [9,10], for the estimation of next most significant bit. The degree of the trading capacitor esteem for the necessity of nth most significant bit (barring sign bit) can be measured as,

Csw(n)= Cdac/4n

The entire capacitance value of digital to analog converter is Cdac and increases to two nano Coulomb for an n-bit digital to analog converter. The estimate of switching capacitor diminishes in a quaternary mold within the scheme introduced[5].

Amid the output of less significant bits, the most significant bit values of capacitors are evacuated, and the evacuation of most significant bit capacitors make a total remaining charge on the capacitive digital to analog converter yield rail which jam the past esteem of the CDAC yield. Consequently the exchanging of the LSB capacitors has to do as it were the increased work. Moreover in this conspire as it were one set of capacitors is exchanged at a time, Vcm to base voltage value or zero supply, which maintains the plan of the advanced rationale basic and vitality proficient. The normal vitality utilization for an multi bit analog to digital converter for the introduced exchanging conspire can be calculated utilizing the equation,

\[E_{avg}(n)=\sum_{i=1}^{n-1} 2^{n-2i-1}(1-\frac{1}{2^{i}})CV^{2}\]

As the higher most significant bit capacitors don't influence vitality utilization amid the estimation of LSBs, the vitality expended for up and down moves are continuously break even with which makes the vitality utilization free of yield code. Lessening within the estimate of the exchanging capacitance is additionally supportive in accomplishing speedier settlement within digital to analog converter and subsequently progresses the speed of the progressive estimation enlist (SAR) ADC[9].

In case the esteem of computerized to analog converter voltage is underneath zero, at that point at that point the esteem can be made positive by changed over by firstly trading the two computerized to analog source values with the comparator or by checking the likeness of this negative DAC voltage with negative of the tried input voltage. The past strategy is favored as the final recognized will alter the adjusted of the comparator circuit which can impact the linearity design of the analog to advanced converter. To alter these voltages it does not require any extra clock flag and hence speed parameter has no affect.

4. SAR Logic Module:
Successive approximation register-ADC executes twofold look calculation utilizing the successive register control rationale. Successive register control rationale decides every bit progressively or consecutively subject to the output of the comparator. The control rationale employments a RC and a code enroll circuit. The RC is essentially a shift register. At the end of clock pulse, one of the yields within the RC has output 1 for flip flop within the shift register. The
yield of the FF decided by the RC is utilized as the clock output value as 1 for the past changed tumble[10].

During the rise time of clock this change flounder produces the output from the comparator circuit. At the conclusion of each transformation, To indicate the end of transformation EOC flag is given. To implement a low power circuit, TG based SR delay logic is used.

5. Simulation results:
The figure 6a and figure 6b shows the graph for magnitude response and graph for phase response of the preamplifier. The simulation values are Gain voltage= 22 decibel and Wp=34 KHz. Figure6c represents the time changing output of the comparator circuit.

Figure 6(a). Preamplifier: Magnitude Response

Figure 6(b). Preamplifier: Phase Response

Figure 6(c). Preamplifier: Transient Response
6. References:

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