Design and Fabrication of Planar Schottky Diode for Electrostatic Discharge Protection

Chong SHEN and Xiu-lan CHENG*
Center for Advanced Electronic Materials and Devices, Shanghai Jiao Tong University, Shanghai 200240, China
*Corresponding author

Keywords: Semiconductor fabrication, Schottky diode, ESD.

Abstract. A type of easy-to-fabricate Schottky diode with controllable breakdown voltage is design and fabricated. The Schottky junction is formed by the contact of Aluminum electrode and light doped n-type silicon. A special comb teeth structure is designed to lower the resistance and breakdown voltage. The diodes can achieve breakdown voltage between 2V and 16V by optimizing the doping concentration of the substrate and the distance of the comb teeth. The diode has great application potential in electro-static discharge (ESD) protection circuit, due to its easy compatibility in CMOS circuit process and ability of withstanding high currents.

Introduction

With the development of semiconductor technology, the IC devices are scaling down, achieving higher device density and faster working frequency. However, the damage that comes with electro-static discharge (ESD) are becoming increasingly significant [1,2]. This makes developing ESD protection devices that are compatible with IC fabrication devices a necessity. Many kinds of devices can be used as ESD protection devices, including Zener diode [3,4] and transient voltage suppressor (TVS) [5,6], etc. They are both variants of PN junction diode. Schottky diode is another option for ESD protection [7,8].

Schottky diode uses certain metal materials, such as gold, silver, aluminum and platinum, as anode, and uses n-type semiconductor as cathode. The contact of these materials produces rectification property. Schottky diode has two major differences: magnitude of reverse saturation current and switching characteristic when compared with PN junction diodes.

The reverse current density of a Schottky diode can be calculated from equation (1) while that of an ideal PN junction can be calculated from equation (2).

\[ J_{st} = A^* T^2 \exp \left( -\frac{e \phi_{Ba}}{kT} \right) \]  
\[ J_s = \frac{e D_n n_p}{L_n} + \frac{e D_p p_n}{L_p} \]

In equation (1), \( e \) is the charge of an electron, \( A^* \) is effective Richardson’s constant, \( \phi_{Ba} \) is the height of Schottky barrier, \( k \) is Boltzmann constant and \( T \) is the temperature (Kelvin). In equation (2), \( D_n \) and \( D_p \) are diffusion coefficient of minority electrons and holes, whose diffusion length is noted as \( L_n \) and \( L_p \). \( n_p \) and \( p_n \) are minority electron and hole density under heat balance.

The transport mechanism of Schottky diode and PN junction diode is different, for the two equations above exhibit different forms. The current in PN junction is mainly determined by the diffusion of minority carrier, whereas that in Schottky junction is mainly determined by thermionic emission of majority carrier. With the same substrate doping concentration, it can be found that the reverse saturation current of Schottky diode is several magnitudes larger than that of PN junction diode.

Another major difference between Schottky diode and PN junction diode is their switching speed. As a device whose current is mainly produced by majority carrier, the switching time of Schottky
diode is magnitudes smaller than that of PN junction diode, whose current is mainly produced by minority carrier[^9].

Typical fabrication process of Schottky diode uses a vertical structure [10,11], the two electrodes are on the different side of the chip. Epitaxy process is also used, as is shown in Figure 1. Vertical structure takes larger space in the circuit and cannot be integrated into CMOS chips. The precise breakdown voltage control is more difficult in this structure as well.

![Figure 1. Typical structure of Schottky diode.](image)

Therefore, a special planar comb structure of Schottky diode is proposed in this paper to achieve easy integration on a single chip. Moreover, the breakdown voltage of the device can be easily controlled by adjusting the distance of the comb teeth. At the same time, the fabrication cost can be lowered for there is no epitaxy process.

### Design and Fabrication

A comb-shaped structure has been employed in order to decrease the series resistance of the diode and improve its performance [12]. The length of the contact area is noted as L, width as w and the distance of two contact area as d. The top view of the structure is shown in Figure 2.

![Figure 2. The top view of the Schottky diode.](image)

The vertical profile of the Schottky diode is shown in Figure 3. The device consists of an n substrate, a heavy doped area, a SiO2 layer and metal electrodes.

![Figure 3. Vertical profile of the Schottky diode.](image)
Two different types of 4-inch n-type <100> wafers are chosen for the fabrication. One has a doping concentration of $5 \times 10^{13}$ cm$^{-3}$ and a thickness of 525um and another has a doping concentration of $1 \times 10^{16}$ cm$^{-3}$ and a thickness of 525um. The first step is to clean the surface of the wafer with acetone and isopropanol, then deposit a 250nm-thick SiO$_2$ layer with plasma enhanced chemical vapor deposition (PECVD). The SiO$_2$ layer is etched to form the area for Schottky diodes and the marks for following alignments with Reactive Ion Etching (RIE). After that, remove the photoresist with acetone cleaning and plasma strip. Ion-implantation at the energy of 15 keV and with the dose of $5 \times 10^{14}$ cm$^{-2}$ is performed to form heavy doped area, whose target concentration is $10^{20} \sim 10^{21}$ cm$^{-3}$. Rapid thermal process (RTP) is performed under 1030°C for 8 seconds to activate the dopants. Then, deposit another 200nm-thick layer of SiO$_2$ with PECVD and form the contact area for the diodes with lithography and etching. This layer of oxide can protect the diodes and reduce the edge electric field, thus decrease the leakage current and improve the diodes’ breakdown performance. Then fabricate the electrodes with Aluminum and form the pad pattern with lift-off process. Before this step, the wafer is cleaned with BOE (Buffered Oxide Etch) for 15 seconds to remove potential natural oxide layer. After the fabrication, anneal the wafer for 10 minutes under 475°C and N$_2$ atmosphere to form good ohmic and Schottky contact. The whole process is shown in Figure.4 and the photos of the fabricated devices are shown Figure.5.

The I-V curve of the fabricated Schottky diodes is tested by Agilent BA-1500 semiconductor parameter tester equipped with a probe station. The voltage applied on the diode sweeps from 0V to...
18V by the step of 0.18V, there are 100 steps in total. The current through the diode is measured and plotted.

**Results and Discussions**

The I-V curves of fabricated Schottky diodes with different electrode distance are shown in Figure 6. The curve ends at 100mA current because the maximum scale of the tester is reached. Figure 7 shows the relationship between the breakdown voltage and the distance of the electrodes, namely the parameter $d$.

![Figure 6: I-V curve of the Schottky diode (Substrate doping concentration: $1 \times 10^{16} \text{cm}^{-3}$).](image)

![Figure 7: Breakdown voltage of the Schottky diode at different distances of the electrodes.](image)

**Effect of Doping Concentration of the Substrate on the Breakdown Voltage**

Figure 7 shows that under the same electrode distance, higher doping concentration of the substrate can achieve lower breakdown voltage. This can be explained by the avalanche break down mechanism of the Schottky diode. When metal and n-type semiconductor contacts each other, a space charge region is formed, whose width $W$ can be calculated with equation (3):

$$W = \left[ \frac{2 \varepsilon_s (V_B + V_R)}{eN_d} \right]^\frac{1}{2}$$  

(3)
where \( \varepsilon_s \) is the dielectric constant of Silicon, \( N_d \) is the doping concentration of the substrate, and \( V_{bi} \) and \( V_R \) are the diode’s built-in potential and reverse bias applied respectively.

Reverse biased, the carriers will start to move due to the electric field. When the electric field is strong enough (critical electric field strength, \( E_{crit} \), related to the condition of the substrate), the mobile carriers can be accelerated to high enough speed to activate other bound electrons, which results in higher current and more electron activations, namely the breakdown phenomenon. When regarded as an abrupt junction, the breakdown voltage \( BV \) of a Schottky junction can be calculated by equation below [13]:

\[
BV = \frac{\varepsilon_s E_{crit}^2}{2eN_d}
\]

\( E_{crit} \) can be calculated by equation (5) where \( E_g \) is the forbidden bandwidth of Silicon [14]:

\[
E_{crit} = 1.1 \times 10^7 \left( \frac{\varepsilon_s}{\varepsilon} \right)^{\frac{1}{2}} \left( \frac{E_g}{1.1} \right)^{\frac{3}{4}} N_d^{\frac{1}{4}}
\]

A lower doping concentration results in a longer space charging area, which needs higher voltage to reach its critical electric field strength.

The height of Schottky barrier \( \phi_{bn} \) can be calculated by equation (6):

\[
e\phi_{bn} = e(\phi_m - \chi_s)
\]

where \( \phi_m \) is the work function of metal and \( \chi_s \) is semiconductor’s electron affinity.

High doping concentration will cause the increase of electron affinity of semiconductor material, thus lower the height of barrier. Therefore, the electrons can pass through the barrier more easily and lower the breakdown voltage.

**Effect of Electrode Distance on the Breakdown Voltage**

It can also be observed from Figure.6 that under the same doping concentration, longer electrode distance yields higher breakdown voltage. A higher slope of the curve can be observed as well when the distance is under 5um. This is because when the distance is small, the depletion area and the heavy doped will affect each other, as is discussed below.

1) When \( x_n << d \), the situation and corresponding \( E-x \) relationship is shown in Figure.8(a) and (b). Enlarging \( d \) will lower the electric field strength in depletion region under the same voltage drop. Therefore, higher reverse bias is needed for the diode to reach the critical electric field strength and breakdown.

2) When \( d \) is too small, the substrate is light doped or reverse bias is too large, the depletion area is close to the heavy-doped area. This situation is similar to the punch through phenomenon in MOSFET or BJT [15]. The depletion region will not expand obviously because of the heavy doping of n+ area. This situation and its \( E-x \) relationship is shown in Figure.8(c) and (d). The electric field strength grows faster when voltage applied increases. Therefore, the breakdown voltage will be lower than normal avalanche situation.

Equation (3) and (4) implies that change of distance will not affect the value of \( E_{crit} \) directly. However, with longer electrode distance, higher voltage is needed to reach critical electric field strength.
The spatial relationship between the depletion area and heavy-doped area and the corresponding E-x relationship.

**Effect of the Comb Teeth Number on the Post-Breakdown Resistance**

The diodes fabricated in this paper is mainly used for ESD protection and will work under reverse biased condition. Lower resistance after breakdown means better protection performance. The resistance of the diodes with 5um electrode distance after breakdown is measured.

All the resistance values are achieved by the slope of the I-V curve at 50mA. It can be observed that more comb teeth can achieve lower post-breakdown resistance. The increase of the teeth number enlarges the contact area, causing the decrease of the resistance and allowing larger current to pass through the diode, thus improve the ESD protection performance. However, more failure in lift-off process is discovered when the number is higher than 10.

**Conclusion**

A CMOS process compatible planar Schottky diode with special comb teeth structure is designed and fabricated. The breakdown voltage of which can be easily controlled by optimizing the doping concentration of the substrate and the distance between the diodes. Breakdown voltage can vary from 2 to 16V by adjusting concentration between $5 \times 10^{13}$ cm$^{-3}$ and $1 \times 10^{16}$ cm$^{-3}$ and electrode distance between 4um and 11um. The post-breakdown resistance is lowered by adding the number of the comb teeth. The Schottky diodes fabricated can withstand current larger than 100mA. Therefore, excellent ESD protection performance with this Schottky diode can be expected.
Acknowledgment

The work is done in Center for Advanced Electronic Material and Devices (AEMD) at Shanghai Jiao Tong University.

References

[1] C. Duvvury, A. Amerasekera, Handbook of Failure Modes, Reliability Issues, and Case Studies, ESD in Silicon Integrated Circuits, 2nd Edition John Wiley & Sons, Ltd, 2002.

[2] Amerasekera A, Duvvury C. The impact of technology scaling on ESD robustness and protection circuit design. IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part A, 1995, 18(2):314-320.

[3] J K Hartman, B McCampbell. Zener diode for protection of integrated circuit explosive bridge. USA Patent, US5309841, 1994.

[4] D Novotney, B Welch, et al. Semiconductor bridge development for enhanced ESD and RF immunity. Joint Propulsion Conference & Exhibit. 2013.

[5] D Bouangeune, S S Choi, et al. Bidirectional Transient Voltage Suppression Diodes for the Protection of High Speed Data Line from Electrostatic Discharge Shocks. Journal of Semiconductor Technology and science. 2014, 14(1): 001.

[6] C L Zuo, Research on the ESD protection theoretical simulation and experimental of Semiconductor Bridge initiators. Nanjing University of Science and Technology, 2016. (in Chinese)

[7] T A Baginski, S L Taliaferro, et al. Novel electroexplosive device incorporating a reactive laminated metallic bridge. Journal of Propulsion and Power, 2001, 17(1): 184.

[8] C S Lin. On the design and fabrication of anti-static-charge ignition chip. National Taiwan University, 2009. (in Chinese)

[9] D A. Neamen. Semiconductor Physics and devices: Basic Principles, Fourth Edition. Beijing: Publishing house of Electronics Industry, 2013.

[10] L L He. The effect of annealing treatment on reverse breakdown voltage of Schottky diodes. Harbin University of Science and Technology, 2007. (in Chinese)

[11] S Chattopadhyay, L K Bera, et al. Pt/p-strained-Si Schottky diode characteristics at low temperature. Applied Physics Letters, 1997, 71(7):942.

[12] Q Li, J Y Wang, et al. Design and Fabrication of Schottky Diode with Standard CMOS Process. Chinese Journal of Semiconductors, 2005, 26(2): 235.

[13] D Y Han. Design on Single-Chip Semiconductor Bridge Integrated with Non-Ignition Circuit. Shanghai Jiao Tong University, 2008. (in Chinese)

[14] X B Chen, Q Z Zhang, et al. Microelectronic devices. Third Edition. Beijing: Publishing House of Electronics Industry. 2011.

[15] J Urresti, S Hidalgo, et al. Lateral punch-through TVS devices for on-chip protection in low-voltage applications. Microelectronics Reliability, 2005, 45: 1181.