Multilevel common-ground inverter with voltage boosting for PV applications

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Abstract
Nowadays, transformer-less Photovoltaic-based grid-connected inverters are more popular in renewable energy application due to their reduced size, cost, and high efficiency. However, the absence of galvanic isolation leads to the flow of leakage current in such system hindering personal safety, and deteriorating power quality. Therefore, this paper presents a five-level transformer-less inverter topology for PV applications with less component count and reduced complexity. The proposed inverter topology completely eliminates the common mode leakage current. Besides, the proposed topology has an inherent capability to boost the voltage without using any magnetic component or boosting circuit, and is based on the principle of switched/auxiliary capacitor. The proposed topology do not have any limitation of modulation index since the auxiliary capacitors are naturally balanced, hence less complex or no dedicated control scheme is required for balancing/regulating the auxiliary capacitor voltages. In order to verify the performance of the proposed inverter topology, a laboratory prototype is developed which confirms the operation, and feasibility of the proposed inverter. Results depicting the output voltage, load current, and voltage across the auxiliary capacitor are presented for various operating conditions. Further, simulation results depicting the leakage current in the proposed, H5, and H6 topologies are included. Finally, a quantitative comparison study is done, highlighting the benefits of the proposed inverter topology regarding boosted voltage, elimination of leakage current, and reduced component count.

1 | INTRODUCTION

Solar photovoltaic (PV) is one of the cleanest, reliable, emission free and widely available energy sources among all renewable energies. In recent years, PV production has increased rapidly in commercial and residential buildings. According to global market outlook of 2018–2022 published by Solar Power Europe, the global solar power generation will reach up to 1,270.5 GW at the end of 2022. In India, it is expected to reach 78.4 GW and 209 GW in China. For the integration of renewable energy sources with the utility grid, power electronic converters play an important role. A conventional PV grid-connected system has two stages namely, dc-dc and dc-ac conversion. For the grid-tied PV systems, dc-ac conversion stage is mandatory to feed the AC power into the utility grid. These grid-tied inverters are majorly classified into non-isolated system and galvanic-isolated system [1]. In general, galvanic isolation is provided by connecting a line frequency transformer on the AC side or a high frequency transformer on the dc side of the inverter. However, line frequency transformers are bigger in size, bulky, costly, difficult to install and reduces the efficiency of the overall system. Whereas, high frequency transformers are smaller in size and cheaper as compared to line frequency transformers. Increase in the number of power conversion stages results in increased complexity and reduced efficiency of the system [2, 3].

To overcome the above demerits, transformer-less grid-connected inverters are more popular in renewable energy application [4, 5]. It results in reduced size, cost and achieve high...
efficiency. Opting for a transformer-less operation leads to the existence of leakage current between PV array and grid, due to PV-to-ground parasitic capacitance [6–8]. To overcome this, it is essential to curtail the leakage current as it leads to deteriorated power quality, personal safety issues and electromagnetic interference (EMI).

In order to eliminate the existing leakage current, a lot of modified transformer-less inverter topologies have been proposed in the literature. These topologies reduce the leakage current by isolating PV array from the utility grid in order to maintain a constant common mode (CM) voltage or by connecting the grid neutral to the midpoint of the dc-link bus or by connecting the grid neutral with PV arrays negative terminal. The CM voltage can be kept constant by disconnecting the ac or dc side of the full-bridge inverter during the freewheeling modes, such as family of H5 [9, 10], H6 [11], HERIC inverters [12] etc. In H5 topology, one switch is connected between the DC link and bridge arms [13]. In the family of H6 topologies, two extra switches are inserted between the DC link and bridge arms. In the family of highly efficient and reliable inverter concept (HERIC) topologies, a freewheeling branch is inserted between full bridge and output filters. These extra switches or branch are inserted to disconnect the path from PV array to the utility grid during freewheeling mode, as shown in Figure 1. These topologies minimize the leakage current by disconnecting the path for some period but are not able to eliminate it [14]. Such topologies require two filter inductors, which lead to increase in size and cost. Moreover, it is difficult to minimize the leakage current because of internal capacitors of switches. In addition, conduction losses are high due to more than three conducting switches in series during active mode [15].

The half-bridge and neutral point clamped (NPC) based topologies have mid-point of the dc link connected with grid neutral, as depicted in Figure 2 [16]. Half-bridge and NPC inverters minimize the leakage current by using two and four semiconductor switches respectively and one filter inductor, but output voltage peak is half of the input dc link voltage [17]. The PV modules are being low voltage type, therefore it is imperative to employ a dc-to-dc boost converter to match the grid voltage requirements. This additional power conversion stage leads to reduced efficiency and hence increased cost. [18].

Recently, common ground type (CGT) based inverter topologies are popular and are depicted in Figure 3. In these type of topologies, utility neutral is directly tied with the negative terminal of the PV module leading to the short-circuiting of PV-to-ground parasitic capacitance. The benefit of the CGT based inverter over other topologies is the complete elimination of the leakage current [19]. Among CGT based inverters, karschny transformer-less inverter consists of five switches, two diodes, two inductors and one capacitor. The circuit structure of Karschny transformer-less inverter, as shown in Figure 3(a) [20] is highly complex requiring sophisticated control method and is incapable of delivering the reactive power to the utility grid. The proposed three-level inverter topology [21], as depicted in Figure 3(b), suppresses the leakage current almost zero but it not able to boost the output voltage. Another CGT based five-level inverter presented in [22], minimizes the number of used components and suppresses the leakage current but is not
able to boost the output voltage. Further, three CGT based single phase transformer-less inverters based on flying capacitor principle [23], these topologies consist of four semiconductor switches, one diode, one flying capacitor and single filter inductor. The attractive feature of these topologies is that during the active mode, the maximum number of conducting switches is 2, resulting in reduced conduction loss.

Another CGT topology presented in [24], yields in zero leakage current. It consists of five switches, one flying capacitor and a single inductor with no voltage boosting ability. Despite boosting ability of topology in [25], the component count stands high. While the magnetic-based topology in [26] require two inductors and capacitors has reduced efficiency. Topology in [27], connects the neutral of the grid with the negative terminal requires six switches, three inductor with two capacitor while generating a three-level waveform.

Generally, in CGT based inverter, auxiliary capacitors are used. These auxiliary capacitors are charged up-to the desired voltage level in the positive half cycle and are discharged during the negative half cycle to generate the desired output voltage. This process is repeated in every fundamental cycle of the grid voltage. Depending on the number of auxiliary capacitors, their respective voltages and the sequence of their interconnection with the source, the inverter generates an output voltage with a fixed number of levels. In practical applications, it is desirous to generate more number of voltage levels in order to reduce the filter size, to decrease voltage stress and to increase efficiency. More number of voltage levels increase the number of auxiliary capacitors which increases the number of sensors and hence the cost of the circuit becomes higher.

This paper examines a grid-tied transformer-less inverter is proposed based on common ground type (CGT) with two auxiliary capacitor. The negative terminal of dc bus is directly connected to neutral line of utility. This leads to the short circuiting of PV-to-ground parasitic capacitance, hence the CM leakage current is completely eliminated. The proposed inverter topology has the inherent voltage boosting capability without using the magnetic components, thereby eliminating the need for an additional boosting stage. Moreover, it generates multilevel output voltage which results in reduced voltage stress, reduced filter size and increased efficiency. The proposed topology does not have any limitation on the achievable modulation index. This inverter topology has \( \leq 3 \) on state switches in the grid current path during the power transfer mode, which leads to reduced conduction losses. The key contribution of this paper is the devising of a five-level inverter with zero leakage current and reduced component count for PV application.

This paper is organized as follows: Structure and operating modes of the proposed inverter topology are explained in Section II. Pulse-width modulation scheme for the proposed topology is elucidated in Section III. Power loss analysis and design guidelines are described in Section IV. A quantitative comparison of existing transformer-less inverters with proposed inverter is done in Section V. Section VI describes the experimental results of proposed inverter topology. Finally, the paper is summarized.

2 | STRUCTURE OF THE PROPOSED INVERTER TOPOLOGY

One of the main objectives of the proposed inverter topology is to completely eliminate the CM leakage current and boost the output voltage without the need for a complex power electronic configuration. This feature makes it a potential candidate for transformer-less grid-tied inverter for PV applications.

2.1 | Structural description of the proposed five-level boosted inverter topology

The schematic of the proposed topology is shown in Figure 4. It consists of seven power switches, two auxiliary capacitors and one diode for synthesizing a five-level output voltage waveform.

2.2 | Operating modes of proposed inverter topology

Various operating modes of the proposed inverter topology are shown in Figure 5. The figure describes switching state of
FIGURE 5  Modes of operation with unity power factor.

TABLE 1  Switching states of the proposed inverter topology

| $V_0$  | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ |
|--------|-------|-------|-------|-------|-------|-------|
| $2V_{dc}$ | 1     | 1     | 1     | 1     | 0     | 0     |
| $V_{dc}$  | 0     | 1     | 1     | 0     | 0     | 1     |
| 0        | 1     | 1     | 0     | 0     | 0     | 0     |
| $-V_{dc}$ | 0     | 1     | 0     | 0     | 0     | 1     |
| $-2V_{dc}$ | 0     | 0     | 0     | 0     | 1     | 1     |

switches, charging and discharging state of auxiliary capacitors, grid-current path (solid red and blue-lines represent the output current path and charging path of auxiliary capacitors respectively) at unity power factor. The appropriate switching states to be employed are listed in Table 1. The switches $(\bar{S}_3), S_6$ works in complementary to switches $S_3$ and $S_1$ respectively. The input voltage is designated as $V_{dc}$. The combination of switches $S_1, S_6$, capacitor $C_1$ and diode $D$ can boost and generate the voltage level $V_{dc}$ and $2V_{dc}$ across the terminals $ab$. Thus, the peak of the ac output voltage is twice of the input source voltage $V_{dc}$, while the other auxiliary capacitor $C_2$ helps to generate the negative levels of the output voltage. To generate the desired output voltage waveform, the voltage across the auxiliary capacitor $C_1$ and $C_2$ is maintained at $V_{dc}$ and $2V_{dc}$ respectively. The proposed topology has five modes of operation, i.e. $+2V_{dc}$, $+V_{dc}$, $0$, $-V_{dc}$ and $-2V_{dc}$, wherein, zero level of output voltage mode is common for both the half cycles, as depicted in Figure 5. The different operating modes of the proposed topology are detailed as follows.

**Mode 1:** During this operating mode, switches $S_1, S_2, S_3$ are operated. By applying the Kirchhoff voltage law (KVL), output voltage is obtained as:

$$V_o = V_{dc} + V_{c1} = 2V_{dc}, \quad i_o > 0.$$  \hspace{1cm} (1)

As the auxiliary capacitor $C_3$ is in parallel with $C_1$ and source voltage, turning ON the switch $S_5$ changes its up to $2V_{dc}$.

**Mode 2:** During this operating mode, switches $S_2, \bar{S}_3$ and $S_6$ are operated. Capacitor $C_1$ is charged from source voltage, while $C_2$ is bypassed ad its voltage remains intact. By applying the KVL, output voltage is obtained as:

$$V_o = V_{c1} = V_{dc}, \quad i_o > 0.$$ \hspace{1cm} (2)

**Mode 3:** During this operating mode, switches $S_1, S_2$ and $\bar{S}_3$ are operated. The capacitor $C_1$ and $C_2$ are in series with source voltage. For positive load current, capacitor $C_1$ is discharged and $C_2$ is charged while for negative load current, vice-versa.
By applying the KVL, output voltage is obtained as:
\[ V_o = V_{dc} + V_{c1} - V_{c2} = 0, \text{ if } i_o > 0 \text{ and } i_o < 0. \] (3)

Mode 4: During this operating mode, switches \( S_2, S_3 \) and \( S_6 \) are operated. The capacitor \( C_1 \) is charged to source voltage while \( C_2 \) is discharged. By applying the KVL, output voltage is obtained as:
\[ V_o = V_{c1} - V_{c2} = -V_{dc}, \text{ if } i_o < 0. \] (4)

Mode 5: During this operating mode, the generated output voltage level is \(-2V_{dc}\) which is provided by auxiliary capacitor \( C_2 \) through switches \( \bar{S}_3 \) and \( S_5 \). In this mode, capacitor \( C_1 \) is charged to source voltage. By applying the KVL, output voltage is obtained as:
\[ V_o = -V_{c2} = -2V_{dc}, \text{ if } i_o < 0. \] (5)

3 | PULSE-WIDTH MODULATION SCHEME

In this section, the pulse-width modulation scheme and the developed logic functions are presented. In Figure 6(a), four carrier signals \((V_{c1}, V_{c2}, V_{c3}, \text{ and } V_{c4})\) are compared with the reference signal \((V_{ref} = A_m \sin \omega t)\). A total of four zones (I, II, III and IV) are defined for each switching state to ease the deliberation of gating pulse generation process. As per the operating modes explained in Section II, logic functions are formulated for each of the switches to generate the desired five-level output voltage, and is demonstrated in Figure 6(b).

The rationale behind the logic operation involves those entries wherein a particular switch needs to be ON. As an example, consider for \( S_1 \), since it is ON for zero and 2\( V_{dc} \) level, the comparator outputs corresponding to these two levels are added (logical OR).

4 | POWER LOSS ANALYSIS AND DESIGN GUIDELINE

In this section, the methodology and relevant mathematical expressions to evaluate the power losses of various switches in the proposed topology is presented.

4.1 | Evaluation of conduction loss

To evaluate the conduction losses of power semiconductor devices, an equivalent circuit for zone-I (switching between 2\( V_{dc} \) and \( V_{dc} \) level) is shown in Figure 7. This particular equivalence is obtained by considering the parasitic resistance of power switches, auxiliary capacitors and filter inductor \( (L_f) \), and assuming that the voltage across auxiliary capacitors are well balanced, i.e. \( V_{dc} \) and 2\( V_{dc} \) for \( C_1 \) and \( C_2 \) respectively. The output voltage is defined as:
\[ V_o = \begin{cases} 
2V_{dc} & 0 < t < d_1T_c \\
V_{dc} & d_1T_c < t < T_c 
\end{cases} \] (6)
Voltage across $L_f$ during this switching operation is expressed as:

$$V_{L_f} = \begin{cases} 2V_d - V_g & 0 < t < d_1 T_i \\ V_d - V_g & d_1 T_i < t < T_i \end{cases}. \quad (7)$$

By applying the volt-second balance, we obtain:

$$\int_0^{d_1 T_i} (2V_d - V_g) d(t) + \int_{d_1 T_i}^{T_i} (V_d - V_g) d(t) = 0 \quad (8)$$

Solving (8) yields duty ratio ($d_1$) as,

$$d_1 = \frac{V_g}{V_d} - 1. \quad (9)$$

By applying the Kirchhoff voltage law for the loops in Figure 7, we obtain:

$$i_1 = \frac{2V_d + (r_2 + r_d) d_1 i_g}{r_1 + r_1 + r_2 + r_2 + r_d} \quad (10)$$

$$i_2 = \frac{V_d + (r_1 + r_d)(1 - d_1) i_g}{r_D + r_1 + r_6}. \quad (11)$$

Once, the instantaneous current are obtained. The conduction losses are evaluated using the current RMS value using the following relation:

$$P_{c_1} = R_1 [i_{r_1}^2] + R_2 [i_{r_2}^2] + (1 - d_1) [i_{g}^2] + \frac{r_3 [i_{g}^2]}{1 - d_1} \quad (12)$$

$$P_{c_2} = R_3 [i_{g}^2] + (1 - d_1) [i_{g}^2] + \frac{r_2 [i_{g}^2]}{1 - d_1} \quad (13)$$

where $R_1 = r_4 + r_1 + r_2 ; R_2 = r_2 + r_d ; R_3 = r_4 + r_d$. By using same concept, conduction losses for all zones can be deduced. Finally, the total conduction loss ($P_c$) is obtained as follows:

$$P_c = P_{c_1} + P_{c_2} + P_{c_3} + P_{c_4} \quad (15)$$

where $L_f$: filter inductor, $d_1$: duty cycle during zone 1, $T_i$: switching period, $f_s$: switching frequency, $V_d$: generated voltage, $V_d$: dc source voltage, $V_{L_f}$: voltage across filter inductor, $r_1$, $r_2$, $r_3$, $r_4$, $r_5$, $r_6$, $r_D$, $r_1$, $r_2$: internal resistance of all switches, diode and capacitors, $P_c$: conduction loss.

### 4.2 Evaluation of switching loss

Switching losses of individual switches depend on their turning on/off time, active current through them and their blocking voltage. During positive-half cycle, current through switch $S_1$ can be expressed as:

$$i_{S_1 \text{on}} = \begin{cases} \frac{I_g}{\pi} & 0 < t < d_1 T_i \\ 0 & d_1 T_i < t < T_i \end{cases}. \quad (16)$$

Hence, the average value of current through $S_1$ is expressed as:

$$I_{S_1 \text{avg}} = \frac{1}{T_i} \int_0^{d_1 T_i} \frac{I_g}{\pi} d(t) = \frac{I_g d_1}{\pi}. \quad (17)$$

As per the circuit arrangement, the maximum blocking voltage for $S_1$ is $V_d$ and using the average current of switch $S_1$ as described in (17), the switching power losses in $S_1$ can be obtained as:

$$P_{sw_1} = f_s \left[ \int_0^{t_{on}} \frac{1}{6} V_d \frac{I_g d_1}{\pi} d(t) + \int_0^{t_{off}} \frac{1}{6} V_d \frac{I_g d_1}{\pi} d(t) \right]$$

$$= \frac{V_d I_g d_1}{6\pi} (t_{on} + t_{off}). \quad (18)$$

During the negative-half cycle, current through switch $S_1$ can be expressed as:

$$i_{S_1 \text{on}} = \begin{cases} 0 & 0 < t < d_1 T_i \\ \frac{d_1 I_g}{(1 - d_1)\pi} d_1 T_i < t < T_i \end{cases}. \quad (19)$$

Hence, the average value of current through $S_1$ is expressed as:

$$I_{S_1 \text{avg}} = \frac{1}{T_i} \int_{d_1 T_i}^{T_i} \frac{d_1 I_g}{(1 - d_1)\pi} d(t) = \frac{I_g d_1}{\pi}. \quad (20)$$

Switching power losses in $S_1$ during negative-half cycle can be obtained as:

$$P_{sw_1} = f_s \frac{V_d I_g d_1}{6\pi} (t_{on} + t_{off}).$$

Within full cycle of line-frequency total switching losses in $S_1$ can be expressed as:

$$P_{sw} = f_s \frac{V_d I_g d_1}{3\pi} (t_{on} + t_{off}).$$

Extending the above principle for the remaining power switches. where $I_g$: grid current, $I_{S_1 \text{avg}}$: average current stress of $S_1$, $P_{sw_1}$: switching loss of $S_1$, $t_{on}$, $t_{off}$: turning on and off time of switch.
4.3 | Inductance value

The current through inductor within a complete switching cycle is calculated as

\[ i_{L_f}(t) = \frac{1}{L_f} \int_0^t V_{L_f}(t) d(t) + i_{L_f}(0). \]  \hspace{1cm} (21)

Therefore, ripple current of the inductor is expressed as:

\[ \Delta i_{L_f} = \frac{(V_d - V_g)(1 - d_1) E}{L_f}. \]  \hspace{1cm} (22)

By using (9) in (22), it written as:

\[ \Delta i_{L_f} = \frac{1}{L_f f_s} \left( 2V_d - 3V_g + \frac{V^2}{V_d} \right). \]  \hspace{1cm} (23)

So, \( L_f \) can be evaluated as:

\[ L_f = \frac{1}{\Delta i_{L_f} f_s} \left( 2V_d - 3V_g + \frac{V^2}{V_d} \right). \]  \hspace{1cm} (24)

where \( i_{L_f} \): current through the inductor, \( \Delta i_{L_f} \): ripple current of the inductor

4.4 | Auxiliary capacitance value

Voltage across the auxiliary capacitor \( C_1 \) is evaluated as:

\[ V_{C_1}(t) = \frac{1}{C_1} \int_0^t i_{C_1}(t) d(t) + V_{C_1}(0). \]  \hspace{1cm} (25)

From Figure 5(a) and (b), it is observed that during the zone II, discharging current of capacitor \( C_1 \) i.e. \( (i_{C_1}) \) is same as inductor current \( (i_{L_f}) \). Hence, ripple voltage across capacitor \( C_1 \) can be obtained as:

\[ \Delta V_{C_1} = \frac{i_{C_1} d_1}{f_s C_1} = \frac{i_{L_f}}{f_s C_1} \left( \frac{V_g}{V_d} - 1 \right). \]  \hspace{1cm} (26)

So, \( C_1 \) can be evaluated as:

\[ C_1 = \frac{i_{L_f}}{f_s \Delta V_{C_1}} \left( \frac{V_g}{V_d} - 1 \right). \]  \hspace{1cm} (27)

Similarly, during the zone III, discharging current of capacitor \( C_2 \), i.e. \( (i_{C_2}) \) is same as inductor current \( (i_{L_f}) \), as depicted in Figure 5(c) and (d). Hence, by applying the same procedure for zone III, the value of \( C_2 \) is obtained as:

\[ C_2 = \frac{i_{L_f} V_g}{f_s \Delta V_{C_2} V_d}. \]  \hspace{1cm} (28)

where \( V_{C_1} \): voltage across \( C_1 \), \( \Delta V_{C_1} \): ripple voltage across \( C_1 \), \( i_{C_1} \): passing current through \( C_1 \)

5 | COMPARISON WITH OTHER SIMILAR TOPOLOGIES

In this section, a comprehensive yet qualitative comparison of the proposed topology against the state-of-the-art inverters is carried out. Table 2 summarizes the various figures of merit considered for the comparative study. The comparison is done in terms of number of components, the number of conducting switches in each cycle, number of output voltage levels, presence of leakage current and boosting ability. The number of power switches is a crucial factor in inverters dictating the overall size and cost. The increase in the number of switches escalates the cost, size and complexity of the circuit, while the number of on-state switches affects the overall conduction and switching losses, and in turn the efficiency of the inverter. From the comparative study, following are the key observations:

1. The required input dc link voltage by the half-bridge and NPC based inverters is twice of the peak grid voltage.
2. None of the topologies under consideration have the boosting ability, therefore additional power conversion stage is required to fulfil the grid voltage requirement.
3. From Table 2, only CGT based inverters have the ability to eliminate the leakage current, whereas other existing grid-tied inverters are capable of only minimizing the leakage current.
4. Karschny inverter does not have the ability to process reactive power and thus can not support the utility grid during the low voltage ride through kind of situation.
5. In [22], the inverter topology requires three auxiliary capacitors to generate five-level output voltage and also requires complex control strategy for balancing the auxiliary capacitor voltages.

Different to the existing topologies, the proposed inverter has inherent voltage boosting capability within a single-stage conversion. The proposed structure is devised with reduced active and passive components resulting as a cost-effective high-power density solution and is structured to inherently eliminate the leakage current due to PV-to-ground parasitic capacitance. The proposed topology have low complexity control strategy for balancing/regulating the auxiliary capacitor voltages, since capacitors are naturally balanced.

6 | RESULTS

6.1 | Simulation verification

In order to verify the theoretical analysis, the proposed single-phase transformer-less boosting inverter is simulated in MATLAB Simulink. A programmable constant current sink is applied as the load on the inverter. The set of simulated waveforms
TABLE 2  Comparative analysis of available grid-tied inverters with proposed topology

| Inverter Topologies             | Number of Components | Maximum Conducting Switches | Output Voltage levels | Leakage current | Boosting Ability | Input DC-link voltage |
|---------------------------------|----------------------|-----------------------------|-----------------------|-----------------|------------------|-----------------------|
| H-Bridge [6]                    | 4 0 0 0 2            | 2                           | 3                     | Non-Zero        | No               | Vdc                   |
| H5 [10]                         | 5 0 1 0 2            | 3                           | 3                     | Non-Zero        | No               | Vdc                   |
| H6 [11]                         | 6 2 2 0 2            | 3                           | 3                     | Non-Zero        | No               | Vdc                   |
| HERIC [12]                      | 6 0 1 0 2            | 2                           | 3                     | Non-Zero        | No               | Vdc                   |
| Half-Bridge [16]                | 2 0 2 0 1            | 1                           | 2                     | Non-Zero        | No               | 2Vdc                  |
| NPC [17]                        | 4 2 2 0 1            | 2                           | 3                     | Non-Zero        | No               | 2Vdc                  |
| ANPC [18]                       | 6 0 2 0 1            | 2                           | 3                     | Non-Zero        | No               | 2Vdc                  |
| Conergy-NPC [14]               | 4 0 2 0 1            | 2                           | 3                     | Non-Zero        | No               | 2Vdc                  |
| Karschny [20]                   | 5 2 1 1 1            | 3                           | 3                     | Zero            | No               | Vdc                   |
| Inverter in [21]                | 4 2 3 0 1            | 2                           | 3                     | Zero            | No               | Vdc                   |
| Inverters in [22] Type-I        | 4 0 2 0 1            | 2                           | 3                     | Zero            | No               | Vdc                   |
| Inverters in [22] Type-II       | 6 0 3 0 1            | 3                           | 5                     | Zero            | No               | Vdc                   |
| Inverter in [28] Type-I         | 5 0 2 0 1            | 3                           | 3                     | Zero            | No               | Vdc                   |
| Inverters in [23] Type-II       | 4 1 2 0 1            | 2                           | 3                     | Zero            | No               | Vdc                   |
| Inverters in [23] Type-III      | 4 0 2 0 1            | 1                           | 3                     | Zero            | No               | Vdc                   |
| Proposed Topology               | 7 1 2 0 1            | 3                           | 5                     | Zero            | Yes              | 0.5Vdc                |

FIGURE 8  Simulation waveforms of leakage current for (a) H-5 (b) H-6 (c) HERIC (d) Proposed Inverter

consists of output voltage, current and charging discharging voltage of capacitor $C_1$ and $C_2$ for various conditions, shown in Figures 9 and 10. To verify the reactive power capability of proposed inverter, simulation for lagging and leading load power factor is performed and the result is displayed in Figure 9. The leakage current waveform for the proposed model, H5, H6 and HERIC topologies are compared with proposed topology, as demonstrated in Figure 8. From the figure, it can be seen that the proposed topology have the ability to eliminate the leakage current completely which is 0 mA while other compared topologies have about 100 mA.

In order to verify the performance during unpredictable atmospheric conditions and variable load, the inverter is simulated for variable source voltage and load, the corresponding waveforms are shown in Figure 10. From all the above results, it is quite evident that the proposed topology operated as intended and with all the previously mentioned features, it qualifies as a potential candidate for transformer-less PV operation.

6.2  | Experimental verification

This section presents the experimental results of the proposed inverter topology obtained using the laboratory prototype. The rating of components and various other parameters are listed in Table 3. The gating-signals for the power switches are applied by using TLP250 drivers. The PWM signals are generated using the DS1202 dSPACE controller. The five-level output voltage, voltage across the auxiliary capacitors along with output current for no-load and on-load, are shown in Figure 11. The input
FIGURE 9  Simulation results at (a) Lagging load power factor (b) Leading load power factor

FIGURE 10  Simulation results at (a) Variable source voltage (b) Variable load

TABLE 3  Used components and required parameters for laboratory prototype

| Components                  | Description       | Value       |
|-----------------------------|-------------------|-------------|
| $S_1, S_2, S_3, S_4, S_5, S_6$ | IRFP460N          | 500V/20A    |
| Power diode                 | MUR1560           | 600V/15A    |
| Gate driver                 | IC                | TLP 250     |
| Input DC-link voltage $V_{dc}$ | -                 | 100V        |
| Output voltage $V_0$        | -                 | 200V        |
| Line frequency              | -                 | 50 Hz       |
| Switching frequency $f_s$   | -                 | 5 kHz       |

TABLE 4  Voltage stress on power switches

| Switch | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $D$ |
|--------|-------|-------|-------|-------|-------|-------|-----|
| Voltage stress | $V_{dc}$ | $2V_{dc}$ | $2V_{dc}$ | $2V_{dc}$ | $2V_{dc}$ | $V_{dc}$ | $V_{dc}$ |

From the Figure 11, it is seen that the voltage across $C_1$ and $C_2$ are well balanced around $V_{dc}$ and $2V_{dc}$ respectively, i.e. 100 V and 200 V. This has been achieved without using any type of voltage or currents sensors. Further, the output waveforms pertaining to loading of the inverter are shown in Figure 11(b).
The peak value of the injected current is 10 A. It is very crucial to investigate the blocking voltages as they dictate the switching loses. The blocking voltage waveform across each power switch and diode are demonstrated in Figure 12. In order to compare the efficiency of H-5, HERIC and proposed topology, the efficiency versus output power curve is shown in Figure 13. The curve is obtained at same circuit parameters, input and output voltage. From the Figure 13 the efficiency of the proposed topology is competent enough with those of its popular counterparts.

7 CONCLUSION

This paper examines a transformer-less grid-tied inverter is proposed based on common-ground type connection with reduced/zero ground leakage current. The proposed topology exhibit inherent voltage boosting capability in single-stage power conversion with no need of any magnetic component or boosting circuit. It generates five-level output voltage which results in raised efficiency, minimized harmonics and reduced less filter size with lesser number of overall components (switches, diodes, gate driver and magnetic components). Also, does not have any limitation of modulation index for the entire range of output power. The auxiliary capacitors have the ability of self-balanced voltage and hence required controller is less complex. The performance of the proposed inverter topology is examined by using the laboratory prototype and detailed simulations. Hardware results obtained to confirm the operation and feasibility of the proposed inverter are presented. Obtained results demonstrates the output voltage, load current and balanced voltage across auxiliary capacitors. Also, it shows the blocking voltage of used switches. The simulation results for the leakage current confirmed the ability of the proposed topology in achieving zero leakage current. Finally, the quantitative comparison study confirms the benefits of the proposed inverter topology regarding boosted voltage, elimination of leakage current and reduced component count against the existing topologies.

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