Research Article

A Test Data Compression Scheme Based on Irrational Numbers Stored Coding

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Test question has already become an important factor to restrict the development of integrated circuit industry. A new test data compression scheme, namely irrational numbers stored (INS), is presented. To achieve the goal of compress test data efficiently, test data is converted into floating-point numbers, stored in the form of irrational numbers. The algorithm of converting floating-point number to irrational number precisely is given. Experimental results for some ISCAS 89 benchmarks show that the compression effect of proposed scheme is better than the coding methods such as FDR, AARLC, INDC, FAVLC, and VRL.

1. Introduction

According to Moore’s law, the integration level of the microchips doubles every 18 to 24 months. As a result, the volume of test data increased dramatically; the test costs become higher; the contradictions between test efficiency and test quality are sharpening. The test data compression technology comes into being to solve the above problems.

Coding compression technology has been widely used because it has such advantages as simple encoding and decompression structure which is independent of the tested chip. A certain encoding scheme is used to encode the original test set. The length of the encoded data is less than the original test set, so as to reduce the test data.

The test set is divided into the sequences of specific law, which can be replaced with new codeword generated by some kinds of coding method. According to the change rule of the length from the original sequence to the codeword, coding methods can be divided into four categories. The first category is fixed-to-fixed coding method, such as dictionary code [1]. The second category is fixed-to-variable coding method, such as Huffman code [2], 9C code [3]. The third category is variable-to-fixed encoding method, such as run-length code [4]. The fourth category is variable-to-variable coding method, such as Golomb code [5], FDR code [6], EFDR code [7], and alternation and run-length code [8].

Among them, the compression method of the first category is the most simple one, but it has the lowest compression efficiency. The compression efficiency of the fourth category is high, but its hardware overhead is larger. The second and third categories have good applicability, which are between the first and fourth categories in terms of compression method, compression efficiency, hardware overhead, and so forth.

It is a new original method to use irrational number to compress test data. It is creative. A scheme of test data compression based on irrational number dictionary code [9] is presented. The encoding rule of this scheme is simple, and the do not-care bit need not be assigned, but it takes extra storage space to store the data dictionary additionally.

A new test data compression scheme based on irrational numbers stored (INS) is presented. It is a fixed-to-variable coding method, which has simple encoding rule and can obtain good compression effect. In this scheme, the test set is converted into floating-point numbers firstly, and then the floating-point numbers are converted into irrational numbers in form of $\sqrt{x}$ (where the numbers $x$ and $r$ are integers) by the successive approximation method. So the storage of the test set can be translated into the storage of...
radicand (integer) and root number (integer). The minimum of corresponding radicand and root number can be found with faster convergence speed. Better compression effect can be obtained when using the INS coding scheme.

The organization of the paper is as follows. Section 2 explains the algorithm of the proposed scheme and gives an example. Section 3 proves the feasibility of the algorithm of the proposed scheme theoretically. The structure of decompressor is presented in Section 4. Section 5 reports the experimental results and analyzes the compression ratio theoretically. Finally Section 6 concludes the paper.

2. INS Coding

In this section, the algorithm of INS coding is described firstly. Then, the flowchart of the scheme is given. Lastly, an example is provided.

2.1. Encoding Rule. The concrete steps of INS coding are as follows.

1. At first, generate the determinate complete test set named T by automatic test pattern generation tools.
2. Then cascade the entire test vector, and connect the head of a vector to the tail of previous vector, remembered as S.
3. Take the first N bits of the test set, and then convert them into a hexadecimal number every four bits a group according to the rules shown in Table 1. Add a decimal point after the first digit, and a hexadecimal floating-point number named f is formed.
4. Calculate the value of x and r in the formula \( \sqrt{x} = f \), by dichotomy to successive approximate f. In this scheme, if the first several bits of f and the root of \( \sqrt{x} \) are exactly the same, that is to say, the two are approximately equal to, then consider the following. (I) Calculate \( f^2 \) first; set bot = \( \lfloor f^2 \rfloor \), top = bot + 1, \( r = 2 \). (II) Calculate \( \sqrt{\text{bot}} \), if its value is equal to f, note x = bot, r, and then go to step (5). Otherwise, calculate \( \sqrt{\text{top}} \), if its value is equal to f, note x = top, r, and then go to step (5). (III) Consider bot = \( \lfloor \text{bot} \ast \sqrt{\text{bot}} \rfloor \), top = \( \lfloor \text{top} \ast \sqrt{\text{top}} \rfloor \), and \( r = r + 1 \). (IV) Set \( \text{mid} = \lfloor (\text{bot} + \text{top})/2 \rfloor \), calculate \( \sqrt{\text{mid}} \), if its value is equal to f, note x = mid, r, and then go to step (5). If its value is greater than f, top = mid + 1. If its value is less than f, bot = mid + 1. Repeat step (IV) until bot > top, and then go to step (V). (V) If top is less than mid, set bot = top, top = mid. Otherwise, set top = bot, bot = mid. Repeat step (4) until \( \sqrt{x} = f \) is valid and go to step (5). In this step, the median (mid) is always integer in operation process. That can reduce the computation complexity, save the running time, and accelerate the operation process.
5. Encode x and r in the form of CEBM [10]. Remove the first N bits of S and repeat steps (3) and (4), until S is empty.

2.2. Encoding Example. An example is provided to make the scheme clear. Without loss of generality, set the original test set T = \{00011010, 11100100, 10011111, 10010100, 01010100, 11101101, 11010011, . . . \}. Cascade all the test vector, and then divide it into sequences of 48 bits. The data flow is 0001101011100100100111110100101011010110011 11101001 . . . Its first 48 bits can convert into a hexadecimal floating-point \( f = 1.E89F995D3 \). (I) Calculate \( f^2 = 2.D413CCCFE7551FCA6F09E9 \), bot = \( \lfloor f^2 \rfloor = 2 \), top = bot + 1 = 3, \( r = 2 \). (II) Calculate \( \sqrt{\text{top}} = \sqrt{5} = 1.BB67AE8584C \), and go to step (III) because its value is not equal to f. (III) Consider bot = \( \lfloor \text{bot} \ast \sqrt{\text{bot}} \rfloor = [2 \ast \sqrt{2}] = 2.D413CCCFE76 = 2 \), top = \( \lfloor \text{top} \ast \sqrt{\text{top}} \rfloor = [3 \ast \sqrt{3}] = 5.32370B9084E \), \( r = r + 1 = 3 \). (IV) Set mid = \( \lfloor (\text{bot} + \text{top})/2 \rfloor \), and calculate \( \sqrt{\text{mid}} \). If its value is equal to f, note x = mid, r, and go to step of encoding. If its value is greater than f, set top = mid - 1. If its value is less than f, set bot = mid + 1. Repeat step (IV) until bot > top (bot = 5, top = 4), and go to step (V). (V) If top is less than mid, set bot = top, top = mid. Otherwise, set bot = top, bot = mid. Then bot = 4, top = 5. Repeat steps (III), (IV), and (V) and we can get the results.
Begin

Generate the test set named $T$, cascade all the vector, remember as $S$

$S$ is not empty

Yes

Take the first $N$ bits, convert into a floating point named $f$

Set $\text{bot} = \lfloor f^2 \rfloor$, $\text{top} = \text{bot} + 1$, $r = 2$, $\text{flag} = 0$

Yes

$\sqrt{\text{bot}} = f$

No

$\sqrt{\text{top}} = f$

No

Flag = 1, $x = \text{bot}$

Yes

Flag = 1, $x = \text{top}$

No

Flag = 0

Yes

Flag = 0 and $\text{Bot} \leq \text{top}$

No

Set $\text{mid} = \lfloor (\text{bot} + \text{top})/2 \rfloor$

Yes

$\sqrt{\text{mid}} = f$

No

$\sqrt{\text{mid}} > f$

No

Flag = 1, $x = \text{mid}$

Yes

Top = $\text{mid} - 1$

Bot = $\text{mid} + 1$

No

Top < $\text{mid}$

Yes

Bot = $\text{top}$, $\text{top} = \text{mid}$

No

Top = $\text{bot}$, $\text{bot} = \text{mid}$

Set $\text{bot} = \lfloor \sqrt{\text{bot}} \rfloor$, $\text{top} = \lceil \sqrt{\text{top}} \rceil$, $r = r + 1$

Encode $x$ and $r$, remove the first $N$ bits of $S$

End

Figure 1: Flowchart of INS coding.
Table 1: Test data transformation rules.

| Test data | Hexadecimal | Test data | Hexadecimal | Test data | Hexadecimal | Test data | Hexadecimal |
|-----------|-------------|-----------|-------------|-----------|-------------|-----------|-------------|
| 0000      | 0           | 0100      | 4           | 1000      | 8           | 1100      | C           |
| 0001      | 1           | 0101      | 5           | 1001      | 9           | 1101      | D           |
| 0010      | 2           | 0110      | 6           | 1010      | A           | 1110      | E           |
| 0011      | 3           | 0111      | 7           | 1011      | B           | 1111      | F           |

Table 2: CEBM.

| Run-length | Group | Odd bits | Even bits | Codeword |
|------------|-------|----------|-----------|----------|
| 2          | A₁    | 0        | 1         | 01       |
| 3          |       | 1        | 1         | 11       |
| 4          |       | 00       | 01        | 00 01    |
| 5          | A₂    | 01       | 01        | 00 11    |
| 6          |       | 10       | 01        | 10 01    |
| 7          |       | 11       | 01        | 10 11    |
| 8          |       | 000      | 001       | 00 00 01 |
| 9          |       | 001      | 001       | 00 00 11 |
| 14         | A₃    |          |           |          |
| 15         |       | 111      | 001       | 10 10 01 |
|           |       |          |           |          |

Therefore, we only need to prove that $\sqrt{\text{bot}}$ is infinitely close to $\sqrt{\text{top}}$ when $r \to \infty$. That is to prove

$$\lim_{r \to \infty} \frac{\sqrt{\lfloor f^r \rfloor + 1}}{\sqrt{\lceil f^r \rceil}} = 1$$

$$\lim_{r \to \infty} \frac{\sqrt{\lfloor f^r \rfloor + 1}}{\sqrt{\lceil f^r \rceil}} = \lim_{r \to \infty} e^{\ln((\sqrt{\lfloor f^r \rfloor + 1})/\sqrt{\lceil f^r \rceil})}$$

$$= \lim_{r \to \infty} e^{\ln((\sqrt{\lfloor f^r \rfloor + 1})/\sqrt{\lceil f^r \rceil})} = \lim_{r \to \infty} (1/r) \ln((\sqrt{\lfloor f^r \rfloor + 1})/\sqrt{\lceil f^r \rceil})$$

$$= \lim_{r \to \infty} \frac{\ln(1 + 1/\sqrt{\lfloor f^r \rfloor})}{r} \to 0$$

$$\lim_{r \to \infty} \frac{\sqrt{\lfloor f^r \rfloor + 1}}{\sqrt{\lceil f^r \rceil}} = \lim_{r \to \infty} e^{\ln((\sqrt{\lfloor f^r \rfloor + 1})/\sqrt{\lceil f^r \rceil})} = 1.$$
This special \( k + 1 \) bits counter is unique. Set its lowest bit as 1; move this bit to high with other data when the data needed to be decoded is moved to the counter. The function can be realized by a combination of some simple circuit, and the hardware overhead will not increase significantly. In the \( k + 1 \) bits counter, the value of \( k \) is decided by the maximum of the radicand and the boot number (named as \( L_{\text{max}} \)) in compression result, \( k = \lceil \log_2(L_{\text{max}} + 1) \rceil - 1 \).

The root operation can be realized by the CPU module on SoC chip as long as the floating-point processing unit \( \times 87 \) FPU integrated in CPU. \( \times 87 \) FPU has its own instruction system, including the commonly used instruction types: floating-point move instructions, floating-point arithmetic operation instructions, floating-point transcendental function instructions, floating-point comparison instructions, and FPU control instructions [11]. Floating-point transcendental function instructions can realize exponent operation (F2XM1 instruction) and logarithmic operation (FYL2X instruction). \( \sqrt{x} \) can be converted into \( 2 \left( \log_2x \right)/r \), which can be calculated by exponent operation instruction and logarithmic operation instruction.

Decompressor works as follows. (1) First, the FSM makes an enable signal named \( en \) into high level, and the encoded data named \( \text{bit-in} \) is split into two parts: odd bits and even bits by the position of data. That is implemented by the T flip-flop. Odd bits are directly shifted into the \( k + 1 \) bits counter, and even bits are shifted into FSM. (2) Then, FSM repeats to read the encoded data until the value of even bit equals 1. Meanwhile, the odd bit is shifted into the \( k + 1 \) bits counter. (3) The data (named \( x \)) of the \( k + 1 \) bits counter is shifted into CPU after all odd bits of data are received in the special \( k + 1 \) bits counter. Repeat step (2); the data of the \( k + 1 \) bits counter (named \( r \)) is shifted into CPU. (4) \( \sqrt{x} \) is calculated by floating-point processing unit \( \times 87 \) FPU in CPU, and the first \( N \) bits of its binary form are outputted.

### 5. Experimental Results

In this section, the effectiveness of the INS coding scheme is verified by using experimental results.

INS coding is applied to the MinTest test sets of the largest ISCAS 89 benchmark circuits. The experimental results are shown in Table 3. The first column shows the circuit name, the second column shows the total number of the data in the original test sets, the third column shows the total number of the compressed data, and the fourth column shows the compression ratio.

In order to verify the validity of this scheme, compare with the similar algorithm, as shown in Table 4. Among them, the first column shows the circuit name, the second to sixth columns, respectively, show the compression effect of FDR code [6], INDIC code [9], AARLC code [8], FAVLC code [12], and VRL code [13], and the seventh column shows compression effect of the scheme presented. Data from Table 3 shows this scheme besides lower compression ratio in the fifth circuit, and the rest of the circuit has higher compression ratio. And this scheme has a good compression effect on the whole. The average compression ratio reaches 65.79%, which is 20.46%, 9.42%, 7.36%, 5.36%, and 1.85% higher than those of FDR, RLR, AARLC, FAVLC, and VRL.

In order to further demonstrate the effectiveness, the results of proposed scheme are compared with other schemes under the same circumstances by the hard fault set of some ISCAS 89 benchmark circuits. The results as shown in Table 5. As can be seen from Table 4, the overall effect of proposed scheme is better. The average compression ratio of the proposed scheme is 3.87%, 3.82%, and 3.31% higher than those of FDR, AR [14], and ARL [15]. These data show the effectiveness of INS Code.

The experimental results indicate the following. (1) Regardless of the fact that the determined bit of the test data is 0 or 1, it has a little effect on compression ratio in the process of finding the irrational number. (2) Do not-care bit can accelerate the search speed of irrational number, reduce the value of irrational number used to store the test data, and improve the compression ratio.

The influence of the do not-care bit probability on compression is explored. The length of the test data fragment is set to be \( K \), and the probability of do not-care bit is set to be \( \rho \). Their relationship can be expressed in the following formula:

\[
\sqrt{x} - f_i < 10^{-(K/4)+1}, \quad i = 1, 2, \ldots, 2^K \rho, \tag{3}
\]

where, \( x \), \( r \), and \( K \) are integers and \( f_i \) is a floating-point number.

The compression gain can be calculated by the following formula:

\[
\beta = \frac{K}{(1 + \log_2(x + 1) + \log_2(r + 1) + \log_2(K + 1))}. \tag{4}
\]
Table 5: Comparison of other algorithms (the hard fault set).

| Circuit | Size of TD bit | FDR | AR | ARL | Scheme presented |
|---------|---------------|-----|----|-----|------------------|
| S5378   | 5992          | 1110| 1160| 1091| 710              |
| S9234   | 73112         | 22038| 21222| 20429| 11982          |
| S13207  | 220500        | 14080| 15334| 15061| 7500           |
| S15850  | 163748        | 14370| 13286| 12861| 12861          |
| S38417  | 2201472       | 103760| 94682| 90397| 103779         |
| S38584  | 456768        | 13840| 15696| 15083| 12551          |

By analyzing the experimental data, the relationship between the compression gain $\beta$ and the probability of not-care bit $\rho$ can be concluded as shown in Figure 3.

From Figure 3, as can be seen, the proposed compression scheme can obtain better compression effect in a higher probability of do not-care bit.

6. Conclusion

INS coding is presented, which uses the floating-point number unfolded by irrational number to store the test set. It is creative. Using the successive approximation method can accelerate the convergence speed in the process of searching the irrational number. The experimental results show that the compression effect of the scheme is better. It provides a new choice to solve the problem of test data compression.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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