**Abstract**

High-k material charge trapping nano-layers in flash memory applications have faster program/erase speeds and better data retention because of larger conduction band offsets and higher dielectric constants. In addition, Ti-doped high-k materials can improve memory device performance, such as leakage current reduction, k-value enhancement, and breakdown voltage increase. In this study, the structural and electrical properties of different annealing temperatures on the Nb$_2$O$_5$ and Ti-doped Nb$_2$O$_5$(TiNb$_2$O$_7$) materials used as charge-trapping nano-layers in metal-oxide-high k-oxide-semiconductor (MOHOS)-type memory were investigated using X-ray diffraction (XRD) and atomic force microscopy (AFM). Analysis of the C-V hysteresis curve shows that the flat-band shift ($\Delta V_{FB}$) window of the TiNb$_2$O$_7$ charge-trapping nano-layer in a memory device can reach as high as 6.06 V. The larger memory window of the TiNb$_2$O$_7$ nano-layer is because of a better electrical and structural performance, compared to the Nb$_2$O$_5$ nano-layer.

**Keywords:** Ti-doped Nb$_2$O$_5$; charge trapping nano-layer; MOHOS memory

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**1. Introduction**

Conventional polysilicon floating gate issues have been explored in recent years because of problems related to the downscaling of memory devices [1–5]. For this study, high-k materials were chosen as replacements for conventional polysilicon floating gate memory to form metal-oxide-high k-oxide-semiconductor (MOHOS)-type memories [6,7]. Compared with the traditional SONOS-type memory, MOHOS-type has larger memory windows [8–11]. Otherwise, charge-trapping layers using high-k materials have faster program/erase speeds and better data retention because of larger conduction band offsets and higher dielectric constants [12–16]. Among various rare earth oxides, High-k Nb$_2$O$_5$ shows a high dielectric constant (k = 40), wide band gap ($E_G = 3.2$ eV), and a large conduction band offset [17]. To further enhance the memory performance of the device, addition of Ti atoms into trapping layer has been conducted, and some studies [18–23] reported that Ti-doped high-k materials as charge-trapping layers can improve memory device performance such as leakage current reduction, k-value enhancement, program/erase speeds improvement, and charge loss reduction. On the other hand, the performances of other different types of memory structures were presented by previous studies; Ostraat et al. reported that aerosol nanocrystal devices with 0.2 mm...
channel lengths exhibit large threshold voltage shifts (>3 V), excellent endurance (>10⁵ program/erase cycles), and long-term non-volatility (>10⁶ s) for low-cost non-volatile memory applications [24,25]. Ruffinno et al. studied the electrical conduction of Au nanoclusters embedded in SiO₂ films. The local I-Vtip characteristics exhibited an asymmetric behavior with a clear threshold voltage Vth for the electrical conduction, decreasing with the average Au grain size [26].

In our study, this work investigated the differences between metal-oxide-high k-oxide-semiconductor (MOHOS)-type flash memory devices using Nb₂O₅ or TiNb₂O₇ as charge-trapping nano-layers. Our research indicates that the Ti-doped Nb₂O₅ (TiNb₂O₇) charge trapping nano-layer has a larger memory window because of the better electrical and structural properties. Therefore, the Ti-doped Nb₂O₅-based flash memory might be promising for future industrial memory applications. Structural analyses included X-ray diffraction (XRD) and atomic force microscopy (AFM), while electrical analyses included Capacitance-Voltage (C-V) hysteresis, program/erase speed, and data retention measurements.

2. Materials and Methods

The schematic diagrams of Al/SiO₂/Nb₂O₅/SiO₂/Si and Al/SiO₂/TiNb₂O₇/SiO₂/Si (MOHOS)-type flash memory devices are shown in Figure 1a,b, respectively. First, single-crystal 4-inch n-type silicon (100) wafers were cleaned using a standard RCA process. Then, a 3-nm SiO₂ film was thermally grown as a tunneling oxide layer using a dry oxidation furnace system at 850 °C. Then, (a) a 12-nm Nb₂O₅ trapping nano-layer was deposited by RF sputtering with a pure niobium target (99.99% pure) in argon (Ar) and oxygen (O₂) gas ambient, while (b) an approximately 12-nm Ti-doped Nb₂O₅ (TiNb₂O₇) trapping nano-layer was deposited by RF co-sputtering of a niobium and titanium target as comparison. After that, the above two kinds of samples underwent rapid thermal annealing treatment in O₂ ambient for 30 second from 700, 800, 900 and 950 °C to form Nb₂O₅ and TiNb₂O₇ charge trapping nano-layers, respectively. Subsequently, a 20-nm SiO₂ film was deposited as a blocking oxide layer by plasma-enhanced chemical vapor deposition at a substrate temperature of 300 °C. After deposition of the blocking oxide layer, a 300-nm Al film was deposited by thermal evaporator and a gate pattern was defined through lithography and wet etching. Finally, a 300-nm Al film was deposited on the backside. C-V hysteresis and data retention were measured with an HP-4284 LCR meter, P/E speed was measured by an HP8110 pulse generator, and leakage current was measured using an HP4156C semiconductor parameter analyzer. Structural analyses of the Nb₂O₅ and TiNb₂O₇ trapping layers were performed by XRD and AFM to examine the connections between electrical characteristics and structural properties. The XRD spectrum was performed by a grazing incidence of CuKα (k = 1.542 Å) radiation. The system used a grazing incidence angle (θ = 0.5) in an XRD spectrum in the diffraction angle range (2θ) from 20° to 60°. The surface morphologies of the Nb₂O₅ and TiNb₂O₇ charge-trapping nano-layers were monitored using atomic force microscopy (AFM) by a Veeco model D5000 operated in tapping mode using an Applied Nano silicon tip with a 50 N/m spring constant. The scan area was 3 um x 3 um with a set engagement ratio of 80%.

Figure 1. The schematic diagram of (a) Al/SiO₂/Nb₂O₅/SiO₂/Si MOHOS (b) Al/SiO₂/TiNb₂O₇/SiO₂/Si (MOHOS)-type flash memory devices.
3. Results and Discussion

To examine device performance under different annealing conditions, we compared different C-V hysteresis curves under sweeping voltages, as shown in Figure 2a,b and Figure S1 of the Supplementary Materials. The forward sweep began from inversion region to accumulation and the reverse sweep moved in another direction with the electrons charging into and discharging from the trapping film. The C-V curves indicate that annealing could enlarge the memory window of the device. The Ti-doped NbO<sub>5</sub> (TiNb<sub>2</sub>O<sub>7</sub>) sample which underwent RTA treatment at 900 °C had a larger memory window (6.06 V) and better storage capability compared with that of the NbO<sub>5</sub> sample annealed at 900 °C (4.64 V). Our research shows that the TiNb<sub>2</sub>O<sub>7</sub> nano-layer possesses better electrical characteristics than the NbO<sub>5</sub> nano-layer, likely because of the enhanced dielectric constants, increased breakdown voltage, and reduced leakage current provided by the addition of Ti. According to the result, it also can be seen that the memory window increased with the annealing temperature from 700 to 900 °C, and the sample annealed at 900 °C had the largest memory window (NbO<sub>5</sub>: 700 °C/0.99 V, 800 °C/2.73 V, 900 °C/4.64 V; TiNb<sub>2</sub>O<sub>7</sub>: 700 °C/1.3 V, 800 °C/4.37 V, 900 °C/6.06 V). As the material quality of the charge-trapping layer is a decisive factor in trapped electron storage capability, the results indicate that the TiNb<sub>2</sub>O<sub>7</sub> charge-trapping nano-layer annealing at 900 °C can enhance the formation of a well-crystallized structure.

![C-V Curves](image)

**Figure 2.** (a) High frequency C-V curves of Al/SiO<sub>2</sub>/NbO<sub>5</sub>/SiO<sub>2</sub>/Si structure after annealing in different temperatures; (b) high frequency C-V curves of Al/SiO<sub>2</sub>/TiNb<sub>2</sub>O<sub>7</sub>/SiO<sub>2</sub>/Si structure after annealing in different temperatures.

Figure 3a,b shows the programming and erasing speed of the NbO<sub>5</sub> and TiNb<sub>2</sub>O<sub>7</sub> charge-trapping nano-layers for 800 and 900 °C annealing under V<sub>p</sub> = 13 V programming voltage and −16 V erasing voltage. By the way, the programming and erasing speed of the above samples with applying various bias were also presented in Figures S2 and S3 of the Supplementary Materials. The V<sub>b</sub> shift is defined as the change in the flat-band voltage between the virginal and erased states. During supply forward bias, the electron will inject from the Si channel to high-k trapping layers and storage in trapping layers and it will change in flat-band voltage. On the other hand, if we supply reverse bias, the electron will de-trapped from high-k trapping layers to Si channel. In these figures, the programmed state was measured at V<sub>p</sub> = 13 V with various time from 1 us to 10 s, and the erase state was measured at V<sub>e</sub> = −16 V with various time from 1 ms to 10 s. In our result, it can be found that the TiNb<sub>2</sub>O<sub>7</sub> charge-trapping nano-layer annealed at 900 °C showed a faster program/erase speed than other samples when operating at same programming/erasing voltage. It can be attributed the TiNb<sub>2</sub>O<sub>7</sub> charge-trapping nano-layer can enhance higher dielectric constant, which can increase the effective electric field across the tunneling oxide and permit electron easily through FN-tunneling from Si channel to the charge-trapping layers.
The programmed state was the same $V_g = 9$ V for 100 ms. Charge loss rate was calculated as:

$$\text{Charge loss rate(\%)} = \left[ \frac{V_{(t)} - V_0}{V_1 - V_0} \right] \times 100\%$$

where $V_{(t)}$ is the $V_{fb}$ of various time, $V_1$ is the first $V_{fb}$ after being programmed, and $V_0$ is the fresh one. In our result, the sample annealing at 900 °C has better retention characteristics than that at 800 °C, it’s because of formation structures in high temperature. On the other hand, the MOHOS-type memory with TiNb$_2$O$_7$ charge-trapping nano-layer after annealed at 900 °C shows a smaller charge loss rate than other samples. The sample annealed at 900 °C shows a smaller charge loss of 9.3% at room temperature (RT) and 17.8% at 85 °C after $1 \times 10^4$ s, this is possibly because of the formation of well-crystallized TiNb$_2$O$_7$ trapping nano-layer. In Figure 4c, shows the leakage current curves of Nb$_2$O$_5$ and TiNb$_2$O$_7$ trapping nano-layer, it can be seen that the TiNb$_2$O$_7$ sample shows a lower leakage current than Nb$_2$O$_5$ sample, this is because the TiNb$_2$O$_7$ can reduce the leakage current and enhance the breakdown of the electric field to improve effectively the above charge loss.
Figure 4. Data retention of the (a) Nb$_2$O$_5$ and (b) TiNb$_2$O$_7$ charge-trapping nano-layers measured at RT and 85 °C; (c) the leakage current density versus gate voltage of the Nb$_2$O$_5$ and TiNb$_2$O$_7$ trapping nano-layers for the top gate applied a positive bias.

In order to identify the composition of Nb$_2$O$_5$ and TiNb$_2$O$_7$ structures at different temperatures, the X-ray diffraction has been used for analysis of Nb$_2$O$_5$ and TiNb$_2$O$_7$ structures. The XRD analysis in the range of diffraction angle 2θ from 20° to 60° was obtained by grazing incidence angle (θ = 0.5°) measurements. Figure 5a,b show the XRD analysis of MOHOS-type memory with Nb$_2$O$_5$ and TiNb$_2$O$_7$ trapping nano-layer before and after annealing at different temperatures. For the Nb$_2$O$_5$ nano-layer, it can be seen that the temperature will induce crystallization in high-k trapping layer. According to the XRD analysis, the Nb$_2$O$_5$ trapping nano-layer has some Nb$_2$O$_5$ diffraction peaks in (0 0 5), (−2 1 5),
(1 1 2), (6 2 1), and (3 8 1) at 29.6°, 33.1°, 47.8°, 54.6°, and 56.4°. The peak intensity became stronger at higher annealing temperatures, and the Nb$_2$O$_5$ nano-layer annealing at 900 °C exhibited stronger peak intensity in Nb$_2$O$_5$ (−215), it can be seen that the sample annealing at 900 °C formed a better Nb$_2$O$_5$ nano-layer structure. For the TiNb$_2$O$_7$ trapping nano-layer, it has some TiNb$_2$O$_7$ diffraction peaks in TiNb$_2$O$_7$ (−3 1 2), TiNb$_2$O$_7$ (0 2 0), TiNbO$_4$ (2 2 0), and TiNb$_2$O$_7$ (−11 1 2) at 28.6°, 47.8°, 54.7°, and 56.4°. The similar trend that the TiNb$_2$O$_7$ peak intensity also became stronger at higher annealing temperature and the TiNb$_2$O$_7$ nano-layer annealing at 900 °C exhibited the strongest peak intensity in TiNb$_2$O$_7$ (0 2 0) than the other temperatures. This means the crystallization enhancement can be found when the sample annealing is at high temperatures. However, when the annealing temperature increased to 950 °C, the TiNb$_2$O$_7$ peaks declined. This may be because of the formation of a thicker Nb-silicate layer between TiNb$_2$O$_7$ charge-trapping nano-layer and oxide interface layer to degrade the crystallinity of TiNb$_2$O$_7$ layer [27].

![XRD spectra of Nb$_2$O$_5$ and TiNb$_2$O$_7$ films.](image)

**Figure 5.** XRD spectra of the (a) Nb$_2$O$_5$ and (b) TiNb$_2$O$_7$ films.

To visualize the film surface texture in a more practical manner, AFM was used to examine surface roughness of the Nb$_2$O$_5$ and TiNb$_2$O$_7$ nano-layers for the as-deposited and RTA-annealed samples at 900 °C, as shown in Figure 6a–d. It can be seen that the surface roughness of Nb$_2$O$_5$ and TiNb$_2$O$_7$ nano-layers of the as-deposited and 900 °C annealed samples exhibit 0.41 nm, 0.51 nm, 2.68 nm, and 3.51 nm, respectively. Since annealing could effectively increase the surface roughness of the film and reinforce the crystallization of TiNb$_2$O$_7$ nano-layers, larger roughness values and larger grains could be observed with increasing annealing temperatures. In line with the above results, the roughest surface and largest grains occurred for the TiNb$_2$O$_7$ nano-layers after RTA treatment at 900 °C. The increase in surface roughness is attributed to the niobium oxide intermixing with the titanium film, resulting in the enhancement of grain growth when annealed at 900 °C. However, the TiNb$_2$O$_7$ nano-layer annealed at 950 °C exhibited a decrease of roughness as compared to 900 °C, indicating that the oxygen leaving the TiNb$_2$O$_7$ layer and moving to the TiNb$_2$O$_7$/oxide interface...
resulted in a poorly crystallized TiNb2O7 structure and a low-k interfacial Nb silicate layer at the TiNb2O7/oxide interface [28]. Figure 6e shows details of the surface roughness of Nb2O5 and TiNb2O7 nano-layers, with increasing annealing temperature. Overly, all the samples with Ti-doping show higher surface roughness as compared to Nb2O5. Larger grains are formed owing to the higher oxygen affinity of Ti increases in the reaction of Nb2O5 and thus enhances the formation of grain growth to cause rougher surface [29,30]. Moreover, the Ti-doped Nb2O5 (TiNb2O7) charge-trapping layer at 900 °C exhibited a larger grain size with more uniform distribution compared with the Nb2O5 layer at 900 °C. The increase in surface roughness is attributed to the titanium-incorporated niobium oxide film resulting in the enhancement of grain growth to obtain a larger grain size [31–34].

Figure 6. AFM images of the (a) as-deposited and (b) 900 °C annealed Nb2O5 films; AFM images of the (c) as-deposited and (d) 900 °C annealed TiNb2O7 films; (e) surface roughness of Nb2O5 and TiNb2O7 films as a function of annealing temperature.

4. Conclusions

Our research evaluated Nb2O5 and Ti-doped Nb2O5 charge trapping layers for non-volatile memory applications. Compared with the Nb2O5 trapping layer, the devices with a TiNb2O7 trapping layer exhibited a larger memory window and faster program/erase speeds. The results indicate that the TiNb2O7 charge-trapping nano-layer annealing at 900 °C can reinforce the bonding strength to enhance the formation of a well-crystallized structure for performance improvement.

In addition, the TiNb2O7 trapping layer shows a smaller charge loss of about 9.3% at room temperature and 17.8% at 85 °C after 10^4 s, because the TiNb2O7 layer can reduce the leakage current and enhance the breakdown electric field to effectively improve the charge loss. Moreover, structural
analyses of the Nb_2O_5 and TiNb_2O_7 trapping layers were performed by XRD and AFM to investigate and confirm the connections between electrical characteristics and structural properties. Therefore, the MOHOS-type memory device with the Ti-doped Nb_2O_5 charge-trapping nano-layer shows itself to be a very promising candidate for future non-volatile flash memory.

**Supplementary Materials:** The following are available online at http://www.mdpi.com/2079-4991/8/10/799/s1, Figure S1: (a) Nb_2O_5 and (b) TiNb_2O_7 charge trapping nano-layers for different temperature after applying various bias; Figure S2: Programming speed of Nb_2O_5 trapping layer for (a) 800 °C, and (b) 900 °C after applying various bias, and programming speed of TiNb_2O_7 trapping layer for (c) 800 °C, and (d) 900 °C after applying various bias; Figure S3: Erasing speed of Nb_2O_5 trapping layer for (a) 800 °C, and (b) 900 °C after applying various bias, and erasing speed of TiNb_2O_7 trapping layer for (c) 800 °C, and (d) 900 °C after applying various bias.

**Author Contributions:** C.H.K., C.H.W. and J.C.W. conceived and designed the experiments; C.J.L. performed the experiments; C.F.L. and C.J.L. analyzed the data; and C.H.K. wrote the paper.

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**Conflicts of Interest:** The authors declare no conflicts of interest.

**References**

1. Kahng, D.; Sze, S.M. A floating gate and its application to memory devices. *IEEE Trans. Electron. Dev.* **1967**, *14*, 629. [CrossRef]
2. White, M.H.; Adams, D.A.; Bu, J. On the go with SONOS. *IEEE Circuits Devices Mag.* **2000**, *16*, 22–31. [CrossRef]
3. Kim, J.H.; Choi, J.B. Long-Term Electron Leakage Mechanisms through ONO Interpoly Dielectric in Stacked-Gate EEPROM Cells. *IEEE Trans. Electron. Dev.* **2004**, *51*, 2048–2053. [CrossRef]
4. Bu, J.; White, M.H. Retention reliability enhanced SONOS NVSM with scaled programming voltage. *IEEE Aerosp. Conf.* **2002**, *5*, 2383–2390.
5. Swift, C.T.; Chindalore, G.L.; Harber, K.; Harp, T.S.; Hoefer, A.; Hong, C.M.; Ingersoll, P.A.; Li, C.B.; Prinz, E.J.; Yater, J.A. An embedded 90 nm SONOS nonvolatile memory utilizing hot electron programming and uniform tunnel erase. In *Proceedings of the Electron Devices Meeting*, San Francisco, CA, USA, 8–11 December 2002; pp. 927–930.
6. Wang, X.; Kwong, D.-L. A novel high-κ SONOS memory using TaN/Al_2O_3/Ta_2O_5/HfO_2/Si structure for fast speed and long retention operation. *IEEE Trans. Electron. Dev.* **2006**, *53*, 78–82. [CrossRef]
7. Wang, X.; Liu, J.; Bai, W.; Kwong, D.-L. A novel MONOS-type nonvolatile memory using high-κ dielectrics for improved data retention and programming speed. *IEEE Trans. Electron. Dev.* **2004**, *51*, 597–602. [CrossRef]
8. Hsu, T.-H.; You, H.-C.; Ko, F.-H.; Lei, T.-F. PolySi-SiO_2-ZrO_2-SiO_2/Si flash memory incorporating a sol-gel-derived ZrO_2 charge trapping layer. *J. Electrochem. Soc.* **2006**, *153*, G934–G937. [CrossRef]
9. Lee, C.-H.; Hur, S.-H.; Shin, Y.-C.; Choi, J.-H.; Park, D.-G.; Kim, K. Charge-trapping device structure of SiO_2/SiN/high-k dielectric Al_2O_3 for high-density flash memory. *Appl. Phys. Lett.* **2005**, *86*, 152908. [CrossRef]
10. Yang, S.-M.; Chien, C.-H.; Huang, J.-J.; Lei, T.-F.; Tsai, M.-J.; Lee, L.-S. Cerium oxide nanocrystals for nonvolatile memory applications. *Appl. Phys. Lett.* **2007**, *91*, 262104. [CrossRef]
11. You, H.-C.; Hsu, T.-H.; Ko, F.-H.; Huang, J.-W.; Yang, W.-L.; Lei, T.-F. SONOS-type flash memory using an HfO_2 as a charge trapping layer deposited by the sol-gel spin-coating method. *IEEE Electron. Device Lett.* **2006**, *27*, 653–655.
12. Tan, Y.N.; Chim, W.K.; Cho, B.J.; Choi, W.K. Over-Erase Phenomenon in SONOS-Type Flash Memory and its Minimization Using a Hafnium Oxide Charge Storage Layer. *IEEE Trans. Electron. Dev.* **2004**, *51*, 1143–1147. [CrossRef]
13. Specht, M.; Reisinger, H.; Stadele, M.; Hofmann, F.; Geschwandtner, A.; Landgraf, E.; Luyken, R.J.; Schulz, T.; Hartwich, J.; Dreesskornfeld, L.; et al. Retention time of novel charge trapping memories using Al_2O_3 dielectrics. In *Proceedings of the 33rd European Solid-State Device Research Conference*, Estoril, Portugal, 16–18 September 2003; pp. 155–158.
14. Tan, Y.N.; Chim, W.K.; Choi, W.K.; Joo, M.S.; Ng, T.H.; Cho, B.J. High-k HfAlO charge trapping layer in SONOS-type nonvolatil memory device for high speed operation. In Proceedings of the IEEE International IEDM Technical Digest, San Francisco, CA, USA, 13–15 December 2004.

15. Sugizaki, T.; Kohayashi, M.; Ishidao, M.; Minakata, H.; Yamaguchi, M.; Tamura, Y.; Sugiyama, Y.; Nakanishi, T.; Tanaka, H. Novel multi-bit SONOS type flash memory using a high-k charge trapping layer. In Proceedings of the 2003 Symposium on VLSI Technology, Kyoto, Japan, 12–14 June 2003; pp. 27–28.

16. Pan, T.M.; Yeh, W.W. A high-k Y2O3 charge trapping layer for nonvolatile memory application. *Appl. Phys. Lett.* **2008**, *92*, 173506. [CrossRef]

17. Soares, M.R.N.; Leite, S.; Nico, C.; Peres, M.; Fernandes, A.J.S.; Graca, M.P.F.; Monteiro, R.; Monteiro, T.; Costa, F.M. Effect of processing method on physical properties of Nb2O5. *J. Eur. Ceram. Soc.* **2011**, *31*, 501–506. [CrossRef]

18. Van Dover, R.B. Amorphous lanthanide-doped TiOx dielectric films. *Appl. Phys. Lett.* **1999**, *74*, 3041. [CrossRef]

19. Kao, C.H.; Chen, C.C.; Huang, C.Y.; Lin, C.J.; Ou, J.C. Investigation of Ti-doped Gd2O3 charge trapping layer with HfO2 blocking oxide for memory application. *Thin Solid Films* **2012**, *520*, 3857–3861. [CrossRef]

20. Chen, F.H.; Pan, T.M.; Chiu, F.C. Metal–Oxide–High-k-Oxide–Silicon Memory Device Using a Ti-Doped Dy2O3 Charge-Trapping Layer and Al2O3 Blocking Layer. *IEEE Trans. Electron. Devices* **2011**, *58*, 3847–3851. [CrossRef]

21. Schroeder, T.; Lupina, G.; Dabrowski, J.; Mane, A.; Wengert, C.; Lippert, G.; Müssig, H.-J. Titanium-added praseodymium silicate high-k layers on Si (001). *Appl. Phys. Lett.* **2005**, *87*, 022902. [CrossRef]

22. Kao, C.H.; Chen, H.; Chen, S.Z.; Hung, S.-H.; Chen, C.Y.; He, Y.-Y.; Lin, S.-R.; Hsieh, K.-M.; Lin, M.-H. Effects of annealing on CeO2-based flash memories. *Vacuum* **2015**, *118*, 69–73. [CrossRef]

23. Kao, C.H.; Chen, H.; Chen, C.C.; Chen, C.P.; Wang, J.J.; Chen, C.Y.; Chen, Y.T.; Lin, J.H.; Chu, Y.C. Comparison of electrical and physical characteristics between Gd2O3 and Ti-doped GdTixOy trapping layers. *Microelectron. Eng.* **2015**, *138*, 2122. [CrossRef]

24. Ostraat, M.L.; De Blauwe, J.W.; Green, M.L.; Bell, L.D.; Brongersma, M.L.; Casperson, J.; Flagan, R.C.; Atwater, H.A. Synthesis and characterization of aerosol silicon nanocrystal nonvolatile floating-gate memory devices. *Appl. Phys. Lett.* **2001**, *79*, 433. [CrossRef]

25. De Blauwe, J. Nanocrystal nonvolatile memory devices. *IEEE Trans. Nanotechnol.* **2002**, *99*, 72. [CrossRef]

26. Ruffino, F.; Grimaldi, M.G.; Giannazzo, F.; Roccaforte, F.; Raineri, V. Atomic force microscopy study of the growth mechanisms of nanostructured gold films on SiO2. *Adv. Colloid Interface Sci.* **2004**, *107*, 104321. [CrossRef]

27. Pan, T.-M.; Yu, T.-Y. Silicone-oxide-nitride-oxide-silicon-type flash memory with high-k NdTiO3 charge trapping layer. *Appl. Phys. Lett.* **2008**, *92*, 112906. [CrossRef]

28. Van Hal, R.E.G.; Eijkel, J.C.T.; Bergveld, P. A general model to describe the electrostatic potential at electrolyte oxide interfaces. *Adv. Colloid Interface Sci.* **1996**, *69*, 31–62. [CrossRef]

29. Pan, T.-M.; Yu, T.-Y.; Wang, C. High-k Nd2O3 and NdTiO3 Charge Trapping Layers for Nonvolatile Memory Metal-SiO2-High-k-SiO2-Silicon Devices. *J. Electrochem. Soc.* **2008**, *155*, G218. [CrossRef]

30. Ruffino, F.; Grimaldi, M.G. Atomic force microscopy study of the growth mechanisms of nanostructured sputtered Au film on Si(111): Evolution with film thickness and annealing time. *J. Appl. Phys.* **2010**, *107*, 104321. [CrossRef]

31. Palasnatzas, G.; Krim, J. Scanning Tunneling Microscopy Study of the Thick Film Limit of Kinetic Roughening. *Phys. Rev. Lett.* **1994**, *73*, 3564. [CrossRef] [PubMed]

32. Ruffino, F.; Grimaldi, M.G.; Giannazzo, F.; Roccaforte, F.; Raineri, V. Atomic Force Microscopy Study of the Kinetic Roughening in Nanostructured Gold Films on SiO2. *Nanoscale Res. Lett.* **2009**, *4*, 262. [CrossRef] [PubMed]

33. Chevrier, J.; Le Thanh, V.; Buys, R.; Derrien, J. A RHEED Study of Epitaxial Growth of Iron on a Silicon Surface: Experimental Evidence for Kinetic Roughening. *Europhys. Lett.* **1991**, *16*, 737. [CrossRef]