A Design of Telemetry System for Small Animals

Abdelali El Boutahiri, Karim El Khadiri, Ahmed Tahiri, and Hassan Qidaa

Abstract—The external unit of small telemetry system for animals uses inductive link to transmit both data and power to a small implant. In this work, firstly, we have presented a wideband frequency shift keying (FSK) transmitter, which is a class E power amplifier (PA) switches between two load networks that make the PA tuned correctly at tow input clock frequencies. Carrier frequencies used for data modulation are 5MHz/10MHz, the data rate of the proposed link is 2.5 Mbps. On the other hand, the analog circuits of the internal unit are designed in this paper. Internal unit has a demodulator circuit to derive directly a frequency clock from the FSK carrier and to sample the binary data stream. It also has a low power generator circuit to generate the supply voltage to the other blocks. The low power generator is composed of a high efficiency, low power rectifier and a low power voltage regulator. To minimize the quiescent current of the regulator, we propose a control section which is a two-stage error amplifier to control the gate voltage of the PMOS transistors used in the differential pair of the voltage regulator and thus stabilize the direct current (DC) level at its output signal (V\text{reg}). The output voltage of the proposed generator circuit is regulated at 1V, the quiescent current simulated is about 9.9µA and the line regulation performance is only 8mV/V. All circuits proposed in this paper were designed and simulated using Cadence in 180 nm CMOS technology.

Index Terms— Telemetry system, class E PAs, wideband FSK, low power, inductive link, modulator, demodulator.

I. INTRODUCTION

A WIRELESS telemetry system is designed that is suited for measuring and collecting of data/information from a small animal of laboratory [1]. The system captures, and transmits this information wirelessly to an end base station (computer or embedded system). The implant unit is implanted totally in the animal’s body. It is a small application specific system, created to capture data of a biosensor (retinal application [5], cardiac [6] and neurological [7] application), it communicates to radio frequency (RF) receiver for further processing.

The implanted device includes three main sub–blocks:

- Analog front end, numeric section (microcontroller & interface circuit) and RF transceiver. Analog front end contains a demodulator to demodulate the data transmitted from the external part and to generate a clock recovery, and low power voltage generator to provide the power supply. Implant device transmits data collected wirelessly, through an RF antenna with a specific RF protocol. Different wireless protocols exist to transmit the binary data stream are HUF 860MHz -960MHz, non-standard 2.4GHz, WIFI, Bluetooth, and other RF proprietary RF frequencies.

- The innovation of this work is the design of 5MHz/10MHz FSK link using a class E PA to increase both the power transfer efficiency and the data rate to carrier frequency. Moreover, the design of voltage generator with low power consumption is proposed.

- The design of telemetry systems for small animals is an active field, for this reason, researchers work to improve their performances such as the size (the size of the implant should be minimized because the small body of the animal), the energy consumption, etc, the role of this work is to improve some performances. The first goal is to increase the power transfer efficiency and to offer a high bandwidth with the carrier frequency, which is limited to a few ten of Mega Hertz (frequencies used in the inductive link are effectively low). Although, coupling inductive insensitivity and power/data transmission have been discussed, few works focus on the aspect of the bandwidth of the inductive link [8-9]. ON-OFF keying (OOK) and Amplitude Shift Keying (ASK) modulations were used in the above applications because of their simple modulation/demodulation and low power consumption. On the other hand, the main drawback of OOK and ASK links are the low data transmission bandwidth [10]. As solution, wideband frequency shift keying was used to provide a large bandwidth. In wideband FSK protocol, binary logic “0” is transmitted by two cycles of the carrier wave f1, and binary logic “1” is transmitted by a single cycle of the carrier wave f2. With f1 twice f2 (f1=2f2), the design of data and clock recovery in the implant becomes simpler [11]. Moreover, we can achieve a larger data rate carrier frequency ratio.

- Class E PAs are generally used to drive inductive links. With the increasing of the quality factor (Q) of the amplifier, the power transfer efficiency of the inductive link will increase directly. However, as Q increases, the amplifier becomes very sensitive to phase and frequency shifts of the input clock and,
as a result, its bandwidth is reduced. In addition, varying the frequency of the input clock detunes the class E PA. Therefore, the implementation of ASK and OOK modulations can be easily designed with an inductive link driven by a class E power amplifier, while FSK modulation on a class E PA is a challenge. For this reason, in this work, an inductive link for small telemetry system is implemented. It uses wideband FSK modulation ($f_1=5\text{MHz}$ and $f_2=10\text{MHz}$) to increase the power transfer efficiency and to provide high bandwidth data transmission. The proposed Class E AP correctly tunes to both clock frequencies $f_1$ and $f_2$, thanks to the switching tow transistors that can switch according to the data signal.

The second objective is to minimize the size and the power consumption of the implant unit. For this reason, we designed the analog front end of the implant, which consists of two main sub-blocks, the first block is the low power wideband FSK demodulator to generate both data and clock signal from the FSK carrier wave, the second block is the low power voltage generator to provide 1V supply voltage. The voltage regulation system consists of a voltage rectifier which is a full-wave cross-coupled rectifier with bootstrap capacitors to minimize the resulting threshold voltage ($V_{th}$) of the rectifier transistors and increase the power efficiency, the generator system contains also a low-dropout LDO voltage regulator which uses a control section to minimize the quiescent current of the voltage regulator and to improve its other performance. The entire circuitry is implemented using the 180 nm CMOS process.

The organization of this work is as follow, Section II presents a theoretical study for the design of wideband FSK transmitter, as well as simulation results that illustrate the 5MHz-10MHz FSK carrier across the transmission coil ($L_t$) and the receiver coil ($L_r$). The FSK demodulator, and the voltage generator with its blocks (rectifier, regulator) are detailed in Section III, this is followed by a detailed results discussions and performance comparison study. Finally, in Section IV, we conclude our research paper.

![Diagram](image_url)

**II. TRANSMITTER DESIGN**

In this section, a wideband FSK modulator to transmit both power and data to the implant unit is implemented. Class E PAs are an important element for the design of the transmission section, they are widely used because of their high theoretical efficiency (about 90-95%), their simplicity, their high energy transmission and their low power consumption when they are used as a modulator as they eliminate the need for mixers. A simple Class E PA is designed to turn and work properly for a special input clock frequency $f$, the load network should be precisely tuned, that can work simply in the design of an OOK or ASK transmitter that uses one carrier wave. Fig. 2 shows a class E PA and Table I presents the values of its parameters that work with 10 MHz input clock, the mathematical model to design a simple amplifier is calculated as follows: We suppose that, $R_L=50$ Ω (load resistor), $f=10$ MHz, $P_{out}=150$ mW, $V_{DD}=3.3$ V, and the switch with 50% of the duty cycle. For optimum the power of the class E PA we have to find the optimum resistance noted $R_{L,opt}$. We use (1) to calculate the optimum resistance.

$$P_{out} = \frac{2 \ V_{DD}^2}{1 + \frac{\pi^2}{4} \ R_{L,opt}}$$  \hspace{1cm} (1)$$

$$C_p = \frac{1}{\omega R_L \left( \frac{\pi^2}{4} + 1 \right) \left( \frac{\pi}{2} \right)} = \frac{1}{5.447 \omega R_L}$$  \hspace{1cm} (2)$$
\[ C_q = C_f \frac{5.427}{Q} \left( 1 + \frac{1.42}{Q^{2.088}} \right) \]  
\[ L_t = \frac{Q R_L}{\omega} \]  
\[ \omega = 2\pi f \]  

For high efficiency, the \( Q \) of the amplifier must be high and compatible with the desired bandwidth. A high \( Q \) of the inductive coil should make the output signal as close as possible to an ideal carrier, and very high \( Q \) reduces the effective bandwidth of the inductive link. In addition, the choice of \( Q \) is calculated as follows.

\[ Q = \frac{\omega L_t}{R} = \frac{2\pi f L_t}{R} \]  

With \( R \) is the resistance total in the series RLC branch of the amplifier, \( \omega, f, L_t \) are the quality factor, the operating frequency and the transmitter coil, respectively.

If we set the Class E AP to operate with a particular frequency, varying the frequency of the input clock causes a sharp degradation in the performance of the Class E AP. Moreover, the power loss in the NMOS switching transistor is increased [12]. This indicates that it is impossible to design the wideband FSK link on a simple amplifier using the input clock frequency shifting.

Furthermore, (2) and (3) show that for each clock frequency, only a special value of \( C_t \) and \( C_p \) can make the AP work properly. Therefore, for two different carrier frequencies \( f_1 \) and \( f_2 \), the values of \( C_t \) and \( C_p \) must be varied so that the power amplifier remains tuned at both frequencies. On the other hand, the inductor \( L_t \), and the resistance \( R \) are unchanged; moreover, the \( Q \) of the amplifier will be proportional to \( f_1 \) and \( f_2 \) [12].

To achieve higher data rate to carrier frequency ratios, and to allow easy data and clock recovery at the receiver side, wideband FSK \( (f_2 = 2f_1) \) is the best choice. Therefore, we chose \( f_2 = 2f_1 = 10 \text{MHz} \) for the wideband FSK transmitter design.

![Fig. 3. Implementation of 5/10 wideband FSK transmitter](image)

![Fig. 2. Schematic of the class E power amplifier](image)

**TABLE I**

| Parameter | Description | Value |
|-----------|-------------|-------|
| \( f \)  | Input Clock Frequency | 10MHz |
| \( L_{fc} \) | Chock Coil | 30µH |
| \( C_p \) | Parallel Capacitor | 69.78pF |
| \( C_t \) | Transmitter Capacitor | 40.1pF |
| \( R_t \) | Transmitter Resistance | 1Ω |
| \( L_t \) | Transmitter Coil | 5µH |

In opposed, when data signal is high (modulating bit “1”), the transistors \( N_2 \) and \( N_3 \) are active, and therefore, the capacitor \( C_{p2} \) is became in parallel to \( C_{p1} \), and \( C_{t2} \) is became in parallel to \( C_{t1} \). At the moment, 2 to 1 multiplexer delivers the clock frequency \( f_1 \) (5MHz) and routes it to the gate of transistor \( N_1 \) (Fig. 5). To synchronize data with clock frequencies a simple D-flop can be used.
In the implementation of proposed circuit, we chose the value of the coil $L_t$ to be 5 $\mu$H and $L_r$ to be 1.7 $\mu$H, this is typical for telemetry implant, and calculated the values of $R_r$, $C_{p1}$, $C_{t1}$, using (2) and (3) to have a $Q$ of 20 at 10MHz input clock frequency. In opposed, we calculated the value of $C_{p2}$ and $C_{t2}$, considering that $Q$ would be about 10 at 5MHz input clock frequency. The calculating of $C_{p2}$ and $C_{t2}$ is as follow, we consider a simple class E PA with 5 MHz input clock, the parallel capacitor of the simple amplifier noted $C_{p5}$ is the equivalent capacitor shown in fig. 3 $C_{p1}$ parallel on $C_{p2}$, and using (2) we can calculate $C_{p5}$.

$$C_{p5}=C_{p1}+C_{p2}=116.8 \text{ pF}$$

(7)

So

$$C_{p2}=C_{p5}-C_{p1}=74.02 \text{ pF}$$

(8)

With the same method, and using (3), the value of $C_{t2}$ is about 51.26pF. The parameters of class E PA and their values are presented in table 2. Fig. 6 and Fig.7 shows the wideband FSK signal across the external unit coil $L_t$ (transmitter) and implant coil $L_r$ (receiver), respectively. The coupling factor $k$ between $L_t$ and $L_r$ is chosen to be 0.3 (typical value).

![Fig. 6. Carrier wave across the transmitter coil $L_t$.](image)

![Fig. 7. Carrier wave across the receiver coil $L_r$.](image)

### TABLE II

**PARAMETERS AND VALUES OF 5MHz/10 MHz CLASS E PA**

| Parameter   | Description               | Value   |
|-------------|---------------------------|---------|
| $L_{ch}$    | Chock Coil                | 30$\mu$H|
| $L_t$       | Transmitter Coil          | 5$\mu$H |
| $L_r$       | Receiver Coil             | 1.7$\mu$H|
| $R_t$       | Transmitter Resistance    | 1$\Omega$|
| $R_r$       | Receiver Resistance       | 6.2$\Omega$|
| $C_{p1}$    | First Parallel Capacitor  | 69.78pF |
| $C_{p2}$    | Second Parallel Capacitor | 74.02pF |
| $C_{t1}$    | First Transmitter Capacitor | 20.62pF |
| $C_{t2}$    | Second Transmitter Capacitor | 51.26pF |
| $C_r$       | Receiver Capacitor        | 140$\mu$F|
| $R_r$       | Receiver Resistance       | 100$\Omega$|
| Element     | Transistor Type           |         |
| $N_1$       | Active Device Switch      | 2N2222  |
| $N_2$       | Commutation Transistor    | 2N2222  |
| $N_3$       | Commutation Transistor    | BSS87   |

### TABLE III

**COMPARISON OF PROPOSED FSK LINK WITH OTHER LINKS**

| Work        | [11]  | [13]  | [14]  | This work |
|-------------|-------|-------|-------|-----------|
| AP          | Linear | Class E | Class E | Class E   |
| Frequencies [MHz] | 5/10   | 0.48±0.004 | 2      | 5/10      |
| Data Rate [Mbps] | 2.5    | 0.12   | 1     | 2.5       |
| Data Rate to Carrier Frequency Ratio | 33.3   | 25     | 24    | 28.6      |
| PTE [%]     | 20    | -     | -     | 28        |
| Process     | Commercial | 130 nm | 180 nm | 180 nm    |

Table III presents the performances of the wideband FSK transmitter/receiver link proposed. The increasing of the carrier frequencies used in this work increased the bandwidth and the data rate which is 2.5Mbps. The power transfer efficiency (PTE) transferred from the source to the load calculated is about is about 28% with 7mm operation distance which is higher than the one mentioned in [13].

### III. IMPLANT DESIGN

#### A. 5/10 wideband FSK demodulator

The circuit demodulator (Fig. 8) derives a constant frequency clock directly from the FSK carrier and uses this clock to sample the data bits [15]. 5MHz/10MHz wideband FSK carrier is treated as an alternative signal and squared up using a clock regenerator (simple comparator can be used). The output of the comparator $CLK_{in}$ includes time-critical information, from which a frequency clock can be generated. Clock recovery from the Manchester coding bitstream circuit can be achieved using a digital monoflop. The monoflop accomplishes the recovery clock, and generates a negative $T_d$ whenever it is triggered by a positive frequency clock transition during the idle state. The output of the monoflop serves as a basic clock signal for further processing of the data stream. The demodulated data signal is acquired by sampling the signal squared at each falling edge of the clock signal. Fig. 9 illustrates the simulation results of wideband FSK demodulator with 5MHz/10MHz input carrier wave.
Comparator
CLK_in
FSK_signal
Monoflop
D
Q
Data_out
Clock_out

Fig. 8. Wideband FSK demodulator block diagram

Fig. 9. Simulation results of the demodulator circuit

B. Voltage regulation system

The power supply module is a power generating circuit used to convert the alternative voltage across the implant coil into a stable and preferred DC voltage. The proposed voltage regulation system has a voltage rectifier to convert the alternative signal to DC voltage and a low-drop voltage regulator to generate the preferred value to power the other sub-blocks.

1) Rectifier

The alternative signal is converted to an unstable signal using AC to DC converter. Generally, a bridge rectifier in CMOS technology or a Dickson charge pump circuit are used to design low power voltage generators. A common drawback of these rectifiers is the drop in output voltage due to the threshold voltage of the MOS transistors. The threshold voltage not only reduces the output voltage, but also reduces the efficiency of the rectifier. In addition, the problem of low power that may be present across the implant antenna is not present, so the use of voltage multipliers (such as the N-stage Dickson charge pump) is not important in our work because the inductive link guarantees enough power across the implant antenna. One of the techniques used to eliminate the threshold voltage of transistors is the using of Schottky transistors [16]. The using of Schottky transistors is not compatible with the CMOS standard, resulting in increased manufacturing cost.

The voltage drop problem is solved thanks to the structure of cross-coupled full-wave rectifier by crossing all transistors. But energy efficiency suffers greatly at higher frequencies. To eliminate the impact of the $V_{th}$ of transistors, there are different techniques that use additional bias circuits in CMOS technology. These additional bias circuits, in the form of either a source-bulk [17], dynamic drain-gate techniques [18] or a bootstrap capacitor [19], are used to generate a DC voltage to eliminate or reduce the effect of $V_{th}$ voltage.

Feature, AC to DC converter architecture proposed in [20] (Fig. 10 (a) and (b)) which is used in the implementation of proposed voltage generator because, its low power consumption, its high efficiency, its small size and its compatibility with our system. This circuit uses Bootstrapping circuits to reduce the resultant threshold voltage $V_{th}$ of transistors M3 and M4. If we consider $V_{th5}=V_{th7}$ by eliminating body effect because of different bulk biasing and process variations, the output signal can be given as follows:

$$V_{out} = V_{in} - (|V_{th5}| - |V_{th7}|)$$

(9)

$$V_{out} = V_{in} - (|V_{th4}| - |V_{th8}|)$$

(10)

From (9) and (10), the threshold voltage resultant of the overall circuit is bringing down as compared with other conventional diode-connected PMOS structure mentioned in other cross coupled approach and result in the increase of voltage signal range for giving input voltage. The using of bootstrapping capacitors educes the effective threshold of the circuit.

To bias the selected transistors ($M_5, M_6$), the Dynamic Bulk Switching (DBS) technique shown in Fig. 10 (b) is used. The DBS technique is typically used to connect most of the auxiliary path transistors ($M_5, M_6$) to the highest available voltage and to reduce current leakage, thereby reducing rectifier voltage drop and power dissipation during startup.

![Fig. 10. (a) Voltage rectifier, (b) Dynamic Bulk Biasing Circuit to bias bulk of diode-tied $M_5$ and $M_6$](image-url)
During the positive input cycle, the main conduction path passes through $M_1$ to the capacitors $C_L$ and $C_{B1}$. The NMOS cross-coupled gate transistor ($M_2$) provides a low impedance return path for the load current. A secondary path with $M_3$ connected as a diode provides a path between the input and output nodes to charge the storage capacitor $C_{B2}$. The transistor connected in diode $M_3$ does not significantly reduce the overall energy efficiency, due to its remarkably small size (large channel resistance) compared to the much larger main path $M_1$ transistor (to produce the desired small channel resistance). As a result, most of the charging current flows through $M_3$, for which the effective threshold voltage is considerably reduced by the firing capacitor connected to its gate.

In steady state, as only a small part of the charging current flows through $M_3$, its contribution to the rectifier power losses remains small. The combination $M_3$, $M_7$ and $C_{B1}$ provide the bias that reduces the effective threshold voltage of $M_1$. In negative cycles. The other circuit (consisting of $M_6$, $M_8$, $M_{B1}$ and $C_{B2}$) rectifies the input voltage (negative cycle) in the same way.

Fig. 12 shows the efficiency of our proposed circuit implanted using 180nm CMOS process versus the amplitude of the input signal $V_{in}$, the efficiency is maximum (about 84%) from an input of amplitude 0.7V. Moreover, it does not depend on the frequency in the range 1MHz - 60MHz as shown in Fig. 13, which is compatible and better with the field of medical telemetry system. Fig. 11 shows the variation of the rectifier output $V_{out}$ according to the input signal.

![Fig. 11. Output voltage versus input voltage](image1)

2) Voltage regulator

The proposed voltage regulator (Fig. 14) consists of two sections: regulation section composed of differential pair, a feedback network (4 PMOS transistors PF1 to PF4), pass device (PMOS transistor pass) and this section is followed by a two-stage amplifier and its compensation capacitor (control section).

In the regulation section, the single-stage differential amplifier is adopted as the error amplifier for the LDO voltage regulator to save the power dissipation. Thus, Fig. 14 shows that a single pair of PMOS current mirrors is used as the active resistor instead of a cascaded current mirror, because an active cascaded current mirror can minimize the bandwidth of the amplifier. Multiple amplifier stages are not necessary because the bandwidth of the error amplifier reduces as the number of amplifier stages increases and the gain is high enough for the transistors in the subthreshold region, moreover, the size of the whole circuit becomes larger.

The feedback consists of four diode-connected PMOS transistors, $P_{F1}$ to $P_{F4}$. The advantages of using PMOS transistors as active resistors are that they minimize the current flowing through the feedback network and the chip surface compared to an ordinary resistor and also eliminate the body effect. As the transistors $P_{F1}$ to $P_{F4}$ are connected in series, they all work in the sub-threshold region, so the voltages across each of them are below the threshold voltage. Thus, the current flowing through the feedback generator can be reduced.

![Fig. 12. Curve of efficiency versus input voltage](image2)

![Fig. 13. Curve of efficiency as a function of frequency](image3)
The stability of the output voltage regulator depends on the bias current $I_{SS}$ (current drain-source of $M_i$ transistor) of the error amplifier. The variation of output voltage regulator $V_{reg}$ according to a variation of the $I_{SS}$ can be approximated as follows [21].

$$\frac{\Delta V_{reg}}{\Delta I_{SS}} \cong \frac{1}{g_{mD}} \frac{R_{F3,4} + R_{F1,2}}{R_{3,4}}$$

(11)

The effect caused of load current variation on $V_{reg}$ (load regulation) is about:

$$\frac{\Delta V_{reg}}{\Delta V_{in}} \cong \frac{R_{F3,4} + R_{F1,2}}{R_{3,4} g_{mD}(r_{on})^2 r_{off}}$$

(12)

$$\cong \frac{1}{\text{Voltage gain of the differential pair}} \frac{R_{F3,4} + R_{F1,2}}{R_{3,4}}$$

The line regulation caused by variation in voltage reference is approximated [21]. It can’t be reduced anyway, since it depends only on the feedback resistors values.

$$\frac{\Delta V_{reg}}{\Delta V_{ref}} \cong \frac{R_{F3,4} + R_{F1,2}}{R_{3,4}}$$

(13)

The load regulation effect according to a variation of the load current is about [21].

$$\frac{\Delta V_{reg}}{\Delta I_L} \cong \frac{1}{R_{3,4} g_{mD}(r_{on})^2 r_{off} R_{\text{mpass}} R_{\text{opass}} R_{L}}$$

(14)

where $g_{mD}$ is the transconductance of $M_{D1}$ and $M_{D2}$ transistors in differential pair, and $R_{F1,2}$ and $R_{F3,4}$ are the equivalent resistance of feedback network, $r_{on}$ and $r_{off}$ are the output resistance of transistors NMOS and PMOS transistor, $g_{mpass}$, $R_{\text{opass}}$ and $R_L$ are the transconductance of $P_{\text{pass}}$, the output restore of $P_{\text{pass}}$ and the load resistor respectively.

From (11) and (12), to improve line and load regulation factors the gain voltage of differential pair and if the channel length of $M_{D1}$ and $M_{D2}$ should be high and long respectively. Moreover, the output resistance of the pass device can be minimized by using a short-channel PMOS transistor. Differential pair directly regulates the gate of the pass transistor. Its role is to suppress output voltage peaks, $V_{reg}$, which are due to a step in the load. The main performance of voltage regulator is influenced by the amplitude of the voltage peaks and the recovery time. The main role of the control section of the proposed voltage regulator is to control the gate voltage of $P_1$ and $P_2$ transistors and thereby stabilize the DC level at $V_{reg}$ signal.

For this function, a two-stage operational amplifier with Miller capacitor compensation was used. Control section is implemented to consume a low quiescent current and will therefore have low energy consumption.

Control section starts at the gate of $N_1$ transistor, then through the OpAmp, goes from the gate to the drain of $P_1$ transistor and then from the gate to the drain of $P_{\text{pass}}$. When the steps in load current occur, control section must be able to drive the gate of $P_1$ and $P_2$ transistors without slewing the transient. Consequently, the common source stage of the control section must produce a high enough drain current $I_{\text{DSS}}$. The required $I_{\text{DSS}}$ can be minimized by choosing a lower $W/L$ for transistors $N_1$ and $N_2$ to minimize the parasitic capacity related to the gate.

The simulation results shown in fig. 15 presents the line regulation performance. It consists in abruptly varying the input voltage ($V_{in}$) from 1.081V to 2.1V, and measuring the variation of the output voltage ($V_{reg}$). It can be seen that the output of the regulator is disturbed by the rapid variation of the input voltage, but it recovers its nominal value after a delay of less than 0.1μs with an overshoot of 8mV. Moreover, the dropout of the proposed voltage regulator and its quiescent current are 81mV and 9.9μA respectively.
The purpose of the load regulation simulation is to verify the ability of the system to regulate the output voltage in the face of a sudden change in load current. We test our regulator by applying a load current variation from its minimum to its maximum value (0 to 1 mA). Fig. 16 illustrates the response of the regulator to these load conditions. A fast variation of the load current of 1 mA causes a small variation measured on the output voltage. We measure a variation of 1 mV when the input voltage drops above the dropout voltage $V_{do}$. Afterwards, when $V_{in}$ drops above the $V_{sat}+V_{do}$ voltage the output of the regulator follows the input voltage. We measure a variation of 17 mV when $V_{in}$ varies from 1.1 V to 3 V. The dropout of the system is 81 mV.

Performances comparison with other published works are shown in Table IV. The quiescent current of this work is 9.9 µA and the voltage drop out $V_{do}$ is 81 mV which is lower than the reported results in [20],[21] and [22], we can note that a low quiescent current and a low voltage drop out will minimize directly the power consumption of the circuit. Moreover, the low line regulation (8 mV/V) and low load regulation (10 mV/mA) simulated makes the power generator works efficiently.

| Parameter                  | This work | [22] | [23] | [24] |
|----------------------------|-----------|------|------|------|
| CMOS Technology            | 180 nm    | 130 nm | 180 nm | 95 nm |
| Drop Out $V_{do}$ [mV]     | 81        | 340  | 300  | 100  |
| Output [V]                 | 1         | 0.97 | 1    | 1 to 1.5 |
| Line Regulation [mV/V]     | 8         | 14   | 2.7  | 17.7 |
| Load Regulation [mV/mA]    | 10        | 11.6 | 7    | 32   |
| Settling Time [µs]         | 1         | 7.9  | 1.6  | 7.5  |
| quiescent Current [µA]     | 9.9       | 10.5 | 28   | 80   |

3) Output waveform of the voltage generator

To verify the correct operation of our voltage regulation system, which consists of the proposed CMOS rectifier and the proposed voltage regulator mentioned in the previous sections, we made a transient analysis, we applied an input signal $V_{in}$ which is a sinusoidal signal of 10 MHz frequency and its amplitude is 5 V, this analysis presented in fig. 18 allows us to see the output signal $V_{out}$ which is regulated at a fixed value of 1 V. Therefore, at the simulation level, the system works correctly. This result indicated that the generator is capable to provide stable, efficient, and input independent power supply. Moreover, the proposed generator can be used in many wireless applications that use low power such as radio frequency identification RFID passive system.

IV. Conclusion

This paper presents the RF front-end circuits of both internal and external units of telemetry system for small animal. The external unit uses class E PA to drive the inductive link. The 5 MHz-10 MHz wideband FSK transmitter is designed to offer high bandwidth and to transfer the maximum power to the small implant, PTE calculated is about is about 28% with 7 mm operation distance. On the implant side, the 5 MHz/10 MHz wideband FSK demodulator is designed to demodulate the transmitted data and to generate the recovery clock, moreover, low-power generator circuit is created to provide 1 V supply voltage to the other circuits (demodulator, digital block and RF transceiver). Although the simulation results show the good performance of the proposed architectures, but the skin of the animals can create small effects on the sent signals. Moreover, the quality factor of PA used in this work remains effectively.
low. This system designed in this work can work effectively with other applications that use high power such as circuits implanted in large mammals and medical implants used by humans such as deep brain stimulators, cochlear implants, and pacemakers.

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Abdelali El Boutahiri was born in Rissani, Morocco in 1993. He received his Master degree in Microelectronics from Faculty of Sciences Dhar El Mahraz, Fez, Morocco, in 2017. He is now a Ph.D. student in the Department of Physics, Sidi Mohammed Ben Abdellah University, Fez, Morocco, Laboratory of Computer Science and Interdisciplinary Physics (L.I.P.I.), Normal Superior School Fez (ENSF) Sidi Mohamed Ben Abdellah University, Fez, Morocco, where he is currently an Assistant Professor and guest researcher at LIMA laboratory in UQO Canada. His current interests include a switch-mode audio amplifier, CMOS mixed-mode integrated circuit design, design techniques for RFID, Li-ion battery charger, and power management.

Karim El Khadiri received the master’s and Ph.D. degree in electrical engineering and computers from the Department of physics, faculty of sciences Dhar El Mahraz Fez, Sidi Mohamed Ben Abdellah University Morocco in 2012, and 2017, respectively. In 2019, he joined the Laboratory of Computer Science and Interdisciplinary Physics (L.I.P.I.), Normal Superior School Fez (ENSF) Sidi Mohamed Ben Abdellah University, Fez, Morocco, Laboratory of Computer Science, Signals, Automation and Cognitivism (LISAC). His main research interest includes renewable energy, medical implant, switch mode audio amplifier, CMOS mixed-mode integrated circuit design, design techniques for RFID, RF front-ends for passive tags, Li-ion battery charger.
Ahmed Tahiri received the graduate degree DES in Department of Physics, Sidi Mohammed Ben Abdellah University, Morocco in 1997, received the Ph.D. degree in physics from the University Sidi Mohamed Ben Abdellah, Faculty of Science, Morocco in 2005. He completed his doctoral studies in didactics of science in the University of Sherbrooke in Canada in 2010. He is now a professor in Normal Superior School, ENS-FEZ, Morocco. His research interests include image processing, computer science and didactics of scientific disciplines.

Hassan Qjidaa received the M.S. and Ph.D. degrees in electrical engineering from Nuclear Physics Institute of Lyon, in France 1984 and 1987, respectively. Since 1987, he served as a Research Scientist at Faculty of science in the University of Sidi Mohammed Ben Abdellah, Fez, Morocco. He has been a Professor with the Department of Physics. He is currently also a Director of the Information Analysis and Micro-system Teams (IAMS), and Vice Director of the electronic signal and systems laboratory (LESSI). His current research interests are in image processing, pattern recognition, data analysis, machine intelligence, low-power circuit design techniques for RFID, RF front-ends for passive tags, and CMOS mixed-mode integrated circuit design.