Good Motive but Bad Design: Why ARM MPU Has Become an Outcast in Embedded Systems

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ABSTRACT
As more and more embedded devices are connected to the Internet, leading to the emergence of Internet-of-Things (IoT), previously less tested (and insecure) devices are exposed to miscreants. To prevent them from being compromised, the memory protection unit (MPU), which is readily available on many devices, has the potential to become a free lunch for the defenders. To our surprise, the MPU is seldom used by real-world products. The reasons are multi-fold. While there are non-technical reasons such as compatibility issues, more importantly, we found that MPU brings virtually no security enhancement at the expense of decreased performance and responsiveness. In this work, we investigate the MPU adoption in major real-time operating systems (RTOSs), in particular, the FreeRTOS, and try to pinpoint the fundamental reasons to explain why MPU is not favored. We hope our findings can inspire new remedial solutions to change the situation. We also review the latest MPU design and provide technical suggestions to build more secure embedded systems.

1 INTRODUCTION
Embedded systems have long been operating in a closed environment, such as industrial plants and vehicle communication systems. The reliability and robustness of such systems were persistently tested in the past decades. However, these tests were conducted in a benign environment. That is, it is assumed that no adversary could actively penetrate the system. Unfortunately, this landscape has changed as more and more embedded devices are exposed to the Internet, where everyone can launch attack remotely.

Since embedded systems are typically programmed using system programming languages such as C/C++, memory errors pose a great threat to the security of these systems, especially considering that many third-party libraries run at the same privilege level as that of the core program. On the defense side, ARM, a leading chip designer for microcontroller unit (or MCU), proposes the memory protection unit (MPU). The MPU is a low-cost security extension to ARM MCUs that safeguards certain sensitive memory regions in case a piece of code is compromised. Therefore, it is a promising mitigation technique to memory vulnerabilities. Other MCUs such as MSP430 FRAM followed this design and implemented similar hardware. Unfortunately, we found this technique is seldom used in real products, although the MPU has been around for more than two decades (since the ARMv4t architecture) and has wide adoption on many devices. Our work is motivated by this observation. We hope to find out major reasons to explain why the MPU has not been popular. To do so, we investigate the usage of MPU on embedded operating systems that support it. This preliminary work reports our results on FreeRTOS, a leader in the IoT and embedded system market. We found that the MPU virtually provides no security benefit other than introducing additional overhead and programming complexity.

2 THE MPU DESIGN
ARM is the leader in MCU design. ARM has developed quite a number of different processor products (i.e., Application Processors (Cortex-A series), Real-time Processors (Cortex-R series) and Micro-controller Processors (Cortex-M series)) corresponding to different applications. Among them, Cortex-R and Cortex-M processors are usually designed to have a much lower silicon area and much high-energy efficiency for real-time and industrial applications. Therefore, they are very popular in the MCU, deeply embedded systems, and IoT market.

Due to its cost and power-efficient design, ARMv7-M/R have limited security feature support. By default, all the instructions run at the same privilege level and access the same address space. As a basic mitigation mechanism, the MPU has been provided for lightweight access control. It allows privileged software to define memory regions and assign memory access permission (read/write execution) and memory attributes (ordering and caching) to each of them. Developers need to configure two registers – Base Address Register (BAR) and Base Attribute/Size Register (BASR). Note that only privileged code can access these registers. If a memory access violates the access permissions, the processor generates a HardFault. The MPU has been supported in main-stream ARM MCUs, including Cortex-M0+/M3/M4/M7 and all Cortex-R series.

The programming model of MPU is described in the ARMv7-M/R architecture manual. First, depending on the implementation, an MPU can support 8-16 memory regions (Cortex-M0+/M3/M4/M7 which are most used by current IoT MCUs only support 8 memory regions\(^1\)). Each region should be aligned. Regarding the start address, it must start at an address of multiple of its size. Regarding the size, it must be 1) at least 32 bytes, and 2) power of two. Thus, when a region of arbitrary size is required, several smaller regions have to be used to reach the target size. Second, to add flexibly

\(^1\)https://community.arm.com/developer/ip-products/processors/b/processors-ip-blog/posts/arm-cortex-m3-processor-the-core-of-the-iot
Table 1: Popular RTOSs MPU adoption

| RTOS    | MPU support | Open source |
|---------|-------------|-------------|
| FreeRTOS | Optional    | Open-source |
| ARM Mbed | Mandatory   | Open-source |
| Nucleus 3.X | Mandatory | Proprietary |
| Keil RTX | None        | Proprietary |
| Contiki  | None        | Open-source |
| ThreadX  | None        | Proprietary |
| TinyOS   | None        | Open-source |
| TI-RTOS  | None        | Open-source |
| uC/OS-II | Optional    | Proprietary |
| VxWorks  | Optional    | Proprietary |

Table 2: Memory Map of MPU-enabled FreeRTOS on ARMv7-M3/4

| Region No. | Base  | Size  | Usage     | Permission Mode | Access Attributes |
|------------|-------|-------|-----------|-----------------|-------------------|
| 0          | 0x0   | 2GB   | Code Segment | Privilege       | rw                |
| 1          | 0x0   | 24kB  | Kernel APIs | Privilege       | rx, rwx            |
| 2          | 0x20000000 | 512B | Kernel data | Privilege       | rw                |
| 3          | 0x40000000 | 2GB  | Standard Peripherals | Privilege       | rwx               |
| 4          | Stack Bottom | Stack Depth | User Stack | Privilege       | rwx               |
| 5-7        | User-defined | User-defined | User-defined | Privilege User | User-defined      |

Memory regions which are unmapped by any MPU region falls in the default region, which can accessed in privileged mode only.

FreeRTOS APIs as the second MPU region. It is set to be read-only in privileged mode, and inaccessible in unprivileged mode.

2. The kernel maintained data (e.g., current control block) are located in a separated 512B region in RAM which is readable or writable only in privileged mode by kernel.

3. By default, standard peripherals (e.g., UARTs) could be read or written in unprivileged mode.

4. Tasks can be created to run in either privileged mode or unprivileged mode (user mode). A separated RAM region is reserved for each user mode task and is inaccessible from any other tasks. A Privileged mode task can set itself into User mode, but once in User mode it cannot set itself back to Privileged mode.

5. The remaining three regions can be defined by user mode tasks individually.

6. A memory address like system peripherals (e.g., system timer, Nested Vectored Interrupt Controller (NVIC), MPU registers, etc.) in private peripheral bus (PPB) space which are not mapped by any MPU region falls in the default region, which can accessed in privileged mode only.

4 PITFALLS OF MPU-ENABLED FREERTOS

We found that the protection implemented in MPU-enable FreeRTOS is incomplete and can be bypassed easily. Moreover, the introduced overhead makes it unsuitable in many scenarios.

Vulnerable Memory Isolation The aforementioned memory isolation can be easily bypassed. Since FreeRTOS APIs are located in a region that can only be accessed in privileged mode, a task has to raise its privilege temporarily if it needs to invoke a kernel API. This is achieved by the xPortRaisePrivilege function (xPortResetPrivilege to drop the privilege). For example, as shown in listing 1, if a user mode task needs memory from the heap, it has to invoke MPU_pvPortMalloc which uses xPortRaisePrivilege function to switch to privilege mode before invoking the FreeRTOS kernel function pvPortMalloc. On the completion of pvPortMalloc, it needs to drop the privilege by invoking xPortResetPrivilege. Since firmware binaries embed all the static compiled program as well as FreeRTOS APIs, function xPortRaisePrivilege can be easily located via reverse-engineering. Once attacker is able to carry out control flow hijacking attack (e.g., by exploiting a memory error) on any user mode task, the hijacked task can directly
escapes privilege via invoking xPortRaisePrivilege and never drop the privilege. With the escalated privilege, the hijacked task can access any resources on the device.

To verify our observation, we artificially built a firmware with a stack overflow bug, and then exploited this bug to launch a classical control flow hijacking attack. Specifically, the original return address on the stack is overwritten by the address of the function xPortRaisePrivilege. As a result, the executing privilege has been escalated. Combining more sophisticated ROP programming, we were able to take over the control flow with elevated privilege. This has been verified by our experiments and others [7]. Ironically, FreeRTOS intends to leverage MPU to protect kernel code from memory errors. However, improper protection to xPortRaisePrivilege itself deconstructs the boundary between the task code and kernel code. In other words, if there is a memory error, the added security can be bypassed completely.

```c
void * MPU_pvPortMalloc( size_t xSize )
{
    void *pvReturn;
    BaseType_t xRunningPrivileged = xPortRaisePrivilege();
    pvReturn = pvPortMalloc( xSize );
    vPortResetPrivilege( xRunningPrivileged );
    return pvReturn;
}
```

Listing 1: pvPortMalloc function in MPU-enable FreeRTOS

Conflicts with Exiting System Design Second, due to MPU integration, some existing mechanisms are diminished or even become incompatible. For example, user mode tasks cannot use dynamic queues because there is no shared memory between any two tasks. To overcome this, a task has to allocate memory statically and shares it with the peers by configuring an MPU region. Note that each peer needs an MPU region for each queue. In addition, semaphore is also a special kind of queue (its queue length is one). As a result, if a task needs multiple queues or semaphore, MPU resources soon become exhausted (there are only three free MPU regions for user mode tasks to use).

Incomplete Protection The MPU-enable FreeRTOS is coarse-grained and inflexible. First, standard peripherals are not protected by default. Although there are three remaining MPU regions can be configured individually by each user mode task, they are not suitable for protecting several separated small peripheral regions due to the alignment problem and limited number of MPU regions as mentioned in Section 2. For instance, the memory map for Audio peripheral on MPS2+ FPGA prototyping system broad (AN386) is 0x40024000-0x40024FFF (16 Bytes). However, the least length of MPU region is 32 bytes.

Second, Since FreeRTOS are located in the region that can only be accessed in privileged mode, a task has to raise its privilege temporarily if it needs to invoke a kernel API. On the other hand, developers have the demand to assign separate access rights to interrupt handlers [2]. However, NVIC registers are located in the system peripheral region which can only be accessed in privilege mode unless MPU is disabled during interrupt handling.

Increased Overhead The “protection” provided by the MPU incurs too much overhead. This is because each invocation to kernel API has to go through a full privilege switch. Since kernel API is frequently invoked in tasks, this poses significant impact on real-time performance. Our experiment shows that one thousand privilege switch takes 3.5ms in average on MPS2+ FPGA prototyping system broad (AN386) with 25MHZ CPU clock frequency. In a previous research [4], similar result was obtained. In addition, the MPU regions of each task is different from each other, so MPU regions have to be reconfigured during task switch, which will also cause time delay.

5 WHY THE MPU HAS BECOME AN OUTCAST

There are multiple reasons that make MPU less attractive. We summarizes the most important ones based on our observations/experiments.

Non-technical Reasons. First, IoT devices are low-cost energy-efficient devices. If more transistors are reserved for complex security features, not only the price of SoC could be raised accordingly, but also increased power consumption rules out many applications in which thermal design power (TDP) concerns.

Second, as IoT business continues to grow, manufacturers are facing increased time-to-market pressure. Although security is a concern, manufacturers tend to reuse existing code base, which is obsolete and less tested on the Internet. At the same time, IoT applications are becoming more and more. Moreover, developing new software leveraging MPU may cause compatibility issues. This is clearly shown in the case of MPU-enabled FreeRTOS and other developer forums [3]. In summary, if existing code works, few companies are willing to harm the profit by investing on security.

Technical Reasons. The MPU is a trimmed down version of MMU. Can we directly borrow the design of MMU to replace MPU? We believe this is infeasible due to two reasons. Except for the aforementioned cost issue, MPU actually benefits very little from advanced features available on MMU. For example, paging which is the underlying technology of virtual memory, is used in a batch of security solutions. Whereas in MCU, paging is an overkill because the RAM in an MCU never exceeds several megabyte. The benefit of virtual memory is substantially diminished. Supporting paging or not becomes a dilemma and ARM obviously chooses not to support it.

Incorporating security checking for each memory access and frequent privilege switches (as is done in MPU-enable FreeRTOS) inevitably introduce performance overhead. As shown in Section 4, the performance is so significant that real time constraints cannot be met in some scenarios [4]. There are two major sources of additional overhead. First, each task switch requires MPU reconfiguration. Second, each hardware interrupt or invocation of kernel API require privilege escalation. This rules out the MPU in many real-time applications.

6 SUGGESTIONS

We propose technical suggestions of building secure embedded systems and review the latest secure embedded system design.
6.1 MPU Revision in ARMv8-M

ARM has already acknowledged the problems with ARMv7-M MPU by revising it in ARMv8-M. However, it only mitigates the problem rather than solving it. The most noticeable improvements include increased region number (as many as 16) and more flexible region alignment. As a result, MPU registers can be used more efficiently to meet the requirement of different region sizes.

Using Start and Limit (end) address to define memory regions simplifies memory region definition and leads to a more efficient use of available memory space. As mentioned in Section 2, when a region of arbitrary size was required, several smaller regions had to be used to reach the target size in ARMv7-M, while ARMv8-M just need one region.

6.2 Suggestions

Better Usage of MPU. A serious limitation with MPU is that only limited number of regions are supported. We found that creatively using sub-region disable field (SRD) in BASR can make MPU more efficient. As mentioned in Section 2, each memory region can be divided into eight sub-regions, which can be enabled/disabled individually. Suppose a developer needs to allocate a 5KB region and a 3KB region for two tasks. Without sub-region, the developer has to configure two regions of 8KB and 4KB separately. There is a waste of 3KB and 1KB memory space correspondingly. With sub-region, the same 8KB region can be shared between the two tasks. Specifically, when running task one, MPU is configured so that the highest three sub-regions of the 8KB region are disabled. When running task two, MPU is configured so that the lowest two sub-regions of the 8KB region are disabled. In this way, the 8KB memory block is reused by the two tasks without wasting any memory.

In addition, it is a common practice that same kinds of peripherals (e.g., UART0 and UART1) have adjacent and same size memory region. Thus, developer can use a large region to cover adjacent and same size peripherals memory region. If several nearby peripherals need to be protected (i.e., only can be access in privilege mode), the developer can just disable these correspond sub-regions when running use mode tasks. Note that above approach is still not able to protect several peripheral memory regions which far from each other.

Software Workaround. Before a better MPU is proposed, on the one hand, we should continue to improve coding quality to avoid program bugs; one the other hand, we can resort to software solutions. Some previous researches [1, 4] propose to use static analysis and recompile the firmware to achieve more effective MPU usage. For example, MINION [4] uses k-means clustering to group memory sections having similar access permissions together to minimize the number of required MPU regions. It also configures MPU during task switches to avoid privilege escalation requests.

Hardware Retrofit. Although, ARMv8-M provide more powerful MPU design, it can not fundamentally solve the problems we mentioned in Section 4. In the long term, we expect a redesigned architecture that fundamentally addresses the illustrated insecurity and inflexibility in a lightweight way. Along this direction, hardware-based solutions have been proposed [5, 6]. The most representative work is TrustLite[5]. It is a radical hardware redesign that efficiently implements many novel security primitives (e.g., execution-aware MPU, secure loader) for embedded devices. In addition, ARMv8-M architecture extends TrustZone technology to Cortex-M series processors for incremental security enhancement. In particular, existing embedded software does not need heavy re-engineering but still benefits from a trusted execution domain.

7 CONCLUSION

This paper attempts to answer the question of why the MPU, as a ready-to-use security feature for protecting ARM-based MCUs, has been largely ignored by both device manufacturers and RTOS communities. We use MPU-enabled FreeRTOS as a concrete example to showcase how the claimed security benefits brought by MPU can be bypassed or undermined. Although FreeRTOS cannot represent all the embedded OSs, we believe our observations apply to other OSs because the demonstrated pitfalls root in the fundamental design drawbacks of MPU. We forecast what future MPU will be like and also provide technical suggestions to safeguard legacy devices.

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