Loss of every bit in traditional logic circuits involves dissipation of power in the form of heat that evolve to the environment. Reversible logic is one of the alternatives that have capabilities to mitigate this dissipation by preventing the loss of bits. It also have the potential to broaden the horizon of futuristic reckon with its applications to quantum computation. Application of testing strategies to the logic circuits is a necessity that guarantees their true functioning where the researchers are at par with solutions for the upcoming challenges and agreements for reversible logic circuits. Novel methods of designing Toffoli, Fredkin and mixed Toffoli-Fredkin gates based reversible circuits for testability are put fourth in this article. The proposed designs are independent of the implementation techniques and can be brought into real hardware devices after obtaining a stable fabrication environment. The experimentation for the proposed models are performed on RCViewer and RevKit tools to verify the functionality and computation of cost metrics. Fault simulations are carried out using C++ and Java to calculate fault coverage in respective methodologies. The results confirmed that all the presented work outperforms existing state-of-art approaches.

**Keywords**  First keyword · Second keyword · More

1 Introduction

In the current scenario, electronic industries are facing the problems of power utilization and overheating of equipment. In the past decades, these issues were used to be solved by adopting the practice of reducing the size of traditional transistors which has also been miniaturized up to certain nanometres. However, if the size of the transistors are further scaled, the power and overheating problems will increase exponentially [Moore 2015, Mack 2018]. Moreover, the well-known Landauer’s theory extricates the limitations of irreversible computation which also bounds the size of transistors in conventional logic circuits as they also involve loss of information in the form of heat [Landauer 1961]. Meanwhile, the demands of more and more applications in single SOCs are also leading to a drastic increase in loss of information. Reversible logic is one of the promising techniques to reduce the power requirements, as these circuits are theoretically proven for providing nearly energy free computation by preventing the loss of information.
and have the capability of producing ultra high speed and compact electronic devices. However, the logic can be applied to traditional logic circuits, but its applications to quantum computation have been proven for achieving excellence in terms of power consumption, speed and size. The identification and implementation of reversible quantum circuits have also been achieved using several probabilistic methods and ideas. Fig. 1 shows some of the dominating technologies where the researchers are currently exploring the possibilities for employing this logic at physical foregrounds.

Figure 1: Computing technologies

The framework of reversible logic circuits design and synthesis techniques is based on Toffoli and Fredkin gates, which can be further scaled into \( n \)-th order gates and libraries, commonly known as Multiple Control Toffoli (MCT) and Multiple Controlled Fredkin (MCF). Several other gates have also been proposed in the literature, but the primary components of these gates are MCF and MCT. Moreover, the final quantum decomposition of the reversible circuits are based on them. The efficiency of the designs are governed by several performance metrics defining their operating cost. These metrics are number of wires, gate cost, quantum cost and garbage output. Testing has also been extensively studied since last decade for the recognition of several types of fault models in reversible circuits. A number of novel paradigms have been presented in both the area of online and offline testing of reversible logic circuits. Online testable environment are provided over pristine design methodologies and circuit modification principles. Test data minimization in offline tesing is achieved over new deterministic, randomized test patter generation algorithms and circuit modification techniques for respective faults. The reduction of operating cost has been achieved to some needful extent in all the proposed approaches with respect to prior ones for narrowing the compensation with overall testing overheads.

A comprehensive and comparative analysis of the existing online and offline testing methodologies for nearly all fault models in reversible circuits has been completed in correlation with the problem statement in the beginning of the proposed work. An overview of reversible logic, cost metrics and associated faults models are also explained for providing background of the work. Overall work in the literature and deeply analyzed and organized into four set of categories that defining the plan of action for the novel development in the area. The illustration in Fig. 2 which shows a generalized framework to achieve the quoted objectives. As overall framework is based on fundamental MCT and MCF gates. At first, an in-depth and comparative analysis of nearly all reversible gates has been done. A three level analysis i.e., gate, design and testability level, has been performed to confirm the efficacy of the fundamental gates. At last, the proposed testable design methodologies for online testing are also applied to obtain an efficient set of testable Data Path Elements (DPE) designs.

The objectives of the work described in this paper from the authors thesis is to development of testable design methodologies at reduced testing overheads in terms of reversible circuit cost metrics, test data volume, design complexity and time. There are the following contributions toward the achievement of stated objectives:

- Novel design methodologies using Multiple Controlled Toffoli (MCT), Multiple Controlled Fredkin (MCF) and mixed Multiple Controlled Toffoli-Fredkin (MCTF) gates which shows built-in testability features towards single bit faults.
- New circuit modification methodologies for MCT, MCF and MCTF circuits are introduced for the detection of single bit faults.
- Efficient circuit modification methodologies along with general test sets are proposed for MCT, MCF and MCTF circuits for the detection of stuck-at faults to minimize the volume of test data.
- New testable designs of Full Adder, Ripple Carry Adder, 4-bit reversible array based Multiplier and Arithmetic & Logic Unit are proposed using MCT and MCF gates.
Lining up with the targeted objectives, a detailed overview and analysis of the proposed work is described in the consecutive sections:

2 Circuit Design and Modification Methodologies for Online Testing

Extensive design methodologies are realized for the construction of MCT, MCF and MCTF circuits. The constructed circuits provide built-in testability feature for the detection of single bit faults. As the utilization of parity preserved architecture with arbitrary design methodology ensures the detection of single bit flip faults in logic circuits. The methodologies are engaged in the creation of parity preserving circuits using MCT, MCF and mixed MCTF gates followed by the fault detection process. The design and test flow of the formulation of these methodologies is depicted in Fig. 3. First, an MCT gates placement technique is proposed for producing parity preserving circuits [Gaur and Singh 2016]. Second, the properties of MCF gates are exploited to showcase the scheme for the detection of faults [Singh et al. 2019]. Third, the MCT gate placement method is utilized in combination with MCF gates to achieve testability in MCTF circuits [Gaur et al. 2018c]. The fault detection is achieved by cascading a parity checker in the circuit using CNOT gates from the inputs and outputs to an additional wire. The circuits produced using proposed methods are incorporated with testability feature rather put extra efforts in converting original circuit into their testable form. A set of benchmark circuits and corresponding testable designs are implemented to observe the cost of designing and proving the efficacy of proposed schemes over existing ones.

Modifications for testability in logic circuits accounts a large increment in operating cost which enhances overall cost of manufacturing. New modification schemes for MCT, MCF and mixed MCTF circuits are introduced at lower operating cost. The modification procedures utilize the technique of parity preservation and generation for providing full coverage of single bit faults. The modification and test flow of the formulation and obtaining the measures for these methodologies is depicted in Fig. 4.

Gates cascading terminology is used for the modification of MCT circuits at the start as these gates are widely used for designing reversible circuits. The method requires only a single wire, around twice number of gates and zero garbage
cost for its formulation [Gaur et al. 2016b]. Derived gates technique is used for the modification of MCF circuits. The
gates are transformed into corresponding testable that provide fault detection as well as location functionality in MCF
circuits. It utilized parity preserving gates rather than to convert a modify a gate into corresponding parity preserving
form [Gaur et al. 2018d]. A three stage process is explored for converting MCT into MCTF circuits which largely
decreases the gate cost using a wire by utilizing gates cascading and parity preserving the property of MCF gates [Gaur
et al. 2019b]. The method involves the steps of simplification of MCT circuits into MCTF cascades and modification
of the resultant circuit. A large set of circuits and benchmarks are designed using proposed methodologies and fault
simulations are performed to evaluate the performance and validate their functionality. The detection of single bit faults
are targeted in all the proposed methodologies. Results prove that the present methods provides excellent reduction in
the operating costs as compared to existing work in this area and provide full coverage of single bit faults.

3 Circuit Modification Methodologies for Offline Testing

Test set generation in reversible circuits is followed by a number of methodologies for the detection of faults. These
methodologies utilize specific deterministic ATPG, randomized ATPG and modification approaches for the detection
of stuck-at, bridging, missing gate, cross-point and cell faults. The existence of the trade-off between testability and
overheads can be seen in all the prior methodologies in terms of performance measures like gate cost and quantum cost,
test size and time utilization. New modification methodologies are introduced for the detection of stuck-at faults in
MCT, MCF and MCTF circuits using test sets of minimal sizes. The flow for the formulation of these methods and
simulations of GTS to obtain the effective measures is depicted in Fig. 5.

The MCT circuits are modified in such a manner that the applied test vector reaches all the levels without any change in
values on the wires of the circuit [Gaur et al. 2018e]. An \( (n + 1) \) dimensional general test set \( (GTS) \) containing only
two test vectors is presented, which provides full coverage of single and multiple stuck-at faults in the circuit. Here \( n \)
denotes the number wires contained by the circuit. Deterministic approaches for the identification and detection of
different types of fault models in MCF circuits are introduced [Singh et al. 2019]. The conservative property of MCF
gates is utilized for multiple types of fault detection in these circuits by the three test sets of sizes \( 2, n \) and \( 2(n-2) \).
Moreover, both the schemes are combined for the detection of stuck-at faults in MCTF circuits [Gaur et al. 2018f]. All the
methodologies have experimented on several benchmark circuits, where an excellent reduction in overall operating
costs has been achieved as compared to prior work experimented in the same platform. Moreover, these circuits can be
tested by general test sets of fixed sizes without spending the excess time required to formulate specific algorithm under
stuck-at fault detection.
4 Testable Designs of Data Path Elements

Modern digital processors are comprised of several data path elements (DPE) like adders, multipliers, multiplexers, logical shifters, arithmetic logic unit etc. These elements are the functional units within the microprocessor which are used to execute computational operations. New testable architectures of a full adder (FA), ripple carry adder (RCA), multiplier (MUL) and an arithmetic & logic unit (ALU) using MCT and MCF gates Gaur et al. [b, 2019c]. The design and simulation flow of these elements is shown in Fig. 6.

![Figure 6: Design and Implementation flow of DPE](image)

The major role is played by the creation of parity preserving circuits for incorporating testability in overall circuits realization. Firstly a full adder is created which is used to develop the architecture of RCA. A 4-bit reversible array based multiplier with scalability factor of order $4^N$ by using RCA and Fredkin gates Gaur et al. [b]. Design of Arithmetic Logic Unit (ALU) which can be scalable up to $N$ number of bits is proposed Gaur et al. [2019c] by combining a novel structure of control unit (CU) using Fredkin gates and FA. The ALU design can be scalable for $N$-bit operations. These designs can be scalable for $N$-bit operations and incorporates testability features for the detection of single-bit faults at lower overheads which shows their exclusive features. The superiority of the designed circuits is acknowledged by implementing them using reversible circuit analyzer tool and obtaining corresponding operating costs.

5 Results and Assessment

The experiments for evaluating the efficacy of the proposed work in this thesis were performed on a machine with 64-bit Ubuntu-16.04LTS having Intel Core i7-4790, 3.60 GHz clock and 4GB memory. The prerequisites which can be seen in different part of the thesis are listed as follows:

- The benchmark circuits description in the form of *pla* and *tfc* are taken from reversible logic synthesis and benchmark pages D. Maslov, G. and Dueck, N. Scott [2004], Wille et al. [2008].
- Revkit-A toolkit is used for reversible logic synthesis Soeken et al. [2012].
- The circuits are synthesized using well-known garbage free transformation based synthesis algorithm.
- RC-viewer and RC-Viewer+ tools for designing reversible circuits is used for calculating respective measures that define operating costs D. Maslov, G. and Dueck, N. Scott [2004].
- QCA-designer is used for the implementation proposed designs and finding out physical reliability at QCA level. Walus et al. [2004].
- Fault coverage is verified using simulations carried out in C++ and Java.

A large set of benchmark circuits are taken from the two platforms which are experimented on the basis of each design methodologies. Design, synthesis and implementation of the methodologies are done using RC Viewer and Revkit tools. QCA structures are also implemented in to obtain the cost measures in some of the cases. Fault simulation is done by creating programs that realize the circuits and computing the fault coverage after inducing a type of fault for which the
design method has been developed. The implementation and simulation of the prior methodologies in the domain has also been executed to compare the presented work and calculate the efficacy. It has been analyzed the present work in the domain of design methodologies for online testing (DMOnT) has achieved the maximum reduction in cost measures by 12\% in case of MCT based designs, 61\% in case of MCF based approaches and 51\% in case of MCTF based design methodologies. The proposed work in the domain of modification methodologies for online testing (MMOnT) has achieved the reduction in cost measures by 45\% in MCT based modification techniques, 49\% in case of MCF based techniques and 75\% in case of MCTF based modification methodologies. The work done in the domain of modification methodologies for offline testing (MMOffT) has achieved the reduction in cost measures by 44\% in MCT based modification techniques, 100\% in case of MCF based techniques and 30\% in case of MCTF based methodologies. These analytics also pictured in Fig. 7.

![Figure 7: Result analysis of presented testing methodologies](image)

The performance of the presented DPE structures is analyzed by implementing 4-64 bit circuits over reversible circuit analyzer tool and compare the characteristics with the prior efficient architectures. Reported results showing the reduction of cost measures are illustrated in Fig. 8. Presented testable FA circuits achieved an average reduction by 11\% in the when all the considered parameters are combined together. RCA achieved a reduction by 12\% and 44\% has been achieved in case of MUL. A reduction up to 60\% in the gate cost has been achieved with respect to recently reported reversible ALU architectures from the literature.

The fault coverage is also calculated in nearly all the proposed methodologies and designs. Full coverage has been achieved in the respective methodologies for a considered fault model. The calculations show a large reduction in operating costs when compared to the prior work in all designs and testing methodologies. The requirements of extra hardware and time to attain testability can be eliminated by utilizing these methodologies during the design process. Hence, the methods provide solutions to both the problem of designing and testability of reversible circuits which can be adopted by any synthesis algorithm to minimize testing overheads.

### 6 Conclusion and Future Scope

The change in technology will give rise to new challenges where the manufacturers would have to commence certain proofs for their truthful functionality to be deliverable in the huge market containing highly ambitious consumers. Testing is the only way out for them to rescue from these situations. However, it is a necessary exercise but it deals with a large increment in operating costs. Moreover, a huge amount of power consumption is governed by the testing methodologies used by the manufacturers. Numerous approaches for constructing built-in testable MCT, MCF and mixed MCTF circuits over novel design methodologies and circuit modification techniques are presented for the detection of single bit faults. The performance of all the approaches is analyzed by experimenting on a set of benchmark circuits. As the logic circuits are very much prone to the occurrence of stuck-at faults, new circuit modification techniques for minimization of test data in MCT, MCF and mixed MCTF reversible circuits are introduced for their detection. In addition, this work introduces new testable designs of scalable adders, multiplier and arithmetic logic
unit for future microprocessors. MCT and MCF gates are taken into account for the formulation of all the proposed approaches as they are proven universal as well as superior for designing and testing of reversible circuits. The efficacy of all the modules is justified by providing the implementation on reliable tools for reversible circuits. The fault tolerance designing model has been identified that utilized the proposed methods in this paper [Gaur et al., 2020c], however, some of the possible limitations and scope still exists:

- This work is merely a start to the research needed in determining the feasibility of reversible circuits as a replacement to present CMOS technology.
- Development of a comprehensive tool for synthesizing reversible circuits based on the proposed framework.
- Efficient ATPG Algorithms can be explored to minimize the test-data volume for the detection of multiple types of fault models in reversible circuits.
- MCF gates based synthesis algorithm can be developed, as it has not gained significant attention by the researchers working in this area.

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