Development of a Low-noise Front-end ASIC for CdTe Detectors

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Abstract

We present our latest ASIC, which is used for the readout of Cadmium Telluride double-sided strip detectors (CdTe DSDs) and high spectroscopic imaging. It is implemented in a 0.35 \mu m CMOS technology (X-Fab XH035), consists of 64 readout channels and has a function that performs simultaneous AD conversion for each channel. The equivalent noise charge of 54.9 e\textsuperscript{-} ± 11.3 e\textsuperscript{-} (rms) is measured without connecting the ASIC to any detectors. From the spectroscopy measurements using a CdTe single-sided strip detector, the energy resolution of 1.12 keV (FWHM) is obtained at 13.9 keV, and photons within the energy from 6.4 keV to 122.1 keV are detected. Based on the experimental results, we propose a new low-noise readout architecture making use of a slew-rate limited mode at the shaper followed by a peak detector circuit.

Keywords: ASIC; Low-noise; X-ray; Gamma-ray; CdTe; Analog front-end

1. Introduction

Imaging spectroscopy of photons from 10 keV to a few hundreds keV has a variety of applications in astronomy, medicine and industry. The wide use of this imaging technique has driven the development of imagers based on CdTe detectors, since they have high absorption efficiency comparable with that of NaI and CsI, and the predominance of photoelectric absorption up to ~250 keV \cite{1,2,3}. In the field of in-vivo molecular imaging, large detection area of ~ 10 cm\textsuperscript{2} is required as well as the energy resolution of ~ 1 keV and spatial resolution of ~ 100 \mu m in order to image multiple radioisotopes\cite{4}. A double-sided strip detector is a promising solution in terms of its small number of readout channels compared to a pixel detector. However large capacitance at the input of the signal processing circuit degrades the noise performance. It is therefore crucial to design a low-noise readout chip which operates under a large detector capacitance.

We present our latest ASIC named KW04H64 which was designed for the readout of CdTe DSD having a detection area of ~ 32 mm × 32 mm, a strip pitch of 250 \mu m, and a capacitance of ~ 10 pF for each channel. The ASIC has been modified from our previous versions (e.g. \cite{5,6}). Section 2 describes the signal processing architecture of the ASIC and its predicted performance based on simulation results. Section 3 reports the first ASIC measurements. In Section 3.2 and 3.3 we discuss the measured noise performance and dynamic range of the ASIC when not connected to a detector. In Section 3.4 we evaluate the spectroscopic performance when the ASIC is connected to a CdTe and Silicon (Si) semiconductor detector, and in Section 4 we propose a new low-noise readout architecture.

2. ASIC Description

2.1. Overview

The KW04H64 ASIC is implemented in a CMOS 0.35 \mu m technology (X-Fab XH035). The chip has 64 readout channels with self-trigger capability and it measures 7.12 mm × 8.03 mm. The dual power supply line
Figure 1: Schematic of the signal processing circuit implemented in each readout channel. Typical values of resistors and capacitors are $R_1 = 5 \, \Omega$, $C_1 = 0.032 \, \text{pF}$, $R_{20} = 50 \, \text{M}\Omega$, $C_{10} = 3.2 \, \text{pF}$, $R_2 = 8 \, \text{M}\Omega$, $C_2 = 0.4 \, \text{pF}$, $C_2' = 0.1 \, \text{pF}$, $R_2' = R_2'' = 0.8 \, \text{M}\Omega$, $C_2'' = 0.4 \, \text{pF}$, $C_3' = 0.1 \, \text{pF}$ and $C_3'' = 0.8 \, \text{pF}$. Note that the ramp signal generator and the counter used in the Wilkinson ADC are implemented in another block in the ASIC whose outputs are provided to each channel.

Table 1: Main characteristics of the ASIC KW04H64.

| Parameter                     | Value                        |
|-------------------------------|------------------------------|
| Fabrication process           | X-Fab XH035                  |
| Chip size                     | 7.12 mm $\times$ 8.03 mm     |
| Number of channels            | 64                           |
| Power rail                    | $\pm 1.65 \, \text{V}$       |
| Polarity                      | Both                         |
| Gain                          | 170 mV/$\text{arc}$          |
| Dynamic range                 | $\sim 6.0 \, \text{fC}$      |
| ENC                           | $58.4 \, \text{e}^- + 12.7 \, \text{e}^-$/pF (Fast shaper) |
|                              | $33.0 \, \text{e}^- + 5.2 \, \text{e}^-$/pF (Slow shaper) |
| Peaking time                  | $\sim 0.5 \, \mu\text{s}$ (Fast shaper) |
|                              | $\sim 2.0 \, \mu\text{s}$ (Slow shaper) |
| Power consumption             | 2.1 mW/channel                |

The signals are read out after the AD conversion at the Wilkinson ADCs for each event. The ASIC has a sparse readout mode as well as a full readout mode. In the sparse readout mode, only those channels carrying the signal data are read out in order to reduce the output data size. Whether each channel carries the signal is judged by either the state of the hit signal (HIT1 in Figure 1) or the value of ADC subtracted by low frequency common mode noise[8].
2.2. Details of the analog signal processing

The CSA employs a folded cascode scheme with a PMOS input transistor having \( W/L = 1440 \mu\text{m}/1.2 \mu\text{m} \) providing a transconductance of \( \sim 3 \text{ mS} \) with a drain current of \( \sim 160 \mu\text{A} \). The drain current can be changed by an externally located potentiometer. In this paper, the feedback capacitance at the CSA is fixed at 0 V, meaning the voltage difference is larger than \( V_{\text{res, max}} \), the resistance circuit switches to the slew-rate limited mode, where it can only source or sink a maximum amount of current given by \( I_{\text{SR}} \). Figure 3 shows the DC performance of the resistance circuit at the slow shaper predicted by simulations. According to simulations, the maximum signal to be processed is expected to be \( \sim 6 \text{ fC} \) with the gain of \( \sim 170 \text{ mV/fC} \), while the noise performance is expected to be \( \text{ENC} = 58.4 \text{ e}^- + 12.7 \text{ e}^-/\text{pF} \) and \( \text{ENC} = 33.0 \text{ e}^- + 5.2 \text{ e}^-/\text{pF} \) for the fast shaper and the slow shaper respectively.

3. Experimental Results

3.1. Experimental Setup

The ASIC performance was evaluated both without a detector and with Si and CdTe detectors. In the setup without a detector, an ASIC was placed in a QFP ceramic package on a test board and test pulses generated internally were used as the input signals. The analog input pads of 56 readout channels are floated, while for 8 channels each pad is connected to a pin on the test board. Due to the difference between these two types of configurations, 56 channels were used for the performance evaluation. In the setup with a detector, bare chips were connected to single-sided strip detectors characterized in Tables 2 and 3, where the input signals to ASICs have positive polarity. The interface with a computer was established using the SpaceWire.
Table 2: Main characteristics of the CdTe detector.

| Parameter      | Value                      |
|----------------|----------------------------|
| Manufacturer   | ACRORADO                   |
| Type           | Schottky CdTe diode        |
| Size           | 4 mm × 4 mm                |
| Thickness      | 1 mm                       |
| Pt side        | 16 strip electrodes        |
|                | 250 µm pitch               |
| In side        | 1 plain electrode          |

Table 3: Main characteristics of the Si detector.

| Parameter      | Value                      |
|----------------|----------------------------|
| Manufacturer   | Hamamatsu Photonics       |
| Type           | PN Si diode               |
| Size           | 12.8 mm × 12.8 mm         |
| Thickness      | 300 µm                    |
| P side         | 32 strip electrodes       |
|                | 400 µm pitch              |

Figure 4: Noise performance at the slow shaper with respect to IBSLOW. The amplitude of the test pulse is ~0.93 fC. The error bars represent one-sigma among the 56 channels.

For IBSLOW ≥ 40 µA, we conjecture that the noise reduction for IBSLOW ≤ 40 µA is related to the slew-rate limited mode of the resistance circuit.

Figure 5 shows the ENC versus the gate voltage of the NMOS used as the feedback resistor at the CSA when IBSLOW = 10 and 40 µA. The feedback resistance increases along with an increase in the absolute value of the VGG, which leads to better noise performance, but at the expense of longer decay constants. In Figure 5, the ENC settles down when the noise from the NMOS becomes negligible compared to that from other components. The best noise performance with the smallest ENC = 54.9 e⁻ ± 11.3 e⁻ (rms) is achieved at the lowest value of IBSLOW = 10 µA.

3.3. Dynamic Range Performance

Figure 6 shows the waveforms at the slow shaper for various input charge under various IBSLOW. The waveform extends for smaller IBSLOW. This peak distortion is due to the behavior of the resistance circuit at the slow shaper. For smaller IBSLOW, the resistance circuit is apt to work in the slew-rate limited mode and can provide small current, which limits the speed of the voltage at the output of the slow shaper. It is also observed that negative pulses make the waveform more distorted than that of positive pulses. This asymmetry is also caused by the resistance circuit where the input NMOS shows a different behavior as a response to positive and negative inputs.

Figure 7 shows the relation between the input charge and the ADC value representing the amplitude of the sample-and-hold voltage from the slow shaper for various IBSLOW. The results from a typical channel are plotted. The hold timing with respect to the hit timing was 3.7 µs for IBSLOW ≥ 40 µA and 5.2 µs for IBSLOW = 10 µA. The gain dispersion was 3-8 % in...
one-sigma among the 56 channels. The dynamic range was found to be \(\sim 6.5 \text{ fC} \) at \(\text{IBSLOW} = 120 \mu\text{A}\) and became smaller following the decrease in IBSLOW, reaching \(\sim 2.0 \text{ fC} \) at \(\text{IBSLOW} = 10 \mu\text{A}\). This trend can be well explained by the behavior of the resistance circuit at the slow shaper and the sample-and-hold circuit. Since in the sample-and-hold circuit the voltage is sampled at a given time after the hit signal is issued, it is impossible to correctly capture the peak if it moves with the signal charge.

3.4 Spectroscopic Performance

The spectra in Figure 8 were acquired using the CdTe detector with \(^{241}\text{Am}, \text{Co}\) and \(^{133}\text{Ba}\) sources, where the detector was biased at 1000 V and cooled at \(-20 ^\circ\text{C}\). The slow shaper was selected as the input of the ADC, and the reference current was set at \(\text{IBSLOW} = 40 \mu\text{A}\). We confirmed the detection of photons whose energy ranges from 6.4 keV to 122.1 keV. The energy resolution at 13.9 keV (FWHM) was found to be 1.12 keV. We also found that energy resolution becomes worse as the peak energy increases, which we will investigate further.

Figure 9 shows the spectrum acquired using an \(^{241}\text{Am}\) source, where the Si detector was biased at 80 V and cooled at \(-10 ^\circ\text{C}\). The slow shaper was selected as the input of the ADC, and the reference current was set at \(\text{IBSLOW} = 40 \mu\text{A}\). The energy resolution was found to be 1.2 keV at 59.5 keV.

4. New low-noise readout architecture

According to the results reported in Section 3.2 and 3.3, the slew-rate limited mode offers better noise performance with some penalty in the dynamic range as long as the sample-and-hold circuit is employed. Figure 10 shows the peaking time and the peak amplitude with respect to the negative input charge. The peaking time gets longer as the input charge increases when the slow shaper works in the slew-rate limited mode, while the peak voltage maintains the linearity regardless of the mode for the input charge up to and above 8 fC. This implies that the combination of the slew-rate limited mode and the peak detector circuit should satisfy both the noise performance and the wide dynamic range.

On the other hand, it should be noted that there exist some reservations to employ the peak detector circuit with the slew-rate limited mode. This architecture makes it hard to detect the common mode noise. Care must be taken so that the AD conversion starts after the voltage reaches its peak for the largest signal to be targeted. In addition, the peaking time reflects noise performance. These matters must be taken into account in employing this architecture.

5. Summary

The KW04H64 ASIC has been designed for the readout of CdTe DSD allowing for high spectroscopic imaging. Evaluating its performance experimentally, the low noise performance, ENC of \(54.9 \text{ e}^- \pm 11.3 \text{ e}^- \text{(rms)}\), has been demonstrated without any detector. From the evaluation of the spectroscopic performance using the CdTe single-sided detector, the ASIC demonstrated the high
Figure 8: Energy spectra acquired with various sources from one channel where only single hit events were extracted.

Figure 9: Energy spectrum acquired using a $^{241}$Am source from one channel where only single hit events were extracted. The horizontal axis represents the value of ADC subtracted by common mode noise.

Figure 10: Peaking time and amplitude with respect to the test pulse negative input charge for different IBSLOW values. The peaking time is defined as the time when the waveform reaches its minimum value.

energy resolution of 1.12 keV for the energy at 13.9 keV and the capability of detecting photons within the energy from 6.4 keV to 122.1 keV. Investigating the circuit behavior under the slew-rate limited mode of the slow shaper, we propose a new readout architecture incorporating a peak detector circuit to achieve a low noise readout without sacrificing the dynamic range. The confirmation of the readout architecture and the performance evaluation of the CdTe DSD will follow.

6. Acknowledgement

This work was supported by JSPS KAKENHI grant number 18H05463. The authors thank P. Caradonna for his critical reading of the manuscript.

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