Study and optimization of heterojunction silicon solar cells

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Abstract. This paper reports on the optimization of fabrication parameters of a heterojunction silicon solar cell using computer simulations and comparison of the simulation data with experimental results. The optimization of the photovoltaic devices was performed with respect to the thicknesses of amorphous silicon layers. As a result, a reasonable correlation between the simulation data and experimental results is observed within the acceptable margin of error with respect to heterojunction silicon solar cells with efficiency exceeding 20%.

1. Introduction
Heterojunction silicon solar cells, also known as HIT (heterojunction with intrinsic thin layer) cells, currently demonstrate efficiencies exceeding 26% [1-3]. Their advantages over diffusion-based technologies include, among others, low manufacturing temperatures below 200°C (compared to 900-1000°C) and a weaker dependence of power output on operating temperature [4]. Despite impressive recent achievements, there is still potential for further improvement of the heterojunction silicon technology both in terms of reaching higher efficiency and reducing the cost. The HIT cells have a rather complex structure representing a $p$-$i$-$n$-$i$-$n'$ junction, where an $n$-type monocrystalline silicon wafer is "sandwiched" between intrinsic and doped layers of amorphous silicon (a-Si). The multilayered structure of the cell brings significant complications to optimization of its performance in laboratory due to the requirement to consider several parameters at once. Computer simulation is an important tool in the study of solar cells that enables their optimization in the absence of significant resources with respect to a number of parameters [5-8]. This approach is employed herein to optimize fabrication parameters of a heterojunction silicon solar cell and compare the obtained data with experimental results.

2. Experiment
Simulation of HIT solar cells was performed using the AFORS-HET simulation tool. The AFORS-HET software is intended for simulation of heterojunction solar cells based on silicon and amorphous silicon and features a rich database with parameters of these materials. The underlying principles of AFORS-HET have been reported elsewhere [9]. The built solar cell models used material parameters both integrated within the software and measured separately on fabricated samples. Some of the key parameters of monocrystalline and amorphous silicon layers used in the simulation are given in tables 1 and 2. Device fabrication was performed using commercial 170 μm-thick $n$-type
monocrystalline silicon wafers subjected to proprietary processes of texturing and oxidation. Oxide layer removal was performed immediately prior to the amorphous layer deposition in a dilute aqueous solution of hydrogen fluoride. This was followed by plasma-enhanced chemical vapour deposition (PECVD) of intrinsic ($i$) and doped ($p/n$) a-Si layers on both sides of the wafer to obtain a $p-i-n-i-n^+$ structure, which was capped with indium-tin oxide (ITO) by means of magnetron sputtering. Finally, the contact grid was printed using a commercial Ag-based metallization paste. Measurements of the cell I-V characteristics were made using a PV Measurements IVL-16 setup.

### Table 1. Parameters of monocrystalline $n$-Si simulated using the AFORS-HET tool.

| Parameter                          | Value                |
|------------------------------------|----------------------|
| Dielectric constant                | 11.9                 |
| Electron affinity                  | 4.05 eV              |
| Effective conduction band density  | $2.846 \times 10^{19}$ cm$^{-3}$ |
| Effective valence band density     | $2.685 \times 10^{19}$ cm$^{-3}$ |
| Band gap $E_g$                     | 1.124 eV             |
| Effective electron mobility        | 1111 cm$^2$/Vs       |
| Auger electron recombination       | $2.2 \times 10^{-22}$ cm$^{-6}$/s |

### Table 2. Parameters of amorphous $p/n$-Si simulated using the AFORS-HET tool.

| Parameter                          | Value                |
|------------------------------------|----------------------|
| Dielectric constant                | 11.9                 |
| Electron affinity                  | 3.9 eV               |
| Effective conduction/valence band density | $10^{20}$ cm$^{-3}$ |
| Band gap $E_g$                     | 1.72 eV              |

### 3. Results

The results presented in this paper represent both the data obtained from computer simulations and the measurements on fabricated devices. Further, we describe the use of HIT cell simulations using the AFORS-HET tool to optimize the device structure with respect to a number of parameters. This is followed by comparison of the simulation data with the results of the structure optimization performed on fabricated devices. Finally, the device model is adjusted based on comparison of the simulation data and experimental results.

The structure of a HIT cell is given in figure 1. Separation of the electron-hole pairs generated within the device proceeds by means of a built-in electric field between an $n$-type crystalline silicon wafer and a $p$-type amorphous silicon layer. These two layers are separated by a thin intrinsic amorphous layer employed for passivation of surface states in a crystalline silicon substrate. The rear side of the crystalline wafer is also coated with an intrinsic amorphous layer, followed by an $n$-type amorphous back-surface field (BSF) layer intended to reduce the minority carrier current in this region. This structure is "sandwiched" from both sides by a transparent conducting oxide and metallic contacts. The initial parameters of the simulated solar cell structure are presented in table 3.

The simulated initial device performance was quite poor. It was characterized by the following parameters: short-circuit current $J_{SC} = 29.25$ mA·cm$^{-2}$, open-circuit voltage $V_{OC} = 683.6$ mV, and fill factor $FF = 56.3\%$, resulting in a power conversion efficiency ($PCE$) of 11.26%.
Figure 1. Schematic representation of the heterojunction silicon (HIT) solar cell structure.

Table 3. Initial parameters of the HIT solar cells simulated using the AFORS-HET tool.

| Parameter | Value |
|-----------|-------|
| $d_{p-a-Si}$ | 10 nm |
| $N_{a,p-a-Si}$ | $7.47 \times 10^{19}$ cm$^{-3}$ |
| $d_{n-c-Si}$ | 300 μm |
| $N_{d,n-c-Si}$ | $1.5 \times 10^{16}$ cm$^{-3}$ |
| $d_{n-a-Si}$ | 5 nm |
| $N_{d,n-a-Si}$ | $1 \times 10^{20}$ cm$^{-3}$ |
| $d_{i-a-Si, front}$ | 10 nm |
| $d_{i-a-Si, rear}$ | 3 nm |

- $d$ denotes the layer thickness.
- $N_a$ denotes the doping concentration of acceptors.
- $N_d$ denotes the doping concentration of donors.

Optimization of the device structure was performed by varying the following parameters in the sequence of their diminishing impact on cell efficiency (identified separately in a work due for publication):

- Doping of the front emitter layer,
- Thickness of the front intrinsic layer,
- Doping of the silicon wafer,
- Thickness of the front emitter layer,
- Thickness of the silicon wafer,
- Doping of the back-surface field (BSF) layer at the rear,
- Thickness of the back-surface field (BSF) layer at the rear,
- Thickness of the rear intrinsic layer.

Taking into consideration the arguments presented elsewhere [10], the intrinsic layer thickness was set to be 5 nm, which is related to the dependence of the minority carrier lifetime within the silicon wafer on the thickness of the passivating $i$-a-Si layer. As a result, the following output characteristics of the optimized cell were obtained: $J_{SC} = 33.60$ mA·cm$^{-2}$, $V_{OC} = 735.2$ mV, $FF = 84.95\%$, and $PCE = 21.02\%$. The respective cell fabrication parameters are given in table 4.

Figure 2 compares the results of computer simulations with the experimental data obtained on fabricated devices with varying thickness of the front $i$-a-Si layer. The intrinsic layer thickness is expected to affect the device performance in two ways: firstly, due to the above mentioned passivation
requiring thicker layers to obtain lower recombination and a higher $V_{OC}$, and secondly, due to the increase in series resistance with growing thickness. The optimal $i$-$a$-Si layer thickness, as suggested by the experimental results, is 7 nm. Qualitative differences between the simulation and the experiment may be explained by the fact that the simulation did not account for the significance of passivation of crystalline silicon surface states. Therefore, increasing thickness of the intrinsic amorphous layer in this case is only expected to result in a higher series resistance. In reality, the requirement for surface passivation leads to a minimum intrinsic layer thickness of 5-7 nm, based, for example, on the dependence of the minority carrier lifetime in a crystalline silicon wafer on the passivation layer thickness presented earlier [10].

Table 4. Optimized parameters of HIT solar cells simulated using the AFORS-HET tool.

| $d_{p-a-Si}$  | 7 nm | $N_{p-a-Si}$ | $1 \times 10^{20}$ cm$^{-3}$ |
|---------------|------|-------------|-----------------------------|
| $d_{n-c-Si}$  | 260 μm | $N_{d,n-c-Si}$ | $2 \times 10^{17}$ cm$^{-3}$ |
| $d_{n-a-Si}$  | 20 nm  | $N_{d,n-a-Si}$ | $1 \times 10^{20}$ cm$^{-3}$ |
| $d_{i-a-Si,\text{front}}$ | 5-7 nm | $d_{i-a-Si,\text{rear}}$ | 5 nm |

Figure 2. Variation in heterojunction silicon solar cell performance with front $i$-$a$-Si layer thickness: (a), (c) – simulation; (b), (d) – experimental results.

Figure 3 considers the change in device performance with thickness of the $p$-type emitter layer. Preliminary simulation results showed that the optimal emitter thickness was 1 nm (or as low as possible), which is explained by the tendency to minimize the scattering of charge carriers and the resistance of cell series. Separately, based on the calculations using the Anderson model, the minimal thickness of the amorphous silicon layer was evaluated with the assumption that it must exceed the width of the space charge region [11]. The calculations have shown that the internal electric field
propagates into the amorphous silicon layer to a distance of 3 nm at the ‘amorphous silicon-crystalline silicon’ interface and to a distance of 4 nm at the ‘amorphous silicon-ITO’ interface. In total, the minimal p-type emitter layer thickness is expected to be at least 7 nm. This argument has been taken into account to specify the minimum p-type layer thickness in the final optimized model of the solar cell. However, the simulation results in figure 3 do not appear to account for these considerations, as evidenced by the data corresponding to a p-type layer thickness below 7 nm. The experimental results in figure 3 suggest that the optimum p-type layer thickness is 10 nm, agreeing rather well with the theory.

**Figure 3.** Variation in heterojunction silicon solar cell performance with p-type emitter layer thickness: (a), (c) – simulation; (b), (d) – experimental results.

In contrast to the front p-type emitter layer acting as a component of a semiconductor junction and an optical filter, the n⁺-type layer is located at the rear of the device, so the influence of its thickness on solar cell output characteristics is not expected to be significant (figure 4). At the same time, it is evident that, on the one hand, the n⁺-type layer thickness must be sufficient to enable formation of the back surface field, and, on the other hand, reduction in thickness is consistent with minimization of series resistance. In terms of computer simulations, variation in thicknesses of the rear i-type and n⁺-type a-Si layers in the range from 1 to 50 nm did not result in any changes in the device output characteristics.

Based on the laboratory optimization of the HIT cell structure, optimal parameters of a HIT-structured solar cell were elucidated for the given wafer quality, and an optimized solar cell was fabricated with the following output characteristics: $J_{SC} = 37.51 \text{ mA}\cdot\text{cm}^2$; $V_{OC} = 713 \text{ mV}$; $FF = 77.18\%$; $PCE = 20.64\%$. The simulated values for comparison were as follows: $J_{SC} = 30.33 \text{ mA}\cdot\text{cm}^2$; $V_{OC} = 781.6 \text{ mV}$; $FF = 85.44\%$; $PCE = 20.26\%$. Respective device parameters are given in table 5.
Figure 4. Variation in open-circuit voltage of a heterojunction silicon solar cell with $n^+$-type rear layer thickness: (a) – simulation; (b) – experimental results.

Table 5. Final optimized parameters of HIT solar cells.

| Layer Type | Thickness | Doping Density |
|------------|-----------|----------------|
| $d_{p-a-Si}$ | 10 nm | $N_{a,p-a-Si}$ | $3.59 \times 10^{20}$ cm$^{-3}$ |
| $d_{n,c-Si}$ | 170 μm | $N_{d,n,c-Si}$ | $2.15 \times 10^{17}$ cm$^{-3}$ |
| $d_{n-a-Si}$ | 20 nm | $N_{d,n-a-Si}$ | $1 \times 10^{20}$ cm$^{-3}$ |
| $d_{i-a-Si, front}$ | 7 nm | $d_{i-a-Si, rear}$ | 9 nm |

Here, the rear $i$-a-Si layer thickness was increased from 7 to 9 nm in order to ensure an efficient surface defect passivation.

4. Conclusion

This paper reports on the efforts of using computer simulation results to optimize the device structure and performance of a heterojunction silicon solar cell. Optimization of the cell performance was done with respect to thicknesses and doping concentrations of the functional layers. In addition, HIT cell fabrication was performed in laboratory to compare the simulation data and experimental results. Reasonable matching of simulation and experimental results is observed, however, further studies are required to account for material properties in the search for higher device efficiencies.

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