Reducing noises of high-speed Bi-JFET charge-sensitive amplifiers during schematic design

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Abstract. The technique of circuit noise reduction of charge-sensitive amplifiers containing bipolar and junction field-effect transistors is considered. The initial and improved circuit of the integrated charge-sensitive amplifiers using the above mentioned technique, the results of the step-by-step noise reduction when changing the sizes and operating modes of transistors, and improvement of the bias circuits are presented.

1. Introduction

Charge-sensitive amplifiers (CSA) are widely used in analog sensor interfaces to convert the charge generated by the sensors into the voltage. In most cases, the main requirement for the CSAs is to ensure the minimum noise level and maximum fast response which is necessary to prevent the pileup.

At the same time, for a number of applications [1-4], much attention is paid to achieve other parameters, for example, the layout sizes of the CSA in multi-channel integrated circuits or low power in case of the cooled CSA.

Significant differences to the required characteristics make it unsuitable to use operational amplifiers to create CSAs and require the development of special circuits, with particular attention to choosing the type and mode of operation of the input transistor [5, 6].

For fast signal processing of capacitive sensors with a large internal capacitance (CD), the most often used are CSAs made according to the scheme of a folded cascode [1, 7]. The cascode provides the high gain, the bandwidth, the small input capacitance, and the folded cascode additionally makes possible to increase the amplitude of the output voltage without the use of level shift circuits.

The noise level of the folded cascode is determined by the parameters of the input transistor, instead of which the low-noise junction field-effect transistors (JFET) with a large transconductance is most often used. To increase the transconductance gM, the parallel connection of several transistors, including the discrete ones, is usually used. Unfortunately, the manufacture of the CSAs with discrete...
JFETs requires significant labor costs for their preliminary selection by parameters since the transistors used in parallel connection should be with identical characteristics [7, 8], and the production dispersion of JFET parameters can reach 100% [9]. Integrated JFETs do not have this drawback, the identity of their parameters is significantly higher.

Thus, when minimizing the noise of the CSA, made according to the scheme of the folded cascode, it is necessary to maximize the transconductance of the input JFET and minimize the noise of the rest of the circuit [8, 10, 11], providing the required fast response.

Earlier, we developed a high-speed CSA which is a part of the commercially available structured array MH2XA010 [12], the features of which are radiation hardness, low power, and minimum layout size on the semiconductor wafer.

The purpose of this article is to consider the step-by-step schematic improvement of the previously developed CSA to reduce its noise when operating with sensors with an internal capacitance of about 500 pF.

2. Description of the original CSA circuit operation

The original electrical CSA circuit is shown in figure 1 [12].

The CSA contains a folded cascode with input p-JFET J2 with the ratio of the gate width to the length W/L=645 μm/1.5 μm, an n-p-n transistor with common base Q12 and an active load on p-n-p transistors Q1, Q4 in cascode connection, and also emitter follower Q7-Q10 on complementary bipolar transistors. In the CSA the capacitive feedback circuit is separated from the resistive feedback circuit, which sets the quiescent output voltage in the absence of the input signal. In the CSA the capacitive feedback is provided by capacitor CF between the pins In and Out, and the resistive feedback is provided by resistor RF between the pins In and RF. This is done in order to ensure the voltage to be about zero at the Out pin due to the shift in the constant voltage level at resistor R6 in the absence of the input signal. Zero voltage is applied to pin Vs, but by changing the voltage at this pin, the output voltage can be adjusted in the absence of the input signal.

![Figure 1. The electrical circuit of the original CSA.](image-url)

The parameter characterizing the noise properties of the CSA is an equivalent noise charge (ENC), which being fed to the input of the CSA, will produce a voltage equal to the rms value of the noise voltage (VNOISE) at its output.
The ENC includes a parallel component described by the noise current generator connected in parallel to the CSA input, and a serial component, which is taken into account by the noise voltage generator connected in series to the CSA input.

The main parameters of the CSA with the folded cascode characterize the relationships [13].

\[
K_v \approx g_{M2} R_{\Sigma},
\]

\[
K_{QV} \approx \frac{1}{C_F} \left( \frac{1}{1 + \left( \frac{C_D + C_{STR} + C_{INP}}{C_F} \right)} \right),
\]

\[
\tau_R = \frac{\tau_{AMPL}}{1 + K_v \frac{C_F}{C_D + C_{STR} + C_{INP}}},
\]

\[
\tau_{AMPL} \approx C_{\Sigma} R_{\Sigma}
\]

\[
C_{INP} = C_{DG} K_M,
\]

where \(K_v\) – voltage gain of the folded cascode without feedback; \(g_{M2}\) - transconductance of input transistor J2; \(R_{\Sigma}\), \(C_{\Sigma}\) - total resistance and capacitance of all parallel circuits connected to the high-impedance node of the folded cascode - collector Q12, respectively; \(K_{QV}\) - conversion factor of the input charge to the output voltage of the CSA under the assumption the gain \(K_v\) maintains a constant value in the frequency spectrum of the input signal; \(C_{STR}\) - stray capacitance connected to the CSA input; \(C_{INP}\) - input capacitance of the folded cascode; \(\tau_R\) – time constant of the rising edge of the CSA; \(\tau_{AMPL}\) - dominant time constant of the folded cascode; \(C_{DG}\) - capacitance of the back-biased p-n-junction of the drain-gate; \(K_M\) - voltage gain at the drain of input transistor J2.

From (3), taking into account (1) and (4) with a large gain \(K_v\), which provides \(K_v C_F >> C_D + C_{STR} + C_{INP}\), we can obtain

\[
\tau_R = \left( C_D + C_{STR} + C_{INP} \right) \frac{C_{\Sigma}}{C_F g_{M2}}.
\]

Relation (6) is refined in comparison with relation [7].

As follows from (6), when the sensor capacitance is increased in order to maintain the required fast response, it is necessary to increase the transconductance of the input JFET or the capacitance in the feedback circuit; however, with an increase in \(C_F\), \(K_{QV}\) decreases.

In accordance with the Shichman – Hodges model in the JFET saturation region, i.e. for \(V_{SD} \geq V_{TH} - V_{GS}, V_{GS} < V_{TH}\) (the signs are given for the p-JFET), the following relation is true

\[
I_D = \beta (1 + \lambda V_{SD}) \left( V_{TH} - V_{GS} \right)^2
\]

where \(I_D\) - drain current; \(\beta\) - specific transconductance of the transfer characteristic (\(\beta \sim W/L\)); \(\lambda\) – coefficient of modulation of the channel length; \(V_{TH}\) - pinch-off voltage (for the p- JFET - positive value), \(V_{SD}, V_{GS}\) – source-drain and gate-source voltage, respectively.

From (7) we can obtain

\[
g_M \approx 2 \sqrt{I_D \beta},
\]
\[
\frac{g_M}{I_D} \approx \frac{2}{(V_{TH} - V_{GS})}.
\]

Obviously, to increase \( g_M \), it is necessary to increase \( W/L \) and \( I_D \). With an increase in the drain current, the power dispersed by the folded cascode increases and the dependence of \( I_D \) on the temperature \( T \) increases. Moreover, as follows from (9), the best ratio of the fast response and the noise of the CSA, determined by \( g_M \), to the power consumption, which mainly depends on \( I_D \), will be reached near the pinch-off voltage, i.e. at \( V_{GS} \approx V_{TH} \). From our point of view, it is most expedient to select \( I_D \) of the input JFET from the condition of ensuring its minimum temperature change \( \Delta I_D/\Delta T \approx 0 \), which for most JFETs is achieved at \( |V_{GS}|=|V_{TH}|=0.66 \) V [9]. Such a drain current is called optimal, i.e. \( I_{OPT}=I_D \) at \( |V_{GS}|=|V_{TH}|=0.66 \) V.

It should be noted that with an increase in \( W/L \), \( C_{DG} \) and, consequently, \( C_{INS} \) increase proportionally, which especially affects the fast response of the CSA at small \( C_D \).

On the base of expressions (1)-(9) and analysis of the known circuit solutions of the CSA [1, 7, 8, 11], we formulate recommendations for reducing the ENC, taking into account the high fast response for the sensors with high capacitance.

1. It is known that when processing a sensor signal in the form of a current \( \delta \) -function using the CSA and the band-pass filter, the minimum of the ENC serial component is ensured by the so-called “capacitive matching of the input JFET and the sensor”:

\[
C_D + C_T + C_{STR} + C_{DG} = C_{SG},
\]

where \( C_{SG} \) - capacitance of the back-biased p-n junction of the source-gate.

For \( C_D = 500 \) pF, it is impossible to fulfill such a condition in the integrated CSA due to the limited area of the semiconductor chip. Thus, for the integrated CSA, the maximum increase in \( W/L \) is recommended, limited only by the allowable occupied area on the chip or other considerations.

2. An increase in \( R_T \) leads to a decrease in the ENC. It is difficult to form an \( R_T \geq 1 \) M\( \Omega \) in the integrated CSA, therefore it is advisable to use an external \( R_T \geq 10^6 \) \( \Omega \). It should be borne in mind that high-value resistors have a parasitic capacitance, which causes a change in the shape of the output pulse signal.

3. In order to reduce the ENC of the CSA in the folded cascode (figure 1), it is necessary to increase \( g_{M2} \), the ratio \( I_{D2}/I_{C12} \), use low-noise transistor \( Q_{12} \), increase the resistance of the emitter resistors, and provide low impedance on the ac signal of the circuit nodes, determining the operating mode.

Features of increasing \( g_{M2} \) are discussed above.

When using a low-noise transistor as \( Q_{12} \), it must be borne in mind that in most low-noise bipolar transistors, the low resistance of the base region, which is the main source of noise, is achieved by increasing the layout sizes, which leads to an increase in the capacitance of collector junction \( Q_{12} \) and \( C_2 \). The reduction in the ENC when using such a transistor can be achieved by reducing the bandwidth of the folded cascode. \( Q_{12} \) should be not only the low noise transistor, but also with the high transition frequency.

4. The transistor current source is characterized by greater noise than the resistor one, therefore it is recommended to set the required \( I_{D2} \) using the resistor connected between drain \( J2 \) and \( V_{EE} \), and its resistance must satisfy the condition \( R \geq 1/g_{M2} \).

3. Simulation results

Prior to the simulation, the current-voltage curves (CVC) of the test transistor, identical in layout sizes to the input JFET, had been determined by which the pinch-off voltage \( V_{TH}=1.78 \) V and the optimal drain current \( I_{D0PT}=0.685 \) mA at \( V_{GS}=1.12 \) V and the ratio \( g_S/I_D=3.53 \) V\( ^{-1} \) at \( V_{GS}=1.12 \) V were determined (figure 2).

The circuit was upgraded for the elements of the array chip MH2XA030 [14], which imposed restrictions on the available resistances of the resistors and the possibility of changing \( W/L \) of the input.
JFET. So, the required resistance, for example R₇=332 Ohm in figure 3, was obtained due to the series and parallel connection of resistors formed on the array chip.

Step-by-step simulation of the original circuit (figure 1) was carried out with the following values of the main parameters \(C_F = 1 \text{ pF}, \ C_D = 500 \text{ pF}, \ R_F = 10^9 \text{ Ohm}, \ T = 30^\circ\text{C}\). The drain current of the input JFET, the current consumption \(I_{EE}\) from the negative voltage source \(V_{EE}\), \(K_QV\), \(V_{NOISE}\) were determined, \(\text{ENC}=V_{NOISE}/K_QV\) in electrons was calculated, and the ratio of \(\text{ENC}_N\) at each stage of upgrading (paragraphs 1-7 in the table 1) to \(\text{ENC}_1\) of the original circuit was determined. According to the simulation results in the original circuit \(I_{D2} = 0.646 \text{ mA}\), which is very close to the \(I_{DOPT}\) value.

![Figure 2](image_url)

**Figure 2.** The transfer CVC of the input JFET at \(V_{SD} = 5 \text{ V}\).

**Table 1.** The results of simulating the parameters of the CSA at different stages of upgrading at \(CD = 500 \text{ pF}\).

| Changes in the CSA circuit | Parameter value  |
|---------------------------|------------------|
|                           | \(I_{EE}, \text{ mA}\) | \(V_{\text{NOISE}}, \text{ mV}\) | ENC, el. | \(\text{ENC}_N/\text{ENC}_1\) |
| 1 The original circuit (figure 1) | 1.698 | 4.755 | 33404 | 1.000 |
| 2 The circuit of p.1, but J2 consists of 9 p-JFETs connected in parallel with W/L=645 \(\mu\text{m}/1.5 \mu\text{m}\) | 1.694 | 3.433 | 23472 | 0.703 |
| 3 The circuit of p. 2, but drain current J2 is increased by a factor of 9 | 6.920 | 9.845 | 67350 | 2.016 |
| 4 The circuit of p. 3, but Q15 is removed, resistor R7 is connected to J2 drain | 6.818 | 2.457 | 17890 | 0.536 |
| 5 The circuit of p. 4, but resistor R1 is increased | 6.810 | 2.078 | 15387 | 0.461 |
6 The circuit of p. 5, but the voltage on resistor R7 and its resistance are increased, resistance of R3, R10 are reduced

| Current Setting | ENC | Current | CSTR | Temperature Stability |
|-----------------|-----|---------|------|-----------------------|
| 6.848           | 1.828 | 13173   | 0.394 |                       |

7 The circuit of p. 6, but a capacitor connected to Q12 base is introduced. The resulting circuit is shown in figure 2

The simulation results for all circuit changes are shown in the table. As the current-setting circuits for all circuit options remained without significant adjustments and the simulation was performed in idle mode, the change in $I_{EE}$ was almost equal to the change in $I_{D2}$.

At the first stage, the transconductance of the input JFET was increased maximum possible for the array chip due to nine p-JFETs connected in parallel with W/L=645 μm/1.5 μm (paragraph 2 of the table), which led to the decrease in the ENC by 29.7%, but caused the increase in $C_{STR}$ from 5.96 pF to 53.68 pF and the deterioration in temperature stability because of $I_{D2}\neq I_{DOPT}$.

Then, to satisfy the condition $I_{D2}=I_{DOPT}$, current $I_{D2}$ was increased by a factor of 9, while the transconductance $g_{M2}$ increased to 20.71 mA/V compared to 2.41 mA/V in the original circuit, but the ENC increased by 101.6% (paragraph 3 of the table) due to the increased shot noise of the collector current of transistor Q15.

A significant reduction in the ENC (paragraph 4 of the table) was ensured by replacing the current source on Q15 with a resistor $R7>1/g_{M2}=48$ Ohms.

The final stages of upgrading were:

- an increase in the resistance of resistor R1;
- an increase in the voltage across resistor R7 due to the change in the connection of Q11, which made it possible to increase the resistance of R7 while maintaining the condition $I_{D2}=I_{DOPT}$;
- a reduction of the impedance on the ac signal of the current-setting nodes by reducing the resistance of circuit R3, R10 and connecting the base Q12 to capacitor C1.

The electrical circuit of the improved CSA is shown in figure 3.

It is difficult to further decrease the ENC by increasing the resistances of R1 and R7 because the increase in R1 leads to the decrease in the collector current of Q4, the increase in $R_2$, $\tau_{AMPL}$ and the CSA does not provide the required fast response, and the increase in R7 while maintaining the condition $I_{D2}=I_{DOPT}$ requires the increase in the negative source voltage $V_{EE}$.

![Figure 3. The electrical circuit of the improved CSA.](image-url)
The dependences characterizing the noise level and the fast response of the improved CSA in comparison with the original one are shown in figures 4, 5.

![Figure 4. Dependence of the time of the rising edge $\tau$ on the sensor capacitance $C_D$: 1- circuit of figure 1 at $C_F = 1$ pF, 2- circuit of figure 3 at $C_F = 1$ pF, 3- circuit of figure 3 at $C_F = 5$ pF.](image)

As can be seen from figure 5, the improved circuit at $C_F = 1$ pF has a significantly lower ENC compared to the original circuit with a sensor capacitance in the range from 10 pF to 1 nF. At the same time, at $C_F = 1$ pF, the improved circuit is characterized by the longer time of the rising edge for $C_D < 200$ pF, which is explained by the almost 9-fold increased capacity of $C_{STR}$ and $C_{INP}$. If it is necessary to significantly increase the fast response of the improved circuit, the increase in $C_F$ to 5 pF is recommended (curve 3 in figure 4), although the ENC increases. Thus, the increase in $C_F$ from 1 pF to 5 pF at $C_D = 500$ pF leads to the decrease in $\tau$ by a factor of 6.2 and the increase in the ENC by a factor of 2.5.

For a specific sensor capacitance, it is necessary to look for a compromise combination of the ENC and $\tau$ obtained by choosing $C_F$.

4. Conclusion
On the base of analytical expressions and analysis of well-known circuit solutions, a technique has been developed to reduce the noise of integrated Bi-JFETs of the high-speed CSA with the input JFET. The application of the technique made possible to develop a high speed low-noise CSA at the array chip MH2XA030 designed to operate with sensors with an internal capacitance of about 500 pF.

The developed CSA can be used to create ICs for signal processing semiconducting particle detectors and ionizing radiation on the array chip MH2XA030.

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