Optimization of Capacitor Voltage Control Strategy for MMC Sub-module

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Abstract. Modular Multilevel Converter (MMC) is widely studied and used because of its own advantages such as high output level number, low switching frequency and good waveform quality. The voltage equalization problem of sub-module capacitors is one of the key research directions of MMC. In the paper, a sorting method of inter-group comparison in two groups, called OF sorting method, is proposed first. The maximum time complexity of this method of sorting is N-1, but the use of this method is limited. Therefore, a new MMC hybrid sorting voltage equalization algorithm is proposed on this basis. This paper proposes a capacitor voltage equalization control strategy based on the combination of improved equalization sorting algorithm and improved insertion sorting algorithm, which reduces the computational effort by monitoring the sub-module capacitance voltage in real time, setting the dispersion index between sub-module voltages, and then controlling the opening and holding of the sorting module to reduce the number of elements to be ranked one by one. Finally, the MMC model is built in Matlab/Simulink. The simulation results show that the improved equalization control strategy can effectively reduce the computational effort and reduce the switching frequency of sub-modules on the basis of better maintaining the capacitor voltage balance.

Keywords: Modular multilevel converter, improved equalization sorting algorithm, improved insertion sorting algorithm, capacitor voltage equalization.

1. Introduction

The rapid development of controlled power electronic components has made the research on voltage-sourced converters (VSC) more and more in-depth. Modular multilevel converter (MMC) is a new type of voltage variation circuit, which can output higher voltage by cascading multiple sub-modules, with the advantages of low switching frequency, small voltage harmonics, and easy modular design. Therefore, MMC technology has wide application prospects in power systems [1-2]. In the paper, a capacitor equalization control strategy based on the combination of improved equalization sorting algorithm and improved insertion sorting algorithm is proposed. The improved sorting algorithm is based on the algorithm itself and the introduction of threshold and upper and lower limits of capacitor voltage, and on the basis of satisfying the equalization of capacitor voltage of sub-modules, the difference of capacitor voltage between modules is reflected by setting a dispersion degree, and the change of dispersion degree index is used to decide the sorting module start and stop, so as to Finally, the MMC model is built on Matlab/Simulink to verify the effectiveness of this method.
2. MMC Topology and Working Principle

The MMC topology [3-4], shown in figure 1, is a three-phase six-bridge-arm structure, with each bridge arm consisting of the number of n identical sub-modules (SM) cascaded together and a series-connected commutation reactor L, bridge arm resistance R0 cascaded [5]. Two controllable renewal switches are connected in series with a DC storage capacitor C0 to form a sub-module, where the controllable renewal switch consists of an insulated gate bipolar thyristor with a renewal diode connected in reverse parallel.

![Figure 1. MMC topology](image)

When the MMC is working normally, the SM is in the input state or the cut-off state, and the corresponding switching devices have four switch configurations [6], as shown in table 1.

The number of input sub-modules in each phase unit must be of the number of n, and the output of different levels can be realized by adjusting the number ratio of the n sub-modules in the upper and lower bridge arms, so as to ensure the stability of the DC voltage. Therefore, the balance of the sub-module capacitor voltage is the key to maintaining the stability of the DC voltage [7].

![Figure 1. MMC topology](image)

| Statuses   | T1  | T2  | i   | U_{sm} | U_{c}    |
|------------|-----|-----|-----|--------|----------|
| Latch      | Off | Off | +   | U_{c}  | Charging |
|            |     |     | -   | 0      | Bypass   |
| Invest in  | On  | Off | +   | U_{c}  | Charging |
|            |     |     | -   | U_{c}  | Discharging |
| Cut out    | Off | On  | +   | 0      | Bypass   |
|            |     |     | -   | 0      | Bypass   |

3. Improved Sub-module Capacitor Voltage Equalization Method

3.1 Sub-module Capacitor Voltage Equalization Control Strategy Based on the Combination of Improved Equalization Sorting Algorithm and Improved Insertion Sorting Algorithm

The paper proposes a sorting algorithm that combines an improved balanced fast sort and an improved insertion sort and introduces thresholds and upper and lower voltage limits to control them, reducing the amount of sorting calculations without changing the sorting result and making it also a kind of voltage fluctuation adjustable equalization calculation, taking the upper bridge arm as an example, the
basic principle of the improved balanced sorting algorithm is as follows.

1) Real-time detection of the DC energy storage capacitor voltage of each sub-module, and real-time storage.

2) Real-time detection of the direction of the bridge arm current, and real-time storage, as a basis for judging capacitor charging and discharging.

3) The number of sub-modules in the input state \( n_{py} \) and the number of sub-modules in the removal state \( n_{pw} \) in the last step of the long upper bridge arm are detected respectively, the number of sub-modules in the input state \( n_{ny} \) and the number of sub-modules in the removal state \( n_{nw} \) in the lower bridge arm are detected.

4) Calculate the change in the number of input sub-modules according to the number of sub-modules that need to be input \( n_{up} \) (the lower bridge arm is \( n_{down} \)) issued by the valve control, and the calculation formula is upper bridge arm \( m = n_{up} - n_{py} \) (lower bridge arm is \( m = n_{down} - n_{ny} \)).

5) According to the sub-module voltage instantaneous value, the upper and lower bridge arms have been put into the sub-module and the sub-module not put into the OF sorting method for sorting, forming \( X_{py}, X_{pw}, X_{ny}, X_{nw} \) and calculating the capacitor voltage average value \( U_n \), the part of the capacitor voltage value greater than \( U_n \) keeps the original trigger pulse, and the difference between the capacitor voltage instantaneous value and the average value is \( \Delta U_2 \).

6) According to the direction of the inflow current \( I_p (I_n) \) and whether \( m \) is greater than zero, the following four sequences are generated:

1) If \( m=0 \), it means that the current and last time output the same level, judge whether the voltage of the sub-module at this time is out of limit, cut off the sub-module that is out of limit and put in the sub-module with the lowest voltage.

2) \( m>0 \), put in the sub-modules with the largest \( \Delta U_2 \) from the sub-modules in the cut-off state, and the over-limit module is cut off. The sub-module with the lowest input voltage, insert and sort the \( k \) sub-module capacitor voltage instantaneous values larger than \( U_n \) in \( X_{py}(X_{ny}) \) with the sub-modules input later to form the sequence \( X_{p gin}(X_{n gin}) \);

3) \( m>0 \), \( I_p(I_n)\geq 0 \), put in the \( (n_{up} - n_{py}) \) sub-modules with the smallest \( \Delta U_2 \) from the sub-modules in the cut-off state, cut the over-limit module, and put in the submodule with the highest voltage, set \( X_{py}(X_{ny}) \) to be larger than \( U_n \). The instantaneous value of the capacitor voltage of the \( k \) sub-modules is inserted and sorted with the subsequent sub-modules to form a sequence \( X_{p din}(X_{nd in}) \);

4) \( m<0 \), \( I_p(I_n)\geq 0 \), excise the \( (n_{py} - n_{up}) \) submodule with the largest \( \Delta U_2 \) from the submodule in the input state, excise the overrun module, input the submodule with the lowest voltage, and sort \( X_{py}(X_{ny}) \) by insertion to form the sequence \( X_{p dout}(X_{nd out}) \);

5) \( m<0 \), \( I_p(I_n)\leq 0 \), excise the \( (n_{py} - n_{up}) \) sub-modules with the smallest \( \Delta U_2 \) from the sub-modules in the input state, cut the over-limit module, and input the submodule with the highest voltage, and sort \( X_{py}(X_{ny}) \) by insertion to form the sequence \( X_{p dout}(X_{nd out}) \);

7) Select the sub-modules to be put in or removed from the sequence formed by step (6); if there exists one of \( n_{py} \) and \( n_{pw} \) equal to zero or one of \( n_{ny} \) and \( n_{nw} \) equal to zero, the following special processing steps are performed.

1) When \( n_{py} \) or \( n_{ny} \) is equal to zero, the \( m \) sub-modules with the smallest \( \Delta U_2 \) are selected for input when charging; the \( m \) sub-modules with the largest \( \Delta U_2 \) are selected for input when discharging.

2) When \( n_{pw} \) or \( n_{nw} \) is equal to zero, the \( m \) sub-modules with the largest \( \Delta U_2 \) are selected for removal during charging; the \( m \) sub-modules with the smallest \( \Delta U_2 \) are selected for removal during discharging.
3.2. Improved Insertion Sort Algorithm

The time complexity of the traditional insertion sort algorithm is $n^2$, which is no different from the bubble sort, but the insertion sort algorithm is more flexible, and the improvement of the insertion sort algorithm in the text is shown below (the above bridge arm $m>0$, $I_p\geq0$ as an example)

1) According to the detected $n_{py}$ and $n_{pw}$, use the quick sort algorithm to generate $X_{py}$ and $X_{pw}$;

2) According to the value of $m$, take the instantaneous value of the capacitance voltage of the sub-module $m+1$ in $X_{pw}(X_{nw})$. According to $U_{m+1}$ in $X_{pw}$, obtain the k ratios in $X_{py}$ $U_{m+1}$. For large elements, generate an ordered sequence $X_{py,-1}$, and at the same time generate an ordered sequence $X_{pw,-1}$ consisting of the remaining $(n_{py} - m)$ elements in $X_{py}$;

3) Compare the size of $k$ and $n_{pw,-1}$ ($n_{pw,-1}=n_{py}-m$):
   1) When $k\geq n_{pw,-1}$:
      Step 1: If the smallest element in $X_{pw,-1}$ is larger than the largest element in $X_{py,-1}$, directly add $X_{pw,-1}$ to the rightmost of $X_{py,-1}$; if the largest element in $X_{pw,-1}$ is smaller than the smallest element in $X_{py,-1}$, add $X_{pw,-1}$ directly to the leftmost side of $X_{py,-1}$. Otherwise, proceed as follows;
      Step 2: Extract the first element in $X_{pw,-1}$ and insert it into $X_{py,-1}$. At this time, this element and elements smaller than this element in $X_{py,-1}$ will not participate in the next comparison;
      Step 3: Extract the last element in $X_{pw,-1}$ and insert it into $X_{py,-1}$. At this time, this element and the elements larger than this element in $X_{py,-1}$ will not participate in the next comparison;
      Step 4: Repeat steps 2 and 3 until the number of elements in $X_{pw,-1}$ is zero, at this time an ordered sequence $X_{pgin}$ is generated.

   2) When $k<n_{pw,-1}$:
      Step 1: If the smallest element in $X_{py,-1}$ is larger than the largest element in $X_{pw,-1}$, directly add $X_{py,-1}$ to the rightmost of $X_{pw,-1}$; if the largest element in $X_{py,-1}$ is smaller than the smallest element in $X_{pw,-1}$, add $X_{py,-1}$ to $X_{pw,-1}$ directly the far left. Otherwise, proceed as follows;
      Step 2: Extract the first element in $X_{py,-1}$ and insert it into $X_{pw,-1}$. At this time, this element and elements smaller than this element in $X_{pw,-1}$ will not participate in the next comparison;
      Step 3: Extract the last element in $X_{py,-1}$ and insert it into $X_{pw,-1}$. At this time, this element and the element larger than this element in $X_{pw,-1}$ will not participate in the next comparison;
      Step 4: Repeat steps 2 and 3 until the number of elements in $X_{py,-1}$ is zero, and then an ordered sequence $X_{pgin}$ is generated.

4. Simulation Analysis

To verify the correctness of the optimized voltage equalization algorithm in this article, the MMC model is built in the MATLAB/Simulink simulation environment, the level number is 11.

Figure 2 shows the phase currents of the three phases A, B, and C and the current on the DC side. Figure 3 shows the simulation diagram of the bridge arm capacitor voltage using the traditional sorting algorithm. Figure 4 shows the combination of the improved balanced sorting algorithm and the improved insertion sorting algorithm. The simulation diagram of the bridge arm capacitor voltage of the sub-module capacitor voltage equalization control strategy can be seen from the two diagrams that the two methods have the same effect on voltage equalization. Although the improved sorting method produces weak interference to its waveform, the quality of the output waveform is good and the deviation of the fluctuation amplitude is small. The optimized sorting algorithm greatly reduces the switching frequency of the sub-modules, and the DC side current is also stable at about 200A, which is relatively stable.
Figure 2. A-phase current, B-phase current, C-phase current, DC side current.

Figure 3. Bridge arm capacitor voltage using traditional sorting algorithm.

Figure 4. The voltage of the upper and lower bridge arms under the control of the improved algorithm.

5. Conclusion

In this paper, the MMC-HVDC sub-module capacitor voltage equalization method is deeply studied, and a sub-module capacitor voltage equalization control strategy based on the combination of the improved equalization sorting algorithm and the improved insertion sorting algorithm for multiple modules is proposed. This method effectively reduces the switching frequency of the sub-modules by setting the dispersion threshold, thereby reducing the system loss and improving the operation speed of the controller. A single-ended 11-level MMC model is built in Matlab/Simulink, and the traditional capacitor voltage equalization control strategy is improved. The capacitor voltage control strategy is compared. The simulation results show that the improved capacitor voltage equalization control strategy guarantees the voltage equalization effect. At the same time, the MMC system characteristics and effects are basically the same and have little impact on the operating characteristics of the HVDC system. Engineering practical value.
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