Design and implementation of an analog signal isolation conditioning circuit

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Abstract. In control systems, external analog signals need to be converted into digital signals. When sampling external input analog signals, such as voltage or current, it is necessary to process the small analog signal amplification or large signal reduction to the digital signal that can be sampled normally by the ADC; at the same time, the complexity of the external environment will affect the accuracy of sampling, and the input and output isolation processing needs to be carried out. Therefore, in order to solve the problem of low sampling accuracy of analog signal ADC in complex environment, this paper proposes an analog signal isolation conditioning circuit, which can filter out the high-frequency noise in the input signal without affecting the rapid sampling of the ADC, and use two-stage operation amplification to perform gain and zero compensation processing, so that the conditioned signal has high accuracy, good linearity, and strong anti-interference ability, which meets the design requirements. Through functional and stress tests, the functional correctness and performance stability of the analog signal isolation conditioning circuit proposed in this paper are verified.

1. Introduction
In the current control system, the need to convert the external input analog signal into a digital signal that the system can recognize for ADC sampling, the accuracy of the conditioning signal puts forward strict requirements for the design of the circuit itself, such as in the amplification or reduction of the analog signal, citing the operational amplifier, the need to process and compensate for the operational amplifier's own characteristics (such as its offset voltage, bias current and other parameters) on the signal impact; the complexity of the external input environment also requires the signal conditioning circuit to be strongly anti-interference ability \cite{1-5}.

Therefore, in order to improve the poor signal conditioning accuracy and weak ability to resist external environmental interference, this paper designs an analog signal isolation conditioning circuit.

2. System solution
An analog signal isolation conditioning circuit designed in this paper uses the AD202 isolation operational amplifier. The AD202 is general purpose, two-port, transformer-coupled isolation amplifier that may be used in a broad range of applications where input signals must be measured, processed, and/or transmitted without a galvanic connection. The AD202 provides total galvanic isolation between the input and output stages of the isolation amplifier through the use of internal transformer-coupling. The functionally complete AD202 eliminates the need for an external, user-supplied dc-to-dc converter. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs.
This analog signal isolation conditioning circuit implements the function of amplifying the analog small signal of the input or reducing the large signal to the ADC that can be sampled normally. A block diagram of the signal isolation conditioning circuit is shown in Figure 1.

3. Isolation conditioning circuit hardware design research

3.1. Power Supply Design

The main circuit of the isolation conditioning circuit is powered by a single supply +12V DC, and the internal voltage is realized by DC/DC conversion, and the internal power supply mainly includes: 15V1, 15V, -15V, REFH, REFLL. The conditioning circuit requires a 15V power supply to power the isolated op amp and inverting op amp, in order to maintain the consistency of the positive and negative voltage supply loads of the DC/DC power module, the 15V of the isolated op amp is powered by a separate DC/DC power supply. The principle of the isolation conditioning circuit power supply circuit is shown in Figure 2.

Figure 2. The principle of the power supply circuit of the isolation conditioning circuit.

3.2. Scale down circuit design

Taking the DC 20V conditioning signal as an example, the precision resistance of 30KΩ and 10KΩ (one-in-ten-thousandth accuracy) is used to realize a proportional resistance network of about 1:4, so that the signal voltage after the input signal passes through the resistor network is 5V. As shown in Figure 3, the input impedance of the input signal is 40KΩ.
Since the input signal introduces noise coupling at all stages of transmission and processing, it needs to be filtered by an RC filter circuit. For DC signals, the lower the cutoff frequency of the RC filter circuit, the better, but a lower cutoff frequency will inevitably lead to a large time delay in the output signal, resulting in excessive deviation of the output during the rapid recovery of each channel. Therefore, the RC parameters in the RC filter circuit need to be carefully selected. In this design, for the RC filter circuit of the signal conditioning channel, the resistor $R_3$ is selected 20KΩ, the capacitor $C_1$ is selected 1nF, and the cutoff frequency is calculated according to the cutoff frequency and time constant calculation formula, and the cutoff frequency is about 8KHz, and the delay time is 100us (5RC) ($V_{out}=0.99V_{in}$) When the charging is basically completed. This design filters out high-frequency noise in the input signal without affecting the fast sampling of the AD module.

Resistor $R_1$ selects 0Ω, $R_2$ selects 250Ω, $R_3$ selects 10KΩ, which can realize microcurrent signal conditioning, that is, 0~20mA current conditioning into 0~5V voltage signal. It is worth noting that the transition voltage cannot exceed the rail voltage of the op amp chip.

### 3.3. Isolated op amp circuit design

The isolated op amp circuit uses an isolated op amp, model AD202, which can effectively isolate input and output signals. The AD202 chip internally isolates its power supply, saving an isolated DC/DC power supply. Isolated op amp circuit if the noninverting op amp gain is selected,

$$V_{out}=V_{in}(1+R_F/R);$$

Here the Gain is greater than 1, that is, the output value of the op amp can only be greater than the input value, and it cannot be adjusted to a smaller extent, so the isolated op amp circuit inverting op amp is used

$$V_{out}=-V_{in} R_F/R;$$

The Gain size is adjustable; RF is the feedback resistor and R is the input resistor.

The op amp itself will have an offset voltage, that is, when the dropout voltage across the input is 0, the output will still have an offset voltage. This offset voltage is amplified by the effect of the secondary op amp, affecting the true data accuracy, so the circuit needs to be zeroed. In order to ensure the stability of zeroing, it is necessary to ensure the stability of the reference voltage and the accuracy to meet the requirements, and the AD688 chip is selected to provide the reference level REFH and REFL. At the same time, keep the resistance in series with input LO below a few hundred ohms to avoid CMR degradation.
3.4. Inverting op amp circuit design

The signal output through the isolated op amp circuit is negative, so to obtain the desired level signal, a 1:1 ratio of inverting op amp is required. The AD202 isolated op amp has a maximum output capability of 400uA, so the R4 can be selected as minimum as 12.5KΩ. If it is less than 12.5KΩ, the AD202 has insufficient driving force and the output cannot be adjusted to the maximum value. The role of R5 is to balance the offset voltage value at the op amp input due to the bias current.

![Inverting op amp circuit design](image)

Figure 5 Analog signal isolation conditioning circuit inverting op amp circuit

4. Circuit simulation

As shown in Figure 1, the hardware circuit is simulated using the NI Multisim simulation tool. The simulation results are shown in Table 1.

| Serial number | V_In (V) | V_Out (V) | V_Expect (V) | Precision (%) | I_In (mA) | V_Out (V) | V_Expect (V) | Precision (%) |
|---------------|----------|-----------|--------------|---------------|-----------|-----------|--------------|---------------|
| 1             | 1        | 0.24991   | 0.25         | 0.36          | 0.5       | 0.12492   | 0.125        | 0.64          |
| 2             | 2        | 0.49989   | 0.5          | 0.22          | 1         | 0.24989   | 0.25         | 0.44          |
| 3             | 4        | 0.99989   | 1            | 0.11          | 2         | 0.49989   | 0.5          | 0.22          |
| 4             | 6        | 1.50015   | 1.5          | 0.063         | 5         | 1.24991   | 1.25         | 0.072         |
| 5             | 7        | 1.74989   | 1.75         | 0.045         | 6         | 1.49982   | 1.5          | 0.12          |
| 6             | 8        | 1.99991   | 2            | 0.049         | 7         | 1.74992   | 1.75         | 0.046         |
| 7             | 9        | 2.24989   | 2.25         | 0.032         | 8         | 2.00013   | 2            | 0.065         |
| 8             | 10       | 2.49992   | 2.5          | 0.03          | 10        | 2.49992   | 2.5          | 0.032         |
| 9             | 12       | 3.00011   | 3            | 0.037         | 9         | 2.24985   | 2.25         | 0.067         |
| 10            | 14       | 3.50029   | 3.5          | 0.083         | 10        | 2.49992   | 2.5          | 0.032         |
| 11            | 15       | 3.74992   | 3.75         | 0.021         | 11        | 2.74989   | 2.75         | 0.04          |
| 12            | 16       | 4.00012   | 4            | 0.03          | 13        | 3.24990   | 3.25         | 0.031         |
| 13            | 17       | 4.25009   | 4.25         | 0.021         | 14        | 3.50021   | 3.5          | 0.06          |
| 14            | 18       | 4.49987   | 4.5          | 0.029         | 16        | 3.99992   | 4            | 0.02          |
| 15            | 19       | 4.75022   | 4.75         | 0.046         | 18        | 4.50019   | 4.5          | 0.042         |
| 16            | 20       | 4.99991   | 5            | 0.018         | 20        | 5.00021   | 5            | 0.042         |

5. Hardware testing

Build the hardware circuit and conduct a physical test, and the results are shown in Table 2.

| Serial number | V_In (V) | V_Out (V) | V_Expect (V) | Precision (%) | I_In (mA) | V_Out (V) | V_Expect (V) | Precision (%) |
|---------------|----------|-----------|--------------|---------------|-----------|-----------|--------------|---------------|
| 1             | 1        | 0.2499    | 0.25         | 0.4           | 0.5       | 0.1249    | 0.125        | 0.8           |
| 2             | 2        | 0.4997    | 0.5          | 0.6           | 1         | 0.2498    | 0.25         | 0.8           |
| 3             | 4        | 0.9995    | 1            | 0.5           | 2         | 0.4998    | 0.5          | 0.4           |
Comparing the test results of Table 1 and Table 2, due to the influence of the characteristics, accuracy and measurement of the multimeter scale of the conditioning circuit device itself, the test results of the actual circuit are slightly worse than the data simulation results. However, the processing error and linearity of an analog signal isolation conditioning circuit designed in this paper can still meet the ADC sampling requirements.

6. Conclusion
In this paper, an analog signal isolation conditioning circuit is designed and implemented, which realizes the digital signal function of analog small signal amplification or large signal reduction to ADC that can be sampled normally, and the error can be controlled below 0.8‰. The analog signal isolation conditioning circuit has high conditioning accuracy, good linearity, strong anti-interference ability, and stable and reliable performance.

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