Multiple switching pattern for a modified reduce switch multilevel inverter: A comparison analysis

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Abstract: A primary concern of multilevel inverter is its capability to produce desired alternating voltage close to sinusoidal at the output, using multiple sources of DC voltage input. Mostly a multilevel inverter is used to generate the AC voltage from DC voltage. The aim of this paper is to investigate the output of 9 level multilevel inverter by modifying the conventional 5 levels H-bridge cascade multilevel inverter. The proposed design intending to reduce the number of switches from 16 switches to 10 switches. Implementation of different switching pattern methods; equal phase (EP), half equal phase (HEP), half height (HH) and feed forward (FF) and the related expression are presented in this paper. In the result section shows a different percentage of total harmonic distortion achieved. Out of all 4 methods, HH method suppressed distortion wave the most and resulted in the lowest THD in the proposed inverter. This paper shows that by reducing the number of switches in multilevel inverter structure maintains the same quality output as the conventional H-bridge topology. Furthermore, the manipulation of the switches firing angle contribute in decreasing the system THD.

1. Introduction

Inverter is a power electronic device that can convert the DC voltage into AC voltage. There are three types of inverter output which is square wave inverters, modified sine wave inverters and also pure sine wave inverters[1–3]. Multilevel inverter is a step level output inverter which the higher the level made the output near to sinusoidal waveform. This inverter usually comprises many switches, and switching angle’s arrangement is an important element to the circuit operation. There are many types of multilevel inverter circuits with different root topologies available. The differences between each topology are in the switching mechanism and the input voltage sources of the multilevel inverters. The most popular multilevel inverter topologies are [4–6]:

- Cascaded H-bridge multilevel inverter(CHMI)
- Diode clamped multi level inverter
- Flying capacitor multi level inverter

Multilevel inverter already gained more attention in medium voltages and in higher power application. It is well known because of its various advantages for instance, has a lower voltage stress on power switches, has lower common mode voltages, lower dv/dt ratio that leads to lower harmonic content in the output voltage and current.

In [7] found out that there are multilevel inverter topologies which can generate the quantity of output level by utilizing less amount of electronic devices. These devices, as for example, switches, driver circuit, thyristor family and direct current (DC) electrical sources that instantly decreases in establishment gap and the rate of the inverter.
This project focuses on a comparative analysis of 9 levels multilevel inverter performance. The conventional 9 level of H-bridge cascade multilevel inverter usually needs 16 switches to generate output waveform. Each switch will produce heat which will cause more power losses. The size of the circuit also increases and simultaneously increases the cost. In order to overcome these problems, the modified 5 level H-bridge cascade multilevel inverter with 10 switches is proposed. This method offered advantages to reduce the switches, give better performance, compact size inverter and less cost as the switches is significantly compressed from 16 switches to 10 switches.

The reason for analyzing the harmonic content of an inverter system is to reduce the total harmonic distortion (THD) to the lowest as possible for the output quality improvisation[8]. The best THD value is obtained using non-filter circuit. A few different angles projected from 4 switching pattern methods are compared to assess the performance of the inverter.

There is a lot of techniques have been developed to control the switching of multilevel inverter. Figure 1 summarizes the switching control technique from the basic fundamental switching until the most advance space vector PWM switching scheme. Apparently, the most popular switching techniques and most applied by the industries is PWM, as there are numbers of existing PWM-based switching control scheme[9]. Pulse Width Modulator (PWM) switching control scheme does comes with many advantages compared to the conventional multilevel fundamental switching schemes. One of the benefits when using PWM methods is that it employs much higher switching frequencies that concern harmonics. The harmonics filtering exercises is much cheaper and easier due to the unwanted harmonics occurred at much higher switching frequencies. And, the production of the harmonics could be over the bandwidth for some actual system. It means that there is no power dissipation due to harmonics. Aside from that, harmonics of multilevel fundamental switching schemes is created at lower switching frequency and it increases the complexities of the activity of filtering.

Multilevel inverter’s parameter output qualities, such as a reduction of harmonic and switching losses usually depend on the modulation strategies that applied to the inverters. Some control modulation and techniques has been developed for this multilevel inverter. Figure 1 showed the control techniques for the multilevel inverter can be classified into Selective Harmonic Elimination PWM (SHEPWM), Pulse Width Modulation (PWM) and Optimized Harmonics Steps Waveform (OHSW). For the Pulse width modulation PWM, it can be classified to open loop and closed loop[10,11].Previous implementation of SHEPWM is presented in [12].
Harmonic optimization of multilevel inverter using particle swarm optimization (PSO) is a popular discussion as stated in [13], as precision in this computational algorithm made it known as feasible solution to solve transcendental equation by producing sets of switching angle for better harmonic performance.

Switching angle is the firing angle of power device in the moment of voltage step up from one level to another. For one complete cycle of voltage output consist of symmetrical quadrant of positive cycle, \(0 \leq \theta \leq 90^\circ\) and \(90 \leq \theta \leq 180^\circ\), then a vertical flip mirrored waveform in negative cycle for the 3rd and 4th quadrant \(180^\circ \leq \theta \leq 270^\circ\) and \(270^\circ \leq \theta \leq 360^\circ\). Thus, this repetitive magnitude level can be simplified and represented by the first quadrant for each angle projection calculation and subsequent quadrant will follow the same value in appropriate mirrored level magnitude[14]. In this project different set of switching patterns are applied and will be further elaborated in part 2.

2. Modified reduce switch multilevel inverter topology

The proposed multilevel inverter structure is a modified cascade H-bridge multilevel inverter. Figure 2 shows the 5-level reduce switch multilevel inverter with 2 DC voltage sources with a basic switching angle in table 1. Table 2 demonstrates the switching operation of 5-level reduce switch multilevel inverter. This structure is further extended in cascade connection to achieve the 9-level output as desired. Figure 3 shows the subjected structure.

![Figure 2: 5-level reduce switch multilevel inverter](image)

| Switch | Switching Angle |
|--------|-----------------|
| G1     | 0°, 180°        |
| G2     | \(\theta, 180^\circ-\theta, 180^\circ, 180^\circ+\theta, 360^\circ-\theta\) |
| G3     | 0°, \(\theta, 180^\circ-\theta, 180^\circ, 180^\circ+\theta, 360^\circ-\theta\) |
| G4     | 180°, 360°      |
| G5     | \(\theta, 180^\circ-\theta, 180^\circ+\theta, 360^\circ-\theta\) |

| Operation | \(D_f\) | S1 | S2 | S3 | S4 | S5 |
|-----------|--------|----|----|----|----|----|
| 0         | 0      | 1  | 0  | 1  | 0  | 0  |
| VDC       | 1      | 1  | 1  | 0  | 0  | 0  |
| 2 VDC     | 0      | 1  | 1  | 0  | 0  | 1  |
| -VDC      | 0      | 0  | 0  | 1  | 0  | 0  |
| -2VDC     | 1      | 0  | 0  | 1  | 1  | 0  |

Table 2: Switching state for less number of switches topology MLI
3. Implementation of multiple switching patterns for harmonic analysis

Implementation of different switching methods [15] is also applied in this project to obtain an optimum switching angle. This method comprises 4 switching patterns with its associated switching by using specific differs formula in eq. (1), (2), (3) and (4):

**Equal-phase (EP) method**

$$\theta_i = i \times \frac{180^\circ}{m} \quad \text{where integer,} i = 1, 2, 3 \ldots (m - 1)/2 \quad \ldots\ldots\text{(eq.1)}$$

**Half equal phase (HEP) method**

$$\theta_i = i \times \frac{180^\circ}{(m+1)} \quad \text{where integer,} i = 1, 2, 3 \ldots (m - 1)/2 \quad \ldots\ldots\text{(eq.2)}$$

**Half height (HH) switching method**

$$\theta_i = \sin^{-1}\left(\frac{2i-1}{m-1}\right) \quad \text{where integer,} i = 1, 2, 3 \ldots (m - 1)/2 \ldots\ldots\text{(eq.3)}$$

**Feed forward (FF) method**

$$\theta_i = \frac{1}{2} \sin^{-1}\left(\frac{2i-1}{m-1}\right) \quad \text{where integer,} i = 1, 2, 3 \ldots (m - 1)/2 \ldots\ldots\text{(eq.4)}$$
4. Result Analysis
The obtained output and THD analysis of presented methods are shown in Figure 4, 5, 6 and 7.

![Figure 4: Voltage output and FFT analysis of EP method](image-url)
Figure 5: Voltage output and FFT analysis of HEP method

Figure 6: Voltage output and FFT analysis of HH method
Table 3 summarizes the percentage of total harmonic distortion by using the previously mentioned switching patterns. From the output spectrum it is clearly seen that the manipulation of switching angle in the voltage level affects the output signal characteristic. Noted that the best system performance is by HH method, in which the least THD obtained is 9.37%. This is because of better suppression of lower order harmonic spectrum by HH method which can be referred in Figure 7.

![Figure 7: Voltage output and FFT analysis of FF method](image)

Table 3: Value of THD percentage using specific formula

| Set  | THD value (%) |
|------|---------------|
| EP   | 25.65         |
| HEP  | 22.13         |
| HH   | 9.37          |
| FF   | 21.41         |

5. Conclusion

As a conclusion of this work, EP, HEP, HH and FF methods have been applied to find the optimum switching angles for a 9-level reduce switch multilevel inverter. The switching component is reduced by 6 switches as compared to the same level H-bridge cascade topology. As per visualize in part 4, the implementation of Half Height (HH) method in manipulating the switching angle successfully influenced the output voltage waveform closer to sinusoid wave characteristic compared to other three methods. The validation is done by simulation work.
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References

[1] Ahmad A, Maqbool S. Square Wave Inverters – A performance Comparison with Pure Sine wave Inverters. 2019;(April):5–8.

[2] Cheema MB, Hasnain SA, Ahsan MM, Ahmad G. Comparative Analysis of SPWM and Square Wave Output Filtration based Pure Sine Wave Inverters. 2015 IEEE 15th Int Conf Environ Electr Eng. 2015;38–42.

[3] Baroi SG, Samanta S, Banerjee S. Study of Different Types of Inverters and FFT Analysis of Output of SPWM Inverter with Change in Modulating Index and Carrier Frequency. 2017;IV(Iv):22–9.

[4] Salodkar PA. Study of Single Phase Multilevel Inverter Topologies Suitable for Photovoltaic Applications. 2017 Int Conf Energy, Commun Data Anal Soft Comput. 2017;2315–8.

[5] Bhargava V. A Comparative Modeling Analysis of Optimized Multilevel Inverter Topologies with Reduced Device Count for SPV and Wind Integration. 2019 6th Int Conf Signal Process Integr Networks. 2019;(978):1125–30.

[6] Belekar RA, Nakade RP, Chahande NM, Parchandekar PSK. Single Phase 9 level MLDCL Inverter with Half Bridge Cell Topology: Performance Analysis. 2013 Int Conf Power, Energy Control. 2013;681–5.

[7] Dhineshkumar K Subramani C. Design and Implementation of nine level multilevel Inverter. 2018;

[8] Dash PSS. Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques. 2011;4(March 2010):951–8.

[9] Balamurugan CR. Prediction of a New Cascaded Hybrid Multilevel Inverter with Less Device Count. 2016;(February):273–81.

[10] Colak I, Kabalci E, Bayindir R. Review of multilevel voltage source inverter topologies and control schemes. Energy Convers Manag. 2011;52(2):1114–28.

[11] Kouro S, Malinowski M, Member S, Gopakumar K, Member S, Pou J, et al. Recent Advances and Industrial Applications of Multilevel Converters. 2010;57(8):2553–80.

[12] Ismail B AMH and ST. FPGA based implementation of selective harmonic elimination PWM for cascade inverter. Int Rev Model Simulations. 2012;5(5):1919–26.

[13] Ismail B, Hassan SIS, Ismail RC, Azmi A, Arshad MH. Elimination of lower order harmonics in multilevel cascaded inverters with equal DC sources using PSO. Int Rev Model Simulations. 2014;7(4):554–60.
[14] Reddy NRS. Performance Analysis of a Multilevel Inverter Topology with Reduced Switches. 2015 Int Conf Comput Commun Control. 2015;1–5.

[15] Jalakanuru NR, Kiber MY. Switching Angle Calculation By EP , HEP , HH And FF Methods For Modified 11-Level Cascade H-Bridge Multilevel Inverter. 2017;6(12):69–75.