Design of High Performance ALU Using Vedic Mathematics

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Abstract. This article proposes a Vedic multiplier-based design of multiply and accumulate unit by employing UrdhvaTiryagbhyam Sutra. Further, it implements an efficacious ALU with 32-bit architecture. Simulation analysis disclosed the comparison of proposed 32-bit ALU with existing architectures. In addition, complexity in hardware, area and delay reduction demonstrated that proposed 32-bit ALU is more efficient over conventional architectures.

Keywords: Vedic Mathematics, UrdhvaTriyakbhyam Sutra, Vedic multiplier, ALU, Conventional architectures.

1. Introduction
A conventional multiplier, adder and aggregator form the general ALU. Where a collector applies the yield to the previous ALU yield. As part of chip and computerised flag processors, the Multiply Accumulate (ALU) unit is commonly used for application of data acquisition, for example separating, transforming and in siding items. For example, discrete cosine changes (DCT) or discrete wavelet changes (DWT) or FFT / IFFT measurements, which can be enhanced by dedicated ALU units, are used in the main for computerised flag planning techniques. Most of them are nonlinear. As the monotone use of duplication and expansion makes them proficient, the speed of increase and expansion determines how rapidly the entire calculation is performed or exercised. The multiplier, since the deferral between the fundamental operating squares is characteristic long in computerised systems, determines the simple route. Duplicate and multiply (ALU) unit configuration using the Urdhva-tiryagbhyam Sutra multiplier. The paper emphasises a professional 32-bit ALU system in combination with 16-bit type and findings are seen in standard structural tests. The productivity as far as zone and speed of proposed ALU unit engineering is seen through lessened zone, low basic deferral and low equipment unpredictability. The suggested unit ALU decreases the area by using MUX as a multiplier using two multipliers. The improvement in task speeds is obtained by the distinct degressive existence of the Vedic multiplier unit, rather than four multipliers and by reducing the quantity of multipliers and units The proposed ALU device will be upgraded to the gadget 3S100ETQ144-5 (Spartan 3) of the field programmable entry cluster (FPGA). The success of the execution.

2. Literature Review
The proposed calculation is Design of Multiplier utilising Vedic multiplier technique and its utilisation of Digital Signal processing [1].NxN multiplier configuration utilising four N/2-bit multiplier, two-bit full adder, one half adder and N/2 bit full adder to include the entirety and convey of half adder [2].16x16 exhibit of cluster Multiplier utilising Vedic multiplier this structure is various levelled plan
calculation is UrdhvaTiryakbhyam sutra on Vedic mathematics [4]. The deferral of proposed ALU unit is 43.899 ns and Conventional ALU is 55.662 ns. The traditional and proposed ALU unit is coded on Verilog-HDL and XILINX ISE simulator [5]. The recreation on Spartan-3e family utilising XILINX ISE device and coding on Verilog. The after-effect of deferral is proposed multiplier is 41.562 ns and parallel multiplier is 94.087 [6].

Vedic arithmetic is the name given to the antiquated arrangement of science which was rediscovered from the Vedas [3]. It gives clarification of a few scientific terms including math, geometry, trigonometry and even analytics. It was developed by Shri Bharatikrsnatheertaji (1884-1960), after his eight long periods of research on Vedas. He built 16 primary sutras and 16 sub sutras. One strategy for increase is UrdhvaTiryakbhyam (Vertical and Crosswise) . The multiplier depends on a calculation UrdhvaTiryakbhyam (Vertical and Crosswise) of old Indian Vedic arithmetic [7]. UrdhvaTiryakbhyam sutra is general increase recipe material to all instance of duplication. Furthermore, less hardware complexity is needed in our design compared with traditional four-parallel approach [8]. UrdhvaTiryakbhyam sutra is a widespread recipes material for repetition in all situations.

In comparison to conventional 4-parallel approaches, limited hardware sophistication is required in our layout [9]. A. The primary inspiration behind Vedic math is to be able to solve complicated equations by simple means. Vedic multiplier the short equation makes them basic to use for all purposes. Urdhva-tyirgabhyam sutra is the general equation perfect for raise activities. A 2 x 2-biter Vedic multiplier should be designed as an indispensable development model for this system, as the related solution to create a 64 x 64-bit Vedic multiplier.

A 4 x 4 multiplier is outlined using a 2 x 2-bit vedic multiplier during the following period of advancement. Aide similarly to the Vedic multiplier 8 x 8! 16 x 16 and 32-bit 32-bit. A fast adder is used for the midway extension of the item for all progress phases. In today ’s computerised circuits the multiplier assumes an important part. This sutras show to cope with the doubling of the greater number (NXN bits), by splitting it down into smaller sizes. The multiplier would be based on UrdhvaTiryakbhyam (Vertical and Transversal) estimation [10].

Advantages
- Vedic multiplier is speedier than alternate multipliers.
- The zone required for vedic multiplier is little when contrasted with another multiplier design.
- ALU is utilized as a part of present-day advanced flag handling. ALU dependably lie in the basic way that decides the speed of the general equipment frameworks [11].
- Uses of replication of parallel and decimal numbers and use unsigned and visible increases in the number.

Disadvantages
- Even the frame becomes difficult with difficult duplications

3. Proposed Method
Proposed 32-bit Vedic multiplier is shown in Figure 1, where a 4-bit Vedic multiplier is utilized to design 32-bit Vedic multiplier [12]. There are four 16x16 Vedic Wallace multiplier blocks present in Figure 1, i.e., assume a = a15 to a0 and b = b15 to b0. Hence, couple of 32-bit input render to 16x16 bit multiplication. There will be total of 64-bits in output line as $S63$ to $S0$.

In this case the sutra "Urdhva-Tiryakbhyam" is used to propose such a strategy to raise two parallel figurations (Vertically and transversely) [13]. Vedic Wallace multiplier superiority is that halfway through item age and changes exist concurrently. Consequently, it is a very much adjusted parallel preparing. [14] The highlights make it more appealing for double increases. This decreases deferral and this is the essential inspiration driving this work. Schematic block diagram of arithmetic logic unit is shown in Figure 2.
3.1. Design of Arithmetic Logic Unit

ALU was supposed to conduct the mathematics and smart controller operations. The 32-bit extension, subtraction and multiplication are the number-crunching operations conducted. AND, OR, XOR, NAND, NOR, XNOR, NOT and Data Buffer are intelligent behaviours. In designing the ALU, the developers took an adaptable outline consisting of littler, but responsive barriers, some of which can be reused [2]. Specify the half-adders, the 2-bit multipliers, the Brent-Kung 4-bit multipliers, the Brent-Kung 8-bit adder, the 8-bits full adder, the Brent-Kung 32-bit adder, the 32-bit full-adder multipliers, the subtractor 32-bit numbers, the legal device and the ALU 32-bit were [7].
3.2. Arithmetic Unit
A corresponding business is carried out by an Arithmetic unit: freight addition, rise and subtraction. The 4-bit Brent-Kung adding and then the 4-bit multiplier were used with a half adder. • 4-bit adder of Brent-Kung to render the 8-bit adder of BrentKung. The eight-bit multiplier is rendered using the Brent-Kung adder and the four-bit multiplier. Subtractors of 8-bit. The 32-bit plug is rendered by the 16-bit plug and the 16-bit Brent-Kung plug-in. Subtractor for 32-bit. The number of multiplexer jugglers is identified [15].

3.3. Logical Unit
The execution of logical circuits was dissected by using the widely used logical doors and a multiplexer for detailing the permissible unit. A logic device performs multiple functions, such as Logical AND, OR, XOR, NOT, NAND, NOR, XNOR etc. In lieu of this numerical and coherent unit juggling unit, it has been consolidated into mathematical justification units. The ALU-Logical Unit’s output is 64 bits. Table 1 displays the ALU behaviour control term.

4. Simulation Results
The multiplier plays an important function in today’s computerised circuits. To cope with the doubling of the larger number. Figure 3 represents power consumption report of proposed method, Figure 4 represents delay (speed) report of proposed method, and Table 1 represents design summary report of proposed method. Figure 5 represents ALU output and Figure 6 depicts the RTL Schematic of proposed method respectively.

| Summary | 2.1. On-Chip Power Summary |
|---------|-----------------------------|

| On-Chip Power Summary |
|-----------------------|
| Clocks               |
| Logic                |
| Displace             |
| Top                  |
| Gatecount            |
| Total                |

| On-Chip | Power (W) | Used | Available | Utilization (%) |
|---------|-----------|-----|-----------|-----------------|
| Clocks  | 0.00      | 0   | ---       | ---             |
| Logic   | 0.00      | 678 | 1177K     | 36              |
| Displace| 0.00      | 430 | ---       | ---             |
| Top     | 0.00      | 135 | 572       | 36              |
| Gatecount| 31.52    |     |           |                 |
| Total   | 31.52     |     |           |                 |

**Figure 3:** Power report

**Figure 4:** Delay report
Table 1: Design summary

| Logic Utilization | Used | Available | Utilization |
|-------------------|------|-----------|-------------|
| Number of Sites   | 2403 | 5088      | 47%         |
| Number of 4 input LUTs | 4240 | 11785     | 36%         |
| Number of 10 input LUTs | 120 | 372       | 32%         |

Figure 5: ALU OUTPUT

Figure 6: RTL Schematic

5. Conclusion

Vedic multiplier-based implementation of multiply and accumulate unit is proposed with the employment of UrdhvaTiryagbhyam Sutra. Further, an efficacious ALU with 32-bit architecture is designed. Simulation analysis disclosed the comparison of proposed 32-bit ALU with existing architectures. In addition, complexity in hardware, area and delay reduction demonstrated that proposed 32-bit ALU is more efficient over conventional architectures.

References

[1] Sravani, Y., & Rameswarudu, E. S. IMPLEMENTATION OF ERROR DETECTABLE CSA FOR ARTIFICIAL INTELLIGENCE APPLICATIONS WITH EASY TESTABILITY.

[2] Sasamal, TrailokyaNath, Ashutosh Kumar Singh, and Anand Mohan. "Design of Arithmetic Logic Unit in QCA." In Quantum-Dot Cellular Automata Based Digital Logic Circuits: A Design Perspective, pp. 107-117. Springer, Singapore, 2020.
[3] Korkmaz, M. (2021). Energy-Efficient Transaction Scheduling in Data Systems.

[4] Costa, N., Sánchez, L., & Couso, I. (2021). Semi-Supervised Recurrent Variational Autoencoder Approach for Visual Diagnosis of Atrial Fibrillation. IEEE Access, 9, 40227-40239.

[5] Liu, R., Ramli, A. A., Zhang, H., Datta, E., & Liu, X. (2021). An Overview of Human Activity Recognition Using Wearable Sensors: Healthcare and Artificial Intelligence. arXiv preprint arXiv:2103.15990.

[6] Rath, Mrs Leena. "Ancient Vedic Multiplication Based Optimized High Speed Arithmetic Logic." International Journal of New Practices in Management and Engineering 3, no. 03 (2014): 01-06.

[7] Kaur, Navdeep, Neeru Malhotra, and Balwinder Singh. "VHDL Implementation of ALU with Built In Self Test."

[8] Nori, Suha M., and Shefa A. Dawwd. "Reduced Area and Low Power Implementation of FFT/IFFT Processor." Iraqi Journal for Electrical And Electronic Engineering 14, no. 2 (2018): 108-119.

[9] Deshmukh, V. V., & Chorage, S. S. (2021). Non-invasive determination of blood glucose level using narrowband microwave sensor. Journal of Ambient Intelligence and Humanized Computing, 1-16.

[10] Miah, M. S., Hossain, M. A., Ahmed, K. M., Rahman, M. M., & Calhan, A. (2021). An Energy Efficient Cooperative Spectrum Sensing for Cognitive Radio-Internet of Things with Interference Constraints.

[11] Kumar, V. K., & Rai, C. S. (2021). Efficient Implementation of Cryptographic Arithmetic Primitives Using Reversible Logic and Vedic Mathematics. Journal of The Institution of Engineers (India): Series B, 102(1), 59-74.

[12] Gowthami, M., Jalall, K., & Kiruthika, K. (2021, March). High Speed and Performance analysis of Multiplier in Field Programming Gate Array. In IOP Conference Series: Materials Science and Engineering (Vol. 1084, No. 1, p. 012062). IOP Publishing.

[13] Rohith, S., Babu, K. R., & Chandrashekar, M. N. FPGA Implementation of 8-Bit Vedic Multiplier for DIT-FFT Application Using Urdhva Tiryagbhyaam Sutra.

[14] Harish, B., Rukmini, M. S. S., & Sivani, K. (2021). Design of MAC unit for digital filters in signal processing and communication. International Journal of Speech Technology, 1-5.

[15] Gowreesrinivas, K. V., & Punniakodi, S. (2021). Improvised hierarchy of Floating Point Multiplication using 5: 3 Compressor. International Journal of Electronics Letters.