Design and analysis of a novel AC-side power decoupling circuit

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Abstract
A large amount of second (2\omega) ripple power are coupled on the DC bus of a single-phase inverter due to the output pulsating power. In this paper, a novel AC-side power decoupling circuit (APDC) based on buck-boost is proposed for a single-phase inverter. The circuit is connected in parallel with the AC side of the inverter to realise the local decoupling of the pulsating power on the AC side. The working principle of APDC is elaborated and the switching sequence of APDC is derived. The corresponding pulse energy modulation (PEM) control strategy is designed to precisely control the decoupled power. The feasibility and superiority of the proposed APDC together with the PEM control strategy are finally verified by both the simulation and experimental results obtained on a 200 W single-phase inverter. The results show that 2\omega-ripple power of the system can be effectively buffered and the capacitor capacity in the inverter system is greatly reduced.

1 | INTRODUCTION

The two-stage single-phase inverter is composed of the front-end DC/DC converter and the backward DC/AC converter, which is widely used in photovoltaic (PV) system, fuel cell generator, marine power system, UPS and other distribution systems. A pulsating instantaneous power exits on the AC side of a single-phase AC load as produced by the sinusoidal voltage and current. The pulsating power creates a 2\omega-ripple on DC voltage or current. In the fuel cell and DC microgrid system, the 2\omega-ripple current will reduce their lifetime and efficiency. The traditional solution is to connect large electrolytic capacitors (E-caps) on the DC bus to absorb the 2\omega-ripple power. In this way, the E-caps containing 2\omega-ripple voltage will shorten the lifetime and reduce the reliability of the system. Therefore, it is significant to reduce the influence of the 2\omega-ripple power in a single-phase inverter.

Therefore, several research works have been carried out and some different solutions are put forward in recent years. In general, they can be divided into two categories. One is to optimise the decoupling control strategy in the present two-stage inverters. The other is to propose a novel inverter topology. With regard to control strategy, reference [1] proposes that increasing the voltage loop gain of the front-end DC–DC converter at 2\omega could reduce 2\omega-ripple current. To satisfy this requirement, proportion integration (PI) regulator plus inductor current feedback is employed to achieve the high bandwidth of the voltage loop. In [2], a control strategy is presented based on the front-end load current feedforward. It intends to control the DC bus voltage to swing properly, making the DC bus capacitor supply all the pulsating power nearly. In [3], a basic approach is proposed from the perspective of the output impedance. It indicates that the output impedance of the front-end DC–DC converter should be designed relatively high at twice the output voltage frequency (2\omega) while relatively low at other frequencies. In [4], a closed-form solution is derived to calculate the amplitude of the ripple-caused harmonics. In [5], an observer-pattern modelling method is proposed to eliminate the time-variance effect from both fundamental components in the load-stage and 2\omega-ripple in the source-stage. In [6], an adaptive sliding mode control strategy for a two-stage converter to reduce 2\omega-ripple is proposed. Adopting the above control methods, 2\omega-ripple current in the front-end DC/DC system can be properly suppressed. However, the 2\omega-ripple power is introduced into large E-caps on DC bus, so the value of E-caps is still quite large. When the value of E-caps increases to a certain value, the ability to absorb 2\omega-ripple power is limited. In addition, large E-caps have some inherent disadvantages, such as short life, large volume [7–10], and so on. Using film capacitors to absorb 2\omega-ripple power has become a hot topic.

The second scheme is to reform traditional two-stage inverters. The DC/DC converter adopts a high-frequency (HF)
transformer, which has the advantages of input-side and output-side being electrical isolation. In [11], a three-port PV micro-inverter is proposed with the strategy of current decoupling instead of power decoupling. In this way, the current decoupling tank can buffer the current difference between the PV panel and the AC grid current. On the basis of a conventional flyback inverter, a modified micro-inverter [12] is derived by incorporating another transformer winding and a power decoupling circuit. This three-switch inverter can extract maximum power from PVs deliver a sinusoidal current to the grid, and compensate for the unbalanced power. In [13, 14], a conventional four-switch flyback-based inverter is turned into an inverter equipped with a series power decoupling circuit. The modified inverter has an inherent snubber circuit, which can restore the energy of the transformer leakage inductance and improves its overall efficiency. These two-stage inverters can step up the voltage using a transformer. In this way, the system needs to use the transformer. However, it is more advantageous to eliminate the transformer because this would reduce the production cost and size and increase power efficiency. Therefore, two-stage transformerless inverters have become a typical object of study as a grid-connected inverter circuit configuration [15].

The DC/AC topology containing decoupling ability has always been a research hotspot. Single-phase differential mode boost inverter [16–19] and single-phase differential mode buck inverter [8, 20] are new inverters developed in recent years. The decoupling method of differential mode power transfer is adopted. In this way, the secondary current harmonics on the DC side can be suppressed without additional switching devices. However, it imports the fourth current harmonics inevitably. Most fatally, the decoupling scheme is actually limited to low power applications.

In addition, some scholars propose active decoupling circuits to divert the pulsating power into decoupling capacitors by controlling the capacitor voltages. In [21–26], the decoupling circuit is connected in parallel with the bus capacitor, and the corresponding active damping method is proposed. Adopting these schemes, the decoupling capacitors are still large. In [27], a variety of DC-side decoupling circuits are compared, and an adaptive decoupling voltage control method is proposed to test the optimal DC-side decoupling circuit.

Based on present active power decoupling schemes, this paper studied the parallel decoupling circuit on the AC side of the inverter. By controlling the pulsating power on the AC side and realising the local decoupling of the \( 2\omega \)-ripple power on AC side, the transmission loop of \( 2\omega \)-ripple power in the system can be shortened and the energy loss on the DC side can be reduced. In addition, AC-side power decoupling circuit (APDC) and two-stage inverter are independent of each other, which reduces the complexity of the system and is conducive to the transformation of traditional inverter equipment.

In this paper, an APDC based on buck-boost mode is proposed. First, the output characteristics of the AC side of the inverter are analysed. The energy flow loop is designed when the two-stage inverter and APDC work together. The PEM control strategy [28] is used to control APDC. Finally, the Simulink simulation model of AC-side decoupling of inverter is established and a 200 W experimental platform based on TMS320F28335 controller is built. The bus capacitance of the platform is 20 \( \mu \)F. Simulation and experimental results verify the effectiveness of APDC.

### 2 POWER COUPLING RELATIONSHIP OF INVERTER

In a single-phase inverter, \( u_s(t) \) and \( i_s(t) \) are the AC voltage and current, which are given by

\[
u_s(t) = \sqrt{2}U_g \sin(\omega t)\]
\[
i_s(t) = \sqrt{2}I_g \sin(\omega t - \varphi)\]  

where \( U_g \) and \( I_g \) are the rms values of \( u_s(t) \) and \( i_s(t) \), respectively, \( \omega \) is the angular frequency, and \( \varphi \) is the phase factor angle. For pure resistive load \( R \), \( \varphi = 0 \), the instantaneous AC-side power \( P_{ac}(t) \) is given by

\[
P_{ac}(t) = u_s(t) \cdot i_s(t) = U_g I_g (1 - \cos(2\omega t))\]  

\( P_n \) is the nominal output power of the inverter, which is obtained as

\[
P_n = \int_0^T P_{ac}(t) \, dt = U_g I_g T\]  

Let \( P_d(t) = P_n - P_{ac}(t) \), whose expression is

\[
P_d(t) = U_g I_g \cos(2\omega t)\]

\( P_d(t) \) is \( 2\omega \)-ripple power of the system and also the power to be decoupled. Let \( T = \frac{2\pi}{\omega f} \) and \( f \) are the angular frequency period and frequency of \( u_s(t) \). Let \( P_d(t) = 0 \), in \( (0, T) \), we get \( t = T/8, 3T/8, 5T/8, 7T/8 \). The polarity of \( u_s(t) \) and \( P_d(t) \) is combined. One working cycle of the inverter can be divided into four modes as shown in Table 2. The Interval distribution of modes is shown in Table 3.

Figure 1 shows the distribution of modes I–IV in \( (0, T) \). The distribution of the four modes is I, II, I, III, IV and III in sequence, with the interval length ratio of 1:2:1:2:1. Modes I and III are divided into two sections in \( T \), with the interval unit...
### TABLE 1 Specifications of the different power decoupling techniques

| Reference | Decoupling capacitance | Nominal power | Efficiency | Decoupling type       |
|-----------|------------------------|---------------|------------|-----------------------|
| [1]       | 820 µF                | 1 kW          | –          | Electrolytic capacitors |
| [2]       | 1.9 mF                | 1 kW          | –          |                       |
| [3]       | 1410 µF               | 1672 W        | –          |                       |
| [11]      | 80 + 35 µF            | 100 W         | 88%        | High-frequency transformer |
| [12]      | 7 + 47 + 25 µF        | 240 W         | 83%        |                       |
| [13]      | 50 + 20 + 40 µF       | 100 W         | 91%        |                       |
| [17]      | 60 µF × 2             | 15 W          | –          | Differential mode inverter |
| [18]      | 30 µF × 2             | 100 W         | 70%        |                       |
| [19]      | 60 µF × 2             | 200 W         | 75%        |                       |
| [22]      | 40 + 50 + 40 µF       | 3 kW          | 94%        | Active decoupling circuit |
| [24]      | 50 + 100 µF           | 1 kW          | 94%        |                       |
| [26]      | 50 µF × 2 + 25 µF × 3 | 400 W         | 91%        |                       |
| Proposed scheme | 20 + 10 µF | 200 W         | 86%        | AC-side power decoupling circuit |

### TABLE 2 Four operation modes of inverter

| Voltage polarity | Power relation | Mode |
|------------------|----------------|------|
| \( n_u(t) > 0 \) | \( P_d(t) > 0 \) | Mode I |
| \( n_u(t) > 0 \) | \( P_d(t) < 0 \) | Mode II |
| \( n_u(t) < 0 \) | \( P_d(t) > 0 \) | Mode III |
| \( n_u(t) < 0 \) | \( P_d(t) < 0 \) | Mode IV |

### TABLE 3 Interval distribution of modes

| Mode    | Time domain                                      |
|---------|--------------------------------------------------|
| Mode I  | \((0\sim T/8)\) and \((3T/8\sim T/2)\)         |
| Mode II | \((T/8\sim 3T/8)\)                             |
| Mode III| \((T/2\sim 5T/8)\) and \((7T/8\sim T)\)       |
| Mode IV | \((5T/8\sim 7T/8)\)                            |

of \( T/8 \). Modes II and IV are divided into one section in \( T_i \) with the interval unit of \( T/4 \).

### 3 ANALYSIS OF APDC

#### 3.1 Topology of six-switch APDC

Figure 2 shows the system structure of the two-stage inverter. Where \( U_{\text{in}} \) and \( I_b \) are the input voltage and current of DC/DC circuit, and \( U_b \) is the voltage of bus capacitor \( C_b \). The inverter adopts a monopolar modulation strategy, whose switching period and switching frequency are \( T_i \) and \( f_s \). \( U_{\text{in}} \) and \( I_o \) are the output voltage and current before filtering.

Based on modes I–IV of the inverter, the APDC is designed, which is composed of switch \( S_1\sim S_6 \), decoupling capacitance \( C_d \) and decoupling inductance \( L_d \) as shown in the blue shadow of Figure 2. \( U_{\text{Cd}} \) is the voltage of \( C_d \) and \( i_{Ld} \) is the current flowing through \( L_d \). The switching period and frequency of APDC are \( T_i \) and \( f_s \), respectively. In \((0, T)\), APDC can also be divided into modes I–IV, corresponding to the inverter.

APDC is connected in parallel with the AC side of the inverter, which adopts \( U_{\text{inv}} \) as the input voltage to realise the local compensation of \( 2\omega \)-ripple power on the AC side. When the inverter works in modes I and III, \( P_{d}(t) > 0, P_{av}(t) > P_{av} \) the DC side delivers energy to APDC and load; when the inverter works in modes II and IV, \( P_{d}(t) < 0, P_{av}(t) > P_{av} \), the DC side and APDC deliver energy to load together. In the switching period of modes I and III, \( U_{\text{inv}} \) transfers energy to \( L_d \), then \( L_d \) transfers energy to \( C_d \) in modes II and IV, \( C_d \) transfers energy to \( L_d \), then \( L_d \) transfers energy to \( U_{\text{inv}} \). Therefore, \( L_d \) is the bridge of energy interaction between the AC side and APDC. Through the precise control of the buffer energy on \( L_d \) in the switching period, the instantaneous \( 2\omega \)-ripple power can be decoupled. The following will analyse modes I–IV of APDC.
3.1.1 Mode I

Mode I of APDC is shown in Figure 3. In mode I, \( U_{\text{inv}} > 0 \) and \( P_d > 0 \), \( S_1 \) is ON and \( S_2, S_3, S_5 \) and \( S_6 \) are OFF. \( S_4 \) is the master switch controlled by the high-frequency PWM signal. The current direction and equivalent circuit of APDC in mode I are shown in Figures 5(a) and (c). According to the ON state and OFF state of \( S_4 \), mode I can be divided into two working stages, that is, stage one and stage two.

In stage one, \( S_4 \) is ON, \( i_{L_d} \) flow path is shown by the red solid line. \( D_{11} \) is the duty cycle of \( S_1 \) and the switch-on time of \( S_4 \) is \( D_{11} T_s \). \( L_d \) stores the energy from the two-stage inverter and \( i_{L_d} \) increases linearly from zero. \( u_{Cd} \) keeps constant and \( U_{Cd0} \) is the initial voltage of \( C_d \). \( i_{L_d}(t) \) and \( u_{Cd}(t) \) can be given as Equation (5)

\[
\begin{align*}
    i_{L_d}(t) &= \frac{U_{\text{inv}}}{L_d} t, \quad (t < D_{11} T_s) \\
    u_{Cd}(t) &= U_{Cd0}
\end{align*}
\]

When \( U_{\text{inv}} > 0 \) and \( P_d > 0 \), the APDC works on mode III, which is shown in Figure 4. In this mode, \( S_2 \) is ON, \( S_3 = S_5 \) and \( S_6 \) are OFF, and \( S_4 \) is the master switch. \( C_d \) stores the energy from the two-stage inverter and \( u_{Cd} \) increases linearly from zero. \( u_{Cd} \) keeps constant and \( U_{Cd0} \) is the initial voltage of \( C_d \). \( i_{L_d}(t) \) and \( u_{Cd}(t) \) can be given as Equation (6)

\[
\begin{align*}
    i_{L_d}(t) &= U_{Cd0} \cos \left( \frac{t}{\sqrt{L_d C_d}} \right) + \frac{U_{Cd0}}{\sqrt{L_d C_d}} \sin \left( \frac{t}{\sqrt{L_d C_d}} \right) \\
    u_{Cd}(t) &= U_{Cd0} \sin \left( \frac{t}{\sqrt{L_d C_d}} \right) + \frac{1}{\sqrt{L_d C_d}} \cos \left( \frac{t}{\sqrt{L_d C_d}} \right)
\end{align*}
\]

3.1.2 Mode II

Mode II of APDC is shown in Figure 4. In mode I, \( U_{\text{inv}} > 0 \) and \( P_d < 0 \), \( S_1 \) is ON, \( S_2, S_4, S_5 \) and \( S_6 \) are OFF, and \( S_3 \) is the master switch controlled by the HF PWM signal. Mode II can also be divided into two stages shown by the red solid line and black dashed line, respectively. At this time, \( C_d \) releases energy to the AC side and \( u_{Cd} \) decreases. Since the inductance of \( L_d \) is small and \( u_{Cd} \) is high, \( i_{L_d} \) rises linearly from zero to the peak current \( i_{L_d, \text{peak}} \) with the slope of \( U_{\text{inv}} / L_d \) in stage one. \( D_{12} T_s \) is the turn-on time of \( S_6 \) and the \( D_{12} T_s \) is the time when \( i_{L_d} \) decreases from \( i_{L_d, \text{peak}} \) to zero. The decreasing process of \( i_{L_d} \) is LC resonance, which is the same as mode I as shown in Figure 3.

3.1.3 Modes III/IV

When \( U_{\text{inv}} < 0 \) and \( P_d > 0 \), the APDC works on mode III, which is shown in Figure 4. In this mode, \( S_2 \) is ON. \( S_1, S_3 - S_6 \) are OFF, and \( S_4 \) is the master switch. \( C_d \) stores the energy and \( u_{Cd} \) increases. When \( U_{\text{inv}} < 0 \) and \( P_d < 0 \), the APDC works on mode IV, which
FIGURE 6 Mode IV (a) current flow path, (b) \(i_{Ld}\) in [\((n-1)T_s \sim nT_s]\), (c) equivalent circuit

FIGURE 7 Driving signal of APDC

is shown in Figure 5. In this mode, \(S_1\) is ON. \(S_1, S_2, S_3\) and \(S_6\) are OFF and \(S_5\) is the master switch. At this time, \(C_d\) releases energy and \(u_{Cd}\) drops.

Combining Figures 5–8, it can be seen that the switching state and current circuit of APDC in mode I–IV are different, but the energy transferring direction of modes I and III is \(U_{inv} \rightarrow L_d \rightarrow Cd\) and the energy transferring direction of modes II and IV is \(Cd \rightarrow L_d \rightarrow U_{inv}\). The magnitude of \(P_d(t)\) determines the absolute value of the time-domain function of \(i_{Ld}\) and \(u_{Cd}\), and the polarity of \(u_g(t)\) determines the polarity of \(i_{Ld}\). It can be seen from Figure 1 that \(P_d(t)\) is symmetric with axis \(t = T/2\) in \(0, T_s\), so the absolute values of time-domain functions of \(i_{Ld}\) and \(u_{Cd}\) in modes III and IV are the same as modes I and II, respectively. The polarity of \(u_g(t)\) is opposite to \((0, T/2)\) and \((T/2, T)\), so the polarity of the time-domain function of \(i_{Ld}\) in modes III and IV is opposite to modes I and II, respectively.

3.2 Time sequence of APDC

It can be seen from the analysis of mode I–IV that the switching state is determined by the magnitude of \(P_d\), the polarity of \(U_{inv}\) and \(P_d\). The switch state table of \(S_1–S_6\) can be obtained as shown in Table 4.

In Table 4, ‘0’ indicates the switch is OFF and ‘1’ indicates the switch is ON. ‘1/0’ indicates the switch is the master switch driven by the HF PWM control signal. ‘A’ and ‘B’ indicates the polarity of \(u_g\) and \(P_d\). ‘A = 1’ indicates \(u_g\) is positive. ‘A = 0’ indicates negative. ‘B = 1’ means \(P_d < 0\). ‘B = 0’ means \(P_d > 0\) \((P_d > 0)\).

According to Table 4, the logic expression of the switch state can be deduced as follows:

\[
\begin{align*}
S_1 &= \overline{A} \cdot \overline{B} \\
S_2 &= A \cdot \overline{B} \\
S_3 &= \overline{A} \cdot B + A \cdot \overline{B} \cdot PWM \\
S_4 &= A \cdot B + \overline{A} \cdot B \cdot PWM \\
S_5 &= A \cdot B \cdot PWM \\
S_6 &= \overline{A} \cdot B \cdot PWM
\end{align*}
\]

Therefore, the driving signals of \(S_1–S_6\) are obtained as shown in Figure 7. The time-domain distribution of \(S_1–S_6\) is based on the distribution of modes I–IV, which is divided into LF constant duty cycle signal and HF PWM signal. The LF signal is used as the auxiliary signal and the HF signal controls \(P_d\). In each working mode, the HF and LF signals work together to control the corresponding switches. With the switching of working mode, the HF and LF signals are switched to the other two switches, respectively.

4 CONTROL STRATEGY DESIGN

4.1 PEM control strategy

APDC is in parallel with the two-stage inverter, so their control system design can be carried out independently. The inverter adopts a unipolar SPWM modulation strategy. This section mainly discusses the control strategy of APDC.

| \(S_1\) | \(S_2\) | \(S_3\) | \(S_4\) | \(S_5\) | \(S_6\) | A | B |
|--------|--------|--------|--------|--------|--------|---|---|
| Mode I | 1      | 0      | 0      | 1/0    | 0      | 0 | 0 |
| Mode II| 0      | 0      | 1      | 0      | 0      | 1/0| 1 |
| Mode III| 0     | 1      | 1/0    | 0      | 0      | 1  | 0 |
| Mode IV| 0      | 0      | 0      | 1      | 1/0    | 0  | 1 |

TABLE 4 Four operation modes of inverter
From Figure 6, it can be seen that $P_d$ is controlled by HF PWM signal. $D(n)$ is the duty cycle of the PWM signal determined by the decoupled energy $W(n)$ in the carrier period. This paper names it as pulse energy modulation (PEM) control strategy.

According to Equation (4), in the $n$th switching period $[(n - 1)T_s \sim nT_s]$, the energy needed to be buffered is

$$W(n) = \int_{(n-1)T_s}^{nT_s} P_d(t)dt = \int_{(n-1)T_s}^{nT_s} U_b I_{d} \cos(2\pi n t)dt$$

$$= \frac{U_b I_{d} T_s}{4\pi} [\sin \left(\frac{4\pi n T_s}{f_s}\right) - \sin \left(\frac{4\pi (n - 1) T_s}{f_s}\right)]$$

$$= \frac{P_d}{4\pi f} \left[\sin \left(\frac{4\pi n f}{f_s}\right) - \sin \left(\frac{4\pi (n - 1) f}{f_s}\right)\right]$$

(10)

where $f_s$ is switching frequency, $f$ is the frequency of $u_c(t)$.

According to Equation (10), the system needs to sample $u_c(t)$ and $i_d(t)$ to obtain instantaneous decoupling power $P_d(t)$. Also, $W(n)$ is related to the output power $P_d$ of the inverter in the carrier period but not to the control of the previous DC/DC circuit. At the same time, $W(n)$ satisfies the energy formula of $L_d$

$$W(n) = \frac{1}{2} L_d i_{dref}(n)^2$$

(11)

$i_{dref}$ is the given value of the peak current of $i_{d,ref}$. When $i_{d,ref}$ rises to $i_{dref}$, the transfer of decoupling energy to $L_d$ is completed. $i_{dref}$ can be

$$|i_{dref}(n)| = \sqrt{\frac{2W(n)}{L_d}}$$

$$= \sqrt{\frac{P_d}{2\pi f I_{d}}} \left[\sin \left(\frac{4\pi n f}{f_s}\right) - \sin \left(\frac{4\pi (n - 1) f}{f_s}\right)\right]$$

(12)

Subsequently, the discrete distribution of $i_{dref}$ in $[0, T]$ and its envelope $i_{d,ref}$ can be obtained as shown in Figure 8.

According to the fitted curve $i_{d,ref}$, the theoretical waveform of $i_{d,ref}$ could be obtained, which is shown in Figure 9. $i_{d,ref}$ flows in the positive direction in modes I and IV while flowing in negative direction in modes II and III. According to Table 2, $P_d$ decreases in $[0\sim T/8]$, so does $i_{d,ref}$. In $[T/8\sim 3T/8]$, $i_{d,ref}$ increases first and then decreases along with $P_d$. The variable tendency of the peak value of $i_{d,ref}$ in the rest time interval is the same as above. In the partial enlarged diagram of $i_{d,ref}$ in modes II and I, it can be seen that $i_{d,ref}$ rises linearly from zero to the peak current. After that, $i_{d,ref}$ decreases to zero along the curve of slope reduction under the resonation of $L_d$ and $C_d$

When APDC absorbs energy from the two-stage inverter in stage one of modes I and III, $U_b$ is equal to the voltage of $L_d$, $i_{dref}(n)$ satisfies

$$i_{dref}(n) = \frac{U_b}{I_{d}} \cdot D(n) \cdot T_s$$

(13)

By substituting Equations (12) into (13), $D(n)$ can be obtained as

$$D(n) = \frac{I_{d} \cdot |i_{dref}(n)|}{U_b \cdot T_s}$$

$$= \frac{f_s}{U_b} \sqrt{\frac{P_d I_{d}}{2\pi f} \left[\sin \left(\frac{4\pi n f}{f_s}\right) - \sin \left(\frac{4\pi (n - 1) f}{f_s}\right)\right]}$$

(14)

Since the working range of modes I and III are $[0\sim T/8]$, $[3T/8\sim 5T/8]$, $(7T/8\sim T)$, $n$ satisfies

$$n \in \left[1, \frac{T}{8T}\right] \cup \left[\frac{3T}{8T} + 1, \frac{5T}{8T}\right] \cup \left[\frac{7T}{8T} + 1, \frac{T}{8T}\right]$$

When APDC delivers energy to the two-stage inverter in stage one of modes II and IV, $U_b$ is equal to the voltage of $L_d$, $i_{dref}(n)$ satisfies

$$i_{dref}(n) = \frac{U_{Cd}}{I_{Cd}} \cdot D(n) \cdot T_s$$

(15)

By substituting Equations (11) into (15), $D(n)$ can be obtained:

$$D(n) = \frac{I_{d} \cdot |i_{dref}(n)|}{U_{Cd} \cdot T_s}$$

$$= \frac{f_s}{U_{Cd}} \sqrt{\frac{P_d I_{d}}{2\pi f} \left[\sin \left(\frac{4\pi n f}{f_s}\right) - \sin \left(\frac{4\pi (n - 1) f}{f_s}\right)\right]}$$

(16)
Since the working ranges of modes II and IV are \((T/8, 3T/8), (5T/8, 7T/8)\), the value range of integer \(n\) is

\[
 n \in \left[ \frac{T}{8T} + 1, \frac{3T}{8T} \right] \cup \left[ \frac{5T}{8T} + 1, \frac{7T}{8T} \right]
\]

Subsequently, the duty of the PEM signal is related to \(U_b\) in charging and it is related to \(U_{Cd}\) in discharging process. It is necessary to sample \(U_b\) and \(U_{Cd}\) in order to calculate the duty of PEM more accurately.

### 4.2 Frequency characteristic of APDC

In the range of \((T/8 \sim 3/8T)\) of \(n_g\), the decoupling energy of the inverter is \(W_t\), which is expressed as

\[
 W_t = \int_{T/8}^{3T/8} P_h(t)dt = \int_{T/8}^{3T/8} U_{Cd}g \cos(2\omega t)dt = \frac{P_h}{2\pi f}
\]

(17)

where \(P_h\) is the rated output power of the inverter.

As \(2\omega\)-ripple power is completely absorbed by decoupling capacitor \(C_d\), then

\[
 W_t = \frac{1}{2} C_d U_{\text{peak}}^2 - \frac{1}{2} C_d U_{\text{av}}^2 = C_d \cdot \frac{U_H + U_L}{2} \cdot (U_H - U_L)
\]

(18)

\[
 \begin{cases}
 \Delta U = U_H - U_L \\
 U_{\text{av}} = \frac{U_H + U_L}{2}
\end{cases}
\]

(19)

where \(U_H\) and \(U_L\) are the peak value and valley value of \(u_{Cd}\). \(\Delta U\) is the peak-to-peak value of \(2\omega\)-ripple voltage coupled on \(u_{Cd}\). \(U_{\text{av}}\) is the given value of DC bias on \(u_{Cd}\).

With the inverter working in the frequency conversion situation, the relationship between \(\Delta U\) and \(f\) can be obtained:

\[
 \Delta U = \frac{P_h}{2\pi U_{\text{av}} C_d} \cdot \frac{1}{f}
\]

(20)

Thus, \(\Delta U\) is inversely proportional to \(f\) when nominal power \(P_h\) and the given value \(U_{\text{av}}\) are set as constant.

### 5 SIMULATION VERIFICATION

In order to verify the APDC and its control strategy in this paper, a simulation platform of the two-stage inverter with the APDC is built in Matlab. The inverter adopts unipolar sine pulse width modulation (SPWM) modulation, and the APDC adopts the PEM control strategy. The simulation parameters of the circuit are shown in Table 5.

Figure 10 shows the simulation waveform of \(i_Ld\) and \(u_{Cd}\) when APDC puts into operation at 0.2 s. As can be seen from Figure 10, the maximum peak value of \(i_Ld\) is 25 A in the charging process and 22 A in the discharging process. The average value of \(u_{Cd}\) is 650 V, and 100 Hz pulsation component is coupled on \(C_d\), and the pulsation range of \(u_{Cd}\) is 582–714 V.

Figure 11 shows the simulation waveform of \(U_{inv}\) and \(u_{g}\). The HF pulse sequence of \(U_{inv}\) shows a large swing, and the waveform of \(u_{g}\) is distorted before 0.2 s. With APDC running, the HF pulse sequence of \(U_{inv}\) is flat, and the waveform quality of \(u_{g}\) is improved.

It can be seen from Figure 12 that \(u_{g}\) is coupled with 150 Hz LF ripple components when APDC not running. At this time, the THD of \(u_{g}\) is 5.49%, and the third harmonic content is 5.47%. The coupling of a large number of LF harmonic components makes \(u_{g}\) seriously distorted. With the APDC running, the third harmonic is effectively suppressed. At this time, the third harmonic component is 0.93%, and the quality of \(u_{g}\) is improved.
Figure 13 shows the simulation waveform of $U_b$ and $I_b$. The average value of $U_b$ is 400 V and the variation range of $U_b$ is 314–480 V. The swing amplitude of twice frequency component is 166 V, which makes up a relatively significant share (30%) of $U_b$ when $t < 0.2$ s. When the APDC puts into operation, the average value of $U_b$ is about 400 V, and the variation range of $U_b$ is 394.8–405.2 V. The amplitude of the second harmonic component is 10.4 V, which is equal to 2.6% of $U_b$. It can be seen that the average value of $I_b$, which is DC-input current is 5.5 A. $I_b$ is also coupled with the second harmonic current component when $t < 0.2$ s. The current swing of $I_b$ is 2.8 A. When the APDC puts into operation, the second harmonic current swing is reduced to 0.7 A.

Figure 14 shows the fast fourier transformation (FFT) analysis of input current. It can be seen that $I_b$ is coupled with 100 Hz LF ripple component when the APDC not running, and the second harmonic content is 24.05%. With the APDC running, the 100 Hz ripple component is effectively suppressed and the second harmonic content of $U_b$ decreases to 1.73%.

The simulation results prove that the proposed six-switch APDC can buffer the unbalance of instant power of DC/AC side and suppress twice the frequency component of $U_b$ and $I_b$.

6 | EXPERIMENTAL VERIFICATION

In order to verify the effectiveness of APDC and its PEM control strategy, an experimental platform is built as shown in Figure 15. The main hardware experiment parameters of the system are shown in Table 6.

### 6.1 Experiment with E-caps

Traditional micro-inverter uses large-capacity E-caps to suppress the second-order ripple power on the DC side. Then,
the micro-inverter experiment is carried out with a 220 µF E-cap selected for $C_b$. The experimental platform is shown in Figure 15. The experimental parameters are shown in Table 6. The experimental results of 220 µF E-cap are shown in Figure 16. It can be seen that the ripple range of $U_b$ is about 8 V.

6.2 Experiment with APDC

The experiment of the novel inverter with APDC is carried out on the experimental platform of Figure 15 and the experimental parameters of Table 4. A 20 µF film capacitor is selected for $C_d$.

Figure 17 is the timing sequence of the driving signals for six switches in APDC. It can be seen that the relationship between the timing sequence of the driving signals is consistent with the theoretical analysis in Figure 7.

Figure 18 shows the experimental waveforms of $i_{L_d}$. It can be seen that the relationship between $i_{L_d}$ and $U_{inv}$ is consistent with the simulation results shown in Figure 10 and the principle analyses shown in Figure 9. In $[0, T]$, the distribution of the four modes is I, II, I, III, IV, III in turn and the proportion of the interval length is 1:2:1:2:1. $i_{L_d}$ flows forward in modes I/IV and reverse in modes II/III.

In the partial enlarged drawing of $i_{L_d}$ in modes I and II, it can be seen from the figure that in the carrier period $T_c$, $i_{L_d}$ rises linearly from zero to peak value, and the charging speed of $i_{L_d}$ is constant. Once the peak current reached, $i_{L_d}$ drops to zero along the curve. The slope of the decline process decreases gradually and the discharge speed of $i_{L_d}$ slows down. The charging and discharging process of $i_{L_d}$ is controlled in the carrier period. The initial value of $i_{L_d}$ in each carrier interval is zero so as to control energy in the carrier unit.

Figure 19 shows the experimental waveforms of $i_{L_d}$ and $u_{Cd}$. As can be seen, the peak current of $i_{L_d}$ in starting process is greater than that in the stable process in modes I/III. The peak current of $i_{L_d}$ in starting process is less than that in stable process modes II/IV. Therefore, the energy absorbed by $C_d$ is greater than the energy released, so the average voltage of $C_d$ increases. After several working cycles of the inverter, the average value of $u_{Cd}$ is 150 V, and the voltage fluctuation amplitude is 130—178 V. The amplitude of the second ripple on $C_d$ is 48 V and the frequency is 100 Hz.

Figure 20 shows the experimental waveforms of $U_b$, $i_{L_d}$, $U_{inv}$ and $u_C$. It can be observed that the HF pulse sequence of $U_{inv}$.
indicates large amplitude and $u_g$ is distorted when APDC not running. Meanwhile, the average value of $U_g$ is 108 V, the fluctuation range is 92–128 V, and the secondary ripple swing is 36 V and accounts for 33.3% of the DC component.

With APDC running, the HF pulse sequence of $U_{inv}$ is straight. The waveform quality of $u_g$ is improved, which is close to the sine wave. The average value of $U_g$ is 100 V, and the fluctuation range of $U_g$ is 96–104 V. The secondary ripple swing is 8 V and accounts for 8% of the DC component. Therefore, the swing of $U_g$ decreases by 77.8% (from 36 to 8 V). The waveform quality of the novel micro-inverter with 20 µF capacitor film is equivalent to the traditional micro-inverter with a 220 µF E-cap.

Figure 21 shows the experimental results of the dynamic characteristics of APDC. The waveforms from top to bottom are $i_g$, $u_{Cd}$, $i_L$, and $u_{Cd}$. When the load changes from 50 to 25 Ω, $u_g$ remains constant basically, $i_g$ increases from 0.8 to 1.6 A, and $P_{av}$ is doubled. With the increase of $P_{av}$, the peak value of the $i_L$ in modes I–IV is higher than before. When the load is 50 Ω, the swing amplitude of the $u_{Cd}$ is 138–158 V; when the load is 25 Ω, the swing amplitude of $u_{Cd}$ is 115–155 V and the decoupling energy of $C_d$ increases. Therefore, the instantaneous decoupled power of APDC can track the output power of the inverter in time.

Figure 22 shows the frequency characteristic of APDC. When the frequency of $u_g$ is smoothly changed from 50 to 25 Hz, the duration of the four working intervals of the inverter changes accordingly. The decoupling inductance current in APDC can compensate the instantaneous decoupling energy in the variable working interval, so the duration of the four working modes of $i_L$ also changes accordingly. In addition, with the decrease in $f$, the frequency of the secondary voltage ripple on $C_d$ decreases and the peak-to-peak value of the secondary voltage ripple $\Delta U$ increases gradually. It can be seen that APDC can track the output frequency of $u_g$ in time to achieve accurate power decoupling. So APDC can be used in variable frequency drive.

The efficiency curve of the proposed inverter versus the output power is drawn in Figure 23. The efficiency is calculated by dividing the inverter output power by its input power. Input and output powers are obtained by multiplying voltage and current values that are measured by a digital multimeter. The efficiency continuously increases as the output power increases.

Based on the above experimental results, it can be seen that the low capacitance film capacitor connected to the two-stage inverter system as the bus capacitance will cause the distortion of the output voltage waveform at the ac side and increase the secondary ripple amplitude at the DC side. APDC can effectively suppress the secondary ripple component on the DC side and improve the distortion of the output voltage waveform caused by the low capacitance film capacitor.

## Conclusion

In this paper, an APDC and corresponding PEM control strategy are proposed. The circuit is connected in parallel with the
When APDC is put into operation, the suppression of 2ω-power ripple in the system. Through the verification of simulation and experimental platform, the following conclusions are drawn. For a 200 W experimental prototype, only 20 μF bus capacitor and 10 μF decoupling capacitor are needed to control the secondary ripple amplitude of bus voltage at about 8 V, which is equivalent to 220 μF E-cap. In the new scheme, the required bus capacitor per unit power is 0.4 μF/W. The PEM control strategy is adopted in APDC, which makes the decoupling of 2ω-power more accurate, simple and easy to realise. When APDC is put into operation, the suppression of 2ω-ripple of the bus voltage in two-inverter no longer depends on large E-caps, which prolongs the life of the inverter and reduces the volume of the system and increases the reliability of the system. However, the existence of semiconductor devices in the decoupling circuit will inevitably increase the cost of the system, so the switching devices in APDC should be further reduced in future research.

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