Intrinsic synaptic plasticity of ferroelectric field effect transistors for online learning

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Nanoelectronic devices emulating neuro-synaptic functionalities through their intrinsic physics at low operating energies is imperative toward the realization of brain-like neuromorphic computers. In this work, we leverage the non-linear voltage dependent partial polarization switching of a ferroelectric field effect transistor to mimic plasticity characteristics of biological synapses. We provide experimental measurements of the synaptic characteristics for a 28nm high-k metal gate technology based device and develop an experimentally calibrated device model for large-scale system performance prediction. Decoupled read-write paths, ultra-low programming energies and the possibility of arranging such devices in a cross-point architecture demonstrate the synaptic efficacy of the device. Our hardware-algorithm co-design analysis reveals that the intrinsic plasticity of the ferroelectric devices has potential to enable unsupervised local learning in edge devices with limited training data.

Harnessing the unique features of ferroelectric materials in essentially a device structure similar to that of a traditional transistor, Ferroelectric Field-Effect Transistor (FeFET) has the potential to expand the capabilities of current CMOS platforms to drive the innovations required in computing for emerging data-oriented applications. The recent discovery of ferroelectricity in CMOS compatible Hafnium Oxide has made this a possibility due to its great scalability and superior energy efficiency. Previously, the incompatibility of perovskite based complex oxide ferroelectrics had put these devices by the wayside. The device, shown in Fig. 1(a-b), is characterized by a HfO₂ film ferroelectric layer replacing the conventional high-k dielectric in the gate stack of a MOSFET. Depending on its direction, the polarization either aids the formation of inversion or depletion/accumulation of the underlying semiconductor channel, hence modulating the threshold voltage of the FeFET.

In addition, partial polarization switching can be induced by applying a voltage pulse train with either identical pulses or varying pulses of different amplitudes or pulse widths to the gate of the FeFET, such that a gradual tuning of the threshold voltage and subsequently the channel conductance can be realized (see Fig. 1(c)). This enables the application of FeFETs as multi-state non-volatile weight cells or synaptic memory elements suitable for integration in dense memory cross-point arrays in neuromorphic systems. Cross-point arrays enable computation and memory update all within the same array itself, circumventing the von Neumann bottleneck of latency and energy overhead associated with moving data back and forth between logic and memory units. Additionally, the multi-level accumulative property of FeFET combined with their merged logic-memory functionality makes them very attractive for on-chip learning and designing adaptive intelligent systems for ubiquitous edge devices that are robust to the changing real-world environment while still remaining energy and area efficient.

Previous works on exploring FeFETs as synaptic elements have primarily focused at the device level without considering system and algorithm level feedback. For instance, Refs. 3–5 abstract the FeFET synaptic functionality driven by a pulse train where the pulsing scheme involves incremental pulse amplitudes. From an online learning perspective, such complex pulsing schemes would require us to read-out individual device states during the learning process and update each device individually by the appropriate pulse train, thereby requiring look-up table based approaches. The overhead of such schemes increase significantly with increasing network size, in addition to the already computationally expensive operations of online device programming events. Moreover, the complex learning schemes are also driven by the goal of achieving linearity in the programmable device states. This work adopts the alternative route of leveraging the intrinsic plasticity characteristics of the FeFET device itself under single programming pulse excitation for learning algorithm formulation. This allows us to preserve the benefits of the core device to higher levels of circuit and system design abstraction.

Designing brain-inspired adaptive intelligent systems that embrace the non-linear intrinsic plasticity of ferroelectric synapses instead of viewing it as a disadvantage will be critical to implement online learning with minimal peripheral overhead. In this work, we showcase the FeFET synaptic properties that can be exploited in a neuromorphic system including experimental characterization, device modelling and benchmarking, algorithm formulation based on intrinsic device physics along with the development of a device-circuit-algorithm co-simulation framework to assess the performance of the FeFET synaptic memory device at scale for a spiking neural network based adaptive learning system.

The multiple state programming capability of ferro-
electric materials occurs due to the presence of multidomains, related with the lateral grain size. The number of domains (and available programming states) therefore increases with increasing device size. Since the coercive voltage varies spatially across domains, the switching voltage of a particular domain varies in proportion with the corresponding coercive voltage. Grain size and grain orientation of the ferroelectric material are some of the major factors that influence the spatially inhomogeneous distribution of the coercive voltage. Upon application of a programming gate voltage, discrete probabilistic switching events of a subset of the domains take place resulting in the threshold voltage of the FeFET changing gradually.

In order to understand the synaptic plasticity characteristics of the FeFET device, we measured the change in channel conductance of the device in response to programming voltages of varying amplitude. The synaptic plasticity/weight change is equivalent to the FeFET conductance change. For a given programming pulse amplitude, FeFETs with lower conductance undergo a greater increase in conductance after the “write” operation since lower conductance is achieved by a larger polarization pointing at the gate metal, hence more are available to switch during the positive “write” pulses, which therefore induces a greater conductance change. The reverse is true for the depression operation where the device conductance is decreased due to the application of a negative programming voltage. To capture this effect in our device modelling, we performed experimental measurements for a 1μm × 1μm FeFET device triggered by a pulsing scheme, as shown in Fig. 2(a) which consists of a reset pulse, a set pulse and a programming pulse. The FeFET is based on an industrial 28nm high-k metal gate (HKMG) technology. The device features an 8nm thick doped HfO₂ ferroelectric layer and ~ 1nm SiO₂ native oxide. During characterization, a reset pulse of magnitude −4V is applied to reset all the domains of the ferroelectric layer to negative polarization states. The device is initialized to different intermediate conductance states by changing the set pulse voltage from 2V to 3.5V with increments of 0.1V. The device plasticity characteristics is then evaluated by the application of a subsequent programming pulse. Finally, measurements are performed for different programming voltage amplitudes ranging from 2V to 4V with 50mV steps. Drain current values after the set pulse (I_D, set) and the programming pulse (I_D, read) are measured for different set pulse voltages representing different intermediate states of the device. Changes in current (∆I_D = I_D, read − I_D, set) as a function of the programming voltage are calculated to reflect the synaptic conductance change for potentiation and depression (Fig. 2(b)).

To develop an experimentally calibrated device model for our device-algorithm co-simulation framework, we utilized a Monte Carlo algorithm to calculate the switching probability of domains at each time step. The ferroelectric behavior modelling framework considers that the ferroelectric layer consists of multiple independent domains, polarized in either one of the two stable orientations. Under a constant electric field, E_fe, the nucleation time constant, τ is independent of time. If a domain switches within a certain time step, ∆t, the domain switching probability, p_i can be expressed as:

\( p_i(t_s < t + \Delta t | t_s > t) = 1 - e^{(-\frac{\Delta t}{\tau})^\beta} \)  \( \tau = \tau_i \) (1)

where, β is the shape parameter of the probability distribution. \( t_s \) is the switching time of the i-th domain considering that the domain has not switched before \( t \), and \( \tau_i \) is the switching time constant of the i-th domain. In case of a switching event, the state, \( s_i(t) \), of the i-th domain gets altered. Total polarization, \( P_{total} \), can be measured by taking the summation of the states of all the N number of domains present in the ferroelectric layer,

\( P_{total}(t) = \frac{P_i}{N} \sum_{i=1}^{N} s_i(t) \) (2)

where, \( P_i \) is a constant polarization for each domain. In our case, since the applied electric field is temporally varying (E_fe(t)), the switching time constant becomes a function of activation field, \( E_a,i \), and applied electric field, \( E_fe(t) \). \( \frac{1}{\tau} \) in Eqn. 1 can be replaced by the history parameter, \( h_i(t) \), of the form,

\( h_i(t) = \int_{t_0}^{t} \frac{dt'}{\tau(E_fe(t'), E_{a,i})} \) (3)

The history parameter, \( h_i(t) \), increases till the domain flips. This growth captures the accumulative behavior of
FIG. 2. (a) Pulses scheme for potentiation (orange) and depression (green) with a reset pulse of magnitude = -4V and pulse duration = 1µs, set pulse of magnitude = 2V to 3.5V and pulse duration = 100ns and programming pulse of magnitude = 2V to 4V (~-2V to -4V) for potentiation (depression) and pulse duration = 100ns. (b) Experimentally measured drain current values have been plotted with respect to the programming voltage amplitude (Vg). Top left (bottom left) plot shows the measured initial current (I_{D,read}) after the set pulse for potentiation (depression) for different set pulse voltages. The curves are almost horizontal as it is independent of the programming voltage. Top middle (bottom middle) plot shows measured read current (I_{D,read}) after the programming pulse during read condition for potentiation (depression). Top right (bottom right) plot shows the change in current (∆I_D) for potentiation (depression).

The ferroelectric layer and therefore the switching probability of a domain can be expressed as,

\[ p_i(t_s < t + \Delta t \mid t_s > t) = 1 - e^{-(b_1(t) - (b_1(t+\Delta t)))^{\beta}} \]  

(4)

By tracking the polarization behavior, the model is then self-consistently solved with transistor charge-voltage equations (see Fig. 1(d)) to obtain FeFET device characteristics. As shown in Fig. 3(a), the normalized read current for different device intermediate states matches well with the corresponding experimental data.

We studied the intrinsic adaptive synaptic characteristics of the FeFET in the context of unsupervised Spike Timing Dependent Plasticity (STDP) in neuromorphic systems. In such a system, spikes are propagated through the network and the synaptic weights are modified by STDP according to the time difference between spiking events of the pre- and post-synaptic neurons. Similar to the way the biological brain works, networks employing such spikes and synaptic learning rules are referred to as Spiking Neural Networks (SNN) and are gaining greater interest owing to their bio-plausibility, energy-efficiency and hardware friendly mechanism. The unsupervised, local, few-shot clustering capability of STDP is an ideal fit for on-chip embedded intelligence in resource constrained edge devices with limited labelled data where it may not be always possible to transmit information to the cloud for real-time processing. In order to envisage the implementation of STDP in FeFET devices, we consider the devices to be programmed by an adaptive programming voltage which is tuned in accordance to the timing delay between pre- and post-synaptic neuron spikes. Interestingly, the ∆I_D plots in Fig. 2(b) reveal that the characteristics saturate at a particular voltage, \( V_{0+}(V_{0-}) \) for potentiation (depression) for all the intermediate states, thereby indicating a saturation voltage beyond which the device is programmed to the other state. Let us discuss the STDP implementation for the potentiation phase. Similar discussions are also valid for depression. STDP corresponds to the change in synaptic weight (\( \Delta w \)) as a function of the time difference (\( \Delta t \)) between post-synaptic neuron and pre-synaptic neuron spikes.

The weight change is maximum at \( \Delta t = 0 \) and decays with increasing \( \Delta t \), thereby promoting temporal correlation. This saturation voltage (\( V_{0+} \)) therefore corresponds to the voltage that is applied to the FeFET corresponding to the \( \Delta t = 0 \) condition. Assuming a direct linear correspondence between applied programming voltage and spiking time-delay (to be implemented by appropriate peripheral operation discussed later), we abstract the STDP synaptic weight change, \( \Delta w \) (electrical analogue: normalized device conductance change, \( \Delta G \)), as a function of the time-delay between spikes (electrical analogue: programming voltage measured with respect to the saturation voltage applied corresponding to \( \Delta t = 0 \), \( \Delta V_+ = V_P - V_{0+} \)) as,

\[
\Delta G = \begin{cases} 
(1 - G)\mu_+ \times A_+ \times e^{-\frac{-\Delta V_+}{\tau_+}}, & \Delta t > 0 \\
(G)\mu_- \times A_- \times e^{-\frac{-\Delta V_-}{\tau_-}}, & \Delta t < 0
\end{cases}
\]  

(5)

where, \( A_+ \) and \( A_- \) are constants, \( \mu_+ \) and \( \mu_- \) refers to the degree of dependence of \( \Delta G \) on current conductance state \( G \), \( \tau_+ \) and \( \tau_- \) represent the STDP time constants. The double exponential nature of the phenomenological model was based on similar switching characteristic modelling of other memristive technologies. The FeFET STDP compact model parameters are extracted from our experimentally calibrated device simulation framework (\( A_+/A_- = 2.91/2.52, \mu_+/\mu_- = 2.5/1.5, \tau_+/\tau_- = (G) = 0.57-0.76G/-1.54-0.79G \)). The conductance depen-
FeFET devices every time the post-synaptic neuron fires ($t_2$) and activate the $V_{POST}$ control signal. Let us first discuss the potentiation, i.e., the positive STDP learning window ($\Delta t > 0$). At the beginning of the positive time-window ($t_1$), the $V_{GS, \text{write}}$ is linearly decreased such that whenever the access transistor is on, the necessary programming voltage for potentiation (applied at the gate terminal of the FeFET) is tuned in accordance to $\Delta t = t_2 - t_1$. The negative learning window can be implemented by a simple extension of the above scheme by using a negative $V_{GS, \text{write}}$ during the programming process.

We evaluate the performance of these synaptic devices and their multiplicative dynamics in a network learning scenario. An experimentally calibrated device-algorithm co-simulation framework was devised in BindsNET\cite{22} (a PyTorch based package) to train an unsupervised SNN\cite{23} on a standard handwritten digit recognition problem based on the MNIST dataset\cite{24}. The network, shown in Fig. 4(a), consists of an excitatory layer of neurons that receives the weighted summation of spikes from the inputs. The analog pixel intensities of the image are mapped to the firing rate of the input spike trains through a Poisson process. The excitatory layer can be therefore mapped to a cross-array of FeFET synapses, as shown in Fig. 1 where the devices are programmed in an online fashion based on spike timings. The PRE-synaptic neurons correspond to the input neurons while the POST-synaptic neurons correspond to the excitatory layer neurons. In order to promote competition, the excitatory neurons are characterized by lateral inhibition effects by preventing other neurons from spiking whenever a particular excitatory neuron fires. Additionally, to ensure no single neuron dominates the firing pattern, homeostasis is implemented through adaptive thresholding where the neuron threshold increases every time a neuron fires. Lateral inhibition and homeostasis effects can be implemented by simple peripheral circuitry\cite{25} of the FeFET synaptic cross-array.

Our network simulations consisted of an excitatory layer of 225 spiking neurons characterized by Leaky Integrate and Fire (LIF) dynamics with intrinsic FeFET synaptic plasticity (see Fig. 3(a-b)). In order to assess the impact of the intrinsic device characteristics on the learning process, we performed a comparative simulation with standard STDP rule. As shown in Fig. 5(c), the multiplicative STDP behavior of the devices resulted in significantly faster convergence of the network, which is advantageous from the perspective of few-shot learning and minimizing costly programming events in the FeFET cross-array. We postulate that this advantage is mainly due to the self-adaptive behavior of multiplicative STDP, as mentioned before. As the weights are randomly initialized at the beginning of the training process, synaptic weights which are further away from their eventual converged values experience a larger synaptic change (potentiation or depression) compared to weights that are relatively close to their final magnitudes. It is worth

\[ V_{GS, \text{write}} = (1 - 3/4) V_{o}^{+} \]

\[ V_{o}^{+} = 3.4V \]
Our SNN architecture consists of an excitatory neuron layer with lateral inhibitory connections for unsupervised learning. The synaptic weights joining the input and excitatory layer are implemented using FeFET devices and undergo STDP learning. Further updates mostly fine-tuned the weights. It can be seen that this convergence in learning occurs with 33.3% fewer training samples while using the FeFET dynamics compared to the standard STDP learning rule.

In summary, the intrinsic non-linear synaptic plasticity and ultra-low programming energies of ferroelectric field effect transistors make them an ideal candidate for future brain-inspired computing paradigms that are able to learn unsupervised representations in an online fashion from limited training data.

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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