Crosstalk Analysis and Suppression of GaN Driving Circuit in Bridge Converter

Yang Zhou, Li Yang * and Xiang Gong
Xichang Satellite Launch Centert, Xichang, China

*Corresponding author e-mail: 27341531@qq.com

Abstract. Enhancement mode Gallium-Nitride power transistors (GaN HEMT) have emerged as promising devices for high frequency, high efficiency and high power density switch mode power supplies. However, when GaN device works in high frequency, the $\frac{dv}{dt}$ and $\frac{di}{dt}$ slopes are increased due to stray inductances and parasitic capacitances, which leads to oscillations and overshoots in gate-source voltage and affect the stability of driving circuits. Especially in the phase-bridge circuit, the crosstalk between the upper and lower switch seriously limits the performance of the device. In order to solve the short circuit problem of bridge arms generated by oscillation and crosstalk, an improved design of gate driving circuit was proposed, which could eliminate the parasitic oscillation and voltage spikes, suppress crosstalk and higher harmonics effectively. In addition, A double pulse test prototype is built and the simulation and experimental results verify the effectiveness of this driving circuit.

1. Introduction
Bridge arm circuit is a commonly circuit structure, which contains two series-connected switching devices, fast switching transient of one device will affect the operating behavior of its complementary device, when the peak voltage of the crosstalk signal reaches the threshold voltage $V_{th}$, the switch may be partially turned on and a shoot-through current will be generated[1].

Currently, some research has been done for crosstalk mitigation, the main methods to suppress crosstalk include: optimizing the layout of the circuit to reduce the parasitic inductance, increasing the driving resistance, adding auxiliary circuit parallel connected with gate–source. when the printed circuit board (PCB) layout is optimized, the stray inductances can be reduced and Crosstalk will be reduced. However, the effectiveness of this approach is limited and depends on the experience of cabling[2], [3]. Change the drive resistance is another way, so a separate loop GaN driver appears, as shown in Fig. 1. It has the separate sink and source outputs to make it excellent for fast turn off and $\frac{dv}{dt}$ immunity, but drive resistance of this circuit is constant, too large will affect the switching speed and loss, too small will make the oscillation increases[4], [5]. Furthermore, many gate driver circuits have been proposed for suppress crosstalk, such as different variations of resonant gate driver or active clamp gate driver. In [6], The resonant driver can work at high frequency and can reduce the switching losses. However, the higher harmonics was not considered and adds problems with the switching delay in turn-off, In [7], By adding auxiliary switch tube, two kinds of active Miller clamp driving circuits are proposed. Although the better suppression effect is obtained, the circuit complexity and control difficulty has increased.In summary, because of the intrinsic characteristics of GaN power devices, such as low threshold voltage,
narrow driving range, previous researchs of crosstalk suppression merely focus on the overshoot and shoot-through, only a few studies consider reducing both crosstalk and loss under the premise of ensuring the switching speed.

Figure 1. Traditional driver circuit of Si MOSFET and GaN HEMT
This paper proposes a novel active gate driver based on simple loop control to actively suppress crosstalk, which uses one auxiliary triode in series with a capacitor is designated as the gate impedance regulation sink and source loop circuit, By discussing the reason of oscillation in switching process, analyzing its influence on driving, structure, detailed operation process, Finally, the experiments for the proposed gate drive circuit is executed with a simple test circuit and demonstrate the validity and effectiveness of the new gate assist methodology.

2. The Mechanism of Crosstalk in The Drive Circuit
In the high-speed switching process of GaN devices, due to the influence of parasitic capacitance and inductor in the device and circuit, damping oscillation will occur in the driver circuit. Which may cause spike voltages, high-frequency leakage currents, and various electromagnetic interference (EMI). The GaN phase-bridge equivalent model considering parasitic parameters is shown in Fig. 2.

Figure 2. GaN equivalent model considering parasitic parameters
The switching process of the device can be characterized by \( \frac{dv}{dt} \) and \( \frac{di}{dt} \). The oscillation of gate-to-source voltage can be expressed in terms of the oscillation period and the amplitude. When the upper arm Q1 turns on, a high \( \frac{dv}{dt} \) is generated between the drain and source of lower arm Q2. The change rate of voltage forms a Miller current on the Miller capacitance \( C_{GS} \). The faster the switch speed, the bigger the \( \frac{dv}{dt} \). Assuming that the opening time of Q1 is \( t_{on} \), during this time, the DC bus voltage is fully applied to the parasitic capacitances \( C_{GS} \) and \( C_{DS} \), \( V_{GS} \) is approximately equal to \( V_{DC} \). The Miller current can be expressed as:

\[
i = C_{GD} \frac{dv_{GD}}{dt} \approx C_{GD} \frac{dv_{DC}}{dt_{on}}
\]

Due to the gate drive branch in parallel with the gate-source parasitic capacitance \( C_{GS} \), according to Kirchhoff's law:

\[
V_{GS}(S) = \left[ l\left((R_g + S L_g + S L_s)\right) + \frac{1}{S C_{GS}} \right] \frac{C_{GD} V_{DC} \left[ R_g + S(L_g + L_s) \right]}{t_{on} \left[ S^2 C_{GS} (L_g + L_s) + S R_g C_{GS} + 1 \right]}
\]
In equation (2), because the drive resistance $R_g$ is usually several ohms, and $L_G, L_S$ is usually only a few to dozens of nH, so $R_g/(L_G + L_S)$ approaches to infinity. Therefore, the value of $S(L_G + L_S) = SL$ is very small, which can be ignored. The above equation can be simplified as:

$$V_{GS} = C_{GD}V_{DC} \cdot V_{ton} \cdot S \cdot R_g + S + 1$$  

(3)

Analysis of the above equation, transform S-domain to time domain:

1) The denominator is small. when Q1 turns on, the gate-to-source voltage of Q2 will generate damping oscillation. At this moment, $R_g^2C_{GS}^2 - 4L_C G_S < 0$, the smaller $R_g$, the greater $L$, the easier to produce oscillation. With the Laplace inverse transformation of the equation, the amplitude of the gate-to-source voltage oscillation can be obtained as follows:

$$V_{gs} - max = C_{GD}V_{DC} \cdot V_{ton} \cdot C_{GS} \cdot 1 \Rightarrow 1$$

(4)

2) The denominator is large. The turn-on of Q1 causes an exponential decaying form of the ringing disturbance at the gate of Q2. Through the anti-Laplace transform, the maximum oscillation amplitude is:

$$V_{gs-max} = \frac{C_{GD}V_{DC}}{t_{on}C_{GS}}$$

(5)

It can be seen from the above analysis, when Q1 turns off and Q2 turns on, the gate-to-source voltage of Q1 will also occur high-frequency oscillation. If the amplitude of the oscillation voltage reaches the threshold voltage, GaN may be false turn-on.

3. An Improved Active Clamp Gate Drive Circuit

The general schematic circuit of the proposed active Mill clamp gate drive is depicted in Fig. 3. The circuit consists of a conventional drive and two auxiliary triode, two auxiliary capacitor, Among them, the transistor and the capacitor in parallel placed in the turn-on and turn-off path with the main loop resistance. Once gate impedance becomes small during the switching transient, most displacement current will be bypassed by the gate loop, resulting in less current that would induce spurious gate voltage, and thus, crosstalk is mitigated.

![Figure 3. General scheme of the proposed active Mill clamp gate drive](image)

The Fig. 3 only gives the driver circuit of the upper tube, the lower tube drive circuit is similar to the upper, and its working principle as follows:

1) When Q1 turns on, the emitter voltage of the auxiliary PNP triode is higher than the base voltage so that it is in off-state, the auxiliary capacitor $C_1$ is not connected to the driver circuit, does not affect the normal operation of the driver circuit, avoiding the increase of turn-on loss caused by the gate-to-source parallel with the capacitor.

2) When Q1 turns off and Q2 turns on, the Miller current generated by crosstalk flows through the driving resistor to turn on the auxiliary PNP triode, and then the auxiliary capacitor $C_1$ is connected to the circuit. The value of $C_1$ is much larger than $C_{GS}$, which is usually more than 10 times. It provides a low impedance discharge channel for Miller current, and effectively suppresses the positive oscillation voltage of gate-to-source.

3) At the moment of Q2 turns off, the gate-to-source capacitor $C_{GS}$ will discharge and produce a left negative right positive voltage on $R_g$, which also enables the auxiliary PNP triode of Q2 to turn on, and
the auxiliary capacitor $C_1$ is connected to the circuit. This can prevent the switch turn-off too fast, avoiding excessive negative voltage of GaN gate-to-source caused by crosstalk. Operation stages of the novel capacitor-less gate drive circuit are described in Fig. 4.

![Operation stages of the proposed active Mill clamp gate drive circuit](image4.png)

**Figure 4.** Operation stages of the proposed active Mill clamp gate drive circuit

After adding the auxiliary capacitor, by solving the Laplace equation, we can get the gate-source voltage amplitude is about:

$$V_{gs_{-max}} = \frac{C_{gb}V_{dc}}{t_{on}(C_{gs} + C_1)}$$  \hspace{1cm} (6)

Where $C_1$ is a auxiliary capacitor. To satisfy the crosstalk voltage requirements, the gate positive crosstalk voltage must be less than the switch on threshold voltage(1.3V). According to the relationship between the gate-to-source voltage, auxiliary capacitor and voltage change rate, as shown in Fig. 5. We can see that, in order to ensure that the oscillation peak is less than the threshold voltage during fast switching (typically GaN $dv/dt \equiv 100v/ns$), the auxiliary capacitor is at least 10nF.

![The relationship between $V_{gs}$, $C_1$ and $dv/dt$](image5.png)

**Figure 5.** The relationship between $V_{gs}$, $C_1$ and $dv/dt$

### 4. Simulation and Experimental Verification

In order to verify the effect of voltage oscillation suppression by the improved active Miller clamp drive circuit with filter, a GaN half-bridge double-pulse test circuit is set up and the schematic diagram shown in Fig. 2. Both Q1 and Q2 are GaN HEMT GS66504B, the upper tube is the device to be tested, and both devices use the same gate driving circuit. In the experiment, only the gate of Q2 applied the trigger signal, while the gate of the Q1 kept low voltage. Therefore, the gate-to-source voltage oscillation of Q1 is completely caused by the fast switch of lower device.

The voltage waveforms comparison of driving circuit before and after the improvement as can be seen from Fig. 6.
High-speed switching brought severe oscillation and overshoot to the conventional driving circuit and the improved active Miller clamp drive circuit can effectively suppress the interference voltage spikes. When the input voltage is 400V, the forward crosstalk and the negative crosstalk voltage are 1.6V and -4V, respectively, which are 15% and 28% lower than the conventional driving circuit, effectively reducing the risk of shoot-through between upper and lower devices of bridge arms, while avoiding the crosstalk voltage is too large to make the power device failure.

At the same time, in order to verify the correctness of the simulation and the effect of voltage oscillation suppression by the improved active Miller clamp drive circuit with filter, a GaN half-bridge double-pulse test circuit is set up and the schematic diagram shown in Fig. 7.

The experimental waveform before and after improvement is shown in Fig. 8. From the waveform curve, we can see that the voltage oscillations and overshoot of the passive switching transistor gate are significantly improved by using the improved drive circuit.

The experimental results show that: the improved active Miller clamp drive circuit can effectively reduce the risk of shoot-through between upper and lower devices of bridge arms while avoiding the too large crosstalk voltage to make the power device failure.
5. Conclusion
In this paper, the mechanism of high-frequency oscillations and crosstalk on the driving circuit of GaN device are analyzed in detail. Then, a new active Miller clamp driving circuit is proposed. Under the premise of ensuring fast, by adding auxiliary capacitors in different loops to effectively suppress the driving voltage spikes, filter out the higher harmonics, and reduce the risk of short in bridge inverters. Finally, the double pulse test circuit platform is built with GS66504B, and the actual effect of the improved drive circuit is verified by simulation and experiment. The results show that compared with the traditional gate driver, the improved driver can effectively make up for the deficiencies of the original method. The peak voltage of the interference signal is completely suppressed below the threshold voltage. Meanwhile, the addition of auxiliary capacitor can also effectively prevent excessive negative crosstalk and higher harmonics caused by high turn-off speed. Therefore, the improved drive circuit has a high engineering application value.

Acknowledgments
This work was financially supported by the science and technology innovation project of Xichang Satellite Launch Center.

References
[1] R. Mitova, R. Ghosh, U. Mhaskar, D. Klikic, M. X. Wang, and A. Dentella, “Investigations of 600-v gan hemb and gan diode for power converter applications,” IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2441–2452, May 2014.
[2] Youhao Xi, Min Chen, Kim Nielson, and Robert Bell. “Optimization of the drive circuit for enhancement mode power GaN FETs in DC-DC converters,” Twenty-Seventh Annual IEEE Applied Power Electronics Conference & Exposition (APEC), 2012, pp2467-2471
[3] ZHANG Hong,ZHENG Jie-xin,GUO Jian-ping “Research and Development of Driving Technique for GaN Power Device”, Power Electronics, vol.51,no.8, August 2017
[4] Y. Lobsiger and J. W. Kolar, “Closed-loop di/dt and dv/dt IGBT gate driver,” IEEE Trans. Power Electron., vol. 30, no. 6, pp. 3402–3417, Jun. 2015.
[5] J. Rice and J. Mookken, “SiC MOSFET gate drive design considerations,” in Proc. IEEE Int. Workshop Integr. Power Packag., May, 2015, pp. 24–27
[6] P. Anthony, N. McNeill, and D. Holliday, “High-speed resonant gate driver with controlled peak gate voltage for silicon carbide mosfets,” IEEE Trans. Ind. Appl., vol. 50, no. 1, pp. 573–583, Feb. 2014.
[7] Zheng Chen, M. Ilisav Danilovic, Dushan Boroyevich. “Modularized design consideration of a general purpose, high speed phase-leg PEBB based on SiC MOSFETs [A], the 14th European Conference on Power Electronics and Applications [C]. 2011. PP.1-10