Simulation and Analysis of P-P-N 10T SRAM cell for IoT based devices

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Abstract. Ultra low power integrated circuits got the major attention due to its lower power dissipation in the era of Internet of Things (IoT) based smarter devices. In this context, a P-P-N based 10T SRAM cell has been designed and simulated on cadence virtuoso tool with GPDK 45nm technology node at supply voltage ranges from 0.6V to 1V. The various parameters such as static noise margin, read/write power, read/write delay of the 10T SRAM cell are determined out and compared with other considered topologies. It is interesting to notice that 10T SRAM cell shows commendable improvement in read static noise margin (RSNM) i.e. 36% and 46% as compared to conventional 6T and differential 8T SRAM cells respectively. The 10T SRAM cell also has reduction in read power of 38.52% and 38% as compared to conventional 6T and differential 8T SRAM cells respectively. The read delay of P-P-N based 10T SRAM cell is improved by 40% with compared to conventional 6T SRAM cell.

Keywords. IoT, Read power, RSNM, WSNM, read delay, write delay.

1. Introduction
In the new media world, fastest growth of Internet of Things (IoT) based devices provide a lot of advantages to the daily exercises of human life by connecting them with integrated technologies [1]. The outcomes of this integration remove all the hurdles to make anatomy a super character for Cloud Cyber Physical System (CCPS). IoT describes the structure of sensual objects that consist of information’s, different software and several technologies which help devices to interconnect each other and sharing the data among them. CCPS promotes IoT based [2] devices like wireless sensors nodes, embedded technologies, functional software etc. These devices requires low power and high speed memory capacity to access the information and stored the data. The static random access memory (SRAM) is the most prominent device which used to store the data in binary form. SRAM is not like as DRAM which requires refreshing cycle. SRAM occupy lots of space on the SoC in consequences of better performance [3].The power dissipation becomes the main concern in design of SRAM cell. The reduction in power dissipation can be achieved with decline in supply voltage [4]. Random dopant fluctuations (RDF) and line edge roughness (LER) results an increment in the threshold voltage variation. These variations introduce inconsistency between the cross coupled inverters by which read stability and write stability of SRAM cell degrades [5]. A device is called to be more efficient if it is consume very less amount of power. The net power in a CMOS circuit particularly depends upon static and dynamic power .static power occurs when all inputs are hold at particular logic level and circuit is with cut-off supply voltage while dynamic power consumption
occurs due to the swapping mode of charging and discharging of capacitor output load at high deflective frequency [3]. Vital sources of power dissipation in CMOS circuits [6] are as shown in equation (1).

\[ P_{\text{avg}} = P_{\text{switching}} + P_{\text{shortcircuit}} + P_{\text{leakage}} \]  

Where,

\[ P_{\text{avg}} = P_o \cdot V \cdot C_L \cdot f_{\text{CLK}} \]  
\[ P_{\text{shortcircuit}} = I_{\text{SC}} \cdot V_d \]  
\[ P_{\text{leakage}} = I_{\text{leakage}} \cdot V_d \]

The second expression describes the switching power component, where \( P_o \) is used for probability of power spends for overall movement; \( f_{\text{CLK}} \) is the period of frequency; \( C_L \) is equal to load capacitance and \( V_{dd} \) is the supply voltage. The third expression appears as short circuit power where \( I_{\text{SC}} \) used for short circuit current occurs when both pulldown and pullup transistors are on at the same time. These above expressions Eq. (2) and Eq. (3) are the major cause of dynamic power dissipation. The fourth expression denotes to leakage power which mainly depend on leakage current that involve sub-threshold leakage current and reverse biased diode current. The power dissipation reduces when SRAM works under sub-threshold region [7]. The stability of SRAM cell can be investigated on the basis of noise margin [3]. Read noise margin indicates an ultimate quantity of dc noise that can hold by storage node by which the cell remains same. A lot of work has been reported to improve stability of SRAM cells [8-11]. A 10T SRAM cell with 2.9 times improvement in SNM and 20.49 times reduction in power reduction has been reported by using dynamic feedback on 45-nm technology for ultra low power application [12]. Authors used both MOSFET and FinFET on 16nm technology. It also shows better noise margin (SNM) with respect to conventional 6T SRAM cell. Aasheesh Sachdeva et al. [13] reported a novel distributed free 10T SRAM cell by using read/write assist scheme which provides 2.93 times and 1.99 times with preferable RSNM and WSNM with respect to conventional 6T SRAM cell at 0.4V on 45-nm technology. A single ended low power 7T SRAM cell [14] has been proposed with improved RSNM and WSNM by separated storage node and read path. A differential 10T SRAM cell [15] utilized forward body biasing which shows high read current with improved read delay at 0.7V on 45-nm technology node. In view of above mentioned challenges, authors have made an attempt to perform the comparative analysis of PPN based 10T with differential 8T and 6T SRAM cells. In this paper, a perfectly stable differential Read Decoupled structure P-P-N based 10T SRAM cell has been simulated and obtained results are analyzed.

2. **Design Methodology**

2.1. **6T SRAM CELL DESIGN**

Figure 1 shows the 6T SRAM cell. Two back to back inverters are connected to form latch type structure which works as storage cells. To perform write operation, bit-line (bl) is raised to be high. To perform write ‘1’ operation word-line (wl) should be high and connected to VDD. Current passes through access transistors (NM3,NM5) and logic ‘1’ stored at node Q and logic ‘0’ stored at node Qb turn on the PM0 and NM1 transistors. For read operation, wl is raised to be high by which both access transistorsNM3 and NM5 become turn on. Bit-line bar (blb) tends to ground through NM1 transistor
while bl is stand with Vdd following the NM0 transistor to turn off. This operation concluded to read ‘1’ stored in SRAM indicated by the sense amplifier.

![Figure 1. Conventional 6T SRAM cell](image1)

### 2.2 Differential 8T SRAM cell

Differential 8T SRAM cell is shown in Figure 2 [16]. Differential 8T SRAM cell structure consists of basic core latch with two additional buffer transistors i.e. MN5 and MN6 and a tail transistor with complementary wordline (wwlb). This extra circuitry supports an enhancement in RSNM. WWLB and tail transistor manages the power consumption. For performing read operation, BL, BLB and WWL are connected to Vdd. According to the data upon storage nodes (H/L), one from the two buffer transistors (MN5/MN6) becomes on which provide logic ‘0’ at the complementary storage node. For conducting write operation, both access transistors are turned on by connecting to VDD and WWLB to the ground.

![Figure 2. Differential 8T SRAM cell](image2)
2.3 P-P-N Based 10T SRAM cell

The read decoupled P-P-N based 10T SRAM cell is shown in Figure 3. The P-P-N structure consists of three transistors of P-P-N in up to down order in cross-coupled invertors as shown in Fig.3. Transistors QP3, QP1 and QN1 form left side inverter while right side inverter is formed by transistors QP4, QP2 and QN2. The circuit has an additional signal VGND which is connected to the ground at the time of read operation only otherwise connected to VDD. During read power operation, there is need of discharging path to discharge the pre-charged high bit-line which is formed by access transistor QN3 and pull down transistor QN5 by which storage node is directly connected to VGND. At the time of read operation there may be some transient voltage glitch at the pseudo storage node PQ and PQB but if operation is conducting by true storage node there may be better results [17]. The read and write operation of the P-P-N structure are as follows.

![Figure 3. P-P-N 10T SRAM](image)

2.3.1 Read operation.

During read operation, word-line should be high by which both access transistors QN3 and QN4 become on. For discharging the bit-line, VGND is connected to the ground. Initially, it assumed that memory should hold some value so storage node Q stores logic ‘0’ and Qb at logic ‘1’ respectively. Node Q is apart from BL due to QN3 and QP1 transistors which is in the middle of pseudo storage node PQ and true storage node Q. Due to this read current does not flow through storage node Q and get pass through QN5. Due to this, consequently read stability measures of the read decoupled P-P-N based 10T SRAM cell at different supply voltage i.e (0.6V to 1V) are also boost up. The waveform for read logic function for P-P-N based 10T SRAM cell is shown in Figure 4.

2.3.2 Write operation.

During write power operation, word-line (WL) is high by which access transistors QN3 and QN4 are on and BLB is connected to the ground. Initially, data stored at storage node Q is ‘0’ and at Qb is ‘1’. Qb will be pull down directly through the discharging path BLB-QN4-QP2 and swapping of data can occur by charging the node Q [16]. The waveform for write logic function is shown in Figure 5.
3 RESULTS AND SIMULATION.

In this section, results obtained from conventional 6T SRAM, differential 8T SRAM and P-P-N 10T SRAM cells have compared on the basis of read/write power, read/write delay and stability.

3.1 Read/Write power.

The power consumption in the CMOS circuit is a notable parameter [18]. Figure 6 displays that conventional 6T and differential 8T SRAM cells consume more power as compared to the P-P-N based 10T SRAM cell. Although, conv. 6T and Diff. 8T consume relatively equal power at different supply voltages. Figure 6 also reveals that read power of P-P-N 10T SRAM is improved by 38.52% and 38% by conventional 6T and differential 8T SRAM cell at 1V supply voltage. It happens due to VGND signal is fixed at ground during read operation and BL is outlying from the storage node Q. The behavior of write power with variation in supply voltage is expressed in Figure 7. It can be observed that differential 8T SRAM cell consumes less write power as compared to P-P-N 10T SRAM cell. The least write power dissipation is observed in conventional 6T SRAM cell.

| Supply Voltage | Conventional 6T SRAM cell (µW) | Differential 8T SRAM cell (µW) | P-P-N 10T SRAM cell (µW) |
|----------------|-------------------------------|-------------------------------|--------------------------|
| 0.6V           | 0.4291                        | 0.4264                        | 0.28415                  |
| 0.7V           | 1.32                          | 1.327                         | 0.933125                 |
| 0.8V           | 2.3                           | 2.338                         | 1.555                    |
| 0.9V           | 3.517                         | 3.506                         | 2.21                     |
| 1V             | 5.108                         | 5.065                         | 3.14                     |

| Supply Voltage | Conventional 6T SRAM cell (nW) | Differential 8T SRAM cell (nW) | P-P-N 10T SRAM cell (nW) |
|----------------|-------------------------------|-------------------------------|--------------------------|
| 0.6V           | 20.52                         | 24.69                         | 40.69                    |
| 0.7V           | 41.13                         | 39.75                         | 82.41                    |
| 0.8V           | 74.99                         | 60.04                         | 142.23                   |
| 0.9V           | 121.94                        | 87.65                         | 219.5                    |
| 1V             | 178.9                         | 123.3                         | 312.5                    |
3.2 Read Stability.

The read stability of SRAM cell can be defined as the quantity of dc noise that can be bear by memory storing part to keep the data in it [19]. The P-P-N based SRAM gives the great Read static noise margin (RSNM) due to VDD–pre-charged bit-line. The bit-line is connected with VDD that enhance the cell stability. The stability analysis can be performed through dc analysis where noise margin can be measured by inclusive the voltage of bit-line (BL) and data storage node. SNM can be calculated graphically, an appropriate shape of square can be fixed in briefer lobe of the curve or say butterfly curve. Then, length of the square gives the accurate value of RSNM. The read stability of P-P-N 10T SRAM is improved by 1.56 times and 1.86 times at 1V supply voltage in comparison to conventional 6T and differential 8T SRAM cells. Figure 8 shows the comparison between read stability of conventional 6T SRAM, differential 8T SRAM cell and P-P-N 10 T SRAM cell for supply 0.6V to 1V.

Table 3. Comparison of Read Stability for different supply Voltage

| Supply Voltage | Conventional 6T SRAM cell (mV) | Differential 8T SRAM cell (mV) | P-P-N 10T SRAM cell (mV) |
|----------------|--------------------------------|--------------------------------|-------------------------|
| 0.6V           | 130                            | 117                            | 238                     |
| 0.7V           | 150                            | 137                            | 280                     |
| 0.8V           | 165                            | 150                            | 318                     |
| 0.9V           | 203                            | 172                            | 355                     |
| 1V             | 250                            | 210                            | 390                     |

3.3 Write ability.

The write ability of an SRAM can be defined as the quantity of voltage required on bit-cell to complete the appropriate write operation. It can also be define as the energy needed to complete the write operation. Write ability of an SRAM cell can be determine by WSNM. The write ability curve can be generated by integration of both read characteristic and write characteristic curves [17, 19]. The read characteristic curve obtained by inclusion of voltage of bit-line and storage node Q as discussed in above while write characteristic curve can be obtained by inclusion of storage node Q and BL at that time WL is connected to Vdd. Subsequently, a square can be fitted into the smaller lobe of WSNM...
curve obtained by merging of read and write characteristic curves. Figure 9 shows the comparison between write ability of conventional 6T SRAM cell, Differential 8T SRAM cell and P-P-N based 10T SRAM cell for supply voltage 0.6 V to 1V.

Table 4. Comparison of Write Stability for different supply Voltage

| Supply Voltage | Conventional 6T SRAM cell (mV) | Differential 8T SRAM cell (mV) | P-P-N 10T SRAM cell (mV) |
|---------------|-------------------------------|--------------------------------|--------------------------|
| 0.6V          | 234                           | 222                            | 210                      |
| 0.7V          | 264                           | 252                            | 245                      |
| 0.8V          | 296                           | 288                            | 285                      |
| 0.9V          | 333                           | 315                            | 325                      |
| 1V            | 370                           | 355                            | 345                      |

Figure 8. Read Stability at different voltage

Figure 9. Write ability at different voltages

3.4 Read/Write Delay.
Read delay can be define as the time difference between W/L activation and bitline voltage discharge up to half of the VDD. Read delay of P-P-N 10T SRAM is 40% less than Conventional 6T SRAM is shown by Table 5 and Figure 10, while Write delay can be define as the time duration in which data of storage node can be change by cell. Write delay of P-P-N 10T SRAM cell is more than other SRAM cell and can be estimated by Table 6 and Figure 11.

Table 5. Comparison of Read Delay for different supply Voltage

| Supply Voltage | Conventional 6T SRAM cell (pS) | Differential 8T SRAM cell (pS) | P-P-N 10T SRAM cell (pS) |
|---------------|-------------------------------|--------------------------------|--------------------------|
| 0.6V          | 207.5                         | 92.08                          | 208.6                    |
| 0.7V          | 115.32                        | 57.25                          | 77.24                    |
| 0.8V          | 72.0                          | 47.78                          | 52.50                    |
| 0.9V          | 67.81                         | 41.91                          | 45.86                    |
| 1V            | 67.23                         | 36.9                           | 40.52                    |

Table 6. Comparison of Write Delay for different supply Voltage
Supply Voltage | Conventional 6T SRAM cell (pS) | Differential 8T SRAM cell (pS) | P-P-N 10T SRAM cell (pS)
--- | --- | --- | ---
0.6V | 795.6 | 194.5 | 1400
0.7V | 271.1 | 149.9 | 527.6
0.8V | 138.4 | 96.22 | 300.3
0.9V | 95.2 | 74.0 | 224.1
1V | 75.79 | 62.62 | 189.1

**Figure 10.** Read Delay at different voltages  **Figure 11.** Write Delay at different voltage

4. **Conclusion.**
In this work, a comparative analysis between PPN 10T, differential 8T and conventional 6T has been performed by implementing on cadence virtuoso tool at 45nm technology node. The various performance parameters such as read/write power, read/write stability and read/write delay are evaluated. It has been observed that P-P-N 10T SRAM cell has better RSNM and WSNM as compared to conventional 6T as well as differential 8T SRAM cell. Further, read/write delay of 6T SRAM cell is better as differential 8T and PPN 10T SRAM cell. It can be concluded through obtained results that PPN 10 T may be the best choice in terms of stability among considered cells for future applications.

5. **References**

[1] Mali, Amol D. "Recent Domain-Specific Applications of Artificial Intelligence Using IoT." *International Journal on Artificial Intelligence Tools* 28.07 (2019): 1930003.

[2] Cho, Yongseong, et al. "Robot software platform for IoT-based context-awareness." *International Journal of Humanoid Robotics* 14.02 (2017): 1750012.

[3] Sachdeva, Ashish, and V. K. Tomar. "Design of Low Power Half Select Free 10T Static Random-Access Memory Cell." *Journal of Circuits, Systems and Computers* (2020): 2150073, https://doi.org/10.1142/S0218126621500730.

[4] Oh, Tae Woo, et al. "Power-gated 9T SRAM cell for low-energy operation." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 25.3 (2016): 1183-1187.
[5] Ataei, Samira, and James E. Stine. "A differential single-port 8T SRAM bitcell for variability tolerance and low voltage operation." 2015 Sixth International Green and Sustainable Computing Conference (IGSC). IEEE, 2015.

[6] Gupta, Priya, Anu Gupta, and Abhijit Asati. "A Review on Ultra Low Power Design Technique: Subthreshold Logic(2013).

[7] Reddy, T. Vasudeva, and B. K. Madavi. "Designing of schmitt trigger-based architecture 8T SRAM of 256 bit cells under 45 NM technology for low power applications." 2017 International Conference on Intelligent Computing and Control (I2C2). IEEE, 2017.

[8] Sachdeva, Ashish, and V. K. Tomar. "A Schmitt-trigger based low read power 12T SRAM cell." Analog Integrated Circuits and Signal Processing (2020): 1-21, https://doi.org/10.1007/s10470-020-01718-6.

[9] Kumar, Hare Krishna, and V. K. Tomar. "Stability analysis of Subthreshold 6T SRAM cell at 45 nm for IoT application." International Journal of Recent Technology and Engineering (IJRTE) 8.2 (2019).

[10] Sachdeva, Ashish, and V. K. Tomar. "Statistical Stability Characterization of Schmitt Trigger Based 10-T SRAM Cell Design." 2020 7th International Conference on Signal Processing and Integrated Networks (SPIN). IEEE, 2020, DOI: 10.1109/SPIN48934.2020.9071365.

[11] Kumar, Harekrishna, and V. K. Tomar. "A Review on Performance Evaluation of Different Low Power SRAM Cells in Nano-Scale Era." Wireless Personal Communications (2020): 1-26 DoI: 10.1007/s11277-020-07953-4.

[12] Kaur, Navneet, et al. "Low power FinFET based 10T SRAM cell." 2016 Second International Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH). IEEE, 2016.

[13] Aasheesh Sachdeva and V. K. Tomar, "Design of 10-T SRAM cell with improved read performance and expended Write margin” Journal of IET Circuits, Devices and Systems, DOI: 10.1049/iet-cds-2020-0080.

[14] Ensan, Sina Sayyah, et al. "A low-power single-ended SRAM in FinFET technology." AEU-International Journal of Electronics and Communications 99 (2019): 361-368.

[15] Gupta, Rajat, Amit S. Rajput, and Nikhil Saxena. "Improvement in Read Performance of 10T SRAM Cell Using Body Biasing in Forward Bias Regime.

[16] Pal, Soumitra, and Aminul Islam. "Variation tolerant differential 8T SRAM cell for ultralow power applications." IEEE transactions on computer-aided design of integrated circuits and systems 35.4 (2015): 549-558.

[17] Lo, Cheng-Hung, and Shi-Yu Huang. "PPN based 10T SRAM cell for low-leakage and resilient subthreshold operation." IEEE Journal of Solid-State Circuits 46.3 (2011): 695-704.

[18] Sachdeva, Ashish, and V. K. Tomar. "Design of a Stable Low Power 11-T Static Random Access Memory Cell." Journal of circuits, Systems and Computers (2020): 2050206, DOI: 10.1142/S0218126620502060.
[19] Kumar, Harekrishna, and V. K. Tomar. "Design of Low Power with Expanded Noise Margin Subthreshold 12T SRAM Cell for Ultra Low Power Devices." *Journal of Circuits, Systems and Computers* (2020). https://doi.org/10.1142/S0218126621501061.