A high performance 19.2MHz digitally controlled crystal oscillator for NB-IoT

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Abstract. This design implements a 19.2MHz digitally controlled crystal oscillator (DCXO) for the narrow-band internet of things system (NB-IoTs). The paper uses positive feedback principle and phase analysis method to design the oscillator, and then the circuit is realized in a 55nm CMOS technology. The DCXO frequency is controlled by a capacitor matrix controlled by a 10bit digital signal. The results show that the crystal tunable range is more than 70ppm, with tuning step of 0.1~0.2ppm. The phase noise in 1 KHz and 10 KHz offset were -137dBc/Hz and -159dBc/Hz, respectively. The maximum power consumption is 0.72mW at 1.2V power supply voltage, including an output buffer with 0.24mW power consumption.

Key words: Narrow band internet of things (NB-IoT), digital controlled crystal oscillator (DCXO), phase noise

1. Introduction

As a reference frequency source, crystal oscillator is widely used in navigation, radar, handheld telephone and other communication equipment. Its performance is also an important factor that restricts the performance of these communication systems. For example, when a crystal oscillator acts as a PLL reference clock source, its phase noise can directly affect the in-band power spectral density of the local oscillator signal in the communication system. Crystal oscillator’s performance is mainly measured by central frequency, tuning range, start-up time, phase noise, power consumption, area and other technical indicators. Because of the differences in communication systems, they have different requirements for the performance of the reference frequency source. Some systems pay more attention to frequency accuracy and stability, such as in high-precision navigation or military radar systems, while others are more concerned with low-power or low-voltage power supplies, such as wearables and handheld devices. Crystal oscillator circuits can be divided into many types, but their purpose is to ensure that the communication process is carried out efficiently by achieving an accurate and stable target clock. In recent years, with the development of communication technology, the Internet of Things (IoT) technology has developed rapidly. In the meantime, 3GPP has customized the licensed narrow band IoT (NB-IoT) technology standard, which follows the relevant technology of LTE and is likely to become the mainstream standard of the new generation of IoT. Low power consumption, high latency, and low cost technology have become the main technical features. This paper mainly studies the digital
controlled crystal oscillator (DCXO) for NB-IoTs. Low power consumption and low cost are the main features of this design. In order to realize frequency calibration, a digital switch is designed to control the crystal load capacitor to adjust the crystal output frequency [1].

We have consulted the relevant DCXO design literature, which has some inspiration for our design, but these designs cannot fully meet our requirements. In [2]-[3], DCXO for LTE may have more flexible frequency calibration, but its power consumption and area are larger. In [4], an oscillator using the Colpitts structure in RF systems occupies only one chip pin, thus reducing the chip resource consumption. However, such a structure has two drawbacks. First, a fixed bias capacitor needs to be placed on one chip, which greatly increases the utilization of chip resources. Secondly, all the parametric capacitance within the chip (including tuning and fixed capacitors) increases the risk of design and makes the design inflexible [5]-[9]. In this paper, the principle of oscillator is analyzed from the Barkhausen Criterion. The main contributions of this paper are as follows. Firstly, the design principle of crystal oscillator is analyzed from the aspects of phase and positive feedback. At the same time, the S parameters of the crystal resonator were tested and analyzed. Secondly, circuit design and layout design are implemented in the 55nm CMOS process. Finally, the results show that the proposed DCXO has a small area and low power consumption, and thus suitable for NB-IoT system.

2. Digitally Controlled Crystal Oscillator Circuit

2.1. Circuit design

![Schematic of the Crystal Oscillator Circuit](image)

Fig. 1. Schematic of the Crystal Oscillator Circuit

Fig. 1 shows the topology of this circuit. The Pierce oscillator is chosen for this paper. In this structure, Two PADs can be drawn from the NA and NB nodes for the final connection of the crystal and the off-chip bias capacitors Ca and Cb, thus occupying a small chip area and avoiding the change of the center frequency deviation and tuning range caused by putting all capacitors on chip. In addition, a push-pull amplifier with a higher gain can make the circuit start faster. In the circuit, Ct is a tuning capacitor designed in the chip, which is composed of a 10bit digital switched capacitor array. In order to improve the phase noise of the circuit, the metal layer comb capacitor is used as the open-tube capacitor.

2.2. Circuit analysis

In the design of the crystal oscillator circuit, the piezoelectric effect of crystal is equivalent to the model of a series resonant circuit with a parallel capacitor. As shown in the red dotted frame in Fig. 2 R1, C1, L1 is determined by the basic properties of the crystal, and their values depend on the size and shape of the crystal cutting. C0 is the electrostatic capacitance of a crystal, which is determined by the dielectric constant of the crystal material, packaging and parasitic crystal circuit. The crystal model is just a simulation of the crystal piezoelectric effect, so it is difficult to establish a set of RCL values identical to the crystal actually.
Fig. 2 shows a small signal equivalent model of the circuit. For an oscillating circuit, two conditional circuits that satisfy both equations (1) and (2) are required to oscillate.

\[ Av(S) \cdot F(S) \geq 1 \]  
(1)

\[ \Phi(S) = 2\pi n \quad (n=0, 1, 2...) \]  
(2)

In the above formula, \( Av(S) \), \( F(S) \) represent the voltage gain of the amplifier and the feedback network respectively, and \( \Phi(S) \) represents the phase-frequency characteristic of the oscillator. Therefore, at a certain frequency, when the phase reaches \( 2\pi n \) and the voltage gain is not greater than 1, the circuit can oscillate. In order to simplify analysis, we separate amplifier circuit from the feedback network and analyze the oscillation characteristics of the circuit by combining the phase.

For a single-stage amplifier, in general, if the output signal is fed back to the input through a pure impedance network, its closed-loop voltage gain can satisfy the gain condition in equation (1), but its phase cannot reach \( 2\pi n \). Fig. 3 is a small signal equivalent model of the amplifier. Assuming that \( C_{in} \) is the input capacitor of MOS transistor (including the capacitance load of oscillating circuit and the gate capacitance of MOS transistor), \( Z_o \) is the output impedance of the previous stage, the voltage gain of the amplifier can be calculated as formula (3).

\[ Av(S) = \frac{g_m \times R_o}{(R_o \cdot C_b \cdot S + 1)(Z_o \cdot C_{in} \cdot S + 1)} \]  
(3)

Fig. 2. Small signal equivalent model of Crystal Oscillator Circuit

Fig. 3. Effective model of the amplifier
From (3), the amplifier has two poles. In theory, its phase can only reach 360° at the infinite frequency (the negative sign represents a 180° DC phase shift). If we simply understand Zo as the impedance of the feedback network, when Zo is a pure impedance network, actually the phase of the circuit does not reach 2π. But when the feedback is a network with a non-zero reactance, the circuit may oscillate as long as it adds the required phase to the loop.

Fig. 4 shows the S-parameter test results for the 19.2 MHz crystal near the resonance point. It can be seen that the crystal has the largest insertion loss at its resonance point, and there is a phase lag of 14°. When the frequency continues to increase, the insertion loss will gradually decrease and the phase will gradually lag to -90°. In other words, the circuit can oscillate if the crystal provides enough phase for the amplifier at a frequency near the resonant point and the closed-loop gain is still greater than 1. When the circuit starts to oscillate, because the amplitude of the AC signal will continue to increase, the amplitude of the amplifier will gradually reduce the gain, until finally meet \( Av(S) \times F(S) = 1 \) when the circuit to achieve stability. In order to reduce the power consumption of the circuit, this design uses a 4bit digital switch to control the current of the oscillating branch, as shown in Fig. 5(A). By controlling the switch, different resistors are connected to the circuit to control the current of the circuit.

Fig. 5 (B) shows the structure of the capacitor array. The 10-bit digital control register \( T < 9:0 > \) controls the access of 1024 capacitors in the circuit. As shown in Fig. 1, Ca and Cb are fixed biased capacitors. Assuming that the oscillation condition is satisfied, the total capacitance of the NA port increases and the corresponding pole frequency shifts to the lower frequency when some switches of the
capacitor array CT of the NA port are turned on. Therefore, the positive feedback condition of the crystal oscillator circuit will be satisfied at a low frequencies, so that the oscillation frequency will be reduced.

3. Simulation Result

Fig 6. The simulation results of phase noise

Fig 7. The result of transient simulation

Fig 8. The layout of the design
Table 1. Process corner simulation of tuning range

| Tuning range /KHz | ss  | tt  | ff  |
|-------------------|-----|-----|-----|
|                   | 2.77| 2.49| 2.17|

Fig. 6 shows the phase noise simulation results of this design. The results show that the phase noise of the crystal oscillator is -137 dBc/Hz at 1K frequency offset. Fig. 7 is a transient simulation diagram, when the time reaches 0.2ms, the circuit starts to oscillate and reaches an output swing of 1.2V. Table 1 is the frequency migration under different process corner. The frequency migration is the largest under the SS corner, and the frequency change is greater than 70ppm, and each step is less than 0.2ppm. Fig. 8 shows the layout of this design, occupying an area of 0.0169 mm2. The above results show that the circuit structure designed in this paper meets various indicators and is a successful design.

Table 2. Performance comparison

| parament | This paper | Ref. [2] | Ref. [4] | Ref. [5] | Ref. [8] | Ref. [9] |
|----------|------------|----------|----------|----------|----------|----------|
| process  | 55nm CMOS  | 180nm CMOS | 180nm CMOS | 65nm CMOS | 65nm CMOS | MEMS-Based |
| VDD(V)   | 1.2        | 1.2      | 3.3      | 1.2      | 1.2      | 1.5-3.6   |
| Power Consumption ( mW) | <0.72    | 0.0665   | 0.0028   | 9       | 4.5     | N.A.     |
| Center Frequency (MHz) | 19.2    | 16       | 32.768   | 38.4    | 38.4    | 32.768   |
| Tuning step size and range (ppm) | 0.1&70   | 0.2&41   | N.A.     | 2&280   | 0.002&280 | N.A.&100 |
| Phase noise @1KHz(dBc/Hz) | -137    | -137     | -120     | -132    | N.A.    | N.A.    |
| Star-up Time(μs) | 200     | 350      | N.A.     | N.A.    | N.A.    | N.A.    |
| area(mm²) | 0.0169  | 0.19     | 0.34     | 0.09    | 0.09    | 1.3175  |

4. Conclusion
A low phase noise, low power consumption and small area NC crystal oscillator circuit is designed for NB-IoT system by 55nm CMOS process. For the purpose of obtaining more applicable circuit, the Pierce oscillator circuit structure is selected. The center frequency and tuning range can be compromised by adding different load capacitors at both ends of the off-chip crystal, which makes the application of the circuit more flexible. The phase-based analysis method is designed to simplify the calculation of complex crystal oscillation circuit combined with the actual measurement of 19.2 MHz crystal. The results show that the area of DCXO is only 0.0169 mm2, the maximum power dissipation is 0.72 mW, the phase noise is -137 dBc/Hz at the frequency offset of 1 KHz, and the starting time is less than 200 us.

Acknowledgements
This work was supported by Tianjin Science and Technology Committee project No. 17YFZCGX01110.

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