Carbon Nanotubes as FET Channel: Analog Design Optimization considering CNT Parameter Variability

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Abstract: Carbon nanotubes (CNTs), both single-walled as well as multi-walled, have been employed in a plethora of applications pertinent to semiconductor materials and devices including, but not limited to, biotechnology, material science, nanoelectronics and nano-electro mechanical systems (NEMS). The Carbon Nanotube Field Effect Transistor (CNFET) is one such electronic device which effectively utilizes CNTs to achieve a boost in the channel conduction thereby yielding superior performance over standard MOSFETs. This paper explores the effects of variability in CNT physical parameters viz. nanotube diameter, pitch, and number of CNT in the transistor channel, on the performance of a chosen analog circuit. It is further shown that from the analyses performed, an optimal design of the CNFETs can be derived for optimizing the performance of the analog circuit as per a given specification set.

Keywords: Carbon nanotube (CNT), CNT parameters, CNT diameter, CNT pitch, Carbon nanotube field effect transistor (CNFET), Analog Design, Analog design optimization.

1. INTRODUCTION

In the continuous search for better semiconductor materials for the electronic industry, one possibility to incorporate Carbon Nanotubes (CNTs) in a channel region of the standard Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). This not-so-subtle change in the fabrication steps of the MOSFET promises great returns in terms of the transistor’s properties. This is simply because of the fact that the conduction mechanism between the Source and the Drain of the MOSFET would now be governed by the electrostatics of the CNTs rather than the properties of the physical (doped) channel itself. Therefore, a lot of research has been moved towards conclusively proving the superiority of a Carbon Nanotube Field Effect Transistor (CNFET) over its standard M-O-S Field Effect Transistor (MOSFET) counterpart [1]–[6].

With the demonstration of the transcendence of CNFETs over MOSFETs, the stage was set for electronics researchers to devise CNFET-based digital and analog circuits [7]–[14]. The design of high performance analog circuits still remains an active research domain [15]–[22], and the introduction of a ‘better’ transistor has augured well for the analog design community.

The present paper attempts to highlight the issue of selection of various physical parameters...
viz. CNT diameter, CNT pitch, and the number of CNTs in a particular CNFET, for the transistor’s subsequent use in the design of an analog circuit. In particular, an analog device referred to as the Second Generation Current Conveyor (CCII) is chosen as the ‘test’ circuit [23]. Thereafter, extensive simulation analyses have been performed to assess the performance of the ‘test’ analog block under different variations of the CNFET parameters, and a number of useful inferences are thereby derived.

This paper is organized as follows. Section-2 deals with the design details of the analog circuit-under-test. Section-3 explores the performance variability with CNT parameter variation. Section-4 contains a discussion about optimization of the chosen design vis-a-vis the CNT parameters. Concluding remarks are presented in Section-5.

2. ANALOG CIRCUIT UNDER TEST

The analog ‘test’ circuit chosen for the exploration of the effects of CNT parameter variation is a second generation current conveyor (CCII) [23]. CCIIIs have long been the workhorses for current-mode analog systems design, and a variety of bipolar and CMOS implementations are reported. However, not many CNFET-based CCII realizations are reported. Therefore, in this paper, first a new CNFET-based CCII is presented and thereafter the effects of CNT parameter variations are demonstrated on the proposed CNFET CCII.

The circuit symbol of a CNFET and a second generation Current conveyor (CC-II) are given in Fig.1a and Fig.1b respectively. AS can be seen from Fig.1b, the CCII has one high-impedance voltage input (Y), one low-impedance current input (X) and one high-impedance current output (Z+) terminals making it suitable for voltage-mode as well as current-mode circuits [24]. The port relations of the Current conveyor are given in (1). In this work, the circuit of CCII is implemented using Carbon Nanotube-FETs as shown in Fig. 2. For proper operation, all the transistors should operate in the saturation region. The transistors M10 to M13 works as DC current sources and transistors (M1 and M2) serve as a long tail pair. Further, the current mirroring action is achieved by M3 and M4. Also, the equilibrium forces equal currents I_B in the transistors M1 and M2, which is achieved by feedback control resulting in gate-to-source voltages of transistors M1 and M2 to be equalized. It allows the voltage (V_X) to follow the voltage (V_Y). Finally, it is observed that transistors M8 and M9 carry the same drain current as transistor M7, and also transistors M12 and M13 carry the same DC current I_B, the current I_X is conveyed to the I_Z.

Fig. 1. (a) Symbol of CNFET (b) Symbol of CC-II
2.1 Performance of the proposed CNFET CCII

The performance of the proposed CNFET CCII of Fig. 2 was tested with 32 nm Carbon nanotube-FET model through HSPICE simulation. The power supplies were kept at ±0.75 V. The AC, DC and transient analysis have been performed to test the design. Fig. 3 shows the frequency response curves of voltage gain between nodes X and Y. Similarly, Fig. 4 presents the simulation result for the frequency response of current gain ($I_{Z+} = I_X$).

Further, the DC analysis has been carried out to test the functionality of the circuit. The Fig. 5 shows the voltage transfer characteristics of X and Y nodes. It satisfies the relation $V_X = V_Y$. Also, the Fig. 6 represents the input-output DC current transfer characteristics of X and Z+ terminals. Here, the relation $I_{Z+} = I_X$ is verified.
Finally, the transient analysis was also performed. Input-output current responses are illustrated in Fig. 7 which verified the relation $I_{Z^+} = I_X$. Moreover, Fig. 8 presents the transient responses of voltage $V_X$ and $V_Y$ and thus proves $V_X = V_Y$. The design parameters associated with the realization of the circuit of Fig. 2 have been illustrated in Table 1.

Table 1: Design Parameters used in the Design of the CNFET CCII

| Parameters                  | Value  |
|-----------------------------|--------|
| Oxide Thickness ($T_{OX}$)  | 4 nm   |
| Dielectric Constant ($K_{OX}$) | 16     |
| Power Supply                | ±0.9 V |
| Chirality of the tube (n, m) | 19, 0  |
| Physical channel length ($L_{ch}$) | 32 nm |
| No. of tubes in the device  | 6      |
| Pitch (S)                   | 14 nm  |

Lastly, it is important to point out the salient feature of the design. As can be observed from Table 2, while the CMOS design suffered from the requirement of differently sized transistors, the proposed CNFET-based CCII implementation utilizes equal sized transistors thereby facilitating the fabrication process.
3. ANALYSIS OF CNT PARAMETER VARIATION

3.1 Overview of Carbon Nanotube-FET

The structural view of carbon nanotube-FET (CNFET) is similar to MOSFET except for a single CNT or an array of CNTs as the channel material instead of silicon in the MOSFET. The CNFET has several advantages over the conventional MOSFET such as reduction in carrier tunneling and short channel effects, better control over the channel, higher current density, enhanced carrier velocity and reduced leakage currents [25]. The top view of CNFET is shown in Fig. 9. The design parameters of carbon nanotube-FET are: the number of CNTs in transistor channel (N), inter-nanotube space called Pitch (S) and diameter of carbon nanotube (D_{CNT}). The gate length and width are illustrated as L_{gate} and W_{gate} respectively. The CNT’s diameter (D_{CNT}), the width of CNFET-based transistor (W), number of CNTs in channel (N), and inter CNT spacing (S) are related by (2), (3) respectively [26]. The terms n and m are the indexes of chiral vector of Graphene lattice and a = 2.49 Å (lattice constant).

\[ D_{CNT} = \frac{a\sqrt{n^2 + m^2 + nm}}{\pi} \] \hspace{1cm} (2)
\[ W = (N-1)*S + D_{CNT} \] \hspace{1cm} (3)
\[ V_{th} = \frac{aV_s}{qD_{CNT}\sqrt{3}} \] \hspace{1cm} (4)
\[ \sum g = \frac{0.84eV}{D_{CNT}} \] \hspace{1cm} (5)

3.2 Variation in Diameter of CNT

The CNT’s diameter is a material property which depends on the indexes of Graphene lattice (n, m) as given in (2). The threshold voltage and band gap of the device can be controlled by diameter of CNT as illustrated in (4) and (5). Next, the impact of CNT’s diameter variation on the performance of CNFET-based CCII is presented. Fig. 10 presents the response of 3-dB Bandwidth with variation in the diameter of the carbon nanotubes. Further, the effect of diameter on estimated average power of CC-II is depicted by Fig. 11. It is observed as the diameter is incremented from 2–5 nm the power consumption also increased. The numerical values are listed in Table 3.

3.3 Pitch Variation

The pitch of CNT is the inter-spacing between two CNTs. The width of CNFET transistor is affected by the pitch as given in (3). The effect of pitch on the 3-dB bandwidth and estimated average power has also been investigated. The result shows that as the pitch is raised, the 3-dB bandwidth of the proposed CNFET CCII also enhances as presented in Fig. 12. Moreover, a similar effect of pitch on average...
power has been observed and is illustrated in Fig. 13. Table 4 gives the detail analysis of the effects of pitch variation.

**Table 3: Diameter Variation**

| Diameter (nm) | BW (GHz) | Average Power (µW) |
|---------------|----------|--------------------|
| 2.0           | 249.3    | 528                |
| 2.5           | 277.4    | 660                |
| 3.0           | 257.3    | 749                |
| 3.5           | 247.3    | 813                |
| 4.0           | 252.1    | 868                |
| 4.5           | 266.9    | 922                |
| 5.0           | 283.3    | 972                |

**Table 4: Impact of Pitch Variation**

| Pitch (nm) | BW (GHz) | Average Power (µW) |
|------------|----------|--------------------|
| 15         | 249.3    | 528                |
| 20         | 255.6    | 542                |
| 25         | 258.5    | 550                |
| 30         | 260.1    | 554                |
| 35         | 261.1    | 556                |
| 40         | 261.7    | 558                |

**3.4 Variation in Number of CNT**

The number of CNT in a Carbon nanotube-FET has a significant effect on the width of the transistor (3). It has been given in the literature that, drain current of CNFET gets doubled by increasing the CNTs two–fold [9]. Simulation results illustrate that the 3-dB bandwidth and the estimated average power are increased with the number of CNTs. Fig.14 and Fig.15 present the effect of CNT count change on the 3-dB bandwidth and the estimated average power respectively. Furthermore, Table 5 verifies the above discussion.
4. CONCLUDING REMARKS

In this paper, a new CNFET-based CCII is proposed which is less area intensive than its CMOS counterpart and has both voltage- and current-bandwidths well beyond 100 GHz. Effect of CNT parameter variations is then studied and discussed. It was observed that a trade-off exists between the various physical parameters of the CNFET and each transistor in the analog design needs to be individually optimized to get an overall optimal solution.

REFERENCES

[1] S. Fr’egon’ese et.al, “Computationally efficient physics-based compact cntfet model for circuit Design,” Electron Devices, IEEE Transactions on, 55(6):1317–1327, 2008.
[2] A. D Franklin, M. Luisier, Shu-Jen Han, G. Tulevski, C. M. Breslin, L. Gignac, M. S. Lundstrom, and W. Haensch, “Sub-10 nm carbon nanotube transistor,” Nano letters, 12(2):758–762, 2012.
[3] T. Ghani, “Challenges and innovations in nano-cmos transistor scaling,” URL: http://download.intel.com/technology/silicon/Neikei Presentation 2009 Tahir Ghani.pdf, 2009.
[4] Jiale Huang, Minhao Zhu, Shengqi Yang, Pallav Gupta, Wei Zhang, Steven M Rubin, Gilda Garret’on, and Jin He, “A physical design tool for carbon nanotube field-effect transistor circuits,” ACM Journal on Emerging Technologies in Computing Systems (JETC), 8(3):25, 2012.
[5] Huq, Hasina F., Bashirul Polash, Nora Espinoza, and Oscar Machado, “Study of Carbon Nanotube Field Effect Transistors for NEMS,” INTECH Open Access Publisher, 2010.
[6] Ali Javey, Jing Guo, Qian Wang, Mark Lundstrom, and Hongjie Dai. Ballistic carbon nanotube field-effect transistors. Nature, 424(6949):654–657, 2003.
[7] Sujatha Cyril and Dharmistan K Varugheese, “Low power high speed cntfet based differential analog viterbi decoder architecture,” Journal of Theoretical & Applied Information Technology, 56(1), 2013.
[8] Ghorbani, Ali, et al. "A novel full adder cell based on carbon nanotube field effect transistors." International Journal of VLSI Design & Communication Systems 3.3 (2012): 33.
[9] Khizar Hayat, Hammad M Cheema, and Atif Shamim, “Potential of carbon nanotube field effect transistors for analogue circuits,” The Journal of Engineering, 1(1), 2013.
[10] Ikram Ilyas, Niger Fatema, Refaya Taskin Shama, and Fahim Rahman, “Performance evaluation of 32-nm cnt-opamps in analog circuits,” Design and comparison of leapfrog filters. Advanced Materials Research, 646:216–221, 2013.
[11] Aminul Islam, MW Akram, and Mohd Hasan, “Energy efficient and process tolerant full adder in technologies beyond cmos,” International Journal on Communication, 2(2), 2011.
[12] AK Kureshi and Mohd Hasan, “Performance comparison of cnfet-and cmos-based 6t sram cell in deep submicron,” Microelectronics journal, 40(6):979–982, 2009.
[13] Moaieryi, Mohammad Hossein, Keivan Navi, and Omid Hashemipour. "Efficient CNFET-based Rectifiers for Nanoelectronics." International Journal of Computer Applications 64.2 (2013).
[14] Claus, Martin, et al. "High-frequency benchmark circuit design for a sub 50 nm CNTFET technology." Microwave & Optoelectronics Conference (IMOC), 2013 SBMO/IEEE MTT-S International. IEEE, 2013.
[15] Sharma, Jyoti, Mohd Samar Ansari, and Jankiballabh Sharma. "Current-Mode Electronically Tunable Resistor-less Universal Filter in ±0.5 V, 32 nm CNFET." Devices, Circuits and Communications (ICDCCom), 2014 International Conference on. IEEE, 2014.

[16] Ansari, Mohd Samar, and Iqbal A. Khan. "Multiphase differential sinusoidal oscillator based on DVCC." Int. J. of Recent Trends in Engineering and Technology 4.3 (2010): 96-99.

[17] Chaturvedi, Bhartendu, and Sudhanshu Maheshwari. "Second order mixed mode quadrature oscillator using DVCCs and grounded components." International Journal of Computer Applications 58.2 (2012).

[18] Maheshwari, Sudhanshu. "Analogue signal processing applications using a new circuit topology." IET circuits, devices & systems 3.3 (2009): 106-115.

[19] Mohan, Jitendra, and Sudhanshu Maheshwari. "Cascadable current-mode first-order all-pass filter based on minimal components." The Scientific World Journal 2013 (2013).

[20] Tripathi, S. K., and Mohd Samar Ansari. "Voltage-mode universal filter for ZigBee using±0.9 V 32nm CNFET ICC-II." Confluence The Next Generation Information Technology Summit (Confluence), 2014 5th International Conference- IEEE, 2014.

[21] Tripathi, S. K., Mohd Samar Ansari, and Iqbal A. Khan. "Performance Comparison of a Current Conveyor in 0.35 µm & 65 nm CMOS and 32 nm CNFET." Devices, Circuits and Communications (ICDCCom), 2014 International Conference on. IEEE, 2014.

[22] Rahman, Syed Atiqr, and Mohd Samar Ansari. "A neural circuit with transcendental energy function for solving system of linear equations." Analog Integrated Circuits and Signal Processing 66.3 (2011): 433-440.

[23] Hassanein, Wessam S., Inas A. Awad, and Ahmed M. Soliman. "New high accuracy CMOS current conveyors." AEU-International Journal of Electronics and Communications 59.7 (2005): 384-391.

[24] Beg, Parveen, M. A. Siddiqi, and Mohd Samar Ansari. "Multi output filter and four phase sinusoidal oscillator using CMOS DX-MOCCII." International Journal of Electronics 98.9 (2011): 1185-1198.

[25] Wong, H-S. Philip, et al. "Carbon nanotube device modeling and circuit simulation." Carbon Nanotube Electronics. Springer US, 2009. 133-162.

[26] Tripathi, S. K., Md Samar Ansari, and Amit M. Joshi. "Low-Noise Tunable Band-Pass Filter for ISM 2.4 GHz Bluetooth Transceiver in±0.7 V 32 nm CNFET Technology." Proceedings of the International Conference on Data Engineering and Communication Technology. Springer Singapore, 2017.

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