Extraordinary Transport Characteristics and Multivalue Logic Functions in a Silicon-Based Negative-Differential Transconductance Device

Sejoon Lee¹,², Youngmin Lee² & Changmin Kim¹

High-performance negative-differential transconductance (NDT) devices are fabricated in the form of a gated p⁺-i-n⁺ Si ultra-thin body transistor. The devices clearly display a Λ-shape transfer characteristic (i.e., Λ-NDT peak) at room temperature, and the NDT behavior is fully based on the gate-modulation of the electrostatic junction characteristics along source-channel-drain. The largest peak-to-valley current ratio of the Λ-NDT peak is greater than 10⁴, the smallest full-width at half-maximum is smaller than 170 mV, and the best swing-slope at the Λ-NDT peak region is ~70 mV/dec. The position and the current level of the Λ-NDT peaks are systematically-controllable when modulating the junction characteristics by controlling only bias voltages at gate and/or drain. These unique features allow us to demonstrate the multivalue logic functions such as a tri-value logic and a quattro-value logic. The results suggest that the present type of the Si Λ-NDT device could be prospective for next-generation arithmetic circuits.

For the last two decades, several types of novel-functional electronic devices have been proposed and demonstrated on a variety of device architectures so as to huddle up the limitation of conventional complementary metal-oxide-semiconductor (CMOS) devices¹–⁴. For example, one of the most promising scheme is the negative-differential transconductance (NDT) and the negative-differential resistance (NDR) devices, in which quantum mechanical characteristics (e.g., resonant tunneling⁵–⁹, single-electron tunneling¹⁰–¹⁸, band-to-band tunneling¹⁹–²¹ etc.) and/or ambipolar carrier actions²²–²⁵ are implemented. In the operation point of view, the NDT/NDR devices exhibit the extraordinary transfer- and/or output-characteristics. Namely, the devices show a current or a voltage oscillation peak at the specific bias point. This enables us to demonstrate some of astonishing functionalities beyond the binary logic system. For instance, multiple logic functions²⁶–²⁸, multivalued logics²⁹–³¹, and stochastic data processes³² are prominent representatives that can put a step closer to the future electronic computing system. Furthermore, since the usage of the NDT/NDR device allows a high-speed operation of the electronic circuit system (e.g., high-frequency oscillators³³–³⁵, high-speed multiplexers³⁶, ³⁷, and fast logic switches³⁸–³⁹ etc.), exploiting the high-performance NDT/NDR devices could be of major importance in the next-generation ultra-large-scale integration technology. To realize highly-functional NDT/NDR devices, many of emerging materials (e.g., carbon nanotube⁴⁰, graphene⁴¹–⁴³, molybdenum disulfide⁷, ¹², single molecule⁴⁴ etc.) and semiconductor nanostructures have been employed in such a prospective concept of the device scheme. Regardless of the extensive efforts made to replace Si, however, technical and scientific knowledge accumulated on Si still can offer an advantage for rapid innovations⁴², ⁴³. These backgrounds prompt a systematic study on highly-functional Si NDT/NDR devices that are not only compatible to CMOS technology but also reliable for high reproducibility.

In light of this, we have fabricated and characterized the Si NDT transistors that can be utilized for next-generation multivalue arithmetic circuits. In this article, we report data on the extraordinary characteristics of the high performance Si NDT transistors, which were fabricated using a CMOS-compatible device fabrication

¹Department of Semiconductor Science, Dongguk University - Seoul, Seoul, 04623, Korea. ²Quantum-Functional Semiconductor Research Center, Dongguk University - Seoul, Seoul, 04623, Korea. Correspondence and requests for materials should be addressed to S.L. (email: sejoon@dongguk.edu)
process. The electrical transport properties and the multivalue logic functions are thoroughly examined, and the transport mechanisms are discussed in detail.

**Experimental Details**

The NDT devices were fabricated in the form of the gated Si p⁺-i-n⁺-i-n⁺ UTB-channel MOSFET on a silicon-on-insulator (SOI) substrate (\(t_{\text{BOX}} \approx 300 \text{ nm}\)) (left-hand-side panel of Fig. 1(a)). To construct such a device structure, we used the undoped (100) Si layer (\(n_{\text{hole}} \approx 5 \times 10^{15} \text{ cm}^{-3}\)) of the SOI substrate as a starting material. For convenience, we refer the undoped Si layer as i-Si. For the formation of the UTB channel, first, the i-Si layer was thinned down to ~20 nm by successive thermal oxidation and chemical deoxidation. Next, the channel areas (W: 0.3–2.0 μm, L: 2.8 μm) were patterned by using conventional lithography techniques (see the right-hand-side panel of Fig. 1(a)). For further thinning of the SOI thickness (<10 nm), thereafter, we carried out local oxidation of silicon at the channel regions. During this step, ~5-nm-thick gate oxide was created; hence, the thickness of the UTB channel became less than 5 nm while that of the source/drain remained thick enough to minimize parasitic resistances. To prevent the gate leakage, we subsequently deposited an additional silicon dioxide layer (\(t_{\text{ox}} \approx 20 \text{ nm}\)) through the low-pressure chemical vapor deposition method. Then, the p⁺-type drain (\(p \approx 10^{20} \text{ cm}^{-3}\)) and the n⁺-type source (\(n \approx 10^{20} \text{ cm}^{-3}\)) were formed by ion implantation of BF₂⁺ and P⁺, respectively. Finally, the n-type polycrystalline Si gate and the Al electrode were constructed via conventional MOSFET fabrication processes. The electrical properties of the Si p⁺-i-n⁺ UTB-channel MOSFETs were measured at room temperature by using a Keysight B1500A device parameter analyzer and an Agilent DSO-6104A oscilloscope system.

**Results and Discussion**

Figure 1(b) shows the drain current vs. gate voltage (I_D–V_G) characteristic curves at room temperature of the fabricated Si p⁺-i-n⁺ UTB-channel MOSFET. Under the drain-source voltage (V_Ds) of 0.3 V, the device clearly exhibits an N-shape transfer characteristic (i.e., NDT effect) with a \(\Lambda\)-shape peak at V_G = 0–|−0.5| V. For convenience, we refer this peak as a \(\Lambda\)-NDT peak in the present study. The full-width at half-maximum (FWHM) of the \(\Lambda\)-NDT peak is less than 170 mV, and the peak-to-valley current ratio (PVCR) is greater than 10⁴. Such a sharp and prominent \(\Lambda\)-NDT feature can be of great benefit for the high-speed analog circuits and the novel functional digital circuits. As a primary task, thus, understanding the physical mechanism of the clear NDT effect is essential for more feasibility and reproducibility.

We, therefore, firstly explain the transport mechanism of the device to help understand operation schemes of our NDT transistor. Figure 1(c–h) illustrate the carrier transport behaviors of the gated p⁺-i-n⁺ Si-UTB transistor under various bias conditions. At thermal equilibrium, a large built-in potential would be formed at the junction between the drain and the channel because the lightly-doped p⁺ channel becomes an n-type due to the band-bending effect from the work-function difference between the n-type polycrystalline-Si gate (\(\Phi_{\text{gate}} \approx 4.0 \text{ eV}\)) and the n⁺-type source.
and the p'-channel (Φch ~ 4.94 eV for p'-Si). (Fig. 1(c)). In addition, a small hump would be formed at the junction between the channel and the source because of the difference in electron concentrations at the n-channel and the n'-source. The potential barrier at each side will be slightly lowered when the forward bias voltage is applied to the drain-source (i.e., VDS > 0) (Fig. 1(d)). At this bias point, despite no gate bias (i.e., VG = 0), a small current can flow through the channel because of carrier recombination and weak diffusion at both p'−n and n'−n' junctions, respectively (e.g., Point D in Fig. 1(a)).

Here, one can easily create the NDT feature by changing the magnitude of |VG| because the gate driving force is very strong in the UTB-based MOS stack (i.e., explicit control of the accumulation-depletion-inversion modes by |VG| in the UTB-channel MOSFETs)44,45. For example, when applying a negative gate voltage (i.e., VG ≤ 0), I0 will start to increase because |−|VG| reduces the electron concentration at the channel and eventually gives rise to the increase in diffusion/drift currents through the source-channel-drain (Fig. 1(e)) (e.g., Point E in Fig. 1(a)). When the magnitude of |−|VG| further increased (i.e., VG ≪ 0), however, I0 will drastically decrease because |−|VG| accumulates plenty of holes in the channel. Namely, |−|VG| will increase the potential barrier height at the channel-source (i.e., p-n' ) junction as large as the diffusion/drift action could be inhibited (Fig. 1(f)). As a result, the reverse saturation would occur at the channel-source junction; hence, I0 will rapidly decrease at VG (e.g., Point F in Fig. 1(a)). Such a sudden drop of I0 causes a Λ-NDT phenomenon in the present type of the NDT transistor.

Through keeping on increasing −|VG| (i.e., VG ≪ 0), the electrons can transfer from the source to the channel via band-to-band tunneling (BTBT). In other words, the BTBT event will occur under −|VG| because large −|−|VG| populates the channel with abundant hole carriers as much as the depletion width becomes thin enough to allow BTBT to the p'−n' junction (Fig. 1(g)). At this bias stage, I0 will significantly increase due to both the hole drift at p'−n' and the electron tunneling event at p'−n' (e.g., Point G in Fig. 1(a)). All of the above allows the gated Si p'−i−n' UTB-channel MOSFET to exhibit the N-shape transfer characteristic in the negative VG region. At the positive VG region (i.e., VG > 0), the value of IG will remain low (e.g., Point H in Fig. 1(a)) because +VG-induced electrons in the channel increases potential barriers at the drain-channel (i.e., p'−n junction) (Fig. 1(h)).

Here, we point out the statistical uncertainty of BTBT at the higher |VG| region (e.g., at |VG| ≫ −2 V in Fig. 1(a)). To perform BTBT, in fact, four necessary and sufficient conditions must be simultaneously satisfied: (i) the occupied energy states should exist in the reservoir to supply charge carriers, (ii) the unoccupied states also should exist in the charge collection region, (iii) the tunnel barrier width should be thin enough to ensure a finite tunneling probability, (iv), the momentum must be conserved during tunneling events. When fabricating the integrated circuit, however, the BTBT probability in semiconductor junction devices would be different from each other because the above conditions are very sensitive to both the energy perturbation and the thermal fluctuation. As a result, the tunneling current will be non-identical for every device, leading to a vague output in the integrated circuit.

On the other hand, the NDT effect at the Λ-shaped peak region (e.g., at VG = 0−[0.5] V in Fig. 1(a)) is reliable and reproducible for every device because the behavior occurs on the basis of only gate-controlled ambipolar carrier actions at the junction areas (i.e., gate control of recombination → diffusion/drift → reverse saturation), as discussed earlier. Furthermore, fast switching of the positive-negative differential transconductance at the Λ-shaped peak region is beneficial for future high-speed and functional circuit applications. Therefore, from now on, we emphasize the features of the Λ-NDT peaks, which can be effectively demonstrated and modulated by junction dynamics in the device.

From the Si p'−i−n' gated-transistors fabricated through the aforementioned procedures, more than 65% of the devices showed clear NDT characteristics at room temperature. As shown in Fig. 2(a–f), the devices clearly exhibit the Λ-NDT peak in their transfer characteristic curves. Regardless of the channel size (i.e., W/L), the Λ-NDT peak clearly appears at VG = [0−0.5] V, while the peak current increases with increasing channel width. This verifies our NDT transistors to hold promise for future CMOS-compatible novel functional circuit applications. The magnitude of PVR is no less than 104 for all devices, and the value of FWHM is~175 mV on average. This verifies our NDT transistors to hold promise for future CMOS-compatible novel functional circuit applications. Therefore, from now on, we emphasize the features of the Λ-NDT peaks, which can be effectively demonstrated and modulated by junction dynamics in the device.

Since the junction-depletion characteristics depend on both the Fermi potential inside the channel and the built-in potential at the channel edge, one may expect that the Λ-NDT conditions (i.e., recombination → diffusion/drift → reverse saturation) can be modulated by controlling either of VG or VDS. We, accordingly, measured the IG−VG characteristics at various VDS to investigate the effect of bias conditions on the modulation of Λ-NDT peaks (Fig. 3). As the magnitude of +VDS increases, the peak current at the Λ-NDT region is exponentially increased because the large +VDS enhances the drift action at the source-channel-drain junction. In addition, the Λ-NDT peak position systematically shifts toward the lower |VG| region with increasing +VDS (see also the inset of Fig. 3).

The precise control of NDT peaks in our Si p'−i−n' UTB MOSFET is quite similar to that in highly-functional single electron/hole transistors that were devised with ultra-small quantum dots (e.g., dQD < 5 nm)13–18. In this otherwise quantum nature-free NDT device (e.g., no quantum dot etc.), however, we explicitly demonstrated the systematic modulation of the Λ-NDT peak through only controlling the electrostatic junction characteristics. Namely, the position and the magnitude of the Λ-NDT peak can be precisely controlled through modifying the potential profile for the NDT condition25. For instance, when a lower |+VDS| is applied to the device, a larger |−|VG| is necessary to accumulate plenty of holes in the channel for performing the Λ-NDT phenomenon (i.e., switching of diffusion/drift → reverse saturation' by |−|VG|), and vice versa at a higher |+VDS|.

When using the NDT device for the electronic circuits, the values of PVR and FWHM play key factors because these are closely related to both the on/off ratio and the switching speed of the device. Thus, we assess the dependences of PVR and FWHM on the bias conditions. As can be seen from Fig. 4(a), the bias voltage of VDS strongly affects the value of PVR. With increasing VDS up to 0.3 V, the magnitude of PVR increases and reaches ~2 × 104, whereas that monotonically decreases when VDS exceeds 0.35 V. This can be explained by the
variation of the off-current upon varying $V_{DS}$. When $V_{DS}$ is low (e.g., $V_{DS} \ll 0.3$ V), the built-in potential at the channel-source junction ($V_{bi(c,s)}$) is still high enough to cut off the carrier transport through the channel (i.e., off-current = very low) (Fig. 4(b)). In this case, since the on-current increases with increasing $V_{GS}$ (e.g., up to 0.3 V), the magnitude of PVCR becomes higher. When $V_{GS}$ is high (e.g., $V_{DS} > 0.3$ V), however, the barrier height of $V_{bi(c,s)}$ is decreased as low as a few of electrons can flow from the source to the channel (i.e., off-current = low) (Fig. 4(c)). In this case, the value of off-current becomes higher and higher with increasing $V_{DS}$. Hence, the magnitude of PVCR decreases in spite of the increase in on-current at higher $V_{DS}$. Different from the behavior of PVCR, the effect of $V_{DS}$ is insignificant on the magnitude of FWHM (Fig. 4(a)) because the capacitive coupling strength of the UTB gate stack is much stronger than that of the drain-channel-source junction.

Another important factor of the NDT device is its $V_{GS}$-tunable swing-slope (SS) at the NDT peak region because SS is a key parameter of the device performance to produce a high speed on/off operation upon the input signals. The dependences of $SS$ values on $V_{DS}$ are shown in Fig. 5. The swing slopes at both the positive- and the negative-differential conductance regions (i.e., $SS_{sep}$ and $SS_{shun}$) show a similar behavior because those are mostly influenced by strong gate-tuning of $V_{bi(c,s)}$ (i.e., fast switching of on/off operations by $V_{GS}$ in the UTB gate stack) (see the inset of Fig. 5). The best value of $SS$ is ~70 mV/dec at $V_{DS} < 0.35$ V, which is comparable to that in the state-of-the-art Si MOSFETs. When $V_{DS}$ exceeds 0.4 V, however, the value of $SS$ begins to increase because of the increased off-current at higher $V_{DS}$ as discussed above.

Figure 6 shows the $I_{DS}-V_{DS}$ characteristic curves of the device at various $V_{GS}$ near the $\Lambda$-NDT peak region. At $V_{GS} = 0$ V, the device exhibits a typical diode-like feature because the p-i-n junction is formed along the drain-channel-source region. As the magnitude of $|V_{GS}|$ increases up to $|−0.4|$ V, the turn-on voltage decreases and the on-state current increases because $V_{GS}$ would induce hole accumulation in the channel and could reduce total $V_{bi}$ along drain-channel-source (i.e., p-i-p-n$^-$). When $|V_{GS}|$ is further increased ($>−0.5$) V), however, the turn-on voltage rapidly increases because the large magnitude of $|V_{GS}|$ would accumulate more holes inside the channel area; hence, total $V_{bi}$ would increase particularly at the junction between channel and source (i.e., p$^+$-n$^-$). In addition, the device also displays the current staircases (CSs) at $V_{GS} = −0.5$ to $0.7$ V (see the inset of Fig. 6) due to the suppression of carrier conduction at the NDT region. As $|V_{GS}|$ increases for the range of CS becomes wide, and the current level of the plateau goes down. Namely, the knee position of CS shifts stepwise toward the lower $V_{DS}$ and the lower $I_{DS}$.

The stepwise-shifts of both NDT peaks and CS plateaus are useful for the circuit application of the NDT device because it can provide multiple operation points for logical functions at a wide range of voltages. Such remarkable tunabilities of NDT and CS can be traced at a glance by measuring the charge diagram of the device. As can be seen from the contour plot of $I_{DS}$ as functions of both $V_{GS}$ and $V_{DS}$ (Fig. 7), both the $\Lambda$-NDT and the CS characteristics are systematically modulated by $V_{GS}$ and $V_{DS}$. For example, at the fixed $V_{DS}$ (e.g., $V_{DS}=0.3$ V), the color of $I_{DS}$ is changed along $|V_{GS}|$ direction (i.e., white → gray → black → gray → white). This corresponds to the $|V_{GS}|$-dependent change in the current level of $I_{DS}$, indicating the appearance of the $\Lambda$-shaped I$_{DS}$ peak (i.e., $\Lambda$-NDT). As the magnitude of $V_{DS}$ increases, the $\Lambda$-NDT region is extended toward the A direction. The extended $\Lambda$-NDT region is fairly long and inversely cuspidal, where the stepwise shifts of the $\Lambda$-NDT peaks and the CS plateaus occur, as confirmed in Figs 3 and 6.
Thanks to the appearance of the extended Λ-NDT peak region, one can choose many of the operation points from a unit device for the demonstration of multivalue logic functions. For example, when using our NDT device as a one-transistor logic gate, two input-bias voltages (i.e., $V_{IN1} = V_G$ and $V_{IN2} = V_D$) can be selected at specific bias points for demonstrating different multivalue logic functions (see also Fig. 8(a)). Following this way, as depicted in Fig. 7, a tri-value and a quattro-value logic functions can be chosen as possible examples of one-transistor multivalue logics. Figure 8(b) and (c) display the measured transient waveforms of the tri-value and the quattro-value logics, respectively. The voltage output ($V_{OUT}$) clearly reveals a sequential count function of the multivalue upon varying $V_G$ ($= V_{pulse1}$) and $V_D$ ($= V_{pulse2}$). Although the output-voltage level is quite low because of the low current level at the NDT region, we believe that the multivalue logic functions can be effectively used for future highly-sensitive low-power arithmetic circuits.

Figure 3. Dependence of the Λ-NDT characteristics on $V_{DS}$ ranging from 0.05 to 0.65 V. The inset displays a semi-logarithmic plot of $I_D$-$V_G$ curves at $V_{DS} = 0.05-0.65$ V.

Figure 4. (a) PVCR and FWHM of the Λ-NDT peaks as a function of $V_{DS}$. (b–c) Potential profiles along the drain-channel-source region at different $V_{DS}$ bias conditions: (b) Lower $V_{DS}$ (e.g., $V_{DS1} \leq 0.3$ V) and (c) Higher $V_{DS}$ (e.g., $V_{DS2} \geq 0.35$ V). The rightmost graph of $n_0 (E)$ vs. $E'$ represents the electron distribution function of n$^+$-Si at room temperature.
Finally, we briefly state the speed limit of the NDT-based multivalue logic circuits. In our device, the channel conductance near the $\Lambda$-NDT peak is in the order of $10^2 \text{nS}$, which corresponds to the junction resistance ($R_J$) of a few of hundreds $\text{M\Omega}$. In addition, the junction capacitance ($C_J \approx \frac{1}{2} \frac{q}{kT} \tau_{IDQ^51}$, where $k$ is the Boltzmann constant, $T$ is the environmental temperature, $I_{DQ}$ is the driving current at an operation point, and $\tau$ is the carrier lifetime) is determined to be $\sim 2 \text{fF}$, when assuming $\tau = 10^{-7} \text{s}^51$. Furthermore, since the gate capacitance ($C_g = W \cdot L \cdot k_{ox} \frac{\varepsilon_0}{t_{ox}}$) is $\sim 1.2 \text{fF}$ for the present device ($W = 0.3 \text{\mu m}$, $L = 2.8 \text{\mu m}$, $t_{ox} = 25 \text{nm}$), the time constant ($\approx R_J C_J$) of our $\Lambda$-NDT device can be estimated to be less than $0.1 \text{\mu s}$. We can, therefore, deduce the intrinsic speed of the device to be no less than several tens of MHz. Although the intrinsic speed limit seems little low, the implementation of high-mobility device architectures (e.g., nanowire- or nanosheet-channel MOSFETs with a gate-all-around stack) to the present type of the NDT device can be the next step to improve the speed of the NDT-based one-transistor multivalue logic circuits.

Conclusion
The NDT devices were fabricated in the form of the Si $p^+\text{-i}-n^+$ UTB-channel MOSFETs. The devices clearly showed a $\Lambda$-shape NDT peak, at room temperature, with the extremely large PVCR ($>10^4$) and the small FWHM ($<170 \text{mV}$). These features were universal for multiple devices that had been fabricated using an identical method (i.e., yield $\sim 65\%$). The best value of $SS$ at the $\Lambda$-shape NDT peak region was $\sim 70 \text{mV/dec}$. In addition, the $\Lambda$-NDT peaks were confirmed to be effectively modulated through the control of the junction characteristics by changing only $V_G$ and/or $V_{DS}$. Owing to the systematic modulation of the $\Lambda$-NDT peaks, we successfully demonstrated the
multivalue logic functions (e.g., tri-value and quattro-value logics) on a single device as a one-transistor multivalue logic gate. These may offer potential applications for low power/high speed multivalue logics beyond the ordinary binary logic system.

References
1. Ferain, I., Colinge, C. A. & Colinge, J.-P. Multigate Transistors As the Future of Classical Metal–Oxide–Semiconductor Field-Effect Transistors. *Nature* **479**, 310–316 (2011).
2. Ionescu, A. M. & Riel, H. Tunnel Field-Effect Transistors As Energy-Efficient Electronic Switches. *Nature* **479**, 329–337 (2011).
3. Morton, J. J. L., McCormac, D. R., Eriksson, M. A. & Lyon, S. A. Embracing the Quantum Limit in Silicon Computing. *Nature* **479**, 345–353 (2011).
4. Venema, L. Silicon Electronics and Beyond. *Nature* **479**, 309–309 (2011).
5. Naquin, C. *et al.* Negative Differential Transconductance in Silicon Quantum Well Metal–Oxide–Semiconductor Field-Effect/Bipolar Hybrid Transistors. *Appl. Phys. Lett.* **105**, 213507 (2014).
6. Naquin, C. *et al.* Gate Length and Temperature Dependence of Negative Differential Transconductance in Silicon Quantum Well Metal–Oxide–Semiconductor Field-Effect Transistors. *J. Appl. Phys.* **118**, 124505 (2015).
7. Campbell, P. M., Tarasov, A., Joiner, C. A., Ready, W. J. & Vogel, E. M. Enhanced Resonant Tunneling in Symmetric 2D Semiconductor Vertical Heterostructure Transistors. *ACS Nano* **9**, 5000–5008 (2015).
8. Sharma, P., Bernard, L. S., Bazigos, A., Magrez, A. & Ionescu, A. M. Room-Temperature Negative Differential Resistance in Graphene Field Effect Transistors: Experiments and Theory. ACS Nano 9, 620–625 (2015).
9. Britnell, L. et al. Resonant Tunnelling and Negative Differential Conductance in Graphene Transistors. Nat. Commun. 4, 1794 (2013).
10. Wang, M. et al. Quantum Dot Behavior in Bilayer Graphene Nanoribbons. ACS Nano 5, 8769–8773 (2011).
11. Stampfer, C. et al. Tunable Graphene Single Electron Transistor. Nano Lett. 8, 2378–2383 (2008).
12. Lee, K., Kulkarni, G. & Zhong, Z. Coulomb Blockade in Monolayer MoS2 Single Electron Transistor. Nanoscale 8, 7755–7760 (2016).
13. Lee, S., Lee, Y., Song, E. B. & Hiramoto, T. Observation of Single Electron Transport via Multiple Quantum States of a Silicon Quantum Dot at Room Temperature. Nano Lett. 14, 71–77 (2014).
14. Lee, Y., Lee, S. & Hiramoto, T. Transport Behaviors and Mechanisms in Cuspidal Blockade Region for Silicon Single-Hole Transistor. Curr. Appl. Phys. 14, 428–432 (2014).
15. Lee, S., Lee, Y., Song, E. B. & Hiramoto, T. The Characteristic of Elongated Coulomb-Blockade Regions in a Si Quantum-Dot Device Coupled via Asymmetric Tunnel Barriers. J. Appl. Phys. 114, 164513 (2013).
16. Lee, S., Lee, Y., Song, E. B. & Hiramoto, T. Modulation of Peak-to-Valley Current Ratio of Coulomb Blockade Oscillations in Si Single Hole Transistors. Appl. Phys. Lett. 103, 105302 (2013).
17. Lee, S. & Hiramoto, T. Strong Dependence of Tunneling Transport Properties on Overdriving Voltage for Room-Temperature-Operated Single Electron/Hole Transistors Formed with Ultranarrow [100] Silicon Nanowire Channel. Appl. Phys. Lett. 93, 043508 (2008).
18. Lee, S., Miyaji, K., Kobayashi, M. & Hiramoto, T. Extremely High Flexibilities of Coulomb Blockade and Negative Differential Conductance Oscillations in Room-Temperature-Operating Silicon Single Hole Transistor. Appl. Phys. Lett. 92, 073502 (2008).
19. Zhang, P. et al. Strong Room-Temperature Negative Conductance in an Axial Si/Ge Hetero-Nanowire Tunnel-Field Effect Transistor. Appl. Phys. Lett. 105, 062106 (2014).
20. Ramesh, A., Berger, P. R. & Loo, R. High 5.2 Peak-to-Valley Current Ratio in Si/Ge Resonant Interband Tunnel Diodes Grown by Chemical Vapor Deposition. Appl. Phys. Lett. 100, 092104 (2012).
21. Ramesh, A. et al. Boron Delta-Doping Dependence on Si/Ge Resonant Interband Tunneling Diodes Grown by Chemical Vapor Deposition. IEEE Trans. Electron Dev. 59, 602–609 (2012).
22. Mueller, E., Konstantaras, G., Spruijtenburg, P. C., van der Wiel, W. G. & Zwanenburg, F. A. Electron–Hole Confinement Symmetry in Silicon Quantum Dots. Nano Lett. 15, 5336–5341 (2015).
23. Bett, A. C., Gonzalez-Zaiba, M. P., Podd, G. & Ferguson, A. J. Ambipolar Quantum Dots in Intrinsic Silicon. Appl. Phys. Lett. 105, 153113 (2014).
24. Lee, S., Lee, Y., Song, E. B., Wang, K. L. & Hiramoto, T. Gate-Tunable Selective Operation of Single Electron/Hole Transistor Modes in a Silicon Single Quantum Dot at Room Temperature. Appl. Phys. Lett. 102, 083504 (2013).
25. Kim, C., Lee, Y. & Lee, S. Systematic Modulation of Negative-Differential Transconductance Effects for Gated p−n+n− Silicon Ultra-Thin Body Transistor. J. Appl. Phys. 121, 124504 (2017).
26. Mongillo, M., Spathis, P., Katsaros, G., Gentile, P. & De Franceschi, S. Multifunctional Devices and Logic Gates With Undoped Silicon Nanowires. Nano Lett. 12, 3074–3079 (2012).
27. Maeda, K. et al. Logic Operations of Chemically Assembled Single-Electron Transistor. ACS Nano 6, 2798–2803 (2012).
28. Lee, Y., Lee, S., Im, H. & Hiramoto, T. Multiple Logic Functions from Extended Blockade Region in a Silicon Quantum-Dot Transistor. J. Appl. Phys. 117, 064501 (2015).
29. Lee, C. K., Kim, S. I., Shin, S. J., Choi, J. B. & Takahashi, Y. Single-Electron-Based Flexible Multivalued Logic Gates. Appl. Phys. Lett. 92, 093101 (2008).
30. Kim, S.-J. et al. Single-Electron-Based Flexible Multivalued Exclusive-Logic Gate. IEEE Trans. Electron Dev. 56, 1048–1055 (2009).
31. Gan, K.-J., Tsai, C.-S., Chen, Y.-W. & Yeh, W.-K. Voltage-Controlled Multiple-Valued Logic Design Using Negative Differential Resistance Devices. Solid State Electron. 54, 1637–1640 (2010).
32. Nishiguchi, K., Ono, Y., Fujiwara, A., Inokawa, H. & Takahashi, Y. Stochastic Data Processing Circuit Based on Single Electrons Using Nanoscale Field-Effect Transistors. Appl. Phys. Lett. 92, 062105 (2008).
33. Feiginov, M., Sydla, C., Cojocari, O. & Meissner, P. Resonant-Tunnelling Diode Oscillators Operating at Frequencies Above 1.1 THz. Appl. Phys. Lett. 99, 233506 (2011).
34. Lee, J. & Yang, K. An On-Off Mode RTD Oscillator Operating at Extremely Low Power Consumption. IEEE Trans. Nanotechnol. 11, 863–865 (2012).
35. Lee, K., Lee, J., Park, J. & Yang, K. A Novel Ku-Band RTD-Based Quadrature VCO for Low Power Applications. IEEE Microw. Wireless Compon. Lett. 25, 326–330 (2015).
36. Choi, S., Jeong, Y., Lee, J. & Yang, K. A Novel High-Speed Multiplexing IC Based on Resonant Tunneling Diodes. IEEE Trans. Nanotechnol. 8, 482–486 (2009).
37. Lee, J., Choi, S. & Yang, K. 40 Gb/s Low-Power 4:1 Multiplexer Based on Resonant Tunneling Diodes. IEEE Tran. Nanotechnol. 11, 890–895 (2012).
38. Liu, G., Ahsan, S., Khitun, A. G., Lake, R. K. & Balandin, A. A. Graphene-Based Non-Boolean Logic Circuits. J. Appl. Phys. 114, 154310 (2013).
39. Núñez, I., Avedillo, M. J. & Quintana, J. M. Two-Phase RTD-CMOS Pipelined Circuits. IEEE Trans. Nanotechnol. 11, 1063–1066 (2012).
40. Lee, J. S., Park, J.-W., Song, J. Y. & Kim, J. Asymmetric Magnetococonductance and Magneto-Coulomb Effect in a Carbon Nanotube Single Electron Transistor. Nanotechnology 24, 195201 (2013).
41. Perrin, M. L. et al. Large Negative Differential Conductance in Single-Molecule Break Junctions. Nat. Nanotechnol. 9, 830–834 (2014).
42. Oda, S. & Ferry, D. K. Silic on Nanoelec onics (Taylor & Francis, New York, 2006).
43. Ono, Y., Fujiwara, A., Nishiguchi, K., Inokawa, H. & Takahashi, Y. Manipulation and Detection of Single Electrons for Future Information Processing. J. Appl. Phys. 97, 031101 (2005).
44. Fenuillet-Beranger, C., Skotnicki, T., Monfay, S., Carriere, N. & Boeuf, F. Requirements for Ultra-Thin-Film Devices and New Materials for the CMOS Roadmap. Solid State Electron. 48, 961–967 (2004).
45. Md Arshad, M. K. et al. UTBB SOI MOSFETs Analog Figures of Merit: Effects of Ground Plane and Asymmetric Double-Gate Regime. Solid State Electron. 90, 56–64 (2013).
46. Collinge, J. P. et al. Nanowire Transistors without Junctions. Nat. Nanotechnol. 5, 225–229 (2010).
47. Chang, H. Y., Adams, B., Chien, P. Y., Li, J. & Woo, J. C. S. Improved Subthreshold and Output Characteristics of Source-Pocket Si Tunnel FET by the Application of Laser Annealing. IEEE Trans. Electron Dev. 60, 92–96 (2013).
48. Lu, H. & Seabough, A. Tunnel Field-Effect Transistors: State-of-the-Art. IEEE J. Electron Devices Soc. 2, 44–49 (2014).
49. Lee, B.-H. et al. Vertically Integrated Multiple Nanowire Field Effect Transistor. Nano Lett. 15, 8056–8061 (2015).
50. Kuo, Y. F., Lin, Y. J. & Chao, T. S. Implantation Free GaA Double Spacer Poly-Si Nanowires Channel Junctionless FETs with Sub-1V Gate Operation and Near Ideal Subthreshold Swing. Proc. IEEE Int. Electron Devices Meeting 631–634 (2015).
51. Taur, Y. & Ning, T. H. Fundamentals of Modern VLSI Devices, 2nd ed. (Cambridge University Press, Cambridge, 2009).
52. Moon, D. L., Choi, S. I., Duarte, J. P. & Choi, Y. K. Investigation of Silicon Nanowire Gate-All-Around Junctionless Transistors Built on a Bulk Substrate. IEEE Trans. Electron Devices 60, 1355–1360 (2013).
53. Fang, W. et al. Impact of the Effective Work Function Gate Metal on the Low-Frequency Noise of Gate-All-Around Silicon-on-Insulator NWFETs. IEEE Electron Device Lett. 37, 363–365 (2016).
54. Al-Ameri, T. et al. Impact of Quantum Confinement on Transport and the Electrostatic Driven Performance of Silicon Nanowire Transistors at the Scaling Limit. Solid State Electron. 129, 73–80 (2017).
55. Thirunavukkarasu, V. et al. Gate-All-Around Junctionless Silicon Transistors with Atomically Thin Nanosheet Channel (0.65 nm) and Record Sub-Threshold Slope (43 mV/dec). Appl. Phys. Lett. 110, 032101 (2017).

Acknowledgements
This research was supported by the National Research Foundation of Korea through Basic Science Research Programs (NRF-2014R1A2A1A11050882, NRF-2016R1A6A1A03012877, and NRF-2017R1A2B4004281) funded by the Korean government.

Author Contributions
S.L. designed the experiments and wrote the main manuscript text. Y.L. and C.K. fabricated the samples and performed their electrical measurements. All authors analyzed the results and reviewed the manuscript.

Additional Information
Competing Interests: The authors declare that they have no competing interests.

Publisher’s note: Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Open Access
This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license, and indicate if changes were made. The images or other third party material in this article are included in the article’s Creative Commons license, unless indicated otherwise in a credit line to the material. If material is not included in the article’s Creative Commons license and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this license, visit http://creativecommons.org/licenses/by/4.0/.

© The Author(s) 2017