Abstract— In this paper, we have worked out a pseudo two dimensional (2D) analytical model for surface potential and drain current of a long channel p-type Dual Material Gate (DMG) Gate All-Around (GAA) nanowire Tunneling Field Effect Transistor (TFET). The model incorporates the effect of drain voltage, gate metal work functions, thickness of oxide and silicon nanowire radius. The model does not assume a fully depleted channel. With the help of this model we have demonstrated the accumulation of charge at the interface of the two gates. The accuracy of the model is tested using the 3D device simulator Silvaco Atlas.

Index Terms— Dual Material Gate (DMG), Gate All-Around (GAA), Tunneling Field Effect Transistor (TFET), nanowires, Two dimensional (2D) modelling. Sub-threshold swing (SS), ON-state current.

I. INTRODUCTION

Studies on novel device structures for VLSI applications is being done extensively these days to provide alternatives to conventional CMOS transistors. This is because MOSFETs scaled to lengths below 100 nm face several problems with regard to leakage currents in the OFF-state, subthreshold swing (SS), drain induced barrier lowering (DIBL) and numerous other short channel effects (SCE). An attractive alternative is TFET [1-6], which has SS below 60 mV/decade, low OFF-state leakage currents and diminished short channel effects (SCE). However, since the source of carriers is band to band tunneling, TFETs have a low ON-state current $I_{ON}$ [3] and it does not meet ITRS requirements [7-9]. Also, a gate all around (GAA) structure provides an improved SS and a solution to SCE and DIBL [10-12] because of the better electrostatic control over the channel. Further, a higher $I_{ON}$ per unit device area is achieved due to the device geometry [13-15]. However, the problems of delayed saturation, low $I_{ON}$ and leakage currents remain in a GAA structure. Thus, to optimize the GAA structure, a Dual Material Gate (DMG) structure is proposed in [16]. A DMG GAA nanowire TFET (Fig. 1) has a tunneling gate with a work function lower than that of the auxiliary gate for an n-channel TFET and vice-versa for a p-channel TFET. The DMG GAA nanowire TFET will provide a higher $I_{ON}$ due to the increased tunneling by a metal of lower work function. It will have a lower OFF-state current ($I_{OFF}$) because of the presence of a minimum in the surface potential and a negative electric field in the channel. Thus we will get a better $I_{ON}/I_{OFF}$ ratio and a better SS [3, 15, 16]. Thus, a DMG GAA nanowire TFET provides a higher $I_{ON}$ with reduced SCEs and better switching characteristics as compared to a planar TFET. The DMG structure has been explored extensively in literature [17-20]. Although, TFETs using other materials are being studied, there is a great interest in silicon TFETs with improved $I_{ON}$ because of their suitability in silicon based CMOS technology.

The DMG GAA nanowire TFET has been studied in [15] using numerical simulations but a compact model for drain current characteristics is needed for a better understanding of the working of the device. Several models have been developed for conventional TFETs [21-26] but a model for DMG GAA TFET is yet to be developed. The objective of this work is, therefore, to develop a pseudo-2D analytical model for the DMG GAA nanowire TFET using the approaches in [27] and [28].

In this work, we begin with the modeling of the surface potential along the channel using a pseudo-2D model [27] for solving the Poisson equation in the silicon channel. We then find the average electric field in the tunneling region and derive the drain current using Kane’s model [29]. To begin with, we develop a model considering equal lengths of tunneling and auxiliary gates but we later extend our model to a more general case where the tunneling gate length is much smaller than the auxiliary gate length as suggested in [16] for optimal results. The accuracy of our models is validated by comparing the results given by our models with three dimensional numerical simulations [30]. The tunneling parameters for the simulations are calibrated by accurately reproducing experimental results published in Fig 6 (a) of [28].

II. MODEL DERIVATION

The schematic view of the p-channel DMG GAA nanowire TFET structure is shown in Fig. 1. The length of the channel is 200 nm and the length of the source and drain regions is 50 nm.

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The channel doping $N_S = 10^{15}/\text{cm}^3$ and the source and drain dopings are $10^{21}/\text{cm}^3$. The radius of the nanowire ($T_{Si}$) is 10 nm and the oxide thickness ($\delta_{ox}$) is 2 nm. The gate which surrounds the entire channel is split into two parts. Tuning gate at the source side with a work function $\Phi_{tunnel} = 4.8 \text{ eV}$ and an auxiliary gate at the drain side with $\Phi_{aux} = 4.4 \text{ eV}$ as suggested in [16] for optimal results. As a general case we begin with equal lengths of both the gates i.e. tunneling gate length $L_t = 100 \text{ nm}$ and auxiliary gate length $L_a = 100 \text{ nm}$ and later extend it for a tunneling gate of shorter length i.e. $L_t = 20 \text{ nm}$ and $La = 180 \text{ nm}$ as suggested by [16] for optimal results.

Fig. 2 shows the simulated band diagram and the surface potential of the device along the $z$-direction. As the current in a TFET is low, it can be observed that the potential drop along the channel is extremely small in the regions shown by the solid arrows in the figure and can be assumed to be constant [28].

Hence it can be inferred that the channel is not depleted in these regions. In Fig. 3, the surface potential of a DMG GAA nanowire TFET has been compared with that of two SMG GAA nanowire TFETs with gate work functions $\Phi_{SMG} = 4.4 \text{ eV}$ and $4.8 \text{ eV}$. As can be seen here, in a DMG GAA nanowire TFET the two non-depleted regions in the channel, one under each gate, has a potential equal to that in an SMG GAA nanowire TFET of the corresponding gate work function. The values of these constant potential regions under the tunneling and the auxiliary gates are denoted as $\psi_{Ci}$ and $\psi_{Ca}$, respectively.

In the channel, TFETs behave like regular MOSFETs apart from the tunneling region at the source end. This is because the mechanism of channel formation and charge transport is the same in both TFETs and MOSFETs. Therefore, the value of $\psi_{Ci}$ is given by

$$\psi_{Ci} = V_D + \psi_{Br} \quad \text{if} \quad |V_D| \leq |V_G - V_{tha}| \quad (1)$$

$$\psi_{Ci} = V_{GS} - V_{tha} + \psi_{Br} \quad \text{if} \quad |V_D| \geq |V_G - V_{tha}| \quad (2)$$

where $\psi_{Br}$ is the channel’s built-in potential under the tunneling gate due to the band bending caused by the gate voltage, and $V_{tha}$ is the threshold voltage of a MOSFET with a gate work function $\Phi = \Phi_{aux}$. The expression for equation (2) will be different for a DMG GAA nanowire TFET with $\Phi_{aux} > \Phi_{tunnel}$. In this case, $V_{tha}$ would be replaced by $V_{tht}$ which is the threshold voltage for a MOSFET with a gate work function $\Phi = \Phi_{tunnel}$. This happens because for a pTFET when $\Phi_{aux} < \Phi_{tunnel}$ then $|V_{tha}| > |V_{tht}|$ and hence, with increasing $V_D$ saturation happens in the auxiliary channel first and the entire channel potential gets saturated. Whereas, when $\Phi_{aux} > \Phi_{tunnel}$, the channel under the tunneling gate gets saturated first and the auxiliary channel potential is dependent on the drain voltage until it gets saturated. The value of $\psi_{Ca}$ is given by

$$\psi_{Ca} = V_D + \psi_{Br} \quad \text{if} \quad |V_D| \leq |V_G - V_{tha}| \quad (3)$$

$$\psi_{Ca} = V_{GS} - V_{tha} + \psi_{Br} \quad \text{if} \quad |V_D| \geq |V_G - V_{tha}| \quad (4)$$

where $\psi_{Br}$ is the channel’s built-in potential under the auxiliary gate due to the band bending caused by the gate voltage. Also,

$$\psi_{Source} = V_S + V_{bi} \quad (5)$$

$$\psi_{Drain} = V_D \quad (6)$$

where $V_{bi}$ is the built-in potential of the source-body junction and $V_S$ is at ground potential.

The channel has four depletion regions, R1, R2, R3 and R4 in saturation as shown in Fig. 2 and only R1, R2 and R3 in linear region. Depletion region R4 need not be considered for drain current calculations, since surface potential near source region is only needed. The surface potential in these regions can be modelled by solving the 2D Poisson equation in cylindrical coordinates as given by:

$$\frac{1}{r} \frac{\partial}{\partial r} \left( r \frac{\partial \psi(r, z)}{\partial r} \right) + \frac{\partial^2 \psi(r, z)}{\partial z^2} = \frac{qN_S}{\varepsilon_{Si}} \quad (7)$$

Fig. 4 shows the potential profile along the $r$-direction of a cross-section of the DMG GAA nanowire TFET. The shape of this profile can be approximated by a second order polynomial [27]:

$$\psi(r, z) = a_0(z) + a_1(z)r + a_2(z)r^2 \quad (8)$$

This polynomial has to satisfy the following three boundary conditions as can be seen in Fig. 4. The potential $\psi$ at $r = T_{Si}$ equals the surface potential $\psi_S$:

$$\psi(T_{Si}, z) = \psi_S(z) \quad (9)$$

Electric field at $r = 0$ is equal to zero:

$$E_r(0, z) = 0 \quad (10)$$

Electric displacement field at $r = T_{Si}$ is equal across the silicon and oxide boundary:

$$E_r(T_{Si}, z) = -C_{ox}(\psi_G - \psi_S(z)) / \varepsilon_{Si} \quad (11)$$

where $\psi_G$ is the electrostatic potential of the gate and is equal to $V_G \cdot V_{FB}$ ($V_{FB}$ is the flat band voltage for the tunneling gate) and $C_{ox}$ is oxide capacitance per unit area at $r = T_{Si}$, given by

$$C_{ox} = \varepsilon_{ox} / (T_{Si} \ln(1 + \delta_{ox} / T_{Si})) \quad (12)$$

By applying these boundary conditions to (8), we get:

$$a_0(z) = \psi_S(z)(1 - \frac{T_{Si}^2 C_{ox}}{2T_{Si}^2 \varepsilon_{Si}} - \frac{T_{Si}^2 C_{ox}}{2T_{Si}^2 \varepsilon_{Si}} \psi_G) \quad (13)$$

$$a_1(z) = 0 \quad (14)$$

$$a_2(z) = -\frac{C_{ox}}{2T_{Si}^2 \varepsilon_{Si}}(\psi_G - \psi_S(z)) \quad (15)$$

Using (8) in (7), the surface potential can be written as:

$$\frac{\partial^2 \psi_S}{\partial z^2} - \frac{2C_{ox}}{T_{Si}^2 \varepsilon_{Si}} \psi_S = \frac{qN_S}{\varepsilon_{Si}} - \frac{2C_{ox}}{T_{Si}^2 \varepsilon_{Si}} \psi_G \quad (16)$$

which gives the following general form solution for the surface potential in regions R1, R2 and R3.

$$\psi_G(z) = C_i \exp(-\frac{z - L_t}{L_d}) + D_i \exp(-\frac{(z - L_t)}{L_d}) + \psi_{Gi} - N_i L_d^2 \frac{C_{ox}}{\varepsilon_{Si}} \quad (17)$$

where $C_i$ and $D_i$ are unknown coefficients, $L_d$ is the length of region $R_i$, $N_i$ is the background negative charge concentration of region $R_i$, $\psi_{Gi}$ is the electrostatic potential gate over region $R_i$ and $L_d$ is the characteristic length. In region R1, (17)
ψ_{s1}(z) = (ψ_{CT} - ψ_{Ga} + \frac{qN_sL_d^2}{\varepsilon_{Si}}) \cosh(\frac{z - L_1}{L_d}) + ψ_{Ga} - \frac{qN_sL_d^2}{\varepsilon_{Si}} \tag{22}

where \( L_1 \) is the length of R1 and can be evaluated by using (19).

Let us now model the surface potential in regions R2 and R3. One important thing to note here is that the value of \( N_i \) will be different for R2 and R3. The channel at the boundary between R2 and R3 behaves like a p+n junction and hence there will be complete depletion in R2 but the mobile charges of the channel which were earlier in region R2 will now move into region R3. We assume this charge in region R3 to be \( n \) per cm^3. Hence, \( N_i \) in R2 will be the body doping \( N_S \) and in R3, it will be \( N_S + n \). There will be two equations like (17) one each for regions R2 and R3. We will have six unknown parameters (\( C_2 \), \( D_2 \), \( L_2 \), \( L_3 \), \( D_3 \), and \( L_3 \)) which can be determined by the following boundary conditions assuming that \( z = 0 \) is the junction of the two gates.

(i) The value of \( ψ_S \) at \( z = -L_2 \) is equal to \( ψ_{CT} \) and at \( z = L_3 \) is equal to \( ψ_{Ga} \).

\[ ψ_{s2}(-L_2) = ψ_{CT} \] \quad \tag{23}
\[ ψ_{s3}(L_3) = ψ_{Ga} \] \quad \tag{24}

(ii) The electric field at \( z = -L_2 \) and at \( z = L_3 \) is zero:

\[ \frac{\partial ψ_{s2}}{\partial z}(-L_2) = 0 \] \quad \tag{25}
\[ \frac{\partial ψ_{s3}}{\partial z}(L_3) = 0 \] \quad \tag{26}

(iii) The surface potential is continuous at \( z = 0 \):

\[ ψ_{s2}(0) = ψ_{s3}(0) \] \quad \tag{27}

(iv) The electric field is continuous at \( z = 0 \):

\[ \frac{\partial ψ_{s2}}{\partial z}(0) = \frac{\partial ψ_{s3}}{\partial z}(0) \] \quad \tag{28}

From (23) and (25), we get

\[ C_2 = D_2 = \frac{ψ_{CT} - ψ_{Ga} + \frac{qN_sL_d^2}{\varepsilon_{Si}}}{2} \] \quad \tag{29}

From (24) and (26), we get

\[ C_3 = D_3 = \frac{ψ_{Ga} - ψ_{CT} + \frac{q(N_S + n)L_d^2}{\varepsilon_{Si}}}{2} \] \quad \tag{30}

From (27), we get

\[ \frac{ψ_{CT} - ψ_{Ga} + \frac{qN_sL_d^2}{\varepsilon_{Si}}}{2} \times (e^{\frac{L_2}{L_d}} + e^{-\frac{L_2}{L_d}}) + ψ_{Ga} - \frac{qN_sL_d^2}{\varepsilon_{Si}} = \frac{qN_sL_d^2}{\varepsilon_{Si}} \times (e^{\frac{L_2}{L_d}} + e^{-\frac{L_2}{L_d}}) \] \quad \tag{31}

From (28), we get

\[ \frac{ψ_{CT} - ψ_{Ga} + \frac{qN_sL_d^2}{\varepsilon_{Si}}}{2} \times (e^{\frac{L_3}{L_d}} + e^{-\frac{L_3}{L_d}}) + ψ_{Ga} - \frac{q(N_S + n)L_d^2}{\varepsilon_{Si}} = \frac{q(N_S + n)L_d^2}{\varepsilon_{Si}} \times (e^{\frac{L_3}{L_d}} + e^{-\frac{L_3}{L_d}}) \] \quad \tag{32}

The value of \( n \) in region R3 can be calculated by adding the following condition in our model, which comes from the
conservation of charge across the p'-p junction at the boundary of the tunneling gate and the auxiliary gate i.e.
\[ n_{ch2} = n_{ch2} L_2 \]  
(33)
where \( n_{ch2} \) is the channel inversion charge concentration under the tunneling gate. Simultaneously solving (31), (32) and (33) gives us the values of \( L_2, L_3 \) and \( n \). These equations have to be solved numerically as they contain non-linear expressions. Since, after the onset of strong inversion, the channel charge does not vary greatly and \( L_2 \) and \( L_3 \) are of the same order, we can simplify our model by assuming \( n \) to be constant. As the inversion charge in strong inversion mostly remains constant with the applied \( V_{GS} \), we can assume \( n \) to be fixed at \( 10^{19}/\text{cm}^3 \) as \( n_{ch2} \) is typically \( 10^{19}/\text{cm}^3 \) in strong inversion. Now, we only need to solve (31) and (32) and find \( L_2 \) and \( L_3 \).

As shown in Fig. 2, in region R1, the slope of the surface potential decreases along the channel length and hence the integration simplifies to calculating the total drain current as has been done in many of the carriers in the tunneling region is given. This generation rate gives us the values of \( L_2, L_3 \) and \( n \). These equations have to be extracted experimentally (C1, D1, L1, C3, D3 and L3). We will again use six boundary conditions as earlier defining \( z = 0 \) as the junction of the two gates.

The tunneling gate length \( L_T \) is the length of region R1 now and not \( L_1 \). Since regions R1 and R2 have merged, we will get a point of minimum in the surface potential at \( z = -L_4 \). As a result, the condition given by (23) will be different now and the value of \( \psi_{sl} \) at \( z = -L_4 \) will be \( V_{bi} \).

The other five boundary conditions given by (24)-(28) remain the same but the variables and constants of region R2 are replaced by those of region R1 (i.e. \( \psi_{s2} \) will become \( \psi_{sl} \) and so on). Solving as done earlier, we get the following:

\[ C_3 = D_3 = \frac{N_S + n L^2}{L} \]  
(39)

\[ C_1 = D_1 = \left( V_{bi} - \frac{N_S L^2}{L} \right) / (2 \cosh \left( \frac{L_4 + L_3}{L} \right)) \]  
(40)

\[ V_{bi} - \frac{N_S L^2}{L} \times (e^{\frac{L_3}{L}} + e^{-\frac{L_3}{L}}) + \frac{N_S L^2}{L} \]  
(41)

\[ \psi_{cs} - \psi_{ga} + \frac{N_S}{L^2} \times (e^{\frac{L_3}{L}} - e^{-\frac{L_3}{L}}) + \frac{N_S L^2}{L} \]  
(42)

Simultaneously solving (40)-(42) gives us \( L_4, L_3 \) and \( C_1 \). The drain current \( I_D \) is then calculated using (34)-(37).

### III. MODEL RESULTS

The proposed models of DMG GAA nanowire TFET are verified against three dimensional numerical simulations [30]. In our simulations, we have used the models for concentration
dependent mobility, electric field dependent mobility, SRH recombination, auger recombination, band gap narrowing and Kane’s band to band tunneling. The parameters for Kane’s band-to-band tunneling in Silvaco Atlas, $A_{Kane} (= 4 \times 10^{19} \text{eV}^{1/2}/\text{cm-s-V}^2)$ and $B_{Kane} (= 41 \text{MV/cm-eV}^{3/2})$ [30] are extracted by reproducing the experimental results given in Fig. 6(a) of [28] as shown in Fig. 5. With these tunneling parameters, we simulate the device structure as shown in Fig. 1 and compare the simulation results with those predicted by our models. Fig. 6 shows the surface potential along the channel given by the model equations (22)-(32) for different values of $V_{GS}$ and $V_{DS}$ and compares them with simulation results. Fig. 7 shows the log($I_{DS}$)-$V_{GS}$ characteristic given by the model equations (34)-(37) for different values of $V_{DS}$ and compares them with simulation results. The model results are in good agreement with the simulations over a large range of $V_{GS}$ above the threshold (which is $-1.3 \text{ V}$). From the model results in Fig.7, it may appear unreasonable to have a lower drain current at a higher absolute drain voltage. However, this is due to the fact that our model is accurate only for gate voltages above threshold. This is because our model takes the shortest tunneling length and uses it over the entire tunneling volume. For gate voltages above the threshold, the shortest tunneling length being small dominates the tunneling current. But for gate voltages in the subthreshold region, the shortest tunneling length is large and is not able dominate the tunneling current. Hence, in the subthreshold region, using a constant tunneling length over the entire tunneling volume gives us inaccurate results. To model the drain current more accurately in the subthreshold region, a numerical approach has to be taken which integrates the tunneling current over all the 1-D tunneling lengths. Our approach to find the tunneling current is analytical and hence inaccurate in the subthreshold region. Fig. 8 shows the $I_{DS}$-$V_{DS}$ characteristic given by the models equations (34)-(37) for different values of $V_{GS}$ and compares them with simulation results. The model results match with the simulation results with reasonable accuracy. In Fig. 9, we have plotted the surface potential along the channel for a DMG GAA nanowire TFET with $L_t = 20 \text{ nm}$ and $L_a = 180 \text{ nm}$ for different values of $V_{GS}$ and compared them with simulation results.

IV. CONCLUSION

In this work, we have developed a pseudo 2D-analytical model for the drain current and surface potential of a DMG GAA nanowire TFET. The accuracy of our model has been tested.
against results obtained from three dimensional numerical simulations calibrated with experimental results. Our model can be used for a better understanding of the DMG GAA nanowire TFET and also for circuit design. It may be pointed out that our model results in the off-state and the sub-threshold region do not match with the simulations. Therefore, further work needs to be done by considering non-local tunneling to refine the models in the low current regime. Also, the models developed in this work are for a long channel device and can be used as long as all the depletion regions (i.e. regions R1, R2, R3 and R4) do not merge into each other. For a highly scaled down TFET, if these depletion regions merge with each other, a fully depleted channel approach [31] needs to be used to develop a suitable model.

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