Leveraging Architectural Support of Three Page Sizes with Trident

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Abstract

Large pages are commonly deployed to reduce address translation overheads for big-memory workloads. Modern x86-64 processors from Intel and AMD support two large page sizes – 1GB and 2MB. However, previous works on large pages have primarily focused on 2MB pages, partly due to lack of substantial evidence on the profitability of 1GB pages to real-world applications. We argue that in fact, inadequate system software support is responsible for a decade of underutilized hardware support for 1GB pages.

Through extensive experimentation on a real system, we demonstrate that 1GB pages can improve performance over 2MB pages, and when used in tandem with 2MB pages for an important set of applications; the support for the latter is crucial but missing in current systems. Our design and implementation of Trident in Linux fully exploits hardware supported large pages by dynamically and transparently allocating 1GB, 2MB, and 4KB pages as deemed suitable. Trident speeds up eight memory-intensive applications by 18%, on average, over Linux’s use of 2MB pages. We also propose TridentP, an extension to Trident that effectively virtualizes 1GB pages via copy-less promotion and compaction in the guest OS. Overall, this paper shows that adequate software enablement can bring practical relevance to even GB-sized pages, in turn motivating architects to continue investing/innovating in large pages.

1. Introduction

It is not uncommon for certain architectural features to require software enablement. Unfortunately, it is also common to find those hardware features that are underutilized or mostly ignored due to the lack of adequate software support. This is, while paying both the runtime cost of having the new hardware, e.g., power dissipation due to the feature, and the one-time hardware design and verification cost. Further, architects are left in the dark about the extent to which those features are beneficial in practice, and whether they should continue enhancing them or drop them in future products.

In this work, we shed light on one such hardware feature that has been languishing for a decade – support for 1GB pages and provide a detailed system software (here, Linux and KVM) enablement for the same.

Big-memory workloads are well known to witness significant slowdowns due to virtual to physical address translation (e.g., up to 20-50%). Modern processors support large pages to help reduce this overhead [30, 35, 36]. A large page TLB (Translation Lookaside Buffer) entry maps a larger contiguous virtual address region to contiguous physical address region (e.g., 2MB or 1GB compared to default 4KB). Consequently, the use of a large page increases TLB coverage and can reduce the number of TLB misses that is the primary source of translation overheads.

However, the hardware support alone is not useful. The OSes and hypervisors (henceforth called system software) that create the address mappings need to enable large pages for applications. Further, the ease of use determines the prevalence of large page’s deployment in practice. If application modifications are necessary for allocating a given large page size, then that page size may not be widely deployed and, consequently, render the corresponding hardware resources underutilized.

The x86-64 processors have supported two large page sizes – 2MB and 1GB, for over a decade. Intel Sandybridge architecture launched in 2010 supported 1GB pages and had a four-entry L1 TLB dedicated for 1GB pages in each core [9]. The current generation of Intel Coffee Lake processors additionally have a 16-entry L2-TLB for 1GB pages [8]. Upcoming Intel Ice Lake processors is presumed to have 1024-entry L2 TLB for 1GB pages [12]. In short, processor vendors continues to enhance support for 1GB pages.

Unfortunately, software enablement of large pages has focused primarily on 2MB large pages. Linux’s Transparent Huge Page (THP) enables dynamic allocation of large pages without user intervention and thus, is key to the widespread use of large pages. But it is limited only to 2MB pages. Previous research works on improving large page support similarly ignore 1GB pages [30, 35, 36].

With the continued growth in the memory footprint of applications, use of 1GB pages is likely to become a necessity for good performance. The advent of denser non-volatile memory (NVM) technologies promises to significantly increase the physical memory size [23, 32]. The ability to efficiently address a large amount of memory is essential to harness the benefits of NVM. While the hardware support for 1GB pages has sped ahead, its software enablement has fallen behind.

However, it is important for architects to find hard evidence of practical usefulness of 1GB pages, over and above 2MB pages, to continue enhancing its support or else consider dropping it in future products. Therefore, we first set out to quantify the usefulness of 1GB pages to various applications, with and without virtualization. We find that while most memory-
intensive applications benefit from 2MB pages over 4KB, a subset of them speeds up further with 1GB pages. Even for applications in that subset, use of the other large page size(s) (here, 2MB) alongside the largest page size (here, 1GB) is important. Mapping a virtual address range with a large page size requires the address range to be at least as long as that page size and be aligned at that page size boundary. Consequently, larger the page size, lesser is the number of virtual address ranges that are mappable by that page size.

We empirically find that often a significant portion of an application’s address space is not mappable with 1GB pages, but mappable with 2MB. Importantly, such address ranges often witness relatively frequent TLB misses. Thus, if only the largest page size is used, then those address ranges would have to be mapped with the smallest (4KB) pages. Consequently, the number of TLB misses would increase significantly.

A larger page size also needs equally longer contiguous physical memory chunk. The larger the page size, shorter is the supply for necessary physical memory chunks. Thus, it may not be possible to map a virtual address range with the largest page size even if it is mappable by that page size.

Driven by the above analysis, we built Trident in Linux to dynamically allocate all available page sizes in x86-64 systems. A key challenge in dynamically allocating 1GB pages is the lack of enough number of 1GB contiguous physical memory chunks. As the free physical memory gets naturally fragmented over time, finding 1GB chunks become far more difficult than 2MB chunks. Thus, the dynamic allocation of large pages needs to periodically compact physical memory to make contiguous free memory available. However, compaction for 1GB memory chunk requires significantly more work than 2MB. Moreover, a compaction attempt fails if it encounters even a single page frame (4KB) with unmovable contents, e.g., kernel’s objects like inodes, in a 1GB region. In short, compaction for 1GB chunks needs a new approach.

Trident introduces a novel smart compaction technique. We observe that the current compaction approach of sequential scanning and moving contents of occupied page frames is not scalable to 1GB. This approach incurs an unnecessarily large amount of data movement. The smart compaction tracks the number of occupied bytes (i.e., the number of mapped page frames) within each 1GB physical memory chunk. Instead of scanning, smart compaction then frees a region with the least number of occupied bytes, which significantly reduces data movement. It also tracks unmovable contents within a 1GB region to further avoid unnecessary data movement.

Even with smart compaction, 1GB memory chunks are not always available when needed. About a third of the attempts to allocate 1GB page fails due to the unavailability of contiguous physical memory. Unsurprisingly, 2MB chunks are more easily available. Trident thus maps address ranges with 2MB pages if it fails to map with 1GB pages. Later, these 2MB page mappings are promoted to 1GB pages, when suitable.

We then propose Tridentpv, an optional extension to Trident under virtualization for copy-less 1GB page promotion and compaction in the guest OS. The guest often copies contents of guest physical pages to create contiguity in guest physical address space for page promotion and compaction. We observe that copying can be mimicked by exchanging the mapping between the guest physical address (gPA) and the host physical address (hPA) of the source and destination. This copy-less technique makes the promotion of 2MB pages to a 1GB page significantly faster than the traditional copy-based approach. However, the guest and the hypervisor need to coordinate to alter the desired gPA to hPA mappings via a hypercall.

We find that on a bare-metal system, Trident speeds up eight memory-intensive applications by 18%, over Linux’s THP, on average. Tridentpv can improve upon Trident’s own performance under virtualization, by up to 10%.

In short, this paper shows that the use of 1GB pages has been hamstrung due to inadequate software enablement even after a decade of hardware support in commercial processors. Therefore, architects must prioritize enhancing the software support before investing further into hardware support for 1GB pages. Our specific contributions are as follows:

- We empirically demonstrate why it is important to deploy all large page sizes, not only the largest one.
- We created Trident in Linux to dynamically allocate all page sizes available in x86-64 processors to significantly speedup applications with large memory footprint.
- We then propose an optional extension to Trident called Tridentpv that employs paravirtualization to enable copy-less 1GB page promotion and compaction in the guest.

2. Background

Hardware support for large pages: Applications with large memory footprints often spend considerable time in address translation (e.g., up to 20-50%) [16, 35]. Address translation overhead is primarily the overhead of performing page table walks on TLB misses. Hits in the TLB are fast, but a page table walk on a miss may require up to four memory accesses to lookup the hierarchical in-memory page table in x86-64 processors. Large pages can help reduce translation overhead in two ways: (1) It reduces the frequency of TLB misses by increasing the TLB coverage since a single entry for a large page maps a larger address range. (2) It quickens individual page table walks by reducing the number of levels in the page table that need to be looked up. For example, a walk for a 1GB page requires up to 2 memory accesses, compared to 3 for a 2MB page and 4 for a 4KB page, in x86-64 processors. Large pages under virtualization: Address translation involves two layers under virtualization through nested page tables. First, a guest virtual address (gVA) is mapped to a guest physical address (gPA) through the guest page tables (gPT) managed by the guest OS running on a virtual machine. gPA is then translated to host physical address (hPA) through host
page tables (hPT) maintained by the hypervisor. Two layers of indirection increase the number of memory accesses required for a page walk. For example, with four-level page tables, a TLB miss requires up to 24 memory accesses for 4KB-pages. Use of 2MB and 1GB pages at both layers reduce the number of accesses to 15 and 8, respectively.

**OS support for large page allocation:** OSes typically provide three mechanisms to allocate large pages. In the pre-allocation based mechanism, users are required to reserve physical memory for large pages and a helper library (e.g., libHugetlbfs) maps specific segment(s) of an application’s memory with large pages from the reserved memory. Unfortunately, this static approach constrains the usability of large pages. The second approach needs explicit system call (e.g., madvise syscall or extra flags in mmap). In the third approach, the OS allocates large pages without the user or programmer involvement. Linux’s Transparent Huge Pages (THP) is an example of this approach.

Internally, THP employs two mechanisms. On a page fault, it checks if the faulting address falls within a virtual address range that is at least as big as and aligned with the large page size. If yes, and a free contiguous physical memory chunk is available, THP maps the address with a large page. For address regions that were not immediately mappable with large pages during page faults, THP employs a background thread (khugepaged) to locate virtual address ranges mapped with 4KB pages and promote (remap) them to large pages, when possible. To ensure enough supply of contiguous physical memory, THP also compacts physical memory. Compaction moves contents of occupied pages to one end of the physical memory for creating contiguous free memory regions on the other end. Unfortunately, THP currently supports only 2MB large pages. Hosted hypervisors, such as KVM uses THP for allocating 2MB large pages in the hypervisor (host).

### 3. Methodology

Table 1 details the configuration of our experimental platform. We evaluate 12 workloads with multi-GB memory footprint (see Table 2) across machine-learning, graph algorithms, key-value stores, HPC, and microbenchmarks (GUPS and BTree). We use Linux’s perf tool [6] to collect microarchitectural events related to virtual memory overheads. Specifically, we monitor events like the number of cycles spent on page walks via counters DTLB_LOAD_MISSES.WALK_DURATION and DTLB_STORE_MISSES.WALK_DURATION.

To study performance under different states of the system, we used a tool to fragment the physical memory (more in Section 5.1). Physical memory is fragmented by reading a large file at random offsets to populate OS’s file cache. This renders physical memory sprinkled with recently used page frames containing file cache contents and thus, fragmented.

### 4. How useful are 1GB large pages?

Hardware support for 1GB pages is not free, and the software running on x86-64 processors pays the price, irrespective of its use of 1GB pages. For example, modern Intel processors have 4-entry L1 TLB and 16-entry L2 TLB dedicated to 1GB pages. Those four L1 entries for 1GB pages are accessed on every load and store since the page size is not known during TLB lookup. Due to frequent accesses, L1 TLBs can contribute to a thermal hotspot in processors [41] and can account for 6% of a processor’s total power [43]. The presence of dedicated TLBs for 1GB pages adds to the cost. The continued increase in the number of TLB entries for 1GB pages would worsen it.

It is, thus, natural to wonder if applications can benefit from 1GB pages. We analyze various applications under different execution scenarios to understand usefulness of 1GB pages.
the applications witness benefits of using 2MB pages (over 4KB), but barely gain any further with 1GB pages. This is not surprising; the walk cycles were already low with 2MB pages, and an out-of-order CPU could hide the remaining cycles.

For the rest of the paper, we will thus focus on the first eight (shaded) applications. We also observe that THP is able to perform within 0.5% of that of libHugetlbfs using 2MB pages without needing memory pre-allocation or user guidance. This emphasizes the importance of THP in the wide deployment of 2MB pages; something yet to be realized for 1GB pages.

4.2. 1GB pages under virtualized execution

Two levels of translation under virtualization can increase overheads. Each level may use a different page size. Thus, a total of nine combinations of page sizes are plausible. While we experimented with all, we discuss only 4KB-4KB, 2MB-2MB, and 1GB-1GB combinations. The first term denotes the page size used for guest, and the second term denotes that in the host. We chose these configurations as they demonstrate the best performance achievable with a given page size.

Figure 3 shows the normalized fraction of page walk cycles under three different page size combinations. We notice significant reductions in walk cycles with 2MB and 1GB pages. For example, the fraction of walk cycles reduced by 80% for Graph500. Even a couple of 1GB page agnostic applications experience a large reduction in walk cycles.

Figure 4 shows the performance under virtualization. We observe that 1GB pages provides a bit more benefit here. The eight 1GB page sensitive applications speed up by 17.6% over 2MB pages, on average. The application BC, which did not benefit from 1GB pages under native execution, becomes slightly sensitive to 1GB pages.

Figure 5 shows the total memory mappable with different page sizes.
4.3. Importance of using all large page sizes

In the analysis so far, only one of the large page sizes was deployed as is the norm in today’s software. However, we find that using all large page sizes together can bring benefits that are not achievable using any one of them.

A virtual address range is mappable by a large page only if: (1) it is at least as long as that large page, and (2) the starting address is aligned at the boundary of that page size. All 1GB-mappable address ranges are, thus, mappable by 2MB pages but not vice-versa. When an application allocates, de-allocates, and re-allocates memory (e.g., Graph500), the virtual address space gets fragmented. Consequently, an application’s entire address space may not be mappable by the largest page size.

We empirically find that often GBs of an application’s virtual memory is 2MB-mappable but not 1GB-mappable. This depends on the application’s memory allocation strategy – whether the application pre-allocates memory in large chunks (low virtual memory fragmentation) or incrementally allocate/de-allocate memory over time (high fragmentation).

We wrote a kernel module to periodically scan an application’s virtual address space to measure 1GB-mappable and 2MB-mappable address ranges. Figure 5 shows the size of allocated virtual memory that is mappable with 2MB and 1GB over time for two representative applications – Graph500 and SVM. The x-axis represents the execution timeline (excluding initialization), and the y-axis is the virtual memory (in GB). The two lines in each graph show the amount of 1GB- and 2MB-mappable memory. We observe that several GBs of memory is mappable by 2MB pages but not by 1GB (the gap between the two lines). If only 1GB pages are used, these memory regions have to be mapped with 4KB pages while wasting 2MB TLB resources.

We then analyzed the importance of mapping the regions that are un-mappable by 1GB pages, with 2MB. We wrote another module to measure the relative (sampled) TLB miss frequencies to the addresses that are mappable by 2MB but not by 1GB and those by both. We periodically un-set the access bits in PTEs (4KB) and then tracks which ones get set again by the hardware, signifying a TLB miss. Figure 6 presents the measurement. The x-axis shows the allocated virtual address regions, and the y-axis shows the relative TLB miss frequencies to pages in those regions. We use different colors for 2MB-mappable but 1GB-unmappable, and 1GB-mappable addresses. We observe that the 1GB-unmappable regions witness frequent TLB misses. Particularly for Graph500, the spike in miss frequency on a relatively small 1GB-unmappable region (about 800MB) stands out (circled). Therefore, it is important to map these 1GB un-mappable address ranges with 2MB pages to reduce TLB misses.

Furthermore, it may not always be possible to map a 1GB-mappable address range with 1GB page due to unavailability of 1GB contiguous physical memory. However, 2MB contiguous physical memory regions are more easily available. In short, it is important to utilize all page sizes available.

We also measured the usefulness of 1GB pages to Linux kernel itself. Linux kernel direct maps entire physical memory with the largest page size. Using a set of OS intensive workloads, we found that 1GB pages improve performance by around 2-3% over 2MB pages (detailed in the Appendix).

Summary of observations: (1) A set of niche but important memory-intensive applications speed up with 1GB pages over 2MB pages. In contrast, 2MB pages almost universally benefit memory-intensive applications. (2) Application-transparent allocation of 2MB pages brings benefits of 2MB pages without user dependency – a capability that 1GB pages lack. (3) It is important to utilize all large page sizes not only the largest.

5. Trident: Dynamic allocation of all page sizes

We design and implement Trident in Linux to enable application-transparent dynamic allocation of all three page sizes on x86-64 processors. Trident minimizes TLB misses by mapping most of an application’s address space with 1GB pages, failing which 2MB, and finally, 4KB pages are used. Challenges: While the dynamic allocation of 2MB pages is not new, that for 1GB pages gives rise to many new challenges. First, Trident needs to ensure a steady supply of free contiguous 1GB physical memory chunks even in the presence of fragmentation. We found that Linux’s sequential scanning based compaction for creating 2MB chunks is not scalable to 1GB due to excessive data copying.

Linux tracks only up to 4MB free physical memory chunks. However, the dynamic allocation of 1GB pages would require maintaining free memory upto 1GB granularity. Besides, allocating a 1GB page during a page fault is much slower than that for a 2MB or 4KB page due to the latency of zeroing entire 1GB memory. Low-latency 1GB page faults are necessary for an aggressive deployment of 1GB pages. Finally, Trident should map a virtual address range with the largest large page size deployable at that given time. It should then periodically look for opportunities to promote address ranges mapped with a smaller large page(s) to a larger one wherever possible.

5.1. Design and implementation

At a high-level, Trident modifies four major parts of Linux. (1) It enhances Linux to track up to 1GB free physical memory chunks. (2) It updates the page fault handler to allocate 1GB page on a fault when possible and fall back to smaller pages if needed. (3) Trident extends THP’s khugepaged background thread to promote virtual address ranges to be re-mapped
(promoted) to 1GB pages when possible. ④ Trident employs a novel smart compaction technique to ensure a steady supply of 1GB physical memory chunks at low overhead.

### 5.1.1. Managing 1GB physical memory chunks.

Linux’s buddy allocator keeps an array of free lists of physical memory chunks of sizes 4KB up to 4MB in the power of 2 [7]. When free memory is needed, the buddy allocator provides a memory chunk from one of its lists based on the request size. Freed physical memory is returned to the buddy, and coalesced with neighboring free memory chunks to create larger ones. Unfortunately, the buddy only keeps track of regions up to 4MB. We thus extended it to include separate lists for tracking up to 1GB memory chunks.

### 5.1.2. Allocating large pages during page fault.

Like THP, Trident allocates large pages either ① during a page fault (e.g., when a process accesses a virtual address for the first time) or ② later during attempts to promote an address range to a large page. We here detail the former.

If the faulting virtual address falls in a 1GB-mappable address range, then Trident attempts to map it with a 1GB page. If it fails, Trident attempts to map the address with a 2MB page, and on failure, with 4KB. If the faulting address falls in a region that is 2MB-mappable but not 1GB-mappable, Trident tries to map it with 2MB.

**Asynchronous zero-fill:** A 1GB page fault takes around 400 milli-seconds; compare that to 850 microseconds for 2MB. The additional latency is due to zero-filling of 1GB memory instead of 2MB*. We instead employ asynchronous zero-fill to speed up 1GB faults. A kernel thread periodically zero-fills free 1GB regions and Trident allocates an zero-filled region, if available. This reduces the average 1GB fault latency from 400 milli-seconds to 2.7 milli-seconds. While prior works [1, 35] explored asynchronous zero-fill for 2MB pages, we find it to be a necessity for 1GB pages in latency-critical workloads. For example, the boot time of a 70GB virtual machine dropped from 25 seconds to 13 seconds with asynchronous zero-fill.

Table 3 shows the portion of applications’ memory footprint mapped by 1GB and 2MB pages under Trident’s various dynamic allocation mechanisms that we will discuss in this section. The first data column shows applications’ memory footprint. The first set of sub-columns capture the behavior with un-fragmented physical memory while the next set represents that under fragmentation. Physical memory is said to be fragmented if free memory is scattered in small holes and thus, non-contiguous. Typically, physical memory is un-fragmented only if the system is freshly booted and/or there is little memory usage. But, the memory gets quickly fragmented as applications/OSS allocate and deallocate memory.

The sub-columns under un-fragmented shows that the page fault handler alone (Page-fault only) is able to map a large fraction of application’s memory with 1GB pages for three out of eight applications (XSbench, GUPS, Graph500). If an application pre-allocates its memory in large chunks, then the fault handler would often find the faulting address to be in a 1GB-mappable region, and map it with a 1GB page. However, Redis and Memcached progressively allocate memory while inserting key-value pairs. Thus, the fault handler could map a small portion of its memory with 1GB pages. SVM, Btree, Canneal do not pre-allocate their entire memory needs, either.

The story is different if the physical memory is fragmented. Even if the fault handler finds a 1GB-mappable address range, it is unlikely to find a free 1GB physical memory chunk. Thus, it would often fall back to 2MB or 4KB pages. This is evident from data in sub-columns for “Page-fault only” under fragmentation (Table 3) as only a few 1GB pages are allocated.

### 5.1.3. Large page promotion.

If an application does not pre-allocate memory or the physical memory is fragmented, it becomes important to later re-map (promote) address ranges with larger pages, when possible. Trident extends THP’s khugepaged thread to promote to both 1GB and 2MB pages.

Figure 7 shows a flowchart of Trident’s page promotion algorithm (changes to THP’s khugepaged thread to promote to both 1GB and 2MB pages).
Table 3: Comparison of 1GB and 2MB pages allocated via different mechanisms employed in Trident.

|                  | Memory footprint (in GB) | Un-fragmented (all data in GB) | Fragmented (all data in GB) |
|------------------|--------------------------|--------------------------------|-----------------------------|
|                  |                          | Un-fault | Promotion       | Promotion                  | Un-fault | Promotion       | Promotion                  |
|                  |                          | 1GB     | Normal compaction| Smart compaction           | 1GB     | Normal compaction| Smart compaction           |
|                  |                          | 2MB     |                  |                            | 1GB     |                  |                            |
|                  |                          |         |                  |                            | 2MB     |                  |                            |
| XSBench          | 17                       | 114     | 2.94             | 116                        | 116     | 1.2             | 6                          | 5.3                        |
|                  |                          | 116     | 1.2              |                            | 79      | 38.1            | 80                         |
|                  |                          | 116     | 1.2              |                            | 53      | 12.2            | 94                         |
|                  |                          | 6       |                  |                            | 31      | 10.3            | 28                         |
|                  |                          | 36      |                  |                            | 16      | 12.73           | 12                         |
|                  |                          | 16      |                  |                            | 11.7    | 8.91            | 23.6                       |
|                  |                          | 9       |                  |                            | 3.35    | 9               | 53                         |
|                  |                          | 0       |                  |                            | 117     | 137             | 16                         |
|                  |                          | 28      |                  |                            | 12      | 6               | 16                         |
|                  |                          | 32      |                  |                            | 58      | 16              | 60                         |
|                  |                          | 51      |                  |                            | 59      | 16              | 60                         |
|                  |                          | 44      |                  |                            | 0       | 0               | 25                         |
|                  |                          | 25      | 4.0              | 16                         | 0       | 7               | 24.2                       |
|                  |                          | 8       |                  |                            | 11.7    | 8.92            | 23.6                       |
|                  |                          | 137     |                  |                            | 58      | 16              | 60                         |
|                  |                          | 32      |                  |                            | 28      | 1               | 22                         |

When the physical memory is fragmented, page promotion helps applications get some 1GB pages, although slightly smaller in number compared to the un-fragmented case. For example, 1GB pages allocated to SVM drops from 65 to 53. This is expected; free 1GB memory chunks are scarce even after compaction.

Overheads of compaction for 1GB, however, can negate benefits of 1GB pages. Creating even a single 1GB chunk often requires significant memory copying. Copying data creates contention in memory controllers and pollutes caches. It also requires scanning larger portions of physical memory during compaction. The applications threads could get a smaller fraction of CPU cycles as they can contend with kernel threads performing compaction. In short, it is necessary to reduce the cost of compaction for 1GB pages to harness its full benefit.

**Smart compaction:** We, thus, propose a new compaction technique, called smart compaction, to reduce the cost of 1GB compaction while creating enough 1GB physical memory chunks. The primary goal is to reduce the number of bytes copied. This directly reduces the cost of compaction.

Figure 8 illustrates the difference between normal compaction as employed in Linux today and the smart compaction employed in Trident. Figure 8(a) shows the working of the normal compaction. On a compaction request, the khugepaged thread starts sequentially scanning physical memory from where it left last time it attempted to compact (remembered in source pointer). Scanning starts from the low to high physical address. As it finds an occupied physical page frame (4KB) it copies its contents to a free page frame found by scanning in the opposite direction from the target pointer. This continues until a free memory chunk of the desired size (e.g., 2MB) is created, or the entire memory is scanned without success.

We observe that this strategy is agnostic to how full or empty a physical memory region is. Consequently, this leads to redundant copying. Let us consider the example in Figure 8(a). The 1GB region starting at address $s$ is mostly occupied and has only 256 free page frames (4KB). Thus, to free that 1GB region, Linux would require to copy 999MB of data ($512 \times 512 - 256$ 4KB pages). Instead, if a mostly free region was freed, then the number of bytes copied would be much smaller. While such sub-optimal compaction could be fine for 2MB, it is not so for 1GB, as the data copying increases with size.

Moreover, if the scan encounters a page frame with unmovable contents (e.g., inodes, DMA buffers) [35], then all copying so far for a region, is wasted. A free chunk cannot have any unmovable contents. The probability of encountering unmovable contents is much more for a 1GB region.

To address these shortcomings, we propose smart compaction. The key idea is to divide the physical memory into 1GB regions and select (not scan for) a region with the least number of occupied page frames for freeing (i.e., the source of copying). Similarly, a region with the most number of occupied page frames is preferred as the target for copying. This strategy minimizes data copy. We also track if a given 1GB region contains any unmovable contents. We avoid selecting regions with unmovable content for freeing (i.e., source). This eliminates unnecessary data copying in futile compaction attempts.

To implement the above idea, we first introduced two counters for each 1GB physical memory regions. One counter tracks the number of free page frames, and the other one...
tracks the number of unmovable pages within a region. Whenever a page is returned to the buddy allocator (i.e., freed), we increment the counter for free frames of the encompassing 1GB region. Further, we decrement the counter for unmovable pages if the freed page frame(s) contained unmovable data. Whenever a page frame(s) is allocated from the buddy allocator the free counter for the encompassing region is decremented. We increment its unmovable page counter if the allocated page frame(s) would contain unmovable data (e.g., requested for allocating kernel data structures). Note that a 1GB region can also have a 2MB page allocated within it. We would not be able to avoid data copy under fragmentation. All measurement is performed when physical memory is fragmented, and an application needs all memory. This measurement is less. Under fragmentation, smart compaction typically provides even more 1GB page. This is because the 1GB pages are predefined for passing the list of page addresses to the hypervisor. The hypervisor then updates the mapping between guest physical pages and hPAs. This copy-less approach quickens both compaction and 1GB page promotion in the guest but needs paravirtualization. We call this optional extension TridentPV.

For brevity, we explain the key idea behind TridentPV with the help of large page promotion only (Figure 10). Let us assume that two contiguous guest virtual pages, v1 and v2, are currently mapped to two non-contiguous smaller pages g1 and g3 in guest physical memory (Figure 10(b)). For simplicity, we assume that a large page is double the size of a small page. To remap gVA encompassing v1 and v2 with a large page, the guest OS first copies their content to two contiguous guest physical pages – g7 and g8 and then updates the mapping between gVA and gPA. This traditional way of promoting large pages by copying contents is shown in Figure 10(a).

Figure 10 (c) shows TridentPV’s approach for page promotion without actual copy. Instead of copying g1 to g7, the hypervisor exchanges the gPA to hPA mappings for g1 and g7. After the exchange, g1 would map to h6 and g7 to h2. Since, h2 contains the data originally mapped by g1, this is same as copying g1 to g7. Similarly, the hypervisor exchanges the gPA to hPA mappings for g3 and g8 to create the effect of copying g3 to g8. Later, gVA encompassing v1 and v2 is mapped by the guest with a large page to contiguous gPA encompassing g7 and g8.

In this approach, the guest OS and the hypervisor need to coordinate for copy-less page promotion and, thus, the need for paravirtualization. Specifically, the guest OS supplies the hypervisor with a list of source and target guest physical pages via a hypercall. The hypervisor then updates the mapping from gPA to hPA in the manner explained above to create the effect of copying guest physical pages. Besides promotion, TridentPV uses the same hypercall for compacting guest physical memory to create 1GB pages in the guest.

While promising, the cost of hypercall (~300ns) to switch between guest and the hypervisor can, however, outweigh the benefits the copy-less promotion. We thus batch request for multiple page mapping exchanges in a single hypercall. Two pages are predefined for passing the list of page addresses to exchange between the guest and the hypervisor. One page contains source gPAs (here, g1 and g3) and the other contains the target gPAs (here, g7 and g8). In a single hypercall it is thus

6. TridentPV: Paravirtualizing Trident

Under virtualization, Trident can be deployed both in the guest OS and in the hypervisor to bring benefits of dynamic allocation of all page sizes, including 1GB pages, to both the levels of translation. We observe that it is possible to further optimize certain guest OS operations with paravirtualization.

The guest OS copies contents of memory pages to (1) to compact gPAs, and (2) to promote address mapping between gVA and gPA to larger pages. While the cost of copying 4KB pages is not high, copying 2MB pages in order to compact or promote to 1GB page is slow. We, however, observe that the effect of copying guest physical pages can be mimicked by simply altering the mapping between corresponding gPAs and hPAs. This copy-less approach quickens both compaction and 1GB page promotion in the guest but needs paravirtualization. We call this optional extension TridentPV.
possible to request exchange for 512 page addresses. Thus, a single hypercall is sufficient to promote entire 1GB region in gVA mapped with 2MB pages. The hypercall returns after switching all the requested pages or logs any failure in the same shared page used for passing list of pages. On failure, the guest falls back to individually copy contents of pages.

We empirically found that promoting 2MB pages to a 1GB page in the guest takes ~600 ms in the copy-based technique. Without batching, Tridentpv can promote the same in less than 30 ms while batching reduces the time to ~500 µs. Note that Tridentpv’s copy-less promotion is less useful for promoting 4KB pages to 2MB since the cost of copying 4KB pages is not significant. Hence, we employ copy-less promotion and compaction for 1GB pages only.

7. Evaluation

We evaluate Trident to answer the following questions. ① Can Trident help improve performance of memory-intensive applications over Linux’s default THP, and over a recent work, called HawkEye [35]? ② How important is Trident’s use of all large page sizes? ③ What are the sources of performance improvement for Trident? ④ How does Trident perform under virtualization? ⑤ Finally, how does Tridentpv impact page promotion/compaction the guest OS?

Performance under un-fragmented physical memory: Figure 11 shows the normalized performance for four configurations (higher is better) – ① Linux’s THP, ② HawkEye, ③ Trident1G-only and ④ Trident. HawkEye is the most recent related work that improved upon THP and other previous works (e.g., [30]). It does so by efficiently allocating 2MB pages to memory regions that suffer the most from TLB misses [35]. This enables us to compare Trident’s performance to current state-of-the-art. Trident1G-only denotes the configuration where Trident is disallowed to use 2MB pages. The difference between Trident1G-only and Trident highlights the importance of leveraging all large page sizes.

For each application, there are four bars in the cluster corresponding to four configurations. The height of each bar is normalized to the performance of the application under THP (Linux’s default configuration). Measurements in Figure 11 were performed when the physical memory is un-fragmented.

First, we observe that Trident improves performance over Linux’s THP by 14%, on average and up to 47% for GUPS. Applications like XSBench, SVM, Btree, Canneal witnessed 4.1%, 11.2%, 15% and 30% performance improvements, respectively. Even if we exclude the micro-benchmark GUPS, performance improvement is 12%, on average, over THP.

Next, we observe that Trident also outperforms HawkEye by 14%, on average. This is expected due to the similarities between huge page management in Linux and HawkEye in an unfragmented system where both utilize 2MB pages aggressively to maximize performance.

Finally, there is a significant performance gap between Trident1G-only and Trident. Trident1G-only loses performance even relative to THP for several applications (e.g., Graph500, SVM). In hindsight, this is expected. Our analysis in the Section 4.3 revealed that these applications have significant portions of their virtual memory that is 2MB-mappable but not 1GB-mappable. Further, these portions also witness a relatively larger number of TLB misses. Trident1G-only is forced to map these 1GB-unmappable regions with base 4KB pages and thus have more translation overheads compared to Trident that could deploy 2MB pages. In the process, Trident1G-only’s benefits from using 1GB pages are more than negated by the overheads of mapping frequently accessed memory with 4KB pages.

A keen reader will also observe that Trident1G-only performs much worse than 1GB-Hugetlbfs (Figure 2, Section 4.1) al-
though neither of them uses 2MB pages. The reason is libHugeTLBFS maps the entire chosen segment of an application’s memory (here, heap) with 1GB pages, irrespective of the sizes of allocation requests. For example, even if an application does a malloc for 12KB memory, libHugeTLBFS will map it with 1GB pages. Thus, the question of 1GB-mappable vs. 2MB-mappable virtual address region does not arise under its static memory allocation mechanism. Since Trident1G-only enables dynamic memory allocation, it does not have any such luxury. Fortunately, Trident is able to more than makeup for it by utilizing all large page sizes while also retaining ease of programmability with dynamic allocation.

**Performance under fragmented physical memory:** Arguably, performance analysis under fragmented physical memory paints a more realistic execution scenario. Figure 13 shows the normalized performance under fragmented physical memory for the same four configurations as before. Trident speeds up applications even more under fragmentation. This is unsurprising since Trident’s smart compaction adds a further edge here. On average, it improves performance by 18% over THP and GUPS quickens by over 50%. Even excluding GUPS, the improvement is 13% over THP.

Trident also outperforms HawkEye in all cases. In some cases under fragmentation, HawkEye performed worse than THP (e.g., Memcached). Our discussions with the authors of HawkEye revealed that this might happen for large memory applications due to: 1) CPU overhead of kbinmanager kernel thread that estimates relative TLB miss rates in HawkEye and 2) potential lock contention between kbinmanager, khugepaged and page-fault handler.

Trident outperforms Trident1G-only by a good margin even under fragmentation. However, note that in cases where Trident1G-only performed worse than THP under un-fragmented physical memory, it performed almost equally under fragmentation. Here, THP could deploy a lesser number of 2MB pages due to lack of contiguous physical memory. This, in turn, reduces the performance gap between Trident1G-only and THP. The execution time for THP also increases due to compaction overhead, narrowing its edge further.

We also measured how often the fragmented physical memory prevents Trident from mapping an address with a 1GB page. Table 4 shows the percentage of attempts to allocate a 1GB page that fails due to fragmentation.

There are “NA” under page fault for Redis and Btree since the fault handler never attempts to allocate a 1GB page due to lack of 1GB-mappable virtual address range during faults. We observe that 71-94% of 1GB page allocations fail due to lack of contiguous physical memory. Even during page promotion, 1GB allocations fail often. This further reinforces the need to utilize all large page sizes. Even if the largest page size cannot be used, a smaller large page (2MB) possibly be deployed.

**Impact on page walk cycles:** Figure 12 shows the normalized fraction of page walk cycles for THP, HawkEye, Trident1G-only, and Trident under un-fragmented memory. Figure 14 shows the same under fragmentation. The reductions in the fraction of walk cycles with Trident over THP are significant – 38-85% under no fragmentation and 40-97% under fragmentation. Across all configurations, we observe that relative improvement in performance correspond to relative reduction in page walk cycles.

**Impact on tail latency:** Tail latency is an important for interactive applications (e.g., Redis) that need to abide by strict SLAs [30]. Table 5 reports 99 percentile latency of Redis with 4KB pages, THP, and Trident, under both un-fragmented and fragmented memory. Trident slightly improves tail latency, relative to both 4KB and THP. Trident avoids long latency 1GB page faults by employing asynchronous zero-fill and 1GB pages reduces TLB misses in the critical path.

**Performance under virtualization:** We measured the performance of applications running inside a virtual machine with Trident deployed both at the guest OS and at the hypervisor (KVM). We do not fragment memory. For comparison, we do the same with HawkEye too. Figure 15 shows the speedups, normalized to THP deployed in the guest OS and KVM. Under virtualization, Trident improves performance by 16% on average, over THP and by 15% over HawkEye. Canneal saw

Table 4: Percentage 1GB physical memory allocation failures

| Application | 4KB-only | 2MB-THP | Trident |
|-------------|----------|---------|---------|
| XSBench     | 94       | 13      | 8       |
| SVM         | 88       | 19      | 32      |
| Graph500    | 91       | 38      | 25      |
| Memcached   | 43       | 81      | 12      |

Table 5: Tail latency analysis for Redis

| Application | No-fragmentation | 4KB-only | 2MB-THP | Trident |
|-------------|------------------|---------|---------|---------|
| Promotion   | 47.5 ms          | 50.3 ms | 46.6 ms |         |
| Promotion   | 53.3 ms          | 53.3 ms | 52 ms   |         |
biggest improvement (50%), but other applications also benefited significantly. For example, SVM and Graph500 witnessed 6% improvement each.

Performance with Trident⁺⁺: When the gPA gets fragmented over time, the guest OS must compact and promote pages with the help of khugepaged thread. However, a significant CPU usage by khugepaged in the guest OS could mean wasted vCPU time (cost) for a tenant in the cloud. In fact, Netflix reported how their deployments on Amazon EC2 can get adversely effected by high CPU utilization by THP’s khugepaged [28]. We, therefore, evaluate Trident⁺⁺ with fragmented gPA but limit khugepaged’s CPU utilization in the guest to maximum of 10% of a single vCPU. This setup helps to find out whether Trident⁺⁺’s faster copy-less promotion/compaction can be useful to use 1GB pages where CPU cycles are not free.

Figure 16 shows the performance of Trident and Trident⁺⁺ normalized to THP. Trident⁺⁺ is more effective than Trident for XSBench, GUPS, Memcached, and SVM by 5%, on average and by up to 10%. We also observe that Trident⁺⁺ does not always improve performance over Trident. Recall that Trident⁺⁺’s hypercall-based copy-less approach is quicker than the copy-based approach only during promotion/compaction of 2MB pages to 1GB pages. Otherwise, the overhead of the hypercall and that of tracing and altering PTEs overshadows the benefits of avoiding copy. In applications such as BTree, Graph500, Canneal, 4KB pages are often promoted directly to 1GB pages without needing to go via 2MB pages limiting Trident⁺⁺’s scope for improving their performance.

Memory bloat: Large pages are well-known to increase memory footprint (bloat) due to internal fragmentation. Larger the page size more is the bloat. Trident causes bloat in two out of eight workloads. It adds 38GB and 13GB bloat for Memcached and BTree over THP. We were able to recover the bloat by simply incorporating HawkEye’s technique for dynamic detection and recovery of bloat by demoting large pages and de-deuplicating zero-filled small pages [35]. However, we do not make any new contribution here and tradeoff between bloat and large pages is well explored [30, 35].

Summary: We demonstrate that Trident significantly improves performance over THP and state-of-art academic proposal [35] under varied execution scenarios.

8. Related work

Address translation overheads is a topic of several recent research efforts spanning multiple fields [11, 18, 27, 31, 37, 40, 42].

Proposals that require hardware support: Hardware optimizations focus on reducing TLB misses or to accelerate page-walks. Multi-level TLBs, and multiple page sizes are found in today’s commercial CPUs [4, 22]. Further, page walk caches are used to make page walks faster [14, 19].

Direct segments [16] can significantly reduce address translation overheads through segmentation hardware. Coalesced-Large-reach TLBs increase TLB coverage through contiguity-aware hints encoded in the page tables [39]. This approach can also be combined with page walk caches and large pages [19, 22, 38]. POM-TLB reduces page walk latency by servicing a TLB miss using a single memory lookup with a large in-memory TLB [42]. SpecTLB speculatively provides address translation on a TLB miss by guessing virtual to physical address mappings [15]. ASAP prefetches translations to reduce page-walk latency to that of a single memory lookup [33]. It first orders page table pages to match that of the virtual memory pages and then uses a base-plus-offset arithmetic that directly indexes into the page tables. Large page support for non-contiguous physical memory has also been proposed [24]. Tailor page sizes use whatever contiguity OS can afford to allocate [29]. In contrast, Trident does not need new hardware; architectural support is complementary to Trident’s goal of fully utilizing large page support.

Proposals with only software support: Software-only solutions mainly focus on better use of large pages. Navarro et. al., proposed a reservation-based large page promotion in FreeBSD as compared to proactive large page allocation in Linux [34]. Ingens proposes to mix THP’s aggressive large page allocation with FreeBSD’s conservative approach to reduce memory bloat and latency while still leveraging large pages. Illuminator showed how unmovable kernel objects hinder compaction [36]. Quicksilver uses hybrid strategies across different stages in the lifetime of a large page. Superficially, it employs aggressive allocation, hybrid preparation, relaxed mapping creation, on-demand mapping destruction and preemptive deallocation to achieve high performance and lower latency and bloat [48]. Carrefour-LP showed how large pages can degrade performance in NUMA systems due to remote DRAM accesses and unbalanced traffic [26]. Trident is com-
plementary to these works; while these works focused on KBs and MBs-sized pages, Trident focuses on 1GB pages which brings its unique challenges for compaction and page promotion. Many insights from these works on 2MB pages are applicable to Trident too e.g., HawkEye’s fine-grained page promotion and Ingens’s adaptive approach of balancing trade-offs with large pages can be applied to Trident too.

Translation Ranger proposed a new OS service to actively create contiguity [47]. Finally, a recent proposal allows in-place compaction of physical memory [45]. This functionality, however, needs to be invoked via a special syscall and is unsuitable for applications that incrementally allocates memory (e.g., Redis). Mitosis [10] eliminates remote memory accesses due to page walks by replicating page tables on NUMA nodes; Trident can also help reduce the impact of remote accesses in page walks, as just a side effect. In a concurrent work to ours, code patches to enhance THP to support 1GB pages were recently posted on Linux mailing list [46]. This shows the Linux community’s growing interest in 1GB pages. However, unlike these patches that simply aim to enable 1GB THP allocation, our work comprehensively shows the type of workloads that could benefit from 1GB pages, deals with physical memory fragmentation via smart compaction and virtualizes 1GB pages via copy-less 1GB page promotion and compaction in TridentPs.

9. Conclusion

Application transparent support is crucial to the success of large pages. While OS support for 2MB pages has matured over the years, 1GB pages have received little attention despite being present in the hardware for a decade. We propose Trident to leverage architectural support of all three page sizes available on x86-64 systems, while also dealing with the latency and fragmentation challenges. Our evaluation shows that transparent 1GB pages, particularly in tandem with 2MB pages, provide a significant performance boost over 2MB THP in Linux. Further, the paravirtualized extension of Trident, called TridentPs, can effectively virtualize 1GB pages with copy-less guest page promotion and compaction. We hope that Trident’s 18% performance improvement over Linux THP motivates researchers to further explore the role of large pages, beyond 2MB, in building efficient large-memory systems.

Trident source will be available at https://github.com/csl-iiisc/Trident.

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