Radio frequency reflectometry in silicon-based quantum dots

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RF reflectometry offers a fast and sensitive method for charge sensing and spin readout in gated quantum dots. We focus in this work on the implementation of RF readout in accumulation-mode gate-defined quantum dots, where the large parasitic capacitance poses a challenge. We describe and test two methods for mitigating the effect of the parasitic capacitance, one by on-chip modifications and a second by off-chip changes. We demonstrate that these methods enable high-performance charge readout in Si/SiGe quantum dots, achieving a fidelity of 99.9% for a measurement time of 1 µs.

I. INTRODUCTION

Quantum computing promises significant speedup of computational tasks that are practically impossible to solve on conventional computers [1–4]. Of the physical platforms available, spin-based quantum bits (qubits) in semiconductors are particularly promising [5, 6]. Single-qubit gates with fidelities above 99.9% [7] and two qubit gate fidelities up to 98% [8, 9] have been demonstrated. Spin qubits in silicon are a strong candidate for realizing a large-scale quantum processor due to the small qubit dimensions, localized nature of the control, CMOS compatibility, long coherence times [10] and possibility of operating beyond 1 Kelvin [11, 12].

Charge sensing is an important technique for measuring spin qubits as their long-lived spin states can be converted into detectable charge states [13, 14]. To detect a charge state, a sensing dot (SD) is placed in close proximity to the qubit. The sensing dot’s resistance is strongly dependent on the charge state. However, measuring this resistance in DC with an amplifier at room temperature requires an integration time on the order of 30 µs – 1 ms due to the presence of noise and the RC time constant from the line capacitance and the amplifier input impedance. This slow readout forms a bottleneck when performing spin qubit experiments, since initialization and manipulation can be performed on the nanosecond or microsecond scale [15, 17].

Radio Frequency (RF) reflectometry [18] has been successfully applied to depletion-mode GaAs quantum dots and has enabled single shot readout with only several microseconds of integration time [19]. However, in accumulation-mode devices, the large parasitic capacitance of the accumulation gates to the two dimensional electron gas (2DEG) below provides a low-impedance leakage pathway to ground for the RF signal, complicating RF reflectometry measurements. Previous works have addressed this problem by the use of circuit board elements [20] and careful gate design [21, 22].

In this work, we further develop the theoretical model of the leakage pathway introduced by this parasitic capacitance and introduce an on-chip method that effectively removes these parasitic capacitances. We first apply this model in the “Ohmic-style” implementation, similar to GaAs, where the signal is sent through an ohmic contact. For this approach, we mitigate the effects of the capacitance by optimizing the onboard elements and sample design. Later we present the “split-gate style”, where the RF signal is carried by a gate which is capacitively coupled to the 2DEG [20]. The leakage pathway to the Ohmic contact is blocked by a resistive channel.

II. RF REFLECTOMETRY

In RF reflectometry a fixed-frequency signal is reflected off an impedance-matching inductive-capacitive (LC) tank circuit that is loaded with the SD with resistance $R_{SD}$, as shown in Figure 1c. In the experimental setup L is a lumped element inductor and $C_0$ represents the total capacitance to ground of the circuit board, a lumped element capacitor and the parasitic capacitance of the bond wires and the metal line connecting the bond pad to the implant region close to the quantum dot. The reflection coefficient of this circuit is given by $\Gamma = (Z - Z_0)/(Z + Z_0)$, where $Z$ is the impedance of the loaded tank circuit and $Z_0 = 50\Omega$ is the source impedance. When the device’s parasitic capacitance $C_{2DEG}$, the contact resistance $R_c$ and the resistance of the reservoir $R_{2DEG}$ can be ignored, the effective impedance of the loaded tank circuit is $Z = i2\pi f L + 1/(R_{SD} + i2\pi f C_0)$ at an input frequency $f$.

$\Gamma$ is strongly modulated near $\Gamma = 0$, which occurs at the matching condition $Z = Z_0$ when driven with $f$ equal to the resonance frequency $f_M = 1/(2\pi\sqrt{LC_0})$ and with
Figure 1. (a) Left: False-colored image of a scanning electron micrograph of a typical Si/SiGe overlapping-gate device. Right: Sample mounted and wire-bonded to a circuit board. (b) Sketch of the signal path for two approaches. For the ohmic approach the signal is applied to the SD through the ohmic contact and for the split accumulation gate approach the signal is sent through the accumulation gate. (c) Circuit diagram for the standard method used for GaAs devices. The bracketed section represents the distributed capacitance and resistance of the 2DEG below the gate. (d) Circuit diagram for the ohmic method. The distributed capacitance $C_{2DEG}$ and resistance $R_{2DEG}$ are replaced with lumped elements and absorbed into $C_g$ and $R_c$ for computational simplicity. (e) Circuit diagram for the split accumulation gate approach.

$R_{SD}$ equal to the matching resistance $R_M = L/C_0Z_0$. $R_{SD}$ is very sensitive to the electric potential at the SD and thus to the charges present in the nearby quantum dots. $L$ and $C_0$ are chosen such that the value of $R_M$ matches that where $R_{SD}$ is most sensitive to the qubit dot’s charge occupation, typically in the range of 50 – 500 kΩ.

In Si/SiGe quantum dots, this simple LCR circuit model fails because $R_{2DEG}$ and $C_{2DEG}$ are not negligible. Figure 1(a) shows a typical device (left panel) and circuit board onto which the device is glued (right panel). A quadruple quantum dot for qubits is formed with the lower set of gates and two sensors are formed with the upper gates. Large accumulation gates control the electron density of the leads from the Ohmic contacts to the quadruple dots and to the SDs. $C_{2DEG}$ between the 2DEG and the accumulation gates adds up to 0.1–1 pF in total. The RF signal passes through the lossy 2DEG channel with resistance $R_{2DEG}$ and is shunted to ground through $C_{2DEG}$ as shown in Figure 1(c), drastically reducing the sensitivity of $\Gamma$ to $R_{SD}$.

To overcome this problem, we demonstrate two alternative approaches as shown in Figure 1(b):

- **Ohmic approach** – the RF signal is sent through the Ohmic contacts. The effect of $C_{2DEG}$ and $R_{2DEG}$ is mitigated by optimizing the circuit board and sample design (Figure 1(d)).

- **Split accumulation gate approach** – the accumulation gate is split into two parts and the RF signal is sent to the SD through the large accumulation gate capacitively (Figure 1(e)). $C_{2DEG}$ becomes the path of the signal rather than a leakage channel.

We note that devices with split accumulation gates are used in the experiments demonstrating both methods below. The gate labeled ‘accumulation gate’ serves to accumulate the 2DEG used as the source reservoir for the sensing dot and the ‘lead gate’ accumulates a second 2DEG, connecting the reservoir 2DEG to the ohmic contact.

### III. Ohmic Approach

The ohmic approach is shown in Figure 1(b) and introduces the RF signal to the lead of the SD through the ohmic contact. The large $C_{2DEG}$ and $R_{2DEG}$ prevents applying the simple RLC model to accumulation-mode SiGe devices. For simplicity, the distributed $C_{2DEG}$ and $R_{2DEG}$ in Figure 1(c) can be treated as a single capacitance, $C_g$, and single resistance, $R_c$ as shown in Figure 1(d). The gates are connected to ground by two channels: the line resistance $R_b$ to the DC voltage supply which serves as RF ground, and the parasitic capacitance $C_p$ to ground from all the metal on the sample side of $R_b$ (gate, bond wire, bond pad, PCB trace). We will begin by exploring how the tank circuit parameters ($R_b$, $C_p$, $C_0$, and $L$) and the device parameters ($R_c$ and $C_g$) affect the matching conditions ($f_M$ and $R_M$). This understanding will then be applied to demonstrate several key strategies that allow for Ohmic-style RF reflectometry in Si/SiGe accumulation-mode devices. The goal is to achieve $R_M$ and $f_M$ values that are experimentally achievable and to ensure the majority of the power is dissipated in $R_{SD}$ resulting in a usable signal-to-noise ratio (SNR).

Prevent shunting to ground through $C_g$. The RF signal in the lead 2DEG has a low impedance path to the accumulation gates through $C_g$. In order to block this pathway, we have designed the printed circuit board (PCB) to have surface mount resistors to increase $R_b$ between the sample bond pads and the RC filters. $C_p$
Control matching with \(C_0\) and \(L\). When a sample is fabricated, \(C_g\) and \(R_e\) are roughly fixed, meaning that the only way to change \(R_M\) and \(f_M\) is through the tank circuit parameters \(L\) and \(C_0\). We present solutions of \(f_M\) in Figure 2(a) and \(R_M\) in Figure 2(b) as a function of \(L\) and \(C_0\) with \(C_g^* = 0.2\) pF and \(R_e = 3\) k\(\Omega\). We note that far from the non-matching regions, the behavior is approximately that of the standard LCR model. Under these conditions, \(C_0 \gg C_g\) which means that \(C_0\) dominates the capacitance of the loaded tank circuit. When \(C_0\) is comparable to or smaller than \(C_g\), \(R_M\) diverges.

In order to tune \(C_0\) and \(L\), our PCB has been designed with solder pads for a surface mount inductor, \(L\), and a surface mount capacitor to control \(C_0\). The board parasitic capacitance also provides a significant contribution (~1 pF) to \(C_0\) and sets a lower bound for possible values of \(C_0\). The ground plane near the tank circuit should be minimized to reduce this board parasitic capacitance, ensuring the tunability of the tank circuit by \(C_0\) and \(L\).

Following the prediction of the model, we tested lumped elements with \(L = 6.8\) \(\mu\)H and \(C_0 = 3.0\) pF for a device with estimated \(R_e = 4\) k\(\Omega\) and \(C_g = 0.5\) pF \((C_g^* = 0.2\) pF). The result in Figure 2(e) demonstrates impedance matching behavior with a usable \(R_M\). However, it comes at a cost of a very low and unusable \(f_M\). Practically, we need \(C_0\) to be as low as allowed by \(C_g^*\) to guarantee a \(f_M\) that is above 100 MHz. For this reason, it is important to reduce \(C_g\) and thus \(C_g^*\).

Balancing \(C_g\) and \(R_e\) in sample design. The dependence of the matching conditions is strongly dependent on \(R_e\), as shown in Figure 2(c). At \(R_e = 0\), the model is reduced to the standard LCR model with an effective \(C_0^* = C_0 + C_g\). The range of \(L\) that can achieve matching is drastically reduced as \(R_e\) increases, since more rf power would be dissipated by \(R_e\) before \(R_{SD}\). Reducing \(R_e\) is therefore key to achieving RF reflectometry. To capture the impact of \(C_g^*\), we present a simulation of the dependence of \(R_M\) in on \(C_g^*\) and \(C_0\) in Figure 2(d). We again observe that matching is only achieved when \(C_0\) is large enough compared to \(C_g\).

The sample design impacts both \(C_g\) and \(R_e\), both of which we want to minimize, through the length \(l\) and width \(w\) of the accumulation gate. Knowing that \(C_g \propto l w\) and \(R_e \propto l / w\) reveals that decreasing \(l\) is ideal for both parameters while decreasing \(w\) to improve \(C_g\) comes at the cost of increasing \(R_e\) and vice versa. We have found that \(w = 5\) \(\mu\)m is sufficient to achieve consistent accumulation for usable \(R_e\) without increasing \(C_g^*\) drastically. In the future we would place Ohms as close to the SD as possible to limit \(l\) as in [21]. The optimized result is demonstrated in Figure 2(f), where we plot the reflected power \(S21\) in the upper panel as a function of \(f\) and \(R_{SD}\). We apply \(V_L = 1\) V on the lead gate to fully turn it on and thus minimize \(R_e\). With this we achieved both a usable \(R_M \sim 100\) k\(\Omega\) and \(f_M = 220\) MHz.

Tuning \(R_e\). To experimentally confirm the dependence of \(R_M\) on \(R_e\), we make use of the lead gate. When \(V_L\) is small, the lead gate is partially turned on and thus leads
to a larger $R_c$. The lower panel in Figure 2(f) shows $S_{21}$ at $f_M$ as a function of $R_{SD}$ when $V_L = 1$ V and 0.45 V. The best matching is achieved with 67 kΩ for the minimized $R_c$, and 200 kΩ for a larger $R_c$, which agrees with the simulation in Figure 2(c). This tunability also allows the use of fixed $C_0$ and $L$ for general devices as the matching condition of the device can be tuned in situ. This tunability, however, is not ideal since the larger $R_c$ gets, more energy is lost before the sensor dot, resulting in a reduced signal to noise ratio.

IV. SPLIT GATE APPROACH

In this approach, the RF signal is sent to the sensing dot via the accumulation gate instead of via the Ohmic contact (Figure 1(b)) [20]. The capacitance $C_g$ between the accumulation gate and 2DEG allows the RF signal to couple in to the 2DEG, as shown in Figure 1(e). The lead gate is used to generate a high-impedance channel to the Ohmic contact, preventing leakage of the RF signal.

We aim for similar design specifications for this method as for the Ohmic method: a matching resistance ($R_M$) ranging from 200 kΩ to 600 kΩ and a resonance frequency ($f_M$) larger than 100 MHz. We simulated $f_M$ and $R_M$ for different circuit configurations. We estimated $C_g$ to be 100 fF from the sample design and $R_{lead} = 10$ MΩ. We varied the parasitic capacitance ($C_p$) and the inductance ($L$), as these are parameters controllable by the device design and inductor choice. From the simulation results in Figure 3 we find a large parameter space that achieves the desired matching condition for practical values of $L$ up to about 5 µH as long as $C_p < 0.3$ pF. In this case, the circuit reduces to the standard LCR model [24] given that the reactance of $C_g$, $\chi_g = \frac{1}{2\pi f C_g} << R_M$ and $R_{lead} >> R_{SD}$. We also simulated the expected measurement bandwidth at the matching condition of this circuit. We only see a weak dependence of the bandwidth on $L$ and $C_p$. The bandwidth of the circuit ranges from 0.5 to 1 MHz.

For the devices used to demonstrate the split accumulation gate approach, we estimated by simulation the total parasitic capacitance to be around $C_p \sim 250$ fF. The parasitic capacitance was kept low using a compact gate layout and high-kinetic-inductance resonators as inductors [24]. We choose an inductor (resonator) value of $L=3.4$ µH, which leads to a resonance frequency of ~180 MHz and a matching resistance of 300 kΩ for the sensing dot. When operating the device, leakage to the Ohmic contact was cut off by tuning $R_{lead}$ above 10 MΩ.

Figure 4(a) shows the response of the resonator versus frequency for several values of $R_{SD}$, with $f_M = 170$ MHz. In Figure 4(b), we find $R_{SD} = 275$ kΩ. The circuit bandwidth can be extracted from the full-width-half-max (FWHM) of the resonance line. For $R_{SD}$ equal to $R_M$, the bandwidth is 0.8 MHz which means that we cannot measure signals faster than ~600 ns. Two sensitive regions that depend strongly on $R_{SD}$ are visible in Figure 4(b), as indicated by the red and green colored area. The inset shows the expected response of the circuit in the IQ plane around $R_M$. The red and green region can by differentiated by a phase $\pi$ in the measured signal. In practice, the coax line between the sample and the measurement circuit adds an unknown phase. In order to maximize the signal-to-noise ratio (SNR), we record both I and Q and convert the result to a scalar. The resistance $R_{SD}$ was roughly 400 kΩ–1 MΩ, just above $R_M = 275$ kΩ. This means we could improve the SNR by a factor 2 by reducing $C_p$ from 250 fF to 150 fF (smaller gate footprint) or increasing the inductance $L$. This would allow for a
value of $R_M$ around 600 kΩ.

To characterize the readout performance, we measured the charge readout fidelity ($F_R$). This fidelity is defined as the probability to correctly determine whether a quantum dot is occupied with no ($N=0$) or one ($N=1$) electron. To estimate $F_R$, we send a train of 10,000 square pulses to the target quantum dot. The dot-reservoir tunnel time is several orders of magnitude shorter than the periods used in the experiment, which means the quantum dot charge state tracks the square pulse. We sample the IQ signal for each half period of the square pulse and plot the distribution for both half periods as shown in the inset of Figure 4(c). The overlap of both signals is the reported infidelity ($1-F_R$). For these measurements, we used a digital filter (FIR type) with a passband between 100 kHz and 2.5 MHz. The lower frequency of the passband was determined by the slowest signal we wanted to detect (5 µs in this case). The upper frequency was taken larger than the bandwidth of the matching circuit to not limit the measurement speed.

Figure 4(c) plots the readout infidelity $1-F_R$ versus the measurement time when we apply an input signal power ($P_{in}$) of -93 dBm to the readout circuit. We find a minimum measurement time of $t_{99.9\%} = 780$ ns in order to achieve $F_R > 99.9\%$. We see that $t_{99.9\%}$ strongly depends on the input power of the RF-readout circuit (Figure 4(d)). The SNR is improved by larger $P_{in}$ until the bandwidth limit of the circuit is reached (0.8 MHz). On the other hand, larger $P_{in}$ also affects the effective electron temperature of the quantum dots. To characterize the trade off, we measured $T_e$ by measuring the polarization line of an interdot transition [25] and plot the result as a function of $P_{in}$ in Figure 4(d). We note that $T_e$ starts to increase dramatically once $P_{in} > -$93 dBm. We recommend to only supply power to the RF readout circuit when readout is being done, to prevent the readout from affecting qubit operations.

V. CONCLUSION

In this work we demonstrated two methods that can be used to achieve a reasonable matching condition for RF reflectometry measurements in accumulation mode devices. For the Ohmic method, we demonstrate that circuit board design can be used to minimize the parasitic capacitance. A careful sample design is necessary in order to obtain both a workable frequency and matching resistance. For the split accumulation gate method, the RF source is directed to the accumulation gate of the sensing dot, and the addition of the lead gate allows to efficiently cut off the leakage path to the Ohmic contact. The charge state of a qubit dot can be read out within 1 µs with a >99.9\% fidelity, which matches state-of-the-art readout performance. Compared to existing methods demonstrated in recent works [21, 22], the split accumulation gate method is especially useful when it is difficult to achieve very low $C_g$ and/or to keep $R_{2DEG}$ sufficiently low.

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