Design and Analysis of Low power Analog to Digital Converter using CMOS Technology

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Abstract: This Paper introduces conventional resistor less analog to digital converter circuit using Microwind 3.1 VLSI Backend Software For any type of applications such as in signal processing we require digital signals for processing so to convert analog-signals into digital “Analog to digital converter” is used. Nowadays for reducing chip size area designers searching analog to digital converter architectures using CMOS techniques. The performance of any digital system depends on the performance parameter of analog to digital converter. The results came from the proposed module shows the circuit made in 32nm technology consumed less power which is 2.659mW.

Keywords: Analog to digital converter, low power, resistorless, switched inverter scheme (SIS) Comparator.

I. INTRODUCTION

Analog-to-digital converters (ADCs) are main design blocks in modern digital communication systems. The A/D conversion is a quantizing process whereby an analog signal is converted into equivalent binary word. The performance parameters of ADC are resolution, quantization error, conversion time. There are various types of ADCs using various techniques which are single ramp ADC, ADC using DAC, Flash ADC. The proposed work is concentrated on the parameters like power consumption, chip area and efficiency. Analysis is done with A to D converter using SIS, clocked SIS, SIS comparator with sleep transistor types.

II. LITERATURE REVIEW

Flash ADC Comparators and Techniques for Their Evaluation” proposed Flash ADC comparators and technique. In this paper they designed three flavors of a periodic comparator to minimize its phase-dependent nonlinearities. One flavor used a differential “quasi-one-junction” SQUID (DQOS) quantizer with a low-inductance clocking scheme. The second flavor used a differential SQUID wheel quantizer, and the third flavor used a symmetric differential SQUID wheel quantizer with time interleaved clocks. They also described a different common mode biasing scheme that gates the quantized signal to apply full signal during the clock aperture, and an attenuated signal outside the clock aperture. They also developed a new performance analysis scheme based on sweeping the dc offset of a single periodic comparator during beat frequency test while following the position of its threshold, which yield both signal reconstruction and duty cycle of the comparator. Using this, they discovered the dependence of the sensitivity of the comparator duty cycle to its dc bias and the slew rate of the signal.[1]

“4-Bit Flash Analog to Digital Converter Design using CMOS-LTE Comparator” proposed 4-bit, 1.8V Flash Analog to Digital Converter (ADC) design using CMOS-LTE (CMOS Linear Tunable Transconductance Element) Comparator with 500nm technology. In their work they used reference voltages were generated by systematically sizing the transistors of the comparators, thus completely eliminating the resistive ladder network required for the architecture. They designed and simulated TIQ Comparator Flash ADC and CMOS-LTE Comparator Flash ADC with 500 nm technology.[2]

“New Flash ADC Scheme With Maximal 13 Bit Variable Resolution and Reduced Clipped Noise for High-Performance Imaging Sensor” proposed flash ADC with 13 bit variable resolution. In their work they presented a high-performance complementary metal–oxide–semiconductor (CMOS) imager with a new analog-to-digital-converter (ADC) scheme. The new ADC scheme, adopting the visual perception of human eyes, has realized a maximal 13 bit variable resolution and reduced clipped noise for imaging. This ADC architecture used an adjustable reference at both the top and bottom of the series of nonuniform resistors to reduce the clipped noise and to provide a wide dynamic range to image sensors. The sensors with the newly developed ADC scheme are fabricated by the 0.18-μm CMOS process. The test results show improved image quality compared to typical CMOS products with a linear ADC. Test results also showed 79-dB signal-to-noise ratio (at gain = 0 dB) with a power consumption of 90 mW at 54 MHz. [3]
“55-mw 300-MHz Analog – Digital Converters using Digital VLSI technology” proposed Analog to Digital Converter using Digital VLSI technology. In their work they presented two versions of ADC that is selected transistors in comparator were designed with channel length of 1.6 micron in one version and 1.2 micron in another. In their final work they shows the statistical difference in DNL between these two versions of ADC designs at 3 sampling frequencies from 30 chips (1920 comparators). The additional 0.4 micron channel length slightly improves the differential non-linearity at lower sampling frequency, and the improvement is more pronounce at higher frequencies. The probability that the DNL is less than 0.5 is 90 %.[4]

“Design of Analog to Digital Converter Using CMOS Logic” proposed Analog to Digital Converter Using CMOS technology. In their work they designed a 3-bit flash ADC using Threshold Inverter Quantization technique with 130nm CMOS technology for high speed and low voltage applications. Threshold Inverter Quantization (TIQ) is a unique way to generate a comparator for a high speed CMOS flash ADC. They improved the fat tree encoder that is highly suitable for the ultrahigh speed flash ADCs. The fat tree encoder was an effective solution for the bottleneck problem in ultra-high speed ADCs. The proposed A/D converter was suitable for System on Chip (SoC) applications in wireless products and other ultra-high speed applications.[5]

III. PROPOSED WORK

The circuit diagram of Analog to digital converter is

![Figure: Circuit of Analog to digital converter](image)

We used three types of comparators. These are
1) Switched Inverter Scheme (SIS) Comparator.
2) Clocked SIS comparator
3) SIS comparator with sleep transistor.

To achieve the proposed target following steps are included in the design and analysis of resistorless analog to digital converter.

1) Design different types of comparators using CMOS circuits.
2) Comparison of all the comparators and their performance measurement.
3) Design of gain booster and code converter using CMOS transistors.
4) Design of ROM encoder using CMOS transistor.
5) Design of ADC using comparator, gain booster and ROM encoder.
6) Performance analysis and Comparison

IV. DESIGN METHODOLOGY

1) Switched Inverter Scheme (SIS) Comparator:

When focusing on overall power for an ADC, the power dissipation of the comparator is important contributor. In case of n bit flash converters the number of comparator equals 2n-1. The switched inverter scheme (SIS) also called Threshold inverter quantization (TIQ) comparator has very simple architecture. It is quite different than the conventional operational amplifier based differential input voltage (DIV) comparator. The key difference between the DIV comparator and the (SIS) comparator scheme lies in the way the reference voltage is generated for each level. In DIV comparator conventional method of using resistor ladder is utilized for externally generating the reference voltage. Whereas in the SIS comparator scheme all 2n-1 reference voltage for an n bit ADC are set internally by adjusting the threshold voltage of each voltage comparator separately by sizing the transistor properly. All DIV comparators are identical and duplicated for 2n-1 times but each SIS comparator is altogether different from others and obtained by varying the ß ratio of the inverters. The SIS comparator design consists of two pairs of inverters connected back to back. Each of the inverter is sized separately to get a unique switching voltage. The cascaded inverters then work as voltage comparator. The full scale voltage range (VFSR) is equally divided by 2n-1 SIS comparators.
Figure: SIS comparator

VLSI Design of SIS comparator:

Design specification of SIS comparator:

| CMOS Technology | 32nm |
|-----------------|------|
| Chip area       | Width: 1.5µm  |
|                 | Height: 1.0 µm |
|                 | Surf: 1.4 µm^2 |
| 2 NMOS          | N1: 0.220×0.060 µm |
|                 | N2: 0.200×0.040 µm |
| 2 PMOS          | P1: 0.200×0.060 µm |
|                 | P2: 0.200×0.040 µm |
| Vdd             | 0.35 V |
| Vdd High        | 1.20 V |

Output Waveform of SIS Comparator:
2) Clocked SIS comparator

Another type of the comparator is clocked SIS comparator (CSIS) uses two cascaded inverters as SIS and two set of PMOS and NMOS connected in parallel. Each pair connected to pull up and pull down networks of the SIS inverter. The pair of PMOS and NMOS is driven by a clock pulse the NMOS is connected to clock whereas PMOS to clockbar. The two pairs are sized to minimum length and width in nm technology to get reduction in static power dissipation of the overall voltage comparator. The saving in power dissipation with the modification is approximately 60.37% to that of the SIS comparator.

Figure: Clocked SIS comparator

VLSI design of clocked SIS comparator

Design specification of Clocked SIS Comparator:

| Specification       | Value                      |
|---------------------|----------------------------|
| CMOS Technology     | 32nm                       |
| Chip area           | Width: 2.5µm               |
|                     | Height: 3.3 µm             |
|                     | Surf: 8.2 µm²              |
| 5 NMOS              | N1: 0.260x0.060 µm         |
Output waveform of Clocked SIS Comparator:

3) SIS comparator with sleep transistor
The comparison circuit of SIS comparator is modified by addition of high threshold PMOS and NMOS near the supply rails. The addition of header & footer reduces the static power dissipation to a great extent due to increased resistance of the high threshold PMOS and NMOS transistors. During the period of no activity the section not in use remains completely off. Whereas, the components are invoked again when any activity is detected. A Local sleep transistor network is used here as opposed to global level network, because every comparator is differently sized and hence the current through each comparator section is also different.

Figure: SIS with Sleep Transistor
VLSI Design of SIS with sleep transistor:

Output waveform of SIS with Sleep transistor:

Design specification of SIS with sleep transistor:

|                         |                  |
|-------------------------|------------------|
| CMOS Technology         | 32nm             |
| Chip Area               | Width: 2.5 µm    |
|                         | Height: 3 µm     |
|                         | Surf: 7.9 µm²    |
| 4 NMOS                  |                  |
| N1: 0.260x0.060 µm      |                  |
| N2: 0.280x0.040 µm      |                  |
| N3: 0.200x0.040 µm      |                  |
| N4: 0.200x0.040 µm      |                  |
| 4 PMOS                  |                  |
| P1: 0.260x0.060 µm      |                  |
| P2: 0.300x0.040 µm      |                  |
| P3: 0.200x0.040 µm      |                  |
| P4: 0.200x0.040 µm      |                  |
| Vdd                     | 0.35 V           |
| Vdd High                | 1.20 V           |
ROM encoder Circuit:
The encoder converts the thermometer code to binary code in two steps. In the first step the thermometer code is converted into one out of \( n \) code by using the truth table as shown in Table 1. The one out of \( n \) codes is then converted to binary code \( d_2, d_1, d_0 \) by Read only memory (ROM) encoder, as shown in Fig. The ROM encoder is a common and straightforward approach to encode the one out of \( n \) code to binary bit. The appropriate row \( m \) in the ROM is selected by using a row decoder that has the output of comparator \( m \) and the inverse of comparator \( m + 1 \) as inputs. The output \( m \) of the row decoder, connected to memory row \( m \), is high if the output of comparator \( m \) is high and the output of comparator \( m + 1 \) is low. The row decoder can be realized by, a number of 2-input NAND gates, where one input to each NAND gate is inverted. The main advantage of the ROM decoder approach is its regular structure that is easy to design.

![ROM Encoder Diagram]

Figure: ROM Encoder

VLSI Design of ROM Encoder:

Design specification of ROM Encoder:

| CMOS technology | 32nm |
|-----------------|------|
| Chip area       | Width: -16.0 \( \mu \)m  |
|                 | Height: -9.5 \( \mu \)m  |
|                 | Surf: -152.6 \( \mu \)m² |
| 8 NMOS          | N1: - 0.560x0.220 \( \mu \)m |
Output Waveform of ROM Encoder:

Analog to digital Converter with sleep transistor:

Design specification of ADC with sleep SIS transistor:

| CMOS technology | Width: 27.3 µm |
|-----------------|----------------|
| Chip area       | Height: 25.6 µm|
|                 | Surf: 700.5 µm²|
|   |   |
|---|---|
| **31PMOS** | **N1**: 1.120×0.220 μm  
**N2**: 1.920×0.220 μm  
**N3**: 0.680×0.260 μm  
**N4**: 1.100×0.240 μm  
**N5**: 0.600×0.200 μm  
**N6**: 0.600×0.200 μm  
**N7**: 0.560×0.220 μm  
**N8**: 0.560×0.220 μm  
**N9**: 0.260×0.0.60 μm  
**N10**: 0.260×0.060 μm  
**N11**: 0.280×0.040 μm  
**N12**: 0.340×0.06 μm  
**N13**: 0.280×0.040 μm  
**N14**: 0.260×0.060 μm  
**N15**: 0.260×0.060 μm  
**N16**: 0.280×0.040 μm  
**N17**: 0.260×0.080 μm  
**N18**: 0.280×0.040 μm  
**N19**: 0.280×0.040 μm  
**N20**: 0.260×0.060μm  
**N21**: 0.280×0.040 μm  
**N22**: 0.280×0.040 μm  
**N23**: 0.200×0.040 μm  
**N24**: 0.200×0.040μm  
**N25**: 0.200×0.040μm  
**N26**: 0.200×0.100 μm  
**N27**: 0.200×0.100 μm  
**N28**: 0.200×0.040 μm  |
| **P1**: 0.720×0.260 μm  
**P2**: 0.680×0.260 μm  
**P3**: 0.740×0.280 μm  
**P4**: 0.260×0.060 μm  
**P5**: 0.260×0.060 μm  
**P6**: 0.300×0.060 μm  
**P7**: 0.260×0.060 μm  
**P8**: 0.260×0.060 μm  
**P9**: 0.260×0.080 μm  
**P10**: 0.260×0.060 μm  
**P11**: 0.300×0.040 μm  
**P12**: 0.200×0.040 μm  
**P13**: 0.300×0.040 μm  
**P14**: 0.320×0.040 μm  
**P15**: 0.300×0.040 μm  
**P16**: 0.300×0.040 μm  
**P17**: 0.200×0.040 μm  
**P18**: 0.300×0.040 μm  
**P19**: 0.0200×0.100μm  
**P20**: 0.300×0.040 μm  
**P21**: 0.200×0.040 μm  
**P22**: 0.200×0.040 μm  
**P23**: 0.300×0.040 μm  
**P24**: 0.200×0.080 μm  
**P25**: 0.200×0.040 μm  
**P26**: 0.200×0.040 μm  
**P27**: 0.200×0.040 μm  
**P28**: 0.200×0.040 μm  
**P29**: 0.200×0.040 μm  
**P30**: 0.200×0.040 μm  
**P31**: 0.200×0.040 μm |
Output waveform of ADC with sleep SIS transistor:

V. CONCLUSION

This paper resulted a resistorless analog to digital converter with different comparators using CMOS transistors only which are made by using 32nm CMOS technology. The purpose of this work is to design a low-power resistorless ADC with a supply voltage of 1.2 V. The above result showed that the power consumption is very low which is 2.659 mW.

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