A Family of Discontinuous PWM Strategies for Quasi Z-source Nine-Switch Inverters

Sherif M. Dabour1, (Senior Member, IEEE), Ayman S. Abdel-Khalik2, (Senior Member, IEEE), Shehab Ahmed3, (Senior Member, IEEE), and Ahmed Massoud4, (Senior Member, IEEE)

1Department of Electrical Power and Machines Eng., Tanta University, Tanta 3111 Egypt
2Department of Electrical Power and Machines, Alexandria University, Alexandria, Egypt
3CEMSE Division at King Abdullah University of Science and Technology, KSA
4Department of Electrical Engineering, Qatar University, Doha, Qatar

Corresponding author: Sherif M. Dabour (e-mail: sherif.dabour@f-eng.tanta.edu.eg).

ABSTRACT This paper proposes a new family of discontinuous PWM strategies to control the quasi-Z-source nine-switch inverters (qZS-NSI). The presented strategies provide buck and boost inversion capabilities, and suitable for common-frequency and different-frequency modes of operation. Accordingly, two different shoot-through (ST) approaches are introduced and compared. The first approach uses three-leg ST, while the second uses single-leg ST to reduce the number of switching commutations, therefore minimizing switching losses. Both approaches can be implemented using simple-boost (SB) and maximum boost (MB) control methods. The operating principles, performance criteria, and PWM modulator of each scheme are introduced. Compared to the conventional PWM technique for the same output voltage gains, the proposed schemes ensure continuous input current with minimum ripples, and the voltage stresses on the switching devices and capacitors could be reduced in the proposed MB control schemes. Moreover, the effective switching frequency of upper and lower switches of all schemes is fixed and could be reduced by 1/3 from the switching frequency of the conventional technique of the qZS-NSI, while only the single-leg ST schemes ensure minimum effective switching frequency of the middle switches. The proposed modulation strategies are digitally implemented and tested on the LAUNCHXL-F28379D DSP. The feasibility of the proposed modulation schemes is confirmed via simulation and experimental results, which show good agreement with the theoretical analysis. Moreover, the presented strategies can be applied to other types of Z-source NSIs.

INDEX TERMS Dual output inverters, quasi-z source inverters, nine-switch inverter, carrier-based PWM

I. INTRODUCTION

Reducing converter size through reduced switch topologies and lower volume passives is an active research theme in power electronics. Conventional nine-switch inverters (NSIs) were proposed in [1] to supply two independent AC loads with only nine active switches instead of the twelve used in the conventional converter, as shown in Fig. 1. As a result, the converter switching losses, thermal stresses, and cost are eventually reduced [2]. The switch-count reduction in NSIs represents the main reason why such a topology received considerable interest in the literature.

The operation of this structure has already been practically confirmed for two different modes of operations: Different Frequencies (DF) mode, which can be used to drive two three-phase ac motors independently, and Common Frequencies (CF) mode, which can be used to control the operation of a six-phase motor [3]-[7]. Various carrier-based (CB), space vector PWM and model predictive control techniques have been proposed to achieve superior performance of the NSI for both DF and CF modes [1]-[4],[8]-[12]. The CB-PWM techniques are a simple and efficient approach to modulate the NSI switches. Fig. 2 shows four different CB-PWM schemes. Many researchers have assessed these schemes, as discussed in [8], [9]. Among these schemes, the discontinuous PWM (DM) with a sawtooth carrier wave scheme dramatically reduces the switching loss of the NSI with minimal low frequency and even harmonic distortion [9].

Literature has also shown that the NSI is a highly functional topology; it is well suited for various applications that require both CF and DF operating modes. The NSI, therefore, has a wide variety of uses, such as uninterruptible power supplies [2], drive systems [5]-[7], [13], charging and propulsion systems for EVs [14], reactive power compensation [15], wind energy [16], unified power quality conditioner [17], [18] and...
reactive power and current harmonic control for unbalanced systems [19].

Unfortunately, the NSI can only work in bucking mode. The output voltage gains are relatively low, especially in DF mode [1]-[12]. In the available literature, two standard solutions are presented for applications where high voltage gains are required. The first approach utilizes an extra boost dc-dc converter [14]. However, this method increases costs. The second method employs special impedance networks with the standard NSI [11],[20]-[24]. In these attempts, the Z-source NSI (ZS-NSI), quasi-Z-source NSI (qZS-NSI), and split-source NSI (SS-NSI) are used to overcome the voltage restriction problem of the NSI. In [11], [20], [21], to achieve the boosting capability in the ZS-NSI, each upper and lower inverter unit is considered as a virtual VSI with its specific modulator. Both modulators' generated signals are combined with additional shoot-through (ST) pulses using a multiplexing approach to control the NSI switches (B9). However, this approach is sophisticated and suitable only for DF mode. Moreover, the input current is discontinuous with high ripples. The qZS-NSI presented in [22] overcomes the input current's discontinuity in the ZS-NSI. Although [22] proposes simple carrier-based PWM approaches for the qZS-NSI, these methods still need appropriate adaptation to enhance NSI performance in terms of the number of commutations and input current ripples.

Research on the modulation and control techniques of the qZSIs has a long track in literature. The recent research in modulation and control of ZSI/qZSI aims to reduce the number of switching commutations [25]-[29], reducing the overall switching losses. An improved DM scheme based on the SVPWM approach that uses a 1L-ST modulator to achieve the maximum voltage gain of the ZSI is introduced in [25]. In this scheme, the number of switching commutations is decreased. A similar scheme but with a Carrier-based PWM concept has been presented in [26]. Moreover, another 1L-ST modulator to reduce both conduction and switching losses for the ZSI is proposed in [27]. Modified PWM strategies to reduce the switching losses of the qZS are presented in [28]. These strategies are based on the SVPWM concept and implemented by new carrier-based modulators. This work enhances the inverter switching characteristics and gives minimum switching losses.

To the best authors’ knowledge, no study to date has concerned with the improvement of the switching characteristics for the dual output qZS-NSIs. Therefore, this paper, based on the concepts of qZSLs, introduces a family of simple and powerful qZS-NSI control methods to improve the inverter switching characteristics. It can be generalized to other impedance network NSI topologies. It relies on the DM approach and appears acceptable for both CF and DF modes of operation and various ST control methods. For the presented DM schemes, new CB-modulators should be used to modulate the multiplexing of the B9 switches due to intrinsic differences between the operation of the NSI and qZS-NSI topologies.

The main features of the proposed schemes for qZS-NSI can be summarized as follows:
1) Provides dual three-phase outputs, while both boosting and bucking operations can be achieved;
2) Continuous input current operation with lower ripples;
3) No need for dead-time intervals;
4) The utilization of ST states increases inverter reliability;
5) The adopted DM schemes reduce the inverter’s switches commutations;
6) The qZS-NSI topology can be utilized for dual-output, six-phase operation, and ac-ac power conversion.

The topology’s main drawback is the higher stresses experienced by both NSI units on the middle switches. Given its many merits, the rest of this paper is organized as follows. Section II introduces the topology of qZS-NSI and its operating principles. Two main PWM strategies based on DM techniques with simple-boost (SB) and maximum boost (MB) control approaches are classified and presented in section III. These strategies are namely three-leg ST and single-leg ST. Sections IV and V present the detailed analysis and the basic concepts of the proposed DM schemes. Moreover, the boosting factor and voltage gain relationships, as well as the modulator of each scheme, are analyzed in detail. The design considerations for the analyzed schemes are presented in section VI. The proposed methods have been compared and assessed in section VII. Finally, Section VII deals with the simulations and experimental results.
II. QUASI Z-SOURCE NINE-SWITCH INVERTER

A. TOPOLOGY

The power circuit of the qZS-NSI and their equivalent circuits for different operating modes are shown in Fig. 3. In addition to a diode, an impedance network is inserted at the front-end of the standard NSI. This combination is used to boost the input dc-voltage using additional ST state combinations.

B. OPERATING PRINCIPLES

The equivalent circuits of the qZS-NSI during the ST and the non-ST states are shown in Fig. 3(b) and (c). From the steady-state analysis of the qZS-NSI, the boost factor, $B$, can be defined by (1);

$$B = \bar{v}_{dc}/E = 1/(1 - 2D_{ST})$$  \hspace{1cm} (1)

where $\bar{v}_{dc}$ is the peak dc-link voltage, $E$ is the input voltage and $D_{ST}$ is the average ST duty cycle, which depends on modulation and shoot-through control methods.

Based on the volt-second balance concept across both $L_1$ and $L_2$, the normalized capacitor voltages are expressed in (2).

$$\begin{align*}
\frac{V_{C1}}{E} &= \frac{1}{(1 - 2D_{ST})} \\
\frac{V_{C2}}{E} &= \frac{D_{ST}}{1 - 2D_{ST}}
\end{align*}$$  \hspace{1cm} (2)

Finally, the voltage-gain for each output unit of the inverter ($G_1$ and $G_2$) is defined as the ratio of the peak voltage-phases of each output to the input dc-voltage. Hence:

$$\begin{align*}
G_1 &= \bar{v}_{\phi1}/E = BM_1/2 \\
G_2 &= \bar{v}_{\phi2}/E = BM_2/2
\end{align*}$$  \hspace{1cm} (3)

III. PROPOSED DM TECHNIQUE FOR QZNSI

The standard DM scheme for NSIs was well described in the literature [8], [9], but several details that serve as the foundation for building the proposed DM strategies for qZS-NSI are first reported in this section. Then, the proposed modulation technique is presented.

A. CONVENTIONAL DM SCHEME FOR NSI

The duty cycles in the DM scheme of the NSI for the upper and lower units, respectively, $(d_j$ and $d_k$) are defined by (4);

$$\begin{align*}
(d_j &= v_0^j + v_{j1} + 1 \\
(d_k &= v_0^k + v_{k1})
\end{align*}$$  \hspace{1cm} (4)

where $d_j \geq d_k (0 \leq d \leq 1)$ and $v_0^j$, $v_{j1}$ and $v_{j2}$, $v_{k1}$ are the sinusoidal reference and zero-sequence signals (ZSS) for both units, respectively.

The sinusoidal references are defined by (5) [9]

$$\begin{align*}
(v_0^j &= M_1 \sin(\omega t - (n - 1)2\pi/3) \\
(v_0^k &= M_2 \sin(\omega t - (n - 1)2\pi/3 + \phi)
\end{align*}$$  \hspace{1cm} (5)

and the ZSSs are governed by (6).

$$\begin{align*}
v_{z1} &= 1/2(1 - \max(v_0^j)) \\
v_{zk} &= -1/2(1 + \min(v_0^k))
\end{align*}$$  \hspace{1cm} (6)

In (5), $\omega_1$ and $\omega_2$ are the frequencies in rad/s, $M_1$ and $M_2$ are the modulation indices of upper and lower units, respectively, the angle $\phi$ represents the phase angle between the two sets of output voltages, where $|\phi| \leq \pi$, and $n \in \{1, 2, 3\}$. In DF operating mode, to avoid the crossover between the duty cycles of each leg (e.g., $d_0$ and $d_0$ for leg 1), the modulation index is limited by $M_1 + M_2 \leq 2/\sqrt{3}$, while for the CF mode, their limit is $M_1 + M_2 \geq 2/\sqrt{3}$ depending on the phase angle $\phi$.

B. PROPOSED DM SCHEMES FOR QZNSI TOPOLOGY

As in the standard ZSI, to achieve the boosting action for the qZS-NSI, the zero switching states are partially or entirely replaced by the ST state. Quite obviously, due to the upward and downward level shift of the duty cycles to obtain a clamping operation in the DM approach, only one zero state $\{0, 0, 0\}$ is generated in the range of $M_1 + M_2 \leq 2/\sqrt{3}$, like the duty cycles drawn in Fig. 4. Therefore, the modulation range for the proposed schemes must be limited by $M_1 + M_2 \leq 2/\sqrt{3}$ in both DF and CF modes. Based on the volt-second balance concept, the zero-state duty cycle is equal to the corresponding region's height, which is varying, as shown in Fig. 4. It can be determined from (7);

$$d_0 = d_{j, min} - d_{k, max} \geq 0$$  \hspace{1cm} (7)

where $d_{j, min}$ and $d_{k, max}$ are the minimum and maximum envelop of upper and lower duty cycles, respectively.

The proposed modulation schemes are classified according to how they achieve the ST state as Three-Leg ST (3L-ST) and Single-Leg ST (1L-ST) approaches. In this paper, the SB and MB control methods are developed for both approaches with CF and DF modes of operations. In the SB method, $d_{ST}$ (the ST duty cycle) is constant and less than $d_0$, while in the MB method, the zero-state duration given in (7) is used for ST.

IV. THREE-LEG SHOOT-THROUGH DM APPROACH

This approach utilizes two additional ST envelope signals, namely $d_{e1}$ and $d_{e2}$ that are inserted in the zero-state region, as shown in Fig. 5(b) and (c) to achieve the ST mode.
Consequently, the total ST duty ratio during a switching period can be obtained from the ST envelope signal as follows

\[ d_{ST} = d_{e1} - d_{e2}. \] (8)

**A. USING SB CONTROL METHOD (3L-ST DM/SB)**

The ST envelope signals in this method (see Fig. 5(b)) are

\[ d_{e1} = 1 - \frac{\sqrt{3}}{2} M_1 \quad \& \quad d_{e2} = \frac{\sqrt{3}}{2} M_2 \] (9)

Based on (9), the ST duration, in this case, is constant, with an average value shown in (10).

\[ D_{ST} = d_{ST} = 1 - \frac{\sqrt{3}}{2}(M_1 + M_2) \] (10)

**B. USING MB CONTROL METHOD (3L-ST DM/MB)**

To achieve maximum boost, the ST envelopes (as shown in Fig. 5(c)) are defined by (11).

\[ d_{e1} = d_{f,min} \quad \& \quad d_{e2} = d_{k,max} \] (11)

Consequently, in this case \( d_{ST} \) is time-varying, output-frequency dependent, and equals the zero-state duty-cycle \( d_0 \) given in (7). Regarding the output frequencies, the average ST duty cycle, \( D_{ST} \) is a constant and given by (12).

\[ D_{ST} = 1 - \frac{3\sqrt{3}}{2\pi}(M_1 + M_2) \] (12)

**C. THREE-LEG ST MODULATOR**

Fig. 6(a) shows the proposed 3L-ST modulator of the qZS-NSI. It is suitable for both CF and DF modes of operation and SB and MB control methods. Firstly, the switches are modulated in the standard way like the conventional NSI by comparing the per-phase duty cycles \((d_j \text{ and } d_k)\) with the carrier wave to obtain the gating pulses of the upper and lower switches \((S_j \text{ and } S_k)\), while the pulses of the middle switches are obtained by XORing both gating sets. Then, the ST-mode generator compares the envelope signals \((d_{e1} \text{ and } d_{e2})\) with the common carrier in such a way to allocate the ST pulses during the zero-state \((0,0,0)\). This results in two logical signals \((g_{e1} \text{ and } g_{e2})\), which are governed by (13).

\[ g_{ST} = g_{e1} \cdot g_{e2} \] (13)

Finally, the ST pulses are logically added to that of the standard modulator to obtain the gating pulses of the qZS-NSI. Fig. 7 shows the duty cycles and gating pulses for both standard and qZS-NSI using the 3L-ST approach. It is evident from Fig. 6(a) that, using this modulator, the NSI-bridge goes to the ST state by turning ON all the switches simultaneously, resulting in an equal distribution of the ST current among them. Furthermore, each switch is continuously commutating with one-third of the ST current during the entire fundamental cycle. Another observation raised from Figs. 4, 7(a), and 7(b) is that the standard NSI has only seven commutations during each switching cycle, while the qZS-NSI has 10 and 8 commutations in the 3LST/SB and 3LST/MB control methods, respectively. This is owed to the application of ST pulses in all switches. Quite expectedly, the 3LST schemes produce higher switching losses under all operating conditions. Besides, it induces high ripples in the inductor currents. Based on the prior discussion, the following section's main objective is to avoid these harmful effects.

**V. SINGLE-LEG SHOOT-THROUGH DM APPROACH**

Alternatively, the 1L-ST approach can be utilized by inserting ST states in one leg during the zero-state. As can be observed from Fig. 4, four state transitions (e.g., Active-1, Active-2, Zero \((0,0,0)\), Active-3, and Active-4) occur in the standard NSI using the DM scheme. As a result, different approaches can be used to insert the ST interval in each switching cycle. Two 1L-ST schemes called DM4 and DM2 are proposed here. It is worth noting that the following constraints should be respected to obtain proper operation of the qZS-NSI with a reduced number of commutations and, therefore, the overall inverter switching losses:

1) The ST insertion should not affect active state length.
2) To maintain clamping operation, the active states A1 and A4 should be applied at the start and end of a switching cycle, respectively. As a result, one phase from the upper group is clamped to the positive dc rail and, another one from the lower group is clamped to the negative dc rail while the remaining phases are modulated.
3) The ST states are added immediately adjacent to the active states of the conventional NSI to ensure minimum commutations of the qZS-NSI switching devices.
4) In each scheme, equal ST sub-intervals are utilized to minimize the inductances in the impedance network.

**A. 1L-ST DM4 SCHEME**

1) USING THE SB CONTROL METHOD

In this scheme, the total ST period is equally divided into four sub-intervals per switching cycle \((d_{ST}/4)\), as shown in Fig. 7(c).
Each sub-interval is inserted immediately adjacent to one of the active states without affecting its length. The first ST state (ST₁) is inserted at the right of the active state A₁, while the last ST state (ST₄) is applied at the left of the active state A₄. The remaining two active states from the upper and lower groups (A₂ and A₃) are then shifted to the right and left by \(d_{ST}/4\), respectively.

Hence, the last two ST states (ST₂ and ST₃) are then applied. Thus, during a switching cycle, this scheme has eight-state transitions (e.g., A₁, ST, A₂, ST, Zero, ST, A₃, ST, A₄) with only seven commutations as in the standard NSI.

Again, scalar implementation of qZS-NSI using 1L-ST DM schemes is possible by modifying the duty cycles given in (4) to obtain the ST states.

In this approach, two duty cycles for each upper and lower switch are utilized. These duty cycles are spaced by the ST sub-interval \((d_{ST}/4\) in this case). Hence, the new duty cycles for the B₉ switches are given by (14):

\[
\begin{align*}
    d_{max,j,u}^* &= d_{max,i}^* = 1 \\
    d_{mid,j,u}^* &= d_{mid,i}^* \\
    d_{min,j,u}^* &= d_{min,i}^* - d_{ST}/4 \\
    d_{max,j,t}^* &= d_{max,i}^* - d_{ST}/2 \\
    d_{mid,j,t}^* &= d_{mid,i}^* + d_{ST}/2 \\
    d_{max,k,u}^* &= d_{max,k}^* + d_{ST}/4 \\
    d_{mid,k,u}^* &= d_{mid,k}^* + d_{ST}/4 \\
    d_{min,k,u}^* &= d_{min,k}^* + d_{ST}/4 \\
\end{align*}
\]

(14)

Finally, under this scheme, the total ST duty cycle is defined by (10). Fig. 5(c) shows the duty cycles of this scheme.

2) USING THE MB CONTROL METHOD

To obtain a maximum-boost operation, the total ST interval should be equal to that of the zero states, and therefore, the zero states will have vanished. Consequently, the ST states should be redistributed to achieve equal sub-intervals. As a result, only three ST sub-intervals are utilized in this scheme, as shown in Fig. 7(d), and the new duty cycles are given in (16), where \(\mu\) is given by (17).

Moreover, the waveforms of this scheme are shown in Fig. 5(d). Finally, it is essential to note that this scheme is called DM4 due to the utilization of 4 modified duty cycles to achieve the performance.

![FIGURE 5](image5.png)

**FIGURE 5.** The modulating and ST envelop signals for the proposed DM strategy. (Shaded areas represent the area of ST states.)

![FIGURE 6](image6.png)

**FIGURE 6.** Proposed DM modulators for qZS-NSI.
1) USING THE SB CONTROL METHOD

Here, the total ST duration is equally divided into two parts per switching cycle \((dST/2)\). Each interval is inserted between the active and the zero states without affecting their intervals, as shown in Fig. 7(e). Therefore, this scheme’s duty cycles are as given in (18) and shown in Fig. 5(e).

\[
\begin{align*}
\bar{d}_{\text{max},j,u} &= \bar{d}_{j,\text{max}} = \bar{d}_{\text{max},j,l} = 1 \\
\bar{d}_{\text{mid},j,u} &= \bar{d}_{j,\text{mid}} \\
\bar{d}_{\text{mid},j,l} &= \bar{d}_{j,\text{mid}} - \frac{dST}{3} \\
\bar{d}_{\text{min},j,u} &= \bar{d}_{j,\text{min}} - \frac{dST}{3} \\
\bar{d}_{\text{min},j,l} &= \mu \\
\bar{d}_{\text{max},k,u} &= \mu \\
\bar{d}_{\text{max},k,l} &= \frac{dST}{3} \\
\bar{d}_{\text{mid},k,u} &= \frac{dST}{3} \\
\bar{d}_{\text{mid},k,l} &= \mu \\
\bar{d}_{\text{min},k,u} &= -1 \\
\bar{d}_{\text{min},k,l} &= \bar{d}_{\text{min},k,l} = \bar{d}_{\text{min},k,l} = -1 \\
\mu &= \frac{1}{2}(1 - \sqrt{3}/2 (M_1 - M_2))
\end{align*}
\]

2) USING THE MB CONTROL METHOD

In this scheme, two adjacent ST intervals with the same length \((d_g/2)\) is used per switching cycle, as shown in Fig. 7(f). The duty cycles of this scheme are expressed in (19).

**FIGURE 7.** Duty cycles, carrier-wave, and corresponding switching signals during one switching cycle or sample period (a)-(b) for 3LST-DM schemes and (c)-(f) for 1LST-DM schemes of the proposed qZS-NSI.

\[
\begin{align*}
\bar{d}_{\text{max},j,u} &= \bar{d}_{j,\text{max}} = \bar{d}_{\text{max},j,l} = 1 \\
\bar{d}_{\text{mid},j,u} &= \bar{d}_{j,\text{mid}} \\
\bar{d}_{\text{mid},j,l} &= \bar{d}_{j,\text{mid}} - \frac{dST}{3} \\
\bar{d}_{\text{min},j,u} &= \bar{d}_{j,\text{min}} - \frac{dST}{3} \\
\bar{d}_{\text{min},j,l} &= \mu \\
\bar{d}_{\text{max},k,u} &= \mu \\
\bar{d}_{\text{max},k,l} &= \frac{dST}{3} \\
\bar{d}_{\text{mid},k,u} &= \frac{dST}{3} \\
\bar{d}_{\text{mid},k,l} &= \mu \\
\bar{d}_{\text{min},k,u} &= \bar{d}_{\text{max},k,u} = \bar{d}_{\text{max},k,l} = \bar{d}_{\text{mid},k,u} = \bar{d}_{\text{mid},k,l} = \bar{d}_{\text{min},k,u} = \bar{d}_{\text{min},k,l} = \bar{d}_{\text{min},k,l} = -1
\end{align*}
\]

**B. 1L-ST DM2 SCHEME**

Another 1L-ST DM scheme is proposed here. It is called the DM2 scheme. It modifies only two duty cycles. Also, both SB and MB control approaches are valid in this scheme.
\[
\begin{align*}
\{ d_{\text{max}.j.u}^* & = d_{\text{max}.j.l}^* = 1 \\
\{ d_{\text{min}.j.u}^* & = d_{\text{min}.j.l}^* \\
\{ d_{\text{min}.j.j}^* & = d_{\text{max}.j.j}^* = \mu \\
\{ d_{\text{min}.k.u}^* & = d_{\text{max}.k.u}^* = \mu \\
\{ d_{\text{mid}.k.u}^* & = d_{\text{mid}.k.l}^* \\
\{ d_{\text{min}.k.u}^* & = d_{\text{max}.k.u}^* \approx 1 \\
\{ B & \cdot D \approx D \\
\{ + & + D \\
\{ . & . \}
\end{align*}
\]

(19)

Fig. 5(f) shows the duty cycles of this scheme.

C. PROPOSED MODULATOR FOR 1L-ST DM SCHEMES
As an illustration, Fig. 6(b) shows the 1L-ST DM modulator. This modulator is suitable for DM4 and DM2 schemes and can be used in SB and MB modes. Using the duty cycles of DM4 or DM2 schemes, the inverter bridge is modulated as follows: the upper switch of each leg, \( S_j \) is turned ON when \( d_{j.u} \) is higher than the carrier-wave, while \( S_k \) is turned ON when \( d_{k.l} \) is lower than the carrier-wave. However, the gating signal of the middle switch of each leg, \( S_{jk} \) is governed by the logical operation in (20):

\[
S_{jk} = g_{ST.j} + S_j \otimes S_k + g_{ST.k}
\]

(20)

where \( g_{ST.j} \) and \( g_{ST.k} \) are the ST pulses due to the upper and lower duty cycles, respectively.

Observing Figs. 7(a) and 7(d), it can be noted that the DM4 scheme gives seven commutations per switching cycle like the NSI. Considering the 1LST modulator of Fig. 6(b) and the resulting switching signals of Fig. 7(a)-(d), it can be observed that ST states are obtained in the 1LST schemes via turning-ON the middle switches, \( S_{jk} \) of B9, which increases the burden of these common switches.

VI. DESIGN CONSIDERATIONS OF qZS-NSI

A. USING SB CONTROL METHOD
As in the qZSI, and based on the volt-second balance concept, the required inductance \( L = L_1 = L_2 \) and capacitance \( C_1 \) and \( C_2 \) for the qZS-NSI can be determined by (21) where \( \tilde{f_s} \) is the effective switching frequency, \( \Delta I_L \) is the current variation, \( I_{in} \) is the average input dc-current, and \( \Delta V_{C1} \) and \( \Delta V_{C2} \) are the peak-to-peak voltage ripples of \( C_1 \) and \( C_2 \), respectively.

\[
\begin{align*}
L & = \frac{d_{ST} \cdot V_{C1}}{\tilde{f_s} \cdot \Delta I_L} = \frac{(1 - D_{ST}) \cdot E}{\tilde{f_s} \cdot \Delta I_L} \\
C_1 & = \frac{I_{in} \cdot T_{sST}}{\Delta V_{C1}} = \frac{I_{in} \cdot \Delta V_{C1}}{\tilde{f_s}} \\
C_2 & = \frac{I_{in} \cdot T_{sST}}{\Delta V_{C2}} = \frac{I_{in} \cdot \Delta V_{C2}}{\tilde{f_s}}
\end{align*}
\]

(21)

In the SB approach, the ST duty cycle is constant and given by (10). Then, the required inductance and capacitance are as shown in (22).

It should be noted that the effective switching frequency on the dc-side varies from one scheme to another, as will be explained in the next section. Even though all SB control schemes have the same voltage gains, they require different inductances and capacitances.

\[
\begin{align*}
L & = \frac{\sqrt{3}(M_1 + M_2) \cdot E}{2(\sqrt{3}(M_1 + M_2) - 1) \cdot \tilde{f_s} \cdot \Delta I_L} \\
C_1 & = \frac{1}{2\Delta V_{C1} \cdot \tilde{f_s}} (2 - \sqrt{3}(M_1 + M_2)) I_{in} \\
C_2 & = \frac{1}{2\Delta V_{C2} \cdot \tilde{f_s}} (2 - \sqrt{3}(M_1 + M_2)) I_{in}
\end{align*}
\]

(22)

B. USING MB CONTROL METHOD
In general, the ST duty cycle in the MB approach is time-variant and has low-frequency components. It repeats at six times the fundamental frequency of the output voltage of qZSIs. However, in the qZS-NSI, there are dual outputs, and the output frequencies may be equal in CF mode or unequal in DF mode. Therefore, although the average value of the ST duty cycle is the same for both CF and DF, the frequency of the fundamental component of the ST duty cycle is varying and given by (23).

\[
f_{do} = 6 \cdot \text{gcd}(f_1, f_2)
\]

(23)

As a result, there are two components of the inductor current ripple: 1) high-frequency components due to the DM schemes’ switching nature and 2) low-frequency components due to the ST duty cycle variation. It should be noticed that the high-frequency component can be negligible compared to the low-frequency component in the evaluation of the impedance network passive components. Following the procedure used in [29] for the qZSI, the required inductance and capacitance for qZS-NSI can be calculated from (24);

\[
\begin{align*}
L & \approx \frac{\tilde{D}_{ST} \cdot \tilde{v}_{dc}}{2\pi f_{do} \cdot \Delta I_L} \\
C_1 & = \frac{\tilde{D}_{ST} \cdot I_{in}}{\Delta V_{C1} \cdot f_{do}} \\
C_2 & = \frac{\tilde{D}_{ST} \cdot I_{in}}{\Delta V_{C2} \cdot f_{do}}
\end{align*}
\]

(24)

where \( \tilde{D}_{ST} \) is the peak value of the fundamental component of the ST duty cycle for the MB control approach. Based on Fourier series expansion \( \tilde{D}_{ST} \) is obtained in the qZS-NSI (25).

\[
\tilde{D}_{ST} = \frac{3V^3}{35\pi} (M_1 + M_2)
\]

(25)

Thus, the values of impedance network elements (inductances and capacitances) are given by (26).

\[
\begin{align*}
L & \approx \frac{3V^3}{70\pi} (3V^3(M_1 + M_2) - \pi) \cdot f_{do} \cdot \Delta I_L \\
C_1 & \approx \frac{3V^3}{35\pi} (M_1 + M_2) \cdot I_{in} \\
C_2 & \approx \frac{3V^3}{35\pi} (M_1 + M_2) \cdot I_{in}
\end{align*}
\]

(26)

Equations (24)-(26) are used to determine the minimum inductance and capacitance for the MB approach.
VI. COMPARATIVE ASSESSMENT AND SIMULATIONS
This section introduces a detailed comparative assessment of the introduced DM schemes of qZS-NSIs described in this paper. This assessment includes the following aspects: steady-state analysis, current and voltage stresses, the effective switching frequency of all semiconductors, and the passive components requirements. Finally, the switching losses and the inverter efficiency are explored.

Note that a one kVA qZS-NSI has been designed and modeled via MATLAB/PLECS platforms to be used in the assessment. A constant dc voltage source of 100V is assumed to feed the inverter. The parameters of the impedance network, output filters, and loads are listed in Table I.

A. MODULATION AND STEADY-STATE EQUATIONS
Table II lists more evident visual comparisons among the analyzed schemes regarding steady-state equations of the qZS-NSI. Since the boosting factor \( B = \frac{V_{dc}}{E} \) is determined by the total average ST duration, \( d_{ST} \), regardless of the ST insertion manner. Therefore, the boosting ability and the corresponding output voltage gains of the qZS-NSI are the same while maintaining the same total ST duration.

![Graph showing the dependency of the Boosting factor.](image)

**FIGURE 8.** Results for analytical comparisons between the presented modulation schemes.

Consequently, the proposed modulation schemes can be subdivided into two groups (SB group and MB group), where each group has the same average ST duty cycle, i.e., the same voltage gain capability. Fig. 8(a) shows the dependency of the boosting factor of the qZS-NSI based on SB and MB control methods on the possible modulation indices. Moreover, the results of the analytical comparisons are shown in Fig. 8(b).

B. IMPLEMENTATIONS
The implementation procedure represents an important aspect that should be considered for the proposed DM schemes. Table III compares the analyzed DM schemes in terms of the number of duty cycles and ST intervals used in the implementation aspects. The complexity is determined based on the analyzed schemes’ implementation procedure using the enhanced PWM (ePWM) modules of modern DSPs. Although the 1L-ST schemes are complex in implementation, it has a minimum number of commutations.

C. EFFECTIVE SWITCHING FREQUENCY
From the prior discussion in the analysis parts of this paper, it has been observed that each scheme has a unique switching pattern. This yields different values of the effective switching frequency of semiconductor switches. Consequently, different dc-side passive elements are required. Table IV lists the effective switching frequency for the qZS-NSI topology as a function of the carrier frequency, \( f_s \).

Furthermore, the following conclusions can be made:

1) The effective switching frequency of upper and lower switches of the B9 is fixed at \( 2/3f_s \) in all schemes. This is owed to the nature of DM techniques, which have clamped modulating signals.

### TABLE I

| Parameter            | Value | Parameter | Value |
|----------------------|-------|-----------|-------|
| Supply voltage       | 100 V | Output filter inductance | 1 mH |
| Peak output voltage  | 100 V | Output filter capacitance | 4.7 μF |
| Load                 | 30 Ω  | Carrier frequency | 20 kHz |

### TABLE II

|                     | Proposed SB-Schemes (DM/SB, DM4/SB, DM2/SB) | Proposed MB-Schemes (DM/MB, DM4/MB, DM2/MB) |
|---------------------|---------------------------------------------|---------------------------------------------|
| \( d_{ST} \)        | Constant                                    | Variable                                    |
| \( d_{ST} \)        | \( 1 - \frac{\sqrt{3}}{2} (M_1 + M_2) \)     | \( 1 - \frac{3\sqrt{3}}{2\pi} (M_1 + M_2) \) |
| \( B = \frac{V_{dc}}{E} \) | \( \frac{1}{\sqrt{3}(M_1 + M_2)} - 1 \) | \( \frac{6\sqrt{3}(M_1 + M_2)}{\pi} \) |
| \( V_{C1}/E \)      | \( \frac{\sqrt{3}(M_1 + M_2)}{2\sqrt{3}(M_1 + M_2) - 2} \) | \( \frac{6\sqrt{3}(M_1 + M_2)}{\pi} \) |
| \( V_{C2}/E \)      | \( \frac{2 - \frac{\sqrt{2}}{2} (M_1 + M_2)}{\sqrt{3}(M_1 + M_2)} - 2 \) | \( \frac{\pi M_s}{6\sqrt{3}(M_1 + M_2) - 2\pi} \) |
| \( G_s \) (*)       | \( \frac{M_s}{2\sqrt{3}(M_1 + M_2) - 2} \) | \( \frac{\pi M_s}{6\sqrt{3}(M_1 + M_2) - 2\pi} \) |

\(*)\) The subscript \( x \) maybe 1 for the upper 3-phase group or 2 for the lower one.

### TABLE III

| Scheme       | ST pulses | Commutations | Duty cycles | Modulator | Implementation complexity |
|--------------|-----------|--------------|-------------|-----------|--------------------------|
| qZS-NSI      | DM/SB     | DM4/SB       | DM2/SB      | Fig. 6(a) | Simple                   |
| qZS-NSI      | DM/SB     | DM4/SB       | DM2/SB      | Fig. 6(a) | Normal                   |
| qZS-NSI      | DM/SB     | DM4/SB       | DM2/SB      | Fig. 6(b) | Complex                  |
| qZS-NSI      | DM/SB     | DM4/SB       | DM2/SB      | Fig. 6(b) | Complex                  |
2) The utilization of all switches of B9 for ST state in the 3L-ST DM schemes increases the total number of commutations, as shown in Table III. This increases the effective switching frequency of the middle switches, as shown in Table IV.

3) In the case of 1L-ST DM schemes (DM4 and DM2), the effective switching frequency of the middle switches are reduced to \( f_z \). Consequently, it can be predicted that the switching loss of these schemes will be reduced.

4) The effective switching frequency of the front-end diode, \( D \) is hugely different between the presented schemes. It has higher values for DM4 schemes. On the other hand, the 3L-ST DM scheme has a lower switching frequency on the dc-side.

### D. REQUIRED PASSIVE COMPONENTS AND RIPPLES

As can be observed from (22), the required inductances and capacitances in the SB control schemes are inversely proportional to the effective switching frequency for the same current and voltage ripples. Consequently, it can be found that the 3LST DM/SB scheme requires a higher inductance and capacitance than the other schemes. On the other hand, in the implementation of MB control schemes, the fundamental frequency of the impedance network \( f_{do} \), given in (23), instead of the effective switching frequency should be considered. This is owed to the presentation of low-frequency (LF) components in the dc-side, as concluded in Table V. Therefore, all MB schemes require higher inductances and capacitances than SB schemes for the same ripples. Fig. 9 shows the required inductance and the capacitance ratio between these control approaches for different voltage gains and operating frequencies.

On the other hand, to ensure the same voltage and current ripple magnitude under various operating conditions, different impedance network capacitances and inductances are required for each scheme. According to (22) and (26), the required \( L \), and \( C \) values to ensure the voltage ripple of 2% and current ripple of 25%, respectively, are determined, and the results are listed in Table VI.

It is worth noting that the impedance network, in practice, shall be designed based on the lowest value of the effective switching frequency to optimize the operation for all analyzed schemes. Based on the values listed in Table VI, the recommended chosen parameters of the 1-kVA qZS-NSI circuit's impedance network are 1.25mH and 470µF, respectively. The dc-link voltage, capacitor voltage, and inductor current waveforms are depicted in Figs based on these values. 10 and 11 for the presented modulation schemes.

Fig. 10 shows the ripple characteristics of the SB control approach. In this case, the modulation indexes are set to 0.3374 to obtain unity voltage gains for both outputs. It can be observed that the inductor current and capacitor voltage waveforms are free from low-order harmonics. Fig. 11 also shows the MB control schemes’ results, where the modulation indexes are set to 0.3561 to obtain the same voltage gains of the SB control approaches.

In both cases, the simulation results confirm and verify the functionality and the reported analysis of the proposed modulation strategies.

![Figure 9](image_url)

**TABLE V** IMPEDEANCE NETWORK REQUIREMENTS

| Switching frequency | SB Schemes | MB Schemes |
|---------------------|------------|------------|
| | DM | DM4 | DM2 | |
| dc-side LF components | No | No | No | Yes |
| dc-Passive components | Normal | Lowest | Low | Highest |

**TABLE IV** EFFECTIVE SWITCHING FREQUENCY

| Effective switching freq. | NSI [8],[9] | qZS-NSI |
|---------------------------|-------------|---------|
| | DM Scheme | DM4 Scheme | DM2 Scheme |
| Upper switches | \( \frac{1}{f_z} \) | \( \frac{1}{f_z} \) | \( \frac{1}{f_z} \) | \( \frac{1}{f_z} \) | \( \frac{1}{f_z} \) | \( \frac{1}{f_z} \) |
| Medium switches | \( f_z \) | \( 2f_z \) | \( \frac{4}{f_z} \) | \( f_z \) | \( f_z \) | \( f_z \) |
| Lower switches | \( \frac{1}{2f_z} \) | \( \frac{1}{2f_z} \) | \( \frac{1}{2f_z} \) | \( \frac{1}{2f_z} \) | \( \frac{1}{2f_z} \) | \( \frac{1}{2f_z} \) |
| Front-end diode | - | \( f_z \) | \( f_z \) | \( 5f_z \) | \( 4f_z \) | \( 3f_z \) | \( 2f_z \) |

**TABLE VI** PASSIVE ELEMENTS OF THE ImpEDANCE NETWORK OF 1 KVA qZS-NSI FOR THE ANALYZED MODULATION SCHEMES

| SB Schemes | MB Schemes |
|------------|------------|
| | DM | DM4 | DM2 |
| | | | 0.337 | 0.337 | 0.337 | 0.356 |
| \( \hat{v}_{dc} \) (V) | 594 | 594 | 594 | 562 |
| \( v_{c1} \) (V) | 347 | 347 | 347 | 331 |
| \( v_{c2} \) (V) | 247 | 247 | 247 | 231 |
| \( L \) (mH) | 1.75 | 0.35 | 0.60 | 4 |
| \( G_1 \) (µF) | 240 | 48 | 80 | 1300 |
| \( G_2 \) (µF) | 77 | 16 | 25 | 414 |
Moreover, the dc-link voltage and current measured values comply with the theoretical values for all cases.

E. VOLTAGE AND CURRENT STRESSES

1) VOLTAGE STRESSES

The boosting factor and capacitor voltages of the analyzed modulation schemes are listed in Table II, where \( V_{dc} \) is the peak dc-link voltage, which represents the voltage stresses across the different B9 switches. Fig. 6 shows the ratio of boosting factors between the presented schemes for the same output voltage gains of the two groups. It is worth noting that the voltage stresses on the switching devices and capacitors, which are proportional to the boosting factor, are lower in the MB control schemes versus SB schemes for the same voltage gains.

2) CURRENT STRESSES

As in all reduced switch count topologies, reducing the active switches of the B9 bridge leads to different current stresses in the inversion stage in the qZS-NSI configuration. This is owed to the middle switches that are shared between the upper and the lower inverter units. Table VII lists the current stresses defined as the peak current through the different semiconductor switches of the qZS-NSI using the analyzed DM schemes. The current stresses are determined as a function of the RMS value of the fundamental components of the output phase currents (\( i_{a1} \) and \( i_{a2} \)), the average value of the inductor current (\( I_L \)), and the peak-to-peak ripples of the inductor current (\( \Delta I_L \)).

It is crucial to note that the 1L-ST modulation schemes (DM4 and DM2) produce higher current stresses in B9 switches. This is due to achieving the ST state through one leg at a time. However, in the 3L-ST DM schemes, the ST current is divided on the legs. Meanwhile, the current stress on the impedance network's front-end diode is the lowest and the same for all schemes.

Fig. 12 shows the upper, middle, and lower switch currents for the first leg of the B9 (\( i_{s_a} \), \( i_{s_{ax}} \) and \( i_{s_x} \)) for the analyzed modulation strategies. As can be seen, the results confirm the analysis of the maximum current through the B9 switches.

TABLE VII

| Maximum switch current | DM   | DM4 and DM2 |
|------------------------|------|-------------|
| \( i_{s} \)           | \( i_{a1} + (2I_L + \Delta I_L)/3 \) | \( i_{a1} + 2I_L + \Delta I_L \) |
| \( i_{s_{ax}} \), \( i_{s_x} \) | \( (2I_L + \Delta I_L)/3 \) | \( 2I_L + \Delta I_L \) |
| \( i_{d} \)            | \( 2I_L + \Delta I_L \) |

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FIGURE 12. Simulation results of the one kVA qZS-NSI using the maximum-boost control method of the proposed modulation strategies.

FIGURE 13. Simulation results of the one kVA qZS-NSI using the maximum-boost control method of the proposed modulation strategies.

FIGURE 14. Simulation results of the one kVA qZS-NSI using the simple-boost control method of the proposed modulation strategies.
F. OUTPUT VOLTAGE AND CURRENT WAVEFORMS
Fig. 13 shows the output current and filtered output line voltage waveforms of the qZS-NSI using SB approaches. It can be observed that these results exhibit high-quality sinusoidal output currents and voltages. Moreover, Fig. 14 shows the FFT spectrum of the output line voltage \( v_{ab} \) using the SB approach. It can be seen from Fig. 14 that all schemes have the same fundamental peak voltage, \( V_{f1} \) (where \( V_{f1} = E \) due to \( \omega_c = 1 \)). However, the DM4 scheme has a minimum harmonic component at the dominant frequencies. This result reflects the dc ripple characteristics on the ac-side. Therefore, it can be concluded that the waveforms and FFT spectrum confirm the preliminary analysis and demonstrate the advantage of using the DM4 scheme over the other schemes.

In MB schemes, some variations in the dc-link voltage envelope can be observed, as shown in Fig. 11. These variations are occurred due to the use of variable magnitude ST periods to boost the supply voltage. As a result of these variations, lower and non-triple odd harmonic components are induced in the FFT spectrum. However, these components are not significant in DM schemes due to the third harmonic injection [22], [28], and their magnitudes in the qZS-NSI still small compared with those at the dominant frequencies. Moreover, another factor that reduces the effect of these harmonics is that to give the same voltage gains, the MB control methods use higher modulation indexes than the SB schemes, as can be observed from Fig. 8 and Table VI. The utilization of higher modulation indexes reduces all of the harmonic components and, therefore, reduces the effect of these induced harmonics. It is important to note that the filtered output voltage and current waveforms of the MB control approaches are like that of the SB approach for all presented schemes.

F. HARMONIC ANALYSIS
To evaluate the harmonic contents of the qZS-NSI outputs, Table VIII lists the unfiltered output voltage total harmonic distortion (THD) values that are determined for the proposed schemes versus the modulation index. To further strengthen the comparative finding, the table also shows the THD values for the standard NSI with the DM techniques documented in [11] and [12] and implemented here using a sawtooth carrier. Quite expectedly, the MB schemes of the qZS-NSI produce slightly higher THD values compared with the standard NSI and the proposed SB schemes under all the tested conditions. This is owed to the dc-voltage fluctuations at the B9 terminals discussed in the previous subsection. However, the SB and conventional DM schemes produce the same THD for the same operating region.

VII. EXPERIMENTAL RESULTS
An experimental qZS-NSI prototype shown in Fig. 15 is designed and tested in the laboratory to investigate the proposed DM schemes. The low-cost DSP LAUNCHXL-F28379D kit is used to control the inverter switches using the proposed modulation strategies.

| TABLE VIII |
|---|
| THD VALUES OF THE ANALYZED PWM SCHEMES |
| Schemes | Conventional DM for NSI [11], [12] | Proposed SB schemes for qZS-NSI | Proposed MB schemes for qZS-NSI |
| Index | \( M_1 = 1.15 \) | \( M_1 = 0.75 \) | \( M_1 = 0.577 \) | \( M_1 = 0.375 \) | \( M_1 = 0.46 \) | \( M_1 = 0.375 \) | \( M_1 = 0.537 \) | \( M_1 = 0.317 \) |
| Value | 0.52 | 0.979 | N.A. | N.A. | 1.244 | 1.709 | 1.244 | 1.709 | 1.261 | 1.731 | 1.482 | 2.32 | 1.482 | 2.32 | 1.513 | 2.494 | 1.709 | 1.909 | 1.709 | 1.907 | 1.729 | 1.927 |

\( \text{1 and 2 refer to the upper and lower inverter units, respectively.} \)

![FIGURE 15. Experimental qZS-NSI prototype.](image)

A series-connected inductive load of 10Ω and 5mH was connected to each of the inverter terminals. Each three-phase group of the load has its neutral point. The qZS-NSI operation was tested for all the presented 3LST and 1L-ST DM schemes, and the results are shown in Fig. 16-18. In the experimental test, the input dc-supply voltage is set at 50V, and the selected output voltage frequencies are adjusted to 50Hz and 25Hz, respectively, while the modulation indices for both units are set at 0.4. A 2.5kHz sawtooth carrier is selected. The experimental parameters are listed in Table IX. As can be observed from Fig. 16 and 17, the MB approach gives a larger dc-voltage than the SB approach. Moreover, the 1L-ST/DM4 scheme gives lower ripples in the current and voltage waveforms in the dc-side than the other schemes in both SB and MB control approaches. On the other hand, all the presented schemes give sinusoidal output currents, and therefore, the results for the 3L-ST/DM with the SB control approach only is introduced in Fig. 18. Moreover, the voltage waveforms for two output phases from each inverter unit are shown in Fig. 19.

Finally, it can be mentioned that the presented theory, concepts, and analysis of the proposed DM schemes of the qZS-NSI and introduced in the analytical sections of this paper are confirmed using the simulation results given in section VI and the experimental work in this section.
VIII. DISCUSSION

This section discusses the performance of the qZS-NSI with the proposed DM schemes. Based on the analysis parts and results sections of this paper, it is clear to say that

- The qZS-NSI can perform bucking, boosting, and inversion processes and increase the system reliability due to the utilization of ST states, and it can be used to replace the two-stage NSI with a front-end boost converter for applications where the required voltage gain is up to 2.
- As is pointed out here, although many types of PWM schemes are introduced for the NSI, the DM technique reduces the number of commutations, which is translated to lower switching losses. Moreover, using the proposed DM schemes, the effective switching frequency of upper and lower switches of the NSI bridge is reduced by $1/3\times f_s$ than the conventional solution.
- Due to the utilization of sawtooth carrier wave in the implementation of the proposed 1L-ST DM schemes, the effective switching frequency of the middle switches are reduced to $f_s$ and therefore, it can be predicted that the switching loss of these schemes will be reduced.
- In practice, the SB control methods required lower passive component values than the MB methods and give better performance in terms of voltage output THD values.
Moreover, unique carrier-based modulators are suggested for the proposed PWM schemes. Furthermore, a comprehensive study of the presented schemes has been performed. Simulations and experimental work were successfully used to validate the theoretical analysis.

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