Parametric non-interference in timed automata

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Abstract—We consider a notion of non-interference for timed automata (TAs) that allows to quantify the frequency of an attack; that is, we infer values of the minimal time between two consecutive actions of the attacker, so that (s)he disturbs the set of reachable locations. We also synthesize valuations for the timing constants of the TA (seen as parameters) guaranteeing non-interference. We show that this can reduce to reachability synthesis in parametric timed automata. We apply our method to a model of the Fischer mutual exclusion protocol and obtain preliminary results.

Index Terms—security, non-interference, parametric timed automata

I. INTRODUCTION

Timed automata (TAs) [AD94] are a powerful formalism using which one can reason about complex systems involving time and concurrency. Among various security aspects, non-interference addresses the problem of deciding whether an intruder (or attacker) can disturb some aspects of the system.

In [BT03], a decidable notion of non-interference is proposed to detect whether an intruder with a given frequency of the actions (s)he can perform is able or not to disturb the set of discrete reachable behaviors (locations); that is, this notion can quantify the frequency of an attack. In this paper, we extend that definition in two different ways: first, by allowing some free parameters within the model—that becomes a parametric timed automaton (PTA) [AHV93]. Second, by synthesizing the admissible frequency for which the system remains secure, i.e., for which the actions of the intruder cannot modify the set of reachable locations.

a) Contribution: In this work, we propose a parametric notion of non-interference in timed automata that allows to quantify the speed of the attacker necessary to disturb the model. Our contribution is threefold: 1) we define a notion of n-location-non-interference for timed automata; 2) we show that checking this notion can reduce to reachability synthesis in PTAs; 3) we model a benchmark from the literature, spot and correct an error in the original model, and we automatically infer using IMITATOR [And+12] parameter valuations for which the system is n-location-non-interfering.

b) Related work: It is well-known (see e.g., [Koc96; Ben+15]) that time is a potential attack vector against secure systems. That is, it is possible that a non-interferent (secure) system can become interferent (insecure) when timing constraints are added [GMR07]. In [Bar+02; BT03], a first notion of timed non-interference is proposed, based on traces and locations. The latter is decidable as it reduces to the reachability problem for TAs [AD94]. In [GMR07], Gardey et al. define timed strong non-deterministic non-interference (SNNI) based on timed language equivalence between the automaton with hidden low-level actions and the automaton with removed low-level actions.

In [Cas09], the problem of checking opacity for timed automata is considered: it is undecidable whether a system is opaque, i.e., whether an attacker can deduce whether some set of actions was performed, by only observing a given set of observable actions (with their timing). In [AS19], we proposed an alternative (and decidable) notion of opacity for timed automata, in which the intruder can only observe the execution time of the system. We also extend this notion to PTAs, and propose a procedure to automatically synthesize internal timings and admissible execution times for which the system remains opaque.

In [VNN18], Vasilikos et al. define the security of timed automata in term of information flow using a bisimulation relation and develop an algorithm for deriving a sound constraint for satisfying the information flow property locally based on relevant transitions.

In [Ben+15], Benattar et al. study the control synthesis problem of timed automata for SNNI. That is, given a timed automaton, they propose a method to automatically generate a (largest) sub-systems such that it is non-interferent if possible. Different from the above-mentioned work, our work considers parametric timed automata, i.e., timed systems with unknown design parameters, and focuses on synthesizing parameter valuations which guarantee non-interference. In [NNV17], the authors propose a type system dealing with non-determinism and (continuous) real-time, the adequacy of which is ensured using non-interference. We share the common formalism of TA; however, we mainly focus on non-interference seen as the set of reachable locations, and we synthesize internal parts of the system (clock guards), in contrast to [NNV17] where the system is fixed.

c) Outline: In Section II, we recall the necessary preliminaries, including non-interference for TAs. In Section III,
II. PRELIMINARIES

We assume a set $X = \{x_1, \ldots, x_H\}$ of clocks, i.e., real-valued variables that evolve at the same rate. A clock valuation is $\mu : X \to \mathbb{R}_{\geq 0}$. We write $\emptyset$ for the clock valuation assigning 0 to all clocks. Given $d \in \mathbb{R}_{\geq 0}$, $\mu + d$ is s.t. $(\mu + d)(x) = \mu(x) + d$, for all $x \in X$. Given $R \subseteq X$, we define the reset of a valuation $\mu$, denoted by $[\mu]_R$, as follows: $[\mu]_R(x) = 0$ if $x \in R$, and $[\mu]_R(x) = \mu(x)$ otherwise.

We assume a set $P = \{p_1, \ldots, p_M\}$ of parameters. A parameter valuation $v$ is $v : P \to \mathbb{Q}_+$. We assume $\mathbb{Q}_+ \in \{0, \ldots, 1, \ldots, 2, \ldots, \}$.

A. Parametric timed automata

Definition 1 (PTA). A PTA $A$ is a tuple $A = (\Sigma, L, \ell_0, X, P, I, E)$, where: i) $\Sigma$ is a finite set of actions, ii) $L$ is a finite set of locations, iii) $\ell_0 \in L$ is the initial location, iv) $X$ is a finite set of clocks, v) $P$ is a finite set of parameters, vi) $I$ is the invariant, assigning to every $\ell \in L$ a guard $I(\ell)$, vii) $E$ is a finite set of edges $e = (\ell, g, a, R, \ell')$ where $\ell, \ell' \in L$ are the source and target locations, $a \in \Sigma$, $R \subseteq X$ is a set of clocks to be reset, and $g$ is a guard.

Example 1. Consider the PTA in Fig. 1, containing two clocks $x$ and $y$, and one parameter $p$, $\ell_0$ is the initial location. Observe that the transition to $\ell_2$ can only be taken if the difference between $y$ and $x$ is larger than 2. This can only happen for selected valuations of the parameter $p$.

Given $v$, we denote by $v(A)$ the non-parametric structure where all occurrences of a parameter $p_i$ have been replaced by $v(p_i)$. We denote as a timed automaton any structure $v(A)$.

The synchronous product (using strong broadcast, i.e., synchronization on a given set of actions) of several PTAs gives a PTA.

Definition 2 (synchronized product of PTAs). Let $N \in \mathbb{N}$. Given a set of PTAs $A_i = (\Sigma_i, L_i, (\ell_0)_i, X_i, P, I_i, E_i)$, $1 \leq i \leq N$, and a set of actions $\Sigma_s$, the synchronized product of $A_i$, $1 \leq i \leq N$, denoted by $A_1 \parallel \ldots \parallel A_N$, is the tuple $(\Sigma, L, \ell_0, X, P, I, E)$, where:

1) $\Sigma = \bigcup_{i=1}^{N} \Sigma_i$.
2) $L = \prod_{i=1}^{N} L_i$, $\ell_0 = ((\ell_0)_1, \ldots, (\ell_0)_N)$.
3) $X = \bigcup_{i=1}^{N} X_i$, $P = \bigcup_{i=1}^{N} P_i$.
4) $I_i((\ell_1), \ldots, (\ell_N)) = \bigcup_{i=1}^{N} I_i((\ell_i))$ for all $(\ell_1, \ldots, \ell_N) \in L$, and $E$ is defined as follows. For all $a \in \Sigma$, let $\zeta_a$ be the subset of indices $i \in 1, \ldots, N$ such that $a \in \Sigma_i$.
5) $A_1 \parallel \ldots \parallel A_N$.

That is, synchronization is only performed on $\Sigma_s$, and other actions are interleaved. When $\Sigma_s$ is not specified, it is assumed to be equal to the intersection of the sets of actions. That is, given $A_1 \parallel A_2 \parallel A_3$, then $A_1 \parallel A_2$.

Definition 3 (Semantics of a TA). Given a PTA $A = (\Sigma, L, \ell_0, X, P, I, E)$, and a parameter valuation $v$, the semantics of $v(A)$ is given by the timed transition system (TTS) $(S, s_0, \to)$, with:

- $S = \{(\ell, \mu) \mid \ell \in L \times \mathbb{R}_0^H \mid \mu \models v(I(\ell))\}$, $s_0 = (\ell_0, \emptyset)$.
- $\to$ consists of the discrete and (continuous) delay transition relations: i) discrete transitions: $(\ell, \mu) \rightarrow (\ell', \mu')$, if $(\ell, \mu), (\ell', \mu') \in S$, and there exists $e = (\ell, g, a, R, \ell') \in E$, such that $\mu' = [\mu]_R$, and $\mu \models v(g)$. ii) delay transitions: $(\ell, \mu) \rightarrow (\ell, \mu + d)$, with $d \in \mathbb{R}_0^H$.

We write $(\ell, \mu) \xrightarrow{e,d} (\ell', \mu')$ for a combination of a delay and discrete transition if $\exists \mu'' : (\ell, \mu) \xrightarrow{\mu''} (\ell, \mu'') \xrightarrow{d} (\ell', \mu')$.

Given a TA $v(A)$ with concrete semantics $(S, s_0, \to)$, we refer to the states of $S$ as the concrete states of $v(A)$. A run of $v(A)$ is an alternating sequence of concrete states of $v(A)$ and pairs of edges and delays starting from the initial state $s_0$ of the form $s_0, (e_0, d_0), s_1, \ldots$ with $i = 0, 1, \ldots, e_i \in E$, $d_i \in \mathbb{R}_0^H$, and $s_{i+1}$. Given $s = (\ell, \mu)$, we say that $s$ is reachable in $v(A)$ if $s$ appears in a run of $v(A)$. By extension, we say that $\ell$ is reachable; and by extension again, given a set $T$ of locations, we say that $T$ is reachable if there exists $\ell \in T$ such that $\ell$ is reachable in $v(A)$. We denote by $\text{Loc}(v(A))$ the set of all locations reachable in $v(A)$.

Example 2. Consider again the PTA $A$ in Fig. 1. Let $v_1$ be such that $v_1(p) = 1$. Then, $\ell_2$ is unreachable in $v_1(A)$; at $x = 1$, one can take a first time the self-loop over $\ell_0$, yielding $y = 1$ and $x = 0$. The guard $y > 2$ to $\ell_2$ is not yet satisfied.
Then at $x = 1$, one can take a second time the self-loop over $\ell_0$, yielding $y = 2$ and $x = 0$. The guard $y > 2$ to $\ell_2$ is still not satisfied. At $x = 1$, the guard $y < 3$ is not satisfied anymore, and the self-loop over $\ell_0$ cannot be taken anymore. Therefore, $\text{Loc}(v_1(A)) = \{\ell_0, \ell_1\}$.

Let $v_2$ be such that $v_2(p) = 0.9$. This time, $\ell_2$ is reachable, by taking three times the self-loop over $\ell_0$ when $y = 0.9$, $y = 1.8$ and $y = 2.7$ respectively. Therefore, $\text{Loc}(v_2(A)) = \{\ell_0, \ell_1, \ell_2\}$.

**B. Reachability synthesis**

We will use reachability synthesis to solve the problem in Section III. This procedure, called $\text{EFSynth}$, takes as input a PTA $A$ and a set of target locations $T$, and attempts to synthesize all parameter valuations $v$ for which $T$ is reachable in $v(A)$. $\text{EFSynth}(A, T)$ was formalized in e.g., [JLR15] and is a procedure that may not terminate, but that computes an exact result (sound and complete) if it terminates. $\text{EFSynth}$ traverses the parametric zone graph of $A$, which is a potentially infinite extension of the well-known zone graph of TAs (see, e.g., [And09; JLR15]).

**Example 3.** Consider again the PTA $A$ in Fig. 1. Let us compute the set of parameter valuations for which $\ell_2$ is reachable. $\text{EFSynth}(A, \{\ell_2\}) = \{p \mid p = 0 \lor p = 1 \lor p \in [1.5, 2] \lor p \geq 3\}$. Intuitively, whenever $p \in (0, 1)$, one can take multiple times the self-loop over $\ell_0$ so that eventually the guard $y > 2$ is satisfied; whenever $p \in (1, 1.5)$, one can take exactly twice the self-loop over $\ell_0$ so that the guard to $\ell_2$ is satisfied; whenever $p \in (2, 3)$, one takes a single time the self-loop over $\ell_0$, and then the guard to $\ell_2$ becomes satisfied. For other valuations, there is no way to reach $\ell_2$.

**Remark 1.** $\text{EFSynth}$ can also be used to compute unreachability (or safety) synthesis, by taking the negation (i.e., the complement of the valuations set) of the result.

**Example 4.** Consider again the PTA $A$ in Fig. 1. Let us compute the set of parameter valuations for which $\ell_2$ is unreachable. $\neg \text{EFSynth}(A, \{\ell_2\}) = \{p \mid p = 0 \lor p = 1 \lor p \in [1.5, 2] \lor p \geq 3\}$.

**C. Non-interference**

Often, non-interference is defined using a set of low-level actions and a set of high-level ones. The idea is that an intruder is allowed to perform some high-level actions. The non-interference property is satisfied whenever the system behavior in absence of high level actions is equivalent to its behavior, observed on low level actions, when high level actions occur [BT03].

In the following, we assume a set of low-level actions $L$ and a set of high-level actions $H$.

**Definition 4** (restriction). Let $A = (\Sigma, L, \ell_0, X, P, I, E)$ be a PTA with $\Sigma = L \uplus H$ ($\uplus$ denotes disjoint union), and $v$ be a parameter valuation. The restriction of $v(A)$ to low-level actions, denoted by $v(A)|_L$, is defined as the automaton identical to $v(A)$ except that any edge of the form $(\ell, g, a, R, \ell')$ with $a \in H$ is discarded.

**Definition 5** (hiding). Let $A = (\Sigma, L, \ell_0, X, P, I, E)$ be a PTA with $\Sigma = L \uplus H$, and $v$ be a parameter valuation. The hiding of high-level actions in $v(A)$, denoted by $v(A)|_H$, is defined as the automaton identical to $v(A)$ except that any edge of the form $(\ell, g, a, R, \ell')$ with $a \in H$ is replaced with an edge $(\ell, g, c, R, \ell')$.

$\epsilon$ is the special silent action.

In [BT03], $n$-non-interference is defined as a concept ensuring that the low level behavior is unaffected by attacks which are separated by more than $n$ time units. An attack is a high-level action decided by the attacker. This concept helps to quantify the necessary attacking speed of the attacker.

Let us now recall from [BT03] the following definition:

**Definition 6** ($n$-location-non-interference). Let $A = (\Sigma, L, \ell_0, X, P, I, E)$ be a PTA with $\Sigma = L \uplus H$, and $v$ be a parameter valuation. Let $n \in \mathbb{Q}_+$, $v(A)$ is $n$-location-non-interfering if $\text{Loc}(v(A)|_L) = \text{Loc}(v(A)|_H)$ project onto the locations of $v(A)$.

By “projected on $v(A)$”, we mean the set $\{\ell \mid \exists \ell' : (\ell, \ell') \in \text{Loc}(v(A)|_H)\}$.

**Example 5.** Consider again the PTA $A$ in Fig. 1. Assume $L = \{l\}$ and $H = \{h\}$. That is, the intruder can take the self-loop over $\ell_0$. Let $v_3$ be such that $v_3(p) = 1.1$. First, note that $\text{Loc}(v_3(A)|_L) = \{\ell_0, \ell_1\}$ since the transition to $\ell_2$ is syntactically removed, preventing $x$ to be reset.

Fix $n = 1$. The product of $v_3(A)$ with $\text{Interf}_H^n$ prevents the system to synchronize faster than every 1 time unit on $h$: 1The hiding of $H$ is not strictly speaking necessary in our setting since we are interested in the reachability of locations but we keep it for sake of consistency with [BT03].
therefore, taking the self-loop labeled with $h$ when $y = 1.1$ and $y = 2.2$ respectively is possible, enabling the transition to $\ell_2$ at $y = 2.2$. This gives that $\text{Loc}(v(A) \parallel \text{Interf}_H^{n})_{H}$ projected onto the locations of $v_3(A)$ is $\{\ell_0, \ell_1, \ell_2\}$. Therefore, $v_3(A)$ is not 1-location-non-interfering.

Now fix $n = 2$. In that case, the self-loop can be taken when $y = 1.1$, but not when $y = 2.2$ because the condition $x_{\text{interf}} \geq 2$ is not satisfied (recall that $x_{\text{interf}}$ is reset in $\text{Interf}_H^{n}$ on the first transition labeled with $h$, and therefore we have $x_{\text{interf}} = 1.1$ when $y = 2.2$). So $\ell_2$ is unreachable. Therefore, $v_3(A)$ is 2-location-non-interfering.

### III. Parametric Location-Non-Interference

In this work, we aim at considering a broader problem: instead of asking whether the intruder with a predefined power can disturb the system, we ask what is the power the intruder needs to perform a successful attack? More precisely, we aim at computing the speed of the intruder needed to successfully disturb the system: that is, for what valuations of $n$ is the system (not) $n$-location-non-interfering?

In addition, our PTA model can contain free parameters too; so the parameter is not only $n$ but also the PTA parameters.

**n-location-non-interference synthesis problem:**

**INPUT:** A PTA $A$ with parameters $P$, a parameter $n$

**PROBLEM:** Synthesize valuations $v$ of $P$ and of $n$ such that $v(A)$ is $n$-location-non-interfering.

Since our problem is location-based, we can solve it using reachability synthesis techniques for PTAs, more precisely using EFsynth. The core idea is to synthesize valuations of $P \cup \{n\}$ such that the set of reachable locations remains identical in both $v(A)$ and $(v(A) \parallel \text{Interf}_H^{n})_{H}$. This therefore reduces to a reachability synthesis problem.

Note that, since reachability-emptiness (i.e., the emptiness of the valuations set for which a given (set of) location(s) is reachable) is undecidable for PTAs [AHV93; And99], reachability synthesis algorithms are not guaranteed to terminate. (We discuss approximations later on.)

**Example 6.** Consider again the PTA $A$ in Fig. 1. Assume $L = \{l\}$ and $H = \{b\}$. First observe that $\ell_1$ (and of course $\ell_0$) can be reached in $v(A)$ regardless of the value of $p$. Second, for all $v$, $\ell_2$ is unreachable in $v(A)_{L}$ since the self-loop on $\ell_0$ is syntactically removed. Therefore, for all $v$, $\text{Loc}(v(A)_{L}) = \{\ell_0, \ell_1\}$.

As a consequence, $n$-location-non-interference synthesis for $A$ reduces to reachability synthesis of valuations of $n$ and $p$ for which $\ell_2$ is unreachable.

The result of $\neg\text{EFsynth}(A \parallel \text{Interf}_H^{n})_{H}, \{\ell_2\}$ is:

- $(0 < p < 1 \land n > p)$
- $(p = 1 \land n \geq 0)$
- $(1 < p < 1.5 \land n > p)$
- $(1.5 \leq p \leq 2 \land n \geq 0)$
- $(p \geq 3 \land n \geq 0)$

This result can be intuitively explained as follows: whenever $p < 1$ (first disjunct), if the intruder can act strictly slower than every $p$ time unit ($n > p$), only one self-loop on $\ell_0$ can be taken, and $\ell_2$ is unreachable, and therefore the system is $n$-location-non-interfering. Whenever $p = 1$ (second disjunct) or $1.5 \leq p \leq 2$ (4th disjunct) or $p \geq 3$ (last disjunct), we saw in Example 3 that $\ell_2$ is unreachable, regardless of the value of $n$. Finally, whenever $1 < p < 1.5$ (3rd disjunct), $\ell_2$ is reachable iff the intruder can act strictly slower than every $p$ time units.

### IV. Application to the Fischer Protocol

**A. The Fischer mutual exclusion protocol**

The protocol proposed by Michael Fischer ensures that two processes never use a critical resource (often denoted by critical section) at the same time. The protocol is based on the speed of the processes.

We consider here the protocol as studied in [BT03]: suppose that two processes $P_1$ and $P_2$ running in parallel compete for the critical section. Assume that atomic reads and writes are permitted to a shared variable $v$ (called $\times$ in [BT03]). Assume also that every access to the shared memory containing $v$ takes $\text{acc}$ units of time. Each process $i$ executes the following code:

```
repeat
  await v = 0
  v := i
  delay b
until v = i
v := 0
```

(Critical section)

The idea is that process $P_i$ is allowed into the critical section only when $v = i$; “await $v=0$” waits until $v$ becomes 0; “delay b” waits exactly $b$ time units, which is ensured by the process local clock. An assignment takes (at most) $a$ time units. The modified model of [BT03] also considers that the maximum time needed to execute the critical section after $v$ is checked is $\text{acc}$.

In [BT03], the protocol is modeled using a network $A$ of TAs made of $i$-process $P_i$, for $i = 1, 2, i)$ an intruder, that can take an $\text{att}$ transition anytime, nondeterministically changing $v$ to 0, 1 or 2, and $ii)$ a “serializer” responsible to model the value of $v$ according to the access and modification requests of $P_1$ and $P_2$; recall that these operations take $\text{acc}$ time units.

The idea is as follows: if the intruder is fast enough, (s)he can successfully disturb the system, i.e., send both processes into the critical section at the same time, thus violating the mutual exclusion. On the contrary, if the intruder is slow, its nondeterministic modifications of $v$ will have no effect on the security.

The crux of [BT03] is that the model is $n$-location-non-interfering iff the previously defined TA $A$ cannot reach a location where both processes are in the critical section at the same time. A sufficient condition over $n$ and $b$ to ensure $n$-location-non-interference is manually inferred and proved.

Our goal is to automatically infer conditions over $n$, $a$, $b$, $\text{acc}$ and $\text{ues}$ guaranteeing $n$-location-non-interference.
B. A modified Fischer model

1) An issue in the existing modeling: While modeling the TA model of [BT03] using a model checker, we spotted a modeling issue, that makes the model wrong. The issue lies in the serializer: the idea of the serializer is to ensure that two consecutive access or modification requests to $v$ are separated by at least $acc$ time units; but, due to the absence of invariants and of “as soon as possible” concept in the TAs of [BT03], there exist runs of the TA such that the access to $v$ can last forever, even if no other process is competing. Although this cannot happen in reality, the model checker always reports that forever, even if no other process is competing. Although this mistake does not impact the definitions nor the overall reasoning of the benchmark application of [BT03], as the authors use a manual reasoning to infer the condition over $n$ and $b$.

Note that this mistake does not impact the definitions nor the overall reasoning of the benchmark application of [BT03], as the authors use a manual reasoning to infer the condition over $n$ and $b$.

2) Our new model: The purpose of the serializer is both to encode the value of $v$, and to maintain a “queue” of requests to read or write accesses to the memory, ensuring that any two consecutive access is separated by $acc$ time units. We therefore entirely rewrote the serializer, also impacting the model of the processes.

a) Processes: We first give the modified model of process $P_i$ in Fig. 3. Process $P_i$ features a local clock $x_i$ and can read or write $v$. The main modification w.r.t. to [BT03, Fig. 6] is the duplication of all locations: indeed, instead of performing a single action (e.g., $try_i$) reading or writing $v$, the process first performs a request $req_i$, then followed by the action $try_i$; the serializer is responsible for answering the request as soon as possible, but not earlier than $acc$ since the latest read or write action. Then, the PTA follows the program given in Section IV-A: $P_i$ first waits until $v = 0$, then updates it to $i$; then, it waits exactly $b$ time units, and checks whether $v$ is still $i$; if not, it moves back to the original location. If $v = i$, the process sets $v$ to $0$, enters the critical section and, after at most $acs$ time units, leaves it to go back to the idle location.

b) Intruder: The intruder is almost identical to the one in [BT03]: it is a one-location PTA with three self-loops synchronizing on $att$ and setting $v$ to 0, 1 or 2 respectively (given in Fig. 4). Setting $H = \{att\}$, the synchronization of the intruder with $Intef^H$ ensures that the intruder may modify $v$ with at least $n$ time units since its last modification.

c) Serializer: The serializer automaton is both very simple and quite complex. Its overall goal is very simple, and is to perform the following behavior: “whenever a process ($P_1$, $P_2$ or the intruder) requests a write or read access to the memory, the serializer shall grant it as soon as possible, and $acc$ time units later than the previous access—unless another process is also requesting access, in which case the request should be queued”. Implementing this in a purely automata-based formalism is however cumbersome, much more than the simplistic serializer of [BT03], that does not encompass for the “as soon as possible” concept. This results in a PTA made of 12 locations and 91 transitions.

V. Experiments

We model the aforementioned automata using the IMITATOR [And+12] parametric timed model checker (version 2.12 “Butter Lobster”). We then run safety synthesis (i.e., the negation of $EFSynth$, implemented in IMITATOR) so as to synthesize parameter valuations for which mutual exclusion is guaranteed, i.e., both processes cannot be in the CS location at the same time.

A. An approximated result

Running IMITATOR on the model, the analysis does not terminate; this is not surprising as $EFSynth$ is not guaranteed to terminate due to the undecidability of the reachability-emptiness for PTAs [AHV93]. A closer look at the analysis let us realize that, after passing the depth of 24 (IMITATOR explores the zone graph in a breadth-first search manner), no new constraint is synthesized, until at least a depth of 1000 (after which we interrupted the analysis, after about 20 hours of processing). The resulting constraint (that does not change after depth 24, reached in about 650 s) is made of 22 disjunctions of convex constraints over the system parameters.

A property of $EFSynth$ is that it returns an under-approximation of the constraint when interrupted; when its negation (safety synthesis) is run, an over-approximation is returned. That is to say, the obtained result contains all possible valuations for which non-interference is satisfied, but the result may also potentially contain valuations for which the system is not non-interfering. We therefore tested valuations from our constraint using the non-parametric timed model checker UPPAAL [LPY97]. We randomly picked up several dozens of parameter valuations, and checked using UPPAAL.

2 All models and results are available at www.imitator.fr/static/ICECCS20.
that non-interference is satisfied iff the valuation belongs to the resulting constraint. The UPPAAL model is identical to the IMITATOR model, but is non-parametric, and therefore the analysis is guaranteed to terminate (depending on the parameter valuations, termination is obtained within a few seconds). This does not formally prove that our result is exact (sound and complete), but increases the degree of confidence. Proving the exactness of our constraint (or developing a new synthesis algorithm able to detect that the constraint is exact and to terminate the analysis) is among our future work.

B. Interpretation

The 22 disjunctions of convex constraints give a set of conditions for which the system is non-interfering, that is the mutual exclusion is guaranteed and an attacker able to disturb the system at most every \( n \) time units cannot succeed in violating mutual exclusion by its actions.

For sake of exemplification, let us consider the first disjunct (the full constraint is available online):

\[
\begin{align*}
n &\geq 0 \\
 b &\geq acc + n \\
 b &\geq 3 \times acc \\
a &> 0 \\
 acc &> ucs > 0
\end{align*}
\]

Recall that \( b \) is the waiting time before testing again the value of \( v \), \( n \) is the minimum time between any two consecutive high-level actions (of the intruder), \( acc \) is the memory access time, and \( ucs \) is an upper bound on the time during which a process remains in the critical section. This constraint ensures that mutual exclusion is guaranteed even when an attacker can change the value of \( v \) no faster than every \( n \) time units if the following conditions are satisfied:

- the delay (\( b \)) is longer than the access time (\( acc \)) and the minimum disturbance time (\( n \)); that is to say, even when the intruder modifies the system, the process can still detect it as its delay is long enough; this helps guaranteeing non-interference;
- the delay is longer than three access times (\( 3 \times acc \)); that is to say, the delay is long enough to detect whether the other process performs \( try, update, \) and \( pre_access \), during the delay; this helps guaranteeing validity of the mutual exclusion;
- the memory access time is longer than the time during which a process remains in the critical section.

Further sufficient conditions ensuring non-interference are guaranteed by the other disjuncts (see Web page).

VI. Conclusion

a) Conclusion: We introduced a definition of \( n \)-location-non-interference, that aims at quantifying the necessary attacker frequency to be able to modify the set of reachable locations in a timed automaton. Using the IMITATOR parametric timed model checker, we obtained preliminary results on an improved version of the Fischer mutual exclusion protocol.

b) Future works: As we only obtained an over-approximation of the result, our first future work is to prove the exactness (soundness and completeness) of the obtained constraint, either by proving it using an ad-hoc reasoning for our case study, or by developing new automated techniques allowing IMITATOR to terminate as soon as the constraint is indeed complete. Alternatively, designing approximated techniques is another interesting direction.

While the general emptiness problem (the emptiness of the set of both timing parameter valuations and admissible values of \( n \) for which the system is \( n \)-location-non-interfering) is very likely to be undecidable (due to the undecidability of reachability emptiness in [AHV93]), the more specific problem of deciding whether there exists a valuation of \( n \) for which the (non-parametric) system is \( n \)-location-non-interfering remains open. Also, we aim at tackling efficient synthesis of these sets, independently of the decidability issues. More generally, proposing new state space reduction techniques dedicated to the problem of \( n \)-location-non-interference is among our future works.

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