Design and Implementation of a Low Complexity Multiuser Detector for Hybrid CDMA Systems

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Abstract—In hybrid CDMA systems, multiuser detection (MUD) algorithms are adopted at the base station to reduce both multiple access and inter-symbol interference by exploiting space-time (ST) signal processing techniques. Linear ST-MUD algorithms solve a linear problem where the system matrix has a block-Toeplitz shape. While exact inversion techniques impose an intolerable computational load, reduced complexity algorithms may be efficiently employed even if they show sub-optimal behavior introducing performance degradation and near-far effects. The block-Fourier MUD algorithm is generally considered the most effective one. However, the block-Bareiss MUD algorithm, that has been recently reintroduced, shows also good performance and low computational complexity comparing favorably with the block-Fourier one. In this paper, both MUD algorithms will be compared, along with other well known ones, in terms of complexity, performance figures, hardware feasibility and implementation issues. Finally a short hardware description of the block-Bareiss and block-Fourier algorithms will be presented along with the FPGA (Field Programmable Gate Array) implementation of the block-Fourier using standard VHDL (VHSIC Hardware Description Language) design.

Index Terms—Low complexity multiuser detector, hybrid CDMA system, TD-SCDMA mobile radio system, CWTS, block-Bareiss algorithm, block-Fourier algorithm, FPGA implementation.

I. INTRODUCTION

In 3G hybrid CDMA systems with antenna arrays at the receivers, space-time (S-T) multiuser detection (MUD) algorithms are adopted at the base station to reduce both inter-symbol (ISI) and multiple access (MAI) interference [1]. For each data-packet or block, in the up-link scenario, linear MUD solves a linear system where the system matrix has a specific block-Toeplitz structure.

Exact MUD computation exhibits a high computational load for large matrix size (i.e. high number of users, antennas and/or symbols per block), as it involves the inversion of a large correlation matrix. Exact inversion of the system matrix is not feasible due to large matrix size and real-time constraints. In fact, in real-time mobile radio systems, computational resources are limited and only reduced complexity algorithms can be employed. Nevertheless, when computational complexity is strongly reduced, sub-optimal algorithms might introduce performance degradation and other unwanted effects (e.g. near-far problems).

Two main MUD techniques are available in literature: block-based MUD [2],[3],[4] and one-shot MUD also known as sliding windows detector (SWD) [5]. Both families may be implemented using real-time hardware [4],[6],[7],[8],[9],[10]. In practice, algorithm selection is performed taking into account various aspects such as performance, complexity and implementation issues. However, when computational power requirement and system complexity are the key constraints, some performance degradation have to be tolerated.

According to these considerations, a new MUD detector scheme based on the block-Bareiss (BB) algorithm has been reintroduced [11],[12]. This algorithm, derived from the plain Bareiss factorization technique [13], combines good performance and low computational load with simple hardware implementation. For a specific hybrid CDMA radio system (i.e. China Wireless Telecommunication Standard or CWTS for short), the BB detector is compared with the reference direct inversion methods and with other well known block algorithms namely the block-Levinson algorithm (BL) [14] and the block-Fourier Transform (BFT) algorithm [4].

Finally a floating-point implementation of the BB processor is compared with the equivalent BFT one. With respect to the above mentioned algorithms, the BB one is well suited for hardware FPGA (Field Programmable Gate Array) implementation not only for its low computational load but also for its good performance. In addition, it does not suffer from near-far effects that plague very low complexity implementation such as low order BFT detectors [15]. It is also worth noticing that the BB detector is also suitable for hardware parallel implementation. However, for perfect power control radio systems, the BFT remains the most effective MUD algorithm in terms of complexity and implementation feasibility. Finally, a FPGA implementation of the BFT algorithm is presented and commented.

The paper is organized as follows: Section II describes the signal model used in hybrid CDMA systems and underlines the peculiarities due to the specific CWTS standard adopted. Section III introduces the Bareiss algorithm and the other reduced complexity algorithms selected for comparison. Both performance and computational complexity of the mentioned MUD algorithms are evaluated and compared in Sections IV and V respectively. The proposed hardware implementation is described in Section VI while Section VII draws some conclusions.

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In hybrid synchronous CDMA systems, such as the CWTS standard [16] whose frame structure is shown in Fig. 1, $K$ users ($1 \leq K \leq 8$) are active in the same frequency band and in the same time slot being separated only by different spreading codes. Each user transmits a data burst consisting of $2N$ QPSK symbols ($N = 352/Q$, $N$ symbols of duration $T_s = QT_c$) where $Q$ is the spreading factor ($Q \in \{1, 2, 4, 8, 16\}$) and the chip rate $F_c$ is defined as $F_c = 1/T_c = 1.28$ Mcps. In the following part of this paper, $Q$ is assumed constant for all $K$ users: $Q = 16$. The semi-burst period $T_{sb}$ is defined as $T_{sb} = NQT_c = 352/F_c = 275$ ms.

The column vector $h_{k,m}$ represents the channel impulse response (CIR) for the link between the $k$th user and the $m$th antenna of the array. Each vector $h_{k,m}$ is also assumed of length $W$ ($W = 16$) when expressed in chip intervals $T_c$. Space-time matrix $H_k = [h_{k,1} \ldots h_{k,m} \ldots h_{k,M}]^T$ for the $k$th user has size $M \times W$ while the complete multi-user channel matrix $H = [H_1 \ldots H_K]$ has size $M \times WK$. Each CIR is assumed known and does not vary during the time slot.

For each semi-burst, the discrete-time base-band MIMO (Multiple Input Multiple Output) signal model is indicated by the following equation:

\[ y = Ad + n. \]  

The $M(NQ + W - 1) \times 1$ vector $y$ represents the signal received by the array of $M$ antennas ($1 \leq M \leq 8$) located at the base station while vector $d$ of size $NK \times 1$ represents the transmitted data for all $K$ users. Moreover, it is $E[dd^H] = I$.

Noise vector $n$ takes care of both electronic noise and inter-cell interference; $n$ is assumed spatially correlated and temporally uncorrelated with covariance matrix given by:

\[ R_n = E[nn^H] = R_n \otimes I_{NQ+W-1}, \]  

where $\otimes$ is the Kronecker’s product, $I_{NQ+W-1}$ is the identity matrix of size $NQ+W-1$ and $R_n$ is the spatial covariance matrix ($R_n|_{m,m} = \sigma_n^2$ for $m = 1, \ldots, M$) of size $M \times M$.

Since the CIRs are assumed constant in the data slot, the matrix $A$ of size $M(NQ + W - 1) \times NK$ containing $N$ shifted copies of blocks $B$. Fig. 2 shows that every sub-matrix $B$ of size $M(Q + W - 1) \times K$ is composed by $K$ column vectors $b_k$ ($k = 1, \ldots, K$); each of them is composed by the convolution $b_{k,m} = c_k \star h_{k,m}$ between the $k$th spreading codes $c_k$ and the CIR vector $h_{k,m}$ ordered for all $M$ antennas: $b_k = [b_{k,1} \ldots b_{k,m} \ldots b_{k,M}]^T$. The normalized term $v = [(Q + W - 1)/Q]$ is the delay spread expressed in symbol intervals.

In the following sections we will assume, without any loss of generality, a zero-forcing (ZF-MUD) detector scheme. The interested reader may refer to [1] for a detector that employs a different estimation technique (e.g. MMSE-MUD). According to Fig. 2 the received signal vector $y$ is at first filtered by the whitening S-T matched filter producing the $NK \times 1$ output vector:

\[ y_{MF} = A^H R_n^{-1} y = A^H R_n^{-1/2} R_n^{-1/2} y; \]  

then linear ZF-MUD is performed by estimating the data symbols vector $\tilde{d}$ of size $NK \times 1$ according to:

\[ \tilde{d} = R^{-1} y_{MF} = (A^H R_n^{-1/2} A)^{-1} A^H R_n^{-1/2} y, \]  

where $R^{-1}$ is the $NK \times NK$ decorrelating matrix obtained from matrix $R = A^H R_n^{-1} A$. Finally, hard decided QPSK symbols $\hat{d}$ are obtained by the threshold detector $\text{dec}(\cdot)$:

\[ \hat{d} = \text{dec}(\tilde{d}) = \text{dec}(R^{-1} y_{MF}). \]

Equation (3) may be rewritten as:

\[ y_{MF} = \tilde{A}^H y = \tilde{R} d + n_{MF} \]  

to indicate that the S-T matched filter output $y_{MF}$ may be also obtained by calculating the output vector $y = R_n^{-1/2} y$ of the first spatial whitening filter (see Fig. 1) and then applying the matched filter $\tilde{A} = R_n^{-1/2} A$; $n_{MF}$ is the noise at the output of the S-T matched filter with $E[n_{MF} n_{MF}^H] = R$.

Please note that, in the case of MMSE-MUD, equation (1) becomes now [1]:

\[ \tilde{d} = \text{dec}(\tilde{d}) = \text{dec}((R + I)^{-1} y_{MF}). \]
III. EFFICIENT DETECTOR ALGORITHMS

Most of the complexity of the linear detector algorithms employed for MUD scheme proposed in the previous section arises from the inversion methods of the large correlation matrix \( R \) and from the matched filter computation [8]. As depicted in Fig. 2, matrix \( R \) is block-Toeplitz and block-banded. It is composed by \( N \times N \) sub-matrices \( R_i \) (\( i = 0, ..., N - 1 \)) having size \( K \times K \):

\[
R = \begin{bmatrix}
R_0 & R_1 & \cdots & R_{N-1}
R_1 & R_0 & \cdots & \vdots
\vdots & \vdots & \ddots & \vdots
R_{N-1} & \cdots & \cdots & R_0
\end{bmatrix},
\]

(8)

where \( R_{i+1} = R_i^H \) (\( i = 1, ..., N - 1 \)). Moreover, matrix \( R \) has only 2\( v \) - 1 non null block-diagonals: \( R_{i+1} = R_i^H = 0 \), for \( i = v, v + 1, ..., N - 1 \).

As far as the matched filter output \( y_{MF} \) is concerned, its computational cost dominates using an antenna array (\( M >> 1 \)); however its calculation has a high degree of parallelism that can be easily exploited during the hardware implementation (e.g. using a polyphase Q-decimated filter bank) [8].

Some MUD algorithms compute directly the decorrelating matrix \( R^{-1} \) and then calculate the solution \( \hat{y} \) by matrix multiplication. On the contrary, other algorithms factorize matrix \( R \) and then solve the equation:

\[
R \hat{d} = y_{MF}.
\]

(9)

While the block-Levinson algorithm [14] belongs to the first class of techniques, the latter family includes the well known block-Fourier (BFT) [17] algorithm and all methods derived from the QR decomposition [18] of the matrix \( R \). To this second family belongs also the block-Bareiss algorithm that will be discussed later on.

All the methods that belong to the second family are similar to the plain Cholesky algorithm and differ only in the used factorization algorithm that takes care of the block-Toeplitz matrix \( R \) having in common the remaining processing steps. For instance, the Cholesky algorithm computes the Cholesky factor \( U \) of the matrix \( R \): \( R = U^H U \). Then, both the lower triangular system:

\[
U^H z = y_{MF}
\]

(10)

and the upper triangular one:

\[
U \hat{d} = z,
\]

(11)

are computed sequentially by using the backward and forward (B/F) algorithm, respectively. The Cholesky factor \( U \) of a block-Toeplitz matrix \( R \) is block-banded but not block-Toeplitz. However, the Cholesky factor structure shown in [19] may be exploited to approximate the factorization and to speed-up the computation if \( N >> v \). This approximation may be used together with the well known generalized Schur algorithm [17] to speed up the whole computation. It is worth mentioning that the B/F algorithm has a complexity in the order of \( O[N^2 K^2] \).

A. Factorization algorithms

The exact computation of the Cholesky factor \( U \) for an arbitrary \( NK \times NK \) matrix \( R \) requires a number of operations in the order of \( O[N^3 K^3] \) that is prohibitive for a large number of symbols \( N \) and/or users \( K \). For this reason, several fast inversion or factorization algorithms have been developed.

B. Block-Fourier algorithm

The BFT algorithm [4] is derived from the plain Fourier algorithm briefly recalled here. The Fourier technique solves the generic problem:

\[
R \hat{x} = y,
\]

(12)

where \( \forall h, k = 0, ..., n - 1 \) it is \( [R]_{h,k} = r_{h,k} \) depends only on the difference \( k - h \) and \( r_{h,h} = r_0 \). The solution is computed by transforming equation (12) into the frequency domain by exploiting the \( n \)th order DFT matrix operator \( F \) defined as:

\[
[F]_{h,k} = \exp\{-j2\pi(h - 1)(k - 1)/n\},
\]

(13)

where \( n \) is the problem size and \( h, k = 1, ..., n \). If the matrix \( R \) is circulant, then it is well known [18] that \( R \) may be factorized as:

\[
R = F^{-1} A F,
\]

(14)

where the matrix \( A \) is the diagonal matrix containing the eigenvalues of \( R \). It may be noticed that if \( A \) is circulant then \( R \) is circulant, too.

The convolution problem (12) becomes now:

\[
F R \hat{x} = A F x = F y,
\]

(15)

while the solution vector \( x \) is obtained by inverse DFT transformation \( F^{-1} \):

\[
x = F^{-1} A^{-1} F y.
\]

(16)

The Fourier method is computationally effective because the diagonal matrix \( A \) that contains the eigenvalues of \( R \), can be efficiently computed by transforming only the first column \( r_1 \) of the matrix \( R \) according to:

\[
\lambda = \text{Fr}_1,
\]

(17)

where column vector \( \lambda \) is obtained from eigenvalue matrix \( \Lambda \) by rearranging its diagonal elements by means of the diag operator:

\[
\lambda = \text{diag}(\Lambda) = \Lambda 1_n
\]

(18)

and \( 1_n \) is the column vector of length \( n \) having all terms equal to one.
Unfortunately, the matrix \( R \) is not circulant, it is also block-Toeplitz and block-band but it has only \( 2v - 1 \) non null block-diagonals (Fig. 2). It may be easily made circulant with few modifications: the circulant block matrix \( \tilde{A}_c \) is obtained from \( A \) just adding and arranging columns of blocks as shown in Fig. 4. The number of added blocks depend on the value \( v \): in our case, the matrix \( \tilde{A}_c \) has size \( DP \times DK \) where \( D = N + v - 1 \) and \( P = MQ \) while circulant matrix \( R_c = \tilde{A}_c^H \tilde{A}_c \), derived from \( A_c \), has size \( DK \times DK \).

Now, the plain Fourier algorithm must be modified to handle the block-circulant matrix \( R_c \) containing \( D^2 \) blocks of size \( K \times K \). In Fig. 4 it is defined the block-Fourier matrix transformation \( \tilde{F}_{DK} = \tilde{F} \otimes I_K \) where \( \otimes \) is the Kronecker’s product, \( I_K \) is the \( K \times K \) identity matrix, \( \tilde{F}_K \) and \( \tilde{F} \) represent the \( K \)th and the \( D \)th order DFT, respectively.

The equation equivalent to (14) is:

\[
R_c = F_{DK}^{-1} A_{DK} F_{DK},
\]

where \( A_{DK} \) is the block-diagonal matrix composed of \( D \) non null blocks of size \( K \times K \) along the main block-diagonal. It is computed (cf. Eq. 17):

\[
\text{diag}_{DK}(A_{DK}) = F_{DK} R_{c1}, \tag{20}
\]

where \( R_{c1} \) is the first block column of the matrix \( R_c \) and \( \text{diag}_{DK}(\cdot) \) is the extension of the \( \text{diag} \) operator (18) to the \( K \times K \) block size case.

Finally, the BFT algorithm computes the following matrix equation corresponding to (15):

\[
F_{DK} \tilde{d} = \Lambda_{DK}^{-1} F_{DK} y_{MF} \tag{21}
\]

and then applying the inverse DFT operator \( F_{DK}^{-1} \),

\[
\tilde{d} = F_{DK}^{-1} \Lambda_{DK}^{-1} F_{DK} y_{MF}. \tag{22}
\]

The block elements of block-diagonal matrix \( \Lambda_{DK} \) have no particular structure; therefore \( \Lambda_{DK}^{-1} \) may be obtained with standard (or approximated) methods such as the Cholesky factorization. In addition, the matched filter output \( y_{MF} \) is obtained from equation (6). Only the first \( NK \) values of \( \tilde{d} \) from the equation (22) are used to compute the vector \( d \).

It is possible to speed up the block-Fourier algorithm by reducing the ideal length \( D \) of the FFT (i.e. using optimized radix-4 operators) with respect to the true value \( N + v - 1 \) and by using the well-known overlap-and-save technique. It requires the use of \( L = \lceil N/(D - \text{prelap} - \text{postlap}) \rceil \) data vector slices of reduced size \( D \) to cover \( N \) symbols [4].

C. Block-Levinson algorithm

The BL algorithm is derived from the plain Levinson algorithm that computes the direct problem \( Rx = y \) by inverting the matrix \( R \) that is Hermitian, Toeplitz and positive defined. For a generic matrix \( R \) of size \( n \times n \), this technique requires a number of operations in the order of \( \mathcal{O}[n^2] \). The BL algorithm has been extended [14,10] to the block-Toeplitz matrices \( R^{(i)} \) of size \( NK \times NK \) by solving the following system at step \( i + 1 \):

\[
R^{(i+1)} \tilde{d}^{(i+1)} = y^{(i+1)}_{MF} \tag{23}
\]

starting from the solution at step \( i \). The original problem (9) is solved through \( N - 1 \) iterations. By defining matrix \( R^{(i)} \) as:

\[
R^{(i)} = \begin{bmatrix}
R_0 & R_{-1} & \cdots & R_{-i} \\
R_1 & R_0 & \cdots & \cdots \\
\vdots & \vdots & \ddots & \vdots \\
R_i & \cdots & R_1 & R_0
\end{bmatrix}, \tag{24}
\]

the system (23) may be rewritten as \((1 \leq i \leq N - 1)\):

\[
\begin{bmatrix}
R^{(i)} & E_i (G^{(i)})^T \\
(G^{(i)})^T & E_i\end{bmatrix} \begin{bmatrix}
\tilde{d}^{(i)} \\
\mu
\end{bmatrix} = \begin{bmatrix}
y^{(i)}_{MF} \\
y^{(i+1)}_{MF}
\end{bmatrix}, \tag{25}
\]

where \( \tilde{d}^{(i)} \) and \( y^{(i)}_{MF} \) are sub-vectors of length \( iK \) obtained from the vectors \( d \) and \( y_{MF} \), respectively. The vector \( y^{(i+1)}_{MF} \) that is extracted from the matched filter output \( y_{MF} \), has size \( K \times 1 \). Matrix \( G^{(i)} \) is defined as \( G^{(i)} = [R^T_i R^T_2 \ldots R^T_i] \), \( E_i \) is the exchange block matrix of size \( iK \times iK \) that inverts the order of the blocks of the previous matrix \( G^{(i)} \) and \( \mu \) is an auxiliary vector [14] of size \( K \times 1 \).

As indicated in the BFT algorithm, it is also possible to increase the algorithm processing speed by considering that, after few iterations, some internal parameters converge rapidly to their final value and may therefore considered constant. Reference [4] shows a detailed description about these optimizations.

D. Block-Bareiss algorithm

The plain Bareiss algorithm [13] employs an iterative technique, derived from the classical Schur algorithm, to solve a
Fig. 5. Structure of matrices $R^{(-i)}$ and $R^{(+i)}$ used in the Bareiss algorithm for $i = 3$. The example refers to tri-diagonal block matrix $R$ found in the CWTS standard with $v = 2$.

For the sake of completeness, the generalized Schur algorithm with the Cholesky approximation (ACD - Approximate Cholesky Decomposition) [19] can reduce the number of operations in the order of $O(n^3)$. For a complete description of this algorithm, the interested reader is referred to [17]. In addition, references [8] and [23] show a brief comparison of the ACD algorithm performance with respect to the SWD one in the TDD-UTRA and CWTS scenario, respectively.

All these MUD algorithms may have different behavior depending on one or more parameters: FFT size ($D$), overlap-and-save parameters (prelap, postlap or $L$) greatly affect BFT algorithm while iteration step ($i$) is the main parameter for BL and BB detectors. These parameters greatly affect performance, computational complexity and architectural issues. Fine tuning of these parameters depends on the adopted mobile radio scenario and will be evaluated in Section IV.

IV. SIMULATION RESULTS

Following the CWTS standard [16], the parameters employed in the system simulations are: $K = 8$, $N = 22$, $Q = 16$ and $W = 16$. The simulation scenario is characterized by 100,000 bursts of up-link traffic data only with scrambling and spreading codes, without channel coding and with perfect power control scheme. The spatio-temporal channel matrix $H$ adopted for the simulations is derived from the Typical Urban (TU) multipath propagation channel as introduced by the COST-207 group [24]. More sophisticated S-T channel models are available; however, this simpler model has been adopted for easy and direct comparison with respect to spatial only algorithms ($M = 1$).

According to the WSSUS (Wide Sense Stationary Uncorrelated Scattering) model introduced previously, for the $k$th user, channel $H_k$ consists of a single cluster of $N_p = 12$
uncorrelated paths, whose delays and mean powers are fixed and set according to the TU model. Each $p$th path angle is a random variable:

$$\theta_{k,p} = N\left(\theta_0, \sigma^2_\theta\right)$$

with mean value $\theta_0 = U\left[-\pi/3, +\pi/3\right]$ and standard deviation $\sigma_\theta = \pi/36$. Amplitude variations due to fast fading are simulated by introducing the Rayleigh distribution. In addition, to speed-up the simulations, no mobile speed is considered since the maximum speed constraint (i.e., $|v| \leq v_{\text{max}} = 120$ Kmph) introduced by the CWS standard does not cause significant channel decorrelation during the semiburst period $T_{sb}$. In fact, according to the Clarke model [25], the correlation of the CIR fading amplitudes is described by the Jakes’ autocorrelation function $\rho_0(\tau) = J_0(2\pi v_{\text{ran}}\tau/\lambda)$ where $\lambda$ is the carrier wavelength ($\lambda = 15$ cm) and $v_{\text{ran}}$ the radial mobile speed. In our case, it is $\rho_0(T_{sb})|v_{\text{ran}}=v_{\text{max}} = 0.96$ and therefore the channel may be considered constant during each time slot (see reference [26] for similar considerations about the TDD-UTRA scenario). Perfect knowledge of the channel is assumed while near-far effects are not present: $E\left[\|H_k\|^2\right]$ is constant for all $K$ users. For discussions about near-far effects of all algorithms presented here, reference [15] may be consulted. The base station receiver employs a single antenna ($M = 1$) or a linear array ($M = 8$) of equally spaced antennas at $\lambda/2$.

In Fig. 6 and 7 the performance of the approximate MUD and the exact inversion algorithms are compared in terms of BER for varying signal to noise ratio at the antenna array receiver $\text{SNR} = QE\left[\|H_k\|^2\right]/2\sigma^2_\theta$ in the case of a single antenna ($M = 1$) and antenna array ($M = 8$), respectively. In these figures, the block-Fourier algorithms are indicated as BFT-4 or BFT-16 if $D = 4$ or $D = 16$ is adopted, respectively. The other algorithm parameters are indicated in the figures.

In the single antenna scenario, for two or more iterations ($i \geq 2$) both BB and BL algorithms have performance similar to the one corresponding to the exact system inversion method.

On the contrary, the BFT algorithm strongly depends on the FFT size $D$ and the prelap (pre) and postlap (post) values. In fact, for $D = 16$, pre $> 0$ and post $> 0$, the BFT detector performance is close to the optimum one, while if $D = 4$ any combination of pre and post coefficients cannot obtain figures near to those corresponding to the exact inversion case being combination pre $= 1$, post $= 2$ the most effective ($L = 22$).

For the linear antenna array scenario with $M = 8$ elements, performance is significantly better than the previous one due to the effect of the array spatial processing. All algorithms show good performance except the BFT one for the artifacts introduced by the overlap-and-save technique (e.g. $D = 16$, pre $= 0$, post $= 0$; $D = 4$, pre $= 0$, post $= 0$; $D = 4$, pre $= 1$, post $= 0$ and $D = 4$, pre $= 0$, post $= 1$). It is worth noticing that only one iteration is enough for BB and BL algorithms to converge to the exact solution.

V. ALGORITHM COMPUTATIONAL COMPLEXITY

Tab. 4 shows the computational complexity of BB, BFT and BL algorithms in terms of complex multiplications ($\times 10^5$) for each semi-burst. The shown algorithms perform the matched filter in the time domain (e.g. BB and BL) or frequency domain (e.g. BFT). Matrix $R$ is tri-diagonal ($\nu = 2$) block-Toeplitz, with a lot of null blocks. Several algorithm optimizations have been adopted to reduce both computational complexity and storage size of the algorithms shown in Section [3]. For instance, in the BB algorithm it is possible to: \(i\) reduce the matrix multiplications of (30) to block multiplications, \(ii\) rearrange the matrices of blocks $R^{(+i)}$ and $R^{(-i)}$ as one column of blocks of variable size for each modified diagonal, \(iii\) reuse the already inverted blocks in the backward substitution phase [12].

Fig. 8 tries to summarize the information from Tab. 4 and Fig. 7. It is apparent that both Bareiss and Fourier (BFT-4) algorithms are well suited for low complexity detectors. On the contrary, the Levinson algorithm, even achieving good
1.2.0.6 1.6 1.8 1.9
Fig. 8. Performances vs. computational complexity of MUD algorithms at
appropriate for a simple hardware implementation.

a FPGA systolic array [23], [9] or an array of DSP/processors
ones requires more sophisticated hardware architecture such as

tions for hybrid CDMA systems are available; however, while

data units (see Fig. 10). However, the BB detector may be

efficiently designed exploiting pipelined structures and parallel

4 algorithm implementation. The BFT-4 algorithm may be

C

Algorithm

OMPUTATIONAL COMPLEXITY OF DETECTOR ALGORITHMS IN TERMS OF

9

Complex multiplications [x 10^5]

BER

M = 8

SNR = 8 dB

SNR = 10dB

SNR = 12dB

SNR = 14dB

SNR = 16dB

BFT-4

BL

BFT-16

SNR = 6 dB

Fig. 8. Performances vs. computational complexity of MUD algorithms at
different SNR conditions. Each dot of a curve indicates the approximation
degree adopted for the algorithm at that specific SNR. From left to right it is:
L = 6, 11, 22 for BFT-4 (D = 4), L = 2, 3, 4 for BFT-16 (D = 16), i = 1, 5, 9, 13, 17, 21 for BB and BL. Simulation values are the same employed in

performance, has high computational complexity and it is not

appropriate for a simple hardware implementation.

VI. HARDWARE IMPLEMENTATION

Fig. 9 and 10 show the block diagrams of the BB and BFT-
4 algorithm implementation. The BFT-4 algorithm may be
efficiently designed exploiting pipelined structures and parallel
data units (see Fig. 10). However, the BB detector may be
paralleled [21] and pipelined, too. Several MUD implementa-
tions for hybrid CDMA systems are available; however, while
the BFT-4 FPGA implementation is straightforward, the other
ones requires more sophisticated hardware architecture such as
a FPGA systolic array [23], [9] or an array of DSP/processors
such as the RCF (Reconfigurable Computer Fabric) processor

[10].

To avoid numerical problems, floating-point arithmetics
have been extensively used having care not to exceed the size
of the FPGA built-in multipliers. The floating-point numerical
format is indicated as (N_t, N_c) where N_t is the exponent and
N_t - N_c is the mantissa size. Both detector implementations
have been simulated adopting the same scenario parameters of
Section IV and their performances shown in Fig. 11 according
to the selected floating-point format. The FPGA implementa-
tion of the detectors dictates for the smallest data size: in both
cases, the (10, 5) format is enough to have figures very close
to the ones corresponding to the full precision simulations of
Fig. 7 and still to be under the size of the FPGA built-in
multipliers. The bad performances of the (10, 4) format are
due to overflow/underflow problems.

From the implementation point of view, comparing only
the design complexity of both BFT and BB processors, it is
apparent that the BFT-4 detector is the most suited for
hardware implementation due to its straightforward design.
In fact, in spite of its performance, the design of the BFT-
4 processor is very simple. The BFT-4 main elements are
the radix-4 FFT/IFFTs that may be easily implemented without
multipliers while the Cholesky computation element and the
matched filter may be designed with fast pipelined multiply-
and-accumulate (MAC) blocks. Assuming a latency of one
time slot (i.e. 675 µs) and estimating about 180 µs for ancillary
computations (e.g. channel estimation, whitening filtering,
is mandatory, the BFT-4 algorithm is the best solution for its straightforward design. However, the BB detector may be also used to solve performance problems of the Fourier detector at a comparable complexity.

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References

[1] S. Verdú: Multi-user Detection, Cambridge University Press, 1998.
[2] Y. Pigeonnat: Joint detection for UMTS: complexity and alternative solutions, Proc. IEEE Proc. of VTC 1999, Vol. 1, pp. 546-550, 1999.
[3] H.R. Karimi, N.W. Anderson: A novel and efficient solution to block-based joint-detection using approximate Cholesky factorization, Proc. IEEE Proc. of PIMRC 1998, Vol. 3, pp. 1340-1345, 1998.
[4] M. Vollmer, M. Haardt, J. Götz: Comparative Study of Joint-Detection Techniques for TD-CDMA based Mobile Radio Systems, Sel. Areas in Communications, Vol. 19, N. 8, pp. 1461-1475, Aug. 2001.
[5] M.J. Juntti, B. Aazhang: Finite memory length linear mutlisensor detector for asynchronous CDMA communications, IEEE Trans. on Comm. Vol. 54, N. 5, pp. 611-622, May 1997.
[6] J. Mayer, J. Schlee, T. Weber: Realtime feasibility of Joint Detection CDMA, Proc. of 2nd European Personal Mobile Communications Conference, pp. 245-252, Bonn, Germany, Sept. 1997.
[7] T. Weber, J. Schlee, S. Bahrenburg, P.W. Baier, J. Mayer, C. Euscher: A Hardware Demonstrator for TD-CDMA, IEEE Trans. on Vehi. Tech., Vol. 51, N. 5, pp. 877-892, Sept. 2002.
[8] M. Beretta, A. Colomonomic, M. Nicoli, V. Rampa, U. Spagnolini: Space-Time mutlisensor detectors for TDD-UTRA: design and optimization, IEEE Proc. VTC 2001, Vol. 1, pp. 78-82, 2001.
[9] D. Noguet: A reconfigurable systolic architecture for UMTS/TDD joint detection real time computation, IEEE Proc. of ISSSTAT, pp. 957-961, Sidney, Australia, Sept. 2004.
[10] E. Martinez: Introduction to TD-SCDMA on the MRC6011 RCF Device, Freescale Semiconductor Application Note AN2684, Rev. 1, 11/2004.
[11] A. Bifano, V. Rampa: Low Complexity Multiuser Detectors for TD-SCDMA Systems: Design and Implementation, Proc. of SoftCOM 2004, Split, pp. 444-448, Oct. 2004.
[12] E. Borello, L. Costa: Algoritmi e Architetture efficienti per la rivelazione multi-utenze nel sistema CWTS, Tesi as Dottore in Ingegneria (in italiano), Dipartimento di Elettronica e Informazione, Politecnico di Milano, 2004.
[13] E.H. Bareiss: Numerical solution of linear equations with Toeplitz and vector Toeplitz matrices, Numer. Math. Vol. 13, pp. 404-424, 1969.
[14] R.A. Wiggins, E.A. Robinson: Recursive solutions to the multichannel filtering problem, J. Geophys. Res., Vol. 70, pp. 1885-1891, 1965.
[15] A. Bifano, V. Rampa: Multiuser Detector for hybrid SCDMA Systems based on the Bareiss algorithm, IEEE Proc. of ICASSP 2005, Philadelphia, Vol. III, pp. 909-912, Mar. 2005.
[16] China Wireless Telecommunication Standard (CWTs) Working Group 1 (WG1): Physical channels and mapping of transport channels onto physical channels, TS C102 v3.3.0 (2000-09).
[17] M. Vollmer, M. Haardt, J. Götz: Schur algorithms for joint-detection in TD-CDMA based mobile radio systems, Ann. Telecommun. Vol. 54, N. 7-8, pp. 365-378, 1999.
[18] G.H. Golub, C.F. Van Loan: Matrix computation, The John Hopkins University Press, 1991.
[19] J. Rissanen: Algorithms for Triangular Decomposition of Block Hankel and Toeplitz Matrices with Application to Factoring Positive Matrix Polynomials, Math. Computations, Vol. 27, pp. 147-154, Jan 1973.
[20] A.E. Yagle: Multichannel Coupled Split Algorithms for Non-Hermitian Block-Toeplitz Matrices, IEEE Trans. on Signal Processing, Vol. 41, N. 1, 505-508, Jan. 1993.
[21] R.P. Brent: Parallel algorithms for Toeplitz systems, Numerical Linear Algebra, Digital Signal Processing, Proc. NATO ASI, Leuven, Belgium, August 1988, edited by G. H. Golub and P. Van Dooren, NATO ASI Series F: Computer and Systems Sciences, Vol. 70, Springer-Verlag, 1991.

[22] A.W. Bojanczyk, R.P. Brent, F.R. de Hoog and D.R. Sweet: On the stability of the Bareiss and related Toeplitz factorization algorithms, SIAM J. Matrix Analysis and Applications, Vol. 10, 225-244, 1995.

[23] A. Bifano, A. Colamonico, M. Nicoli, V. Rampa, U. Spagnolini: Sliding windows multiuser detectors for TD-SCDMA systems, Proc. of European Conference on Wireless Technology - ECWT '02, Session E3, September 2002.

[24] COST-207: Digital land mobile radio communications, Final Report, Luxemburg, Office for Official Publications of the European Communities, 1989.

[25] G.L. Stuber: Principles of Mobile Communications, Kluwer Academic, 1996.

[26] M. Nicoli, M. Stemad, U. Spagnolini, A. Ahlen, Reduced-rank channel estimation and tracking in time-slotted CDMA systems, Proc. IEEE International Conference on Communications (ICC '02), vol. 1, pp. 533-537, April-May 2002.

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