1.3 kV Vertical GaN-Based Trench MOSFETs on 4-Inch Free Standing GaN Wafer

Wei He¹, Jian Li¹, Zeliang Liao¹, Feng Lin¹, Junye Wu¹, Bing Wang¹, Maojun Wang², Nan Liu³, Hsien-Chin Chiu⁴, Hao-Chung Kuo⁵, Xinnan Lin⁶, Jingbo Li⁷ and Xinke Liu¹*

Abstract

In this work, a vertical gallium nitride (GaN)-based trench MOSFET on 4-inch free-standing GaN substrate is presented with threshold voltage of 3.15 V, specific on-resistance of 1.93 mΩ·cm², breakdown voltage of 1306 V, and figure of merit of 0.88 GW/cm². High-quality and stable MOS interface is obtained through two-step process, including simple acid cleaning and a following (NH₄)₂S passivation. Based on the calibration with experiment, the simulation results of physical model are consistent well with the experiment data in transfer, output, and breakdown characteristic curves, which demonstrate the validity of the simulation data obtained by Silvaco technology computer aided design (Silvaco TCAD). The mechanisms of on-state and breakdown are thoroughly studied using Silvaco TCAD physical model. The device parameters, including n⁻-GaN drift layer, p-GaN channel layer and gate dielectric layer, are systematically designed for optimization. This comprehensive analysis and optimization on the vertical GaN-based trench MOSFETs provide significant guide for vertical GaN-based high power applications.

Keywords: Free standing gallium nitride (GaN), Trench MOSFET, GaN MOSFET, Breakdown, TCAD

Introduction

Wide-bandgap GaN-based power devices have been regarded as the great potential candidates for the next generation efficient power electronics and compact power systems, owing to the superior material properties such as high electron mobility, large breakdown field strength and high thermal stability [1–5]. Compared with high electron mobility transistors (HEMTs) [6–11] and current aperture vertical electron transistors (CAVETs) [12–15], GaN-based trench metal oxide semiconductor field effect transistors (MOSFETs) [16–18] are more competitive to realize intrinsically normally-off operation with higher current density, lower specific on-resistance ($R_{on,sp}$) and lower current collapse. Moreover, GaN-based trench MOSFETs possess relatively simple manufacturing process and do not need the regrowth of AlGaN/GaN layers [19, 20].

The development of lateral GaN-based MOSFETs has approximately come to saturation, due to the breakdown voltage ($V_{BR}$) limited by the length of lateral drift region. Although the growth of length can increase $V_{BR}$, the size of device enlarges, leading to reduction of the effective current density per unit chip area. In contrast, vertical GaN-based devices have been fully advanced. Under the same required $V_{BR}$ and amperage rating, smaller size and less cost can be realized on vertical GaN-based MOSFETs when make a contrast with lateral GaN MOSFETs [21]. In comparison with Si, Sapphire, SiC and Diamond substrate, the MOSFETs on free-standing GaN substrate can greatly reduce the probability of the high-density trap states and non-linearity contributed by lattice mismatch while operating at high power [22].

More studies have made great progress in $V_{BR}$, $R_{on,sp}$ and device reliability for GaN vertical MOSFETs in recent years. Floating P-body had been introduced in the N⁻-GaN drift region to form “P-body/N-drift” junction...
via TCAD simulation for the improvement of $V_{BR}$ of the enhancement-mode vertical GaN MOSFET [23]. Vertical GaN interlayer-based trench MOSFET (OG-FET) on a large-area in-situ oxide performed threshold voltage ($V_{th}$) of 2.5 V, $R_{on,sp}$ of 0.98 mΩcm² and $V_{BR}$ of 700 V with regrown 10-nm unintentional-doped-GaN interlayer as the channel and 50-nm in-situ Al₂O₃ as the gate dielectric [24]. Vertical GaN trench-MOSFETs with MBE regrown UID-GaN channel were investigated, which avoided the need to reactivate the buried body p-GaN and promised the same benefit on channel mobility compared to the MOCVD regrowth [25]. The device characteristics had been improved for vertical GaN trench MOSFETs by using Silvaco ATLAS 2-D simulation in order to get the best trade-off between $V_{BR}$ and $R_{on,sp}$ [26].

In this work, we present vertical GaN-based trench gate MOSFETs (GaN TG-MOSFETs) on 4-inch free-standing GaN substrate exhibiting normally off operation for high power applications. We use Silvaco TCAD to simulate the structure and performance of GaN TG-MOSFETs based on semiconductor physics and advanced process. The simulation results obtained by Silvaco ATLAS simulation are consistent well with experiment data on the characteristic curves of transfer, output, and breakdown voltage, respectively. The device parameters are researched comprehensively by using TCAD for providing guide in actual fabrication and optimization. The design of the parameters includes the thickness of n⁻-GaN drift body layer ($L_{drih}$), n⁻-GaN drift trench region ($L_{trench}$), p-GaN channel layer ($L_{channel}$) and gate dielectric layer ($L_{dielec}$). The doping density of p-GaN channel layer ($N_{p}$) and n⁻-GaN drift layer ($N_{d}$) are included.

**Experiment and Simulation Approach**

High-quality, large-size and less-expensive GaN substrates are crucial for the progress of vertical GaN power devices. More techniques were proposed to optimize the growth of bulk GaN crystals, such as halide vapor phase epitaxy (HVPE), high nitrogen pressure solution (HNPS), basic and acidic ammonothermal, Na-flux method and near atmospheric pressure solution growth [27, 28]. HVPE is the main method for mass fabrication of GaN crystals, due to its high growth rate, high purity, high process repeatability and easy doping. The transparent 4-inch freestanding GaN wafer grown by HVPE with 13 points position for test is shown in Fig. 1a. We utilized a 420-μm-thick free-standing n⁻-GaN substrate in the device fabrication with the average mobility of 614 cm²/Vs⁻¹ and the average dislocation density of $1.94 \times 10^6$ cm⁻² at the top surface, as determined by contactless Hall measurement and cathodoluminescence (CL). The test result and CL image of the epitaxial layer are presented in Fig. 1b, c, respectively.

The fabrication process of the GaN TG-MOSFETs discussed in this work is shown in Fig. 1d. The epitaxial growth began with 12-μm lightly doped $8.0 \times 10^{15}$ cm⁻³ n⁻-GaN as the drift region. A 1.0-μm heavily doped p-GaN with a doping density of $1.0 \times 10^{18}$ cm⁻³ was deposited as the channel region. Thereafter, a 0.2-μm-thick heavily doped n⁺-GaN with a doping density of $3 \times 10^{18}$ cm⁻³ was grown as the source contact layer. The device fabrication process started with the formation of 0.2-μm-deep vertical trench and 1.7-μm-deep vertical mesa for p-body and gate contacts by using Cl₂-based gases in reactive ion etching (RIE) at 15 W power, respectively. A 16-nm-thick Al₂O₃ film was deposited by atomic layer deposition (ALD) as gate dielectric. High-quality and stable MOS interface with low-density trap states is essential for GaN TG-MOSFETs. A two-step process, including simple acid cleaning and a following (NH₄)₂S passivation, was required to drastically reduce the interface states and border traps [29]. The source and drain electrodes with Ti/Al were annealed at 550 °C for 5 min in N₂ ambient for ohmic contacts. The gate and p-body electrodes were composed of Ti/Au and Palladium, respectively. A 400-nm-thick SiO₂ film was deposited by plasma enhanced chemical vapor deposition (PECVD) as the passivated isolation mesa. Finally, field plate termination was employed to impair the peak electric field crowded at the edge of PN junction around the isolation mesa. The Al-based field plate was connected to the source electrode.

The schematic of energy band lined-up at the Al₂O₃/GaN heterointerface in Fig. 1e. The forbidden band of GaN was exactly contained in that of Al₂O₃, where the deviations of the conduction band and valence band were 3.38 eV and 0.22 eV, respectively. It revealed that Al₂O₃ could maintain excellent insulation with GaN for electrons, which greatly reduced gate leakage current and improved device performance. The 3D drawing structure and parameters needed for optimization are shown in Fig. 1f. Figure 1g shows the micrograph of the device. The hexagonal crystal structure contained the outward vertical C axis, three horizontal axes $a_1$, $a_2$ and $a_3$, and crystal planes in various directions.

The physical simulation models concerned for simulation were the parallel electric field-dependent mobility model, concentration-dependent mobility model, low field mobility model, Shockley–Read–Hall recombinination model, Auger recombination model, impact ionization model, energy bandgap narrowing model and trap model [26, 29–31]. The main physical models and parameter values for simulation are shown in Table 1.

For GaN simulation, Si donors and Mg acceptors were not completely ionized at room temperature since their high activation energies, especially for Mg-doped
Thus, according to Fermi–Dirac distribution, the incomplete ionization model was incorporated in the simulation for accurately reproducing the breakdown voltage. The ionized donors and acceptors impurity concentrations were given as follows

\[
N_D^+ = \frac{N_D}{1 + g_D \cdot \exp \left( \frac{E_F + E_{D0} - \theta_n \cdot \sqrt{N_D - E_C}}{kT} \right)}
\]

\[
N_A^- = \frac{N_A}{1 + g_A \cdot \exp \left( \frac{E_V + E_{A0} - \theta_p \cdot \sqrt{N_A - E_V}}{kT} \right)}
\]

Here, \( g_D \) and \( g_A \) are the appropriate degeneracy factors for conduction and valence bands. \( E_{D0} \) and \( E_{A0} \) are the donor and acceptor ionization energy at very low doping levels. \( \theta_n \) and \( \theta_p \) are constants accounting for geometrical factors as well as for the properties of the material. Low field mobility model is the result of fitting Caughey Thomas like model to Monte Carlo data [26, 32]. It can be defined as

\[
\frac{\mu_{1(n/p)}}{T, N} = \frac{\mu_1(n/p) \cdot (T/300)^{\beta_1(n/p)}}{(\mu_2(n/p) - \mu_1(n/p)) \cdot (T/300)^{\beta_2(n/p)}} \left[ 1 + \left( \frac{N}{N_{ref(n/p)}} \right)^{(\beta_3(n/p))/300} \right]^{\rho(n/p)/(T/300)^{\beta_4(n/p)}}
\]

where \( \mu_1, \mu_2 \) are the minimum and maximum mobility, \( \rho, \beta_1, \beta_2, \beta_3, \beta_4 \) are all temperature dependent fitting parameters, \( N_{ref} \) is the reference doping level and \( N \) is the donor concentration.

The Poisson’s equations and Current continuity equation were essential for the analysis of simulation [35]. As in semiconductor PN junction, avalanche breakdown occurred when the impact ionization integral reached unity

\[
I_n = \int \alpha_n \exp \left( \int w \alpha_p - \alpha_n \, dv \right) \, dw = 1
\]

where \( I_n \) is the impact ionization integral of electrons. The utilized ionization rate model of electrons and holes
are variation of the classical Chynoweth model [36], which based upon the following expressions,

\[ \alpha_n = AN \cdot \exp\left[-\left(\frac{BN}{E}\right)^{BETAN}\right] \]  

(5)

\[ \alpha_p = AP \cdot \exp\left[-\left(\frac{BP}{E}\right)^{BETAP}\right] \]  

(6)

Here, \( E \) is the electric field in the direction of current flow at the p-GaN channel layer in the structure. Various group has reported impact ionization coefficients to accurately predict the breakdown of GaN power devices in recent years [37–41]. The coefficients \( AN, AP, BN, BP, BETAN \) and \( BETAP \) of the impact ionization model in this work were determined by referring to the experiments above.

In this study, the work was mainly carried out by TCAD. The data obtained by simulation had been calibrated with the result of experiment on GaN TG-MOSFET shown in the third part. The comprehensive analysis and optimization design on \( L_{\text{drift}}, L_{\text{trench}}, L_{\text{dielectric}}, L_{\text{channel}}, N_a \) and \( N_d \) of devices were demonstrated in the fourth part, respectively.

### Results and Discussion

The initial device parameters of simulation model were set as follows: \( N_d = 8.0 \times 10^{15} \text{ cm}^{-3}, N_a = 1.0 \times 10^{18} \text{ cm}^{-3}, L_{\text{drift}} = 12 \mu\text{m}, L_{\text{trench}} = 0.5 \mu\text{m}, L_{\text{channel}} = 1.0 \mu\text{m}, \) and \( L_{\text{dielectric}} = 16 \text{ nm} \). The interface state could capture the free electrons in the channel and formed the negative interface charge, leading to the decrease of the number of free electrons and the increase of \( R_{\text{on}, \text{sp}} \). A low density of interface state was beneficial to reduce \( R_{\text{on}, \text{sp}} \) and switch loss. The interface state in the simulation was defined as \( 10^{11} \text{ cm}^{-2} \cdot \text{eV}^{-1} \) by referring to the previous work [25]. The characteristic curves of transfer, output, and breakdown of GaN TG-MOSFET via experiment (Exp) and simulation (Sim) are shown in Fig. 2, respectively. This simulation results were consistent well with the data of experiment, which could verify the validity of the results obtained by simulation and calibrate the simulation model.

Figure 2a shows the \( I_D-V_G \) characteristics at \( V_{DS} = 0.5 \text{ V} \). Several extraction methods were used to determine the value of \( V_{th} \) from the measured \( I_D-V_G \) characteristics [42]. Normally-off operation with \( V_{th} \) (defined at \( I_{DS} = 1 \mu\text{A/mm} \)) of 3.15 V was observed. Figure 3a shows the current could not be conducted between the source and drain, since the channel was not yet formed a conduction path. In Fig. 3b, the inversion layer of electron was effectively generated in the channel only when \( V_{GS} > V_{th} \), hence generating the drain-to-source current. The distributions of energy band along line A and line B during off-state and on-state are shown in Fig. 3c and Fig. 3d, respectively. From off-state to on-state, the energy of conduction band (CB) obviously reduced until closing to the Quasi-Fermi level (QFL). Therefore, electrons could easily jump to CB and generate conduction current. Figure 2b exhibits the output \( I-V \) characteristics at \( V_{GS} = 0 \text{ V}, 5 \text{ V}, 10 \text{ V}, 15 \text{ V} \) and \( 20 \text{ V} \), respectively. The \( R_{on,sp} \) estimated from the linear region was 1.93 mΩ cm² at \( V_{DS} = 0.5 \text{ V} \) and \( V_{GS} = 20 \text{ V} \).

Figure 2c demonstrates the off-state \( I-V \) characteristics measured at \( V_{GS} = 0 \text{ V} \). This work achieved the hard breakdown \( V_{BR} \) of 1306 V when \( I_{DS} = 50 \text{ mA/cm²} \) from experiment, while the \( V_{BR} \) of simulation reached 2278 V. The insufficient activation of the Mg dopant existing in the p-GaN was considered as the reason for making the discrepancy in \( V_{BR} \) between experiment and simulation. Finally, the corresponding figure of merit (FOM) obtained were 0.88 GW/cm² and 1.68 GW/cm² by experiment and simulation, respectively.

Two breakdown mechanisms, namely punch-through breakdown and avalanche breakdown, existed in the device, which were dominated by the product of \( L_{\text{channel}} \) and \( N_a \) \( (L_{\text{channel}} \cdot N_a) \) of p-GaN. Taking the
$N_a = 2.0 \times 10^{17}$ cm$^{-3}$ and various $L_{\text{channel}}$ for example by simulation as shown in Fig. 4a. Punch-through breakdown would occur when $L_{\text{channel}} \cdot N_a$ was lower than a certain value, such as $L_{\text{channel}} = 0.6$ μm and $N_a = 2.0 \times 10^{17}$ cm$^{-3}$ in Fig. 4a. However, it would be changed to avalanche breakdown when $L_{\text{channel}} \cdot N_a$ was high enough, such as $L_{\text{channel}} = 0.8$ μm and $N_a = 2.0 \times 10^{17}$ cm$^{-3}$. Moreover, the breakdown mechanisms were studied in detail from the expansion of depletion region (DR), distributions of electric field and impact generation rate (IGR). Figure 4b shows the schematic of the device. Figures 4c–f and 5a–f show the expansion of DR and avalanche and avoid punch-through breakdown with the permature breakdown. The peak IGR was located in the red circle of Fig. 6d. The electron current mainly flowed to drain, while hole current flowed to the source along p-GaN region. In the red circle of Fig. 6d, the peak IGR was located at the gate corner. It implied that the breakdown characteristic was similar to that of PN junction diode as long as punch-through did not occur. The simulation showed that device could achieve avalanche and avoid punch-through breakdown with enough value of $L_{\text{channel}} \cdot N_a$. The effect of various $N_a$ on the breakdown mechanism was similar to that of $L_{\text{channel}}$.

### Analysis and Performance Evaluation

This simulation focused on studying the effects of various device parameters and obtaining the scheme of optimization design. Firstly, the thickness and doping density of n$^-$-GaN drift layer were researched with different initial values. Then, we analysed the thickness and doping density of p-GaN channel layer based on the optimal parameters of n$^-$-GaN drift layer. Finally, the impact of the thickness of gate dielectric was thoroughly studied.
All the changes of the above parameters were discussed within a reasonable range. The power figure of merit $FOM = \frac{V_{BR}^2}{R_{on,s}}$ and $V_{th}$ could be used as a criterion for optimization.

**Analysis the Influence of n⁻-GaN Drift Layer**

As shown in Fig. 7a, $V_{BR}$ increased and saturated at a certain value as $L_{drift}$ increased with different initial conditions. The phenomenon that DR extended and saturated with the growth of $L_{drift}$ caused the $V_{BR}$ increased and saturated. Conversely, $V_{BR}$ decreased with the growth of $N_d$. The situation was equivalent to the effect of the doping.
(a) \( N_a = 2.0 \times 10^{17} \text{ cm}^{-3}, L_{\text{channel}} = 1.2 \mu \text{m} \) (avalanche)

(b) \( N_a = 2.0 \times 10^{17} \text{ cm}^{-3}, L_{\text{channel}} = 0.4 \mu \text{m} \) (punch-through)

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**Fig. 5** a-f Depletion region at different reverse bias under \( N_a = 2.0 \times 10^{17} \text{ cm}^{-3} \) and \( L_{\text{channel}} = 1.2 \mu \text{m} \), including \( V_{DS} = 200 \text{ V}, 400 \text{ V}, 800 \text{ V}, 1000 \text{ V}, 1500 \text{ V} \) and \( 2000 \text{ V} \). g Electric Field distributed along line B at \( V_{DS} = 2000 \text{ V} \)

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**Fig. 6** (a), (b) were the distributions of Total Current Density and Impact Gen Rate under \( N_a = 2.0 \times 10^{17} \text{ cm}^{-3} \) and \( L_{\text{channel}} = 0.4 \mu \text{m} \), respectively. (c), (d) were the distributions of Total Current Density and Impact Gen Rate under \( N_a = 2.0 \times 10^{17} \text{ cm}^{-3} \) and \( L_{\text{channel}} = 1.2 \mu \text{m} \), respectively.

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**Fig. 7** (a) Simulated \( R_{\text{on,sp}} \) and \( V_{BR} \) of the device versus \( L_{drift} \) and \( N_d \). (b) \( V_{th} \) and FOM as a function of \( L_{drift} \) and \( N_d \). (c) Simulated \( R_{\text{on,sp}} \) and \( V_{BR} \) of the device versus \( L_{trench} \) and \( N_d \). (d) \( V_{th} \) and FOM as a function of \( L_{trench} \) and \( N_d \). In (a)-(d), the square, circle and triangle curves were simulated under \( N_d = 6.0 \times 10^{15} \text{ cm}^{-3} \), \( N_d = 8.0 \times 10^{15} \text{ cm}^{-3} \) and \( N_d = 1.0 \times 10^{16} \text{ cm}^{-3} \), respectively.
concentration in the low-doped side of the PN single junction diode on the $V_{BR}$, which demonstrated that the value of $N_d$ was inversely proportional to $V_{BR}$. It implied that $V_{BR}$ prematurely saturated at thin $L_{drift}$ with high $N_d$. Low $N_d$ had larger DR than high $N_d$ due to the IGR of electron was low. Large DR could withstand high voltage and prevent electron absorbing electric field energy to reach breakdown. The change of $R_{on,sp}$ was mainly caused by the variation of $R_{drift}$ ($R_{on,sp}$ of $n$-GaN drift layer). $R_{on,sp}$ decreased with the increase of $N_d$ and decrease of $L_{drift}$, respectively. $R_{on,sp}$ decreased from 2.55 m$\Omega$·cm$^2$ to 1.56 m$\Omega$·cm$^2$ and $V_{BR}$ reduced from 2558 to 1997 V as $N_d$ increased from $8.0 \times 10^{15}$ cm$^{-3}$ to $1.0 \times 10^{16}$ cm$^{-3}$ under $L_{drift} = 12$ $\mu$m. In Fig. 7b, the obtained peak FOM were 2.76 GW/cm$^2$, 2.69 GW/cm$^2$ and 2.62 GW/cm$^2$ under $L_{drift} = 16$ $\mu$m, $L_{drift} = 12$ $\mu$m, and $L_{drift} = 10$ $\mu$m with the growth of $N_d$, respectively. It demonstrated that the optimal FOM could be obtained under the low $N_d$ and thick $L_{drift}$. In contrast, the change of $N_d$ and $L_{drift}$ had no effect on $V_{th}$ and it remained at 3.15 V. The impact on $R_{on,sp}$ and $V_{BR}$ were obvious by the change of $N_d$ and $L_{drift}$ while hardly influenced $V_{th}$.

With the increase of $L_{trench}$ from 0.1 to 1.0 $\mu$m in Fig. 7c, $R_{on,sp}$ continuously decreased. In contrast, $V_{BR}$ and FOM first increased and then decreased as the advance of $L_{trench}$ finally reaching peak value at $L_{trench} = 0.2$ $\mu$m. The obtained peak FOM were 3.15 GW/cm$^2$, 3.45 GW/cm$^2$ and 3.64 GW/cm$^2$ under $N_a = 6.0 \times 10^{15}$ cm$^{-3}$, $N_a = 8.0 \times 10^{15}$ cm$^{-3}$, and $N_a = 1.0 \times 10^{16}$ cm$^{-3}$, respectively. The impact of $L_{trench}$ on FOM was apparent when it was thin. The variety of $N_a$ and $L_{trench}$ also made little difference on $V_{th}$. $V_{th}$ showed independence for the change of $N_a$, $L_{drift}$ and $L_{trench}$ due to the p-type channel region.

**Analysis the Impact of p-GaN Channal and Dielectric**

The effects of the $L_{channel}$ and $N_a$ of p-GaN channel layer were investigated based on $L_{drift} = 12$ $\mu$m and $L_{trench} = 0.2$ $\mu$m of $n$-GaN drift layer. The change of $R_{on,sp}$ was mainly caused by the variation of $R_{channel}$ ($R_{on,sp}$ of p-GaN channel layer). The curves of $R_{on,sp}$ showed continuous rising trend with the enhancement of $L_{channel}$ as shown in Fig. 8a. As $N_a$ increased from $2.0 \times 10^{17}$ cm$^{-3}$ to $3.0 \times 10^{18}$ cm$^{-3}$ under $L_{channel} = 1.0$ $\mu$m, $R_{on,sp}$ showed increasing trends from 1.94 m$\Omega$·cm$^2$ to 1.96 m$\Omega$·cm$^2$. The effect on the $R_{on,sp}$ brought by the variety of $L_{channel}$ was little. The growth of $N_a$ could enlarge the $V_{BR}$ from 65 to 2632 V under 0.1 $\mu$m. $V_{BR}$ increased and saturated at $L_{channel} = 0.8$ $\mu$m under $N_a = 2.0 \times 10^{17}$ cm$^{-3}$. In contrast, $V_{BR}$ increased and saturated at $L_{channel} = 0.2$ $\mu$m under $N_a = 8.0 \times 10^{17}$ cm$^{-3}$ and $N_a = 1.0 \times 10^{18}$ cm$^{-3}$, respectively. Moreover, $V_{BR}$ kept saturated from 0.1 $\mu$m to 1.0 $\mu$m of $L_{channel}$ under $N_a = 3.0 \times 10^{18}$ cm$^{-3}$. The high enough value of $L_{channel} = N_a$ could achieve avalanche breakdown, which could be seen from the saturated $V_{BR}$. On the contrary, the unsaturated $V_{BR}$ was known as punch-through breakdown. Similarly, the variation trend of FOM was the same as $V_{BR}$. The peak FOM obtained was 3.59 GW/cm$^2$. $V_{th}$ grew from 1.19 V to 7.93 V under $L_{channel} = 1.0$ $\mu$m with the increase of $N_a$ as shown in Fig. 8b. The change of $N_a$ had a marked effect on $V_{th}$, whereas the impact brought by the variety of $L_{channel}$ on $V_{th}$ was negligible.

The impact of the $L_{dielectric}$ was researched based on $L_{channel} = 1.0$ $\mu$m. The growth of $L_{dielectric}$ would reduce $C_{ox}$ and electron concentration of channel layer under on-state condition, resulting in larger $R_{on,sp}$ and $V_{th}$. $R_{on,sp}$ increased from 1.92 m$\Omega$·cm$^2$ to 2.24 m$\Omega$·cm$^2$ and $V_{th}$ enhanced from 1.87 V to 8.97 V for $L_{dielectric}$ increasing from 8 to 50 nm as shown in Fig. 8c. $L_{channel}$ had no effect on $V_{BR}$, leading to the reduction of FOM from 3.63 GW/cm$^2$ to 3.10 GW/cm$^2$.
Conclusion
In this work, we analysed the performance of the fabricated GaN TG-MOSFET on 4-inch free-standing GaN substrate by Silvaco TCAD. The mechanisms of on-state and breakdown have been well studied. The key device parameters have been thoroughly researched considering the trade-off between $R_{on,AP}$ and $V_{BR}$. The normally off operation and high breakdown voltage show enormous potential to provide a bright future application for vertical GaN-based high power electronics.

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Authors’ contributions
XL and WH conceived the idea. ZL and JL did the experiment part of this work. JL and FL did the simulation part of this work. JW collected and sorted out the data. JZ and JL did the experiment part of this work. We thank the reviewers for their valuable comments.

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Availability of data and materials
All data generated or analyzed during this study are included in the article.

Declarations

Competing interests
The authors declare that they have no competing interests.

Author details
1College of Materials Science and Engineering, College of Electronics and Information Engineering, College of Physics and Optoelectronic Engineering, Institute of Microelectronics (IME), Shenzhen University, Shenzhen 518060, China. 2Institute of Microelectronics, Peking University, Beijing 100871, China. 3Shaanxi Reactive Microelectronics Co., Ltd, Xi’an 710075, China. 4Department of Electronic Engineering, Chang Gung University, Taoyuan 333, Taiwan. 5Department of Photonic and Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan. 6The Shenzhen Key Lab of Advanced Electronic Device and Integration, ECE, Peking University Shenzhen Graduate School, Shenzhen 518055, China. 7Institute of Semiconductors, South China Normal University, Guangzhou 510631, Guangdong, China.

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