SYNTHESIZING COLLECTIVE COMMUNICATION ALGORITHMS FOR HETEROGENEOUS NETWORKS WITH TACCL

Aashaka Shah 1  Vijay Chidambaram 1 2  Meghan Cowan 3  Saeed Maleki 3  Madan Musuvathi 3
Todd Mytkowicz 3  Jacob Nelson 3  Olli Saarikivi 3  Rachee Singh 3

ABSTRACT

Large ML models and datasets have necessitated the use of multi-GPU systems for distributed model training. To harness the power offered by multi-GPU systems, it is critical to eliminate bottlenecks in inter-GPU communication — a problem made challenging by the heterogeneous nature of interconnects. In this work, we present TACCL, a synthesizer for collective communication primitives for large-scale multi-GPU systems. TACCL encodes a profiled topology and input size into a synthesis problem to generate optimized communication algorithms. TACCL is built on top of the standard NVIDIA Collective Communication Library (NCCL), allowing it to be a drop-in replacement for GPU communication in frameworks like PyTorch with minimal changes. TACCL generates algorithms for communication primitives like ALLGATHER, ALLTOALL, and ALLREDUCE that are up to 3× faster than NCCL. Using TACCL’s algorithms speeds up the end-to-end training of an internal mixture of experts model by 17%. By decomposing the optimization problem into parts and leveraging the symmetry in multi-GPU topologies, TACCL synthesizes collectives for up to 80-GPUs in less than 3 minutes, at least two orders of magnitude faster than other synthesis-based state-of-the-art collective communication libraries.

1 INTRODUCTION

Modern language modeling tasks employ truly massive models. MT-NLG is a generative language model using the transformer model architecture with 530 billion parameters (MT-NLG). Likewise, the Switch-C mixture of experts model has 1.6 trillion parameters (Fedus et al., 2021). Large models (trained on large amounts of text) are often more accurate on downstream tasks than their smaller counterparts and thus this trend of large models is here to stay.

Models of this size do not fit in a single GPU and therefore need to be distributed across many GPUs using model, pipeline and expert parallelism (Shoeybi et al., 2019; Lepikhin et al., 2020; Fedus et al., 2021) for training and inference. Training large models takes significant hardware resources and inference often requires low-latency response for interactive scenarios. Thus, efficient utilization of training and inference hardware is paramount to the success of infusing AI into our daily lives.

Inspired by MPI (Dongarra et al., 2013), NVIDIA released NCCL (NVIDIA NCCL), a set of communication primitives (ALLGATHER, ALLREDUCE, etc.) for GPU to GPU communication, both within a node and across. Designing fast communication collectives requires solving two key challenges. First, the collective has to be optimized specifically for the underlying topology. This is particularly important for workloads running on a large number of GPUs wherein the underlying topology is necessarily heterogeneous, e.g., with GPUs inside nodes connected using faster NVLinks (150-300 GBps unidirectional bandwidth per GPU) and across nodes using relatively slower Infiniband links (12.5-25 GBps per NIC). The popular Ring ALLREDUCE — used for example in NCCL — is bottlenecked by the slowest link in the topology (Wang et al., 2020).

Second, the collective has to be optimized specifically for the input size. As observed in recent work (Cai et al., 2021), although bandwidth-optimal algorithms (such as Ring) are optimized for large input sizes (a few GB), they do not necessarily perform well with smaller input sizes. Typically, the input sizes seen in training and inference scenarios can range from a few KB to a few MB for model parallelism. This means that communication algorithms need to be optimized for both latency and bandwidth.

To address these challenges, we develop TACCL (Topology Aware Collective Communication Library), a tool that empowers developers with abstractions to model GPU topologies, search the space of algorithms for various input sizes, and a backend to execute them during training or inference.
This paper demonstrates the efficacy of TACCL by first strates how a developer uses TACCL to search over the hardware. For each hardware platform, the paper demon-

Inference scenarios on NVIDIA’s DGX-2 distributed and communication algorithms used in model and data parallel training investigating the performance of critical collective commu-

can be expressed as ratios of small integers.

erogeneous bandwidths in SCCL is only efficient when they model links with heterogeneous latencies and modeling heter-

size to decide between two main types of communication algorithms — Ring and Tree, it is agnostic to the exact performance profile of the links, and thus (as we show) is often multiple times slower than TACCL’s custom collectives. Likewise, while Blink (Wang et al., 2020) specializes for the underlying topology by using a spanning-tree packing algorithm to maximize bandwidth utilization, it defaults to a hierarchical approach for cross-node communication. And, lastly, SCCL (Cai et al., 2021) specializes collectives for input sizes, but its restrictive formulation cannot faithfully model links with heterogeneous latencies and modeling heter-

eon of algorithms for various input sizes. Our experiments show that TACCL generated algorithms outperform both NCCL and hierarchical algorithms, generated by com-

workload.

In contrast, prior work does little to specialize collective communication algorithms for the underlying topology and input sizes. For example, while NCCL uses the topology of GPU connections and NIC placement along with buffer size to decide between two main types of communication algorithms — Ring and Tree, it is agnostic to the exact performance profile of the links, and thus (as we show) is often multiple times slower than TACCL’s custom collectives. Likewise, while Blink (Wang et al., 2020) specializes for the underlying topology by using a spanning-tree packing algorithm to maximize bandwidth utilization, it defaults to a hierarchical approach for cross-node communication. And, lastly, SCCL (Cai et al., 2021) specializes collectives for input sizes, but its restrictive formulation cannot faithfully model links with heterogeneous latencies and modeling heterogeneous bandwidths in SCCL is only efficient when they can be expressed as ratios of small integers.

This paper demonstrates the efficacy of TACCL by first investigating the performance of critical collective communication algorithms used in model and data parallel training and inference scenarios on NVIDIA’s DGX-2 distributed hardware, as well as an Azure NDv2 cloud-based distributed hardware. For each hardware platform, the paper demonstrates how a developer uses TACCL to search over the space of algorithms for various input sizes. Our experiments show that TACCL generated algorithms outperform both NCCL and hierarchical algorithms, generated by com-

Figure 1 demonstrates the overall workflow of TACCL. It synthesizes algorithms specialized both for the underlying topology and input sizes as follows: First, the developer uses bandwidth and latency probes to determine the underlying physical topology (see Section 2), which enables TACCL to be applicable in virtualization infrastructure that obscures the underlying topology. These probes additionally provide the latency and bandwidth of each link in the topology. Then, the developer uses TACCL to create a logical topology that avoids over-subscription of specific links and switches (Section 3). Finally, the developer encodes the logical topology, along with latency and bandwidth costs for a specific input size, into a novel mixed-integer linear programming prob-

| Collectives | Data partitioning | Solver inclination | Number of instances |
|-------------|-------------------|-------------------|---------------------|
| A\_LLGATHER | Heuristic ordering | Lowering          | Runtime             |
| Path encoding | Contiguity encoding |                  |                     |

Figure 1. TACCL workflow.

### 2 Physical Topology Profiler

A variety of multi-GPU systems have been developed to meet the scaling challenges posed by growing machine learning models. The performance characteristics of their heterogeneous links are sparsely documented and for some cloud offerings (Azure ND-series) even the topology is not given. As a first step towards specializing collective communication for these systems, TACCL includes a physical topology profiler to infer performance characteristics of links (§2.1) and topologies of multi-GPU systems (§2.2).

#### 2.1 Profiling and modeling link performance

TACCL uses the well-known $\alpha$-$\beta$ (Hockney, 1994) cost model, where $\alpha$ is the latency of a link and $\beta$ is the inverse of its bandwidth. The cost of sending a chunk of size $s$ along a link is $\alpha + \beta \cdot s$. In this section, we show how the physical topology profiler infers $\alpha$ and $\beta$ costs of different types of links in GPU systems.

Modern GPU systems, e.g., Azure NDv2 (Figure 2a) and Nvidia DGX-2 (Figure 2c), have the following types of
interconnects: (1) *Peripheral Component Interconnect Express* (PCIe), (2) NVLink (Nvidia NVLink), (3) Infiniband (IB) NICs (Nvidia Infiniband). A PCIe bus connects GPUs to CPUs with limited shared bandwidth (PCIe Gen3 offer $\approx 13$ Gbps). PCIe connections often form a hierarchy with PCIe switches (Figure 2b). NVLink (Nvidia NVLink), however, is a GPU to GPU intra-node connection with dedicated bandwidth. NVLinks are either directly connected to other GPUs (see Azure NDv2 in Figure 2a) or they are connected to other GPUs via NVSwitches (Nvidia NVSWITCH) (see Nvidia DGX2 in Figure 2c). NVSwitches enable fully-connected GPU-GPU communication through NVLinks. IB is a multi-node interconnect which allows GPUs to communicate with GPUs in other nodes like in the Azure NDv2 (Figure 2b). IB NICs are usually connected to PCIe switches and GPUs may communicate directly with the NICs through Remote Direct Memory Access (RDMA) or indirectly via host memory.

The profiler empirically derives the $\alpha$ and $\beta$ parameters of different links in the network by performing peer-to-peer data transfers between GPUs. We send $n$ chunks one after another on a link and measure the time to transfer. As per the $\alpha - \beta$ cost model, the time to transfer is $n \cdot (\alpha + \beta \cdot s)$. We then send $n$ chunks all at once on the link and attribute that time to be $\alpha + n \cdot \beta \cdot s$. Using several measurements of time to transfer, we solve for $\alpha$ and $\beta$. For NDv2 systems we found that NVLink $\alpha$ and $\beta$ values are 0.7 us and 46 us/MB, and for InfiniBand, they are 1.7 us and 106 us/MB. This means that two 32 KB chunks sent together over the IB is 17% faster than when sent one after the other. However, chunks sent together can only be forwarded once the last chunk is received. Based on the $\alpha$-$\beta$ values, TACCL’s synthesizer determines if and when to send chunks together on a link.

### 2.2 Inferring multi-GPU topologies

To determine the PCIe topology of a VM, the profiler sends bandwidth and latency probes between the two CPUs and between pairs of GPUs. It answers the following questions:

- Which CPU is nearest to the NIC? We find this by the latency of loopback RDMA operations to each CPU.
- Which GPUs share a PCIe switch? We find all pairs of GPUs that get low bandwidth in a simultaneous copy to the CPU, indicating contention.
- Which GPUs share a PCIe switch with the NIC? We find which GPUs get low bandwidth in copies from the CPU closest to the NIC while it is doing an RDMA loopback copy between buffers on the CPU.

We first validate the profiler on Nvidia DGX-2 systems and then use it to find the unknown topology of NDv2 systems.

**Nvidia DGX-2** servers have 16 GPUs connected in a full mesh with NVLinks and NVSwitches (Figure 2c). There are 8x12.5 GBps Infiniband NICs, each shared with a pair of GPUs through a PCIe switch.

**Azure NDv2** has 8 GPUs connected with NVLink (Figure 2a) and one 12.5 GBps Infiniband NIC, which connects to a PCIe switch shared with two GPUs (Figure 2b). PCIe peer-to-peer communication (and thus GPUDirect RDMA [gpu, 2021]) is not enabled, meaning that all communication happen through buffers in CPU memory over potentially shared PCIe links. Further, virtualization obscures the true PCIe topology (all 8 GPUs and the NIC appear directly connected to one CPU) and NUMA node and GPU IDs are not assigned consistently from VM to VM. This means that, without additional information, software cannot avoid contention over shared PCIe links, creating interference and high variance in performance. Our physical topology profiler finds which GPUs do not share PCIe links with each other or with the NIC (Figure 2b) helping TACCL improve the performance of communication collectives.

### 3 Extracting Logical Topology

After determining the physical topology of the GPU system using the topology profiler (§2), TACCL extracts a logical topology that is encoded into the constraint solver. This is to create a simpler intermediate abstraction of the physical topology that is amenable to optimization by the synthe-
sizer using the idealized $\alpha$-$\beta$ cost model. Each connection embodies in a logical topology a set of physical links and switches. Logical connections can be enabled or disabled during algorithm synthesis.

3.1 Modeling Switches

In a switched fabric with full bisectional-bandwidth, such as the NVSwitch or IBSwitch fabrics in DGX-2 and NDv2 systems, nodes can simultaneously communicate at the full bandwidth of their ingress or egress links. However, as the number of flows through a switch, originating from a single GPU or NIC increases, the resulting queuing delays increase the latency. To account for this, TACCL allows fixing the number of simultaneous flows from a switched node by controlling the number of logical connections passing through the switch. Figure 3a shows a physical topology of three GPUs connected by a switch, where each GPU can communicate with any other GPU with a latency cost $\alpha$ and inverse bandwidth cost $\beta$. Figure 3b shows the logical topology that enables parallel connections between all pairs of GPUs. TACCL uses such logical topologies to generate algorithms for small chunk sizes since small chunk sizes lower the likelihood of congestion at the switch. Here each logical connection has half the bandwidth of the underlying link without any change in latency. In contrast, the logical topology in Figure 3c only enables a single connection from one GPU. This topology is useful for synthesizing algorithms for larger chunk sizes. Restricting the number of logical connections limits the congestion in the switch and allows TACCL to accurately model the latency and bandwidth of the underlying physical link.

3.2 Modeling Oversubscription

Our profiler reveals the inter-node architecture of NDv2 GPU systems. It identifies which pairs of GPUs share PCIe connections to the CPU through PCIe switches. Thus, the PCIe bandwidth to the CPU is oversubscribed by a factor of 2:1. Additionally, the IB NIC is connected to one of the PCIe switches, further oversubscribing the PCIe link to the CPU. This would not be a performance constraint had PCIe peer-to-peer communication and GPUDirect RDMA (gpu, 2021) been enabled on these machines, as it is on the DGX-1 and -2, allowing the NIC and adjacent GPUs to communicate directly. Since it is not, any communication between the GPU and network must first be copied to a buffer in the CPU’s memory. Thus, obtaining maximum throughput on the NDv2 systems requires scheduling data movement to avoid conflicting flows on the oversubscribed PCIe links. TACCL maximizes the inter-node bandwidth by dedicating one of the GPUs as a sender and another as a receiver. TACCL ensures that the sender GPU, the receiver GPU and the NIC are connected to three different PCIe switches to avoid any oversubscription. Additionally, TACCL allows the user to manually enable and disable logical connections. We use this capability to model the oversubscription of PCIe links to the CPU in NDv2 systems.

4 TACCL SYNTHESIZER

4.1 Problem formulation

GPUs participating in a communication collective partition their data into chunks, which are then scheduled by TACCL’s synthesizer. Given a communication collective, a logical topology with $\alpha$-$\beta$ costs and a chunk size, the synthesizer decides chunk transfer schedules across every link in the network, such that each chunk reaches its destination GPU as specified by the collective in the minimum time. TACCL formulates this as a mixed integer linear programming (MILP) problem that solves for binary decision variables that decide whether a chunk should be sent on a given link. It also finds the start time i.e., time when a chunk is available for transmission from a source GPU, and chunk send times from every GPU in the network. The chunk transfer schedules are subject to bandwidth and correctness constraints on the start and send times. The goal of the formulation is to minimize the total time of the chunk transfer schedule (full synthesizer formulation in Appendix A).

An important feature of the synthesizer is its ability to decide which chunks to transfer contiguously on a link. By sending $n$ chunks contiguously on a link, TACCL can increase the transfer size and reduce the total transfer time by $(n-1) \times \alpha$. However, this trades-off chunk pipelining, as all $n$ chunks only become available for subsequent sends at the receiver after every contiguously sent chunk has been received. The synthesizer formulation encodes this tradeoff and determines efficient contiguity for all chunk transfer along links. Since the $\alpha$ cost for NVLinks is much lower than IBs, we only allow chunk contiguity for IB transfers.

However, mixed integer linear programming problems are NP-hard. Moreover, to express bandwidth constraints, the synthesizer needs to determine the ordering of chunks over a link. Conditional to the chunk order, the synthesizer constrains the send time of a later chunk to not overlap with the send of a previous chunk. For $C$ chunks, the formulation has $O(C^2)$ booleans decision variables to determine the ordering for every link. As the number of nodes increase, the number of links increase linearly and the number of chunks involved in a collective increase linearly (ALLGATHER) or even quadratically (ALLTOALL). This combination of large problem size and computational hardness leads to infeasible solver time and memory requirements.

To solve this problem, we divide the synthesis into parts - first, the synthesizer solves an optimization problem to determine the path used by every chunk without fixing any ordering among chunks, then it heuristically orders the chunks
over every link, and finally, it solves another optimization problem to determine chunk contiguity. We elaborate on the three steps in the following.

**Step 1: Path encoding** determines the path of each chunk independent of other chunks without fixing the order of chunks. Chunks may be sent at the same time along a link and are not constrained by link bandwidth. Since chunk ordering is absent in path encoding stage, the number of booleans needed in the formulation reduces from $O(C^2)$ to $O(C)$ (constraints deciding if a chunk is sent) per link, reducing the encoding complexity. This encoding uses relaxed bandwidth constraints (Appendix A.1). We further scale the path encoding by constraining it to not allow a GPU to receive the same chunk more than once. Since we synthesize algorithms where each node is symmetrical to every other node, we add collective-specific symmetry constraints for intra-node chunk transfers. We also allow a chunk to only traverse a path in which the GPUs belong to any of the shortest paths from the chunk source to the destination.

**Step 2: Heuristic ordering** decides the order of chunks sent on a link. Since path encoding allows multiple chunks to have the same send time on a link, we order the sends of these chunks using scheduling heuristics like chunk-with-shortest-path-until-now-first and chunk-with-longest-path-from-now-first. However, the send order of a chunk over a link also determines its send time downstream along the chunk path, which is something the scheduling heuristics mentioned above fail to capture. To deal with this, we keep a running estimate of link time, which is the earliest time at which a chunk can be scheduled over the link and a running estimate of chunk time, which is the earliest time at which the next link transfer can be scheduled for the chunk. We decide chunk ordering based on the tracked link and chunk times along with the scheduling heuristics. Appendix A.2 provides details on the heuristic ordering.

**Step 3: Contiguity encoding** determines if chunks should be sent contiguously over a link or not and gives us the exact schedule of the link transfers. The path to be taken by the chunks and the ordering of chunks over links have already been determined at this point of time in the synthesizer. The job of the contiguity encoding is to determine when to trade-off chunk pipelining for latency gains due to chunk contiguity. Appendix A.3 explains the constraints in this encoding. If two chunks are ordered one after the other on a link, we either assign the first chunk to be sent before the second, or both the chunks to be contiguously. Using these three steps, TACCL’s synthesizer solves for an ALLGATHER for 8 NDv2 nodes in about 200s.

### 4.2 Synthesizer inputs

**Data partitioning.** The synthesizer takes as input the data partitioning parameter which determines the number of chunks a GPU partitions its data into. Inspecting the generated algorithms indicates that more data partitions often allow the synthesizer to utilize otherwise unutilized links (see Appendix C for more details). On the other hand, too many partitions increase the latency cost of transfer and also add complexity to synthesizer.

**Solver inclination.** By default, TACCL does not fix the number of parallel connections for NVSwitch when creating a logical topology to optimize for. Instead, it uses the solver in the path encoding to automatically control the enabling/disabling of logical connections using the concept of **solver inclination**. We incline our synthesizer to either produce algorithms that maximize the number of unique connections between the switched GPUs, known as uc-max, or that minimize the number of unique connections between switched GPUs, known as uc-min. We do this by adding the number of unique NVSwitch connections to the objective function in the path encoding. The uc-max configuration inclines the synthesizer to produce algorithms that maximize link sharing while at the same time minimizing the algorithm time. This configuration performs best for small buffer sizes. The uc-min configuration inclines the synthesizer to produce algorithms that minimize link sharing while also minimizing the algorithm time. This configuration works well when the buffer size is large.

### 4.3 Synthesizing combining collectives

We synthesize combining collectives (i.e., collectives that combine chunks like REDUCESCATTER and ALLREDUCE) by using the non-combining collectives, similar to the tech-
nique use by SCCL (Cai et al., 2021). REDUCESSCATTER can be implemented as an inverse ALLGATHER - a send from a source GPU in ALLGATHER is instead received and reduced on the source GPU. However, simply inverting the sends does not work - a GPU may do simultaneous sends on different links in an ALLGATHER, but it cannot reduce all receives together in the inverse case. We thus order the inverse sends using heuristic ordering followed by contiguity encoding in order to synthesize REDUCESSCATTER. ALLREDUCE can be synthesized directly by concatenating REDUCESSCATTER with an ALLGATHER algorithm.

5 Backend

The synthesizer described above generates an abstract algorithm that specifies the order in which the nodes communicate the various chunks. The goal of the backend is to implement this abstract algorithm. To do so, we extend NCCL (NVIDIA NCCL) with an interpreter which we call TACCL runtime\(^1\). While any communication algorithm can be trivially implemented using NCCL’s point-to-point sends and receives, TACCL runtime enables us to execute the entire algorithm in a single kernel launch, eliminating multiple launch overheads. In addition, by reusing NCCL transport mechanisms, TACCL runtime is able to support all of NCCL’s communication backends such as IB, Ethernet, NVLink, and PCIe.

5.1 TACCL runtime

The input to TACCL runtime is an TACCL-EF program, which is an XML format for representing collective algorithms. TACCL-EF programs operate on three buffers: input, output and scratch. For each buffer, the program specifies the number of chunks it will be sliced into such that all chunks are equal size. Every step of the algorithm is expressed in terms of these chunks.

The program is divided into a set of GPU programs made up of threadblocks. Each threadblock is made up of a series of steps that are executed sequentially, with each step specifying an instruction and operands as indices into the input/output/scratch buffers. The current instruction set includes sends, receives (with optional reduction), and local copies. To simplify the implementation of TACCL runtime, each threadblock can send to and receive from at most one GPU. Additionally, threadblocks within a GPU can synchronize by indicating that one step depends on another step, which will cause the interpreter to wait until the dependency has completed before executing the dependent step.

The TACCL runtime extends NCCL and it is backward compatible with its API. Therefore, integrating TACCL runtime into training/inference frameworks such as PyTorch is a single line change wherein that change swaps the third-party NCCL library for TACCL runtime. This allows TACCL to dynamically swap in collective algorithms generated for any training/inference workload using torch.distributed.

5.2 Lowering to TACCL runtime

To target TACCL-EF, abstract algorithms are lowered to the executable format. The sets of sends operating on abstract chunks that comprise the steps of the algorithm are transformed into pairs of send and receive operations operating on concrete buffer indices. Furthermore, these operations are placed sequentially into threadblocks and any necessary dependencies recorded between them.

**Buffer allocation** Chunks are allocated indices in the input, output and scratch buffers based on whether the rank is their source, destination or neither. For chunks that are both input and output (e.g. as in ALLGATHER) a local copy to the output buffer is performed at the end.

**Instruction generation** The operations of the abstract algorithm are split into two instructions for the sender and receiver GPU, and chunks are translated into buffer references and indices according to the buffer allocation. At this point instructions are still grouped by their global steps.

**Dependency insertion** To transform the global time step of TACCL and SCCL synthesized algorithms into the asynchronous execution model of TACCL-EF, dependencies are added to ensure that all possible executions respect the data dependencies present in the abstract algorithm. Dependencies are tracked for each buffer index separately. Both sends (i.e. reads) and receives (i.e. writes) depend on the latest write to the buffer index. Additionally, receives depend on all the reads that happened after the latest write.

This approach was inspired by how the happens-before relation is tracked in Fig. 3 in (Saarikivi et al., 2012) — reads synchronizing with only the latest write allows them to be concurrent, reducing unnecessary synchronization.

**Threadblock allocation** Instructions are grouped by their time step in the abstract algorithm, the remote GPU they interact with, and whether they are sends or receives. Each of these groups are allocated a threadblock that will execute them such that (i) no two groups of the same time step have the same threadblock, and (ii) each threadblock has at most one peer for sending and at most one for receiving.

**Instances** The number of concurrent threadblocks in the TACCL runtime effectively limits the peak bandwidth of the algorithm. The TACCL runtime can improve this by creating \(n\) parallel instances of the algorithm. Chunks are divided

---

\(^1\)TACCL runtime code can be publicly accessed here: [link removed for double-blind purposes]
into \( n \) subchunks that follow the same path as the parent chunk but execute in parallel to increase the bandwidth of the algorithm. Section 6.2 explores the performance implications of different choices of \( n \).

6 Evaluation

In this section, we evaluate the algorithms obtained by TACCL for ALLGATHER, ALLTOALL, and ALLREDUCE collectives on clusters of NVIDIA DGX-2 and Azure NDv2 hardware. We use algorithm bandwidth (NCCL Tests), which is a measure of throughput obtained by dividing the input buffer size with the time taken by an algorithm, for performance comparisons. We compare TACCL algorithms against NCCL (v.2.8.4-1) as well as implementations of hierarchical algorithms. The hierarchical algorithms involve three phases, a local communication, a cross-node communication, and then a local communication. Next, we evaluate the performance of TACCL synthesized algorithms by changing the TACCL inputs like chunk size, number of logical inter-node connections, synthesizer inclination, and number of instances. We limit our comparison to 32 GPUs, i.e., 2 DGX-2 nodes or up to 4 NDv2 nodes. Finally, we provide end-to-end training speedup results for a large mixture of experts model when using algorithms generated by TACCL.

6.1 Standalone experiments

ALLGATHER (a) DGX-2. Figure 4 shows the algorithm bandwidth for ALLGATHER algorithms on a 2-node NVIDIA DGX-2 for varying buffer sizes. We synthesize a set of algorithms by varying the inputs to TACCL— we set chunk sizes as 1 KB, 32 KB, and 1 MB, fix the number of inter-node links to one per IB card, and vary the synthesizer inclination and number of instances. We plot the maximum algorithm bandwidth achieved for each buffer size from the algorithms. TACCL generates better ALLGATHER algorithms than NCCL for almost all buffer sizes. For the small buffer size regime ranging from 1 KB to 1 MB, TACCL synthesizes algorithms that are up to \( 4 \times \) faster than NCCL. In the moderate buffer size regime of 2 MB to 128 MB, TACCL-synthesized algorithms perform similar or slightly better than NCCL. In the large buffer size regime from 256 MB to 1 GB, TACCL synthesizes algorithms that nearly saturate the inter-node bandwidth, resulting in up to 25% faster ALLGATHER on 32 DGX-2 GPUs.

The hierarchical ALLGATHER algorithm consists of an all-pair ALLGATHER within a node, cross-node transfer of data from GPU \( i \) of each node to GPU \( i \) of every other node, and local all-pair broadcast of chunks received from the other nodes. Our implementation of the hierarchical algorithm is up to 26% faster than NCCL for small to moderate buffer sizes. TACCL-generated algorithms perform better than the hierarchical algorithm for all buffer sizes.

(b) NDv2. Figure 5 (i) shows the algorithm bandwidth for ALLGATHER algorithms run on 2-node Azure NDv2 for varying buffer sizes. The TACCL plot is generated by taking the best from a set of TACCL-synthesized algorithms for each buffer size. The set of algorithms is generated by varying the inputs to the TACCL synthesizer - we vary the chunk size similar to previously mentioned in DGX-2 experiment, fix the number of internode links to one per IB card, and vary the number of instances used by the TACCL runtime. TACCL can generate similar or better performing ALLGATHER algorithms than NCCL for all buffer sizes.

For 2 nodes, at smaller buffer sizes, TACCL synthesizes algorithms that are up to 23% faster than NCCL. In the moderate and large size regime, as the buffer size increases, the performance improvement of TACCL algorithms increases, reaching a \( 3.4 \times \) higher algorithm bandwidth than NCCL for the largest buffer size of 1 GB. The performance improvement at larger buffer sizes is because TACCL-generated algorithms can better saturate the inter-node bandwidth by modeling the number of outgoing IB connections and by reducing the sharing of PCIe for inter-node transfers as discussed in Section 3.

The hierarchical algorithm for NDv2 nodes is similar to the one for DGX-2 nodes, except that it uses a single outgoing IB connection to reduce the sharing of PCIe for inter-node transfers. Hence, for moderate to large buffer sizes greater than 1 MB, the hierarchical algorithm is faster than NCCL, having up to \( 2.8 \times \) faster algorithm bandwidth than NCCL at 1 GB. Even so, the algorithms synthesized by TACCL are up to 50% faster than the hierarchical algorithm due better pipelining of intra-node and inter-node transfers.

For 4 nodes, as shown in Figure 7b (i) in the Appendix, TACCL algorithms are up to \( 2 \times \) better than NCCL for ALLGATHER involving 4 NDv2 nodes.

ALLTOALL (a) DGX-2. Figure 7a shows the algorithm bandwidth for ALLTOALL algorithms on a 2-node NVIDIA DGX-2 for varying buffer sizes. We synthesize a set of algorithms by varying the inputs to TACCL— we choose either one or two inter-node links per IB card (unlike in ALLGATHER), and vary the synthesizer inclination between uc-min and uc-max. We plot the maximum algorithm bandwidth for each buffer size from these algorithms. TACCL generates better ALLTOALL algorithms than NCCL for small and large buffer size regimes. TACCL-synthesized algorithms are up to 55% faster than NCCL for small buffer sizes ranging from 1 KB to 16 KB and up to 11% faster than NCCL for large buffer sizes ranging from 4 MB to 1 GB. For moderate buffer sizes however, TACCL algorithms are slower than NCCL, by up to 14%. For small sizes, TACCL algorithms perform better than NCCL due to less number of channel instances, which reduces the latency cost. For
large sizes, TACCL algorithms perform slightly better than NCCL due to coalescing of chunks sent in inter-node transfer which reduces the latency of transfer, thereby slightly reducing the total algorithm time.

We implement a hierarchical ALLTOALL algorithm that consists of three phases - local multi-rooted Gather within a node, cross-node communication of data from GPU $i$ of each node to GPU $i$ of every other node, and local multi-rooted Scatter of chunks received from other nodes. Due to the high chunk granularity required for a multi-rooted phase, the hierarchical algorithm performs worse than NCCL.

(b) NDv2. Figure 5 (ii) shows the algorithm bandwidth for ALLTOALL algorithms on 2-node Azure NDv2 for varying buffer sizes. The TACCL plot takes the best from a set of TACCL-synthesized algorithms for each buffer size. The set of algorithms is generated by varying the inputs to the TACCL synthesizer - we fix the number of internode links to one per IB card and vary the number of instances used by the TACCL runtime. TACCL generates up to 66% better performing ALLTOALL algorithms than NCCL for moderate to large buffer sizes greater than 1 MB for 2 NDv2 nodes. For buffer sizes smaller than 1 MB, it is better to use NCCL which is 13% - 78% faster than TACCL algorithms.

The hierarchical ALLTOALL algorithm for NDv2 nodes is similar to the one for DGX-2 nodes, except that it uses a single-root Gather and Scatter for the first and last phase of the algorithm to reduce the sharing of PCIe for inter-node transfers. Due to this design, it is 23% - 64% faster than NCCL for moderate to large buffer sizes. Even so, the algorithms synthesized by TACCL are up to 14% faster than the hierarchical algorithm due better pipelining of intranode and inter-node transfers.

As the number of nodes increases, TACCL’s performance improvement reduces, TACCL algorithms are still up to
46% faster than NCCL for buffer size greater than 1 MB for 4 NDv2 nodes as shown in Figure 7b (ii).

Allreduce Figure 5 (iii) shows the performance of TACCL algorithms on 2 node NDv2. We evaluate Allreduce algorithms synthesized by TACCL and run using 1 and 8 instances. For 2 NDv2 nodes, single instance TACCL Allreduce outperforms NCCL by up to 37%, for buffer sizes of up to 1 MB. For buffer sizes larger than 1 MB, TACCL Allreduce algorithm run using 8 instances outperforms NCCL by 1.3x - 2.7x. We also design a hierarchical algorithm for Allreduce that locally reduces chunks within a node, performs a cross-node reduction, and then locally broadcasts the reduced chunks. This is similar to the multi-node Allreduce protocol suggested in Blink (Wang et al., 2020). We make use of the same logical topology used by TACCL - a single outgoing IB connection and reduce reduced PCIe sharing for inter-node transfers. 

Changing transfer cost using chunk size Another input to the synthesizer is the \( \alpha - \beta \) cost model that depends on a chunk size input. Using this, the synthesizer determines the latency and bandwidth costs of transfers as \( \alpha \) and \( \beta \times \text{chunk}_\text{size} \) respectively. We analyze how changing the chunk size input to the synthesizer affects the performance of the synthesized algorithm. Figure 6b shows the performance of Allgather algorithm at three different chunk sizes (1 KB, 32 KB, and 1 MB) that were synthesized with three cost models using chunk size inputs (1 KB, 32 KB, and 1 MB). Note, that the chunk size input only affects the synthesizer’s cost model and is not necessarily the chunk size of the input data.

Changing logical topology One of the inputs to the TACCL synthesizer is a logical topology in which we fix the IB connections between nodes. Figure 6a shows the algorithm bandwidth of Allgather obtained by varying the number of IB connections for a fixed chunk size of 1 KB, 32 KB, and 1 MB. We fix the solver inclination input to uc-max for these experiments and feed in chunk size 1 KB, 32 KB, and 1 MB for each of the subplots. For small 1 KB chunk size which corresponds to a 32 KB buffer size for 2-node DGX-2 Allgather, we see that the algorithm that uses 8 IB connections per NIC performs better than algorithms using fewer connections. As the chunk size increases to 32 KB (buffer size 1 MB) and 1 MB (buffer size 32 MB), the optimal number of IB connections per NIC reduces to 4 and 1 respectively. This is because the benefits of link sharing reduces as the chunk size increases and \( \beta \)-cost starts dominating over the \( \alpha \)-cost.

Changing data partitioning Figure 6c shows the algorithm bandwidth of algorithms generated by partitioning data on each GPU into a single chunk or into two chunks. We fix the synthesizer chunk size to 1 MB for both experiments, set the solver inclination to uc-min, and fix number of instances to 8. At large buffer sizes, the algorithm generated for two data chunks utilizes bandwidth better as compared to the algorithm generated for a single data chunk per GPU.

Changing number of instances Figure 6e shows the algorithm bandwidth of algorithms generated by varying the number of IB connections per NIC with instances ranging from 1 to 8 for different buffer sizes. Increasing the number of instances improves bandwidth utilization — multiple threadblocks seem to be needed to keep the six NVLinks in a V100 busy. However, a larger
number of threadblocks also increases latency, which we suspect is due to unfavorable scheduling of synchronization related memory operations onto the NVLinks at the start of each send. Since latency cost dominates for small buffer sizes, using a large number of instances only increases the latency cost. As the buffer size increases, the bandwidth improvements due to more instances become predominant. Since solver inclination and number of instances have a similar relation with chunk sizes, we always run uc-max algorithms with a single instance and uc-min algorithms with 8 instances.

6.3 Synthesis time

TACCL takes about 1s to generate ALLGATHER, 48s to generate ALLTOALL, and about 2s to generate ALLREDUCE for 32 GPUs in NDv2 systems. To understand synthesis time, we also synthesized an ALLGATHER for 80 GPUs (10 nodes) in 8 minutes. It takes about 41s to generate ALLGATHER and 125s to generate ALLTOALL for 32 GPUs on a DGX-2 system. The synthesis time for ALLTOALL for different chunk sizes varies with some configurations taking more time, but we limit synthesis time for all algorithms to 30 minutes. Given the scale of jobs for both inference and training, we believe these synthesis times are reasonable.

We evaluated the publicly available version of SCCL (Cai et al., 2021; Microsoft SCCL) on topologies of NDv2 nodes and DGX2 nodes. We modified the codebase to include both topologies and attempted to synthesize ALLGATHER and ALLTOALL collectives using SCCL’s pareto-optimal solver strategy. We set a 24 hour time limit for each synthesis query. For both ALLGATHER and ALLTOALL, SCCL was not able to finish synthesis for two machines with either the NDv2 or DGX2 nodes. The pareto-optimal strategy in SCCL is such that latency optimal algorithms are found first, followed by increasingly bandwidth optimal algorithms. In 24 hours SCCL was only able to find the latency optimal algorithm for ALLGATHER on two NDv2 nodes and no further algorithms after that.

6.4 End-to-end training

We evaluated TACCL on end-to-end training for an internal workload in a large enterprise company on two NDv2 nodes which requires ALLTOALL and ALLREDUCE collective primitives. The model is implemented in PyTorch and all communication happens through torch.distributed and as explained in Section 5, utilizing TACCL algorithms is quite straightforward. The ALLTOALL and ALLREDUCE sizes that were required for this model are ≈ 6MB and ≈ 256MB, respectively. Given TACCL improvement for these primitives on NDv2 hardware, the throughput of this model was improved by 17% end-to-end.

7 RELATED WORK

The MPI standard provides a set of collective communication algorithms that enable efficient distributed computations of interconnected nodes (Dongarra et al., 2013). The HPC community has focused on the efficient implementation of these MPI collective algorithms (Pješivac-Grbović et al., 2007; Thakur et al., 2005) and demonstrated how to build optimized algorithms for specific interconnects, like mesh, hypercube, or fat-tree (Scott, 1991; Bokhari & Berryman, 1992; Barnett et al., 1993). In contrast to TACCL, these prior works assume homogeneous interconnects and are often only focused on bandwidth optimality.

There are hybrid algorithms which (at least for mesh net-
works) provide optimized implementations of collectives for various input sizes. These approaches first build bandwidth and latency optimal algorithms and then to optimize for input size, generate a hybrid which switches between the bandwidth and latency optimal algorithms along each dimension of a mesh network (Chan et al., 2007; Barnett et al., 1993). In contrast, TACCL generates algorithms for various input sizes for general networks.

As discussed earlier, NCCL (NVIDIA NCCL) is a GPU to GPU implementation of a subset of the standard MPI collectives, optimized for NVLINK and Infiniband interconnects. While NCCL uses the topology of GPU connections and NIC placement along with buffer size to decide between two main types of communication algorithms — Ring and Tree, it is agnostic to the exact performance profile of the links, and thus (as we show) is often multiple times slower than TACCL’s topology aware collectives.

There are also hierarchical approaches to implement collectives (Cho et al., 2019; Sergeev & Balso, 2018; Luo et al., 2020; Wang et al., 2020). For example, Horovod (Sergeev & Balso, 2018) implements an ALLREDUCE by a local ReduceScatter, a global ALLREDUCE, and then a local ALLGATHER. These methods do not search over possible algorithms, but instead pick from a known set of decompositions. One interesting idea for future work is to consider that such a decomposition might help synthesis based techniques scale as they break a large collective into a series of smaller ones. However, as we demonstrate, TACCL’s heuristics enable our synthesis to scale, despite lacking such decomposition.

Lastly, recent works Blink (Wang et al., 2020) and Plink (Luo et al., 2020) specialize algorithms for the underlying topology. Blink uses a heuristic spanning-tree packing algorithm to maximize bandwidth utilization within a node and a hierarchical approach across. Blink has good performance over NCCL in the case when NCCL cannot create rings spanning all GPUs inside a node. TACCL, on the other hand, outperforms NCCL when using the entire node of GPUs. Plink constructs a logical topology based on bandwidth and latency probes of the physical topology to avoid oversubscribed and congested links and searches for a reasonable clustering of nodes for a two-level hierarchical reduction strategy. Plink builds that hierarchical reduction from known primitives and does not search over the space of possible algorithms.

8 Conclusion

TACCL is a topology and input-size aware collective communication library for multi-node distributed machine learning training and inference. TACCL synthesizes efficient collective algorithms using a scalable by-parts synthesizer. The algorithms thus generated are up-to 2.7× faster than the state-of-the-art NCCL, and result in 17% faster end-to-end training time.

References

GPUDirect

RDMA, 2021. https://developer.nvidia.com/gpudirect.

Azure ND-series. Azure ND-series, 2021. https://docs.microsoft.com/en-us/azure/virtual-machines/nd-series.

Barnett, M., Littlefield, R., Payne, D. G., and van de Geijn, R. Global combine on mesh architectures with wormhole routing. In [1993] Proceedings Seventh International Parallel Processing Symposium, pp. 156–162. IEEE, 1993.

Bokhari, S. H. and Berryman, H. Complete exchange on a circuit switched mesh. In 1992 Proceedings Scalable High Performance Computing Conference, pp. 300–301. IEEE Computer Society, 1992.

Cai, Z., Liu, Z., Maleki, S., Musuvathi, M., Mytkowicz, T., Nelson, J., and Saarikivi, O. Synthesizing optimal collective algorithms. In Proceedings of the 26th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, pp. 62–75, 2021.

Chan, E., Heimlich, M., Purkayastha, A., and Van De Geijn, R. Collective communication: theory, practice, and experience. Concurrency and Computation: Practice and Experience, 19(13):1749–1783, 2007.

Cho, M., Finkler, U., Serrano, M., Kung, D., and Hunter, H. Blueconnect: Decomposing all-reduce for deep learning on heterogeneous network hierarchy. IBM Journal of Research and Development, 63(6):1:1–1:11, 2019.

Dongarra, J. et al. MPI: A message-passing interface standard version 3.0. High Performance Computing Center Stuttgart (HLRS), 2(5):32, 2013.

Fedus, W., Zoph, B., and Shazeer, N. Switch transformers: Scaling to trillion parameter models with simple and efficient sparsity. CoRR, abs/2101.03961, 2021. URL https://arxiv.org/abs/2101.03961.

Hockney, R. W. The communication challenge for mpp: Intel paragon and meiko cs-2. Parallel Computing, 20(3):389–398, 1994. ISSN 0167-8191. doi: https://doi.org/10.1016/S0167-8191(94)80015-8. URL https://www.sciencedirect.com/science/article/pii/S0167819106800219.

Lepikhin, D., Lee, H., Xu, Y., Chen, D., Firat, O., Huang, Y., Krikun, M., Shazeer, N., and Chen, Z. Gshard: Scaling giant models with conditional computation and automatic sharding. CoRR, abs/2006.16668, 2020. URL https://arxiv.org/abs/2006.16668.
Luo, L., West, P., Nelson, J., Krishnamurthy, A., and Ceze, L. Plink: Discovering and exploiting locality for accelerated distributed training on the public cloud. In Proceedings of Machine Learning and Systems 2020, pp. 82–97. 2020.

Microsoft SCCL. Microsoft sccl, 2021. https://github.com/microsoft/sccl.

MT-NLG. Using deepspeed and megatron to train megatron-turing nlg 530b, the world’s largest and most powerful generative language model. https://www.microsoft.com/en-us/research/blog/using-deepspeed-and-megatron-to-train-megatron-turing-nlg-530b-the-worlds-largest-and-most-powerful-generative-language-model/. Accessed October 2021.

NCCL Tests. Nccl tests, 2021. https://github.com/NVIDIA/nccl-tests.

Nvidia Infiniband. Nvidia InfiniBand, 2021. https://www.nvidia.com/en-us/networking/infiniband-adapters/.

NVIDIA NCCL. Nvidia nccl, 2021. https://github.com/NVIDIA/nccl.

Nvidia NVLink. Nvidia NVLink and NVSwitch, 2021. https://www.nvidia.com/en-us/data-center/nvlink/.

Nvidia NVSWITCH. NVIDIA NVSWITCH The World’s Highest-Bandwidth On-Node Switch , 2021. https://images.nvidia.com/content/pdf/nvswitch-technical-overview.pdf.

Pješivac-Grbović, J., Angskun, T., Bosilca, G., Fagg, G. E., Gabriel, E., and Dongarra, J. J. Performance analysis of mpi collective operations. Cluster Computing, 10(2):127–143, 2007.

Saarikivi, O., Kähkönen, K., and Heljanko, K. Improving dynamic partial order reductions for concolic testing. In 2012 12th International Conference on Application of Concurrency to System Design, pp. 132–141, 2012. doi: 10.1109/ACSD.2012.18.

Scott, D. S. Efficient all-to-all communication patterns in hypercube and mesh topologies. In The Sixth Distributed Memory Computing Conference, 1991. Proceedings. pp. 398–399. IEEE Computer Society, 1991.

Sergeev, A. and Balso, M. D. Horovod: fast and easy distributed deep learning in tensorflow, 2018.

Shoeybi, M., Patwary, M., Puri, R., LeGresley, P., Casper, J., and Catanzaro, B. Megatron-LM: Training multi-billion parameter language models using model parallelism. CoRR, abs/1909.08053, 2019. URL http://arxiv.org/abs/1909.08053.

Thakur, R., Rabenseifner, R., and Gropp, W. Optimization of collective communication operations in mpich. The International Journal of High Performance Computing Applications, 19(1):49–66, 2005.

Wang, G., Venkataraman, S., Panishayee, A., Devanur, N., Thelin, J., and Stoica, I. Blink: Fast and generic collectives for distributed ml. In Dhillon, I., Papailiopoulos, D., and Sze, V. (eds.), Proceedings of Machine Learning and Systems, volume 2, pp. 172–186, 2020. URL https://proceedings.mlsys.org/paper/2020/file/43ec517d68b6edd3015b3edc9a11367b-Paper.pdf.

A TACCL SYNTHESIZER IN DETAIL

Formulation 1 gives a non-exhaustive overview of the MILP problem. start and send times are continuous variables whereas sent, before, and together are booleans. R is the number of GPUs in the topology, and C is the total number of chunks to be transferred. \( \text{start}[c, r] \) is the time at which chunk \( c \) becomes available at GPU \( r \). \( \text{send}[c, s, r] \) is the time at which chunk \( c \) is sent from GPU \( s \) to GPU \( r \). \( \text{sent}[c, s, r] \) represents whether a chunk \( c \) is sent from GPU \( s \) to GPU \( r \). \( \text{before}[c, o, r] \) represents whether chunk \( c \) is sent to GPU \( r \) before chunk \( o \) is sent, both form the same source GPU. \( \text{together}[c, o, r] \) represents whether chunks \( c \) and \( o \) are sent to GPU \( r \) together from the same source, thus sharing the bandwidth and reducing the latency cost of transfer. The collective precondition, \( \text{coll}. \text{precondition} \), is the set of all start GPUs for every chunk taking part in the collective. \( \{ (c, r) \mid \text{chunk } c \text{ starts on GPU } r \} \).

The collective postcondition, \( \text{coll}. \text{postcondition} \), is the set of all final destination GPUs for every chunk taking part in the collective. \( \{ (c, r) \mid \text{chunk } c \text{ ends up on GPU } r \} \).

A.1 Path encoding

The main aim of the path encoding is to give us the path that every chunk takes. It does not respect bandwidth constraints of any link - the generated solution may send two chunks simultaneously over a link at the time cost of one chunk. It does however ensure correctness constraints, for example, that chunks are sent only after they are received. The path encoding assumes that no chunk is sent contiguously with another and does not use before and together variables. Instead of bandwidth constraints, this encoding uses relaxed bandwidth constraints shown in Formulation 2. They are expressed by aggregating the link transfer time of all chunks sent over a link and using it to lower bound the total time of the algorithm (eq. 1). For switched connections,
We start the heuristic ordering by determining the paths each chunk takes using the solution of the path encoding. We then consider the first link in every path as a candidate for scheduling a chunk transfer. Using heuristics like chunk-with-shortest-path-until-now-first and chunk-with-longest-path-from-now-first, we select a path (and thus a chunk) which should be scheduled in this round. We keep a running estimate of link time, which is the earliest time at which a chunk can be scheduled over the link. We also keep a running estimate of chunk time, which is the earliest time at which the next link transfer can be scheduled for a chunk. At the start, the link time for every link is 0 and the chunk time for every chunk is 0. When a path is chosen in the first round, the chunks associated with the path are scheduled to traverse the first link in the path. The link time of that link increases by link latency and chunk time of that chunk increases by link latency. The link candidate from the selected path is also updated to be the next link in the path. For the next rounds, we decide which path’s candidate link to schedule next using the tracked link and chunk times along with the scheduling heuristics. This keeps going until we have scheduled a data transfer over all the links in all the paths.

A.2 Ordering heuristics

We start the heuristic ordering by determining the paths each chunk takes using the solution of the path encoding. We then consider the first link in every path as a candidate for scheduling a chunk transfer. Using heuristics like chunk-with-shortest-path-until-now-first and chunk-with-longest-path-from-now-first, we select a path (and thus a chunk) which should be scheduled in this round. We keep a running estimate of link time, which is the earliest time at which a chunk can be scheduled over the link. We also keep a running estimate of chunk time, which is the earliest time at which the next link transfer can be scheduled for a chunk. At the start, the link time for every link is 0 and the chunk time for every chunk is 0. When a path is chosen in the first round, the chunks associated with the path are scheduled to traverse the first link in the path. The link time of that link increases by link latency and chunk time of that chunk increases by link latency. The link candidate from the selected path is also updated to be the next link in the path. For the next rounds, we decide which path’s candidate link to schedule next using the tracked link and chunk times along with the scheduling heuristics. This keeps going until we have scheduled a data transfer over all the links in all the paths.
Synthesizing Collective Communication Algorithms for Heterogeneous Networks with TACCL

Formulation 3 Contiguity encoding

Input: alpha cost $\alpha_{src,r}$, beta cost $\beta_{src,r}$ collective coll, is_sent($C,R,R$), order over link lkOrder($R,R$), send/recv order for switch swtSendOrder($R$), swtRecvOrder($R$)

Variables: time, start($C,R$), send($C,R,R$), before($C,R,R$) (boolean), together($C,R,R$) (boolean)

Objective: Minimize time

for all ($src,r$) $\in$ topo.edges do
  for i $\leftarrow$ 1 to len(lkOrder[$src,r$]) do
    for j $\leftarrow$ i + 1 to len(lkOrder[$src,r$]) do
      c = lkOrder[$src,r$][i]
      o = lkOrder[$src,r$][j]
      $\alpha_{prev} = lkOrder[src,r][j - 1]$
      Ordering constraints:
      before[c,o,r] = 0
      before[c,o,r] + together[c,o,r] = 1
      together[c,o,r] $\leq$ together[c,o,prev,r]

for all r $\in$ topo.switch.sources do
  for i $\leftarrow$ 1 to len(swtSendOrder[$r$]) do
    for j $\leftarrow$ i + 1 to len(swtSendOrder[$r$]) do
      allow_together = True
      c, dst$_c$ = swtSendOrder[$r$][i]
      o, dst$_o$ = swtSendOrder[$r$][j]
      for k $\leftarrow$ i + 1 to j do
        $\alpha_{prev}$, dst$_{prev} = swtSendOrder[r][k]$
        if dst$_{prev}$ = dst$_o$ then
          allow_together = False
          if allow_together then
            before[c,o,r] = 1

// Similarly for swtRecvOrder

GATHER, ALLTOALL, and ALLREDUCE on 4-node NDv2 clusters.

C ANALYSIS OF SYNTHESIZED ALGORITHM

In this section, we discuss the novel algorithm synthesized by TACCL for ALLGATHER on 2 NVIDIA DGX-2 nodes. It outperforms NCCL by up to 25% at large buffer sizes and almost saturates the inter-node network bandwidth.

Every two GPUs in a 16-GPU DGX-2 node share a PCIe switch which is connected to the NIC. We generate a logical topology in which only one of the two GPUs in the pair performs inter-node sends and the other performs inter-node receives over the IB. Figure 8 shows the physical and logical topology used for the synthesis. For simplicity, we only show 4 GPUs per node. We also ignore the $\alpha$-cost of the links in our analysis below for simplicity. This is acceptable because at large buffer sizes, the $\beta$-cost anyway dominates over the $\alpha$-cost. We assume 1 MB chunk size, set solver inclination to uc-min, and set number of instances to 8. Since only every other GPU in a DGX-2 node can receive chunks over the IB (according to our logical topology), we decide to partition GPU data into two chunks. Intuitively, this will lead to a more efficient link utilization since it allows chunks received from other nodes to be distributed to the GPUs that only send to other nodes. This is exactly what happens in the algorithm synthesized by TACCL, as we explain in the following paragraph.

The generated algorithm can roughly be divided into 4 parts, also shown in Figure 9:

1) A local ring-based Allgather is performed for the chunks present in each node. The time taken is $(n - 1) \times \beta_{NV} \times$ num_chunks_per_GPU, or $15 \times 8 \times 2 = 240$ us. Parallely, the algorithm performs an inter-node transfer of both chunks present at each sender GPU. The time taken for this is $\beta_{IB} \times$ num_chunks, or $107 \times 2 = 214$ us. The total time taken in this step is the maximum of the local and inter-node transfers, i.e., , 240 us.

2) Next, one out of the two chunks received at each GPU from the inter-node send is sent to their corresponding sender GPUs in time $\beta_{NV}$, or 8 us, followed by a ring-based Allgather of the chunks within the node which takes $(n - 1) \times \beta_{NV} \times$ num_chunks_per_GPU, or $15 \times 8 \times 1 = 120$ us. Parallely, the algorithm performs an inter-node transfer of one chunk with a precondition at the corresponding receiver GPU, time for which is $\beta_{IB} \times$ num_chunks, or $107 \times 1 = 107$ us. The total time taken in this step is thus 128 us.

3) Next, the chunks obtained from the inter-node transfer in step 2 are Allgather’ed in a ring-based algorithm, where only alternate GPUs have a data chunk to transfer. The time for this is $15 \times 8 \times 1 = 120$ us. Parallely, the algorithm performs a final inter-node transfer of the single remaining chunk with a precondition at the corresponding receiver GPU. The time for that is $107 \times 1 = 107$ us. The total time taken in this step is thus 120 us.

4) Finally, the last chunks obtained from the inter-node transfer in step 3 are Allgather’ed in a ring-based algorithm, taking time 120 us.

All in all, the partitioning the data into two chunks allows chunks to be distributed to the remaining GPUs and increases link utilization. By profiling the inter- and intra-node links and using them to solve the contiguity encoding, we are able to generate an ALLGATHER algorithm that reaches 95% of the network bandwidth.
Synthesizing Collective Communication Algorithms for Heterogeneous Networks with TACCL

Figure 7. Algorithm bandwidth and speedup over NCCL of TACCL, NCCL, and hierarchical algorithm on various collectives and hardware.

Figure 8. Topologies of 2 NVIDIA DGX-2 nodes.
Figure 9. The four steps of an \textsc{AllGather} algorithm generated by TACCL for 2 NVIDIA DGX-2 nodes. Each GPU has 2 chunks in the start which are shown right below the GPU. Mentioned under every step in the figure is a set of chunks that every GPU in a node has after the completion of that step.