Abstract
In this paper, we explored the opportunity to enhance power grid robustness after routing stage, and propose a linear programming based algorithm that maximizes the improvement of power grid strengthening with given available routing resource. We further discussed some techniques to leverage trade-offs between runtime and optimality of the solutions. Experimental results show substantial power integrity improvement with “zero cost”.

Keywords — linear programming, power grid, runtime complexity

1. Introduction
In modern digital circuit design, frequency is increasing constantly, power density is increasing drastically, while routing resource does not scale the same way [1]. Thus power grid design has been increasingly challenging since more routing resource need to be saved for signal routing. Power integrity (mainly IR drop and electromigration, i.e. EM) has become extremely difficult to close [2]. In this paper, we propose a post-route power grid enhancement methodology that leverage the existing no-used routing resource to strengthen the power grid to achieve power integrity sign-off quality.

2. Motivation
When timing is closed for a given design, there is no need to utilize any of the open routing space anymore [3]. However, these open spaces can be used to strengthen power grid weakness for “zero cost” [4]. Figure 1 illustrates a potential example, how an open space can help improve power integrity of the design.

Fig 1. Using open space to share current

In Figure 1, an instance is power hungry and is drawing large current that causes IR drop hotspot [5]. By utilizing the open space, we manage to share current from the two adjacent parallel power wires and resolve the hotspot issue [6]. Using this mechanism, it can also help to significantly reduce impact from variations [7][8], especially for critical designs [9]. EM-sensitive wires can also benefits from this operations [10]. In the next Section 3, we will discuss the details of applying a linear programming (LP) based algorithm to optimize the power grid strengthening methodology; in Section 4, we will discuss a few techniques to trade-off between optimality and...
3. LP-Based Power Grid Enhancement
When using open space, we noticed that there will be potential conflict and competing between two different power wires. Figure 2 illustrates such an example.

Vias are critical to power grid integrity as well as reliability [12]. To optimize the number of wires and vias added to share power supply current, we formulated the problem into a binary linear programming algorithm [13]. The main constraints are coming from via spacing. Equation set (1) defines the problem formulation.

$$\text{maximize} \quad y = \sum_{i=1}^{m} \sum_{j=1}^{n} x_{i,j}$$

subject to

$$x_{i,j} + x_{i+1,j} \leq 1, i \in \{1,2,...,m\}, j \in \{1,2,...,n\}$$

$$x_{i,j} \in \{0,1\}$$

(1)

In Figure 2, when the horizontal center wire is added, the wires above and below will lose its resource, since the via to via spacing design-rule-check (DRC) prevents a via to be created for those wires [11].

Vias are critical to power grid integrity as well as reliability [12]. To optimize the number of wires added to share power supply current, we formulated the problem into a binary linear programming algorithm [13]. The main constraints are coming from via spacing. Equation set (1) defines the problem formulation.

where $i$ is the row index and $j$ is the column index, $x_{i,j}$ is the potential via candidate at location $(i,j)$, $y$ is the total number of vias to be added. There are various numerical solvers to calculate binary linear programming results. However, runtime complexity is a concern, we will discuss technique to speed up the runtime performance in Section 4.

4. Trade-Off Technique
In Section 3, we discussed the binary linear programming algorithm to maximize the chances of adding current sharing wires. It should be noted that binary linear programming is a NP-hard problem, and cannot be efficiently solved within polynomial runtime [14]. Even with efficient numerical computation packages in Python or Matlab, runtime is not desirable. To overcome this issue, we propose to split the whole design into separate partitions [15]. Figure 3 illustrates how a break is introduced to split the design and decompose the problem into smaller sub-problems.

Since the runtime exponentially increases with the number of potential via candidates, by artificially split the design into smaller areas, we cut down the problem sizes. The optimality loss from this technique is small, equation (2) gives the bound of the heuristic solutions using this technique.

$$y' \geq y^* - k \times m$$

(2)

where $k$ is the number of break lines introduced, $m$ is the number of rows in the design, $y^*$ is the
optimal solution, and \( y' \) is the suboptimal solution derived using our heuristic technique.

![Fig 3. Break lines for partitioning design](image)

5. Experiments
We used one block from the open source design or1200_fpu_arith [16] as our benchmark testcases. The logical synthesis is done using Synopsis Design Compiler [17] and physical synthesis is done using Synopsis ICC2 [18]. Sign-off extraction is done using Synopsis Star-RC [19] and power integrity checks are run using Apache RedHawks [20]. Temperature effects are also taken into account [21]. Worst case current is estimated using [22]. Table 1 shows the results of applying our proposed power grid enhancement algorithm.

It can be observed that using our approach of 10 partition LP, we are able to improve the power integrity by 6.0% compared to reference and runtime by 62.6% compared to optimal LP. If we use 100 partition LP, we can achieve 2.1% worst case power integrity improvement and 87.8% runtime improvement compared to optimal LP.

6. Conclusions
In this paper we discuss opportunities to enhance power grid after timing closure. By leveraging the open space available, we were able to improve the power integrity significantly with “zero cost”. We propose the binary linear programming algorithm to optimize the power grid enhancement result. Given the NP-hard property of binary linear programming algorithm, we proposed a decompose technique to split and reduce problem

| Table 1. Comparison between sign-off and DFS checks |
|-----------------------------------------------|
| reference | optimal LP | 10 partition LP | 100 partition LP |
|-----------|------------|-----------------|------------------|
| # vias added | N/A | 105.6k | 100.1k | 76.4k |
| voltage drop avg (mV) | 35.6 | 30.8 | 31.2 | 34.1 |
| voltage drop worst (mV) | 66.7 | 62.7 | 63.2 | 65.3 |
| runtime (hrs) | N/A | 12.3 | 4.6 | 1.5 |
size. The split approach greatly reduces the runtime with little loss of optimality.

References
[1] V. Adhinarayanan, I. Paul, J. L. Greathouse, W. Huang, A. Pattnaik and W. c. Feng, "Measuring and modeling on-chip interconnect power on real hardware," 2016 IEEE International Symposium on Workload Characterization (IISWC), Providence, RI, 2016, pp. 1-11.
[2] R. Reis. Circuit Design for Reliability, Springer, New York, 2015.
[3] Pei-Ci Wu, M. D. F. Wong, I. Nedelchev, S. Bhardwaj and V. Parkhe, "On timing closure: Buffer insertion for hold-violation removal," 2014 51st ACM/EDAC/IEEE Design Automation Conference (DAC), San Francisco, CA, 2014, pp. 1-6.
[4] D. A. Li, M. Marek-Sadowska and S. R. Nassif, "A Method for Improving Power Grid Resilience to Electromigration-Caused via Failures," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 1, pp. 118-130, Jan. 2015.
[5] Yu Zhong and M. D. F. Wong, "Fast algorithms for IR drop analysis in large power grid," ICCAD-2005. IEEE/ACM International Conference on Computer-Aided Design, 2005., 2005, pp. 351-357.
[6] L. Kong, Zhang Jin, Qiu Zhijie and Meng Jinlei, "Research and measurement of chip current imbalance in IGBT module with multiple chips in parallel," 2013 International Conference on Electrical Machines and Systems (ICEMS), Busan, 2013, pp. 1851-1856.
[7] D. Li, et al. Variation-aware electromigration analysis of power/ground networks. Proceedings of the International Conference on Computer-Aided Design, 2011.
[8] D. Li, et al. “Layout Aware Electromigration Analysis of Power/Ground Networks”. Circuit Design for Reliability, 2015.
[9] Q. Wang, et al. Research on phase locked loop based on DSP and CPLD. Mechanical & Electrical Engineering Magazine, 2007.
[10] D. Li, et al. On-chip em-sensitive interconnect structures. Proceedings of the international workshop on system level interconnect prediction, 2010.
[11] Y. H. Su and Y. W. Chang, "VCR: Simultaneous via-template and cut-template-aware routing for directed self-assembly technology," 2016 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), Austin, TX, 2016, pp. 1-8.
[12] F. Chen et al., "Investigation of emerging middle-of-line poly gate-to-diffusion contact reliability issues," 2012 IEEE International Reliability Physics Symposium (IRPS), Anaheim, CA, 2012, pp. 6A. 4.1-6A.4.9.
[13] https://en.wikipedia.org/wiki/Integer_programming
[14] https://en.wikipedia.org/wiki/NP/List_of_NP-complete_problems
[15] https://en.wikipedia.org/wiki/divdeconquer/Divide_and_conquer_algorithm
[16] https://github.com/openrisc/or1200
[17] https://www.synopsys.com/support/training/rtl-synthesis/design-compiler-rtl-synthesis.html
[18] https://www.synopsys.com/implementation-and-signoff/physical-implementation/ic-compiler-ii.html
[19] https://www.synopsys.com/implementation-and-signoff/signoff/starcc.html
[20] https://www.apache-da.com/products/redhawk/redhawk-resources
[21] D. A. Li, M. Marek-Sadowska and S. R. Nassif, "T-VEMA: A Temperature- and Variation-Aware Electromigration Power Grid Analysis Tool," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 10, pp. 2327-2331, Oct. 2015.
[22] D. Li and M. Marek-Sadowska, "Estimating true worst currents for power grid electromigration analysis," Fifteenth International Symposium on Quality Electronic Design, Santa Clara, CA, 2014, pp. 708-714.