Insights into Cold Source MOSFETs with Sub-60 mV/decade and Negative Differential Resistance Effect

Yiheng Yin†, Zhaofu Zhang‡ *, Chen Shao†, John Robertson†‡ and Yuzheng Guo† *

† School of Electrical and Automation, Wuhan University, Wuhan, Hubei 430072, China
‡ Department of Engineering, University of Cambridge, Cambridge, CB2 1PZ, United Kingdom

Abstract: To extend the Moore’s law in the 5 nm node, a large number of two dimensional (2D) materials and devices have been thoroughly researched, among which the “cold” metals 2H MS₂ (M = Nb, Ta) with unique band structures are expected to achieve the sub-60 mV/dec subthreshold swing (SS). The studied “cold” metal field-effect transistors (CM-FETs) based on the “cold” metals are capable to fulfill the high-performance (HP) and low-dissipation (LP) goals simultaneously, as required by the International Technology Roadmap for Semiconductors (ITRS). Moreover, gaps of “cold” metals also enable the CM-FETs to realize negative differential resistance (NDR) effect. Owing to the wide transmission path in the broken gap structure of NbS₂/MoS₂ heterojunction, the recording 4110 μA/μm peak current, several orders of magnitude higher than the tunneling current of the Esaki diode, is achieved by NbS₂/MoS₂ CM-FET. The largest peak-valley ratio (PVR) 1.1 × 10⁶ is obtained by TaS₂/MoS₂ CM-FET with \( V_{GS} = -1 \) V at room temperature. Our results claim that the superior on-state current, SS, cut-off frequency and NDR effect can be obtained by CM-FETs simultaneously. The
study of CM-FETs provides a practicable solution for state-of-the-art logic device in sub
5 nm node for both more Moore roadmap and more than Moore roadmap applications.

**Keywords:** “cold” metals, CM-FET, sub-60 mV/dec SS, negative differential resistance, peak-valley ratio

1. INTRODUCTION

The Moore’s law now faces the bottleneck due to the short channel effect of Si-based metal-oxide-semiconductor field effect transistors (MOSFET).\[1-2\] Considering the prospect of integrated circuits (ICs), two main technology roadmaps have been put forward by the industry field, namely more Moore roadmap and more than Moore roadmap.\[3-4\] The more Moore roadmap aims to pursue the device scaling complying with the Moore’s law,\[3\] while the more than Moore technology focuses on improving the functionality of ICs, such as combining digital electronics with devices such as radio frequency (RF), power devices and sensors.\[4\] In the more Moore field, unlike the obvious thickness-dependent mobility of Si and Ge channels, two dimensional (2D) materials not only have atomically thin channel thickness which is beneficial for the gate control, but also maintain promising carrier mobility.\[5-8\] Previous works have proven that devices using 2D materials are capable to fulfill the International Technology Roadmap for Semiconductors (ITRS) requirements\[9\] even with nanometer-scale gate length.\[10-15\] Recently, the transistor channel length has already scaled down to 5 nm node.\[16\] How to further decrease the power consumption and sustain the Moore’s law is a task of top
priority. Various novel transistors such as Fin filed-effect-transistors (FinFETs),\textsuperscript{[17]} fully depleted silicon on insulator (FDSOI) transistors,\textsuperscript{[18]} tunneling FET (TFETs)\textsuperscript{[19-20]} and negative capacitance (NC) transistors\textsuperscript{[21-22]} have been put forward. Apart from novel device configurations, looking for new materials is an alternative approach to sustain the Moore’s law. Recently, cold-source FETs (CS-FETs) have been proposed to achieve sub-60 mV/dec subthreshold swing (SS), which can be realized by using materials with desired density of state (DOS) such as Dirac materials\textsuperscript{[23]}, appropriately doped semiconductors\textsuperscript{[24-25]} and materials with gaps near the Fermi level ($\varepsilon_F$).\textsuperscript{[26]} Compared with the complex heterostructure fabricated by Dirac source materials or appropriately doped semiconductors, the “cold” metal 2H MS$_2$ (M = Nb, Ta) with gaps close to the $\varepsilon_F$, equivalent to a naturally p-doped or n-doped semiconductor, would be an ideal solution to fulfill the steep slope of SS.\textsuperscript{[26]} The unique band structure allows the “cold” metal MOSFET (CM-FET) to filter the transmission of high-energy carriers in the subthreshold region and reach sub-60 mV/dec SS.\textsuperscript{[23]} Another cornerstone is that the “cold” metal monolayer 2H NbS$_2$ and TaS$_2$ have been successfully synthesized\textsuperscript{[27-28]} and served as the injection source in the heterojunction transistors,\textsuperscript{[29]} which solidifies the way for the research of “cold” metal heterojunctions and transistors.

In this work, we conduct a comprehensive electronic and transport calculation of “cold” metals (NbS$_2$ and TaS$_2$) and their devices with transition metal dichalcogenide (TMD) channels. The SS of CM-FETs successfully breakthrough the 60 mV/dec thermionic limit.
at room temperature. In terms of more Moore field (to extend the Moore’s law), CM-FETs are capable to fulfill the on-state current, power consumption and cut-off frequency \( (f_T) \) requirements of both ITRS high performance (HP) and low dissipation (LP) goals. Apart from the favorable performance against ITRS goals, the CM-FETs with unique band structures of “cold” metals can successfully achieve the negative differential resistance (NDR) effect, which is expected to fulfill the multifunctional ICs in the more than Moore field. Owing to the wide transmission path in the broken gap characters of MS\textsubscript{2}/MoS\textsubscript{2} heterojunctions, the peak current is several orders of magnitude higher than the typical tunneling current of Esaki diode,\textsuperscript{[30-31]} whose operation principle is shown in Figure S1. The benchmarking 4110 \( \mu \)A/\( \mu \)m peak current and \( 1.1 \times 10^6 \) peak-valley ratio (PVR) are achieved by NbS\textsubscript{2}/MoS\textsubscript{2} and TaS\textsubscript{2}/MoS\textsubscript{2} CM-FETs, respectively. The results claim that the superior \( I_{on}, SS, f_T \) and NDR effect are obtained by our CM-FETs simultaneously, which provides a feasible method for the development of state-of-the-art logic devices beyond the Moore’s law.

2. RESULTS

2.1 The performance of CM-FETs against the ITRS goals

In the more Moore domain, we only focus on whether the transistors can satisfy the ITRS goals and extend the Moore’s law. The calculated lattice constants of monolayer 2H NbS\textsubscript{2} and TaS\textsubscript{2} are \( a_1 = 3.36 \) Å and \( a_2 = 3.31 \) Å respectively, which is in agreement with previous results.\textsuperscript{[29,32]} The band structures and DOS of 2H NbS\textsubscript{2} and TaS\textsubscript{2} are shown
in Figure 1. Energy gaps occur above \(E_{CG}\) and below \(E_{VG}\) the \(\varepsilon_F\) of “cold” metals. The NbS\(_2\) and TaS\(_2\) can thus be considered as heavily p-doped or n-doped semiconductors and used as the injection source of a transistor. Considering the DOS between the \(\varepsilon_F\) and \(E_{VG}\) is higher than the DOS above the \(\varepsilon_F\), the “cold” metal is more suitable to serve as the source electrode in a p-type transistor. Previous work presented that MX\(_2\) CM-FETs with 10 nm gate length have successfully reached the sub-60 mV/dec SS at room temperature.\(^{[26]}\) To illustrate the mechanism of superior SS, schematic energy band diagram comparisons of the p-type conventional MOSFET and CM-FET in off-state are shown in Figure 1(c, d).
The SS is defined as

$$SS = \frac{dV_{GS}}{d(\log I_{DS})} = \ln 10 \left( \frac{k_BT}{q} \right) \left( \frac{C_{OX} + C_S}{C_{OX}} \right)$$

where $V_{GS}$ is voltage applied between gate and source electrodes. $I_{DS}$ is the drain-source current. $k_B$ and $T$ are the Boltzmann constant and temperature, respectively. $q$ is the electronic charge. $C_{OX}$ and $C_S$ are the oxide capacitance and semiconductor capacitance, respectively. The thermionic limit of 60 mV/decade is owing to the constant term $\ln 10 \left( \frac{k_BT}{q} \right) \approx 60$. Because carriers in the source have an energy distribution complying to the Fermi-Dirac distribution $f(E)$.[33] The energy distribution of carriers is defined as $n(E) = g(E)f(E)$, where $g(E)$ is the DOS distribution as a function of energy. Based on Eq. (1), the SS is proportional with $T$. With the decreasing of $T$, the $f(E)$ around the Fermi level becomes sharp, leading to the sub-60 mV/dec SS. Similarly, unlike the $n(E)$ of normal source having a long thermal tail, the thermal tail of “cold” metal source below $\varepsilon_S$ is filtered by the $g(E)$ around $E_{VG}$.[23] The $n(E)$ of “cold” metal source, steeper than the $f(E)$, decreases super-exponentially with the decreasing of energy, which allows the CM-FET to achieve the sub-60 mV/dec SS. Meanwhile, electrons localized around the $\varepsilon_S$ permit a large on-state current. The schematic energy band diagrams of the CM-FET
corresponding to the on-state and the off-state are shown in Figure S2. As the transistor channel length scales down, it is of interest to investigate whether the superior SS can be maintained in the sub-5 nm node CM-FETs.

Figure 2. (a) The schematic view of top contact MS₂/TMDs CM-FET. (b-e) I-V curves of CM-FETs and p-doped TMD MOSFETs. SS of each I-V curve is labelled in (b-e). The blue lines labelled in (b-e) represent the SS of 60 mV/dec.

The schematic view of MS₂/TMDs CM-FET and the corresponding I-V curves are
shown in Figure 2. The source and drain electrodes are modelled by “cold” metal and p-doped TMD materials, respectively, with the heterojunction of “cold” metal and TMD materials is shown in Figure S3. The p-type doping concentration of source is $3 \times 10^{13}$ cm$^{-2}$. Considering the top contact configuration in Figure 2a is more feasible than the edge contact configuration shown in Figure S4, we only calculate the performance of top contact CM-FETs in the next sections. I-V curves and performance benchmark of edge contact CM-FETs are shown in Figure S4 and Figure S5, respectively. The current of device is calculated by the Landauer–Büttiker formula,$^{[34]}

$$I = \frac{2e}{h} \int_{-\infty}^{+\infty} \{T(E)[f_s(E - \varepsilon_S) - f_D(E - \varepsilon_D)]\} dE$$

(2)

where $T(E)$ is the transmission coefficient, $f_s$ and $f_D$ are the Fermi-Dirac distribution functions for source and drain electrodes, $\varepsilon_S$ and $\varepsilon_D$ are the Fermi levels of source and drain electrodes, respectively. On-state current ($I_{on}$) is obtained by the corresponding on-state gate voltage ($V_{GS(on)}$). The $V_{GS(on)}$ is defined as $V_{GS(on)} = V_{GS(off)} + V_{DS}$, where $V_{GS(off)}$ is the off-state gate voltage defined by ITRS standards in 2013.$^{[9]}$ $V_{DS}$ is the bias voltage applied between the source and drain electrodes, fixed at 0.64 V in our work. It is observed that SS of CM-FETs significantly outperforms that of heavily p-doped TMD MOSFETs. Among these studied CM-FETs, NbS$_2$ CM-FETs exhibit lower SS because of the $E_{VG}$ close to the $\varepsilon_F$, while TaS$_2$ CM-FETs deliver larger currents owing to the wide transmission path between the $E_{VG}$ and $\varepsilon_F$ as shown in Figure 1b. The most favorable SS (45 mV/dec) and $I_{on}$ (2643 $\mu$A/µm) achieved by NbS$_2$/MoSe$_2$ and
TaS$_2$/ MoS$_2$ CM-FETs respectively prove the above analysis. The top contact CM-FETs with smaller SS and $I_{on}$ than that of edge contact CM-FETs (data shown in Figure S4 and Figure S5) indicates that barriers of top contact devices interacted by the van der Waals force is higher than that of edge contact configurations. So, with the extreme low SS, the CMFET proposed in this work can fully sustain the more Moore roadmap in the 5nm nodes.
Figure 3. Benchmark of $I_{on}$ and SS of top contact CM-FETs for (a) HP goal and (b) LP goal, respectively. The other data are extracted from the arsenene,[35] antimonene,[35] BP,[36] Te,[37] GeSe,[38] silicane,[39] AsP,[40] Si nanowire (NW)[41] and carbon nanotube (CNT).[42] (c) The $f_T$ and PDP of CM-FETs compare with ITRS goals. The $I_{on}$ of ITRS HP and LP is set to 900 $\mu$A/$\mu$m and 295 $\mu$A/$\mu$m, respectively. The ITRS PDP is set as 0.24 fJ/$\mu$m.

To present a panoramic performance analysis of CM-FETs in 5 nm node, $I_{on}$ and SS of our work compared with previous results are shown in Figure 3. The $I_{on}$ of CM-FETs
ranges from 693 μA/μm to 2643 μA/μm and TaS2/MoS2 CM-FET with largest $I_{on}$ is about three times higher than that of ITRS HP goals. The $I_{on}$ performance is only inferior to the monolayer arsenene and antimonene MOSFETs ($I_{on}$ of 3200 μA/μm and 2980 μA/μm, respectively) and comparable with the black phosphorus (BP) MOSFET with 1994 μA/μm $I_{on}$. As is known, the BP is limited to the poor air-stability.\[43]\] The superior $I_{on}$ of arsenene and antimonene MOSFETs benefits from the ideal heavily doped source/drain electrodes which can get rid of the influence of contact resistance.\[35]\] As for SS, the performance of CM-FETs is overall superior to previous results in Figure 3. Especially, the NbS2/MoSe2 and TaS2/MoSe2 CM-FETs even achieve the low SS of 45 and 47 mV/dec, respectively at room temperature. In Figure 3c we plot the power dissipation (PDP) and cut-off frequency ($f_T$). PDP is a decisive parameter for low dissipation applications, defined as $PDP = V_{DS}(Q_{on} - Q_{off})/w$, where $Q_{on}$ and $Q_{off}$ are the total charge of the channel in on-state and off-state, respectively. $w$ is the channel width. The PDP values of CM-FETs vary from 0.144 to 0.197 fJ/um, obviously lower than the ITRS requirement of 0.24 fJ/um, showing a desired gate control capability. $f_T$ is a relevant factor for radio frequency devices, obtained by $f_T = g_m / (2\pi C_G)$, where $g_m$ is the transconductance of MOSFETs, defined as $g_m = I_{DS}/V_{GS}$. $C_G$ is the gate capacitance, defined as $C_G = \partial Q_{ch} / \partial V_{GS}$, where $Q_{ch}$ is the charge in gate electrode region. All CM-FETs $f_T$ in Figure 3c reach the THz level, indicating that our CM-FETs are competent to be applied into radio frequency circuits.\[44]\] Hence, the air-stability and
excellent performance totally strengthen the competitive advantage of CM-FETs among these low-dimensional material MOSFETs as listed in Figure 3.

To better understand the mechanism of extreme low (sub-60 mV/dec) SS achieved by the CM-FETs, we take the NbS$_2$/MoSe$_2$ CM-FET as an example to plot the projected local density of states (PLDOS) in Figure 4. The SS ranges from 45 mV/dec to 59 mV/dec with $V_{GS}$ increasing form -0.2 V to 0 V in Figure 4a. The PLDOS in Figure 4b and 4c represents the switching process of the device. At $V_{GS} = -0.2$ V, the $\Phi_B$ is small. Thermal emission current can directly transport through the channel region. With the increasing of $V_{GS}$, $\Phi_B$ and $E_{VG}$ are overlapped. Therefore, the current is only tunneling around the top of $E_{VG}$, so the transmission efficiency, $T(E)$, around the $\epsilon_S$ decreases rapidly compared with its counterpart in Figure 4b.

![Figure 4](image)

**Figure 4.** (a) The SS of NbS$_2$/MoSe$_2$ CM-FET as a function of $V_{GS}$. (b, c) Projected local density of states of NbS$_2$/MoSe$_2$ CM-FET with the barrier ($\Phi_B$) (b) above ($V_{GS} = -0.2$ V) and (f) below ($V_{GS} = 0$ V) the $E_{VG}$ of source.

### 2.2 The NDR effect of CM-FETs
Figure 5. (a, b) The I-V curves of NbS$_2$/MoS$_2$ and TaS$_2$/MoS$_2$ CM-FETs. PVR labelled in (a, b) is the ratio of the peak current and valley current. (c) Energy band diagrams under different bias voltages ($V_{DS}$) at $V_{GS} = -1$ V. The pink areas in (c) represent gaps of NbS$_2$/MoS$_2$ heterojunction. The $\epsilon_S$ and $\epsilon_D$ are the Fermi level of source and drain, respectively. The width of red arrows represents the magnitude of currents.

Apart from the superior $I_{on}$ and SS, CM-FETs are also capable to realize the NDR effect, which can be used in the analog circuits and is desirable for the multi-valued logic (MVL) system.$^{[45]}$ Based on the PLDOS in Figure 4, the “cold” metal source can form the type-III band alignment with the heavily p-doped MoS$_2$. I-V curves of NbS$_2$/MoS$_2$ and TaS$_2$/MoS$_2$ CM-FETs under various $V_{GS}$ are shown in Figure 5. Results claim that the NbS$_2$/MoS$_2$ CM-FET tends to deliver a large peak current from 1791 µA/µm to 4110 µA/µm, while the large peak-valley ratio (PVR) is readily to be obtained by the TaS$_2$/MoS$_2$ CM-FET with the detailed values labelled in Figure 5. The NbS$_2$/MoS$_2$
CM-FET fulfills the largest peak current 4110 μA/μm at $V_{GS} = -2V$. The largest PVR of $1.1 \times 10^6$ is achieved by the TaS$_2$/MoS$_2$ CM-FET at $V_{GS} = -1V$, several orders of magnitude higher than the mainstream reports which will be discussed later. It is noteworthy that the $V_{GS}$ plays an important role in controlling the peak current and peak-valley ratio (PVR). The peak current varies inversely with the $V_{GS}$, while the PVR is proportional with the $V_{GS}$.

We plot the energy band diagrams at $V_{GS} = -1V$ in Figure 5c to analyze the NDR mechanism in the NbS$_2$/MoS$_2$ CM-FET. The I-IV in Figure 5c represent the energy band diagrams under various bias voltages ($V_{DS}$). Notably, unlike the conventional type-III band alignment NDR device with a narrow transmission path between the broken gap,[45-46] the wide transmission path, as shown in Figure S6, allows the CM-FET to achieve a large current, which is desirable for the extremely high PVR. Considering the $\varepsilon_S$ is already tuned to the valence band maximum (VBM) of MoS$_2$ with 0.2 V $V_{DS}$, the current reaches the peak point. With the increasing of $V_{DS}$, the current comes to the valley point, because the transmission is blocked by the overlapped gaps of NbS$_2$ and MoS$_2$. As the $V_{DS}$ further increases, the current starts to rise with a transmission path appearing below the VBM of MoS$_2$. It can be concluded that the width of energy window between the $\varepsilon_D$ and VBM of MoS$_2$ is a key factor for the peak current. Considering lower $V_{GS}$ corresponds to a wider transmission path as shown in Figure S7, the peak current is inversely proportional with the $V_{GS}$. In terms of the PVR, with the decreasing of $V_{GS}$, a
larger $V_{DS}$ is needed to shift the gap of MoS$_2$ and reach valley point. The $\varepsilon_D$ in valley point is even close to the VBM of NbS$_2$, which leads to more efficient transmission through the VBM of MoS$_2$ and a larger valley current. Hence, the PVR is proportional with the $V_{GS}$.

**Figure 6.** (a) I-V curves of the NbS$_2$/MoS$_2$ CM-FET at various temperature from 100 K to 300 K. (b) Enlarged views of I-V curves at peak point and valley point under different temperature. $I_{\text{peak}}$ and $I_{\text{valley}}$ represent the peak current and the valley current. (c) The PVR as a function of temperature from 100 K to 300 K. (d, e) The transmission spectrum of NbS$_2$/MoS$_2$ MOSFET at peak point and valley point, respectively. The $\varepsilon_S$ and $\varepsilon_D$ are the Fermi level of NbS$_2$ and MoS$_2$, respectively. The magnitude of $T(E)$ indicates the transmission efficiency of carriers. (f) Fermi-Dirac distribution at different temperature.

Furthermore, to analyze the relationship between temperature and NDR effect, I-V curves of NbS$_2$/MoS$_2$ CM-FET with $V_{GS} = -1$V at various temperature are shown in Figure 6. The corresponding analysis of TaS$_2$/MoS$_2$ CM-FET is shown in Figure S7. Encouragingly, the NDR effect is improved with the decreasing of temperature. As temperature decreases in Figure 6b, the peak current increases, while the valley current decreases. Consequently, the PVR(peak current) increases from 549(989 $\mu$A/$\mu$m) to 2.3
$\times 10^6 (1070 \, \mu \text{A/} \mu \text{m})$ with temperature decreasing from $300 \, \text{K}$ to $100 \, \text{K}$. Based on Eq. (2), the current is mainly contributed by transmission between the $\varepsilon_S$ and $\varepsilon_D$ of device. As temperature decreases in Figure 6f, the Fermi-Dirac distribution near the $\varepsilon_F$ becomes sharp. Thus, the weight of current contributed by the transmission between $\varepsilon_S$ and $\varepsilon_D$ is even higher, while the weight of transmission below the $\varepsilon_S$ and above the $\varepsilon_D$ becomes lower. In terms of peak current in Figure 6d, there is large $T(E)$ around the $\varepsilon_S$. On the contrary, the $T(E)$ of valley current between $\varepsilon_S$ and $\varepsilon_D$ is really flat. As a result, the valley current is proportional with the temperature and peak current varies inversely with the temperature. These results claim that the NDR performance of NbS$_2$/MoS$_2$ CM-FET is immune to the temperature oscillation, which enables the NbS$_2$/MoS$_2$ CM-FET adapt to more complex working environment.

Apart from the temperature effect, PVR and peak current are regarded as two decisive factors for practical applications. The NDR performance of NbS$_2$/MoS$_2$ and TaS$_2$/MoS$_2$ CM-FETs compared with previous results is summarized in Figure 7. To deliver a fair comparison, the device width is normalized to $10 \, \mu \text{m}$ for both our devices and data from previous reports. The PVR of NbS$_2$/MoS$_2$ CM-FET is only inferior to the MoS$_2$/WSe$_2$ and BP/Al$_2$O$_3$/BP heterojunction NDR devices. However, the poor air-stability of BP and the small peak current of MoS$_2$/WSe$_2$ NDR device hinder their practical application. Compared with previous results superior in either PVR or peak current, the NDR devices in our work are fully capable to achieve both large PVR and peak current simultaneously.
Especially, the peak currents in this work are several orders of magnitude higher than previous results. The large peak current not only improves the noise margin ability of NDR devices and relevant circuits, but also increases the output power and enhances the stability of oscillation circuits. With the large peak current and PVR, NbS$_2$/MoS$_2$ and TaS$_2$/MoS$_2$ CM-FETs are suitable for the MVL system and multifunctional device in more than Moore field.

![Benchmark of PVR as a function of peak current. Other data are extracted from the BP/ReS$_2$, MoS$_2$/WSe$_2$, Si/Ge, BP/SnSe$_2$, BP/Al$_2$O$_3$/BP, Carbon quantum well, WSe$_2$/MoSe$_2$, Gra/BN/Gra and Gra/WSe$_2$/Gra NDR devices. The blue and red oval marks represent the performance variation of NbS$_2$ and TaS$_2$ CM-FETs, respectively.](image)

3. CONCLUSIONS

In summary, we present a comprehensive electronic and transport calculation of nanoscale CM-FETs based on the “cold” metal NbS$_2$ and TaS$_2$ heterojunctions. The $I_{on}$ of CM-FETs with 5 nm channel length can achieve ITRS HP and LP goals simultaneously
to further sustain the more Moore roadmap, which are rarely fulfilled in previous calculations because of the contradictory requirements of HP (high drain current) and LP (small SS). The dilemma is successfully solved by the superior switching performance of “cold” metals and the favorable mobility of 2D TMDs. The extreme low SS of 45 and 47 mV/dec is obtained for NbS$_2$/MoSe$_2$ and TaS$_2$/MoSe$_2$ CM-FETs, respectively. In terms of NDR effect in more than Moore field, our results claim that the large peak current and PVR can be both achieved by NbS$_2$/MoS$_2$ and TaS$_2$/MoS$_2$ CM-FETs, owing to the wide broken gap feature, which is an obstacle of the Esaki diode. We find that the peak currents and PVR can be effectively controlled by the gate voltage and immune to the temperature influence. The recording 4110 $\mu$A/$\mu$m peak current and $1.1 \times 10^6$ PVR are achieved by NbS$_2$/MoS$_2$ and TaS$_2$/MoS$_2$ CM-FETs, respectively. The results prove that “cold” metal materials are competitive candidates for multifunctional logic devices and can be employed into the MVL system and radiofrequency circuits.

4. METHODOLOGY

We calculated the electronic and transport properties of “cold” metal MS$_2$ and their devices with TMD channels based on density functional theory (DFT) and non-equilibrium Green function (NEGF) with Atomsitis Tool Kit 2020 package.$^{[54]}$ The exchange correlation was the Perdew-Burke-Ernzerhof (PBE) functional of generalized gradient approximation (GGA). All simulations are conducted with the Pseudo Dojo pseudopotential and DFT-D3 van der Waals correction.$^{[55]}$ A 80-Hartree cut-off energy
was adopted. Monkhorst-Pack grids used for the transport calculation sampling the $8 \times 1 \times 163$ k point meshes. To avoid the interaction from adjacent layers, a 30 Å vacuum was applied to the device for transport calculations. The other basic settings refer to our previous work.[56-58]

**AUTHOR INFORMATION**

**Corresponding Author**

* E-mail: vguo@whu.edu.cn

* E-mail: zz389@cam.ac.uk

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

**ACKNOWLEDGMENTS**

This work is supported by Wuhan University. Authors acknowledge the financial support from the Fundamental Research Funds for the Central Universities, and the funding from EPSRC grant EP/P005152/1. The numerical calculations in this work is conducted on the supercomputing system in the Supercomputing Center of Wuhan University.

**Conflict of Interest**

The authors declare no conflict of interest

**Reference**

[1] R. Chau, B. Doyle, S. Datta, J. Kavalieros, K. Zhang, *Nat. Mater.* 2007, 6, 810.

[2] Y. Lv, W. Qin, C. Wang, L. Liao, X. Liu, *Adv. Electron. Mater.* 2019, 5, 1800569.
[3] M. Badaroglu, K. Ng, M. Salmani, S. Kim, G. Klimeck, C.-P. Chang, C. Cheung, Y. Fukuzaki, "More Moore Landscape for System Readiness-ITRS2. 0 Requirements", presented at 2014 IEEE 32nd International Conference on Computer Design (ICCD), 2014.

[4] W. Arden, M. Brillonü, P. Cogez, M. Graef, B. Huizing, R. Mahnkopf, More-than-Moore White Paper. https://www.seas.upenn.edu/~ese570/spring2015/IRC-ITRS-MtM-v2%203.pdf, accessed: August, 2014.

[5] D. Akinwande, C. Huyghebaert, C.-H. Wang, M. I. Serna, S. Goossens, L.-J. Li, H.-S. P. Wong, F. H. Koppens, Nature 2019, 573, 507.

[6] Y. Liu, X. Duan, H.-J. Shin, S. Park, Y. Huang, X. Duan, Nature 2021, 591, 43.

[7] Y. Liu, X. Duan, Y. Huang, X. Duan, Chem. Soc. Rev. 2018, 47, 6388.

[8] C. Song, G. Noh, T. S. Kim, M. Kang, H. Song, A. Ham, M.-k. Jo, S. Cho, H.-J. Chai, S. R. Cho, ACS Nano 2020, 14, 16266.

[9] International Technology Roadmap for Semiconductors (2013 edition), http://www.itrs2.net/2013-itrs.html, accessed: August, 2013.

[10] A. D. Franklin, M. Luisier, S.-J. Han, G. Tulevski, C. M. Breslin, L. Gignac, M. S. Lundstrom, W. Haensch, Nano Lett. 2012, 12, 758.

[11] A. M. Hammam, M. E. Schmidt, M. Muruganathan, S. Suzuki, H. Mizuta, Carbon 2018, 126, 588.

[12] A. Nourbakhsh, A. Zubair, R. N. Sajjad, A. Tavakkoli KG, W. Chen, S. Fang, X. Ling, J. Kong, M. S. Dresselhaus, E. Kaxiras, Nano Lett. 2016, 16, 7798.

[13] K. Xu, D. Chen, F. Yang, Z. Wang, L. Yin, F. Wang, R. Cheng, K. Liu, J. Xiong, Q. Liu, Nano Lett. 2017, 17, 1065.

[14] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, H. Dai, Phys. Rev. Lett. 2008, 100, 206803.

[15] R. Quhe, L. Xu, S. Liu, C. Yang, Y. Wang, H. Li, J. Yang, Q. Li, B. Shi, Y. Li, Physics Reports 2021.

[16] G. Yeap, S. Lin, Y. Chen, H. Shang, P. Wang, H. Lin, Y. Peng, J. Sheu, M. Wang, X. Chen, "5 nm CMOS Production Technology Platform Featuring Full-Fledged EUV, and High Mobility Channel FinFETs with Densest 0.021 μm 2 SRAM Cells for Mobile SoC and High Performance Computing Applications", presented at 2019 IEEE International Electron Devices Meeting (IEDM), 2019.

[17] D. Hisamoto, W. C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. J. King, J. Bokor, C. M. Hu, IEEE Trans. Electron Devices 2000, 47, 2320.

[18] R. Carter, J. Mazurier, L. Pirro, J. Sachse, P. Baars, J. Faul, C. Grass, G. Grasshoff, P. Javorka, T. Kammler, "22 nm FDSOI Technology for Emerging Mobile, Internet-of-Things, and RF Applications", presented at 2016 IEEE International Electron Devices Meeting (IEDM), 2016.

[19] A. M. Ionescu, H. Riel, Nature 2011, 479, 329.

[20] H. Lu, A. Seabaugh, IEEE J. Electron Devices Soc. 2014, 2, 44.

[21] M. Si, C.-J. Su, C. Jiang, N. J. Conrad, H. Zhou, K. D. Maize, G. Qiu, C.-T. Wu, A. Shakouri, M. A. Alam, P. D. Ye, Nat. Nanotechnol. 2018, 13, 24.

[22] X. Wang, P. Yu, Z. Lei, C. Zhu, X. Cao, F. Liu, L. You, Q. Zeng, Y. Deng, J. Zhou, Nat. Commun. 2019, 10, 1.

[23] C. Qiu, F. Liu, L. Xu, B. Deng, M. Xiao, J. Si, L. Lin, Z. Zhang, J. Wang, H. Guo, Science 2018, 361, 387.

[24] F. Liu, C. Qiu, Z. Zhang, L.-M. Peng, J. Wang, H. Guo, IEEE Trans. Electron Devices 2018, 65, 2736.

[25] F. Liu, C. Qiu, Z. Zhang, L.-M. Peng, J. Wang, Z. Wu, H. Guo, "First Principles Simulation of Energy
Efficient Switching by Source Density of States Engineering", presented at 2018 IEEE International Electron Devices Meeting (IEDM), 2018.

[26] F. Liu, Phys. Rev. Appl. 2020, 13, 064037.
[27] J. N. Coleman, M. Lotya, A. O’Neill, S. D. Bergin, P. J. King, U. Khan, K. Young, A. Gaucher, S. De, R. J. Smith, Science 2011, 331, 568.
[28] J. Wu, J. Peng, Z. Yu, Y. Zhou, Y. Guo, Z. Li, Y. Lin, K. Ruan, C. Wu, Y. Xie, J. Am. Chem. Soc. 2018, 140, 493.
[29] Y. Zhang, L. Yin, J. Chu, T. A. Shifa, J. Xia, F. Wang, Y. Wen, X. Zhan, Z. Wang, J. He, Adv. Mater. 2018, 30, 1803665.
[30] P. Paletti, R. Yue, C. Hinkle, S. K. Fullerton-Shirey, A. Seabaugh, npj 2D Mater. Appl. 2019, 3, 1.
[31] H. Schmid, C. Bessire, M. T. Björk, A. Schenk, H. Riel, Nano Lett. 2012, 12, 699.
[32] J. Hall, N. Ehlen, J. Berges, E. van Loon, C. van Efferen, C. Murray, M. Rosner, J. Li, B. V. Senkovskiy, M. Hell, ACS Nano 2019, 13, 10210.
[33] A. I. Khan, K. Chatterjee, B. Wang, S. Drapcho, L. You, C. Serrao, S. R. Bakaul, R. Ramesh, S. Salahuddin, Nat. Mater. 2015, 14, 182.
[34] S. Dutta, Quantum transport: atom to transistor, Cambridge university press, 2005.
[35] G. Pizzi, M. Gibertini, E. Dib, N. Marzari, G. Iannaccone, G. Fiori, Nat. Commun. 2016, 7.
[36] R. Quhe, X. Peng, Y. Pan, M. Ye, Y. Wang, H. Zhang, S. Feng, Q. Zhang, J. Shi, J. Yang, ACS Appl. Mater. Interfaces 2017, 9, 3959.
[37] J. Yan, H. Pang, L. Xu, J. Yang, R. Quhe, X. Zhang, Y. Pan, B. Shi, S. Liu, L. Xu, Adv. Electron. Mater. 2019, 5, 1900226.
[38] Y. Guo, F. Pan, G. Zhao, Y. Ren, B. Yao, H. Li, J. Lu, Nanoscale 2020, 12, 15443.
[39] Y. Pan, J. Dai, L. Xu, J. Yang, X. Zhang, J. Yan, J. Li, B. Shi, S. Liu, H. Hu, Phys. Rev. Appl. 2020, 14, 024016.
[40] W. Zhou, S. Zhang, Y. Wang, S. Guo, H. Qu, P. Bai, Z. Li, H. Zeng, Adv. Electron. Mater. 2020, 6.
[41] H. Lee, L.-E. Yu, S.-W. Ryu, J.-W. Han, K. Jeon, D.-Y. Jang, K.-H. Kim, J. Lee, J.-H. Kim, S. Jeon, "Sub-5 nm All-Around Gate FinFET for Ultimate Scaling", presented at 2006 Symposium on VLSI Technology, 2006. Digest of Technical Papers., 2006.
[42] C. Qiu, Z. Zhang, M. Xiao, Y. Yang, D. Zhong, L.-M. Peng, Science 2017, 355, 271.
[43] Q. Zhou, Q. Chen, Y. Tong, J. Wang, Angew. Chem. Int. Ed. 2016, 55, 11437.
[44] H. Wang, X. Wang, F. Xia, L. Wang, H. Jiang, Q. Xia, M. L. Chin, M. Dubey, S.-j. Han, Nano Lett. 2014, 14, 6424.
[45] J. Shim, S. Oh, D.-H. Kang, S.-H. Jo, M. H. Ali, W.-Y. Choi, K. Heo, J. Jeon, S. Lee, M. Kim, Nat. Commun. 2016, 7, 1.
[46] T. Roy, M. Tosun, X. Cao, H. Fang, D.-H. Lien, P. Zhao, Y.-Z. Chen, Y.-L. Chueh, J. Guo, A. Javey, ACS Nano 2015, 9, 2071.
[47] P. Zhang, S. T. Le, X. Hou, A. Zaslavsky, D. E. Perea, S. A. Dayeh, S. T. Picraux, Appl. Phys. Lett. 2014, 105, 062106.
[48] R. Yan, S. FathiPour, Y. Han, B. Song, S. Xiao, M. Li, N. Ma, V. Protasenko, D. A. Muller, D. Jena, Nano Lett. 2015, 15, 5791.
[49] X. Xiong, M. Huang, B. Hu, X. Li, F. Liu, S. Li, M. Tian, T. Li, J. Song, Y. Wu, Nat. Electron. 2020, 3,
[50] M. L. Perrin, R. Frisenda, M. Koole, J. S. Seldenthuis, J. A. C. Gil, H. Valkenier, J. C. Hummelen, N. Renaud, F. C. Grozema, J. M. Thijssen, Nat. Nanotechnol. 2014, 9, 830.
[51] Y.-C. Lin, R. K. Ghosh, R. Addou, N. Lu, S. M. Eichfeld, H. Zhu, M.-Y. Li, X. Peng, M. J. Kim, L.-J. Li, Nat. Commun. 2015, 6, 1.
[52] L. Britnell, R. Gorbachev, A. Geim, L. Ponomarenko, A. Mishchenko, M. Greenaway, T. Fromhold, K. Novoselov, L. Eaves, Nat. Commun. 2013, 4, 1.
[53] G. W. Burg, N. Prasad, B. Fallahazad, A. Valsaraj, K. Kim, T. Taniguchi, K. Watanabe, Q. Wang, M. J. Kim, L. F. Register, Nano Lett. 2017, 17, 3919.
[54] S. Smidstrup, T. Markussen, P. Vancraeyveld, J. Wellendorff, J. Schneider, T. Gunst, B. Verstichel, D. Stradi, P. A. Khomyakov, U. G. Vej-Hansen, J. Phys.: Condens. Matter 2019, 32, 015901.
[55] M. J. van Setten, M. Giantomassi, E. Bousquet, M. J. Verstraete, D. R. Hamann, X. Gonze, G.-M. Rignanese, Comput. Phys. Commun. 2018, 226, 39.
[56] Y. Yin, C. Shao, C. Zhang, Z. Zhang, X. Zhang, J. Robertson, Y. Guo, ACS Appl. Mater. Interfaces 2020, 12, 22378.
[57] Y. Yin, Z. Zhang, H. Zhong, C. Shao, X. Wan, C. Zhang, J. Robertson, Y. Guo, ACS Appl. Mater. Interfaces 2021, 13, 3387.
[58] J. Zhao, X. Huang, Y. Yin, Y. Liao, H. Mo, Q. Qian, Y. Guo, X. Chen, Z. Zhang, M. Hua, J. Phys. Chem. Lett. 2021, 12, 5813.

TOC