A novel reversible logic gate and its systematic approach to implement cost-efficient arithmetic logic circuits using QCA

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A B S T R A C T
Quantum-dot cellular automata, is an extremely small size and a powerless nanotechnology. It is the possible alternative to current CMOS technology. Reversible QCA logic is the most important issue at present time to reduce power losses. This paper presents a novel reversible logic gate called the F-Gate. It is simplest in design and a powerful technique to implement reversible logic. A systematic approach has been used to implement a novel single layer reversible Full-Adder, Full-Subtractor and a Full Adder–Subtractor using the F-Gate. The proposed Full Adder–Subtractor has achieved significant improvements in terms of overall circuit parameters among the most previously cost-efficient designs that exploit the inevitable nano-level issues to perform arithmetic computing. The proposed designs have been authenticated and simulated using QCADesigner tool ver. 2.0.3. © 2017 The Authors. Published by Elsevier Inc. This is an open access article under the CC BY license (http://creativecommons.org/licenses/by/4.0/).

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### Specifications Table

| Subject area                          | Nanoelectronics                        |
|--------------------------------------|----------------------------------------|
| More specific subject area           | Nanotechnology QCA reversible logic design |
| Type of data                         | Table, figure                          |
| How data was acquired                | QCADesigner software Bistable engine and Analysis process have been applied to attain the data results |
| Data format                          | Analyzed                               |
| Experimental factors                 | Reversible F-Gate has been proposed. It has been testified to determine various arithmetic logic circuits |
| Experimental features                | Computational Simulation study has been used to determine results |
| Data accessibility                   | Data is available within this article   |

### Value of the data

- Gates are the basic building block to design logic in digital systems. A new reversible F-Gate has been proposed to enhance the performance of digital systems.
- Adder circuits are widely investigated since their performance can directly affect the whole digital system performance. We have proposed an optimal reversible Arithmetic circuits including Adder, Subtractor and Adder-Subtractor using the proposed F-Gate.
- The presented circuit designs and data analysis can support the researchers to reduce the circuit complexity and implement high robust Arithmetic logic designs.
- The proposed QCA reversible designs can be used to reduce hardware cost and design energy lossless arithmetic logic unit (ALU) in quantum computers.

### 1. Data

In this paper, a new high speed and a low power reversible gate called the F-Gate has been proposed. The logic symbol, QCA layout, and its simulation results are shown in Fig. 1. The proposed gate has been used in a systematic manner to implement single layer arithmetic logic functions such as reversible Full Adder (RFA), reversible Full Subtractor (RFS) and reversible Full Adder-Subtractor (RFAS). The logic symbol, QCA layout, and simulation results of the proposed Arithmetic circuits are shown in Figs. 2–4, respectively. A detailed report on the hardware costs achieved from the proposed QCA implementations in terms of area, cell counts and clock delays are provided in Table 1. However, the structural evaluation of the proposed RFAS circuit has been compared with their conventional counterparts [1–5]. The detailed comparison results of RFAS are shown in Table 2.

### 2. Experimental design, materials and methods

QCADesigner tool ver. 2.0.3 [6] with default parameters have been verified the functioning of the proposed QCA-circuits. The default parameters are listed as: QCA cell size = 18 nm, diameter of quantum dots = 5 nm, number of samples = 50,000, convergence tolerance = 0.001, radius of effect = 65 nm relative permittivity = 12.9, clock low = 3.8e–23 J, clock high = 9.8e–22 J, clock amplitude factor = 2.000, layer separation = 11.5 nm and maximum iterations per sample = 100.
The simulation result, shown in Figs. 1–4, validates the functionality of the proposed circuits, which has used the proposed F-Gate as its main functional block. The construction of the F-Gate is simple in design. It consists of three inputs \( A, B, \) & \( C \) and three outputs \( "P, Q, & R" \). The main processing part of the F-Gate is a three-input XOR (TIEO) \([8]\). The \( Q = (A \oplus B \oplus C) \) is carried out from the main part of the F-Gate. The logic expression of inputs & outputs are expressed as:

\[
P = A
\]

\[
Q = (A \oplus B \oplus C)
\]

\[
R = B
\]

Fig. 1. (a) Logic symbol (b) QCA Layout (c) Simulation results.
To testify the functionality of the F-Gate it has been used as a main component to compute Sum bits of the reversible Full-Adder (RFA), Difference of the reversible Full-Subtractor (RFS) and Sum/Difference of the reversible Full Adder-Subtractor (RFAS). Table 2 includes a comparison between our proposed Full Adder-Subtractor with their conventional counterparts. An extensive structural analysis have been developed in different aspects of Area, Circuit complexity and cost of the proposed Full Adder-Subtractor and previously published works [1–5]. The proposed RFAS produce one garbage outputs. However, clock zones for wire crossing signal synchronization makes the latency (number of clock cycles), a little head greater than conventional designs. But the RFAS have achieved a significant improvements in terms of Cost = Area × Delay × Power [7] than existing one. It performs both addition and subtraction operations. The main outputs of the RFAS circuit are, \( P = A \oplus B \oplus C \), ...
Fig. 3. (a) Logic diagram (b) QCA Layout (c) Simulation results.
Fig. 4. (a) Logic diagram (b) QCA Layout (c) Simulation results.
produces Sum/Difference. The Sum/Difference is the Sum and Difference of the three inputs \((A, B, C)\) and \(Q = MV (A', B, C) \& R = MV (A, B, C)\) are the outputs of Borrow and Carry, respectively.

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**Transparency document. Supplementary material**

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**Appendix A. Supplementary material**

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References

[1] X. Ma, J. Huang, C. Metra, F. Lombardi, Reversible and testable circuits for molecular QCA design, in: M. Tehranipoor (Ed.), Emerging Nanotechnologies, Springer, US, 2008.
[2] B. Sen, M. Dutta, S. Some, B.K. Sikdar, Realizing reversible computing in QCA framework resulting in efficient design of testable ALU, ACM J. Emerg. Technol. Comput. Syst. 11 (2014) 8–22 (30).
[3] B. Sen, M. Dutta, M. Goswami, B.K. Sikdar, Modular design of testable reversible ALU by QCA multiplexer with increase in programmability, Microelectron. J. 45 (2014) 1522–1532.
[4] Z. Mohammadi, M. Mohammadi, Implementing a one-bit reversible full adder using quantum-dot cellular automata, Quantum Inf. Process. 13 (2014) 2127–2147.
[5] M. Moaiyeri, E. Taherkhani, S. Angizi, A Novel Efficient Reversible Full Adder-Subtractor in QCA Nanotechnology, CS, arXiv1610.09473, 2016.
[6] K. Walus, T.J. Dysart, G.A. Jullien, R.A. Budiman, QCADesigner: a rapid design and simulation tool or quantum-dot cellular automata, IEEE Trans. Nanotechnol. 3 (2004).
[7] V.G. Oklobdzija (Ed.), The Computer, Engineering Handbook, CRC Press, Boca Raton, FL, 2002, pp. 81–86.
[8] F. Ahmad, Gh. Mohiuddin Bhat, H. Khademolhosseini, S. Azimi, S. Angizi, K. Navi, Towards single layer quantum-dot cellular automata adders based on explicit interaction of cells, J. Comput. Sci. 16 (2016) 8–15.