Research and Implementation of Clock Synchronization Technology Based on PTP

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Abstract. With the rapid development of power system, the requirement of network clock synchronization accuracy is becoming higher and higher, in many cases, it needs to reach microsecond level. In order to meet the increasing demand, based on the analysis of the basic principle of PTP clock synchronization protocol, a physical layer clock synchronization system based on STM32 MCU and DP83640 chip is proposed. The system synchronization time error is less than 1 microsecond by using the timeacc-007 time precision measuring instrument. The scheme meets the requirements of accurate clock synchronization for all distributed nodes in the power system.

Key words: PTP, clock synchronization, DP83640, STM32

1. Introduction
IEEE1588 is a precise clock synchronization protocol standard developed by IEEE, which is called PTP (precision timing protocol)[1]. It is mainly used to realize high precision time synchronization between control systems, especially for precise clock synchronization of distributed control system constructed by Ethernet.

2. Principle of PTP clock synchronization technology
Each node in PTP network needs to complete two tasks to achieve clock synchronization. Firstly, establish the master-slave clock relationship, that is, the clock source with the best stability in the network is selected as the master signal according to the optimal master clock algorithm; second, the clock signal of each slave clock distribution node is coordinated with the master clock signal, Through the information exchange between computers, the clock signal difference between the distributed node
and the master clock node is calculated, and the clock signal of the distributed node is automatically adjusted to synchronize with the master clock.

2.1. **PTP system composition**

The main components of PTP system include two devices, time protocol device and non-time protocol device. The time protocol equipment mainly includes general clock module, edge clock module, node to node transmission clock module, peer-to-peer transmission clock module, etc. Non time protocol equipment must include server, gateway and other basic computer network communication equipment[2].

2.2. **PTP clock synchronization process**

2.2.1. *Establishment of master slave synchronization level*

In each cycle of PTP, each clock node of general clock module and edge clock module runs independently. When the system works, it is necessary to inspect the announcement message received by each node. According to the principle of "state determines event", the message content is analyzed according to the best master clock algorithm, and the normal clock or boundary clock is analyzed to determine the working state of each clock. The port status of the master-slave hierarchy is determined as follows:

a) Master: it takes the time source on its itinerant path as the node;

b) Slave: the node synchronizes to a device on the path that has a port in the master clock state;

c) Passive: it does not take the master clock module on the itinerant path as the node, and does not coordinate with the master clock module.

The establishment of master-slave synchronization level needs to go through the following steps:

a) Announcement message receiving and sending: the general clock module or edge clock module uses the format of the announcement message to send the clock information data of the node's grandmaster to each other;

b) BMC algorithm: run the best master clock algorithm (BMC) at each distributed node receiving message data, determine which distribution node to select as the grandfather clock information receiving port or select itself as the grandfather clock signal, and recommend the status of each distributed node;

c) Data set update: the recommended state of BMC algorithm, and the data information of each data set is updated by equipment data set;

d) Port state determination: using the recommended state calculated by BMC and the current state of distributed nodes, each distributed node runs the state machine separately, and finally determines the principal and subordinate relationship between each node, so as to determine the master-slave system of the whole domain.

2.2.2. *basic master slave synchronization mechanism*

In the precision clock synchronization system, the exchange mode of synchronous message is as shown in Figure 1. The specific steps of message exchange mode are as follows:
a) The main body issues synchronous message to each service object, and records the sending time t1 of the message in the main body;
b) The slave node receives the synchronization message issued by the main body and records the local time t2 when the slave node receives the message from the main body;
c) The master node can tell the slave node the sending time t1 of synchronization message in the following two ways:
   1) To embed the time stamp T1 in the synchronous message, it requires relevant operations at the hardware level to compress the error to a small enough value.
   2) In follow The time stamp t1 is embedded in the up message.
d) The slave node then sends a delay request to the master node and records the sending time t3;
e) The main node receives the delay request and records the arrival time t4 of the message;
f) At last the main node sends a delay request response message to inform the slave node t4.

Then the time of calculation is:
\[ t2 - t1 = \text{delay} + \text{offset} \]  
\[ t4 - t3 = \text{delay} - \text{offset} \]

Namely:
\[ \text{Offset} = \frac{([t2-t1]-(t4-t3))/2} \]
\[ \text{Delay} = \frac{([t2-t1]+(t4-t3))/2} \]

Fig. 1 Basic synchronous message exchange

3. Implementation of PTP clock synchronization node

3.1. design of PTP clock synchronization node
At present, there are three ways to realize the clock synchronization of precision clock protocol. One is to use the processor chip with internal integration of precision clock protocol; the second is to use customized SoC system on chip with built-in precision clock protocol; the third is to use management chip with internal integration of precision clock protocol function. Through the comparison of the schemes, in order to meet the needs of the project, we adopt the third scheme, the dedicated Ethernet
physical layer management chip DP83640[3]. The application principle block diagram of the scheme is shown in Fig. 2.

![Application Principle Block Diagram](image)

**Fig. 2** Design scheme block diagram of PTP clock synchronization unit

3.2. Design and implementation of PTP clock synchronization node

This scheme adopts embedded platform design. STM32F103 is selected as the main control chip, and a DP83640 chip with PTP protocol is controlled. The precise clock protocol is realized by the distribution of embedded network nodes. Precise clock synchronization can be realized on the hardware of distributed control system. The schematic diagram of the scheme is shown in Fig. 3.

![Schematic Diagram](image)

**Fig. 3** PTP clock synchronization principle block diagram

The main control chip selected in this scheme is STM32F103 single chip microcomputer produced by Italian semiconductor company. It adopts Cortex-M3 architecture of arm company as the foundation, and has strong data processing ability. Moreover, the working clock frequency can be set to 72Mhz, with fast response speed. It is equipped with flash ROM, which can complete the data access[4], and has rich I / O port, time timer, communication interface, convenient connection and communication with external equipment. The processor can carry out data processing, protocol operation, peripheral control and other functions. Mac function module is a media intervention controller, which is divided into two parts: receiving and sending[5]. The function module is implemented by Altera ep3ce chip. The DP83640 chip produced by national semiconductor company of the United States is selected in this scheme. Its clock output signal can be programmed to set its working speed. The clock frequency can be synchronized with IEEE1588 clock frequency through the program. Therefore, the chip can support the precise clock protocol in the physical layer, and receive and detect all kinds of event messages of the precise clock.

4. PTP clock synchronization function tests
4.1. **PTP master and slave node clock message interaction test**

Test requirements: master and slave clocks shall exchange information according to message format and process specified in PTP protocol.

Test configuration:

1) build a precise clock synchronization function test platform, the experimental platform block diagram is shown in Figure 4. Set node M1 as the master clock signal and node S1 as the slave clock signal. Connect M1 and S1 to IEEE 1588 switch port.

![Fig. 4 The master-slave equipment is connected through PTP switch](image)

2) The master and slave clock message exchange process data are obtained by data grabbing tool software.

Test results: the master-slae clock message exchange process data is shown in Figure 5, and the transmission format is Ethernet.

![Fig. 5 Master slave clock message exchange process data](image)

4.2. **PTP clock timing accuracy test**

The time synchronization error of precise clock protocol is measured by timeacc-007. Timeacc-007 is equipped with global positioning module and controllable crystal oscillator, which can obtain...
extremely accurate world unified time from satellite. With this time as reference, it can accurately measure the time accuracy of various synchronous clock signals.

Technical requirements: the time accuracy error of the clock signal issued by the main clock node should be less than 1 microsecond.

Test configuration:
1) The master clock M1 and timeacc-007 are synchronized with GPS.
2) Set the message data to Ethernet format, delay_Resp mechanism.
3) According to the test connection block diagram of PTP time synchronization given in Fig. 6, the master clock M1 is connected to the time accuracy comprehensive tester with network cable, and the mode setting of timeacc-007 is selected as the slave clock. After the synchronization is debugged, the precision test is started, and the measurement data of 100 sampling points are continuously recorded.

![Fig. 6 PTP clock synchronization accuracy test connection block diagram](image)

Experimental results: the experimental results of PTP clock accuracy measured by the time accuracy comprehensive tester are shown in Fig. 7. It can be seen from the figure that the instantaneous time deviation of master clock M1 is -849.0ns, and the average time deviation of 100 sampling points is -355.0ns.

![Fig. 7 Timing accuracy of master slave clock](image)

Timeacc-007 has a built-in high-speed memory module (2GB flash ROM), which can store the time precision measurement experiment into it, so as to collect and analyze the experimental data. Select the timeacc-007 function as the continuous measurement mode, and set the data measurement
Once per second. After 1000 consecutive data measurements, the precision clock measurement accuracy analysis chart is obtained, as shown in Figure 8:

![PTP clock timing accuracy analysis chart](image)

**Fig. 8** PTP clock timing accuracy analysis chart

5. Conclusion

According to the working principle of PTP network time service, the STM32F103 processor is used as the data processing and control chip, and the special physical layer chip DP83640 is added to construct the precise clock synchronization node. The experimental results recorded by timeacc-007 show that the synchronization clock error of the system is less than 1 microsecond. This scheme realizes the requirements of precise clock synchronization for all distributed nodes in power system.

Reference

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