Reconfigurable Photovoltaic Emulator for Differential Diffusion Charge Redistribution Solar Modules

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ABSTRACT Evaluating, validating, testing, and performing research on hardware components that are connected to actual solar photovoltaic systems can be challenging; photovoltaic emulators are a common practical approach. In particular, addressing emulation for the crucial research topics of partial shading and cell mismatch is important. Differential diffusion charge redistribution is a switched-capacitor architecture using differential power processing for performing maximum power point tracking with cell-level granularity using only a single module-level converter. Among the prohibitive challenges is preventing damage to the module-embedded integrated circuits for the corner cases during fault and failure testing of connected hardware components including power converters. Emulators not only benefit research, but also product development and manufacturing of hardware components and power converters. This paper investigates a reconfigurable linear emulator with an analog controller for photovoltaic modules configured for differential diffusion charge redistribution. Cell mismatch and partial shading are shown to be equivalent and that the averaged behavior of these switched-capacitor solar photovoltaic modules can be represented by two separate continuous-time circuits that are coupled by feedback and constraints leading to an emulator design that is demonstrated through a hardware prototype.

INDEX TERMS Diffusion charge redistribution, MPPT, PV emulator, photovoltaic, solar.

I. INTRODUCTION
Solar power is one of the greatest alternative energy resources with photovoltaics (PV) as the most prevalent harvesting platform. However, evaluating, validating, testing, and performing research on hardware components that are connected to actual PV systems can be challenging [1]. Temperature dependency along with cell variation and mismatch, which are time-dependent, often result in poor repeatability, and together with needing large physical space are among the obstacles to using actual solar PV panels/modules [1], [2]. Furthermore, to illuminate PV modules, a high-power controllable light source [2] is typically needed, making the required power supply bulky and expensive [3]; otherwise, one would struggle with the high variability of actual solar illumination [1].

In particular, there are additional challenges with diffusion charge redistribution (DCR) [4] and differential DCR (dDCR) [5] solar PV modules because they contain integrated circuits (ICs). Preventing damage to prototype ICs is an additional concern that arises while performing actual-PV research on converters or inverters while connected to these modules or while trying different control algorithms; the risk is particularly great for the corner cases encountered in fault and failure testing.

Cell mismatch and partial shading are crucial issues in solar PV systems. Reduction of accessible power, non-convexity in maximizing output power, and hotspots are some of the problems that arise due to mismatch and partial shading. In one example, 10% shading of a solar PV module can result in 30% total power loss [6]. Hence, addressing the partial shading and mismatch problems continue to be crucial research topics in solar PV systems—central maximum power point tracking (MPPT) [7], distributed MPPT [8], and differential power...
processing (DPP) [9]–[18] are among those being investigated. Most of the DPP methods require external energy storage components per PV element including capacitors [9], [11], [12], inductors [13], [14], or transformers [10], [15]–[18].

DCR [4] is a switched-capacitor solution which enables one to perform MPPT with cell-level granularity using only a single module-level converter [19] with dDCR as an architectural extension for DPP. DCR and dDCR architectures rely on the intrinsic diffusion capacitance of the solar PV cells and do not require external energy storage elements. There have been efforts to use charge balancing of cells at the sub-module level, but not the cell level in [20], [21]. These methods use external capacitors for energy storage instead of the intrinsic diffusion capacitance of the solar PV cells. Recently, a modified DCR topology had been used to address cell and illumination mismatches in solar roofs for plug-in hybrid electric vehicles (PHEVs) [6]. In comparison to dDCR, [6] does not perform DPP and has higher conduction losses than a comparable dDCR solar PV module. As with conventional solar PV modules, having a PV emulator for DCR and dDCR not only benefits research, but also testing and validation of hardware components and power converters in product development and manufacturing.

Generally, a PV emulator consists of two important parts: (1) the controller, which includes a PV model reference, and (2) the power stage. There are two types of controllers in the literature: analog and digital controllers; and two types of power stages: switching and linear [22].

Emulator controllers use analog or digital control loops together with analog representations, digital calculations, or digitally-stored tabulations of PV models as references [2]. Analog controllers are typically implemented with operational amplifiers (op-amps). Digital controllers together with their references have been implemented on different computational platforms [2] including dSPACE [3], [23], DSPs [24], [25], microcontrollers [26], FPGAs [27], and ARM processors [28]. Examples of analog representations of PV models as a reference include using an actual PV cell [29], [30], a photosensor [31], an analog circuit [32], and a series-diode stack [30]. Digitally-implemented references are typically more flexible; for example, parameter changes to the PV model like temperature and illumination level can be imposed easily. However, digital implementations have a drawback in that current-voltage relationships are exponential, making quantization error a potential issue in either or both the analog-to-digital or digital-to-analog converter.

Switching-converter-based PV emulators use a switching power converter that is controlled to replicate the output characteristics of a solar PV module. Different dc-dc topologies are used including buck [3], [23], [25], [27], interleaved buck [29], buck-boost [26], forward [28], and full-bridge [24].

The disadvantages to switching-converter emulators include potential instability from interactions with other power electronics such as MPPT converters due to switching frequency and harmonic intermodulation and higher order converter dynamics.

Linear emulators [22], [33]–[39] do not have instability problems from switching intermodulation and higher order dynamics that are typical of switching-converters. Furthermore, quantization error is not an issue when analog controllers are used. However, analog implementations are not as flexible in setting model parameters (e.g. temperature, illumination, and shading) as emulators that use digital controllers.

A power converter for dDCR solar PV modules was validated and tested using a configurable linear emulator with an analog controller in a previous paper [19]. This new paper in the following sections analyzes and explains in detail the dDCR module emulator and validates the capability of the emulator to replicate the averaged behavior of dDCR solar PV modules.

The main new contributions include: (1) showing that the averaged behavior of switched-capacitor dDCR solar PV modules can be represented by two separate continuous-time circuits that are coupled by feedback and constraints; (2) proving the equivalency of cell mismatch and partial shading; (3) demonstrating a design method for reconfigurable and scalable emulators for dDCR solar PV modules, which is easily capable of simulating mismatched conditions.

This paper is organized by first briefly introducing DCR and dDCR solar PV modules, followed by showing that cell mismatch and partial shading are equivalent. Then, we show how the averaged behavior of the dDCR switched-capacitor system can be represented by two separate continuous-time circuits that are coupled by feedback and constraints, which leads to the implementation of the emulator. Finally, hardware results are presented to demonstrate that the emulator replicates the averaged behavior of dDCR solar PV modules.

II. DIFFERENTIAL DIFFUSION CHARGE REDISTRIBUTION FOR SOLAR PHOTOVOLTAIC SYSTEMS

Diffusion charge redistribution balances all the average voltages of the cells in a solar PV module by using the large intrinsic capacitance of solar PV cells as energy storage while charge is dynamically redistributed. Differential DCR is a method to extract the power so that only the mismatch power is processed by the dynamic charge redistribution.

A. PV MODEL

A commonly-used model for PV cells in PV emulator applications is the single-diode model [3]. The I-V relation of the single-diode model shown in Fig. 1(a) can be written [3] as

\[ I = I_p - I_s \left[ \exp \left( \frac{V + IR_s}{\frac{q}{n} k T} \right) - 1 \right] - \frac{V + IR_s}{R_p}, \]  

(1)

where \( I \) is the PV cell current (A), \( V \) is the PV cell voltage (V), \( I_p \) is the photo-generated current (A), \( I_s \) is the diode saturation current (A), \( R_s \) is the equivalent series resistance (Ω), \( R_p \) is the equivalent parallel resistance (Ω), \( \alpha \) is the diode ideality factor, \( k \) is the Boltzmann constant (1.38 \times 10^{-23} \text{ J/K}) , \( T \) is the absolute temperature of the junction (K), and \( q \) is the electron charge (1.6 \times 10^{-19} \text{ C}).
B. DCR AND dDCR CONCEPTS

DCR is a switched-capacitor solution to the problems from cell mismatch and partial shading in PV systems by using the intrinsic diffusion capacitance of solar PV cells together with integrated semiconductor switches. This technique increases energy extraction and improves MPPT efficiency under mismatch and partial shading [4]. In fact, it makes a solar PV module behave as a supercell [4] and enables us to perform MPPT with cell-level granularity using only a single module-level converter [19].

The diode capacitance $C_d$ in the single-diode model in Fig. 1(b) represents a significant amount of capacitance [4]. The intrinsic diffusion capacitance $C_d$ of a solar PV cell in [4] is as high as 10 $\mu$F. These intrinsic capacitances together with semiconductor switches form a switched-capacitor structure, which ultimately balances the average voltages among the solar PV cells. An example $3 \times 2$ DCR structure is shown in Fig. 1(c). However, this structure has one drawback in that all the power from the right string is necessarily processed through two switches, which are circled in Fig. 1(c); in other words, the current through these switches is not just the mismatch current as it for all the other switches, but rather the entire string current, hence causing a larger insertion loss [19].

To solve this problem, the dDCR architecture has been introduced [5] by adding a second port to the DCR architecture. An example $3 \times 2$ dDCR structure is shown in Fig. 1(d). The dDCR architecture preserves DPP by ensuring that only mismatch power is processed by the switches. Since the dDCR architecture is a two-port structure, it needs a two-port converter [19] and the conventional one-port converters like a boost converter cannot be applied to dDCR solar PV modules. Similarly, the one-port PV emulators presented in the literature do not represent the behavior of the two-port dDCR solar PV modules; as an example, a one-port PV emulator cannot be used for evaluating and testing a two-port converter suitable for dDCR solar PV modules. Thus, a two-port PV emulator is investigated in this paper to replicate the averaged behavior of dDCR solar PV modules. Although, the focus of this study is emulating dDCR solar PV modules, the time-averaged analysis of the dDCR switched-capacitor structure introduced in Section III can be used for similar switched-capacitor structures in solar PV systems. Furthermore, the general concepts used for hardware implementation of the investigated linear emulator in this paper can be utilized to design conventional PV emulators.

It should be noted that, an important advantage of dDCR PV solar modules is that for practical implementations, where the losses from interconnects and switch resistances are small, the maximization of output power is convex with respect to: (1) the sum of the output currents, and (2) the proportion of the current from each of the two strings, even under mismatched/partial shading conditions [5]. This makes it possible to perform a simple two-dimensional perturb-and-observe MPPT to find the maximum power point [19]. As a result of this interesting property, the $P$-$V$ curves of dDCR solar PV modules and also the investigated emulator in this paper always have only one peak in contrast to the possible multi-peak $P$-$V$ curves of conventional PV modules and emulators, even under mismatched/partial shading conditions. This will be validated in Section V.

C. DCR AND dDCR MODULES: PRINCIPLES OF OPERATION

Solar PV modules that use DCR and dDCR in its simplest form consist of ladder structures that form two strings of solar PV cells in series. Cells of each string are individually shorted to particular cells of the adjacent string via semiconductor switches. A DCR or dDCR structure with $2N+1$ solar PV cells consists of $2N+2$ semiconductor switches. Figure 1 shows two examples: a $3 \times 2$ DCR and dDCR structure, each consisting of 5 PV solar cells and 6 semiconductor switches. The switches are denoted in Figs. 1(c) and 1(d) by their phases: the $\varphi_a$-switches alternately turn ON with the $\varphi_b$-switches at 50% duty cycle. To clarify the principle of operation in DCR and dDCR solar PV modules, the corresponding switched-capacitor structures of a $3 \times 2$ dDCR architecture during $\varphi_a$ and $\varphi_b$ are shown in Fig. 2(a) and Fig. 2(b), respectively. Figure 2 shows that during each phase, the diffusion capacitance $C_d$ of each solar cell is shorted to the diffusion capacitance $C_d$ of a particular solar cell from the adjacent string via two particular semiconductor switches. As a result, the average voltages of the cells become equal, even under partial shading and cell mismatch [19].

III. DIFFERENTIAL-DCR EMULATOR: CONCEPTS AND PRINCIPLES

Typical implementations of diffusion charge redistribution in a solar PV module have open-loop dynamics in that the behavior of the switches is dependent only on a fixed clock; intermodulation effects can be eliminated by synchronizing connected power converters to this clock. Under these
conditions, a continuous-time PV emulator can represent the averaged behavior of the dDCR switched-system well.

A. CELL MISMATCH AND PARTIAL SHADING EQUIVALENCY

Partial shading or shading mismatch is when PV cells within a single module are under different levels of solar illumination. In other words, the cells, each represented by Fig. 1(b), have different corresponding photo-generated current $I_{ph}$. Cell mismatch, on the other hand, occurs when cells are physically different. In other words, the cells have different corresponding $\alpha$, $I_s$, $T$, $R_s$, and/or $R_p$ in (1). In this section, we show that these two phenomena manifest as electrical equivalents.

Assume that for a given mismatched solar PV cell $\alpha$, $I_s$, $T$, $R_s$, and $R_p$ have been changed to $(\alpha + \Delta \alpha)$, $(I_s + \Delta I_s)$, $(T + \Delta T)$, $(R_s + \Delta R_s)$, and $(R_p + \Delta R_p)$. For this cell, the mismatch appears as

$$I = I_{ph} - (I_s + \Delta I_s) \left[ \exp \left( \frac{V + I (R_s + \Delta R_s)}{(\alpha + \Delta \alpha) k(T + \Delta T)} \right) - 1 \right] - \frac{V + I (R_s + \Delta R_s)}{R_p + \Delta R_p}.$$  (2)

This cell mismatch has a corresponding variation in photo-generated current $\Delta I_{ph}$ with the same voltage $V$ and current $I$,

$$I = I_{ph} + \Delta I_{ph} - I_s \left[ \exp \left( \frac{V + IR_s}{\alpha kT} \right) - 1 \right] - \frac{V + IR_s}{R_p},$$  (3)

which results in

$$\Delta I_{ph} = I_s \left[ \exp \left( \frac{V + IR_s}{\alpha kT} \right) - 1 \right] + \frac{V + IR_s}{R_p}$$

$$- (I_s + \Delta I_s) \left[ \exp \left( \frac{V + I (R_s + \Delta R_s)}{(\alpha + \Delta \alpha) k(T + \Delta T)} \right) - 1 \right] - \frac{V + I (R_s + \Delta R_s)}{R_p + \Delta R_p}.$$  (4)

So, for each cell mismatch case ($\Delta \alpha$, $\Delta I_s$, $\Delta T$, $\Delta R_s$, $\Delta R_p$), there is an equivalent partial shading case ($\Delta I_{ph}$), which corresponds to the same cell terminal voltage $V$ and current $I$.

B. AVERAGED MODEL FOR dDCR SOLAR PV MODULES

In this section, the switched-capacitor analysis presented in [40] is used to model the time-averaged behavior of switched-capacitor dDCR solar PV modules. A dDCR solar PV module consisting of $2N + 1$ cells is shown in Fig. 3(a). Replacing the cells in the dDCR structure with the modified single-diode model, neglecting the resistors, results in Fig. 3(b) and Fig. 3(c) for $\psi_a$ and $\psi_b$, respectively.

In Figs. 3(b) and 3(c), $q_{\lambda,i}^a$ denotes the charge flow of the element $x$ during phase $\psi_i$, where $i$ represents the PV cell number or output node. During $\psi_a$, shown in Fig. 3(b), Kirchhoff’s Current Law (KCL) for nodes $N_i$ results in

$$q_{\lambda,1}^a + q_{\lambda,2}^a = q_{\lambda,2i-1}^b - q_{\lambda,2i-1}^a - q_{\lambda,2i-1}^a$$

$$+ q_{\lambda,2i} - q_{\lambda,2i-1}^a - q_{\lambda,2i}^a$$  (5)

for $i = 1, \ldots, N$. For node $N_i$, shown in Fig. 3(b), Kirchhoff’s Current Law (KCL) for node $N_i$ is equal to $q_{\lambda,1}^a + q_{\lambda,2}^a$.

It is worth noting that KCL for node $N_{N+1}$ leads to an equation which differs from (5), because there is no PV cell in the right string connected to this node from the top. KCL for this node gives

$$q_{\lambda,1}^a + q_{\lambda,2}^a = q_{\lambda,2N+1}^a - q_{\lambda,2N+1}^a - q_{\lambda,2N+1}^a + q_{\lambda,2}^a.$$  (6)

For node $N_i$, shown in Fig. 3(b), Kirchhoff’s Current Law (KCL) for node $N_i$ is equal to $q_{\lambda,1}^a + q_{\lambda,2}^a$.

It is worth noting that KCL for node $N_{N+1}$ leads to an equation which differs from (5), because there is no PV cell in the right string connected to this node from the top. KCL for this node gives

$$q_{\lambda,1}^a + q_{\lambda,2}^a = q_{\lambda,2i-1}^b - q_{\lambda,2i-1}^a - q_{\lambda,2i-1}^a$$

$$+ q_{\lambda,2i-2} - q_{\lambda,2i-2} - q_{\lambda,2i-2}.$$  (7)

for $i = 2, \ldots, N + 1$. Again, for each node the sum of the intermediate charges, for example $q_{\lambda,2i-1}^a$ for node $N_2$, is equal to $q_{\lambda,1}^a + q_{\lambda,2}^a$. During $\psi_b$, KCL for node $N_1$ leads to an equation which differs from (7), because there is no PV cell in the right string connected to this node from the bottom. KCL for this node gives

$$q_{\lambda,1}^a + q_{\lambda,2}^a = q_{\lambda,1}^a - q_{\lambda,1}^a + q_{\lambda,2}^a.$$  (8)
Summing the charge flows in each node from phases $\varphi_a$ and $\varphi_b$, (5)–(8), results in

$$
(N + 1) \left( q_{\text{out},1}^a + q_{\text{out},1}^b \right) + N \left( q_{\text{out},2}^a + q_{\text{out},2}^b \right) = 
+ \sum_{i=1}^{2N+1} \left( q_{\text{ph},i}^a + q_{\text{ph},i}^b \right) - \sum_{i=1}^{2N+1} \left( q_{d,i}^a + q_{d,i}^b \right)
- \sum_{i=1}^{2N+1} \left( q_{c,i}^a + q_{c,i}^b \right).
$$

(Note that, capacitor charge balance in steady state enforces

$$
q_{c,i}^a + q_{c,i}^b = 0,
$$

for $i = 1, \ldots, 2N + 1$, which leads to

$$
(N + 1) \left( q_{\text{out},1}^a + q_{\text{out},1}^b \right) + N \left( q_{\text{out},2}^a + q_{\text{out},2}^b \right) = 
+ \sum_{i=1}^{2N+1} \left( q_{\text{ph},i}^a + q_{\text{ph},i}^b \right) - \sum_{i=1}^{2N+1} \left( q_{d,i}^a + q_{d,i}^b \right).
$$

One observes that, $(q_{\text{out},1}^a + q_{\text{out},1}^b)$ and $(q_{\text{out},2}^a + q_{\text{out},2}^b)$ are the total charge of the first and second outputs $V_1$ and $V_2$, respectively, over a complete switching period. Also, $(q_{\text{ph},i}^a + q_{\text{ph},i}^b)$ and $(q_{d,i}^a + q_{d,i}^b)$ are the total charge of the $i$th current source and the $i$th diode, respectively, over a complete switching period. The time-averaged currents can be obtained by dividing the charge flows by the switching period $T$

$$
(N + 1) I_1 + N I_2 = \sum_{i=1}^{2N+1} I_{\text{ph},i} - \sum_{i=1}^{2N+1} I_{d,i},
$$

where

$$
I_1 = \frac{q_{\text{out},1}^a + q_{\text{out},1}^b}{T}; I_2 = \frac{q_{\text{out},2}^a + q_{\text{out},2}^b}{T};
$$

$$
I_{\text{ph},i} = \frac{q_{\text{ph},i}^a + q_{\text{ph},i}^b}{T}; I_{d,i} = \frac{q_{d,i}^a + q_{d,i}^b}{T}.
$$

dDCR enforces equal average cell voltages by transferring electrical charge among the cells. This can be represented by the following DCR constraint

$$
\bar{V}_{d,1} = \cdots = \bar{V}_{d,2N+1} = \bar{V}_d,
$$

where $\bar{V}_{d,i}$ is the time-averaged voltage of the $i$th diode. In other words,

$$
\bar{V}_{d,i}(I_{d,i}, I_{\text{ph},i}) = \bar{V}_d(I_{d,j}, I_{\text{ph},j}) = \bar{V}_d
$$

even when there is a cell mismatch, which means

$$
I_{d,i} \neq I_{d,j},
$$

or there is a shading mismatch which means

$$
I_{\text{ph},i} \neq I_{\text{ph},j},
$$

where $\bar{V}$ and $\bar{I}$ refer to time-averaged voltages and currents, respectively. However, because cell mismatch is equivalent to shading mismatch, equality of all $\bar{V}_{d,i}$ means that a variation.
in diode current can be transformed into a variation in photo-generated current
\[ \Delta I_d(\Delta \alpha, \Delta T, \Delta I_s, \Delta R_s, \Delta R_p) \mapsto \Delta I_{ph}. \] (18)

Hence, we can make all \( I_{d,i} \) equal and encapsulate all the mismatches in \( I_{ph,i} \). Rewriting (12) gives
\[ (N + 1) I_1 + NI_2 = \sum_{i=1}^{2N+1} I_{ph,i} - (2N + 1) I_d. \] (19)

C. EMULATOR CONCEPT: FEEDBACK AND CONSTRAINTS APPROACH
We take the time-averaged dDCR currents and voltages and map them to continuous-time currents and voltages in the analog emulator. Furthermore, we would like to simplify the dDCR structure by aggregating the current sources, separating the series-strings, and eliminating the switched-capacitor network while satisfying (14) and (19) using feedback and algebraic constraints. In this section, we show that the emulator in Fig. 4 is a correct simplification.

Observe that, for Fig. 3(a), (14) results in
\[ V_L = V_R = N \bar{V}_d. \] (20)

This can be modeled by two series-diode stacks as shown in Fig. 4(a). It should be noted that, the average voltage difference of two series-diode stacks is \( \bar{V}_d/2 \). In other words, there is a small offset between \( V_1 \) and \( V_2 \) which can be approximately modeled by a single Schottky diode.

For the emulator in Fig. 4(a) we want
\[ I_1^* - I_{d,L} = I_1, \] (21)
\[ I_2^* - I_{d,R} = I_2, \] (22)
where
\[ I_{d,L} = I_{d,R} = I_d. \] (23)

![FIG. 4. Emulator concept: (a) Power Stage; (b) Control Stage.](image)

We use (21) and (22) to map the average currents in (19) to continuous-time currents in the emulator and write
\[ (N + 1) I_1 + NI_2 = (N + 1) I_1^* + NI_2^* - (2N + 1) I_d. \] (24)

Now by comparing (19) and (24) one observes that
\[ \sum_{i=1}^{2N+1} I_{ph,i} = (N + 1) I_1^* + NI_2^*, \] (25)
which gives
\[ I_{ph,avg} = \frac{\sum_{i=1}^{2N+1} I_{ph,i}}{2N + 1} = \frac{N + 1}{2N + 1} I_1^* + \frac{N}{2N + 1} I_2^*, \] (26)
where \( I_{ph,avg} \) is the collective average of the time-averaged photo-generated current of all the cells. The control scheme that enforces (20) and (26) for Fig. 4(a) is shown in Fig. 4(b).

In other words, the emulator in Fig. 4 replicates the time-averaged behavior of the dDCR structure in Fig. 3(a). The parameters needed to program the emulator are \( I_{ph,avg} \) and \( N \).

IV. EMULATOR: HARDWARE IMPLEMENTATION
The emulator elaborated in section III can be implemented using \( v_{be}\)-multipliers [41], PFETs, op-amps, and difference amplifiers. A realization of the emulator shown in Fig. 4 is illustrated in Fig. 5.

A. POWER STAGE
The power stage of this emulator is linear and consists of closed-loop current sources and \( v_{be}\)-multipliers.
1) CURRENT SOURCES

As shown in Fig. 5(a), each series-string uses a PFET in closed-loop as the current source. The current of the PFET is measured via a Hall-effect sensor, which outputs a voltage proportional to the current. An op-amp \((A_1 \text{ or } A_2)\) compares this voltage to a reference voltage coming from the control circuit in Fig. 5(b), creating an appropriate gate voltage for the PFET. The currents of each PFET would be proportional to the respective reference voltages \(V(I_1^+)\) and \(V(I_2^+)\). It should be noted that level shifting is not shown in Fig. 5 for clarity.

2) \(v_{be}\)-MULTIPLIERS

To reduce the number of discrete power devices, two series-strings of \(v_{be}\)-multipliers denoted by \(v_{be-M}\) are used instead of two series-diode stacks. In this way, for each side in Fig. 5(a), three \(v_{be}\)-multipliers are used instead of 35 diodes (for a 70+1 cell module). It should be mentioned that the reason for using three \(v_{be}\)-multipliers instead of one is the limit on thermal dissipation.

Each \(v_{be}\)-multiplier consists of Darlington-connected BJTs and two resistors, which behaves like a power diode with an approximate voltage drop of

\[
V_{ON} = 2 \times 0.7 \, \text{V} \times \frac{R_1 + R_2}{R_2},
\]

where 2 is the multiplicity of the Darlington pair and 0.7 V is the approximate voltage drop of a silicon diode. Using \(v_{be}\)-multipliers makes the emulator scalable, resistable, and easily reconfigurable by changing the values of \(R_1\) and \(R_2\). It will be discussed later how cell mismatch can also be easily implemented by changing these resistors. As mentioned previously, there is a small offset between the voltages of the two sides from the extra cell, which can be well-approximated by a single Schottky diode.

As mentioned in Section II, the general concepts used for hardware implementation of the investigated linear emulator in this paper can be utilized to design conventional PV emulators. As an example, if we put one current source and one bypass diode across each \(v_{be}\)-multiplier, then multi-peak \(P-V\) curves can be produced as in a conventional PV emulator [36].

B. CONTROL STAGE

The control circuit in Fig. 5(b) realizes the controller in Fig. 4(b). This means that \(I_1^+\) and \(I_2^+\) are controlled in a way that (20) and (26) are satisfied.

1) SUBTRACTOR

\(V_L\) and \(V_R\) are subtracted using unity-gain difference amplifiers (\(A_3, A_4\), and \(A_5\)), which corresponds to an error voltage. In fact, the positive (\(V_L^+\) and \(V_R^+\)) and negative (\(V_L^-\) and \(V_R^-\)) ports of \(V_L\) and \(V_R\) are subtracted using \(A_3\) and \(A_4\), respectively. Then, the outputs of \(A_3\) and \(A_4\) are subtracted via \(A_5\).

2) INTEGRATOR

After the subtractor stage, the error voltage is integrated by op-amp \(A_6\), as shown in Fig. 5(b).

3) REFERENCE OUTPUT

The output of the integrator is in fact the reference of the first current source \(V(I_1^+)\). Writing the equation for op-amp \(A_7\) leads to

\[
V(I_{ph,avg}) = \frac{R_5}{R_4 + R_5} V(I_1^+) + \frac{R_4}{R_4 + R_5} V(I_2^+),
\]

where \(V(I_1^+)\) is the reference of the second current source and \(V(I_{ph,avg})\) is the reference of the average photo-generated current of the cells. Recall that the currents of the PFET current sources are proportional to the reference voltages, which can be written as

\[
V(I_1^+) = pI_1^+, \quad V(I_2^+) = pI_2^+,
\]

and

\[
V(I_{ph,avg}) = pI_{ph,avg}
\]

where \(p\) is a proportionality factor. Substituting (29)–(31) into (28) results in

\[
pI_{ph,avg} = \frac{R_5}{R_4 + R_5} I_1^+ + \frac{R_4}{R_4 + R_5} I_2^+,
\]

which leads to

\[
I_{ph,avg} = \frac{R_5}{R_4 + R_5} I_1^+ + \frac{R_4}{R_4 + R_5} I_2^+.
\]

Now, by comparing (33) and (26) it can be easily obtained that to satisfy (26), it is sufficient to satisfy

\[
\frac{R_4}{R_5} = \frac{N}{N + 1}.
\]

Thus, \(R_4\) and \(R_5\) can be changed to emulate dDCR solar PV modules of different sizes. Also, \(I_{ph,avg}\), corresponding to the illumination level, can be set by changing \(V(I_{ph,avg})\) via a potentiometer. This enables the emulator to be scalable, resizable, and easily reconfigurable.

V. HARDWARE RESULTS AND DISCUSSION

A prototype of the dDCR emulator was constructed, evaluated, and tested in hardware.
FIG. 7. Hardware Results: A comparison of the emulator behavior under unshaded/matched and mismatched conditions. (a) The output contour under Unshaded/Matched Conditions. (b) The $P-V$ curves for Trajectories 1 and 2, corresponding to the power-optimal current ratio of 0.6 and the suboptimal current ratio of 0.3, respectively. (c) The output contour under Mismatched Condition A. (d) The $P-V$ curves for Trajectories 3 and 4, corresponding to the power-optimal current ratio of 0.65 and the suboptimal current ratio of 0.4, respectively. (e) The output contour under Mismatched Condition B. (f) The $P-V$ curves for Trajectories 5 and 6, corresponding to the power-optimal current ratio of 0.35 and the suboptimal current ratio of 0.7, respectively. (g) The output contour under Mismatched Condition C. (h) The $P-V$ curves for Trajectories 7 and 8, corresponding to the power-optimal current ratio of 0.48 and the suboptimal current ratio of 0.8, respectively.
A. HARDWARE SETUP
To vary output voltages and currents, the emulator was connected to the two-port converter discussed in [19]. A photograph of the system is shown in Fig. 6. In all the tests, the emulator was powered by a 27 V power supply (V_{bus} in Fig. 5(a)) and the load of the two-port converter was a constant 5 A current sink. Automated hardware experiments were performed to change I_1 and I_2, via the connected two-port converter. The output voltages and currents of the emulator were saved and maps of the emulator output characteristics under unshaded/matched conditions (Fig. 7(a) and Fig. 7(b)) and three different mismatched conditions (Fig. 7(c) to Fig. 7(h)) were obtained. It should be noted that the raw data is filtered and reduced in Fig. 7.

In the prototype, N is large (i.e. 35), so R_4 and R_5 are very nearly equal based on (34) and 10 kΩ resistors were used for R_4 and R_5. Also, the values of R_1 and R_2 were 127 Ω and 27 Ω, respectively. With these values, the voltage of each v_{be}-multiplier varied between 0 V and approximately 8 V. Therefore, the output voltages of the emulator, V_1 and V_2, varied between 0 V and approximately 24 V.

B. HARDWARE RESULTS
1) UNSHARED/MATCHED CONDITIONS
In this test, the behavior of the emulator under unshaded/matched conditions was evaluated. The experimental results are presented in Fig. 7(a) and Fig. 7(b). Figure 7(a) shows the experimental output contours of the emulator where the x-axis is the current ratio I_1/(I_1 + I_2) and the y-axis is the total current of the emulator (I_1 + I_2). This result agrees with the simulation results for real switched-capacitor dDCR solar PV modules shown in [5] and shows the convexity of the total output power of the dDCR solar PV module with respect to (I_1 + I_2) and I_1/(I_1 + I_2). Also, Trajectory 1 in Fig. 7(a), corresponding to a P-V curve slice at the power-optimal current ratio of 0.6, is plotted in Fig. 7(b). In this figure, the x-axis is V_1 and the y-axis is the total output power of the emulator. The P-V characteristic of the emulator is identical to that of a conventional solar P-V operating with a maximum power point of 100.3 W. Trajectory 2 in Fig. 7(a), corresponding to a P-V curve slice at the suboptimal current ratio of 0.3, is also plotted in Fig. 7(b). As shown, the maximum power point at this current ratio is 99.3 W which is smaller than the one at the power-optimal current ratio.

2) MISMATCHED CONDITIONS
In these tests, the behavior of the emulator under three different mismatched conditions was evaluated.

- **Mismatched Condition A**: To realize the mismatched condition, R_1 of v_{be-M5} was changed from 127 Ω to 102 Ω, which reduces the voltage and can, for example, represent partial shading. The experimental results are presented in Fig. 7(c) and Fig. 7(d). As shown, the experimental output contour has changed and the maximum power occurs at a different current ratio; furthermore, the maximum power has reduced. Trajectories 3 and 4, corresponding to a P-V curve slice at the power-optimal current ratio of 0.65 and a P-V curve slice at the suboptimal current ratio of 0.4, are plotted in Fig. 7(d). In this test, the P-V characteristic of the emulator at the power-optimal current ratio is identical to a uniformly-illuminated conventional solar P-V with a maximum power point of 98.4 W instead of 100.3 W. This demonstrates the result of an imposed mismatch on the emulator. Recall that cell mismatches are equivalent to shading mismatches, so this result could be interpreted as the behavior of the emulator under either cell or shading mismatched conditions. Note that this result agrees with the simulation results for real switched-capacitor dDCR solar PV modules shown in [5] and shows the convexity of the total output power of the dDCR solar PV module with respect to (I_1 + I_2) and I_1/(I_1 + I_2), even under mismatched/shading conditions. Also, the maximum power point at the suboptimal current ratio of 0.4 is 96.69 W, which is smaller than that at the power-optimal current ratio.

- **Mismatched Condition B**: To intensify the mismatched condition, R_1 of v_{be-M5} was changed from 102 Ω to 73 Ω. The experimental results are presented in Fig. 7(e) and Fig. 7(f). Again, the experimental output contour differs from that for the Unshaded/Matched Conditions and Mismatched Condition A with the maximum power occurring at a different current ratio. Also, the maximum power has further decreased. Trajectories 5 and 6, corresponding to a P-V curve slice at the power-optimal current ratio of 0.35 and a P-V curve slice at the suboptimal current ratio of 0.7, are plotted in Fig. 7(f). In this test, the maximum power point is 93.35 W at the power-optimal current ratio and is 92.96 W at the suboptimal current ratio of 0.6.

- **Mismatched Condition C**: Mismatched Condition B was intensified by changing R_1 of v_{be-M2} from 127 Ω to 102 Ω. The experimental results are presented in Fig. 7(g) and Fig. 7(h). Trajectories 7 and 8 shown, corresponding to a P-V curve slice at the power-optimal current ratio of 0.48 and a P-V curve slice at the suboptimal current ratio of 0.8, are plotted in Fig. 7(h). In this test, the maximum power point

![FIG. 8. Hardware Results: The P-V curves of the emulator for Trajectories 1 (.), 3 (.), 5 (.), and 7 (.) corresponding to the power-optimal current ratios for the Unshaded/Matched Conditions and Mismatched Conditions A, B, and C, respectively.](image-url)
is 88.92 W at the power-optimal current ratio and is 87.33 W at the suboptimal current ratio of 0.8.

To compare the behavior of the emulator under the four above-mentioned conditions, the $P$-$V$ curves of the emulator for Trajectories 1, 3, 5, and 7 are collectively plotted in Fig. 8. As expected, the maximum power of the entire emulator reduces by imposing more severe mismatches, yet the curves are convex for maximization.

VI. CONCLUSION

In this paper, the critical concerns in solar PV modules of cell mismatch and partial shading were shown to be equivalent. Then, it was shown that the averaged behavior of switched-capacitor dDCR solar PV modules can be represented by two separate continuous-time circuits that are coupled by feedback and constraints. From this, a reconfigurable and scalable linear emulator for dDCR solar PV modules was investigated, which not only readily simulates mismatched conditions, but is also easy to implement in hardware. A prototype of the emulator was built and the capability of the emulator to replicate the averaged behavior of dDCR solar PV modules was demonstrated. The modeling and circuit strategies described in this paper are potentially useful in the design and analysis of continuous-time emulators for switched-capacitor circuits.

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