**dMath**: A Scalable Linear Algebra and Math Library for Heterogeneous GP-GPU Architectures

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**Abstract**—A new scalable parallel math library, *dMath*, is presented in this paper that demonstrates leading scaling when using intranode, or internode, hybrid-parallelism for deep-learning. *dMath* provides easy-to-use distributed base primitives and a variety of domain-specific algorithms. These include matrix multiplication, convolutions, and others allowing for rapid development of highly scalable applications, including Deep Neural Networks (DNN), whereas previously one was restricted to libraries that provided effective primitives for only a single GPU, like Nvidia’s cublas & cudnn or DNN primitives from Nervana’s neon framework.

Development of HPC software is difficult, labor-intensive work, requiring a unique skill set. *dMath* allows a wide range of developers to utilize parallel and distributed hardware easily. One contribution of this approach is that data is stored persistently on the GPU hardware, avoiding costly transfers between host and device. Advanced memory management techniques are utilized, including caching of transferred data and memory reuse through pooling. A key contribution of *dMath* is that it delivers performance, portability, and productivity to its specific domain of support. It enables algorithm and application programmers to quickly solve problems without managing the significant complexity associated with multi-level parallelism. *dMath* can use intranode GPU-Direct Remote Direct Memory Access (GDR), developed in collaboration with the OpenMPI and MVAPICH groups that has shown to decrease latency and increase bandwidth when compared to previous techniques. Efficient inter-GPU communication is crucial to achieving greater net performance and supporting effective use of the cost-effective, GPU-dense COTS architecture adopted. *dMath*’s caching approach addresses one of the key drawbacks of GPUs, which is to keep data sets cached and to avoid overheads of the CPU-GPU memory interface wherever possible.

**Keywords**—GP-GPU, CUDA, MPI, deep learning, deep neural network, matrix-matrix multiplication, InfiniBand, scalability

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1That is, minimum time to solution is the goal.

**I. INTRODUCTION**

Machine learning algorithms leverage traditional scientific computing—correlations, convolutions, FFTs, matrix and tensor multiplication, and combinations thereof. Thus, central to the solution of key machine learning algorithms such as stochastic gradient descent is the need both for scalable architectures and algorithmic libraries that implement these kernels efficiently. Strong (Amdahl’s law) scaling is the appropriate performance metric, because problems are not field-based, and do not scale to support weak scaling (Gustafson-Barsis or scaled speedup).

The emergence of COTS x86-64 multicore servers as the hardware platform together with successive generations of faster and faster PCI buses and fabrics complete the overall picture needed to create COTS-based heterogeneous systems—from the hardware perspective—that are tuned for fast machine learning. However, a suitable programming model that supports both high performance in single machines (utilizes the GPUs for data-parallel and task parallel concurrency) and exploits the scale-out feature of the systems (medium-grain, data parallel concurrency achieved with message passing) is needed. Users will rarely be willing to write data-parallel programs in MPI that couple with local vectorized/GPU-enabled math libraries or with MPI-based libraries. Instead, they seek ease of use. Furthermore they will often want to alternate between data parallelism and task parallelism, such as in-memory analytics (e.g., Spark). Furthermore, higher productivity, and abstraction of the algorithms and details of dealing with the various sources of performance are needed, and MPI and scalable libraries of the traditional sort are insufficient.

The vast majority of users wish to solve problems involving machine learning and data analytics in a timely, efficient manner. Most often they do not want to become parallel programming experts in order to exploit the performance of GP-GPU-enabled high-speed clusters. Their primary goal is algorithmic design and evaluation, and utilization in applications. In all cases, time to solution of fixed sized problems is the chief concern for such users.

To address these opportunities and challenges, this paper presents *dMath*, a new scalable distributed math library. *dMath* provides key linear algebra operations, convolutions and other fundamental algorithms useful in the implementation of Distributed Neural Networks (DNNs). Other examples, such as cuDNN from Nvidia, provide primitives for Deep Learning (DL) on a single GPU. In contrast, *dMath* provides primitives for distributed DL. We will identify several key components that have helped in the rapid development and scalability of *dMath*.

Fundamental features of this library include: a) support for persistent storage of operands in the GPU’s device memory...
to avoid the CPU-GPU bottleneck; b) the ability to exploit multiple paths for data transfer; c) a novel data management service that allows caching of objects shared through data parallel operations for later reuse; d) services for data reorganization to support optimization of operations in series; e) an object-oriented design that abstracts multi-GPU, multi-server computing from the end-user; and f) an effective master-worker model to allow users (including those performing in-memory analytics and other task parallel operations) to utilize dMath without requiring detailed knowledge of CUDA, MPI, or data reorganization. Performance and efficiency of GPU computations (strong scalability) are emphasized. Flexible data layouts of matrix objects are supported as well. This library also demonstrates the ability to use single, double, and half-precision floating point in support of key parallel algorithms. Fast type conversion, lossy compression, sharing of data at lower precision, and mixing heterogeneous half and float precision operations are emerging features. Finally, fault tolerant aspects of this library and applications built thereon are discussed.

The main innovative claims of dMath are as follows:

- dMath looks and feels like a regular math library.
- dMath provides efficient primitives for distributed DL, and will be demonstrated via Expresso – Caffe powered by this distributed library.
- Abstract matrix and vector classes are used as the basis for specialized versions with precision, layout and computational targets (CPU, GPU, Distributed).
- dMath allows user code to be written without direct knowledge of its inner workings, or focus on specifics of the data-parallelism (all levels/kinds).
- A client-server model is supported, where the user’s main thread drives backend parallel computations; the data remains resident in the MPI processes and, specifically, cached in GPU memory.
- Within concrete implementations of the distributed matrix and vector types, dMath dispatches work to the worker nodes that collaborate via an MPI communicator.
- Eases data reorganization of concurrent objects.

A further contribution of dMath is that it achieves leading scaling when using intranode, or internode, hybrid-parallelism \( \text{II} \) (See section \[VII\]). This also means as model sizes grow one is not restricted to the memory size of a single GPU, like that of data-parallel techniques, but the aggregate of all GPUs chosen to be utilized.

dMath features a data reorganization and replication service that allows for reshaping matrices (providing a simple copy mechanism for changing concurrency for different stages of operations, and remaps between parallel data layouts). A key application of this feature is the optimization of a DNN pipeline. For instance, the matrix-matrix multiplication (GEMM) level is fastest on a relatively smaller number of GPUs. This contrasts with the convolutions which require little to no communication, and scale easily. Therefore, the ability to move from one data layout and concurrency to another is key to achieving good overall performance (rather than making compromises between stages to keep data statically laid out).

With large amounts of GPU memory and extensive computational functionality, data and computation remains persistent on the GPUs. Avoiding transfers between host and device avoid crippling scalability, dMath thereby addresses one of the key challenge of GPUs, which is the difficulty of keeping data sets cached and avoiding the overhead of the CPU-GPU memory interface wherever possible. Furthermore, a key feature of the memory management within nodes offered by dMath is pooling of unused GPU memory that avoids the costly CUDA allocation and registration with the IB driver.

Another notable feature of the system is the ability to "keep what you've seen." Because the data management layer has semantic understanding of matrices and vectors, as certain algorithms (such as a Cyclic GEMM) progress, portions of the parallel matrix can be retained in a cache (within each MPI process). This allows for reduced communication in subsequent steps, such as in the back-propogation stage of DNN training. The fact that the systems can store the output data unscably leads to better overall performance, and points to the efficacy of the GPU architecture for certain classes of strong scaling problems. For problems where computations are memory bound, replication is disabled.

Last, we exploit GPU-enabled MPI to enhance performance and exploit non-blocking MPI operations to address overlapping of communication and computation through double buffering, where appropriate. These steps are often difficult for application programmers to implement; solving these problems in dMath simplifies development.

The remainder of this paper is organized as follows. Section \[II\] provides background on the motivations for the creation of an heterogeneous, multinode architecture suitable for high performance algorithms, machine learning, and analytics based on COTS components. It also addresses the motivations for the creation of the dMath library and programming model. The system architecture underlying dMath is described in Section \[VI\]. A detailed explanation and motivation for the dMath architecture is given in Section \[III\]. Section \[IV\] highlights similarities and differences of dMath to related work. Section \[VI\] describes that COTS architecture, including the synergistic combination of latest generation NVIDIA GPUs, 100Gbit/s Mellanox InfiniBand, and high performance PCI-Gen3 Xeon Haswell servers. Examples of performance and speedup are then given in Section \[VII\]. In Section \[VIII\] we discuss the issues that heterogeneity introduces into the system including non-uniform performance of the multiple network connections of the architecture. We also address the maturity of the COTS components including MPI middleware. Future Work (cf., Section \[IX\]) is covered next, including how the architecture and dMath are evolving to exploit new features of GPUs and systems, followed by conclusions in Section \[X\].

II. BACKGROUND

High-speed machine learning is becoming one of the most important areas of high performance computing (HPC), in the commercial sphere, in academia and elsewhere. Cost-effective, scalable machine learning is a crucial aspect in the solution of significant problems. Time to solution and the potential for online applications include cloud-based and enterprise-based services such as mobile applications. However, off-the-shelf commodity clusters need to be optimized both in software
and hardware dimensions in order to support optimized data-parallel machine learning algorithms and task-parallel, in-memory analytics.

Since the early 1980’s (e.g., [10]), systems based on communicating sequential processes [11], data parallelism [12], and shared-nothing message passing have proven the most scalable for massive scale-out computations and large memories. These architectures have evolved into cluster computers with high speed COTS interconnects such as Myrinet [13], and now predominantly, InfiniBand [14]. The most effective source of raw high performance floating point performance has emerged in the last decade as long-vector accelerators typified by Nvidia and AMD General-Purpose Graphical Processing Units (GP-GPUs). Multicore CPUs have not kept up with GPU hardware; far less attention to floating point has been given, despite the emergence of short-vector instruction sets (e.g., AVX2 [15]) on x86-64 processors.

In the area of mathematical libraries, much work has been done for multiprocessor, multicore, and multicomputer architectures, typified by ScalaPack [16], Plapack [17], LAPack [18], BLAS [19], and more recently BLIS [20]. These libraries comprise de facto API standards. In the areas of vector-accelerated math libraries, Nvidia provides high performance FFTs [21] and matrix algebra cuBLAS [22] for GP-GPUs, in addition to third-party offerings. The PCI switching architecture provides efficient access to many object-oriented design principles. For example, the Matrix class is an abstract class, defining the interface for a Matrix. Subclasses such as CudaMatrix then implement the virtual methods. This abstraction allows us to use the Abstract Factory design pattern. A MathFactory interface is defined, and concrete subclasses of MathFactory are used to create specific varieties of Matrix and Vector objects (CPU, CUDA, or Distributed).

III. \textit{dMath} ARCHITECTURE

Requirements, design, and implementation issues are considered in this section.

A. Requirements

\textit{dMath} was created based on a number of key requirements:

- Support DNN pipelines efficiently with a variety of key algorithms;
- Utilize multiple GPUs together with multiple MPI processes to reduce time to solution for meaningful problem sizes for a range of commercial applications of interest to industry;
- Exploit the latest GPUs from NVIDIA, latest InfiniBand from Mellanox, and latest MPIs that utilize GDR in order to maximize inter-GPU performance;
- Exploit the availability of PCI switching in order to gain density within x86-64 servers;
- Use modern C++ design and implementation strategies based on object-oriented and meta-programming principles;
- Allow users to write their algorithmic code without attention to the details of how concurrency and data motion take place in the background to effect scalable operation;
- Support basic fault tolerance through checkpoint restart.

\textit{dMath} runs as a set of MPI processes (subsets of MPI\textunderscore COMM\textunderscore WORLD less a master node), with a single master and many workers. The framework is initialized by the developer at the beginning of the program. At this point the workers enter run loops, waiting for commands from the master node. The developer uses \textit{dMath} like any other mathematics library; the distributed computation is handled internally, and implicitly, where the high-level user is unaware of the distributed multi-GPU implementation.

B. Encapsulation and Abstraction

\textit{dMath} exploits many object-oriented design principles. For example, the Matrix class is an abstract class, defining the interface for a Matrix. Subclasses such as CudaMatrix then implement the virtual methods. This abstraction allows us to use the Abstract Factory design pattern. A MathFactory interface is defined, and concrete subclasses of MathFactory are used to create specific varieties of Matrix and Vector objects (CPU, CUDA, or Distributed).

C. Managing persistent data in the GPUs

The PCI switching architecture provides efficient access to multiple GPUs per root complex, but even with a single GPU per root complex, copying data across the CPU-GPU boundary is undesirable. \textit{dMath} data remains within the GPUs (except when explicitly required by an algorithm to copy to the master process) as it carries out the workflow required to implement a data parallel computation. Caching is therefore a critical feature of \textit{dMath} needed to improve the efficiency of CUDA-accelerated numerical computations. The strong adherence to this model means that comparatively little of the resources of the multicore CPUs are utilized.

In \textit{dMath}, a distributed matrix is split into multiple non-overlapping blocks, which are stored on individual workers. Each worker is aware of the layout of every matrix, allowing the workers to synchronize with each other without the intervention of the master node. The blocks must be of the same size, with the exception of the last row or column, which may be smaller.

The \textit{dMath} user is free to specify the layout of the blocks, taking advantage of domain-specific knowledge. Four sample layouts for a square matrix are shown in Figure 1. The block size and worker assignment must be chosen carefully. Computation is most efficient when the blocks are larger (GEMM for example), while pipelining is easier when the blocks are smaller.

Often it is desirable to have a copy of a matrix on each worker. In situations where the data rarely changes...
Fig. 2. Replication of a distributed matrix. The top row shows blocks stored by a worker in dark blue, and those stored by others in light blue. The bottom row illustrates how each worker stores a replicated copy of the entire matrix.

Fig. 3. (a) Matrix multiplication for the forward pass through a fully connected layer ($Y = W^TX$). The input data (top right) is already on the workers required for computing the output (bottom right). The blocks of the weight matrix are cycled through the workers to perform the full computation (bottom left). (b) The backward pass ($\nabla X = W^T\nabla Y$) can be done without any communication between nodes, if the blocks of the weight matrix were cached on the forward pass.

and memory is abundant, this sort of caching is beneficial. dMath supports this through the replication feature, shown in Figure 2. When the underlying matrix is updated, the workers automatically redistribute their data.

Replication and caching allow us to efficiently perform backward passes when training the fully connected layer of a neural network. As seen in Figure 3, the blocks of the weight matrix are rotated through the workers in the GEMM routine. By caching these blocks in the forward pass, the backward pass can be done without any communication.

As the program runs, memory is often used and then discarded, both by the user and internally. Instead of freeing this memory, dMath pools such memory for later reuse. This avoids the high cost of memory allocation in CUDA and the registration of this memory with the IB driver.

D. Matrix Multiplication

Matrix multiplication in dMath is performed with a variant of Fox’s algorithm [23]. A one dimensional decomposition is used like in parts (a) (b) and (c) of Figure 1. The main difference from Fox’s algorithm is that we have pipelined asynchronous rolling and no broadcasting. The algorithm is divided into outer stages, based on the number workers used. Each outer stage is divided into a number of inner stages, depending on how many blocks a worker’s data is divided into. On each step of the algorithm, every worker starts both an asynchronous GEMM call and an asynchronous cyclical transfer for the data in that row. Each block has two buffers, used for sending and receiving. On later stages, the algorithm will block until the required transfers and computation are completed before starting the next round.

A few steps of the algorithm can be seen in Figure 4. Stage 0.0 initiates GEMM and transfers for the first row of C. This is then repeated for the next two rows in stages 0.1 and 0.2. On stage 1.0, the algorithm waits until the computation and transfers are complete, ensuring that data is not overwritten while still being used. Variants of this algorithm are implemented for transposes and rowmajor decompositions.

The architecture of the system (see Figure 5) influenced our use of cyclic as opposed to broadcast based data transfer. By maintaining one to one communication between devices, we can full PCIe3 speeds. Communication tends to be the bottleneck in many scenarios, so this approach helps speed up the overall algorithm.

Other GEMM routines have been implemented in dMath that can handle arbitrary matrix layout. This generality comes at a price, however, and the cyclic variety presented above is preferred.

E. Further Experience

1) Data loading: While scaling up an application such as the training of a Deep Neural Network (DNN), it’s critical to load data fast enough so that the algorithm doesn’t stall. dMath handles this problem by storing the datasets on high speed storage, including large amounts of host memory or solid state devices. While this can significantly reduce loading time, distributing the data to the workers can also be a significant bottleneck. To remedy this issue, each worker loads its subset of the data asynchronously in a thread. The next batch is typically ready by the time the current one is done processing. A strong argument towards in-memory storage is random access, important because it can give better sampling of the data, rather than using the same mini-batch periodically in every epoch of the data.

2) Reproducibility: The ability to reproduce results is incredibly important, and when certain subroutines are stochastic in nature, one can get different results that may be extremely difficult to duplicate. In dMath we use seed values that are distributed via the master node to workers to ensure reproducible
results in many cases. Nonetheless, there are areas where concurrency and non-deterministic ordering of operations can lead to small differences in results. For example, in the distributed version of our *AddRowColSumMatrix* subroutine we sacrifice deterministic outcomes for speed and scalability, because of summing in a non-deterministic way can produce different results).

3) Fault Tolerance: The main goals of *dMath* is to aid in tractability for computationally expensive machine learning techniques such as DNNs and for this reason fault tolerance is not one of driving forces as it adds too much overhead. That said, we rely on redundant arrays of inexpensive disks (RAID) 10 disk arrays, solid-state disks (SSDs) and most importantly a dynamic checkpoint variable. The checkpoint provides a means for the high-level user to grab a snapshot of the current system, in order to save the results to disk. We encourage such functionality because some experiments can run for hours, days, weeks, or even months and energy and development cycles are often expensive.

IV. Related Work

In the area of mathematical libraries, we note previous work by many (e.g., [10], [13], [20], [24]). In the area of GPU-enabled libraries, there is significant work by vendors and others [2], [3], [21], [22], [23], [25], [26]. In the area of data-distribution-independent libraries, contributions from several researchers are noted [27], [28], [29], [30]. Vast work on dense matrix-matrix multiplication in parallel systems has been undertaken, such as SUMMA [31], PUMMA [32], and matrix multiplication poly-algorithms [33], among many others. Work on Strassen-based multiplication on CPUs and GPUs is of potential relevance too (e.g., [34]) in problems that require low precision. There are two noteworthy libraries providing primitives for DL, cuDNN and neon [2], [3]; the former has broader and more generic implementation but both are intended for single-GPU use.

As mentioned above, in the area of high-performance interconnects, Mellanox has devised the GDR-enabled optimization for Nvidia GPUs, GPU-Direct RDMA (GDR) [3]. This, together with InfiniBand networking provides the basis for COTS x86-64 or Power [35] clusters. EDR InfiniBand [36] represents the best approach to connecting such systems currently available. Numerous production and experimental clusters based on InfiniBand, and GDR exist worldwide. However, regarding PCI connectivity, we note the contribution of Cirrascale [37], which currently enables 96-lane PCI Gen3 connectivity on PCI root complexes in advanced x86-64 servers. Adding this component provides a design point that greatly improves density and cost effectiveness, but also drives the need for efficient caching and bandwidth utilization, which is noted above as one of *dMath*’s strengths.

In the area of productivity for scalable parallel programming, PETSc [38] is among the most of successful problem solving environments (PSEs) for a domain-specific approach to productivity. *dMath* follows a similar approach of abstracting parallelism and providing a complete set of primitives upon which to build an application, but in the machine-learning, signal processing, and linear-algebra domain. Matlab offers numerous toolboxes and parallel backends [39] as well, focused on experimentation and prototyping and scientific exploration rather than for creating production parallel software, or for handling multi-mode computations (i.e., data parallel and task parallel combinations such as *dMath* enables).

There are a number of DL systems that must be accredited as they are pioneering work in the field. Consider, the cloud-like computing systems from Google – Dean et al. [40], Microsoft Research – Chilimbi et al. Project Adam [41], and more GPU-centric distributed frameworks from Stanford – Coates et al [42] and Baidu – Wu et al. Minwa system [43]. Although these systems are interesting they are discerned to be single-pipeline, that is, Automatic Speech Recognition, Image Recognition, or NLP, etc, based rather than true general purpose pipelines able to tackle any task. *dMath* was constructed based on base-primitive subroutines and this means we could easily construct AIR and ASR pipelines. This is incredibly useful as it allows various internal groups to utilize *dMath* for their specific problems and benefit from reduced experimental time and development cycles. Those libraries from Microsoft & Google, CNTK [44] & TensorFlow [45] respectively, are the closest to *dMath*. CNTK was benchmarked but has stability issues on several systems we evaluated and TensorFlow is incredibly powerful but is not refined enough for performance at the time of this submission. Lastly, MXNet is another candidate in the distributed domain but lacks comparable scaling [46], given that MXNet is slower than BVLC-Caffe, and we analyze Nvidia-Caffe, a faster version of Caffe, we believe this is comprehensive enough review.

V. Algorithms and Degrees of Freedom

*dMath* combines a set of innovative ideas that simplify writing data parallel algorithms while supporting key kernels. We consider each briefly in turn.

A. Algorithms

*dMath* provides the following numerical kernels/operations distributed over MPI communicators comprising the workers. Gather and scatter of these objects to/from the master is done when needed, but this is avoided except when absolutely essential. Active objects are cached in GPU memory whenever possible, rather than moved in/out with each kernel invocation. These parallel operations are currently supported; extensions; and, b) hundreds of algorithms and methods normative to a DNN computation pipeline. These building blocks allow a variety of DNN-based pipelines to be created (implicitly with parallel backends).

B. Data Distribution Independence

Algorithms in *dMath* are correct independently of the how the distributed objects are mapped to the MPI processes (workers). Unlike other popular data-parallel math libraries, *dMath* does any needed communication to ensure compatibility, rather than limiting the distributions to block-cyclic (and/or linear) 1D or 2D decompositions, such as used in Scalpack and other libraries. Previous libraries (e.g., [27], [28]) achieve data distribution independence and varying degrees of compatibility with rectangular matrices and cartesian decompositions, but notably require that the objects be laid out compatibly at the beginning of the GEMM function, rather than offering
remapping services. As with other libraries, the shape of the data and concurrency changes the performance of $dMath$ kernels (just not the correctness). (It is notable that older libraries work hard to avoid any data reorganizations, or leave that strictly to the user to implement, such as on top of MPI_AlltoAll*.)

C. Precisions

As with many object-oriented libraries, and even traditional API-based libraries, multiple precisions are a key degree of freedom of $dMath$. Nominally, single and double precision IEEE floating point operations are provided in the parallel backend workers. These are also the precisions that are highly optimized in current high end GPU’s, such as the Nvidia K80. However, $dMath$ also has added support for half-float precision, which is available with functional support in CUDA 7.5, and has been supported in terms of compressed storage in earlier CUDA versions too.

Half-float is an IEEE-standard, 16-bit representation \[42\] that is suitable for certain parts of computations, but may be totally unsuitable for others where a longer significand is warranted. While CUDA supports half-float, current GPUs do not directly support high performance on these datatypes with 16-bit arithmetic logic units (ALUs); such ALUs are anticipated in future GPU’s, such as Nvidia’s Pascal architecture. At present, we utilize these operations with the understanding that underlying CUDA BLAS will perform single-precision computations (even through the HGEMM interface), rather than half-float computations. Nonetheless, bandwidth and on-GPU storage savings achieved by storing and moving 50% less data across the CPU-GPU boundary are both of significant value. At present, $dMath$ is providing anticipatory support for future GPUs where the 16-bit precision will actually run faster than float precision (32-bit). CUDA HGEMMs directly support operations on this precision, but we also provide the option to convert between half and float prior to using a CUDA BLAS call in order to optimize what comes after this in the pipeline.

D. Mixed Precision Computations

From stage to stage, certain but not all stages of the data-parallel pipeline of interest to $dMath$ users can work effectively varied precisions. For this reason, $dMath$ currently offers the ability to transfer vectors and matrices at lower precision (with rounding), such as by moving a float matrix at half precision and reconverting when needed prior to computation. This saves storage, memory & network bandwidth. As noted above, there are no fundamental high performance BLAS that work on mixed precisions at present, so all the numerical objects must be in the same precision before performing a CUDA BLAS kernel. $dMath$ implements certain of its own mixed precision operations at present, and apparently, with the advent of future GPUs that support higher performance on half float, we may be able to justify the value of cuBLAS that offer heterogeneous data types, rather than requiring pre- and post- conversions in a separate kernel. This will be particularly relevant once next-generation GPUs provide for higher performance with half precision.

Because of $dMath$’s object-oriented flexibility, experimenting with lower precision in certain stages of a pipeline does not require a major rewrite of a code, thereby enabling the algorithm designer to explore the error implications of changing precision and rounding.

E. Data Reorganization and Caching

Where appropriate, $dMath$ allows an algorithm to

1) reshape (including a change of concurrency and layout), over the same group of processes or a (super/sub)set
2) change precision during reshape.

This type of operation poses interesting challenges because such operations combine CUDA kernels with MPI non-blocking point to point and/or collective communications. At present, because there is no way to have kernel completion trigger MPI, or MPI completion trigger a CUDA kernel, we have to have pre- and post- conversions operate synchronously to the user thread before launching a non-blocking collective. In future, we may introduce Pthreads to support this, but that introduces the potential for needing a multithreaded MPI implementation with good multithreaded performance. So efficient reentrancy in MPI is becoming important, as is the need to be able to have efficient merger of completion notification methodologies between CUDA events, and MPI_Wait/Test/Probe\[43\].

When the size of the objects is sufficiently small (as is often the case in DNN problems), entire matrices fit in the individual GPU memories (hence can be reused with reduced communication and synchronization). As such, our stepwise refinement that maximized the concurrency of matrix formation need not correspond with the layout or gross concurrency needed to minimize time to solution for a subsequent step. Remapping helps address the former issue. However, because of the temporal locality of operations involved in DNNs, keeping segments of matrices that arrive as temporary buffers during a matrix multiplication can allow a subsequent matrix multiplication with the same operand to function with communication suppressed. Libraries of which we are aware have not exploited such excess memory capacity; in $dMath$, the data not only is retained, it is retained in the GPU memory for maximum reuse performance. We exploit the distinctive advantage here of needing to solve problems for which architectural memory capacity is sufficient for the GEMM phase to allow whole matrices to be cached; we do not need to go to asymptotically large problems in order to obtain peak performance for benchmarking purpose. Other parts of the computation utilize concurrency without replication. This may be counter intuitive to readers who always assume that any unscalability is harmful. By exploiting the provided resources fully, meaningful problems are faster than without such scalable replication; furthermore, these problem sizes are not growing faster than the available GPU memories for many use cases.

\[3\] Mixed precisions have no cuBLAS API at present, but could follow the specifications in \[45\].

\[4\] This gap motivates potential future standardization in the MPI Forum on interoperability between MPI and other parallel programming environments/notations like CUDA.
VI. HARDWARE ARCHITECTURE & CONSIDERATIONS

The dMath library provides for performance-portable parallel programs, as described in section III. It is important to indicate the underlying hybrid, heterogeneous architecture that Samsung Electronics has created in order to deliver the performance of cost-effective, high performance parallel algorithms to end users without extensive explicit parallel programming experience, with systems based integration of commodity off the shelf (COTS) technologies.

As illustrated in Figure 5 the heterogeneous architecture utilized is comprised of X86-64 servers ( multicore Haswell Xeon 2690 v2.0 [49]) connected by dual EDR InfiniBand [36], 512GB of host-memory, and SSDs for staging. We utilize the dual PCI-Gen3 buses to support up to eight NVIDIA GP-GPU’s and one InfiniBand EDR network adapter per scalable server unit root complex. At present, we utilize NVIDIA K80 GPU’s [50] where auto boost is disabled and clocks set to 758Mhz, but this architecture is suitable for use with next-generation Maxwell [51] and Pascal GP-GPU’s [52] as well. When the text refers to a GPU it is that of a single-GPU not a dual GPU card, this is true for the experiments too.

The PCIe 3.0 crossbar switch fills an essential role, because it provides low-latency switching, and full bandwidth communication between any pair. For instance, at any given moment, four GPUs can communicate and the host could be communicating via IB at full PCIv3 speeds. As long as one maintains pairwise communication between two devices, communication does not degrade, and there is no congestion in this scenario. Many of the subroutines within dMath are aware of the importance to use one to one communication to maintain optimal use of the h/w. If we were to compare this COTS architectures having only two GPUs per root-complex we can quickly see from Table I & II that the denser root complex scenario that utilizes CUDA P2P, and the PCIe 3.0 crossbar switch, is favored over shared-memory, or Internode IB EDR, for most use cases.

Modern computers have a variety of mediums for interprocess communication, e.g. shared-memory, CUDA P2P, InfiniBand, etc. Figure 5 depicts these as blue, red, and black edges, respectively, and each has associated latencies and bandwidth.

By understanding these mediums, and the workload, one can make effective use of them for specific tasks. As highlighted in Figure 5 there are several mediums to communicate and Table I - II show that communicating via shared-memory for GPU communication is very inefficient given high latency, and low bandwidth, whereas communication via Internode GDR is superior. Given the aforementioned observation we set out to introduce a new means for GPU intranode communication, where GPUs residing on different PCIe root complexes could communicate more efficiently. We worked with both OpenMPi and MVAPICH groups to provide the means to continue transferring host side communication via shared memory but used Infiniband for GPU to GPU traffic when GPUs were on different PCIe root complexes [53, 54]. As one can see latency decreased and bandwidth increased but not to the level of Internode GDR; we are actively working to match the performance of both intranode and internode GDR traffic over Infiniband EDR. There is an important consideration that both versions of MPI supported the ability to disable shared memory but this would entail the need for small meta data, often transferred between processes, to traverse the IB stack and it is not as efficient as going through shared memory, e.g. consider latency for small transfers. The results reported are from an OpenMPI but MVAPIC2-GDR-PCC are similar. In terms of real-world application performance, we will consider the use case of distributed Deep Learning (DL), where dMath v1.0 has a dedicated pipeline. The intradenode GDR showed training reductions in the order of 10-20%, depending on the number of nodes and the number of fully-connected layers, where network communication is often the bottleneck and not computation. We quickly considered the situation of scaling beyond one compute node where contention to use the IB fabric for both intranode and internode communication could be an issue. However, testing revealed for the DL pipeline scaling to 2, 4, and beyond nodes, that is, 32-64+ GPUs, still benefitted from the intranode GDR but one should be mindful of possible congestion on the EDR fabric and adjust to use shared-memory, or hybrid, for intranode communication if the workload dictates it.

We have shown and demonstrated alternative methodology for intranode communication that decreases latency and increased bandwidth; likewise scales well for Deep-Learning. The technique has shown to decrease runtime for GPU aware applications that rely on communication, such as training a CNN with fully-connected layers. The techniques are now available in both OpenMPI 2.0 and MVAPIC2-GDR-PCC from which all users of these MPIs can benefit.

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**TABLE I. COMMUNICATION MEDIUMS: LATENCY**

| Transfer | Shared Memory Host | Shared Memory GPU | IntraNode IB - EDR GDR | InterNode IB - EDR GDR | CUDA P2P |
|----------|--------------------|------------------|------------------------|------------------------|---------|
| Size     | Bytes              | Memory           |                        |                        |         |
| 0        | 0.86µs             | 0.87µs           | 0.91µs                 | 1.33µs                 | 0.93µs  |
| 1        | 1.11µs             | 3.70µs           | 6.13µs                 | 2.98µs                 | 19.41µs |
| 128      | 1.28µs             | 26.25µs          | 5.83µs                 | 5.77µs                 | 15.31µs |
| 512      | 1.54µs             | 26.20µs          | 12.00µs                | 11.58µs                | 13.33µs |
| 16384    | 6.95µs             | 30.97µs          | 16.95µs                | 16.74µs                | 17.50µs |
| 324288   | 138.61µs           | 163.39µs         | 218.72µs               | 157.12µs               | 80.91µs |
| 2097152  | 501.10µs           | 515.71µs         | 458.22µs               | 425.37µs               | 279.04µs|
| 4194304  | 971.19µs           | 936.43µs         | 765.36µs               | 741.80µs               | 541.65µs|

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![Fig. 5. Samsung Heterogeneous Multicomputer Node Architecture.](image-url)
VII. Examples of Performance and Speedup

A. Deep Neural Network Training

dMath provides hundreds of distributed, non-distributed GPU, and CPU subroutines and benchmarking is a constant process via continuous integration but annotating all those results is difficult; instead, we will show generalized Matrix Multiplication (GEMM) and the entire CNN pipeline for forward and backward propagation for raw AlexNet \[52\] & GoogLeNet v1. Profiling with AlexNet is beneficial as it includes high ratio of Fully Connected (FC) layers, where GEMM is often utilized, to convolutional layers. These FC layers are often computationally light but heavy on communication and provide a good worst-case scenario for our system. The most prominent models, as of this publication, are those that use a higher ratio of convolutional to FC layers such as VGG 16 and 19 layer models \[56\], GoogLeNet \[57\], BN-Inception \[58\], inception-variants, etc. These latter scale well when the batch size is increased, one has to be cognizant of possible accuracy degradation with larger batches but we have found many ways to stabilize the accuracy while scaling up the batch size, e.g. batch normalization and PreLU have been found many ways to stabilize the accuracy while scaling GPUs. This is an important learning publication, we include those results and exhibit an iterative metric that is often overlooked in many distributed learning publications, we include those results and exhibit stable accuracy when scaling GPUs. This is an important attribute of dMath and it is because we solved the harder problem, that of hybrid parallelism, no matter the number of GPUs the accuracy is never impacted. The only impact on accuracy is that of batch size, nonetheless 1024 seems to 8-64 GPU and 128 for below 8 GPU. The single asterisk for Expresso designates non-optimal algorithm choice for convolutions due to memory constraints; hence super linear scaling from two to four GPUs. Whereas the double asterisk signifies the GPU device memory thrashing, i.e. need for costly alloc / dealloc is seen and impacts performance for nvidia-caffe 0.14.

1) Weak Scaling DNN Tests: We profile Expresso, a Samsung internal forked version of Caffe powered by dMath that employs hybrid parallelism \[11\], compared to a forked version of Caffe \[57\], from Nvidia \[59\], which provides leading open-source multi-GPU scaling in a single machine via data - parallelism with models synced after every batch, i.e. n sync of one. We profiled both and achieved a 2615 FPS on 0.14 branch with cuDNNV4, Expresso obtaining 4198, FPS when utilizing AlexNet, 16 GPUs, and a 1.024 batch size. As one can see, the results favour Expresso and one has to consider that because it is powered by dMath one can scale past a single machine, as seen in the 32 and 64 GPU tests, whereas BVLC Caffe and Nvidia’s own branch are limited to only intranode scaling. Likewise, the hybrid nature of the implementation means the models are spread across the devices and the total models size is limited to the aggregate device-memory of the total number of GPUs used during execution, versus data-parallel techniques, where the model must be able to fit into a single GPUs memory. This means, as models grow, Expresso is a more favourable contender as it provides better intranode scaling, provides internode scaling, preserves accuracy, has the lowest memory footprint, and can support larger models.

The experiments in Table III use a batch size of 1.024 for AlexNet 2-64 GPU, 512 for single, 1024 for GoogLeNet

| Number of GPUs | AlexNet 1024 Batch (FPS) | GoogLeNet v1 1024 Batch (FPS) |
|----------------|--------------------------|--------------------------|
| 1              | 479                      | 115                      |
| 2              | 940                      | 215                      |
| 4              | 1996                     | 300                      |
| 8              | 3103                     | 973                      |
| 16             | 4198                     | 1498                     |
| 32             | 5187                     | 2330                     |
| 64             | 5786                     | 3025                     |
| Memory GB (16 GPUs) | 2.29                    | 5.27                     |
| Accuracy (Top-1%) | 55.38                   | 65.39                    |

| Number of GPUs | Expresso v0.5 | CNTK x2016-02-08 | CNTK (1-bit) x2016-02-08 | nv-caffe 0.14 |
|----------------|---------------|------------------|--------------------------|----------------|
| 1              | 533           | 580              | 588                      | 550            |
| 2              | 915           | 487              | 485                      | 711            |
| 4              | 1440          | 428              | 416                      | 898            |
| 8              | 1702          | -                | 8                        | 970            |
| 16             | 2008          | -                | -                        | 875            |
| 32             | 2104          | -                | -                        | -              |
| 64             | 2271          | -                | -                        | -              |
| Accuracy (Top-1%) | 58.59        | -                | -                        | 57.01          |
be the sweet spot for good scaling and maintaining accuracy. We are not showing the top accuracy that can be obtained in Table III-IV for these models but simply identical hyper parameters, solvers, single crop, non-ensemble to demonstrate accuracy stability when scaling the number of GPUs. We would rather not speculate on why CNTK, or Nvidia Caffe, has lower accuracy but we can state that the Expresso employs hybrid-parallelism and has provided stable accuracy as one scales the number of GPUs for a constant batch size.

B. Matrix Multiplication

We tested the performance of dMath on basic matrix multiplication, a fundamental of many computationally intensive problems. The results can be seen in Table V where dMath provide leading intranode and internode scaling. In some runs of dMath and cublas 7.5, there was insufficient memory to store the data (indicated by a dashed cell) in GPU device-memory whereas cublasXT can store in host memory. For each of the listed sizes, a square matrix multiplication was performed 100 times. The column for one GPU was done without dMath, using a simple cuBLAS 7.5 program. For the remaining columns, the matrix was split up into equal parts in both rows and columns, with each row of blocks stored on a separate GPU device memory and maintaining the in-memory characteristics of the library. There are alternatives for intranode scaling like cublasXT or Magma [60], the latter does not support GEMM, but these libraries can not scale past a single machine or achieve the same speedup.

For smaller matrix sizes, distributing to many GPUs was detrimental. This was to be expected. The performance of the cuBLAS GEMM routine is better with larger matrices as it utilizes the GPU more effectively. Computation in matrix multiplication grows cubically, while storage / communication grows quadratically. So at larger sizes, computation becomes detrimental. This was to be expected. The performance of GDR-enabled operations, including non-blocking collective implementations, which are experimental. We expect these implementations to continue to mature, and to expand support of GDR-enabled operations, including non-blocking collective processing analytics in memory (task parallel at the MPI process granularity). Within the scope of applications that we currently see as crucial to dMath users, large numbers of MPI processes (and underlying GPUs) are suitable for matrix-formation/filling. However, the finite size of the objects often means that less concurrency at the MPI process level is needed to minimize time to solution, as noted above. Furthermore, the problem sizes encountered are small enough so that they often fit entirely in each GPU memory, not just distributed over a set of GPUs. This “over service” of GPU memory at the linear algebra and data-parallel stage is a great benefit, because it means that some operations gain additional performance through the elimination of communication needed in a purely distributed environment. We note such savings in Figures 2, 3 In short, excess GPU memory is of great value for relevant problem sizes.

C. Experimental Results Conclusion

We have shown an entire DNN pipeline that provides leading intranode / internode strong / weak scaling for a DNNs. We have also shown profiling of GEMM, a fundamental base-primitive for many domains, where we also exhibit leading performance. The hybrid nature of the system provides the ability to distributed the model across all available GPU nodes, whereas many others are constrained to the memory available in a single GPU, i.e. data-parallel techniques.

VIII. Heterogeneity and System Issues

A. Implications of Heterogeneity

MPI implementations of which we are aware do not recognize the kinds and degrees of heterogeneity of systems such as contained in our node architecture. While almost all floating point computation is performed in GPUs (and hence we don’t have concerns about heterogeneity between CPU and GPU validity), the performance of MPI collective operations and point-to-point operations is impacted by the memory hierarchy. For instance, data traversing QPI is substantially slower than data traversing EDR. Furthermore, transfers between GPUs in a single root complex outstrip transfer performance between complexes. Typical MPI implementations make choices of collective operations based on a schedule, but with a homogeneous view toward the performance of the underlying links and resources. This is suboptimal in our architecture. This poses the need for topology awareness within MPI for the architecture, and comprises near-future work for our project.

B. Strong scaling and Excess Memory Capacity

Whereas many problems derive from finite approximations of partial differential equations, and scale well with added resources, our matrix-oriented problems are finite in dimension, and require strong scaling (Amdahl’s law speedup) in order to be beneficial to dMath users. Three basic stages of operations are involved in typical applications: formation of matrices, data-parallel operations on those matrices (e.g., comprising machine learning algorithms), and potential post-processing analytics in memory (task parallel at the MPI process granularity). Within the scope of applications that we currently see as crucial to dMath users, large numbers of MPI processes (and underlying GPUs) are suitable for matrix-formation/filling. However, the finite size of the objects often means that less concurrency at the MPI process level is needed to minimize time to solution, as noted above. Furthermore, the problem sizes encountered are small enough so that they often fit entirely in each GPU memory, not just distributed over a set of GPUs. This “over service” of GPU memory at the linear algebra and data-parallel stage is a great benefit, because it means that some operations gain additional performance through the elimination of communication needed in a purely distributed environment. We note such savings in Figures 2, 3 In short, excess GPU memory is of great value for relevant problem sizes.

C. Maturity of the System Components

The architecture and system created here composes a number of COTS architectures, several at the leading edge. It is worthwhile to note that the maturity of drivers, the PCI switch, servers, and GPUs has been for the most part quite good. However, a number of issues have naturally arisen on the “bleeding edge” involving the GDR-enabled MPI implementations, which are experimental. We expect these implementations to continue to mature, and to expand support of GDR-enabled operations, including non-blocking collective communication, which is not currently supported by either OpenMPI or MVAPIC2H. Topology awareness of blocking and non-blocking collectives in MPI implementations that reflect the heterogeneous and hierarchical nature of the architecture.

| Size               | 1 GPU | 2 GPUs (cublas, 7.5) | 2 GPUs (dMath) | 4 GPUs (cublas, 7.5) | 4 GPUs (dMath) | 8 GPUs (cublas, 7.5) | 8 GPUs (dMath) | 32 GPUs (cublas, 7.5) | 32 GPUs (dMath) |
|-------------------|-------|----------------------|----------------|----------------------|----------------|----------------------|----------------|----------------------|----------------|
| 4096              | 0.025 | 0.015                | 0.146          | 0.044                | 0.169          | 0.109                | 0.101          | 0.109                | 0.101          |
| 6144              | 0.174 | 0.109                | 0.589          | 0.038                | 0.259          | 0.104                | 0.104          | 0.104                | 0.104          |
| 8192              | 0.413 | 0.245                | 1.399          | 0.076                | 0.493          | 0.121                | 0.121          | 0.121                | 0.121          |
| 12288             | 1.450 | 0.840                | 2.268          | 0.433                | 1.420          | 0.258                | 0.258          | 0.258                | 0.258          |
| 16384             | 3.340 | 2.034                | 8.455          | **0.528**            | 3.223          | 0.726                | 0.726          | 0.726                | 0.726          |
| 24576             | 12.279| 6.809                | 28.062         | 1.744                | 10.295         | 1.091                | 1.091          | 1.091                | 1.091          |
| 32768             | -     | -                    | 68.618         | 4.015                | 24.657         | 2.389                | 2.389          | 2.389                | 2.389          |
| 49152             | -     | -                    | 187.344        | 14.016               | 82.161         | 5.260                | 5.260          | 5.260                | 5.260          |
| 65536             | -     | -                    | 461.233        | -                    | 192.380        | 10.592               | 10.592         | 10.592               | 10.592         |

TABLE V. MATRIX MULTIPLICATION PERFORMANCE
will also be needed to obtain efficient reductions and broadcasts as well. Furthermore, new and better standardized MPI concepts that allow simultaneous and/or adaptive use of the multiple data transfer paths available for certain transfers bears exploration; work considered in the MPI-4 Forum involving persistence and channels may help support optimizations along these lines in future MPI versions.

IX. Future Work

Significant near term opportunities present themselves for additions to dMath. In the algorithmic area, we are introducing additional variants for matrix-matrix multiplication, following [33]. This strategy will allow dMath to use the fastest algorithm based on the specific shape and concurrency of the problem.

Additionally, we plan to utilize the Maxwell and Pascal architectures’ high-speed, half-float precision. Since certain algorithmic steps can tolerate half-float precision, the introduction of half-float linear algebra will save memory bandwidth and transfer costs while providing adequate accuracy for certain numerical algorithms.

Longer term, improvements in InfiniBand (EDR to HDR), represents an additional opportunity, but this has to be keyed to greater overall availability of root complex bandwidth. Shorter term, we may explore utilizing heterogeneous server notes, that support a higher degree of bandwidth to GPU cards, in order to support certain stages of a computation with fan-in, and limited floating point requirements. Since dMath can remap efficiently, such a heterogeneous note would be useful for early and late stages of some operations. In particular, we could support nodes with dual or quad HCA’s per root complex, and dual GPUs, vs. our standard of four GPUs and a single HCA per root complex. However, before adding the level of heterogeneity to our system, we will explore the achievable performance and total cost implications of introducing a few of such nodes in a system.

X. Conclusion

A new scalable parallel math library, dMath, was presented that provides a complete primitive pipeline for mathematics and has a dedicated DL pipeline, we have shown experimental results, via Expresso, that demonstrates superior scaling to all open-source frameworks. When compared to previous work, we have shown better single node scaling, and distributed multi-node scaling, and both these results are important because they aid in tractability of the problem while experimental time is reduced. We have shown class leading strong & weak scaling that preserve accuracy when scaling up the number of GPUs. We believe the most important aspect is the dMath framework provides a high-level programming language that implicitly utilizes distributed multi-GPU programming and enables the end-user to focus on their domain specific problem without the need to understand parallel and distributed programming. We have demonstrated the effectiveness of dMath via Expresso but also have a version of the popular open-source speech recognition library Kaldi [61] powered by dMath that shows the generality of the library. We have instrumented changes in OpenMPI and MVAPICH2 MPI frameworks that have shown to decrease latency and increase bandwidth. We shared how understanding of the hardware can lead to better software, as in cyclic GEMM, a variant of Fox’s algorithm. Last, we have detailed further experiences that will inform all interested in distributed learning or key mathematical operations at scale.

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