As CUDA programs become the de facto program among data parallel applications such as high-performance computing or machine learning applications, running CUDA on other platforms has been a compelling option. Although several efforts have attempted to support CUDA on other than NVIDIA GPU devices, due to extra steps in the translation, the support is always behind a few years from supporting CUDA's latest features. The examples are DPC, Hipfy, where CUDA source code have to be translated to their native supporting language and then they are supported. In particular, the new CUDA programming model exposes the warp concept in the programming language, which greatly changes the way the CUDA code should be mapped to CPU programs. In this paper, hierarchical collapsing that correctly supports CUDA warp-level functions on CPUs is proposed. Based on hierarchical collapsing, a framework, COX, is developed that allows CUDA programs with the latest features to be executed efficiently on CPU platforms. COX consists of a compiler IR transformation (new LLVM pass) and a runtime system to execute the transformed programs on CPU devices. COX can support the most recent CUDA features, and the application coverage is much higher (90%) than for previous frameworks (68%) with comparable performance. We also show that the warp-level functions in CUDA can be efficiently executed by utilizing CPU SIMD (AVX) instructions.

Keywords GPU, code migration, compiler transformations

1 Introduction

The high-performance computing power in GPUs has developed a strong software eco-system based on GPU programs. Although there are other choices for GPU programming such as HIP [1], OpenMP and DPC [2], in recent years, CUDA is still in the dominant place. In the realm of Deep Learning, both of the two most popular frameworks, Pytorch and TensorFlow, support only CUDA for GPU backend [3]. In the multimedia realm, for the video editing applications, as lists in [4], CUDA is compatibility in 14 of the 17 applications, while OpenCL is only supported by 9 of them.

Unfortunately, despite the popularity of CUDA programs, NVIDIA GPUs are the main hardware platforms to run them. Although there have been several efforts to run CUDA on non-NVIDIA GPUs, they are lack supporting newer CUDA features. There are mainly two challenges to run CUDA on other platforms are. The first is to convert Single Program Multiple Data (SPMD) programs to programs for non-SPMD friendly architectures. In the SPMD programming model, the same kernel is executed by many threads at runtime, and the GPU is built on for through-put-oriented architectures by supporting many threads (or warps). However, other architectures often do not have that many threads, so the CUDA programs need to be converted to a fewer number of threads efficiently. The second problem is a continuous support for
still evolving programming models like CUDA. To address the second problem, we utilize the open-source compiler frame LLVM as much as possible. In this paper, we tackle the first problem: Supporting CUDA with fewer number threads, which is an essential component for running CUDA on X86, ARM, or Intel-GPU, which has fewer hardware threads than NVIDIA GPUs.

Several projects aim to support this transformation: running GPU programs on CPUs [2,5,16]. While a few projects focus on narrowing the gap between SPMD and MPMD by adding a hardware extension [15] or adding system-level support for faster context switching [16], most projects try to do compiler-level transformation to translate GPU functions to be suitable for CPUs. These projects use the same granularity of transformation: a CPU thread is responsible for executing all the threads in a CUDA block (or OpenCL work-group). The CUDA-block-to-CPU-thread mapping is optimal based on three observations: 1) it has a fewer CPU threads compared with CUDA-thread-to-CPU-thread mapping, which can lead to low overhead for context switching; 2) the memory access within a CUDA block utilizes GPU caches. Both shared memory in the CUDA programming model (or local memory in OpenCL) and global memory with spatial/temporal locality within a CUDA block utilize caches. These memory accesses from a CUDA block are mapped into a CPU thread, so those memory accesses would also utilize CPU caches [17]; 3) threads within a block have similar computation patterns, which makes them amenable to the SIMD instructions [12,18] common in the current CPU architectures for further optimizations [19,25]. The transformation is shown in Figure 1(b): for an original GPU kernel, the translator first splits it into different regions according to synchronization instructions and then wraps each region with a loop whose size equals to the GPU block size. However, this transformation was proposed based on early GPU programming models and cannot support several important features that were proposed in recent GPU programming models. One of the significant changes is the warp-level programming model in CUDA [1]. And this new feature is critical for achieving high performance. hierarchical collapsing is proposed to support these warp-level features on CPUs. Although this might sound like a trivial extension, it is critical to identify new types of barriers in the warp level. And warp- and block-level barriers form a hierarchical relationship that complicates translating loops or branches into a CPU-friendly version. Throughout the paper, the focus is on the CUDA programming model. However, the same techniques would also be applicable to other SPMD programming models (e.g., OpenCL [26], HIP [1], DPC [2]). Based on hierarchical collapsing, a framework, COX, is implemented that efficiently executes CUDA programs with the latest features on X86 devices. COX also uses SIMD instructions explicitly to take advantage of the hardware features in the latest CPUs.

The main contributions of this paper as follows:

- propose hierarchical collapsing, which provides the correctness for mapping GPU programs that use warp-level functions to CPU programming models, and implement it with LLVM passes.
- extend the Parallel Region concept into the Hierarchical Parallel Region to provide the correct translation when the GPU programs have warp-level functions.
- implement the COX framework, which executes CUDA source code on CPUs. The framework includes a new LLVM pass that contains hierarchical collapsing and a lightweight runtime system.\(^1\)

---

\(^1\)Warp is now officially a part of the programming model instead of being a microarchitecture concept.

---

2 the frame will be released as an open source once the paper is accepted.

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Figure 1: The programming model for input CUDA SPMD and output CPU programs by flat collapsing and hierarchical collapsing

(a) GPU SPMD

(b) Output of flat collapsing

(c) Output of hierarchical collapsing
2 Background and Motivation

2.1 Running SPMD Programming Models on CPUs

The basic mechanism to support SPMD programming models on CPUs is to map a thread block/work-group to a CPU thread and iterate for the thread block/work-group using a loop \([5,7,12,21]\). Figure 1(a) and (b) show the input and output of the basic process. This transformation has different names in different projects: microthreading \([8]\), thread aggregation \([27]\), thread-fusion \([6]\), region-based serialization \([17]\), loop chunking \([28]\), and kernel serialization \([29]\).

In this paper, this transformation is called flat collapsing, as it uses a single loop to represent all threads within a block. The loop can be vectorized by the compiler, and multiple CPU threads (essentially multiple CUDA blocks) are executed in parallel on multiple cores using runtime system such as p-thread or openMP. When a GPU program contains synchronization primitives inside (e.g., `syncthreads()`), the loop needs to be split (loop fission).

Below is some of the terminologies used in \([5,7,12]\) to support this transformation in general cases:

- **Parallel Region (PR)**: These are the regions between barriers that must be executed by all the threads within a block before proceeding to the next region. Typically, loops are generated to wrap each PR. In Figure 1, statements-A and statements-B form two PRs.

- **Extra barrier**: Unlike explicit barriers that are inserted by programmers (e.g., `syncthreads()`), the flat collapsing inserts extra barriers that are necessary to define the Parallel Region. The flat collapsing groups instructions between barriers as PRs and wraps these PRs by loops. However, when barriers are present in the conditional statements, the situation becomes more complex. For example, to transform a CUDA kernel that has a barrier within an if–then construct, flat collapsing has to insert extra barriers in the original CFG so that it can get correct PRs in the further step.

The definition of Parallel Region in previous project for flat collapsing cannot support wrap-level features. The flat collapsing generates a single loop for each PR to simulate all threads within a block. This coarse-grain simulation cannot distinguish threads among different wraps. In this paper, an extension definition is proposed and used to support warp-level features. (See Section 3.5 for details.)

2.2 Warp-level Programming Features

2.2.1 Warp-Level Collectives

CUDA provides a list of warp-level collective functions, which are necessary when achieving high performance for reduction. This section introduces two of them that are commonly used in existing benchmarks.

- **Warp shuffle**: In early versions, although most GPUs have local memory and global memory to support data exchange between threads, there was no efficient way to exchange data among threads within a warp. To efficiently exchange data that is stored in registers, CUDA provides a series of warp shuffle instructions. When the warp shuffle instructions are invoked, a thread can send its local data to another thread in the same warp. Warp shuffle can be used with warp vote to write more flexible programs.

- **Warp Vote**: Instead of only exchanging data among threads within a warp, warp vote instructions can directly make logical reductions (e.g., all, any) for the local variables, controlled by the mask argument. These features, used with warp shuffle and cooperative group, are necessary to implement high-performance reduction kernels.

2.2.2 Cooperative group

In the early CUDA programming models, there are only two explicit groups of threads: block and grid. Users cannot easily organize a sub-group among a small group of threads within the block. NVIDIA proposed a new concept in CUDA 7.0 called cooperative group. The corresponding instructions allow users to group threads within a block and this group can further be used for data exchange. There are two kinds of grouping strategies: static and dynamic. For the static grouping, it is known whether a thread belongs to a group in compile time (e.g., group threads with index 0 and 1), while for dynamic grouping, it can only be known during runtime (e.g., group all activated threads).

2.2.3 Limitation of COX

This project focuses mainly on the compile-level transformation. Thus, only the static features can be addressed. The latest CUDA supports several dynamical features. For example, for warp-level collective operations, users can assign

\[\text{https://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#warp-shuffle-functions}\]
only a sub-group of threads within the wrap to do the collective operations. The sub-group is organized by a mask argument at runtime. For the cooperative group, users can also group all activated threads into a group at runtime. For these warp-level features, although these dynamic features provide more flexibility, they can be harmful for performance, as they may incur warp-divergence. Thus, most high-performance implementations\cite{30,31} use warp-level collectives and the cooperative group without warp-divergence. In the following sections, only the non warp-divergence use cases for these new features are of concern. For the same reason, only the aligned barriers\cite{35} are of concern. In other words, for a block/wrap barrier, it is assumed that all or none of the threads within a block/wrap can reach this barrier.

2.3 Motivation

Section 2.1 introduced the concepts of Parallel Region (PR) and extra barrier. This section discusses, with examples, the limitation of these concepts and how to extend them. Assume the input kernel shown in Code 1 and its block size is $b_{\text{size}}$. The code accumulates the variable $val$ within the first warp and stores the accumulated value in the first thread of this warp. Figure 2 illustrates an example of the last two iterations.

```
1  int val = 1;
2  if (threadIdx.x < 32) {
3      for (int offset = 16; offset > 0; offset /= 2)
4          val += __shfl_down_sync(-1, val, offset);
5  }
```

Code 1: Input GPU reduction kernel

Although none of the existing projects can support this kernel, it is assumed that flat collapsing would generate code with the following steps:

- group consecutive instructions between two barriers, and wrap each group with a for-loop whose length equals to the block size. In Code 2 there are three groups that are separately wrapped by three for-loops in line 3, line 6, and line 9. Please note that the loop in line 5 is from the source input;
- replace the use of threadIdx.x by the loop iteration variable $tx$;
- replicate variables (e.g., $val$) used by more than one group into an array form;

Unfortunately, these steps are insufficient to generate the correct CPU program for this GPU kernel. The key reason is that there are implicit warp-level barriers derived from $\text{shfl\_down}()$: each thread within a warp has to first calculate its $val$ and then invoke $\text{shfl\_down}()$ at the same time (see Section 3.2 for details). These warp-level barriers are inside a branch of an if–then construct, which creates a more complex situation. In previous projects, there are only block-level barriers, so it can safely be assumed that for each barrier instruction, all or no threads within the block can access it. Thus, it will just wrap the barrier instructions with for-loops with lengths $b_{\text{size}}$, and these for-loops are located in the branch of a if–then construct: if it is known at runtime that this barrier will be accessed, then the control flow will directly runs into this branch and execute the for-loop; or go to another branch otherwise. However, in the example, these warp-level barriers are only accessible for the threads in the first wrap. To get the correct result, one needs to not only wrap the barrier instructions with for-loops, but also replicate the control flow instruction in if–then construct (line 2 in Code 1 and insert them into line 7 and line 10 in Code 2). With the above modifications, Code 1 would become Code 2. These transformations are quite complex, even for the demo example, not to mention implementing it in compilers used for all possible CFGs. Based on the above analysis, hierarchical collapsing is proposed which produces Code 3. The concept is also illustrated in Figure 1(c). Compared with Code 2, Code 3 has two types of generated loops: the loop with induction variable $wid$ (line 4) is for the block level called inter-warp loop, while the inner loops with induction variable $tx$ (lines 5, 7, 12, 14) are for the warp level called intra-warp loop. With inter/intra warp loops, compared with a single-level loop for all threads within a block, the complexity of the generated code can be reduced:

4 https://docs.nvidia.com/cuda/parallel-thread-execution/index.html#parallel-synchronization-and-communication-instructions-bar

This example is a simplified version of reduction_kernel.cu in CUDA 10.1 SDK.
no longer needs to replicate and insert the if-then construct. Instead, it is maintained only with a simple loop peeling (line 10 in Code 3). With the low complexity, hierarchical collapsing can easily be implemented and integrated into compilers. In COX, hierarchical collapsing is implemented as a new LLVM pass to automatically transform the GPU kernels.

```c
1 int shfl_arr[32];
2 int val[b_size];
3 for (int tx = 0; tx < b_size; tx++)
4    val[tx] = 1;
5 for (int offset = 16; offset > 0; offset /= 2) {
6    for (int tx = 0; tx < b_size; tx++)
7        if (tx < 32)
8            shfl_arr[tx] = val[tx];
9    for (int tx = 0; tx < b_size; tx++)
10       if (tx < 32)
11          if (tx + offset < 32)
12             val[tx] += shfl_arr[tx + offset];
13 }
```

Code 2: CPU warp shuffle program generated by flat collapsing

```c
1 int shfl_arr[32];
2 int val[b_size];
3 bool flag[32];
4 for (int wid = 0; wid < b_size / 32; wid++) {
5    for (int tx = 0; tx < 32; tx++)
6        val[wid * 32 + tx] = 1;
7    for (int tx = 0; tx < 32; tx++)
8        flag[tx] = (wid * 32 + tx) < 32;
9    // loop peeling
10   if (flag[0]) {
11      for (int offset = 16; offset > 0; offset /= 2) {
12          for (int tx = 0; tx < 32; tx++)
13             shfl_arr[tx] = val[wid * 32 + tx];
14          for (int tx = 0; tx < 32; tx++)
15             if (tx + offset < 32)
16                val[wid * 32 + tx] += shfl_arr[tx + offset];
17      }
18   }
19 }
```

Code 3: CPU warp shuffle program by hierarchical collapsing

Below are several details worth mentioning:

- As the input CUDA kernel has a `shfl_down` inside an if-then construct, this is quite a complex situation: not all warps can access the implicit warp-level barriers derived from `shfl_down`. According to CUDA document, for a given warp-barrier, none or all threads within a warp can access it. Thus, loop peeling (line 10 in Code 3) is used to evaluate the condition of the if-then construct only for the first thread in the warp, and then all other threads in the warp just follow the same path. (See Section 3.3 for details);
- Although only `flag[0]` is needed, the instructions to calculate other elements in `flag` are also executed. Because these instructions may have a side effect, to guarantee the correctness, they have to be executed even these outputs are not needed;

The rest of this paper is organized as follows: Section 3 introduces the key part of the hierarchical collapsing. The runtime system is introduced in Section 4. Section 5 shows the evaluation of COX with CUDA SDK, heter-Mark, and GraphBig benchmarks and the comparison of the performance with POCL and DPC, which are the state-of-the-art open source frameworks. Section 6 provides a survey that describes various attempts to migrate GPU programs to CPU devices. Finally, concluding thoughts are presented in Section 7.

### 3 IR Transformation

#### 3.1 Overview of COX

Figure 3 shows an overview of the COX framework. At a high level, a CUDA kernel is compiled with Clang, which produces NVVM IR for the NVIDIA GPU. Then, COX transforms the NVVM IR into the CPU-friendly LLVM IR. The hierarchical collapsing is implemented in this transformer. After that, the LLVM IR is linked with host programs and runtime libraries to generate a CPU-executable file.

[https://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#synchronization-functions](https://docs.nvidia.com/cuda/cuda-c-programming-guide/index.html#synchronization-functions)
Figure 3: COX pipeline for generating CPU executable files from CUDA kernel codes.

| Step | Description |
|------|-------------|
| 1. **Global** | void VoteAll(int *result) |
| 2. | int tx = threadIdx.x; |
| 3. | result[tx] = __all_sync(-1, tx % 2); |
| 4. | } |
| 5. **Transformed LLVM-IR** | |
| 6. | We include a helper function in the runtime library to | |
| 7. | call the native warp barrier | |
| 8. | call the warp barrier | |
| 9. **Executable File** | |

Code 4: CUDA Warp Vote example

```
__global__ void VoteAll(int *result) {
    int tx = threadIdx.x;
    result[tx] = __all_sync(-1, tx % 2);
}
```

(a) Original Code.

Figure 4 shows an example of transforming CUDA kernels shown in Code 4 into a LLVM-IR for CPU. First, warp-level functions are replaced with built-in functions defined in the runtime library, as shown in Step 1 (Section 3.2). Second, in Step 2, the extra barriers are identified and inserted (Section 3.3). Last, through Steps 3 to 5, hierarchical parallel regions are identified, and intra/inter-warp loops are generated accordingly to create a CPU-friendly version (Section 5.4). After Step 5, the generated LLVM IR will be compiled and linked with host programs and runtime libraries to generate a CPU-executable file.

(d) Step 3: Split blocks by barriers.

(e) Step 4: Wrap the current CFG with intra-warp loop.

(f) Step 5: Wrap the current CFG with inter-warp loop.

Figure 4: Steps of NVVM to LLVM-IR transformer in Figure 3
### 3.2 Support Warp-level Functions

In a GPU architecture, when threads within a warp invoke the warp functions, the GPU will have internal communications to accumulate and communicate the local variables among the warp. To support these features on CPUs, the corresponding accumulation and communication need to be explicitly performed. This section describes how to support warp-level collectives.

In the initialization, COX allocates an array \( \text{warp\_vote} \) with length 32. The \( \text{warp\_vote} \) should be stored in CPU thread local memory, as a CPU thread is used to simulate a GPU block. Otherwise, if \( \text{warp\_vote} \) is stored in global memory that is accessible to all CPU threads, a data race can occur when multi CPU threads read/write the \( \text{warp\_vote} \) variable at the same time. A GPU warp vote instruction is translated to the following CPU instructions: for threads within a warp, first, each thread stores its local flag into a different element in \( \text{warp\_vote} \). After all the elements are set, the result for this warp vote can easily be computed. The function \( \text{warp\_all} \) is defined in a runtime library that will be linked at the final compilation. To utilize the computation resource of X86, \( \text{warp\_all} \) is implemented with the AVX instructions. The benefits brought by AVX are evaluated in Section 5.2.3. The ways to support warp shuffle are quite similar. See Code 1 and Code 5 for example.

COX also needs to insert the implicit warp-level barriers when supporting these warp-level functions. As discussed in [33], two warp-level barriers are required: barriers for the Read-after-Write (RAW) hazard and barriers for the Write-after-Read (WAR) hazard. The use of these two barriers is shown in Code 5. There are two consecutive warp vote instructions and the inserted barriers 1) without the barriers for RAW hazard, a thread will invoke \( \text{warp\_all} \) before other threads set \( \text{warp\_vote}[tx] \) to 1 (the first vote) or 2 (the second vote); 2) without the barriers for the WAR hazard, a thread will set \( \text{warp\_vote}[tx] \) to 2 before other threads invoke the first vote function. The use of consecutive warp-level collective functions is really common when implementing reduction.

### 3.3 Insert extra Barriers

In Steps 3, 4, and 5, hierarchical collapsing needs barrier information to identify the Parallel Region and generate intra/inter-warp loops accordingly. Thus, it is important to insert extra barriers that are not shown in the input GPU codes but necessary for identifying the Parallel Region. Some researchers [12] proposes a similar concept and corresponding algorithm, but they cannot support warp-level functions. The extra barriers are sourced from barriers in conditional statements. An example is shown in Figure 5.

![Figure 5: An example of extra barriers needed for identifying PRs. a) the input CUDA kernel, which has a barrier in for-loop construct; b) as there is a barrier in the conditional statement, extra barriers are inserted to guide the generation of intra/inter-warp loops in future steps; c) according to the barriers, two PRs are identified and two for-loops are generated separately. Note, all transformations in COX are done in the LLVM IR level. This source code level example is only used for explanation.](image-url)
To make the hierarchical collapsing work, extra block-level barriers are inserted at the beginning of the entry block and at the end of the exit block as POCL does [7].

The two most common conditional statements are If-Then construct and 2) For-loop construct.

### 3.3.1 Barriers in if–then construct

The CFG of a classical if–then construct is shown in left side of Figure 6(a). In the block if.body, there is a barrier. According to [34], for a block/wrap barrier, none or all threads within the block/wrap can reach it. Thus, COX can apply loop peeling on the CFG; COX peels the first thread to evaluate the branch direction and the rest of the threads within the warp/block can just follow the same direction. See Code 3 for a loop peeling example. The result after inserting extra barriers and block split is shown in the right side of Figure 6(a). Several details are worth mentioning:

- insert extra barriers with the same type as the barrier in if.body. In the example, there is a warp barrier in if.body, thus, hierarchical collapsing also inserts warp barriers as extra barriers;
- after transformation, all blocks will be wrapped by intra-warp loops, except if.cond, which is used for loop peeling;
- if.cond should contain only a single conditional-branch instruction and it should not have any side-effect. In Figure 6(a), all computation instructions are put into if.head so that they are executed b_size times, as the original GPU program does.

![Figure 6: After transformation, the inserted barriers are shown in bold. The PRs identified in further step are also shown in the figure.](image)

The detailed algorithm for inserting extra barriers derived from barriers in if–then construct is described in Algorithm[1]. COX has to do some additional checking to avoid an infinite loop caused by a for-loop construct in CFG. For simplicity this checking part is not shown in Algorithm[1].

---

7This rule does not exist for non-aligned barriers in CUDA, which is beyond the scope of this paper.
Algorithm 1 Transformation for inserting extra barriers for barrier in if-then construct

Input: $K$: The CFG for the input kernel
Input: $PDT$: The Post Dominator Tree for the input CFG
Input: $DT$: The Dominator Tree for the input CFG

1: $\text{conditional\_block} \leftarrow []$
\> Find all barriers in if-body construct
2: for all $block \in K$ do
3: \> if has\_barrier($block$) then
4: \> \> if !$PDT$.dominates($block, K.entry$) then
5: \> \> \> $\text{conditional\_block}.insert(block)$
6: \> \> end if
7: \> end if
8: end for
\> Insert extra barriers
9: for all $block \in \text{conditional\_block}$ do
10: $\text{NearestEntry} \leftarrow block.precessor$
11: \> $\text{NearestEntry} \leftarrow NearestEntry.precessor$
12: while $PDT$.dominates($block, NearestEntry$) do
13: \> $\text{NearestEntry} \leftarrow NearestEntry.precessor$
14: \> $\text{insert\_barrier\_before}(\text{predecessor.terminator})$
15: $\text{pre\_successor} \leftarrow block$
16: $\text{successor} \leftarrow block.successor$
17: while $DT$.dominates($block, successor$) do
18: \> $\text{pre\_successor} \leftarrow successor$
19: \> $\text{successor} \leftarrow successor.successor$
20: end while
\> Insert barrier in the beginning of if-exit
21: $\text{insert\_barrier\_before}(successor.begin)$
\> Insert barrier in the beginning of if-body
22: $\text{insert\_barrier\_before}($\text{pre\_successor.terminator}$)
\> Inserted extra barriers may generate another if-then construct that contains barriers
23: if !$PDT$.dominates($\text{NearestEntry}, K.entry$) then
24: $\text{conditional\_block}.insert(\text{NearestEntry})$
25: end if
26: end for

3.3.2 Barriers in for-loop construct

Although CUDA supports several loop styles (e.g., for-loop, while-loop, do-while-loop), after LLVM’s transformation, all loops will be simplified to the canonical format, which 1) has single latch; 2) has the loop headers dominating all exit blocks. Thus, COX only needs to concern these canonical loops.

COX inserts extra barriers before/after the branch instructions (back edge of the loop). Figure 6(b) shows the example of inserting extra barriers for a for-loop construct which contains a block barrier. The same as with an if-then construct, all these inserted extra barriers (shown by bold text in the figure) should have the same type as with the barriers in $\text{for\.header}$ (block barrier in the example).

3.3.3 Supporting other conditional statements

CUDA is a high-level flexible language; even a single concept can generate quite a different CFG. For example, the loop concept can be implemented by different CFGs, such as do-while-loop, while-loop, and for-loop. However, with the existing LLVM transformations, COX can automatically convert the input CFGs to canonical formats and only focus on these canonical formats in the above discussion. Below are some important features in the canonical format:

---

8 A latch is a node in the loop that has an edge to the loop header. An exiting edge is an edge from inside the loop to a node outside of the loop. The source of such an edge is called an exiting block, its target is an exit block. [35]
• Each branch instruction has only two successors; most input CFGs already have this feature, except the CFG which uses switch-case construct. For these exceptions, COX uses LLVM’s lowerswitch transformation to convert the switch-case construct into if–then constructs.

• All loops are in canonical format that 1) they all have pre-headers; 2) each loop has only a single latch, in other words, a single backedge; and 3) the loop header will dominate all exit blocks. COX calls LLVM’s loop — simplify transformation to translate the input CFG loops to the canonical format.

3.4 Split Blocks Before/After Each Barrier

As the instructions before/after a barrier in a block need to be wrapped by different intra/inter-warp loops, in this step, COX splits the blocks that have barriers inside. See Step 3 in Figure 4 for an example.

3.5 Hierarchical Parallel Region

As discussed in Section 2.3, each parallel region (PR) becomes a for-loop. Due to the warp-level functions, COX has to generate two kinds of for-loops: inter-warp loop and intra-warp loop. Thus, COX needs two kinds of Parallel Regions: 1) warp-level Parallel Region, which will be wrapped by intra-warp loop and 2) block-level Parallel Region, which will be wrapped by inter-warp loop. It is obvious that a warp-level PR will always be a subset for a block-level PR (a GPU warp is always within a GPU block); thus, the new concept is called a Hierarchical Parallel Region. An example of a Hierarchical Parallel Region is shown in Figure 7.

Figure 7: As there is a warp barrier in block1, after transformation, there are two warp-level PR ({ block1},{block2}) and a single block-level PR ({block1, block2}).

Thus, the rest of the steps are for finding the block/warp level PRs and wrapping them with inter/intra-warp loops. The algorithm (Alg. 2) is used for finding the set of warp-level PRs. The algorithm for finding the block-level PRs is very similar, except it only concerns the block barrier. COX cannot find the PR for the warp level and block level simultaneously: COX first finds all warp-level PRs and generates intra-warp loops to wrap these PRs. Then, COX finds the block-level PRs in the new CFG and wrap them with inter-warp loops.

3.6 Wrap PR with For-Loop

In this step, COX wraps warp/block-level PRs by intra/inter-warp loop. Please see Figure 4(e)(f) for an example. Although this step is quite straightforward, it requires proving the correctness after inserting intra/inter-warp loops, each instruction from the input GPU kernel is executed b_size times (b_size is the block size), except the instructions used for loop peeling.

Finally, after adding intra/inter-warp loops, some local variables are needed to be replicated: for local variables that are used in several warp-level PRs but only used in a single block-level PR, they are replicated with an array of length 32. For local variables that are used among different block-level PRs, they are replicated by an array of length equals to block size.

9Due to page limitation, we move the proof into Appendix
Algorithm 2 Find all warp-level PRs

Input: $K$: The CFG after Step3
Output: $PR_set$: The set of PRs.

1: $PR_set ← \{\}$
2: $end\_block ← []$
3: for all $block ∈ K$ do
4:   if $block$ contains warp/block barrier then
5:     $end\_block$.insert($block$)
6: end if
7: end for

8: for all $block ∈ end\_block$ do
9:   if $block$ has more than one predecessors then
10:     continue
11: end if
12: $PR ← \{block\}$
13: $pending\_block ← block$.precessors
14: while $!pending\_block$.empty() do
15:   current ← $pending\_block$.front()
16:   $pending\_block$.pop()
17:   if has visited current then
18:     continue
19: end if
20: if current has warp/block barriers then
21:   continue
22: end if
23: $PR$.insert(current)
24: $pending\_block$.insert(current$.preproccessors$)
25: end while

26: if $PR$ only has a single block which only contains a conditional branch then
27:   continue
28: end if
29: $PR_set$.insert($PR$)
30: end for

4 Runtime System

The above section describes only the CUDA device part. As for the CUDA host part which involves memory allocation, memory transfer, and kernel launch, these features has to be manually migrated. The automatic translation from CUDA host code to CPU is left for future work. In the runtime system, p-thread is used for multi-threads. In this paper, both host and device are x86; thus, CUDA malloc and memcpy are replaced by C malloc and memcpy. In Figure 8(a), a CUDA host example is presented for vector copy. The migrated COX host code is shown in Figure 8(b), with the corresponding CUDA operations recorded in the comments. Compared with the CUDA host program, the COX host program has the following differences: 1) COX uses thread-local variable $block\_index$ to store the block index, and the block index is explicitly set during invocation; 2) COX replaces the CUDA memory operations with corresponding CPU operations; 3) COX uses pthread fork/join to replace kernel launch in CUDA. There are several potential optimization for the runtime system, such as using thread-pool instead of fork/join for kernel launching and using regular expression or LLVM transformation to automatically generate COX host programs from the CUDA source code. These optimizations are beyond the scope of this paper and are open for future research.

The following steps make up the workflow for COX: It 1) compiles the input CUDA source code with Clang and gets the NVVM IR of kernel functions and; 2) transforms the NVVM IR with hierarchical collapsing; 3) links the transformed kernel with the COX host program (manually migrated from CUDA host program) and generates the CPU-executable file. COX has two modes: 1) normal mode to maintain the runtime configuration as variables (e.g., grid size, block size) and 2) JIT mode to compile the program with the given runtime configuration. In the normal mode, COX only needs to compile programs once, and it can be used for different runtime configurations. In JIT mode, a program has to be recompiled when executed with different configurations. Although the JIT mode requires recompiling, in some cases,
int main()
{
    int n = 1024;
    int grid_size = n/1024;
    // Host input vectors
    int *h_a, *h_b;
    // Device input vectors
    int *d_a, *d_b;
    // Size, in bytes, of each vector
    size_t bytes = n*sizeof(int);
    h_a = (int*)malloc(bytes);
    h_b = (int*)malloc(bytes);
    cudaMalloc(&d_a, bytes);
    cudaMalloc(&d_b, bytes);
    cudaMemcpy(d_a, h_a, bytes, cudaMemcpyHostToDevice);
    cudaMemcpy(d_b, h_b, bytes, cudaMemcpyHostToDevice);
    vecCopy<<<grid_size, 1024>>>(d_a, d_b);
    cudaMemcpy(h_b, d_b, bytes, cudaMemcpyDeviceToHost);
    cudaFree(d_a);
    cudaFree(d_b);
    return 0;
}

(a) CUDA host code.

int main()
{
    int n = 1024;
    int grid_size = n / 1024;
    // Host input vectors
    int *h_a, *h_b;
    // Device input vectors
    int *d_a, *d_b;
    // Size, in bytes, of each vector
    size_t bytes = n * sizeof(int);
    h_a = (int*)malloc(bytes);
    h_b = (int*)malloc(bytes);
    d_a = (int*)malloc(bytes); // cudaMalloc(&d_a, bytes);
    d_b = (int*)malloc(bytes); // cudaMalloc(&d_b, bytes);
    cudaMemcpy(d_a, h_a, bytes, cudaMemcpyHostToDevice);
    cudaMemcpy(d_b, h_b, bytes, cudaMemcpyHostToDevice);
    vecCopy<<<grid_size, 1024>>>(d_a, d_b);
    cudaMemcpy(h_b, d_b, bytes, cudaMemcpyDeviceToHost);
    cudaFree(d_a);
    cudaFree(d_b);
    return 0;
}

(b) Migrated COX host code.

Figure 8: The host code in COX is similar with the original CUDA host code. The automatic migration from CUDA host code to COX host code is open for future work.
it can generate higher-performance programs, as it provides more opportunities for optimizations. For more details, please see Section 5.2.2.

5 Experimental Results

To verify the correctness and performance, this section describes the experiments for supporting the CUDA kernel in several benchmarks on X86 and ARM architectures. Although several frameworks also support executing CUDA on CPU, most of them were developed decades ago and cannot really support programs that use new CUDA features. Below are the hardware and software environments for the experiments:

- Software: Ubuntu 18.04, LLVM 7.5.0, CUDA 10.1, POCL 1.4, DPCT [2] Ver. : 2021.3.0.
- X86-Hardware: 8 x Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
- ARM-hardware: 48 x ARM(R) A64FX CPU @ BogoMIPS 200.00
- Benchmarks: CUDA SDK 10.1, Hetero-mark [36], GraphBig [31];
- Time: average time for running more than 1000 times; fork/join time of threads is also included.

5.1 Coverage

Table 1 analyzes examples in CUDA SDK10.1 that use but do not require special hardware support (e.g., tensorcore, unified memory). POCL and DPCT are chosen for the coverage comparisons since they are the currently activated projects that support executing CUDA programs on CPUs. As POCL is designed for OpenCL and cannot directly execute CUDA programs, a third-party translator [37] is used to support executing CUDA with POCL. Besides, although POCL has both compilation and runtime parts, only the compilation is used in this experiment. For POCL evaluation, the GPU programs is compiled by POCL and then executed on COX. Thus, it's fair to compare the execution time to show the results of compilation and avoid the effect of runtime system.

As shown in the table, the existed frameworks can only automatically support at most 21 kernels (coverage=68%). Those failed kernels are using new CUDA features. On the other hand, COX supports 28 kernels (coverage=90%).

| Kernel name     | Features                      | POCL | DPCT | COX |
|-----------------|-------------------------------|------|------|-----|
| initVectors     |                               | x    | x    | x   |
| gpuDotProduct   | warp cooperative group        |      |      |     |
| gpuSpMV         |                               |      |      |     |
| r1_div_x        |                               |      |      |     |
| a_minus         |                               |      |      |     |
| gpuConjugateGradient | grid sync           |      |      |     |
| multiGpuConjugateGradient | multi grid sync |      |      |     |
| MatrixMulCUDA   |                               |      |      |     |
| matrixMul       |                               |      |      |     |
| copy2pq         |                               |      |      |     |
| reduce0         | block cooperative group       | x    |      |     |
| reduce1         | block cooperative group       |      | x    |     |
| reduce2         | block cooperative group       | x    |      |     |
| reduce3         | block cooperative group       |      | x    |     |
| reduce4         | warp cooperative group        | x    | x    | x   |
| reduce5         | warp cooperative group        | x    | x    | x   |
| reduce6         | warp cooperative group        | x    | x    | x   |
| shift_intimage_rows | warp shuffle                 | x    |      |     |
| shift_vertical_shift | warp shuffle                 | x    |      |     |
| shift_scan_test | warp shuffle                  |      | x    |     |
| uniform_add     |                               |      | x    |     |
| reduce          | warp cooperative group        | x    |      |     |
| reduceFinal     | warp cooperative group        | x    |      |     |
| simpleKernel    |                               |      |      |     |
| voteAnyKernel1  | warp vote                     |      |      |     |
| voteAllKernel2  | warp vote                     |      |      |     |
| voteAnyKernel3  | warp vote                     |      |      |     |
| spinWhileLessThanone |                  |      |      |     |
| matrixMultiplyKernel |                        |      |      |     |
| vectorAdd       |                               |      |      |     |
| filter_arr      | activated thread sync         |      |      |     |

Table 1: Coverage of COX compared to other frameworks. *enabled by manual code migration [38]

The CUDA features supported by POCL, DPCT and COX is also shown in Figure 9.

Although the coverage with COX can be significantly improved, there are still three kernels that cannot be supported yet. `gpuConjugateGradient` and `multiGpuConjugateGradient` rely on synchronization between different grids and devices, which utilize the grid cooperative group and multi-grid cooperative group separately. `filter_arr` uses a dynamic cooperative group: it dynamically groups all activated threads. As discussed in Section 2.2.2, all these features
should be supported at the runtime level: frameworks should schedule threads accordingly at runtime, and each thread can only know whether it is activated during runtime. Supporting runtime features is included for future work.

5.2 Performance

Figure 10 shows a performance comparison of POCL, DPC, and COX on CUDA SDK, Hetero-Mark, and GraphBig benchmark on X86 architecture.

In most cases, COX and POCL have close execution time. Thus, the POCL’s normalized execution times are always close to 1. However, DPC’s normalized execution time has large variance. This is due to: 1) DPC’s most optimizations are for multiple block cases, which are runtime optimization. While in the evaluation, to shown the compile-level optimization, there is only a single block in each application; 2) DPC has optimizations on new Intel CPUs, while POCL and COX do not have special optimizations for the new Intel architectures.

The evaluation results for ARM CPU with AArch64 architecture is shown in Figure 11. As DPC does not support ARM CPU, only POCL and COX are evaluated. The performance between COX and POCL are close among all experiments.

5.2.1 Performance effects of flat collapsing vs. hierarchical collapsing

Although hierarchical collapsing can support wrap-level features, it generates nested loops instead of a single loop as flat collapsing does. The complex nested loops incurs more instructions and also makes it difficult to do some optimizations. Figure 12 shows the overhead of hierarchical collapsing over flat collapsing on X64 architecture, for three micro-benchmarks by varying the vector/matrix sizes, and none of these three benchmarks use warp-level functions. As the results show, hierarchical collapsing downgrades performance by 13% on average due to additional instructions. Hence, COX uses hybrid-mode: for each input kernel, first checks whether there are warp-level functions or other features for which cannot be supported by flat collapsing. If not, flat collapsing is used in default.
5.2.2 Normal mode vs JIT mode

Loop optimization is an important optimizations for high-performance programs. Although the intra-warp loop’s length is always 32, the inter-warp loop’s length depends on the block size, a runtime configuration. COX supports two compile modes: normal mode and JIT mode. Although the programs generated by these two modes will both forward to LLVM’s optimizer (with \(-O3\) flag), they have an obvious difference, especially when compiling complex kernels. Figure 13 shows the difference in execution time between two modes. These two modes have a relatively small difference for the VectorAdd kernel, as it is quite simple and can easily be vectorized with compiler optimization even the block size is not provided at compile time. However, for more complex kernels, JIT mode generates programs with higher performance.
Table 2: Both functions gain around 10x speed up when using AVX instructions.

### 5.2.3 SIMD instructions

For CPU programs, SIMD instructions are necessary to achieve high performance [18, 39–41]. The warp vote function execution time with/without AVX is shown in Table 2. With AVX instructions, around 10x speedup is achieved for both functions. The benefit is due to fewer instructions and branches.

### 5.2.4 Scalability

Besides the single block execution time, the execution time for multi-block cases are also measured and the result is shown in Figure 14. In the Hetero-mark benchmark, the kernels have fixed block sizes. Thus, to enlarge the grid size, workload size is also enlarged. As the X86 platform has eight CPU cores; the speed up significantly degrades when the grid sizes are larger than eight. Up to eight, it shows good scalability.

![Figure 14: Multi-core execution time with COX.](image.png)

### 6 Related Work

The CPU architecture belongs to MPMD, while the GPU architecture is SPMD. Although users can naively execute a GPU thread with a CPU thread, due to the limited parallelism in CPU, the system can only execute around 100 CPU threads simultaneously, which is much smaller than the parallelism in the GPU architecture. Thus, to achieve the same number of threads as a GPU, the CPU has to create more threads than it can actually execute simultaneously, which will incur a large amount of thread context switching overhead. Two methods solve this issue. The first is to accelerate the context-switching time in the CPU. Some researchers extend the CPU architecture to accelerate the context switching [15], these hardware-level extensions are beyond the scope of this paper. In the software level, [16] proposes to use lightweight threading to accelerate the context switching. Context switching only stores and reloads a few registers, while maintaining the stack memory. Most modifications are in the runtime level, and users can directly use the original GPU source code. As reported in [17], the AMD CPU OpenCL implementation is based on this technology. However, even with these optimizations, there is still significant overhead for context switching, around 10ns per switching.

Thus, another direction is being explored: increasing the workload of each CPU thread. For each CPU thread, instead of executing a single GPU thread, it executes whole GPU threads within a block. This mechanism can elicit two benefits: 1) it can increase the CPU execution time to make it much larger so that context switching overload becomes negligible; 2) with more workload in a single thread, there are more opportunities to do optimizations (e.g., vectorization, loop transformation). This mechanism has several different names: microthreading [8], thread aggregation [27], thread-fusion [6], region-based serialization [17], loop chunking [28], and kernel serialization [29]. In this paper, this mechanism is given a new name: flat collapsing. In [5][8], the authors propose to wrap an SPMD kernel
with a loop, and the loop size is equal to the block size. Thus, each loop iteration can simulate a GPU thread within a block, and the CPU thread is mapped to a GPU block. An important technical detail is supporting synchronization instructions: compilers should separately wrap instructions before/after a synchronization instruction into different loops to maintain the correctness. A similar technology is also discussed in [28] which utilizes loop transformations (e.g., loop strip-mining, interchange, distribution, unswitching) to transform SPMD execution models with synchronization to Task Parallel execution models. The authors in [27] propose improved static analysis to vectorize the generated loop-programs to improve the performance, and also propose another algorithm to wrap the original kernels with loops to avoid additional synchronization points in previous works. In some GPU architectures, such as NVIDIA GPU, there is implicit lock step within a group of threads. [42] proposed transformations to detect these implicit warp-level synchronizations and maintained them during transformations. The authors in [17] propose to use C Extensions for Array Notation to further accelerate the generated CPU programs with SIMD execution and better spatial locality. Several projects have been proposed to execute CUDA on non-NVIDIA devices. In the early days, NVIDIA provided an emulation framework [14] to execute CUDA on a CPU; each thread within a GPU block is executed by a CPU thread. Horus [43] is another emulator. It supports parsing and executing NVIDIA PTX instructions on CPU devices. These emulators are for debugging rather than for performance. In MCUDA [5], the authors also use a source-to-source translation to translate CUDA to C with the flat collapsing mechanism. Ocelot [6] uses the same mechanism, but instead of source-to-source translation, it converts in the PTX level to avoid recompiling. MapCG [44] is a hybrid computing framework. It uses source-to-source translation to translate CUDA kernels to C programs, which can be executed on a CPU. [45] proposes another framework for hybrid-computing based on Ocelot to translate GPU programs on the PTX level. Cumuls [29] uses Clang to parse the CUDA programs and modifies them on AST level. Cumuls is mainly concern on CUDA runtime support, as for compilation part, it reuses the transformation in MCUDA. Instead of directly translating CUDA/PTX to CPU executable files, other projects utilize the portability of other front-end languages. The authors in [46, 47] propose using source-to-source translation to translate CUDA to OpenCL. Instead of source-to-source translation, [37, 48] implements the translations with LLVM IR. DPC++ Compatibility Tool [2] and HIPIFY [9] are frameworks that translate CUDA to source languages for Intel and AMD devices. Most related works only focus on supporting old CUDA features. However, the rapid evolution of GPU hardware and software stacks bring lots of new features which are important to achieve high performance, such as warp-level collectives, unified memory and CudaGraph. Achieving high coverage on these new features is still an ongoing project. The researchers in [33] propose to use explicitly barriers and memory exchanges to support warp shuffle on OpenMP, which shares the same insight with COX. OpenCL is another framework that supports executing SPMD programs on MPMD architectures. POCL [7] is an open source OpenCL implementation which supports CPU backend. To support SPMD programs on CPU, POCL implements flat collapsing on LLVM IR level. The authors in [12] also proposes to use flat collapsing on OpenCL, but with a different method to insert extra synchronization and find parallel region which result in fewer extra synchronization barriers. However, this method is not extendable for Hierarchical Parallel Region, thus, cannot be utilized to support warp-level features. In [49], another OpenCL implementation has been proposed, which mainly focus on support OpenCL programs on multi-device clusters with heterogeneous devices.

7 Conclusion

This project proposes and builds COX, a framework that supports executing CUDA kernels on CPU devices. It also proposes hierarchical collapsing which can be used to transform SPMD programs to MPMD friendly programs and it supports the latest warp-level functions in CUDA. Using CUDA 10.1 Sample as a benchmark, the previous projects can only support 21 of 31 kernels (coverage=68%), while COX can support 28 (coverage=90%). The kernel performance is also compared on X86 and AArch64 architectures and shows that the performance is comparable. COX is based on compile-time transformation. Future work will provide a runtime system to support other CUDA features.
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A Proof of the generation kernel

In this section, we prove that after inserting intra-warp loops and inter-warp loops, each instruction from the input GPU kernel is executed $b\_size$ times ($b\_size$ is the block size), except the instructions used for loop peeling.

Proof1: For if-body/for-body that contains a warp/block barrier, their conditional branch instructions do not belong to any warp/block-level PR

For if-then construct after Step 3, we insert barriers in the end of if-head (barrier in if\_head), the beginning of if-exit (barrier in if\_exit) and the end of if-body (barrier in if\_body2), shown in Figure 6(a). As for for-latch, we insert two barriers around the conditional branch instruction, as shown in Figure 6(b). For if\_cond, it can only be included in PR together with if\_body1 or if\_exit. For if\_exit, it has two predecessors, thus we will ignore it line10 in Alg. 2. As for if\_body1, as it does not post-dominate if\_cond, it will not include if\_cond into the PR. The proof of for\_cond is quite same.

Proof2: All other blocks must belong to one and only one warp/block-level PR

This paragraph only proof the block-level PR. The warp-level PR is quite similar. First, let us prove a block can only belong to at most one block-level PR. If a block $B$ belongs to more than one PRs, this block must be the ancestor of two blocks that both have block-level barriers. Assuming the block NCA is the nearest common ancestor of these two blocks in the control flow graph, it is obvious that NCA is the head of an if-then-construct or the latch of a for-construct. However, from the Proof1, we know neither of them belongs to any PR. In other situations, if a block $B$ doesn’t belong to any PR, it means all nodes that post-dominates $B$ do not have a block-level barrier. However, in Step2, we insert a block-level barrier at the end of the exit block. And exit block will always post-dominates $B$. 

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