Low-Loss Active Grid Impedance Cancellation in Grid-Connected Inverters with LCL Filter

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Article

Abstract: Distributed power inverters with inductive capacitive–inductive (LCL) filters have become popular in distributed power generation system. However, due to unknown grid impedance, the inverters are confronted with challenges of local filter resonance, poor power quality, and multiple interactive resonance. This paper proposes a low-loss active compensator that can counteract effects of the grid impedance on the current control performance of single-phase grid-connected inverter with an LCL filter. The compensator utilizes dual unit point-of-common-coupling voltage feedforward control mechanisms (VFFC), in which one is integrated with the inverter controller, and the other is generated through an extra low voltage source converter (LV-VSC) in series with the filter capacitor. The LV-VSC has no additional passive inductive-capacitive filtering elements and provides very low volt-ampere. To confirm its validity, a single-phase inverter testbed integrated with the compensator was built. The experimental results validate the current-controlled performance enhancement of the proposed inverter system operating under different grid conditions.

Keywords: inverters; LCL filter; grid impedance; weak grid; active compensator

1. Introduction

Distributed renewable energy resources are commonly connected to the power grid through a current-controlled voltage source inverter (VSI) via an output power filter, such as inductive capacitive–inductive (LCL) filter [1,2]. Due to the filter resonance, the grid current regulation of these VSIs faces a critical challenge of system stability. To alleviate such concerns, the prior arts aimed to reshape the inverter equivalent output impedance by passive or active damping approaches. The passive damping method acts on the LCL filter by inserting the impedance around the filter resonant frequencies at the expense of additional power loss and degradation of filtering attenuation [3–5]. The active damping (AD) approach is to integrate the damping function into the inverter control so that the inverter equivalent output impedance around the filter resonant frequencies or over the frequency range is increased [2,6–13]. Among them, active damping methods are preferred because no additional power consuming resistor is required. However, the performance of active damping in the digitally controlled inverter is sensitive to the ratio between the sampling frequency and the filter resonant frequency [11]. Even worse, the variation of equivalent grid impedance under different grid conditions changes the filter resonant frequency a lot. Thus, more considerations should be paid to wide variation of the ratio between the sampling frequency and the filter resonant frequency [14]. In prior arts, the issue regarding unknown grid impedance was further alleviated by using some improved damping methods, such as robust or hybrid damping schemes [15–17].

Due to the existence of equivalent grid impedance, multiple distributed inverters interfacing to the grid with high-order LCL filters, as presented in Figure 1, could exhibit multiple interactive resonance [18,19]. The multiple interactive resonances are composed of internal filter resonance,
parallel resonance among inverters, and series resonance with the grid. Thus, the distributed power generation system (DPGS) in Figure 1 faces severe challenges of local filter resonance, background harmonics, and multiple interactive resonance [19]. Even when a single inverter is designed to suppress the local filter resonance and comply with the stability requirements, multiple distributed inverters together can have harmonic interactions in the DPGS. Auxiliary converters based on the concept of active damping are helpful to suppress multiple resonances at the point-of-common-coupling (PCC), such as resistive-active power filter (R-APF) [20] and adaptive parallel hybrid-active power filter (P-APF) [21]. However, they do not address the dynamic interaction among sources and/or loads at the same PCC. The dynamic interaction among them impacts the stability and power quality of the DPGS. A well-established technique to analyze such interactive stability problem is by the impedance-based analytical approach: the ratio of the converter output impedance to the load input impedance must satisfy Nyquist stability criterion in order for the DPGS to be stable [22,23]. In the DPGS, an impedance-based analytical approach is usually applied to incorporate multiple paralleled inverters into a single inverter based on the assumption that all paralleled inverters together with their control function are equal [24,25], but it becomes difficult to use when DPG inverters are not equal because the system with different inverters requires a complicated reformulation of the system description [26].

As previously described, the existence of grid impedance is the critical factor to challenge the suppression of the local filter resonance, arouse the multiple interactive resonance, and aggravate the injected power quality of the DPGS [27,28]. A well-known method is to utilize the PCC voltage feedforward control to ease such dynamic interaction between inverters and the grid and improve the power quality of the inverter. However, it has been proven that the unit PCC voltage feedforward control method weakens the inverter stability due to the effect of digital delay [29]. Therefore, the PCC voltage feedforward control method with reduced digital delay is studied to cancel the negative real part of the inverter output admittance according to passivity-based stability approach [30]. In references [31,32], a full PCC voltage feedforward control technique is also proposed to counteract the effect of grid impedance and maintain wide control bandwidth of inverters through a full-order state observer, but it faces the challenge of filter parameter drifting and noise amplification due to the differentiator. Recently, unit capacitor voltage feedforward with converter-side current regulation is also presented to sustain the inverter control bandwidth and decouple the effect of grid-side impedance, wherein the digital delay is effectively compensated through the lead compensator [33]. The problem is that the resonance caused by grid-side inductor and filter capacitor still challenges the inverter stability. In reference [34], an active circuit in series at the inverter output is used to mimic the negative grid impedance and cancel the effects of grid impedance on the dynamic interaction between inverters and
the grid. By doing so, the stability of the grid-connected inverter is guaranteed regardless of the value of grid impedance and the number of parallel inverters. Because the additional circuit is in series at the inverter output, the cost and power loss increase with the inverter output power.

The fundamental contribution of this paper is to develop a low-loss active compensator to counteract the negative effects of grid impedance on current-controlled single-phase grid-connected VSI with an LCL filter. The active compensator is realized through a dual unit PCC voltage feedforward control mechanisms (VFFC), in which one is inserted into the inverter current control and the other generates voltage regulation of an additional low voltage source converter (LV-VSC) in series with the filter capacitor. The LV-VSC has no extra passive filtering elements and provides very low volt-ampere (VA). Thus, the inverter efficiency is not sacrificed. The rest of this paper is organized as follows. In Section 2, the rationale of the grid impedance compensator is elaborated. Then, the control strategy is thoroughly elucidated, and the system modeling is studied in Section 3. Simulation results are given in Section 4, and a single-phase inverter prototype with the compensator is built and evaluated in Section 5. Its steady-state and transient behaviors under different grid conditions are examined. Conclusions follow in Section 6.

2. Configuration of the Proposed Grid Impedance Compensator

2.1. Review of the Grid Impedance Compensator

A simplified circuit structure of single-phase grid-connected voltage source inverter (GC-VSI) is given in Figure 2, where \( Z_1(s) = sL_1 \), \( Z_2(s) = sL_2 \), and \( Z_C(s) = 1/sC_f \). The corresponding control block diagram with the grid current control loop can be presented in Figure 3a, where \( G_f(s) \) means the digital delay, and \( G_C(s) \) is the current controller. To simulate the worst case, no resistive parts in the filter parameters and equivalent grid impedance \( Z_g \) are considered. Such an assumption has no effect on the analytical results in the following studies. For simplicity, the inverter gain is assumed to be unity.

![Figure 2. A simplified single-phase GC-VSI.](image)

![Figure 3. Control block diagram of single-phase GC-VSI. (a) Single-loop grid current regulation; (b) Active cancellation of grid impedance in reference [34].](image)

In terms of ac small signal, the cancellation of the grid impedance is to decouple the injected disturbance signal \( \Delta U_{pcc} \). As shown in Figure 3b, use of a unit PCC voltage feedforward can counteract the effect of grid impedance, where the PCC voltage is inserted to the inverter output at the node...
2.2. Derivations of the Proposed Low-Loss Grid Impedance Compensator

The circuit in Figure 4 can be simplified into the one as given in Figure 5a, where the output voltage of the compensator equals \( u_{\text{pcc},h} \). According to Kirchhoff’s voltage law (KVL), the circuit in Figure 5a can be written as the following equations:

\[
\begin{align*}
    u_C &= u_{\text{pcc}} + u_{L_2} - u_{\text{pcc},h} \quad (1) \\
    u_i + u_{L_1} &= u_{\text{pcc}} + u_{L_2} - u_{\text{pcc},h} \quad (2)
\end{align*}
\]

where \( u_{L_1} \) and \( u_{L_2} \) represent the voltage across the inverter-side inductors \( L_1 \) and \( L_2 \), respectively. Equations (1) and (2) can be rewritten as the following equations:

\[
\begin{align*}
    u_C + u_{\text{pcc},h} &= u_{\text{pcc}} + u_{L_2} \quad (3) \\
    (u_i + u_{\text{pcc},h}) + u_{L_1} &= u_{\text{pcc}} + u_{L_2} \quad (4)
\end{align*}
\]

C. In [34], Figure 3b is realized through an active compensator of grid impedance as illustrated in Figure 4, in which an LV-VSC is in series at the inverter output to provide the required injected voltage, \( u_{\text{pcc},h} = u_{\text{pcc},h} \). Because the LV-VSC is in series at the inverter output as shown in Figure 4, the cost and power loss of the circuit increases with the inverter output power.

\[u_{\text{pcc},h} = u_{\text{pcc},h}\]
Thus, the added voltage source in series at the inverter output, \( u_{\text{pcc,h}} \), is divided into two equivalent voltage sources as shown in Figure 5b, where the one is in series with the inverter output voltage \( u_o \), and the other is in series at the filter capacitor branch. It indicates that the grid impedance cancellation can be realized through two separate PCC voltage feedforward mechanisms, as presented in Figure 5b. The equivalent control block diagram of Figure 5b is presented in Figure 6a, in which the two equivalent voltage sources are inserted through the nodes A and B, respectively. For simplicity, the PCC voltage harmonic extraction at nodes A and B is not revealed in Figure 6a.

\[ u_A, B = u_o, \quad u_{\text{pcc}}, \quad u_{\text{pcc}}, h \]

Figure 6. Configuration of the proposed grid impedance cancellation. (a) Control block diagram; (b) Circuit diagram.

Therefore, the circuit realization of the proposed grid impedance cancellation is drawn in Figure 6b, where \( u_{A} = u_{\text{pcc}} \) is feedforwarded to the modulator of the inverter and \( u_{B} = u_{\text{pcc}}, h \) is implemented through an active voltage-controlled voltage-source (VCVS) in series at the filter capacitor branch. The power stage of the VCVS is realized through a LV-VSC in series with the filter capacitor as shown in Figure 7. Because the capacitor current through the LV-VSC is small, the proposed LV-VSC is expected to consume much lower power loss than the one as shown in Figure 4.

![Circuit diagram](image)

Figure 7. Circuit illustration of the proposed low voltage source converter (LV-VSC) to generate \( u_{o, B} \).

3. System Control and Modelling with the Proposed Compensator

According to Figure 6b, the operation principle of the proposed inverter system includes (1) output voltage regulation of the LV-VSC and (2) grid current regulation of the GC-VSI. Figure 8 presents the details of such control mechanism. In the following subsection, regulation of the LV-VSC and the system modeling will be introduced.
3.1. Regulation of the LV-VSC

3.1.1. AC Voltage Regulation

Because there are no additional passive LC filter elements in the LV-VSC, the added voltage, \( u_{o,B} \), is the output voltage of the LV-VSC and can be realized directly through a unit PCC harmonic voltage feedforward control as shown in Figure 8. The harmonic voltage components of \( u_{pcc} \), \( u_{pcc,h} \), are extracted through a notch filter with the center frequency \( \omega_0 \) shown in Figure 8.

3.1.2. Active Damping Function

Although the PCC harmonic voltage, \( u_{pcc,h} \), has been feedforwarded to the modulator of the LV-VSC to generate the required voltage, \( u_{o,B} \), the stability of the LV-VSC still faces the challenge of filter resonance caused by the LCL filter. Thus, the active damping function is integrated into the LV-VSC controller and suppresses the filter resonance. Among different active damping schemes, the capacitor current-based active damping is preferred to provide a virtual resistor in series at the filter capacitor branch. As shown in Figure 8, \( R_v \) is the active damping gain or the virtual resistance in series at the filter capacitor branch. According to the design criterion in reference [4], the optimal value of \( R_v \) is designed based on the filter resonant frequency. In our case study, it can be designed at the value of 30 \( \Omega \).

3.1.3. DC Capacitor Voltage Regulation

The dc capacitor voltage of the LV-VSC can be regulated by balancing the absorbed and released energy through the LV-VSC. As discussed above, the LV-VSC absorbs high-frequency components to emulate the virtual resistance \( R_v \) and eliminate the effects of equivalent grid impedance. As shown in Figure 8, the absorbed high-frequency power is transformed to the line-frequency component by generating a voltage signal in phase with the line-frequency component of the capacitor current so that the dc capacitor voltage is sustained. To make the dc capacitor voltage track the reference value, \( u_{dc,ref} \), precisely, the PI controller is adopted. The control bandwidth of dc capacitor voltage regulation can be chosen much lower than the line frequency and does not interact with the inverter current control [35].
3.2. Modeling Analysis of the Active Compensator

3.2.1. Calculation of the feedforwarding voltage, $u_{oA}$

Considering the effect of digital delay, $u_{oA}$ in Figure 5b is calculated as

$$\Delta U_{oA}(s) = e^{-1.5sT_S} \Delta U_{pcc}(s) \equiv e^{-1.5sT_S} \Delta U_{pcc,h}(s)$$

(5)

where the line-frequency component in $u_{oA}$ is neglected for simplifying the following combination of $u_{oA}$ and $u_{oB}$. Such simplification does not affect the stability analysis because line-frequency component stays away from the control bandwidth of the GC-VSI.

3.2.2. Calculation of the LV-VSC Output Voltage, $u_{oB}$

By combining the ac voltage regulation and the active damping function as presented in Figure 8, the generated output information, $u_d$, is derived.

$$\Delta U_d(s) = G_{NF}(s) e^{-0.5sT_S} \left( \Delta U_{pcc}(s) + R_C \Delta I_C(s) \right)$$

(6)

where $e^{-0.5sT_S}$ represents the equivalent sampling delay during processing $u_{pcc}$ and $i_C$, and the transfer function of the notch filter, $G_{NF}(s)$, is written as

$$G_{NF}(s) = \left( s^2 + \omega_0^2 \right) / \left( s^2 + 2\omega_b s + \omega_0^2 \right)$$

(7)

where the center frequency $\omega_0$ is obtained from the PLL term and the filter bandwidth $\omega_b$ determines the responding time.

The output voltage information of the PI controller for regulating the dc capacitor voltage is calculated as

$$\Delta U_d(s) = G_{PI}(s) \left( \Delta U_{dc}(s) - \Delta U_{dc,ref}(s) \right) \left( \frac{s}{s^2 + \omega_0^2} e^{-0.5sT_S} \right)$$

(8)

where $G_{PI}(s)$ means the transfer function of PI controller and $\frac{s}{s^2 + \omega_0^2}$ is the $s$-domain function of the sinusoidal signal, $\cos \omega_0 t$.

By adding Equation (6) with Equation (8), the modulating voltage of the LV-VSC, $\Delta U_m$, is obtained

$$\Delta U_m(s) = \frac{[\Delta U_d(s) + \Delta U_d(s)]}{U_{dc}} e^{-sT_S} = \frac{[\Delta U_d(s) + \Delta U_d(s)]}{U_{dc}} e^{-sT_S}$$

(9)

Thus, the converter output voltage of the LV-VSC becomes

$$\Delta U_{oB}(s) = [\Delta U_d(s) + \Delta U_d(s)] e^{-sT_S}$$

(10)

Because the control bandwidth of dc capacitor voltage regulation is much lower than the line frequency, $\Delta U_d$ is neglected. Then, (10) is simplified into

$$\Delta U_{oB}(s)_{\Delta U_d(s) \neq 0} = \Delta U_d(s) e^{-sT_S} = G_{NF}(s) e^{-1.5sT_S} \left[ \Delta U_{pcc}(s) + R_C \Delta I_C(s) \right] = e^{-1.5sT_S} \Delta U_{pcc,h}(s) + e^{-1.5sT_S} R_C \Delta I_C_h(s)$$

(11)

where the voltage source $\Delta U_{oB}$ is mainly composed of the feedforwarding voltage for grid impedance cancellation and the voltage for damping filter resonance.

3.3. Modeling Analysis of the Whole System

By combining Equations (5) and (11), the equivalent circuit is obtained as shown in Figure 9a, in which

$$G_d(s) = e^{-1.5sT_S}$$

(12)
which has been studied in reference [34].

Figure 9 can be further simplified into Figure 9b by combining the two separated voltage sources based on KVL, as described in Section 2. Based on Figure 9b, the transfer function of the plant from the inverter output voltage $u_i$ to grid current $i_o$ is derived.

$$G_w(s) = \frac{\Delta I_o(s)}{\Delta I_i(s)} = \frac{s b_1 + 1}{s^3 a_3 + s^2 a_2 + s a_1}$$ (13)

where $b_1 = R_d C_f G_d(s)$, $a_1 = L_1 + L_2 + L_g \left[1 - G_d(s)\right]$, $a_2 = R_d C_f d(s) \left[L_1 + L_2 + L_g \left[1 - G_d(s)\right]\right]$, and $a_3 = L_1 C_f \left[L_2 + L_g \left[1 - G_d(s)\right]\right]$.

Thus, based on the parameters tabulated in Table 1, the corresponding frequency characteristics of the original LCL filter, and the reshaped one with and without the digital delay are compared and plotted in Figure 10. It indicates that the original filter resonant frequency varies widely with the change of grid impedance while the effect of grid impedance would be cancelled only if the digital delay is not considered. The negative virtual grid impedance, $-Z_g G_d(s)$, with the digital delay, only counteracts the effect of grid impedance within the filter resonant frequency. It is noted that the damping behavior of the compensator with $-Z_g G_d(s)$ in Figure 10 is brought in by the digital delay, which has been studied in reference [34].

| System Parameter            | Value               |
|-----------------------------|---------------------|
| LCL filter                  | $L_1$ 3.8 mH        |
|                             | $L_2$ 1.2 mH        |
|                             | $C_f$ 3.3 µF        |
| Filter resonant frequency   | $f_r$ 2.9 kHz       |
| Grid inductance             | $L_g$ 0-0.1 pu      |
| DC capacitor                | $C_{dc}$ 3 × 1000 µF|
| Switching frequency         | $f_{sw-1}$ (Inverter)| 20 kHz              |
|                             | $f_{sw-2}$ (Compen.)| 40 kHz              |
| DC bus voltage              | $u_{in}$ 220 V      |
| DC capacitor voltage        | $u_{dc}$ 30 V       |
| Grid voltage                | $u_{pcc}$ 125 V     |
Equivalent circuit of the grid impedance compensator with the effect of digital delay.

\[
G_\delta(s) = \frac{\Delta I_\delta}{\Delta U_\delta} = \frac{s}{b_1 + 1} \frac{s^7 a_7 + s^6 a_6 + s^5 a_5}{s^8 a_8 a_7 a_6 + s^7 a_7 a_6 a_5 + s^6 a_6 a_5 a_4 + s^5 a_5 a_4 a_3 + s^4 a_4 a_3 a_2 + s^3 a_3 a_2 a_1 + s^2 a_2 a_1 + s a_1 + 1} 
\]

where

\[
b_1 = R_v G_\delta(s) + L_v + L_s + L_m \left[1 - G_\delta(s)\right] \\
a_5 = R_v C \delta d(s) \left[L_v + L_s + L_m \left[1 - G_\delta(s)\right]\right] \\
a_7 = L_v C_m \left[L_s + L_m \left[1 - G_\delta(s)\right]\right] 
\]

Thus, based on the parameters tabulated in Table 1, the corresponding frequency characteristics of the original LCL filter, and the reshaped one with and without the digital delay are compared and plotted in Figure 10. It indicates that the original filter resonant frequency varies widely with the change of grid impedance while the effect of grid impedance would be cancelled only if the digital delay is not considered. The negative virtual grid impedance, \(-Z_G G_\delta(s)\), with the digital delay, only counteracts the effect of grid impedance within the filter resonant frequency. It is noted that the damping behavior of the compensator with \(-Z_G G_\delta(s)\) in Figure 10 is brought in by the digital delay, which has been studied in reference [34].

To evaluate the system performance in the case of digital delay, a proportional-resonant-plus-harmonic-compensation (PR+HC)-based grid current control is adopted by the reshaped inverter (CASE II), and compared with the original one by using typical capacitor current-based active damping scheme with unit PCC VFFC (CASE I). The equation of PR+HC regulator is given as

\[
G_C(s) = K_P + \sum_{h=1,3,5,7,9} \left( K_{ih} s^2 + s \omega_B s^2 + s \omega_h^2 \right) 
\]

where \(K_P\) is the proportional gain of current regulation, and \(K_{ih}\) and \(\omega_B\) are the gain and band of individual resonant frequency \(\omega_h\). Thus, by combining Figure 8 with (13) and (14), the open loop transfer function of the reshaped inverter is obtained,

\[
T_i(s) = G_{vi}(s) G_C(s) G_d(s) 
\]

where the controller parameters are chosen based on the design criterion in [36] and the virtual resistance is designed as \(R_v = 30 \, \Omega\). The open loop transfer function of the inverter by using the capacitor current-based active damping function with unit PCC VFFC (CASE I) can be found in reference [11].

Then, comparative frequency response of \(T_i(s)\) with and without the grid impedance compensator is plotted in Figure 11. As seen, without the compensator, although the cutoff frequency of the main inverter is sustained above 0.9 kHz, the phase margin decreases sharply from 60 deg to 16 deg, when the grid impedance increases to 0.1 pu. With the compensator, not only is the cutoff frequency sustained at 1 kHz, but the phase margin is also maintained at 70 deg, even with wide variation of grid impedance. It reveals that the compensator decouples the effect of grid impedance successfully within the filter resonant frequency.
\[ G(s) = K_0 + sK \frac{1}{\omega s + \omega_0} \]

where the controller parameters are chosen based on the design criterion in [36] and the virtual transfer function of the reshaped inverter is obtained, individual resonant frequency is activated. As expected, both the inverter stability and high injected power quality are sustained at THDi 1.69%, which benefits from the unit PCC VFFC and PR effect of inverter current control effectiveness of inverter current control against PCC voltage distortion, a 300 W rectifier load is in shunt at the PCC in the following simulation.

Therefore, by adopting the proposed low-loss active compensator and neglecting the effect of digital delay, the reshaped well-damped GC-VSI with the cancellation of both grid impedance and harmonic grid voltage can be presented in Figure 12, where the effect of grid impedance has been counteracted, \( u_{g,0} \) represents the line frequency component of grid voltage, and current regulation of GC-VSI with a well-damped LCL filter is then eased.

![Fig 11](image1.png)

**Figure 11.** Comparative frequency response of the open loop transfer function (CF: cutoff frequency; PM: phase margin). (a) without the compensator (CASE I); (b) with the proposed compensator (CASE II).

**4. Simulation Results**

In this section, the simulation study is to verify the control functions of the LV-VSC, and conduct comparative evaluations between CASE I and CASE II as described in Section 3. The simulation is implemented in PSIM software. The parameters are given in Table 1, in which the dc capacitance of the LV-VSC is chosen to be large enough to mitigate the double frequency ripple at the dc side, and the LCL filter parameters are designed based on the criterion in reference [4]. The current control parameters are chosen properly according to reference [11]. To validate the effectiveness of inverter current control against PCC voltage distortion, a 300 W rectifier load is in shunt at the PCC in the following simulation.

Figure 13 presents the inverter output performance under different grid conditions when only active damping function (\( R_v = 30 \) \( \Omega \)) of the LV-VSC in Section 3.1.2 is activated. It indicates that the active damping function in the LV-VSC is helpful to stabilize the grid-connected inverter with an LCL filter in relatively strong grid condition. At \( L_g = 0.04 \) pu (4 mH), the total harmonic distortion (THD) of grid current is sustained at THDi = 1.69\%, which benefits from the unit PCC VFFC and PR+HC current regulator. However, with the increase of grid inductance, the grid current is highly distorted due to poor stability under the weak grid condition. To counteract such negative effect of grid impedance on the inverter output performance, ac voltage regulation of the LV-VSC introduced in Section 3.1.1 is activated. Figure 14 shows the simulation results with the grid impedance cancellation function of the LV-VSC enabled. As expected, both the inverter stability and high injected power quality

![Fig 12](image2.png)

**Figure 12.** Reshaped well-damped GC-VSI with the grid impedance cancellation.
are guaranteed even under very weak grid condition. That matches with the theoretical analysis in Section 3. Figure 15 simulates the dynamic operation of dc capacitor voltage regulation in the LV-VSC. The dc capacitor voltage tracks the reference command at 30 V gradually.

![Figure 13. Simulation results under different grid conditions when only active damping function of the proposed LV-VSC is enabled.](image1)

![Figure 14. Simulation results under different grid conditions when both active damping function and grid impedance cancellation function of the proposed LV-VSC are enabled (CASE II).](image2)

![Figure 15. The dynamic response of dc capacitor voltage regulation in the proposed LV-VSC.](image3)
To further demonstrate the importance of grid impedance cancellation, the inverter output performance with traditional current control method (CASE I) is also examined in simulation. To offer a fair comparison, the current control parameters in CASE I are kept the same with the proposed method (CASE II). Figure 16 shows the inverter output performance under different grid conditions for CASE I. It can be seen that the inverter stability becomes poor with the increase of grid inductance, which matches well with the theoretical analysis in Figure 11a. The poor performance in the extremely weak grid (i.e., \( L_g = 0.20 \text{ pu (10 mH)} \)) would be disastrous because other devices at the same PCC expose to the highly distorted PCC voltage. This problem is addressed successfully by using the proposed grid impedance cancellation method (CASE II), as indicated in Figure 14.

Figure 16. Simulation waveforms of the inverter outputs with traditional current control scheme (CASE I).

5. Experimental Validation

A 125 V, 50 Hz inverter prototype with the proposed grid impedance compensator was built for demonstration purposes and evaluate the system at the scaled-down laboratory level. Figure 17 shows the inverter prototype, where the volume of the compensator is much smaller than the GC-VSI owing to its extremely low volt-ampere (VA) rating. The design parameters are tabulated in Table 1. The inverter is supplied by an external DC power supply CHROMA 62050H-600S, and controlled by the digital controller, Texas Instruments TMS320F28379D. The experimental inverter setup is shown in Figure 18, where the inverter is connected to a 220 V, 50 Hz power grid through an isolator for the safety reason. The leakage inductance of the isolator is 0.65 mH. In Figure 18, an optional \( R_d - C_d \) branch is connected in shunt at the PCC to smooth the PCC voltage, which is usually included in the EMI filter. Because the LV-VSC is in series with the utility before the inverter is enabled, it will be activated after the dc capacitor voltage increases gradually to the reference voltage. Thereafter, the inverter will get involved and reach the steady-state operation.

Figure 19 presents the key waveforms of the inverter system. As seen, the dc capacitor voltage, \( u_{dc} \), of the LV-VSC is regulated at 30 V, which is superposed at the inverter output voltage, \( u_o \). The grid current, \( i_o \), is regulated in synchronous with the PCC voltage, \( u_{pcc} \). Owing to the full feedforwarding mechanism (as shown in Figure 8), strong harmonic rejection performance against grid harmonic distortion is obtained for the grid current as indicated in Figure 19.
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Figure 17. Top view of single-phase inverter prototype with the LV-VSC.

Figure 18. Experimental inverter setup with variable grid inductance.

Figure 19. Key waveforms of the inverter system.

5.1. Comparative Results with and without the Proposed LV-VSC

Figures 20–22 present the steady-state waveforms of the inverter outputs with the active compensator from disable state (CASE I) to enable state (CASE II) under different grid impedance. They indicate that the grid impedance compensator exhibits strong harmonic rejection capability of the inverter against the grid voltage distortion even with wide variations of equivalent grid inductance.

Figure 19. Key waveforms of the inverter system.

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They indicate that the grid impedance compensator exhibits strong harmonic rejection capability of the inverter against the grid voltage distortion even with wide variations of equivalent grid inductance.

Figure 20. Comparative waveforms of the inverter outputs with the active compensator from disable to enable when $L_g = 0$.

Figure 21. Comparative waveforms of the inverter outputs with the active compensator from disable to enable when $L_g = 0.04$ pu.

Figure 22. Comparative waveforms of the inverter outputs with the active compensator from disable to enable when $L_g = 0.1$ pu.

With the active compensator disabled, the inverter stability is vulnerable to the variation of the equivalent grid inductance, $L_g$, as shown in Figures 20–22. Due to poor stability margin with large grid impedance, the measured total harmonic distortion (THD) of the grid current increases from 1.9% to 4.2%. Although the THD of the grid current at $L_g = 0.1$ pu still meets the standard requirement, i.e., IEEE Std 1547.2-2008, the maximum odd harmonic current distortion at 1.25 kHz is 2.2% highlighted in Figure 23 and exceeds the odd harmonic current distortion limit of 0.6% [37]. That is because the inverter becomes poor stable with the increase of grid impedance. Moreover, the voltage at the PCC, $u_{pcc}$, is distorted due to poor quality grid current and might affect the devices at the PCC.
oscillation is seen at the PCC voltage. The above experimental results match with the theoretical analysis in Section 3.3.

To further validate the effectiveness of the proposed control mechanism against the grid distortion, a nonlinear rectifier load is in shunt at the PCC to distort the grid voltage. The corresponding experimental results with highly distorted PCC voltage are presented in Figure 24. As indicated in Figure 24a, without the proposed method in CASE I, the grid current quality is poor (THDi = 10.00%) due to highly distorted PCC voltage and poor stability under relatively weak grid condition, which matches with the theoretical analysis in Figure 11a. By integrating the proposed method into the inverter, the inverter stability with large stable margin will be guaranteed as analyzed in Figure 11b, and strong harmonic suppression against the grid distortion can be ensured as shown in Figure 12. As expected, with the proposed method in CASE II, both the inverter stability and grid current quality are guaranteed (THDi = 4.22%) even under the weak grid condition with highly distorted PCC voltage as presented in Figure 24b.

![Figure 23. Frequency spectrum of the grid current without the compensator at $L_g = 0.1$ pu.](image)

With the active compensator enabled, the inverter maintains stable even under wide variation of equivalent grid inductance because the active damping function in the LV-VSC is activated. The measured grid current THD is sustained at 1.5%, 1.7%, and 1.5%, respectively. Moreover, no oscillation is seen at the PCC voltage. The above experimental results match with the theoretical analysis in Section 3.3.

To further validate the effectiveness of the proposed control mechanism against the grid distortion, a nonlinear rectifier load is in shunt at the PCC to distort the grid voltage. The corresponding experimental results with highly distorted PCC voltage are presented in Figure 24. As indicated in Figure 24a, without the proposed method in CASE I, the grid current quality is poor (THDi = 10.00%) due to highly distorted PCC voltage and poor stability under relatively weak grid condition, which matches with the theoretical analysis in Figure 11a. By integrating the proposed method into the inverter, the inverter stability with large stable margin will be guaranteed as analyzed in Figure 11b, and strong harmonic suppression against the grid distortion can be ensured as shown in Figure 12. As expected, with the proposed method in CASE II, both the inverter stability and grid current quality are guaranteed (THDi = 4.22%) even under the weak grid condition with highly distorted PCC voltage as presented in Figure 24b.

![Figure 24. Cont.](image)
Figure 24. Comparative waveforms with a shunt rectifier load at the PCC ($L_g = 0.1$ pu.) (a) without the proposed method. (b) with the proposed method.

5.2. Transient Behavior

The transient behavior of the inverter with the proposed active compensator is investigated under the relatively weak grid condition ($L_g = 0.1$ pu). The power rating is suddenly programmed from half to full power and vice versa. The corresponding experimental results waveforms are shown in Figure 25. They indicate that the inverter with the proposed compensator operates well with the power transients.

Figure 25. Transient behavior of the grid-connected inverter when $L_g = 0.1$ pu.

5.3. Power Consumption of the LV-VSC

Owing to the extreme low dc capacitor voltage, low voltage switching devices are chosen for the LV-VSC, which are MOSFETs FDD86110 (100 V, 50 A) with on-state resistance of 10.2 mΩ. Based on that, Figure 26 shows comparative results of the calculated and measured power loss ($P_d$) between the proposed LV-VSC in series with the filter capacitor and the one in series at the inverter output in [34].
as a function of the inverter output current ($i_o$), in which the power loss of the LV-VSC is mainly from switching devices and dc capacitors.

![Power loss comparison between the proposed LV-VSC and the one in [34].](image)

As seen, the power loss of the LV-VSC in [34] increases obviously with the inverter output current because the current through the LV-VSC equals to the inverter output current. However, the power loss of the proposed LV-VSC in series with the filter capacitor is maintained around 1W since the small value of capacitor current through the LV-VSC is independent on the inverter output power. For example, the capacitor current through the proposed LV-VSC is maintained around 0.4 Arms in the case study regardless of the increase of inverter output current. Thus, the efficiency of the entire system is not sacrificed since the VA rating of the proposed impedance compensator is sustained extremely low.

6. Conclusions

A low-loss active compensator based on dual unit PCC VFFCs has been proposed to counteract the effects of grid impedance on the inverter current control performance. The grid impedance compensator has been proven to feature

1. Extremely low power loss;
2. Requiring no additional passive LC filtering components;
3. Strong harmonic rejection capability against grid disturbance; and
4. Eliminating the negative effects of grid impedance on the inverter current control performance.

Both simulation results and experimental verifications are provided to validate the feasibility of the compensator. It reveals that the inverter stability and injected power quality even under different grid conditions have been enhanced compared with traditional capacitor current-based active damping scheme with unit PCC VFFC. The digitally controlled inverter with the active compensator counteracts the effect of equivalent grid impedance. Although the proposed concept introduces additional hardware and losses, it is thought that the benefits may justify the extra costs in the applications of distributed power generation systems with LCL filter-based grid-connected inverters.

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