Low-Latency Online Multiplier with Reduced Activities and Minimized Interconnect for Inner Product Arrays

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Received: 16 May 2022 / Revised: 24 January 2023 / Accepted: 28 February 2023 / Published online: 19 April 2023
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Abstract
Multiplication is indispensable and is one of the core operations in many modern applications including signal processing and neural networks. Conventional right-to-left (RL) multiplier extensively contributes to the power consumption, area utilization and critical path delay in such applications. This paper proposes a low latency multiplier based on online or left-to-right (LR) arithmetic which can increase throughput and reduce latency by digit-level pipelining. Online arithmetic enables overlapping successive operations regardless of data dependency because of the most significant digit first mode of operation. To produce most significant digit first, it uses redundant number system and we can have a carry-free addition, therefore, the delay of the arithmetic operation is independent of operand bit width. The operations are performed digit by digit serially from left to right which allows gradual increase in the slice activities making it suitable for implementation on reconfigurable devices. Serial nature of the online algorithm and gradual increment/decrement of active slices minimize the interconnects and signal activities resulting in overall reduction of area and power consumption. We present online multipliers with; both inputs in serial, and one in serial and one in parallel. Pipelined and non-pipelined designs of the proposed multipliers have been synthesized with GSCL 45nm technology on Synopsys Design Compiler. Thorough comparative analysis has been performed using widely used performance metrics. The results show that the proposed online multipliers outperform the RL multipliers.

Keywords Online arithmetic-based multiplier · Left-to-right arithmetic · Working precision reduction · Low-power computation

1 Introduction
Multiplication is regarded as the fundamental operation in various signal processing and machine learning applications. Multipliers are regarded as the bottleneck in performance of various algorithms and it has been well versed that the architecture of the multiplier has direct effect on the performance of these applications in terms of area utilization, power consumption, and critical path delay. Based on the partial product generation and reduction, conventional multipliers can be categorized as linear array multipliers and tree multipliers [1, 2]. Multipliers utilizing the digit-parallel computation require full bandwidth interconnection datapaths, resulting in an increased power/energy requirement. Digit-serial arithmetic is, therefore, often used to reduce the interconnection and hardware complexity. Both serial-parallel and serial-serial multipliers have been proposed over the years where one or both operands are provided serially, respectively. However, one of the drawbacks of using these multipliers is that their latency is dependent on the word size of operands. Furthermore, conventional arithmetic-based serial-serial and serial-parallel multipliers have limitation on throughput as the succeeding operation can be started only after the completion of current operation.

Online or left-to-right (LR) arithmetic [3], which processes the input operands and generates result digits serially in a most significant digit first (MSDF) manner, can serve as
a potential computing paradigm to address the limitations of conventional arithmetic and achieve aforementioned requirements of latency, throughput, area, and power. There are several benefits of using online arithmetic-based operators:

- Operands and result are streamed serially which reduces the interconnection bandwidth, area, and energy dissipation [4].
- The computation can be started without waiting for full precision data after an initial delay also called the online delay (\( \delta \)) during which, a few input bits are received. \( \delta \) is a small number and represents the inter-operation latency.
- Successive operations have delay of \( \delta + 1 \), therefore, they can be pipelined regardless of data dependency and achieve high throughput with minimum interconnect.
- It makes use of redundant number system which makes cycle time of the operation independent of precision.
- The working precision can be truncated such that \( n \)-digit precision result can be obtained by implementing \( p < n \) digit slices.
- Computation can be stopped upon reaching the desired precision due to the MSDF mode of operation, thus, it can be configured as a variable/approximate computation algorithm.

Online arithmetic has been widely adopted for the design and development of various simple and complex arithmetic circuits e.g., adders [5], multipliers [6], 3-D vector normalization [7], as well as in a number of compute intensive digital signal processing (DSP) applications [8], and matrix computation [9]. In [10], online arithmetic operators were studied for implementation on FPGA where the property of online arithmetic was exploited and a fixed piece of hardware was utilized to perform calculations at any precision. This resulted in 8x speed-up to execute Newton’s method compared to parallel-in-serial-out fixed point method. In [11], online operators were focused for efficient implementation on FPGA in order to achieve area savings and obtain speed-ups. For different online operators, a reduction of up to 56% silicon area and speed-up of around 1.5x was shown on Xilinx Virtex-6 FPGA.

The idea of pipelining the online serial-serial multiplier had been presented in our previous work [12]. In the continuation, we present the design of the online serial-serial pipelined multiplier with the derivations and detail of implementation of each module of the multiplier. Furthermore, the design of a pipelined serial-parallel online multiplier is also presented in this work. For the serial-serial online multiplier, we exploit the property of online arithmetic to truncate the maximum working precision i.e., to obtain \( n \) bit result, \( p < n \) bit slices are implemented which reduce the signal activities and interconnections. Furthermore, the slice activity of the proposed multiplier follows an increasing/decreasing pattern in terms of active slices i.e., the number of active slices increases systematically up-to a maximum of \( p < n \) and then decreases. To which end, each step of the algorithm has been unrolled such that each stage instantiates only the desired number of bit slices to minimize the interconnection and signal activities.

The proposed designs of digit-level-pipelined serial-serial and serial-parallel multipliers have been synthesized to obtain area, power, and critical path delay results using Synopsys Design Compiler with GSCL 45 nm liberty cell library from the Free45PDK and compared with non-pipelined versions of online multipliers as well as conventional multipliers.

The rest of the paper, we proceed as follows: an overview of online arithmetic and online multiplier has been presented in Section 2. Details about the architecture, algorithm, and implementation of the proposed pipelined multipliers have been presented in Section 3. The implementation results have been presented in Section 4, followed by the conclusion of the paper in Section 5.

### 2 Online Arithmetic

Several researchers have considered online arithmetic for implementing complex DSP algorithms on hardware to achieve high degree of parallelism [8, 13, 14]. Requirement of reduced interconnection bandwidth makes them suitable for adoption in the multi-module structures in both parallel and pipelined configurations where the interconnection bandwidth is constrained. The online delay \( \delta \), during which the inputs are received, is independent of precision and, therefore, pipelining of the serially produced output digits is possible with the latency of \( \delta \) in contrast to the digit-parallel algorithms where throughput is governed by the data dependency [3]. The timing difference between conventional and online arithmetic is such that for the sequence of dependent operations in the online arithmetic, the computation can be started as soon as the MSD of the result is generated from the preceding operation i.e., after \( \delta + \) compute cycles. On the contrary, the conventional arithmetic operators must wait for the completion of previous computation. This phenomenon, assuming \( \delta = 3 \) and compute cycle \( c = 1 \), has been depicted in Fig. 1.

The output is computed on the basis of partial information about the inputs, therefore, the redundant number system is employed which allows a number to be represented in more than one way. Although, the cost per bit is increased, it results in an overall advantage, as the need for carry propagation is eliminated and cycle time of the operation becomes independent of bit-precision. We employ signed digit (SD) redundant number system where number representation is...
done in radix ($r$) form and each signed digit belongs to a set \{-a, ..., -1, 0, 1, ..., a\} and $\frac{-a}{2} \leq a < r$. For a digit set to be redundant, the digit set must fulfill the condition $2a + 1 > r$ such that $a \leq r - 1$. The amount of redundancy in the number system is represented by $\rho = \frac{a}{r-1}$. A digit set is said to be redundant if $\rho > \frac{1}{2}$, whereas if $\frac{1}{2} < \rho < 1$, the digit set constitutes to maximally and over-redundant digit sets respectively. For simplicity, all implementations in this study use radix-2 SD representation on a symmetric redundant digit set of \{-1, 0, 1\}. In cases where the conversion of SD to conventional number system is required, an efficient conversion technique named on-the-fly conversion (OTFC) is adopted [15]. The process of OTFC does not require carry propagate adders, hence the computation is carried out without any additional delay.

### 2.1 Non-pipelined Online Multiplier

The online arithmetic algorithms including online adder and online multiplier use fractional numbers to make them compatible with all operations and to simplify the alignment of the operands, therefore, the weight of the operand’s first digit is $r^{-1}$. At any $j^{th}$ iteration, a digit $x_j$ is represented by two single bits, $x_j^+$ and $x_j^-$, and their subtraction produces the value of the represented digit (1), allowing a conventional number to be represented in several ways.

$$x_j = SUB(x_j^+, x_j^-)$$

(1)

The numerical value of the digit $x$ at iteration $j$ and $j + 1$ is denoted as $x[j]$, and $x[j + 1]$ respectively, and its corresponding online form is represented as:

$$x[j] = \sum_{i=1}^{j+\delta} x_i r^{-i}$$

$$x[j + 1] = x[j] + x[j + 1 + \delta] r^{-(j + 1 + \delta)}$$

(2)

The non-pipelined radix-2 online multiplier with $n$ precision as shown in Fig. 2, presented in [16], has an online delay $\delta = 3$ and the selection function requires $t = 2$ fractional bits along with 2 integer bits (ibs) to select the output. The description of each module in the figure is presented in Section 3.3. The input operands $x$ and $y$ in the signed digit redundant representation are computed to produce the product digit $z$ ranging from $(-1, 1)$ from the symmetric signed
digit set \([-a, \ldots, a]\). The operands and the resulting product digit at iteration \(j\) are given as:
\[
x[j] = \sum_{i=1}^{j+\delta} x_i r^{-i}, \quad y[j] = \sum_{i=1}^{j+\delta} y_i r^{-i}, \quad z[j] = \sum_j z_i r^{-i},
\]
where the subscripts denote the digit index and the iteration index is indicated by square brackets.

The algorithm executes for \(n + \delta\) iterations, during which one digit of input operands \(x_j\) and \(y_j\) is introduced per iteration, except for the last \(\delta\) cycles where the input digits are set to zero. Similarly the output digit \(z_j\) is produced at each iteration after \(\delta\) cycles, whereas, in the first \(\delta\) iterations, the result for the output digit remains zero. The fundamental part of the online algorithms is the development of recurrence on the internal state and defining a selection function with selection constants to produce the result digit. Both these methodologies and the algorithm of the online multiplier have been detailed in the ensuing section.

### 2.1.1 Residual and its Recurrence

Method for developing online algorithms including addition, multiplication, and division have been presented in Chapter 9 of [16]. For completeness, we present the derivations of residual and recurrence in the online multiplication in the following. At each iteration \(j\), a SD input is received such that the entrance of one of the operands (in this case \(y\)) is one clock cycle prior to the other. The SD input is converted to two's complement representation in digit serial manner using on-the-fly conversion/append (CA) function as: \(x[j] = CA(x[j-1], x_{j+4})\) and \(y[j] = CA(y[j-1], y_{j+4})\). An output is produced on the basis of only partial information of the inputs, therefore, an error bound must be defined as follows:
\[
|\lbrack x[j] \cdot y[j] - z[j] \rbrack| < r^{-j}
\]

The above relation is subjected to a transformation function to develop the recurrence having primitive functions only, which is then scaled by a factor to have a bound on the error after the computation of \(j\) digits. The corresponding scaled residual is given by:
\[
w[j] = r^j (x[j] \cdot y[j] - z[j])
\]

The residual can be deduced to obtain the recurrence \(w[j + 1]\):
\[
w[j + 1] = rw[j] + (x[j] \cdot y_{j+1+\delta} + y[j + 1] \cdot x_{j+1+\delta}) r^{-\delta} - z_{j+1}
\]
This can be decomposed into:
\[
v[j] = rw[j] + (x[j] \cdot y_{j+1+\delta} + y[j + 1] \cdot x_{j+1+\delta}) r^{-\delta}
\]
\[
w[j + 1] = v[j] - z_{j+1},
\]
or,
\[
v[j] = rw[j] + H_1
\]
\[
w[j + 1] = v[j] + H_2(z_{j+1})
\]
resulting in,
\[
H_1 = (x[j] \cdot y_{j+1+\delta} + y[j + 1] \cdot x_{j+1+\delta}) r^{-\delta}
\]
\[
H_2 = -z_{j+1},
\]
so that \(H_i\) is independent of \(z_{j+1}\).

For \(r = 2\) and \(\delta = 3\), \(v[j]\) in (7) can be rewritten as:
\[
v[j] = 2w[j] + (x[j] \cdot y_{j+4} + y[j + 1] \cdot x_{j+4}) 2^{-3}
\]

The multiplication of terms with \(2^{-3}\) in (10) is carried out using arithmetic right shift by 3. As can be observed in Fig. 2, the residual, \(w[j]\), in the redundant carry-save form actually has a 2’s complement representation and is represented by the vectors \(WS[j]\) and \(WC[j]\).

Next step is to determine the bounds of \(w[j + 1]\) in terms of \(H_1\) and \(H_2\). This is given as:
\[
\overline{o} = r\overline{w} + \max(H_1) + H_2(a)
\]
resulting in
\[
\overline{o} = -\frac{\max(H_1) + H_2(a)}{r - 1}
\]
Likewise,
\[
\underline{o} = -\frac{\min(H_1) + H_2(-a)}{r - 1}
\]
For the case of serial-serial multiplier, \(\max(H_1)\) and \(\min(H_1)\) results in \(2ar^{-\delta}\) and \(-2ar^{-\delta}\) respectively, whereas \(H_2(a)\) and \(H_2(-a)\) are \(-a\) and \(a\) respectively. Substituting values of \(H_1\) and \(H_2\) in relations 12 and 13, yields following results
\[
\overline{o} = -\frac{2ar^{-\delta} - a}{r - 1}
\]
Likewise,
\[
\underline{o} = \frac{2ar^{-\delta} - a}{r - 1}
\]

### 2.1.2 Selection Function with Selection Constants

Two methods have been suggested for the selection of output digit in [16], one of which uses selection constants, while the other method is based on rounding of the residual which
is used for higher radix \( (r > 4) \). In this research, we employ radix-2, therefore, the selection function is implemented using selection constants. The output digit \( z_{j+1} = q \) where \( q_i = -a, -a + 1, \ldots, a \) depends upon the selection intervals of \( v[j] \) is selected using a selection function such that the residual \( w[j+1] \) remains bounded. Only \( t \) most significant fractional bits along with integer bits of \( v[j] \) are used from the result generated by the [4 : 2] adder in carry-sum pair (WS and WC) to give its estimate, \( \hat{v}[j] \).

The output digit \( z_{j+1} \) is produced using the selection function in a way that \( w[j+1] \) remains bounded according to relations 12 and 13. In the method with selection constants it is described by the selection constants \( m_k \) such that

\[
z_{j+1} = k \quad \text{if} \quad m_k \leq \hat{v}[j] < m_{k+1} \tag{16}\]

Here \( \hat{v}[j] \) is an estimate of \( v[j] \), computed by truncating \( v[j] \) to \( t \) fractional bits. To produce a correct selection function, the selection constants must satisfy

\[
\max(\hat{L}_k) \leq m_k \leq \min(\hat{U}_k) \tag{17}
\]

where \([\hat{L}_k, \hat{U}_k]\) is the selection interval of the estimate \( \hat{v}[j] \). The selection intervals \([L_k, U_k]\) are obtained from relation, and then the intervals are restricted for \( \hat{v}[j] \).

\[
\bar{\omega} = U_k + H_2(k) \quad \bar{\omega} = L_k + H_2(k) \tag{18}
\]

An error is introduced due to truncation and using estimate \( \hat{v}[j] \), given as

\[
e_{\min} \leq v[j] - \hat{v}[j] \leq e_{max} \tag{19}
\]

For carry-save representation, \( e_{max} = 2^{-t+1} - ulp \) and \( e_{min} = 0 \), which when substituted in Eq. (18) for \( \hat{L}_k \) and \( \hat{U}_k \), and using carry-save representation, for \( w[j] \) and \( v[j] \), results in the following

\[
\hat{U}_k = [\rho(1 - 2r^{-\delta}) + k - 2^{-t}], \quad \hat{L}_k = [-\rho(1 - 2r^{-\delta}) + k] \tag{20}
\]

To determine \( t \) and \( \delta \), we use the relation \( \hat{U}_{k-1} - \hat{L}_k \geq 0 \). The corresponding expression is given as

\[
[\rho(1 - 2r^{-\delta}) + k - 1 - 2^{-t}], -\hat{L}_k = [-\rho(1 - 2r^{-\delta}) + k], \geq 0 \tag{21}
\]

Since \( \rho = 1 \) and radix \( r = 2 \) is known, we substitute one variable, either \( t \) or \( \delta \) to obtain the value of another. The objective is to obtain small values of both the variables. Starting from minimum values the relation is checked for satisfaction. For serial-serial multiplier, the relation is satisfied for \( \delta = 3 \) and \( t = 1 \). The selection constants \( m_k \)'s are obtained from

\[
\hat{L}_k \leq m_k \leq \hat{U}_{k-1} \tag{22}
\]

which results in \( m_0 = -2^{-1} \) and \( m_1 = 2^{-1} \).

The range of \( v[j] \) is given by:

\[
[r\bar{\omega} + \min(H_1) - e_{max}] \leq \hat{v}[j] \leq [r\bar{\omega} + \max(H_1) + |e_{min}|], \tag{23}
\]

Substituting corresponding values we obtain \(-2 \leq \hat{v}[j] \leq \frac{7}{4} \).

This is used to define the selection function \( SELM \) as shown in relation \( (24) \).

\[
z_{j+1} = SELM(\hat{v}[j]) = \begin{cases} 1 & \text{if } \frac{1}{2} \leq \hat{v}[j] \leq \frac{7}{4} \\ 0 & \text{if } -\frac{1}{2} \leq \hat{v}[j] \leq \frac{1}{4} \\ -1 & \text{if } -2 \leq \hat{v}[j] \leq -\frac{3}{4} \end{cases} \tag{24}
\]

The product digit \( z_{j+1} \) uses similar coding as \( (1) \) and the corresponding selection function is shown in Table 1. The estimate of the residual is calculated in the \( V \) block and the calculation of the updated residual \( w[j+1] \), which requires subtraction of \( z_{j+1} \) from \( v[j] \), is carried out by the \( M \) block. The subtraction is performed using a Boolean expression rather than explicit subtraction \[14\], as shown later in Section 3.3.2.

### 2.1.3 Algorithm

The conventional algorithm has two steps; (1) initialization: having execution length equal to \( \delta \), during which the input digits are collected and no output is generated, (2) recurrence: which executes for \( n \) iterations, producing one output digit in each iteration. The pseudocode of the non-pipelined radix-2 serial-serial online multiplier is shown in Algorithm 1.
2.2 Non-pipelined Serial-Parallel Online Multiplier

For the serial-parallel multiplier, one of the operands enters in serial MSDF manner and the other is a constant and is available in parallel at the implementation time. The radix-2 non-pipelined serial-parallel online multiplier depicted in Fig. 3, has an online delay of 2. Its selection function requires \( t = 2 \) fractional and 1 integer bit. The derivation of online serial-parallel multiplier has been presented in [8]. It follows same steps as the online multiplier with both operands in serial, therefore, only the results of the derivations are presented in this section.

The online operands (input \( x \) and output \( z \)) in each cycle are represented as (2), and the constant is represented as:

![Figure 3](image)

**Figure 3** Non-pipelined radix-2 serial-parallel online multiplier. Online delay \( \delta = 2 \) and \( t = 2 \).
\[ Y[j] = Y = -y_0 \cdot r^0 + \sum_{i=1}^{n} y_i r^{-i} \]  

(25)

### 2.2.1 Residual and its Recurrence

The error bound at each computation step is given as:

\[ |x[j] \cdot Y - z[j]| < r^{-j} \]  

(26)

The scaled residual at step \( j \) is given as:

\[ w[j] = r^l (x[j] \cdot Y - z[j]) \]  

(27)

Recurrence in the function \( w[j+1] \) is obtained as:

\[ w[j+1] = rw[j] + (x_{j+\delta} \cdot Y) r^{-\delta} - z_{j+1}, \]  

(28)

The bounds of \( w[j+1] \) are determined similarly as (11), (12), and (13). However, for serial-parallel online multiplier \( \max(H_1) \) and \( \min(H_1) \) are \( ar^{-\delta} \) and \( -ar^{-\delta} \) respectively.

The resulting \( \overline{\omega} \) and \( \underline{\omega} \) are given as:

\[ \overline{\omega} = \frac{-ar^{-\delta} - a}{r - 1}, \]  

(29)

and,

\[ \underline{\omega} = \frac{ar^{-\delta} - a}{r - 1} \]  

(30)

### 2.2.2 Selection Function with Selection Constants

The selection function for serial-parallel online multiplier is obtained in a similar manner as for the serial-serial online multiplier derived in Section 2.1.2. However, the corresponding values of \( H_1 \) and \( H_2 \) are substituted in relations to obtain \( \hat{U}_k \) and \( \hat{L}_k \) as follows:

\[ \hat{U}_k = [\rho(1 - r^{-\delta}) + k - 2^{-t}], \]  

\[ \hat{L}_k = [-\rho(1 - r^{-\delta}) + k], \]  

(31)

Similarly the values of \( t \) and \( \delta \) are determined using following relation:

\[ [\rho(1 - r^{-\delta}) + k - 1 - 2^{-t}], -\hat{L}_k = [-\rho(1 - r^{-\delta}) + k], \geq 0 \]  

(32)

Relation (32) yields \( t = 2 \) and \( \delta = 2 \) for the online serial-parallel multiplier. They are then used to determine the range of \( v[j] \) using (23), which in turn yields similar values as of serial-serial multiplier. The selection constants for serial-parallel multiplier are also similar, therefore, the same selection function (24) is utilized for serial-parallel online multiplier with 2 integer bits.

### 2.2.3 Algorithm

Similar to serial-serial online multiplier, the algorithm has two steps, (1) initialization: having execution length equal to \( \delta \) during which, the input digits are collected and no output is generated, (2) recurrence: which executes for \( n \) iterations, producing one output digit in each iteration. The pseudocode of the non-pipelined radix-2 serial-parallel online multiplier is shown in Algorithm 2.

### 3 Proposed Pipelined Online Multiplier

In the non-pipelined design of online multiplier, the working precision of \( n \) bits is constant and all digit slices remain active during all iterations. However, in [4], sources of reduction of active slices have been presented which include gradual use of the input digits and reduction of working precision to \( p < n \). The proposed pipelined design is a 2D implementation in which the inactive modules are not implemented which results in savings of both dynamic and static power.

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**Algorithm 2 Serial-Parallel Online Multiplication**

1: Initialize:
   \[ x[-2] = w[-2] = 0 \]

2: for \( j=-2, -1 \) do
   3: \( v[j] = 2w[j] + (x_{j+2} \cdot Y) 2^{-2} \)
   4: \( w[j+1] \leftarrow v[j] \)
   5: end for

6: Recurrence:
7: for \( j = 0 \ldots n + \delta \) do
   8: \( v[j] = 2w[j] + (x_{j+2} \cdot Y) 2^{-2} \)
   9: \( z_{j+1} = SELM(v[j]) \)
   10: \( w[j+1] \leftarrow v[j] - z_{j+1} \)
   11: \( Z_{out} \leftarrow z_{j+1} \)
   12: end for
3.1 Precision Reduction

Since the output digit of the online algorithm is based on a selection function which utilizes a few most significant bits of the residual comprised of an integer and fractional bits, as discussed in Section 2.1.2, to obtain the residual’s estimate denoted by \( \hat{v} \). Therefore, it is possible to achieve \( n \) bits accuracy by implementing only \( p \) (\( p < n \)) bit slices and ignoring a few least significant \( h \) bit slices as shown in Fig. 4.

For \( j \leq p \) iterations \( j + \delta \) modules are active in \( j^{th} \) recurrence step; whereas, for \( j > p \), the availability of only \( p \) modules introduces an error due to truncation. The algorithm’s convergence can be assured if the \( t \) bits in the selection function are not affected due to the truncation error. The optimal number of \( p \) varies according the type of adder used in the recurrence equation, the number of ignored bit slices \( h \), and the initial delay \( \delta \). For a valid selection in an online multiplier with \([4 : 2]\) adder, and using \( t \) fractional bits \( p - 2h + \delta \geq t \).

\[
\begin{align*}
\hat{v} & = \frac{2n + \delta + t}{3} \\
\end{align*}
\]

Due to the gradual increase in the precision of the incoming digits, the signal activity is not constant and increases gradually in each iteration. Furthermore, if \( p < n \) slices are implemented for the given multiplier, the signal activity begins to decrease after \( p \) iterations due the truncation error which affects \( (j-2)^{th} \) result bit and is shifted one bit towards left due to the left shift operation in the recurrence. Overall, the error propagates to 3 bit slices, therefore, the 3 least significant bit slices can be turned off in the subsequent stage of the pipeline yielding a low-power design.

Based on these properties, 8, 16, 24 and 32 bit low-power designs of pipelined serial-serial multiplier have been compared with pipelined serial-serial online multiplier with full working precision in [12]. According to relation (33), the \( n \) precision result can be obtained by employing 7, 12, 18 and 23 modules for 8, 16, 24 and 32 bit designs respectively. The proposed low-power design has been implemented as a two-dimensional pipeline array, where the bit widths of the registers (CA-Reg, Reg WS, Reg WC), adder, and selector are increased till \( p^{th} \) iteration and then decreased till \( n + \delta \) iteration.

3.2 Pipelined Online Multiplier

The non-pipelined online multiplier has its throughput limited by its latency because it produces one vector in \( n + \delta + 1 \) cycles. In applications where large number of multiplications have to be performed, this limitation on the throughput may not be acceptable. Therefore, to process large number of operations, it is suitable to unfold and pipeline the multiplier. For \( n \)-bit precision, \( n + \delta \) stages of the multiplier are

\[
\begin{align*}
\text{Cycles} & : 1 & 2 & 3 & 4 & 5 & 6 & 7 \\
\text{Pipeline Stages} & : 1 & 2 & 3 & 4 & 5 & 6 & 7 \\
\end{align*}
\]

Due to the gradual increase in the precision of the incoming digits, the signal activity is not constant and increases gradually in each iteration. Furthermore, if \( p < n \) slices are implemented for the given multiplier, the signal activity begins to decrease after \( p \) iterations due to the truncation error which affects \( (j-2)^{th} \) result bit and is shifted one bit towards left due to the left shift operation in the recurrence. Overall, the error propagates to 3 bit slices, therefore, the 3 least significant bit slices can be turned off in the subsequent stage of the pipeline yielding a low-power design.

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\[
\begin{align*}
\text{Cycles} & : 1 & 2 & 3 & 4 & 5 & 6 & 7 \\
\text{Pipeline Stages} & : 1 & 2 & 3 & 4 & 5 & 6 & 7 \\
\end{align*}
\]
unfolded and pipelined. It takes \( n + \delta \) cycles to fill the pipeline, and once the pipeline is in steady state, the multiplier produces \( n \)-bit output vector in each cycle. This phenomenon has been depicted in Fig. 5, for 8 bit wide \( K \) vectors of \( X \) and \( Y \). The cycle time for the pipelined online multiplier is the same as the non-pipelined online multiplier and is also independent of bit precision. This drastically improves the throughput of the network. As discussed in Section 3.1, the input bit precision is increased gradually and \( p < n \) modules are sufficient to produce \( n \)-bit precision result, only the required number of modules can be activated up to \( p^\text{th} \) iteration and after truncation in \((p+1)^\text{th}\) iteration, the modules can be turned off using some switching mechanism according to the error profile. In a pipelined scheme, however, the inactive modules are not implemented, hence no dynamic/static power is consumed.

### 3.2.1 Algorithm

We present the algorithm in three steps [12], including, (1) initialization: having execution length equal to \( \delta \), during which the input digits are collected and no output is generated, (2) recurrence: which executes for \( n - \delta \) iterations, producing one output digit in each iteration. (3) last \( \delta \) cycles: having execution length equal to \( \delta \), during which the input digits are zero and output is generated in each iteration. The pseudocode of the non-pipelined radix-2 online multiplier presented in [16], with initialization and recurrence loops, has been modified to have three loops as shown in the Algorithm 3, the corresponding block diagrams were presented in [12].

A 16-bit pipelined scheme which is a two-dimensional array structure with 16 stages has been depicted in Fig. 6. The digit selection module in the most significant place is instantiated after initialization steps to generate an output digit and the residual signals are transferred vertically to the subsequent linear array instead of left shifting as in the conventional implementation. The input vectors are arranged in a stair-case manner to match the pipeline online flow using a stair-case shifter array shown in Fig. 7. This simply adds a delay in the \( i^\text{th} \) digit of a vector using an \( i \)-bit shift register [7]. The details of each digit slice has been presented in the forthcoming section.

### 3.3 Implementation Details

In the proposed design, each digit slice has been fine tuned in order to reduce signal activities, area utilization and power consumption. Accordingly, only useful modules are

---

**Algorithm 3 Proposed Online Multiplication**

1: Initialize:
   \[ x[-3] = y[-3] = w[-3] = 0 \]
2: for \( j = -3, -2, -1 \) do
3:   \( x[j + 1] \leftarrow CA(x[j], x_{j+4}) \);  
   \( y[j + 1] \leftarrow CA(y[j], y_{j+4}) \);
4:   \( v[j] = 2w[j] + (x[j]y_{j+4} + y[j + 1]x_{j+4})2^{-3} \)
5:   \( w[j + 1] \leftarrow v[j] \)
6: end for

7: Recurrence:
8: for \( j = 0 \ldots n - \delta - 1 \) do
9:   \( x[j + 1] \leftarrow CA(x[j], x_{j+4}) \);  
   \( y[j + 1] \leftarrow CA(y[j], y_{j+4}) \);
10: \( v[j] = 2w[j] + (x[j]y_{j+4} + y[j + 1]x_{j+4})2^{-3} \)
11: \( z_{j+1} = SELM(v[j]) \)
12: \( w[j + 1] \leftarrow v[j] - z_{j+1} \)
13: \( Z_{out} \leftarrow z_{j+1} \)
14: end for

15: Last \( \delta \) cycles:
16: for \( j = n - \delta \ldots n - 1 \) do
17: \( x[n - \delta \ldots n - 1] = y[n - \delta \ldots n - 1] = 0 \)
18: \( v[j] = 2w[j] \)
19: \( z_{j+1} = SELM(v[j]) \)
20: \( w[j + 1] \leftarrow v[j] - z_{j+1} \)
21: \( Z_{out} \leftarrow z_{j+1} \)
22: end for

---
instantiated in each step of the three sub-loops. We present the details of each module and the corresponding digit slice structure in the following.

### 3.3.1 Initialization

During initialization, the algorithm executes for $\delta$ cycles to accumulate sufficient input digits to produce the first output.

Since no output digit is produced during initialization, the modules to generate the output digit are not implemented. The digit slices in the initialization consist of OTFC units and selectors. While the presence of adders either half, full, or their combination depends on the position of the digit slice. The detail of each unit in the initialization stage is as follows:

**On-the-fly Conversion** The redundant SD inputs are required in the conventional form during the recurrence step $j$, which are obtained without any additional delay using the OTFC module; proposed in [15]. Two OTFC units are instantiated for the two operands during initialization and recurrence, each composed of two $2 \to 1$ multiplexers, 2-input OR and AND gates and two registers to store $Q$ and $QM = Q - 1$ as shown in Fig. 8. In each iteration, a new incoming digit is appended in the least-significant digit of either $Q$ and $QM$ registers depending on the value of $q_j + 1$, increasing its width by one bit up to $n+ib$. Two integer bits are initialized as ‘00’ or ‘11’ representing ‘0’ and ‘−1’ for the first positive or negative digit, respectively.

**Selection module during recurrence** SEL block evaluates three bits to compute the output and is therefore larger than the rest of digit slices [17].

**Selection module last $\delta$ cycles**

**Repeated digit slices (RDs)**

**$k^{th}$ digit slice**

**$(k - 1)^{th}$ digit slice**

**Inactive digit slice in an iteration**

**Truncated digit slices**

---

**Figure 6** Signal activity of radix-2 online multiplication algorithm with truncated working precision of $p$ with $\delta = 3$, 2 integer bits ($ib$) and $t = 2$. Different colors of the digit slice refer to their distinct structure as discussed in Section 3.3.1. SEL block evaluates three bits to compute the output and is therefore larger than the rest of digit slices [17].

**Figure 7** Stair-case input shifter array [7].
negative fractional bit respectively. The conversion/append (CA-Reg) registers correspond to the $Q[j + 1]$ register of the OTFC unit. According to the online multiplier’s algorithm, the computation requires advance availability of one of the operands (in this case operand $y$), therefore, the bit width for ‘$y$’ OTFC unit is one bit longer than ‘$x$’ in all iterations.

**Selector** Multiplication is performed by selector, which is a $4 - to - 1$ multiplexer as shown in Fig. 9. Since it receives the inputs from the CA-Reg registers, the width of its inputs also increases up to $p^\delta$ iteration, and then begins to decrease. As there are no inputs in the last $\delta$ cycles, the selector module is instantiated during initialization and recurrence stages only. In each iteration, the signed digit selector can take values from 1, $-1$ or 0, encoded as ‘10’, ‘01’ and ‘00’, for which the selector outputs $x, y, x, y$ or 0 respectively.

**Adder** A [4 : 2] carry-save adder (CSA) is employed to perform the addition of the input operands and the residual. The functionality of this adder is obtained by utilizing two full adders. Intermediate sums and carries are denoted by VS and VC respectively, whereas the final output vectors of sum and carry are denoted as VS and VC respectively. The requirement is to add the two carry-save operands in WS and WC, with the two conventional operands ($x[j] \cdot y_{j+4}^+$) and ($y[j + 1] \cdot x_{j+4}^+$). The reduction is implemented by two carry-save adders as shown in Fig. 10. The [4 : 2] adder has fixed delay of two full adders, which is significantly smaller than the carry-propagate adders.

At any given iteration $j$, the number of bits in $x$ and $y$ are $k + ib + \delta$ and $k + ib + \delta + 1$ respectively, where $k$ are the number of fractional bits in a given iteration. The length of residual registers WS and WC is $k + ib + \delta - 1$ during initialization.

For the low-power implementation, a distinct structure of adder is specified according to the bit position, as shown in different colors in Fig. 6. For the two’s complement representation, multiplication with ‘$-1$’ can be performed by negating the input bits and adding a logical 1 to the unit in the last place (ulp), therefore, the least significant bit $vc_k$ of the $vc[j]$ vector is designated for $c_x$ ($c_x = y_{j+4}^+ \cdot y_{j+4}^-$). The corresponding digit slice to obtain the least significant bits of $vc$ and $vs$ is the red colored slice $k$ from the Fig. 6 and its internal circuit is depicted in Fig. 11(d). It has no adders because the length of vector $y[j]$ is largest and there are no digits to be added, therefore, $y_k$ and $c_k$ are simply copied to $vs_k$ and $vc_k$ respectively.

For the same reason of achieving correct result of multiplication of a vector by ‘$-1$’ in the two’s complement, the least significant bit $VC_k$ of the $VC[j]$ is accounted for $c_x$ ($c_x = y_{j+4}^+ \cdot y_{j+4}^-$). Since the length of vector $x[j]$ is one digit smaller than $y[j]$, $c_x$ is present in the $(k - 1)^{th}$ digit slice. This is the purple colored slice in Fig. 6 and its internal circuit is depicted in Fig. 11(c). The length of the recurrence registers is one bit smaller than that of $x[j]$, therefore a single full adder is employed to add the three input digits $x[j]m$, $y[j]m$, and $c_x$. Furthermore, absence of an adder in the $k^{th}$ place accounts for no output carry, therefore, a permanent ‘0’ is placed at the $vc_{k-1}$ position.

Due to a single full adder in $(k - 1)^{th}$ position, there is no intermediate sum or carry digits, instead, a final sum $vs_k$ and a carry $vc_{k-2}$ is produced. This implies that in the $(k - 2)^{th}$ digit slice, a full adder in the first stage and a half adder in the second stage is sufficient to produce the outputs. This slice is shown in yellow in Fig. 6 while its logic is shown in Fig. 11(b). The $(k - 2)^{th}$ digit slice however, generates both intermediate and final carry digits to the higher digit slice, therefore, the $(k - 3)^{th}$ digit slice is composed of two full adders. First full adder evaluates the sum of $x[j]$, WS$[j]$, and WC$[j]$ and produces an intermediate carry and sum vector named as VC$[j]$ and VS$[j]$. 

![Figure 8](image1.png)  
**Figure 8** Digit slice of on-the-fly converter.

![Figure 10](image2.png)  
**Figure 10** [4:2] carry-save adder using two stages of full adders [16].

![Figure 9](image3.png)  
**Figure 9** Digit slice of selector unit.
respectively. The second full adder evaluates the sum of \( VS[j], VC[j], \) and \( y[j + 1] \) to produce final sum and carry, expressed as, \( vs[j] \) and \( vc[j] \) respectively, and are collectively represented as \( v[j] \) shown in Eq. 35. This grey colored digit slice from Fig. 6 is implemented using the logic shown in Fig. 11(a). It is named as repeated digit slice (RD) as the same digit slice is repeated 

\[ \text{Residual Calculation} \] In the initialization phase, the residual for the next iteration \((2w[j + 1])\) corresponds to the left shifting of \( vs \) and \( vc \) vectors. The most significant \( ibs \) of both vectors (i.e., \( vs_{-1} \) and \( vc_{-1} \)) are discarded and the vectors are left shifted by a simple re-wiring. The updated residual \((2w[j + 1])\) is shown in relation (34).

\[ 2w[j + 1] \begin{bmatrix} vs_0 & vs_1 & vs_2 & vs_3 & vs_4 & \ldots \\ vc_0 & vc_1 & vc_2 & vc_3 & vc_4 & \ldots \end{bmatrix} \]  
\[ \begin{bmatrix} v_{-1} & v_0 & v_1 & v_2 & \ldots \end{bmatrix} \]

(34)

\[ \text{V Block} \] The output is based on the estimate \((\hat{v}[j])\) of the residual \((v[j])\) and is evaluated in the V block. It is a carry propagation adder that performs the addition of \( t \) most significant fractional bits and the integer bits of \( v[j] \) (represented by \( vs[j] \) and \( vc[j] \) vectors shown in Eq. (35)) to generate the estimate of the residual \((\hat{v})\) as shown in Eq. (36).

\[ v[j] = \begin{bmatrix} vs_{-1} & vs_0 & vs_1 & vs_2 & vs_3 & vs_4 & \ldots \\ vc_{-1} & vc_0 & vc_1 & vc_2 & vc_3 & vc_4 & \ldots \end{bmatrix} \]

(35)

\[ \hat{v} = \begin{bmatrix} v_{-1} & v_0 & v_1 & v_2 & \ldots \end{bmatrix} \]

(36)

\[ \text{SELM Module} \] The result of the V block is subjected to the SELM module for selecting the corresponding output from a look-up table shown in Table 1. In case of radix-2 online multiplier, the least significant estimate bit \( v_2 \) is not used and the three MSBs i.e., two \( ibs \) \((v_{-1} \) and \( v_0)\) and one fractional bit \( (v_1)\) are sufficient to select the output \( z_{j+1} \).

\[ \text{M Block} \] It performs the subtraction of \( z_{j+1} \) from the residual’s estimate \((\hat{v})\) to produce \( 2w[j + 1] \). The subtraction to obtain \( v^p_0 \) is performed using the following Boolean expression [14]:

\[ v^p_0 = v_0 \times OR |p_{j+1}| \]

(37)

\[ \text{Adders} \] The RDs and the least significant digit slices for adder are similar to the initialization stage, and for \( k \) bit precision, \( k + ib - 3 \) number of RDs are instantiated in a certain iteration. The length of the vector \( vc \) after being subjected to V block is reduced by 3 bits (refer to Eq. (38)). Therefore, in the 3 most significant bit slices, which accounts for the SEL block, instead of two stages of full adders, a half adder is employed in the first stage and a full adder is employed in the second stage. The multiplication of the terms \( x[j] \cdot y_{j+4} \) and \( y[j + 1] \cdot x_{j+4} \) in the recurrence equation with \( 2^{-3} \) in both
initialization and recurrence stages corresponds to the sign extension of the MSBs, which is done by performing 3 bit arithmetic right shift operation without any additional cost.

**Residual** The MSB of \( \hat{v}_j \) i.e., \( \hat{v}_{-1} \) is discarded and the remaining 3 bits are vertically transferred to \( v_s \) vector consequently resulting in an updated residual as shown in relation (38). In this manner the left shifting of the residual (2\( w[j] \)) is carried out.

\[
2w[j + 1] v_0 v_1 v_3 v_4 v_5 \ldots v_3 v_4 v_5 \ldots 
\]

### 3.3.3 Last \( \delta \) Cycles

The remaining output digits are obtained in the last \( \delta \) iterations which produces one output digit in each cycle. All the inputs are utilized in the initialization and recurrence stages in the non-pipelined online multiplier, and three 0s are applied as an input for last \( \delta \) iterations. However, in the proposed low-power design, all unused modules are eliminated and therefore, the OTFC, selector, and \([4 : 2]\) adders

![Figure 12](image12.png)

*Figure 12* Logic for the SEL digit slice during recurrence. The three MSBs are composed of a combination of half and full adders in contrast to two full adders in the repeated digit slices.

![Figure 13](image13.png)

*Figure 13* Logic for the MSB in last \( \delta \) cycles. The SEL digit slice is simplified to a carry propagation adder, SELM, and M block; taking the shifted residuals as input and producing an output in each cycle.
are not implemented. The residual containing two vectors \( WS \) and \( WC \) are subjected to the \( V, M, \) and \( SELM \) modules to perform their respective tasks and generate the output digit. The digit slice used during the last \( \delta \) iterations has been depicted in Fig. 13.

### 3.4 Pipelined Serial-Parallel Multiplier

With one operand available in parallel, the circuitry for serial-parallel multiplier is simplified. As shown in Fig. 3, the multiplier does not have OTFC modules and requires \( [3:2] \) adder i.e., only one stage of full adder in each bit slice. The range of input and output is similar to serial-serial, thus same selection function is employed. The truncation strategy for serial-parallel multiplier has not been adopted, rather the entire \( n \)-bit operand is utilized during all iterations. However, as shown in Algorithm 4, the algorithm has been divided into three sections namely initialization, recurrence, and last \( \delta \) cycles.

The block diagram corresponding to each step of the algorithm is shown in Fig. 14. It can be observed that in each stage, only the corresponding circuits are instantiated to reduce area utilization and power consumption. For instance, in the initialization step shown in Fig. 14a, the modules for output generation are not instantiated. Likewise, in the last \( \delta \) cycles, where the input is 0, the modules for input are not instantiated as shown in Fig. 14c. During recurrence however, an input is received and an output is produced in each cycle, the corresponding block diagram is depicted in Fig. 14b.

To select the output digit, the selection function takes \( t = 2 \) fractional bits and 2 integer bits from the estimate computed by \( V \) block. The selection function is same as of serial-serial online multiplier shown in Table 1.

### 4 Results

#### 4.1 Empirical Analysis

We use Mentor Graphics ModelSim to verify the correctness of logical operation of the Verilog codes developed for the proposed and contemporary multipliers. A case study to show the effect of reduction in working precision has been presented for 16-bit precision serial-serial multiplier with the following operands:

\[
x = 0.11010110110110100 \\
y = 0.11101101111011011
\]

The numerical value of \( x \) and \( y \) is 0.66644287109375 and \(-0.31562805175781\) respectively. The actual product in conventional form is \(-0.2103480650112033\) and the calculated product from online multiplier is \(-0.2103424072265625\). The difference between the actual and calculated product is \(5.657784640789032 \times 10^{-6}\) which is well under the error bound of the last iteration which is \(2^{-16} = 1.52587890625 \times 10^{-5}\). Not only the final result, but the result of the online multiplier in each cycle is within the

---

**Algorithm 4** Proposed Pipelined Serial-Parallel Online Multiplication

1. Initialize:
   \[
x[-2] = w[-2] = 0
\]
2. for \( j = -2, -1 \) do
3. \[
v[j] = 2w[j] + (x_{j+2}, Y]) 2^{-2}
\]
4. \[
w[j + 1] \leftarrow v[j]
\]
5. end for

6. Recurrence:
7. for \( j = 0 \ldots n + \delta \) do
8. \[
v[j] = 2w[j] + (x_{j+2}, Y]) 2^{-2}
\]
9. \[
z_{j+1} = SELM(v[j])
\]
10. \[
w[j + 1] \leftarrow v[j] - z_{j+1}
\]
11. \[
Z_{\text{out}} \leftarrow z_{j+1}
\]
12. end for

13. Last \( \delta \) cycles:
14. for \( j = n - \delta \ldots n - 1 \) do
15. \[
v[j] = 2w[j]
\]
16. \[
z_{j+1} = SELM(v[j])
\]
17. \[
w[j + 1] \leftarrow v[j] - z_{j+1}
\]
18. \[
Z_{\text{out}} \leftarrow z_{j+1}
\]
19. end for
respective error bound according to relation (4). In the event of variable precision requirement, the computation can be stopped upon reaching the desired precision, resulting in an accurate result up to that precision; unlike approximate circuits in which the result is not accurate.

For reduced working precision for $n=16$, $p=13$ was evaluated from relation (33). The digit slices are gradually increased according to the increasing precision of the inputs until $p - \delta$ cycles. Truncation is applied in $p - \delta + 1$ cycle that introduces an error in positions $p$, $p - 1$, and $p - 2$ which propagates to the left for residual calculation ($2w[j]$). Consequently, the 3 least significant digit slices affected by the truncation error are not implemented in the forthcoming cycles. For the last $\delta$ iterations, the modules for input and carry-save adder are not present and one bit reduction in the digit slice is due to the left shift operation of the residual. The input digits used in the proposed design are shown in clear fonts in Table 2, whereas the pipelined design without precision reduction uses both clear and shaded digits. The $[4:2]$ adder takes two inputs from Selector units and residuals $WS$ and $WC$, generating redundant vectors $VS$ and $VC$, the sum of which is shown as $v[j]$ in Table 2.

4.2 Synthesis Results and Experimental Setup

Conventional multipliers are implemented either sequentially, or using combinational approach. The sequential multiplier computes the result recursively using a single adder and produces the product in $n$ steps. The combinational implementation, however, is composed of several adders arranged to form either an array or tree for partial product reduction. The product is computed in 1 cycle, however, the cycle time of combinational designs depends on the operand’s width and is larger than the sequential designs. We use a sequential multiplier from [18] and a linear array based

Figure 14 Proposed stages of pipelined online multiplier.

(a) Initialization stage: inputs are received and number bit-slices increase in each cycle. No output is produced, therefore, $V$, $M$ and $SELM$ modules are not instantiated.

(b) Recurrence stage: all modules are functional and follow gradual activation/deactivation of bit-slices.

(c) Last $\delta$ cycles: input is 0, therefore, the input reception modules are removed from the design.
The behavioral description of all the designs for 8, 16 and 32 bits precision including non-pipelined and pipelined online multipliers as well as the conventional multipliers were written in Verilog. Their functional verification was done using ModelSim. The designs for all the multipliers cycle. \( \delta_{ss} \) and \( \delta_{sp} \) depicts the online delays for online serial-serial and online serial-parallel multipliers respectively. For large number of vectors i.e., \( K >> n \), the delay to fill pipeline is negligible and therefore, the proposed pipelined designs have significant advantage over other designs. With the precision independence, short and fixed critical path, the proposed online arithmetic-based designs can be operated at higher frequencies compared to conventional arithmetic based multiplier designs.

The number of clock cycles required to compute \( K = 8 \) products of two input vectors with \( n \) bits.

| \( j \) | \( y_{j+4} \) | \( x_j \) | \( y_{j+1} \) | \( v_j \) | \( p_{j+1} \) | Error bound |
|---|---|---|---|---|---|---|
| -3 | 1 | 1 | 0.0000000000000000 | 1.1000000000000000 | 0.0000000000000000 | 11.1111 | - | - | - |
| -2 | 1 | 1 | 0.1000000000000000 | 1.1000000000000000 | 0.0000000000000000 | 11.1111 | - | - | - |
| -1 | 0 | 0 | 0.1000000000000000 | 1.1010000000000000 | 0.0000000000000000 | 11.1111 | - | - | - |
| 0 | \( T \) | 1 | 0.1010000000000000 | 1.1010000000000000 | 0.0000000000000000 | 11.110000000000000 | 0 | 0.0 | 2 \( ^{-1} \) |
| 1 | 0 | 1 | 0.1010000000000000 | 1.1010000000000000 | 0.0000000000000000 | 11.010000000000000 | \( \bar{T} \) | -0.25 | 2 \( ^{-2} \) |
| 2 | \( T \) | 0 | 0.1010000000000000 | 1.1010000000000000 | 0.0000000000000000 | 00.0100000000000000 | 0 | -0.25 | 2 \( ^{-3} \) |
| 3 | \( T \) | \( T \) | 0.1010000000000000 | 1.1010000000000000 | 0.0000000000000000 | 1.0010000000000000 | 1 | -0.1875 | 2 \( ^{-4} \) |
| 4 | 0 | 1 | 0.1010000000000000 | 1.1010000000000000 | 00.0000000000000000 | 11.010000000000000 | \( \bar{T} \) | -0.21875 | 2 \( ^{-5} \) |
| 5 | 1 | 0 | 0.1010000000000000 | 1.1010000000000000 | 00.0000000000000000 | 11.010000000000000 | 0 | -0.21875 | 2 \( ^{-6} \) |
| 6 | 1 | 1 | 0.1010000000000000 | 1.1010000000000000 | 01.0000000000000000 | 11.010000000000000 | 1 | -0.2109375 | 2 \( ^{-7} \) |
| 7 | \( T \) | \( T \) | 0.1010000000000000 | 1.1010000000000000 | 00.0000000000000000 | 11.010000000000000 | 0 | -0.2109375 | 2 \( ^{-8} \) |
| 8 | 0 | 1 | 0.1010000000000000 | 1.1010000000000000 | 00.0000000000000000 | 11.010000000000000 | \( \bar{T} \) | -0.2109375 | 2 \( ^{-9} \) |
| 9 | \( T \) | 1 | 0.1010000000000000 | 1.1010000000000000 | 00.0000000000000000 | 11.010000000000000 | 1 | -0.2099609375 | 2 \( ^{-10} \) |
| 10 | 1 | \( T \) | 0.1010000000000000 | 1.1010000000000000 | 01.0000000000000000 | 11.010000000000000 | \( \bar{T} \) | -0.21044921875 | 2 \( ^{-11} \) |
| 11 | 0 | 0 | 0.1010000000000000 | 1.1010000000000000 | 00.0000000000000000 | 11.010000000000000 | 0 | -0.21044921875 | 2 \( ^{-12} \) |
| 12 | 0 | \( T \) | 0.1010000000000000 | 1.1010000000000000 | 00.0000000000000000 | 11.010000000000000 | 1 | -0.2103271484375 | 2 \( ^{-13} \) |
| 13 | - | - | - | - | - | - | 11.010000000000000 | 0 | -0.2103271484375 | 2 \( ^{-14} \) |
| 14 | - | - | - | - | - | - | 11.010000000000000 | \( \bar{T} \) | -0.210357666015625 | 2 \( ^{-15} \) |
| 15 | - | - | - | - | - | - | 00.1010000000000000 | 1 | -0.2103424072265625 | 2 \( ^{-16} \) |

\( \delta_{ss} = 3 \), \( \delta_{sp} = 2 \)

Table 3 Number of clock cycles required to compute \( K = 8 \) products of two input vectors with \( n \) bits.
were synthesized using Synopsys design compiler with GSCL 45nm Liberty cell library from the Free45PDK. It was aimed to find the shortest critical path of each design therefore, all designs were time constrained to obtain the maximum achievable frequency. Tables 4, 5, and 6 present the post-synthesis results for online pipelined/non-pipelined serial-serial and serial-parallel multipliers along with conventional multiplier designs for 8, 16, and 32 bit precision respectively. As discussed earlier, this pipeline filling time is negligible for a large number of vector computation and therefore, not considered while computing the performance and performance density. The evaluation of the designs has been presented for several parameters discussed in the following sections.

### 4.2.1 Period

Several multiplier types require different number of clock cycles to produce the result according to the precision of operands and implementation. The multiplier implemented using combinational logic takes one clock cycle to produce the output, however, the cycle time or period of the clock varies correspondingly. Therefore, we present the results of the period to show the critical path. All the designs were time constrained to yield the smallest critical path, or in other words, the designs were executed at the maximum achievable frequency. It can be observed that the period for the conventional multipliers is dependent on the word size, whereas the online multipliers have smaller cycle time. The

### Table 4 Synthesis results for several 8 bit multipliers using Synopsys Design Compiler with GSCL 45nm technology.

| Design          | Sequential [18] | Array [19] | Non-Pipelined Online Serial-Serial [16] | Non-Pipelined Online Serial-Parallel | Pipelined Online Serial-Serial | Pipelined Online Serial-Parallel |
|-----------------|-----------------|-----------|----------------------------------------|-----------------------------------|-------------------------------|----------------------------------|
| Period (ns)     | 0.84            | 1.19      | 0.75                                   | 0.50                              | 0.75                          | 0.50                             |
| Latency (ns)    | 8 cycles = 6.72 | 1 cycle = 1.19 | 11 cycles = 8.25                       | 10 cycles = 5.00                  | 11 cycles = 8.25              | 10 cycles = 5.00                 |
| Area (μm²)      | 1,174.94        | 1,315.44  | 1,614.39                               | 459.91                            | 5,174.5                       | 3,516.94                        |
| Power (mW)      | 0.91            | 0.06      | 1.71                                   | 0.57                              | 5.38                          | 4.27                            |
| EDP (zJ)        | 0.64            | 0.09      | 0.96                                   | 0.14                              | 0.37                          | 0.13                            |
| Performance     | 1 vector/8 cycles = 0.14 x 10⁹ OPS | 1 vector/1 cycle = 0.84 x 10⁹ OPS | 1 vector/12 cycles = 0.12 x 10⁹ OPS | 1 vector/11 cycles = 0.20 x 10⁹ OPS | 1 vector/1 cycle = 1.33 x 10⁹ OPS | 1 vector/1 cycle = 2.00 x 10⁹ OPS |
| Performance Density | 0.85E-03 OPs/1μm² | 0.76E-03 OPs/1μm² | 0.61E-03 OPs/1μm² | 2.17E-03 OPs/1μm² | 1.54E-03 OPs/1μm² | 2.27E-03 OPs/1μm² |

*OPS Operations per second, OPs Number of operations*

Assuming δ = 3 for online serial-serial and δ = 2 for online serial-parallel multipliers

### Table 5 Synthesis results for several 16 bit multipliers using Synopsys Design Compiler with GSCL 45nm technology.

| Design          | Sequential [18] | Array [19] | Non-Pipelined Online Serial-Serial [16] | Non-Pipelined Online Serial-Parallel | Pipelined Online Serial-Serial | Pipelined Online Serial-Parallel |
|-----------------|-----------------|-----------|----------------------------------------|-----------------------------------|-------------------------------|----------------------------------|
| Period (ns)     | 0.90            | 1.60      | 0.75                                   | 0.50                              | 0.75                          | 0.50                             |
| Latency (ns)    | 16 cycles = 14.40 | 1 cycle = 1.60 | 19 cycles = 14.25                       | 18 cycles = 9.00                  | 19 cycles = 15.25              | 18 cycles = 9.00                 |
| Area (μm²)      | 2,604.15        | 7,816.83  | 2,458.66                               | 814.70                            | 16,408.14                     | 11,561.00                       |
| Power (mW)      | 1.80            | 0.57      | 2.40                                   | 1.11                              | 16.88                         | 15.04                           |
| EDP (zJ)        | 1.46            | 1.46      | 1.35                                   | 0.27                              | 0.59                          | 0.23                            |
| Performance     | 1 vector/17 cycles = 0.06 x 10⁹ OPS | 1 vector/1 cycle = 0.62 x 10⁹ OPS | 1 vector/20 cycles = 0.07 x 10⁹ OPS | 1 vector/19 cycles = 0.11 x 10⁹ OPS | 1 vector/1 cycle = 1.33 x 10⁹ OPS | 1 vector/1 cycle = 2.00 x 10⁹ OPS |
| Performance Density | 0.38E-03 OPs/1μm² | 0.12E-03 OPs/1μm² | 0.40E-03 OPs/1μm² | 1.23E-03 OPs/1μm² | 0.97E-03 OPs/1μm² | 1.38E-03 OPs/1μm² |

*OPS Operations per second, OPs Number of operations*

Assuming δ = 3 for online serial-serial and δ = 2 for online serial-parallel multipliers
cycle time of the online multipliers remains constant when they are pipelined and is independent of word length, suggesting the opportunity to execute them at much higher frequency. The cycle time of online multiplier with both operands in serial is approximately 12%, 20%, and 92% smaller for 8, 16, and 32 bit sequential multiplier respectively. Comparing it with combinational multiplier, a reduction of approximately 58%, 113%, and 326% is observed for 8, 16, and 32 bit multipliers. Online serial-parallel multiplier has approximately 68%, 80% and 188% smaller cycle time for 8, 16, and 32 bit designs of sequential multiplier. Comparing it with the combinational multiplier, a reduction of approximately 138%, 220%, and 540% cycle time is observed for 8, 16, and 32 bit multiplier designs respectively.

4.2.2 Latency

Latency of the online multipliers depend on the precision of the operands and the online delay. However, the inter-operating latency depends on only, which is fixed and small. For a series of online operations, the overall latency is the sum of online delays of the corresponding operation and is independent of precision. This implies that the use of online arithmetic based algorithms is even better for wider word sizes and long chains of data dependent operations.

4.3 Power, Performance and Area (PPA)

The proposed pipelined designs have been optimized to have savings in area and power. They account for higher area utilization and power consumption than the non-pipelined online and conventional multipliers. However, it is noteworthy that for $K$ number of vector multiplication, each pipeline stage is computing inputs from a distinct vector as shown in Fig. 5, ultimately increasing the performance and performance density than the non-pipelined and conventional multipliers. The pipelined online multiplier with reduced working precision has 38% and 44% less power consumption and area utilization respectively than the pipelined online multiplier with full working precision design [12]. Both dynamic and static power of each designs have been considered and results of total power have been reported for 8, 16, and 32 bit multiplier designs in Tables 4, 5, and 6 respectively.

The throughput of the multipliers in OPS (operations per second) has been reported as performance metric. The pipelined designs produce one vector per cycle in steady state, whereas the number of clock cycles to produce a vector output by the non-pipelined online designs depends on the word size hence increases linearly with the bit precision. An improvement of approximately 88%, 94%, and 98% is observed for 8, 16, and 32 bit precision in pipelined online serial-serial multiplier compared with sequential multiplier respectively. Similarly, an improvement of approximately 36%, 53%, and 76% is observed for 8, 16, and 32 bit precision in pipelined online serial-parallel multiplier respectively. Pipelined serial-parallel multiplier shows even better performance. In particular, it shows performance improvement of approximately 92%, 96%, and 98% compared to the 8, 16, and 32 bit precision sequential multipliers respectively. Furthermore, an improvement of approximately 58%, 68%, and 84% is observed for 8, 16, and 32 bit precision, respectively, when compared with the performance of combinational multiplier.

4.3.1 Energy-Delay Product (EDP)

Energy delay product is useful metric that shows the delay of an operation times the energy consumed to perform that operation. Smaller values of energy-delay product suggest a more energy-efficient design [20]. The results of EDP metric
have been shown in Tables 4, 5, and 6 in the order of zepto-Joules ($10^{-21}$J).

4.3.2 Performance Density

Performance density is a useful metric to perceive the actual performance of the proposed designs. It is defined as the number of operations performed per unit area. The proposed implementation results in a higher performance density compared to the conventional designs. In particular, for 32-bit precision, the pipelined online multiplier with both serial inputs has approximately 69% and 95% higher performance density than sequential and combinational multipliers respectively. Similarly, the pipelined online multiplier with one input in parallel shows 74% and 96% higher performance density than sequential and combinational multipliers for 32-bit precision.

5 Conclusion

In this paper, we present online arithmetic-based serial-serial and serial-parallel multipliers which have been pipelined such that in a steady state, one vector is generated in each cycle. The properties of the online arithmetic not only allows massive pipelining of the successive operations regardless of the data dependency, the signal activity of the algorithms can also be reduced. The digit serial nature of the online arithmetic and possibility to reduce the maximum working precision, due to which $n$ bit precision result can be obtained by employing $p < n$ bits, manifest the reduction of active slices and signal activities which results in saving power and area during implementation. Several precision multipliers are proposed and compared with the conventional online multipliers. The proposed designs have been synthesized using Synopsys design compiler with GSCL 45nm technology. Results show that the proposed designs produce accurate results with higher throughput and have better performance density compared to other designs. In future, we shall utilize the proposed designs to interface with the online arithmetic based adder to present kernels including matrix multiplication, FFT, sum-of-products, etc., for several real World applications.

Supplementary Information The online version contains supplementary material available at https://doi.org/10.1007/s11265-023-01856-w.

Acknowledgements This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2020R1I1A3063857). The EDA tool was supported by the IC Design Education Center (IDEC), Korea.

Data Availability Not Applicable.

Declarations

Conflict of Interest The authors declare that they have no competing interests.

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