Analysis and design of gradient descent based pre-synchronization control for synchronverter

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Abstract
Synchronverter (SV) control has emerged as a popular method for distributed energy resources (DERs), to emulate response of a synchronous generator. In this work, a simple gradient descent based pre-synchronization control for SV scheme is proposed that varies the reference frequency in SV control alone. Thus, local load connection to DER can remain intact during synchronization with proposed pre-synchronization method, unlike virtual current based methods. Normally, phase-locked loop used for synchronization purpose, uses a first order loop filter such as a PI controller. In the proposed pre-synchronization control, the inherent low pass filter of SV scheme itself is used as a loop filter. Transient response analysis is presented in this work, based on small signal transfer functions derived from the proposed method. From the theoretical analysis of proposed pre-synchronisation control, design of the parameters is presented. Thus, there is no trial and error basis for parameters tuning in the proposed method, as compared to virtual current based methods. Validation of proposed pre-synchronisation control through experiments are presented for all initial conditions. The transient response analysis, effectiveness of proposed method during local load changes and grid integration are verified by experimental results.

1 | INTRODUCTION

The usage of distributed energy resources (DERs) has been steadily increasing for utility grid systems and microgrid systems as well. In the conventional current controlled DERs, there are drawbacks relating to the transient behaviour, which in turn raise stability concerns [1]. In order to solve these issues, several concepts like virtual inertia [2, 3], virtual synchronous generator (VSG) [4, 5], synchronverter (SV) [6], etc. have been proposed lately, in order to mimic behaviour of synchronous generators (SG). The SV control is a popular one among them and there have been several improvements [7–11] to the original SV control. An important improvement is the self-synchronisation feature as given in [11]. With the usage of self-synchronisation feature, the DER voltage is synchronised with the grid voltage during the start-up stage of DER and thereby eliminating the need of a phase-locked loop (PLL). The process of synchronising DER voltage to grid voltage, before connecting DER to the grid is known as pre-synchronisation. This process is necessary so as to avoid the high inrush current while connecting DER to the grid.

The self-synchronisation feature in [11] was based on the concept of reducing a virtual current to zero. The virtual current is fed to the SV control instead of the actual inverter current and it is calculated from the inverter voltage, grid voltage and a virtual impedance. However, the virtual impedance is tuned by trial and error. The concept of virtual current based self-synchronisation, is developed from the simple circuit of SG connected to an infinite bus source. But in this circuit, when the phase difference between SG and bus voltage is beyond $-\pi/2$ or $+\pi/2$, the rotor of SG rapidly accelerates and loses synchronisation with the infinite bus. The response during self-synchronisation process for the aforementioned scenario has not been discussed in [11]. Also, an additional PI controller was
used during synchronisation to generate the incremental reference frequency, without detailing the design of PI controller parameters.

In [12], the resemblance between structure of droop control and PLL was used along with virtual current concept of [11], to demonstrate self-synchronisation ability for droop controlled DERs. The self-synchronisation concept in [11] was also applied to the universal droop control scheme in [13]. A current-limiting droop control for a single-phase system was proposed in [14], along with the self-synchronisation ability based on virtual current concept in [11]. However, the synchronisation performance with initial phase difference beyond $-\pi/2$ or $+\pi/2$ has not been addressed in [12–14]. In [15], a single-phase SV with current limitation capability has been proposed and the virtual current concept of [11] was used for self-synchronisation. A term based on $\pi/2$ phase shifted voltage was added to the reference voltage generation and due to this term self-synchronisation was achieved for the full range of initial phase difference, that is, $(-\pi, +\pi)$. In [16], a self-synchronising three-phase SV control is presented, where a virtual resistance branch is used for calculating virtual active and reactive power feedback signals. A coordinate transformation was used while calculating virtual active and reactive power signals, which allows synchronisation for the full range of phase difference. Even though the problem of higher initial phase difference was addressed in [15] and [16], there are other common drawbacks in virtual current based self-synchronisation methods. These drawbacks have been highlighted in the following subsection. PLL based pre-synchronisation methods was applied to VSG in [17–19] and their drawbacks have also been highlighted in the next subsection.

1.1 | Motivation

When virtual current based self-synchronisation methods as given in [11–16] are applied, the actual inverter current cannot be fed to the SV control. Thus, virtual current based methods restrict the connection of local loads to DER, during synchronisation at start-up or at reconnection after fault clearance. Another common drawback of virtual current based pre-synchronisation methods is that the virtual impedance (virtual resistance in case of [16]) and other self-synchronisation parameters (additional PI controller, damping correction factor) are tuned by trial and error. Since the value of virtual impedance and other self-synchronisation parameters vary with power rating of DERs, there may be difficulty in tuning these parameters. Further, there may be difficulty in tuning the self-synchronisation parameters while considering all initial conditions. In PLL based pre-synchronisation methods for VSG [17–19], it is seen that there is no clear design method for the integral or PI control based frequency and phase regulators. Also, all initial conditions have not been considered while designing pre-synchronisation methods in [17–19], which may lead to slow synchronisation or even synchronisation failure.

1.2 | Contributions

- Taking into account the above mentioned limitations, a simple gradient descent based pre-synchronisation method for SV control is proposed in this work. The structure of proposed pre-synchronisation control is such that, it only varies the reference frequency in the SV control. Thus, the inverter current feeding the local load can be given as an input to the SV control during synchronisation and local loads can remain connected to the inverter at all stages of operation. In order to make sure that local load operation is not affected during synchronisation, the SV frequency is limited to a certain range using a saturation block. Also, comprehensive analysis of SV frequency response and time taken for synchronisation is presented in this work for all initial conditions, which includes effect of SV frequency limits.
- PLLs used for synchronisation purpose, has a loop filter along with a phase detector. The loop filter mainly removes the high frequency components after phase detection along with shaping dynamic response, and a first order loop filter such as a PI controller is generally used [20]. The gradient descent based minimisation method also requires a loop filter while applying it for synchronisation. Thus in the proposed pre-synchronisation method, the inherent low pass filter (LPF) of SV control itself is used as a loop filter, instead of an additional PI controller.
- The transient response during pre-synchronisation varies with the variation in loop filter parameters. Hence, a tunable variable is added to the SV control, in order to vary the time constant of inherent LPF in SV control. Using appropriate small signal transfer functions, the analysis of transient response during pre-synchronisation is presented. Based on complete theoretical analysis for all initial conditions, design of pre-synchronisation control parameters using relevant equations is also presented in this work.

The paper is organised as follows. In Section 2, the detailed explanation for the usage of gradient descent method for synchronisation is presented. The complete implementation and analysis of proposed pre-synchronisation control for SV scheme is given in Section 3, along with a comparison study of proposed method with other self-synchronisation methods through simulations. The experimental validation of the proposed pre-synchronisation control is presented in Section 4 and the concluding remarks are given in Section 5.

2 | APPLICATION OF GRADIENT DESCENT METHOD FOR PRE-SYNCHRONISATION

In order to connect a three-phase SG to the grid or point of common coupling (PCC), a pre-synchronisation control is initially used to match the amplitude, frequency, phase angle and phase sequence of SG and the grid voltages. In case of a SV controlled DER too, a pre-synchronisation control is needed.
before connecting to the grid or PCC through a breaker CB2 as shown in Figure 1. The amplitude matching can be easily taken care by varying the modulation index in the PWM unit of control according to the measured RMS value of grid voltage. The simple method for amplitude matching, along with appropriate expressions is presented in the next section. Thus, the phase and frequency matching of inverter voltage with grid voltage becomes an important problem of synchronisation, and the gradient descent method approach for this problem is discussed in detail below. Consider a balanced, 1 p.u. (peak) instantaneous three-phase grid voltage \( \mathbf{u}_{abc} \) of frequency \( \omega_g \) and a 1 p.u. (peak) instantaneous three-phase inverter output voltage \( \mathbf{y}_{abc} \) of frequency \( \omega_{inv} \) as given below:

\[
\mathbf{u}_{abc} = \begin{bmatrix} \sin(\phi_g) & \sin(\phi_g - 2\pi/3) & \sin(\phi_g + 2\pi/3) \end{bmatrix}^T, \tag{1}
\]

\[
\mathbf{y}_{abc} = \begin{bmatrix} \sin(\phi_{inv}) & \sin(\phi_{inv} - 2\pi/3) & \sin(\phi_{inv} + 2\pi/3) \end{bmatrix}^T. \tag{2}
\]

The instantaneous phases \( \phi_g \) and \( \phi_{inv} \) used in above equations are defined as given below, with respect to \( t = 0 \) as reference.

\[
\phi_g = \int_0^t \omega_g(\tau) d\tau \quad \text{and} \quad \phi_{inv} = \int_0^t \omega_{inv}(\tau) d\tau + \delta_{inv}. \tag{3}
\]

Here, \( \delta_{inv} \) is the initial phase angle by which the inverter voltage leads the grid voltage at start of minimisation and this angle \( \delta_{inv} \) will remain as a constant during minimisation. Let an error signal be defined as given below:

\[
\mathbf{e}_{abc} = \mathbf{y}_{abc} - \mathbf{u}_{abc} = \begin{bmatrix} e_a & e_b & e_c \end{bmatrix}^T. \tag{4}
\]

This error signal should be reduced to zero or close to zero in order to achieve synchronisation. The shape of error signal before start of synchronisation will be that of a beat interference pattern, due to the error being the difference of two sinusoids with their frequencies being close to each other. Since the error can be positive as well as negative, a cost function proportional to the square of error is considered, which is defined below:

\[
C = \frac{1}{3} |\mathbf{e}_{abc}^T| |\mathbf{e}_{abc}| = \frac{1}{3} (e_a^2 + e_b^2 + e_c^2). \tag{5}
\]

Upon further simplification of (5) by substituting error signal, the final expression of cost function is obtained as given below:

\[
C = 1 - \cos(\phi_{inv} - \phi_g) = 1 - \cos(\omega_{inv} - \omega_g) \epsilon + \delta_{inv}. \tag{6}
\]

From the expression of cost function, it is observed to be a convex function by considering \( (\phi_{inv} - \phi_g) \) as the variable for the full range of phase difference \((\pi, +\pi)\). The minimum of zero value exists for the cost function when the variable \( (\phi_{inv} - \phi_g) \) is zero, that is, when synchronisation between signals \( y_{abc} \) and \( u_{abc} \) is achieved. As the cost function is convex and a minimum exists, gradient descent approach can be used to minimise this cost function. For this minimisation problem the frequency \( \omega_{inv} \) is varied alone, as the SV control directly controls the frequency of inverter voltage and not the phase angle of inverter voltage. Thus, the variable \( \omega_{inv} \) in this cost function is updated for every \((i + 1)\) step by using the following equation until the convergence is achieved.

\[
\omega_{inv}^{i+1} = \omega_{inv}^i + \Delta \omega_{inv}^i = \omega_{inv}^i - K_i \frac{\partial C}{\partial \omega_{inv}}. \tag{7}
\]

Here \( K_i \) is known as the learning rate or hyper-parameter. The expression for differential of cost function \( C \) with respect to variable \( \omega_{inv} \), which represents the slope of cost function is obtained in terms of the error signal as given below.

\[
\frac{\partial C}{\partial \omega_{inv}} = \frac{2}{3} \begin{bmatrix} \cos(\phi_{inv}) & \cos(\phi_{inv} - 2\pi/3) & \cos(\phi_{inv} + 2\pi/3) \end{bmatrix}^T \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}. \tag{8}
\]

The above equation is obtained by omitting the time term \( t \), in order to arrive at a time invariant equation. Since the time variable is always positive, the sign of slope does not get affected by this omission. The slope of cost function with respect to \( \omega_{inv} \) is further simplified by substituting the expressions for error signal and it is given below in different forms.

\[
\frac{\partial C}{\partial \omega_{inv}} = \sin(\phi_{inv} - \phi_g) = \sin((\omega_{inv} - \omega_g) \epsilon + \delta_{inv}). \tag{9}
\]

The expression in (8) is used in the implementation of proposed pre-synchronisation control, while the simplified form of (8) given in (9), is used for analysis. Upon substituting (9) in (7), the equation of updated frequency during minimisation is obtained as given below:

\[
\omega_{inv}^{i+1} = \omega_{inv}^i + \Delta \omega_{inv}^i = \omega_{inv}^i - K_i \sin(\phi_g - \phi_{inv}). \tag{10}
\]

The following subsection begins with the analysis of gradient descent minimisation for the case of no limits on frequency \( \omega_{inv} \). This analysis helps in understanding, how the instantaneous phase difference and frequency difference are reduced by varying \( \omega_{inv} \) alone. Since there is a local load connected to the inverter during synchronisation, inverter frequency should remain within a specified range, so that local load operation is not affected. Thus, the gradient descent minimisation for frequency being limited within the range of 49.5 and 50.5 Hz is analysed. Numerical simulations for both cases are also presented in the next subsection. It should be noted that, the
The gradient descent minimisation or synchronisation process involves the reduction of frequency difference \((\omega_g - \omega_{\text{inv}})\) and reduction of instantaneous phase difference. As only the frequency \(\omega_{\text{inv}}\) is varied during minimisation, the frequency difference cannot be reduced in the beginning, when there is an initial phase difference, that is, when \(\delta_{\text{inv}}\) is non-zero. Thus, the phase difference caused due to \(\delta_{\text{inv}}\) will be reduced first, followed by reduction of frequency difference. The instantaneous phase difference \((\phi_g - \phi_{\text{inv}}) = ((\omega_g - \omega_{\text{inv}})t - \delta_{\text{inv}})\), will be first reduced to zero by either increasing or decreasing the frequency \(\omega_{\text{inv}}\) to a maximum or minimum peak. Later, the frequency \(\omega_{\text{inv}}\) will move towards the value of grid frequency \(\omega_g\).

The value of frequency \(\omega_{\text{inv}}\) before start of minimisation will be that of nominal frequency. At the start of minimisation, if inverter voltage lags the grid voltage, that is, when \(\delta_{\text{inv}}\) lies in the range of \((-\pi, 0)\), the term \((\phi_g - \phi_{\text{inv}})\) is positive and hence incremental frequency will be positive at the start. Whereas, if inverter voltage leads the grid voltage at start of minimisation, that is, when \(\delta_{\text{inv}}\) lies in the range of \((0, \pi)\), the term \((\phi_g - \phi_{\text{inv}})\) is negative and hence incremental frequency will be negative at the start. From (10), it is seen that the incremental frequency is directly proportional to \(\sin(\phi_g - \phi_{\text{inv}})\). Thus, if \(\delta_{\text{inv}}\) is in the range of \((-\pi, 0)\) there will be a maximum peak during minimisation and if \(\delta_{\text{inv}}\) is in the range of \((0, \pi)\) there will be a minimum peak during minimisation.

Consider the minimisation is started at \(t=0\), and time \(t=t_p\), be the instant when frequency \(\omega_{\text{inv}}\) reaches the peak \(\omega_{\text{inv}}^{(p)}\). Due to instantaneous phase difference \((\phi_g - \phi_{\text{inv}})\) being zero at \(t=t_p\), the following expression is obtained.

\[
\{\omega_{\text{inv}}^{(p)} - \omega_{\text{inv}}\}t_p = -\delta_{\text{inv}}.
\]  

(11)

The above expression is valid for all \(\delta_{\text{inv}}\) in the full range of \((-\pi, +\pi)\). From (11), it is inferred that for a given \(K_l\), the time \(t_p\) will be constant and the peak frequency \(\omega_{\text{inv}}^{(p)}\) will increase, with increase in \(\delta_{\text{inv}}\). Besides, it should be noted that even though the term \((\phi_g - \phi_{\text{inv}})\) becomes zero at instant \(t_p\), the steady state minimum has not been attained yet, as \(\omega_{\text{inv}}\) is not equal to grid frequency. Thus after \(t_p\), the frequency \(\omega_{\text{inv}}\) will move towards the grid frequency from peak value of \(\omega_{\text{inv}}^{(p)}\).

When there are limitations on frequency \(\omega_{\text{inv}}\), it may not reach the peak frequency in order to reduce the initial phase difference. Thus, the frequency will either be at the upper or lower limit \(\omega_{\text{inv}}^{(l)}\) for a particular time \(t_{\text{lim}}\), in order to reduce the instantaneous phase difference \((\phi_g - \phi_{\text{inv}})\) to zero. When

The frequency \(\omega_{\text{inv}}\) corresponds to either 50.5 or 49.5 Hz for negative initial phase difference or positive initial phase difference, respectively. The steady state minimum has not been attained yet at instant \(t_{\text{lim}}\), as the frequency \(\omega_{\text{inv}}\) is not equal to grid frequency. From (12), an important conclusion can be made that the time \(t_{\text{lim}}\) increases linearly with increase in magnitude of \(\delta_{\text{inv}}\).

In order to verify the above analysis and expressions, numerical simulation results of gradient descent based minimisation for the cases of frequency without any limits and with limits are presented in Figure 2. The response given in Figure 2a is that of inverter frequency \(f_{\text{inv}}\) in units of Hz. For this simulation, the frequency of grid voltage is fixed at 50 Hz, while the initial phase difference \(\delta_{\text{inv}}\) is set to \(-\pi/2\) (-1.5708 rad). The initial frequency of inverter voltage is set at 50 Hz and the learning rate parameter is taken as 0.01 for all numerical simulations.
Figure 3  Numerical simulation response of frequency $f_{inv}$ using gradient descent minimisation (a) for grid frequency of 50 Hz and different initial phase differences $\delta_{inv}$, (b) for phase difference of $+\pi/2$ and different grid frequencies $\omega_{g}$.

From Figure 2a, it can be observed that the frequency response for both cases follows the analysis stated earlier. The time $t_{lim}$ and peak frequency $\omega_{p}$ from simulations are used to calculate the phase angle $\delta_{inv}$ using expressions (11) and (12). The calculated $\delta_{inv}$ are $-1.570$ and $-1.572$ rad for cases of frequency without limits and frequency with limits, respectively. With the calculated $\delta_{inv}$ being close to the actual phase angle of $-1.5708$ rad, expressions (11) and (12) are verified for this particular initial condition.

From Figure 2b,c it can be seen that for the case of frequency without limits, the cost function $C$ and phase-error $e_{\phi}$ reduce close to zero around $t=0.25$,s. However, for the case of frequency with limits, the cost function and error steadily decrease to a small value around $t=0.5$,s. From the numerical simulation for frequency without limits, it is evident that the deviation of inverter frequency from nominal value will be high for a large initial phase difference. Thus, saturation limits on inverter frequency is necessary, when local loads are connected during synchronisation.

The proposed method achieves synchronisation by two stages: initially the SV frequency stays at either upper limit or lower limit for a time $t_{lim}$ which depends on the initial phase difference and grid frequency; after $t_{lim}$, the SV frequency reaches the grid frequency value. The calculated $\delta_{inv}$ decreases with increase in the range of frequency limits. For example, if the limits were 47.5 and 52.5 Hz, then the time $t_{lim}$ will be 1/5th when compared to case of 49.5 and 50.5 Hz limits. Thus, the overall time taken for synchronisation decreases with increase of inverter frequency saturation limits.

In order to cover different initial conditions for frequency being limited, numerical simulations are presented for: (i) grid frequency of 50 Hz with different initial phase differences $\delta_{inv}$ in Figure 3a; (ii) initial phase difference of $+\pi/2$ ($+1.5708$ rad) with different grid frequencies in Figure 3b. The time $t_{lim}$ for different cases are obtained from the simulations in Figure 3 and using expression (12), the equivalent phase difference for all cases are computed. The actual phase differences and calculated phase differences for different cases in Figure 3a are shown in Table 1 and they are very close to each other. For the different cases in Figure 3b, the equivalent phase differences are calculated to be $+1.573$, $+1.572$, $+1.57$, $+1.572$, and $+1.571$ rad and these are also close to the actual value of $+1.5708$ rad. Therefore, expression (12) is said to be applicable for all range of initial phase difference and frequency difference conditions.

### 3 PROPOSED GRADIENT DESCENT BASED PRE-SYNCHRONISATION CONTROL FOR SV SCHEME

A standard PLL used for synchronisation, has a phase detector, loop filter and an oscillator as illustrated in Figure 4a. The loop filter has two functions: (a) control of frequency dynamic response so as to maintain stable synchronisation under different disturbances; (b) limiting the high frequency components from phase detector and sending the filtered output $\omega$ to the oscillator. A loop filter of first order is sufficient for a simple PLL in power systems applications and generally a PI controller is used as a loop filter [20].

In the proposed pre-synchronisation control, the inherent LPF of SV scheme is used as the loop filter as shown in Figure 4b. In the SV control, a LPF action is created by the
active power–frequency loop, with SV reference frequency \( \omega^*_{\text{syn}} \) as input and actual SV frequency \( \omega_{\text{syn}} \) as output. While implementing gradient descent minimisation in continuous state for any cost function, the slope of cost function with respect to the variable is multiplied with negative of learning rate and subsequently added to the initial value of the variable. Then, this sum is integrated to obtain the variable of the cost function. Hence in the proposed method, the incremental frequency term of (7) is added to nominal frequency \( \omega_g \) and the sum is sent through LPF of SV to obtain the SV frequency. It should be noted that LPF acts as an integrator for low frequency components. Since the sum of incremental frequency and nominal frequency is given as reference frequency to SV control, the incremental frequency term is represented as \( \Delta \omega^* \) in Figure 4b.

The calculated frequency from SV control, that is, \( \omega^*_{\text{syn}} \) is fed to the saturation block, where the limits on SV frequency are defined. Finally, the phase \( \theta^*_{\text{syn}} \) is calculated from the output of saturation block. Thus, the similarity of proposed presynchronisation control with that of a standard PLL can be seen from Figure 4. The basic SV scheme is briefly presented in the next subsection, followed by the implementation and transient response analysis of proposed pre-synchronisation control.

### 3.1 Basic synchronverter scheme

Based on the mathematical model equations of a simple round rotor SG, the original SV scheme is derived in [5]. The expressions for electrical torque \( T_e \), instantaneous emf \( e^*_{\text{syn}} \) and reactive power \( Q_G \) shown in Figure 5, are obtained from SG model equations. The notations \( \sin \theta^*_{\text{syn}} \) and \( \cos \theta^*_{\text{syn}} \) used in equations of SV scheme are defined as given below for any general angle \( \theta \).

\[
\begin{bmatrix}
\sin(\theta) \\
\sin(\theta - \frac{2\pi}{3}) \\
\sin(\theta + \frac{2\pi}{3})
\end{bmatrix}, \quad \begin{bmatrix}
\cos(\theta) \\
\cos(\theta - \frac{2\pi}{3}) \\
\cos(\theta + \frac{2\pi}{3})
\end{bmatrix}
\]

(13)

An active power loop is used in SV which serves the purpose of frequency droop control along with the regulation of active power. Based on the mechanical equation or the standard swing equation of a basic SG, the active power loop was derived and the equation governing this loop is given below:

\[
f \frac{d\omega_{\text{syn}}}{dt} = T_m - T_e - D_p(\omega_{\text{syn}} - \omega^*_{\text{syn}}).
\]

(14)

The variable \( f \) in (14) is the total moment of inertia referred to rotor. SV frequency \( \omega^*_{\text{syn}} \), being the important variable of SV control, is obtained by the active power loop and upon integrating it, the phase output of SV control \( \theta^*_{\text{syn}} \) is obtained. The mechanical torque \( T_m \) is calculated by dividing reference value of active power \( P^*_g \) with nominal angular frequency \( \omega^*_g \). Hence, based on (14) and expression of electrical torque \( T_e \), the active power loop is implemented as shown in Figure 5. The reactive power control in SV is implemented using an integral control, with inputs of either difference between reference and actual reactive power, or difference between nominal RMS voltage and measured RMS grid voltage. Based on the principle of excitation control in SG, the output of reactive power control is set as excitation flux \( M_j i_j \) and thereby the amplitude of output voltage is controlled. The reactive power loop of SV control can be operated either in voltage droop control mode (\( S_1 \) is open, \( S_2 \) is closed) or fixed reactive power generation mode (\( S_1 \) is closed, \( S_2 \) is open). Generally, fixed reactive power generation with 0 VAr as reference is the preferred mode of reactive power loop operation for grid connected DERs and throughout the paper, this mode is used for simulations and experiments. Thus, in a SV control the input signals are the instantaneous inverter current \( i_{\text{out}} \), the RMS value of grid or PCC voltage \( V^*_g \), nominal voltage \( V^*_n \), active power reference value \( P^*_g \) and reactive power reference value \( Q^*_g \). The output signals from the SV are the reference voltage \( e^*_{\text{syn}} \) and phase \( \theta^*_{\text{syn}} \), which are sent to the space vector pulse width modulation (SVPWM) unit, thereby generating the pulses for the inverter.
Table 2 State of switches used in the overall control

| Mode of operation                        | State of switch |
|------------------------------------------|-----------------|
| Pre-synchronisation                      | $S_1=S_2=\pi/2$, $S_1=1$, $S_2=1$, $S_v$ in position 2 |
| Grid connection with voltage droop control | $S_1=0$, $S_2=1$, $S_1=0$, $S_2=0$, $S_v$ in position 1 |
| Fixed reactive power generation          | $S_1=1$, $S_2=0$, $S_1=0$, $S_2=0$, $S_v$ in position 1 |

3.2 Implementation of proposed pre-synchronisation control

The simple method used for amplitude matching of inverter voltage with that of grid voltage is illustrated in Figure 6. The switch $S_v$ shown in Figure 6 will be in position 2 during pre-synchronisation, so as to calculate amplitude of grid voltage. Thus, the modulation index will be varied according to grid voltage amplitude, which leads to matching of inverter and grid voltage amplitudes. After connection of DER to grid, the switch $S_v$ will be set to position 1. The amplitude calculation for a balanced three-phase voltage ($v_{abc}$) is done using the expression below, where $V_m$ is the phase voltage amplitude [6].

$$
\sum_abc \sqrt{\frac{3}{2}} V_m
$$

In Section 2, the error signal is obtained from difference of p.u. voltage signals. This error signal is implemented using the three-phase instantaneous SV voltage $e_{\text{syn}}$, instantaneous grid voltage $v_g$ and RMS value of grid voltage $V_g$ as given below:

$$
e_{\text{abc}} = \frac{e_{\text{syn}} - v_g}{\sqrt{2}V_g}.
$$

The slope of cost function as in (8), can be implemented using the error signal defined above and $\cos \theta_{\text{syn}}$ term of SV control. Hence, slope of cost function along with the learning rate $K_{p}$, is used to calculate the incremental reference frequency $\Delta \omega^r$ as represented in Figure 5. In order to control the start and end of pre-synchronisation process, a switch $S_{1}$ is used before adding incremental reference frequency $\Delta \omega^r$ to the nominal frequency. The sum of $\omega^r + \Delta \omega^r$ becomes the reference frequency $\omega_{\text{syn}}^r$ for SV control. Also, the droop coefficient is varied using a variable $k'$ and a switch $S_{2}$, so as to vary time constant of LPF in SV control during synchronisation. Since a single SV controlled inverter with a local load is considered in this work, change of droop coefficient during synchronisation does not affect the power supplied to local load. The saturation block with limits of 50.5 and 49.5 Hz is added for SV frequency before feeding it to the integrator as shown in Figure 5.

There are five switches in the control, that is, $S_1$, $S_2$, $S_{11}$, $S_{12}$ and $S_v$. The overall control has three possible modes of operation: pre-synchronisation mode, grid connection with voltage droop control and grid connection with fixed reactive power generation mode. The control always starts in the pre-synchronisation mode and upon completion of synchronisation, the control can be operated in either grid connection with voltage droop control or fixed reactive power generation mode. Also, it should be noted that the circuit breaker CB2 between inverter and the utility grid will be opened during pre-synchronisation mode and subsequently closed at the start of grid connection. The state of all switches in the control during the three modes is listed below.

- **Pre-synchronisation mode**: The switches $S_{11}$, $S_{12}$ are closed and the switch $S_v$ is set to position 2. The state of switches $S_1$ and $S_2$ is not relevant during pre-synchronisation, as the reactive power loop is not involved in this mode.
- **Grid connection with voltage droop control mode**: The switches $S_{11}$, $S_{12}$ are opened and the switch $S_v$ is set to position 1. The switch $S_1$ is opened and switch $S_2$ is closed.
- **Grid connection with fixed reactive power generation mode**: The switches $S_{11}$, $S_{12}$ are opened and the switch $S_v$ is set to position 1. The switch $S_1$ is closed and switch $S_2$ is opened.

The various states of switches in the control for each mode have been summarised in Table 2.

3.3 Transient response analysis of proposed pre-synchronisation control

The transient response during pre-synchronisation is analysed by deriving the small signal based transfer functions in this sub-section. The small signal analysis may not replicate the complete non-linearity of the system, as it linearises the system around an operating point. However, the small signal analysis method is robust enough to study transient responses and design control parameters as shown in [4], [8], [10] and [15]. Hence, small signal analysis is applied for the proposed pre-synchronisation method as well. When pre-synchronisation process is started, the equation of active power loop under this condition is as given below.

$$
\frac{d\omega_{\text{syn}}}{dt} = T_m - T_i - D_p(1 + k')(\omega_{\text{syn}} - \omega_o - \Delta \omega^r).
$$

In (17), the different variables involved during synchronisation are observed to be $T_m$, $T_i$, $\Delta \omega^r$ and $\omega_{\text{syn}}$. Here, the effect of small change in incremental reference frequency on the change in SV frequency alone is considered. Hence, the variables $\Delta \omega^r$ and $\omega_{\text{syn}}$ are replaced with the sum of operating point ($\Delta \omega^r$,
\( \Delta \omega^* = \Delta \omega^t + \Delta \omega^s \) and \( \omega_{\text{syn}} = \omega_{\text{syn}, t} + \omega_{\text{syn}, s} \) \hspace{1cm} (18)

\[
\frac{\hat{\omega}_{\text{syn}}}{\hat{\Delta} \omega^s} = \frac{D_p(1 + k')}{f_s + D_p(1 + k')}, \quad (19)
\]

From the above expression, it is clear that the SV frequency during synchronisation is obtained using the inherent LPF of SV with a time constant \( \tau'_s = f/(D_p(1 + k')) \) and unity gain. In order to include the effect of gradient descent method into small signal analysis, the change in incremental reference frequency and change in SV frequency can be expressed as given below:

\[
\Delta \omega^* = K_f \left( \hat{\delta}_g - \hat{\delta}_{\text{syn}} \right) \quad \text{and} \quad \hat{\omega}_{\text{syn}} = \hat{\Theta}_{\text{syn}} \quad (20)
\]

Based on the final expression of incremental frequency from (10) and using approximations for small signals, first half of (20) is obtained. The change in SV phase \( \hat{\Theta}_{\text{syn}} \) is multiplied with \( \tau'_s \) to obtain \( \hat{\omega}_{\text{syn}} \), since SV phase is obtained by integrating SV frequency. The transfer function between small change in output phase and small change in input phase is analysed, so as to obtain the desired transient response by tuning the loop filter parameters. Hence, by substituting both expressions of (20) into (19), the transfer function between small change in phase of SV \( \hat{\delta}_g \) and small change in phase of grid \( \hat{\delta}_{\text{syn}} \) is obtained as given below:

\[
\frac{\hat{\delta}_{\text{syn}}}{\hat{\delta}_g} = \frac{K_l}{s^2 + \frac{D_p(1 + k')}{f} + \frac{D_p(1 + k')}{f} K_l} = \frac{1}{s^2 + \frac{1}{\tau'_f} s + \frac{1}{\tau'_f} K_l \cdot K_f} \quad (21)
\]

Thus, the parameter in gradient descent method, that is, \( K_f \) and the tunable time constant of LPF in SV, That is, \( \tau'_f \), can be varied to obtain desired transient response. From (21), it is observed that the time taken by SV frequency to reach grid frequency after reduction of phase difference, depends on the time constant of LPF. By comparing (21) with a standard second order transfer function, the damping factor \( \zeta \) is obtained as given below.

\[
\zeta = \frac{1}{2 \sqrt{\tau'_f / K_l}} \quad (22)
\]

The poles or the roots of the transfer function in (21) are calculated to be as given below:

\[
s = \frac{-1 \pm \sqrt{1 - 4 \tau'_f K_l}}{2 \tau'_f}. \quad (23)
\]

The stability and dynamic performance can be analysed by calculating the poles denoted in (23) for different values of the two parameters, that is, \( K_f \) and \( \tau'_f \). Thus, the calculated poles are plotted for two cases: (i) fixed \( \tau'_f \) with increasing \( K_f \) as shown in Figure 7a; (ii) fixed \( K_f \) with decreasing \( \tau'_f \) as shown in Figure 7b. For first case, \( \tau'_f = 10 \) ms and \( K_f \) is increased from 1 to 100, while for second case \( K_f = 100 \) and \( \tau'_f \) is decreased from 100 to 2 ms. Hence, it is observed that with higher \( K_f \) and lower \( \tau'_f \), the poles move to the left side. By choosing desirable transient response and pole locations, the two parameters \( K_f \) and \( \tau'_f \) can be determined. However, the influence of different initial conditions at start of synchronisation must also be considered while determining these parameters. Hence the process in selecting \( K_f \) and \( \tau'_f \) has been detailed in the next subsection.

### 3.4 Design of proposed pre-synchronisation control

The incremental reference frequency \( \Delta \omega^* \) is directly influenced by the learning rate \( K_f \). It should also be noted that, the value of \( \Delta \omega^* \) upon completion of synchronisation must be equal to difference between grid and nominal frequency. Hence, while designing the proposed pre-synchronisation control, \( K_f \) is first calculated and the tunable time constant of LPF in SV \( \tau'_f \), is calculated later using the transfer function analysis. Based on the simplified expression of incremental frequency as given in (9), the parameter \( K_f \) is calculated using the equation given below.

\[
K_f = \frac{\Delta \omega^*_{\text{max}}}{\sin \delta_{\text{conv}}} \quad (24)
\]
Here, $\Delta \omega_{\text{max}}^*$ is the maximum deviation of grid frequency from the nominal value under normal conditions. In this work, the value of $\Delta \omega_{\text{max}}^*$ is taken to be $(2 \times \pi \times 0.5)$ rad/s. Based on the local grid conditions, the value of $\Delta \omega_{\text{max}}^*$ can be chosen. The term $\delta_{\text{conv}}$ corresponds to the instantaneous phase difference between grid and SV voltage after attainment of convergence by gradient descent minimisation. Thus, it is preferred to take a very small value for $\delta_{\text{conv}}$ such as 1°, while calculating $K_l$.

In a second order transfer function, the damping factor is generally tuned to 0.707 for a fast and oscillation free response. After calculation of $K_l$, the time constant $\tau_f'$ can be calculated using (22) for a damping factor of 0.707 and thereby calculate the value of $k'$.

### 3.5 Comparison study

In this subsection, a comparative study of the proposed pre-synchronisation control with virtual current based self-synchronisation methods [11, 16], is presented. From the structure of proposed method given in Figure 5, it is clear that the measured inverter current will not be removed from SV control during synchronisation. Thus, local load can remain connected to DER during synchronisation with the usage of proposed method, unlike virtual current based methods. Further detailed comparison based on synchronisation performance, time taken and parameters design process is given below along with appropriate MATLAB/Simulink simulations.

The single phase equivalent configuration of grid connected DER as shown in Figure 8, is used for simulations. The parameters of configuration and the basic SV control used for all simulations are given in Table 3. The self-synchronisation parameters for methods in [11, 16] were tuned by trial and error for the simulations. In the proposed pre-synchronisation control, the value of $K_l$ is first determined using (24), by considering $\Delta \omega_{\text{max}}^*$ to be $(2 \times \pi \times 0.5)$ rad/s and $\delta_{\text{conv}}$ to be 1°. Upon calculation, $K_l$ is obtained as 180 rad/s. In order to obtain damping factor of 0.707, time constant $\tau_f'$ is calculated using (22). Thus, $\tau_f'$ is obtained as 2.8 ms and eventually the value of $k'$ is calculated to be 2.571 for $J/D_p$ of 10 ms. Thus, the corresponding poles are $-178.6 \pm j178.6$ and with the poles being stable, the designed values of $K_l$ and $k'$ are used.

![Figure 8](image-url)  
**Figure 8** Configuration of grid connected DER with local load

The error $e_{\text{abc}}$ as given in (16), is calculated for all simulations to determine completion of synchronisation. Along with error $e_{\text{abc}}$, the SV frequency is also plotted for all simulations. For all the simulations given in this subsection, the grid frequency is set to 50.1 Hz, so that a frequency difference is created. The saturation limits of the SV frequency is taken as 49.5 and 50.5 Hz for first case of comparison. The simulation results of self-synchronised SV as given in [11] and the proposed pre-synchronisation control is as shown in Figure 9. The pre-synchronisation was enabled at $t=1$ s and the phase difference at $t=1$ s was $+125^\circ$ for both cases. It is mentioned in Section 1 that self-synchronisation method in [11] may not be successful when initial phase difference is beyond the range of $(-\pi/2, +\pi/2)$. Thus, this can be verified as the error $e_{\text{abc}}$ does not reduce to zero, due to the initial phase difference being $+125^\circ$. The SV

### Table 3 Control and configuration parameters

| Parameters | Values | Parameters | Values |
|------------|--------|------------|--------|
| $J$        | 0.0084 kgm² | $D_p$     | 0.84 Nm-s/rad |
| $K$        | 2.726 VAr/rad | $D_q$   | 4.33 VAr/rad |
| $P_g$      | 250 W     | $Q_g$     | 0 VAr   |
| $K_l$      | 180 rad/s | $k'$      | 2.571   |
| $L_f$      | 5 mH      | DC link voltage | 175 V |
| $C_f$      | 15 μF     | Nominal phase RMS voltage | 60 V |

![Figure 9](image-url)  
(a, b) Simulation results of self-synchronised synchronverter in [11]. (c, d) Simulation results of proposed pre-synchronisation control with SV frequency limits of 49.5 and 50.5 Hz
frequency response shown in Figure 9b, reaches the grid frequency of 50.1 Hz in spite of unsuccessful synchronisation and this is due to the additional PI controller in the active power loop. The simulation results for the proposed pre-synchronisation control show that synchronisation has been achieved as the error $e_{abc}$ is reduced to zero. Also, the SV frequency reaches grid frequency of 50.1 Hz from the lower limit 49.5 Hz, with the desired transient response. Using the initial phase difference of $+125^\circ$ in (12), the time $t_{lim}$ is calculated to be 0.578 s and it is close to the actual time of 0.576 s as observed from simulation.

In [16], virtual current based method is used to obtain fast synchronisation for the full range of phase difference. In the proposed pre-synchronisation control too, fast synchronisation can be achieved by having higher saturation limits on SV frequency and these are taken as 45 and 55 Hz for simulations. Thus, the synchronisation time is compared, for the method given in [16] with the proposed pre-synchronisation method through simulation results as shown in Figure 10. The pre-synchronisation is enabled at $\zeta=1\zeta$ and the phase difference at $\zeta=1\zeta$ is $+105^\circ$ for both cases. The simulation results of Figure 10a,b for the method in [16], show that within 100 ms the error has been reduced to zero and the SV frequency has reached the grid frequency of 50.1 Hz. For the proposed method too, the simulation results in Figure 10c,d shows that fast synchronisation within 100 ms is achieved and the desired transient SV frequency response is also obtained. The main advantage of proposed method over the method in [16], is simple calculation of control parameters and detailed discussion on this is given later in this subsection. The time $t_{lim}$ from Figure 10d is observed to be 53 ms and it is close to the calculated value of 57 ms using (12). Thus, the expression (12) is verified for different frequency limits. Further, the speed of synchronisation for the proposed pre-synchronisation method is compared with that of a standard three-phase synchronous reference frame (SRF) PLL as given in [20] through simulations. A standard SRF PLL was simulated with the same initial conditions as in the case of simulations presented in Figure 10, that is, initial phase difference of $+105^\circ$ and grid frequency of 50.1 Hz. By comparing simulation of proposed method in Figure 10 with that of SRF PLL in Figure 11, it can be seen that the synchronisation speed of proposed method is similar to that of a SRF PLL. Thus, fast synchronisation performance as in case of a SRF-PLL, is also achievable by the proposed pre-synchronisation method. Even though synchronisation time for the method in [16] and the proposed method are almost the same, one of the main advantages of the proposed method lies in the simple calculation of pre-synchronisation control parameters. In the original self-synchronisation method [11], parameters including virtual impedance and a PI control had to be tuned by trial and error. For the method proposed in [16], parameters including virtual resistance, damping factor and a parameter in reactive power loop had to be tuned by trial and error. Due to virtual current based self-synchronisation, the parameters vary with power ratings of DER and this leads to difficulty in parameters tuning. Further difficulty in tuning of parameters may arise while ensuring successful synchronisation for all initial conditions, that is, maximum phase difference and maximum frequency difference. The parameters design of proposed pre-synchronisation control as given in previous subsection, is based on equations derived from the gradient descent method analysis and the transient response analysis. From the parameters design equations, it can be seen that the parameters are independent of power ratings. Also, all initial conditions have been considered in parameters design, which ensure successful synchronisation for all conditions. Hence, the design...
of pre-synchronisation parameters for the proposed method is much more simpler upon comparison with virtual current based self-synchronisation methods in [11, 16].

### 3.6 Simulation for unbalanced and distorted grid voltage

The simulation results of proposed pre-synchronisation method for unbalanced and distorted grid voltage condition of 50.1 Hz, with SV frequency limits of 50.5 and 49.5 Hz is presented in Figure 12. The grid voltage as shown in Figure 12a, consists of 5% unbalance in phases a and c along with fifth harmonic component of 10% and seventh harmonic component of 5%. The pre-synchronisation is started at \( t = 1 \) s and the initial phase difference is +150°. From Figure 12b, it can be seen that the SV frequency reaches the grid frequency and it has a ripple of approximately ±0.04 Hz due to the distorted grid voltage. The error \( \varepsilon_{abc} \) caused due to the initial phase difference and frequency difference, reduces from a high value of 2 p.u. to 0.1 p.u. as shown in Figure 12c. The error \( \varepsilon_{abc} \) settles to 0.1 p.u. after synchronisation, as the pre-synchronisation method is designed for tracking the fundamental frequency. Figure 12d,e shows that the phase difference between SV and the distorted grid voltage has reduced. Thus, the simulation results show that the proposed pre-synchronisation is quite robust for distorted grid voltage.

### 4 EXPERIMENTAL VERIFICATION

The configuration used for simulations as shown in Figure 8, is also used for experimental verification. In this work, the VSC/inverter is considered to be fed by a constant dc source DER and the transformer TF is used either for isolation or step up purpose. Upon completion of pre-synchronisation, the breaker CB2 between output of the inverter and the PCC bus will be closed. An equivalent three-phase experimental setup of the configuration is used in this work as shown in Figure 13. The setup is integrated to the grid using a three-phase auto transformer, which is represented as 3ϕ AT in Figure 13. Resistances of 60 Ω are used as the local load in the experimental setup. The SV control and configuration parameters given in Table 3 was also used for the experimental setup. Also, the parameters of proposed pre-synchronisation control used in experiment is the same as the parameters used in simulations, that is, \( K_f = 180 \text{ rad/s} \) and \( k' = 2.571 \). The saturation limits of the SV frequency is taken as 49.5 and 50.5 Hz for experimental verification.

The analysis of proposed pre-synchronisation control for frequency with limits as given in Section 2, is verified by corresponding experimental results of the following first subsection. The results are presented for high positive and negative initial phase difference, with grid frequency being close to 50 Hz. In order to obtain high frequency difference test condition, the nominal frequency was varied beyond 50 Hz and the corresponding results are also presented in the first subsection. As only the performance of pre-synchronisation control is tested, local load was not considered for results in the first subsection. So as to verify the transient frequency response analysis given in Section 3, results with different time constant \( \tau_f' \), are
presented in the second subsection. Also, the effectiveness of pre-synchronisation control for changes in local load during synchronisation is verified by the results presented in second subsection. In the last subsection, the results corresponding to grid integration after closing of breaker CB2 are presented.

4.1 Results for different initial conditions

The experimental results for a high initial phase difference of around 150° and grid frequency close to 50 Hz are as shown in Figure 14. The SV frequency $f_{\text{syn}}$ in Hz, phase-a error $e_a$, SV and grid voltages during the synchronisation process are shown in Figure 14a. At the instant $t_1$, the proposed pre-synchronisation control is enabled and the voltages of SV and grid around this instant are as shown in Figure 14b. The SV frequency is at 50.15 Hz before $t_1$ as no local load was connected. The SV and grid voltages around the instant $t_2$ are shown in Figure 14c and it is seen that mismatch between the two voltages reduces as synchronisation progresses. The SV and grid voltages around the instant $t_3$, that is, after completion of synchronisation, are as shown in Figure 14d. The response of error $e_a$ and SV frequency $f_{\text{syn}}$ in Figure 14a is similar to the simulation results shown in Figure 9c,d, as the $e_a$ steadily decreases to zero and the SV frequency reaches grid frequency with the desired transient response. Using $\delta_{\text{inv}}$ of 150° in (12), the calculated $\tau_{\text{lim}}$ is 0.83 s and it is close to the actual value of 0.82 s as observed from the result. If local load was connected before start of pre-synchronisation, the only difference in the response will be that the SV frequency will be lesser than 50.15 Hz before $t_1$.

The experimental results for a negative initial phase difference of around $-162^\circ$ are as shown in Figure 15. The SV frequency, error $e_a$, SV and grid voltages during the synchronisation process are shown in Figure 15a. At the instant $t_1$, the pre-synchronisation control is enabled and the voltages around this instant are as shown in Figure 15b. The mismatch between SV and grid voltages reduces during synchronisation process as shown in Figure 15c. The SV and grid voltages around the instant $t_3$, that is, after completion of synchronisation, are as shown in Figure 15d. Using $\delta_{\text{inv}}$ of $-162^\circ$ in (12), the calculated $\tau_{\text{lim}}$ is 0.9 s and it is close to the actual value of 0.91 s. Thus, the results in Figures 14 and 15 verify that SV frequency will reach the lower limit for positive initial phase difference and SV frequency will reach the upper limit for negative initial phase difference.

High frequency difference condition is tested in this work by changing nominal frequency $\omega_n$ to 50.4 and 49.6 Hz, while maintaining $P^*_{\text{g}}$ at zero. Experimental results with a positive and negative initial phase difference for a nominal frequency of 50.4 Hz are shown in Figure 16a,b, respectively. Experimental results with a negative and positive initial phase difference for a nominal frequency of 49.6 Hz are shown in Figure 16c,d, respectively. The incremental frequency in units of Hz is represented as $\Delta f^*$ in Figure 16. A saturation of $\pm 1$ Hz was used while recording $\Delta f^*$, so as to obtain the same scale as that of $f_{\text{syn}}$. For all cases in Figure 16, synchronisation was successful as $e_a$ reduces close to zero and $f_{\text{syn}}$ reaches the grid frequency of around 50 Hz. From Figure 16, it can be observed that difference between value of $f_{\text{syn}}$ after synchronisation and nominal frequency (50.4 Hz for Figure 16a,b, 49.6 Hz for Figure 16c,d) is equal to $\Delta f^*$ value after synchronisation for all cases. Also, these results show that LPF in the SV control functions as a loop filter to remove the high frequency ripples from output of gradient descent method, that is, $\Delta f^*$. 
4.2 Results with different $\tau'_f$ and changes in local load

The results for different time constants $\tau'_f$ are presented in Figure 17. For all cases, the synchronisation process was started at the instant $t_1$ and the local load was connected to inverter at instant $t_2$. The results for $J/D_p = 10$ ms with $k'_f$ being zero and with $k'_f = 2.57$ are shown in Figure 17a,b, respectively. Due to $\tau'_f$ being higher in Figure 17a, SV frequency has an oscillatory response. In Figure 17c, the response for $J/D_p = 20$ ms with $k'_f$ being zero is shown. The oscillations of SV frequency in Figure 17c are higher when compared to Figure 17a, due to
increase in $f/D_p$. By using a $k'$ of 6.143 with $f/D_p = 20$ ms, the time constant $\tau'_f$ becomes 2.8 ms and the corresponding results are shown in Figure 17d. When time constant $\tau'_f = J[f/(D_p(1 + k'))]$ increases beyond the calculated value of 2.8 ms, the damping factor will decrease from the desired value of 0.707.

Figure 17     Experimental results of inverter output power ($P_{out}$), error ($e_a$) and SV frequency in Hz ($f_{syn}$) for (a) $f/D_p = 10$ ms with $k' = 0$, (b) $f/D_p = 10$ ms with $k' = 2.57$, (c) $f/D_p = 20$ ms with $k' = 0$ and (d) $f/D_p = 20$ ms with $k' = 6.143$

This leads to more oscillations in SV frequency and higher settling time taken by SV frequency to reach grid frequency and this behaviour is verified for different cases in Figure 17. At the instant when local load is connected, that is $t_2$, the output power of inverter $P_{out}$ starts increasing to 180 W and $f_{syn}$ deviates from the grid frequency for all cases. But, $f_{syn}$ is restored back to the grid frequency after $t_2$ and this shows that synchronisation was maintained even after change in local load. The time taken to reach grid frequency after $t_2$, increases with increase in $\tau'_f$ as shown in Figure 17.

Experimental results for change in local loads during the synchronisation process are also presented here. In the first sequence as shown in Figure 18a, the pre-synchronisation control was enabled at $t_1$ and the local load was connected during synchronisation at $t_2$. From the results, it can be seen that the synchronisation process is unaffected after connection of local load when SV frequency was at the lower limit. In the second sequence as shown in Figure 18b, the local load was initially connected at $t_1$, followed by the start of pre-synchronisation control at $t_2$ and the local load was removed at instant $t_3$. In this case too, $f_{syn}$ is restored to the grid frequency and the synchronisation is still maintained despite the removal of local load at instant $t_3$.

Figure 18     Experimental results of inverter output power ($P_{out}$), error ($e_a$) and SV frequency in Hz ($f_{syn}$) for (a) first sequence of changes in local load and (b) second sequence of changes in local load during synchronisation

4.3 Results of grid integration

The results corresponding to grid integration after completion of synchronisation are presented in Figure 19. The results in Figure 19a,b correspond to the case of local load being
connected to the inverter before grid integration and the results in Figure 19c,d are that of the local load not being connected. After successful synchronisation, the breaker CB2 is closed and the switches (S_s1, S_s2) in pre-synchronisation control are opened at instant \( t_1 \). From Figure 19, it is observed that there are no transients in voltages and currents after grid integration. The change in power \( P_{out} \) from 0 to 250 W in Figure 19c, being higher than the change of 180 to 250 W in Figure 19a.

5 | CONCLUSION

In this work, a simple gradient descent based pre-synchronisation control for SV scheme is proposed, wherein the reference frequency in SV control alone is varied. Thus, the measured inverter current can be fed to the SV control during synchronisation and the local load connection to DER is not disturbed with the usage of proposed pre-synchronisation control. From the analysis and simulations of gradient descent minimisation, it is evident that SV frequency will have a large deviation from nominal value while reducing phase difference. Thus, saturation limits are needed for the SV frequency during synchronisation, so that local load operation is not affected. It is shown that higher saturation limits for SV frequency can be taken to achieve faster synchronisation, but the local load connected in the configuration should be considered before determining the limits.

In the proposed pre-synchronisation control, gradient descent minimisation method acts as a phase detector and the inherent LPF of SV control itself is used as a loop filter. Transient response analysis is presented, based on the small signal transfer functions for the proposed method. Based on the analytical discussion of the proposed method, the design of pre-synchronisation control parameters with relevant equations are presented. From a comparative study, it is seen that the structure and design of parameters in the proposed method is simple, whereas the parameters in virtual current based methods are tuned by trial and error. Efficacy and analysis of the proposed pre-synchronisation control for all initial conditions are validated by experimental studies. Further, the transient response analysis, effectiveness of pre-synchronisation control for changes in local load and the grid integration of a DER with local load are verified by experimental studies.

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