Comparing quaternary and binary multipliers

Daniel Etiemble
Computer Science Laboratory (LRI)
Paris Saclay University
Orsay, France
d@lri.fr

Abstract—We compare the implementation of a 8x8 bit multiplier with two different implementations of a 4x4 quaternary digit multiplier. Interfacing this binary multiplier with quaternary to binary decoders and binary to quaternary encoders leads to a 4x4 multiplier that outperforms the best direct implementation of a 4x4 quaternary multiplier. The far greater complexity of the 1-digit multipliers and 1-digit adders used in this direct implementation compared to the binary 1-bit multipliers and full adders cannot be compensated by the reduced count of quaternary operators. As the best quaternary multiplier includes the corresponding binary one, it means that there is no opportunity to get less interconnects, less chip area, less power dissipation with the quaternary multiplier.

I. INTRODUCTION

Since the 50’s, many implementations of multivalued circuits have been proposed. In the last decade, most proposals used the CNTFET technology.

Most presented implementations of ternary or quaternary circuits claim advantages of multiple valued circuits. The following quote summarizes the arguments that may be found in most of these papers: “MVL circuits have potential advantages. Using MVL circuits reduces the complexity of interconnection via reducing the number of wires since each wire carries more than one digit of data. Power consumption and area of the MVL circuits are generally less than the corresponding binary circuits due to the reduction in number of active elements [1].

We examined ternary circuits in [2] and we compared the implementations of ternary adders and multipliers with the corresponding binary ones in [3]. In [4], we presented the best implementation of quaternaryadders that is compared to the previously proposed ones [5] [6] [7]. In this paper, we examine quaternary multipliers to check the validity of the previous quote for these important combinational circuits.

The implementation of N-digit adders is easily derived from the implementation of 1-digit adders, with variants to speed-up the carry propagations. Multipliers are most complicated as they involve two steps to multiply N x N digits in the common implementations with minimal propagation delays:

- Multiply the ith digit by the jth digit for 0<i<N and 0<j<N. It involves N² 1-digit multipliers
- Sum the different lines of partial products. Reduction trees such as Wallace or Dada trees [8] are generally used

As a N*N multiplier involves both 1-digit multipliers and 1-digit adders, we compare an 8x8 bit multiplier with two 4x4 quaternary digit multipliers. Possible variants of these multipliers are discussed before a final conclusion.

II. METHODOLOGY

A. Why CNTFET technology?

This technology uses field-effect transistors that use a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFETs. The MOSFET-like CNTFETs having p and n types look the most promising ones. The technology has advantages and drawbacks:

- CNTFETs have variable threshold voltages (according to the inverse function of the diameter). This is a big advantage compared to CMOS for which different masks are needed to get different threshold voltages.
- Among advantages, high electron mobility, high current density, high transductance can be quoted.
- Lifetime issues, reliability issues, difficulties in mass production and production costs are quoted as disadvantages.
- CNTFET technology is far from being a mature one. In 2019, a 16-bit RISC microprocessor has been built with 14,000 CNFET transistors [9]. While this is an advance for CNTFET technology, we may observe that the Intel 8086 CPU, which was a 16-bit microprocessor, has been launched in 1978 with 29,000 transistors, more than 40 years ago!

However, as CMOS circuits and CNTFET ones have basically the same circuit styles, CNTFETs can be used to propose a new implementation of quaternary operators and compare it with previous published proposals.

B. Comparing different implementations of quaternary multipliers

The transistor count is used to compare different implementations of quaternary adders. As comparisons are done by using the same technology and the same operators, the transistor count is significant as it is very doubtful that more transistors could lead to:

- less interconnects
- reduced chip area
- reduced power dissipation
TABLE I

TRUTH TABLE OF A QUATERNARY MULTIPLIER

| A | Bi | QS | QC | A | Bi | QM | QC |
|---|----|----|----|---|----|----|----|
| 0 | 0  | 0  | 0  | 2 | 0  | 0  | 0  |
| 0 | 1  | 0  | 0  | 2 | 1  | 2  | 0  |
| 0 | 2  | 0  | 0  | 2 | 2  | 0  | 1  |
| 0 | 3  | 0  | 0  | 2 | 3  | 2  | 1  |
| 1 | 0  | 1  | 0  | 3 | 0  | 0  | 0  |
| 1 | 1  | 2  | 0  | 3 | 1  | 3  | 0  |
| 1 | 2  | 3  | 0  | 3 | 2  | 2  | 1  |
| 1 | 3  | 0  | 1  | 3 | 3  | 1  | 2  |

• reduced propagation delays
• Etc.

III. QUATERNARY CIRCUITS

As previously mentioned, we use the CNTFET technology that as been used in the most recent papers proposing quaternary adders. In [4], we have summarized the different techniques to get 4 voltage levels, either with three power supplies or only one power supply, that have been used in papers [5] [6] [7]. In these last two papers that present both versions, the 3 power supplies versions always use less transistors than the 1 power supply one. Version [7] with 3 power supplies is the best direct quaternary implementation. We use this version for the comparison with binary implementations.

IV. QUATERNARY 1-DIGIT MULTIPLIER

Table I shows the truth table of a 1-digit quaternary multiplier. From Table I, we can observe that:
• When A = 0 then QM = 0 and QC=0
• When A = 1 then QM = B and QC = 0/0/0/1 for B=0/1/2/3
• When A = 2 then QM = 0/2/0/2 and QC = 0/0/1/1 for B = 0/1/2/3
• When A = 3 then QM = 0/3/2/1 and QC= 0/0/1/2 for B = 0/1/2/3

Using the same technique as in [7], the Product and Carry circuits are shown in Fig. 1. The QMux 4:1 presented in [7] is shown in Fig. 2. The different other circuits used in the multiplier are shown in Fig. 3. NQI, IQI and PQI functions correspond to Table II in which binary values are 0 and 3. NQI, IQI and PQI outputs are provided by 3 inverters having 3 different threshold levels. Fig. 4 shows the corresponding circuits presented in [5].

The transistor count depends on the layout. Without this layout, it can be evaluated according to two different ways:
• Count the lower bound of the number of transistors, assuming that fan-out is unlimited and that there is no

Fig. 1. Quaternary multiplier

Fig. 2. QMUX 4:1 presented in [7]

Fig. 3. Multiplier subcircuits

TABLE II

TRUTH TABLE OF DECODER CIRCUITS

| IN | NQI | IQI | PQI |
|----|-----|-----|-----|
| 0  | 3   | 3   | 3   |
| 1  | 0   | 3   | 3   |
| 2  | 0   | 0   | 3   |
| 3  | 0   | 0   | 0   |
TABLE III
QUATERNARY MULTIPLIER TRANSISTOR COUNT

| Input | Circuits | Min Subblock |
|-------|----------|--------------|
| A     | NQI,NQI\,IQI,PQI, PQI/ | 12 24 |
|       | O202,0321 | 10 20 |
|       | 0011,0012 | 10 10 |
|       | MUX4      | 12 12 |
| Total |          | 54 76 |

interconnection issues for the layout. This lower bound is unrealistic. For the multiplier, it means that the same inverter gates (NQI, IQI, PQI, etc) driven by A controls the two Qmux 4:1 and that the same inverter gates driven by B controls the different subcircuits (0202, 0321, 0011, and 0012).

- Assume that QP and QC are two different subblocks. There are separate inverter gates controlling the Qmux 4:1 and the subcircuits in the QP and QC blocks.

The two corresponding transistor counts are given in Table III. The lower bound in 54 T while 76 T is a more realistic value. The 1x1 bit multiplier is implemented by an AND gates (6T). However, a direct comparison cannot be done, as a NxN digit multiplier uses both 1x1 digit multipliers and 1x1 digit adders.

V. A 8 X 8 BIT BINARY MULTIPLIER

Wallace tree is a typical reduction tree used to implement fast combinational multipliers. Dadda tree is another one. Fig. 5 presents this 8*8 multiplier. There are 64 AND gates (1*1 bit multiplier), 38 1-bit adders (FAs) and 15 1-bit half adders (HAs) for the reduction tree. Either a 10-bit Carry Propagate Adder (CPA) or a 10-bit Carry Look-ahead Adder can be used. The CPA would use 9 FAs and 1 HA.

The 1-bit multipliers are implemented with 6 T (Nand + inverter) for a total of 64 x 6 = 384 T. The overall transistor count depends on the implementation of FAs and HAs. A survey was presented in [10]. The transistor counts range from 28 T for the conventional CMOS design down to 8 T for a scheme using 3T Xor gates. Typical implementations with transmission gates use 14 T or 16 T. All circuits are not equivalent: while conventional CMOS design has maximal noise margins, circuits using transmission gates, or directly connecting inputs either to drain or source of transistors can have reduced noise margins. They can have poor driving capability issues and their switching performance degrades drastically in the cascaded mode of operation if the suitably designed buffers are not included. For a fair comparison with quaternary circuits, we will consider a 16 T implementation (such as [11]) and the 28 T of the conventional CMOS design. The transistor count for the 8 x 8 bit multiplier is given in Table IV.

VI. A 4X4 DIGIT QUATERNARY MULTIPLIER WITH QUATERNARY TO BINARY INTERFACES

In this section, we implement a 4x4 digit quaternary multiplier by using a 8x8 bit binary multiplier and quaternary to binary decoders and binary to quaternary encoders.

A. Quaternary to binary interfaces

These interfaces have already been used in [9].

1) Quaternary to binary decoder: Table V presents the truth table of the quaternary to binary conversion. Binary values are 0 and 3. The decoder circuit is presented in Fig. 6. The circuitry is the same using 3 or 1 voltage levels. It is based on the inverters 1, 2 and 3 with the different threshold levels (such as the inverters presented in Fig. 4) followed by usual binary gates. The number of transistors depends on the implementation of the XOR gate. It ranges from 16 T when using 4 Nand gates down to 3 T as proposed in [12]. An acceptable value is 9 T, which corresponds to the conventional CMOS implementation used in [13]. This implementation doesn’t use pass transistors and has a full swing output. The overall transistor count for the decoder is then 21 T.
TABLE V
TRUTH TABLE OF DECODER CIRCUITS

| Q | NQI | IQI | PQI | X1 | x0 |
|---|-----|-----|-----|----|----|
| 0 | 3   | 3   | 3   | 0  | 0  |
| 1 | 0   | 3   | 3   | 0  | 3  |
| 2 | 0   | 0   | 3   | 3  | 0  |
| 3 | 0   | 0   | 0   | 3  | 3  |

Fig. 6. Quaternary to Binary Decoders

2) Binary to quaternary encoder: With 3 power supplies, the encoder can be implemented with the mux approach with pass transistors as shown in Fig. 7. The transistor count including two invertors is 14 T.

3) Interface transistor count: The transistor count for decoding and encoding a quaternary digit is 21 + 14 = 35 T.

Fig. 7. Binary to Quaternary encoder

B. Quaternary multiplier transistor count

When using CPAs for the final step of the Wallace tree, the overall transistor count is given in Table VI.

| Circuit             | 16T FA | 28T FA |
|---------------------|--------|--------|
| Interface           | 35 × 4 = 140 T | 140 T |
| 8x8 bit multiplier  | 1392 T  | 1892 T |
| Total               | 1532 T  | 2032 T |

TABLE VI
TRANSISTOR COUNT FOR THE QUATERNARY MULTIPLIER WITH BINARY INTERFACES

VII. DIRECT IMPLEMENTATION OF A 4 X 4 DIGIT QUATERNARY MULTIPLIER

We now use the 1-digit multiplier presented in section IV. The multiplier has 16 1-digit multipliers. However, as these multipliers generate both a product and a carry output, there are 8 lines of 4 quaternary digits to be reduced by the Wallace tree.

A. 1-bit multipliers

According to Table IV the transistor count is 54 x 16 = 864 T (MIN) or 76 x 16 = 1216 T (Subblock option).

B. Wallace tree and final add

The 4x4 Wallace tree with a final stage of CPAs is presented in Fig. 8. In this figure, 3 corresponds to a quaternary value, 2 to a ternary value and 1 to a binary value. The first stage reduces 8 lines of 4 digits produced by the 16 1-bit multiplier. Lines of 3 correspond to QP quaternary outputs and lines of 2 correspond to QC ternary outputs of the 1-bit multipliers. Using 3 and 2 (max values of quaternary and ternary digits) has the advantage to indicate the different types of adders that must be used. While binary Wallace trees only use binary FAs and HAs, the situation is more complex for quaternary Wallace trees:

- Q332 adds two quaternary inputs and one ternary input. The ternary input correspond to a QC output of the 1-bit multiplier. As 3+3+2 = 20 (base 4), it means that Q332 generates a quaternary sum and a ternary carry.
- Q331 adds two quaternary inputs and one binary input. 3+3+1 = 13 (base 4). Q331 generates a quaternary sum and a binary carry. It turns out that Q331 is the quaternary 1-digit adder to be used for N-digit quaternary adders.
- Q32 adds one quaternary input and one ternary input. 3+2 = 11 (base 4). Q32 generate a quaternary sum and a binary carry. It is a degraded form of the Q33 quaternary half adder.
- Q31 adds one quaternary input and one binary input to generate a quaternary sum and a binary carry.

As shown in Fig. 8 the Wallace tree with a final CPA has 9 Q33, 13 Q331, 3 Q32 and 2 Q31. There are two options:

- Using the four different types of adders to minimize the transistor count
- Only using Q332 and Q32 adders to minimize the different cells and simplify placement and routing of these cells

Fig. 9 presents the truth table of quaternary adders (sum and carry outputs) when Cin=0/1/2.

As shown in Fig. 8, we use the QFA (Q331) adder presented in Fig. 10 with three power supplies. The half adder is shown in Fig. 11 The Sum part of the full adder corresponds to the higher square of the middle columns. It should be noticed that both input and output binary carries use the 0 and 3 values.

The Q332 adder corresponds to the entire truth table. It is shown in Fig. 12 The sum part is easily derived from Fig. 9.
Now, both input and output carries are ternary. This explains why the Cout computation must generate 0, 1 and 2 levels.

The QH32 half adder is presented in Fig. 15. Cout-QH32 has the binary values 0/3. In the Wallace tree, Cout-QH32 is connected to the Cin input of QH31. It should be noticed that A and B inputs are not symmetric: A is a ternary value controlling the MUX while B is a quaternary value.

The QH31 half adder is presented in Fig. 14 with one quaternary input and one binary input (0/3). Cout is also a 0/3 binary output.

The Q321 adder is similar to Q331 (Fig. 11) except that 0 input in the carry should be replaced by a Vdd input. So, there is no interest to define a specific Q321 adder.

The transistor count for these quaternary adders and half adders is given in Table VII.

The overall transistor count for the 4x4 quaternary digit multiplier is given in Table VIII.

VIII. DISCUSSING RESULTS

The different implementations of 4x4 quaternary multipliers compared with 8x8 bit multipliers lead to the following results:
These results lead to the following conclusions:

- The best implementation of a 4x4 multiplier is obtained by interfacing a 8x8 bit multiplier with quaternary to binary decoder circuits and binary to quaternary encoder circuit.
- The most conservative implementation of a 8x8 bit multiplier (1892 T) has far less transistors than the unrealistic lower bound of the transistor count of the direct implementation of 4x4 digit quaternary multiplier (2888 T): 0.65 ratio.
- As interfacing a binary multiplier with 4-valued interfaces lead to the most efficient implementation, it means that the only gain is to divide by two the number of input and output connections. The overall number of connections is increased: the internal interface connections are added to the binary internal connections.

| TABLE VIII | QUATERNARY MULTIPLIER TRANSISTOR COUNT |
|------------|----------------------------------------|
| Circuits   | Nb | Min | Total  | Nb | Subblock  | Total  |
| Q331       | 13 | 100 | 1300   | 13 | 118       | 1534   |
| Q332       | 9  | 154 | 1386   | 9  | 184       | 1656   |
| QH32       | 3  | 50  | 150    | 3  | 54        | 162    |
| QH31       | 2  | 26  | 52     | 2  | 30        | 60     |
| Total      |    |     | 2888   |    | 3412      |        |

IX. CONCLUDING REMARKS

With the same technique that has been used in the best direct implementation of quaternary adders [7] and the CNTFET circuit styles, we have presented different implementations of a 4x4 digit quaternary multiplier. The best implementation is obtained by using a 8x8 bit multiplier interfaced with quaternary to binary interfaces. It would be the same with any NxN digit multiplier as the issue is with the far greater complexity of 1-digit multipliers and 1-digit adders compared to the complexity of the corresponding binary ones. These results are similar with the results already presented in [4] for N-digit adders. These results contradict the statement on the advantages of multivalued circuits that is quoted in the introduction. With far more transistors, there is no chance that the quaternary multipliers would have less interconnects, less power dissipation, last chip area than the corresponding binary multipliers.

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