Feasibility Evaluation on Elimination of DC Filters for Line-Commutated Converter-Based High-Voltage Direct Current Projects in New Situations

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Abstract: The line-commutated converter (LCC)-based high voltage direct current (HVDC) technology has been widely applied on long-distance and bulk-capacity power transmission occasions. Due to the terrible interferences in the vicinity of communication lines, DC filters (DCFs) are always installed to mitigate the interferences within acceptable levels for almost all in-service overhead line transmission LCC-HVDC schemes. With the rapid development of the communication technology, however, the anti-interference capability of the telephone system has been remarkably improved. Thus, the original purpose of employing DCFs has been virtually absent, and the necessity of the DCFs shall be re-evaluated in sufficient depth not only for new LCC-HVDC projects, but also in the case of refurbishment of older projects. To demonstrate this constructive topic, this paper carries out a commercial ±800 kV/8000 MW LCC-HVDC project as an illustrative example to analyze and discuss those crucial aspects, which may influence the LCC-HVDC stable operation and reliability after removing the DCFs. Then, the paper studies the harmonic voltage/current stresses of the DC equipment, the DC loop low-order harmonic resonances, and the overvoltage under the switching surge and lightning stroke. Finally, it is concluded that the DCF elimination mainly affects the harmonic steady-state stresses of the DC equipment, but has little influence on the transient stresses. For the refurbishment of older projects, the evaluation on the cost between the DCFs' maintenance cost and the equipment modification is needed for the DCFs' elimination. For new LCC-HVDC projects, the DCFs' elimination or at least simplification may be a more economical and attractive alternative, thereby reducing the footprint and cost.

Keywords: line-commutated converter (LCC); high voltage direct current (HVDC); DC filter (DCF); harmonic steady-state stresses; low-order harmonic resonances

1. Introduction

To fulfill the ever-growing energy demand, high-voltage direct current (HVDC) transmission technology has drawn an indispensable role on long-distance and bulk-capacity power transmission occasions, notably the vast territory areas where the energy sources and load demands are distributed unevenly [1–5]. Up to now, over 150 point-to-point line-commutated converter (LCC)-based HVDC projects have been in service worldwide due to its high technology maturity, small operation loss, low investment and maintenance cost [6–8]. Especially in China, nearly 20 LCC-based ultra-HVDC (LCC-UHVDC) projects with operational DC voltage from ±800 kV to ±1100 kV are already commissioned with approximately 1000 km to 3000 km distances [9–12].

Due to the LCC nonlinear switching actions, quantities of harmonic voltages are generated at the converter terminals, causing harmonic currents flowing into the DC lines [13,14]. If the DC lines are placed in the vicinity of communication lines, the harmonic currents will produce terrible interferences in adjacent communication lines through inductive coupling [15–17]. Thus, for almost all in-service overhead line transmission LCC-HVDC schemes, the DC filters (DCFs) are always installed to mitigate the interferences within
acceptable levels [18,19]. As shown in Figure 1, the DCF circuits are usually arranged in parallel between the DC pole busbar and the neutral bus. Contrarily, the back-to-back and the cable transmission LCC-HVDC schemes do not require DCFs [20].

![Figure 1. Structure of the LCC-HVDC system.](image)

Though the performance of the DCFs in mitigating the interferences is highly effective, the equipment cost is high, and the design procedure is time-consuming. The occupational area is generally largest of all DC-side equipment [20]. The high voltage (HV) capacitor is the most cost-intensive element, as it has to require numerous series capacitor units to withstand the entire pole-to-neutral DC voltage [10]. These series units with internal grading resistors form a super slim HV capacitor tower, which is very vulnerable to wind and earthquake [21]. Especially for the voltage levels of 800 kV and above, such tall towers are more difficult to manufacture and maintain, and the corresponding expenditure is inevitably increased. Meanwhile, the DCF design is an iterative procedure of trial and error, converging to a near-optimal solution. In order to fulfill the desirable performance criteria and determine the maximum steady-state stresses of all individual DCF elements, extensive calculations for all possible specified operation conditions must be taken into account [19]. Further, any element in DCFs inevitably suffers some risk of failure, consequently increasing the failure rate and reducing the reliability of the entire LCC-HVDC system.

In the early stage of HVDC development, the interference in nearby communication lines is a serious problem, as the open-wire telephone lines are extensively applied over the world, which are particularly sensitive to harmonic induction [22]. Thus, DCFs are absolutely necessary at that time. Since the 1990s, however, the communication technology has been rapidly developed, and the anti-interference capability of the telephone system has been remarkably improved. The digital communication network with optical fibers as main frame has a particularly high penetration, in which the optical fiber is the insulation medium and can completely eliminate all harmonic induction. Based on a survey [23] in China, the vast majority of the obsolete telephone lines have been superseded, and only part of residual lines may still be disturbed. Compared with installing the costly DCFs, it is a more economical alternative to modify those disturbed telephone lines.

With the state-of-the-art communication technology, the original purpose of employing DCFs to suppress the inductive interference has been virtually absent. Thus, with a potential large cost reduction, the necessity of the DCFs shall be re-evaluated in sufficient depth not only for new LCC-HVDC projects, but also in the case of refurbishment of older projects.

For the DCFs, the existing literatures almost focus on the design, which are old, and may be un-adapted for new situations. To the best of the knowledge of the authors, up till now, only [21] proposed this topic, while no related literature has presented the comprehensive analysis and argument. To demonstrate this constructive question, this paper
carries out a commercial LCC-UHVDC project as an illustrative example. Then, some crucial aspects, which may impact the LCC-UHVDC stable operation and reliability after removing the DCFs, are meticulously analyzed and discussed. The aspects comprise the harmonic steady-state stresses on DC-side apparatus, the low-order harmonic resonances of the entire DC loop, and the overvoltage protection levels of the DC-side surge arresters. The contributions of this paper are summarized as follows:

1. To scientifically demonstrate the feasibility on the elimination of DC filters, a ±800 kV/8000 MW in-service LCC-UHVDC project is taken as a representative example, including the DC loop parameters and surge arresters’ arrangement.
2. In order to comprehensively research the impacts on the harmonic steady-state stresses and the transient stress on DC-side apparatus after removing the DCFs, the mature technologies (i.e., the standard steady-state frequency-domain analysis, and the PSCAD/EMTDC simulation) are adopted.
3. Suggestions are put forward for the DCFs’ configuration or refurbishment of LCC-HVDC project in China, which could be a reference for similar LCC-HVDC projects in the world.

The outline of this paper is organized as follows. Section 2 describes the development of communication technology. Section 3 introduces the HVDC system modeling and the solution for the steady-state DC-side circuit. In Section 4, the DC loop parameters and surge arresters’ arrangement of the project are presented. Section 5 analyzes the steady harmonic stresses. Section 6 calculates the switching and lightning overvoltage. Section 7 dwawns the conclusion.

2. Development of Communication Technology

Since the 1990s, the communication systems have changed beyond recognition. As depicted in Figure 2, through the upgrade from overhead open-wire lines, shielded aerial or buried cables to the optical fibers, the anti-interference capability of the communication lines has been remarkably improved. Among them, the overhead open-wire lines are particularly vulnerable to harmonic induction, whereas the optical fibers are absolutely immune to induced noise [24]. With the optical fibers as main frame, the digital communication network has a particularly high penetration all over the world. Besides, the mobile telephony is now ubiquitous, which is also immune to noise.

![Anti-interference capability](image)

**Figure 2.** Communication lines: (a) Overhead open-wire lines; (b) Shielded aerial/buried cables; (c) Optical fiber.

Since the overhead HVDC lines are mostly constructed in the rural areas and suburbs, specific concerns should be paid to the village communication lines, the railway signal cables and the military cables. According to a survey [23] in China, the fiber to the premises (FTTP) has been implemented in most villages, where the vast majority of the obsolete telephone lines have been superseded, and only a fraction of residual lines may still be disturbed. The railway signal cables are all armored and shielded with alumina sheath, leading to a high degree of immunity from interference. All military cables are paved with optical fibers. Thus, in the case of refurbishment of older projects, especially for
new LCC-HVDC projects, compared with installing the costly DCFs, it may be a more economical and attractive alternative to modify those disturbed lines.

3. HVDC System Modeling

3.1. Subsection

As presented in Figure 1, the DC-side harmonic filtering system includes the DCF, the smoothing reactor (SR) and the neutral bus capacitor (NBC). Among them, the DCF has no other function than to mitigate the interference by shunting several prominent large-amplitude harmonic currents to the station neutral bus or ground through the low-impedance circuits, thus having the possibility of eliminating the DCF.

The DCF circuits are usually installed in parallel between the DC busbar and the station neutral bus or ground. They are specifically designed to mitigate the harmonic currents flowing in the overhead DC transmission line and the electrode line. In practice, the double- or triple-tuned passive filters with a shared HV capacitor are mostly employed due to the technical and economical superiorities, whose algorithm for parameters could be referred to as in [25]. In some projects, the blocking filters series in the neutral bus are also required to mitigate low-order harmonic resonances.

As a key equipment in HVDC projects, besides the harmonic suppression capability, the SR has the following main functions: (1) avoid the intermittent current and attendant overvoltage in the light load range; (2) limit the rise rate of fault current in the event of AC short-circuit faults or DC line faults; (3) protect the converter from lightning strikes on the DC line; (4) suppress the low-order harmonic resonances. For the voltage levels of 800 kV and above, the SR is often split equally in pole bus and station neutral bus, owing to the limitations of insulation and manufacture [11].

The NBC is installed in parallel between the station neutral bus and ground, which is a large capacitor in the range of 10–30 µF. It provides a nearby low-impedance in-station return path for the triple harmonic currents flowing through the stray capacitance, and significantly inhibits these currents flowing into the electrode line. It can also buffer over-voltage caused by a lightning strike on the electrode line.

3.2. Harmonic Voltage Source Model

The three-pulse harmonic voltage source model is widely adopted to analyze the harmonic behavior on the DC side, as it can represent explicitly all triple harmonic voltages and the leakage paths formed by the stray capacitance from converter transformer windings and bushings to ground [14]. As shown in Figure 3, a twelve-pulse bridge comprises two six-pulse bridges with a 30° phase displacement, and is equivalent to four series-connected three-pulse harmonic voltage sources with internal inductances.

![Three-pulse harmonic voltage source model of a twelve-pulse bridge.](image)
In Figure 3, $L$ is one-half of the time-average value of the commutating inductance; $C$ is the stray capacitance to ground in the bridge, and its typical value is $10-20$ nF; $V_{3p}(t)$, $V_{3p}(t - 60^\circ)$, $V_{3p}(t - 30^\circ)$, and $V_{3p}(t - 90^\circ)$ are the equivalent harmonic voltage sources of four three-pulse half bridges, respectively. Considering the effect of various asymmetries in the valve firing angle, the commutation reactor, and the deviation of the winding parameters and AC system imbalances, the piecewise linear analysis approach in [15] is adopted to calculate the three-pulse harmonic voltages.

Obviously, the harmonic voltages vary with the operation conditions. To ascertain the worst-case harmonics and save the computational efforts, the worst non-consistent set is adopted in calculations 19. First, under a specific operating mode (e.g., bipolar, nominal DC voltage, etc.), considering the asymmetries, several harmonic sets for different operating points are calculated. Here, the DC power is increased from minimum (0.1 p.u.) to maximum (1.2 p.u.) at the step of a certain percentage (5% or 10%) of the rated DC power. Then, the worst set of harmonics is formed by selecting the worst individual order harmonic voltage among the multiple harmonic sets in the full power range, namely the worst non-consistent set. Finally, by repeating the above two steps, the worst non-consistent sets of other possible operating modes are obtained. This approach is somewhat pessimistic, since the worst individual harmonic does not occur simultaneously at a certain operating point.

3.3. DC Transmission Line Model

In practical projects, the structures of the overhead DC transmission line and electrode line are shown in Figure 4, respectively. The overhead DC transmission line consists of four coupled wires physically in parallel on the same tower, or three coupled wires for the electrode line. In the majority of line installations, the earth wires are used as shield wires and are solidly earthed at both the sending and receiving ends. As a simplification, the earth wires are not shown in Figure 1.

![Diagram of DC transmission lines](image)

**Figure 4.** Structure of DC transmission lines: (a) Overhead DC line; (b) Electrode line.

In the analysis of the DC-side harmonic behavior, the non-linear influences of the earth and the conductors with respect to frequency are particularly important for long transmission lines. Accounted for the ground resistivity and skin-effect, the distributed parameters of lines are calculated by using Carson’s equations [26], which are expressed with the frequency-dependent series impedance matrices $Z$ and shunt admittance matrices $Y$ per unit length. The parameters necessary for distributed-parameter calculation comprise all wires’ data (i.e., type, size, geometry, resistivity), tower and span geometry, sag, and ground resistivity.
When solving the DC-side circuit, the coupled multi-phase transmission line is regarded as a multi-node element. Based on the phase-mode transformation, the nodal admittance matrix of the line \( Y_l \) is expressed as [27]:

\[
\begin{bmatrix}
I_s \\
I_R
\end{bmatrix} = Y_l \begin{bmatrix}
U_S \\
U_R
\end{bmatrix} = \begin{bmatrix}
Y_s & -Y_m \\
-Y_m & Y_s
\end{bmatrix} \begin{bmatrix}
U_S \\
U_R
\end{bmatrix}
\]

(1)

where, \( U_S, U_R, I_S, \) and \( I_R \) are the voltage and current vectors at the sending end and the receiving end of lines, respectively; \( Y_s \) and \( Y_m \) are the self- and mutual-admittance matrices; \( \Gamma \) is the propagation matrix; \( \Lambda \) is the eigenvalues matrix of \((ZY)\), and \( T_u \) is the transformation matrix composed of eigenvectors corresponding to \( \Lambda_l \); \( l \) is the length of the transmission line.

### 3.4. Solution for the DC-Side Circuit

The equivalent DC-side model for harmonic behavior analysis is formed as in Figure 5. The model is a linear but frequency-dependent circuit, which synthesizes the three-pulse harmonic voltage sources, the DC-side harmonic filtering system, the overhead DC transmission line, the electrode lines and the ground electrode resistances.

![Figure 5. Equivalent DC-side harmonic analysis model.](image)

Based on the standard steady-state frequency-domain analysis technique, the DC-side circuit can be solved with the nodal voltage analysis method, namely, \( I = Y_{dc}U \). Here, \( I \) is the injection current vector; \( U \) is the nodal voltage vector; \( Y_{dc} \) is the nodal admittance matrix of the entire DC-side circuit.

The solution for the DC-side circuit mainly includes five steps, as follows:

1. **Step (1).** Calculate the worst non-consistent sets of three-pulse harmonic voltage sources with the piecewise linear analysis approach derived in [15].
2. **Step (2).** Form the nodal admittance matrix \( Y_{dc}(n) \) at \( n \)-th order harmonic. First, calculate the nodal admittance matrix of lines \( Y_l(n) \) in (1), including the DC transmission line and the electrode lines. Then, insert the \( Y_l(n) \) into \( Y_{dc}(n) \) as multi-node
elements. Finally, \( Y_{dc}(n) \) is constructed by adding other elements in Figure 5 one by one.

Step (3). Solve the entire DC circuit. First, suppose that the three-pulse sources at the rectifier act alone and the sources at the inverter are set to zero, the injection current vector \( \mathbf{I}(n, 1) \) is calculated with the Norton equivalent. Second, the nodal voltage vector \( \mathbf{U}(n, 1) \) is obtained with the nodal voltage analysis method. Then, repeat the similar process, the voltage vector \( \mathbf{U}(n, 2) \) excited solely by the three-pulse sources at the inverter is acquired. Finally, the harmonic voltages \( U_e(n, i) \) that the elements bear and the harmonic currents \( I_e(n, i) \) flowing in elements are calculated. Here, \( i \) is 1 or 2, which denotes the rectifier or the inverter.

Step (4). Calculate the steady-state stresses of elements. Synthesized with all individual harmonics, the steady state stresses of the capacitors are expressed as in:

\[
\begin{align*}
\mathbf{U}_C &= \sum_{i=1}^{n=N} \sum_{n=1}^{i=2} U_e(n, i) \\
\mathbf{I}_C &= \sum_{i=1}^{n=N} \sum_{n=1}^{i=2} I_e(n, i)
\end{align*}
\]  
(2)

where \( N \) is the maximum harmonic order. The voltage stress expression of the reactors \( U_L \) are the same as that of the capacitor, while the current stress of the reactors are calculated by the root sum of squares (RSS) method as:

\[
I_L = \sqrt{\sum_{i=1}^{i=2} \sum_{n=1}^{n=N} I_e^2(n, i)}
\]  
(3)

Step (5). Calculate the DC-loop impedance. Firstly, insert two identical test voltage sources at point A in Figure 5, whose schematics are shown in Figure 6. Here, \( \mathbf{U}_A(f) \) is the voltage phasor of the inserted voltage source at the specified frequency \( f \), \( R_{in} \) is the internal resistance; \( \mathbf{I}_A(f) \) is the current phasor flowing through point A; \( \mathbf{U}_a(f) \) and \( \mathbf{U}_b(f) \) are the voltage phasors at point \( a \) and point \( b \), respectively.

\[ \mathbf{U}_a(f) \quad \mathbf{U}_a(f) \quad \mathbf{R}_{in} \quad \mathbf{U}_b(f) \quad \mathbf{U}_b(f) \]

\[ a \quad R_{in} \quad b \]

Figure 6. Schematic of the test voltage source.

Then, with the passive part in Figure 5 and the inserted test voltage sources, \( \mathbf{U}_a(f) \) and \( \mathbf{U}_b(f) \) are calculated by using the method similar to Step (2) and Step (3). Finally, the DC-loop impedance from the rectifier side \( Z_{dc,R}(f) \) is derived as:

\[
Z_{dc,R}(f) = \frac{\mathbf{U}_A(f)}{\mathbf{I}_A(f)} = \frac{\mathbf{U}_A(f) \cdot R_{in}}{\mathbf{U}_b(f) - \mathbf{U}_a(f) + \mathbf{U}_A(f)}
\]  
(4)

4. Parameters of the Test System

In this paper, a ±800 kV/8000 MW LCC-UHVDC project is taken as an illustrative example. As shown in Figure 1, each pole consists of two 12-pulse converters connected in series, i.e., a HV converter, and a low-voltage (LV) converter. The main parameters of the converter stations are listed in Table 1.
Table 1. Parameters of converter stations.

| Items                                                      | Values                          |
|------------------------------------------------------------|---------------------------------|
| Nominal DC power (bipolar), \( P_{\text{dcN}, \text{MW}} \) | Rectifier 8000 Inverter 800     |
| Nominal DC voltage, \( U_{\text{dcN}, \text{kV}} \)        | 800                             |
| Nominal DC current, \( I_{\text{dcN}, \text{kA}} \)        | 5                               |
| Nominal AC system frequency, \( f, \text{Hz} \)            | 50                              |
| Nominal AC system voltage, \( U_{\text{ac}, \text{kV}} \)  | 530 510                         |
| Nominal ideal no-load DC voltage, \( U_{\text{di0N}, \text{kV}} \) | 231.45 218.54                   |
| Firing angle, \( \alpha, ^\circ \)                        | 15 ± 2.5                        |
| Extinction angle, \( \gamma, ^\circ \)                     | 17 ± 1                          |

Converter transformer

| Items                                                      | Values                          |
|------------------------------------------------------------|---------------------------------|
| Winding voltages (L-L), kV/kV                              | Rectifier 530/171.4 Inverter 510/161.83 |
| 3-phase capacity, MVA                                       | 1212 1146                       |
| Commutation reactance, \%                                   | 19.5 19                         |
| Tap changer, \%                                            | 1.25 (+23/-5)                   |

Three-pulse model

| Items                                                      | Values                          |
|------------------------------------------------------------|---------------------------------|
| Internal inductance, \( L, \text{mH} \)                    | Rectifier 14.16 Inverter 13.34  |
| Stray capacitance, \( C, \text{nF} \)                      | 18.15 (HV) 24.36 (LV)           |

Earth electrode resistance, \( R_{\text{G1}} / R_{\text{G2}}, \Omega \)

| Values | Rectifier 0.25 Inverter 0.25 |

4.1. Subsection

The operating modes include bipolar or monopolar, and full or reduced (70%) DC voltage operation. The asymmetries are as follows: (1) the negative-sequence AC voltage of the 1.1% fundamental positive sequence is used, where the phase angle is assumed to be uniformly and randomly distributed between \( 0^\circ \) and \( 360^\circ \); (2) the imbalances in firing angle between the valves in a 12-pulse converter are assumed to have a standard deviation of \( 0.0184^\circ \); (3) the phase reactance deviations from the mean values are assumed to be normally distributed with a standard deviation of 0.7%; (4) other factors are also considered, such as background harmonic voltages [21]. For the limited space, only the worst non-consistent set of bipolar and full DC voltage operation are listed in Table 2. Here, the maximum harmonic order \( N \) is 50, and the harmonic voltages of LV converter are equal to those of the HV converter.

Table 2. Three-pulse voltages of bipolar and full DC voltage operation.

| 3-pulse voltages at positive pole, kV                        |
|--------------------------------------------------------------|
| Order | Station   | YYP1   | YYN1+YDP1 | YDN1   |
|-------|-----------|--------|-----------|--------|
| 2nd   | Rectifier | 1.76<0° | 3.52<0°   | 1.76<0° |
|       | Inverter  | 1.52<0° | 3.03<0°   | 1.52<0° |
| 12th  | Rectifier | 3.98<−24.06 | 7.95<−24.06 | 3.98<−24.06 |
|       | Inverter  | 3.65<−38.80 | 7.31<−38.80 | 3.65<−38.80 |
| 24th  | Rectifier | 2.64<142.63 | 5.28<142.63 | 2.64<142.63 |
|       | Inverter  | 2.48<125.68 | 4.95<125.68 | 2.48<125.68 |

| 3-pulse voltages at negative pole, kV                        |
|--------------------------------------------------------------|
| Order | Station   | YYN2   | YYP2+YDN2 | YDP2   |
|-------|-----------|--------|-----------|--------|
| 2nd   | Rectifier | 1.76<10° | 3.52<10°   | 1.76<10° |
|       | Inverter  | 1.52<10° | 3.03<10°   | 1.52<10° |
| 12th  | Rectifier | 3.09<−69.12 | 6.19<−69.12 | 3.09<−69.12 |
|       | Inverter  | 4.02<−17.51 | 8.04<−17.51 | 4.02<−17.51 |
| 24th  | Rectifier | 2.31<70.89 | 4.63<70.89   | 2.31<70.89 |
|       | Inverter  | 2.62<161.67 | 5.25<161.67 | 2.62<161.67 |

4.2. DC-Side Harmonic Filtering System

Two identical SRs with nominal reactance of 75 mH are installed on both DC 800 kV pole busbar and neutral bus at each pole in each station, namely 150 mH. The NBCs at the rectifier and inverter are 17 µF and 15 µF, respectively. The DCFs’ configuration are
identical for each pole in each station. The schematics and parameters of two double-tuned DCFs are shown in Figure 7, respectively. In order to avoid the fundamental frequency resonance, the blocking filters are placed in series at the neutral bus in both poles of the rectifier.

![Figure 7. Schematics and parameters of the DCFs: (a) High Pass (HP) 12/24; (b) HP 2/39.]

4.3. DC Transmission Lines

Table 3 elaborates the parameters of the overhead DC lines and the electrode lines. Here, to approximate the varying earth resistivity, the overhead DC lines are split into two sections.

| Items                  | Overhead DC Line | Electrode Line |
|------------------------|------------------|----------------|
|                        | Section I | Section II | Rectifier | Inverter |
| Length, km             | 1140      | 539.9      | 103       | 23.6      |
| Earth resistivity, Ω*m | 180       | 300        | 180       | 300       |
| Height, m              | 42.2       | 42.2       | 22        | 24        |
| Horizontal spacing, m  | 20         | 20         | 6.6       | 6         |
| Sag, m                 | 21.2       | 21.2       | 11.5      | 15.52     |
| Sub-conductor number   | 6          | 6          | 2         | 2         |
| Sub-conductors spacing, m | 0.45     | 0.45       | 0.5       | 0.4       |
| Outer radius, m        | 0.0203     | 0.01995    | 0.015     | 0.015     |
| Total strands number   | 84         | 72         | 48        | 48        |
| Strand radius, m       | 0.001845   | 0.001995   | 0.0018    | 0.0018    |
| Resistivity, Ω*m       | 2.84 × 10⁻⁸ | 2.84 × 10⁻⁸ | 2.84 × 10⁻⁸ | 2.84 × 10⁻⁸ |

4.4. Surge Arrester Scheme

The surge arrester configuration of the studied project is illustrated as in Figure 8. Here, the specific description of each arrester could be referred to as in [28], and will not be repeated here in full depth.
Shield wire data

| Horizontal spacing, m | 16 | 16 |
|----------------------|----|----|
| Sag, m               | 13 | 13 |
| Outer radius, m      | 0.007875 | 0.007875 |
| Total strands number | 19 | 19 |
| Strand radius, m     | 0.00175 | 0.00175 |
| Resistivity, Ω·m     | 2.0 × 10⁻⁷ | 2.0 × 10⁻⁷ |

4.4. Surge Arrester Scheme

The surge arrester configuration of the studied project is illustrated as in Figure 8. Here, the specific description of each arrester could be referred to as in [28], and will not be repeated here in full depth.

Figure 8. Arrester scheme of the studied project.

On the basis of the arrangement principles of arresters and arrester stresses for different events, the stresses of the arresters (i.e., DB1/DB2, DR, and E) are most likely to be affected after removing the DCFs. Table 4 shows the basic parameters and protection levels for the relative arresters [29].

Table 4. Parameters and protection levels for arresters.

| Arrester | CCOV, kV | U_ref, kV | LIPL, kV/kA | SIPL, kV/kA | Columns | Energy Capability, MJ |
|----------|----------|----------|-------------|-------------|---------|-----------------------|
| DB1      | 824      | 969      | 1625/20     | 1391/1      | 3       | 14                    |
| DB2      | 824      | 969      | 1625/20     | 1391/1      | 3       | 14                    |
| DR       | 44       | 483 rms  | 900/05      | /           | 1       | 3.4                   |
| E        | 95       | 304      | 478/5       | /           | 2       | 3                     |

Note: CCOV: Crest value of continuous operating voltage; LIPL/SIPL: Lightning/switching impulse protective level.

5. Study on Steady Stress

Based on the calculation procedure described in Section 3.4, the steady harmonic stresses for the DC-side circuit are solved. For the steady harmonic stress without the DCFs, some equipment which may be impacted are researched, including the NBC, the SR at the DC pole bus, the voltage at the DC line inlet, and DC-side low-frequency impedance. Three operation modes are considered as follows: (1) bipolar and full DC voltage (BIF); (2) monopolar with earth return and full DC voltage (MGF); (3) monopolar with earth return and reduced DC voltage (MGR).

5.1. NBC

As listed in Table 5, the harmonic voltage stresses for the NBC are increased by only about 1.0 kV after removing the DCFs. Under normal operation, the NBC withstands the tiny DC voltage. Thus, after removing the DCFs, the upgrading and reconstruction for the NBC is hardly necessary.
Table 5. Harmonic voltage stress for the NBC.

| Operation mode      | BIF       | MGF       | MGR       |
|---------------------|-----------|-----------|-----------|
|                     | DCF  | no DCF  | DCF  | no DCF  | DCF  | no DCF  | DCF  | no DCF  |
| Voltage SUM, kV     | 2.26 | 2.68    | 11.47 | 12.23   | 10.00 | 11.17   |
| Major harmonic      | 3/0.67 | 2/1.07 | 2/7.84 | 2/2.94 | 2/8.43 | 2/8.60 |
| (order/voltage), kV | 2/0.61 | 3/0.76 | 3/2.07 | 3/2.03 | 1/0.25 | 12/0.91 |
|                     | 6/0.40 | 6/0.32 | 6/0.83 | 6/1.01 | 3/0.22 | 4/0.29 |
|                     | 12/0.12 | 4/0.13 | 4/0.10 | 12/0.47 | 4/0.19 | 1/0.27 |

Neutral bus at positive pole in inverter

| Operation mode      | BIF       | MGF       | MGR       |
|---------------------|-----------|-----------|-----------|
|                     | DCF  | no DCF  | DCF  | no DCF  | DCF  | no DCF  |
| Voltage SUM, kV     | 2.99 | 3.23    | 4.34  | 5.52    | 2.63  | 3.70    |
| Major harmonic      | 3/1.39 | 3/1.55 | 6/2.13 | 6/2.80  | 2/0.83 | 12/1.12 |
| (order/voltage), kV | 6/0.63 | 6/0.51 | 2/0.78 | 2/0.79  | 6/0.34 | 2/0.84 |
|                     | 2/0.31 | 2/0.41 | 3/0.42 | 12/0.62 | 4/0.30 | 4/0.42 |
|                     | 4/0.20 | 4/0.35 | 39/0.28 | 3/0.44  | 39/0.26 | 6/0.39 |

5.2. SR

Before and after eliminating the DCFs, the harmonic current stresses for the SR are presented in Table 6. This is an interesting result, that is, the harmonic current stresses for the SR are unexpectedly diminished. The reason is that the DCF branches supply a nearby low-impedance circuit for specific tuning harmonic currents (i.e., 2nd, 12th, 24th, etc.) to flow into the neutral bus instead of the pole bus. The DCF branch shunt a majority of those harmonic currents, while the currents at the line side of the DCFs are decreased. In other words, compared to the DC circuit without the DCFs, the DC loop impedance with the DCFs is relatively smaller at the specific tuning frequencies, thus resulting in larger currents.

Table 6. Harmonic current stress for the SR.

| Operation mode      | BIF       | MGF       | MGR       |
|---------------------|-----------|-----------|-----------|
|                     | DCF  | no DCF  | DCF  | no DCF  | DCF  | no DCF  |
| Current RSS, A      | 36.23 | 25.78   | 37.72  | 25.77   | 65.55 | 46.61   |
| Major harmonic      | 12/29.41 | 12/19.40 | 12/30.31 | 12/21.73 | 12/59.05 | 12/42.87 |
| (order/current), A  | 6/11.79 | 6/9.17   | 2/18.27 | 24/6.14  | 2/19.52 | 24/12.98 |
|                     | 39/7.12 | 24/5.97  | 39/7.43 | 2/6.00   | 24/15.16 | 2/6.73   |
|                     | 24/6.33 | 39/4.13  | 24/7.14 | 3/5.23   | 39/9.83  | 39/5.46  |

Pole bus at positive pole in inverter

| Operation mode      | BIF       | MGF       | MGR       |
|---------------------|-----------|-----------|-----------|
|                     | DCF  | no DCF  | DCF  | no DCF  | DCF  | no DCF  |
| Current RSS, A      | 41.12 | 26.86   | 46.10  | 28.37   | 65.38 | 43.55   |
| Major harmonic      | 12/28.01 | 12/17.82 | 12/29.17 | 12/20.60 | 12/53.17 | 12/36.94 |
| (order/current), A  | 6/18.93 | 6/11.50  | 39/24.31 | 2/15.60  | 2/25.03  | 2/16.22  |
|                     | 39/14.22 | 2/6.23   | 2/23.69 | 24/5.65  | 39/22.35 | 24/12.63 |
|                     | 2/8.95  | 24/5.56  | 24/6.64 | 39/5.01  | 24/14.80 | 39/5.46  |

Thereby, the DCFs’ removal has barely an effect on the SR, whereas the currents flowing in the DC switching devices and DC current transformer (CTs) at the line side of the DCFs are adversely enlarged, resulting in increase of losses.
5.3. Voltage at the DC Line Inlet

Before and after canceling the DCFs, the harmonic voltage stresses at both ends of the positive pole DC line are exhibited as in Table 7. Without the DCFs, the harmonic voltage stresses at both ends of the DC line are evidently magnified, mainly dominated by the 2nd and 12th harmonics. It may accelerate the insulation aging, and shorten lifetime for the equipment near both ends of the pole DC line. At the same, the operating voltage for the arresters of DB1/DB2 are also enlarged.

Table 7. Harmonic voltage stress at pole line inlet.

| Operation mode | Pole line inlet at positive pole in rectifier | Pole line inlet at positive pole in inverter |
|----------------|---------------------------------------------|---------------------------------------------|
| Voltage RSS, kV | BIF DCF no DCF MGF DCF no DCF MGR DCF no DCF | BIF DCF no DCF MGF DCF no DCF MGR DCF no DCF |
| Major harmonic (order/voltage), kV | Voltage RSS, kV | Voltage RSS, kV |
| Voltage RSS, kV | 18.01 2/12.73 6/18.9 2/15.12 2/14.88 2/16.00 12/18.24 | 17.17 2/12.47 6/19.26 2/14.48 2/14.78 2/15.60 12/15.93 |
| Major harmonic (order/voltage), kV | 6/9.79 2/11.83 6/6.73 12/9.56 14/2.31 2/15.71 | 500 3/5.47 12/10.49 3/4.19 6/7.87 12/1.70 48/4.64 |
| Voltage RSS, kV | 3/5.37 3/4.63 14/2.32 3/3.83 1/1.08 24/3.90 | 1000 2/12.73 6/18.9 2/15.12 2/14.88 2/15.60 12/17.63 |
| Major harmonic (order/voltage), kV | 6/9.61 2/11.61 6/6.78 12/9.44 14/2.19 2/15.93 | 500 14/5.54 12/5.96 3/3.08 6/8.24 12/1.53 48/4.74 |
| Voltage RSS, kV | 3/2.99 48/3.91 14/2.23 30/2.97 4/1.06 24/2.86 | 1500 14/2.99 48/3.91 14/2.23 30/2.97 4/1.06 24/2.86 |

5.4. DC Loop Impedance

Due to the very large inductances and capacitances of both the LCC converters and the DC lines, resonances at the lower frequencies (generally fundamental and 2nd harmonics) are almost inevitable [21]. When the DC system resonance occurs, excessive harmonic currents and voltages may be generated, and can even damage the converter, the SR and other equipment.

Insert two identical 1.0 kV test voltage sources at point A in Figure 5, and then the DC loop impedances for bipolar mode are calculated and drawn in Figure 9. Here, the frequency f is ranged from 1 Hz to 200 Hz at the step of 1 Hz. It is observed that due to the blocking filter, the DC impedances at 50 Hz are amplified to about 500 Ω whether the DCFs are present or not. Without the DCFs, the DC impedance is reduced from 561.52 Ω to 287.55 Ω at 100 Hz. Hence, the DC system suffers the risk of the 2nd resonance.
5.5. Summary

Based on the research, in this Section, it is concluded that it has little effect on the NBC and SR after canceling DCFs. The voltage and current stresses are undesirably elevated for the DC-side apparatus at the line side of the DCFs, such as the DC line switch, CTs, and pole arresters (DB1/DB2). The elevated stresses will imply a higher operation loss, equipment voltage rating, insulation, and consequently, the increased expenditure for those affected devices. Since the existing LCC-UHVDC projects usually install the series fundamental blocking filters, no resonance will occur near 50 Hz, and the concern on resonance has shifted to 2nd harmonic resonance.

In the case of refurbishment of older projects, the evaluation on the cost between the DCFs’ maintenance cost and the equipment modification is needed for the question of whether DC filters are required. If the equipment modification cost is lower, the DCF removal is technically feasible, and vice versa. For new LCC-HVDC projects, the enhancement on voltage rating and insulation may be a more economical and attractive alternative than installing the extensive DCFs, thereby reducing the footprint and cost. At least, the DCF branch could be simplified to a 2/12 double-tuned DCF, where the 2nd tuning frequency is applied for the resonance suppression, and 12th for mitigating the prominent harmonic.

6. Study on Transient Stress

In this Section, the LCC-UHVDC electromagnetic transient model is benchmarked on the PSCAD/EMTDC to study the protection performance for the surge arresters listed in Table 4. The arrester configuration in Figure 8 is also accurately built.

6.1. Switching Overvoltage

The surge arrester is modeled with a non-linear resistance, and the Frequency Dependent (Phase) Line Model is employed. Other equipment uses PSCAD model, such as LCC converter and converter transformer. The events for the switching overvoltage study are listed in Table 8 [28].

Table 8. Events for switching overvoltage.

| Event | Arrester DB1 | Arrester DB2 | Arrester DR | Arrester E |
|-------|--------------|--------------|-------------|------------|
| 1 DC pole line to earth fault | ✓ | ✓ | ✓ | ✓ |
| 2 AC phase to earth fault at valve side | ✓ | ✓ | ✓ | ✓ |
| 3 AC earth fault at grid side | ✓ | ✓ | ✓ | ✓ |

The events are applied respectively, and the corresponding residual voltages of arresters are recorded as in Table 9. According to the simulation results, the residual voltages are always below the SIPL of the arresters, regardless of whether the DCFs are absent or not.

Table 9. Residual voltages of arresters for switching surge.

| Arrester | Residual Voltage, kV | Event 1 | Event 2 | Event 3 |
|----------|----------------------|---------|---------|---------|
| DB1      |                      | DCF     | No DCF  | DCF     | No DCF  |
| DB2      |                      | 1083.07 | 1060.87 | 1085.44 | 941.23  | 922.67  |
| DR       |                      | 160.36  | 220.70  | 250.74  | 177.75  | 179.15  |
| E        |                      | 240.59  | 255.67  | 252.67  | 237.20  | 262.77  |
6.2. Lightning Overvoltage

All DC-side equipment is modeled with high-frequency model, including the LCC converter, the converter transformer, SR, surge arresters, and so on. As pictured in Figure 10, the tower is modeled with multi-segment multi-surge impedance model, and the Frequency Dependent (Phase) Line Model is adopted to connect the two sides of the tower [30]. The lightning current is simulated by double-exponential model. Both the counterstrike and the shielding failure are calculated with monopolar with earth return. The lightning current of the former is 260 kA with 300 Ω, and 24.46 kA/800 Ω for the latter.

Both the counterstrike and shielding failure are implemented, and the corresponding residual voltages of arresters are recorded as in Table 10. Before and after eliminating the DCFs, the residual voltages of lightning strikes are always lower than the LIPL of the arresters. It is noted that the residual voltage of the arrester E decreases drastically after canceling the DCFs, and the reason is that the lightning current path through the DCFs’ circuit to the neutral bus is obstructed after removing the DCFs.

Table 10. Residual voltages of arresters for lightning stroke.

| Arrester | Counterstrike | Shielding Failure |
|----------|---------------|-------------------|
| DCF      | No DCF        | DCF               | No DCF          |
| DB1      | 1253.44       | 1352.45           | 1566.09         | 1606.22         |
| DB2      | 1247.69       | 1346.15           | 1514.99         | 1564.84         |
| DR       | 215.75        | 304.35            | 287.13          | 307.27          |
| E        | 350.83        | 9.26              | 398.56          | 7.2             |

6.3. Summary

Based on the overvoltage calculations, in this Section, it is concluded that the residual voltages are always below the protection levels of the arresters under both the switching surge and lightning stroke, regardless of whether the DCFs are absent or not. Thereby, under the consideration of DCFs’ elimination, little concern needs to be taken into the overvoltage and insulation co-ordination studies.
7. Conclusions

This paper first meticulously researches and evaluates the question on elimination of DC filters for LCC-HVDC projects in new situations. To demonstrate this constructive question, this paper carries out a commercial ±800 kV/8000 MW LCC-UHVDC project as an illustrative example. Then, based on the standard steady-state frequency-domain analysis and the PSCAD/EMTDC simulations, some crucial aspects, which may impact the LCC-UHVDC stable operation and reliability after removing the DCFs, are analyzed and discussed.

According to the studies, the conclusions are drawn as follows:

1. The DCF elimination mainly affects the harmonic steady-state stresses of the DC equipment, but has little influence on the transient stresses.
2. In the case of refurbishment of older projects, if the equipment modification cost is lower, the DCF removal is technically feasible, and vice versa.
3. For new LCC-HVDC projects, the enhancement on voltage rating and insulation of DC equipment may be a more economical and attractive alternative than installing the extensive DCFs, thereby reducing the footprint and cost. At least, the DCF branch could be simplified to a 2/12 double-tuned DCF.

In further research, harmonic interaction between connected AC systems will be emphasized and studied.

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