Abstract—Relaxing the sequential specification of shared objects has been proposed as a promising approach to obtain implementations with better complexity. In this paper, we study the step complexity of relaxed variants of two common shared objects: max registers and counters. In particular, we consider the \(k\)-multiplicative-accurate max register and the \(k\)-multiplicative-accurate counter, where read operations are allowed to err by a multiplicative factor of \(k\) (for some \(k \in \mathbb{N}\)). More accurately, reads are allowed to return an approximate value \(x\) of the maximum value \(v\) previously written to the max register, or of the number \(v\) of increments previously applied to the counter, respectively, such that \(v/k \leq x \leq v \cdot k\). We provide upper and lower bounds on the complexity of implementing these objects in a wait-free manner in the shared memory model.

Index Terms—Distributed computing, distributed algorithms, shared memory, fault tolerance, concurrent data structures, relaxed specifications

I. INTRODUCTION

With the ubiquitousness of multi-core and multi-processor systems, there is a growing need to gain better understanding of how to implement concurrent objects with improved complexity, while maintaining the natural correctness guarantees provided to programmers by linearizability. Relaxing the sequential specification of linearizable concurrent objects is one promising approach of achieving this \([1], [2]\). An object’s sequential specification defines its correct behavior in sequential executions. Roughly speaking, linearizability\([3]\) guarantees that any concurrent execution is equivalent to a sequential one.

There is empirical evidence that relaxing the sequential specification of some common objects, e.g. queues and counters, yields improved performance of linearizable implementations, e.g.\([2], [4]\). However, the theoretical principles to implement concurrent objects more efficiently by relaxing their sequential specification are not yet clear.

In this paper, we study relaxed-semantics variants of two well-known concurrent objects – counters and max registers, in the classical shared memory model. In particular, we investigate the extent to which allowing wait-free linearizable implementations of these objects to return approximate values, rather than accurate ones, may improve their step complexity.

A counter is a linearizable object that supports a \texttt{CounterIncrement} operation and a \texttt{CounterRead} operation. The sequential specification of a counter requires that a \texttt{CounterRead} operation returns the number of \texttt{CounterIncrement} operations that precede it. A relaxed variant of the counter is the \(k\)-multiplicative-accurate counter, defined in \([5]\), where a \texttt{CounterRead} operation returns an approximate value \(x\) of the number \(v\) of \texttt{CounterIncrement} operations that precede it, such that \(v/k \leq x \leq v \cdot k\) for some parameter \(k > 0\).

A max register \(r\) supports a \texttt{Write}(\(v\)) operation that writes a non-negative integer \(v\) to \(r\) and a \texttt{Read} operation that returns the maximum value previously written to \(r\). \([5]\). We define the \(k\)-multiplicative-accurate max register by allowing a \texttt{Read} operation to return an approximate value \(x\) of the largest value \(v\) written before it, such that \(v/k \leq x \leq v \cdot k\) for some parameter \(k > 0\).

A. Related Work

A well-known result by Jayanti, Tan and Toueg\([6]\) proved a linear lower bound in the number of processes \(n\) on the worst-case step complexity of obstruction-free implementations from historyless primitives (e.g. read,write, test&set) of a large class of shared objects that includes exact counters. A wait-free exact counter with optimal worst case step complexity can be constructed easily by using a wait-free atomic snapshot: to increment the counter, a process simply increments its component of the snapshot, and to read the counter’s value, it invokes \texttt{Scan} and returns the sum of all components in the view it obtains. Since wait-free atomic snapshot can be implemented, using reads and writes only, with worst-case step complexity linear in \(n\), e.g.\([7]\), so can counters.

Aspnes, Attiya and Censor-Hillel\([8]\) show the possibility of implementing exact counting algorithms whose step complexity is sub-linear when the number of operations is bounded. In particular, they presented a wait-free exact counter for which the step complexities of \texttt{CounterIncrement} and \texttt{CounterRead} operations are \(O(\min(\log n, \log v, \log n))\) and \(O(\min(\log v, n))\), respectively, where \(v\) is the object’s current value. However, for executions in which the number of \texttt{CounterIncrement} operations is exponential in \(n\), both the worst-case and the amortized step complexities of their construction become linear in \(n\).

In\([9]\) Baig et al. present the first wait-free read/write exact counter whose amortized step complexity is polylogarithmic in \(n\), \(O(\log^2 n)\), in executions of arbitrary length and prove
that their algorithm is optimal in terms of amortized step complexity up to a logarithmic factor.

Approximate counting has many applications (e.g., [10], [11]) and there is a large literature in approximate probabilistic counting, both in the sequential (e.g., [12], [13]) and concurrent setting (e.g., [14], [15]). In [14], Aspnes and Censor present a randomized algorithm to implement an approximate counter that requires sublinear step complexity, and where any CounterRead operation has a high probability of returning a value which is at most a fraction of δ less than the number of increments that have finished before the read started, and at most a fraction of δ more than the number of increments that have started before the read finished. Similarly to their counter, the k-multiplicative accurate counter we study in this paper, allows a multiplicative error of the exact value. However, we study approximate deterministic counting, where the value returned by CounterRead operations is always ensured to be within the given approximation range.

Aspnes et al. also study k-additive counters that allow some additive error for the value returned by CounterRead operations, [8]. In particular they prove a lower bound of \( \Omega(n - 1, \log m - \log k) \) on the worst-case step complexity of any deterministic asynchronous linearizable implementation of a k-additive counter, where \( m \) is the number of states of the counter and \( n \) is the number of processes. No matching upper bound is given.

The exact max register object has been proposed in [8] where Aspnes et al. present a bounded variant of this object to beat the linear lower bound on the worst case step complexity by Jayanti et al. In particular, their algorithm has \( O(\log m) \) worst case step complexity for both Read() and Write(v) operations provided that the value written in the max register does not exceed the value \( m \). Their algorithm is optimal [5]. Baig et al. [9] presented an unbounded deterministic max register implementation with polylogarithmic amortized step complexity in executions of arbitrary length.

### B. Our Contribution

**k-multiplicative-accurate counter:** To the best of our knowledge we present the first deterministic approximate counter with constant amortized complexity. More precisely, we present a wait-free linearizable k-multiplicative-accurate counter for \( k \geq \sqrt{n} \) where \( n \) is the number of processes, with constant amortized step complexity for executions of arbitrary length. Then, by extension of the lower bound of Attiya and Hendler, [10], we prove that any \( n \)-process solo-terminating implementation of a k-multiplicative-accurate counter from read/write and conditional primitive operations (including k-word compare-and-swap) has amortized step complexity of \( \Omega(\log(n/k^2)) \), for \( k \leq \sqrt{n}/2 \). Our results together with the upper and lower bound on exact counting proved in [9] show that when the approximation parameter \( k \) does not depend on \( n \), relaxing the counter semantics by allowing a multiplicative error cannot asymptotically reduce the amortized step complexity by more than a logarithmic factor.

We also prove that the worst-case step complexity of obstruction-free implementations of m-bounded k-multiplicative-accurate counters from historyless primitives is \( \Omega(\min(n, \log_2 \log_k m)) \), where \( n \) is the number of processes and \( m \) is a bound on the number of CounterIncrement operation instances that can be performed on the counter. This implies that for unbounded k-multiplicative-accurate counters, the worst case step complexity is in \( \Omega(n) \), and we fall back to the linear lower bound by Jayanti, Tan and Toueg [6].

**k-multiplicative-accurate max register:** We prove that relaxing the semantics of the bounded max register by allowing inaccuracy of even a constant multiplicative factor yields an exponential improvement in the worst-case step complexity. In particular, we prove that the worst-case step complexity of obstruction-free read/write implementations of m-bounded k-multiplicative-accurate max registers is \( \Omega(\min(n, \log_2 \log_k m)) \), where \( n \) is the number of processes. A max register is m-bounded, if it can only represent values in \( \{0, \ldots, m - 1\} \). Then, we present a novel m-bounded k-multiplicative-accurate max register algorithm whose worst-case step complexity matches this lower bound. We can easily “plug-in” our bounded k-multiplicative-accurate max register into the construction proposed by Baig et al. [9] to obtain an unbounded k-multiplicative-accurate max register with sub-logarithmic amortized step complexity (omitted due to space constraints).

### II. Model and Preliminaries

We consider an asynchronous shared memory system, where a set \( \mathcal{P} \) of \( n \) crash-prone processes communicate by applying operations to shared objects. An object is an instance of an abstract data type. It is characterized by a domain of possible values and by a set of operations that provide the only means to manipulate it. An implementation of a shared object provides a specific data-representation for the object from a set of shared base objects, each of which is assigned an initial value; the implementation also provides algorithms for each process in \( \mathcal{P} \) to apply each operation to the object being implemented. To avoid confusion, we call operations on the base objects primitives and reserve the term operations for the objects being implemented.

An execution fragment is a (finite or infinite) sequence of steps performed by processes as they follow their algorithms. In each step, a process applies at most a single primitive to a base object (possibly in addition to some local computation). We consider read, write and test&set primitives. An execution is an execution fragment that starts from the initial configuration. This is a configuration in which all base objects have their initial values and all processes are in their initial states.

A set of primitives is historyless if all the nontrivial primitives in the set overwrite each other; we also require that each such primitive overwrites itself. A primitive is nontrivial if it may change the value of the base object to which it is applied.

Operation \( op_1 \) precedes operation \( op_2 \) in an execution \( E \), if \( op_1 \)'s response appears in \( E \) before \( op_2 \)'s invocation. We consider only deterministic implementations, in which the next
step taken by a process depends only on its state and the response it receives from the event it applies.

Roughly speaking, an implementation is linearizable \[5\] if each operation appears to take effect atomically at some point between its invocation and response; it is wait-free \[17\] if each process completes its operation if it performs a sufficiently large number of steps; it is obstruction-free (also called solo-terminating) \[18\] if each process completes its operation if it performs a sufficiently large number of steps when running solo.

The worst-case amortized step complexity (henceforth simply amortized step complexity) is defined as the worst-case (taken over all possible executions) average number of steps performed by operations. It measures the performance of an implementation as a whole rather than the performances of individual operations. More precisely, given a finite execution \(E\), an operation \(Op\) appears in \(E\) if it is invoked in \(E\). We denote by \(Nsteps(op, E)\) the number of steps performed by \(op\) in \(E\) and by \(Ops(E)\) the set of operations that appear in \(E\). The amortized step complexity of an implementation \(A\) is then:

\[
\text{AmtSteps}(A) = \max_E \sum_{op \in Ops(E)} \frac{Nsteps(op, E)}{|Ops(E)|}
\]

III. UNBOUNDED APPROXIMATE \(k\)-MULTIPLICATIVE-ACCURATE COUNTER

We present a wait-free linearizable unbounded \(k\)-multiplicative-accurate counter with \(k \geq \sqrt{n}\) whose amortized step complexity is constant (Algorithm 1).

The algorithm uses an unbounded sequence of bits initially equal to 0, denoted \(switch_0, switch_1, \ldots\) to approximately keep track of the number of increments that have been performed by the processes. For each \(i \geq 0\), \(switch_i\) can be accessed by \text{test&set} and \text{read} operations. \text{switch}_i.test&set() sets the value of \(switch_i\) to 1 and returns its previous value. A \text{read} simply returns the value of \(switch_i\).

In a nutshell, each process locally keeps an accurate count of the number of \text{CounterIncrement} operations it performs and that are not yet known by the other processes. This count is increased locally, by attempting to set a switch in an appropriate bounded range. When a process succeeds in setting a switch to 1, it will restart the local count from 0. \text{switch} bits are set in increasing order with regards to their index, one after the other.

In particular, the initial value of the threshold is 1 and after their first call to \text{CounterIncrement}, each process will attempt to set \(switch_0\). Afterwards, the sequence of \(switch_i\) with \(i \geq 1\) is partitioned into consecutive intervals of size \(k\). For any such interval \([qk+1,(q+1)k]\), where \(k\) is an integer, and for any \(j \in [qk+1,(q+1)k]\), \(switch_j\) equals to 1 indicates that \(kq^{i+1}\) instances of \text{CounterIncrement} have been performed by some process. In other words, a process \(p\) locally performs \(kq^{i+1}\) instances of \text{CounterIncrement} before attempting to set a switch in the interval \([qk+1,(q+1)k]\) and it increments its local threshold only if it knows that the last switch in this interval is set to 1 (i.e., at least \(k \cdot k^{q+1}\) instances of \text{CounterIncrement} have been performed). The threshold is incremented by a factor \(k\). There is no guarantee that \(p\) will succeed in setting to 1 one of the switches. But in this case, sufficiently many increments have been performed by the processes so that a \text{CounterRead} operation can safely ignore the increments kept locally by \(p\) and still returns a value within a bounded factor of the actual number of increments.

By using \text{test&set} to modify a \text{switch} from 0 to 1, we ensure that the \text{CounterIncrement} instances accounted for by \text{switch}_j\)' are distinct from those accounted for by \text{switch}_j', for any \(j' \neq j\).

Performing an instance of a \text{CounterRead} operation \(op\) consists in traversing the sequence of switches until 0 is found. An approximation of the total number of \text{CounterIncrement} is then deduced from the index of the last switch \(j\) that \(op\) found equal to 1. The value returned is the sum of the \text{CounterIncrement} operations represented by each switch from \(switch_0\) to \(switch_j\). In particular, \(switch_q\) counts for one \text{CounterIncrement}, and each \(switch_i\) in an interval \([qk+1,(q+1)k]\) for some integer \(q \leq q\), counts for \(k^{q+1}\) \text{CounterIncrement} operations, where \(switch_j\) belongs to the interval \([qj,k+1,(qj+1)k]\).

A. The \text{CounterIncrement} operation

Each process \(i\) is equipped with two persistent local variables, \(l\text{counter}_i\) and \(\text{limit}_i\). The former stores the number of \text{CounterIncrement} instances performed by process \(i\) not yet announced to the other processes; and the latter stores the threshold on the number of \text{CounterIncrement} that can be performed by process \(i\) without informing the other processes.

When a \text{CounterIncrement} operation is invoked by a process \(i\), \(l\text{counter}_i\) is first incremented (line 11). To ensure that a \text{CounterRead} operation instance returns a value that is within a multiplicative factor \(k\) of the actual number of increments, when \(l\text{counter}_i\) reaches a certain threshold stored in \(\text{limit}_i\), process \(i\) tries to inform the other processes of the number of increments it has performed locally (lines 12). The value of \(\text{limit}_i\) is initially 1 and is multiplied by \(k\) each time it is modified (line 17 and line 23). When \(l\text{counter}_i = \text{limit}_i = k^{q+1}\) for some integer \(q\), process \(i\) tries to set to 1 one of the \(k\) \(switch_j\) whose index \(j\) is in the corresponding range \([qk+1,(q+1)k]\) (lines 15 23). If it succeeds, it resets the local counter \(l\text{counter}_i\). The number of \text{CounterIncrement} instances it has performed locally has been announced to the other processes, and thus will be taken into account by future \text{CounterRead} operations.

Additionally, process \(i\) writes the index of the switch it sets together with a sequence number into a shared variable \(H[i]\) (lines 17 and 18). As explained later this pair is intended to help \text{CounterRead} operation instances to complete. Finally, the process will also update the value of the local persistent variable \(lq\) to indicate the index of the switch it managed to set within the interval (line 22). By doing so, we ensure that the process will avoid attempting to reset the same switches every
time it reaches the threshold of \( \text{limit}_i \) in the current interval by starting from the index \( qk + l_0 \) in the next attempt. If it does not succeed, every \( \text{switch}_j \), where \( j \in [qk + 1, (q + 1)k] \) is set. We show in the proof that for \( k \geq \sqrt{n} \), this number is sufficiently large for allowing \( \text{CounterRead} \) operations to return values within a factor \( k \) of the total number of \( \text{CounterIncrement} \) instances (Section III-C). The threshold \( \text{limit}_i \) is then incremented by a factor \( k \) (line 28) and the value of \( l_0 \) is reset to 1 (line 24).

**B. The \text{CounterRead} operation**

When a \text{CounterRead} operation is invoked, process \( i \) scans the first and last \( \text{switch} \) of each interval of \( k \) switches, looking for the first one that is not yet set to 1. When such a switch is found, the index \( h \) of the last switch read that was equal to 1 is stored in the persistent local variable \( \text{last}_{\text{t}} \) to avoid scanning the sequence from the beginning each time. We compute the value \( \text{ret} \) returned by the \text{CounterRead} operation in the function \( \text{Return Value}(p, q) \) where \( h = q \cdot k + p \) (line 30). First, we consider the required increments needed to set all the switches in the current interval \( [qk + 1, (q + 1)k] \) by adding to \( \text{ret} \) the value \( q \cdot k^{q+1} \) (line 31). Next, we add 1 to \( \text{ret} \) to account for the first switch \( \text{switch}_0 \) (line 31), and then for each previous interval \( [(l-1)k+1, lk] \) where \( 1 \leq l \leq q \), we add \( k^{l+1} \) to \( \text{ret} \) (line 33). Finally, we return the computed value \( \text{ret} \) multiplied by a factor \( k \) to ensure \( \text{ret} \) falls in the approximation range of the \( k \)-multiplicative-accurate counter.

However, it may be the case that the condition at line 37 is never verified, as other processes may concurrently execute \text{CounterIncrement} operations. Thus, to ensure wait-freedom, we employ the following helping mechanism: a \text{CounterIncrement} operation by a process \( i \) that succeeds to set a \( \text{switch}_j \) writes the index \( j \) of this switch together with a sequence number in the shared register \( H[j] \) (lines 17 and 18). A \text{CounterRead} operation \( op \) that fails to find a switch to 0 after \( \theta(n) \) steps, reads all the \( n \) shared registers \( H[i] \) with \( i \in \{1, \ldots, n\} \). If a consistent value is found, then it returns at line 55. Otherwise, it executes another \( \theta(n) \) steps. The first time \( op \) scan the array \( H \), it stores the sequence number read in each \( H[j] \), denotes \( sn_j \). When scanning \( H \) again, \( op \) will select a pair whose timestamp is greater than or equal to \( sn_j +2 \). This ensures, that the corresponding switch has been set by process \( j \) in the execution interval of \( op \).

**C. Proof**

1) **Wait-freedom and technical lemmas:** Let \( E \) be an execution of the \( k \)-multiplicative-accurate unbounded counter implemented in Algorithms 1

**Lemma III.1.** Operations \( \text{CounterIncrement}() \) and \( \text{CounterRead}() \) are wait-free.

**Proof.** Let \( op_r \) and \( op_w \) denote a \text{CounterRead} and \text{CounterIncrement} instance respectively in \( E \). The number of steps taken during \( op_w \) is bounded since at most the process will attempt to set \( k \) switches during a call to \text{CounterIncrement} and there are no other loops or function calls in the \text{CounterIncrement} operation.

Suppose by contradiction that \( op_r \) does not terminate. Meaning that every bit \( \text{switch}_k \) it reads has been set to 1. Since the bits are initially 0, there is at least one process \( q \) that infinitely often performs a successful test&set operation on these bits. Note that each time this occurs, \( q \) increments its sequence number \( sn_q \) and reports the new value in the helping array \( H \) (lines 17-18). As every \( n \) iterations of the while loop, \( op_r \) scans the array \( H \), it will eventually detects that the sequence number of \( q \) has been incremented at least twice, hence \( op_r \) terminates via the helping mechanism (lines 50-55). Therefore, operations \( \text{CounterIncrement} \) and \( \text{CounterRead} \) are wait-free.

2) We continue with a few technical lemmas.

**Lemma III.2.** Switches are set to 1 in \( E \) in increasing order of their index, starting from \text{switch}_0.

**Proof.** For each process \( p \) the initial value of \( \text{limit}_p \) is 1 and of \( \text{counter}_p \) is 0, thus the first \text{CounterIncrement} operation by process \( p \) applies a test&set primitive to \( \text{switch}_0 \) according to lines 11-12-13-27. We now prove that for any given process \( p \) and for any \( j \geq 1 \), \( p \) applies a test&set primitive (if any) on each of the switches with indexes in the interval \( [(j-1) \cdot k+1, \ldots j \cdot k] \) in an increasing order of their index, starting from \( \text{switch}_{(j-1) \cdot k+1} \). First observe that for any process \( p \), the initial value of \( l_0 \) is 1, and \( l_0 \) is set to 1 iff the value of \( \text{limit}_p \) is multiplied by a factor \( k \) (lines 24-28 and lines 21-22). This implies that when a new \( j \) is computed at line 13 the value of \( l_0 \) is 1.

Then the first iteration of the for loop at line 15 starts at \( l = (j-1) \cdot k+1 \). Also, the value of \( l \) is incremented by one at each iteration of the for loop at line 15 unless \( p \) successfully sets a \( \text{switch}_{(j-1) \cdot k+i} \) with \( i \in \{1, \ldots, k\} \). In this latter case, the value of \( l_0 \) is modified at line 22 and takes the value \( i+1 \) if \( i < k \), or \( l \) otherwise (we reach the end of the set). If \( l_0 \) takes a value different from 1, that is \( l \neq j \cdot k \), (otherwise the claim is proved), then the \text{CounterIncrement} operation returns at line 23 without modifying the value of \( \text{limit}_p \). Thus, in the execution of a successive \text{CounterIncrement} operation (if any), process \( p \) will apply the next test&set primitive (if any) to \( \text{switch}_{j \cdot k+i+1} \) (because of lines 12-13-15).

The value of \( \text{limit}_i \) is multiplied by \( k \) (and thus the value of \( j \) is incremented by one) only after a process has applied a test&set primitive (both successfully or not) to the last switch in the current interval \( [(j-1) \cdot k+1, \ldots j \cdot k] \) with \( \log_k(\text{limit}_i) = j \) (lines 21-28). This completes the proof.

3) **Lemma III.3.** For any given execution \( E \), if a \text{CounterRead} operation \( op \) returns the value computed in \( \text{Return Value}(p, q) \) at line 55, then \( \text{switch}_{q \cdot k+p} \) was equal to 0 before the invocation of \( op \) and the test&set primitive that sets \( \text{switch}_{q \cdot k+p} \) to 1 is applied during the execution interval of \( op \).
Algorithm 1: k-multiplicative-accurate unbounded counter, code for process i.

1. Shared variables
2. switch \(j \in \{0, 1\} : \) for each \(j \in \mathbb{N}\), a 1-bit register that supports test&set and read primitives, initially all 0
3. \(H[n] : \) an array of \(n\) integer pairs \((val, sn)\)

4. Persistent local variables
5. \(last_i, \in \mathbb{N}_0 : \) largest index of a switch accessed by \(i\), initially 0
6. \(lcounter, : \) number of unannounced CounterIncrement by process \(i\), initially 0
7. \(limit_i, : \) number of CounterIncrement that process \(i\) can perform locally, initially 1
8. \(sn_i, : \) number of switches set to 1 by process \(i\), initially 0
9. \(l_0, : \) index of last switch accessed by the process \(i\) in the current set of switches, initially 1

10. Function CounterIncrement()
11. \(lcounter_i : = lcounter_i + 1\)
12. if \(lcounter_i \leq \text{limit}_i\), then
13. \(j : = \log(k(lcounter_i))\)
14. if \(j > 0\) then
15. for \(j = (j - 1)k + l_0, \ldots, j \cdot k\) do
16. if \(\text{switch}_j.\text{test}&\text{set}() = 0\) then
17. \(sn_i : = sn_i + 1\)
18. \(H[i] : = (t, sn_i)\)
19. \(lcounter_i : = 0\)
20. if \(\ell = jk\) then
21. \(\text{limit}_i : = k \cdot \text{limit}_i\)
22. \(l_0 : = 1 + \ell \mod k\)
23. return
24. else
25. if \(\text{switch}_0.\text{test}&\text{set}() = 0\) then
26. \(\text{limit}_i : = k \cdot \text{limit}_i\)
27. return
28. \(\text{Function ReturnValue}(p,q)\)
29. \(\text{ret} : = 1 + p \cdot k^{t+1}\)
30. if \(q \geq 1\) then
31. \(\text{ret} : = \text{ret} + \sum_{i=1}^{q} k^{i+1}\)
32. return \(k \cdot \text{ret}\)

35. Function CounterRead()
36. \(c : = 0\)
37. while \(\text{switch}_\text{last}_i, \neq \text{null}\) do
38. \(p : = \text{last}_i \mod k\)
39. \(q : = \lfloor \frac{\text{last}_i}{k} \rfloor\)
40. if \(\text{last}_i \mod k = 0\) then
41. \(\text{last}_i : = \text{last}_i + 1\)
42. else
43. \(\text{last}_i : = \text{last}_i + k - 1\)
44. \(c : = c + 1\)
45. if \(c \mod n = 0\) then
46. for \(j = 1, \ldots, n\) do
47. \(\text{help}_p[j] : = H[j].\text{sn}\)
48. else
49. for \(j = 1, \ldots, n\) do
50. \((val, sn) : = H[j]\)
51. if \(sn - \text{help}_p[j] \geq 2\) then
52. \(p : = val \mod k\)
53. \(q : = \lfloor \frac{val}{k} \rfloor\)
54. return ReturnValue(p, q)
55. if \(\text{last}_i = 0\) then
56. return 0
57. return ReturnValue(p, q)

Proof. At line \(51\) \(op\) reads a pair \((val, \sigma)\) from an entry \(H[p']\) of the helping array \(H\) where \(val = q \cdot k + p\). According to lines \(16\) \(17\) and \(18\) a unique process \(p'\) sets to 1 the \(\text{switch}_{\text{val}}\) and associates with \(val\) the sequence number \(\sigma\) computed at line \(17\) before writing the pair \((v, \sigma)\) to \(H[p']\) in the execution of a CounterIncrement operation \(op'\).

Let \(p\) be the process that executes the CounterRead operation \(op\). Denote by \(\sigma'\) the value of \(H[p'].\text{sn}\) read by \(p\) at line \(48\) in the execution of \(op\). According to line \(52\) \(\sigma - \sigma' \geq 2\). This means that process \(p'\) executes line \(17\) at least twice during the execution interval of \(op\). In particular \(p'\) executes the step that set \(\text{switch}_{\text{val}}\) to 1 after \(op\) was invoked by \(p\). This proves the claim.

2) Linearizability: We next define the linearization \(L\) of the operations in \(E\) by first removing any CounterRead operation that did not complete and any incomplete CounterIncrement operation that has not successfully executed line \(16\).

Let \(OP_W\) be the set of (complete and incomplete) CounterIncrement operations that successfully set a switch while executing line \(16\). Let \(OP_{LO}\) be the remaining complete CounterIncrement operations in \(E\) and \(OP_R\) be the set of complete CounterRead operations in \(E\). Observe that each CounterIncrement operation successfully sets at most one switch, and each switch is successfully set by at most one process. Thus we can univocally associate each operation in \(OP_W\) with the switch it sets. We order the operations in \(OP_W \cup OP_{LO} \cup OP_R\), according to the following rules:

1) We linearize each operation in \(OP_W\) at the step where it sets its corresponding switch. By claim \(III.2\) operations in \(OP_W\) are totally ordered and this order respect the real-time order. In the following we denote \(opw_{ij}\) the \(i\)-th operation in \(OP_W\) according to our linearization order with \(i \geq 0\).
Let $\mathcal{L}$ be a linearizable implementation of a $k$-multiplicative-accurate counter.

**Claim III.4.** Let $opr$ be a CounterRead operation. We have that $opr$ is linearized at some point after its invocation.

**Lemma III.5 (Linearizability).** Algorithm 1 is a linearizable implementation of a $k$-multiplicative-accurate unbounded counter.

**Proof.** Let $op_1$ and $op_2$ be two operations in $E$ such as $op_1$ ends before $op_2$ is invoked. We prove that the linearization order $L$ respects the real-time order, thus $op_1$ precedes $op_2$ in $L$. First, we have the following claim:

- Let $op_1$ and $op_2$ be two CounterIncrement operations. If at least one of these operations is in $OP_{LO}$, the claim trivially follows from rule 3. Otherwise it is already proved in rule 1.

- Let $op_1$ and $op_2$ be two CounterRead operations. If both $op_1$ return normally the claim trivially holds from rule 2 and claim III.4. So consider that $op_1$ returns through the helping mechanism and let $h_1 = q \cdot k + p$ be the index of the switch read by $op_1$ at line 54 the last time before returning. According to rule 2, $op_1$ is linearized immediately after $opw_{h_1}$. Also, by Lemma III.3 and rule 2, $op_2$ is linearized after $opw_{h_1}$. The claim follows since according our linearization rules, if several operations are ordered at the same position, they are ordered respecting their real time order.

- Consider that $op_1$ is a CounterIncrement and $op_2$ is a CounterRead operation. The claim follows from rules 1 and 2 and claim III.4 (the reverse follows a similar reasoning).

Next claim will be useful for proving that the ordering $L$ is consistent with the sequential specification of the $k$-multiplicative-accurate counter.

**Claim III.6.** Let $op$ be a CounterRead operation invoked by a process $p_i$ that returns $ReturnValue(p, q)$. Then, the number of CounterIncrement operations linearized before $op$ in $L$, denoted $\nu$, is at least $u_{min} = \sum_{i=1}^{q} k^{i+1} + p \cdot k^{q+1}$ and at most $u_{max} = \sum_{i=1}^{q} k^{i+1} + p(k-1)k^{q+1} + n(k^{q+1} - 1)$ where $n$ is the number of processes.

**Proof.** Let $op$ be a CounterRead operation invoked by a process $p_i$ that returns $ReturnValue(p, q)$ and let $h = q \cdot k + p$ with $p \geq 0$. Consider the CounterIncrement operation by $p_j$ that sets $1$ to the switch $h$, denoted $opw_h$.

$op$ is linearized at the step where it reads $switch_h$ if it returns normally, or immediately after $opw_h$. Thus, from our linearization rules, the minimal number of CounterIncrement operations that are linearized before $op$ includes each $opw_i$ in $OP_W$ with $0 \leq i \leq h$, and every CounterIncrement operation in $OP_{LO}$ linearized before $op$.

We have by construction that each $switch_s$ in the $(l+1)$-th set of $k$ switches indexed in the interval $[l \cdot k + 1 \ldots (l + 1)k]$ with $l \geq 0$, requires a process to perform $k^{l+1}$ CounterIncrement operation instances before attempting to set $switch_s$ to 1. In other words a process $p_i$ needs its local variable $lcounter_i$ to be equal to $k^{l+1}$ before it can attempt to set any $switch_s$ in $[l \cdot k + 1 \ldots (l + 1)k]$ (line 19).

Since the value of $lcounter_i$ is reset to 0 after a successful test&set primitive is applied on a switch (line 19), the sets of CounterIncrement operation instances associated with any pair of successful test&set primitives are disjoint. Thus, $u_{min} = 1 + k \sum_{i=0}^{l-1} k^{i+1} + p \cdot k^{q+1} = 1 + k \sum_{i=1}^{l} k^{i+1} + p \cdot k^{q+1}$ since we account for, in addition to the $p$ switches in the $(q + 1)$-th set and $switch_0$, all $k$ switches in each of the sets indexed from 1 to $q$.

Similarly, we compute an upper bound $u_{max}$ on the maximum number of CounterIncrement linearized before $op$. First suppose that $op$ returns normally. As already said, $op$ is linearized at the step where it reads $switch_h$ with $h = qk + p$. We have two possible cases either $p$ is equal to 0 or it is equal to 1 because the process checks the first and last switch of each set during the $CounterRead()$ instance. These two cases are depicted in Figure 4 (a) and (b) respectively. If $p$ is equal to 0, then process $p_i$ read $switch_{q+1} = 0$ in the execution of $op$, and according to our linearization rules $opw_{q+1}$ is linearized after $op$. In a similar way, if $p$ is 1, $p_i$ read $switch_{(q+1)k} = 0$ and $opw_{(q+1)k}$ is linearized after $op$. However, in this second case, all the $k - 1$ switches with $j \in [q \cdot k + 2 \ldots (q + 1)k - 1]$ may have been set to 1 before $op$ applied its read to $switch_{q+1}$, and all the corresponding $opw_j$ may be linearized before $op$. Thus, the number of $opw_j$ linearized before $op$ is smaller than or equal to $1 + \sum_{i=1}^{q} k^{i+1} + p(k-1)k^{q+1}$. It remains to count the number of CounterIncrement in $OP_{LO}$ linearized before $op$. For every process $p_i$ the value of $lcounter_i$ is smaller than $k^{q+1}$ immediately before $p$ read either $switch_{q+1} = 0$ or $switch_{(q+1)k} = 0$ in the execution of $op$. Since a process resets the value of its local counter only when it succeeds to set a switch to 1 (line 19), $lcounter_i$ defines the number of
CountIncrement by \( p \), in \( OP^k_{LO} \) that are linearized before \( op \). Therefore, \( u_{max} = 1 + i \sum_{i=1}^n k^{i+1} + p(k-1)k^{q+1} + n(k^{q+1} - 1) \) where \( n \) is the number of processes. If \( op \) returns \( \text{helping mechanism} \), then according to rule \( \text{[26]} \), it is linearized immediately after \( opw_{k+p} \) with \( 0 \leq p < k \). Thus, \( 1 + \sum_{i=1}^q k^{i+1} + pk^{q+1} \) is the number of CountIncrement in \( OP^k_{W} \) linearized before \( op \). Since \( p < k \) the local counter of every process immediately after \( opw_{k+p} \) sets the corresponding switch is smaller than \( k^{q+1} \). Since \( k > 1 \), the claim follows.

Let \( op \) be a CountRead operation and let \( v_{op} = \text{ReturnValue}(p, q) \) be the value it returns. According to lines \( 31 \) and \( 33 \) of Algorithm \( 1 \), \( v_{op} = k(1 + \sum_{i=1}^q k^{i+1} + p \cdot k^{q+1}) \); that is \( v_{op} = k \cdot u_{min} \). According to claim \( III.6 \), the number of CountIncrement operations linearized before \( op \) in \( L \), denoted \( u \), is at least \( u_{min} = 1 + \sum_{i=1}^q k^{i+1} + p \cdot k^{q+1} \) and at most \( u_{max} = 1 + \sum_{i=1}^q k^{i+1} + p(k-1)k^{q+1} + n(k^{q+1} - 1) \) (where \( n \) is the number of processes). And we have:

\[
\frac{u_{max}}{k} = \frac{1}{k} + \sum_{i=1}^q k^i + \frac{k-1}{k} k^{q+1} + \frac{n}{k} (k^{q+1} - 1)
\]

\[
\geq \sum_{i=1}^q k^i + p \cdot k^{q+1} + n \cdot k^q
\]

And \( v_{op} = k(1 + k \sum_{i=1}^q k^i + p \cdot k^{q+1}) \)

\[
= k(1 + k \sum_{i=1}^{q-1} k^i + k^{q+1} + p \cdot k^{q+1})
\]

\[
= k + k \sum_{i=2}^q k^i + k^{q+2} + k^{q+2}
\]

Thus, for \( k \geq \sqrt{n} \), \( \frac{u_{max}}{k} \leq v_{op} \). Therefore, since \( p < k \), we have \( \frac{n}{k} \leq \frac{u_{max}}{k} \leq v_{op} \leq k \cdot u_{min} \leq k \cdot u \). This completes the proof.

![Fig. 1. Switches state for the proof of claim III.6. The dotted line indicate the \( q + 1 \)h interval of consecutive switches. When \( p = 1 \), \( op \) does not distinguish between cases b.1) and b.2)](image)

3) Complexity analysis:

Lemma III.7. If process \( p \) applies a test\&set() primitive to a switch \( \alpha \) with \( i \cdot k + 1 \leq \alpha \leq (i + 1) \cdot k \) for some integer \( i \geq 0 \), then \( p \) has performed at least \( k^{i+1} \) CountIncrement operations.

Proof. Suppose that \( p \) has executed a test\&set() primitive to a switch \( \alpha \) with \( i \cdot k + 1 \leq \alpha \leq (i + 1) \cdot k \) in the execution of a CountIncrement() operation \( op \). According to line \( 13 \), \( j \) was equal to \( i + 1 \) when computed at line \( 13 \) meaning that \( l_{\text{counter}_p} \) was equal to \( k^{i+1} \). The claim holds because \( l_{\text{counter}_p} \) is incremented only at line \( 11 \), that is once for each CountIncrement() operation performed by \( p \).

Lemma III.8 (Amortized complexity). For \( k \geq \sqrt{n} \), the amortized complexity of Algorithm \( 1 \) is constant.

Proof. Let \( E \) be a finite execution of the unbounded \( k \)-multiplicative-accurate counter object implemented in Algorithm \( 1 \). Let \( r \) denote the number of CountRead() instances in \( E \) and \( s \) be the number of CountIncrement() instances in \( E \). We additionally denote \( \text{Ops}_W(E) \) the set of CountIncrement() operations that execute at least one step in \( E \), and \( \text{Ops}_R(E) \) the set of CountRead() operations in \( E \). We want to compute

\[
\text{AmtSteps}(E) = \sum_{op \in \text{Ops}_W(E) \cup \text{Ops}_R(E)} \text{Nsteps}(op, E)
\]

where \( \text{Nsteps}(op, E) \) is the number of steps executed by \( op \) in \( E \).

Let \( \text{Ops}_{W_p}(E) \) denote the CountIncrement() operations in \( \text{Ops}_W(E) \) executed by process \( p \) and \( s_p \) denote the total number of CountIncrement() operations executed by process \( p \). Let \( \alpha_p \) be the index of the furthest switch accessed by a process \( p \) when executing any of the CountIncrement() operations in \( \text{Ops}_{W_p}(E) \). We have that \( i_p \cdot k + 1 \leq \alpha_p \leq (i_p + 1) \cdot k \) for some integer \( i_p \geq 0 \) (the case where \( \alpha_p = 0 \) is trivial).

In the worst case, process \( p \) applies a test\&set() primitive to switch \( \alpha \) for every \( h \in [0, \ldots, \alpha_p] \) and one additional step to write into \( H[p] \) (line \( 18 \)) each time \( p \) successfully set one of those switches. On the other hand, by Lemma \( III.7 \) if process \( p \) applies a test\&set() primitive to the switch \( \alpha_p \), then it has performed at least \( k^{i_p+1} \) CountIncrement() operations. Therefore,

\[
\sum_{op \in \text{Ops}_{W_p}(E)} \text{Nsteps}(op) \leq 2 \cdot (i_p + 1) k + 1
\]

\[
\text{And } s_p \geq k^{i_p+1}
\]

Thus, the total number of steps executed by the set of all processes \( P \) in order to perform the CountIncrement() operations in \( E \) is:

\[
\sum_{op \in \text{Ops}_W(E)} \text{Nsteps}(op) \leq \sum_{p \in P} \sum_{op \in \text{Ops}_{W_p}(E)} \sum_{p \in P} \text{Nsteps}(op) \leq 2 \cdot (i_p + 1) k + 1
\]

\[
\text{And } s = \sum_{p \in P} s_p \geq \sum_{p \in P} k^{i_p+1}
\]
Now we consider the number of steps applied by each process to perform CountRead operations. Let $\alpha$ be the index of the furthest switch set to 1 by any process in $P$. If $\alpha = 0$ then the claim follows. Then suppose $i \cdot k + 1 \leq \alpha \leq (i+1) \cdot k$ for some integer $i \geq 0$. For any sequence of switches with the index in $[j \cdot k + 1, \ldots, (j+1) \cdot k]$ with $0 \leq j \leq i$ a process $p$ only reads the first and the last switch in such interval (i.e., \texttt{switch}$_{j \cdot k+1}$ and \texttt{switch}$_{(j+1) \cdot k}$). This is because at the beginning $last_p$ is equal to 0 and it is incremented by 1 if it is a multiple of $k$ (at line 47), by $k-1$ otherwise (line 43). Also, $last_p$ is a persistent variable, thus a process $p$ reads a given switch that has been set to 1 at most once. This implies that the total number (in all its CountRead operations) of read primitives applied by a process $p$ to the switches is less or equal to $2(i+2)$ (2 per each of the $i+1$ intervals, plus \texttt{switch}$_0$ and \texttt{switch}$_{i+1}$). Furthermore, any CountRead() operation executes $O(n)$ steps of the for loop at line 47 or line 50 once every $n$ iterations of the while loop (when the condition of line 45 is satisfied). This means that the total number of steps executed by a process $p$ when performing its CountRead() operations is less or equal to $4(i+2)$. Thus,

$$\sum_{op \in Ops_R(E)} N\text{steps}(op) \leq \sum_{p \in P_r} 4(i+2) \leq 4(i+2) \cdot n_r,$$

where $P_r$ is the set of processes who have invoked at least one CountRead() operation and $n_r$ is the cardinality of $P_r$. Consider $n_r > 0$, the other case is trivial. Therefore:

$$\text{AmtSteps}(E) \leq \sum_{p \in \mathcal{P}} 2(i_p + 1)k + 1 + \frac{4(i+2) \cdot n_r}{s+r} \sum_{p \in \mathcal{P}} k^{i_p+1} + r + r,$$

Furthermore, by lemma III.7 the minimum number of instances of the CountIncrement() operation executed to set the switch $\alpha$ is $k^{i+1}$. Thus,

$$\text{AmtSteps}(E) \leq \sum_{p \in \mathcal{P}} 2(i_p + 1)k + 1 \frac{1}{k} + \frac{4(i+2) \cdot n_r}{s+r} \sum_{p \in \mathcal{P}} k^{i_p+1} + r + r.$$

We have $k^r \geq x + 1$ for $k \geq e$ and $\forall x \in \mathcal{R}$, it follows:

$$\sum_{p \in \mathcal{P}} 2(i_p + 1)k + 1 \frac{1}{k} \sum_{p \in \mathcal{P}} k^{i_p+1} + r \leq \frac{\sum_{p \in \mathcal{P}} 2(i_p + 1)k + 1}{\sum_{p \in \mathcal{P}} (i_p + 1)}.$$

If $i = 0$, and since $r \geq n_r$ we have:

$$\frac{4(i+2) \cdot n_r}{k^{i+1} + r} \leq \frac{8 \cdot n_r}{k + r} \leq 8.$$

If $i \geq 1$, because $n_r \leq n$ and $k^{i+1} \geq i \cdot k^2$ we have:

$$\frac{4(i+2) \cdot n_r}{k^{i+1} + r} \leq \frac{4(i+2) \cdot n}{i \cdot k^2 + r}.$$

Resulting in an amortized complexity of $O(1)$ for $k \geq \sqrt{n}$.

D. An Amortized Step Complexity Lower bound for k-multiplicative accurate Counters

In this section, we prove that the amortized step complexity of solo-terminating implementations of $k$-multiplicative accurate counters is $\Omega(\log_{q+1} p_k)$ for $k \leq \sqrt{n}/2$, assuming the implementation uses base objects that support only read, write and either reading or regular conditional primitives of arity $q$ or less. A primitive has arity $q$ if it is applied atomically to a vector of $q$ base objects. In all the paper but this section, we consider $q = 1$. Definitions and most of the technical lemmata hold from [16]. In the following we provide the main idea of the lower bound and the Lemma that most differs from the original work. To this aim, in the following we remember some of the definitions formalized in [16].

Processes communicate with one another by issuing events that apply read-modify-write (RMW) primitives to vectors of base objects. We assume that a primitive is always applied to vectors of the same size and that all the base objects to which a primitive is applied are over the same domain $D$. A RMW primitive, applied to a vector of $k$ base objects over some domain $D$, is characterized by a pair of functions, $(g,h)$, where $g$ is the primitive’s update function and $h$ is the primitive’s response function. The update function $g : D^k \times W \rightarrow D^k$, for some input-values domain $W$, determines how the primitive updates the values of the base objects to which it is applied.

Let $e$ be an event, issued by process $p$ after execution $E$, which applies the primitive $(g,h)$ to a vector of base objects $(o_1, \ldots, o_k)$. Then $e$ atomically does the following: it updates the values of objects $o_1, \ldots, o_k$ to the values of the components of the vector $(v_1, \ldots, v_k)$, respectively, where $\vec{v} = (v_1, \ldots, v_k)$ is the vector of values of the base objects after $E$, and $w \in W$ is an input parameter to the primitive. We call $\vec{v}$ the object-values vector of $e$ after $E$. The RMW primitive returns a response value, $h(\vec{v}, w)$, to process $p$. If $W$ is empty, we say that the primitive takes no input.

Next, we revise the concept of conditional synchronization primitives.

**Definition III.1.** A RMW primitive $(g,h)$ is conditional if, for every possible input $w$, $|\{v|g(\vec{v}, w) \neq \vec{v}\}| \leq 1$. Let $e$ be an event that applies the primitive $(g,h)$ with input $w$. The change point of $e$ is the unique vector $\vec{c}_w$ such that $g(\vec{c}_w, w) \neq \vec{c}_w$; any other vector is a fixed point of $e$.

For example, $k$-CAS is a conditional primitive for any integer $k \geq 1$. The single change point of a $k$-CAS event with input $\langle old_1, \ldots, old_k, new_1, \ldots, new_k \rangle$ is the vector $\langle old_1, \ldots, old_k \rangle$. Read is also a conditional primitive, since read events have no change points.

A RMW event is invisible if its object-values vector is a fixed point of the event when it is issued. A RMW event $e$ that is applied by process $p$ to an object vector is also invisible if, before $p$ applies another event, a write event is applied to each object $o_i$ that is changed by $e$ before another RMW event is applied to $o_i$. If a RMW event $e$ is not invisible in an execution
is of base objects. We say that an event is visible in E on o. If e is not invisible in E, we say that e is a visible event in E.

Lower bound: The key intuitions behind the following lower bound is that first, in any n-process execution of a k-multiplicative accurate counter implementation, ‘many’ processes need to be aware of the participation of ‘many’ other processes in the execution, and second, if processes only use read, write and conditional primitives, then a scheduling adversary can order events so that information about the participation of processes in the computation accumulates ‘slowly’.

We formalize the first key intuition by proving Lemma III.10. The rest is straightforward from the lower bound in the original work [16].

The next definition captures the extent to which processes are aware of the participation of other processes in an execution. Intuitively, a process p is aware of the participation of another process q if p reads a shared-memory value that was either directly written by q or indirectly influenced by a value written by q. The following definitions formalize this notion.

Definition III.2. Let e_q be an event by process q in an execution E, which applies a non-trivial primitive to a vector v of base objects. We say that an event e_p in E by process p is aware of e_q if e_p accesses a base object o such that at least one of the following holds:

- There is a prefix E' of E such that e_q is visible on o in E' and e_p is an RMW event that applies a primitive other than write to o, and it follows e_q in E', or
- there is an event e_r that is aware of e_q in E and e_p is aware of e_r in E.

If an event e_p of process p is aware of an event e_q of process q in E, we say that p is aware of e_q and that e_p is aware of q in E.

The following definition quantifies the extent to which a process is aware of the participation of other processes in an execution.

Definition III.3. Process p is aware of process q after an execution E if either p = q or p is aware of an event of q in E. The awareness set of p after E, denoted AW(E,p), is the set of processes that p is aware of after E.

The following lemma proves a relation between the value returned by a CounterRead operation instance of a process in some execution and the size of that process’ awareness set after that execution. This is our main technical contribution to the lower bound.

Lemma III.10. Let E be an execution of a solo-terminating k-multiplicative accurate counter object implementation where each process executes one instance of the CounterIncrement() operation followed by one instance of the CounterRead() operation. If the CounterRead() instance by a process p returns i in E then \(|AW(E,p)| \geq \frac{1}{k} i\).

Proof. Assume, by way of contradiction, that there is an execution E where each process executes one instance of the CounterIncrement() operation followed by one instance of the CounterRead() operation, and a process p such that a CounterRead() instance by p, namely op, returns i and \(|AW(E,p)| < \frac{i}{k}\).

We construct a new execution E' as follows: for any process q \(\notin AW(E,p)\), we first remove all the events of q from E; then, for any process q', we remove all the events of q' that are aware of q. Note that if an event e_{q'} of q' is aware of q, then all following events by q' are also aware of q and are removed. Also, no events of p are removed since p is aware only of processes in AW(E,p).

We prove that E' is an execution, and that it is indistinguishable from E. We consider events in the order they appear in E'. Let e'_q be an event by process q' that appears in E', namely E' = E'_1e'_2. Since e'_q is also in E, we can also write E = E_1e'_2. For the induction, assume that E'_1 is an execution and that it is indistinguishable to every process that appears in it from E_1. In particular, q' does not distinguish between E'_1 and E_1 and takes the same step after both of them. To see why q' obtains the same response in e'_q after E'_1 and after E_1, note that it can return a different response only if in E, e'_q is aware of an event e that was removed from E_1. This happens only if e is aware of some process q \(\notin AW(E,p)\), meaning that in E, e'_q is also aware of q, contradicting the fact that e'_q was not removed. Hence E'_1e'_q is an execution and q' does not distinguish between E_1e'_q and E_1e'_q.

This implies that the CounterRead() instance by p returns i also in E'; on the other hand, less than \(\frac{i}{k}\) processes participate in E'. Let E'' be the extension of E' in which the processes that participate in E' complete their operation instances, one at a time. This execution exists by solo-termination, and results in a quiescent execution. However, less than \(\frac{i}{k}\) instances of CounterIncrement() operations completed in E'', and we have that p returns i when invoking op. Thus, the response of the op is not linearizable. In particular, consider any linearization L of E'' and let v be the number of CounterIncrement() instances linearized before op in L, we have that \(\frac{i}{k} \leq i \leq k \cdot v < k \cdot \frac{n}{k} = i\).

Corollary III.10.1. Let E be a quiescent n-process execution of a solo-terminating k-multiplicative accurate counter implementation, where each process executes one instance of the CounterIncrement() operation followed by one instance of a CounterRead() operation. Then, the awareness sets of \(\frac{n}{k}\) processes contain at least \(\frac{n}{k^2}\) other processes after E.

Proof. Let L denote any linearization of E, and let op be the i-th CounterRead() instance in L. Since op is the i-th instance of CounterRead() in L, it returns v such that v \(\geq \frac{i}{k}\). By considering the last \(\frac{n}{k}\) processes linearized and by Lemma III.10 the claim follows.

Information about processes that participate in an execution is transferred through base objects. To complete the proof, we need to show that each of the \(\frac{n}{k}\) processes has to apply \(\Omega(\log_{q+1}(n/k^2))\) events to build its awareness set (proved in the Appendix).
The following theorem formalize our step complexity lower bound.

**Theorem III.11.** Let $A$ be an $n$-process solo-terminating implementation of a $k$-multiplicative counter from base objects that support only read, write and either reading or regular conditional primitives of arity $q$ or less. Then $A$ has an execution $E$ that contains $\Omega(n \log_{q+1}(n/k^2))$ events for $k \leq \sqrt{n}/2$, in which every process performs a single CounterIncrement() instance and a single CounterRead() instance.

IV. A $k$-MULTIPLICATIVE-ACCURATE BOUNDED MAX REGISTER

In this section, we present an implementation of a $k$-multiplicative-accurate max register. The algorithm is wait-free, and has asymptotically optimal worst-case step complexity. Indeed, we present in the next section a matching lower bound.

The key idea of our algorithm is to consider the $k$-base representation of values written to the register and have Write operations store only the index of the bit preceding (i.e., to the left of) the most significant bit (MSB) of their arguments. These indices are stored in an (accurate) $(\lceil \log_k(m - 1) \rceil + 1)$-bounded max register implemented in a wait-free manner [8].

A Read operation $R$ reads the value $p$ of the accurate max register. If it equals 0 (implying that it was not written to yet), $R$ returns 0. Otherwise, $p$ is the largest index written so far to the accurate max register and $R$ returns $k^p$. The pseudocode is presented by Algorithm 2.

Algorithm 2: A $k$-multiplicative-accurate $m$-bounded max register

1. Shared variables $M$: $(\lceil \log_k(m - 1) \rceil + 1)$-bounded max register initially 0
2. Function Read()
3.   $p \leftarrow M$.read()
4.   if $p = 0$ then return 0;
5.   else return $k^p$;
6. end
7. Function Write($v$)
8.   $p \leftarrow \lfloor \log_k v \rfloor + 1$;
9.   $M$.write($p$);
10. end

We now prove that Algorithm 2 is a correct wait-free implementation of a $k$-multiplicative-accurate max register.

**Observation 1.** Algorithm 2 is a wait-free implementation of a $k$-multiplicative-accurate $m$-bounded max register.

**Proof.** Follows directly from the wait-freedom of the max register algorithm of [8].

**Lemma IV.1.** Algorithm 2 is a linearizable implementation of a $k$-multiplicative-accurate $m$-bounded max register.

**Proof.** Let $M^k_m$ denote a $k$-multiplicative-accurate $m$-bounded max register implemented by Algorithm 2 and let $E$ be an execution of $M^k_m$. We now specify how operation instances on $M^k_m$ in $E$ are linearized. First, all the instances of Read that did not execute line 3 in $E$ and all the instances of Write operations did not execute line 2 in $E$ do not appear in the linearization. We say these are removed operations. Note that none of the removed operations has completed in $E$. For all remaining instances, we define the linearization point of a Read operation on $M^k_m$ to be the linearization point of the read operation it invoked on $M$ in $E$ (in line 3) and the linearization point of a Write operation on $M^k_m$ as the linearization point of the write operation it invokes on $M$ (in line 9). Since each non-removed operation instance on $M^k_m$ in $E$ is linearized at a step it performs (hence during its execution interval), the linearization order we have define, denoted by $L$, respects the real-time order of the operation instances in $E$.

It remains to show that $L$ satisfies the sequential specification of a $k$-multiplicative-accurate $m$-bounded max register. First note that since values written to $M^k_m$ are from $\{1, ..., m - 1\}$ and from lines 8, 9 only values from $\{1, ..., \lfloor \log_k (m - 1) \rfloor + 1\}$ are written to $M$. Let $R$ denote a Read instance in $L$ that returns 0 in line 2. Since only positive values are ever written to $M$, it follows that $R$ is not preceded in $L$ by any Write instance, hence the value of $M^k_m$ when $R$ is linearized is its initial value 0, so $R$ returns the exact value of $M^k_m$.

Assume, then, that $R$ is preceded in $L$ by one or more Write instances and returns a positive value $v = k^p$ for some $p \geq 1$. We need to prove that $v/k \leq x \leq v/k$ holds, where $v$ is the maximum value written by any Write() instance linearized before $R$ in $L$. Since $M$ is linearizable and since we have linearized all non-removed instances applied to $M^k_m$ in $E$ according the order of the operations they applied to $M$ in line 2 or in line 9, there exists a Write operation that writes some value $w$ and appears before $R$ in $L$, such that $\lfloor \log_k w \rfloor = p - 1$ and $p$ is the maximum value written to $M$ by any Write instance that precedes $R$ in $L$. Let $V = \{w | \lfloor \log_k w \rfloor = p - 1\}$ be the set of all the values written to $M^k_m$ in $L$ before $R$ whose MSB equals $p - 1$. Let $v = \max(V)$. It follows that $v$ is the maximum value written to $M^k_m$ by any Write() instance linearized in $L$ before $R$. We have $v \in [k^{p-1}, k^p - 1]$ and $x = k^p$. Consequently, $v \leq x \leq v/k$ and the sequential specification of the k-multiplicative-accurate max register is satisfied.

**Theorem IV.2.** Algorithm 2 is a wait-free linearizable implementation of a $k$-multiplicative-accurate $m$-bounded max register with worst case operation step complexity $O\left(\min\{\log_2(\log_k m), n\}\right)$.

**Proof.** Wait-freedom and linearizability follow from Observation 1 and Lemma IV.1 respectively. As for step complexity – the worst case operation step complexity of the wait-free implementation of an $m$-bounded max register of [8] is $O(\min(\log m, n))$ for both Read and Write operations. Each operation of Algorithm 2 applies a single operation on a $(\lfloor \log_k (m - 1) \rfloor + 1)$-bounded max register and a constant number of additional steps. The theorem follows.
Aspnes et al. [5] proved a worst-case step complexity on the lower bound of a class of concurrent objects called \textit{L-perturbable}, that includes objects such as max registers, counters and snapshots. \textit{L} is called the \textit{perturbation bound}. Roughly speaking, an object is \textit{L-perturbable} if, for every implementation of the object, there exists an operation \textit{Op} and an execution \textit{E}, in the course of which \textit{Op} is “perturbed” \textit{L} times. An outstanding operation \textit{Op} by process \textit{p} is said to be perturbed by a process \textit{q}, if a solo execution by \textit{q} can change the response of a solo execution by \textit{p}. They prove [5] Theorem 1] that any obstruction-free implementation of an \textit{L}-perturbable object \textit{O} from \textit{historyless} primitives has an execution in which some process accesses \( \Omega(\min(\log_2 L, n)) \) distinct base objects during a single operation instance.

\textbf{V. A Lower Bound on the Worst Case Step Complexity of k-multipllicative m-bounded Max Register and Counter}

Lemma V.1. A \textit{k}-multipllicative-accurate \textit{m}-bounded max register is \( \Theta(\log_k m) \)-perturbable for \( k > 1 \).

\textit{Proof.} Let \( O \) be a \textit{k}-multipllicative-accurate \textit{m}-bounded max register and consider an obstruction-free implementation of \( O \). We show that \( O \) is \( (\frac{1}{2}\log_k (m - 1)) \)-perturbable for a \textit{Read}() operation instance \( op_n \) by process \( p_n \). We proceed by induction where the base case for \( r = 0 \) is immediate. Let \( r < \frac{1}{2}\log_k (m - 1) \) and let \( \alpha_{r-1}\lambda_{r-1} \) be an \((r - 1)\)-perturbing execution of \( O \). If \( \alpha_{r-1}\lambda_{r-1} \) is saturated, then it is also an \( r \)-perturbing execution. Otherwise, denote by \( v_{r-1} \) the maximum input to the \textit{write()} operations linearized before \( op_n \) in the execution sequence \( \alpha_{r-1}\lambda_{r-1} \). Since \( \alpha_{r-1}\lambda_{r-1} \) is not saturated, there exists a process \( p_k \neq p_n \) that does not take steps in \( \lambda_{r-1} \). Let \( \gamma \) be the execution fragment by \( p_k \) where it finishes any incomplete operation in \( \alpha \) and then performs a \textit{write()} to the max register with the value \( v_r = k^2v_{r-1} + 1 \). Then \( op_n \) must return a value \( x \) such that \( k v_r < v_r < k v_r \) when run after \( \alpha_{r-1}\gamma\lambda_{r-1} \). It follows that an \( r \)-perturbing execution can be constructed from \( \alpha_{r-1}\lambda_{r-1} \) and \( \gamma \) as specified by [5], Definition 2. Because \( O \) is an \( m \)-bounded max register, during the \( r \)th step of the induction, the value written to the max register must satisfy \( v_r \leq m - 1 \). Consequently it suffices to have:

\[ v_r \leq (k+1)^{2r} \leq m-1 \iff r \leq \frac{1}{2}\log_{k+1}(m-1) = \Theta(\log_k m) \]

from Lemma V.1 and [5]. Theorem 1 we have the following theorem:

Theorem V.2. The worst-case step complexity of a \textit{k}-multipllicative \textit{m}-bounded max register is \( \Omega(\min(\log_2(\log_k m), n)) \).

Lemma V.3. A \textit{k}-multipllicative-accurate \textit{m}-bounded counter is \( \Theta(\log_k m) \)-perturbable for \( k > 1 \).

\textit{Proof.} Let \( O \) be a \textit{k}-multipllicative \textit{m}-bounded counter and consider an obstruction-free implementation of \( O \). We show that \( O \) is \( (\frac{1}{2}\log_k (m - 1)) \)-perturbable for a \textit{CounterRead()} operation instance \( op_n \) by the process \( p_n \). We proceed by induction where the base case for \( r = 0 \) is immediate. Let \( \alpha_{r-1}\lambda_{r-1} \) be an \((r - 1)\)-perturbing execution of \( O \). If \( \alpha_{r-1}\lambda_{r-1} \) is saturated, then it is also an \( r \)-perturbing execution. Otherwise, let \( I_r \) denote the number of \textit{CounterIncrement()} operation instances performed by the perturbing process in iteration \( r \). We have that \( I_1 = 1 \) in order for \( op_n \) to return a value greater than \( 0 \). For \( r > 1 \), if \( op_n \) runs after \( \alpha_{r-1}\lambda_{r-1} \) it can return a value that is as large as \( k \cdot \sum_{j=1}^{r-1} I_j \). Therefore, we need the number of complete \textit{CounterIncrement()} operation instances after \( \alpha_{r-1}\gamma\lambda_{r-1} \) to be at least \( k^2 \cdot \sum_{j=1}^{r-1} I_j + 1 \) for \( op_n \) to return a value greater than \( k \cdot \sum_{j=1}^{r-1} I_j \).

Besides the \textit{CounterIncrement()} operation instances in \( \gamma \), at least \( \sum_{j=1}^{r-1} I_j - (r - 1) \) have finished, therefore setting

\[ \text{\textit{Accesses } } \Omega(\min(\log_2 L, n)) \text{ distinct base objects during a single operation instance.} \]
Theorem V.4. The worst-case step complexity $k$ of a variant of deterministic approximate counters and Welch [19] of relaxed queues in the message passing systems by Talmage indicates benefit from some common relaxation of unbounded theoretical evidence that worst-case time complexity does not step complexity of the bounded variant and in the amortized factor yields an exponential improvement in the worst-case by allowing inaccuracy of even a constant multiplicative amortized step complexity.

We also show that relaxing the semantics of max registers depend on $n$ k. The maximum improvement in the worst case step complexity of unbounded counters by more than a $1/k$ is greater than a similar result has been proved for relaxed queues in the message passing systems by Talmage and Welch [19].

\[
I_r = (k^2 - 1) \cdot \sum_{j=1}^{r-1} I_j + r \text{ implies that } op_n \text{ returns at least } \\
\frac{1}{k} (\sum_{j=1}^{r-1} I_j - (r-1) + I_r) = \frac{1}{k} (\sum_{j=1}^{r-1} I_j - (r-1) + (k^2 - 1) \cdot \sum_{j=1}^{r-1} I_j + r) = \frac{1}{k} (k^2 \cdot \sum_{j=1}^{r-1} I_j + 1) \text{ which is greater than } \\
k \cdot \sum_{j=1}^{r-1} I_j \text{ as needed.}
\]

From Lemma V.3 and [5], Theorem 1, we prove the following Theorem

**Theorem V.4.** The worst-case step complexity of a $k$-multiplicative $m$-bounded counter is

$$\Omega\left(\min(\log_2((\log km)), n)\right)$$

VI. DISCUSSION

We have presented upper and lower bounds on the step complexity of a variant of deterministic approximate counters and max-registers. We have proved the possibly counter-intuitive $\frac{1}{k}$ result that when the accuracy parameter $k$ does not depend on $n$, relaxing counter semantics by allowing inaccuracy of a multiplicative factor cannot asymptotically reduce the step complexity of unbounded counters by more than a logarithmic factor. Then, we present a wait-free linearizable $k$-multiplicative-accurate counter for $k \geq \sqrt{n}$ with constant amortized step complexity.

The maximum improvement in the worst case step complexity of the bounded variant of $k$-multiplicative-accurate counters remains an open question. Also, when $k$ is constant, it is unclear whether there exists a deterministic wait-free $k$-multiplicative-accurate counter implementation with $o(\log^2 n)$ amortized step complexity.

We also show that relaxing the semantics of max registers by allowing inaccuracy of even a constant multiplicative factor yields an exponential improvement in the worst-case step complexity of the bounded variant and in the amortized step complexity of the unbounded one. Overall we provide theoretical evidence that worst-case time complexity does not indicate benefit from some common relaxation of unbounded counters and max-register while average complexity does. It is interesting to note that a similar result has been proved for relaxed queues in the message passing systems by Talmage and Welch [19].

ACKNOWLEDGMENT

Alessia Milani and Corentin Travers are supported by ANR projects Descartes and FREDDA. Adnane Khattabi is supported by UMI Relax. Danny Hendler is supported in part by ISF grant 380/18.

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