Deep Learning Stereo Vision at the edge

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Abstract—We present an overview of the methodology used to build a new stereo vision solution that is suitable for System on Chip. This new solution was developed to bring computer vision capability to embedded devices that live in a power constrained environment. The solution is constructed as a hybrid between classical Stereo Vision techniques and deep learning approaches. The stereoscopic module is composed of two separate modules: one that accelerates the neural network we trained and one that accelerates the front-end part. The system is completely passive and does not require any structured light to obtain very compelling accuracy. With respect to the previous Stereo Vision solutions offered by the industries we offer a major improvement is robustness to noise. This is mainly possible due to the deep learning part of the chosen architecture. We submitted our result to Middlebury dataset challenge. It currently ranks as the best System on Chip solution. The system has been developed for low latency applications which require better than real time performance on high definition videos.

Index Terms—Stereo Vision, SoC, Real Time, Low Power

1 INTRODUCTION

In the past few years the demand for accurate, low latency, high definition 3D environment reconstruction has increased dramatically. Many existing applications can benefit from the addition of scene depth information. Furthermore, the existence of high quality 3D reconstruction liberates completely new use cases (e.g. Augmented Reality with occlusion handling). The output of a 3D reconstruction pipeline is usually either a 3D point cloud or a depth map (a.k.a. disparity map). These representations can be used alongside normal images to make many applications far more robust. A few use cases that can benefit from the addition of depth information are: face recognition, object count, object segmentation and autonomous driving. The fundamental requirements of these systems is to provide high accuracy at a real time frame rate (>30 fps), high resolution (>720p) and very low latency. The only way to fulfill all these requirements at the same time is to do the necessary computation on board. The only current method to reach this kind of performance using off-the-shelf solutions is to use GPU based systems. This kind of hardware, though, is not ideal for a power constrained environment (i.e. surveillance cameras in the wild). For this reason we developed a custom System on Chip (SoC) capable of achieving industry standard state of the art.

In general, there are two different classes of 3D reconstruction techniques. On class uses an “active” approach that couple an optic sensor with an optic emitter: while the emitter projects a known pattern on the scene, the sensor infer the environment from the deformation of the pattern \cite{18}. The other class uses a “passive” approach using only optic sensors for 3D reconstruction. This can be challenging and more sophisticated techniques (which requires more computation) are required. However in return, the main advantages are a lower power usage (mainly because no emitter is used) and no interference problems (mainly given by the sun light). The most established and reliable algorithms for passive reconstruction are without any doubt Stereo Vision algorithms. These techniques try to solve the stereo matching problem: given a pair of frames taken from two different twin cameras, match every pixel from the first view with a pixel from the second. Some constraints can be added to the camera positions to simplify the problem. In particular the focal axes of the two cameras are considered. In fact, if the two axes are parallel, the search for the correct pixel match is much easier. In this set up the Stereo Vision algorithm has to search for the correct match on a single line of pixels instead of the whole image. Unfortunately the perfect alignment of camera axis can only be accurate to some extent. For this reason a further process of camera calibration and image rectification is used to make sure that the epipolar lines in the two input frames are parallel. Once that the input frames are captured and rectified they are processed through a series of logical steps retrieving the 3D geometry of the scene. The output of this process is a third frame whose pixels contain information about the depth of the scene.

A taxonomy of stereo vision approaches has been described in \cite{15}. Generally speaking a classical pipeline is composed of four main stages:

- Cost Matching Computation;
- Cost Aggregation;
- Disparity Selection;
- Disparity Refinement.

In order to run the first stage (the Cost Matching Computation) we need to define the cost of the matching. Essentially we define a distance function able to compare one pixel from one frame against one from the other frame. The smaller the distance the lower the matching cost. A low matching cost means that two pixel are very similar, this similarity can be defined in many way. The most naive way is to compare the color of the two pixels. Unfortunately two pixels can have similar color but not belong to the same spot in the scene. For this reason more robust similarity functions have
been proposed. Most of these are based on sliding window approaches, where a signature is extracted from every sub-window in the image. A function that is able to map one feature vector (every value in the window) to a different feature space is called an embedding function. The most famous embedding function in Stereo Vision field is the census transform [12]. In this hand crafted technique all the pixel values in a fixed size window are compared with the value of the pixel at the center. If a pixel has a greater value than the center we place a 1 in the final binary vector, 0 otherwise, in this way a signature (also called descriptor) for every sub-window is created.

Once a cost function is defined, the Cost Matching Computation step is used to combine the two frames into a volume: each descriptor of position \((x, y)\) in the reference frame is compared with \(N\) descriptors from the target frame. The positions of the target pixels belong to the range \([x-N, y], (x, y)\). The output volume has the same height and width of the input frames and depth \(N\). The depth size has to be chosen carefully: a big value for \(N\) increases drastically the memory requirements of the volume. This volume contains the information of \(N\) comparisons for each \((x, y)\) position in the reference frame. In an ideal world the \(argmin\) of each \(N\) vector will represent the correct displacement (or disparity) for each final disparity map pixel. Unfortunately this step can be very noisy because many points can have similar a descriptor but not represent the same object, for this reason the Cost Aggregation step is fundamental to make the volume information more reliable. The values in the volume are modified using a set of specific rules and their neighboring values. Finally in the Disparity Selection step the \(argmin\) for each position \((x, y)\) in the volume is used to chose the best disparity. The Disparity Refinement step is used to increase the overall accuracy using smoothing and denoising filters. Even though standard Stereo Vision is generally performed in a passive way, it is possible to project a pattern on the scene to make the matching process more robust [11].

With the beginning of the Deep Learning era many of these steps (if not all) have been replaced by deep neural network [12], [10], [7]. This new tool in the hand of researchers has greatly increased the accuracy of the state-of-the-art approaches. The main drawback of these techniques, though, is the high demand of computational power (billions, if not trillions of operations) and memory footprints (Gigabytes of storage for each pair of frames). Such requirements are too high for efficient SoC solutions. For this reason we had to find the right trade-off between accuracy and performance. Our stereo vision module is able to deliver high accuracy disparity maps with very low latency and low power usage, the rest of the paper is divided in the following sections:

- Section 2 expands the architecture of the Stereo Vision module;
- Section 3 lists the of problems to address in order to accelerate a neural network model;
- Section 4 describes the motivation for the usage of binary descriptors;
- Section 5 shows the ablation study we used to determined the best model to use;
- Section 6 expands the quantization technique we used to compress the network;
- Section 7 and 8 shows the results and conclusion drawn.

2 The Architecture

The main difference with off-the-shelf solution is the usage of a deep learning based descriptor. It enabled the removal of the census transform module which has very well known limitations. Figure 1 shows an accurate representation of the new architecture: on the left side the Neural Network Accelerator (NNA) module is used to accelerate the computation of the neural network descriptor. The output of the NNA is then fed to the Stereo Vision Accelerator for the computation of the final disparity map. A technique that increases the robustness of a Stereo Vision algorithm is the left right consistency check: the basic Stereo Vision algorithm uses the left image as a reference frame and the right one as target. This means that the pixel from left is compared with multiple pixels on the right. There is no reason to choose one of the two frames over the other as reference or target. In fact, most of the classical approaches compute both disparity maps, left vs right and right vs left. The two disparity maps are then checked for consistency and merged together. This improves the final accuracy a lot and very easily removes random fluctuations in the disparity values. However it effectively reduces in half the frame rate of the pipeline. We addressed this problem in the stereo vision accelerator and decide to make the NNA run a single time for each
stereo pair. For the core of the accelerator we decided to go for a very basic box filter that smooths the volume values followed by the very well known Semi Global Matching (SGM) algorithm [9].

The time complexity of these algorithms is generally quadratic with the size of the images. For this reason they are not very efficient in single core systems. To increase the throughput of our solution we created a fully pipelined architecture. Once all the sub-modules fill the internal buffers (initial delay) we get an output disparity every two clock ticks (constant complexity).

3 Deep learning for Stereo Vision

Deep Learning can be used to greatly enhance the performance of a Stereo Vision pipelines. Many papers in the past few years have shown state-of-the-art results for this particular field. The first proposed technique [16] used a Convolutional Neural Network (CNN) called MC-CNN as a first stage of a classical Stereo Vision pipeline. The convolutional kernels are used in a sliding window fashion in order to obtain a 32 or 64 floating point descriptor for every sub-window. The descriptors are then compared in different way according to the modality chosen. Two versions are proposed:

- An accurate one in which another CNN is used to learn a Cost Matching function;
- A fast one that uses a simple dot product (a.k.a. cosine similarity) as the Cost Matching function between the descriptors.

Although the computational requirements are very different, the accuracy drop between the two is just around 1% on common Stereo Vision datasets. When it was first published this method has proven to be a breakthrough in the Stereo Vision community. The ability of CNN to learn new robust descriptors has increased the accuracy a lot over the previous algorithms using handcrafted descriptors. At the time of first submission both KITTI [9] and Middlebury [14] tests have ranked it among the top methods. The authors reported a run-time of less than a second for the fast architecture on a GPU.

After this outstanding result many more deep learning based approaches have been proposed. Some of these replace even more steps of the pipeline [12], while others have gone as far as learning the whole 3D reconstruction function end-to-end. We can find example of both passive [10] and active [7] methodology.

3.1 At the edge acceleration

In the past few years a lot of new at-the-edge hardware accelerator have been presented both by the academic world [3, 5] and industries [2, 3, 1]. For our Stereo Vision solution we use the neural network accelerator already present in the chip, namely the NNA. A critical limitation for all embedded devices is the resources available: principally the computational capabilities and memory size. Strictly speaking, the main limitation for CNN accelerators is the quantity of fast memory available to the processor. While a DDR like memory would be big enough to store whole neural network models and their respective feature maps, a cache-like fast-access memory is usually very small in size, in the best cases around the Megabytes order. This may represent a problem for a pipelined architecture that needs to be full the whole time to avoid reduction in efficiency.

Let’s take a closer look at the fast architecture proposed in [16] (by far one of the leanest). The main CNN is a very shallow network composed of only four convolutional layers Table [1]. Since every layer has a 3x3 kernel the final receptive field is 9x9. The final output of the convolution is a feature map that has more or less the same resolution of the input (not considering padding) and 32 channels for each element. Essentially 32 floating point numbers are extracted from each 9x9 patch of the input frame. For this reason there is no constraint on the input resolution and can be changed at will during inference time. With these basic considerations we can see that the memory and computation required by this simple network is proportional to the size of the input resolution.

Usually the neural network accelerator uses its fast-access memory to store both the weights of the model and the intermediate feature maps. Even though the model is very shallow the amount of weights to store is:

$$\#weights = 1 * 32 * 3 * 3 +$$
$$32 * 32 * 3 * 3 +$$
$$32 * 32 * 3 * 3 +$$
$$32 * 32 * 3 * 3 = 27,936$$

If we do not consider any compression technique we may need to store up to 112KB of floating point numbers (float32). Although these figures seem reasonable the main problem with the four layers model is the memory required to store the intermediate feature maps. Even if we assume that we keep in memory the output of each layer at a time we have to store a feature map that can be as big as 1280 * 720 * 32 = 29.5 * 4Byte = 118 MB (again using float32 numbers). This amount is definitively too much for a fast-access (cache-like) memory that is accessed by the neural network accelerator.

Besides the memory problem we have also to consider the actual amount of operations required to process a single frame. The metric that is generally used to profile the amount of operation required by a CNN is the number of FLoating point OPerations (FLOPs), practically speaking the number of multiplication to perform on the input and intermediate feature maps in order to obtain the output, for a single layer we have:

$$\#FLOPs = ch_{in} * ch_{out} * k^2 * input_w * input_h$$

were $ch_{in}$ and $ch_{out}$ are respectively the number of input and output channel, $k$ is the size of the kernel and $input_w$ and $input_h$
and \( \text{input}_h \) are the width and height of the input feature map. Let’s consider the CNN used in [16] and a 720p HD input frame (i.e. 1280 x 720): we have four layers with input and output channels equals to 32 (except for the first input channel which is 1), all together:

\[
\#FLOPs = 1 \times 32 \times 9 \times 1280 \times 720 + \\
32 \times 32 \times 9 \times 1280 \times 720 + \\
32 \times 32 \times 9 \times 1280 \times 720 + \\
32 \times 32 \times 9 \times 1280 \times 720 = 34 \times 10^9
\] (2)

This result has to be further multiplied by the number of frames per second we want to obtain. No embedded hardware accelerator in the market can reach this kind of performance. For this reason we searched for an even smaller architecture.

The second problem to address is the complexity of the comparison function used for the descriptor. In the original fast architecture the cosine similarity is used. This function is not really hardware friendly (a lot of multiplications and divisions have to be performed). For this reason we decided in favor of a binary descriptor. These kind of descriptor are much more compact and can be compared with a distance function as efficient as the hamming distance.

Finally the third problem to address is the computational demand of floating point multiplications. All the current at-the-edge hardware accelerators do not encourage the usage of floating point multiplication. In fact, it has been shown that 8bit quantization can be used to fully replace full precision model with very low loss [4], [13]. This not only decreases the footprint of the model in the memory but it also allows the usage of smaller and much more efficient 8 bit multiplier.

4 Binary Descriptors

The first challenge we faced is the replacement of the floating point descriptor with binary ones. For this reason we took [13] code-base and replaced the cosine similarity with hamming distance. Since quantization loss is to be expected we did different experiments to check how much the accuracy drops with a decreasing number of bits. What we discovered is that even using a single bit for each float number the accuracy of the output does not decrease too much.

The way we quantize a float number into a single bit is straightforward, we simply threshold its value on zero, if the original number is bigger we set the bit to 1, 0 otherwise. We also tried to use the mean value for each output channel as a threshold but we found no improvement respect to a simple threshold on zero. Instead of 32 float feature vector (one for each output channel) we end up with an array of 32 bits. These are then compared in the Cost Matching Computation using hamming distance. The accuracy drop we got on KITTI dataset is very small, testing for KITTI error metric T3 (all the pixel with a disparity value more wrong than 3 from the ground truth) the figures increased from 4.875% to 4.887%. In this way the bandwidth between the two modules decreases 118MB per frame to only 3.6MB per frame.

In Figure: it is shown the actual difference between the two results using different distance functions, the two functions give very similar results as long as the rest of the pipeline remains the same.

5 Ablation Study

We explored different variations of the network in Table: [1] We first tried to decrease the number of input and output channels in different combinations of four and eight, with the only exception for the last layer which still remains 32 since we want a 32 bit descriptor. We choose four and eight mainly because the addressing and the scheduling for these values its very hardware friendly. This reduces drastically the number of FLOPs required by the network. Unfortunately the main problem with a multilayer network is the necessity to store the intermediate feature maps during the computation. Since in this use case the amount of memory is proportional to the resolution of the input image, it is very challenging to find a solution for this particular problem. To satisfy the trade off between performance and accuracy we had to make big cut on the computational budget to allow a better data flow. We decided in favor a final model with a single layer network that has 32 kernel of 9x9 size, in this way the receptive field is kept constant respect to the original model. Ablation studies were also performed in [16] in subsection Hyperparameters, but it must be noticed that a bigger kernel size has not been tested. The usage of a single layer allows for on-the-fly computation: i.e. we don’t have to wait for the whole frame to be completely processed. Essentially we can start to send binary descriptors as soon as we process 9 lines of inputs. Our experiments have shown little degradation in the final accuracy. In Figure: [3] it is shown the difference between the original MC-CNN and the single layer one. The front end (cost computation,
In the table are shown three different network topologies, the top row represents the original architecture from [16]: four layers with 32 channels each. The middle row is the smallest four layers network we tried, the bottom row is the single layer network with the input of one channel and output of 32. The dataset used is MiddleburyV3 Quarter resolution. The metrics in the columns are respectively: the Fill Factor (which indicates the amount of non invalidated pixel), the TX metrics (which shows the percentage of disparities more wrong than X), the FX.X scores (which have the classical definition).

| Kernel size: 3x3 | Fill_Factor(%) | T0.125(%) | T0.25(%) | T0.5(%) | T0.75(%) | T1(%) | T2(%) | T4(%) | F0.5 | F0.75 | F1.0 |
|------------------|----------------|-----------|-----------|---------|----------|-------|-------|-------|------|-------|------|
| Ch.: 1,32,32,32  | 93.111         | 77.721    | 59.493    | 37.433  | 22.175   | 14.703| 11.391| 0.951 | 0.96  | 0.968  |      |
| Kernel size: 3x3 | 92.124         | 78.169    | 60.56     | 38.925  | 29.169   | 24.224| 16.67 | 13.113| 0.942 | 0.953  | 0.963 |
| Ch.: 1,4,4,8,32 | 91.692         | 78.384    | 61.587    | 40.949  | 31.268   | 26.093| 18.118| 14.178| 0.935 | 0.947  | 0.958 |

TABLE 2

In Table 3 Final result on MiddEval3 evaluation tool.

|       | bad2.0 % | invalid % | tobad % | avgErr |
|-------|----------|-----------|---------|--------|
| four layer | 16.226   | 10.95     | 27.178  | 3.819  |
| single layers | 17.39    | 11.50     | 28.89   | 4.202  |

FIG. 3. Visual difference between MC-CNN (top) and the single layer (bottom) network accuracies. The two results are very similar, this shows how much the front end of the system is resilient to the neural network changes.

Cost aggregation, etc...) has been kept the same for both experiments. The smaller network does not degrade the accuracy dramatically and it keeps the overall metrics to an acceptable level, in Table 2 a summary is shown.

The four metrics reported by the MiddEval3 evaluation tool are very close to the one used for the middlebury ranking. We have: “bad2.0” which measure the percentage of disparities that are at least 2 units wrong (the lower the better), “invalid” which measures the number of disparities not set by the algorithm (the lower the better), “totbad” is the total number of bad pixel (the lower the better), “avgErr” measures the distance between each predicted disparity and the ground truth (the lower the better) (Table 3).

In the end the number of FLOPs required to process a whole frame falls from $34 \times 10^9$ to a mere $265 \times 10^6$. This can be handled by our accelerator at 55 fps using only 10% of its resources.

6 THE QUANTIZATION TECHNIQUE

All the work we did to search for a smaller network is useless if we don’t quantize its weights and features maps. For this reason we come out with the following quantization methodology, it is quite generic and works very well with shallow model like the ones we studied. We define the original model (the one to quantize) as composed of a sequence of L convolutional layer and activation layer: $\text{model}[\Gamma_1...\Gamma_L]$, where $\Gamma_l$ indicate the l-th convolution and $W_l$ and $B_l$ are respectively its weights and biases. The procedure we suggest is a serial one in which we quantize the weights and biases one layer at a time. Quantizing a convolutional layer basically means remap all the floating point weights and biases into a smaller quantized interval. The obtained set of values is indicated by $\hat{W}_l$ and $\hat{B}_l$, this new convolutional layer is defined using $\hat{\Gamma}_l$ (Fig 4). The quantization interval in this case is given by the capability of our platform, i.e. 7 bits plus 1 sign bit ($\text{int}8$). A naive approach would be to spread the weights into the interval $[-128, +127]$ as much as possible, this approach doesn’t give good results if the weights are not evenly distributed in the float range, e.g. if the absolute value of one of the weight is 10 times bigger than the rest. In this case the smaller weights would be quantized in the same bin. This would increase the quantization loss a lot. For this reason it is necessary to make an exhaustive search for the best division factor. Luckily, this procedure has to be performed just once in a batch manner, so the run-time is not a critical factor at this stage.

Generally speaking, the weights and biases of a convolutional layer are floating points in a narrow range (e.g. $[-1.0, 1.0]$), converting them to 8 bit signed values means rescaling this interval to $[-128, 127]$. We define the scale factor $S_l \in \mathbb{R}$ as the factor used to scale the weights from...
floating point to integer at layer $l$. The scaling is performed in the following way:

$$
\hat{W}_l = \text{round} \left( \frac{W_i \cdot S_l}{\tau} \right) = R_{S_l}(W_i)
$$

$$
\hat{B}_l = \text{round} \left( \frac{B_i \cdot S_l}{\tau} \right) = R_{S_l}(B_l)
$$

Where the round function simply rounds to the nearest integer and $\tau$ is the upper limit of our interval (e.g. 127). Since $\tau$ is constant for the whole process of quantization we can redefine $S_l$ to encompass it:

$$
\hat{S}_l = \frac{S_l}{\tau}
$$

If we now consider the input $x$, we can say that:

$$
\hat{S}_l \cdot (W_i \cdot x + B_l) \approx \hat{W}_l \cdot x + \hat{B}_l
$$

$$
\hat{S}_l \cdot \Gamma_l(x) \approx \hat{\Gamma}_l(x)
$$

Where $\hat{\Gamma}_l$ is the new symbol that defines the convolution operation at layer $l$ multiplied by $\hat{S}_l$. As you notice it is necessary to multiply the original output by the scale factor $\hat{S}_l$ to make the approximation symbol meaningful.

This approximation problem which would have been relatively easy to solve if we had only continuous function, becomes intractable in this case since the round operator is introduced. Such a problem is of Integer Programming Optimization, which is NP-Complete. This kind of complexity can be tackled only with exhaustive search algorithm or sub-optimal optimizer. We chose the first option since the sub-optimality can be tackled only with exhaustive search algorithm or sub-optimal optimizer. We chose the first option since the step is “small enough”, good results can be obtained. Finally we can redefine our optimization problem:

$$
\text{arg min}_{\hat{S}_l} \left[ \text{Dist}(\Gamma_{\hat{S}_l}, \hat{\Gamma}_l, X) \right]
$$

Since $\hat{S}_l$ has to be positive and for $\hat{S}_l$ bigger than the maximum weight there is always a big loss in quantization, we can define the search range in $(0, \text{max}(W_i))$, with a step-search it is possible to obtain good results. In our experiments we found that if the step is three order of magnitude smaller ($< 10^3$) than max$(W_i)$ we can safely assume that the search was exhaustive enough.

### 6.1 Quantization loss

There are different way to define (5) but the main problem is that each $S_l$ has to be tested for all possible input $X = \{x_1...x_n\}$. According to [13] to speed up the quantization loss evaluation process it is more practical to compare the histogram of the activation instead of the actual value. Good results are claimed to be obtained for the quantization loss function called Kullback-Leibler (KL) Divergence:

$$
D_{KL}(H \parallel \hat{H}) = \sum_i \log_2 \left( \frac{H_i}{\hat{H}_i} \right) H_i
$$

Where $H$ and $\hat{H}$ are two discrete distributions which in our case are modelled upon the histograms obtained from the left and right side of (4). In our experiment we also tested the classic Root Mean Square Distance ($D_{RMS}$) between each respective bin:

$$
D_{RMS}(H, \hat{H}) = \frac{1}{n} \sum_i \sqrt{(H_i - \hat{H}_i)^2}
$$

No relevant differences have been noticed using the two functions.

These approaches, though, rely on an important assumption: the more similar the histograms the smaller the quantization loss. This is not always true since two outputs could switch position in the histogram bin at the same time preserving the histogram shape even when the quantization function has made mistake. For this reason in our work we check the actual relation between input and output before and after the quantization. With these premises, equation (7) becomes:

$$
RMS \left( \Gamma_{\hat{S}_l}, \hat{\Gamma}_l, X, \hat{X} \right) = \frac{1}{n} \sum_{x_i, \hat{x}_i \in X, \hat{X}} \sqrt{(\Gamma_{\hat{S}_l}(x_i) - \hat{\Gamma}_l(\hat{x}_i))^2}
$$

Where $\hat{X}$ represents the quantized activation coming from the previously quantized layer. Using this instead of the original output allows to recover from previous error. For this reason, sometimes, during the quantization process, it is possible to see that the quantization loss decreases layer after layer. As an alternative the norm $\ell_1$ can be used:

$$
\ell_1 \left( \Gamma_{\hat{S}_l}, \hat{\Gamma}_l, X, \hat{X} \right) = \frac{1}{n} \sum_{x_i, \hat{x}_i \in X, \hat{X}} |\Gamma_{\hat{S}_l}(x_i) - \hat{\Gamma}_l(\hat{x}_i)|
$$
In our model we are going to compare binary descriptors. We check the final quantization loss using the sign of the outputs. To compute the quantization loss we used hamming distance:

\[
HD\left(\Gamma_{\hat{S}_i}, \hat{\Gamma}_i, X, \hat{X}\right) = \sum_{x_i \in X, \hat{x}_i} \text{sign}(\Gamma_{\hat{S}_i}(x_i)) \oplus \text{sign}(\hat{\Gamma}_i(\hat{x}_i))
\]

Where the \text{sign} function returns the actual sign of the output activation and then a \(\oplus\) (XOR) returns 1 if the the two values have different sign, 0 otherwise.

6.2 Channel-Wise Quantization

If the hardware allows to set a different scale factor for each output channel of the convolution, it is possible to perform a channel-wise quantization. Allowing a different scale for each output channel can reduce the quantization loss. A different mapping for each channel onto the int8 range involves the post re-scaling of each component in order to make the input activation compatible with the weight of the next layer. Let \(N\) be the number of output channels of a convolutional layer \(l\). Starting from (4) it is possible to redefine the problem for channel-wise quantization:

\[
\begin{align*}
&\hat{S}_i = \{\hat{S}_i^1, \ldots, \hat{S}_i^N\} \\
&W_i = \{W_i^1, \ldots, W_i^N\} \\
&B_i = \{B_i^1, \ldots, B_i^N\}
\end{align*}
\]

\[
\forall i \in [1\ldots N] \left\{ \begin{array}{l}
\hat{S}_i^l \cdot \left( W_i^l \cdot x + B_i^l \right) \approx \hat{W}_i^l \cdot x + \hat{B}_i^l \\
\hat{S}_i^l \cdot \hat{\Gamma}_i^l(x) \approx \hat{\Gamma}_i(x) \\
\hat{\Gamma}_i(x) \approx \hat{\Gamma}_i^l(x)
\end{array} \right.
\]

At this point we can define Algorithm 1 to quantize a single convolutional layer in a channel-wise manner.

6.3 Quantize Activation

Multiplying and accumulating int8 values produces very large values in output (e.g. int32), and since the activation output of a layer has to be given as input to the next layer, it is necessary to re-scale the values to int8 range. Essentially, what we do after the forward pass is to reconstruct the original value of the feature map with the lowest possible quantization loss. Starting from (4) we get:

\[
\begin{align*}
&\hat{\Gamma}_i(x) \approx \hat{\Gamma}_i^l(x) \\
&\hat{S}_i \cdot \hat{\Gamma}_i(x) \approx \hat{\Gamma}_i(x) \\
&\Gamma_i(x) \approx \hat{\Gamma}_i^l(x) \\
&\Gamma_i(x) \approx \hat{\Gamma}_{\hat{S}_i^l}(x)
\end{align*}
\]

Since this re-scale process is applied during the forward pass it is necessary to find an efficient way to perform the division by the \(\hat{S}_i\) factor(s). Generally speaking, a multiply-shift operation is more efficient to perform compared to a division operation, especially if the multiply factor \(m\) and the shift factor \(h\) are integers instead of floats:

\[
\hat{S}_i \hat{\Gamma}_i(x) \approx (\hat{\Gamma}_i(x) \cdot m) >> h
\]

\[
\hat{\Gamma}_{\hat{S}_i^l}(x) \approx \hat{\Gamma}_i^l(x)
\]

Where \(\hat{\Gamma}_{m,h}\) indicate the multiply-shift operation performed after the quantized convolution at layer \(l\) (\(\hat{\Gamma}_i\)). For this reason we optimize the following problem:

\[
\begin{align*}
&Q(\hat{\Gamma}_{\hat{S}_i^l}, \hat{\Gamma}_i^l, m, h, x) = \\
&\left| \hat{\Gamma}_{\hat{S}_i^l}(x) - (\hat{\Gamma}_i(x) \cdot m) >> h \right|
\end{align*}
\]

\[
\begin{align*}
&\arg\min_{m,s} \{Q(\hat{\Gamma}_{\hat{S}_i^l}, \hat{\Gamma}_i^l, m, s, x)\} \\
&Q(\hat{\Gamma}_{\hat{S}_i^l}, \hat{\Gamma}_i^l, m, h, i, x) = \\
&\left| \hat{\Gamma}_{\hat{S}_i^l}(x) - (\hat{\Gamma}_i(x) \cdot m) >> h \right|
\end{align*}
\]

Which, again, can be cast to the channel-wise quantization domain in the following way:

\[
\begin{align*}
&Q(\hat{\Gamma}_{\hat{S}_i^l}, \hat{\Gamma}_i^l, m, h, s, i, x) = \\
&\left| \hat{\Gamma}_{\hat{S}_i^l}(x) - (\hat{\Gamma}_i(x) \cdot m) >> h \right|
\end{align*}
\]

Where now \(m\) and \(h\) are two arrays containing one value for each channel \(i\).

Since \(m_i\) and \(s_i\) are integer in a very limited range (e.g. \([0, \ldots, 2^8 - 1]\)), it is not hard to check for the best pair that optimize (12). If we take the example of ReLU\_127 (a ReLU with a clamping threshold of 127), the codomain of (12) is limited in \([-128, +127]\). It is very easy to check which is the combination that gives optimal solution (0 error). For this reason we implemented Algorithm 2.
Table 4

| Kernel size: 9x9 | Ch: 1,32 | Fill | Factor(%) | T0.125(%) | T0.25(%) | T0.25(%) | T0.5(%) | T1(%) | T2(%) | F0.5 | F0.75 | F1.0 |
|-----------------|---------|------|-----------|-----------|-----------|-----------|----------|--------|--------|------|-------|------|
| Quantized       |         | 91.692 | 78.384 | 61.587 | 40.949 | 31.268 | 26.093 | 18.118 | 11.2 | 29.6 | 31.35 |

Accuracy drop due to the quantization loss in the single layer network. The dataset used is Middlebury V3 Quarter resolution.

Function quant_act \((\hat{\Gamma}_{S_i}, \hat{\Gamma}_i, \hat{X})\):

\[ m = \{m_1, ..., m_{N_l}\} \]
\[ h = \{h_1, ..., h_{N_l}\} \]

for \(S_i \in S\) do

for \(M = [0, ..., 2^z - 1]\) do

for \(H = [0, ..., 2^z - 1]\) do

if \(Q(\hat{\Gamma}_i, \hat{\Gamma}_{M,H,i}, \hat{X}) < \min\) then

\[ \min = Q(\hat{\Gamma}_i, \hat{\Gamma}_{M,H,i}, \hat{X}) \]
\[ m_i = M \]
\[ h_i = H \]

end

end

end

Return \(m, h\)

Algorithm 2: Procedure to quantize the activation

Depending on the activation function (ReLU, Sigmoid, Tanh, ...) different scaling can be applied. With ReLU there are not many problems since we minimize the difference between non-quantized and quantized output, this means that positive values will stay positive and vice-versa, if the value is close to 0 the activation will be not dramatically changed. A different challenge is for Sigmoid and Tanh which have a narrow non-saturation interval, scaling this interval proportionally to \(S\) solves the problem. After that the activation and scaling is applied, the big values are again in int8 format.

6.4 The algorithm

At this point we can put all together, quantizing one layer at a time, the convolution and then the activation, it is possible to obtain very close result even if we scaled from float to int8.

Function Quantization(model[\(\Gamma_1, ..., \Gamma_L\)], \(X\)):

\[ \hat{X} = X \]

for \(\Gamma_i \in \text{model}[\Gamma_1, ..., \Gamma_L]\) do

\[ \hat{\Gamma}_i = \text{quant.conv}(\Gamma_i, X, X) \]
\[ \hat{\Gamma}_{m,h} = \text{quant.act}(\hat{\Gamma}_{S_i}, \hat{\Gamma}_i, \hat{X}) \]
\[ X = \Gamma_i(X) \]
\[ X = \hat{\Gamma}_{m,h}(X) \]

end

Return model[\(\hat{\Gamma}_{m,h}^1, ..., \hat{\Gamma}_{m,h}^L\)]

Algorithm 3: Procedure to quantize the activation

As you can see in Algorithm 3 the input is forwarded through the original network as a reference. The final metrics reported for the chosen quantized network are shown in Table 4.

7 RESULTS

We finally compare our solution with the state-of-the-art approaches, for this reason we submitted our disparity maps to the Middlebury ranking. Currently our method ranks half way of the ranking and it is the first among all the ASICs. In Table 5 are shown the metrics we obtained:

The ranking measures a lot of metrics for different setup, the main difference between the setups is what it is considered for evaluation: we have a setup that considers only the non occluded pixel in the ground truth (nonocc) and one that considers all pixels. Furthermore the testing tools try to evaluate the metrics with the original results (sparse) and with a cleverly filled version (dense). Since the algorithm is capable of subpixel resolution also bad0.5 is shown. This one counts the percentage of disparities that are more wrong than 0.5 units of disparity. For a more comprehensive summary refer to Figure 5.

7.1 Performance

Since the architecture is divided in two main modules we must distinguish between the performance of the NNA and the SVA. The NNA will only run the trained CNN, this module has to process the two frames coming from the cameras. For parallelism reasons the NNA is composed of 10 submodules, using one of this submodule it is possible to process 55 frames with 720p resolution \((1280 \times 720)\). Using only two submodules it is possible to reach more than real time performance. The SVA instead is far more efficient. It can process up to 250fps in left-right check mode. Practically speaking the module can be used for multiple camera pairs at the same time. This differentiation makes different use cases possible. While it is true that we might have the whole NNA and SVA processing stereo pairs of frame, we can also use a part of the NNA to process a single disparity map and use the rest of the NNA to accelerate a deep learning based recognition algorithm.

8 CONCLUSION

The accuracy and performance given by our new architecture of passive Stereo Vision system is increased as never
seen before in the market. Deep learning descriptors combined with a classical methodology gives an extra boost to the accuracy of the 3D reconstruction. Future development will try to make the architecture even more robust and efficient.

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