Research on Low Power Design Technology of HPLC

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Abstract. Power line communication (PLC) is widely used in electric power Internet of Things (IoT). Its performance, including data rate and anti-interference ability, has made great breakthroughs from Narrowband PLC (NB PLC) to high-speed PLC (HPLC) in recent years. In the context of continuously improving functions, the power consumption of HPLC is gradually increasing, this is equivalent to increasing the line loss of power transmission, which has an adverse effect on the large-scale deployment of HPLC. This paper analyses the structure of HPLC chip and communication unit, mainly exploring the low power design technology from chip architecture design, frequency band selection, physical layer (PHY) design, and MAC layer process. Currently the latest HPLC chip has been developed successfully, and the corresponding communication unit have started large-scale applications, and lab test and field application results show the HPLC can well meet the power consumption requirements in electric power IoT.

1. Introduction
PLC refers to a communication method that uses power lines to transmit data and media signals. Owing to the advantage of convenient deployment of power line infrastructure, PLC has been widely applied in the local communication of the electric power IoT. Power line endures substantial noises, attenuations, and frequency selective fading, and there are apparent differences of the distribution grid characteristics between at home and abroad [1], moreover, the existing NB PLC[2-3] technology cannot meet the increasing bandwidth requirements of bi-directional interactive services in smart grid[4], therefore, State Grid has developed its own HPLC technology [5].

Compared with NB PLC, HPLC has obvious advantages in communication speed and anti-interference ability. However, the increase in bandwidth and speed also brings an increase in power consumption. Considering that there are more than 500 million electric meters in China, the total power loss is very large, at the same time, the power supply capacity of the equipment installed with the HPLC communication unit is also very limited, all these have brought great challenges to the low power design of HPLC.

2. Power Consumption Requirements and Composition

2.1. Power Consumption Requirements
The State Grid has specially formulated low voltage power line broadband communication interoperability technical specification [5], which has very clear requirements for the power consumption of HPLC communication unit, as shown in Table 1.
Table 1. Communication unit power consumption requirements

| Local communication unit type | Static power | Dynamic power |
|------------------------------|--------------|---------------|
| Single phase electricity meter | ≤0.4W        | ≤1.5W         |
| Three phase electricity meter | ≤0.8W        | ≤2.5W         |
| Concentrator                | ≤1W          | ≤6W           |

At the same time, the State Grid is working to formulate HPLC and radio frequency (RF) dual-mode communication technical specifications. The power consumption requirements of the dual-mode must be the same as HPLC. This also brings higher requirements to the low power design technology of the latest HPLC design. In practical applications, more than 95% of the communication units are used in single phase electricity meters, and the power consumption requirements are also the most stringent, so it will be the focus of this paper.

2.2. Power Consumption Composition

HPLC is baseband communication system, and it is composed of digital circuits and analog circuits. The digital circuit transistor works in the cut-off region and the saturation region. As shown in formula (1) [6], its power consumption is composed of dynamic power \( P_D \), short-circuit power \( P_S \) and static power \( P_L \), influencing factors include load capacitance \( C \), power supply voltage \( V_{DD} \), operating frequency \( f \), switching coefficient \( N \), short-circuit charge \( Q_{SC} \) and leakage current \( I_{leak} \).

\[
P = P_D + P_S + P_L = 0.5CV_{DD}^2fN + Q_{SC}V_{DD}fN + I_{leak}V_{DD}
\]  

The analog circuit is difficult to define the power consumption composition like the digital circuit. The analog circuit transistor works in the linear amplification area, and an appropriate bias voltage (or current) needs to be set. When it works in the sub-threshold mode, the power consumption can be greatly reduced. In addition, the analog module usually provides a low power shutdown or sleep mode, which can be controlled by a digital circuit or processor.

3. HPLC Chip and Communication Unit Design

3.1. HPLC Chip Design

As shown in Figure 1, and HPLC baseband chip is a typical SoC and it adopts AHB/APB two-level bus structure. The AHB bus uses a high efficiency and low latency matrix structure. The AHB masters includes CPU core, MCU core (a lightweight processor reserved for dual-mode and extended applications), DMA, HPLC MAC hardware accelerator (PLC MAC HW), and HPLC PHY accelerator. The AHB slaves include PSRAM controller, BootROM, QSPI Flash controller, and AHB2APB bridge. APB peripherals include UART, Timer, PWM, GPIO, SPI controller, ethernet interface (SPI EMAC), and system control unit (SCU). In addition, HPLC also integrates a high performance analog front end (AFE), and the AFE includes ADC, DAC, band pass filter (BPF), and programmable gain amplifier (PGA).
3.2. Communication Unit Design

HPLC communication unit (single phase electricity meter) is shown in Figure 2, and is mainly composed of HPLC chip, Line Driver, board level RLC BPF, and a transformer. HPLC chip and Line Driver are two core ICs. Line Driver is used to amplify the analog signal sent, and the highest output voltage is above 12V. It usually adopts a bipolar process which is quite different with CMOS process of HPLC chip. Line Driver has a large power consumption, and it is directly related to the signal power spectral density (PSD). The State Grid has strict regulations on PSD, and in-band PSD and out-of-band PSD are not larger than -45dBm/Hz and -75dBm/Hz respectively [5]. To reduce the Line Driver power consumption, HPLC can reduce bandwidth and transmission power, but it will bring a drop in data rate and communication distance. Therefore, a comprehensive trade-off is required in standard development and field application.

4. HPLC Low Power Design

4.1. Working Frequency Band

Broadband PLC(BPLC) such as IEEE1901 and ITU-T G.hn (1.8-30 MHz) is applied in short distance indoor environment, while HPLC is used in outdoor scenes, pay more attention to communication distance and power consumption, however, the average PHY data rate of 10Mbps can meet all needs.
of the application in electric energy data acquisition system[7], so working frequency band can be greatly reduced compared with BPLC. HPLC selects medium frequency 780KHz -12MHz as the basic frequency band. The medium frequency avoids faster attenuation of high frequency and larger noise of low frequency where the NB PLC works, which improves PHY communication distance. The HPLC uses the similar orthogonal frequency division multiplexing (OFDM) technology to IEEE P1901 FFT PHY layer. Due to the narrower bandwidth, 1024-point FFT with 24.414KHz subcarrier space is adopted, so sampling rate ($F_s$) is only 25MHz, and it can be further reduced to 12.5Msps in small bandwidth mode, which is several times lower than the IEEE P1901 sampling rate (75Msps or higher). The lower sampling rate with lower-order modulation can make HPLC SoC and PHY work at a lower clock frequency ($\leq 4$ times $F_s$ clock), and greatly reduce performance requirements of AFE and Line Driver, thereby reducing the cost and power consumption.

4.2. Chip-level Low Power Design
HPLC chip uses an advanced 40nm low power process with low dynamic power consumption. Due to lower clock frequency, the chip can use high-threshold standard cells and low leakage SRAMs in most circuits, which effectively reduces static power consumption. The chip adopts a fully synchronous design with low read/write latency, but the clock ratio between the CPU, bus and peripherals can be dynamically adjusted according to the working scenario and performance requirement, which helps to reduce power consumption of non-core modules and non-critical paths. In the memory architecture, the SDRAM with many pins and high-power consumption in the previous design[8] is removed and replaced by a high-speed QSPI Flash and a large-capacity on-chip SRAM solution. At the same time, considering that the concentrator communication unit requires a larger program and data space, the chip provides an extension interface for PSRAM. QSPI Flash adopts SIP(System-In-Package) package solution, which can reduce IO load capacitance, thereby reducing dynamic power consumption generated by charging and discharging when IO toggle. SRAM adopts a multi-bank combination, but usually only one bank is activated at a time, and other banks are in a low-power standby state, which can effectively reduce the dynamic power consumption.

4.3. PHY Low Power Design
As shown in Figure 3, HPLC PHY is a time division duplex link, including a transmission path (TX) and a reception path (RX). Both TX and RX are composed of a digital baseband and AFE.

![PHY block diagram](image)

Because power line is a shared medium, coupled with the burst transmission of the PLC, this is very beneficial for low power control. HPLC PHY defines four main working states: sending, carrier sense, receiving and standby. The sending state is initiated by the processor when the channel is idle, RX is closed during sending, and TX is opened for sending. When not transmitting, PHY is usually in the carrier sense state. At this time, the time domain processor of the RX is in the working state, and the frequency domain and bit-level processor are turned off. When the received signal strength (energy detection) is higher than the threshold or detecting the carrier (preamble detection), PHY will switch to the receiving state. When receiving, the TX is closed and the RX is working. After the reception is completed, the RX will also be closed. After a inter frame space (IFS) turnaround, PHY will switch to the sending or carrier sense state. The standby state is a special low-power state, in this state, the entire
PHY is shut down, and the upper layer protocol also stops processing. After a specific timer overflows or a peripheral interrupt arrives, it goes to the sending or carrier sense state.

Both TX and TX use a pipeline structure. The output of the previous stage is used as the input of the next stage to promote the processing of the next stage. Therefore, the clock gating driven by the data stream can be used to dynamically open and turn off module clock during implementation to reduce power consumption of TX and RX. In frame synchronization, in order to obtain good correlation performance, a cross-correlation algorithm is adopted. Considering the long preamble symbol of power line communication, frame synchronization will intercept a sequence with the most significant correlation in the 1024-point SYNCP sequence as a local cross-correlation sequence (short sequence), and use a binary exponential notation to perform correlation operations. Under ensuring the correlation performance, the complexity of the correlation operation (multiplication and addition) can be significantly reduced, thereby greatly reducing the circuit area of frame synchronization and the power consumption in the carrier sense state.

Because the signal attenuation changes greatly in power line channel, RX AFE needs to have a large dynamic range, but PGA works in the high-voltage domain (3.3V), and a large gain PGA requires a multi-stage amplification structure, which will bring higher power consumption. Considering that the ADC works in the low-voltage domain (1.1V), and the noise in the harsh power line environment is usually relatively large, RX AFE uses a architecture that combines a PGA with a relatively small gain range and a high-precision ADC to obtain a better balance between power consumption and performance. In addition, A digital gain amplifier circuit is added to the RX AGC to ensure that the subsequent time-frequency domain processing signal remains within a reasonable dynamic range, thereby ensuring the sensitivity of the RX. The power consumption of the TX is mainly in the Line Drive. A dedicated Line Driver with high power conversion efficiency is necessary, and HPLC will periodically measure the channel attenuation and impedance between the neighbour nodes to dynamically adjust the power amplification of the Line Driver. In addition, Line Drive can enter a low power sleep state when no sending.

4.4. MAC Layer Low Power Design

After the PHY correctly decodes the frame control (FC) of the MPDU frame, as shown in Figure 4, the MAC layer can determine the length of the frame transmission or the single frame transmission with/without acknowledgement according to the frame length, the number of physical blocks, and the number of symbols in the FC. The interaction duration, combined with the accurate timing information provided by the timing/frame synchronization module, can accurately calculate the time of the subsequent IFS. During the IFS, the PHY can be directly enter standby.

4.4. MAC Layer Low Power Design

HPLC networks is a tree-shaped network with Central Coordinator (CCO) as the center and Proxy Coordinator (PCO) as the relay agent, connecting all Stations (STA) with multi-level associations. After entering the network, the HPLC can identify its own role according to the network topology and its own node location. If it is an STA, it means that the station is the end node of the HPLC network. After receiving the MAC frame, it can quickly parse the MAC frame header. If the destination address of the MAC frame is not the STA, the STA can directly discard the MAC frame and quickly enter the standby state.

HPLC uses a channel access mechanism that combines CSMA/CA and TDMA. Its time slots are divided into beacon time slot, CSMA time slot, TDMA time slot and bind CSMA time slot, and each
time slot is divided into 3 time slices for A, B, C three-phase lines respectively. The CCO needs to process 3 time slices, but PCO and STA only needs to keep active in its specific phase time slice according to the phase recognition result after joining the network, so PCO and STA can use sleep mode and timing wake-up mechanism to reduce power consumption, and there are almost 2/3 of the time in sleep mode.

5. Power Consumption Test

In the static power consumption test, there is only one STA in the whole test environment, the STA is in a non-communication state, and the STA receiver is basically in the carrier sense state, but it should be ensured that once a valid HPLC PPDU (PHY Protocol Data Unit) signal is detected, the STA should quickly enter the receiving and sending state, therefore, the STA cannot be completely in the standby state. Static power consumption is qualified by average power consumption. The dynamic power consumption test uses a CCO and a STA to setup a one-to-one network, and then periodically perform the meter reading test. An attenuator is used to simulate channel attenuation between CCO and STA, and a Spectrum Analyzer is connected to the power line on the STA side to measure the PSD, and ensure that in-band and out-of-band PSD meets the requirements of the State Grid. Dynamic power consumption mainly focuses on peak power consumption. The test results are shown in Table 2. Compared with the previous design[8], power consumption has an obvious improvement.

Table 2. Power consumption test result

| Test item       | Power requirement | Test value[8] | Test value |
|-----------------|-------------------|---------------|------------|
| Static power    | ≤0.4W             | 0.38W         | 0.25W      |
| Dynamic power   | ≤1.5W             | 0.86W(TX)     | 0.75W(TX)  |

*Test result is based on 12V power supply and measured current.

6. Conclusion

By adopting a variety of low power design technologies at different levels, HPLC power consumption is controlled at a lower level. Currently, HPLC has been mass-produced and entered large-scale field applications. The application results show that HPLC has obvious advantages in meter reading speed and success rate compared with NB PLC. While maintaining a larger transmission distance and lower cost, its static and dynamic power consumption also fully meets the requirements of the State Grid and has a large margin, which has important significance for accelerating large-scale deployment of HPLC and the evolution from HPLC to dual mode, and improving the level of communication technology and comprehensive service capabilities of electric power IoT.

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