Analysis On Power Gating Circuits Based Low Power VLSI Circuits (BCD Adder)

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Abstract. Currently, energy consumption in the digital circuit is a key design parameter for emerging mobile products. The principal cause of the power dissipation during idle mode is leakage currents, which are rising dramatically. Sub-threshold leakage is increased by the scaling of threshold voltage when gate current leakage increases because oxide thickness is scaled. With rising demands for mobile devices, leakage energy consumption has received even greater attention. Since a mobile device spends most of its time in standby mode, leakage power savings need to prolong the battery life. That is why low power has become a significant factor in CMOS circuit design. The required design and simulation of an AND gate with the BSIM4 MOS parameter model at 27 °C, supply voltage of 0.70V with CMOS technology of 65nm are the validation of the suitability of the proposed circuit technology. AND simulation. The performance parameters for the two AND input gate are compared with the current MTCMOS and SCCMOS techniques, such as sub-threshold leakage power dissipations in active and standby modes, the dynamic dissipation, and propagation period. The proposed hybrid super cutoff complete stack technique compared to the current MTCMOS technology shows a reduction in sub-threshold dissipation power dissipation by 3.50x and 1.15x in standby modes and active modes respectively. The hybrid surface-cutting technique also shows savings of 2.50 and 1.04 in power dissipation at the sub-threshold in standby modes and active modes compared with the existing SCCMOS Technique.

1. Introduction
Complementary Metal Oxide Silicon (CMOS) technology has emerged as the dominant technology for IC design because CMOS is simple to implement on silicon, has lower fabrication cost, and consumes the least amount of power. CMOS is the most appealing technology for the application because of the low development costs and the ability to position analog and digital circuits on the same chip [1-5]. The great advantage of CMOS digital circuits is that they can be designed with low static power consumption in steady-state conditions. Power is consumed primarily when circuits switch between the two logic states and thus, the average power consumption is smaller. CMOS is widely used in almost every type of microelectronic application including personal computers, cell phones, internet applications, and a variety of other communication types of equipment. These are the most important reasons that have directed the semiconductor industry towards CMOS digital circuit designs and place CMOS technologies as the leader in the microelectronics semiconductor industry.

The growing speed and complexity of current technologies show that the power consumption of high-speed integration chips (VLSI) increases considerably. Researchers have developed a range of different design strategies to minimize power to meet this challenge. With over 100 million transistors and a clock size of over 1 GHz, the complexity of today's ICs would render optimizing manual power slow and likely to contain errors. Tools and methodologies of computer-aided design (CAD) are required[6].

1.1 History
The electronics industry began with the invention of vacuum tubes. This equipment monitors the vacuum movement of electrons. But after the Second world war, the complexity and the energy consumption of these devices increased dramatically due to a large number of discrete components.
This will cause the system output to continue to decline. One example is a Boeing B-29, made up of 300-1000 aspirator tubes during the war. Each additional component will reduce trust and increase the time for troubleshooting.

The first point-contact Germanium transistor was revealed in 1947 by John Baden, William Shockley, and Watter Brattain of the Bell labs. Shockley developed the first Bipolar Transistor in 1950 (BJT). Transistors are effective, powerful, and smaller in contrast to a vacuum tube. The transistor is a three-terminal transistor unit electrically operated. A terminal functions as a control terminal. The system ideally works as a switch close to the two ends which, if power is applied on the control terminal, otherwise works as the open switch. In 1958, the first integrated circuit consisted of two bipolar transistors connected on a single piece of silicone and was created by Jack Kilby of Texas Instruments. Bipolar transistors were employed by Early ICs. One of the disadvantages of BJT is that it has more static static power consumption. It implies that even though the device is not switching, power is drawn. This limits transistor numbers which can be integrated into a single silicon chip.

1.2 Need for low voltage and low power design
Due to rapid developments in integration technology and large-scale systems design, the electronics industry has undergone huge growth in recent decades. In the fast-growing electronic world, both analogs as well as digital integrated circuits continue to play an important role for sensing and networking, security and safety, health-care medical and life science. The need for low-power components is increasingly relevant from cell phones to handheld DVD players[8-12]. In recent years, several different approaches have been proposed to operate devices with lower power requirements, including design consideration of emerging technologies. The low power dissipation enhances the available battery life. These constraints of low power consumption are desirable for implantable medical devices. Therefore, the need for the advent of low voltage and low power CMOS integrated circuits arises due to factors based on market demands, technology, and design requirements.

2. Review Of Literature
M.Geetha Priya, et.al (2012), [1]. Leakage power dissipation in low-power VLSI circuits, particularly on-chip systems, is now one of the most challenging issues, with the number doubling every two years. The reduction of threshold voltage greatly increased the leakage of subthreshold, causing very high dissipation of static (leakage) electricity. As stated in the International technology road map for semiconductors, the global power dissipation can be made a major contribution to the dissipation (ITRS). Drainage power means that the long-standing battery-operated devices drain quickly. Leakage power dissipation plays an important role in CMOS submicron technologies. In the literature review, however, numerous strategies for low-power designs to minimize leak power efficiently are suggested.

Ali Peiravi, (2008), et.al [2]. The fast decrease in CMOS technology has made the decline in leak power a major concern in low-voltage, low-power, and high-performance applications. This article introduces a new technique for the design of circuits that minimizes the current of sub-threshold leakages by zeroing the voltage of the drain. In sleep mode, leakage power is reduced, especially in large gates. The proposed circuit design technique is planned to depend less on the size and the temperature of the technology as the power of the subthreshold current increases dramatically in sub-100nm technology.

M.V.S.R.KISHORE, (2017),et.al [3]. Several developments in the rich technology and logical architecture of processes and CAD tools allow for the increasingly greater and faster implementation of systems in integrated circuit designs. As a consequence, these huge integrated systems consume a large amount of power. Decreases not only cost, reduced the energy consumption of the integrated circuit systems but also allows the integrated system to be wide open to many other applications. The power exhausted in Complementary metal-oxide-semiconductor (CMOS) is categorized as leakage or static power consumption and dynamic power consumption. The static power is dissipated when the current leaks between multiple transistor terminals, and when the individual circuit nodes are switched the dynamic power are dissipated.
Qing Xie, (2010), et.al [4], Energy usage has always been a key measure for integrated circuits (ICs). The low voltage has been demonstrated to efficiently minimize the energy usage of ICs. A low-voltage decrease to a very low value which slightly exceeds the value of the transistor threshold voltage leads to a minimal use of energy for some uses such as wireless portable devices, medical devices, and network sensor nodes.

Rajesh Mehra, (2012), et.al [5], The improvement of advanced incorporated circuits is tested by higher force utilization. The blend of higher clock speeds, more prominent utilitarian reconciliation and more modest cycle calculations has added to noteworthy development in power thickness. Scaling improves semiconductor thickness and usefulness on a chip. Scaling assists with speeding up and recurrence of activity and subsequently better. As voltages scale descending with the calculations, limit voltages should likewise diminish to pick up the exhibition points of interest of the innovation, yet spillage current increments exponentially. More slender entryway oxides have prompted an expansion in gate spillage current. Spillage power has become a genuine worry in nanometer CMOS advancements.

Anjita Oza, (2014), et.al [6], Power diffusion in the design of nano-scaling CMOS VLSI circuits is a major consideration. Different strategies for reducing leakage in CMOS transistors have been suggested. Thanks to the new technologies, the current of the leakage have become a significant contributor to the overall energy usage of the integrated devices. Reduction of power consumption is highly desirable for high efficiency and system reliability. Consequently, the importance of low-energy circuits has now increased. The scaling trend led to an increase of sub-threshold leakage rate current and thus static power consumption. This paper focuses on various strategies for minimizing leakage in deep submicron technology.

Wit Basker, (2013).et al [7]. With recent improvements in silicon technology which increase the number of transistors, Modern chip design has made considerable progress, increasing the complexity of a chip while retaining its size. This will continue, with at least 10 microprocessors today fitting on a single chip before 2005. by 2005. This will happen. There are also exceedingly challenging methods and methodologies for designing and evaluating complex digital circuits. While VLSI circuit designers are eager to solve these challenges effectively, the testing process is now among the most costly and problem-solving aspects of the circuit design cycle, which demonstrates the ever-changing need for innovating, testing solutions. VLSIs solutions provide an uncompromising approach to these challenges.

Vinay Kumar Madasu, et.al (2013), [8]. The reduction in threshold voltage due to voltage scaling contributes to a greater amount of sub-threshold leakage and thus static power dissipation in CMOS circuits. Leakage dissipation has become a major concern for VLSI circuit designers for the new CMOS feature measurements (e.g. 45nm and 65, nm). ITRS reports that dissipation of leakage power can regulate total electricity consumption. The power dissipation and adjustments in process parameters have been significant design considerations in the nanometer technology regime. With the power leakage being a dominant power consumption, these problems continue to develop.

Ajay Kumar Dadoria, et.al (2014), [9]. The rapid advancement in semiconductor technology led to transistor characteristics being reduced by the introduction of Deep Sub-Micron (DSM) technology; it enables integration on a single chip due to its extremely complex functionality. The electronic battery-operated system forms the backbone of the increasing demand worldwide for mobile handheld devices. Smart devices, including computers on tablets, personal communication devices (mobiles, PCs, PDAs), listening systems, and implantable pacemakers, have to meet exceptionally low battery life requirements. Leakage energy consumption in CMOS circuit design is one of DSMs main technical problems.

Ruchiyata Singh, et.al (2014), [10]. Leakage power has now become an increasingly important issue in the production of processor hardware and software. An increasing proportion of the processor power consumption is powered mainly by the leak, which increases exponentially with decreasing device measurements. In 65 nm and below technology, leakage is 30–40 percent of processor power. In line with ITRS, leakage dissipation will gradually dominate total energy consumption, as technical feature sizes decrease. In the future, leakage power dissipation may prevail. Although there are many technological processes and circuit-level solutions for reducing processor leakage, a new method is proposed for reducing leakage and dynamic power with a potential minimum area and delay tradeoff.
Yibin Ye, et.al (1998), [11], In the past a variety of techniques for reducing the leakage capacity of standby processors, including Multi-threshold (MTCMOS), Dual-Vt, and Back Body Bias, have been suggested. In this article, we propose a new standby leakage control device that takes advantage of the large drops in leakage current that can be achieved by making more than one transistor disabled from nMOS or PMOS supply & land. A large circuit block usually has a considerable number of logical gates of “stacks” transistors (e.g. PMOS stack in NOR or nMOS stack in NAND gates).

Mohab Anis, et.al (2003), [12], Reducing power dissipation in very large-scale integration is one of the most significant issues today. Scaling allows a major component of total power dissipation to be sub-threshold leakage currents. As a promising way of reducing leak capacity, multi-threshold technology has emerged. This paper includes a variety of heuristic methods for effective gates clustering on multi-threshold circuits by bin-packing (BP) and partitioning (SP) modeling. This paper describes the problems. The SP technique takes into consideration the dynamic routing complexity of the circuit, necessary for the implementation of deep sub microns (DSM).

Anjana R, et.al (2013), [13], Leakage power dissipation has become a big part of the overall electricity consumption in the integrated unit, with the international technology roadmap for Semiconductors predicted to rapidly increase in the next decade (IRTS) (IRTS). This affects the battery-operated devices directly since they have long idle periods. By that the threshold voltage, the sub-threshold leakage current has thus increased immensely and the static dissipation is very high. A variety of techniques were proposed to overcome this high leakage power dissipation to overcome this problem.

Varsha Bendre, et.al (2015), [14], The market demand for low-voltage (LV) circuit designs for low power (LP) consumption has guided industry to develop powerful electronic portable systems. Reducing supply voltage quadratically decreases complex capability and the power from the leakage linearly. The key objective of the low-power design therefore remained supply voltage scaling. This has contributed to circuits operating at less than a threshold voltage of a transistor (i.e. sub-threshold region). Sub-threshold leakage and drain from source current are a major contributor to statistical energy consumption if the voltage at the gate is below the threshold stress. Due to the drop in threshold voltage, the technology's size decreases by a sub-threshold leak current exponentially.

Paulo F. Butzen, et.al (2007), [15], In recent years, electricity use has become an important issue with new mobile products. Also, the dissipation currents in idle mode in advanced CMOS technology have substantially increased, where the device's threshold voltage and gate oxide thickness has been decreased. Consequently, extensive work has been done to understand and model leakage mechanisms and to develop design techniques for static energy saving. The key factors for complete dissipation of leakage in the design of CMOS are the current under threshold and gate oxide.

3. Analysis Of Steady And Dynamic States In A Cmos Transistor
In this work, we carry out a detailed study and review of the possible steady states in a CMOS circuit of both PMOS and NMOS transistors. Based on this basic analysis, we define problems with the previous stable state model and provide a precise stable state model in CMOS circuits. Also, we propose five distinct types of steadily dependent leakage components for a single transistor to better understand the leakage behavior, and examine the components of steady states inside and outside the on- and off-state network CMOS network to classify the main leakage sources for each network (on and off-state network). Finally, we describe main CMOS transistor constant states since, unlike other constant states, main steady states can be found in each CMOS logic gate.

Dynamic dissipation of switching power is induced by circuit loading energy. During each high to low output transition, the CL load capacitance is shown in fig. 1, PMOS loads from the transistor and some energy from the supply of energy. The PMOS distributes half of this energy and the CL retains part. The energy saved is discharged and discharged through the NMOS transistor during the high to low-energy transition.

\[ P = P_{\text{dynamic-switching}} + P_{\text{short-circuit}} + P_{\text{static-biasing}} + P_{\text{leakage}} \]
Figure 1 displays the CMOS inverter. Concerning the assumption that the input waveform does not increase and drop time, the energy consumption during the low to high output transition can be achieved by the integration of instantaneous power. $V_{DD}^2$ regular Joule from the power supply. Equation (2) indicates that it draws CL.

$$E_{Vdd} = \int_0^{\infty} i_{Vdd}(t)V_{dd} \, dt = V_{dd} \int_0^{\infty} C_i \frac{dV_{out}}{dt} \, dy = C_i V_{dd} \int_0^{V_{dd}} dv_{out} = C_i V_{dd}^2$$

The charge that is stored on the capacitor is the equation of CL. $V_{dd}^2/2$ (3). This means that only half of the power source energy is contained in CL. The other half of the PMOS transistor was dissipated. The transition between high and low output dissipates the stored energy to the NMOS transistor from the load ability.

$$E_{C_L} = \int_0^{\infty} i_{Vdd}(t)V_{out} \, dt = V_{dd} \int_0^{\infty} C_L \frac{dV_{out}}{dt} \, dv_{out} = C_L V_{dd}^2 \frac{1}{2}$$

To measure energy consumption, how much the circuit is switched must be taken into account. Due to the frequency of the gate switching $f$, the power from the supply is:

$$P_{\text{dynamic-switching}} = C_i V_{dd}^2 f$$

Compared to other power dissipation components in digital CMOS circuits, for technologies up to 0.18μm, the dynamic switching power dissipation has been controlled by approximately 90% of the overall circuit dissipation. The second source of total dissipation of energy defined in equation (1) is short circuit power. (1). (1). During the transition phase, NMOS and PMOS are simultaneously performed, creating a current flow through the direct route between the power supply and ground terminals. Typically, this short circuit current takes place at very limited ranges. This current is produced with the static CMOS inverter while the input voltage is above ground, higher than the NMOS threshold voltage ($V_{thn}$), and lower as shown in Figure 2, below the power supply of the PMOS threshold voltage ($V_{thp}$). The input ramp, the output load, and the size of the transistors are proportional. The equation can be determined by (5)

$$P_{\text{short-circuit}} = K(V_{dd} - 2V_{th})^3 \mu \cdot f$$

Where $K$ is a constant depending on the size of the transistor and on the parameters of the technology, $V_{dd}$ is the power voltage, $V_{th}$ is the voltage level, $\mu$ is the time to raise or drop the input and $F$ is the frequency of the clock.
If the NMOS and PMOS transistors are calculated to match the rise/fall of the signal slopes at the input and output nodes, this factor accounts for less than 20% of the dynamic shift power requirement. The above two sources of dissipation of power in the CMOS circuits are connected to transitions at door terminals, and therefore dynamic power dissipation is usually referred to. The other two power dissipation components, static bias, and leakage are on the other hand linked to the current which flows when the gate terminals are not changing, and are therefore commonly referred to as static power dissipation. CMOS circuits are preferably not static dissipation of power in steady-state. This is CMOS technology’s most appealing feature. However, there are degraded voltage levels of real systems that feed CMOS gates, and current flow from power to ground nodes is observed. This flow is called static tendency.

Fig. 2. CMOS inverter short-circuit current

In Fig. 3, an inverter drives an NMOS pass-transistor. It is understood that voltage is decreased in A node from CMOS basic circuit theory (Vdd-Vth). The output should be low because the inverter input is high (Vdd-Vth). The PMOS transistor, however, is weakly ON, and thus has a static distortion of power from the ground to earth nodes. The static bias current exists only under the above-stated conditions. Static current from Vdd to ground nodes is known as the leakage capacity without degraded inputs. The magnitude of leakage was poor in earlier technologies and was commonly ignored. However, the equipment has improved its density and its efficiency for decades.

Fig. 3. The degraded voltage level at the input node of a CMOS inverter results in static biasing power consumption.
As a result, a large part of the power dissipation in the CMOS circuits is being made from the leaking current of the nanometer regime, as shown in the figure. 4.

![Active and leakage power dissipation](image)

**Fig. 4.** Active and leakage power dissipation.

Due to dynamic power and reliability problems, the supply voltage must be reduced with technology scaling. However, the unit threshold voltage (Vth) needs to be scaled to ensure a reasonable drive gate. The 5th decrease causes the sub-threshold current to rise exponentially. Also, oxide thickness needs to be reduced to monitor the short channel effects (SCEs) and retain the drive power of the transistor at low supply voltage. A strong tunneling current through the transistor insulator results in the violent scale of the oxide thickness. Also, the use of higher substratum doping densities is mandatory for scaled devices. The drain- and source-to-substrates interconnections cause severe leakage current under high reverse distortion. These are the three primary types of leakage mechanisms: the subthreshold, gate oxide, and PN-junction leakage (BTBT).

4. Research Methodology

In this chapter, performance characteristics of a two-input NAND gate using existing sub-threshold leakage control techniques such as stack technique, MTCMOS technique, sleepy keeper technique, and SCCMOS technique are compared with the conventional CMOS logic technique in 45nm CMOS technology. Performance characteristics such as static power dissipation, dynamic power dissipation, and propagation delay of a two-input NAND gate are analyzed. Reduction in static power dissipation by reduction factors of 1.13x, 1.27x, 1.40x, and 1.44x are observed by using stack technique, MTCMOS technique, sleepy keeper technique, and SCCMOS technique respectively in comparison with a conventional CMOS logic technique for a two-input NAND gate. SCCMOS technique lowers the sub-threshold leakage power dissipation most effectively. This technique therefore effectively decreases the total static power dissipation of deep submicron CMOS technology on digital logic circuits. The efficiency of the proposed CMOS CIRS circuit technology in terms of dissipation of standby sub-threshold leakage power is also compared with the existing techniques in the CMOS bulk CMOS technology, as well as in the SOI CMOD technology.

4.1 Introduction

In the power dispersal of current CMOS circuits, innovation and VLSI supply/limit voltage are continuously decreasing. Spillage management has become more and more important. For example, in the 90nm process cycle, sub-limit spillage energy is anticipated to contribute as much as 42% of the aggregate capacity. In MTCMOS VLSI circuit the use of spillage controls is a big problem. With reduced channel length, limit stress, and door oxide thickness, the principal drive for CMOS circuit
distribution increases. Some take a picture of how the speed and force of such circuits are simplified. It is appealing to reach higher speeds by using low power. The reduction in the power usage of advanced circuits is one of the effective techniques to minimize the voltage of the supply. Furthermore, as an exponential dependence on the voltage supply level through the depleted supply, the lower-edge current is the fundamental spill section of OFF gadgets and has reduced consequences. The activity of ON gadgets can live in the super limit, narrow edge, or sub-edge regions, depending upon the measurement of the decrease in supply voltage.

4.2 Concept Of Sccmos
The p-MOS insertion case concept for the SCCMOS shows. This paper describes and tests the p-MOS insertion case. This is because a substrate material of the p-type is normal and appropriate for the case of p-MOS insertion. The p-type substrate can vary in the p-MOS well voltage in the logic circuit and the p-MOS cut-off, as both pits can be isolated electrically. Consequently, P-MOS bodies can be attached to the virtual V DD, V DDV line in logic circuits that does not require other lines of the p-MOS body bias. The V DD line in the current cell library is thus used to reduce the V DD line and the cell library layout update. The PMOSs can also be well shared between the p-MOS in logical circuits. In that case, the cell libraries must be fitted with an extra virtual VDD line. An additional virtual baseline for the cell libraries is also possible for an n-MOS insertion case.

In series, Fig 3.6 is inserted into logic circuit boundaries consisting of low- V TH moisturizes with low V TH Cut-off PMOS, M1, whose V TH is 0.1–0.2 V. The low V TH ensures that logic circuits run at high speed. M1, V G's gate voltage is triggered to turn M1 on in an active mode. When logic circuits are standby, V G is overrun to V DD+0.4 V to cut the leakage current completely. The low V TH is 0.1–0.2 V lower than the conventionally high V TH and thus can retain the stand-by current level by this excessively-imported mechanism. If V TH is below 0.1–0.2 V or negative, V G should be reduced as long as no gate-oxide reliability problem or gate-induced drain leakage is present (GIDL). In case of n-MOS insertion V DD is applied in the active mode to the gate of the n-MOS cut-off and in stand-by mode overdriven to 0.4 V.

Without any input, the V G gateway generator can be made reasonably simple, as shown in Fig. 3.6, since correct V G control is not needed until the reliability of gate oxides or the GIDL becomes a problem. V G can be run slowly because when the logic circuits reach the stand-by service, high speed is not necessary. The pumping frequency may therefore be small.

![Fig. 5. Concept of SCCMOS.](image)
Fig. 6 demonstrates the gate-oxide reliability strategy, as is the case for future scale-down applications, to minimize voltage across gate-oxide. V DD falls to earth in standby mode, V SS because of the large flow of the low MOSFET. This can contribute to the issue of the p-MOS gate oxide durability when thin-gate oxide is used. In stand-by mode at 0.8-V, 1.2 V is used throughout the gate oxide of the p-MOS cut-off. The connection of 2 P-MOSs is successful in series to prevent the gate oxide from breaking down.

In the SCCMOS technique, a p-MOS transistor is fastened between a logical circuit and a power (VdD) voltage (p-MOS) that has the same threshold voltage as a p-MOS transistor, and between the logical circuit and the soil a n-MOS transistor with the same threshold voltage as that of a n-MOS transistor is equipped in Fig. 3.6.2. This technique is used to view a circuit scheme of a two-input NAND gate. When the sleep transistors are working, the connections of GND at VGS1 and VDD are switched on during the process. During the sleep mode, the positive and negative gate voltages are turned on during the sleep transistors at VGS1 and VGS2.

Fig. 7. Circuit diagram of a two-input NAND gate using SCCMOS technique.

4.3 Hybrid Sccmos Complete Stack Technique
It is similar to the whole stack technique of hybrid MTCMOS. The only difference was that the transistor between the VDD and the logic circuit was low and a transistor low VTH n-MOS between the logical circuit and GND. The only difference was a low VTH p-MOS transistor. This hybrid approach uses a logic circuit. Positive (VGS1) and negative (VGS2) gate voltages are used in this technique for completely switching off p-MOS transistor sleep and n-MOS sleep transistor in standby mode, respectively.
Fig. 8. Logic circuit using hybrid super cutoff complete stack technique.

Due to the use of positive (VGS1) and negative (VGS2) gate tensions to the p-MOS transistors, and to sleep n-MOS transistors, as well as to the stacking effect, sub-threshold leakage dissipation exponentially reduces. In the active mode, the low VTH sleep transistors are switched on by GND and VDD to the PMOS sleep transistor and NMOS sleep. Therefore, it offers a low resistance route to the logical level transition. With the use of low VTH sleep transistors the delay in circuit propagation is minimized in active mode compared to the full MTCMOS hybrid stack technique.

4.5 Hybrid SCCMOS Partial Stack Technique

This technology is similar to the partial stacking technique of the hybrid MTCMOS. The difference between the VDD and the logic circuit and the VTH n-MOS transistor (the Sleep PMOS transistor) is low and the GND sleep NMOS transistor is low.

Figure 9. Logic circuit using hybrid super cutoff partial stack technique.

Due to the use of Positive (VGS1) and NGS2, PMOS transistor and Sleep NMOS transistors as well as the stacking effect, the power dissipation of the sub-threshold leakage decreases exponentially while still in standby mode. In active mode, the sleep transistors with low VTH are triggered so that the logical level is changed on a low resistance path. This technology provides the biggest benefit in comparison with the hybrid SCCMOS full stacking technique because it uses only partial stacking of sleep p-MOS and sleep n-MOS transistors. The total propagation delay in active mode is reduced.

5. Experimental Results

Figs. 5.1 – 5.6 display layout diagrams using current techniques (MTcmos, SCCMOS and
sleeping keeper techniques, two input NAND gates, and one bit ALU (hybrid MTCMOS complete stack technique, hybrid MTCMOS partial stack technique, hybrid SCCMOS complete stack technique, hybrid SCCMOS partial stack technique, a novel circuit technique, and an improved SOI CMOS technology based circuit technique).

Fig. 10 Layout of a two input NAND gate using MTCMOS technique.

Fig. 11 Layout of a one bit ALU using MTCMOS technique.

Fig. 12 Layout of a two input NAND gate using SCCMOS technique.
6. Conclusion
Sub-threshold leakage power reduction is very important in standby modes, where computing takes place only in short burst intervals and the device is mainly in standby mode. It is extremely undesirable to wash out valuable battery energy for a long standby. Portable electronic devices like mobile phones and payphones are used very easily in active mode. Their valuable battery power is
exhausted for a very long time. The leakage of battery power during standby mode on portable laptop is also highly undesirable. The techniques for minimizing sub threshold leakage in standby mode will substantially lower the leakage in applications in burst mode.

This paper introduces a conversion from bulk CMOS to SOI CMOS technology with standby subset threshold leakage management techniques. This paper also introduces an improved SOI CMOS-based technology circuit technology to minimize standby substratum leakage power dissipation efficiently. The proposed technique is tested using the proposed and current standby sub-threshold leakage control techniques by design and simulation of a 1 bit complete adder circuit.

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