Powerful electronic devices require performant short-channel transistors. For organic electronics, though, promising low-cost and flexible electronic circuits, high processing costs for short channel devices are not acceptable. In this regard, vertical organic transistors (VOTs) are an attractive alternative, and in fact, today they reach the highest transition frequency (40 MHz) and the highest footprint current density (>1 MA cm$^{-2}$) among all organic transistors. Here, all VOT concepts are reviewed, while discussing device physics, integration approaches, and highlighting the recent developments. The upcoming challenges for the VOT technology are also presented with a guideline for further developments.

1. Introduction: Vertical Versus Lateral Organic Transistors

The field-effect transistor, invented by Julius Lilienfeld in 1926$^{[1]}$ and first realized in silicon in the 1960s by Kahng,$^{[2]}$ is the key element of modern electronics. Transistors serve many different functions such as logic circuits, amplification, display driving, and many more. The main driving force for the exceptional development of electronics has been the scaling of the silicon metal–oxide–semiconductor field-effect transistor (MOS-FET): By a constant reduction of all dimensions of the devices, the number of devices on a chip has exponentially increased over many orders of magnitude, following the so-called Moore’s law.$^{[3]}$ Additionally, the speed of these transistors has been improved to the range of hundreds of gigahertz. The high performance of these highly scaled silicon transistors is only possible by using high purity single-crystalline substrates and involved processing techniques, including high temperatures and expensive microstructuring steps.

However, there are many application areas where this sophisticated technology based on single-crystalline silicon cannot be used: for instance, flexible display backplanes require transistors deposited on large area substrates by thin-film techniques. Additionally, for flexible displays, it should be possible to bend them to small radii. Besides display technologies, there are many other future applications where flexibility and deposition on non-crystalline substrates are needed. For these purposes, a large number of thin-film transistor technologies have been developed in the past decades. The most prominent technology is based on amorphous silicon, which is used in liquid crystal displays (LCDs). For high resolution LCD displays (>300 ppi) and more demanding displays technologies like organic light-emitting diodes (OLEDs), which require significant current and superior stability, polycrystalline silicon or oxide thin-film transistors have been developed. Polycrystalline Si or oxide transistors have considerably higher mobilities and transition frequencies and thus can also drive displays at higher resolution and refresh rate. Additionally, they enable the integration of transistors into flexible communication devices with ever higher broadcast frequencies. For large area applications and truly flexible substrates though, these technologies are reaching their inherent limits.

Another alternative thin-film technology is based on organic semiconductors, i.e., carbon-based materials which allow a huge variety in materials by chemical synthesis. Furthermore, these materials can be deposited by very simple technologies, like printing, on almost any surface and do not need any high temperature processing which the inorganic thin-film technologies usually require. Therefore, research on organic thin-film transistors has been intensive in the last decades.

The first organic transistor was presented in 1986 by Tsumura et al.$^{[4]}$ Since then, a huge improvement in organic transistors has been achieved. The main thrust in research has been to improve the mobility of organic semiconductors. Indeed, in recent decades the mobility has improved from $10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ in the first organic transistors to values close to 100 cm$^2$ V$^{-1}$ s$^{-1}$, higher than amorphous Si and competitive with poly-Si and oxide devices. However, as recently shown by several authors, many of the measurements to determine the mobility were incorrect as effects from contact resistances have been neglected.$^{[5–7]}$ Many publications in the literature are presenting data which seriously overestimate the real mobility in the devices. One solution relies in using four-point measurements, e.g., the gated van der Pauw method as suggested by Rolin et al.$^{[8]}$ It is also telling that these recent increases in mobility values did not lead to improved device parameters: For instance, the most important measure, the transition frequency of organic transistors, has not significantly increased in the last few years.

The most straightforward way to increase transition frequencies is to shorten the channel length $L$, as the transition frequency scales with $1/L^2$. Until recently, the best transition frequencies achieved with an organic transistor were in the range of about 20 MHz.$^{[9,10]}$ Although sub-micrometer channel
lengths have been used, these frequencies are still significantly lower than required for many interesting applications, such as high-resolution displays or flexible devices with communication functions. A recent review by Klauk points out that GHz organic transistors should be possible, using very short channels in the sub-micrometer regime.\(^{[11]}\) However, this paper also clearly shows that besides short channel length, low contact resistances are crucial for high frequencies.

The downscaling of channel lengths also addresses the second important parameter of transistors, the saturation current. For instance, this applies to OLED displays which use current driven pixels (in contrast to voltage-driven LCDs). Here, high current densities are an advantage since they allow for the reduction of the transistor footprint. The saturation current increases linearly with the ratio of mobility to channel length \(\mu/L\), further emphasizing the need to use very short channels.

For realizing low-cost electronics on flexible substrates, it seems inadvisable to use highly sophisticated micro- or nano-structuring techniques. One approach to overcome the problem of low frequencies and avoid microstructuring is to use transistors with a vertical channel. The basic idea is to convert the channel length definition by structuring into one by layer thickness. Since current deposition methods allow control over layer thicknesses comparatively easily in the tens of nanometer range, this approach can realize transistors with very short channels, completely avoiding involved lateral structuring in the nanometer range.

The first vertical transistors were realized with inorganic semiconductors.\(^{[12]}\) With organic materials, the first vertical transistor was proposed by Yang and Heeger in 1994.\(^{[13]}\) Since then, an increasing number of articles per year have been published on vertical organic transistors reporting on the continuously improving performance of the devices (Figure 1). Merely in 2018, this number has decreased, which is an indication that the topic has matured in the last several years and research groups have identified and focused only on the most promising device concepts. The device parameters of vertical devices have recently exceeded those of conventional lateral organic field-effect transistors (OFETs) and have achieved world records in current density and transition frequency: in 2017, a current density of 1 kA cm\(^{-2}\) was reached,\(^{[14]}\) for a device suitable, e.g., for integration with an OLED display. This current density

![Figure 1. Number of peer-reviewed articles published on vertical organic transistors since 1994.](image)

Hans Kleemann obtained his physics diploma from the University of Jena in 2009. From 2009–2012, he joined Prof. Leo’s group at Technische Universität Dresden working on organic electronics. After receiving his Ph.D. in 2013, Hans joined NOVALED/Samsung SDI as a researcher/project leader on organic transistors for display applications. He returned to academia in 2016 and joined the group of Prof. Feng Wang in the Physics Department of UC in Berkeley, USA, where he explored charge carrier transport and dielectric screening phenomena in 2D materials. In April 2017, Hans became a group leader at TU Dresden, focusing on next-level organic electronic devices.

Kevin Krechan completed his Master of Science in the group of Professor Karl Leo (IAPP, TU Dresden) in 2018. The focus of his investigation was to find evidence of modulation doping in organic semiconductor heterostructures to adapt this concept for remote-doped organic transistors. He continued working as a scientific assistant to develop an in-depth understanding of the underlying charge transfer mechanism. Currently, he is pursuing a Ph.D. at the IAPP, where he investigates materials and techniques for the realization of biodegradable sensors and electronic circuits for medical applications.

Karl Leo obtained his Diplomphysiker degree from the University of Freiburg in 1985 and Ph.D. from the University of Stuttgart in 1988. From 1989 to 1991, he was a postdoc at AT&T Bell Laboratories in Holmdel, NJ, USA, and from 1991 to 1993 with RWTH Aachen, Germany. Since 1993, he is a full professor of optoelectronics at TU Dresden. His main interests are novel semiconductor systems like semiconducting organic thin films. His work was recognized by several awards, including the Leibniz-Award (2002) and the Zukunftspreis of the German president (2011). He is co-founder of several companies, including Novaled and Heliatek.
would allow the transistor area to be restricted to a small part of the OLED pixel. More recently, this current density has been further increased by three orders of magnitude in a vertical electrolyte-gated organic transistor.[15] Figure 2 summarizes the recent progress in current densities achieved for vertical organic transistor devices, in particular, it shows current densities versus the on–off ratio.

Recently and for the first time, vertical transistors were also achieving the highest transition frequencies observed across all organic transistor devices. Using a vertical organic permeable base transistor (OPBT), a new record of 40 MHz was reached.[21] Figure 3 summarizes the recent progress in transition frequency obtained for all sorts of organic transistors. Here, the transition frequency normalized by driving voltage is an insightful figure of merit as it is important to achieve high speed at low applied voltages.

The purpose of this review is to summarize this recent rapid progress, in particular relative to our review in 2015,[30] and show the huge potential the vertical device concept has for organic transistors. Furthermore, we specifically address the different ways vertical transistors have been realized.

The review is organized as follows: We first discuss the different device principles for controlling vertical currents in an organic semiconductor device. Three basic principles are discussed: We start with the vertical OFET design which makes use of the gate control as in lateral OFETs. Then, we discuss the recently very successful OPBT, which uses a concept similar to a vacuum triode: the carriers move from a planar emitter electrode toward a planar collector electrode, and the current is controlled by a semitransparent base contact. Additionally, we also address the so-called vertical organic static induction transistor (OSIT). Beyond these well-established vertical organic transistor concepts, we also summarize very recent developments in the field leading to current densities of up to 1 MA cm⁻². Finally, we provide a comparison of important performance figures of vertical organic transistors and compare it to state-of-the-art lateral OFETs.

2. Overview Over Device Principles and State-of-the-Art

There is a large diversity of different device concepts for vertical organic transistors, far more than for lateral organic transistors. This is likely due to the fact that the 3D device architecture along with the challenge of forming an ultrashort vertical channel has inspired researchers to envision new device structures. In this section, we provide an overview of all vertical organic transistor principles, describing their operation and providing an update on the current state-of-the-art compared to our previous review article.[30] Additionally, we discuss very recent trends in the field including the development of vertical electrochemical transistors. Beyond reviewing the device concepts, we use this article to critically assess the performance of...
vertical organic transistors and provide a detailed comparison of performance figures of state-of-the-art vertical versus lateral transistors. This comparison clearly shows that vertical organic transistors can outperform their lateral counterparts in some aspects. However, it also shows where further optimization is required in order to bring the performance up to par with the requirements for applications.

Generally speaking, vertical organic transistor concepts can be categorized into FET-like (closely resembling conventional FET structures) and solid-state triode structures (resembling a vacuum tube triode). For both categories, devices with outstanding performance have been demonstrated, and as we will see in Section 2.6, nowadays vertical organic transistors are leading-edge devices which are highly attractive for electronic applications, e.g., in wireless communication or active-matrix display driving. First, we will review the FET-like architectures such as the Schottky barrier vertical organic field-effect transistor (SB-VOFET) and the VOFET. Due to their structural similarity to conventional organic field-effect transistors, SB-VOFET and VOFET devices offer convenient device integration employing established processing techniques. However, as we will see, the term vertical organic transistor is often misleading for VOFETs, since many of these structures only possess a pseudo-vertical channel (a hybrid of lateral and vertical transport, often with lateral transport up to several micrometers). In contrast to VOFETs, triode-like vertical organic transistors such as the OPBT and the OSIT offer almost pure vertical transport and, hence, the highest performance (lateral transport only occurs on the nanometer scale). However, this advantage comes at the expense of a more complex integration procedure often requiring nonscalable processes.

2.1. Schottky Barrier Vertical Organic Field-Effect Transistors

SB-VOFETs belong to the category of FET-like vertical organic transistors. In such a device, the source, active semiconductor, and drain electrode are vertically stacked. The gate electrode is below the source electrode, from which it is separated by an insulating layer (Figure 4a). The source electrode, semiconductor, and drain electrode form a diode with a Schottky-like contact at the source–semiconductor interface. The operation of the SB-VOFET relies on the modulation of the height of this Schottky barrier by the gate potential, which eventually results in a modulation of the charge carrier injection probability into the semiconductor. Consequently, the operation of the SB-VOFET relies on modulation of the injection/contact resistance, rather than a direct manipulation of the charge carrier densities as in conventional field-effect transistors.

Effectively controlling the barrier, though, is only possible if the electric field of the gate is not completely screened by the free charge carriers in the source electrode. However, this condition requires metallic electrodes to have a thickness of ≤1 nm due to the high charge carrier density and small Debye length. Alternatively, the source electrode might be composed of a discontinuous metal film (e.g., caused by surface roughness) or a porous network of thin conductive wires such as single-walled carbon nanotubes (SWCNTs). In general, the scientific and technological challenge for SB-VOFETs is, first, to find fitting combinations of the semiconductor and the source electrode material with appropriate barrier height and, second, to find materials and methods in order to form the weakly screening source electrode. In this regard, a manifold of electrode materials, such as single-layer graphene (SLG), SWCNT networks, discontinuous metal films, porous indium tin oxide, or even black phosphorous have been reported.

The first SB-VOFET was pioneered by Ma and Yang in 2004 (Figure 4a). They employed a porous layer of LiF as a gate insulator material which was covered by a 20 nm thick source electrode. The roughness of this source electrode was comparable to the film thickness, which has been argued to be the reason for the weak screening by the metal electrode. This resulted in an effective control of the injection barrier height to the semiconductor material C60. Impressive performance
figures were obtained for these first devices including a maximum on-current density of 4 A cm$^{-2}$, an on–off ratio of $\geq 10^5$, and a driving voltage of $\leq 5$ V. Despite these encouraging values though, the group did not publish further achievements and the devices remained a lab curiosity. Moreover, other groups also failed to reproduce these devices. The reason for this is probably because of the LiF insulator, which has a capacitance and also conductance that vary significantly with the environmental humidity. More specifically, Ma and Yang measured a specific capacitance of 25 $\mu$F cm$^{-2}$ at 44% and 0.01 $\mu$F cm$^{-2}$ at 0% humidity. Thus, the transistor operation was highly dependent on the environmental conditions, which made it almost impossible to reproduce.

Nonetheless, these developments have proven the great potential of SB-VOFETs and have motivated other researchers to explore new designs and materials. Among them is the Tessler group which has continuously developed in the last decade a very robust, high performance SB-VOFET device.[35,38–47] Moreover, they significantly contributed to the development of a rigorous understanding of the SB-VOFET operation by means of drift-diffusion modeling.[38,42]

Ben-Sasson et al.[35] avoided the shortcomings of Ma’s approach by choosing conventional gate insulator materials (e.g., SiO$_2$ or Al$_2$O$_3$) and most importantly by replacing the rough metal electrode by a thin nanopatterned metal film. The challenge was to find a suitable technique which enabled the fabrication of nanometer size openings in the thin metal film. For this purpose Ben-Sasson et al. had chosen a soft lithography method based on a self-assembled block polymer (polystyrene (PS)-poly(methyl methacrylate)) and a lift-off process which facilitates the fabrication of 50–100 nm openings in a 10 nm thin metal electrode[43] (Figure 4b). Performance figures such as an on–off ratio of $10^4$ and an on-current density of 0.1 mA cm$^{-2}$ were reported for the first devices which were based on C$_{60}$ as the semiconductor material. After various improvements over the years (higher gate capacitance, optimized Schottky barrier, and semiconductor material with higher charge carrier mobility), the group of Nir Tessler reported devices with an on-current density of 3 A cm$^{-2}$, an on–off ratio of $\geq 10^5$, and a driving voltage of only 3 V.[41,43] Furthermore, this group greatly contributed to the theoretical understanding of the device operation by introducing the concept of the virtual contact which is used to describe the electric field within the electrode openings. Moreover, they emphasized the fact that lateral transport on the scale of 50–100 nm within the electrode openings gives an important contribution to the overall transport.

Another approach to circumvent the shortcomings of Ma’s structure is employing SLG or conductive networks of single-walled carbon nanotubes as source electrode material (Figure 4c,d, respectively). In either case, the thin electrode material gives rise to an incomplete screening of the gate field which leads to the fact that the work function of the source electrode material can be directly manipulated by the gate field. This effect has been nicely demonstrated by Park et al.[50] who have proven that the work function of SLG can be shifted by up to 0.6 eV depending on the position of the Dirac point, which can be tuned by doping. Although this effect might be suppressed in SWCNT networks due to the bundle formation of the CNTs, the porous character of the network with its plethora of nanometer size openings leads to a weaker screening compared to a continuous graphene film. Both approaches have been successfully demonstrated by several research groups for p-type,[50,51] n-type,[52–55] and ambipolar charge carrier transport.[56] The best devices have been shown with an on-current density of 50 mA cm$^{-2}$, an on–off ratio of $\geq 10^5$, and a driving voltage of only 4 V.[48] Such a low voltage was enabled by a very thin 10 nm gate insulator (5 nm of Al$_2$O$_3$ and 5 nm of BCB). For thicker, conventional insulating layers though, such SB-VOFETs often show a significant hysteresis and low on–off ratio due to the weak impact of the gating effect on the work function of the source electrode.[33,50] Another problem inherent to all SB-VOFET structures is the trade-off between the electrical conductivity of the source electrode and the permeability to the gate field. In particular, for SWCNTs- (typical sheet resistance of 10–15 k$\Omega$ sq$^{-1}$) and SLG-based SB-VOFETs, this problem has been shown to limit the overall current density which can be driven through these devices,[48] leading to even the highest current densities being several orders of magnitude smaller than for other vertical transistor concepts.

2.2. Vertical Organic Field-Effect Transistors

Despite the above-mentioned obstacles (comparably low on–off ratio, sheet resistance limitation, and hysteresis), SB-VOFETs have attracted considerable attention due to the possibility of monolithically integrating an OLED into a transistor stack,[36,46,50,57] yielding a vertical organic light-emitting transistor (VOLET). Such an integration is of high interest for the design of active matrix organic light-emitting diode (AMOLED) displays for several reasons. First, combining the driving transistor and the OLED saves valuable space in the pixel, which can be used to increase the size of the OLED, which in turn also improves the overall power efficiency of the display.[57] Second, the monolithic integration reduces the overall driving voltage (needed for the driving transistor and the OLED, Figure 5), which also significantly raises the overall power efficiency. Moreover, some of the disadvantages of SB-VOFETs are only of secondary importance for the driving transistor in an AMOLED. For example, the low on–off ratio of only 10$^3$ is sufficient to achieve an excellent optical contrast of the display (only the switching transistor in the display is required to have a high on–off ratio for state-retention).

The technology of carbon nanotube-based SB-VOFETs seems to be favorable for integration with OLEDs. In particular, the Rinzler group has achieved great progress on the single device level (stability and power efficiency[57]) but also on the display level. Most interesting to the vertical transistor community is to see the development of their spin-off, Matrix Technologies,[58] which recently received funding from the flat panel industry in order to pioneer this technology and bring it to the display market.

2.2. Vertical Organic Field-Effect Transistors

The vertical organic transistor concept which most resembles the traditional planar organic field-effect transistor, in terms of structure as well as operation, is the VOFET. When a gate–source voltage is applied, the charge carrier density at
the semiconductor–insulator interface is effectively modulated, switching the device from its on- to its off-state, or from accumulation to depletion, respectively. Additionally, the electric field between drain and source pulls the charge carriers toward the drain electrode, thereby causing the net drain current to flow. In contrast to the planar OFET structure, the channel of transport in VOFETs is no longer restricted to the semiconductor–insulator interface, but rather becomes distributed, with contributions in lateral and vertical direction to the gate insulator interface. Hence, unlike most of the other vertical organic transistor concepts, the channel of transport is not truly vertical and the exact geometry of the electrodes governs the balance between lateral and vertical transport. In nonoptimized geometries, lateral transport may take place over several micrometers.

A strong advantage of VOFETs, which is also caused by their close structural similarity to planar FETs, is the fact that mature processing techniques as developed for planar FETs, such as photolithography, wet- and dry-etching, and printing, can also be exploited for the fabrication of vertical field-effect transistors. In particular, all VOFET architectures reported do not require any complex nanoscale structuring as needed for other vertical transistor concepts. In this sense, the moderate device complexity of VOFETs over other vertical transistors, as well as the possibility to adopt scalable and mature processing techniques in order to prepare compact device designs, justifies the interest in VOFETs as a suitable technology for future flexible high-resolution active matrix backplanes based on organic transistors.

2.2.1. VOFET Structure and Fabrication

Vertical organic field-effect transistors and their fabrication techniques have experienced a continuous evolution over the last 15 years which has resulted in a steady improvement in performance and a maturing of processes. The first organic devices which can be named VOFETs were step-edge transistors, as shown in Figure 6a,b, while later other structures have also been proposed.

A step-edge transistor geometry is composed of vertically displaced source and drain electrodes with an insulator as a spacer. The step-edge of the insulator connecting both electrodes defines the channel of transport. Depending on whether the device follows bottom- or top-gate architecture (Figure 6a,b), either the source–drain insulator acts as the gate insulator (bottom-gate) or an additional insulator layer is wrapped around the step-edge covered by the semiconductor (top-gate). In any case, the semiconductor–insulator interface defines the channel of transport, which is formed in the first few molecular layers of the organic semiconductor adjacent to the insulator interface. Consequently, there is no major contribution of charge carrier transport perpendicular to the semiconductor–insulator interface and therefore

Figure 5. Monolithic integration of an SWCNT-based SB-VOFET and RGB OLEDs.[49] The current density and luminance versus gate voltage are shown for the integration with a) red, b) green, and c) blue OLED. d) The emission of the SB-VOFET-RGB-OLED device in the on- and off-state. Reproduced with permission.[57] Copyright 2011, AAAS.

Figure 6. Vertical organic field-effect transistor designs: a) Top-gate step-edge VOFET as proposed by Stutzmann et al.[59] and Parashkov et al.[60,61], b) bottom-gate step-edge VOFET described by Uno et al.[62] and Kudo et al.[63], and c) stacked bottom-gate pseudo-VOFET with additional insulator between source and drain electrodes as employed by Nakamura et al.[64] and Kleemann et al.[65]
step-edge transistors resemble ultrashort channel transistors, rather than being truly vertical devices.

The first organic step-edge transistors being reported[59–61] were top-gate devices as shown in Figure 6a. While Stutzmann et al.[99] produced this pyramid-like structure by a solid-state embossing with a sharp protruding master tip, Parashkov et al.[60,61] utilized the tilted step-edge of a photosensitive layer after patterning. In both cases, the insulating layer defines the channel length by its thickness and its angle to the substrate and it has been reported to vary between 900 and 1200 nm. Furthermore, the polymer layer which forms the step-edge is employed as an electrical insulator between the source and drain electrode. Strictly speaking, the channel formed between the source and drain is still parallel to the gate insulator interface and hence, as described above, it is more appropriate to call such step-edge devices short-channel transistors rather than truly vertical. Nonetheless, the short channel length in these step-edge devices gives rise to several short-channel effects which are also observed in truly vertical structures and, therefore, these early studies provided detailed insights into some aspects of operation of vertical organic transistors. In particular, short-channel effects (cf. ref. [66] for a general overview) such as loss of saturation, threshold voltage roll-off (threshold voltage depends on the drain–source field), strong contact resistance, and high on–off ratios of ≤10⁶, a transition frequency of 5 MHz, and self-aligned electrodes even on flexible substrates. Additionally, the potential of bottom-gate step-edge VOFETs to operate at below 1 V has been highlighted.[76]

Despite their exceptional performance and the appealing simplicity of processing, at present, bottom-gate step-edge VOFETs have not been transferred successfully from laboratories to application. The ease of processing by shadow masks and a self-alignment of electrodes at the step-edge is deceptive, because in practice even the smallest defects at the step-edge create a direct connection between the source and drain and hence result in a dysfunction of the transistor. Additionally, the self-alignment at the step-edge dictates the electrode design and such a restriction is unacceptable for the development of electronic circuits.

An alternative VOFET architecture which combines the attractive performance of bottom-gate step-edge VOFETs with the ease of processing of lateral organic transistors has been conceived by the Kudo group in the form of a vertical light-emitting transistor where an organic light-emitting diode is embedded between the source and drain electrodes.[64,77] This concept has been substantially improved by Kleemann et al.[65] in order to achieve high speed operation for p-type transistors.

These bottom-gate vertical field-effect transistors (Figure 6c) conceptually resemble a lateral field-effect transistor with an additional insulating layer atop the source electrode (often denoted as a charge-blocking-layer (CBL)). The drain electrode, rather than being laterally aligned to the source, is vertically stacked on top of the insulating material (which is composed, e.g., of SiO₂ or a photosensitive film). Consequently, this arrangement of electrodes should result in a vertical channel length defined by the thickness of the organic semiconductor layer which can be as thin as 100 nm, hence promising exceptionally high current densities. In practice though, the effective channel length is not only given by the organic semiconductor film thickness but also to a large extent by the lateral overlap of the insulator over the source electrode. Hence, although the term vertical transistor is justified because the main contribution to the overall channel is formed along the vertical insulator edge which is orthogonal to the gate insulator interface, lateral transport might deliver a considerable contribution to the overall transport. Consequently, it is more appropriate to denote these transistors as pseudo-VOFETs rather than truly vertical OFETs.

The overlap leading to the lateral transport is practically unavoidable in this device structure and its size is inherent to the patterning and alignment method being used. While
Nakamura et al.\textsuperscript{[64]} employed a shadow mask system for this patterning step resulting in an overlap of several micrometers, Kleemann et al. developed several techniques over the years in order to bring this overlap down to the nanometer scale. Among these techniques are: lift-off processes,\textsuperscript{[65]} complex dual-step photolithography methods,\textsuperscript{[79,80]} and photolithography combined with wet-etching.\textsuperscript{[81]} In particular, the development of a photolithographic process including wet-etching resulted in an overlap of ≤50 nm which leads to an overall channel length of these pseudo-VOFETs in the range of 100–200 nm. Another substantial improvement, which is essential to achieve high current densities for short-channel transistors, is the implementation of contact doping in order to reduce the contact resistance. This implementation has been successfully demonstrated in refs. \textsuperscript{[82–85].}

Overall, the pseudo-VOFET concept as proposed by the Kudo group and later improved by the Leo group enables the fabrication of high-performance vertical organic transistors with fabrication methods which are compatible with conventional OFETs. This renders the possibility for a seamless integration of such high performance devices into existing pilot lines for OFETs, e.g., for application in active matrix backplanes. Due to this attractiveness of pseudo-VOFETs, we will review in the following subsection the VOFET operation in more detail in order to understand the true potential and restrictions of this transistor technology.

2.2.2. VOFET Operation—Experiment and Theory

The charge carrier transport in pseudo-VOFETs substantially differs from step-edge devices which are sufficiently described by the physics of lateral short-channel transistors. As mentioned in the previous section though, the charge transport in pseudo-VOFETs is composed of lateral and vertical components. The device parameters which mainly define the ratio between these two contributions are the lateral overlap of the source insulator over the source electrode and the thickness of the organic semiconductor layer (Figure 6c). Furthermore, another important parameter which governs the balance of these two contributions is the anisotropy of charge carrier mobility in the organic semiconductor film.

The first systematic study on the charge carrier transport in pseudo-VOFETs was carried out by Kleemann et al.\textsuperscript{[65]} The two most important findings of this study are that the overall current scales with the width of the drain electrode (which is equivalent to the channel width of a lateral transistor) and that the current–voltage characteristics are mainly limited by the charge carrier injection from the source electrode rather than the channel itself. This last finding is in agreement with studies on contact resistance in lateral OFETs, where the contact resistance governs the OFET performance for a channel length of typically ≤10 μm.\textsuperscript{[86]} Consequently pseudo-VOFETs usually do not operate in the linear or saturation regimes but rather are described by nonlinear current–voltage characteristics. Additionally, other short-channel effects are also inherent to pseudo-VOFETs. In particular, threshold voltage roll-off and increased off-state current due to unintentional background doping are frequently observed;\textsuperscript{[65,81–83]} the latter effect can be partially mitigated by the choice of an appropriate semiconductor material.\textsuperscript{[81,87]}

In contrast to lateral OFETs, the contact resistance is not accessible for measurement in pseudo-VOFETs, e.g., by the transmission-line-method (TLM) or 4-probe-techniques. Hence, the influence of the contacts can only be analyzed by modeling in conjunction with a comparison to the experiment. The first attempt to model the transport including the contact effects have been reported by Kwon et al.\textsuperscript{[88]} They modeled the contact properties by taking into account the barrier height for injection at the source electrode and the lateral and vertical resistance of the semiconductor film between the source electrode and the gate insulator (current-crowding model).\textsuperscript{[89]} In particular, they highlighted that the overall contact resistance is mainly limited by the barrier between the source metal and the semiconductor if the height of the barrier is ≥0.3 eV. Additionally, they argued that the drain-source voltage mainly drops across the contacts (including the resistance of the semiconducting film between the source electrode to the gate insulator) and hence the linear and saturation regimes are not expected to be observed for these devices. Later, Sawatzki et al. developed a more detailed model for the transport in pseudo-VOFETs by focusing on the role of the lateral overlap of the charge-blocking-layer over the source electrode and the influence of a different lateral and vertical charge carrier mobility.\textsuperscript{[79]} By means of a 2D drift-diffusion model they analyzed the charge carrier distribution within the device in order to understand how the ratio of lateral and vertical transport governs the shape of the channel. In particular, they discussed how far the channel extends in the lateral direction. As shown in Figure 8, they have proven that after injection, charge carriers are not only accumulated at the gate insulator interface, but also at the interface to the CBL. The latter effect is due to the strength of the drain–source field which forces charge carriers to form a second channel interface. The transport in the lateral direction toward the edge of the CBL only originates from diffusion due to the weak lateral electric field. Once the edge of the CBL is reached, charge carriers are pulled upward to the drain by the strong electric field thereby forming the vertical channel at the edge of the CBL. Surprisingly, the lateral extension of the vertical channel is only in the range of several hundreds of nanometers (upper limit estimated to be ≤1 μm) which is mainly explained by the strong vertical component of the electric field. This finding is very important for integrated vertical transistors because it means that the vertical channel of adjacent transistors will not overlap due to strong lateral transport. Sawatzki et al. even went a step further and provided experimental evidence for their theoretical prediction. They incorporated an OLED into the transistor structure and carefully analyzed the emission profile at the CBL edge (Figure 9). In agreement with the model, the lateral extension of the channel can be tuned by the gate–source and drain–source voltage and an upper limit for the size of the lateral channel extension has been determined to be ≤4 μm (limited by the optical resolution).

Overall, a robust understanding of the transport in pseudo-VOFETs has been developed over the last several years. Besides the importance of contact resistance, also the influence of the lateral transport and in particular the lateral overlap of the CBL over the source electrode has been highlighted. As argued by
Sawatzki and co-workers, the lateral transport is governed by diffusion. Hence, if the overlap of the CBL exceeds the vertical channel length, lateral diffusion is expected to restrict the overall current density. Consequently, the most promising strategy in order to improve the performance of pseudo-VOFETs is to reduce the lateral CBL overlap. In this regard, substantial progress has been made by using photolithography[65,85] and wet-etching techniques to pattern the source electrode and CBL. Nowadays, pseudo-VOFETs have been reported with a lateral overlap of merely 50–100 nm which enables leading-edge performance of the transistors with on–off ratios in excess of 10⁷ and highest on-current densities in the range of 50 A cm⁻².[81]

2.3. Organic Permeable Base Transistors

The vertical transistor structures discussed in the previous sections are rather similar to conventional FETs in the sense that the gate electrode is outside of the semiconducting layer and well separated by an insulating material. However, the OPBT represents a substantially different vertical transistor concept. In particular, the OPBT resembles a vacuum triode where a thin metal electrode (denoted as the base) is sandwiched between the charge carrier injecting electrode (called the emitter) and the electrode for charge carrier extraction (also known as the collector, Figure 10a). The thin base electrode is employed to control the current flow from the emitter to the collector electrode, thereby creating the transistor function. Obviously, the thin metal electrode needs to have the special property that it is permeable for charge carriers moving from the emitter to the collector and that the degree of permeability is controllable by the potential at the base electrode.

In the following, we will review the structure and operation of OPBTs. Most importantly though, we will discuss the most recent developments in the field of organic permeable base transistors which have led to considerable improvements in on–off ratio, the highest reported current densities, device reliability, operation stability, and transition frequency. Overall, due to these recent improvements, the OPBT with its truly vertical character is one of the most promising vertical organic transistor concepts and has already proven to be the fastest organic transistor today.

In 2005, Fujimoto et al.[90] reported on the first OPBT which was based on C₆₀ and Me-PTC as active semiconductor materials. Already these first devices (n-type) had shown exceptional performance with an on–off ratio of ≥10⁵. Later the focus shifted to p-type OPBTs, where a similar level of performance had been reached.[91-94] The real performance breakthrough though came with Fischer et al. who reported in a series of papers[14,21,84,95-100] on the continuous improvement of an n-type OPBT, which ultimately led to the performance records mentioned previously. Furthermore, Fischer and co-workers[101]
The OPBT operation can be described as follows. Charge carriers are injected from the emitter electrode into the organic semiconductor material by applying an emitter–collector voltage $V_{CE}$. Without applying a base–emitter voltage $V_{BE}$, electrons are not able to pass through the base and hence do not reach the collector—the OPBT is in its off-state and the off-state current is only limited by the number of electrons falling into the base electrode (the transfer curve of an OPBT is shown in Figure 10c). After applying a positive base–emitter voltage, the OPBT turns on and charge carriers coming from the emitter accumulate at the base electrode in front of the native AlO$_X$ passivation layer. Once accumulated, electrons laterally diffuse to the pinholes (Figure 10a) from which they are pulled toward the collector (scale of lateral diffusion in the range of 50 nm).

The on-state of the OPBT shows three distinct regions:
- The exponential increase of the collector current $I_C$ with a slope of 60–85 mV dec$^{-1}$, a linear region for $V_{BE} \leq 0.6$ V, and saturation for $V_{BE} \geq 1.1$ V (for a $V_{CE} = 1$ V). The steep exponential increase, which is very close to the thermodynamic limit of the subthreshold slope at room-temperature, provides evidence for the very effective switching of the OPBT. The saturation of the transfer curve though is not expected from conventional transistor theory. Its appearance has been explained by device simulations which prove that the OPBT is purely limited by space-charge-limited currents in the intrinsic layers in this regime and the overall on-current can only be increased by applying a higher emitter–collector voltage. Consequently, the OPBT is only limited by the thickness and the vertical bulk mobility of the intrinsic layers at high current densities—the transistor channel, which is the pinholes through the base, is highly conductive and does not limit the transistor operation. Furthermore, evidence for this behavior is found in the output curves of the OPBT (Figure 10d,e) where, besides a linear regime for small $V_{CE}$, a space-charge-limited current (SCLC) is obtained. Thus, contact resistance in an OPBT is not only not by the injection resistance at the metal electrode but rather by the vertical transport resistance of the connecting semiconductor layer—an effect which has also shown to be relevant for lateral organic transistors and other vertical transistors such as the VOFETs.

Based on this understanding, Fischer and co-workers employed several optimization steps in order to push the performance of OPBTs to their inherent limit. The first improvement concerns the emitter and collector electrode as well as the charge carrier injection. Because the highest on-current that the OPBT can drive is limited by the contact resistance, electrodes optimized for charge carrier injection were developed. A combination of aluminum and chromium has been shown to be the most effective, giving the lowest contact resistance to $C_{C60}$. This contact resistance has been further reduced by inserting a chemically doped C$_{60}$ layer directly underneath the emitter electrode as shown in Figure 10a. In this way, the contribution of the C$_{60}$ layer to the overall device resistance is greatly reduced and the transport is purely limited by the SCLC and thus by the mobility of the semiconductor.

The second optimization concerns the device geometry and electrode layout. Due to the triode-like configuration and the fact that there is only an ultrathin native oxide separating the semiconductor and the base electrode, reducing the parasitic...
electrode overlap areas is a vital task in order to reduce the off-current of the OPBT and other parasitic effects such as charging of non-overlapping areas by lateral transport. In this context, a special transistor layout has been proposed where an additional insulating layer of either SiO or the poorly conductive organic material Spiro-TTB is patterned either on top of the base electrode [97] or underneath the emitter electrode [14] (Figure 10a). This layer is patterned in a way that it defines the trench for the overlap of emitter, collector, and base, and hence thereby the active area of the device (Figure 10b). This technique, called the indirect structuring method, has led to the realization of smaller active area, a significant reduction of leakage current, and parasitic electrode resistance, and hence a higher on–off ratio. [104]

The third optimization concerns the most fragile part of the OPBT—the thin native oxide film surrounding the base electrode. Despite its appealing simplicity, the formation of the base passivation by oxidation in ambient severely limits the device reliability and reproducibility. Therefore, an alternative oxidation method is desirable, which ideally would also enable the usage of a thicker base layer as well as the ability to modify the thickness of the oxide by means of the process. Very recently, Dollinger et al. [99] proposed electrochemical anodization as a method to control the AlO$_X$ thickness by the anodization potential. Most surprisingly, they demonstrated that the anodization, a wet-chemical process, can be carried out on top of the base electrode and the organic semiconductor without significant degradation of the organic material. Moreover, they have proven that the thickness of the oxide cannot only be tuned precisely by the anodization method (Figure 11), but also that the increased strain during the anodization compared to oxidation in ambient air facilitates the formation of a sufficiently large number of pinholes even in a 50 nm thick base electrode. This approach has also successfully been demonstrated by Liu et al. [105] Creating thicker base electrodes with lower sheet resistance that still possess openings and are perfectly insulated toward the semiconductor can be seen as major step forward in the field of OPBTs.

By all these optimizations, the performance of C$_{60}$-based OPBTs has greatly improved over the years. The most important performance figures are: an on–off ratio of $\geq 10^8$, a maximum on-current density of 1 kA cm$^{-2}$, a transition frequency of 40 MHz, [21] and a current gain of $2.5 \times 10^5$ [99] which corresponds to a transmission factor for electrons through the base of 99.9996%. Thus, OPBTs are clearly among the best organic transistors available today and have even set a new record for the fastest organic transistor. Moreover, keeping in mind that this performance has been achieved for an organic semiconductor material with a vertical charge carrier mobility of only 0.06 cm$^2$ V$^{-1}$ s$^{-1}$ (Figure 10d), the huge potential for future improvements is obvious.

2.3.2. High Current Density and High Speed OPBTs

As mentioned above, OPBTs can be driven at very high current densities at which effects can be observed which usually do not occur in other organic transistors. One of these effects
is the Joule heating of the devices during operation at high current densities. Joule heating is frequently observed in inorganic devices, but for future flexible organic devices this effect is of great importance because of the low thermal conductivity of the organic semiconductor as well as the flexible substrates made from plastics.

Joule heating leads to an increasing device temperature during operation and can be easily observed, e.g., by a thermal camera (Figure 12a). However, as we will see, the temperature increase is highly dynamic during a measurement and it can severely affect important transistor performance parameters such as the transition frequency, which is usually thought to be a static property.

Figure 11. Energy dispersive X-ray spectroscopy (EDX) analysis in TEM using electron transparent cross-sections of OPBTs a) with a 15 nm base layer oxidized in ambient air, b) with a 15 nm base layer anodized at 2 V, and c) with a 50 nm base layer anodized at 4 V. A clear increase in oxide layer thickness can be observed. The oxide thickness is the same above and below the base layer. The SiO layers in (b) and (c) are used for indirect structuring. Reproduced with permission.[99] Copyright 2019, Wiley-VCH.

Figure 12. OPBTs operating high current densities. a) Thermal imaging confirms the increased temperature in the active area of the OPBT. b) Output characteristic of an OPBT revealing S-NDR behavior. At low base-emitter voltages, a voltage sweep (blue lines) is used. In order to stabilize the NDR at base-emitter voltages starting from $V_{BE} = 0.5$ V, a current controlled measurement (blue circles) is used. All curves are measured with forward and backward sweeps, demonstrating the repeatability of the self-heating effect. The model (red lines), assuming an Arrhenius-like temperature activation of the conductivity, leads to a reasonable agreement with the experimental data. The black squared point indicates where the thermal image is taken. Inset: The OPBT shows a nonideal saturation behavior. It can be described by a linear curve with an additional offset. a,b) Reproduced with permission.[98] Copyright 2018, Springer Nature. c) Transconductance versus pulse-biased emitter current and d) intrinsic voltage gain versus pulse-biased emitter current for OPBTs as discussed by Klinger et al.[14,21,98] c,d) Reproduced with permission.[21] Copyright 2018, Springer Nature.
The power generated in a device is given by the product of current and voltage. In case of low power, the heat is effectively distributed during a current–voltage measurement and the device thermalizes to almost the same temperature for each voltage. Once a high power measurement is started, the device temperature starts to increase due to the limited power dissipation, which causes the charge carrier mobility and charge carrier density to increase due to the hopping-like mechanism that governs transport in many organic semiconductor materials. This effect in turn leads to an increasing electrical conductivity and current which eventually results in an increasing power being generated. This so-called positive feedback loop gives rise to the fact that once a critical device temperature is reached, the temperature rapidly increases until the device eventually breaks. The critical temperature in this case is mainly given by the thermal conductivity of the substrate and the semiconductor’s thermal activation energy of electrical conductivity. The influence of this effect on the OPBT performance is shown in Figure 12b. At moderate $V_{\text{BE}}$, the heating effect is small and the device reaches a static temperature during a current–voltage measurement at each point (the power is sufficiently dissipated). At high $V_{\text{BE}}$ though, the heat dissipation via the substrate limits the heat flow and the device starts to show the self-heating effect. As also shown in Figure 12b, the self-heating causes the current and device temperature to run away for a fixed voltage, which manifests itself in a so-called S-like negative differential resistance (S-NDR).[98] Thus, the measurement is not static anymore and a constant-current mode is needed to stabilize the device. An isothermal measurement of the transistor can only be attained in a pulsed measurement mode preventing the heat up of the device. A more detailed view on the self-heating also describing the dynamics of heating is given by Fischer et al.[106,107]

Since the heating effect occurs at high current and power densities (several hundreds of W cm$^{-2}$), it is most relevant for high frequency operation of transistors. Typically, the evaluation of the dynamic properties of a transistor is carried out in a static situation, e.g., measuring the unity-gain cutoff frequency by applying a sinusoidal signal at the gate electrode, or measuring the stage delay in a stable ring-oscillator. Thus, these measurements give the dynamic properties at an unknown device temperature which is higher than the environmental temperature and hence they do not display the true performance of the transistor. In this regard, Kheradmand-Boroujeni et al.[21] developed a special measurement circuit which is able to precisely apply a current and measure a voltage (or vice versa) within 10μs and measure the temporal evolution of the current–voltage characteristics. In this way, the heating effect can be avoided and the device is measured at a defined temperature which enables a small-signal characterization over a $\approx 10$ times wider bias range, with $\approx 10^5$ times less bias-stress effects.

Employing this special measurement setup, Kheradmand-Boroujeni and co-workers measured the small- and large-signal properties of the high-performance OPBTs reported by Klinger et al.[104] almost free of bias-stress and self-heating. As shown in Figure 12c, already for moderate voltages they reached a new speed record for the operation of organic transistors of 40 MHz, which is more than 10MHz above the previous record as visualized in Figure 3. Moreover, this record is reached even at a moderate supply voltage and is only limited by the measurement setup, which is reportedly not able to deliver more than 100 mA at these frequencies. Besides the record, the interesting device physics lie in the temporal evolution of the dynamic properties, which has been recorded by the shift of the base–emitter voltage $\Delta V_{\text{BE}}$ (since the measurement is carried out at constant-current conditions). As shown in ref. [21], the heating effect occurs on the timescale of several hundreds of microseconds, but even on the millisecond- and second-scale a significant shift to the base–emitter voltage is observed. While the effect on the millisecond-scale is assigned to lateral diffusion of charge carriers, bias-stress effects are observed on the second-scale (Figure 12d). Hence, any transition frequency measurement using static conditions would be negatively influenced by these effects, resulting in a considerably underestimated value for the transition frequency $f_t$. Furthermore, the measurement technique proposed by Kheradmand-Boroujeni et al. seems to be much closer to many application situations where only short pulses are applied and hence neither bias-stress nor heating play a role. Most notably, the switching transistor in an AMOLED backplane is only turned on for micro- or even nanoseconds, while it remains off for several milliseconds, allowing the transistor to recover. In this light, the performance of organic transistors, e.g., for AMOLED switching, has been underestimated for years and their capability for these applications should be reconsidered.

The huge potential for OPBTs to be used in high-power and high-frequency applications has very recently been underlined by Dollinger et al.[109] reporting for the first time on the electrical stability of OPBTs under high-power stress conditions. In this publication, Dollinger judged on the device stability by means of the threshold voltage shift $\Delta V_{\text{th}}$ which has been measured under continuous off-state stress (electric field stress at 0.1 MV cm$^{-1}$), but most importantly also under continuous on-current stress at a high current density of 3 A cm$^{-2}$. As shown in Figure 13a, even at a continuous on-current stress for 10$^4$ s, the threshold voltage shift remained below 100 mV. Only at elevated temperature, a stronger thermal activation of the stress has been observed. However, in any case, the threshold voltage shift under stress is reported to be reversible when the device is switched from on- to off-state or vice versa.

Dollinger et al. went also one step further and evaluate how the threshold voltage shift scales with the current densities applied during the stress test (Figure 13b). A linear relation between these quantities was observed. Most importantly though, the magnitude of threshold voltage shift remained far below the shift which was observed under elevated temperature. Thus, they concluded that the electrical stress is mainly activated by temperature and other parameters such as stress current density or illumination are only of secondary importance. A study by Subedi et al. further suggests that traps at the oxide layer, which surrounds the base electrode, play an important role to understand the threshold voltage shift, which is similar to the effect taking place in lateral organic field-effect transistors.[108]

Overall, the stability study by Dollinger et al. impressively shows that optimized OPBT can be very stable under electrical stress. In particular, the strength of the stress effect observed in such OPBTs is on par with best lateral OFETs which are competitive even to polycrystalline silicon transistors.[109]
Another triode-like vertical organic transistor concept similar to the OPBT is the OSIT also known as space-charge-limited transistor or solid-state vacuum triode, which has a structure as shown in Figure 14. However, an important difference is that insulating layers are applied above and below the porous base electrode in order to separate it from the other electrodes. Due to this, OSITs usually show superior off-state performance compared to other vertical organic transistors. Another difference to the OPBT, with its self-assembled porous base electrode, is that the base electrode in OSITs is created by top-down methods, which renders a high degree of process and device control. Apart from that, the selection and optimization of the patterning technique for the formation of the base electrode is vital in order to obtain high performance devices. Hence, we will put a special focus in this section on top-down patterning techniques for OSITs. We will only briefly discuss the OSIT operation since it is rather similar to the OPBT. For a detailed review on the working principles, the reader is recommended to read previous review articles[30,110]

In terms of electrical performance, the OSIT has demonstrated high on–off ratios $\geq 10^5$ and small driving voltages.[111] However, in terms of highest current density, the OSIT can not compete at all with the OPBT due to the superior aspect ratio of the pinholes for the self-assembled base process.

2.4.1. Working Principle and Simulation

Similar to the OPBT, the most essential element in order to understand the device operation of an OSIT is the metal–semiconductor diode. More specifically, the diode is composed of the Schottky-contact at the metal–semiconductor interface and the bulk transport through the semiconductor which is often described by the SCLC model. Also similar to the OPBT, if the combination of metal and semiconductor is properly chosen, the charge carrier injection is expected to be Ohmic and the transport mainly limited by the bulk. Differing from the OPBT though is the size of the openings in the base electrode, which is in the range of 100–200 nm for OSITs. Due to this difference, the potential landscape is also expected to be different compared to the OPBT and therefore has been of high interest for device modeling.

Lin et al. simulated the potential profile between the emitter and collector[110] They reported that the potential between the emitter and collector can be modified by changing the base–emitter voltage to such an extent that the transistor can be switched on and off. In particular, this result proves that the electrostatic field of the base electrode is strong enough in order to fully deplete the 100 nm wide pinholes. They also simulated the potential curve through the central vertical channel of the OSIT. The profile of the potential hardly changes from $-1.5$ to $-5$ V between the emitter and the base. As a result, the remaining voltage only drops across the area between the base and the collector. Since the injection of holes is controlled by the potential distribution between emitter and base, the current saturates for $V_{BE} = -0.6$ V at $V_{CE} = -1.5$ V.

However, such an ideal saturation has not been shown in real OSITs. The reason for this is that perfect insulators are used in the simulation, but they cannot be realized in practice. Also, the pure SCLC-limited behavior is usually not observed in experiments. In particular, for small emitter–collector voltages the devices are still limited by the Schottky barrier, which becomes negligible only at higher voltages and the curves are approaching an SCLC.

Figure 15 shows the experimental output characteristics of an OSIT based on P3HT as organic semiconductor. The simulation as well as the real measurement show the limitation of the SCLC model for large emitter–collector voltages ($< -1.0$ V).
However, for smaller emitter–collector voltages the OSIT shows a steep turn-on behavior which originates from the Schottky-diode at the contacts. Furthermore, due to the larger diameter of the openings and nonideal insulation layers, the OSIT does not reach the saturation regime.

2.4.2. Novel Approaches to Form the Base Contact

One challenge with OSITs is the structuring of the base. This layer has to be perforated with pinholes in the nanometer range. The pinholes should not be too large so that the OSIT can still be turned off, but they also should not be too small in which case they might limit the on-current. Ideally they should have a size of 100–200 nm. In addition, insulating layers have to be applied above and below the base without closing the holes, which makes the base fabrication difficult. New techniques were developed to obtain the desired base and to improve the properties of the transistor. These techniques are highlighted in the following.

One technique is colloidal lithography (compare Figure 16).[112,113] This involves placing tiny PS spheres in a solution and then distributing them over the sample, e.g., by spin-coating. Since the spheres are charged, they repel each other and thus ensure a uniform distribution if their density is chosen appropriately. When the base contact is deposited, the spheres prevent the surface from being covered entirely by the shadowing effect. After evaporation, the spheres are removed and the insulator is etched by oxygen plasma. During this etching process, the remaining base contacts serve as hard-masks helping to form a vertical profile of the etching trenches. With this technique it is possible to prepare pinholes with a diameter of 100–200 nm.

However, there are some disadvantages. Since the spheres are applied either by a dipping or spin-coating process, the distribution of the spheres is often not uniform over the substrate and the spheres might cluster in a particular area with a high density. Furthermore, the pinhole formation process as described above is, strictly speaking, a lift-off process, which is usually avoided in the semiconductor industry due to yield constraints. Overall, this process is considered to have a limited reproducibility and is not suitable for large-area fabrication.

For this reason, new techniques have been suggested for the formation of the pinholes. In order to make the manufacturing process scalable and achieve a greater level of uniformity on a larger area, the PS spheres were applied using blade-coating.[113] In order to prevent the formation of several layers...
of PS spheres, the sample is treated 3 to 4 times with isopropyl alcohol (IPA) and drawn off with blade-coating. This process results in a high density and uniformity over several centimeters on one substrate. The problem with the lift-off step though, is not solved by this process.

In this regard, nanoimprint lithography (NIL) has been proposed in order to circumvent the lift-off\cite{111, 114}. NIL employs a soft stamp in order to stamp the pinhole relief into a patterning layer (denoted as ARC in Figure 17). After patterning transfer into the Al base electrode by wet-etching, the ARC layer is removed from the substrate by oxygen plasma (reactive ion etching (RIE)) while simultaneously creating the pinholes in the bottom layer polymer (PVP in Figure 17). As a last step, the organic semiconductor and the emitter contact are deposited. Overall, the NIL process gives the most reliable device performance and is expected to be favored for potential large scale production. The main drawbacks of the NIL are the expensive preparation of the stamp and the maintenance of the stamp quality.

### 2.5. Novel Approaches

In addition to the already mentioned vertical transistor structures, recently new vertical structures have also been conceived. For the sake of completeness, we will introduce three of these new developments.

#### 2.5.1. Nanopillar-VOFET (NP-VOFET)

The group around Tamer Dogan\cite{115} recently proposed another vertical structure which we have denoted as an NP-VOFET due to its similarity in operation to the VOFET design. In the NP-VOFET, a pillar is formed by means of photolithography and etching, which defines a vertical edge along the direction the charge carrier transport occurs. The source and drain electrodes are positioned adjacent to the pillar edge. They are vertically stacked and separated by the semiconductor layer and an additional insulator (Figure 18b,c). In this way, the device stack resembles a pseudo-VOFET with the gate attached at the side of source and drain electrode.

The process for this NP-VOFET is rather complex. Nanopillars with a high area density (≈10⁶ pillars mm⁻¹) are patterned by structuring a layer of photoresist in a hexagonal lattice structure with a lattice constant of 250 nm and a pillar radius of 100 nm. To create this pattern, they used a heavily doped silicon substrate and employed displacement Talbot lithography (DTL), where the resist dots served as an etching mask during the dry-etching process. The results of this process are highly parallel and uniformly arranged nanopillars (Figure 18a).

In the next step, the entire substrate is covered with an insulating 45 nm thick silicon nitride (Si₃N₄) layer using stoichiometric low-pressure chemical vapor deposition (LPCVD). Afterward the lower gold contact is evaporated serving as the source electrode. During evaporation, some gold accumulates on top of the nanopillars, which increases their radius and ultimately leads to a mushroom-like shape. Due to this shadowing of the material stream, the lower contact forms a trapezoidal shape (Figure 18d).

The same process is also used to apply a 25 nm thick insulating layer of Al₂O₃. By adding more material, the diameter of the nanopillars also increases, resulting in a greater distance between the evaporated layer and the pillars. Figure 18c shows a scanning electron microscope (SEM) image of a nanopillar.

Before the organic semiconductor is applied, the surface is treated with UV light and ozone. In addition, self-assembled monolayers (SAMs) are deposited on the Si₃N₄ dielectric (trimethoxy(octadecyl)silane (OTS)) and on gold (perfluorodecanethiol (PFDT)). Poly [2,5-(2-octyldodecyl)-3,6-diketopyrrolopyrrole-alt-5,5-(2,5-di(thien-2-yl)thieno) [3,2-b]thiophene...
(DPP-TTT) [2] serves as the active semiconductor material which is prepared by spin-coating. It forms a ≈60 nm thick layer on the Al₂O₃, while it is ≈100 nm thick around the individual pillars (Figure 18d). Finally, the drain electrode which is composed of palladium is deposited. A thin silicon oxide layer underneath the drain electrode prevents the diffusion of metal atoms from the palladium into the soft organic layer.

The transistors created in this way have a short channel length of 100 nm. Due to the insulating layers, a high on–off ratio of up to 10⁶ was achieved. Moreover, a switching frequency of 0.1 MHz was reached thanks to the short channel length. Also, a high current density of 0.1 A cm⁻² was obtained due to the compact device design. However, compared to the pseudo-VOFET designs that show a current density up to 50 A cm⁻²,[81] the current in NP-VOFETs is probably restricted by the edge-contact between the semiconductor and the source/drain electrode.

Overall, the performance of these devices is good but not above other vertical transistors. For this reason, more improvements are necessary in order to justify the rather complex fabrication process.

2.5.2. Electrochemical Vertical Organic Transistor

The group around Thomas Weitz developed a radically new transistor structure which can be considered a truly 3D vertical organic transistor.[15] In this structure, the planar gate electrode is replaced by an electrolyte which makes the transistor become a volumetric device (organic electrochemical transistor) rather than a 2D interface device like conventional FETs.

Figure 19 shows the individual manufacturing steps for the new transistor structure. Electrodes for the source and drain were created by electron-beam lithography. The final channel length was determined by the thickness of the insulator layer (here SiO₂) between the drain and source contacts. For adhesion, a thin layer of titanium was applied between the SiO₂ and the gold contacts. SiO₂ and titanium layers between the gold contacts were etched away with a 1% HF acid, so that the upper contact was underetched. The depth d_c can be determined by the etch time. Finally, spin-coating was used to apply the organic semiconductor diketopyrrolopyrrole–terthiophene donor–acceptor polymer (PDPP). The excess semiconductor material was removed by RIE which removes the semiconductor everywhere except between the contacts. The device was completed by casting a drop of the liquid electrolyte 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([EMIM][TFSI]) onto the transistor.

With this structure, a channel length of 40 nm was realized. Due to the high capacitance of the liquid gate, permanent current densities over 2 MA cm⁻² at −0.3 V bias with an on–off ratio of 10⁸ were reached. Also, the operation of the transistor at low voltages (down to 10 μV) was impressive. On the other hand, the high capacitance of the electric double-layer of the electrolyte meant that the switching frequency of the device was small, ≈1 kHz.

2.5.3. 3D Inorganic Vertical Transistor by Ink-Jet Printing

There are also promising developments with regard to printed electronics and inorganic semiconductor materials. Baby et al. successfully built a transistor with a vertical structure and a channel length of less than 50 nm.[116] As ink, they used a metal–organic precursor which they printed on a prepatterned bottom electrode. Before annealing the metal–organic layer, they put an electrode on top (Figure 20b). The sample was then annealed so that the precursor formed a mesoporous oxide semiconductor (in this case SnO₂) as shown in Figure 20c. The size of the porous structure can be changed by the choice of the polymer or by changing the annealing process. Its pores are still sufficiently large so that the printable dielectric (CSPE) reaches all cavities (Figure 20e).

Similar to an organic electrochemical transistor, the charge carrier density in the mesoporous SnO₂ can be effectively modulated by the gate potential. In this way, Baby et al. were able to...
achieve an on–off ratio of $10^8$ and a current density in the range of $100 \ \text{kA cm}^{-2}$. However, similar to the 3D device described in the previous subsection, the high capacitance of the device does not allow for a high switching frequency.

### 2.6. Performance of Vertical Versus Lateral Transistors

A fair comparison of vertical and lateral transistors and even between different vertical transistor concepts is difficult, because such a comparison should not only account for the performance figures such as on–off ratio or transconductance, but should also account for the targeted application, process maturity and technology readiness, and specific advantages of each technology. The latter point concerns, for example, the use of vertical organic transistors in conjunction with OLEDs forming a light-emitting transistor for AMOLED displays.

In this context, the devices reported by McCarthy et al.\(^{[57]}\) are certainly not exceptional vertical organic transistors—however, in combination with the OLED, they enable a unique application which cannot be easily achieved with other transistor architectures.

The second important aspect for a fair comparison, as mentioned above, is the technology readiness and the process maturity. Unfortunately, in this particular case, the development of vertical organic transistors have not reached a satisfying state, which can be seen by the fact that, e.g., not a single ring-oscillator circuit or complementary logic circuit has been reported for vertical organic transistors. There have only been initial attempts to integrate vertical transistors into AMOLED displays.\(^{[57,81]}\) Thus, the reader should keep in mind that although the best lateral organic transistors do not perform as well as the best vertical organic transistors, e.g., with regard to the transition frequency, the technology of lateral organic transistors is mature,
Vertical organic transistors are short-channel devices and hence their main application will be for high-power and high-frequency applications, but not necessarily for, e.g., low-speed, low-power complementary circuits. Therefore, only a couple of device parameters are important, such as transition frequency, device capacitance, etc., while others are only of secondary importance, such as the ideality of saturation and linearity. In the following, we will list the most important performance metrics in order to compare lateral and vertical transistors. This list of metrics is a selection for high-power and high-frequency applications such as wireless communication and high-resolution AMOLED backplane switching. Furthermore, as it will be discussed, there are general performance measures which can be used for comparison without further considerations, and there are specific measures which need to be recalculated depending on the specific transistor architecture.

However, before we discuss these measures, we will briefly focus on a few important definitions which are essential for a fair comparison. For lateral OFETs and pseudo-VOFETs, quantities such as the transconductance or current density are usually given per channel width $W$ or $L_{ov}$, while for, e.g., OPBTs and other vertical transistors these quantities are normalized to the active area $A_{act}$ (Figure 21c). However, these definitions are often misleading and do not reflect the real device dimensions. In particular, there are overlap areas which need to be included when referring to the current density. For this reason, we introduce the technical device area metric which, in our opinion, should be used by researchers in order to guarantee comparability between different transistor technologies. The technical device area for OFETs, pseudo-VOFETs, and triode-like structures such as the OPBT is defined by

$$A_{T} = (W + 2L_{ov})(L + 2L_{ov})$$ \hspace{1cm} (1)

and for the triode $A_{T}^{\text{trio}} = (X + 2L_{ov})(Y + 2L_{ov})$ \hspace{1cm} (2)

assuming that the organic semiconductor is patterned to the size of the gate/base electrode. For simplicity, we assume here that all overlap lengths $L_{ov}$ are equal. Thus, quantities such as transconductance and on-current should ideally be normalized by the technical device area rather than the channel width $W$ or active area $A_{act}$.

After clarifying this definition, we will first discuss the general performance measures. The most important general performance measure is the transition frequency $f_T$, which is defined by the measurement of the unity-gain-condition—or in other words, at which frequency the gate displacement current $i_G$ matches the drain current $i_D$ so that the net gain is zero. Following the definition of the unity-gain-condition, the transition frequency is given by

$$f_T = \frac{g_m}{2\pi C_{tot}} \Leftrightarrow \text{gain} = \left| \frac{i_D}{i_G} \right| = 1 \hspace{1cm} (3)$$

where $g_m$ is the transconductance and $C_{tot}$ is the total device capacitance. In this sense, the transition frequency weights the conductance over the capacitance and hence it is a measure for the effectiveness of the field-effect. Furthermore, the transition frequency accounts for all parasitic effects. For example, the transconductance not only is determined by the charge carrier mobility and channel geometry but it also includes the effect of the contact resistance. Similarly for the total capacitance, not only does the channel capacitance play a role but also parasitic overlap areas due to alignment tolerances. Thus, the transition frequency is a measure that is not forgiving of design mistakes, e.g., too large alignment tolerances or unstructured conductive layers, and hence it is also a good indicator for the quality of device integration. Overall, the transition frequency can be taken without further considerations for the comparison between lateral and vertical transistors. Thus, the speed record of vertical organic transistors (Figure 3) really gives a big benefit over any lateral organic transistor that currently exists.

There are only two situations where care must be taken when comparing $f_T$ of different transistor concepts. First although $f_T$ is normalized to the specific gate insulator capacitance, it is not fully independent of the gate capacitance value since different insulating materials (with different energy gaps) also possess a different dielectric breakdown field. Thus, high breakdown voltage insulators such as Al₂O₃ can be driven at higher voltage (and thus higher charge carrier density) compared to materials with a breakdown at a lower electric field (e.g., PVA).

The second aspect where care needs to be taken when comparing $f_T$ of different transistor concepts is the size of the device. For large devices (large channel width $W$ for OFET and VOFET, or large active area $A_{act}$, e.g., OPBTs), the contribution of parasitic capacitances (due to alignment tolerances, etc.) to the overall capacitance is reduced, which leads to the fact that all OFETs reported with $f_T \geq 20\text{MHz}$ have a channel width of ≥500 μm.\[9,10\] A second effect related to the area is the influence of metal-line excess resistance to the overall device resistance. For large $W$ or larger active area, the width of the metal-lines can be increased, which leads to a reduced resistance and hence higher $f_T$ compared to small devices. In order to define what is a large or small device one has to look at the specific application. For example, for a fast switching transistor for a high-resolution AMOLED display (e.g., 400 ppi), the channel width of the transistor cannot be larger than 10 μm due to the area limitation in the pixel.
The second general quantity is the subthreshold slope SS, which measures the maximum steepness if the transistor is turning from its off- to on-state. This parameter is a measure of how effectively the states at the channel interface can be occupied. Therefore, it is independent of the transistor technology and only a property of the specific semiconductor–insulator interface. The thermodynamic limit of SS at room temperature is \( \approx -60 \text{mV}\,\text{dec}^{-1} \), a value which is reached by lateral OFETs as well as by the best vertical transistors, if optimized interfaces are employed. Nonetheless, for vertical transistors it is in principle more difficult to reach this limit at high drain–source or emitter–collector voltage, respectively. This is due to the drain-induced-barrier-lowering (DIBL), a well-known short-channel effect.

The last general quantities which can directly be used in order to compare lateral and vertical transistors is the on–off ratio. Although, the origin of off-currents in organic transistors are not fully clear (e.g., generation processes, trapping, unintentional doping, parasitic current pathways, etc.), the on–off ratio is often independent of the channel length and width because on- and off-current scale in the same way. However, this statement is not true if the semiconductor covers ungated areas or the base electrode does not fully cover the overlap of emitter and collector (Figure 21). In this case the off-current is significantly increased. For ideal device designs though, comparable values for the on–off ratio of \( \geq 10^8 \) can be reached for lateral and vertical transistors. However, similar to the discussion for the subthreshold slope, short-channel effects can severely deteriorate the on–off ratio in vertical transistors, e.g., due to the DIBL.

Performance parameters such as the on-current density and transconductance are often used in order to highlight the quality of the transistor. These quantities depend on the specific device design and hence they are not suited for a meaningful comparison to other transistors. Instead, renormalized quantities should be used in order to compare vertical and horizontal transistors. As proposed earlier in this article, the current/transconductance should be normalized to the technical device area and not to the active area/channel width (Figure 21). Although, there is nothing technically wrong about the current normalized to the active area, the new definition has the advantage that it accounts for the technical footprint of the device and hence is also an indicator for the integratability of the transistor technology. In particular, the new definition ensures that the current/transconductance and transition frequency go hand in hand. Furthermore, the new definition provides clarity for the calculation of the current density in lateral transistors since the active area is usually not known due to the influence of the contact resistance/injection length.

3. Outlook: Summary and Need for New Materials

Although the first vertical organic transistors were realized not long after the first lateral organic transistors, there was little research done on this new geometry. In the past few years, however, research on vertical organic transistors has rapidly picked up. The most prominent indicators for these developments are the transition frequency and current density records which are now held by vertical organic transistors.

What should be the most important topics of future research? Based on this review, we would argue for the following list:

- In the past few years, a large variety of different structure designs for vertical devices have been made, which has to be seen as very positive. However, in many cases similar structures were named differently. It would be very useful if a unified nomenclature would be agreed upon. A related issue is that many of the structures combine vertical and lateral transport. Here, it would be useful if this is clearly delineated.

- The last decades have seen intensive research toward better materials for organic FETs. However, this work was almost completely dedicated to achieving improved properties in lateral transistor designs. What is needed is research on materials which allow for the full exploitation of the potential of vertical devices. Here, challenges are different as the transport is usually not restricted to a thin layer close to the gate insulator, as is the case in lateral transistors. The fact that records in transition frequency were obtained with mobilities below 0.1 cm² V⁻¹ s⁻¹ indicates the huge potential vertical devices possess with improved mobility. Furthermore, another lesson from the fast OPBT devices is that the development of new materials with an improved vertical mobility is needed. There are basically two approaches: The processing conditions such as the evaporation rate, the substrate temperature, or the use of a seed layer can be utilized to influence the growth of the semiconductor layer. The other approach is to chemically synthesize new materials that form crystals that have higher charge carrier mobility in vertical direction. At the same time, these efforts should also target a lower activation energy of transport in order to suppress destructive self-heating effects at high current densities.

- While vertical devices have already achieved excellent parameters, detailed understanding of device function and charge carrier transport is still limited. In contrast to lateral transistor designs, vertical structures usually have a more complicated geometry and therefore require modeling in higher dimensions. For example, the organic permeable base transistors have a complicated combination of vertical and lateral transport around the pinholes of the perforated base. Similarly, step-edge transistors require involved modeling to correctly describe lateral and vertical contributions to the current flow. Obviously, we need a better modeling of these effects to fully exploit the potential of the device principle. Additionally, in order to develop device simulations quantitatively matching experimental values, experimentalists and theoreticians should develop better methods to determine and model the charge carrier injection in vertical transistors.

- Most of the studies on vertical organic transistors have not addressed the stability of the devices, both in operation and in storage. For meaningful applications though, devices with good threshold stability and little current degradation are needed. Due to the different physics of the devices, one can expect that the relevant effects determining stability will also differ from lateral devices.

- Finally, a significant challenge is to leverage the excellent performance of vertical organic transistors in circuits and
systems. For lateral organic transistors, this has been performed to a significant extent, culminating in designing a microprocessor employing (for the p-type transistors) OFETs.[34] These devices also point to another issue which is crucial for circuit and system design: For complimentary logic, both n- and p-type devices with good performance and controlled threshold voltages are needed.

In summary, we believe that vertical organic transistors are an exciting and quickly growing field of research. There is a multitude of further research challenges in chemistry, physics, and engineering that must be solved to fully exploit the potential of this new class of devices. However, we see a high likelihood that vertical devices may soon make a major impact on the commercial use of organic transistors.

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Equation 3 was corrected on May 15, 2020 after initial online publication.

Conflict of Interest

The authors declare no conflict of interest.

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organic electronics, organic transistors, short-channel transistors, thin-film electronics, vertical organic transistors

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