Impact of structural process variation on junctionless silicon nanotube FET

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Abstract

In this paper, the impact of process variation on the performance parameters of junctionless silicon nanotube field effect transistor (JLSiNT-FET) is studied using 3D numerical simulations. The performance metrics, ON current, OFF current, and unity gain frequency are taken for different physical factors. Sensitivity of the physical factors is computed over a range at various points. The ranking of the structural parameters for various performance metrics is done using a two level full factorial design of experiment method. Overall ranking proposes that the outer diameter of the silicon tube is the most sensitive parameter and inner diameter of the silicon tube is the least sensitive parameter.

Keywords: SiNT-FET, process variation, junctionless

Classification numbers: 1.00, 2.07, 3.02, 5.01, 6.00

1. Introduction

Conventional single gate planar MOSFET has evolved into multi-gate devices such as FinFETs to deal with the short channel effects [1, 2]. Silicon nanotube field effect transistor (SiNT-FET) is known as the advanced version of the multi-gate structures that was explored in 2012 [3]. Since SiNT-FET has the tubular channel controlled by the inner and outer gates, it gives enhanced performance in terms of excellent channel control compared to the silicon nanowire (SiNW) structure [4]. The tunneling operation is realized on SiNT-FET structure in reference [5]. Junction-less operation is realized on the SiNT-FET structure (JLSiNT-FET) in the literature [6] since junction-less transistor has been appeared as one of the most expectant device due to their better immunity to short channel effects (SCEs) and well-matched process flow with the existing CMOS technologies [7].

In the device manufacturing, the process induced variations are inevitable. There have been many literatures available for process variations on MOSFETs and FinFETs [8–11]. Literatures [12, 13] discuss about the sensitivity of the gate-all-around (GAA) MOSFETs to process variations. Analysis of scalability and process variation on SiNW was explored in [14–16]. Process variation study on the vertical SiNW tunnelling FET was done in [15]. Since the SiNT-FET has excellent scalability over SiNW, the impact of the process variation on conventional junction based SiNT-FET is done in [17]. The tube wall thickness and gate length dependencies on the output parameters of JLSiNT-FET are presented in reference [6]. The important physical parameters, silicon tube ovality and gate oxide thickness also influence the characteristics of the device apart from silicon wall thickness and gate length, and hence an organized study of structural process variation together with the important factors such as, silicon tube ovality, gate oxide thickness for inner and outer gates of JLSiNT-FET is to be studied.

In this paper, we have realized the impact of process variation on six important structural factors such as gate length ($L_G$), outer gate oxide thickness ($T_{OX\_OUT}$), inner gate oxide thickness ($T_{OX\_IN}$), silicon tube wall thickness for two cases: (i) for constant outer diameter (OD) and (ii) for constant inner diameter (ID), and silicon tube ovality. The performance metrics such as ON current ($I_{ON}$), OFF
current ($I_{\text{OFF}}$), Threshold voltage ($V_{\text{TH}}$) and unity gain cut-off frequency ($f_T$) are provided. The ranking of the structural factors is done using two level full factorial design of experiments (DOE) method.

The rest of the paper is organized as follows. The device description and calibration are dealt in section 2. Section 3 discusses the sensitivity analysis over a range for different structural factors. The ranking of the structural parameters is done using DOE method in section 4. Finally, conclusions are given in section 5.

### 2. Device structure and $I_D-V_G$ calibration

To execute the simulations, Sentaurus Structure Editor and Sentaurus Device Simulator from TCAD are used. To do the device simulations, Drift-diffusion transport model is used. Normal field degradation, high field saturation, degradation due to doping, degradation due to interface are taken care in the simulations. Carrier carrier scattering, Doping Dependency model, Philips Unified Mobility model and Lombardi models at interface are included in the simulations. Considering the smaller dimensions of the device, Quantum corrections are also included [18]. Based on ITRS standard for the given technology, 50 $\Omega$ resistor is added with source and drain contacts in the electrode section of the simulator during AC analysis.

The device structure and its current-voltage characteristics from [6] are used for the device calibration. JLSiNT-FET device created by TCAD is given in figure 1(a), showing all the regions of the device. JLSiNT-FET with gate oxide and spacer removed i.e. Silicon portion alone is shown in figure 1(b). The schematic vertical cross section of the JLSiNT-FET is given in figure 1(c). The schematic circular cross section of
the JLSiNT-FET is given in figure 1(d). JLSiNT-FET device details are given in table 1. The calibrated $I_D-V_G$ characteristics plot is given in figure 2.

3. JLSiNT-FET structural factors sensitivity analysis

The structural parameters of JLSiNT-FET such as $L_G$, $T_{OX\_IN}$, $T_{OX\_OUT}$, $T_{SI}$ and silicon tube ovality ($\phi$) are varied over a range. Using the sensitivity analysis, these above structural parameters impact on $I_{ON}$, $I_{OFF}$ and unity gain frequency $f_T$ are studied. As already stated in introduction, the $T_{SI}$ can be changed either by changing OD (ID constant), or by changing the ID (OD constant) of the silicon tube.

Sensitivity analysis has been done for one factor at a time with $\pm 10\%$ variations (keeping all other parameters constant). The expression (1) given below is used to compute the sensitivity in which $\Delta y$ is the change in the performance metrics, $I_{ON}$, $I_{OFF}$ and $f_T$ and $\Delta x$ is the change in the structural factors, $L_G$, $T_{OX\_IN}$, $T_{OX\_OUT}$, $T_{SI\_IN}$, $T_{SI\_OUT}$ and $\phi$

$$S_y(x) = \frac{|\Delta y/y|}{|\Delta x/x|}.$$  

3.1 Structural factors impact on $I_{ON}$, $I_{OFF}$ and $f_T$

In this subsection, the impact of structural factors on $I_{ON}$, $I_{OFF}$ and $f_T$ is given. Variation of $I_{ON}$, $I_{OFF}$ and $f_T$ is plotted against $L_G$, $T_{OX\_IN}$, $T_{OX\_OUT}$, $T_{SI}$ and $\phi$, and are given in figures 3–8. The structural parameters values are given in table 2. Their sensitivities are also calculated in this range as given in expression (1) at various points and sensitivity as a function of $L_G$, $T_{OX\_IN}$, $T_{OX\_OUT}$, $T_{SI}$, and $\phi$ are plotted in the graphs (figures 3–8).

As $L_G$ decreases $I_{ON}$ is expected to increase which can be confirmed from figure 3(a) as expected. $I_{ON}$ sensitivity is increased with respect to $L_G$. Figure 3(b) shows the usual $I_{OFF}$ versus $L_G$ characteristics and $I_{OFF}$ sensitivity decreases with respect to $L_G$.

Since JLSiNT-FET has two gate oxides (inner and outer), there are two cases: (i) varying $T_{OX\_OUT}$ ($T_{OX\_IN}$ is constant) and (ii) varying $T_{OX\_IN}$ ($T_{OX\_OUT}$ is constant). Figure 4(a) depicts that $I_{ON}$ and its sensitivity as a function of $T_{OX\_IN}$. It can be observed from figure 4(a) that $I_{ON}$ decreases when $T_{OX\_IN}$ or $T_{OX\_OUT}$ is increasing. $I_{ON}$’s sensitivity is also decreased with respect to $T_{OX\_IN}$ and $T_{OX\_OUT}$. The sensitivity is higher for $T_{OX\_OUT}$ and this is due to the rate of decrease in effective gate oxide thickness is more when $T_{OX\_OUT}$ is increased.
compared to $T_{OX\_IN}$ [17]. The effective oxide thickness is expressed as follows:

$$T_{OX\_OUT} = a_{OUT} \ln \left(\frac{b_{OUT}}{a_{OUT}}\right),$$
$$T_{OX\_IN} = a_{IN} \ln \left(\frac{b_{IN}}{a_{IN}}\right),$$

(2)

where $a_{OUT}$, $b_{OUT}$, $a_{IN}$ and $b_{IN}$ are as shown in figure 1(d).

Figure 4(b) shows $I_{OFF}$ versus $T_{OX}$ plot along with its sensitivity. It can be observed from figure 4(b) that when $T_{OX}$ increases, the channel control by the gates reduces, and hence, $I_{OFF}$ increases. Figure 5(a) gives $f_T$ versus $L_G$ diagram. $f_T$ decreases when $L_G$ increases. The simulation results go with the $1/L_G$ trend with a coefficient value ($R^2$) of 0.98. $f_T$ sensitivity is increasing with respect to $L_G$. Figure 5(b) depicts $f_T$ as a function of $T_{OX\_OUT}$ and $T_{OX\_IN}$. We can see from figure 5(b) that $f_T$ increases with $T_{OX\_IN}$. We can see from JLSiNT-FET structure (figure 1(a)) that the inner gate is covering all drain, channel and source regions and hence the inner associated parasitic is more compared with the outer
gate (outer gate of JLSiNT-FET is covering only the channel portion). When increasing the inner gate oxide thickness ($T_{OX_{IN}}$), the parasitic associated to inner gate reduces. We also know that

$$f_T = \frac{g_m}{(2\pi C_{gg})},$$  \hspace{1cm} (3)

where, $g_m$ is the trans-conductance, $C_{gg}$ is the combination of gate to source capacitance ($C_{gs}$), gate to drain capacitance ($C_{gd}$), and overlap capacitance $C_{ov}$. When $C_{gg}$ reduces, $f_T$ increases which can be confirmed with the figure 5(b). From figure 5(b), it can also be noted that $f_T$ is more sensitive to $T_{OX_{IN}}$ compared to $T_{OX_{OUT}}$.

As mentioned already, the silicon tube thickness can be changed either by changing OD (for constant ID) or by changing the ID (for constant OD). The silicon tube thickness $T_{SI}$ can be changed either by changing OD (for constant ID) or by changing the ID (for constant OD). Channel width is given as $2\pi R$ for outer channel and $2\pi r$ for inner channel where, $R = OD/2$ and $r = ID/2$. For constant ID, to increase $T_{SI}$ the OD should be increased and hence the channel width also increases. This results the current to increase for constant ID. For constant OD, to increase $T_{SI}$ the ID should be decreased and hence the channel width decreases. This makes the current to decrease for constant OD. The above statement is true for the absolute values of current and not true for normalized values of current. Figure 6(a) shows that $I_{ON}$ and its sensitivity as a function of $T_{SI}$. From figure 6(a) it can be seen that the normalization current goes up when $T_{SI}$ increases for both constant ID and constant OD cases. $I_{ON}$’s sensitivity is decreased when OD is constant whereas $I_{ON}$’s sensitivity increased when ID is constant. Figure 6(b) shows that $I_{OFF}$ and its sensitivity as a function of $T_{SI}$. When $T_{SI}$ increases leakage cross section increases, and hence, $I_{OFF}$ increases which can be noted from figure 6(b). $I_{OFF}$’s sensitivity also increases with respect to $T_{SI}$.

Figure 7(a) gives the $f_T$ and its sensitivity as a function of $T_{SI}$. It can be seen from figure 7(a) that the $f_T$ and its sensitivity increase with respect to $T_{SI}$ for both constant ID and constant OD cases. It can be observed from figure 7(a) that for increasing the $T_{SI}$ we need to decrease the ID (for constant OD case), results reduction in inner gate area, and hence one can anticipate the $I_{ON}$ to reduce. But this inner gate area reduction reduces the parasitic associated with that and thereby increases $f_T$. To increase the $T_{SI}$, we need to increase the OD (for constant ID case). This will increase the outer gate area, which will increase the $g_m$ and $C_{gg}$ but $g_m$ takes over $f_T$ to increase.

![Figure 8](image-url) (a) $I_{ON}$ and its sensitivity as a function of ovality; (b) $I_{OFF}$ and its sensitivity as a function of ovality.

![Figure 9](image-url) Individual ranking for structural factors of JLSiNT-FET.
Normally Silicon tube is intended to be a circular shape but because of the critical fabrication procedures, it will end up with oval shape. To capture that effect in device characteristics, the ovality (φ) of the silicon tube is also varied here. When ovality is 1, the perfect circular tube shape will occur otherwise the oval shape will occur. Figure 7(b) shows φ and its sensitivity as a function of OD. It can be noted from figure 7(b) that φ increases due to an increase in the channel width and small reduction in effective oxide thickness with φ. More sensitivity is observed in larger φ. ION and its sensitivity as a function of φ are depicted in figure 8(a). It can be noted from figure 8(a) that when φ increases ION increases due to the channel width increases. When φ = 1, the JLSiNT-FET is more sensitive. IOFF versus φ plot is shown in figure 8(b). When φ increases, the gate control on the channel reduces and so the IOFF increases (from figure 8(b)).

5. Conclusion

In this paper, we have examined the effect of structural factors, LG, TOX_IN, TOX_OUT, TSI, and silicon tube ovality, on the performance metrics, ION, IOFF, SS, VTH, and fT of JLSiNT-FET using 3D numerical simulations. The investigation is done by the three ways: (i) varying the structural factors over a range and finding their impact on each of the performance factors; (ii) calculating their sensitivity by performing ±10% deviations at different points over a range; and (iii) individual and overall ranking of structural factors with respect to each performance metric using DOE method. The results in the overall ranking show that the OD is the most sensitive factor whereas the ID is the least sensitive factor. Ovality is the significant factor next to OD.

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Table 3. Overall ranking for the structural parameters of SiNT-FET.

| Rank | Structural factors |
|------|--------------------|
| 1    | OD                 |
| 2    | Ovality            |
| 3    | TOX_IN             |
| 4    | TOX_OUT            |
| 5    | LG                |
| 6    | ID                |

Based on the β value (coefficient terms), the ranking of structural parameters has been done. Expressions for other performance parameters can also be done similarly. Figure 9 shows the individual structural factors ranks that are computed in the above manner. It can be observed from figure 9 that the OD has occupied the first rank and ID has occupied the last rank on the impact of performance metrics, except for VTH. It is observed that TOX_OUT is more sensitive compared to TOX_IN in the case of ION whereas in the case of fT, it is vice versa.

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In this paper, we have examined the effect of structural factors, LG, TOX_IN, TOX_OUT, TSI, and silicon tube ovality, on the performance metrics, ION, IOFF, SS, VTH, and fT of JLSiNT-FET using 3D numerical simulations. The investigation is done by the three ways: (i) varying the structural factors over a range and finding their impact on each of the performance factors; (ii) calculating their sensitivity by performing ±10% deviations at different points over a range; and (iii) individual and overall ranking of structural factors with respect to each performance metric using DOE method. The results in the overall ranking show that the OD is the most sensitive factor whereas the ID is the least sensitive factor. Ovality is the significant factor next to OD.

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Overall sensitivity of structural factors is calculated by adding all the β values. Adding all the β values and arranging them in the descending order, the overall ranking is evaluated and is given in table 3. One can observe that OD is the most sensitive factor and ID is the least sensitive parameter. Table 3 depicts that the OD and ovality occupy the top two ranks. The last two ranks are occupied by LG and ID.
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