Ultra-High-density 3D vertical RRAM with stacked JunctionLess nanowires for In-Memory-Computing applications

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Abstract—The Von-Neumann bottleneck is a clear limitation for data-intensive applications, bringing In-Memory Computing (IMC) solutions to the fore. Since large data set are usually stored in Non-Volatile Memory (NVM), various solutions have been proposed based on emerging memories, such as OxRAM, that rely mainly on area hungry, one transistor (1T) one OxRAM (1R) bit-cell. To tackle this area issue, whereas keeping the programming control provided by 1T1R bit-cell, we propose to combine Gate-All-Around stacked junctionless nanowires (1JL), and OxRAM (1R) technology to create a 3D memory pillar with ultra-high-density. Nanowire junctionless transistors have been fabricated, characterized, and simulated to define current conditions for the whole pillar. Finally, based on SPICE simulations, we demonstrated IMC scouting logic operations up to three pillar’s layers, with one operand per layer.

Keywords— in/near-memory-computing (IMC), stacked nanowires, junctionless transistors, OxRAM, scouting logic.

I. INTRODUCTION

With the increasing number of connected devices and Artificial Intelligence (AI) applications, the “data deluge” is a reality, making energy efficient computing systems a must have. Unfortunately, the well-known Von-Neumann architecture is computing centric and not data-centric. Actually, data movements in the memory hierarchy result in 50% energy waste [1]. To overcome this limitation, In/Near-Memory Computing (IMC/NMC) rises to be a solution with the co-location of data and logic operations, reducing drastically data movements.

Several IMC approaches can be found in literature, shared between volatile (DRAM or SRAM) and non-volatile memory (Resistive memories as well as charge storage) [2]. Since massive data are mainly stored in Non-Volatile Memory (NVM), they are naturally a good candidate for low-power IMC. In the landscape of the NVM, the RRAM are a promising solution, since they can be scaled down to $10 \times 10^{10}$mm² with a good reliability and low voltage operation [3]. In this context, numerous boolean IMC/NMC approaches based on RRAM have been proposed like [4-7]. Mainly, two concepts are competing: the first one implies read and write operations, based on our new one junctionless nanowire (1JN) with ultra-high density integration (Fig. 1). In addition, uniformly doped nanowires with an excellent electrostatic control have been demonstrated, improving both performance and density [13]. As demonstrated in [14], a high number of stacked Si channels can be used and laterally co-integrated with OxRAM, paving the way for 3D ultra-high-density integration (Fig. 1). In addition, uniformly doped channel without junctions (junctionless) devices have emerged as an alternative to conventional devices due to their ease of fabrication and a higher gate oxide reliability [15].

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Fig. 1: 3D pillar structure scheme with 4 layers, including BL, WL and SL voltages configurations to program (SET/RESET) and read a given bitcell.

In this context, the aim of this article is to demonstrate SCL operations, based on our new one junctionless nanowire (IJN) with one lateral OxRAM (1R) ultra-dense pillar structure presented in section II. In section III, the fabrication and electrical characterization of junctionless transistor is described and TCAD simulation is performed, to define the transistor configuration compatible with the
different OxRAM programming scenarios. The SCL operations in our new pillar structure, is validated with SPICE simulations based on these technological inputs in section IV. Finally, section V concludes the paper.

II. A NEW 3D MEMORY: PILLAR STRUCTURE AND MEMORY OPERATION

The memory technology we consider in this paper mixes at a fine grain level the most advanced and energy-efficient CMOS technology (GAA stacked nanowires) with a lateral OxRAM. The bitcell topology is represented in Fig.1. Conversely to GAA transistors, each source and drain of the stacked nanowires is independent. Thus each nanowire can address an OxRAM, whose materials (oxide and top electrodes) are deposited in a vertical pillar; the bottom electrode of the memory being localized at the drain side of each transistor. So, the final structure includes two times n stacked nanowires with a common gate (WL1, WL2), separate drains (BL1a to BLna, and BL1b to BLnb) and a common pillar called SL gathering the sources.

Programming and read operations on the pillar are performed in a classical manner, like in standard 1T1R memories. SET, RESET or READ voltages are applied on BLs or SLs. The bitcells of the same column which are unused are short circuited, while access transistors of unused columns are off.

Such a memory technology presents the advantages of 1T1R structures with a high integration provided by GAA transistor technology, as long as the transistor features a thin gate oxide (GO1 transistor). This may be possible since GO1 devices already proved their compatibility with OxRAM endurance requirements [16]. In our simulations, four stacks (n=4) are considered but up to seven ones were already demonstrated experimentally [14]. Moreover, in order to extend the up-scaling of such a technology in the vertical dimension, junctionless nanowire transistors are studied in section III. Actually, the integration of junctionless transistor relaxes the constraints in terms of source/drain doping for multiple stacked nanowires (n>4).

III. ANALYSIS OF JUNCTIONLESS DEVICES

A. JunctionLess process flow and performances

To provide insights on the pillar performances, especially on the current driven by junctionless (JL) transistors, a Tri-Gate-JL (TG-JL) NMOS were fabricated. The Si thickness of TG-JL transistors is 11nm with a channel doping of $7 \times 10^{19}$ at/cm$^3$. The gate stack consists of HfO$_2$ dielectrics (equivalent oxide thickness EOT=1nm), 5nm ALD TiN, and polysilicon layers. After the gate patterning, a 8nm SiN spacer is defined. To lower the source/drain access resistance the source and drain are highly doped by ion implantation. The process flow is described in [17] and a device cross-section is given in Fig. 2-(a). To enable read and write operation of RRAM memory, a high drive current is required to set a logic state into the memory element, together with a small ON variability to reduce the resistance distribution. That’s why the drive current and variability of TG-JL were experimentally extracted.

First, the tradeoff between the ON- and OFF-state currents (I$_{ON}$-I$_{OFF}$, see Fig. 2-(b)) shows that in average, devices of 50nm width and 80nm (respectively 60nm) gate length drive 87µA (120µA) ON-current for an OFF current of $10^{-6}$A ($10^{-5}$A) at $V_D$=1.3V and $V_G$=1.5V.

Secondly, as far as global variability is concerned, NMOS shows a threshold voltage $V_T$ (extracted at constant current) of 0.18V and a $V_T$-deviation of 48mV at W=50nm and L=80nm (Fig. 3). It should be pointed out that the higher sub-threshold variability reported for junctionless transistor vs. inversion-mode ones does not translate necessary into a higher ON current variability thanks to screening effects at high gate voltage [17]. From the measured Pelgrom plot (Fig. 4-(a)), we extrapolated a 42mV variation reduction by enlarging the device width to W=75nm. In the next part, the electrostatics and drive current capability for W=75nm Gate-All-Around transistors will be explored with TCAD simulations.

Fig. 3: (a) $I_D$-$V_D$ curves for W=50nm and L=80nm junctionless nMOS at $V_T$=1.3V. (b) $I_D$-$V_D$ curves for W=50nm and L=80nm.

B. Drive current for stacked nanowires (W=75nm)

To have insights on JL drive current in the memory array, TCAD simulations (Fig. 4-(b)) have been performed considering TG-JL and GAA nanowire (GAA-NW) configurations at W=75nm. Sentaurus Device tool from Synopsys was used for this study. Compared to the TG-JL (REF in Table I) at W=50nm, simulated TG-JL at W=75nm drives 50% more current at a slightly higher OFF current. Going to a JL-GAA-NW configuration increases both electrostatic control and drive current (-3 decades on I$_{OFF}$ and +70% on I$_{ON}$). Finally, increasing the channel doping $N_D$ (from $7 \times 10^{18}$ at/cm$^3$ to $10^{19}$at/cm$^3$) enables to increase by +150% the drive current compared to the experimental Ref at the same I$_{OFF}$.

Fig. 4: (a) Experimental pelgrom plot measured for TG-JL nMOS (global variability). (b) REF structure for TCAD simulation with the defined process parameters.
In order to assess the impact of the current delivered by the JL transistors configurations, four SET conditions were considered in the following: weak (70µA), Light typical (100µA), Strong Typical (150µA) and Strong (200µA) conditions.

| Configuration | TG | TG | GAA | GAA |
|---------------|----|----|-----|-----|
| W (nm)        | 50 | 75 | 75  | 75  |
| N₀ (at/cm³)   | 7.10¹⁸ | 7.10¹⁸ | 7.10¹⁸ | 10⁹ |
| log(I_{off}) (A) | -7 | -6.5 | -10 | -7 |
| I₀ @ V_D=1.3V, V_G=1.5V (µA) | 50 | 75 | 86 | 126 |

C. OxRAM distribution extraction

We fabricated OxRAM cells of 10nm HfO₂/Ti 10nm/TIN stack deposition on top of a TiN bottom electrode and arranged into 4kbits 1T1R array (details are given in [18]). Resistance distributions (mean μ and standard deviation σ) for previously defined current compliance are extracted for a T_{pulse}=100ns pulse width and a 2V source line voltage (table II and illustrated in Fig. 8). The RESET conditions for V_{HRS}=2.5V BL voltage and T_{pulse}=100ns corresponds to a lognormal HRS distribution with parameters μ=120kΩ and σ=0.63.

| SET condition | Compliance current (µA) | Resistance parameters μ(kΩ) /σ(kΩ) |
|---------------|-------------------------|-------------------------------------|
| Strong        | 200                     | 5.2/0.58                            |
| Strong Typical| 150                     | 5.7/0.73                            |
| Light Typical | 100                     | 8/1.3                               |
| Weak          | 70                      | 10/2                                |

IV. SCouting Logic in the 1JN-1R Ultra Dense Pillar

In this section, the feasibility of the scouting logic on our 1JN-1R new pillar structure is demonstrated with electrical simulations based on technological inputs. In this aim, 4 SET programming conditions are considered to increase the numbers of functional layers and thus the number of operands processed in parallel.

All the SPICE simulations presented in this section use (1) an OxRAM model based on experimental distributions given in Table II and (2) a transistor model from a commercial design kit emulating the performances of the junctionless nanowire given Table I. Variability is considered up to 6 sigma, and Monte Carlo simulations are performed with 1000 runs.

Fig. 6: Scouting logic results with Light Typical SET on three layers represented according to (a) current distributions and (b) Memory Windows values between current distributions.

Fig. 7: Scouting logic results with Strong SET on three layers represented according to (a) current distributions and (b) Memory Windows values between current distributions.

To implement SCL successfully on a given number of layers, current distributions corresponding to the different combinations of HRS and LRS states must not overlap. Fig. 6-(a) shows the current distributions when 3 layers are activated and a Light Typical SET programming condition is considered. We observe that the third distribution (one HRS and two LRS cells) overlaps, whereas a slightly positive Memory Windows

(MW) is existing for the other cases. Fig. 6-(b) gives for each pair of side distributions the MW value as a positive value, whereas the overlap value is given as a negative value, both expressed in in µA. The same results are presented in Fig. 7, but with Strong SETs. We notice that all MW are preserved, making the implementation of SCL possible.

SCL performance is linked to the number of operands processed in parallel, i.e. the number of layers successfully accessed in parallel without overlap. Thus, a successful operation highly depends on HRS and LRS distributions, and therefore on SET and RESET conditions. However, LRS distributions seems to have a bigger impact on current distributions overlapping [19], as LRS cells conductance is higher.

Fig. 8 shows MW and overlaps for various SET conditions, from one (Fig. 8-(a)) to four (Fig. 8-(d)) activated layers, with V_{SL}= 0.5 V. We notice that, (1) classical read operations (only 1 layer activated) can be achieved by all SET conditions (Fig. 8-(a)), (2) scouting logic can be performed with up to three layers with the two strongest SET conditions, and (3) as expected, MW are higher for stronger SET conditions.

Fig. 8: MW and overlap as a function of SET conditions, on a pillar of four layers, with one (a) to four (d) activated layers @ V_{SL}=0.5V.

V. Conclusion

We proposed a high-density 3D vertical RRAM pillar with stacked Junctionless nanowires (1JN-1R configuration) for In-Memory-Computing purposes. Based on electrical characterization and TCAD/SPICE simulations, we demonstrated the capability of junctionless transistors for performing classical read/write operations, and for delivering sufficient compliance current during SET, enabling SCL with up to three operands. Future work will consider simulations on a whole memory cube with the corresponding periphery to demonstrate the concept on a larger scale.

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