Hardware Acceleration of Explainable Machine Learning using Tensor Processing Units

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Abstract—Machine learning (ML) is successful in achieving human-level performance in various fields. However, it lacks the ability to explain an outcome due to its black-box nature. While existing explainable ML is promising, almost all of these methods focus on formatting interpretability as an optimization problem. Such a mapping leads to numerous iterations of time-consuming complex computations, which limits their applicability in real-time applications. In this paper, we propose a novel framework for accelerating explainable ML using Tensor Processing Units (TPUs). The proposed framework exploits the synergy between matrix convolution and Fourier transform, and takes full advantage of TPU’s natural ability in accelerating matrix computations. Specifically, this paper makes three important contributions. (1) To the best of our knowledge, our proposed work is the first attempt in enabling hardware acceleration of explainable ML using TPU. (2) Our proposed approach is applicable across a wide variety of ML algorithms, and effective utilization of TPU-based acceleration can lead to real-time outcome interpretation. (3) Extensive experimental results demonstrate that our proposed approach can provide an order-of-magnitude speedup in both classification time (25x on average) and interpretation time (13x on average) compared to state-of-the-art techniques.

Index Terms—Hardware acceleration, explainable machine learning, tensor processing unit, outcome interpretation

I. INTRODUCTION

Machine learning (ML) techniques powered by deep neural networks (DNNs) are pervasive across various application domains. Recent advances in ML algorithms have enabled promising performance with outstanding flexibility and generalization. Unfortunately, ML is not able to interpret the outcome (e.g., explain its prediction) since it produces the outcome based on computations inside a “black-box”. This lack of transparency severely limits the applicability of ML. For example, in case of safety-critical applications, a user would like to know the rationale behind its decision to trust its prediction. Similarly, an ML algorithm is expected to provide an outcome (prediction) as well as interpretation of the outcome in many security applications so that a security expert can act judiciously. For example, during malware detection, it is important to know whether a software is malicious or benign. In order to trust the results, it is important to understand the rationale for such a classification. Moreover, the interpretation of the results is crucial to enable the localization (e.g., clock cycle and specific reason) of the malicious activity in a malware [1].

Explainable ML is a promising direction to enable outcome interpretation. There are a large number of existing efforts in the area of explainable ML [2]. Due to inherent inefficiency in these algorithms, they are not applicable in real-time systems. These algorithms treat the explanation process as an extra procedure, and performs the interpretation outside the learning model, which makes them inefficient in practice. Specifically, it solves a complex optimization problem that consists of numerous iterations of time-consuming computations. As a result, such time-consuming interpretation is not suitable for time-sensitive applications with soft or hard deadlines. In soft real-time systems, such as multimedia and gaming devices, inefficient interpretation can lead to unacceptable Quality-of-Service (QoS). In hard real-time systems, such as safety-critical systems, missing task deadlines can lead to catastrophic consequences.

In this paper, we propose an efficient framework to perform explainable ML utilizing Tensor Processing Unit (TPU). TPU is an Application Specific Integrated Circuit (ASIC) developed specifically to accelerate the computations in deep neural networks. TPU has shown great potential in improving training efficiency of various ML tasks [3]–[7]. According to the experimental evaluation in [8], TPU can achieve 15 to 30 times higher throughput compared to contemporary CPU and GPU based acceleration. Our proposed approach effectively utilizes the synergy between matrix based representation of interpretation procedure and TPU-based acceleration of matrix operations. Specifically, this paper makes the following three important contributions.

1) To the best of our knowledge, our approach is the first attempt in TPU-based hardware acceleration of explainable machine learning.
2) Our proposed method exploits inherent advantage of TPU in transforming a complex interpretation process to a simple computation equivalent to one forward pass.
3) Experiments using two popular ML models demonstrate that our proposed approach can provide significant improvement compared to the state-of-the-art methods.

The rest of this paper is organized as follows. We survey related efforts in Section I. Section II describes our proposed method for accelerating explainable ML algorithms using TPU. Section III presents experimental results. Finally, Section IV concludes the paper.

II. BACKGROUND AND RELATED WORK

A. Accelerating Machine Learning using TPU

Tensor Processing Unit (TPU) proposed by Google is a domain-specific hardware for accelerating computation process of deep learning models. There are two fundamental
reasons for the superior performance of TPUs compared to CPU/GPU based acceleration: quantization and systolic array \cite{9}. Quantization is the first step of optimization, which uses 8-bit integers to approximate 16-bit or 32-bit floating-point numbers. This can reduce the required memory capacity and computing resources. Systolic array is a major contributor to TPU’s efficiency due to its natural compatibility with matrix manipulation coupled with the fact that computation in neural networks can be represented as matrix operations. Figure 1 shows an overview of the simplified structure of TPU.

![Image](image.png)

Fig. 1: The structure of TPU, whose key component is the Matrix Multiply Unit (MXU) implemented by systolic array.

From a global perspective, the core of the entire TPU is the Matrix Multiply Unit, which is a 256×256 systolic array composed of multiple computation cells. Each cell receives a weight parameter along with an input signal at a time, and performs accumulation of their products. Once all weights and input signals are propagated to neighboring cells, top to bottom and left to right respectively, it immediately starts next round of iteration. By this calculation scheme, the entire matrix multiplication is actually completed by the collaboration of all computation cells. The systolic array of MXU contains 256 × 256 = 65,536 ALUs, which means that the TPU can process 65,536 8-bit integer multiplications and additions per cycle. Due to the systolic architecture, input data is actually reused for multiple times. Therefore, it can achieve higher throughput while consuming less memory bandwidth. **While TPU has been successfully used for accelerating machine learning algorithms, there are no prior efforts in utilizing TPU for accelerating explainable ML.**

### B. Explainable Machine Learning

The demand for explainable ML has been steadily increasing ever since ML algorithms were widely adopted in many fields, especially in security domains. In this section, we briefly introduce explainable ML, and then discuss one widely adopted explanation technique. In general, explainable ML seeks to provide interpretable explanation for the results of machine learning model. Specifically, given an input instance \( x \) and a model \( M \), the classifier will generate a corresponding output \( y \) for \( x \) during the testing time. Explanation techniques then aim to illustrate why instance \( x \) is transformed into \( y \). This often involves identifying a set of important features that make key contributions to the forward pass of model \( M \). If the selected features are interpretable by human analysts, then these features can offer an “explanation”. Most existing explanation methods exploit the concept of “model distillation” \cite{10}. The basic idea of model distillation is that it develops a separate model called as “distilled model” to be an approximation of the input-output behavior of the target machine learning model. This distilled model, denoted as \( M^* \), is usually chosen to be inherently explainable by which a user is able to identify the decision rules or input features influencing the outputs. In reality, model distillation is composed of three major steps.

- **Model Specification:** To begin with, the type of distilled model has to be specified. This often involves a challenging trade-off between transparency and expression ability. A complex model can offer better performance in mimicking the behavior of original model \( M \). But meanwhile, increasing complexity also lead to the inevitable drop of model transparency, where the distilled model itself becomes hard to explain, and vice versa.

- **Model Computation:** Once the type of distilled model \( M^* \) is determined and corresponding input-output pairs are provided, the model computation task aims at searching for optimal parameters \( \theta \) for \( M \) using Equation 1, which is an optimization problem.

\[
\theta = \arg \min_{\theta} \| M^*(x) - y \| \quad (1)
\]

- **Outcome Interpretation:** Based on the computed distilled model in the previous step, the explanation boils down to measuring the contribution of each input feature in producing the classification result. For instance, assume a linear regression model is applied which can always be expressed as a polynomial. Then by sorting the terms with amplitude of coefficients, we have access to many crucial information including the input features it found to be most discriminatory, and features or output correlations relevant for classification.

Notice that interpreting the distilled model may not provide us with deep insights into the internal representation of the ML model, or demonstrate anything about the model’s learning process, but it can at least provide insight into the correlations and relational rules to explain how the ML model makes a decision. **While explainable machine learning has received significant attention in recent years, to the best of our knowledge, there are no prior efforts in enabling hardware acceleration of explainable machine learning.** The next section describes our proposed approach for TPU-based acceleration of explainable machine learning.

### III. TPU-BASED EXPLAINABLE MACHINE LEARNING

#### A. Overview

Figure 2 shows an overview of our proposed framework for TPU-based acceleration of explainable machine learning. For a specific ML task, we apply traditional training scheme to construct a well-trained model and corresponding input-output dataset. Then we build a corresponding distilled model, which is able to provide reasonable explanation for target model’s behavior. In this work, we consider three major tasks...
to achieve fast model distillation. First, we perform task transformation to map the model distillation problem to Fourier transform computation by utilizing the inherent property of matrix convolution (Section III-B). Next, we develop two synergistic activities to accelerate the computation procedure of Fourier transform using TPUs. The first activity performs data decomposition (Section III-C), where the complete computing task is split into multiple sub-tasks, and each sub-task can be executed by a TPU core without requiring any data exchange between TPU cores (sub-tasks). The other one exploits the TPU’s inherent ability in parallel computation (Section III-D) to process multiple input-output pairs concurrently. Simultaneous execution of these two activities can provide significant improvement in acceleration efficiency, which is demonstrated in our experimental evaluation (Section IV).

B. Task Transformation

As described in Section II, model distillation is applied in our work to provide explanation for a pre-trained ML model. In this section, we demonstrate how to convert model distillation task into a matrix computation. Specifically, model distillation aims at distilling features learned by a complex and cumbersome ML model, and use a lightweight “shadow” model to mimic its input-output mapping behavior, which is called as distilled model. To make the distilled model useful, two crucial requirements need to be satisfied.

- Simplicity: The distilled model should be lightweight and simple. Otherwise it is difficult for users to understand the behaviors of distilled model.
- Compatibility: The type of distilled model should be compatible with the original one. For instance, use of a fully-connected network to approximate a convolution neural network would lead to loss of accuracy.

To satisfy these requirements, our proposed solution consists of the following three steps: model specification, model computation and outcome interpretation.

Model Specification: In this work, a regression model is applied in order to satisfy the two requirements outlined above. Formally, given input data $X$, output $Y$, we need to find a matrix $K$ using Equation 2 where “$*$” denotes the matrix convolution.

$$X \ast K = Y$$

(2)

Intuitively, we are using a one-layer convolution network to approximate the original ML model. First, convolution is a linear-shift-invariant operation, which guarantees the distilled model to be sufficiently lightweight and transparent. Second, a large portion of ML models encountered in reality are mainly composed of convolution layers. Moreover, convolution approximation is a natural fit and is more accurate than naive approaches such as polynomial approximation. Under this scenario, the model computation task boils down to solving for the parameters in matrix $K$.

Model Computation: To solve for $K$, one key observation is that we can apply Fourier transformation on both sides of Equation 2 and by discrete convolution theorem, it gives

$$\mathcal{F}(X \ast K) = \mathcal{F}(Y)$$

(3)

$$\mathcal{F}(X) \circ \mathcal{F}(K) = \mathcal{F}(Y)$$

where $\circ$ is the Hadamard product. Therefore, the solution is given by this formula:

$$K = \mathcal{F}^{-1} (\mathcal{F}(Y) / \mathcal{F}(X))$$

(4)

Outcome Interpretation: The primary goal of explainable ML is to measure how each input feature contributes to the output value. Once $K$ is obtained, the contribution of each feature can be viewed in an indirect way – consider a scenario where we remove this component from the original input, and let it pass through the distilled model again to produce a “perturbed” result. Then by calculating the difference between the original and newly generated outputs, the impact of the key feature on the output can be quantized. The intuition behind the assumption is that hiding important features are more likely to cause considerable changes to the model output. Formally, assume that the input is $X = [x_1, x_2, \ldots, x_{i-1}, x_i, x_{i+1}, \ldots, x_d]$. We define the contribution factor of $x_i$ as

$$con(x_i) \triangleq Y - X' \ast K$$

(5)

where $X' = [x_1, x_2, \ldots, x_{i-1}, 0, x_{i+1}, \ldots, x_d]$, which is nothing but removing the target component from the original input.

As we can see, the original model distillation task has been fully converted into a matrix computation problem, which consists of matrix convolution, point-wise division and Fourier transform only. The first two types of operations are inherently accelerated by TPU’s built-in structure [8]. The next section describes the details for accelerating Fourier transform.

C. Data Decomposition in Fourier Transform

In this section, we demonstrate how to apply data decomposition to disentangle Fourier transform computation, and further utilize TPU’s computation resource to significantly accelerate the computing process. The general form of a 2-D Discrete Fourier Transform (DFT) applied on an $M \times N$ signal is defined as:

$$X[k, l] = \frac{1}{\sqrt{MN}} \sum_{n=0}^{N-1} \sum_{m=0}^{M-1} x[m, n] e^{-j2\pi \frac{mk}{M}} e^{-j2\pi \frac{nl}{N}}$$

(6)

where $k = 0, \ldots, M - 1$, $l = 0, \ldots, N - 1$. If we define intermediate signal $X'$ such that

$$X'[k, n] \triangleq \frac{1}{\sqrt{M}} \sum_{m=0}^{M-1} x[m, n] e^{-j2\pi \frac{mk}{M}}$$

(7)
and plug into Equation \[9\] we have
\[
X[k, l] = \frac{1}{\sqrt{N}} \sum_{n=0}^{N-1} X'[k, n] e^{-j2\pi \frac{nl}{N}}
\] (8)

Notice the similarity between Equation \[7\] and the definition of 1-D Fourier transform applied on a \(M\)-length vector:
\[
X[k] = \frac{1}{\sqrt{M}} \sum_{m=0}^{M-1} x[m] e^{-j2\pi \frac{mk}{M}}
\] (9)

If we treat \(n\) as a fixed parameter, then application of Equation \[7\] is equivalent to performing a 1-D Fourier transform on the \(n\)-th column of the original input \(M \times N\) matrix. Note that for 1-D Fourier transform, it can always be written as a product of input vector and Fourier transform matrix. Therefore, we can rewrite Equation \[7\] as:
\[
X'[k,n] = W_M \cdot x[m,n]
\] (10)
where \(W_M\) is the \(M \times M\) Fourier transform matrix. By varying \(n\) from 1 to \(N-1\) and showing results side by side, we get:
\[
X' = [X'[k,0], \ldots, X'[k,N-1]] = W_M \cdot x
\] (11)

If we treat \(k\) as a parameter and view the definition of \(X'[k,n]\) as the 1-D Fourier transform with respect to the \(k\)-th row of input \(x\), a similar expression can be obtained using the above derivation steps as:
\[
X = X' \cdot W_N
\] (12)
where \(W_N\) is the \(N \times N\) Fourier transform matrix. Using Equation \[11\] the final expression of \(X\) can be written as:
\[
X = (W_M \cdot x) \cdot W_N
\] (13)

This transformed expression indicates that a 2-D Fourier transform can be achieved in a two-stage manner. First, transform all the rows of \(x\) to obtain intermediate result \(X'\). Second, transform all the columns of the resulting matrix \(X'\). An important observation is that the required computation for each row/column are completely independent. This implies that in TPU-based implementation, we can always split the computation process into sub-threads. Given \(p\) individual TPU cores involved and a \(M \times N\) matrix as input, every core is assigned at most \(\frac{\max(M,N)}{p}\) 1-D Fourier transforms workload and can execute in parallel. Our analysis reveals that merging the results afterwards exactly matches the desired 2-D Fourier transform result. Algorithm \[1\] outlines the major steps in data decomposition.

### D. Parallel Computation of Multiple Inputs

In addition to exploiting TPU to accelerate Fourier transform, we make use of TPU’s parallel computing ability to further improve the time efficiency. Notice in the training phase, multiple inputs will be fed into the model to generate corresponding outputs. The above data decomposition technique is applied on each individual input such that the computation cost is distributed among several TPU cores. Extending from single to multiple input is straightforward and only requires one-step further utilization of parallel computation.

An illustrative example is shown in Figure \[3\] where the goal is to perform 1-D Fourier transform on each column of three input matrices. First, each input matrix is segmented into pieces and each core obtains a slice of them. Next, each piece is assigned to a TPU core to perform the Fourier transform. During computation, an internal table is utilized to keep track of the distribution to guide the process of reassembling.

![Fig. 3: An example of parallel computing in TPU. Each input is separated into pieces for multiple cores to run in parallel. The outputs are reassembled to obtain the desired results.](image-url)

In terms of matrix multiplication, the framework is exactly the same except the fact that block matrix multiplication is applied. Original matrices are partitioned into small blocks, then by performing multiplication between blocks and merging afterwards, we achieve same-level of parallel computing efficiency. Due to the data decomposition step applied in Section III-C, the whole computing procedure contains Fourier transform, matrix multiplication and point-wise division only.

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### Algorithm 1: Acceleration of Fourier Transform

**Input:** \(M \times N\) matrix \(x\), number of TPU cores \(p\)

**Output:** 2D Fourier Transform result \(X\)

Initialize each TPU core \(c_1, c_2, \ldots, c_p\)

\(X = 0\)

for each \(i \in [0, \ldots, p-1]\) do

Split \(M/p\) rows \(x_i\) from \(x\)

\(X'_i = \text{Execute}(c_i, x_i)\)

end for

Merge Results: \(X' = [X'_1, X'_2, \ldots, X'_p]^T\)

for each \(j \in [0, \ldots, p-1]\) do

Split \(N/p\) columns \(x'_j\) from \(X'\)

\(X_j = \text{Execute}(c_j, x'_j)\)

end for

Merge Results: \(X = [X_1, X_2, \ldots, X_p]\)

return \(X\)

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which indicates parallelism is maintained across the entire computation process.

In this work, the communication among TPU cores is implemented with `tf.cross_replica_sum` and is required at every iteration of reassembly process to compute the summation of the partial matrices across the cores. The proposed data decomposition and the parallel implementation not only efficiently utilizes TPU’s strength in matrix multiplication but also requires minimal communication time, which leads to drastic improvement in acceleration performance.

IV. EXPERIMENTAL EVALUATION

We evaluated the effectiveness of our TPU-based framework in accelerating explainable machine learning models.

A. Experimental Setup

Experiments were conducted on a host machine with Intel i7 3.70GHz CPU, equipped with an external NVIDIA GeForce GTX 1080 GPU. We utilize Google’s Colab platform to access Google Cloud TPU service. In our evaluation, we used TPUv2 with 64 GB High Bandwidth Memory (HBM), and 128 TPU cores. We developed code using Python [11] for model training and PyTorch 1.6.0 [12] as the machine learning library. Two benchmarks are considered in our experiment.

1) The VGG19 [13] classifier for CIFAR-100 [14] image classification.
2) The ResNet50 [15] network for MIRAI [16] malware detection.

We have used the following three hardware configurations to highlight the importance of our proposed TPU-based acceleration approach. Meanwhile, to address the compatibility of proposed optimization approach (Algorithm 1) and TPU, same optimization methods (data decomposition and parallel computing) are also deployed on CPU and GPU:

1) CPU: Ordinary execution with CPU, which is considered as baseline method.
2) GPU: Model training and outcome interpretation are deployed on the external NVIDIA GPU, which is considered as state-of-the-art ML acceleration technique.
3) TPU: Our proposed approach with fast implementation of explainable machine learning procedure.

The model training process consists of 500 epochs in total, with a mini-batch size of 128. As for result evaluation, we first evaluated classification performance by reporting ML models’ classification accuracy and execution time. Next, we report the average time for completing outcome interpretation step for each configuration. Finally, we present the effectiveness of proposed method in interpreting classification results.

B. Comparison of Accuracy and Classification Time

Table I compares the classification time and accuracy. Each row represents for a specific model structure trained with corresponding hardware configuration. For both training time and testing time, each entry represents time cost of 10 epochs on average. As we can see, with sufficient number of training epochs, all methods obtain reasonable classification accuracy. However, when it comes to time-efficiency, CPU-based approach lags far behind the other two, which achieved the slowest speed. GPU provides accelerated performance, but our TPU-based acceleration provides 65x and 25.7x speedup compared to CPU and GPU based methods, respectively, on VGG19. When it comes to ResNet50, high speedup (44.5x and 23.9x) are also obtained. Such a drastic improvement will also lead to significant energy savings by our proposed approach compared to CPU and GPU-based methods.

C. Scalability of Outcome Interpretation

In this section, we demonstrate the efficiency of our proposed method on explaining ML models. The average time for performing outcome interpretation for every 10 input-output pairs is presented in Table II. The VGG19 result demonstrates that the proposed method is 36.2x and 11x faster than CPU and GPU based approaches, respectively. As expected, the improvements are even higher in case of ResNet50, where 39.5x and 13.6x speedup obtained over CPU and GPU based approaches, respectively.

Aside from the overall efficiency analysis presented above, we also randomly select several matrices with varying sizes and compare time efficiency in Figure 4. It is expected that the time will increase with the increase in the size of the matrices. Figure 4 demonstrates that our proposed approach is scalable compared to the other two methods. There are two reasons for the scalability of our approach. (1) Our approach utilized data decomposition technique to break larger matrices into smaller sub-matrices. (2) Another dimension of improvement comes from the fact that these smaller sub-matrices are distributed across multiple MXU inside each TPU core. This drastically reduces the bandwidth requirement during the computation and leads to a significant improvement in computation speed. For matrices in the size of 1024 × 1024, proposed method is more than 30x faster than the baseline method. This indicates that for training and outcome interpretation on large-scale neural networks (tens of thousands of matrix operations involved), our proposed method can save hours of computation time, which will lead to significant energy benefit.
In this section, we provide two examples from two different domains (image classification and malware detection).

Figure 5 shows an example of interpreting the classification results for a picture from CIFAR-100 dataset. We segmented the given image into square sub-blocks, and the explainable ML framework is applied to compute contribution factor of each individual block towards the classifier’s output, so that it can illustrate what part is crucial for the classifier to distinguish it from other categories. In the given picture, the cat’s face (central block) and ear (mid-up block) are the keys to be recognized as ‘cat’.

![Fig. 5: Interpretation of CIFAR image’s classification](image)

Let us consider an example on malware detection from ResNet50. The ML-based detector receives running data of MIRAI malware \[16\] as input in the format of a trace table, where each row represents the hex values in a register in specific clock cycles (each column represents a specific clock cycle). Figure 6 shows a snapshot of the trace table.

![Fig. 6: Interpretation of MIRAI malware traced signals](image)

Our proposed method computed the corresponding contribution factor of each clock cycle towards the output using model distillation. Contribution factors are shown as weights in the last (colored) row. Clearly we can see that the weight of $C_2$ is significantly larger than the others. By tracing the execution, it has been shown that $C_2$ corresponds to the timestamp of assigning value to the variable “ATTACK VECTOR” in Mirai. This variable records the identity of attack modes, based on which the bot takes relative actions to perform either a UDP attack or DNS attack. This attack-mode flag is the most important feature of a majority of malware bot programs, and our proposed method successfully extracted it from the traces to illustrate the reason for classifying it as a malware. This interpretation will not only provide confidence in malware detection but also helps in malware localization.

### V. Conclusion

While machine learning techniques are popular in many domains, they have two major limitations in real-world applications: long running time and lack of transparency. In this paper, we address these fundamental bottlenecks using TPU-based hardware acceleration of explainable machine learning. While acceleration improves the classification time, model distillation provides the explainability (transparency) of the classification results. Our proposed method made two important contributions. First, it effectively converts the model distillation problem to linear algebra computation. As a result, it is able to fully exploit TPU’s inherent ability in computing ultra-fast matrix operations. Next, it enables parallel computing by performing data decomposition to break a large matrix into multiple small matrices. Experimental results on a diverse set of benchmarks demonstrated that our approach is scalable and outperforms state-of-the-art acceleration techniques for explainable machine learning. Specifically, our TPU-based acceleration provides drastic improvement in classification time (25x on average) as well as interpretation time (13x on average) for both image classification and malware detection benchmarks over GPU-based acceleration.

| Model  | CPU  | GPU  | TPU  | Impro./CPU | Impro./GPU |
|--------|------|------|------|------------|------------|
| VGG19  | 550.7 | 168  | 15.2s | 36.2x      | 11x        |
| ResNet50 | 1456.1 | 502  | 36.8s | 39.5x      | 13.6x      |
| Average | 1003.4 | 335  | 26.4s | 38.6x      | 12.8x      |

### TABLE I: Comparison of accuracy and classification time for various benchmarks

| Model  | Accuracy (%) | Training-time(s) | Testing-time(s) | Accuracy (%) | Training-time(s) | Testing-time(s) | Speedup./CPU | Speedup./GPU |
|--------|--------------|------------------|-----------------|--------------|------------------|-----------------|--------------|--------------|
| VGG19  | 94.06        | 24.2             | 10.9            | 92.09        | 8.1              | 5.8             | 0.4          | 0.14         |
| ResNet50 | 78.99       | 176.2            | 129.8           | 86.87        | 109.7            | 55.0            | 4.3          | 2.60         |
| Average | 86.52        | 100.2            | 70.35           | 89.47        | 58.9             | 30.4            | 1.37         | 54.7x        |

### TABLE II: Average time (seconds) for outcome interpretation
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