Si$_{0.97}$Ge$_{0.03}$ microelectronic thermoelectric generators with high power and voltage densities

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Microelectronic thermoelectric generators are one potential solution to energizing energy autonomous electronics, such as internet-of-things sensors, that must carry their own power source. However, thermoelectric generators with the mm$^2$ footprint area necessary for on-chip integration made from high thermoelectric figure-of-merit materials have been unable to produce the voltage and power levels required to run Si electronics using common temperature differences. We present microelectronic thermoelectric generators using Si$_{0.97}$Ge$_{0.03}$, made by standard Si processing, with high voltage and power generation densities that are comparable to or better than generators using high figure-of-merit materials. These Si-based thermoelectric generators have <1 mm$^2$ areas and can energize off-the-shelf sensor integrated circuits using temperature differences ≤25 K near room temperature. These generators can be directly integrated with Si circuits and scaled up in area to generate voltages and powers competitive with existing thermoelectric technologies, but in what should be a far more cost-effective manner.
The development of miniature (<1 cm² total area) silicon integrated circuit (IC) sensors and networking devices for a broad range of internet-of-things (IoT) applications has spurred the question of how to provide reliable and sustainable power to such ICs. IoT devices are often intended to be embedded in enclosed environments not meant to be routinely accessible, such as inside a heating system or buried under pavement, where utility line power is unavailable, changing batteries is impractical, and there is insufficient light for photovoltaics. Many IoT devices must then be energy autonomous. That is, they must carry with them a small, renewable energy source, preferably integrated on the same chip or in the same package. Consequently, significant interest has developed in small microelectronic thermoelectric generators (µTEGs) as one method to power energy autonomous IoT devices wherever a reliable thermal gradient exists.

Most current research on thermoelectric (TE) technology concentrates on developing new materials having a high TE figure-of-merit $ZT = (S^2/κT)$, where $S$, $κ$, and $T$ are the material’s thermoelectric power factor, electrical conductivity, and thermal conductivity, and $T = \frac{1}{2}(T_C + T_H)$ is the mean temperature between a cold reservoir at temperature $T_C$ and a hot reservoir at $T_H$ (in Kelvin). This focus on complex high $ZT$ materials is because a TEG’s ideal thermodynamic efficiency increases with the $ZT$ of the materials used to form the thermopile. Modern high $ZT$ materials such as PbTe, the BiSbTe system, CuI, Heusler alloys, SnS$_2$, Se$_2$, CsSnI$_3$, Cl$_2$, Cu$_3$Te-Ga$^{19}$, and dichalcogenides generally aim to achieve $ZT \approx 1$ for $T$ near 300 K.

Higher efficiency means less heat is drawn to generate a given power. Maximizing efficiency is important if the total heat capacities of the $T_H$ and $T_C$ reservoirs are small enough that the heat flow from $T_H$ to $T_C$ significantly decreases the temperature difference $ΔT = (T_H - T_C)$. However, for µTEGs the heat flow cross-section is small, so little heat is typically drawn, and the $T_H$ and $T_C$ heat capacities are usually very large or have actively maintained temperatures. In this case efficiency may not be the primary concern. The critical criterion is the ability to directly energize an IoT device or trickle charge its battery when operating from commonly encountered $ΔT$s between 10 to 50 K with $T_C$ near room temperature. In practice this means generating voltage $>1.5$ V with $≥$ several $μA$ of current (i.e., several $μW$ of power). This voltage is required to cross the threshold that turns on Si transistors or to push charge into a typical battery. Because material Seebeck coefficients are typically $~0.1$ mVK$^{-1}$, producing $>1.5$ V from $ΔT = 10$ K requires a thermopile connecting $~10^3$ thermocouples in series. TEGs using bulk high $ZT$ materials need areas of several cm$^2$ to accommodate this many thermocouples. Small area (≤ few mm$^2$) high $ZT$ TEGs, which are desirable for integration with IoT devices, have yet to reach this voltage/current threshold using $T_C$ near 300 K and moderate $ΔT$ $~ 20$ K. Furthermore, high $ZT$ materials can be expensive to synthesize, often contain toxic or non-earth-abundant elements, and are incompatible with Si IC processing, all of which increase the cost-per-Volt and cost-per-Watt generated.

In this article we report small area (≤1 mm$^2$) µTEGs with Si$_{1-x}$Ge$_x$ as the TE material, fabricated using standard Si IC processing. These µTEGs can generate power densities (per unit area for heat flow) comparable to or better than high $ZT$ TEGs and can energize IoT devices from commonly encountered $ΔT$s. These µTEGs build on the alternative approach to Si-based µTEGs we recently reported to overcome silicon’s inferior $ZT$.

This approach emphasizes application of device physics and circuit engineering principles to optimize a µTEG’s generated power density at given $ΔT$, rather than focusing on thermodynamic efficiency. This strategy exploits the ability of Si processing to fabricate thermopiles consisting of a very large number of TE elements in a small area, thereby producing a high total power density despite relatively low power per TE element, and to control parasitic thermal and electrical resistances.

**Results**

**Description of µTEG device structures.** Two types of µTEG devices were made, test mode and harvest mode, all fabricated on an industrial 65 nm node Si IC process line. The test mode device structures and measurement protocols are identical to those detailed in refs. 22,24. Design and fabrication details for the harvest mode devices are given in Methods and in Supplementary Fig. 1. Each test mode device constitutes a thermocouple having total cross-sectional area of $48 \mu m \times 36 \mu m$ with an on-chip integrated resistive heater as the $T_H$ reservoir. The purpose of the integrated heater is to give a highly reproducible series thermal impedance between heat source and thermocouple. This facilitates de-embedding the thermocouple’s intrinsic performance characteristics from parasitic thermal impedances. However, most µTEG applications require harvesting heat from an off-chip $T_H$ source. Harvest mode µTEGs omit the integrated heater and instead connect a thermopile thermally (but not electrically) to a thermal contact pad on the chip surface. A heated copper rod placed on this pad acts as the $T_H$ reservoir, so the thermal impedance depends sensitively on the quality of the contact between Cu rod and thermal pad.

Operating from $T_C$ near 300 K and $ΔT$ between 5 to 50 K, test mode µTEGs were designed to optimize power density, not voltage. By contrast, harvest mode µTEGs were designed to maximize voltage density rather than power and so consist of 640 thermocouple unit cells (each with area of $19.8 \mu m \times 15.7 \mu m$) connected in series. As the following results show, operating from nearly the same $T_C$ and $T_H$, test mode devices generated power density $~6x$ higher than harvest mode, while harvest mode devices generated voltage density $~3.6x$ higher than test mode.

The basic TE elements of both test mode and harvest mode devices are 80 nm wide $× 700$ nm long $× 350$ nm tall blades of Si$_{1-x}$Ge$_x$, where $x$ is nominally 0, 0.01, 0.02, and 0.03. To maintain compatibility with standard Si IC processing, bulk Si$_{1-x}$Ge$_x$ could not be used. Instead, as described in Methods, Ge was incorporated into the top surface of a 300 nm diameter Si wafer by ion implantation followed by activation anneal. For reasons given in Methods, this restricted the maximum usable Ge concentration to $x \leq 0.03$.

Si$_{1-x}$Ge$_x$ was used because both bulk and nanostructured Si$_{1-x}$Ge$_x$ show significantly enhanced Z compared to pure Si due to suppression of the phonon contribution to $κ$ through random alloy and grain boundary scattering. A large amount of TE device work using Si$_{1-x}$Ge$_x$ exists, particularly targeted at high temperature applications. These works generally use alloy compositions with $0.2 ≤ x ≤ 0.5$ because $κ$ is near its minimum value through that range. However, the majority of the decrease in $κ$ with increasing $x$ occurs in the narrow range going from $x = 0$ to $x = 0.05$. This suggests that a significant increase in $Z$ and hence TE performance may be expected using only a few % Ge.

**Performance characteristics of test mode µTEGs.** Figure 1a shows power–current–voltage ($P–I–V$) characteristics at various $ΔT$ ($T_C = 300$ K) of the test mode Si$_{0.97}$Ge$_{0.03}$ µTEG with the highest power density. The thermopile design for this specific µTEG is given in Supplementary Fig. 2. Three nominally identical devices were tested; all had $P–I–V$ characteristics within 5% of each other. As $ΔT$ increases, the linear $I–V$ offsets further from the origin. The source resistance is $R_S = |ΔV/ΔI| = 5.2$ $Ω$. The open-circuit voltage, $V_{OC}$, and short-circuit current, $I_{SC}$, are the intercepts of the $I–V$ lines with
the V and I axes, respectively. The generated power $P = VI$ has maximum $P_{\text{max}} = V_{\text{OC},\text{SC}/4}/A = V_{\text{OC}}/4R_S = \text{power delivered to a load}
resistance $R_L = R_S$ known as matched load conditions. Figure 1b shows $V_{\text{OC}}$ is linearly dependent on $\Delta T$, with the slope of the linear fit giving the Seebeck coefficient of the TEG device, $S_{\text{TEG}} = V_{\text{OC}}/\Delta T = 0.173 \text{ mVK}^{-1}$. Figure 1c shows $P_{\text{max}}$ is linearly dependent on $(\Delta T)^2$. The slope of the fitted line $= 1.45 \times 10^{-3} \text{ mWK}^{-2}$ gives the power per square of temperature difference. Normalizing to the 48 $\mu$m × 36 $\mu$m heat cross-sectional area gives the specific power density, $I_P = 84 \text{ Wcm}^{-2}K^{-2}$, $I_P$ measures $P_{\text{max}}$ normalized to both TEG area and operating $\Delta T$. Figure 1d plots how $I_P$ and $S_{\text{TEG}}$ increase with x for four $\mu$TEGs having the same design as the $\mu$TEG of Fig. 1a, but different x. For this $\mu$TEG design, $I_P$ increases by x factor of 3.5 x and $S_{\text{TEG}}$ approximately doubles as x goes from 0 to 0.03. $I_P$ does not exactly scale with $S_{\text{TEG}}^2$ because $R_S$ increases by $\pm 10\%$ with Ge content over this range.

For the TEG device $V_{\text{OC}} = S_{\text{TEG}}\Delta T$, but at the level of the thermopile itself, $V_{\text{OC}} = S\Delta T_{TP}$, where $S$ is the net Seebeck coefficient of the TE material and $\Delta T_{TP}$ is the actual temperature difference across the TE blades forming the thermopile. Because of parasitic thermal impedances between hot/cold reservoirs and the TE blades, $\Delta T_{TP} < \Delta T$, and for pure Si $(x = 0)$ thermopiles we estimated$^{23}$ that $\Delta T_{TP}/\Delta T = 0.10$ to 0.18. For Si$_{1-x}$Ge$_x$, literature values show that the TE material $S$ is insensitive to $x$ between $x = 0$ and 0.03$^{23,31}$. Consequently, the increase in $S_{\text{TEG}}$ with x from Fig. 1d indicates that $\Delta T_{TP}$ must nearly double (at same applied $\Delta T$) as x increases from 0 to 0.03 due to a decrease in TE material $S$ with increasing Ge content.

For each value of $x$, we tested sixteen $\mu$TEG layout design variations. Layout structure variations explored different number of TE blade elements per unit area, different electrical lead and contact configurations, and different heat exchange structures to thermally couple to the $T_{H}$ reservoir, but all used the same TE blade size and n- and p-dopant densities. For any given layout, $I_P$ increased monotonically with increasing x, with $I_P(x = 0.03)$/$I_P(x = 0) = 2.5$ to 3.5 depending on layout design. Among the 16 different $\mu$TEG layouts with $x = 0.03$, the variant used for Fig. 1a gave the highest $I_P$, the variant with the lowest $I_P$ generated 5 $\mu$Wcm$^{-2}$K$^{-2}$, and the plurality of layout variants gave $I_P$ between 20 to 30 $\mu$Wcm$^{-2}$K$^{-2}$. Higher $I_P$ layouts were associated with two features. First, they had electrical and thermal lead/contact configurations that gave lower parasitic series resistances. Second, they came closer to using an optimum number of TE blade elements to maximize $V_{\text{OC}}/R_S$ by properly balancing the trade-off between using fewer TE blades to increase the thermopile’s thermal resistance to increase $\Delta T_{TP}$ and hence $V_{\text{OC}}$, and using more TE elements to decrease the thermopile’s $R_S$.$^{24,34}$

In situations where the thermal reservoirs have large heat capacities or where $T_H$ and $T_C$ are actively maintained, $I_P$ may be a more practically important metric than efficiency. $I_P$ can be used to compare power generation capability across different types of TEGs. For example, from its data sheet$^{21}$ a high ZT TEG of 9 cm$^2$ area generates $P_{\text{max}} = 0.41$ W from $T_H = 110 \degree C$ and $T_C = 50 \degree C$, so its $I_P = 12.7 \mu$Wcm$^{-2}$K$^{-2}$, $I_P$ values compiled from summaries$^{7,35-37}$ of (Bi$_2$Sb)$_3$(Te$_2$Se)$_3$ TEGs range from 1 to 20 $\mu$Wcm$^{-2}$K$^{-2}$ for commercial devices and up to $\sim 100 \mu$Wcm$^{-2}$K$^{-2}$ for research devices. Thus, the $I_P = 84 \mu$Wcm$^{-2}$K$^{-2}$ for our Si$_{0.07}$Ge$_{0.93}$ $\mu$TEG is competitive with the best high ZT TEGs from the standpoint of areal power density produced using the same $\Delta T$.

Performance characteristics of harvest mode $\mu$TEGs. Figure 2a illustrates the cross section of a harvest mode $\mu$TEG. Details of the harvesting $\mu$TEG measurement protocol are given in Methods. The top of a harvest mode thermopile is thermally connected (but electrically isolated) through an integrated heat exchanger to an Al coated thermal contact pad, shown in Fig. 2b. The heat exchanger consists of several layers of interdigitated Cu

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**Fig. 1** Performance of test mode $\mu$TEG with highest power density. a Power-current-voltage data with $T_C = 300 \degree K$ and $\Delta T = 3.8 \degree K$ (purple diamonds), 7.7 K (blue circles), 11.6 K (green triangles), and 16.1 K (red squares). Open symbols are voltage data (left axis) and filled symbols are power = VI data (right axis). Dashed lines are linear (for I-V) and quadratic (for I-P) least-square fits to the data. b Open circuit voltage $V_{\text{OC}}$ vs. $\Delta T$. The dashed line is a linear least-square fit. c Maximum power, $P_{\text{max}}$, as determined from the data in a. vs. $(\Delta T)^2$. The dashed line is a linear least-square fit. d Specific power density, $I_P$ (green squares, left axis) and TEG device Seebeck coefficient, $S_{\text{TEG}}$ (red circles, right axis) vs. Ge percentage x for four $\mu$TEGs having the same device layout as the one represented in a. The solid lines simply connect data points.
electrodes, one set extending up from the thermopile and the other extending down from the thermal contact pad, spaced by a dielectric stack consisting of relatively high thermal conductivity Si₃N₄/SiC layers.

Harvest µTEGs were designed to generate high voltage density rather than high \( I_p \), so they consist of many small thermocouple unit cells connected electrically in series and thermally in parallel. Figure 2c depicts the design of one such unit cell. Each unit cell is built using the same size, shape, and dopant density TE blade elements as test mode devices, but has fewer blades per unit area to facilitate the multiple series electrical connections needed to increase output voltage. Since the n-side blades are connected electrically in parallel, as are (separately) the p-side blades, fewer blades result in higher resistance per unit area and hence lower output current and power density. A complete harvest mode µTEG is composed of 640 unit cells covering a total heat flow cross-sectional area of 0.64 mm × 0.32 mm, the same as the surface Al thermal contact pad.

Figure 3a shows \( P–I–V \) characteristics of a Si₀.⁹Ge₀.⁰³ harvest mode µTEG whose unit cell design is depicted in Fig. 2c. A heated Cu rod touching the thermal contact pad served as the \( T_H \) source. Details of the measurement protocol are given in Methods. Figure 3b plots \( V_{OC} \) vs. \( \Delta T \) to obtain the total Seebeck coefficient \( S_{tot} = 0.102 \text{VK}^{-1} \) for the 640 unit cells in series. We found \( S_{tot} \) could vary between 0.07 to 0.11 \text{VK}^{-1} depending strongly on how well the Cu rod contacted the thermal pad. From Fig. 3b, the Seebeck coefficient per cell is then \( S_{cell} = S_{tot}/640 = 0.16 \text{mVK}^{-1} \). The source resistance of this harvesting µTEG is \( R_S = 76 \text{kΩ} \). Among harvesters tested of identical design, \( R_S \) was between 75 to 77 kΩ independent of Cu rod contact conditions. The resistance per unit cell is \( R_{cell} = R_S/640 = 120 \text{Ω} \). The harvester’s \( R_{cell} \) is greater than the test mode’s \( R_S \) because the test mode thermocouple consists of 20× more TE blades connected in parallel, reducing the test mode’s source resistance and increasing its \( I_{SC} \) compared to the harvest device. If we scale \( R_{cell} \) to the same number of blades in parallel as the test mode device, the harvester’s per-cell resistance would then be \( R_{cell}/20 = 6 \text{Ω} \), slightly more than the \( R_S = 5.2 \text{Ω} \) for the test mode device from Fig. 1a. Previous modeling of \( x = 0 \) test mode devices estimated the parasitic resistance from leads and contacts to be \( \sim 2 \text{Ω} \) per thermopile. Harvest mode devices may have a somewhat higher parasitic resistance per cell due to the additional leads and contacts needed to connect multiple thermocouple cells in series, connections not needed in test mode device.

**Energizing IoT devices.** Using \( \Delta T \) from 20 to 25 K, these harvest µTEGs could energize commercial Si ICs made for low-power IoT applications. Figure 4a illustrates a harvest µTEG connected as the unregulated power input to a BQ25570 power management integrated circuit (PMIC). The PMICs are widely used to support energy autonomous electronics by producing a regulated output voltage \( V_{out} \) from an unregulated, high source resistance input \( V_{in} \) and storing excess input energy by charging a capacitor or backup battery. The BQ25570 was run without a battery and so used only the electrical input from the µTEG. To initiate a cold start from the state where the PMIC is fully discharged required operating the µTEG with \( \Delta T = 29 \text{K} \) to charge the PMIC’s storage capacitor up to \( V_{stor} = 4.2 \text{V} \). This stored charge is used to regulate \( V_{out} \). After cold start, the PMIC operated continuously with \( \Delta T \) as low as 24 K. Figure 4b plots the PMIC’s steady-state \( V_{out} \) and \( V_{stor} \) vs. load resistance \( R_L \), with µTEG operating from \( \Delta T = 24 \text{K} \). The PMIC was configured to produce a regulated \( V_{out} = 1.80 \text{V} \), which it could do for \( R_L \geq 0.900 \text{MΩ} \), corresponding to a maximum output current of 2 \text{μA} \. For \( R_L < 0.900 \text{MΩ} \), the load’s
connections between a hot Cu rod, thermal contact pad, by the OPT3001 in response to a red light-emitting diode (LED) and a white Δ operating from output.

energize a commercial OPT3001 visible light sensor intended for speci OPT3001 directly from the µTEG and found it operated within power to perform its regulation functions, we tried powering the it ran stably using ΔT = 24 K. If this µTEG/PMIC configuration were energizing a real device having a variable load resistance, the device would either be fully on (when Rₐ > 0.90 MΩ) or fully off (when Rₐ < 0.90 MΩ), as Fig. 4b shows a very sharp transition between Vₒut = 1.80 V and Vₒut = 0 V. In a real situation, operational continuity would be maintained when Rₐ drops below 0.90 MΩ (or when ΔT drops to <24 K) by using a backup battery with the PMIC.

Figure 4c illustrates a harvest µTEG connected directly to energize a commercial OPT3001 visible light sensor intended for use as an IoT sensor. The sensor’s data sheet specifies a minimum input voltage and current of 1.6 V and 1.8 µA. We first powered the OPT3001 using the µTEG via the PMIC output, and it ran stably using ΔT = 24 K. Because the PMIC needs to draw power to perform its regulation functions, we tried powering the OPT3001 directly from the µTEG and found it operated within specified tolerances using ΔT down to 22 K. This was the smallest ΔT at which the harvester could generate both the minimum voltage and the minimum current needed to for the OPT3001 to operate within specifications. (From Fig. 3b, using ΔT = 17-18 K would generate VₒC = 1.8 V, the same as the PMIC output voltage used to energize the OPT3001, but at zero current.) Fig. 4d shows the OPT3001’s light intensity readings when powered by the µTEG is identical to its readings when powered by a conventional DC power supply. Further details on the operation of the BQ25570 and OPT3001 using the µTEG are given in Methods.

Discussion

The µTEGs in this work use small footprint areas appropriate for on-chip or in-package integration with energy autonomous IoT ICs. Given the highly parallel nature of Si fabrication over a 300 mm diameter Si wafer, there are no significant technical barriers to scaling such µTEG designs to much larger areas. For example, using an appropriate photolithography mask set, Si IC fabrication...
could make over 5 × 10^8 replicas of the thermopile used for Fig. 1 within a 9 cm² area without adding processing steps or increasing process time or cost. Comparing to the same area bulk high ZT material TEG of ref. 21 operating from the same ΔT = 60 K, a Si_{0.97}Ge_{0.03} TEG would generate optimal power of 2.7 W compared to the 0.41 W for the bulk TEG. Perhaps as importantly, industrial Si processing uses widely abundant materials and has a much higher production volume throughout than any other material technology, so the cost-per-watt generated with a Si-based TEG should be substantially lower than with any other TE material.

All our µTEG devices were designed to be tested on a wafer probe station with the probe station chuck as \( T_C \) reservoir, so both thermal interfaces were incompatible with standard IC chip package heat exchangers. Looking towards the future, engineering thermal interfaces to optimize heat exchange between a µTEG’s hot and cold thermal contacts and application-specific \( T_H \) and \( T_C \) reservoirs will be critical to advancing practical use of µTEGs in energy autonomous devices. The goal is to minimize parasitic series and contact thermal impedances and to maintain uniform heat distribution throughout the µTEG thermopile across the interface. Low thermal impedance chip packages\(^{10}\) designed to remove heat from power ICs to a cold reservoir could conceivably be adapted for use with a µTEG’s cold side contact. Solutions for the hot side contact are less straightforward as there is little established work aimed at directing external heat into an IC chip.

Assuming thermal interface issues can be solved, these Si based µTEGs could energize IoT ICs and sensors using a \( T_C \) near 300 K and ΔT of 20 to 25 K. Several conceivable IoT environments can generate such temperature profiles, such as the temperature differences between the exterior (\( T_C \approx 273 \) K) and interior (\( T_H \approx 295 \) K) of a heated building in winter, or between subsurface earth (\( T_H \approx 285 \) K) and roadway pavement (\( T_H \approx 310 \) K)\(^{3}\). Using µTEGs for biothermal energy harvesting presents a more difficult challenge, since ΔT between core human body temperature and an air-conditioned room is about 10 to 15 K, and ΔT between skin surface temperature and ambient air is usually taken to be ≤ 5 K\(^{41}\). Because TEG power generation scales as \((\Delta T)^2\), reducing ΔT from 20 K to 5 K using the same TEG device reduces power output by a factor of 16. The Si based harvest mode µTEG design from Fig. 1 would then require a total \( T_H \) area of 16 × 0.2 mm² = 3.2 mm², not too much larger than the 1 mm² desired for integrated energy autonomous devices. This area could be further reduced by increasing the number of TE blade elements in each unit cell of this harvest mode µTEG design.

### Methods

#### General µTEG design and processing

All µTEGs were fabricated on an industrial 65 nm node technology silicon complementary metal-oxide-semiconductor (CMOS) process line. The 100 mm diameter Si wafers used for device fabrication. Designs comply with all standard design rules, including minimum feature areas, line-widths, and aspect ratios, and used only material sets and dopants normally available for commercial Si CMOS device fabrication. These design rules ensure process compatibility with all other CMOS devices and circuits that could be fabricated on the same wafer.

The front surface of each blank wafer was protected with a 50 nm thick thermal oxide. Then a thin surface Si_{0.97}Ge_{0.03} alloy layer was created using a blanket (unmasked) Ge ion implantation followed by activation anneal. Three consecutive implant energies & dosages were used to form a Si_{0.97}Ge_{0.03} layer: (1) 100 keV & 1 × 10^{14} cm⁻², (2) 200 keV & 6 × 10^{13} cm⁻², and (3) 270 keV & 2.4 × 10^{15} cm⁻², followed by a 1050 °C activation anneal for 20 mins. Simulations of Ge density vs. depth into the wafer surface are shown in Supplementary Fig. 3. The freely available Monte-Carlo based Transport of Ions in Matter (TRIM) application\(^{22}\) was used to model the as-implanted Ge distribution, but it does not simulate annealing.

A Technology Computer Aided Design (TCAD) semiconductor process simulator\(^{23}\) was also used to estimate implanted Ge distribution after annealing, using published values of thermal diffusion coefficients for Ge in Si\(^{44}\). Results indicate the Ge density is between 1 to 2 × 10^{13} cm⁻² to a depth of ~ 250 nm. Nominal 3% Ge corresponds to a Ge density of 1.5 × 10^{13} cm⁻², and the base of the NiCr layer that form the thermopile structure are etched down to a nominal depth of 350 nm.

Post-anneal optical microscope inspection using a Schimmel defect etch and stain\(^{24}\) showed no detectable defects resulting from the implantation. However, for \( x > 0.03 \) the surface Si_{1-x}Ge_x layer resulted in sufficient bowing of the wafers that the wafer curvature, very high resolution, shallow depth-of-focus photolithography needed could no longer be done with adequate precision. This prevented us from going higher than 3% Ge content.

The fundamental thermopile elements were nanostructured blades formed by the boron and phosphorus ion implantation and Si etch process normally used to create isolation trenches for Si CMOS transistor circuits in this process technology. Doped n-type blades were etched from n⁺-wells formed by P and As ion implantation (dopant concentration 3.9 × 10^{18} cm⁻³), and p-type blades were etched from p⁺-wells formed by B ion implantation (dopant concentration 4.3 × 10^{18} cm⁻³). Each individual blade was nominally 80 nm wide × 750 nm long × 350 nm tall, although cross-sectional scanning electron microscope (SEM) images\(^{22}\) showed the actual blades to be slightly trapezoidal in cross section. An 80 nm width was used as it is the minimum width that can be reliably etched to form a 3- dimensional structure using 65 nm node process technology. SiO₂ filled the space between n-type and p-type blades for mechanical support. Each blade was electrically and thermally contacted individually from the top using a tungsten (W) plug. The blades were electrically contacted from the bottom using commercial n⁺- and p⁺-well contacts formed by a mesh of silicide lines in each well. The silicide mesh was used to minimize the parasitic series spreading resistance through the relatively high resistivity doped silicon wells to the metal electrode. A heated rod made of oxygen-free high conductivity (OFHC) copper brought thermal contact to each unit cell of a harvest mode µTEG. Cu metal layers and vias were used to connect all n-type blades electrically in parallel, and, separately, all p-type blades electrically in parallel. The n-type side and the p-type side were then connected electrically in series to form a thermopile.
of chuck temperature always agreed with the chuck’s embedded thermistor to within ±0.2 K, so the chuck’s embedded thermistor was used to determine $T_c$.

### Integrated circuit measurement protocol

Both the BQ25570 and the OPT3001 ICs were purchased solder-mounted onto evaluation module (EVM) printed circuit boards. The EVMs brought the IC’s input and output pins out to convenient wiring terminals and provided resistor networks and jumpers to select various function settings. For both ICs, the power input ($V_{in}$) terminal on the EVM was wired directly to the probe station probe contacting the n-contact on a harvesting mode $\mu$TEG, and the circuit common (GND) terminal on the EVM was wired directly to the probe station probe contacting the p-contact on the same harvesting mode $\mu$TEG. Total external wiring resistance was $<2 \Omega$, negligible compared to the 76 kΩ resistance of the $\mu$TEG.

For the $\mu$TEG, no back-up battery was used. Energy was stored using the 4.8 μF storage capacitor that came mounted on the EVM. Without a back-up battery and with no charge on the storage capacitor, the BQ25570 needed to be “cold-started” by first charging the storage capacitor before it began delivering output power. The cold start needed a minimum $\Delta T=29$ K applied to the $\mu$TEG. Settings on the BQ25570 were configured so that it began delivering regulated output voltage of 1.80 V when the voltage on this storage capacitor reached 4.2 V (its minimum setting), which ended the cold start phase. After cold start, the BQ25570 delivered a steady-state regulated 1.80 V output with a $\Delta T=24$ K applied to the $\mu$TEG. The BQ25570 was also configured to maximize power input from the $\mu$TEG by dynamically adjusting its input resistance to match the $\mu$TEG’s source resistance, thereby transferring $P_{\mu\text{TEG}}$ from the $\mu$TEG. Finally, the output terminals on the EVM were directly wired to a variable MΩ resistor box used to vary the load resistance. Voltmeters monitored the output voltage across the resistor box as well as the voltage across the storage capacitor to generate the data in Fig. 4b of this paper.

For the OPT3001, the EVM normally connects to a computer through a USB interface that powers the sensor and sends serial digital data from the sensor to the computer. The data is processed by an executable program into light intensity (in units of lux). For this experiment, the $V_{in}$ terminals on the EVM were not connected to the USB interface but were instead wired to the $\mu$TEG as shown in Fig. 4a. The OPT3001 EVM was mounted in fixed position inside an opaque box with a red light emitting diode (LED) light source inside the box and a portal through which a white flashlight could be shone onto the sensor. Light intensity levels were recorded in the dark, with the red LED on, and with the flashlight on. The OPT3001 operated stably through the BQ25570 using $\Delta T$ as low as 22 K applied to the $\mu$TEG, or directly from the $\mu$TEG using $\Delta T$ as low as 22 K. To compare whether the measured light intensities were reliable when using the experimental thermoelectric energy source, we repeated light measurements with the sensor energized using a conventional wall-plug powered DC power supply using the voltages specified in the sensor’s technical data sheet.

### Data availability

The data that support the findings of this study are available from the corresponding author on reasonable request.

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Author contributions

R.D., P.M., and G.H. carried out the experiments, analyzed results, and helped write the paper. H.E. conceived the nanoblade µTEG devices. K.M. and H.E. designed the device layouts. K.M. performed thermal simulations on the designs. H.E., J.D., and T.T. developed processing recipes and supervised fabrication of the wafers. H.E. and M.L. analyzed results and conceived further experiments and measurements. M.L. designed and set up measurements, performed calculations, and drafted the paper. All authors coedited the manuscript.

Competing interests

T.T., K.M., and H.E. are employed by Texas Instruments Incorporated. J.D. performed this work as an employee of Texas Instruments Incorporated. The remaining authors declare no competing interests.

Additional information

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