Low Power Inductorless LNA using Noise Cancellation Technique for UWB Applications

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Abstract. This paper deals with the performance analysis of low power (LP) Low noise amplifier (LNA) for Ultra wide band (UWB) applications. The proposed inductorless LNA has two stages, one is complementary common gate (CCG) stage and the other one is body biased common source stage (BBCS). In CCG stage current reused techniques is used to reduce the power consumption and to provide broad band impedance matching in UWB band. Apart from this, CCG stage is also used to reduce the noise of BBCS stage using noise cancellation technique. BBCS stage is used to provide high and flat gain. Biasing voltage is optimized through body voltage. The proposed LNA was successfully simulated in 45-nm CMOS technology. All the simulations have been done for a range of frequency 3GHz to 8GHz in cadence virtuoso. The proposed LNA achieved a peak power gain (S21) of 17.1dB and -16.4dB S11, at frequency 4.1GHz. The bandwidth of proposed LNA is 3.7GHz - 5.5 GHz, -9.9dBm IIP3 with minimum NF is 1.1dB. The proposed LNA consumes a power of 3.6mW with supply voltage 1V.

Keywords: Low-noise Amplifier (LNA), Ultra Wide Band (UWB), Noise figure (NF), Body biased common source (BBCS), Complementary common gate (CCG).

1. Introduction

A rapid incremental demand of wireless sensing network in the field of internet of things (IoT), required a frontend circuit which is compact in size and consumes as little power as possible. The scaling in CMOS technology can be utilized in both the areas for compactness of device modeling and low power. But, it creates a challenge to use of existing circuit topology and degradation in mobility, velocity saturation, transit frequency and output conductance [1-2]. The low noise amplifier (LNA) has different set of specification for low power (<1mW) as compared to typical LNA, designed for wideband matching, high gain, low noise and good linearity. The low power LNA is always used as first block of receiver in low data-rate application where high NF is tolerated for low power consumption [3]. The designing of LNA for low value of power is always a challenging and active research topic in industry as well as in academia. A number of well-known topologies has been proposed in literature. Figure 1(a) represents common gate (CG) wide band LNA with T-matched input network [4]. The LNA has been designed for Ultra wide band (UWB) range and the flat gain is achieved as inductors L1 and L4 resonate with internal parasitic at lower and upper corner frequency.
This LNA has very low power consumption, less than 1 mW but quoted a very low gain 7.9dB and large chip area (0.73mm\(^2\)). Therefore, cannot be used in area sensitive applications.

Since inductor consumes a large area, a compact inductorless shunt feedback LNA has been proposed by Mahdi et al [5] as shown in Figure 1(b), in which a feedback between input and output is utilized for low power input matching. Current efficiency is also improved due to the feedback current utilized by main transistor. The LNA consumes very low power (0.4mW) due to low transconductance (g\(_{m}\)) and has low chip area (0.0052mm\(^2\)), but it all comes at the cost of poor NF (4.9dB) and low IIP\(_3\) (-13dBm). Since NF is directly affected by the influence of the voltage gain of circuit and has inverse relation. Belmas et al [6], present an inductorless Gm-boost CG LNA shown in Figure 1(c). This LNA has less power consumption and low NF but the LNA has very low IIP\(_3\) of -13dBm[6]. Bruccoleri et al [7] present a LNA as shown in Figure 1(d) in which the noise of CS stage is reduced with the help of CG stag. The presented LNA is very good in metric of NF and gain but it suffers from high power consumption (35mW). A number of different techniques on noise cancellation have been proposed but they had the drawback of either linearity or power consumption [8-10]. Therefore, this paper deals with a design technique to improve the performance of LNA in terms of low NF and low power consumption with broad band matching. The proposed LNA has a current reused technique, in which both MOS, connected in cascode and share the common bias current, beneficiary for low power. A parallel combination of BBCS and CCG stages improve the NF by noise cancellation throughout the wide band. The rest of the paper progresses as Section 2 deals with design challenges and technique of low power LNA. Section 3 presents the description of the proposed LNA. Section 4 describes the simulation results and comparison of the proposed work with other cited work, while conclusion of proposed LNA is in Section 5.

![Figure 1. Schematic of ULP LNA in state of art (a) Input T-matched wideband CG LNA. (b) Shunt feedback LNA. (c) Gm boost CG LNA (d) Block diagram of noise cancellation of LNA](image)

### 2. Design challenges and techniques of low power LNA

This section deals with low power design technique and challenges to optimize the biasing voltage. Then for optimization of the power, a complementary common gate current is reused along with body biased CS has been discussed

#### 2.1. Design challenges of low power

As the applied voltage is reduced to get the objective of low power, MOS transistor moves from strong inversion (SI) to weak inversion (WI). LNA performance is degraded in term of different parameters such as transit efficiency (g\(_{m}\)/I\(_D\)), intrinsic voltage gains (g\(_{m}\)/g\(_{ds}\)), transition frequency (f\(_T\)). Therefore, an optimized biasing metric is required, to get the value of drain to source voltage (V\(_{DS}\)) and gate to source voltage (V\(_{GS}\)). Which include the effect of above specified parameters. An extended biasing metric [\((g_{m}/g_{ds})+ (g_{m}/I_{D}) + (f_{T})\)] with respect to inversion coefficient (IC) is shown in Figure 2 and has been designed for CS amplifier in 45 nm CMOS technology for different value of V\(_{DS}\). All the formulations with all notations is shown in Table 1.

| Table 1 Expression for Inversion Coefficient (IC) |
Name of Parameters and their symbols

| Parameter                              | Symbol |
|----------------------------------------|--------|
| Inversion coefficient                  | \( IC \) |
| Drain-source current                   | \( I_D \) |
| Transistor size aspect ratio           | \( W/L \) |
| Technology Current                     | \( I_{D0} \) |
| Substrate factor                       | \( n_0 \) |
| Low-field mobility                     | \( \mu_0 \) |
| Gate-oxide cap.                        | \( C_{ox} \) |
| Thermal voltage                        | \( U_T \) |
| Body-effect factor                     | \( \gamma \) |
| Source bulk voltage                    | \( V_{SB} \) |
| Substrate doping concentration         | \( N_{SUB} \) |
| Silicon intrinsic carrier concentration| \( N_I \) |
| Psi parameter                          | \( \psi_0 \) |
| Fermi Potential                        | \( \phi_F \) |

Formulation

\[
IC = \frac{I_D}{I_{D0}}
\]

\[
I_{D0} = 2n_0 \cdot \mu_0 \cdot C_{ox} \cdot U_T^2 \left( \frac{W}{L} \right)
\]

\[
n_0 = 1 + \frac{\gamma}{2 \sqrt{\psi_0 + V_{SB}}}
\]

\[
\psi_0 \approx 2\phi_F + 4U_T
\]

\[
\phi_F = U_T \cdot \ln \left( \frac{N_{SUB}}{n_i} \right)
\]

If the value of IC<0.1, transistor is in weak inversion (WI), moderate inversion (MI) for 0.1<IC<10 and in strong inversion (SI) for IC>10. A significant downfall can be observed in performance as \( V_{DS} \) shift from 0.6V to 0.2V [11-12]. The numeric value of drain to source voltage \( V_{DS, sat} \) and gate to source voltage \( V_{GS} \) can be obtained from \( V_{DS, sat} = 2U_T \sqrt{IC + 0.25} + 3U_T \) and \( V_{GS} = 2nU_T \ln(e^{\sqrt{IC}} - 1) + V_{TH} \cdot \)

![Figure 2. Extended biasing metric for an NMOS transistor in 45-nm for different value of \( V_{DS} \).](image)

### 2.2. Complementary common gate current reused

A popularly design technique used in low power analog circuit implementation is current reuse [13-14]. In current reuse technique transistors shared the common biasing current. Henceforth, reduction in power consumption or improving in efficiency is noticed. Complementary MOS structure has additional advantage of high voltage gain and low value of overall noise [15-16]. A Complementary current reused structure as shown in Figure 3(a) and (b) in which NMOS (M1) and PMOS(M2) transistors shared the common biasing current. Since structure in Figure 3(b) has advantage over the structure Figure 3(a) that the output current of shunt transistor M3 or M4 can be reused with the input stage if connected in feedback configuration. Therefore, in the proposed LNA,
structure Figure 3(b) has been used due to better reuse of current or more beneficiaries for low power application.

![Figure 3: Inductorless CCG architecture](image)

**Figure 3.** Inductorless CCG architecture (a) Inverter type NMOS-PMOS structure (b) NMOS-PMOS flipped structured

2.3. **Forward body biased CS structure**

Since the objective is low power and compact in size with low NF as much as possible. Therefore, in the proposed LNA design body biased CS structured is used in sub threshold conduction region [17-18]. Transconductance ($g_m$) and threshold voltage ($V_{TH}$) in weak inversion is given by equation (1) and (2)

$$g_m = \frac{I_{D0}}{nU_T}(e^{(V_{CT}-V_{TH})/2nU_T})$$  \hspace{1cm} (1)

$$V_{TH} = V_{TH0} + \alpha(\sqrt{2\phi_F-V_{BS}} - \sqrt{2\phi_F})$$  \hspace{1cm} (2)

Where $\alpha$ is process dependent body effect parameter and $\phi_F$ is the substrate Fermi potential. Variation in $g_m$ with $V_{TH}$ is given by equation (3)

$$\frac{\partial g_m}{\partial V_{TH}} = \frac{I_{D0}}{2(nU_T)^2}(e^{(V_{CT}-V_{TH})/2nU_T})$$  \hspace{1cm} (3)
Figure 4. Transconductance ($g_m$) for different value of body to source voltage ($V_{bs}$)

Since the $g_m$ is exponential increase with decrease in $V_{TH}$. While $V_{TH}$ can be reduced with increased value of body to source voltage ($V_{bs}$). Transconductance ($g_m$) can be varied and controlled with variation in $V_{bs}$, a graph of $g_m$ is shown in Figure 4 for different value of $V_{bs}$ from 0V-0.4V. The body voltage is fed with six bit DAC have an LSB of 0.015V to control the threshold voltage.

3. Design analysis of proposed LNA

The schematic of proposed LNA as shown in Figure 5 and its equivalent in Figure 6. The LNA consists of two stages one is forward body biased CS stage, providing sufficient amount of gain and consumes very low power because MOS ($M_3$) is biased in WI region. The Input and output characteristics of transistor $M_3$ can be controlled by forward body biased (FBB) generated by externally DAC signal. The second stage is the CCG stage, very good for input impedance matching because input impedance is mostly independent from various transistor parameters and numerically equivalent to inverse of transconductance. As both transistors $M_1$ and $M_2$ share the common biased current, therefore, power consumption is in available power budget. CCG stage and the body biased CS stages are connected in parallel, have two merits of advantage. First one is the final voltage gain of the proposed LNA, is the sum of individuals one and second is the, CCG stage and is utilized to improve the noise figure by noise cancellation technique. A detailed analysis of input impedance is required for matching henceforth improvement in bandwidth, voltage gain and noise equations of individual stage and cancellation are as follows:
3.1 Input Impedance.

Input impedance $Z_{in}$ as shown in Figure 6 given by equation (4).

$$Z_{in} = \frac{1}{s(C_{g_{m1}} + C_{g_{r2}})} \left( \frac{(R_1||R_2)(g_{dr1} + g_{dr2} + 1)}{g_{m1} + g_{m2} + g_{dr1} + g_{dr2}} \right)$$

(4)

Where $g_{m1}$, $g_{dr1}$ and $C_{g_{m1}}$ is the transconductance, drain to source conductance and gate to source capacitance of Mi transistor. If the drain to source conductance is ignored as compared to transconductance, input impedance $Z_{in}$ is equivalent to $\frac{(R_1||R_2) + 1}{g_{m1} + g_{m2}}$. A $50\,\Omega$ impedance matching can be obtained for just half value of transconductance as compared to conventional CG stage. Therefore, saving in power consumption. Internal parasitic play vital role at high frequency so it becomes important to choose the value of load resistance $R_1$ and $R_2$ in such a way that $50\,\Omega$ matching is obtained throughout the desired band of interest.
3.2 Voltage gain

As total voltage gain of the proposed LNA is the sum of gain of CCG path and forward body biased CS path. The gain of CCG path is given by

\[
A_{\text{CCG}} \approx \left( \frac{R_L (g_{m1} + g_{m2} + g_{d1i} + g_{d2i})}{1 + R_L (g_{d1i} + g_{d2i}) (1 + sC_{gs})} \right) \left( \frac{g_{m5} (r_{ds4} \parallel r_{ds5})}{1 + g_{m5} (r_{ds4} \parallel r_{ds5})} \right)
\] (4)

Where \( R_L \) is the parallel combination of \( R_1 \) and \( R_2 \), at low frequency and assume \( g_{d1i} \) and \( g_{d2i} \) is very low gain of CCG stage approximately equivalent to \( (R_1 \parallel R_2) (g_{m1} + g_{m2}) \).

Gain of forward body biased CS path is given by

\[
A_{\text{CS}} \approx \frac{1}{2} g_{m3} R_3 \frac{g_{m4}}{g_{m5}}
\] (5)

Total voltage gain \((A_T)\) of proposed LNA is sum of both the stage given by equation (4) and (5) and represent by equation (6) given below

\[
A_T \approx \left( \frac{Z_L (g_{m1} + g_{m2} + g_{d1i} + g_{d2i})}{1 + Z_L (g_{d1i} + g_{d2i}) (1 + sC_{gs})} \right) \left( \frac{g_{m5} (r_{ds4} \parallel r_{ds5})}{1 + g_{m5} (r_{ds4} \parallel r_{ds5})} \right) + \frac{1}{2} g_{m3} R_3 \frac{g_{m4}}{g_{m5}}
\] (6)

Total gain as given by equation (6) can be increased with large value of \( g_{m1} \) and \( g_{m2} \) but decreases in the value of input impedance given by equation (4). Therefore, a trade-off required between impedance matching and gain of the LNA.

3.3 Noise analysis and reduction technique of proposed LNA.

The main noise contributor in the proposed LNA is the channel noise \((\overline{i_n^2} = 4KT \frac{\gamma}{\alpha} g_m \Delta f)\) of transistors and thermal noise \((\overline{i_n^2} = 4KT \frac{1}{R} \Delta f)\) due to passive resistive element where \( \gamma \) denotes the thermal noise coefficient and \( \alpha \) is the ratio of \( g_m \) and \( g_{d0} \). Since noise of first stage only plays the significant role. Therefore, noise factor mainly has the term of channel noise term of transistor M1, M2 and M3 and the thermal noise term of \( R_1 \) and \( R_2 \) and \( R_8 \) and given by
The second term in the equation (7) is represents noise due to transistor M$_1$ and M$_2$ while noise contributed by load is given by the third term and the fourth term is the noise contributor of M$_3$ transistor. Since the noise of first stage play dominant role in NF. Therefore, noise of M$_4$ and M$_5$ can be ignored in noise factor analysis. The body biased CS stage can be used to reduce the noise generated by CCG stage because voltage generated at terminal A and B as shown in Figure 7 are in 180° phase and can be explained as:

Noise voltage at terminal $V_A = i_{n2}(Z_m \| R_s) \approx i_{n2} \frac{1}{g_{m1} + g_{m2}}$ (8)

Noise voltage at terminal $V_B \approx -i_{n2}(1 - g_{m2} R_s / 2)R_2$ (9)

![Figure 7. Schematic of noise cancellation technique.](image)

Where, $i_{n2} = \sqrt{\frac{4KT\gamma}{\alpha}} g_{m2}$. Since the noise voltage $V_A$ is amplified by forward body biased CS stage and $V_B$ is passed through the transistor $M_t$ therefore total noise voltage ($V_T$) at output terminal is given by

$$V_T = A_{CS} V_A + \beta V_B e^{j\Delta \theta}$$ (10)

Where $\beta$ is given by $\frac{g_{m5}(r_{ds} \| r_{os})}{1 + g_{m5}(r_{ds} \| r_{os})}$ and $\Delta \theta$ assumes the phase mismatch between the body biased CS stage and CCG stage. Equation (10) can be elaborated after getting the value of $V_A$ and $V_B$ from equation (8) and (9) and given by

$$V_T = i_{n2} \frac{1}{g_{m1} + g_{m2}} A_{CS} - \beta i_{n2}(1 - g_{m2} R_s / 2) R_2 e^{j\Delta \theta}$$ (11)
Noise contributor can be minimized if real part of $V_T$ becomes zero in equation (11) which requires the condition as

$$\frac{1}{g_{m1} + g_{m2}} - A_{CS} = \beta (1 - g_{m2}R_g / 2)R_g \cos(\Delta \theta)$$

4. Results and Discussion

In this section simulations for $S$-parameters, NF, linearity, have been done. All simulations have been done for UWB range (3GHz-8GHz) and mathematically correlated with mathematics as explained in Section-3. Process Corner and Monte-Carlo is also simulated to verify the robustness of the proposed LNA.

4.1 $S$-Parameters

It is observed reflections increase at high frequency. Therefore, it is important to study the simulations behavior of power gain and reflection at high frequency. Figure 8(a) represent the power gain ($S_{21}$) and input reflection coefficient ($S_{11}$) with respect to frequency range of 3GHz to 8GHz. The $S_{21}$ is positive and $S_{11}$ is negative throughout the frequency range. The maximum and minimum range of $S_{21}$ and $S_{11}$ is 17.1dB, and -16.4dB at frequency 4.1GHz.

![Figure 8. S-Parameters of proposed LNA (a) S$_{21}$ and S$_{11}$ (b) Process corner simulation (S$_{21}$, S$_{11}$)](image)

Process corner simulation represents the burst power or burst speed through all corners slow-slow, slow-fast, fast-slow and fast-fast (S-S, S-F, F-S, FF). $S_{21}$ and $S_{11}$ has been shown in Figure 8(b) for all corners and approx. twenty-three percent variations across the typical corner.

4.2 Noise Figure

NF of proposed LNA as shown in Figure 9(a), for the frequency range of 3GHz-8GHz. The maximum and minimum range of NF is 4.8dB and 1.1dB simultaneously. The decrement in NF with frequency validates the mathematics of noise cancellation explained in Section-3.
To check the robustness of the proposed LNA, Monte Carlo simulation has been done for NF as shown in Figure. Simulation has been done for a sample size of 1000 at frequency 4.1GHz. the mean value and standard deviation of NF is 1.21dB and 0.14dB.

4.3 Mismatching effect

To make the proposed LNA more robust, Monte Carlo simulations have been done at frequency 4.1GHz for $S_{21}$ and $S_{11}$ as shown in Figure 10(a), (b). The Sample size in the Simulation is 1000 and both effect process variation and mismatch was considered in simulation. The mean value and standard deviation is 16.8 dB and 0.98 dB for $S_{21}$ while -15.2db and 0.82dB for $S_{11}$.

4.4 Linearity

In the recent research of advanced circuit, nonlinearity and chaos is in focus. In this paper third order intercept(IIP$_3$) and second order intercept(IIP$_2$) as metric for nonlinearity is simulated and shown in Fig.11, for IIP$_3$ a two tone was simulated with spacing of 100 MHz and center frequency of both the tone varied throughout the band. While a spacing of 1GHz in two tone test has been considered for IIP2. The plot of output power with input power shown in Figure 11 and acquired the value of IIP$_3$ -9.9dBm The worst case was noted at frequency of 5.2GHz and acquired a value of IIP$_2$ of 9.8dBm.
As LNA has different parameters of design metric. Therefore, Figure of merit (FOM) is used to compare the overall performance of LNA. FOM includes the effect of power gain, bandwidth, linearity, NF and power dissipation and given as in equation (13)[19-20]. Different parameters comparison of proposed LNA with other work is shown in Table 2.

$$FOM = 20 \log_{10} \left( \frac{S_{21\text{av,lin}}} {P_{\text{dc,mW}}} \times \frac{BW_{\text{GHz}} \times |IIP_3|_{\text{mW}}}} {IIP_2} \right) \times (F_{\text{av,lin}} - 1)$$ \hspace{1cm} (13)

Table 2. Performance Summary of State of Art with Proposed Work

| Parameter | [21] TCAS | [27] TMITT | [22] IMS | [28] MWCL | [23] MWCL | [24] JSSC | [25] TMITT | [26] TMITT | Proposed work* |
|-----------|-----------|-----------|---------|----------|----------|----------|----------|----------|---------------|
| NF (dB)   | 2.8-3.4   | 3.8       | 2.76    | 3.9-5.8  | 3.0\(^*\) | 4.5-5.1  | 2.57\(^*\) | 4.9-6     | 1.1\(#\)      |
| 3dB bandwidth (GHz) | 0.2-3.8    | 0.1-2.0   | DC-5    | 1.6-9.7  | 0.0-1.4  | 1.2-11.9 | 1.05-3.05 | 0.1-2.2   | 3.7-5.5       |
| S11 (dB)  | <-9       | <-10      | <-10    | <-10     | <-11\(^*\) | <-11\(#\) | <-9       | <-16.4\(^#\) |
| PDC (mW)  | 5.7       | 3         | 10.4    | 10.6     | 12.8     | 29       | 12.6      | 0.4       | 3.6           |
| Peak Gain (dB) | 19\(^*\) | 7.6       | 13.9    | 12.6     | 16.4     | 9.7      | 16.9\(\#\) | 12.3      | 17.1          |
| Supply (V) | 1         | 1.2       | 1.8     | 1.8      | 1.2      | 1.8      | 1.8       | 1         | 1.0           |
| No. of Inductors | 0         | 0         | 2       | 6        | 0        | 5        | 4         | 0         | 0             |
| Technique | Noise cancellatio n | Feedbac k | Dual feedbac k | Post Distortio n | Shunt feedbac k | Noise cancellatio n | Dual negative feedbac k | Tunable active feedbac k | Inductorles s CCG-BBCCs |
| FOM       | 22\(^*\)  | 12        | -5.9    | -       | -9.2     | -9       | 12\(^*\)  | 8.9\(\#\) | 12.4          |
| Technology | 130nm     | 130nm     | 180nm   | 180nm    | 180nm    | 130nm    | 180nm     | 130nm     | 45nm          |

\(^*\)Estimated from the curves, \(^\#\)simulated result, \(^\#\)Minimum value, \(^\#\)Voltage gain de-embedded out buffer
It can be directly observed from Table 2 that proposed LNA has good result in term of NF, input reflection coefficient. Proposed LNA has sufficient bandwidth (3.7-5.5GHz) and can be used as front end circuit in wireless for UWB. The overall performance is better and can be observed by FOM as compared with the state-of-art.

5. Conclusion
In the proposed LNA two stages were there, one was CCG and the other one was the BBCS. Both have been used, the CCG stage is good in terms of low power consumption and the input impedance matching throughout the band. While BBCS stage is good at the biasing voltage and provides high and flat gain. A noise cancellation method is adopted to reduce the bandwidth of 3.7 GHz–5.5 GHz, minimum NF of 1.1 dB, maximum and minimum values of $S_{21}$ and $S_{11}$ are 17.1dB, –16.4dB respectively at frequency 4.1 GHz and shows a good strength, consumes a very less power of dissipation 3.6 mW. FOM represents the good result as compared to other popular techniques.

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