Fabrication of 4H-SiC lateral double implanted MOSFET on an on-axis semi-insulating substrate without using epi-layer

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4H-SiC lateral double implanted metal–oxide–semiconductor field effect transistors (LDIMOSFET) were fabricated on on-axis semi-insulating SiC substrates without using an epi-layer. The LDIMOSFET adopted a current path layer (CPL), which was formed by ion-implantation. The CPL works as a drift region between gate and drain. By using on-axis semi-insulating substrate and optimized CPL parameters, breakdown voltage (BV) of 1093 V and specific on-resistance (Raon) of 89.8 mΩ⋅cm² were obtained in devices with 20 µm long CPL. Experimentally extracted field-effect channel mobility was 21.7 cm²/V⋅s and the figure-of-merit (BV/√Raon) was 13.3 MW/cm². © 2017 The Japan Society of Applied Physics

Silicon carbide (SiC) is an attractive material for high power devices due to high mobility and high breakdown electric field.1,2) A number of vertical high voltage devices such as SiC double-implanted MOSFET (DMOSFETs) and U-shaped MOSFET (UMOSFETs), have been demonstrated.3–6) In contrast, not many lateral SiC devices have been investigated, in comparison with the vertical devices.7–10) Recently, there has been increased demand for the lateral devices, to implement both high voltage power device and low-voltage circuits on a single chip.11)

In general, lateral SiC MOSFETs are fabricated on a SiC epi-layer which was grown on off-axis conducting substrates. For 4H-SiC, 4°-offward (110) substrate is widely used in order to avoid poly-type inclusion.12) However, step bunching often occurs during the epitaxial growth and high temperature activation process.13) The step bunching makes surface rough14) and causes scattering of carriers at the surface. Consequently, the channel mobility of the MOSFET is dramatically reduced.15,16) Therefore, on-axis wafer has advantages for improving current characteristics compared to the off-axis wafer.

However, it is still possible to create poly-type defects on an on-axis wafer during epitaxial growth, and elimination of the epi-layer is preferred in many aspects.17) In this paper, 4H-SiC lateral double implanted MOSFET (LDIMOSFET) have been designed and fabricated on an on-axis high purity semi-insulating (HPSI) substrate. In order to avoid the problems mentioned above, we used the on-axis SiC substrate. Our devices showed similar static characteristics comparable to those of the conventional devices.

Figure 1 shows a cross-sectional view of our device. We simulated the static characteristics by using a device simulator Silvaco-ATLAS. As shown in the figure, the proposed device adopted a current path layer (CPL) instead of an epi-layer used in the conventional device. The CPL region is formed by ion-implantation. N⁺ and p regions in the figure are also realized by ion implantation. The CPL region plays an important role in obtaining MOSFET characteristics. At a forward bias condition, the CPL serves as a current path, and at reverse bias it serves to support the breakdown voltage. Without the CPL region, only the semi-insulating layer exists between the p-base and n⁺ drain of the device. In this case the forward current will be very small, due to a low carrier density in the semi-insulating substrate.

It is important to optimize the CPL parameters (doping concentration and depth), in order to obtain desired forward and reverse characteristics. For optimization, device simulation was performed by using Silvaco-ATLAS. Simulations were performed by varying the doping concentration (Ncpl), depth (Dcpl), and length (Lcpl) of the CPL region. The doping concentrations of p-base and n⁺ source/drain were fixed at 2.5 × 10¹⁹/cm³ and 8 × 10¹⁹/cm³, respectively. A channel length of 2 µm and a gate oxide thickness of 55 nm were used. Device parameters used in the simulation are shown in Table I.

Figure 2 shows the simulated characteristics (breakdown voltage and specific on-resistance) of the proposed device as a function of Ncpl and Dcpl. In this figure, Lcpl was fixed at 5 µm. When Dcpl varies from 0.1 to 0.4 µm in Fig. 2, the device exhibited breakdown voltages of 210–615 V. When the Ncpl and Dcpl were increased, the breakdown

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**Table I.** Device parameters used in simulation.

|                     | Doping conc. (cm⁻³) | Depth or length (µm) |
|---------------------|---------------------|----------------------|
| P-base region       | 2.5 × 10¹⁷           | Depth: 0.6           |
| Sourced/drain region| 8 × 10¹⁹             | Depth: 0.3           |
| CPL region          | 1 × 10¹⁵–1 × 10¹⁷    | Length: 5–20         |
| Semi-insulating substrate | <10⁹             | Depth: 0.1–0.4       |

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Specific On-resistance increases significantly when \( N_{\text{CPL}} > 4 \times 10^{16} \text{cm}^{-3} \) and \( D_{\text{CPL}} > 0.3 \mu\text{m} \), breakdown voltages sharply decreased. At a given doping density of \( N_{\text{CPL}} \), an increase of the depth \( D_{\text{CPL}} \) encourages the electric field in the depletion layer to have a triangular shape, and the maximum electric field becomes higher. This explains the lower breakdown voltages as \( D_{\text{CPL}} \) increases.

Figure 3 shows surface electric field distributions in the devices with \( D_{\text{CPL}} \) of 0.1 and 0.4 \( \mu\text{m} \), simulated at \( V_{\text{Drain}} = 300 \text{ V} \). As shown in the figure, depletion layer of the device with \( D_{\text{CPL}} = 0.4 \mu\text{m} \) does not reach the drain, and the maximum electric field is higher. As shown in Fig. 2, specific on-resistance increases significantly when \( N_{\text{CPL}} \) is lower than \( 2 \times 10^{16} \text{cm}^{-3} \). Therefore, in order to obtain high breakdown voltage and low specific on-resistance, \( N_{\text{CPL}} \) and \( D_{\text{CPL}} \) should be within range of \( 2 \times 10^{16} \lesssim N_{\text{CPL}} \lesssim 4 \times 10^{16} \text{cm}^{-3} \) and \( 0.2 \leq D_{\text{CPL}} \leq 0.3 \mu\text{m} \), respectively. For device fabrication, considering the simulation results, we used \( N_{\text{CPL}} = 2 \times 10^{16} \text{cm}^{-3} \) and \( D_{\text{CPL}} = 0.3 \mu\text{m} \), respectively.

Drain currents (a) and transconductances (b) as a function of gate voltages. Currents measured in two devices (with and without a current path layer) are compared.
There are considerable amounts of intrinsic deep traps such as low drain current, due to the highly resistive drift region. Currents were measured in two devices (with and without a current path)

Fig. 5. (Color online) Drain currents as a function of drain voltages. Currents were measured in two devices (with and without a current path layer).

The reported mobility range of the Al-implanted MOSFETs fabricated on the 8° off-axis epitaxial layer is 6 to 9 cm²/V·s. In contrast, mobility range of the Al-implanted MOSFET fabricated on the on-axis epitaxial layer is 9 to 19 cm²/V·s, and they explain that the mobility increase is due to the lower surface roughness. In our device, we used on-axis substrate to avoid the surface roughness scattering caused by the step bunching and we observed mobility comparable to those measured in the device implemented on the epitaxial layer grown on the on-axis wafer. This results suggests that our mobility increase is related to the lower surface roughness in the on-axis substrate.

The extracted threshold voltage of the device by using the $g_{m}$-max method is 7 V. The device without CPL shows very low drain current, due to the highly resistive drift region. There are considerable amounts of intrinsic deep traps such as $Z_{A1/2}$ and $E_{A1/7}$ in the semi-insulating substrate, which removes free carriers in the device without CPL. Figure 4 shows that CPL can replace the epi-layer in the LDIMOSFET structure.

Figure 5 shows measured drain currents as a function of drain voltage. The device with CPL shows transistor characteristics ($L_{CPL} = 5 \mu m$). Gate voltage was changed from 0 to 25 V with 5 V increment. In the figure, the highest drain current is 22 mA/mm. Although the current flow is restricted to a thin layer (0.3 µm depth), the device exhibits large current due to the high carrier concentration in the CPL. Currents in the device without CPL slightly increase when drain voltage exceeds 10 V. This small increase of current comes from the drift flow of electrons due to the high electric field between p-base and n⁺ drain. A specific on-resistance of the device 17.2 mΩ·cm² at $V_G = 25$ V and $V_D = 1$ V. When the $L_{CPL}$ was increased from 5 to 20 µm, the specific resistance of the device also increased, from 17.2 to 89.8 mΩ·cm².

The maximum breakdown voltage of a conventional lateral device implemented on conducting substrate is determined by the thickness and doping concentration of the epi-layer. Thick lightly doped epi-layer under the drift region is required to prevent breakdown in the vertical direction. In other words, breakdown voltage is limited by the depletion in the vertical direction. In our device, epi-layer and drift region of the conventional device is replaced by semi-insulating substrate and CPL region. Because the doping concentration of the semi-insulating substrate is extremely low, maximum breakdown voltage of the device is determined by the depletion in the CPL region. Therefore, breakdown voltage of our device depends on $L_{CPL}$, $D_{CPL}$, and $N_{CPL}$. The measured breakdown voltages for different $L_{CPL}$ are shown in Fig. 6. The current shows a sharp rise at high drain voltages, and we define this voltage as the breakdown voltage.

As shown in the figure, longer $L_{CPL}$ shows higher breakdown voltage, and the maximum voltage of 1093 V was observed in the device with $L_{CPL} = 20 \mu m$. The observed breakdown voltages show almost linear dependence on $L_{CPL}$, and this suggests that the whole CPL regions are depleted in this configuration. Our simulation results also confirmed that entire region of CPL was depleted, even in the device with $L_{CPL} = 20 \mu m$.

Maximum breakdown voltage (BV) of 1093 V was achieved with low specific on-resistance ($R_{on,sp}$) of 89.8 mΩ·cm² at $L_{CPL} = 20 \mu m$. The figure of merit (BV²/$R_{on,sp}$) of the fabricated device in this paper is 13.3 MW/cm². The breakdown voltage of the fabricated device can be improved by using a field plate. Due to the two-dimensional effects at the bottom corner of the p-base and n⁺ drain, field crowding occurs at the edges leading to the field spikes, and the breakdown voltage is reduced as a result. This can be avoided by using field plates placed on top of the gate and drain.

The specific on-resistance of the device can be improved by adopting the RESURF principle. Parameters for the full depletion with higher doping in the CPL region can be found by the simulation. The effect of the field plates and RESURF principle is under investigation.

In conclusion, 4H-SiC LDIMOSFET have been designed and fabricated on off-axis HPSI substrate without using an epi-layer. We confirmed that the CPL could replace the epi-layer of the conventional device, without sacrificing their performance. Measured effective channel mobility of 21.7 cm²/V·s was obtained, and high breakdown voltage and low specific on-resistance were achieved. Our device exhibited a specific on-resistance of 89.8 mΩ·cm² with a threshold voltage of 7 V, when $L_{CPL} = 20 \mu m$. The measured maximum breakdown voltage was 1093 V, yielding a figure of merit (BV²/$R_{on,sp}$) of 13.3 MW/cm². These results show that 4H-SiC LDIMOSFET fabricated on a semi-insulating substrate without an epi-layer is a prospective candidate for power integrated circuits.
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