An FPGA-Based System for Remote Data Monitoring of Underwater Gravity Measurement

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Abstract. Considering that underwater gravity measurement has the characteristics of a large amount of data and poor communication conditions, a data transmission link based on FPGA and wireless network is designed. The build of the wireless network could get rid of the dependence on cable and increase the adaptability to the working environment onboard. The multi-level wireless network is easy to expand and the compatibility and extension of equipment are better than the traditional wired transmission by cables, which enables devices to keep safe by working in the room rather than on the deck. In this condition, FPGA (Field Programmable Gate Array) can be used to preprocess the gravimeter data, and process the original miscellaneous data information into a short and effective data frame, which effectively reduces the communication pressure and makes the data transmitted by wireless network possible. The experiment shows that the design can effectively transmit the effective data collected by the deep-sea gravimeter and display the data in real-time on the remote computer when the mobile network bandwidth is about 1Mbps.

1. Introduction
Modern underwater near-bottom gravity measurement mainly uses the bottom detection technology, in which the vehicle periodically lands on the sea bed, and uses a gravimeter in a manually operated vehicle to measure gravity [1]. It could take several days for the gravimeter to reach a steady-state for operation and during the operation period, it is forbidden to de-energize the gravimeter. Therefore, it is particularly important to monitor the status information of the gravimeter. In this paper, a data link design based on FPGA and LAN is proposed, in which the communication technology and FPGA development board are used to realize the automatic transmission and processing of gravimeter data. Besides, devices on the deck are always explored to the sunshine, salty steam, and other dangerous factors. The design achieves the purpose of remote monitoring to the underwater gravimeter’s working state and keeps the data link stable.

In recent years, with the rapid development of 5G/4G network, IoT (Internet of Things Technology) is becoming more and more popular. FPGA is used as a part of the data transmission link in various special cases because of its powerful operation and expansion ability. Xue Ping et al. in Harbin University of Science and Technology devise a Power quality remote monitoring system based on FPGA. The system uses hardware phase-locked frequency tracking technology for synchronous sampling of the three-phase voltage, current, reducing leakage, and spectral interference between...
spectrums [2]. Sometimes, complex design in FPGA could process the data before the data are sent to the upper computer rather than pass through only. In reference [3-5], FPGA first preprocesses the data for the convenience of transmission in multipath. The expansion ability of FPGA enables it to work in different conditions to meet different needs. Roukhami, M, et al. in the University of Tunis El-Manar build accelerators for tag-less remote person identification based on FPGA, which could work on the active power ranges between 6.24 and 34.7mW [6]. In our design, the most vital problem we face is the severe working conditions on board. Here, we list the requirements as follows:

1) High reliability. When facing the complex working environment, the information of gravimeter is only sent back by this testing equipment. The safety and reliability of gravimeter are guaranteed by this equipment, so first of all, this equipment should ensure the reliability of its own work. Underwater gravimetry has a long period of operation, and the operation time is usually several days to more than ten days. The monitoring system needs to have high reliability of long-term stable operation, as well as the characteristics of shock resistance and temperature change resistance.

2) Data frames need to be short and compact. In consideration of the limited wireless communication capacity on the sea(far away from the mobile wireless signal), a large amount of information transmitted by gravimeter needs to be processed to be a new frame before entering the data transmission which could keep the information effective and short as well [7].

2. Hardware in the design
Considering the characteristics of offshore operation, WLAN and LAN wireless transmission modes are adopted in the data link, relying on the WiFi module and DTU (Data Transfer Unit) respectively. As shown in Figure.1, it shows the hardware facilities of the whole design, the layout location, and the flow of data in the design.

![Figure 1. Hardware connection.](image)

2.1. WiFi module
We use ALIENTEK ATK-RM04 in this design. Data acquisition equipment broadcasts data in the wireless network through WiFi. The establishment of wireless network and reception of broadcast data needs two WiFi modules working in AP (Wireless Access Point) mode and STA (Station) mode respectively. After the data enters the wireless network, the WiFi module as AP establishes the wireless network, and the module as STA receives the data and transmits the data through the serial port to the FPGA.
2.2. **DTU**

DTU selected is USR-GPRS232-730 GPRS DTU provided by YOUREN Company. In general, DTU is a device for data transmission that relies on the cloud server. Its working pattern is to use the data network (5G/4G/3G/2G) provided by mobile network operators to offer users wireless long-distance data transmission function. Most DTUs use high-performance industrial communication processors or communication modules, and the embedded real-time operating system is used as the software to support the hardware platform. Most of the data interaction interfaces support the RS232 or RS485 (or RS422) interfaces, which can be directly connected with the serial port equipment, from the fact that data transmission or other more complex functions.

![USR-GPRS232-730 GPRS DTU.](image1)

**Figure 2.** USR-GPRS232-730 GPRS DTU.

![Part of the devices working in the room.](image2)

**Figure 3.** Part of the devices working in the room.

2.3. **FPGA**

The selection of the development board must be based on the requirements of hardware in the design. Structurally, considering the actual need to add gravimeter information and environment information to the development board, other conditions of the development board, under the same conditions, give priority to the model with more serial ports or easy serial port expansion. In terms of performance, there are certain requirements for the computing power and serial port function of the development board: the high-efficiency unframed development board has the required computing power, and the serial port communication process needs its UART structure to have a transceiver register, and a flag bit to display the transceiver register in real-time. In addition, the development board also needs to provide clock and reset signal resources for its circuits. According to the requirements, the development board used in this design is Xilinx spartan6 FPGA development board.
According to the design above, the data collected from the gravimeter can be transmitted to the FPGA working in the room through the WiFi module after getting on the ship through the cable. After the FPGA processes the original data frame into a short new data frame, it can be transmitted to the further monitor through the LAN under the Limited communication bandwidth by DTU. The data frame will be displayed in real-time on the monitor through the supporting virtual instrument. At the same time, GPRS module can be extended to ensure that the collected abnormal values and conditions can be transmitted to the designated Guardian through SMS when the LAN bandwidth is severely limited.

3. Design of FPGA

The xc6slx9 of spartan6 (Figure.4) series developed by Xilinx company is mainly composed of main chip, clock and reset circuit, the power supply part, configuration circuit, expansion IO socket, reserved row hole, and other parts. Xilinx spartan6 FPGA development board core board chip has 144 pins, except for some special function pins, other pins can be expanded.

3.1. COSUMER THEORY

The process of deciphering data frames is very time-consuming due to Producer/consumer mode is a unique mode of data transmission in the ControlNet network, which is easy to set and safe to use. Because of its good application practice, its idea has been more and more applied to other programs that need data transmission. Based on this theory, programs to data acquire, process, and transmit on FPGA are designed.

![Figure 4. Core on the xc6slx9 of spartan6.](image)

![Figure 5. Pins on the FPGA.](image)
In this mode, the producer’s function is to produce products (data), and the consumer uses products (data). Without production, the consumer cannot use products. Compared with the senders in point-to-point transmission, a producer can correspond to multiple consumers, but a consumer can only correspond to one producer. After using the producer-consumer model, the producer and the consumer can be two independent concurrent subjects, which can properly solve the problem of the imbalance between the producer and the consumer. In addition, the design pattern reduces the coupling between the producer and the consumer, avoiding that the producer cannot find the dependent object due to modifying the corresponding class of the consumer.

3.2. PORTS AND REGISTERS ON FPGA

3.2.1. RS232 serial port. The FPGA development board has an RS232 serial port. The circuit built is based on two RS-232 serial ports that can work stably. In this design, we choose MB core with a strong UART function. However, spartan6 has only one serial port. So, after adding two serial ports in the circuit design, the hardware needs to correspond with spartan6. In the hardware, the TTL serial port on the FPGA development board can be transformed into an RS232 serial port by using the serial port expansion module to expand the serial port.

As shown in Figure 5, pin6 and pin8 are not defined on the FPGA, so they can be used for serial port expansion. In Planahead, pin6 can be defined as the receiving end and pin8 as the sending end. It can be seen from the figure that pin6 and pin8 belonging to the core board are respectively connected to pin 13 and pin 15 on the P1 module of the bottom board. Therefore, the receiver and sender end of the serial port expansion module connect to pin 13 and pin 15 respectively, and then the power and ground are well connected, so an RS-232 serial port can be expanded in this way.

3.2.2. Register. In this design, we mainly operate the receive register, send register, and status register in the XPS UART Lite (Figure 6). Receiving register and sending register are applied to provide buffer space for data in receiving and sending state, while state register can represent the working state of Rx FIFO and TX FIFO through flag bits, which plays an irreplaceable role in coordinating software and hardware timing logic [8].

After the external circuit structure setting as shown in Figure 7, the SDK can be used to write code to the MB core. Starting from the working principle of hardware, according to the ideas in the producer / consumer model, data flow will keep running.

![Figure 6. XPS UART Lite.](image)

![Figure 7. I/O setting on the MB core.](image)
3.3. PROGRAM ON MB Core

The peripheral circuit of the FPGA is designed to make the best of serial port expansion capability and UART status register on the development board. The main work of FPGA depends on MB core which reads the status register, judges that there is data in the receive FIFO, reads in the data processing, and finally sends out the new data frame through another serial port.

To meet the design requirements, the MB core needs 3 steps in a data processing process: save, reframe, and send. Figure 8 shows every step of the data in this transmission link, which can be taken apart in three parts: collection, processing, and transmission. The three steps above are relatively independent function blocks. The following will introduce the three functional modules in the form of a block diagram.

![Figure 8. Program on the MB core.](image)

3.3.1. Data saving module. The data saving module is the most basic and complex part of the program. The difficulty lies in the coordination of the C language execution clock and the hardware execution clock. This processing method is not necessarily the optimal solution, but in many practical tests, it can ensure stable operation and correct data.

| Base Address + Offset | Description       | Access Type | Default Value |
|-----------------------|-------------------|-------------|---------------|
| C-BASEADDR+0x0        | Rx FIFO           | Read        | 0x0           |
| C-BASEADDR+0x4        | Tx FIFO           | Write       | 0x0           |
| C-BASEADDR+0x8        | STAT_REG          | Read        | 0x4           |
| C-BASEADDR+0xC        | CTRL_REG          | Write       | 0x0           |
Table 2. XPS urat lite register.

| Bit (s) | Name          | Core Access | Reset Value |
|--------|---------------|-------------|-------------|
| 0-23   | Reserved      | Read        | 0           |
| 28     | Tx FIFO Full  | Read        | '0'         |
| 29     | Tx FIFO Empty | Read        | '1'         |
| 30     | Rx FIFO Full  | Read        | '0'         |
| 31     | Rx FIFO Valid Data | Read | '0' |

The first step of data collection is to determine whether there is data transferred from FIFO at this time. According to the flag bit (last bit) of the FIFO status register, you can judge whether the current FIFO is empty. See TABLE I and TABLE II for details. When it is judged that FIFO is not empty at this time, the program will save the data in the array.

In the test process, it is found that due to the execution speed of the software is too fast, the consumer consumption speed is far faster than the producer's speed. Even the speed of the software is faster than the change speed of the state register level in the FPGA. As a result, when FIFO is empty, the flag level of state register hasn't changed yet, but the software has been executed and entered a new judgment. At this time, the FIFO information will be misjudged, which will cause the software execution logic to repeatedly collect the unreduced level in the FIFO at this time. In addition, because of the slow speed of the producer, when FIFO has been mined out, the producer must wait for a long time and check the status register many times to get the data produced by the producer. This process includes the change of the flag bit of the status registers many times, which is easy to produce the situation of FIFO information misjudgment. For this reason, the cache array buf [] is set in this logic. Since the FIFO size is set to 128bits = 16bytes, the array length is set to 16, that is, each small cycle can collect 16 characters. In this way, it can ensure that consumers will wait for a period of time to consume the data stored in FIFO by producers after each time the consumption of the data stored in FIFO is finished.

It is not enough to deal with data frames only by cache array. On the one hand, because the format of the data frame is not fixed, the interpretation of the data frame needs the integrity of the data frame; on the other hand, because the data needs to be processed and forwarded after the data is saved, the consumption speed of each consumption level is different, and the setting of buffer array is the necessary means.

After the data is orderly pressed into the processing array, the program will calculate the data length of the processing array. Because the frame length is fixed (or the frame length information can be read out in the frame header), it can judge whether the data frame has been received according to the data length of the current processing array. If not, initialize the cache array (record the long number to zero) and start to input new data to the cache array; if not, enter the processing and sending stage.

3.3.2. Reframing module. Data processing includes two processes: unframe and repackage. The first step of data framing is to process the string into a decimal number. The function can convert the character corresponding to hex (0-F) to decimal (0-16) without transcoding the symbol information such as space in the original string. The result of the function is obtained by subtracting the ASCII code corresponding to '0' or 'a' from the ASCII code corresponding to the character.

After the decimal number is obtained, the data will be calculated according to the requirements. Since the operation generally does not involve advanced mathematics, this step is relatively simple, which will not be described here. The calculated result needs to be converted to a string before sent. It relies on the transformation function: struct tag into char (int integral). Here, the struct tag is a custom structure, which means to keep the integrity of the string corresponding to the decimal number. For example, when we calculated the result of the decimal number in the previous step to 120, according
to the encapsulation rule, it will be encapsulated as "0120". That is, when the integration is any natural number less than 9999, the return value would have four characters. However, the return value of a function in C cannot be an array, so you need to define the structure as follows:

```c
struct tag {
    unsigned char a[4];
} x, y;
```

In this way, the character corresponding to a decimal number can be stored in a struct tag variable.

In this design, the operation rules of unframe are customized according to the sub sensor used in the underwater gravimeter. In our experiment, the sensor adopts eight channels and each channel of data contains five analog quantities collected continuously in the sampling time. Considering the actual needs, this program takes the average of 5 data in each path and carries out subsequent calculation when unframed, encapsulates the calculated decimal number according to the content of the previous paragraph, and sends out after the completion of 8-way data encapsulation.

3.3.3. Sending module. The data transmission of FPGA mainly depends on the transmitting FIFO. Its working principle and performance are the same as those of the receive FIFO. When the data is completely sent, the program begins to enter the next cycle and is ready to receive new data frames. Therefore, the processing array needs to be initialized.

![Reframe framework](image)

**Figure 9.** Reframe framework.

The above design ensures that the gravimeter data can be broadcast effectively through the limited bandwidth LAN under the safe working environment of the equipment all the time, and enables the remote equipment to monitor the data in real-time. The experimental result is as follows in Figure.10:

![Data frame before and after reframing](image)

**Figure 10.** Data frame before and after reframing.

On this basis, the expansion of the MB core in FPGA makes it possible to use one FPGA to settle the data of multiple units at the same time. In addition, the existing industrial standard Modbus communication protocol is used to reduce the frequent conversion of the communication protocol in the process of data transmission, and the device expansion compatibility is better. At this time, only the MB core code in FPGA needs to be rewritten to change the communication protocol, so that FPGA
can be used as a data relay station to collect the data of the lower computer and respond to the requirements of the upper computer.

4. Test on the sea

4.1. Test introduction
We implemented an underwater gravimetry trial in the South China Sea in November 2019. We measured six 10-km-length lines, including four east-west lines and two north-south lines (Figure 12). A picture of the improved strapdown underwater gravimeter is shown in Figure 11.

![Strapdown underwater gravimeter](image1)

Figure 11. Strapdown underwater gravimeter.

![Real trajectories](image2)

Figure 12. Real trajectories.

4.2. Test results
We could collect data about 5GB for 12 hours during the experiment from the gravimetry. We select 3 physical quantities to be sent to remote monitor: depth on channel0, the voltage on channel 4, and current on channel 5. All data collected in one lane are about 2GB, which are compressed to about 0.4GB after reframing. The data showed on remote monitor is Figure 13.
The data link could keep stable during the whole test line for about 2 hours one time. The work of WLAN is little influenced by sea conditions. However, the DTU’s work which relies on the LAN cannot stay at a good state when facing the Class V sea state. Compared with the efficiency of about to 97% in paper [9], our design would keep the packet loss rate remains at about 2% in ideal condition and 10% in severe condition. Most of the massage was lost during the transmission through the LAN and the logic of reframing on FPGA also increases this rate because we select to abandon the whole frame when finding it incomplete to reduce false alarm.

The bandwidth of LAN would be greatly affected when the sea conditions get worse. The transmission speed is no longer a problem after data reframing but we faced serious packet loss, which would cause the data curve is not smooth. To solve this problem, a warning message could be succeeded in sending at this time. To summarize all, the design we applied qualified the job to monitor the data without wiring on the deck and send the vital frame to the remote computer to keep the minimal communication even the conditions get worse (Figure.14).

5. Conclusion

We designs remote data detection equipment based on FPGA and wireless network transmission equipment, which is suitable for ship operation. The data processing logic of FPGA is designed by using producer/consumer mode, and the data acquisition of gravimeter would be selected and simplified. Experiments show that the design has a safe layout and good performance on the ship. In case of severe weather, GPRS module is designed to send further simplified warning information by using short message. In the future, because the computing power of FPGA has not been fully utilized, we can perform more complex operations on FPGA like the design in paper [10]. The next time we go to the sea for experiments we plan to apply a new frame to design the FPGA to decrease the data loss rate to 5% in severe sea state.
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