Non-isolated high step-up DC/DC power converter with coupled-inductor

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Abstract
This paper presents a non-isolated single switch converter with high voltage gain. Its circuit topology is combined with coupled-inductor, clamp circuit, and voltage lift capacitor techniques. The proposed converter has several advantages: First, the circuit is controlled by only single pulse width modulation (PWM) for the power switch, which keeps the circuit simple. Secondly, the proposed converter is used as a clamping circuit, which let the energy of the leakage inductance can be circulated to the capacitor, so that the voltage spike on the active switch can be suppressed, and improves efficiency. This paper will introduce the principle of action, theoretical analysis, and experimental waveform in order. Finally, in the case of input voltage of 48 V, output voltage of 400 V, and output power of 1 kW, the performance of the proposed converter is verified. As a result, the maximum efficiency is up to 96.5% and full load efficiency is 92.3%.

Keywords
High voltage gain, coupled-inductor, clamp circuit, power converter, voltage-lift capacitor

Introduction
With the shortage of energy and forever rising oil prices, renewable energy research and green energy are becoming more and more important. These clean energies, comprising fuel cell (F.C.), wind energy, and photovoltaics (PV) can be applied as distributed generation (DG) systems. In a solar photovoltaic system, energy is generated by solar cells, and electricity is generated by converting DC to AC, so high-efficiency inverters must be used. However, inverters have some problems, such as
high switching losses, large output filter space, and many harmonics.\textsuperscript{1,2} High step-up dc–dc converters can be used in these systems as interface converters to increase the output voltage. By connecting these converters to each PV panels, they can be controlled a novel high step-up dc–dc converter was presented. The proposed converter benefits from some advantages such as low-ripple input current, high voltage gain, zero current switching of the main switch, and low voltage stress of the main switch.\textsuperscript{3} A new method is proposed for a high-boost high efficiency converter with low switching stress.\textsuperscript{4,5} The another presented converter is based on the SEPIC converter. However, the converter voltage gain is improved by employing a coupled inductor and two voltage multipliers.\textsuperscript{6} Recently, DC–DC converters with high conversion ratio become popular as required in the front-end of the electrical grid supplied by environmental friendly sources of energy, or in hybrid/electric vehicles, or in data and telecommunication applications.\textsuperscript{7} The challenges in high step-up renewable energy applications are summarized to generate the next generation non-isolated high step-up DC/DC converters. The output voltage generated by the photovoltaic arrays, the fuel stacks, the super capacitors, or the battery sources is relatively low, even lower than 48 V. It should be boosted to a high voltage, such as 380 V for the full bridge inverter or 760 V for the half bridge inverter in the 220 V AC grid-connected power system\textsuperscript{9,10} as shown in Figure 1.

This paper mainly designs 48 V\textsubscript{DC}/400 V\textsubscript{DC} converters. Traditional boost converters cannot provide such high boost ratios. However, isolated converters can achieve higher voltage boost ratios through the transformer turns ratio, such as flyback converters, full-bridge converters, but isolated converters suffer high voltage spikes and high power consumption due to the leakage inductance of the transformer. In order to solve the shortcomings of traditional converters and improve conversion efficiency and voltage gain, this thesis combines switched capacitor technology, boost capacitor technology and capacitor-diode voltage multiplier technology\textsuperscript{11–13} to achieve transformerless, high boost ratio, and high efficiency DC converter.\textsuperscript{13,14}

This paper proposes an integrated boost-flyback converter architecture (IBFC).\textsuperscript{12,15,16} The converters using coupled inductors can achieve high boost gain

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{system_architecture.png}
\caption{System architecture of green energy and charging station.}
\end{figure}
by adjusting the turns ratio, but the coupled inductors can cause leakage energy and voltage spikes. In order to solve the above two problems, this paper uses non-dissipative snubber circuit and active clamp circuit, which not only absorbs the leakage inductance energy of the coupled inductor,\textsuperscript{17–21} but also limits the leakage voltage and spike voltage stress of the active switch, thereby improving the circuit efficiency.\textsuperscript{22}

The circuit diagram of the proposed converter is shown in Figure 2. Input DC voltage $V_i$, power switch $S_1$, primary side winding $N_1$, secondary side winding $N_2$, and third side winding $N_3$ are winding coupling inductors, clamping capacitor $C_1$, clamping diode $D_1$, voltage-boost Capacitor $C_2$, rectifier diodes $D_2$ and $D_o$, output capacitor $C_o$, and output load resistance $R_o$. Base on the working principle, when the power switch $S_1$ is turned on, the capacitor $C_2$ is charged by the input power $V_i$, the clamp capacitor $C_1$, the secondary side winding $N_2$, and the third side winding $N_3$ are charged in series. During the time interval switch $S_1$ is off, the leakage inductance $L_{k1}$ and the magnetizing inductance $L_m$ charge the capacitor $C_1$. In addition, a part of the energy of the magnetizing inductor $L_m$ is released through the secondary side winding $N_2$ and the third side winding $N_3$ of the coupled inductor. The energy of the DC power supply $V_i$, the excitation inductor $L_m$, the capacitor $C_2$, and the secondary side winding $N_2$ is charged to the output capacitor $C_o$ and the load $R_o$.

**Analysis of proposed high step-up DC/DC converter**

**Operation principle of the proposed converter in continuous conduction mode (CCM)**

As shown in Figure 3, the converter operates in continuous current mode (CCM) and the waveform working principle of each point

According to Figure 4(a)–(f) are the six processes of the converter in continuous current mode, which are described as follows:
Mode I \([t_0 \leq t \leq t_1]\): At \(t = t_0\), switch \(S_1\) is turned on. Diode \(D_1\) and \(D_2\) are turned off, and \(D_o\) is turned on. The current-flow path is shown in Figure 4(a). The voltage equation of the primary-side of coupled-inductor is that \(V_i = V_{Lm} + V_{Lk1}\). At this time, \(V_{N2}\) generates an induced voltage, the primary-side coupled inductance \(i_{Lk1}\) increases, and the secondary current \(i_{L2}\) decreases. When the current \(i_{L2} = 0\), no current flows through the diode \(D_o\). Since the current \(i_{Lk1}\) is equal to \(i_{Lm} + n_2 \cdot i_{L2}\) at \(t = t_1\), this operating mode ends.

Mode II \([t_1 \leq t \leq t_2]\): The current path is shown in Figure 4(b). During this time, the switch \(S_1\) and the diode \(D_2\) are turned on, the input power \(V_i\) charges the inductor \(L_m\), and the diodes \(D_1\) and \(D_o\) are not turned on. Meanwhile, on the secondary-side winding \(N_2\) is connected in series with voltages \(V_{C1}\) and \(V_{N3}\) to charge

![Figure 3. The waveform of each point of the converter in one cycle.](image-url)
capacitor $C_{2:N2} + n_3V_{N3}$. The output capacitor $Co$ provides energy to the load $Ro$. When $t = t_2$, switch $S_1$ is non-conducting, and this operation mode II ends.

Mode III $[t_2 \leq t \leq t_3]$: The current path is shown in Figure 4(c). During this time, the switch $S_1$, diode $D_1$, and diode $Do$ are turned off, and $D_2$ is turned on. The leakage inductance $Lk1$ and the inductance $Lm$ charge the parasitic capacitor $Cds$ of the switch $S_1$. The input voltage charges the capacitor $C_2$ through the $V_{C1}$, $V_{N3}$, $D_2$, and $VL2$ paths. Output capacitor $Co$ provides the energy to the load $R_o$. While the capacitor voltage $V_{C1}$ is equal to $V_i + V_{ds}$ at $t = t_3$, diode $D_1$ conducts and this operating mode is ended.

Mode IV $[t_3 \leq t \leq t_4]$: The current path is shown in Figure 4(d). The switch $S_1$ and the diode $Do$ are not conducting, and the diode $D_1$ and the diode $D_2$ are conducting. The energy of the leakage inductance $Lk1$ and the inductance $Lm$ charges the capacitor $C_1$, so the leakage inductance energy is recovered. When time $t = t_4$, the secondary side current $i_{D2} = 0$, the diode $D_2$ is cut off, and the diode $D_o$ is on.

Figure 4. Current-flow path of the operating modes at CCM: (a) Mode I, (b) Mode II, (c) Mode III, (d) Mode IV, (e) Mode V, and (f) Mode VI.
Mode V \([t_4 \leq t \leq t_5]\): The current-flow path is shown in Figure 4(e). During this time, switch \(S_1\) is turned off. Diodes \(D_1\) and \(D_o\) are turned on, and \(D_2\) is turned off. At \(t = t_4\), the leakage inductance \(L_k\) and magnetizing inductor \(L_m\) charge capacitor \(C_1\). The voltage stress on the switch is limited. Also, a part of the energy of magnetizing inductor \(L_m\) is released via the secondary-side of coupled-inductor. Therefore, diode \(D_o\) is turned on and current is starting to increase. The secondary-side voltage \(V_{N2}\) is connected in series with voltages \(V_i\), \(V_{Lm}\), and \(V_{C2}\). The energies of DC-source \(V_i\), \(L_m\), \(C_2\), and \(N_2\) charge output capacitor \(C_o\) and load \(R_o\). When \(V_{N2}\) is equal to \(n_2V_{Lm}\) at \(t = t_5\), this operating mode is ended.

Mode VI \([t_5 \leq t \leq t_6]\): The current-flow path is shown in Figure 4(f). During this time, switch \(S_1\) is still turned off. Diodes \(D_o\) is turned on, \(D_1\) and \(D_2\) are turned off. The energy of magnetic inductor is released by coupling-inductor. The energy of the DC-source \(V_i\), \(V_{C2}\), and magnetizing energy of \(L_m\) provide energy to output capacitor \(C_o\) and load \(R_o\). This mode is ended at \(t = t_6\) during \(S_1\) is turned on at the beginning of the next switching period.

Steady-state analysis of the proposed converter in continuous conduction mode (CCM)

In order to analyze the steady-state characteristics of the proposed converter under Continuous Conduction Mode (CCM), the following formulas ignore the leakage inductance, the Equivalent series inductance (ESL) of the inductor winding, and the Equivalent Series Resistance (ESR) of the capacitor; the capacitors \(C_1\), \(C_2\) and \(C_o\) are ideal capacitors, and the coupled inductor model is \(L_m\). And the output voltage is a fixed voltage.

As shown in Figure 5(a), the equivalent circuit when the power switch \(S_1\) is turned on, the voltage on the magnetizing inductance \(V_{Lm}\) is \(V_i\). Current \(\Delta i_{Lm(on)}\) is represented as

\[
\Delta i_{Lm(on)} = \frac{V_i}{L_m} \cdot D \cdot T_S, \quad (0 \leq t \leq DT_S)
\]

The voltage on \(C_2\) can be written as

\[
V_{C2} = V_i + V_{C1} + V_{N2} + V_{N3}
\]

Figure 5(b) is the equivalent circuit when the power switch \(S_1\) is off. At this time, the voltage across \(V_{Lm}\) can be expressed as

\[
V_{Lm} = V_o - V_i - V_{C2} - V_{N2}
\]

And current \(\Delta i_{Lm(off)}\) is expressed as

\[
\Delta i_{Lm(off)} = \frac{V_o - V_i - V_{C2} - V_{N2}}{L_m} \cdot (1 - D) \cdot T_S, \quad (DT_S \leq t \leq T_S)
\]
According to the volt-second balance theorem, the voltage of the inductor $V_{Lm}$ is expressed as:

$$V_{Lm} = \frac{D}{1 - D} \cdot V_i$$ (5)

The voltage which across the second-side winding $V_{N2}$ and third-side winding $V_{N3}$ are expressed as follows

$$V_{N2} = n_2 \cdot V_i$$ (6)

$$V_{N3} = n_3 \cdot V_i$$ (7)

The voltage of the clamp capacitor $C_1$ can be denoted as

$$V_{C1} = V_{Lm} = \frac{D}{1 - D} \cdot V_i$$ (8)

By using the volt-second balance principle, (1) and (4) the follows equation can be represented as

$$\Delta i_{Lm(on)} = \Delta i_{Lm(off)}$$ (9)

Substituting (5)–(8) into (9), the output voltage $V_o$ can be derived as

$$\frac{V_o}{V_i} = \frac{(2 + n_2 + n_3) - n_3 \cdot D}{1 - D}$$ (10)

The circuit of the voltage gain and duty cycle of the coupled inductor at various turns ratios is shown in Figure 6. Compared with increasing the third-side winding $N_3$, increasing the secondary-side winding $N_2$ can obtain a higher voltage gain.
Effects of the ESRs on the semiconductor devices

Figure 7 shows the equivalent circuit including inductor copper inductances $r_{L1}$, $r_{L2}$, and $r_{L3}$, on resistances of diode $r_{D1}$, $r_{D2}$, and $r_{D3}$, and on resistance $r_{DS(on)}$ of the main switch. The following conditions of the proposed converter are assumed in this analysis of the Model:

1. The main switch parasitic capacitor and the diode capacitor are excluded.
2. During the switch is turned on can be modeled a resistance $r_{DS(on)}$, and during the switch turned off can be modeled an infinite resistance.
3. The diodes are modeled by the forward voltage $V_{D1}$, $V_{D2}$, and $V_{Do}$, and the forward resistances $r_{D1}$, $r_{D2}$, and $r_{Do}$. When the diodes are reversed-biased they can be modeled by an infinite resistance.

4. The effect of leakage inductances $L_{k1}$, $L_{k2}$, and $L_{k3}$ are neglected.

5. Switching loss and ESRs of capacitors are neglected.

6. Assumed the magnetizing inductor is sufficiently large to ensure a small-ripple current approximation.

7. To consider DC components during the off period, the average current is $I_{L1} = i_{L1(t)}$, and the average current is $I_{L2} = i_{L2(t)}$.

8. The capacitors $C_1$, $C_2$, and $C_o$ are assumed to be large enough and output voltage $V_o$ is constant.

Based on the Kirchhoff’s voltage law (KVL) principle, during the switch $S_1$ is turned on as shown in Figure 8(a), the following equations can be represented as follow

\[
V_i = V_{L1(on)} + i_{L1} \cdot r_{L1} + i_{DS} \cdot r_{DS} \tag{11}
\]

\[
V_{L1(on)} = V_i - i_{L1} \cdot (r_{L1} + r_{DS}) - i_{L2} \cdot r_{DS} \tag{12}
\]

\[
V_{C2} = V_i + V_{C1} + V_{L2(on)} + V_{L3(on)} - i_{L2} \cdot (r_{L2} + r_{L3} + r_{D2}) - i_{DS} \cdot r_{DS} - V_{D2} \tag{13}
\]

where

\[
i_{DS} = i_{L1} + i_{D1}
\]

\[
i_{L1} = i_{D1} + i_{L2}
\]

The current of output capacitors $C_O$, $C_1$, and $C_2$ are given as follow:

\[
i_{C1}^- = -i_{L2} \tag{14}
\]

\[
i_{C2}^+ = i_{L2} \tag{15}
\]

\[
i_{CO}^+ = -\frac{V_O}{R_L} = -i_O \tag{16}
\]

During the main switch $S_1$ is turned off as shown in Figure 8(b), the following equations can be represented as follow

\[
V_{C1} = V_{L1(off)} - i_{L1} \cdot r_{L1} - i_{D1} \cdot r_{D1} - V_{D1} \tag{17}
\]

\[
V_O = V_{CO} = V_i + V_{L1(off)} + V_{C2} + n_2 \cdot V_{L1(off)} - i_{L1} \cdot r_{L1} - i_{L2} \cdot (r_{L2} + r_{DO}) - V_{DO} \tag{18}
\]

The current of $C_1$, $C_2$, and output capacitor $C_O$ are given as follow

\[
i_{C1}^- = i_{L1} - i_{L2} \tag{19}
\]
\[ i_{C2}^- = -i_L \] (20)
\[ i_{CO}^- = i_L - i_O \] (21)

Substituting (13) into (18), the inductor voltage \( V_{L1(\text{off})} \) is derived as
\[
V_{L1(\text{off})} = \frac{1}{2 + n_2} \cdot \left[ V_O - V_i(2 + n_2 + n_3) + (i_{L1} \cdot (2r_{L1} + r_{DS})) + (i_{D1} \cdot r_{D1}) \right. \\
+ (i_{L1} \cdot (r_{L1} + r_{DS})) \cdot (a + b) + (i_{L2} \cdot r_{DS}) \cdot (a + b) \\
\left. + (i_{L2} \cdot (r_{L2} + r_{D2} + r_{DS})) + (i_{L2} \cdot (r_{L2} + r_{D2})) \right] + V_{D1} + V_{D2} + V_{D0}
\] (22)

Based on the amp-second balance principle, from (14)–(16) and (19)–(21) can be rewritten as follows:
\[
\int_0^{DT_S} i_{C1}^- dt + \int_{DT_S}^{T_S} i_{C1}^+ dt = 0 \] (23)
\[
\int_0^{DT_S} i_{C2}^- dt + \int_{DT_S}^{T_S} i_{C2}^+ dt = 0 \] (24)
\[
\int_0^{DT_S} i_{CO}^- dt + \int_{DT_S}^{T_S} i_{CO}^+ dt = 0 \] (25)

According to (25), the current flow path the \( C_o \) can be presented as
\[
- \frac{V_O}{R_L} \cdot DT_S + \left( i_{L2} - \frac{V_O}{R_L} \right) \cdot (1 - D)T_S = 0
\] (26)

Form equation (26), the current \( i_{L2} \) is determined as
\[
i_{L2} = \frac{1}{1 - D} \cdot \frac{V_O}{R_L}
\] (27)

According to (23), the current flow path the \( C_1 \) can be presented as
\[
- \frac{1}{1 - D} \cdot \frac{V_O}{R_L} \cdot DT_S + i_{C1} \cdot (1 - D)T_S = 0
\] (28)

Form equation (28), the current \( i_{D1} \) is determined as
\[
i_{D1} = \frac{D}{(1 - D)^2} \cdot \frac{V_O}{R_L}
\] (29)

According to (27) and (29), the current flow path the \( i_{L1} \) can be derived as follows
\[
i_{L1} = i_{D1} + i_{L2}
\] (30)
From (27) and (31), $i_{L1}$ can be rewritten as

$$i_{L1} = \frac{1}{1-D} \cdot \frac{V_O}{R_L}$$  \hspace{1cm} (31)$$

Where in the steady state, the principle of volt-second balance can be given as equation:

$$[V_i - [i_{L1} \cdot (r_{L1} + r_{DS})] - (i_{L2} \cdot r_{DS})] \cdot DT_S = \frac{1}{2 + n_2} \cdot$$

$$\{V_{CO} - V_i(2 + n_2 + n_3) + (i_{L1} \cdot (2r_{L1} + r_{DS}))$$
$$+ (i_{D1} \cdot r_{D1}) + (i_{L1} \cdot (r_{L1} + r_{DS})) \cdot (n_2 + n_3)$$
$$+ (i_{L2} \cdot r_{DS}) \cdot (n_2 + n_3) + (i_{L2} \cdot (r_{L2} + r_{L3} + r_{D2} + r_{DS}))$$
$$+ (i_{L2} \cdot (r_{L2} + r_{Do})) + V_{D1} + V_{D2} + V_{Do} \} \cdot (1-D)T_S$$  \hspace{1cm} (33)$$

Where $n_2 = \frac{N_2}{N_1}, n_3 = \frac{N_3}{N_1}$

Substituting (32) into (33), the equation can be rewritten as

$$V_O = \left( \frac{(2 + n_2 + n_3) - n_3 \cdot D}{1-D} \right) \cdot V_i - (V_{D1} + V_{D2} + V_{Do})$$
$$- \left[ (2 + n_2) \cdot \frac{D}{1-D} + (2 + n_2 + n_3) \right] \cdot i_{L1} \cdot r_{L1}$$
$$- 2(1-D) \cdot i_{L1} \cdot r_{L2} - (1-D) \cdot i_{L1} \cdot r_{L3}$$
$$- \left[ (2 + n_2) \cdot \left( \frac{D}{1-D} + D \right) + (1 + n_2 + n_3) \cdot (2-D) \right] \cdot i_{L1} \cdot r_{DS}$$
$$- [D \cdot r_{D1} + (1-D) \cdot (r_{D2} + r_{Do})] \cdot i_{L1}$$  \hspace{1cm} (34)$$

Substituting (31) into (34), the proposed converter output voltage $V_O$ is derived as
\[
V_O = \frac{(2 + n_2 + n_3) - n_3 \cdot D}{1 - D} \cdot V_i - V_O \\
\cdot \left\{ \frac{a}{(1 - D)^3 \cdot R_L} + \frac{b}{(1 - D)^2 \cdot R_L} + \frac{c}{(1 - D) \cdot R_L} \right\} \frac{d}{V_i}
\]

(35)

Where

\[
\begin{align*}
  a &= (2 + n_2) \cdot ((r_{L1} + r_{DS}) \cdot D) \\
  b &= (2 + n_2 + n_3) \cdot r_{L1} + (2 + n_2) \cdot r_{DS} \cdot D + (1 + n_2 + n_3) \cdot r_{DS} + r_{D1} \cdot D \\
  c &= 2r_{L2} + r_{L3} + (1 + n_2 + n_3) \cdot r_{DS} + r_{D2} + r_{D0} \\
  d &= (V_{D1} + V_{D2} + V_{D0})
\end{align*}
\]

and \( n_2 = \frac{N_2}{N_1}, n_3 = \frac{N_3}{N_1}. \)

From equation (35), the voltage conversion ratio \( V_O/V_i \) is represented as follows:

\[
\frac{V_O}{V_i} = \frac{(2 + n_2 + n_3) - n_3 \cdot D}{1 - D} \cdot \left[ 1 + \frac{a}{(1 - D)^3 \cdot R_L} + \frac{b}{(1 - D)^2 \cdot R_L} + \frac{c}{(1 - D) \cdot R_L} \right] \frac{d}{V_i}
\]

(36)

Where

\[
\begin{align*}
  a &= (2 + n_2) \cdot ((r_{L1} + r_{DS}) \cdot D) \\
  b &= (2 + n_2 + n_3) \cdot r_{L1} + (2 + n_2) \cdot r_{DS} \cdot D + (1 + n_2 + n_3) \cdot r_{DS} + r_{D1} \cdot D \\
  c &= 2r_{L2} + r_{L3} + (1 + n_2 + n_3) \cdot r_{DS} + r_{D2} + r_{D0} \\
  d &= (V_{D1} + V_{D2} + V_{D0})
\end{align*}
\]

The voltage gain and efficiency affected by different ESRs with coupled-inductor is shown in Figure 9. It can be seen that increase the equivalent series resistance \( r_{L1} \) is obtained lower voltage gain than increase the equivalent series resistance \( r_{L2} \) or \( r_{L3} \). The maximal voltage gain is constrained by the equivalent series resistances, and the efficiency will be decreased by the extreme duty ratio.

Neglecting the equivalent series resistance of the proposed converter, the ideal voltage gain can be expressed as

\[
M_{CCM} = \frac{V_O}{V_i} = \frac{(2 + n_2 + n_3) - n_3 \cdot D}{1 - D}
\]

(37)

According to (36), the equation can be reorganized and the equivalent circuit is shown in Figure 10 as follows

\[
V_i \cdot ((2 + n_2 + n_3) - n_3 \cdot D) - V_O \cdot (1 - D) - i_{L1} \cdot r_{L1} \cdot a - i_{L1} \cdot r_{L2} \cdot b \\
- i_{L1} \cdot r_{L3} \cdot c - i_{L1} \cdot r_{DS} \cdot d - i_{L1} \cdot r_{DX} - V_{DX} = 0
\]

(38)

Where

\[
\begin{align*}
  a &= (2 + 3 \cdot n_2 + n_3) - D \cdot (n_2 + n_3) \\
  b &= 2 \cdot (1 - D)^2 \\
  c &= (1 - D)^2 \\
  d &= 2 \cdot (1 + n_2 + n_3) \cdot D \cdot (1 - n_2 - 3 \cdot n_3 - D) \\
  d_1 &= (r_{D1} \cdot D - 1) + (r_{D2} + r_{D0}) \cdot (1 - D)^2 \\
  d_2 &= (V_{D1} + V_{D2} + V_{D0}) \cdot (1 - D)
\end{align*}
\]

and

\[
\begin{align*}
  r_{DX} &= r_{D1} \cdot D \cdot (1 - D) + (r_{D2} + r_{D0}) \cdot (1 - D)^2 \\
  V_{DX} &= (V_{D1} + V_{D2} + V_{D0}) \cdot (1 - D)
\end{align*}
\]
The input power and output power of the converter can be calculated as shown in equation (39) and (40), respectively.

\[ P_{in} = \frac{(2 + n_2 + n_3) - n_3 \cdot D}{C_0} V_i \cdot i_{L1} \]  

\[ P_{out} = \frac{1 - D}{C_1} V_o \cdot i_{L1} \]  

\[ \eta = \frac{P_{out}}{P_{in}} \]  

According to the equations (39)–(41), the converter efficiency can be derived as follows.

**Figure 9.** Voltage gain versus duty ratio and efficiency versus duty ratio under different ESRs with coupled-inductor.
\[ h = \frac{1}{C_0} \left( 2 + n_2 + n_3 - n_3 \cdot D \right) \]

\[ a \cdot r_{L1} + b \cdot r_{L2} + c \cdot r_{L3} + d \cdot r_{DS} = \left(1 - D\right)^3 \cdot R_L \]

\[ i_{L1} = \left(1 - D\right) \cdot V_o \]

From equation (42) shows that the efficiency is affected by the equivalent series resistance. Figure 11 shows the voltage gain and efficiency affected by various turns ratios and ESRs.

To analysis of the effect on leakage inductance and winding resistance leads to the current waveform being exponential functions at the off period of the switching cycle, as shown in Figure 12.

The maximal magnetizing current at ton as follow

\[ i_{Lm(peak)(on)} = \left( \frac{V_i}{L_m + L_{k1}} + \frac{V_i}{L_{k2} + L_{k3}} \right) \cdot t_{on} + t_i(0) \]  

(43)

The magnetizing current during switch \( S_1 \) in turned off can be given as follows:

\[ i_{Lm} = i_{Lk1} + n_2 \cdot i_{Do} \]  

(44)

\[ i_{Lk1} = i_{D1} + i_{Do} \]  

(45)

Substituting equations (45) into (44) derived as

\[ i_{Lm} = i_{D1} + (1 + n_2) \cdot i_{Do} \]  

(46)

During switch \( S_1 \) in turned off, the voltage across the magnetizing inductor \( V_{Lm} \) and leakage inductance \( L_{k1} \) can be expressed as
\[ V_{Lm} = L_m \frac{d}{dt} i_{Lm} = L_m \frac{d}{dt} (i_{D1} + (1 + n_2) \cdot i_{Do}) \]

\[ \Rightarrow V_{Lm} = L_m \frac{d}{dt} i_{D1} + (1 + n_2) \cdot L_m \frac{d}{dt} i_{Do} \quad (47) \]

\[ V_{Lk1} = L_{k1} \frac{d}{dt} (i_{D1} + i_{Do}) \quad (48) \]

**Figure 11.** The efficiency versus duty ratio under various turn ratios and ESRs.

**Figure 12.** The equivalent circuit during switch \( S_1 \) turned off period.
The voltage across the secondary winding $V_{L2}$ and the leakage inductance $L_{k2}$ can be expressed as

$$V_{L2} = n_2 \cdot L_m \frac{d}{dt} (i_{D1} + i_{Do}(1 + n_2))$$  \hspace{2cm} (49)$$

$$\Rightarrow V_{L2} = n_2 \cdot L_m \frac{d}{dt} i_{D1} + (n_2 + n_2^2) \cdot L_m \frac{d}{dt} i_{Do}$$  \hspace{2cm} (50)$$

$$V_{Lk2} = L_{k2} \frac{d}{dt} i_{Do}$$  \hspace{2cm} (51)$$

Based on the Kirchhoff’s voltage law (KVL) to find the inductor voltage during the switch $S_1$ is turned off period of each cycle is represented as follow:

$$V_o = V_i + V_{Lm} + V_{Lk1} + V_{C2} + V_{L2} + V_{Lk2} - (i_{D1} + i_{Do}) \cdot r_{L1} - i_{Do} \cdot r_{L2}$$  \hspace{2cm} (52)$$

Then

$$V_o - V_i - V_{C2} = V_{Lm} + V_{Lk1} + V_{L2} + V_{Lk2} - (i_{D1} + i_{Do}) \cdot r_{L1} - i_{Do} \cdot r_{L2}$$  \hspace{2cm} (53)$$

Therefore

$$V_o - V_i - V_{C2} = (L_m + L_{k1} + n_2 \cdot L_m) \frac{d}{dt} i_{D1} + ((1 + n_2)L_m + L_{k1} + (n_2 + n_2^2) \cdot L_m) \frac{d}{dt} i_{Do} - (i_{D1} + i_{Do}) \cdot r_{L1} - i_{Do} \cdot r_{L2}$$  \hspace{2cm} (54)$$

The other loop of current $i_{D1}$ flow through $D_1$ to charge the clamped capacitor $C_1$, the equation can be represented as:

$$V_{C1} = V_{Lm} + V_{Lk1} - (i_{D1} + i_{Do}) \cdot r_{L1}$$

$$\Rightarrow V_{C1} = (L_m + L_{k1}) \frac{d}{dt} i_{D1} + ((1 + n_2) \cdot L_m + L_{k1}) \frac{d}{dt} i_{Do} - (i_{D1} + i_{Do}) \cdot r_{L1}$$  \hspace{2cm} (55)$$

According equations (54) and (55) in matrix form can be rewritten as

$$\begin{bmatrix} V_o - V_i - V_{C2} \\ V_{C1} \end{bmatrix} = \begin{bmatrix} i_{D1}(t) \\ i_{Do}(t) \end{bmatrix}$$

$$\begin{bmatrix} (L_m + L_{K1} + n_2 \cdot L_m) \cdot D - r_{L1} \\ (L_m + L_{K1}) \cdot D - r_{L1} \end{bmatrix} \begin{bmatrix} ((1 + n_2) \cdot L_m + L_{K1} + (n_2 + n_2^2) \cdot L_m) \cdot D - (r_{L1} + r_{L2}) \\ ((1 + n_2) \cdot L_m + L_{K1}) \cdot D - r_{L1} \end{bmatrix} \begin{bmatrix} D \in \frac{d}{dt} \end{bmatrix}$$  \hspace{2cm} (56)$$

From equation (56), by using the Kramer Law to solving of the $i_{D1}$ and $i_{Do}$ can be derived as follow:
Substituting equations (59) and (60) into (57) and (58) given as

\[
i_{D1} = \frac{-K_1 \cdot r_{L1} + K_2 \cdot (r_{L1} + r_{L2})}{\alpha \cdot D^2 - \beta \cdot D - \gamma} = \frac{-K_1 \cdot \frac{r_{L1}}{\alpha} + K_2 \cdot \frac{(r_{L1} + r_{L2})}{\alpha}}{D^2 - \frac{\beta}{\alpha} \cdot D - \frac{\gamma}{\alpha}} = \frac{-K_1 \cdot \frac{r_{L1}}{\alpha} + K_2 \cdot \frac{(r_{L1} + r_{L2})}{\alpha}}{(D - P_1) \cdot (D + P_2)} \tag{57}
\]

\[
i_{Do} = \frac{-K_1 \cdot r_{L1} + K_2 \cdot r_{L1}}{\alpha \cdot D^2 - \beta \cdot D - \gamma} = \frac{-K_1 \cdot \frac{r_{L1}}{\alpha} + K_2 \cdot \frac{r_{L1}}{\alpha}}{D^2 - \frac{\beta}{\alpha} \cdot D - \frac{\gamma}{\alpha}} = \frac{-K_1 \cdot \frac{r_{L1}}{\alpha} + K_2 \cdot \frac{r_{L1}}{\alpha}}{(D - P_1) \cdot (D + P_2)} \tag{58}
\]

Where:

\[
\begin{align*}
\alpha &= n_2 \cdot L_m \cdot L_{k1} - (n_2^2 + n_2) \cdot L_m \cdot L_{k1} \\
\beta &= - \{ r_{L1} \cdot (n_2 \cdot L_m - (n_2^2 + n_2) \cdot L_m) + r_{L2} \cdot (L_m + L_{k1}) \} \\
\gamma &= - r_{L1} \cdot r_{L2}
\end{align*}
\]

and

\[
\begin{align*}
P_1 &= \frac{\beta + \sqrt{\beta^2 + (4 \alpha \gamma)}}{2 \alpha} \\
P_2 &= \frac{\beta - \sqrt{\beta^2 + (4 \alpha \gamma)}}{2 \alpha}
\end{align*}
\]

and

\[
\begin{align*}
K_1 &= V_O + V_i - V_{C2} \\
K_2 &= V_{C1}
\end{align*}
\]

and \( n_2 = \frac{N_2}{N_1}, n_3 = \frac{N_3}{N_1} \)

Substituting equations (57), (58) into (55) is obtained the following

\[
c_1 = \frac{r_{L1} - ((1 + n_2) \cdot L_m + L_{k1}) \cdot P_1}{(L_m + L_{k1}) \cdot P_1 - r_{L1}} \cdot d_1 \tag{59}
\]

\[
c_2 = \frac{r_{L1} - ((1 + n_2) \cdot L_m + L_{k1}) \cdot P_2}{(L_m + L_{k1}) \cdot P_2 - r_{L1}} \cdot d_2 \tag{60}
\]

Substituting equations (59) and (60) into (57) and (58) given as

\[
\begin{align*}
i_{D1}(t) &= A_1 \cdot d_1 \cdot e^{p_1 t} + A_2 \cdot d_2 \cdot e^{p_2 t} + A_3 \\
i_{Do}(t) &= d_1 \cdot e^{p_1 t} + d_2 \cdot e^{p_2 t} + A_4
\end{align*} \tag{61}
\]

Where:

\[
\begin{align*}
A_1 &= \frac{r_{L1} - ((1 + n_2) \cdot L_m + L_{k1}) \cdot P_1}{(L_m + L_{k1}) \cdot P_1 - r_{L1}} \\
A_2 &= \frac{r_{L1} - ((1 + n_2) \cdot L_m + L_{k1}) \cdot P_2}{(L_m + L_{k1}) \cdot P_2 - r_{L1}} \\
A_3 &= \frac{(K_1 - K_2)}{r_{L1}} \\
A_4 &= -\frac{(K_1 - K_2)}{r_{L2}}
\end{align*}
\]

From equation (61) the initial current of \( i_{D1} \) and \( i_{Do} \) are as follow respectively:
\[
\begin{align*}
    i_{D1}(0) &= I_p = A_1 \cdot d_1 + A_2 \cdot d_2 + A_3 \\
    i_{Do}(0) &= I_s = d_1 + d_2 + A_4
\end{align*}
\] (62)

By solving the equation (62) can be derived as follow:

\[
    d_1 = \frac{[I_p - A_3 \quad A_2]}{A_1 - A_2} = \frac{(I_p - A_3) - (I_s - A_4) \cdot A_2}{A_1 - A_2}
\] (63)

\[
    d_2 = \frac{[A_1 \quad I_p - A_3]}{A_1 - A_2} = \frac{(I_s - A_4) \cdot A_1 - (I_p - A_3)}{A_1 - A_2}
\] (64)

From equation (56) that the ESRs are neglected, the off period current \(i_{d1}\) and \(i_{do}\) can be derived as

\[
    i_{D1} = \frac{(V_O - V_i - V_{C2}) \cdot [(1 + n_1)L_m + L_{k1}] - V_{C1}[(1 + 2 \cdot n_1 + n_1^2)L_m + L_{k1}]}{(L_m + L_{k1} + a \cdot L_m)^2 - (L_m + L_{k1})[(1 + 2 \cdot n_1 + n_1^2)L_m + L_{k1}]} \cdot t + i_{D1}(0)
\] (65)

\[
    i_{Do} = \frac{V_{C1}(L_m + L_{k1} + a \cdot L_m) - (V_O - V_i - V_{C2})(L_m + L_{k1})}{(L_m + L_{k1} + a \cdot L_m)^2 - (L_m + L_{k1})[(1 + 2 \cdot n_1 + n_1^2)L_m + L_{k1}]} \cdot t + i_{D2}(0)
\] (66)

According to equations (57) to (65), the diode currents \(i_{D1}\) and \(i_{Do}\) are exponential due to the R-L circuit formation between the equivalent series resistances and the leakage inductances. The diode current waveforms \(i_{D1}\) and \(i_{Do}\) are shown in Figure 13.

**Analysis of voltage stress of the power devices**

The voltage stress is an important issue related to the cost and efficiency of converter. Due to low voltage rating and low \(r_{DS(on)}\) of power switch can be utilized in the circuit. Therefore, the switching and conduction losses can be reduced. In addition, the lower cost and higher efficiency of the converter can be received.

The voltage stress across power switch \(V_{DS}\) can be equaling the summation of DC-source \(V_i\) and magnetizing inductor voltage \(V_{Lm}\) in turned off period. Therefore, the voltage stress across power switch \(S_1\) is

\[
    V_{DS} = \frac{1}{1 - \bar{D}} \cdot V_i
\] (67)

\[
    M_S = \frac{V_{DS}}{V_O} = \frac{1}{(2 + n_2 + n_3) - n_3 \bar{D}}
\] (68)

While the switch \(S_1\) is turned on, the diodes \(D_1\) and \(D_o\) are reverse-biased. Therefore, the voltage stresses of diodes \(D_1\) and \(D_o\) is as follows
While the switching $S_1$ is turned off, the diode $D_2$ is reverse-biased. Therefore, the voltage stresses across $D_2$ is as follows

$$V_{D_2} = \frac{1 + n_2 + 2n_3 - 2n_3D}{1 - D} \cdot V_i$$

**Experiment of the proposed converter**

The converter is tested to operate at the 48 V dc-input voltage and the switching frequency $f_s$ is 50 kHz. The output voltage and output power are specified as $V_o = 400$ V and $P_o = 1$ kW respectively, and by using the current mode PWM IC UC3845 to achieved performance of the circuit. From the above design procedure, the power switch is selected as IXFH120N20P which has low ON state resistance $r_{DS(on)}$ of 22 mΩ and is rated at 200 V. The winding $N_1:N_2:N_3$ is obtained as 1:1:2. The diode $D_1$ selected as B30H150G is Schottky diode and is rated at 150 V, 30 A. The voltage stress of voltage diodes $D_2$ and $D_O$ are larger than $D_1$. Schottky diodes are not suitable for utilized. Therefore, diodes $D_2$ and $D_O$ are selected as fast diode DSEI8-06A which are rated at 600 V, 8 A. Table 1 lists the main components and parameter requirements for the prototype.
This section introduces the voltage waveform and current waveform at each point of the converter under a full load of 1 kW. Figure 14 shows the converter’s magnetizing inductance current $i_{Lm}$ and the power switches $V_{GS}$ and $V_{DS}$.

Table 1. Components and parameters in the proposed converter.

| Components                  | Specifications |
|-----------------------------|----------------|
| MOSFET $S_1$                | IXFH120N20P    |
| Diode $D_1$                 | B30H150G       |
| Diode $D_2/D_o$             | DSEI8-06A      |
| Magnetic core               | MPP core       |
| Coupled-inductor turns ratio| $N_1:N_2:N_3 = 1:1:2.2$ |
| Magnetizing inductor $L_{m}$| 185 uH         |
| Leakage inductor $L_{k1}$   | 3.15 uH        |
| Capacitor $C_1$             | 200 V/470 uF   |
| Capacitor $C_2$             | 450 V/180 uF   |
| Capacitor $C_o$             | 450 V/180 uF   |
| PWM IC                      | UC3845         |

Figure 14. Experimental coupled-inductor current and power switch voltage waveforms under various output power: (a) 250 W, (b) 500 W, (c) 750 W, and (d) 1 kW.
And as shown in Figure 15, when the output voltage $V_O = 400$ V, the power switch $V_{DS}$ can be clamped to avoid high voltage stress. The voltage across the diodes $D_1$, $D_2$, and $D_O$ are shown in Figure 16.

The cut-off voltage of $V_D$ and $V_{DO}$ is less than the output voltage. The clamping circuit of the charging current $i_D$ is shown in Figure 17(a). The inrush current is caused by the leakage inductance of the coupled inductor while the power switch turned-off. Furthermore, the leakage inductance energy is recycled to the capacitor $C_1$ for further improve the efficiency of the converter. Figure 17(b) shows that the current $i_D$ of the secondary-side winding $N_2$ is connected in series with $V_i$, $V_{C1}$, and $V_{N2}$ to charge capacitor $C_2$. Figure 17(c) depicts the output current $i_{Do}$ of the energies of $V_i$, $L_n$, $C_2$, and $N_2$ charge output capacitor $C_o$ and load $R_o$. As shown in Figure 18, the efficiency of the converter under different output powers $P_O$, where the maximum efficiency is about 96.5% at 200 W, and the efficiency is about 92.3% at a full load of 1 kW.
Figure 17. Experimental current flow through diodes of the proposed converter with $V_O = 400\,\text{V}$ and $P_O = 1\,\text{kW}$: (a) $D_1$, (b) $D_2$, and (c) $D_O$. 
Conclusion

This paper proposes a non-isolated high-boost DC/DC converter. The converter architecture combines switched capacitor technology, boost capacitor technology, and capacitor diode voltage doubler technology, not only can recover the leakage inductance energy on the coupled inductor, improve the conversion efficiency, but also has a higher voltage gain. In addition, the active clamp circuit limits the peak voltage on the $V_{DS}$ of the power switch, reducing the voltage stress of the power switch. Based on the above conditions, this paper proposes that the converter architecture achieves high voltage gain, high efficiency, and effective suppression of voltage stress, and can be effectively applied to the conversion system of green energy grids and electric vehicle charging station.

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