PURINE: A BI-GRAPH BASED DEEP LEARNING FRAMEWORK

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ABSTRACT

In this paper, we introduce a novel deep learning framework, termed Purine. In Purine, a deep network is expressed as a bipartite graph (bi-graph), which is composed of interconnected operators and data tensors. With the bi-graph abstraction, networks are easily solvable with event-driven task dispatcher. We then demonstrate that different parallelism schemes over GPUs and/or CPUs on single or multiple PCs can be universally implemented by graph composition. This eases researchers from coding for various parallelization schemes, and the same dispatcher can be used for solving variant graphs. Scheduled by the task dispatcher, memory transfers are fully overlapped with other computations, which greatly reduces the communication overhead and helps us achieve approximate linear acceleration.

1 INTRODUCTION

The need for training deep neural networks on large-scale datasets has motivated several research works that aim to accelerate the training process by parallelising the training on multiple CPUs or GPUs. There are two different ways to parallelize the training. (1) Model parallelism: the model is distributed to different computing nodes (Sutskever et al., 2014) (2) Data parallelism: different nodes train on different samples for the same model (Seide et al., 2014; Chilimbi et al., 2014). Some of the works even use a hybrid of them (Krizhevsky, 2014; Dean et al., 2012; Le, 2013). For data parallelism, there are also two schemes regarding communication between the peers. (1) the allreduce approach where all updates from the peers are aggregated at the synchronization point and the averaged update is broadcasted back to the peers (Seide et al., 2014; Krizhevsky, 2014). (2) the parameter server approach handles the reads and writes of the parameters asynchronously (Dean et al., 2012; Le, 2013; Chilimbi et al., 2014). Efficient implementations of the various parallelization schemes described by previous works are non-trivial.

To facilitate the implementation of various parallelization schemes, we built a bigraph-based deep learning framework called “Purine”. It is named “Purine”, which is an analog of caffeine in molecular structure, because we benefited a lot from the open source Caffe framework (Jia et al., 2014) in our research and the math functions used in Purine are ported from Caffe.

2 BI-GRAPH ABSTRACTION

Purine abstracts the processing procedure of deep neural networks into directed bipartite graphs (Bi-Graphs). The Bi-Graph contains two types of vertices, tensors and operators. Directed edges are only between tensors and operators and there is no interconnection within tensors or operators. Figure 1 illustrates the Bi-Graph for the convolution layer defined in Caffe.

All feed-forward neural nets can be represented by a directed acyclic bipartite graph, which can be solved by a universal task dispatcher. There are several works that use similar abstractions. For
Figure 1: (a) shows the convolution layer defined in Caffe together with its inputs and outputs. (b) is the corresponding bipartite graph that describes the underlying computation inside the convolution layer. There are two types of vertices in the Bi-Graph. Boxes represent data tensors and the circles represent operators. Operators are functions of the incoming tensors and the results of the functions are put in the outgoing tensors.

example, the dataflow graph in Dryad [Isard et al., 2007] and Pig Latin [Olston et al., 2008] are the same as the Bi-Graph abstraction introduced in this paper. Graphlab [Low et al., 2010] proposed a more general abstraction which is applicable to iterative algorithms. However, these systems are designed for general problems and do not support GPU. Theano [Bergstra et al., 2010] compiles math expressions and their symbolic differentiations into graphs for evaluation. Though it supports GPU and is widely used for deep learning, the ability to parallelize over multiple GPUs and over GPUs on different machines is not complete.

2.1 Task Dispatcher

Purine solves the Bi-Graph by scheduling the operators within the Bi-Graph with an event-driven task dispatcher. Execution of an operator is triggered when all the incoming tensors are ready. A tensor is ready when all its incoming operators have completed computation. The computation of the Bi-Graph starts from the sources of the graph and stops when all the sinks are reached. This process is scheduled by the task dispatcher.

2.2 Iterations

Although it has been argued in Low et al. [2010] that the directed acyclic graph could not effectively express iterative algorithms as the graph structure would depend on the number of iterations. We overcome this by iteration of the graphs. Because the task dispatcher waits until all the sinks of the graph are reached, it acts as a synchronization point. Thus parallelizable operations can be put in a single graph, while sequential tasks (iterations) are implemented by iteration of graphs. A concrete example is shown in Figure 2.

3 Parallelization

Parallelization of the Bi-Graph on a cluster of CPUs or GPUs or mixed can be easily implemented by introducing a “location” property for the tensors and operators. The “location” property uniquely identifies the computation resource (CPUs/GPUs) on which a tensor/operator should be allocated. The “location” property comprises two fields: hostname and device id. In a multi-machine cluster, hostname identifies the machine that the vertex resides on. Device id specifies whether the tensor/operator should be allocated on CPU or GPU and the ordinal of the GPU if there are multiple GPUs installed on a single machine. Besides the “location” property, another property “thread” is assigned to operators because both CPU and GPU support multithreading. Operators with the same
Figure 2: Implementation of SGD by Graph iteration. Every iteration of SGD calculates a modification of the network parameter, and updates the parameter before the next iteration. Since direct updating the network parameter would form a cyclic loop in the graph, it is dissected into two parts. (a) The DNN graph calculates the updated parameters and places them in “new params”, (b) The swap graph will swap the memory address of the “new” and “old” parameters. As a whole, SGD is implemented by iterating the two graphs as in (c).

thread id will be queued in the same thread, while those with different ids are parallelized whenever possible. It is up to the user to decide the assignment of the graph over the computation resources.

3.1 Copy Operator

In the multidevice setting, data located on one device are not directly accessible by operators on another. Thus a special “Copy” operator is introduced to cross the boundary, connecting parts of the Bi-Graph on individual devices. The Copy operators, just like other operators, are scheduled by the task dispatcher. Therefore it is straightforward to overlap copy operations with other computation tasks by assigning different threads to them.

3.2 Task Dispatcher

In the case of single machine and multiple devices, only one dispatcher process is launched. Operators are associated to their threads and scheduled by the global task dispatcher. In the case of multiple machines and multiple devices, individual dispatcher processes are launched on each of the machines. Copy operators that copy data from machine A to machine B are sinks on machine A and sources on machine B. This way, each machine only needs to schedule its own subgraph and no global scheduling mechanism or communication between dispatchers is necessary.

3.3 Model Parallelism

We demonstrate how model parallelism can be implemented in Purine by taking a two-layer fully connected neural network as example. It can be extended to deeper networks easily. As is shown in Figure 3, execution of the two-layer network can be divided into three sequential steps. They are labeled as A, B, C correspondingly. To keep resources busy all the time, the network is replicated three times and executed in order.

3.4 Data Parallelism

Data parallelism is a simple yet straightforward way to parallelize deep networks. In data parallelism, computation peers each keep a replicate of the deep network. The communication between peers can be either synchronous or asynchronous. In the synchronous case, the gradients from peers are gathered by the parameter server. The updated parameter is calculated and copied back to all the peers.

A hybrid of data parallelism and model parallelism has previously been proposed by [Krizhevsky, 2014] in which the convolution layers use data parallelism and fully connected layers use model parallelism. This is based on the observation that the number of parameters is large and thus the communication cost is big for fully connected layers. The hybrid approach greatly reduces the communication cost. A different approach to reduce communication overhead is to overlap the data
transfer with computations. Double buffering is proposed by Seide et al. (2014) to break a minibatch in half and exchange the gradients of the first half while doing computation of the second half.

With the scheduling of the task dispatcher in Purine, we propose a more straightforward way to hide the communication overhead. We show that data parallelism is feasible even for fully connected layers, especially when the network is very deep. Since the fully connected layers are usually at the top of the neural networks, exchange of the parameter gradients can be overlapped with the backward computation of the convolution layers. As is shown in Figure 4, exchange of gradients in the higher layer can be overlapped with the computation of lower layers. Gradient exchange of lower layers could be less of a problem because they usually have a much smaller number of parameters.

Figure 3: Implementing model parallelism in Purine. (a) The two-layer network can be divided into three subgraphs which execute in sequence. (b) The network is replicated three times and executed in order.

Figure 4: Overlapping communication with computation.
4 RESULTS

We carried out experiments on the Purine framework with data parallelism on GoogLeNet (Szegedy et al., 2014). Data parallelism often results in larger batch sizes, which are unfavorable for SGD convergence demonstrated by previous studies. In this paper we ignored the possible change in convergence rate but instead studied how much more data can be processed per unit time with the parallelization.

We compared the number of images processed per second for GoogLeNet with different numbers of GPUs for data parallelism. The batch size we use is 128 per GPU. There are 3 GPUs installed on each workstation, interconnected with 10 Gigabit Ethernet.

As is shown in Table 1, the speed increases linearly with more GPUs added. The speed is faster than the previous version of this paper because we upgraded the CUDNN library to version 2, which is faster compared to version 1.

Note that the machines are connected by 10 gigabit ethernet and thus data on GPU need to go through CPU memory to be transferred over the ethernet. Even with this limitation, the speed up is linear thanks to the overlapping of communication with computation.

Table 1: Number of images per second with increasing number of GPUs. (GPU number smaller than or equal to 3 are tested on single machine. Performances of GPU number larger than 3 are on different machines interconnected with 10 Gigabit Ethernet.)

| Number of GPUs | 1   | 2   | 3   | 6   | 9   | 12  |
|----------------|-----|-----|-----|-----|-----|-----|
| Images per second | 112.2 | 222.6 | 336.8 | 673.7 | 1010.5 | 1383.7 |

Running GoogLeNet with 4 GPUs on a single machine is profiled and shown in Figure 5. It can be seen that the memory copy of model parameters between CPUs and GPUs is fully overlapped with the computations in the backward pass. The only overhead is in the first layer of the network, which results in the gap between iterations.

It is favorable to have small batch size in stochastic gradient descent. However, regarding parallelism, it is more favorable to have larger batch size and thus higher computation to communication ratio. We searched for the minimum batch size possible to achieve linear speed up by exploring different batch sizes.

Figure 5: Profiling results of Purine. Memory copies (row 1 and 2) are overlapped with computation (row 3). The only overhead is the memory copy of first convolution layer, which results in the gap between iterations.

Table 2: Number of images per second with 12 GPUs and different batch sizes.

| Batch size per GPU | 128 | 64 | 56 | 48 | 40 | 32 |
|--------------------|-----|----|----|----|----|----|
| Images per second  | 1383.7 | 1299.1 | 1292.3 | 1279.7 | 1230.2 | 1099.8 |
| Acceleration Ratio | 12 | 11.26 | 11.20 | 11.09 | 10.66 | 9.53 |

Table 2 shows the processing speed with different batch sizes. The acceleration ratio is not reduced much with batch size 64 as compared to 128. We can still achieve 9.53 fold acceleration with 12 GPUs when the batch size is set to 32.
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