First test results of the trans-impedance amplifier stage of the ultra-fast HPSoC ASIC

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Abstract: We present the first results from the HPSoC ASIC designed for readout of Ultra-fast Silicon Detectors. The 4-channel ASIC manufactured in 65 nm CMOS by TSMC has been optimized for 50\,\mu m thick AC-LGAD. The evaluation of the analog front end with $\beta$-particles impinging on $3 \times 3$ AC-LGAD arrays (500\,\mu m pitch, $200 \times 200\,\mu m^2$ metal) confirms a fast output rise time of 600\,ps and good timing performance with a jitter of 45\,ps. Further calibration experiments and TCT laser studies indicate some gain limitations that are being investigated and are driving the design of the second-generation pre-amplification stages to reach a jitter of 15\,ps.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; Timing detectors; VLSI circuits
1 Introduction

Low Gain Avalanche Detectors (LGADs) are thin silicon detectors (ranging from 20 to 50 \( \mu m \) in thickness) with moderate internal signal amplification (up to a gain of \( \sim 50 \)) [1, 2], providing timing measurements for minimum-ionizing particles with resolution of about 30 ps [3, 4]. In addition, the fast rise time (as low as 180 ps for 20 \( \mu m \) thickness) and short full charge collection time (around 1 ns) of LGADs are suitable for high repetition rate measurements in photon science and other fields [5, 6]. The first implementation will be the High-Granularity Timing Detector (HGTD) in ATLAS [7] and the Endcap Timing Layer (ETL) in CMS [8] for the LHC upgrade.

Future applications in the ePIC [9] and PIONEER [10] experiments will require high precision in both time and space. High precision spatial resolution while maintaining a 100% fill factor is provided by the increased segmentation of AC-LGADs [11] (also named Resistive Silicon Detectors RSD). This is achieved by employing an un-segmented (p-type) gain layer and (n-type) N-layer, and a di-electric layer separating the metal readout pads. The design allows to decrease the number of readout channels and the value of the sensor capacitance. Versions of AC-LGADs have shown to provide spatial resolution on the scale of few to 10s of micrometers [12].

In this paper we describe the development and first measurements of the ASIC “HPSoC” prototype optimized for fast read out of AC-LGAD. We first describe the properties of the sensor signals and derive the requirements for the readout ASICs. Then we give an overview of the basic function of the ASIC, followed by results from the electric characterization using fast calibration signals. This is followed by the investigation of the response to IR laser TCT and \( \beta \) particles impinging on an AC-LGAD array wire-bonded to the ASIC, and by the interpretation of the results in terms of the expected jitter.
2 Concept and design of HPSoC ASIC

2.1 LGAD signals

The requirements for the ASIC performance are derived from the measured signal current from MIPs in a typical AC-LGAD. Signals for AC-LGAD of 20 and 50 μm thickness, with an internal gain of 20, are shown in figure 1. It shows the characteristic dependence of LGAD signals on the sensor thickness, i.e. the maximum current does not depend on the thickness, while the rise time and slew rate dV/dt do.

![Figure 1](image1.png)

Figure 1. Input current from AC-LGAD with gain = 20 measured for 50 μm sensor thickness and scaled for 20 μm sensor thickness.

The signal characteristics critical for the jitter, the time resolution depending on the electronics, are shown in table 1, which in turn yield the ASIC design goals summarized in table 2.

| LGAD Thickness | 50 μm | 20 μm |
|----------------|-------|-------|
| Rise time (10–90%) [ps] | 455 | 182 |
| Input charge (G = 20) [fC] | 11 | 4.6 |
| I_{MPV} input current [μA] | 15 | 15 |

### Table 1. MIP signal characteristics.

| ASIC parameter | 50 μm | 20 μm | Comment |
|----------------|-------|-------|---------|
| Rise time [ps] | 455 | 182 | Rise time (electronics) = Rise time (sensor signal) |
| Jitter [ps] | 10 | 5 | <30% of the “Landau” noise |
| S/N | >50 | >40 | S/N = Rise Time/Jitter |
| Voltage signal [mV] | 70 | 70 | V_{MPV} = R_{FB} * I_{MVP} [R_{FB} = 5 kΩ] |
| Noise RMS [mV] | 1.4 | 1.8 | N = S/(S/N) |
| Internal sensor gain | >20 | >20 |

### Table 2. ASIC design goals.

2.2 ASIC design and layout

The HPSoC design implements signal pre-amplification along with full waveform sampling and digitization in an ultra-small area package size compatible with small-pitch sensors [13]. It is
designed to service up to 100 channels in a single die for bidimensional sensor arrays with a pitch as small as 300 μm. The HPSoC will operate with 10 GSa/s waveform digitization and will implement autonomous triggering, feature extraction and multichannel data fusion. The goals for the ASIC design are shown in table 2. They are based on matching the amplifier rise time to the sensor rise time. The amount of allowable jitter is given by the requirement that the jitter should contribute only a small fraction (<10%) to the total time resolution.

The design and fabrication of a 4-channel HPSoC prototype discussed here emphasizes initially the first stage Trans-Impedance Amplifier (TIA) shown figure 2. This small prototype ASIC includes a subset of the components which will be required for the full HPSoC design and has been manufactured using a standard 65 nm CMOS process by TSMC. Figure 3 (left) shows a photo of the prototype chip with annotated inputs.

![Figure 2. Schematic of the HPSoC TIA.](image)

![Figure 3. (Left) Micrograph of fabricated 1.5 mm × 1.0 mm HPSoC prototype chip; (right) test board with AC-LGAD sensor wire-bonded to HPSoC prototype ASIC.](image)
3 Results

The HPSoC ASIC prototype was mounted on a PCB that was custom designed to read out one channel of the chip during electrical calibration, laser TCT and charge collection with β-particles. The TIA was read out with a fast oscilloscope and the signal was analyzed in terms of the collected charge, the maximum of the pulse height (Pmax), the rise time (10–90%) and the RMS noise of the baseline. While the calibration was performed without load, for the laser TCT and β-particle charge collection, the ASIC input was wire bonded to a LGAD or AC-LGAD as described below. The arrangement is shown in figure 3 (right).

3.1 Calibration results

Then calibration pulse was generated by passing a step pulse of 200 ps rise time and height P through a 0.1 pF capacitor, thus creating an input charge of 0.1* P [fC/V]. The output of the TIA is shown in figure 4 (left) when recorded with a differential probe with three different scope bandwidths. While the signals taken at 2.0 GHz and 13.5 GHz are indistinguishable, the pulse taken at 500 MHz is clearly slowed down. Thus, the charge collection data was recorded using the 2.0 GHz scope bandwidth, since that setting exhibits lower noise RMS than the 13.5 GHz setting. Figure 4 (center) shows the signal amplitude as a function of the input charge: it is linear up to 100 fC input and its slope is reduced to 1/3 above 200 fC. Figure 4 (right) shows a rise time as low as 300 ps, the same order of magnitude as the rise time of the input pulse mentioned above.

![Figure 4. TIA output: (left) calibration pulse recorded with scope bandwidth 500 MHz, 2.5 GHz and 13.5 GHz; (center) calibration Pmax vs. input charge, (right) 10–90% rise time, both for calibration and TCT.]

3.2 Laser TCT results

For the laser TCT one channel of the ASIC was wire-bonded to a 60 µm thick 3 × 3 AC-LGAD array from the FBK RSD1 production (500 µm pitch, 200 × 200 µm² metal pads, capacitance ~120 fF). The IR laser beam was focused close to the connected pad and the input signal was varied by increasing the sensor gain with the bias voltage. As shown in figure 4 (right), the observed rise time for TCT of between 600 and 800 ps is about twice rise time from the calibration, since it includes the rise time of the sensor signal.
3.3 β-scope results

The response to β particles was tested to determine the time jitter, calculated event-by-event from the rise time $T_{\text{rise}}$ and the signal-to-noise ratio $\text{SNR} = \text{Signal}/\text{Noise}$ [1]:

$$\text{Jitter} = \frac{\text{Noise}}{(dV/dt)} \approx \frac{T_{\text{rise}}}{\text{SNR}}.$$  

This was done on two different LGAD types: the timing and pulse shapes were tested with the AC-LGAD described above. To measure the signal height ($= P_{\text{max}}$) would require readout of all neighboring pads sharing the created pulse. Therefore, the SNR was determined by comparing the pulses from a single pad of a 50 μm thick TI-LGAD, read out by either HPSoC or the fast single channel discrete component “UCSC” board based on SiGe transistor technology [4]. In both cases the noise was of the order of RMS $\approx 1 \text{ mV}$.

3.3.1 Response to AC-LGAD

The β data using the AC-LGAD was taken with an elevated self-trigger threshold. The pulse shape of the HPSoC shown in the insert of figure 5 (left) indicates the very fast rise time and somewhat slower fall-time of the pulse. The main histogram of figure 5 (left) is the 10–90% rise time of the AC-LGAD sensor with a mean of 677 ps. Since this was done with a 60 μm thick sensor, we can scale this number by the sensor thickness to arrive at

$$\text{Rise time (50 μm)} = 677 \ast (50/60) \text{ ps} = 564 \text{ ps},$$  

which is within 20% of the goal in table 2.

![Figure 5. HPS0C β-pulse data from a 60 μm thick AC-LGAD: (left) rise time with a mean of 677 ps (insert: pulse shape); (right) observed jitter vs. $P_{\text{max}}$.](image)

The jitter distribution in figure 5 (right) indicates the expected $1/P_{\text{max}}$ dependence.

3.3.2 Response to TI-LGAD

Although the HPSoC pulse shape in the insert of figure 5 (left) appears to be very sharp, a comparison with the TI-LGAD pulses using the UCSC board in figure 6 shows the longer tail and the lower signal height of the HPSoC, even though the rise times are comparable. The pulse height
Figure 6. Average β-pulse distributions from a 50 μm thick TI-LGAD sensor read out by: (left) HPSoc prototype, and (right) single-channel UCSC board (“SC”) compared to HPSoc prototype (with arbitrary delay, note the different time and voltage scales).

...ratio is about 4 and the pulse width ratio about 1/3. Using the value of the pulse height Pmax = 28 mV from figure 6 (left), we can estimate a HPSoc jitter of 45 ps. A redesign of the TIA to “sharpen” the backend of the pulse to gain a factor 3 in pulse height would result in Pmax = 84 mV and a jitter of between 10 to 20 ps.

4 Conclusions

The HPSoc prototype shows very good rise time: 300 ps calibration, 564 ps for 50 μm sensor.

Lower gain and wider pulse width are observed with respect to circuit simulation, which is currently being investigated.

Future work will include the optimization of the input stage, such as lowering the input impedance, co-optimization for the digitizer load target, and optimization for different sensor geometries, i.e. longer strips.

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