Reliability analysis of component-level redundant topologies for solid-state fault current limiter

Masoud Farhadi, Mehdi Abapour and Behnam Mohammadi-Ivatloo

Department of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran

ABSTRACT
Experience shows that semiconductor switches in power electronics systems are the most vulnerable components. One of the most common ways to solve this reliability challenge is component-level redundant design. There are four possible configurations for the redundant design in component level. This article presents a comparative reliability analysis between different component-level redundant designs for solid-state fault current limiter. The aim of the proposed analysis is to determine the more reliable component-level redundant configuration. The mean time to failure (MTTF) is used as the reliability parameter. Considering both fault types (open circuit and short circuit), the MTTFs of different configurations are calculated. It is demonstrated that more reliable configuration depends on the junction temperature of the semiconductor switches in the steady state. That junction temperature is a function of (i) ambient temperature, (ii) power loss of the semiconductor switch and (iii) thermal resistance of heat sink. Also, results’ sensitivity to each parameter is investigated. The results show that in different conditions, various configurations have higher reliability. The experimental results are presented to clarify the theory and feasibility of the proposed approaches. At last, levelised costs of different configurations are analysed for a fair comparison.

ARTICLE HISTORY
Received 26 February 2017
Accepted 20 August 2017

KEYWORDS
Power electronics; semiconductors; fault current limiter; reliability; redundant

1. Introduction
Nowadays, increasing consumption demand and continuous growth of distributed generation has led to short-circuit-level increment in interconnected networks. This exceeded current is one of the main concerns of network operators. In recent years, various solutions are proposed to solve this problem. Considering their technical, political and economic difficulties, the use of fault current limiter (FCL) is one of the most promising proposed methods (Fotuhi-Firuzabad, Aminifar, & Rahmati, 2012; Kim & Kim, 2011). Up to now, different studies have been carried out on FCLs with specifically focused on their impacts on reliability of faulty systems (Fotuhi-Firuzabad et al., 2012; Kazemia & Lehtonenb, 2013). But issues like FCL reliability calculations or fault-tolerant design are not discussed, while reliability of FCL has a large effect on its impact on system reliability.

Recently, various solutions have been proposed for fault-tolerant design. These solutions could be classified into two major categories: (1) algorithmic solutions without change of the existing hardware (Farhadi, Abapour, & Sabahi, 2016; Jamshidpour, Poure, & Saadate, 2016) and (2) fault-tolerant designs with redundant hardware (Aghdam & Abapour, 2016; Cho, Kwak, & Lee, 2015; Farhadi, Tahmasbi-Fard, Abapour, & Tarafdar-Hagh, 2017). The second category could be also divided into four categories: (1) component level, (2) leg level, (3) module level and (4)
system level (Zhang et al., 2014). Component-level redundancy, in general, is the duplication of extra switches in order to have a backup in the case of post-fault (Chen, Zhang, He, & Cui, 2009; Kou, Corzine, & Familiant, 2004). Leg-level redundancy is provided by incorporating extra legs in parallel or series connection into the main legs. Extra leg is added to override the effects of a failed leg. Module-level redundancy can be further subdivided into (1) neutral shift, (2) DC-bus voltage reconfiguration and (3) redundant module installation. Neutral-shift strategy attempts to adjust phase shifts among phase-voltage references to maintain balanced line-to-line voltages in post-fault (Lezana & Ortiz, 2009; Song-Manguelle, Thurnherr, Schroder, Rufer, & Nyobe-Yome, 2010). The second strategy involves attempts to sustain an unchanged output voltage by raising the input voltage (Maharjan, Yamagishi, Akagi, & Asakura, 2010). Redundant module installation, in general, is the duplication of extra modules in order to have a backup in the case of post-fault (Son et al., 2012). System-level redundancy is the most expensive redundancy that can be employed in industrial applications. Two usual types of system-level redundancy are the cascaded redundant and the parallel redundant (Fischbachee, 1958; Flannery & Venkataramanan, 2008). Among hardware redundancy solutions, the component-level redundant solution achieves a better compromise between the system cost and simplicity that has become a hot area of fault-tolerant research.

In (Richardseau and Pham (2013), the authors present a global reliability comparison between two-level and three-level/five-level inverter topologies in single- and three-phase operations. Harb et al. have proposed a new methodology for calculating the reliability of the photovoltaic module-integrated inverter based on a stress factor approach (Harb & Balog, 2013). In Arifujjaman, Liuchen (2012), the reliability analysis of the power electronic converters for a grid connected permanent magnet generator-based wind energy conversion system is presented. In Valipour, Fotuhi-Firouzabad, Rezazadeh, and Zolghadri (2015), FIDES method has been governed to estimate the reliability of two industrial AC/DC converters with resonant and non-resonant topologies. In Caroline, Vincent, and Guy (2007), a study of different inverter topologies to increase reliability and avoid an expensive redundancy is presented. Many points have been considered and discussed for performance of parallel and series connected switches in previous researches. However, the reliability point of view has not been studied.

For the first time to our knowledge, in this article, a comparative reliability analysis between different component-level redundant topologies for FCL has been proposed. Though the methodology presented is general and can be extended to other similar power electronics systems, results associated with a solid-state fault current limiter (SSFCL) are presented and discussed in this work. Two different operation scenarios (perfect fault coverage and imperfect fault coverage) are considered and more reliable configurations are determined for different operation scenarios.

In order to ensure increasing current and voltage rating of power switches, paralleling and serialising are inevitable. On the other hand, it is a technical challenging task to ensure proper current and voltage sharing between the parallel and series connected semiconductor switches. Control strategies have been suggested in Bortis, Beila, and Kolar (2007), Gibbs and Kimmel (2001) and Musumeci, Pagano, Frisina, and Melito (2002) to improve the dynamic and static sharing between switches. It should be noted that prior to this, the voltage and current ratings of commercially available semiconductors were limited and far below high-voltage application requirements. Therefore, the suitable topology was selected based on available ratings of semiconductors. But today, currently available semiconductors are able to endure surge current up to 80 kA. In consequence, reliability challenges should be considered in power electronics circuit design.

It is demonstrated that the more reliable configuration is determined by the junction temperature of the switches. This is because of high contribution of temperature factor in failure rate of power semiconductor devices. The junction temperature is a function of ambient temperature, power loss of the semiconductor switch and thermal resistance of heat sink. By controlling these parameters, we can achieve an appropriate configuration with more reliability.
2. **Length state space diagrams and MTTFs of different redundant topologies for SSFCL**

SSFCL topologies are classified into three major groups: the series switch, the bridge and the resonant types (Abramovitz & Smedley, 2012). In this article, without loss of generality, a generic topology of the series switch-type FCL is selected for discussion and analysis. The topology of series switch-type FCL incorporated in a single-phase power line as shown in Figure 1. It consists of a bidirectional AC switch, a fault current limiting inductor $L_M$ and a voltage limiting element (e.g. metal oxide varistor (MOV)). The principle of series switch-type FCL operation has been verified by experiments and simulations (Ueda, 1993). The field experience confirms that power switches are the most vulnerable components. Moreover, magnetic components and MOVs are much more reliable (Chan & Calleja, 2009; Khosroshahi, Abapour, & Sabahi, 2015; Song & Wang, 2013). Therefore, only power switches are considered in component-level redundancy. Note that it is assumed the SSFCL is non-repairable, capable to short/open circuit detection, isolation and reconfiguration (DIR). Also, it is assumed that the bidirectional switch is a pair of anti-parallel switches. To observe abridgement in subsequent text, switch will be used instead of bidirectional switch. In the following, the state space diagrams and mean time to failure (MTTFs) for four possible redundant configurations in component level are explained that can provide a useful starting point.

2.1. **SSFCL with shunt redundant switch (parallel from a reliability point of view)**

In this configuration, main and redundant switches are paralleled and each switch is in series with a low-frequency electromechanical relay. Both relays are normally closed and in case of fault detection in each switch, respective relay will be open. In this case, the requirement for system failure is that both switches fail, so switches are connected in parallel from a reliability point of view. This configuration is shown in Figure 2(a). In this case, each switch carries half of the load current. After fault occurrence, the DIR controller opens the corresponding relay and total current will be carried by intact switch and this leads to differences in failure rates before and after the fault. Therefore, we will use the subscript ‘H’ for failure rate before the fault. Figure 2(b) shows the state space diagram of this configuration. The system has seven performance states and each status is shown by a rectangle. The failure rates corresponding to a transition from state i to state j are shown by the corresponding arrows. For example, failure rate corresponding to a transition from state 1 to state 3 is equal to multiplication of short-circuit rate of, one of two switches in half-load $2\lambda_{S,C,H}$ and perfect relaying probability $P_S$. If the relay cannot open, FCL is short-circuited. So the failure rate corresponding to a transition from state 1 to state 4 is equal to multiplication of short-circuit rate of one of two switches in half-load $2\lambda_{S,C,H}$ and relay failure probability $(1 - P_S)$. Now, using state space diagram, we can form stochastic transitional probability matrix $P$. $P$ is an n-by-n square matrix for an n-state system. Where $P_{ij}$ (i $\neq$ j) is transition probability from state i to state j. Since the summation of the probabilities in each row of the $P$ is equal to 1, $P_{ii}$ is $(1 - \sum P_{ij})$. The stochastic transitional probability matrix for this case is as follows:
Then, by defining the absorbing states as a state which leads to system failure, truncated probability matrix, $Q$, is formed based on $P$ and by deleting the rows and columns associated with the absorbing states (for further information, refer Aven & Jensen, 2013; Birolini, 2013; Rausand & Høyland, 2004). According to the state space diagram in this configuration, states 4–7 are absorbing states which, once entered, cannot be left until the process starts again. So the truncated matrix $Q$ is given by

$$
P = \begin{bmatrix}
1 - 2(\lambda_{O.C,H} + \lambda_{S.C,H}) & 2\lambda_{O.C,H} & 2\lambda_{S.C,H} & 2(1 - P_S)\lambda_{S.C,H} & 0 & 0 & 0 \\
0 & 1 - (\lambda_{OC} + \lambda_{SC}) & 0 & 0 & \lambda_{OC} & \lambda_{SC} & 0 \\
0 & 0 & 1 - (\lambda_{OC} + \lambda_{SC}) & 0 & 0 & \lambda_{OC} & \lambda_{SC} \\
0 & 0 & 0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1
\end{bmatrix}
$$

(1)
According to Equations (3) and (4), truncated matrix can be used to calculate the average time which is expected to last in operation, (i.e. MTTF), where $M$ and $I$ are the fundamental matrix and unit matrix, respectively.

$$M = [I - Q]^{-1}_{3 	imes 3}$$

If the system starts in state $i$, the MTTF of the system is sum of the values in $i$th row of fundamental matrix, $M$. So, with assumption that the system starts in state 1, the MTTF is

$$MTTF_{SH} = \sum_{i=1}^{3} m_{1,i} \frac{\lambda_{OC} + \lambda_{SC} + 2(\lambda_{OC,H} + P_{S}\lambda_{SC,H})}{2(\lambda_{OC} + \lambda_{SC})(\lambda_{OC,H} + \lambda_{SC,H})}$$

2.2. SSFCL with shunt redundant switch (standby from a reliability point of view)

In this configuration, switches and relays are connected similar to the previous case, but corresponding relay to the main switch and corresponding relay to the redundant switch will be normally closed and normally open, respectively. In this case, redundant switch will enter to circuit after fault occurrence in main switch, so switches are connected in standby from a reliability point of view that leads each of switches to carry full load current. After fault detection, corresponding relay to the main switch is open and corresponding relay to the redundant switch is closed to isolate fault and reconfiguration. At first sight, it may be thought that this configuration is more reliable than the previous configuration, but in the following, we will see that this statement is not always true.

Figure 3 shows the configuration of the SSFCL with shunt redundant switch (standby from a reliability point of view) and corresponding state space diagram. Using state space diagram and procedure outlined in the section 2.1, MTTF in this case is calculated as follows:

$$MTTF_{SH,SB} = \frac{\lambda_{OC} + \lambda_{SC} + P_{S}\lambda_{OC} + P_{S}^{2}\lambda_{SC}}{(\lambda_{OC} + \lambda_{SC})^{2}}$$

2.3. SSFCL with series redundant switch (parallel from a reliability point of view)

In this configuration, main and redundant switches are in series together and each switch is paralleled with a relay. Both relays are normally open and after fault detection in each switch, respective relay will be short circuit. This configuration is parallel from a reliability point of view. As noted earlier, the bidirectional switch is a pair of anti-parallel switches. In each of these switches, the applied voltage is much less than rated voltage (applied voltage/rated voltage < 0.3), so according to Department of Defense Tech. Rep. (1991), the voltage stress factor will always be the lowest value. On the other hand, regardless of how many switches are in the circuit, each of switches carries full load current; therefore in this configuration, there is no difference between failure rates before and after the first fault. Also from the beginning, both switches are in the circuit.

Figure 4 shows the configuration of the SSFCL with series redundant switch (parallel from a reliability point of view) and corresponding state space diagram. The MTTF of this configuration is calculated as follows:

$$MTTF_{SP} = \frac{\lambda_{OC} + \lambda_{SC} + 2\lambda_{SC} + 2P_{S}\lambda_{OC}}{2(\lambda_{OC} + \lambda_{SC})^{2}}$$
2.4. **SSFCL with series redundant switch (standby from a reliability point of view)**

In this configuration, main and redundant switches are in series; corresponding relay to the main switch and corresponding relay to the redundant switch will be normally open and normally closed, respectively. In this case, redundant switch will enter to circuit after fault occurrence in main switch, so switches are connected in standby from a reliability point of view. This configuration is like second configuration with difference that this time redundant switch enters to circuit that is in series with main switch circuit. So, if the probability of fault coverage, \( P_S \) is 1, expected MTTFs of these configurations are same as together. The main role of relays in this configuration is open circuit fault isolation. This means that if a short circuit occurs in each switch, its corresponding relay does not operate, while the main role of relays in second configuration is short circuit fault isolation. Since short circuit faults impose the most power switches faults, and if the probability of fault coverage, \( P_S \) is less than 1, this configuration is more reliable than the second configuration.

On the other hand, if a short circuit fault occurs in main switch to isolate this fault in the second configuration, corresponding relay to the main switch and corresponding relay to the redundant switch must be open and closed, respectively. But in this configuration, only corresponding relay to the redundant switch is opened. The failure rate of the relay contacts is composed of two failure modes: the failure in closing the contacts and the failure in opening the contacts. The contribution of the failure in closing the contacts is often assumed to be some 50 times greater than the contribution of the failure in opening the contacts (Boyce, 2010). Again this configuration is more reliable than the second configuration.

![Figure 3. Configuration and state space diagram of the SSFCL with shunt redundant switch (standby from a reliability point of view). (a) Configuration. (b) State space diagram.](image)
Figure 5 shows the configuration of the SSFCL with series redundant switch (standby from a reliability point of view) and corresponding state space diagram. The MTTF of this configuration is calculated as follows:

\[
MTTF_{SSB} = \frac{\lambda_{O.C} + \lambda_{S.C} + P_s^2 \lambda_{O.C} + P_s \lambda_{S.C}}{(P_s^2 \lambda_{O.C} + \lambda_{S.C})(\lambda_{O.C} + \lambda_{S.C})}
\]  

(7)

3. Reliability comparison of different SSFCL redundant topologies in perfect fault coverage

Since relays are mission-oriented components in FCL (not continuously operated components), the information that is given in the empirical-based data sources is not suitable for relays. So in this article, fault coverage (fault detection, isolation and reconfiguration) probability \((P_s)\) has been employed. To compare different topologies in this article, both different operation scenarios (perfect fault coverage and imperfect fault coverage) are considered. In this section, a comparative reliability study is carried out to determine the more reliable configuration in perfect fault coverage. So, the probability of fault coverage is assumed unity. Also, sum of open circuit rate and short circuit rate is defined as failure rate \((i.e. \lambda_{O.C} + \lambda_{S.C} = \lambda_{SW})\), which is equal to twice as the failure rate of a unidirectional switch \((\lambda_{SW} = 2\lambda_s)\). Considering these assumptions, the MTTFs equations can be rewritten as follows:
Comparing Equations (8)–(10), it is clear that the series redundant configuration with parallel operation from a reliability point of view has the lowest MTTF. Also it can be seen that standby topologies from a reliability point of view have the same MTTF. Now we compare the shunt redundant configuration (parallel from a reliability point of view) with standby configurations from a reliability point of view. To do this, the following inequality is used. MTTFs of these configurations as a function of switch failure rate in full load and half load are compared in Figure 6.

\[
MTTF_{SH,P} = \frac{\lambda_{SW} + 2\lambda_{SW,H}}{2\lambda_{SW}\lambda_{SW,H}} \quad (8)
\]

\[
MTTF_{SH,SB} = MTTF_{S,SB} = \frac{2}{\lambda_{SW}} \quad (9)
\]

\[
MTTF_{S,P} = \frac{3}{2\lambda_{SW}} \quad (10)
\]

According to the MIL-HDBK-217 Department of defense Tech. Rep (1991), as major reference of failure rate calculation, the general form of failure rate of power semiconductor switch
(unidirectional switch) is calculated using Equation (14), other parameters of Equation (14) are same for all configurations except \( \pi_T \). The general form of \( \pi_T \) is as per Equation (15):

\[
\lambda_S = \lambda_b \pi_T \prod_{j} \pi_i
\]  

(14) \[
\pi_T = e^{-\frac{T_j + 273}{C_0}}
\]  

(15) 

From Equations (13)–(15), the following equations can be obtained:

\[
\frac{\pi_T}{\pi_{T,H}} > 2
\]  

(16) 

\[
\frac{1}{T_{j,H} + 273} - \frac{1}{T_j + 273} > \frac{\ln(2)}{a}
\]  

(17) 

\[
T_j > \left( 1 + \frac{\ln(2)}{a} \right) \frac{T_{j,H} + \frac{\ln(2)}{a} 273^2}{-\frac{\ln(2)}{a} T_{j,H} + \left( 1 - \frac{\ln(2)}{a} 273 \right)}
\]  

(18) 

Regardless of the term \( (\ln(2)T_{j,H}/a) \), the condition in which the shunt redundant configuration with parallel operation from a reliability point of view is more reliable can be derived as follows:

\[
T_j > \frac{(a + 273 \ln(2))T_{j,H} + \ln(2) 273^2}{a - 273 \ln(2)} = C_1 T_{j,H} + C_2
\]  

(19) 

With the assumption that the bidirectional switch is composed of a pair of thyristors, \( a, C_1, C_2 \) coefficients in Equation (19) are 3082, 1.1308 and 17.8582, respectively. Boundary condition, in which both shunt redundant configuration (parallel from a reliability point of view) and redundant configuration with standby operation from a reliability point of view have the same MTTF, is shown in Figure 7, in which regions (a) and (b) are regions in which the shunt redundant switch (parallel from a reliability point of view) configuration and redundant switch (standby from a reliability point of view) configuration are more reliable, respectively.
4. Reliability comparison between different SSFCL redundant topologies in imperfect fault coverage

In this scenario, it is assumed that the fault coverage (fault detection, isolation and reconfiguration) is imperfect \((P_S \neq 1)\). As mentioned in Section 2, in this case, the series redundant configuration (standby from a reliability point of view) has a higher MTTF than the shunt redundant configuration (standby from a reliability point of view). So in this section, series redundant configuration (standby from a reliability point of view) and shunt redundant configuration (parallel from a reliability point of view) are compared. Probabilities in different cases must be segregated. Also, the percentages of the different failure modes should be specified. If we assume that \(\chi\%\) of the faults are short circuit, we can write the following equations:

\[
\lambda_{SC} = \chi \lambda_{SW} \tag{20}
\]

\[
\lambda_{OC} = (1 - \chi) \lambda_{SW} \tag{21}
\]

Considering this assumption, the MTTFs equations can be rewritten as follows:

\[
MTTF_{SH,P} = \frac{\lambda_{SW} + [2 + 2\chi(P_{SH,P} - 1)]\lambda_{SW,H}}{2\lambda_{SW} \lambda_{SW,H}} \tag{22}
\]

\[
MTTF_{SSB} = \frac{1 + P_{SSB}^2 + (P_{SSB} - P_{SSB}^2)\chi}{\lambda_{SW}[P_{SSB}^2 + (1 - P_{SSB}^2)\chi]} \tag{23}
\]

Using these equations, the condition in which the shunt redundant configuration with parallel operation from a reliability point of view is more reliable can be derived as follows:

\[
\frac{\lambda_{SW,H}}{\lambda_{SW}} < \frac{0.5[\chi + (1 - \chi)P_{SSB}^2]}{1 - \chi + \chi^2 + \chi P_{SSB} - \chi^2 P_{SH,P} + (\chi - \chi^2)P_{SSB}(1 - P_{SH,P})} \tag{24}
\]

The last term in the denominator of Equation (24), i.e. \((\chi - \chi^2)P_{SSB}^2(1 - P_{SH,P})\) can be safely neglected.
where $\gamma$ is defined as the ratio of the perfect relaying probability in shunt redundant configuration to perfect relaying probability in series redundant configuration which can have a value between 0 and 1 and is usually close to 1. Also, according to Smith (2011), the percentage of the short circuit failure, $\chi$ is 0.98 for thyristor. Thus, following equations can be deduced:

$$P_{SB} = \gamma P_{SH}$$

(26)

On other hand, according to the MIL-HDBK-217, failure rate ratio based on temperature factor ratio is calculated as follows:

$$\frac{\lambda_{SW,H}}{\lambda_{SW}} = \frac{\pi_{TH}}{\pi_T} = e^{\frac{a}{T_j - 273}}$$

(27)

Now, in comparison with Equations (27) and (28), we can identify the appropriate redundant configuration. In Figure 8, Equations (27) and (28) have been cut and appropriate regions for shunt redundant configuration (parallel from a reliability point of view) and series redundant configuration (standby from a reliability point of view) are determined.

5. Sensitivities of more reliable configuration to different parameters

In this section, sensitivities of more reliable configuration to ambient temperature, power losses and thermal resistance of heat sink are analysed. As seen in Section 4, predicted lifetime of each configuration is a function of junction temperature of switches. Also, more reliable configuration has been determined by junction temperature range, therefore junction temperature is one of the principal parameters and a common input parameter of the reliability calculation. The used thermal model for power switch is shown in Figure 9(a), in which the thermal impedance between the junction and case is usually modelled as a multi-layer foster RC network in the manufacturer datasheets (see Figure 9(b)). Regardless of the thermal capacitance $C_{th}$, which describes dynamic changes, the junction temperature based on the thermal equivalent model of Figure 9(a) is calculated as follows:

$$T_j = T_a + P_{loss}(R_{th,jc} + R_{th,Ja})$$

(29)

Usually sum of thermal resistance between the case-heat sink and thermal resistance between the heat sink-ambient is considered as the thermal resistance of heat sink.

$$R_{th,Ja} = R_{th,CH} + R_{th,Ha}$$

(30)

From Equations (19), (29) and (30), region in which the shunt redundant configuration with parallel operation from a reliability point of view, is more reliable can be derived as:

$$P_{loss} - C_1P_{loss,H} > \frac{(C_1 - 1)T_a + C_2}{R_{th,jc} + R_{th,Ja}}$$

(31)

Since the ambient temperature coefficient is positive in Equation (31), increasing the ambient temperature increases the right side of (31), and consequently, Equation (31) is more likely to be satisfied. Also, by increasing the rated power level, $(P_{loss} - C_1P_{loss,H})$ – the left term – increases as well. Therefore, increasing the rated power level leads the above inequality more likely to be satisfied. In other words, the shunt redundant configuration with parallel operation from a reliability point of view is more appropriate for the systems with high power and low ambient temperature applications. However, for an application
with specified ambient temperature and rated power level, thermal resistance of heat sink is the main parameter to determine the more reliable configuration.

Figure 9(c) compares MTTFs of two candidate topologies (i.e. shunt redundant configuration with parallel operation from a reliability point of view and series redundant configuration with standby operation from a reliability point of view) as a function of failure rate of switch in full load and half load.

6. Experimental results

To have a better understanding of Equations (19), and (31), a case study has been performed in this section. To do this, a low-power SSFCL with shunt redundant configuration (parallel from a reliability point of view) has been developed. Since in the standby operation, only one switch is in the circuit, the purpose of this section is to calculate power losses and junction temperature of switches. Thus, instead of series redundant configuration, we use a SSFCL without redundant component. Figure 10(a) shows the experimental set-up of the SSFCL with shunt redundant configuration (parallel from a reliability point of view) which is able to lead out redundant switch. The circuit and SSFCL parameters can be found in Table A1 in the Appendix.

Figure 10 shows thermal image of two mentioned topologies in steady-state conditions which, instead of the inaccessible junction temperatures, represents case temperatures of the individual switches. The case temperature of thyristors in each topology is given in the images (i.e. 44.46°C and 104.46°C for shunt redundant configuration and without redundant configuration, respectively). According to Figure 10 and Equation (29), the junction temperatures of switches in shunt redundant configuration and without redundant configuration are 44.90°C and 106.20°C, respectively. Also according to the procedures specified in the Appendix, the power loss of thyristors is calculated. The power losses of each thyristor in shunt redundant configuration and without redundant configuration are 0.335 and 1.34 W, respectively. Based on obtained values for junction temperature and power losses, Equations (19) and (31) are satisfied. So, shunt redundant configuration (parallel from a reliability point of view) is more reliable for SSFCL with the given properties.

Figure 8. Failure rate of SSFCL at half load to full load ratio. (a) Region in which the shunt redundant configuration (parallel from a reliability point of view) is more reliable. (b) Region in which the series redundant configuration (standby from a reliability point of view) is more reliable.
7. Cost analysis

The MTTF of non-redundant FCL is achieved simply by reversing the failure rate of two switches. In general, this equation can be expressed in the form of

\[
MTTF_{\text{non-red}} = \frac{1}{\lambda_{SW}} = \frac{1}{2\lambda_S}
\]  

(32)

According to Equations (8)–(10), compared to non-redundant FCL, a potential benefit brought by the redundant FCL is the possibility of achieving high reliability. So, compared to non-redundant FCL, cost of outage, regarding the customer interruption cost, is lower for redundant FCL.
Nevertheless, redundant design means the need for more components. So, the investment cost of the redundant FCL is higher than non-redundant FCL. To find the configuration with the lowest cost per million hours, a levelised indicator for each structure with respect to the structure total cost is considered. The levelised cost (LC) of the redundant and non-redundant structures determines the net cost of FCL for expected lifetime divided by its expected lifetime. Consequently, it can be a good measure to compare the economic justification of the redundant and non-redundant structures. The LC of a structure can be expressed as follows:

\[
LC = \frac{C_{\text{tot}}}{MTBF} = \frac{C_{\text{inst}} + C_{\text{loss}} + C_{\text{repair}} + C_{\text{outage}}}{MTTF + MTTR}
\]  

(33)

where \(C_{\text{tot}}\), \(C_{\text{inst}}\), \(C_{\text{loss}}\), \(C_{\text{repair}}\), \(C_{\text{outage}}\), MTBF and MTTR are the net cost of FCL for expected lifetime, investment cost, loss cost, repair cost, outage cost, mean time between failures and mean time to repair, respectively. The investment cost includes the installation cost that is proportional to the rating of the FCL. The investment cost of an \(I^{KA}\) FCL with \(X\) redundant switches is

\[
C_{\text{inst}} = X \times C_0 \times I
\]

(34)

where \(C_0\) is the cost of FCL per ampere. According to the survey of energy information administration (U.S. Energy Information Administration, 2015), power loss cost \(C_{lo}\) is assumed to be 12 $/kWh. Therefore, the power loss cost for expected lifetime of FCL is derived as

\[
C_{\text{loss}} = P_{\text{loss,x}} \times MTTF \times C_{\text{lo}}
\]

(35)
Repair cost consists of the cost of reinstallation, labour and transportation of the technical support staff. The labour transportation cost per failure $C_{LT}$ is estimated to be $300 \$/kA/day (Canada, Moore, Strachan, & Post, 2003). The repair cost is as follows:

$$C_{repair} = C_{inst} + (C_{LT} \times MTTR)$$ (36)

Finally, the outage cost is the total revenue loss from customers because of their inability to access network during the outage period. This cost is significantly higher than electricity prices and related to the system scale. The outage cost per day $C_{d0}$ for a 50-A system is around $1200 \$/day (Berkeley National Laboratory, 2003). The total outage cost within expected lifetime of FCL is calculated as follows:

$$C_{outage} = C_{d0} \times MTTR$$ (37)

In this article, the field data, MTTR and price coefficients, which are listed in Table A1, come from the following sources: the military handbook (Department of defense Tech. Rep, 1991) and the provided field data in Begovic, Pregelj, and Rohatgj (2000), Berkeley National Laboratory (2003), Canada et al. (2003), Taylor, Hanson, Lubkeman, & Treichel (2005) and U.S. Energy Information Administration (EIA) (2015). Here, we consider the previous cases in reliability analysis as an example. The power losses of each thyristor in shunt redundant configuration and without redundant configuration are 0.34 and 1.35 W, respectively. The results of LC calculation under different cases of redundancy are shown in Table 1. As indicated in Table 1, the LC is minimised for shunt redundant configuration (parallel from a reliability point of view). Therefore, shunt redundant configuration (parallel from a reliability point of view) not only improves the reliability level but also reduces the LC of system.

The LC can be easily influenced by data set. So, it should be noted that the objective of this section was not to judge the economic merits of one configuration over another, but rather to present a method of applying a usage model for comparing different configurations.

### 8. Conclusion

A comprehensive reliability analysis between the four possible configurations for the redundant design in component level (i.e. shunt or series redundant switch with parallel or standby operation from a reliability point of view) is carried out. Proposed analysis provides valuable information to enhance system reliability, to choose better redundant system configuration and to realise maximum benefit of redundant design.

It is shown that the more reliable configuration is determined by junction temperature of switches. Junction temperature range is formulated in which the SSFCL with shunt redundant configuration (parallel from a reliability point of view) is more reliable. If junction temperature was not in the mentioned range, the SSFCL with series redundant configuration (standby from a reliability point of view) is more reliable. Also, this comparison shows that the SSFCL with series redundant configuration (parallel from a reliability point of view) has the lowest reliability. Sensitivities of more reliable configuration to ambient temperature, power losses and the thermal resistance of heat sink are analysed. Thermal resistance of heat sinks is regulated to ensure that shunt redundant configuration with parallel operation from a reliability point of view is more

| Configuration                                      | Levelised costs ($/million hours) |
|---------------------------------------------------|----------------------------------|
| Non-redundant                                     | 25,578.06                        |
| Shunt redundant (parallel from a reliability point of view) | 3861.39                          |
| Shunt redundant (standby from a reliability point of view) | 6662.11                          |
| Series redundant (parallel from a reliability point of view) | 8936.58                          |
| Series redundant (standby from a reliability point of view) | 6662.11                          |
reliable. Also, the optimal configuration was found economically. In addition, to calculate the junction temperature, switches loss calculation are investigated in the Appendix.

Finally, further research may investigate the redundant design in other levels (i.e. leg-level, module-level and system-level). It is under research to identify the more reliable configuration.

**Disclosure statement**

No potential conflict of interest was reported by the authors.

**ORCID**

Behnam Mohammadi-Ivatloo [http://orcid.org/0000-0002-0255-8353]

**References**

Abramovitz, A., & Smedley, K. M. (2012). Survey of solid-state fault current limiters. *IEEE Transactions on Power Electronics*, 27(6), 2770–2782.

Aghdam, F., & Abapour, M. (2016). Reliability and cost analysis of multistage boost converters connected to PV panels. *IEEE Journal of Photovoltaics*, 6(4), 981–989.

Arifujaman, M., & Liuchen, C. (2012). *Reliability comparison of power electronic converters used in grid-connected wind energy conversion system*. 2012 3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), pp. 323–329. IEEE. doi:10.1109/PEDG.2012.6254021

Aven, T., & Jensen, U. (2013). *Stochastic models in reliability*. London: Springer Verlag.

Begovic, M., Pregelj, A., & Rohatgj, A. (2000). *Four-year performance assessment of the 342 kW PV system at Georgia Tech*. Proc. IEEE PVSC, pp. 1575–1578. doi:10.1109/PVSC.2000.916198

Berkeley National Laboratory. (2003). A framework and review of customer outage costs. Retrieved from [http://emp.lbl.gov/sites/all/files/REPORT%20lbnl%20-%20%2054365.pdf](http://emp.lbl.gov/sites/all/files/REPORT%20lbnl%20-%20%2054365.pdf)

Birolini, A. (2013). *Reliability engineering: Theory and practice*. New York, NY: Springer Verlag.

Bortis, D., Beila, J., & Kolar, J. (2007). Active gate control for current balancing in paralleled IGBT modules in a solid state modulator. Proc. IEEE Int. Conf. Plasma Sci. doi:10.1109/PSSP.2007.4346097

Boyes, W. (2010). *Instrumentation reference book* (4th ed., pp. 737–787). Boston, MA: Butterworth Heinemann.

Canada, S., Moore, L., Strachan, J., & Post, H. (2003, October). *Off-grid hybrid systems: Maintenance costs*. Solar Energy Technol. Syst. Symp, Montreal.

Caroline, D., Vincent, L., & Guy, F. (2007). Inverter topology comparison for remedial solution in transistor faulty case. 2007 European Conference on Power Electronics and Applications, pp. 1–8. doi:10.1109/EPE.2007.4417248

Chan, F., & Calleja, H. (2009). Design strategy to optimize the reliability of grid-connected PV systems. *IEEE Transactions on Industrial Electronics*, 56(11), 4546–4572.

Chen, A., Zhang, C., He, X., & Cui, N. (2009, May). Fault-tolerant design for flying capacitor multilevel inverters. *Proc. IEEE 6th Int. Power Electron. Motion Control Conf.*, pp. 1460–1464. doi:10.1109/IPEMC.2009.5157616

Cho, H. K., Kwak, S. S., & Lee, S. H. (2015). Fault diagnosis algorithm based on switching function for boost converters. *International Journal of Electronics*, 102(7), 1229–1243.

Department of defense Tech. Rep. (1991). *Reliability prediction of electronic equipment*. U.S. Lockheed Martin.

Farhadi, M., Abapour, M., & Sabahi, M. (2016). Failure analysis and reliability evaluation of modulation techniques for neutral point clamped inverters—A usage model approach. *Engineering Failure Analysis*, 71, 90–104.

Farhadi, M., Tahmasbi-Fard, M., Abapour, M., & Tarafdar-Hagh, M. (2017, March). DC-AC converter-fed induction motor drive with fault-tolerant capability under open-and short-circuit switch failures. *IEEE Transactions on Power Electronics*. doi:10.1109/TPEL.2017.2683534

Fischbach, R. E. (1958). Designing for reliability in electronic instrumentation. *Journal of Electronics and Control*, 5(5), 471–482.

Flannery, P., & Venkataramanan, G. (2008). A fault tolerant doubly fed induction generator wind turbine using a parallel grid side rectifier and series grid side converter. *IEEE Transactions on Power Electronics*, 23(3), 1126–1135.

Fotuhi-Firuzabadi, M., Aminifar, F., & Rahmati, I. (2012). Reliability study of HV substations equipped with the fault current limiter. *IEEE Transactions on Power Delivery*, 27(2), 610–617.

Gibbs, I., & Kimmel, D. (2001). Active current balance between parallel thyristors in multi-bridge AC–DC rectifiers. *IEEE Transactions on Energy Conversion*, 16(4), 334–339.

Harb, S., & Balog, R. (2013). Reliability of candidate photovoltaic module-integrated-inverter (PV-MII) topologies—A usage model approach. *IEEE Transactions on Power Electronics*, 28(6), 3019–3027.
Jamshidpour, E., Poure, P., & Saadate, S. (2016). Switch failure diagnosis based on inductor current observation for boost converters. *International Journal of Electronics*. doi:10.1080/00207217.2016.1138243

Kazemia, S., & Lehtonenb, M. (2013). Impact of smart subtransmission level fault current mitigation solutions on service reliability. *Electric Power Systems Research*, 96, 9–15.

Khosroshahi, A., Abapour, M., & Sabahi, M. (2015). Reliability evaluation of conventional and interleaved DC-DC boost converters. *IEEE Transactions on Power Electronics*, 30(10), 5821–5828.

Kim, S. Y., & Kim, J. O. (2011). Reliability evaluation of distribution network with DG considering the reliability of protective devices affected by SFCL. *IEEE Transactions on Applied Superconductivity*, 21(3), 3561–3569.

Kou, X., Corzine, K. A., & Familiant, Y. L. (2004). A unique fault-tolerant design for flying capacitor multilevel inverter. *IEEE Transactions on Power Electronics*, 19(4), 979–987.

Lezana, P., & Ortiz, G. (2009). Extended operation of cascade multicell converters under fault condition. *IEEE IEEE Transactions on Industrial Electronics*, 56(7), 2697–2703.

Maharjan, L., Yamagishi, T., Akagi, H., & Asakura, J. (2010). Fault-tolerant operation of a battery-energy-storage system based on a multilevel cascade PWM converter with star configuration’. *IEEE Transactions on Power Electronics*, 25(9), 2386–2396.

Musumeci, S., Pagano, R., Frisina, A., & Melito, M. (2002). *Parallel strings of IGBTs in short circuits: Analysis of the parameter influence and experimental behavior*. Proc. 28th IEEE Annu. IECON, pp. 555–560. doi:10.1109/IECON.2002.1187568

Rausand, M., & Høyland, A. (2004). *System reliability theory*. Hoboken, NJ: Wiley.

Richardau, F., & Pham, T. T. L. (2013). Reliability calculation of multilevel converters: Theory and applications. *IEEE Transactions on Industrial Electronics*, 60(10), 4225–4233.

Smith, D. J. (2011). *Reliability, maintainability, and risk* (2nd ed., pp. 391–393). London: Butterworth Heinemann.

Son, G. T., Lee, H.-J., Nam, T. S., Chung, Y.-H., Lee, U.-H., Baek, S.-T., … Park, J.-W. (2012). Design and control of a modular multilevel HVDC converter with redundant power modules for non-interruptible energy transfer. *IEEE Transactions on Power Delivery*, 27(3), 1611–1619.

Song, Y., & Wang, B. (2013). Survey on reliability of power electronic systems. *IEEE Transactions on Power Electronics*, 28(1), 591–604.

Song-Manguelle, J., Thurnherr, T., Schroder, S., Rufer, A. & Nyobe-Yome, J. (2010). Re-generative asymmetrical multi-level converter for multimegawatt variable speed drives. *Proc. IEEE Energy Conversion Cong. Expo.*, pp. 3683–3690. doi:10.1109/ECCE.2010.5618343

Taylor, T., Hanson, A., Lubkeman, D., & Treichel, K. (2005). *Fault current review study* (pp. 41–45). Raleigh, NC: ABB Inc. Electric Systems Consulting.

U.S. Energy Information Administration (EIA). (2015). http://www.eia.gov/electricity/monthly/

Ueda, T. (1993). Solid-state current limiter for power distribution system. *IEEE Transactions on Power Delivery*, 8(4), 1796–1801.

Valipour, H., Fotuhi-Firouzabad, M., Rezazadeh, G., & Zolghadri, M. R. (2015). Reliability comparison of two industrial AC/DC converters with resonant and non-resonant topologies. *The 6th Power Electronics, Drive Systems & Technologies Conference (PEDSTC2015)*, pp. 430–435. doi:10.1109/PEDSTC.2015.7093313

Zhang, W., Xu, D., Enjeti, P. N., Li, H., Hawke, J. T., & Krishnamoorthy, H. S. (2014). Survey on fault-tolerant techniques for power electronic converters. *IEEE Transactions on Power Electronics*, 29(12), 6319–6331.
Appendix

Power loss analysis

Power dissipation of a semiconductor switch consists of two parts: conduction loss and switching loss. Switching loss is composed of power losses during turn-on and turn-off switching transitions and the conduction losses are the power losses caused by the switch on-state resistance and forward voltage drop. So, the power loss can be derived as follows:

\[
P_{\text{loss}} = P_{\text{SW}} + P_{\text{Cond}} = f_{\text{SW}}(E_{\text{ON}} + E_{\text{OFF}}) + \frac{1}{T} \int_{0}^{T} E_{\text{Cond}} \, dt \tag{38}
\]

\[
E_{\text{Cond}} = (V_0 + R_{SI}(t))i(t)T_s \tag{39}
\]

Table A1. SSFCL and system parameters.

| Symbol | Quantity                                      | Value              |
|--------|-----------------------------------------------|--------------------|
| \(L_M\) | Inductance of fault current limiting inductor | 0.02 H             |
| -      | Power switch type                             | BT151              |
| \(R_{th,jC}\) | Thermal resistance between the junction and case | 1.3°C/W          |
| \(R_{th,CA}\) | Thermal resistance between case and ambient (in free air) | 58.7°C/W            |
| \(V_S\) | Secondary side voltage of isolation transformer | 63 V               |
| \(\omega\) | Grid angular frequency                       | 2\pi \times 50 rad/S |
| \(P_L\) | Power of the downstream load                 | 200 W              |
| \(T_a\) | Ambient temperature                           | 25°C               |
| \(MTTR\) | Mean time to repair (Birolini, 2013)          | 24 days            |
| \(C_0\) | Cost of FCL per capacity (Aven & Jensen, 2013) | 710 $/KA          |