A Proof-of-Concept 70 nA ECG Processor for Real-Time R-Wave and NN50 Detection

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Abstract. Unobtrusive health monitoring applications necessitate accurate, real-time, and energy-efficient computation of health-related parameters. Two important parameters for cardiovascular and cardiac autonomic health assessment are heart rate (HR) and heart rate variability (HRV). In this paper, an energy-efficient mixed-signal processor ASIC for real-time monitoring of HR and NN50, a well-established HRV score for parasympathetic activity assessment, is presented. The proposed ASIC, designed in a 0.5 μm CMOS technology, detects R-waves of ECG signals and compares successive R-R intervals to identify the NN50 events in real-time. Post-layout simulation results using ECG signals of four recordings from the MIT-BIH arrhythmia database are compared with DSP calculations on MATLAB. Based on simulation results, the processor detects R-waves with an average accuracy of 99.1%, and NN50 events with average sensitivity and positive predictive values of 94.7% and 96.9%, respectively. The processor consumes 70 nA when supplied by ±1.6 V.

1. Importance of Heart Rate and Heart Rate Variability
Heart rate (HR) and heart rate variability (HRV) are important physiological indicators of cardiovascular and autonomic nervous system (ANS) health status [1]. Particularly, HR is correlated with cardiovascular risk factors as well as survival rate of populations with cardiovascular disorders. HRV serves as a quantitative measure on health status of the regulation mechanisms of HR, namely sympathetic and parasympathetic nervous system. HR and HRV can be determined from the timing of ECG R-waves. HR is the number of R-waves in a minute and HRV can be quantified using R-R intervals through several time-domain, frequency-domain, and/or nonlinear methods - many of which are closely correlated with each other. One of the widely-used time-domain HRV metrics is NN50, the number of successive R-R intervals differing by >50 ms. NN50 is a marker of parasympathetic activity and is useful in determining autonomic dysfunction [1]. The non-invasive nature of ECG signal and the ability to extract HR and HRV scores in real-time, make ECG an attractive and viable signal for ambulatory cardiovascular and ANS health-monitoring applications, which can facilitate a proactive approach in healthcare. Accordingly, many wearable ECG-based ubiquitous HR and HRV monitoring systems have been reported in the literature, which leverage digital processing, where the custom processors can perform R-wave detection while consuming sub-μA current (excluding A/D conversion): 410 nA in [2] and 372.5 nA in [3]. In this paper, we demonstrate a proof-of-concept digitally-assisted analog-signal-processing approach eliminating the need for an A/D. The processor consumes ~20% of the current consumption of [2-3] while providing more functionality: in addition to R-wave detection, NN50 events are also captured in real-time. In Section 2, the design and operation of the processor are detailed.
Methods for validation of the circuit are summarized in Section 3, which is followed by evaluation of post-layout simulations and discussion in Section 4. The paper is concluded in Section 5.

2. ECG Processor Design
The block diagram of the processor is shown in Figure 1(a). For energy-efficiency, core computation blocks operate in the analog domain leveraging CMOS subthreshold region. Digital blocks generate the clocks for timing of the analog blocks. A 9-transistor OTA is extensively used in several analog blocks (Figure 1(b)).

2.1. Circuit operation
The 1st time derivative of the ECG signal peaks before and after each R-wave. To detect those peak points, a hysteretic differentiator is designed (Figure 1(c)). The output of the hysteretic differentiator is converted into pulses, $ECG_R$, at a voltage comparator. The time duration between consecutive R-waves, $TR_R$, is converted into a voltage signal, $V_{RR}$, by an upper envelope detector circuitry (Figure 1 (d)). The input to the envelope detector is a delayed version of $ECG_R$, namely $ECG_{R,del}$. When $ECG_{R,del}$ is high, the NMOS controlled by the OTA output charges the load capacitor, $CL_2$, which increases the output, $V_{RR}$, to a maximum level, $V_{RR,max} = 0.85 V$, a value set by $\frac{V_{L}}{2} = 0.6V$, $CL_2 = 36 \mu F$. When $ECG_{R,del}$ is low, the NMOS controlled by a fixed bias voltage, $V_{bias,1}$, discharges the $CL_2$ with a current $IM_1$. The relationship between the minimum value of $V_{RR}$, $V_{RR,min}$, which occurs immediately before the consecutive R-wave, and $TR_R$ is $V_{RR,min} = V_{RR,max} - IM_1TR_R/CL_2$. To a first order approximation, the $V_{RR}$ dependence of $IM_1$ can be neglected for a sufficiently small $V_{RR}$ variation, and thus resulting in a linear dependence between $V_{RR,min}$ and $TR_R$. To compare the absolute time difference between two successive R-R intervals, namely $|TR_{R1}-TR_{R2}|$, and 50 ms in real-time, a sample-and-hold (S/H) circuitry samples the value of $V_{RR}$ during $TR_{R1}$ period and holds it during the R-R interval that follows $TR_{R2}$ to create $V_{RR1}$. Another S/H circuitry operates in a complementary manner to sample $V_{RR}$ during $TR_{R2}$ period and hold it during $TR_{R1}$ period to create $V_{RR2}$. The difference between $V_{RR1}$ and $V_{RR2}$ is proportional to $|TR_{R1}-TR_{R2}|$ and calculated as an OTA output current, $I_{diff}$ in Figure 1(e). An absolute value circuit, which is implemented as a Class-B stage fed by the output of an inverter with a small gain and a pair of source current-mirrors and a sink current- mirror, outputs a current $|I_{diff}|$ (Figure 1(e)). A winner-take-all circuit (WTA) compares $|I_{diff}|$ with a threshold current $I_{th} = 12.1 nA$ corresponding to an R-R interval of 50 ms. A NAND gate converts the output of the WTA into digital pulses, $NN50i$, which is ‘0’ only if WTA output is low during an evaluation period (i.e., $P_{eval} = ‘0’$) (Figure 1(f)). Digital circuitry generates (i) $P_{eval}$ and $ECG_{R,del}$ to ensure that comparison of $|I_{diff}|$ and $I_{th}$ is completed before $V_{RR1}$ and $V_{RR2}$ starts ramping up at the onset of the arrival of the subsequent $ECG_R$ pulse; and (ii) clocks controlling the S&H timing. A bootstrap reference with a diode-connected MOS start-up and an off-chip resistor (10 MΩ) generates the bias currents.
3. Methods for validation
The processor is designed and laid out in a 0.5-μm CMOS technology with a footprint of 0.475 mm x 0.75 mm (Figure 3). In this proof-of-concept study, R-wave and NN50 event detection was demonstrated through post-layout transient simulations using 1000 s segments of four recordings (Rec. 100 to Rec. 103) from the MIT-BIH arrhythmia database [4, 5].

4. ECG processor results and discussion
For validation, simulations of R-wave and NN50 event detection were compared against DSP calculations on MATLAB. For a total of 4501 R-waves in all recordings, the average R-wave detection accuracy is 99.1%. Average sensitivity (S=TP/(TP+FN)) and positive predictive (PV+=TP/(TP+FP)) values for NN50 event detection are S=94.7% and PV+=96.9%; where TP, FN, and FP are true positive, false negative, and false positive events. The ECG processor outputs of NN50 events and DSP calculations are presented in Figure 4. The total current consumption of the system excluding the bias circuitry is 69.87 nA.

5. Conclusion
In this paper, an energy-efficient and real-time ECG processor is proposed. The mixed-signal ASIC processor generates pulses timestamping the R-waves and events of NN50, which is a heart-rate-variability score. Based on post-layout simulations, the processor achieves 99.1% R-wave detection accuracy and 96.9% positive predictive value while consuming low current (70 nA) and area (~0.36 mm²). Results suggest the potential of digitally-assisted analog-processing in achieving more functionality with less power consumption than digital ECG processing solutions of the state-of-the-art wearables.

References
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