Implementing High-Order FIR Filters in FPGAs

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Abstract—Contemporary field-programmable gate arrays (FPGAs) are predestined for the application of finite impulse response (FIR) filters. Their embedded digital signal processing (DSP) blocks for multiply-accumulate operations enable efficient fixed-point computations, in cases where the filter structure is accurately mapped to the dedicated hardware architecture. This brief presents a generic systolic structure for high-order FIR filters, efficiently exploiting the hardware resources of an FPGA in terms of routability and timing. Although this seems to be an easily implementable task, the synthesizing tools require an adaptation of the straightforward digital filter implementation for an optimal mapping. Using the example of a symmetric FIR filter with 90 taps, we demonstrate the performance of the proposed structure with FPGAs from Xilinx and Altera. The implementation utilizes less than 1% of slice logic and runs at clock frequencies up to 526 MHz. Moreover, an enhancement of the structure ultimately provides an extended dynamic range for the quantized coefficients without the costs of additional slice logic.

Index Terms—digital filters, field-programmable gate arrays, FIR filters, fixed-point arithmetic

I. INTRODUCTION

NOWADAYS, finite impulse response (FIR) filters are a major application of field-programmable gate arrays (FPGAs) in the context of digital signal processing (DSP). An FPGA design is traditionally implemented in a hardware description language on the register-transfer level (RTL). Therefore, the design flow from the RTL top level down to the logic and circuit level postulates clear definitions and constraints for an optimal implementation result. As a consequence, the architecture of the device impacts the design, and a straight separation of the abstraction layers is practically impossible for an efficient realization in terms of logic utilization or speed. Although some approaches to hardware efficient filter structures exist [11], [2], the key to a valuable exploitation of the hardware resources is an adaptation of the FIR filter structure to the architecture of the FPGA. Moreover, at the early stage of filter design, a reduction of hardware complexity is possible [8]. At last, an adaptation of the mathematical modelling to the dedicated silicon (DSP blocks) maximizes performance [4] while versatility decreases.

In fact, an implementation of numerical algorithms in an FPGA, including FIR filters, is a trade-off between targeted precision, allocated logic, achievable clock frequency, and allowed latency. An operation with a fixed-point arithmetic is usually preferred if resources or speed weigh more than the highest precision. Thus, state-of-the-art FPGAs have hundreds of built-in DSP blocks, capable of fixed-point operations with a precision of at least 18 bits [5], [6]. Consequently, we will adapt a symmetric FIR filter structure to a generic FPGA architecture and meet the challenges regarding routability, timing, and precision.

A. Prior work

Several convenient structures of FIR filters can be found in the literature, e.g. direct-form realization [7], transposed direct-form [8], and symmetry exploiting direct-form structures for linear-phase systems [9]. The literary work covers the basic mathematical operations and structures but bypasses the technical aspects concerning the prevalent DSP block architectures of contemporary FPGAs. Nevertheless, the major manufacturers of FPGAs support their platforms with practical explanations [10], [11], [12].

Besides the hardware-mapped structures, an improved precision of a symmetric FIR filter without increasing the coefficient bit-widths was proposed by Shen [13]. The presented parallel method implementation utilizes an accumulator in combination with variable shift operations. Although FPGAs have “flexible multidata bus routing capabilities” [13], the suggested shift of the accumulator input contradicts the architecture of state-of-the-art embedded DSP blocks (e.g. [5], [6]). As Shen omits a benchmark with an FPGA implementation, the synthesis results of the optimized structure on a Xilinx FPGA were presented by Yuan [14]. These results show a further consumption of slice logic in addition to the DSP blocks, but neglect the specific architecture of the FPGA and do not properly include the DSP blocks in their optimization.

B. Aim of this work

High-order digital filters require a cascade of sub-filters for an efficient realization [3] or, alternatively, an efficiently mapped hardware design. With regard to recent hardware architectures, a FIR filter whose length exceeds the number of cascaded DSP blocks (DSP chains) in an FPGA, can be referred to as high-order filter. This brief presents the methodology and implementation of a systolic FIR filter in an FPGA, which ideally matches the prevalent embedded DSP block architecture. Consequently, the direct implementation of large structures avoids the cascading into small filters. The challenges of such a design are discussed, exemplary solved, and compared to the key performance indicators of an FPGA implementation: logic utilization and clock frequency. Moreover, in reference to the “bit compression” introduced by Shen [13], we adapt their parallel method and implement it for an FPGA in terms of routability and timing.
an improved precision of the frequency response without additional logic utilization.

II. OPTIMIZED FIR FILTER STRUCTURE FOR FPGAS

Within the scope of high-order parallel FIR filters, it is suitable to design the filter with a linear phase. Thus, the coefficients \( h[k] \) of the FIR system of order \( M \) would satisfy the symmetry condition \( h[M - k] = h[k] \), where \( k = 0, 1, \ldots, M \) and the number \( N \) of coefficients and taps for the FIR system is \( N = M + 1 \) [9]. Consequently, the generalized equation for the output \( y \) of a symmetric FIR filter with an even number \( N \) of taps can be expressed as [9]:

\[
y[n] = \sum_{k=0}^{M-1} h[k] (x[n-k] + x[n-M+k]) .
\]

In the case of symmetric FIR filters, the number of coefficient multipliers is essentially halved [9]. Other types of symmetry, e.g. point symmetry or an odd number \( N \) of taps, are developed by an analogy with the ongoing methodology. However, the taps of the input samples \( x[n] \) are folded around half of the filter length by \( N/2 \) pre-adders, before the sums are multiplied by \( h[k] \). Finally, the products are convoluted by \( N/2 - 1 \) post-adders. Hence, a basic arithmetic logic unit for a DSP operation incorporates a pre-adder, a multiplier and a post-adder as shown in Fig. 1.

![Fig. 1. The prevalent architecture for a DSP operation in an FPGA with pre-adder (C = A + B), multiplier (E = C \times D) and post-adder (Y = E + F). The bit-widths \( W \) of the inputs and outputs depend on the FPGA architecture.](image)

Contemporary FPGA architectures embed multiply-accumulate blocks for digital filters, either by integrated hardware primitives or by synthesized logic blocks. The mapping of Eq. (1) to parallel DSP blocks according to the direct-form implementation is convenient, but results in a large adder tree for the running sum, which slows down the maximum clock frequency of the system. If the design targets a high throughput at the highest clock frequency, a systolic structure with a pipeline will maximize the performance of the FIR filter, as long as latency is negligible. The structure is described in \( z \)-domain by using the time-shifting property of the \( z \)-transformation \( x[n-k] \leftrightarrow z^{-k}X(z) \) [9] and Eq. (1) resulting in:

\[
Y = \sum_{k=0}^{M-1} h[k] (z^{-k} + z^{-M+k}) X ,
\]

where \( h_k = h[k] \). Furthermore, a pipeline is embedded into the systolic structure by adding registers to the output of each running sum element. In terms of the \( z \)-transformation, the pipeline register is a unit delay \( z^{-1} \). Therefore, the pipelining of the FIR filter can be expressed as:

\[
Y z^{-1} = z^{-1} \sum_{k=0}^{M-3} h[k] (z^{-k} + z^{-M+k}) X + z^{-1} h_{M-1} (z^{-M+2} + z^{-M-2}) X .
\]

(3)

\[
Y z^{-2} = z^{-1} \sum_{k=0}^{M-3} h[k] (z^{-k} + z^{-M+k}) X + z^{-1} h_{M-3} (z^{-M+3} + z^{-M-3}) X + z^{-2} h_{M-1} (z^{-M+2} + z^{-M-2}) X .
\]

(4)

Eq. (3) illustrates the decomposition of the last term of the running sum with a pipeline register. In addition, the second pipeline stage is formed by Eq. (4). Finally, the complete decomposition of the adder tree with \( M \) unit delays reveals the FIR filter function in terms of iteration of the basic systolic element

\[
Y_k = z^{-1} Y_{k-1} + z^{-k} h_k (z^{-k} + z^{-M+k}) X = z^{-1} Y_{k-1} + h_k (z^{-2k} + z^{-M}) X
\]

(5)

\[
Y_0 = h_0 (1 + z^{-M}) X ,
\]

(6)

where the output \( Y \) from Eq. (2) is equal to the output of the last pipeline stage at position \( k = M-1 \) from Eq. (5). The block diagram of the symmetric systolic FIR filter is shown in Fig. 2. A detailed mapping of this structure to the Xilinx specific architecture is shown in [4].

![Fig. 2. A linear phase FIR filter of order \( M \) (odd number). The filter function is folded around half of the filter length \( N \) (even number) according to Eq. (3), and the adder tree for the running sum is replaced by the systolic structure derived from Eq. (6).](image)

It is clear, that the pipeline registers at the outputs of the multiply-accumulate operations cause a delay of \( k \) clock cycles, but the derived iteration from Eq. (5) also inserts an initial pipeline delay, as the first folded sum from Eq. (5) is only valid after passing the tapped delay line with \( M \) stages. A modification of the fundamental filter function from Eq. (2) brings it to

\[
Y = \sum_{k=0}^{M-1} h_{M-1-k} (z^k + z^{-1-k}) X ,
\]

(7)

and yields an alternative iterated function

\[
Y_k = z^{-1} Y_{k-1} + h_{M-1-k} (1 + z^{-1-2k}) X
\]

(8)

\[
Y_0 = h_{M-1} (1 + z^{-1}) X ,
\]

(9)
where the initial delay is reduced to the unit delay. The corresponding block diagram is shown in Fig. 3. The overall latency is determined by the number of DSP blocks, which in this case is $N/2$.

The featured symmetric systolic structure is generic so as to match the DSP block architecture of state-of-the-art FPGAs. Although the vendors put forward the systolic FIR filter, the synthesis of the structure faces two major challenges, discussed in the following subsections [II-A] and [II-B]. The achieved results are highlighted in section [II-C].

### A. Routability

Firstly, as the DSP blocks are embedded at dedicated locations in multiple chain-like structures, the interconnection capabilities are limited. In correlation with the filter order, the routability experiences less flexibility. Thus, successful mapping and routing of relatively large filters, compared to the number of DSP blocks, mainly depends on the ability of the development tools to exploit the DSP chain architecture. Even though a generic VHDL design permits an unrestricted synthesis, several failures were observed during the implementation process. Actually, physically separated DSP chains limit a realization of high-order FIR filters beyond the length of a DSP chain. An efficient concatenation of DSP chains is impossible for the evaluated tools without adaptation. Moreover, the mapping of the systolic structure to dedicated slices becomes more error prone, as the number of multiply-accumulate operations exceeds the total number of available DSP blocks. In this case, the tools cannot map the systolic FIR filter to the DSP blocks and distributed arithmetic built on the slice logic at the same time. In conclusion, the implementation of systolic FIR filters, which overlap multiple DSP chains, requires further efforts in the design. As a manual placement and routing is inadequate, the generic structure of the filter is adapted in such a manner so as to support the routability.

The routability is rapidly improved by further pipeline registers between the cascaded running sum. Consequently, theiterated function from Eq. (3) ultimately changes to

$$Y_k = \begin{cases} 
z^{-1}Y_{k-1} + h_{M-1-k} (z^{-b_k} + z^{-1-2k-b_k}) X(10) \\
z^{-1}Y_{k-1},
\end{cases} \tag{11}$$

where Eq. (11) covers the case that a register is inserted at an arbitrary position $k$ satisfying the condition $M-1 > k > 1$. The elements $b_k$ of Eq. (10) represent the number of injected registers before position $k$. At least one register between the DSP blocks breaks the systolic structure to match a two-column chain architecture. Dedicated routes of DSP chains are thus replaced through slice logic utilizing a simple register (Fig. 4). Moreover, this method also facilitates the routing of the systolic FIR structure within DSP blocks in combination with distributed arithmetic. After all of the above, the number of DSP blocks or the length of DSP chains no longer restricts the order of realizable digital filters.

### B. Timing

Secondly, within the scale of an FPGA, DSP chains are distantly located. Each type of device comes along with its specific physical dimensions and arrangement of configurable logic. However, the minimum clock period for the circuit primarily depends on the longest path between the logic elements. The interconnections of DSP chains can therefore be a bottleneck in terms of timing and thus limit the maximum achievable clock frequency. Even if the tools are capable of mapping systolic FIR filters spanning multiple DSP chains, the path lengths cannot be automatically reduced. In this case, a partial break with one register or more at distinguished positions in accordance with the DSP chain lengths reduces the overall path lengths (Fig. 3). The maximum clock frequency of the FPGA design is consequently the maximum sample rate of the filter. That limit is verified by timing constraints with the design tools.

### C. Results

For the proof of concept, we chose an FPGA from Xilinx (Artix 7, XC7A35T-3CSG324) and from Altera (Cyclone 5, 5CEFA5F23C6). Their DSP blocks [5], [6] are able to perform the basic operations from Fig. 1. The bit-widths of the generic VHDL design are adjusted to be $(W_A, W_B, W_C, W_D, W_E, W_F) = (15, 15, 16, 18, 34, 36)$, where the 15-bit wide input samples $(W_A, W_B)$ are adapted to our application, and, furthermore, the bit-widths of the multiplier $(W_C, W_D)$ and post-adder $(W_E, W_F)$ are chosen to avoid overflows and to fit into both FPGA architectures. To illustrate an example, a low-pass filter with a cutoff frequency $f_{pass}$ to be one-tenth of the sampling frequency $f_s$ and a stopband frequency $f_{stop}$ to be one-eighth of $f_s$ was selected. Furthermore, the stopband attenuation $A_{stop}$ is chosen to be 102 dB, which corresponds to the quantization noise floor of 18 bit signed coefficients. Estimating the number $N_{FIR}$ of taps with [15]

$$N_{FIR} \approx \frac{A_{stop}}{22 (f_{stop} - f_{pass})}, \tag{12}$$

![Fig. 3. A block diagram of the FIR filter structure from Eq. (5) with reduced initial pipeline delay.](image1)

![Fig. 4. The symmetric systolic FIR structure with additional registers for improved routability and timing. Registers between the systolic elements break the dedicated routes of DSP chains.](image2)
186 taps are required to achieve that frequency response. However, we truncated $N_{\text{FIR}}$ to 180, because the symmetry exploiting structure ultimately fits the total 90 DSP blocks of the Xilinx device. The Altera device includes 150 DSP blocks. Finally, the adaptation of the straightforward structure with dedicated register stages at distinct positions in the data path was evaluated and compared to the state-of-the-art FIR compiler tools [16, 17] in Tab. I.

| TABLE I | EXEMPLARY LOGIC UTILIZATION OF 90-TAP FIR FILTERS |
|---------|-----------------------------------------------|
| 90 taps | systolic structure | Vivado 2016.2 | XCTA35T-3CSG324 |
| straightforward | LUT: 6 / 20,800 | ALM: 3,145 / 29,080 |
| | Reg.: 10 / 41,600 | Reg.: 2,537 / 58,160 |
| | DSP: 90 / 90 | DSP: 76 / 150 |
| partial break ($z^{-1}$) | LUT: 5 / 20,800 | ALM: 2,682 / 29,080 |
| | Reg.: 6 / 41,600 | Reg.: 2,434 / 58,160 |
| | DSP: 90 / 90 | DSP: 76 / 150 |
| full break ($z^{-1}$) | LUT: 10 / 20,800 | ALM: 1,858 / 29,080 |
| | Reg.: 4 / 41,600 | Reg.: 544 / 58,160 |
| | DSP: 90 / 90 | DSP: 88 / 150 |
| full break ($z^{-2}$) | LUT: 15 / 20,800 | ALM: 1,069 / 29,080 |
| | Reg.: 7 / 41,600 | Reg.: 3736 / 58,160 |
| | DSP: 90 / 90 | DSP: 88 / 150 |
| Xilinx | FIR Compiler 7.2 | LUT: 320 / 20,800 |
| 16 | Reg.: 2,923 / 41,600 | not applicable |
| Altera | FIR Compiler 16.0 | ALM: 801 / 29,080 |
| 17 | not applicable | Reg.: 2,883 / 58,160 |

With identical configurations for the bit-widths, both tools were capable of implementing the systolic structure of the 90 taps FIR filter. Apparently, a Xilinx implementation is capable of including the tapped delay line and the output registers into DSP blocks in various ways. Therefore, the tool maps the investigated structures efficiently to the hardware architecture, consuming very less (< 0.5%) additional logic. On the contrary, the DSP architecture of Altera is not that versatile, as only one variant of the FIR filter structure results in competitive results with less than 1 % additional logic. As a result, the structure with one additional register stage at the output of each systolic element performs best in terms of resource utilization.

As discussed, the timing performance is improved by further registers breaking the dedicated routes. The obtained values from the tools are shown in Tab. II.

| TABLE II | MAXIMUM ACHIEVABLE CLOCK FREQUENCIES OF 90-TAP FIR FILTERS |
|---------|-----------------------------------------------|
| 90 taps | systolic structure | Vivado 2016.2 | XCTA35T-3CSG324 |
| straightforward | 238.10 MHz | 238.10 MHz |
| partial break ($z^{-1}$) | 303.03 MHz | 148.82 MHz |
| full break ($z^{-1}$) | 476.39 MHz | 218.77 MHz |
| full break ($z^{-2}$) | 526.32 MHz | 231.75 MHz |
| Xilinx | FIR Compiler | 451.78 MHz |
| 16 | not applicable | 213.72 MHz |

The best timing performance is achieved by the fully pipelined structure with two additional registers at each output. Further registers have no noticeable impact on timing. The values for the clock frequencies were obtained from the slow process corner of the timing reports. For the Xilinx implementation, the timing constraints were successively increased to reach the limit. Besides the improved timing in terms of maximum clock frequency, the overall latency of the filter is increased depending on the injected register stages.

In conclusion, at least one variant of our generic design utilizes less logic and operates at a higher clock frequency than the compiler-generated implementation. The efficiency is caused by the simplicity of the approach, whereas the automated design tools include excessive configuration options.

III. OPTIMIZED FIXED-POINT ARITHMETIC

For the implementation of high-order FIR filters, the coefficient quantization becomes significant, as the granularity of coefficients increases. Thus, an increased dynamic range for the quantization of coefficients preserves the accuracy of the digital filter. The precision of a signed fixed-point operation depends on the bit-width $b$ supported by the hardware. Hence, the transformation from a real coefficient $h$ to the corresponding integer value $I \in \mathbb{Z}$, used for a signed fixed-point calculation is, in general, described as:

$$I = \text{round}(h 2^{b-1}) \leftrightarrow \frac{I}{2^{b-1}} = h_I.$$  \hspace{1cm} (13)

An efficient method for an improved fixed-point precision was shown by Shen [13]. This method, referred to as "bit compression", performs a left shift operation on the integer value, until all redundant sign extension bits are removed. However, this equals a multiplication with $2^b$, and we calculate $Q$ as follows:

$$Q = \left\lfloor \log_2 \left( \frac{h b^{b-1}}{h} \right) \right\rfloor - (b - 1).$$  \hspace{1cm} (14)

The removal of sign extension bits increases the dynamic range of the fixed-point representation of the coefficients, but requires that all products are normalized to a common base before they are added by the accumulator. Therefore, Shen’s parallel method implementation performs a normalization at the input of the running sum accumulator. Indeed, the operation is incompatible to the DSP block architecture and is therefore synthesized on distributed logic. Thus, the proposed FIR filter structure does not exploit the entire performance of a hardware mapped systolic FIR filter.

In general, the normalization of a partial term $S$ from Eq. 1 to a common base is realized in fixed-point representation by:

$$2^{-d_k} S = \text{round} (h_k 2^{b-1+Q_k} (z^{-k} + z^{-1-k}) X$$  \hspace{1cm} (15)

where $Q_k$ is calculated by Eq. (14) and $d_k$ is a normalization factor, which must be individually calculated for each coefficient. Moreover, Eq. [5] reveals that the multiplication with $2^{d_k}$ (left shift operation) performs normalization and can be applied to the delayed input samples (Fig. 5). For our approach, the $d_k$ left shift operation for normalization is restricted by the bit-widths of the DSP block architecture, and therefore $Q_k$ must be limited to an upper value. The bounded value $Q_k$ is determined by the largest bit shift applicable
to the input samples but does not exceed the bit-width $W_C$ of the pre-adder. That method benefits from a generously designed pre-adder with regard to the bit-width. With a look at the contemporary DSP architecture from Xilinx \cite{6}, the pre-adder operates at $W_C = 25$ bit and the multiplier supports $25 \times 18$ bit operations. Thus, for 16-bit input samples and a 25-bit wide pre-adder, the limit of $Q_C$ is 9-bit.

A. Results

For the evaluation of the proposed structure from Fig. 5 we designed a low-pass filter of order 179 with the window method \cite{15} based on Nuttall’s window \cite{18}. Furthermore, the result of the FIR filter generated by the Xilinx FIR Compiler is compared to that of the proposed structure with additional bit shift operations and a floating point calculation. The frequency responses, which are derived by a Fourier transform of the simulated impulse responses of the filters, are shown in Fig. 6.

A comparison of frequency responses of the compiled FIR filter structures from Xilinx and Altera with 18 bit signed coefficients reveals no significant differences. However, our proposed structure with shift operations for coefficient normalization results in an improved stopband attenuation, even though it also exploits 18 bit signed coefficient multiplier. On a Xilinx FPGA, that structure utilizes exactly the same logic resources in comparison to the equivalent variant without left shift operations. The critical path delays remain constant without reducing the maximum clock frequency.

IV. Conclusion

In this brief, a systolic structure for a symmetric FIR filter was proposed, where the systolic elements ideally match the prevalent DSP block architecture of FPGAs. Thus, the derived iterative mathematical functions for the systolic structure support the mapping of a digital filter to various architectures with different constraints. Moreover, a generic FIR filter design was synthesized by the tools from Altera and Xilinx to evaluate the efficiency of the structure in terms of logic utilization and maximum clock frequency. The results confirmed that the proposed structure with additional register stages improves routability and timing of high-order FIR filters and is superior to state-of-the-art FIR compiler tools. Furthermore, to yield an increased dynamic range for coefficients quantization, we enhanced the structure by shift operations, thus improving the precision of fixed-point arithmetic. Finally, the exploitation of the entire DSP blocks enables an efficient realization of high-order FIR filters with fixed-point arithmetic in FPGAs, while utilizing less than 1% additional slice logic and running at clock frequencies above 200 MHz.

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