Low-Voltage, Low-Area, nW-Power CMOS Digital-Based Biosignal Amplifier

PEDRO TOLEDO\textsuperscript{1,2}, (Graduate Student Member, IEEE), PAOLO S. CROVETTI\textsuperscript{1}, (Senior Member, IEEE), HAMILTON D. KLIMACH\textsuperscript{2}, (Member, IEEE), FRANCESCO MUSOLINO\textsuperscript{1}, (Member, IEEE), AND SERGIO BAMPI\textsuperscript{2}, (Senior Member, IEEE)

\textsuperscript{1}Department of Electronics and Telecommunications (DET), Politecnico di Torino, 10129 Turin, Italy
\textsuperscript{2}Graduate Program in Microelectronics (PGMICRO), Federal University of Rio Grande do Sul, Porto Alegre 90010-150, Brazil

Corresponding author: Paolo S. Crovetti (paolo.crovetti@polito.it)

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ABSTRACT This paper presents the operation principle and the silicon characterization of a power efficient ultra-low voltage and ultra-low area fully-differential, digital-based Operational Transconductance Amplifier (OTA), suitable for microscale biosensing applications (BioDIGOTA). Measured results in 180nm CMOS prototypes show that the proposed BioDIGOTA is able to work with a supply voltage down to 400 mV, consuming only 95 nW. Owing to its intrinsically highly-digital feature, the BioDIGOTA layout occupies only 0.022 mm\textsuperscript{2} of total silicon area, lowering the area by 3.22 \times times compared to the current state of the art, while keeping reasonable system performance, such as 7.6 NEF with 1.25 \( \mu \)VRMS input referred noise over a 10 Hz bandwidth, 1.8% of THD, 62 dB of CMRR and 55 dB of PSRR.

INDEX TERMS Ultra-low voltage (ULV) CMOS, ultra-low power (ULP), operational transconductance amplifier (OTA), digital-based circuit, the Internet of Things (IoT).

I. INTRODUCTION Next-generation biosensing, which envisions drinkable, autonomous bio-electronic circuits with dimensions suitable to be internalized into the human body to sense and transmit clinical pieces of information (\textit{Body Dust}) [1], [2], as illustrated in Fig. 1, poses many critical challenges to integrated circuit (IC) designers.

Focusing on the analog signal acquisition, the stringent requirements in terms of low noise and distortion, typical of biosensing applications, need to be met under ultra-low area and power consumption restrictions, since a tight miniaturization and sub-\( \mu \)W operation are intrinsically demanded by the nature of the biosensing application [2].

While low power and low area can be achieved in digital ICs leveraging geometrical scaling provided by advanced Complementary Metal-Oxide-Semiconductor (CMOS) technology nodes [3], operation in near-threshold close to the minimum energy point [4], and energy-quality scaling [5], the same techniques cannot be applied to analog interfaces [6]–[8], which are indeed the bottleneck in terms of power, cost and performance of present day ICs, and in particular to those targeting biomedical signal acquisition [9]–[16].

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Given the above limitations, there has been an increasing research interest towards the implementation of traditional analog blocks by low-cost CMOS digital-based replacements. This concept has been previously proposed in all-digital phase-locked loops (PLLs) [17]–[19], Analog-to-Digital-Converters (ADCs) [20]–[34], Digital-to-Analog Converters (DACs) [20], [35]–[38], Low-Dropout Regulators (LDOs) [39]–[44], switching-mode power converters [45], [46], filters [47], [48], voltage references [49]–[51], temperature sensors [52], oscillators [53] and Operational Transconductance Amplifiers (OTAs) [54]–[63]. Most of these solutions achieve relevant area reduction and power savings compared to traditional analog solutions with similar performance, as shown in Fig. 2 [8], which make them potential candidates to meet the requirements of next-generation Body Dust biosensing. Besides, unlike traditional ones, this digital-based analog circuit design trend takes advantage of CMOS scaling and the benefits of an automatic digital design flow.

In this context, the DIGOTA approach presented in [54], [55] has been adopted in [64] to design a first-order filter addressing biomedical signal amplification targeting the Body Dust requirements in terms of extreme low area, low supply voltage, and low power. In this paper, silicon measurements for a Fully-Differential (FD) Digital-Based
Operational Transconductance Amplifier (BioDIGOTA), for which simulation results have been previously presented in [64], are shown for the first time, highlighting body dust can take advantage of the power and area reductions of digital-based analog design methodology. Furthermore, the erroneous Noise Efficiency Factor (NEF) and Power Efficiency Factor (PEF) evaluation found in [64] using simulation results are now fixed and re-calculated for the measurement data herein presented.

The paper is organized as follows: in section II, the DIGOTA circuit operation is revisited for a single-end structure, and its noise performance is compared with the current state of the art. Next, a new fully differential BioDIGOTA schematic is presented, along with design guidelines for power and noise reduction. In section IV, the measured performance of the proposed BioDIGOTA is shown and compared with other state-of-the-art designs. Finally, in section V, some concluding remarks are drawn.

II. BioDIGOTA CIRCUIT DESCRIPTION

The fully-differential BioDIGOTA circuit proposed in this paper is based on the single-ended DIGOTA topology presented in [54], [58], and [56], which exploits a Muller C-element gate implemented in CMOS - whose symbol, truth table and CMOS schematic are reported in Fig.3 - as an input stage. The operation of the single-ended DIGOTA [54] will be briefly revised before discussing the necessary modifications needed to achieve fully-differential operation and to meet the biosignal acquisition requirements [64].

A. SINGLE-ENDED DIGOTA CIRCUIT OPERATION

As shown in Fig.4a [54], [55], the single-ended DIGOTA circuit is comprised of two MullerC gates (MULLERC+,
MULLERC−), two inverters (INV+ and INV−), a common-mode compensation block (MCSwap) and a three-state buffer as an output stage. As any OTA, DIGOTA is intended to amplify the differential input signal while rejecting its common-mode component, and this is efficiently accomplished by a digital self-oscillating common-mode compensation loop, which drives the circuit through four different states A, B, C and D, depending on the logical value of the outputs of the inverters (MUL+, MUL−) [56], [58], as shown in Fig.4b. The same self-oscillating loop also performs differential-input-voltage-to-time and time-to-output-voltage conversion, in order to drive the output stage with digital pulses whose width is proportional to the input differential voltage, as described in the following.

In details, the two CMOS inverters are used to compare the voltage level of MullerC gates vMUL+,(−) with respect to their logic trip points (VT), resulting in four possible logical outputs: (MUL+, MUL−) = (0, 0), (1, 1), (1, 0), (0, 1) corresponding to states A, B, C and D in the state-transition diagram shown in Fig. 4b.

Asuming perfect matching and neglecting the delay of the inverters and of the gates in the MCSwap block [55], when VIN+ − VIN− = 0 the circuit oscillates between states A and C, with a natural oscillation period T0 approximately given by

\[ T_0 = 1/f_0 \approx \frac{\Delta V_{MUL} C_{MUL}}{I_{CM}} \approx \frac{V_{DD} C_{MUL}}{I_{CM}} \]  

where \( \Delta V_{MUL} \) is the swing of the MullerC elements output signals vMUL+,(−) (from simulations, it can be approximated to \( V_{DD} \)), C_{MUL} is their parasitic output capacitance, and I_{CM} is the equivalent drain current as a function of vIN+,(−).

As soon as a differential input signal is applied, i.e., vIN+ ≠ vIN−, the waveforms of vMUL+,(−) have different slopes, since the charging/discharging currents of the MullerC gates output parasitic capacitances, which depend on the vIN+,(−) voltages, are different (Fig. 4c for \( t > t_0 \)). For instance, in state A, in which vMUL+,(−) are both increasing, if vIN+ > vIN− (vIN+ < vIN−), vMUL− (vMUL+) is lagging since the capacitor C_{MUL} in the inverting (non-inverting) branch is charged by a lower current compared to the corresponding capacitor in the non-inverting (inverting) branch. In this way, vMUL− (vMUL+)
crosses the trip point of the inverter INV− (INV+) after \( v_{\text{MUL+}} \) (\( v_{\text{MUL−}} \)) crosses the trip point of the inverter INV+ (INV−) and, for a certain time interval (MUL+, MUL−) = (0, 1) ((MUL+, MUL−) = (1, 0)) the state B is activated as detailed in Fig.4b. An analogous behavior can be observed in state C, leading to transitions to state D, as shown in Fig. 4c for \( t > t_3 \).

In states B and D the output stage is triggered and \( v_{\text{out}} \) is either increased or decreased according to \( v_d \) sign, remaining in these states for a time interval

\[
\Delta t \approx \frac{\delta v_{\text{MUL}}(v_d)C_{\text{MUL}}}{I_{\text{MC}}}, \tag{2}
\]

proportional to \( \delta v_{\text{MUL}} = v_{\text{MUL+}} - v_{\text{MUL−}} \), which is in turn fairly proportional to the input differential voltage \( v_d \).

### B. FULLY-DIFFERENTIAL BioDIGOTA

The DIGOTA concept described in Sect.II-A is exploited in this paper to design a fully differential biosignal amplifier targeting the requirements of electrocardiogram (ECG) amplification [9]–[16], whose schematic is shown in Fig 5a and whose design is described in what follows [64].

The proposed fully-Differential (FD) BioDIGOTA includes a FD noise-optimized version of the single-end DIGOTA presented in last subsection II-A, detailed in Fig. 5b, and an on-chip capacitive feedback network \((C_{\text{in}}C_{\text{fp}}R_1)\) shown in Fig. 5a) implemented by Metal-insulator-Metal (MIM) capacitors and pseudo-resistors. In Fig. 5b, the Muller-C cells are implemented in CMOS as in Fig. 3, and the other logical gates (inverters, NANDs, NORs) are based on their canonical CMOS implementation [65].

Aiming to allow FD operation, the proposed FD-DIGOTA includes a Muller-C based input stage, two inverters and a MCswap common-mode compensation stage analogous in concept to the corresponding blocks of the single-ended version in Fig.4, whereas its output stage is now comprised of two three-state inverters so that to generate the positive and negative output voltages \( v_{\text{out+}} \) and \( v_{\text{out−}} \) at the same time, as needed to enforce a common-mode output voltage closer to \( V_{\text{DD}}/2 \). By contrast, whenever \( OUT^+ \neq OUT^- \), which implies that the CM output voltage differs from \( V_{\text{DD}}/2 \) by less than one half of the output differential signal \( v_{\text{d,out}} \), both the output stages are kept in a high impedance state.

In essence, from the truth table 1 it is observed that whenever \( IN^+ \) and \( IN^- \) are logically equal, the input common-mode is always compensated as in the single-ended DIGOTA circuit, whereas, the output common-mode component is either increased or decreased if \( OUT^+ \) and \( OUT^- \) are \((0,0)\) or \((1,1)\), and CM output stage is kept at high impedance only when \( OUT^+ \) and \( OUT^- \) is \((1,0)\) or \((0,1)\).

### C. BioDIGOTA PERFORMANCE ANALYSIS

Based on the same modeling approach adopted for the single-ended DIGOTA circuit in [55], the main performance of the proposed BioDIGOTA circuit can be evaluated as follows:

As detailed in [55], \( \delta v_{\text{MUL}} \) is related to \( v_d \) through a first order system, and train of current pulses \( i_{\text{OUT}} \) in Fig. 4c) with width equals to Eq. (2) also pass through a first order system at output stage, providing the following transfer function for the differential input signal

\[
A_D(s) = \frac{4g_mR_o \cdot \frac{I_{\text{DN}}}{C_{\text{IM}}}}{(1 + s \cdot 2 \cdot r_{\text{OUT}} C_{\text{L}}) \cdot (1 + s \cdot r_o C_{\text{MUL}})} \tag{3}
\]

where \( g_mR_o \) is the intrinsic gain of Muller-C stage, \( I_{\text{CM}} \) and \( r_o \) are the effective common-mode current and the effective output resistance of the Muller-C stage, defined as in [55], \( I_{\text{DN}} \) and \( r_{\text{OUT}} \) are the ON current and the output resistance of each output buffer, and \( C_{\text{L}} \) is the differential output capacitance.

The DIGOTA noise performance is dominated by the shot noise from the input devices within the Muller-C stage [55], where the in-band integrated input noise is given by

\[
\frac{v_{\text{IN}}}{N} = 2\pi \frac{2qI_{\text{CM}}}{g_{\text{m}}^2 f_{\text{BW}}} \tag{4}
\]

where \( q \) is the electrical charge and \( f_{\text{BW}} \) is amplifier bandwidth.
The NEF, Eq. (5), is a well-known metric to quantify the performance of low noise amplifiers for biomedical application.

\[ \text{NEF} = \frac{v_{IN, RMS}^2}{I_D} \]  

where \( \phi_T \) is the thermal voltage, \( k_B \) is the Boltzmann constant, \( T \) is the temperature, and \( I_D \) is current consumption.

Once the DIGOTA is designed to reduce the total noise, most of the power is consumed in the first stage (\( I_D \approx I_{CM} \)) given by Eq. (6) and its \( g_m \) is given by Eq. (7) for weak inversion regime.

\[ I_D = \frac{\text{Power}}{V_{DD}} = \frac{2C_{MUL}V_{DD}}{T_0} \]  
\[ g_m = \frac{I_D}{n\phi_T} \]

Substituting Eqs (1), (6) and (7) in (4) and after in (5), we have

\[ \text{NEF}_{\text{DIGOTA}} \approx n \]  

Fig. 6 compares \( \text{NEF} \) and the power efficiency factor \( \text{PEF} = \text{NEF}^2 V_{DD} \) of current state of the art of low frequency and low noise CMOS amplifier solutions. Among them, the discrete-time low-noise amplifier made by switched-capacitors achieves the best \( \text{NEF} \) and \( \text{PEF} \) at the cost of a big silicon area [11]. In [10], current reused is implemented to increase the equivalent transconductance by \( N \) stacked inverters and, then, the final \( \text{NEF} \) is reduced by \( \sqrt{N} \). However, the later of approach limits the minimum \( V_{DD} \). In the case of the proposed amplifier [64], the \( \text{NEF} \) is equivalent to the stacked inverters for \( N = 1 \), but no any bias circuit is needed, the circuit is compatible to digital flow, and the total silicon area is further reduced.
III. BioDIGOTA CIRCUIT DESIGN

The proposed FD BioDIGOTA has been designed and fabricated in 180nm CMOS and its layout is shown in Fig. 7a along with its micro-photo. Once most of the noise contribution is related to the input stage [55], its design deserves a special care in order to meet the requirements of biomedical signal amplification. For this purpose, the area of the Muller-C is increased one hundred times compared to [64] to reduce noise [66], by connecting one hundred cells in parallel. The delays of the non-inverting and inverting signal paths have been matched and the active components have been integrated under the MiM capacitors to further reduce the area of the layout. The circuit layout occupies just 0.022 mm$^2$, thus achieving 3.322× lower silicon area compared to the minimum size found in the current literature [14]. In Fig. 7a, the area breakdown shows that more than 50% of the area is occupied by the MullerC logic-gates while almost 40% of the total is covered by the MiM capacitors of the feedback network. In other words, only 0.018 of 0.022 mm$^2$ is dedicated to the active devices, including the pseudo-resistors.

IV. MEASUREMENTS RESULTS

Three BioDIGOTA samples have been measured and their performance has been compared with biosignal amplifiers presented in recent literature. The 3Hz frequency time-domain input and output measured waveforms of the proposed FD BioDIGOTA at $V_{DD} = 400$mV and $C_{out} = 10$ pF capacitive load are reported in Fig.7b and reveal the operation of the circuit as a filter with less than 2% THD and 100nW of power consumption. Under such conditions, the BioDIGOTA circuit works properly with an output swing larger than 400 mV peak-to-peak, as shown in Fig.7b, offering 10Hz bandwidth with 35 dB gain, without slew-rate distortion, meaning its slew-rate exceeds 12 V/s.

A DC voltage gain of 35 dB has been measured for this configuration. The power breakdown is also included in the Fig.7a. A relevant power is consumed in the first stage, as expected, to reduce the noise. The wide-band output spectrum is reported in Fig.7c, revealing in-band harmonics (THD=1.8%). Table 2 shows THD measured for all three samples.

In [64], the proposed BioDIGOTA has been verified under process and mismatch variations by Monte Carlo (MC) simulations performed on 100 samples, achieving $\frac{\sigma}{\mu} = 34\%$ for output THD having a mean value of $\mu = 5.13\%$, $\frac{\sigma}{\mu} = 41\%$ for noise having $\mu = 1.97\mu V_{RMS}$, and $\frac{\sigma}{\mu} = 20.1\%$ for the power consumption having $\mu = 146nW$. $\sigma$ represents the standard deviation.

A. DIFFERENTIAL AMPLIFICATION, CMRR, AND PSRR FREQUENCY RESPONSE

The measured frequency response of the BioDIGOTA differential amplification is reported in Fig.8a and reveals 35dB in-band gain and 10Hz bandwidth under $C_{out} = 10$pF load. In the same plot, the common-mode rejection ratio (CMRR) and the power supply rejection ratio (PSRR) are also depicted, revealing a CMRR exceeding 62dB and a PSRR exceeding 55 dB in the signal bandwidth for the best sample (sample #3).

B. NOISE

Fig.9 shows the measured power spectral density of the input-referred noise for the three samples. The BioDIGOTA integrated noise over the entire bioDIGOTA bandwidth
TABLE 2. Measured performance for all three samples @ $V_{DD} = 400\text{mV}$, 27 °C temperature, input amplitude of 3.5mV and frequency of 3 Hz.

| Sample Number | THD (%) | Power (nW) | Gain (dB) | Noise ($\mu V_{RMS}$) | NEF | PEF |
|---------------|---------|------------|-----------|-----------------------|-----|-----|
| 1             | 1.7     | 100.84     | 34.3      | 2.52                  | 15.69 | 98.49 |
| 2             | 1.25    | 78.63      | 36.84     | 2.13                  | 11.73 | 55  |
| 3             | 1.8     | 95         | 35        | 1.25                  | 7.59  | 23  |

The measured results of sample #3 (bold) are also presented in the comparison table (Table 3).

TABLE 3. Performance summary and comparison.

| Performance | [16] | [12] | [13] | [14] | [10] | [11] | [68] | [69] | This work* |
|-------------|------|------|------|------|------|------|------|------|------------|
| Design      | Analog | Analog | Analog | Analog | Analog | Analog | Analog | Analog | Digital |
| Technology  | 180   | 65   | 65   | 180  | 180  | 180  | 180  | 130  | 180  nm |
| Supply      | 0.2/0.8 | 0.6 | 0.6  | 1    | 0.45 | 1.2  | 1.35 | 1    | 1.2     |
| Die Area    | 1     | 0.2  | 0.6  | 0.29 | 0.25 | 0.071 | 0.24 | 2.33 | 0.19 | 0.1 |
| Power       | 790   | 1    | 16.8 | 250  | 730  | 2,000 | 18.7 | 620  | 800  | 35,800 |
| BW          | 670   | 370  | 250  | 10,000 | 5,000 | 240  | 5,000 | 5,000 | 100,000 |
| CMRR        | 85    | 60   | 80   | 84   | 73   | -    | 95   | 91.8 | 58   | 62 |
| PSRR        | 74    | 63   | 67   | 76   | 80   | -    | 68   | 83   | 54   | 67 |
| THD         | 0.3   | 0.53 | 0.02 | 0.16 | 0.025 | 1    | 1    | 1.8% |
| Input-Referred Noise | 36 | 1,400 | 253   | 43   | 29   | 40   | 158  | 11.85 | 59.18 | 13 | 395 |
| NEF         | 2.1   | 2.1  | 2.64 | 1.07 | 1.57 | 4.9  | 0.86 | 0.45 | 2    | 2.5  | 7.6 |
| PEF         | 1.6   | 2.64 | 4.1  | 1.14 | 1.12 | 28   | 0.99 | 0.2  | 4    | 7.5  | 23 |
| $NEF_{AREA} = \frac{NEF \times Area_{mm^2}}{Area_{mm^2}}$ | 2.1  | 0.42 | 1.58 | 0.31 | 0.39 | 0.35 | 0.2064 | 1.045 | 0.38 | 0.25 |
| $PEF_{AREA} = \frac{PEF \times Area_{mm^2}}{Area_{mm^2}}$ | 1.6 | 0.528 | 2.46 | 0.33 | 0.28 | 1.98 | 0.238 | 0.466 | 0.76 | 0.75 | 0.46 |

FIGURE 8. Gain, CMRR, and PSRR at $V_{DD} = 400\text{mV}$.

(0.05 Hz - 10 Hz specify the bandwidth here) is $1.25\mu V_{RMS}$, corresponding to a 395 nV/$\sqrt{\text{Hz}}$ average PSD over the same bandwidth for sample #3. Power, NEF and PEF are listed for all samples in Table 2. Amongst all samples, the lowest NEF and PEF found are 7.6 and 23, respectively, for the sample #3.

C. COMPARISON WITH THE STATE OF THE ART

Compared to biosignal amplifiers proposed in recent literature [9]–[16], whose performance is summarized in Tab. 3, the BioDIGOTA presented here is able to work properly at the lowest $V_{DD}$ (2× lower than [12], [13]), at the lowest silicon area (3.22× lower than [14]), keeping reasonable noise performance. These results prove that digital-based analog design is very attractive for body dust applications. The comparison in terms of NEF and PEF versus area is also illustrated in Fig. 10. If the NEF and PEF are both...
and Va ULV Passive-less FD BioDIGOTA has been presented here are available for any fabrication process. To enable process-counterpart when operating in Ultra Low Voltage (ULV) and digital domain, presenting lower silicon area than its analog counterpart, as previously predicted in Fig. 2 [8].

In this paper, the authors have proposed a FD Digital-based NEF, and area reduction, as previously predicted in Fig. 2 [8].

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In this paper, the authors have proposed a FD Digital-based OTA that emulates an analog biomedical amplifier in the digital domain, presenting lower silicon area than its analog counterpart when operating in Ultra Low Voltage (ULV) and Ultra Low Power (ULP) conditions. The proposed architecture can also be implemented using CMOS standard-cells that are available for any fabrication process. To enable processing the bio-potential signals digitally with static logic gates, a ULV Passive-less FD BioDIGOTA has been presented here achieving at $V_{DD} = 400$ mV a NEF = 7.6 and PEF = 23, while consuming just 95 nW and 0.022 mm² of silicon area with 35 dB gain and 395 nW/$\sqrt{\text{Hz}}$ power spectral density. Through this implementation, digital-based analog design has been proven to be a good alternative for reducing area and design effort for body dust applications working in low voltage domain.

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REFERENCES

[1] S. Carrara and P. Georgiou, “Body Dust: Miniaturized highly-integrated low power sensing for remotely powered drinkable CMOS bioelectronics,” Apr. 2018, arXiv: 1805.05840.

[2] S. Carrara, “Body dust: Well beyond wearable and implantable sensors,” IEEE Sensors J., vol. 21, no. 11, pp. 12398–12406, Jun. 2021.

[3] R. H. Dennard, “Past progress and future challenges in LSI Technology: From DRAM and scaling to ultra-low-power CMOS,” IEEE Solid-State Circuits Mag., vol. 7, no. 2, pp. 29–38, 2015.

[4] N. Pinckney, D. Blauuw, and D. Sylvester, “Low-power near-threshold design: Techniques to improve energy efficiency,” IEEE Solid State Circuits Mag., vol. 7, no. 2, pp. 49–57, Jun. 2015.

[5] M. Alioto, “From less batteries to battery-less alert systems with wide power adaptation down to nWs—Towards a smarter, greener world,” IEEE Design Test, vol. 38, no. 5, pp. 90–133, Oct. 2021.

[6] A. L. S. Lake, C. K. Lee, and B. M. Leary, “Nanoscale CMOS implications on analog/mixed-signal design,” in Proc. IEEE Custom Integrate Circuits Conf. (CICC), Apr. 2019, pp. 1–5.

[7] P. S. Crovetti, F. Musolino, O. Aiello, P. Toledo, and R. Rubino, “Breaking the boundaries between analogue and digital,” Electron. Lett., vol. 55, no. 12, pp. 672–673, Jun. 2019.

[8] P. Toledo, R. Rubino, F. Musolino, and P. Crovetti, “Re-thinking analog integrated circuits in digital terms: A new design concept for the IoT era,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 68, no. 3, pp. 816–822, Mar. 2021.

[9] Y. Zhang, F. Zhang, Y. Shakhsheer, J. D. Silver, A. Klinfelter, M. Nagarajan, J. Boyle, J. Pandey, A. Shrivastava, E. J. Carlson, and A. Wood, “A batteryless 19 µW MICS/ISM-band energy harvesting body sensor node for ExG applications,” IEEE J. Solid-State Circuits, vol. 48, no. 1, pp. 199–213, Dec. 2013.

[10] S. Mondal and D. A. Hall, “A 13.9-nA ECG amplifier achieving 0.86/0.99 NEF/PEF using AC-coupled OTA-stacking,” IEEE J. Solid-State Circuits, vol. 55, no. 2, pp. 414–425, Feb. 2020.

[11] G. Atzeni, A. Novello, G. Cristiano, J. Liao, and T. Jang, “A 0.450/0.2 NEF/PEF 12-nV/$\sqrt{\text{Hz}}$/highly configurable discrete-time low-noise amplifier,” IEEE Solid-State Circuits Lett., vol. 3, pp. 486–489, 2020.

[12] P. Harpe, H. Gao, R. van Dommele, E. Cantatore, and A. H. M. van Roermund, “A 0.20 mm² 3 nW signal acquisition ic for miniature sensor nodes in 65 nm CMOS,” IEEE J. Solid-State Circuits, vol. 51, no. 11, pp. 2430–2438, Oct. 2016.

[13] Y.-P. Chen, D. Jeon, Y. Lee, Y. Kim, Z. Foo, J. Lee, N. B. Langhals, G. Kruger, H. Oral, O. Berenfeld, and Z. Zhang, “An injectable 64 nW ECG mixed-signal SoC in 65 nm for arrhythmia monitoring,” IEEE J. Solid-State Circuits, vol. 50, no. 1, pp. 379–390, Jan. 2015.

[14] H. Chandrakumar and D. Markovic, “An 80-mVpp linear-input range, 1.6-o input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to 650-mVpp common-mode interference,” IEEE J. Solid-State Circuits, vol. 52, no. 11, pp. 2811–2828, Oct. 2017.

[15] D. Han, Y. Zheng, R. Rajkumar, G. S. Dawe, and M. Je, “A 0.45 V 100-channel neural-recording ic with sub-µW/channel consumption in 0.18 µm CMOS,” IEEE Trans. Biomed. Circuits Syst., vol. 7, no. 6, pp. 735–746, Dec. 2013.

[16] F. M. Yaul and A. P. Chandrakasan, “A noise-efficient 36 nV/$\sqrt{\text{Hz}}$ Chopper amplifier using an inverter-based 0.2-V supply input stage,” IEEE J. Solid-State Circuits, vol. 52, no. 11, pp. 3032–3042, Sep. 2017.

[17] R. B. Staszewski, K. Muhammad, D. Leipold, C.-M. Hung, Y.-C. Ho, J. L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, and J. Koh, “All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS,” IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.

[18] Y. Park and D. D. Wentzloff, “An all-digital PLL synthesized from a digital standard cell library in 65nm CMOS,” in Proc. IEEE Custom Integrate Circuits Conf. (CICC), Sep. 2011, pp. 1–4.

[19] W. Deng, D. Yang, T. Ueno, T. Siriburanon, S. Kondo, K. Okada, and A. Matsuzawa, “A fully synthesizable all-digital PLL with interpolative phase coupled oscillator, current-output DAC, and fine-resolution digital varactor using gated edge injection technique,” IEEE J. Solid-State Circuits, vol. 50, no. 1, pp. 68–80, Jan. 2015.

[20] P. S. Crovetti, “All-digital high resolution D/A conversion by dyadic digital pulse modulation,” IEEE J. Solid-State Circuits, vol. 39, no. 5, pp. 1–5, May 2004.

[21] M.-J. Seo, Y.-J. Roh, D.-J. Chang, W. Kim, Y.-D. Kim, and S.-T. Ryu, “A reusable code-based SAR ADC design with CDAC compiler and synthesizable analog building blocks,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 12, pp. 1904–1908, Dec. 2018.

[22] O. Aiello, P. Crovetti, and M. Alioto, “Fully synthesizable low-area analogue-to-digital converters with minimal design effort based on the dyadic digital pulse modulation,” IEEE Access, vol. 8, pp. 70890–70899, 2020.

[23] J.-E. Park, Y.-H. Hwang, and D.-K. Jeong, “A 0.5-V fully synthesizable SAR ADC for on-chip distributed waveform monitors,” IEEE Access, vol. 7, pp. 63686–63697, 2019.
[25] S. Weaver, B. Hershberg, and U.-K. Moon, “Digitally synthesized stochas-
tic flash ADC using only standard digital cells,” *IEEE Trans. Circuits Syst.
I, Reg. Papers*, vol. 61, no. 1, pp. 84–91, Jan. 2014.

[26] A. Fahmy, J. Liu, T. Kim, and N. Maghari, “An all-digital scalable and
reconfigurable wide-input range stochastic ADC using only stan-
dard cells,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 8,
pp. 731–735, Aug. 2015.

[27] A. Waters and U.-K. Moon, “A fully automated verilog-to-layout synthe-
sized ADC demonstrating 56 dB-SNR with 2MHz-BW,” in *Proc. IEEE
Asian Solid-State Circuits Conf.* (A-SSCC), Nov. 2015, pp. 1–4.

[28] M. Z. Straayer and M. H. Perrott, “A 12-bit, 10-MHz bandwidth,
continuous-time ΣΔ ADC with a 5-bit, 950-MS/s-VCSoC-based quantizer,”
*IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, Mar. 2008.

[29] G. Taylor and I. Galton, “A mostly-digital variable-rate continuous-time
delta-sigma modulator ADC,” *IEEE J. Solid-State Circuits*, vol. 45, no. 12,
pp. 2634–2646, Dec. 2010.

[30] V. Nguyen, F. Schembri, and R. B. Staszewski, “A 0.2-V 30-MS/s 11b-
ENOB open-loop VCO-based ADC in 28-nm CMOS,” *IEEE Solid-State
Circuits Lett.*, vol. 1, no. 9, pp. 190–193, Sep. 2018.

[31] G. G. E. Gielen, L. Hernandez, and P. Rombouts, “Time-encoding analog-
to-digital converters: Bridging the analog gap to advanced digital CMOS—
Part 1: Basic principles,” *IEEE Solid State Circuits Mag.*, vol. 12, no. 2,
pp. 47–55, Jun. 2020.

[32] G. G. E. Gielen, L. Hernandez, and P. Rombouts, “Time-encoding analog-
to-digital converters: Bridging the analog gap to advanced digital CMOS—
Part 2: Architectures and circuits,” *IEEE Solid State Circuits Mag.*, vol. 12,
no. 3, pp. 18–27, Aug. 2020.

[33] V. Unnikrishnan and M. Vesterbacka, “Time-mode analog-to-digital con-
version using standard cells,” *IEEE Trans. Circuits Syst. I, Reg. Papers*,
vol. 61, no. 12, pp. 3348–3357, Dec. 2014.

[34] A. Jayaraj, M. Danesh, S. T. Chandrasekaran, and A. Sanyal, “76-dB
DR, 48 fstep second-order VCO-based current-to-digital converter,”
*IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 4, pp. 1149–1157,
Apr. 2020.

[35] E. Ansari and D. D. Wentzloff, “A 5 mW 250 MS/s 12-bit synthesized
digital-to-analog converter,” in *Proc. IEEE Custom Integ. Circuits Conf.*,
Sep. 2014, pp. 1–4.

[36] P. S. Crovetti, R. Rubino, and F. Musolinio, “Relaxation digital-to-analog
converter with foreground digital self-calibration,” in *Proc. IEEE Int.
Symp. Circuits Syst. (ISCAS)*, Oct. 2020, pp. 1–5.

[37] O. Aiello, P. Crovetti, and M. Aliotto, “Standard cell-based ultra-compact
DACs in 40-nm CMOS,” *IEEE Access*, vol. 7, pp. 126479–126488, 2019.

[38] O. Aiello, P. Crovetti, and M. Aliotto, “Fully synthesizable low-area digital-
to-analog converter with graceful degradation and dynamic power
resolution scaling,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 8,
pp. 2865–2875, Aug. 2019.

[39] Y. Okuma, K. Ishida, Y. Ryu, X. Zhang, P.-H. Chen, K. Watanabe,
M. Takamiya, and T. Sakurai, “0.5-V input digital LDO with 98.7% current
efficiency and 2.7 μA quiescent current in 65 nm CMOS,” in *Proc. IEEE
Custom Integ. Circuits Conf.*, Sep. 2010, pp. 1–4.

[40] S. Bang, W. Lim, C. Augustine, A. Malavasi, M. Khellah, J. Tschanz,
and V. De, “25.1 A fully synthesizable distributed and scalable all-digital
LDO with adaptive current step size control,” in *Proc. IEEE Custom Integ.
Circuits Conf.*, Oct. 2019, pp. 1–5.

[41] G. Palumbo and G. Scotti, “A novel standard-cell-based implementation of
the digital OTA suitable for automatic place and route,” *J. Low Power
Electron. Appl.*, vol. 11, no. 4, p. 42, Oct. 2021. [Online]. Available:
https://www.mdpi.com/2079-9292/9/9/1410

[42] P. Toledo, O. Aiello, and P. S. Crovetti, “A 300 mV-supply standard-cell-
based OTA with digital PWM offset calibration,” in *Proc. IEEE Nordic
Circuits Syst. Conf. (NORCAS), NORCHIP Int. Symp. Syst.-on-Chip (SoC),
2019*, pp. 1–5.

[43] P. S. Crovetti, “A digital-based analog differential circuit,” *IEEE Trans.
Circuits Syst. I, Reg. Papers*, vol. 60, no. 12, pp. 3107–3116, Dec. 2013.

[44] S. Kalani and P. R. Kinget, “Zero-crossing-time-difference model for
stability analysis of VCO-based OTAs,” *IEEE Trans. Circuits Syst. I, Reg.
Papers*, vol. 67, no. 3, pp. 839–851, Mar. 2020.

[45] S. Kalani, A. Bertolini, A. Richelli, and P. R. Kinget, “A 0.2 V 492 mW
VCO-based OTA with 60 kHz UGB and 207 μVrms noise,” in *Proc. IEEE
Int. Symp. Circuits Syst. (ISCAS)*, May 2017, pp. 1–4.

[46] G. Cai, C. Zhan, and Y. Liu, “A 0.7 V fully-on-chip pseudo-
digital LDO regulator with 6.3 μA quiescent current and 100 mV dropout
voltage in 180nm CMOS,” in *Proc. IEEE 44th Eur. Solid State Circuits
Conf. (ESSCIRC)*, Sep. 2018, pp. 206–209.

[47] Y. Lu, F. Yang, F. Chen, and P. K. T. Mok, “A distributed power delivery
grid based on analog-assisted digital LDOs with cooperative regulation
and IR-drop reduction,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67,
no. 8, pp. 2859–2871, Aug. 2020.

[48] L. Qian, D. Li, K. Qian, Y. Ye, Y. Xia, and T. Mak, “A fast-transient
response digital low-dropout regulator with dual-modes tuning technique,”
*IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 12, pp. 2943–2947,
Dec. 2020.

[49] S. J. Kim, R. K. Nandwana, Q. Khan, R. C. N. Pilawa-Podgurski, and
P. K. Hanumolu, “A 4-phase 30–70 MHz switching frequency buck con-
verter using a time-based compensator,” *IEEE J. Solid-State Circuits*,
vol. 50, no. 12, pp. 2814–2824, Dec. 2015.
PEDRO TOLEDO (Graduate Student Member, IEEE) received the B.Sc. degree in electronic engineering from the Universidade Federal de Pernambuco (UFPE), Recife, Brazil, in 2010, and the M.Sc. degree in microelectronics from the Universidade Federal do Rio Grande do Sul (UFRGS), Porto Alegre, Brazil, in 2015. He is currently pursuing the joint Ph.D. degree with the Politecnico di Torino and the Universidade Federal do Rio Grande do Sul, working with digital-based analog processing for IoT applications. He completed the IC-Brazil Program, in 2011. His research interest includes electrical engineering, focusing on analog/RF CMOS design and microelectronic education. He currently works as an AMS Circuit Designer at Synopsys with sub-10 nm CMOS technologies for high performance computer. He is a Graduate Student Member of the IEEE Circuits and Systems Society and the IEEE Solid-State Circuits Society.

PAOLO S. CROVETTI (Senior Member, IEEE) was born in Turin, Italy, in 1976. He received the Laurea (summa cum laude) and Ph.D. degrees in electronic engineering from the Politecnico di Torino, Turin, Italy, in 2000 and 2003, respectively. He is currently an Associate Professor with the Department of Electronics and Telecommunications (DET), Politecnico di Torino and the Universidade Federal do Rio Grande do Sul, Porto Alegre, Brazil, in 1988 and 1994, respectively. He is currently a Visiting Research Advisor at the Microelectronics Graduate Program (PGMicro), Federal University of Rio Grande do Sul. Since 2016, he has been a Local Coordinator of the Training Center 1 of the Brazilian Design Training Program (IC Brazil Program), where he has been serving as a Lecturer, since 2009. His research interests include the areas of analog, mixed-signal and RF IC design, in semiconductor devices variability modeling. He is a member of the IEEE Circuits and Systems Society and IEEE Solid-State Circuits Society.

FRANCESCO MUSOLINO (Member, IEEE) was born in Turin, Italy, in 1972. He received the Laurea and Ph.D. degrees in electronic engineering from the Politecnico di Torino, Turin, Italy, in 1999 and 2003, respectively. He is currently a Researcher with the Department of Electronics and Telecommunications (DET), Politecnico di Torino, where he teaches courses on power electronics and electronics for electric drives. His research interests include electronics for power conversion and motor drive applications, mixed-signal circuits, electromagnetic compatibility at the system levels, and the analysis, modeling, and experimental characterization of electromagnetic compatibility problems at the printed circuit board and package level.

SERGIO BAMPI (Senior Member, IEEE) received the B.Sc. degree in electronics and the B.Sc. degree in physics from the Federal University of Rio Grande do Sul (UFRGS), in 1979, and the M.Sc. and Ph.D. degrees in electrical engineering from Stanford University, in 1982 and 1986, respectively. He is currently a Full Professor at the UFRGS Informatics Institute. He was a Distinguished Lecturer (2009–2010) of IEEE Circuits and Systems Society, the Technical Director of the Microelectronics Center CEITEC (2005–2008), and is the past President of the FAPERGS Research Funding Foundation. He was a Visiting Research Professor at Stanford University (1998–1999) and the Director of the National Supercomputer Center (1993–1996). He has coauthored more than 480 articles in the field of CMOS circuit design and CAD. His research interests include the area of IC design and modeling, mixed-signal and RF CMOS circuits design, architectures and SoCs for image and video processing, nano-CMOS devices, ultra-low power digital CMOS design, and dedicated complex algorithms and architectures. He chaired LASCAS 2013, SBCCI 1997 and 2005, and SBMICRO 1989 and 1995. He served as the President of scientific societies SBPC and SBMICRO (2002–2004) and a Council Member of IEEE SSC Society, Brazilian Computer Society, and Brazilian Society for Advancement of Science.

HAMILTON D. KLI MACH (Member, IEEE) received the B.E. and M.Sc. degrees in electrical engineering from the Federal University of Rio Grande do Sul, Porto Alegre, Brazil, in 1988 and 1994, respectively, and the Dr.Eng. degree in electrical engineering from the Federal University of Santa Catarina, Florianopolis, Brazil, in 2008. Since 1990, he has been a Full Professor with the Department of Electrical Engineering, Federal University of Rio Grande do Sul, where he was the Head of the Department, from 2010 to 2011, and the M.Sc. and Dr.Eng. Advisor at the Microelectronics Graduate Program (PGMicro), Federal University of Rio Grande do Sul. Since 2016, he has been a Local Coordinator of the Training Center 1 of the Brazilian Design Training Program (IC Brazil Program), where he has been serving as a Lecturer, since 2009. His research interests include the areas of analog, mixed-signal and RF IC design, in semiconductor devices variability modeling. He is a member of the IEEE Circuits and Systems Society and IEEE Solid-State Circuits Society.