The Architecture of Memory for Core Processors

Amit Aggarwal* and Sanket Kansal**

ABSTRACT

The effectiveness and storage capacity of single-bit cache memory have been investigated. Write driver circuit, random access memory cell, and current mode detector make up the single-bit cache. Using various strategies, such as power-saving components like current mode sensing amplifiers and static random access memory cells, memory systems with just one bit of cache can use less power. To save power, substitute a forced stack and a current mode detecting amplifier for a single-bit cache.

Keywords: Current Mode Sense Amplifier (CMSA); Single Bit SRAM CMSA Architecture (SBSCMSA); Sense Amplifier (SA); Static Random-Access Memory Cell (SRAMC); Write Driver Circuit (WDC).

1.0 Introduction

As transistors get smaller, large integrated circuits can have more circuits and function better. Transistors in most integrated circuits are connected by wiring [1-4]. The wiring within a semiconductor is referred to as the "global interconnect on-chip." Other global linkages, including those connecting cache memory to CPUs, are emerging alongside breakthroughs in submicron VLSI technology. How long it takes to make depends on how many connections a chip has globally [5-7]. Transceivers and signalling protocols enable faster message transmission. The recordings of sense amplifiers used as connection receivers allowed for this discovery. A combination of the SRAMC and sense amplifier has also been suggested [8-10].

1.1 Power reduction techniques

The requirements of a circuit are met while using less electricity [11].

1.1.1 Sleep transistor technique

State-destructive operations can harm PMOS and NMOS sleep transistors connected to the supply voltage or ground. The same technology is known by the names VDD and gated-ground [12]. Sleep semiconductor technology lowers the power used during sleep by separating logical networks from sleep transistors (see Figure 1).

1.1.2 Forced stack technique

Figure 2 illustrates the forced stack. Costs can be further decreased by stacking transistors. By turning off lots of transistors at once, stacking the semiconductor device lowers the subthreshold leakage current [13].

*Corresponding author; Senior Engineer, Adobe Systems India Pvt. Ltd., Noida, Uttar Pradesh, India (E-mail: amitcs06@gmail.com)
**HXM Practice Partner, DXC Melbourne, Victoria, Australia (E-mail: sanketkansal@yahoo.com)
1.1.3 Dual sleep technique

Every component in the circuit is either NMOS or NMOS-like (NM0 and NM1). On the other hand, the header and footer employ NMOS and PMOS transistors, respectively. The two options are "on" and "off" [14]. These two devices operate normally when not used, as seen in Figure 3.

2.0 Single-Bit Memory Architecture

Figure 4 depicts an example of single-bit cache memory. This machine's most critical components include SRAMC/WDC/CMSA. The description has three sections: Bit, WE, and BL escape BLBAR as BLBAR moves into WDC [15,16]. The SRAMC's two output pins are designated by the letters WL and V1. Ysel/BL/BLBAR/PCH/SAEN inputs are available when the CMSA is connected to the WDC.
2.1 WDC

Figure 5 shows the write driver for this application. The bit line's high pre-load level is below the writing margin of the SRAMC when the WDC is turned on. With the aid of a WDC, the necessary voltage may be calculated. When WE are set to 1, all data received from an input line is sent to that line's bit lines. The word "Write Enable" is highlighted at the very top of the code. Finally, access transistors provide the data to the proper memory cell. Before the WDC, each computer bit cell was required to have a particular value [17,18].
2.2 Conventional SRAM

The shifting of the 6T SRAMC is shown in Figure 6. Due to how much data they can store, "static RAM cells" are also known as SRAMCs. Six NM8/NM9 NMOS transistors and six CMOS inverters serve as access transistors for the SRAMC (PM6, PM7, NM6, and NM7). The cross-coupled inverters for each bit are constructed using transistors and SRAMC. The only possible values in the cell [19,20] are 0 or 1. In a bi-stable latching circuit, two inverters control six SRAMC transistors.

Figure 6: Conventional SRAM

![Diagram of Conventional SRAM]

2.3 CTDSA

The sensing amplifier plays a key role in the cache memory's construction. Only one of the two-bit lines is wired to the power source during reading. A current sense amplifier comprises various parts that talk to one another [21-23].

Figure 7: CTDSA

![Diagram of CTDSA]
3.0 Analysis of Result

In this section, the output of each circuit is described and rated. Figure 8 displays the SAEN, WL, and CMSA open and reading data. This sensing amplifier can read only the bit lines of SRAM cells. The bit lines provide data to V3 and V4.

![CTDSA Output Waveform](image)

**Figure 10: CTDSA Output Waveform**

| S.No. | Parameters | Power Consumption | Sensing Delay |
|-------|------------|-------------------|---------------|
| 1.    | R=42.3Ω   | 25.78µW           | 20.41ηs       |
| 2.    | R=42.3KΩ  | 30.87µW           | 20.41ηs       |

Less power is needed as the resistance rises. A circuit's resistance impacts its size, functionality, and speed. In essence, it makes the spread of authority more challenging.

**Table: 2 Different Parameters While Utilizing Different Power-Reduction Methods Over SA**

| Techniques        | Architecture | SBSCMSA |          |          |
|-------------------|--------------|---------|----------|----------|
|                   |              | Power Consumption | Sensing Delay | No. of Transistors |
| Dual Sleep        |              | 26.68 µW   | 20.11 ns  | 40       |
| Sleep Transistor  |              | 26.78 µW   | 20.51 ns  | 38       |
| Forced Stack      |              | 26.88 µW   | 20.81 ns  | 38       |

To cut down on power usage when using a forced stack technique, CMSA uses the SRAM strategy shown in Table 3.

**Table 3: Utilizing Various Power Reduction Techniques, SRAM with CMSA Power Consumption**

| Techniques        | SBSCMSA |          |
|-------------------|---------|----------|
|                   | Power Consumption | Sensing Delay |
| Dual Sleep        | 24.32 µW   | 20.11 ns  |
| Sleep Transistor  | 26.55 µW   | 20.51 ns  |
| Forced Stack      | 25.55 µW   | 20.81 ns  |
4.0 Conclusion

Researchers examined single-bit cache memory to determine its effectiveness. Single-bit cache memory comprises a write driver circuit, a static random access memory cell, and a current mode detection amplifier. Single-bit cache memories can consume less power using sleep transistors, forced stacks, and dual sleep on components like current-mode sensors and static random-access memories. In this study, it was discovered that SRAM cells consumed less power than single-bit caches.

References

1. Y. He, J. Zhang, X. Wu, X. Si, S. Zhen, and B. Zhang, "A Half-Select Disturb-Free 11T SRAM Cell with Built-In Write/Read-Assist Scheme for Ultralow-Voltage Operations," in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 27, no. 10, pp. 2344-2353, Oct. 2019.

2. R. Fragasse et al., "Analysis of SRAM Enhancements Through Sense Amplifier Capacitive Offset Correction and Replica Self-Timing," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 6, pp. 2037-2050, June 2019.

3. Tripathi Tripti, Chauhan D. S., Singh S. K., and Singh S. V. "Implementation of Low-Power 6T SRAM Cell Using MTCMOS Technique", In Advances in Computer and Computational Sciences, Springer, Singapore, 2017.

4. M. Geetha Priya, Dr. K.Baskaran, D. Krishnaveni. "Leakage Power Reduction Techniques in Deep Submicron Technologies for VLSI Applications." ELSEVIER, International Conference on Communication Technology and System Design 2011.

5. K Sridhara, G S Biradar, Raju Yanamshetti, "Subthreshold leakage power reduction in VLSI circuits: A survey," Communication and Signal Processing (ICCSP) 2016 International Conference on, pp. 1120-1124, 2016.

6. S. Gupta, K. Gupta, B. H. Calhoun, and N. Pandey, "Low-Power Near-Threshold 10T SRAM Bit Cells with Enhanced Data-Independent Read Port Leakage for Array Augmentation in 32-nm CMOS," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 3, pp. 978-988, March 2019.

7. H. Dounavi, Y Sfikas, and Y. Tsiatouhas, "Periodic Aging Monitoring in SRAM Sense Amplifiers," 2018 IEEE 24th International Symposium on On-Line Testing And Robust System Design (IOLTS), Platja d'Aro, 2018, pp. 12-16.

8. S. Ahmad, B. Iqbal, N. Alam, and M. Hasan, "Low Leakage Fully Half-Select-Free Robust SRAM Cells with BTI Reliability Analysis," in IEEE Transactions on Device and Materials Reliability, vol. 18, no. 3, pp. 337-349, Sept. 2018.
9. B. N. K. Reddy, K. Sarangam, T. Veeraiah, and R. Cheruku, "SRAM cell with better read and write stability with Minimum area," TENCON 2019 - 2019 IEEE Region 10 Conference (TENCON), Kochi, India, 2019, pp. 2164-2167.

10. A. Surkar and V. Agarwal, "Delay and Power Analysis of Current and Voltage Sense Amplifiers for SRAM at 180nm Technology," 2019 3rd International Conference on Electronics, Communication, and Aerospace Technology (ICECA), Coimbatore, India, 2019, pp. 1371-1376.

11. Gomes Iuri A.C., Meinhardt Cristina, Butzen Paulo F. "Design of 16nm SRAM Architecture" South Symposium on Microelectronics, 2012.

12. Chakka Sri Harsha Kaushik, Rajiv Reddy Vanjarlapati, Varada Murali Krishna, Tadavarthi Gautam, V Elamaran, "VLSI design of low power SRAM architectures for FPGAs," Green Computing Communication and Electrical Engineering (ICGCCEE) 2014 International Conference on, pp. 1-4, 2014.

13. Richa Choudhary, Srinivasa Padhy, Nirmal Kumar Rout, "Enhanced Robust Architecture of Single Bit SRAM Cell using Drowsy Cache and Super cut-off CMOS Concept," International Journal of Industrial Electronics and Electrical Engineering, Volume-3, PP.63-68, July 2011.

14. Jesal P. Gajjar, Aesha S. Zala, Sandeep K. Aggarwal, "Design and Analysis of 32 bit SRAM architecture in 90nm CMOS Technology" Volume: 03, Issue: 04, Apr-2016, pp:2729-2733.

15. Shikha Saun, Hemant Kumar, "Design and performance analysis of 6T SRAM cell on different CMOS technologies with stability characterization", OP Conf. Series: Materials Science and Engineering561 (2019).

16. A. Bhaskar, "Design and analysis of low power SRAM cells," 2017 Innovations in Power and Advanced Computing Technologies (i-PACT), Vellore, 2017, pp. 1-5.

17. Yong-peng Tao, Wei-ping Hu, "Design of Sense Amplifier in the High-Speed SRAM," International Conference on Cyber-Enabled Distributed Computing and Knowledge Discovery, pp. 384-387, 2015.

18. M. Jefremow et al., "Time-differential sense amplifier for sub-80mV bit line voltage embedded STT-MRAM in 40nm CMOS," 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, San Francisco, CA, 2013, pp. 216-217.

19. Y. Tao and W. Hu, "Design of Sense Amplifier in the High-Speed SRAM," 2015 International Conference on Cyber-Enabled Distributed Computing and Knowledge Discovery, Xi'an, 2015, pp. 384-387.

20. Manoj Sinha, Steven Hsu, Atila Alvandpour, Wayne Burleson, Ram Krishnamurthy, Shekhar Borhr. "High-Performance and Low-Voltage Sense-Amplifier Techniques for sub-90nm SRAM" SOC Conference, 2003. Proceedings IEEE International [Systems-on-Chip].
21. Ravi Dutt, Abhijeet. "High-Speed Current Mode Sense Amplifier for SRAM Applications" IOSR Journal of Engineering, Vol. 2, pp: 1124-1127, 2012

22. Yiqi Wang, Fazhao Zhao, Mengxin Liu, and Zheng sheng Han, "A new full current-mode sense amplifier with compensation circuit," 2011 9th IEEE International Conference on ASIC, Xiamen, 2011, pp. 645-648.

23. Rajendra Prasad S, BK Madhavi, K Lal Kishore, "design of 32nm Forced Stack CNTFET SRAM Cell for Leakage Power Reduction", IEEE Conference on Computing, Electronics and Electrical Technologies, pp. 629-633, 2012.

24. Saxena, K. K., Srivastava, V., & Sharma, K. (2012). Calculation of Fundamental Mechanical Properties of Single Walled Carbon Nanotube Using Non-Local Elasticity. Advanced Materials Research, 383–390, 3840–3844. https://doi.org/10.4028/www.scientific.net/AMR.383-390.3840

25. Investigate the optimal combination of process parameters for EDM by using a grey relational analysis, M Tiwari, K Mausam, K Sharma, RP Singh, Procedia Materials Science 5, 1736-1744