HD OLED-on-silicon micro-display aided by high-efficient operator IP

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Abstract In order to improve the higher rate of OLED-on-Silicon Micro-display, this paper proposes a high-efficient operator strategy, which is based on the cancel of waiting time. The theory structure of high-efficient operator is proposed through the relationship between sub-field sequences and bit sequence for different gray levels. This operator is tested using the IP core and self-built HD OLED micro-display system. The experiment shows that the high-efficient operator can obtain excellent scan utilization under idle condition, compared with the traditional scan methods.

Keywords: high-efficient, scan, OLED, micro-display, digital, HD

Classification: Circuits and modules for electronics display

1. Introduction

Compared with the traditional luminescent materials, the Organic Light Emitting Diode (OLED)-on-Silicon micro-display devices, which doesn’t require the additional background-light, can deal with the large viewing size and smart device very well [1, 2, 3, 4]. With these characteristics, the OLED-on-Silicon micro-display are very suitable for the projectors and Near To Eye (NTE) system [5, 6, 7].

Based on the different strategy for OLED-on-Silicon micro-display, the scanning circuits can be roughly divided into two types: analog driving and digital driving. Meanwhile, the analog is typically consisted of DAC converters [8, 9]. This driving circuit is not efficient for the OLED-on-Silicon micro-display, and a challenging work for designing an ultra gray-levels (such as 10bit, 11bit and more) for pixels with the restrict layout [10, 11]. Considering that the luminous flux is proportional to active lighting time, the digital driving is designed to generate the gray levels through controlling the duty of the current. While the digital driving scheme makes the circuit more immune to pixel luminous and simplify the driving circuit, the key disadvantage is that the adding data-width will need the dramatically number of pixels and gray levels. This drawback will restrict the frame rate and resolution. As a result, this paper establishes the high-efficient operator as the driving scanning and exhibits the relative experiment.

2. High-efficient operator

In order to improve the digital scanning strategy, the high-efficient operator is proposed based on the relationship between sub-field sequences and gray level for larger resolution. The following section gives the vividly interpretation.

2.1 Operator theory

Traditional pixel data transmitting sequence obeys the electron beam scanning strategy: from left to right and from top to bottom [12, 13, 14]. The obvious advantage of this operation is that this strategy is suitable for current systems. All the pixels are injected into the same bit sequence and all the same bit of pixel data are transferred to the display within one field or sub-field period. Then, the waiting time between data transfer and data hold is the key factor influencing efficiency. Nevertheless, these scanning strategies aren’t essential in the digital driving for OLED-on-Silicon. Then, the scanning efficiency will be optimized if the bit scanning sequence is adjusted. An example of the high-efficient scanning sequence for 16 gray levels is illustrated in Fig. 1.

The subspace scan period \( T_s \) of the x axis indicates the data transfer or data hold period for one subspace. \( T_s \) becomes the benchmark time for high-efficient scanning instead of \( T \). Current frame \( N \) has been displayed between 0 \( T_s \) and 39 \( T_s \), though each subspace begins at different time. The y axis indicates the subspace, which is defined as a full...
partition of the whole display and always includes one or more adjacent rows. The bit scanning sequence inside one subspace follows the same regular order, for example, 8-4-2-1 order, but the bit scanning sequences between different subspaces are not necessarily the same. In fact, they are always different from each other as shown in Fig. 1. The driving circuit is responsible for switching from one subspace to any other subspace during row selecting. In the Fig. 1, the most important principle is that when the waiting time between adjacent scanning for one pixel, this strategy can scan the other pixels. In order to establish our theory, the vividly conditions can be expressed as the following:

Pre-condition 1: the scan time of each subspace in one frame can be divided into several proportional periods. The proportional factors range from the shortest one to the longest one will keep the same value for all subspaces. The number of periods within one frame is equal to the bit width, and the gray levels $G$ are equal to $2^b$.

Pre-condition 2: the matrix number of subspaces should be equal to $2^{b-1}$ to make full use of the waiting time between data transfer and data scan.

Pre-condition 3: there must be one point, and at most one point, driving one pixel during any time of the current frame.

Then, if we define one scan point as the data transfer period in one subspace. The pixel data will change its value only at the scan points, otherwise the value will be held. The total number of scan points from all the $2^{b-1}$ subspaces is equal to $b2^{b-1}$, which is defined as the time depth of the frame.

Suppose that the relationship between the scan time and the sub-field can be described by one matrix $M_b$, while the rows indicate the sub-field and the columns indicate the time. Only two elements, 0 and 1, are included in $M_b$. 1 indicates the efficient scanning of one pixel, and 0 indicates that the pixel data will be kept the same as that in the previous time. $I_n$ stands for the n-dimensional column vector which only includes the element 1.

Theorem 1: If $M_b$ is defined as the b-bit high-efficient operator, it must satisfy the below conditions:
(1) $M_b$ is one $2^{b-1} \times b2^{b-1}$ order matrices.
(2) The column sum of $M_b$ is $1_{b2^{b-1}}$.
(3) The row sum of $M_b$ is $1_{b1^{2^{b-1}}}$.
(4) Distances of two adjacent 1, in every row, can be arranged from the bigger to smaller number. The distance between the last 1 and first 1 is extended by $b2^{b-1}$ periodic extension. Then, the maximum distance is larger than $2^{b-1}$, and the minimal distance is also larger than 1.

Based on these conditions, in order to establish the high-efficient scanning structure, the sign of the transfer matrix is introduced as the following functions:

$$T_{m,n}(A_{m,n}) = \overline{A}_{m,n} \quad (1)$$

Meanwhile, the matrix $A_{m,n}$ is $(a_{ij})_{m \times n}$ and $\overline{A}_{m,n} = \overline{a}_{1m \times n}$. $a_{m \times n}$ are $m \times n$ order. They must satisfy:

$$a_{ij} = a_{m-1 \times n-j+1} \quad i = 1, 2, \Lambda, m; \quad j = 1, 2, \Lambda, n \quad (2)$$

Then, $A(m, n)$ can be defined:

$$A_{m,n} = \begin{bmatrix} a_{11} & a_{12} & \cdots & \cdots & a_{1n} \\ a_{21} & a_{22} & \cdots & \cdots & a_{2n} \\ \vdots & \vdots & \ddots & \ddots & \vdots \\ \vdots & \vdots & \ddots & \ddots & \vdots \\ a_{m1} & a_{m2} & \cdots & \cdots & a_{mn} \end{bmatrix} \quad (3)$$

According to the above analyses, the $\overline{A}_{m,n}$ is defined as the following functions:

$$\overline{A}_{m,n} = \begin{bmatrix} a_{m,n} & a_{m,n-1} & \cdots & \cdots & a_{m1} \\ a_{m-1,n} & a_{m-1,n-1} & \cdots & \cdots & a_{m-1,1} \\ \vdots & \vdots & \ddots & \ddots & \vdots \\ \vdots & \vdots & \ddots & \ddots & \vdots \\ a_{1,n} & a_{1,n-1} & \cdots & \cdots & a_{11} \end{bmatrix} \quad (4)$$

Then, in the high-efficient operator, the $(b + 1)$-bit scanning structure is defined based on the b-bit scanning structure as the following function shows:

$$M_{b+1} = \begin{bmatrix} L_{2^b} & \overline{M}_b & O_b \\ O_b & M_b \end{bmatrix} \quad (5)$$

$L_n$ is one $n \times n$ order square matrix. Then, the function can be re-defined:

$$L_{2^b} = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 1 \\ 2 & 0 & \cdots & 0 & 1 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ 2^b & 1 & 0 & \cdots & 0 & 0 \end{bmatrix} \quad (6)$$

$O_b$ stands for one $2^{b-1} \times b2^{b-1}$ order zero-matrix. The following theorem (Theorem 2) can be interpreted that the $M_{b+1}$ is the $b + 1$-bit high-efficient structure.

Theorem 2: If $M_b$ and $M_{b+1}$ are both similar to the b-bit high-efficient structure, then $M_{b+1}$, which is structured by Function (5), is the $b + 1$-bit high-efficient structure.

Prove:
(1) $M_{b+1}$ stands for one $2^b \times (b + 1)2^b$-order matrix. This satisfies the first condition in Theorem 2.
(2) $M_b$ and $M_{b+1}$ both have the similar structure. The column sum of $M_b$ is $1_{b2^{b-1}}$ and the row sum of $M_b$ is $b1_{2^{b-1}}$. According to the structure of Function (5), the column sum of $M_{b+1}$ is $1_{(b+1)2^b}$, and the row sum of $M_{b+1}$ is $(b + 1)1_{2^b}$. Then this satisfies the second and third conditions in Theorem 1.
(3) Suppose that $M_{b+1}$ still satisfies Condition (4) in Theorem 1. The same procedure as Step (2) can be used. Then $M_{b+1}$ satisfies the fourth condition in Theorem 1.

2.2 High-efficient operator

Based on Theorem 2, it is easy to establish the high-efficient scanning structure of ordinary bits. From the
1-bit scanning structure, it is obvious that $M(1) = 1$ is the 1-bit optimal high-efficient scanning structure. Then, Theorem 2 can be repeatedly used in the high-efficient scanning structure of ordinary bits:

$$M_2 = \begin{pmatrix} L_2 & M_1 \\ O_1 & O_1 \end{pmatrix} = \begin{pmatrix} 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 \end{pmatrix}$$ (7)

$$M_3 = \begin{pmatrix} L_4 & M_2 \\ O_2 & O_2 \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{pmatrix}$$ (8)

$M_4$ is an $8 \times 4$ order matrix. If the scanning time interval is used as the matrix elements, $M_b$ can be expressed by the following functions:

$$M_4 = \begin{pmatrix} L_8 & M_3 \\ O_3 & O_3 \end{pmatrix} = \begin{pmatrix} 1 & 1 & 3 & 8 & 20 \\ 3 & 1 & 8 & 20 \\ 8 & 1 & 3 & 20 \\ 8 & 3 & 1 & 20 \\ 20 & 1 & 3 & 8 \\ 20 & 3 & 1 & 8 \\ 20 & 8 & 1 & 3 \\ 20 & 8 & 3 & 1 \end{pmatrix}$$ (9)

Following these steps, $M_b$, which stands for the high-efficient structure of ordinary bits, can be established as the Fig. 2. The 4-bit is also showed in the Fig. 1.

From the function(5) and Fig. 2, we can see that the high-efficient operator is self-similarity operator. This operator is similar to the fractal model. In fact, this is a continuous one-to-one mapping from $M_b$ to $M_{b+1}$, while the ranges of $M_{b+1}$ are $\{[0, 1], [0, 1]\}$ for any value of $b$. When $b$ limits near positive infinity, the fractal model will become an infinitely partitioned self-similar structure, which is appropriate for describing the high-efficient operator with ultra high gray levels versus the limited subspace and scanning time. [15, 16, 17, 18, 19, 20].

3. Experiment and analysis

In order to evaluate the performance of the high-efficient operator, the hardware IP of this operator is designed and tested using Altera Cyclone III [21, 22, 23].

3.1 Hardware IP

To investigate the benefits of the proposed operator, this IP is designed using Verilog HDL in RTL level [24]. Table I shows the hardware overhead details in Quartus. Meanwhile, the serial signal of the scanning IP is shown in Fig. 3. The pixel-data indicates the 8-bit gray-level of pixel cell in the OLED-on-Silicon micro-display. The control signals are col.shift_ena, col.latch_ena, row.latch_ena, row.dec_ena, sel; the data signals are pixel.data, row, data. In order to test the performance of the high-efficient operator, the OLED micro-display platform is designed.

| Name                        | Parameters   |
|-----------------------------|--------------|
| Total combinational functions | 3382(LE)     |
| Dedicated logic registers   | 1551(LE)     |
| Total registers             | 1151         |
| Total Memory bits           | 172240       |

![Fig. 2. 2-bit and 3-bit high-efficient operator](image)

![Fig. 3. High-efficient operator hardware IP](image)

3.2 OLED micro-display system

![Fig. 4. Micro-display platform](image)

Fig. 4 and Fig. 5 exhibit the detailed functional block diagram for the OLED micro-display system and IP with the other modules. This scanning operator can be designed on FPGA, which is the MCU of testing platform. The OLED micro-display IC is taped out using the SMIC 0.18um technology [25, 26]. A dual-link LVDS interface,
which contains four data lines, is used [27, 28]. The Trans module changes the RGB data to the relative bits [29, 30]. All data are rearranged and stored to the SDRAM. Meanwhile, the SDRAM is used as the frame buffer. The high-efficient scanning module mainly generates the command to operate the SDRAM. The SDRAM works at READ burst mode and WRITE burst mode in order to improve read and write efficiency. The address of either the input data or the output data is increased one by one. With the scanning operator, all of the same weight bit data of the frame are read or written continuously when one time transfers. Because the pixel data are injected one by one, there still need one buffer to rearrange weight bits and transfer them to the SDRAM according to the input sequences. Meanwhile, the scanning module is used to configure the weight bits from the SDRAM under the control of the read buffer and generates the driving control signals. Fig. 6 shows the actual OLED micro-display hardware platform.

3.3 Result and analysis

Fig. 7 shows the display results using the high-efficient operator on the OLED-on-Silicon micro-display system. In Fig. 7, the Chinese characters are clearly displayed.

Besides, the scanning linearity of this operator is shown in Fig. 8(a) and can be accepted by eyes. The period between two adjacent scan points in one subspace is indicated by the number of \( T_s \), and is proportional to the gray weights. The gray weights of the direct scanning, field scanning and sub-field scanning are incremented by \((1, 2, 4, 8, \ldots)\), so the gray levels increase by the same step and show linearity of the pixel data. Otherwise, the lighting efficiency can’t reach 100% considering the data waiting time. Fig. 8(b) shows the luminance value measured by the radiance color-meter SRC-200M [31]. As shown in Fig. 8(b), the luminance value changes from 430 cd/m\(^2\) to 540 cd/m\(^2\) corresponding to pixel data ranges from 128 to 160. The measured curve is almost close to a straight line.

![Fig. 5. OLED micro-display block](image)

![Fig. 6. OLED micro-display system hardware platform](image)

![Fig. 7. OLED micro-display system](image)

![Fig. 8. Performance and luminance value](image)

Table II lists some typical display results using different digital scanning strategies under the same conditions. The key indices: gray level, scanning efficiency, linearity and frame rate, are included in Table II. While, the scanning efficiency can be calculated through Function (10):

\[
T_s = \frac{M}{2^n - 1} \times 100\%
\]
In function (10), the $M$ stands for the valid output numbers to finish the all grays levels in all the sub-fields, $n$ for the gray bit and $2^n − 1$ for the all gray levels in this frame.

From the Table II, the traditional subfield scanning strategies have lower scanning efficiency, and their frame refresh rate reduces rapidly when the subfield number increases. The $Z$ fractal scanning has better scanning efficiency, but shows a poor linearity. Although the high-efficient operators have lower scanning efficiency, and improved linearity with the sacrifice of 5.8% gray levels, the high-efficient operator can reach 122 frame rate when the pixel clock frequency is 100 MHz. In Table II, the resolution is 1920 x 1080 pixels, the pixel clock is 100 MHz.

| Table II. Different scan strategy               |
|----------------------------------------------|
| Scan strategy | Gray level | Scanning efficient | Linearity | Frame rate (HZ) |
|----------------|------------|-------------------|------------|-----------------|
| 12 subfield scan /[15] | 256/256 | 66.41% | 100% | 85 |
| 19 subfield scan /[15] | 256/256 | 83.88% | 100% | 54 |
| $Z$ fractal scan /[15] | 256/256 | 100% | 25% | 85 |
| Our method | 256/256 | 98% | 94.3% | 122 |

4. Conclusion

This paper proposes the new digital scanning operator, high-efficient operator, to satisfy the requirements of HD OLED micro-display. This paper firstly analysis the traditional scanning methods, digital scanning and analog scanning. Based on the relationship between sub-field code sequences and gray sequences for different gray levels, the high-efficient operator is proposed. Thirdly, the performance of this operator is tested on the OLED-on-Silicon micro-display hardware platform. The testing results show that the high-efficient operator is the excellent scanning operator for the HD images.

Acknowledgments

The authors would like to acknowledge the financial support of China National Natural Science Fund with No. 61674100, open funding from Key Laboratory of Advanced Display and System Applications, Shanghai Science and Technology Commission with No. 16JC140062 and No. 18JC1410402.

References

[1] B. Liu, et al.: “P-53: A novel pixel circuit providing expanded input voltage range for OLED micro-displays,” SID Symp. Dig. Tech. Pap. 48 (2017) 1438 (DOI: 10.1002/sdtp.11916).
[2] M. Yang, et al.: “A DC-DC converter applied on the OLEDs micro-display drive chip with the negative output voltage,” Optoelectronic Technology 38 (2015) 96 (DOI: 10.3969/j.issn.1005-488X.2015.02.006).
[3] H. Lu and H. Li: “A bulk-driven pixel circuit with wide data voltage range for OLED microdisplays,” IEEE International Conference on ASIC (2018) (DOI: 10.1109/ASICON.2017.8252647).
[4] B.-C. Kwak and O.-K. Kwon: “A 2822-ppi resolution pixel circuit with high luminance uniformity for OLED microdisplays,” J. Display Technol. 12 (2016) 1083 (DOI: 10.1109/JDT.2016.2593048).
[5] T. Levo: “Diffraction optics for virtual reality displays,” J. Soc. Inf. Disp. 14 (2006) 467 (DOI: 10.1889/12206112).
[6] U. Vogel, et al.: “77:1: Invited paper: Ultra-low power OLED microdisplay for extended battery life in NTE displays,” SID Symp. Dig. Tech. Pap. 48 (2017) 1125 (DOI: 10.1002/sdtp.11836).
[7] D. Lannan, et al.: “Near-eye light field displays,” ACM Siggraph Emerging Technologies (2015) (DOI: 10.1145/2503368.2503379).
[8] H. De Smet, et al.: “Design, fabrication and evaluation of a high-performance XGA VAN-LCO’s microdisplay,” Displays 23 (2002) 89 (DOI: 10.1016/S0167-9322(02)00014-8).
[9] J. Savoy, et al.: “A 12-G/S phase-calibrated CMOS digital-to-analog converter” (2007) (DOI: 10.1109/VLSC.2007.4342769).
[10] J. Genoe, et al.: “30.2 Digital PWM-driven AMOLED display on flex reducing static power consumption,” IEEE International Solid-state Circuits Conference (2014) (DOI: 10.1109/ISSCC.2014.6757524).
[11] M. Xu, et al.: “A novel OLED controller with fractal scan scheme,” Robot. Comput.-Integr. Manuf. 26 (2010) 570 (DOI: 10.1016/j.rcim.2010.08.002).
[12] Y. Ji, et al.: “Optimal scan strategy for mega-pixel and kilo-gray-level OLED-on-silicon microdisplay,” Appl. Opt. 51 (2012) 3731 (DOI: 10.1364/AO.51.003731).
[13] J. I. Yuan, et al.: “Current PWM pixel driving circuit with OLED luminescence compensation,” Yijing Yu Xianshi 31 (2016) 563 (DOI: 10.3788/YJYXS2016106.0563).
[14] Y. Ji, et al.: “A digitally driven pixel circuit with current compensation for AMOLED microdisplays,” J. Soc. Inf. Disp. 22 (2014) 465 (DOI: 10.1002/jSid.259).
[15] M. H. Xu, et al.: “Optimal scanning architecture and fractal model for flat panel display system,” Tien Tzu Hsueh Pao 34 (2006) 1376.
[16] H. O. Petgen, et al.: “Classical fractals and self-similarity” (1992) (DOI: 10.1007/978-1-4757-2172-0.2).
[17] J. Hart: Computer Display of Linear Fractal Surfaces (University of Illinois at Chicago, 1992).
[18] T. Mitsa and J. R. Alford: “An application of fractal analysis in halftoning,” J. Soc. Inf. Disp. 5 (1997) 217 (DOI: 10.1889/1.1985155).
[19] M. Xu, et al.: A Novel OLED Controller With Fractal Scan Scheme (Pergamon Press, Inc. 2010).
[20] Z. Han and W. U. Qilin: “Application study of fractal theory in mechanical transmission,” Chin. J. Mech. Eng. 29 (2016) 18.
