Memristors are two-terminal passive circuit elements that have been developed for use in non-volatile resistive random-access memory and may also be useful in neuromorphic computing. Memristors have higher endurance and faster read/write times than flash memory and can provide multi-bit data storage. However, although two-terminal memristors have demonstrated capacity for basic neural functions, synapses in the human brain outnumber neurons by more than a thousandfold, which implies that multi-terminal memristors are needed to perform complex functions such as heterosynaptic plasticity. Previous attempts to move beyond two-terminal memristors, such as the three-terminal Widrow–Hoff memristor and field-effect transistors with nanoionic gates, did not achieve memristive switching in the transistor. Here we report the experimental realization of a multi-terminal hybrid memristor and transistor (that is, a memtransistor) using polycrystalline monolayer molybdenum disulfide (MoS$_2$) in a scalable fabrication process. The two-dimensional MoS$_2$ memtransistors show gate tunability in individual resistance states by four orders of magnitude, as well as large switching ratios, high cycling endurance and long-term retention of states. In addition to conventional neural learning behaviour of long-term potentiation/depression, six-terminal MoS$_2$ memtransistors have gate-tunable heterosynaptic functionality, which is not achievable using two-terminal memristors. For example, the conductance between a pair of floating electrodes (pre- and post-synaptic neurons) is varied by a factor of about ten by applying voltage pulses to modulatory terminals. In situ scanning probe microscopy, cryogenic charge transport measurements and device modelling reveal that the bias-induced motion of MoS$_2$ defects drives resistive switching by dynamically varying Schottky barrier heights. Overall, the seamless integration of a memristor and transistor into one multi-terminal device could enable complex neuromorphic learning and the study of the physics of defect kinetics in two-dimensional materials.

Uniform polycrystalline monolayer MoS$_2$ films with an average grain size of 3–5 μm were grown by chemical vapour deposition (CVD) on SiO$_2$/Si substrates (Methods) and characterized using X-ray photoelectron, photoluminescence and Raman spectroscopies. MoS$_2$ memtransistors were fabricated in a field-effect geometry with channel lengths ($L$) and widths ($W$) varying from 5 μm to 150 μm (Fig. 1d–f). Because clean interfaces between MoS$_2$ channels and metal electrodes were found to be critical, we developed an unconventional photolithography process based on a polymethylglutarimide (PMGI) and photore sist bilayer (Methods and Extended Data Fig. 2).

At large drain bias $V_D$ in the sub-threshold regime (with gate bias, $V_G$, smaller than the threshold voltage, $V_{th}$), a typical memtransistor is in a high-resistance state (HRS) for the $V_D$ sweep from 0 V to 80 V (sweep 1) and gradually changes to a low-resistance state (LRS) (Fig. 2a). The device maintains the LRS during the sweep from 80 V to 0 V (sweep 2), is reset to the HRS during the sweep from 0 V to −80 V (sweep 3), and maintains the HRS from −80 V to 0 V (sweep 4). Thus, these devices act as LRS–HRS memtransistors. Figure 2b shows that when $V_G$ is varied from 50 V to −50 V, both the LRS and HRS resistances change by a factor of about 10$^4$ and the switching ratio ($I_{LRS}/I_{HRS}$ at $V_D = 0.5$ V) is reduced from 300 to 8 (Fig. 2e inset). Owing to the n-type MoS$_2$ channel, the forward-biased ($V_D > 0$ V) device is completely off at $V_G = −50$ V (Fig. 2c), and the reverse-biased ($V_D < 0$ V) device is insulating for a range of $V_D$ values, depending on the applied $V_G$ (Fig. 2b and Extended Data Fig. 3c). The gate leakage current ($I_{G}$) remains below 200 pA during high-$V_D$ and -$V_G$ sweeps (Extended Data Fig. 3a).

Unlike filament-based resistive switching, MoS$_2$ memtransistors do not require an electroforming process to train the device, although the switching ratio increases with increasing range of the $V_D$ sweep (Extended Data Fig. 3b). The largest switching ratio, higher than 100, was obtained from devices with $W = 100–150$ μm and $L = 5–15$ μm. These devices showed bipolar resistive switching, where reversing the bias polarity is essential to restoring the initial resistance states (Extended Data Fig. 3d, e). The hysteresis in the $I_D$–$V_D$ curves of these MoS$_2$ memtransistors is fundamentally different from the commonly reported hysteresis in the transfer characteristics ($I_D$–$V_G$ curves) of field-effect transistors (FETs), which are typically due to oxide-related traps. Instead, the $I_D$–$V_G$ curves of MoS$_2$ memtransistors in the LRS and the HRS show large shifts (about 10 V) in threshold voltage, and intersect at $V_G = V_{cross}$ (Fig. 2c). Compared to the LRS, the HRS shows up to 100 times higher resistance for $V_G < V_{cross}$ and 2 times higher field-effect mobility ($\mu$) at $V_G > V_{cross}$. Therefore, the forward-bias switching loop changes from anticlockwise (LRS to HRS) for $V_G < V_{cross}$ to clockwise (HRS to LRS) for $V_G > V_{cross}$ (Fig. 2b and Extended Data Fig. 3f).

Figure 2d shows the endurance characteristics of a MoS$_2$ memtransistor that was switched 475 times between the LRS and the HRS using full-sweep cycles. Within a subset of these cycles, $I_D$ saturates at an upper value via stretched exponentials (Extended Data Figs 3g–k, 4a). Between neighbouring subsets, $I_D$ jumps randomly to a value about 10 times smaller, followed by the same inverse exponential growth, which suggests an oxide-related trap-release process activated by large fields near the source electrode in the forward bias. This behaviour is reduced under reverse bias (Extended Data Fig. 4b), possibly owing to smaller band-bending near the drain electrode. Because the HRS and the LRS show similar transitory decays, the switching ratio (about 100) remains relatively constant (Fig. 2d). Individual resistance states measured within periods of up to 24 h show a projected retention of distinct states for timescales of the order of years (Fig. 2e and Extended Data Fig. 4e). A statistical study of 62 devices fabricated with identical geometry on a single chip showed a logarithmic normal distribution

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**LETTER**

**Multi-terminal memtransistors from polycrystalline monolayer molybdenum disulfide**

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Figure 1 | Architecture of the MoS$_2$ memtransistor. a, Optical micrograph of CVD-grown polycrystalline monolayer MoS$_2$. The darker regions indicate sparse growth of bilayer MoS$_2$, while the red features correspond to grain boundaries within monolayer MoS$_2$. b, Spatial mapping of photoluminescence intensity (wavelength, 670 nm) for the area shown in a. c, Lateral force microscopy retrace image of monolayer MoS$_2$, showing grain boundaries etched by reactive ion etching before metallization. d, Optical micrograph of an array of MoS$_2$ monolayer strips with varying width, W, etched by reactive ion etching before metallization. e, Optical micrograph of a photodiode readout corresponding to the cantilever tilt. f, Optical micrograph of an array of MoS$_2$ monolayer strips with varying channel length, L. (see Extended Data Fig. 1e for topography image). The colour bar shows the photodiode readout corresponding to the cantilever tilt.

Figure 2 | Electrical characteristics of MoS$_2$ memtransistors. a, $I_D$–$V_D$ curve (open circles) of a MoS$_2$ memtransistor ($L = 5 \mu m$, $W = 100 \mu m$) at gate bias $V_G = 10$ V. The direction of the drain bias ($V_D$) sweep 1 → 4 is indicated by coloured arrows. The sweep rate is 10 V s$^{-1}$ throughout. The solid green line represents simulated data from a memristor model (see Methods and Extended Data Fig. 7). b, $I_D$–$V_D$ curves for ten consecutive sweeps at each gate bias $V_G$ for the same device. The switching directions are shown by the curved arrows. $V_G$ was decreased for each consecutive sweep cycle. c, Transfer characteristics of a memristor at $V_D = 0.1$ V, showing a shift in threshold voltage and field-effect mobility from $V_{th} = 20$ V and $\mu \approx 0.6$ cm$^2$ V$^{-1}$ s$^{-1}$ in the HRS to $V_{th} = 10$ V and $\mu \approx 0.3$ cm$^2$ V$^{-1}$ s$^{-1}$ in LRS. The curves intersect at $V_G = V_{cross} \approx 30$ V. d, Endurance of the current (top) and $I_{LRS}/I_{HRS}$ (bottom) at $V_D = 0.5$ V in the HRS (sweep 1) and the LRS (sweep 2) for 475 consecutive sweep cycles of a memristor at $V_G = 40$ V (see Extended Data Fig. 3d–k for all $I_D$–$V_D$ curves). e, Retention of the HRS and LRS currents at $V_G = 100$ mV and $V_G = 0$ V in a 24-h period. The inset shows the gate tunability of $I_{LRS}/I_{HRS}$. f, Histogram showing the largest $I_{LRS}/I_{HRS}$ ratios of 62 distinct memtransistors ($L = 5 \mu m$, $W = 100 \mu m$). The distribution is fitted with a logarithmic normal curve with mean and variance $(\log(I_{LRS}/I_{HRS}))$ of 1.96 and 0.54, respectively.
of switching ratios (Fig. 2f). Device-to-device variability is attributed to spatial inhomogeneity in the CVD-grown MoS2 film.

Owing to its two-dimensional (2D) nature, the MoS2 channel allows the switching mechanism to be probed via in situ electrostatic force microscopy (EFM), as shown in Fig. 3a and b. The drain contact and conductive cantilever were biased independently (Extended Data Fig. 5c–f for EFM images). The dashed-line ovals show band bending near the source electrode in forward-biased HRS and LRS. The dip that appears near the drain in the top panel is a topography artefact. Dependence of the effective barrier height ($\Phi_b$) on $V_G$ extracted from variable-temperature conductivity measurements in the HRS (top) and the LRS (bottom). For $V_G = V_{FB}$, $\Phi_b$ deviates from the linear dependence on $V_G$ of the thermionic emission model. The inset shows the flat-band condition at $V_D = V_{FB} = 2\text{ V}$, $\Phi_b = 125\text{ meV}$ in the HRS and $V_{FB} = -8\text{ V}$, $\Phi_b = 80\text{ meV}$ in the LRS (see Methods and Extended Data Fig. 6). d, $I_D-V_G$ curve of an LRS–LRS MoS2 memtransistor with an approximately 1.5-nm-thick photoreist layer under the metal contact at different $V_G$ values. The direction of the $V_D$ sweep 1$\to$4 is indicated by arrows. $V_G$ was decreased between $V_D$ sweep cycles. e, Schematic showing the energy band diagram of an LRS–LRS memtransistor at the four switching stages shown in the centre. $E_{b1}$ and $E_{b2}$ are non-equilibrium quasi-Fermi levels for holes and electrons, respectively (see Methods and Extended Data Fig. 8 for details). CB and VB stand for conduction band and valence band, respectively. Purple arrows show defect migration. See Methods section ‘The switching mechanism’ for detailed description of stages i–iv.

Figure 3 | In situ measurements and switching mechanism. a, EFM phase image of a MoS2 memtransistor at $V_D = 5\text{ V}$, $V_S = 0\text{ V}$ and $V_{FB} = 0\text{ V}$ ($V_{tip}$ voltage of the EFM tip) in the forward-biased HRS. D, drain; S, source. b, Line profiles of EFM phase along the red dashed line in a for EFM images taken in the forward-biased HRS, forward-biased LRS, reverse-biased HRS and reverse-biased LRS, respectively, as shown schematically on the right (see Extended Data Fig. 5c–f for EFM images). The dashed-line ovals show band bending near the source electrode in forward-biased HRS and LRS, and near the drain in the reverse-biased LRS and HRS. The dip that appears near the drain in the top panel is a topography artefact. c, Dependence of the effective Schottky barrier height ($\Phi_b$) on $V_D$, extracted from variable-temperature conductivity measurements in the HRS (top) and the LRS (bottom). For $V_G = V_{FB}$, $\Phi_b$ deviates from the linear dependence on $V_G$ of the thermionic emission model. The inset shows the flat-band condition at $V_D = V_{FB} = 2\text{ V}$, $\Phi_b = 125\text{ meV}$ in the HRS and $V_{FB} = -8\text{ V}$, $\Phi_b = 80\text{ meV}$ in the LRS (see Methods and Extended Data Fig. 6). d, $I_D-V_G$ curve of an LRS–LRS MoS2 memtransistor with an approximately 1.5-nm-thick photoreist layer under the metal contact at different $V_G$ values. The direction of the $V_D$ sweep 1$\to$4 is indicated by arrows. $V_G$ was decreased between $V_D$ sweep cycles. e, Schematic showing the energy band diagram of an LRS–LRS memtransistor at the four switching stages shown in the centre. $E_{b1}$ and $E_{b2}$ are non-equilibrium quasi-Fermi levels for holes and electrons, respectively (see Methods and Extended Data Fig. 8 for details). CB and VB stand for conduction band and valence band, respectively. Purple arrows show defect migration. See Methods section ‘The switching mechanism’ for detailed description of stages i–iv.

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Owing to its two-dimensional (2D) nature, the MoS2 channel allows the switching mechanism to be probed via in situ electrostatic force microscopy (EFM), as shown in Fig. 3a and b. The drain contact and conductive cantilever were biased independently (Extended Data Fig. 5), while the phase shift of the cantilever was recorded as the tip traced the topography profile of the MoS2 channel and electrodes 50 nm above the surface. Because the phase shift is proportional to the square of the potential difference between the tip and the surface, the phase image provides a map of the local potential. Line profiles reveal a sharper potential drop (larger field) at the source in the forward-biased HRS compared to the forward-biased LRS, suggesting a smaller contact resistance in the HRS than in the LRS (Fig. 3b). The reverse-biased HRS also shows a larger field at the drain compared to the reverse-biased LRS, although this difference is smaller, which is consistent with the smaller switching ratio at reverse bias. Multiple line profiles confirm that the differences between the HRS and LRS electric fields are consistent along the entire channel width, despite grain-boundary-induced EFM phase variations far from the contacts (Extended Data Fig. 5g–o). Because a reverse-biased Schottky diode at the source (drain) dominates $I_D$ at $V_D > 0\text{ V}$ ($V_D < 0\text{ V}$), EFM measurements provide direct evidence that the switching from the HRS to the LRS (from the LRS to the HRS) in memtransistors is caused by the dynamic tuning of Schottky barriers. Using charge-transport measurements with variable temperature ($T$) and assuming a 2D thermionic emission model, the effective barrier heights ($\Phi_b$) in different states are extracted from the slope of $\ln(I_D/T^{3/2})$ versus $1/T$ at different $V_G$ values (Extended Data Fig. 6). Thermionic emission dominates at $V_G < V_{FB}$ (flat-band voltage), producing $\Phi_b$ values that vary linearly with $V_G$. Thermally assisted tunnelling through a deformed Schottky barrier begins to contribute to $I_D$ at $V_G > V_{FB}$, resulting in deviation from the linear trend (Fig. 3c). Thus, the Schottky barrier height ($\Phi_b = \Phi_b$) is extracted from the relationship $V_G = V_{FB}$. $V_{FB}$ decreases from 2 $\text{ V}$ (HRS) to $-8\text{ V}$ (LRS), which is consistent with a $V_G$ shift of 15 $\text{ V}$ for the same device (Extended Data Fig. 6). In addition, $\Phi_b$ decreases from 125$m\text{ meV}$ (HRS) to 80$m\text{ meV}$ (LRS), confirming the EFM observations.

Charge transport in MoS2 LRS–HRS memtransistors can be described by Schottky barrier transistors (equations 1 and 2), where $\Phi_b$ is a function of an internal state variable ($w$) defined as the width of the region with excess dopants ($\Delta n$) (Extended Data Fig. 7a). Tuning the Schottky barrier through increased doping near contacts ($\Phi_b = \sqrt{\text{w}}\Delta n$) is a standard practice in conventional FETs. Similarly, we propose that defects in MoS2 act as dopants and their local migration under an applied bias is facilitated by grain boundaries, as previously observed using transmission electron microscopy and explained by ab initio calculations. Thus, we develop a memtransistor model in which $\Phi_b$ changes by image charge lowering and tunnelling at high biases (see Methods), resulting in the following coupled equations:

$$I_D = D\exp \left[ \frac{e(V_G - V_{FB})}{e_k T} \right] \left[ 1 - \exp \left( -\frac{e V_D}{k T} \right) \right] \exp \left[ \frac{\Phi_b(w)}{k T} \right]$$ (1)
where $A$, $D$, $E$ and $\phi_{b0}$ are fitting parameters, and $e$, $n$, $\varepsilon_s$ and $k_b$ are the charge of the electron, the doping level, the dielectric constant of monolayer MoS$_2$ and the Boltzmann constant, respectively. Equation (3) describes the nonlinear kinetics of the dopants near the contacts using a window function, where the degree of nonlinearity is defined by a positive integer $p (p = 4$ in Fig. 2a; see Methods)$^{29}$. This model agrees well with the experimental data (Fig. 2a and Extended Data Fig. 7) and helps establish that the dependence of $w$ on $V_C$ (through $I_D$) is the most important feature of the MoS$_2$ memristor, distinguishing it from a two-terminal memistor$^{17}$. To further illustrate this non-trivial switching mode, we fabricated MoS$_2$ devices without the PMGI-based process and used a residual photoresist layer about 1.5 nm thick as a tunnelling barrier between MoS$_2$ and the metal contacts (Fig. 3d, e and Extended Data Fig. 8). The tunnelling barrier minimizes pinning of the Fermi level and causes the resistance states to change abruptly upon crossing the 0 V level, resulting in LRS–LRS memristors. Overall, the switching mechanism of both LRS–HRS and LRS–LRS memristors can be described by two memristors at the contacts connected by a FET (see Methods section 'The switching mechanism' and Extended Data Fig. 8e).

While grain boundaries in polycrystalline MoS$_2$ memristors enable large switching ratios and prevent electrical breakdown by lowering Schottky barriers through dynamic defect migration, control devices without grain boundaries on single grains of CVD-grown MoS$_2$ show a qualitatively different, reversible breakdown phenomenon (Fig. 4a). This breakdown is marked by a sharp drop in the conductance at a voltage $V_B$ during sweep 1, with a subsequent increase to the original conductance value during sweep 2. This abrupt change in charge transport is accompanied by the emergence of dendritic features (about 300–500 nm in length) close to the source electrode (upper inset in Fig. 4a and Extended Data Fig. 9a, b). Control devices reveal a linear correlation of the breakdown current ($I_B$) with the width of the source electrode ($W_x$) and no correlation with $L$ (lower inset in Fig. 4a and Extended Data Fig. 9f–j). Because $I_B$ is normally proportional to $W/L$, the observed deviation from this relationship at breakdown suggests that the reverse-biased Schottky diode at the source electrode creates a bottleneck for electron injection at the channel$^{27}$, ultimately causing electromigration at the source contact. This reversible breakdown in CVD-grown MoS$_2$ differs from the irreversible breakdown induced in exfoliated MoS$_2$ by Joule heating$^{28}$. In the high-bias limit ($\pm 120$ V), polycrystalline MoS$_2$ memristors also degrade irreversibly in a manner that shows light emission in each subsequent sweep (Extended Data Fig. 9c–e).

The 2D planar geometry of the MoS$_2$ memristor allows the realization of multi-terminal neural circuits that mimic multiple synaptic connections in neurons. For example, in a six-terminal memristor, the conductance between any two of the four inner electrodes can be modulated by high-bias pulses applied to the two outer electrodes while the inner electrodes are disconnected (Fig. 4b and Extended Data Fig. 10). To achieve heterosynaptic plasticity, the conductance between pre-synaptic and post-synaptic neurons should be controlled by additional modulatory terminals$^{30}$. While this type of modulation has been demonstrated previously in Ag-based cationic memristors, this design is limited to only three terminals, owing to the requirement of filament formation across the channel$^{6,30}$. In contrast, the MoS$_2$ memristor can have a larger number of terminals and allows facile tuning through the modulation of the local Schottky barrier at each terminal (see Methods section ‘The switching mechanism’). Multi-terminal memristors also allow further tuning of heterosynaptic plasticity through a gate electrode, in which the switching ratio for any pair of side electrodes can be increased by about two to ten times by varying $V_G$ from 50 V to 20 V (Extended Data Fig. 10f).

MoS$_2$ memristors also demonstrate long-term potentiation and depression, which mimic excitatory and inhibitory synapses in organisms (Fig. 4c). The post-synaptic current is shown to increase and decrease exponentially with the repetition of positive- and negative-bias pulses of 1 ms (Fig. 4c). The linearity of the pulse train is comparable to that of metal-oxide memristors and can be further improved by employing bipolar pulsing schemes$^{1,13}$. By mimicking indirect spike-timing-dependent plasticity, paired pulses separated by a time interval induce positive and negative changes in the synaptic weight using positive and negative pulses (Fig. 4d), resulting in time constants of about 2 ms and 6 ms, respectively, which are comparable to the response times of biological synapses$^{1,12}$. In conclusion, MoS$_2$ memristors combine resistive switching with transistor gating to realize nonlinear charge transport with wide...
tunability of individual states and switching ratios. In contrast to conventional devices that require single-crystal MoS2 flakes, the utilization of polycrystalline and all-surface MoS2 films allows the straightforward scaling of this technology to large-area integrated circuits and post-growth defect engineering. The 2D planar geometry of monolayer MoS2 further enables the realization of multi-terminal memtransistors with unprecedented heterosynaptic plasticity. This technology may enable complex learning from multiple inputs in neuromorphic computing by mimicking biological neurons with multiple synapses.

Online Content Methods, along with any additional Extended Data display items and Source Data, are available in the online version of the paper; references unique to these sections appear only in the online paper.

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1. Strukov, D. B., Snider, G. S., Stewart, D. R. & Williams, R. S. The missing memristor found. Nature 453, 80–83 (2008); corrigendum 459, 1154 (2009).
2. Yang, J. J. et al. Memristive switching mechanism for metal/oxide/metal nanodevices. Nat. Nanotechnol. 3, 429–433 (2008).
3. Kuzum, D., Yu, S. & Wong, H. S. P. Synaptic electronics: materials, devices, and applications. Nanotechnology 24, 382001 (2013).
4. Yu, S. & Chen, P. Y. Emerging memory technologies: recent trends and prospects. IEEE Sol. Stat. Circuit Mag. 8, 43–56 (2016).
5. Yang, J. J., Strukov, D. B. & Stewart, D. R. Memristive devices for computing. Nat. Nanotechnol. 8, 12–24 (2013).
6. Waser, R., Dittmann, R., Staikov, G. & Szot, K. Redox-based resistive switching memories – nanionic mechanisms, prospects, and challenges. Adv. Mater. 21, 2632–2663 (2009).
7. Pershin, Y. V. & Di Ventra, M. Memory effects in complex materials and nanoscale systems. Adv. Phys. 60, 145–227 (2011).
8. Wong, H. S. P. et al. Metal-oxide RAM. Proc. IEEE 100, 1951–1970 (2012).
9. Thomas, A. Memristor-based neural networks. J. Phys. D 46, 093001 (2013).
10. Indiveri, G. et al. Integration of nanoscale memristor synapses in neuromorphic computing architectures. Nanotechnology 24, 384010 (2013).
11. Jo, S. H. et al. Nanoscale memristor device as synapse in neuromorphic systems. Nano Lett. 10, 1297–1301 (2010).
12. Kim, S. et al. Pattern recognition using carbon nanotube synaptic transistors with an adjustable weight update protocol. ACS Nano 11, 2814–2822 (2017).
13. Kim, S. et al. Experimental demonstration of a second-order memristor and its ability to bioelectrically implement synaptic plasticity. Nano Lett. 15, 2203–2211 (2015).
14. Widrow, B. An Adaptive Adaline Neuron using Chemical Memristors. Technical Report 1553–2 www-isl.stanford.edu/~widrow/papers/t1960anadaptive.pdf (Stanford Electronics Laboratories, 1960).
15. Lai, Q. et al. Ionic/electronic hybrid materials integrated in a synaptic transistor with signal processing and learning functions. Adv. Mater. 22, 2448–2453 (2010).
16. Diorio, C., Hasler, P., Minch, A. & Mead, C. A. Single-transistor silicon synapse. IEEE Trans. Electron Dev. 43, 1972–1980 (1996).
17. Mouttet, B. Memristive systems analysis of 3-terminal devices. In IEEE Int. Conf. on Electronics, Circuits and Systems 930–933 (IEEE, 2010).
18. Azizi, A. et al. Dislocation motion and grain boundary migration in two-dimensional tungsten disulphide. Nat. Commun. 5, 4867 (2014).
19. Komsa, H.-P. et al. From point to extended defects in two-dimensional MoS2: Evolution of atomic structure under electron irradiation. Phys. Rev. B 88, 035301 (2013).
20. Sangwan, V. K. et al. Gate-tunable memristive phenomena mediated by grain boundaries in single-layer MoS2. Nano Lett. 15, 403–406 (2015).
21. Yu, G. Z., Zhang, Y.-W. & Yakobson, B. I. An anomalous formation pathway for dislocation-sulfur vacancy complexes in polycrystalline monolayer MoS2. Nano Lett. 15, 6855–6861 (2015).
22. Bessonov, A. A. et al. Layered memristive and memcapacitive switches for printable electronics. Nat. Mater. 14, 199–204 (2015).
23. He, G. et al. Thermally assisted nonvolatile memory in monolayer MoS2 transistors. Nano Lett. 16, 6445–6451 (2016).
24. Apkarian, A. J. et al. Memristive systems analysis of 3-terminal devices via hysteresis engineering in MoS2 transistors. ACS Nano 11, 3110–3118 (2017).
25. Chua, L. Resistance switching memories are memristors. Appl. Phys., A Mater. Sci. Process. 102, 765–782 (2010).
26. Shannon, J. M. Control of Schottky barrier height using highly doped surface layers. Solid-State Electron. 19, 537–543 (1976).
27. Sze, S. M. & Ng, K. K. Physics of Semiconductor Devices (Wiley-Interscience, 2006).
28. Hemberger, M., Papavassiliou, G. & Toumazou, C. A versatile memristor model with nonlinear dopant kinetics. IEEE Trans. Electron Dev. 58, 3099–3105 (2011).
29. Lemble, D. & Kis, A. Breakdown of high-performance monolayer MoS2 transistors. ACS Nano 6, 10171–10179 (2012).
30. Yang, Y., Chen, B. & Lu, W. D. Memristive physically evolving networks enabling the emulation of heterosynaptic plasticity. Adv. Mater. 27, 7720–7727 (2015).
31. Wang, L. T. et al. 3D Ta2O5/TiO2/Ti synaptic array and linearity tuning of weight update for hardware neural network applications. Nanotechnology 27, 365204 (2016).
32. Bi, G.-Q. & Poo, M.-M. Synaptic modifications in cultured hippocampal neurons: dependence on spike timing, synaptic strength, and postsynaptic cell type. J. Neurosci. 18, 10464–10472 (1998).

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Author Contributions V.K.S., H.-S.L. and M.C.H. conceived the idea and designed the experiments. V.K.S. and H.-S.L. fabricated all the devices and performed measurements and analysis. H.B. and I.B. handled the growth of MoS2 and conducted materials characterization. V.K.S. developed the memtransistor model. M.E.B. assisted in model fitting and device fabrication. K.-S.C. assisted in electrostatic force microscopy. All authors wrote the manuscript and discussed the results at all stages.

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METHODS

CVD of MoS₂ film. Polycrystalline monolayer MoS₂ with continuous film coverage was directly grown on oxidized Si substrates by CVD using sulfur powder (Sigma-Aldrich) and molybdhenum trioxide powder (MoO₃, 99.98% trace metal, Sigma-Aldrich) following the procedure reported earlier. Prior to growth, Si substrates were bath-saturated for 10 min in acetone and isopropyl alcohol and subsequently cleaned under O₂ plasma (Harrick Plasma) at about 200 mTorr for 2 min with 10.2 W power applied to the radiofrequency coil. The substrates were placed in a chamber of 12 mg of MoO₃ powder in an N₂:H₂ (1:1) mixture in a 1-inch-diameter quartz tube furnace (Lindborg/Blue). 150 mg of sulfur powder in an alumina boat was placed about 30 cm upstream of the MoO₃ boat (outside the furnace) and was heated independently using a temperature-controlled heating belt. The tube furnace was purged using ultrahigh-purity Ar gas at 200 standard cubic centimetres per minute (sccm) for 10 min. Then, the pressure was increased to 400 Torr, and the tube was evacuated to its base pressure of about 60 mTorr. The purging process was repeated twice to achieve an inert growth environment. The pressure was kept at 150 Torr with a 25-sccm flow of Ar gas during growth and cooling. After the purge process, the furnace was heated to 150 °C for 5 min and held at that temperature for 20 min to remove physisorbed contaminants from the growth environment. The furnace was then heated to 800 °C at a rate of 12 °C min⁻¹ and held at that temperature for 20 min, followed by natural cooling to room temperature. Concurrently, the heating belt around the sulfur boat was first ramped to 50 °C for 5 min and was held at that temperature for 49 min. The heating belt was then brought to 150 °C at a rate of 4.5 °C min⁻¹ and held at that temperature for an additional 23 min, after which it was allowed to cool to room temperature naturally.

Chemical characterization of monolayer MoS₂ film. The coverage and growth quality of continuous polycrystalline monolayer CVD-grown MoS₂ on 5 mm × 5 mm Si substrates were characterized by optical microscopy, Raman microscopy, and photoluminescence spectroscopy. Raman spectra collected with a Horiba Scientific XploRA PLUS Raman microscope (Extended Data Fig. 1a) show a peak spacing of about 19 cm⁻¹ between the in-plane A₁g and the out-of-plane E₂g breathing modes, thus confirming the growth of monolayer MoS₂. Photoluminescence spectroscopy (Extended Data Fig. 1b) shows a dominant exciton A at 673 nm, typical of CVD-grown monolayer MoS₂ on SiO₂. The chemical composition of CVD-grown polycrystalline monolayer MoS₂ films was confirmed by X-ray photoelectron spectroscopy (XPS) measurements using a Thermo Scientific ESCA Laboratory 250Xi XPS instrument connected with a monochromatic Kα AlX-ray line. The X-ray beam size was approximately 900 μm in diameter with an elliptical cross-section. A charge-neutralization Ar⁺ ion flood gun was also used to compensate for local electrostatic fields arising from charge buildup in the MoS₂/SiO₂ samples. All XPS spectra were analysed using Avantage software (Thermo Scientific). All Mo 3d subpeaks were fitted using the Gauss–Lorentzian mixing and modified Shirley background subtraction. Fitting of Mo 3d subpeaks ensured that their full-width at half-maximum values were lower than 3 eV, and doublets were also constrained to have the same full-width at half-maximum. In the XPS spectra analysis, charging effects were compensated by correcting all spectra against the C 1s full-width at half-maximum. In the XPS spectra analysis, charging effects were compensated by correcting all spectra against the C 1s full-width at half-maximum. In the XPS spectra analysis, charging effects were compensated by correcting all spectra against the C 1s full-width at half-maximum. In the XPS spectra analysis, charging effects were compensated by correcting all spectra against the C 1s full-width at half-maximum. In the XPS spectra analysis, charging effects were compensated by correcting all spectra against the C 1s full-width at half-maximum. In the XPS spectra analysis, charging effects were compensated by correcting all spectra against the C 1s full-width at half-maximum. In the XPS spectra analysis, charging effects were compensated by correcting all spectra against the C 1s full-width at half-maximum. In the XPS spectra analysis, charging effects were compensated by correcting all spectra against the C 1s full-width at half-maximum. In the XPS spectra analysis, charging effects were compensated by correcting all spectra against the C 1s full-width at half-maximum.

Scanning probe microscopy. The CVD-grown MoS₂ films were characterized by atomic force microscopy (AFM) in ambient conditions using an Asylum Cypher AFM system in lateral force microscopy (LFM) mode and tapping mode. For LFM, NanoWorld FMR cantilevers with a resonance frequency of about 75 kHz and contact force of approximately 5 nN were used (Fig. 1c). The LFM retrace image was acquired by scanning the tip from right to left with a contact force of about 1 nN. For tapping mode, NanoWorld NCHR-W Si cantilevers (resonance frequency of about 320 kHz) were used (Extended Data Fig. 1e, f). A step height of 0.73 nm at the edge of a MoS₂ flake confirmed monolayer thickness. AFM measurements of individual flake devices after electrical breakdown (upper inset in Fig. 4a and Extended Data Fig. 9) were conducted in the tapping mode using a Bruker Dimension FastScan AFM system. EFM of MoS₂ memristors was conducted in ambient conditions using the environment cell of the Asylum Cypher AFM system and NanoWorld PointProbe EFM tips coated with PtIr (resonance frequency of about 75 kHz).

Fabrication of MoS₂ memristors. MoS₂ LRS–HRS memristors were fabricated following a photolithography process developed to minimize processing residues. First, a PMGI film was spin-coated on Si/SiO₂ substrates covered by polycrystalline monolayer MoS₂ at 4500 rpm for 45 s, followed by baking at 170 °C for 10 min using a hot plate. Note that the baking conditions for the PMGI layer were found to be critical. Lower temperature (160 °C) resulted in delamination during development, while higher temperature (180 °C) made it difficult to remove PMGI during the lift-off step. Afterwards, a thin film of photore sist (S1813, Shipley Company) was spin-coated at 4000 rpm for 1 min followed by another prebaking step at 115 °C for 1 min. The bilayer resist was exposed to ultraviolet light (365 nm) for 15 s and then developed in MF319 developer (Shipley Company) for 20 s without post-baking. The samples were rinsed with deionized water and thoroughly dried before subjecting them to reactive ion etching to pattern the exposed MoS₂ film. The MoS₂ film was etched using Ar at a power of 100 mTorr and flow rate of 50 sccm for 20 s. Subsequently, the bilayer resist mask was removed by submerging the substrate overnight in an N-methyl-2-pyrrolidone (NMP) bath heated at 80 °C. At this stage, the patterned MoS₂ strips resembled the optical image shown in Fig. 1e. Finally, source and drain electrodes were fabricated by patterning a negative photoresist NR9-1000PY (Futurrex, Inc.), followed by thermal evaporation of metals (3 nm Ti and 50 nm Au) and lift-off in NMP. The MoS₂ LRS–LRS memristors were fabricated using the same process, but without a PMGI layer.

Electrical measurements. All room-temperature electrical measurements were carried out in a vacuum probe station at a pressure of about 5 × 10⁻⁵ Torr in the dark using a LakeShore CRX 4K probe station. Endurance, retention and neural learning tests were conducted in vacuum using pulse measure units in a Keithley 4200A-SCS Parameter Analyser and home-built LabVIEW programs. For the variable-temperature transport measurements, the devices were first switched to the HRS, and the I₉–W₀ data were collected at V₉ = 0.1 V from 300 K to 75 K at a scan rate of 25 K. A pressure of 8 × 10⁻⁷ Torr was achieved during cryogenic measurements using a built-in cryopump. The devices were allowed to heat up to room temperature overnight and were then switched to the 2D model at room temperature, followed by similar variable-temperature transport measurements in the LRS. In the sub-threshold regime, the charge transport in Schottky-barrier FETs (SB-FETs) is dominated by thermionic emission.

LETTER
edge (Extended Data Fig. 9a) changes the maximum electric field \( E_{\text{max}} \) (and the effective Schottky barrier height \( \Delta \phi_{\text{image}} \)) by image charge lowering\(^{27} \) as:

\[
\Delta \phi_{\text{image}} = \frac{e}{4 \pi \varepsilon_s} \frac{m n_1}{d^2} \frac{d}{w} \approx \frac{m n_1}{4 \pi \varepsilon_s} \]

where \( d \) is the depletion width, \( n_1 \) is the net excess density near the contact, \( n \) is the dopant density in the channel away from the contacts and \( \Delta n = n_1 - n \), as defined in Extended Data Fig. 7a. In the case of a 2D semiconductor, the metal image plane is cut by half, and thus equation (8) for a bulk semiconductor changes only by a factor of 2, which is neglected here because \( n_1 \) is a fitting parameter. However, the lowering of the image charge also depends on the drain bias \( V_D \) and the gate bias \( V_G \), and cannot be neglected at large biases. As shown previously\(^{27,40} \), the easiest way to incorporate a high-bias scenario is through the geometrical factors \( A \) and \( B \), which results in:

\[
\Delta \phi_{\text{image}} = \frac{c \varepsilon_{\text{ox}}}{4 \pi \varepsilon_s} = \frac{c \varepsilon_{\text{ox}}}{4 \pi \varepsilon_s} \left[ \frac{B(V_G - V_D)}{t_{\text{ox}}} + \frac{2\varepsilon_{\text{ox}}(\phi_{\text{bs}} + A V_D)}{e_s} \right] \]

where \( \varepsilon_{\text{ox}} \) is the thickness of the oxide dielectric. Furthermore, at high biases, tunnelling cannot be neglected and its main features can be described by the following expression\(^{40} \):

\[
\Delta \Phi_{\text{tunnel}} = \frac{1}{4 \pi \varepsilon_s} \frac{3 \varepsilon_0 (\ln 2)^{2/3}}{2^{2/3}} \left( \frac{B(V_G - V_D)}{t_{\text{ox}}} \right)^{2/3} \]

where \( m^* \) is the effective mass and \( h \) is the Planck constant. The net change in effective barrier height \( \Delta \Phi \) can be determined by adding equations (8), (9) and (10) to obtain

\[
\Delta \Phi = \Delta \phi_{\text{image}} + \Delta \phi_{\text{image}} + \Delta \phi_{\text{tunnel}}
\]

A dynamically varying barrier changes the transistor’s \( I_D \)–\( V_D \) curve to yield a pinched hysteresis loop. Because the memristive switching ratio is largest in the sub-threshold regime (Fig. 2b), we take the following expression for the \( I_D \)–\( V_D \) relationship of SB-FETs\(^{40} \):

\[
I_D = \left[ \frac{e(V_G - V_D)}{c_\text{k} kT} \right] \left[ 1 - \exp \left( \frac{-eV_D}{c_\text{k} kT} \right) \right]
\]

where the first exponential term gives a straight line in the logarithmic–linear plot of \( I_D \) vs. \( V_D \) (Fig. 2c) and the corresponding (sub-threshold) slope is given by 2.3\( \frac{kT}{c_\text{k} kT} \). The second exponential term of equation (13) is responsible for the large asymmetry observed in the high-bias curve (Fig. 2a). The second term becomes negligible for \( V_D > 2kT \), and thus the forward-bias current saturates quickly with increasing \( V_D \) (Fig. 2b). Because the variable-temperature conductivity fits well to the thermionic emission model (Fig. 3c) in the sub-threshold regime (\( V_D < V_G \)), we obtain the equation of the voltage-controlled memristor by multiplying equation (13) with the barrier height term from the thermionic equation (4):

\[
I_D = \sum \exp \left( \frac{e(V_G - V_D)}{c_\text{k} kT} \right) \left[ 1 - \exp \left( \frac{-eV_D}{c_\text{k} kT} \right) \right]
\]

where \( \phi_b = \phi_b - \Delta \Phi \), as shown schematically in Extended Data Fig. 7a, and \( \phi_{bs} \) and \( \phi_b \) are the effective barrier heights before and after image lowering by \( \Delta \Phi \), respectively. For \( V_D > 0 \), \( V_D \) at the source is reverse biased and acts as a bottleneck for the device current, whereas, for \( V_D < 0 \), the Schottky diode at the drain is reverse biased. Therefore, dopant redistribution at the two different contacts dominates in the positive and negative bias regimes, and the device can be visualized as two memristors connected by a transistor (Extended Data Fig. 8e). Local electrostatics at the contacts is inherently asymmetric at large positive and large negative \( V_D \) values because \( V_D - V_G < 0 \) at the source for \( V_D > 0 \) (we note that \( V_G = V_D \) for \( V_D \), \( V_D > 0 \) at the drain for \( V_D < 0 \) in the most relevant regime of \( V_G < 0 \) and \( |V_D| > |V_G| \)). In other words, the Fermi level of MoS\(_2\) is located deeper into the bandgap at the source in the forward bias than at the drain in the reverse bias. Because both \( V_D \) and \( V_G \) define the Schottky barrier modulation, we need two different sets of equations for the source and drain in the forward and reverse biases. Neglecting the gate leakage current \( I_G \) (Extended Data Fig. 3a), we modify equation (6) to get equations (15), where the only differences between functions \( f \) and \( g \) and between \( h \) and \( j \) are the fitting parameters.

\[
\frac{\partial w}{\partial t} = f(w_s, V_D, V_G, t)
\]

\[
\frac{\partial w}{\partial t} = g(w_s, V_D, V_G, t)
\]

\[
I_D = \sum \left[ \frac{h(w_s, V_D, V_G, t)}{j(w_s, V_D, V_G, t)} \right] \text{for } V_D \geq 0
\]

\[
I_G = 0
\]

Dynamic redistribution of dopants under bias is usually governed by drift motion. Consequently, physical models of memristors often require a nonlinear drift with the field to keep the state variable \( w \) within the boundary conditions. Dopant drift is greatly suppressed as it approaches the dimension of the device on either side, thereby avoiding irreversible hard switching or breakdown. The nonlinearity of dopant drift is usually modelled by a window function \( F(w) \), and thus we obtain:

\[
\frac{\partial w}{\partial t} = \mu F(w) \left[ v_d ^0 \right] F(w)
\]

where \( d \) is the range of dopant drift, \( \mu \) is the dopant mobility, \( I(t) \) is the current as defined in equation (5) and \( R_{\text{on}} \) is the resistance of the device when \( w \) spans the whole range \( d \). The window function\(^{16} \):

\[
F(w) = 1 - \left( \frac{w - 0.5 \mu T}{0.75 \mu T} \right)^2
\]

has reproduced bipolar resistive switching in a wide range of metal-oxide memristors. It should be noted that larger \( \mu \) values imply larger nonlinearity. Thus, by taking \( \Delta n \approx \Delta n \) for large modulation in dopant density, we combine equations (12), (14), (15) and (17) to get the following set of equations for \( V_D \geq 0 \):

\[
I_D = \sum \exp \left( \frac{e(V_G - V_D)}{c_\text{k} kT} \right) \left[ 1 - \exp \left( \frac{-eV_D}{c_\text{k} kT} \right) \right]
\]

\[
\frac{\partial w}{\partial t} = \sum \left[ \frac{h(w_s, V_D, V_G, t)}{j(w_s, V_D, V_G, t)} \right] \text{for } V_D \geq 0
\]

Equation (20) describes the drain bias sweep, and \( A, D, E \) and \( \Delta n \) are fitting parameters. The parameter \( p = 4 \) provides sufficient non-linearity. The geometrical factor \( c_\text{k} kT \) has a role similar to that of \( c_\text{k} kT \) and limits the exponentially growing current at high negative biases. Here, we first focus on fitting the \( I_D \)–\( V_D \) curve for a fixed \( V_G \); therefore, the terms involving the geometrical factor \( B \) in equation (12) are absorbed in the fitting parameter \( D \). Similarity, the following set of equations describes the behaviour of the memristor for \( V_D < 0 \):

\[
I_D = \sum \exp \left( \frac{e(V_G - V_D)}{c_\text{k} kT} \right) \left[ 1 - \exp \left( \frac{-eV_D}{c_\text{k} kT} \right) \right]
\]

\[
\frac{\partial w}{\partial t} = \sum \left[ \frac{h(w_s, V_D, V_G, t)}{j(w_s, V_D, V_G, t)} \right] \text{for } V_D < 0
\]
where a different set of fitting parameters, $A'$, $D'$, and $E'$, is needed owing to asymmetric electrostatics and dopant kinetics.

The experimental memristor characteristics are fitted well with this model, as shown in Fig. 2a. Extended Data Fig. 7b and c shows the dynamic modulation of $w_I$ and $w_r$ with $V_G$. The experimental values $c_2 = 83.3$ and $c_3 = 20$ were used in addition to the constants $\phi_m = 385$ meV and $\epsilon_r = 4$ for monolayer MoS$_2$. The fitting parameters in Fig. 2a are $A = 10^{-5}$, $D = 5.5 	imes 10^{-10}$ and $E = 7 	imes 10^{-10}$. We note that although we treat $w$ and $\Delta n$ independently in the mathematical formalism, we cannot measure them independently. Thus, we treat the product $w_\Delta n$ as an internal state variable. For the fitting in Fig. 2a, we get $w_\Delta n < 10^{-6}$ cm$^{-2}$ and $w_\Delta n < 3.5 \times 10^{-6}$ cm$^{-2}$ in order to get Schottky barrier heights covering the entire range of the experimental values (80–125 meV) shown in Fig. 3c (in the model, $\Delta n$ has units of cm$^{-1}$). The fitting in Fig. 2a results in effective Schottky barrier heights ranging from 20 meV to 280 meV in the LRS and the HRS, respectively. Thus, overestimation of the simulated values in the HRS and underestimation in the LRS could result from non-idealities in the transistor transport model at high biases. Assuming that $w$ is of the order of a few nanometers, we get maximum excess doping of $\Delta n \approx 10^{10}$ cm$^{-2}$, which is within the range of previous measurements of doping from MoS$_2$ defects.

The smaller value of $w_\Delta n$ compared to $w_\Delta n$ results from the smaller fields at the drain for $V_D > 0$ than at the source for $V_S > 0$, which is consistent with the smaller hysteretic loop in the reverse bias. We note that although the net device current ($I_D$) is determined by $w_I$ for $V_D > 0$ and by $w_r$ for $V_S < 0$, for the device to exhibit reversible behaviour, $w_\Delta n$ must return to its initial value when $V_D > 0$ ($V_S < 0$). This is achieved by setting appropriate fitting parameters $D$, $E$ ($D'$, $E'$). In real devices, a large electric field near forward-biased Schottky diodes and redistribution of dopants to the initial configuration are also expected. Finally, by considering the first exponential term in equations (18) and (21), which contains $V_G$, we simulate the gate tunability of memristor characteristics that is consistent with the observed experimental behaviour (Extended Data Fig. 7d, e). Deviations between simulations and experiments become larger at larger $V_G$ values owing to the decreased validity of the SB-FET model beyond the sub-threshold regime.

The switching mechanism. The switching mechanism of MoS$_2$ memristors can be understood by assuming two memristors at the source (S-memristor) and the drain (D-memristor) that are connected by a FET (Extended Data Fig. 8e). We note that gate-tunable resistive switching cannot be obtained by simply connecting two conventional memristors with a transistor. The Schottky barrier height modulation is closely connected to the operation of the SB-FET in the MoS$_2$ memristor. Thus, this distinction between memristor and transistor only serves to specify the switching mechanism. MoS$_2$ memristors with residue-free interfaces between the metal and MoS$_2$ (Fig. 2) undergo HRS-to-LRS switching at positive bias and LRS-to-HRS switching in negative bias and are called LRS–HRS memristors here. MoS$_2$ memristors with an approximately 1.5-nm-thick polymer tunnel barrier between the metal and MoS$_2$ (Extended Data Fig. 8a–d) undergo similar HRS-to-LRS switching at both positive and negative biases and are called LRS–LRS memristors. The main difference between the two types is that the LRS–HRS memristor retains its state while crossing 0 V level, whereas LRS–LRS memristors undergo switching while crossing 0 V (Figs 2b, 3d). Both of these contrasting behaviours can be explained by the resistance table in Extended Data Fig. 8e. HD and LD are the resistance values of the HRS and LRS of the D-memristor, whereas HS and LS are the resistance values of the HRS and LRS of the S-memristor, respectively. We have HD $>$ LD and HS $>$ LS for both kinds of memristors, and their relative amplitudes determine the switching ratio. LD' and LS' are intermediate states with resistance values that differ vastly for LRS–HRS and LRS–LRS memristors.

For LRS–HRS memristors, switching events A and B dominate, while switching event C is negligible (Extended Data Fig. 8e). Switching A occurs at the bottleneck contact (that is, the source for forward bias and the drain for reverse bias), while switching B occurs at the other contact in order to restore the dopant distribution at the end of a full sweep cycle. This condition is necessitated by bipolar resistive switching, and its physical origin is well explained by the memristor model. Thus, intermediate states LD and LS' have resistance values close to LD and LS, respectively.

On the other hand, for LRS–LRS memristors, all switching events A, B, and C appear. The resist layer acts at a tunnel barrier that minimizes pinning of the Fermi level of MoS$_2$. Similar minimization of the Fermi level has been shown in MoS$_2$ by employing ultrathin tunnel barriers, such as 2 nm MgO (ref. 35), 1 nm TiO$_2$ (ref. 52), 1.5 nm Ta$_2$O$_5$ (ref. 53) and 0.6 nm hexagonal boron nitride$^{34}$, resulting in reduction of the effective Schottky barrier height from 100 meV to 23 meV, from 121 meV to 27 meV, from 95 meV to 29 meV and from 159 meV to 31 meV, respectively. Introduction of the tunnel barrier increases the thermionic emission contribution to the total current considerably, outweighing the additional tunnel resistance. Here, a tunnel barrier of about 1.5-nm-thick polymer resist makes the resistances of reverse-biased Schottky diodes at the source ($V_D > 0$) and drain ($V_D < 0$) more symmetric, resulting in more symmetric $I_D$–$V_D$ compared to LRS–HRS memristors (see Figs 3d, 2b). This switching involves a dynamic negative differential resistance feature for $V_D > 0$ common in memristors (Fig. 3d$^3$). This phenomenon increases the resistance of the intermediate states LD' and LS so that LD' $>$ LD and LS $>$ LS. In other words, switching B in Extended Data Fig. 8e cannot be neglected, which explains the full switching cycles of LRS–LRS memristors. Compared to LRS–HRS memristors, LRS–LRS memristors show higher conductivity at the same $V_D$ bias and switching at smaller $V_D$ bias. This behaviour can be explained by the smaller contact resistance from the lack of Fermi level pinning or increased doping from the residue layer.

This analysis of the LRS–HRS memristor also sheds light on the operation mechanism of heterosynaptic multi-terminal devices (Fig. 4b). Conductance changes occur between the side electrodes 1–4 upon the application of high-bias low-pulses between the main electrodes (5, 6) owing to modulation of the Schottky barrier near the side electrodes. The switching ratios were observed to increase with the overlapping areas of the side electrode with the MoS$_2$. Thus, floating electrodes pin the Fermi level of MoS$_2$, and the energy level of MoS$_2$ under the barriers near the side electrodes. The switching ratios were expected to be distributed near the floating electrodes in the same manner as LRS–HRS memristors during sweeps 2 and 4 (Fig. 2a).

Data availability. The data that support the findings of this study are available from the corresponding author upon reasonable request.
Extended Data Figure 1 | Material characterization of the MoS$_2$ film.

a, Raman spectrum of CVD-grown polycrystalline monolayer MoS$_2$, measured using an excitation wavelength of 532 nm. The Lorentzian peak fits correspond to the $E_{2g}^1$ and $A_{1g}$ modes. 

b, Photoluminescence spectrum of MoS$_2$ collected with the same microscope.

c, d, XPS spectra of MoS$_2$ on a SiO$_2$/Si substrate, showing the Mo 3$d$, S 2$s$ and S 2$p$ peaks. 

e, AFM topography image corresponding to the lateral force microscopy image of Fig. 1c. 

f, AFM topography image of the edge of a MoS$_2$ flake, showing a monolayer step height of about 0.73 nm.
Extended Data Figure 2 | AFM analysis of a residue-free photolithography process. **a**, AFM topography image of MoS$_2$ crystals patterned by PMGI-assisted photolithography. The dashed green line shows the location of the edge of the patterned photoresist in the left region and the white dashed line shows the triangular MoS$_2$ crystal domain before reactive ion etching. **b**, Magnified AFM topography image of the region defined by the black dashed line in **a**, showing chequered regions of protected (1) MoS$_2$, (2) etched MoS$_2$, (3) protected SiO$_2$ and (4) etched SiO$_2$. **c**, Height profiles taken along the two horizontal lines in **b**, showing minimal residue left on the protected SiO$_2$ region. **d**, Height profiles taken along the two vertical lines in **b**, showing minor etching of SiO$_2$ under the etched MoS$_2$ region (2). The noise in the height profiles is due to surface roughness and tip artefacts.
Extended Data Figure 3 | Extended electrical characteristics of the MoS₂ memtransistor. a, Leakage current $I_L$ of the MoS₂ memtransistor of Fig. 2a as a function of $V_G$ after a high-bias sweep from $V_D = 80$ V to $V_D = -80$ V. We note that the current level of 100 pA is close to the instrumentation noise floor. b, $I_D$–$V_D$ curve of a memtransistor ($L = 15 \mu$m, $W = 150 \mu$m) for different $V_D$ sweeps from $|20|$ V to $|80|$ V, showing increasing switching ratio with sweep range (switching ratio $> 10^3$ for the range from 80 V to $-80$ V). c, Magnified view of 50 sweep cycles of the device from Fig. 2b, showing an insulating state in a range of negative $V_D$ values that is dependent on $V_G$ and non-zero crossing, suggesting memcapacitance from contacts. d, $I_D$–$V_D$ curve of a MoS₂ memtransistor during ten consecutive unipolar positive-bias sweeps from $V_D = 0$ V to 80 V. e, $I_D$–$V_D$ curve of the same MoS₂ memtransistor during ten consecutive unipolar negative-bias sweeps from $V_D = 0$ V to $-80$ V. f, Switching from the LRS to the HRS for the MoS₂ memtransistor of Fig. 2b in the forward bias for $V_G > V_{cross}$, where $V_{cross} \approx 35$ V. $I_D$–$V_D$ curve of the device of Fig. 2d during 475 voltage sweeps: g, sweeps 1–100; h, sweeps 100–200; i, sweeps 200–300; j, sweeps 300–400; k, sweeps 400–475.
Extended Data Figure 4 | Current endurance characteristics.

a, Exponential and stretched exponential fits to a typical subset of endurance points from Fig. 2d. The stretched exponential function is defined as $I_D = A - Be^{(C + D/n_0)}$, where $A$, $B$, $C$ and $n_0$ are constants and $\gamma \approx 0.8$. Both the exponential and stretched exponential fits show $R^2 \approx 0.97$, but the stretched exponential shows a better fit at the tail end of the curve. b, Endurance characteristics of a memtransistor, showing only one exponential decay in reverse bias ($V_D = -10 \, \text{V}$). c, $I_D$–$V_D$ curve ($V_G = 0 \, \text{V}$) of a device with $L = 20 \, \mu\text{m}$ and $W = 150 \, \mu\text{m}$, showing a negligible memristive loop (ten sweep cycles) for an unoptimized geometry. d, $I_D$–$V_D$ curve ($V_G = 60 \, \text{V}$) of a device with $L = 10 \, \mu\text{m}$ and $W = 5 \, \mu\text{m}$, showing a negligible memristive loop (19 sweep cycles) for an unoptimized geometry. e, HRS and LRS retention characteristics from Fig. 2e plotted and extrapolated in a doubly logarithmic scale. The relaxation of the two states is faster than conventional filament-based memristors, such as TiO$_2$. © 2018 Macmillan Publishers Limited, part of Springer Nature. All rights reserved.
Extended Data Figure 5 | In situ EFM of a MoS$_2$ memtransistor.

a, Schematic of the in situ EFM measurements of MoS$_2$ memtransistors. b, AFM topography image of the device from Fig. 3a, showing grain boundaries highlighted by red arrows. c, Reproduction of the EFM phase images of Fig. 3a in the forward HRS. d–f, EFM phase images in the forward LRS, reverse LRS and reverse HRS, which were used for the line profiles shown in Fig. 3b. g–o, EFM phase profiles along the red dashed lines 1–8 and 10 in c and d. The EFM phase profile along line 9 is shown in Fig. 3b. All profiles are averaged over 128 lines and are normalized with the EFM phase values at the drain and source.

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Extended Data Figure 6 | Low-temperature transport measurements of a MoS$_2$ memtransistor. 

**a**, $I_D$–$V_G$ curve of the device shown in Fig. 3c (in the LRS) at $V_D = 0.1$ V for temperature varying from 300 K to 75 K at a step of 25 K. 

**b**, Plot of $\ln(I_D/T^{3/2})$ versus $1000/T$ for different $V_G$ values, which was used to extract the Schottky barrier height through the thermionic emission model. 

**c**, $I_D$–$V_G$ and field-effect mobility versus the $V_G$ value of the same device in the LRS and the HRS, respectively. The crossing curves in c show $V_{th}$ shifts by 15 V between the HRS and LRS and $V_{cross} \approx 42$ V.

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Extended Data Figure 7 | Memtransistor modelling. a, Schematic of the increased doping region near the contact, which results in a larger field and reduced metal–semiconductor Schottky barrier height. b, Simulated variation of $w_s\Delta n$ at the source contact for forward bias (sweeps 1 and 2 in Fig. 2a). c, Simulation variation of $w_d\Delta n$ at the drain contact for reverse bias (sweeps 3 and 4 in Fig. 2a). d, Simulated $I_D-V_D$ curve of a MoS$_2$ memtransistor in the forward bias with different $V_G$ values from 10 V to $-30$ V. e, Simulated variation in $w_s\Delta n$ for the same $V_G$ values. The key between d and e applies to both plots.
Extended Data Figure 8 | LRS–LRS MoS$_2$ memtransistor characteristics and mechanism. a, Schematic of an LRS–LRS memtransistor in which a thin photoresist layer acts as a tunnel barrier between the metal contacts and the MoS$_2$ film. b, AFM topography images, showing the step height of the remaining photoresist on a blank Si substrate after a fabrication process without using PMGI. The inset shows the height profile along the white dashed line, which reveals a thickness of about 1.5 nm. c, Gate-tunable $I_D$–$V_D$ curves from Fig. 3d, shown in a linear scale. d, $I_D$–$V_D$ curves of 50 sweep cycles of the LRS–LRS memristor of Fig. 3d. e, Table showing the resistive switching characteristics of LRS–HRS and LRS–LRS memtransistors at the source and drain contacts during the four stages of a full sweep cycle. The conditions of the relative resistance values that are necessary for the two different switching behaviours are listed in the top right corner. Three kinds of resistive switching events, A, B and C, are shown by coloured arrows (see Methods section ‘The switching mechanism’ for details).
Extended Data Figure 9 | Electromigration-induced degradation in control MoS2 devices. a, AFM topography images (corresponding to the upper inset of Fig. 4a), showing electromigration-induced degradation in the material (cyan arrow) near the source electrode (top). The colour scale represents height difference. b, AFM phase image of a device with an hourglass-shaped channel (that is, varying channel length from 5 μm to 1 μm), showing dendritic features along the entire source electrode (top). Without Schottky contacts, we expect a thermal ‘hot spot’ with high local temperature in the region of the highest electric field (V_D/L) (that is, only in the narrowest region in the centre of the channel). Absence of such localized breakdown rules out Joule heating and favours electromigration near the source contact as the dominant phenomenon. The width of the source electrode edge (W_s) is shown by the white arrows. c, I_D–V_D curves (85 sweep cycles) of a degraded polycrystalline monolayer MoS2 memtransistor at V_G = 0 V (L = 5 μm, W = 100 μm). d, AFM topography image of the device of c, showing the dendritic features above the white dashed line. e, A series of five successive snapshots (left to right) from a video captured by a black-and-white camera during sweep 3, as indicated by the dashed red line in c. The red outline and dashed black line in the first frame show the probe tip and electrode pads, respectively. The three middle frames show bright spots from light emission in the channel close to the source electrode (right), marked by black arrows. Light emission was observed during all 85 sweep cycles shown in c. f, Breakdown current I_br (defined in Fig. 4a), showing a linear correlation with W_s for nine single-flake control MoS2 devices. g, Breakdown voltage V_br (defined in Fig. 4a), showing a linear correlation with L, which suggests that the potential decreases both across the channel and at the Schottky contacts. h, Power (I_br × V_br), showing a linear correlation with the channel area (L × W). i, V_br, showing no correlation with W_s. j, I_br also shows no correlation with L.
Extended Data Figure 10 | Electrical characteristics of multi-terminal heterosynaptic device. a–e, Low-bias $I_{ij}-V_{ij}$ curves of 5 permutations of the inner electrodes 1–4 of Fig. 4b at $V_G = 20 \text{ V}$, where $ij = 12, 13, 14, 23$ and 34. $I_{34}-V_{34}$ is shown in Fig. 4b. The key in a applies to all panels a–e. The black curves were measured before any pulsing. The green curves were measured after applying a $-80\text{ V}$ pulse at $V_{65}$ (5, drain; 6, source) four times at a voltage ramping rate of $10 \text{ V s}^{-1}$. The red curves were measured after applying a $-80\text{ V}$ pulse at $V_{56}$ (6, drain; 5, course) three times at the same ramping rate. The conductance returns to the pre-pulse state for all electrode combinations. The $I_{34}-V_{34}$ curve could not be measured after the $V_{65}$ pulse cycle. f, Change in the conductance between electrodes 2 and 4 ($G_{24}$) with $V_{56}$ and $V_{65}$ pulses for different $V_G$ values showing gate tunability of heterosynaptic plasticity. g, h, Spatial profile of the MoS$_2$ conductance band minimum ($E_c$) along the two dashed lines in g, which pass through (s) and outside (y) the side electrodes.