Design of Phased Array T/R Component Microsystem Based on Heterogeneous Integration Technology

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Abstract. An X-band silicon-based 2x2 phased array T/R module was developed based on MEMS technology and three-dimensional heterogeneous integration technology such as through-silicon via (TSV). The module uses a transceiver integrated multifunction chip solution and is packaged in two layers of silicon: upper layer integrated low noise amplifier, power amplifier, switch, power modulation driver, PMOS and other chips; lower layer integrated multifunction chip, serial-to-parallel chip, logic operation chip. Two-layer silicon package are stacked by solder balls. The T/R module sample’s size is 20mm×20mm×3mm. The test results show that at 8-12GHz, the transmit power is higher than 29dBm, the transmit gain is 20dB, the receive gain is 29dB, the noise figure (NF) is 3dB, and the switch isolation is 37dB.

1. Introduction
Phased array antennas can achieve good search and tracking of fast maneuvering targets and have been one of the key research topics in the field of antennas. With the rapid development of monolithic integrated circuit technology, new electronic materials and assembly interconnection technology, solid-state active phased array technology has become more and more widely used in military and civilian electronic equipment. The active phased array transceiver (T/R) component is the core part of the active phased array system, which directly determines the performance of the phased array[1].

For any electronic system, miniaturization has always been the unchanging pursuit. Especially in the field of military confrontation with higher performance requirements, small size and high integration are important manifestations of the core competitiveness of equipment[2]. At present, most phased array transceiver (T/R) component modules are manufactured using the SMT process, and their integration is relatively low. The three-dimensional heterogeneous technology can not only greatly reduce the global interconnect length, but also improve chip integration and reduce chip size. The structure fabricated by the three-dimensional heterogeneous integration technology has the advantage that the planar two-dimensional structure cannot be compared[3].

In this paper, the MEMS bulk silicon processing technology is used to realize the three-dimensional vertical interconnection through the wafer level bonding process and TSV. A silicon-based X-band 2x2 phased array sub-array T/R module is successfully designed and manufactured to realize the miniaturization of the volume. At the same time, it has higher circuit performance.

2. Design of rf transceiver system
The silicon-based 2x2 RF transceiver module of this design not only needs to meet the requirements of electrical performance, but also requires small size, light weight and high integration in the physical performance. According to the principle of the array antenna, in order to suppress the grating lobes, the
The antenna array should not be too large, which limits the layout space of the transceiver module[4]. Comprehensive consideration, this topic uses a transceiver integrated multi-function chip program.

After the successful development of the amplitude and phase control multi-function integrated chip, the chip used in the T/R component can be simplified into four chips: limiter, low noise amplifier, power amplifier, and amplitude and phase control multifunction chip. The block diagram of the T/R component using the amplitude and phase control multifunction chip is shown in the Figure1.

![Figure 1. RF transceiver system block diagram (multi-function chip solution)](image)

The use of multi-function chips can greatly reduce the size of the transceiver front end, reduce the number of chips, increase reliability, reduce circuit complexity and assembly difficulty. Therefore, the amplitude and phase control multi-function chip fabricated by GaAs E/D PHEMT process is used to realize the amplitude and phase control function of the transmitted and received signals. The chip integrates the following circuit functions: SPDT switch, 6-bit digital phase shifting, 6-bit digital control attenuation, 3-level amplification, 14-bit amplitude and phase control parallel port drive. The operating frequency covers 8GHz to 12GHz, the receiving gain is 10dB, the transmission gain is 12dB, the switching speed is 100ns, and using TTL control level.

Because the size of the circulator is too large and the isolation of the circulator is generally small. In this design, the antenna end transceiver switching adopts a high-power GaN MMIC switch with a switch isolation of 37dB. In this way, the transmission and reception link time-sharing work can well avoid the crosstalk of the transmission link, reduce the noise figure, and further realize the miniaturization and broadband performance of the components.

The receiving channel should have low noise and large dynamic characteristics. The noise figure of the cascade system is:

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1G_2} + \frac{NF_4 - 1}{G_1G_2G_3} + ... + \frac{NF_n - 1}{G_1G_2...G_{n-1}}$$

According to this formula, the first three stages of the receiving link contribute to the main part of the system noise. Therefore, the insertion loss of the high-power switch and the limiter and the noise figure of the LNA are the key factors to meet the design specifications. When the loss of the passive device is smaller, the noise figure of LNA is lower, and the gain is larger, the noise figure of the receiving link is lower.

After considering, the receiving link adopts GaAs MMIC limiting low noise amplifier chip, which integrates limiting and low noise amplification functions, and its frequency range covers 7 to 13GHz. The PIN driver chip is used as the pulse modulation power supply of the LNA. The transmit link uses a GaAs MMIC power amplifier with an operating frequency of 8 to 12GHz. In addition to the power amplifier chip, it also requires a peripheral bias drive chip for GaAs FET gate bias and drain power modulation.

In summary, the main technical specifications of the RF transceiver system are:
- Transmit power: 29dBm;
- Transmit gain: 20dB;
Receive gain: 29dB;
Noise figure: 3dB;

3. Structural design and technological process

3.1 Structural Design

Although the design uses a multi-function chip for transceiver, which greatly reduces the number of chips, since the multi-function chip contains more functional modules and the power output of the power amplifier is larger, the area of the multi-function chip and the power amplifier is larger, so many control circuits and DC interfaces cannot be reasonably placed on a silicon substrate.

Comprehensive consideration, the RF transceiver system is packaged in two silicon-based packages: upper integrated low noise amplifier, power amplifier, high power switch, power modulation driver, PMOS and other chips; lower layer integrated multifunction chip, serial to chip, logic Operation chip and power divider chip. The power splitter is divided into two paths, and then divided into four channels by two power splitters, which are allocated to the common end of the multi-function chip of each channel. The principle of the integrated module transceiver link is shown in Figure 2.

![Figure 2. 2×2 integrated package module](image)

The MEMS microsystem silicon-based package used in this design consists of four layers of silicon. The lower three layers form the silicon-based package, and the top silicon is the silicon-based cover. Upper and lower silicon-based modules and the PCB mother board are all connected by solder ball. The specific package structure is shown in Figure 3.

![Figure 3. 2×2 integrated package structure sectional view](image)
mentioned transceiver link principle, the circuit layout and routing design are performed by using ADS software, as shown in Figure 4 below:

3.2 Technological Process

The modules designed in this paper are implemented using MEMS bulk silicon processing and chip-to-wafer processes. The silicon wafer is prepared by the MEMS bulk silicon process. Figure 5. shows the main flow of the process[5]. The following is a brief description of the process:

a) Select 6-inch high-resistance silicon as the substrate, the high-resistance silicon resistivity is $10000 \sim 20000 \ \Omega \cdot cm^2$. After surface treatment, a $SiO_2$ passivation layer of 1~2 μm was prepared (Figure 5(a)).

b) Etching and splicing the same size of the chip to be assembled in the $SiO_2$ layer by photolithography and BOEing etching (Figure 5(b)).

c) Using KOH as the etching solution, the cavity buried by the chip was prepared by a wet etching process with a cavity depth of 105μm. Use BOE etching technology to remove the remaining $SiO_2$ layer to achieve higher thermal conductivity of the silicon wafer (Figure 5(c)).

d) Prepare TSV vias by dry etching process(Figure. 5(d)).

e) A seed layer is prepared by a sputtering process, and a 3μm thick metal pattern is prepared by photolithography and electroplating(Figure 5(e)).

The chip-to-wafer integration process is used to assemble the MMIC chip into the cavity of the underlying silicon wafer. The interconnection between the chip and the chip and the substrate is realized by wire bonding[6]. After completing the intermediate electrical test, a low-temperature bonding process is used to achieve wafer-level three-dimensional integration and packaging[7]. The main process flow of the dual-channel three-dimensional receiving front-end module is shown in Figure 6.
MEMS Process

Chip-Wafer Process

BGA assembly and Solder ball planting technology

Slicing process

Figure 6. The main process flow of the 2x2 phased array T/R module

4. Measured Results

The T/R module uses four layers of high-resistance silicon to form a microwave circuit package with a size of 20mm×20mm×3mm. The product evaluation photo is shown in Figure 7. The module's receiving gain, NF, phase shift accuracy and attenuation accuracy are analyzed by vector network analyzer, and the transmission power is measured by a power meter.

The results are shown in Figure 8.

Figure 7. The test structure of the 2x2 phased array T/R module

(a) The gain of the receiving channel
(b) NF of the receiving channel

(c) Transmission power

(d) Attenuation accuracy of RMS
Figure 8. Measured results of the 2x2 phased array T/R module

5. Conclusion
In this paper, a silicon-based X-band phased array T/R component sample was successfully designed and fabricated based on MEMS process and three-dimensional heterogeneous integration technology. The test results show that the module has a noise figure (NF) of less than 3dB in 9.5-12GHz and a receiving gain of (29±1)dB in 8-12GHz, while ensuring phase shift accuracy of RMS≤4° and attenuation accuracy of RMS≤0.5dB. The module basically achieves the expected design goals and proves the feasibility of using the three-dimensional integration technology to realize the miniaturization of the RF transceiver system. It has certain reference value for the research of RF transceiver micro-system.

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