Ultra-low power on-chip learning of speech commands with phase-change memories

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Abstract—Embedding artificial intelligence at the edge (edge-AI) is an elegant solution to tackle the power and latency issues in the rapidly expanding Internet of Things. As edge devices typically spend most of their time in sleep mode and only wake-up infrequently to collect and process sensor data, non-volatile in-memory computing (NVIMC) is a promising approach to design the next generation of edge-AI devices. Recently, we proposed an NVIMC-based neuromorphic accelerator using the phase change memories (PCMs), which we call as Raven. In this work, we demonstrate the ultra-low-power on-chip training and inference of speech commands using Raven. We showed that Raven can be trained on-chip with power consumption as low as 30 µW, which is suitable for edge applications. Furthermore, we showed that at iso-accuracies, Raven needs 70.36 × and 269.23 × less number of computations to be performed than a deep neural network (DNN) during inference and training, respectively. Owing to such low power and computational requirements, Raven provides a promising pathway towards ultra-low-power training and inference at the edge.

Index Terms—Artificial intelligence, internet of things, phase change memories, non-volatile synaptic circuits, neuromorphic computing.

I. INTRODUCTION

In this era of rapidly expanding internet of things (IoT), embedding artificial intelligence (AI) at the edge (edge-AI) is an elegant solution to tackle the cost, bandwidth, power, latency, and privacy issues arising from edge-to-cloud computing [1]–[4]. At present, deep neural networks (DNNs) provide the best classification accuracies in solving many AI problems such as image classification, pattern/object recognition, speech recognition, etc. [5]–[7]. As a result, DNNs are commonly used to embed AI at the edge. Usually, the training of DNNs is performed in the cloud, the learned weights are transferred to the edge, and only inference is performed at the edge. The reason is that the training of DNNs typically requires back-propagation of end results throughout the network [8], and it needs large amounts of memory and computational resources. However, IoT environments such as autonomous driving, security surveillance, and smart cities continuously change over time. If training for such environments is performed in the cloud, a large amount of data needs to be transmitted to the cloud, which leads to higher costs, increased latencies, and lower bandwidths [9], [10]. Alternatively, performing training at the edge can be a promising approach to achieve continuous real-time learning with reduced cost, latency, and bandwidth concerns.

Recently, spiking neural networks (SNNs) have emerged as potential computing paradigms for enabling AI at the edge [11], [12]. Inspired by the information processing mechanisms in the brain, the data in SNNs is encoded and processed in the form of binary spikes. As processing time increases, the spiking activity in SNNs reduces drastically [13], [14]. Moreover, SNNs are event-driven, which means computations are performed only when the neurons emit/receive the spikes [15], [16]. Furthermore, SNNs can be trained using the spike-time-dependent plasticity (STDP) learning rule [17]. STDP is a localized learning rule, where the weights are updated based on the relative timing of spikes emitted by a neuron and of those that it receives. Therefore, due to the STDP-based localized learning ability, sparse spiking activity, and event-driven computations, the SNNs facilitate ultra-low-power training and inference of data at the edge.

On the other hand, one major concern in today's edge devices [18]–[20] is that they are designed based on the conventional von Neumann architecture with separate memory and processing units. As a result, the data must be transferred between memory and processing units to perform any operation. Such data movement results in long inference delays and additional power overheads. In addition, there exists a significant gap between memory and processor speeds. The widely used main memories-dynamic random-access memories (DRAMs) [21] are several orders lower than their processing counterparts. As a result, the overall performance of the system is limited more by the slow memories rather than processors.

One solution that has recently emerged is in-memory computing (IMC), where some computational tasks are performed within the memory subsystem [22]–[25]. When provided with inputs, the data in IMC engines (IMCEs) can be updated and processed in-situ by eliminating the latency and power consumed to transfer data between memory and processing units in conventional von Neumann architectures. Presently, many existing and emerging memory technologies can be used to design the IMCEs [22]–[25]. Several works have recently demonstrated IMCEs based on DRAMs and static random-access memories (SRAMs) [23], [27]. Though SRAMs and DRAMs facilitate relatively fast read, write and compute operations, they are volatile memories (i.e. the memory sub-system must be always ON for data to be retained). As edge devices typically spend most of their time in sleep mode, the use of volatile memories results in significant standby power.

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consumption.

In contrast, the non-volatile in-memory computing (NVIMC) is a crucial design technique for enabling ultra-low power edge devices with reduced latencies [28]–[34]. The data in NVIMC engines (NVIMCEs) is retained even if the power is turned off. Thus, the NVIMCEs can be powered down to achieve near-zero standby power consumption when the device is in deep sleep mode. If the device wakes up, data in the NVIMCE can be updated and processed in-situ. The non-volatile memory (NVM)-based crossbar array is a promising design technique to accelerate the neural networks with massive parallelism [31], [35]–[38]. Recently, we proposed a non-volatile phase change memory (PCM)-based crossbar architecture [39] for accelerating the SNNs in memory. For convenience, we call this architecture as Raven for the rest of this paper.

In this work, using the devices, circuits, and architectures of Raven (i.e. are proposed in [39]), we demonstrate ultra-low-power on-chip training and inference of speech commands. First, we considered the Google’s speech commands dataset [40] and converted the audio files into the Mel-frequency cepstral coefficient (MFCC) images [41]. To learn and classify these images, we accelerated the spiking restricted Boltzmann machines (RBMs) with event-driven contrastive divergence (CD) based learning [42] on Raven (i.e. using software simulations). Our simulation results show that Raven can be trained on-chip with power consumption as low as 30 μW, which is suitable for edge applications. Next, we also compared the classification accuracies of our work with the results obtained from DNNs [43]–[45], commonly used for speech command recognition.

The rest of this paper is structured as follows. Section II introduces the devices, circuits, and architectures of Raven (i.e. are proposed in [39]). Section III presents the design strategies implemented to achieve on-chip training and inference of speech commands using Raven. Section IV introduces the PCM hardware-aware spiking RBM simulator used to demonstrate the speech command recognition using Raven. Section V presents the results and discussion on speech command recognition. Finally, Section VI concludes this chapter.

II. PHASE-CHANGE MEMORY BASED SYNAPTIC CIRCUITS AND ARRAYS

PCMs typically exist in either an amorphous phase or in one of the several crystalline phases [46]–[48]. When the PCM is in the amorphous phase, a high resistance-state is sensed. When the PCM is in one of the crystalline phases, a low resistance-state is sensed. Furthermore, the phase/resistance of PCMs can be modified electrically based on the joule heating mechanism. Recently, a PCM cell having 200–1000 states, changes in the conductance is demonstrated experimentally [49]. Therefore, owing to the linearity, non-volatility, a large number of resistance states, and high-yield manufacturability, PCMs have recently been the subject of great interest for different applications such as embedded memory [50]–[52], in-memory processing [31], [33], [53], [54], neuromorphic computing [34], [39], [55], [56], etc.

Recently, we proposed a novel PCM-based synapse comprising of two 3T1R circuits [39]. The two variable resistors, \( R_p \) and \( R_n \), are used to store the signed weight of the synapse. To access the stored weight, two currents are passed through the \( R_p \) and \( R_n \) in 3T1R(+) and 3T1R(-) circuits, respectively. The difference between the resistance values of \( R_p \) and \( R_n \) determines the magnitude and sign of the weight. In addition, when placed in a neural circuit with pre and postsynaptic spiking neurons, the two 3T1R circuits can enable asynchronous operation of three fundamental mechanisms in SNNs: a) spike propagation from pre to the postsynaptic neuron, b) spike propagation from post to the presynaptic neuron, and c) weight update based on STDP.

As mentioned in Section I, the capacitor-based LIF neurons [39] are used as pre/postsynaptic neurons in this work. As shown in Fig. 2, the neuron circuits consist of capacitors, current mirrors, comparators, and single-shot pulse generators. The voltage stored in the capacitor (\( V_{cap} \)) is treated as a membrane potential of the neuron. Using \( V_{cap} \), the current mirror circuits charge and discharge the current based on the resistance values of \( R_p \) and \( R_n \). Consequently, \( V_{cap} \) will be updated. The current mirror circuit configuration can be found in [39]. If \( V_{cap} \) exceeds the pre-defined threshold voltage, \( V_{th} \), the comparator will generate a spike using the subsequent single-shot pulse generator. Additionally, several other circuits are needed and used in this work to implement the refractory, leaky, and reset behaviors of conventional LIF neurons. The additional circuitry is omitted from the Figs. [33] for simplicity. The complete circuit configuration can be found in [39].

Now, let us discuss the three operations of the synapse. First, if the presynaptic neuron fires, a spike will be propagated into the word line, \( LIF_{WL} \). The red-colored line in Fig. 2 (a) highlights the direction of spike propagation. Consequently, the transistors, \( T_1 \), and \( T_4 \) will be ON and, the current flows...
After some delay, the second spike will be fired into the current mirror circuit which is connecting to LIF highlighted using the green-colored lines in Fig. 2 (a) and negative current, respectively. The current directions are specified, positive current flows from BLIF into LIF and negative current flows from current mirror circuit through $R_p$ and $R_n$ as positive and negative current, respectively. The current directions are highlighted using the green-colored lines in Fig. 2 (a) and the amount of current is determined by Ohm’s law. Then, the current mirror circuit which is connecting to $LIF_{BL}R_p$ and $LIF_{BL}R_n$ senses the difference of the positive and the negative current by charging and discharging one capacitor in the postsynaptic neuron. By using this differential sensing scheme, $V_{cap}$ is increased or decreased depending on the polarity and value of the synaptic weight with every incoming spike.

As discussed earlier, if $V_{cap}$ exceeds $V_{th}$, the postsynaptic neuron will fire spikes into lines, $STDP_{BL}$ and $BLIF_{WL}$. The pulse timing of spikes emitted by the postsynaptic neuron is depicted in Fig. 2 (b). First, a spike will be fired into the bit-line, $STDP_{BL}$ and this will be used for modifying the resistance values of $R_p$ and $R_n$. After some delay, the second spike will be fired into the word-line, $BLIF_{WL}$. Spikes in $BLIF_{WL}$ will be used for transmitting the spiking information from post to the presynaptic neuron.

If a postsynaptic neuron fires, a spike will be propagated into $BLIF_{WL}$ (as discussed in the last paragraph). The direction of spike propagation is highlighted by the red-colored line in Fig. 3 (a). Consequently, the transistors, $T_2$ and $T_3$ will be turned ON. Then, the current flows from the current mirror circuit in presynaptic neurons into $STDP_{BL}$ through $R_p$ and $R_n$ as positive and negative current, respectively. Specifically, positive current flows from $BLIF_{BL}R_p$ to $T_2$ to $R_p$ to $STDP_{BL}$ and negative current flows from $BLIF_{BL}R_n$ to $T_2$ to $R_n$ to $STDP_{BL}$. The current directions are highlighted using the green-colored lines (See Fig. 3 (a)). The $V_{cap}$ of the postsynaptic neuron will be either increased or decreased depending on the resistance values of $R_p$ and $R_n$. If $V_{cap}$ exceeds the $V_{th}$, the presynaptic neuron fires spikes into lines, $LIF_{WL}$, $STDP_{WL}R_p$ and $STDP_{WL}R_n$. The timing of spikes emitted by the presynaptic neuron is depicted in Fig. 3 (b). First, the spikes will be fired into $STDP_{WL}R_p$ and $STDP_{WL}R_n$. These spikes will be used for modifying the weight based on the STDP rule. Next, a spike will be fired into $LIF_{WL}$, and that can be used for transmitting the spiking information from pre to the postsynaptic neuron.

On the other hand, the spikes propagating through the bit-line, $STDP_{BL}$, and word-lines, $STDP_{WL}R_p$ and $STDP_{WL}R_n$, enable modification of the weight. For instance, spikes propagating through $STDP_{WL}R_p$ and $STDP_{WL}R_n$ will turn ON the transistors, $T_3$ and $T_6$. The directions of spikes propagating in the circuit are highlighted by the red-colored lines (See Fig. 3 (a)). Concurrently, if a spike propagates through $STDP_{BL}$, new current paths will emerge: a) $STDP_{BL}$ to $R_n$ to $T_3$ to GND and b) $STDP_{BL}$ to $R_p$ to $T_6$ to GND (as highlighted by the green-colored lines in Fig. 3 (a)). Depending on the magnitude and duration of currents passing through these paths, the resistances of $R_p$ and $R_n$ will be modified. For example, when a spike propagating through $STDP_{WL}R_p$ has low magnitude and large pulse width as shown in Fig. 3 (b), the resistance value of $R_p$ decreases. In other words, the PCM is being set to the crystalline phase (i.e. low resistance state).
Fig. 3. Circuit operation of PCM-based synapse in the presence of pre and postsynaptic neurons [39]. (a) when spikes propagate from post to the presynaptic neuron. If the potential of presynaptic neuron exceeds the threshold, spikes with predefined pulse timing (b) will be fired.

Fig. 4. (a) the circuit operation during the STDP-based weight update, and the timing diagrams of spikes needed to (b) increase or (c) decrease the weight [39].
However, if a spike propagating in $STDP\_WL\_R_p$ has high magnitude as shown in Fig. 4 (c), the resistance value of $R_p$ will increase. In other words, the PCM cell is changed to an amorphous phase (i.e. high resistance state). If spikes propagating through $STDP\_WL\_R_p$ and $STDP\_WL\_R_n$ as designed with timing diagrams as shown in Fig. 4 (b), $R_p$ will increase and $R_n$ will decrease and the overall weight will be increased. If spikes propagating through $STDP\_WL\_R_p$ and $STDP\_WL\_R_n$ as designed with timing diagrams as shown in Fig. 4 (c), $R_p$ will decrease and $R_n$ will increase and the overall weight will be decreased.

Furthermore, Fig. 5 shows the architecture of Raven designed using the above-discussed synaptic and neural circuits. As shown in Fig. 5, the synaptic circuits are arranged in a crossbar array-like structure with presynaptic neurons in the left and postsynaptic neurons at the bottom. Moreover, the area of an 832×832 array connected to 832 presynaptic neurons in the left and 832 postsynaptic neurons at the bottom is estimated to be 2.20 mm×2.55 mm.

### III. Speech Command Recognition using Spiking RBMs

The Raven circuits and architectures introduced in Section II can be used to demonstrate the on-chip training and inference of speech commands. We will now discuss the design strategies, algorithms, and neural networks used for such a demonstration.

First, Google’s speech commands dataset is considered in this work. This dataset contains more than 0.1 million utterances of 30 different words. Importantly, it contains words that can be used as commands in the IoT/robotics applications, e.g. stop, go, left, right, up, down, on, off, yes, no, etc. Besides, it also contains the recordings of spoken digits from 0 to 9, various kinds of background noise, and few random utterances (e.g. “happy”, “bird”, “horse”, “tree”, “wow”, etc). Each audio file in the dataset is one-second-long and is sampled at 16 kHz.

Throughout this work, 500 audio files of each command are used to create the training datasets and 250 different audio files of each command are used for creating the test datasets.

Currently, in most of the automatic speech recognition systems, the sound data is first converted into MFCC images, and the images are fed as inputs to the neural networks. Specifically, four main steps listed below are involved in generating the MFCC images.

1. Generate a spectrogram (Fig. 6 (b)) for the sound data of an audio file (Fig. 6 (a)) using Short-Time-Fourier Transforms (STFT). The time-varying sound waves are divided into several small overlapping time frames. The frequencies of sound waves in each time frame are then calculated using the fast Fourier transforms. Note that depending on the size of the time frame and the extent of overlap between the two adjacent frames, the spectrogram can either have better time resolution or frequency resolution.

2. Perform the Mel-frequency sampling on the output spectrogram (Fig. 6 (b)). This sampling re-scales the frequency axis of the spectrogram and emphasizes more on the frequency information in the human’s hearing range.

3. Compress the Mel-sampling output (Fig. 6 (b)) using discrete cosine transforms. This step removes redundant information in the Mel-sampling output.
Fig. 6. The step-by-step procedure followed to demonstrate speech recognition. (a) the raw sound data is first converted into (b) a spectrogram by applying short-term Fourier transforms, (c) and then into a Mel-frequency sampled image. (d) The image is then compressed using the discrete cosine transforms followed by (e) normalization problem. The final normalized output is provided as input to the (f) spiking RBMs.

4) Finally, normalize the compressed output (Fig. 6 (c)). This step reduces the influence of background noise and cancels out the differences in feature maps between different speakers.

As shown in Fig. 6 (e), the final output of these steps is fed as input to the spiking RBMs [57]. RBMs are bi-layer stochastic neural networks with neurons in one layer connected to all the neurons in the other layer, but not connected to neurons within the layer. As shown in Fig. 7, neurons in the first (i.e. visible) layer are divided into three categories-image, label, and bias neurons. The size of input images determines the number of image neurons required in this layer. Similarly, the total number of labels under classification determines the number of label neurons needed. On the other hand, neurons in the second (i.e. hidden) layer are divided into two categories-hidden neurons and bias neurons (See Fig. 7). The hidden neurons learn the features of input images and the number of hidden neurons required depends on the total number of weights required to achieve higher accuracies. Finally, the number of bias neurons required (i.e. in both the visible and hidden layers) needs to be tuned to achieve higher accuracies.

The spiking RBMs are trained with the STDP-based event-driven CD algorithm [42]. Specifically, training is performed in two phases-data phase (Fig. 7 (a)) and model phase (Fig. 7 (b)). In the data phase, images and their labels will be given as inputs to the visible neurons in the form of Poisson spike trains. High (low) pixel values in image results in high (low) spiking rates of corresponding image neurons. Further, if an image belongs to a particular class, only the label neurons related to that class will have high spiking rates and all the others will have low spiking rates. All the bias neurons in visible and hidden layers receive Poisson spike trains with high spiking rates. In the data phase, these externally generated spike trains will propagate from visible to the hidden layer and the weights will be updated positively. Next, in the model phase, no external input spikes are provided to the visible/hidden layer neurons except for the bias neurons. Only the internal spikes and the bias neuron spikes will propagate between the two layers and the weights will be updated negatively. When learning converges, there won’t be any further change in the weight be it in the data phase or model phase.

On the other hand, to perform the inference (Fig. 7 (c)), Poisson spike trains of input images will be provided to the visible neurons. The spikes fired by all the label neurons during the inference period will be counted. The label neurons firing more number of spikes compared to others would be considered as the classification output. For example, when an MFCC image of speech command-“stop” is given as input and the “stop” label neurons fired more spikes than others, the classification output will be “stop”. In contrast, if the “go” label neurons fire more spikes than others, the classification output will be “go”.

Note that all the operations required to be performed in spiking RBMs can be accelerated using the Raven (Fig. 5) introduced in Section. III. The presynaptic neurons connected to the left-side of the synaptic array can be used as visible neurons, whereas the postsynaptic neurons connected at the bottom of the synaptic array can be used as hidden neurons.
Fig. 7. Network structure of spiking RBMs with image, label, hidden, and bias neurons. (a) During the data phase in training, the Poisson spike trains are provided as inputs to image, label, and bias neurons. (b) During the model phase in training, only bias neurons receive the Poisson spike trains. (c) During the inference process, an image is provided as input to the image neurons (i.e. in form of the Poisson spike trains) and the classification output is obtained by counting the spikes fired by label neurons.

Fig. 8. The step-by-step procedure followed in the hardware-aware spiking RBM simulator (i.e. indicated by the red-colored text). The output of each process in the flowchart is provided (i.e. indicated by blue-colored text).

The input (output) spike trains can be provided (read) using the external spike input (output) circuitry. During the data phase of training, the pulse timings of $STDP_{WL_{p}}$ and $STDP_{WL_{r}}$ can be configured as shown in Fig. 4 (b). In such configuration, $R_{p}$ will decrease, and $R_{r}$ will increase and the weight will be updated positively. Similarly, during the model phase of training, the pulse timings of $STDP_{WL_{p}}$ and $STDP_{WL_{r}}$ can be configured as shown in Fig. 4 (c). In such configuration, $R_{p}$ will increase, and $R_{r}$ will decrease and the weight will be updated negatively. Finally, during the inference, the lines, $STDP_{BL}$, $STDP_{WL_{p}}$, and $STDP_{WL_{r}}$ can be disabled and no spikes will propagate through them. Input spike trains of images will be provided to the visible neurons and concurrently, the spikes fired by all the label neurons will be counted using external counters.

IV. PCM HARDWARE-ARE AWARE SPIKING RBM SIMULATOR

We will now discuss the PCM hardware-aware spiking RBM simulator developed to demonstrate the speech command recognition in this work.

Based on the earlier works on event-driven CD in spiking neuromorphic systems [42], we first developed a spiking RBM simulator that can take sound data as input and perform training and inference operations on the data. This simulator needs several input parameters such as spiking rate, magnitude and pulse width of spikes, equilibrium/rest potential, alpha parameter to update the potential, threshold potential,
refractory time, and leak time constant. To estimate these parameters and to take the hardware characteristics/limitations into account, we followed the step-by-step procedure shown in Fig. 8. First, the characteristics of PCM cells such as minimum and maximum resistance values, and current/voltage versus resistance curves are extracted from the experimental data. Next, depending on the size of the synaptic array, the voltages and pulse widths required to read and program the synaptic weights are estimated using SPICE circuit simulations. The behavior of pre and post-synaptic neuron circuits is then studied using SPICE simulations and the abovementioned parameters are estimated and provided as inputs to the spiking RBM simulator, which provides the classification accuracies. Finally, the hardware-software co-optimization is performed based on the classification accuracies and the performance evaluation of circuits in SPICE.

V. Results and Discussion

Using the simulator introduced in Section IV we will now study the feasibility of performing on-chip training and inference using Raven.

First, the audio files are converted into MFCC images by choosing the size of each time frame in STFT as 160 ms and the overlap between two adjacent frames as 120 ms. Also, 22 frequency bins are used in DCTs. As a result, the output MFCC images have a size of $22 \times 22$ pixels. Next, these MFCC images are provided as inputs to the spiking RBMs simulator with network parameters tabulated in Table I and

| TABLE I  |
|------------------|
| Quantity         | Value       |
| Visible neurons  | 384         |
| Label neurons in visible layer | 20         |
| Bias neurons in visible layer | 8          |
| Hidden neurons in hidden layer | 500        |
| Bias neurons in hidden layer | 8          |
| Reset/equilibrium potential value | 0          |
| Alpha parameter for updating the potential | 0.06       |
| Threshold potential value | 1          |
| Leak time constant | 1 ms       |
| Refractory time period | 4 ms       |
| Spiking rate | 20 Hz       |

and Table II.

| TABLE II  |
|------------------|
| Quantity         | Value       |
| VSBL             | 2.5 V       |
| VBWL, VLWL       | 1.2 V       |
| VWLL             | 0.75 V      |
| VWLH             | 1.4 V       |
| a                | 9.1 $\mu$s (min) - 2040 $\mu$s (max) |
| b                | 4.4 $\mu$s (min) - 85.8 $\mu$s (max) |
| c                | 20 ns (min) - 79 ns (max) |
| d                | 27 $\mu$s (min) - 4251.6 $\mu$s (max) |

Fig. 9. (a) sample sound data with the utterance of command in first 0.5 s and (b) the test error rates of four speech commands when the raw sound data is used for training and inference. In each epoch, the average error rate of four speech commands is denoted by the height of a vertical bar. The four colors in a bar represent the contribution of four commands to the average error rate. (c) the modified sound data with utterance centered at 0.5 s and (d) the test error rates of four speech commands when the modified sound data is used for training and inference.
the magnitude and pulse widths of spikes used are tabulated in Table II. When a set of four speech commands—up, down, left, and right—is considered for training and inference, the best test error rate is found to be 25%. Fig. 9(b) shows the test error rates observed in each epoch.

The high error rates (see Fig. 9(b)) arise due to the differences in the exact time at which the commands are uttered in a second. For example, in the sample sound data shown in Fig. 9(a), the utterance occurred in the first half of a second. If such sound data is used to create an MFCC image, the extracted features will be on the left side of the image (not shown here). Similarly, if the sound data is present in the second half of a second, the extracted features will be on the right side of the image. We found that such variations in the position of features lead to high classification error rates.

To resolve this problem, we modified the timing data of each audio file in such a way that the utterance always occur around 0.5 s (as shown in Fig. 9(c)). As a result, the best test error rate got reduced to 15% as shown in Fig. 9(d).

![Fig. 10. Dependence of test error rates on the image width and height. Color bar represents the error rate percentages.](image)

Moreover, as discussed in Section III the size of input images determine the number of image neurons required and thereby the total number of weights in the network. Furthermore, depending on the image size, the MFCC image can either have better time resolution or frequency resolution, but not both. Therefore, it is crucial to find out the optimum image size required to achieve low classification error rates. The phase diagram shown in Fig. 10 depicts the dependence of error rates on the input image size. As shown in Fig. 10 low error rates are obtained when the image width/height is between 20 to 24 pixels.

To further reduce the error rates, it is proven in the literature that multiple images of different sizes can be placed side by side and provided as input to the neural networks [58]. We also studied this possibility and found that an error rate of 13.5% can be achieved by using two images of sizes 16×16 and 8×16. Next, using such a two image configuration, we estimated the classification accuracies for different sets of speech commands and compared them with the results obtained from the state-of-the-art convolution neural networks (CNNs) [43–45]. As shown in Table III, the minimum (maximum) accuracy difference between CNNs and our work is found to be 5.12% (18.93%). Such an accuracy difference is expected as SNNs with STDP-based learning generally have moderate classification performance when compared to DNNs trained with backpropagation. Currently, there are several ongoing research efforts to close the accuracy gap between DNNs and SNNs [59–61].

| Speech commands                  | CNNs | Our work |
|----------------------------------|------|----------|
| up, down, left, right            | 94.5%| 86.4%    |
| bed, cat, happy, bird, five      | 91.36%| 86.24%   |
| spoken digits [0-9]              | 90%  | 78.36%   |
| stop, go, left, right, on, off, up, down, yes, no, silence, unknown | 88.2%| 69.27%   |

![Table III](image)

Next, to compare the memory and computational requirements of our work with the CNNs at iso-accuracies, we implemented a fully-convolutional neural network (FCNN) [62] with 8 layers as shown in Table IV. In Table IV, W and H represent the width and height of the feature maps, IFs represent the number of input feature maps provided to each layer, OFs represent the number of output feature maps extracted from each layer. We optimized and the parameters tabulated in Table IV to achieve the same classification accuracies as our work. The backpropagation algorithm with stochastic gradient descent is used to train the FCNNs [8], while the spiking RBMs are trained using event-driven CD algorithm. Note that unlike the spiking RBMs, weights in FCNNs are trained using 32-bit floating-point numbers. The number of parameters, spikes/multiply-and-accumulate operations (MACs), and epochs required to obtain iso-accuracies are estimated and tabulated in Table V. MACs are the fundamental operations required by the CNNs. As shown in Table V the number of MACs performed in the FCNNs during training and inference is 269.23× and 70.36× greater than the number of spikes generated in the spiking RBMs, respectively. Due to such low computational requirements, the spiking RBM implementation can be more suitable for edge applications, in which accuracies may not be of paramount importance.

| Description | W×H×IFs  | W×H×OFs |
|-------------|---------|---------|
| Conv1       | 24×16×1 | 22×14×64 |
| Maxpool1    | 22×14×64| 11×7×64 |
| Conv2       | 11×7×64 | 9×5×52  |
| Maxpool2    | 9×5×52  | 4×2×52  |
| Conv3       | 4×2×52  | 3×1×36  |
| Maxpool3    | 3×1×36  | 1×1×10  |
| Conv4       | 1×1×36  | 1×1×10  |
| Dense       | 1×1×10  | 10      |

![Table IV](image)
Finally, using the SPICE simulations, we estimated the power and latencies consumed by the Raven circuits and architectures during the training and inference operations. The power and latencies consumed during the training of 5000 MFCC images are estimated to be 30 $\mu$W (7 $\mu$W of active power and 23 $\mu$W of static power) and 3000 sec, respectively. Also, the power and latency consumed for an inference operation on Raven are estimated to be 28 $\mu$W (5 $\mu$W of active power and 23 $\mu$W of static power) and 0.45 sec, respectively. Note that we used the 90 nm CMOS technology for this work.

VI. CONCLUSION

In summary, the ultra-low-power on-chip training and inference of speech commands are demonstrated using the phase change memory (PCM)-based synaptic arrays. The power and latencies consumed during on-chip training (inference) are estimated to be 30 $\mu$W and 3000 sec (28 $\mu$W and 0.45 sec). Furthermore, at iso-accuracies, the number of multiply-and-accumulate operations (MACs) needed during the training of a deep neural network (DNN) model is found to be 269.23 $\times$ greater than the number of spikes required in our work. Similarly, during inference, the number of MACs needed during the inference of DNN is 70.36 $\times$ greater than the number of spikes required in our work. Overall, due to such low power and computational requirements, the PCM-based synaptic arrays can be promising candidates for enabling AI at the edge.

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### Table V

| Quantity | Our work | FCNNs |
|----------|----------|-------|
| Training method | Event-driven CD | Backpropagation with SGD |
| Total number of training images | 5000 | 5000 |
| Size of input image | 24×16 | 24×16 |
| Parameters | 209296 | 38476 |
| Epoch | 6 (batch size = 1) | 3 (batch size = 1) |
| Spikes/MACs during inference | 0.022 M | 1.548 M |
| Spikes/MACs during training | 172.51 M | 46.45 B |
