Area Optimisation of Two Stage Miller Compensated Op-Amp in 65 nm using Hybrid PSO

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Abstract—Analog circuit design can be formulated as a non-linear constrained optimisation problem that can be solved using any suitable optimisation algorithms. Different optimisation techniques have been reported to reduce the design time of analog circuits. A hybrid particle swarm optimisation algorithm with linearly decreasing inertia weight for the optimisation of analog circuit design is proposed in this study. The proposed method is used to design a two-stage operational amplifier circuit with Miller compensation. The results show that the proposed optimisation method can substantially reduce the design time needed for analog circuits.

Index Terms—Analog circuit design, area optimization, particle swarm optimisation algorithm.

I. INTRODUCTION

A NALOG circuit design has become an integral part in interfacing the real world signals with digital signal processing applications. There may be multiple analog interfaces to process signals such as voice, touch, motion, image, video, etc., present in a single chip. However, because of the shrinking device dimensions and the reducing supply voltages etc., analog circuit design has become increasingly complex. The highly nonlinear relationship between the circuit performance and design parameters has made analog design heavily dependant on the designer’s intuition and experience [1], [2]. To reduce this dependency, researchers are actively looking at automated analog circuit design as a solution. To automate a design, circuit sizing can be formulated as a non-linear constrained optimisation problem that can be solved using optimisation algorithms.

Many optimisation techniques have been reported in literature for the optimisation of analog circuits [3]. Gradient-descent based optimisation techniques [4] that have been reported for analog circuit optimisation involve the calculation of derivatives, and the optimal solution obtained is highly dependant on the initial guess for the design variables. Convex optimisation techniques reported for the automation of analog circuit design [5] result in a global optimum solution, but it requires a thorough understanding of the transistor models to design the constraints. Since the state-of-the-art transistors have really complex mathematical models, the problem becomes even more challenging. In recent studies [6], [7], Bayesian optimisation methods have been reported for automated analog circuit sizing. Another class of algorithms, called the evolutionary algorithms (EAs) have been reported to be used in analog circuit optimisation. EAs can give global solutions for complex optimisation problems. Moreover, EAs do not require the calculation of derivatives and can be applied to optimise complex systems. One such popular heuristics-based EA is particle swarm optimisation (PSO). PSO has been implemented in a wide range of real world problems because of its advantages such as robustness, simple representation, lesser number of adjustable parameters, ease of implementing parallel computation, and short computational time [8].

PSO has been reported to be used for the optimisation of circuit sizing problems in different studies. Studies also show that PSO can be combined with other optimisation techniques for area optimisation of analog circuits [9], [10]. In [11], a modified version of PSO called hierarchical PSO has been used to optimise the component sizing of various analog circuits and has been found to give solutions with better repeatability when compared to PSO. PSO algorithm has been reported in [12] to be used for the area optimisation of a two-stage operational amplifier (op-amp). Simulation results have proven that the PSO-based design met all design specifications and also gave a better result in terms of area with respect to the convex optimisation method. A modified PSO algorithm has been used for area optimisation of a complementary metal oxide semiconductor (CMOS) differential amplifier while considering design specifications of gain, phase, power dissipation, area occupied, etc., in [13]. A craziness based PSO reported in [14] has been found to give better results for the area optimisation of a CMOS two-stage op-amp than other reported techniques.

In this paper, a hybrid PSO with linearly decreasing inertia weight is proposed for the area optimisation of analog circuits. A particle generation function is used to generate the particles in the swarm together with a survivability test to ensure that the particles meet all the circuit requirements. In this study, the decision vector has been formulated with transistor widths and the bias current. The circuit specifications are considered as the constraints for the optimisation problem. We have used the proposed optimisation technique to design a two-stage op-amp with Miller compensation.

II. OVERVIEW

Formulation of the analog circuit optimisation problem and an overview of the standard PSO are given in this section.

A. Problem Formulation

Analog design deals with trade-offs between various circuit parameters such as noise, linearity, gain, supply voltage, voltage swing, speed, input/output impedance, and power dissipation [1]. Such trade-offs create many challenges in the analog circuit design procedure that requires experience.
and intuition to get optimal circuits. It can be said that such trade-offs along with specific circuit requirements make the analog design procedure a multidimensional optimisation problem, that has a solution space rather than a single solution. All analog circuit designs can be considered as optimisation problems with the design parameters as the design variables and the circuit specifications as constraints. The expression for the fitness function depends on the circuit parameters that need to be optimized for a particular analog design.

The primary objective of an optimisation problem is to determine a vector \( \mathbf{x} = [x_1, x_2, x_3, \ldots, x_n] \), called the position vector, that minimizes or maximizes a fitness function, \( f(\mathbf{x}) \). \( \mathbf{x} \) is an \( n \)-dimensional vector, where \( n \) represents the number of decision variables, the values of which have to be determined in the optimisation problem. The value of the fitness function, \( f(\mathbf{x}) \), gives a measure of how good a particular solution represented by \( \mathbf{x} \) is. The set of all possible solutions constitute the search space for an optimisation problem.

The main goal of our work is to optimise analog circuits in terms of area i.e., optimal sizing of transistors. The proposed optimisation method is used to design a two stage Miller compensated op-amp. A schematic of the op-amp is shown in Fig. 1. Its first stage comprises a differential amplifier, with an NMOS input stage consisting of \( M_1 \) and \( M_2 \) and a PMOS current mirror load consisting of \( M_3 \) and \( M_4 \). A current mirror consisting of \( M_5 \) and \( M_6 \) is used to bias the first stage. The second stage is a common source amplifier with a PMOS input stage, \( M_8 \) and an NMOS current source load, \( M_7 \).

In Fig. 1 we have assumed that the transistors \( M_1 \) and \( M_2 \), \( M_3 \) and \( M_4 \), and \( M_5 \) and \( M_6 \) are matched such that \( W_1 = W_2 \), \( W_3 = W_4 \), and \( W_5 = W_8 \). The bias current is denoted as \( I_{bias} \). Since our objective is to minimize the chip area while meeting all other design specifications, the bias current \( I_{bias} \) is used to bias the first stage. The area of the circuit is chosen as the fitness function. The bias current and the widths of the transistors are taken as the decision variables for the optimisation problem. Specifications such as minimum voltage gain \((A_{v,min})\), minimum cut-off frequency \((f_{dB,min})\), minimum unity gain-bandwidth \((UGB_{min})\), maximum power dissipation \((P_{max})\), minimum slew rate \((SR_{min})\), input common-mode range \((ICMR)\), maximum area \((A_{max})\), minimum phase margin \((PM_{min})\), and maximum noise \((S_{n,max})\) are taken as constraints for this problem. The position vector, \( \mathbf{x} \), comprising the decision variables, and the fitness function, \( f(\mathbf{x}) \), can be expressed as

\[
\mathbf{x} = [W_{1,2}, W_{3,4}, W_{5,8}, W_6, W_7, I_{bias}] \quad \text{and} \quad f(\mathbf{x}) = \sum_{i=1}^{n} W_i \times L_i, \tag{1}
\]

respectively, where \( M \) is the total number of transistors in the circuit and \( W_i \) and \( L_i \) are the width and length, respectively, of the \( i \)-th transistor. For the circuit under consideration, \( M = 8 \).

**B. Overview of PSO**

PSO algorithm, introduced by Kennedy and Eberhart in 1995 [15], is inspired by the intelligent collective behavior of a swarm of animals such as a flock of birds or a school of fishes. Typically, these swarms work towards a common goal where each member continuously alters its trajectory based on individual experience as well as that of other members.

In the standard form of PSO, the system is initialized with a population/swarm of particles, with each particle representing a potential solution. Initial positions of the particles are assigned by random values within the bounds of the solution space as defined in the optimisation problem. Trajectory and position of each particle change with each iteration where they are updated based on the particle’s current position, the best position in its history, and the global best position that any of the particles in the swarm has ever attained. Let the position vector, \( \mathbf{x}_k \), denote the position of a particle, and the velocity vector, \( \mathbf{v}_k \), represent the velocity of the particle, where \( k \) is the index of the particle. Throughout the iterations, each particle remembers its individual best position and the global best position, i.e., the best solution of the swarm. If the number of particles in the population is \( N \) and the dimension of the search space is \( D \), then the position of the \( j \)-th particle in the \( i \)-th iteration is represented as

\[
\mathbf{x}_{i,j} = [x_{1,1}, x_{2,1}, x_{3,1}, \ldots, x_{D,1}], \quad j = 1, 2, \ldots, 8, \quad i = 1, 2, \ldots, n. \tag{2}
\]

For every iteration, the velocity and position of each particle are updated using the equations

\[
v_{i,j+1} = w v_{i,j} + c_1 r_1 (p_{i,j} - x_{i,j}) + c_2 r_2 (g_{j} - x_{i,j}) \quad \text{and} \quad x_{i,j+1} = x_{i,j} + v_{i,j+1}, \tag{3}
\]

where \( w \) is the inertia weight, \( v_{i,j} \) is the velocity of the \( i \)-th particle in the \( j \)-th iteration, \( p_{i,j} \) is the best position of the \( i \)-th particle so far, \( g_{j} \) is the global best position among all the particles, \( r_1 \) and \( r_2 \) are two random numbers uniformly distributed in the interval \([0,1]\), and \( c_1 \) and \( c_2 \) are the constriction factors that are used to control and constrict the velocities. The iteration is repeated until all the particles have converged to the position representing the optimum solution.

**III. PROPOSED OPTIMISATION METHOD**

Details of the proposed optimisation technique and its application in the design of a two stage op-amp with Miller compensation are discussed in this section. Results of proposed method used for the area optimisation of a differential amplifier circuit are reported earlier in [16].
A. Particle Generation Function

Particles of the initial population as well as the subsequent iterations are generated using a particle generation function. A flow diagram depicting the particle generation function is given in Fig. 2. As shown in step (a), the maximum and minimum bounds for the design variables are fixed using the design specifications listed in Table 1 and saturation conditions of the transistors using the I-V characteristics of the transistors. Random values are picked from these bounds for each of the design variables to create a particle, as illustrated in step (b). In step (c), the generated particle is made to undergo a survivability test. If the particle fails the test, it is discarded and the process is repeated until a suitable particle is obtained. Here, fixing the bounds for the design variables using the design specifications and the saturation conditions increases the probability of a particle passing the survivability test. This results in substantial reduction of time required to generate a particle.

B. Survivability Test

A particle is made to undergo a survivability test to determine whether it is meeting all the design specifications and saturation conditions of the transistors in the circuit. The survivability test is carried out using ngspice simulations. A flow diagram showing steps in the survivability test is given in Fig. 3. The op-amp circuit that is being optimised is simulated using ngspice with the design parameters represented by each particle, as shown in step (a). In step (b), DC operating point analysis, AC analysis, and noise analysis are carried out. The circuit is then checked for saturation conditions as well as the required specifications, as illustrated in step (c).

C. Hybrid PSO with Linearly Decreasing Inertia Weight

Variants of the standard PSO have been used in multiple applications. One such variant is the PSO with linearly decreasing inertia weight. In this variant, the inertia weight, $w$, is varied linearly between $w_{\text{max}}$ and $w_{\text{min}}$ over the iterations [17], [18]. This modification of the inertia weight ensures global exploration in the initial iterations, thereby maximising the probability of finding a global solution. A lower inertia weight towards the final iterations results in local exploration that helps in faster convergence to the optimal solution. This variant of PSO is found to give better results for our optimisation problem. Since the values of $w_{\text{max}}$ and $w_{\text{min}}$ are highly problem dependant, we have chosen the set of values giving consistent results for multiple runs with the best optimal value for the fitness function.

A pictorial representation of the proposed hybrid PSO algorithm is given in Fig. 4. The main difference of the proposed method from the standard PSO is how the velocity of each particle is getting updated in every iteration. For the proposed hybrid algorithm, the position vector and the fitness function are the same as (1) and (2). The position and velocity update equations are given in (4) and (5). The particles passing the survivability test are shown in green and inside the bounds, and those which are failing are shown in red and as out of bounds in the figure. In this variant of PSO, the initial swarm is generated using the particle generation function, as shown in step (a) in the figure. In every iteration, after updating the position of each particle, the particle is made to undergo the survivability test. This is illustrated in step (b) in the figure, in which two particles are shown as out of bounds. Unlike standard PSO, for the particles out of bounds, velocity and position updates are carried out again using equations (4) and (5). These particles are subjected to the survivability test once more. If they fail the test, the above process is repeated either until suitable particles are obtained or the number of velocity updates reaches a predefined limit. Even after this limit, if the particles are unable to pass the survivability test, new particles generated using the particle generation function are introduced in their place. The multiple velocity updates for particles that are out of bounds is shown in step (c). This is carried out for all the particles throughout the iterations. Then the particle parameters are updated as shown in step (d). The next iterations are implemented in the same manner till the stopping criteria for the optimisation algorithm are met.

The repeated updates to the velocity in a single iteration in the proposed hybrid PSO is found to be helpful for this...
Algorithm 1 The proposed hybrid PSO.

1) Particle generation function
   a) Generate particle.
   b) Conduct survivability test for the particle.
   c) If the test fails, go to 1a. Else, exit the function.

2) Main algorithm
   a) Initialise PSO parameters: $w_{\text{max}}$, $w_{\text{min}}$, $c_1$, $c_2$, $N$, $i = 0$, $ite = 0$, count = 0, maxite, maxcount.
   b) Generate initial swarm.
      i) If $i > N$, go to step 2c. Else, continue.
   c) Conduct survivability test for the particle.
   d) Begin iterations: Set $ite = 0$, $i = 0$, count = 0.
      i) If $ite > maxite$, go to step 2e. Else, continue.
      ii) Update $i = i + 1$ and go to step 2b-i.
   d) Conduct survivability test for the particle.
   e) Update initial velocity, fitness values, pbest, and gbest of the swarm.
   g) If the test fails, go to 1a. Else, exit the function.
   h) Generate particle.
   i) If the test fails, go to step 2d-v. Else, continue.
   j) Update initial velocity, fitness values, pbest, and gbest.
   k) Update velocity and position of the particle. Set count = count + 1.
   l) If count > maxcount, call particle generation function.
   m) Conduct survivability test for the particle.
   n) If the test fails, go to step 2d-x. Else, continue.
   o) Update fitness value, pbest, and gbest.
   p) Update $ite = ite + 1$ and go to 2d-i.
   q) Update best fitness and the optimal solution.

TABLE I
SPECIFICATIONS USED FOR THE TWO STAGE OP-AMP DESIGN.

| Specification               | Value                        |
|-----------------------------|------------------------------|
| Voltage gain ($A_v$)        | $\geq$ 20 dB                 |
| Power dissipation ($P$)     | $\leq$ 400 $\mu$W            |
| Slew Rate ($SR$)            | $\geq$ 100 $V/\mu$s$^{-1}$   |
| Cut-off frequency ($f_{\text{DC}}$) | $\geq$ 10 MHz              |
| Unity gain bandwidth ($UGB$) | $\geq$ 100 MHz             |
| Phase margin                | $\geq$ 60°                   |
| Input common-mode ($V_{\text{in,CM}}$) | $0.6 V \leq V_{\text{in,CM}} \leq 1.0 V$ | |
| Power spectral density ($S_n(f)$) | $\leq 60 nV/\sqrt{Hz}$ at 1 MHz  |
| Area ($A$)                  | $\leq 1 \mu m^2$            |
| Load capacitance ($C_L$)    | 200 $fF$                     |
| Transistor sizes ($W/L$)    | 2 to 200                     |

![Fig. 5. PSO convergence characteristics for 10 runs with 100 iterations.](image)

TABLE II
OPTIMUM PARAMETERS OBTAINED FOR TWO STAGE OP-AMP.

| $I_{\text{bias}}$  | $W_{1,2}$ | $W_{3,4}$ | $W_{5,6}$ | $W_7$ |
|-------------------|-----------|-----------|-----------|-------|
| 29.7 $\mu$A       | 206 nm    | 783 nm    | 126 nm    | 1115 nm | 191 nm   |

TABLE III
OPTIMUM PARAMETERS OBTAINED FOR THE TWO STAGE OP-AMP.

| Design Criteria       | Specifications | MC Results |
|-----------------------|----------------|------------|
| $A_v$                 | $\geq$ 20       | 21.6       | 1.34      |
| $f_{\text{DC}}$       | $\leq$ 10       | 13.9       | 1.6       |
| $UGB$                 | $\geq$ 100      | 169.7      | 4.6       |
| Phase Margin ($\phi$) | $\geq$ 60       | 62.4       | 2.64      |
| $SR$                  | $\geq$ 100      | 288        | 47        |
| $P$ ($\mu$W)          | $\leq$ 150      | 89         | 20        |
| $S_{n}(f)@1$MHz       | $\leq$ 60       | 53         | 0         |
| $S_{n}(f)@10$MHz      | $\leq$ 19       | 0          |           |
| CMRR (dB)             | $\geq$ 35.5     | 9.1        |           |
| PSRR$+$ (dB)          | $\geq$ 20.8     | 2.9        |           |
| PSRR$-$ (dB)          | $\geq$ 49.2     | 9.4        |           |
| Settling time with 2% tol. (ns) | $\leq$ 5.4     | 0.84       |           |
| Settling time with 5% tol. (ns) | $\leq$ 4.3     | 0.49       |           |
| $A$ ($\mu m^2$)       | $\leq$ 1        | 0.22       |           |

IV. SIMULATION RESULTS

The design specifications used for the two stage op-amp are given in Table I. The circuit is designed in 65 nm technology. The supply voltage, $V_{DD}$, is taken as 1.1 V. The length of all the transistors is fixed to 60 nm. The PSO parameters are taken as: $w_{\text{min}} = 0.5$, $w_{\text{max}} = 0.8$, and $c_1 = c_2 = 1.7$. To ensure a phase margin of 60°, the value of $C_c$ is taken as 0.3 times $C_L$.

Fig. 3. The proposed optimisation algorithm is implemented in Matlab with the survivability test performed using ngspice simulations. The algorithm is run multiple times with swarm sizes of 10, 15, and 20 for 100 iterations in each run. From the simulations, it is observed that the variance of the converged value of the fitness function decreases with increasing swarm size. Hence, a swarm size of 20 is chosen. The PSO convergence characteristics for 10 runs with 100 iterations with a swarm size of 20 are shown in Fig. 3. From the runs, the best value in terms of the fitness function is taken as the final solution, and the circuit parameters corresponding to these values are found out. The design parameters of the final solution obtained are given in Table II. The optimal solution is found to meet all the required specifications in the ICMR of 0.6 V to 1 V. The results for the Monte Carlo simulations for the optimal design for 1000 runs across various PVT corners are summarized in Table III.

The comparison of results of the proposed method and other reported studies in 350 nm [12] and 180 nm [19] technologies...
for the two stage op-amp are summarised in Table IV. It can be seen that the proposed algorithm gives a better optimal area than the ones reported in [12, 19]. The proposed method has been used for the design of the op-amp reported in [19] for an unconstrained optimisation in 180 nm technology and the comparison with the reported Bayesian optimisation method is given in Table V. It shows that the proposed technique converges to a higher fitness function value showing a better performance. The proposed algorithm converges to the optimal value in less than 50 iterations for all the considered cases.

### Table IV

| Design Criteria (µm²) | 350 nm Technology | 180 nm Technology |
|----------------------|-------------------|-------------------|
| PSO This work        | specs.            | PSO This work     |
| $A_{in}$ (dB)        | $\geq 60$         | $\geq 50$         |
| $UGB$ (MHz)          | $\geq 3$          | $\geq 10$         |
| Phase Margin ($^\circ$) | $\geq 45$       | $\geq 45$         |
| $SR$ (V $\mu s^{-1}$) | $\geq 10$         | $\geq 10$         |
| $P$ (mW)             | $\geq 2.5$        | $\leq 1$          |
| $CMRR$ (dB)          | $\geq 60$         | $\geq 60$         |
| $PSRR_{+}$ (dB)      | $\geq 70$         | $\geq 60$         |
| $PSRR_{-}$ (dB)      | $\geq 70$         | $\geq 60$         |
| $Vin,CM_{max}$ (V)   | $\leq 2$          | $\leq 2$          |
| $Vin,CM_{min}$ (V)   | $\geq -1.5$       | $\geq -1.5$       |
| $V_{DD}$ (V)         | $= 2.5$           | $= 1.8$           |
| $V_{SS}$ (V)         | $= -2.5$          | $= 0$             |
| $C_L$ (pF)           | $= 10$            | $= 1$             |
| $A$ (µm²)            | $\leq 300$        | $\leq 300$        |

### Table V

| Algorithm   | Best   | Worst  | Mean   | Std    |
|-------------|--------|--------|--------|--------|
| MACE [19]   | 690.36 | 690.27 | 690.34 | 0.03   |
| This work   | 2100.1 | 2100.1 | 2104.8 | 2.9    |

V. CONCLUSION

In this paper, a hybrid PSO with linearly decreasing inertia weight suitable for the optimisation of analog circuit sizing is proposed. The proposed method is used to design a two-stage op-amp with Miller compensation in 65 nm technology, and the simulation results are presented. The optimal solution obtained is found to meet all the required circuit specifications. The study shows that the proposed method can substantially reduce the design time required for analog circuits. The method can be used to optimise more complex analog circuits and for multi objective optimisation problems.

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