Dynamic Power Reduction in a Novel CMOS 5T-SRAM for Low-Power SoC

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Abstract — This paper addresses a novel five-transistor (5T) CMOS SRAM design with high performance and reliability in 65nm CMOS, and illustrates how it reduces the dynamic power consumption in comparison with the conventional and low-power 6T SRAM counterparts. This design can be used as cache memory in processors and low-power portable devices. The proposed SRAM cell features ~13% area reduction compared to a conventional 6T cell, and features a unique bit-line and negative supply voltage biasing methodology and ground control architecture to enhance performance, and suppress standby leakage power.

Keywords: Five-transistor SRAM; low-power low-area SRAM; cache memory; standby and dynamic power reduction.

1 INTRODUCTION

Today’s microprocessor chips consist of cache memories and computing cores. It is predicted that cache memories may reach 90% of the chip area in some applications by 2013 [4]. In addition, cache memories consume a significant portion of the power budget in SoC applications [3]. This is particularly important in portable and battery-powered electronics such as cellular phones, PDAs, wireless, and low-power biomedical devices since dynamic and standby leakage power determine the battery life. With recent aggressive growth of technology scaling, standby leakage power is increased nearly five times each technology generation while active power remains constant [3]. Also, process variations and hence performance fluctuations are widely noticed in 65nm and beyond in CMOS technologies [5]. Five-transistor Static Random Access Memories (5T SRAMs) are attractive due to their advantage in area and power efficiency compared to 6T SRAMs [1][2][8][9][16]. Research in the past on this type of memory has been mostly focused on improving performance and stability while maintaining the promised area saving in a particular technology node. On the other hand, with continuous scaling down of CMOS transistors, new techniques have been developed in 6T SRAMs such as Dynamic Standby Mode [4][12], DRV method [3], and well biasing, some of which are summarized in [3] and [4]. Therefore, in order to suppress leakage power consumption and combat performance fluctuations due to process variations, the previous research in 5T SRAMs such as [8] and [9], can no longer compete with current 6T SRAMs and that is why 6T SRAMs are still predominantly used in current systems.

In [1], standby power reduction has been described for the new 5T SRAM design. In this paper, an improved low-power design with the focus on its dynamic power reduction advantage is addressed. The new 5T SRAM cell with dual grounds (5TSDG) features a novel bit-line biasing technique, and guarantees operation under all process variations and temperatures while taking benefit of area reduction. In addition, 5TSDG has an improved performance compared to previous research in [2][8][9].

This research is supported by CMC Microsystems and funded in part by NSERC of Canada.

![Fig. 1](image-url) (a) Conventional 6T SRAM cell, (b) Proposed 5T SRAM cell (5TSDG), (c) 5T SRAM architecture (M cells/sub-column) with sub-column circuitry and $V_{SSM}$ control.
TABLE I. Different types of SRAM cells used in this paper, $V_{DD} = V_{DDM}=1.3V, \beta = (W_N/S)/(W_P/S)$. 

| Type      | Inverter Tr.'s | Access Tr.'s | $\beta$ | $V_{SSM}$ | BL pre-charge |
|-----------|----------------|--------------|---------|-----------|---------------|
| 5TSDG     | HVT            | SVT          | 1.0     | 600mV     | 600mV         |
| Low-Power 6T | HVT          | SVT          | 1.4     | 600mV     | $V_{DD}$      |
| Conv. 6T  | HVT            | SVT          | 1.4     | 0mV       | $V_{DD}$      |

2 5TSDG DESIGN

A conventional 6T cell in comparison with the 5TSDG is demonstrated in Fig. 1 (a) and Fig. 1 (b) respectively. A block diagram of 5TSDG including the sub-column circuitry is depicted in Fig. 1 (c). Standby and Ground control circuits are required per every sub-column while $V_{SSM}$ control is shared in the entire memory array. TABLE I specifies some of the design parameters of 5TSDG, low-power 6T, as well as conventional 6T cells used in this paper for comparison. An area reduction of ~13% is predicted compared to a conventional 6T cell using standard 65nm design rules [1].

The “portless” 5T SRAM in [16] does not use a dedicated read-write port transistor, but has an “access transistor” that shorts Q and $Q_2$ nodes during read and write. $V_{DDM}$ nodes are replaced by dual bit lines for I/O and power reduction. A detailed comparison between 5TSDG and the portless 5T SRAM of [16] would be useful future work. The portless design appears to need larger PMOS and access transistors than 5TSDG.

2.1 Standby Mode

One of the effective and proven methods to suppress leakage power during standby in 6T SRAMs is to use dynamic sleep design while maintaining a sufficient Static Noise Margin (SNM), which ultimately determines the integrity of the stored data [4][6]. The most effective way to use this method is by raising the negative supply voltage of the memory cells, $V_{SSM}$, as opposed to lowering the positive one, $V_{DDM}$, to minimize bit line and cell leakage power [1][4][12].

Considering this method in 5T SRAM, a prominent feature of 5TSDG that makes it different from previous research work is that $V_{SSM}$ can also be used to pre-charge the bit line, BL, in standby via $M_{dsh}$, as shown in Fig. 1 (c) so that 1) channel and gate leakage through $N_3$ is reduced and minimized by up to 90% especially when a ‘0’ is stored, and 2) the cell maintains a reasonable Read Noise Margin (RNM) when accessed close to the optimum achievable point and 3) To accelerate read/write operation explained in the next sections.

TABLE II shows standby leakage current and worst case RNM for various types of SRAM cells introduced in TABLE I. Fig. 2 compares the power consumption of 5TSDG including peripheral circuits with a low-power 6T design in various process corners. Traditional 5T designs as in [8][9], where $V_{SSM}$ is held at $V_{SS}$ level, require lower $V_{in}$ for internal cell transistors in 65nm technology, such as $N_1$, and $P_2$ (Fig. 1), to enable write ‘1’ operation discussed in section 2.4. Thus, even though some leakage power is saved by cutting a bit line and biasing the other to a lower voltage, the overall leakage is quite high, being about half of the conventional 6T cell value in TABLE II.

TABLE II. Leakage current and RNM comparison in different SRAM types (not including peripheral circuits)

| Type       | Leakage (nA) | RNM (mV) |
|------------|--------------|----------|
| 64 cells   | 80.6         | 172.3    |
| 5TSDG      | 88.7         | 123.2    |
| Low-Power 6T | 2020.0     | 123.2    |
| Conventional 6T | 2020.0     | 123.2    |

Using two carefully sized diode-connected transistors, $M_i$ and $M_2$, the voltage across the cell in standby can be biased to remain static for various temperatures and process corners (See also [14]). In this design, a minimum voltage across the cell, $V_{min} = V_{DDM} - V_{SSM}$, of 0.7V is selected to yield sufficient stability [7], resulting in a simulated SNM between 181-222mV in all corners and temperatures at $V_{DDM}=1.3V$ [10]. A 64Kbit memory array arranged in 64x16 blocks was simulated in standby mode using BSIM v.4 and HSPICE at $V_{DD}=V_{DDM}=1.3V$. The large capacitance of $V_{SSM}$ consisting of mostly junction and wire capacitors and sufficient available leakage current are the key factors in stability of $V_{SSM}$ during standby/write/read modes. In case of lack of leakage especially due to HVT transistors, in some corners or temperatures, $M_1$ is turned on more strongly to provide the charges to $V_{SSM}$. During read and write operations, $V_{SSM}$ remains within 20mV of the standby steady state value.

Another unique feature of 5TSDG that makes it different from previous research work is that $V_{SSM}$ can also be used to pre-charge the bit line, BL, in standby via $M_{dsh}$, as shown in Fig. 1 (c) so that 1) channel and gate leakage through $N_3$ is reduced and minimized by up to 90% especially when a ‘0’ is stored, and 2) the cell maintains a reasonable Read Noise Margin (RNM) when accessed close to the optimum achievable point and 3) To accelerate read/write operation explained in the next sections.
2.2 Read Operation

The read operation is similar to a 6T SRAM except that only one bit line is used. In 5TSDG, the bit line is pre-charged in standby by $V_{SSM}$ which is near the optimum point to maximize RNM in the worse case (FS). Another advantage of this pre-charge method compared to [9] is that it does not require an additional power supply on chip such as a DC-DC converter or a level shifter which will add to the chip area and power consumption. A simple sense amplifier circuit used in 5TSDG is shown in Fig. 3 (b). Although not the fastest type, it is attractive due to its simplicity and that it does not need a clock signal [13]. During read, rd signal in Fig. 1 (c) is raised causing $V_{g1}$ and $V_{g2}$ to be pulled down to $V_{SS}$ by $M_{selrd}$ and $M_{selrd}$, which will maximize RNM and read performance. The global bit line, Gbit, is the output of the sense amplifier and is pre-charged to $V_{SSM}$ through $M_6$ in standby and is pulled down to $V_{SS}$ by $M_6$ during a read ‘0’. Therefore, a read ‘1’ is always implied unless Gbit is pulled down. Inverter $M_6$ should have a sufficient noise margin to prevent a false trigger. This sense amplifier can be shared by two bit lines from two adjacent sub-columns. For instance, in a 128-cell column composed of two 64 cell sub-columns, the sense amplifier is placed in between bit lines BitL and BitR. SelL and SelR signals should be selected by a row decoder to select the appropriate bit line to read from. $M_1$ and $M_4$ are used to pre-charge the input of the inverter $M_2-M_5$ in standby. For similar bit line capacitances, read speed in 5T and 6T SRAMs is comparable.

Fig. 4 (a) shows simulation results of the read operation in a conventional 6T cell using a sense amplifier shown in Fig. 3 (a). In this simulation, WL pulse is artificially generated such that BL reaches about $V_{DD}/2$ in read for power saving reasons. Gbit and Gbitz are the outputs of the sense amplifier, and are pre-charged high using prez pulses before the read operation.

Fig. 4 (b) demonstrates the read operation of 5TSDG using a sense amplifier shown in Fig. 3 (b) in a 64Kbit memory array arranged in 64x16 bit blocks for two neighboring cells sharing the same word line, WL, storing a ‘0’ and a ‘1’ on Q0 and Q1 nodes, and having two bit lines BL0 and BL1 respectively. Gbit load in 5TSDG is the same as that in Gbit and Gbitz in the 6T counterpart. Q0-Q0z-BL0-Gbit0 and Q1-Q1z-BL1-Gbit1 are related to a cell in 5TSDG storing a ‘0’ and ‘1’ respectively and sharing the same word-line (WL).

A dynamic increase in Q0 node occurs while reading a ‘0’ due to the current flow from the bit line to $N_3$ and $N_3$ as the word line is raised and as shown in Fig. 4 (b) ($Q_{max}$). During read ‘1’ a drop of voltage in Q1 node is observed for a similar reason ($Q_{min}$). $Q_{max}$ and $Q_{min}$ should not cause a read upset i.e. they should be less and more than the tripping voltage of the inverter pairs, respectively, to avoid turning a read into a write, especially in FS corner. To further reduce the probability of read-upset in 5T, it is possible to increase word-line rise time and make the bit lines shorter to reduce their capacitances [2]. The latter may also improve read speed by reducing bit line swing delay.
TABLE III shows the trip voltage vs. Qmax and Qmin while reading in different corners in 5TSDG. These results when compared with RNM measurements for various mismatch cases in worst case corner FS, show the stability of 5TSDG. RNM is measured with VSSM on the bit line similar to [9]. The best biasing voltage for VSSM maximizes RNM for the FS corner.

| 5T Cell | Trip point voltage (mV) / Qmax (mV) |
|---------|--------------------------------------|
| FF      | 883/193                              |
| SF      | 686/185                              |
| TT      | 934/202                              |
| SS      | 899/195                              |
|         | 905/196                              |

2.3 VSSM Stability in Dynamic Mode

During standby mode of the 5TSDG cell, VSSM is used as a power supply to raise Vg1 and Vg2 above VSS and pre-charge the bit-line. During read operation, Vg1 and Vg2 are driven to VSS to maximize RNM and the read speed. On the other hand, after a read operation is completed, Vg1, Vg2 and the bit-line are driven back to VSSM since the memory cell will be in standby again. This voltage swing of Vg1, Vg2 and the bit-line affects voltage level of VSSM since each re-charge of these voltages takes charges away from VSSM causing it to drop by an amount of ∆V, where i is the index of consecutive read operations. In a case of reading a ‘1’, the bit line will actually add charges to VSSM but that amount is much less than the effect of the ground lines taking away charges after being driven low for a read. Fortunately, VSSM is highly capacitive with much higher capacitance than Vg1 and Vg2, and many memory cells in standby provide electric charges to it. Therefore, VSSM changes very little during read operation especially when it has large capacitance (attached to large memory arrays), and even if it does, it will actually help the read operation in terms of performance and read noise margin (see Fig. 5). In addition, VSSM does not decrease beyond a steady-state value, and when reading is complete, it is pulled back towards its standby level due to an increase in memory cell leakage (see Fig. 6 and Fig. 7).

C(SubCol) = (NＢ0 + NＢ1)(CBL + CVg1 + CVg2),

Cg1, Cg2, CBL, and are the capacitances of Vg1, Vg2, and the bit-line respectively. It is assumed that Vg1 and Vg2 have been driven to 0V initially. VBLg and VBLs are the bit-line voltages after a read ‘0’ and a read ‘1’ respectively. NＢ0 and NＢ1 are the number of ‘0’ and ‘1’ bits in a word respectively (16 bits/word in the simulation results of this paper). In standby, C(SSM(stby)) includes the capacitance of all sub-column connections, and VSSM interconnections. During read, a single sub-column with capacitance of C(SubCol) is removed. iavg(i) is the average memory leakage current over the i-th read cycle period, ∆t. It is increased as VSSM is reduced. Similarly, VSSM(i) is the VSSM voltage at the end of the i-th read cycle. As the memory array size is increased, φ(i) approaches to one since C(SSM(read)) approaches C(SSM(stby)). Part of ∆V_i is caused by a small amount of overlap between rd and stby signals in Fig. 4 (b).

This effect on VSSM occurs also in write operation when the bit-lines are charged and discharged. However, for explanatory purposes, read operation, which is the most severe, is selected to be demonstrated. The number of cells per bit-line and number of bits per word also contribute to this effect.
this problem,\[9\] studied a W1 using NMOS, which
performed in a similar way. On the other hand, in W1, the bit
storage node is pulled down when W1 is at V\textsubscript{SS} and is at V\textsubscript{SS} otherwise. The role of this transistor is
to limit the disturb \(\Delta V_g = V_{g2} - V_{g1}\) as shown in Fig. 9 to improve SNM of the disturbed cells in the same sub-column. The strength of \(M_{eq}\) is chosen through simulation to limit write disturb for all process corners especially for fast NMOS corner cases [2]. This disturbance can also be minimized by reducing the write pulse period to its limit. In summary, in W1, \(N_1\) will have a stronger current drive than \(N_2\) since its \(V_{DS}\) is maximized i.e. increased by \(V_{SS}\).

The threshold voltage of the access transistor, \(V_{th}\), plays a key role in W1 performance. Simulation results reveal that the access transistor can be between the HVT and LVT for \(N_3\). In order to improve W1 performance, \(V_{th}\) of \(N_3\) can be reduced with some loss of SNM. In 5TSDG, \(V_{th}\) of \(N_3\) can be between the HVT and LVT to maintain a reasonable RNM/W1 performance as shown in TABLE IV (for W1 delay measurement see Fig. 9). RNM can be further increased by reducing bit-line capacitance and/or increasing word-line rise time [2].

| \(5T\) Cell RNM (mV) | \(W1\) Delay (ps) for Various \(N_3\) \(V_{th}\) |
|----------------------|-------------------------------|
| LVT (~230 mV)        | 144.1/96.8                    |
| SVT (~440 mV)        | 172.3/116.4                   |
| HVT (~600 mV)        | 225.1/170.6                   |

![Fig. 9 W1 operation of 5TSDG cell in slow corner (SS) (120°C)](image)
Therefore, to improve read stability and write-ability (particularly W1), the solution is to find a reasonable mid-point considering the fact that N3 does not play a key role in standby power consumption. Limited to three choices for Vth selection, SVT for N3 is reasonable as shown in TABLE IV. However, in chip foundries, even a lower threshold somewhere between LVT and SVT can be achieved by changing gate oxide thickness. Fig. 11 compares W0 and W1 performance of 5TSDG with a low-power 6T SRAM described in TABLE I. For both cases, W1 delay is measured from when WL = 50%VDDM to when Q=80%VDDM, and W0 delay is measured similarly but when Q=20%VDDM above VDD. This measurement is different from what was reported in TABLE IV (word-line to Q-z cross point). W1 can be ~11-31% slower than a conventional 6T design and can be improved by reducing Vth of N3. W0 performance is similar to conventional 6T design.

Fig. 10 (a) shows how the voltage of Vg1 in W1 can affect SNM on disturbed cells while driving Vg2 at a fixed voltage (at VSSM) mimicking that there is no Mep. Fig. 10 (b) demonstrates the reverse scenario where Vg1 is fixed at 0V, and Vg2 varies from 0V to VSSM. Similarly, this figure shows that with no weak equalization between Vg1 and Vg2, the disturbed cells are susceptible to data corruption due to environmental disturbances. The strength of Mep will determine the limitation on this disturbance by both lowering Vg2 from VSSM and not allowing Vg1 to be pulled down so much. In 5TSDG, Mep was ratioed such that the W1 disturbed SNM was greater than ~50mV.

![Fig. 10 SNM in W1 disturb cells vs. Vg1 and Vg2 voltages](image)

The write margin of the proposed 5T SRAM design can be divided into W0 margin (W0M), and W1 margin (W1M) since as opposed to the 6T cell counterpart, W0 and W1 have different WMs. One of the common methods to measure WM in conventional 6T SRAMs is by measuring the maximum BL voltage able to flip the cell state [15]. For 5TSDG, W1M is defined to be the difference between the positive supply voltage, VDDM, and the minimum BL voltage able to write a ‘1’ into the cell while W0M is defined to be the maximum BL voltage able to write a ‘0’ into the cell. In the 5TSDG (VDDM=1.3V), for a typical-temporal corner (TT), W1M is ~0.5V, and W0M is ~0.4V.

3 DYNAMIC POWER CONSUMPTION

Dynamic power consumption of 5TSDG can be divided into read and write power. Power consumption during read is a function of Vmin, which determines VSSM biasing level. During several consecutive reads, Vg1 and Vg2 in Fig. 1 are driven to VSS and VSSM frequently. Active power consumption is changed as supply voltage is changed due to the square law dependency. This power is also dependent on the frequency of VSSM swing during read. Equation 2 shows the dynamic power consumed due to the voltage swing of the ground lines of 5TSDG, where CL is the summation of Vg1 and Vg2 capacitances, ΔV is VSSM-VSS and f is the frequency of voltage swing.

\[ P_{dyn} = C_L \Delta V^2 f \]  

Equation 2

Reading a ‘0’ (R0) consumes more power than reading a ‘1’ (R1) since in R0, the bit-line is pulled sufficiently low to trigger the sense amplifier, and the global bit-line of the sense amplifier is also pulled down. In R1, bit-line is only required to be pulled high enough to avoid activating the sense amplifier, and the global bit-line stays at VSSM. Fig. 12 shows read power and standby power for various VDDM values while keeping Vmin=VDDM-VSSM constant at 0.7V for a 64x16 bit block of 5TSDG. As VDDM is increased, VSSM also increases accordingly causing ΔV in equation 2 to increase during read operation. Therefore, read power is increased quadratically with higher VDDM.

![Fig. 12 Comparison of normalized read and standby power vs. VDDM for 5TSDG cell, 64x16 bit block, reading 16 ‘0’s continuously from 16-bit words (FF corner, 120℃)](image)
Fig. 13 demonstrates case study results of worst-case (FF, 120°C) normalized power consumption in standby mode, read, and write operations of 5TSDG in comparison with low-power 6T design. Other corners have similar results comparable to Fig. 2. Read power consists of standby power of the idle memory cells, and the dynamic power described by equation 2. In this case study where a 64Kbit array consisting of 64x16 bit blocks was studied (reading continuously from a 16-bit word), 5TSDG could achieve up to ~30% power reduction in read mode compared to that of the low-power 6T structure. In this example, $R_1$ consumes ~7% less power in 5TSDG compared to a R0 as explained earlier. Obviously, larger number of read operations will result in a linearly higher power consumption difference in comparison with standby power due to larger values of $f$ in equation 2. Read operation of the low-power 6T and 5TSDG designs in this experiment were similar to Fig. 4(a) and Fig. 4(b) respectively. In a pipelined “smart” memory, back-to-back reads from the same sub-block would consume less dynamic power if $V_{g1}$ and $V_{g2}$ are held at $V_{SS}$ between consecutive reads.

The 5TSDG write power can be divided into W0 and W1 power, each consisting of idle cell standby power, plus the dynamic power. In Fig. 13, a 64Kbit array consisting of 64x16 bit blocks was studied while writing into a 16-bit word. In this example, W0 consumes ~80% less power, and W1 consumes ~9% less power compared with a low-power 6T structure in worst case scenario (FF corner, 120°C). Since R0 and R1 use similar power, storing bits to favor W0 (i.e. cell inverted) may reduce total power.

![Normalized Power Graph](image)

Fig. 13 Case study results of the worst-case write power consumption in comparison with read and standby power for 5TSDG vs. low power 6T design (FF, 120°C), 1≈ 33.8mW

4 CONCLUSION

In this paper, the operation of a new low-power and high performance design for a 5T SRAM cell was addressed which has improvements in static and dynamic power consumption, stability margins and performance when compared to previous designs in this area. The stability of the novel biasing scheme in dynamic mode was analyzed. The reduction in dynamic power consumption in comparison with a low-power 6T counterpart was demonstrated. A significant area saving is predicted compared to a conventional 6T cell.

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