Easy and structured approach for software and firmware co-simulation for bus centric designs

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ABSTRACT: Although software and firmware co-simulation is gaining popularity, it is still not widely used in the FPGA designs. This work presents easy and structured approach for software and firmware co-simulation for bus centric designs. The proposed approach is very modular and software language agnostic. The only requirement is that the firmware design is accessible via some kind of system bus. The concept has been used for testing DAQ system being developed for high energy physics experiment.

KEYWORDS: co-simulation, bus functional model, field-programmable gate array, fusesoc
1 Introduction

Software and firmware co-simulation can save a lot of time and money, as it leads to a lower number of HDL project builds and reduces the number of test iterations with the real hardware. Despite its apparent advantages the co-simulation is still relatively rare to see in FPGA designs. There are at least four reasons for such a situation. The first one is that setting up a co-simulation framework requires knowledge of multiple computing areas. The second one is that it might be time-consuming. The third one is that ready-to-use frameworks sometimes do not support some of the desired HDL features, for example handling compound types such as records or arrays. The fourth one is that ready-to-use frameworks, such as cocotb [1], are strictly coupled with a single programming language. This work presents the modular approach that tries to be in line with the Unix philosophy.

2 Concept

The co-simulation framework proposed in this work consists of the following mandatory elements:

1. software co-simulation interface,
2. HDL co-simulation interface,
3. HDL BFM (Bus Functional Model),
4. IPC (Inter-Process Communication) mechanism,
5. test runner.
Figure 1 shows scheme of the co-simulation framework concept. The framework blocks are loosely coupled, and each of them can be easily replaced. The whole test bench additionally consists of the project’s software and firmware code. The co-simulation interfaces are relatively short and straightforward, and once written, they can be reused for different tests within the project. If different software languages are used for the prototype and target implementation phases, it is also easy to write a co-simulation interface for the new language and reuse the co-simulation framework from the prototyping phase. The BFM can be custom or taken from a library such as OSVVM [2] or UVVM [3, 4]. The idea is based on the assumption that all communication is done via the bus. Not only the regular data is transferred via the bus, but also the test bench specific data. Such an approach is immune to the lack of support for compound types. What is more, the bus infrastructure is tested by the way.

The proposed approach is not free of drawbacks. The first one is that the firmware design must have some kind of system bus. This should not be a problem as almost all complex FPGA designs have some kind of bus, Wishbone [5] and AXI [6] being probably the most popular. The second one is that precise timing checking between signals is hard to achieve solely within the test bench software. It requires a firmware checker accessible via the bus. Another approach is using PSL (Property Specification Language) or SVA (SystemVerilog Assertions).

3 Implementation

The concept has been successfully implemented. A simplified example showing a co-simulation for an adder is available on [7]. The FuseSoc [8, 9] and fsva [10] tools have been used as the test runner. The AGWB [11, 12] tool is used for the registers generation. Wishbone has been chosen as the system bus. The firmware bus infrastructure comes from the General-Cores [13] library. The Wishbone BFM comes from the UVVM library. Although all listed components are necessary, it
is worth noting that the whole concept is agnostic to the chosen components. They all depend on the project and personal preferences.

Figure 2 shows directory structure of the example. At first it may seem that setting up single co-simulation requires relatively a lot of files. However, most of these files are reused between co-simulations and are short. For example, files: `tb_cosim.sh`, `sw/cosim_interface.py` and all files in the `fw/cosim` directory are reused in case of multiple co-simulations in the same project. The only two files strictly related with the particular module co-simulation are `tb_cosim.vhd` and `tb_cosim.py`.

Listing 1 presents the snippet from `adder.core` file, showing how paths for named pipes are passed both to the firmware and software sides. The paths could be hardcoded in the `tb_cosim.vhd` and `tb_cosim.py` files, however such approach increases the maintenance burden and enforces keeping the same information in multiple files. Keeping all the paths related information in the single `.core` file also makes any further editing easier.

3.1 Co-simulation interface

The co-simulation interface is a custom protocol for controlling the BFM and simulation progress. Its features and structure depend on the particular project requirements. The bare minimal interface for two-side communication must support write and read bus transfers, as well as a command for advancing a simulation for a given amount of time. More complex interfaces might also support block read, block write and stream transfers. They can also model access times or count the number of transactions.

4 Example run and output

To run the co-simulation in the example project one needs to simply execute `fsva ::adder tb_cosim` (assuming the dependencies listed in the `README.md` file are already installed). By default, only the standard output and standard error from the firmware side are attached to the terminal. This is because only the firmware simulator is started directly by the FuseSoc. The software is started by the pre-run hook, and its standard output and standard error need redirecting to a file. This is done in the `tb_cosim.sh` file. A need to redirect the output from the software side is
targets:
tb_cosim:
  default_tool: ghdl
toplevel: tb_cosim
generate:
  - agwb_regs
files:
  - agwb_dep
  - src
  - tb_cosim
hooks:
  pre_run: [tb_cosim]
parameters:
  G_SW_FW_FIFO_PATH: /tmp/fusesoc_cosim_example/adder_python_vhdl
  G_FW_SW_FIFO_PATH: /tmp/fusesoc_cosim_example/adder_vhdl_python

scripts:
tb_cosim:
  cmd:
    - ../../../tb_cosim.sh
    - adder
    - /tmp/fusesoc_cosim_example/adder_python_vhdl
    - /tmp/fusesoc_cosim_example/adder_vhdl_python

Listing 1: adder.core file snippet showing passing paths for named pipes.

Figure 3. Software side log for the example co-simulation.

not a big issue, as one can simply run tail -f /tmp/fusesoc_cosim_example/adder.log to get a live, terminal like print experience. Figure 3 presents software side log and figure 4 presents firmware side log.
Figure 4. Firmware side log for the example co-simulation.

5 Real use case

The proposed approach has been used for testing of DAQ (Data Acquisition) system for the CBM (Compressed Baryonic Matter) [14] experiment that is being prepared at FAIR (Facility for Antiproton and Ion Research) in Darmstadt.

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