A Novel Learning Algorithm for Bayesian Network and Its Efficient Implementation on GPU

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Abstract—Computational inference of causal relationships underlying complex networks, such as gene-regulatory pathways, is NP-complete due to its combinatorial nature when permuting all possible interactions. Markov chain Monte Carlo (MCMC) has been introduced to sample only part of the combinations while still guaranteeing convergence and traversability, which therefore becomes widely used. However, MCMC is not able to perform efficiently enough for networks that have more than 15–20 nodes because of the computational complexity. In this paper, we use a general purpose processor (GPP) and general purpose graphics processing unit (GPGPU) to implement and accelerate a novel Bayesian network learning algorithm. With a hash-table-based memory-saving strategy and a novel task assigning strategy, we achieve a 10-fold acceleration per iteration than using a serial GPP. Specially, we use a greedy method to search for the best graph from a given order. We incorporate a prior component in the current scoring function, which further facilitates the searching. Overall, we are able to apply this system to networks with more than 60 nodes, allowing inferences and modeling of bigger and more complex networks than current methods.

Index Terms—Bayesian Networks; GPU; MCMC; Priors

I. INTRODUCTION

Bayesian network (BN) is a probabilistic graphical model that describes causal relationship through directed acyclic graphs (DAG). In this work, we focus on the problem of learning a Bayesian network that characterizes the causal relationship from experimental data. This problem is proved to be NP-complete [1]. Due to the large number of graph structures, sampling-based methods are proposed to find the best matching graph using a scoring metric. Several sampling methods have been proposed, including graph-space sampling, order-space sampling, and order-graph sampling [2]. Among all these sampling methods, order-space sampling is demonstrated to be the best one [2]. However, these methods are still not efficient enough for large graphs. In this paper, we proposed a new strategy for sampling the order space. Specifically, we apply a greedy strategy into the order sampling procedure. Our new method is more accurate than the previous ones while maintaining the same complexity in the sampling stage. Furthermore, it does not require a postprocessing part which is needed in the previous methods.

In addition to experimental data, in many situations, prior knowledge for at least part of a given Bayesian network is available. Adding prior knowledge in the learning process can enhance the accuracy of the result while significantly reduce the searching space. Methods of adding priors include graph-based and probability-aimed [3]. However, the “pairwise” prior knowledge which indicates the likelihood of one event causing another is more easily obtained. Yet, no methods exist that can integrate such prior knowledge into the BN learning algorithm. In this work, we propose a novel prior component which can be easily added into our scoring function as a pairwise weight. It represents user’s “confidence” in the possible existence or non-existence of an edge.

Nevertheless, learning Bayesian interactions is still compute-intensive, demanding both software and hardware advancements. Novel computational platforms such as field-programmable gate array (FPGA) and graphics processing unit (GPU) have been applied to facilitate the learning of Bayesian networks [4]–[6]. GPU is known to be highly efficient for massively parallel computational problems. In this work, we exploit the parallelism in our novel Bayesian network learning algorithm and implement it on GPU. The combination of our novel algorithm and its GPU implementation allows us to learn graphs with up to 60 nodes.

The remainder of the paper is organized as follows. In Section 2, we introduce the background on the problem of learning Bayesian networks. In Section 3, we describe the improved learning algorithm. In Section 4, we demonstrate our novel method for adding priors. In Section 5, we discuss the implementation on GPU. In Section 6, we show the experimental results on the performance of our algorithms. We conclude the paper in Section 7.

II. BACKGROUND

A Bayesian network $G$ is a probabilistic graphical model that represents a set of random variables and their conditional dependencies via a directed acyclic graph (DAG). Each node in
the graph is associated with a random variable. Each directed edge indicates a causal relationship between the variables connected by that edge. Nodes that are not connected represent random variables that are conditionally independent. A parent set \( \pi_i \) of a given node \( v_i \) is a set of nodes which have a directed edge pointed to \( v_i \). Each node \( v_i \) is also associated with a probability distribution conditioned on all its parent variables, \( P(v_i|\pi_i) \). The joint probability distribution of all the random variables in a Bayesian network can be written as a product of the conditional distributions for all the nodes:

\[
P(v_1, v_2, ..., v_n) = \prod_{i=1}^{n} P(v_i|\pi_i) \tag{1}
\]

An example of a Bayesian network is shown in Figure 1(a). Every node is influenced by its parents. For instance, node \( E \) in Figure 1(a) has two parents, \( A \) and \( C \). Thus, the probability distribution of \( E \) is determined by the states of \( A \) and \( C \). This conditional distribution \( P(E|A, C) \) is shown in Figure 1(d) for all combinations of \( A \) and \( C \).

![Bayesian Network Example](image)

The graph learning problem is an NP-complete problem. The number of possible graphs grows super-exponentially with the number of nodes. Table I shows the numbers of possible graphs for different numbers of nodes. Compared to the number of graphs, the number of orders for a given number of nodes is much smaller. Table II also lists the numbers of orders for the same set of node numbers. Due to the reduced number of combinations, order sampler can converge in fewer steps compared to graph sampler and hence, reduce the overall complexity. Moreover, sampling in order space provides opportunities for parallel implementation. Due to these advantages, we develop our algorithm within the framework of order-space sampling.

Learning Bayesian networks aims at finding a graph structure which best explains the data. We can measure each different Bayesian graph structure with a Bayesian scoring metric, which is defined as [3]:

\[
P(G, D) = P(G)P(D|G)
\]

where \( P(G) \) denotes the prior distribution of a graph and \( D \) denotes the experimental data. Given a Bayesian network with \( n \) nodes, using the decomposition relation shown in Equation (1), we can represent the scoring metric as a product of \( n \) local scores \( P(v_i, \pi_i; D) \) as

\[
P(G, D) = \prod_{i=1}^{n} P(v_i, \pi_i; D). \tag{2}
\]

The local score \( P(v_i, \pi_i; D) \) can be calculated as

\[
P(v_i, \pi_i; D) = \gamma|\pi_i| \prod_{k=1}^{r_i} \frac{\Gamma(\alpha_{ik})}{\Gamma(\alpha_{ik} + N_{ik})} \prod_{j=1}^{|\pi_i|} \frac{\Gamma(N_{ijk} + \alpha_{ijk})}{\Gamma(\alpha_{ijk})} \tag{3}
\]
where $\gamma$ serves as a penalty for complex structures [2], $\alpha$ is the hyperparameter for prior of Bayesian Dirichlet score, $r_i$ refers to the number of different states of the parents set $\pi_i$, and $|v_i|$ refers to the number of possible states of the random variable $v_i$, $N_{ijk}$ and $N_{ijk}$ are counted from experimental data [3]. $\Gamma$ is the gamma function [11]. In order to reduce the overall complexity, we limit the maximal size of parent sets to a constant $s$.

III. ALGORITHM DESCRIPTION

In this section, we discuss our algorithm. The overall flow of our algorithm is plotted in Figure 2 while its pseudocode is shown in Algorithm 1. After the preprocessing step, we start scoring an order. The score is defined to be the best score of all the graphs satisfying that order. The scored order is accepted with a probability based on the Metropolis-Hasting rule [12]. We then apply the Markov chain Monte Carlo (MCMC) strategy to sample the order space: each new order is generated from the previous one by randomly selecting and swapping two nodes in the previous order. We sample the orders for a specified number of iterations. Each subroutine of our algorithm is discussed in detail in the following sections.

A. Preprocessing

As shown in Figure 2, our learning algorithm is started with a preprocessing part, which includes order initialization and the generation of all possible local scores (refer to Equation (3)). The order initialization randomly generates an initial order as the starting point. As we will show in Section III-B, the scoring part heavily relies on the computation of local scores. Indeed, each local score is repeatedly used in a large number of iterations. However, calculating the local score according to Equation (3) is time-consuming. Thus, instead of recomputing local scores each time when they are needed, we choose to compute local scores for all the possible combinations of the node and its parent set at the preprocessing stage. We store the result in a hash table keyed by the node $v_i$ and the parent set $\pi_i$. Later on, when a local score for a specific combination of a node and its parent set is needed, we just fetch the score from the hash table. This strategy leads to more than 10 folds speedup on GPP according to our experimental results.

Since the local score shown in Equation 3 is very small, we perform the computation in the log-space. Given a node $v_i$ and its parents set $\pi_i$, equation for a local score ($ls$) is now changed to:

$$ls(i, \pi_i) = \log_{10} \frac{\gamma^{|\pi_i|}}{\sum_{k=1}^{r_i} \log_{10} \Gamma(\alpha_{ik}) - \log_{10} \Gamma(\alpha_{ik} + N_{ijk}) + \sum_{j=1}^{s} (\log_{10} \Gamma(N_{ijk} + \alpha_{ij}) - \log_{10} \Gamma(\alpha_{ij}))}$$

(4)

The scoring function for a graph is changed to:

$$P(G, D) \propto \sum_{i=1}^{n} ls(i, \pi_i)$$

(5)

B. Scoring

Algorithm 1 Algorithm for our novel BN Learning algorithm.

1: Preprocess()
2: for 1 to iteration_num do
3: for every node $v_i$ in an order do
4: maxLs <= -LargeNumber
5: for each parent set $\pi_i$ consistent with this order do
6: if maxLs < ls($i, \pi_i$) then
7: maxLs <= ls($i, \pi_i$)
8: bestParents <= $\pi_i$
9: end if
10: end for
11: bestGraph.insert($i$, bestParents)
12: score <= maxLs + score
13: end for
14: Metropolis-Hasting-Comparison()
15: Best-Graph-Updating()
16: Order-Generation()
17: end for
18: return globalBestGraph

The scoring part is a major subroutine of our algorithm, which scores a given order. To effectively measure an order, we introduce a new scoring function different from the one proposed in [5]. Given a specific order, there are many graphs that satisfy that order. We define the score of an order to be the best score for all the graphs satisfying the order, i.e.,

$$P(D, \prec) \propto \max_{G \in \prec} P(G, D)$$

Based on Equation 5, we further have

$$P(D, \prec) \propto \max_{G \in \prec} \sum_{i=1}^{n} ls(i, \pi_i)$$

Due to the Markov property of Bayesian networks, global maximum equals to the sum of the maximal local scores of all the nodes, each of which is taken among all the combinations of the node and its parent sets that are consistent with the order. Mathematically, the scoring function can be represented as

$$P(D, \prec) \propto \sum_{i=1}^{n} \max_{\pi_i \in P_{\pi_i}} \sum_{\pi_i \in P_{\pi_i}} ls(i, \pi_i)$$

(6)

where $P_{\pi_i}$ is the set of all possible parent sets of the node $v_i$ that are consistent with the order. The scoring subroutine is shown at Line 3 ~ 13 in Algorithm 1. We notice that a
similar algorithm was previously mentioned in [13]. However, it is only used in the postprocessing part where a best graph is constructed from the best order. In [5], a different order scoring function was used, which is the sum of all the scores of the graphs that are consistent with the order. Compared to that scoring function, ours is better in the following ways:

- Our algorithm only needs comparison and assignment operations, avoiding the time-consuming exponentiation and logarithm operations required by the previous algorithm.
- The sum-based scoring function may lead to an incorrect result, because the best matching graph may not be consistent with the order which generates the largest score. However, since our function uses the max operation, the globally best graph must be consistent with the globally best order.
- The previous algorithm needs a postprocessing part which constructs the best graph from the best order. Our algorithm generates the best graph for each sampled order. Thus, we do not need any postprocessing.

In summary, since our algorithm avoids many expensive operations and reduces a large amount of computation, the total computation time is decreased.

In [4] and [5], bit vectors are used to generate every compatible parent set with respect to a given order. However, our experimental results indicate that bit vector is not a suitable implementation since it is very slow. According to our experiment, the bit vector implementation consumes a huge amount of time for networks with more than 20 nodes. This is because for the last node in an order, each of the $n-1$ nodes preceding it could be its parent. Therefore, we need to compare $2^{n-1}$ bit vectors to filter out the compatible parent sets for the last node. However, we notice that in practice the maximal size of a parent set is limited to a constant $s \ll n$. Given this, we only need to consider $\sum_{j=0}^{s} \binom{n-1}{j}$ potential parent sets for the last node, which is much smaller than $2^{n-1}$. Table II compares the runtime for generating all $2^n$ parent sets with the runtime for generating only those parent sets with a size limit of 4. We compare these runtimes (per iteration) for different numbers of the candidate parents ranging from 15 to 25. We can see that there is a dramatic increase in speed if we only generate those parent sets with a size limit of 4.

| Number of Candidate Parents | Generating all possible parent sets (Sec.) | Generating parent sets with a size limit of 4 (Sec.) | Speedup |
|-----------------------------|------------------------------------------|-----------------------------------------------|--------|
| 15                          | 0.011                                    | 1.29 × 10^{-9}                               | 1100   |
| 16                          | 0.017                                    | 1.29 × 10^{-9}                               | 1317   |
| 17                          | 0.085                                    | 1.66 × 10^{-9}                               | 3915   |
| 18                          | 0.104                                    | 2.38 × 10^{-9}                               | 4369   |
| 19                          | 0.125                                    | 2.86 × 10^{-9}                               | 6818   |
| 20                          | 0.297                                    | 2.84 × 10^{-9}                               | 10136  |
| 21                          | 0.645                                    | 4.04 × 10^{-9}                               | 15965  |
| 22                          | 1.238                                    | 4.48 × 10^{-9}                               | 27857  |
| 23                          | 3.425                                    | 5.43 × 10^{-9}                               | 63075  |
| 24                          | 6.814                                    | 5.88 × 10^{-9}                               | 115884 |
| 25                          | 12.185                                   | 7.51 × 10^{-9}                               | 162250 |

### C. Metropolis-Hasting Comparison, Best Graph Updating, and Order Generation

We apply the Markov chain Monte Carlo method (MCMC) to sample the order space, which essentially performs a random walk in that space. Each time a new order is proposed, even if its score is less than the score of the previous order, it still could be accepted based on the Metropolis-Hasting rule [12], which is to accept the new order with the probability

$$p = \min[1, \frac{P(\prec_{\text{new}}, D)}{P(\prec, D)}]$$

Suppose that the log-space score for the new order $\prec_{\text{new}}$ and that for the previous order $\prec$ are $\text{score}(\prec_{\text{new}})$ and $\text{score}(\prec)$, respectively. The new order is accepted if

$$\log(u) < \text{score}(\prec_{\text{new}}) - \text{score}(\prec),$$

where $u$ is a random number generated uniformly from the unit interval $[0, 1]$. Due to the property of MCMC, after a sufficient number of iterations, the Markov chain will converge to its steady distribution. At that time, each order is sampled with a frequency proportional to its posterior probability. Thus, an order with a high probability of occurring (corresponding to a high Bayesian score) is very likely to be sampled.

Our ultimate goal is to find the graph with the highest score. Therefore, we keep track of a number of best graphs obtained so far as the sampling procedure proceeds. At the end of each iteration, if a new order is accepted, then we compare the score of the best graph consistent with that order to the scores of the best graphs recorded so far. We update the record of the best graphs if the current graph is better.

At the end of each iteration, we generate a new order by randomly selecting two nodes $v_i$ and $v_j$ in the current order and swapping them, i.e., changing the order $(v_1, \ldots, v_i, \ldots, v_j, \ldots, v_n)$ to the order $(v_1, \ldots, v_j, \ldots, v_i, \ldots, v_n)$.

### IV. Priors for Characterizing Pairwise Relationship

In this section, we present our novel prior component that could effectively characterize the prior knowledge on the causal relationship between a pair of nodes.

Assume that a function $p(i, m)$ indicates the prior knowledge on the causal relationship between a pair of nodes $v_i$ and $v_m$. Equivalently, $p(i, m)$ represents the prior knowledge on the existence of an edge from $v_m$ to $v_i$. We add $p(i, m)$ into the scoring Equation (2) to affect the posterior probability of graphs as follows

$$P(G, D) = \prod_{i=1}^{n} \prod_{m \in \pi_i} p(i, m) \prod_{i=1}^{r_i} \frac{\Gamma(\alpha_{ik} + N_{ik})}{\Gamma(\alpha_{ik})} \times \prod_{j=1}^{|v_i|} \frac{\Gamma(N_{ijk} + \alpha_{ijk})}{\Gamma(\alpha_{ijk})}$$

(7)

Note that in the above equation, given an arbitrary graph, the prior probabilities on all the edges are multiplied together to influence the posterior probability of the graph. Thus, if the prior probability on the existence of an edge in the Bayesian network is large, the probabilities of the graphs containing that
edge will be increased and hence, these graphs are more likely to be sampled. In the log-space, Equation \( \text{(7)} \) becomes
\[
P(G, D) \propto \sum_{i=1}^{n} \left[ \log_{10}(p(i, m)) + \sum_{m \in \pi_i} \log_{10}(p(i, m)) \right] \tag{8}
\]
where \( \log_{10}(p(i, m)) \) is the local score in Equation \( \text{(4)} \). We call \( \log_{10}(p(i, m)) \) as the pairwise prior function (PPF) for the nodes \( v_i \) and \( v_m \). It is also denoted as \( \text{PPF}(i, m) \). Thus, Equation \( \text{(9)} \) becomes
\[
P(G, D) \propto \sum_{i=1}^{n} \left[ \log_{10}(p(i, m)) + \sum_{m \in \pi_i} \text{PPF}(i, m) \right] \tag{9}
\]

With this general form of adding pairwise priors, we can meet different needs by applying different PPFs.

In our design, we provide an interface for users. It is an \( n \times n \) matrix \( R \), where \( n \) is the number of nodes in the graph. Each entry in the matrix \( R \) is between zero and one. If the value \( R(i, m) \) is between 0 and 0.5, it means that there unlikely exists an edge from \( v_m \) to \( v_i \); if the value \( R(i, m) \) is between 0.5 and 1, then it means there likely exists an edge from \( v_m \) to \( v_i \); if the value \( R(i, m) \) is 0.5, it means that there is no bias on whether or not there exists such an edge from \( v_m \) to \( v_i \). This interface provides a convenient way to specify the pairwise priors. The actual PPF is a function on the value in the matrix \( R \). It must satisfy the following requirements:
- \( \text{PPF}(i, m) = 0 \) iff \( R[i, m] = 0.5 \)
- \( \text{PPF}(i, m) > 0 \) iff \( R[i, m] > 0.5 \)
- \( \text{PPF}(i, m) < 0 \) iff \( R[i, m] < 0.5 \)

Furthermore, according to our experiment results, PPF should also satisfy:
- when \( R[i, m] \) approaches 1, \( \text{PPF}(i, m) \) is around 10
- when \( R[i, m] \) approaches 0.5, \( \text{PPF}(i, m) \) approaches 0
- when \( R[i, m] \) approaches 0.5, \( \text{PPF}(i, m) \) is around −10

where 10 and −10 are chosen empirically to have a significant impact on the ultimate score of a graph.

Based on the above-mentioned requirements, we propose the following cubic polynomial to transform the value in the interface matrix \( R \) into the PPF:
\[
\text{PPF}(i, m) = 100(R[i, m] - 0.5)^3 \tag{10}
\]
The above function is plotted in Figure \ref{fig:3} to give a clear view.

V. IMPLEMENTATION OF THE LEARNING ALGORITHM ON GPU

In this section, we discuss the implementation of our algorithm on GPU for learning Bayesian networks.

A. The Architecture of GPU

Figure \ref{fig:4} shows the architecture of a typical GPU. Host refers to a CPU, which assigns tasks to and collects results from the GPU. As we show in Figure \ref{fig:5}, the GPU implements the scoring part of our algorithm, since the max operation can be paralleled both within each node and across all the nodes (refer to Equation \( \text{(6)} \)). The remaining parts of our learning algorithm are handled by the GPU. The CPU also takes charge of the communication with the GPU. Specifically, it passes a new order to the GPU and gets the best graph and its score from the GPU, as shown in Figure \ref{fig:4}.

A GPU contains a number of blocks connected in the form of a grid. Each block usually includes 256 threads. Each thread has a number of registers and a local memory. All the threads within a block can access the shared memory of that block. All the threads can also access the global memory of the GPU.

The GPU we use is based on Fermi architecture \cite{14}. Fermi architecture provides true cache hierarchy for us to use the shared memory of GPU. Also, it is fast in context switching operation and the atomic operations of read-modify-write for parallel algorithms. Fermi architecture has up to 16 streaming multiprocessors (SM) with each containing 32 CUDA cores. Thus, it features up to 512 CUDA cores. A CUDA core executes a floating point or an integer instruction per clock for a thread. The GPU has \( 6 \times 64 \)-bit memory partitions for a 384-bit memory interface, supporting up to a total of 6 GB of GDDR5 DRAM memory. The SM schedules threads in groups of 32 parallel threads called warps. Each SM features two
warp schedulers and two instruction dispatch units, allowing two warps to be issued and executed concurrently.

B. Task Assigning Strategy

GPU implements the order scoring part of the Bayesian network learning algorithm. This requires us to assign the tasks evenly among all the blocks and all the threads. We describe our task assigning strategy in this section.

First, we assign $h$ blocks for each node. These $h$ blocks together will get the maximal local score $\max_{\pi_i \in P_{\pi_i}} l_s(i, \pi_i)$ for the node $v_i$ (refer to Equation 6). The number of local scores they need to compare equals to the size of the set $P_{\pi_i}$, or the number of parent sets of the node $v_i$ that are consistent with the given order $\prec$. Now we will assign these $|P_{\pi_i}|$ parent sets evenly to all the threads in the $h$ blocks. Assume that the total number of threads in the $h$ block is $T$. Then, each thread will handle $|P_{\pi_i}|/T$ local scores and get the “local” maximum among them. After that, we will further compare all the local maximal scores obtained by the threads and get the largest one. We need to assign to each thread the parent sets they are in charge of.

Since each thread has a thread ID and a block ID in the CUDA programming environment, we can assign a specific task to a thread based on its ID. The problem is how a thread predicts the parent sets that it needs to handle. This corresponds to predicting which parent set $\pi_k$ the $k$-th thread needs to lookup in the hash table to get the local score $l_s(i, \pi_k)$. This problem can be converted into a subset indexing problem: given a set of $n$ nodes, we want to index all the subsets with at most $s$ nodes in a regular way so that given an arbitrary valid index we can easily get the corresponding subset. Note that the total number of the subsets with at most $s$ nodes is $S = \sum_{j=0}^{s} \binom{n}{j}$. Indeed, we can index these subsets in a regular way. For example, consider a set of nodes $\{0, 1, 2, 3, 4, 5\}$. If the size limit on the subsets is 4, then we can obtain the total number of subsets as $S = \sum_{j=0}^{4} \binom{6}{j} = 57$. We assign index 0 to the subset $\{0, 1, 2, 3\}$, index 1 to the subset $\{0, 1, 2, 4\}$, index 2 to the subset $\{0, 1, 2, 5\}$, index 3 to the subset $\{0, 1, 3, 4\}$, ..., index $S - 2$ to the subset $\{5\}$, and index $S - 1$ to the subset $\emptyset$.

Now the problem is how to recover the subset from a given index if we use the above indexing method. We propose an algorithm shown in Algorithm 2 to solve this problem, which is inspired by an algorithm proposed in [15]. Since GPU cannot support recursive functions, we provide a non-recursive version. Given the number of candidate parents $n$, the size of parent sets $k$, and the index of the expected parent set $l$, it can return the $l$-th parent set which is composed of $k$ nodes chosen from the $n$ candidates.

Algorithm 2 Algorithm for obtaining the $l$-th $k$-combination of $n$ elements in lexicographic order.

1: Given three integers $n$, $k$, and $l$
2: $low \leftarrow 0$
3: for $pos = 1$ to $k - 1$ do
4:   $\{Compute the element for each position in the $k$-combination\}
5: $s \leftarrow 0$
6: $sum \leftarrow 0$
7: for $s = 1$ to $n$ do
8:   if $sum + \binom{n-s}{k-1} < l$ then
9:      $sum \leftarrow sum + \binom{n-s}{k-1}$
10: else
11:      break
12: end if
13: end for
14: $comb[pos] \leftarrow low + s$
15: $low \leftarrow comb[pos]$  
16: for $k = n - s$ to $s$ do
17:   $comb[k] \leftarrow low + l$
18: $return$ $comb$.

Our purpose is to compute the $k$-combination of $n$ elements that is at a given position $l$ in the lexicographic order, without explicitly counting them one by one. The solution is quite straightforward. Suppose that the $n$ elements are $1, 2, \ldots, n$. We obtain each element in the $k$-combination $(a_1, a_2, \ldots, a_k)$ one by one from the first to the last. We assume that the elements in each combination are in increasing order from the first to the last, i.e., $a_1 < a_2 < \cdots < a_k$. With this assumption, we can see that there are $\binom{n-m}{k-1}$ $k$-combinations beginning with the value $m$ ($m = 1, 2, \ldots, n - k + 1$). Based on this fact, we can obtain the first element $a_1$ as the largest number such that $sum = \sum_{i=1}^{a_1} \binom{n-i}{k-1} \leq l$. In order to get the second element $a_2$, it is equivalent to obtaining the $(k - 1)$-combination of $(n - a_1)$ elements at the position $(l - sum)$. Thus, $a_2$ is the largest number $s$ such that $\sum_{i=1}^{a_1} \binom{n-a_1-i}{k-1-1} \leq (l - sum)$, plus the shift $a_1$, namely $a_2 = a_1 + s$. We compute all the remaining elements in the combination in a similar way.

With Algorithm 2 each thread can get the first parent set it needs to handle based on its ID. With this, the remaining parent sets it needs to handle can be obtained incrementally. However, the above algorithm requires additional computation on GPU. Our second strategy is to create a parent set table (PST) and store all the combinations in the the global memory of the GPU. Figure 6 shows an example of the PST.
and the additional memory requirement for storing the PST. Suppose that we have in total $T$ threads to handle $S$ parent sets. Then, each thread handles $\frac{S}{T}$ parent sets. Therefore, the $i$-th thread should handle the $\frac{iS}{T}$-th up to the $\frac{(i+1)S}{T}$-th parent sets from the PST. Compared to the above-mentioned combinatorial algorithm, PST-based method is much faster since it only needs to read the table. Although it requires additional memory, the overhead is small. Indeed, as shown in Figure 6(b), a 60-node graph only costs 7.99 MB additional memory when the size limit on the parent set is $s = 4$. Using the PST and a proper mapping strategy, we can assign to each thread the parent sets it is responsible for.

\[ \begin{array}{cccccccccccccccccc}
1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 \\
0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 \\
-3 & -2 & -1 & 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 \\
\end{array} \]

Fig. 6. An example of a parent set table and its additional memory requirement. (a) The PST for a set of candidate parents \{0, 1, 2, 3, 4, 5\}. The size of the subset is limited to 4. (b) The additional memory requirement for the PST versus the size of the candidate parent set.

\[ \begin{array}{cccccccccccccccccc}
1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 \\
0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 \\
-3 & -2 & -1 & 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 \\
\end{array} \]

Fig. 7. An illustration of the reduction algorithm to find the highest score in the shared memory.

After completing its task, each thread stores its best parent set and the best score in a shared memory within each block. We further need to find the best score and the best parent set among all choices stored in the shared memory. In order to do this efficiently, we modified a reducing algorithm mentioned in \[16\]. Each thread has kept its local best parent set and the corresponding local best score. The problem is to pick the highest score among all the local best scores as well as its corresponding parent set. This problem is not as simple as the problem of searching the highest score since we have to recover its original position during a highly dynamic process. We have to consider both the efficiency and the correctness. An illustration of our algorithm is shown in Figure 7 (a). Assume that a shared memory has 16 entries. We want to move the highest score to the entry 0 of the array and record the ID of the thread that gives the highest score in entry 1. In this example, the highest score is $-1$ and the thread ID is 3. In the first reduction, we first divide the array into two halves. We move the higher scores to the left half and record their original thread IDs in the right half as shown in the third row of Figure 7. It requires half of the threads to participate. For example, thread 0 compares its value with the value in entry 8. Then, thread 0 assigns entry 0 of the shared memory with value $-3$ and entry 8 with 0, which is the ID of the thread giving the larger value $-3$. Each reduction halves the amount of memory involved.

In the rest of the reductions, we have to keep track of the ID of the original thread that gives the better value. For example, in the second reduction, entry 2 of the shared memory has to be compared with entry 6 of the shared memory. Since $-2$ is larger than $-9$, $-2$ is stored in entry 2. Note that $-2$ is now from entry 6. However, the ID of the original thread that gives the value $-2$ is store in entry 6 of shared memory of size $8 = 14$, where 8 is the current number of threads involved. Then, we update entry 6 with the original thread ID by copying the value of entry 14 to entry 6. The total number of iterations required to get the best score among a total of $n$ scores is $\log_2 n$. After obtaining the ID of the original thread that gives the highest score, we can fetch the best parent set from that thread.

VI. EXPERIMENTAL RESULTS

We perform experiments on our algorithm both on GPP and GPU. The GPP we use is a 2.4 GHz Intel Xeon E5620 processor with 8GB RAM. The GPU we use is an NVIDIA Tesla M2090 GPU with 6GB GDDR5 RAM. Our GPU-based implementation is described in Figure 5 with its scoring part performed on the GPU and the remaining parts performed on the CPU. The operating system is Ubuntu 10.04.4.

In our experiments, we set the maximal size of the parent set as $4$ ($s = 4$). In our implementation, the GPU is used to accelerate each order scoring iteration. We first study its speedup effect. Figure 8 shows both the runtime of our scoring implementation on GPP and the runtime of the implementation on GPU for different graph sizes. From Figure 8 we can see that the GPU implementation achieves a significant speedup over the GPP implementation. The detailed runtimes per iteration for both the GPP and the GPU implementations, together with the acceleration rates, are listed in Table III. Acceleration rate is peaked at 10 for graphs with around 50 nodes. For smaller graphs, i.e., graphs with fewer than 13 nodes, their acceleration rates are less than 1. That is due to the time consumed on the context switching on GPU. As a result, GPU is not a good choice for small graphs.

To make the results more practical, we further apply our learning algorithm to two well-known networks: 1) an 11-node signaling transduction network (STN) from human T-cell \[10\]; and 2) a 37-node ALARM network \[17\]. Table IV shows the runtimes for both the 11-node graph and the 37-node graph. Note that the preprocessing part of the GPU implementation is done on a CPU, as we mentioned before. The GPU-based implementation takes more time on preprocessing than the GPP-based implementation. Still, the total runtime of the GPU-based implementation is about 1/3 of the runtime of the GPP-based implementation for the large
37-node network. Scoring orders is the most time-consuming part of the Bayesian network learning algorithm. Accelerating scoring subroutine is our primary goal in this work. We will study how to speedup the preprocessing part in our future work.

We also compare the implementation that generates all possible parent sets with the implementation that generates only parent sets with a limited size. We evaluate these two implementations on GPP using the previous 11-node graph and a randomly synthesized 20-node graph. We do not use the 37-node graph because the generation of all the possible parent sets is prohibitively time-consuming. The runtime results are shown in Table V. From the table, we can see that for both graphs, the total acceleration rate is almost 300% when we only generate parent sets with a limited size. The speedup in the preprocessing part is not so significant for the 11-node graph, while it is more than 3 times faster for the 20-node graph.

We also empirically study the accuracy of our algorithm. We use the receiver operating characteristic (ROC) curve introduced in [18] to measure the accuracy. A ROC curve is a plot of the true positive (TP) rate versus the false positive (FP) rate. True positive rate gives the fraction of true positives out of the observed positives, while false positive rate gives the fraction of false positives out of the observed negatives. The closer to the upper-left point (0, 1), the more accurate is the graph learning result. We tried a 20-node graph with 1,000 and 10,000 iterations separately. The ROC curves for these two experiments are shown in Figure 9 and 10 respectively. Clearly, the resulting curve with 10,000 iterations is closer to the upper-left corner than the resulting curve with 1,000 iterations. However, the curve with 1,000 iterations is pretty closer to the upper-left corner. It indicates that our algorithm is highly accurate with even a small number of iterations. In these two figures, the points from the right to the left are generated as follows: the first point is obtained without adding any prior knowledge on edges; the second point is obtained by assigning “interface” prior value (refer to Section IV) 0.7/0.2 with a probability of 0.2 to edges which are mistakenly removed/added when learned without any prior knowledge; the third point is obtained by adding the same prior knowledge used in generating the second point but with a probability of 0.4; the fourth point is obtained by assigning “interface” prior value 0.8/0.1 with a probability of 0.2 to edges which are mistakenly removed/added when learned without any prior knowledge; the fifth point is obtained by adding the same prior knowledge used in generating the fourth point but with a probability of 0.4. Note that the priors added becomes stronger as we generate the points from the first to the last.

In realistic situations, the observed data may contain a large amount of noise and hence become faulty. In order to learn BNs correctly in these situations, the algorithm must be highly tolerant to noise. We study the fault tolerance of our algorithm by injecting errors into the data. We test our algorithm in learning Bayesian networks with two states. In this case, we assume that each data has a probability p to flip its state. That is, every single data would change from 1 to 0 or from 0 to 1 with a rate of p. In realistic context, this means that every

![Fig. 8. Average runtimes per iteration for both the GPP and the GPU implementations.](image)
Fig. 9. A ROC curve for learning a 20-node graph from 1,000 observed data. Our learning algorithm samples the order space 10,000 times.

Fig. 10. A ROC curve for learning a 20-node graph from 1,000 observed data. Our learning algorithm samples the order space 1,000 times.

Fig. 11. A ROC curve for learning a 20-node graph from 1,000 observed data with different rates of fault injection. Our learning algorithm samples the order space 10,000 times.

VII. CONCLUSION

Learning Bayesian network structure from experimental data is a computational challenging problem. In this paper, we have demonstrated a novel BN learning algorithm and its implementation on GPU. Our proposed algorithm is three times faster than the traditional algorithm when run on GPP. Further, our GPU implementation has achieved a 10-fold speedup per iteration over the GPP implementation. When the entire learning procedure is considered, the GPU implementation has a 3-fold speedup. Overall, we have accelerated the BN learning algorithm at least 9 folds. Experimental results also demonstrated that our algorithm gives accurate result and is highly tolerant to errors in the data.

Our algorithm is an improved version over the one proposed in [5]. We have proposed a better method for scoring the order based on the best graph consistent with the order. We have also introduced a new way of adding pairwise priors to enhance the accuracy of learning Bayesian networks. In addition, we have proposed two strategies for distributing the scoring tasks evenly among a given number of threads in GPU. In our current implementation, we take advantage of the parallelism in the order scoring part and accelerate that part using GPU. In our future work, we will study how to accelerate the preprocessing part using GPU.

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