A Very Low Reference Spur Phase Offset Technique in Fractional-N Charge pump PLLs

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Abstract—Fractional-N charge pump phase locked loops (PLLs) suffer from the problem of increased in-band phase noise due to charge pump non-linearity caused by UP/DN charge pump current mismatch. Existing techniques that resolve this problem by introducing phase offset between reference and divide signals cause large reference spurs or increase jitter at PLL output. A very low reference spur phase offset technique is proposed in this work. A detailed comparison of the reference spurs caused by the existing and the proposed techniques to introduce phase offset is presented. Simulation results show that the reference spur level generated at the PLL output after applying the proposed technique is 26 dB lower than the existing techniques in the presence of 5% charge pump current mismatch.

Index Terms—Fractional-N PLL, frequency synthesizer, reference spur, spur reduction, Sigma-Delta modulator

I. INTRODUCTION

One of the important problems in low noise Fractional-N PLLs is the increased in-band phase noise due to the phase frequency detector/charge pump (PFD/CP) non-linearity caused by non-idealities like UP/DN charge pump (CP) current mismatch [1], [2], [3], [4]. As shown in Fig. 1, in the presence of CP current mismatch, the charge pump transfer characteristics (charge delivered to loop filter Q_{cp} vs the input phase error dt[k]) has a slope discontinuity at the origin. The Σ−Δ quantization noise when passed through this non-linear transfer characteristics results in folding of the high frequency quantization noise inside the PLL bandwidth.

Existing techniques [2], [5], [6], [7] to reduce the increased in-band noise due to PFD/CP non-linearity involve introducing a phase offset between reference and divide signals. But these techniques introduce large reference spurs [5], result in increased jitter contribution [2], [6], [7] and require PVT trimming. A phase offset technique which offers theoretically zero spur and needs no PVT trimming is proposed in this work. It is shown through simulations that even in the presence of 5% CP mismatch, the reference spur level is 26 dB lower than the existing techniques. A conceptually similar technique is discussed in [8], [9], but implementation details are not given in [8] and the proposed solution is simpler in implementation and offers much lower spur (≈ 29 dB lower) compared to [9].

Section II describes the existing phase offset techniques and a detailed comparison of the reference spurs in those techniques. The proposed method and its performance degradation in the presence of non-idealities is discussed in Section III. The simulation set up and the results showing the efficacy of the proposed technique is discussed in Section IV. The conclusions drawn from the simulation results are presented in Section V.

II. PRIOR WORK

A common approach to address the problem of increased in-band noise due to PFD/CP non-linearity is to shift the operating point of the PFD/CP to non-zero phase error (±T_{os}) as shown in Fig. 2. Thus Σ−Δ quantization phase error always sees the UP (or DN) current path instead of switching between the two currents in the steady state. The phase offset T_{os} is chosen such that T_{os} > max(|dt[k]|), where dt[k] is the instantaneous phase error between the reference and divide signals in the steady state and max(|dt[k]|) is the maximum value of |dt[k]|. The rest of this section describes the techniques to introduce phase offset between the reference and divide signals.

Section II describes the existing phase offset techniques and a detailed comparison of the reference spurs in those techniques. The proposed method and its performance degradation in the presence of non-idealities is discussed in Section III. The simulation set up and the results showing the efficacy of the proposed technique is discussed in Section IV. The conclusions drawn from the simulation results are presented in Section V.

![Fig. 1. Fractional-N PLL with non-linear PFD/CP transfer characteristics](image1)

![Fig. 2. Steady state operating region of the CP a) before introducing phase offset, b) after introducing a positive phase offset T_{os} and c) after introducing a negative phase offset −T_{os}](image2)
A. Constant current offset (CCO) method

By connecting a constant current source $I_{os}$ to charge pump output [5] as shown in Fig. 3.(a), a charge of $I_{os}T$ is removed from the loop filter every reference cycle ($T$ is the reference clock period). The PLL feedback action responds by skewing the reference and divide edges by $T_{os}$ such that net charge delivered to the loop filter per cycle is zero (excluding the Fractional-N noise).

$$I_{cp}T_{os} - I_{os}T = 0 \rightarrow T_{os} = I_{os}T/I_{cp} \quad (1)$$

$I_{os}$ is chosen based on the CP current $I_{cp}$ and the desired offset delay $T_{os}$. This method is referred to as the constant current offset (CCO) method in this work. The steady state UP/DN signals and the charge pump current waveforms in the CCO method are shown in Fig. 3.(b).

![Fig. 3. (a) Modified CP in CCO method b) steady state CP current pulses in the CCO method](image)

B. Reset delay mismatch (RDM) method

The other approach to introduce phase offset is by introducing a delay mismatch [6] in the UP and DN reset paths in the PFD as shown in Fig. 4.(a). In this method, the UP path reset time is $T_{rst}$ seconds and the DN path reset time is $T_{rst} + T_{os}$. Thus the DN current is turned ON for an additional $T_{os}$ seconds every reference cycle. This amounts to removing a charge of $I_{cp}T_{os}$ every reference cycle, which is compensated by the PLL by offsetting the reference and divide edges by $T_{os}$ seconds. This method is referred to as the reset delay mismatch (RDM) method in this work. The steady state UP/DN signals and the charge pump current pulses in the RDM method are shown in Fig. 4.(b).

![Fig. 4. a) Modified PFD in RDM method b) steady state CP current pulses in RDM method](image)

The magnitude of the reference spur level at $k^{th}$ harmonic in the CCO method (in dBc) can be shown as [10], [11], [12]

$$S_{\Phi,cco}(k_{f_r}) = 20 \log \left( \frac{|L_{cp}T_{os} \cdot \operatorname{sinc}(k_{f_r}T_{os})|}{2k_{f_r}} \right) \quad (3)$$

where $Z(f)$ is the loop filter impedance, $f_r = 1/T$ is the reference frequency and $K_v$ is the VCO tuning sensitivity. Using Eq.(2), the reference spur level in the RDM method can be expressed in terms of the CCO method as

$$S_{\Phi,rdm}(k_{f_r}) = S_{\Phi,cco}(k_{f_r}) + 20 \log |2 \sin(\pi k_{f_r}(T_{os} + T_{rst}))| \quad (4)$$

The spur level in the RDM method can be seen as a high pass filtered version of the CCO method. Thus it sees a huge attenuation (20 log $|2 \sin(\pi k_{f_r}(T_{os} + T_{rst}))|$) for the lower harmonics of $f_r$. Though the RDM method introduces a lower reference spur, the main disadvantage with this method is the realization of the delay precisely and its jitter [6].

In most commercial RF synthesizers, the PLLs are required to support a wide range of frequencies and the offset delay $T_{os}$ has to track the VCO time period. The delay either needs to be trimmed based on the VCO frequency or it needs to be over designed by ensuring it works for the largest operating time period of the VCO. This increases, not only the reference spur level at the VCO output (as it is proportional to $T_{os}$) but also the CP noise contribution [2]. Furthermore the delay line needs to be trimmed for PVT variations, which adds to additional complexity. Thus, besides introducing very low reference spur, a good phase offset technique should have the following properties to make it more attractive a solution. 1) It should be independent of the process variation, 2) it should track the VCO output time period, without increasing the implementation complexity of the PLL and 3) the delay element should not add any additional noise to the PLL. The next section discusses the proposed solution which satisfies all the aforementioned properties.

C. Comparison of reference spurs

Let $i_{oc}(t)$ and $i_{rdm}(t)$ be the steady state charge pump current waveforms injected into the loop filter in the CCO and RDM methods respectively. Ignoring the $\Sigma - \Delta$ noise ($dt[k] = 0$), it can easily seen from Fig.3.(b) and Fig.4.(b) that $i_{rdm}(t) = i_{oc}(t) - i_{oc}(t - T_{os} - T_{rst})$. The steady state CP current PSD in RDM ($S_{irdm}(f)$) method and CCO ($S_{ioc}(f)$) method can be expressed as

$$S_{irdm}(f) = S_{ioc}(f) \left| 1 - e^{-j2\pi f(T_{os} + T_{rst})} \right|^2 \quad (2)$$

III. THE ZERO SPUR OFFSET (ZSO) METHOD

All the techniques that introduce phase offset, do so by removing a fixed charge from the loop filter every reference cycle. However the only way the PLL feedback action can compensate this fixed charge is by injecting an equal charge...
at the beginning of the cycle\(^1\). In case of CCO method, the charge removal happens throughout the reference cycle (Fig.\(5.(a)\)) and in case of RDM method, the charge removal takes place \(T_{\text{rst}}\) seconds after charge injection (Fig.\(5.(b)\)). The reason why reference spur arises is that the charge removal and injection process takes place at different times. In this work we propose a PFD architecture where the charge removal and injection takes place simultaneously as shown in Fig.\(5.(c)\), thus theoretically achieving zero reference spur. Hence this method is referred to as zero spur phase offset (ZSO) method.

![Fig. 5. Steady state current waveforms in 1) CCO method, 2) RDM method and 3) Proposed ZSO method.](image)

\(A.\) \textit{Modified PFD in the ZSO method}

The modified PFD in the proposed ZSO method is shown in Fig.\(6.(a)\). In addition to the ‘ref’ and ‘div’ signals, the modified PFD also operates on a delayed version of the ‘div’ signal (delayed by a fixed delay of \(T_{os}\)) referred to as ‘divd’. The UP pulse width is controlled by the upper half of the PFD (comprising of flip-flops FF1 and FF2 driven by ‘ref’ and ‘divd’) and the DN pulse width is controlled by the lower half of the PFD (comprising of flip-flops FF2 and FF3 driven by ‘div’ and ‘divd’). Similar to the RDM method, the DN path is used as a ‘fixed charge’ removing circuit. Every reference cycle the DN signal goes high when the ‘div’ signal goes high and is reset when the signal ‘divd’ goes high. Thus it is high for a fixed duration of \(T_{os} + T_{rst}\) every cycle. To attain phase locking, the PLL feedback action will offset the rising edges of ‘ref’ and ‘divd’ signals by \(T_{os}\) so that width of the UP pulse is same as the DN pulse, thus ensuring the net charge dumped into the loop filter is zero. Fig.\(7.(a)\) & (b) show the signals of the modified PFD and CP current before and after the locking is attained. In the steady state, the UP and DN signals will go high at the same time and will be reset simultaneously when ‘divd’ goes high. Thus the current injected into the loop filter is zero, leading to zero reference spurs.

It should be noted that in the presence of \(\Sigma - \Delta\) noise, the charge injected every reference cycle will not be zero, but now only the ‘UP’ pulse width is varied in proportion to the phase error between ‘ref’ and ‘divd’ signals. Thus the PFD/CP operating point is now shifted away from the zero phase error operating point. The steady state UP/DN current pulses in the presence of \(\Sigma - \Delta\) noise with the varying ‘UP’ pulse width and fixed ‘DN’ pulse width are shown in Fig.\(6.(b)\).

\(1\)To make the explanation simpler the \(\Sigma - \Delta\) noise is assumed to be zero. In the presence of sigma delta noise the average value of the charge over many reference cycles will be zero. But the net charge injected into the loop filter will not be zero every reference cycle.

\(2\)A divide by 128 circuit with a 2 GHz input clock, designed in a UMC 180 nm CMOS process consumes a power of \(\approx 1.1 mW\) and the offset delay circuit for an offset of \(3.5 T_{vco}\) (seven flip flops) consumes only \(\approx 56.35 \mu W\) from a 1.8 V supply. The results are obtained from schematic level simulations.
B. Performance in the presence of Non-idealities

In the presence of PFD/CP non-idealities like CP current mismatch, charge injection, clock feed-through and delay mismatch between the UP/DN signal paths, reference spurs arise in the ZSO method as well\(^3\). Ignoring the \(\Delta \) noise, the reference spur at the \(k\)th harmonic in the presence of CP current mismatch, in the ZSO method can be approximated as \([10],[11],[12]\)

\[
20 \log \left| \frac{l_{mis}(T_{ref} + T_{os})}{T} \right| = 2 \left( \frac{\pi k f_c(T_{ref} + T_{os})}{2} \right) \left( \frac{Z(k f_c)k_v}{2k f_c} \right)
\]

where \(l_{mis} = I_{up} - I_{dn}\) is the mismatch between the UP and DN currents. The reference spur levels due to these non-idealities in Fractional-N PLLs should be estimated from transient simulations. The simulation test bench used to estimate the reference spurs and a comparison of the different techniques for introducing phase offset is discussed in the next section.

As a final remark on reference spurs, it should be noted that the loop bandwidth of Fractional-N PLLs is typically two orders of magnitude lower than the reference frequency \((BW < f_c/100)\), so additional poles can be added in the loop filter to reduce reference spurs without compromising the stability of the PLL. However PLLs employing feedforward \(\Delta \) noise cancellation \([3],[6]\) and ring oscillator VCOs tend to have higher bandwidth. In such cases the ZSO method can help reduce spurs significantly without compromising the loop phase margin.

In addition to that, the advantages of the ZSO method like simpler implementation, PVT independent offset delay etc., still stand irrespective of the PLL bandwidth.

IV. Simulation Results

A 2.4 GHz output PLL with a \(f_c = 20 \text{MHz}\) reference frequency (shown in Fig.9) is simulated to compare all the techniques. The PLL is a Type-II PLL with two poles at DC, a stabilizing zero and two high frequency poles after the unity gain bandwidth to reduce spurs. The UGB (\(f_u\)) of the PLL is \(500 \text{kHz}\). The zero is placed at \(f_z = 197 \text{kHz}\), and the poles are at \(f_{p1} = 2 \text{MHz}\) and \(f_{p2} = 5.27 \text{MHz}\). The phase margin of the PLL is \(51^\circ\). The charge pump current is \(I_{cp} = 1 \text{mA}\), the nominal divide value in Integer-N mode is \(N = 120\) and in Fractional-N mode is \(N.f = 120.333\). The VCO gain is \(K_v = 200 \text{MHz/V}\). The loop filter component values are \(R_1 = 2.1 \text{k}\Omega, R_2 = 4 \text{k}\Omega, C_z = 550 \text{pF}, C_1 = 40 \text{pF}, C_2 = 10 \text{pF}\).

All the blocks in the PLL are modeled behaviorally except the loop filter which is at schematic level. The VCO and the fractional divider were modeled with a combined VCO and divider model to reduce simulation time \([14]\). A 3\(^{rd}\)-order \(\Delta \) MASH 1-1-1 modulator \([15]\) was used to generate the divide value for the fractional part. To measure the reference spurs, the PLL is simulated in the Fractional-N mode in a transient simulation\(^4\). The phase noise (and the reference spurs) at the PLL output can be estimated by computing the PSD of control voltage and then passing it through the VCO transfer function \((K_v/2f_c)^2\) to compute the one-sided PSD as shown in Fig.9. The transient simulations were carried out in Spectre\([14]\) and the data is then transferred to MATLAB for further processing and to generate the plots. The phase noise estimated from the test bench from a transient simulation (for a divide value of \(N.f = 120.333\)) is compared with the analytical expression \([2]\) and shown in Fig.10. It can be seen that the phase noise obtained from simulation is in close agreement with the theoretical results.

The offset delay required to linearize the charge pump is found from simulation by estimating the peak deviation of the phase error in the fractional-N mode. The value of the offset delay is \(T_{os} = 3.5T_{vco} = 1.45833 ns\). In the CCO method, a constant current of value \(I_{os} = I_{p}T_{os}/T\) is connected at the charge pump output. In the RDM method, a timing mismatch of value \(T_{os}\) is introduced in the reset delay path of the PFD. The ZSO method is implemented using the modified PFD shown in Fig.6.(a).

\(^4\)To measure reference spurs in the Integer-N mode, the PLL can be locked in a periodic steady state (pss) simulation. Once the PLL is locked, using the Narrow band FM approximation \([11],[12]\), the reference spurs can be obtained by passing the spectrum (obtained from the pss simulation) of the control voltage through the VCO transfer function \((K_v/2f_c)^2\). As there is no periodic steady state operating point in Fractional-N PLLs, a transient simulation with the same accuracy settings as a pss simulation was performed.

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\(^3\)It should be noted that both the CCO and RDM methods introduce large reference spurs even in the absence of any non-idealities. The equations Eq.(3) and Eq.(4) do not take the PD/CP non-idealities into account. However the spur levels caused by the non-idealities are much lower compared to the reference spurs due to the phase offset techniques (CCO and RDM) themselves.
Fig. 10. Phase noise computed from the test bench overlaid with the analytical expressions.

Fig. 11. Reference spurs at PLL output before and after applying the phase offset techniques. Plot shows the power integrated in a bandwidth of \( f_s / 1024 \approx 19.5 \text{kHz} \).

Fig. 9. The simulated phase noise of the PLL with 5\% CP current mismatch before and after applying the techniques is shown in Fig. 11. It can be seen that the in-band noise is reduced after the introduction of the phase offset, but the reference spur levels are increased. The reference spur level in RDM method is 20 log \( |\sin(\pi f_s T_{os} + T_{mis})| \) lower than the CCO method as predicted by Eq. (4). The spur level in ZSO method is 26 dB lower than the RDM method as predicted by the analysis\(^3\). A higher mismatch current will increase the spur level in the ZSO method but will still be much lower than the RDM method.

\(^3\)By subtracting Equations Eq.(4) and Eq.(5), it can be easily shown that \( S_{\phi,ZSO}(f_s) = S_{\phi,RDM}(f_s) - 20 \log(I_{\text{mis}}/I_{\text{os}}) = S_{\phi,RDM}(f_s) - 26 \text{dB} \).

V. CONCLUSION

A very low reference spur phase offset technique to reduce the increase in the in-band noise due to PFD/CP non-linearity is proposed and analysed in detail. It was shown that the proposed technique offers very low reference spur, is simpler in implementation and requires no PVT trimming. The simulation setup for accurately estimating reference spurs in Fractional-N PLLs is also discussed. The simulation results are in close agreement with the analytical equations presented. From the simulations, the reference spur levels are finally shown to be at least 26 dB lower (for a 5\% mismatch in CP current) compared to the existing techniques.

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