Comparison of KOH and TMAH Etching on SiNW Arrays Fabricated via AFM Lithography

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Abstract. Silicon nanowire (SiNW) arrays were fabricated by using top-down fabrication approach via atomic force microscopy (AFM) lithography on silicon-on-insulator (SOI) (100) substrate. Local anodic oxidation (LAO) technique carried out by AFM lithography to draw oxide pattern on top of the SOI substrate. The next steps to fabricate silicon nanowires involve chemical etching of the unmasked silicon by wet etching with the addition of organic additive. In this research, isopropyl alcohol (IPA) was used to improve the surface smoothness of silicon nanowires. Two types of etchant, potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH) with and without admixture of IPA at different etching time (10s, 20s, and 30s) were studied. After etching, the local oxide pattern was removed using dilute hydrofluoric acid (HF). The relationships between etching time with wall angle and surface roughness of the produced SiNWs were characterized in detail by using AFM and SEM. The result revealed that the wall angle for SiNW arrays that etched using TMAH was higher compare to KOH. Increasing the etching time produced large wall angle (θ) for both etchants. It was also found that the surface roughness for SiNW arrays was decreased with increasing time. SiNW arrays etched using KOH have higher surface roughness compared to TMAH. The obtained results also show that the etching depths increased with increasing etching time.

1. Introduction

Nanotechnology enclosed many processes that are vital in the fabrication of integrated circuits, memory devices, display units, biochips and biosensor. One of the key processes in nanofabrication is the creation and construction of functional unit in the size regime of less than 100 nm. Nanowire is one-dimensional (1D) nanostructure that has thickness, diameter or length in range of 0.1 nanometers to 100 nanometers. Silicon nanowire (SiNW) represents a class of 1D nanostructure of nanoscience and technology. There are two major processes involve in fabricating SiNWs; bottom-up and top-down processes. AFM lithography is one of the top-down processes that have been used during fabrication of SiNW arrays. The AFM lithography works based on the principle of interaction between the probe and substrate separation in close
contact condition < 1 nm. So, the AFM lithography can be operate in the contact mode [1-3] and noncontact mode [4]. Etching process is a must and plays a critical role when it is related to lithography technique.

The two major types of etching processes are wet etching [5] and dry etching [6]. Wet etching process involves the using of liquid chemicals or etchants in order to take off the substrate material. Dry etching using gaseous these gaseous diffused and reacted into the substrate and the byproduct expelled through the vacuum system. There are three types of dry etching; chemical reactions (by using reactive plasma or gases), physical removal (generally by momentum transfer), and a combination of chemical reactions and physical removal. On the other hand, wet etching is only involved a chemical process. Depending on the silicon wafer orientation and the type of etchant being used, wet etching can be either isotropic or anisotropic [7, 8]. Isotropic etching used wet etchants that removes the material uniformly in all directions, whereas anisotropic etching used wet etchants that are orientation dependent and these etchants will etch in different direction at different rates. Anisotropic wet etching is commonly used to fabricate simple microstructures and nanostructures on a single crystal SOI wafer [9]. The most frequently used anisotropic etchant include tetramethyl ammonium hydroxide (TMAH), potassium hydroxide (KOH), sodium hydroxide (NaOH), thylendiamine pyrocate chol water (EDP) and hydrazine/water [9, 10]. Nevertheless, hydrazine/water and EDP are not ideal because of their toxicity, instability and difficulty of handling. The KOH solution becomes a popular anisotropic etchant because of its good etching performance and non-toxic compared with NaOH. However, there is potassium ionic contamination for KOH etchant. TMAH also has attracted much attention because it was found that TMAH produced an excellent etching characteristics, non-toxic and without metal ions [11].

In the present work, a simple, low cost wet chemical etching method was used for the fabrication of SiNW arrays fabricated via AFM lithography on SOI wafer. SOI wafer was used because it has buried oxide that act as a barrier to prevent bulk leakage during electron movement from source to drain. The solution of KOH and TMAH with and without admixture of isopropyl alcohol (IPA) at different etching time (10s, 20s, and 30s) was studied. The IPA is the most commonly used additives and has been known as a very effective additive to increase the smoothness of silicon etched in anisotropic etchant. Its addition has proven useful in the case of silicon etching with TMAH and KOH solutions for obtaining smoother surfaces [11, 12]. The structural characterizations of SiNWs such as wall angle, surface roughness and etching depth were examined by atomic force microscope (AFM) and scanning electron microscope (SEM). The excellent geometrical features and surface of SiNW arrays are crucial for obtaining a semiconductor device with outstanding performance depending on the device application.

2. Experimental procedure

2.1 Fabrication of SiNW arrays

By using AFM lithography, the SiO₂ nanowire were patterned on the clean surface of SOI (100) wafer. The SiO₂ nanowire were designed by using a Nanonavi program vector scan under the scanning probe microscope (SPM) machine (SPI3800N/4000) at a temperature of 24–26 °C with relative humidity of 55–65%. Chromium/platinum (Cr/Pt) cantilever tip (Budgetsensors) with 13 kHz of resonant frequency and 0.2 N/m of force constant under contact mode was used at 9 V bias voltage with 0.4 μm/s writing speed. After the AFM lithography process, thin SiO₂ nanowire pattern were formed on the SOI wafer surface and functioning as the masking layer for the following etching processes.
2.2 Etching process of silicon and oxide tracks

There were two major steps of etching in order to create the SiNW arrays; etching of silicon layer and etching of oxide pattern. For this work, 25 wt% of KOH and 25 wt% of TMAH with and without admixture of 10 vol % of IPA were used to etch the silicon layer. This etching process was done in three different etching times which were 10 seconds, 20 seconds and 30 seconds. Heating temperature and stirring can be affected towards the formation of SiNW arrays during etching process. For this work, the mixture of KOH and TMAH with IPA was heat up to ~ 65˚C - 70 ˚C and stirred at 600 rpm. The second etching process was done to remove the oxide pattern by using dilute HF. The SOI wafer with SiNW pattern was immersed into the solution of 1: 30, HF: DIW for five seconds. Figure 1 shows the illustration of the steps during fabrication of SiNW arrays.

![Figure 1](image)

**Figure 1** The illustration of the steps during fabrication of SiNW arrays.

3. Experimental result and discussion

3.1 Effect of KOH and TMAH etching on SiNW arrays

Throughout this experiment we compared the effect of 25 wt% KOH and 25 wt% TMAH etching on SiNW arrays at different etching time (10 sec, 20 sec and 30 sec). Figure 2 shows the results of wall angle and surface roughness of SiNWs after etching process. The value of wall angle was varies based on the etching time. The wall angle for standard anisotropic etching of the silicon (100) wafer produced a wall angle with value of 54.7°. In this study, we obtained different value of wall angles at different etching time. It was clearly shown that wall angle of TMAH with value 40.08°, 46.57° and 47.96° was higher compare to KOH with value 13.67°, 25.83° and 34.12° at 10 sec, 20 sec and 30 sec of etching time respectively. The value of the wall angle decrease when the height and width of SiNWs are small and large, respectively. Different values of wall angle were obtained because different etching times produced different width and etching depth which affected wall angle value. Therefore, this situation can influence the wall angle measurement. Equation 1 shows the method to calculate the wall angle for every sample and the calculation of wall angle for SiNWs was illustrated in figure 3, where Ed is etching depth, and a is the adjacent segment that can be measured by using AFM.

\[
\theta = \tan^{-1} \frac{E_d}{a}
\]  

**Equation 1**
Table 1 shows the AFM topography of SiNW arrays on SOI substrates after etched with KOH and TMAH and the results were depicted in the form of graphs in figure 2 to facilitate understanding. From figure 2, it shows that surface roughness for SiNWs etched by KOH and TMAH decreased by increasing etching time. However, surface roughness of SiNWs that etched using KOH is higher than TMAH. The value of surface roughness for KOH was 2.23 nm, 1.69 nm and 1.19 nm and surface roughness for TMAH was 1.45 nm, 1.27 nm and 1.02 nm for 10 sec, 20 sec and 30 sec of etching respectively. Compared with figure 3 (a) and (b), it can be observed that the TMAH etching produced a very clean surface. Nevertheless, there were a lot of insoluble floccules were residual on the surface for the KOH etching, which may contaminate the silicon surface and affect the surface roughness.

Table 1. AFM topography of SiNW arrays on SOI substrates after etched using KOH and TMAH.

|          | 10 second | 20 second | 30 second |
|----------|-----------|-----------|-----------|
| KOH      | Ra=2.23nm | Ra=1.69nm | Ra=1.19nm |
| TMAH     | Ra=1.45nm | Ra=1.27nm | Ra=1.02nm |

Figure 2. Surface roughness and wall angle at different etching time for KOH and TMAH.

Figure 3. Silicon nanowire arrays with trapezoidal cross-section.
3.2 Effect of KOH and TMAH etching with addition of IPA on SiNW arrays.

Table 2 shows AFM topography of SiNW arrays on SOI substrates after etched with KOH and TMAH with the addition of IPA at different etching time. Figure 5 shows the variation of surface roughness for SiNWs at different etching time with different etchant, KOH and TMAH with and without addition of IPA which was measured using AFM by taking the average profiles of five SiNWs. From figure 5, it shows that surface roughness was decreased respectively when the etching time increased. It is also found that the addition of IPA for both of etching solution drastically reduced the roughness of SiNWs. This clearly indicates that the addition of IPA was very efficient in providing smoother etched surfaces as well as making the etching process more controllable. This phenomenon occurs because the 10 vol % of IPA in KOH and TMAH solution is concentrated, giving rise to the aggregation of IPA molecules and formation of a monolayer on the Si surface as obtained in the previous work that carried out by Yusoh and Yaacob. The formation of this monolayer promotes the adsorption of IPA molecules on the Si surface with the hydrocarbon chains binding to the hydrogen-terminated Si surface \[9\]. In addition, the hydroxyl groups (OH\(^-\)) of IPA are oriented toward the solution. This adsorption would prevent the OH\(^-\) from etching the Si surface and leads to the reduction in the etching rate.

**Table 2.** AFM topography of SiNW arrays on SOI substrates after etched using KOH and TMAH with addition of IPA.

|          | 10 second | 20 second | 30 second |
|----------|-----------|-----------|-----------|
| KOH+IPA  | Ra=0.75nm | Ra=0.48nm | Ra=0.32nm |
| TMAH+IPA | Ra=0.61nm | Ra=0.43nm | Ra=0.27nm |

![Figure 4. SEM image of SiNW after etched with (a) 25 wt% KOH and (b) 25 wt% TMAH at 30s.](image)
Figure 5. Surface roughness of SiNW arrays after etched using KOH and TMAH with and without addition of IPA at different etching time.

Hydrogen ions were produced during the wet etching process. This presence of hydrogen can be observed through the generated bubbles coming off near to the SOI surface and influence the surface roughness. The density and size of hillocks was affected by hydrogen bubble that produced during etching process [9]. The existence of hillocks after etching is the main contribution to the rougher surface. The addition of IPA produced a smooth surface (Figure 5) because it promotes the wettability of the etchants and decreases the formation of the hydrogen bubbles. As can be seen, the addition of IPA into KOH solution gave high surface roughness of SiNWs compare to TMAH solution. The lowest value of surface roughness obtained by SiNWs etched using TMAH with addition of IPA with 30 second of etching time, 0.27 nm.

4. Conclusion

In this work, KOH and TMAH comparative etching experiments on a SiNW arrays have been carried out at different etching time (5 sec, 10 sec and 15 sec) with and without addition of IPA. The thickness and height of SiNW arrays was controlled by the etching time. Nevertheless, the surface roughness of the SiNW arrays was influenced by the presence of IPA solution in the etchant (KOH and TMAH) and changed considerably with the changes in etching time. It has been found that TMAH solution has higher value of wall angle after etching process compare to KOH solution. More importantly, the surface roughness analysis shows that TMAH etching can obtain smooth surface compared with KOH etching. Unlike the clean surface for TMAH etching, KOH etching always results in the contamination of residual insoluble floccules on the silicon surface. The addition of IPA improved the surface roughness of SiNW arrays for both KOH and TMAH. However, the lowest surface roughness was obtained from SiNWs that etched using TMAH with addition of IPA with 30 sec of etching time.

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