Design and testing of high-speed interconnects for superconducting multi-chip modules

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Abstract
Superconducting single flux quantum (SFQ) circuits can process information at extremely high speeds, in the range of hundreds of GHz. SFQ circuits are based on Josephson junction cells for switching logic and ballistic transmission for transferring SFQ pulses. Multi-chip modules (MCMs) are often used to implement larger complex designs, which cannot be fit onto a single chip. We have optimized the design of wideband interconnects for transferring signals and SFQ pulses between chips in flip-chip MCMs and evaluated the importance of several design parameters such as the geometry of bump pads on chips, length of passive microstrip lines (MSLs) and number of corners in MSLs as well as flux trapping and fabrication effects on the operating margins of the MCMs. Several test circuits have been designed to evaluate the above mentioned features and fabricated in the framework of a 4.5 kA cm\(^{-2}\) HYPRES process. The MCM bumps for electrical connections have been deposited using a wafer-level electroplating process. We have found that, at the optimized configuration, the maximum operating frequency of the MCM test circuit, a ring oscillator with chip-to-chip connections, approaches 100 GHz and is not noticeably affected by the presence of MCM interconnects, decreasing by only about 3\% with respect to the same circuit with no inter-chip connections.

(Some figures may appear in colour only in the online journal)

1. Introduction

Very long ago it was recognized that superconducting transmission lines provide extremely low dispersion and, therefore, are suitable for transferring short picosecond pulses over relatively long distances [1] and for chip-to-chip communication [2]. Currently various kinds of superconducting transmission lines, e.g., coplanar lines (CL) [3], strip lines (SLs) and microstrip lines (MSLs) [4] are vitally important components of superconductor digital circuits. For instance, they are widely used for inter-chip routing of single flux quantum (SFQ) pulses in integrated circuits (ICs).

Most of the requirements for transmission lines, such as low losses and low signal distortion, are identical in semiconductor and superconductor technologies. There is one difference, however. All digital semiconductor devices are suited for operation with relatively high impedance loads. This enables using of transmission lines with the highest possible characteristic impedance, and 50 \(\Omega\) transmission lines are used almost exclusively. In contrast, the natural impedance of transmission line in superconductor electronics is around 4 \(\Omega\) as it provides the best matching to currently available Josephson junctions [5, 6]. With future technology advances [7], the matched impedance can increase up to...
Characteristic impedance of film microstrip lines (figure 1) in which the signal strip and ground plane are separated by dielectric films, and a desired dielectric thickness from $\sim 0.1 \mu m$ up to $\sim 1 \mu m$ could be selected simply by placing signal strips on different superconducting layers. High impedance (50 $\Omega$) transmission lines are also important for superconductor electronics because they serve as components of interfaces between semiconductor and superconductor circuits. However, they are quite similar to well investigated semiconductor counterparts [10] and require no special attention here.

10 $\Omega$–15 $\Omega$. Such low impedance lines are exotic for room-temperature electronics. They became useful only together with Josephson junctions. At optimal impedance matching [8] the known drivers and receivers required for connecting active Josephson circuitry by transmission lines contain only a few Josephson junctions, see, for example [8, 9]. At such low junction overhead, superconducting transmission lines have already become routine intra-chip connections when miniaturization and circuit density are of primary concerns.

The required miniaturization is achieved by using thin film microstrip lines (figure 1) in which the signal strip width $W$ and the ground plane are located on the same side of the substrate. Characteristic impedance $\rho$ is inversely proportional to width of the signal strip $W$:

$$\rho \sim \sqrt{1/W},$$

and can be easily adjusted to the desired level by a simple manipulation of the strip width. It is more difficult to manipulate by the thickness of the dielectric $t$. However, integrated circuits have several (three to six) levels of metallization separated by dielectric films, and a desired dielectric thickness from $\sim 0.1 \mu m$ up to $\sim 1 \mu m$ could be selected simply by placing signal strips on different superconducting layers. High impedance (50 $\Omega$) transmission lines are also important for superconductor electronics because they serve as components of interfaces between semiconductor and superconductor circuits. However, they are quite similar to well investigated semiconductor counterparts [10] and require no special attention here.

In recent years there has been significant interest in developing multi-chip module (MCM) technology for superconducting digital circuits in order to increase functionality and complexity of superconducting digital systems. This requires transferring SFQ (clock and data) pulses between chips with rates comparable to intra-chip rates in order to realize the full ultra-high-speed potential of superconductor ICs. The most challenging components of such MCMs are inter-chip connections. The fact of successful transmission of SFQ pulses between chips was reported long time ago [11, 12]. Unfortunately all earlier reports [11–15] either did not share interconnect design details or presented results of numerical simulations without experimental results [15]. In all these earlier works, the inter-chip data transfer rates were found to be very sensitive to the size and geometry of solder bumps used for chip-to-chip connections.

Electrical connections for signal transfer (in z-direction) between two chips in a flip-chip configuration are provided via some conducting medium (solder bumps, balls, gold studs, etc) connecting transmission lines on one chip with the corresponding lines on the other chip. This transition in z-direction should provide very good impedance matching in order to maximize the interconnect bandwidth and minimize signal reflection. Various highly developed interconnect technologies exist for MCMs with semiconductor ICs (see, e.g. [10]). So, it may seem to be a simple matter to adapt them to superconducting circuits. However, the mentioned above low $\rho$ value of superconducting transmission lines requires special optimization of interconnects that will be considered in this paper.

Our technique for connecting low impedance microstrip lines by evaporated gold bumps and some experimental results on data transfer rates in superconducting flip-chip MCMs were presented earlier [16]. Recently we have carried out more comprehensive optimization of wideband bumps and developed a more advanced fabrication technique with more compact bumps. Here we report our recent findings and, in particular, results of investigations of dependences of flip-chip interconnect performance on several factors including MSL length, the number and geometry of bumps connecting MSLs located on different chips, etc. We also show that our connection technique, while sensitive to thin film patterns in the chip (x–y) plane, is quite insensitive to the bump geometry (bump shape and height). This insensitivity of the proposed technique to the features of chip connecting media (bumps) is a great advantage over the previously used approach [14] that, in contrast, is very sensitive to the details of bump geometry as discussed in the cited paper.

### 2. Design of chip interconnects

To introduce our technique for connecting low impedance microstrip lines located on different chips, let us consider two simplified examples. Assume we need to join together signal strips of two similar MSLs, see figure 2(a), using some bonding medium that is slightly unmatched, e.g., non-superconducting. (Let us repeat that this is the artificial example.) It is intuitively clear that the impact of mismatching would be weaker if the strip edges in the joint are not straight (figure 2(a)) but tapered as shown in figure 2(b). In this case the contact area is larger and undesirable contact resistance of the joint is lower. Since our real tapering technique is quite complicated, we think it is appropriate to show yet another example of tapering in figure 2(c). Here our goal is to taper the electromagnetic width (and hence the impedance) of a microstrip without tapering its signal strip. This can be achieved by tapering a much wider ground plane (contoured by black line in figure 2(c)) under the strip.

To connect two MSLs located on different chips, it is necessary to connect their signal strips and ground planes. In the flip-chip configuration, the assembly is much easier if geometries and vertical (layer) structure of layers to all bump connections on both chips are made identical (figure 3(a)), and only conducting joints (bumps) are placed between them. We strictly follow this recommendation, and our design technique is restricted to optimization of thin film patterns of interconnects in the vicinity of the bumps. Our goal is to make...
Figure 2. Straight (a) and tapered ((b), (c)) cuts of microstrip lines is an essential part of the suggested bump design technique. Bonding stuff connecting the left and right strips in (a) and (b) is shown in gray.

Electrodynamics properties of the signal bump connection similar to the discussed earlier (figure 2(b)) properties of a tapered joint of two strips. Since the bump material is usually non-superconducting and we want to decrease both its resistance and the contact resistance of the joint, the bump diameter should usually be made larger than the width of the strips that is typically $\sim 10 \, \mu m$ or less. This requires making a widening of the signal strip (a contact pad) for placing there the bump. An example of this widening, making a circular contact pad, is shown in figure 3(b). In this case, the current from the signal strip on the base chip (shown in blue) flows up (in $z$-direction) to the strip on the flip chip (orange) along the perimeter of the bump. Because of ‘impedance tapering’ the current is uniformly distributed along the perimeter. The required tapering is achieved by making a narrow circular cut (a moat) in the ground plane film around the bump contact pad, shown as a white donut in figure 3(c). The complementary signal bump contact pad on the flip chip has exactly the same design but is simply mirror-inverted with respect to the $y$-axis, as shown in figure 3(b). As a result, the whole structure after flip-chip bonding should behave almost as a uniform microstrip line which has a transition in the $z$-direction from the MCM carrier (base chip) onto the flipped chip. To reduce the resistance of the non-superconducting joint, the bump height should be made as low as technologically possible, just enough to provide for the needed compression.

A major deviation from this ideal model is caused by four ground bumps surrounding, but remote from, the signal bump and providing electrical connection of the ground planes of two chips. (In general, the ground bumps can be shared between the neighboring MSLs.) It is well known that in an MSL the signal current flows in the microstrip while the return current mainly flows in the ground plane area under the microstrip and the fringing is usually small. However, this is not the case in a flip-chip MCM because the return current must flow via the ground bumps in order to get from chip to chip. So the return current must ‘depart’ from under the signal strip. Such distribution of the return current causes an additional parasitic inductance. This parasitic inductance is low because the magnetic field induced by this current is ‘boxed’ in a small volume between two ground planes (the distance between the ground plane of two chips in $z$-direction is much less than the distance between bumps in $x$–$y$ plane). Since we deal with mainly 2D problem, the inductance

$$L_P = L_{\square} N$$

is measured in the number of squares that only logarithmically depends on the radius of contact pad, $R_1$, and the distance between the signal and ground bumps, $R_2$:

$$N = \ln[R_2/(R_1)]/2\pi.$$
The sheet inductance \( L_{\text{C}} = \mu_0 t_m \) is defined by magnetic gap \( t_m = t + 2\lambda \), where \( \lambda \) is magnetic field penetration depth and \( t \) is the spacing between the carrier and the flip-chip ground planes. At the typical values, \( t_m = 3 \mu m \) and \( L_{\text{C}} \approx 3.8 \) pH. At \( R_2/R_1 = 1.35 \) the number of squares equals 0.21. As a result, the parasitic inductance \( L_P \) is about 0.8 pH. Thus, even at a low impedance of the MSL (e.g., \( \rho \approx 4 \Omega \)), the cutoff frequency \( f \sim \rho/2\pi L_P \) corresponding to this parasitic inductance is \( \sim 840 \) GHz. In practice, the cutoff frequency can be even higher. This is because the estimated lump inductance \( L_P \) is only a simplified model for an inductance distributed along the microstrip line. The small impact of the parasitic inductance could be further compensated by a local increase of the signal strip widening.

We complemented the described qualitative design considerations by numerical simulations using Full-wave 3D Planar Electromagnetic Field Solver Software [17]. During the simulations we indeed could observe some resonant reflection related to mismatch effect discussed in the previous paragraph. The reflection was observed to be either inductive or capacitive, depending on numerical value of \( R_3 \) (see figure 3(c)) that served as the main adjustable parameter. The optimized value of \( R_3 \) corresponds to no noticeable reflection in simulations. At this value of \( R_3 \), an excessive capacitance of the signal contact pad circle exactly compensates the parasitic inductance.

Note that it is difficult to compare our approach with the one used in [14]. This is because we optimized the matching by tuning patterns of superconducting thin films deposited on the base and flip chips. In our approach, the matching conditions only weakly (logarithmically) depend on the dimensions and distances between the bump pads. In \( z \)-direction, our approach relies on the use of very short bumps giving small parasitic inductance. In contrast, the authors of [14], considering large bumps, illustrated that the matching depends mostly on dimensions and shape of solder bumps and distance between them, whereas the thin film patterning was not taken into the consideration. As a result, the floor plans are even not shown in the cited paper.

Similarly to the described MSL interconnects, we also optimized flip-chip interconnects between 50 \( \Omega \) coplanar waveguide (CPW) lines serving for delivery of RF signals and clock to chips in MCMs. The proper matching was achieved by tapering (widening) the CPW gap in the ground plane and the central line of the CPW around the signal bump contact pad.

### 3. Fabrication of circuits and MCMs

Superconducting integrated circuits used in this work for MCM testing have been fabricated using HYPRES process for superconductor electronics and Nb/Al/A1Ox/Nb Josephson junctions with 4.5 ka cm\(^{-2}\) critical current density [6, 7]. This process uses four Nb superconducting layers: 100 nm thick ground plane layer, M0, and three wiring layers M1 (150 nm), M2 (300 nm), and M3 (500 nm). All contact pads for placing bumps present a stack containing all these layers, so the pad can be attached to any microstrip line formed in any of the superconducting layers. All dielectric layers in the stack are removed. The total thickness of Nb stack is, hence, 950 nm. The top surface of the stack was covered by a layer of underbump metallization (UBM) consisting of Mo/Pd/Au multilayer with the following thicknesses of the layers: 50 nm (Mo), 200 nm (Pd), and 100 nm (Au).

In our previous work, bumps for flip-chip bonding were formed at the very last step of the wafer fabrication by using a wafer-level lift-off process and e-beam evaporation of the bump material (Au or Cu with Au capping layer) [16]. In this work we have developed an electroplating process for depositing bumps in order to minimize the use of gold evaporation and the process cost.

For electroplating of uniform bumps all contact pads where bumps are intended to be placed need to be electrically connected. To achieve this we changed a few last steps in the standard HYPRES process [18] as follows. After the last Nb wiring layer deposition (layer M3), the entire wafer surface is covered by a well conducting metal. In the standard HYPRES process [18], the next step would be patterning of this layer that would create electrically isolated contact pads. Instead, we used this continuous M3 layer to perform electroplating. Firstly, a UBM was formed on M3 layer by a lift-off process and e-beam evaporation. A multilayer of Mo/Pd/Au with the thicknesses given above was used. The lift-off mask was formed by an image reversal process using AZ5214E photoresist. After the lift-off, a new photolithography was done to create circular openings in the photoresist for electroplating of bumps on the UBM. Since the rate of electroplating depends on the local current density, all bumps were chosen to have the same diameter (30 \( \mu m \)) in order to obtain uniform bump heights. Secondly, indium bump electroplating was done using an electrolytic cell with indium sulfamate bath [19] and a solid In anode. The total plating current was 20 mA, and the typical plating time was 3 min. The typical bump height was 5 \( \mu m \). Indium bumps were plated on contact pads located on flip chips and on the carrier (base chip). The typical picture of the plated bump is shown in figure 4. After the plating, the photoresist mask was removed and the wafer was cleaned. Finally, the M3 layer was patterned by using photolithography and reactive ion etching. During the etching In bumps were protected by photoresist mask. The final view of the fabricated interconnects is shown in figure 5 for a 50 \( \Omega \) CPW line.

After wafer dicing, the MCMs were assembled on FC-150 flip-chip bonder. A force of \( \sim 5 \) g per bump was applied to press In bumps on the flip chip into the corresponding bumps on the carrier and join them together. A cryogenic adhesive (epoxy Tra-Bond 2115) was added between the chip and the carrier to increase the bonding strength, stability, and improve heat conduction between chips [20]. The adhesive was cured at 65 \( ^\circ \)C for 90 min. The adhesive was chosen to have the thermal expansion coefficient larger than that of Si and Nb. Therefore, the bumps become additionally compressed upon MCM cooling.

For many practical applications, MCMs would need to operate not immersed in liquid helium but in vacuum on closed cycle cryocoolers. This chip cryopackaging is
Figure 4. SEM picture of electroplated In bump on top of Nb contact pad with underbump metallization. Bump diameter is 30 µm and height is 4 µm. It has a slight mushroom shape due to slope of walls of plating holes in photoresist.

Figure 5. SEM picture of the fabricated CPW interconnects, showing electroplated In bumps in the centers of all contact pads. Each connection to a signal line (shown in the center) is surrounded by four ground plane connections which can be shared between adjacent signal lines. Niobium ground plane film is removed around the signal line connection and under the signal line to provide a proper 50 Ω impedance of the line and optimize the interconnect bandwidth. These areas look darker black in the SEM image due to fewer backscattered electrons.

4. MCM testing technique

Our approach to characterization of SFQ pulse transmission through inter-chip connections is based on a conventional ring oscillator shown in figure 6 and described, for example, in [4]. The ring contains a Josephson transmission line (JTL) and a microstrip line that can be ‘broken’ by one or several transitions through bumps. The rate of pulse transmission is controlled in two different ways. A coarse control is provided by the number of SFQ pulses circulating in the ring. The number of pulses can be changed by injecting a new pulse via a merger cell that is also part of the ring. A fine control is provided by adjusting the bias current applied to the JTL. The quality of the oscillator and, therefore, of the chip-to-chip connections is characterized by margins for the bias current applied to the receiver (marked as Res in figure 6) that converts electromagnetic pulses propagating along the MSL into SFQ pulses. The operation of the ring is monitored by measuring the dc voltage and, therefore, the rate of pulse traveling along the ring. (The measured dc voltage is related to the number and the oscillation frequency of SFQ pulses in the ring by the Josephson relation.) Transmission failures are detected via spontaneous changes of the voltage corresponding to a loss or creation of an extra pulse.

One reference circuit was intentionally laid out without chip-to-chip connections and used to evaluate the properties, in particular the maximum frequency of operation, of the circuit without any bump crossings. All test circuit components were designed using Josephson junction logic blocks developed at Stony Brook, and were designed to minimize parasitic flux trapping using methods described in [27, 28].

All JTL sections include LR components shown in figure 6(b). They create a strong anti-bunching effect and therefore provide a more uniform distribution of pulses along the ring. The signal strips of MSLs were laid out in M2 layer, while M0 layer served as the ground plane. Lengths of the MSLs were varied from 1.8 to 20 mm. We used both straight MSL and meandered ones (containing 90° turns) to increase the length. Although a 90° turn of microstrip line usually does not cause any noticeable problems at microwave frequencies, it might be reasonable to consider such corners as a potentially disturbing factor for circuits operating with picosecond SFQ pulses having THz frequency components.

All design variations and parameters of studied interconnects are given in tables 1 and 2. Their expected influence on the performance of interconnects can be qualitatively explained as follows. As was mentioned, the main optimization parameter was radius of M2 disk, $R_3$, shown in figure 3(c). An increase of $R_3$ increases overlap with the ground plane and leads to a larger capacitance of the bump pad to the ground and to a lower inductance of the connection. Only the overlapping part of the disk (located outside of the circular moat in the ground plane shown as white ring in figure 3(c)) contributes to the effective inductance and capacitance, because the moat isolates the ground plane from the pad. It is difficult to qualitatively predict the effect of moat width, $dM$, because of 3D distribution of magnetic conductivity for the existing and planned superconductor electronics systems including Digital-RF systems described in [21–25]. Thermal conductivity of MCMs is then important because heat released on superconducting chips has to be removed via the MCM bumps and cryogenic adhesive to the cryocooler’s cold plate without heat exchange liquid or gas. Thermal conductivity of the adhesive used in our flip-chip MCM at low temperatures was studied in [20]. It was found that heat conduction through the adhesive is larger than through the metal bumps. Additionally, the heat conduction in the MCM can be improved by loading the adhesive with carbon nanotubes [26].
Figure 6. (a) Block diagram of the ring oscillator used for testing inter-chip SFQ pulse transmission. SFQ driver and receiver are marked Drv and Res, respectively. (b) The element of the Josephson transmission delay line (JTDL) with $L_5/R \sim 5$ ps.

Table 1. Parameters of chip interconnects in different test circuits (ring oscillators) studied.

| Test circuit | Bump pad design $\mu$m | Comment |
|--------------|------------------------|---------|
| Expt. 2, 3, 5, 8 | $dM = 5, R_3 = 45, dC = 7.5$ | The best geometry according to numerical simulations |
| Expt. 4 | $dM = 5, R_3 = 45, dC = 0$ | No misalignment between pad and M2 layer disk |
| Expt. 6 | $dM = 10, R_3 = 45, dC = 7.5$ | The width of the ground plane donut hole is increased |
| Expt. 9 | $dM = 5, R_3 = 50, dC = 10$ | The capacitance of M2 and the misalignment are increased |
| Expt. 10 | $dM = 5, R_3 = 40, dC = 7.5$ | The capacitance of M2 circle is reduced |
| Expt. 7 | $dM = 5, R_3 = 45, dC = 0$ | No high frequency tuning structure |

Table 2. Parameters of chip-to-chip connections and the maximum frequency of operation.

| Test circuit | Length of MSL $\mu$m | No. of bumps | No. 90° turns | Maximum frequency GHz |
|--------------|----------------------|--------------|--------------|----------------------|
| Expt. 1 (Ref.) | 1950                | 0            | 4            | 96 (MCM # 1)        |
| Expt. 2     | 4100                | 2            | 4            | 80 (MCM # 1)        |
| Expt. 3     | 2300                | 2            | 4            | 82 (MCM # 1)        |
| Expt. 4     | 2450                | 4            | 10           | 76 (MCM # 2)        |
| Expt. 5     | 19570               | 2            | 16           | 82 (MCM # 1)        |
| Expt. 6     | 2150                | 2            | 4            | 67 (MCM # 1)        |
| Expt. 7     | 4350                | 2            | 4            | none (MCM # 1)      |
| Expt. 8     | 4350                | 2            | 4            | 87 (MCM # 1)        |
| Expt. 9     | 2450                | 4            | 10           | 93 (MCM # 1)        |
| Expt. 10    | 2450                | 4            | 10           | 82 (MCM # 2)        |

and electric fields in the moat area. Although 3D effects are expected to be quite weak, we included $dM$ into our list of studied parameters. Finally, the linewidth tapering discussed above was varied by varying disk misalignment, $dC$. This misalignment produces a tapered disk shape (shown in blue in figure 3(c)) and gives a slow reduction of the active width of the signal line (and therefore the increase of its characteristic impedance) going from right to left. An ideal misalignment $dC$ would be such that gives zero effective width of the tapered disk on the left edge. However, this would contradict the fabrication design rules [18]. Therefore, we tested different misalignments that are more preferable from this point of view.

Test circuits 4, 6, 7, 9, and 10 all have some modifications of signal bump pads with respect to the optimal shape found in numerical simulations. E.g., in test circuit 6, the moat width, $dM$, is increased from 5 to 10 $\mu$m. In test circuits 4, 9, and 10 we varied $dC$ and $R_3$, whereas $dM = 5 \mu$m was kept the same. In test circuit 7, the M2 misaligned structure was completely removed, that is expected to convert the signal bump into a low frequency structure. In circuits 4, 9, 10, we placed 4 bumps interrupting the MSLs because we expected the adverse effects of bump connections to multiply, making it easier to detect.

5. Experimental results

The measurements have been carried out in a cryocooler setup. To prevent the undesirable flux trapping we followed the thermo-cycling and magnetic shielding procedures described in [27, 28]. The measurement results were quite reproducible if we followed the shielding precautions.
Let us start with the reference test circuit laid out with MSL without bump crossings. The microstrip line is 20 µm wide, 1950 µm long, and contains four 90° turns. The measurement results are collected into two plots shown in figure 7. The left plot (figure 7(a)) shows the upper and lower margins for receiver bias current as a function of the pulse circulation rate. The plot shows the margins at 18 different circulation rates. In fact, we can extract margins at any particular rate because, as was mentioned earlier, the rate can be tuned by changing the JTL bias. Figure 7(b) shows these transmission rates at a different number (one to eighteen) of pulses traveling along the ring. It is easy to check that at higher rates the shown traces cover all frequencies. It means that it is possible to set SFQ pulse transmission at any rate within the covered range and measure the receiver margins at this particular rate. However, this procedure is quite time consuming. To speed up the measurements, all other circuits have been investigated at one JTL bias current corresponding to the center of its one JTL bias current corresponding to the center of its measured margins. According to figure 7(a) the margins are almost frequency independent at lower rates and partially degrade above ∼80 GHz. Ninety six GHz was the highest frequency of stable operation for this reference circuit. At higher frequencies the margins sharply collapse to zero and no data are presented. The highest observed on-chip transmission frequency is somewhat below our expectations and the previously obtained results for circuits with evaporated bumps [16]. It is determined by the maximum speed of operation of circuits made in this particular fabrication run and has nothing to do with interconnects. However it is sufficiently high to investigate the disturbing impacts of interconnect matching and bump bonds on chip-to-chip transmission.

Test results for circuits with inter-chip connections are shown in figures 8–10 and summarized in table 2. As was said, the reference circuit (Expt. 1) demonstrated the best performance with 96 GHz maximum frequency. The presence of any bump connections degrades the circuit performance (the maximum transmission rate). However, the observed degradation is quite small. For the optimized pad geometry (Expts. 2, 3, 5 and 8) the maximum frequency was in the range from 80 to 87 GHz. The degradation is stronger for interconnects with intentionally distorted pad geometries. The worst performance with about 60 GHz maximum rate was observed in Expt. 4, where pads have been intentionally made without any misalignment between the pad and M2 disk (dC = 0). Interconnects with a wider cut in the ground plane (Expt. 6) also show more degraded performance with maximum frequency about 67 GHz.

In Expt. 9 we intentionally increased the size of M2 disk with respect to the size optimized in electromagnetic simulations. This increased the capacitance and decreased the inductance. At the same time, the line tapering was also increased by increasing the misalignment, dC. This circuit demonstrated the best performance, giving the highest maximum frequency of chip-to-chip transmission (∼93 GHz) among all studied interconnects. It is likely that our simulations slightly underestimate some parasitics (inductance), and thus small adjustments of the tuning parameters improved the performance. This experimentally found adjustment to the parameters optimized in simulations should be regarded as the experimentally optimized geometry of interconnects. At this new optimum, the maximum chip-to-chip SFQ pulse transmission rate through 4 bump bonds in series is only ∼3% lower than in the control circuit without any bump crossings.

As expected, in a test circuit with removed impedance matching structure in the interconnect (Expt. 7), no chip-to-chip SFQ pulse transmission through the MSL interrupted by this interconnect was found. These experiments confirm the importance of a careful high frequency design of the chip-to-chip connections and high sensitivity of the maximum inter-chip transfer rates to relatively small variations in the interconnect tuning structure, which is not surprising given that picosecond SFQ pulses contain very high frequency components.

Some of the experiments were repeated for the second MCM assembled from chips fabricated on a different wafer in order to check the reproducibility of the results. Figure 10 illustrates the results of two measurements (Expt. 3 and Expt. 9), demonstrating quite low spread of performances between
Figure 8. The upper and lower margins of the receiver bias current as a function of SFQ pulse transmission rate between the flip chip and the MCM carrier for test circuits with interconnect design optimized in simulations (\(dM = 5, R3 = 45, dC = 7.5\)): (a) Expt. 2; (b) Expt. 3; (c) Expt. 5; (d) Expt. 8.

Figure 9. The upper and lower margins of the receiver bias current as a function of SFQ pulse transmission rate between the flip chip and the MCM carrier for test circuits with different bump pad designs as indicated in table 1: (a) Expt. 6; (b) Expt. 4; (c) Expt. 9 and (d) Expt. 10.

As can be seen in figures 7–10, besides the existence of the maximum operation frequency discussed above, we also observed a relatively sharp decrease of the upper operation margin above a certain frequency. This frequency is usually in \(~50\) to \(85\) GHz range and varies from circuit to circuit; compare, e.g., experiments 2 and 8 in figure 8. At the same time, the lower operation margin tends to be much less frequency dependent and usually has no features at this frequency. We are not sure about origins of this behavior. We are confident that it is not caused by microstrip line resonances. This is because the above described frequency lies well above the fundamental resonance frequencies in the used microstrip lines. (The possible fundamental resonances
at $L = \lambda_g/2$ and $\lambda_g/4$, where $\lambda_g$ is the guided wavelength, for the studied range of microstrip lengths $L$ are in the range from $\sim 2$ to $25$ GHz.) Also, this feature was observed in the control circuit (at $\sim 77$ GHz, see figure 7(a)) that does not have bump connections and associated potential discontinuities in the microstrip line. This makes it unlikely that the feature is in some way related to the presence of bump bonds and chip-to-chip interconnects. A probable cause of it could be in an internal dynamics of the ring oscillator and complex dynamics of vortices traveling along Josephson transmission lines. We are planning to investigate the problem in future.

6. Conclusion

In this paper, we described and experimentally proved our design technique for MCM interconnects with ultra-high chip-to-chip data transfer rates in flip-chip MCMs. We carried also some stress tests. In particular, we allowed the microstrip lines to pass through several (up to 4) bump bonds and intentionally distorted bump pad geometry away from the optimal. All stressed circuits remained operational, and even the lowest observed chip-to-chip transfer rate ($\sim 60$ GHz) well exceeds (a factor of 2–4) the maximum clock rates achievable in simultaneously fabricated complex digital circuits using HYPRES 4.5 kA/cm$^2$ fabrication technology. This means that the developed interconnect design, wafer bumping and flip-chip MCM assembly are fully suitable for this as well as the next node of the superconductor integrated circuit fabrication technology where the clock rates are expected to rise to $\sim 60$ GHz. Bond-bumped chip-to-chip connections remained stable within the entire investigated range (1.8–20 mm) of MSL lengths. Some MSLs contained up to sixteen 90° turns. We did not detect any problems with magnetic flux that could be trapped in the bump pads. The measured MCMs successfully passed mechanical and thermal stressing, going over 100 thermo-cycles. All these observations could be used as a proof that the developed design technique is quite robust against unavoidable deviations in chip fabrication and MCM assembly technologies and delivers about 100 GHz data transfer rate at transferring picosecond SFQ pulses between integrated circuits.

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