A New Type of Tri-Input TFET with T-Shaped Channel Structure Exhibiting Three-Input Majority Logic Behavior

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In this paper, we propose a new type of tri-input tunneling field-effect transistor (Ti-TFET) that can compactly realize the “Majority-Not” logic function with a single transistor. It features an ingenious T-shaped channel and three independent-biasing gates deposited and patterned on its left, right, and upper sides, which greatly enhance the electrostatic control ability between any two gates of all the three gates on the device channel and thus increase its turn-on current. The total current density and energy band distribution in different biasing conditions are analyzed in detail by TCAD simulations. The turn-on current, leakage current, and ratio of turn-on/off current are optimized by choosing appropriate work function and body thickness. TCAD simulation results verify the expected characteristics of the proposed Ti-TFETs in different working states. Ti-TFETs can flexibly be used to implement a logic circuit with a compact style and thus reduce the number of transistors and stack height of the circuits. It provides a new technique to reduce the chip area and power consumption by saving the number of transistors.

1. Introduction

Due to the 60 mV/dec physical limit in subthreshold swing (SS) of conventional MOSFETs at room temperature, it is unrealizable to reduce power consumption by infinitely reducing the supply voltage, which would seriously degrade the circuit performance [1, 2]. The tunneling field-effect transistor (TFET) with band-to-band tunneling (BTBT) transport mechanism can achieve steep SS far below 60 mV/dec [3–8]. TFETs are considered as one of the best candidates for the next generation of low-power devices because their manufacturing process is compatible with modern CMOS and FinFET technology. However, TFETs also face some problems such as low turn-on current and ambipolar behavior [9–12].

Multigate transistors with strong channel control ability have higher turn-on current than the single-gate ones. It can also effectively suppress short channel effects and reduce leakage current, which has attracted researchers’ wide interest. However, most of the current multigate TFETs have only a single input terminal [13–16]. Previous studies have shown that the double-input TFET has better signal processing ability than the single-input one. For example, the TFET with two symmetric gates can accept two input signals and produce a corresponding output. Thus, it can implement a Boolean logic function in a single transistor [17–19].

In this paper, a new type of TFET with three-input terminals (Ti-TFET) is proposed. The “Majority-Not” logic function can be realized compactly by using Ti-TFET. The invented T-shaped channel (T-channel) enhances the gate control ability on channel potential of any two gates, thus increasing its turn-on current. Taking N-type Ti-TFET as example, the influence of the coupling effect on the potential, energy band, and current density distribution is analyzed. The results show an interesting feature that a single Ti-TFET exhibits the three-input “Majority-Not” switch behavior and a reconfigurable logic function between NAND and NOR. Device characteristics such as turn-on current, leakage current, and the ratio of turn-on/turn-off current \( \frac{I_{on}}{I_{off}} \) are optimized by choosing the appropriate work function and body thickness. The main objective of this paper is to demonstrate a novel TFET technique by taking silicon-based
TFET as an example to expand the logic function in a single transistor. In order to obtain an acceptable turn-on current, we select the supply voltage of 1 V in this paper.

The paper is composed of five sections. Section 2 describes the simulation approaches and main physical models used to model the proposed device in the TCAD environment. Section 3 describes the simulation results, and then the device optimization methods are described in Section 4. The conclusion and summary are included in Section 5.

2. Device Structure and Simulation Approach

In this section, taking N-type Ti-TFET as an example, the structure and parameters of the device are introduced [20], and then the TCAD simulation models used in this paper are presented. Finally, the fabrication process flow of the Ti-TFET device is explained.

The 3D structure of the N-type Ti-TFET is shown in Figure 1(a). The cross section along the center of the Y-Z plane of the device is shown in Figure 1(b). The special T-shaped channel can be divided into a horizontal channel and a vertical channel. The horizontal channel can be divided into two subchannels: Channel 1 and Channel 2. For convenience, we call the vertical channel, Channel 3. The region in red is the high-k dielectric layer HfO$_2$. Three independent-biasing gates, Gate 1, Gate 2, and Gate 3, are deposited and patterned on the surface of the oxide layer. The spacer is used to isolate the gates from the source and drain.

The optimized parameters of the Ti-TFET are shown in Table 1. The doping concentration of heavy P$^{++}$ doped source, heavy N$^{++}$ doped drain, and the light N-doped channel are 1 × 10$^{20}$ cm$^{-3}$, 1 × 10$^{18}$ cm$^{-3}$, and 1 × 10$^{14}$ cm$^{-3}$, respectively, which ensures the abrupt doping of the source-to-channel and small leakage tunneling current. The body thickness $T_b$ of the T-shaped channel is set as 5 nm, which ensures that the coupling strength of all the gates on channel potential is large enough. The source length $L_S$, channel length $L_{ch}$, and drain length $L_D$ are all selected as 30 nm. The thickness of the High-k dielectric layer is set as 3 nm for appropriate gate capacitance [21]. In order to obtain the required threshold voltage, we use TiN$_x$ as the gate material with controllable nitrogen concentration to realize the adjustable work function $\Phi$ [22].

The fabrication process flow for a Ti-TFET is detailed in Figure 2. We started from an initial Si wafer, with epitaxial silicon film thinned above 60 nm, and then Gate 1 was deposited and patterned on the oxide layer. After sacrificial oxide layer deposition, molecular bonding on handling oxidized wafer was achieved. The T-shaped channel was formed by selective etching and chemical mechanical polishing (CMP). Later, Gate 2 and Gate 3 were deposited and patterned on the right and left sides of the T-channel, respectively. Finally, the initial substrate and buried oxide (BOX) were removed chemically.

In this paper, the electronic performance of the proposed device is verified and optimized in the 3D simulation environment with SILVACO TCAD. The Kane BTBT model considering the position-dependent band gap and the magnitude of the electric field is used to describe the carrier transport mechanism. This model is widely used in nanowire and other 3D TFETs [23, 24], and its theoretical analysis is in good agreement with the experiments. Along with that Shockley-Read-Hall Recombination models, Band Gap Narrowing Effects, Fermi-Dirac Statistics, and Doping-Dependent Mobility Model are also employed for more accurate simulation results. Since the minimum bulk silicon thickness of the device is 5 nm, quantum confinement effects are considered to calculate the potential, the carrier concentrations, and the discrete subband spectrum of both conduction and valence bands.

3. The Device Performances

In this section, the current density distribution, current characteristics, and energy band distribution are analyzed. In order to obtain an acceptable turn-on current, we select the supply voltage of 1 V in the simulation.

3.1. Current Density Distribution in the Different Switching States.

The BTBT mainly occurs on the interface between the source and channel. We intercept the contour plots of the current density on this interface, as shown in Figure 3. The greater the current density in the channel, the larger the total current flowing through the channel. There are three subchannels in the T-shaped channel, and each subchannel has two current paths near the channel surface. Therefore, there are six current paths in the entire T-shaped channel.

When $V_{GS1} = V_{GS2} = V_{GS3} = 1$ V, the current density distribution on the interface between source and channel is shown in Figure 3(a). In this switching state, the coupling effect between all the gates on the three subchannels is the strongest, and maximum drain current flows through all surfaces of all the three subchannels.

When $V_{GS1} = 1$ V, $V_{GS2} = 0$ V, and $V_{GS3} = 1$ V, the coupling effect between Gate 2 and Gate 1 (or Gate 3) is weakened, resulting in the decrease of the control ability on the Channel 1 and Channel 3, so that the currents flowing through Channel 1 and Channel 3 are reduced, as shown in Figure 3(b). In this switching state, since the coupling effect of Gate 1 and Gate 3 on Channel 2 is still strong, a relatively large current still flows through both surfaces of Channel 2.

When $V_{GS1} = 0$ V, $V_{GS2} = 1$ V, and $V_{GS3} = 1$ V, the current density distribution is shown in Figure 3(c). In this switching state, the coupling effect between Gate 1 and Gate 2 (or Gate 3) is weakened, and the control ability on Channel 1 and Channel 2 decreases, but a relatively large current still flows through both surfaces of Channel 3.

When $V_{GS1} = V_{GS2} = 0$ V and $V_{GS3} = 1$ V, the current density distribution is shown in Figure 3(d). The channel coupling effect between all three gates is simultaneously reduced. From Figure 3(d), almost no current flows through Channel 1, but Gate 3 is still biased at 1 V, and few carriers flow through the right surface of Channel 3 and the lower surface of Channel 2.

From the above analysis of current density distribution, it can be seen that each gate of the Ti-TFET controls two
subchannels. When only one gate is biased at 1 V, this gate has weak control on corresponding subchannels, and thus the corresponding drain current is small. When the bias voltages of the two gates are 1 V, the T-channel structure can generate a strong coupling on the corresponding subchannel, resulting in an exponential increase in drain current. Therefore, the proposed T-channel structure allows the device to show the “Majority-Not” switching behavior.

3.2. Device Characteristics of Ti-TFETs. The drain current of the device depends on the gate-to-source voltage \( (V_{GS1}, V_{GS2}, \text{and } V_{GS3}) \). In order to analyze the DC characteristics of the Ti-TFET device comprehensively, we carry out DC sweep analysis for a gate voltage with the fixed biasing voltage of 1 V or 0 V for the other two gates. Considering the symmetry between Gate 2 and Gate 3, the DC sweep analysis of the Ti-TFET is performed only for Gate 1 and Gate 3. The simulation results of the transfer characteristics \( (I_D-V_{GS1} \text{ and } I_D-V_{GS3}) \) with fixed \( V_{GS}=1 \text{ V} \) are shown in Figures 4(a) and 4(b), respectively.

Figure 4(a) shows the transfer characteristics \( (I_D-V_{GS1}) \) of the device with the fixed biasing voltages \( (V_{GS2} \text{ and } V_{GS3}) \) of 1 V or 0 V. Figure 4(b) shows the transfer characteristics \( (I_D-V_{GS3}) \) of the device with the fixed biasing voltages \( (V_{GS1} \text{ and } V_{GS2}) \) of 1 V or 0 V. In Figure 4, the DC sweep analysis of the Ti-TFET is classified as eight modes. For example, the mode \( M_{X10} \) shown in Figure 4(a) indicates that the DC scan analysis for the gate-to-source voltage \( V_{GS1} \) is performed with \( V_{GS2}=1 \text{ V} \) and \( V_{GS3}=0 \text{ V} \), while the mode \( M_{10X} \) shown in Figure 4(b) indicates that the DC scan analysis for the gate-to-source voltage \( V_{GS3} \) is performed with \( V_{GS1}=1 \text{ V} \) and \( V_{GS2}=0 \text{ V} \).

In the modes \( M_{X11} \) and \( M_{11X} \), the drain current of the device ranges from 1.45 \( \mu \text{A} \) to 4.28 \( \mu \text{A} \), and thus the device is turned at all the times of the modes \( M_{X11} \) and \( M_{11X} \), as shown in the two yellow lines in Figure 4. In modes \( M_{00X} \) and \( M_{X00} \), the drain current of the device is always less than 1 nA, and thus the device is always turned off, as shown by the two blue curves in Figure 4. In the other four modes, \( M_{X01}, M_{X10}, M_{01X}, \text{and } M_{10X} \), the device changes from turn-off state to turn-on state when the gate-source voltage increases from 0 V to 1 V. When all the three gates are shorted, the transfer characteristics of the N-type Ti-TFET are shown in Figure 4(c). As we can see, the proposed device with shorted gates behaves similar to a conventional N-type TFET with a high threshold voltage. The Ti-TFET exhibits the minimum subthreshold swing \( SS \) (40.78 mV/dec) due to the strong gate coupling, and it has good off-state leakage.

Table 2 lists the drain current of the device in eight switching states. Here, logic “1” and logic “0” indicate that the gate-source voltage is 1 V and 0 V, respectively. The drain current of the device is normalized accordingly and listed in the rightmost column of Table 2. From Table 2, the maximum turn-off current of the device is 8.21 \( \times 10^{-4} \mu \text{A} \), while the minimum turn-off current reaches 1.41 \( \mu \text{A} \). The Ti-TFET exhibits a worst-case switching ratio \( I_{on}/I_{off} \) of 1767.

3.3. Energy Band Distribution of the Channel Surfaces. As we can see from Table 2, the strong coupling between all the gates would increase the turn-on current of the device. In order to understand the mechanism of current multiplication caused by the coupling effect, we analyze the energy band distribution of the channel surface in different biasing conditions.

Figure 5 shows the energy band diagram and BTBT rate of the Ti-TFET along the top and bottom cut lines (shown in Figure 1(a)) in different switching states \( (V_{GS1}=0 \text{ V or } \)
As shown in Figure 1(a), the top cut line is located at 0.5 nm directly below the HfO2 layer under Gate 1 along the x-direction. The bottom cut line is in the same plane as the top cut line and located at 0.5 nm above the HfO2 layer. W1 and W2 are the minimum tunneling widths with the fixed $V_{GS1} = 1\,\text{V}$ and $V_{GS1} = 0\,\text{V}$, respectively.

For the energy band distribution on the surface of Channel 2, only $V_{GS1}$ and $V_{GS3}$ need to be considered. The four dashed curves in Figure 5(a) represent the conduction and valence energy band along the top cut line and bottom cut line, where $V_{GS1} = 0\,\text{V}$. We found that the energy value of the conduction band in the source region is still lower than that of the valence band in the channel region along the top cut line, and thus BTBT hardly ever occurs in the top region of Channel 2, and BTBT rate is approximately equal to zero.

As we can see from Figure 5(a), the enlarged view along the bottom cut line, the energy value of the conduction band decreases obviously along the bottom cut line, and the tunneling window is opened. Therefore, the BTBT occurs in the bottom region of Channel 2 in this biasing condition, the tunneling window is small, and the tunneling distance W2 is relatively large. The BTBT rate increases in the bottom region of Channel 2, but the value is still small so that the tunneling current is relatively small.

The energy band distribution curve along the top and bottom cut lines is shown as the solid lines shown in Figure 5(b) with the fixed $V_{GS1} = 1\,\text{V}$ and $V_{GS3} = 1\,\text{V}$. From Figure 5(b), as $V_{GS1}$ becomes 1 V, the coupling on the potential of Channel 2 is enhanced. In the top region of the channel near Gate 1, the curvature of the energy band at the interface between the source and channel increases obviously, and thus BTBT occurs accordingly. Due to the influence of $V_{GS1}$, the tunneling width W1 becomes smaller.
than W2 and the tunneling window is also larger. Therefore, the BTBT rate near the bottom region of the Channel 2 is greatly increased, which leads to a substantial increase in BTBT current in two paths, and thus the device is turned on.

4. Optimization

In this section, taking the turn-on current $I_{on}$ and switching current ratio $I_{on}/I_{off}$ as the optimization objective, the body thickness $T_{Si}$ and work function $\Phi$, which have the greatest impact on the device performance, are optimized.

The turn-on current $I_{on}$ and the switching current ratio $I_{on}/I_{off}$ for different body thickness $T_{Si}$ and work functions $\Phi$ are shown in Figure 6(a), and Figure 6(b) is 2D contour plots for better observation. IRDS2020 points out that the turn-on current of a transistor should be at least 1 $\mu$A even for low-power applications. Hence, the switching current ratio should also be more than three orders of magnitude. From Figure 6(b), in order to obtain a large switching current ratio and acceptable turn-on current, $T_{Si}$ could be selected from 5.0 nm to 5.5 nm and $\Phi$ from 4.05 eV to 4.10 eV.

4.1. Body Thickness $T_{Si}$. Figure 7 shows the sensitivities of the transfer characteristics $I_D-V_{GS}$ to the body thickness variations, where $V_{GS1}=1$ V and $V_{GS2}=0$ V. In Figure 7, $I_{on}$ is the turn-on current $I_{on}$ of the device, while $I_{100}$ is turn-off current $I_{off}$. It can be seen that the $I_{off}$ of the device shows a continuous decrease trend as $T_{Si}$ decreases from 9 nm to 5 nm, while an opposite trend can be observed for $I_{on}$. Therefore, the reduction in $T_{Si}$ is the most effective method to reduce the leakage current and increase the switching current ratio. It is important to notice that these trends of $I_{on}$ and $I_{on}/I_{off}$ for different work functions are almost the same, as shown in Figure 6.

This phenomenon could be well explained by using the energy band distribution and BTBT rate shown in Figure 8, where $T_{Si}=5$ nm and $T_{Si}=9$ nm. From Figure 8, the device with thin $T_{Si}$ would have small tunneling width and thus obtain the large BTBT rate. Therefore, we might draw the conclusion that $I_{on}$ of the device increases with the decrease of the body thickness and thus the better performance.

4.2. Work Function $\Phi$. The relationship between the current characteristics and work function $\Phi$ is shown in Figure 9(a), where $V_{GS1}=1$ V, $V_{GS2}=0$ V. It can be seen both turn-on current and turn-off current of the device decrease as the work function is increased.

The curve in black in Figure 9(b) represents the turn-on current $I_{on}$ of the device with different work functions. We find that $I_{on}$ shows an exponentially increased trend with the decrease of $\Phi$. The curve in red shown in Figure 9(b) shows the switching current ratio $I_{on}/I_{off}$ as a function of $\Phi$. We find that the ratio of $I_{on}/I_{off}$ decreases rapidly as $\Phi$ varies from 4.2 eV to 3.8 eV. From Figure 9(b), we also find that $I_{on}/I_{off}$ decreases rapidly as $\Phi$ decreases from 4.1 eV to 3.8 eV.

This phenomenon could be well explained by using the energy band distribution and BTBT rate with different work functions ($\Phi$ varies from 3.8 eV to 4.2 eV) in the turn-off state, as shown in Figure 10. When $\Phi > 4.2$ eV, the conduction band energy of the channel region was still higher.
than the valence band energy of the source region. Thus, the BTBT does not occur, so that device is not yet turned on, and the turn-off current \( I_{100} \) of the device is very small.

Therefore, when \( \Phi > 4.2 \text{ eV} \), \( I_{100}/I_{100} \) decreases rapidly because of rapidly decreased \( I_{100} \).

When \( \Phi \) decreases to 4.1 eV, the tunneling window is turned on nearly, and BTBT rate begins to occur also, as shown in Figure 10, so that the turn-off current \( I_{100} \) increases quickly, but the BTBT rate is not large enough. As \( \Phi \) continues to decrease, the tunneling window is fully open, so that the leakage current \( I_{100} \) increases rapidly. Therefore, when \( \Phi \) decreases from 4.1 eV to 3.8 eV, \( I_{100}/I_{100} \) decreases rapidly because of rapidly increased \( I_{100} \) rather than \( I_{100} \).

From the above analysis, we can see that the device with \( \Phi = 4.1 \text{ eV} \) is at a near turn-on state when \( V_{GS1} = 1 \text{ V} \), \( V_{GS2} = V_{GS3} = 0 \text{ V} \). In this case, once a small biasing voltage is applied to Gate 3 or Gate 2, the tunneling current would increase rapidly, so that the proposed Ti-TEFT would be

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**Table 2**: The turn-on and turn-off currents of the N-type Ti-TFET device.

| Switching state   | \( V_{GS1} \), \( V_{GS2} \), \( V_{GS3} \) (V) | \( I_D \) (\( \mu \text{A}/\mu \text{m} \)) | Normalized \( I_D \) |
|-------------------|-----------------------------------------------|----------------------------------------|---------------------|
| Turn-off State 1  | 0, 0, 0                                      | 1.81E-10                                | 0.4E-08             |
| Turn-off State 2  | 0, 0, 1                                      | 1.98E-04                                | 0.5E-04             |
| Turn-off State 3  | 0, 1, 0                                      | 2.58E-04                                | 0.6E-04             |
| Turn-off State 4  | 1, 0, 0                                      | 8.21E-04                                | 1.9E-04             |
| Turn-on State 1   | 1, 1, 0                                      | 1.45                                   | 0.3428              |
| Turn-on State 2   | 1, 0, 1                                      | 1.45                                   | 0.3428              |
| Turn-on State 3   | 0, 1, 1                                      | 1.41                                   | 0.3311              |
| Turn-on State 4   | 1, 1, 1                                      | 4.28                                   | 1.0000              |
Figure 5: $V_{GS3} = 1\ V$ and $V_{GS2} = 0\ V$, energy band distribution and BTBT rate along top and bottom cut lines shown in Figure 1(a) in different switching states, (a) $V_{GS1} = 0\ V$ and (b) $V_{GS1} = 1\ V$, the inset is an enlarged view of the energy band distribution at the interface between source and channel.

Figure 6: (a) Turn-on current $I_{on}$ and switching current ratio $I_{on}/I_{off}$ with different body thickness and work functions and their (b) 2D contour plots.
turned on when two or more input terminals are biased with high level.

5. Logic Cells

The “Majority-Not” circuit is a fundamental logic cell that can be widely used to implement efficiently complex logic circuits. The truth table of the three-input “Majority-Not” is shown in Figure 11(a). The traditional “Majority-Not” cell using static complementary CMOS logic is shown in Figure 11(b). Another realization of the “Majority-Not” cell using a reconfigurable logic function with NAND and NOR along with a MUX is shown in Figure 11(c). Since a single N-type Ti-TFET exhibits the three-input “Majority-Not” switching behavior, only one N-type and one P-type Ti-TFET can be used to compactly implement the “Majority-Not” logic cells, as shown in Figure 11(d). Compared with the two traditional 10-T “Majority-Not” logic cells, the “Majority-Not” logic cell using Ti-TFETs can effectively reduce the number of transistors and stack height.

The power consumption and power delay product of the static complementary Majority-Not cell using 7 nm FinFETs [25], 20 nm AlGaSb/InAs single-gate TFETs [26] Ti-TFETs are compared in Table 3. The power consumption and power delay product of the Majority-Not logic gate based on Ti-TFETs can effectively reduce the number of transistors and stack height.

![Figure 7: The $I_D-V_{GS3}$ characteristics of the Ti-TFET with different body thicknesses ($T_{Si} = 5, 6, 7, 8, \text{and } 9 \text{ nm}$) in $V_{GS1} = 1 \text{ V}$ and $V_{GS2} = 0 \text{ V}.$](image)

![Figure 8: Energy band distribution at the top cut line with $T_{Si} = 5 \text{ nm}$ and $T_{Si} = 9 \text{ nm}$ ($V_{GS1} = 1 \text{ V}$, $V_{GS2} = 0 \text{ V}$, $V_{GS3} = 1 \text{ V}$.)](image)
Figure 9: (a) $I_D$-$V_{GS3}$ characteristics of the Ti-TFET with different work functions ($\Phi = 3.8 \text{ eV}, 3.9 \text{ eV}, 4.0 \text{ eV}, 4.1 \text{ eV}, 4.2 \text{ eV}, 4.3 \text{ eV}$), and (b) turn-on current and $I_{on}/I_{off}$ with different work functions.

Figure 10: The energy band distribution and BTBT rate of the Ti-TFET with different work functions ($\Phi$ varies from 3.8 eV to 4.2 eV) in a turn-off state.
gate TFET, and 1.1 nW for the Ti-TFET. Therefore, reduced power is due to both TFET operation and the multigate transistor architecture.

6. Conclusion

This paper has proposed a new type of TFET with tri-input terminals, and the objective of this paper is to demonstrate a technique to expand the logic function in a single transistor and reduce transistor count in circuits. The proposed Ti-TFET has been optimized by selecting the channel structure, body thickness, and work function. We also highlight the fabrication guidelines for Ti-TFETs. The special T-channel structure enhances the channel coupling of any two gates, and thus drain current can exponentially increase. Since the Ti-TFET exhibits the three-input Majority-like switching behavior, the proposed devices can provide a new perspective for further application of different types of TFETs to realize the compact logic circuits.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Disclosure

An earlier version of this paper was presented at the 20th IEEE Conference on Nanotechnology with 4 pages [20]. Now, the authors significantly expand the previous conference version to contain substantial new technical material, and the content has also expanded by more than 70%.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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Table 3: The power consumption and power delay product of static complementary Majority-Not cell using FinFETs, single gate TFETs, and Ti-TFETs.

| Devices                | Power consumption (nW) | PDP ($10^{-18}$) |
|------------------------|------------------------|-----------------|
| 7nm FinFETs            | 60.13                  | 17.22           |
| 20nm AlGaSb/InAs TFETs | 49.15                  | 19.85           |
| Ti-TFETs               | 2.25                   | 4.22            |

Figure 11: Majority-Not logic cell. (a) Truth table, (b) the traditional “Majority-Not” cell using static complementary CMOS logic, (c) a realization using NAND, NOR, and MUX with a select signal $S$, and (d) the logic cell using Ti-TFETs.
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