Work Function Adjustment by Using Dipole Engineering for TaN-Al$_2$O$_3$-Si$_3$N$_4$-HfSiO$_x$-Silicon Nonvolatile Memory

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Abstract: This paper presents a novel TaN-Al$_2$O$_3$-HfSiO$_x$-SiO$_2$-silicon (TAHOS) nonvolatile memory (NVM) design with dipole engineering at the HfSiO$_x$/SiO$_2$ interface. The threshold voltage shift achieved by using dipole engineering could enable work function adjustment for NVM devices. The dipole layer at the tunnel oxide–charge storage layer interface increases the programming speed and provides satisfactory retention. This NVM device has a high program/erase (P/E) speed; a 2-V memory window can be achieved by applying 16 V for 10 $\mu$s. Regarding high-temperature retention characteristics, 62% of the initial memory window was maintained after $10^3$ P/E-cycle stress in a 10-year simulation. This paper discusses the performance improvement enabled by using dipole layer engineering in the TAHOS NVM.

Keywords: TaN-Al$_2$O$_3$-HfSiO$_x$-SiO$_2$-Silicon (TAHOS); nonvolatile memory (NVM); dipole engineering; work function

1. Introduction

Nonvolatile memory (NVM), because of its high density and low cost, is widely used for portable mass storage purposes in digital cameras, tablet PCs, and smartphones [1]. A crucial challenge in the electronics industry is obtaining low-power fast NVM devices with small dimensions. A silicon-oxide-nitride-oxide-silicon (SONOS)-like structure has become widely used for charging
devices because it does not have a planar scaling problem for floating gate isolation and exhibits considerable potential for achieving high program/erase (P/E) speeds, low programming voltages, and low power performance [1–7].

Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) flash memory devices are potential candidates for replacing conventional floating-gate NAND (Not AND) flash devices in the sub-32 nm technology node [6,7]. SONOS-like devices have several advantages over the conventional floating-gate device, such as rapid programming, low-power operation, high-density integration, and excellent reliability.

According to studies on SONOS flash, TaN-Al2O3-Si3N4-SiO2-silicon (TANOS) structure flash memory [8–10] exhibits excellent performance because of its immunity to gate injection when metal gate TaN with a high work function is used. Moreover, several studies have presented various types of high-k dielectric trapping layers as potential candidates for replacing Si3N4 to provide discrete NVM charge storage [11–16]. Furthermore, high-k dielectric materials can improve the gate capacitance, and maintain an equivalent potential difference for a greater thickness compared with SiO2. Therefore, the leakage through the dielectric can be minimized, and the scaling limits can be extended. Moreover, to achieve a large memory window for differentiating between stable programs and erased states, a high-k dielectric trapping layer can provide sufficiently high trapping density for charge storage [17]. According to the International Technology Roadmap for Semiconductors, high-k trapping layer use in flash memory has high potential for scalability below the 32-nm node [18].

Metal gate electrodes with high-k dielectric oxide may be made more effective than poly-Si by improving the carrier mobility, thus avoiding the poly-Si depletion effect and dopant penetration through the gate oxide [19–22]. However, using a metal gate layer requires n- and p-type metals with appropriate work functions for targeting the suitable threshold voltage (Vth) for high-performance complementary metal-oxide-semiconductor (CMOS) logic applications on bulk Si [23,24]. In addition, studies have demonstrated Vth shift caused by dipole formation at high-k/SiO2 interfaces [25–27]. The areal density difference of oxygen atoms is the driving force in dipole formation at these interfaces [28,29]. In this study, we used the dipole engineering for NVM to modulate Vth with different high-k dielectric layers. The proposed design with adjustable Vth exhibited excellent characteristics such as a considerably large memory window, high-speed P/E, excellent endurance, and optimal disturbance.

2. Experimental Section

Figure 1 illustrates the structure of our TAHOS SONOS-like NVMs. These devices were fabricated on 6 inch Si wafers. After the active region was patterned, a 4 nm oxide tunnel was thermally grown at 1000 °C in a vertical furnace system. Next, 1 nm HfO2 and Al2O3 thin films, used in the dipole layer, were deposited using metal–organic chemical vapor deposition (MOCVD). We compared three samples: one without a dipole layer, one with a 1 nm HfO2 dipole layer, and one with a 1 nm Al2O3 dipole layer. Table 1 compares the devices. After a 10 nm trapping HfSiOx deposition, MOCVD was used to deposit a 10 nm Al2O3 thin film, which was used as a blocking oxide. Next, a 100 nm TaN layer was deposited using a sputtering method. After gate patterning, a self-aligned implantation was used to create an n+ source/drain with As+ at a dose of 5 × 1015 cm−2 and energy of 15 keV. Dopant activation and the interaction of the dipole layer with tunnel oxide were accomplished through rapid thermal annealing (RTA) at 950 °C for
15 s. The remainder of the subsequent standard CMOS procedures were completed for fabricating the TAHOS SONOS-like NVM devices.

3. Results and Discussion

Figure 2 plots the Id-Vg curve of the proposed TAHOS NVM devices. The drain voltage (V_d) of the Id-Vg curve is 0.1 V, and V_g transverses from 0 to 5 V. The V_th at 10^-7 A I_d is 1.68, 2.11, and 1.82 V for the without dipole, Al_2O_3 dipole, and HfO_2 dipole samples, respectively. Al_2O_3/HfO_2 dipole layer incorporation in the TAHOS stacks results in a positive V_th shift in the NVM devices. The V_th tuning was found to be proportional to the net dipole moment associated with the Hf-O/Si-O and Al-O/Si-O bonds at the high-k/SiO_2 interface because of electronegativity and areal density difference of oxygen atoms [28,29]. According to the electrical measurement results, the dipole effects caused by the interfacial Al_2O_3 and HfO_2 dipole layer shift the effective work function toward p-metal. Therefore, different dipole layers can be used for V_th adjustment for tuning the conventional gate electrode work function.

X-ray photoelectron spectroscopy (XPS) was performed by using an Al Kα X-ray source (1486.6-eV photons) to determine the bonding environments of the Hf atoms. Figure 3 shows the Hf 4f photoemission peaks of the samples without dipole, with Al_2O_3 dipole, and with HfO_2 dipole. The test sample for XPS was prepared for the without dipole or with Al_2O_3 dipole layer following preparation of the HfSiO_x thin film after RTA at 950 °C for 15 s. In the without dipole sample, we observed well-defined 4f_{5/2} and 4f_{7/2} feature peaks for the HfSiO_x thin film that correspond to Hf–O–Si bonding. For the HfO_2 dipole sample, these peaks shifted to lower binding energies (4f_{5/2}: ca. 17.7 eV; 4f_{7/2}: ca. 16.2 eV), resulting in HfO_2 dipole formation after RTA [30]. Moreover, for the Al_2O_3 dipole sample, these peaks shifted to higher binding energies (4f_{5/2}: ca. 18.7 eV; 4f_{7/2}: ca. 17.2 eV), resulting in Al_2O_3
dipole formation after RTA [31]. The XPS results provide definite evidence of HfO$_2$ and Al$_2$O$_3$ dipole formation through dipole engineering.

**Figure 2.** $I_d$–$V_g$ curve of the TAHOS NVM devices.

**Figure 3.** Hf 4f XPS spectra of the samples without dipole, with Al$_2$O$_3$ dipole, and with HfO$_2$ dipole.

Figure 4a,b presents the P/E characteristics of various pulse widths for different operation conditions. The P/E operations were performed using Fowler–Nordheim tunneling at $V_g = 16$ V and $V_g = -15$ V with $V_d = V_s = 0$ V. The $V_{th}$ shift is defined as the threshold voltage change of a device between the written and the erased states. $\Delta V_{th}$ increased with the P/E pulse time and bias, and the memory window was >1.5 V. In conventional flash memory, >0.8 V memory window is sufficient for judge the “1” or “0” state, the $V_{th}$ window of the device between program/erase state is enough for flash memory operation. No erase saturation effect occurred even at high erase bias or over a long erase time because of TaN’s high work function (4.7 eV), which prevents the injection of electrons from the gate [10].

Regarding the dipole splits, the Al$_2$O$_3$ and HfO$_2$ dipole samples have higher programming speeds than does the without dipole sample because of the low barrier height for electron tunneling. The Al$_2$O$_3$ or HfO$_2$ dipole samples have slightly lower erasing speeds because of the increasing thickness of gate oxide.
Figure 4. (a) Program characteristics of the TAHOS NVM devices; (b) Erase characteristics of the TAHOS NVM devices.

Figure 5 plots the endurance characteristic of the proposed TAHOS NVM devices. To achieve approximately the same memory window, we used the following P/E conditions: $V_g = 16 \text{ V}$, 1 us/$V_g = -15 \text{ V}$, and 0.1 s for the without dipole sample; $V_g = 16 \text{ V}$, 1 us/$V_g = 16 \text{ V}$, and 0.1 s for the Al$_2$O$_3$ dipole sample; and $V_g = 16 \text{ V}$, 1 us/$V_g = -16 \text{ V}$, and 0.1 s for the HfO$_2$ dipole sample. The NVM device displayed more favorable endurance, retaining 75% of its initial memory window after $10^3$ P/E cycles. For the endurance characteristics, higher erasing $V_t$ after cycling is the reliability issue in the conventional flash memory for thick tunnel oxide degradation [2,6,8]. This result is because the degradation of the tunnel oxide (SiO$_2$) in TAHOS NVM devices mainly depends on the electrical field. In addition, the endurance curves increase slightly as the number of P/E cycles increase, because of the formation of operation-induced trapped electrons. This is intimately related to the use of thick tunnel oxide and presence of minute residual charges in the SiO$_2$ after cycling.

Figure 5. Endurance characteristics of the TAHOS NVM devices.

Figure 6 illustrates the retention characteristics with $10^3$ P/E cycled stress condition of the proposed TAHOS NVM at a high temperature ($T = 85$ °C). The retention time was up to $10^8$ s for 38%, 48%, and
72% charge losses for the Al₂O₃ dipole, HfO₂ dipole, and without dipole samples, respectively. The retention of both of the dipole samples was superior to that of the without dipole sample because of the formation of a thick tunnel oxide. Moreover, the Al₂O₃ dipole sample exhibited superior retention to that of the HfO₂ dipole sample because the Al₂O₃ layer has a greater electron barrier height [31].

![Figure 6. Retention characteristics of the TAHOS NVM devices.](image)

4. Conclusions

TAHOS NVM was fabricated using an Al₂O₃/HfO₂ dipole layer at an HfSiOₓ/SiO₂ interface, demonstrating a Vₜh shift and providing work function adjustment. A 2-V memory window was achieved by applying 15 V for only 10 μs. Regarding endurance, a 1-V of memory window was maintained after 10³ P/E stress cycles. Regarding retention, 62% of the initial memory window was maintained after a 10-year simulation at high temperature (T = 85 °C). Thus, dipole engineering has great potential for work function adjustment in conventional SONOS-type NVM.

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Author Contributions

Yu-Hsien Lin organized the research and wrote the manuscript; Yi-Yun Yang performed the experiments and performed data analysis; Yu-Hsien Lin and Yi-Yun Yang discussed the experiments and the manuscript.
Conflicts of Interest

The authors declare no conflict of interest.

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