Photoresist Challenges for Logic and Memory using 0.33NA EUV Lithography

Danilo De Simone* and Geert Vandenberghe
IMEC, Kapeldreef 75, 3001 Leuven, Belgium
*danilo.desimone@imec.be

With the scaling evolution of logic and memory technologies the extreme ultraviolet lithography (EUVL) technology is becoming part of the high-volume manufacturing device landscape. Currently, the single patterning of both logic metal layer and DRAM storage layer are approaching the resolution limit on the 0.33NA full field exposure scanner. Furthermore, because the logic technology nodes are scaling at a faster pace than memory nodes, the development of leading-edge logic node (N5) will move first the EUVL insertion from a single patterning to a double patterning technology with relaxed pitches to overcome the current 0.33NA EUVL limits. In this paper, the EUV photoresist challenges are discussed on the horizon of up-coming industry technology nodes.

Keywords: EUV, EUVL, Photoresist, Logic, Memory

1. Introduction

The continuous efforts on the development of extreme ultraviolet (EUV) lithography have allowed to push the lithographic performance of the EUV photoresists close to the imaging limits of the ASML NXE 0.33NA full field exposure scanner. On the other hand, the scaling of both logic and DRAM technologies are bringing the development of logic metal and DRAM storage layers close to the resolution limit on the exposure tool. The development of leading-edge logic node (N5) will therefore soon move from a single EUVL patterning to a double patterning approach with relaxed pitches. In such a way the scaling evolution of logic and memory technologies is embracing the EUVL technology and it is becoming more and more part of the high-volume manufacturing (HVM) device landscape. Representative critical layer roadmap of current industry technology nodes and EUV lithography capability roadmap are reported in Fig. 1.

Although EUVL is nowadays part of the HVM roadmap, in order to reduce the total cost of ownership, increase the yield and reduce the time to ramp, the HVM requires to have a cost-effective low exposure dose photoresist (20-35 mJ/cm² exposure dose range) and excellent control on process stability and defectivity. Today the low exposure dose regime in EUV remains a big challenge and pattern defectivity at nano-scale is the major limiting factor of the lithographic process window of EUV resist when looking at tight pitches close to the resolution limit of the exposure tool [1]. Recent studies on pitch 32nm dense line space patterning and pitch 36nm dense orthogonal contact hole patterning have shown pattern defectivity as nano-bridges and broken-lines, and merging or closing, respectively [2,3]. A new way of characterizing and benchmarking the EUV resists has been introduced to be effective at the early characterization stage to quantify the resist roughness and the nano-failures [4-6] induced by a stochastic EUV patterning regime, the random nature of the light-matter interaction and consequent chemical reactions.

In this paper, the EUV photoresist challenges are
discussed on the horizon of up-coming industry technology nodes. Two use-cases are considered for the EUV single patterning: (i) a logic metal pattern at 32nm dense line-space, (ii) a DRAM storage staggered pillars at 40nm pitch. In both cases the new metric to count pattern failures have been applied on a series of EUV resists after development. Furthermore, a third user case for EUV double patterning is introduced with focus on 42nm dense line-space after development (21nm pitch in pitch doubling technology). The experimental setup and the results of such an exploration are described and discussed in the next paragraphs.

2. Experimental

The EUV resist evaluation was carried out by printing the desired pattern with a mask with dark tonality. A 300 mm TEL clean track Lithius ProZ™ interfaced with the ASML NXE3300B full field EUV scanner was used. Dedicated illumination modes were used depending on the patterning feature to target. Stacked wafers with a hard-mask underneath the resist were used to enable pattern transfer process after the lithographic patterning. The optimum exposure dose and focus offset was picked up for each pattern from a focus-exposure matrix. Hitachi CG6300 scanning electron microscope (CD-SEM) was used to collect top-down images to measure critical dimension (CD) of lines and CD and local CD-uniformity (LCDU) for pillars. Line roughness (LWR and LER) was measured through CD-SEM (biased roughness values) and the commercial computational metrology software Fractilia (unbiased roughness values). SEM images from CD-SEM and KLA eDR7380 tool were collected to analyze them and quantify the nano-failures on the inspected patterned areas. Stochastic nano-failures were quantified using IMEC in house software Stochalis and KOLAONA [1,6].

3. Results and discussion

3.1. Single patterning, metal layer Logic case (pitch 32nm dense LS)

A large EUV photoresist screening activity has been carried out at imec aiming to assess the lithographic performance of EUV resists on 32nm dense line space. 469 wafers were exposed aiming to satisfy the provided requirements (Fig. 2). The patterning result of the best sample per supplier is reported in Fig. 3. One resist sample required a very high dose (110 mJ/cm²) while the other five samples worked in the exposure dose regime between 42 mJ/cm² and 57 mJ/cm². These resists were further analyzed to quantify the failure free latitude (FFL) [7] by using the ‘pixel-not-ok’ metric [1,4] at the best focus offset with an upper limit spec of 2E10-6. The results are reported in Fig. 4. In such a case, each resist showed different FFL and the largest FFL was delivered by R4 resist. Considering the total inspected area per CD is equivalent to 268 μm², the overall FFL is quite small (< 4 nm) for all tested resists suggesting that further improvements are needed to suppress the nano-bridges and broken line failures and increase the process window area.

| Key parameters                | targets                        |
|------------------------------|--------------------------------|
| Dose-to-line                 | 20 ≤ DR ≤ 90 mJ/cm²            |
| CD tg and spec               | Line CD in the range 15nm and 17nm with a CD spec of ±10% |
| Resist Film Thickness        | ≤ 40 nm                        |
| Nano-failures                | <2E-6 pixel NOK (100 images)   |
| LWR/LER                     | 3.0nm (unbiased-LWR), 2nm (unbiased-LER) |

Fig. 2. Key EUV resist requirements for pitch 32nm dense line-space pattern.

![Fig. 2](image2.png)

Fig. 3. Pitch 32nm dense line-space EUV pattern. Summary results, best resist per supplier. Resists from R1 to R5 have the exposure dose in spec. (< 60 mJ/cm²).

![Fig. 3](image3.png)

Fig. 4. Pitch 32nm dense line-space EUV pattern. Failure Free Latitude (FFL), best sample per supplier. R4 shows the larger FFL (~4 nm). Overall the FFL is small (≤ 4 nm) considering that the limited total inspected area per CD equivalent to 268 μm².

![Fig. 4](image4.png)
The same SEM image collection used for the nano-failure quantification at the best exposure conditions were used to quantify the roughness (LER and LWR) for the 6 best resists. The power spectra analysis (PSD) was carried out and the PSD trends as function of different frequency domains are reported in Fig. 5. From the PSD analysis the unbiased values for the roughness were calculated. The score card per best EUV resist sample is reported in Table 1 grouping both FFL value and PSD analysis outputs performed on the 32nm dense line-space pattern. R4 resist was confirmed to deliver the best overall performance with an unbiased LER and LWR of 1.5 nm and 1.89 nm, respectively.

Table 1. Pitch 32nm dense line-space EUV pattern. Score card per EUV resist. R4 resist shows the best lithographic performance.

| Dose [mJ/cm²] | Failure Free Latitude [nm] | LWR unbiased [nm] | LER unbiased [nm] | PSD(0) LWR [mm²] | PSD(0) LER [mm²] |
|---------------|-----------------------------|-------------------|-------------------|------------------|------------------|
| R1            | 42                          | 1.4               | 1.94              | 6.17             | 9.22             |
| R2            | 52                          | 1.5               | 1.75              | 12.40            | 9.08             |
| R3            | 53.6                        | 1.9               | 1.78              | 12.97            | 9.01             |
| R4            | 54.6                        | 1.7               | 1.50              | 6.17             | 6.39             |
| R5            | 47.75                       | 2.8               | 1.73              | 14.98            | 9.77             |
| R6            | 126                         | 2.11              | 1.56              | 8.72             | 8.22             |

The MOR pillars after development show a jagged shape with a tendency to form spikes around the pillar perimeter. To avoid an overestimated count of the nano-failures after development, the pillars were transferred to a silicon oxide/titanium nitride layer to improve the pillar shape eliminating the tiny MOR spikes. The impact of the pillar shape by the etch process is shown in Fig. 8. The MOR was then analyzed to quantify the failure free latitude (FFL) [7] by counting the pillars affected by defectivity. The total inspected area per CD after etching (AEI-CD) was equivalent to 48 mm². Across the AEI-CD range of 22-30 nm nano-bridge failures only were detected. No missing pillars were detected. The FFL was quantified as ~2.5 nm at the best focus exposure. The results of the defectivity count as function of the AEI-CD are reported in Fig. 9. The results indicate that further studies are needed to understand the mechanism that leads to the formation of the nano-bridge especially in the AEI-CDs on the left of the FFL.
3.3. Double patterning, metal layer Logic case (pitch 21nm dense LS)

The advances in the development of the N5 logic metal layer would lead the metal pitch below 30 nm. This year the EUV resist benchmarking at imec is started to explore the EUV resist performance for the initial lithographic pitch of 42nm dense line space to equivalent to the final 21nm pitch after a double patterning process flow (Fig. 10). The lithographic requirements of such a patterning are reported in Fig. 11.

The first results of such a EUV resist benchmarking are reported in Fig. 12. The activity is currently on going at imec and further progress are expected to be reached. These preliminary results are indicating that 40 mJ/cm² is reachable by most of the resist suppliers. Further studies will be addressed to quantify the roughness and the failure count after the first pattern transfer of the double patterning flow.

Fig. 11. Key EUV resist requirements for 42nm dense line-space pattern.

Fig. 12. Pitch 42nm dense line-space EUV pattern. Summary results, best resist per supplier. All resists, except T1 resist, work in the dose regime between 28 mJ/cm² and 42 mJ/cm². The roughness of the line (LWR and LER) are expected to become better after unbiased the values.

4. Conclusion

In this work we have reported on the state-of-the-art for the EUV resists when pushing their resolution on the ASML 0.33NA full field EUV scanner looking at three specific EUV layers of the up-coming industry technology nodes for both logic and memory devices (metal and storage layer cases, respectively). The performance of the EUV resists were assessed by looking at the RLS performance and the nano-failure count on pattern.

The best advanced EUV resists provided by six different material suppliers were analyzed by looking at 32nm dense line-space pattern for single EUV patterning and 42nm dense line-space pattern for the EUV double patterning (equivalent to 21nm final pitch). The results show that best performance on 32nm pitch are obtained with an exposure dose of ~60 mJ/cm² while the pitch 42nm is feasible at the exposure dose of ~40 mJ/cm². The unbiased roughness for a 16nm dense line is 1.89 nm (LWR) and 1.5 nm (LER). Furthermore, the results show that the MOR is capable to print 40 nm staggered
pillars with outstanding printability compared to chemically amplified resists with a LCDU of 2.6 nm at the exposure dose of ~60 mJ/cm². The characterization of the EUV resists from a defectivity standpoint lead to the conclusion that the performance of all materials (CARs and non-CARs) are limited in performance by the nano-failures at the exposure dose of ~60 mJ/cm² when pushing the imaging limits of the 0.33NA exposure scanner.

Further efforts are needed to develop novel EUV resists to deliver high resolution, high sensitivity and clean patterning capable to enable the scaling of novel logic and DRAM devices using 0.33NA EUV single patterning. Further studies are in progress to assess the resist roughness and failures for a double patterning process in EUVL.

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