Medium Frequency Physical Vapor Deposited Al2O3 and SiO2 as Etch-Stop-Layers for Amorphous Indium-Gallium-Zinc-Oxide Thin-Film-Transistors

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Amorphous oxide semiconductors (AOSs) are gaining traction to replace the a:Si:H in TFTs applied in liquid crystal display (LCD) and organic light-emitting diode display (OLED) backplanes. These oxide semiconductors have high transparency and relatively high electron mobility in the amorphous state. An additional advantage lies in the low process temperature required for AOS integration on plastic film and so potentially enabling flexible transparent display and electronics. Among many AOSs, a-IGZO is the most promising due to its high mobility, excellent uniformity, and the compatibility with transparent and flexible substrate, as compared to conventional amorphous and polycrystalline silicon. For either LCD or OLED displays with IGZO backplane, bottom-gate top-contact (BGTC) ESL configuration is preferred. The ESL protects the a-IGZO back channel from damages caused during the source-drain metallization and patterning. The damage-free surface improves the bias stabilities especially at accelerated bias stress conditions under illumination. However commonly the ESL is deposited by plasma assisted CVD processes to which a-IGZO can be sensitive. Therefore there is a need to investigate the effect of the ESL on the characteristics of a-IGZO TFTs.

PECVD based SiO2 deposited at temperature higher than 350°C using SiH4/N2O chemistry is commonly used as an ESL in Flat-Panel-Display (FPD) industry due to its low deposition rate, high uniformity and good step coverage. For the integration on commercialized flexible substrates like PEN or polyimide, deposition and process temperature should be lower to prevent shrinkage of the plastic foil and allow easy de-lamination. It is known that PECVD ESL based TFTs suffer from degradation caused by hydrogen which is problematic for a-IGZO TFTs because it leads to uncontrolled doping density. Few research groups have demonstrated the use of PVD based dielectrics (SiO2 and Al2O3) as passivation layer or ESL as an alternative to PECVD ESL layer which has the doping issue with a-IGZO. Despite the fact that PVD dielectrics intrinsically contain less hydrogen, parameters such as deposition rates, uniformity, defect density and electrical properties like leakage current and breakdown voltage are often insufficient to meet the manufacturing requirements of the industry. Recently mf-PVD Al2O3 layers have been demonstrated with high deposition rate and sufficient uniformity up to Gen-8 size. This might allow to replace the conventional PECVD SiO2 layer to achieve better TFT characteristics. In this paper, we realized IGZO-TFTs with different mf-PVD ESL (SiO2 and Al2O3) and compared them to conventional PECVD SiO2 ESL based TFTs.

Experimental

All TFT were made on conducting silicon substrate with thermal SiO2 (120 nm) as gate dielectric and the Si substrate was used as a common gate electrode. The use of high-quality high-temperature thermal SiO2 guarantees that none of the observed bias instabilities is related to the gate dielectric (GD) layer. In the first step, a-IGZO layer was deposited by dc sputtering at room temperature (RT) using a-Ar mixture. In the next step the ESL/a-IGZO stack was patterned by dry etch and wet etch followed by contact opening by dry etch. The Mo S/D contacts were formed by molybdenum (Mo) sputtering and wet etch. All layers were patterned by standard photolithography. In the last step all the samples were subjected to thermal annealing at 250°C in N2 ambient for 1 hr. The electrical properties of a-IGZO TFTs were measured using an Agilent 4156 parameter analyzer in N2 environment. The characteristics of the ESL were measured by the ellipsometry and electrical characterization techniques. Relative layer density was characterized with standard BHF (1:50 with H2O) wet etch rate and hydrogen content was characterized by Elastic-Recoil-Detection (ERD) technique.

Results and Discussion

The use of high quality thermally grown SiO2 as gate-dielectric assures that any variations in TFT characteristics and the bias-stress stabilities are most likely related to the ESL. Fig. 1 shows a schematic cross-section of the a-IGZO TFTs. Fig. 2(a) and 2(b) shows typical transfer (IDS – VDS) and output (IDS – VDS) characteristics of three TFTs. As listed in Table I, for TFTs with mf-PVD ESLs the characteristics such as μFE, SS–1 and ION/OFF ratio are between 1.5–17 cm2/Vs, 0.20–0.30 V/decade and < 10 respectively. TFT with PECVD SiO2 ESL in comparison has a substantially lower μFE of 10–12 cm2/Vs, while the other parameters are comparable to the TFT with mf-PVD ESL.

In case of the PECVD based ESL, the impact of the deposition temperature on the TFT characteristics cannot be completely decoupled.
between the change in SiO₂ quality and the impact of the temperature on the a-IGZO. The low deposition temperature (<250 °C) of PECVD SiO₂ ESLs lead to increase in hydrogen content, decrease in the density and corresponding poorer electrical performance. Several research groups have reported that hydrogen atoms produced by SiH₄ plasma diffuse fast in the a-IGZO layer, creating a shallow electron donor level. On the other hand, oxygen atoms in N₂O plasma were inclined to oxidize the a-IGZO layer surface, which decreased the carrier concentration of a-IGZO layers. An optimized H₂ and O₂ plasma ratio layer can lead to improved transistor characteristics. In case of mf-PVD layers, optimized sputter plasma (O₂ to Ar ratio) tends to cause less impact on the a-IGZO below. In this case, because no hydrogen source is present, changes in TFT characteristics related to hydrogen doping can be ruled out with exemption to the PECVD SiO₂. The Ar rich plasma can change the a-IGZO layer from semiconducting to conducting by changing the ratio of metal atoms (Ga, In and Zn) and the O₂ rich plasma can cause the surface oxidation leading to more resistive layer and therefore both can influence the TFT characteristics. In fact it is reported that the Ar plasma treated surface has relatively higher In and relatively lower Ga and Zn due to the difference of the sputtering yield of these atoms. However, these differences are reduced after an annealing step. In case of TFT with mf-PVD ESLs, high mobility and negative VTH could be due to the change in the conductivity of the channel at the ESL interface. It could also be possible that the longer or higher temperature anneal conditions are required for mf-PVD ESL based TFTs to have similar properties like PECVD ESL based TFT. In further TFT characterizations, the bias-stress stabilities in dark conditions as shown in Fig. 3 under positive bias-stress (PBS) and negative bias-stress (NBS) have been characterized. The properties of the individual ESLs are listed in Table II. It is clearly understood that PECVD SiO₂ layer’s based TFTs are poor in characteristics as the layers properties such as density and dielectric constant are far off compared to ideal layer characteristics.

![Figure 1. Cross-section of ESL configuration based a-IGZO TFTs.](image)

**Table I. Comparison of TFT parameters for the three different types of ESLs.**

| TFT Parameters | ESL RT mf-PVD SiO₂ | ESL RT mf-PVD Al₂O₃ | ESL 200 °C PECVD SiO₂ |
|----------------|--------------------|---------------------|---------------------|
| μFE Range (cm²/V·s) | 15–17 | 15–17 | 10–12 |
| SS⁻¹ Range (V/dec) | 0.2–0.3 | 0.2–0.3 | 0.2–0.3 |
| VON Range (V) | -0.5–3.0 | -0.5–4.0 | -(0.1–2.5) |
| Hysteresis (V) | <0.1 | <0.1 | <0.1 |
| IBFFa (pA) | <1.0 | <1.0 | <1.0 |
| NBS & PBS (V) | <1.0 | <1.0 | ≥1.5 |
| NBSIS (V) | <2.0 | <2.0 | >6.0 |

![Figure 2. (a) Transfer (VGS-IDS) and (b) output (VDS-IDS) characteristics of TFTs with mf-PVD SiO₂, mf-PVD Al₂O₃ and PECVD SiO₂ ESL’s with W/L = 60/20 μm/μm.](image)
Figure 3. Transfer characteristics (VGS-ID) of a-IGZO TFT (W/L = 60/20 µm/µm) as function of duration time at 1MV/cm field in positive and negative gate bias stress direction for TFT with (a) mf-PVD SiO2, (b) mf-PVD Al2O3 and (c) PECVD SiO2. (d) VTH shift of all a-IGZO TFTs as a function of stress time.

Figure 4. Transfer characteristics (VGS-ID) of a-IGZO TFT (W/L = 60/20 µm/µm) as function of duration time at −1MV/cm field under light for TFTs with (a) mf-PVD SiO2, (b) mf-PVD Al2O3 and (c) PECVD SiO2. (d) VTH shift of all a-IGZO TFTs as a function of stress time.
it is clear that the PECVD SiO2 layer's hydrogen content is 6.43 at.% which is much higher than 1.01 at. % of mf-PVD SiO2 layer and 2.8 at.% of mf-PVD Al2O3 layer.

In bias stress experiments in the dark (NBS and PBS) and under light (NBIS) conditions, the change at back channel interface due to the ESL deposition dominate the VTH shift. Not much is reported on these stress stabilities for PVD ESL based TFTs. In few publications where PVD layer (SiO2 and Al2O3) is used as passivation layer15–16 or as dopant blocking layer,21 little explanation around the NBS and PBS is provided. In our previous work; we compared the mf-PVD SiO2 ESL based TFT characteristics and their bias-stress stabilities (NBS and PBS) data. In addition NBIS data for all the SiO2 ESL based TFT characteristics and their bias-stress stabilities (PBS and NBS) to high temperature (300 ◦C) PECVD SiO2 and low temperature (200 ◦C) SiO2 ESL based TFTs.22 We observed that high temperature PECVD SiO2 ESL and mf-PVD SiO2 ESL based TFTs show comparable characteristics. Here we extended our work with the addition of mf-PVD Al2O3 ESL TFT characteristics and their bias-stress stabilities (NBS and PBS) data. In addition NBIS data for all the ESL stacks (PECVD SiO2, mf-PVD SiO2 and mf-PVD Al2O3) have been elaborated on. In PBS as the TFT operate in fully on mode, only the ESL deposition dominate the VTH shift. Not much is reported on the ESL deposition in case.24,26 We also extracted the traps for all the three different type of TFFs with NBIS data from the equation: Trap Charges = (∆VTH∗Cox); where Cox = (KSiO2 × Kt) / (Xox) cm−2, where ∆VTH is voltage shift under NBIS, KSiO2 = 3.9 for SiO2, Kt = 8.854e−12 F/m, Xox is the thickness of dielectric. With the assumption of uniform distribution these empty regions of poor passivation. Moisture reaching the a-IGZO layer enhances the generation of shallow donor states created by visible light radiation and thus induces an increase in carrier density within a-IGZO. This enhances the conductivity and so reflects in large negative shifts under bias conditions. Other possible explanation is the peak hydrogen concentration which varies opposite to deposition temperature in PECVD processes i.e. layers at 200 ◦C will contains higher hydrogen than that of layers at higher temperature. These results support the conjecture that a significant amount of hydrogen must have been incorporated for low temperature layers case. Hydrogen is well known to contribute shallow donor states to a-IGZO, which increases their electrical conductivity. It is very probable that the incorporation of hydrogen has generated donor states within the a-IGZO bulk, hence inducing a large –ve shift due to the additional carriers. Over all in both the PBS and the NBS cases, the difference in the amount of the VTH shift originate from the difference in bond structure at the a-IGZO/ESL interface. The deposition temperature of SiO2 has a strong influence on both the microstructure of SiO2 and the a-IGZO/SiO2 interface bonding state. The silicon oxide layer when deposited at a higher temperature (>300 ◦C) much stronger bonds could be formed at the interface.22,24 The quality of the a-IGZO/SiO2 interface is conjectured to determine the VTH shift of all TFTs in bias tests. Reported higher temperature (deposited >300 ◦C) PECVD ESLs or passivation and dual layer passivation layers stacks due to their much better passivating properties do not show similar kind of large PBS and NBS shifts.25–26 Quite similar to NBS explanation, the back channel interface change produces a substantial instability under NBIS. It is reported that the back channel interface exhibits a high density of near valence-band-maximum (VBM) states caused by oxygen vacancies (VO), which generate holes by photo-exciting electrons to the conduction band when illuminated.27–28 The holes then diffuse to the interface of the gate dielectric by the assistance of the negative bias stress. Post a-IGZO process integration steps affect these back channel interface VBM states. ESL and passivation layers are used to prevent these back surface changes, however, the deposition conditions of those layers also impact the VBM states. The amount of oxygen, hydrogen and water molecules, which are present in these layers, become very important. It is also mentioned that increasing the amount of incorporated hydrogen (occurring during PECVD ESL deposition) increases the NBIS related instability due to formation of a hydrogen-related complex29–30 and incorporated O2 (possible in case of PVD ESL) in a-IGZO reduces the deep traps caused due to oxygen vacancy related defects.31 In summary, PVD SiO2 is deposited in oxygen rich plasma and this reduces the deep trap states close to the back surface. PECVD SiO2 doesn’t oxidize a-IGZO, but introduces interstitial hydrogen into the material which doesn’t reduce the deep trap states and involve in large VTH shifts. To counter this some groups established N2O plasma treatment to back a-IGZO surface prior to PECVD SiO2 deposition. This treatment oxidizes the top surface of the IGZO and reduces the deep traps caused due to oxygen vacancy related defects.31 It doesn’t oxidize a-IGZO, but introduces interstitial hydrogen into the material which doesn’t reduce the deep trap states and involve in large VTH shifts.

Table II. Properties comparison of the mf-PVD SiO2, mf-PVD Al2O3 and PECVD SiO2 layers.

| SiO2 Parameters      | RT mf-PVD SiO2 | RT mf-PVD Al2O3 | 200◦C PECVD SiO2 |
|----------------------|----------------|----------------|-----------------|
| Deposition Rate (nm) | Medium         | Medium         | High            |
| Etch Rate in 8% BHF (nm) | 33             | 37             | 112             |
| Breakdown (MV/cm)   | 8              | 7              | 5.9             |
| Hydrogen Content (%) | 1.01           | 2.91           | 6.41            |
| Dielectric Constant | 3.9            | 8              | 5.7             |
| Leakage @ 2MV/cm²    | 2.8 at.%       | 1.01 at.%      | 6.41 at.%       |

Figure 5. ERD comparison of mf-PVD SiO2, mf-PVD Al2O3 and PECVD SiO2 layers.
the above calculated charges were divided by thickness of a-IGZO. It is observed that the numbers for the PECVD SiO2 layer’s TFTs were much higher i.e. 1.5 e18 cm−3 than in case of PVD layer case TFTs i.e. 4.50 e17 cm−3 in PVD SiO2 TFTs and 3.00 e17 cm−3 in PVD Al2O3 TFTs. Overall the lower hydrogen content of mf-PVD layer and its better passivating properties could be the reasons behind better bias-stress stabilities of mf-PVD ESL based TFTs but parameters such as layer’s density, dielectric constant and leakage, which correspond to the number of defects and the dangling bonds, can also influence the TFT characteristics. Further if we assumed that increased trapping due to higher defect density of the ESL would be the main issue, the improvement in bias-stress stability with PVD ESL should mostly be visible in the negative bias-stress and not significantly influence the positive bias-stress. As we see improvement in both positive and negative bias-stress stability (under dark), which is more in-line with changes in the bulk properties of a-IGZO with mf-PVD layer as ESL.

Conclusions

In summary, mf-PVD SiO2 and mf-PVD Al2O3 ESL based a-IGZO TFTs has been realized. In comparison to the conventional PECVD SiO2 ESL based TFTs, the TFTs with mf-PVD (SiO2 and Al2O3) ESL exhibited better bias-stress stabilities under dark and light conditions. Better passivation properties and the lower hydrogen content of mf-PVD (SiO2 and Al2O3) layers has been identified as the major cause of this difference.

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