Integrated Design of Information Security Chip Based on Artificial Intelligence System Level Package (Sip)

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Abstract. At present, because of the information security chip encryption, authentication, storage and other advantages of multiple integration, and can provide a more complete and confidential information protection services, it has increasingly become a leading technology to dominate the information security market, information security applications in the future of the main development trend. The purpose of this paper is to promote the further development of information security technology through the integrated design of information security chip based on the system level packaging of artificial intelligence. This paper first introduces the system-level packaging technology, artificial intelligence technology and related design algorithms, and then proposes a specific design scheme of system-level packaging information security chip integration based on artificial intelligence starting from specific design experiments. The experimental results show that compared with the traditional technology supported by SOC, the security performance of the integrated design proposed in this paper is improved by about 17%, the information processing performance is improved by about 22%, and the signal cycle is accelerated by about 16%.

Keywords: Artificial Intelligence, System-level Packaging, Information Security Chip, Integration Design

1. Introduction

With the development of artificial intelligence and electronic technology, the demand for integrated circuit is getting higher and higher, especially in the field of information security chip. In order to meet this requirement, this problem has been solved in the way of chip system for a long time in the past, but this way has great limitations in terms of specific chip integration [1-2]. Therefore, many scientists have proposed solutions based on encapsulation, and thus proposed a system-level encapsulation solution based on artificial intelligence [3].
Since system-level packaging is related to the further development of electronic product functions and security systems, and society has high requirements for information security chips, domestic and foreign scholars have conducted a series of studies on them \[4\]. In literature \[5\], the author compares the applications of traditional SOC technology and system-level packaging technology in the field of electronic products, and compares and illustrates the advantages and disadvantages of the two technologies. In the literature \[6\], the author analyzed some problems existing in the current stage of the technology from the analysis of the key technologies of system-level packaging, and proved that the key to the current technical problems lies in the development of high-performance substrates. In literature \[7\], the author introduces the specific requirements of information security chip integration design at the present stage, and explains the corresponding functional states in detail.

In order to promote the further development of information security chip integration, promote the further improvement of electronic technology and information security. This paper first introduces system-level packaging technology, artificial intelligence technology and related design algorithms, and then proposes a specific design scheme for system-level packaging information security chip integration based on artificial intelligence \[8-9\] based on specific design experiments. The research in this paper not only promotes the rapid development of information security chip integration design in the future, but also lays a theoretical foundation for future research \[10\].

2. Method

2.1. System-level Packaging

By means of any combination, the active electronic devices with different function types and passive electronic components with selective characteristics are composed to form a single standard package that can provide multiple functions. Finally, a relatively complete system is produced, which is called system-level package. Systems-level packaging takes each component in a single module into consideration and shows great advantages over traditional SOC, which are mainly reflected in the aspects of precise packaging, multi-function design, short time to enter the market and low development cost. System-level packaging is supported by a whole technology platform, in which substrate design, new media and flip chip technology are the key components of the technology platform. The characteristics of system-level packaging are mainly shown in the following two aspects: first, it changes the state of components on the traditional PCB board, realizes the collection of discrete components to integrated components, and forms a miniaturized comprehensive system; Second, the chip in system-level package has different process and function, and the system function is relatively complete.

2.2. Artificial Intelligence

Artificial intelligence (AI) is developed on the basis of the rapid development of information technology. It is an interdisciplinary subject established by integrating a variety of disciplines, including computer science, information theory, psychology, neurophysiology and other aspects. The intelligent behaviors that intelligent robots can perform that are closely related to human intelligence are usually called artificial intelligence. The activities related to human intelligence include a series of thinking activities such as recognition, judgment, reasoning and thinking. The system-level encapsulation based on artificial intelligence satisfies the requirements of high performance,
autonomous control and security of information security chip. The chip is based on a cryptographic algorithm that provides security for information security chips. The specific algorithm is as follows:

\[ E = (a_1, a_2, ..., a_n) + b \]

\[ F = f_1 + f_2 + ... + f_n/n + c \]

In formula (1), E represents the optimal path for information transmission security, \( a_1 \) represents the specific path choice of information transmission, while b represents the fixed security factor. In formula (2), F represents the artificial intelligence construction scheme, while F represents the security function index.

3. Experimental Introduction

In order to ensure the scientific integration design scheme, this paper provide sufficient data for their design support, the author first refer to the relevant data such as ten thousand square, hownet website, analyzes the present research information on the arrangement, a total of 26 references, refer to related information to the relevant research data classification, data collected from research, the data is the important experiment data in this article. Secondly, in order to ensure the accuracy of the experimental results, the author carefully selected the specific software platform and experimental equipment needed for the experiment. The data of the specific experimental equipment and its model are shown in Table 1. The data in the table are the results collected and sorted by the author. Finally, after the completion of the integrated design of the information security chip, in order to ensure that the design can be put into use smoothly, the author carries out testing experiments on the integrated design of the information security chip based on the system-level packaging of artificial intelligence.

Table 1. Experimental equipment and model data

| Name of the equipment     | Equipment model       |
|--------------------------|-----------------------|
| Design software          | Risc CPU              |
| Processor                | Aemel AT45DB321       |
| Storage                  | Cadence Allegro SPB   |
| Experiment chip          | ISRSAMM11KBV1         |
| Detection software       | Linux Fedora 8.0      |

*Data are derived from the results of experimental collation*

4. Discuss

4.1. Integration Design Scheme

The author collected the research data and experimental data, including the characteristics of the artificial intelligence system level of packaging design, put forward the following specific design
scheme, the design scheme of the specific as follows: first, an analysis the demand of the design goals, according to the requirements of information security chip integrated sufficiency to consider design specifications, including substrate materials, heat dissipation, constraints, information, and reliability and so on several aspects; Second, the circuit details of the information security chip are designed. Two key issues need to be considered in this phase of design. Firstly, it is the problem of chip distribution and connection mode of each part of the substrate, because its specific distribution and connection will have a direct impact on the reception of chip signals. Secondly, it is about the design of substrate passive devices, which requires comprehensive consideration of process limitations, parameters and frequency. The third is the system level packaging layout and planning and design, in the design of this phase, the author defines each active and passive components in the substrate concrete distributed by the set of encapsulation structure, concrete structure design plan should consider connecting method, the size of the packaging and various aspects such as the placement of concrete way and, for those cooling demand larger chips to separate sex a design of the cooling channels. Another upon completion of the aspects of planning layout, also need to check the planning mode is a feasible, on the layout in the specific time to clear the influence of information transmission, thus to determine port to meet specific letter well, the most important thing is to the power distribution system to evaluate the accuracy of the previous phase, once appear, questions about the system performance, etc. timely modify optimization, and design to achieve the optimal effect. Fourth, layout physical layout circuit design. According to the constraint information, including electrical and physical aspects, each component is placed in the design area defined in the previous planning step, and detailed wiring is carried out. It should be noted here that the circuit return route of each part of the power system should be comprehensively considered when wiring, and the corresponding distribution between the power supply layer and the grounding plane should be conducted according to the different ages of the voltage, so as to minimize the crosstalk probability between the chips. All clock connections need to be isolated from other signal lines to promote EMI reduction. In addition, the function consumption of each key chip is estimated, and then the heat dissipation performance of system-level package is analyzed and optimized by means of 3d model and finite element analysis. Fifth, simulation check after wiring. After the wiring is completed, it is necessary to check the specific rules of the design, and at the same time, extract the specific clock signal, CPU input information signal and memory signal effectively, and simulate the transfer entity under the key signal network, so as to maximize the accuracy of the time series and waveform of the verification signal. The specific content of simulation is shown in Table 2.

Table 2. Simulation content

| Simulation content     | Specific level                      | Proportion |
|------------------------|-------------------------------------|------------|
| Clock synchronization signal | Signal quality            | 56.12%     |
|                        | Set up the time                |            |
| Asynchronous signal    | Monotony, overshoot tolerance and small oscillation | 61.34%     |
| Cabling area           | Cross talk between lines        | 59.86%     |
Table 2 for the simulation of the specific content and proportion of content are analyzed, from the data in the table can see, timing and signal quality problems in the simulation process is regular, more direct influence on the effect of integration design, therefore, the author from the three aspects of the above problem is optimized, the first to adjust the characteristics of the transmission line impedance; Secondly, the distance between the wiring adjustment; Then the resistance of the pin end resistance is adjusted. The ultimate purpose of such adjustment is to ensure the final transmission speed and quality of the signal, so as to meet the requirements of the relevant design. Sixth, with the help of relevant software technology, drilling and light drawing software are finally generated to produce the data output. Seventh, by the packaging manufacturer in the design documents on the basis of the packaging design of the sample packaging manufacturing; Finally, the overall function of the integrated design sample is tested.

4.2. Integrated Design and Detection of Information Security Chip

In order to ensure the smooth production and use of the integrated design of information security chip, it is necessary to carry out feasibility test on the integrated design in this paper. The experimental data obtained by the author are shown in Figure 1 and Figure 2 through testing experiments.

![Data Comparison Between SOC and SIP Integration Design](image)

**Figure 1.** Data comparison between SOC technology and sip technology in integration design
Figure 2. Prediction of information security development under SIP technology integration design

From the data in Figure 1, we can see that compared with the traditional technology supported by SOC, the integrated design proposed in this paper has improved security performance by about 17%, information processing performance by about 22%, and signal cycle by about 16%. From the data in Figure 2, we can see that the improvement degree of information security in the future is positively correlated with the effect of SIP technology integration design. As the technology continues to mature, information security has been rapidly improved. In summary, the information security chip integration design based on artificial intelligence (SIP) is scientific and feasible.

5. Conclusion

In order to effectively solve the problems of integration in confidence security system, this paper proposes an integrated design scheme of information security chip based on artificial intelligence (AI) based on the existing research data, and probes into the important issues such as layout and wiring simulation, function and performance verification of package samples, and proves the feasibility of this design. The research of this paper not only promotes the further development of the information security field, but also lays a theoretical foundation for the future research on related aspects.

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