Mitigating Read-disturbance Errors in STT-RAM Caches by Using Data Compression

Sparsh Mittal

Abstract

Due to its high density and close-to-SRAM read latency, spin transfer torque RAM (STT-RAM) is considered one of the most-promising emerging memory technologies for designing large last level caches (LLCs). However, in deep sub-micron region, STT-RAM shows read-disturbance error (RDE) whereby a read operation may modify the stored data value and this presents a severe threat to performance and reliability of STT-RAM caches. In this paper, we present a technique, named SHIELD, to mitigate RDE in STT-RAM LLCs. SHIELD uses data compression to reduce number of read operations from STT-RAM blocks to avoid RDE and also to reduce the number of bits written to cache during both write and restore operations. Experimental results have shown that SHIELD provides significant improvement in performance and energy efficiency. SHIELD consumes smaller energy than two previous RDE-mitigation techniques, namely high-current restore required read (HCRR, also called restore-after-read) and low-current long latency read (LPLL) and even an ideal RDE-free STT-RAM cache.

Index Terms

Non-volatile memory (NVM), cache memory, STT-RAM, read disturbance error, data compression, reliability.

I. INTRODUCTION

Recent trends of increasing core-counts and LLC capacity have motivated researchers to explore low-leakage alternatives of SRAM for designing large LLCs. Due to their high density and near-zero leakage power consumption, non-volatile memories such as STT-RAM and ReRAM (resistive RAM) have received significant attention in recent years [1], [2]. Of these, STT-RAM is considered especially suitable for designing LLCs due to its close-to-SRAM read latency and high write endurance [3].

Since the write latency/energy of STT-RAM are higher than those of SRAM, previous work has mainly focused on addressing this overhead to enable use of STT-RAM for designing on-chip caches [4]. However, a more severe issue of ‘read disturbance error’ (RDE) in STT-RAM caches has not been adequately addressed. Specifically, with feature size scaling, the write current reduces, however, read current does not reduce as much [5]. In fact, for sub-32nm feature size, the magnitude of read current becomes so close to the write current that a read operation is likely to modify the stored data and this is referred to as RDE (refer Section II for more details). Since reads happen on critical access path, RDE is likely to severely affect performance and reliability. In fact, it is expected that with ongoing process scaling, readability and not writability will become the most crucial bottleneck for STT-RAM [6], [7]. [8]. [9].

Contributions: In this paper, we present a technique, named ‘SHIELD’, which shields STT-RAM caches against both RDE and high write latency/energy overhead. SHIELD works by using data compression to reduce the number of...
bits written to cache (Section III). Firstly, SHIELD does not write any bits to STT-RAM block for all-zero data, since during next read operation, such data can be reconstructed from compression encoding bits. This avoids RDE and high write latency/energy issue for all-zero data. Secondly, SHIELD keeps two copies of data in the block if the data have compressed width ($CW$) of at most 32B (assuming 64B block size). On the next read operation, one copy gets RDE which is not corrected since the second copy still remains free of RDE. This avoids one restore operation for such narrow data ($0 < CW \leq 32B$). On any future read to this block, the single error-free copy of data is read and then restored. Thirdly, for any data with $CW > 32B$, including an uncompressed data-item, a single copy is written which is restored after each read operation.

**Salient Features:** By virtue of writing compressed data, SHIELD reduces the bits written in restore operation and saves write energy. Thus, SHIELD addresses both RDE and write overhead issue for compressed data, whereas previous techniques [10], [11] reduce some restore operations only and do not reduce the overhead of read and write operations (Section IV). SHIELD forgoes the capacity advantage of compression and thus, stores only one cache line in a block. Hence, SHIELD does not suffer from overheads which generally accompany compression techniques [12] such as extra tags, compaction, fragmentation, changes in cache replacement policy, etc. Further, some techniques for reducing soft-error vulnerability in SRAM caches (e.g., [13]) work by keeping two or three copies of an entire cache block (64B) in a cache set. This, however, leads to sharp degradation in cache capacity. By comparison, SHIELD duplicates compressed data of at most 32B size within a 64B cache block itself, and thus SHIELD does not degrade cache capacity. While SHIELD can work with any compression technique, in this paper, we demonstrate SHIELD with base-delta-immediate (BDI) compression algorithm [14].

**Evaluation and results:** We have performed microarchitectural simulation with an X86 full-system simulator (Section V). Also, we have compared SHIELD with two mechanisms for addressing RDE, namely restore-after-read (also called high-current restore required read or HCRR) and low-current long latency read (LCLL) (refer Section V-D). The results show that SHIELD provides higher performance and energy efficiency compared to these techniques (Section VI). Compared to an ideal RDE-free STT-RAM LLC, for single and dual-core configurations, SHIELD provides energy saving of 1.7% and 3.0%, respectively, whereas LCLL (which, on average, performs better than HCRR) incurs energy loss of 5.1% and 5.2%, respectively. Also, the relative performance with SHIELD is $0.98 \times$ and $0.97 \times$, whereas that with LCLL is $0.96 \times$ and $0.96 \times$, respectively. Additional experiments show that SHIELD works well for different cache sizes and selective replication used in SHIELD contributes positively to its effectiveness.

**II. BACKGROUND**

We now provide a brief background and refer the reader to previous work for more details [5], [15], [16].

**A. Motivation for using non-volatile memories**

Conventionally SRAM has been used for designing on-chip caches. However, SRAM has low density and high leakage power due to which large SRAM caches contribute greatly to the overall power consumption. Although several architectural techniques have been proposed to manage the power consumption of SRAM caches, such as cache reconfiguration, near-threshold computing, etc., the power budget targets of next-generation systems require magnitude order higher energy efficiency. This has motivated the researchers to explore alternatives of SRAM, such as eDRAM, STT-RAM, etc. [17].
B. Working of STT-RAM

STT-RAM utilizes a Magnetic Tunnel Junction (MTJ) as the memory storage. An MTJ contains two ferromagnetic layers separated by an oxide barrier layer. The magnetization direction of one ferromagnetic layer is fixed while that of the other ferromagnetic layer can be altered by passing a current. The resistance of the MTJ is determined by the relative magnetization direction of these two layers. If the two layers have different directions, the resistance of the MTJ is high and vice versa. Using this property, a binary value is stored in an STT-RAM cell [4]. Another characteristic of STT-RAM is that the read and write operations to it are asymmetric, since a write operation consumes larger time and energy than a read operation.

Although STT-RAM has lower density than PCM and RRAM and higher write latency and energy than SRAM, it has been widely used for designing caches due to its high write endurance. Another advantage of STT-RAM is that its non-volatility can be traded to improve its write energy and latency. Based on the application characteristic and the level of cache hierarchy, a designer can choose a suitable value of retention period.

C. Origin of read-disturbance error

STT-RAM stores data in magnetic tunnel junction (MTJ) [3]. For performing both read and write operations to MTJ, a voltage is applied between bit line and source line. The only difference between read and write operations is that read operations use smaller voltage than write operations [10]. With decreasing feature size, there is an exponential reduction in MTJ area [10] such that halving the feature size leads to 25% MTJ area and 75% write current reduction. However, read current does not scale well with feature size scaling since sensing correct data using low-current (< 20µA) is challenging [5], [11]. At large feature size (e.g. 130nm), read current is much lower than the write current, however, at small feature size (e.g. 32nm), read and write current magnitudes become so close that a read may inadvertently write (i.e., disturb) the cell being read. This is referred to as RDE.

D. Characteristics of read-disturbance error

RDE is data-dependent, e.g., using read current from BL to SL disturbs cells storing ‘1’ only and not ‘0’. In STT-RAM, reads and writes cannot be independently optimized, e.g., reducing the MTJ thermal stability for improving switching performance increases probability of read disturbance and thus, RDE mitigation involves tradeoffs. For these reasons, RDE is expected to become the most severe bottleneck in STT-RAM scaling and performance.

It is interesting to note the difference between the read disturbance error in STT-RAM and the write-disturbance error (WDE) in PCM [6], [18]. While RDE affects the same cell which is read, WDE affects the nearby cells. Also, RDE happens on a read operation whereas WDE happens on a write operation.

E. Strategies for addressing RDE

There are several possible strategies for addressing RDE:

1) One possible approach for reducing RDEs is to increase STT-RAM write current, which increases the margin between read and write currents. However, since STT-RAM write current and energy values are already high, increasing them further will make STT-RAM unsuitable for use in designing on-chip caches.

2) Conventionally, error-correcting codes are used for mitigating errors in caches [19], [20] and along similar lines, ECC can be used for mitigating read-disturbance error in STT-RAM [21]. However, at small feature sizes, RDE
4) Once the data-value is sensed by sense amplifiers (SAs), it remains locked in SAs and thus, it remains correct (free of RDE) [11]. Hence, after a read operation, writing the stored data back to cells (called ‘restore’ operation) can avoid RDE. This scheme, known as restore-after-read (or HCRR) has been used in a recent STT-RAM prototype [5]. However, this scheme fails to leverage the properties of data value and cache access behavior and hence, incurs large energy and performance penalty (refer Section VI-A).

5) To address RDE, low-current sense amplifiers can be used which have larger sensing period. This approach does not create RDE but may increase sensing latency by three times [22], [11], which harms performance.

6) Other researchers have proposed architectural management techniques, such as phased access of MRU and non-MRU ways [23], avoiding restore operations by using LCLL reads [11], data compression [24], data-duplication [24], by exploiting cache/register-file access properties [10], [25] and by using an SRAM buffer to absorb reads for minimizing reads from STT-RAM [25]. By comparison, some techniques postpone restores by scheduling them at idle times.

Clearly, architecture-level techniques for mitigating RDEs such as SHIELD can complement device-level techniques and can be especially useful at small feature sizes.

F. Cache properties

A cache has a set-associative structure, where a newly-arrived cache block may reside in any of the cache ways, as decided by the cache replacement policy. The optimization target for designing each level of cache is different. The first-level cache (L1) is accessed very frequently and hence, it should have high speed and write endurance, even if it has a small size or high leakage power. The last level cache (L2 in this paper) is designed to reduce off-chip accesses and hence, it must have large capacity. A high latency of last level cache can be usually tolerated using techniques such as instruction-level parallelism. In general, based on their latency and write endurance values, along with capacity advantage, STT-RAM is more suitable for the last level cache than the first level cache. Further, based on the latency-tolerance property of L2 cache, we use data compression in L2 cache and not in L1 cache.

III. SHIELD: KEY IDEA AND ARCHITECTURE

Before describing the main idea and working of SHIELD in detail, we briefly discuss the compression algorithm used. We also define a metric which is helpful in understanding the effectiveness of any RDE-mitigation technique.

A. Compression algorithm

SHIELD uses data compression approach for reducing the amount of data written to cache. While SHIELD can work with any compression technique, in this paper, we illustrate its working using BDI (base-delta-immediate) compression algorithm [14] due to its low decompression latency and reasonable compression ratio.
It is well-known that for many cache blocks, the difference between the values stored in the blocks is small \cite{12}. Based on this, BDI represents a block with a base and an array of differences, which reduces the total block size compared to the original size. To compress blocks with two different dynamic ranges, BDI uses two bases where one base is always zero and the second base is taken from actual data-contents \cite{14}. BDI algorithm first tries to compress every element using a zero base. Then, for any uncompressed block, compression is attempted by taking the first uncompressed element as the base. A 1-bit mask is used to record whether the corresponding base is zero.

A BDI-compressed block is represented as $B_p\Delta_q$, where $p$ and $q$ represent the size of base and Delta (difference), respectively. BDI uses 6 such patterns, viz. $B_8\Delta_1$, $B_8\Delta_2$, $B_8\Delta_4$, $B_4\Delta_1$, $B_4\Delta_2$ and $B_2\Delta_1$. BDI also checks if the block has repeated 8-byte values or is all-zero \cite{14}. Thus, after attempting to compress the block data using these 8 compression states, the one providing the smallest compressed size is finally chosen.

\section*{B. Defining consecutive reads}

For any cache block, we define a metric \textit{consecutive-read (CRead)}, which measures the average number of consecutive reads (i.e., no intermediate writes) seen by it during its residency in LLC. Also, for any application, the CRead is defined as the average CRead for all its cache blocks. Note that CRead is defined differently than the ‘reuse-count’ of a block which measures both read and write operations in one generation of a block. For example, in Figure \ref{fig:1} CRead for the block is $2 = (2+1+3)/3$, whereas reuse-count is 8.

\section*{C. SHIELD: Key Idea}

Caches work on the temporal locality principle, which states that a data item which is referenced at one point of time will be referenced again in near future. Such data item is stored in caches to avoid accessing main memory. For an RDE-affected STT-RAM cache, data are written to cache on both actual write operations and restore operations. To reduce the data written to STT-RAM during both these operations, SHIELD writes data in compressed form using BDI algorithm. This reduces the STT-RAM cache write energy. We perform two optimizations to BDI algorithm \cite{30}, \cite{24} for avoiding restore operations and further reducing the amount of data written to cache.

First and importantly, for data with all-zeros, no bit is stored in the STT-RAM block since the original uncompressed data can be easily recovered based on compression state encoding bits. Second, the first delta in BDI algorithm is always...
zero since it is the difference between the non-zero base with itself. Hence, we do not store this delta. The corresponding element is generated from the non-zero base.

Based on our optimizations and LLC access pattern, SHIELD uses the following insights to reduce restore operations.

1. For all-zero data \((CW = 0)\), no bits are written to or read from STT-RAM blocks and thus, RDE does not occur for such data. Hence, all the restore operations to such data are completely avoided.

2. It is well-known that due to filtering from L1 cache, LLC sees much smaller data locality than L1 cache [31]. Hence, most LLC blocks are read only few times. In fact, our experiments have shown that average value of CRead for single and dual-core configurations is 1.61 and 1.32, respectively (refer Figures 3(c) and 4(c)). Clearly, after any write operation, cache blocks see less than 2 read operations. Based on this, SHIELD keeps two copies of the data with \(0 < CW \leq 32B\) within the same block. On a later read operation, one copy gets RDE, whereas the second copy still remains free from RDE. Thus, keeping two copies is equivalent to restoring the data at the time of original write operation to avoid one future restore operation. Thus, if CRead value is less than two, keeping two copies can avoid at least half of the restore operations for such narrow-width \((0 < CW \leq 32B)\) blocks.

Fig. 2. Overview of SHIELD and action taken on a cache write operation

D. Action on read and write operations

We now discuss the action taken by SHIELD on any write and read operation.

Write operations: On any write operation, the cache controller compresses the data and computes CW. For \(0 < CW \leq 32\), two copies of data are stored and for other CW values, only one data copy is stored. Figure 2 summarizes the action taken on a write operation and benefit/cost incurred for different CW values. Table I shows the 4-bit encoding used for different compression states for BDI algorithm. Out of 16 combinations from 4 bits, 13 combinations are utilized and the remaining 3 are not utilized. For each block, this 4-bit encoding is stored at the time of a write operation using a memory technology that does not suffer from RDE (e.g. SRAM). Note that due to our optimizations to BDI algorithm (refer Section III-C), the sizes of compressed blocks are different in our work (shown in Table I) than those in the original BDI algorithm [14].

Read operations: On any read operation, first the encoding (E) is consulted. If \(E = 0000\), then the zero-data are reconstructed without accessing the block which avoids RDE and need of restoration. If \(E = 0011, 0110, 1101\) or 0111, it implies that \(0 < CW \leq 32B\) and 2 copies of data are stored. Hence, one copy is read, no restore is performed and the
TABLE I
ENCODING AND COMPRESSED SIZES FOR DIFFERENT BDI COMPRESSION STATES, ALL SIZES ARE IN BYTES (ENC. = ENCODING, UNCOMP. = UNCOMPRESSED)

| Enc. | State | Copies | Size | Enc. | State | Copies | Size |
|------|-------|--------|------|------|-------|--------|------|
| 0000 | Zeros | 1      | 0    | 1100 | B₄Δ₁ | 1      | 19   |
| 0001 | Repeat| 1      | 8    | 1101 | B₄Δ₁ | 2      | 19×2 |
| 0011 | Repeat| 2      | 8×2  | 0100 | B₄Δ₂ | 1      | 34   |
| 0010 | B₈Δ₁ | 1      | 15   | 1110 | B₂Δ₁ | 1      | 33   |
| 0110 | B₈Δ₁ | 2      | 15×2 | 1000 | B₈Δ₄ | 1      | 36   |
| 0101 | B₄Δ₂ | 1      | 22   | 1111 | Uncomp.| 1      | 64   |
| 0111 | B₈Δ₂ | 2      | 22×2 |      |       |        |      |

encoding is changed to 0001, 0010, 1100 and 0101, respectively, which indicates that now only one (error-free) copy of data is stored in the block. If \( E = 0001, 0010, 1100, 0101, 0100, 1110, 1000 \) or 1111, then data value is read, a restore operation is issued and the encoding remains unchanged.

E. Overhead assessment

Latency overhead: The latency overhead of BDI compression and decompression is 2 and 1 cycles, respectively [14]. We account for these values in performance simulation. Since STT-RAM write latency is high, a small value of BDI compression latency is easily hidden.

Energy overhead: We now compute the energy overhead of compression and decompression. From Wu et al. [32], we note that a 1-byte (8-bit) adder consumes nearly 15 fJ energy. Assuming that a subtractor also consumes same amount of energy, we first compute the overhead of compression by counting the number of subtractions in BDI algorithm. Each of \( B₈\Delta₁ \), \( B₈\Delta₂ \) and \( B₈\Delta₄ \) perform seven 8-byte subtractions. Both \( B₄\Delta₁ \) and \( B₄\Delta₂ \) perform fifteen 4-byte subtractions and \( B₂\Delta₁ \) performs thirty-one 2-byte subtractions. Repeated value detection requires seven 8-byte subtractions. Thus, there are 406 (=3×7×8+2×15×4+1×31×2+7×8) byte subtractions, which consume 6.09 pJ (=406×15 fJ). To account for other overheads and zero detection circuit, we increase the value and assume the overhead of compression as 8 pJ. As for decompression, it requires a maximum of thirty-one 2-byte additions, which consume 0.93 pJ (=31×2×15 fJ). Hence, we assume the decompression overhead as 1 pJ. We account for these overheads in energy computations.

To see the energy overhead of encoding bits, we note that a 2-bit counter consumes 0.1pJ in each access [33], thus a 4-bit counter would consume 0.20pJ. Since the encoding is written at the time of a cache write, we compare this energy with the write energy of STT-RAM cache. From Table II, write energy of 4MB L2 cache is 0.389nJ and thus, the dynamic energy of encoding bits is 0.05% of the cache energy. Hence, we ignore its contribution in energy.

IV. SALIENT FEATURES OF SHIELD AND QUALITATIVE COMPARISON

Some researchers have proposed techniques for addressing RDEs in STT-RAM caches. The technique of Wang et al. [10] seeks to avoid restore operations for blocks which are expected to see a write operation in near future. To perform L2 restore operations and updating L1 or L2 metadata bits, their technique requires observing the state of the block in other (i.e., L2 or L1) cache. Also, their technique postpones restore operations and hence, in their cache design, a dirty L2 block may have RDE. Since this RDE-affected L2 block cannot be written back to memory, their technique writes back the corresponding block in L1 cache directly to memory. Due to these, their technique complicates cache
management and incurs overhead which increases with rising number of cores. Also, their technique would require significant modifications to work with different cache coherence schemes, however, they do not present these details. By comparison, SHIELD performs restore operations immediately and hence, always keeps the L2 cache RDE-free. Also, SHIELD works based on data-width only and hence, can be integrated with any cache coherence scheme.

Jiang et al. [11] propose selectively performing short-latency read (requires restore) and LCLL read (long-latency read with no requirement of restores) depending on whether a particular bank is idle. However, short-latency reads still require restores and LCLL reads increase read latency. A key benefit of SHIELD is that it avoids read, write and restore operations for all-zero data and restore operations for narrow data. Thus, SHIELD addresses both write latency/energy overhead and RDE issue by using data compression. By comparison, previous techniques [10], [11] reduce some restore operations only and do not reduce read operations or address the overhead of write operations. Also, the technique of Jiang et al. [11] is proposed for main memory where the memory controller buffers read/write requests. Due to differences in cache and main memory architecture, their technique may not be applicable or effective for caches.

To reduce the restore energy, some researchers propose restoring only cells with ‘1’ value [10], since only these cells may be disturbed during reads. These techniques are orthogonal to SHIELD and hence, can be easily integrated with it.

Note that SHIELD does not use an additional buffer for postponing refresh operations and performs any required restore operation immediately after a read operation. Thus, the data in the cache are always kept error-free. Also, SHIELD actually reduces restore operations, whereas techniques that use a buffer for postponing restore operations do not reduce restore operations, but merely reschedule them to avoid interfering with normal accesses.

V. EXPERIMENTATION PLATFORM

A. Simulator parameters

We use Gem5 simulator to perform simulations using detailed timing model. L1 data/instruction caches have 32KB size with 2-way associativity. The L1 caches are private to core and the L2 cache (LLC) is shared between cores. The size of L2 cache in single and dual-core configurations is 4MB and 8MB, respectively. All caches are write-back and use LRU replacement policy. The L2 cache parameters for 16-way STT-RAM L2 are obtained using DESTINY [34], [35], [36] for 32nm feature size. We assume that the cache is optimized for write EDP (energy-delay-product) and uses sequential tag-data access. The values obtained are shown in Table II.

|                | 2 MB | 4 MB | 8 MB | 16 MB |
|----------------|------|------|------|-------|
| Hit latency (ns) | 4.063 | 3.737 | 4.058 | 4.350 |
| Miss latency (ns) | 1.976 | 1.567 | 1.805 | 1.814 |
| Write latency (ns) | 4.920 | 4.970 | 5.003 | 5.145 |
| Hit energy (nJ) | 0.264 | 0.304 | 0.333 | 0.391 |
| Miss energy (nJ) | 0.107 | 0.105 | 0.112 | 0.113 |
| Write energy (nJ) | 0.366 | 0.389 | 0.427 | 0.490 |
| Leakage power (W) | 0.019 | 0.044 | 0.072 | 0.138 |
B. Workloads

We use all the 29 benchmarks from SPEC2006 suite with reference inputs and 3 benchmarks from HPC field (shown as italics in Table III) as single-core workloads. Using these, we randomly create 16 dual-core multiprogrammed workloads, such that a benchmark is used exactly once. Table III shows the workloads.

| Single-core workloads and their acronyms |
|-----------------------------------------|
| As(aster), Bw(bwaves), Bz(bzip2), Cd(cactusADM) |
| Ca(calculix), Dl(dealII), Ga(gamess), Gc(gcc) |
| Gm(gemsFDTD), Gk(gobmk), Gr(gromacs), H2(h264ref) |
| Hm(hmmer), Lt(lbm), Ls(leslie3d), Lq(libquantum) |
| Mc(mcf), Mt(milc), Nd(namd), Om(omnetpp) |
| Pe(perlbench), Po(povray), Sj(sjeng), So(soplex) |
| Sp(sphinx), To(tonto), Wr(wrf), Xa(xalancbmk) |
| Ze(zeusmp), Co(comd), Lu(lulesh), Xb(xsbench) |

| Dual-core workloads (using acronyms shown above) |
|-------------------------------------------------|
| BwLu, PeLq, XaTo, CaMc, GkLh, GmWr, PoSp, NdGr, GcMi, BzZe, LsSo, SjXb, OmH2, CoCd, AsDl, HmGa |

C. Simulation completion strategy

In multiprogrammed workloads, different programs have different IPCs and thus, different rate of progress. Hence, they may execute the same number of instructions in different amount of time. Due to this, a strategy is required for ensuring that in each run with a workload (with baseline or a technique), the number of instructions simulated should be nearly equal.

One strategy for this is to simulate each workload for a fixed number of cycles, however, in this strategy, the number of instructions simulated may be different for baseline and a technique, depending on the performance impact of a technique.

We use another strategy, where we simulate every workload till each application in the workload has executed nInst instructions. The value of nInst is 150M for single-core workloads and 100M for dual-core workloads. This keeps the simulation turnaround time manageable since we perform detailed timing simulation with a full-system simulator and simulate a large number of workloads, techniques (baseline, SHIELD, HCRR, LCLL) and their parameter configurations/variants. The early-completing benchmarks continue to run but their IPC (instruction per cycle) is recorded only for the first nInst instructions, following the well-established simulation methodology [36], [30]. Remaining metrics are computed for the whole execution, since they are system-wide metrics (whereas IPC is a per-core metric).

D. Comparison with related schemes

Our baseline is an ideal scheme that assumes a cache free of RDE. We compare our technique with two other schemes for mitigating RDE.

High current restore required read (HCRR) : This technique uses normal current (20µA) to read the STT-RAM cell and performs a restore (i.e. write) operation after every read operation to correct the RDE. This technique is also referred to as refresh (or restore) after read [10] and ‘disruptive reading and restoring’ [27] technique.
Low-current long latency read (LCLL): To avoid RDEs, low-current (~10μA) sense amplifiers (SAs) can be used which have larger sensing duration \cite{22}, \cite{11}. These SAs also require extra sensing stages to minimize sensing margin degradation due to variations in STT-RAM cells. This approach, referred to as LCLL, does not create RDE, but incurs 3× the sensing latency of traditional SAs \cite{22}, \cite{11}.

![Graphs](image)

Fig. 3. Results for single-core system

### E. Evaluation Metrics

We use the following evaluation metrics:

1) L2 cache energy (leakage+dynamic)

2) Weighted speedup (referred to as relative performance), defined as \(\Sigma_n (IPC_n (\text{technique})/IPC_n (\text{baseline})) / N\), where \(N\) is the number of cores.

3) Average CRead value for baseline (Section III-B).

4) \(\Delta \text{BWPKI} (=\text{BWPKI}_{\text{technique}} - \text{BWPKI}_{\text{baseline}})\), where BWPKI refers to bytes written to cache per kilo instruction. BWPKI shows the write traffic to cache and since compression changes the size of each block, we have used BWPKI instead of writes per kilo instruction. Thus, \(\Delta \text{BWPKI}\) shows the increase in write traffic due to RDE.
under any technique (SHIELD or HCRR) compared to an ideal RDE-free cache. Since this metric for LCLL is nearly zero, we do not show this value for LCLL in Figures 3(d) and 4(d).

For SHIELD, we also show

5) **Compressed width (CW) of data on each cache write.** We classify the CW values in four ranges (refer Table I):

- \( CW = 0 \), \( 0 < CW \leq 32B \) (i.e. \{8B,15B,19B,22B\}),
- \( 32B < CW < 64B \) (i.e. \{33B,34B,36B\}),
- \( CW = 64B \) (i.e. uncompressed).

6) Percentage of restore operations avoided (RstAvd). Let \( \text{Reads}_{CW=0} \) be the reads to blocks with \( CW = 0 \) data and \( \text{Reads}_{0<CW\leq32\text{ _2copy}} \) be the reads to blocks with \( 0 < CW \leq 32B \) data having two copies. Then, \( \text{RstAvd} = \frac{(\text{Reads}_{CW=0} + \text{Reads}_{0<CW\leq32\text{ _2copy}})}{\text{TotalReads}} \times 100 \)

Note that for BDI algorithm, \( \text{Reads}_{CW=0} \) corresponds to \( E = 0000 \) and \( \text{Reads}_{0<CW\leq32\text{ _2copy}} \) corresponds to \( E = 0011, 0110, 1101 \) or \( 0111 \).

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**VI. RESULTS AND ANALYSIS**

**A. Main Results**

Figure 3 and 4 shows the results and Table IV summarizes the results. We now analyze the results.
**TABLE IV**

|                   | Single-core |         |         | Dual-core |         |         |
|-------------------|-------------|---------|---------|-----------|---------|---------|
|                   | SHIELD      | HCCR    | LCLL    | SHIELD    | HCCR    | LCLL    |
| **Energy Saving** | 1.73%       | -6.57%  | -5.09%  | 3.03%     | -6.96%  | -5.23%  |
| **Rel. Perf.**    | 0.98×       | 0.93×   | 0.96×   | 0.97×     | 0.93×   | 0.96×   |
| **ΔBWPKI**        | -1980       | 2085    | -4      | -1725     | 1877    | -5      |

**SHIELD:** Compared to the RDE-free cache (baseline), both HCRR and LCLL incur *energy loss*, whereas SHIELD provides *energy saving*. Also, SHIELD provides higher performance than HCRR and LCLL. The energy and performance improvement of SHIELD for an application depends on the fraction of restores avoided. This, in turn, depends on the compressibility of application’s data blocks and its read/write access pattern, specifically its CRead value. Out of total 48 workloads, compared to baseline, SHIELD saves energy for 28 workloads and improves performance for 18 workloads.

**Results on percentage of restores avoided:** For single and dual-core configurations, SHIELD reduces 50.7% and 48.5% of restore operations, respectively. For many applications, more than 95% of restores are avoided, e.g. Bw(99.3%), Gk(98.8%), Lb(99.3%), Lq(96.3%), Lq(99.9%), Sj(95.4%), Wr(97.0%), Ze(97.4%), Co(99.9%), Lu(99.9%), BwLu(99.7%), GkLb(99.4%), SjXb(96.3%), etc. This happens because either these applications have highly compressible data and/or their CRead values are small.

**Data compressibility and CRead results:** For some applications, more than 95% of blocks are all-zero ($CW = 0$), e.g. Bw(97.8%), Gk(98.2%), Lq(99.9%), Sj(98.9%), Wr(97.9%), Co(99.9%), Lu(99.9%), BwLu(98.7%), GmWr(98.2%), etc. Similarly, low CRead values for Gk(0.04), Lb(0.0003), Lq(0.0003), Sj(0.03), Wr(0.02), Ze(0.03), Co(0.002), Lu(0.0006), GkLb(0.006), BzZe(0.01), SjXb(0.02) etc., indicate that only few restore operations are required for these applications since SHIELD avoids restores for narrow-data ($0 < CW \leq 32B$) and these applications are read-unintensive. For these applications, large performance improvement and energy saving are achieved and write traffic is significantly reduced.

For some applications CRead values are small, (e.g., Mi(0.006), etc.), but only few blocks are compressible. Opposite is true for applications where CRead values are high, (e.g. Bw(5.58), BwLu(2.40), PeLq(3.14), etc.), but most blocks are compressible. From perspective of energy saving with SHIELD, these effect partially cancel each other, and hence, these applications show only small energy gain/loss.

For some applications, CRead values are high, e.g. Gc(2.20392), Gm(2.0307), Ca(7.88), Nd(8.42531), Om(2.27), Pe(6.16507), So(2.286), Xa(2.32), etc. The restore requirement for these applications is also high and thus, restore operations lead to performance and energy loss for these applications. On using SHIELD, only four out of 48 workloads show relative performance less than 0.90× viz. Gc(0.89), Pe(0.83), Xa(0.84) and XaTo (0.88×). Similarly, in some applications, most blocks are either incompressible or have compressed width greater than 32B, e.g., Gc, Gm, Hm, Mi, Pe, Po, To, Xa, XaTo, PoSp, HmGa, etc., and hence, compared to RDE-free baseline, SHIELD incurs energy loss or very small energy saving due to restore operations.

**ΔBWPKI results:** SHIELD brings large reduction in cache write traffic, which is due to the use of compression and avoiding many restore operations. Especially for applications with compressible data, SHIELD brings large reduction in BWPKI, e.g., Bw(23606), Gk(6011), Sj(6945), Co(10942), Lu(6397), BwLu(16015), GkLb(5281) etc. Clearly, in addition to RDE, SHIELD also addresses the write overhead in STT-RAM caches.

**Overhead of (de)compression:** For single and dual-core systems, the compression and decompression energy (refer
Section III-E together account for 0.14% and 0.15% of the total L2 energy. Clearly, the energy overhead of SHIELD is negligible.

We conclude that SHIELD can bridge the large performance gap between an ideal RDE-free cache and an RDE-affected cache that uses restore-after-read (HCRR) scheme. Also, SHIELD completely removes the energy overhead of restore operations and hence, it has lower energy consumption and lower LLC write traffic than an ideal RDE-free cache.

**HCRR:** With HCRR, each read operation also leads to a write operation and thus, HCRR causes significant increase in write traffic to STT-RAM cache. The increase in BWPKI is especially high for read-intensive applications, e.g., Bw(20844), Bz(4181), Sj(5478), BwLu(10194), BzZe(4218), CoCd(3858), etc. Since STT-RAM writes have high energy/latency overhead, HCRR incurs large energy and performance loss and is also likely to cause bandwidth issues. In fact, the worst case performance with HCRR can be very poor, e.g., Bw(0.76×), Gc(0.87×), Pe(0.82×), Po(0.89×), Xa(0.83×), BwLu(0.84×), PeLq(0.88×), XaTo(0.88×), CoCd(0.86×), etc. Also, for some applications, HCRR incurs more than 10% energy loss, e.g., Ca(-12.4%), Gm(-10.7%), Pe(-10.1%), Sp(-10.6%), XaTo(-10.6%), CaMc(-12.1%), PoSp(-12.6%), etc. With increasing number of cores, the LLC access intensity increases and hence, restore operations will cause port obstruction and make the LLC unavailable for serving accesses. Clearly, due to its large penalty, use of HCRR in performance-critical systems is challenging.

| TABLE V |
| PARAMETER SENSITIVITY RESULTS (RstAvd = % RESTORES AVOIDED) |

| | Single-core | | Dual-core | |
|---|---|---|---|---|
| **Energy Saving** | | Rel. Perf. | ΔBWPKI | RstAvd | | Energy Saving | Rel. Perf. | ΔBWPKI | RstAvd |
| Default | 1.73% | 0.981× | -1980 | 50.7% | 3.03% | 0.973× | -1725 | 48.4% |
| SHIELD1 | 1.84% | 0.978× | -2003 | 45.3% | 3.16% | 0.967× | -1726 | 43.9% |
| SHIELD3 | 0.79% | 0.980× | -1938 | 50.4% | 2.70% | 0.972× | -1692 | 48.5% |
| Half-size L2 | 2.84% | 0.980× | -1983 | 50.3% | 3.77% | 0.983× | -1799 | 48.1% |
| Double-size L2 | 1.1% | 0.977× | -1970 | 51.0% | 3.39% | 0.992× | -1710 | 49.0% |

**LCLL:** LCLL degrades performance by slowing down the read operations. Since read operations happen on critical access path, the large read latency in LCLL may not be easily hidden. In worst case, LCLL can cause large energy loss, Sp(-18.1%), PoSp(-11.2%). On average, LCLL incurs energy loss for both single and dual-core configurations, whereas SHIELD saves energy. Compared to RDE-free cache (baseline), LCLL has negligible impact on BWPKI, whereas SHIELD brings large reduction in BWPKI (as shown above), thus, SHIELD reduces the write traffic to cache more effectively than LCLL.

Although LCLL provides better performance and energy efficiency compared to HCRR, a crucial limitation of LCLL is that use of small read current in LCLL can lead to decision failure [27], such that it may not be possible to distinguish between two states of a bit-cell during read operation. Also, since process variation affects device parameters [37], to guarantee RDE-free read operations, the value of read current needs to be set even lower than that assumed here [8]; this, however, would further increase the read latency and cause performance loss. Given this, SHIELD presents as a better technique for mitigating RDE than LCLL.

**B.Parameter Sensitivity Results**

We henceforth focus exclusively on SHIELD. Also, we omit per-workload results for brevity and only present average results in Table V. For comparison purpose, the results with default parameters are also shown.
1) **Effect of Replication:** As shown in Section III-C, SHIELD replicates the narrow \((0 < CW \leq 32B)\) data to reduce restore operations. We now present two variants of SHIELD which explore the tradeoffs associated with it.

**SHIELD1:** SHIELD1 does not replicate a data-item with width \(0 < CW \leq 32B\), but otherwise works same as SHIELD. For BDI algorithm, four states, viz., repeated value, \(B_8\Delta_1\), \(B_8\Delta_2\) and \(B_4\Delta_1\) have \(CW\) at most \(32B\).

SHIELD1 reduces the number of bits written originally at the cost of incurring one extra restore operation later. Due to this, SHIELD1 saves higher energy but achieves lower performance than SHIELD (Table V) and thus, a designer can choose an appropriate variant to optimize a metric of interest. It is noteworthy that the higher performance of SHIELD can reduce execution time which leads to lower leakage power in other processor components and hence, SHIELD may be preferable over SHIELD1. Also, SHIELD avoids larger percentage of restore operations than SHIELD1. For single and dual-core systems, \(0 < CW \leq 32B\) data account for 14.3% and 10.0% of data blocks (refer Figures 3(c) and 4(c)) and thus, due to the relatively smaller contribution of \(0 < CW \leq 32B\) data, the difference between performance/energy of SHIELD and SHIELD1 is relatively small.

**SHIELD3:** On any write operation, SHIELD3 makes three copies of data with \(0 < CW < 22B\), but otherwise works same as SHIELD (i.e., two copies of data with \(0 < CW \leq 32B\) and one copy for other data). For BDI algorithm, three states, viz., repeated value, \(B_8\Delta_1\), and \(B_4\Delta_1\) have \(CW\) at most \(22B\).

SHIELD3 avoids the need of restore on two read operations at the cost of increasing the bits written to cache initially. However, SHIELD3 reduces energy saving without providing corresponding performance improvement. This is because average CRead values for single and dual-core configurations is 1.61 and 1.32, respectively (refer Figures 3(c) and 4(c)). Thus, most L2 cache lines see less than two consecutive reads and hence, keeping three copies does not generally avoid an extra restore operation compared to keeping two copies. Further, SHIELD3 may have higher complexity than SHIELD due to keeping two and three copies of data of different widths.

2) **Effect of cache size:** To evaluate the impact of cache size, we experiment with half and double of default L2 cache size (4MB for single-core and 8MB for dual-core).

In general, restore operations incur larger overhead at lower cache sizes due to increased cache contention and hence, the scope of energy/performance gains with lower-sized caches is also higher. Hence, SHIELD brings larger gains at smaller cache sizes (refer Table V). Overall, SHIELD performs consistently well at different cache sizes: maintaining performance close to baseline, saving energy, avoiding nearly half of the restores and bringing large reduction in write traffic.

### VII. Conclusion and Future Work

In this paper, we presented a technique to mitigate read-disturbance errors in STT-RAM caches. Our technique uses compression and selective duplication of compressed-data to address both RDE and write overhead issue in STT-RAM. Experimental results performed with single and dual-core system configurations have shown that our technique is effective in improving performance and energy efficiency in presence of RDE. Also, it outperforms two other techniques for mitigating RDE.

We now list some possible directions for future work:

1) Our future work will focus on synergistic integration of SHIELD with device-level techniques (e.g., [15]) to reduce RDEs and approximate computing techniques to tolerate RDEs [38].
2) By reducing the read accesses to an STT-RAM cache, the read disturbance errors can be reduced. For achieving this, cache bypassing [] or read buffers can be used. Also, using

3) We also plan to explore SRAM-STTRAM hybrid caches (e.g., [39], [40]) where frequently-accessed blocks are migrated to SRAM. This will reduce pressure on STT-RAM ways and mitigate the impact of RDE on performance.

4) In this paper, we explored STT-RAM for designing CPU caches. CPUs primarily focus on optimizing latency in serial applications, and hence, they use large caches and small register file. By comparison, GPUs focus on optimizing throughput and hence, they use small caches and a very large register file to support their massively multithreaded architecture. Due to its high density, STT-RAM is suitable for designing GPU register file, however, the read-disturbance error may make this challenging. Some recent techniques seek to address this issue [25]. We plan to propose novel techniques for managing RDE in STT-RAM based GPU register file for improving performance and energy efficiency.

5) Several other emerging memory technologies provide attractive properties. For example, SOT-RAM (spin-orbit torque RAM) which does not suffer from read disturbance issue [41]. We also plan to explore use of domain wall memory for designing caches [42].

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