Systematic high-level design of a fifth order Continuous-Time CRFF Delta Sigma ADC

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Abstract—In this paper we present the development of a Systematic high level design model based on MATLAB scripts. It is integrated into a graphical behavioral model toolbox for the synthesis and simulation of a Continuous-Time Delta Sigma ADC. For this, we decided to use a Model-based design approach which it is adopted to address problems associated with designing complex control and signal processing systems such as the case of Continuous-Time Delta Sigma ADC. The goal of our study is the design of a 10 bit ENOB ADC for energy measurement systems used in particle identification through a new generation of detectors based on diamond. Results of the synthesis of a proposed fifth order Continuous-Time Delta Sigma ADC modulator for 10-bit ENOB ADC based on a Cascaded Resonators Feedforward architecture and simulations of the dispersion of its components (due to fabrication process) using the proposed tool are demonstrated and discussed.

Index Terms—Analog to digital converters, Continuous-time, Delta Sigma, CMOS analog integrated circuits, Mathematical modeling, front-end electronics, model-based design, circuit simulation.

I. INTRODUCTION

Designing complex Continuous-Time (CT) Delta sigma ($\Delta \Sigma$) ADC involves engineers who possess the knowledge, intuition, creativity, and technical expertise to turn their ideas into real-life devices [1]. Until now, this type of architectures does not appear in the field of designing electronics for particle detection. Yet, we believe that it can provide interesting solution, as we will be showing in the case of energy measurement systems.

This class of systems are classically designed as shown in figure [1](a). The problem with this topology is the analog shaping block, which represents a bottleneck when it comes to ensuring high accuracy and minimal variation between channels. It also limits the single chip integration with complexity, high power consumption and large area occupation. The idea here (for the second topology) is to digitize the signal as soon as possible as demonstrated in figure [1](b). To enable that, $\Delta \Sigma$ ADC are recommended as shown in [2], [3]. It was explained in the literature that these architectures – more precisely continuous time – are suitable for this kind of applications [4], [5]. The main difficulty remains in the complexity of the design of such architecture, since it requires frequency domain analysis that usually requires a lot of time, experience and effort. For this purpose, we propose in this article a systematic high-level design of a fifth order CT $\Delta \Sigma$ modulator for 10-bit ENOB ADC based on a Cascaded Resonators Feedforward (CRFF) architecture. To synthesis and design efficiently this modulator, we decided to adopt a model-based design approach built around the use of graphical behavioral models [1] that integrate the widely known Schreier’s Toolbox [6], then adding a set of custom scripts. This method allows firstly the synthesis of a CT $\Delta \Sigma$ modulator enabling different choices of specifications, then to simulate - given a set of conditions - the effect of the variations of each main parameter of the chosen topology. This permits us to extract information about the critical parameters so we can optimize the design of each constructive block.

All this development is based on MATLAB scripts applied to the graphical model and the conditions of simulations in SIMULINK.

For this paper, we will focus on the study the effect of component dispersion (due to fabrication process) of the loop coefficients of the proposed CT $\Delta \Sigma$ modulator.

The paper is organized as follows: In Section II, we present the different arguments for the chosen architecture and the targeted specifications. In Section III, we explain the systematic high-level system method (the algorithm of the script) to analyze the the effect of component dispersion. Section IV shows the results of simulations. We finish with conclusions and perspectives in Section V.
II. THE ARCHITECTURE OF CT $\Delta$Σ MODULATOR

A. Modulator specifications

For such application [7], we need to design an ADC with a resolution of 10 bits and a bandwidth of 40 MHz (we decided to target slightly larger specifications in order to anticipate any cause of degradation without affecting the application). The targeted specifications of the CT $\Delta$Σ ADC are resumed in table I.

### TABLE I: Proposed specifications of the CT $\Delta$Σ ADC

| Parameter          | Value         |
|--------------------|---------------|
| Signal bandwidth   | 40 MHz        |
| OSR                | 8             |
| Loop filter order  | $L = 5$       |
| Modulator ADC N    | 3-Bit         |
| Sampling frequency | 640 MHz       |
| Theoretical SQNR   | 80 dB         |
| Linearity          | <0.2%         |

The fact that we are designing a wide band modulator, oblige us to choose a low oversampling ratio topology in order to avoid more complexity problems in the acquisition phase; we decided to work with an OSR of eight, which means a sampling frequency of 640 MHz. To define correctly the rest of key specifications, we used equation (1):

$$SNR_{max}[dB] = 6.02N + 1.76 + (2L + 1) \log_{10}(OSR) + 10\log_{10}(2L + 1) - (2L)10\log_{10}(\pi)$$  (1)

It is already shown that the theoretical SQNR is usually chosen to be 10 – 20 dB higher than the required one in order to provide some tolerance for the inevitable degradation caused by the circuit non-idealities and to allow as much as possible of the noise budget for thermal noise [1], [6].

B. Architecture Selection

We chose to work with a Cascaded Resonators Feedforward architecture (CRFF) for the following reasons [1], [6], [8]:

- The first integrator of this architecture is wide band compared to other implementations which allows us to reduce both area and power consumption in terms of integrators implementations (size of capacitors).
- The use of large bias currents in the first stage that allow us to limit noise and distortion.
- Allow us to reach high SQNR values with low oversampling ratio (OSR) values.

Figure 2 illustrates a simplified block diagram of the proposed modulator.

This architecture was implemented as a graphical model in SIMULINK as explained in [1] based on the general definition presented in [6]. It is designed to meet the targeted requirement of table II.

III. SYSTEMATIC HIGH-LEVEL MODELING

In this section, we explain the use of the graphical behavioral simulation tool as an application of the model-based design approach. This allows to synthesize the parameters of the desired $\Delta$Σ modulator using Schreier’s Toolbox. After that, we discuss the integration of a MATLAB script that control the simulation settings of the graphical model for the study of the dispersion’s effect of the loop coefficients. This helps to reduce considerably the amount of time and effort applied during the schematic design phase. This method gives more information about the behavior of the topology than what is classically obtained via the use of Schreier’s toolbox at the same design phase.

A. Integration of MATLAB scripts

The idea behind this is to optimize the use of the graphical behavioral simulation tool using MATLAB scripts as shown in figure 3. This give us access to add new features and more control over the systematic design such as the case of parametric Monte Carlo like simulations to check the effect of every parameter choice in a fast way before going to the transistor level implementation. Usually, this class of models are used to create a reference theoretical “ideal” model of a topology. Thus, it is always described, as “it is only useful to simply illustrate the concept of a topology.” Yet, we believe that it has more potential when we combine it with MATLAB scripts in order to estimate as soon as possible in the design flow, the impact of non-idealities such as the case of process variation. We propose the integration of scripts that control the graphical model tool focusing on two main steps:

- First, we evaluate the theoretical impact of the choice of the main parameters on the signal-to-quantization-noise
Ratio (SQNR) using equation [1] In our case, this equation is calculated using MATLAB Symbolic Math Toolbox.
- Second, we give access to the value of each parameter of every building block. Every parameter is defined as a variable in MATLAB scripts before injecting it into the graphical model. Since the model is controlled by the set of scripts, we can create any type of scenarios where parameters can vary according to a defined function with a defined number of iterations.

B. Implementation of Monte Carlo like simulations

As an application to the feature explained above, we built Monte Carlo like simulations, where we vary independently each parameter following a normal distribution function in a chosen range of error. Using this, we can simulate in the case of this paper, the effect of component dispersion on the final SQNR value. This study is the first step to demonstrate the use of our proposed scripts as a fast method of designing CT modulators. It allows extracting a lot of useful information as explained below.

Figure 4 shows the results.

![Simulated SQNR of the simulated ADC](image)

We achieved a simulated ENOB of 12 bits using an input sine wave signal with a frequency of 35 MHz and an amplitude of 0.7 of the full input range referred to the unity as shown in figure 4 (As expected, we have around $-10$ dB compared to the theoretical SQNR). The obtained loop filter coefficients are summarized in table II. These Coefficients are used to calculate values for the component used in the implementation of the modulator such as the values of resistors and capacitors.

![Algorithm 1: Monte Carlo like simulation for parameters dispersion](image)

**Algorithm 1: Monte Carlo like simulation for parameters dispersion**

**Input:**
- $a_s, b_s, c_s, g_s$ // Calculated Coefficients using Schreier’s toolbox
- $\Delta p, \delta m$ // Process variation error, Mismatch error
- $K$ // Number of iterations, in our case $K = 10000$

**Output:**
- $a_i, b_i, c_i, g_i$ // Coefs adding dispersion
- $SQNR_i, ENOB_i$ // Calculated SQNR and ENOB for every added dispersion

**Function** GenerateDisp($a_s, b_s, c_s, g_s, \Delta p, \delta m, K$):

while $i \leq K$

Pick a random value $\Delta p_i \in [-\Delta p, \Delta p]$
Pick a random value $\delta m_i \in [-\delta m, \delta m]$
Calculate $a_i, b_i, c_i, g_i$ using equation [2]
Increment $i$ 
end 
return $a_i, b_i, c_i, g_i$

**Procedure** SimulateDisp($a_i, b_i, c_i, g_i, K$):

while $i \leq K$

Inject $a_i, b_i, c_i, g_i$ in SIMULINK Model
Run Simulation using a sinus input with $f_{in} = 40MHz$
Calculate $SQNR_i, ENOB_i$ using the digital output of the model
Increment $i$
end 
return $SQNR_i, ENOB_i$

**Table II: Coefficients of the loop filter**

| Coefficient | $a_s$ | $b_s$ | $c_s$ | $g_s$ |
|-------------|-------|-------|-------|-------|
| 1           | 4.4392 | 0.0493 | 0.2102 | 0.2102 |
| 2           | 6.3822 | 0.2762 | 0 | 1.1023 |
| 3           | 3.4840 | - | 0 | 0.9044 |
| 4           | 1.8533 | - | 0 | 0.7257 |
| 5           | 0.0382 | - | 0 | 0.4537 |
| 6           | - | - | 1.0000 | - |

**IV. Simulations results**

In this section, we present the results of the synthesis of the modulator and the analysis of the effect of component dispersion on the final SQNR value. This study is the first step to demonstrate the use of our proposed scripts as a fast method of designing CT modulators. It allows extracting a lot of useful information as explained below.

A. Synthesis results

The modulator was synthesized using the graphical behavioral simulation tool for the specifications shown in table I. The obtained loop filter coefficients are summarized in table II. These Coefficients are used to calculate values for the component used in the implementation of the modulator such as the values of resistors and capacitors.
TABLE III: Integrators specifications

| Integrator | Maximum output swing | DC Gain | Saturation |
|------------|----------------------|---------|------------|
| Integrator 1 | ±174 mV | 40 dB | 450 mV |
| Integrator 2 | ±170 mV | 40 dB | 450 mV |
| Integrator 3 | ±163 mV | 40 dB | 450 mV |
| Integrator 4 | ±189 mV | 40 dB | 450 mV |
| Integrator 5 | ±195 mV | 40 dB | 450 mV |

for the physical implementation. The main extracted parameters of the different Opamp-RC integrators are illustrated in table III.

B. Dispersion simulation

In this application example, we described the variation of each coefficient of the loop individually following a normal Gaussian distribution with $\Delta p = 20\%$ and $\delta m = 1\%$. Results of 10000 simulations are shown in figure 5.

Fig. 5: SQNR values for 10000 simulations with $\Delta p = 20\%$, $\delta m = 1\%$ on each coefficient

We can see that the modulator is not immune to this level of dispersion, which leads to many questions. In order to investigate this, we did a series of simulations to find the most critical parameters that cause this behavior. This time, we applied the same dispersion on one parameter a time, and for every simulation, and we found that the coefficients $a_1, a_2, b_1, c_1$, which are the most critical ones. We doubted that the main reason of this drop of SQNR is the saturation of integrators. To validate this hypothesis, we only reduced the range of $\Delta p = 10\%$, $\delta m = 0.5\%$ for these critical parameters.

Results of this simulation are presented in figure 6.

Fig. 6: SQNR values for 10000 simulations with $\Delta p = 10\%$, $\delta m = 0.5\%$ on each coefficient

We concluded that in order to guarantee the desired specifications, these parameters must be correctly designed within a range of error as low as possible.

V. Conclusion

In this paper, we discussed the development of a systematic high-level design a fifth order CT $\Delta \Sigma$ modulator for 10-bit ENOB ADC based on a CRFF architecture. The following results are reported here:

- We showed the use of the graphical behavioral models in the flow of design of CT $\Delta \Sigma$ modulators.
- We explained the synthesis of a fifth order CT $\Delta \Sigma$ modulator for 10-bit ENOB ADC based on a CRFF architecture.
- We presented the results of the study of the effect of the dispersion (due to fabrication process) of the loop coefficients taking into consideration the non-idealities of Opamp-RC integrators.

More non-idealities of the other blocks will be added to the model (DAC non-linearity, Jitter...etc.) which allow us to estimate more precisely the SQNR and calculate more key performances as the SNDR. This extracted data is used to design the building blocks using fast design methodologies such as: $\frac{g_m}{I_d}$.

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