A 5-13GHz Power Amplifier for UWB Applications in 40 nm CMOS Technology

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Abstract. A two-stage power amplifier using current multiplexing technology and resistor shunt feedback technology to flatten gain and expand bandwidth is designed in this paper. In this paper, the SMIC 40nm CMOS process is used. The power amplifier proposed works in the 5-13GHz frequency range, providing more than 10dB of the gain at the voltage of 1.0V, and has good input and output matching. The return loss is lower than -30dB. The stability factor Kf is maintained at about 1.1, and Bf is greater than 0. The peak power added efficiency of the power amplifier can reach 24%.

1. Introduction
The ultra-wideband technology has become more and more important in today's world, the advantage of which is that it can transmit data on a wide frequency band in a short time at a low power but at a higher rate. The ultra-wideband technology is different from the traditional narrow-band radios. The data energy in ultra-wideband is transmitted over a wide spectrum, not by modulating the power level, phase and frequency of the carrier signal to transmit information. This also makes the ultra-wideband technology have good anti-interference ability. With these application advantages, the UWB technology has been receiving great interest from the academic and industrial communities for many years. The ultra-wideband power amplifier is one of the key components in radio frequency transmitters, which provide the required transmit signal power to meet the specifications of various applications. Therefore, the design of the power amplifier needs a better balance between linearity, low power consumption, stability and high gain.

The ultra-wideband power amplifier introduced in this paper adopts resistor shunt feedback and current multiplexing technology, and can achieve gains of more than 10dB in the 5-13GHz frequency range, which satisfies the good match between input and output. What’s more, the circuit proposed can ensure that the stability and linearity of the entire system meet the design requirements.

2. Methodology

2.1. Resistor shunt feedback technology
As shown in the figure.1, it’s the simplest parallel resistance negative feedback amplifier and its small signal model diagram. Ignoring the influence of the gate-source capacitance Cgs, the corresponding S-parameter can be obtained as:

\[ |S_{11}| = |S_{22}| = \frac{R_f - g_m Z_0^2}{g_m Z_0^2 + Z_0 + R_f} \]

\[ |S_{21}| = G = \frac{2Z_0 - 2g_m Z_0 R_f}{g_m Z_0^2 + Z_0 + R_f} \]

\[ |S_{22}| = \frac{2Z_0}{g_m Z_0^2 + Z_0 + R_f} \]  

(1)

Among them, \(Z_0\) is the characteristic impedance, \(R_f\) is the parallel negative feedback resistance. When an exact match is achieved:

\[ |S_{11}| = |S_{22}| = 0 \]  

(2)

Therefore:

\[ G = 1 - \frac{R_f}{Z_0} \]  

(3)

From the above formula, the gain of the parallel negative feedback amplifier is mainly determined by \(R_f\) and has nothing to do with the frequency. By adjusting the size of the feedback input impedance, a flat gain can be obtained to achieve a wide frequency band.

2.2. Parallel Peaking Technology

The realization of parallel peaking technology at the output end expands the bandwidth and its cost is lower. figure. 2(a) shows a standard parallel-compensated common-source amplifier with an inductor in series at the load.

\[ vin \]

\[ vout \]

\[ R \]

\[ C \]

\[ I_{in} \]

\[ vout \]

\[ R \]

\[ C \]

\[ L \]

\[ vin \]

\[ vout \]

\[ R \]

\[ C \]

\[ L \]

Figure.2. (a) Parallel Fenghua amplifier. (b) Small signal model diagram
Considering the transistor as an ideal element, the bandwidth of the circuit is controlled by the resistance $R$, the inductance $L$, and the capacitance $C$. The element that plays a role in increasing the bandwidth is the inductance $L$. Figure 2 (b) is its equivalent small-signal circuit model. Through the series inductance, a zero point is added to the output impedance, expanding the circuit bandwidth. At the same time, it compensates to a certain extent the decrease in capacitance impedance when the frequency becomes larger. In general, the total output impedance value is kept approximately constant over a wide frequency range.

The impedance of the RLC structure network can be expressed as follows:

$$Z(s) = (sL + R)\left|\frac{1}{sC} + \frac{R[s(L/R) + 1]}{s^2LC + sRC + 1}\right|$$

(4)

$$|Z(j\omega)| = R\sqrt{\frac{1}{(1 - \omega^2LC)^2 + (\omega RC)^2}}$$

(5)

Let $m = \frac{RC}{L/R}$, $\tau = L/R$, then the normalized frequency-dependent impedance value is:

$$|Z(j\omega)| = \frac{R}{\sqrt{(1 - \frac{\omega^2\tau^2m^2}{1 + \omega^2m^2})}}$$

(6)

So:

$$\frac{\omega_2}{\omega_1} = \sqrt{\left(-\frac{m^2}{2} + m + 1\right) + \sqrt{\left(-\frac{m^2}{2} + m + 1\right)^2 + m^2}}$$

(7)

In order to maximize the bandwidth, $m = \sqrt{2} \approx 1.41$ should be taken. At this time, the frequency response has a peak of 20%[4], which is not conducive to the flatness index of the circuit. When $m = 2.41$, the frequency response of the circuit is the flattest. The corresponding $m$ value can be determined according to different index requirements of the actual design circuit, so as to obtain the best design[5].

2.3. Schematic design of power amplifier

![Figure 3. Recommended power amplifier schematic](image-url)
The proposed power amplifier is shown in figure 3. C1 and L1 form the simple input matching network, while C1 can also play a role in blocking DC. The first stage is a common source circuit that uses resistance shunt feedback technology [6]. The advantage is that it can provide higher gain and larger bandwidth for the circuit and improve the stability of the system. At the same time provide good reverse isolation and flat gain correspondingly.

In the second stage, two common source amplifiers are connected in cascode mode [7], so that the amplifier works in class AB. The use of feedback resistors allows current to be reused from the output end to the input end without additional drive current. This is the current reuse structure which can reduce the power consumption of the circuit. The inductance between the two transistors provides high impedance to suppress the movement of the AC signal from the output stage of M1 to the source stage of M2. C3 is the bypass capacitor. The output end inductor L7 and resistor R5 have peaking characteristics, which can widen the bandwidth and reduce the return loss of the output end.

3. Results
Several important parameters to measure the power amplifier are the input and output matching, gain, power and system stability of the power amplifier. The following will show the work of this PA from these aspects.

![Figure 4: Simulated stability parameters of PA (Kf & Bf)](image)

![Figure 5: Simulation result of input matching losses (S11)](image)

The stability of the power amplifier is considered by the simulation results of the two parameters Kf and Bf. As shown in the figure 4, the stability factor Kf of this circuit fluctuates around 1.1, and the stability factor Bf> 0, so the integrated design circuit has better stability [8]. figure 5 is the S11 parameter simulation of the power amplifier. It can be seen that the input return loss is less than -10dB in the range of 3.5-14GHz, which shows that the circuit has excellent input matching characteristics.

![Figure 6: Simulation result of output matching losses (S22)](image)

![Figure 7: Simulation result of variation of the gain (S21)](image)
As shown in figure 6, it's the S22 parameter simulation of the power amplifier. It can be seen that the output return loss is less than -14.5dB in the range of 4-14GHz, which shows that the circuit has excellent output matching characteristics. Figure 7 is the simulation of S21 gain parameters. In the range of 4.7 to 14 GHz, it can be seen that the gain is greater than 10.5dB, and the maximum gain can reach 26dB, indicating that the gain of the power amplifier meets the design requirements.

Figure 8 is the S12 parameter simulation of the power amplifier. It can be seen that the power amplifier achieves good reverse isolation of 30 dB in the frequency range of 4.7-13.7 GHz. Gain added efficiency is an important parameter to measure the performance of the power amplifier. As can be seen from the figure 9, the peak value of the power added efficiency of the power amplifier is 24%.

4. Discussion
This paper uses 40nm CMOS technology to design an ultra-wideband power amplifier in the 5-13GHz frequency range. The power amplifier uses resistance shunt feedback and current multiplexing technology, and uses peaking inductance to provide good input and output matching and stability. Post-layout simulation results indicate that the gain of the circuit proposed is greater than 10dB, and the input and output return loss are less than -10dB, and the reverse isolation is less than -30dB at the operating voltage of 1.0V.

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