Few electron limit of n-type metal oxide semiconductor single electron transistors

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Abstract

We report the electronic transport on n-type silicon single electron transistors (SETs) fabricated in complementary metal oxide semiconductor (CMOS) technology. The n-type metal oxide silicon SETs (n-MOSSETs) are built within a pre-industrial fully depleted silicon on insulator (FDSOI) technology with a silicon thickness down to 10 nm on 200 mm wafers. The nominal channel size of $20 \times 20$ nm$^2$ is obtained by employing electron beam lithography for active and gate level patterning. The Coulomb blockade stability diagram is precisely resolved at 4.2 K and it exhibits large addition energies of tens of meV. The confinement of the electrons in the quantum dot has been modeled by using a current spin density functional theory (CS-DFT) method. CMOS technology enables massive production of SETs for ultimate nanoelectronic and quantum variable based devices.

(Some figures may appear in colour only in the online journal)

1. Introduction

The fabrication of semiconductor quantum dots in complementary metal oxide semiconductor (CMOS) technology provides the ground for integration of existing microelectronics with ultimate nanoelectronics for quantum circuits. We report on the realization of single electron transistors (SETs) in pre-industrial CMOS technology at the limiting channel size of $20 \times 20$ nm$^2$ and on the characterization of the quantum transport at cryogenic temperature, enabling the detection of the first electron in the SET.

Silicon SETs based on CMOS technology represent a natural environment for realizing scalable electron spin and orbital quantum devices for quantum information processing [1] because of long coherence times [2] and scalability. The need to create a workable Hilbert space with good quantum numbers [3] at increasingly high temperatures towards room temperature operability implies a reduction of the size of the quantum dots down to the current limits.
of fabrication [4]. The drawback is an increasing sensitivity of the confinement potential imposed by the control gate to impurities and roughness, and a consequent impact on the electronic shell structure of the quantum dot. In the past, some approaches for creating single electron silicon quantum dots have been explored, including the employment of a gate induced two-dimensional electron gas (2DEG) at the Si/SiO₂ interfaces [5], global gate controlled edge roughness of an ultra-small nanowire [6], local gate equipped underlap geometry where the gate is not state-of-the-art and consequently enforces the use of large gate voltages [7], triple-layer gate stacks [8] and Si/SiGe modulation-doped heterostructures [9].

Our approach consists in confining electrons in a well defined bilateral doping modulation. Indeed barriers are a consequence of undoped silicon below spacers which are on both sides of the gate [10]. In the past, this approach has been exploited to fabricate compact double and triple quantum dots realized with only two gates [11]. The two main advantages are on one hand its compactness compared with previous state-of-the-art works on Si including an additional upper gate [12], and on the other the detection of a clear single electron regime.

The use of CMOS technology in quantum dot fabrication has the benefit of reproducibility and reliability, as well as the co-integration of quantum circuits with traditional CMOS.

In section 2 the fabrication of the CMOS device is illustrated, while in section 3 the simulation of electron confinement is discussed. In section 4 the quantum transport obtained in the 20 × 20 nm² samples at the temperature $T = 4.2$ K is presented.

2. Fabrication of the devices

For the purposes of repeatability and reliability our metal oxide silicon SETs (MOSSETs) are built within a pre-industrial fully depleted silicon on insulator (FDSOI) technology on 200 mm wafers. Only a few modules of the device are slightly modified, such as the gate stack and the source/drain (S/D) implantation. Since we aim to scale our MOSSETs down to 20 nm in both gate length and gate width dimensions, electron beam lithography was used for active and gate level patterning. Dots as small as $20 \times 20 \times 10$ nm³ are achieved with this process.

The undoped SOI layer is thermally thinned down to reach a silicon thickness of either 13 or 20 nm, depending on the sacrificial oxide thickness. After the first e-beam lithography treatment, the SOI layer is etched to pattern the active area above the buried oxide (BOX). As a result of these first process steps a silicon nanowire is achieved with this process.

Figure 1. (a) TEM micrograph of a typical scaled MOSSET adapted from the FDSOI technology. The polysilicon gate length is 22 nm long, and dot thickness is 17 nm (the dot width is not shown on this view). The SiO₂ gate oxide of 4 nm, the nitride spacers of 11 nm and the raised source/drain are also clearly visible. (b) Scheme of the simulated device. Light-blue represents the silicon nanowire. The tri-sided gate is highlighted in red whereas the source and drain contacts are in blue and silicon dioxide is in yellow. The electron density in the central planes of the nanowire is reported as color-scaled projections for the case of single electron occupancy of the dot.

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MOSSET coming from a wafer used for the morphological characterization with channel thickness $T_{Si} = 17$ nm, oxide thickness $T_{ox} = 4$ nm and gate length $L_g = 22$ nm realized with a process identical to the samples reported throughout the text.

3. Simulation of the electrostatic confinement

In order to evaluate the confinement of the electrons induced by the applied electrostatic potential we used a three-dimensional self-consistent simulator based on current spin density functional theory (CS-DFT) in the framework of the NanoTCAD ViDES package [13–16]. This package solves the many particle Schrödinger equation by means of CS-DFT, by transforming the many electron problem into a single electron problem with exchange–correlation potential. It embraces the local density approximation and the effective mass approximation with parabolic bands. The method provides the ground state of the system for each occupation number $N$ of electrons. They fill the lowest single-particle Kohn–Sham eigenvalues calculated for each spin and each pair $j = 1–3$ of the three $\Delta$ valley pairs aligned to the main directions in $k$ space.

The final shape of the confining potential energy is reached by self-consistently solving the Poisson equation. The effective nature of the confinement is due to the combination of the band alignment between the silicon and silicon dioxide and of the applied external potentials.

The SET is modeled as a silicon nanowire with length $L$ along the $x$ direction and with a rectangular section of area $W_{eff} \times T_{Si}$ on the $y-z$ plane with source and drain contacts at the head and tail of the nanowire on the top of a silicon dioxide slab of thickness $T_{box}$ (see figure 1(b)). The device has a tri-sided gate structure and the gate is insulated from the nanowire with a $T_{ox}$ thick silicon dioxide layer.

The many particle problem is solved in the entire silicon nanowire and in a $1 \text{ nm}$ thick region inside the surrounding oxide. Potentials to the tri-sided gate, source and drain regions are applied, whereas a zero electric field $z$-component boundary condition is forced at the bottom of the device. We simulate the electrostatic behavior of the SETs imposing an effective gate length $L_{g, eff} = 22$ nm, an effective width $W_{eff} = 10$ nm to take into account the variability of the lithography process on the nominal length $L_g = 20$ nm and both the variability of the lithographic process and the oxidation reduction on the nominal width $W = 20$ nm.

In figure 1(b) the electron density in the central planes of the nanowire is reported as color-scaled planes, showing a strong confinement in the region under the gate contact biased at $V_g = 26$ mV when one electron is in the dot. The first addition energy $E_{(2,1)}$ which provides the energy separation between the one-electron state and the two-electrons state has been calculated. By using the effective size of $L_{g, eff} = 22$ nm, $W_{eff} = 10$ nm we determined an addition energy of $E_{(2,1)} = 17 \text{ meV}$. Note that our simulations take into account all the couplings of the SET with the gate electrode but also with the source and drain contacts. Our approach does not take into account the possible disorder caused by the impurities and the interface roughness, which are expected to further enhance the confinement of the wavefunction in such small devices.

4. Quantum transport: experimental results

The investigation of the electronic transport through the devices yields both the electron filling as a function of the QD gate voltage $V_g$, as well as the addition energies $E_{(n+1,n)}$ needed to add the $(n+1)$th electron when $n$ electrons occupy the quantum dot. The characterization at the temperature $T = 4.2 \text{ K}$ of several nominally identical samples like those described in section 2 demonstrate that the transistors operate as single-electron devices, with relatively high addition energies.

In figure 2(a) the stability diagram of a typical device with of $L_g = 20$ nm and $W = 20$ nm is shown. The coupling with the source, drain and gate are $C_s = 1.0 \text{ aF}$, $C_d = 1.3 \text{ aF}$ and $C_g = 4.0 \text{ aF}$, respectively. The lever arm factor, which allows one to convert the voltage spacing between the peaks into
addition energies and which is defined as $\alpha = C_g/(C_g + C_s + C_d)$, assumes a value of 0.64. The first addition energy of the device shown in figure 2(a) is $E_{(g,1)} = 30$ meV. Figure 2(b) shows the Coulomb blockade observed from $N = 0$ up to a filling number of 6 in the range from −0.1 to 0.3 V. In the inset the results of the conductance measurement performed at room temperature are reported.

In these small devices it is possible to reduce the electron occupancy of the quantum dot down to the empty state, hence the transition from 1 to 0 electron occupancy of the SET becomes observable, a key step towards single electron charge and spin manipulation.

The experimental confirmation is obtained by the lack of Coulomb diamond and any detectable current (up to $V_d = 100$ mV) below the first reported Coulomb oscillation at $V_g = 40$ mV. Moreover we notice that there is no significant shift between the threshold voltage obtained at $T = 300$ K ($\sim 40$ mV) calculated as the maximum of the second derivative of the drain current with respect to the gate voltage; see inset of figure 2(b) and the gate voltage position of the first Coulomb peak at low temperature ($V_g = 40$ mV), taking into account the thermal broadening at $T = 300$ K.

The presented samples are smaller than similar samples previously studied ($L, W = 30–40$ nm [10], and [17]). The silicon thickness ($T_{Si} = 10$ nm) and the spacer length (11 nm) have been scaled down accordingly to obtain a good trade-off between the first electron orbital–electrodes coupling and a large Coulomb energy. By contrast, in previously reported similar devices [10] the first electrons in the accumulation channel are not detected and the first measurable current is at a significantly larger gate voltage than the threshold voltage at room temperature. On the contrary for similar samples but without nitride spacers [8], and therefore a smaller effective channel length, the first electrons are on shallow donors in the body of the silicon and detected at a gate voltage much below the threshold voltage at room temperature [18, 19]. In that case there is no MOSSET effect in the accumulation channel.

Similar results have been obtained in nominally identical devices. Because of the residual disorder determined by the interface roughness, the electron wavefunction is further confined so that the first addition energies are even larger than those predicted from the simulation of the devices and are subject to some variability. From the addition energies found in typical devices, an effective radius of less than 12–15 nm can be estimated.

5. Conclusions

Our results show that the CMOS technology used allows reliable fabrication of single electron transistors with a gate size of $20 \times 20$ nm$^2$. Strong confinement has been predicted by CS-DFT simulations and a clearly resolved Coulomb blockade pattern at 4.2 K with high addition energies of more than 20 meV exceeds the simulated values. The fabrication of SETs in CMOS technology provides the possible ground for integration between traditional microelectronics and quantum circuit oriented nanoelectronics.

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References

[1] Friesen M, Ruhheimer P, Savage D E, Lagally M G, van der Weide D W, Joynt R and Eriksson M A 2003 Practical design and simulation of silicon-based quantum-dot qubits Phys. Rev. B 67 121301
[2] Morton J J L, McCamey D R, Eriksson M A and Lyon S A 2011 Embracing the quantum limit in silicon computing Nature 479 343–53
[3] Friesen M, Chutia S, Tahan C and Coppersmith S N 2007 Valley splitting theory of SiGe/Si/SiGe quantum wells Phys. Rev. B 75 115318
[4] Pauluiac-Vaujour S et al 2011 Patterning strategy for monoelectronic device platform in a complementary metal oxide semiconductor technology Japan. J. Appl. Phys. 50 066GF15
[5] Xiao M, House M G and Jiang H W 2010 Parallel spin filling and energy spectroscopy in few-electron Si metal-on-semiconductor-based quantum dots Appl. Phys. Lett. 97 32103
[6] Kobayashi M, Miyaji K and Hiramoto T 2008 On the origin of negative differential conductance in ultranarrow-wire-channel silicon single-electron and single-hole transistors Japan. J. Appl. Phys. 47 1813
[7] Shin S J, Jung C S, Park B J, Yoon T K, Lee J J, Kim S J, Choi J B, Takahashi Y and Hasko D G 2010 Si-based ultrasmall multishifting single-electron transistor operating at room-temperature Appl. Phys. Lett. 97 103101
[8] Lim W H, Yang C H, Zwanenburg F A and Dzurak A S 2011 Spin filling of valley–orbit states in a silicon quantum dot Nanotechnology 22 335704
[9] Simmons C B, Thalakulam M, Shaji N, Klein L J, Qin H, Blick R, Savage D E, Lagally M G, Coppersmith S N and Eriksson M A 2007 Single-electron quantum dot in Si/SiGe with integrated charge sensing Appl. Phys. Lett. 91 213103
[10] Hofheinz M, Jehl X, Sanquer M, Molas G, Vinet M and Delelmonis S 2006 Simple and controlled single electron transistor based on doping modulation in silicon nanowires Appl. Phys. Lett. 89 143504
[11] Pierre M, Wacquez R, Roche B, Jehl X, Sanquer M, Vinet M, Prati E, Belli M and Fanciulli M 2009 Compact silicon double and triple dots realized with only two gates Appl. Phys. Lett. 95 242107
[12] Liu H W, Fujisawa T, Ono Y, Inokawa H, Fujiwara A, Takashina K and Hirayama Y 2008 Pauli-spin-blockade transport through a silicon double quantum dot Phys. Rev. B 77 073310
[13] Lisieri M, Fiori G and Iannaccone G 2007 3d simulation of a silicon quantum dot in a magnetic field based on current spin density functional theory J. Comput. Electron. 6 191–4
[14] Opensource release available at http://nanohub.org/tools/vides

[15] Fiori G, Pala M G and Iannaccone G 2005 Three-dimensional simulation of realistic single electron transistors IEEE Trans. Nanotechnol. 4 415

[16] Fiori G and Iannaccone G 2007 Three-dimensional simulation of one-dimensional transport in silicon nanowire transistors IEEE Trans. Nanotechnol. 6 524

[17] Roche B, Voisin B, Jehl X, Wacquez R, Sanquer M, Vinet M, Deshpande V and Previtali B 2012 A tunable, dual mode field-effect or single electron transistor Appl. Phys. Lett. 100 032107

[18] Pierre M, Wacquez R, Jehl X, Sanquer M, Vinet M and Cueto O 2010 Single donor ionization energies in a nanoscale cmos channel Nature Nanotechnol. 5 133–7

[19] Leti G, Prati E, Belli M, Petretto G, Fanciulli M, Wacquez R, Vinet M and Sanquer M 2011 Switching quantum transport in a three donors silicon fin-field effect transistor Appl. Phys. Lett. 99 242102