Simulation Study of Ge p-type Nanowire Schottky Barrier MOSFETs

Jaehyun Lee and Mincheol Shin

Abstract—Ambipolar currents in Germanium p-type nanowire Schottky barrier MOSFETs were calculated fully quantum-mechanically by using the multi-band $k\cdot p$ method and the non-equilibrium Green’s function approach. We investigated the performance of devices with [100], [110], and [111] channel orientations, respectively, by varying the nanowire width, Schottky barrier height, and EOT. The [111] oriented devices showed the best performance. In comparison to Si as a channel material, Ge is more desirable because more current can be injected into the channel, resulting in steeper subthreshold slope and higher on-state current. Our calculations predict that the Ge channel devices should have an EOT gain of $0.2 \sim 0.5$ nm over Si channel devices.

Index Terms—Germanium, Schottky barriers, MOSFETs, p-type MOSFETs, Nanowire, Non-equilibrium Green’s function, Hole transport, $k\cdot p$ method

I. INTRODUCTION

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ormalium has recently regained attention as a channel material to replace silicon in metal-oxide semiconductor field-effect transistors (MOSFETs) [1]-[4]. Ge is particularly well suited for p-type devices, thanks to its high hole mobility which is about four times greater than that of silicon, as well as some processing related issues, such as dopant solubility and Fermi level pinning at the valence band.

In this work, we explore the possibility of using Ge as a channel material in p-type MOSFETs with Schottky barrier (SB) contacts or SB-MOSFETs. Our motivation may be summarized as follows. Despite their advantages in reducing short channel effects (SCEs), SB-MOSFETs have the major drawback that on-state drain currents ($I_{\text{on}}$) are limited by the SBs at the channel/silicide interfaces [5]-[12]. A solution to this problem is to use a channel material with low SB height (SBH) and low effective masses to enhance the tunneling current ($I_{\text{tunn}}$) in the on-state. In this respect, Ge p-type SB-MOSFETs are quite promising because a low SBH for holes at Ge/metal interfaces is feasible (~ 0 eV or less) and the light hole effective mass ($m_{lh}$) of bulk Ge is as low as 0.046 $m_0$, where $m_0$ is the free electron mass [13]-[15]. Devices with nanowire configuration are considered in this work to assess their ultimate performance limits.

II. SIMULATION APPROACH

The structure of Ge p-type nanowire SB-MOSFETs is shown in Fig 1. To describe the hole transport in the Ge channel, we adopted the multi-band $k\cdot p$ method [16]. The $k\cdot p$ parameters for Ge have been adjusted, so that the nanowire subband structures of Ge calculated by the $k\cdot p$ method match those by the $sp^3$ s’ tight-binding (TB) method [17].

Simple parabolic effective mass (PEM) Hamiltonians were adopted to the metallic source and drain [18-20]. It was also assumed that the virtual valence band top and the effective mass were 1.0 eV above the Fermi level and 0.5 $m_0$ in the transport direction, respectively. These values have little effect on the results in this paper.

Accurate calculation of $I_{\text{tunn}}$ is vital in any SB-MOSFET simulations, and in this work, this has been implemented by treating the full quantum transport of holes. That is, the hole density and current were calculated by self-consistently solving Poisson’s equation and the non-equilibrium Green’s function (NEGF) equation [6] with the 6-band $k\cdot p$ Hamiltonian with spin-orbit coupling. Ballistic transport was assumed. The coupled mode-space $k\cdot p$ method was employed for efficient calculation [16,21].

Note that electron current was also calculated in this work. Since the band gap of Ge in bulk is only 0.66 eV, one should check whether the off-current ($I_{\text{off}}$) is limited by the ambipolar current. The electron transport in the n-branch was calculated by considering the eight equivalent $\Lambda$ valleys of Ge and the generalized effective mass Hamiltonian with the full inverse mass tensor was used.

III. RESULTS AND DISCUSSION

In our simulations of the Ge p-type nanowire SB-MOSFETs shown in Fig. 1, the Ge channel with a square cross-section of width ($W$) is assumed to be intrinsic. The gates surround the channel, and the channel length ($L$) is scaled as $L = 4W$. The equivalent oxide thickness (EOT) is 1 nm, SBH is 0.2 eV, and the drain voltage ($V_{DD}$) of -0.5 V is applied.

In the following, we first characterize the device performance of Ge p-type nanowire SB-MOSFETs. Fig. 1 shows the drain current ($I_D$)-gate voltage ($V_G$) characteristics of the device of $W = 10$ nm for the three channel orientations. The currents are ambipolar. Despite the fact that the band gap of Ge is quite small, the electron current in the n-branch has little effect on the off-state hole current in the p-branch. The fact that the effective SBH for electron is considerably raised due to the size quantization effect in nanowires also significantly...
contributes to the suppression of the electron current. Only the hole current is considered hereafter.

![Diagram of Ge p-type nanowire SB-MOSFETs.](image)

In the hole branch in Fig. 1, the crossover from the thermionic to the tunneling regimes is seen in the threshold region, which is typical in SB-MOSFETs. That is, in the inset of Fig. 1 where the $I_{\text{thm}}$ contribution to the $I_d$ is shown, the regions of $V_{g}V_{th} > V_{th}$ and $V_{g}V_{th} < V_{th}$ correspond to the thermionic- and tunneling-current dominant regimes, respectively, and between them, there is a transition region where we measure the subthreshold swing (SS).

![Graph showing $I_d$ vs $W$ for different EOT values.](image)

As seen in Fig. 1, the current level of the [111]-oriented device is about 2.5 times larger than that of the [100]-oriented device. The normalized $I_{\text{ON}}$ (divided by $W$) versus $W$ in Fig. 2 (a) consistently shows the behavior for the range of $W = 3 \sim 10 \text{ nm}$. $I_{\text{ON}}$ was calculated with $V_{DD} = -0.5 \text{ V}$ after adjustment of the gate work function such that $I_{\text{ON}} = 10 \text{ nA/\mu m}$. Note that the increase of $I_{\text{ON}}$ with the decrease of $W$ is usually observed in ballistic transistor simulations regardless of whether the contacts are ohmic or Schottky.

The dependence of the SS on $W$ is shown in Fig. 2 (b). As $W$ is reduced, the SS improves, which is due to the fact that current injection is enhanced with improved gate controllability at smaller $W$. The SS in the [111]-oriented devices is steeper than that in the [100]-oriented devices, which can be also clearly seen in Fig. 1. The superiority of the [111] channel orientation with respect to the SS is particularly noteworthy. For the [111] channel orientation, the device with $W = 10 \text{ nm}$ already achieves a SS of 100 mV/decade or below, whereas $W$ should be reduced to about 6 nm to achieve the same SS for the [100] channel orientation. This 'gain' of 3 ~ 4 nm in $W$ is an attractive factor in favor of the [111] channel orientation.

The performance disparity with respect to channel orientation is largely due to the different $m_0$. The $m_0$ value is lighter in the order of the [100], [110], and [111] directions in bulk, which are 0.046 $m_0$, 0.042 $m_0$, and 0.040 $m_0$, respectively, and the device performance improves in the same order. In fact, the hole effective masses become heavier as $W$ becomes smaller in all the three directions, but the bulk effective masses can still be useful for comparison.

Another important factor that affects $I_{\text{thm}}$ is the size quantization effect. This effectively raises the SBH by the quantization energy ($\phi_Q$), which increases sharply as $W$ is reduced below 5 nm. See Fig. 2 (c). The [100]-oriented device is most disadvantageous. The size quantization effect further lowers the device performance of the [100]-oriented device in comparison with the other orientations. Also, note the fact that the dependence of $I_{\text{ON}}$ on SBH is significantly more sensitive in the [100]-oriented device than in the other devices, as shown in Fig. 2 (d), which implies greater variability in orientation.

![Graph showing $I_{\text{thm}}$ vs EOT for different channel orientations.](image)

Figs. 3 (a) and (b) show the tunneling distance ($d_{\text{tunn}}$) in the on-state, which is defined to be the thickness of SB at the source Fermi level. As expected, the shortening of $d_{\text{tunn}}$ with the decrease of EOT is observed. Our calculation shows that $d_{\text{tunn}}$ is shortened by about 0.7 nm as EOT is reduced by 1.0 nm, leading to a rough estimation that $d_{\text{tunn}}$ linearly scales with EOT.
The above results for Ge p-type SB-MOSFETs are qualitatively similar to those obtained when Si is used as the channel material [9]. Quantitatively, however, Ge outperforms Si in all aspects, as will be discussed. The lighter \( m_0 \) of the former is considered the main factor in the significant difference. For instance, the \( m_0 \) value of Ge and Si are 0.11 \( m_0 \) and 0.20 \( m_0 \), respectively, for nanowire of \( W = 5 \) nm [17].

The \( I_{ON} \) of Ge channel devices is about 15–30 \% larger than that of Si devices. This translates into the EOT gain of 0.2 nm (see Fig. 3 (c)). That is, in achieving the same \( I_{ON} \), the EOT of Ge channel devices can be larger by the amount of the EOT gain than that of the Si channel devices. Note that the same SBH of 0.2 eV was used in this work for both Ge and Si channel devices. Considering the fact that the SBH for holes of the former is expected to be lower than that of the latter, the difference in \( I_{ON} \) can be further increased. When it comes to SS, there is even larger EOT gain of 0.5 nm as seen in Fig. 3 (d). For instance, to achieve an SS of 85 mV/decade, the EOT of the Si devices should be as small as 0.6 nm, whereas the EOT of the Ge devices can be 1.1 nm. Considering the gate leakage reduction associated with a thicker gate oxide, such an amount of EOT gain is quite significant.

IV. CONCLUSION

The device performance of SB-MOSFETs largely depends on how well current can be injected into the channel. In this respect, \( m_0 \) is the most important factor. Thanks to the small \( m_0 \) of Ge in the [111] direction, Ge p-type nanowire SB-MOSFETs oriented in this direction show superior performance to the other two orientations considered. In comparison to Si as a channel material, Ge is more desirable. Our calculations predict that Ge channel devices should have an EOT gain of 0.2 ~ 0.5 nm over Si channel devices.

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