The most promising quantum algorithms require quantum processors that host millions of quantum bits when targeting practical applications. A key challenge towards large-scale quantum computation is the interconnect complexity. In current solid-state qubit implementations, an important interconnect bottleneck appears between the quantum chip in a dilution refrigerator and the room-temperature electronics. Advanced lithography supports the fabrication of both control electronics and qubits in silicon using technology compatible with complementary metal oxide semiconductors (CMOS). When the electronics are designed to operate at cryogenic temperatures, they can ultimately be integrated with the qubits on the same die or package, overcoming the ‘wiring bottleneck’. Here we report a cryogenic CMOS control chip operating at 3 kelvin, which outputs tailored microwave bursts to drive silicon quantum bits cooled to 20 millikelvin. We first benchmark the control chip and find an electrical performance consistent with qubit operations of 99.99 per cent fidelity, assuming ideal qubits. Next, we use it to coherently control actual qubits encoded in the spin of single electrons confined in silicon quantum dots and find that the cryogenic control chip achieves the same fidelity as commercial instruments at room temperature. Furthermore, we demonstrate the capabilities of the control chip by programming a number of benchmarking protocols, as well as the Deutsch–Josza algorithm, on a two-qubit quantum processor. These results open up the way towards a fully integrated, scalable silicon-based quantum computer.
As a benchmark of performance, we use the cryo-controller to coherently control a two-qubit quantum processor. The quantum processor is made of a double quantum dot (DQD) electrostatically confined in an undoped $^{30}$Si/3%SiGe heterostructure. By tuning the voltage on the plunger gates LP and RP, two single electrons are locally accumulated underneath each gate, shown in blue and red in the scanning electron microscope (SEM) image in Fig. 1a. By applying an external magnetic field of 380 mT, combined with the longitudinal magnetic field induced by a micro-magnet on top of the DQD (see Extended Data Fig. 7), we can encode the qubit states into the Zeeman split states of the two electrons, where spin up is used as $|1\rangle$ and spin down as $|0\rangle$. The resonance frequencies of qubit 1 (Q$_1$; underneath gate LP) and qubit 2 (Q$_2$; underneath gate RP) are 13.62 GHz and 13.51 GHz, respectively. Rotations around the $x$ and $y$ axes are implemented by sending microwave bursts, with the microwave phase controlling the rotation axis; for example, an in-phase (quadrature) microwave burst implements a rotation around $\hat{x}$ ($\hat{y}$). The microwave bursts are applied to gate MW, which drives an electric–dipole spin resonance enabled by the transverse magnetic field gradient from the micro-magnet, whereas rotation around the $z$ axis (phase control) is achieved by changing the reference phase in the cryo-controller, which adds a phase shift to all the subsequent bursts. The two-qubit interaction is mediated by the exchange coupling ($J$) between the two spins, controlled by gate T. Its effect here is to shift the anti-parallel spin states down in energy. As a result, the resonance frequency of each qubit now depends on the state of the other qubit, allowing conditional operations on each qubit via narrow-band microwave bursts (Fig. 1b). The corresponding four different frequencies can be individually addressed using frequency multiplexing. Both qubits are read out in single-shot mode (see Methods).

Figure 2 shows the system-level architecture of one transmitter module (TX) in the cryo-controller, which consists of a digital signal-generation unit with an analogue/radiofrequency (RF) front end. At the core of the digital signal generation, a numerically controlled oscillator (NCO) outputs a sequence of bit strings every clock period. This bit string encodes a phase that is intended to track the reference phase of one particular qubit. The output of 16 NCOs is multiplexed...
A domain using 1 GS s⁻¹ (GS, 10⁹ samples) 10-bit current-steering range allows the control of various solid-state qubits, such as spin qubits connecting to the qubits. Such a wide frequency and output power range allows the main output tone, LO rejection ratio (LOR) and SFDR limited by the image tone.

The purity of the generated signal can be quantified using the output signal spectrum shown in Fig. 2b. The generated signal has an SFDR of 46 dB at 13.54 GHz in a 1-GHz bandwidth, excluding the residual LO leakage (see Extended Data Fig. 5 for a two-tone test). The noise floor is flat across the 1-GHz bandwidth, and the cryo-controller leaves the electron temperature of the quantum device unaffected (see Extended Data Fig. 8). The SNR is 48 dB when integrating over 25 MHz, corresponding to the targeted maximum qubit Rabi frequency. Along with the low quantization noise and frequency noise, the output signal quality is predicted to achieve a single-qubit gate fidelity of 99.99%, assuming ideal qubits. The amplitude and phase modulation capabilities of the controller allow the chip to generate arbitrary waveforms to precisely shape the spectral content of the pulse used to manipulate the qubits, as shown in Fig. 2c. In illustration, Fig. 2d shows the response of Q₂ to a microwave burst with a rectangular envelope versus a Gaussian one, both calibrated to invert the qubit state when the drive is on-resonance with the qubit.

Next, we test the functionality of the cryo-controller for controlling uncoupled qubits. The LO frequency is set to 13.54 GHz, Q₁ is then offset from the LO by 24 MHz and Q₂ by −90 MHz. The qubit resonances are found by sweeping one single-sideband tone generated by one NCO (Fig. 3a), using the 22-bit FTW. Then, we use one NCO from each bank to generate two tones on resonance with the two qubits and drive both calibrated to invert the qubit state when the drive is on-resonance with the qubit.
Fig. 3 | Frequency-multiplexed qubit control and fidelity benchmarks with the cryo-controller. a, Spectra showing the qubit resonances. Inset, SEM image indicating the positions of the qubits. b, Frequency-multiplexed control producing simultaneous Rabi oscillations of Q, (left) and Q, (right). The decay arises mainly from the residual coupling between the two qubits (see Extended Data Fig. 9 for Rabi oscillations in individual driving mode). c, (σ) of Q, measured after an AllXY sequence consisting of 21 different pairs of gates, each listed vertically on the X-axis. The output power is calibrated to achieve a Rabi frequency of about 1 MHz (the same applies to the QST and RB experiments). The visibility is normalized by removing the readout error (see Methods). d, Trajectory of the state of Q, under an X gate reconstructed by QST. Orange data points indicate the qubit state after incrementing microwave burst times. e, Randomized benchmarking of Q, performed by the cryo-controller and the RT setup. We offset the orange data points by ~0.05 along the Y axis to facilitate comparison of the two traces.

The pulses for single-qubit rotations are precisely calibrated using the AllXY sequence35. In the AllXY experiment, 21 different pairs of gates from the set \{I, X, Y, Y\}2 are applied to a qubit initialized to |0⟩. Here I is the identity operation, X and Y are π/2 rotations around the X and Y axis, respectively, and X2 and Y2 are π rotations. The final-state measurement of (σ) takes values from [−1, 0, +1] under perfect operation (shown as the grey shaded areas in Fig. 3c). Any miscalibration in the amplitude, frequency or phase of the pulse results in deviations from the ideal outcome (hatched bars in Fig. 3c). In addition, we reconstruct the trajectory of an X gate by performing quantum state tomography (QST)36 at incremental burst times of a rectangular microwave signal (Fig. 3d), which shows an average state fidelity of 97.92%. Here the infidelity comes from the error during the operation, as well as the errors in the initialization and readout of the qubit (see Methods). The QST results indicate that the single-qubit gate set is well calibrated, offering a good starting point for benchmarking the gate fidelity.

The gate fidelity is a crucial metric used to express the performance of a quantum processor and its classical controller. We use single-qubit randomized benchmarking (RB)37,38 to compare the performance of the cryo-controller with the conventional RT setup, which consists of an arbitrary waveform generator (Tektronix S014C) and a vector signal generator (Keysight E8267D). A programmable mechanical microwave switch placed at the 3-K plate allows us to conveniently alternate between the cryo-controller and the RT setup. In the RB experiment, sequences of increasing numbers of randomly selected Clifford operations are applied to the qubit (Q), followed by a final Clifford operation that returns the qubit to its initial state in the ideal case. For each data point in Fig. 3e, 32 different sequences are randomly sampled, and each is repeated 200 times. Envelopes of all gates to be used are uploaded to the envelope memory and saved as instructions. The random sequences are constructed by updating the instruction list. The instructions in the list are executed sequentially after an external trigger is received via the serial peripheral interface (SPI) in Fig. 2a. Exactly the same random sequences are used in an RB experiment using the RT setup. We find an average single-qubit gate fidelity of 99.71 ± 0.03% with the RT setup and 99.69 ± 0.02% with the cryo-controller (see Methods; all uncertainties are one standard deviation). The fidelities are consistently identical within the error bars and well above the threshold for fault tolerance39, with the infidelity limited by the qubit. These experiments demonstrate the high quality of the signal from the cryo-controller, as well as its capability of generating complex sequences.

To further test the programmability of the cryo-controller, we use it to implement two-qubit logic in the quantum processor (Fig. 4a). Taking advantage of the frequency shift of each qubit being conditional on the state of the other qubit (Fig. 1b), we use controlled-rotation (CROT) gates as the native two-qubit gates. These are achieved by frequency-selective addressing40, thus demanding two NCOs per qubit (see Methods). A π rotation at the higher or lower frequency implements the canonical controlled NOT (CNOT) gate or the zero-controlled NOT (Z-CNOT) gate, respectively, up to a single-qubit π/2 rotation on the control qubit. Because of cross-talk, an additional phase correction in the form of a π/2 rotation is needed. All π/2 rotations are implemented by updating the reference phase of the NCO (see Extended Data Fig. 3). Single-qubit gates are implemented by addressing both frequencies of the same qubit sequentially. Making use of four NCOs, we program the cryo-controller to run the two-qubit Deutsch–Josza algorithm, which determines whether a function gives constant or balanced outcomes41. The two constant (balanced) functions that map one input bit on one output bit are implemented by the CNOT and Z-CNOT (Y and X2) operations. Here, we choose Q to be the output qubit and Q, to be the input qubit. Fig. 4b shows the pulse sequence and the measurement results, where the constant (balanced) functions lead to a high probability of 78%–80% (79%–82%) for

| Article

| Number of Clifford operations | 0 | 20 | 40 | 60 |
|------------------------------|---|----|----|----|
| Spin-up probability          | 0.5 | 0.6 | 0.7 | 0.8 |
| Experiment                   | ⊙ | ⊙ | ⊙ | ⊙ |
| Perfect pulses               | ⊙ | ⊙ | ⊙ | ⊙ |
| Spin-up probability          | 0.5 | 0.6 | 0.7 | 0.8 |
| Experiment                   | ⊙ | ⊙ | ⊙ | ⊙ |
| Perfect pulses               | ⊙ | ⊙ | ⊙ | ⊙ |
| Spin-up probability          | 0.5 | 0.6 | 0.7 | 0.8 |
| Experiment                   | ⊙ | ⊙ | ⊙ | ⊙ |
| Perfect pulses               | ⊙ | ⊙ | ⊙ | ⊙ |

| Sideband frequency (MHz)     | 0 12345–9 | 0.0 | 0.5 | 0.6 |
|-------------------------------|------------|----|----|----|
| Spin-up probability          | 0.2 | 0.3 | 0.4 | 0.5 |
| Experiment                   | ⊙ | ⊙ | ⊙ | ⊙ |
| Perfect pulses               | ⊙ | ⊙ | ⊙ | ⊙ |
| Spin-up probability          | 0.2 | 0.3 | 0.4 | 0.5 |
| Experiment                   | ⊙ | ⊙ | ⊙ | ⊙ |
| Perfect pulses               | ⊙ | ⊙ | ⊙ | ⊙ |
| Spin-up probability          | 0.2 | 0.3 | 0.4 | 0.5 |
| Experiment                   | ⊙ | ⊙ | ⊙ | ⊙ |
| Perfect pulses               | ⊙ | ⊙ | ⊙ | ⊙ |
| Spin-up probability          | 0.2 | 0.3 | 0.4 | 0.5 |
| Experiment                   | ⊙ | ⊙ | ⊙ | ⊙ |
| Perfect pulses               | ⊙ | ⊙ | ⊙ | ⊙ |
measuring the data qubit as $|1\rangle$ ($|0\rangle$), as expected. This experiment highlights the ability to program the cryo-controller with arbitrary sequences of operations.

The cryo-controller allows for much more complex sequences, containing up to 2,048 instructions for each of the four transmitters. Each instruction defines a microwave burst at one of 32 independent frequencies, with an amplitude and phase profile that can be arbitrarily shaped. The cryo-controller can be conveniently embedded in existing micro-architectures and programmed via standard QASM variants. This quantum–classical architecture can thus be directly applied to multi-qubit algorithms and noisy intermediate-scale quantum devices.

The versatile programmability, combined with a signal quality allowing up to 99.99% gate fidelities, a footprint of just 4 mm², a power consumption of 384 mW, the ability to integrate multiple transmitters on one die, and operation at 3 K demonstrate the potential of the quantum processor to address key challenges in building a large-scale quantum computer. Optimized design of cryogenic CMOS circuits—such as the use of a narrower frequency band—can substantially reduce the power consumption (see Methods) and make it possible to work at 1 K or even lower temperatures. Furthermore, FinFET quantum dots that are fully compatible with CMOS processing and increased operating temperatures (about 1 K) of spin qubits show only a modest reduction in coherence times. These advances imply that it may be possible to fully integrate the quantum processor with the classical controller on chip or by flip-chip technology, lifting a major roadblock in scaling.

Online content
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Fig. 4 | Programming a quantum processor with the cryo-controller.
(a) Two-qubit logic with the cryo-controller. The middle panel shows the spectra of two qubits obtained using the cryo-controller with the exchange coupling ($J$) between the qubits turned on. Selective excitation of each of the four resonances can be used for implementing various two-qubit CROT gates, shown in the upper panel. The lower panels (shared Y-axis labels) show the Rabi oscillations at each frequency. (b) Pulse sequences of the Deutsch–Jozsa algorithm programmed into the cryo-controller (top) and measured probabilities of the output qubit state ($Q_1$) after running the algorithm (bottom) for constant or balanced functions, implemented through the unitary operation $U_f$. A constant function is composed of either a CNOT or a $Z$-CNOT gate, which consists of a CROT gate on $Q_2$ and a phase correction on $Q_1$ (not plotted). Only the lower frequency (green branch, $Z$-CROT) is used for the $\neg Y$ and $\neg Z$ gates on $Q_2$, because $Q_1$ (ideally) starts from and ends up in (0). Error bars are standard deviations of the measured probability data. The visibility of $Q_2$ is normalized by removing the readout error. Empirically, we attribute the remaining errors mostly to charge noise in the presence of a finite $f$ (see Methods).

1. Van Meter, R. & Horsman, C. A blueprint for building a quantum computer. Commun. ACM 56, 84–93 (2013).
2. Pillarisetty, R. et al. Qubit device integration using advanced semiconductor manufacturing process technology. In 2018 IEEE International Electron Devices Meeting 6.3.1–6.3.4 (IEEE, 2018).
3. Vandersypen, L. M. K. et al. Interfacing spin qubits in quantum dots and donors—hot, dense, and coherent. npj Quantum Inf. 3, 34 (2017).
4. Patra, B. et al. Cryo-CMOS circuits and systems for quantum computing applications. IEEE J. Solid-State Circuits 53, 309–321 (2018).
5. Zajac, D. M. et al. Resonantly driven CNOT gate for electron spins. Science 359, 439–442 (2018).
6. Huang, W. et al. Fidelity benchmarks for two-qubit gates in silicon. Nature 569, 532–536 (2019).
7. Deutsch, D. & Jozsa, R. Rapid solution of problems by quantum computation. Proc. R. Soc. Lond. A 439, 553–558 (1993).
8. Arute, F. et al. Quantum supremacy using a programmable superconducting processor. Nature 574, 505–510 (2019).
9. Barnd, J. C. et al. Design and characterization of a 28-nm bulk-CMOS cryogenic quantum controller dissipating less than 2 mW at 3 K. IEEE J. Solid-State Circuits 54, 3043–3060 (2019).
10. Patra, B. et al. A scalable cryo-CMOS 2- to 20GHz digitally intensive controller for 4 × 32 frequency multiplexed spin qubits/transmons in 22nm FinFET technology for quantum computers. In 2020 IEEE International Solid-State Circuits Conference 304–306 (IEEE, 2020).
11. Le Guevel, L. et al. A 110mK 295μW 28nm FSOSi CMOS quantum integrated circuit with a 2.8 GHz excitation and nA current sensing of an on-chip double quantum dot. In 2020 IEEE International Solid-State Circuits Conference 306–308 (IEEE, 2020).
12. Bardin, J. C. et al. Cryogenic characterization of 22-nm FSOSi CMOS technology for quantum computing ICs. IEEE Electron. Device Lett. 40, 127–130 (2019).
13. Esfahliyan, A. et al. A fully integrated DAC for CMOS-position-based charge qubits with single-electron detector loopback testing. IEEE Solid-State Circuits Lett. 3, 354–357 (2020).
14. El-Bayoumy, S. R. et al. Characterization of SOS-CMOS FETs at low temperatures for the design of integrated circuits for quantum bit control and readout. IEEE Trans. Electron Dev. 57, 539–547 (2010).
18. Mukhanov, O. et al. Scalable quantum computing infrastructure based on superconducting electronics. In 2019 IEEE International Electron Devices Meeting 31.2.1–31.2.4 (IEEE, 2019).
19. Xu, Y. et al. On-chip integration of Si/SiGe-based quantum dots and switched-capacitor circuits. Appl. Phys. Lett. 117, 144002 (2020).
20. Batey, G., Matthews, A. J. & Patton, M. A new ultralow-temperature cryogen-free experimental platform. J. Phys. Conf. Ser. 568, 032014 (2014).
21. Green, M. A. The cost of coolers for cooling superconducting devices at temperatures at 4.2 K, 20 K, 40 K and 77 K. In IOP-Conference Series: Materials Science and Engineering Vol. 101, 012001 (IOP, 2015).
22. Petit, L. et al. Universal quantum logic in hot silicon qubits. Nature 580, 355–359 (2020).
23. Yang, C. H. et al. Operation of a silicon quantum processor unit cell above one kelvin. Nature 580, 350–354 (2020).
24. Urdampilleta, M. et al. Gate-based high fidelity spin readout in a CMOS device. Nat. Nanotechnol. 14, 737–741 (2019).
25. van Dijk, J. P. G. et al. Designing a DDS-based SoC for high-fidelity multi-qubit control. IEEE Trans. Circuits Syst. I 67, 5380–5393 (2020).
26. Beckers, A., Jazaeri, F. & Enz, C. Characterization and modeling of 28-nm bulk CMOS technology down to 4.2 K. IEEE J. Electr. Dev. Soc. 6, 1007–1018 (2018).
27. Hart, P. A. T., Babaie, M., Charbon, E., Vladimirescu, A. & Sebastiano, F. Subthreshold mismatch in nanometer CMOS at cryogenic temperatures. IEEE J. Electr. Dev. Soc. 8, 797–806 (2020).
28. Patra, B. et al. Characterization and analysis of on-chip microwave passive components at cryogenic temperatures. IEEE J. Electr. Dev. Soc. 8, 448–456 (2020).
29. Pioro-Ladrière, M. et al. Electrically driven single-electron spin resonance in a slanting Zeeman field. Nat. Phys. 4, 776–779 (2008).
30. Vandersypen, L. M. K. & Chuang, I. L. NMR techniques for quantum control and computation. Rev. Mod. Phys. 76, 1037–1068 (2005).
31. Petta, J. R. et al. Coherent manipulation of coupled electron spins in semiconductor quantum dots. Science 309, 2180–2184 (2005).
32. Meunier, T., Calado, V. E. & Vandersypen, L. M. K. Efficient controlled-phase gate for single-spin qubits in quantum dots. Phys. Rev. B 83, 121403 (2011).
33. Xue, X. et al. Repetitive quantum nondemolition measurement and soft decoding of a silicon spin qubit. Phys. Rev. X 10, 021006 (2020).
34. Saul, P. H. & Mudd, M. S. J. A direct digital synthesizer with 100-MHz output capability. IEEE J. Solid-State Circuits 23, 819–821 (1988).
35. Reed, M. Entanglement and Quantum Error Correction with Superconducting Qubits. PhD Thesis, Yale Univ. (2013).
36. Altepeter, J. B., Jeffrey, E. R. & Kwiat, P. G. Photonic state tomography. Adv. At. Mol. Opt. Phys. 52, 105–159 (2005).
37. Knill, E. et al. Randomized benchmarking of quantum gates. Phys. Rev. A 77, 012307 (2008).
38. Magesan, E., Gambetta, J. M. & Emerson, J. Characterizing quantum gates via randomized benchmarking. Phys. Rev. A 85, 042311 (2012).
39. Fowler, A. G., Mananti, M., Martinis, J. M. & Cleland, A. N. Surface codes: towards practical large-scale quantum computation. Phys. Rev. A 86, 032324 (2012).
40. Svore, K. M., Aho, A. V., Cross, A. W., Chuang, I. & Markov, I. L. A layered software architecture for quantum computing design tools. Computer 39, 74–83 (2006).
41. Preskill, J. Quantum computing in the NISQ era and beyond. Quantum 2, 79 (2018).
42. Boter, J. M. et al. A sparse spin qubit array with integrated control electronics. In 2019 IEEE International Electron Devices Meeting 31.4.1–31.4.4 (IEEE, 2019).

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Methods

Programming the cryo-controller
The setup (Extended Data Fig. 1) contains a field-programmable gate array (FPGA) that configures the cryo-controller (for example, FTW), programs the various memories inside the cryo-controller (for example, envelope memories, instruction tables and instruction lists) and controls the start of the execution of the instruction list. The FPGA is connected to the host PC, which sends the data that need to be uploaded to the cryo-controller over the SPI. The instruction list integrated in the cryo-controller does not support classical instructions that allow for, for example, branching or wait statements, as required for performing certain qubit experiments and for synchronization with other equipment. Therefore, switching between different instruction lists and synchronization with the rest of the equipment are controlled by two trigger lines from the AWG to the FPGA. The application of the execute trigger starts the execution of the instruction list that is programmed in the cryo-controller for performing repeated measurements. The application of the sweep trigger loads the next instruction list from the static random-access memory (SRAM) of the FPGA into the cryo-controller’s instruction list.

Power budget
All memory blocks except NCO phase-update registers (to perform phase corrections; ‘Z-Corr.’ in Extended Data Fig. 3a) are implemented using SRAM. The high power consumption of the digital circuitry of the cryo-controller (Extended Data Fig. 4) is due to the lack of clock gating in registers, thus causing them to operate continuously instead of only during the read/write cycle. This could easily be reduced by further optimizations (for example, by replacing more registers with SRAM memory and by adding clock gating) that were not included in the first-generation cryo-controller. On the basis of the Cadence simulation with clock-gating, the power consumption of the digital circuitry should be lower than 40 mW instead of 330 mW in the current design. Migrating to a finer technology node would result in further substantial power savings.

Moreover, this chip was designed to address both transmons and spin qubits, and hence an ultrawide output frequency range was supported, that is, 2–20 GHz with an LO frequency of 2.5–14.5 GHz, using both fundamental and third-harmonic outputs (see Extended Data Fig. 3b). Once the qubit frequency is fixed within a range of a few gigahertz, the power consumption of the analogue circuitry can be substantially reduced to limit the power consumption to - 20 mW instead of 54 mW. In the current architecture (Extended Data Fig. 3 and ref. 25), such power savings can be achieved by: (1) eliminating the output drivers and compensating the gain loss by increasing the matching network impedance transformation, as allowed by the reduced frequency range, which also results in a higher mixer load and consequently lower VGA bias current; (2) replacing the folded current topology of the anti-aliasing filter with a stacked topology; (3) replacing the active balun before the LO drivers with a passive matching network. Further power savings could be achieved by architecture improvements, for example, by replacing the gm-C filter with a passive filter, thus eliminating the power consumption of the filter. Moreover, the integration of a phase-locked loop can eliminate I/Q active baluns completely.

Si/3SiGe heterostructure
The 28Si/3SiGe heterostructure is grown on a 100-nm n-type Si(001) substrate using an Epsilon 200 (ASMI) reduced-pressure chemical vapour deposition reactor equipped with a 28SiH4 gas cylinder (1% dilution in H2) for the growth of isotopically enriched 28Si. The 28SiH4 gas is obtained by reducing 28SiF4 with a residual 28Si concentration of 0.08%, as described in ref. 25. Starting from the Si substrate, the layer sequence comprises a 900-nm linearly graded 28Si0.7Ge0.3 layer (Ge concentration varied from 0 to 0.3), followed by a 300-nm strain-relaxed 28Si0.7Ge0.3 buffer layer, an 8-nm tensile strained 28Si quantum well, a 30-nm Si0.7Ge0.3 barrier and a 1-nm sacrificial Si cap. These undoped 28Si/3SiGe heterostructures are insulating at low temperature and support via gating the accumulation of a two-dimensional electron gas with transport mobility of up to 10^6 cm^2 V^{-1} s^{-1} at 55 mK (ref. 44). Extended Data Fig. 7 shows concentration profiles obtained by secondary ion mass spectroscopy (SIMS) of a control 28Si/3SiGe heterostructure. This control 28Si/3SiGe heterostructure has an increased quantum well thickness of 20 nm, which facilitates the investigation of the chemical composition therein by reducing the impact of the knock-on SIMS artefact. The concentration profiles of isotopes of Ge, 30Si, 29Si and 28Si show a high-purity and homogeneous 28Si quantum well. The residual concentration of non-zero-spin nuclei 31Si is reduced from 3.29% in the Si0.7Ge0.3 buffer and barrier to 0.08% in the quantum well, demonstrating that the 28SiH4 precursor purity is maintained during the heterostructure deposition process. As a result, we achieve a suitable quantum grade environment for the qubits in which decoherence due to hyperfine interaction is minimized. Furthermore, the concentration of common background contaminants C and O is below the detection limit of around 3 × 10^16 cm^{-3} and 1 × 10^17 cm^{-3}, respectively, reducing scattering sources in the qubit-surrounding environment that can be sources of charge noise.

Quantum dot device fabrication
On top of the heterostructure, a 7-nm-thick AlOx layer is deposited using atomic-layer deposition, followed by a 20-nm Al metal film, which is patterned using electron beam lithography in order to define the first gate layer, which shapes the potential landscape. Next, another 7-nm AlOx layer is deposited, followed by a 70-nm Al layer that uniformly covers the quantum dot area. Finally, a 200-nm Co film is deposited and patterned into a micro-magnet (see Extended Data Fig. 7).

Qubit readout
The readout scheme is described in Extended Data Fig. 6. After each operation sequence, Q2 is measured by spin-selective tunnelling to the electron reservoir, where a spin-up (|1⟩) electron can tunnel out and a spin-down (|0⟩) electron is blocked from tunnelling out. Such a spin-to-charge conversion changes the charge occupancy in the quantum dot, conditional on the spin state. This in turn changes the current signal in an adjacent capacitively coupled single-electron transistor (SET). Single-shot readout of the qubit state can be done by thresholding the current signal through the SET. The post-measurement state in this readout protocol is the |0⟩ state, serving as reinitialization. Q0 is tuned to be only weakly coupled to the SET, which serves as the electron reservoir for Q2. This is to minimize the back-action from the SET, but also makes it less efficient to readout Q0 by spin-selective tunnelling to the SET. Therefore, with Q2, reinitialized, a CROT gate is applied to map the state of Q2 onto Q0. Then, Q3 is read out by measuring Q2 again. The readout fidelity of Q0 is mainly limited by the thermal broadening of the electron reservoir, and the readout fidelity of Q2 is limited by both the error in the CROT gate and in the readout of Q2. Thus, the readout visibility of Q0 is lower than that of Q2. Alternatively, Q2 could be read out by shutting the electron to the location of Q2 after emptying the dot hosting Q2. We here chose to map the state of Q2 onto that of Q0 using a CROT gate, because this reduces charging effects on the bias tees on the printed circuit board (PCB). The CROT gate used here is also executed by the cryo-controller.

Readout error removal
In the AIIXY experiments and in the implementation of the Deutsch–Jozsa algorithm, the readout probabilities of Q2 are normalized with the calibrated readout fidelities (F_{Q0}, F_{Q2}). After preparing Q0 in |0⟩, F_{Q0} can be calibrated directly through the measured spin-down probability, and F_{Q2} is calibrated through the measured spin-up probability after a spin-flip operation (the spin-flip fidelity is above 9%). On the basis of the measured state probabilities in the AIIXY and Deutsch–Jozsa
experiments, $P^M = \left( P^{M}_0, P^{M}_1 \right)$, the actual state probabilities ($P_0$, $P_1$) can be reconstructed by $P = F^{-1} P^M$, where

$$F = \begin{pmatrix} F_0 & 1 - F_1 \\ 1 - F_0 & F_1 \end{pmatrix}.$$ 

(1)

**Error sources**

In the simultaneous Rabi oscillation experiment (Fig. 3b), we attribute the visible decays in both curves to the residual exchange coupling between the two qubits. Simultaneous Rabi oscillations recorded (in this case, using the RT setup) over larger numbers of oscillations show beating patterns. These patterns are well reproduced by numerical models of the spin evolution in the presence of a finite residual exchange coupling. Such a beating effect looks like a decay in the beginning. It is absent in the individually driven Rabi oscillation (Extended Data Fig. 9). In the two-qubit experiments shown in Fig. 4, the decay in the controlled-rotation Rabi oscillations and the finite visibilities in the Deutsch–Jozsa algorithm are largely attributed to charge noise. With the exchange coupling turned on, as needed for two-qubit gates, the energy levels are much more sensitive to charge noise.

**Quantum state tomography**

In the QST experiment, the qubit state is measured by projecting it onto the $\{ -\hat{z}, +\hat{x}, -\hat{y}, +\hat{z} \}$ axes. The projection on the $-\hat{z}$ axis is measured by direct readout of the spin state, whereas the projections on the other axes are measured by applying an $X$, $Y$ or $X^2$ gate, which are calibrated by the AllXY experiment, before the readout. The trajectory of the qubit state in the course of an $X^2$ gate can be reconstructed by performing QST at incremental burst times of a rectangular microwave signal (Fig. 3c), with each measurement repeated 1,000 times. To visualize the qubit state in the Bloch sphere, we remove the readout error from the data. Given that error removal can lead to unphysical states, such as data points outside the Bloch sphere, a maximum-likelihood estimation is implemented to find the closest physical state of the qubit. From residual state preparation and measurement error after imperfect readout error removal.

**Data availability**

Data supporting this work are available at https://doi.org/10.5281/zenodo.4061970.

**Code availability**

The codes used for data acquisition and processing are from the open-source Python packages QCoDeS (available at https://github.com/QCoDeS/Qcodes), QTT (available at https://github.com/QuTech-Delft/qt) and PycQED (available at https://github.com/DiCarloLab-Delft/PycQED_py3).

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**Author contributions** X.X., B.P. and J.P.G.v.D. performed the experiment. N.S. fabricated the quantum device. A.S., B.P.W. and G.S. designed, grew and characterized the Si/SiGe heterostructure. A.C. contributed to the preparation of the experiment. X.X. and B.P. analysed the data presented in the main manuscript. F. Sebastiani, M.B., S.P., E.C. and L.M.K.V. conceived and supervised the project. X.X., B.P. and L.M.K.V. wrote the manuscript with input from all authors.

**Competing interests** The authors declare no competing interests.

**Additional information**

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**Extended Data Fig. 1 | Experiment setup.** The quantum dot device is wire-bonded onto a PCB placed on a cold finger attached to the mixing chamber plate (~20 mK) of a dilution refrigerator (Bluefors XLD). Voltage pulses onto gates RP and LP are generated by the AWG at RT, and go through a low-pass filter (Minicircuits) and attenuators before reaching the device. These pulses are used to control the electrochemical potentials of the quantum dots and load/unload electrons from/to the electron reservoir (see Extended Data Fig. 6). A programmable mechanical switch at 3 K is used to connect gate MW either to a vector signal generator (VSG) at RT or to the cryo-controller at 3 K (represented as two boxes next to the switch) through a 12–14 GHz band-pass filter to filter out wide-band noise. The mechanical switch can also be configured to send the output signals from the cryo-controller to the oscilloscope and the spectrum analyser at RT for electrical characterization in the time and frequency domains. The cryo-controller is programmed via an FPGA to generate the microwave bursts using an external LO signal and a clock (CLK) signal from a microwave signal generator (MSG) at RT. The SET next to the quantum dots is voltage-biased, and the current signal ($I_{SET}$) through it is converted to a voltage signal through a transimpedance amplifier and digitized by a digitizer card after an analogue low-pass filter employed to remove out-of-band (~10 kHz) noise. $I_{SET}$ is sensitive to the charge occupation of the quantum dots, allowing binary single-shot readout of the qubit states via spin-to-charge conversion (Extended Data Fig. 6).
Extended Data Fig. 2 | Dilution refrigerator setup. a, Location of the cryo-controller and the quantum device inside the dilution refrigerator (left). Top and bottom views of the 3-K plate, showing the mounted chip enclosure and the fixed holder for the enclosure, respectively (right). b, Top view of the gold-plated annealed copper enclosure (without the lid), which is used to mount and thermalize the cryo-controller. c, Ball-grid array (BGA 324) package hosting the cryo-controller chip with on-package decoupling capacitors (shown as a white box in b). d, The Wilkinson power divider (WPD) splits the input LO power into two equal paths with half power in each, implemented on a PCB. Discrete I/Q hybrids that create the in-phase and quadrature-phase components of the input LO are wire-bonded on the PCB for LO distribution between the different transmitters inside the cryo-controller (shown as a red box in b).
Extended Data Fig. 3 | Detailed cryo-controller schematic. a, Detailed representation of the digital circuitry. b, Detailed system-level schematic of the analogue circuitry inside the controller.
Extended Data Fig. 4 | Power consumption and self-heating of the cryo-controller. 

a, Power-consumption pie chart showing the contribution of the digital and analogue circuits in the cryo-controller. A breakdown of the power consumption of individual circuit blocks is shown for the analogue circuits. The digital circuits use a 0.7-V supply and the analogue circuits use a 1-V supply.

b, Chip micrograph showing the on-chip bumps used as inputs/outputs. The locations of on-chip temperature-sensing diodes and the analogue and digital circuitry (in TX0) are highlighted.

c, On-chip and 3-K plate temperature, measured using different sensors, versus the power consumption of TX0, as reported in ref. 13. The power consumption is varied by changing the clock frequency of the chip. The nominal operating point for the work presented here and the corresponding temperatures are highlighted with a dashed vertical line. All the other transmitters (TX1, TX2, TX3) are switched off in this measurement.
Extended Data Fig. 5 | Detailed electrical characterization of the cryo-controller. 

**a** | Schematic of the output driver (complete version in Extended Data Fig. 3) showing the two different RF outputs, which use the same external LO to generate two different frequencies—that is, a 1-GHz band around the LO frequency \( f_{\text{LO}} \) or a 1-GHz band around \( 3 \times f_{\text{LO}} \)—by selecting the ‘RF-Low’ or ‘RF-High’ path, respectively. RF-High uses the third harmonic output of the mixer to generate the tone around \( 3 \times f_{\text{LO}} \).

**b** | Peak output power versus frequency generated using the RF-Low and RF-High path, respectively, as reported in ref. 13. The output power can be lowered by up to 40 dB below the peak power in the entire frequency range; for example, at 6 GHz the amplitude range is from −56 dBm to −16 dBm.

**c** | Two-tone output spectrum of the cryo-controller used in the simultaneous Rabi oscillation experiment.

**d** | SNR and SFDR of the cryo-controller at various NCO frequencies around 13.54 GHz.
Extended Data Fig. 6 | Pulsing scheme used in qubit experiments.

a, Charge-stability diagram of the DQD system, showing the differential current signal ($dI_{SET}/dV_{RP}$) and charge occupation ($M, N$) (where $M$ denotes the number of electrons in the dot below LP and $N$ represents the number of electrons in the dot below RP) as a function of the voltages applied to gates LP ($V_{LP}$) and RP ($V_{RP}$). The three main stages of a typical pulse sequence are marked by the numbered circles. The gate voltages of stage 3 vary between different experiments: in the experiments with exchange coupling turned on, owing to the cross-capacitance between the barrier (gate T) and the plungers (gates RP and LP), the LP and RP voltages differ from those in the experiments without exchange coupling by ~15 mV. This allows a spin-down electron to tunnel into the dot but forbids spin-up electrons from tunnelling in—a mechanism called spin-selective tunnelling. During the qubit operations, the system is pulsed to the middle of the (1, 1) region (stage 3), so both electrons are well confined inside the DQD. The barrier (gate T) voltage is used to turn off the exchange coupling between the two spins in the operation of uncoupled qubits (all measurements in Fig. 3) and to turn on the coupling for two-qubit logic operations (all measurements in Fig. 4). After the operations, the Q2 state is read out via spin-selective tunnelling and reinitialized into the spin-down state (stage 2). The state of Q1 is read out by mapping its state onto Q2 via a two-qubit CROT gate (stage 3), followed by readout of Q2 again (stage 2).
Extended Data Fig. 7 | Magnetic field gradient. a, Wafer stack schematic with corresponding layer thicknesses. b, Depth concentration SIMS profile of $^{28}$Si (red), $^{29}$Si (blue), $^{30}$Si (purple), Ge (black), oxygen (green) and carbon (blue). The residual $^{29}$Si concentration in the quantum well is 0.08%, considerably reducing qubit decoherence due to hyperfine interaction. Both carbon and oxygen concentrations are below their respective detection limits of $3 \times 10^{16}$ cm$^{-3}$ and $1 \times 10^{17}$ cm$^{-3}$. c, Schematic showing the first and second Al gate layers in green and purple, respectively. A cobalt micro-magnet is located on top of the metallic gates (pink-shaded area). d, The micromagnet is magnetized by sweeping the external magnetic field (in the $\hat{z}$ direction) from 0 to 3 T and back to 380 mT. The magnetized micro-magnet provides an additional magnetic field (brown dashed lines) that has a longitudinal ($\hat{z}$) component with a field gradient along the double quantum dots. This longitudinal magnetic field gradient (light blue arrows) makes the Zeeman splittings (resonance frequencies) of the two qubits different by ≈110 MHz. Additionally, the micro-magnet also induces a transverse ($\hat{x}$) magnetic field gradient (green arrows). When a microwave pulse is sent to the device through gate MW, the wave functions of the electrons are oscillating in the $\hat{z}$ direction. If the microwave frequency is in resonance with the qubit frequency, the electron is subject to an oscillating magnetic field along the $\hat{x}$ direction, which induces electric-dipole spin resonance.
Extended Data Fig. 8 | Electron temperature measured at different configurations. a, b. SET current signal ($I_{\text{SET}}$) as a function of RP voltage ($V_{\text{RP}}$) measured at the charge transition between (1, 0) and (1, 1) when the quantum device is connected to the VSG (a) and to the cryo-controller (b) (at zero magnetic field). The electron temperatures are extracted by fitting the curves with the Fermi–Dirac distribution, with a lever arm of 0.172 eV V$^{-1}$. The measurements indicate that the output noise of the cryo-controller does not affect the electron temperature more than the noise from the RT setup reduced by 6 dB at the 3-K plate.
Extended Data Fig. 9 | Rabi oscillations of qubits individually driven by the cryo-controller. The output frequency of two NCOs are set to the frequencies of Q1 and Q2, respectively, but only one NCO is active each time. Using the same method as described in the main text, the Rabi oscillations of Q1 (a) and Q2 (b) are measured individually. Compared to the simultaneous Rabi oscillations shown in Fig. 3b, the decay is much slower in the individual driving experiments.