A dual-output hardening design of inverter chain for P-hit single-event transient pulse elimination

Changyong Liu\textsuperscript{1,a)}, Chunyu Peng\textsuperscript{1}, Zhiting Lin\textsuperscript{1}, Xiulong Wu\textsuperscript{1b)}, Ziyang Chen\textsuperscript{1}, Qiang Zhao\textsuperscript{1}, Xuan Li\textsuperscript{1}, Junning Chen\textsuperscript{1}, Xuan Zeng\textsuperscript{2}, and Xiangdong Hu\textsuperscript{3}

\textsuperscript{1} School of Electronics and Information Engineering, Anhui University, Hefei 230601, China
\textsuperscript{2} State Key Laboratory of ASIC & System, Department of Microelectronics, Fudan University, Shanghai 200433, China
\textsuperscript{3} Shanghai High Performance Integrated Circuit Design Center, Shanghai 200433, China
\textsuperscript{a)} liuchangyongcv@foxmail.com
\textsuperscript{b)} xiulong@ahu.edu.cn, Corresponding Author

Abstract: A dual-output design of inverter chain that is hardened against P-hit single-event transient (SET) is proposed in this paper. The output nodes of the proposed inverter chain are hardened by dual-output topological structure design and stacked PMOSs with isolation. The simulation results based on a 65 nm CMOS technology suggest that the proposed design can eliminate SET pulse significantly. In comparison with the conventional inverter chain and inverter chain using the source-isolation technique, the proposed design is capable of maintain the output steadily irrespective of whether an ion hits “0” or hits “1”, i.e., the struck node is at logic “0” or logic “1”. Besides, the SET pulse occurring at any stage of inverter chains with the proposed methodology will not disturb the final output, as long as it does not occur at the final stage.

Keywords: inverter chain, P-hit, single-event transient

Classification: Integrated circuits

References

[1] M. Glorieux, \textit{et al.}: “Detailed SET measurement and characterization of a 65 nm bulk technology,” IEEE Trans. Nucl. Sci. 64 (2017) 81 (DOI: 10.1109/TNS.2016.2637935).
[2] R. C. Baumann: “Soft errors in advanced semiconductor devices-part I: The three radiation sources,” IEEE Trans. Device Mater. Rel. 1 (2001) 17 (DOI: 10.1109/7298.946456).
[3] P. E. Dodd, \textit{et al.}: “Current and future challenges in radiation effects on CMOS electronics,” IEEE Trans. Nucl. Sci. 57 (2010) 1747 (DOI: 10.1109/TNS.2010.2042613).
[4] J. Chen, \textit{et al.}: “Novel layout technique for single-event transient mitigation
1 Introduction

With the CMOS technologies scaling down into nanometric feature sizes, the integrated circuits (ICs) employed in space environment are susceptible to the voltage and charge variation, which were caused by radiation effect [1, 2, 3]. It is
likely to induce soft errors. One of the key factors giving rise to soft errors is the SET owing to an ion that hits the sensitive region of circuits [1, 3]. In a case where the SET pulse width ($W_{SET}$) is wide enough, it is going to become a disturbed signal which is likely to result into an incorrect output.

Inverter chains are common in the ICs. Unfortunately, it has been proved that inverters are quite susceptible to SET [2, 4, 5, 6]. As revealed by the earlier experiments, the maximal SET occurs when an ion strikes PMOS not NMOS. That is owing to the fact that charge collection is enhanced by the parasitic bipolar junction transistor (BJT) in PMOS but not NMOS [4, 7].

Fig. 1(a) shows the schematic of the inverter chain with the use of conventional inverters. It has been proved that SETs occur when the particles hit at the drain of an off PMOS [7, 8, 9, 10, 11]. The source-isolation layout design methodology was proposed in [8]. It can be used in inverter to reduce $W_{SET}$ of P-hit significantly. Fig. 1(b) presents the schematic of the inverter chain using source-isolation technique. In the layout configuration of each stage inverter, the two serial PMOSs are isolated from each other by shallow trench isolation (STI).

Nevertheless, we observed that the source-isolation technique is only suitable for the PMOS at the OFF-state. As regards an ion striking on the PMOS at the ON-state, it will cause the output of the inverter to switch from high to low. As we know, when a heavy ion strikes at the drain of the P21 as shown in Fig. 1(b), a large number of electron-hole pairs will be generated along the ion track. Near the P-N junction that is caused by P+ deep well and N-well, the built-in electric field will drive holes to P-region and electrons to N-region. The electrons will be constrained by the N-well and give rise to the drop of N-well potential. The P-N junction that is caused by the drain of P21 and the N-well will drive the holes in the drain to the N-well. The potential of the drain of P21 will drop down to even logic “0”, if the energy of ion striking is large enough. Thereafter, the transient negative pulse is likely to propagate through the chain.

To solve the problems of P-hit SET of the inverter chains stated earlier, in this paper, we proposed a dual-output radiation hardened design of inverter chain for the mitigation of the P-hit SET no matter the PMOS is at the ON-state or at the OFF-state.
2 The proposed design of inverter chain

The schematic of the proposed design of inverter chain has been presented in Fig. 2. In every stage, the inverter has a pair of output nodes, i.e., the drain of the uppermost PMOS and the drain of the lowermost PMOS. The two output nodes connect to the gates of the PMOSs and NMOSs in the next stage inverter respectively. In Fig. 2, n1 is the input signal, n2 (the drain of P10) and n3 (the drain of P12) are a pair of output nodes of the first stage inverter. Node n2 connects to the gates of P20, P21 and P22, and node n3 connects to the gates of N20, N21, and N22. The rest can be done in the same manner, and n13 is the final output. Despite the fact that the proposed methodology suffers from area penalty, yet it is capable of substantially lowering the effect of SET on inverter chain. We make use of the second stage inverter as an example for the analysis of the SET immunity of the proposed design.

Case1-hit “0”: if the voltages of node n4 and node n5 in Fig. 2 are logic “0”, and the outputs of the third stage inverter are at high level. As regards the node n4, in a case where the drain of P20 is struck and a SET pulse occurs at the node n4, the voltage of n4 changes to logic “1”, which is likely to lead to the PMOSs in the third stage inverter to turn off. Nevertheless, since the voltage of n5 still stays at low level, the NMOSs in the third stage inverter will not be turned on. The output nodes of the third stage inverter will have no path to discharge, accordingly, the voltage will not decrease. The third stage to the final stage will output correctly. As regards the node n5, due to the stacked PMOSs, we make use of the STI for the isolation of P22 from P21, and the parasitic BJT will be broken. Together with that, N21 will be at the ON state, so the source of P22 and the drain of P21 will be discharged by N21. Accordingly, the bipolar effect will be lessened further. Therefore, the quantity of charge collected by the drain of P22 is lowered, which will mitigate the SET if the drain of P22 is struck by an ion. The logic level of n5 will not turn over. The outputs of the third stage to the final stage are going to be both correct and stable.

Case2-hit “1”: if the voltages of node n4 and node n5 are logic “1”, and the outputs of the third stage inverter are at low level. As regards the node n4, since the source of P20 is connected to the VDD and P20 is conducted, the logic level of n4 will be high stably after an ion striking at drain of P20. The outputs will not be
disturbed. As regards the node n5, as mentioned above, owing to the drawback of the source-isolation technique, the voltage of n5 will decrease if the drain of P22 is hit by an ion. We assume the LET value of striking ion is large enough to make the voltage of n5 change to low level, so the NMOSs of the third stage inverter will be turned off. Nevertheless, the voltage of n4 is still logic “1”, thus, the PMOSs of the third stage inverter stay at the OFF state. VDD can not charge the output nodes of the third stage inverter, and the voltages of the output nodes of the third stage will stay at a low level. Thus, the third stage to the final stage can achieve correct output.

The two outputs of each stage inverter are not susceptible to ion striking simultaneously. Therefore, at least one output node is at correct logic level after ion striking. And the worst state is that the PMOSs and the NMOSs of the next stage inverter are at the OFF state simultaneously. But the outputs of the next stage will not change immediately. The final output of the inverter chain will be stable. On the contrary, when a SET pulse occurs at output node of any stage after an ion striking, the final output of the conventional inverter chain and the inverter chain with the use of source-isolation technique will change. The proposed approach can eliminate the SET pulse thoroughly, so long as the pulse does not occur at the final stage.

3 Simulation setup

Three-dimensional mixed-mode TCAD simulation has been proven to be a useful means of investigating single-event effects (SEEs) in ICs [4, 9, 12, 13, 14, 15, 16, 17, 18, 19]. In this work, we have adopted a Sentaurus TCAD from Synopsys, using 65 nm CMOS technology. The W/L ratios of PMOS and NMOS are both 140 nm/65 nm. The TCAD models of MOSFETs that we used for simulations are calibrated to make the electrical characteristics be in line with the commercial 65 nm bulk CMOS process design kit (PDK). The TCAD model of PMOS has been presented in Fig. 3. The NMOS is also modeled similarly. The Id-Vd and Id-Vg curves of TCAD and PDK are shown in Fig. 4. Vd and Vg represent the voltage of the drain and gate, respectively, and Id means the current of the drain.

In the simulations, SETs were produced in six stages inverter chains of three structures mentioned above. As regards the three inverter chains, the MOSFETs in the second stage are modeled by a TCAD numerical model, and the other transistors are modeled as SPICE model. The layouts of PMOSs of the second stage inverter of inverter chain that makes use of source-isolation technique and the proposed design have been presented in Fig. 5. The ion strikes through the device

Fig. 3. TCAD model of PMOS.
on a $20 \times 20 \times 20 \mu m^3$ substrate normally, which has the LET value that is increased from $10 \text{MeV} \cdot \text{cm}^2/\text{mg}$ to $60 \text{MeV} \cdot \text{cm}^2/\text{mg}$ with an increment of $10 \text{MeV} \cdot \text{cm}^2/\text{mg}$. The LET value is kept constant along the heavy ion track. The length and the radius of the ion track are $10 \mu m$ and $0.05 \mu m$, respectively. We assume that the ion strikes at the center of the drain of PMOS and it strikes the surface of the structure normally. The striking time is set to 50 ps. The supply voltage of circuits is 1.2 V.

Fig. 4. Id-Vd and Id-Vg curves of PDK and TCAD.

4 Simulation results and discussion

4.1 Hits “0”

As the input $n_1$ is low, as regards the two existing and the proposed inverter chains, all the outputs of the first stage inverter (i.e., the inputs of the second stage inverter) are at high level, and all the outputs of the second stage inverter are at low level. It implies that the voltages of node $n_3$ in Fig. 1(a) and Fig. 1(b), node $n_4$ and node $n_5$ in Fig. 2 are at low level. When an ion strikes at the drain of PMOS of the second stage inverter vertically with the LET value of $30 \text{MeV} \cdot \text{cm}^2/\text{mg}$, the voltage curves of output nodes of the second and the final stages of the three inverter chains have been presented in Fig. 6 to Fig. 9.

Fig. 5. The layouts of PMOSs of the second stage inverter

Fig. 6. Output curves of the second stage and the final stage of the conventional inverter chain.
Fig. 6 shows the output curves of the second stage (which is \( n_3 \)) and the final stage (which is \( n_7 \)) of the conventional inverter chain. As evident to us, a SET pulse occurs immediately subsequent to an ion striking, and it propagates through the inverter chain. It is no doubt that the pulse will affect other circuits that connect with the final output of the inverter chain.

![Fig. 6. Output curves of the second stage and the final stage of the inverter chain (conventional).](image)

Fig. 7 shows the output curves of the second stage (which is \( n_3 \)) and the final stage (which is \( n_7 \)) of the inverter chain using source-isolation technique. In comparison with the conventional inverter chain, it can mitigate SET substantially. The voltage of the drain of struck PMOS is basically less than \( V_{DD}/2 \). The voltage variation does not disturb the signal of the final output.

![Fig. 7. Output curves of the second stage and the final stage of the inverter chain using source-isolation technique.](image)

Fig. 8 presents the output curves of the second stage and the final stage of the proposed technique when an ion hits at the drain of \( P_{20} \) which has been presented in Fig. 2 and Fig. 5(b). The SET pulse still occurs subsequent to striking. Nevertheless, the final output is not disturbed. It implies that the proposed technique can prevent the SET pulse from propagating further through the circuit. After hitting by an ion, \( n_4 \) (the voltage of the drain of \( P_{20} \)) rises to a high level rapidly. The gates of the PMOSs of the third stage are connected to \( n_4 \), and the PMOSs of the third stage are turned off. Nonetheless, \( n_5 \) (the voltage of the drain of \( P_{22} \)) remains at the low level, and \( n_5 \) connects to the gates of the NMOSs of the third stage. So, the NMOSs would not be conducted, and the outputs of the third stage keep at high level. The SET pulse is eliminated quite effectively that can not affect the final output (which is \( n_{13} \)) at all.

![Fig. 8. Output curves of the second stage and the final stage of the proposed technique when an ion hits at the drain of \( P_{20} \).](image)

Fig. 9 shows the output curves of the second stage and the final stage of the proposed technique when an ion hits at the drain of \( P_{22} \) in Fig. 2 and Fig. 5(b). As
evident to us, n5 is basically less than VDD/2 subsequent to an ion striking, and n4 is hardly disturbed. Just as discussed in section 2, the SET pulse at node n5 is mitigated, and the final output is quite stable.

When an ion strikes vertically with LET of different values, the simulation results are shown in Fig. 10. With the increasing of the value of LET, as regards the conventional inverter chain, the SET pulse gets increasingly wider, but the proposed inverter chain still displays good performance.

As regards an ion striking at east-to-west (E-W) 30° angle [direction (a) in Fig. 11], at E-W 60° angle [direction (b) in Fig. 11], at west-to-east (W-E) 30° angle [direction (c) in Fig. 11], and at W-E 60° angle [direction (d) in Fig. 11], the simulation results of different structures with different ion striking angles have been presented in Fig. 12. As evident to us, the SET affects conventional inverter chain obviously. When an ion strikes at an angle of W-E 60°, even the output signal of the inverter chain using source-isolation technique is interrupted, but the outputs of the proposed schematic stay stable as usual.

Fig. 10. $W_{SET}$ at the terminal of chain when an ion strikes vertically.

Fig. 11. Different directions of ion striking.
When the input $n_1$ is high, for the three inverter chains, all the outputs of the first stage inverters are at the low level, and all the outputs of the second stage inverters are at the high level. We assume that an ion with the LET value of 50 MeV·cm$^2$/mg hits at the center of drain of PMOS of the second stage inverter vertically. The voltage curves of output nodes of the second stage and the final stage of the inverter chains are shown in Fig. 13 to Fig. 16.

**Fig. 12.** $\text{W_{SET}}$ at the terminal of chain when an ion strikes at different angles.

**4.2 Hits “1”**

When the input $n_1$ is high, for the three inverter chains, all the outputs of the first stage inverters are at the low level, and all the outputs of the second stage inverters are at the high level. We assume that an ion with the LET value of 50 MeV·cm$^2$/mg hits at the center of drain of PMOS of the second stage inverter vertically. The voltage curves of output nodes of the second stage and the final stage of the inverter chains are shown in Fig. 13 to Fig. 16.

**Fig. 13.** Output curves of the second stage and the final stage of the conventional inverter chain.

Fig. 13 presents the output curves of both the second stage and the final stage of the conventional inverter chain. The voltage of $n_3$ stays at logic “1” after striking, and the final output is stable.

**Fig. 14.** Output curves of the second stage and the final stage of the inverter chain using source-isolation technique.
Fig. 14 shows the output curves of the second stage and the final stage of the inverter chain using source-isolation technique. As stated earlier, subsequent to an ion striking at the drain of P21 in Fig. 1(b) and Fig. 5(a), the voltage of node n3 drops to low level quickly, and the negative pulse caused by ion striking propagates through the inverter chain.

Fig. 15 presents the output curves of the second stage and the final stage of the proposed technique when an ion hits at the drain of P20 as shown in Fig. 2 and Fig. 5(b). The trend of the output curves is similar to the trend of the output curves in Fig. 13. The logic levels of n4 and n5 do not change, and the final output is stable.

Fig. 16 shows the output curves of the second stage and the final stage of the proposed technique when an ion hits at the drain of P22 in Fig. 2 and Fig. 5(b). The voltage of node n5 gets lowered to logic “0” subsequent to an ion striking, whereas, the fluctuation of the voltage of node n4 is quite small. So, the PMOSs of the third stage are still at OFF-state. The third stage to the final stage still output correctly.

Fig. 17 presents the output curves of different structures with the LET of different values. With the increasing of the value of LET, as regards the inverter
chain using source-isolation technique, the negative SET pulse occurs and gets increasingly wider. As regards the proposed design, the disturbance caused by ion striking does not change the logic level of the final output, which means that the disturbance disappears in the end of chain.

Fig. 18 shows the output curves of different techniques with different ion striking angles. When an ion strikes at an angle of W-E 60°, the outputs of all structures stay stable, but when an ion strikes at other directions, the circuit performance of the inverter chain that make use of the source-isolation technique is disappointed. However, the proposed schematic can hold the output stably all along.

5 Conclusion

In this paper, a dual-output hardening design of inverter chain is proposed for P-hit SET mitigation. In combination with the optimization design of isolation in layout, the proposed dual-output structure can eliminate SET pulse effectively. On the basis of TCAD 65 nm CMOS technology, the simulation results show that the proposed structure can solve the problem of conventional inverter chain when an ion hits “0” and the problem of the inverter chain using source-isolation technique when an ion hits “1”. Together with that, the SET pulse that occurs at any stage of the proposed inverter chain will be eliminated, as long as it does not occur at the final stage.

Acknowledgment

This work was supported by the National Natural Science Foundation of China (Grant No. 61674002, 61574001 and 61474001) and National Science and Technology Major Project (Grant No. 2017ZX01028-101-003).