Energy Efficiency Tradeoffs for Sub-THz Multi-User MIMO Base Station Receivers

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Abstract—Sub-terahertz (sub-THz) antenna array architectures significantly impact power usage and communications capacity in multi-user multiple-input multiple-output (MU-MIMO) systems. In this work, we compare the energy efficiency and spectral efficiency of three MU-MIMO capable array architectures for base station receivers. We provide a sub-THz circuits power analysis, based on our review of state-of-the-art D-band and G-band components, and compare communications capabilities through wideband simulations. Our analysis reveals that digital arrays can provide the highest spectral efficiency and energy efficiency, due to the high power consumption of sub-THz active phase shifters or when SNR and system spectral efficiency requirements are high.

Index Terms—sub-THz, D-band, G-band, power consumption, MU-MIMO, 6G, base station, receiver

I. INTRODUCTION

As demand for cellular data increases, wide bandwidths available at upper millimeter-wave (mmW) and sub-THz frequencies are being proposed for future wireless networks. Studies for future 5G and 6G standards are considering D-band (110-170 GHz) and G-band (140-220 GHz) as the natural progression from mmW systems in current 5G New Radio (NR) standards. However, the power consumption of transceivers at these bands, especially those capable of spatially multiplexing multiple users at once with MU-MIMO, is a major concern for future development. While many studies have assumed base station (BS) power consumption is irrelevant to system performance, this perspective ignores the ongoing operational costs, stricter thermal design requirements, and the environmental concerns of higher power usage.

Few prior works have considered the power consumption or energy efficiency of sub-THz systems. The power consumption study in [1] analyzed digital and analog handheld sub-THz receiver (RX) architectures, but analog arrays do not support MU-MIMO capability. The authors of [2] used a theoretical link budget to compute sub-THz RX and transmitter (TX) power. Neither examined the impact of array architectures on communications capability.

Several publications have investigated BS power consumption at mmW bands. [3] detailed tradeoffs in array architecture, communications capability, power consumption, and circuit area for 28 GHz BS TXs but not RXs. Additionally, the trade study in [4] compared the theoretical capacity and energy efficiency of 60 GHz RX designs, but did not use simulations to evaluate realistic achievable rates.

This work investigates the energy efficiency of sub-THz BS RXs with three MU-MIMO capable array architectures. We compare the digital array architecture (DA), the sub-array hybrid architecture (SA), and the fully connected hybrid architecture (FH) for power consumption and simulated communications performance. Our detailed circuits and systems modeling, utilizing a literature survey of recent D-band and G-band components, provides a higher fidelity power model than prior studies at sub-THz. Wideband, symbol-level, MU-MIMO orthogonal frequency division multiplexing (OFDM) simulations then provide realistic estimates of each architecture’s communications capabilities. Compared to prior work, we provide a more realistic trade study for sub-THz BS RXs.

II. PROBLEM STATEMENT

To understand the RX power consumption, we first review the three array architecture designs. Fig. 1 shows block diagrams for the DA, SA and FH. Table I then summarizes the total number of each component required for each design. The number of RF chains, \( N_{RF} \), limits both the maximum number of simultaneous streams the RX can support and the degrees of freedom for MIMO combining. While \( N_{RF} \) for the DA is fixed to the number of BS antennas \( N_{BS} \), \( N_{RF} < N_{BS} \) is a design parameter for the SA and the FH. Although this work assumes \( N_{RF} = U \), where \( U \) is the number of users simultaneously connected to the BS, the SA and FH each offer unique combinations of hardware requirements and degrees of freedom for combining. Compared to the DA, the SA and FH reduce communications capability and increase the number of RF components in order to reduce the number of baseband components. Additionally, analog-to-digital converters (ADC) resolution and wideband channels make the tradeoff more complex. The goal of this work is to evaluate this tradeoff between RX architecture, power consumption, communications capability, and ADC resolution using realistic circuit component power.

III. ANALYSIS APPROACH

To capture the power consumption and communications capabilities of each of these array designs, we use spectral
efficiency (SE) and energy efficiency (EE) as system metrics. SE is commonly used as a system requirement, defined as

\[ S = \frac{1}{K} \sum_{k=1}^{K} \sum_{u=1}^{U} \log_2 (1 + \gamma_{u,k}) \] (1)

where \( K \) is the number of subcarriers and \( \gamma_{u,k} \) is the signal-to-interference-and-noise ratio (SINR) for user \( u \) at subcarrier \( k \) after MIMO combining. (1) computes the SE from capacities averaged over subcarriers, but summed over all users. As in [4], the EE is defined by the data rate achieved per unit power consumed: \( E = \frac{S}{P} \) where \( B \) is the total system bandwidth and \( P \) is the total receiver power consumption. Since EE depends on SE, the tradeoff was computed in three steps: 1) simulate the system SE; 2) calculate the total circuit power from the circuits literature survey; and 3) assess the EE using the assumed \( B \) and computed \( S \) and \( P \).

Wideband Monte Carlo (MC) simulations implemented MIMO-OFDM to compute the SE. Each user is assumed to have an analog phased array TX with \( N_U \) antennas. By concatenating all \( U \) user TX arrays and their channels, we modeled the system at subcarrier \( k \) in (2), where \( \mathbf{Y} \) represents the concatenated received streams for all users, \( \mathbf{W}_D \in \mathbb{C}^{N_R \times U} \) is the digital combiner, \( \mathbf{W}_{RF} \in \mathbb{C}^{N_B \times N_R} \) is the analog combiner (an identity matrix for the DA), \( \mathbf{V}_{RF} \in \mathbb{C}^{U \times N_U} \) is the concatenated analog precoding for all users, and \( \mathbf{Z} \) is the Gaussian noise at the antennas.

\[ \mathbf{Y}[k] = \mathbf{W}_D^H[k] \mathbf{W}_{RF}^H[k] \mathbf{H}[k] (\mathbf{V}_{RF} \mathbf{S}[k] + \mathbf{Z}[k]) \] (2)

The precoder and combiner matrices were computed using the algorithms detailed in [5] and [6], with the multiple users acting as a distributed sub-array TX. Due to the PS constraints, each entry of \( \mathbf{W}_{RF} \) and \( \mathbf{V}_{RF} \) must be unit magnitude. Additionally, the array architectures require \( \mathbf{W}_{RF} \) for the SA and \( \mathbf{V}_{RF} \) to be block diagonal matrices. Thus, \( \mathbf{W}_{RF} \) and \( \mathbf{V}_{RF} \) required an iterative algorithm due to these hardware constraints on the matrix solutions and the wideband sub-THz channel, while \( \mathbf{W}_D \) was computed with the MMSE solution. As one of the few sub-THz channel models based on experimental data, the simulations used NYUSIM 3.0 [7], a statistical channel model based on indoor measurements at 140 GHz. We used 10 MC trials to average the SE over many channel realizations, totaling 80 independent user channels.

Each MC trial simulated 1000 symbols to estimate the stream SINR. Symbols for each subcarrier were modeled using zero-mean, complex Gaussian random numbers with variance defined by the signal power. We used Gaussian symbols to represent a generalized amplitude and phase modulation. Simulations estimated the user SINR for each subcarrier in (3), applying the MMSE solution \( \hat{\mathbf{g}}_{u,k} = \mathbf{s}_{u,k}^\dagger \mathbf{y}_{u,k} \) for the output signal gain \( \gamma_{u,k} \) using known transmitted symbols \( \mathbf{s}_{u,k} \) and received symbols \( \mathbf{y}_{u,k} \). Table II lists the other critical system assumptions used in the simulations.

\[ \gamma_{u,k} = \frac{\| \mathbf{g}_{u,k} \|_2^2}{\sigma_{int}^2}, \quad \sigma_{int}^2 = \mathbb{E}[\| \mathbf{y}_u - \hat{\mathbf{g}}_{u,k} \mathbf{s}_{u,k} \|^2] \] (3)

**IV. SUB-THZ COMPONENT POWER AND SURVEY**

The total RX power was modeled as a sum of component powers determined from our literature survey [8]. Explicitly, the power is computed in (4), with the component powers described in the remainder of this section.

\[ P = (P_{LNA} \cdot N_{BS}) + (P_{RF} \cdot N_{RF}) + P_{DSP} \] (4)

\[ P_{RF} = P_{LO} + P_{Mixer} + P_{VGA} + P_{ADC} \] (5)

LNA power was computed based on a figure-of-merit (FoM) from our literature survey, as in (6). [9] showed the highest FoM in the survey, with \( F_{LNA} = 1.84 \text{ mW} \). We assumed a noise figure (NF) of 10 dB (\( F_{LNA} = 10 \)) and gain \( G_{LNA} = 26 \text{ dB} \), as in the selected LNA design, translating to a unit power of 24 mW. The gain was fixed to determine a realistic LNA power, though higher power LNAs with larger gains may be needed to meet implementation specific RX NF requirements. The remainder of the gain required in the signal path was generated in the baseband (BB) VGAs.

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**TABLE I: Summary of the number of required components**

| Component                                | DA   | SA    | FH   |
|------------------------------------------|------|-------|------|
| Low Noise Amplifiers (LNA)               | \( N_{BS} \) | \( N_{BS} \) | \( N_{BS} \) |
| Phase Shifters (PS)                      | 0    | \( N_{RF} \) | \( N_{RF} \) |
| Mixers                                   | \( N_{BS} \) | \( N_{RF} \) | \( N_{RF} \) |
| Local Oscillators (LO)                   | \( N_{RF} \) | \( N_{RF} \) | \( N_{RF} \) |
| Variable Gain Amplifier (VGA)            | \( N_{RF} \) | \( N_{RF} \) | \( N_{RF} \) |
| ADCs                                     | \( N_{RF} \) | \( N_{RF} \) | \( N_{RF} \) |

**TABLE II: Simulation settings and assumptions**

| Channel scenario | Indoor office line-of-sight (LOS) |
|------------------|----------------------------------|
| \( N_{BS} \)    | \([16 \times 4, (32 \times 4), (24 \times 8), (32 \times 8)]\) |
| \( N_U \)       | 16 \times 4                      |
| Number of Subcarriers | 256                              |
| Power            | \( 800 \text{ MHz} \)            |
The sub-THz survey included both active and passive mixer designs. As in [1], we selected a passive mixer ($P_{\text{Mixer}} = 0$) to minimize DC power consumption, although active mixers may be more suitable depending on implementation specific ADC, VGA, LO, and NF requirements. With a conversion loss of $I_M = 9.8$ dB, the lowest among passive mixers, [10] minimized the VGA gain required. The LO in [11] was then selected for having the highest DC-to-RF efficiency and sufficient RF output for the mixer. If signal distribution losses are low, the total power potentially could be reduced by using one LO to drive two mixers, since the LO in [11] outputs 3.3 dB more RF power than the mixer in [10] requires. For simplicity, we assumed that each mixer required its own LO. PS, splitter, and combiner losses affect the VGA power by determining the maximum gain required. PS power and insertion loss (IL) vary based on the required resolution; active PS’s generally support higher resolutions than passive designs but require DC power. In our power analysis, we considered two PS cases: passive PS’s based on [12] with an IL of $I_P = 6$ dB and active PS’s based on [13] requiring 30 mW of power and $I_P = 5.8$ dB IL. As shown in the literature survey, splitters and combiners at sub-THz have significant insertion loss. Based on [14], we assumed an IL of $I_S = I_C = 1.3$ dB for up to 8 output traces for splitters and 8 input traces for combiners. The total distribution loss was computed based on the number of series splitters and combiners required to support enough RF signal paths in each hybrid architecture. The BB VGA was modeled to provide the required input voltage range for the ADCs. Based on the survey, VGAs tend to use nearly the same power within their designed gain range. Using [15], we assumed a unit power of $P_v = 10.8$ mW for each unit of $G_v = 20$ dB gain required. We selected the total BB gain to amplify the weakest input signals, assuming a minimum per-antenna SNR of 0 dB ($\zeta = 1$) and thermal noise at $T = 300$K, to the ADC’s peak-to-peak input swing $V_a$ (V). (7) shows the total power for each set of VGAs to meet the required total gain in (8), where $P_a = \zeta P_v$ and $P_n = k_B T B$ are the minimum per-antenna input signal and noise power (W) respectively and $k_B$ is the Boltzmann constant.

$$P_{\text{VGA}} = P_v \cdot \left[ \frac{G_{\text{VGA}}}{\zeta v} \right]$$

$$G_{\text{VGA}} = 10 \log_{10} \left( \frac{V_a^2}{8R I_S + I_P + I_C + I_M} \right) = G_{\text{LNA}} + I_S + I_P + I_C + I_M$$

ADC and digital signal processing (DSP) power are both computed using FoMs. The ADC power was computed in (9), with the Walden FoM, sampling frequency $F_s = 2B$, and an ADC resolution of $N_b$ bits. We assumed $FoM_{\text{ADC}} = 40$ fJ/sample, and the median FoM of designs surveyed in [16] over the last 6 years, and $V_a = 0.5$ V from [17]. (10) computes the DSP power with $FoM_{\text{DSP}} = 13$ GOPS/mW, where $U \cdot (2N_{RF} - 1)$ represents the number of operations to apply the digital combiner. Although the $W_D[k]$ is applied to every subcarrier, the total number of operations does not scale with $K$, as the results are only computed for each OFDM symbol instead of each sample. The DSP FoM was selected from [18] for a 40 nm CMOS radio processor.

$$P_{\text{ADC}} = FoM_{\text{ADC}} \cdot F_s \cdot 2^{N_b} = FoM_{\text{ADC}} \cdot B \cdot 2^{N_b + 1}$$

$$P_{\text{DSP}} = U \cdot (2N_{RF} - 1) \cdot B \cdot FoM_{\text{DSP}}^{-1}$$

V. Tradeoff Results

The total RX power consumption depends primarily on the architecture and the PS’s. A breakdown of the power consumption by component is shown in Fig. 2. Since the active PS’s have nearly the same IL as the passive PS’s, this graph can illustrate power for both cases. If the PS group bars are ignored for the passive PS case, Fig. 2 shows that the DA uses much more power than other architectures in nearly all components. However, for the active PS case, PS’s consume the most power of any component in the SA and FH due to the sheer number of devices. Fig. 3 compares the total power of several design combinations and illustrates the impact of PS’s clearly. Requiring active PS’s increases the FH’s power by an order-of-magnitude and increases the SA’s power to be nearly the same as that of the DA.

Although higher ADC resolution exponentially increases ADC power, high resolution does not significantly affect total power in any of the three architectures. Fig. 2 demonstrates that the RF and BB components consume an order-of-magnitude or more power than 5-bit ADCs, while Fig. 3 illustrates the minimal impact ADC resolution has on the total RX power. This conclusion is consistent with [1], although different assumptions on gain distribution shift the total power consumption amongst the BB and RF components.

The SE and EE tradeoffs summarize the reduced power efficiency resulting from higher communication capability requirements, combining the impacts of component power, architecture, and assumed SNR. Note that each point on a given EE vs SE curve represents a different array size; larger
Fig. 3: Total power for primary RX configurations

arrays generally have higher SE and lower EE, corresponding to the bottom right of the graphs. Fig. 4 provides the worst scenario for the DA with low per-antenna SNR (0 dB) and passive PS’s. The low SNR limited the array’s maximum capacity, inhibiting the DA’s ability to take advantage of more combiner parameters and resulting in similar SE performance between the DA and the FH. In this case, the FH with 5-bit ADCs provided the best EE vs SE tradeoff, since passive PS’s allowed the SA and the FH to utilize much less power than the DA. Only in cases where the maximum SE is required, around 1 bits/s/Hz higher than the FH’s maximum, is the DA the only option and thus the most efficient.

Requiring active PS’s or higher SNRs made the DA more competitive. Fig. 5 shows the active PS case with 0 dB SNR. The huge increase in power for the SA and FH with active PS’s reduced the EE of the SA by half and the EE of the FH by nearly 10 times. Thus, the DA became more efficient than the hybrid designs at high SEs and the FH was not viable under any SE requirement. Fig. 6 demonstrates the benefit of higher per-antenna SNRs for the DA. While the hybrid arrays saw small increases in SE, the DA achieved nearly 3 bits/s/Hz improvement. Thus, at higher SNRs, the DA with 5-bit ADCs became the most efficient option for high SE requirements.

VI. CONCLUSION AND FUTURE WORK

This paper presents realistic power consumption and trade-offs in EE for required SE. MC communication simulations and a survey of state-of-the-art sub-THz circuit components provides a realistic analysis of BS RX capacity and power consumption. Our results show that the DA can be the most efficient architecture, especially in high SNRs, when active PS’s must be used, or when high SE is required. Sub-THz TX considerations, realistic sub-THz cellular link budgets, the impact of PS quantization on hybrid combining, and additional channel environments are left as future work for sub-THz BS analysis. Low power sub-THz LNAs, LOs, and PS’s could significantly improve the efficiency of future array designs.
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