Galvanostatic Plating with a Single Additive Electrolyte for Bottom-Up Filling of Copper in Mesoscale TSVs

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A methanesulfonic acid (MSA) electrolyte with a single suppressor additive was used for potentiostatic bottom-up filling of copper in mesoscale through silicon vias (TSVs). Conversely, galvanostatic deposition is desirable for production level full wafer plating tools as they are typically not equipped with reference electrodes which are required for potentiostatic plating. Potentiostatic deposition was used to determine the over-potential required for bottom-up TSV filling and the resultant current was measured to establish a range of current densities to investigate for galvanostatic deposition. Galvanostatic plating conditions were then optimized to achieve void-free bottom-up filling in mesoscale TSVs for a range of sample sizes.

Since the breakdown of Dennard scaling and Moore’s Law there has been increased focus on 3D and heterogeneous integration in order to continue the advancement of microelectronic systems. 3D integration, through the use of through silicon vias (TSVs), offers many advantages to microelectronics. As opposed to wire bonds at the periphery of a chip, TSVs are able to increase the attainable number of I/O by taking advantage of the full area of a chip. All metal TSVs, as compared to doped poly-silicon TSVs, greatly improve thermal conduction away from the chip surface and reduce electrical parasitics, both of which are particularly advantageous in RF and microwave applications. In order to increase I/O counts per area and decrease overall package sizes, shrinking the TSV pitch is of significant interest in industry. A reduction in pitch has led to a reduction in TSV depth, due to aspect ratio limitations in reactive ion etching (RIE), which necessitates thinning the Si substrate. However, many applications, such as MEMS devices, depend on the full thickness of the silicon (Si) substrate to maintain structural rigidity, control the radius of curvature of the substrate, and/or conserve mass for accelerometer devices. Maintaining optimal substrate thickness is desired, but there has been sparse work focused on integrating TSVs with fully thick substrates or silicon-on-insulator (SOI) based technologies. This work develops a Cu plating process for a TSV-last integration scheme that is compatible with SOI substrates without the need for Si thinning.

Numerous studies have evaluated potentiostatic Cu filling of micrometer scale TSVs. These studies have offered a productive understanding of the Cu filling mechanism with various additives in the electrolyte. However, the implementation of these techniques on an industrial level has been limited because conventional copper plating tools often are not equipped with reference electrodes which are required for potentiostatic deposition. This work leverages the principals of Cu reduction in a suppressed solution during potentiostatic deposition to establish and optimize galvanostatic plating conditions for use in a production level plating tool. Historically, plating electrolytes with three additives have been utilized. These systems consist of an accelerator, a leveler, and a suppressor which are derived from chemistries developed for plating vias in printed circuit boards (PCBs). The accelerator is a surfactant molecule that adsorbs on the surface and preferentially increases the plating rate as a function of surface coverage. This effect is desired for filling concave bottoms of high aspect ratio features and is known as curvature enhanced accelerator coverage (CEAC). The suppressor is a large chain polymer (1k–20k MW) which inhibits deposition. As a gradient in the surface coverage of the suppressor occurs throughout the depth of a feature, a counter-balancing gradient in the deposition rate is achieved (slower deposition higher in the via where there is a larger concentration of suppressor molecules). The leveler behaves as a grain refiner and helps to reduce the overburden thickness. Chloride, which is a fourth additive common to all Cu plating chemistries, competitively complexes with the suppressor and accelerator species at the surface of the cathode and is required for the suppressor to function.

In contrast to conventional three-additive systems which rely on the CEAC mechanism, bottom-up superfilling of large TSVs using a single polyether suppressor additive has been achieved. This bottom-up superfilling mechanism is dependent on a careful balance between the applied potential and the diffusion of both suppressor molecules and Cu ions. Void-free bottom-up filling was realized in die level plating experiments on sample sizes ranging from 1 cm² up to approximately 10 cm². The plating was first performed potentiostatically while measuring the resulting current in order to determine an optimal current density for realizing void-free filling of vias. Chronoamperometry was performed to understand the relationship between voltage and current in a poloxamine suppressor containing chemistry on a single TSV die. Next, samples of varying area were subjected to the same chronoamperometric conditions to establish a range of current densities likely to achieve bottom up filling. Galvanostatic plating conditions were then established and void-free superfilling of mesoscale TSVs is demonstrated.

Experimental Procedure

TSV definition.—The TSVs for this work consist of 100 μm diameter vias etched through a 600 μm thick handle layer of a SOI substrate integrated in a TSV-last approach. Figure 1a shows a cross-sectional illustration of the integration approach. On the frontside of the SOI substrate, concentric trenches are etched through the device layer of the SOI substrate, landing on the buried oxide (BOx), and filled with tungsten (W) deposited through chemical vapor deposition (CVD), (Figure 1c). An isolation trench, outbound of the W vias is etched and filled with stoichiometric nitride and undoped poly-Si to isolate the concentric vias from the rest of the substrate and adjacent TSVs (Figure 1d). A multiple metal layer device is fabricated on the topside of the Si wafer employing AlCuSi metal layers, SiO₂ inter-metal dielectric, and W vias. After the device is fabricated on the top Si, the final metal layer is protected with 0.5 μm of SiO₂ and the TSVs are patterned and etched on the handle (backside) of the SOI substrate.

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Figure 1. (a) Graphical illustration of TSV integration approach. (b) Cross-sectional optical image of an array of Cu filled TSVs. (c) Scanning electron micrograph (SEM) of the isolation trench and W vias in the device layer Si of the SOI substrate contacting a two metal layer test structure device. (d) SEM of W vias implanted in device layer Si making electrical contact to ECD Cu. (e) SEM of Cu filled TSV at the top side of an SOI substrate.

3 μm of resist is patterned on top of a 6 μm thick SiO2 hard mask for the 600 μm thick handle layer etch. The deep Si etch lands on BOX of the SOI substrate. Substantial over etch during the deep Si etch is performed to compensate for the etch non-uniformity across the 150 mm diameter wafer. This over-etch results in notching at the bottom of the TSV. A fluorine chemical downstream etch is used to remove Si spires resulting from the deep etch and to smooth the sidewalls of the Si. The BOX is then etched to reveal the W vias in the device layer Si for making electrical connection to the plated Cu. Due to the etch profile of the TSV in the Si handle, and in particular the notch at the bottom of the via, atomic layer deposition (ALD) is used to deposit a 300 nm thick layer of Al2O3 to insulate the TSV from the handle Si. A directional etch is used to remove the Al2O3 from the horizontal surfaces while leaving the insulating layer on the sidewall of the via. A 60 nm thick plasma of Pt (Pt) is conformally deposited on the Al2O3 insulating layer to serve as a barrier layer and a conductive seed metal for electrochemically deposited (ECD) Cu. Figure 1b is a cross-sectional optical image of an array of TSVs filled with Cu and Figure 1e is a SEM image of the interface between the ECD Cu and the W trench vias in the device layer Si.

Electrochemical deposition apparatus.—Die level plating experiments were conducted using a machined aluminum (Al) rod threaded into a rotating disk electrode (RDE) apparatus for electrical contact. A cleaved wafer was mechanically and electrically connected to the aluminum rod using a perpendicular machined slot and underside set screw, Figure 2a. Chemical stop off masking, XP2000 (Tolber, USA), was used to control the conductive area during plating and mask the bottom of the Al rod to prevent IR loss (voltage drop) due to any additional exposed conductive surfaces in the electrolyte. The rod is rotated at 400 rpm in solution to instigate solution replenishment in the deep TSVs. Potential and current were controlled with a BioLogic SP-200 potentiostat (Bio-logic USA, LLC) and EC-lab software.

TSV Pre-wet process.—In order to achieve bottom-up filling in TSVs, the Cu electrolyte must be able to fully fill the vias without any trapped air bubbles when immersed in the plating electrolyte. TSV pre-wetting consisted of immersing the sample into −18 °C isopropyl alcohol (IPA, Sigma Aldrich USA) and pulling vacuum on the solution with a rough pump. Figure 2c shows a 150 mm diameter Si wafer, with 100 μm wide and 600 μm deep TSVs, submersed in IPA while under vacuum. The bubbles in Figure 2c are due to air evacuating the TSVs at the reduced chamber pressure. Samples remain submersed in IPA until transferred directly into the plating electrolyte to prevent ingress of air into any of the TSVs before plating is initiated. Once in the plating solution, the sample is rotated at 400 rpm for 2 minutes to allow the solvent to diffuse into the chemistry and the Cu electrolyte to fill the vias.

ECD solution.—An electrolyte consisting of 1.25 M CuSO4, 0.25 M methane sulfonic acid (MSA), 1 mM KCl and 50 μM Tetronic 701 was used for TSV filling experiments. Previous work by Josell and Moffat11,12,21,22 has outlined a characteristic S-shaped negative differential resistance (S-NDR) property for chemistries that are capable of achieving bottom-up superfilling of TSVs from continuous conductive seed metals. Figure 2b shows a CV curve of this MSA electrolyte at varying concentrations of Tetronic 701 suppressor ranging from 6 to 100 μM. Figure 2b shows that this plating chemistry exhibits the characteristic S-NDR shape that is representative of a chemistry capable of achieving bottom-up superfilling. Sulfuric acid was replaced with MSA as the electrolyte because MSA has a higher solubility of Cu compared to sulfuric acid at similar acid concentrations, thereby reducing Cu depletion near the TSV bottom. Bottom-up superfilling of these TSVs through potentiostatic plating with a reference electrode was demonstrated in this same electrolyte at an overpotential of −0.64 V vs the saturated mercury mercurous sulfate reference electrode (SSE) and the determination of this adequate overpotential is described in a separate publication.25

Results and Discussion

To understand the effect of the suppressor additive on current-voltage characteristics, plating using a base electrolyte of 1.25 M copper sulfate, 0.25 M MSA, and 1 mM potassium chloride was performed with and without the presence of 50 μM Tetronic 701 suppressor. Unpatterned Si test coupons coated in a platinum seed metal were plated in both chemistries at varying applied current densities. Current was applied galvanostatically while measuring the resulting voltage.
The electrochemical cell consisted of 250 ml of the plating solution both with (Figure 3a) and without (Figure 3b) 50 μmol/L of Tetronic 701 suppressor. Each plating run was conducted with a known area of unmasked Pt on the diced piece of Si and the samples were rotated at 400 rpm in the same arrangement as described in Figure 2a. Using the SP-200 from BioLogic Science Instruments, constant current was applied at current densities of 0.5, 1, 2, 5, and 10 mA/cm² for two hours while the voltage was recorded at a frequency of 1 Hz.

For initial plating, a slightly more negative voltage is required to reach the suppressor breakdown potential and initiate nucleation. This suppressor breakdown potential is the location on the x-axis in Figure 2b. where sufficient voltage is applied to disrupt the adsorbed polyether-Cl⁻ complex evident by a dramatic increase in current. As plating proceeds and the surface is coated in copper, reduction of Cu²⁺ ion increases and the voltage relaxes slightly. The tight fluctuations in voltage in the 0.5 mA/cm² curve in Figure 3a suggest the destabilization and re-stabilization of the suppressor. When a higher current density is applied, 2 mA/cm², the potential is significantly more consistent. In the case of no suppressor, Figure 3b, significantly less voltage is needed to achieve the target current density.

These results are a direct visualization of the suppressor functioning and correlate with the cyclic voltammograms in Figure 2b. Even when the applied current density is significantly low, 0.5 mA/cm², the minimum voltage needed to achieve that current density, ~0.6 V(SSE), is near the breakdown potential of the suppressor. Further, the voltage does not increase much beyond the breakdown point in order to achieve the higher current densities. Without the presence of the suppressor, the voltage varies more than 100 mV across the range of current densities. Conversely, the voltage varies on the order of 50 mV in the chemistry with suppressor present. The fact that the voltage remains near the suppressor breakdown potential at a wide range of current densities, Figure 3a, indicates that a galvanostatic plating regime is capable of achieving bottom-up filling, as well as overcoming any changes in the bath chemistry that may result in fluctuations in the breakdown potential.

To determine the range of current densities that should be analyzed for galvanostatic filling of TSVs, a set of samples with varying numbers of TSVs were plated potentiostatically at ~0.64 V(SSE), which was previously determined to be the optimum voltage for obtaining void-free filling. Three samples having via areas of 0.0123 cm², 0.073 cm², and 0.123 cm² (100, 600, and 1000 TSVs respectively) were plated at a constant voltage and the resulting current density was measured as a function of time, Figure 4. When deposition occurs in a bottom-up superfilling regime, the effective current density during deposition is calculated using only the area at the bottom of the TSVs and the contributions of the sidewalls of the TSVs and the top field of the substrate is neglected as it is assumed that they are insulated by the suppressor molecules. Throughout this paper, the current densities mentioned are based only on the surface area of the bottom of the TSVs. At the optimum over potential of ~0.64 V(SSE) each of the samples exhibit a void free fill however the current densities used do not increase consistently corresponding to the increased plating area. As a result, the data in Figure 4 was used to establish a range of current densities to use for galvanostatic plating experiments.

Currents of 80, 100, 160, and 320 mA/cm² were applied for three hours to different samples having the same plating area. Figure 5 shows via fill and overpotential behavior for each sample. The lower current densities, 80 and 100 mA/cm², exhibited signs of small voids within the vias and the larger current density, 320 mA/cm², resulted in significantly more plating on the field of the sample which is indicative of the current overcoming the suppressor molecules on the field of the sample. 160 mA/cm² was observed to result in the best fill profile. Figure 5e shows overpotential behavior for each sample and is revealed to be very close to the breakdown suppression voltage observed in
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Figure 3. Chronopotentiometry without (a) and with (b) 50 μM Tetronic 701 suppressor additive on unpatterned Si pieces with ALD Pt seed metal plated at current densities ranging from 0.5 up to 10 mA/cm².

Figure 2b. The potential throughout the deposition does not hold constant at −0.64 V(SSE) but instead fluctuates slightly over time and varies slightly from sample to sample. The varying voltage is suspected to be a result of either the chemistry changing between samples due to the suppressor molecules oxidizing at the anode or slight variation in the distance between the reference electrode, anode, and cathode between experiments.

In order to verify the repeatability and scalability of this galvanostatic plating approach, 160 mA/cm² was applied to three different sample sizes and the resulting voltage during each of these runs was recorded. Figure 6 shows that plating at 160 mA/cm² on varying sample areas results in void free filling. The chronopotentiometry plot in Figure 6 also shows that the resultant voltage from the galvanostatic run is again within range of the breakdown potential of the suppressor containing electrolyte.

Summary

In this work, a plating chemistry consisting of MSA, CuSO₄, KCl, and Tetronic 701 poloxamine suppressor was utilized to achieve void-free Cu filled mesoscale TSVs. To establish a plating process compatible with production level plating tools, without a reference electrode, galvanostatic plating conditions were developed. Potentiostatic plating conditions were first utilized to establish conditions for a void-free fill and determine a range of current densities to investigate. The utility of the galvanostatic approach for achieving void-free filling was evaluated along with the scalability of this methodology. The galvanostatic plating conditions appear to present a better deposition approach, as compared to potentiostatic filling, because it is capable of compensating for shifts in the breakdown suppression point as the chemistry changes over time. Future work will implement this strategy into a full wafer plating apparatus and apply these plating conditions to 150 mm substrates.

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Figure 5. Cross sectional optical images of galvanostatically plated runs at current densities of 80, 100, 160, and 320 mA/cm² and resultant chronopotentiometry.

Figure 6. Cross sectional optical images and chronopotentiometry of samples containing 100, 400, and 900 TSVs corresponding to via areas of 0.012 cm², 0.048 cm², and 0.096 cm² plated at 160 mA/cm² exhibiting void free Cu filling.

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References

1. C. Kim and Y. K. Yoon, “High Frequency Characterization and Analytical Modeling of Through Glass Via (TGV) for 3D Thin-film Interposer and MEMS packaging,” Electronic Components and Technology Conference, 2013.
2. E. M. Chow, V. Chandrasekaran, A. Partridge, T. Nishida, M. Sheplak, C. F. Quate, and T. W. Kenny, “Process Compatible Polysilicon-Based Electrical Through-Wafer
interconnects in Silicon Substrates,” *Journal of Microelectromechanical Systems, 11* (6) (2002).

3. J. Y. Lee, S. W. Lee, S. K. Lee, and J. H. Park, “Through-glass copper via using the glass reflow and seedless electroplating processes for wafer-level RF MEMS packaging,” *J. Micromech. Microeng., 23*, 085012 (10pp) (2013).

4. K. Kumagai, U. Oneda, H. Iriumino, H. Shimjojo, M. Sunohara, T. Kurihara, M. Hijashi, and Y. Mabuchi, “A Silicon Interposer BGA Package with Cu-Filled TSV and Multi-Layer Co-Plating Interconnect,” *2008 Electronic Components and Technology Conference*.

5. M. Motoyoshi, “Through-Silicon Vias (TSV),” *Proceeding of the IEEE, 97* (1) (2009).

6. P. Ramm, M. J. Wolf, A. Klumpp, R. Wieland, B. Wunderle, and B. Michel, “Through Silicon Via Technology - Processes and Reliability for Wafer-Level 3D System Integration,” *2008 Electronic Components and Technology Conference*.

7. Cheng-Ta Ko and Kuan-Neng Chen, “Wafer-level bonding/stacking technology for 3D integration,” *Microelectronics Reliability*, 50, 481 (2010).

8. Mukta G. Farooq and Subramanian S. Iyer, “3D integration review,” *Science China Information Sciences*, 54, 1012 (2011).

9. A. Eilmovskaya, Y-W. Lin, and A. M. Shkel, “Double-Sided Process for MEMS SOI Sensors With Deep Vertical Thru-Wafer Interconnects,” *Journal of Microelectromechanical Systems, 27*(2) (2018).

10. G-K. Lau, J. Soon, H-Y. Li, K. Chui, and Y. Mingbin, “Process Integration and Challenges of Through Silicon Via (TSV) on Silicon-On-Insulator (SOI) Substrate for 3D Heterogeneous Applications,” *2015 17th Electronics Packaging Technology Conference*.

11. D. Josell and T. P. Moffat, “Superconformal Copper Deposition in Through Silicon vias by Suppression-Breakdown,” *Journal of The Electrochemical Society, 165*(2), D23 (2018).

12. T. P. Moffat and D. Josell, “Extreme Bottom-Up Superfilling of Through-Silicon-Vias by Damascene Process: Suppressor Disruption, Positive Feedback and Turing Patterns,” *Journal of The Electrochemical Society, 159*(4), D208 (2012).

13. D. Josell, D. Wheeler, and T. P. Moffat, “Modeling Extreme Bottom-Up Filling of Through Silicon Vias,” *Journal of The Electrochemical Society, 159*(10), D570 (2012).

14. D. Wheeler, T. P. Moffat, and D. Josell, “Spatial-Temporal Modeling of Extreme Bottom-up Filling of Through Silicon-Vias,” *Journal of The Electrochemical Society, 160*(12), D3260 (2013).

15. J-J. Sun, K. Kondo, T. Okamura, S. Oh, M. Tomisaka, H. Yonemura, M. Hoshino, and K. Takahashi, “High-Aspect-Ratio Copper Via Filling Used for Three-Dimensional Chip Stacking,” *Journal of The Electrochemical Society, 150*(6), G355 (2003).

16. R. Beica, C. Charbono, and T. Ritzdorf, “Through Silicon Via Copper Electrodeposition for 3D Integration,” *2008 electronic Components and Technology Conference*.

17. M. J. Wolf, T. Dretchkow, B. Wunderle, N. Jurgensen, G. Engelmann, O. Ehrenmann, A. Uhlig, B. Michel, and H. Reich, “High Aspect Ratio TSV Copper Filling with Different Seed Layers,” *2008 Electronic Components and Technology Conference*.

18. E. Delbos, L. Omnes, and A. Etcheberry, “Bottom-up filling optimization for efficient TSV metallization,” *Microelectronics Engineering, 87*, 514 (2017).

19. O. Luhn, A. Radisic, P. M. Vereecken, C. Van Hoof, W. Ruythooren, and J.-P. Celis, “Changing Superfilling Mode for Copper Electrodeposition in Blind Holes from Differential Inhibition to Differential Acceleration,” *Electrochemical and Solid-State Letters, 12*(5), D39 (2009).

20. T. P. Moffat, D. Wheeler, S.-K. Kim, and D. Josell, “Curvature enhanced adsorbate coverage mechanism for bottom-up superfilling and bump control in damascene processing,” *Electrochimica Acta, 53*(1), 145 (2007).

21. D. Josell and T. P. Moffat, “Extreme Bottom-Up Filling of Through Silicon Vias and Damascene Trenches with Gold in a Sulfite Electrolyte,” *Journal of The Electrochemical Society, 160*(12), D3035 (2013).

22. D. Josell and T. P. Moffat, “Superconformal Bottom-Up Nickel Deposition in High Aspect Ratio Through Silicon Vias,” *Journal of The Electrochemical Society, 163*(7), D22 (2016).

23. Q. Huang, B. C. Baker-O’Neal, C. Parks, M. Hopstaken, A. Fluegel, C. Emnet, M. Arnold, and D. Mayer, “Leveler Effect and Oscillatory Behavior during Copper Electroplating,” *Journal of The Electrochemical Society, 159*(9), D526 (2012).

24. S. K. Cho, M. J. Kim, and J. J. Kim, “MSA as a Supportin Electrolyte in Copper Electroplating for Filling of Damascene Trenches and Through Silicon Vias,” *Electrochemical and Solid-State Letters, 14*(5), D52 (2011).

25. L. A. Menk, D. Josell, T. P. Moffat, E. Baca, M. G. Blain, A. Smith, J. Dominguez, J. McClain, P. D. Yeh, and A. E. Hollowell, “Bottom-Up Copper Filling of Large Scale Through Silicon Vias for MEMS Technology,” *Journal of The Electrochemical Society, 166*, D3066 (2018).

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