Investigative analysis of match-line sensing schemes in TCAM for high-speed performance

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Abstract. This paper delineates an investigation of TCAM-design techniques for both circuit level and architectural level. In the case of circuit level, low power Match Line sensing techniques and Search Line driving propositions are exhibited. At the architectural level, four processes for curtailing power absorption are introduced. In this paper, 16×16 bit TCAM is designed in 0.18µm CMOS. The hypothesized Match Line sensing scheme truncates power absorption by pruning search time and dampering voltage swing of traditional ones. With respect to the conventional CR-MLSA, the proposed MLSAs delineate the depletion of 56% and 48% for measuring energy. For simulation, 1.8V supply voltage is used.

Keywords. CMOS, Current Race Scheme, MDPA, AF, RF

1. Introduction

Ternary Content Addressable Memory, in other words, named as TCAM, is a tremendous mechanism orchestrated by the structural architecture. The complexity and the delicacy beheld the painstaking efforts of the researchers for their future progeny. Many different kinds of algorithms have been squinting wearily in the misty fogs of the industrial environment for many purposes like medical and healthcare [1-3], power electronics [4-5], and many more which can be so revitalizing that anyone cannot help rejuvenated. TCAM is based on hardware and it is a parallel look-up table in company with masking capability in bitwise level role-playing a coprocessor in any sophisticated network. This momentous sight rode us to an epiphany of thought revealing the intricacies of TCAM and how only purposeful efforts tinged with an earnest target for the well-being of the future can bring about such a wonderful creation. In this case, a flexible and adaptable processing solution is provided by a vicarious value which can be emerged as contemplation about the workflow. TCAM can explicitly be utilized in the case of network routers. Here, each address usually consists of a Network Address and Host address. Only a meaningful stride stemming from a poignant target to uplift the quality of processing will lead to a quantum leap towards success through this.

Network address proliferates in case of the size usually on subnet configuration. On the contrary, the rest of the bits are engrossed by the host address. Utilizing Ternary CAM in the routing table delineates this lookup affair quite coherently. In this case, the address can be stored denoting ‘X’ for the host portion. Look-up destination address sustains scrupulous routine engagement without further
In this regard, developed architectures are apprehending that supplemental functionality cannot but be consummated in an avant-garde way so that deep packet classification can be accelerated and forwarded in the next generation [6-8].

In this paper, the basic construction of TCAM is shown in section 2. The objective is to limit power consumption maintaining high search speed. Maximum consumption of power occurs in match-line (ML) and search-line (SL). In section 3, different match-line sensing schemes are discussed. In section 4, simulation and results and comparisons of different ML sensing schemes are portrayed. The simulations are done in HSPICE environment.

2. Ternary Content Addressable Memory

Ternary Content Addressable Memory (TCAM) is an exceptional archetype of data searching souvenir which can search its total content in a single clock cycle [9]. The significance of the term ‘ternary’ is that it can query and store for (i) High, (ii) Low, and (iii) Wildcard (Ternary) states.

| Entry No. | Address Binary | Output Port |
|-----------|----------------|-------------|
| 1         | 101XX          | A           |
| 2         | 0110X          | B           |
| 3         | 011XX          | C           |
| 4         | 10011          | D           |

It is the key device to speed up packet forwarding in internet routing. IP (Internet Protocol) forwarding is the main objective of internet routers [10-11]. Speed is the main performance parameter here. TCAM is one of the fastest devices in this case. How a CAM effectuates address lookup in Table 1 is portrayed in Figure 1 [12-14].

3. Match-line (ML) Sensing Schemes

MLs and SLs are highly capacitive. Combined SL capacitance arising from a large number of columns is also very large. During the search, MLs are activated simultaneously along with SLs. The switching of these extreme capacitive lines causes vast power absorption in the time of match detection. To lessen this power loss, energy-efficient match detection in ML sensing schemes are quite handy.

3.1. Precharge-High ML Sensing Scheme:

To further materialize the development, improvements should be analyzed with more insight and an empirical-based mathematical model will help in simulating the conditions necessary to implement these improvements in a perspicacious way. Hence, substantial efforts need to be undertaken to set up a qualitative model that can weigh in the standards prevailing state-of-the-art to ensure the practical
realization of making the fundamental part. At first, pre-charging is required high in the match-line, consecutively evaluating by dint of accessing NOR cells. While in case of a miss, it pulls down, in case of a match, leaves the ML high. The imposition of the ML scheme is portrayed as a schematic diagram in Figure 2 (a). SL precharge, ML precharge and ML evaluation are depicted in Figure 2 (b) [15].

![Figure 2](image1.png)

**Figure 2.** (a) A levying Structure and (b) Respective sketch portraying corresponding alterations [6]

However, all the match lines are precharged to VDD. As the number of mismatch of words is lower than match word and those mismatched ML voltages are discharged to the ground, a large amount of wastage of energy is encountered [6]. The comparison circuit suffers from charge distributing perplexity. It depends on the connection between the storage bits and the top transistors or lowest transistors in case of the pull-down path.

![Figure 3](image2.png)

**Figure 3:** (i) Two possible configurations for the NOR cell [6] and (ii) Simple implementation of the selective-precharge match-line technique.

In the Figure 3 (i), gates are connected to the bottom transistors. Charge sharing occurs between ML and nodes X₁, X₂. After the match-line precharge phase during search line precharge one of the search lines is turned ON causing ML voltage V₆L to drop. To solve this from this charge sharing problem configuration shown in Figure 3 (ii) can be used where search bits are convoluted to those transistors which lie in top positions. As it is evident that the stored bit is constant in the course of a search operation, the charge share is annihilated.

### 3.2. Selective-Precharge Scheme

In the conventional scheme, the same amount of energy is required for each match-line regardless of the data pattern and match/mismatch. A selective precharge scheme can provide a good saving in power consumption. Except for the worst-case scenario selective precharge scheme is one of the most quotidian procedures utilized to conserve power on ML. In this scheme, at first, only a subgroup of TCAM cells from the cumulative word is juxtaposed and further requirement of comparison is decided
accordingly. A mundane schematic of selective precharge akin to that presented in [16] is shown in Figure 3(ii).

3.3. Current Race (CR) Scheme

To overcome the problems of conventional ML sensing schemes, the Current Race (CR) scheme is proposed by [10]. CR scheme is the most versatile scheme. For the structural architecture, fundamental for the construction is used by many researchers [7], [8], [10], [12], [13], [14], [15] till date to get a modified dispatch with respect to CR.

Traditional Scheme is precharged high. On the other hand, the CR scheme is precharged low. That is the main discrepancy between them. In this way, despite charging all MLs into high, what CR scheme does is to pre-discharge them to low. Figure 4 (a) and (b) exhibit the CR scheme for word and dummy word respectively.

![Figure 4](image-url) (a)Word in Current Race Scheme and (b) Dummy word in Current Race Scheme

4. Positive Feedback Match-line (PFML) Sensing Schemes

The state-of-the-art CR-MLSA usually charges MLs with a similar enormity of current for both matched and mismatched cases. As long as matched MLs charge to a higher voltage value, consecutively current will gradually decrease in those cases. On the contrary, mismatched ones possess a higher conductive path to ground. Whenever numerical values for mismatch will rise high, the equivalent resistance of the ML will automatically decrease. Current through ML will rise with a spiraling number of mismatches. Undoubtedly, the number of mismatched MLs are enormous. Consequently, a significant amount of energy is squandered due to the high magnitude current in these mismatched MLs. The proposed Positive Feedback Match-line Sensing Scheme solves this problem by supplying a smaller current to mismatched MLs.

4.1. Mismatch-Dependent Power Allocation (MDPA) Scheme

This tremendously excellent Scheme is hypothesized by [8]. In this scheme, to discern mismatched MLs in the time of rising charge and depleting current to these, a feedback unit adheres to the fundamental CR MLSA. The proposed one is depicted in Figure 5 (a). This feedback unit is consisting of two parts namely the level shifter and feedback circuit. All this is to enact the feedback mechanism. At first, the MLSO, voltage of ML, and voltage of VAR are pre-discharged to control the speed. MLEN begins the charge dissipation for all of the MLs. Initially, not only $V_{ML}$ but also $V_{VAR}$ are raised high by current $I_{ML}$ and $I_{bias}$ respectively.

An increment of VAR voltage will simultaneously cause a decrement of ML current. On the contrary, increased $V_{ML}$ will cause the rising of the output of level shifter as well. Matched $I_{ML}$ is noteworthy with respect to mismatched $I_{ML}$. Indistinguishable dummy word is utilized to supply $ML_{OFF}$ signal to hegemonize the ML charging time. Although a huge amount of energy curtail is
depicted in this, the level shifter along with the feedback unit always absorbs almost tantamount energy. In case of a mismatch N1 sometimes remains weakly turn on which means there is a conducting path between $V_{DD}$ and ground. So, for considering a vast amount of mismatches, $V_{ML}$ is a bit of a tiny one for there are numerical paths to ground for MLs which in turn causes static power consumption. On top of that, due to the large size of the level shifter transistor, ML’s capacitive loading spirals up. Again transistor count in this MLSA is higher than the conventional one. Finally, feedback action is very sensitive to $V_{bias}$ and transistor sizes. For the above reasons, the size of the transistor is required to be tuned for modified and proper implementation.

![Figure 5](image1.png)  
**Figure 5.** MLSA in (a) Mismatch-Dependent Power Allocation Scheme. [8], [14] and (b) AF Scheme [7], [15].

**4.2. Active Feedback (AF) Scheme**

To amortize the difficulties of MDPA scheme, the Active Feedback (AF) ML sensing scheme is convoluted. No invariable power is consumed by this proposed one and it outperforms the MD-MLSA in numerous terms namely momentum, energy, area, stoutness, and so on [7]. Figure 5 (b) shows the proposed MLSA with active feedback.

**4.3. Resistive Feedback (RF) Scheme**

The proposed MLSA with resistive shielding is shown in Figure 6. With a view to decoupling, a transistor is required here which lies in a non-linear region. On the other hand, the channel outlasts the sensory point from high capacitance. Accordingly, $I_{Ch}$ should be down-sized to hoard power notwithstanding the sacrificing of the sensing speed. The N3 channel resistance simultaneously will be reducing by dint of body effect as well as decrement of gate-to-source voltage ($V_{GSN3}$) while the voltage of ML is spiraling high [7]. It is excruciatingly dependent upon the mismatch bit’s number.

![Figure 6](image2.png)  
**Figure 6.** MLSA in RF Scheme [7], [15].
5. Results and Simulation

A 16×16 size array and 0.18µm technology are used. These schemes are simulated in HSPICE simulation software. In the case of State-of-the-art Current Race Scheme, Search time is calculated between Voltage of $ML_{RST}$ and Voltage of $ML_{SOD}$ at the half percent of the input voltage. Moreover, $V_{\text{margin}}$ is preredited between the connecting point of $ML_1$ and $ML_{SO1}$ and the highest margin of $ML_3$ in the traditional scheme. These two are shown in the Current Race Scheme, Mismatch Controlled Power Allocation Scheme, Active Feedback Scheme, and Resistive Feedback Scheme in Figure 7, Figure 8, Figure 9, and Figure 10 respectively.

![Figure 7. Current Race (CR) Scheme](image)

![Figure 8. Mismatch-Dependent Power Allocation (MDPA) Scheme](image)

![Figure 9. Active Feedback (AF) Scheme](image)
Figure 10. Resistive Feedback (RF) Scheme

Table 2. Search Time and Voltage Margin for different schemes (ns).

| Name of the Schemes                          | Search Time (ns) | Voltage Margin (ns) |
|----------------------------------------------|------------------|---------------------|
| Current Race (CR) Scheme                     | 5.0446           | 1.112225            |
| Mismatch Dependent Power Allocation (MDPA) Scheme | 2.5927           | 0.81093             |
| Active Feedback (AF) Scheme                  | 2.6361           | 0.859028            |
| Resistive Feedback (RF) Scheme               | 2.5266           | 0.67165             |

From Table 2, we can see that the Resistive Feedback scheme has the lowest search time. And Current Race Scheme has the highest voltage margin. Other than CR scheme, the Active Feedback scheme has a higher voltage margin. It is very difficult to get the optimum value of both speed and noise performances.

6. Conclusion

Among these schemes, RF scheme is with the best speed performance and CR scheme is with the best noise immunity performance. But, its search time is too high (almost double than that of other positive feedback schemes). As a result, its overall efficiency is compromised. To obtain better speed, the voltage margin has to be compromised and vice versa. So, for better speed performance, RF schemes can be used and for a noisy environment, the AF scheme can be used. So, the performance of different ML schemes largely depends on the search speed also known as the search time, and noise margin also known as voltage margin. The advantage of low search time is that search speed increases which is one of the main concerns in designing TCAM. Again the advantage of a higher voltage margin is that if noise is added then it will not show a false match. The proposed positive feedback schemes improve search speed but a tiny bit of a curtailment of the voltage margin has been rendered. PFML has taken a leap-frog in its endeavor to become one of the most well-matched TCAM with a prudent plan taking into account the limitations and capacities of idiosyncratic properties. Till now, it has been remaining on a small-scale but the infrastructure does have the scope to utilize its available resources aided by further development to incorporate more criteria thereby creating a hub of knowledge and the grounds for creating multifaceted co-processors. To disseminate quality performance irrespective of difficulties, it is exigent to expend extensive efforts in the development of the existing structures. MDPA scheme improvises a significant power curtail. On the other hand, AF and RF schemes necessitate a fewer number of transistors in the schematic design. Expediting energy of the MLSAs portrays axing of 56% and 48% with respect to the traditional one.
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