A High Step-Up Interleaved Current-Fed Resonant Converter for High-Voltage Applications

DANESH AMANI¹, (Member, IEEE), REZA BEIRANVAND¹, (Senior Member, IEEE), MOHAMMADREZA ZOLGHADRI², (Senior Member, IEEE), AND FREDE BLAABJERG³, (Fellow, IEEE)
¹Faculty of Electrical and Computer Engineering, Tarbiat Modares University, Tehran 14117-13116, Iran
²Electrical Engineering Department, Sharif University of Technology, Tehran 14588-89694, Iran
³Centre of Reliable Power Electronics (CORPE), Department of Energy Technology, Aalborg University, 9220 Aalborg, Denmark

Corresponding author: Reza Beiranvand (beiranvand@modares.ac.ir)

ABSTRACT A current-fed LLC resonant converter is proposed for high-voltage and high-power applications. Here, a two-phase interleaved structure is used in the input stage under the continuous conduction mode (CCM) to effectively reduce the input current and output voltage ripple values and the input filter and the output capacitors volumes. Due to the expandable structure and high voltage gain, the proposed configuration is suitable for high voltage applications since low voltage stresses are applied across its components. In fact, voltage stresses across the power semiconductors, i.e., MOSFETs and output diodes, along with the output capacitors, are almost one-third of the output voltage in the implemented three-stage configuration of the proposed converter. Here, the switching frequency is chosen close to, but less than, the converter series resonant frequency to reduce its different components’ current stresses and perform soft-switching operation for all power devices under wide input voltage and output power variations. Therefore, conduction and switching losses, and EMI noises are effectively reduced. Consequently, efficiency is improved and high-frequency operation is possible, which reduces the volume of passive components to achieve high-power density. The given topology is thoroughly analyzed mathematically. Also, a 1 kW prototype converter has been implemented to validate the given simulations and analyses. Here, wide input voltage (100 V-200 V) and output power (100 W-1000 W) variations are applied, and an asymmetric pulse width modulation (APWM) technique is used at 143 kHz switching frequency to regulate the output voltage at 1 kV. The obtained maximum efficiency value is 95.3%.

INDEX TERMS Asymmetric pulse width modulation (APWM), current-fed converter, interleaved technique, LLC resonant converter, multi-winding transformer.

I. INTRODUCTION Recently, renewable energy sources have been regarded as a solution to the environmental issues [1], [2]. Since depletable energy sources mostly have low and fluctuating output voltage, using a dc-dc step-up power converter is indispensable to both level up and regulate their output voltages [3], [4]. Till now, various converters such as high step-up, high voltage, interleaved, and resonant converters have been introduced to increase voltage gain, output voltage, and output power of the dc-dc converters. The given converters in [5], [6], [7], and [8] that have been introduced for high voltage applications usually use large transformers turn-ratios to obtain high voltage gains, which in practice increase voltage stresses on some output stage components.

On the other hand, although the transformer turn ratios in most of the high step-up converters [4], [9], [10], [11], [12], [13] are lower than the previously referred ones, they still use large transformer turn ratios to obtain high voltage gains. Consequently, these converters also suffer from similar disadvantages, as mentioned earlier. In some other converters [14], [15], where the transformer turn ratios are small, lower voltage gains are obtained in practice.

Interleaved structures [2], [16], [17], [18], [19], [20], [21] are another large category of converters, which are proposed to increase output power, but they often give small output
voltages, and they are not suitable for high voltage applications. Some of these converters have been used as PFC converters [22], [23], [24].

On the other hand, among the different isolated and non-isolated dc-dc topologies, the full-bridge converter is preferred in many pieces of literature [18], [25], [26], [27], [28]. The soft switching operation is achievable for this converter by phase-shifting without using auxiliary circuits. But, the soft-switching range in conventional phase-shifted full-bridge (PSFB) converter is limited due to the loss of zero voltage switching (ZVS) for primary switches in worst-case conditions. Also, circulating currents power losses are high [29]. Albeit using additional circuits may widen the soft-switching range [30], [31], [32], [33], it leads to higher components count and cost. Resonant-type full-bridge converters can realize soft-switching operation by using resonant tank on the primary side, which can improve the efficiency by eliminating MOSFET-based [28], [34] and IGBT-based [35] converters’ turn-on and turn-off switching losses, respectively.

Another one of the most widely used converters is LLC-based resonant converters, which have received much attention from researchers and industry in recent years due to their good features. These resonant converters have low electromagnetic interference (EMI), and they can provide ZVS condition for primary MOSFETs and zero current switching (ZCS) turn-off condition for output diodes when they operate between series-resonance and parallel-resonance frequencies [36], [37]. Moreover, by paralleling small capacitors to the drain-source of MOSFETs, their turn-off switching losses can be reduced [38], [39]. The LLC resonant converter is widely used in practice in many applications such as renewable energy systems [40], [41], on-board chargers [42], [43], light-emitting diodes (LEDs) [44], [45], and power factor correction (PFC) [46]. To regulate the output voltage of the LLC-based resonant converters, several methods such as Pulse Frequency Modulation (PFM), Phase Shift Modulation (PSM), Pulse Width Modulation (PWM), Asymmetric PWM (APWM), or hybrid modulation strategies like PFM + PWM and PFM + PSM can be utilized [26]. In the PFM strategy that operates based on the resonant tank impedance modification, a wide frequency range is used to regulate the output voltage. So, optimal designs of transformer(s) and inductor(s) are a challenge [47]. Besides, in the PSM strategy, the lagging leg soft commutation may also be lost under the light-load conditions [48].

However, topologies like [22], [23], [49] are only suitable for low voltage applications. Also, the achievable output voltages in [5], [11], [14], [15], [16], [17], [24], [50], [51], and [52], which are roughly twice the aforementioned LLC-based resonant converters due to their half or full bridge output rectifiers, are still low for lots of applications. On the other hand, using voltage quadrupler rectifier configuration [2], [6], [20], [53], [54] increases the converter voltage gain and output voltage values, these values are still low for some applications and we need more improvements.

Interleaving the primary current fed stages and stacking the output rectifiers stages of series-based [19] or LLC-based [55] resonant topologies is a good approach to increase the converter voltage gain, output voltage, and power values. However, many components must be used in these topologies, which in practice reduce the converters’ reliabilities and increase their costs.

Finally, it should be mentioned that [7] is a good configuration for high-voltage high power applications, but its VM rectifier stage needs more capacitors, and lower voltage gain is achieved as compared to the given one here, which has a continuous input current with small ripple value instead of a pulsating current waveform.

Here, a high step-up interleaved current-fed LLC resonant converter, suitable for high-voltage high-power applications, is introduced. Low input current and output voltage ripples, as well as soft-switching operations, are performed under wide input voltage and output power variations by using the well-known asymmetric PWM (APWM) technique to control the output voltage. So, low EMI, high efficiency, high frequency operation, and high power density are practically achievable.

The proposed converter is introduced in Sec. II and its key waveforms and different operational states are given in Sec. III. Then, its steady-state and dead-time analyses are given in Sec. IV and V, respectively. Next, the resonant tank components are calculated in Sec. VI. Also, output stage capacitors values are derived in Sec. VII. Finally, experimental results and conclusions are respectively given in VIII and IX.

II. PROPOSED CONVERTER

The proposed converter with full-bridge topology, suitable for high-power applications, is shown in Fig. 1. This converter current-fed interleaved structure reduces the input current ripple, as well as the input filter volume. The LLC resonant circuit is employed, among existing resonant topologies, due to its excellent features such as soft switching operation of all primary stage switches and output stage diodes even under the wide input voltage and output load variations, low EMI, high efficiency, high power density, low circulating currents, and so forth. A full-wave rectifier is used for each output stage to reduce each diode voltage and current stress. Also, the output-stage diodes and capacitors voltages stresses can be reduced by adding more stages. So, the proposed converter can be used for high-voltage applications. Here, two small capacitors are connected in parallel to $M_{d1}$ and $M_{d2}$ MOSFETs to reduce all power MOSFETs’ turn-off switching losses. Furthermore, the output voltage is regulated by the APWM technique at a desired fixed switching frequency. As a result, unlike pulse frequency modulation (PFM), magnetic components can be designed more efficiently.

III. PROPOSED CONVERTER KEY WAVEFORMS AND ITS DIFFERENT OPERATIONAL STATES

The fundamental waveforms of the proposed converter are plotted in Fig. 2. Based on these waveforms, the proposed
FIGURE 1. General configuration of the proposed step-up converter.

FIGURE 2. The fundamental waveforms of the proposed converter.

The converter has eight different operational states during a switching period for a three-stage configuration, as depicted in Fig. 3. These states are summarized as follows:

State I \([t_0 - t_1]\): at the beginning of this interval, the body diode of \(M_{a_2}\) begins conducting. Therefore, this power switch can be turned on under ZVS condition, as shown in Fig. 2. Diodes \(D_{a_2,4}\) and \(D_{b_1,3}\) also start conducting current from zero by increasing their currents sinusoidally. Here, \(D_{a_2,4}\) and \(D_{b_1,3}\) are conducting and delivering power to the load during this interval, \(M_{b_1}\) is also conducting current and \(M_{a_1}, M_{b_2}, D_{a_1,3}\), and \(D_{b_2,4}\) are all off, as shown in Fig. 3(a). This state ends after \(M_{a_2}\) is turned off. The resonant tank capacitor voltage and inductors current waveforms are respectively given as follows:

\[
v_{C_r}(t) = Z_0 i_{L_r}(0) \sin (\omega_0 t) + \left( v_{C_r}(0) - V_{\text{out}1} + \frac{1}{n} V_{\text{out}2} \right) \cos (\omega_0 t) + V_{\text{out}1} - \frac{1}{n} V_{\text{out}2} \cos (\omega_0 t) \tag{1}
\]

\[
i_{L_r}(t) = i_{L_r}(0) \cos (\omega_0 t) - \frac{1}{Z_0} \left( v_{C_r}(0) - V_{\text{out}1} + \frac{1}{n} V_{\text{out}2} \right) \sin (\omega_0 t) \tag{2}
\]

\[
i_{L_m}(t) = \frac{V_{\text{out}2}}{n L_m} t + i_{L_m}(0) \tag{3}
\]

where,

\[
\omega_0 = \frac{1}{\sqrt{L_r C_r}}, \quad Z_0 = \frac{L_r}{\sqrt{C_r}} \tag{4}
\]

State II \([t_1 - t_2]\): during this interval, \(M_{b_1}\) continues to conduct current, but \(M_{a_2}\) is turned off with small switching losses due to the presence of its drain-source equivalent parasitic capacitance, its fast gate drive signal, and a properly selected dead-time value. In addition, the output stage diodes are switched off under ZCS condition. Therefore, the reverse recovery issue is simply overcome. The conducting states of the different components of the converter are shown in Fig. 3(b).

State III \([t_2 - t_3]\): at the beginning of this interval, the body diode of \(M_{a_1}\) starts conducting current after discharging its drain-source capacitance at the end of the previous state. Therefore, \(M_{a_1}\) can be switched on under ZVS condition. \(M_{b_1}\) is still conducting, but \(M_{a_2}\) and \(M_{b_2}\) are off. Since, the transformer magnetizing current reaches the resonant inductor current, no current passes from the primary side winding to the secondary and third windings. As a result, the output diodes are off and the output load is fully powered by the output capacitors. The conducting states of the converter components are shown in Fig. 3(c). The resonant tank capacitor voltage and inductors currents can be given as follows:

\[
v_{C_r}(t) = Z_0 i_{L_r}(t_2) \sin (\omega_1 (t - t_2)) + v_{C_r}(t_2) \cos (\omega_1 (t - t_2)) \tag{5}
\]
where,

\[ \omega_1 = \frac{1}{\sqrt{(L_r + L_m) C_r}} \quad Z_1 = \frac{\sqrt{L_r + L_m}}{C_r} \]  

State IV \([t_3 - t_4]\): during this state, the body diode of \(M_{a1}\) continues to conduct current, but \(M_{b1}\) is turned off with small switching losses, as previously explained for \(M_{a2}\) during operational State II. All output diodes are still off, and the load is still powered by the output capacitors, as shown in Fig. 3(d). During the next half-switching period, the different operating states of the converter are the same as previously described for States I-IV, but in the opposite direction. Also, the operating states for \(D < 0.5\) are the same as described for \(D > 0.5\), but there are two simple differences.

For \(D < 0.5\), \(M_{a2}\) and \(M_{b2}\) gate-source signals overlap, in contrast to \(D > 0.5\), where the gate-source signals of the lower switches, i.e., \(M_{a1}\) and \(M_{b1}\) overlap. States III and IV are depicted in Fig. 4 for \(D < 0.5\). States VII and VIII are similar to States III and IV, but in opposite directions.

IV. STEADY-STATE ANALYSIS OF THE CONVERTER

To simplify the analysis of the steady-state behavior of the converter, following assumptions are considered: 1) During a switching period, voltage ripples of the output capacitors (i.e., \(C_{out1} - C_{outm}\)) are ignored. 2) The primary stage switches and the output stage diodes are considered ideal. 3) Both input inductors are the same (\(L_a = L_b = L\)). 4) Two non-dominant operational States of II and IV are ignored first, but the converter behavior during the deadtime is separately analyzed in more details later. 5) Different turns ratios of the transformer are considering being the same, i.e., \(N_2/N_1 = \cdots = N_m/N_1 = n\).
1) VOLTAGE STRESSES OF THE OUTPUT CAPACITORS

By applying the volt-second balance principle to one of the input inductors, voltage across \( C_{out1} \) is derived.

\[
V_{C_{out1}} = \frac{V_{in}}{1 - D}
\]

(8)

Thus, voltages of the other capacitors can be identified.

\[
V_{C_{out2}} = \cdots = V_{C_{outm}} = \frac{V_{out}}{m - 1} - \frac{V_{in}}{(m - 1) (1 - D)}
\]

(9)

where, \( m \) is the number of the stages of the converter.

2) INITIAL RESONANT INDUCTOR CURRENT AND RESONANT CAPACITOR VOLTAGE

By ignoring the non-dominant operational States, i.e., II and IV, the following equations set can be derived during a half switching period:

\[
\begin{align*}
  i_{L_p} (0) &= -i_{L_p} (t_a) \\
  i_{L_m} (0) &= i_{L_m} (0) \\
  i_{L_p} (t_a) &= i_{L_m} (t_a) \\
  v_{C_r} (0) &= -v_{C_r} (t_a)
\end{align*}
\]

(10)

Furthermore, since non-dominant operational states are ignored, the following expressions can then be derived:

\[
\begin{align*}
  i_{L_m} (t_2) &= i_{L_m} (t_2) \\
  v_{C_r} (t_2) &= v_{C_r} (t_2)
\end{align*}
\]

(11)

(12)

where, \( i_{L_m}, v_{C_r} \) and \( i_{L_m}, v_{C_r} \) are the magnetizing inductor current and resonant capacitor voltage during operational States I and III, respectively. By using (10)-(12), the resonant inductor current and capacitor voltage initial values, i.e., \( i_{L_p} (0) \) and \( v_{C_r} (0) \), are derived as:

\[
\begin{align*}
  i_{L_p} (0) &= -a_2 V_{out} - b_2 V_{in} \\
  v_{C_r} (0) &= -c_2 V_{out} - d_2 V_{in}
\end{align*}
\]

(13)

(14)

where the given coefficients are calculated as follows:

\[
\begin{align*}
  a_2 &= \frac{\theta_y \cos \theta_y}{n(m - 1) L_m \omega_0 d_1} \\
  &\quad + \frac{\sin \theta_y}{Z_1 d_1} \left[ \left( c_2 - \frac{1}{n(m - 1)} \right) \cos \theta_y + \frac{1}{n(m - 1)} \right] \\
  b_2 &= \frac{-\theta_y \cos \theta_y}{n(m - 1) L_m \omega_0 (1 - D) d_1} \\
  &\quad + \frac{\sin \theta_y}{Z_1 d_1} \left[ \left( d_2 + \frac{n(m - 1) + 1}{n(m - 1) (1 - D)} \right) \cos \theta_y - \frac{n(m - 1) + 1}{n(m - 1) (1 - D)} \right] \\
  c_2 &= \frac{1}{c_1 + d_1} \left[ \frac{\theta_y a_1}{n(m - 1) L_m \omega_0} - \frac{b_1}{n(m - 1)} \right] \\
  d_2 &= \frac{-1}{c_1 + d_1} \left[ \frac{\theta_y a_1}{n(m - 1) L_m \omega_0} - \frac{b_1}{n(m - 1)} \right]
\end{align*}
\]

(15)

(16)

(17)

(18)

(19)

Here \( \theta_x, \theta_y, \lambda, \) and \( F \) parameters are given as follows:

\[
\theta_x = \begin{cases} 
\frac{2\pi D}{2\pi(1-D)} & D \leq 0.5 \\
\frac{2\pi(0.5-D)}{2\pi(0.5-D)} & D > 0.5
\end{cases}
\]

(20)

\[
\theta_y = \begin{cases} 
\frac{2\pi(0.5-D)}{2\pi(0.5-D)} & D \leq 0.5 \\
\frac{2\pi(D-0.5)}{2\pi(D-0.5)} & D > 0.5
\end{cases}
\]

(21)

\[
\lambda = \frac{L_r}{L_m}, F = \frac{f_s}{f_r}
\]

(22)

A. CONVERTER VOLTAGE GAIN

Voltage gain of the proposed converter can be derived by calculating the average output current value as follows:

\[
I_{out} = \frac{V_{out}}{R_L} = \frac{1}{nT_s} \int_0^{T_s/2} (i_{L_m} (t) - i_{L_m} (t)) dt
\]

(23)
By substituting (2), (3), (8), (9), (13), and (14) into (23) and doing some straightforward algebraic calculations, the converter voltage gain is derived, given by as in (24), shown at the bottom of the page. Here, \( R_N = R_L/Z_0 \) is the normalized output load resistance value. (24) clearly shows that the converter voltage gain depends on the converter duty cycle, normalized output load, and normalized switching frequency.

Since the output voltage regulation by varying switching frequency can cause some problems such as inefficient design of magnetic components and also efficient usage of parasitic components of the transformer is a challenge by employing this approach [4], [56]; therefore, the APWM approach is used here to regulate the output voltage.

To identify the necessary duty cycle variations for regulating the output voltage at a desired switching frequency when both input voltage and load variations are applied to the converter, the normalized output voltage is defined as follows:

\[
V_{\text{out}}N = \frac{V_{\text{out}}}{V_b} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{MV_{\text{in}}N}{V_b} \tag{25}
\]

Here, \( V_{\text{in}}N \) is the normalized input voltage and \( V_b \) is defined as:

\[
V_b = \frac{V_{\text{in}}\text{min} + V_{\text{in}}\text{max}}{2} \tag{26}
\]

Using (25), the converter normalized output voltage has been plotted in Fig. 5 under the two worst-case conditions, i.e., (a) minimum input voltage and minimum output load resistance and (b) maximum input voltage and maximum output load resistance. Fig. 5(a) depicts three-dimensional normalized circuit voltage gain versus normalized load resistance, \( R_N \) and duty cycle. The intersections of the desired normalized output voltage value with the two other normalized output load and load resistance and (b) maximum input voltage and maximum output load resistance, \( i_{\text{in}} = V_{\text{in}}\text{max}/\eta V_{\text{in}} \) and \( i_{\text{in}} = i_{L_a} + i_{L_b} \), and doing some straightforward algebraic calculations, the minimum and maximum values of the input current are derived as follows:

\[
\begin{align*}
I_{\text{in}}\text{min} & = \left[ \frac{M}{\eta R_L} + \frac{D T_S}{2 \pi M} \right] V_{\text{out}} \\
I_{\text{in}}\text{max} & = \left[ \frac{M}{\eta R_L} - \frac{D T_S}{2 \pi M} \right] V_{\text{out}}
\end{align*} \tag{28}
\]

where \( \eta \) and \( M \) are the efficiency and voltage gain of the converter, respectively. Since a two-phase interleaved structure is used at the primary side of the proposed converter, the input current ripple is minimized because the inductors currents are the same, but 180 degrees out of phase, as shown in Fig. 6. It should be noted that when \( D = 0.5 \), the inductors currents cancel out each other ripples; thus, the converter has a ripple-free input current under this condition. In addition, when the proposed converter operates under the CCM conditions, the inductors current ripple values as well as the converter input current ripple are further reduced. Therefore, a smaller input filter can be used. Both inductors current
Calculating the ratio of the converter input current ripple value to each of its input inductor current ripple values, i.e., $\Delta i_{in}$ to $\Delta i_L$, it can be shown that how much the input current ripple value decreases with respect to the values of the inductors currents ripples values in the given interleaved structure.

$$\frac{\Delta i_{in}}{\Delta i_L} = \begin{cases} 
\frac{1-D}{1-D} & D \leq 0.5 \\
\frac{2D-1}{D} & D > 0.5 
\end{cases}$$

(30)

By substituting (29) into (30), the normalized input current ripple of the interleaved two-phase structure can be derived as:

$$\Delta i_{inN} = \frac{\Delta i_{in}}{T_s V_{out}/L} = \begin{cases} 
\frac{D(1-2D)}{(1-D)M} & D \leq 0.5 \\
\frac{2D-1}{M} & D > 0.5 
\end{cases}$$

(31)

Based on (31), some curves are plotted in Fig. 7, where Fig. 7(a) illustrates the normalized input current ripple versus different duty cycles and normalized output resistance load values. This figure clearly shows that the input current ripple value increases by increasing the output power value. In addition, when the duty cycle deviates from $D = 0.5$, then the input current ripple increases. Therefore, to minimize the input current ripple, the converter should operate around $D = 0.5$ under full load conditions. Fig. 7(b) shows the normalized input current ripple versus $\lambda$. Because $\lambda$ has a little effect on the normalized input current ripple value, as shown in Fig. 7(b), using large magnetizing inductor value is preferred to minimize the circulating currents and conduction losses.

V. DEAD-TIME ANALYSIS

Although turn-on switching losses of the MOSFETs of the proposed converter are almost eliminated due to their ZVS operation, their turn-off switching losses are still remaining. To decrease these switching losses, small capacitors may be connected in parallel with the MOSFETs’ drain-source [39], [57], [58], in addition to their parasitic capacitances, by turning them off fast and properly considering dead-time subintervals. These switching losses are effectively reduced by increasing the abovementioned capacitances, even when the minimum input voltage is applied to the converter and maximum power is delivered to the load, which is the worst-case condition for turn-off switching losses of the MOSFETs. However, using higher capacitances lead to a narrower ZVS operation range because larger currents are required to fully charge/discharge these capacitors to provide the ZVS condition. Consequently, a proper trade-off between reducing the turn-off switching losses and providing the ZVS condition for reducing the turn-on switching losses must be addressed here for the abovementioned worst-case conditions to overcome this issue in practice. Fig. 8 shows the operational State II, occurring due to the considered dead-time subinterval. Therefore, maximum capacitance value, $C_S$, can be identified as follows:

$$C_S \frac{dv_{C_S}}{dt} = i_{C_S min} = (I_{Lr} - i_{Lr(t_2)})_{min}$$

$$\approx C_{S max} \frac{V_{in max}}{\Delta T}$$

(32)
By keeping in mind that $i_{Lr}(t_2) = i_{Lm}(t_2)$ and using (3), (9), (16), (28), and (32), the maximum capacitance value of $C_S$ can be calculated as follows:

$$C_{S\text{max}} \leq \frac{(1 - D_{\text{min}}) \Delta T}{V_{\text{in max}}} \times \left[ \frac{(1 - D_{\text{min}})T_S}{n(m - 1)\bar{L}_{\text{m}}} + a_2 \right] V_\text{out} - \left( \frac{D_{\text{min}}T_S}{2L} - \frac{T_S}{n(m - 1)\bar{L}_{\text{m}}} - b_2 \right) V_{\text{in max}}$$

(33)

Here, $\Delta T$ is the dead-time value which can be obtained from the datasheet of the used power MOSFET by considering some parameters such as rise and fall times, turn on and off delay times, and body-diode reverse recovery duration time [59].

VI. CALCULATING THE RESONANT TANK COMPONENTS VALUES

Here, a simple approach is used to calculate the converter components values. $V_{C_{\text{out}}}$ is approximately applied to the transformer primary winding because the converter operates near its series resonant frequency. Therefore, the transformer turns ratios can be approximated as follows:

$$n = \frac{V_{C_{\text{out}}}}{V_{C_{\text{out}}}}$$

(34)

So, the transformer turns ratios can easily be identified. Since the output stage capacitors with the same voltages stresses are preferred in practice, the transformer unity turns ratios are considered here. Considering Fig. 9, voltage of $C_r$ changes from minimum to maximum value during $t_x$ to $t_z$ time duration and these values are respectively occurring when $i_{D1}(t_x) = i_{D_{a1}}(t_z) = I_{\text{out}}$ during States I and IV. Therefore,

$$\frac{1}{2n} \left( i_{Lr}(t) - i_{Lm}(t) \right) = \frac{V_\text{out}}{R_L}$$

(35)

Substituting (2), (3), (13), and (14) into (35), $t_x$ and $t_z$ can be obtained numerically. Consequently, peak-to-peak voltage variation of $C_r$ is obtained as follows:

$$\Delta V_{C_r} = \frac{1}{C_r} \int_{t_x}^{t_z} i_{Lr}(t) \, dt$$

$$= \frac{1}{C_r} \left( \int_{t_x}^{t_z} e^{D_T} i_{Lr}(t) \, dt + \int_{D_T}^{t_z} i_{Lr}(t) \, dt + \int_{t_x}^{t_z} i_{Lr}(t) \, dt \right)$$

(36)

Doing some algebraic calculations, $\Delta V_{C_r}$ can be calculated as expressed in (37), shown at the bottom of the next page.
Here, different parameters are given as follows:

\[
\begin{align*}
\kappa_1 &= \chi_1 d_2 - n(m - 1) + 1 \\
\kappa_2 &= T_s + \chi_3 b_2 \\
\kappa_3 &= Z_1^{-1} \sin \left(\omega_0 D T_s\right) \\
\kappa_4 &= Z_1^{-1} \cos \left(\omega_0 D T_s\right) \\
\kappa_5 &= \chi_1 d_2 + n(m - 1) + 1 \\
\kappa_6 &= (1 - D) T_s - \chi_2 a_2 \\
\chi_1 &= n(m - 1 - 1) \\
\chi_2 &= n(m - 1) I_{in} \\
\tau_1 &= \sin \left(\omega_0 D T_s\right) - \sin \left(\omega_0 t_s\right) \\
\tau_2 &= \sin \left(\omega_0 t_s\right) - \sin \left(0.5\omega_0 T_s\right) \\
\tau_3 &= \cos \left(\omega_0 D T_s\right) - \cos \left(\omega_0 t_s\right) \\
\tau_4 &= \cos \left(\omega_0 t_s\right) - \cos \left(0.5\omega_0 T_s\right)
\end{align*}
\]

(38)

Considering (38), and substituting (4) and (7) into (37), \(C_r\) can be identified numerically from (37) for given voltage ripple value under the worst-case condition. Then, for given resonant frequency, \(L_r\) is also simply identified from (4).

**VII. CALCULATING THE OUTPUT STAGE CAPACITORS VALUES**

To limit the output voltage ripple value, the output stage capacitors values must be chosen properly. Fig. 10 shows the different output capacitors voltages ripples and currents waveforms for \(D > 0.5\) during a switching period. Considering these waveforms, the capacitors voltages ripples are calculated. As illustrated in Fig. 10, \(V_{\text{out}1\text{max}}\) is occurred at \(t_y\), which can be identified as follows:

\[
t_y = \frac{(1 - D) T_s}{2}
\]

(39)

Therefore, peak-to-peak voltage variations of \(C_{\text{out}1}\) is identified.

\[
\Delta V_{\text{out}1} = \frac{1}{C_{\text{out}1}} \int_0^{t_y} i_{\text{out}1}(t) \, dt
\]

\[
= \frac{1}{C_{\text{out}1}} \int_0^{t_y} \left[ \frac{1}{\eta} (i_{\text{in}}(t) - i_{\text{in}}(t)) - i_{\text{out}} \right] \, dt
\]

\[
= \frac{1}{C_{\text{out}1}} \left[ \left(\frac{\kappa_2}{\chi_3} + \frac{(1 - D) b_2 k_8 + k_9}{(1 - D) \chi_4} \right) V_{\text{in}}
\right]
\]

\[
+ \left(\frac{\kappa_{10} + a_2 k_8 + k_{11}}{\chi_4} \right) V_{\text{out}}
\]

(40)

\[
\Delta V_{C_r} = \frac{1}{C_r} \left[\frac{b_2 (t_2 - t_1)}{\omega_0} + \frac{C_r \kappa_{1} (t_4 - t_3)}{\chi_1} - \frac{\kappa_2}{\omega_1 \chi_2} \sin \left(\omega_1 (D - 0.5) T_s\right) + \frac{Z_0 \chi_1 b_2 + k_4 k_5}{\chi_1} (D - 0.5) T_s \right] V_{\text{in}}
\]

\[
+ \left(\frac{a_2 (t_2 - t_1)}{\omega_0} + \frac{C_r (\chi_1 c_2 - (1 - D)) (t_4 - t_3)}{\chi_1} \right) + \left(\frac{Z_0 \kappa_{3} a_2}{\chi_1} \right) (D - 0.5) T_s
\]

\[
+ \left(\frac{\kappa_{6}}{\omega_1 \chi_2} \sin \left(\omega_1 (D - 0.5) T_s\right) \right) V_{\text{out}}
\]

(37)

Moreover, \(V_{\text{out}_{2 \ldots m}}\) varies from its minimum to maximum value during \(t_x\) to \(t_p\). Therefore, peak-to-peak voltage variations of \(V_{\text{out}_{2 \ldots m}}\) is obtained as follows:

\[
\Delta V_{\text{out}_{2 \ldots m}} = \frac{1}{C_{\text{out}_{2 \ldots m}}} \int_{t_x}^{t_p} i_{\text{out}_{2 \ldots m}}(t) \, dt
\]

\[
= \frac{1}{C_{\text{out}_{2 \ldots m}}} \times \left[ \left(\frac{\kappa_{12} b_2 t_6 + \kappa_{12} \kappa_{13} \tau_7}{Z_0} \right)
\right.
\]

\[
+ \left. \frac{t_8}{(1 - D)} + \frac{b_2 t_9}{2n} \right) V_{\text{in}}
\]

\[
- \left(\frac{\kappa_{12} a_2 t_6 + \kappa_{12} \kappa_{14} \tau_7}{Z_0} + t_8 - \kappa_{15} t_9 \right) V_{\text{out}}
\]

(42)
where,

\[
\begin{align*}
\kappa_{12} &= \frac{1}{2m} \\
\kappa_{13} &= d_2 + \frac{1}{1} + \frac{1}{n(m-1)}Z_0(1-D) \\
\kappa_{14} &= c_2 - \frac{1}{n(m-1)} \\
\kappa_{15} &= \frac{2d}{1} - \frac{1}{1} \\
\tau_6 &= \sin(\omega_0 t) - \sin(\omega_0 t) \\
\tau_7 &= \cos(\omega_0 t) - \cos(\omega_0 t) \\
\tau_8 &= \frac{t^2 - t^2}{4\pi^2(n-1)}L_{m} \\
\tau_9 &= t_p - t_x
\end{align*}
\]

Also, \( t_p \) can be approximated as follows:

\[
\begin{align*}
t_p &\approx \begin{cases} 
1 - D & D > 0.5 \\
0 & D \leq 0.5
\end{cases} \tag{44}
\end{align*}
\]

Now, for the given voltages ripples values, the output stage capacitors can be identified by considering (40) and (47). Finally, it must be mentioned that voltage stresses of all power MOSFETs are equal to \( V_{C\text{out}} \). Also, each stage output capacitor and diode voltage stresses are the same. Since all output capacitors voltages are almost equal, consequently, all power diodes voltage stresses are also the same. Therefore, each MOSFET, diode, and capacitor voltage stress can be identified.

\[
\begin{align*}
V_{DS} &= \frac{V_{\text{out}}}{m} \\
V_D &= V_{C\text{out}} = \frac{V_{\text{out}}}{m} \tag{45}
\end{align*}
\]

The converter stages number can be identified easily by considering the available devices volt-ratings and the desired output voltage values properly. Because the converter devices entirely operate under the soft switching conditions over wide input voltage and output power variation ranges, the conduction losses are dominant components of the converter losses. Thus, to reduce the converter conduction losses and to improve its efficiency, low volt-rating devices are preferred. Therefore, a trade-off between efficiency, cost, and complexity of the converter must be done to properly identify the converter stage number in practice.

**VIII. EXPERIMENTAL RESULTS**

To confirm the theoretical analyses of the proposed converter, a 1 kW prototype converter has been implemented, as shown in Fig. 11. The implemented converter can step up wide input voltage variation ranges (100-200 V) to be regulated to 1000 V at the output port. Also, its output power varies in a wide range (100 W-1 kW). Here, unlike the conventional LLC resonant converter, where the minimum switching frequency determines the sizes of the converter’s magnetic devices, the switching frequency is fixed at \( f_s = 143 \text{ kHz} \), and the output voltage is regulated by the APWM method, as mentioned before. Therefore, the converter’s magnetic components used in the input filter, resonant inductor, and multi-winding transformer can be designed more appropriately. The specifications of the main parameters of the prototype converter are given in Table 1. Here, the gate driver signals are generated by a STM32F334R8 board. The steady-state experimental waveforms for two worst-case conditions, i.e., \( V_{\text{in}} = 100 \text{ V}, V_{\text{out}} = 1 \text{ kV}, \text{ and } P_{\text{out}} = 1 \text{ kW} \), (a) switch \( M_{S1} \), (b) switch \( M_{S2} \), (c) switch \( M_{S3} \), and (d) switch \( M_{S4} \). (a) switch \( M_{S1} \), (b) switch \( M_{S2} \), (c) switch \( M_{S3} \), and (d) switch \( M_{S4} \).
conditions. So, all MOSFETs turn-on switching losses are effectively eliminated due to their ZVS operation. Switching losses of the MOSFETs are illustrated by the bottommost waveforms of the different parts of Figs. 12 and 13, too.

Also, the bottommost waveforms of Figs. 14 and 15 clearly show that the output stage diodes turn-off switching losses are effectively eliminated due to their ZCS operations that significantly alleviate their reverse recovery problem. Therefore, the soft-switching operation is guaranteed for all power switches of the proposed converter in all input voltage and output power variations ranges. It means that high efficiency, low EMI noises, and high switching frequency operation are achievable. Consequently, high power densities can be realized in practice.

Fig. 16 shows the input inductors currents and the converter input current waveforms under the abovementioned two worst-case conditions. Due to the converter interleaved structure, its input current ripple value is effectively lower than both input inductors current ripple values, as clearly illustrated in Fig. 16. Also, the input current frequency is twice the frequency of both input inductors current waveforms, which is effectively reducing the input filter volume. Fig. 17 shows the resonant tank inductor current and capacitor voltage waveforms under the abovementioned two worst-case conditions when the output voltage is 1 kV. Also, Fig. 18 shows the different output stage capacitors voltages as well as the output stage diodes, experience the same voltage stresses, even when more stages are used to employ either lower volt-rating devices or to achieve higher output voltage values in practice. Also, Fig. 19(a) shows the converter’s different efficiency curves versus output power for different input voltages. Besides, Fig. 19(b) depicts the loss distribution of the proposed converter. Based on Fig. 19(b), although the dominant switching losses of the MOSFETs are eliminated due to soft-switching, most of the losses are related to the conduction losses of the MOSFETs. Thus, by selecting switches with a lower $r_{ds\, on}$ higher efficiencies can be achieved. To gain a deeper insight about this issue, the proposed converter is compared with the most similar converters in Table 2. Although some better efficiencies have been reported in the literature, this is mainly due to their used components with lower conduction losses and switches.

### TABLE 1. Main parameters of the prototype converter.

| Parameter or device | Symbol | Value |
|---------------------|--------|-------|
| Input DC voltage    | $V_{in}$ | 100 V – 200 V |
| Output DC voltage   | $V_{out}$ | 1 kV |
| Output power        | $P_{out}$ | 100 W – 1 kW |
| Input inductors     | $L_a, L_b$ | PQ 32/20 core 50 μH |
| Transformer         | $N_1, N_2, N_3$ | ETD 34/17/11 core 15/15/15 |
| Resonant inductor   | $L_r$ | RMS core 11.8 μH |
| Resonant Capacitor  | $C_r$ | 100 nF |
| Output capacitors   | $C_{out, a, b}$ | 47 μF |
| Capacitors connected in parallel with lower MOSFETs | $C_{a1}, C_{a2}$ | 1 nF |
| Switching frequency | $f_s$ | 143 kHz |
| Power MOSFETs       | $M_{a1}, M_{a2}, M_{b1}, M_{b2}$ | IPP50R140CP |
| Rectifier diodes    | $D_{a1} – D_{a4}, D_{b1} – D_{b4}$ | MUR450 |
TABLE 2. Comparison of the proposed converter with the most similar converters.

| Ref. | No. | DC | R_{on} (mΩ) | V_{in} (V) | DC | L_{b} (μH) | No. | C (μF) | No. | n | Suitable for high power | Suitable for high voltage |
|------|-----|----|-------------|------------|----|------------|-----|--------|-----|---|------------------------|--------------------------|
| [18] | 6   | 120 | 100         | 120        | 6  | -          | 3   | 2×0.141, 2×20 | 1   | 1.85 | NO                     | NO                       |
| [2]  | 4   | 57  | 23          | 1000       | 4  | 1.7        | 3   | 2×2, 2×220  | 1   | 1   | YES                    | NO                       |
| [24] | 4   | 36  | 80          | 800        | 6  | 2.4        | 3   | 0.068, 17, 1500 | 1   | 1   | 96.2 NO                | NO                       |
| [19] | 4   | 69  | 49          | 200        | 8  | 0.975      | 4   | 2×4, 2×50  | 5   | -   | 94.7 YES               | NO                       |
| [52] | 4   | 38  | 75          | -          | -  | -          | 3   | 17.715, 107.54, 108.64 | 1   | 2   | NM YES                 | NO                       |
| [20] | 4   | 31  | 82          | 1000       | 1  | 1.1        | 3   | 0.32, 4×10, 270 | 1   | 1.5 | NM YES                 | YES                      |
| [55] | 8   | 56  | 40          | 600        | 6  | 1.6        | 5   | 2×0.356, 110, 2×440 | 2   | 1.3 | NM YES                 | YES                      |

Proposed 4 23 140 8 500 4 1.28 3 11.8, 2×50 4 0.1, 3×47 1 1 95.3 YES YES

NM: Not Mentioned

FIGURE 16. Converter input current and its input inductors currents waveforms under different conditions: (a) and (b) $V_{in} = 100$ V, $V_{out} = 1$ kV, and $P_{out} = 1$ kW, and (c) and (d) $V_{in} = 200$ V, $V_{out} = 1$ kV, and $P_{out} = 100$ W.

FIGURE 17. Resonant tank inductor current and capacitor voltage waveforms under different conditions (a) $V_{in} = 100$ V and $P_{out} = 1$ kW and (b) $V_{in} = 200$ V and $P_{out} = 100$ W.

FIGURE 18. Output capacitors and regulated output voltages waveforms under different conditions (a) $V_{in} = 100$ V, $V_{out} = 1$ kV, and $P_{out} = 1$ kW and (b) $V_{in} = 200$ V, $V_{out} = 1$ kV, and $P_{out} = 100$ W.

with lower on-state resistances, as clearly given in Table 2. Based on Figs. 12-15, the dominant switching losses of the MOSFETs and diodes are eliminated due to the converter’s soft-switching operation in wide input voltage and output power variation ranges. Effects of the power MOSFETs and diodes conduction losses on the converter efficiency curves have been simulated, as given in Fig. 19(c). These simulation results clearly show that to improve the converter efficiency, different components with low conduction losses can be used. In practice, a trade-off between the converter efficiency and its cost can be done to improve the converter efficiency.
and pay a reasonable cost by choosing low-loss inductors and transformer, low-ESR capacitors, and low voltage drop MOSFETs and diodes.

By considering Table 2, some conclusions are given as follows:

a) Generally, transformers and inductors are massive components that strongly affect the converter’s power densities and prices. However, Table 2 clearly shows that this is a common issue in many dc-dc converters. The soft-switching operation of the converters, which is

### TABLE 1. Comparison of the proposed converter with some different existing topologies.

| Parameters | References | $V_{in}$ (V) | $V_{out}$ (V) | $P_{out}$ (W) | MOSFETs | Diodes | Switching operation | Input Inductance (mH) | Capacitors Capacitance (µF) | Resonant Inductance (µH) | Transformer turn ratio (%) | Peak efficiency (%) | Modulation Strategy |
|------------|------------|--------------|---------------|---------------|---------|--------|---------------------|----------------------|--------------------------|------------------------|------------------------|-----------------|------------------|
| High step-up | [4]        | 200          | 40-80         | 200           | †        | **     | 100                 | 5                    | 6                       | -                      | 0.1795, C            | 11.8            | PWM              |
|            | [9]        | 210          | 25-100        | 250           | NM       | NM     | 80-140              | 6                    | 8                       | -                      | 0.408, 200, 3.16    | 16.2            | 5.64             |
|            | [10]       | 300          | 12-24         | 600           | **       | -      | 50                  | 5                    | 6                       | 500                    | 0.36, C              | 9.3, 9.9         | 12               | 94               | PWM              |
|            | [11]       | 380          | 20-40         | 300           | †        | NM     | 90-180              | 4                    | 4                       | -                      | 0.99, 20, 4x0.001   | 1.1              | 13               | 96               | PFM + PWM         |
|            | [12]       | 400          | 36-57         | 1000          | †        | NM     | 60                  | 5                    | 4                       | 54                     | 4.4, 220, 2x330, 2x560 | 0.4              | 2.92             | 2.75             | PWM              |
|            | [13]       | 400          | 80-200        | 1000          | †        | **     | 80-160              | 4                    | 4                       | -                      | 2x6.141              | 2x0.2           | 0.5              | 97.3             | PFM              |
|            | [14]       | 600          | 100           | 1000          | †        | **     | 200                 | 4                    | 2                       | -                      | 0.22, 4x100          | 2.86             | 1.5              | 97               | PWM              |
| High voltage | [5]        | 1000         | 24            | 600           | **       | **     | 90-100              | 4                    | 4                       | NM                     | 1.2                  | 0.25             | 30               | 92               | PFM              |
|            | [6]        | 2500 (per module) | 240-440       | 5000 (per module) | Ans: †, †† | Main: † | 37.5                           | 10                   | 8                       | -                      | 2x0.1, 4x1         | 2x211           | 3                | 98.8             | PSM              |
|            | [7]        | 8000-10000   | 100           | 325-250       | †        | **     | 32-48               | 4                    | 16                      | -                      | 0.2, 15x3           | 78.5            | 20               | 96               | PFM              |
|            | [8]        | 15000        | 424-636       | 5000          | S_{L2}, L_{2}, ** , S_{L1}, L_{1}, †† | D_{L1}, L_{1}, †† | 20 | 6 | 10 | NM | 0.622, 0.2 | 3.6 | 20 | 93 | PWM |
| Interleaved | [16]       | 100          | 30-30, 64-60  | 600           | †        | **     | 100                 | 6                    | 2                        | 2x100                 | C                      | 5                | 0.75             | 97               | PWM + PSM         |
|            | [2]        | 200          | 25            | 400           | †, ††    | **     | 50                  | 4                    | 4                        | 2x68                  | 2x2, 22, 2x220      | 0.9              | 1                | 96.8             | PSM              |
|            | [17]       | 360          | 65-115, 160-200 | 500           | †        | **     | 74-100              | 4                    | 4                        | 2x159                 | 0.0735, C            | 34.4             | 1.8              | 96               | PSM + PWM         |
|            | [18]       | 380          | 35-45         | 600           | S_{L2}, L_{2}, †, S_{L1}, L_{1}, †† | - | 50 | 6 | 0 | 2x60 | 2x0.141, 2x20 | 35.6 | 1.85 | 97.3 | PWM |
|            | [19]       | 380          | 40            | 1500          | †        | **     | 70 | 4 | 4 | 2x50 | 2x10, 3x20 | 2x4 | - | 94.7 | PWM |
|            | [20]       | 400          | 40-60         | 500           | †        | **     | 60-80               | 4 | 4 | 2x159 | 0.32, 4x10, 270 | 10 | 1.2 | - | 94.6 | PWM |
|            | [21]       | 400          | 20            | 500           | -        | -      | 100                 | 3 | 6 | 3x100 | 3x=8, 2x22, 2x120 | - | - | - | 94.6 | PWM |
|            | [52]       | 60           | 10-20         | 18            | † | - | NM | 4 | 4 | 108.64, 187.54 | 0.133, 10, 100 | 17.715 | 2 | NM | PSM |
|            | [22]       | 48           | 120 RMS       | 350           | †        | **     | 140                 | 4 | 2 | 2x110 | 0.0099, 0.164, 409 | 70 | 0.125 | 92.3 | NM |
|            | [24]       | 400          | 110-220 (PFC) | 1000          | †        | **     | 100                 | 4 | 6 | 2x1000 | 0.068, 17, 1500 | 37 | 1 | 96.2 | PWM |
|            | [23]       | 48           | 35-265 (PFC)  | 300           | †        | **     | 50-119              | 4 | 4 | 2x195 | 0.0133, 120, 660 | 177 | 7.1 | 92.7 | PFM/IAPWM |
|            | [49]       | 20-160       | 12            | 48            | †        | **     | 100                 | 4 | 2 | 2x2000 | 0.053, 100, 200 | 50 | 4.7 | - | NM | NM |
| LLC-based converters | [51]       | 400          | 44-52         | 1000          | †        | **     | 7k-135              | 4 | 4 | 2x24.2 | 2x856, 2x220, 1000 | 2x3 | 3.75 | 93.3 | PFM |
|            | [55]       | 400          | 40-76         | 1200          | †        | **     | NM | 8 | 4 | 4x10 | 2x0.356, 2x440, 110 | 2x14.5 | 1.3 | NM | PWM, PFM |
|            | [53]       | 500-840      | 390           | 1300          | †        | **     | 100                 | 6 | 8 | - | 0.044, 6x150, 2xC | 57 | 2.6 | 95.5 | PFM |
|            | [54]       | 760          | 25-50         | 300           | †        | **     | 75-110              | 6 | 8 | - | 0.62, 6xC | 4.1 | 4 | 96.1 | PFM |

† ZVS turn on, †† ZVS turn off, * ZCS turn on, ** ZCS turn off, C: Unknown, and NM: Not Mentioned

**TABLE 3.** Comparison of the proposed converter with some different existing topologies.
also achieved here, is an efficient approach to overcome this problem and improve the power density and reduce the cost.

b) Number of the active switches and their driver and control circuits are other issues. But, Table 2 clearly shows that the proposed converter is one of the best solutions from this point of view.

c) Input filter and output capacitors are also reduced here due to the given symmetrical configuration.

d) Although more diodes have been used here, as tabulated in Table 2, this is not a significant issue because lower current and voltage stresses are applied to these components, and this issue cannot very much affect the price and power density of the proposed converter in practice.

Fig. 20 shows the dynamic response of the proposed converter when the load changes between 90% and 10%. To have a better clarification, an implemented 3-stage configuration of the proposed converter has been compared in more details in Table 3 with some other existing high step-up, high-voltage, interleaved, and LLC-based converters.

Finally, it must be mentioned that some unavoidable manufacturing mismatches may lead to improper operation of this proposed converter in practice, like many well-known power electronics converters, including interleaved-based topologies. For instance, any mismatches between the input inductors, the power switches of the different legs, their gate-drive circuits, their gate-source generated pulses, and so forth can affect the ideal operation of the proposed converter. This is a well-known issue in the power electronics field, and there are some solutions to overcome this problem. For instance, the average or peak current control approach can easily be used here to overcome this issue. However, the small signal modeling and closed-loop control approach of the proposed converter are ignored and not addressed here in detail to shorten the subject.

IX. CONCLUSION

In this paper, a new expandable high step-up LLC-based converter is proposed. The experimental results clearly show that all its primary stage MOSFETs and output stage diodes are operating under the soft-switching conditions in the entire wide input voltage and output power variation ranges. Therefore, high efficiency and low EMI noises are achievable, and high frequency operation is possible to reduce its passive components volume and thereby increase its power density. Also, integrating a two-phase interleaved current-fed structure with a LLC resonant converter makes it possible to achieve high voltage gain, as well as low input current ripple value. Besides, the input current frequency is twice the switching frequency that effectively reduces the input filter volume in practice. To regulate the output voltage, an asymmetric PWM technique at a fixed switching frequency is used to design the converter magnetic components, including input filter, resonant inductor, and multi-winding transformer, more effectively. A 1 kW prototype converter has also been implemented to verify the given analyses results. Wide input voltage 100-200 V, and output power 100-1000 W variations are applied to the converter. The APWM technique at 143 kHz switching frequency is used to regulate the output voltage at 1 kV.
[35] R. Suryadevara and L. Parsa, “FB-ZCS DC–DC converter with dual-capacitor resonant circuit for renewable energy integration with MVDC grids,” *IEEE Trans. Ind. Appl.*, vol. 56, no. 6, pp. 6792–6802, Nov. 2020, doi: 10.1109/TIA.2020.3016926.

[36] J. Liu, Z. Zheng, K. Wang, and Y. D. Li, “Comparison of boost and LLC converter and active clamp isolated full-bridge boost converter for photovoltaic DC system,” *IET Power Electron.*, vol. 2019, no. 16, pp. 2236–2244, 2019, doi: 10.1049/joe-1.2018.8507.

[37] J. Deng, C. C. Mi, R. Ma, and S. Li, “Design of LLC resonant converters based on operation-mode analysis for level two PHEV battery chargers,” *IEEE/ASME Trans. Mechatronics*, vol. 20, no. 4, pp. 1595–1606, Aug. 2015, doi: 10.1109/TMECH.2014.243979.

[38] X.-F. Cheng, C. Liu, D. Wang, and Y. Zhang, “State-of-the-art review on soft-switching technologies for non-isolated DC-DC converters,” *IEEE Access*, vol. 9, pp. 119235–119249, 2021, doi: 10.1109/ACCESS.2021.3107861.

[39] R. Beiravan, “Analysis of a switched-capacitor converter above its resonant frequency to overcome voltage regulation issue of resonant SCs,” *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5315–5325, Sep. 2016, doi: 10.1109/TIE.2016.2561170.

[40] A. Awasthi, S. Bagawade, A. Kumar, and P. Jain, “An exact time domain analysis of DCM boost mode LLC resonant converter for PV applications,” in *Proc. IEEE 44th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2018, pp. 1005–1010, doi: 10.1109/IECON.2018.8591854.

[41] H.-D. Gu, Z. Zhang, X.-F. He, and Y.-F. Liu, “A high voltage-gain LLC micro-converter with high efficiency in wide input range for PV applications,” in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2014, pp. 637–642, doi: 10.1109/APEC.2014.6803575.

[42] H. Xu, Z. Yin, Y. Zhao, and Y. Huang, “Accurate design of high-efficiency LLC resonant converter with wide output voltage,” *IEEE Access*, vol. 5, pp. 26653–26665, 2017, doi: 10.1109/ACCESS.2017.2757764.

[43] Y. Shen, W. Zhao, Z. Chen, and C. Cai, “Full-bridge LLC resonant converter with series-parallel connected transformers for electric vehicle on-board charger,” *IEEE Access*, vol. 6, pp. 13490–13500, 2018, doi: 10.1109/ACCESS.2018.2811760.

[44] M. F. Menke, J. P. Duranti, L. Roggia, F. E. Bisogno, R. V. Tambara, and A. R. Seidel, “Analysis and design of the LLC LED driver based on state-space representation direct time-domain solution,” *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12666–12701, Dec. 2020, doi: 10.1109/TPEL.2020.2959542.

[45] M. F. Menke, Á. R. Seidel, and R. V. Tambara, “LLC LED driver small-signal modeling and digital control design for active ripple compensation,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 387–396, Jan. 2019, doi: 10.1109/TIE.2018.2829683.

[46] C. Li, Y. Zhang, Z. Cao, and D. Xu, “Single-phase single-stage isolated ZCS current-fed full-bridge converter for high-power AC/DC applications,” *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6800–6812, Sep. 2017, doi: 10.1109/TPEL.2016.2537764.

[47] Y. Wei, Q. Luo, X. Du, N. Altin, J. M. Alonso, and H. A. Mantooth, “Analysis and design of the LLC resonant converter with variable inductor control based on time-domain analysis,” *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5432–5443, Jul. 2020, doi: 10.1109/TIE.2019.2934085.

[48] J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, *Principles of Power Electronics*. Boston, MA, USA: Addison-Wesley, 1991.

[49] H. Setiai and H. Fujita, “Reduction of switching power losses for ZVS operation in switched-capacitor-based resonant converters,” *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 1104–1115, Jan. 2021, doi: 10.1109/TPEL.2020.3001956.

[50] R. Beiravan, B. Rashidian, M. R. Zolghadri, and S. M. H. Alavi, “Optimizing the normalized dead-time and maximum switching frequency of a wide-adjustable-range LLC resonant converter,” *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 462–472, Feb. 2011, doi: 10.1109/TPEL.2010.2068563.

[51] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. New York, NY, USA: Springer, 2001.

**DANESH AMANI** (Member, IEEE) received the M.Sc. degree in power electronics engineering from Tarbiat Modares University, Tehran, Iran, in 2021. His current research interests include step-up dc–dc converter, LLC-based resonant converter, soft-switching techniques, and PV-based renewable energy systems.

**REZA BEIRANVAND** (Senior Member, IEEE) received the M.Sc. and Ph.D. degrees in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 1999 and 2010, respectively. From 1999 to 2007, he was an Engineer at the Research and Development Centers of PARS-Electric and RADIO SHAHAB MFGs, Tehran, where he was engaged in designing the LCD, and LED TVs based on the ST, LT, NXP, and Fairchild devices. From 2010 to 2012, he was a Postdoctoral Research Fellow with the Faculty of Electrical Engineering, Sharif University of Technology. He was the IEEE Consultant (2017–2019) and the Head of the Power Group (2018–2020) with Tarbiat Modares University, Tehran. He is currently an Associate Professor at the Faculty of Electrical and Computer Engineering, Tarbiat Modares University. He is among the “Top 2 Percent Scientists of the World,” based on what is called Stanford University Released List in Elsevier, in 2020 and 2021. His research interests include power electronics converters, soft switching techniques, SCCS, SMPS, capacitive-coupling power transfer (CPT) and inductive power transfer (IPT) techniques, and PV-based renewable energy systems.
MOHAMMADREZA ZOLGHADRI (Senior Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 1989 and 1992, respectively, and the Ph.D. degree in electrical engineering from the Institute National Polytechnique de Grenoble (INPG), Grenoble, France, in 1997. In 1997, he joined the Department of Electrical Engineering, Sharif University of Technology. From 2000 to 2003, he was a Senior Researcher with the Electronics Laboratory of SAM Electronics Company, Tehran. From 2003 to 2005, he was a Visiting Professor with North Carolina A&T State University, USA. He is currently an Associate Professor and the Head of the Power System Group, Department of Electrical Engineering, Sharif University of Technology. He is the Founder and the Head of the Electric Drives and Power Electronics Laboratory (EDPEL), Sharif University of Technology. He is the author of more than 100 publications in power electronics and variable speed drives. His research interests include application of power electronics in energy systems, modeling, and control of power electronic converters and variable speed drives. He has been a member of the Founding Board of Power Electronics Society of Iran (PESI) and the Chairman of the Board of PELSI, since February 2019.

FREDE BLAABJERG (Fellow, IEEE) received the Ph.D. degree in electrical engineering from Aalborg University, in 1995. He is currently pursuing the Honoris Causa degree with University Politehnica Timisoara (UPT), Romania, and Tallinn Technical University, Estonia. He was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. He became an Assistant Professor, an Associate Professor, and a Full Professor of power electronics and drives with Aalborg University, in 1992, 1996, and 1998, respectively. In 2017, he became a Villum Investigator. He has published more than 600 journal articles in the fields of power electronics and its applications. He has coauthored four monographs and an editor of ten books in power electronics and its applications. His current research interests include power electronics and its applications, such as in wind turbines, PV systems, reliability, harmonics, and adjustable speed drives. He has received 33 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019, and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS, from 2006 to 2012. He has been a Distinguished Lecturer for the IEEE Power Electronics Society, from 2005 to 2007, and the IEEE Industry Applications Society, from 2010 to 2011 and from 2017 to 2018. From 2019 to 2020, he served as the President of the Danish Academy of Technical Sciences. From 2014 to 2020, he was nominated by Thomson Reuters to be between the most 250 cited researchers in Engineering in the world.