Non-floating and low-power adiabatic logic circuit

Mei Han\textsuperscript{1)}, Yasuhiro Takahashi\textsuperscript{2)}, and Toshikazu Sekine\textsuperscript{2)}

Abstract This paper proposes a new adiabatic logic. Adiabatic logic is a good method to reduce power consumption. Several common adiabatic logics suffer from floating output which results in lack in robustness, by using the periodic power supply. At first, we analyze the floating phenomenon of previously proposed 2PC2AL in this paper. The proposed adiabatic logic can prevent the floating of the nodes to add two logic switches between the power supply and charging-discharging transistor. This paper also reports a comparison of energy dissipation between the different adiabatic logics such as, ECRL, 2N2N2P, 2PASCL, 2PC2AL, and the proposed circuit. In the SPICE simulation, the target application is a 4-bit multiplier for IoT products. Through the simulation, the output of the proposed circuit with cascade connection has a stable function.

Keywords: adiabatic logic, non-floating output, low power, energy recovery logic

Classification: Integrated circuits

1. Introduction

Low power consumption has become a common requirement of the modern electronic systems. It can improve the overall performance of the product, enhance the market competitiveness of the product, and have significant social and economic benefits.

Adiabatic logic has been implemented on low-power electronic circuits, which means that reversible logic having better energy efficiency than static CMOS logic as proved by formers \cite{1, 2, 3, 4, 5, 6, 7, 8, 9, 10}. The 2PC2AL (2-Phase Clocked CMOS Adiabatic Logic) belongs to the Quasi-adiabatic logic that has two sinusoidal waveforms and has a similar simple structure as static CMOS circuit. In Ref. \cite{11}, we can see that the 2PC2AL has ultra-low power consumption compared to the conventional CMOS and other adiabatic logic circuits. However, the main disadvantage of 2PC2AL is that the output node may be floating because of the two sinusoidal waveforms that benefits the energy saving. With floating, the output voltage will be indeterminate, catch any noise, and may change as time passes which is an uncertain factor to the circuit.

In Ref. \cite{12}, a new circuit based on the 2PC2AL has been proposed which solves the problem of floating of 2PC2AL and has been proved to have lower power consumption compared to the static CMOS. This paper is an extension of Ref. \cite{12}. Here we will analyze the timing chart of the non-floating circuit in detail and check the proper switch on time. And then we will compare the energy dissipation of a 4-bit multiplier of the different adiabatic logics, that is, 2N2N2P \cite{13, 14, 15}, 2PC2AL \cite{11}, ECRL (Efficient Charge Recovery Logic) \cite{16, 17, 18}, 2PASCL (Two-phase Clocked Adiabatic Static CMOS Logic) \cite{19, 20, 21}, and our previously proposed circuit \cite{12} in the SPICE simulation.

2. Adiabatic theory

In conventional CMOS circuits, the dynamic energy consumption is an important component of the overall power consumption of the circuits, and it can even become a major part of the dissipation. In the dynamic consumption, the power dissipation primarily occurs during the flip process of switching. Fig. 1 reflects the conventional CMOS inverter and the equivalent circuit including a resistor and a parasitic capacitance \(C\) in a non-ideal circuit. The energy drawn from the power supply is \(CV_d^2\) \cite{22, 23}.

Assuming that the energy drawn from the power supply is equal to that supplied to \(C\), the energy stored in \(C\) becomes half of the supplied energy, which is \(1/2CV_d^2\) and called as non-adiabatic power consumption if released to the ground. The remaining half energy is dissipated in resistance \(R\) as adiabatic power consumption.

The main feature of the adiabatic logic technology is that it can reduce the power consumption of the circuit at the circuit level. It uses a step or pulse voltage source to power the circuit, while the traditional CMOS circuit uses a DC voltage source as a power supply. By using slow raising/falling step or pulse voltage, it can significantly be reduced the power consumption of the load resistor when charging and discharging the power circuit as shown in Fig. 1(c). Sinusoidal source is widely used in the adiabatic logic from the point of view of power clock circuit configuration, hence we consider that the power source of the

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\textsuperscript{1}Graduate School of Engineering, Gifu University, 1–1 Yanagido, Gifu-shi 501–1193, Japan
\textsuperscript{2}Department of EECE, Faculty of Eng., Gifu University, 1–1 Yanagido, Gifu-shi 501–1193, Japan

a) v3814001@edu.gifu-u.ac.jp

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\begin{figure}[h]
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\includegraphics[width=\textwidth]{fig1}
\caption{(a) Structure of conventional CMOS inverter. (b) Equivalent circuits for CMOS and adiabatic inverters. (c) Current for equivalent circuits.}
\end{figure}
conventional 2PC2AL or the proposed circuit is a sinusoidal. We can obtain the dissipated energy, where $\tau$ is the ramping time of the ramped step voltage $V_{dd}$:

$$E_{\text{diss}} = \frac{RC}{\tau} CV_{dd}^2$$

When $\tau$ is significantly greater than $RC$, the energy dissipation can reach close to zero. In addition, it can recover the used electrical charge back to the power supply which means there is no non-adiabatic power consumption. In theory, this part dissipation can be fully given back to the power supply. The conventional CMOS circuits directly discharge this portion of the charge to ground, which not only consumes the power of the circuit, but also generates heat loss.

### 3. Fundamental theory of 2PC2AL

The 2PC2AL inverter is shown in Fig. 2. The inverter uses two-phase clocking split-level sinusoidal power supplies, $V_p$ and $V_n$. One clock is in-phase while the other is inverted. The two voltages change synchronously: one goes up and the other goes down, meanwhile providing logic high and logic low voltages and minimizing the voltage difference among the electrodes in the circuit. The power consumption can be suppressed compared to $V_{dd}$ power supply by using two peak-to-peak voltages of $V_{dd}/2$. With low-level and high-level inputs, the transistors P1 and N1 operate alternately. The waveform of the power supply can be classified into two modes: charging and discharging. When the input is low, transistor P1 works by creating a conducting road from output to the power, hence the $V_{out}$ is charged by $V_p$ to the peak of $V_p$ and then discharged to the wave trough. Thus, we can get a high-level output voltage. With high-level input, P1 turns close, N1 works, and the output port follows power supply $V_n$ by charging and discharging. The voltages $V_p$ and $V_n$ work as power supply and clock. There is no need to consider phase lag which increases the complexity of circuit design.

#### 3.1 Floating phenomenon

The two peak-to-peak voltages $V_p$ and $V_n$ provide a continued voltage supply to the output. The output can be charged or discharged through the transistor P1 and N1 when the signal $IN$ is low or high. But when the signal $IN$ changes from low to high or contrarily, there is always a period when P1 and N1 are both off, called noise-intolerable zone as shown in Fig. 3(a).

When both P1 and N1 are off, the $V_{out}$ becomes floating. With floating, the output voltage will be indeterminate, catch any noise, and may change as time passes which is an uncertain factor to the circuit. To check the correctness of output with noise sources, we made some experiments based on [24, 25]. As shown in Fig. 3(b), we add white noise into the clocks and get incorrect outputs in the marked zone due to the influence of noise during the floating period.

### 4. Proposed non-floating 2PC2AL logic

In this section, a new logic switch based on 2PC2AL is proposed by adding two switches to prevent the voltage difference from getting lower than the critical value as shown in Fig. 4. The simulation parameters are shown in Table I. From the analysis above, the floating occurs when the input changes, or when the clocks $V_p$ and $V_n$ are approaching to each other. Before the floating occurs, the $V_s$ turns high and the $V_{sb}$ turns low as shown in Fig. 5(a), and as a result the added transistors P2 and N2 get off. This data is kept until the condition changes and the floating is prevented. To ensure the switch takes place on time $t_s$ (the time maintaining high level of $V_s$ in one cycle), the function and the energy consumption of the proposed circuit are checked when the $t_s$ goes from 10 ns to 500 ns in SPICE. Fig. 5(b) shows the consumption relationship: the energy consumption increases as the switch is extended on time. Thus, we set the $t_s$ as 100 ns when the clock frequency is 1 MHz.
The simulation result of the proposed 2PC2AL inverter by using the 0.18 µm technology is shown in Fig. 4(b), when the switch on time, or the high time of \( V_s \), is 0.1 μs. When the input is 0, the transistor P1 works, and N1 is off, the output is charged by the clock \( V_p \). Before the input increases to the threshold voltage, \( V_s \) changes from 0 to 1 and \( V_{sb} \) changes from 1 to 0, and then transistors P2 and N2 are turned off. Here, the voltage of the output can not be controlled by the input and has to be kept in the high voltage level. When the voltage increases over the margin period by 0.1 μs, \( V_s \) turns from 1 to 0, \( V_{sb} \) turns from 0 to 1, and the transistors P2 and N2 are turned on. Thus, the output continues the charging and discharging process through N1. The floating has been avoided.

5. Application and simulation results in 4 bit multiplier

5.1 Fundamental circuits

In this part we design and simulate NAND [26], XOR, half adder and full adder circuit in SPICE by using our proposed method. Fig. 6 shows the 2PC2AL NAND logic circuit and simulation result in SPICE by using the 0.18 µm technology. When the input A or B is zero, at least one pMOS opens with making a conductive path between the power source \( V_p \) and output is charged to high level voltage. Only when A and B are both high voltage, the channel between the output port and power source \( V_n \) can be turned on and the output is discharge to low level voltage that realizing the function of NAND gate.

Same with proposed 2PC2AL inverter circuit, we add two switches into the 2PC2AL NAND circuit as shown in Fig. 7(a) getting a proposed NAND circuit. When the power sources get closest, or input signals change from zero to high, the switches work and avoid floating phenomenon. Fig. 7(b) indicates that the circuit can realize the function of NAND gate.

Fig. 8(a) shows the 2PC2AL XOR logic circuit. When both of inputs A and B are high or low level voltage, the channel between output and power source \( V_n \) opens, and we can get a low level voltage. When the input of A and B are different, the out is connected to power supply \( V_p \) and charged to high level voltage that realizes the logic function of XOR gate. Fig. 8(b) indicates the correctness function of XOR gate. Similarly, we can design the proposed XOR gate as Fig. 9(a) with two switches. Fig. 9(b) is the simulation result in SPICE by using the 0.18 µm technology.

### Table 1. Parameters in 0.18 µm process

| Parameter     | Value                  |
|---------------|------------------------|
| CMOS size     | \( W/L = 0.6 \mu m/0.18 \mu m \) |
| \( V_{ss}, V_{sd} \) | 1.8 V                  |
| \( f_p \)     | \( f_{sl}/2-2V_{dd} \) 2 MHz |
| \( f_n \)     | \( 0-V_{dd}/2, 2 \) MHz |
| Clock         | 1 MHz                  |
| \( t_{rise(IN)}, t_{fall(IN)} \) | 10 ns                  |
Fig. 10 shows the block diagram and simulation result for half adder and full adder by using NAND and XOR logic we mentioned above [27, 28, 29]. From the simulation result in Fig. 11 of the adders, they can realize the logic function correctly.

5.2 4-bit multiplier
We apply the proposed circuits into 4-bit array multiplier which consists of sixteen NANDs, sixteen buffers, six full adders and four half adders as shown in Fig. 12 [30, 31, 32]. A0 to A3 and B0 to B3 are input signals while P7 to P0 are the outputs. For the least significant bit P0, it is determined by the product of input a0 and b0. P1 is determined by sum of a0 \times b1 and a1 \times b0. P2 is determined by a2 \times b0, a1 \times b1, a0 \times b2 and the carry signal from upper half adder, so that we use a full adder ensuring the signals are all included. Then we can get all the output signals from P7 to P0.

The function of the multiplier can be realized in the SPICE simulation as shown in Fig. 13 where the parameters are the same with Table I. In Fig. 14, we can get clear output of the re-time by DFF sampling. Fig. 15 shows the energy comparison of the multipliers when the transistor frequency increases from 10 kHz to 100 MHz in SPICE using the 0.18 \mu m technology. However, the circuits cannot work in higher frequencies than 100 MHz. Because higher frequency will cause logical error, the circuit become unable to implement the specified logic function. Most of adiabatic circuits have lower energy consumption in only low frequency domain. Therefore, considering the efficient working frequency, the proposed circuit can be used in proper frequency domain, such as RFID, smart cards, sensors and so on.

Fig. 10. (a) Structure of half adder circuit. (b) Structure of full adder circuit.

(a) (b)

Fig. 11. (a) Simulation result of half adder circuit. (b) Simulation result of full adder circuit.

(a) (b)

Fig. 12. Structure of 4-4 array multiplier.

Fig. 13. Simulation result of 4-4 array multiplier (1 MHz).
the number of transistors in inverter is four which is the medial level among the inverters. There is no floating in the proposed circuit as shown in Fig. 14.

From the simulation results and energy check, we can draw the merits of the proposed 2PC2AL circuit:
1) It can overcome the disadvantage of floating of the 2PC2AL eliminating an uncertain factor for the circuit.
2) The energy consumption gets lower than the static CMOS circuit.
3) The structure of proposed 2PC2AL circuit is simple relatively.

6. Conclusion
In this paper, the 4 bit array multiplier was realized by the proposed non-floating adiabatic logic. The comparison among ECRL, 2N2N2P, 2PASCL, 2PC2AL and the previously proposed circuit is drawn and shows the advantage of the proposed circuit: it can realise the logic function without floating phenomenon and has relatively small power consumption.

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