The Normalized Singular Value Decomposition of Non-Symmetric Matrices Using Givens fast Rotations

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Abstract—In this paper we introduce the algorithm and the fixed point hardware to calculate the normalized singular value decomposition of a non-symmetric matrices using Givens fast (approximate) rotations. This algorithm only uses the basic combinational logic modules such as adders, multiplexers, encoders, Barrel shifters (B-shifters), and comparators and does not use any lookup table. This method in fact combines the iterative properties of singular value decomposition method and CORDIC method in one single iteration. The introduced architecture is a systolic architecture that uses two different types of processors, diagonal and non-diagonal processors. The diagonal processor calculates, transmits and applies the horizontal and vertical rotations, while the non-diagonal processor uses a fully combinational architecture to receive, and apply the rotations. The diagonal processor uses priority encoders, Barrel shifters, and comparators to calculate the rotation angles. Both processors use a series of adders to apply the rotation angles. The design presented in this work provides 2.83 ∼ 6.49 times better energy per matrix performance compared to the state of the art designs. This performance achieved without the employment of pipelining; a better performance advantage is expected to be achieved employing pipelining.

I. INTRODUCTION

Emerging technologies require a high performance, low power, and efficient solution for singular value decomposition (SVD) of matrices. A High performance and throughput hardware implementation of SVD is necessary in applications such as linear receivers for 5G MIMO telecommunication systems [1], various real-time applications [2], classification in genomic signal processing [3], and learning algorithm in active systems [1], various real-time applications [2], classification in such as linear receivers for 5G MIMO telecommunication hardware implementation of SVD is necessary in applications (SVD) of matrices. A High performance and throughput algorithm and the fixed point hardware to calculate the normalized singular value decomposition of a non-symmetric matrices using Givens fast (approximate) rotations. This algorithm only uses the basic combinational logic modules such as adders, multiplexers, encoders, Barrel shifters (B-shifters), and comparators and does not use any lookup table. This method in fact combines the iterative properties of singular value decomposition method and CORDIC method in one single iteration. The introduced architecture is a systolic architecture that uses two different types of processors, diagonal and non-diagonal processors. The diagonal processor calculates, transmits and applies the horizontal and vertical rotations, while the non-diagonal processor uses a fully combinational architecture to receive, and apply the rotations. The diagonal processor uses priority encoders, Barrel shifters, and comparators to calculate the rotation angles. Both processors use a series of adders to apply the rotation angles. The design presented in this work provides 2.83 ∼ 6.49 times better energy per matrix performance compared to the state of the art designs. This performance achieved without the employment of pipelining; a better performance advantage is expected to be achieved employing pipelining.

1) The hardware implementation requires floating-point arithmetic.
2) The algorithm only works for symmetric matrices.
3) Using this method the BLV algorithm loses its quadratic convergence speed (quadratic to number of sweeps).
4) The proposed algorithm does not provide the “Normalized” results.

In this work we address the disadvantages of Givens fast rotations. The proposed hardware does not require the floating-point arithmetic, and as the result, it does not need the pre-processing (alignment of exponents) and post-processing (renormalization of matrices) blocks mentioned in implementations of Givens fast rotation. The algorithm that we proposed is able to handle symmetric as well as non-symmetric matrices (calculating the rotations for non-symmetric matrices require the calculation of two intermediate variable angles, proximate calculation of these two intermediate variables
makes the calculation of rotation angles challenging and we were able to offer an adaptive solution for it. Also, the proposed algorithm provides the "Normalized" results. The rest of this work is organized as follows: First we introduce the method to merge the NSVD algorithm \([8]\) with Givens fast rotations and Delsome double rotations method \([24]\). The result (ERNSVD algorithm) is similar to the Gotze work in \([23]\) to find the Eigenvalues of a symmetric matrix except the algorithm is able to calculate the decomposition of a non-symmetric matrix. In addition we introduce a method that directly calculates the horizontal and vertical fast rotations using the Forsythe and Henrici SVD (FHSVD) algorithm and called it expedite rotations SVD (ERFHSVD) \([8]\). We use the Givens fast rotations and Delsome double rotations method \([24]\) to reduce the implementation complexity. In this section rotations presented in \([23]\) and double rotation by Delsome FHSVD algorithm presented in \([8]\). We use the Givens fast rotations do not symmetrize a more symmetric matrix with each rotation or they reduce or diagonalize the matrix in one rotation, in fact they generate the off-diagonal norm of the matrix; using this method the algorithm calculates the horizontal (\(\Theta\)) and vertical (\(\theta\)) rotations. The NSVD algorithm calculates the first rotation to symmetrize the matrix using \([2]\) and then using \([3]\) generates the diagonalizing rotations.

\[
\rho = \tan^{-1}\left(\frac{c+b}{d-a}\right) \quad (2)
\]

\[
B = R_\rho \times A = \begin{bmatrix} \cos(\rho) & -\sin(\rho) \\ \sin(\rho) & \cos(\rho) \end{bmatrix} \begin{bmatrix} a & b \\ c & d \end{bmatrix} = \begin{bmatrix} p & q \\ q & r \end{bmatrix} \quad (3)
\]

\[
\phi = \tan^{-1}\left(\frac{2q}{q-p}\right) \quad (4)
\]

\[
\Sigma = R_\phi^T \times B \times R_\phi = \begin{bmatrix} d_1 & 0 \\ 0 & d_2 \end{bmatrix} \quad (5)
\]

The FHSVD algorithm first calculates the \(\alpha\) and \(\beta\) using \([5]\) and \([7]\) as the intermediate values, and using \([8]\) and \([9]\) the algorithm calculates the horizontal (\(\Theta\)) and vertical (\(\theta\)) rotations. In the last step FHSVD algorithm swaps the values of \(\sin\) and \(\cos\) and change the sign of these values if needed to make sure \(d_1 \geq d_2\).

\[
\alpha = \tan^{-1}\left(\frac{c+b}{d-a}\right) \quad (6)
\]

\[
\beta = \tan^{-1}\left(\frac{c-b}{d+a}\right) \quad (7)
\]

\[
\Theta = \frac{\alpha + \beta}{2} \quad (8)
\]

\[
\theta = \frac{\alpha - \beta}{2} \quad (9)
\]

\[
\Sigma = R_\phi^T \times A \times R_\Theta = \begin{bmatrix} d_1 & 0 \\ 0 & d_2 \end{bmatrix} \quad (10)
\]

\[
\begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix}^T \begin{bmatrix} a & b \\ c & d \end{bmatrix} = \begin{bmatrix} \cos(\Theta) & \sin(\Theta) \\ -\sin(\Theta) & \cos(\Theta) \end{bmatrix} \quad (11)
\]

\[\text{Sign}(x) = \begin{cases} 1 & \text{if } x \geq 0 \\ -1 & \text{if } x < 0 \end{cases} \quad (12)\]

\[\exp_2(x) = \begin{cases} (0, 0) & \text{if } x = 0 \\ ([\log_2|x|], 1) & \text{if } x \neq 0 \end{cases} \quad (13)\]

There are two measures that are normally used in different Jacobi based decomposition.

1) The approximation error \(|\epsilon|\) in \([23]\) for a \(2 \times 2\) symmetric matrix defined as the absolute value of off
diagonal element before and after the application of \( k^{th} \) rotation \((13)\). The smaller \(|d|\) shows a more accurate approximation.

\[
|d| = \left| \frac{q(k+1)}{q_k} \right| \tag{13}
\]

This is applied to the \( 2 \times 2 \) matrix, and \(|d|_{\text{Max}} < 1\) is called error bound and is one of the two conditions to assure the convergence of the algorithm. The other condition is to keep the orthogonality of the rotation matrix. We plan to apply this measures to non-symmetric matrices so we extend the equation \((13)\) to \(|D|\). Note that \(|d|\) is the same as \(|D|\) if the matrix is symmetric.

\[
|D| = \sqrt{b_{k+1}^2 + c_{k+1}^2} \tag{14}
\]

The approximation error (as the dependent variable) is normally measured for different values of \(\tau\) (as the independent variable) as defined in \((15)\).

\[
\tau = \frac{\tau - p}{2q} \tag{15}
\]

To extend equation \((15)\) to an independent variable applicable to non-symmetric matrices, we define \(\tau_1\) and \(\tau_2\) in \((16)\) and \((17)\) accordingly. \(\frac{1}{\tau_2} = 0\) and \(\tau_1 = \tau\) if the matrix is symmetric.

\[
\tau_1 = \frac{d - a}{b + c} \tag{16}
\]

\[
\tau_2 = \frac{d + a}{b - c} \tag{17}
\]

2) The Norm of the off-diagonal elements of a matrix versus (Vs.) the number of sweeps is the second metric used for measuring the quality of any fast rotation methods as well as the comparison of the diagonalization speed in different methods. In [23] this value is calculated for a \(70 \times 70\) matrix. The elements of matrix are randomly generated numbers of normal distribution. We run the same test for 100 times and calculate the RMS (root mean square) of the off-diagonal norms \(\text{RMS}_{\text{ODN}}\) to keep the comparability and also keep the result accurate.

Figure 1 shows the Off-diagonal Norm of a \(70 \times 70\) vs. number of sweeps for the fast rotations (dotted curve) and the original Givens rotations (solid line). The dashed lines show the accuracy achievable by different number of bits. This figure provided in [23] is to support the fast rotations method with the following explanation: While achieving the accuracy of 16 bits or better; the original method requires seven iterations versus twelve iterations in the fast rotation method. One must realize that the calculation of 16-bit exact sine and cosine values requires more complexity. As an example if the sine and cosine are implemented using CORDIC method, it requires 16 inner iteration to calculate these values. In the next two subsections we will present two algorithms that are basic blocks of eminent rotations NSVD (ERNSVD).

A. Symmetrizing Algorithm

Algorithm 1 is the approximation to the rotation angle achieved from equation \((2)\). Boundaries in Step 2 of the algorithm are based on the suggestion in \([22]\) that guaranties \(|d| \leq \frac{1}{3}\). Authors in [23] explain that using Delsome double rotations this limit does not hold any more (this method will guaranties \(|d| \leq \frac{7}{12}\); however, the authors explain that this is not an issue since the approximation error merges to the original bounds when the rotation angles get smaller. It should be mentioned that the bounds to approximation error is still less than one.

B. Diagonalizing Algorithm

Algorithm 4 is the approximation to the rotation angle achieved from equation \((4)\). Figure 2 demonstrates the \(|D|\) vs. \(\tau\) when Algorithm 4 is applied on a symmetric matrix. Figure 3 demonstrates the \(|D|\) vs. \(\tau_1\) and \(\tau_2\) when Algorithm 4 is applied on a non-symmetric matrix with ideal symmetrizing rotations. The fast rotations NSVD (FRNSVD) algorithm is based on applying the fast symmetrizing and fast diagonalizing algorithms on a given matrix.

Figure 4 demonstrates the \(|D|\) vs. \(\tau_1\) and \(\tau_2\) when Algorithm 1 and Algorithm 4 is applied on a non-symmetric matrix. The approximation errors are typically higher in this method when compared to Figure 5. This increase in the approximation error is expected since the approximation error of two algorithms can boost the total approximation error. Figure 6 compares the \(\text{RMS}_{\text{ODN}}\) for NSVD, FRNSVD, and ERNSVD. The error floor that happens in iterations 19th and after in ERNSVD, and FRNSVD are due to the fixed point (32 bit) implementation of the algorithm.

C. Relaxing the Boundary Conditions

Implementing the case statement in Step 2 of both algorithms beside the two comparators requires two Barrel shifters, two adders to calculate the coefficients of \(N\) and an adder to calculate \(1.5 \times D\). We can reduce the complexity of...
Algorithm 1 Algorithm to Calculate the Symmetrizing Fast Rotations for Non-Symmetric Matrices.

**Input:** A.

**Output:** Rotation Matrix $R_{\tilde{\phi}}$.

**Step 1:** Calculate the initial values:

\[
S_N = \text{Sign}(b - c) \\
S_D = \text{Sign}(d + a) \\
N = \vert b - c \vert \\
D = \vert d + a \vert \\
K = \exp_2(D) - \exp_2(N)
\]

**Step 2:** Calculate $l_{\tilde{\phi}}$ using following case statement:

\[
l_{\tilde{\phi}} = \begin{cases} 
K + 1 & \text{if } 1.5 \times D > (2^{K+1} - 2^{-K}) \times N \\
K - 1 & \text{if } 1.5 \times D < (2^K - 2^{-K+1}) \times N \\
K & \text{default}
\end{cases}
\]

\[
l_{\tilde{\phi}} = \max(l_{\tilde{\phi}} + 1, 1)
\]

**Step 3:** Calculate the $(c, s)$ pair using the following case statement:

\[
(1, 0) \quad \text{if } N = 0 \\
(0, 1) \quad \text{if } D = 0 \\
\left(\frac{1}{1 + 1 / t_{\tilde{\phi}}} \times (1 - t_{\tilde{\phi}}^2), 2 \times S_N \times S_D \times t_{\tilde{\phi}}\right) \quad \text{default}
\]

**Step 4:** Calculate the Symmetrizing $R_{\tilde{\phi}}$:

\[
R_{\tilde{\phi}} = \begin{bmatrix} c & s \\ -s & c \end{bmatrix}
\]

---

**Algorithm 2** Algorithm to Calculate the fast Diagonalizing Rotations for Symmetric Matrices.

**Input:** B.

**Output:** Rotation Matrix $R_{\tilde{\phi}}$.

**Step 1:** Calculate the initial values:

\[
S_N = \text{Sign}(b + c) \\
S_D = \text{Sign}(d + a) \\
N = \vert c + b \vert \\
D = \vert d - a \vert \\
K = \exp_2(D) - \exp_2(N)
\]

**Step 2:** Calculate $l_{\tilde{\phi}}$ using following case statement:

\[
l_{\tilde{\phi}} = \begin{cases} 
K + 1 & \text{if } 1.5 \times D > (2^{K+1} - 2^{-K}) \times N \\
K - 1 & \text{if } 1.5 \times D < (2^K - 2^{-K+1}) \times N \\
K & \text{default}
\end{cases}
\]

\[
l_{\tilde{\phi}} = \max(l_{\tilde{\phi}} + 1, 2, 1)
\]

**Step 3:** Calculate the $(c, s)$ pair using the following case statement:

\[
(1, 0) \quad \text{if } N = 0 \\
(0, S_N) \quad \text{if } D = 0 \\
\left(\frac{1}{1 + t_{\tilde{\phi}}} \times (1 - t_{\tilde{\phi}}^2), 2 \times S_N \times S_D \times t_{\tilde{\phi}}\right) \quad \text{default}
\]

**Step 4:** Calculate the diagonalizing $R_{\tilde{\phi}}$ using the following case statement:

\[
R_{\tilde{\phi}} = \begin{bmatrix} c & s \\ -s & c \end{bmatrix} \quad \text{if } S_N < 0 \\
\begin{bmatrix} s & c \\ c & -s \end{bmatrix} \quad \text{else}
\]

---

Fig. 2. $\vert D \vert$ vs. $\tau$ for symmetric matrix when Algorithm 2 is applied.

Fig. 3. $\vert D \vert$ vs. $\tau_1$ and $\tau_2$ when Algorithm 2 is applied for non-symmetric matrix with ideal symmetrization.
uses (6) and (7) to calculate $\alpha$ symmetric matrices based on FHSVD algorithm. Assuming a enable us to directly calculate the fast rotations for non-

D. Direct Estimate Algorithm

One major contribution of this work is the algorithm that enable us to directly calculate the fast rotations for non-

$$l = \begin{cases} K + 1 & \text{if } 1.5 \times D > 2^{K+1} \times N \\ K - 1 & \text{if } 1.5 \times D < 2^K \times N \\ K & \text{default} \end{cases}$$

We called the relaxed version of fast rotations the expedite rotations NSVD (ERNSVD). Figure 6 compares the $RMS_{ODN}$ for NSVD, FRNSVD and ERNSVD. The $RMS_{ODN}$ are very close for both methods and with ERNSVD being less complex the new boundaries are studied after this point. Figure 5 demonstrates the $\| D \|$ vs. $\tau_1$ and $\tau_2$ for ERNSVD. The FRNSVD has lower approximation error compare to ERNSVD when $\tau_1$ or $\tau_2$ are closer to zero. This is the effect of the empirical change we applied to the boundaries in equation (18).

and we only need to calculate the value of $\alpha$ (Gotze algorithm is for symmetric matrices only).

While Gotze method is using the same flow as in the calculation of accurate rotation angles and then divides the results by two to take benefit of double rotations, we use $\tan(x) \approx x$ and the fact that this approximation is more accurate for smaller angels ($\lim_{x \to 0} \tan(x) = x$), to provide more accurate estimation of rotation angles.

Figure 7 shows the boundaries for the relaxed version with a rhombus indicator on the axis while the approximated angles are shown with circle indicators. This shows that as an example if the range of the tangent is between $(\frac{3}{8}, \frac{5}{8})$ its approximation will be $\frac{1}{4}$. The notion $B$ or $b$ are used when the original rotation angle is larger than approximations while $B$ is used for the bigger angle between $\alpha$ and $\beta$. The notion $S$ or $s$ are used when the rotation angle is smaller than its approximation while $L$ is used for the bigger angle between $\alpha$ and $\beta$. Knowing if the fast rotation angle is overestimating or underestimating the original rotation angle might requires an extra comparator (depends on the implementation) in angle calculation circuit but it could provide considerable benefit as we will demonstrate in following sections.

TABLE I gives a better understanding of how the rotation angles ($\phi$ and $\theta$) are decided only based on having an
approximation of $\alpha$ and $\beta$, $\tilde{\alpha}$ and $\tilde{\beta}$ are approximations to $\alpha$ and $\beta$ that Delsome double rotation and angle approximation are both applied (In TABLE I $\alpha$ and $\beta$ are half the rotation angles achieved from (6) and (7) to take advantage of tangent properties: $\lim_{x \to 0} \tan(x) = x$). Column $\theta$ in the table shows the possible range of $\theta$ based on the value of $\tilde{\alpha}$, $\tilde{\beta}$, and if the approximation angels are larger or smaller than the original rotation angles. $\tilde{\theta}_{\text{big}}$ is the approximation if we use the biggest possible rotation angle in the range, and $\tilde{\theta}_{\text{small}}$ is the approximation if we use the smallest possible rotation angle in the range (same notation is applied to $\tilde{\Theta}_{\text{big}}$ and $\tilde{\Theta}_{\text{small}}$).

Choosing the bigger rotation angles in general might result in increased floor level of $\text{RMS}_{\text{ODN}}$ while it results in a faster convergence rate. Columns $\tilde{\theta}$ and $\tilde{\Theta}$ in the table show the approximation we used in algorithm 3 as an example; however, this does not mean that any application of the algorithm has to use the same numbers. In fact we urge a search on the possibilities based on the application.

### E. Reducing the Direct Estimation Complexity

Algorithm 3 shows the complete flow for the calculation of $\tilde{\theta}$ and $\tilde{\Theta}$. The complexity of angle calculation is optimized for achieving reasonable hardware complexity. In Step 2 the calculation of $(l_{1\text{temp}}, B)$ or $(l_{2\text{temp}}, b)$ can be reduced to two comparison if we do not use $B$ and $b$, and it will only affect one of the fast rotation angles in the TABLE I. This case statement is represented in (18). We named this method ERFHSVD2. The $||D||$ of ERFHSVD vs. $\tau_1$ and $\tau_2$ is demonstrated in Figure 9. The comparison between the $||D||$ of ERFHSVD and ERFHSVD2 shows higher values for ERFHSVD which is expected since ERFHSVD2 is the less complex approximation. The $\text{RMS}_{\text{ODN}}$ of both methods are represented in Figure 10. The loss in convergence speed is two extra rotation at maximum performance for 32 bit representation, while it requires an extra comparator. The performance of unquantized representation of ERFHSVD2 is also demonstrated in Figure 10 to prove that the floor in the $\text{RMS}_{\text{ODN}}$ is due to the quantization and not approximations. This figure also demonstrates the difference between ERNSVD and ERFHSVD. The loss in convergence speed is four extra rotations at maximum performance for 32 bit representation, this difference is smaller when larger $\text{RMS}_{\text{ODN}}$ is acceptable. We must note that depending on the implementation, one iteration of ERFHSD might be equal to applying two iteration of ERNSVD. The ERNSVD needs to calculate and apply the symmetrizing rotation and then calculate and apply the diagonalizing rotation.

### III. Hardware Implementation

These algorithms can be implemented in different methods on the higher level. Figure 11 shows a high level systolic implementation of the decomposition algorithm for an $8 \times 8$ matrix. Figure 12 shows how the scheduling for this implementation can be organized so four independent rotations are applied in each clock cycle. Each pair shows the number of rows and columns that rotation is calculated from and applied to. While different high level designs choose different method to manage their memory unit, timing, and connections, majority of these architectures follow some common design footsteps. These architectures are constructed from two differ-
ent types of processor: diagonal and non-diagonal processors. The diagonal processor calculate, transmit and applies the horizontal and vertical rotations while the non-diagonal processor receives, and applies the rotations. Since all our contributions can be explained with more details in lower design discussions, we focus on the design of basic circuits for diagonal and non-diagonal processors (DP, and NDP). The discussed and presented are only one possible implementation. The two’s complement representation is used in this design to represent negative numbers. The fully combinational implementation of the design is discussed here.

A. Calculating the Rotations

Figure 13 demonstrates the diagram for calculating the Given’s Rotations based on the ERFHSV algorithm. This involves the first four steps of Algorithm [9]. The inputs are the elements of $2 \times 2$ matrix that is the target of decomposition. The outputs are the sign $(\text{Sign})$ and power $(l)$ in $\tan(\tilde{x}) = t = \text{Sign} \times 2^{-l}$ for both rotation angles $\tilde{\theta}$ and

| $\tilde{\alpha}$ and $\tilde{\beta}$ | $\tilde{\theta} = \alpha - \beta$ | $\tilde{\theta}_{\text{big}}$ | $\tilde{\theta}_{\text{small}}$ | $\tilde{\theta}$ | $\tilde{\theta} = \alpha + \beta$ | $\tilde{\theta}_{\text{big}}$ | $\tilde{\theta}_{\text{small}}$ | $\tilde{\theta}$ |
|---|---|---|---|---|---|---|---|---|
| $\tilde{\alpha} = \frac{1}{4}$ | Bb $(\frac{1}{4}, \frac{1}{2})$ | $\frac{1}{4}$ | $\frac{1}{2}$ | $\frac{1}{2}$ | 1 | 1 | 1 | 1 |
| $\tilde{\beta} = \frac{1}{4}$ | Bs $(0, \frac{1}{2})$ | $\frac{1}{2}$ | 0 | 0 | 1 | 1 | 1 | 1 |
| $\tilde{\alpha} = \frac{1}{4}$ | Sb $(\frac{1}{4}, 0)$ | $\frac{1}{4}$ | 0 | 0 | 1 | 1 | 1 | 1 |
| $\tilde{\beta} = \frac{1}{4}$ | Ss $(\frac{1}{4}, \frac{1}{2})$ | $\frac{1}{4}$ | $\frac{1}{2}$ | $\frac{1}{2}$ | 1 | 1 | 1 | 1 |

**TABLE I**

**DIFFERENT POSSIBILITIES OF CHOOSING THE FAST ROTATION ANGLES**

Fig. 10. Comparison of the $RMS_{\text{ODN}}$ for NSVD, ERNSVD, ERFHSDVD, Unquantized ERFHSDVD, and ERFHSDVD2

Fig. 11. Architecture of the design.

$p, q = (1, 2)(3, 4)(5, 6)(7, 8)$

$(1, 4)(2, 6)(3, 8)(5, 7)$

$(1, 6)(4, 8)(2, 7)(3, 5)$

$(1, 8)(6, 7)(4, 5)(2, 3)$

$(1, 7)(8, 5)(6, 3)(4, 2)$

$(1, 5)(7, 3)(8, 2)(6, 4)$

$(1, 3)(5, 2)(7, 4)(8, 6)$

Fig. 12. Scheduling of matrix processing order.
Algorithm 3 Algorithm to Directly Calculate the fast Rotation Angles for Non-Symmetric Matrices.

Input: A.
Output: Rotation Matrix $R_{\theta}$ and $R_{\tilde{\theta}}$.

Step 1: Calculate the initial values:

\[
\begin{align*}
S_{N1} &= \text{Sign}(c + b) \\
S_{D1} &= \text{Sign}(d - a) \\
N1 &= |c + b| \\
D1 &= 2 \times |d - a| \\
K1 &= \exp_{2}(D1) - \exp_{2}(N1) \\
S_{N2} &= \text{Sign}(c - b) \\
S_{D2} &= \text{Sign}(d + a) \\
N2 &= |c + b| \\
D2 &= 2 \times |d - a| \\
K2 &= \exp_{2}(D2) - \exp_{2}(N2)
\end{align*}
\]

Step 2: Calculate $l_\alpha$ and $l_\beta$ using following case statement:

\[
(l1_{\text{temp}}, B) =
\begin{cases}
(K1 + 1, 1) & \text{if } 1.5 \times D1 > 2^{k_{1}+1} \times N1 \\
(K1 - 1, 0) & \text{if } 1.5 \times D1 < 2^{k_{1}} \times N1 \\
(K1, 1) & \text{if } D1 < 2^{k_{1}} \times N1 \\
(K1, 0) & \text{default}
\end{cases}
\]

\[
(l2_{\text{temp}}, b) =
\begin{cases}
(K2 + 1, 1) & \text{if } 1.5 \times D2 > 2^{k_{2}+1} \times N1 \\
(K2 - 1, 0) & \text{if } 1.5 \times D2 < 2^{k_{2}} \times N1 \\
(K2, 1) & \text{if } D2 < 2^{k_{2}} \times N1 \\
(K2, 0) & \text{default}
\end{cases}
\]

\[
l_\alpha = \max(l1_{\text{temp}} + 1, 2)
\]

\[
l_\beta = \max(l2_{\text{temp}} + 1, 2)
\]

Step 3: Calculate the $l_\theta$ and $l_\tilde{\theta}$ using the following case statement:

\[
(l_\theta, l_\tilde{\theta}) =
\begin{cases}
(l_\alpha, l_\alpha) & \text{if } (N2 = 0) \\
(l_\beta, l_\beta) & \text{if } (N1 = 0) \\
(l_\beta - (B & b), l_\alpha) & \text{if } (l_\beta - l_\alpha = -1) \\
(l_\alpha - (B & b), l_\beta) & \text{if } (l_\beta - l_\alpha = 1) \\
(l_\beta - 1, 0) & \text{if } (l_\beta - l_\alpha = 0) \\
(min(l_\alpha, l_\beta), min(l_\alpha, l_\beta)) & \text{default}
\end{cases}
\]

Step 4: Calculate the $S_{\theta}$ and $S_{\tilde{\theta}}$ using the following case statement:

\[
S =
\begin{cases}
S_{D1} * S_{N1} & \text{if } (l_\beta - l_\alpha > 0 \ || \ N2 = 0) \\
S_{D2} * S_{N2} & \text{default}
\end{cases}
\]

\[
(S_{\theta}, S_{\tilde{\theta}}) =
\begin{cases}
(S, S) & \text{if } (N2 = 0) \\
(S, -S) & \text{if } (N1 = 0) \\
(S * \text{Sign}(l_\beta - l_\alpha), S) & \text{default}
\end{cases}
\]

Step 5: Calculate the $(c_{\theta}, s_{\theta})$ and $(c_{\tilde{\theta}}, s_{\tilde{\theta}})$ pairs using the following case statement:

\[
\begin{align*}
\tilde{t}_1 &= \begin{cases}
0 & \text{if } l_\theta = 0 \\
2 - l_\theta & \text{default}
\end{cases} \\
\tilde{t}_2 &= \begin{cases}
0 & \text{if } l_{\tilde{\theta}} = 0 \\
2 - l_{\tilde{\theta}} & \text{default}
\end{cases} \\
(c_{\theta}, s_{\theta}) &= \frac{1}{1 + \tilde{t}_1} \times (1 - \tilde{t}_1^2, 2 \times S_{\theta} \times \tilde{t}_1) \\
(c_{\tilde{\theta}}, s_{\tilde{\theta}}) &= \frac{1}{1 + \tilde{t}_2} \times (1 - \tilde{t}_2^2, 2 \times S_{\tilde{\theta}} \times \tilde{t}_2)
\end{align*}
\]

Step 6: Calculate the rotation matrices $R_{\theta}$ and $R_{\tilde{\theta}}$ using the following case statement:

\[
R_{\theta} =
\begin{cases}
\begin{bmatrix}
c_\theta & s_\theta \\
-s_\theta & c_\theta
\end{bmatrix} & \text{if } S_{D1} < 0 \\
\begin{bmatrix}
s_\theta & c_\theta \\
c_\theta & s_\theta
\end{bmatrix} & \text{else}
\end{cases}
\]

\[
R_{\tilde{\theta}} =
\begin{cases}
\begin{bmatrix}
c_{\tilde{\theta}} & s_{\tilde{\theta}} \\
-s_{\tilde{\theta}} & c_{\tilde{\theta}}
\end{bmatrix} & \text{if } S_{D1} < 0 \\
\begin{bmatrix}
s_{\tilde{\theta}} & c_{\tilde{\theta}} \\
c_{\tilde{\theta}} & s_{\tilde{\theta}}
\end{bmatrix} & \text{else}
\end{cases}
\]

\[\tilde{\Theta}. \text{ This circuit is only exists in diagonal processors (DPs). After calculating the value this circuit transmits the values to the circuit for applying rotations in the DP. This circuit also sends the required signals to the circuit for applying rotations in the same DP (l_\tilde{\theta}, l_\tilde{\theta}, S_\tilde{\theta}, S_\theta, S_{N1}, l_\tilde{\theta}^2 = 0, and \tilde{\theta}^2 = 0) and ND apoptosis in the same row (l_\tilde{\theta}, S_\tilde{\theta}, S_{N1}, and l_\tilde{\theta}^2 = 0), and column (l_\tilde{\theta}, S_\tilde{\theta}, S_{N1}, and l_\tilde{\theta}^2 = 0). The circuit for each of the steps is discussed hereafter.}

1) ERFHSV Step 1: Figure 14 demonstrates the diagram of the proposed design for the first step of ERFHSV algorithm. This circuit generates the initial values for being used at the next steps in ERFHSV algorithm. The inputs are the elements of $2 \times 2$ matrix that is the target of decomposition. $1^t_{t_{\tilde{\theta}}} = 0$ is the signal name and will be one if $l_{\tilde{\theta}}$ is equal to zero (this signal is used to make decision on cases in Step 2 of the Algorithm ??), and $S_{N1}$ is the sign of the numerator in equation ??.

Fig. 13. Diagram for calculating the Given’s Rotations based on the ERFHSV algorithm.
The MSB block does not have any cost in VLSI implementation and it is demonstrating that the most significant bit of the value is used to determine the sign (The implementation is two’s complement). The blocks with \(|\phi|\) on them are the circuits to calculate the absolute value of the input value. We assume this will cost an XOR complementing circuit and an adder to calculate the two’s complement of negative numbers. To avoid overflow or the need to use saturation, the adder size of the \(|\phi|\) circuits should be at least of the same size as the matrix input argument. The P-Enc blocks are priority encoders as explained in (12), where \(v\) is the valid signal and is zero when the input signal is equal to zero, and it is one for rest of the cases. The blocks with \(<< 1\) are indicating shifts to the left (or multiplying by two) and their VLSI implementation does not have any cost. The last two subtractors in this diagram have the size of \(ceil(log_2(bit))\) where \(bit\) is the number of bits each element of input matrix is represented with. One of the conditions of the second step is to limit the value of \(K1\) and \(K2\) to the minimum of two. The over flow outputs of the last two subtractors are indicating a negative result since both inputs are positives.

2) ERFHSVD Step 2: Figure 14 demonstrates the diagram of the proposed design for the second step of ERFHSVD algorithm. This block shows how \(l_{\theta}\) is calculated. A similar block can be used to generate \(l_{\beta}\). This circuit uses an adder and a B-Shifter to generate the signals required for the case statement in Step 2. The blocks with \(<< 1\) are indicating shifts to the left (or multiplying by two) and their VLSI implementation does not have any cost. The adder, B-Shifter, and comparators are of the size \(bit\). The last adder and mux in the block diagram are of the size \(ceil(log_2(bit))\). The L-Ckt is indicating a logical circuit that can be implemented with a and, or, and inverter representation or any other means necessarily. We have merged the case statements of Step 2 with the mathematic phrase coming right after them and represented them both in one circuit. In fact the last multiplexer in the diagram is saturating the results to the minimum of two; while the “L-Ckt 2” is generating its select signal inputs. The “L-Ckt 1” outputs, zero, one or two to be added in the final adder based on the case condition; while also generating the “B” signal. For "L-Ckt 1", \(B = I_0 I_1 + I_2, O_0 = I_1 I_2,\) and \(O_1 = I_2.\) For "L-Ckt 2", \(O_0 = I_5 + I_2 + I_1 I_6.\) The signal \(K1 = 0\) is generated with an eight-input NOR gate while the signal \(K = 1\) is generated with a NOR gate and an inverter. We did not show these gates in the figure in favor of keeping the diagrams straightforward.

3) ERFHSVD Step 3: Figure 15 demonstrates the diagram of the proposed design for the third step of ERFHSVD algorithm. This circuit takes the \(l_{\alpha}, l_{\beta}. N2^2 = 0, Bb, (S_{N2} + SD2) + (S_{N1} + S_{D1}), N1^2 = 1\) signals as inputs and outputs the values of \(l_{\delta}\) and \(l_{\delta}\) to the circuit for applying rotations and the sign bit of \(l_{\beta} - l_{\alpha}\) to Step 4. This design merges the case statement in Step 3 and the mathematical phrase after it, and implements both together. Shift left logical (SLL blocks marked with \(<<\)), adder, subtractor, and multiplexers blocks are of the size \(ceil(log_2(bit))\). The block that is supposed to determine if the result of the subtract is zero (this block is marked with \(\tilde{\theta} = 0\)) requires a NOR gate of size \(ceil(log_2(bit)) + 1\) assuming that overflow (Ov) can happen and for detecting “one” an inverter and a NOR gate is required, since both \(l_{\alpha}\) and \(l_{\beta}\) are positive an AND gate of size \(ceil(log_2(bit))\) with an inverter can be used to synthesize the block marked with \(\tilde{\theta} = -1\). This provision is taken to prevent the usage of comparators. The L-Ckt 1 applies any change necessary on the value of \(l_{\beta}\) by adding zero, minus one, or minus two to it. The L-Ckt 2 generates the input signals to the mux based on the inputs to assure that correct values are assigned to \(l_{\delta}\) and \(l_{\delta}\). Since \(l_{\beta} \geq 2\), the result of the additions can be negative, the Ov outputs of the adders can be ignored. The final multiplexer of the circuit is needed to guarantee that diagonalized output matrix is normalized. In L-Ckt 1, \(O_0 = T_0 T_2 T_3 T_5 + T_0 T_2 T_4 T_6 + T_0 I_4 T_5, O_1 = T_1 I_4 T_5 + T_0 T_1 T_5, O_2 = T_0 T_1 T_2 I_5 + T_0 I_2 T_4 I_5 + 0\).

\({\text{N1}}^2 = 0\) will be one if \(N1 = 0\) (which \(N1\) is the numerator in equation 6).
$T_0 I_1 I_4 I_5$, and $O_2 = T_1 I_4 I_5 + T_0 T_1 I_5$. In L-Ckt 2, the signals are defined as follows: $O_0 = I_5 I_6 + I_5 I_6 I_1 + I_6$, $O_1 = I_0 + I_1 + I_2 + I_3 I_5 + I_6$, $O_2 = I_5 I_5 + I_0 I_1 I_5 + I_6$, and $O_3 = I_0 + I_1 + I_2 + I_3 I_1 I_6$.

Using the circuit presented in Figure 16 with minor changes in L-Ckt 1 and L-Ckt 2 implementation, every different value in the first three rows of TABLE I can be assigned as the rotation angle. If implementation of more rows from the table is required, the circuit to detect plus and minus two also should be added and feed to the logical circuits. The simple design presented for this step of the algorithm would assist the designers to change table values based on their application need. For more complex design, in case the number of inputs to the logical circuits is high, an alternative design can be explored that two-input multiplexers (two AND gates of size $\text{ceil}(\log_2(\text{bit}))$) are used to impedance the second case statement in Step 3. The multiplexer swaps the value of $l_\theta$, and $l_\theta$ if $(S_{D1} \oplus S_{N1}) \oplus (S_{D2} \oplus S_{N2}) = 1$. This will reduce the complexity of L-Ckt 1 and might eliminate the need for one of the adders.

4) ERFHSD Step 4: Figure 17 demonstrates the diagram of the proposed design for the fourth step of ERFHSD algorithm. This circuit takes the sign bit of $l_\beta - l_\alpha$ ($\text{Sign}(l_\beta - l_\alpha)$), $N2^2 = 0$, $N1^2 = 0$, $S_{N1}$, $S_{D1}$, $S_{N2}$, and $S_{D2}$ as input and generates the sign of the rotations ($S_{\text{tilde} \theta}$ and $S_{\text{tilde} \bar{\theta}}$). Correct implementation of this step is vital for convergence of the iterations as well as achieving the normalized diagonal elements. For "L-Ckt 1", $O_0 = T_0 T_3 I_4 + I_0 I_2 I_3 + I_0 I_2$, and $O_1 = T_0 I_1 I_2 T_3 + I_0 I_3 + I_0 I_2 + I_0 I_1$.

B. Applying the Rotations

Figure 18 demonstrates the diagram of the proposed design for applying rotations. This circuit includes the major part of the NDP (except memory units and the mechanism to receive the input arguments and transfer the results). Assuming a $2 \times 2$ matrix decomposition is presented in (19). For an iterative algorithm this unit should be able to apply both rotation matrices on the old value of $U (\Sigma_{\text{Old}})$ based on the values of $l_\theta$ and $l_\bar{\theta}$, it also should apply one rotation matrix on the old value of $V (\Sigma_{\text{Old}})$ based on the values of $l_\bar{\theta}$ to generate the new values. The $\text{Sign}$ signal is in fact one if $S_N \geq 0$ as we will explain in the next sub section. The initial value of $\Sigma$ is $A$ and the initial value of $U$ and $V$ is identity matrix.

\[ A = U \times \Sigma \times V^T \quad (19) \]

1) Applying Double and Single Given’s Matrix Rotations: Figure 19 demonstrates the diagram of the proposed design for calculating the single Given’s Rotation. It is important to note that applying a Given’s rotation is in fact a multiplication of two $2 \times 2$ matrices. This is equal to eight multiplication and four addition if no other consideration is made about the implementation of the system. We can use this circuit to calculate the value of $V$ and $U$. The scale circuit is demonstrated with doted outline to remind readers that its presence or implementation complexity (and accuracy as the result) can be adapted based on the application need. The $\text{Sin}$ signal that is an input to each Multiply block shows if that block has to multiply the input argument with $\text{Sin}(\bar{\theta})$ or $\text{Cos}(\bar{\theta})$. A control unit can separately assign different values to each Multiply block, or it can choose to multiply the input value with $\text{Sin}(\bar{\theta})$ or $\text{Cos}(\bar{\theta})$. In the design the blocks are with a different color to make sure they multiply the input argument with $\text{Cos}(\bar{\theta})$ while the normal blocks are multiplying the input arguments with $\text{Sin}(\bar{\theta})$.

$^3\text{Sin}$ is one when a block going to apply sine rotation and cosine rotation otherwise.
Figure 20 demonstrates the diagram of the proposed design for calculating the single Given’s Rotations. The same notation as in Fig 19 is used in this diagram. The circuit in this diagram has double complexity compared to the design of Figure 19.

This is expected since this circuit has to multiply the input $2 \times 2$ matrix with two rotation matrices of $R_\theta$ and $R_\phi$.

2) Multiplying and Scaling: The rotation angles are the approximations to $t = |\tan(x)|$ with $\tilde{t} = |\tan(\tilde{x})| = 2^{-l}$ and as the result of applying double rotations the elements of any rotation matrix should be zero, one, or the values derived from equation (20) or equation (21). The $\text{Sign}$ in (21) will be determined in Step 4 ($S_{\phi}$ or $S_{\theta}$). The part $\frac{1}{1+t^2}$ is common between all the coefficients and we will discuss it in detail after presenting the circuit which applies the uncommon part of the multiplications (this is referred to as scaling) if the proposed circuit is able to apply any of these coefficients using only control signals then we can merge Step 5 and Step 6 in algorithm 3 (this is referred to as multiplying).

$$\frac{1}{1+t^2} \times 1 - \tilde{t}^2$$ \hspace{1cm} (20)

$$\frac{1}{1+t^2} \times 2 \times \text{Sign} \times \tilde{t}$$ \hspace{1cm} (21)

Figure 21 demonstrates the diagram of the proposed design for multiplications. This is a fully combinational circuit and a possible design. The input $A$ is any of the elements of the matrix in $\tilde{A}$. If $\xi$ is zero ($l = 0$, $\text{Sin}^\ast = 1$, $\text{Comp}^\ast = 1$), then the adder in the figure is adding $A$ with $-A$. If $\xi$ is one ($l = 0$, $\text{Sin}^\ast = 0$, $\text{Comp}^\ast = 0$), then the adder is adding $A$ with zero. To apply equation (20), the input value has to be shifted to the right twice the value of $l$ and then subtracted from the original value ($l \neq 0$, $\text{Sin}^\ast = 0$, $\text{Comp}^\ast = 1$). The circuit should be able to apply equation (21) assuming sign can be negative or positive. For this equation the adder only adds one to the input value to convert one’s compliment values to two’s compliment values ($l \neq 0$, $\text{Sin}^\ast = 1$, $\text{Comp}^\ast = 1$). For this circuit a control unit can define the values for selecting input of multiplexers or the value of $\text{Comp}^\ast$ however if we use the signals as defined in Figure 21 we can assign $\text{Sin}^\ast = S_{N1}$ and just swap the input index for multiplexers if a unit needs to apply $\text{Cos}(\tilde{x})$ when $S_{N1} < 0$. If the multiplication circuit belongs to a DP then the $S_{N1}$ signal of the same processor is used to determine the $\text{Sin}^\ast$ signals, while if the circuit belongs to an NDP then $S_{N1}$ that is transmitted from the DP in the same row is used for determining the $\text{Sin}^\ast$ signals in the first row of the double Given’s rotations circuit and updating the values of $U$. The $S_{N1}$ that is transmitted from the DP in the same column is used for determining the $\text{Sin}^\ast$ signals in the second row of the double Given’s rotations circuit and updating the values of $V$.

Applying scaling is one of the more resource demanding parts in this design while it might not be necessary for every application to apply scaling coefficients when decomposing a matrix. This generally results in applying orthogonal rotation angles and an increase in the value of diagonal elements of decomposition which might be acceptable for some applications. Comparing the fast rotations method with CORDIC method the complexity of the scaling circuit is increased when applying fast rotations. The fact that CORDIC method applies all the rotation angles and only the sign of the rotations are different results in a constant scaling value; while, the fast rotations can be different any time, this results in different scaling for different rotation angels. (23) and (22) suggest using the Tailor series representation of $\frac{1}{1+t^2}$ as in (22). The estimation of complexity depends on the implementation, but a simplified look at the problem is presented in (23) and (22). The complexity of other CORDIC based implementations is also presented there. The implementation of the scaling factor for 32 bits implementation requires four Shifts and four additions. A closer look at the scaling coefficient would help reducing the complexity of scaling circuit to four addition, and one shift. Table 11 shows the scaling coefficient that needs to be applied for each rotation angle of $\tan(\tilde{x}) = 2^{-l}$. Increase in the value of $l$ causes the scaling coefficient to merge to one; as the result, for $l \geq 16$ the 32 bit representation of the coefficient is rounded to one. The notation $Z = \text{Acc.}\{\Delta\} \gg \delta$ is equal to $Z = \Delta + \Delta \gg \delta$ which $\Delta \gg \delta$ means arithmetic shift of the $\Delta$ to right $\delta$ times. Figure 22 demonstrates the diagram of the proposed design for scaling in ERFHSVD algorithm.

$$\left(1 + 2^{-2l}\right) \left(1 + 2^{-4l}\right) \left(1 + 2^{-8l}\right) \left(1 + 2^{-16l}\right) \ldots$$ \hspace{1cm} (22)

In Figure 22 a 32 bit value is multiplied by scale factor $\lambda$ based on the representation in the last column of table 11. This circuit tries to gain the benefit from repetitive nature of coefficient $\lambda$. If $l \geq 16$ then the scaling factor would simply be one. The circuit presented in this figure is not extendable directly for higher number of bits accuracy and it would be a simpler circuit for lower number of bits. The select signals for the multiplexers has to be assigned based on the value of $l$. For the multiplexer we assumed that the three and four-input multiplexers are made of two-input multiplexers and rearrange them in a way that minimum number of two-input multiplexers are required. In addition, we assume that the Barrel shifters are made out of two-input multiplexers to be able to compare the complexity of the new implementation with the implementation that requires four shifts and four adds. Following the assumptions made, the shifts are requiring the use of B-Shifter since the value of $l$ is different each time. Each B-Shifter will require 160 two-input multiplexers, and our design will require 224 two-input multiplexers for the multiplexers represented in the circuit.

$^4\text{Comp}$ is one if the multiplicand is negative.
Fig. 20. Diagram for applying double Given’s rotations

TABLE II

| Scale (A) | Fraction | Decimal | Binary (32 bit) | Circuit representation of \(\Lambda G\) (any 32 bit input) |
|-----------|----------|---------|-----------------|--------------------------------------------------|
| 1         | 2        | 0.111001100110011001100110011001 | \(\text{Acc.} \{\text{Acc.} \{G - 2^{-16}G\} >> 4\} >> 8\} >> 16\) |
| 2         | 4        | 0.111100001111000011110000110000 | \(\text{Acc.} \{G - 2^{-16}G\} >> 12 + (G - 2^{-16}G) >> 24\) |
| 3         | 6        | 0.1111110000001111110000111111 | \(\text{Acc.} \{G - 2^{-8}G\} >> 16\) |
| 4         | 8        | 0.1111111100000011111110000000 | \(\text{Acc.} \{G - 2^{-12}G\} >> 20\) |
| 5         | 10       | 0.1111111111000000000000000000 | \(\text{Acc.} \{G - 2^{-12}G\} >> 24\) |
| 6         | 12       | 0.1111111111110000000000000000 | \(\text{Acc.} \{G - 2^{-12}G\} >> 28\) |
| 7         | 14       | 0.1111111111111100000000000000 | \(G - 2^{-18}G\) |
| 8         | 16       | 0.1111111111111110000000000000 | \(G - 2^{-20}G\) |
| 9         | 18       | 0.1111111111111111000000000000 | \(G - 2^{-20}G\) |
| 10        | 20       | 0.1111111111111111000000000000 | \(G - 2^{-22}G\) |
| 11        | 22       | 0.1111111111111111110000000000 | \(G - 2^{-24}G\) |
| 12        | 24       | 0.1111111111111111111100000000 | \(G - 2^{-26}G\) |
| 13        | 26       | 0.1111111111111111111110000000 | \(G - 2^{-28}G\) |
| 14        | 28       | 0.1111111111111111111111000000 | \(G - 2^{-30}G\) |
| 15        | 30       | 0.1111111111111111111111110000 | \(G - 2^{-32}G \approx G\) |
| 16        | 32       | 0.1111111111111111111111111100 | \(G - 2^{-32}G \approx G\) |
This will result in saving 156 two-input multiplexers. This results is approximately saving the cost of one B-Shifter. This circuit also has effects on critical path delay. While a B-Shifter that uses 160 two-input multiplexer has five level of two-input multiplexers the multiplexers in our design at most have two levels. The major benefit of the circuit presented in Figure 22 is when some error occurs in applying the scaling factor is acceptable. If we implement the circuit only with the first subtraction, the maximum error in applying the scale coefficient will be 6.25%. If we represent the circuit with the second adder the maximum error in scaling coefficient will be 0.39% (it multiplies the input value with 0.797 instead of 0.8). The circuit with three adders would have maximum of 0.024% error in applying the coefficients (it multiplies the input value with 0.7998 instead of 0.8). Due to the complexity of scaling circuit in comparison with the rest of the architecture and its variable importance due to the application, we recommend a detailed study for each application. Based on the required accuracy of the result the scaling circuit may be completely ignored or represented with less complex and less accurate circuit. For example the two shifts that are represented in different color (and dotted exterior line), their associated paths, and the last level of adder/multiplexer are only need to be implemented if 32 bit accuracy for the scaling coefficient is needed.

IV. COMPLEXITY

The calculation of computational complexity (delay, and resource requirement) depends on the multiple factors other than only the block diagram of the subsystem; however we will try to provide an approximation using some basic assumption to provide a better understanding of this work achievements. We divide the discussions to two sub sections of calculating and applying the rotations. We assume the critical path of any of the blocks in the block diagram representation of any circuit is known as it is represented with symbol $\Delta$. We assume that every subtractor (Sub) is an adder with carry-in equal to one and an array of inverters; as the result, its delay is higher than an adder of same number of bits. We assume that the size of the inputs are $\Lambda$ bits with $\lambda = ceil(log_2\Lambda)$.

For resource estimation, we use $A$ as area or resources required for implementing of a particular circuit. The $A_{Add}$ is representing the area or resources required to implement an adder of size $\Lambda$ bits.

A. Calculating the rotations

In order to be able to evaluate the delay of the system we assume that an adder of size $\Lambda$ bits has higher delay than a B-Shifter of the same size.

1) Step 1: The critical path starts from the subtractor that generates the absolute value of $D_1$ or $D_2$ in the first step and the adder that generates $1.5 \times D_1$ in the second stage, instead of the adder that generates the $N_1$ or $N_2$ in the first Stage and the B-Shifter in the second stage. In (23) the critical path delay for the first step of ERFHSVD algorithm is presented.

$$
\Delta_{Step \ 1} = \Delta_{AddSub} + \Delta_{Add|\Phi|} + \Delta_{AddP-Enc} + \Delta_{AddSub}
$$  

The phrase $\Delta_{AddSub}$ means that the critical path of a $\Lambda$ bit subtractor; similar notations are used for other elements. The $|\Phi|$ is the circuit calculating the absolute values, and $\Delta_{AddP-Enc}$ refers to the critical path of a $\Lambda$ bit P-Enc. As explained in the beginning of this section the delay path of the subtractor and $|\Phi|$ can be translated to the delay of adders.

In (24) we tried to apply this.
\[ \Delta_{\text{Step 1}} = \Delta_{\text{bitAdd}} + \Delta_{\text{Neg}} + \Delta_{\text{bitAdd}} + \Delta_{\text{Complement}} + \Delta_{\text{bitP-Enc}} + \Delta_{\text{bitAdd}} + \Delta_{\text{Neg}} \]
\[ = 2 \times \Delta_{\text{bitAdd}} + 2 \times \Delta_{\text{Inv}} + \Delta_{\text{2InpXOR}} + \Delta_{\text{bitP-Enc}} + \Delta_{\text{bitAdd}} \]  
(24)

We assume that \( \Delta_{\text{Neg}} \) refers to the delay of an inverter and \( \Delta_{\text{Complement}} \) refers to the delay of a two-input XOR gate. We replaced the \( \Delta_{\text{Neg}} \) with \( \Delta_{\text{Inv}} \) (inverter) and \( \Delta_{\text{Complement}} \) with \( \Delta_{\text{2InpXOR}} \) (two-input XOR) and we will keep that notation hereafter. The Area required to implement this circuit is represented in \( (25) \).

\[ A_{\text{Step 1}} = 8 \times A_{\text{bitAdd}} + 2 \times (\Lambda + \lambda) \times A_{\text{Inv}} \]
\[ + 4 \times \Lambda \times A_{\text{2InpXOR}} + 4 \times \Delta_{\text{bitP-Enc}} \]
\[ + 2 \times A_{\lambda \text{bitAdd}} \]  
(25)

2) Step 2: In \( (26) \) the Critical path delay for the first step of ERFHSVD algorithm is presented. In this equation \( \Delta_{\text{2InpMux}} \) is the critical path delay of a two-input multiplexer.

\[ \Delta_{\text{Step 2}} = \Delta_{\text{bitAdd}} + \Delta_{\text{Complement}} + \Delta_{\text{L-\text{Ckt 1}}} + \Delta_{\text{bitAdd}} + \Delta_{\text{2InpMux}} \]
\[ = \Delta_{\text{bitAdd}} + \Delta_{\text{2InpXOR}} + \Delta_{\text{L-\text{Ckt 1}}} + \Delta_{\text{bitAdd}} + \Delta_{\text{2InpMux}} \]  
(26)

Where,

\[ \Delta_{\text{L-\text{Ckt 1}}} = \Delta_{\text{Inv}} + \Delta_{\text{2InpAnd}} + \Delta_{\text{2InpOr}} \]  
(27)

The Area required to implement this circuit is represented in \( (28) \).

\[ A_{\text{Step 2}} = 2 \times (A_{\text{bitAdd}} + 2 \times (A_{\text{bitShifter}} + \Delta_{\text{bitAdd}} + \Delta_{\text{bitComparator}} + \Delta_{\text{L-\text{Ckt 2}}}) + A_{\lambda \text{bitAdd}} + \lambda \times A_{\text{2InpMux}}) \]  
(28)

Where,

\[ A_{\text{L-\text{Ckt 2}}} = 3 \times (A_{\text{Inv}} + A_{\text{2InpOr}} + 2 \times A_{\text{2InpAnd}}) \]  
(29)

and

\[ A_{\text{L-\text{Ckt 1}}} = 6 \times A_{\text{Inv}} + 2 \times A_{\text{3InpOr}} + 2 \times A_{\text{2InpOr}} \]
\[ + 4 \times A_{\text{3InpAnd}} + 6 \times A_{\text{4InpAnd}} \]  
(30)

3) Step 3: In \( (31) \) the Critical path delay for the first step of ERFHSVD algorithm is presented. In this equation \( \Delta_{\text{2InpMux}} \) is the critical path delay of a two-input multiplexer.

\[ \Delta_{\text{Step 3}} = \Delta_{\text{bitSub}} + \Delta_{\text{L+1InpNor}} + \Delta_{\text{L-\text{Ckt 1}}} + \Delta_{\text{bitAdd}} + \Delta_{\text{4InpMux}} \]
\[ = 2 \times \Delta_{\text{bitAdd}} + \Delta_{\text{L+1InpNor}} + \Delta_{\text{L-\text{Ckt 1}}} + \Delta_{\text{bitAdd}} + \Delta_{\text{4InpMux}} \]  
(31)

If we assume the four-input multiplexer is made of two levels of two-input multiplexers, we can further simplify the equation.

\[ \Delta_{\text{Step 3}} = 2 \times \Delta_{\text{bitAdd}} + \Delta_{\lambda+1\text{InpNor}} + \Delta_{\text{L-\text{Ckt 1}}} + \Delta_{\text{Inv}} + 2 \times \Delta_{\text{2InpMux}} \]  
(32)

where,

\[ \Delta_{\text{Ckt 1}} = \Delta_{\text{Inv}} + \Delta_{3\text{InpOr}} + \Delta_{4\text{InpAnd}} \]  
(33)

The Area required to implement this circuit is represented in \( (34) \). We assume that nine-input NOR and AND gates do require the same area.

\[ A_{\text{Step 3}} = 3 \times A_{\text{bitAdd}} + 3 \times \Delta_{\text{L+1InpNor}} \]
\[ + \Delta_{\text{L-\text{Ckt 1}}} + \Delta_{\text{L-\text{Ckt 2}}} + 10 \times A_{\text{Inv}} + \lambda \times A_{\text{2InpMux}} \]  
(34)

If we assume that a four-input multiplexer, is made of three, two-input multiplexers the area requirement is presented in \( (35) \).

\[ A_{\text{Step 3}} = 3 \times A_{\text{bitAdd}} + 3 \times \Delta_{\text{L+1InpNor}} \]
\[ + \Delta_{\text{L-\text{Ckt 1}}} + \Delta_{\text{L-\text{Ckt 2}}} + 10 \times A_{\text{Inv}} + \lambda \times A_{\text{2InpMux}} \]  
(35)

Where,

\[ A_{\text{Ckt 1}} = 6 \times A_{\text{Inv}} + 2 \times A_{3\text{InpOr}} + 2 \times A_{2\text{InpOr}} \]
\[ + 4 \times A_{3\text{InpAnd}} + 6 \times A_{4\text{InpAnd}} \]  
(36)

and,

\[ A_{\text{Ckt 2}} = 2 \times A_{\text{Inv}} + 2 \times A_{3\text{InpOr}} + 2 \times A_{5\text{InpOr}} \]
\[ + 3 \times A_{2\text{InpAnd}} + 2 \times A_{3\text{InpAnd}} \]  
(37)

4) Step 4: In \( (38) \) the area requirement of the proposed circuit for the fourth step of ERFHSVD is estimated. The Critical path delay of this circuit is not presented since the delay of that circuit does not have any affect on the total delay of the design. In fact the delay of this step is less than the delay of the third step of the algorithm which runs in parts parallel to this step of the ERFHSVD algorithm.

\[ A_{\text{Step 4}} = A_{\text{2InpMux}} + A_{\text{L-\text{Ckt 1}}} + A_{\text{2InpXOR}} \]  
(38)

where,

\[ A_{\text{Ckt 1}} = \Delta_{\text{L-\text{Ckt 1}}} + \Delta_{\text{L-\text{Ckt 2}}} \times A_{\text{4InpNor}} + \times A_{3\text{InpNor}} \]
\[ + 3 \times A_{3\text{InpAnd}} + 4 \times A_{2\text{InpAnd}} \]  
(39)

B. Applying the rotations

The circuit of applying the rotations has expanding symmetry and is self-similar. This simplifies its implementation and complexity estimation. This also makes it a good candidate for pipelining. A high level look at the design of this circuit shows that it is made of 4 similar blocks each capable of applying single Given’s Rotation. The critical path is determined by the circuit that applies double Given’s rotations.
\[ \Delta_{\text{ApplyingRotations}} = 2 \times \Delta_{\text{OneGiven\'sRotation}} \]
\[ = 2 \times (\Delta_{\text{AddMultiply}} + \Delta_{\text{AddAdd}} + \Delta_{\text{AddScale}}) \] (40)

\[ A_{\text{ApplyingRotations}} = 4 \times A_{\text{OneGiven\'sRotation}} \]
\[ = 4 \times (\lambda \times A_{\text{AddMultiply}} + 4 \times A_{\text{AddAdd}} + 4 \times A_{\text{AddScale}}) \] (41)

Assuming that the circuit of multiply as it represented in Figure 21 the followings equation will calculate the area and latency of the Multiply circuit.

\[ \Delta_{\text{Multiply}} = \Delta_{\text{AddAdd}} + \Delta_{\text{AddB-Shifter}} + \Delta_{\text{2InpXOR}} + \Delta_{\text{AddAdd}} \] (42)

\[ A_{\text{Multiply}} = A_{\text{AddAdd}} + A_{\text{AddAdd}} + \lambda \times A_{\text{2InpXOR}} + A_{\text{AddB-Shifter}} + (\lambda + \lambda) \times A_{\text{2InpMax}} \] (43)

Considering the circuit represented in Figure 21 for Scaling, we calculate the delay and area requirement of this circuit for a 32 bit representation.

\[ \Delta_{\text{Scale}} = \Delta_{\text{32bitBShifter}} + \Delta_{\text{32bitSub}} + \Delta_{\text{2InpMax}} + \Delta_{\text{32bitAdd}} + \Delta_{\text{2InpMax}} + \Delta_{\text{32bitAdd}} + \Delta_{\text{2InpMax}} \]
\[ = \Delta_{\text{32bitB-Shifter}} + 4 \times \Delta_{\text{32bitAdd}} + \Delta_{\text{Inv}} + \Delta_{\text{2InpMax}} + 2 \Delta_{\text{InpMax}} \]
\[ = \Delta_{\text{32bitB-Shifter}} + 4 \times \Delta_{\text{32bitAdd}} + \Delta_{\text{Inv}} + 5 \times \Delta_{\text{2InpMax}} \] (44)

\[ A_{\text{Scale}} = A_{\text{32bitBShifter}} + A_{\text{32bitSub}} + 32 \times A_{\text{2InpMax}} + 32 \times A_{\text{32bitAdd}} + 32 \times A_{\text{4InpMax}} + 32 \times A_{\text{32bitAdd}} + 32 \times A_{\text{4InpMax}} + 32 \times A_{\text{32bitAdd}} + 32 \times A_{\text{4InpMax}} + 64 \times A_{\text{4InpMax}} \]
\[ = A_{\text{32bitB-Shifter}} + 4 \times A_{\text{32bitAdd}} + 32 \times A_{\text{Inv}} + 32 \times A_{\text{2InpMax}} + 64 \times A_{\text{4InpMax}} + 64 \times A_{\text{4InpMax}} \]
\[ = A_{\text{32bitB-Shifter}} + 4 \times A_{\text{32bitAdd}} + 32 \times A_{\text{Inv}} + 224 \times A_{\text{2InpMax}} \] (45)

V. Results

We implemented the architecture presented in this work. Our implementation uses a 16 bit fixed point representation at the input (this number changes in the internal levels). We did not consider use of pipelining technique since pipelining and its achievable gain is orthogonal to the main idea of this paper. The use of the pipelining and parallel hardware can be employed without any complications since the matrices are independent of each other. The use of parallel hardware can increase the throughput while it dose not effectively benefit the hardware efficiency and our design hardware efficiency will be poorer than some of the previous designs; on the other hand using pipelining will increase the throughput as well as hardware efficiency.

The comparison of the presented method in this with some of the state of the art works is presented in inverse chronological order in Table III. This results show considerable improvement in energy per matrix target function over other designs. The state of the art designs apply their algorithm on complex matrices, while our approach is employed to take advantage of reduced complexity achievable. This approach is valid since the recent publications are using SVD on the complex valued channel matrix of telecommunication systems; however for an application that requires the decomposition of a real valued matrix it is not that efficient. Any complex valued channel matrix can be converted to real valued channel matrices with four times the number of elements. To keep comparability we presented our synthesis results in a comparable form. A 2 × 2 matrix size in Table III is a 2 × 2 complex valued matrix and equivalent to a 4 × 4 real valued matrix.

For comparison we considered the most resent designs that are able to calculate the SVD of nonsymmetric matrices and decompose a matrix to three matrices of U, Σ, and V. Our goal is to show how our proposed design is able to provide energy efficient design with minimal hardware complexity. Due to the lack of pipelining and parallelism our proposed hardware does not achieve high hardware efficiency but the achievable gain from those methods is orthogonal to the benefit of this work original idea. In Table III the results for various target functions are presented. In the telecommunication era power consumed to accomplish a task (as an indicator to show how fast the portable devices will drain their power using that particular device), and the throughput of a system are of the most importance. The value of the target function energy per matrix holds the effect of both important parameters. This parameter does not include the effect of hardware complexity. Energy per matrix is the target function that can be used for comparison in this case. This function is able to project the effect of power consumption and throughput at the same time and ignores the effect of orthogonal techniques used for reducing the power, however, this function is still not able to eliminate the effect of hardware reuse in pipelining.

Beside the works compared in the Table III authors in 24 use a method called supper linear SVD (SL-SVD) and are able to decompose a matrix sizes of 1 × 1 ∼ 4 × 4 very efficiently. The only downside to this algorithm is that it relies on the matrix quality and the channel characteristic. This matrix characteristic is harder to achieve with bigger size matrices. The convergence of this algorithm relies on all the singular values being different and in the case of two or more singular values being equal this algorithm never converges.

In comparison with 26 our design achieves a lower throughput in smaller matrix sizes while our design without using any pipelining is able to achieve 23% higher throughput for an 8 channel matrix. Authors in 26 use different bit sizes (12 ∼ 16) for different matrix size (2 × 2 ∼ 8 × 8) and uses different number of sweeps (3 ∼ 15) for various matrix sizes. This method is also only designed to calculate the SVD of square matrices with even number of rows with complex
elements. Our design on the other hand keeps the 16 bit input accuracy for all the matrix sizes, and maps the number of sweeps used in [26] to the equivalent number for fast rotations method based on the values demonstrated in Figure 10. The proposed design is also able to decompose any square matrix of size $1 \times 1 \sim 8 \times 8$ (complex valued elements) and is able to as effectively decompose matrices with real valued element. In term of energy efficiency or our target function of energy per matrix our design provides $2.83 \sim 5.32$ (2.83 achieves from comparison of $8 \times 8$ matrices and 5.32 from comparison of $2 \times 2$ matrices) times better efficiency.

The authors of [27] and [28] do not provide the power consumption of their design. The hardware complexity of the design represented in these works is considerably lower specially for lower sized matrices, however the throughput and normalized throughput of those designs is also lower. This in other word means that the hardware efficiency of these designs is lower and they are not good candidates for high throughput applications.

The authors in [29] use a Givens Rotation based design with a bipartite decomposition algorithm. First they convert a general matrix to a bidiagonalized matrix. The next step is to nullify the off diagonal elements. This design is capable of calculating both SVD and QRD (QR Decomposition). The proposed architecture in [29] is only capable of decomposing $4 \times 4$ matrices. Various techniques including pipelining, hardware sharing, and early termination are utilized to increase the hardware efficiency and throughput of the design. In the Table 11 the power consumption of the design is mentioned with and without utilization of early termination process. This is to provide a fair comparison number since the gain achieved from early termination is application specific and also other designs could employ it. This design adopts a 12 bit implementation in contrast with our 16 bit implementation. The energy per matrix function of this design is $15.4\%$ better than our proposed design and its hardware complexity is $0.72\%$ higher.

In comparison with [30] the energy per matrix of our proposed design is $649 \sim 36.131$ times for matrix sizes of $2 \times 2 \sim 8 \times 8$ respectively. This benefit is achieved as the result of lower power usage of our work which is due to the simplicity of the hardware and eliminating the need for multiple pipeline registers. The achievable throughput and normalized achievable throughput are also higher in our proposed design.

In conclusion in term of Throughput as the target function, this design shows a superior performance compared to the works presented in [27], [30], and [28]. The work in [26] is 4.51 times better than our design for matrix size of $2 \times 2$; while this gap in the throughput result is reduced with the increase in the matrix size, and our design provides $1.24$ times better throughput for $8 \times 8$ matrices. This achievement is considerable since our design does not use any parallelism or pipelining. In term of hardware efficiency or Normalized Throughput function the design presented in this work provides better results than the work presented in [27], [30], and [28]. While the normalized throughput of this work is $1.47 \sim 3.931$ times for matrix sizes of $2 \times 2 \sim 8 \times 8$ respectively compared to the work presented in [26], this is not far from expected since we expected the hardware efficiency of our design to be poorer.

VI. Conclusion

In this work, for the first time we presented an algorithm that directly estimates the fast rotations for singular value decomposition of a non symmetric matrix. This method, unlike the previous efforts to implement an eigenvalue decomposition, is able to provide the “Normalized” results. An implementation is presented for $2 \times 2$ matrix as the basic block cell of any matrix of higher size. Unlike the previous efforts the proposed hardware does not require any floating point representation or hardware. The analysis of implementation requirement and complexity is also presented. The hardware complexity of the $2 \times 2$ matrix decomposer is much lower than the previous floating-point implementations. This design provides $2.83 \sim 649$ times better energy per matrix performance compared to the most resent designs.

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TABLE III
Comparison of different decomposition algorithms.

| Algorithm                  | Matrix Size | Max. Frequency (MHz) | Power (mW) | Energy per Matrix (mJ) |
|----------------------------|-------------|----------------------|------------|------------------------|
| ERFH-SVD                   | 1×1 ~ 8×8   | 145                  | 0.01       | 0.0016                 |
| napSVD                     | 2×2/4/4×/6/6/6/6/8 | 125                  | 0.01       | 0.0016                 |
| 2-Sided Jacobi             | 2×2/4/4×/6/6/6/6/8 | 175                  | 0.01       | 0.0016                 |
| GR Based Adaptive SVD      | 2×2/4/4×/6/6/6/6/8 | 175                  | 0.01       | 0.0016                 |
| GK Based Adaptive SVD      | 2×2/4/4×/6/6/6/6/8 | 175                  | 0.01       | 0.0016                 |
| Algorithm based on [15]    | 1×1          | 145                  | 0.01       | 0.0016                 |
| Algorithm based on [16]    | 2×2/4/4×/6/6/6/6/8 | 125                  | 0.01       | 0.0016                 |
| Algorithm based on [17]    | 2×2/4/4×/6/6/6/6/8 | 175                  | 0.01       | 0.0016                 |
| Algorithm based on [18]    | 2×2/4/4×/6/6/6/6/8 | 175                  | 0.01       | 0.0016                 |
| Algorithm based on [19]    | 1×1          | 145                  | 0.01       | 0.0016                 |
| Algorithm based on [20]    | 2×2/4/4×/6/6/6/6/8 | 125                  | 0.01       | 0.0016                 |

1 The power numbers are considered with/without early termination method.
2 The power numbers are considered with/without early termination method.
3 Only the results for 2×2/4/4×/6/6/6/6/8 is mentioned in the table in favor of simplifying the presentation.
4 The power numbers are considered with/without early termination method.

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