Fully Anonymous Shared Memory Algorithms

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Abstract. Process anonymity has been studied for a long time. Memory anonymity is more recent. In an anonymous memory system, there is no a priori agreement among the processes on the names of the shared registers they access. As an example, a register named $A$ by a process $p$ and a shared register named $B$ by another process $q$ may correspond to the very same register $X$, while the same name $C$ may correspond to different register names for the processes $p$ and $q$. This article introduces the fully anonymous model, namely a model in which both the processes and the registers are anonymous. A fundamental question is then “is this model meaningful?”, which can be translated as “can non-trivial fundamental problems be solved in such a very weak computing model?” This paper answers this question positively. To this end, it shows that mutual exclusion, consensus, and its weak version called set agreement, can be solved despite full anonymity, the first in a failure-free system, the others in the presence of any number of process crashes. More precisely, the paper presents three fully anonymous algorithms. The first one is an $n$-process deadlock-free mutual exclusion algorithm which assumes read/modify/write registers. The model parameter $m$ defining the size of the anonymous memory (number of registers), the paper also shows that $m \in M(n) = \{ m \mid \forall \ell : 1 < \ell \leq n; \gcd(\ell, m) = 1 \}$ is a necessary and sufficient condition for the existence of such an algorithm. Considering the same model in which any number of processes may crash, an $n$-process wait-free consensus algorithm is presented. Finally, considering full anonymity and weaker registers (namely, read/write registers) an obstruction-free set agreement algorithm is presented. As far as we know, this is the first time full anonymity is considered, and where non-trivial concurrency-related problems are solved in such a strong anonymity context.

1 Introduction: Computing Model

1.1 On the process side

Process anonymity The notion of process anonymity has been studied for a long time from an algorithmic and computability point of view, both in message-passing systems (e.g., \cite{27,32}) and shared memory systems (e.g., \cite{4814}). Process anonymity means that processes have no identity, have the same code and the same initialization of their local variables (otherwise they could be distinguished). Hence, in a process anonymous system, it is impossible to distinguish a process from another process.
Process model  The system is composed of a finite set of \( n \geq 2 \) asynchronous, anonymous sequential processes denoted \( p_1, \ldots, p_n \). Each process \( p_i \) knows \( n \), the number of processes, and \( m \), the number of registers. The subscript \( i \) in \( p_i \) is only a notational convenience, which is not known by the processes. Sequential means that a process executes one step at a time. Asynchronous means that each process proceeds in its own speed, which may vary with time and always remains unknown to the other processes.

1.2 On the memory side

Memory anonymity  The notion of memory anonymity has been recently introduced in [30]. Let us consider a shared memory \( R \) made up of \( m \) atomic registers. Such a memory can be seen as an array with \( m \) entries, namely \( R[1..m] \). In a non-anonymous memory system, for each index \( x \), the name \( R[x] \) denotes the same register whatever the process that accesses the address \( R[x] \). Hence in a non-anonymous memory, there is an a priori agreement on the names of the shared registers. This facilitates the implementation of the coordination rules the processes have to follow to progress without violating the safety properties associated with the application they solve [18,25,29].

The situation is different in an anonymous memory, where there is no a priori agreement on the name of each register. Moreover, all the registers of an anonymous memory are assumed to be initialized to the same value (otherwise, their initial values could provide information allowing processes to distinguish them). The interested reader will find an introductory survey on process and memory anonymity in [26].

Anonymous shared memory  The shared memory is made up of \( m \geq 1 \) atomic anonymous registers denoted \( R[1...m] \). Hence, all the registers are anonymous. As already indicated, due to its anonymity, \( R[x] \) does not necessarily indicate the same object for different processes. More precisely, a memory-anonymous system is such that:

- For each process \( p_i \) an adversary defined a permutation \( f_i() \) over the set \( \{1, 2, \ldots, m\} \), such that when \( p_i \) uses the address \( R[x] \), it actually accesses \( R[f_i(x)] \),
- No process knows the permutations, and
- All the registers are initialized to the same default value denoted \( \bot \).

| Identifiers for an external observer | Local identifiers for process \( p_i \) | Local identifiers for process \( p_j \) |
|-------------------------------------|--------------------------------------|--------------------------------------|
| \( R[1] \)                          | \( R_i[2] \)                          | \( R_j[3] \)                          |
| \( R[2] \)                          | \( R_i[3] \)                          | \( R_j[1] \)                          |
| \( R[3] \)                          | \( R_i[1] \)                          | \( R_j[2] \)                          |
| Permutation                         | \( f_i() : [2, 3, 1] \)               | \( f_j() : [3, 1, 2] \)               |

Table 1. Illustration of an anonymous memory model

An example of anonymous memory is presented in Table 1. To make apparent the fact that \( R[x] \) can have a different meaning for different processes, we write \( R_i[x] \) when \( p_i \) invokes \( R[x] \).
Anonymous register model  We consider two types of anonymous register models.

– RW (read/write) model. In this model all the registers can be read or written by any process.

– RMW (read/modify/write) model. In this model, each register can be read, written or accessed by an operation that atomically reads the register and (according to the value read) possibly modifies it. More precisely, this operation, denoted \(\text{compare\&swap}(R[x], \text{old}, \text{new})\) has three input parameters, a register \(R[x]\) and two values \(\text{old}\) and \(\text{new}\), and returns a Boolean value. It has the following effect: if \(R[x] = \text{old}\) the value \(\text{new}\) is assigned to \(R[x]\) and the value \(\text{true}\) is returned (the \(\text{compare\&swap()}\) operation is then successful). If \(R[x] \neq \text{old}\), \(R[x]\) is not modified, and the value \(\text{false}\) is returned.

In both models, atomic \([20]\) means that the operations on the registers appear as if they have been executed sequentially, each operation appearing between its start event and its end event, and for any \(x \in \{1,...,m\}\), each read operation of a register \(R[x]\) returns the value \(v\), where \(v\) is the last value written in \(R[x]\) by a write or a successful \(\text{compare\&swap}(R[x],-,-)\) operation (we also say that the execution is linearizable \([19]\)). We notice that the RMW model is at least as strong as the RW model.

On a practical side, it was recently shown that epigenetic cell modifications can be modeled by anonymous entities cooperating through anonymous communication media \([27]\). Hence, fully anonymous distributed systems could inspire bio-informatics (and be inspired by it) \([22,23]\).

1.3 Content of the paper

This article addresses mutual exclusion and agreement in fully anonymous RMW and RW systems.

Mutual exclusion  Mutual exclusion is the oldest and one of the most important synchronization problems. Formalized by E.W. Dijkstra in the mid-sixties \([11]\), it consists in building what is called a lock (or mutex) object, defined by two operations, denoted \(\text{acquire()}\) and \(\text{release()}\). The invocation of these operations by a process \(p_i\) follows the following pattern: \(\text{acquire()}; \text{critical section}; \text{release()}\), where “critical section” is any sequence of code. It is assumed that, once in the critical section, a process eventually invokes \(\text{release()}\). A mutex object must satisfy the following two properties.

– Mutual exclusion: No two processes are simultaneously in their critical section.

– Deadlock-freedom progress condition: If there is a process \(p_i\) that has a pending operation \(\text{acquire()}\) (i.e., it invoked \(\text{acquire()}\) and its invocation is not terminated) and there is no process in the critical section, there is a process \(p_j\) (maybe \(p_j \neq p_i\)) that eventually enters the critical section.

Two memory-anonymous symmetric deadlock-free mutual exclusion algorithms are presented in \([3]\). One is for the RW register model, the other one for the RMW register model. These two algorithms are symmetric in the sense that the processes have identities that can only be compared for equality. We notice that algorithms for anonymous processes are, by definition, symmetric.
Mutual exclusion cannot be solved in the presence of process crash failures: if a process crashes just after it obtained the critical section, it will never release it, and consequently the upper layer application can block forever. The computing model must be enriched with additional computability power (for example with failure detectors, see e.g., [5, 10]) to be able to solve mutual exclusion in the presence of failures.

Consensus

Consensus is the most important agreement problem of fault-tolerant distributed computing. Let us consider that any number of processes may crash. A crash is a premature halting (hence, until it possibly crashes, a process behaves correctly, i.e., reliably executes its code). The consensus problem consists in building a one-shot operation, denoted propose(), which takes an input parameter (called proposed value) and returns a result (called decided value). One-shot means that a process can invoke the operation at most once. The meaning of this operation is defined as follows:

- Validity: A decided value is a proposed value.
- Agreement: No two processes decide different values.
- Liveness (Wait-freedom): If a process does not crash, it decides a value.

Algorithms solving consensus in different types of non-anonymous shared memory systems are described in several textbooks (e.g., [18, 25, 29]). In this paper, we consider the multi-valued version of consensus (i.e., the domain of proposed values is not restricted to be binary). While consensus can be solved from registers in a non-anonymous RMW memory [15], it cannot in a non-anonymous RW memory [13, 21]. It is, however, possible to solve a weaker version of consensus in non-anonymous RW system, when the progress condition is weakened as follows [16]:

- Liveness (Obstruction-freedom): If a process does not crash, and executes alone during a long enough period, it decides. I.e., if a process runs alone starting from some point in the execution then it decides after executing a finite number of steps.

Set agreement

Set agreement captures a weaker form of consensus in which the agreement property is weakened as follows:

- At most \( n - 1 \) different values are decided upon.

That is, in any given run, the size of the set of the decision values is at most \( n - 1 \). In particular, in runs in which the \( n \) processes propose \( n \) different values, instead of forcing the processes to agree on a single value, set agreement forces them to eliminate one of the proposed value. The set agreement problem as defined above is also called the \((n - 1)\)-set agreement problem [9]. While much weaker than consensus, as consensus, set agreement cannot be solved in non-anonymous RW memory systems [6, 17, 28] (and consequently cannot be solved in an anonymous memory either), but, as consensus, it can be solved when considering the weaker obstruction-freedom progress condition.

Content of the paper

Table 2 describes the technical content of the paper. As an example, the first line associated with consensus states that Section 3 presents a consensus algorithm for an anonymous RMW system for \( n > 1 \) and \( m \geq 1 \). As far as the mutex algorithm is concerned, it is also shown that \( m \in M(n) \), where \( M(n) = \{ \ell \mid \forall \ell : 1 < \ell \leq n : \gcd(\ell, m) = 1 \} \) is a necessary and sufficient condition on the size of the anonymous memory for such an algorithm.
Table 2. Structure of the paper

| Problem      | Section | Crashes | Reg. type | Progress condition | \( n \) | \( m \) |
|--------------|---------|---------|-----------|-------------------|-------|-------|
| Mutual exclusion | 2       | No      | RMW       | Deadlock-freedom  | \( n > 1 \) \( m \in M(n) \) |
| Consensus    | 3       | Yes     | RMW       | Wait-freedom      | \( n > 1 \) \( m \geq 1 \) |
| Set agreement| 4       | Yes     | RW        | Obstruction-freedom | \( n > 1 \) \( m \geq 3 \) |
| Consensus    | 5       | Yes     | RW        | Obstruction-freedom | \( n = 2 \) \( m \geq 3 \) |

2 Fully Anonymous Mutex using RMW Registers

As already mentioned, the mutual exclusion problem can be solved for non-anonymous processes in both the anonymous RW register model and the anonymous RMW register model [3]. However, there is no mutual exclusion algorithm when the processes are anonymous, even when using non-anonymous RW registers. To see that, simply consider an execution in which the anonymous processes run in lock-steps (i.e., one after the other) and access the RW registers in the same order. In such a run it is not possible to break symmetry as the local states of the processes will be exactly the same after each such lock-step.

2.1 A necessary and sufficient condition

Let us recall that two integers \( x \) and \( y \) are said to be relatively prime if their greatest common divisor is 1, notice that a number is not relatively prime to itself. Let \( M(n) = \{ m \text{ such that } \forall \ell : 1 < \ell \leq n : \gcd(\ell, m) = 1 \} \).

Theorem 1. There is a deadlock-free mutual exclusion algorithm for \( n \geq 2 \) anonymous processes communicating through \( m \geq 1 \) anonymous RMW registers if and only if \( m \in M(n) \).

Proof. The proof of the if direction, follows from the very existence of the deadlock-free mutual exclusion algorithm for \( n \) anonymous processes using \( m \) anonymous RMW registers, where \( m \in M(n) \), presented in Section 2.2 and proved in Section 2.3. The proof of only if direction, is an immediate consequence of the following observations:

- The lower bound result in [3], which states that \( m \in M(n) \) is a necessary and sufficient condition for symmetric deadlock-free mutual exclusion for \( n \) non-anonymous processes and anonymous RMW registers. As already noticed, algorithms for anonymous processes are, by definition, also symmetric.
- The non-anonymous processes and anonymous RMW registers model is at least as strong as the fully anonymous RMW model. \( \square \)

Remark. It is worth noticing that, from a distributed computing understanding and computability point of view, the condition \( m \in M(n) \) shows that, as far as deadlock-free mutual exclusion using RMW registers is concerned, there is no computability gap between full anonymity (as addressed here) and register-restricted anonymity (addressed
in [3]). Both require \( m \in M(n) \). Actually this condition tightly captures the initial “asymmetry” seed that allows \( n \) (anonymous or non-anonymous) processes to solve deadlock-free mutex using anonymous memory.

### 2.2 A Fully anonymous RMW mutex algorithm

**The anonymous memory** As already indicated, each RMW register of the anonymous memory \( R[1..m] \), is initialized to the value \( \perp \). Moreover, it is assumed that \( \perp \) is smaller than any non-negative integer.

**Local variables at each process** Each process \( p_i \) manages the following local variables.

- \( \text{max}_i \) is used to store the maximal value contained in a register (as seen by \( p_i \)).
- \( \text{counter}_i \) is used to store the number of registers owned by \( p_i \). A process owns a register when it is the last process that wrote a non-\( \perp \) value into this register.
- \( \text{myview}_i[1..n] \) is an array of Boolean values, each initialized to false. When \( \text{myview}_i[j] \) is equal to true, \( p_i \) owns the register \( R_i[j] \).
- \( \text{round}_i \) (initialized to 0) is the round number (rung number in the ladder metaphor, see below) currently attained by \( p_i \) in its competition to access the critical section.

When \( \text{round}_i = n \), \( p_i \) is the winner and can enter the critical section.

**Principle of the algorithm: concurrent climbing of a narrowing ladder** At some abstract level, the principle that underlies the behavior of the algorithm is simple. Assume there is a ladder with \( (n+1) \) rungs, numbered from 0 to \( n \). Initially, all the processes are at rung number 0 (hence their local variables \( \text{round}_i \) are equal to 0). For each process \( p_i \), \( \text{round}_i \) is equal to the rung number it attained. The aim of the algorithm is to allow processes to progress from a rung \( r \) to the next rung \( (r+1) \) of the ladder, while ensuring that, for any \( r \geq 1 \), at most \( (n-r+1) \) processes currently are at rung \( r \). From the local point of view of a process, this means that process \( p_i \) is allowed to progress to the rung \( r = \text{round}_i + 1 \) only when some specific condition is satisfied. This condition involves the notion of ownership of an anonymous register (see above), and the asymmetry assumption provided by the model, namely \( m \in M(n) \).

**Algorithm** The algorithm is described in Fig. 1. A process enters a “repeat” loop, that it will exit when it will have attained the last rung of the ladder, i.e., when \( \text{round}_i = n \). When \( \text{round}_i = r > 0 \), which means \( p_i \) is at round \( r \), it attempts to own more registers, by writing the rung number \( r \) in the registers it owned previously and in new registers. Its behavior in the loop body is composed of three parts.

- **Part 1:** lines 2-6. A process \( p_i \) first scans (asynchronously) all the registers to know the highest value they contain. This value is stored in \( \text{max}_i \) (lines 3-4). Then, if registers are different from \( \perp \) (i.e., are owned by some processes, we have then \( \text{round}_i < \text{max}_i \), line 5), \( p_i \) loops at lines 3-6 until it finds all the registers equal to \( \perp \). In short, as \( p_i \) sees that other processes climbed already at higher rungs, it stays looping at the rung numbered 0.

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4 This principle is not new. As an example it is found in Peterson’s \( n \)-process RW mutex algorithm, where processes raise and lower individual flags—visible by all processes—and write their identity in a size \( n \) non-anonymous memory [24].
Algorithm 1: Code of an Anonymous Process \( p_i \)

Constants:

\[ n, m: \text{positive integers.} \quad //\text{of processes and # of shared registers} \]

model constraint  
\[ //\forall \ell: 1 < \ell \leq n, m \text{ and } \ell \text{ are relatively prime} \]

Anonymous RMW shared registers:

\[ R[1..m]: \text{array of } m \text{ anonymous RMW registers, initially all } \perp \quad //\perp < 0 \]

Local variables:

\[ \text{myview}[1..m]: \text{array of } m \text{ Boolean bits, initially all } \text{false} \quad //\text{indicates ownership} \]

\[ \text{counter}, \text{round}, \text{max}: \text{integer} \]

operation \text{acquire()} is

1. \text{counter} \leftarrow 0; \text{round} \leftarrow 0 \quad //\text{begin entry code} 
2. \text{repeat} 
3. \text{max} \leftarrow 0 \quad //\text{check if another process is in a higher round} 
4. \text{max} \leftarrow \max(\text{max}, R_i[1], \ldots, R_i[m]) \quad //\text{find maximum in } R_i[1..m] 
5. \text{if round}_i < \text{max}, \text{then round}_i \leftarrow 0 \quad //\text{withdraw from the competition} 
6. \text{else round}_i \leftarrow \text{round}_i + 1 \quad //\text{continue to the next round} 
7. \text{if round}_i = 1 \text{ then} \quad //\text{first round} 
8. \quad \text{for each } j \in \{1, \ldots, m\} \text{ do} \quad \text{try to own as many shared} 
9. \quad \quad \text{myview}[j] \leftarrow \text{compare\&swap}(R_i[j], \perp, 1) \quad \text{registers as possible} 
10. \quad \text{if myview}[j] \text{ then counter, } \leftarrow \text{counter, } + 1 \text{ fi fi} \quad \text{own one more} 
11. \text{if round}_i \geq 2 \text{ then} \quad //\text{try to own additional released registers} 
12. \quad \text{for each } j \in \{1, \ldots, m\} \text{ do} \quad \text{try to own additional released} 
13. \quad \quad \text{myview}[j] \leftarrow \text{compare\&swap}(R_i[j], \perp, \text{round}_i) \quad \text{registers as possible} 
14. \quad \text{if myview}[j] \text{ then counter, } \leftarrow \text{counter, } + 1 \text{ fi fi} \quad \text{own one more} 
15. \text{if round}_i \geq 1 \text{ then} \quad //\text{not eliminated} 
16. \quad \text{competitors} \leftarrow n - \text{round}_i + 1 \quad //\text{max # of competing processes} 
17. \text{if counter, } < m/\text{competitors} \text{ then} \quad //\text{withdraw from the competition} 
18. \quad \text{for each } j \in \{1, \ldots, m\} \text{ do} \quad //\text{since not own enough registers} 
19. \quad \quad \text{if myview}[j] \text{ then } R_i[j] \leftarrow \perp; \text{myview}[j] \leftarrow \text{false} \text{ fi od} \quad //\text{release} 
20. \quad \text{wait}(\forall j \in \{1, \ldots, m\}: R_i[j] = \perp); \quad //\text{wait until all are } \perp 
21. \quad \text{counter, } \leftarrow 0; \text{round}_i \leftarrow 0 \text{ fi} \quad //\text{start over} 
22. \text{until round}_i = n \quad //\text{until the winner owns all } m \text{ registers} 
23. \text{return (done).} 

operation \text{release()} is

27. \text{for each } j \in \{1, \ldots, m\} \text{ do } R_i[j] \leftarrow \perp; \text{myview}[j] \leftarrow \text{false} \quad //\text{release all} 
28. \text{return (done).} 

Fig. 1. Deadlock-free mutual exclusion for \( n \) anonymous processes and \( m \in \mathcal{M}(n) \) anonymous RMW registers
– Part 2: lines 7-17. This part subdivides in two sub-parts, according to the round number of \( p_i \). In both cases, \( p_i \) tries to own as many registers as possible.

- \( \text{round}_i = 1 \). In this case, \( p_i \) owns no registers. So, it scans the anonymous memory and, for each register \( R_i[j] \), it invokes \( \text{compare}\&\text{swap}(R_i[j], \bot, 1) \) to try to own it. If it succeeds, it updates \( \text{myview}_i \) and \( \text{counter}_i \) (line 8-10).

- \( \text{round}_i \geq 2 \). In this case, \( p_i \) became the owner of some registers during previous rounds. It then confirms its ownership of these registers with respect to its progress to the current round \( r \) (line 12-13). Then it attempts to own more registers. But, to ensure deadlock-freedom, it considers only the registers that contain a round number smaller than its current round \( r \). The array \( \text{myview}_i \) and the local variable \( \text{counter}_i \) are also updated according to the newly owned registers (line 14-17).

– Part 3: lines 18-24. The aim of this part is to ensure deadlock-freedom. As the proof will show, if \( p_i \) attains rung \( r > 0 \) (i.e., \( \text{round}_i = r \)), there are at most \( (n - r + 1) \) processes competing with \( p_i \) (line 19), and these processes attained a rung \( \geq r \). In this case, at least one of them (but not all) must withdraw from the competition so that at most \( (n - r) \) processes compete for the rung \( r \).

The corresponding “withdrawal” predicate is \( \text{counter}_i < m/(n - r + 1) \) (line 20), which involves the asymmetry-related pair \((n, m)\) and \( \text{round}_i = r \), which measures the current progress of \( p_i \). If the withdrawal predicate is false and \( p_i \) attained \( \text{round}_i = n \), it enters the critical section (predicate of line 25). If the predicate is false and \( \text{round}_i < n \), \( p_i \) re-enters the loop, to try to own more registers and progress to the next rung of the ladder.

If the withdrawal predicate is true, \( p_i \) releases all the registers it owns and updates \( \text{myview}_i \) accordingly (lines 21-22). Then, it waits until it sees all the registers equal to their initial value (lines 23). After that, \( p_i \) resets its local variables to their initial values (lines 24), and re-enters the loop body.

**Abortable mutex** Let a deadlock-free abortable mutex algorithm be a mutex algorithm that, while it always satisfies the deadlock-freedom property, allows an invocation of acquire() to return the control value abort in the presence of concurrency (see, e.g., [25,29]). In this case, the invoking process \( p_i \) learns that the critical section is currently used by another process. From its point of view, it is as if it did not invoke acquire(). Let us observe that, with abortable mutex, all the invocations of acquire() terminate (some obtaining done and others obtaining abort). The previous algorithm can be easily transformed into a deadlock-free abortable algorithm by replacing the statement \( \text{round}_i \leftarrow 0 \) by \( \text{return} (\bot) \) at line 5, and replacing the lines 23-24 by \( \text{return} (\text{abort}) \).

**Remark** The algorithm remains correct if the predicate of line 25 is replaced with the predicate “\( \text{counter}_i = m \)”, namely once a process owns the \( m \) registers it may enter its critical section. This shows that the algorithm establishes a strong termination-related relation between the number of asynchronous rounds (i.e., time) and the size of the memory (i.e., space).
2.3 Proof of the algorithm

Reminder: \( M(n) = \{ m \text{ such that } \forall \ell : 1 < \ell \leq n : \gcd(\ell, m) = 1 \} \). Moreover, let us say that “process \( p_i \) executes round \( r \)” when its local variable \( \text{round}_i = r \).

**Lemma 1.** Let \( m \in M(n) \) and \( r \in \{2, ..., n\} \). The values \( m/(n-r+1) \) are not integers.

**Proof.** The set of the values \( (n-r+1) \) for \( r \in \{1, ..., n-1\} \) is \( X = \{n, n-1, ..., 2\} \). The fact that, for any \( x \in X \), \( m/x \) is not an integer is a direct consequence of the definition of \( m \), namely, \( m \in M(n) \).

**Lemma 2.** Let us consider the largest round \( r \) executed by processes. At most \( (n-r+1) \) processes are executing a round \( r \).

**Proof.** Let us consider a process that executes line 6, where it sets its local variable \( \text{round}_i \) to 1. As there are \( n \) processes, trivially at most \( n \) processes are simultaneously executing round \( r = 1 \). Let us assume (induction hypothesis) that round \( r \) is the largest round currently executed by processes, and at most \( (n-r+1) \) processes execute it.

We show that at most \( (n-r) \) processes will execute round \( r+1 \).

Let \( P_r \) be the set of processes that execute round \( r \). Let us consider the worst case, namely, \( |P_r| = n-r+1 \). We have to show that at least one process of \( P_r \) will not execute round \( (r+1) \). This amounts to showing that at least one process \( p_i \) of \( P_r \) never exits the wait statement of line 23, or executes line 24 where it resets its variable \( \text{round}_i \) to 0. Whatever the case, this amounts to showing that there is at least one process \( p_i \) of \( P_r \) for which the predicate \( \text{counter}_i < m/(n-r+1) \) is satisfied at line 20.

When a process of \( P_r \) exits the set of statements of lines 8-10 when \( r = 1 \), or line 12-17 when \( r > 1 \), the value of each anonymous register is \( \geq r \). Let us observe that, when different from 0, the local variable \( \text{counter}_i \) of a process \( p_i \) counts the number of anonymous registers that this process set equal to \( \text{round}_i \), where \( \text{round}_i = r \), i.e., \( \text{counter}_i = |\{x \text{ such that } \text{myview}_i[x] = \text{true}\}| \) (line 8-10 when \( \text{round}_i = 1 \), and lines 12-17 when \( \text{round}_i > 1 \)). Notice also that, in the last case, \( \text{counter}_i \) increases from round to round and thanks to the atomicity of the operation \( \text{compare\&swap}(R[j], \perp, \text{round}_i) \) at line 9 or 16 that, with respect to the registration in the local variables \( \text{myview}_i[1..n] \), no anonymous register can be counted several times by the same process or counted by several processes.

Assume (by contradiction) that the predicate of line 20 is false at each process of \( P_r \), and let \( \text{counter}(x) \), for \( 1 \leq x \leq |P_r| \), be the value of their counter variables. Then \( \text{counter}(1) + \cdots + \text{counter}(|P_r|) = m \), and each counter is greater or equal to \( m/(n-r+1) \). Hence, \( \forall x: \text{counter}(x) \geq m/(n-r+1) \). As, due to Lemma 1, \( m/(n-r+1) \) is not an integer, it follows that \( \forall x: \text{counter}(x) \geq [m/(n-r+1)] \).

And consequently, \( \text{counter}(1) + \cdots + \text{counter}(|P_r|) \geq (n-r+1)[m/(n-r+1)] \).

But \( (n-r+1)[m/(n-r+1)] > m \), a contradiction.

Hence, at least one local variable \( \text{counter} \) is such that \( \text{counter} < (m/(n-r+1)) \).

It follows that at least one process of \( P \) executes line 27, which concludes the proof of the lemma.

**Theorem 2.** No two processes are simultaneously in the critical section.
Proof. The theorem follows directly from the previous lemma and the fact that a process enters the critical section only when its local variable \(\text{round} = n\) (line 25).

\[\square\]

**Lemma 3.** Let \(r, 1 \leq r < n\) be the highest round attained by processes. At least one process attain the round \((r + 1)\).

Proof. Let \(r, 1 \leq r < n\), be the highest round attained by processes, and \(P(r)\) the corresponding set of processes. As in the proof of Lemma 2, let \(P_r\) be the set of processes that execute round \(r\). As previously, we have \(\text{counter}(1) + \cdots + \text{counter}(|P_r|) = m\).

If the predicate of line 20 is satisfied at each process of \(P_r\) we have \(\forall x : \text{counter}(x) < m/(n - r + 1)\). As due to Lemma 1, \(m/(n - r + 1)\) is not an integer, it follows that \(\forall x : \text{counter}(x) \leq \lfloor m/(n - r + 1)\rfloor\). Consequently, \(\text{counter}(1) + \cdots + \text{counter}(|P_r|) \leq \lfloor (n - r + 1) m/(n - r + 1) \rfloor\). But \((n - r + 1) m/(n - r + 1) < m\), a contradiction. \(\square\)

**Theorem 3.** If at some time no process is inside the critical section and one or more processes want to enter the critical section, at least one process will enter it.

Proof. The theorem follows directly from the previous lemma, applied from round 1 until round \(n\). \(\square\)

3 Fully Anonymous Wait-free Consensus using RMW Registers

When considering a fully anonymous system of size \(m = 1\), consensus can be easily solved with the \texttt{compare\&swap()} operation: the first process that writes its value in the single register \(R[1]\) (initialized to \(\perp\)) imposes it as the decided value (actually, when \(m = 1\) the memory is not really anonymous). When using anonymous objects, the fact that a given problem can be solved using only one object (i.e., \(m = 1\)) does not imply that the problem can also be solved using any finite number of \(m \geq 1\) objects [3].

The algorithm describes in Fig. 2 presents a simple consensus algorithm for any size \(m \geq 1\) of the anonymous RMW memory. This algorithm assumes that the set of values that can be proposed is totally ordered. Each process tries to write the value it proposes into each anonymous register. Assuming that at least one process that does not crash invokes \texttt{propose()}, there is a finite time after which, whatever the concurrency/failure pattern, each anonymous register contains a proposed value. Then, using the same deterministic rule the processes decide the same value (let us notice that there is an a priori statically defined agreement on the deterministic rule used to select the decided value).

4 Fully Anonymous Obstruction-free Set Agreement using RW Registers

We present an obstruction-free set agreement algorithm for crash-prone anonymous \(n\)-process system, where communication is through \(m \geq 3\) anonymous RW registers.
Fully Anonymous Shared Memory Algorithms

Algorithm 2: Code of an Anonymous Process $p_i$

Constants:

$n, m$: positive integers  // # of processes and # of shared registers

Anonymous RMW registers:

$R[1..m]$: array of $m$ RMW registers, initially all ⊥  // ⊥ cannot be proposed

operation propose($in_i$) is  // $in_i$ value proposed by $p_i$

1. for each $j \in \{1, ..., m\}$ do compare&swap($R_i[j], ⊥, in_i$) od  // try to write
2. return($\max(R_i[1], ..., R_i[m])$)  // decide the max value in $R[1..m]$.

Fig. 2. Consensus for $n \geq 2$ anonymous processes and $m \geq 1$ anonymous RMW registers

4.1 A fully anonymous RW set agreement algorithm

The algorithm is described in Fig. 3. The anonymous memory is made up of $m \geq 3$ RW atomic registers. Each anonymous RW register can store the preference of a process. Each participating process $p_i$ scans the $m$ registers trying to write its preference ($preference_i$) into each one of the $m$ registers. Before each write, the process scans the shared array (line 4), and operates as follows:

- If its preference appears in all the $m$ registers (line 9), it reads the array again (line 10), and if, for the second time, its preference appears in all the $m$ registers (line 11), it decides on its preference.
- Otherwise, if some preference appears in more than half of the registers (line 5), the process adopts this preference as its new preference (line 6).

Afterward, the process finds some arbitrary entry in the shared array that does not contain its preference (line 7) and writes it into that entry (line 8). Once the process finishes writing it repeats the above steps.

4.2 Proof of the algorithm

Lemma 4 (Set agreement and Termination under Obstruction-freedom). Any participating process that runs alone for a sufficiently long time, eventually decides. Moreover, the processes that decide, decide on at most $n - 1$ different values.

Proof. Clearly in all the runs in which less than $n$ processes decide, they decide on at most $n - 1$ different values. Below, we prove that in runs in which all the $n$ processes participate and decide, the $n$ processes decide on at most $n - 1$ different values.

Let $\rho$ be an arbitrary run in which all the $n$ processes participate and decide. We prove that, in $\rho$, the processes decide on at most $n - 1$ different values. Each one of the $n$ processes, before deciding (line 12), must first read all the $m$ registers (line 4), find out that its preference appears in all the $m$ registers (line 9), then it must read the array again (line 10) and only if, for the second time, its preference appears in all the $m$ registers (line 11), it may decide on its preference and terminate. We call these...
last two consecutive reads of the $m$ registers by a specific process a successful double collect (SDC) of that process. We emphasize that from the moment a process starts its successful double collect until it decides, the process does not write.

Let us denote by $p_i$ and $p_j$ the last two processes which start their SDC in the run $\rho$. Clearly, by definition, during these two last SDCs, each one of the other processes has either decided and terminated or has already started it SDC, and hence does not write during $p_i$ and $p_j$ SDCs. We show that $p_i$ and $p_j$ must decide on the same value which implies, as required, that the $n$ processes decide on at most $n - 1$ different values in $\rho$.

From now on we focus only on processes $p_i$ and $p_j$. Denote the value that $p_i$ decides on by $v$. Assume w.l.o.g. that $p_i$ has started its (last and only) SDC before process $p_j$ has started its (last and only) SDC. Let $t_0$, $t_1$ and $t_2$ denote: the last time $p_i$ enters the inner loop just before reading the $m$ registers (between lines 3-4), the last time at which $p$ exits the inner loop (between lines 9-10), and the time at which $p_i$ exits the outer loop (between lines 11-12), respectively. At the time interval $[t_0, t_2]$, $p_i$ never writes, and it completes an SDC. That is, $p_j$ reads the array twice, and in both cases finds out that its preference (i.e., $\text{mypref}_i$) appears in all the $m$ registers. There are three possible cases.

1. **Process $p_j$ does not write during the time interval $[t_0, t_1]$.** Thus, since in the time interval $[t_0, t_1]$, $p_i$ has found that the value of each one of the $m$ registers equals $v$, it must be that at time $t_0$, the value of each one of the $m$ registers equals $v$. After
time \( t_0 \), and before executing line 4, process \( p_j \) might write at most once into one of the \( m \) registers possibly overwriting the \( v \) value. Thus, when executing line 5, \( p_j \) will find that \( v \) appears in at least \( m - 1 \) of the entries of \( \text{myview}_j[1..m] \). Since \( m \geq 3 \), this means that \( p_j \) will find that \( v \) appears in more than half of the entries of \( \text{myview}_j[1..m] \). Thus, \( p_j \) will set its preference to \( v \) (line 6). From that point on, since \( p_i \) does not write anymore, the only possible decision value for \( p_j \) is \( v \).

2. Process \( p_j \) has written a value \( u \neq v \) during the time interval \([t_0, t_1]\). Since in the time interval \([t_1, t_2]\), \( p_i \) has found that the value of each one of the \( m \) registers equals \( v \), it must be that after writing the value \( u \), process \( p_j \) has later written the value \( v \) (overwriting \( u \)). Thus, between these two writings (of \( u \) and later \( v \)), \( p_j \) must have changed its preference to \( v \). From that point on, since \( p_i \) does not write anymore, the only possible decision value for \( p_j \) is \( v \).

3. Process \( p_j \) has written only the value \( v \) during the time interval \([t_0, t_1]\). Let \( t'_0 \) be the time after the last write of \( p_j \) in \([t_0, t_1]\). Since \( p_i \) never writes after \( t_0 \), at time \( t'_0 \) the values of all the registers written by \( p_j \) are \( v \). Also, the values of all the other registers must be \( v \), since this is their value when \( p_j \) reads them during \([t_0, t_1]\). Thus, \( p_j \) will never change its preference after \( t'_0 \), and the only possible decision value for \( p_j \) is \( v \).

We have shown that both \( p_i \) and \( p_j \) decide on the same value \( v \) in \( \rho \). Thus, the \( n \) processes together decide on at most \( n - 1 \) different values in \( \rho \).

Next, we show that each process eventually decides (and terminates) under obstruction-freedom (that is, if it runs alone for a sufficiently long time). When a process, say process \( p_i \), runs alone from some point on in a computation, \( p_i \) will read the shared array (line 4) and set its preference to some value \( v \). From that point on, in each iteration of the repeat loop, \( p_i \) will set one more entry of the shared array to \( v \). Thus, after at most \( m \) iterations the values of all the \( m \) entries will equal \( v \), and \( p_i \) will be able to exit the repeat loops, decide \( v \) and terminate.

Lemma 5 (Validity). The decision value is the input of a participating process.

Proof. At each point, the current preference of a process is either its initial input or a value (different from \( \bot \)), it has read from a register. Since a process may only write its preference into a register, the result follows.

Theorem 4. Algorithm 3 solves set agreement in a fully anonymous system made up of \( n \geq 2 \) processes and \( m \geq 3 \) anonymous RW registers.

Proof. The proof that the algorithm satisfies the Validity, Agreement, and Obstruction-freedom properties (which define set agreement) follows directly from Lemma 4 and Lemma 5.

5 Fully Anonymous 2-Process Obstruction-free Consensus using RW Registers

A simple instantiation of Algorithm 3 As the reader can easily check, instantiating Algorithm 3 with \( n = 2 \) provides us with 2-process obstruction-free consensus built using \( m \geq 3 \) RW registers.
Remark. Let us consider Algorithm 3, which assumes \( n \geq 2 \), in which the requirement \( m \geq 3 \) is strengthened to \( m \geq 2n - 1 \). It is tempting to think that the resulting algorithm solves obstruction-free consensus for \( n \) processes, however, this is incorrect as the resulting algorithm does not even solve obstruction-free consensus for three processes using five registers. Finding a counterexample is left as an exercise for the reader.

Finally, it was recently proved in [31] that there is no obstruction-free consensus algorithm for two non-anonymous processes using only anonymous bits. Thus, as was shown in [31], anonymous bits are strictly weaker than anonymous (and hence also non-anonymous) multi-valued registers.

6 Conclusions

This article has several contributions. The first is the introduction of the notion of fully anonymous shared memory systems, namely, systems where the processes are anonymous and there is no global agreement on the names of the shared registers (any register can have different names for distinct processes). The article has then addressed the design of a mutual exclusion algorithm and agreement algorithms (consensus and set agreement) in specific contexts where the anonymous registers are read/write (RW) registers or more powerful read/modify/write (RMW) registers. On the mutual exclusion side, the paper has shown that, for fully anonymous mutual exclusion based on RMW registers, the condition on the number \( m \) of registers, namely \( m \in M(n) = \{ m \text{ such that } \forall \ell : 1 < \ell \leq n : \text{gcd}(\ell, m) = 1 \} \), is both necessary and sufficient, extending thereby a result of [3] (which was for non-anonymous processes and anonymous registers).

Last but not least, let us notice that, despite the strong adversary context (full anonymity, and failures in the case of agreement algorithms), the proposed algorithms are relatively simple to understand. However, some of their proofs are subtle.

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Let us remind that simplicity is a first class property [1,12]. A stated by J. Perlis (the recipient of the first Turing Award) “Simplicity does not precede complexity, but follows it”.
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