A comprehensive investigation of silicon film thickness ($T_{SI}$) of nanoscale DG TFET for low power applications

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Abstract

In this work we demonstrate an N-channel tunnel field effect transistor (TFET) i.e. double gate N-TFET for improved subthreshold slope (SS) and OFF-state leakage current ($I_{OFF}$) with reference to drain bias ($V_{DS}$), and body thickness ($T_{SI}$). Device thickness is becoming a crucial parameter as more devices can be built on thin film and integrate double or multi-gate MOSFETs. In this model we analyze the impact of $V_{DS}$ and $T_{SI}$ on the device performances and express the limitation of $T_{SI}$ with respect to ON-state current ($I_{ON}$), electric field, energy band diagram, etc. TFETs have become popular because these devices can operate in the sub-threshold region with the larger transconductance to current ratio ($g_{m}/I_d$) than MOSFETs, the current turn-on mechanism being interband tunneling rather than thermionic emission. The proposed model can achieve a subthreshold swing less than 35 mV/decade that is desirable for designing low-power high-frequency analog integrated digital circuit applications.

Keywords: TFET, drain bias ($V_{DS}$), body thickness ($T_{SI}$), subthreshold slope (SS), short channel effects (SCEs), transconductance generation factor (TGF)

Classification numbers: 2.07, 3.02, 4.12, 5.01, 6.01

1. Introduction

According to the present scenario, the limitation of power consumptions in modern CPU should not be beyond 100 W as shown in [1]. Nowadays, the tunnel field effect transistor (TFET) is one of the most promising devices for low power digital circuit applications [2]. TFETs are beneficial because they can be operated at a very low power supply, and are suitable for biomedical applications like biosensors, etc due to their low power operating region [3]. The power dissipation of any analog device can be observed from its subthreshold operation. In addition, the TFET is more efficient as a generator of transconductance in the subthreshold region.

In the subthreshold operation, the subthreshold slope (SS) relates to the transconductance to current ratio ($g_{m}/I_d$) as [4]

$$
\frac{g_{m}}{I_d} = \ln 10 \frac{SS}{kT/q}
$$

(1)

$$
SS = \frac{kT}{q} \ln \left( 1 + \frac{C_d}{C_{ox}} \right) \ln 10
$$

(2)

where $g_{m}$ is transconductance, and $I_d$ is drain current, $C_d$ is depletion capacitance, $C_{ox}$ is oxide capacitance, $k$ is Bolzmann constant, $q$ is charge of electron, $T$ is temperature (K).

In metal oxide semiconductor field effect transistors (MOSFETs), the $g_{m}/I_d$ ratio is limited to values below 38.5 V$^{-1}$ due to the restriction of SS to 60 mV/decade at room temperature ($C_d \ll C_{ox}$). But TFETs are free of this drawback of MOSFETs with a higher transconductance to current ratio ($g_{m}/I_d$) at room temperature [5]. This is because the TFETs can achieve SS values less than 60 mV/decade at room temperature. The importance of the $g_{m}/I_d$ ratio is described in the following way: (1) it is strongly related to the...
performance of the analog circuits, (2) it also provides the operating region of the devices, and finally (3) it allows a tool for calculating the transistor dimensions like width, length, etc [6]. The working principle of the TFET is interband tunneling [7]; it means that the current injection mechanism of an N-channel tunnel field effect transistor (N-TFETs) is based on band to band tunneling (BTBT), i.e. an electron tunnels from the valence band of the source region into the conduction band of the intrinsic (channel) region.

Previously, Mishra et al [8] have proposed a single gate silicon on insulator (SOI) TFET by investigating the impact of the variation in $T_{SI}$ and gate oxide thickness ($T_{OX}$) on the device characteristics and they have also analyzed various analog and RF parameters like electric field, transconductance ($g_m$), drain conductance ($g_d$), gate capacitance ($C_{gs}$), cut-off frequency ($f_T$). However, this work mainly focuses on improving the SS, ON-state current ($I_{ON}$) by considering a double gate TFET (DG-TFET) device. The $T_{SI}$ is optimized by analysing the device characteristics and various performance parameters like the electric field, transconductance generation factor (TGF) and SS for the DG-TFET.

However, the only concern in TFETs is the ON-state current, which is very low as compared to conventional MOSFETs. Hence, there are many techniques used to improve the ON-state current without degrading the OFF-state current, such as (i) using a lower band gap semiconductor (SiGe, InGaAs, etc) at the source region [4, 9], and (ii) using high-k material, gate dielectric scaling, source and drain doping profile, which leads to an enhancement of the electric field (it improves the ON-state current) [10]. High-k spacer materials are widely used to enhance the device performance with more immunity towards the short channel effect (SCE) [11]. The design presented here is a DG N-TFET with a low-k gate dielectric to improve the drive current and ON–OFF ratio of the N-TFET. In order to evaluate the importance of $T_{SI}$ and optimize its value, we have performed the analysis of DG TFET with variations of $T_{SI}$. In this paper, we have demonstrated that the $I_{ON}$ is in the order of $10^{-6}$ A and $I_{OFF}$ is in the order of $10^{-18}$ A at $V_{DS} = 1.5$ V with respect to different $T_{SI}$. Due to its low ON-state and OFF-state currents, we can use this device for low-power complementary tunneling FET applications [12].

2. Device structure and simulation setup

The schematic layout and simulated device structure for an N-TFET are shown in figures 1 and 2, respectively. The device dimensions considered here are based on the International Technology Roadmap for Semiconductors [13], as shown in table 1. The source, drain, and intrinsic regions are formed with a specified dimension. A constant (or) uniform doping profile is used for all the regions, i.e. source, drain, and intrinsic regions. The source acts as a highly doped p-region with a concentration of $10^{20}$ atoms/cm$^3$; the intrinsic region is lightly doped with a concentration of $10^{17}$ atoms/cm$^3$ and the drain region acts as a highly n-type doped with a concentration of $10^{20}$ atoms/cm$^3$. An insulated gate material made up of silicon dioxide (SiO$_2$) with a dielectric constant of 3.9 is placed over the channel. The oxide thickness ($T_{OX}$) of the gate dielectric is 1 nm. Here, $T_{SI}$ is considered as a variable ranging from 5–30 nm. To achieve better performance, the $T_{SI}$ is a beneficial parameter because it leads to better gate control and the reduction of the bulk capacitive effect. The source, drain, and gate contacts are made with metal, and the work function of the gate metal is chosen as 4.1 eV.

For more accurate results, such as the ON-state current and OFF-state current, meshing is applied carefully for all the regions, i.e. source, drain and intrinsic regions. Two-dimensional simulations are done for double gate N-TFET using a
commercially available device simulator Sentaurus TCAD [14]. For the device operation of N-TFET, a positive drain to source voltage ($V_{DS}$) is applied. $V_{DS}$ is much less effective for the tunnel barrier width. But at a constant $V_{GS}$ when we increase the $V_{DS}$, after a certain point, drain induced barrier narrowing is introduced, which leads to SCE in the TFETs. The current injection mechanism of an N-TFET is based on the BTBT of electrons from the valence band of the source region to the conduction band of the intrinsic region. In TFETs, drain current under high gate and drain bias can be expressed by equation

$$I_D = A \int_{E_C}^{E_V} [F_S(E) - F_D(E)] T(E)N_SN_D dE.$$  \hspace{1cm} (3)$$

It is possible because the channel quasi-Fermi level is in equilibrium with the drain Fermi level at high gate and drain bias. In equation (3), $T(E)$ is the electron tunneling probability, because the ON-state current is proportional to the electron tunneling probability. $F_S(E)$ and $F_D(E)$ are the source and drain side Fermi–Dirac distributions, responsibility, and $N_S$ and $N_D$ are the corresponding density of states, $A$ is the area of the device. The integral range from $E_C$ to $E_V$ (source) represents the range of energies over which tunneling takes place. The Wentzel–Kramers–Brillouin expression for tunneling probability is shown in

$$T(E) = \exp \left( -4 \sqrt{2m^*E_g^3/3q} \right).$$ \hspace{1cm} (4)$$

where $E_g$ represents the barrier height seen by the particle touching the tunnel barrier (band-gap of the material in this case), $m^*$ is the effective mass of the tunneling particle (material dependent) and $F$ is the maximum electric field at the tunnel junction. It means that the lower band-gap, low mass materials (low $E_g$ and $m^*$) and higher electric fields will not make much difference for small values of $V_{GS}$ because the tunneling of electrons occurs based on the applied gate bias.

### 3. Results and discussion

The transfer characteristics ($I_D$–$V_{GS}$) of a double gate N-TFET with a channel length of 50 nm is shown in figure 3(a). From the characteristics, the variation of $V_{DS}$ does not make much difference for small values of $V_{GS}$ because the tunneling of electrons occurs based on the applied gate bias. The tunneling of electrons occurs when the value $V_{GS}$ is above the threshold voltage ($V_{Th}$). The value of $V_{Th}$ obtained from the transfer characteristics is shown in table 2.

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![Figure 3. Device transfer characteristics for different values of $V_{DS}$ and silicon film thickness ($T_{SI}$): (a) transfer characteristics for different values of $V_{DS}$; (b) transfer characteristics for different values of $T_{SI}$.

Table 2. Performance analysis of double gate TFET.

| Parameter       | Nomenclature     | $T_{SI} = 5$ nm | $T_{SI} = 7$ nm | $T_{SI} = 10$ nm | $T_{SI} = 30$ nm |
|-----------------|------------------|----------------|----------------|----------------|-----------------|
| $V_{Th}$ (V)    | Threshold voltage| 0.431          | 0.452          | 0.472          | 0.491           |
| SS (mV dec$^{-1}$) | Subthreshold slope | 25.458        | 28.407         | 33.227         | 46.941          |
| $I_{ON}$ (μA)   | ON-state current  | 0.453          | 0.310          | 0.237          | 0.102           |
| $I_{OFF}$ (pA)  | OFF-state current | $1.104 \times 10^{-4}$ | $8.215 \times 10^{-6}$ | $1.703 \times 10^{-6}$ | $4.366 \times 10^{-5}$ |
| $I_{ON}/I_{OFF}$ | ON–OFF ratio     | $4.09 \times 10^9$ | $37.7 \times 10^9$ | $139 \times 10^9$ | $2.35 \times 10^9$ |
result in higher ON-state currents [19]. The maximum TGF can be expressed as

$$\left( \frac{g_m}{I_{D}} \right)_{\text{max}} = \lim_{V_{GS} \rightarrow 0} \frac{g_m}{I_{D}},$$

(5)

where $E_g$ is the barrier height, $V_{GS}$ is the gate to source voltage.

Further, we consider the results with the variation of $T_{SI}$ at a particular drain to source voltage, i.e. $V_{DS} = 1.5$ V. The results are depicted in figure 3(b), as we decrease the $T_{SI}$, the ON-state current improved with a reference of 10 nm, and when $T_{SI}$ increases, the ON-state current is reduced. It means that a smaller value of $T_{SI}$ has better electrostatic control of the dual gate over the channel, which helps to eliminate the SCE. With an aligned gate dielectric, the improved electrostatics lead to an increase of the ON-state current and lower threshold voltage as well as lower SS when the silicon film thickness is made thinner. However, some limitations are observed with a decrease of $T_{SI}$ below 10 nm, i.e. the $I_{OFF}$ current degrades (as shown in table 2), due to the quantum mechanical effects [20, 21]. The Schrödinger formulation of quantum mechanics deals with the particle tunneling through an energy barrier, as with the propagation of evanescent electromagnetic waves [22]. The extremely narrow potential well is created for the lower $T_{SI}$ values because of the strong sub-band splitting and carrier confinement in the vertical direction [23].

Also, from the characteristics, we can state that the $I_{OFF}$ current is very low and the SS obtained is 25 mV/decade that are very small compared to conventional MOSFET [4]. The parameters extracted from the transfer characteristics are tabulated as shown in table 2 at $V_{DS} = 1.5$ V.

In TFETs, the electric field plays a very vital role in improving the ON-state current of the devices. As given in equation (5), when the electric field increases at the tunnel junction, the tunneling of the electron probability is improved that accelerates the drain current. There are many methods introduced to improve the electric field at the tunnel junction, such as: (1) gate dielectric scaling, (2) the realization of devices on ultrathin SOI structure, (3) underlap drain structure, and (4) source and drain doping profile.

As the tunnel width decreases with increasing $V_{DS}$, it results in an increase of the electric field at the tunnel junction. The variation of the electric field with $V_{DS}$ is shown in figure 4(a). Similarly, as the value of $T_{SI}$ decreases, the electric field of the tunnel junction is improved, as can be seen from figure 4(b). This is because of the inversely proportional nature of the electric field to the $T_{SI}$ according to the relation given in equation (5).

With the help of the energy band diagram, the ON–OFF state phenomenon of the double gate N-TFETs is explained in figure 5. As shown in figure 5(a), when $V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V, the tunnel barrier width is more and the height is less, so electrons do not have enough energy to move from the valance band of the source to the conduction band of the channel. This phenomenon is known as the OFF-state. As shown in figure 5(b), when $V_{GS} = 1.0$ V and $V_{DS} = 1.0$ V, the barrier width is less and the height is more; at $V_{DS} > V_{TH}$ the electrons have sufficient energy to move from one band to another band. This phenomenon is known as interband tunneling or ON-state.

Figure 6 shows that the energy barrier width is dependent on the applied $V_{GS}$ as well as $V_{DS}$. The barrier width is maximum at $V_{GS} = 0$ V, and as we increase the applied gate bias, the barrier width is reduced. However, at high values of $V_{GS}$, the barrier width starts to saturate. Hence, for the limited value of $V_{GS}$, the barrier width is effected and elsewhere it is constant.

Tunneling region (barrier height and width) is not much affected by the variation of $V_{DS}$ for a constant $T_{SI}$, as shown in figure 7(a). As $T_{SI}$ is decreased, the change in energy levels becomes less gradual from the source to the drain, as can be observed from figure 7(b). This analysis confirms the existence of a charge-neutral region, meaning that the surface region of the channel is less depleted of electrons because increasing the $V_{DS}$ results in less resistance in the tunnel junction. Thus, the ON-state current is improved. If we compare the electric field and band diagram, it concludes that

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**Figure 4.** The electric field behavior analysis of double gate N-TFET. The electric field variations (a) with different $V_{DS}$, and (b) with different silicon film thickness ($T_{SI}$).
the electric field is more, where the energy band is a steeper slope; elsewhere the electric field is approximately negligible.

Figure 8 shows the transconductance of a double gate N-TFET with the variation of $V_{DS}$ and $T_{SI}$. The transconductance increases by decreasing the $T_{SI}$. This happens due to the interrelation of transconductance to drain current (ON-state). From the above analysis, we have observed that the ON-state current is inversely proportional to the $T_{SI}$. The transconductance is also an important parameter for analog applications like gain, and the cut-off frequency of any device [24, 25].

Figure 9 shows the output or drain characteristics of the double gate N-TFET by varying $V_{GS}$ and $T_{SI}$. The output characteristic is improved and the threshold value is decreased with decreasing $T_{SI}$. The current achieves its optimum for $T_{SI} = 5$ nm.

Thus the transconductance generation factor (TGF) of TFETs is very high as compared to conventional MOSFETs. The maximum TGF, i.e. $(g_m/Id)_{max}$ is calculated with the help of equation (5) and the values of device thickness are presented in table 3.

Table 3 shows that the device thickness $T_{SI} = 5$ nm gives larger $(g_m/Id)_{max}$ values than the other values of $T_{SI}$. Such large values have been beneficial in the design of the circuits meant for analog applications.

The effect of $T_{SI}$ on the SS as well as on drain induced barrier lowering (DIBL) is shown in figure 10. Their
performances are improved by the reduction of $T_{SI}$ and that results in better gate control on the channel and also reduces SCEs.

Figure 11 shows the current density plot at fixed $V_{GS} = 1.0$ V and varying $V_{DS}$ as well as $T_{SI}$ of the double gate N-TFET. The current density is more at the drain region as compared to the channel region because, at higher $V_{DS}$, the accumulation of electrons is decreased at the channel region. By increasing $V_{DS}$, the maximum number of electrons is more depleted from the source region than at the channel region. On the other hand, we have observed that the current density increases as we decrease the $T_{SI}$ because the electron concentration per unit area will be increased.

Table 3. The maximum variation of transconductance generation factor ($g_m/I_d)_{max}$ at different silicon film thickness $T_{SI}$ (obtained from equation (5)).

| $T_{SI}$ (nm) | $(g_m/I_d)_{max}$ (V$^{-1}$) |
|--------------|-------------------------------|
| 5            | 1320                          |
| 7            | 1140                          |
| 10           | 486                           |
| 30           | 263                           |

Figure 8. The analog performance of the double gate N-TFET: transconductance variation with different values of (a) $V_{DS}$ and (b) silicon film thickness ($T_{SI}$).

Figure 9. Device output characteristics for double gate N-TFET: the output characteristics for different values of (a) gate voltage ($V_{GS}$) and (b) silicon film thickness ($T_{SI}$).

Figure 10. The subthreshold slope (black line) and DIBL (red line) is a function of double gate N-TFET silicon film thickness ($T_{SI}$).
4. Conclusion

In this paper, we have proposed TFETs that can operate at a very low subthreshold region with a higher transconductance generation factor \( \frac{g_{m}}{I_d} \) and a lower \( T_{Si} \). Details of the investigation have been carried out for a double gate N-TFET with reference to \( T_{Si} \) and \( V_{DS} \). By using the device with proper process parameters and biasing conditions, we can design low power analog circuits. For a \( T_{Si} \) of 5 nm, a high ON-state current can be achieved, which helps to increase the operating speed of the device. It is also compatible with lower DIBL so that it is less sensitive towards SCEs.

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