Characterization and TCAD Modeling of Mixed-Mode Stress Induced by Impact Ionization in Scaled SiGe HBTs

Nicolò Zagni, Member, IEEE, Francesco Maria Puglisi, Member, IEEE, Giovanni Verzellesi, Senior Member, IEEE, and Paolo Pavan, Senior Member, IEEE

Abstract— We investigate the reliability of state-of-the-art SiGe heterojunction bipolar transistors (HBTs) in 55-nm technology under mixed-mode stress. We perform electrical characterization and implement a TCAD model calibrated on the measurement data to describe the increased base current degradation at different collector-base voltages. We introduce a simple and self-consistent simulation methodology that links the observed degradation trend to interface traps generation at the emitter/base spacer oxide ascribed to hot holes generated by impact ionization (II) in the collector/base depletion region. This effectively circumvents the limitations of commercial TCAD tools that do not allow II to be the driving force of the degradation. The approach accounts for self-heating and electric fields distribution allowing to reproduce measurement data including the deviation from the power-law behavior.

Index Terms—Degradation, impact ionization (II), reliability, silicon germanium (SiGe) heterojunction bipolar transistor (HBT), TCAD modeling.

I. INTRODUCTION

Silicon germanium (SiGe) heterojunction bipolar transistors (HBTs) are currently the leading technology option for amplifiers for 5G networks and terahertz (THz) industrial automation, communications, and space exploration. Despite the high performance and cost-effectiveness, several aspects related to the reliability of these devices need to be addressed to further improve the technology and its pervasiveness [1]. Since HBTs are frequently driven close to the safe-operating-area (SOA) limits, they are prone to self-heating (SH) and degradation issues. Specifically, prolonged operation leads to degradation of the low-frequency gain $\beta$ due to base current increase, which is conventionally attributed to surface states generation at the emitter–base (E–B) spacer oxide due to impinging hot carriers generated by impact ionization (II) [4]–[7]. In earlier technologies such as the 0.13-μm process from IHP [4] and the first generation of the 55-nm process from STM [8], the base current degradation was reported to empirically follow a power-law. However, deviations occurred at some point in time (typically after several hours), depending on the specific stress conditions, which is thought to be related to the combined effect of SH and II dynamics [4]. Nevertheless, in the literature, the physics of this mechanism was either only partially analyzed [5], [7], or explained by empirical [4] or approximated analysis [6] that are better suited for aging compact models to be used in circuit simulations than for TCAD aging models to be exploited for degradation-aware device optimization. This calls for more comprehensive modeling efforts, especially with further device scaling.

In this article, we perform electrical characterization of mixed-mode (MM) stress reliability of state-of-the-art scaled second-generation SiGe HBT technology from STM under different collector–base stress voltages. We implement a TCAD model of the HBT device and calibrate it to reproduce the behavior of fresh devices. A self-consistent simulation methodology that considers SH and the effect of 2-D electric field distribution is then introduced that allows correctly reproducing MM stress data by ascribing the degradation to hot holes generated by II at the collector/base junction that drift toward the E–B spacer oxide. The developed model gives a direct empirical connection between trap generation rate and II rate in contrast to earlier reports that either i) computed the generation rate from hot carriers models [5] or from the energy distribution function of carriers [7]; or ii) derived an approximated analytical solution for the generated trap density with generation rates used as fitting parameters [6].

II. DEVICES AND EXPERIMENTS

The devices analyzed in this study are state-of-the-art SiGe HBTs fabricated in 55-nm bipolar complementary–metal–oxide–semiconductor technology (BiCMOS) by STM [9]. With respect to the first generation of the technology, device dimensions have been scaled in the vertical direction.
TABLE I
COMPARISON OF TECHNOLOGY PARAMETERS AND DIMENSIONS

| Parameter   | STM B55 [9] | HHP SG13S [10] |
|-------------|-------------|----------------|
| $A_E$ ($\mu$m$^2$) | 0.2 $\times$ 5.56 | 0.16 $\times$ 0.52 |
| $f_T$ (GHz) | 320         | 250            |
| $f_{\text{MAX}}$ (GHz) | 370         | 300            |
| $BV_{CE0}$, $BV_{CEO}$ (V) | 1.45, 5.2 | 1.7, 5.0 |

(e.g., base width $W_B$) and doping profiles were accordingly redefined, especially at base–collector junction. Each device is composed of two parallel HBT structures in the CBEB structure configuration with three emitter fingers, with an emitter width and length of $W_E = 0.20$ $\mu$m and $L_E = 5.56$ $\mu$m (in the third dimension), respectively. The Gummel curves at $V_{CE} = 1.2$ V and output curves at different $V_{BE}$ values (in the range 0.75–0.9 V) collected on fresh devices are shown in Fig. 2(a) and (b), respectively, with the latter showing the signature of a modest device SH only at $V_{BE} = 0.9$ V. The device dimensions and most relevant figures of merit are reported in Table I, benchmarked with HHP SG13S technology [10] (used for comparison also in the degradation analysis). To assess the reliability of the devices under study, we performed MM stress by forcing an emitter current density, $J_{E, STR}$, of 1 mA/$\mu$m$^2$, which corresponds to a $V_{BE}$ of $\approx$0.8 V. The base terminal is kept grounded while the voltage at the collector–base junction, $V_{CB, STR}$, is set to different values ranging from 1.5 to 2.1 V. These values are chosen as a reasonable trade-off between keeping stress conditions close to the operating ones and getting a non-negligible degradation in a reasonable amount of time, with the total stress time set to $10^4$ s. Indeed, in typical circuits for high-frequency applications such as power amplifiers, $V_{CB}$ ranges from 0 to 1.5 V [2], whereas $J_E$ (or equivalently $J_C$) varies in the range where the $f_T$ peaks—typically tens to tens of mA/$\mu$m$^2$ [1], [4]. The stress sequence was interrupted every 100 s to measure Gummel curves at $V_{CE} = 1.2$ V, as shown in Fig. 4(a), which allows extracting the relative increase (when compared to the fresh device) of $I_B$ at different $V_{CB, STR}$ as an indicator of the devices reliability. $I_B$ is evaluated at $V_{BE} = 0.7$ V to directly compare the results reported here with the outcomes of MM stress experiments performed on a previous technology (0.13 $\mu$m) and reported in the literature [4]. All measurements are performed at room temperature.

III. TCAD MODEL AND CALIBRATION

The sketch of the SiGe HBT device cross section implemented in the simulator is shown in Fig. 1. The TCAD simulation tool is the commercial software SDevice by Synopsys, Inc. [11]. The device structure was derived by refining an existing model in SDevice for the HBT device, and the mesh was revised to optimize the trade-off among computation time, simulation accuracy, and reproducibility. Comparison of measurement data and calibrated TCAD simulations is shown in Fig. 2, in terms of Gummel plot, Fig. 2(a), and output characteristics, Fig. 2(b). Because the dc MM stress conditions represent an upper limit to HBT degradation under RF operating conditions, here we discuss only the calibration of the device dc characteristics. Analysis of dynamic characteristics (to estimate $f_T$ and $f_{\text{MAX}}$, for instance) and comparison between measurements and simulations will be the subject of future work.

The Ge mole fraction ($x$) profile in the Si$_{1-x}$Ge$_x$ varies from 0 to 0.28 from the emitter to the collector junction. The base width was set to 26 nm ($W_B$ in Fig. 1). In agreement with results in the literature, the doping profile in the emitter is assumed flat, while a Gaussian doping profile is assumed in the base [1]. The doping profile in the collector/subcollector and, in general, the overall doping profile is in agreement with that suggested by a TCAD-based roadmap for SiGe HBT devices developed in the DOTSEVEN project [1]. Hydrodynamic simulations were carried out to correctly reproduce the currents in all regimes of operation [12]. The lattice, electron, and hole temperatures are self-consistently calculated in TCAD, which accounts for the effects of SH. Models for carriers’ recombination (and doping-dependent Shockley–Read–Hall), II (Okuto model), and field-, material-, and doping-dependent mobility [12]–[14] were also included. Calibrating such models for SiGe required only a slight tuning of few parameters in agreement with earlier literature reports [8], [14]. To consolidate the soundness of the calibration procedure, default values for Si and polysilicon were used. Series resistances and thermal resistances were also included at all contacts, and their values were calibrated to capture the behavior of the output curves in the saturation region and in the active region, respectively, as confirmed by the good agreement between experimental and simulated output curves at different $V_{CE}$ [Fig. 2(b)]. Specifically, the good agreement at high $V_{CE}$—when SH effects start to be visible—was obtained by tuning the thermal resistance at the emitter, base, and collector contacts (which strongly depend on the structure
of the overlying back-end-of line). Conversely, to strengthen the dependability of the calibration procedure, the substrate thermal resistance was set in agreement with previous reports in the literature [14]–[16]. In addition, finite carriers’ recombination velocity at the emitter was included [13]. Auger recombination and band-to-band tunneling were also included, as they are known to affect the excess base current at low bias. Finally, defects at the E–B spacer interface located at recombination and band-to-band tunneling were also included, which occurs at $t_\gamma \approx 2 \times 10^7$ s and $t_\gamma \approx 1.5 \times 10^4$ s for the STM and IHP technology, respectively. This deviation calls for a more precise modeling strategy of degradation phenomena.

In the following, we exploit TCAD simulations to refine our understanding of $I_B$ degradation (and its deviation from the single power-law behavior) by linking it to the effects of device geometry and II rate, and to check whether additional mechanisms must be considered in the description of the degradation. To this extent, the calibrated simulation deck is used to reproduce measured degradation data. Analogous conditions to those used during the stress tests (described in Section II) were adopted in the simulations. The constant emitter current density ($I_{E,STR} = 1$ mA/μm²) was set by applying a negative voltage to the emitter contact with the base grounded. This was done for numerical reasons as this solution guaranteed convergence for all stress conditions with different $V_{CB,STR}$. Stress was simulated for $t_{STR} = 10^2$, $10^3$, $10^4$ s, after which the $I_B$–$V_{BE}$ curves were recorded. The device aging in terms of interface traps generation (at the emitter/base access region—the SiGe/SiO₂ interface, see Fig. 1) was reproduced by adapting the reaction–diffusion (R–D) model available in SDevice [11]. The evolution of interface trap concentration ($N_{IT}$) reads

$$\frac{dN_{IT}}{dt} = v(N - N_{IT}) - \gamma N_{IT}$$

where $v(\gamma)$ is the depassivation (passivation) rate, $\gamma = \gamma_0 N_H/N_{IT}$ where $\gamma_0$ is obtained by imposing the equilibrium condition at $t = 0$, that is, $\gamma_0 = \nu_0 (N - N_{IT}^0)/N_{IT}^0$ ($N_{IT}^0$ is the concentration of defects at $t = 0$, $\nu_0$, and $\gamma_0$ are the depassivation/passivation constants, respectively). $N_H (N_{IT}^0)$ is the (equilibrium) hydrogen concentration at the interface (in the oxide). In this work, we assume degradation to be mostly limited by reaction, thus $N_H/N_{IT}^0 = 1$. The approach followed in [19], that considered similar depassivation rates but passivation rates depending on hydrogen concentration (and thus on the diffusion rate), reached similar conclusions regarding the deviation from the single “power-law” behavior (due to partial annealing of defects). The dependence of $v$ on the activation energy ($E_A^v$) and on the electric field is written.
as [11], [20]

\[ v = v_0 \exp \left( \frac{E_A^0}{kT_0} - \frac{E_A^0 + \Delta E_A}{E_T} \right) \]  

where \( \Delta E_A = -E(E_1) + (1 + \beta)E_T \ln(N_{IT}/N_{IT}^0) \) is the change in \( E_A^0 \) due to stretching of Si–H bonds by the perpendicular electric field and by chemical potential variation (first and second term, respectively). \( E_T = kT + E(E_1) \) is energy of hydrogen in Si–H bonds \( (T \) is the lattice temperature) that depends on the electric field parallel to the interface. However, this model as is cannot be successfully used to verify the role of II in the degradation dynamics since the depassivation rate does not depend directly on the hot carrier current, see (2). This comes from the fact that \( v \) does not depend on the excess carrier generation due to II. Thus, for reproducing the measurements in Fig. 4, we varied \( E_A^0 \) (see Table III) to equivalently take into account the effect of increased \( V_{CB,STR} \) in the R–D model. This allowed to self-consistently consider the effect of lattice temperature and both parallel and vertical electric field on the degradation process. It is important to observe that \( E_A^0 \) is varied only to mimic the \( v \) variation with \( V_{CB,STR} \) in the simulator without altering the model implementation itself (as done for example in [5]). The actual physical mechanism that causes \( v \) variation is in fact II, and not a change in \( E_A^0 \). The set of parameters that allows reproducing the measured data is reported in Table III. Specifically, the lattice temperature at different stress conditions was directly extracted from the TCAD by averaging the temperature profile along the E–B spacer interface. The resulting \( N_{IT} \) versus \( t_{STR} \) profile under the four different stress conditions obtained from these simulations are reported as symbols in Fig. 5(a).

The connection between \( v \) and hot carriers (generated by II) is then estimated by rewriting the depassivation rate change at each \( V_{CB,STR} \) in terms of an empirical factor \( k_{HC} \) as follows:

\[ v = v_0 \rho_{HC} \]  

where \( k_{HC} \) in (3) can be assumed to be a power-law function of hot carrier current [11] or II rate \( \alpha_n \) as follows:

\[ k_{HC} = 1 + \delta_{HC}(\alpha_n/\alpha_0)^{\rho_{HC}} \]  

where \( \delta_{HC} \) and \( \rho_{HC} \) are fitting parameters \( (\alpha_0 = 1 \text{ cm}^{-1}) \) is a normalization factor. To verify the validity of the proposed model and to determine the fitting parameters \( \delta_{HC} \) and \( \rho_{HC} \) we evaluated the relation between \( v/v_0 \) and the II coefficient \( \alpha_n \) as obtained from simulations. This is shown in Fig. 5(b), where the power-law trend is evidenced. The resulting fitting parameters are also shown in Fig. 5(b). Moreover, we compared the \( N_{IT} \) versus \( t_{STR} \) profiles obtained by using (1) and (2) by varying \( E_A^0 \) [symbols in Fig. 5(a)] with the ones obtained by using (1), (3), and (4) [black solid lines in Fig. 5(a)] obtaining an excellent agreement. Note that, while \( \alpha_n \) accounts for the likelihood of hot holes generation, the parameter \( \alpha_0 \) could be used to account for the probability of the generated hot holes to recombine or scatter while drifting toward the E–B spacer interface, which determines the generation rate of interface states. Therefore, in principle, \( \alpha_0 \) could be taken to be dependent on \( J_{E,STR} \), which regulates the scattering chance. Still, analyzing this dependence is out of the scope of this article and will be addressed in future works.

As shown in Fig. 4, the model allows reproducing the base current degradation at different stress times and conditions. The experimental and simulated \( I_B-V_{BE} \) curves at \( V_{CB,STR} = 1.5 \text{ V} \) for different \( t_{STR} \) in Fig. 4(a) show excellent agreement. Fig. 4(b) shows the experimental and simulated relative \( I_B \) variation (\( \Delta I_B = (I_B^0 - I_B^t)/I_B^0 \)) at a fixed \( V_{BE} = 0.7 \text{ V} \) (conventionally used to estimate the device lifetime [17]) for the four \( V_{CB,STR} \) [see legend in Fig. 4(b)] under investigation in this work. Notably, also the curvature of the degradation

---

**TABLE III**

| Parameter                  | Value                    |
|----------------------------|--------------------------|
| De-Passivation Constant \( (v_0) \) | \( 1.0 \times 10^4 \text{ s}^{-1} \) |
| Passivation Temperature \( (T_0) \) | \( 300 \text{ K} \) |
| Lattice Temperature \( (T) \) | \( [313.8; 314.6; 316.2; 318.6] \text{ K} \) |
| Activation Energy \( (E_A^0) \) | \( [0.8; 1.6; 2.3; 2.6] \text{ eV} \) |
| Bond Concentration \( (N) \) | \( 1.0 \times 10^{14} \text{ cm}^{-2} \) |
| Initial Trap Concentration \( (N_{IT}^0) \) | \( 8.8 \times 10^{12} \text{ cm}^{-2} \) |
| Power Exponent Coefficient \( (\beta) \) | \( 0.5 \) |
| Passivation Constant \( (\gamma_0) \) | \( 1.14 \times 10^4 \text{ cm}^{-1} \) |

---

**Fig. 4.** Comparison between simulations and measurements of the evolution of base current with stress time \( t_{STR} \). (a) \( I_B-V_{BE} \) curve for \( V_{CB,STR} = 1.5 \text{ V} \) at different \( t_{STR} \). (b) \( \Delta I_B \) (%) versus \( t_{STR} \) for different \( V_{CB,STR} \) (see legend). Good agreement between simulations and measurements is obtained under all conditions.

**Fig. 5.** (a) Comparison of simulated (black lines) and calculated (colored symbols) \( N_{IT} \) versus \( t_{STR} \) for different \( V_{CB,STR} \) (see legend). The calculation is achieved by combination of (1) and (3). (b) Comparison between simulated \( v/v_0 \) versus \( \alpha_n \) (II coefficient) and \( v/v_0 \) obtained from (3) and (4). The comparison shows how to effectively translate \( N_{IT} \) degradation as obtained from simulations with (1) and (3) (a) to II coefficient variation by fitting simulation data inserting the power-law model of (4) in (3).
trend in Fig. 4(b) is well captured (i.e., the deviation from the power-law approximation). The sudden base current increase occurring for $V_{CB,STR} = 2.1$ V at $I_{STR} \approx 2000$ s is likely due to collector–base junction breakdown (as confirmed by the concurrent collector current increase, not shown for brevity). This behavior could not be captured with simulations possibly due to the simplified simulated structure (see Fig. 1) that could lead to an underestimation of electric field peaks possibly present in the real device. However, since the goal in this work was to capture the base current degradation due to E–B spacer interface trap generation (ascribed to II-generated hot holes) at the E–B spacer oxide. This approach circumvented the limitations of commercial TCAD tools that do not allow II to be the driving force of the degradation. In addition, i) accounts for SH and electric fields distribution; ii) directly links the II coefficient ($\alpha_II$) to the generation of traps; and iii) allows reproducing measurement data including the deviation from the power-law behavior observed at relatively short stress times.

V. CONCLUSION

We investigated the reliability of state-of-the-art SiGe HBTs in 55-nm technology under MM stress. Experimental results were successfully reproduced by using a TCAD model calibrated on fresh devices. We developed a self-consistent simulation methodology that connects the observed degradation trend to interface traps generation (ascribed to II-generated hot holes) at the E–B spacer oxide. This approach circumvents the limitations of commercial TCAD tools that do not allow II to be the driving force of the degradation. In addition, it i) accounts for SH and electric fields distribution; ii) directly links the II coefficient ($\alpha_II$) to the generation of traps; and iii) allows reproducing measurement data including the deviation from the power-law behavior observed at relatively short stress times.

REFERENCES

[1] M. Schroter et al., “SiGe HBT technology: Future trends and TCAD-based roadmap,” Proc. IEEE, vol. 105, no. 6, pp. 1068–1086, Jun. 2017, doi: 10.1109/JPROC.2015.2500024.

[2] B. Heinemann et al., “SiGe HBT technology with $f_T/f_{max}$ of 300GHz/500GHz and 2.0 ps CML gate delay,” in IEDM Tech. Dig., Dec. 2010, pp. 30.5.1–30.5.4, doi: 10.1109/IEDM.2010.5703452.

[3] P. Chevalier et al., “Towards THz SiGe HBTs,” in Proc. IEEE Bipolar/BICMOS Circuits Technol. Meeting, Oct. 2011, pp. 57–65, doi: 10.1109/BCTM.2011.6082749.

[4] G. G. Fischer and G. Sasso, “Aging and thermal recovery of advanced SiGe heterojunction bipolar transistors under long-term mixed-mode and reverse stress conditions,” Microelectron. Rel., vol. 55, nos. 3–4, pp. 498–507, Feb. 2015, doi: 10.1016/j.micrel.2014.12.014.

[5] K. A. Moen, P. S. Chakraborty, U. S. Raghunathan, J. D. Cressler, and H. Yasuda, “Predictive physics-based TCAD modeling of the mixed-mode degradation mechanism in SiGe HBTs,” IEEE Trans. Electron Devices, vol. 59, no. 11, pp. 2895–2901, Nov. 2012, doi: 10.1109/TED.2012.2210898.

[6] C. Mukherjee, T. Jacquet, G. G. Fischer, T. Zimmer, and C. Maneux, “Hot-carrier degradation in SiGe HBTs: A physical and versatile aging compact model,” IEEE Trans. Electron Devices, vol. 64, no. 12, pp. 4861–4867, Dec. 2017, doi: 10.1109/TED.2017.2766457.

[7] H. Kamrani et al., “Microscopic hot-carrier degradation modeling of SiGe HBTs under stress conditions close to the SOA limit,” IEEE Trans. Electron Devices, vol. 64, no. 3, pp. 923–929, Mar. 2017, doi: 10.1109/TED.2017.2653197.

[8] F. M. Puglisi, L. Larcher, and P. Pavan, “Mixed-mode stress in silicon–germanium heterostructure bipolar transistors: Insights from experiments and simulations,” IEEE Trans. Device Mater. Rel., vol. 19, no. 2, pp. 275–282, Jun. 2019, doi: 10.1109/TDMR.2019.2912835.

[9] A. Gauthier et al., “450 GHz $f_T$ SiGe:C HBT featuring an implanted collector in a 55-nm CMOS node,” in Proc. IEEE Bipolar Compound Semiconductor Integr. Circuits Technol. Symp. (BICSTS), Oct. 2018, pp. 72–75, doi: 10.1109/BICSTS.2018.8551057.

[10] H. Rucker et al., “A 0.13 $\mu$m SiGe BiCMOS technology featuring $f_T/f_{max}$ of 240/330 GHz and gate delays below 3 ps,” IEEE J. Solid-State Circuits, vol. 45, no. 9, pp. 1678–1686, Sep. 2010, doi: 10.1109/JSSC.2010.2051475.

[11] Sentaurus Device Manual (O-2018.06), Synopsys, Mountain View, CA, USA, 2018.

[12] G. Wedel and M. Schroter, “Hydrodynamic simulations for advanced SiGe HBTs,” in Proc. IEEE Bipolar/BICMOS Circuits Technol. Meeting (BCTM), Oct. 2010, pp. 237–244, doi: 10.1109/BIPOL.2010.5667955.

[13] Z. Yu, B. Ricco, and R. W. Dutton, “A comprehensive analytical and numerical model of polysilicon emitter contacts in bipolar transistors,” IEEE Trans. Electron Devices, vol. 31, no. 6, pp. 773–784, Jun. 1984, doi: 10.1109/TED.1984.21606.

[14] V.-T. Vu. (2016). Exploration and Evaluation of a Novel Si/SiGe Heterojunction Bipolar Transistor Architecture for Next BiCMOS Generation. [Online]. Available: https://www.theses.fr/2016BORD0304.pdf

[15] S. Balanethiram, R. D’Esposito, A. Chakravorty, S. Fregonese, and T. Zimmer, “Extraction of BEOL contributions for thermal resistance in SiGe HBTs,” IEEE Trans. Electron Devices, vol. 64, no. 3, pp. 1380–1384, Mar. 2017, doi: 10.1109/TED.2016.2654615.

[16] S. Balanethiram, R. D’Esposito, S. Fregonese, T. Zimmer, J. Berkner, and D. Celi, “Extracting the temperature dependence of thermal resistance from temperature-controlled DC measurements of sige HBTs,” in Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM), Oct. 2017, pp. 94–97, doi: 10.1109/BCTM.2017.8112919.

[17] P. Cheng, C. M. Grees, A. Appaswamy, P. S. Chakraborty, and J. D. Cressler, “Modeling mixed-mode DC and RF stress in SiGe HBT power amplifiers,” in Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting, Oct. 2008, pp. 133–136, doi: 10.1109/BIPOL.2008.4662730.

[18] G. G. Fischer, “Analysis and modeling of the long-term ageing rate of SiGe HBTs under mixed-mode stress,” in Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM), Sep. 2016, pp. 106–109, doi: 10.1109/BCTM.2016.7738958.

[19] M. Courret et al., “Scalable compact modeling of trap generation near the EB spacer oxide interface in SiGe HBTs,” Solid-State Electron., vol. 169, Jul. 2020, Art. no. 107819, doi: 10.1016/j.sse.2020.107819.

[20] O. Penzin, A. Haggag, W. McMahon, E. Lyumkis, and K. Hess, “MOSFET degradation kinetics and its simulation,” IEEE Trans. Electron Devices, vol. 50, no. 6, pp. 1445–1450, Jun. 2003, doi: 10.1109/TED.2003.813333.