Towards Reverse Engineering Reversible Logic

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Abstract

Reversible logic has two main properties. First, the number of inputs is equal to the number of outputs. Second, it implements a one-to-one mapping; i.e., one can reconstruct the inputs from the outputs. These properties enable its applications in building quantum computing architectures.

In this paper we study reverse engineering of reversible logic circuits, including reverse engineering of non-reversible functions embedded into reversible circuits. We propose the number of embeddings of non-reversible functions into a reversible circuit as the security metric for reverse engineering. We analyze the security benefits of automatic synthesis of reversible circuits. We use our proposed security metric to show that the functional synthesis approaches yield reversible circuits that are more resilient to reverse engineering than the structural synthesis approaches. Finally, we propose scrambling of the inputs and outputs of a reversible circuit to thwart reverse engineering.

Index Terms—Reversible logic, Reverse engineering, Security, Structural synthesis, Functional synthesis, BDD synthesis, QMDD synthesis, Number of embeddings.

I. INTRODUCTION

The globalization of the design flow for integrated circuits (ICs) leads to security vulnerabilities such as reverse engineering [1]. IC counterfeiting, Intellectual Property (IP) piracy, unauthorized overproduction by the contract foundry [2], [3], and malicious circuit modification [4]. An adversary anywhere in the design flow can reverse engineer the IP/IC, steals its ownership, and make pirated copies. An untrusted foundry can overbuild ICs and distribute them illegally. Furthermore, detailed knowledge of the design can allow one to identify sensitive parts of the design and make malicious modifications, refereed to as Hardware Trojans.

Reverse engineering can discover the technology used in the device [5], extract the gate level implementation [1] and reveal the functionality of the design [6]. Software tools are used to reverse engineer the chip [7], [8]. An adversary can use reverse engineering to steal IP, illegally fabricate ICs and insert Hardware Trojans. Design-for-Trust techniques thwart reverse engineering of CMOS-based logic circuits. Obfuscation techniques have been proposed to hide the implementation and the functionality of the design by inserting additional gates, which are controlled by a secret key [9]–[11]. The design can function correctly only when the correct key is applied to these gates. IC camouflaging is a layout-level protection against malicious end users from extracting the gate level implementation of the design [12]–[14]. In camouflaging, layouts of the standard logic gates are designed to look alike. Most of these considerations focus on conventional CMOS-based technologies.

Reversible logic is a novel computing paradigm where one obtains not only the output value for a given input value but also the other way around. Obviously, reversible logic significantly differs from conventional CMOS-based non-reversible logic. In traditional CMOS-based logic, it is possible to infer some of the inputs of a conventional NAND gate if its output is 0 (then, both inputs are 1) while it is not possible to unambiguously infer the input values if the NAND gate output is a 1. Reversible circuits realize bijective n-input n-output functions that map each possible input vector to a unique output vector. This is beneficial in building quantum computing architectures [15] since quantum computations are inherently reversible [16], [17].

Besides, reversible logic has applications in low power computing [18], [19], adiabatic computing [20], encoder/decoder design [21]–[23], circuit verification [24], and optical computing [25].

Security assessment of reversible circuits is the focus of this paper. Reversible circuits differ significantly from conventional circuits and hence may be susceptible to these and other threats. For example, in reversible circuits fanout and feedback are not (directly) allowed and each circuit is realized as a cascade of reversible gates. Similarly, the function (which is not necessarily reversible) is embedded into a reversible circuit structure resulting in ancillary inputs and garbage outputs. We investigate how these unique constraints inform the security of reversible circuits with a particular focus on reverse engineering. We investigate the challenges for a reverse engineer assuming different levels of knowledge about the synthesis schemes. Next, we propose a metric to quantify the ability of a design to resist reverse engineering. Finally, we propose scrambling the inputs and outputs to make reverse engineering difficult. Overall, this paper provides a first understanding of the risks of reverse engineering in reversible logic.

The remainder of this paper is organized as follows. Section II provides a background on reversible logic. Then, reverse engineering of reversible circuits is analyzed in detail for
different threat models in Section III. In Section IV, we provide a simple input/output scrambling solution to thwart reverse engineering of reversible circuits. Experimental results in Section V demonstrate the difficulty of reverse engineering of non-reversible functions embedded into reversible circuits implementations and report the number of possible embeddings encountered by an attacker. We evaluate the proposed scrambling technique with respect to the number of possible embeddings and the costs. We conclude the paper in Section VI.

II. BACKGROUND

In this section, we provide an overview of reversible logic and established automatic synthesis approaches to realize a (not necessarily reversible) target function using reversible logic gates.

A. Reversible Logic

A reversible logic circuit has an equal number of input and output signals. Furthermore, the reversible circuit realizes a bijection, i.e. each input assignment maps to a unique output assignment. Accordingly, computations can be performed in both directions (from the inputs to the outputs and vice versa).

Reversible circuits are implemented as cascades of reversible gates. Each reversible gate over the inputs \( X = \{x_1, \ldots, x_n\} \) consists of a (possibly empty) set \( C_1 \subseteq \{x_j \mid x_j \in X\} \cup \{x_j \mid x_j \in X\} \) of positive \((x_j)\) and negative \((\overline{x_j})\) control lines and a set \( T \subset X \setminus C \) of target lines. The most commonly used reversible gate is the Toffoli gate \( \text{TOF}(C, x_t) \) \([26]\), which consists of a single target line \( x_t \in X \setminus C \) whose value is inverted if all values on the positive (negative) control lines are set to 1 (0) or if \( C = \emptyset \). All remaining values are passed through the gate unaltered. The cost of a reversible circuit is defined either by the number of gates or by so called quantum cost \([27]\). The quantum cost of a Toffoli gate with \( C \) positive control lines is computed as \( 2^{C+1} - 3 \), while for negative control lines, the quantum cost is computed in the same way except for the case where the Toffoli gate is entirely composed of negative control lines in which the cost is increased by two \([28]\).

Example 1. Fig. 1 shows a reversible circuit composed of three circuit lines and three Toffoli gates. The circuit is labeled with the values on the circuit lines for input \( x_3 x_2 x_1 = 001 \). The first gate \( g_1 = \text{TOF}(\{x_1\}, x_3) \) inverts the value of the target line \( x_3 \) since the positive control line \( x_1 \) is initialized to 1. The second gate \( g_2 = \text{TOF}(\{x_3, \overline{x}_2\}, x_1) \) inverts the value of the target line \( x_1 \). In contrast, the third gate \( g_3 = \text{TOF}(\{x_1\}, x_2) \) keeps the value of the target line \( x_2 \) intact, since the positive control line \( x_1 \) is 0.

In order to realize non-reversible functions, ancillary inputs and garbage outputs are used. An ancillary input of a reversible circuit is an input that is set to a fixed value (either 0 or 1). A garbage output of a reversible circuit is an output, which is a don’t care for all possible input conditions.

Example 2. Fig. 2 shows the realization of a full adder using reversible gates with the top input of the reversible circuit set to 0. The bottom two outputs are garbage outputs of this circuit.

B. Reversible Logic Synthesis

Several approaches to automatically synthesize non-reversible and reversible functions using reversible gates have been proposed (see e.g. \([29]–[34]\)). These synthesis approaches either implicitly or explicitly embed the target (reversible or non-reversible) function into a reversible function.

TABLE I

| \( \text{Table I} \) FULL ADDER AND A POSSIBLE EMBEDDING INTO A REVERSIBLE FUNCTION |
|---|
| (a) Full Adder | (b) Reversible Embedding |
| \( x \) | \( y \) | \( c_{in} \) | \( c_{out} \) | \( \text{sum} \) |
| \( 0 \) | \( 0 \) | \( 0 \) | \( 0 \) | \( 0 \) |
| \( 0 \) | \( 1 \) | \( 0 \) | \( 0 \) | \( 0 \) |
| \( 0 \) | \( 0 \) | \( 0 \) | \( 0 \) | \( 0 \) |
| \( 1 \) | \( 1 \) | \( 1 \) | \( 1 \) | \( 1 \) |
| \( 1 \) | \( 0 \) | \( 1 \) | \( 0 \) | \( 0 \) |
| \( 1 \) | \( 1 \) | \( 0 \) | \( 1 \) | \( 0 \) |
| \( 1 \) | \( 0 \) | \( 1 \) | \( 0 \) | \( 1 \) |
| \( 1 \) | \( 1 \) | \( 1 \) | \( 1 \) | \( 1 \) |

Example 3. Consider the full adder in Table [I(a)]. The full adder has the carry in \( c_{in} \) and summands \( x \) and \( y \) as the inputs and the carry out \( c_{out} \) and the sum as the outputs. The full adder is not reversible since (1) the number of inputs differs from the number of outputs and (2) there is no unique input-output mapping. Adding an additional output to the function does not make it reversible. The first four rows of the truth table can be embedded with respect to reversibility as shown in the rightmost column of Table [I(a)]. However, since \( c_{out} = 0 \) and sum = 1 already appeared twice (marked in bold), a unique embedding for the fifth row of the truth table is no longer possible. The same holds for the italicized rows.
Overall, at least $\lceil \log(m) \rceil$ garbage outputs are required to make a non-reversible function reversible, where $m$ is the maximum number of times an output pattern is repeated in the truth table of the target function. Three output patterns are repeated in the full adder truth table. $\lceil \log(3) \rceil = 2$ garbage outputs and, hence, one additional ancillary input are required to make the function reversible.

The value of the ancillary inputs can be chosen by the designer. Garbage outputs are by definition don’t cares leading to an incompletely specified function. However, many synthesis approaches require a completely specified function so that all don’t cares are assigned a concrete value. The adder is embedded in a reversible function including four variables, one ancillary input, and two garbage outputs.

**Example 4.** One possible assignment to the ancillary input and the don’t care values of the garbage output are shown in Table I(b). Here, the target full adder is obtained if the ancillary input $c_{in}$ is set to 0 and outputs $c_{out}$ and sum are observed. $g_1$ and $g_2$ are the two garbage outputs.

State-of-the-art synthesis approaches are of two kinds: In functional synthesis, the target function is embedded into a fully reversible function as sketched above (using methods such as in [35]–[37]). The resulting function is synthesized using methods directly relying on reversible function descriptions [31]–[34]. In structural synthesis, the target function is first represented by dedicated function descriptions such as Exclusive Sum of Products (ESoPs) or Binary Decision Diagrams (BDDs). They are then mapped to reversible circuits. Here, embedding is implicitly conducted during synthesis. [29], [30] are well-known structural synthesis approaches. In both schemes, the use of ancillary inputs and garbage outputs is essential to realize a non-reversible target function in reversible logic.

**III. REVERSE ENGINEERING OF REVERSIBLE CIRCUITS**

Reversible circuits obtained using the state-of-the-art synthesis methods are challenging to an adversary who has access to the gate level implementation aiming to reverse engineer a circuit. We illustrate these challenges first. Then, we discuss several reverse engineering threat models.

**A. Challenges for Reverse Engineering**

An adversary who has access to the gate level implementation of a circuit realizing a reversible function can trivially reverse engineer it. However, when a non-reversible function is embedded into a reversible circuit, a major challenge for the reverse engineer, who is unaware of the location of the inputs and outputs of the target function, is to identify the value and the location of the ancillary input bits and the location of the garbage output bits – both are vital to reverse engineer the target function.

**Example 5.** Consider the full adder embedding shown in Fig. 2. If the attacker is unaware of the location and values of the ancillary inputs, he/she cannot determine the target function. If $c_{in}$ is the ancillary input bit, setting $c_{in}$ to 0, results in $\text{sum} = x \oplus y$, while setting $c_{in}$ to 1, results in $\text{sum} = x \oplus y$. Another challenge for the attacker is to identify the primary and garbage output bits. In Fig. 2 any of the four output bits can be a garbage output. From the designer’s perspective, the reversible circuit in Fig. 2 realizes a full adder. Hence, he/she knows the primary outputs and the garbage outputs of the target function. If this information is unavailable, it is difficult to reverse engineer the functionality.

Overall, the ancillary inputs and garbage outputs can naturally hide the embedded, non-reversible target function. The key question is how can an attacker identify the ancillary inputs and determine their values and identify the garbage outputs from a gate-level netlist?

In the remainder of this paper, we will discuss these reverse engineering challenges. Different threat models will be considered according to the level of knowledge the attacker has about the synthesis approach used to derive the circuit. More precisely, what if the attacker

- is ignorant of the synthesis method used to generate the circuit,
- knows the synthesis method used to generate the circuit.

**B. Reverse Engineering without Knowing the Synthesis Approach**

If the attacker does not know how the circuit has been obtained, he/she cannot distinguish the garbage outputs from the primary outputs and the ancillary inputs from the primary inputs. Hence, his/her primary goal is to determine the location and value of the ancillary inputs as well as the location of the garbage outputs. We first derive the number of possible target functions embedded into a reversible circuit. This presents the difficulty of reverse engineering for an attacker. This analysis is independent of the synthesis approach used to generate the reversible circuit.

Assume that a reversible circuit has $n$ input/output bits. There are $2^n$ possible input/output combinations. The circuit can be represented as a function $f(x_1, x_2, \ldots, x_n) = (y_1, y_2, \ldots, y_n)$. Each $x_i$ can be either a primary input of the target function or an ancillary input, while each $y_i$, can be either a primary output of the target function or a garbage output, where $i$ varies from 1 to $n$.

Each output $y_i$, can be computed as $y_i = f_1(x_{i_1}, x_{i_2}, \ldots, x_{i_m})$, where $m_i (1 \leq m_i \leq n)$ is the number of inputs that drive $y_i$. Let $k_i$ ($0 \leq k_i \leq m_i$) be the number of inputs that drive $y_i$ but not $y_p$ where $p$ anywhere in the interval from 1 to $i - 1$ ($1 \leq p < i$). The number of possible embedded functions in $y_i$ can be obtained by considering any subset of the $k_i$ inputs as ancillary inputs. Thus, the number of possible embedded functions for $y_i$ is

$$e(k_i) = \sum_{j=0}^{k_i} C(k_i, j) \times 2^j$$  \hspace{1cm} (1)
where the binomial coefficient \( C(k_i, j) \) refers to the number of ways (combinations) of selecting \( j \) unordered ancillary inputs from \( k_i \) inputs. We denote the number of embedded functions with \( n \) primary output bits of a reversible circuit as

\[
E(n, K) = \prod_{i=1}^{n} e(k_i)
\]

(2)

where \( k_i \in K \).

However, each output bit of a reversible circuit can be either a primary or a garbage output. Thus, the number of all possible target functions embedded into a reversible circuit with \( n \) inputs/outputs is

\[
EMB(n, K) = (2^n - 1) \times E(n, K)
\]

(3)

where \( 2^n - 1 \) indicates the number of all possible combinations of the output bits of a reversible circuit. We subtract one to exclude the case where all the output bits of a reversible circuit are garbage.

**Example 6.** In Fig. 7 \( k_1 = 3, k_2 = 0, \) and \( k_3 = 0. \) Thus, \( e_1 = 27, e_2 = 1, \) and \( e_3 = 1. \) The number of possible embedded functions is \( 27 \times (2^3 - 1) = 189. \)

From the attacker’s perspective, it is hard to differentiate the target function from the other possible function embeddings. The number of possible embeddings can thus be used as the metric to assess the strength of defenses for reversible circuits against reverse engineering.

**C. Reverse Engineering Knowing the Synthesis Approach**

Next, we analyze how the attack changes when the adversary is aware of the synthesis approach used to generate the reversible circuit. More precisely, does the knowledge of the synthesis approach help the attacker to identify the positions and values of constant inputs and garbage outputs?

The attacker may utilize visualization tools such as \( \text{[38]} \) to highlight the structure and properties of a reversible circuit. Based on this information, the structure of the reversible circuit can be analyzed, the applied synthesis approach can be identified, and, possibly the target function can be reverse engineered.

In the following, we discuss this case considering circuits obtained by both, structural synthesis and functional synthesis reviewed in Section II-B. BDD-based synthesis \( \text{[30]} \) represents a structural synthesis approach and QMDD-based synthesis \( \text{[39]} \) represents a functional synthesis approach.

1) **BDD-based Synthesis of Reversible Logic:** In BDD-based synthesis as proposed in \( \text{[30]}, \) the target function is provided in terms of a Binary Decision Diagram (BDD) \( \text{[40]}, \) i.e. a directed acyclic graph \( G = (V, E) \) where e.g. a Shannon decomposition

\[
f = \overline{x_1} \cdot f_{x_1=0} + x_1 \cdot f_{x_1=1}
\]

is carried out in each node \( v \in V. \) The function \( f_{x_1=0} \) (\( f_{x_1=1} \)) is the negative (positive) co-factor of \( f \) obtained by assigning \( x_1 \) to 0 (1). In the following, the node representing \( f_{x_1=0} \)

\[
(\text{f}_{x_1=1}) \]

is denoted by \( \text{low}(v) \) (\( \text{high}(v) \)), while \( x_i \) is called the select variable.

**Example 7.** Fig. 3 shows a BDD representing the function \( f = \overline{x_1} \cdot x_2 \cdot x_3 \cdot x_4 + \overline{x_1} \cdot x_2 \cdot \overline{x_3} \cdot \overline{x_4} + x_1 \cdot x_2 \cdot \overline{x_3} \cdot x_4 + x_1 \cdot x_2 \cdot \overline{x_3} \cdot \overline{x_4} \) as well as the respective co-factors resulting from the application of the Shannon decomposition.

Given a BDD \( G = (V, E) \) of a function, a corresponding reversible circuit can easily be derived. To this end, all nodes \( v \in V \) of \( G \) are traversed in a depth-first fashion and substituted with a cascade of reversible gates. The respective cascade of gates depends on the successors of the node \( v. \)

![Fig. 3. BDD of \( f = \overline{x_1} \cdot x_2 \cdot x_3 \cdot x_4 + \overline{x_1} \cdot x_2 \cdot \overline{x_3} \cdot \overline{x_4} + x_1 \cdot x_2 \cdot \overline{x_3} \cdot x_4 + x_1 \cdot x_2 \cdot \overline{x_3} \cdot \overline{x_4} \)](image)

Fig. 3. BDD of \( f = \overline{x_1} \cdot x_2 \cdot x_3 \cdot x_4 + \overline{x_1} \cdot x_2 \cdot \overline{x_3} \cdot \overline{x_4} + x_1 \cdot x_2 \cdot \overline{x_3} \cdot x_4 + x_1 \cdot x_2 \cdot \overline{x_3} \cdot \overline{x_4} \)

In this manner, \( \text{low}(v) \) (\( \text{high}(v) \)) of each \( v \in V \), the select variable.

Thus, to realize the target function, decomposition is applied leading to smaller sub-functions for which existing building blocks can be applied. Then, the resulting sub-circuits can be composed to realize the overall function. Overall, this realizes arbitrary (i.e. not necessarily reversible) functions – at the expense of a huge number of additional lines leading to many ancillary inputs and garbage outputs.

2) **Reverse Engineering BDD-based Reversible Circuits:** BDD-based synthesis yields structured reversible circuits from which several properties can easily be obtained.

**Example 9.** Consider the circuit obtained by BDD-based synthesis as shown in Fig. 5. Fig. 5(a) and Fig. 5(b) show

\[
(\text{f}_{x_1=1}) \]

\[
(\text{f}_{x_1=0}) \]

Note that an additional circuit line is added to preserve the values of \( x_4 \) and \( x_3 \) which are still needed by the co-factors \( f_3 \) and \( f_4 \), respectively.
The attacker can exploit these properties to reveal the ancillary input value associated with sub-circuits, which can be reconfigured to universal gates, which can be recomputed to support different sub-functions depending on the associated ancillary input value. A reverse engineer can extract the value of the ancillary inputs associated with sub-circuits which have a unique structure. Assuming that the attacker knows the decomposition used to generate the BDD-based reversible circuit, he/she can generate the look-up table shown in Fig. 4. The attacker partitions the reversible circuit into sub-circuits, where each sub-circuit consists of the maximum number of adjacent reversible gates that match at least one sub-circuit in

![Image of reversible circuit](image1)

Fig. 4. Look-up table for reversible cascades representing Shannon decomposition of BDD. High(f) (low(f)) indicates the value of function f when the input $x_i$ is set to 1 (0).

![Image of reversible circuit](image2)

Fig. 5. Reversible Circuit derived from the BDD of $f$, where $p_i$ is the $i_{th}$ partition of the reversible circuit.

function embedded in a reversible circuit by:

1) Distinguishing primary and garbage outputs.
2) Identifying the location of the ancillary inputs.
3) Identifying the value of the ancillary inputs.

![Image of reversible circuit](image3)

Fig. 6. Visualization of Reversible Circuits: (a) Ancillary Inputs and Garbage Outputs, (b) Target and Control Lines

First, the attacker distinguishes the primary and garbage outputs of the reversible circuit. As shown in Fig. 6(b), the lines of the reversible circuit in the green region do not include any target line, and thus, they are connected to the garbage outputs, while the gate at the rightmost part of the reversible circuit is connected to the primary output. To this end, the second property discussed above can be exploited. Then, the attacker realizes the location of the ancillary inputs based on the first property. Finally, the attacker discovers the value of the ancillary inputs as follows:

1) Partitioning the reversible circuit into sub-circuits.
2) Identifying the ancillary input values of the sub-circuits.

Decomposition of a target function generates different co-factors, which can be represented as nodes of the BDD. Each node is substituted with the corresponding sub-circuit. Some sub-circuits have a unique structure, which enables identifying the associated ancillary input value, while others behave as universal gates, which can be recomputed to support different sub-functions depending on the associated ancillary input value. A reverse engineer can extract the value of the ancillary inputs associated with sub-circuits which have a unique structure. Assuming that the attacker knows the decomposition used to generate the BDD-based reversible circuit, he/she can generate the look-up table shown in Fig. 4.

In circuits obtained using BDD-based synthesis, the input $x_i$ is set to 1 (0).

1) the primary inputs are directly connected to the garbage outputs and
2) an intermediate output of a sub-circuit that has no control over other reversible gates is a primary output.

The attacker can exploit these properties to reveal the positions of the ancillary inputs and garbage outputs as well as the positions of control (green color) and target (yellow color) lines, respectively. The green region indicates the location of the primary inputs, which directly drive the garbage output bits of the BDD-based reversible circuit. The remaining inputs are ancillary inputs as illustrated in Fig. 6(a). The primary output of the reversible circuit is connected to the target line of right most gate as shown in Fig. 6(a).
the look-up table. Then the attacker maps each sub-circuit of the reversible circuit to the corresponding node in the look-up table to identify the associated ancillary input value, and thus, the target function.

**Example 10.** In Fig. 4, case 4 and 5 show an example of a sub-circuit that can represent any of two co-factors (nodes) depending on the associated ancillary input value. On the other hand, the sub-circuits in case 1, 2, 3, 6, and 7 represent unique co-factors (nodes).

**Example 11.** To illustrate the attack let us consider the reversible circuit in Fig. 5. BDD-based synthesis using Shannon decomposition is utilized to create the reversible circuit. The attacker first identifies the primary output, which is \( y_5 \) using the second property of the BDD-based reversible circuit. Also, he/she identifies the location of garbage outputs as they are directly connected to the inputs; here they are \( y_1, y_2, y_3 \), and \( y_4 \) derived using the first and second properties of the BDD-based reversible circuit. From the attacker perspective \( y_6, y_7, \) and \( y_8 \) are potential primary outputs. Then, the attacker determines the location of the ancillary inputs, which are \( x_5, x_6, x_7, \) and \( x_8 \) using the first property of the BDD-based reversible circuit. Next, the attacker partitions the reversible gates into sub-circuits as explained above. As shown in Fig. 5, the number of partitions is six. Let’s consider \( p_i \) as the \( i^{th} \) partition of the reversible circuit. \( p_1, p_2, \) and \( p_3 \) are mapped to case 7, 6, and 2 in Fig. 4, respectively. Thus, \( p_1, p_2, \) and \( p_3 \) can be uniquely identified. As a result, the value of the ancillary inputs \( x_6, x_7, \) and \( x_8 \) are 1, 0, and 0, respectively. However, \( p_0 \) can be mapped to case 4 or 5. Each of these two cases results in a different co-factor, which requires a different ancillary input bit value. As a result, the number of possible functions at \( y_5 \) is 2. In general, for \( m \) unknown ancillary input bits that drive a primary output \( y_i \), the number of possible realized functions at \( y_i \) is \( 2^m \). For each of the remaining output bits \( y_6, y_7, \) and \( y_8 \), the number of possible embeddings is 1. Thus, the number of possible embeddings for the reversible circuit in Fig. 3 is \( 2^3 \times 2 \), in which \( 2^3 \) indicates the number of all possible combinations of selecting potential primary output bits as primary output bits of the reversible circuit.

As we show in the experimental section, one can successfully identify all the primary outputs of reversible circuits synthesized using BDD-based tools.

3) **Functional Synthesis of Reversible Logic:** The embedded function in a reversible circuit may be hidden under different configurations of ancillary inputs and garbage outputs bits. Embedding a function results in a different number and value of ancillary inputs, while maintaining reversibility. In addition, the value of the garbage outputs as well as the outputs of the non-functional input assignments can be chosen arbitrary as long as they satisfy reversibility. Selecting the number and the value of the ancillary inputs combined with the possible locations where the garbage and the primary outputs can be placed can make reverse engineering of the target function more difficult.

**Example 12.** A possible embedding of the 1-bit adder into a reversible circuit. The value of the ancillary input that activates the target function, 0 in this example, can be replaced by a 1. Furthermore, one can assign different values to garbage output bits \( g_1 \) and \( g_2 \), while maintaining reversibility. For example, for input vector \( c_{in}, xy = 000, g_1, g_2 \) can be assigned 00, 01, 10, or 11. The output of the non-functional input assignments, when the ancillary input is 1 in this example, such as \( c_{out}, x y = 000 \), can be assigned an arbitrary value as well, such as \( c_{out}, x y, g_1, g_2 = 1100 \), as long as the given output is not used as an output for a functional input assignment that precedes this output in Table 1.

Quantum Multiple-valued Decision Diagrams (QMDD)-based synthesis [39] takes the reversible function generated by the embedding step and creates a reversible circuit. We omit the details of QMDD-based synthesis since the ancillary inputs and garbage outputs are placed during the embedding phase which is a preprocessing step prior to the functional synthesis approach. As discussed above, due to the embedding step, the structure of the resulting reversible circuit varies in the value, the number, and the location of the ancillary inputs as well as in the value and position of the garbage outputs.

**Example 13.** Fig. 7 shows the three possible reversible circuits for a 1-bit adder shown in Table 1(a), which have been obtained by QMDD-based synthesis with different values and numbers of ancillary inputs, garbage outputs, and outputs of non-functional input assignments.

![Fig. 7. QMDD-based reversible circuit of a 1-bit adder with: (a) two ancillary input bits of value 00, (b) a single ancillary input bit of value 0, (c) a single ancillary input bit of value 1.](image)

Assume that the attacker is unaware of the number, the value, and the location of ancillary input bits as well as the number and the value of the garbage outputs. That means, even if the attacker knows the used synthesis scheme, the number of possible target functions remains the same. The complexity of reverse engineering is introduced by the embedding phase.
and not the synthesis step, which makes it difficult to reverse engineer a reversible circuit by a rogue in the foundry even if he/she has access to the gate level netlist of the synthesized reversible circuit with the knowledge of the applied functional synthesis approach.

IV. INPUT AND OUTPUT SCRAMBLING

We have shown that the functional synthesis approaches (such as QMDD) are more resilient than structural synthesis approaches (such as BDD) to reverse engineering. To hamper reverse engineering of BDD-based reversible circuits, we propose scrambling the inputs or outputs of a synthesized reversible circuit by adding extra ancillary inputs or garbage outputs. Scrambling of inputs entails, not identifying which inputs are primary inputs and which inputs are ancillary inputs and what constant values are assigned to these ancillary inputs, while scrambling of the output entails, not identifying which outputs are primary outputs and which are garbage outputs.

Extra ancillary inputs or garbage outputs are added to the target function before the synthesis step. While the knowledge of the structural synthesis approach can assist in identifying the location and the value of the ancillary inputs and the location of the garbage output, the extra ancillary inputs and garbage outputs are independent of the structural synthesis approach. Scrambling the ancillary inputs and the garbage outputs will hinder an attacker’s ability to discover the target function.

Structural synthesis approaches, which realize arbitrary functions add additional ancillary inputs and garbage outputs regardless of the target functions, and thus, resulting in large number of circuit lines but relatively small quantum cost. While the attacker is able to identify the majority of the ancillary input bits of a reversible circuit generated using BDD-synthesis approach, in the presence of the extra ancillary inputs added prior to the realization of the embedded function, every input is a potential ancillary input. As a result, the number of possible embeddings increases significantly.

Example 14. Fig. 8(a) illustrates the BDD-based reversible circuit of function \( f \) in Fig. 3 in the presence of an extra ancillary input \( x_5 \) of value 0. Our proposed attack with the information of the synthesis approach in Section III-C2 can identify three ancillary input bits out of five introduced by the synthesis approach. However, the extra ancillary input can be any input classified as primary input by a reverse engineer, \( x_1, x_2, x_3, x_4, \) or \( x_5 \) are possible locations for the ancillary input.

Moreover, in the presence of extra garbage bits, every output of a reversible circuit generated using BDD-based (and thus structural) synthesis can be a potential output bit, which violates the second property of BDD-based reversible circuits as indicated in Section III-C2. Thus, although the attacker can identify most of the ancillary input bits, he/she can no longer differentiate the primary outputs from the garbage outputs, resulting in a significant number of possible embeddings.

Example 15. Fig. 8(b) illustrates the BDD-based reversible circuit of function \( f \) in Fig. 3 in the presence of an extra garbage output \( g_1 \). Both \( g_1 \) and \( f \) are connected to intermediate outputs of sub-circuits that do not control other reversible gates. In other words, the attacker can no longer distinguish \( g_1 \) from \( f \).

The size of the additional garbage outputs and ancillary inputs is driven by two optimization criteria, (1) maximizing the number of embeddings, and thus, the security level, and (2) minimizing the quantum cost. Increasing the number of garbage outputs and ancillary inputs results in increasing not only the number circuit lines and the quantum cost, but also the number of embeddings. In the experimental section, we analyze the trade-off between the security level in the presence of extra ancillary inputs/garbage outputs and their associated quantum cost.

Functional synthesis approaches can exploit the extra ancillary inputs and garbage outputs effectively to support reversibility at the expensive of large quantum cost.

Example 16. An ancillary input \( k \) can be added to the target function in Table II(a) with a value 0. The embedding phase takes updated target function as an input and generates the corresponding reversible function. One potential reversible function is given in Table II(b). Similarly, one can insert a garbage output bit such as \( g_1 \) to the target function in Table II(a) which can also lead to the reversible function in Table II(b).

V. EXPERIMENTAL RESULTS

To evaluate the difficulty of extracting the target (non-reversible) function from the reversible circuit, we have conducted various experiments. In each experiment, we report the number of possible embeddings as a security metric and the
quantum cost. We show the trade off between the security level and the hardware cost. First, we reverse engineer reversible circuits without the knowledge of the synthesis approach that generates the reversible circuit. Second, we reverse engineer reversible circuits with the knowledge of the applied synthesis approach. Finally, we launch our attacks on reversible circuits generated after adding extra ancillary inputs or garbage outputs to the target function. We consider reversible circuits generated using BDD-based synthesis as an example of the structural synthesis and QMDD-based synthesis as an example of the functional synthesis provided in RevLib [41].

A. Reverse Engineering without Knowing the Synthesis Approach

In the first set of the experiments we assume that the attacker does not know the synthesis approach used to generate the reversible circuit. In Table II and III we measure the number of possible embeddings of BDD- and QMDD-based reversible circuits, respectively. In Table II, column 5 indicate the target circuit name, the number of input/output bits, garbage output bits, and ancillary input bits, and the quantum cost of the reversible circuit, respectively. Column 6 and 7 are measured under the assumption that the attacker does not know the applied synthesis approach. %Garbage in
column 6 reports the percentage of leaked garbage output bits due to the direct connection between some of the inputs and outputs of the reversible circuit. These output bits can be easily classified as garbage outputs if the attacker has access to the gate level implementation of the circuit. #Embed func. reports the number of possible embeddings in column 7.

Table II shows that on average the attacker can identify 42% of the garbage output bits in BDD-based reversible circuits. However, the number of garbage output bits of BDD-based reversible circuits is significantly large. This is due to the fact that every node of the BDD can produce a garbage output. Moreover, the location and the value of the ancillary inputs are unknown to the attacker forcing him to explore a large number of possible embeddings using equation 3 in Section III-B.

The QMDD-based synthesis approach generates the reversible circuits whose core data is summarized in Table III using arbitrary values to ancillary inputs that satisfy the reversibility. Column 1 through 4 indicate the circuit name, the number of input/output bits, and garbage output bits, and the percentage of leaked garbage output bits by the attacker due to the direct connection between inputs and outputs of the reversible circuit, respectively. Columns 5 and 6 summarize the quantum cost and the number of possible embeddings, respectively.

The results show that the percentage of identified garbage output bits of QMDD-based reversible circuits is 35% on average. The number of embeddings of reversible circuits generated using BDD and QMDD synthesis approach is very large. However, the quantum cost of QMDD-based reversible circuits exceeds the corresponding one of BDD-based reversible circuits. We conclude that while reverse engineering reversible circuits with no information of the applied synthesis approach is always difficult, the quantum cost varies significantly based on the applied synthesis approach.

### B. Reverse Engineering Knowing the Synthesis Approach

In the second set of the experiments, we assume that the attacker knows the synthesis approach used to generate the reversible circuit. We launch our attack on BDD-based reversible circuits, while we note that reverse engineering QMDD-based reversible circuits with/without knowing the synthesis approach yields the same results. Column 8 through 9 in Table II provide the percentage of recovered ancillary input bits and the number of possible embeddings after reverse engineering the same BDD-based reversible circuits used in the previous experiment, however, giving that the attacker knows the applied synthesis approach.

We conclude that the attacker can identify the majority of the constant input bits value of BDD-based reversible circuits. On average 81.6% of the ancillary input bits can be recovered by the attacker. Thus, the attacker can identify most of the target function. The large number of possible embeddings in column 9 is due to the large number of potential primary outputs. Although the attacker can recover the location of primary outputs that satisfy the second property of BDD-based reversible circuits in Section III-C2 he/she can not determine whether the outputs of sub-circuits, which are connected to the reversible circuit outputs and also used to control other target lines, are garbage outputs. Thus, the number of all possible primary output combinations increases significantly depending on the size of these potential output bits. Our experiment shows that the attacker can identify all the primary outputs of the given BDD-based reversible circuits using our proposed reverse engineering except for three reversible circuits. In other words, the number of possible embeddings of the BDD-based reversible circuits can be reduced significantly by ignoring the potential primary outputs, which makes reverse engineering easier.

Fig. 9 shows a comparison between BDD- and QMDD-based (with 0-embedding) reversible circuits in terms of the

| Benchmark | #Input /Output | Garbage # | Quantum Cost | #Embed | Cir |
|-----------|----------------|-----------|--------------|--------|-----|
| 4mod5-v0_18 | 5/4 | 0/0 | 93 | 5.49E+06 |
| 4mod7-v1_96 | 5/3 | 3/3 | 187 | 2.31E+06 |
| 5xp1_194 | 17/7 | 14/3 | 2803 | 6.75E+35 |
| add3_196 | 19/12 | 8/3 | 16626 | 5.91E+39 |
| adr4_197 | 13/8 | 12/5 | 1625 | 4.98E+22 |
| aj-e11_165 | 4/0 | - | 89 | 710775 |
| alu1_198 | 20/12 | 25/0 | 215 | 5.65E+46 |
| alu2_199 | 16/10 | 40/0 | 28010 | 2.14E+40 |
| alu3_200 | 18/10 | 0/0 | 11156 | 2.54E+47 |
| alu4_201 | 22/14 | 28/6 | 3987932 | 2.39E+58 |
| apex4_202 | 28/9 | 44/4 | 282265 | 9.32E+45 |
| apla_203 | 22/10 | 0/0 | 18935 | 3.77E+40 |
| C7552_205 | 21/5 | 40/0 | 980 | 1.77E+47 |
| clip_206 | 14/9 | 44/4 | 35333 | 1.45E+43 |
| cm150a_210 | 22/21 | 0/0 | 2023 | 2.13E+45 |
| cm151a_211 | 28/19 | 68/4 | 8415 | 2.32E+49 |
| cm152a_212 | 12/11 | 72/7 | 236 | 5.19E+10 |
| cm42a_207 | 14/4 | 0/0 | 307 | 1.51E+36 |
| cm82a_208 | 8/5 | 40/0 | 155 | 7.32E+10 |
| cm85a_209 | 14/11 | 45/5 | 10242 | 2.31E+32 |
| cmb_214 | 20/17 | 23/5 | 32775 | 8.24E+49 |
| con2_215 | 15/14 | 14/2 | 229775 | 1.07E+25 |
| con1_216 | 9/7 | 42/9 | 254 | 1.24E+13 |
| cordic_218 | 25/23 | 8/3 | 102742609 | 7.00E+39 |
| cu_219 | 25/15 | 33/3 | 9674 | 1.47E+67 |
| dcl_220 | 11/4 | 0/0 | 368 | 6.72E+23 |
| dl_17_222 | 21/10 | 0/0 | 8284 | 8.62E+76 |
| example3_231 | 16/10 | 40/0 | 28010 | 3.04E+36 |
| f510_233 | 22/14 | 42/9 | 1028459 | 1.83E+66 |
| hw6_266 | 6/0 | 28/4 | 7358 | 6.01E+11 |
| hw8_27 | 7/1 | 0/0 | 31411 | 2.74E+15 |
| hwbv_211 | 8/1 | 0/0 | 152018 | 3.68E+39 |
| mises3_242 | 28/14 | 50/0 | 3321686 | 3.28E+122 |
| mlp4_245 | 16/8 | 75/0 | 12345 | 5.72E+47 |
| msp_258 | 10/7 | 0/0 | 3225 | 4.61E+20 |
| snr_260 | 12/8 | 0/0 | 1529 | 8.82E+27 |
| xor2_254 | 6/5 | 60/0 | 16 | 2.18E+47 |
| utf2_277 | 8/0 | - | 120705 | 3.68E+19 |
| table3_264 | 28/14 | 35/7 | 4301514 | 1.51E+119 |
| sao2_257 | 14/10 | 0/0 | 47224 | 6.94E+32 |
| pm1_249 | 14/4 | 0/0 | 307 | 2.99E+40 |
| rad6_250 | 13/8 | 0/0 | 1392 | 1.15E+32 |
| root_235 | 13/8 | 25/0 | 11798 | 1.04E+33 |
| ry6_256 | 17/16 | 87/5 | 254477 | 2.90E+26 |
| sym9_317 | 27/26 | 34/6 | 762136380 | 3.05E+155 |
| squar5_261 | 13/5 | 20/0 | 507 | 1.26E+35 |
| x2_267 | 17/10 | 30/0 | 1339 | 2.31E+32 |
number of embeddings and the quantum cost of a selected set of target functions given that the attacker knows the applied synthesis approach. Reverse engineering BDD-based reversible circuits generates less number of embeddings, and thus, it is easier to attack, compared to QMDD-based reversible circuits. On the other hand, the quantum cost of the QMDD-based reversible circuits exceeds the corresponding one of BDD-based reversible circuits.

C. Reverse Engineering Reversible Circuits with Input/Output Scrambling

We apply our attacks on BDD- and QMDD-based reversible circuits in the presence of extra ancillary inputs and garbage outputs. In Fig. 10 for each \( n \) input/output reversible circuit, we created five variants of the reversible circuit with \( 0, 0.1x, 0.2x, 0.5x, \) and \( x \) extra ancillary inputs, where \( x \) is the number of input/output bits of the reversible circuit.

Additional ancillary inputs significantly inflate the number of embeddings of not only QMDD-based reversible circuits but also BDD-based reversible. Every input classified as a primary input by reverse engineering BDD-based reversible circuit can be a potential ancillary input in the presence of our proposed input scrambling approach, which results in a massive increase in the number of embeddings. Moreover, increasing the number of the extra ancillary inputs in few BDD-based reversible circuits may result in a slight reduction in the quantum cost and the number of embeddings due to the random value of the ancillary input bits that determines the corresponding sub-circuits. Recall that Shannon decomposition used in BDD-based reversible circuits generates different sub-circuits, which have different numbers of gates. Some of these sub-circuits can easily be used to infer the associated ancillary input bit value, while others are difficult.

In the presence of additional garbage outputs in a BDD-based reversible circuit, the first step of the attack can not be applied anymore. As shown in Fig. 11 output scrambling of BDD-based reversible circuits results in a larger number of possible embeddings compared to input scrambling at the expense of high quantum cost.

While we show the impact of our proposed input/output scrambling on QMDD-based reversible circuits in Fig. 10(d), 10(c), 11(d), and 11(c) we emphasize that reverse engineering QMDD-based reversible circuits without applying our proposed input/output scrambling is still difficult.

VI. Conclusion

In this paper, we analyze reverse engineering of reversible logic. We focus on non-reversible functions embedded into reversible circuits. We measure the number of possible embeddings of reversible circuits implemented using different synthesis approaches and under different threat models as a security metric to evaluate the difficulty of extracting the target function through reverse engineering. We propose an attack to reverse engineering reversible circuits generated using BDD-based synthesis approach, an example of structural syntheses, that provides scalability at the cost of significant circuit lines overhead. We show that reversible circuits created using functional synthesis approaches are inherently secure against reverse engineering at the expense of high quantum cost. We also propose a countermeasure to thwart reverse engineering of BDD-based reversible circuits by adding extra ancillary inputs or garbage outputs prior to the synthesis step to scramble the inputs or the outputs of reversible circuits, respectively.

Our future work will explore reverse engineering of reversible circuits generated using synthesis approaches that provide both scalability and significant reduction in the number of circuit lines. Another direction is to develop a systematic way to identify the synthesis approach that generates a given reversible circuit considering all the state-of-the-art synthesis approaches.

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Fig. 10. Obfuscation using extra ancillary inputs. In BDD-based reversible circuits (a) Quantum Cost and b) number of embeddings. In QMDD-based reversible circuits (c) Quantum Cost and b) number of embeddings.

Fig. 11. Obfuscation using extra garbage outputs. In BDD-based reversible circuits (a) Quantum Cost and (b) number of embeddings. In QMDD-based reversible circuits (c) Quantum Cost and (b) number of embeddings.

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