Investigation of temperature dependent threshold voltage variation of Gd$_2$O$_3$/AlGaN/GaN metal-oxide-semiconductor heterostructure

Atanu Das, Liann Be Chang, and Ray Ming Lin

Citation: AIP Advances 2, 032159 (2012); doi: 10.1063/1.4750481
View online: http://dx.doi.org/10.1063/1.4750481
View Table of Contents: http://aip.scitation.org/toc/adv/2/3
Published by the American Institute of Physics
Investigation of temperature dependent threshold voltage variation of Gd$_2$O$_3$/AlGaN/GaN metal-oxide-semiconductor heterostructure

Atanu Das, Liann Be Chang, and Ray Ming Lin

Department of Electronic Engineering and Green Technology Research Center, Chang Gung University, Tao-yuan, Taiwan, 333, Republic of China

(Received 21 June 2012; accepted 22 August 2012; published online 29 August 2012)

Temperature dependent threshold voltage ($V_{th}$) variation of GaN/AlGaN/Gd$_2$O$_3$/Ni-Au structure is investigated by capacitance-voltage measurement with temperature varying from 25$^\circ$C to 150$^\circ$C. The $V_{th}$ of the Schottky device without oxide layer is slightly changed with respect to temperature. However, variation of $V_{th}$ is observed for both as-deposited and annealed device owing to electron capture by the interface traps or bulk traps. The $V_{th}$ shifts of 0.4V and 3.2V are obtained for as-deposited and annealed device respectively. For annealed device, electron capture process is not only restricted in the interface region but also extended into the crystalline Gd$_2$O$_3$ layer through Frenkel-Poole emission and hooping conduction, resulting in a larger $V_{th}$ shift. The calculated trap density for as-deposited and annealed device is $3.28 \times 10^{11} \sim 1.12 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ and $1.74 \times 10^{12} \sim 7.33 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ respectively in measured temperature range. These results indicate that elevated temperature measurement is necessary to characterize GaN/AlGaN heterostructure based devices with oxide as gate dielectric.

I. INTRODUCTION

GaN based material system has been intensively studied over the last few decades. GaN based semiconductor has distinct advantages, such as high electron mobility, high breakdown voltage, high frequency operation and high thermal and chemical stabilities. Owing to large spontaneous and piezoelectric polarization in GaN/AlGaN heterostructure, metal-semiconductor heterostructure field effect transistor (MESHFET) or high electron mobility transistor (HEMT) is widely studied for high power and high frequency applications. Conventional Schottky gate limits the device performance due to large gate leakage current. Consequently several approaches have been proposed to reduce gate leakage current and a variety of gate oxide in metal-oxide-semiconductor gate (MOS) structures have been reported.

Considering electron counting rule, it is relatively easy to define an ideal (100)Si-HfO$_2$ interface, because Si is non-polar and has a valence number of 4, like Hf. However, the (100) GaAs-HfO$_2$ interface is harder to define, because (1) GaAs is a polar molecule, and (2) Ga has 3 valence electrons while As has 5 valence electrons. Therefore it is useful to interpose a trivalent oxide matching layer on III-V’s to allow charge matching across the interface. This may be the reason why trivalent oxide like Gd$_2$O$_3$, Ga$_2$O$_3$, Sc$_2$O$_3$ or Al$_2$O$_3$ makes better interfaces with III-V’s. In addition, high dielectric Ga$_2$O$_3$ (Gd$_2$O$_3$) and pure Gd$_2$O$_3$ are thermodynamically stable with the III–V’s. GaAs and GaN based metal oxide field effect transistor (MOSFET) has been successfully demonstrated using Gd$_2$O$_3$ as gate dielectric while very few studies have focused on using Gd$_2$O$_3$ as gate dielectric in GaN/AlGaN heterostructure.
A standard high frequency C-V measurement is usually performed at room temperature (RT) to analyze the interface and oxide quality of MOS-HFET devices. Owing to complex device structure (two interfaces) and wide band gap nature of GaN/AlGaN, the above mentioned RT characterization may not be adequate to fully understand the interface behavior between AlGaN and insulator. Most of the deep interface states are frozen at RT which can only manifest at higher temperature. Thus, the C-V measurement in elevated temperature is useful to characterize the quality of oxide-AlGaN interface.

In this study, we demonstrate the temperature dependence of the threshold voltage ($V_{th}$) of GaN/AlGaN/Gd$_2$O$_3$/Ni-Au structure by means of capacitance-voltage measurement. Owing to the interface states between AlGaN and oxide, the $V_{th}$ variation is obvious at elevated temperatures. Therefore, thermal stability of oxide/AlGaN interface should be one of the criteria to determine the quality of MOS-HFET devices.

II. EXPERIMENT

The Al$_{0.27}$Ga$_{0.73}$N (25nm)/GaN (4μm) heterostructure was first grown on sapphire substrate by atmospheric pressure metal organic chemical vapor deposition (AP-MOCVD) system. The native oxide of exposed AlGaN surface was removed using dilute hydrochloric acid ($\text{HCl}:\text{H}_2\text{O} = 1:10$) for 90 sec. Then 20nm Gd$_2$O$_3$ film was deposited on AlGaN/GaN sample by e-beam evaporation from 99.99% pure Gd$_2$O$_3$ granules under $2 \times 10^{-6}$ Torr chamber pressure with a very low deposition rate of 0.2Å/s. After the oxide film deposition, a rapid thermal annealing (RTA) was performed at 850°C for 30s in air ambient. Then Ti/Al/Ti/Au metal stack was deposited by e-beam evaporation system followed by RTA at 700°C for 30s in N$_2$ ambient for ohmic contact formation. During RTA process of Gd$_2$O$_3$ film, Ti/Al/Ti/Au metal stack cannot be annealed owing to air annealing ambient which may cause oxidation of the metal stack. A lower annealing temperature of 700°C was chosen for ohmic contact formation. Higher annealing temperature ($\geq$750°C, N$_2$, 30s) degrades the interface (AlGaN/Gd$_2$O$_3$) which will cause “smearing out” the C-V curve. In this condition, the C-V curve exhibits no sharp transition from depletion to accumulation region. Finally Ni/Au top electrode (100μm diameter circular dot) was evaporated as gate contact. The crystal quality of GaN/AlGaN heterostructure was investigated by employing high resolution X-ray diffractometer (HR-XRD). To characterize the microstructure of GaN/AlGaN/Gd$_2$O$_3$ sample, high resolution transmission electron microscopy (HR-TEM) was performed using Philips Tecnai F20 FEG-TEM. The capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics of fabricated MOS structure were characterized by Agilent E4980A precision LCR meter.

III. RESULTS AND DISCUSSION

Figure 1 shows the schematic cross sectional image of GaN/AlGaN/Gd$_2$O$_3$/Ni-Au structure. By means of Hall measurement, the sheet electron concentration and mobility are about $1.15 \times 10^{13}$ cm$^{-2}$ and 1130 cm$^2$.V$^{-1}$.s$^{-1}$ respectively. Figure 2(a) shows the $(0 0 0 2)$ diffraction profile of GaN/AlGaN heterostructure. The main two peaks are assigned to be GaN $(0 0 0 2)$ and AlGaN $(0 0 0 2)$. Satellite peaks are also clearly observed in the XRD spectra. Figure 2(b) shows the cross-sectional HR-TEM image of GaN/AlGaN/Gd$_2$O$_3$ structure after annealing at 850°C for 30s. The HR-TEM image confirms that Gd$_2$O$_3$ has a good interface to AlGaN. The polycrystalline phase formation of Gd$_2$O$_3$ layer after high temperature annealing is also evident from the TEM image.

Three different kinds of devices were fabricated with similar process flow i.e. control (Schottky device without Gd$_2$O$_3$ layer), as-deposited (Gd$_2$O$_3$ layer without RTA) and annealed (Gd$_2$O$_3$ layer with RTA treatment). To investigate the effect of measurement temperature on $V_{th}$ of the fabricated devices, capacitance-voltage measurement was performed between room temperature (RT) and 150°C. The frequency and ac modulation voltage were kept at 1MHz and 25mV respectively. Figure 3 shows the C-V characteristics of control, as-deposited and annealed devices measured in bias range from $-10V$ to 0V. The RT $V_{th}$ of control device is found to be $-4.1V$ whereas $V_{th}$ of as-deposited and annealed device are found to be $-4.8V$ and $-8.2V$ respectively. The less negative $V_{th}$ for as-deposited device is attributed to negative fixed oxide charge in the Gd$_2$O$_3$ layer whereas
FIG. 1. Schematic cross-sectional image of GaN/AlGaN/Gd$_2$O$_3$/Ni-Au metal-oxide-semiconductor heterostructure.

more negative $V_{th}$ for annealed device is attributed to change of homogeneity of oxide layer and removal of negative charge by annealing.  

It is well known from the Si based MIS (i.e. Si/SiO$_2$) capacitor C-V analysis that the positive $V_{th}$ shift is attributed to electron trapping in the structure. A positive $V_{th}$ shift is observed for three kinds of devices in elevated temperature. Temperature induced Fermi level movement through built-in potential leads to an opposite shift of the $V_{th}$. Temperature dependent conduction band discontinuity and sheet carrier density in triangular quantum well (2-DEG) is negligible. The only possibility behind the positive $V_{th}$ shift in the fabricated structure in elevated temperature is electron capture by the interface states or Gd$_2$O$_3$ bulk traps.

Figure 4 shows the C-V characteristics of three kinds of devices with varying temperature from RT to 150$^\circ$C. For the control device [shown in Fig. 4(a)] the $V_{th}$ at RT of $-4.1$V is slightly shifted to $-3.9$V at 100$^\circ$C and remains almost constant up to 150$^\circ$C. The small positive $V_{th}$ shift is originated from the electron capture in the interfacial layer between AlGaN layer and gate metal. It was reported that a sub nanometer thick interfacial layer (AlO$_x$ and NiO$_x$) present between the Ni/Au gate metal stack and AlGaN epilayer. As the $V_{th}$ shift is minimum in the whole temperature range, the control devices shows good thermal stability at elevated temperature. In case of as-deposited device, RT C-V shows a small hysteresis window of 0.2V [shown in inset of Fig. 4(b)]. The hysteresis window is diminished in elevated temperature and $V_{th}$ is shifted from $-4.8$V at RT to $-4.4$V at 150$^\circ$C [Fig. 4(b)]. On the other hand, annealed device shows different trapping phenomena during thermal stress [Fig. 4(c)]. The parallel shift towards positive voltage direction of C-V curve is very prominent with increasing temperature. The resultant $V_{th}$ shift of around 3.2V is observed in the temperature up to 150$^\circ$C. For Si based MIS (i.e. Si/SiO$_2$) capacitor, it is well known that any “smearing out” in the experimental high frequency C-V curve indicates the presence of interface states and any parallel shift indicates the presence of fixed oxide charge. However, our measured C-V shows fixed oxide charge like behavior with increasing temperature. The C-V curve of the GaN/AlGaN heterostructure is mostly governed by 2-DEG at GaN/AlGaN interface. As the AlGaN/Gd$_2$O$_3$ interface is located far from the 2-DEG channel, any charge trapping by this interface states or bulk traps give rise to parallel shift of C-V curve. Therefore, large $V_{th}$ shift in elevated temperature is attributed to the electron capture by interface states as well as crystalline Gd$_2$O$_3$ bulk traps which is explained below. The two main ohmic conduction mechanisms in an insulator are Frenkel-Poole emission and
hooping conduction which are expressed, respectively, by\textsuperscript{17}

\begin{equation}
J \propto E_f \exp \left[ -\frac{q(\phi_B - 2\sqrt{E_f/C})}{kT} \right],
\end{equation}

\begin{equation}
J \propto E_f \exp \left( -\frac{\Delta E_{ac}}{kT} \right),
\end{equation}

where \( C \) is a material dependent constant, \( q \) is the electronic charge, \( \phi_B \) is the barrier height, \( E_f \) is the electric field, \( k \) is the Boltzmann constant, \( T \) is the temperature and \( \Delta E_{ac} \) is the activation energy of electron hopping. The two ohmic conductions are dependent on both electric field and temperature. So the electron capture process is not only restricted in the interface region, but is also extend into the Gd_2O_3 layer through above the mentioned mechanism during thermal stress.
FIG. 3. High frequency (1MHz) capacitance vs. gate voltage (C-V) characteristics of control, as-deposited and annealed devices at RT. A decrease in capacitance for as-deposited and annealed devices is due to the oxide capacitance. When compared with the as-deposited device, the observed small $V_{th}$ shift ($\sim 0.4V$) indicates lesser amount of interface states related to the electron trapping phenomena. In addition, the as-deposited amorphous Gd$_2$O$_3$ has fewer trapping nodes which results in lesser bulk trapping event.

The electron capture by the bulk traps in crystalline Gd$_2$O$_3$ film during thermal stress is verified through C-V measurement under positive gate bias stress at different temperatures. There is no noticeable hysteresis window observed under applied bias from $-10V \rightarrow 0V \rightarrow -10V$ for annealed devices when measured at RT [Fig. 5(a)], $100^\circ C$ [Fig. 5(b)] and $150^\circ C$ [Fig. 5(c)].

The device is stressed under different positive voltage pulse of $3V$ and $5V$ with fixed pulse duration of 100ms. The $V_{th}$ is then monitored by applying small sweeping voltage. A similar shift of $V_{th}$ (0.8V) is occurred under $5V@100ms$ stress at RT [Fig. 5(a)] and $100^\circ C$ [Fig. 5(b)] whereas small shift of $0.2V$ is observed at $150^\circ C$ [Fig. 5(c)]. The origin of $V_{th}$ shift under positive pulse in gate is owing to tunneling induced electron transport from two dimensional electron (2-DEG) gas to bulk traps.$^{18}$

The tunneling induced electron transfer effect in GaN/AlGaN/Gd$_2$O$_3$ (crystalline)/Ni-Au structure opens up a way to design GaN/AlGaN based memory device and have already been studied previously.$^{19}$ During positive gate voltage stress at RT and $100^\circ C$, the tunneling electron from 2-DEG are captured by bulk traps ($\Delta V_{th} = 0.8V$). However, in the case of thermal stress at $150^\circ C$, most of the bulk traps are previously occupied through ohmic conduction mechanism in insulator whereas very few ($\Delta V_{th} = 0.2V$) are available for tunneled 2-DEG electrons.

Some estimation of fast interface trap density has been made for both as-deposited and annealed device by single frequency approximation method proposed by W.A. Hill and C.C. Coleman.$^{20}$ The interface trap density $D_{it}$ is calculated from conductance-voltage (G-V) and capacitance-voltage (C-V) curves with the following expression

$$D_{it} = \frac{2qA}{f} \left( \frac{G_{m,max}/\omega}{C_{m}} \right)^2 + \left( 1 - \frac{C_m}{C_{ox}} \right)^2,$$

where $q$ is the electronic charge, $A$ is the area of the capacitor, $G_{m,max}$ is the peak value of conductance, $\omega = 2\pi f$, $f$ is the measurement frequency, $C_{ox}$ is the capacitance in accumulation region and $C_m$ is the capacitance corresponding to $G_{m,max}$. The RT C-V and G-V curves at 0.1MHz of annealed device are shown in Fig. 6(a) indicating the specifics of the input data employed for the calculation. In a similar way, the $D_{it}$ is extracted for as-deposited and annealed device and plotted as function of temperature over the whole temperature range [Fig. 6(b)]. The density of the fast trap decreased from $3.28 \times 10^{11}$ to $1.12 \times 10^{11}$ eV$^{-1}$cm$^{-2}$ for as-deposited device, and $1.74 \times 10^{12}$ eV$^{-1}$cm$^{-2}$ to
FIG. 4. High frequency (1MHz) capacitance vs. gate voltage (C-V) characteristics of (a) control, (b) as-deposited and (c) annealed devices with varying temperature from RT to 150°C. The inset is the capacitance vs. gate voltage (C-V) characteristic of as-deposited devices at RT.

$7.33 \times 10^{11} \text{eV}^{-1}\text{cm}^{-2}$ for the annealed device with an increase in temperature as the energy levels move deeper into the band gap. The trap density is also calculated from the concept of trapped electron density ($N_{\text{electron}}$) from the following expression

$$N_{\text{electron}} = \frac{\Delta V_{th} \times C_{ox}}{q A},$$  \hspace{1cm} (3)
FIG. 5. High frequency (1MHz) capacitance vs. gate voltage (C-V) characteristics of annealed devices with positive gate bias stress at (a) RT, (b) 100°C and (c) 150°C.

where $\Delta V_{th}$ is the resultant threshold voltage change, $C_{ox}$ is the capacitance in accumulation region, $q$ is the electronic charge and $A$ is the area of the capacitor. The trap density are found to be $3.58 \times 10^{11} \text{cm}^{-2}$ and $3.45 \times 10^{12} \text{cm}^{-2}$ for as-deposited and annealed device respectively which are higher, when compared to the calculated $D_{it}$ value owing to contribution of bulk traps. The trap density for the annealed device is around one order of magnitude higher than that of the as-deposited device. This is owing to crystallization annealing of Gd$_2$O$_3$ film. Higher trap density for Al$_2$O$_3$/AlGaN/GaN MOSHEFT was reported than that of HFETs owing to the gate oxide grown at higher (600°C) temperature. Therefore it is crucial to understand the properties of trap states for control and optimization of interface between insulator and GaN/AlGaN system.

IV. CONCLUSIONS

In conclusion, temperature dependent $V_{th}$ variation of GaN/AlGaN/Gd$_2$O$_3$/Ni-Au structure has been investigated through capacitance-voltage measurement. The electron capture by the interface states or bulk traps is responsible for the $V_{th}$ variation in three kinds of devices. In terms of $V_{th}$ variation in elevated temperature, as-deposited device shows a more thermal stability characteristic ($\Delta V_{th} = 0.4V$) as compared to annealed device ($\Delta V_{th} = 3.2V$). Single frequency approximation method reveals that $D_{it}$ is around one order of magnitude higher in annealed device ($1.74 \times 10^{12} \sim 7.33 \times 10^{11} \text{eV}^{-1}\text{cm}^{-2}$) than that of as-deposited device ($3.28 \times 10^{11} \sim 1.12 \times 10^{11} \text{eV}^{-1}\text{cm}^{-2}$). Our study demonstrates the importance of elevated temperature C-V measurement to characterize GaN/AlGaN
FIG. 6. (a) The RT capacitance vs. gate voltage (C-V) and conductance vs. gate voltage (G-V) characteristics of annealed devices indicating the specifics of the input data employed for the calculation of interface trap. (b) Density of fast traps as a function of ambient temperature for the Gd$_2$O$_3$/AlGaN/GaN structure.

heterostructure based devices with oxide as gate dielectric. It is suggested that the as-deposited oxide will be better for MIS-HEFT devices. On the other hand, high temperature annealed oxide will be useful to realize memory device in GaN/AlGaN system.

ACKNOWLEDGMENTS

The authors would like to thank Prof. Lee Chow of Department of Physics, University of Central Florida for his valuable comments and suggestions. This work was supported by the National Science Council (NSC), Taiwan, under contract no. NSC-99-2221-E-182-057.
1 M. A. Khan, J. N. Kuznia, D. T. Olson, W. J. Schaff, J. W. Burn, and M. S. Shur, Appl. Phys. Lett. 65, 1121 (1994).
2 S. N. Mohammad and H. Morkoc, Prog. Quantum Electron. 20, 361 (1996).
3 S. J. Pearton, C. Zolper, R. J. Shul, and F. Ren, J. Appl. Phys. Rev. 86, 1 (1999).
4 L. B. Chang, R. M. Lin, M. J. Lai, and C. H. Huang, Appl. Phys. Express 4, 012106 (2011).
5 S. C. Hung, Y. L. Wang, B. Hicks, S. J. Pearton, D. M. Dennis, F. Ren, J. W. Johnson, P. Rajagopal, J. C. Roberts, E. L. Piner, K. J. Linthicum, and G. C. Chi, Appl. Phys. Lett. 92, 193903 (2008).
6 M. A. Khan, X. Hu, A. Tarakji, G. Simin, J. Yang, R. Gaska, and M. S. Shur, Appl. Phys. Lett. 77, 1339 (2000).
7 S. Arulkumaran, T. Egawa, and H. Ishikawa, Jpn. J. Appl. Phys. 44, L812 (2005).
8 P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Hwang, Appl. Phys. Lett. 86, 063501 (2005).
9 P. W. Peacock and J. Robertson, Phys. Rev. Lett. 92, 057601 (2004).
10 M. Hong, J. Kwo, A. R. Kortan, J. P. Mannaerts, and A. M. Sergent, Science 283, 1897 (1999).
11 W. H. Chang, C. H. Lee, Y. C. Chang, P. Chang, M. L. Huang, Y. J. Lee, C. H. Hsu, J. M. Hong, C. C. Tsai, J. R. Kwo, and M. Hong, Adv. Mater. 21, 4970 (2009).
12 M. Miczek, C. Mizue, T. Hashizume, and B. Adamowicz, J. Appl. Phys. 103, 104510 (2008).
13 J. Chen, D. G. Ivey, J. Bardewell, Y. Liu, H. Tang, and J. B. Webb, J. Vac. Sci. Technol. A 20, 1004 (2002).
14 A. Das, S. Maikap, W. C. Li, L. B. Chang, and J. R. Yang, Jpn. J. Appl. Phys. 48, 05DF02 (2009).
15 M. R. Holzworth, N. G. Rudawski, S. J. Pearton, K. S. Jones, L. Lu, T. S. Kang, F. Ren, and J. W. Johnson, Appl. Phys. Lett. 98, 122103 (2011).
16 D. A. Neamen, Semiconductor Physics and Devices (McGraw-Hill, New York, 2003).
17 T. Hori, Gate Dielectrics and MOS ULSIs Principles, Technologies, and Applications (Springer, New York, 1997).
18 L. Z. Hao, J. Zhu, W. B. Luo, H. Z. Zeng, Y. R. Li, and Y. Zhang, Appl. Phys. Lett. 96, 32103 (2010).
19 L. B. Chang, A. Das, R. M. Lin, S. Maikap, M. J. Jeng, and S. T. Chou, Appl. Phys. Lett. 98, 222106 (2011).
20 W. A. Hill and C. C. Coleman, Solid-State Electron. 23, 987 (1979).
21 P. Kordoš, D. Donoval, M. Florovü, J. Kovář, and D. Gregušová, Appl. Phys. Lett. 92, 152113 (2008).