Omnivore: An Optimizer for Multi-device Deep Learning on CPUs and GPUs

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ABSTRACT

We perform a study of the factors affecting training time in multi-device deep learning systems. Given a specification of a convolutional neural network, we study how to minimize the time to train this model on a cluster of commodity CPUs and GPUs. Our first contribution focuses on the single-node setting, in which we show that by using standard batching and data-parallel techniques throughput can be improved by at least 5.5× over state-of-the-art systems when training on CPUs. This ensures an end-to-end training time directly proportional to the throughput of a device regardless of its underlying hardware, allowing each node in the cluster to be treated as a black box. Our second contribution is a theoretical and empirical study of the tradeoffs affecting end-to-end training time in a multiple-device setting. We identify the degree of asynchrony and statistical efficiency as key features affecting both hardware and statistical efficiency. We show that asynchrony can be leveraged as introducing a momentum parameter, which we use to limit our search space; in turn, this leads to a simpler optimizer, which is our third contribution. Our optimizer involves a predictive model for the total time to convergence and selects an allocation of resources to minimize that time. We demonstrate that the most popular distributed deep learning systems fall within our tradeoff space but do not optimize within the space. By doing such optimization, our prototype runs 1.9× to 12× faster than the fastest state-of-the-art systems.

1. INTRODUCTION

Deep learning has emerged as a powerful technique in machine learning, providing astonishing improvements in quality for a number of data-driven applications. An important aspect of deep learning is that quality improves with the amount of data, and so advances in system efficiency and scalability directly improve quality. This observation has led to an arms race of distributed deep learning systems both in industry (e.g., Google’s DistBelief, Microsoft’s Adam) and in academia. In spite of this proliferation of deep learning systems, there have been few studies of deep learning from a data-systems perspective. Each of these systems makes a set of design decisions, although these design decisions may not work for other tasks or hardware settings. To address this concern, we perform a first study of the design space for deep learning systems. Moreover, systems that do implement a number of design choices provide no way of automatically selecting an optimal configuration, placing this burden on the user. In our experience working with multiple PhD-level users of these systems—including experts in pathology, radiology, computer vision, and the energy sector—it is often very difficult even for advanced users to make these design decisions themselves. It is not uncommon for a suboptimal design choice to result in a runtime that is an order of magnitude slower end-to-end than what is possible. By exploiting our understanding of the tradeoff space and new theoretical insights on asynchrony, we develop a simple optimizer that enables our own prototype system to be 1.9× to 12× faster than the fastest competitor systems.

We focus on perhaps the most popular deep learning models, Convolutional Neural Networks (CNNs), which are state-of-the-art for a wide range of applications (e.g., image processing, video analysis, drug discovery) and which contain many of the fundamental layers used in other deep learning models. Our study answers the question: “Given a cluster (e.g., X machines, Y GPUs, Z CPUs, etc.), how do I train my CNN as quickly as possible?”. Answers to this question have obvious implications for performance as well as total cost of ownership and end-user cost in the cloud.

We assume that the following are given: (i) a deep learning model (network architecture), (ii) a dataset for training this model, and (iii) a set of computational resources (a number of devices on machines, their throughput, and the network speed). We then study how to minimize the total training time. We build a complete prototype capable of training the most popular deep learning models. This allows us to hone in on two major choices: (i) how to use hardware on each node and (ii) the degree to which asynchrony can be tolerated. Our work demystifies these factors by identifying the key tradeoffs that underlie all design decisions, providing theoretical guidance about asynchrony, and quantifying the impact of those tradeoffs experimentally.

In this paper, we study how to train a single convolutional neural network (CNN) on a cluster of commodity CPUs with the constraint that all nodes in the cluster are housed on the same rack. The machines are connected by a uniform and fast topology, e.g., if they were housed on the same rack.
Overview of Technical Contributions

To conduct our study, we develop a prototype distributed system called Omnivore as it scales to consume all available hardware resources. We make three contributions.

Contribution 1: Single-Device Optimizations. In Section 2, we demonstrate that we can achieve throughput proportional to the FLOPS of both CPUs and GPUs. This statement is not trivial—there has been a long debate about CPUs vs GPUs for deep learning: GPUs are popular for CNN systems because of the high throughput they provide, but they contain smaller off-chip memories than CPUs. Microsoft’s Project Adam argues that CPUs can deliver more cost-effective performance [7]. For users who cannot control their data-center hardware, another issue is that Amazon’s EC2 provides GPUs but Google Compute does not. Also, Amazon provides more aggregate available FLOPS if one selects CPU clusters. We observe that while state-of-the-art systems achieve GPU speeds proportional to the device throughput, existing CPU implementations can be sped up significantly compared to what is reported in the literature.

Our study explores two key optimizations that we first reported last year [19]. We use batching and data-parallel optimizations—not employed in other systems—to achieve end-to-end speedups of more than 5.5× over state-of-the-art systems on commodity CPUs. Such optimizations are not always possible on the GPU, but by selecting this strategy for the CPU, we now achieve speeds proportional to the peak throughput. This allows us to build a radically simpler optimizer by modeling CPUs and GPUs as black boxes.

Contribution 2: Multi-device Tradeoffs. In Section 3, we describe our second contribution, an empirical study of the factors affecting training time for multi-device deep learning training. We analyze the decisions made on existing systems and conclude that, while diverse, the strategies of the most popular systems fall within a tradeoff space defined by two fundamental dimensions [5, 7, 8, 15, 19, 25]: (i) the server architecture, or how the layers of a CNN map to devices; and (ii) the execution strategy, or how batches of data are mapped to machines for processing. We develop a simple framework that allows us to model each of these approaches. Devices are organized in compute groups. Each compute group is responsible for a single batch of data per iteration. Inside a group, the CNN computation for that batch occurs in standard, synchronous steps. Across groups, however, computation happens asynchronously. This leads to the use of stale model parameters.

This setting lets us hone in on a key aspect in deep learning: asynchrony during training. Asynchronous approaches are widely used in industry as they make better use of the hardware by forgoing any locking [7, 20]. The question is: how does one divide up available resources? Because deep learning models are often trained iteratively, we decouple the problem into two portions: (i) hardware efficiency (HE), the time per training iteration; and (ii) statistical efficiency (SE), the number of iterations required for training to converge. From these definitions, SE × HE = total training time, which we want to minimize.

Contribution 3: Simple Automatic Optimizer. In Section 4, based on the theory above, the intuition behind our optimizer is very simple: pick the highest degree of asynchrony such that the implicit momentum induced by asynchrony is below the optimal momentum. Given a fixed number of compute groups (asynchrony), we grid-search the parameters for learning rate and momentum. If the best-found momentum is non-zero, the optimizer chooses this configuration. If it is zero, we assume that there could be a better setting with fewer compute groups. Our optimizer is able to choose a near-optimal point in the tradeoff space and we demonstrate that our system achieves end-to-end speedups of 1.9× to 12× on popular CNN workloads compared to state-of-the-art tools that choose suboptimal tradeoff points. To leverage the above tradeoff, we show that it suffices to measure the statistical and hardware efficiency for minutes (less than 10% of the time to train a network). We compare our simple optimizer with a state-of-the-art Bayesian optimization approach [22]. Both approaches are able to reach the same final accuracy (within 1%), but the Bayesian strategy takes almost 6× as long.

Finally, we demonstrate that our optimizer is generic, and we apply it to other deep learning systems. In some cases this prevents those other tools from diverging, and in other cases the optimizer speeds them up by a factor of 7×.

Outline. We present background in Section 2. Section 3 and Section 4 introduce the tradeoff space related to single-machine and multi-device settings, respectively. Section 5 describes the optimizer for making decisions in this tradeoff space. We validate our results in Section 6, discuss related work in Section 7, and conclude in Section 8.
2. BACKGROUND

2.1 Convolutional Neural Networks (CNNs)

A convolutional neural network (CNN, [17]) consists of layers $L_1, L_2, \ldots, L_P$. Each layer is an operator which takes as input a 3D data tensor $D \in \mathbb{R}^{n \times n \times d_{in}}$ and transforms it to a resulting 3D data tensor $R \in \mathbb{R}^{m \times m \times d_{out}}$, i.e. $f^{FW}_{p}(D_p) = R_p$. $FW$ indicates the layer running in the “forward” direction to transform $D$ into $R$. Layers have a second operation, backward or $BW$, described later. As a running example, let the input $D_1$ to the first CNN layer $L_1$ be an image $I \in \mathbb{R}^{224 \times 224}$, where 3 represents the RGB color channels.

For layers after $L_1$ (the input layer), the input tensor $D_p$ comes from the output of a prior layer (usually $D_p = R_{p-1}$), such that the CNN layers are cascaded to define a composite operation (boldface highlights inputs and outputs)

$$R_P = L_{P}^{FW} \circ L_{P-1}^{FW} \circ \ldots \circ L_{2}^{FW} \circ L_{1}^{FW} \quad (2)$$

The final result $R_P$ is the CNN’s prediction for image, $I$. For example, if the task is image classification with 1000 categories, the tensor $R_P \in \mathbb{R}^{1 \times 1 \times 1000}$ is a vector containing the probability of each category. This prediction is then compared to $C$, the true classification for $I$, using a loss function $\ell(R_P, C)$ that evaluates the quality of the prediction. A lower loss indicates a better prediction.

Many types of layers exist in a CNN. Some layers perform a pre-defined transformation such as downsampling while other layers contain a model, $W$, and perform an operation parameterized by the model. Models are also known as weights or parameters. The models of all layers constitute the entire set of weights or parameters of the CNN, i.e. $W = W_N = \{W_{L_1}, \ldots, W_{L_P}\}$—although recall some layers have no model parameters.

2.2 Stochastic Gradient Descent

The goal of CNN training is to optimize the model $W$ in order to minimize the loss function $\ell(R_P, C)$, also denoted as $\ell(W, I, C)$ to make the fact that $R_P$ is a function of $W$ and $I$ explicit. Low loss is correlated with high prediction accuracy and in this work we refer to both. The most popular training algorithm for CNNs is an iterative technique called stochastic gradient descent (SGD). Each SGD iteration consists of a forward and backward pass. The input to each SGD iteration is an image-label tuple $(I, C)$ as described above. The forward pass calculates the prediction $R_P$ of $I$ using equation (2), and then the prediction error compared to $C$ is used to calculate the gradient (or derivative) of $\ell$ with respect to $R_P$. We denote this gradient as $\nabla_{R_P, \ell}$. Now the cascade of equation (2) runs in reverse by applying each layer in the “backward” direction:

$$L_{1P}^{BW} \circ L_{2P}^{BW} \circ \ldots \circ L_{P-1}^{BW} \circ L_{P}^{BW} (\nabla_{R_P, \ell}) \quad (3)$$

equation (3) implements the chain rule of calculus. The $BW$ operation of layer $p$ takes as input a data gradient $\nabla_{R_P, \ell}$ and outputs a data gradient $\nabla_{W_p, \ell}$. Internally, it also updates that layer’s model $W_{L_p}$ by (i) calculating a gradient of the loss with respect to the model, $\nabla_{W_p, \ell}$, and (ii) using an SGD update on the model. The SGD algorithm repeats iteratively for many iterations, often in the millions, until the loss is sufficiently low, i.e. the model is sufficiently optimized. The initial model $W^{(0)}$ is randomly initialized. The SGD update at step $t$ takes the form

$$W^{(t)} \leftarrow W^{(t-1)} + V^{(t)}, \quad (4)$$

where the new step, $V^{(t)}$, consists of a scaled version of the previous step, $V^{(t-1)}$, plus a gradient calculated on the new tuple $(I, C)$.

$$V^{(t)} \leftarrow \mu V^{(t-1)} - \eta \left[ \nabla_W \ell \left( W^{(t-1)}, I, C \right) + \lambda W^{(t-1)} \right] \quad (5)$$

In Section 4 we introduce the notion of asynchronous updates. The main change in equation (5) under asynchrony, is the use of an older model, $W^{(s)}$, when evaluating the gradient $\nabla_{W, \ell}$. This gradient (specifically, its negative) is the direction to “step” within the parameter space each SGD iteration. The learning rate, $\eta$, is the scale factor applied to the magnitude of this gradient, i.e. the size of the step. $\lambda$ dictates the amount of regularization, which is an input to the training problem (part of the CNN model to train). $\mu$ is the amount of explicit momentum we add to the update. Momentum is used to “accelerate” learning in the directions common to each gradient by keeping a history of past gradients and adding this history to the gradient of the current step, with past gradients decayed exponentially. Commonly, in order to produce more stable gradients, each SGD iteration does not process a single tuple $(I, C)$, but a batch of $b$ tuples, e.g. 256, in which case $D$ and $R$ become 4D. The gradients from each tuple are summed to produce a single, combined gradient for that iteration.

Selecting the right values for hyper-parameters $(\eta, \mu, b)$ is critical for performance. We will describe a simple optimizer to pick these parameters.

2.3 CNN Computation

Of all the CNN layers, two model layers are the most computationally intensive, convolutional (conv) and fully-connected (FC) layers. A convolutional layer performs many independent convolutions over an image, i.e., several sliding-window operations; in contrast, an FC layer performs a dense matrix multiplication. In many popular implementations, the bottleneck in both layers is a matrix multiply implemented as a call to either a BLAS or cuBLAS library. For our study, their data properties are more important, and we refer to Chetlur et al. [8] for a more detailed description of their use in machine learning.

As shown in Figure 1 in state-of-the-art models, all convolutional layers always appear before all fully-connected layers. Therefore, in this work we introduce an abstraction
which separates a CNN into two phases, each consisting of a number of consecutive layers: first the convolution phase (conv), whose layers have large data tensors \(D\) and \(R\) (e.g., 100MB-1GB) and small models \(W\) (e.g., 5-50 MB), followed by the fully-connected phase (FC), whose layers have small \(D\) and \(R\) (e.g., 1-10MB) and large \(W\) (e.g., 30-300 MB). The reduction in data size is in part due to pooling layers in the convolution phase which perform down-sampling. The increase in model size is due to the fact that convolution layers repeat the same weights for the sliding window. Note that our two-phase categorization also applies to modern, non-linear CNNs [14]. See Appendix B.1 for a full description of CNN trends.

The computation for both the conv and FC phases is usually compute-bound although the conv phase contains significantly more computation (e.g., in AlexNet conv is 1.6 TFLOPs and FC is 80 GFLOPs, or 95% of the computation is convolution). Within a machine, each layer’s computation can be mapped to CPUs, GPUs or a combination of both. In addition, this computation can be parallelized either using data parallelism (partitioning the data batch and replicating the model, which works well for the conv layers) or model parallelism (partitioning the model and replicating the data batch, which works well for the FC layers). These single-machine choices are studied in Section 3.

Section 4 studies these same choices but in the distributed setting. There the layer computations are mapped across machines, although as we will show this mapping is always done at the coarser granularity of entire phases (conv or FC) because it reduces network delays due to the distinct model and data sizes of the two phases. In addition, Section 4 studies techniques to parallelize the iterative (seemingly sequential) SGD algorithm in a distributed setting.

2.4 Problem Definition

We study systems tradeoffs to build an optimizer for the most widely used networks/algorithms. We focus on SGD due to its popularity, although our optimizer applies to other algorithms as well. More precisely, we are given as input the following: (i) a CNN architecture \(\{L_1, ..., L_p\}\), including regularization, (ii) a dataset \(D\) consisting of data batches, (iii) a device graph \(G\) in which vertices are hardware devices (specified by their throughput) and edges are communication speeds between devices. Our goal is to design an optimizer which creates a plan for the execution strategy in order to train as quickly as possible.

A plan for physical mapping maps the computation (both FW and BW) of each layer of the CNN to vertices (e.g., GPUs or CPU cores) of the device graph. Section 3 first studies how to do this mapping across devices in order to parallelize SGD in the multi-device case. The key decision here is the degree of asynchrony in execution. This is further described in Section 3.

3. SINGLE-DEVICE TRADEOFF

The first step towards building a distributed optimizer is understanding the systems tradeoffs within a single device. We show that for each device (GPU or CPU) we can achieve throughput that is proportional to its peak FLOPS. This will enable the distributed optimizer to treat each device as a black box in Section 4. This is not a trivial property for deep learning: many CNN systems exist [1,2,10] which use either CPUs or GPUs, but these always report that GPU implementations are an order of magnitude faster than CPU. This is true even when the devices offer similar FLOPS. Therefore the challenge is to utilize the FLOPS on the CPU. We study the key kernel in CNN implementations, which is compute bound. We introduce a data batching technique which trades off memory footprint for compute time and demonstrate that this tradeoff gives a more than 5× CPU speedup over existing systems. With this optimization now both CPUs and GPUs give throughput proportional to the FLOPS offered by the device.

3.1 Convolutional Layer Computation

As reported in the literature and confirmed by our experiments, the most computationally intensive layers in the CNN are the convolutional layers. Together, all convolutional layers in a CNN often consume between 70-90% of total execution time. Recall that a convolutional layer contains a model, which we will also call its kernel and denote as \(K\). A convolutional layer accepts as input a 4D data tensor \(D \in \mathbb{R}^{n \times n \times d_{in} \times b}\), where recall \(b\) is the batch size. \(K\) is also a 4D tensor, \(K \in \mathbb{R}^{k \times k \times d_{in} \times d_{out}}\). The output is a 4D data tensor \(R \in \mathbb{R}^{n \times n \times d_{out} \times b}\), where:

\[
R_{x,y,z,w} = \sum_{k'=0}^{d_{in}-1} \sum_{x'=0}^{k-1} \sum_{y'=0}^{k-1} D_{x-x',y-y',z,w} K_{x',y',d',z}
\]

Like most HPC kernels a straightforward implementation is suboptimal, and many optimized implementations of this convolution kernel exist [3,16,24]. A popular implementation is to perform equation (6) as a dense matrix multiplication (also known as GEMM, general matrix multiply),
| Device Type (EC2 Instance) | Device Type (GPU Grid K520) | Device Type (Dual-GPU Grid K520) |
|---------------------------|----------------------------|---------------------------------|
| 1x CPU Xeon E5-2666 (c4.4xl) | 1,670 8% 40% 71% (c4.xlarge) | 1,229 53% 54% 99% (g2.2xlarge) |
| 2x CPU Xeon E5-2666 (c4.8xlarge) | 1,670 8% 40% 71% (c4.xlarge) | 1,229 53% 54% 99% (g2.2xlarge) |
| Dual-GPU Grid K520 (g2.8xlarge) | 2,458 26% 52% 99% | 2,458 26% 52% 99% |

Figure 3: Across several CPUs and GPUs we obtain throughput on convolution layers that is \( \sim 50\% \) of the device peak (shown for AlexNet, total \( FW + BW \) time for all conv layers). We also show large GEMM as a reference of what the device can achieve.

Figure 4: The impact of batch size (\( b_p \)) and number of threads on the GEMM kernel (total batch size \( b = 256, 8 \) physical cores). Shown for the GEMM in the largest convolutional layer of AlexNet.

### 3.2 Batching and Data Parallelism

The design tradeoff between CPUs and GPUs arises as a result of this increase in data size. Assume that we are given a fixed batch size of \( b \) images (e.g., \( b = 256 \), discussion on selecting \( b \) in Appendix E.1). GPUs cannot fit an entire batch of lowered data into off-chip memory, therefore many CNN implementations on GPUs perform lowering/GEMM serially on one or few images at a time until all \( b \) have been processed. On the CPU however, off-chip memory is larger which allows lowering/GEMM to be performed on all \( b \) images at once. This leads to significant CPU speedups compared with state-of-the-art tools which do not explore this data parallelism.

Generalizing this implementation tradeoff, \( b_p \) images can be processed in parallel by the convolution layer, where \( 1 \leq b_p \leq b \). Increasing \( b_p \) increases the memory footprint but decreases the overall execution time. Figure 4 shows batching experiments for a CPU GEMM kernel (the GPU is discussed in Appendix C.2). All points in each graph perform GEMM on 256 images (i.e., \( b = 256 \)), but the number of total GEMM calls depends on \( b_p \) (e.g., if \( b_p = 256 \), there is one large GEMM). We therefore advocate the strategy of selecting \( b_p \) as large as possible (up to \( b \)) such that \( D \) fits into the off-chip memory. This can be predicted because memory usage increases linearly with \( b_p \) as seen in Figure 4(c). For a range of modern CPUs that we used in our experiments, the optimal \( b_p \) value is always \( b \).

While this tradeoff is simple, it enables FLOPS proportional scheduling which allows us to abstract away the details of devices in our distributed implementation.

### 4. MULTI-DEVICE TRADEOFF

Having studied the tradeoffs for a single device, this section now studies the distributed setting. Given a CNN, an input set of data and a set of devices, our goal is to map each layer of the CNN and a subset of data to each device. While many diverse distributed CNN systems exist, we explain in Appendix D.3 that these can be mapped to points within our tradeoff space.

Our exploration revealed that a key tradeoff is the degree of asynchrony. Following the HE, SE decomposition in equation (1), we build models predicting how hardware efficiency (Section 4.1) and statistical efficiency (Section 4.2) are affected by asynchronous execution. As we will see HE and SE are in opposition, but by decoupling them and creating a separate model for each the optimizer can find a balance and minimize the total time to convergence. Specifically, we argue for an analytic model for HE and we are able to give a new theoretical characterization of SE.

We separate each layer into compute servers, responsible for computation, and a model server responsible for handling reads from and writes to the model. These “servers” are virtual: many servers may be mapped to the same device or an individual server may be mapped to several devices. While
Asynchrony and Staleness. In most systems, compute groups communicate *asynchronously*\(^\text{[7, 8, 20]}\)\(^{3}\) the models are updated without locking or barriers, and so forward and backward passes may be computed with a stale model. Intuitively, the lack of coordination allows one to make better use of the hardware (better hardware efficiency) but the use of stale information may reduce statistical efficiency. If there are \(g = S + 1\) compute groups, we call \(S\) the staleness parameter. This is justified as the computation within each group in step (ii) above is very regular for CNNs (standard deviation of runtime is less than 6\% of mean), hence these groups execute in a nearly round-robin fashion.

Throughout this section, we make two simplifying assumptions: First, we focus our description on the two phases described in Section 2, i.e., we abstract networks into convolutional layers (conv) which have a large amount of data but a small model, and fully-connected layers (FC) which have small data but a large model. Practically, these two layers are the main bottlenecks in current networks. Their differing characteristics give rise to different points of the tradeoff space. Second, many popular networks are simply a single chain, not a DAG (e.g. AlexNet), and DAGs can be serialized into a chain, hence we view the input as a list of layers (without loss of generality).

**Execution.** Given a list of layers, the main computational loop is to move through the list forward calling the forward operation and in reverse order calling the backward operation at each step. As we have decomposed each layer into a model server and compute servers and further mapped compute servers to compute groups over several devices, it is the responsibility of our execution engine to make sure that all data is on each device when needed. We use standard techniques to hide latency of device copies, e.g., double buffering.

### 4.1 Hardware Efficiency Model

The goal of this section is to create a predictive model \(HE(S)\) for hardware efficiency, specifically how \(HE\) is affected by the amount of staleness \(S\) in the system (or equivalently the number of compute groups, \(g\)). We derive a simple analytic model which reasons about the bottlenecks.

An *execution strategy* partitions the \(N\) conv devices into \(g\) compute groups. Again for concreteness, assume there are \(k\) devices per group \((k = N/g)\). Let \(t_{\text{conv}}(k)\) be a function that returns the time that a group of size \(k\) needs to compute the convolution phase. We make the assumption that FC only operates sequentially\(^{4}\). Note that the number of requests to the FC phase is a function of the number of groups, and let \(t_{\text{fc}}\) be the time that the FC phase needs to serve one group.

Given \(g, t_{\text{conv}}(k)\) and \(t_{\text{fc}}\), our goal is to create a hardware efficiency model which predicts the time per iteration. There are two cases depending on which phase is the bottleneck:

- **Case 1: Saturated FC** The first case is when FC phase is saturated, i.e., it starts to serve the next request immediately after the previous request finishes. In this case,

  \[
  \text{Time per iteration}_{\text{saturated fc}} = t_{\text{fc}}
  \]

- **Case 2: Saturated Conv** When the FC phase is not saturated, each conv group becomes the bottleneck. In this case (the proof is in the Appendix D.4),

  \[
  \text{Time per iteration}_{\text{saturated conv}} = (t_{\text{conv}}(k) + t_{\text{fc}})/g
  \]

which is the total time for a single iteration divided by the number of parallel groups.

Thus, our predicted model for iteration time, \(HE(g)\), is:

\[
HE(g) = \max\{t_{\text{fc}}, (t_{\text{conv}}(k) + t_{\text{fc}})/g\}
\]

Given \(t_{\text{conv}}(k), t_{\text{fc}}\) and the number of groups, \(g\), the model can now predict what the mode of saturation will be and therefore the time per iteration. In Appendix D.4, we show that this works across a range of datasets.

**Obtaining the Parameters.** The parameters above can be measured with high accuracy and low variance. \(t_{\text{fc}}\) can be measured by running an iteration on a single device, but \(t_{\text{conv}}(k)\), though still directly measurable, requires measurements for each \(k\). Instead, \(t_{\text{conv}}(k)\) can be calculated from (i) the throughput of each node; (ii) the network speed; and (iii) a measurement of \(t_{\text{conv}}(1)\) (which only needs to be measured for a single \(k, k = 1\), and on a single device).

We present this calculation in Appendix D.4, and Figure 5 (b) shows that given only (i) to (iii) above, the end-to-end

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3 For simplicity, assume different groups (batches) cannot be executed in parallel on the FC server (we handle this in Appendix D.4).

4 Note that the number of requests to the FC phase is a function of the number of groups, and let \(t_{\text{fc}}\) be the time that the FC phase needs to serve one group.
4.2 Statistical Efficiency Model

Our goal is to characterize the effect of staleness on statistical efficiency. During our study, we discovered a theoretical characterization of this phenomenon, which was surprising to us as deep learning problems are seemingly impenetrable to theory. We demonstrate that staleness can be regarded as a synchronous update—but with a stronger momentum term. We state a simplified version of this result that is sufficient to understand our optimizer, and describe a more detailed version in a companion theoretical paper [18]. More importantly, we validate the predictions of this model on a range of deep learning models. In turn, this will form the basis of our optimizer.

We make the following modeling assumptions, which are not necessary but help us capture the essence of the result and form the basis of our optimizer. The full model, detailed assumptions and proofs can be found in [18]. We make the three following simplifying assumptions.

(A0) The batch to be used for each step is drawn uniformly at random with replacement. This is a standard assumption of SGD.

(A1) Variations in the time it takes to process a step are due to unmodeled system behavior. Importantly, variations are independent of the specific batch drawn. This is justified by the fact that, for all batches, all computation involves dense operations.

(A2) The time it takes to process a step is exponentially distributed and independent from other steps. This is a simplifying but standard assumption from queuing theory [12]. A more general (and complex) version of Theorem 1 below holds without this assumption.

**Theorem 1.** Consider $g$ asynchronous groups and set explicit momentum to zero, i.e. $\mu = 0$ in the update of equation (5). Under the above assumptions, the expected update becomes

$$E V^{(t+1)} = \left(1 - \frac{1}{g}\right) E V^{(t)} - \frac{g}{E} W \ell(W^{(t)}). \quad (7)$$

In which $\ell(W)$ denotes the expectation of $\ell(W,I,C)$ over the random draw of possible batches $(I,C)$.

In plain English, asynchrony increases momentum – there is implicit momentum of $1 - 1/g$. This simple version is interpretable in that it exactly matches the standard form of momentum used by deep learning practitioners in equation (5). Moreover, it successfully predicts measured system behavior. Figure 4 shows the predicted and actual measured momentum for two datasets: Theory suggests that, as long as the asynchrony-induced implicit momentum is less than the optimal total momentum, we can algorithmically compensate with explicit momentum. When however, implicit momentum exceeds the optimal total momentum, we start incurring statistical inefficiency. We use this intuition as the basis for our optimizer in Section 5.

Figure 6: Predicted and measured momentum moduli: (Left) Predicted, Theorem 1 (Middle) Measured, CIFAR (Right) Measured, ImageNet

**Cold-start.** We observe a phenomenon similar to burn-in [21] in Gibbs samplers. The model needs a few iterations to set the appropriate scale of the model parameters. On ImageNet-1000, we find that 5 passes over the dataset (< 15% of total execution) suffice to “warm up” the model. As a result, the optimizer starts by running synchronously and then switches to asynchronous (see Section 5).

5. DISTRIBUTED OPTIMIZER

This section uses the models and tradeoff space characterization of the previous two sections to create (i) a plan for physical mapping which maps each server to a machine, and (ii) a plan for the execution strategy which defines the number of compute groups by allocating data batches to each server. As in previous sections we assume a fixed number of machines. We first discuss the process of physical mapping and then describe our optimizer. We conclude with theoretical and empirical justification for the optimizer, and in Section 5.3 compare it to state-of-the-art, Bayesian approaches.

5.1 Physical Mapping

We observe that in all CNNs the architecture of Figure 5 (a) works best, and describe other physical maps and the search space in Appendix D.4. Omnivore maps the FC compute and model servers to the same machine, an approach we call merged FC. Merging the FC compute and model servers to the same device was shown in [7] to reduce communication overhead in a CPU cluster (improving HE), however it was not known that (1) this also benefits HE for a GPU cluster, and (2) this technique also benefits SE by eliminating staleness in the FC model. These are both observations we make. The remaining machines are used for the conv compute servers. The conv model servers are mapped to one of the conv compute machines. These optimizations are critical: on a cluster of 33 EC2 c4.4xlarge machines, not merging the FC servers incurs an additional hardware efficiency penalty of 1.2× due to increased communication as well as a statistical efficiency penalty of 2.5× because of staleness in the FC model. The key tradeoff is therefore the number of conv compute groups, which we describe next.

5.2 Optimizer

Multiple factors impact the performance of the training procedure: (1) the number of compute groups; (2) the momentum; and (3) the learning rate. As we illustrated in Section 4.2 all these three are interdependent. Moreover, the optimal setting of these parameters might change during training, so our optimizer runs periodically in epochs (e.g., every hour). Algorithm 1 shows the end-to-end optimizer that runs after the initial cold-start period (described in more detail in Appendix E.4).
Algorithm 1 Automatic Optimizer for the Tradeoff

Input: Time budget $T$ and possible choices of (1) # compute groups $CG$, (2) momentum $M$, and (3) learning rate $H$.
Output: Trained model $W$.

1: $g = CG$
2: while not reaching the termination criteria do
3:   $(\mu, \eta) \leftarrow \text{gridSearch}(M, H(W, g))$
4:   while $g = 0$ or $g > 1$ do
5:     $g \leftarrow g/2$
6:   $(\mu, \eta) \leftarrow \text{gridSearch}(M, H(W, g))$
7:   end while
8:   $W \leftarrow \text{train}(g, \mu, \eta, W)$ for $T$ minutes
9: end while
10: return $W$.

Figure 7: Hardware efficiency, statistical efficiency, and total time for various execution strategies.

In each of the epochs, the key issue is to set the number of compute groups, $g$. We perform a grid search over both the learning rate and the momentum starting at a particular value of $g$. This search determines the optimal explicit momentum for that $g$ by selecting the configuration with the lowest final loss. The key intuition is: set the highest amount of asynchrony, $g$, such that this explicit momentum is non-zero. The reasoning is that, when the optimal explicit momentum is 0, the implicit momentum is likely higher than the optimal value, and a cause of statistical inefficiency (c.f. Figure 6). In this case, we reduce the amount of asynchrony by reducing $g$. We provide an initial value for $g$ by leveraging the HE model of Section 4.1. In particular, we start with the smallest number of compute groups that saturate the FC server. This can be determined analytically or through measurements during the cold start phase. Having selected a $(g, \eta, \mu)$, we run for the rest of the epoch, which is an hour. At the end of the hour, the epoch ends, the model is checkpointed (written to disk), and the optimizer repeats.

Importance of Compute Groups. We demonstrate that using the right number of compute groups has an impact on performance. Fixing the total number of machines, we try different numbers of compute groups on CPU-L (Figure 9) for the Imagenet 1000-class dataset, and AlexNet CNN. We grid-search a number of values for the learning rate and momentum and report the best result achieved in each case (details in Appendix E.3). Figure 5 reports (a) the time per iteration (hardware efficiency, HE), (b) the number of iterations to reach a specific training loss (statistical efficiency, SE), and (c) their product, which by equation 1 is the total time required to reach the final loss. Note that the HE curve in (a) is the same as in Figure 5(b).

We see in Figure 7 (c) that $g = 32$ (fully asynchronous) is $3.7 \times$ faster than $g = 1$ (synchronous) as measured by wall-clock time to final loss. This is due to its $6.7 \times$ faster iteration time (HE) in (a), although it requires $1.8 \times$ more iterations (SE) as shown in (b). This matches the theory’s prediction: increasing $g$ causes the optimal explicit momentum, $\mu^*$, to decrease. We see that $\mu^*$ drops to 0 at $g = 32$, and consequently there is a penalty in SE. Running the optimizer of Algorithm 1 selects $g = 4$, which is near-optimal: $5.3 \times$ faster than sync and $1.4 \times$ faster than async. We repeat the same experiment for CIFAR and report similar wall-clock time plots in Appendix F.3. We see that in all cases, the optimal number of groups is more than 2x faster compared to sync, and that Algorithm 1 always picks a near-optimal point strictly better than sync.

6. EXPERIMENTS

We evaluate the runtime performance of our system, and we observe that Omnivore outperforms state-of-the-art tools by 1.9x to 12x on a range of training tasks. Our result holds (i) across a diverse range of hardware, including both CPUs and GPUs, (ii) in both single device and multiple device/machine settings. Importantly, Omnivore does not require users to pick hyperparameter values. The tradeoff analysis presented in Section 4 leads to the automatic optimizer of Section 3 which takes care of those choices. Our experiments validate that our optimizer produces better results compared to hand-tuned schedules and is up to 6x faster compared to state-of-the-art Bayesian optimizers.

6.1 Experiment Setup

We begin by describing the datasets, models and tasks as well as the hardware we run on.

Datasets and Models. We validate the performance of Omnivore on a diverse range of datasets and models, as shown in Figure 6. The largest corpus we use is ImageNet, which contains 1.3M images. ImageNet is the de facto benchmark for deep learning systems. Training a model on ImageNet can take tens of hours even on the latest 7 TFLOPS Titan X GPU. NVIDIA reports that it took three days to train with a single GPU. For some of our experiments, which require running many configurations to convergence, we used a reduced version, ImageNet8, containing the first 8 classes. We train the standard CaffeNet on both data sets. We also use smaller, but standard, datasets CIFAR and MNIST, which are for object recognition and handwriting recognition, respectively. We train the standard networks in Caffe’s tutorials for both.

Metrics. Our main metric of performance is the wall-clock time required to achieve a given training accuracy. As in Section 5, we measure the statistical efficiency, which is the number of iterations needed to achieve a given training accuracy.

Competitor Systems and Experiment Settings. We compare Omnivore against a range of existing tools using both a single-machine and multiple machines. Single machine: we compare Omnivore to Caffe and Google’s TensorFlow, the two most popular CNN systems, using Caffe’s

https://github.com/BVLC/caffe/tree/master/models/bvlc_reference_caffenet
https://blogs.nvidia.com/blog/2015/03/17/digits-devbox/
Table 8: Summary of Machines and Clusters. The given machines/cluster can provide. We are unable to open $3 4 \times$GPU machines due to limited EC2 availability and therefore there is no GPU-L.

| Name      | Machines | TFLOPS | Network | $/hour |
|-----------|----------|--------|---------|--------|
| 1xCPU     | 1 \times c4.4xlarge | 0.74   | -       | $0.84  |
| 2xCPU     | 1 \times c4.8xlarge | 1.67   | -       | $1.68  |
| 1xGPU     | 1 \times g2.2xlarge | 1.23   | -       | $0.65  |
| 4xGPU     | 1 \times g2.8xlarge | 4.89   | -       | $2.60  |

| Name      | Machines       | TFLOPS | Network | $/hour |
|-----------|----------------|--------|---------|--------|
| CPU-S     | 9 \times c4.4xlarge | 6.68   | 1 Gbits | $7.56  |
| CPU-L     | 33 \times c4.4xlarge | 24.51  | 1 Gbits | $27.72 |
| GPU-S     | 9 \times g2.8xlarge | 44.24  | 10 Gbits | $23.40 |

Figure 8: Statistics of Data Sets. All data sets are image-related except Shakespeare, a natural language corpus for text synthesis used in our RNN experiments.

Figure 9: Summary of Machines and Clusters. TFLOPS are the total TFLOPS that the given machine/cluster can provide. We are unable to open $3 4 \times$GPU machines due to limited EC2 availability and therefore there is no GPU-L.

We validate our claim that Omnivore’s performance is FLOPS-proportional, which means it scales with available FLOPS, regardless of the number or type of devices available. We first explain the protocol of our experiments. Then we report our results and discuss the importance of FLOPS-proportional system performance.

6.2.2 Single Machine Experiments

We validate our claim that Omnivore’s performance is FLOPS-proportional, which means it scales with available FLOPS, regardless of the number or type of devices available. We first explain the protocol of our experiments. Then we report our results and discuss the importance of FLOPS-proportional system performance.

Protocol. We compare Omnivore against Caffe and TensorFlow on a single machine. We train CaffeNet on the full ImageNet dataset on hardware described in Figure 9. We measure the time each system needs to finish 40 iterations of training (following 10 iterations of warm-up), using the standard batch size in CaffeNet (256 images). Our single-machine optimizations only affect hardware efficiency; the number of iterations needed for convergence does not change. Hence, we can use time per iteration as a surrogate for performance.

6.2.1 End-to-end Performance

For large datasets, Omnivore is faster than state-of-the-art tools. We validate this on ImageNet, the de facto deep learning benchmark. We compare Omnivore with MXNet and SINGA. We train the standard CaffeNet on all systems using both CPU-L and GPU-S clusters. We time out each run after 8 hours and report the training accuracy at a given time. We tune all competitor systems following the official performance tuning guidelines. (We describe the full setting in Appendix F. The time for this tuning of other tools exceeds Omnivore’s automatic tuning time for the cold start phase so we omit these initial tuning times). For Omnivore, we use its automatic optimizer that does not require any hyperparameters. Because SINGA is always slower than MXNet in our experiments, we omit it from this figure but discuss SINGA more in Section 6.2.3.

Figure 10 shows the result. We report sync and async for MXNet as their documentation suggests trying both. Omnivore reaches the same accuracy up to $11 \times$ faster than MXNet on the GPU cluster and $12 \times$ faster on the CPU cluster. Compared to sync, Omnivore is $4.5 \times$ and $1.9 \times$ faster respectively. This includes the 10% overhead of Omnivore’s optimizer during the run. The optimizer reduces momentum or learning rate each time it runs (full details in Appendix F.5). In the remainder of this section we conduct detailed analysis of Omnivore, MXNet, and SINGA to understand this improvement. As we will see, Omnivore’s optimizer, which searches within the larger tradeoff space, is the key reason for our system’s performance.
Results. Figure 11 shows the results. We normalize all execution times by the slowest system in each column and report the resulting speedups. We see that on a single CPU, Omnivore is 3.9× faster than both Caffe and TensorFlow; on a single GPU, all systems show similar speed. This is consistent with our observation in Section 5.2. TensorFlow and Caffe use the same strategy for both CPU and GPU, which is optimal for GPU but suboptimal for CPU. One interesting consequence of this speedup result is that, although Caffe on 1xCPU is 7× slower than on 1xGPU, Omnivore is only 1.8× slower on 1xCPU, which we will see matches the FLOPS ratio of these devices. The gap increases for more CPU sockets (2xCPU) or GPU cards (4xGPU).\footnote{\textsuperscript{8}We also run experiments on a 4-socket, 56-core Haswell CPU machine, and Omnivore is 13× faster than Caffe.}

FLOPS Proportionality. The training performance of CPUs is commonly believed to be an order of magnitude slower than GPU performance. Literature often reports so; we also see that this is the case for Caffe on 1xCPU and 1xGPU. We validate that Omnivore delivers performance proportional to the FLOPS that a device can provide.\footnote{\textsuperscript{9}SINGA does not converge to 99% in 2 hours and Omnivore is 11× faster than SINGA to reach 60% accuracy.} As shown in Figure 9, 1xGPU provides 1.7× more FLOPS than 1xCPU, and Omnivore has a 1.8× gap between 1xCPU and 1xGPU. In other words, regardless of the type of device, Omnivore performs proportionally to the number of FLOPS available. We also observe that proportionality holds for all machines in Table 9; details are deferred to Appendix C.5. FLOPS-proportionality means that, using both CPUs and GPUs on the same machine, we should be able to construct an even faster system. We validate this by using both CPUs and GPUs on 4xGPU, whose CPU and GPU provides 0.67 TFLOPS and 4.89 TFLOPS, respectively. By using data parallelism across the CPU and a single GPU, Omnivore achieves an 18% speedup over just using the GPU.

6.2.3 Distributed Experiments

We now conduct experiments to understand our end-to-end improvement across three different clusters described in Figure 9. As we will show, our tradeoff characterization contributes to the performance gains of Omnivore. We first describe the settings and the performance metric used in the experiments. Then we discuss the optimizer’s contribution and analyze across different clusters.

Protocol. A systematic understanding of the performance gap between Omnivore, MXNet, and SINGA requires running multiple systems to convergence under multiple settings. For this reason, we focus on ImageNet\textsuperscript{8} that contains the first eight classes of ImageNet. This allows us to grid search all parameters in MXNet and SINGA, including synchronization strategies and learning rate, and pick the best run. Because the goal of this section is to understand the difference of training performance, we do not include the time of our optimizer, which also takes significantly less time compared with the grid search we did for MXNet and SINGA. We run all systems for 2 hours and measure the training accuracy at a given time. Figure 12 shows the results.

Results. (Small CPU Cluster: CPU-S) CPU-S is a small CPU cluster that contains 9 1xCPU machines. Because each machine is slow and the network is fast, we expect that a fully synchronous strategy will be fast in terms of hardware efficiency while having the best statistical efficiency. Figure 12(a) shows the results. All systems reach accuracy 60% within 2 hours, and Omnivore reaches 60% the fastest. Omnivore is 2.3× faster than MXNet (388 seconds vs. 907 seconds). At 3000 seconds, Omnivore already achieves an accuracy > 99%, while MXNet achieves the same accuracy after 7000 seconds. The speed up here is also 2.3×. As expected, both systems chose a fully synchronous strategy, so statistical efficiency is not the cause of this performance gap. The 2.3× speed up is due to our CPU-based optimization (Section 5.1)\footnote{\textsuperscript{10}As of the time of writing, SINGA does not support GPUs and is omitted from Figure 12(b).} and merging FC servers (Section 5.1).

(Small GPU Cluster: GPU-S) GPU-S is a small GPU cluster that contains 9 4xGPU machines (36 GPUs). In this case, because each node is significantly (7×) faster than 1xCPU, we expect the optimal strategy to be more asynchronous, and thus, statistical efficiency to come into play. Figure 12(b) shows the results\textsuperscript{10}. Similarly to the CPU-S cluster, Omnivore outperforms MXNet: it reaches 99% accuracy 4.8× faster. MXNet only supports completely synchronous or asynchronous execution, and its optimal run uses the completely synchronous strategy. On the other hand, Omnivore’s optimizer chooses to run with two compute groups. Had Omnivore chosen the same strategy as MXNet, it would be 1.7× slower than Omnivore’s actual choice due to a different choice of the synchronization strategy. The remainder of the 4.8× gap is due to the physical mapping (merging FC) used by Omnivore, and this improves both HE and SE; while originally described as a mechanism to reduce network communication\textsuperscript{7}, we find that merged FC also improves SE by reducing staleness in the FC model.
**Importance of Choosing the Right Number of Compute Groups**

This shows the importance of choosing the right number of compute groups to balance both SE and HE.

**Impact of Optimizer**

In the experiments above, we use grid search to find the optimal strategy for both MXNet and SINGA. On the other hand, Omnivore relies on the optimizer to automatically choose the best strategy. Had we not used the grid search for MXNet and relied on default parameters, the performance gap would be 20× on ImageNet8. This is compared to MXNet’s completely asynchronous strategy, which is recommended in their performance tuning guideline for networks like AlexNet. We study this in more detail in Appendix F.3.

**Comparison across Clusters**

Omnivore’s optimizer makes different choices on different clusters. It is interesting to compare them. As we can see, given the same amount of machines (CPU-S vs. GPU-S), as devices get faster, Omnivore tends to choose more asynchronous strategies. Intuitively, the faster compute nodes get, the easier for the network to get congested. The fully synchronous approach incurs higher penalty in that case. On the other hand, given the same speed of each compute node (CPU-S vs. CPU-L), when the number of machines gets larger, Omnivore also tends to choose a strategy that is between a fully synchronous and a fully asynchronous strategy: (1) when the staleness gets very large, even a properly tuned, fully asynchronous strategy incurs a penalty in terms of statistical efficiency, and (2) when the number of machines that need to be synchronized gets larger, a fully synchronous strategy incurs a penalty in terms of hardware efficiency. Omnivore’s optimizer makes it possible for us to be robust across different devices and cluster sizes.

### 6.3 Tradeoff and Optimizer of Omnivore

We validate the hypothesis that (1) the tradeoffs studied in this paper and (2) the automatic optimizer have a significant impact on the performance of Omnivore. We study the importance of compute groups, as well as compute-group-specific momentum tuning. We also study the effectiveness of Omnivore’s automatic optimizer for this tradeoff space by comparing it against a standard Bayesian optimizer.

#### 6.3.1 The Tradeoff Space

In this section we demonstrate that the various dimensions of the tradeoff space have a significant impact on performance. Throughout this paper we already illustrated some of these tradeoffs, so here we only summarize them and leave the detailed discussion Appendix F.3. In Section 6.2.3 and

![Figure 13: Lesion study of momentum. Default momentum = 0.9, which is also the optimal momentum for the fully synchronous strategy.](image)

Section 6.1 we showed that tuning the learning rate is necessary for convergence and that the physical mapping has both HE and SE benefits. In Section 5.2 we showed that using the right number of compute groups can yield 6.7× speedups compared to fully synchronous and 1.8× compared to fully asynchronous execution. We now focus on the importance of properly tuned momentum, which as we prove in Section 4.2, is a function of the level of asynchrony.

**Importance of Momentum Tuning.** We validate that the correct value of momentum depends on the number of groups. We expect that properly tuned momentum would outperform a momentum tuned agnostically to the number of compute groups. Therefore, we compare different methods of momentum tuning on the optimal number groups for ImageNet8 on CPU-L. The optimal number of groups for ImageNet8 on CPU-L is 4. We fix that number of groups and (i) set momentum to 0.9 (as reported in AlexNet [17]); (ii) use the momentum tuned for a synchronous system; (iii) tune the momentum using Omnivore’s optimizer for 4 compute groups. As we see in Figure 13, tuning for the right amount of asynchrony is important: if Omnivore did not tune momentum, it would be 1.5× slower. This both verifies our expectations for this experiment and provides further support for our theory in Section 4.2.

**Discussion: Other Models.** We find that these tradeoffs are impactful when applied to other models. We find that for Recurrent Neural Network models and LSTM models (e.g., [11]), the same choices affect performance—for example, choosing a completely synchronous or asynchronous configuration can be up to 2× slower than the optimal configuration. We report the details in Appendix F.6. This could imply speedups for applications in which RNNs are widely used, such as handwriting, speech recognition, and general sequence or time-series data.

#### 6.3.2 Optimizer

We validate that our optimizer outperforms state-of-the-art Bayesian optimization algorithms. We compare our optimizer with the optimizer proposed by Snoek et al. [22], which requires knowledge of the number epochs to run. To be fair we give the Bayesian Optimizer this information. We measure both the number of configurations and the total number of epochs that the Bayesian optimizer needs to achieve an accuracy within 1% of the configuration with the highest accuracy after 1000 seconds. In our experiments, the Bayesian optimizer never discovers a configuration which outperforms the optimal configuration obtained by grid search. We report the detailed result in Appendix F.8. We found that
the Bayesian optimizer takes 12 runs to find a near-optimal strategy, which on average is 6× more epochs than running that strategy. Because of this search overhead it was not feasible to use the full ImageNet1000 dataset so we used ImageNet8 (whereas recall from Figure 10() than Omnivore had an overhead of only 10% on ImageNet1000). We used the GPU-S cluster. Typically Bayesian optimizers can amortize this cost by running in parallel, but here that is not possible as the parameters depend on the hardware configuration and so the optimizer needs complete access to the entire cluster.

7. RELATED WORK

Single Node. Optimizing CNN performance has become a well-studied problem in recent years. Popular libraries include Caffe [16], cuDNN [6], TensorFlow [3], Theano [2], and Torch [12]. To compute convolutions, many of these frameworks use lowering, an idea proposed by Chellapilla et al. [4] that takes advantage of highly-optimized BLAS libraries. Our work follows from this line of research and demonstrates how to optimize lowering for CPUs in order to build a system which is robust to different types of hardware.

Distributed Deep Learning. Distributed systems for Deep Learning is a popular topic including SINGA [25], MXNet [9], FireCaffe [15], SparkNet [10], DLA [14], Google's DistBeliever [8], and Microsoft's Project Adam [3]. Each selects different execution strategies and other optimizations. A contribution of our study is to show a combined trade-off space including the union of all these techniques. We did this by decoupling the hardware and statistical efficiency for each technique and optimizing these separately. Our work is the first to provide a theoretical characterization for statistical efficiency and to demonstrate that hyper-parameters need to be adjusted in order to compensate for asynchrony.

The idea of splitting number of iterations and time per iteration and analyzing each separately is not new for distributed CNN systems. MXNet reported hardware efficiency and statistical efficiency separately, providing a plot of accuracy vs. iteration which was decoupled from the time per iteration. SINGA also decoupled these, and also went deeper into the tradeoff, identifying the compute group size as a tunable parameter. They advocate combining both synchronous and asynchronous training and offer a flexible training architecture which enables trading off the convergence rate with the time per iteration in order to to minimize training time. However, while SINGA identifies this tradeoff and provides experimental evidence of its importance similar to the curves we showed, the onus is currently on the user to manually select the optimal configuration.

SparkNet also separated the time per iteration and number of iterations by building models of each. They did not explore the same tradeoff of machines per group, but rather a similar tradeoff related to staleness. Because SparkNet uses a MapReduce framework they implement model averaging (see terminology section in Appendix D.2). Within this technique they explore, in isolation, how the staleness (their $\tau$ parameter) impacts the number of iterations to convergence and the time per iteration. Their hardware efficiency model was measured (both network speed and compute time) and their statistical efficiency model was also empirical (they varied staleness and measured the $SE$ penalty).

8. CONCLUSIONS

We described the first explicit study of the tradeoff space for deep learning systems, a popular, high-value type of industrially deployed learning systems. We identified critical issues in how one maps layers to devices and are the first to systematically study widely used techniques like asynchrony. We designed a new optimizer and showed that it has excellent end-to-end performance and is independent of our particular implementation substructure.

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while Intel’s current Haswell CPU can achieve 1.4 TFLOPS on a single chip. Moreover, SIMD parallelism has doubled in each of the last four Intel CPU generations and is likely to continue.

B. APPENDIX FOR BACKGROUND (SECTION 2)

B.1 CNN Computation

AlexNet FLOPS. We approximate the FLOPs (# floating point operations) in AlexNet by the sum of all the GEMM operations with batch size 256. Specifically, we add 1 GEMM in the forward pass for each Conv and FC layer, plus two GEMMs in the backward pass for each Conv and FC layer (although Conv1 backward has only 1 GEMM because no gradient is needed with respect to the data).

Terminology. This section introduces model and data parallelism as two techniques to parallelize CNNs. For a full description of these concepts, see the Terminology in Appendix D.2.

CNN Trends. This section viewed CNNs as two phases, Conv and FC. Recent CNNs, e.g. Residual Networks (ResNets) and Inception Networks, can also be categorized into this partitioning. For instance early Inception variants contained multiple FC layers at different parts of the network, but from a computational point of view these are all considered to be part of the FC phase.

In particular, CNNs have undergone a number of changes in the past few years. We summarize a few here:

- Multiple FC layers replaced with average pooling, leaving a single fully-connected layer (for the softmax). This leads to a reduction in the overall model size (e.g. 60 million parameters for AlexNet compared to 4 million for GoogleNet).
- Increase in network depth (e.g. AlexNet with 5 conv layers, compared to ResNet with > 150). This increases memory requirements of networks, and makes multi-device training necessary.

As we will see, the optimizer presented in this paper considers the impacts of each of these points when making decisions for physical mapping and execution strategy.

Table 1: Tradeoff space when designing distributed deep learning systems.

| Tradeoff                  | Some Examples                                      |
|---------------------------|----------------------------------------------------|
| Single Node Hardware      | CPUs, GPUs, both together                         |
| Type of Parallelism       | Model, Data                                        |
| Batch size                | Large (few accurate updates), Small (many parallel updates) |
| Batch allocation within node | 1 CPU or GPU per batch, many CPUs or GPUs per batch |
| Batch allocation across nodes | 1 batch across all machines, 1 parallel batch per machine, groups of machines per batch |
| Combining Model Replicas  | Atomic gradient updates, Model averaging, Ensembles, Race conditions (Hogwild!) |
| Server Architecture       | Separate parameter/compute, Merged parameter/compute |
| Network Architecture      | Model Size (impacts communication), Model Depth (impacts memory / batch size) |
| Optimization Algorithm    | SGD, Adagrad, momentum                             |
| Hyperparameter Optimization | Grid/Random search, Bayesian, Plateau (e.g. ResNet), Decay Schedule (e.g. Inception-v4) |

APPENDIX

A. APPENDIX FOR INTRODUCTION (SECTION 1)

Tradeoff Table. While many distributed deep learning systems exist, each of these makes design decisions suited for a particular type of (1) compute cluster, (2) deep learning model and (3) dataset, although these same decisions may not work for other problem settings or hardware resources. This is because deep learning is known to be complex both from a computational and machine learning perspective, and designing a highly efficient and scalable deep learning engine involves a number of interrelated design decisions. Table 1 shows a number of factors to consider when designing distributed deep learning systems. Given a fixed number of machines, a number of tradeoffs exist from how to use hardware on each node, how to allocate batches of data to machines, to the type of deep learning model to use in order to minimize communication. In addition, these decisions impact one another – for instance the batch size influences the number of machines which can be used to effectively parallelize within a batch and therefore influences the total number of parallel gradients being computed to update the model. Our work, which is a study, demystifies these factors by identifying the key tradeoffs which underlie all design decisions and quantifying the impact of those tradeoffs experimentally.

Contribution 1: Single-Node Optimization

Even focusing on just a single node, there has been a long debate about CPUs vs GPUs for deep learning. GPUs are popular for CNN systems because of the high throughput they provide. Modern GPUs offer between 1.2 TFLOPS (NVIDIA GRID K520, per GPU) and 8 TFLOPS (NVIDIA Titan Z). However, GPUs contain smaller off-chip memories than CPUs, and GPUs are connected to host memory by a slow PCI-e interconnect. On the other hand, Microsoft’s Project Adam argues that CPUs can deliver more cost-effective performance. This debate is only going to get more interesting, as modern GPUs offer high-speed interconnect with host memory, while Intel’s current Haswell CPU can achieve 1.4 TFLOPS on a single chip. Moreover, SIMD parallelism has doubled in each of the last four Intel CPU generations and is likely to continue.
B.2 Problem Definition

Scope of Work. Our work does not focus on improving machine learning techniques but rather studies systems trade-offs in order to build an optimizer that is robust to the most widely used networks/algorithms. Our study uses the SGD algorithm due to its popularity, although our optimizer applies to other algorithms as well. Similarly we do not modify the CNN architecture but assume that this is provided by the user.

Terminology. The physical mapping maps the layer computation to vertices in G. Vertices in G may contain other vertices, e.g. GPUs or CPU cores within a machine. Section 3 first studies how to map the CNN to hardware within a machine, and concludes that with proper optimization only the throughput of each vertex matters, not its underlying hardware. Section 4 then studies how to map the CNN to all of G, i.e. across machines.

C. APPENDIX FOR SINGLE-NODE TRADEOFFS (SECTION 3)

This section describes the optimizer’s physical plan (how to map the CNN to hardware) at the level of a single machine. Given a machine containing devices of various throughput (CPUs, GPUs), our goal is to run the CNN computation as quickly as possible. We do this by identifying two tradeoffs. Our first tradeoff introduces a data batching technique which trades off memory footprint for compute time. We demonstrate that this tradeoff gives a > 5 × CPU speedup over existing systems. With this optimization now both CPUs and GPUs give throughput proportional to the FLOPS offered by the device, and our second tradeoff partitions the CNN computation across both the CPU and GPU to combine their FLOPS – a known HPC trick, but one which has not been applied to CNNs.

C.1 Convolutional Layer Computation

A 3D convolution consumes a pair of order 3 tensors—the data D ∈ Rn×m×d in and the kernel K ∈ Rk×k×d in. For example, if D is a color image with 3 (RGB) color channels, d in = 3. In AlexNet [17], n ∈ [13, 227], k ∈ [3, 11], and d in ∈ [3, 384]. The output is a 2D matrix R ∈ Rm×out where m = n − k + 1 and each element Rx,y is defined as:

\[ R_{x,y} = \sum_{d'=-1}^{d} \sum_{x'=0}^{k-1} \sum_{y'=0}^{k-1} D_{x+\frac{d'}{2}+x',y+\frac{d'}{2}+y'} \cdot K_{x',y',d'} \]  

The kernel also supports parameters called padding and stride, which affect the size of m. For details on stride and padding see [http://cs231n.github.io/convolutional-networks/#conv](http://cs231n.github.io/convolutional-networks/#conv). This is the standard image 3D discrete convolution. A convolution layer in the CNN contains a number of kernels \( \{K_j\} \), not just one, where we call \( d_{out} = |K_j| \) the number of output channels. These kernels \( \{K_j\} \) constitute the model of the convolutional layer, and the reason for computing multiple kernels rather than just 1 in the convolutional layer is to be a more powerful machine learning model. The convolutional layer takes as input the 3D data tensor D and performs \( d_{out} \) 3D convolutions, one per \( \{K_j\} \), such that the output of the convolutional layer is now not a 2D matrix R but a 3D tensor \( R \in R^{m \times x \times d_{out}} \). Similarly the model of the CNN can be viewed as a 4D tensor \( K \in R^{k \times k \times d_{in} \times d_{out}} \).

Finally, recall that often rather than process a single data example the CNN processes a batch of b examples simultaneously. The motivation for doing this is that gradient computations during learning are less noisy. Therefore in the most general case, the input D to a convolutional layer is not 1 but \( b \times 3 \) data tensors, or equivalently a 4D data tensor \( D \in R^{n \times m \times d_{in} \times b} \). The model is unchanged, but the convolutional layer now performs the \( d_{out} \) 3D convolutions on each element in the batch, i.e. the batched convolution layer performs \( b \times d_{out} \) 3D convolutions. The output of the convolutional layer is therefore also a 4D tensor, \( R \in R^{m \times x \times d_{out} \times b} \).

To summarize, a convolutional layer accepts as input a 4D data tensor \( D \in R^{n \times m \times d_{in} \times b} \), performs a total of \( b \times d_{out} \) 3D discrete convolutions using \( D \) and its model \( K \in R^{k \times k \times d_{in} \times d_{out}} \), and outputs a 4D output data tensor \( R \in R^{m \times x \times d_{out} \times b} \). The full formula is:

\[ R_{x,y,z,w} = \sum_{d'=0}^{d_{in}-1} \sum_{x'=0}^{k-1} \sum_{y'=0}^{k-1} D_{x+\frac{d'}{2}+x',y+\frac{d'}{2}+y',z,w} \cdot K_{x',y',d'} \]  

Many implementations of this convolutional layer exist. Like most other HPC kernels, a straightforward implementation of this operation is suboptimal. Optimized implementations include directly computing the convolutions, as in cuda-convnet2 [41], computing the convolution as a discrete Fourier transform as in [24], or implementing the convolution as a matrix multiply, as in Caffe [16] or cuDNN [4]. While the studies in these papers conclude that different strategies perform best for different kernel sizes, cuDNN [4] demonstrates that the third technique of performing convolution as a matrix multiplication is versatile and fast for a range of size parameters, as matrix multiplication kernels are often highly optimized.

In order for the convolution to be carried out as a matrix multiplication, an initial reformatting phase called lowering is required to put the data and kernel into the correct format, which we discuss in the next subsection of this appendix.

C.1.1 Convolution by Lowering and GEMM

Lowering followed by a general dense matrix multiplication (GEMM) is a popular way to implement the convolution operation. Figure 2 shows the three logical steps in the lowering process: (1) lowering, which transforms 4D tensors \( D \) and \( K \) into 2D matrices \( \hat{D} \) and \( \hat{K} \); (2) matrix multiply (GEMM), in which we multiply \( \hat{D} \hat{K} \) to get the result \( \hat{R} \); and (3) lifting, which transforms \( \hat{R} \) back to a tensor representation of \( R \).

Lowering Phase in which we construct the matrix \( \hat{D} \) and \( \hat{K} \). A value of \( D \) will appear more than once in the lowered matrices.

Multiply Phase (GEMM) in which we multiply \( \hat{D} \) and \( \hat{K} \) to create \( \hat{R} = \hat{D} \hat{K} \).

Lifting Phase in which we map \( \hat{R} \) back to \( R \).

Three techniques exist to perform this process, each corresponding to a different way to group the sum in Equation 5. Each of these techniques requires replicating the data or the kernel in order to allow the convolution to be implemented.10

https://code.google.com/p/cuda-convnet2/
as a GEMM, but the amount of replication and the size of the GEMM depend on whether the replication happens in the lowering phase, lifting phase, or partly in each. The tradeoff is studied in detail by [13], which concludes that the best choice is determined entirely by the ratio $d_{in}/d_{out}$ (the ratio of the number of input channels to the number of output channels of the convolution), and that for modern CNNs these ratios suggest that the data replication should be done during the lowering phase. Therefore in the lowering used by this work, there are two components to convolution: lowering (which requires replication of data), and the GEMM. The lifting does not require any memory copies or computation in the optimal technique. Note also that in this technique, the kernel does not require any replication, only the data. CNNs are continuously evolving however, and so it is possible that future CNN architectures will benefit from other lowering strategies. For a full study of the lowering tradeoff, refer to [13].

The amount of data replication required by the lowering in this work is $m^2 k^2/n^2$, where $m < n$ and $m$ depends on the stride and padding of the convolution. The replication can be on the order of 1 to 2 orders of magnitude (i.e. $10-100 \times$ more data). In turn, this blowup in the data size requires more memory and computation in step 2 (GEMM). The benefit however is that a sparse computation has become dense, which is important for hardware implementations because the direct computation of the 3D convolution is usually memory bandwidth-bound (due to the small convolution window size, $k \in [3,11]$). A GEMM implementation on the other hand, while performing more computation as a result of lowering, receives hardware acceleration which eclipses the increase in data size.  

C.2 Batching and Data Parallelism  

C.2.1 Batching Analysis  

Batching is the implementation tradeoff that arises between the CPU and GPU as a result of available off-chip memory. It concerns how many images of the batch to process in parallel by the convolution layer. Recall that $b_p$ images are processed in parallel, where where $1 \leq b_p \leq b$. $b$ is the batch size, i.e. the total number of images that need to be processed. The value of $b_p$ (how much to batch to the convolution computation) is determined by how many lowered images can be stored in off-chip memory.

Modern GPU cards cannot store entire batches of lowered data into off-chip memory and implementations of CNNs on GPUs perform lowering and GEMM serially on one or few images at a time until all $b$ have been processed, i.e. $b_p = 1$. On the CPU, off-chip memory is larger which allows for batching techniques that perform lowering and GEMM on all images in parallel and therefore allow CPU caches and vector instructions to be fully utilized. This tradeoff is more complex and is solved by the CPU by using parallelism in the GEMM kernel. For modern CPUs, memory is large and so $b = b_p$, for the remaining CPU experiments in this section.

C.2.2 Data Parallelism in non-GEMM Kernels  

On the CPU, recall that the batching technique above makes a single matrix that is $b$ times (full batch size) larger than it would be for a single image, and then performs a single GEMM on this large matrix. A related strategy is to split a batch into multiple partitions, and process each partition in parallel using a separate thread.  

For GEMM, processing an entire batch of size $b$ with $n$ threads is equivalent to partitioning the batch into $p$ partitions of size $b/p$ with $n/p$ threads used in each GEMM. For example, batching $b$ images and performing a single GEMM with 8 threads is equivalent to creating 8 matrices, each with $b/8$ images, and performing 8 parallel GEMM kernels with 1 thread each. These are equivalent as this is exactly how BLAS parallelizes GEMM: by partitioning partition columns of B in $A \times B$ and allocating 1 thread per partition.

While partitioning and then performing the GEMM kernel is the same as simply performing the GEMM kernel, this is not true for other kernels which are not multi-threaded For non-GEMM kernels such as lowering, or other layers such as pooling, the second technique of partitioning the batch and processing each partition using a separate thread gives significant speedups (this is simply data parallelism) across all cores. For example, it can be used to lower images in parallel using all cores by assigning a subset of the images in the batch to each core.

Figure [3] shows the impact of data parallelism on a full end-to-end CaffeNet on the EC2 c4.xlarge instance with 8 physical cores (CPU only). The batch size used is 256 images and the horizontal axis represents into how many parallel partitions we partitioned these 256 images for each layer of the CNN. I.e. the horizontal axis is the number of
of threads used for data parallelism. Note that the GEMM kernel is always parallelized (OpenBLAS was used) and uses the maximum number of threads (16).

“None” indicates the default Caffe implementation. For all layers, each image is processed serially. For example, one image is lowered, then the convolution GEMM is performed, and then the next image is lowered, etc. The only multi-threaded kernels are the BLAS GEMM kernels used in the convolution and FC.

“1” is identical to the Caffe implementation except that lowering is first done for all images (serially, i.e. one image lowered at a time), and then a single, large GEMM is done for the convolution. All other layers are the same.

For all other number of parallel partitions $p$, the 256 images were equally split into $p$ partitions. For example if $p = 2$, two partitions of size 128 images each were created. Then, layers processed each partition in parallel, one thread per partition. For example if $p = 2$, lowering was done with two threads, each lowering 128 images. Following the lowering, a GEMM was performed for each partition. The total number of threads used for these GEMM kernels was always 16, i.e. the GEMM is performed on each partition with 16/p threads per GEMM.

Figure 14 (None vs 1) shows that batching the GEMM kernels (one large GEMM as opposed to 256 smaller ones) saves $\sim 2.2$ s of convolution time. Then, data parallelism provides another $\sim 10$ s of reduction. The final time is then 4s, where $\sim 3$s is spend in convolution layers. Therefore the batching of the GEMM made the convolution roughly $\sim 2 \times$ faster (in the optimized execution), and the remaining speedups were due to data parallelism.

Finally, studying more closely the speedups from data parallelism, the time reduction from 14 seconds to 4 seconds from data parallelism was roughly 80% due to speeding up the lowering, and 20% due to speeding up the other layers. I.e. the final iteration time would be $\sim 6$ s if data parallelism was only used for the Conv layers. The remaining 20% is for data parallelism in pooling, normalization, dropout and ReLU layers. Fully-Connected layers are simply a GEMM which always uses 16 threads, so data parallelism and model parallelism do not apply on the CPU, although as we also saw previously this GEMM can be made slightly faster by using 8 threads instead for the FC layers (because there are 8 physical cores).

Overall, batching combined with data parallelism gives more than a $4 \times$ speedup end-to-end when running Caffe’s AlexNet on 8 physical cores. Importantly, this end-to-end speed is now proportional to the peak throughput of the CPU.

In summary, we show two sources of speedup on the CPU. First, by batching the lowering and GEMM, we perform a single GEMM which is $b \times$ larger, as opposed to $b$ smaller GEMMs, which as described above has better hardware utilization on the CPU. Second, we apply the batch partition (data parallel) technique above to parallelize non-GEMM kernels such as lowering. These optimizations are possible for the CPU because it has more memory to store the lowered matrices. As a result the CPU performance is proportional to the device FLOPS, which allows partitioning computation across both the CPU and GPU proportional to the device throughput.

C.3 Device Throughput

**FLOPS Experiments.** Figure 3 showed throughput for the CNN when using Caffe, Omnivore and also for reference a single-precision GEMM kernel. For the CPU the GEMM experiment used OpenBLAS and matrices of size 16384 $\times$ 16384. For the GPU GEMM we used a GEMM kernel from NVIDIA’s CUDA examples. For Caffe and Omnivore we focus on only the Convolution layers, specifically the time to run forwards and backwards on all 5 layers of CaffeNet.

**FLOPS calculations.** The c4.4xlarge instance contains a single-socket Haswell CPU with 8 physical cores. The c4.4xlarge instance CPU FLOPS are calculated as: 8 physical cores $\times$ 2.9 GHz $\times$ 32 = 0.742 TFLOPS, where 32 is the single-precision Haswell instructions per cycle (8-float SIMD $\times$ 2 FMA per cycle, and FMA is fused-multiply-add).

Each g2.2xlarge instance provides a single Grid K520 GPU, i.e. 1536 cores $\times$ 800 MHz = 1.23 TFLOPS (the Grid K520 contains a total of 3072 cores, 1536/GPU).

The c4.8xlarge instance contains a dual-socket Haswell CPU with 16 physical cores. The FLOPS are calculated as: 16 physical cores $\times$ 2.9 GHz $\times$ 32 = 1.670 TFLOPS.

C.4 FLOPS-Proportional Scheduling

Given that both CPU and GPU speeds are now proportional to the device FLOPS, we next consider whether the CPU and GPU can be used simultaneously to process each layer. We do this using data parallelism (batch is partitioned, model is replicated) for all layers in the convolution phase, which is compute-bound and has small data. The tradeoff is what fraction of the batch to give to each device. We select the simple but optimal choice that a device should process a fraction $p$ of the input where $p$ is the proportion of total FLOPS which that device contributes. E.g. if a CPU provides 1 TFLOPS and a GPU 4 TFLOPS, 1/5 of the batch is processed by the CPU for an ideal speedup of 20% over the GPU alone.

C.5 Single-Node Experiments

Omnivore matches Caffe’s output on each layer. It accepts the same input files as Caffe and produces the same
| EC2 Instance Price, Hardware | System and Devices Used | Available TFLOPS | End-to-end Speedup |
|-------------------------------|-------------------------|------------------|-------------------|
| c4.4xlarge $0.84/hr, 8 CPU cores (Haswell) | Tensorflow CPU | 0.74 | 0.15x |
|                              | Caffe CPU               | 0.74 | 0.15x |
|                              | Omnivore CPU            | 0.74 | 0.57x |
| g2.2xlarge $0.65/hr, 1 K520 GPU | Tensorflow GPU*        | 1.23 | 0.93x |
|                              | Caffe (cuDNN v4) GPU    | 1.23 | 0.95x |
|                              | Omnivore GPU            | 1.23 | 0.97x |
|                              | Caffe GPU               | 1.23 | 1.00x |
|                              | Omnivore (cuDNN v3) GPU | 1.23 | 1.04x |
| c4.8xlarge $1.68/hr, 16 CPU cores (Haswell) | Caffe CPU | 1.67 | 0.15x |
|                              | TensorFlow CPU          | 1.67 | 0.16x |
|                              | Omnivore CPU            | 1.67 | 0.83x |
| g2.8xlarge $2.60/hr, 4 K520 GPUs, 16 CPU cores (Ivy Bridge) | Omnivore 1GPU+CPU | 1.89 | 1.14x |
|                              | Caffe (cuDNN v4) GPU    | 4.89 | 0.61x |
|                              | Caffe (cuDNN v3) GPU    | 4.89 | 0.68x |
|                              | Caffe 4GPU              | 4.89 | 0.94x |
|                              | TensorFlow 4GPU*        | 4.89 | 1.18x |
|                              | Omnivore 4GPU           | 4.89 | 3.14x |

* Tensorflow uses cuDNN v4, which we observe is always faster than v3 for Tensorflow

Figure 15: End-to-end performance comparison across EC2 machines on CaffeNet. All numbers are normalized as the speedup over running Caffe's GPU version on g2.2xlarge instance ($0.65/hour).

Our experiments compare against Caffe and use the CaffeNet CNN, which is Caffe's implementation of the popular AlexNet (the default architecture for benchmarking), as well as the ImageNet dataset.

Both systems take as input the same network configuration files that Caffe provides. We remove grouping for convolution layers because the full AlexNet fits in the memory of a single K520 (g2.2xlarge) GPU. We use the same external libraries for both Caffe and Omnivore: GCC-4.8, CUDA-7.5, and OpenBLAS. For Caffe we report both cuDNN v3 and v4.

We built the same timer into Caffe and Omnivore (measuring wall-clock time, clock_gettime in C). We run for 50 iterations and omit the first 10 times as there may be disk or other delays in the first few iterations not representative of steady-state execution. Beyond these first 10 iterations we noticed that all iterations were consistent in terms of time for both tools and had a coefficient of variation less than 5%.

We also ran Tensorflow using the same protocol as above (40 iterations, burn-in of 10, identical network).

### C.5.1 End-to-end Performance

Figure 15 also shows the results of running Omnivore and Caffe on various EC2 instances. Given that Omnivore and Caffe generate the same outputs, we concentrate on throughput. We ran both Omnivore and Caffe on each EC2 instance for 50 iterations, and counted the last 40. On the c4.4xlarge GPU instance Omnivore outperforms Caffe by nearly 4× due to batching and data parallelism. On the g2.2xlarge GPU instance Omnivore and Caffe achieve the same speed (within 5%). Note that the c4.4xlarge instance offers 60% of the TFLOPS of the g2.2xlarge instance, and the ratio of Omnivore speeds on these instances is 59%, i.e. Omnivore delivers speed proportional to the TFLOPS. On the two-socket c4.8xlarge CPU instance Omnivore is now 5.5× faster than Caffe. Caffe does not speed up given the additional cores, but Omnivore does. The speedup is not linear because the extra cores are distributed across sockets and not all layers are compute-bound. However, these results show that given similar device throughput, CPU CNN performance is not an order of magnitude slower than GPU performance as the literature often reports and as is the case in Caffe. Lastly we compared Omnivore to Caffe on a 4-socket, 56-core Haswell (non-EC2) CPU machine, and Omnivore is 13× faster than Caffe.

**FLOPS calculations.** See Appendix C.3 for the FLOPS calculations in Figure 15.

### C.5.2 CPU/GPU Hybrid and Multi-GPU

Figure 15 also shows that using the CPU in a GPU instance can accelerate purely GPU training. The g2.8xlarge instance’s CPU provides 0.67 TFLOPS, and by using data parallelism across the CPU and a single GPU we achieve an 18% speedup in Omnivore end-to-end over just using the GPU. This is faster than all other single GPU results.

Finally, we also apply this data parallel partitioning across multiple GPUs. We ran both Omnivore and Caffe using the 4 GPUs on the g2.8xlarge instance and show that while Caffe actually slows down compared to the 1 GPU case, Omnivore becomes 3.1× faster.

For CPU + GPU, each g2.8xlarge GPU provides 1.23 TFLOPS as shown above, and the CPU provides 665.6 TFLOPS (Sandy/Ivy bridge, i.e. 16 SP instructions per cycle ×16 physical cores ×2.6 GHz). The ratio of CPU:GPU FLOPS is therefore 1.2; i.e. we should partition roughly 1/3 of the data on the CPU and 2/3 on the GPU. Since a batch size is 256 images, we rounded 67% on the GPU to 75%, such that the CPU processes 64 images, because this partition is better suited to hardware (although we see only a 5% speedup compared to using the exact ratio). This partitioning gives a 18% speedup over just using the GPU.

For parallelization across 4 GPUs, we use data parallelism for all layers (each GPU given 1/4 of the batch and a model replica) except for the FC layers, which use model parallelism (each GPU given 1/4 of the model and a replica of the batch).

We ran Caffe on 4 GPUs with cuDNN v4, cuDNN v3 and no cuDNN, and found that Caffe was fastest but neither gave a speedup compared to 1 GPU.

Therefore while CNN parallelization is challenging even for state-of-the-art systems, we’ve shown that FLOPS-proportional partitioning is possible across a range of hardware devices. We now extend this technique to multiple machines, where the added challenge of network delay motivates re-thinking the SGD algorithm.

D. APPENDIX FOR DISTRIBUTED TRADEOFFS (SECTION 4)
Having studied the tradeoffs for a single machine, this section now studies the distributed setting. The goal of this section is to build an optimizer that creates (1) a physical plan $P(A, G)$ which maps the CNN architecture $A$ to machines in the device graph $G$, and (2) an execution plan $E(G, D)$ which parallelizes SGD by allocating data batches from the dataset $D$ to each machine. This section begins by describing why these two are the most important tasks for the optimizer. While many distributed CNN systems exist and each describes their own distribution techniques, upon analyzing these strategies we discover that, though diverse, they all describe either (1) or (2) above. Given these two fundamental design dimensions, we then arrange existing strategies into a tradeoff space and restate our optimizer’s goal precisely within this space. The remainder of the section then quantifies the impact of these tradeoffs to allow optimization within the space.

### D.1 Distributed CNN Tradeoff Space

This section describes popular techniques for distributed CNN training and refines them into a tradeoff space.

#### D.1.1 Distributed Stochastic Gradient Descent

Recall that SGD iteration $i$ (1) reads a batch of data $B_i$, (2) uses the current model $M_i$ to compute the model gradient $\nabla M(M_i)$, and (3) subtracts $\nabla M(M_i)$ from $M_i$ to obtain $M_{i+1}$. Iteration $i + 1$ reads a new batch $B_{i+1}$ and the algorithm repeats until convergence.

Figure 16 (a) shows a common distributed implementation of SGD in which the entire CNN model is stored on a server called a model server or parameter server. There are also a number of compute servers which each perform the CNN calculation (Equations 2 and 3). Each iteration, every compute server reads $M$ over the network from the parameter server, as well as a batch of data $B$ from a local database. Each compute server calculates a gradient $\nabla M$ which is sent back to the parameter server and used to update the model. In this example, compute servers operate in parallel and do not synchronize or communicate with one another.

In Figure 16 (a), each server physically maps to a single machine (node). Generally, multiple servers can map to a single machine or a single server to multiple machines. For example, parameter and compute servers can map to the same node to reduce network communication. Figure 16 (b) shows a more complex server architecture for SGD in which rather than two types of servers (compute and model), there are now 4 types: (1) conv compute, (2) conv model, (3) FC compute, and (4) FC model. 1 and 2 are for layers in the conv phase of the CNN while 3 and 4 are for layers in the FC phase. In Figure 16 (b), the FC compute and model servers map physically to the same machine, i.e. the computation of the FC phase happens on the same machine as where the FC model is stored. There are many benefits to Figure 16 (b) vs. (a): Recall that FC has small data, large model whereas conv has large data, small model. This server architecture has the benefit of only needing to communicate the conv model (and its gradients) and the FC data (and its gradients) across the network. Second, computation is offloaded from the compute machines to the FC model server, which otherwise is majorly idle. These benefits both improve hardware efficiency, and were described in [7]. However, yet another benefit is that by having only a single FC compute machine, the FC model does not experience any staleness – a term we define next. This improves statistical efficiency.

#### D.1.2 Staleness

_Staleness_ is a metric used to quantify the statistical efficiency (# iterations to convergence). Figure 17 shows staleness graphically for the simple server architecture of Figure 16 (a). In Figure 17 (a) there is a single worker, and so that worker always computes the gradient using the current model. In this diagram, we assume that once a worker sends the updates back to the model server, it is immediately sent a new model, i.e. in this diagram, write/read is an atomic operation for each worker (the write to the model and read from the model happen together).

In Figure 17 (b), there are now two concurrent workers. Assume for now that (1) these workers update the model in round-robin order, (2) write/read is again atomic, and (3) the server architecture is again as in Figure 16 (a). We notice that now each worker computes the gradient using a copy of the model which is stale by 1 iteration, e.g. updating model 2 to produce model 3, but doing so using a gradient update which was calculated using model 1. The reason for this staleness is that while worker 0 is computing its next update, worker 1 updates the model. This staleness is bad for statistical efficiency (i.e. more iterations are required to converge) because now each gradient used to update the model no longer points in the direction of steepest descent for the model it is applied to, but rather the direction of steepest direction for a model from an earlier iteration.
Precisely, we define **staleness** as follows: given N workers, the staleness is the number of updates to the model between a worker’s read from the model and subsequent write back to the model. Because the updates are round-robin, this staleness is the same for all workers, and is equal to \( S = N - 1 \). E.g. if there are 100 parallel workers, \( S = 99 \). Intuitively, the staleness is just equal to the number of parallel workers sending gradient updates (minus one, although this can often be ignored because the number of workers is large).

The three assumptions above are useful to give a precise definition but are not necessary in practice.

**Assumption 1**: In practice the workers do not proceed in round-robin order due to inherent variance across machines, but we observe empirically that for dense models the updates are nearly round-robin. This is because dense model computations like those used in deep learning have roughly constant time per iteration (this is not true for sparse models).

**Assumption 2**: Writes and reads do not need to be atomic, and in fact this can be beneficial for statistical efficiency. Rather than have a conv compute server request an entire updated model as soon as it publishes all of its gradients to the conv model server, it may instead publish gradients layer-by-layer in a backwards fashion during the backward pass of iteration \( i \), and then lazily request the updated model in the forwards pass of the next iteration \( i+1 \). For example, AlexNet may update the model with gradients from conv5, conv4, conv3, conv2, and conv1, and then begin its next forwards pass and request conv1, conv2, conv3, conv4 and conv5. These requests can happen asynchronously from the computation to hide latency and overlap the network delays with the computation. As a result the write/read for conv1 may be almost atomic, but there would be some delay between the write/read for conv5. This delay in fact reduces staleness slightly because it reduces the number of intermediate writes by other workers between a worker’s read and subsequent write (intuitively, in the extreme case, if the delay was very large, then every worker would write before any of them read the new model. Then this is just equal to mini-batch, except with a larger batch size, although that would of course make each iteration slower, i.e. harm hardware efficiency). In practice we observed a roughly 20% reduction in the number of iterations to converge by requesting models in this lazy fashion (which does not harm hardware efficiency).

**Assumption 3**: Staleness also applies to the server architecture of Figure 15 (b), which recall reduces network communication by merging the FC model and FC compute servers, i.e. mapping them to the same machine which does both the gradient computation and model updates for the FC phase. This merged FC server processes only one batch at a time, and thus produces only one FC model gradient at a time. This means that the staleness for the FC model is 0 which is good for statistical efficiency. The conv compute servers on the other hand still calculate the updates to the conv model in parallel (once they receive their data gradients from the FC machine), therefore the merged architecture in Figure 16 (b) still contains staleness, but only for the conv model.

**D.1.3 Compute Groups**

The final concept common to all systems is the **compute group**. Consider the example of two conv compute machines in Figure 18 (a). This configuration has a conv staleness of \( S = 1 \), as there are 2 workers independently updating the model. However, it is not necessary to introduce staleness in order for both compute machines to be utilized, and Figure 18 (b) shows a second configuration in which data parallelism is used across the machines: each conv compute worker processes **half** the data of a single batch, using the same model replica, and produces **half** of the final gradient. A barrier is then introduced in which the gradients are summed, and a single, final gradient is applied to the model. Figure 18 (b) seemingly solves both problems: all the hardware is being utilized (good for hardware efficiency), and \( S = 0 \) (good for statistical efficiency). However the price we pay is in hardware efficiency, specifically the cost of synchronization across the machines. Indeed, we will show that the hardware efficiency of Figure 18 (b) is poorer than that of Figure 18 (a).

We define a compute group as a group of machines working together to process a single batch of data. A compute group is characterized by processing a single data batch at a time, with all machines in the group using the same model replica, and returning a single gradient to the model server. The compute groups in Figure 18 are shown with black dotted lines. Figure 18 (a) has 2 compute groups, and since there are 2 machines, the **compute group size** is 1 machine. Figure 18 (b) has 1 compute group of size 2. Note that this allows us to simplify our definition of staleness: because the number of parallel gradients being computed in the system is equal to the number of compute groups, the **staleness is just equal to the number of compute groups** (minus one).

Generally, if we have \( N \) machines used as conv compute servers, Figures 18 (a) and (b) show two extreme cases. Figure 18 (a) is the extreme case of 1 machine per compute group, and \( N \) groups. This technique is often called **asynchronous SGD**, or “async” for short. In async, workers do not communicate and each worker updates the model independently. Every worker computes a separate gradient using a separate batch and separate model replica, and then sends these gradients to the parameter server in order to update the model. Figure 18 (b) is the other extreme case of
I group, and all N machines in that single compute group. This technique is often called synchronous SGD, or “sync”. In sync, all machines work synchronously and in parallel on a single batch of data and using a single model replica to compute a single gradient. In this case the gradients over all workers are aggregated each iteration (or batch) before updating the model. An intermediate configuration could also exist, for example one which has 4 groups each of size N/4. There could even be groups of different sizes if different machines have different throughput (some GPUs, some CPUs, etc.). Notice that because the compute group in Figure 18 (b) parallelizes the conv phase, it uses data parallelism, i.e. the batch is partitioned across the machines in the group.

D.1.4 Precise Problem Definition

This section has described two key tradeoffs: (1) the server architecture, concerned with physically mapping servers to machines, and (2) the execution strategy (the number of compute groups vs. their size), concerned with mapping batches to servers. We can now restate the goals of the optimizer from 2.4 in terms of our tradeoff space. Given (1) A, the CNN architecture, (2) D, the dataset, and (3) G, the device graph, our optimizer transforms A into S, an abstracted network of logical server types (Conv\textsubscript{model}, Conv\textsubscript{compute}, FC\textsubscript{model}, and FC\textsubscript{compute}), and creates (1) a physical plan P(S, G) mapping each server in S to machines in G (note that we also refer to this distributed portion of the physical plan as the server architecture), and (2) an execution plan E(S, D) which defines the number of compute groups by allocating batches of D to each server in S. Both of these choices impact hardware and statistical efficiency, and our next task is to quantify this impact. First, we present terminology and then finish this section by describing where existing systems fall within this tradeoff space.

Our mapping from CNN layers to devices is shown in Figure 19.

We are given: (1) a network, which can be viewed as a labeled directed acyclic graph in which each node is a type of layer (e.g. convolution, fully connected, max pooling) and edges indicate dataflow dependencies, and (2) a set of devices grouped into machines. Our goal is to devise a mapping from the network to the machines.

D.2 Terminology

In this work we interchangeably use the terms node and machine to refer to a single box, connected to other nodes or machines over a network. We also interchangeably use the terms device and (when describing a device graph) vertex to refer to a discrete unit of compute hardware (e.g. a GPU or CPU core. When discussing a cluster, a device can also be a machine in that cluster.). Finally, we also use the terms group and compute group interchangeably, as defined in Section 2.

Existing work also often contains a lot of terminology, which we summariz here. Consider for these examples the simple case of N identical compute devices (e.g. N machines, N GPUs, N CPU cores, etc.)

D.2.1 Synchronous Batches

These first two definitions apply to a single batch of data, i.e. there are not multiple parallel batches in the system used to compute asynchronous gradients, but rather a single batch used to compute a single gradient. As a result, this gradient is applied to the model at once to produce a new model, i.e. there only ever a single model in the system (although it may be replicated, in which case all models are identical). This is also known as the synchronous case above.

Model Parallelism: A single replica of the model and N replicas of the data batch are created. Each device is given 1/N of the model replica and 1 replica of the data batch. This is useful for parallelizing fully-connected layers, which contain small data but large models: each device receives 1/N of the model and a replica of the data, and uses the data to compute a gradient for that portion of the model. These gradients in total combine to a single gradient with respect to that entire model, using the data batch.

Data Parallelism: A single replica of the data batch and N (identical) replicas of the model are created. Each device is given 1/N of the data replica and 1 replica of the model. The model is replicated and used to compute asynchronous gradients, but rather a single gradient is used to update the model and produce a new model (physically the updates may occur locally on each device communication, i.e. the device updates its portion of the model).

Note that logically, a single gradient is produced by all devices together and that single gradient is used to update the model and produce a new model (physically the updates may occur locally on each device communication, i.e. the device updates its portion of the model).

D.2.2 Asynchronous Batches

The above definitions apply to a single data batch in the system (although it may have been replicated for the purpose of parallelization). Consequently, there was always one gradient being computed at once, and so each model replica was identical.

This definition focuses on the asynchronous case mentioned previously, i.e. N\textsubscript{B} parallel batches in the system being used to compute N\textsubscript{B} parallel gradients. Each of these N\textsubscript{B} batches of data in the system is different. Each batch is
allocated to a compute group (a group of devices), and each batch (i.e., each group of devices) is given a replica of the model. For example if $N_B = N/4$, then there will be 4 devices assigned to each batch, and one model replica assigned to each of these $N/4$ batches (i.e., each group of 4 devices). Each compute group of 4 devices will then compute a gradient given that model and that batch, and the devices in the group may do so using either model or data parallelism (i.e., choosing to create additional model or data replicas within the group, as described above, e.g., if the group uses data parallelism it will create 4 additional model replicas, but each of these models will be identical).

Note that here the number of batches in the system, the number of compute groups, and the number of parallel gradients being computed by the system are all the same number. Within a compute group (group of devices), additional model replicas will be the same. However across compute groups, the model replicas may be out of sync, because of asynchronous gradient computations. This is discussed in the final definition.

To make all the definitions above concrete, consider the example of 2 devices, e.g., 2 GPUs. There are 3 possible scenarios: (a) 2 parallel asynchronous batches (“async”), (b) 1 batch with data parallelism across the 2 devices (“sync”), or (c) 1 batch replicated twice with model parallelism across the 2 devices (also sync).

### D.2.3 Combining Model Replicas

If there are $G$ asynchronous compute groups, each using a separate data batch and producing a separate gradient each iteration, then each group will also have a separate version of the model as a result of the asynchronous gradient computations.

**Parameter server** is a technique in which these separate compute groups will not perform their model updates locally, but rather each publish their gradients to a global parameter server which will then broadcast the updated model to a group upon receiving the update for that group. In this way the groups always have models which are almost the same (they will still be slightly out of sync because gradients are published asynchronously and so models are returned to the groups asynchronously as well). DistBelief, Adam, SINGA, MXNet use this technique, and it is the focus of our study.

Note that if the parameter server waits for each parallel group to publish a gradient and then broadcasts the model to all groups (i.e., introduces a barrier), this is no longer asynchronous, and is now equivalent to the synchronous case above (data parallelism) where the batch size is $N$ times larger than it is per individual compute group.

Finally, the updates to the server from parallel groups can happen with or without race conditions. The case of race conditions is known as Hogwild!.

**Model Averaging** is a technique in which there is also a global parameter server, but model updates happen locally within each group. Then periodically, every $\tau$ iterations, the groups will publish not their gradients but their entire models to the parameter server. The parameter server will average the models (reduce step) and then broadcast them to each group (map step). This averaging does not have theoretical guarantees because neural networks are non-convex, but works in practice. This technique works well for map/reduce frameworks, e.g., Spark/Hadoop, and is used by SparkNet and DL4J. Here the models are more different than they are in the parameter server case.

The choice of the $\tau$ parameter is similar to the tradeoff of multiple groups of varying size, except that here staleness comes not from multiple asynchronous workers updating a single model, but multiple workers with a separate model combining models. In the case where $\tau = 1$, this is identical to the synchronous case of parameter server (all machines in a single group, i.e., all computing a single batch/gradient).

**Ensembles** are used by AlexNet. Here each group trains an entirely separate model to convergence and then predictions of these models are combined (e.g., through voting). The gradients or models themselves are never combined.

In this study we focus on the parameter server approach, which is the most widely used by distributed CNN systems.

### D.3 Existing Systems

Using the terminology above, we discuss design decisions made by CNN systems in Table 2. In our review of the literature, these are the tradeoffs which we identified as most impactful to minimizing convergence time.

| Tool          | sync (g=1) | 1<g<N | async (g=N) | Model Avg. | Merge |
|---------------|-----------|-------|-------------|------------|-------|
| DistBelief    | *         |       |             |            |       |
| Adam          | *         |       |             |            |       |
| FireCaffe [15]|           |       |             |            |       |
| MXNet [5]     | *         |       |             |            |       |
| SINGA [25]    |           |       |             |            |       |
| SparkNet [19] |           |       |             |            |       |
| DL4J          |           |       |             |            |       |

**Table 2: Points in the distributed CNN tradeoff space chosen by popular systems. g is the number of compute groups, N is the number of machines.**
SparkNet [19] and DL4J [http://deeplearning4j.org/]. Model averaging is also described above. The key difference between model averaging and parameter server is the way in which model replicas are combined.

**Physical Map, Modern Networks.** The second point in the distributed tradeoff space is the server architecture (how servers map to hardware), specifically whether the FC compute and FC model servers are mapped to the same physical machine (or machines, for multi-machine model parallelism).

This is a technique introduced by Microsoft’s Project Adam [7] to avoid communicating the large FC model and its gradient. The method was reported for older networks with large, fully-connected layers (AlexNet, VGG), however it also is useful for modern networks (Inception, ResNets). In traditional networks, the fully-connected layers contained the majority of the model parameters [17] (> 90%). Newer networks instead use average pooling and have only a single FC layer (for softmax regression) [14]. Therefore newer networks contain fewer parameters in the FC phase, and fewer parameters overall, however this single FC layer can still be very large (e.g. when predicting among 22,000 classes on ImageNet 22k) and still benefits from reduced FC communication (because the number of FC weights will always be less than the number of inputs to the FC phase). Therefore while newer networks contain only a single FC layer, the merged FC optimization of Project Adam is still relevant, and while a characteristic of newer networks is that their overall model size is smaller due to the elimination of multiple FC layers, ultimately this does not translate to reduced communication overall because the cost of communicating the FC layers has been eliminated in prior work.

In addition, as we show, the benefit of merging the FC servers is not only improving HE due to reduced network communication, as [7] noted, but also improving SE because staleness in the FC model is eliminated (i.e. the device or devices which compute the FC model gradient updates also store that subset of the model). Moreover there is no consequence of merging the FC servers for small FC models because little computation in the FC phase means it is less likely for the FC to saturate (become the bottleneck), but merging still provides the benefit of (1) improving SE, (2) reducing communication and (3) offloading computation to the parameter server machines.

As our goal is to be a complete study, we study both cases (many large FC layers, few small FC layers) in order to build a system which is robust to any application. For example future CNN architectures may employ multiple FC layers again to support transfer learning tasks, or may need to predict among many object classes (e.g. hundreds of thousands or millions), further increasing the communication bottleneck for the FC. In addition, FC layers are also used for RNNs and other architectures.

This is the subset of the tradeoff which we study in this work, summarized in Table 2. Our goal is to find best point in the tradeoff space given the model, data, and hardware specifications from the user. Specifically we do not change the neural network architecture, but assume that this model is given to us. I.e. we do not focus on machine learning algorithms or techniques in this work, but rather study systems tradeoffs which exist for the most widely used networks/algorithms. We focus on the SGD algorithm for learning, as it has been and continues to be used along with momentum by annual ImageNet winners [13,17]. Other algorithms exist for training deep learning models and can also be parallelized, for example Google’s deep learning system uses Adagrad [8]. Microsoft on the other hand uses SGD [7]. Because the systems tradeoffs we study in this work are orthogonal to the choice of update algorithm, in this work we focus on SGD, although the same tradeoff applies to other algorithms as well.

**D.4 Hardware Efficiency Model**

The goal of this section is to create a predictive model for how the hardware efficiency (HE) varies with the amount of staleness $S$ in the system, given a fixed number of machines and batch size. Recall that the staleness $S$ is equal to the number of compute groups (minus one). This is because a compute group is characterized by processing a unique data batch and returning a unique gradient to the model server, so the number of parallel gradients being computed is equal to the number of compute groups. $S = 0$ is the case of 1 compute group, also called the synchronous case.

Figure 20 shows a plot of staleness vs. hardware efficiency penalty for three datasets. The standard networks from Caffe’s tutorials are used for each dataset. The hardware efficiency penalty, or $P_{HE}$, is defined as the ratio of the time per iteration relative to the time per iteration for this synchronous case,

$$P_{HE}(S) = \frac{HE(S)}{HE(0)}$$

A higher $P_{HE}$ is worse (more time per iteration). $P_{HE}$ decreases (iterations become faster) as the number of compute groups increases. This is because, if we fix the number of machines to be $N$, the smallest time per iteration occurs when there is no synchronization, i.e. when the compute group size is 1 and there are $N$ compute groups (asynchronous case). In this case $S = N - 1$. As the compute group sizes increase, and hence the number of groups decreases (because the number of machines is fixed to $N$), $P_{HE}$ will increase due to synchronization delays within the groups. When the number of compute groups is 1, that group contains all $N$ machines and requires the most synchronization. In this case $S = 0$, and this has the highest penalty $P_{HE}$.

The hardware efficiency penalty is dimensionless. It is the ratio of hardware efficiencies (time per iter / time per iter). Because $P_{HE}$ is normalized to the synchronous ($S = 0$) case, $P_{HE} \leq 1$. Note also that the hardware efficiency penalty is only comparable across different staleness values if the number of machines is fixed.
The hardware efficiency penalty can be predicted analytically. However, as we will see in a later section, the cold-start phase of the optimizer performs a short adaptive grid search across different staleness values. Because a few iterations are run for various staleness values, the execution time for these iterations can be used to provide a precise hardware efficiency model (deep learning layer computations are dense, not sparse, so there is little variation in iteration time). Nevertheless understanding the hardware efficiency precisely is important:

1. to understand the execution bottlenecks and either hard-code or allow the optimizer to make physical mapping choices
2. because it may be too time-consuming to obtain static information for every staleness value of interest, and
3. because our work is a study meant to inform future systems which may not use a static optimizer

Figure 20 was run on 33 EC2 CPU machines. The server architecture shown in Figure 18 was used, i.e. one machine contains the merged FC compute and FC model servers, and the other 32 machines contain Conv Compute servers. The Conv Model server is mapped to one of the Conv Compute machines. We make two observations, which are true for all datasets in Figure 20.

Observation 1: As the number of groups decreases (and hence as their sizes increases), the hardware efficiency becomes poorer. There are two reasons for this: (1) machine variance, which causes synchronization delays, and (2) network congestion, because the convolution model needs to be sent simultaneously to all machines in the group (and gradients need to be send back simultaneously). Our analysis below shows that while machine variance exists, it is insignificant compared to increased network congestion.

Observation 2: As the number of groups increases, the speedup is not linear (it saturates). This is because the FC phase processes only a single batch at once, or equivalently because the FC compute and FC model server map to the same physical machine (or machines, as the FC compute / model server may use multi-machine model parallelism). Recall that this has benefits for both hardware efficiency (by reducing network communication) and statistical efficiency (by reducing the staleness of the FC model). However it means that only one gradient computation (batch) is processed by the FC at a time, and so it may become a computational bottleneck.

Many optimizations exist for both of these observations. They are presented after our derivation of the model.

D.4.1 Full Derivation of Analytic Model

Formally, let there be $N + 1$ machines. 1 machine is allocated to the FC phase, and $N$ machines (e.g. 32) to the conv phase. An execution strategy partitions the $N$ conv machines into $g$ compute groups. Each group contains $k$ machines, and the $k$ machines in a group compute the conv phase with data-parallelism. Therefore, there will be $g = N/k$ compute groups sharing the single FC server machine. In addition, let $t_{conv}(k)$ be a function that returns the time that a group of size $k$ needs to compute the convolution phase (forwards and backwards for only the conv phase), and $t_{fc}$ be the time that an FC server needs to serve one group (forwards and backwards for only the FC phase). Note that $t_{fc}$ is independent of $k$, the number of machines used to perform convolution on each batch). We also define that $t_{fc}$ includes the network time to transfer the data from the conv phase to the fc phase and the data gradients from the fc phase back to the conv phase, although we observe that this network time is often small compared to the computation time of $t_{fc}$. Note that $t_{fc}$ is independent of $k$, the number of machines used to perform convolution on each batch. Finally, assume for now as we did above that different groups (batches) cannot be executed in parallel on the FC server (that case is described later).

Given $k$, $g$, $t_{conv}(k)$ and $t_{fc}$, our goal is to create a hardware efficiency model which predicts the time per iteration or, equivalently, which given a time interval $T$ predicts how many batches will be processed by the system. Because each batch must be processed by the FC server, this is equivalent to determining the number of requests that the FC server can process from the $g$ convolution groups in time $T$. There are two cases, also illustrated in Figure 21.

Case 1: Saturated FC Server The first case is when FC server is saturated, i.e. it starts to serve the next request immediately after the previous request finishes. In this case, the hardware efficiency is straightforward. The server will serve $T/t_{fc}$ requests in time $T$, or equivalently.

Time per iteration_{saturated fc} = t_{fc}

Case 2: Saturated Conv Server When the FC Server is not saturated, each conv server becomes the bottleneck. In this case, the FC server serves $Tg/(t_{conv}(k)+t_{fc})$ requests in time $T$, or equivalently,

Time per iteration_{saturated conv} = (t_{conv}(k) + t_{fc})/g

which is the total time for a single iteration divided by the number of parallel groups. This is because the groups all are computed in parallel, with the exception of the FC server which is serial, but the FC server is never saturated so it can also be seen as being part of each parallel group. Refer
to Figure 21 for an illustration of this case. To understand this case, note that:

1. When each conv server is fast ($t_{\text{conv}}(k)$ is small), the FC server serves more requests in time $T$
2. When the FC server is fast ($t_{\text{fc}}$ is small), the FC server serves more requests in time $T$
3. When the number of concurrent group is large ($g$ is large), the FC server serves more requests in time $T$

**Determining Saturation** Finally, the model needs to predict when the FC server will saturate. This occurs at the boundary of the times above, specifically the FC server saturates (case 1) when:

$$t_{\text{conv}}(k) + t_{\text{fc}} > g t_{\text{fc}}$$

Intuitively, if the combined FC time to process all groups ($gt_{\text{fc}}$) exceeds the time for a single group’s iteration ($t_{\text{conv}}(k) + t_{\text{fc}}$), then the FC server will always be saturated. Note that:

1. When each conv server is fast ($t_{\text{conv}}(k)$ is small), it is easier to saturate the FC server
2. When the FC server is fast ($t_{\text{fc}}$ is small), it is harder to saturate the FC server.
3. When the number of concurrent group is large ($g$ is large), it is easier to saturate the FC server.

We now have an expression for the time per iteration in both cases as well as a condition to decide which case applies. Given the following:

- Two of: $N$, $g$ or $k$ (the third can be calculated from the other 2),
- $t_{\text{conv}}(k)$, the time to complete the convolution portion of the network (forwards and backwards) given the group size, and
- $t_{\text{fc}}$, the time to complete forwards and backwards on the FC phase,

the model can predict the mode of saturation and therefore the time per iteration.

$t_{\text{conv}}(k)$ can be calculated given the throughput of each node and the network speed. It has two components:

$t_{\text{conv,compute}}(k)$ and $t_{\text{conv,network}}(k)$.

Let us define:

$t_{\text{conv,compute}}(1) = T_{c,c}$, i.e. $T_{c,c}$ is the time it takes for a single machine ($k = 1$) to compute the forward and backward pass of the convolution phase. Similarly, let us define:

$t_{\text{conv,network}}(1) = T_{n,c}$, i.e. $T_{n,c}$ is the time needed for a single copy of all the conv phase’s models (forwards pass) and model gradients (backwards pass) to be passed over the network. We will describe how to determine these two quantities later.

The computation time for the convolution phase for $k > 1$ is then:

$t_{\text{conv,compute}}(k) = T_{c,c}/k$, because recall that a single compute group performs computation on a single batch of data (data parallelism), i.e. the amount of data per group is always the same per iteration (e.g. $b$ images) and so if there are $k$ machines in a group, each will process $b/k$ images. We assume a linear speedup.

On the other hand, the time for the network communication increases with $k$. This is because of increased network communication from the conv model server, i.e. the model needs to be sent to $k$ workers simultaneously and gradients will be received from $k$ workers simultaneously (all requests are made at almost the same time, because the workers in the group are synchronous). The network time for the convolution phase for $k > 1$ is then:

$t_{\text{conv,network}}(k) = T_{n,c} * k$.

Here, we assume a linear slowdown.

So while the compute time decreases with $k$, the network time increases with $k$. We assume that both of these are linear. Empirically we notice that the convolution computation does not scale exactly linearly with $k$: on 8 c4.4xlarge machines in a single group, the forward pass of the convolution becomes $7.2 \times$ faster and the backwards pass $6.6 \times$ faster. Similarly, we observe that the network slowdown is usually linear but can be super-linear, which we attribute to thrashing.

Given $t_{\text{conv,compute}}(k)$ and $t_{\text{conv,network}}(k)$, we can naively approximate:

$$t_{\text{conv}}(k) = t_{\text{conv,compute}}(k) + t_{\text{conv,network}}(k)$$

However, these two can be done in parallel, i.e. while one layer is computing its forwards pass, the model for the next layer is being sent over the network. This does not entirely overlap because the first layer needs to complete its backwards pass before requesting the model for its next forwards pass, but we can approximate the total convolution phase time as:

$$t_{\text{conv}}(k) = \max(t_{\text{conv,compute}}(k), t_{\text{conv,network}}(k))$$

Finally, it is necessary to obtain $T_{c,c}$, $T_{n,c}$ and $t_{\text{fc}}$. We measured these because they only need to be measured once (not for each $k$), but they can be calculated using the node throughput and network throughput: $T_{c,c}$ and $t_{\text{fc}}$ can be approximated by counting the total number of operation from each GEMM operation in the conv and fc phases and assuming that BLAS achieves the device peak. $T_{n,c}$ can be approximated by counting the total number of bytes in the conv models and assuming the peak network throughput is achieved. These assumptions are justified because the matrices and models are large.

Also note that measurements of these quantities are accurate for all iterations because deep learning computations are dense and so there is little variation in the computation time across iterations, as shown in Figure 22. Note that there is a standard deviation of than 6% for $t_{\text{conv}}(1)$ and $t_{\text{fc}}$, and a standard deviation of 8% for the total iteration time. For CIFAR-10, the standard deviation for total iteration time was 1.5%. We also observed similar variances on a GPU cluster.
Using measurements of $T_{c,c}$, $T_{n,c}$ and $t_{fc}$. Figure 9 shows that the analytic model of hardware efficiency is accurate. When the FC server is saturated (right side of the graph), the model is almost exact. When the FC server is not saturated (left side of the graph), the slowdown and speedups are not exactly linear, and we underestimate the time per iteration.

While this analytic model may seem specific to CNNs, it extends to any deep learning model because its derivation relies only on queuing theory, not any specific properties of CNNs.

### D.4.2 Further Optimizations

A primary goal for understanding the hardware efficiency above is to determine possible optimizations.

**Saturated Conv Server.** We showed above that as the group size ($k$) increases, there is no longer FC saturation, because

$$t_{conv}(k) + t_{fc} > gt_{fc}$$

and recall

$$t_{conv}(k) = \max(t_{conv, compute}(k), t_{conv, network}(k))$$

Specifically, in Figure 9 the case of a single group (left side of the graph) is so much slower than FC saturation (right side of the graph) because $t_{conv, network}$ becomes very large, i.e. the time it takes to send the conv model to all 32 machines in the group is significantly greater than the computation time, which is small due to data parallelism across 32 machines.

In particular, note that a single, large group is slower than many small groups not because of synchronization delays due to machine variance exists, but because of increased network congestion, although some variance does exist in the computation time across machines.

Microsoft’s Adam [7] discusses techniques to mitigate both of these problems, from not requiring each worker in a group to finish processing all of its images to adding multiple NIC cards on the parameter server machines. FireCaffe [15] uses the technique of reduction trees for their parameter server machines. FireCaffe, or mapping 4 FC Compute servers to a machine that contains 4 GPUs, etc. Another example is merging the FC compute and FC model server and mapping them to the same physical hardware as in Figure 16(b), but where that hardware is not a single machine as shown in Figure 16(b) but multiple machines e.g. using model parallelism.

Finally, a common technique is to "pipeline" the servers by mapping multiple conv compute servers to the same physical machine. For instance in the synchronous case (1 group of $N$ machines), during the FC computation all $N$ machines are idle (because they are waiting for the FC to return data gradients before they can begin the backwards pass of the conv phase). During this idle time those machines can be processing a different batch, i.e. $N = 32$, but there are two groups of size 32. Note that in this example, this pipelining increases staleness from 0 to 1. Using this pipelining, the time per iteration in conv saturation becomes:

$$\text{Time per iteration}_{\text{saturated conv}} = \frac{t_{conv}(k)}{g}$$

i.e. the FC time is completely hidden.

### D.5 Statistical Efficiency Model

Because asynchrony can be viewed as increasing implicit momentum, asynchrony can be made equivalent to synchronous execution by properly reducing the explicit momentum in order for the total explicit + implicit momentum to stay the same as the optimal momentum of the synchronous case. This is true as long as the implicit momentum is less than the optimal momentum of the synchronous case. This is a key discovery because it means that staleness can exist in the system without incurring a statistical penalty, which is advantageous for hardware efficiency. Also, making the momentum stay the same (rather than just ignoring this result and letting there be extra momentum) is important because a total momentum that is too high will diverge, which we show experimentally in Appendix E. This theory also successfully predicts measured
E. APPENDIX FOR DISTRIBUTED OPTIMIZER (SECTION 5)

This section describes how to use the models from the previous two sections to choose (1) a physical mapping which maps each server to a machine, and (2) an execution strategy which defines the number of compute groups by allocating data batches to each server. As in previous sections we assume that the number of machines are fixed.

E.1 Selecting the Batch Size

We first study the batch size in Figure 23 which uses the imagenet-8 dataset with $S = 0$ and momentum $\mu = 0.9$. The x axis varies the batch size and the y axis plots the # passes over the dataset (or epochs) until convergence. For each batch size we used an oracle to find the optimal learning rate, $\eta^*$, i.e., $\eta > \eta^*$ diverged.

We see that as long as $\eta^*$ increases with the batch size, there is little penalty for larger batch sizes. This is because larger batch sizes provide a truer gradient each iteration and permit a larger $\eta$ before divergence, therefore while a larger batch consumes more of the dataset, the progress made by each step is greater. $\eta^*$ cannot scale infinitely however, and plateaus beyond $\eta^* = 0.0032$. As a result, larger batch sizes make no more progress per iteration than smaller batch sizes, but consume much more of the dataset each iteration. This is catastrophic for performance (it can take $30\times$ more epochs to converge) as computation is effectively “wasted”, which is why neural networks have been trained with SGD rather than batch gradient descent since the early days. This also greatly exceeds the staleness cost incurred of “splitting” a large batch into smaller, asynchronous batches (which we show is nearly flat), which is why asynchrony is necessary for systems to scale to very large clusters.

This suggests that the optimizer needs to tune batch size, however for imagenet-8 and other datasets we observe that this performance penalty is negligible around 256 (specifically we use 256 for Imagenet, 128 for CIFAR-10 and 64 for MNIST, based on published results for these datasets). In principle the optimizer could tune $b$ as well, but we observe that unless $b$ is too large the penalty is small so we dont study this in more detail.

E.2 Physical Mapping

As discussed in the text, for the physical map which maps servers to machines, we map the FC compute and model servers to the same machine (i.e., “merge” the FC servers, which as [2] argues reduces communication overhead because it avoids communicating the large FC model) and use one compute group for the FC phase. The rest of the machines are used for the conv compute servers. The conv model servers are mapped to one of the conv compute machines.

Empirically we show in Appendix F.3 that this mapping is best for both hardware and statistical efficiency: on a cluster of 33 EC2 c4.4xlarge machines, not merging the FC servers incurs an additional hardware efficiency penalty of $1.2\times$ due to increased communication as well as a statistical efficiency penalty of $2.5\times$ because of staleness in the FC model. We describe this result further in the experimental results of Appendix F.3. Our current optimizer therefore always chooses this server architecture, although Appendix D.5 (for Section 4.1) described other architectures scenarios in which these penalties are justified to eliminate FC saturation, as well as additional optimizations within this server architecture (such as reduction trees or multi-machine model parallelism for the FC phase).

E.3 Optimizer Details

For each epoch, Algorithm 1 performs an adaptive grid search over both the learning rate and the momentum starting at the current value of $g$. Specifically, we run each learning rate and momentum (see below) for one minute and select the configuration with lowest loss after 1 minute of execution. If after 1 minute all these configurations have the same loss, we continue to run another minute until there is a clear winner in terms of loss (we determine this using a threshold of 5% from the loss of the past 50 iterations, although a statistical test can be used as well). We then run this best $(\mu^*, \eta^*)$ for an hour and then rerun the optimizer.

One could use more sophisticated parameter search routines, but this took less than 10% of the execution time.

We search the learning rate as follows. Let the learning rate be $\eta$ at the current value of $g$. Specifically, we run each learning rate and momentum (see below) for one minute and select the configuration with lowest loss after 1 minute of execution. If after 1 minute all these configurations have the same loss, we continue to run another minute until there is a clear winner in terms of loss (we determine this using a threshold of 5% from the loss of the past 50 iterations, although a statistical test can be used as well). We then run this best $(\mu^*, \eta^*)$ for an hour and then rerun the optimizer.

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One could use more sophisticated parameter search routines, but this took less than 10% of the execution time.

E.3.1 Empirical Validation
The optimizer will "short-circuit" Algorithm 1 to begin at through measurements during the cold start phase), the op- instead of (c) their product, which by equation (1) is the total time to ℓ sync (the AlexNet CNN. We run each execution strategy from experimentally. We use a cluster of 33 EC2 CPU machines (CPU-L in Figure 2), the Imagenet 1000-class dataset, and the AlexNet CNN. We run each execution strategy from sync (g = 1 conv compute group) to async (g = 32), each for a single epoch (1 hour). Specifically, we plot 6 strategies: g = {1, 2, 4, 8, 16, 32}, where the number of conv compute machines is fixed to 32. Each strategy starts from the same checkpoint (i.e. same loss), but achieves a different final loss by the end of the epoch. We select the lowest final training loss achieved by all strategies, ℓ F, and plot three measures in Figure 7: (a) the time per iteration (hardware efficiency, HE), (b) the number of iterations to reach ℓ F (statistical efficiency, SE), and (c) their product, which by equation (1) is the total time to reach ℓ F. For completeness, each strategy uses an oracle to exhaustively find its optimal explicit momentum, µ∗ (within 0.3) and optimal learning rate η∗ (within an order of magnitude. For all strategies η∗ = 0.01 was optimal). The HE curve in (a) is the same as in Figure 5 (b).

We see in (c) that g = 32 (fully asynchronous) is 4× faster to reach ℓ F than g = 1 (synchronous). This is due to its faster iteration time (HE) in (a), although it requires 1.8× more iterations (SE) to reach ℓ F in (b). This matches the theory’s prediction: increasing g decreases the explicit momentum µ∗, which falls to 0 at g = 32, and consequently there is a penalty in SE. The optimizer of Algorithm 1 would therefore select g = 16, which is near-optimal.

However, our optimizer additionally employs an optimization to leverage the HE model from Section 4.1.1 because the FC server saturates at g = 4 (determined analytically or through measurements during the cold start phase), the opt- imizer will “short-circuit” Algorithm 1 to begin at g = 4 instead of g = 32, and ends up selecting g = 4, which is 5× faster than sync.

Figure 24 shows the accuracy vs. time (and for reference accuracy vs. iter, i.e. statistical efficiency) for each config- uration (# groups) in Figure 7. Recall that the optimizer selected 4 groups because with proper momentum tuning the statistical efficiency was nearly the same for all curves, but 4 or more groups had the best hardware efficiency. Fig- ures 7 and 24 use ImageNet 1000 class (1 hour of training) as described above with 33 EC2 c4.4xlarge machines.

### E.4 Cold Start Phase

The model is trained synchronously before beginning asynchronous execution in Algorithm 1. This is needed in order to set the appropriate scale for the weights. However fully synchronous execution may be slow, and just as an optimization to Algorithm 1 was to run asynchronously only up to FC saturation, similarly this section focuses on acceler- ating training during the cold-start phase. In particular, a fully synchronous execution may significantly increase the duration of the cold-start phase due to poor hardware effi- ciency, and so a cold-start run with slight asynchrony may more quickly terminate the cold start phase. Therefore, tuning the number of compute groups is also important for the cold-start phase.

**Cold Start Grid Search.** To do this, as in Algorithm 1, we grid search hyper-parameters for each number of groups (1, 2, 4, . . . , N, for N machines). For each we also grid search learning rate and momentum. We use a standard adaptive grid search algorithm for its simplicity. For each staleness, the algorithm searches for optimal settings of momentum and learning rate by running each configuration of parameters for 1 minute, and selecting the parameters with the lowest loss after 1 minute.

The search happens as follows, and is similar to the search in the steady-state execution of Algorithm 1. We start with S = 0, fix the momentum to 0.9, and run 1 minute for each learning rate η ∈ {0.1, 0.01, 0.001, 0.0001, 0.00001}. We search from lowest to highest and stop early if a learning rate produces a final loss worse than the previous learning rate (or if a learning rate causes divergence). We select the learning rate which has the lowest loss after 1 minute. Call this η∗ sync. Therefore for S = 0, the optimal configuration (µ∗, η∗) = (0.9, η∗ sync). We do not tune momentum for sync because 0.9 is standard [17], because this saves optimizer time, and because there is no implicitly induced momentum due to asynchrony for S = 0.

For the remaining S after S = 0, we perform the following iteration: We increase the number of groups to the next highest power of 2 (after sync, this is g = 2, then g = 4, g = 8, etc, i.e. S = 1, 3, 7, . . . ) Let the optimal configuration from the previous S be (µ∗ last, η∗ last). For the current S, we run a grid search for (µ, η)µ ∈ {0.0, 0.3, 0.6, 0.9}, η ∈ {η∗ last, η∗ last/10}. I.e., η∗ last defines the search range for the next S. In addition, µ∗ last reduces the search space for the next S: we do not search a higher momentum than µ∗ last while searching η = η∗ last.

We notice empirically that there is not a large impact of running a finer grid for momentum (although this can be done by adding a second-phase of search which fixes η∗ and searches µ around µ∗). Running multiple random seeds (net- work weight initializations) can also be used to find a good starting point for the SGD algorithm (this is a known tech- nique). Tuning parameters is not a novel idea in machine learning, but unlike existing work our problem is more so- phisticated as we are coupling tuning hyper-parameters and execution strategies (staleness). Our work is the first to show that hyper-parameters and execution strategies need to be tuned jointly to avoid divergence as staleness increases.

Once we obtain (µ∗, η∗) for each S, we then run each S for one minute at a time until there is a clear winner in terms of loss (we determine this using a threshold of 5% from the loss of the past 50 iterations, although a statistical test can be used as well). We then run this best S with its (µ∗, η∗) for an hour (the cold-start period).
**Parameter Search Experiments.** The remainder of this section describes experiments motivating the pruning above, in particular why a larger staleness does not need to try larger learning rates or larger momentum values at the same learning rate. There are a number of insights which allow us to prune the search space for the cold-start phase and reduce the total search time. We discovered that as staleness increases, the optimal learning rate and momentum parameters when \( S = 0 \) cause divergence (loss goes to infinity) for larger staleness values, e.g. \( S = 31 \). This makes sense given our theoretical foundation from the steady-state optimizer: staleness induces implicit momentum, hence if explicit momentum is not decreased as \( S \) increases, total momentum can be \( > 1 \) and cause divergence. As \( S \) increases, we note that one or both of \( \eta \) and \( \mu \) need to be reduced otherwise SGD will diverge (loss goes to infinity).

Table 3 shows the optimal parameters for the same datasets and networks used in Figure 20 at different staleness values. Here the optimal parameter settings with which the training converges in seconds, and therefore Algorithm 1 could be run part-way during execution to select a better strategy for the remainder of the execution (e.g. asynchronous), the overhead of re-running Algorithm 1 is not justified for these small datasets, i.e. it is faster to treat the entire run as the cold-start phase. Therefore we use these smaller datasets to study the cold-start phase.

The table shows that, with a fixed batch size, as staleness increases the optimal momentum and/or learning rate decreases, and in some cases not decreasing these parameters and using the parameters for \( S = 0 \) causes divergence. Also, we see that decreasing the learning rate means momentum can increase again. Intuitively this is because momentum can be viewed as increasing the learning rate (larger SGD steps), and so if the learning rate is decreased too much, momentum increases to compensate for this decrease. Our grid search searches orders of magnitude for the learning rate, following from previous work [17], but decreasing the learning rate by a smaller factor may avoid the need for momentum to increase and provide faster overall convergence. We leave this exploration to future work.

| Dataset (Network) | Staleness | Optimal Momentum | Optimal Learning Rate |
|-------------------|-----------|------------------|-----------------------|
| MNIST (LeNet)     | 0         | 0.6              | 0.1                   |
|                   | 31        | 0.0              | 0.1                   |
|                   | 127       | 0.8              | 0.01                  |
| CIFAR-10 (Krizhevsky) | 0   | 0.9              | 0.001                 |
|                   | 31        | 0.7              | 0.0001                |
|                   | 127       | 0.1              | 0.0001                |
| ImageNet-8 (CaffeNet) | 0 | 0.6              | 0.01                  |
|                   | 31        | 0.0              | 0.01                  |

### F. APPENDIX FOR DISTRIBUTED EXPERIMENTS (SECTION 6)

#### F.1 Single-Node Experiments

See Appendix C.5.

#### F.2 Small Cluster Experiments

This section provides additional details of the experimental setup. For the end-to-end experiment on ImageNet 1000, see Appendix F.5.

We ran all systems with a timeout of 2 hours. For each system we used the same CPU and GPU external libraries as discussed in Appendix C.5.

We further sped up other tools by applying our optimizer to the extent that no code change was required. MXNet offers both the sync and async strategy. Given our observation that async requires tuning parameters, to ensure training did not diverge we ran each strategy of MXNet with 4 orders of magnitude of the learning rate for 10 minutes each. We then selected the best strategy (as the static optimizer would) and ran it until convergence or timeout. For SINGA we followed the same procedure and tried all available configurations. SINGA supports not only sync (1 group) and async (1 machine per group) strategies, but also intermediate group sizes. We ran SINGA with 1, 2, 4, and 8 machines per group, and also 4 orders of magnitude for the learning rate \( \eta \) in each case. All runs were also for 10 minutes, and then as with MXNet the best one was run to convergence.

For Omnivore we ran our optimizer, which merged the FC compute and model servers to one machine and used the other 8 machines as conv compute machines. As with SINGA, the optimizer searched statically among 1, 2, 4, and 8 machines per group, but for 1 minute per execution setting. Overall the optimizer ran for less time than the tuning we did to ensure no divergence for MXNet and SINGA.

We followed the tutorials for each system and also ensured that all three systems used identical networks and parameters, including weight initializations and data preprocessing.

The network we use is CaffeNet, which is Caffe’s version of Alexnet\(^{21}\). AlexNet is the standard network for ImageNet and Caffe is the most widely used CNN framework, so this ensures reproducibility. The weight initializations, batch size, regularizations, and other hyperparameters are the same as CaffeNet, with a few minor differences:

Unlike Caffe and SINGA, MXNet does not easily support learning rate and weight decay multipliers, or different initializations for each model and bias. For consistency across tools, we therefore just made all 3 tools use the same weight initialization scheme, which is Gaussian with mean 0 and standard deviation 0.01, and no multipliers.

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\(^{21}\)https://github.com/BVLC/caffe/blob/master/models/bvlc_reference_caffenet
MXNet and SINGA do not support the grouping in AlexNet (which was done in 2012 to save GPU memory), so this is disabled from CaffeNet (and also is not important anymore as GPUs have more memory)

No random data preprocessing was used (crop, mirror), and we show convergence on the training set, not a test or validation set. We do this because these are machine learning concerns/optimizations and our focus is the system.

We do subtract the image mean to avoid divergence.

Similarly, we disable the learning rate schedule in all tools and use a constant learning rate. We do this because we only train on a subset of ImageNet and to reduce the search space of the parameter configurations.

The following subsections describe in detail the individual settings used for each system to ensure fairness in our comparison.

### F.2.1 Detailed Settings for Both Systems

For both systems we built in a wall-clock timer to ensure accurate timing. We created and shuffled the dataset using the tools provided by the systems: MXNet required shuffling beforehand, SINGA provided an im2rec utility. Those tools also were used to calculate the image mean: MXNet automatically generated the mean file when it ran and SINGA as part of im2rec. Because we focus on the training set we removed any validation set from the tools to ensure no time was spent on that. We used the provided AlexNet examples for each system and changed them only as above to ensure identical settings across all three systems (e.g. weight initializations, L2 regularization, etc.) Accuracy was reported instead of loss for all tools to ensure consistency. The MXNet examples do not report loss so we used their accuracy eval metric. Moreover MXNet’s acc metric is by default on the entire epoch while SINGA’s is since last time printing, so we averaged the logs to ensure consistency across all three tools.

### F.2.2 Detailed MXNET Settings and Results

We removed all machine learning optimizations from both tools except those described above. For MXNet this meant removing gradient clipping. Because we ensure the parameters are used for all tools, including the batch size (256 for CaffeNet), this meant that for MXNet’s dist_sync strategy on 8 machines, a batch size of 32 was used, and for 32 machines, a batch size of 8 was used (other tools partition the batch size for the sync strategy, i.e. they partition b images by sending b/N to each sync worker, but MXNet uses that batch per worker, i.e. they use a batch size of b × N). We fixed the random seed to 1 so the initialization is always the same.

We created a single data file and ensured that each worker read it from different location (using ImageRecordIter as in the AlexNet example). The timer was added as modified version of the stopclock callback (using time.time(), which is wall-clock time in python).

We used a cluster of 9 machines in these experiments because MXNet’s AWS documentation instructs to “Prepare a host file with all slaves private IPs”. Therefore in order to test parallelism across 8 machines, we opened 9 EC2 machines, ran MXNet from the master (root) machine, and placed the other 8 machines in the hosts file.

On the cluster of 9 c4.4xlarge machines we ran the 4 orders of magnitude learning rate for each execution strategy and noticed after 10 minutes that the best was learning rate 0.01 and sync, so we ran until 99% convergence. We needed 4 orders of magnitude to ensure that the optimal setting was never on the “boundary” of the interval, i.e. the optimal η we report was superior to an order of magnitude higher η and lower η. For async no parameter setting had high accuracy after 10 minutes: The best sync was 60% in 10 min and the best async got to 20% in 10 min, in spite of better hardware efficiency for async (72 s per epoch async, 120 s per epoch sync). The best async was with learning rate 0.0001.

On the cluster of 9 g2.8xlarge machines (again following MXNet’s documentation, 1 parameter server machine and 8 compute machines), we tried both cuDNN v3 and v4 and found no speed difference. Again we searched learning rate and found that 0.01, sync was best.

On the c4.4xlarge machines we used all the cores, and on the g2.8xlarge machines that all 4 GPUs on each worker were utilized (using nvidia-smi).

### F.2.3 Detailed SINGA Settings and Results

For SINGA, the timer built into TrainOneBatch. It also uses wall-clock time (clock_gettime, same as Omnivore). Again we use the default AlexNet example with only small changes to make all weight initializations the same (as in MXNet), and to remove learning rate / weight decay multipliers (since not supported easily in MXNet).

Tuning parallelism across groups: we tried tuning partition_dim for each layer. Specifically we first used the default, i.e. partition_dim commented out (as in their AlexNet example). We then uncommented those recommended partition_dim settings in the example (i.e. dim 0 or batch parallelism for convolution, and dim 1 or model parallelism for FC) and found no difference, so we left partition_dim commented out as in the default AlexNet SINGA example.

Tuning parallelism across groups: To ensure different data for each worker we tried specifying a random_skip in the data section but this made no difference. Documentation v0.1.0 suggested using random_skip but in v0.2.0 (which we used) it was deprecated, so as with partition_dim we left this out and used the default AlexNet SINGA example settings.

Next, we had to select for each machine number of workers per process. For each machine, we tried 1 process of 8, 16, and 32 threads on a single machine. The number of physical cores is 8 on the c4.4xlarge, and virtual cores is 16 (nproc = 16). 16 was fastest so we used 16 workers per process.

As with MXNet we followed the documentation for SINGA and also included 8 machines in the hostfile. We ran 4 orders of magnitude for the learning rate as described above and found that 0.0001 and 4 groups of 2 machines each was best after 10 minutes. The result was noisy however, and looked similar to the distributed results in the “SINGA: Putting Deep Learning in the Hands of Multimedia Users” paper. We then ran the best configuration for but it did not converge in 3 hours (got to 70-80%).

SINGA GPU distributed did not work at the time of this study so it is not included.

### F.2.4 Detailed Omnivore Settings and Results

Omnivore was run using the same network and parameters as the systems above. The optimizer was run as described above in Appendix E. Each configuration was searched by
the optimizer for 1 minute and search time was reduced by pruning the space across staleness values. The second search phase was skipped (momentum granularity was 0.3). We fixed the random seed to 1 so the initialization is always the same. The overall optimizer time was less than the search time to avoid divergence in other tools.

On the CPU cluster, the strategy chosen was the same as with MXNet, i.e. sync with $\eta = 0.01$. Momentum is untuned for both Omnivore and MXNet, i.e. 0.9, because our contribution is tuning momentum to compensate for staleness and sync has no staleness. Since the parameters and staleness are the same as MXNet, as expected Omnivore achieves the same statistical efficiency. However, it is $2.3 \times$ faster in terms of hardware efficiency, for an overall end-to-end convergence speedup of $2.3 \times$. On the GPU cluster, the optimizer chose 2 groups of 4 m/g, and was $5.0 \times$ faster to converge. The following section studies the benefits of the optimizer in more detail, and also examines how the tradeoffs change on a large cluster which has more options for execution strategies: for example, the extreme strategies of sync or async may not be sufficient for a larger cluster. This may prevent MXNet, which only supports these strategies, from scaling to a larger cluster.

### F.3 Detailed Tradeoff Space Analysis

This section analyzes the speedsups observed in the previous section to understand the contribution of each tradeoff selection that the optimizer made. These tradeoffs include (1) execution strategy (number of groups), (2) optimizing hyper-parameters to compensate for staleness, and (3) physical plan (server to machine allocation).

#### F.3.1 Penalty Definition

Consider again Figure 7 which we’ve replicated here for convenience in Figure 25 and also shown momentum (note that when the optimal explicit momentum is 0, there is an associated SE penalty). Recall this figure showed the tradeoff for compute groups on the CPU-L cluster for an epoch of ImageNet 1000. The HE and SE plots were multiplied to produce the right-most plot of total time to reach a final loss.

The vertical axis of the SE figure in Figure 25 shows what we call the SE penalty, $P_{SE}(S)$, which is defined as the ratio of the # iterations needed to converge relative to the case of no staleness ($S = 0$),

$$P_{SE}(S) = \frac{SE(S)}{SE(0)}$$

$P_{SE}$ is dimensionless, because it is the ratio of statistical efficiencies (#iter / #iter). The penalty is 1 when the staleness is 0, and should be higher for all $S > 0$. A higher $P_{SE}$ is worse (more iterations to converge).

Recall also that we defined hardware efficiency penalty ($P_{HE}$). This is shown in the middle graph of Figure 25. Since the statistical efficiency penalty is defined as the ratio of the # iterations to convergence with respect to $S = 0$, for consistency $P_{HE}(S)$ is also normalized with respect to $S = 0$. $S = 0$ is the case of 1 compute group, also called the synchronous case. The hardware efficiency penalty is defined as the ratio of the time per iteration relative to the time per iteration for this synchronous case,

$$P_{HE}(S) = \frac{HE(S)}{HE(0)}$$

As with $P_{SE}$, a higher $P_{HE}$ is worse (more time per iteration). Whereas $P_{SE}(S)$ increased with staleness, for hardware efficiency this trend is reversed: $P_{HE}$ decreases (iterations become faster) as the number of compute groups increases.

Note in these figures, the staleness is 0 for the FC model, so staleness on the horizontal axis refers only to the conv models (i.e. the number of conv compute groups).

Finally, recall that the product of hardware and statistical efficiency is the total time to convergence (Equation 1). Since the horizontal axis (staleness, i.e. # groups) is the same on both the SE and HE plots, these plots can be multiplied, and the resulting vertical axis is the total penalty, defined as the ratio of the total time to convergence (normalized to sync, i.e. $S = 0$):

$$P_{Total}(S) = P_{SE}(S) \cdot P_{HE}(S) = \frac{SE(S) \cdot HE(S)}{SE(0) \cdot HE(0)}$$

We use figures of this format throughout this section to quantify the benefit of the choice of compute groups.

#### F.3.2 End-to-End Imagenet 1000

Recall that Figure 25 was run for a 1-hour optimizer epoch of ImageNet 1000, on the CPU-L cluster. Figure 25 (bottom 2 sets of figures) shows the same experiment on the GPU-S cluster. Notice again that SE is flat, i.e. maximum asynchrony is optimal.

These figures show steady-state execution, hence the SE curves show no penalty (nearly flat). The same curves but for the cold-start epoch of the GPU-S cluster are shown in the top of Figure 25.

We also validate this for the small cifar dataset in Figure 29. Here for exposition we reduced the epoch size to 2 minutes (otherwise the cold start would converge after only a few minutes).

#### F.3.3 Small Clusters

The optimizer’s choice of execution strategy for the small cluster experiments is shown in Figure 28 (CPU-S) and Figure 29 (GPU-S). In addition to the imagenet-8 dataset we also include CIFAR-10 to show the optimizer is robust across datasets. We see that for these small clusters, choosing the execution strategy incorrectly incurs a penalty of roughly $1.5 \times$.

Note that Figure 28 and Figure 29 have the same statistical efficiency curves but different hardware efficiency curves. This is because the difference in throughput between the GPU machines and CPU machines exceeds the difference in network speed between these clusters so there is a higher
Figure 26: Cold start vs Steady state for Imagenet 1000 on GPU-S

penalty for the sync case on the GPU cluster. Also, neither of these 9 machine clusters reach FC saturation.

Next we consider the CPU-L cluster.

F.3.4 Large Cluster

The tradeoff for CPU-L is shown in Figure 30. (8 machines per group) was the optimal point, and that the optimizer chose this execution strategy. The detailed tradeoff space for CPU-L is analyzed in Figure [11]. Each curve, from the bottom up, represents a selection made by the optimizer. We’ve isolated each selection to observe their relative impact.

Avoiding Divergence. First, consider the red line, which represents the default point chosen by many systems: asynchronous with a large number of machines. Indeed, statistical efficiency is often ignored by other systems and so by default, the configuration with the best hardware efficiency (fastest iteration time) is erroneously selected. However if the published AlexNet hyper-parameters [17] (which are optimal for the sync case) are naively used in the async case, there is divergence. Thus, our tuning approach is critical.

The green curve shows that if only the learning rate $\eta$ is tuned, divergence can be avoided. Tuning $\eta$ is also common practice, although prior work does not do so explicitly to compensate for staleness as we advocate. In the green curve momentum is not been tuned, as many systems always use a momentum of 0.9 (as mentioned in [17]). For example, at the time of this study MXNet hard-codes this momentum into every example.

22. https://github.com/dmlc/mxnet/blob/02a0f4cbbf6ecacaf3a2341eb07a12d6298f88a6d/example/image-classification/train_model.py#L77

Figure 27: Cold start vs Steady state for cifar on GPU-S

Also, the green curve does not merge the FC compute and model servers by physically mapping them to the same machine. Instead, this curve represents the architecture shown in Figure 16 (a), i.e. there is an FC compute server for each CONV compute server, and each of these server pairs is mapped to a separate machine. Of the 33 machines therefore, one machine contains the CONV and FC model servers, while each of the other 32 contains a CONV compute and FC compute server. This configuration represents the strategy chosen by MXNet, so we report their async curve as the green line because their system is optimized for this case (note that doing this disadvantages our final speedup figure, i.e. if we had used Omnivore’s implementation of this tradeoff point our optimizer’s speedup would be $> 20 \times$). The remaining curves have their hardware and statistical efficiencies normalized to those of this green curve.

Device Mapping. We now examine our choice of merging the FC compute and model servers to the same machine (the 33rd machine), as Section 5 described. The other systems do not support this merging so we take “unmerged” as the baseline, and use the 33rd machine for the conv and FC model servers as MXNet and SINGA’s documentation suggests. The remaining curves will have their hardware and statistical efficiencies normalized to those of this curve.

The turquoise curve merges the FC servers. We see that this gives a $1.18 \times$ improvement to hardware efficiency (due to reduced communication) and a $2.55 \times$ improvement to statistical efficiency (due to no staleness in the FC model).

Overall, this is $3.01 \times$ faster to converge than the baseline.

In the turquoise curve, note that the hardware efficiency improvement is only $1.18 \times$ for the merged FC. As discussed
in Section 4.1 this is because while communication is reduced by merging these servers, on the large CPU cluster the FC saturation point is reached at 4 groups, and not mapping the FC servers to the same physical machine as described above eliminates the saturation (but requires more network communication and incurs a statistical efficiency penalty).

**Parameter Tuning for Staleness.** Divergence can always be avoided by tuning $\eta$ alone, and indeed most systems always use a momentum of 0.9 (see comment above) which is standard for the sync case [17]. However, we show in the purple curve that at larger staleness values, additionally tuning the momentum $\mu$ permits using a higher $\eta$. This does not change hardware efficiency, but now gives an overall 5.85 $\times$ speedup over the baseline due to improved statistical efficiency.

**Execution Strategy.** Finally, the blue line represents the actual choice made by the optimizer. In addition to the selections above, the optimizer did not choose 32 groups but 4 groups (Figure 30), which further improves the statistical efficiency to give an overall speedup of $> 20 \times$ compared to standard choices traditionally made by deep learning systems. Note that changing the number of groups to 4 did not hurt hardware efficiency because the FC server is already saturated (see Section 4.1).

**F.4 Scalability to a Larger Cluster**

The previous section showed that as a result of the optimizer’s tradeoffs Omnivore is able to scale to 32 machines. In this final experiment we compare Omnivore to the best competitor from the small clusters, MXNet, on this larger cluster. We use the same dataset and network as the small cluster experiments, and define convergence the same way (99% accuracy).

We attempted to open a cluster of 33 g2.8xlarge instances but continuously ran into EC2 errors related to not enough machines available (InsufficientInstanceCapacity).

As in Section 6.2 we repeat the same procedure to apply our optimizer to MXNet, i.e. we run each configuration for 10 minutes, select the best execution strategy and learning rate, and run that to convergence. The best strategy was once again sync with $\eta = 0.01$. Specifically, as in the previous experiments, we followed MXNet’s documentation and used the EC2 master machine as the root, and put the other 32 workers in the hostfile. We ran MXNet for 10 minutes with both sync/async and 4 orders of magnitude learning rate as described above. This time all 4 orders of magnitude for $\eta$ were needed because for sync with 32 machines, after 10 minutes 0.001 and 0.01 were almost the same, although 0.001 was better by $\sim 5\%$ points. Since this differs from the optimal $\eta$ from the 8 machine case, which was 0.01 (i.e. statistical efficiency changed for the larger cluster), to be sure we ran MXNet with each $\eta$ to convergence and noticed that in fact 0.01 was significantly faster to converge in the end, as was true on the smaller clusters. Similarly, for async after 10 minutes the best $\eta$ was 0.00001, although this was close to 0.0001, therefore once again we ran both to convergence and noticed that 0.0001 was faster to con-
verge for MXNet. We did not do this extended parameter tuning for Omnivore, and only ran the 1 minute static runs described above, to make sure that we were getting the best possible performance from MXNet for our comparison.

For Omnivore the optimizer was used as described in the previous section. The best result of MXNet and Omnivore is shown in Figure 12(c). We see that Omnivore is 3.2× faster than MXNet to converge now (it was 2.3× faster on the 9 CPU cluster). In addition, we see that compared to Figure 12(a), Omnivore sped up on the larger cluster but MXNet did not. Therefore not only does the optimizer give speedups by not relying solely on the sync strategy and by merging the FC servers, but also enables scalability to more machines.

If we do not apply our optimizer to MXNet, Omnivore now converges 20× faster. This is compared to MXNet’s async strategy, which has poor statistical efficiency for 32 machines. This 20× corresponds exactly to the speedup in the previous section because the green curve in that section is MXNet using the async strategy (i.e. they are the same point in the tradeoff, see the discussion in Appendix F.3.) By applying our optimizer to MXNet we select the sync strategy instead, which lowers the gap with Omnivore to 3× on this cluster. Therefore this section shows not only that the optimizer gives speedups of more than an order of magnitude, but that it is versatile and can be applied to existing tools.

F.5 End-To-End Experiments

The end-to-end result is in Figure 10. We trained the standard CaffeNet (same setup as in Appendix F.2) using ImageNet-1000 on both systems using both the CPU-L and GPU-S clusters. We time out each run after 8 hours and report the training accuracy vs. time.

According to MXNet’s official performance tuning guideline, they recommend trying the sync strategy, but also state that “if the model size is quite large or you use a large number of machines, you may want to use dist_async”. Immediately above, they describe large as “models with size >> 100MB such as AlexNet and VGG.” Because we are training AlexNet and use up to 33 machines, which may be considered large, then according to these instructions async could be the best choice. Because they do not provide an automatic mechanism to make this decision we followed this advice and tried both strategies, as we did above in section F.2. This required tuning the learning rate for each strategy. We used the optimal learning rate obtained for each strategy on ImageNet-8, as recommended by 3 which states that “the best way to determine the correct learning rates is to perform experiments using a small but representative sample of the training set”. In addition, MXNet does not provide a learning rate schedule for their AlexNet example (as of the writing of this study) so we use the standard learning rate schedule of 17 which decreased the learning rate by 10× when training plateaued.

For Omnivore, we ran the optimizer end-to-end. We ensure a 10% overhead by running the optimizer and then training for 10× the optimizer time before rerunning the optimizer. Each time the optimizer runs, it searches momentum, μ and learning rate, η, either reducing one, reduc-

![Figure 32: Recurrent Neural Network using 9 EC2 c4.4xlarge CPU machines.](https://example.com/image-7.png)

![Figure 33: Comparison of Omnivore’s optimizer to CaffeNet’s default learning rate schedule on Full ImageNet with AlexNet.](https://example.com/image-8.png)

F.6 Preliminary RNN/LSTM Result

To understand if our tradeoff applies more broadly, we implemented the Recurrent Neural Network model and LSTM proposed by Graves [11]. Following the same protocol as Figure 28 and using the CPU-S cluster, we see in Figure 32 that the tradeoff between statistical efficiency and hardware efficiency is comparable, and choosing a completely synchronous or asynchronous configuration can be up to 2× slower than the optimal configuration.

F.7 Comparison to Standard Schedules

We have shown that tuning is critical for good performance. We next validate the hypothesis that Omnivore’s optimizer outperforms standard tuning and parameter scheduling methods. To validate this, we run Omnivore on the full ImageNet using the standard CaffeNet. We run two versions of Omnivore: (1) Omnivore (Default Schedule), which uses CaffeNet’s default learning rate schedule

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24 We also see a similar tradeoff in the LSTM variant proposed by Graves [11].
that decreases the learning rate by 10\(x\) every 100,000 iterations; and (2) Omnivore, which uses the standard Omnivore optimizer. To be fair, both versions use the same grid search strategies to select the optimal learning rate, momentum, and number of compute groups at the beginning. In addition, we run Omnivore for 10\(x\) the optimizer time before it re-optimizes the parameters.

Figure 33 shows the training loss vs. wall-clock time. The two plateaus shown in Omnivore correspond to the times Omnivore re-optimizes the parameters. The losses of both Omnivore (Default Schedule) and Omnivore decrease over time. However, after the first parameter re-tuning, Omnivore’s loss starts to decrease more rapidly. Finishing at 36K seconds, Omnivore is 1.5\(x\) faster to achieve the same loss as Omnivore (Default Schedule). Omnivore does not require the user to specify the number of iterations to run before re-optimizes the parameters.

**F.8 Comparison to Bayesian Optimizer**

We compare our simple optimizer with the state-of-the-art Bayesian optimization approach that explores the parameter space of CNNs. The results are shown in Figure 34. We follow Snoek et al. to model the search space as \((\eta, \mu, S, N)\) where \(N\) is the number of epochs to run. We use the same search space for \((\eta, \mu, S)\) as in our optimizer and measure both the number of configurations and the total number of epochs that the Bayesian optimizer needs to run before finding a run that achieves an accuracy within 1% of the best loss after 1000 seconds.

Our procedure is as follows. We first run Omnivore to obtain a run which reaches 99% convergence using the same dataset and cluster as in Figure 12(b). This took 80 epochs. We then give the Bayesian optimizer \(N = 80\) and it tries to fit \(\eta, \mu\) and \(S\) in order to reach the lowest loss (highest accuracy) by 1000 seconds. It searches \(N\) in the range \(1, \ldots, 80\), \(\mu\) in the range \(0.0, 0.3, 0.6, 0.9\), and learning rates in the range \(0.1, 0.01, 0.001, 0.0001, 0.00001\), i.e. the same as Omnivore searches.

It took the Bayesian optimizer on average 12 runs before finding a strategy which achieves accuracy within 10% of Omnivore’s run. On average this takes 6\(x\) more epochs than just training to convergence, which makes the Bayesian approach infeasible to run on Imagenet 1000 (whereas Omnivore’s optimizer incurred only a 10% overhead).

Compared with our optimizer, one difference is that we are using the first minute’s execution as a proxy for a longer run, while on the other hand, Snoek et al. have the number of epochs to run as a parameter to explore and do not share information across runs. It is of course possible to use Bayesian optimization to guide our grid search for the first minute, however, it is future work to integrate this heuristic into the Bayesian optimization framework in a principled way.

**G. APPENDIX STUDYING TOTAL COST OF OWNERSHIP (TCO)**

Our study showed that CNN training is compute-bound regardless of the compute device used. Given that we can now train CNNs on CPUs proportional to the CPU FLOPS, this opens new questions in total cost of ownership (TCO) for running CNN systems. We discuss those trends and changes.

**Single Node:** We compare the price of running Omnivore on a GPU instance (g2.2xlarge, $0.65/hr, 1.2 TFLOPS) and a CPU instance (c4.4xlarge, $0.838/hr, 0.7 TFLOPS) for the same number of iterations. As Figure 11 showed, Omnivore’s speed on the c4.4xlarge instance is 0.57\(x\) the speed of the g2.2xlarge instance. This ratio closely matches the FLOPS ratio 0.7/1.2. Therefore we observe that running on a CPU instance is 2.1\(x\) more expensive than a GPU instance, due to the difference in the FLOPS/dollar ratio for these instances. This suggests that on cloud services such as Google Compute which do not have GPU instances, CPU-based deep learning is a viable and cost-effective option when using Omnivore. Moreover, organizations that can amortize the cost of CPUs in more ways than GPUs may find them to be a cheaper alternative.

**Distributed:** In the distributed setting we consider again the case of 9 machines and compare Omnivore running on the GPU cluster (g2.8xlarge, $2.60 per machine-hr, 4.8 TFLOPS per machine) and CPU cluster (c4.4xlarge, $0.838 per machine-hr, 0.7 TFLOPS per machine). The difference in peak FLOPS between these clusters is 6.8\(x\), and the speedup to convergence obtained by Omnivore on the GPU cluster compared to the CPU cluster is 5\(x\)-note it is not quite 6.8\(x\) because network speed does not scale with the node throughput. If we consider only hardware efficiency (since statistical efficiency is unrelated to the underlying hardware), the GPU cluster is 5.6\(x\) faster than the CPU cluster, which is nearly the FLOPS ratio. As in the single-machine case therefore it is only the FLOPS/dollar ratio which matters. The GPU cluster is more cost-effective, now by a factor of 1.8\(x\).

These results show that CPU deep learning is not significantly different from GPU in terms of consumer cost, and it will be exciting to see how these trends change for future CPUs which have increased SIMD parallelism as well as newer GPUs which optimize for lower power. As SIMD processor bandwidth has been doubling in each generation, it seems that CPU training may indeed catch GPUs relatively soon.

**G.1 Distributed Calculation**
The ratio of peak FLOPS of the GPU cluster / CPU cluster is $4.9/0.74 = 6.6$. Considering the optimal points chosen by our optimizer, the CPU / GPU time to convergence is $5\times$. If statistical efficiency is ignored, and we compare only the speeds of the async cases on each cluster, the ratio is now $34s/iter$ for the CPU cluster and $6s/iter$ for the GPU, or $5.6\times$, which almost matches the ratio in device FLOPS. Given that GPU cluster is $\$2.6/\$0.838 = 3.1\times$ more expensive, the GPU cluster is $1.8\times$ cheaper per iteration which matches closely with the FLOPS/dollar ratio.

H. APPENDIX FOR CONCLUSIONS (SECTION 8)

Our study first demonstrated that on a single machine we could achieve CPU speeds proportional to the device FLOPS, showing end-to-end speedups of more than $5.5\times$ on EC2 CPU instances over state-of-the-art tools. With this improved CPU speed we showed that CNN computations in a machine to be treated as a black-box, and we are $2.7\times$ faster than other systems on 4 GPUs and also $15\%$ faster on a single GPU by using the weak CPU alongside the EC2 instance’s GPU. More generally, we show that each device or node in a cluster can be treated as a black-box that is characterized only by the throughput which it provides and is irrelevant to the type of hardware on that node (e.g. CPUs or GPUs).

Our second contribution was an empirical study of the factors affecting time to convergence for distributed deep learning training, and a novel, theoretical characterization of asynchrony which demonstrates that by tuning algorithmic (explicit) momentum in SGD there is no statistical penalty associated with asynchronous execution. We justified this empirically. We defined a tradeoff space and demonstrated that the execution strategy and server architecture were key in reducing the total time to convergence. We further showed that all existing distributed deep learning systems fall somewhere along this tradeoff space, but do not optimize within the space.

Finally, we studied each of these tradeoffs by decoupling their impact on hardware and statistical efficiency. This made it possible to study these factors in isolation and build an optimizer which optimizes within the tradeoff space. We showed both theoretically and empirically the need to jointly tune hyper-parameters with execution strategies in order to avoid slower convergence or divergence. We show that our optimizer provides a $>20\times$ reduction in time to convergence compared to other systems which select sub-optimal points in the space, and we also show that our optimizer is versatile by applying it to existing tools. In doing so, we close the gap between our system to $3\times$ faster than other systems, in some cases also preventing divergence in those other tools.