Performance Analysis Comparison of 4-2 Compressors in 180nm CMOS Technology

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Abstract: In this paper, different 4-2 compressors are designed by using various logic styles and their performances are compared. Different 4-2 compressors are designed and simulated by using the Cadence Virtuoso tool in 180nm CMOS technology and the performance parameters of these are studied in terms of maximum output delay, average power consumption and power-delay-product (PDP) with a variation of supply voltage ranging from 1.2V to 3.0V. Simulation results depict that the performance of a compressor depends on the performance of Exclusive-OR-Exclusive-NOR (XOR-XNOR) module and Multiplexer (MUX), and performance varies as per the logic styles used to implement these blocks.

Keywords: Compressor, CMOS logic style, high speed, low power, pass transistor logic style.

1. INTRODUCTION

Day by day, popularly the demands and necessity for a high speed and low power electronics system are increasing. That’s the reason it has been a field of greater concern and interest of the VLSI design engineers to develop and design a fast and efficient system over decades. A (m:n) compressor which is a processing element having the versatile use in the high speed systems takes m inputs and produces n outputs [1]. Therefore the utility and demand of high speed compressors are increasing in a broad spectrum in many parts of a digital system, especially in digital signal processors, digital filters, general purpose microprocessors, three dimensional (3-D) graphics applications, motion estimation accelerators etc [2]-[7]. Multiplier is the crucial constituent of some of these aforementioned applications. In multiplier compressors are introduced to reduce the number of operands when the partial products generated at the first stage of multiplication are added [1], [4]. Hence to improve the performance of various multipliers like Vedic multiplier, Wallace tree multiplier, Array multiplier, RSFQ multiplier etc. the high speed, low power and area efficient compressors are employed [5], [8]-[11]. VLSI designers have designed various high performance 4-2 compressors and it is one of the popular compressors among them due to its regular interconnection and simple structure which make it suitable for fast digital computational circuits.

In this paper various designs of existing high performance 4-2 compressors with different logic styles are studied. In Section 2 a brief description about the 4-2 compressor and two existing architectures of it is explained. In Section 3 various existing 4-2 compressors designed
with different logic styles are discussed. The simulation results these compressors are presented in Section 4 and at last Section 5 concludes the paper.

2. 4-2 COMPRESSOR

4-2 compressors are combinatory circuit which compresses number of operands when partial products are added. The block diagram and full adder based configuration of 4-2 compressors are shown in Fig. 1(a) and Fig. 1(b) respectively. It accepts five inputs namely M1, M2, M3, M4 and Cin which are weighted as i and generates three outputs Sum, Carry and Cout which are weighted as i, i+1 and i+1 respectively. The Cin comes from a compressor in preceding stage having weight i-1 and the Cout goes to a compressor in succeeding stage having weight i+1. It has been observed in Fig. 1 that Cout is independent of Cin which makes it advantageous for high speed operation. In Fig. 2 two commonly used architectures are shown [13], [15]. The architecture shown in Fig. 2(b) is the modified version of the architecture shown in Fig. 2(a). This modified architecture exhibits faster operation as it involves critical path delay of one Exclusive-OR-Exclusive-NOR (XOR-XNOR) module plus two multiplexers (MUX) while the gate delay offered by the architecture in Fig. 2(a) and the full adder based configuration in Fig. 1(b) are three Exclusive-OR (XOR) gates and four XOR gates respectively. A 4-2 compressor has to comply with (1):

\[ M1 + M2 + M3 + M4 + Cin = Sum + 2 \times (Carry + Cout) \]  

(1)

Based on (2)-(4), the architectures are implemented:

\[ Sum = M1 \oplus M2 \oplus M3 \oplus M4 \oplus Cin \]  

(2)

\[ Cout = (M1 \oplus M2) \times M3 + (M1 \oplus M2) \times M1 \]  

(3)

\[ Carry = (M \oplus M2 \oplus M3 \oplus M4) \times Cin + (M1 \oplus M2 \oplus M3 \oplus M4) \times M4 \]  

(4)

![Fig.1.](image)

Fig.1. (a) Block diagram (b) Full adder based configuration of 4-2 compressor.
In literature several designs of 4-2 compressor have been depicted [2], [4], [5], [12]-[17]. In this paper some of the existing designs of 4-2 compressor are studied. The fully Complementary Pass-Transistor Logic (CPL) and Double Pass-Transistor Logic (DPL) multiplexer based 4-2 compressors are presented in [14]. They are considered as one of the fastest design among compressor family. A hybrid compressor is proposed in [15]. This compressor utilizes the advantages of both CMOS logic style and transmission gate logic style. The delay and power consumption of the 4-2 compressor is less compared to that of CMOS. A new 4-2 compressor designed with 10 transistors (10T) XOR-XNOR module and transmission gate MUX is proposed in [16]. This design offers high speed and good driving power. Another 4-2 compressor designed with 8 transistors (8T) XOR-XNOR module and transmission gate MUX is presented in [17]. It consumes low power.

3. 4-2 COMPRESSOR WITH DIFFERENT LOGIC STYLES

3.1 4-2 Compressor Based on CMOS Logic Style

CMOS logic style uses equal number of PMOS and NMOS transistors. Fig. 3 shows a 4-2 compressor (named as D_1) designed by using CMOS logic style [15], [16]. Compressor designed by using this logic style gives stable and reliable operation for different power supplies and offers high noise immunity. It also has high driving capability due to presence inverter at output terminals. However it consumes more power and takes more area as more number of transistors is used to implement this logic style.

3.2 4-2 Compressor Based on CPL and DPL Logic Style

The fully CPL and DPL logic style based 4-2 compressors are shown in Fig. 4 and Fig. 5 respectively [14]. CPL based 4-2 compressor (D_2) consists of NMOS pass transistor network and for which it cannot produce full voltage swing when logic high signal needs to pass. For this reason, CPL network needs a level restoring arrangement at output terminals. Here two PMOS transistors are used. In DPL logic based compressor (D_3) equal number of PMOS and NMOS transistors are used and therefore extra level restoring circuitry is not required. However DPL structure covers comparatively more area as PMOS transistors are used. Both structures are dual rail structure, thus inverter is used at input terminals to generate the complementary input pairs which increases the switching activity. Hence these types of very fast compressors consume more power.
3.3 4-2 Compressor Based on Combination of CMOS Logic Style and Transmission Gate Logic Style (Hybrid)

Different logic styles are combined to design various high performance compressors. This type of compressors are called hybrid compressors. A 4-2 hybrid compressor (D_4) designed by using a combination of the CMOS logic style and transmission gate logic style is shown in Fig. 6 [15]. Here the use of transmission gate MUX in the intermediate stage has optimized the speed of the compressor.
and also reduced the number of transistor counts. Furthermore this design utilizes the XOR and XNOR outputs for which the carry generators and the intermediate MUX don’t require additional inverter for select inputs. Hence the power consumption is also decreased. This design is suitable for tree structured applications as CMOS logic style is used to generate the output which offers sufficient driving capacity.

3.4 4-2 Compressor Based on 10 Transistors (10T) XOR-XNOR Module and Transmission Gate MUX

The circuit diagram of the 4-2 compressor (D_5) consists of 10 transistors (10T) XOR-XNOR module and transmission gate based MUX module is shown in Fig. 7 [16]. In this design the 10T XOR-XNOR gate can able to produce full voltage swing at outputs for every combination of inputs due to the presence of serially connected PMOS transistors and NMOS transistors, and for a pair of feedback PMOS-NMOS transistors [4]. Thus, this 4-2 compressor is suitable for high speed computational circuits. Moreover the inverters at the outputs give high driving capability to the compressor. But due to the presence of these inverters the switching activities increase which leads power dissipation in the design.

3.5 4-2 Compressor Based on 8 Transistors (8T) XOR-XNOR Module and Transmission Gate MUX

A new low power XOR-XNOR module consisting of 8 transistors is proposed in [17]. As static CMOS inverter is used to implement this XOR-XNOR module, this design can capable to provide good driving power and operate at low supply voltages. By using this 8T XOR-XNOR module and Transmission gate MUX a low power 4-2 compressor (D_6) is designed. The circuit diagram of the compressor is shown in Fig. 8. Here transmission gate MUX doesn’t use inverters at its output terminal. Although this type of low power MUX provides higher speed than CMOS MUX, it cannot provide adequate driving capability. Thus, when this type of compressor is used in tree structured configuration buffer needs to be added after some stages for which power consumption increases.
Fig. 7. 4-2 compressor designed by using 10T XOR-XNOR module and transmission gate logic style (D_5).

Fig. 8. 4-2 compressor designed by using 8T XOR-XNOR module and transmission gate logic MUX (D_6).

4. PERFORMANCE ANALYSIS OF 4-2 COMPRESSORS

The simulations of these six different designs of 4-2 compressor are performed by using Cadence Virtuoso Tool in 180nm CMOS technology. Table I shows the configuration of all simulated designs of 4-2 compressors. It shows the comparison of number of transistor required to implement the 4-2 compressors. Design D_6 uses only 40 transistors while D_1 uses maximum number of transistors.

Table II, Table III and Table IV show the comparison of the maximum output delay, average power consumption and power-delay-product (PDP) of the 4-2 compressors respectively. The comparisons are carried out at various supply voltages ranging from 1.2V to 3.0V at the operating frequency of 100MHz. Table II shows that the designs D_2 and D_3 have comparatively shorter maximum output delay among all the 4-2 compressors. Again, designs D_1 and D_4 exhibit higher delay among all designs. The design D_6 has the highest delay at 1.2V and exhibits moderate speed for the supply voltages ranging 1.6V to 3.0V. However this compressor consumes the lowest power given in Table III. The design D_1 and D_5 consume comparatively more power among all simulated compressors. But the design D_3 consumes the highest power at supply 1.2V and 1.4V. The PDPs of designs D_2, D_3 and D_6 are comparatively better than the other designs.

| Table I. Configuration of 4-2 compressors |
|------------------------------------------|
| Compressor Designs | Transistor Count | Reference |
|---------------------|------------------|-----------|
| CMOS (D_1)          | 72               | [15], [16]|
| CPL (D_2)           | 46               | [14]      |
| DPL (D_3)           | 58               | [14]      |
| Hybrid (D_4)        | 62               | [15]      |
| 10T XOR-XNOR module and Transmission gate MUX (D_5) | 60 | [16] |
| 8T XOR-XNOR module and Transmission gate MUX (D_6) | 40 | [17] |
Table II. Comparison of maximum output delay of 4-2 compressors in picoseconds

| Supply (V) | D_1   | D_2   | D_3   | D_4   | D_5   | D_6   |
|-----------|-------|-------|-------|-------|-------|-------|
| 1.2       | 860.2 | 521.6 | 513.9 | 958.0 | 740.5 | 997.8 |
| 1.4       | 667.1 | 389.5 | 365.7 | 703.5 | 565.3 | 656.0 |
| 1.6       | 556.9 | 310.2 | 282.0 | 560.3 | 462.8 | 429.4 |
| 1.8       | 486.3 | 263.9 | 234.6 | 473.9 | 397.1 | 396.2 |
| 2.0       | 437.9 | 238.7 | 209.3 | 418.0 | 352.0 | 336.7 |
| 2.2       | 403.0 | 223.1 | 190.8 | 379.6 | 320.2 | 296.6 |
| 2.4       | 377.1 | 210.1 | 176.9 | 351.6 | 296.4 | 267.7 |
| 2.6       | 357.3 | 200.1 | 166.3 | 330.7 | 278.5 | 246.0 |
| 2.8       | 341.6 | 192.3 | 157.6 | 314.4 | 263.7 | 229.0 |
| 3.0       | 329.1 | 186.0 | 150.7 | 301.5 | 252.0 | 215.4 |

Table III. Comparison of average power consumption of 4-2 compressors in microwatts

| Supply (V) | D_1   | D_2   | D_3   | D_4   | D_5   | D_6   |
|-----------|-------|-------|-------|-------|-------|-------|
| 1.2       | 33.78 | 31.53 | 34.76 | 28.50 | 31.97 | 20.98 |
| 1.4       | 47.02 | 44.01 | 47.84 | 40.15 | 44.60 | 29.94 |
| 1.6       | 62.84 | 58.73 | 63.15 | 54.22 | 59.86 | 41.14 |
| 1.8       | 81.35 | 75.64 | 80.77 | 70.91 | 77.82 | 54.76 |
| 2.0       | 102.7 | 94.74 | 100.7 | 90.38 | 98.60 | 70.92 |
| 2.2       | 126.9 | 116.1 | 123.0 | 112.6 | 122.3 | 89.70 |
| 2.4       | 154.1 | 139.6 | 147.7 | 137.9 | 149.1 | 111.2 |
| 2.6       | 184.4 | 165.5 | 174.9 | 166.0 | 178.9 | 135.5 |
| 2.8       | 217.7 | 193.6 | 204.6 | 197.3 | 211.8 | 162.8 |
| 3.0       | 254.4 | 224.1 | 237.0 | 231.9 | 248.1 | 193.3 |

Table IV. Comparison of power-delay-product of 4-2 compressors in femtojoules

| Supply (V) | D_1   | D_2   | D_3   | D_4   | D_5   | D_6   |
|-----------|-------|-------|-------|-------|-------|-------|
| 1.2       | 29.05 | 16.45 | 17.86 | 27.30 | 23.67 | 20.93 |
| 1.4       | 31.36 | 17.14 | 17.50 | 28.25 | 25.21 | 19.64 |
| 1.6       | 34.99 | 18.22 | 17.81 | 30.38 | 27.70 | 20.26 |
| 1.8       | 39.56 | 19.96 | 18.95 | 33.60 | 30.90 | 21.70 |
| 2.0       | 44.97 | 22.61 | 21.08 | 37.78 | 34.71 | 23.88 |
| 2.2       | 51.14 | 25.90 | 23.48 | 42.74 | 39.16 | 26.61 |
| 2.4       | 58.11 | 29.33 | 26.13 | 48.49 | 44.19 | 29.77 |
| 2.6       | 65.88 | 33.12 | 29.09 | 54.90 | 49.82 | 33.33 |
| 2.8       | 74.36 | 37.23 | 32.24 | 62.03 | 55.85 | 37.28 |
| 3.0       | 83.72 | 41.68 | 35.72 | 69.92 | 62.52 | 41.64 |

5. CONCLUSION

Different 4-2 compressors designed with different logic styles are studied in this paper. The performance parameters of these compressors are compared with varying the supply. From the simulation results it has been culminated that for very fast applications compressors (D_2, D_3) designed by using CPL and DPL logic are suitable. Although these are energy efficient but they consume more power. For low power and high speed applications design D_6 is suitable. The designs D_2 and D_6 are preferable for area efficient applications as they use less number of transistors. Moreover designs D_1, D_4 and D_5 are suitable for tree structured configurations owing to their sufficient driving capability. For low power and area efficient applications design D_6 is preferable while for high speed and area efficient applications design D_2 is preferable.
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