A 56-Gbps PAM4 amplitude-rectification-based receiver with threshold adaptation and 1-tap DFE

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Abstract This paper presents a 56-Gbps four-level pulse amplitude modulation (PAM4) quarter-rate receiver based on amplitude rectification. Compared with the conventional three-comparator structure, the PAM4 signal is converted into a 2-digit gray-code rather than a 3-digit thermometer-code. The amplitude is detected to decode the least significant bit (LSB), which allows the proposed receiver to use significantly less power by reducing the number of comparators. An inverter-based common-mode voltage stabilization circuit (CVSC) is proposed to reduce the effect of common-mode level changes as the amplitude is determined. To minimize the feedback delay, the 2-digit gray-code is fed back to DFE’s summer directly. By reducing the digit of the feedback signal, the power will be further reduced as the DFE tap increases. The device consumes 83.5 mW over a 55-nm process.

key words: PAM4, receiver, amplitude-rectification-based, DFE,
Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

High-speed serial links have become a popular choice for modern communication systems. Todays demand for increasingly high bandwidth is difficult to accommodate due to channel and IC process limitations. Four-level pulse amplitude modulation (PAM4) signaling may be used to replace NRZ signaling due to its much lower bandwidth. Many I/O standards currently support PAM4 at high speeds [1, 2]. PAM4 signaling requires different threshold voltages to distinguish the four levels, which increases the systems complexity.

ADC-based receivers convert the input PAM4 signal into digital signal. Then the signal processing is implemented by digital circuit, including the slicers, the DFE and so on. Thus, these receivers are widely used because of their de-

logics, and can reach very high speed. However, comparator-comparators consume a great deal of power, thus markedly increasing the total power consumption of the system.

Another important issue inherent to PAM4 signaling is that the DFE feedback signal should represent four levels rather than two levels. The traditional PAM4 DFE feedback 3-digit thermometer code needs three comparators [22, 23, 24]. The number of latches increases 3 times as the number of DFE taps increases, which consumes a large amount of power. Previous researchers have established a receiver that is amplitude-rectification-based [25]. By performing amplitude rectification for decoding the least significant bit (LSB), the receiver uses fewer comparators than the traditional architecture and thus consumes less power. Although this receiver does use relatively few comparators, changes in common-mode voltage may affect the accuracy of amplitude rectification.

To determine the threshold voltage, the conventional PAM4 receiver first detects 4 levels [21, 23, 24] and then determines the threshold voltage (the middle of the eye). Compared with the conventional receiver, a receiver based on amplitude-rectification should only distinguish 2 levels of the rectifier output; this greatly simplifies the threshold voltage adaptation process.

This paper proposes a 56 Gbps PAM4 amplitude rectification-based receiver. The receiver consumes relatively little power due to its reduced number of comparators without sacrificing its functional effectiveness.

2. Proposed Receiver Architecture

Fig. 1 shows the architecture of the proposed receiver. PAM4 signals are detected by an amplitude-rectification-based decoder. To ensure stable detection, a sample-and-hold (S/H) holds the sampled values when decoding signals. The outputs of the decoder, gray-code for PAM4, are converted to binary-code for further processing. The 2-bit gray-code is fed back to the summer directly to minimize feedback delay.

2.1 Amplitude-rectification-based Decoder

The conventional topology includes three comparators that distinguish the four levels of the PAM4 signal. The most
significant bit (MSB) of the PAM4 signal can be decoded by a comparator with a threshold of 0 while the LSB is decoded by two comparators. If the LSB can be decoded with one comparator, fewer comparators are necessary and the load of the previous circuit would be reduced. PAM4 signals have two amplitudes which contain the LSB information; detecting the amplitude of PAM4 signals decodes the LSB. The architecture of the proposed amplitude-rectification-based decoder is shown in Fig. 2. The rectifier detects the amplitude of the PAM4 signal and outputs two voltage levels. The output of the rectifier distinguished by a comparator (latch) with a threshold voltage \( V_t \), then the G_LSB is decoded. Another comparator (latch) decodes the G_MSB. The amplifier before MSB detection amplifies the amplitude and reduces the latch delay. The outputs of the two comparators are 2-digit gray-code which must be converted into binary-code, so a logical transformation (not shown in Fig. 2) is necessary. Latches with threshold voltages \( V_{th} \) and \( V_{ll} \) detect the top and bottom of the rectifiers eye diagram, then adjust the threshold voltage according to the result. Details regarding the threshold voltage generation process are provided below in the section “Threshold-adaptation”.

The circuit of the rectifier is shown in Fig. 3. An NMOS transistor pair detects the amplitude (power) of the input signal. The current flowing through the NMOS pair increases as the amplitude increases, thus, the voltage \( V_{out} \) at the output node decreases. The current flowing through the NMOS pair decreases as the amplitude decreases, thus, the voltage \( V_{out} \) at the output node increases. The voltage \( V_{out} \) reflects the amplitude of the input signal.

2.2 PAM4 Signal Decoding

PAM4 signals have two amplitudes that can be defined as \( V_{big} \) (large) and \( V_{small} \) (small), respectively. The relationships between PAM4 signals and comparator outputs are shown in Table I. As mentioned above, the outputs of the two comparators are 2-digit gray code.

Fig. 4 shows the timing of the decoder. The S/H holds the input signal for 2 periods when clock phase 0 rises. Then the rectifier detects the amplitude of the signal and gets the LSB. Note that the rectified result is the opposite of LSB. Thus, the differential input of latch should be reversed. By using the S/H, the signal is maintained for 2 periods, which relaxes the hold time of the latch.

To convert them into binary code, \( B_{MSB}=G_{MSB} \) and \( B_{LSB}=G_{MSB} \oplus G_{LSB} \). Only a XNOR gate is required for this operation, which is simpler than the thermometer code decoder in traditional PAM4 architecture.

| Data | V_{big} | V_{small} |
|------|---------|-----------|
| 11   | 1       | 1         |
| 10   | 1       | 0         |
| 01   | 0       | 0         |
| 00   | 0       | 1         |

Table I. Relationships Between PAM4 Signals and Comparator Outputs
3. Common-mode Voltage Stabilization Circuit

The output voltage changes as the input common-mode level changes, which causes the rectifier to detect the PAM4 signal amplitude incorrectly. To eliminate this problem, the input of the rectifier must have a stable common mode level.

![Common-mode Voltage Stabilization Circuit](image)

Fig. 5. Common-mode Voltage Stabilization Circuit

The CVSC serves to eliminate changes in the common-mode level by subtracting two differentially input signals. The input voltage changes can be divided into common mode voltage changes $\Delta V_c$ and differential mode voltage changes $\Delta V_d$.

\[ \Delta V_{inp} = \Delta V_c + \Delta V_d \]  

\[ \Delta V_{inn} = \Delta V_c - \Delta V_d \]  

The idea of CVSC is to subtract two differential inputs. Thus, the changes in common mode voltage will be eliminated. Taking $V_{outp}$ as an example, $V_{outp}$ is equal to $V_{inn}$ and added to $V_{inn}$ after the reverse, then re-reversed; that is, $V_{outp}$ is equal to $V_{inn}$ minus $V_{inn}$. The output of the common mode level stabilization circuit is shown in Eqs. 3 and 4. After the common mode level stabilization circuit, the change of the common mode level of the differential signal is eliminated and only the differential mode level is retained. Therefore, the common mode level of the output signal remains basically unchanged.

To show the minimum input voltage which can be detected, the input-referred offset voltage of CVSC is shown in Fig. 7, and its $\sigma$ is 12.3 mV. However, as shown in [27], the layout of inverter-based CVSC resembles a standard cell style. Thus, the area is minimized and the systematic mismatches caused by thermal gradient and process gradient effect are reduced. The mismatches of the CVSC maybe much smaller than the simulation results.

![Input-referred offset voltage of CVSC](image)

Fig. 7. Input-referred offset voltage of CVSC

\[ \Delta V_{outp} = \Delta V_{inn} \cdot \left( \frac{g_{ml}}{g_{ml}} \right) \cdot \left( \frac{g_m}{g_{ml}} \right) - \Delta V_{inn} \cdot \left( \frac{g_m}{g_{ml}} \right) \]

\[ = \left( \frac{g_m}{g_{ml}} \right) \cdot (\Delta V_{inn} - \Delta V_{inn}) \]

\[ = 2 \cdot \left( \frac{g_m}{g_{ml}} \right) \cdot \Delta V_d \]  

(3)

\[ \Delta V_{outn} = \Delta V_{inn} \cdot \left( \frac{g_{ml}}{g_{ml}} \right) \cdot \left( \frac{g_m}{g_{ml}} \right) - \Delta V_{inn} \cdot \left( \frac{g_m}{g_{ml}} \right) \]

\[ = \left( \frac{g_m}{g_{ml}} \right) \cdot (\Delta V_{inn} - \Delta V_{inn}) \]

\[ = -2 \cdot \left( \frac{g_m}{g_{ml}} \right) \cdot \Delta V_d \]  

(4)

4. DFE

4.1 DFE Summer

The DFE summer is shown in Fig. 8. Vin is the input signal of the summer; its tail current source $I_{main}$ corresponds to the main tap coefficient. $V_{msb}$ and $V_{lsb}$ are the Gray code MSB output and LSB output of the previous bit of the PAM4 signal. The tail current source $I_{post}$ corresponds to the first tap coefficient. The tap coefficient can be changed by changing $I_{post}$.

In a traditional NRZ DFE, the feedback signal (sign of the previous signal) is multiplied by the tap coefficient and then accumulated with the input signal. In PAM4 DFE, the previous signal has four levels and the feedback signal needs to represent one of them. In the proposed design, $G_{msb}$ indicates the sign of the previous signal and $G_{lsb}$ indicates
its amplitude. \( G_{msb} \) and \( G_{lsb} \) are the MSB and LSB of the gray-code, respectively. When \( G_{lsb} = 1 \), the amplitude of the feedback signal is 1. When \( G_{lsb} = -1 \), the amplitude of the feedback signal is 1/3. The DFE summer controls the accumulation times of the feedback signal \( G_{msb} \) according to its amplitude (\( G_{lsb} \)) so that the feedback signal can represent one of 4 levels.

\[
\begin{align*}
D_{out}(t) &= D_{in}(t) + \omega \cdot 3 \cdot G_{msb}, \quad G_{lsb} = 1 \\
D_{out}(t) &= D_{in}(t) + \omega \cdot G_{msb}, \quad G_{lsb} = -1
\end{align*}
\]

4.2 DFE Timing

There are two critical paths in DFE, one is the MSB path, the other is the LSB path. As the delay of the amplifier in the MSB path is less than the delay of CVSC and rectifier, the LSB path has more stringent timing. To meet the stringent timing, the delay of CVSC and rectifier should be designed carefully. Moreover, the 2-digit gray-code (instead of the binary-code) is fed back to DFE’s summer directly to minimize the feedback delay.

5. Threshold-adaptation

The output level of the rectifier is uncertain, so a threshold voltage adaptation process is necessary to distinguish the two levels of rectified results. To obtain accurate results, the threshold voltage should be placed in the middle of the eye diagram. By detecting the top and bottom of the eye, the voltage in the middle of the eye diagram can be determined. The threshold-adaptation circuit is implemented by digital circuit. As mentioned in the section 2.1, latches with threshold voltages \( V_{th} \) and \( V_{tl} \) detect the top and bottom of the rectifiers eye diagram. \( E_h \) and \( E_l \) are the detected results. At the beginning, \( V_{th} \) and \( V_{tl} \) are reset to supply voltage \( V_{dd} \) and ground voltage \( V_{ss} \), respectively.

In the initial state, \( V_{th} \) is higher than the top of the rectifiers eye diagram, and should be decreased. \( V_{tl} \) is smaller than the bottom of the rectifiers eye diagram, and should be increased. To determine when the \( V_{th} \) and \( V_{tl} \) reaches the top or bottom, the last 200 bits \( E_h \) or \( E_l \) are added. Take the \( E_h \) as an example, \( E_h \) is 0 when the rectifiers result is less than \( V_{th} \). If the sum is more than 0, it means the \( V_{th} \) is less than the maximum of the rectifiers result. As \( V_{th} \) decreased, the sum will increase until \( V_{th} \) reaches the top of the eye diagram.

At this time, 50% of the rectifiers results are higher than \( V_{th} \), and 50% are less, and the sum is 100. Actually, the probabilities of high and low levels may be not equal. Thus, the \( V_{th} \) may be wrong when 50% ones are detected. In this work, \( V_{th} \) is determined when sum is around 80 (40%), and \( V_{tl} \) is determined when sum is around 120 (60%). Fig. 9 shows the flow of the eye detection. The threshold voltage \( V_t \) is the average of \( V_{th} \) and \( V_{tl} \). Fig. 10 shows the threshold adaptation step. At the end of the adaptation step, \( V_{th} \) is placed at the top, \( V_{tl} \) is placed at the bottom, and \( V_t \) is placed in the middle of the rectifiers eye.

6. Simulation Results

The PAM4 receiver was designed in 55-nm CMOS technology. PAM4 signal generator generates data that passes a channel with 4.4 dB of loss at 14 GHz. Fig. 13(a) shows the eye diagram of input signal and Fig. 13(b) shows the eye
diagram of CVSC when the DFE is off. Figs. 13(c) and 13(d) show eye diagrams of the summer and CVSC, respectively. Fig. 13(e) and Fig. 13(f) show the eye diagram of MSB and LSB output. Fig. 13(g) shows the eye diagram of the rectifier. The eye heights shown in Fig. 13(c) are 223 mV, 256 mV, and 226 mV; those of Fig. 13(d) are 329 mV, 395 mV, and 325 mV. The peak-peak jitter of MSB and LSB are 4.74 ps and 8.68 ps, respectively.

With a 1.2 V supply, the total power consumption of the proposed device is 83.5 mW, and Fig. 11 is the power breakdown. The layout (without the digital circuit) is shown in Fig. 12 and the total area is 0.2*0.1 mm$^2$. There are 4 CVSCs in total and the area of each CVSC is only 10*10 μm$^2$. The CVSC occupy 0.5% percent of the area and 11.36% percent of the power. Compare with other circuit, the area of CVSC is much smaller.

A performance comparison is given in Table II. Reference [15] and [22] are conventional 3-comparator structures each with a 1-tap DFE. The proposed device consumes less power than both and even less power as the DFE tap increases. The power consumption of reference [25] is relatively low, but it does not have a DFE and its data rate is slow. Compared with similar structures, the proposed structure performs well while consuming less power.

Fig. 11. Power breakdown

Fig. 12. Layout (without the digital circuit)

7. Conclusion

This paper proposed a novel 56-Gbps PAM4 receiver design. Based on amplitude-rectification, a reduced number of comparators are applied to reduce the power consumption of the receiver. A common-mode voltage stabilization circuit is introduced to minimize the effect of common-mode level changes. When realized on a 55 nm process with 1.2 V supply, the power consumption of the proposed receiver is 83.5 mW and the area is 0.2*0.1 mm$^2$.

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Table II. Performance Comparison

| Function          | Process (nm) | Data rate (Gb/s) | Channel loss (dB@Nyquist) | Power (mW) | Power efficiency (pJ/bit) | Area (mm²) |
|-------------------|--------------|-----------------|---------------------------|------------|--------------------------|------------|
| CTLE+ DFE         | 40           | 56              | 2                         | 240        | 4.29                     | 1.6*       |
| CTLE+ DFE         | 65           | 32              | 23*                       | 80         | 2.5                      | 0.16       |
| CTLE+ DFE +CDR    | 28           | 24              | 3                         | 4         | 1.38                     | 0.024      |
| Decoder+ ILO      | 55           | 56              | 4.4                       | 33         | 1.49                     | 0.02       |

* Including 2-tap TX FFE equalization
** Including CDR

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