Dc-link current computational methods for three-phase inverter with low-order harmonic output current

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Abstract: Both the spectral analysis and the closed-form root-mean-square (RMS) equations are widely used to determine the three-phase inverter dc-link current for capacitor rating proposed. However, the analytical models of the dc-link currents have rarely been reported for applications like the active power filter, where ac currents are mostly low-order harmonics (LOHs). This paper first derived expressions for each dc-link LOH current, in order to compute the capacitor losses for each LOH frequencies. Then, it is shown that the derivation of the dc-link switching harmonic current (SHC) RMS equation is very much complicated when LOHs are present in the ac currents. Hence, new set of generalised RMS equations were successfully derived and simplified into one equation to facilitate the worst case design. The design case of the dc-link current is demonstrated with the proposed equations. A flexible grid-tied inverter lab prototype is developed to inject arbitrary combinations of LOH currents of different orders, sequences, amplitudes and angles into the grid. Good match between the computational and experimental results validates the proposed methods.

1 Introduction

A key design factor of the three-phase voltage source inverters (VSIs) system is the dc capacitors rating. The dc-link current of VSIs with three-phase sinusoidal ac currents has a dc component, switching harmonics ($f_{sw}$, $2f_{sw}$, …) and its sideband components [1–4]. The harmonic currents absorbed by the dc capacitors produce the power losses over the capacitor Equivalent Series Resistance (ESR), and the resulting heat could exceed the capacitor thermal limits and shorten its life expectation.

The dc-link current is in high frequency pulsed forms as the superposition of currents in the three upper phase legs of VSI [5, 6]. Among the analytical methods proposed [1–4, 7–11], double Fourier series analysis is widely used to generate the full spectrum of all the harmonics in the dc-link current and a general method to analyse the dc-link current spectra for most types of inverters was proposed in [2], where each frequency component needs to be individually obtained to compute the capacitor losses. In practical design cases, the capacitors ESR (electrolytic or film) at the pulse width modulated (PWM) switching frequencies almost remains constant [12–14]. Therefore, only one root-mean-square (RMS) equation for the dc-link switching harmonic currents (SHC) is needed [1, 7–11], where the dc-link current RMS value is expressed in terms of the modulation index, power factor and the amplitude of the output current. As the inverter output voltage is a PWM voltage, the output current also contains SHC ripples, whose impacts to the dc-link current RMS value are also investigated. In [7], the dc-link current RMS value is derived by Fourier analysis for the three-phase inverter. Herein, it is discovered that the SHC ripples impacts can be neglected when they are <0.3 times of the rated output ac current. Paper [8] demonstrates that the SHC ripples have very limited influence on dc-link current by numerous simulations. In [9, 10], the dc-link current RMS closed-form expression is directly derived and it is also shown that there is only about 10% error by neglecting the large SHC ripples in the output ac current. In [15], the dc-link voltage ripple is analysed for three-phase VSIs. In [11], the dc-link current and voltage ripple are analysed considering the antiparallel diode reverse recovery spikes. It is concluded that the error caused by this practical complication is only 2%.

So far, almost all attempts to derive the spectra or RMS value of the dc-link current assume sinusoidal three-phase ac currents. However, for many applications like the active power filter (APF), multiple low-order harmonics (LOHs) are present in ac currents and the dc-link current envelopes and patterns are totally different and more complicated to analyse. Very few studies are reported [16, 17] so far. Pei et al. [16] dealt with the unbalanced ac currents at the fundamental frequency. Therein, overall RMS values are obtained by integrating the dc-link current expression within each switching cycle over one sector, and the dc-link LOH current is obtained in the same process. Initial investigation into the dc-link current under non-linear (including unbalanced) loads was made in [17] using spectral analysis, where it was stated that if each spectral component in ac output voltages and currents including switching components are enumerated, each dc-link SHC and LOH current could be obtained. However, to enumerate spectral components of the PWM voltages, double Fourier series analysis has to be performed for each different modulation strategy being used, as it alters the spectral distribution of the voltage and the dc-link current. Meanwhile, as aforementioned, for many practical design cases, the SHC RMS value is sufficient and this value actually stays constant with different modulation strategies.

This paper proposes quantitative equations set to compute the dc-link current for the capacitors rating design in three-phase VSIs applications with LOHs in the ac currents. In Section 2, the basic circuit operation and the dc-link current models are introduced together with the capacitor design aspects and power losses model. In Section 3, the LOH currents in the dc-link are formulated with an instant power based method in synchronous reference frames. Then, the LOH voltages and its maximum value are also formulated. The method simplifies the lengthy trigonometric derivation as in the power computation with three-phase quantities. With a given set of LOH ac currents, the individual dc-link LOH currents are obtained to compute the capacitor power loss for each LOH frequencies with their different capacitor ESR. In Section 4, it is shown that the derivation of the dc-link SHC RMS equation is very much complicated when LOHs are present in the ac currents. Then, the new generalised SHCs RMS equations are successfully formulated, which are also compatible with the equations in prior art when dealing with sinusoidal ac currents. For worst case rating design, the full range of the phase angles of the given LOHs in ac currents is considered.

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currents must be considered, since they bring up infinite amount of dc-link current patterns and corresponding RMS values. Therefore, the proposed equations are successfully simplified to facilitate the worst case rating design and then demonstrated with quantitative examples. Finally, Section 5 shows a flexible grid-tied inverter prototype developed to inject arbitrary combinations of LOH currents of different orders, sequences, amplitudes and angles into the grid. The dc-link current is measured in specially designed laminated busbars. Thorough experiments are performed and validate the results from the proposed computational methods, and the differences between the experiment and computation results are formulated and explained definitely.

2 Basic analytical models of the dc-link current

2.1 Circuit description and basic operations

The typical circuit diagram of the three-phase VSI applications is as shown in Fig. 1. Therein, the inverter is connected to the grid through an LCL filter. Without a neutral line, the sum of the three-phase currents is zero. The inverter is supplied by either a stable dc source or simply a capacitor bank for APF applications. \( C_{dc} \) is the dc-link capacitor. \( T_{a1} - T_{a2} \) are six switches with antiparallel diodes. Slight differences between the fundamental frequency component of the inverter PWM output and the grid voltages are applied over the LCL filter inductance to control the ac currents into or from the grid, where the SHC are absorbed by the LCL capacitors, and the desired fundamental frequency (\( \omega_1 \)) currents or LOH currents (5\( \omega_1 \), 7\( \omega_1 \), etc.) in an APF flow to or from the grid.

Other three-phase VSI applications such as UPS and motor drives use LC types of output filters. As long as ac current ripples are much smaller than the fundamental component, the analytical methods for the dc-link current are the same.

2.2 Dc-link current models

As illustrated in Fig. 1, the dc-link current is the sum of the products of each phase current and its switching state as expressed by

\[
i_d = S_a i_a + S_b i_b + S_c i_c
\]

where the switching state \( S_j \) (\( j = a, b, c \)) equals to 1 or 0, respectively, when switch \( T_j \) is on or off; and the phase currents can be obtained by inverter transfer function and filter impedance [18].

Modulation techniques, such as Sinusoidal Pulse Width Modulation (SPWM), Space Vector Pulse Width Modulation (SVPWM), Discontinuous Pulse Width Modulation (DPWM), Nearest Adjacent Vector Pulse Width Modulation (NSPWM), and so on, have different zero vector placement and different patterns of the piecewise dc-link current over one switching period, so it alters both the SHCs spectrum and the dc-link voltage ripple amplitudes. As discussed in [19], the dc-link SHC’s RMS values are the same for different modulation strategies. In this paper, the SVPWM is used in all the subsequent derivation process.

2.3 Dc-link impedance impacts

The dc-link impedance has effects on the harmonic current distribution between the dc capacitors and front end. The typical three-phase VSI with the LOHs in ac currents considered in this paper is the APF system. As the APF system has only capacitors in the dc-link, the dc-link currents are the same as the capacitor currents, no matter what impedances the dc-link and the capacitors might have.

As for the dc-link harmonic current distribution in between multiple power stages, for example, in energy storage applications, the inverter is fed by the battery pack. Herein, it is to be verified that the capacitor bank impedance is much lower than that of the battery pack at high frequencies to absorb most of the dc-link harmonic currents as [3].

Moreover, the dc-link impedance effects on the dc-link current distribution were usually not considered or discussed in the literature. Nearly all the reference papers [1, 2, 7–10, 16] discussing dc-link currents or voltage ripples do NOT have dc-link impedance discussion. They all use the simple assumption that the capacitor currents are equal to the dc-link harmonic currents. As stated in [16], a well-designed dc-link capacitors bank needs to absorb most of the harmonic components.

The dc-link LOH currents distribution mechanism is a much more complicated issue. In some applications with multi-stages power conversion [20, 21], the dc-link and capacitors impedances are to be considered to quantify the dc-link LOH currents distribution. However, the LOH currents distribution are dominated by multiple layers of control loops, which effectively alters the output impedance of the front end of the dc-link. However, these discussions are beyond the scope of the paper.

2.4 Capacitor design goals and power losses

In a typical dc voltage source design with strict voltage output tolerance, the voltage ripple would obviously be the primary design goal. However, in the industrial design practice of the inverter applications, the dc capacitor voltage ripple is usually the secondary design goal. Given the dc-link harmonic currents, the primary design goal is usually the thermal margin, which has to be satisfied with the proper capacitor losses, current ratings and the corresponding capacitance. Then the secondary goal is to verify that the capacitor selected in the first round of design is sufficient to keep the voltage ripple within certain limits. This is particularly relevant when the output currents have LOHs. Note that the inverter modulator has the dc voltage feedbacks, so that the output ac voltage can be accurately synthesised even with certain voltage fluctuation. Therefore, the dc voltage tolerance here is much looser than in a dc voltage source. Still, the voltage ripple limit should at least maintain the least sufficient dc voltage to synthesise the ac output voltage.

As for the primary design goal, the power losses are to be limited to get sufficient thermal margin. The power losses \( P_{C, loss} \) are directly related to the dc currents in steady state [1–4, 7–10]

\[
P_{C, loss} = I_{C, rms}^2 R_{ESR}
\]

where \( R_{ESR} \) represents the capacitor ESR resistance, and \( I_{C, rms} \) is the capacitor current RMS value. A typical ESR versus frequency curve [12–14] is shown in Fig. 2. It is clear that the capacitor ESR stays almost constant with the frequencies >1 kHz and varies greatly at the frequencies below 1 kHz. Therefore, the capacitor power dissipation in (2) can be rewritten as

\[
I_{C, rms}^2 R_{ESR} = \sum_{f=f_1}^{1 kHz} I_{C, rms}(f) R_{ESR}(f) + \sum_{f > 1 kHz} I_{C, rms}(f) R_{ESR}(f)
\]

where the first term and second term in (3) represent the power losses caused by the individual LOH currents and overall SHC RMS value in the dc-link, respectively.
3 Calculation of the dc-link LOH currents and voltages

3.1 Dc-link low-order harmonic currents

As the capacitor ESR varies significantly with the frequencies <1 kHz, the individual dc-link LOH current should be obtained to compute the power losses per harmonic order. A straightforward derivation process is proposed here to formulate the dc-link LOH currents induced by LOH or negative sequence currents on the ac side.

The ac side instantaneous power is expressed with the $d$-$q$ quantities in the synchronous reference frame as

$$p_{ac} = \frac{3}{2}(v_d i_d + v_q i_q)$$  \hspace{1cm} (4)

The full expressions of three-phase voltages contain the LOH voltages and the full spectra of the switching harmonic voltages $v_{low\_harm}$ ($i = a, b, c$). The voltage equations after the $d$-$q$ transformation are expressed as

$$\begin{align*}
v_d &= \frac{V_d}{\sqrt{2}} \left[ M_d \cos(\phi_i + \frac{\pi}{2}) + \sum_{k=1}^{K} M_d \cos[k(1-\omega)t - \phi_i(n)] \right] \\
   &= \frac{V_d}{\sqrt{2}} \left[ -\sum_{n=1}^{M} M_d \cos[(n+1)\omega t - \phi_i(n)] + 2v_{low\_harm} \right] \\
   &= \frac{V_d}{\sqrt{2}} \left[ -M_d \sin(\phi_i) + \sum_{n=1}^{M} M_d \sin[(k-1)\omega t - \phi_i(n)] + 2v_{low\_harm} \frac{V_d}{v_c} \right] \\

v_q &= \frac{V_q}{\sqrt{2}} \left[ M_q \cos(\phi_i) + \sum_{k=1}^{K} M_q \cos[k(1-\omega)t - \phi_i(n)] \right] \\
   &= \frac{V_q}{\sqrt{2}} \left[ -\sum_{n=1}^{M} M_q \cos[(n+1)\omega t - \phi_i(n)] + 2v_{low\_harm} \frac{V_q}{v_c} \right]
\end{align*}$$  \hspace{1cm} (5)

where $M_d^+$ and $M_q^+$ are the $M$-indexes of the harmonic of different sequence and order as defined by

$$M_d = \frac{2V_d}{v_c}, \quad M_q = \frac{2V_q}{v_c} \hspace{1cm} (6)$$

In (5) and all the subsequent equations, the superscript ‘+$’ and ‘$-$’ represent the positive and negative sequence, and their respective harmonic orders are defined by the subscripts ‘$k$’ and ‘$n$’. $e_{ac}$ is the first positive sequence voltages on the grid side and $\omega t$ is its phase angle. $\phi_i$ ($i = n$ or $k$) is the phase angle between the 4th or $n$th harmonic and $e_{ac}$. As the inverter output voltage and $e_{ac}$ are not exactly in phase, $\phi_i$ represents this tiny phase difference.

When the grid voltages have LOH distortions, a properly designed closed-loop controller of a grid-tied inverter outputs same amount of voltage harmonics in order to keep sinusoidal grid side currents. In APF applications, the current regulators add small amount of additional LOHs into the modulation signals to produce the required harmonic ac currents. As for the inverter filter inductance voltage drops, there are design rules such as in [22, 23], where it is defined that a regular grid-tied inverter allows the inductance voltage drop at fundamental frequency <10%. The same rule is also applicable in an APF system. Therefore, compared to the fundamental frequency voltages output of a grid-tied inverter or APF, which are close to the grid voltages, the LOH voltages needed to cancel out the grid side low-order voltage harmonics or induce the LOH currents over the filter inductances are negligible.

By neglecting the LOHs in (5) and $\phi_i$, which is close to zero, the $d$-$q$ voltage could be simplified as

$$\begin{align*}
v_d &= \frac{V_c}{\sqrt{2}} M_d + v_{low\_harm} \\
v_q &= v_{low\_harm}
\end{align*}$$  \hspace{1cm} (7)

Unlike the voltages, the LOHs in ac currents could not be neglected as they are the dominant components in applications like the APF. Instead, current ripples (or SHC) are negligible in the ac current expressions as defined by

$$\begin{align*}
i_d &= \sum_{k=1}^{K} I_d \sin(\omega t - \phi_i(n)) + \sum_{n=1}^{M} I_n \sin(\omega t - \phi_i(n)) \\
i_q &= \sum_{k=1}^{K} I_d \cos(\omega t - \phi_i(n)) + \sum_{n=1}^{M} I_n \cos(\omega t - \phi_i(n)) \\
i_k &= \sum_{k=1}^{K} I_d \sin[(k-1)\omega t - \phi_i(n)] + \sum_{n=1}^{M} I_n \sin[(n+1)\omega t - \phi_i(n)] \\
i_q &= \sum_{k=1}^{K} I_d \cos[(k-1)\omega t - \phi_i(n)] + \sum_{n=1}^{M} I_n \cos[(n+1)\omega t - \phi_i(n)]
\end{align*}$$  \hspace{1cm} (8)

By substituting (7) into (4), the complete expression of instantaneous power on inverter ac side is obtained as

$$p_{ac} = \frac{3}{4} v_i M_d i_d + \frac{3}{4} v_{low\_harm} i_d + v_{low\_harm} i_q \hspace{1cm} (10)$$

The dc side instantaneous power could be seen as equal to (10) without considering power losses of the inverter. Hence, by dividing $v_i$ from (10), the dc-link current is expressed as

$$i_{dc} = \frac{3}{4} M_d i_d + \frac{3}{4} v_{low\_harm} i_d + v_{low\_harm} i_q \hspace{1cm} (11)$$

The first term in (11) represents the dc-link LOH currents, which is the projection of three-phase currents onto the $d$-axis with a coefficient of $3M_d^+/4$. So if ac currents are unbalanced and/or have LOHs, $i_d$ and $i_q$ are no longer constant and have a series of sinuosoids at various frequencies as in (9).

The $v_{low\_harm}$ and $v_{low\_harm}$ in the second term of (11) represent the full spectra of the switching harmonic voltages in $d$-$q$ reference frame. As spectra details of the dc-link SHC are not needed for capacitor loss computation, they will not be expanded for further derivation. By substituting (9) into the first term of (11), the LOH currents in the dc-link become

$$i_{dc\_low\_harm} = \frac{3}{4} M_d \left[ \sum_{k=1}^{K} I_d \cos[(k-1)\omega t - \phi_i(n)] - \sum_{n=1}^{M} I_n \cos[(n+1)\omega t - \phi_i(n)] \right] \hspace{1cm} (12)$$

The reason for the power expression derivation in the $d$-$q$ reference frame is that it needs no trigonometric derivation. Only (4) and (7) are needed to express (11), into which (9) is to be substituted. Note that if (9) was derived from (8) by the normal $d$-$q$ transformation, it would have gone through the same lengthy process as in the stationary reference frame. However, by easy visualisation of the rotating vectors of the harmonics being projected onto the synchronous reference frame as in [24], (9) could be directly rewritten from (8).

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880

IET Power Electron., 2019, Vol. 12 Iss. 4, pp. 878-890

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The three-phase APF design requirements include a group of the LOH currents to be injected into the grid. According to (12), the ac side $k$th positive and $n$th negative sequence currents induce the $(k-1)$th and $(n+1)$th currents in the dc-link. Instructively, if $k-n=2$, the vectors of the $(k-1)$th and $(n+1)$th dc-link LOH currents add up, which could either cancel out ($\varphi_+^k=\varphi_-^n$) or reinforce ($|\varphi_+^k-\varphi_-^n|=\pi$) each other. For example, when ac currents have the $-1$st, $-5$th, $+7$th, $-11$th harmonics, the $2$nd, $6$th, $12$th harmonic currents show up in the dc-link.

For verification of (12), $k$ is set as $1$ and the average dc-link current expression could be written as

$$I_{dc\_avg} = \frac{3}{4} M_1' \cos(\varphi_t')$$

which matches (6) in [1].

Due to the frequency-dependent ESR characteristics, the overall RMS expression of the dc-link LOH currents (including the average dc value) is not suitable for calculating the capacitor losses. However, it is needed to derive the dc-link SHC RMS value as in Section 6. So, it is obtained from (12) as

$$I_{dc\_LOH} = \frac{3}{4} M_1' (\cos(\varphi_t') + \sum_{k=1}^n \sum_{k+n=2}^n |I_k \sin(\varphi_k - \varphi_n)|)$$

where the fourth term under the square root sign represents the vector sum of the $(k-1)$th and $(n+1)$th dc-link LOH currents, when $k-n=2$.

3.2 DC-link low-order harmonic voltages

According to the Kirchhoff’s Current Law (KCL) law and Fig. 1, the capacitor current can be written as

$$i_{cap} = i_{dc} - i_{dc\_LOH}$$

(15)

As the impedance of the capacitor is infinity for the dc frequency, the average component of $i_{dc\_LOH}$ is totally provided by the dc front-end current $i_{DC}$. Also as discussed previously, the dc-link capacitor absorbs almost all the harmonic components (including LOHs and SHCs) in the dc-link. Then, the dc capacitor current can be rewritten as

$$i_{cap} = -i_{dc\_LOH} - i_{SHC}$$

(16)

The resulting dc-link voltage ripple is calculated as

$$\Delta v_c = \frac{1}{C_{dc}} \int_{t} i_{cap} dt = \frac{1}{C_{dc}} \int (-i_{dc\_LOH} - i_{SHC}) dt$$

$$= \Delta v_c\_LOH + \Delta v_c\_SHC$$

(17)

Obviously, the dc-link voltage ripples have both the LOH $\Delta v_c\_LOH$ and switching harmonic components $\Delta v_c\_SHC$. As the integral time of switching harmonic voltage is far less than the LOH voltage, the LOHs are the dominating component in the dc-link voltage and the switching harmonic voltage can be safely neglected.

As the $i_{dc\_LOH}$ represent LOH currents in the dc capacitors current, it does not have the dc average component as in (12). The $i_{dc\_LOH}$ is expressed as

$$i_{dc\_LOH} = \frac{3}{4} M_1' \left[ \sum_{k=1}^{n} I_k \cos[(k-1)\omega_0 t - \varphi_k^-] \right. - \left. \sum_{n=1}^{k} I_n \cos[(n+1)\omega_0 t - \varphi_n^+] \right]$$

(18)

Then the LOH voltage in dc-link can be obtained by the integral of (18) as

$$\Delta v_c\_LOH = \frac{3}{40} M_1' \left[ \sum_{k=1}^{n} \frac{I_k}{k-1} \sin[(k-1)\omega_0 t - \varphi_k^-] \right. - \left. \sum_{n=1}^{k} \frac{I_n}{n+1} \sin[(n+1)\omega_0 t - \varphi_n^+] \right]$$

(19)

Obviously, the LOH voltage is independent of the modulation strategies. As the $\varphi_k^+$ and $\varphi_n^-$ are independent variables, the maximum value of the LOH voltage ripple $\{\Delta v_c\_LOH\}_{max}$ is

$$\{\Delta v_c\_LOH\}_{max} = \frac{3}{40} M_1' \left[ \sum_{k=1}^{n} \frac{I_k}{k-1} + \sum_{n=1}^{k} \frac{I_n}{n+1} \right]$$

(20)

4 Derivation and application of RMS expressions of the dc-link SHCs

4.1 DC-link current envelopes under low-order harmonics in ac currents

As illustrated in Fig. 3a, when the ac currents are sinusoidal and balanced, the dc-link current switching pulses has a cyclic pattern with a period of $\pi/3$. The way to derive the SHCs RMS value [1, 7, 8] is to express the RMS value of a switching cycle, and integrate it over a period of $\pi/3$ as

$$I_{dc\_RMS} = \left( \frac{1}{\pi/3} \int_{0}^{\pi/3} \left( \tilde{i}_d t_{d+1} + \tilde{i}_d t_{d-1} \right) dt \right)$$

(21)

The RMS values from (21) include the contributions from both the dc average value and PWM switching harmonics. However, (21) is no longer valid, as the LOHs in the ac currents reshape the dc-link current patterns significantly. Figs. 3b–d show the various patterns of the dc-link currents, when ac currents contain the $-1$st component, the combination of the $+1$st and $-4$th harmonics, and the combination of the $-5$th and $+7$th harmonics, respectively. Their repetitive periods are $\pi$, $2\pi$ and $3\pi$. Considering all possible LOHs combinations in ac currents, the RMS expression of the dc-link current per switching cycle should be integrated over a fundamental cycle of $2\pi$. 
4.2 RMS value of the dc-link switching harmonic currents

Eq. (26) could be further simplified by eliminating the second term, when \( n = 3m - 1 \) (\( m = 1, 2, \ldots \)).

The third part of (24) stems from any two positive sequence LOHs \((k_1\text{th} \text{ and } k_2\text{th})\) in ac currents as defined by (see (27)) . Only when \( k_1 + k_2 = 6m + 2 \) (\( m = 1, 2, 3, \ldots \)) or \( k_1 - k_2 = 6m \) (\( m = 1, 2, 3, \ldots \)), (27) has non-zero values.

The fourth part of (24) stems from any two negative sequence LOHs \((n_1\text{th} \text{ and } n_2\text{th})\) in ac currents as defined by (see (28)) . Only when \( n_1 + n_2 - 6m - 2 \) (\( m = 1, 2, \ldots \)) or \( n_1 - n_2 = 6m - 1 \) (\( m = 1, 2, \ldots \)), (28) has non-zero values.

The fifth part of (24) stems from any pair of a positive and negative sequence LOH \((k_1\text{th and } n_2\text{th})\) in ac currents as defined by (see (29)) . Only when \( k-n = 6m - 4 \) (\( m = 1, 2, \ldots \)) or \( k+n = 6m \) (\( m = 1, 2, \ldots \)), (29) has non-zero values.

It should be noted that (24)–(29) represent the overall RMS values including dc average, LOHs and switching harmonics in the dc-link current. To obtain the RMS value of SHC, (14) needs to be eliminated from (24) as

\[
I_{dc_{\text{switch RMS}}} = \sqrt{I_{dc_{\text{RMS}}}^2 - I_{dc_{\text{low RMS}}}^2} \tag{30}
\]

Equations (24)–(30) are a complete set of generalised tools to analytically obtain the RMS value of the dc-link SHC.

4.3 Equations compatibility with special cases

Equations (24)–(29) could be very much simplified when applied to special cases, such as grid-tied inverter applications, where only the first-order positive sequence component exists in ac currents. By setting \( k = 1 \) in (25), the resulting dc-link current RMS value expression as in (31) exactly matches (7) in [1]

\[
I_{dc_{\text{RMS}}} = I' \sqrt{\frac{3M_0^2}{4\pi} + \frac{3M_1^2 \cos(2\phi)}{2\pi}} \tag{31}
\]

### Table 1

| Vector | \( V_1 \) | \( V_2 \) | \( V_3 \) | \( V_4 \) | \( V_5 \) | \( V_6 \) | \( V_7/V_6 \) |
|--------|----------|----------|----------|----------|----------|----------|-------------|
| \( i_{dc} \) | \( i_a \) | \(-i_c \) | \( i_b \) | \(-i_a \) | \( i_c \) | \(-i_b \) | 0 |

Equation (22) gives the relationship between the dc and ac currents for each grid voltages is usually aligned with the \( d \)-axis and the phase angle \( \alpha_{It} \) of the reference vector \( V_s \) is defined in Fig. 4.

Figure 4 shows the vector space of a three-phase VSI, and Table 1 expression is formulated by (24)–(29). The RMS result as in (24) has five parts, which is further defined by (25)–(29)

\[
I_{dc_{\text{RMS}}} = \sum_{n_1,n_2} (I_{dc_{\text{RMS}}}^2) + \sum_{k=1} I_{dc_{\text{RMS}}}^2 + \sum_{k=1} I_{dc_{\text{RMS}}}^2 \tag{24}
\]

The first part of (24) stems from the \( k \text{th} \) positive sequence harmonic in ac currents as defined by

\[
(U_{dc_{\text{RMS}}}^2) = \frac{3\sqrt{3}M_1^2}{4\pi} - \frac{3\sqrt{3}M_1^2}{4\pi} \cos(2\phi k) \times \left[-2\cos\left(k - 1\right) + (-1)^k\right] \tag{25}
\]

The second part of (24) stems from any negative sequence harmonic in ac currents as defined by

\[
(U_{dc_{\text{RMS}}}^2) = \frac{3\sqrt{3}M_1^2}{4\pi} - \frac{3\sqrt{3}M_1^2}{4\pi} \cos(2\phi k) \times \left[-2\cos\left(n + 1\right) + (-1)^n\right] \tag{26}
\]

Equation (25) could be further simplified by eliminating the second term, when \( k \neq 3m - 2 \) (\( m = 1, 2, \ldots \)).

The fourth part of (24) stems from any sequence LOH in ac currents as defined by (see (27)) . Only when \( k_1 + k_2 = 6m + 2 \) (\( m = 1, 2, 3, \ldots \)) or \( k_1 - k_2 = 6m \) (\( m = 1, 2, 3, \ldots \)), (27) has non-zero values.

The fifth part of (24) stems from any pair of a positive and negative sequence LOH \((k_1\text{th and } n_2\text{th})\) in ac currents as defined by (see (29)) . Only when \( k-n = 6m - 4 \) (\( m = 1, 2, \ldots \)) or \( k+n = 6m \) (\( m = 1, 2, \ldots \)), (29) has non-zero values.
where the second term under the square root symbol is obtained by (29). Therefore, the overall dc-link current RMS expressions (24)–discovered that most of the phase angle dependent terms in (25)–

In an APF design, a set of ac side LOHs amplitudes are usually considered. The dc-link current RMS is derived by setting $k=1$ and $n=1$ in (25), (26) and (29). The resulting (32) exactly matches the (27) in [16]

Therefore, simplifications are made here to facilitate the design practice.

**4.4 Equations simplification for practical design**

In an APF design, a set of ac side LOHs amplitudes are usually given as requirements. However, it is impractical trying to obtain the worst case RMS value of the dc-link SHC and LOH currents by traversing the full range of phase angles of each individual LOH. Therefore, simplifications are made here to facilitate the design practice.

**4.4.1 SHC RMS simplification for the worst case:** It is discovered that most of the phase angle dependent terms in (25)–(29) are negligible due to their overwhelmingly large denominators, except for the cases when $k=1$ in (25) or $k-n=2$ in (29). Therefore, the overall dc-link current RMS expressions (24)–(29) can be simplified by eliminating all the terms with phase angles in (26)–(28), the resulting equation is

\[
I_{\text{dc,RMS}} = \sqrt{\sum \frac{3 \sqrt{3} M_1^2 (I_1)^2 + \sum (I_n)^2}{4\pi} + \frac{3 \sqrt{3} M_1^2 (I_1)^2 \cos(2\varphi_n)}{4\pi}}
\]

By removing the RMS values of the LOHs and the dc average as defined by (14), the simplified RMS expression of the dc-link SHC could be obtained from (34) as

\[
I_{\text{dc,switchRMS}} \approx \sqrt{\frac{3 \sqrt{3} M_1^2}{4\pi} + \sum \frac{9 (M_1)^2}{32} (I_1)^2 + \sum (I_n)^2} + \frac{\sqrt{3} M_1^2 (I_1)^2 (\frac{\sqrt{3} M_1^2}{4\pi} + \cos(\varphi_1)^3 (\frac{\sqrt{3} M_1^2}{4\pi} - \frac{9 M_1^2}{16}) - M_1 (\frac{\sqrt{3} M_1^2}{4\pi} - \frac{9 M_1^2}{16}) \sum_{k-n=2} I_k T_k \cos(\varphi_k - \varphi_n)}{4\pi}}
\]

where the third term only exist when the LOHs in ac currents come in pairs and satisfy $k-n=2$. When this does occur, $I_{\text{dc,switchRMS}}$ would vary noticeably with the phase angles. For practical design, only its maximum value is actually needed. Herein, once the $M$-index or dc voltage is given, the maximum $I_{\text{dc,switchRMS}}$ is obtained if the third term in (34) satisfies $\varphi_1 = \varphi_n$, or $0.98 < M_1 < 1.15$ or $|\varphi_1 - \varphi_n| = \pi$. Hence, the maximum $I_{\text{dc,switchRMS}}$ is derived from (34) as

\[
I_{\text{dc,switchRMS}} \approx \frac{3 \sqrt{3} M_1^2}{4\pi} \sum \frac{(I_1)^2 + \sum (I_n)^2}{4\pi} \times [3 + 2\cos(2\varphi_1) - \frac{\sqrt{3} M_1^2}{\pi} \sum_{k-n=2} I_k T_k \cos(\varphi_k - \varphi_n)}
\]
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Fig. 5 Comparison of the maximum values of the angle dependent terms of the SHC’s RMS and LOH currents RMS

Fig. 6 Capacitor power losses worst case design flow chart

\[ I_{\text{dc, switch RMS max}} = \frac{3\sqrt{3}M_1^2}{4\pi} - \frac{9M_1^4}{32} \sum_{n=2} (U_n)^2 + \sum_{n=1} (U_n)^2 \]

\[ = M_1^4 \left[ \frac{3\sqrt{3}}{4\pi} + \cos(\phi) \left( \frac{3\sqrt{3}}{16} - \frac{9M_1^4}{16} \right) \right] + M_1^4 \left[ \frac{\sqrt{3}}{16} - \frac{9M_1^4}{16} \right] \sum_{n=2} (U_n)^2 \]

\[ \approx \frac{9M_1^2}{32} \] 

\[ (35) \]

Apparently, (35) is very easy to use even for the design cases with a large group of LOHs on the ac side such as the 5th, 7th, 11th, 13th and so on. Obviously, it would be impractical for the conventional methods such as the double Fourier series analysis or numeric simulations to obtain the worst case rating results out of numerous dc-link current patterns varying with the infinite number of combinations of the LOHs phases angles.

4.4.2 LOH currents RMS for the worst case: Besides the dc-link SHC RMS, the individual dc-link LOH currents also need to be considered in the rating of dc-link capacitors. It is clear to see from (12) that the 4th positive and nth negative sequence current on the ac side would induce the LOH current at the same frequency in the dc-link when \( k=n=2 \). The RMS value of their vector sum varies with the LOH phase angles and the worst case is expressed in Table 2. When \( k=n=2 \), the overall RMS values of the \((k-1)\)th and \((n+1)\)th LOH currents in the dc-link are fixed despite their phase angles combinations.

4.4.3 Overall worst case for capacitor power losses with both SHCs and LOH currents RMS: To obtain the overall worst case of capacitor power losses, the RMS values of both the SHCs and LOH currents are to be considered. In (36), the two terms \( I_{\text{SHC Vary}} \) and \( I_{\text{LOH Vary}} \) are extracted from (34) and from Table 2, respectively. Only when the 4th positive and nth negative sequence harmonics \((k-n=2)\) in the ac currents co-exist, the two terms \( I_{\text{SHC Vary}} \) and \( I_{\text{LOH Vary}} \) are non-zero. Moreover, both terms vary with the LOHs phase angles combinations and determine the worst cases of the SHC RMS and LOH currents RMS. For the full M-index range, the worst cases phase angles combinations are listed in Table 3.

\[
\begin{align*}
I_{\text{SHC Vary}} &= M_1^4 \left( \frac{3\sqrt{3}}{16} \right) \sum_{k=1}^{N-2} (U_t^k)^2 + \sum_{n=2} (U_n)^2 \\
I_{\text{LOH Vary}} &= \left( \frac{3M_1^2}{4\pi^2} \right) \sum_{k=1}^{N-2} (U_t^k)^2 - 2\sum_{n=2} (U_n)^2 \cos(\phi_1 - \phi_n)
\end{align*}
\]

\[ (36) \]

From Table 3, it is clear that the RMS values of the SHCs and LOH currents could reach their respective maximum at the same time (when \( |\phi_1-\phi_n|=\pi \)) for the M-index range of \([0, 0.98]\). However, as for the M-index between 0.98 and 1.15, if one reaches its maximum, the other is at its minimum. So to obtain the worst case for capacitor power losses, the maximum values of \( I_{\text{SHC Vary}} \) and \( I_{\text{LOH Vary}} \) are symbolically expressed from (36) and Table 3, and then plotted and compared in Fig. 5. It is clear that the maximum value of \( I_{\text{LOH Vary}} \) (when \( |\phi_1-\phi_n|=\pi \)) is larger than that of \( I_{\text{SHC Vary}} \) (when \( \phi_1 = \phi_n \)). Moreover, the ESR values for LOH frequencies are greater than the ESR value at the switching frequencies. Therefore, the maximum of \( I_{\text{LOH Vary}} \) (when \( |\phi_1-\phi_n|=\pi \)) corresponds to the worst case capacitor power losses when the M-index is between 0.98 and 1.15.

It is then concluded that, for the full M-index range, the worst case for capacitor power losses is always when \( |\phi_1-\phi_n|=\pi \). Fig. 6 shows the flow chart of the worst case design process for the capacitor power losses.

Table 2 RMS value of two dc-link LOHs at the same frequency

| dc-link LOH currents RMS | Maximum RMS value |
|-------------------------|------------------|
| \( \frac{3M_1^2}{4\pi^2} (U_t^k)^2 + (U_n)^2 - 2I_{dc}\cos(\phi_1 - \phi_n) \) | \( \frac{3M_1^2}{4\pi^2} (U_t + U_n) \) |

Table 3 Worst cases of the SHC RMS and LOH current RMS

| Category          | M-index | Worst case angle combinations |
|-------------------|---------|-------------------------------|
| SHC               | 0–0.98  | \( |\phi_1 - \phi_n| = \pi \) |
| 0.98–1.15         |         | \( \phi_n = \phi_1 \)          |
| LOH               | 0–1.15  | \( |\phi_1 - \phi_n| = \pi \) |

\[ \text{Table 2} \] RMS value of two dc-link LOHs at the same frequency

\[ \text{Table 3} \] Worst cases of the SHC RMS and LOH current RMS
Table 4 Requirements of LOHs in ac currents for the worst case design study
| ac currents | case 1 | case 2 |
|-------------|--------|--------|
| (-1st, 15 A), (-5th, 15 A), (+7th, 10 A) | (1st, 20 A) | (+1st, 20 A), (-5th, 15 A) |

Table 5 Requirements of LOHs in ac currents for the comparative case study
| ac currents | case 1 | case 2 |
|-------------|--------|--------|
| +1st, 20 A, -5th, 15 A | (+1st, 20 A), (-5th, 15 A) |

4.5 Practical design case study

In the following two quantitative design case studies of an APF dc-link, the grid line-to-line voltage is 400 V and their requirements of the maximum LOHS in ac currents are shown in Tables 4 and 5, respectively. It should be noted that the phase angle of each LOH in ac currents varies within \([0–2\pi/2] \), while the phase angle of the current of the fundamental frequency and positive sequence is

\[ I_{1+} = 15 \text{ A}, I_{5-} = 15 \text{ A}, I_{7+} = 10 \text{ A} \]

4.5.1 Worst case design study: In this case study, two dc voltages (568 and 700 V) are used to exemplify two cases with different \( M \)-indexes (0.93 and 1.15).

First, the dc-link SHC RMS values \( (I_{dc\_switch\_RMS}) \) are calculated. For comparison, the computation results of the complete equations set (24)–(30) and its simplified form (34) are both plotted in Fig. 8 side by side for the full ranges of phase angles \( (\phi_5^-\) and \( \phi_7^+\)) of the given fifth and seventh harmonics. In Fig. 8b, \( I_{dc\_switch\_RMS} \) dependence on \( \phi_5^- \) and \( \phi_7^+ \) are clear when \( M_1^+ = 1.15 \). In Fig. 8a, \( I_{dc\_switch\_RMS} \) only varies within tiny ranges with the \( \phi_5^- \) and \( \phi_7^+ \), when \( M_1^+ = 0.93 \). In both Figs. 8a and b, it is obvious that the plot contours and peaks from (34) well match those from the complete equations set and the error percentage is below 5%. So that the simplified (34) and its variant (35) is very efficient in obtaining the maximum RMS value of the dc-link SHC out of all possible phase angles of the ac currents LOHs with given amplitudes.

Then, the worst case LOH currents (when \( |\phi_5^- - \phi_7^+| = \pi \)) are computed and listed in Table 6. As explained in Section 4.4.1, when the \( M \)-index 0.93 is within \([0, 0.98]\), the worst case for SHC RMS value (9.04 A) and LOH currents both occur with the same LOHs phase angle combination; when the \( M \)-index 1.15 is within \([0.98, 1.15]\), the phase angle combination with the worst case LOH currents brings up the worst case for the overall capacitor power losses, even though it corresponds to the minimum SHC RMS value (6.36 A).

According to the dc-link LOHs and SHCs in the worst case as in Table 6, the dc-link capacitor bank is designed with 900 V peak rating with two 450 V-rated B43504A5397M000 in series and eight branches in parallel. The normalised capacitor losses at 100, 600 Hz and the switching frequencies for individual capacitors and the capacitor bank are computed and listed in Table 6.

The normalised losses of the capacitor bank and the individual capacitor are computed as 100.83 and 6.30 (\( M_1^+ = 1.15 \)), respectively. While with the maximal permissible current of 4.86 A (peak) at 60°C as given by the datasheet, the allowable normalised individual capacitor loss is 11.81. Hence, there is sufficient design margin under the worst case operation point.

4.5.2 Comparative design case study: In order to better clarify the benefits of the proposed method, two APF dc capacitor design cases are compared. As defined in Table 5, the base case only considers the fundamental frequency component in the ac currents (reactive power compensation), while the comparative case also considers the fifth negative sequence component. In both cases, the maximum values of LOHS and SHCs RMS can be computed according to the design flow path 1 in Fig. 6. The computed results are listed in Table 7.

In case 1, the APF dc-link capacitor rating is only determined by the SHC RMS values. To have sufficient thermal margin, the dc-link capacitors are designed with 900 V peak rating with two 450 V-rated B43504A5397M000 in series and two branches in parallel. From Table 7, it is clear that the normalised losses of the capacitor bank and the individual capacitor are computed as 17.1 and 4.3 in case 1, respectively. While with the maximal permissible current of 4.86 A (peak) at 60°C as given by the datasheet, the allowable normalised individual capacitor loss is 11.81. Hence, there is sufficient design margin under the worst case operation point for case 1. Then the capacitor voltage ripple is verified. The maximum dc-link switching harmonic voltage ripple is only 0.52 V.
However, if the same capacitors are used in case 2, the LOHs in the ac currents not only increase the capacitor power losses significantly, the SHC RMS values are increased as well. The normalised losses of the capacitor bank and the individual capacitor are 52.5 and 13.1, respectively. Therefore, the capacitors designed without considering LOHs would be over-heated and have premature failure. Moreover, it is computed with (18) that, the peak dc voltage ripple is increased from 0.52 to 14.2. Obviously, the proposed method provides more accurate capacitor losses estimation and ratings design, when the output ac currents contain LOHs.

### 5 Experimental validation

To validate the proposed analytical models under any harmonic currents conditions, a flexible three-phase grid-tied inverter prototype is developed in order to freely inject combinations of harmonic currents of different harmonic orders, sequences, phase angles and amplitudes into the ac grid, so that the dc-link current could be conveniently evaluated under any LOH currents, such as an APF compensating a required set of harmonic currents. The experimental setup is as shown in Fig. 9. Therein, three-phase high power density 15 kVA inverter assembly was constructed using multi-layer packaging design. The dc-link current is measured in specially fabricated laminated busbars as in Fig. 9. An easy to use graphic user interface is programmed to control the grid-tied inverter outputs via CAN data-link and monitor its status as in Fig. 10. The dc voltage is set at 570 V. The three-phase grid side voltage after the transformer is set at 240 V. The LCL filter and dc-link capacitor parameters are listed in Table 8.

High-performance closed-loop control based on PI controller paralleled with multiple PR controllers in $d$–$q$ reference frame was implemented and well-tuned to inject the sinusoidal LOH currents into the grid, particularly at the higher harmonic orders. So the accuracy of the dc-link current measurements is not affected by unexpected harmonics. Moreover, the PLL algorithm based on multiple reference frames guarantees the accuracy of the real-time phase angle extraction despite the grid voltage harmonics. The

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**Table 6** Summary sheet of the worst case design study

| Dc-link LOH frequency, Hz | 100 | 600 | >1000 |
|--------------------------|-----|-----|-------|
| single capacitor normalised ESR (ESR/ESR$_{100\,\text{Hz}_{60°C}}$) | 1.0 | 0.46 | 0.33 |
| capacitor bank normalised ESR (ESR/ESR$_{100\,\text{Hz}_{60°C}}$) $\times$ 2/8 | 0.25 | 0.12 | 0.08 |
| $M_1^*$ 0.93 LOH current RMS, A | 10.5 | 17.4 | — |
| SHC RMS, A | — | 9.04 | — |
| normalised capacitor bank loss ($I^2 \times (\text{ESR/ESR}_{100\,\text{Hz}_{60°C}}) \times (2/8)$) | 27.56 | 36.33 | 6.54 |
| total normalised capacitor bank loss | 70.43 | — | — |

| $M_1^*$ 1.15 LOH current RMS, A | 12.9 | 21.6 | — |
| SHC RMS, A | — | 6.36 | — |
| normalised capacitor bank loss ($I^2 \times (\text{ESR/ESR}_{100\,\text{Hz}_{60°C}}) \times (2/8)$) | 41.60 | 55.99 | 3.24 |
| total normalised capacitor bank loss | 100.83 | — | — |

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**Table 7** Summary sheet of the comparative design case study

| Dc-link LOH frequency, Hz | 0 | 600 | >1k |
|--------------------------|---|-----|-----|
| single capacitor normalised ESR (ESR/ESR$_{100\,\text{Hz}_{60°C}}$) | — | 0.46 | 0.33 |
| capacitor bank normalised ESR (ESR/ESR$_{100\,\text{Hz}_{60°C}}$) $\times$ 2/2 | — | 0.46 | 0.33 |
| case 1 LOH current RMS, A | 0 | — | — |
| SHC RMS, A | — | — | 7.2 |
| maximum voltage ripple, V | — | 0.52 | — |
| normalised capacitor bank loss ($I^2 \times (\text{ESR/ESR}_{100\,\text{Hz}_{60°C}}) \times (2/2)$) | — | 17.1 | — |
| total normalised capacitor bank loss | 17.1 | — | — |

| case 2 LOH current RMS, A | 0 | 7.4 | — |
| SHC RMS, A | — | 9.1 | — |
| maximum voltage ripple, V | — | 14.2 | — |
| normalised capacitor bank loss ($I^2 \times (\text{ESR/ESR}_{100\,\text{Hz}_{60°C}}) \times (2/2)$) | — | 25.2 | 27.3 |
| total normalised capacitor bank loss | 52.5 | — | — |
closed-loop control is implemented on a digital signal processor (TMS320F28335). The PWM switching and control loop frequency was set to 10 kHz.

As the simulation results match the experimental waveforms very well, only experimental results are provided to validate the analytical methods. Meanwhile, the oscilloscope data were exported for FFT analysis to compare with the computational results of the LOHs by (12) and SHC RMS values by (24)–(30).

5.1 Experimental results

Groups of LOHs in the ac currents in the experiments are selected according to the practical APF operation, such as compensating the reactive power while cancelling the fifth and seventh harmonics, or compensating negative sequence currents while cancelling LOH currents and so on. Therefore, the following six groups of LOH currents were selected as the output to the grid: (i) $I_{1-1} = 18$ A ($\phi_{1-1} = \pi/2$), $I_{1-2} = 12$ A ($\phi_{1-2} = 0$), $I_{1-9} = 9$ A ($\phi_{1-9} = 0$), $I_{2+1} = 6$ A ($\phi_{2+1} = \pi$), $I_{2+2} = 8$ A ($\phi_{2+2} = 0$), $I_{2+9} = 9$ A ($\phi_{2+9} = 0$); (ii) $I_{1+1} = 12$ A ($\phi_{1+1} = 0$), $I_{1+9} = 9$ A ($\phi_{1+9} = 0$), $I_{1+2} = 6$ A ($\phi_{1+2} = \pi$), $I_{1+6} = 8$ A ($\phi_{1+6} = 0$), $I_{1+3} = 6$ A ($\phi_{1+3} = \pi$), $I_{1+8} = 8$ A ($\phi_{1+8} = 0$), $I_{1+7} = 6$ A ($\phi_{1+7} = 0$), $I_{1+10} = 12$ A ($\phi_{1+10} = \pi/2$), $I_{1+4} = 12$ A ($\phi_{1+4} = 0$), $I_{1+5} = 8$ A ($\phi_{1+5} = \pi/2$), $I_{1+1} = 10$ A ($\phi_{1+1} = 0$), $I_{1+7} = 8$ A ($\phi_{1+7} = 0$).

The oscilloscope data of the six dc-link current shows quite complex and varying patterns in Fig. 11, so that calculating the dc-link SHC RMS values appears to be a daunting task. However, with the proposed equation set, reasonably accurate results are easily obtained, as validated by the lab results in Fig. 12. The comparison of the calculated and experimental results of the dc-link LOH currents is also shown in Table 9. In these two special cases, the LOHs in the dc-link should be even smaller than the reality. From Tables 9 and 10, the differences are safely neglected when the LOH voltages and SHC ripples in the ac currents are considered during the derivation, the inverter output voltage as in (7) and (9) is redefined as

$$V_d = V_d + \frac{\sum_{k=2}^{M} M_i \cos[(k-1)\omega_0 t - \phi_{d,k}]}{2} - \frac{\sum_{n=1}^{M} M_{n} \cos[n \omega_0 t - \phi_{n}]}{2}$$
$$V_q = V_q + \frac{\sum_{k=2}^{M} M_i \sin[(k-1)\omega_0 t - \phi_{d,k}]}{2} + \frac{\sum_{n=1}^{M} M_{n} \sin[n \omega_0 t - \phi_{n}]}{2}$$

where the $i_{\text{low, harm}}$ and $i_{\text{high, harm}}$ represent the SHC ripples in the ac currents. Then the instantaneous power on the inverter ac side is obtained by substituting (37) and (38) into (4) as

$$P_{\text{ac}} = P_{\text{ac}} + \frac{3}{2} i_{\text{low, harm}} + \frac{3}{4} i_{\text{high, harm}}$$

By dividing the dc voltage $V_c$ from (39), the dc-link current can be expressed as in (40).

5.2 Error analysis

Although the experimental results of the dc-link LOH currents and SHC RMS values well matched the computational results, there are still slight differences among them. Tables 9 and 10 list the error percentages between the experimental and computation results for the LOH currents and SHC RMS values, respectively. Note that the total RMS value of all the LOH currents computed with (14) as listed in Table 9 is just used to verify the overall accuracy, instead of being used for capacitor losses computation. It should also be noted that two special cases are labelled as ‘not relevant’ in Table 9. In these two special cases, the LOHs in the dc-link should nearly cancel each other. However, in practical tests, small amount of LOHs exist, due to the non-ideal grid voltages as analysed later in this subsection. Therefore, the LOHs error percentages for the two special cases are not relevant, as the comparison base is too small. Even though the error percentage is well within the design margin, it is very instructive to explain these differences in detail.

The LOHs in the inverter output voltage, SHC ripples in the ac current and power module losses are the three main reasons for these differences. For simplicity, they are safely neglected when establishing the computation models for the dc-link LOH currents and the SHC RMS value.

Suppose that the LOH voltages and SHC ripples in the ac current are considered during the derivation, the inverter output voltage as in (7) and (9) is redefined as

$$V_d = V_d + \frac{\sum_{k=2}^{M} M_i \cos[(k-1)\omega_0 t - \phi_{d,k}]}{2} - \frac{\sum_{n=1}^{M} M_{n} \cos[n \omega_0 t - \phi_{n}]}{2}$$
$$V_q = V_q + \frac{\sum_{k=2}^{M} M_i \sin[(k-1)\omega_0 t - \phi_{d,k}]}{2} + \frac{\sum_{n=1}^{M} M_{n} \sin[n \omega_0 t - \phi_{n}]}{2}$$

Table 8 System parameters

| Description                          | Part number      | Parameters        |
|--------------------------------------|------------------|-------------------|
| filter inductor on the grid side $L_g$ | custom-made      | 200 μH, 30 Arms   |
| filter inductor on the inverter side $L_f$ | custom-made      | 400 μH, 40 Arms   |
| filter capacitor (Y-connected) $C_f$ | MKP1847610354P4  | 10 μF            |
| damping resistor $R_d$               | TEH1000M1RR00JE  | 1 Ω              |
| dc-link capacitor $C_{dc}$          | B435045477M000   | 940μF            |
| IGBT power modules                  | SKiiP 39AC126V2  | 1200 V, 157 A/ch. |
Fig. 11 Experimental results of the dc-link currents under six groups of LOHs in the ac currents

(a) $I_{1^+}=18A$ ($\phi_{1^+}=\pi/2$), $I_{1^-}=12A$ ($\phi_{1^-}=0$), $I_{5^+}=9A$ ($\phi_{5^+}=0$), $I_{7^+}=9A$ ($\phi_{7^+}=0$), (b) $I_{1^+}=12A$ ($\phi_{1^+}=\pi/2$), $I_{5^-}=9A$ ($\phi_{5^-}=0$), $I_{7^-}=9A$ ($\phi_{7^-}=\pi$), (c) $I_{1^+}=12A$ ($\phi_{1^+}=\pi/2$), $I_{5^-}=9A$ ($\phi_{5^-}=0$), $I_{7^-}=9A$ ($\phi_{7^-}=\pi$), (d) $I_{1^+}=12A$ ($\phi_{1^+}=\pi/2$), $I_{11^-}=10A$ ($\phi_{11^-}=0$), $I_{13^+}=8A$ ($\phi_{13^+}=0$)
The fourth and fifth extra components are the fifth and sixth terms in (40), which indicates that LOH voltages introduce additional dc-link LOH currents. The interaction between the 4th positive harmonic voltage and 3rd negative harmonic current or 3rd negative harmonic voltage and 4th positive harmonic current would induce \((k+n)\)th LOH current in the dc-link. The 5th and 6th positive harmonic current would induce \((k_1-k_2)\)th LOH current in the dc-link. The 7th negative harmonic current would induce \((n_1-n_2)\)th LOH current in the dc-link. For example, when the ac currents consist of 1st, 7th, and 11th harmonics, besides the dominating positive sequence fundamental frequency component, the inverter output voltage also has small amount of the −1st and +7th harmonics. Therefore, besides the 2nd and 6th harmonic currents in the dc-link, it is deduced from (34) that the 8th harmonic current is also present in small quantities in the dc-link. This interesting phenomenon can also be observed from the experimental results as shown in Fig. 11. More interestingly, the experimental results in Fig. 11 have small amount of the dc-link LOH current that are not present as deduced from (40). This is obviously due to the miscellaneous grid voltage harmonics in the practical tests.

### 6 Conclusion

This paper proposes generic equations set to analyse the dc-link current for three-phase VSI applications like the APF, where LOHs are dominant in the ac currents. As the capacitor ESR varies at the low frequencies and stay nearly constant at the switching frequencies, the equations of the individual dc-link LOH currents and the overall RMS value of the SHCs in the practical tests. The method simplifies the lengthy trigonometric derivation as in the power computation with three-phase quantities. Next, after complicated trigonometric derivation, the dc-link SHC RMS equations were successfully formulated, given any LOHs in ac currents. Moreover, the full ranges of the phase angles of the given LOHs in ac currents are also considered, since they bring up infinite dc-link current for three-phase VSI applications like the APF, where LOHs are dominant in the ac currents.
design, the SHC RMS equations are further simplified into one equation and then demonstrated with quantitative design cases of an APF dc-link. The dc-link current experimental results under different groups of grid side LOH currents validate the proposed computation methods. Not only the proposed equations set is a practical tool to analyse the dc-link current under arbitrary unbalanced and harmonic ac currents, the dc-link current RMS equations in prior art could also be obtained as its special cases.

7 Reference

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