Design and Analysis of Efficient Maximum/Minimum Circuits for Stochastic Computing

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Abstract

In stochastic computing (SC), a real-valued number is represented by a stochastic bit stream, encoding its value in the probability of obtaining a one. This leads to a significantly lower hardware effort for various functions and provides a higher tolerance to errors (e.g., bit flips) compared to binary radix representation. The implementation of a stochastic max/min function is important for many areas where SC has been successfully applied, such as image processing or machine learning (e.g., max pooling in neural networks). In this work, we propose a novel shift-register-based architecture for a stochastic max/min function. We show that the proposed circuit has a significantly higher accuracy than state-of-the-art architectures at comparable hardware cost. Moreover, we analytically proof the correctness of the proposed circuit and provide a new error analysis, based on the individual bits of the stochastic streams. Interestingly, the analysis reveals that for a certain practical bit stream length a finite optimal shift register length exists and it allows to determine the optimal length.

Index Terms

Stochastic computing, sequential logic, finite state machine, stochastic max/min function

I. INTRODUCTION

Stochastic computing (SC) is a promising computing paradigm, which represents a real-valued number by a stochastic stream [1]–[3]. The value is encoded by the probability of obtaining a one in the stream. Compared to binary radix representation, the stochastic representation leads to low hardware cost and high fault tolerance to circuit noise and bit flips [4], [5].

In SC, basic arithmetic operations can be realized with simple combinational logic [1]. Moreover, combinational logic can be synthesized to implement arbitrary polynomial functions, by manipulating them into a Bernstein polynomial with coefficients in the unit interval [6]–[8]. However, in order to implement more complex (non-linear) functions, sequential logic is required [4], [9]. In particular, linear finite-state machines (FSM) have been proposed to implement complex functions, which can be realized by either employing saturating up/down counters or shift registers [10]. The stochastic exponentiation and the tanh function were presented in [9] and the absolute value as well as exponentiation based on an absolute value were proposed in [4]. Recently, a new synthesis method which allows to implement arbitrary functions using FSM-based elements was introduced in [11].

In recent years, SC has been successfully applied to a variety of applications such as decoding of modern error correcting codes [12]–[14], control systems [15], [16], image processing [17]–[19], filter design [20], [21], and neural networks [9], [22]–[24]. Most of these applications exploit
the low complexity circuitry of SC in algorithms that do not require a high numerical precision of the final result.

In many of the aforementioned application domains, the efficient implementation of a stochastic max/min (SMax/SMin) function is very important. Especially, for neural networks, where such functions are the key element in the max pooling layer [22], [23]. Two architectures for SMax functions have been proposed in literature [17], [23]. The implementation in [17] is based on a stochastic comparator, which requires a stochastic number generator (SNG) that is usually realized by a linear feedback shift register. In order to reduce the overhead of the SNG, an optimized SMax function was proposed in [23]. However, both approaches have only been validated empirically.

Thus, the first goal of this paper is to analytically prove the correctness of the SMax functions in [17], [23]. Then, we propose a novel shift-register-based architecture for a stochastic SMax/SMin function and analytically prove its correctness. We show that the novel architecture provides a higher accuracy than [17], [23] at comparable hardware cost. We provide a new error analysis of the proposed circuit, considering the individual bits of the stochastic streams. To the best of our knowledge, no such analysis has been done before for an FSM-based stochastic computing element. Based on the error analysis we show that for practical bit stream lengths a finite optimal shift register length exists. Moreover, we determine the optimal shift register size for certain bit stream lengths.

II. STOCHASTIC COMPUTING BASICS

In this section, we briefly review the main principles of SC and introduce the basic computing elements used in this work. A comprehensive overview on SC can be found in [2] and recent challenges and potential solutions are discussed in [3].

A. Unipolar Coding Format

In the unipolar coding format, the value of a deterministic number \( x \in [0, 1] \) is encoded in a stochastic bit stream \( X \) of length \( N \). The individual bits in the stochastic stream are indicated by \( X[i] \in \{0, 1\} \). The probability for each bit in the stream to be one is given by \( x = P_X = P(X[i] = 1) \). In practical realizations, the rate of ones in the stochastic bit stream is used to represent the number \( x \)

\[
 r(X) = \frac{\sum_{i=1}^{N} X[i]}{N} = \frac{o(X)}{N},
\]

where \( o(X) = \sum_{i=1}^{N} X[i] \) denotes the number of ones in the stream. The precision (representation resolution) of the unipolar format is given by \( 1/N \). Thus, \( r(X) = x \) only if \( N \to \infty \), otherwise \( r(X) \) is only an approximation of \( x \).

1It is important to note that the circuits proposed in this work are also valid for the bipolar format, which enables the representation of negative values [1].
B. Combinational Logic-based SC Elements

Certain arithmetic operations in SC can be implemented by single combinational elements, for example scaled addition and multiplication can be realized using a multiplexer and an AND gate, respectively. Moreover, an XOR gate with the input streams $A$ and $B$ implements the function $A + B - 2AB$, which involves addition and subtraction. In the following, we briefly explain the principles of the aforementioned operations, as they are the main building blocks of the SMax/SMin functions presented in Secs. III and IV.

1) Multiplication: The stochastic multiplication can be implemented using a simple AND gate as shown in Fig. 1a. If we assume that the input stochastic streams $A$ and $B$ are uncorrelated and have the probabilities $P_A$ and $P_B$, then we have at the output

$$P_C = P_A P_B.$$  \hspace{1cm} (2)

For the unipolar format the values encoded by the stochastic streams $A$, $B$ and $C$ are $a = P_A$, $b = P_B$ and $c = P_C$, and, thus we obtain

$$c = ab.$$  \hspace{1cm} (3)

2) Scaled Addition: The stochastic circuit for scaled addition, a multiplexer, is shown in Fig. 1b. If we assume that the stochastic streams $A$ and $B$ are uncorrelated with the stochastic stream $S$, and $P_A$, $P_B$ and $P_S$ are their corresponding probabilities, the output can be expressed as

$$P_C = P_S P_A + (1 - P_S) P_B.$$  \hspace{1cm} (4)

According to the unipolar format, we substitute $P_A$, $P_B$, $P_C$ and $P_S$ by $a$, $b$, $c$ and $s$, and obtain the following output

$$c = sa + (1 - s)b.$$  \hspace{1cm} (5)

In order to perform unbiased addition, $s$ is set to $1/2$.

3) Non-Scaled Addition and Subtraction: If we assume uncorrelated input stochastic streams $A$ and $B$, with the corresponding probabilities $P_A$, $P_B$, then according to the Boolean function of the XOR gate (cf. Fig. 1c) we have at the output

$$P_C = P_A(1 - P_B) + P_B(1 - P_A) = P_A + P_B - 2P_A P_B.$$  \hspace{1cm} (6)

For the unipolar coding format (i.e. $a = P_A$, $b = P_B$ and $c = P_C$) we can rewrite (6) as follows

$$c = a + b - 2ab.$$  \hspace{1cm} (7)
C. FSM-based SC Elements

Combinational logic can be used to realize polynomial functions of a specific form [6] and to approximate non-polynomial functions, for example using the MacLaurin expansion [8]. However, highly non-linear functions such as the exponential or the tanh function cannot be realized. Hence, FSM-based SC elements have been introduced [4], [9]. Here, we briefly review the stochastic tanh function\(^3\) (STanh) which builds the basis for the state-of-the-art SMax/SMin functions presented in Sec. III.

1) Stochastic Tanh Function: Fig. 2 shows a linear FSM, with \(M\) states \(S_0, \ldots, S_{M-1}\) arranged in a linear form. The state transition process of the FSM can be modeled as a time-homogeneous irreducible and aperiodic Markov chain, which has a single steady state. The steady state probability is given by [4]

\[
P_i = \frac{\left(\frac{P_X}{1-P_X}\right)^i}{\sum_{j=0}^{M-1} \left(\frac{P_X}{1-P_X}\right)^j},
\]

where \(P_X\) denotes the transition probability from state \(S_i\) to \(S_{i+1}\) (state is incremented) and \((1 - P_X)\) indicates the transition from state \(S_i\) to \(S_{i-1}\) (state is decremented).

In order to realize the STanh function, the FSM output can be expressed as [9]

\[
P_Z = \sum_{i=M/2}^{M-1} P_i.
\]

Substituting \(P_i\) given in (8) into (9) results in [4]

\[
P_Z = \frac{\left(\frac{P_X}{1-P_X}\right)^{M/2}}{1 + \left(\frac{P_X}{1-P_X}\right)^{M/2}}.
\]

If we substitute \(P_X\) and \(P_Z\) by \(x\) and \(z\) (unipolar coding format) we obtain [4]

\[
z = \frac{\left(\frac{x}{1-x}\right)^{M/2}}{1 + \left(\frac{x}{1-x}\right)^{M/2}} = \frac{1}{2} + \frac{\tanh \left(M/2 \left(x - 1/2\right)\right)}{2},
\]

\(^3\)In [4], [9] various other FSM-based SC elements are presented as well.
which corresponds to a scaled and shifted tanh function\textsuperscript{4}. For a large number of states $M$, (11) behaves like a step function

$$
\lim_{M \to \infty} z = \begin{cases} 
0, & 0 \leq x < 0.5 \\
0.5, & x = 0.5 \\
1, & 0.5 < x \leq 1.
\end{cases}
$$

(12)

III. STATE-OF-THE-ART STOCHASTIC MAX/MIN FUNCTIONS

In this section, we discuss two recently proposed architectures of SMax/SMin functions [17], [23]. Moreover, we provide analytical proofs of their correctness, since [17], [23] only provide empirical validations. For the sake of clearness, we focus our analysis on the SMax function, since the presented propositions and proofs can be easily applied to the SMin function.

A. Stochastic Max/Min Function in [17]

Fig. 3 shows the architecture of the SMax function proposed in [17], which is based on the stochastic comparator (input multiplexer and STanh function). The SMin function is obtained by swapping the input streams at the final multiplexer. The following proposition validates the correctness of the circuit shown in Fig. 3.

Proposition 1. For uncorrelated input bit streams $A$ and $B$, encoding the values $a = P_A$ and $b = P_B$ (unipolar coding format), the output of the circuit shown in Fig. 3 can be expressed as

$$
c = a + \frac{b - a}{1 + \left( \frac{1 + (a - b)}{1 + (b - a)} \right)^{M/2}},
$$

(13)

where $c = P_C$ denotes the value encoded in the output stream $C$. For $M \to \infty$ the expression in (13) can be written as

$$
\max(a, b) = \lim_{M \to \infty} c = \begin{cases} 
a, & a > b \\
a, & a = b \\
b, & a < b,
\end{cases}
$$

(14)

\textsuperscript{4}Substituting $P_X$ and $P_Z$ in (10) with their bipolar coding format results in $z = \tanh(M/2x)$ [4], representing the signum function for $M \to \infty$. 

Fig. 3. Implementation of the SMax function proposed in [17]
which validates the functionality of the SMax function.

Proof. The output of the first multiplexer is given by (cf. (4))

\[ P_D = P_{S_1} P_A + (1 - P_{S_1})(1 - P_B) = 1/2(1 + P_A - P_B), \]  

with \( P_{S_1} = 1/2 \). According to (10), the output of the STanh function can be expressed as

\[ P_{S_2} = \frac{\left( \frac{P_D}{1-P_D} \right)^{M/2}}{1 + \left( \frac{P_D}{1-P_D} \right)^{M/2}}. \]  

Finally, the output of the second multiplexer is given by (cf. (4))

\[ P_C = P_{S_2} P_A + (1 - P_{S_2}) P_B \]

\[ = P_A + \frac{P_B - P_A}{1 + \left( -1 + \frac{2}{1-(P_A + P_B)} \right)^{M/2}}. \]  

When substituting \( P_A, P_B \) and \( P_C \) with their corresponding unipolar coding format values \( a, b \) and \( c \) we obtain

\[ c = a + \frac{b - a}{1 + \left( \frac{1+(a-b)}{1+(b-a)} \right)^{M/2}}. \]  

If \( M \to \infty \) the denominator in (13) becomes infinity or zero when \( a > b \) or \( a < b \), respectively. Thus, \( c = a \) or \( c = b \) if \( a > b \) or \( a < b \), which proves the correctness of the SMax circuit shown in Fig. 3. \( \square \)

Fig. 4 illustrates the analytical expression in (13), the bit-wise simulation results of the circuit shown in Fig. 3 and the exact max function. We observe a good match between the theoretical and simulation results. Moreover, we observe that already a moderate number of states \( M \) provide a good approximation of the max function.

B. Stochastic Max/Min Function in [23]

Fig. 5 shows the architecture of the SMax function proposed in [23]. Similar to Sec. III-A, the SMin function is obtained by swapping the input streams at the final multiplexer. The following proposition validates the correctness of the circuit shown in Fig. 5.

Proposition 2. For uncorrelated input bit streams \( A \) and \( B \), encoding the values \( a = P_A \) and \( b = P_B \) (unipolar coding format), the output of the circuit shown in Fig. 5 can be expressed as

\[ c = a + \frac{b - a}{1 + \left( \frac{a(1-b)}{b(1-a)} \right)^{M/2}}. \]  

where \( c = P_C \) denotes the value encoded in the output stream \( C \). For \( M \to \infty \) the expression in (20) can be written as

\[ \max(a, b) = \lim_{M \to \infty} c = \begin{cases} a, & a > b \\ a, & a = b \\ b, & a < b. \end{cases} \]
which validates the functionality of the SMax function.

Proof. The output of the XOR gate can be expressed as (cf. (6))

$$P_D = P_A + P_B - 2P_A P_B.$$  \hfill (22)

In contrast to the STanh function presented in Sec. II-C1 the STanh function shown in Fig. 5 has two inputs $A$ and $D$. The stochastic stream $D$ is used to enable the FSM state update and the $A$ updates the state according to its value. In particular, if $D[i] = 1$ then the state increases if $A[i] = 1$ and decreases if $A[i] = 0$; if $D = 0$ the state is not updated independently of $A[i]$. 

Fig. 5. Implementation of the SMax function proposed in [23].

Fig. 4. SMax function [17]. Solid lines: theoretical results (13); markers (+): bit-wise simulation for $N = 10^6$; dotted line: exact max function.
Thus, the probability that the state increases or decreases is given by \( P_A P_D \) and \((1 - P_A) P_D\), respectively. According to (8), the steady state probability is given by

\[
P_i = \frac{\left( P_A P_D \right)^i}{\sum_{j=0}^{M-1} \left( P_A P_D \right)^j}
\]

\[
= \frac{\left( P_A (1 - P_B) \right)^i}{\sum_{j=0}^{M-1} \left( P_B (1 - P_A) \right)^j},
\]

with \( P_A P_D = P_A (1 - P_B) \) and \( P_D (1 - P_A) = P_B (1 - P_A) \). According to (10), the output of the STanh function can be expressed as

\[
P_S = \frac{\left( \frac{P_A (1 - P_B)}{P_B (1 - P_A)} \right)^{M/2}}{1 + \left( \frac{P_A (1 - P_B)}{P_B (1 - P_A)} \right)^{M/2}}.\]

Finally, the output at the multiplexer is given by (cf. (4))

\[
P_C = P_S P_A + (1 - P_S) P_B
\]

\[
= P_A + \frac{P_B - P_A}{1 + \left( \frac{P_A (1 - P_B)}{P_B (1 - P_A)} \right)^{M/2}}.
\]

For the unipolar encoding format (i.e. \( a = P_A \), \( b = P_B \) and \( c = P_C \)) we have

\[
c = a + \frac{b - a}{1 + \left( \frac{a(1 - b)}{b(1 - a)} \right)^{M/2}}.
\]

If \( M \to \infty \) the denominator in (20) becomes infinity or zero when \( a > b \) or \( a < b \), respectively. Thus, \( c = a \) or \( c = b \) if \( a > b \) or \( a < b \), which proves the correctness of the SMax circuit shown in Fig. 5.

Fig. 6 illustrates the analytical expression in (20), the bit-wise simulation results of the circuit shown in Fig. 5, and the exact max function. We observe a good match between the theoretical and simulation results. Similar to Fig. 4, we observe that already a moderate number of states \( M \) provide a good approximation of the max function. However, in Fig. 6 one can already see a closer match of this approach compared to the SMax function of [17].

IV. NOVEL STOCHASTIC MAX/MIN FUNCTION: ARCHITECTURE

In this section, we propose a novel architecture for the SMax function as shown in Fig. 7. This circuit can be easily converted to realize the SMin function by inverting its inputs \( A \) and \( B \) as well as its output \( C \). Hence, we only consider the SMax function in the following description. In contrast to the state-of-the-art SMax functions [17], [23], the FSM-based SC element used in the proposed architecture does not implement the STanh function. However, similar to the architecture in [23] it has two inputs \( A \) and \( D \). Input \( D \) enables the FSM state update and \( A \) updates the state according to its value (cf. Sec. III-B). FSM-based elements can either be
implemented using up/down counters or shift registers. When using a shift register, its length $L$ is equal to the last state of the FSM, i.e. $L = M - 1$. For the novel SMax function we use a shift register, since it has some distinct advantages compared to a counter-based implementation [10]. One advantage is that the values in a shift register are of equal significance, in contrast to a binary counter, where the bits are weighted by different powers of two. This allows to design more fault-tolerant SC computing circuits when using shift registers. Furthermore, as the following description demonstrates, shift registers are naturally suited to implement the described functionality.

Depending on the actual value of the input streams $A$ and $B$ the functionality of the SMax function (cf. Fig. 7) can be described as follows:

- $A[i] = B[i]$: Since $D[i] = 0$ the content of the shift register remains unchanged (state is not updated) and the output of the circuit is given by $C[i] = B[i]$.
- $A[i] = 0$, $B[i] = 1$: Since $D[i] = 1$ and $A[i] = 0$ a zero is shifted from the right into the shift register (state is decremented) and the output of the circuit is given by $C[i] = B[i]$.
- $A[i] = 1$, $B[i] = 0$: Since $D[i] = 1$ and $A[i] = 1$ a one is shifted from the left into the shift register (state is incremented). In this case the rightmost value of the shift register is output by the circuit, i.e. $C[i] = U[i]$.

According to the description above it is important to note that the ones in the stream $B$ also appear in the output stream $C$.

In the following, we provide two approaches for analyzing the functionality of the proposed SMax function. First, we describe the functionality by considering the individual bits in the stochastic bit stream. Then, similar to Sec. III we proof the correctness of the circuit assuming
very long stochastic bit streams. We denote these two methods as deterministic and probabilistic analysis, respectively.

A. Deterministic Analysis
For the deterministic analysis of the novel SMax function we distinguish the two cases: \( r(A) \leq r(B) \) and \( r(A) > r(B) \).

1) SMax Circuit Behavior for \( r(A) \leq r(B) \): If \( r(A) \leq r(B) \), the stream \( B \) has more (or equal) ones than bit stream \( A \). For a correct functionality it is desired that the number of ones \( o(B) \) in the input stream \( B \), and the number of ones \( o(C) \) in the output stream \( C \), are equal. As discussed above, all ones of stream \( B \) are included in the output stream \( C \). However, if a subsequence of \( A \) has more ones than the corresponding subsequence of \( B \), also ones of stream \( A \) might be additionally injected into the output stream \( C \). This occurs if the excess of ones in this subsequence is larger than the shift register length \( L \). We refer to such an event as right overflow of the shift register. Thus, the number of ones in the output stream \( C \) can be expressed as

\[
o(C) = o(B) + o_R,
\]

where \( o_R \) denotes the additional number of ones due to the right overflows. If the shift register is sufficiently long, no right overflows occur, i.e. \( o(C) = o(B) \).

2) SMax Circuit Behavior for \( r(A) > r(B) \): If \( r(A) > r(B) \), the bit stream \( A \) has more ones than bit stream \( B \). For a correct functionality, it is desired that \( o(A) \), the number of ones in the input stream \( A \), and \( o(C) \), the number ones in the output stream \( C \), are identical. Similar as above, all ones of \( B \) are included in the output stream \( C \). In addition, the excess of ones in stream \( A \) is shifted into the shift register and once the shift register is filled, the ones are injected into the output stream \( C \) when \( B[i] = 0 \) and \( A[i] = 1 \) occurs. However, at the end there might be ones left in the shift register, which are missing in the output stream \( C \). We denote the number of missing ones by \( o_S \). Moreover, if a subsequence of \( B \) has more ones than the corresponding subsequence of \( A \), also ones of stream \( B \) might additionally be injected into the output stream \( C \). This happens if the excess of ones leads to an empty (all-zero) shift register, and, thus, an input pattern \( B[i] = 1 \) and \( A[i] = 0 \) (and assuming a later following \( B[i] = 0 \) and \( A[i] = 1 \)) injects an additional one

\footnote{We assume the same length for all stochastic streams, which is a typically assumption in SC.}
in the output stream $C$. We refer to this effect as left overflow of the shift register and denote the number of additional ones due to left overflows by $o_L$. This allows expressing the number of ones in the output stream $C$ as

$$o(C) = o(B) + (o(A) - o(B)) + o_L - o_S,$$  \hspace{1cm} (29)

where $(o(A) - o(B))$ denotes the excess of ones in stream $A$ compared to stream $B$. Expression (29) shows the two opposite error effects. One the one hand, the number of left overflows $o_L$ becomes smaller for long shift registers. On the other hand, the error due to the remaining ones in the shift register $o_S$ becomes smaller, for short shift registers. In Sec. V we determine the optimal shift register length for a given bit stream length.

B. Probabilistic Analysis

The following proposition validates the correctness of the circuit shown in Fig. 7.

**Proposition 3.** For uncorrelated input bit streams $A$ and $B$, encoding the values $a = P_A$ and $b = P_B$ (unipolar coding format), the output of the circuit shown in Fig. 7 can be expressed as

$$c = b + \frac{b - a}{\left(\frac{b(1-a)}{a(1-b)}\right)^M - 1},$$ \hspace{1cm} (30)

where $c = P_C$ denotes value encoded in the output stream $C$. For $M \to \infty$ the expression in (30) can be written as

$$\max(a, b) = \lim_{M \to \infty} c = \begin{cases} 
  c = a, & a > b \\
  c = b, & a = b \\
  c = b, & a < b.
\end{cases}$$ \hspace{1cm} (31)

which validates the functionality of the $SMax$ function.

**Proof.** The output of the XOR gate can be expressed as (cf. (6))

$$P_D = P_A + P_B - 2P_A P_B.$$ \hspace{1cm} (32)

Similar to Sec. III-B, the FSM has two inputs $A$ and $D$ and, thus, the steady state probability can be written as (cf. (23))

$$P_i = \left(\frac{P_A(1-P_B)}{P_B(1-P_A)}\right)^i \sum_{j=0}^{M-1} \left(\frac{P_A(1-P_B)}{P_B(1-P_A)}\right)^j.$$ \hspace{1cm} (33)

According to Fig. 7, the FSM outputs can be expressed as

$$P_U = P_{M-1} = \left(\frac{P_A(1-P_B)}{P_B(1-P_A)}\right)^{M-1} \sum_{j=0}^{M-1} \left(\frac{P_A(1-P_B)}{P_B(1-P_A)}\right)^j = \frac{P_B - P_A}{P_A(1-P_B)\left(-1 + \left(\frac{P_A(1-P_B)}{P_B(1-P_A)}\right)^{-M}\right)}.$$ \hspace{1cm} (34)
The output of the AND gate can be calculated as (cf. (4))

\[ P_S = P_D(1 - P_B) = P_A(1 - P_B). \] (35)

Finally, the output of the multiplexer is given by

\[ P_C = P_S P_U + (1 - P_S) P_B = P_B + \frac{P_B - P_A}{\left(\frac{P_B(1 - P_A)}{P_A(1 - P_B)}\right)^M - 1} \] (36)

For the unipolar encoding format (i.e. \( a = P_A, b = P_B \) and \( c = P_C \)) we have

\[ c = b + \frac{b - a}{\left(\frac{b(1-a)}{a(1-b)}\right)^M - 1}. \] (37)

If \( M \to \infty \) the denominator in (20) becomes zero or infinity depending on whether \( a > b \) or \( a \leq b \), respectively. Thus, \( c = a \) or \( c = b \) if \( a > b \) or \( a \leq b \), which proves the correctness of the SMax circuit shown in Fig. 7.

Fig. 8 illustrates the analytical expression in (30), the bit-wise simulation results of the circuit shown in Fig. 7 and the exact max function. We observe a good match between the theoretical and simulation results. Moreover, we observe that already a low number of states \( M \) provide a good approximation of the max function. In contrast to the state-of-the-art SMax functions [17], [23] the proposed function does not approach the exact max function at \( a = b \), but provides a better approximation for \( a \neq b \).

Next, we compare the approximation error of the state-of-the-art SMax functions and the novel SMax function. For this we calculate the expected value of the absolute error, assuming a uniform distribution of \( a \) and \( b \) over the interval \([0,1]\), respectively. We define the absolute error \( e \) by \( e = |c_{\text{exact}} - c| \), with the exact max function \( c_{\text{exact}} = \max(a, b) \) and the FSM-based approximations \( c \) given in (13), (20) and (30), respectively. Then, the expected absolute error can be calculated as

\[ E(e) = \int_0^1 \int_0^1 |c_{\text{exact}} - c| da db. \] (38)

The absolute value of the error in (38) allows to consider both, erroneously added ones (i.e. \( c > c_{\text{exact}} \)) as well as erroneously removed ones (i.e. \( c < c_{\text{exact}} \)) in the bit stream representing \( c \). When considering a stochastic bit stream of \( c_{\text{exact}} \), then the absolute difference \( e \) can be interpreted as a bit error probability of \( c \) compared to such a bit stream of \( c_{\text{exact}} \). This is crucial in order to enable a comparison with the analysis results presented in Sec. V. We observe from Fig. 9 that the novel SMax function has a significantly lower approximation error than the state-of-the-art SMax functions. This is because the denominator of (30) (power of \( M \)) converges faster to zero or infinity as the number of states \( M \) increases compared to the denominators in (13) or (20) (power of \( M/2 \)). Moreover, we observe that the SMax function proposed in [17] has the highest approximation error among the three approaches.
V. NOVEL STOCHASTIC MAX/MIN FUNCTION: ERROR ANALYSIS

We observed from the deterministic analysis in Sec. IV-A that long shift registers reduce the errors due to right and left overflows. However, a large shift register length increases the error caused by the remaining bits in the shift register. It is important to note that especially the last observation cannot be inferred from the probabilistic analysis presented in the previous chapter. The probabilistic analysis becomes exact if and only if the bit stream length goes to infinity. In such a case, a finite number of remaining bits in the shift register does not matter. However, when using a finite bit stream length, these remaining bits matter. In the following analysis, we assume a finite bit stream length that is significantly larger than the shift register length (a typical scenario in SC). This allows using the probabilistic FSM description in Sec. IV-B for modelling the behavior of the shift register for finite bit stream lengths. Moreover, having sufficiently long bit streams justifies using the probabilities of ones instead of the rate of ones in the stream (cf. Sec. II-A) for the following error analysis.

In the following, we derive the expected error probability, based on the deterministic analysis in Sec. IV-A. With this expression we determine the optimal shift register length $L_{opt}$, with respect to the bit stream length $N$. Similar to Sec. IV-A we distinguish two cases: $a \leq b$ and $a > b$.

A. Error Probability for $a \leq b$

In this case, an error occurs due to right overflows. In particular, the shift register is filled with ones, i.e. the FSM is in the last state $M-1$, and the input $A[i] = 1$ and $B[i] = 0$ is applied.
The probability for this error event can be described as

$$P_{e,a \leq b} = P_{M-1}P_A(1 - P_B),$$

(39)

where $P_{M-1}$ describes the probability of the FSM to be in the last state (cf. (34)).

**B. Error Probability for $a > b$**

In this case, errors can originate from two sources: Left overflow and remaining ones in the shift register. At the left overflow, the shift register is empty (all-zeros), i.e. the FSM is in state $S_0$, and the input pattern $A[i] = 0$ and $B[i] = 1$ occurs. The probability for this error event can be expressed as

$$P_{e,0} = P_0P_B(1 - P_A).$$

(40)

where $P_0$ denotes the probability of the zero state of the FSM, i.e. an all-zero shift register (cf. (33)). The corresponding expected number of erroneously added ones in the output stream can be calculated by

$$E_{a} = NP_{e,0}.$$  

(41)

For the error caused by the remaining ones in the shift register we compute the expected value of the shift register state, i.e. the expected number of ones in the shift register, as

$$E_r = \sum_{i=0}^{M-1} iP_i.$$  

(42)
where $P_i$ denotes the probability of the FSM to be in the $i$th state. Note that the expected number of ones in the shift register corresponds to the number of ones that are missing on average in the output stream. Combining (41) and (42) and considering that left overflows add ones to the output stream, while the remaining bits in the shift register are the missing ones in the output stream, the expected number of erroneous ones is given by

$$E_{e,a>b} = E_a - E_r = N P_{e,0} - \sum_{i=0}^{M-1} i P_i. \quad (43)$$

Finally, the error probability can be expressed as

$$P_{e,a>b,N} = \left| \frac{E_{e,a<b}}{N} \right| = \left| P_{e,0} - \frac{1}{N} \sum_{i=0}^{M-1} i P_i \right|. \quad (44)$$

Interestingly, the second term in (44) depends on the stream length $N$, which goes to zero for $N \to \infty$. This is because a finite number of missing bits has a higher impact on the error for shorter streams than for longer streams.

C. Expected Error Probability

Assuming a uniform distribution for $a$ and $b$ over $[0,1]$ and using (39) and (44), the expected error probability can be derived as follows

$$E(P_{e,N}) = \int_0^1 \left( \int_0^b P_{e,a<b} da \right) db + \int_0^1 \left( \int_0^a P_{e,a>b,N} db \right) da. \quad (45)$$

The two integrals in (45), cover exactly half of the two dimensional space $[0,1] \times [0,1]$. Thus, they form the expected value over the whole space.

Unfortunately, to the best of our knowledge, for this integral no closed-form solution exists. Thus, we calculated it through numerical integration. Fig. 10 shows the error probabilities obtained through numerical integration and the simulation results. For each simulated point, the empirical error probability was averaged over 10000 test cases. We observe a good match between the theoretical and the simulation results. However, the analytical results are obtained much faster than the simulation results. Moreover, it can be seen that for a certain stream length $N$ there exists an optimal shift register length $L_{opt}$. For example, for $N = 10^4$ the error probability decreases until length 15 and then increases due to the remaining bits in the shift register. Thus, for $N = 10^4$ the optimal shift register length is given by $L_{opt} = 15$. In Fig. 10, we marked the optimal shift register lengths with triangles and added extra ticks at the x-axis. The lower bound curve in Fig. 10 corresponds to the performance limit if the bit stream length $N$ goes to infinity. It can either be obtained by numerically integrating (38) or (45), the latter with $N \to \infty$. For the latter approach, the second term on the right hand side of (44) goes to zeros, resulting in $P_{e,a>b,N \to \infty} = P_{e,0}$. This is because when the stream length goes to infinity, a finite number of remaining bits in the shift register does not matter.

VI. CONCLUSIONS

In this work, we investigated the stochastic SMax/SMin function, which is an important building block in many applications (e.g., max pooling in neural networks). Prior works have proposed circuits for the SMax/SMin function and provided empirical validation. In this paper, we analytically
proved the correctness of these architectures. Moreover, we proposed a novel shift-register based SMax/SMin function, which outperforms the state-of-the-art architectures in terms of accuracy, while having comparable hardware cost. We provided a new error analysis of the proposed circuit, considering the value of the individual bits in the stochastic stream. This analysis revealed that for practical bit stream lengths a finite optimal shift register length exists. Moreover, we showed that increasing the shift register length beyond the optimal value deteriorates the accuracy. This is due to the error caused by the remaining bits in the shift register. Hence, finding strategies to empty the shift register might be an interesting future extension of this work.

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