Computation Error Analysis of Block Floating Point Arithmetic Oriented Convolution Neural Network Accelerator Design

Zhourui Song†, Zhenyu Liu‡, Chunlu Wang†, Dongsheng Wang‡
†School of Cyberspace Security, BUPT, Beijing, 100876, China
‡RIIT, Tsinghua University, Beijing, 100084, China
Email: liuzhenyu73@mail.tsinghua.edu.cn

Abstract

The heavy burdens of computation and off-chip traffic impede deploying the large scale convolution neural network on embedded platforms. As CNN is attributed to the strong endurance to computation errors, employing block floating point (BFP) arithmetics in CNN accelerators could save the hardware cost and data traffics efficiently, while maintaining the classification accuracy. In this paper, we verify the effects of word width definitions in BFP to the CNN performance without retraining. Several typical CNN models, including VGG16, ResNet-18, ResNet-50 and GoogLeNet, were tested in this paper. Experiments revealed that 8-bit mantissa, including sign bit, in BFP representation merely induced less than 0.3% accuracy loss. In addition, we investigate the computational errors in theory and develop the noise-to-signal ratio (NSR) upper bound, which provides the promising guidance for BFP based CNN engine design.

1 Introduction

Convolutional neural networks (CNNs) have achieved state-of-art performance in many artificial intelligence tasks, especially in image recognition (Ciregan, Meier, and Schmidhuber 2012) (Russakovsky et al. 2015b), nature language processing(Kim 2014)(Goldberg 2016), strategic planning(Silver et al. 2016), etc. This success is partially facilitated by the advance of computation infrastructure. With GPU clusters, large-scale CNNs can be deployed though they are memory-intensive, computation-intensive and resource-consuming(Li et al. 2016). However, when deploying CNNs in data center, GPU clusters is not the first preference because of the low power efficiency of GPU. Therefore, promoting energy efficiency became one prominent target in CNN accelerator design. Researchers have committed to exploring how to deploy CNNs on FPGAs (Ovtcharov et al. 2015), or designing AISCs(Jouppi et al. 2017), as they have higher energy efficiency due to their specific architecture.

To transplant CNNs on FPGA, two serious issues, i.e., off-chip traffic bottleneck and huge amount of floating-point arithmetics overhead, need to be addressed. The off-chip traffic stems from that, for large scale networks, the feature maps and the network parameters must be stored in the off-chip SDRAM. The frequent accesses to these data induces no-trivial bandwidth requirements. Secondly, as the hardwired floating-point modules are not always equipped in FPGA, employing the floating point operations in FPGA CNN accelerator degrades the throughput and the energy efficiency severely.

Methods like data reusing, compression and trimming have been developed to meet the bandwidth requirement of FPGA. (Chen et al. 2017) (Karam et al. 2017) reduced external data access with delicate data reuse at the cost of reconfiguring FPGA for different layers of computation. (Zhang et al. 2015) creatively proposed a method that dynamically choose optimization techniques, including loop tiling and transformation, under the help of roofline model. Though they balanced computation throughput and memory bandwidth, they failed in reducing computation. Sparsifying parameters is another popular solution, (Han, Mao, and Dally 2015) proposed a three-stage compression method, namely pruning, trained quantization and Huffman coding that significantly reduced the size of DNNs without decrease in accuracy. However, the requirement of retraining becomes the hindrance of deploying their method as retraining is time consuming, and Huffman coding makes it even more time consuming than training the original network. The primary hindrance of network compressing is that the sparsity and the entropy coding degrade the throughput of CNN accelerator. Trimming, proposed in (Han et al. 2015) and (Parashar et al. 2017), also suffers from retraining as they need to find the import connections and abandon the others.

Researchers have committed to replacing 32-bit floating point number format with fixed point number format. (Page and Mohsenin 2016) utilized singular value decomposition on dense layers and limited precision fixed-point representations of convolutional weights, at the cost of less than 0.2% decrease in accuracy on MNIST, CIFAR-10 and SVHN with 3-bit integer and 6-bit fraction fixed point format. Rounding model has also draw attention. (Gupta et al. 2015) proposed that deep networks can be trained in 16-bit fixed point representation with stochastic rounding. However, a shared weakness of methods mentioned above is that they all require retrain to amended parameters, while retrain is very expensive, and when applied in deep neural networks, the quick growth of word width requirement consumes more chip area, power, and bandwidth, which becomes the hindrance of employing integer arithmetic in complex network models. For example, (Hill et al. 2016) proved that GoogLeNet acquires 40-
bit fixed point representation to maintain an acceptable accuracy using stochastic rounding mentioned above.

(Mellempudi et al. 2017) proposed a method that divide weights and activations into clusters, and each cluster holds a joint scaling factor, in this way, the numbers in the same cluster can be represented by a integer index. The subsequent convolution operation can be carried out in the integer domain. They designed a system that utilizes 8-bit integer achieving 6% decrease in ResNet-101 top-1 accuracy without retraining. This scheme partly eliminated the floating point operations. In specific, the scaling procedure is still carried out with floating point arithmetics, which even include the divide and the root operations.

In this paper, we proposed a block floating point (BFP) based convolution implementation. BFP representation can be attributed as a special case of floating point representation where numbers within a block share a joint exponent. Hence, BFP possesses the high dynamic range of floating point representation as it has exponent part. On the other hand, the computation complexity of two BFP blocks is reduced to the degree of integer representation. Experiments in our paper revealed that even with 7-bit mantissa, we can achieve less than 0.3% accuracy loss when implementing the BFP transform procedure are denominated as the quantization errors. There are two ways to handle the out-of-range errors that can be accumulated in layer-wise and finally in-put layer. Because the truncation operation always generates the DC errors and the rounding operation introduces a large bias. In contrast, the rounding operation introduces the zero-mean Gaussian white noises, and then no accumulated bias exists.

The energy of quantization errors of BFP is related to the distribution of numbers within the block, block size $n$ and mantissa bit length. To be specific, when $L_m$ is fixed, if $X$ contains a few numbers with large magnitude while others are small, the overall precision of $X'$ will be low. Secondly, when the distribution of numbers is given, the more number one block contains, the possibility of one block contains large peak and rather small mean value arises, resulting into a small overall precision. Obviously, the precision of BFP is proportionate to $L_m$.

2 Block-Floating Point Arithmetic

2.1 Definition of Block Floating Point Arithmetic

Block floating point representation holds one common scaling factor, named block exponent, for $n$ numbers within a block. The block exponent is determined by the largest magnitude in the block, and smaller ones will be right shifted to align, which is called block formatting.

The associated nomenclature are defined to simplify our statement at first. For a cluster of numbers, denoted as $X$, $x_i$ is the $i$th element of $X$, $m_i$ and $e_i$ are the mantissa and exponent part of $x_i$. Further, when $X$ is block formatted into $X'$, the mantissa part and block exponent is written as $M_X$ and $e_X$.

For example, given a block $X$ that contains $N$ floating numbers, $X$ can be expressed as

\[ X = (x_1, \cdots x_i, \cdots x_N) \]
\[ = (m_1 \times 2^{e_1}, \cdots, m_i \times 2^{e_i}, \cdots, m_N \times 2^{e_N}) \]

With BFP representation, $X$ is transformed to $X'$, which is written as

\[ X' = (x'_1, \cdots x'_i, \cdots x'_N) \]
\[ = M'_X \times 2^{e_X} \]

where

\[ M'_X = (m'_1, \cdots m'_i, \cdots m'_N) \]
\[ e_X = \max_{i \in [1, N]} e_i \]

$e_X$ is the maximum exponent in the block $X$ and $m_i$ is the aligned entry-wise mantissa that is derived with the following method,

\[ m'_i = m_i >> (e_X - e_i) \]

where $a >> b$ means right shifting $a$ for $b$ bits.

For CNN accelerator design, block-floating-point representation (BFP) possesses two advantages. First, the concise expression contributes to saving the memory and the traffic bandwidth. If we have a block floating point format with $L_m$-bit mantissa, $L_e$-bit exponent and one sign bit, the average length of $n$ numbers is $1 + L_m + L_e/n$, while floating point representation costs $1 + L_m + L_e$ bits per number. Lower average storing length means a lot to memory consuming applications and to chips whose memory is limited. In addition, with BFP, all multiply-accumulate operations in convolutional layer is carried out in fixed-point format. The fixed-point arithmetic unit in FPGA and ASIC design is much more efficient than the floating point one. For example, a 32-bit fixed-point adder in FPGA Virtex 7 690t consumes 1DSP with 300MHz clock speed. In contrast, a 16-bit 4-stage -pipeline floating-point adder is constituted of 2 DSPs and 117 LUT with 219MHz working frequency.

Acceleration in additions and multiplications is achieved at the cost of computation accuracy loss as compared with the floating-point counterpart because the small numbers in the block scarified more valid bits during the block based aligning procedure as shown in equation (1). The errors during the BFP transform procedure are denominated as the quantization errors. There are two ways to handle the out-shifted bits, namely truncating and rounding off. Our experiment proved that rounding off outperforms truncating, because the truncation operation always generates the DC errors that can be accumulated in layer-wise and finally introduces a large bias. In contrast, the rounding operation introduces the zero-mean Gaussian white noises, and then no accumulated bias exists.
maps are expanded into two matrices namely \( W \) and \( I \). In this figure, the padding and stride are formed from kernels, input feature maps and output feature maps respectively. In this figure, the padding and stride are set to 0 and 1 with 1 channel.

### 2.2 Matrix Representation of Convolutional Neural Networks

When transforming into matrix, kernels and input feature maps are expanded into two matrices namely \( W \) and \( I \). To be specific, kernels belonging to the same output feature map compose one row vector of \( W \) are expanded to row vector of \( W \), and receptive fields of input feature maps of one output pixel constitute one column vector in \( I \). This procedure is illustrated as Fig.1. The entry in \( O \) located at \( mn \)th row, \( n \)th column corresponds to the output feature map of \( mn \)th kernel on \( n \)th receptive field. After that, the size of input feature maps arises dramatically, which is unacceptable for FPGA with limited memory and bandwidth. Therefore, when designing hardware, convolution operations are still dealt with the old-fashioned way (Chunsheng et al. 2017). Here we use matrix representation to make it easier to understand how to apply BFP in CNNs.

### 2.3 BFP in Hardwired CNN Accelerator Oriented Matrix Partition

Further, block formatting \( W \) and \( I \) facilitates the advantages of BFP in hardwired CNN accelerator design. The precision of BFP is related to the distribution of numbers within the block, block size and mantissa bit length. As the distribution of input feature maps and weights are predetermined, we can only optimize the other two factors, namely block size and mantissa bit length, to achieve best overall performance. Under this guideline, the first issue is how to partition \( W \) and \( I \) as verifying the impact of mantissa bit length is easier to code compared with testing block size. Denote matrix \( O_{M \times N} = W_{M \times KN}I_{K \times N} \), where \( M, K \) and \( N \) are the number of filters, the size of filter and the number of receptive field. The process of matrix multiplication is described as below:

\[
O = WI
\]

from the perspective of entry-wise, matrix multiplication is represented as

\[
o_{mn} = \bar{w}_{m}^T \bar{r}_{n}
\]

and, if described in row-wise or column-wise, it turns to

\[
\bar{o}_{m}^T = \bar{w}_{m}^T \bar{I}
\]

\[
\bar{o}_{n} = \bar{W} \cdot \bar{r}_{n}
\]

In fact, equation (2), (3), (4) and (5) show four different ways to block format \( W \) and \( I \). Equation (2) shows \( W \) and \( I \) are block formatted into two blocks as a whole individually, thus the average store length reaches minimum at the price of highest accuracy loss. Equation (3) shows that block format \( \bar{w}_{m}^T \) and \( \bar{r}_{n} \) with block size \( K \), in this case, the minimum loss is achieved with increasing storing cost. Equation (4) and (5) represent a balanced approach that maintained the accuracy of filter matrix and the minimum storing cost of input feature map matrix, for they both block formats one matrix as a whole while the other one by row vector or column vector. The complexity and resource consuming comparisons of the above BFP transform methods are illustrated in Table 1.

| Method | \( AL_W \) | \( AL_I \) | Time |
|--------|-----------|-----------|------|
| Equation (1) | \( 1 + L_W + L_o/(M \times K) \) | \( 1 + L_I + L_o/(K \times N) \) | 2 |
| Equation (2) | \( 1 + L_W + L_o/K \) | \( 1 + L_I + L_o/K \) | \( M + N \) |
| Equation (3) | \( 1 + L_W + L_o/K \) | \( 1 + L_I + L_o/(K \times N) \) | 1 + M |
| Equation (4) | \( 1 + L_W + L_o/(M \times K) \) | \( 1 + L_I + L_o/K \) | 1 + N |

Table 1: the cost of 4 different methods block formatting \( W_{M \times K} \) and \( I_{K \times N} \). “\( AL_W \)”, “\( AL_I \)” are the average storing length of \( W \) and \( I \). “Time” is times need to run block formatting.

Consider one typical layer in VGG-16, “conv1_1”, after turned into matrix representation, we get \( M = 64, K = 9 \) and \( N = 50176 \), where \( N \) is much greater than \( M \). According to table 1, equation (2) and (4) involve thousands of times of block formatting operation, which slows the whole process. Besides, the cost of storing common exponents is much larger than equation (1) and (3). The major difference of equation (1) and (3) is the block size of \( W \). We tested the influence of block size on accuracy, shown in table 2. Experiment revealed that the top-1 accuracy of equation (3) is 1.6% higher than equation (1). Therefore, we choose equation (3) to block format \( W \) and \( I \).

### 2.4 Data Flow of Block Formatting in CNN

Giving

\[
I = \begin{pmatrix} (1.01)2 \times 2^0 \ 1.01)2 \times 2^2 \\ (1.01)2 \times 2^1 \end{pmatrix}
\]
3 Error Analysis of Block Floating Point Oriented Convolution Operations

We propose a three-stage error analysis model. The first stage is the quantization error, the second stage describes how error accumulates in matrix multiplication, and the third one describes how error is transported between convolution layers. And signal-to-noise ratio (SNR) and noise-to-signal ratio are used accordingly to simplify our statement.

3.1 Quantization Error Analysis Model

According to (Kalliojarvi and Astola 1996), for block X, the quantization error has zero mean, and variance $\sigma^2$ is described as below.

$$p_{\gamma_i} = \begin{cases} 1 & i = \varepsilon \chi \\ 0 & i \neq \varepsilon \chi \end{cases}$$

(7)

Based on that, we rewrite equation (6) to

$$\sigma_{\alpha}^2 = \frac{2^{-2L_m}}{12} \cdot 2^{2\gamma_1} \cdot 2^{2\varepsilon_1}$$

(8)

Based on equation (4), input matrix turned into a $K \times N$ block as a whole and weight matrix is block formatted into $M$ blocks with block length $K$. Thus the signal-to-noise ratio (SNR) of block floating point represented input matrix is

$$SNR_i = 10 \cdot \log_{10} \frac{E(Y^2)}{\sigma_i^2}$$

(9)

where $E(Y^2)$ is the mean square of input matrix, $\sigma_i^2$ is the energy of quantization error of $I$. To be specific,

$$\sigma_i^2 = \frac{2^{-2Lm}}{12} \cdot 2^{2\varepsilon_1}$$

(10)

Similarly, SNR of $m$th BFP represented weight matrix is

$$SNR_{w_m} = 10 \cdot \log_{10} \frac{E(X^2_{m_w})}{\sigma_{w_m}^2}$$

(11)

where $E(X^2_{m_w})$ is the mean square of $m$th row vector of weight matrix and $\sigma_{w_m}^2$ energy of quantization error of $m$th row vector,

$$\sigma_{w_m}^2 = \frac{2^{-2Lw}}{12} \cdot 2^{2\varepsilon_{w_m}}$$

(12)

The average SNR of whole weight matrix is

$$SNR_w = 10 \cdot \log_{10} \frac{\sum_{m=1}^{M} E(X^2_{m_w})}{\sum_{m=1}^{M} \sigma_{w_m}^2}$$

(13)

3.2 Single Layer Error Analysis Model

Matrix multiplication is composed of vector inner products. Therefore, researching vector inner product assists us in understanding how error is accumulated in BFP represented matrix multiplication. Giving two vectors with length $K$ as $\vec{P}$ and $\vec{Q}$, block formatted into $\vec{P}_b$ and $\vec{Q}_b$, we further define $\vec{P} = \vec{P}_b - \vec{P}$ and $\vec{Q} = \vec{Q}_b - \vec{Q}$ as the quantization error. Then the mean square of block floating point represented inner product $\sigma^2_r$ is

$$\sigma^2_r = E((\vec{P} \cdot \vec{Q})^2)$$

(14)

Assume $\vec{P}$ and $\vec{Q}$ are statistically independent, meanwhile ignore the higher order item $E((\vec{P} \cdot \vec{Q})^2)$, then

$$\sigma^2_r = E(\vec{P} \cdot \vec{Q})^2 + E((\vec{P} \cdot \vec{Q})^2) + E((\vec{P} \cdot \vec{Q})^2)$$

(15)
where
\[\|\hat{P}\|^2 = \sum_{k=1}^{K} P^2_k, \|\hat{Q}\|^2 = \sum_{k=1}^{K} Q^2_k\]
\[\|\hat{P}\|^2 \text{ and } \|\hat{Q}\|^2, \text{ denoted as } \eta_P \text{ and } \eta_Q, \text{ are noise-to-signal-ratio (NSR) of } \hat{P} \text{ and } \hat{Q}, \text{ which can be derived from SNR, e.g.}\]
\[\eta_P = 10 \log_{10} \frac{SNR_P}{SNR_{IP}}\]
where \(SNR_P\) has been discussed in equation (9). Then the NSR of inner product is
\[\eta_r = \frac{\sigma^2}{E((\hat{P} \cdot \hat{Q})^2)} = \eta_P + \eta_Q\]
(16)

Since \(o_{mn} = \tilde{w}^T_{mn} \cdot \tilde{i}_n\), we can use equation 15 to calculate the NSR of it. Further, when calculating the average NSR of \(O\), we assume that \(\tilde{w}^T_{mn}\) are independent and identically distributed, similarly to \(\tilde{i}_n\), then NSR of \(\tilde{w}^T_{mn}\) and \(\tilde{i}_n\) can be replaced with the NSR of \(W^T\) and \(I^T\). Thus the average NSR of \(O\), denoted as \(\eta_O\), is
\[\eta_O = \eta_r + \eta_W\]
(17)
where \(\eta_r\) and \(\eta_W\) are NSR of input matrix and weight matrix. Substituting equation (16), SNR of output matrix is
\[SNRO = -10 \cdot \log_{10} \eta_o = SNRP + SNRW - 10 \cdot \log_{10}\]
\[\left(\frac{SNRP}{10} + \frac{SNRW}{10}\right)\]
(18)
where \(SNRP\) and \(SNRW\) have been discussed in equation (9) and (13), thus we get the single layer error analysis model as equation (18).

### 3.3 Multi-Layers Error Analysis Model

In VGG-16, every convolution layer is followed by a ReLU layer, and the output of ReLU is the input of next convolution layer. To simplify our model, we assume that error is uniformly distributed in negative and positive output feature maps, and then we ignore the impact of ReLU layer on SNR. The difference between multi-layers model and single layer model is that the original input feature maps of multi-layers model carry error while single layer’s not. Fortunately, the quantization error is uniformly distributed on signal and carried error. Hence, we can utilize single layer model to calculate new generated error, and then we use the SNR of last layer to distinguish the carried error and signal.

\(\eta_1\) and \(\eta_2\) stand for the last layer output NSR and the NSR of block formatted input feature maps, \(E(Y^2)\), \(\sigma_1^2\) and \(\sigma_2^2\) are the energy of signal, the energy of error inherited from the last layer and the energy of quantization error. Based on equation (9) and (16),
\[\eta_2 = \frac{\sigma_2^2}{E(Y^2 + \sigma_1^2)}\]
(19)
where \(\sigma_1^2 = \eta_1 \cdot E(Y^2)\) and \(\sigma_2^2\) derived from equation (8). And then, the overall NSR \(\eta\) of this input feature map is
\[\eta = \frac{\eta_2(E(Y^2) + \eta_1 E(Y^2))}{E(Y^2)} = \eta_2 + \eta_1 \eta_2\]
(20)

### 3.4 Deviation of Error Analysis Model

Correlation between Filters and Input Feature Maps

We assumed that weights and input feature maps are statistically independent to simplify our single layer error analysis model. However, when weights and input feature maps are rather strong correlated, which results into SNR arising as noise is independent to weights while signal is not, our
model deviates from it. Another indication of strong correlation is that strong correlated layers generate more large values compared with others as filters extract aimed features from receptive fields, the higher the degree of coincidence is tends to generates more large values.

ReLU Layer ReLU (Glorot, Bordes, and Bengio 2011) is a nonlinearity layer, which drops values smaller than zero and keeps positive values as they are. In VGG-16, each convolution layer is followed by a ReLU layer, which is followed by another convolution layer or max pooling layer. In our multi-layers model, we used SNR of last convolution layer’s output as SNR of next convolution layer’s input matrix, thus the influence of ReLU layer is ignored.

Pooling Layer VGG-16 uses max pooling layer every several convolution layers to lessen the number of parameters and to control overfitting. A max pooling layer extracts the biggest number of $2 \times 2$ receptive filter with stride 2. It seems reasonable to assume that pooling layer always promote the overall SNR, if we assume bigger magnitude is sum of the products of bigger multiplier, and because bigger magnitudes have higher SNR when represented in block floating point, the SNR of the biggest number with the $2 \times 2$ filter is higher than the average SNR of the filter. However, this does not necessarily be true as it is possible that big positive and negative magnitudes offset each other, resulting a rather small value, while smaller magnitudes accumulated to a big one, and selected as the output. Because of the uncertainty pooling layer’s impact on SNR, we take the output SNR of pooling layer as the input SNR of next layer.

## 4 Experiments

### 4.1 Accuracy Test of BFP Oriented CNN

The magnitude of the decrease in accuracy is one of the most important criteria for measuring the performance of CNN accelerators. We verified BFP arithmetic on several typical deep neural networks, including VGG-16, GoogLeNet, ResNet-18 and ResNet-50, besides, smaller convolution neural networks like mnist and cifar10 are also tested.

### Experiment Setup

Caffe (Jia et al. 2014) is a popular deep learning scheme, which turns convolution operations to matrix multiplications. It is convenient to apply BFP in CNN based on caffe as we only need to rewrite the convolution function in caffe under the instruction of figure 2. To be specific, input feature maps and weights are block formatted accordingly, and then matrix multiply, finally the output feature map is transformed to floating point representation as $W'$ holds different block exponent for different row vector, because weights are block formatted row by row. What worth to mention is that ReLU and pooling layers remained unchanged, but this has no impact on our test as these two layers do not involve numeric computation.

### Results

Results are shown in table 3. $L_W$ and $L_I$ denote the bit length of weight and input mantissa after block formatted. For deep neural networks, when set $L_W$ and $L_I$ larger than or equal to 8, the drop of accuracy is less than 0.3%. In addition, 4-bit mantissa and 7-bit mantissa is sufficient for mnist and cifar10 respectively.

Another noteworthy is that the magnitude of decrease is more sensitive to $L_I$ than $L_W$. This is attributed to two factors, namely the block size of $I'$ is much larger than the size of $W'$, and the dynamic range of input feature map is much larger than weights, as our experiments revealed.

To draw a conclusion, when designing FPGA based CNN accelerators, it is a good choice to take BFP as the numeric format as BFP removed floating point computation in convolution operation, and the BFP involved decrease in accuracy is very few. Further, because BFP oriented accelerator does not acquire retraining, the cost of implementing BFP is low. And, as our experiments revealed, BFP can be used in a variety of convolution neural networks without specific reconfiguration.

### 4.2 Error Analysis Model Verifying

#### Experiments Setup

To verify error analysis model, we defined floating point represented numbers as signal, and the difference between floating point represented numbers and
| Layer   | Ex SNR  | Single SNR | Multi SNR |
|---------|---------|------------|-----------|
| conv1_1 | input   | 40.1236    | 41.8047   | –         |
|         | weight  | 43.9925    | 44.3538   | –         |
|         | output  | 37.5638    | 37.5641   | –         |
|         | ReLU    | 37.5641    | –         | –         |
| pool1   | max     | 36.3581    | –         | –         |
| conv2_1 | input   | 27.7676    | 27.3567   | 28.5668   |
|         | weight  | 34.1054    | 31.9899   | 31.9899   |
|         | output  | 30.0439    | 28.3815   | 27.7393   |
|         | ReLU    | 35.1707    | –         | –         |
| pool2   | max     | 26.2151    | –         | –         |
| conv3_1 | input   | 23.7616    | 29.3567   | 28.5668   |
|         | weight  | 33.7565    | 34.9562   | 34.9562   |
|         | output  | 25.3109    | 26.5601   | 26.3628   |
|         | ReLU    | 23.311     | –         | –         |
| pool3   | max     | 21.7996    | –         | –         |
| conv4_1 | input   | 20.1885    | 27.9558   | 28.5668   |
|         | weight  | 31.0773    | 32.5038   | 32.5038   |
|         | output  | 22.9078    | 24.9042   | 20.0699   |
|         | ReLU    | 22.9214    | –         | –         |
| pool4   | max     | 18.8514    | –         | –         |
| conv5_1 | input   | 18.5113    | 24.4103   | 18.786    |
|         | weight  | 31.0754    | 32.2424   | 32.2424   |
|         | output  | 22.1491    | 23.7497   | 17.6331   |
|         | ReLU    | 22.1483    | –         | –         |
| conv5_2 | input   | 18.4841    | 33.9519   | 33.9193   |
|         | weight  | 32.4689    | 33.6544   | 33.6544   |
|         | output  | 23.6306    | 23.6976   | 15.7846   |
|         | ReLU    | 23.6191    | –         | –         |
| pool5   | max     | 17.7955    | –         | –         |

Table 4: Experimental and theoretical SNR. In this table, “ex SNR”, “single SNR” and “multi SNR” respectively represent experimental SNR, single layer model calculated SNR and multi-layer model calculated SNR.

Figure 3: energy distribution comparison of layer “conv1_1”, “conv1_2”, “conv2_1” and “conv2_2”. The horizontal axis represents normalized magnitude from 0.8 to 1, and the area shows the comparison of each layer’s normalized energy.

BFP represented numbers as error. And then, we ran VGG-16 on ILSVRC2012 for 20 iterations with batch size set to 50 to gather data, such as the output of every layer and the input feature maps and weights of convolution layer. These data are stored in separated files in binary format, with which we calculate the signal energy and error energy to derive the experimental SNR.

**Results** As shown in table 4, the theoretical data are in good agreement with the experimental data, where the biggest difference between them is less than 8.9dB, which is close enough to guide hardware design. What worth to mention is that previous assumptions about ReLU layer proved to be reasonable. To be specific, the SNR of ReLU output is consistent with its input SNR, which proved that the output of convolution layer is evenly distributed in the positive and negative parts. And, the impact on SNR of pooling layer acts exactly as what we assumed.

We calculated the energy distribution of layer “conv1_2” as it induces the largest deviation, layer “conv1_1”, “conv2_1” and “conv2_2” are also tested as reference. Figure 3 reveals that, compared with other two layers, the energy of layer “conv1_2” is more concentrated at large value, which indicates stronger correlated.

### 5 Conclusion

In this paper, we designed a CNN accelerator that replaced floating point representation with BFP representation. With BFP, floating point computation in convolution layer, which is the majority of total computation, is replaced with fixed point computation and up to 75% bandwidth requirement of convolution layer is saved. Meanwhile, drop in accuracy of deep neural networks is less than 0.3% without retraining. In addition, we developed the NSR upper bound with the largest deviation less than 8.9dB, which provides guidance for hardware design.

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