Scalar Arithmetic Multiple Data: 
Customizable Precision for Deep Neural Networks

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Abstract—Quantization of weights and activations in Deep Neural Networks (DNNs) is a powerful technique for network compression, and has enjoyed significant attention and success. However, much of the inference-time benefit of quantization is accessible only through customized hardware accelerators or with an FPGA implementation of quantized arithmetic.

Building on prior work, we show how to construct very fast implementations of arbitrary bit-precise signed and unsigned integer operations using a software technique which logically embeds a vector architecture with custom bit-width lanes in fixed-width scalar arithmetic. At the strongest level of quantization, our approach yields a maximum speedup of $\sim 6 \times$ on an x86 platform, and $\sim 10 \times$ on an ARM platform versus quantization to native 8-bit integers.

I. Motivation

Quantizing weights and activations in DNNs can reduce (1) the size of data, which reduces the required memory footprint, and (2) memory traffic, which consumes execution time and energy [2]. Performing inference in reduced bit precision also offers the possibility of decreased execution time. Quantization is extraordinarily effective for DNNs, and many networks can function correctly under very aggressive quantization [17].

Custom hardware accelerators [10], [12], [11] and FPGAs [6] can exploit this reduction in data precision to reduce the area and power required for the implementation of the corresponding arithmetic, and also to increase throughput. In contrast, conventional CPU/GPU microarchitectures typically provide native support for just a few fixed levels of precision, such as 8-, 16-, 32- and 64-bit integer values and 32- and 64-bit floating point. The result is that software is seldom able to take full advantage of relaxed precision requirements. For example, Ristretto [3] can quantize DNN activations to signed 6-bit integer precision, but we are unaware of any machine with 6-bit native arithmetic to implement the operations.

Contribution

In this paper we show that bit-level custom precision on commodity hardware is not only possible, but highly efficient for deep convolutional neural networks (CNNs). We extend prior research to embed a SIMD vector architecture with custom bit-precise integer vector lanes in native fixed-width scalar arithmetic. We implement a wide range of operations over arrays of bit-precise signed and unsigned integer types.

However, merely emulating the lane-wise operations of existing vector architectures neglects the true potential of custom precision in software. Instead, we argue that the greatest opportunities arise from defining entirely new operations that do not necessarily correspond to existing SIMD vector instructions.

These new operations are not easy to find because they depend on novel insights into the sub-structure of existing machine instructions. Nonetheless, we provide an example of one such operation: a custom bit-level precise operation which computes the 1D convolution of two input vectors, based on the wide integer multiplier found in general-purpose processors.

Mixed signed-unsigned integer arithmetic is a particular challenge, and we present a novel solution. While the performance benefits are attractive, writing this kind of code by hand is difficult and error prone. We implement the technique in a domain-specific code generator, which synthesizes efficient C code implementations of the arithmetic operations.

We evaluate our approach using published quantization scenarios on multiple hardware platforms, including embedded/IoT class devices.

II. Background

Vector computer architectures are among the most successful parallel computers for a wide variety of applications. In the 1970s supercomputers such as the Cray-1 and Cray X-MP used deeply-pipelined vector floating point units for performance on scientific applications. From the mid-1990s vector units started to appear in general-purpose processors, such as Intel MMX (1996) and SSE (1999) and PowerPC AltiVec (1997). Vector processors are single-instruction multiple data (SIMD) parallel computers, where a single instruction operates on multiple data points in parallel.

Modern vector processors have vector registers that contain a fixed number of lanes, each of which contains a scalar value. Vector instructions operate on all lanes in parallel, using either pipelined arithmetic units (a vector pipeline architecture) or using multiple parallel arithmetic units (a vector SIMD architecture [13]). It is worth noting that both vector SIMD and vector pipeline architectures fit within the SIMD category of Flynn’s taxonomy [5].

In 1997 Fisher and Dietz proposed a slightly different classification of vector architectures [4]. They coined the term SIMD within a register (SWAR) to encompass both the then-emerging vector SIMD architectures and another approach to vector parallelism that is less well known. This latter approach is a software-only emulation of vector computing
that is implemented with scalar instructions. Scalar registers are divided into notional sub-words, and scalar instructions are used to operate on multiple sub-words in parallel.

Fisher and Dietz went on to create a SWAR programming model and compiler that could target either conventional vector instructions or a software emulation of vectors using scalar instructions. Unfortunately, Fisher and Dietz overloaded the term SWAR to include three quite separate ideas: (1) all hardware vector SIMD architectures, (2) their approach to software emulation of vector architectures, and (3) their high-level programming model and compiler. As a result, despite doing much pioneering work in the field, they left no separate term for software emulation of vector architectures. In the absence of an existing term, we refer to this software vector approach as Scalar Arithmetic with Multiple Data (SAMD).

Algorithms to operate on multiple subwords in parallel have been known for some time. A 1957 programming textbook for the 35-bit EDSAC contains a recursive divide and conquer algorithm to compute the number of set bits (or popcount), where the bit-width of each partial sum doubles on each iteration. The famous 1972 HAKMEM technical report from MIT contains an example (no. 115) that operates on base-4 subwords using bitwise operations.

In 1975 Lamport outlined a vision for processing multiple n-bit “bytes” within full word instructions (where n is not necessarily eight). Lamport outlines an algorithm for SAMD addition with and without spacer bits, and mentions the possibility of vector times scalar multiplication albeit without details. The main focus of the work is lane-wise comparisons and masks, particularly for processing character data.

Fu et al. present a method for multiplying two 8-bit inputs by an 8-bit scalar value in a single step using the DSP accelerator units on Xilinx FPGAs. According to their description — which is tightly bound to implementation on Xilinx FPGAs — their approach can deal with both signed and unsigned numbers.

Umuroglu et al. propose FINN, another hardware framework for fast binarized neural network inference. In their formulation, points in a convolution can take on the values from the set \{-1,0,+1\}. This quantization scheme can be represented without loss of accuracy in our SAMD 2 format, which permits the values \{-2,-1,0,+1\}. Umuroglu et al. propose to use a customized hardware unit, implemented on FPGA to actually perform inference.

### A. Emulating Vector Architectures

On a 64-bit 8-way vector architecture, 64-bit vector registers can be divided into eight lanes, each containing a single byte.

```c
uint64_t unsigned_add_spacer(uint64_t a, uint64_t b, int bits)
{
    // create mask with zeros in spacer bits
    uint64_t mask = ~MSB_LANE_MASK(bits+1);
    // clear the spacer bits in each input
    uint64_t a_clear = a & mask;
    uint64_t b_clear = b & mask;
    // add the numbers
    return a_clear + b_clear;
}
```

Fig. 1: Correct (0) and incorrect (1) carries in scalar addition on 4-bit data when packed in a 16-bit data word. Incorrect carries corrupt neighbouring packed values.

Fig. 2: Addition of unsigned SAMD vectors using one permanent spacer bit between each lane.

Vector arithmetic instructions can be used to perform operations such as lane-wise addition. It is equally possible to pack the same eight bytes into a 64-bit scalar register, but applying scalar addition will not give a correct result (Figure 1). The problem is that scalar arithmetic assumes that all bytes are parts of a singular integer value.

Scalar addition computes carries across the entire 64-bit word. In contrast, vector operations break the carry-chain at the boundary of each lane. To emulate vector arithmetic using scalar arithmetic, some software mechanism is needed to sever the carries at vector lane boundaries. Fisher and Dietz proposed spacer bits to solve this problem.

Spacer bits consist of one or more bits placed between vector lanes to catch carries from the neighbouring lane. In the example in Figure 2 a single spacer bit is added between each lane, and as a result only seven one-byte values fit within the 64-bit word alongside the spacer bits.

To perform unsigned vector addition using unsigned scalar addition, the spacer bits must first be set to zero. We set the spacer bits in the inputs, a, b to zero, using a 64-bit mask, and then add the two resulting values. Any overflows at lane boundaries are caught in these spacer bits. We refer to these as permanent spacer bits because they persist throughout the lifetime of the value.

Note that throughout this paper we use many bitwise masks to isolate particular lanes or bits within a word. The particular value of the mask typically depends on the lane-width and the presence or absence of spacer bits. To describe these masks clearly, we introduce a small function as shown in Figure 3.

### B. Temporary Spacer Bits

A downside of permanent spacer bits is that they occupy space within the vector word. Fisher and Dietz proposed virtual spacer bits to prevent overflow between lanes without permanent spacer bits.

A virtual spacer bit is a short-lived spacer bit that is introduced within a routine for operating on SAMD vectors and is eliminated before the completion of the routine. We refer to these as temporary spacer bits.

Figure 4 shows unsigned addition using this approach, computing the correct answer for the addition from Figure 1. The most significant bit of each lane is masked to zero and acts as a temporary spacer bit. The scalar addition is performed...
C. Our Thesis

In this paper we argue that emulating existing vector instruction sets is exactly the wrong use of software techniques to perform vector arithmetic with scalar instructions. Vector instruction sets are now ubiquitous, and it is difficult for SAMD techniques to compete when performing the same operations. On the contrary, we argue that SAMD is most effective when it is used for operations that are not already supported by vector instructions. In particular we argue that SAMD is ideal for customized integer data precision in approximate computing applications. Further, as we show in Section V, SAMD can sometimes exploit the structure of scalar arithmetic to perform multiple vector operations using a single scalar instruction. To demonstrate our point, we first review examples of SAMD operations that emulate existing vector instructions.

Fig. 3: Construct a mask for clearing bits and lanes in SAMD computation, and examples of masks used throughout paper.

```c
uint64_t build_mask(int start, int len, int stride)
{
    // create a mask of len 1's
    uint64_t sub_mask = (1 << len) - 1;
    uint64_t mask = 0;
    // lay down the sub_mask at intervals of stride
    for(int i = start; i < size((uint64_t)*8; i += stride){
        mask = mask | (sub_mask << i);
    }
    return mask;
}
#define MSB_LANE_MASK(w) build_mask(w-1, 1, w)
#define LSB_LANE_MASK(w) build_mask(0, 1, w)
#define ODD_LANE_MASK(w) build_mask(w, 2w)
#define EVEN_LANE_MASK(w) build_mask(0, w, 2w)
```

Fig. 4: Dataflow in SAMD addition with temporary spacer bits on 3-bit values, and any overflow is caught in the temporary spacer bits.

To get a full 4-bit result in each lane, it is necessary to replace the temporary spacer bit with the correct value of the most significant bit of the addition. Fortunately, one-bit addition can be computed with bitwise xor of the most significant bit of each of the two input and of the carry bit that is stored in the temporary spacer bit.

Temporary spacer bits remove the need for persistent spacer bits at the cost of some additional computation. This greatly simplifies the task of emulating operations found in hardware vector instruction sets such as Intel MMX or SSE.

III. CONVENTIONAL SAMD ARITHMETIC

Fisher and Dietz published only a handful of their SAMD operations, but the source code of Fisher’s compiler for the “SWARC” language contains many more. Figure 5 shows simplified versions of SAMD operations for integer add and subtract. These operations are correct for both signed and unsigned values, and can be used for lane-widths with any fixed number of bits.

Unfortunately there is no efficient way to compute lane-wise multiplication using scalar multiplication instructions. Unlike addition with its single linear carry-chain which can be broken using bitwise operations, multiplication has many carry chains. The code generator in Fisher’s SWARC compiler can generate a sequence of bitwise shift, mask and add instructions that are capable of performing lane-wise multiplication. Their instruction sequence is complex and requires $O(b)$ iterations of a shift and add algorithm, where $b$ is the lane-width. Further, each iteration uses $O(\log_2 b)$ operations to build a mask, for a total of $O(b \log_2 b)$ operations to complete lane-wise SAMD multiplication.

In Figure 6 we present an improved lane-wise SAMD multiplication sequence that requires just $O(b)$ operations for SAMD multiplication. Our approach builds the write mask for the multiplication in a constant number of steps. We rely on the observation that we can efficiently compute an integer, $mask$ with all bits in the range start to stop set to 1, where $start > stop$; we simply compute $mask = (1 \ll start) - (1 \ll stop)$.

```c
uint64_t samd_add(uint64_t a, uint64_t b, int bits)
{
    uint64_t mask = MSB_LANE_MASK(bits);
    uint64_t msb = (a ^ b) & mask;
    uint64_t sum = (a & ~mask) + (b & ~mask);
    return msb ^ sum;
}
```
uint64_t unsigned_scale_b_spaces(uint64_t vec, uint64_t scalar, int bits)
{
    // clear the spacer bits in the input
    uint64_t mask = ODD_LANE_MASK(bits);
    uint64_t vec_clear = vec & mask;

    return vec * scalar;
}

Fig. 7: Unsigned vector scale with $b$ permanent spacer bits

IV. VECTOR SCALE

Although lane-wise vector multiplication of SAMD vectors cannot be efficiently implemented with a scalar multiply instruction, another useful operation can be. Key operations of many algorithms such as matrix multiplication and discrete convolution can be expressed as vector scale operations, where a vector of values are multiplied by a single scalar.

The very simplest case of vector scaling operates on unsigned lanes of $b$ bits, where each lane is separated by $b$ permanent spacer bits. In this case, vector scaling can be implemented by a scalar unsigned multiplication as shown in Figure 7. In this example the scalar value occupies the lowest $b$ bits of the scalar parameter. The vector contains several $b$ bit values, each separated by $b$ permanent spacer bits. The product of two $b$ bit numbers contains $2b$ bits, with the $b$ bits of overflow stored in the permanent spacer bits.

As we have seen for other operations, a weakness of using permanent spacer bits is that they occupy space in the input and result. Assuming that we want a $b$ bit result in each lane, we can simply ignore or mask out the contents of the spacer bits. However, it is worth noting that the $b$ bit vector scale actually returns a product of $2b$ bits — the lower half in the result bits, and the upper half in the neighbouring spacer bits.

A. Vector Scale with Temporary Spacer Bits

The downside of permanent spacer bits can be avoided by using temporary spacer bits for vector scale as shown in Figure 8. We first extract odd and even numbered lanes of the vector into separate registers using bitmasks, which creates $b$ zero-valued spacer bits between each lane. We duplicate each of the odd and even vectors by the $b$-bit scalar. The result is two sets of vectors where each lane contains a $2b$-bit value. Finally, we mask off the upper half of each lane, and merge the odd and even vectors into a single vector of $b$-bit values.

Note that when multiplying two $b$-bit integers, the result in the lower $b$ bits is the same regardless of whether we use unsigned or two’s-complement signed multiplication [7]. Therefore, the routine in Figure 8 gives the correct $b$-bit result in each lane for either signed or unsigned SAMD arithmetic. Each signed lane of the vector gets the correct value, despite the fact that the routine uses unsigned arithmetic on the underlying integer type that is used to store the SAMD vector.

V. CONVOLUTION

The most computationally-intensive operation in CNNs is convolution. Simple 1D convolution can be used to express other operations, such as polynomial multiplication.

uint64_t vector_scale_wrap(uint64_t vec, uint64_t scalar, const int bits)
{
    // separate odd and even numbered lanes
    uint64_t even_mask = EVEN_LANE_MASK(bits);
    uint64_t odd_mask = ODD_LANE_MASK(bits);
    uint64_t even = vec & even_mask;
    uint64_t odd = vec & odd_mask;

    // compute product and mask out higher half
    even = (even * scalar) & even_mask;
    odd = (odd * scalar) & odd_mask;

    return even | odd;
}

Fig. 8: Vector scale with $b$ temporary spacer bits.

For example, the two polynomials $2x^2 + 3x + 7$ and $x^2 - 5$ can be expressed as vectors $a = [2, 3, 7], b = [1, 0, -5]$. The product of the polynomials can be expressed as the convolution $conv(a, b)$. Likewise, convolution can be expressed as products of polynomials. Given that we already have computer hardware to perform multiplication of numbers in a positional system, an intriguing question arises: can we use the same hardware multipliers to perform convolution?

The polynomial product is similar to numeric multiplication, except that it does not allow overflow from one coefficient to the next. Therefore, if we can prevent overflow between coefficients is to ensure that there are enough bits in each lane of the result to ensure that overflow cannot happen.

As we saw in Section IV, we can scale an unsigned vector with $b$-bit lanes by a $b$-bit unsigned scalar using native full-word multiplication by ensuring that there are always $b$ spacer bits between each lane of the SAMD vector. We can use a similar technique to perform convolution of SAMD vectors, by ensuring that there are always enough bits in each result lane to contain the maximum value computable by the convolution.

Consider the case where we convolve a vector of $b$-bit values by a 1D convolution kernel of three $b$-bit values. Each output point in the result consists of the sum of three values. Each of these values is the product of a $b$-bit input value and a $b$-bit kernel value, which gives a $2b$-bit result.

The sum of these three values requires a maximum of $2b + 2$ bits to represent. Therefore, if we guarantee that the output lane into which we compute such a value has $2b + 2$ bits, then there will never be overflow between output lanes. One way to ensure that each output lane has $2b + 2$ bits is to modify the inputs so that each input and kernel lane has $b + 1$ bits and is separated by $b + 1$ spacer bits.

It is worth reiterating that our objective is not to guarantee the absence of overflow in general, but to provide the same overflow behaviour as a $b$-bit scalar value. However, if $b$ bits is not enough, the programmer needs to use a higher precision. For DNN applications, the exact precision for quantization of each convolution is often discovered through some type of iterative search procedure.
Fig. 9: Convolutional substructure in unsigned multiply

The effect of putting each $b$-bit value into an input lane with $2b + 2$ bits (including spacer bits) is that we can consider ourselves to be performing arithmetic on values with base $2^{2b+2}$. By design each input has only $b$ bits, so we are guaranteed that our base-$2^{2b+2}$ convolution never overflows between lanes. Thus, we can perform SAMD convolution using multiplication.

Consider the example in Figure 9. We have four input values $i_0, i_1, i_2, i_3$ and a 1D convolution kernel of three values $k_1, k_2, k_3$. The input and the kernel are packed into SAMD vectors with zero-valued spacer lanes between each lane containing a value. Figure 9 shows each intermediate value that is computed as part of the long multiplication.

Each intermediate value is the product of two inputs and is therefore occupies a double-width lane in the result. When performing the multiplication we use machine instructions that compute the full double-width result. For example, the x86-64 architecture has a 64-bit multiply instruction that returns a 128-bit result split across two registers. The result contains the convolution of the input and kernel.

Note that the example in Figure 9 has an input of length four and kernel of length three. Each fits within a single SAMD register, and it is therefore possible to compute the convolution with just a single multiply. In convolutional neural networks the kernel typically has a short, fixed length such as three or five. However, the input is normally much longer, and we must therefore typically compute the convolution of a kernel that fits within a single SAMD register, and an input sequence that does not.

If we again consider the example in Figure 9 but assume that the input is just a short subsection of a much larger input, a pattern emerges. In a long convolution with a kernel of length three, we expect all output to consist of the sum of three products. In the example we see that two lanes of the output — those containing the values $k_3i_0 + k_2i_1 + k_1i_2$ and $k_3i_1 + k_2i_2 + k_1i_3$ — are the sum of three non-zero products. These two output values are complete result values of the overall convolution. In contrast, the other four outputs are partial results. Each is the sum of just one or two products. To compute the final results for these output points, we need to combine partial results from different multiplications.

If we look at the pattern of non-zero intermediate values of the multiplication in Figure 9 we see that they form a parallelogram-shaped region. When we perform a longer convolution the result is a sequence of such parallelograms.

```c
uint64_t samd_sign_extend4mul(uint64_t vec, int bits) {
    // get mask with 1 in MSB of each lane
    uint64_t mask = vec & MSB_LANE_MASK(bits);
    // extract the sign bits of each lane
    uint64_t sign_mask = vec & mask;
    // subtract sign bits from adjacent spacer bits
    return vec - (sign_mask << 1);
}
```

Fig. 10: Special-purpose sign extension for vector scale or convolution

To get the result of a long convolution we simply align the adjacent parallelograms by bit shifting the output word and add the overlapping points. In this way, we can build the convolution of a sequence of arbitrary length piecewise from overlapping and adding fixed-size convolutions.

VI. HANDLING OF SIGNED VALUES

Our discussion of SAMD convolution and vector scale has so far assumed that inputs are unsigned. However, CNNs normally use signed values, at least for the convolution kernel.

Most processors provide separate signed and unsigned multiply instructions. The lower $b$ bits of the result of multiplying two $b$-bit values is the same for both signed and unsigned multiplication. However, the higher $b$ bits of the result are different depending on whether the multiplication is signed or unsigned.

If we are operating on $b$-bit inputs and computing $b$-bit outputs, multiplication of signed values is straightforward. We simply compute the $2b$-bit result using whatever multiplication is available and discard the upper $b$ bits. However, multiplying $b$-bit signed inputs to create $2b$-bit results is much more complicated, because signed scalar multiplication deals only with the leading bit of the full machine word as the indication of a negative value.

The issue is that the signed scalar multiplier is unable to identify signed SAMD lanes within a machine word. Our approach therefore uses unsigned scalar multiplication, with a fixup operation to adjust the result to account for negative values in lanes. Grys [7] provides an overview of software methods for computing signed multiplication by adjusting the result of unsigned multiplication.

For simplicity, we assume the input vector and convolution kernels consists of signed $b$-bit integer lanes, each separated by $b$ zero-valued spacer bits. Note that scalar times vector multiplication is simply a special case of convolution, where the kernel contains just one value.

To sign-extend a negative lane, we need to extend its leading sign bits into the adjacent $b$ zero-valued spacer bits to its left. Figure 10 shows a simple method for sign extension. We shift the leading sign bit of each vector lane by one position, and subtracting it from the adjacent spacer bit to the left. Where the leading sign bit has value zero, that lane contains a positive (or zero) number, and zero is subtracted from the adjacent spacer bit leaving it zero.

Where the leading sign bit is one, the number is negative, and all $b$ spacer bits must be set to one to fully sign extend...
```c
uint128_t signed_convolution(uint64_t vec, uint64_t kernel, int bits)
{
    // compute 128 bit product of 64-bit inputs
    uint128_t product = (uint128_t)vec * (uint128_t)scalar;
    // fix underflow from adjacent lane
    uint128_t mask = MSB_MASK(bits+2);
    uint128_t sign_bits = product & mask;
    // add the sign bit to itself to increment
    // lane to the left of a negative number
    product = product + sign_bits;
    // correct the MSB for wrongly removed sign
    return product & sign_bits;
}
```

Fig. 11: Signed convolution algorithm with underflow correction

The method of signed convolution presented so far has assumed that we need to compute the correct value for the MSB of each vector lane. However, it is worth noting that computing the correct MSB can be surprisingly expensive for SAMD operations.

For example, in the SAMD addition operation in Figure 4, half of the bitwise operations are devoted to computing the correct value of the MSB. If we are willing to sacrifice one bit of precision and not maintain the MSB, SAMD addition is much more efficient. Where we maintain a permanent spacer bit in the MSB of each SAMD lane, we can use cheaper operations, such as the addition in Figure 2 which uses far fewer bitwise operations.

In the case where we maintain a permanent spacer bit in the MSB of each lane, we can also perform convolution more efficiently. First, the final xor operation in the convolution code in Figure 11 is unnecessary if we do not need to compute the MSB. Given that the xor operates on a double-width value (in this case 128 bits), this likely corresponds to two scalar machine instructions.

A second optimization of convolution arises because of the way that we correct for negative adjacent lanes. Recall that to correct for negative lanes we extract the sign bit from the result of the multiplication and add it back into the result. Where the sign bit has value 1, this propagates a positive carry into the neighbouring lane. Unfortunately this operation also corrupts the sign bit, but where the MSB is a spacer bit, this is not a problem. However, the result of the addition can leave the lane of a SAMD vector in one of two possible states.

If before the addition, the SAMD lane contained the value -1, then after the addition, the SAMD lane contains the value zero in all bits except the MSB, which has value 1. If before the addition the SAMD lane contained any other value, then after the addition it contains a zero in the MSB and arbitrary values in other bits.

In CNN convolution, the output of our convolution operation is normally added to an accumulation of the values across multiple channels. Where a permanent spacer bit is used in SAMD lanes, we normally clear the MSB of each operand before performing the addition (as shown in Figure 2).

However, given that the MSB of each lane in the output of our convolution operation is already zero all cases, except the case where it is one and all other bits are zero, addition with a SAMD lane where the MSB is zero cannot overflow into the neighbouring lane. Therefore, where the output of our convolution feeds directly into addition with a permanent spacer bit, there is no need to clear the MSB of the lanes of our convolution result.

VII. EXPERIMENTAL EVALUATION

To implement low precision integer arithmetic on a general purpose processor without hardware support, the simplest option available to the programmer is to unpack the low-precision values into the closest available native integer type. On the vast majority of commodity processors, the smallest
integer type is 8 bits in length. For example, the pointwise sum of two streams of 6-bit integers can be computed by zero-padding the values to 8 bits, and using native 8-bit addition.

Using this approach, the arithmetic sequence performing any computation on streams of values smaller than 8 bits is identical, with the only adjustment being the number of zeroes used to inflate individual elements (i.e., the shift factor, on machines which shift in zeroes).

The class of convolutions with inputs of width at most 8 bits is precisely the target of our evaluation, since these are typically only used when hardware acceleration is available. Figure 12 shows some example C code implementing DNN convolution. For our evaluation, we built a small code generator which synthesizes the SAMD instruction sequence implementing the highlighted arithmetic, using the underflow correction approach from Figure 11. Since unpacking to native 8-bit integer arithmetic can be used for all narrower bitwidths, the performance of the native 8-bit version of the code is our baseline for benchmarking.

After we generate the C code implementing the SAMD arithmetic operations, we compile everything to machine code using the native compiler (in our case, GCC release 7.2).

```c
for (unsigned m = 0; m < kernels; m++)
  for (unsigned h = k/2; h < (img_h-(k/2)); h++)
    for (unsigned w = k/2; w < (img_w-(k/2)); w++)
      T result = output[m][h][w];
      for (unsigned d = 0; d < channels; d++)
        for (unsigned y = 0; y < k; y++)
          result +=
            (T)image[d][(h + y)-(k/2)][(w + x)-(k/2)]*
            (T)kernel[m][d][y][x];
      output[m][h][w] = result;
```

Fig. 12: DNN convolution (DIRECT-SUM2D).

The entire coloured area corresponds to a single $k \times k$ 2D convolution, and the orange area specifically corresponds to the 1-dimensional sub-convolution which is implemented by the SAMD convolution operator.

A. Experimental Setup

We evaluated our approach on an AMD Ryzen 7 2700X, and on an ARM Cortex-A57. For our experiments we are using the convolutional layers of the VGG-B network of Simonyan et al. [4]. From left to right on the graphs, the depth of the layer in the network increases, increasing the number of channels and the number of convolutional kernels. The precise dimensions of each convolution are tabulated in [4].

The $SAMD(N)$ bars show the performance of our generated SAMD convolution layer when quantized to $N$-bit signed integer weights and activations. In experiments, we step $N$ down from 8 (emulating native 8-bit integers) to 2 (a single data bit with a sign bit).

Recall from Figure 9 that each individual multiply instruction generated to implement the SAMD arithmetic sequence computes multiple subterms of the overall sum-of-products in a $k \times k$ 2-D convolution. If $t$ inputs are convolved with a $K$ point kernel, the SAMD arithmetic uses only $(I - K) + 1$ integer multiplies and $(I - K)$ integer additions to compute the result, while the native arithmetic must use $(I \times K)$ multiplies and adds to compute the result. Since the length of the machine word is fixed, $I$ is larger for smaller types. Using 3-bit integers with 64-bit machine words, a 3-point 1D convolution can be computed using only $(10 - 3) + 1 = 8$ multiplies using SAMD arithmetic, while the native 8-bit code requires 30 multiplies.

B. Experimental Results: Ryzen 7

Figures 13 and 14 show the results of benchmarking on Ryzen 7. Using temporary spacer bits, a more complex instruction sequence is required (shown in Figure 4) than where the format contains permanent spacer bits, leading to a higher execution time overall. Although using temporary spacer bits minimizes memory, the overhead of the more complex instruction sequence is clearly visible in the execution time.

The Ryzen 7 processor has fast native SIMD vector instructions for 8-bit integer arithmetic. In convolution layers late in the VGG network, with very large numbers of channels, the native 8-bit SIMD code is faster than some of the wider SAMD instances with temporary spacer bits, but in general, as the quantization factor increases (meaning we can fit more values in a SAMD vector) the performance of SAMD improves.

The best available speedup for an individual convolution layer, using 2-bit quantization, is approximately $6\times$. 

![Fig. 13: AMD Ryzen 7 2700X: Temporary Spacer Bits](image1)

![Fig. 14: AMD Ryzen 7 2700X: Permanent Spacer Bits](image2)
C. Experimental Results: ARM Cortex-A57

On the ARM Cortex-A57, the SAMD code for temporary spacer bits is faster than unpacking to native integers for all SAMD widths less than 8 bits (Figure 15). This is likely due to the narrower issue width and increased operation latency versus the Haswell processor. Using permanent spacer bits (Figure 16), the gap widens even further. Where the incoming data are in reduced precision, SAMD is a very effective mechanism to achieve parallelized execution on constrained processors such as the Cortex-A57.

Using the low-complexity operations with permanent spacer bits (Figure 16), the best speedup available for an individual SAMD convolution layer, using 2-bit quantization, is approximately $10\times$ versus native 8-bit integer implementation.

VIII. CONCLUSION

Our approach allows proven quantization schemes from prior work to be run on a general-purpose CPU in a highly efficient manner. As we have demonstrated, the layers of this network can be run on a Cortex-A57 with a 2-bit quantized inference scheme yielding a speedup approaching $10\times$ for several layers.

As demonstrated by our experimental evaluation, quantization can enable not only memory savings, but also inference performance gains without requiring custom hardware support. Software support for bit-precise quantized DNN operations using our approach can often match, and sometimes far exceed, the performance of inference quantized to the sizes supported in native arithmetic.

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