High-frequency resonant gate driver with isolated class-E amplifier

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Abstract: This paper proposes the high-frequency resonant gate driver, which is based on the class-E amplifier with isolation transformer, for driving SiC MOSFETs. By applying the isolation transformer to the resonant filter, the destruction risk decreases in the proposed driver. It is possible to obtain the sinusoidal driving waveform without distortion because the proposed driver includes the gate capacitance and the gate resistance in the resonant circuit. Additionally, low power consumption of the driver can be achieved by satisfying the class-E zero-voltage switching and zero-derivative switching conditions. Therefore, the thermal problem can be mitigated in the proposed driver. As a result, the proposed driver is suitable for the SiC driver at high frequencies, in particular. The high-frequency SiC drive was confirmed by simple test circuit. Additionally, the 7 MHz SiC class-E amplifier was implemented, which was driven by the proposed driver. The validity of the analytical expressions and the design procedure were shown by the quantitative agreements between analytical and experimental results.

Key Words: resonant driver, SiC MOSFET, high frequency, low power consumption, class-E amplifier

1. Introduction

Silicon Carbide (SiC) devices attract attentions as next generation semiconductor devices. SiC power devices have characteristics of high breakdown voltage and low on-resistance, which are suitable to high-frequency and/or high-power applications. A gate driver is, however, one of the bottlenecks for achieving high-frequency operations with SiC devices [1–9]. This is because the gate capacitance and the gate resistance of SiC devices are generally larger than those of silicon (Si) and gallium nitride (GaN) devices. The design of high-frequency SiC drivers is an important problem for practical realization of SiC devices.

Under these backgrounds, high-frequency gate drivers for SiC MOSFETs have been recently proposed [1–4]. These drivers, however, have large switching losses because of the hard-switching operation, which causes a thermal problem. Additionally, the output voltage of these drivers is a rectangular waveform. In actual SiC drive with these drivers, the square-voltage output is applied to the gate terminal. As a result, the gate voltage is distorted due to the gate capacitance of the SiC MOSFETs,
which no longer looks a square waveform. The resonant gate driver [9–16] is one of the solutions to the above problems. In the resonant driver, the gate capacitance and the gate resistance are included in the output resonant filter. Therefore, it is unnecessary to consider the gate-voltage distortion. Additionally, soft-switching techniques can be applied to the switching device of the driver. Therefore, the thermal problem is mitigated compared with hard-switching drivers.

The class-E amplifier [17–27] is a typical high-frequency resonant circuit. Because the switch voltage can satisfy the class-E zero-voltage switching and zero-derivative switching (ZVS/ZDS) conditions in the class-E amplifier, it is possible to achieve low switching losses at high frequencies. Because of high-efficiency characteristic, the class-E amplifier is suitable to the resonant driver [9, 10]. Because high power applications are main targets of SiC devices, high voltage may appear across drain-to-source of the SiC MOSFETs. This means that the SiC driver has a risk to cause electrical destructions. Therefore, the isolation measure is required for ensuring safety [2, 7–9].

This paper, which is the extended version of [9], proposes the resonant gate driver which is based on the class-E amplifier with isolation transformer, for driving SiC MOSFETs. The proposed driver has the same advantages as the previous class-E driver, which are the decrease in the driving-voltage distortion and thermal-problem mitigation. By having the isolation transformer in the resonant filter, the destruction risk decreases in the proposed driver. The analytical expressions and step-by-step design procedure of the proposed driver are presented. The high-frequency SiC drive was confirmed by simple driving-test circuit. Additionally, the SiC class-E amplifier with 7 MHz and 109 W output was implemented in this paper, which was driven by the proposed driver. It can be stated from the experimental results that the proposed driver is useful for high-frequency drive of SiC MOSFETs. The validities of the analytical expressions and the design procedure were shown by the quantitative agreements between the analytical and experimental results.

2. Circuit description

This section introduces the class-E amplifier, which is the basic circuit of the proposed driver, and its operation. In the proposed gate driver, isolated transformer is adopted at the resonant filter of the class-E amplifier.

2.1 Class-E amplifier

Figure 1 shows a circuit topology of the class-E amplifier [17]. The class-E amplifier consists of dc-supply voltage $V_{DD}$, dc-feed inductance $L_C$, MOSFET $S$ as a switching device, shunt capacitance $C_S$, resonant circuit $L_1 – C_1$, and load resistance $R$. When the dc-feed inductance is sufficient large, the current flowing through the dc-feed inductance is regarded as a direct current. Namely, the dc-supply voltage and the dc-feed inductance are modeled as a direct current source. Additionally, the MOSFET works as an ideal switching device. Therefore, the equivalent model of the class-E amplifier

![Fig. 1. Circuit topology of the class-E amplifier. (a) Fundamental circuit topology. (b) Equivalent circuit.](image-url)
is illustrated as shown in Fig. 1(b) [18].

Figure 2 shows example waveforms of the class-E amplifier. In this paper, it is assumed that the switch turns on and off at $\theta = 0$ and $2\pi(1 - D)$, respectively. When the loaded quality factor is high, the current through the resonant filter $i_1$ is a pure sinusoidal wave. During the MOSFET is in off-state, the difference of the input direct current $I_C$ and the resonant current $i_1$ flows through the shunt capacitance. Because $i_1$ is a sinusoidal current, the pulse-type shape voltage appears across the drain-to-source of MOSFET as shown in Fig. 2. Namely,

$$v_S = \frac{1}{\omega C_S} \int_{2\pi(1-D)}^{\theta} (I_C - i') d\theta', \text{ for } 2\pi(1 - D) \leq \theta < 2\pi$$

Fig. 2. Nominal waveforms of the class-E amplifier.

The most important operation of the class-E amplifier is to satisfy the class-E ZVS/ZDS conditions at the MOSFET turn on instant, which are expressed as

$$v_S(2\pi) = 0$$

$$\left. \frac{v_S(\theta)}{d\theta} \right|_{\theta=2\pi} = 0,$$

where D is the switch on-duty ratio, $\theta = \omega t = 2\pi ft$ is the angular time, and $f$ is the operating frequency. By satisfying the ZVS condition, no switching loss occurs ideally. On the other hand, the ZDS condition means that the current flowing through the MOSFET rises from zero continuously at switch turn-on instants as shown in Fig. 2. By adding the ZDS condition to the ZVS condition, both the switch voltage and current are zero at turn-on instant. As a result, the switching losses can be suppressed even if there are component tolerances, which is the reason why the class-E amplifier achieves high power-conversion efficiency at high frequencies.

### 2.2 Basic concept of the class-E driver

Figure 3 shows an equivalent model of the MOSFET, which is used in this paper. The equivalent circuit between gate and source terminals is expressed by the gate capacitance $C_g$ and the gate resistance $R_g$, which are connected in series as shown in Fig. 3 [8, 10, 14–16]. The gate capacitance includes the effects of the gate-to-source and gate-to-drain capacitances. The MOSFET is in the on-state when the gate voltage is higher than the threshold voltage. Additionally, the drain-to-source capacitance is also considered. The nonlinearities of the MOSFET parasitic capacitances [22] are, however, ignored for simplicity in this paper.
When $C_1$ and $R$ of the class-E amplifier in Fig. 1 are replaced into the gate capacitance and the gate resistance of the SiC MOSFET, the class E amplifier becomes a resonant gate driver of the SiC MOSFET \[10\]. The driver achieves the soft switching by satisfying the class-E ZVS/ZDS conditions. In this paper, the MOSFET in the gate driver and the SiC MOSFET driven by the gate driver are called “driver-MOSFET” and “main-MOSFET”, respectively.

Because the resonant current is sinusoidal waveform, the voltage across the gate-to-source of the main MOSFET is also sinusoidal waveform. Generally, SiC MOSFETs have larger gate capacitance and higher gate resistance than Si and GaN devices. Therefore, the square-waveform driver suffers from the driving-voltage distortion at high frequencies, in particular. The mitigation of the drive-voltage distortion is an advantage of the sinusoidal-voltage driver compared with the square-waveform one. Additionally, the class-E driver has also an advantage against thermal problem compared with the hard-switching driver because of the class-E ZVS/ZDS at the driver MOSFET.

By the way, it is generally considered that the main SiC circuit handles much larger power than the driver circuit. Namely, the SiC driver circuit has a risk of the destruction by the inrush current from the main circuit. The safety measure is required to the gate driver for SiC MOSFET, in particular.

### 2.3 Proposed gate driver

Figure 4 shows a circuit topology of the proposed SiC gate driver. In the proposed driver, the isolation transformer is newly added to the class-E amplifier. The transformer is modeled by the primary and secondary inductances, $L_1$ and $L_2$, with the coupling coefficient $k$. The coupling coefficient is defined as

$$k = \frac{M}{\sqrt{L_1 L_2}},$$

where $M$ is the mutual inductance of the transformer. By adding the isolation transformer, it is possible to protect the class-E driver from the inrush current from the main SiC circuit. By implementing low-coupling-coefficient transformer intentionally, the leakage magnetic flux can be used as a resonant

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Fig. 3. Model of MOSFET.

Fig. 4. Circuit topology of the proposed gate driver.
inductance at the primary part.

At the secondary part, there is the impedance matching reactance $X_S$. By resonating $L_2 - X_S - C_g$ with the driving frequency, the secondary current becomes sinusoidal wave. As a result, the driving voltage, which is the voltages across the $C_g$ and $R_g$, is also sinusoidal.

Figure 5 shows example waveforms of the proposed gate driver. The advantage of the class-E driver can be inherited by the proposed driver. By satisfying the class-E ZVS/ZDS conditions, low power consumption can be achieved at high frequencies. Therefore, the thermal problem can be suppressed in the proposed driver compared with the hard-switching driver. Additionally, the driving voltage distortion is reduced because the gate capacitance and the gate resistance are included in the resonant filter of the secondary circuit.

![Fig. 5. Waveforms of the proposed driver. (a) At primary side. (b) At secondary side.](image)

3. Analysis of proposed driver

This section derives analytical expressions of the proposed driver. It is necessary to determine the component values for achieving the required amplitude of the gate voltage. Additionally, the class-E ZVS/ZDS conditions are satisfied for the soft-switching operation. It is, however, not easy to fix the component values for satisfying three conditions simultaneously, applying trial-and-error procedure. The steady-state analytical expressions of waveforms, which are the functions of the component values, are helpful for determining the component values.

Figure 6 shows circuit transformations for the analysis in this paper. The strategies of the analysis are: 1. the secondary part is expressed by the equivalent inductance and resistance with keeping the driving voltage information, 2. the proposed driver is transformed into the basic class-E amplifier topology by using the equivalent inductance and resistance of the secondary part, and 3. the component values for satisfying the class-E ZVS/ZDS conditions are expressed.

3.1 Analysis assumptions

The analysis in this paper is based on the following assumptions.

1. The driver MOSFET works as an ideal switch. Therefore, switching time is zero, off-resistance is infinite, and on-resistance is zero.

2. The passive components work ideally. No winding capacitance of the transformer is considered.

3. The dc-feed inductance is large enough to flow the direct current.
4. The driver MOSFET turns on at $\theta = 0$ and off at $\theta = 2\pi(1 - D)$, where $D$ is the on-duty ratio of a driver MOSFET.

5. The currents flowing through the primary and secondary resonant filters are pure sinusoidal waveforms.

From the above assumptions, the equivalent circuit can be illustrated as shown in Fig. 6(a).

![Equivalent Circuit Diagram](image)

**Fig. 6.** Analytical transformations of the proposed gate driver. (a) Equivalent circuit. (b) Equivalent circuit of the primary part. (c) Equivalent circuit of the secondary part. (d) and (e) Equivalent circuits resulting in the basic topology of the class-E amplifier.

### 3.2 Analytical expressions of the proposed driver

From the assumption 5, the current flowing through the secondary inductance is

$$i_2 = I_2 \sin(\theta + \phi_2),$$

(4)

where $I_2$ and $\phi_2$ are the amplitude and the phase shift of the secondary resonant current, respectively. The amplitude of the gate voltage $V_g$ should be less than the breakdown gate voltage of main MOSFET. By using $V_g$, the amplitude of the secondary current is expressed as

$$I_2 = \frac{V_g}{\sqrt{R_g^2 + \left(\frac{1}{\omega C_g}\right)^2}}.$$  

(5)

In this paper, the secondary resonant frequency is tuned to be the same as the operating frequency. This is because the secondary current needs to be sinusoidal. Therefore, we have
\[ \omega \frac{1}{C_g} - \omega L_2. \]  

From \( L_2, X_S, C_g, \) and \( R_g, \) the impedance of the secondary part \( Z_2, \) which is defined in Fig. 6(c), is expressed as

\[ Z_2 = R_g + j \left( \omega L_2 + X_S - \frac{1}{\omega C_g} \right) = R_g. \]  

From (7), the amplitude of induced voltage from the primary part is

\[ V_{ind} = |Z_2|I_2 = R_g I_2. \]  

The rectangular box part in Fig. 6(b) shows a model of the transformer used in this analysis. The transformer model uses the impedance of \( X_S - C_g - R_g \) network as shown in Fig. 6(c), which is expressed as

\[ Z_{sec} = R_g + j \left( X_S - \frac{1}{\omega C_g} \right). \]  

From (9), the impedance of \( Z_{eq}, \) which is indicated in Fig. 6(b), is expressed as

\[ Z_{eq} = \frac{\omega^2 k^2 L_1 L_2 R_g}{R_g^2 + (\omega L_2 + X_S - \frac{1}{\omega C_g})^2} + j \omega \left[ \frac{k^2 L_1 \left\{ R_g^2 + \omega L_2 X_S - (-X_S)^2 \right\}}{R^2 + (\omega L_2 + X_S - \frac{1}{\omega C_g})^2} + L_1 (1 - k^2) \right]. \]  

Substituting (6) into (10), we have

\[ Z_{eq} = \frac{(\omega k N L_1)^2}{R_g} + j \omega L_1, \]  

where \( N = \sqrt{L_2/L_1} \) is the turn ratio of the secondary coil to the primary one. Therefore, the equivalent resistance \( R_{eq} \) and inductance \( L_{eq}, \) which are described in Fig. 6(d), are expressed as

\[ R_{eq} = \frac{(\omega k N L_1)^2}{R_g}, \]  

and

\[ L_{eq} = L_1, \]  

respectively.

From the above analytical expressions, the equivalent circuit of the proposed driver is modeled as shown in Fig. 6(d), which is the same topology of the basic class-E amplifier as shown in Fig. 1(a).

According to the assumption 5, the primary current can be expressed as

\[ i_1 = I_1 \sin(\theta + \phi_1), \]  

where \( I_1 \) and \( \phi_1 \) are the amplitude and phase shift of the primary current, respectively. From (8) and (12), the amplitude of the primary current is

\[ I_1 = \frac{V_{ind}}{\omega k N L_1} = \frac{V_{ind}}{\sqrt{R_{eq} R_g}} = \sqrt{\frac{R_g}{R_{eq}}} I_2. \]  

Additionally, the phase shift of the primary current is determined uniquely for satisfying the class-E ZVS/ZDS conditions [19], which can be obtained from

\[ \phi_1 = \pi + \tan^{-1} \frac{\cos(2\pi D) - 1}{2\pi(1 - D) + \sin(2\pi D)}. \]  

For achieving the class-E ZVS/ZDS conditions, the resonant filter \( L_1 - C_1 \) should be inductive. Therefore, \( L_1 \) can be divided into \( L_0 \) and \( L_x \) as shown in Fig. 6(e), where \( L_0 \) and \( C_1 \) realize an ideal resonant filter tuned to the operating frequency. Namely, we have
\[ C_1 = \frac{1}{\omega^2 L_0} = \frac{1}{\omega^2 (L_1 - L_x)} = \frac{1}{\omega^2 (L_{eq} - L_x)}. \]  

(17)

Additionally, \( L_x \) is used for adjusting the phase shift of the primary current. For achieving the class-E ZVS/ZDS conditions, \( L_x \) is fixed uniquely [19] as

\[ L_x = R_{eq} \frac{2(1-D)^2 \pi^2 - 1 + 2 \cos \phi_1 \cos(2\pi D + \phi_1) - \cos 2(\pi D + \phi_1) |\cos(2\pi D) - \pi(1-D) \sin(2\pi D)|}{4\omega \sin(\pi D) \cos(\pi D + \phi_1) \sin(\pi D + \phi_1) [(1-D) \pi \cos(\pi D) + \sin(\pi D)]}. \]  

(18)

From the class-E amplifier design viewpoint, the amplitude of the output current can be regulated by the dc-supply voltage and the duty ratio. The relationships among dc-supply voltage, equivalent resistance, and duty ratio are expressed as

\[ V_{DD} = -\frac{\pi(1-D)}{2 \sin(\pi D) \sin(\pi D + \phi_1)} R_{eq} I_1 = -\frac{\pi(1-D)}{2 \sin(\pi D) \sin(\pi D + \phi_1)} \sqrt{\frac{R_{eq}}{R_g} V_{ind}}. \]  

(19)

The shunt capacitance for satisfying the class-E ZVS/ZDS conditions should also satisfy

\[ C_S = \frac{2 \sin(\pi D) \cos(\pi D + \phi_1) \sin(\pi D + \phi_1) [(1-D) \pi \cos(\pi D) + \sin(\pi D)]}{\omega \pi^2 (1-D) R_{eq}}. \]  

(20)

From the assumption 3, the dc-feed inductance should be sufficient large because it is assumed that the input current is direct one. The dc-feed inductance need to satisfy

\[ L_C > \frac{R_{eq}}{f} \left( \frac{2 \pi^2}{4} + 1 \right), \]  

(21)

for ensuring less than 10% current ripple of the input current [19].

### 3.3 Duty ratio of main-MOSFET

Because the gate input voltage of the main-MOSFET is sinusoidal, the relationship between the SiC gate threshold voltage \( V_{th} \) and gate voltage \( V_g \) is expressed using the duty ratio \( D_m \) as

\[ \frac{V_{th}}{V_g} = \sin \frac{\pi - 2\pi D_m}{2}. \]  

(22)

Therefore, the duty ratio of the main-MOSFET can be adjusted in the range of

\[ 0 < D_m < \frac{\pi - 2 \sin^{-1} \left( \frac{V_{th}}{V_{gb}} \right)}{2\pi}, \]  

(23)

by having the amplitude of the gate voltage \( V_g \), where \( V_{gb} \) is the breakdown gate voltage of the main-MOSFET.

### 4. Design example

In this paper, 7 MHz gate driver for C3M0280090D SiC MOSFETs from Wolfspeed is designed. Table I gives characteristics of the C3M0280090D SiC MOSFET, where values of \( C_g \), \( R_g \), and \( C_{ds} \) were measured by the Keysight E4990A impedance analyzer and the threshold and breakdown gate

|               | SiC-1 | SiC-2 | SiC-3 |
|---------------|-------|-------|-------|
| Gate capacitance \( C_g \)    | 327 pF | 335 pF | 324 pF |
| Gate resistance \( R_g \)      | 26.0 Ω | 26.3 Ω | 26.8 Ω |
| Drain-to-source capacitance \( C_{ds} \) | 150 pF | 143 pF | 151 pF |
| Threshold voltage \( V_{th} \) | 2.1 V  | 2.1 V  | 2.1 V  |
| Breakdown gate voltage \( V_{gb} \) | 19 V   | 19 V   | 19 V   |

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voltages are obtained from datasheet. In this paper, three SiC devices, which are SiC-1, -2 and -3 were prepared for evaluating the parasitic component tolerances effects. For the driver design, values of $C_g$ and $R_g$ of SiC-1 were used.

Figure 7 shows circuit topologies of the main circuits. In this paper, two types of SiC main circuits are operated with the proposed gate driver. One is the simple driving-test circuit [1], which is composed of dc-voltage source, resistance, and SiC MOSFET as shown in Fig. 7(a). The other is the SiC class-E amplifier as shown in Fig. 7(b). The proposed driver can be applied only at specified frequency with fixed duty ratio and the fixed type of the main-MOSFET, which are the restrictions of the proposed driver. The class-E amplifier is one of good examples, which operates at the fixed frequency and duty ratio.

![Fig. 7. Circuit topology of main circuits. (a) Driving-test circuit. (b) Class-E main amplifier.](image)

4.1 Driver-circuit design
For the driver designs, the following specifications are given: operating frequency $f = 7$ MHz, gate resistance $R_g = 26.0 \, \Omega$, gate capacitance $C_g = 327 \, \text{pF}$, and amplitude of the driving voltage across the SiC gate terminal $V_g = 15 \, \text{V}$. Additionally, the switch on-duty ratio $D = 0.5$ is also given. The turn ratio of the primary and secondary inductances and the coupling coefficient of the transformer are fixed as $N = 1$ and $k = 0.2$, respectively. Mica capacitances were used in the experiments. The capacitance values were adjusted in detail by connecting multiple capacitances in parallel.

4.2 Step-by-step design procedure of the proposed driver
From (5) and the design specifications, the amplitude of the secondary current should be
\[
I_2 = \sqrt{\frac{V_g}{R_g^2 + (\omega C_g)^2}} = 0.204 \, \text{A.} \tag{24}
\]
From (8), the amplitude of the voltage across the secondary inductance is
\[
V_{ind} = R_g I_2 = 5.30 \, \text{V.} \tag{25}
\]
It is seen from (15) that large amplitude current follows through the primary inductance when the secondary inductance $L_2(= N^2 L_1)$ is low. For avoiding much current through the primary inductance, it is set that the amplitude of the primary current is the same as that of the secondary one. Therefore, we have
\[
I_1 = I_2 = 0.204 \, \text{A.} \tag{26}
\]
From (15) and (26), the secondary inductance is
\[
L_2 = \frac{V_{ind}}{\omega k I_1} = 2.96 \, \mu\text{H}. \tag{27}
\]
Because the secondary resonant filter needs to be tuned to the operating frequency, the adjusting reactance is

\[ X_S = \frac{1}{\omega C_g} - \omega L_2 = -61.1 \, \Omega. \tag{28} \]

It is seen from the condition of \( X_S < 0 \) that the adjusting reactance is capacitance, which can be obtained from

\[ C_2 = -\frac{1}{2\pi f X_S} = 372 \, \text{pF}. \tag{29} \]

From \( N = 1 \) and (27), the primary inductance is

\[ L_1 = NL_2 = 2.96 \, \mu H. \tag{30} \]

From (15) and (26), the equivalent resistance can be obtained as

\[ R_{eq} = R_g \left( \frac{I_2}{I_1} \right)^2 = 26.0 \, \Omega. \tag{31} \]

From (16), phase shift of the output current is

\[ \phi = \pi + \tan^{-1} \frac{\cos(2\pi D) - 1}{2\pi(1 - D) + \sin(2\pi D)} = 2.57 \, \text{rad}. \tag{32} \]

Therefore, the dc-supply voltage is obtained from (19) as

\[ V_{DD} = -\frac{\pi(1 - D)}{2\sin(\pi D)\sin(\pi D + \phi_1)} R_{eq} I_1 = 4.931 \, \text{V}. \tag{33} \]

From (18), \( L_x \) is

\[ L_x = R_{eq} \frac{2(1 - D)^2\pi^2 - 1 + 2 \cos \phi_1 \cos(2\pi D + \phi_1) - \cos 2(\pi D + \phi_1)[\cos(2\pi D) - \pi(1 - D)\sin(2\pi D)]}{4\omega \sin(\pi D)\cos(\pi D + \phi_1)\sin(\pi D + \phi_1)[(1 - D)\pi\cos(\pi D) + \sin(\pi D)]} \]

\[ = 0.681 \, \mu H. \tag{34} \]

From \( L_1 \) and \( L_x \), we have

\[ C_1 = \frac{1}{\omega^2 L_0} = \frac{1}{\omega^2 L_1 - L_x} = 227 \, \text{pF}. \tag{35} \]

From (20), the shunt capacitance of the driver MOSFET can be obtained as

\[ C_S = \frac{2\sin(\pi D)\cos(\pi D + \phi)\sin(\pi D + \phi)[(1 - D)\pi\cos(\pi D) + \sin(\pi D)]}{\omega^2(1 - D)R_{eq}} = 160 \, \text{pF}. \tag{36} \]

Finally, the dc-feed inductance for providing the direct input current with less than 10 % ripple ratio needs to be in the range of

\[ L_C > R_{eq} \left( \frac{2\pi^2}{4} + 1 \right) = 25.8 \, \mu H. \tag{37} \]

The SiC MOSFET was driven by the sinusoidal driving voltage, whose amplitude is \( V_g = 15 \, \text{V} \). Because the threshold voltage of the SiC MOSFET is \( V_{th} = 2.1 \, \text{V} \), the switch on-duty ratio of the main amplifier is specified as

\[ D_m = \frac{\pi - 2\sin^{-1} \left( \frac{V_{th}}{V_g} \right)}{2\pi} = 0.455. \tag{38} \]
Table II. Analytical and measurement values of the proposed gate driver.

|                  | Analytical | Measured | Difference |
|------------------|------------|----------|------------|
| $f$              | 7.0 MHz    | 7.0 MHz  | 0.0 %      |
| $D_1$            | 0.5        | 0.5      | 0.0 %      |
| $V_{DD}$         | 4.93       | 4.95     | 0.40 %     |
| $L_1$            | 2.96 µH    | 3.01 µH  | 1.69 %     |
| $L_2$            | 2.96 µH    | 2.99 µH  | 1.01 %     |
| $L_C$            | 25.8 µH    | 130 µH   | -          |
| $k$              | 0.2        | 0.2      | 0.0 %      |
| $C_1$            | 227 pF     | 227 pF( = 198 pF + 29 pF) | 0.0 %      |
| $C_2$            | 372 pF     | 374 pF( = 324 pF + 50 pF) | 0.53 %     |
| $C_S$            | 160 pF     | 155 pF( = 103 pF + 22 pF + 30 pF) | −3.12 %   |
| $C_g$            | 327 pF     | 327 pF   | 0.0 %      |
| $R_g$            | 26.0 Ω     | 26.0 Ω   | 0.0 %      |
| Power consumption | -          | 4.95 W   | -          |

5. Experimental verifications

5.1 Driver-circuit implementation

The SUD06N10 Si MOSFET from Vishay was selected as the switching device of the driver, whose breakdown drain-to-source voltage is 100 V. The drain-to-source parasitic capacitance of the Si MOSFET is 30 pF. Therefore, 125 pF of additional capacitance was added to the drain-to-source of the driver-MOSFET in parallel. The driver MOSFET was driven by Intersil EL7104CNZ gate driver. Mica condensers were adopted for both resonant and shunt capacitances. In the actual implementations, multiple capacitances are connected in parallel for fine adjustments. Table II gives the analytical and measurement component values of the proposed driver. All the component values were measured by Keysight E4990A impedance analyzer. The dc-feed inductance and transformer were implemented by using the TDK PC47EI30-Z EI core and the Micrometals T-68-2 toroidal core, respectively, with single-strand winding. The winding capacitance is 2.70 pF. It could be confirmed that self-resonant frequency of the primary and secondary coils are 65 MHz both, which are much higher than the operating frequency. From above measurements, the validity of the assumption 2 was confirmed.

5.2 Driving-test circuit

The driving-test circuit works with operating frequency $f = 7$ MHz, input voltage $V_{Im} = 100$ V, and load resistance $R_{Lm} = 50 \, \Omega$. The dummy load from Bird was used for the load resistance. In the test circuit, the drain-to-source voltage of the main-MOSFET is zero when the main-MOSFET is in the on state. On the other hand, when the main-MOSFET is in the off state, the switch voltage is as the same as the $V_{Im}$. Figure 8 shows the experimental waveforms of the driving-test circuit with SiC-1 and the proposed gate driver. The experimental waveforms were measured by Keysight DSO-X-2004A oscilloscope. It is seen from Fig. 8(b) that the SiC MOSFET was driven with 7 MHz frequency by applying the proposed gate driver. Additionally, it is also confirmed that the proposed driver achieved the class-E ZVS/ZDS conditions. The achievement of the class-E ZVS/ZDS conditions denotes the validity of the gate-terminal modeling, namely series connection of the capacitance and the resistance, of the main-MOSFET. It is seen from Figs. 8(a) and (b) that the experimental waveforms agreed with the theoretical ones quantitatively. The above results showed the validities of the analytical expressions.

5.3 7 MHz SiC class-E amplifier

As the second example, the SiC class-E amplifier was designed and implemented as the main circuit. The specifications of the SiC class-E amplifier are operating frequency $f = 7$ MHz, loaded quality factor $Q_m = 3$, load resistance $R_m = 25\, \Omega$, and switch on-duty ratio $D_m = 0.455$. From these specifi-
Waveforms of 7 MHz SiC driving-test circuit and the proposed gate driver. (a) Theoretical waveforms. (b) Experimental waveforms.

Table III. Analytical and measurement values of the 7 MHz SiC class-E amplifier.

|       | Analytical | Measured | Difference |
|-------|------------|----------|------------|
| $f$   | 7.0 MHz    | 7.0 MHz  | 0.0 %      |
| $D_m$ | 0.455      | –        | –          |
| $V_{Dm}$ | 100 V     | 100 V    | 0.0 %      |
| $L_{1m}$ | 1.71 $\mu$H | 1.70 $\mu$H | -0.58 %   |
| $L_{Cm}$ | 68.2 $\mu$H | 570 $\mu$H | -          |
| $C_{1m}$ | 857 pF     | 856 pF(=514 pF+303 pF+39 pF) | -0.11 %  |
| $C_{Sm}$ | 220 pF     | 220 pF(=50 pF+20 pF+150 pF)  | 0.0 %     |
| $R_m$  | 25 $\Omega$ | 25.1 $\Omega$ | 0.40 %   |
| $V_{om}$ | 78.3 V    | 75.3 V   | -3.93 %    |

cations, component values for achieving the class-E ZVS/ZDS conditions were determined uniquely by following design procedure in [19]. Table III gives the component values of the SiC class-E amplifier. In the SiC class-E amplifier, 20 pF and 50 pF of external capacitances were added to the drain-to-source of the main SiC MOSFET in parallel. This is because drain-to-source parasitic capacitance of the SiC MOSFET was 150 pF. The dc-feed and resonant inductances were implemented with the TDK PC47El60-Z EI core and the Micrometals T-200-2 toroidal core, respectively. Dummy load from Bird was used as the load resistance. Figure 9 shows the experimental setup for the 7 MHz SiC class-E amplifier operations.

Figure 10 shows waveforms of the proposed driver and the SiC class-E amplifier with SiC-1. The SiC MOSFET was driven by the proposed gate driver. It is seen from Fig. 10(b) that the driver-MOSFET voltage $v_S$ achieved the class-E ZVS/ZDS conditions. It is also seen from Fig. 10(b) that the experimental main-MOSFET voltage $v_{Sm}$ also achieved the class-E ZVS/ZDS conditions. It can be stated that the class-E amplifier with SiC MOSFET could be realized with 7 MHz and 109 W output. The input power of the proposed driver was 4.95 W and no heatsink was necessary at the driver. It is seen from Figs. 10(a) and (b) that the experimental waveforms agreed with the theoretical predictions quantitatively, which showed the validities of the analytical expressions including the modeling of the SiC MOSFET as shown in Fig. 3.
For evaluating the effects of parasitic-component tolerances to the proposed driver, the SiC MOSFET was changed to the other one, which is called SiC-2 and SiC-3, those characteristics are given in Table I. Figure 11 shows waveforms of the 7 MHz class-E SiC amplifier for the fixed SiC MOSFET. It can be confirmed from Fig. 11 that there are little differences among waveforms with fixed SiC MOSFETs. All the driver- and main-MOSFET voltages satisfied the soft-switching condition, which showed the strength against the component tolerances of the class-E amplifier. It can be stated from this result that the proposed driver absorbs the effects of main-MOSFET parasitic component tolerances by applying the class-E ZVS/ZDS conditions and realizes stable operations.
6. Conclusion

This paper has proposed the high-frequency resonant gate driver, which is based on the class-E amplifier with isolation transformer, for driving SiC MOSFETs. Additionally, the analytical expressions and the step-by-step design procedures of the proposed driver are presented. The experimental results showed the usefulness of the proposed driver for high-frequency drive, in particular. The validities of the analytical expressions and the design procedure were confirmed by the quantitative agreements among theory and experimental results.

There are cases that the effects of parasitic inductance and capacitance of PCB need to be considered. It is necessary to derive analytical expressions including these effects, which is an important problem we should address in the future.

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