Non-destructive peak junction temperature measurement of double-chip IGBT modules with temperature inhomogeneity

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ABSTRACT: Considering the problem of measuring the peak junction temperature of a double-chip module with temperature inhomogeneity, we use a double-chip parallel model to analyze peak junction temperature measurement error for the traditional electrical method. An improved test method is proposed that is based on the small current–voltage drop method—specifically the dual current test method employing an extended-dimension calibration curve library. This method realizes a match of the calibration current with the test current by expanding the dimension database, eliminates errors of temperature measurements, and finally obtains the peak junction temperature of the module. The measurement result is close to the set temperature of the model, thereby verifying its accuracy.

1. Introduction

With different heat dissipation conditions in multi-chip insulated-gate bipolar transistor (IGBT) modules, thermal power consumption during operations creates inhomogeneities in the temperature distribution of each chip. The reliability of the chip with the highest junction temperature determines the upper limit for the module [1]. The measurement of this peak junction temperature for an IGBT module is particularly important.

Among existing methods for the measurement of the junction temperature, the infrared thermal imaging method [2] provides the means to obtain the temperature distribution of the module, and hence the peak junction temperature inside the module; the drawback is that the packaging structure of the module is destroyed. By measuring changes in electrical parameters such as current and voltage drops, traditional electrical methods [3] can extract the junction temperature of the device speedily without destroying the device package. However, with nonuniform temperatures in the chip, large errors accrue between the measured junction temperature and the peak junction temperature. The measured junction temperature is the average temperature value weighted by the internal current of the device [4], and the measurement result is affected by the magnitude of the test current. In 1999, Miao Qinghai and colleagues studied the inhomogeneity of the temperature in bipolar transistors and discovered a small current overheating effect [5]. Taking this into account, a thermal spectroscopy method was proposed in 2005 to obtain the temperature distribution within transistors and to measure the peak junction temperature of transistors [6]; In 2013, Qiu Zhijie and colleagues reported fitting the IGBT current [7] based on results obtained by varying the test conditions. The voltage–temperature relationship was used to estimate the peak temperature of the junction of a IGBT module. In 2020, Wang Sijin and colleagues [8] used the relationship between the changes in current and temperature for an IGBT under different gate voltages to measure the changes in current of the dual-chip IGBT module applying high and low...
gate voltages to obtain the average temperature together with the highest and lowest temperatures.

In view of the problems mentioned regarding the chip parallel module, this paper analyzes the measurement error for the traditional electrical method using the IGBT double-chip parallel model. A dual-current electrical measurement method is proposed for which the dimension calibration curve library is extended so as to measure the peak junction temperature of the double-chip IGBT module. By expanding the dimension database, the calibration current is matched to the test current, thereby eliminating temperature measurement errors and ultimately yielding a more accurate reading of the peak junction temperature of the module.

2. measurement error analysis of the traditional electrical method

2.1 Double-chip parallel model

Because the packaged module cannot monitor and change the internal parallel chip parameters, many difficulties are present in experiments and therefore the module is not suitable for basic research regarding temperature measurement methods. To study measurement errors associated with the traditional electrical method and stemming from the temperature differences between parallel chips, we devised a parallel test model (Figure 1) that screens each discrete IGBT (model IKW30N60H3, TO-247 package) for the same parameter characteristics. A method employing small static current–voltage drops was mainly used (Figure 2). Although there are many parasitic parameters associated with the power module package compared with a parallel-connected discrete device, such parameters have little influence on static parameters during measurements. In this model, in addition to regulating the temperature, electrical parameters of parallel chips were monitored.

![Figure 1. Schematic diagram of double-chip parallel model](image1)

![Figure 2. Photograph of the setup](image2)

2.2 Analysis of measurement error of small current pressure drop method

Using our two-chip parallel model together with the small current–voltage drop method, the junction temperature was measured against current in the range 0–100 mA for various temperature distributions (Figures 3 and 4; note the change in temperature range). The test results show that when the temperature is not uniform, the junction temperature and the peak junction temperature measured by this method exhibit discrepancies. As the temperature difference and the test current increase, the difference between the measured junction temperature and the peak junction temperature increases.
By testing the branches of the parallel model chip, the values of the current on the high-temperature chip were obtained for different temperature distributions and fixed current tests as seen in Table 1. We observed that because the temperature is uniform, the current is evenly distributed among the parallel chips. With uneven temperatures, the high-temperature tube current gradually increases with increasing temperature difference. Therefore, during testing, although the external test current is always the same, the test current in the actual internal high-temperature chip is not fixed and varies with the nonuniformity of the internal temperature. This violates the traditional assumptions underlying the application of the small current–voltage drop method.

### Table 1: Current values for the high-temperature chip under different temperature differences

| Main circuit current (mA) | TH=40°C (40°C-40°C) | TH=50°C (40°C-50°C) | TH=60°C (40°C-60°C) | TH=70°C (40°C-70°C) | TH=80°C (40°C-80°C) |
|--------------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| 10                       | 5.02                | 6.21                | 7.14                | 7.88                | 8.39                |
| 20                       | 10.03               | 12.11               | 13.87               | 15.40               | 16.65               |
| 30                       | 15.06               | 17.72               | 20.03               | 22.19               | 24.07               |
| 40                       | 20.01               | 23.15               | 25.90               | 28.51               | 30.90               |
| 50                       | 25.03               | 28.51               | 31.59               | 34.57               | 37.36               |

When establishing a dual-chip parallel temperature calibration curve library used in the traditional small current–voltage drop method, the relationship between the internal single tube voltage and temperature and current at a certain fixed test current I and for a certain peak temperature T is

\[ V = f(I, T) \]  

(1)

In actual measurements of parallel-connected modules with a certain temperature inhomogeneity, the current and voltage of the single tube, the internal high temperature of which is T, is

\[ V = f(I_{th}, T), \quad \frac{I}{2} \leq I_{th} \leq I \]  

(2)

Because the temperature correction current of the temperature correction curve and the actual test current are different, there is a discrepancy between the junction temperature measured by the traditional method and the actual peak junction temperature.

### 3. extended-dimension double current electrical measurement method

#### 3.1 Improving the small current–voltage drop method

From the above experimental analysis, we see a difference between the temperature calibration current
when the temperature calibration curve library is established and the actual measured current, which leads to a discrepancy between the temperature measurement and the actual peak junction temperature. The peak junction temperature for parallel chips can be measured if the test current is the same as the calibration current in the actual test or if a new calibration curve library is established using the actual test current as the calibration current. As an example, we set the current at 10 mA and obtained the test results (see Table 2).

Table 2: Measurement results of peak junction temperature with a temperature difference between 40°C and 80°C under different test conditions

| Parallel chip temperature: 40°C-80°C | Temperature measurement mode | The calibration current matches the test current | The test current matches the calibration current |
|------------------------------------|-----------------------------|-----------------------------------------------|-----------------------------------------------|
|                                    |                             | I(test) 10mA | I(test) 5.95mA | I(test) 8.39mA | I(test) 5mA |
|                                    |                             | I(calibration) 16.78mA | IH (calibration) 10mA | I(calibration) 10mA | IH (calibration) 5mA |
|                                    |                             | I_H(test) 8.39mA | I_H (calibration) 5mA |
| Peak junction temperature results  |                             | 79.6°C | 79.8°C |

I(test)–parallel model trunk test current, I(calibration)–parallel model trunk temperature calibration current, I_H(test)–parallel model high-temperature branch test current, I_H(calibration)–parallel model high-temperature branch temperature calibration current

The experimental results show that when the test current is consistent with the calibration curve current, the junction temperature of the high temperature chip can be measured using the small current–voltage drop method. However, in actual measurements, because the temperature of the parallel chips in the module is not uniform, the temperature of each chip and the shunt current of each branch is unknown. Ensuring that the current on the high-temperature chip is consistent with the temperature calibration current is difficult by changing the main circuit test current. However, the calibration current can be matched with the test current by expanding the dimension database to eliminate temperature measurement errors. With this match, the peak junction temperature of the module can finally be obtained. A comparison between the two methods—traditional small current–voltage drop and the extended-dimension dual current method—is given in Figure 5.

Figure 5. Comparison of the traditional electrical method and the extended dual current method

3.2 Establishment of extended-dimension calibration curve cluster

For the dual current test method, we need first to establish for any test current a library of temperature calibration curves covering temperature calibrations over a reasonable current interval. Taking the aforementioned IGBT device as a test device combined with the parallel model, and setting the test current to 10 mA as an example, we next describe briefly how to establish the extended-dimension calibration curve library.

We first fix the heating platform temperature (30 °C–90 °C, temperature step 5 °C) and $V_{GS} = 15$ V for various temperatures. Next, using a B1505A tester, we find the relationship between voltage $V_{CE}$ and
current in the range 0–20 mA, and build a three-dimensional I–V–T database (Figure 6).

![Figure 6. I–V–T three-dimensional substrate data for test currents 0–20 mA.](image)

![Figure 7. Extended dimension V–T–P calibration curve cluster](image)

Depending on the formula, the temperature correction current is converted into a corresponding current ratio

\[ P = \frac{I_A}{I_B} N \]  

(3)

where \( P \) denotes the current ratio, \( I_A \) the 0–20-mA calibration curve current, \( I_B \) the 10-mA test current, and \( N \) the number of parallel devices.

Combined with the actual analysis, in the dual-chip parallel model, the current for the high-temperature chip is higher than that for the low-temperature chip. With increasing temperature difference, the current of the high-temperature tube gradually increases, so the actual current ratio is 50%–100%. Using the database based on the traditional V–T calibration curve, an expanded V–T–P calibration curve cluster including the current ratio is obtained.

Figure 7 illustrates a cluster of voltage vs. temperature curves with current ratios in the range 50%–100%. The top inset shows an enlargement of the curves encircled in red whereas the bottom inset is an enlargement of the temperature calibration curve with current ratio 50% encircled in blue. The latter is also the temperature calibration curve with a test current of 10 mA obtained by the traditional method.

4. results and discussion

Taking temperature differences of 40°C–80°C as an example, we measured the conduction voltage drop for test currents of 10 mA and 20 mA. From the measured voltage and the corresponding cluster of temperature calibration curves, the current ratio and the curve for the change in junction temperature for the two test currents were then obtained (Figure 8).

![Figure 8. Current ratio and curves for the change in junction temperature at test currents of 10 mA and 20 mA](image)
From the results in Figure 8, there is a large discrepancy in the junction temperature and the peak junction temperature measured by the traditional method. Moreover, the junction temperature obtained by the dual current test method is closer to the peak junction temperature. Combined with the analysis of the actual current value of the parallel double transistor measured in our previous content, the discrepancy between the junction temperature and the peak junction temperature arises because the current ratio of the high temperature transistor is not the same for the different test currents and gradually increases with decreasing value of the test current. However, when test currents are close, the current ratios are close. Therefore, if a reasonable test current is selected, the intersection of the measured results will be near the true value of the peak junction temperature.

5. conclusion
In summary, the non-uniformity of temperature in a parallel module leads to discrepancies between the current distribution in the actual test and that in the temperature calibration, and hence errors result in the traditional electrical measurement. An improved test method based on the small current–voltage drop method was proposed that essentially is a dual current test method employing an extended library of dimension calibration curves. We use the dual-chip parallel model to verify the measurement results of our method. Compared with traditional test results, the temperature measurement results are clearly better. Moreover, this method is not limited to peak temperature measurements of the junction of a dual chip module. In future research, peak junction temperature measurements on multi-chip parallel IGBT modules with more than three chips are envisaged.

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