Charge Density Based Small Signal Modeling for InSb/AlInSb Asymmetric Double Gate Silicon Substrate HEMT for High Frequency Applications

T. Venish Kumar 1 · M. Venkatesh 2 · B. Muthupandian 3 · G. Lakshmi Priya 4

Received: 14 August 2021 / Accepted: 10 September 2021 / Published online: 18 September 2021 © Springer Nature B.V. 2021

Abstract
This paper proposes the Asymmetric Double Gate Silicon Substrate HEMT (ADG-Si-HEMT) to study the carrier concentration and intrinsic small signal parameters of the InSb/AlInSb silicon wafer DG-HEMT device. The HEMTs work as a three-port system and the device is named Asymmetric Double Gate HEMT when the top and bottom gates are biased with different gate voltages. The position of quasi-Fermi energy levels (E_F) is used to investigate the modulation of back-channel charge density caused by the front gate voltage. Also, the small signal model is obtained for various parameters such as cut off frequency, gate to source capacitance and transconductance. To enhance device operation, the effects of the following factors are being investigated delta doping, drain current for various top and bottom gate voltages. The transconductance 2390 Sm/mm for V_fg = 0.2 V and cut off frequency around 197 GHz for V_bg = 0.3 are obtained. The analytical results are compared to the results of the Sentaurus 3-D TCAD simulation. Because of the variation in threshold voltage and modifying carrier density in dual channels, the asymmetric biasing approach has a wide range of mixed applications.

Keywords Indium Antimonide · TCAD · Double gate HEMT · Semiconductor · Capacitance

1 Introduction
In this article, InSb based asymmetric HEMTs are presented to enhance the performance of the HEMT. The Indium Antimonide (InSb) based High Electron Mobility Transistors (HEMTs) are the most suitable for high-speed applications due to their highest electron mobility (30,000 cm² V⁻¹S⁻¹) and high saturation velocity (5 × 10⁷ cm/s) than the other known compound semiconductors [1–3]. HEMTs are symmetric or asymmetric, depending on how the top and bottom gates are biased [4, 5].

As asymmetric DG-HEMT, the potential well is formed perpendicular to the interface between layers AlInSb and InSb because of their bandgap differences, and charged electrons are transferred from the doped (delta doping- δ) layer to the InSb layer [6]. The accumulation of transferred electrons in the narrow bandgap material (InSb) is referred to as a potential well or a two-dimensional electron gas (2DEG) [7]. The Coulomb scattering is reduced in the high electron mobility transistor because the electrons are separated from the donor atoms. The electrons are permitted to move in the vertical direction of an interface and the concentration of electrons depends on the gate bias and delta doping of the barrier layer [8–12].
The operation of Asymmetric Double Gate HEMT differs from the typical HEMTs. The bottom channel carrier concentration is fixed by the back gate voltage in the fabrication itself and variable voltage is applied to the top gate. Therefore, the top gate took control and modulates the electron’s accumulation in both channels. This system works like typical HEMTs but the single gate controls the dual channel and it provides double the amount of current density than the conventional HEMTs. The variable front gate bias provides better immunity against the second order effects, enhanced gate control over the channel and additional flexibility achieved in the threshold voltage by controlling the backchannel carrier concentration [13].

Therefore, a detailed analysis is necessary to understand the sheet charge density ($n_s \text{cm}^{-2}$) in the Asymmetric DG-HEMT device. There are several linear and nonlinear analytical models are proposed since the 1980s to calculate charge density in the channel. The linear approximation for Fermi-level ($E_F$) versus sheet charge density ($n_s$) was done by Drummond and the team [14]. Since 1988, various other research groups are expressed the non-linear approximation of $E_F$ versus $n_s$ but these approximations are appropriate only if devices are not operated in the subthreshold region [15]. Further, Dasgupta expresses the good nonlinear approximation but this expression is not suitable for a wider range of $n_s$ values [16].

Finally, the new expression for Fermi energy level versus sheet charge density is proposed by Jinrong and Fermi energy level ($E_F$) is calculated for three different values of $n_s$ [17, 18]. Based on this approximation the Asymmetric double gate HEMT sheet charge density ($n_s$) is calculated for three different regions of operation ($V_{fg} > V_{th1} + k_i V_{th1} < V_{fg} < V_{th1} + k_i$). Further, the front gate modulation on the backchannel is expressed using Gauss’s law. In general, this analysis leads to further analysis of the frequency performance and speed of carriers in the channel. Because the gate length and gate foot to channel distance are interrelated to the frequency performance of the device [19–21]. So, in the continuous analysis of charge density, the work extended to calculate the small-signal model to extract the Gate to Source Capacitance, Cut off Frequency and Transconductance are obtained of Asymmetric DG-HEMT.

### 2 Device Structure Description

Figure 1 shows the cross-sectional view of Asymmetric Double Gate HEMTs (DG-HEMTs). The wide bandgap material Aluminium Indium Antimonide (AlInSb) grown over a narrow bandgap material Indium Antimonide (InSb), therefore the 2-dimensional electron gas or quantum well is formed in narrow bandgap material, unlike the MOSFETs. In the Asymmetric DG-HEMT device, two quantum wells are formed on the back and forth of the InSb layer because the InSb is inserted between the two wide bandgap AlInSb materials and two identical gates are placed on the top ($V_{fg}$) and bottom ($V_{bg}$) of the device structure. The cap layer is used to reduce the conductance of Ohmic contacts, followed by AlInSb barrier layer width is $T_a$, AlInSb spacer width is $T_s$, delta doping AlInSb layer width is $T_d$ with doping concentration $N_D$ and the total width of AlInSb layer is $T = T_a + T_s + T_d$ on both sides of InSb layer thickness is $T_{ch}$. The device parameters are listed in Table 1. Silicon is employed as a substrate for the growth of InSb and AlInSb materials.

Figure 2 shows the energy band diagram of the Asymmetric DG-HEMT for three different circumstances. The solid line signifies the conduction of both top and bottom quantum well, the dotted line signifies the front channel is in the threshold region but the backchannel is conducting, the dashed line signifies the front channel is in the cut off regions but the backchannel is conducting with fixed back gate voltage $V_{bg}$. In this analytical model, the source and drain contacts are limited for channel region and do not consider for parallel conduction.

| S.No. | Layers                  | Doping | Dimensions (nm) |
|------|-------------------------|--------|-----------------|
| 1    | Cap layer               | $5 \times 10^{23} \text{cm}^{-3}$ | 10   |
| 2    | Doped AlInSb            | $2 \times 10^{23} \text{cm}^{-3}$ | 15   |
| 3    | Te δ –doping ($T_{d}$)  | $3 \times 10^{23} \text{cm}^{-3}$ | 3    |
| 4    | Silicon wafer AlInSb ($T_s$) | $1 \times 10^{19} \text{cm}^{-3}$ | 7    |
| 5    | Silicon wafer InSb ($T_{ch}$) | –       | 20   |
| 6    | Gate Length ($L$)       | –      | 80   |
3 Charge Density Model for Asymmetric Silicon Wafer DG-HEMT

### 3.1 Top and Bottom 2-Dimensional Electron Gas

The 2-dimensional electron gas/quantum well is formed at the boundary of two dissimilar compound semiconductors due to the variance in the electron affinity of the materials. The electron transfer across the interface can be written by equating the depletion of carriers from the barrier AlInSb Silicon layer to the accumulation of carriers in the quantum well InSb Silicon layer. The maximum quantity of carriers is depleted from the AlInSb barrier layer is given by using Lee theory \[22\],

\[
n_{si} = \frac{2\varepsilon_A N_{Di}}{q} (\Delta E_{ci} - E_{F1}) + N_{Di}^2 T_{si} - N_{Di} T_{si}
\]

(1)

where \(\varepsilon_A\) is the permittivity of the AlInSb barrier layer, \(\Delta E_{ci}\) is the conduction band discontinuity of top (i = 1) and bottom (i = 2) hetero-interface, \(E_{F1}\) quasi-Fermi energy level of top and bottom hetero-interface and q is the electron charge.

For large negative voltage is applied to the gates, the gate depletion and the heterointerface depletion will overlap, in this case, eq. (1) is replaced by the Poisson Equation for the solution of top and bottom interface and expressed by

\[
n_{si} = \frac{\varepsilon_A}{q T} (V_{GSi} - V_{offi} - E_{F1})
\]

(2)

where, \(V_{GSi}\) (i = 1 for top-gate bias \(V_{fg}\) and i = 2 for bottom gate bias \(V_{bg}\), \(V_{offi}\) is threshold voltage.

\[
V_{offi} = \phi_{bi} - \Delta E_{ci} - \frac{q N_{Di} T_{si}^2}{2\varepsilon_A}
\]

(3)

where \(\phi_{bi}\) barrier height of the top and bottom gate.

The model formulated using the relationship among the sheet charge density \(n_s\) and quasi-Fermi energy level \(E_F\) and the accurate model for Fermi level \(E_F\) versus carrier concentration \(n_s\) is expressed by Pu [23].

\[
E_F = K_1 + (K_2 n_i + K_3 n_i^2)^{\frac{1}{2}}
\]

(4)

where, \(K_1, K_2, K_3\) are temperature-dependent parameters.

### 3.2 Sheet Charge Density of Top Hetero Interface AlInSb/InSb \((n_{s1})\)

The charge density of the top channel is found by substitute eqs. (3) and (4) in (2).

\[
n_{s1} = \frac{\varepsilon_A}{q T} \left( V_{fs} - \phi_{bi} - \Delta E_{c1} - \frac{q N_{Di} T_{si}^2}{2\varepsilon_A} \right) - K_1 \left( K_2 n_{i1} + K_3 n_{i1}^2 \right)^{\frac{1}{2}}
\]

(5)

\[
n_{s1} = \frac{q T}{\varepsilon_A} \left( \phi_{bi} + \Delta E_{c1} + K_1 - V_{fg} + \frac{q N_{Di} T_{si}^2}{2\varepsilon_A} \right) - \left( K_2 n_{i1} + K_3 n_{i1}^2 \right)^{\frac{1}{2}}
\]

(6)

The top channel sheet charge density \((n_{s1})\) is obtained as

\[
n_{s1} = \frac{-B + \sqrt{B^2 - 4AC}}{2A}
\]

(7)

where,

\[
A = \left( \frac{q T}{\varepsilon_A} \right)^2 - K_3
\]

\[
B = 2 \frac{q T}{\varepsilon_A} \left( \phi_{bi} + \Delta E_{c1} + K_1 - V_{fg} + \frac{q N_{Di} T_{si}^2}{2\varepsilon_A} \right) - K_2
\]

\[
C = \left( \phi_{bi} + \Delta E_{c1} + K_1 - V_{fg} + \frac{q N_{Di} T_{si}^2}{2\varepsilon_A} \right)^2
\]
3.3 Sheet Charge Density of Bottom Hetero Interface InSb/AlInSb ($\text{n}_{s2}$)

Similarly, the backchannel carrier concentration is fixed by the back gate bias ($V_{fg}$), but the large voltage applied to the top gate ($V_{fg}$) at $V_{fg} = V_{off1}$ the top channel enters into the subthreshold region and the carriers are got depleted subsequently at $V_{fg} = V_{off1} + K_1$. Therefore, the top gate bias is starting to modulate the back gate channel carrier concentration at $V_{fg} > V_{off1}$. The modulation of back-channel carrier concentration ($n_{sm}$) is expressed as $[24, 25]$

$$n_{sm} = \frac{\mathcal{E}_A}{q} (E_1 - E_2) - N_A T_{ch} \tag{8}$$

where the $E_1$ and $E_2$ are the vertical electric field at the top and bottom interface and is given by

$$E_1 = \frac{V_{fg} - V_{off1} - E_{F1}}{T} \tag{9}$$

$$E_2 = \frac{V_{fg} - V_{off2} - E_{F2}}{T} \tag{10}$$

Substituting eqs. (9) and (10) in eq. (8), we get the modulation of the back carrier concentration along with front gate voltage and the fixed bottom gate voltage is formulated as

$$n_{sm} = \frac{\mathcal{E}_A}{q} \left( \frac{V_{fg} - V_{off1} - E_{F1}}{T} - \frac{V_{fg} - V_{off2} - E_{F2}}{T} \right) - N_A T_{ch} \tag{11}$$

To obtain the charge control model for the modulated backchannel, the new relationship between the quasi-fermi energy level of back-channel ($E_{F1}$) and the modulated carrier concentration by front gate bias is required.

$$n_{s2} = n_{s2} - n_{sm} \tag{12}$$

The above equation leads to the new relationship between the $E_{F2}$ and $n_{s2}$ same as reported in Eq. (4) and is given by

$$E_{F2} = K_1 + \left( K_2 n_{s2} + K_3 n_{s2}^2 \right)^{1/2} \tag{13}$$

However, the depletion of charge carriers in the backchannel is equal to the accumulation of charge carriers in the top heterointerface. So that the top heterointerface is the function of $E_{F2}$ and it is formulated as

$$E_{F1} = -E_{F2} + E_1 T_{ch} \tag{14}$$

In the last term in the above equation, the multiplication of top hetero-interface ($E_1$) and channel thickness ($T_{ch}$) is added to analyse the effect of channel thickness in the charge control model.

$$E_{F1} = -K_1 - \left( K_2 n_{s2} + K_3 n_{s2}^2 \right)^{1/2} + E_1 T_{ch} \tag{15}$$

Similar to front channel sheet charge density ($n_{s1}$) and carrier density $n_{s2}$ of the backchannel is found from the eq. (4) (11) and (15).

The total sheet charge density of the Asymmetric DG-HEMT device for the three regions of operation is expressed as

$$n_s = \begin{cases} 
  n_{s1} + n_{s2}, & V_{fg} > V_{off1} + K_1 \\
  n_{s1} + n_{s2}, & V_{off1} < V_{fg} < V_{off1} + K_1 \\
  n_{s2}, & V_{fg} \leq V_{off1} + K_1 
\end{cases} \tag{16}$$

3.4 Drain Current Model for AlInSb/InSb/AlInSb Silicon Substrate Asymmetric DG-HEMT

The general solution of the drain current model for Asymmetric DG-HEMT is given by

$$I_D = q W n_s(y) v(y) \tag{17}$$

where the $v(y)$ is the carrier velocity in the perpendicular direction of the heterointerface taken as a field-dependent parameter $[26, 27]$ and expressed as

$$v(y) = \begin{cases} 
  \mu_0 \frac{E(y)}{E_c} & E < 2E_c \\
  \frac{E(y)}{2E_c} & E \geq 2E_c \\
  v_{sat} & E \geq 2E_c 
\end{cases} \tag{18}$$

where the $E(y) = \frac{dV(y)}{dy}$ is the electric field in the 2-dimensional electron gas, $\mu_0$ is the carrier mobility at the heterointerface, $v_{sat}$ is the electron saturation velocity at the interface and $E_c = \frac{\sqrt{2}}{4\pi} \mu_0$ is the critical field.

3.5 Front Channel Drain Current ($I_{D1}$) at the Linear Region ($V_d < V_{sat}$)

The drain current for the top channel at the linear region is found by substituting the eq. (18) in general drain current model Eq. (17) for $v(y)$ at $E < 2E_c$.

$$I_{D1} = q W n_s(y) \frac{\mu_0}{1 + \frac{E(y)}{2E_c}} \tag{19}$$

$$I_{D1} \left[ 1 + \frac{dV(y)}{2E_c dy} \right] = q W n_s(y) \mu_0 \frac{dV(y)}{dy} \tag{20}$$

Taking integration on both sides with respect $y$ from “0” to “L” and substituting the boundary conditions $V(0) = 0$ and $V(L) = v_{dr}$, we obtain the drain current of the top channel.

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as

\[ I_{D1} = \frac{w q \mu_0 f(x_1) - f(x_0)}{2 A \left( L + \frac{H_0 V_d}{2 \nu_{sat}} \right)} \] (21)

where

\[ f(x) = -B + \frac{2x^2}{3} \]

\[ x_1 = \left( \frac{q T}{E_A} \right)^2 K_2 + 2 \frac{q T}{E_A} \left( \phi_{bi} + \Delta E_{c1} + K_1 - V_{fg} + \nu_{sat} + \frac{q N_D T_s^2}{2E_A} \right) - K_2 \]

\[ x_2 = \left( \frac{q T}{E_A} \right)^2 K_2 + 2 \frac{q T}{E_A} \left( \phi_{bi} + \Delta E_{c1} + K_1 - V_{fg} + \nu_{sat} + \frac{q N_D T_s^2}{2E_A} \right) - K_2 \]

3.6 Front Channel Drain Current (I_{D1}) at Saturation (V_d \geq V_{sat})

The drain current is obtained for the saturation region at the channel near the drain, the electron velocity is saturated at \( \nu_{sat} \).

\[ I_{sat1} = \frac{w q \nu_{sat} \left( -B + \frac{2x^2}{3} \right)}{2 A} \] (22)

where,

\[ x = \left( \frac{q T}{E_A} \right)^2 K_2 + 2 \frac{q T}{E_A} \left( \phi_{bi} + \Delta E_{c1} + K_1 - V_{fg} + \nu_{sat} + \frac{q N_D T_s^2}{2E_A} \right) - K_2 \]

\[ \nu_d = \nu_{sat} \] at the channel near the drain.

3.7 Back-Channel Drain Current (I_{D2})

The expression of the drain current for backchannel hetero interface (I_{D2}) requires the sheet charge density (n_{sm}) (variation effect of back-channel due to the front gate voltage) at the backchannel but it is complicated to solve eqs. (15) and (4) iteratively. So that the sheet charge density (n_{sm}) is obtained using the polynomial relationship between the modulated carrier densities (n_{sm}) and front gate bias \( V_{fg} \).

The drain current for backchannel hetero interface is obtained using a fourth-order polynomial relationship.

\[ n_{sm} = \sum_{j=1}^{4} p_j \left( V_{fg} - V(y) \right)^j \] (23)

where, \( p_j \) is the polynomial coefficient.

Substituting the eq. (23) and (18) in (17) we obtain the drain current expression for backchannel hetero interface for \( v(y) \) at \( E < 2 E_c \) as follows

\[ I_{D2} = w q \sum_{j=0}^{4} p_j \left( V_{fg} - V(y) \right)^j \left( \frac{H_0 E(y)}{E(y)} \right) \frac{E(y)}{2 E_c} \] (24)

Integrating the above equation concerning for to y from “0” to “L” and \( V(0) = 0 \) and \( V(L) = V_{DS} \), the drain current expressed as.

For linear region

\[ I_{D2} = \frac{w q \mu_0}{L + \frac{H_0 V_d}{2 \nu_{sat}}} \sum_{j=0}^{4} p_j \left( V_{fg} - V_{DS} \right)^j + 1 \] (25)

For Saturation region

\[ I_{sat2} = \frac{w q \mu_0}{L + \frac{H_0 V_d}{2 \nu_{sat}}} \sum_{j=0}^{4} p_j \left( V_{fg} - V_{DSat} \right)^j + 1 \] (26)

Finally, the total drain current is obtained from the top and bottom heterointerface drain current eqs. (21) to (25) and is express as

\[ I_D = \begin{cases} 
I_{D1} + I_{D2}, & V_{fg} > V_{off} + 1 + K_1 \\
I_{D1} + I_{D2}, & V_{fg} < V_{off} + 1 + K_1 \\
I_{D2}, & V_{fg} \leq V_{off} + 1 + K_1 
\end{cases} \] (27)

3.8 Small Signal Equivalent Circuit

The traditional small signal equivalent circuit is shown in Fig. 3, it consists only of the intrinsic components. \( R_{11}, R_{22}, R_{gd1}, C_{gd1}, C_{gd2}, C_{gs1}, C_{gs2} \), are the intrinsic parasitic resistance and capacitance. The ratio between the variation in the drain current with respect to changes in the drain to source voltage is called drain current (G_d). [27]

\[ G_d = \frac{dI_d}{dV_{ds}} \mid_{V_{gs}=\text{Constant}} \] (28)

The \( Y_m \) is calculated using the following equation

\[ Y_m = g_m e^{-i\omega t} \] (29)

where \( V_{gs1} = V_{fg}, V_{gs2} = V_{bg}, \tau - \text{transient time}, \omega - \text{angular frequency} \).

\( g_m \) is the transconductance and it is calculated as the ratio of drain current to gate to source voltage with constant drain voltage.

4 Results and Discussions

In this sheet charge model, the 2-dimensional electron gas concentration of the front and back channel is analyzed with
a fixed back gate voltage and variable front gate voltages for three different regions of operation at the position of \( x = 0 \) and \( x = T_{ch} \). Also, the relationship of the backchannel with the applied front gate voltage is expressed using Gauss’s Law. The drain current is developed separately for the front and back channel because the independent bias is applied to the gates and the device act as a three-port system. The drain current is compared with sentaurus 3D-TCAD tool simulation results. In the device simulation, the carrier transport mechanism is represented using concentration-dependent mobility, electric-field dependent mobility, Shockley-Read-Hall (SRH) recombination, Auger recombination, and Bandgap narrowing techniques [28–31].

Fig. 4 (a) and (b) predict the electron density modulation in the backchannel along with front gate voltage for three different fixed back gate voltages. The negative voltage at the front gate starts to deplete the charge carriers on the backchannel. The continuous injection of increasing negative voltage on the front gate completely depletes all charge carries and makes the backchannel turn off, this modulation effect is predicted in eq. (11). Further, the backchannel carrier concentration also depends on the back gate bias, the channel thickness, and doping, it is shown in Fig. 4(b). In this plot, both the channel thickness (\( T_{ch} = 30 \) nm, 25 nm) is saturated at the same level of the backchannel carrier concentration with fixed back gate bias. But, the thicker channel requires more negative voltage to turn off the device. Also, the thick channel layer creates two separate 2DEG at the top and bottom of the channel layer.

The top gate controls both channels but the shrinking in the channel thickness may cause two junctions of the interface to get overlap. Besides, the channel thickness causes a serious problem in the threshold voltage variation. The proper selection of the channel thickness is yields better performance in the dual-channel technology. If the fixed voltage of the bottom gate is reduced, the carrier concentration of the backchannel get reduces, which also reduces the required front gate voltage to completely deplete charge carriers in the backchannel. This effect is predicted in Fig. 4 a and b, the back gate bias at \( V_{bg} = -0.1 \) V requires more negative front gate bias to deplete the charge carriers in the backchannel but it is comparatively low for \( V_{bg} = -0.2 \) V and \( V_{bg} = -0.3 \) V.

The expression (16) indicates that the total charge carrier concentrations of the channel depends on both variable front gate voltage and fixed back gate voltage but the threshold voltage varies concerning the carrier concentration of both channel. Therefore, the backchannel has less threshold voltage than the front channel, for which the back gate bias is fixed less than the variable front gate voltage.

The front channel electron density \( n_{s1} \) for three different \( \delta \) doping (\( 3 \times 10^{12}, 2 \times 10^{12}, 1 \times 10^{12} \) cm\(^{-2}\)) and back channel electron density for two different \( \delta \) doping (\( 3 \times 10^{12}, 2 \times 10^{12} \) cm\(^{-2}\)) with three different back gate voltages (\( -0.1, -0.2, -0.3 \) V)
−0.3 V) are compared in fig. 4.2 a & b. Both graphs clearly show that the density of charge carriers in both channels depends on the delta doping concentration of the barrier layer. According to the solution given in eq. (14). After the front channel reaches the subthreshold region, the carrier density in the quantum well increases with the accumulation of electrons from the top barrier layer also depleted electrons from the backchannel. Therefore, the single gate takes control of both channels in the Asymmetric Silicon substrate DG-HEMT. Further, the electrons accumulation depends on the barrier width. If the device has a larger barrier width, it increases the distance between the channel and the gate foot causes the reduction in electrons in the quasi-fermi level, this was explained in the previous section. The subthreshold voltage also varies with the channel thickness and the interface charges of 2DEG.

In the Asymmetric DG-HEMTs, the doping is done on both sides of the channel (InSb) with the AlInSb barrier layer to enhance the accumulation of electrons in the quantum well. Therefore, doping profile analysis is an unavoidable important parameter in the density of carrier concentration calculation on both the top and bottom of the two-dimensional electron gas. The top barrier doping profile was explained in Fig. 5(a) and the bottom barrier doping profile analysis is shown in Fig. 5(b). The graph clearly shows the larger delta doping profile with the same back gate voltage produces high carrier density on back channel. Also, the larger doping profile shifts the entire plot to the left side, which indicates that the variation of threshold voltage with delta doping. Further, the electron concentration drop on the channel by decreasing the delta doping in the barrier layer is compensated by surface charge density.

The charge density $n_{s1}$, $n_{s2}$, and total charge density $n_s$ relationships are shown in Fig. 6, for two different back-gate voltages ($V_{bg} = −0.1$ V and $V_{bg} = −0.3$ V). The graph clearly shows the total carrier density $n_s$ follows then $n_{s2}$ up to the front channel reaches the subthreshold region of the operation. When the top channel enters into the subthreshold region, the total carrier density $n_s$ variation depends on both the top and bottom of carrier concentration ($n_s$). In addition, the plot shows that the top channel reaches the maximum density and it depletes the backchannel carrier concentration due to modulation effects on the backchannel by front gate bias. But the total carrier density is the function of both the top and bottom carrier density of quantum well. However, the backchannel concentration is the only function of back gate voltage and the density of the charge carriers is saturated and no longer varies for fixed back gate bias. Therefore, the total charge density ($n_s$) variation is only due to the modulation effect in the top channel charge carriers.
The function of donor layer thickness ($T_d$) in the gate to source capacitance along with back gate voltage is shown in Fig. 7. The thick donor layer (5 nm) shows the low gate to source capacitance but it led to more negative voltage needed to deplete the quantum well formulated under the donor layer. As mentioned in Fig. 2, the distance between the gate foot and the quantum well is increased, the gate loses control over the channel.

The frequency variation for three different back gate voltages along with front gate voltage ($V_{fg}$) is shown in Fig. 8. The cut-off frequency ($F_t$) linearly increasing by increasing the biasing voltage on the back gate from negative and reaches the maximum of operation speed and get reduces with increasing front gate biasing voltage. These effects were observed because of modulation in the transconductance and gate to source capacitance when increasing voltage in the front gate beyond the limit of saturation. So, understanding of transconductance relationship with front and back gate voltages is an unavoidable analysis and it is shown in Fig. 9.

It is observed that the transconductance is increasing along with back gate voltage with constant front gate bias and reaches the maximum, further increasing bias at the back gate it starts to decreases. Also, increasing front gate bias could achieve high total transconductance. Because the front gate controls the total transconductance of the device.

The drain current for three different back gate biases with front gate voltage is shown in Fig. 10. The plot clearly shows that the back gate bias varies the threshold voltage because the backchannel concentration is a function of the back gate voltage. The variable threshold voltage achieved by modulating

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**Fig. 7** Gate Source Capacitance variation along with back gate voltage for three different channel thickness $T_d = 2$ nm, $3$ nm, $5$ nm, $V_{ds} = 0.3$ V

**Fig. 8** Cut-off frequency variation along with front gate voltage for three different back gate voltage $V_{bg} = -0.1$ V, $0.1$ V, $0.3$ V at $V_{ds} = 0.3$ V

**Fig. 9** Transconductance ($g_m$) variation along with back gate voltage for three different front gate voltage $V_{fg} = -0.1, 0.2$ V, $V_{ds} = 0.3$ V

**Fig. 10** Variation of drain current versus front gate voltage for three different back gate voltages ($V_{bg} = 0.1$ V, $V_{bg} = 0$ V, $V_{bg} = -0.1$ V)
backchannel carrier concentration with back gate voltage also provides better results against the short channel effects. The backchannel carrier concentration is fixed by the fixed back gate voltage during the fabrication. The developed drain current expressions result closely matched with sentaurus TCAD simulation results.

Figure 11 shows the drain current variations versus drain to source voltage for different front gate voltages. The drain current results are developed according to eq. (27) by considering both the channels. The carrier concentration of the channel or drain current approaches zero at which the threshold voltage is calculated for the Asymmetric DG-HEMT. The drain current for various front gate biases compared with sentaurus TCAD simulation results.

5 Conclusion

A compact model has been developed to predict the sheet charge density and small signal intrinsic parameters for Asymmetric Silicon substrate DG-HEMT. The sheet charge density (n_s) is calculated by comparing the quasi-fermi energy level to the back channel modulation effects caused by various front gate biases. Various parameters such as back gate bias, doping concentration, barrier, and InSb channel thickness were used to study the variation of carrier concentration on dual channels. The influence of the carrier concentration modification on the threshold voltage is also investigated and components with variable threshold voltage are used in high-frequency mixed-mode circuits. The proposed small signal model is used to determine the Gate to Source Capacitance and Cut Off frequency as a function of dual channels, and the Cut Off frequency was found to be around 197 GHz for \( V_{bg} = 0.3 \) V. For \( V_{fg} = 0.2 \) V, the transconductance of the dual channel is also around 2390 Sm/mm. Furthermore, the model parameters are expanded to develop the drain current characteristics of Asymmetric Silicon wafer DG-HEMTs. The drain current analytical results are validated and compared to the sentaurus 3-D TCAD results. The simulation results are very close to the charge control model’s obtained results.

Availability of Data and Material There are no linked research data sets for this submission. The following reason is given: No data was used for the research described in the article.

Code Availability Not Applicable.

Author's Contributions Author 1 (T.Venish Kumar): Conceived and design the analysis, contributed data, analysis tools, and wrote the paper. Author 2 (M.Venkatesh): Performed the analysis, calibrated the results, and wrote the paper. Author 3 (B.Muthupandian): Worked in the TCAD portion of the proposed device and analytical Modeling. Author 4 (G.Lakshmi Priya): Worked in TCAD simulation of drain current modeling, and wrote the paper for the corresponding portion.

Funding The authors of the manuscript did not receive any funding, grants, or in-kind support in support of the research or the preparation of the manuscript.

Declarations Yes

Consent to Participate Yes

Consent for Publication Yes

Conflict of Interest All authors have participated in (a) conception and design, or analysis and interpretation of the data; (b) drafting the article or revising it critically for important intellectual content; and (c) approval of the final version. This manuscript has not been submitted to, nor is under review at, another journal or other publishing venue. The authors have no affiliation with any organization with a direct or indirect financial interest in the subject matter discussed in the manuscript.

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• This manuscript has not been submitted to, nor is under review at, another journal or other publishing venue.
• The authors have no affiliation with any organization with a direct or indirect financial interest in the subject matter discussed in the manuscript.
• The following authors have affiliations with organizations with a direct or indirect financial interest in the subject matter discussed in the manuscript.

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Fig. 11 Variation of drain current versus drain voltage for different front gate voltages
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