ISyNet: Convolutional Neural Networks design for AI accelerator

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Abstract

In recent years Deep Learning reached significant results in many practical problems, such as computer vision, natural language processing, speech recognition and many others. For many years the main goal of the research was to improve the quality of models, even if the complexity was impractically high. However, for the production solutions, which often require real-time work, the latency of the model plays a very important role. Current state-of-the-art architectures are found with neural architecture search (NAS) taking model complexity into account. However, designing of the search space suitable for specific hardware is still a challenging task. To address this problem we propose a measure of hardware efficiency of neural architecture search space – matrix efficiency measure (MEM); a search space comprising of hardware-efficient operations; a latency-aware scaling method; and ISyNet – a set of architectures designed to be fast on the specialized neural processing unit (NPU) hardware and accurate at the same time. We show the advantage of the designed architectures for the NPU devices on ImageNet (Figure 1) and the generalization ability for the downstream classification and detection tasks.

1 Introduction

Specialized neural processing unit (NPU) hardware was developed for fast neural network inference and training. The core feature of these devices is a design of highly optimized matrix multiplication unit, as the most computationally expensive operations – convolution and fully-connected layer – can be reduced to matrix multiplication. Speed of deep neural networks (DNN) inference and training on NPU devices depends not only on amount of matrix multiplication operations, but also on optimal data transfer and vector operations. To design a set of architectures fast for specific device and accurate at the same time a researcher needs to pass the following steps: find and construct a search space, adapt search method for the developed search space, decide how to take complexity of architectures into account. To address these issues we propose several steps, which make process of architectures search much easier. Our main contributions presented in this paper are:

- matrix efficiency measure (MEM) - novel measure for numerical evaluation of efficiency of DNN architectures and search spaces to the NPU hardware;
- NPU-efficient search space design having high MEM value;
• NPU-efficient scaling algorithm that allows to scale architectures with respect to the latency on the target hardware;
• ISyNet - novel family of NPU-efficient architectures that provide optimal accuracy vs. latency trade-off and have strong generalization ability proven on various downstream datasets and computer vision tasks. We open-sourced ISyNet architectures in MindSpore Model Zoo.

https://gitee.com/mindspore/models/tree/master/research/cv/ISyNet

2 Background and Related Art

Search of accurate and fast architectures for computer vision was a tricky work for a long time. VGGNet [40] with 19 convolutional layers was proposed in 2014 and showed the benefit of constructing complex powerful models. ResNet [7] architectures were proposed in 2015 to overcome the problem of training very deep networks. This work gave technology for successful training of architectures up to 200 layers with the help of residual connections. One of the first and still popular research works considering model complexity is a MobileNet architectures family [9, 39]. Authors used depth-wise separable convolutions to build lightweight deep neural networks.

NAS was developed to change paradigm of neural networks construction and automate the work of human researchers. NAS consists of 3 main parts: search space, search method and response function. The search space is defined as a subspace of all architectures limited by some manually defined constraints. The choice of the search space is a key point of NAS. However, it isn’t deeply discussed in the literature. Typical search spaces are: hierarchical search space [43] and cell-based search space [49]. Main search methods are reinforcement learning (RL) [48], evolutionary algorithms (EA) [34], surrogate-model based optimization (SMBO) [22, 25] and one-shot approaches [23]. RL, EA and SMBO are time consuming, but found architectures outperform to those found by one-shot method [36]. As a response function authors typically use task-specific metrics (classification top1 accuracy, detection mAP and so on) possibly combined with complexity penalty [2].

Thanks to NAS, automatically constructed architectures became state-of-the-art first for small datasets such as CIFAR-10 [46] and later for big datasets such as ImageNet [44]. Platform-aware NAS [43] allows to look for models with a good trade-off between the accuracy and the latency on the mobile devices. NAS requires a huge amount of computational resources, that’s why it’s computationally expensive to obtain architectures for all necessary complexity scenarios. To overcome this problem scaling methods are used [44]. EfficientNet series of architectures obtained by NAS and scaled with compound scaling are now state-of-the-art on the ImageNet [31]. While compound scaling considers FLOPS as a complexity measure of an architecture other researches show that total activations number in the model has stronger influence to the latency on the real hardware than the FLOPS [32]. Authors of the EfficientNet-EdgeTPU [6] models family designed to be efficient on the Google Edge TPU devices conclude that theoretical computation measures (MACs, FLOPS) are not an optimal proxy for the real latency and use special cycle-accurate performance simulator. In our work we use surrogate-model based optimization. This approach uses a surrogate model \( f \) to approximate the response function \( r \). This model is trained on meta-dataset which contains architecture descriptors and their response values gathered during the architecture search: \( H = \{ (\alpha_1, f(\alpha_1)), (\alpha_2, f(\alpha_2)), \ldots \} \). Generally, surrogate model is trained to minimize squared error: \( L = \sum_{(\alpha, f(\alpha)) \in H} (f(\alpha) - f(\alpha))^2 \). In practice very precise estimation is not necessary as long as surrogate provides a useful ranking to identify promising candidate. After candidate \( \alpha^* \) is trained and evaluated corresponding meta instances \( (\alpha^*, f(\alpha^*)) \) are added to \( H \) and the surrogate model is updated.

Figure 1: Accuracy/latency trade-off for different models on ImageNet. ‘ISyNet-N’ curve shows our models results; ‘ResNet baseline’ denotes original ResNet results; ‘ResNet+’ denotes original ResNet models trained with our training procedure; ‘MobileNetV2’ and ‘EfficientNet-EdgeTPU’ [6] curves denote original corresponding architectures.
3 Problem

3.1 NPU design and constraints

There exist a number of AI acceleration hardware (e.g. Google Cloud TPU [5, 16], NVidia Jetson [29], Huawei Ascend [12], Intel Movidius Myriad [13]), and these devices set a constraints for the DNNs to be deployed. These devices are typically good at parallelizable tasks of tensor and matrix multiplications and additions as well as other operations commonly used in DNNs, such as activation functions and other element-wise operations. In our paper we consider the optimization for Ascend 310 NPU based on DaVinci architecture [11], however, our model can be implemented for any AI accelerators that support 2D convolution with non-square kernels. Example of an application for this platform can be found in [45].

The AI core is a main part of Ascend 310 NPU and it executes tensor and vector operations. Three main compute units of AI Core are: the cube unit, which performs the matrix multiplications, including the fully-connected layers and the convolutions; the vector unit which executes the vector operations like an element-wise sum of tensors, batch normalization [14] and the activation functions; the scalar unit which is responsible for the scalar operations and controls the program flow and addressing.

The cube unit performs multiplication of two 16x16 float16 matrices or 16x32 and 32x16 int8 matrices at a time, and this is one of the most important constraint imposed by the design of the cube unit. Matrices of larger size are multiplied by parts. If a size of multiplied matrices is less than specified they will be padded by zeros. It is acceptable, but the highest cube unit utilization is reached for the matrices with a size divisible by 16 or 32 depending on the computation precision. The vector unit is responsible for the vector computations. It provides less computational power than the cube unit, but the capabilities of computations are more flexible. To process and store the data there are several storage units in AI core and in some scenarios data data buses may become a bottleneck.

What properties should an NPU-efficient neural architecture search space have?

- For all shapes of tensors (including weights and activations) that are processed by the Cube Unit divisibility by 16 (considering float16 precision) is preferable.
- Matrix operations are more preferable than vector operations and operations with data. Operations that could be reduced to matrix multiplication (e.g. Convolutions and Fully-connected layers) are preferable over operations that can be done on the Vector Unit only. The only exception is “operator fusion” mechanism that allows to fuse vector operations following matrix operation into one fused operation. An example of such efficient fusion is a sequence (Convolution → BatchNorm → Activation).
- When possible it is better to avoid an element-wise product, sum and permutation.
- Every operation in a computational graph requires input and output data to be transferred, which increases the total latency. Branched architectures like DenseNet [10] or Inception [41] should be avoided. Chain-like graph is preferable. The number of residual connections should be minimized.
- Lightweight activation functions (e.g. ReLU) are preferable over complex ones (e.g. Swish [33], Mish [27] or GELU [8])

3.2 Matrix Efficiency Measure

To evaluate efficiency of specific architectures and whole search spaces to NPU we propose a novel Matrix Efficiency Measure (MEM). Let us consider three most important sources of latency during neural networks inference: matrix operations, vector operations and data transfer (including input, output and weights). Scalar operations are negligible and not counted for simplicity.

For each operation $o_i$ in Neural Network $A$ we can define the following measures: $m(o_i)$ – the number of matrix operations; $v(o_i)$ – the number of vector operations. $d(o_i)$ – the number of input, output data and weights of the operation. Matrix efficiency measure for architecture $A = \{o_1, o_2, \ldots, o_N\}$ can be estimated as follows:

$$MEM(A) = \frac{w_m \cdot \sum_{i=1}^{N} m(o_i)}{\sum_{i=1}^{N}(w_m \cdot m(o_i) + w_v \cdot v(o_i) + w_d \cdot d(o_i))}$$

$\forall A : MEM(A) \in [0; 1)$ and the closer $MEM(A)$ to 1 the more efficient $A$ to NPU design, because matrix operations are preferable over the others. For a specific design space $D = \{A_1, A_2, \ldots, A_K\}$ mean matrix efficiency measure can
Figure 2: Overall scheme of ISyNAS - NPU-aware architectures search algorithm. Algorithm is based on 2 surrogate models (SM). One for accuracy and another for latency. After gathering meta-dataset of architectures and training SMs we sample architectures with limited latency and good estimation of accuracy. Meta-dataset updated and SMs retrained. Best found models scaled with scaling procedure and trained with long improved training procedure.

be estimated as follows:

$$mMEM(D) = \frac{1}{K} \sum_{j=1}^{K} MEM(A_j);$$  \hfill (2)

The closer $mMEM(D)$ to 1 the more efficient whole design space $D$ to NPU design.

To find values of $w_m, w_v$ and $w_d$ we train the following linear regression model that approximates latency of architecture $A$:

$$lat(A) = w_0 + w_m \cdot \sum_{i=1}^{N} m(o_i) + w_v \cdot \sum_{i=1}^{N} v(o_i) + w_d \cdot \sum_{i=1}^{N} d(o_i)$$  \hfill (3)

In our experiments we found that: $w_0 = 0.773; w_m = 2.57e-9; w_v = -1.26e-8; w_d = 3.36e-8$. This model has mean absolute percentage error $12.54\%$ and coefficient of determination $0.94$ which is reasonable for such a simple model. Negative value of $w_v$ can be explained by the fact that $m(o_i), v(o_i)$ and $d(o_i)$ are not linearly independent. We used linear regression model because of its simplicity and interpretability. Ablation study for the latency models is presented in the supplementary materials.

Table 1 shows hardware efficiency of operations according to our model. $Conv7x7, Conv5x5, Conv3x3, Conv1x1$ and convolutions with non-squared kernel $(7x1, 5x1, 3x1)$ show similar efficiency. Depthwise convolutions efficiency

| Operation       | #Matrix ops. | #Vector ops. | Data ops. | MEM(op)  |
|-----------------|--------------|--------------|-----------|----------|
| Conv7x7         | 2.9e+11      | 0            | 2.9e+7    | 9.7e-1   |
| Conv5x5         | 1.5e+11      | 0            | 2.0e+7    | 9.6e-1   |
| Conv3x3         | 5.4e+10      | 0            | 1.4e+7    | 9.2e-1   |
| Conv7x1         | 4.2e+10      | 0            | 1.3e+7    | 9.0e-1   |
| Conv5x1         | 2.3e+10      | 0            | 1.2e+7    | 8.8e-1   |
| Conv3x1         | 1.8e+10      | 0            | 1.1e+7    | 8.2e-1   |
| Conv1x1         | 6.0e+9       | 0            | 1.05e+7   | 6.2e-1   |
| DepthWiseConv5x5| 3.3e+8       | 0            | 1.01e+7   | 8.6e-2   |
| DepthWiseConv3x3| 1.2e+8       | 0            | 1.01e+7   | 3.2e-2   |
| Pooling3x3      | 0            | 2.2e+7       | 1.1e+7    | 0        |
| ReLU            | 0            | 6.5e+6       | 1.3e+7    | 0        |
| ReLU6           | 0            | 1.3e+7       | 1.3e+7    | 0        |
| Swish           | 0            | 1.3e+7       | 1.3e+7    | 0        |
| BatchNorm       | 0            | 5.2e+7       | 1.3e+7    | 0        |
| ElementwiseAdd  | 0            | 6.5e+6       | 1.9e+7    | 0        |
| Concatenation   | 0            | 0            | 2.6e+7    | 0        |

Table 1: Averaged matrix, vector, data and MEM characteristics of different operations
are less by one order. Operations which do not have matrix operations (poolings, activations, BatchNorms, addition and concatenation) are considered as non-efficient for NPU.

However, BatchNorm and activation placed after convolution operation can be efficiently fused into one operator and do not result in significant slowdown at the inference stage. Elementwise addition and concatenation operations are widely used in residual blocks, which is essential for convergence of the model training. Thus, we can’t avoid these blocks at all, but can use them flexibly, depending on real impact to the model properties.

4 Method

4.1 Search space design

To optimize architecture search we propose the search space, which incorporates only suitable for NPU operations and use flexible block length, width to add additional freedom in NAS. This search space is defined by the following set of rules:

- Model is divided into $NS$ stages, $NS \in [1, ..., 6]$ is not fixed, but limited;
- Every stage $s \in [1, ..., NS]$ is divided into blocks $Bs$ of identical structure. The number of blocks $NBs \in [1, ..., 20]$ in each stage is not fixed, but limited;
- Every block $Bs$ is divided into four edges ($Es,i$) each of them can be a convolution with kernel 1x1, 3x3, 5x5, 7x7, sequence of convolutions with non-square kernels 1x3+3x1, 1x5+5x1, 1x7+7x1 or an identity operation;
- Output of the block could be summed up with its input by a skip connection which is defined by the flag $SKs \in [0, 1]$ for all blocks in the stage $s$;
- Each convolution edge has the follow-up normalization operation (BatchNorm) and coupled with an activation (ReLU);
- Last non-identity edge could be uncoupled with activation which is defined by flag $LAs \in [0, 1]$ for all blocks in the stage $s$.
- The number of output channels of block $Bs$ is $2^{2i+CI_s}$, where $CI_s \in [0, 2]$ is searched non-negative integer defined for all blocks in the stage $s$;
- The number of output channels for every intermediate (except the last one) edge of blocks in the stage $s$ is multiplied by $EFs$ – positive integer searched parameter;
- First block of stage differs from all others. It has stride 2 in the first non-identity edge and no skip connection.

Flexible block length and skip connections together with hardware-efficient operations make the proposed search space better for hardware-targeted NAS. Comparison of mMEM values for different search spaces are shown in the table 2. ISyNet space outperforms ResNet [7], MobileNetV2 [39] and MNasNet [43] search spaces.

| Design space | #arch | mMEM  |
|--------------|-------|-------|
| ResNet       | 1000  | 0.294 |
| MobileNetV2  | 100   | 0.167 |
| MNasNet      | 100   | 0.17  |
| ISyNet-N (ours) | 3800 | 0.378 |

Table 2: $mMEM$ of different design spaces. Average $mMEM$ of proposed design space is better, then ResNet due to flexible block length and skip-connections. MobileNet and MNasNet search space $mMEM$ is worse due to non-optimal NPU operations.

4.2 Search method

As it is shown in [32, 6] FLOPS and MACs are not the best option to measure the complexity for the real hardware. In our work we use the accuracy and the latency surrogate models for efficient and more accurate search of the architectures and scaling. Overall scheme of ISyNAS, NPU-aware neural architecture search approach, is shown on the Figure 2. We use a surrogate model (SM) based optimization. To train SM we encode each architecture according to the proposed notation of search space design with following vector:

$$E = (NS, [V_{1}, V_{2}, ..., V_{NS}]),$$

$$V_s = (LAs, NBs, EFs, SKs, CI_s, E_{s,0}, E_{s,1}, E_{s,2}, E_{s,3}), s \in [1, ..., NS]$$

(4)

The value of $E_{s,i} \in [0, 7]$ is coded with following encoding: (conv1x1: 0, conv3x3: 1, conv5x5: 2, conv7x7: 3, conv1x3+conv3x1: 4, conv1x5+conv5x1: 5, conv1x7+conv7x1: 6, Identity: 7). If $NS < 6$ encoding vector is padded.
with zeros. For SM we use LSTM architecture to process the encoded vector and apply fully-connected layer to the resulting embedding. We train two different SM for the accuracy and the latency. To train SM we collected dataset of 400 architectures trained on ImageNet and measured on Ascend 310 NPU with batch 16.

We use following training procedure to collect dataset: SGD optimizer with momentum 0.9, 2 epochs warmup to maximum learning rate 0.4, 120 epochs with exponential learning rate decay, multiplying by 0.1 every 30 epochs, weight decay 0.0001, 8 NVidia V100 GPUs, total batch size 1024, O1 optimization.

4.3 Scaling algorithm
Tan et al. [44] proposed a method of compound architecture scaling which performs the small exhaustive search of the scaling parameters for width, depth and input resolution. For this purpose we select the parameters of architecture related to depth ($NB_s$) and width ($EF_s, CI_s$) and measure their impact on the accuracy and the latency. We have empirically found that increase of parameters related to the depth provide better accuracy/latency trade-off, than increase of parameters related to width. Out result matches experimental results obtained in [19]. Scaling of the input resolution affects only ImageNet performance, while does not affect the downstream tasks which are often use different resolution. Thus, we scale only depth of models and use the different scaling coefficients for the different stages. We use the latency as a scaling complexity function by carefully estimating latency of blocks. We perform the small brute-force search of scaling coefficients to find Pareto frontier of the scaled architectures. The comparison of our scaling method with the compound scaling is shown on the figure 3.

5 Experiments

5.1 Architectures
Found ISyNet architectures are described in the table 3. Every architecture is defined by its stages. Stages are defined by block patterns and number of blocks ($NB$). Block patterns are defined by the list of operations, presence of last activation ($LA$) and skip connection ($SK$). Architectures N0, N1, N2, N3 are found by NAS, while N1-S1, N1-S2, N1-S3 are found by scaling method from architecture N1. The process of the search took about 20000 GPU*hours which is comparable with the other approaches [36].

5.2 ImageNet experiments
To train our models on ImageNet [38] we use one server with 8 Ascend 910 NPUs and the following training setup: AdamW optimizer; 40 epochs warmup to maximum learning rate 0.001; 550 epochs with cosine learning rate decay, weight decay 0.05; batch size 1024 (128 per device); RandAugment [3] augmentation policy; Deep Mutual Learning [47] with larger model (for ISyNet models ISyNet-N3, for ResNet models ResNet-101), BatchNorm after the last fully-connected layer ("LastBN"), label smoothing. The ablation study for the listed tricks is presented in the supplementary materials. Training results are shown in the table 4 and Pareto frontiers are illustrated on the figure 1. For the fair comparison we train the ResNet models with our training procedure and they are presented in the table and figure as ResNet+. For the MobileNetV2 architectures our procedure does not bring an improvement and we use an original results. Latency of all resulting architectures are measured on the Ascend 310 NPU with batch size 16 and reduced to a single image.

5.3 Transfer learning experiments
To verify generalization ability of ISyNet models we do the transfer learning experiments for the following downstream datasets and tasks: classification (CIFAR-10, CIFAR-100 [18], Caltech 101 [20], Flowers [28], Oxford-IIIT Pet [30],
Table 3: Specification of found architectures.

| Model    | Stage | Operations in Block | $L_A$ | $N_B$ | $S_K$ |
|----------|-------|---------------------|-------|-------|-------|
| N0       | 0     | 5x5x16              | 1     | 1     | 0     |
|          | 1     | 3x3x32, 3x3x32      | 1     | 2     | 1     |
|          | 2     | 3x3x64, 3x3x64, 1x1x64, 1x1x64 | 1 | 4 | 1 |
|          | 3     | 1x1x128, 3x3x128    | 0     | 2     | 1     |
|          | 4     | 3x3x256, 3x3x256, 1x1x256 | 1 | 6 | 1 |
| N1       | 0     | 7x7x16              | 1     | 1     | 1     |
|          | 1     | 1x5x32+5x1x32, 1x1x32, 3x3x32, 5x5x32 | 1 | 1 | 1 |
|          | 2     | 3x3x128, 3x3x128, 3x3x128 | 1 | 4 | 1 |
|          | 3     | 3x3x128, 1x1x128, 3x3x128 | 1 | 6 | 1 |
|          | 4     | 1x1x256, 1x1x256, 1x1x256 | 1 | 3 | 1 |
| N1-S1    | 0     | 7x7x16              | 1     | 1     | 1     |
|          | 1     | 1x5x32+5x1x32, 1x1x32, 3x3x32, 5x5x32 | 1 | 1 | 1 |
|          | 2     | 3x3x128, 3x3x128, 3x3x128 | 1 | 5 | 1 |
|          | 3     | 3x3x128, 1x1x128, 3x3x128 | 1 | 6 | 1 |
|          | 4     | 1x1x256, 1x1x256, 1x1x256 | 1 | 6 | 1 |
| N1-S2    | 0     | 7x7x16              | 1     | 1     | 1     |
|          | 1     | 1x5x32+5x1x32, 1x1x32, 3x3x32, 5x5x32 | 1 | 1 | 1 |
|          | 2     | 3x3x128, 3x3x128, 3x3x128 | 1 | 6 | 1 |
|          | 3     | 3x3x128, 1x1x128, 3x3x128 | 1 | 8 | 1 |
|          | 4     | 1x1x256, 1x1x256, 1x1x256 | 1 | 7 | 1 |
| N1-S3    | 0     | 7x7x16              | 1     | 1     | 1     |
|          | 1     | 3x3x16, 7x7x16, 7x7x16 | 1 | 1 | 1 |
|          | 2     | 5x5x64, 3x3x64, 3x3x32 | 0 | 3 | 1 |
|          | 3     | 3x3x128, 1x1x128    | 0     | 17 | 1    |
|          | 4     | 1x1x512, 1x1x512, 1x1x512 | 1 | 2 | 1 |
| N2       | 0     | 5x5x32, 7x7x32      | 1     | 1     | 0     |
|          | 1     | 3x3x64, 3x3x64      | 0     | 5     | 1     |
|          | 2     | 3x3x128, 3x3x128, 3x3x128, 3x3x128 | 1 | 3 | 1 |
|          | 3     | 1x1x256+3x1x256, 1x1x256 | 0 | 13 | 1 |
|          | 4     | 1x1x1024, 1x1x1024, 1x1x1024 | 1 | 1 | 1 |
| N3       | 0     | 5x5x32, 7x7x32      | 1     | 1     | 0     |
|          | 1     | 3x3x64, 3x3x64      | 0     | 5     | 1     |
|          | 2     | 3x3x128, 3x3x128, 3x3x128, 3x3x128 | 1 | 3 | 1 |
|          | 3     | 1x1x256+3x1x256, 1x1x256 | 0 | 13 | 1 |
|          | 4     | 1x1x1024, 1x1x1024, 1x1x1024 | 1 | 1 | 1 |

Table 4: ISyNet performance results on ImageNet. Table shows, that ResNet-18 and ResNet-34 have very good MEM due to optimization of NPU devices to these specific architectures. In the same time average MEM of ResNet space has lower MEM according to table 2. It allow us to find architectures in our space, which outperform ResNets. We don’t show results for other type of architectures like MobileNet, EfficientNet as they are non-efficient on NPU according to figure 1.

Stanford Cars [17], Food-101 [1] and object detection (Pascal VOC 2007 [4], as a backbone for YOLOv3 [35]; MS COCO [21], as a backbone for Faster R-CNN [37]). The details about experimental setup are presented in the supple-
Figure 4: Results of transfer learning for different downstream tasks. Latency (in ms.) is plotted along the horizontal axis. Target metrics on the corresponding dataset are plotted along the vertical axis of each plot. Curves show stable improvement over ResNet architectures both for classification downstream datasets and as backbone for detection datasets.

Figure 5: ISyNet transfer learning performance results on the downstream tasks

Table 5: ISyNet transfer learning performance results on the downstream tasks

| Model          | CIFAR-10 | CIFAR-100 | Caltech-101 | Flowers | Oxford-IIIT Pets | Stanford Cars | Food-101 | VOC 2007 | COCO |
|----------------|----------|-----------|-------------|---------|------------------|---------------|----------|----------|------|
| ISyNet-N0      | 97.55    | 84.31     | 95.05       | 97.55   | 90.31            | 90.58         | 85.39    | 76       | 36.6 |
| ResNet-18+     | 97.35    | 83.9      | 94.92       | 97.19   | 91.39            | 90.28         | 85.89    | 76.54    | 35.6 |
| ISyNet-N1      | 97.92    | 85.27     | 95.44       | 97.97   | 91.86            | 92.68         | 88.16    | 78       | 37.5 |
| ISyNet-N1-S1   | 97.86    | 85.73     | 95.74       | 97.95   | 92.35            | 92.59         | 88.40    | 78.40    | 38.0 |
| ISyNet-N1-S2   | 98.05    | 85.91     | 95.74       | 98.21   | 92.65            | 92.83         | 88.59    | 78.94    | 38.4 |
| ISyNet-N1-S3   | 97.88    | 86.23     | 96.03       | 98.36   | 93.57            | 92.86         | 89.06    | 79.13    | 39.4 |
| ResNet-34+     | 98.17    | 86.13     | 95.05       | 97.64   | 93.30            | 92.09         | 87.99    | 79.67    | 39.1 |
| ISyNet-N2      | 98.07    | 86.65     | 95.87       | 98.59   | 93.55            | 92.62         | 88.60    | 78.30    | 39.3 |
| ISyNet-N3      | 98.3     | 87.1      | 96.26       | 98.72   | 93.46            | 93.46         | 89.69    | 80.90    | 41.3 |
| ResNet-50+     | 98.15    | 86.96     | 96.26       | 98.47   | 93.22            | 92.77         | 89.82    | 78.18    | 39.4 |

6 Conclusions

In this paper we study the problem of efficiency of neural networks for NPU devices - specialized AI accelerators. To address the question of “NPU-efficiency” estimation we propose MEM - novel measure of matrix computations efficiency in Neural Networks. With the help of MEM we design the search space for our convolutional backbones and do Neural Architecture Search in this space. Finally, we propose ISyNet - the family of NPU-efficient convolutional backbones that outperform strong NPU-efficient baselines by a significant margin and prove good generalization properties of ISyNet on many Computer Vision datasets and tasks.
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A Transfer learning experimental setup

For all classification tasks we used the following fine-tuning setup: SGD optimizer with momentum 0.9; learning rate 0.02; 300 epochs with exponential learning rate decay, multiplying it by 0.97 every 2.4 epochs; weight decay 0.0001; 8 NVidia V100 GPUs, total batch size 512; RandAugment augmentation policy; Exponential Moving Average of model weights with coefficient 0.9999.

For the object detection on Pascal VOC with YOLOv3 we used the following setup: image size 608x608, batch size 64 per GPU, 2 NVidia V100 GPU, 52000 iterations of SGD optimizer starting with learning rate 0.0005. We change the learning rate to 0.0001, 0.0002, 0.0005, 0.001, 0.0001 and 0.00001 at steps 400, 700, 900, 1000, 40000 and 45000.

For the object detection on COCO with Faster R-CNN we used the following setup: image size 608x608, batch size 32 per GPU, 8 NVidia V100 GPU, 120000 iterations of SGD optimizer starting with learning rate 0.0001. We change the learning rate to 0.01, 0.001, 0.0001 at steps 5000, 60000 and 80000.

B Ablation study for the MEM model

To study the impact of the latency regression model to $MEM$ value we trained several classic regression models to predict the latency based on the number of matrix operations, vector operations and amount of data transfer for each architecture. The results are presented in the table 6.

Let $f$ is a regression model and $A$ is an arbitrary architecture with number of matrix, vector and data transfer operations $m(A)$, $v(A)$ and $d(A)$ respectively. Then

$$\text{latency}(A) = f(m(A), v(A), d(A))$$

According to the table 6, all models show similar $R^2$ score and mean average percentage error (MAPE), but the linear regression model has better or equal quality of the prediction and has the interpretable coefficients which is more important for our study. Thus, we made a decision to use linear regression to estimate $MEM$. Note that we didn’t consider such models as nearest neighbors regression and decision trees regression because these models weren’t clearly interpretable in our task. It is important to note that values of $MEM$ score for different architectures are consistent across different regression algorithms.

| Model                      | $R^2$ score | MAPE   | MobileNetV2 | MnasNet | ResNet | ISyNet |
|-----------------------------|-------------|--------|-------------|---------|--------|--------|
| Linear Regression           | 0.944       | 12.54% | 0.167       | 0.17    | 0.294  | 0.378  |
| Ridge Regression            | 0.943       | 12.67% | 0.144       | 0.148   | 0.266  | 0.349  |
| Orthogonal Matching Pursuit | 0.944       | 12.54% | 0.167       | 0.17    | 0.294  | 0.378  |
| Bayesian Ridge Regression   | 0.944       | 12.54% | 0.167       | 0.17    | 0.294  | 0.378  |
| SGD Regressor               | 0.942       | 12.74% | 0.139       | 0.143   | 0.237  | 0.339  |
| Linear SVR                  | 0.944       | 12.59% | 0.155       | 0.158   | 0.279  | 0.363  |

Table 6: Results of different latency prediction models. Linear Regression, Ridge Regression and Bayesian Ridge Regression models were used with default hyperparameters. SGD Regressor and Linear SVR models were used with squared epsilon insensitive loss, Orthogonal Matching Pursuit was used with number of nonzero coefficients is equal to 3.

Dependency of latency on different types of operations is shown on the Figure 5. For some plots (e.g. latency vs. number of memory operations) near-linear dependency exists. For other plots linearity is not so clear, but the linear regression is still correspond to the maximal density of the data points.

C Ablation study for the training procedure

To investigate the impact of each training trick we sequentially disable them and train model ISyNet-N0. Results are shown in the table 7. We have found that the most beneficial tricks are BatchNorm after classifier’s Fully Connected layer; Exponential Moving Average [15] on model parameters; Deep Mutual Learning with stronger peer model [47]; and
training for longer time with smooth decay of learning rate (we multiply it by 0.97 every 2.4 epochs similar to [43]); All the listed tricks improve ISyNet-N3 by 4.69 top-1 ImageNet accuracy.

Figure 5: Dependency of latency on different types of operations. These plots show how the latency depends on the number of matrix, vector and data transfer operations. Additionally, we show the dependency between number of vector operations and data transfer.
| #  | LS | AW | LBN | RA | LT | DML | Top-1 Acc. | Δ       |
|----|----|----|-----|----|----|-----|------------|---------|
| 1  | -  | -  | -   | -  | -  | -   | 75.92      |         |
| 2  | -  | -  | -   | -  | -  | +   | 76.77      | +0.85   |
| 3  | -  | -  | -   | -  | +  | +   | 78.4       | +1.63   |
| 4  | -  | -  | +   | +  | +  | +   | 79.53      | +1.13   |
| 5  | -  | +  | +   | +  | +  | +   | 80.08      | +0.55   |
| 6  | +  | +  | +   | +  | +  | +   | 80.3       | +0.42   |
| 7  | +  | +  | +   | +  | +  | +   | 80.61      | +0.11   |

Table 7: The impact of training tricks to the accuracy of ISyNet-N3. ML denotes mutual learning [47]; RA denotes RandAugment [3]; LBN denotes Batch Normalization [14] after classifier’s fully connected layer; LT denotes number of training epochs, where '-' is 90 epochs and '+' is 550 epochs; AW denotes AdamW optimizer [24]; LS denotes Label Smoothing regularization [42].

| #  | RA | DML | LT | LBN | Top-1 Acc. | Δ       |
|----|----|-----|----|-----|------------|---------|
| 1  | -  | -   | -  | -   | 68.89      |         |
| 2  | -  | -   | -  | +   | 71.59      | +2.7    |
| 3  | -  | +   | +  | +   | 73.11      | +1.52   |
| 4  | -  | +   | +  | +   | 75.11      | +2.0    |
| 5  | +  | +   | +  | +   | 75.32      | +0.21   |

Table 8: The impact of training tricks to the accuracy of ISyNet-N0. ML denotes mutual learning [47]; RA denotes RandAugment [3]; LBN denotes Batch Normalization [14] after classifier’s fully connected layer; LT denotes number of training epochs, where '-' is 90 epochs and '+' is 550 epochs;