Computationally-Efficient Optimal Control of Cascaded Multilevel Inverters With Power Balance for Energy Storage Systems

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Abstract—This article proposes an optimal current control technique with switching event minimization for grid-active cascaded multilevel inverters (CMI) interfaced with battery energy storage sources. The proposed control scheme enables power-balancing functionality of battery cells, realizing optimal smart operation of CMI. Model predictive control (MPC) is known as a potential approach for multiobjective control schemes in single-loop manner for power electronics interfaces. However, MPC schemes suffer from high computational burden that is magnified in topologies like the CMI, which have a substantial number of redundant control actions. The proposed control scheme utilizes a dynamic lookup matrix as an internal optimizer tool. The redundant switching sequences are cycled to equalize the power drawn from the independent battery energy storage sources while achieving a minimum energy control. The theoretical analysis and experimental case studies verify robustness and computational efficiency of the proposed multicriteria optimal controller with similar objective tracking when compared to finite-set MPC.

Index Terms—Energy storage systems, grid-tied inverter, model predictive control (MPC), optimal control, smart inverter.

I. INTRODUCTION

With the sustained increase in renewable energy technology, energy storage systems are being considered to address the inherent drawbacks of renewable energy. Namely, the variability of renewables and its potential effect of grid stability and power quality at high penetration [1], [2]. A popular realization of energy storage systems is through the use of strings of battery modules in a cascaded topology, referred to as cascaded multilevel inverters (CMI). This topology consists of series-connected full-bridge inverters, which have a battery module connected to their dc link [3]–[5]. The CMI enables direct connection to medium and high-voltage grids without the use of transformers and without the necessity of acquiring semiconductors with high voltage-blocking capability [6], [7]. Additionally, the reduced harmonic content of the output voltage waveform reduces filter requirements. The same benefits apply for battery modules, which can operate at voltages far lower than the grid voltage.

However, the compound topology inherent to CMI tends to limit the range of control techniques that are feasible. Particularly, cost optimization-based control schemes such as model predictive control (MPC) lack feasibility for CMIs with a large number of voltage levels, as the optimization set is too large to run a practical sampling frequency of the digital controller. Nonetheless, MPC is often regarded as a control technique with generally fast dynamic response and easy inclusion of constraints and nonlinearities in the objective function. The subset of MPC known as finite-control set MPC, although perhaps the most intuitive solution, is the most computationally demanding subset. Whereas continuous-control set MPC includes offline optimization and online searching of the optimal action, finite-control set MPC schemes predict the behavior of a set of possible control actions and implements that which is most aligned with the reference. This is distinct in that a switching modulator is eliminated, yet the optimization is done online [8]. Within the subset of finite-control set MPC, a further distinction can be made based on the nature of the control set. Common in three-phase applications, MPC schemes which choose among a set of space vectors is referred to as an optimal space vector (OSV) control [9], [10], while the remainder evaluate a set of possible switching states; this is known as optimal switching sequence (OSS) finite-set MPC [11]. With the number of nonredundant space vectors in a converter smaller than its number of possible switching sequences, OSS-based MPC proves the most computationally demanding within MPC [8]. To mitigate the computational burden inherent to finite-set MPC, authors have suggested modified MPC schemes which...
reduce the optimization set based on the previous control action. For OSV MPC, this is done by considering only adjacent voltage vectors in $\alpha\beta$ frame, referred to as the nearest neighbor method [12]. A similar idea is proposed for OSS MPC of multilevel inverters by applying a voltage window [13] which is essentially the nearest neighbor method applied to a one-dimensional control set. However, both techniques reduce the control set, which can negatively affect dynamic performance. In [14]–[16], the next-state current is replaced with a reference current in the predictive equation, creating a reference output voltage (in the $\alpha\beta$ frame for a three-phase system). By creating a reference output voltage and considering the output voltage vectors time invariant, next-state predictions can be removed. Though this has been proposed for OSV MPC, eliminating the next-state prediction has yet to be proposed for OSS MPC, the most computationally demanding subset of MPC. Additionally, removing redundant switching sequences, as is done in OSV MPC, has undesirable consequences in applications with multiple power sources. Depending on the redundant switching sequences that are implemented by the converter, power can be unintentionally drawn at uneven rates from the sources [17]. For the application of grid-tied batteries, this will create a divergence in the state of charge among the battery modules.

This work aims to eliminate all aforementioned challenges of finite-set MPC. The presented control includes a method of optimization similar to finite-set model predictive current control. Specifically, the control exploits the fact that next-step current is affected only by output voltage. In doing so, current control is achieved with a control set that increases linearly with the number of H-bridges in the inverter, rather than increasing exponentially, as is seen in traditional finite-set MPC. This distinction creates a remarkable reduction in online computations, thus increasing achievable sampling frequency when compared to traditional finite-set MPC on a given control platform/embedded control system. The method of reducing the control set involves an objective function which includes time-invariant control actions, eliminating the next-state predictions, the “predictive element” of predictive control. Thus, the proposed control is referred to as an optimal control scheme, where optimal control is a superset of predictive control. Still, the control selects a specific switching sequence at each sampling instant, a distinction shared by finite-set MPC. Further, switching event minimization is achieved as a secondary objective. This is done offline, by computing the number of switching events between switching sequences during construction of the lookup matrix. A collection of switching sequences that achieve the optimal output voltage in minimal switching events is realized using a lookup matrix, where the previous switching sequence and optimal output voltage serve as the address for an optimal switching sequence (or list of switching sequences) within the matrix. The control rotates through the list of redundant optimal switching sequences at each call to its respective matrix address. This equalizes the time that each full-bridge implements a nonzero output voltage, which in turn equalizes the average power drawn from each isolated power source. This is particularly useful for grid-tied battery applications, as the control scheme supports equal state of charge for all batteries. By deriving current references according to an active and reactive power reference per phase, the power drawn is equalized not only for each source in a phase but for all sources in the three-phase system. This holds true even for phase-to-neutral grid voltage sags. This article is a post conference edition of [18], and includes a more in-depth theoretical analysis of the optimizing data structure, a computational comparison of the proposed control against finite-set model predictive control, and experimental verification of the proposed control scheme.

The remainder of this article is organized as follows. Section II explains the formulation of the optimal output voltage selection. Section III explains the structure of proposed lookup matrix, dimension of the lookup matrix, and the cycling of redundant states. Section IV compares proposed method with finite-set MPC. In Section V, the stability of the proposed control is analyzed using the Lyapunov stability criterion. In Section VI the proposed system is tested against transients in grid voltage to demonstrate the low voltage ride through (LVRT) operation capability. The control is also compared with a finite-set MPC scheme and a traditional, pulse-width modulation (PWM)-based control scheme. Finally, Section VII concludes this article.

II. SYSTEM DESCRIPTION

An overview of the topology and proposed control scheme is shown in Fig. 1. Each phase is controlled separately. This allows the optimization set to be reduced and allows the controller to respond to grid voltage imbalance. Without loss of generality, the control formulation is described for a single phase. The converter implements current control, but the current reference is generated from a desired active and reactive power injection. To implement instantaneous active and reactive power equations in single-phase, an orthogonal signal generator (OSG) is applied to the sensed phase voltages. This permits the use of active and reactive power equations in the rotating reference frame

$$\dot{P}_{k} = \frac{1}{2} (v_{d,k} i_{d,k} + v_{q,k} i_{q,k}), \dot{Q}_{k} = \frac{1}{2} (v_{q,k} i_{d,k} - v_{d,k} i_{q,k}),$$

where $v$ and $i$ are the grid phase voltage and current, respectively. A second-order generalized integrator-based OSG [19] creates

![Fig. 1. Proposed power electronics interface.](image-url)
the orthogonal voltage signal. The Park transform is applied to the original and quadrature phase voltages to produce $v_{d,k}$ and $v_{q,k}$. Solving the equations in (1) for the decoupled current components based on the desired active and reactive power injection (per-phase) is used to generate the reference current

$$i_{d,k}^* = \frac{2(P^* v_{d,k} + Q^* v_{q,k})}{v_{d,k}^2 + v_{q,k}^2}, i_{q,k}^* = \frac{2(P^* v_{q,k} - Q^* v_{d,k})}{v_{d,k}^2 + v_{q,k}^2}. \tag{2}$$

The asterisk denotes a reference. Thus, we have a desired reference current components which are transformed to a time-variant signal using the inverse Park transform

$$i_k^* = i_{d,k}^* \sin(\theta_k) + i_{q,k}^* \cos(\theta_k). \tag{3}$$

The phase angle of the grid voltage, $\theta_k$, is computed using a phase-locked loop which regulates the term $v_{q,k}$ to zero. The determination of the optimal control action is formulated by considering the ac KVL equation of the circuit

$$v_{\text{inv}} = Ri + L \frac{di}{dt} + v. \tag{4}$$

$v_{\text{inv}}$ is the voltage applied at the output of the inverter. $R$ and $L$ are the equivalent series resistance (ESR) and inductance of the output filter, respectively. The single prediction method which is proposed in [14] for controlling three-phase grid voltages in the $\alpha\beta$ frame, is modified to find a reference line-to-neutral voltage for each phase, next-state predictions for grid current as is the well-established predictive current control method. By discretizing the differential in (4) with the measured and reference current, the optimal output voltage is computed

$$v_{\text{inv},k}^* = v_k + R i_k + L(T_s)^{-1}[i_k^* - i_k]. \tag{5}$$

where $v_{\text{inv},k}^*$ is the optimal output voltage at discrete time instant $k$. In traditional finite-set MPC, the current in the next time instant is estimated for all control actions. With this technique, the output voltage that would produce the reference current in the next state is estimated, the benefit being that no prediction is necessary for the realizable output voltages.

The number of output voltage levels that a CMI can produce is $2M + 1$, where $M$ is the number of full-bridges in series. Considering the output voltage levels as the control set, the control set is now $[-M M], M \in \mathbb{Z}$. In this article, this set of integers is considered as the control set, called vector $M$. The output voltage to implement in the next time instant is computed as

$$M_k = \arg \min \left| M - \frac{v_{\text{inv},k}^*}{V_{\text{dc},k}} \right| \tag{6}$$

where $<V_{\text{dc},k}>$ is the average of the measured dc link voltages. It is assumed that the dc link voltages will be regulated to nearly equal values. By adjusting the control set to the optimal output voltage level $M_k$, a remarkable reduction in online computation has been achieved. For $N$ H-bridges in a CMI, there are $2N + 1$ voltage levels and $4^N$ unique switching sequences. A quantitative measure of increased computational efficiency is provided in Section IV. The following section will discuss how the lookup table is used to select a particular switching sequence from the optimal output voltage $M_k$.

III. MATRIX STRUCTURE AND OPERATION

In Section II, it was revealed how finite-set MPC can be adjusted into a computationally efficient optimal current control technique. Computational efficiency is claimed here because finite-set current control is enabled while replacing the original control set, which has an exponential relationship with the converter topology, to a control set with a linear relationship. In this section, the remaining problems with finite-set MPC discussed in the introduction are addressed. Namely, how the optimal output voltage level is translated to a specific switching sequence while minimizing switching events and addressing the issue of power imbalance.

For the remainder of the article, it will be useful to reference particular switching sequences (a specific combination of logic applied to each gate in the CMI). However, with the 9-level CMI, there exist 256 unique switching sequences, which is far too many to define explicitly in a table. Thus, a nomenclature is defined here to make referenced switching sequences deducible: The gate logic value of the top switch in each inverter leg ($S_a, S_b, ... , S_h$) will be concatenated. Consider this sequence of logical values a binary number. Now, convert this value to its decimal equivalent and add one. Adding one simply allows the names of switching sequences to start at switching sequence one rather than switching sequence zero. An example of this nomenclature is provided in Fig. 2. Note that the value of the lower switches in each leg ($S_{an}, S_{bn}, ... , S_{hn}$) need not be considered when defining switching sequences, as they will be the logical opposite of the upper switches in their respective legs (e.g., if $S_a$ is one/closed, $S_{an}$ must be zero/open).

Offline switching event minimization can be achieved because the number of switching events between two distinct switching sequences can be determined a priori. For example, it is known that, to transition from switching sequence 256 to switching sequence 128, two switching events must occur (the gate logic of $S_a$ and $S_{an}$ must invert). Further, the output voltage level of a switching sequence can be determined as

$$M = \sum_{i=a,c,e,g} S_i - \sum_{x=b,d,f,h} S_x \tag{7}$$

where the value of a switch $S_x$ is denoted as one for ON/closed and zero for OFF/open. Thus, given the deducibility of a switching
sequence’s output voltage level and the number of switching events required to transition to different switching sequences, it is concluded that switching event minimization can be achieved offline. What remains to be determined is how the number of switching events between switching sequences should affect the switching sequence selection. In traditional finite-set MPC, this is decided by factoring each cost term in the objective function with a weight factor. This will be detailed in Section IV. In this work, switching event minimization is considered a secondary objective to current control. This means that, once an optimal output voltage level \( M_k \) is determined, the set of switching sequences to consider in the next state is reduced to those which produce the optimal output voltage level. It is called a secondary objective because, although it can be locally minimized, the number of switching events will never alter the selected output voltage level \( M_k \). For this reason, the control is considered a hierarchical optimal control. Current is globally optimized, while the number of switching events is minimized locally in the remaining control set.

Although switching events can be computed offline, as discussed previously, the control requires knowledge of the previously selected switching sequence \( (s_k) \) for switching event minimization. Additionally, the selected switching sequence must produce the optimal output voltage level \( M_k \). Thus, the control requires an indication of \( s_k \) (previously chosen switching sequence) and \( M_k \) (optimal output voltage level) to locate the optimal switching sequence. At this point, it is worthwhile to note that both \( s_k \) and \( M_k \) fall within a finite range of discrete variables (integers from 1 to 256 and from \(-4\) to \(4\), respectively). This is the intuition for the operation of the lookup matrix. A lookup matrix (or two-dimensional array) is apt for this problem, as we can input the optimal output voltage level \( M_k \) and the previous switching sequence \( s_k \) and retrieve the optimal switching sequence. This switching sequence would implement \( M_k \) in minimal switching events. This can be achieved by indicating \( M_k \) via lookup matrix row number, and \( s_k \) via column number, with \( s_k + 1 \) indicated by the value within that row–column combination, or matrix address. Thus, with the lookup matrix, switching event minimization is achieved without online computations.

The final issue of finite-set MPC to be addressed is power imbalance among the isolated voltage sources. First, the cause of this issue must be explained. To do so, consider a time instant \( k \) in which switching sequence 1 is implemented; all upper switches \((S_u, S_{u+1}, \ldots, S_n)\) are set to logic-low, and the resultant inverter output voltage is zero. During current optimization at time instant \( k \), \( M_k \) is computed as one, meaning the controller has determined that an output voltage of \(+V_{DC}\) will bring the current closest to \(i^*\). This requires a change in the output voltage level of \(+1\). To change the voltage level by one with minimal switching events, the logic gates of one leg must be inverted. In this scenario, inverting the gate logic of any of the left-most full-bridge legs will create the appropriate output voltage level (inverting the logic of \(S_u/S_{u+1}, S_u/S_{u+2}, S_u/S_{u+3}, \) or \(S_u/S_{u+4}\)). Thus, using the switching sequence nomenclature previously established, switching sequences 3, 9, 33, and 129, are optimal and redundant. That is, each produce the optimal output voltage level \( M_k \) in minimal switching events. Note here that these switching sequences each apply positive voltage across a different full-bridge output. In turn, power will be drawn from a different battery module for each switching sequence. Thus, by ignoring all but one of these redundant switching sequences, power will be drawn exclusively from one of the battery modules. If one redundant sequence is chosen at each address of the lookup matrix, this will result in unequal power draw from the batteries. In finite-set MPC, only one of these switching sequences will be selected in this scenario. Traditionally, it is the first-seen optimal switching sequence. Thus, in this scenario, finite-set MPC would only select switching sequence 3, which draws power from full-bridge 4’s battery module. Since the control actions of a finite-set MPC are nondeterministic, it cannot be said with certainty how exactly power draw will vary among the isolated battery modules. Even if the sequences are carefully selected such that nonzero voltage is applied across each full-bridge an equal number of times in the lookup table, the frequency in which addresses are called will vary, thus unequal power draw will remain inevitable. Thus the power imbalance that occurs from finite-set MPC in this topology is caused by the existence of redundant optimal switching sequences that are ignored during optimization. Fig. 3 shows the number of redundant optimal switching sequences exist at each matrix address. The number of redundant switching sequences tends to increase as the magnitude of \(M_k\) decreases. This is because each \(H\)-bridge has two switching sequences that produce zero output voltage. Oppositely, it is noted that for all addresses at row one and row nine, there is only one switching sequence; just one switching sequence can achieve an output voltage level of four (switching sequence 171), and likewise for negative-four (switching sequence 86). Additionally, it is intuitive that if the output voltage level of \(s_k\) is equal to \(M_k\), then there will only be one optimal switching sequence, and \(s_k + 1\) will be set to \(s_k\). That is, if \(M_k = M_{k-1}\), then no switching events must occur.

The power imbalance among the isolated voltage sources is mitigated by implementing all redundant switching sequences over time. This can be done by implementing a multidimensional array. This is simply a matrix with nonunitary depth; this data structure can also be considered a 3-D matrix.
The row and columns work exactly as previously described with the lookup table, except the additional layers will be used for selection of redundant switching sequences. Fig. 4 illustrates the concept more clearly. Each matrix address has a list of redundant optimal switching sequences. The first two layers decide which of the redundant switching sequences are in queue for selection. Layer one of each matrix address is an integer equal to the length of the list in its associated stack. Layer two acts as a pointer, containing the location of the next switching sequence to implement when the associated matrix address is called. Fig. 5 explains exactly how the matrix is used. Once \( M_k \) is computed, it is converted to the associated row number by adding five (row number one is associated with \( M_k \) equal to negative four). The previous switching sequence determines the column number. Then, the layer number (\( z \)-coordinate) that will be implemented is determined by layer two, making layer two referred to as the pointer layer. The value within the layer number being pointed to is the selected switching sequence according to the previously defined nomenclature. The value within layer two of the selected matrix address is then incremented. This will ensure that, the next time this matrix address is called, a new redundant switching sequence will be selected. This is visualized in block six of the algorithm. The value in layer two was \( n \), thus the switching sequence that was selected was contained in cell \( n \) of the stack. Then, layer two points to the cell above it (cell \( n + 1 \)) for the next time this address is called. The conditional block that follows is related to what was shown in Fig. 3. That is, these lists of redundant switching sequences vary in length. However, the matrix must have a fixed length, width, and depth. Thus, the depth of the matrix must be large enough to contain the longest list (a list of seventy switching sequences). However, most lists are not this long. Pointing to layer numbers that extend beyond the lists must be prevented. This is the purpose of layer one, which specifies the length of the list at its address. If the value of layer two points beyond the limits of the list, the value is reset to three, which contains the first switching sequence in the list. Thus, the control rotates through the list at each address. Here, it must be acknowledged that using a multidimensional array as described is not the most memory-efficient solution, since many of the matrix elements contain null blocks, or places in memory that have been allocated but will never be written to or read from. Null blocks are necessary to use a multidimensional array as the data structure. The memory-efficient solution is to convert the matrix into a group of lists. This way, each stack would have length equal to the number of redundant sequences at its address, removing the null blocks. Fig. 6 demonstrates how changing the algorithm to implement a group of lists would reduce the necessary random access memory (RAM). Note that, for CMI topologies with more than four full-bridges, the variables must be defined using two-byte variables (presumably 16-bit unsigned integers). This is because the number of possible switching sequences exceeds 256, which is the total number of values that can be distinguished in a single byte. Despite the memory that can be saved by converting to a group of lists, the control technique is described using a multidimensional array, to aid in visualizing the control technique and to avoid making the concept more convoluted. The algorithm described can be easily modified to the memory-efficient implementation.

IV. COMPUTATIONAL COMPARISON WITH FINITE-SET MPC

To better comprehend the reduction in on-line computations to reach an appropriate control action with the proposed control technique, the operations are compared against finite-set MPC.
First, the finite-set MPC of which the proposed control is compared against must be defined.

The finite-set MPC that is being considered will contain the same objectives as the proposed control: Current control with minimal switching events. The reference current is developed exactly as it is for the proposed control using (1)–(3), and thus the techniques will only differ in how the control action is decided. In traditional MPC, each control action is individually considered, meaning a prediction will be computed for each possible switching sequence in finite-set MPC. The next-state prediction is derived from (4), of which the differential term is discretized using the Forward Euler approximation. Solving for the next-state prediction leads to

$$i_{k+1} = (1 - RT_s(L)^{-1})i + T_s(L)^{-1}(v_{inv,k+1} - v_k)$$  (8)

where $i_{k+1}$ is a vector of next-state current predictions according to each possible switching sequence, and $v_{inv,k+1}$ is a vector of the output voltage that would results from each possible switching sequence, which is defined by

$$v_{inv,k+1} = V_{DC1}(S_{a,k+1} - S_{b,k+1}) + V_{DC2}(S_{c,k+1} - S_{d,k+1}) + V_{DC3}(S_{e,k+1} - S_{f,k+1}) + V_{DC4}(S_{g,k+1} - S_{h,k+1})$$  (9)

where the gate signals are defined for all 256 switching sequences. Further, since switching event minimization is another control objective, defined as the changes in gate logic between possible switching sequences and the previously selected switching sequence. This will be included in the overall cost function $J$, which is defined as

$$J = |i_{k+1} - i^*| + \lambda \times 2 \sum_{i=a,b,h,...,h} |S_{i,k+1} - S_{i,k}|.$$  (10)

The factor of two accounts for the lower switches’ gate signals which must change along with their respective upper switches (if $S_a$ changes, so must $S_{an}$). The $\lambda$ is referred to as a weight factor, and its magnitude is chosen according to the desired effect of switching events on the control action. Note here that there are only nine unique next-state current predictions: One for each voltage level. Thus, switching event minimization can be considered among a single next-state current prediction by making $\lambda$ sufficiently small. So long as the cost of switching events does not exceed the differences between next-state current predictions, the optimization will work similarly to the proposed optimal control scheme, where switching event minimization acts as a secondary control objective. The control action which minimizes $J$ will be chosen for time $k+1$

$$s_{k+1} = \arg \min(J).$$  (11)

With both control techniques detailed, Table I summarizes the number of floating-point operations needed for one iteration of the finite-set MPC and the proposed control, as a function of $H$: The number of full-bridges in the CMI. The column labeled Value Comparisons is related to the size of the control set of which each control minimizes its objective loss. Fig. 7 is a logarithmic plot which visualizes how the total computations increase with the number of full-bridges in the CMI topology. The critical difference in the number of operations is that the proposed control compares voltage levels in real time, while the finite-set MPC compares switching sequences in real time. The number of voltage levels increases linearly with the number of full-bridges [6], while the number of switching sequences increases exponentially. Here it is evident how standard finite-set MPC loses its feasibility as the CMI includes more full-bridges. Note that the total computations should not necessarily be considered directly proportional to the execution time nor to potential sampling frequency of the controller. The speed of each type of floating-point operation will vary according to the selected processor, and the speed of one iteration will depend on the selected processor(s) and number of processors used in the CMI’s embedded system. Thus, a theoretical discussion on explicit improvements in runtime is avoided. However, an empirical metric is available, as both control techniques are implemented using the dSPACE CP1103 rapid control prototyping hardware. The graphical user interface is ControlDesk. Upon loading the control algorithms into the hardware, ControlDesk offers a metric called turnaround time. This metric represents the time taken to execute a single iteration of the control algorithm, providing insight into the real-time sampling frequency that can be used without causing overrun. However, the turnaround time is not suitable for comparing the two control algorithms alone, as the controller’s analog-to-digital converters and reference signal generation creates substantial overhead on total execution time. It is possible to measure the execution time of an individual subsystem. This metric will be distinguished with the label control execution time. Both metrics are measured. Upon
predictive control takes nearly 28 μs to compute, while the proposed control finds the optimal switching sequence in under 5.6 μs, making the proposed control roughly five times faster for this topology.

V. STABILITY ANALYSIS

System stability is verified using the Lyapunov stability criterion. Like the control itself, the system stability is analyzed per-phase. The next-state converter output voltage \( v_{\text{inv},k+1} \) necessary for optimal tracking is represented by

\[
 v_{\text{inv},k+1} = v_{\text{inv},k} + \theta_k
\]

where \( v_{\text{inv},k+1} \) is not bolded in this case, as it represents the output voltage selected by the controller, rather than the nine-element array of output voltages \( v_{\text{inv},k+1} \). \( \theta_k \) is the distance from \( v_{\text{inv},k} \) that is minimized during the selection of output voltages, but results from the discrete output voltage levels that can be achieved from the CMI. This error is referred to as the output quantization error. We define a value \( \vartheta \) as a positive real number greater than 1 for this topology.

\[
 \vartheta \equiv \frac{l s}{221e}
\]

Table II. Controller Speed Comparison With MPC

| Timing on CP1103 | Finite-Set MPC | Proposed Control |
|------------------|---------------|------------------|
| Controller Execution Time (Average / Standard Deviation) | 27.95 μs / 128.7 ns | 5.578 μs / 26.09 ns |
| Turnaround Time (Average / Standard Deviation) | 35.87 μs / 158.0 ns | 13.57 μs / 99.22 ns |

The output voltage that guarantees a negative time derivative of \( L \) is given as

\[
 v_{\text{inv},k+1} = L s^{-1} i_{k+1} + i_k \left[ R - L s^{-1} \right] + v.
\]

From (17), Lyapunov stability is met if the system meets these criteria

\[
 L(i_{\varepsilon,k}) \geq D_1 |i_{\varepsilon,k}|^n, \forall i_{\varepsilon,k} \in \Upsilon
\]

\[
 L(i_{\varepsilon,k+1}) \geq D_2 |i_{\varepsilon,k+1}|^n, \forall i_{\varepsilon,k} \in \Gamma
\]

\[
 L(i_{\varepsilon,k}) - L(i_{\varepsilon,k+1}) < -D_3 |i_{\varepsilon,k+1}|^n - D_4
\]

\[
 D_1, D_2, D_3, D_4 \in \mathbb{R}^+, \eta \geq 1
\]

\[
 \Gamma \subset \Upsilon \subset \mathbb{R}^+. \quad (18)
\]

Substituting (16) into (18)

\[
 (T_s L^{-1}) \bar{\dot{i}}^2 - i_{\varepsilon,k}^2 \geq L(i_{\varepsilon,k}). \quad (19)
\]

Further, the error of the output current converges to the space \( \psi \) defined as

\[
 \psi = \left\{ ||i_{\varepsilon,k}||^2 \leq T_s L^{-1} \bar{\dot{i}} \right\}. \quad (20)
\]

From (20)

\[
 D_1 = D_2 = 2, D_3 = 1, D_4 = (T_s L^{-1})^2. \quad (21)
\]

Thus, the controlled parameters are bounded, and the system satisfies the Lyapunov stability criterion.

VI. RESULTS AND DISCUSSION

The proposed control scheme is validated and compared with finite-set MPC experimentally for one phase. Fig. 8 provides an overview of the hardware setup. Table III presents system parameters, both for the proposed optimal control and the comparable finite-set MPC scheme. The plots that follow are exported measurements from the dSPACE CP1103 discussed in Section IV. However, for the controller to successfully execute in real time, the sampling rate of the exported data is reduced by a factor of four. In other words, the control samples at 50 kHz, but the exported data are sampled at 12.5 kHz. A bidirectional grid emulator is used for testing the control under changes in
TABLE III
SYSTEM PARAMETERS FOR HARDWARE EXPERIMENT

| Parameter                                      | Value  |
|------------------------------------------------|--------|
| $P^*$ (Single-Phase Active Power Reference)    | 1 kW   |
| $Q^*$ (normal grid condition)                  | 0 VAR  |
| $Q^*$ (grid voltage sag, LVRT mode)            | 250 VAR|
| DC Link Voltages                               | 80V    |
| $f_0$ (proposed control scheme)                | 50kHz  |
| $f_0$ (comparison with MPC)                    | 25kHz  |
| Filter Inductance                              | 2.5mH  |
| Filter ESR                                     | 0.2Ω   |
| Imposed dead-time                              | 1μs    |

grid condition. First, the proposed control is shown for changes in grid voltage and power reference. Then, it is compared with finite-set MPC to demonstrate the comparable tracking capability and balancing of power draw from each H-bridge in the topology.

The control’s response to dips in grid voltage are shown in Fig. 9, in which a ten percent grid voltage is induced at $t_1$. To retain 1-kW power injection, the active current reference is increased, as evidenced by the increase in grid current amplitude. Fig. 10 shows the system response to the grid voltage returning to normal condition, where the control responds by reducing $i^*$ from about 13 to around 11.5 A.

Next, a more severe dip in grid voltage is considered to demonstrate the LVRT operation capability of the proposed controller. Fig. 11 shows a twenty percent sag in grid voltage at $t_3$. For more substantial grid voltage sags, the control is programmed to inject 250V AR. Thus, $i^*_q$ is stepped up from zero to about 14.7 A. Meanwhile, $i^*_d$ also increases to about 14.7 A to retain 1-kW power injection during the voltage sag, which is the requirement for constant active power LVRT operation strategy [20]. This leads to a notable increase in grid current amplitude following $t_3$. Reactive power injection is evidenced by the waveform of the injected grid current following the grid voltage. In Fig. 12, the grid voltage returns to healthy condition at $t_4$. The control responds quickly by reducing $i^*_q$ to zero and returning $i^*_d$ to 11.7 A, as evidenced both by the reduction in grid current amplitude and immediate phase alignment of the grid voltage and injected grid current.

As discussed previously, the power reference is considered a fixed value, or determined from a higher-level control. A step change in the active power reference of the CMI is considered to emulate such changes. Fig. 13 demonstrates the response of the system to a reduction in active power reference. At $t_5$, $P^*$ is reduced from 1 to 0.5 kW. The CMI quickly tracks the new current reference, which has a new active current amplitude of 5.88 A. In Fig. 14, the active power reference returns to 1 kW at $t_6$. Again, the control tracks the new, increased current reference.

The proposed control is now compared, both to a traditional finite-set MPC and a traditional PWM-based proportional-resonant (PR) current control. The modulation technique is referred to as subharmonic multilevel PWM [21]. This switching
scheme employs an individual carrier wave for each H-bridge in the CMI. The fundamental frequency of the carrier waves is set to 10 kHz. The proportional and resonant gains of the control were manually tuned to 0.6 and 24.5, respectively, by evaluating the tradeoff between steady-state power quality and transient settling time. The traditional PWM control scheme is illustrated in Fig. 15. For the topology presented, the finite-set MPC is unable to sample at 50 kHz. Table II from Section IV showed that the turnaround time for the MPC is about 36 $\mu$s. To avoid any over-run errors, the sampling frequency of the MPC had to be reduced to 25 kHz (sampled every 40 $\mu$s). Further, so the comparison is not biased, we are including results in which the proposed optimal control is also sampled at 25 kHz, rather than the 50 kHz previously presented. An increase in current distortion is apparent, as a result of the reduced sampling rate, both for the finite-set MPC and the proposed control. Additionally, the exported measurement data from the CP1103 experience a similar reduction in sampling rate, to 6.25 kHz. For consistency, the proportional resonant controller was also sampled at 50 kHz and exported at 6.25 kHz, though this did not affect the power quality; the switching frequency and sampling frequency do not hold a direct relationship in traditional PWM-based switching schemes. It is worthwhile to note that the current references are computed identically for each control scheme, and thus the contrasts in performance are strictly a result of the controllers themselves. The control schemes are tested at steady state and for a step change in active power reference. Fig. 16 presents the finite-set MPC. The control is able to track the current reference, and can quickly adjust the reduction in active power reference at $t_7$. However, Fig. 16(b) shows the power drawn from each battery module for the finite-set MPC, and it is revealed that the power draw characteristics are drastically varied among the cells. As discussed previously, the upper switches in full-bridge one ($S_a, S_b$) are the most significant bits, and the upper switches in full-bridge two ($S_g, S_h$) are the least significant bits. Thus, switching sequences when $S_a$ and $S_b$ are switched ON tend to be considered less often, tending toward lesser power draw. It was also mentioned in Section III that this cannot be avoided, even when reducing the control set for finite-set MPC, because the frequency in which each voltage level is selected cannot be easily predicted or controlled.

In Fig. 17(a), the same transient is applied to the traditional PR current control at $t_8$. From the current, the power quality appears higher than that of the finite-set MPC scheme. This is because the carrier waves remain fixed at 10 kHz. The modulation signal from the PR current control determines which H-bridge is switching, and with each H-bridge switching roughly one-fourth of the period of the modulation signal, it is concluded that the average switching frequency is about 2.5 kHz for each H-bridge. However, it is noted that, unlike the finite-set MPC, the PR control does not reach the new steady-state amplitude.
during the step change in $P^{*}$ than that of cells two and three. This behavior is maintained for about 2 grid cycles. Further, the output current is misaligned with the grid voltage following $t_{6}$, and this continues for about 3.5 grid cycles as it is shown in Fig. 17. Thus, the traditional PR-based control scheme suffers from slower transient response when compared to the MPC scheme. The settling time can be improved with increasing the proportional and resonant gains of the control but will negatively affect steady-state power quality, demonstrating an inherent tradeoff when tuning this control. In Fig. 17(b), the power draw characteristics of each H-bridge are shown. There are two distinct power draw levels. Specifically, cells one and four exhibit similar power draw, while cells two and three are roughly the same. However, power draw is not equal for each H-bridge. This can be explained by looking back at the carrier waves in Fig. 15. Because the amplitude of the modulation signal is less than the sum of the amplitude of the two carrier wave levels, cells one and four switch for a smaller fraction of the modulation cycle. Thus, their power draw is less than that of cells two and three. This behavior is maintained during the step change in $P^{*}$ following $t_{6}$. From this, it can be determined that cells one and four will not draw any power from their sources if the amplitude of the modulation signal is less than that of the carrier waves’, as the respective H-bridges will not be switched. Likewise, equal power draw can only be achieved when the modulation index equals one. Thus, power draw inequality from the isolated voltage sources is inherent to this switching scheme for the presented topology. Finally, it is noted that the power draw for this switching scheme does not contain substantial low-frequency content that is visible in the finite-set MPC scheme. This is because the finite-set MPC and the proposed control both contain variable switching frequency, inducing similar frequency content upon the power draw.

In Fig. 18(a), the same transient as was shown in Fig. 13 is shown again, only this time at the reduced sampling rate. At $t_{9}$, the power reference is reduced from 1 kW to 500 W. The current tracking capability is similar to the finite-set MPC. The new current amplitude is tracked in a few controller sampling instants. Additionally, Fig. 18(b) shows the power draw characteristics of each battery module. A much more equalized power draw among the cells is noted, which occurs both before and after a reduction in the active power reference. Slight inequalities in the average power draw is noted. However, this is likely caused by slight mismatch in the dc voltages and the reduction in sampling rate. Because there is no bias among redundant switching sequences, this difference in average power draw will reduce as the measured time interval increases.

The comparison of the proposed control with standard finite-set MPC and a traditional PR current control with subharmonic multilevel PWM switching is summarized in Table IV. The results of the proposed control are shown for the 100-kHz sampling frequency, rather than the 50-kHz sampling that was shown in the direct comparison. Unlike the traditional finite-set MPC, the proposed control was able to sample at 100 kHz, resulting in a negligible increase in settling time for the presented active power step change, but a notable reduction in total harmonic distortion (THD). This is because the faster achievable sampling enabled a higher average switching frequency. Additionally, the distinction in power draw is dramatically reduced with respect to the other two control schemes presented. The PR current controller had lower power draw distinction than the finite-set MPC and higher power quality but suffered from slower dynamic response. Finally, it is worthwhile to mention that the finite-set MPC and the PR control both require tuning effort, unlike the proposed control. Namely, the PR controller requires tuning the proportional and resonant gains, and the MPC requires tuning the weight factor ratio. The proposed control contains an inherently hierarchical objective tracking structure, and thus does not require tuning.

### VII. Conclusion

An optimal current control technique for grid-connected CMI was proposed which addresses the major setbacks of finite-set MPC paradigm for the proposed application. The proposed control achieves equivalent current tracking as is attained using finite-set MPC, but sheds substantial computation associated with next-state current predictions. Further, by invoking time-invariant parameters in the topology, online computations become a linear function of the number of full-bridges, rather than an exponential function seen by the comparable finite-set MPC. This reduced the control’s execution time by a factor of five, allowing the proposed control scheme to run at twice the sampling rate of the finite-set MPC scheme in experimentation. The control also implements switching event minimization as a secondary. Further, the lookup matrix contains a third dimension, which contains a variable list of redundant optimal switching sequences at each address of the lookup matrix. This eliminates

| Control Technique | Current THD | Settling time ($P^{*}$ reduction) | Average Power Draw Difference |
|-------------------|-------------|----------------------------------|------------------------------|
| Proposed Control  | 2.17%       | ~40µs                            | ~10.3W                       |
| Traditional FS- MPC | 5.28%     | ~80µs                            | ~184W                        |
| PR current control | 3.91%       | ~58µs                            | ~130W                        |
the unintentional bias towards redundant optimal switching sequences that is seen in finite-set MPC. By removing this bias, the power drawn from the battery modules is balanced on average. The proposed control was tested experimentally and shown to provide superior power quality, power balance, and dynamic performance when compared to a finite-set predictive control and a proportional-resonant current control with PWM switching.

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