CapStore: Energy-Efficient Design and Management of the On-Chip Memory for CapsuleNet Inference Accelerators

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ABSTRACT

Deep Neural Networks (DNNs) have been established as the state-of-the-art algorithm for advanced machine learning applications. Recently, CapsuleNets have improved the generalization ability, as compared to DNNs, due to their multi-dimensional capsules. However, they pose high computational and memory requirements, which makes energy-efficient inference a challenging task. In this paper, we perform an extensive analysis to demonstrate their key limitations due to intense memory accesses and large on-chip memory requirements. To enable efficient CapsuleNet inference accelerators, we propose a specialized on-chip memory hierarchy which minimizes the off-chip memory accesses, while efficiently feeding the data to the accelerator. We analyze the on-chip memory requirements for each memory component of the architecture. By leveraging this analysis, we propose a methodology to explore different on-chip memory designs and a power-gating technique to further reduce the energy consumption, depending upon the utilization across different operations of a CapsuleNet. Our memory designs can significantly reduce the energy consumption of the on-chip memory by up to 86%, when compared to a state-of-the-art memory design. Since the power consumption of the memory elements is the major contributor in the power breakdown of the CapsuleNet accelerator, as we will also show in our analyses, the proposed memory design can effectively reduce the overall energy consumption of the complete CapsuleNet accelerator architecture.

1 INTRODUCTION

Deep Neural Networks (DNNs) have shown promising results for various machine learning (ML)-based applications, e.g., image and video processing, automotive, medicine, and finance, but at a cost of high computational complexity, energy consumption, and memory requirements. To reduce the energy and latency, many researchers have designed specialized DNN inference accelerators [1] [2] [3] [4] [6] [10] [12]. Recently, Sabour and Hinton et al. [14] investigated the CapsuleNets, a particular type of DNNs which has multi-dimensional capsules instead of uni-dimensional neurons (as used in traditional DNNs). The ability to encapsulate hierarchical information of different features (position, orientation, scaling) in a single capsule allows to achieve high accuracy in computer vision applications (e.g., MNIST [8] handwritten digits classification).

To tackle the challenge of performing efficiently CapsuleNet inference, systolic array-based hardware accelerators can be employed for inference hardware architectures. Recently, Marchisio et al. [11] proposed a systolic array-based hardware accelerator to improve the performance efficiency of CapsuleNet inference, compared to GPUs. This work primarily focused on the computational parts using an array of accelerators, which optimizes the routing-by-agreement algorithm, but ignores the memory architecture design and management for such hardware accelerators, which is a crucial component when considering energy reductions of the overall hardware design. Our experimental analysis in Section 3 illustrates that the memory energy for both the on-chip and off-chip contributes to 96% of the total energy consumption. Therefore, only employing an accelerator-based processing array is not sufficient to achieve a high energy efficiency. It is crucial to invest further effort to analyze the possibilities and opportunities to reduce the total/overall memory energy. The assumptions made by many DNN accelerator architectures (like [6] and [12]) and the recent CapsuleNet accelerator [11] of having a huge on-chip memory is not applicable in embedded applications (e.g., deployed in the IoT-edge devices), where the hardware resources are constrained and memory resources are scarce. Hence, there is a significant need to investigate energy-efficient design and management of on-chip memory hierarchy for CapsuleNet hardware architectures to enable their embedded inference. To understand the memory design challenges and the optimization potential for CapsuleNet accelerator-based architectures, we perform a detailed analysis of the memory requirements in terms of size, bandwidth and accesses for every stage of the CapsuleNet inference.

Research Challenges: Traditional memory hierarchies of DNN accelerators are composed by an off-chip DRAM and an on-chip SRAM. An efficient design of a memory hierarchy requires exploration of several design parameters (like size, banks, partitions, etc.) for multiple levels, affecting each other, which makes it a very challenging problem. Intensive off-chip memory accesses reduce the energy efficiency and performance due to high access latency, while a large on-chip size may have a significant impact on the area and the leakage power. On the other hand, a large on-chip memory enhances high throughput computations, and a limited on-chip memory size is required to efficiently reduce the energy consumption. Further improvements can be achieved by systematic partitioning and power-gating (i.e., using sleep transistors [13] to switch-off the power supply of the correspondent memory sectors) under different memory usage scenarios. Note, the power-gating technique comes with the cost of wakeup energy and latency overhead. However, their usage is beneficial to significantly reduce the leakage power. To overcome the above challenges, a key information to consider could be the application-specific knowledge (i.e., different processing aspects of CapsuleNet inference). Such an application-aware design of memory hierarchy and the power management of the on-chip memory may bear the potential to provide significant energy savings compared to the traditional memory designs, while keeping high throughput, as we will demonstrate in this paper. The overview of our work is depicted in Figure 1, where the blue-colored boxes represent our novel contributions, as discussed below.

Our Novel Contributions:

(1) Memory Analysis (Section 3): we perform an extensive analysis of the memory requirements (size, accesses), performance and energy, for every operation of the CapsuleNet inference.
2 BACKGROUND: CAPSULENETS

The work by Hinton et al. [5] showed the potential of CapsuleNets, particular types of DNNs where the basic units across the layers are capsules, i.e., multi-dimensional elements. The differences between CapsuleNets and DNNs are described in Section 2.1. Following the work of [14], which showed the efficient routing-by-agreement algorithm, CapsuleNets had become even more attractive for the community, thus demanding an effort from the hardware side to support such required processing. For this purpose, recently an accelerator for CapsuleNet inference was proposed in the work of [11], whose architecture is described in Section 2.2.

2.1 Inference on CapsuleNets vs. DNNs

As compared to traditional DNNs, a CapsuleNet has:

- **Capsule:** a multi-dimensional neuron, which is able to encapsulate hierarchical information of multiple features (position, scale, orientation, etc.).

- **Routing-by-agreement:** a multi-dimensional non-linear function, which efficiently fit for the prediction vector.

- **Squash activation function:** an algorithm to learn the connections between two subsequent Capsule layers. It is an iterative algorithm, which iterates over a defined number of routing iterations.

The last point is a very challenging aspect from the hardware perspective, as it means that there is a feedback loop in the inference path (highlighted by the red-colored arrows in Figure 2). This property implies that it is more difficult to massively parallelize and pipeline the accelerator to compute such operations.

2.2 CapsuleNet Accelerator

Figure 3a shows the architecture of the specialized accelerator for CapsuleNet inference [11]. The core of the processing unit is the systolic array (16x16 Processing Elements), for efficiently parallelizing the computation. Systolic array-based architectures have been also used for specialized DNN accelerators [3][6]. The accumulator stores the partial sums and computes further internal additions when required. The activation unit computes the activation functions needed. The dedicated connections between accelerator and memories allow data and weight reuse, properties which are particularly effective for the routing-by-agreement computation.

In the original paper [11], all the memory elements are on-chip, forming an overall size of 8MB. Since for memory constrained systems such size can potentially exceed the limits, we decided to break the memory hierarchy into an on-chip SRAM, followed by an off-chip DRAM, as shown in the blue-colored boxes and green-colored boxes of Figure 3b, respectively. This solution can potentially generalize the problem for different applications and more complex CapsuleNet architectures. For this purpose, we adopt...
the following policies to define the sizes and the communications between off-chip and on-chip memories:

- Minimize the off-chip memory accesses.
- Keep the same latency and throughput, as compared to having all the memory on-chip.
- Minimize the on-chip memory size.

The aforementioned constraints and limitations motivate our analysis of the resource requirements, which is presented in Section 3.

3 ANALYSIS: CAPSULENET RESOURCE REQUIREMENTS

We perform an extensive analysis to identify the resource requirements for computing the inference on CapsuleNets. As a case study, we investigate the CapsuleNet architecture described by [14], which performs MNIST [8] classification. First, in Section 3.1 we analyze the performance and the on-chip memory requirements for every operation of the CapsuleNet inference. Then, we analyze the on-chip read and write accesses for every operation of the inference. Finally, in Section 3.2 we compute the energy breakdown, between the accelerator and the components of the memory.

3.1 Performance, Memory Usage and Accesses

Considering the design policies discussed in Section 2.2, we analyze the on-chip memory requirements for each operation of the CapsuleNet inference. The results are shown in Figure 4a. The overall size is determined by the operation which requires the largest amount of memory (PrimaryCaps layer in our case). For this configuration, the on-chip memory is shared between data, weight and accumulator items. The dashed line represents the maximum value, and for each operation we display the percentage of utilization.

Figure 4b reports the number of clock cycles required to compute each operation of the CapsuleNet inference. Note, the last two operations (Sum+Squash and Update+Sum) are executed at each routing iteration (i.e., 3 times in our example). If we combine the results of Figures 4a and 4b, we notice that, potentially, a significant amount of leakage energy can be saved by power-gating part of the on-chip memory, when the utilization is below 100%. This idea will be described and implemented in Section 4.3.

Figure 4c presents the memory requirements for each memory component (data memory, weight memory and accumulators). Such analysis enables the design space exploration of an application-aware memory architecture (CapStore), which explores the possibility to handling separate the memory components of the on-chip memory. It will be discussed in Section 4.2. The accumulator size is higher than data and weight memory for each operation, because it must store the temporary partial sums of different output feature maps. Data and weight memory requirements, however, vary significantly across different operations. In the first two layers, the weight memory requirements are quite low as compared to the other stages, because the architecture can efficiently employ weight reuse in convolutional networks. In the ClassCaps layer, however, the data memory is low, because data reuse is efficient. Weight reuse is also more efficient in the last two operations, as compared to the third one.

Figures 4d and 4e show the read and write accesses, respectively, for each operation of the inference, i.e., C1, PC and CC-FC. These values are needed to compute the energy consumptions of the memories in the following sections. Note, the off-chip accesses are not reported in the graphs for space reasons. Their values can be easily computed using the Equations (1) and (2), which are valid for the first three operations. In the last two operations, the off-chip memory is not accessed: all the values that have to be saved during the routing-by-assignment are stored on-chip.

\[
(*\text{Reads}_{\text{off-chip}}) = (*\text{Writes}_{\text{weight-mem}} + *\text{Writes}_{\text{data-mem}}) \quad (1)
\]

\[
(*\text{Writes}_{\text{off-chip}}) = (*\text{Reads}_{\text{data-mem}}) \quad (2)
\]

3.2 Energy Breakdown

In this stage, we compute the energy consumption of the complete architecture. We develop two different versions:

(a) Fig. 3a: accelerator (composed by systolic array, activation unit and control unit), on-chip buffers (data buffer, weight buffer and accumulator) and on-chip memory (data memory
and weight memory). This is the architecture proposed in [11], where the on-chip memory has size equal to 8MB.
(b) Fig. 3b: accelerator, on-chip and off-chip memories. The sizes are derived from the requirements analyzed in Section 3.1.

The energy breakdowns are shown in Figure 5. Note, the results relative to the accelerator and the on-chip buffers have been obtained by synthesizing the CapsuleNet accelerator of [11] in a 32nm CMOS technology, while on-chip and off-chip memory values have been extracted using CACTI-P [9].

This analysis shows that, by organizing the memory in a different hierarchy, we can already save 66% of the total energy, as compared to the state-of-the-art architecture [11]. Moreover, since the on-chip memory consumes 45% of the total energy, an application-aware power management (discussed in Section 4.3) can potentially have a significant impact on the overall energy consumption.

3.3 Key Observations from our Analyses

From the analyses performed in Sections 3.1 and 3.2, we derive the following key observations:

- Most of the energy is consumed by the (on-chip and off-chip) memory, as compared to the computational array of the accelerator.
- An application-aware memory hierarchy, composed by an on-chip SRAM and an off-chip DRAM, can save up to 66% of energy, without compromising the throughput, as compared to having a fully on-chip memory organization.
- The utilization of the on-chip memory is variable, depending upon the operation of the CapsuleNet inference. Thus, applying power-gating to the non utilized sectors can potentially further reduce the energy consumption.
- Partitioning the on-chip memory into separated chips (for data, weight and accumulator) can be beneficial for storing values and feeding the accelerator in an efficient way.

4 CAPSTORE: ON-CHIP MEMORY DESIGN AND MANAGEMENT

4.1 Memory Models

In this section, we present the memory models used in our work. Our reference design of the CapStore on-chip memory is shown in Figure 6. The on-chip memory is connected to the CapsuleNet accelerator and to the off-chip memory through dedicated bus lines. We design our CapStore memory as partitioned into N banks, and each bank into S equally-sized sectors. All the sectors with the same index, across different banks, are connected through a power-gating circuitry to the same sleep transistor. This implies that each sleep transistor is responsible for power-gating N sectors, one for each bank. The sleep transistors are connected to our application-aware power management unit, which gives the control signals to handle ON ↔ OFF transitions. Since we perform power-gating on the on-chip SRAM and we do not need data retention, our model consists of just two sleep modes, i.e., ON (full swing voltage) and OFF (zero voltage). All the intermediate sleep modes (data retentive with reduced voltage) has not been considered in our model, since they are not useful for our scenarios. The transitions between sleep modes come at a cost of a certain wakeup energy and latency overhead. However, the usage of power-gating leverages the tradeoff between wakeup overhead and static (leakage) power savings. Note, our memory model can be generalized for each memory size and parallelism, including multi-port memories.

We design 3 different on-chip memory architectures:

(a) Fig. 7a - Shared Multi-Port Memory (SMP): the on-chip memory is shared across a multi-port memory, which has 3 ports (for weight memory, data memory and accumulator).
(b) Fig. 7b - Separated Memory (SEP): weight memory, data memory and accumulator are separate memories.
(c) Fig. 7c - Hybrid Memory (HY): a combination of a shared multi-port and three separated memories.

4.2 Application-Aware Design Space Exploration

Having defined the memory models, we now design the number of banks (N), the number of sectors (S) per bank, the organization, the parallelism and the power-gating management. In this section we cover all the aforementioned aspects, except for the power-gating, which will be discussed in Section 4.3.

The knowledge of the application plays a key role for designing the on-chip memory. We explore different configurations of the memory architecture and, for each case, we compute area and energy consumption (see Section 5). Different levels of abstraction of application-aware knowledge are employed. The derivations are explained in the following considerations.

- **Architecture**: the parallelism of the systolic array of the CapsuleNet architecture (16x16 processing elements) suggests to employ 16 banks.
- **Overall utilization**: the memory requirements (worst case of Figure 4a) suggest the size of the SMP memory.
- **Utilization for different elements**: the worst case memory requirements of Figure 4c and the organization into different blocks (data memory, weight memory and accumulator) suggest the sizes of the SEP memory. The minimum utilization of the memory in Figure 4c suggests the sizes of the separated memories in the HY architecture. The size of the shared multi-port memory of the HY architecture is suggested by the difference between the worst case utilization and the sum of the sizes of the separated memories.
- **Utilization across different layers**: Figures 4a and 4c suggest the sector size, in order to apply power-gating to the unused sectors of the memory.

We design six different versions of the CapStore on-chip memory, one for each memory architecture presented in Figure 7, with or without enabling power-gating (denoted by the prefix -PG). The different architecture organizations are reported in Table 1. Note, when power-gating is not enabled, the memory architectures are slightly different: the hardware overhead composed by the sleep transistors and the power management unit (PMU) is missing. Therefore, for such architectures, each bank contains only 1 sector.
4.3 Application-Aware Power Management

Our application-aware PMU is responsible to give the control signals to the sleep transistors, according to the utilization of the memory, derived from the Figures 4a and 4c. The additional hardware circuitry, apart from the PMU itself, is represented by the sleep transistors. A simple schematic showing how one sleep transistor is connected to its relative sectors of the memory is depicted in Figure 8. The sleep request is followed by the acknowledge signal, forming a 2-way handshake protocol. The timing diagram of a complete sleep cycle \((\text{ON} \rightarrow \text{OFF} \rightarrow \text{ON})\) is shown in Figure 9.

5 CAPSTORE ARCHITECTURE EVALUATION

5.1 Area and Energy Consumption of the On-Chip Memory

For each memory architecture organization explored in Section 4, we evaluate the area and the energy consumption (see Table 2), using CACTI-P [9] simulation tool. Figure 10a presents the area breakdown of the different memory components of the CapStore on-chip memory. We notice that, while the organizations SEP and PG-SEP have higher memory size, compared to the other four architectures, the area occupied is significantly lower. This effect is due to having single-port memories instead of shared multi-ports. A shared 3-port memory, indeed, occupies a high area due to the overhead of the interconnections. Moreover, the power-gating circuitry (mainly based on the sleep transistors) is significant in terms of area, as each sleep transistor size depends upon the number of memory cells controlled by itself.

In the following paragraph, we show the energy consumption for different architectures of the CapStore on-chip memory, analyzed from different perspectives. Figure 10b presents the energy breakdown of the different memory components of the on-chip memory. It is evident that the architectures SEP and PG-SEP are more energy efficient than the others, due to having single-ports. Moreover, the energy consumption can be reduced by applying power-gating. The advantage of using such technique is more significant for the SEP architecture. The reason of this behavior can be explained by considering that the ratio between the ON sectors and the complete memory is higher, as compared to SMP and HY. Figure 10c shows the contributions of the dynamic and static energy, for the different architectures. It highlights that (1) moving from SMP to SEP, we are able to significantly reduce the dynamic energy and (2) moving from SEP to PG-SEP, we can significantly reduce the static energy. Besides this, we noticed that the wakeup energy overhead is negligible, because the transitions of the memory sectors between OFF and ON are very less frequent (they can only happen when we switch from an operation to the following one), as compared to the periods of time when the states are stable. Figure 10d shows the energy breakdown for the different components of the CapsuleNet inference: the proportions of the energy consumed remains approximately similar across the different architectures. We notice that
Table 2: Area and energy consumption for different CapStore on-chip memory architectures.

|                | Area [mm²] | Energy [mJ] |
|----------------|------------|-------------|
| All On-Chip    | 18.486     | 38.6733     |
| SMP            | 11.423     | -           |
| PG-SMP         | 34.4412    | -           |
| SEP            | -          | 0.108034    |
| PG-SEP         | -          | 0.514265    |
| HY             | 7.1157     | 3.4014      |
| PG-HY          | 19.427     | 3.8613      |

Figure 10: Area and energy results for the different architecture organizations of the CapStore on-chip memory. (a) Area and (b) energy consumption for different memory components. (c) Energy consumption, showing dynamic and static contributions. (d) Energy consumption, for different operations of the CapsuleNet Inference.

Figure 11: (a) Energy and (b) area breakdown of the complete architecture of the accelerator.

5.2 Energy and Area of our Complete CapsuleNet Accelerator Architecture

Based on the evaluations achieved in Section 5.1, we select the CapStore PG-SEP architecture, as it is the most efficient organization in terms of energy consumption, among the six architectures proposed in the exploration. We synthesize the complete architecture of the CapsuleNet accelerator in a 32nm CMOS technology library, using the ASIC design flow with the Synopsys Design Compiler, and we measure the area and energy consumption. Figure 11 shows the energy and the area breakdowns. For both metrics, the contribution of the accelerator to the total value is very limited (4 to 5%), while the main contribution is due to the off-chip memory. Compared to the initial version, discussed in Section 3.2 version (a), the total energy is reduced by 78% and the area by 25%. Compared to version (b), the on-chip energy is reduced by 86%, the on-chip area by 47%. As a consequence, the total energy is reduced by 46% and the total area by 25%.

6 CONCLUSIONS

In this work, after an initial analysis showing the performance and hardware requirements for CapsuleNet inference, we identified that a significant amount of energy can be saved by designing a specialized memory hierarchy (combination of off-chip and on-chip memories). To achieve high efficiency, we designed the on-chip memory in a way to minimize the off-chip memory accesses and maintaining high throughput. We explored different memory hierarchies and we design the CapStore, a specialized on-chip memory for CapsuleNet accelerators, with its own application-aware power management unit to further reduce the leakage power. As per our knowledge, this paper proposes the first on-chip memory design performing the inference on CapsuleNets. Our work opens up interesting ideas for energy-efficient memory design, even beyond CapsuleNet inference applications.

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