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ABSTRACT
Spin transfer magnetoresistive random access memory (STT-MRAM) shows potential applications with the properties of non-volatility, low power consumption and high write/read speed. With the maturity of the STT-MRAM process, it has gradually entered the mass production stage. Reliability will be an important factor limiting the development of this device. Error correction technology is highly required to be developed on this specific memory circuit. In this paper, a combination of low density parity check (LDPC) is used on STT-MRAM, in which the encoding constructs a no 4-girth check matrix. In its fulfillment, the decoded method combines soft decision and hard decision. The simulation results demonstrate that the LDPC shows promising application scenario for STT-MRAM error correction, especially for large-capacity storage arrays.

I. INTRODUCTION
Spin-transfer torque magnetic random access memory (STT-MRAM) is a new generation non-volatile memory. It is regarded as the most popular memory because of its fast reading/writing speed and “unlimited” endurance. With the cutting-edge development of semiconductor technology, the memory capacity can be increased into large volume by increasing the cell density. However, at the same time, the error rate of MRAM has gradually become a critical issue for the data reliability. This deteriorates the reliability of the overall circuit. Well known, error-correcting codes (ECC) has adopted in the memory systems, such as static random access memory (SRAM), dynamic random access memory (DRAM), and Flash, which can reduce the error rate and improve the data reliability. For the emerging STT-MRAM, the error correction mechanism is investigated intensely by several groups all over the world. For example, Brandon Del Bel et al. employed multi-bit error correction with DRAM-style refreshing to mitigate errors and provides a methodology for determining the optimal level of correction. Xiaochen Guo et al. proposed a new error protection mechanism-Sanitizer, which improves performance by 1.22× and reduces end-to-end system energy by 22%. Yang et al. studied the Bose-Chaudhuri-Hocquenghem (BCH) error correction mechanism for STT-MRAM.

As the storage capacity of STT-MRAM increases, the error rate gradually increases. Based on the incumbent error correction algorithm, Low Density Parity Check (LDPC) code plays an important role in the error correction field of Flash. The performance of the LDPC code not only approaches the Shannon limit, but also has strong error correction capability, low decoding complexity, fast decoded speed (parallel decoded), and code rate adaptation. So far, no application of LDPC method on STT-MRAM is conducted. In this paper, as far as authors know, for the first time, the trial of the application of the error correction method of LDPC on the high-density STT-MRAM is made. The mechanism related to occurring of the STT-MRAM reading and writing error is introduced. Several different error correction methods are compared in terms of the error rate.

II. ERROR CORRECTION MECHANISM OF STT-MRAM
The memory cell of STT-MRAM is composed of a magnetic tunnel junction (MTJ) and a n-type metal oxide semiconductor
The information is recorded by the high and low resistance states of the MTJ device. There are two states of the MTJ device, the parallel state (with low resistance) and the anti-parallel state (with high resistance). The resistance can be changed by the flowing direction of the current, in which the current changes the magnetization state of the magnetic layer. The writing error of the MTJ is usually occurs when the pulse width is less than the switch time or the low stress voltage.\(^{9}\)

The stored data is judged by the magnitude of the current flowing through the MTJ during the read operation of the MTJ. When the read current is greater than the threshold current, the data “1” is read. On the contrary, when the read current is less than the threshold current, the data “0” is read. Based on the above principle, during the reading, there are two kinds of read error. The first one is named the data bit flip (1 → 0/0 → 1) caused by the excessive current. The other one is caused by the overlap of ‘read 1’ current and ‘read 0’ current. Figure 1(a) shows the write failure occurring when the pulse width or voltage is too small. Figure 1(b) shows the read failure when there is an overlap between the read 1 current and the read 0 current. In STT-MRAM arrays, a single cell’s read and write failures will cause the failing of the whole row or the whole column.\(^{10}\) It is necessary to design the error correction circuit in the array of STT-MRAM to improve the overall reliability.

As the density of STT-MRAM increases to 4 Gbit,\(^{11}\) the read and write error rates are also rising dramatically. Not only the external signal mentioned in the previous section affects the bit error rate of the MRAM, but also the magnetic interference caused by the higher density deteriorates the reliability of the reading and the writing. In this way, an effective error correcting approach is highly required in the STT-MRAM design. The error correcting code can effectively reduce the bit error and improve its data reliability.

Generally, the error correction codes used in the memories include Hamming code, Bose Chaudhuri Hocquenghem code (BCH),\(^{7}\) Reed Solomon code (RS),\(^{12}\) and LDPC.\(^{13}\) Hamming code has high transmission efficiency and simple code circuit. However, it can only be used in the single bit correction. RS code is suitable for the correction of the continuous-bit distribution errors. BCH shows good error correction capability. However, it cannot meet the error correction requirements of STT-MRAM with the high-capacity and the high-density storage arrays. The LDPC code has excellent characteristics close to Shannon’s tolerance. It is suitable for the memory correction with high volume and high density. In this paper, the LDPC approach is used on the high-density STT-MRAM to investigate its feasibility in the correction properties.

### III. DESIGN OF LDPC IN STT-MRAM MEMORY

The chip architecture of STT-MRAM memory is designed and fulfilled, as shown in Fig. 2. The pins of the STT-MRAM memory, including the chip enable, the read/write enable, the address latch and the command latch enable, are the inputs for the control signal ports and are controlled by I/O. The block diagram is made up of the basic logic control, the address, the sense amplifier, the ECC and

![Diagram](https://example.com/diagram.png)
After the calculation, it is forwarded to the connected information node. During each iteration, the information is transmitted to the next level child node. As shown in Fig. 3, a closed loop is composed by the check nodes, the edges, and the information nodes. The number of the edges experienced by the loop is called the length of the loop, and the length of the loop with the shortest loop length in all loops is called the girth, which is an important indicator for constructing LDPC codes. If there is no girth in the Tanner graph, the information node is independent of each other. There is no information feedback. The data sent from the check node would pass through a loop and then return to itself if there is a girth in the Tanner graph. The more frequent the information feedback when the girth is shorter. The traditional LDPC adopts a method of randomly generating code words. The short loop is easily generated for high code rates and long code word. The “4-girth” is shown in Fig. 3. Therefore, the minimum ring should be avoided when generate the check matrix.

In this paper, the approach of quasi cyclic-low density parity check (QC-LDPC) is used to avoid the appearance of a minimum loop. Its check matrix is composed of a series of sparse sub-matrices of the same size. The QC-LDPC code is a subclass of the LDPC code, which simplifies the coded modes by sacrificing certain randomness. The QC-LDPC code divides the general LDPC code into blocks so that each sub-block has a cyclic shift characteristic. The shift register can be used to achieve its encoding, which greatly reduces the encoding time and coding complexity. Not only preserves the sparse and random characteristics of the LDPC code, but also greatly simplifies the complexity of compiled code.

Based on the above analysis, the cyclic sub-matrix has the following characteristics: I. Square matrix. II. Any rows on the matrix are obtained by cyclically shifting the previous row one bit to the right. In addition, the first row of the matrix is cyclically shifted by the last row.

A QC-LDPC check matrix without four-girth is constructed by using a method from the index matrix. The shift factor index matrix is as following:

$$S = \begin{bmatrix} 1 & a & \ldots & a^{t-1} \\ b & ab & \ldots & a^{t-1}b \\ \vdots & \vdots & \ddots & \vdots \\ b^{t-1} & ab^{t-1} & \ldots & a^{t-1}b^{t-1} \end{bmatrix},$$ (1)

Given that the dimension $L$ of the cyclic permutation matrix is a prime number, $a, b \in (2, \ldots, L-1)$, and the following conditions are met:

$$(b^f - 1) \cdot (a^d - 1) + 0 \mod L, 1 \leq d \leq t - 1, 1 \leq f \leq c - 1,$$ (2)

The decoded method of the LDPC includes soft decision and hard decision (bit flipping). Two decision decoded methods have their own advantages and disadvantages. For example, for the soft decision error correction, its capability is strong, but the operation is complicated. On the contrary, for the hard decision error correction, its capability is poor, but its parallel structure can greatly improve the decoding rate. The implementation of the hardware circuit of the hard decision is simpler than that of the soft decision. Based on the large storage density of STT-MRAM and the requirement on the fast read speed, the hard-decision decoding method is selected to meet the reading requirements of the storage array. The decoded method in this paper uses the improved bit flipping, which
uses the soft message of the channel to weight the bit flipping criterion. This method is able to improve the decoded performance without additional decoding complexity.

To simulate the effect of the error correction method proposed in the paper, the Additive White Gaussian Noise (AWGN) signal is added to the channel. Binary Phase Shift Keying (BPSK) modulation and demodulation method is used. The block diagram of the ECC approach for the encoded and decoded process is as shown in Fig. 2. The $E_b/N_0$ (dB) is named the signal to noise ratio, and the noise is given by Additive White Gaussian Noise. $E_b$ represents the energy per bit of signal, taken as unit energy. $N_0$ represents noise energy.

Based on the above analysis, we set $a=5$, $b=2$ to compile and decode the code word. The simulation results are shown in Fig. 4. The QC-LDPC without 4-girth can significantly reduce the bit error rate of the code word. With the increasing of the signal-to-noise ratio (SNR), the more pronounced the BER decreases compare to the BCH and RS.

IV. CONCLUSION

In this paper, the LDPC coding approach is used in STT-MRAM with high volume and high density. Compared with the other coding approaches, including Hamming code, RS, BCH, the LDPC approach is suitable for the error correction on the high-density STT-MRAM. The characteristics of LDPC is close to the Shannon limit. The no 4-grith search matrix is used to construct the check matrix. Simulation results shows that the BER is reduced by comparison with the other codes. The weight bit flip hard decoding method can maintain high error correction characteristics at the expense of small space and rate.

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