Here, a broadband electrostatic discharge (ESD) protection circuit using area-efficient multi-layer helical inductors is presented. The proposed concept was verified in a 0.18 μm 1P6M CMOS process, and the circuit area is only 54 × 63 μm². The measurement results show that a bandwidth of around 30 GHz is achieved, and the impedance matching is kept under –20 dB up to 40 GHz. The measured TLP and VF-TLP currents reach 2.19 and 5.80 A, respectively, which indicates a good ESD robustness.

Introduction: Electrostatic discharge (ESD) events would cause fatal damage to electronic parts especially to integrated circuits (ICs). Hence, the ESD protection circuits are usually indispensable for IC products. However, adding ESD protection devices or circuits will definitely introduce parasitics and probably degrade the frequency performance of the ICs, which makes ESD protection a critical issue for the design of high-speed and radio frequency (RF) ICs.

The dual-diode circuit is one of the most commonly used protection solutions, with one diode connected to VDD and the other to VSS [1]. The junction capacitances of the diodes are the main source of parasitics. There are mainly two ways to lower the impact of parasitic capacitance, and one of them is by reducing the parasitic capacitance. The stacked diode structure is a simple method to reduce effective capacitance, but at the same time it increases on-resistance [2]. Silicon controlled rectifiers (SCRs) manifest themselves as low capacitance, low device area and high ESD robustness, and attract much research [3]. However, the parasitic capacitance still has a notable negative impact as the frequency increases. The other way is to compensate the impact of the parasitic capacitance by employing inductors to form LC resonators [4], distribution-like structures [5] or T-coils [6-9]. The T-coils are often used to extend the bandwidth [10], and are first introduced in [6] to build broadband ESD protection circuits. Moreover, the T-coils also provide good impedance matching. In [7], a distributed diode design is employed into the T-coil to further improve the frequency and ESD performance. However, the on-chip planar inductors always occupy a large chip area. In [8], an asymmetric T-diode design is given, but only the top two metal layers are exploited for the inductor design, which did not make full use of the process potential. In [9], the top five metal layers are exploited, but no ESD test data are given.

In this letter, we follow the circuit structure in [7], but instead of a planar one we employ a multi-layer helical inductor to build a compact broadband ESD protection circuit.

Circuit description: Figure 1 shows the schematic diagram of the proposed circuit. The 3D structure of the multi-layer helical inductor is also shown in the figure. There is only one turn in each metal layer, which leads to a high quality factor due to the lack of the proximity effects between the parallel metal paths in the same metal layer [11]. As a T-coil, the helical inductor has three ports including Port A at the top layer, Port B at the bottom layer and Port X at the middle point along the path from Port A to Port B. Port A is tied to the input port of the circuit, and Port B is tied to the termination resistor R₁ in order to lower the impact of the inductor-to-substrate parasitics on the input port. Port X is connected to the internal core circuit. The inductor and C₁ work as low impedance paths for low and high frequencies, respectively, which helps to produce a broadband impedance matching.

The diodes are distributed among Port A, Port B and Port X. The parasitic junction capacitances of the diodes and the input capacitance of the internal core circuit have significant impacts on the frequency characteristics of the circuit. But, if designed properly, the transfer function, which is defined as Vᵢ/Vᵢᵣ, can show broadband characteristics. The power rail ESD clamp circuit is necessary in forming complete ESD current discharging paths, including positive-to-VDD (PD), negative-to-VDD (ND), positive-to-VSS (PS) and negative-to-VSS (NS).

Test chip: We verified the proposed concept by using a 0.18 μm 1P6M CMOS process. D₁ and D₂ are implemented with P+/N-well and N+P-sub diodes, respectively. The total width of diode D₁ (D₂) is 60 μm, and distributes at Port A, Port B and Port X as listed in Table 1. An nmos transistor M₀ with a size of W/L = 80 μm/0.18 μm is employed to emulate the core circuit to be protected as shown in Figure 2 [12]. An additional version of the test circuit implementing the conventional dual-diode circuit was also fabricated. The total width of the diodes and the size of M₀ are the same as above. With proper voltage bias, M₀ equivalents to a loading capacitance of 167 fF, and the parasitic capacitances of D₁ and D₂ are 36 and 40 fF respectively. The multi-layer helical inductor uses 5 metal layers, from M2 to M6. The inner diameter and the path width are 25 and 5 μm, respectively. The total inductance of the inductor is about 0.7. In consideration of the parasitic capacitance between the stacked metal layers, we remove C₁ for the final version of the test circuit, which simplifies the circuit and reduces the area.

Figure 3 shows the chip micrograph of the test circuits. The total area of the proposed circuit, including the helical inductor, all the diodes and the termination resistor, is 54 × 63 μm².

Table 1. ESD circuits parameters and performance summary

| Dual-diode | Proposed |
|------------|----------|
| Inductor   | N/A      | 5-layer helical inductor |
| D₁, D₂, D₃ | 60 μm    | 24 μm               |
| D₁, D₂, D₃ | N/A      | 12 μm               |
| Circuit area | N/A | 54 × 63 μm² |
| Input matching | –7.6 dB | @ 30 GHz  |
| TLP I₂     | PD: 2.13A; PS: 2.23A | PD: 2.25A; PS: 2.19A |
| VF-TLP I₂  | PD: 7.54A; PS: 7.44A | PD: 6.13A; PS: 5.80A |

Fig. 1 Schematic diagram of the proposed broadband ESD protection circuit using multi-layer helical inductors

Fig. 2 Core circuit emulator for verification
ESD protection circuit

Chip micrograph of the proposed and the conventional dual-diode ESD protection circuit

Fig. 3 Chip micrograph of the proposed and the conventional dual-diode ESD protection circuit

Z with 1) is characterized by the reflection coefficient Γ, which is calculated with Z₁₁, as follows:

\[ \Gamma = \frac{Z_{11} - 50}{Z_{11} + 50} \]

The transfer function \( V_x/I_n \) can be directly obtained from \( Z_{11} \).

Figures 5 and 6 show the measured TLP and VF-TLP I–V curves, respectively. Both PD and PS results are given. The snapback behaviour in the PS curves attributes to the turning on of the power rail ESD clamp circuit. The secondary breakdown current (I₂₁) of each curve is extracted and listed in Table 1. It is found that D₂₁ burns down and the metal over it gets fused for the proposed circuit. Though the T-coil circuit actually shows a lower current handling ability than the conventional dual-diode circuit in VF-TLP test, it still provides good ESD robustness.

Compared with the corresponding parameters from [7], it worth noting that the area of the proposed circuit is only 42% as that in [7], which is \( 85 \times 95 \mu m^2 \).

Conclusion: A compact broadband ESD protection circuit using multilayer helical inductor is proposed, which occupies a much smaller chip area compared to the prior art which uses a planar inductor. Meanwhile, it provides ~30 GHz bandwidth and good ESD robustness, which make it suitable for the design of high speed and broadband circuits.

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