Failure Analysis of a Chip Damaged by Electro-Static Discharge

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Abstract — A process of failure analysis of a COMS chip damaged by Electro-Static Discharge (ESD) is presented. The method of the thermal image was used to locate the failure spot. To find out the root of the failure, the circuit principle and the layout of the chip were analyzed, and it was found that the layout design was not unreasonable. An ESD test was carried out to confirm the analysis. This work has reference significance for the failure analysis and reliability improvement of the integrated circuit product.

1. INTRODUCTION
Electro-Static Discharge (ESD) is a common factor that leads to the failure of the integrated circuit (IC), and has become a big problem for the reliability of the IC product [1-5]. The static electricity is everywhere during the manufacture, testing, packaging, and usage of the IC. When the ESD reaches to a certain degree, it can easily damage the IC. It was reported that about 40% of the failure of IC products is caused by ESD [2]. Therefore, failure analysis is fundamental and invaluable to the design and development methodology of ESD-robust IC products [4].

For a faulty chip, failure analysis needs to determine its failure location and find out its failure cause. For some ESD-damaged cases, the failure can be located by an optical microscope as there is commonly a breakdown trace on the surface [6-8]. But when the electrostatic potential is relatively low, it may lead to the damage inside the IC which will complicate the failure location. Besides, how to figure out the failure cause is not easy, especially for the ESD-induced damage. One has to combine the specific circuit principle to analyze the failure mechanism.

In this paper, using electrostatic testing and thermal imaging, we locate and analyze an ESD-induced failure of a CMOS chip. This work can provide a reference for the failure analysis and optimization design of the IC product.

2. FAILURE PHENOMENON AND LOCATION
The failure event occurred on eight chips fabricated using the CMOS process. This is a negative pressure reference chip which is powered by a single power supply (VEE) of -5V. When working in the supply voltage, It was found that the negative power supply current far exceeded the standard value of 5 mA. Table 1 shows the current of the qualified chip and the eight faulty chips. For a qualified sample,
the current should be less than 1mA. However, the current of faulty chips fluctuates between 12.84mA and 78.10mA, which is obviously abnormal.

| Sample  | negative power supply current(mA) |
|---------|----------------------------------|
| Qualified | 0.98                             |
| Failed 1# | 19.44                            |
| Failed 2# | 78.10                            |
| Failed 3# | 70.92                            |
| Failed 4# | 75.72                            |
| Failed 5# | 75.75                            |
| Failed 6# | 15.15                            |
| Failed 7# | 12.84                            |
| Failed 8# | 73.87                            |

To get a more detailed condition of the faulty chip, we further tested the characteristics of each port. The diode characteristics between the ports of the eight faulty chips was tested, and it was found that the diode characteristics between the VEE port and the GND port of the eight faulty products was all abnormal at 1.09V, while the comparison of the qualified samples was 1.43V. In addition, we further tested the I-V characteristics between VEE port and GND port. Fig.1 gives the comparison of I-V characteristics between the qualified chip and a faulty chip. The gate voltage of the qualified chip is about 0.7V, while the faulty chip is less than 0.7V. So, the faulty chip has abnormal diode characteristics between the VEE port and the GND port.

![Figure 1. Comparison of the I-V characteristics between a faulty chip and a standard chip](image)

Based on the aforementioned tests, the faulty product has abnormal diode characteristics between the VEE port and the GND port, and electric parameter test performance for negative power supply current exceeds.

To find the failure location, we first tried to examine the eight chips using the optical microscope. Fig.2 gives an example of the optical image of the faulty chip. It can be seen from Fig.2 that nothing abnormal can be found from the surface as there was no obvious burnt-out trace. And all eight chips had the same surface and showed no signs of burns. Since the visual inspection method doesn’t work for the failure location, the thermal imaging is applied to the eight chips, and Fig.3 shows an example. Through the thermal image, a bright spot can be observed at the lower-left corner, and such a similar
bright spot exists in all the eight faulty chips. It is can be inferred from the thermal image that the failure occurs there.

Figure 2. The optical image of a faulty chip

Figure 3. Thermal image of a faulty chip

3. FAILURE ANALYSIS

3.1 Working principle
Though we found the failure location, the failure cause is not clear. To figure out the failure cause, it is necessary to study the circuit principle of this chip in the first step.
This CMOS chip is a negative pressure reference chip, and the circuit diagram of its output unit is shown in Fig. 4. This chip is powered by a single power supply (VEE) of -5V, and including the input stage, the reference, the switch, and the operational amplifier and the output stage. By comparing the thermal image and the layout of the chip, we confirmed the location of the bright spot is where the penultimate NMOS tube (N1 tube) stands. The abnormal increase of the negative power supply current of the chips is determined by the penultimate NMOS tube (N1 tube).

3.2 Reason analysis

Through the analysis of the circuit principle, we confirmed that the N1 tube is the root of this failure. It may be caused by either the manufacture process of the product or the interference of external electrostatic stress.

1) The internal reasons

Generally, the chip will burn out if the internal design and manufacture process of the chip are defective.

This batch of chips is processed by the standard process and its Process Control Monitor (PCM) parameter was checked without any exception. The damaged NMOS tube in Fig. 4 is a standard device fabricated by this process. Besides, the limit operating voltage of this chip designed by Process Design Kit (PDK) is -8V, while the actual operating voltage is -5V. The limit operating voltage of the device provided by the process PDK is shown in table 2. It can be seen from table 2 that the NMOS tube has a large margin in device selection. The supply voltage of this chip is less than 0.7 times of the maximum voltage of the device. According to GJB/Z 35-93, the device supply voltage has realized the Class I derating. In other words, the internal design and manufacture process of the chips are normal. Therefore, it is possible to exclude the manufacture process of the product.

| Device name | actual operating voltage (V) | limit operating voltage (V) |
|-------------|-----------------------------|----------------------------|
| pmos        | -5                          | -8                         |
| nmos        | 5                           | 8                          |
After reviewing the layout structure of the damaged NMOS tube of the chip (Fig.5), it was found that the layout index of the layout structure of the NMOS device is about 20 and the gate width is 0.5 μm. Traditionally, an IC which takes the electrostatic protection into account requires a grid index of 8 to 10 and a grid width of 40 to 60 μm [5]. So, we preliminarily determined that electrical stress may cause uneven gate current distribution, which makes the structure prone to damage.

2) External static stress

According to the circuit diagram of the output unit of the chip (Fig. 4), output port has ESD protection structure shown in Fig. 4 which are the same with other ports. According to the specification of the chip, its electrostatic capacity can reach 500V.

According to the circuit diagram of the output unit of the chip (Fig. 4), when the device is subjected to external a certain degree electrostatic stress (>500V), the electrostatic pulse time is extremely short (about 100nS). Due to the large area of the output N2 and P2 tubes, the parasitic capacitance is large. The large capacitance will store a large number of static charges. When the static charge discharges, due to the coupling effect, a large electrostatic pulse will pass through the N2 and P2 tubes and act on the front-end N1 and P1 tubes. At the same time, because the layout area of the N1 tube is smaller than that of the P1 tube, N1 tube would be more susceptible to ESD stress.

To confirm our analysis, we conducted the ESD test. Three qualified samples were selected for the HBM ESD test [2]. The applied voltage increased from 100V to 700V by a step of 100V. The test result shows in table 3, the negative power supply current increases abnormally to more than 12mA when the voltage reaches 700V. In addition, we chose one faulty chip to test the IV curve between VEE port and GND port, shown in Fig 6. It was found that the negative power supply current far exceeded the standard value, and the diode opening voltage is less than 0.7V, which are the same with faulty product.

| sample  | negative power supply current(mA) |
|---------|----------------------------------|
| Qualified product | 0.98 |
| Failed 1# | 18.96 |
| Failed 2# | 15.19 |
| Failed 3# | 12.88 |

Then, we checked the thermal images of the samples after the 700V ESD test. We chosed one faulty chip to test the thermal imaging as shown in Fig.7. The failure location is consistent with that of the faulty chips, a bright spot can be observed at the lower-left corner, indicating the electrostatic stress can cause similar failure.
This experiment result proves that the ESD-resistant ability of the N1 tube is relatively weaker than other tubes. Therefore, it is determined that external ESD stress will cause damage to the N1 tube, resulting in an increase in the negative power supply current of the product.

4. CONCLUSION
Many factors may lead to the failure of an IC chip, and failure analysis plays an important role in improving the reliability of the IC product. In this paper, failure analysis was done with the help of the thermal image to find out the failure spot. It is found that the fundamental reason for the failure of the CMOS chip lies in the ESD. For COMS chips, gate index, grid width, and the layout spacing [9] have great effects on the ESD robustness. One should pay attention to ESD robustness design from the perspective of the layout of the IC.
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