An all-digital phase-locked loop with a PGTA-based TDC and a 0.6-V DCO

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Abstract: An all-digitally phase-locked loop (ADPLL) with a pipeline time-to-digital converter (TDC) is proposed in this paper. The TDC employs a programmable-gain time amplifier (PGTA) to achieve two-step time quantization. A compensator is used to correct the gain error of the PGTA. The low-voltage DCO uses current-reuse structure to achieve lower and use bridging-capacitance technique to achieve high frequency resolution. The proposed design is validated by the ADPLL fabricated in the 65-nm CMOS technology. The measurement results show that the in-band and out-band phase noises are $-90 \text{ dBc/Hz@10 kHz}$ offset and $-130 \text{ dBc/Hz@1 MHz}$ offset, respectively. The RMS and peak-peak jitter are 1.24 ps and 8.65 ps respectively.

Keywords: all digitally phase-locked loop, time-to-digital converter, programmable-gain time amplifier, current-reuse

Classification: Integrated circuits

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1 Introduction

The last decade has witnessed a transition from the analog to the digital implementation of the phase-locked loops (PLLs) which are important building blocks of the transceivers and systems on chip (SoCs). Compared with their analog counterparts, the all-digital PLLs (ADPLLs) exhibit better adaptability to the deep submicrometer technologies, have higher noise immunity, smaller area due to the usage of a digital loop filter, and greater programmability.

As the key modules of the ADPLLs, the time-to-digital converters (TDCs) influence the in-band phase noise. As analyzed in [1], the in-band phase noise caused by the quantization effect in a TDC is given by

\[
\mathcal{L} = \frac{(2\pi t_{\text{LSB}})^2 N_{\text{div}} f_{\text{DCO}}}{12}
\]

where \(t_{\text{LSB}}\) is the resolution of a TDC, \(N_{\text{div}}\) is the dividing ratio of a divider, and \(f_{\text{DCO}}\) is the output frequency of a digital controlled oscillator (DCO). To reach the performance of the counterparts in the analog PLLs, i.e., the phase detectors and charge pumps, the TDCs have been widely researched over the past decade. A flash TDC [2] has the simplest structure, but its resolution is limited by the gate class. A \(\Delta\Sigma\) TDC [3, 4] can achieve noise shaping, but the power dissipation is relatively high. A SAR TDC [5] has a simple structure and a relatively low power but suffers from a low speed. A stochastic TDC [6] has high resolution, good PVT immunity, and simple architecture, but it cannot achieve accurate measurement due to its stochastic characteristic. A pipeline TDC [7, 8, 9, 10] based on the two-step time quantization has high resolution and fast speed; however, it is impossible to achieve accurate measurement without a linear time amplifier (TA).

A TA is a key module in a pipeline TDC, which amplifies the residue generated in the first-step quantization. A TA determines the measurement accuracy of a TDC and in-band phase noise of an ADPLL. The SR-latch-based TA [7] and the cross-couple structure [8] have a very narrow linear range due to the metastable work...
region and limited discharging time, respectively. A closed-loop TA [9] has a wider input linear range than the SR-latch structure, but the gain is not programmable. A promising TA [10] achieves time amplification by duplicating the residue in an OR gate, providing the wide input linear range and programmable gain simultaneously. However, its accuracy deteriorates due to the inevitable gain error generated by the long delay lines especially when the gain is high.

A pipeline TDC with a programmable-gain TA (PGTA) that has a wide linear range is proposed in this paper. The PGTA gain can be set to any integer as long as the delay line is long enough. Furthermore, the gain error of the PGTA can be compensated by a novel compensator. Using the proposed TDC, a 2.4-GHz ADPLL is implemented. The paper is organized as follows. The pipeline TDC is described and analyzed in Section 2, the ADPLL is presented in Section 3. In Section 4, the experimental results are presented and discussed, followed by a brief conclusion.

2 The proposed TDC

The proposed pipeline TDC is composed of a coarse TDC (CTDC), a PGTA, a compensator, a fine TDC (FTDC), and an encoder, as shown in Fig. 1. The CTDC is based on a traditional 16-stage delay-line structure with a unit delay time of about 30 ps, which defines the measurement range and resolution of the CTDC which are 480 ps and 30 ps, respectively. The arbiters based on a differential structure are used to shorten the metastable region.

In this work, the PGTA amplifies the residue generated in the CTDC by an integer value of up to 8. The compensator is used to correct the gain error of the PGTA. The output of the PGTA is fed to the FTDC that is based on a gated-vernier-delay-line (GVDL) structure.

2.1 PGTA

In the existing works [7, 8, 9, 10], the TAs amplify the residue in the stage where \( \text{stop} \) catches up with \( \text{start} \), which corresponds to the \( i \)th stage in the CTDC, as shown in the grey part of Fig. 1. In fact, the residue exists not only in the \( i \)th stage but also in every stage of the delay line. For instance, the time interval between \( \text{start}[i-1] \) and \( \text{stop} \) is \((\Delta t + \varepsilon)\) in the \((i-1)\)th stage. In the proposed PGTA, the
time amplification is achieved by adding $N_t$ time intervals in $N_t$ different stages, and the residue is thereby amplified by $N_t$ times. The PGTA is composed of a pulse shifter, an OR gate, and a digital controller, as shown in Fig. 2(a). The pulse shifter receives $N_t$ time intervals and shifts them with different delay buffers to avoid any overlapping among them. The OR gate sums the shifted intervals to generate serial pulses. The digital controller determines which time intervals will be fed to the PGTA according to the PGTA gain and $i$. If $i < N_t$, $N_t$ time intervals after the $i$th stage will be fed to the PGTA; otherwise, $N_t$ time intervals before the $i$th stage will be fed to the PGTA.

The total pulse width of the PGTA output can be determined as

$$
T_{\text{PGTA}} = \begin{cases} 
N_t \epsilon + \sum_{k=1}^{N_t-1} k\Delta t, & i \geq N_t \\
-N_t \epsilon + \sum_{k=1}^{N_t} k\Delta t, & i < N_t
\end{cases}
$$

where $N_t$ is the PGTA gain, $\epsilon$ denotes the residue, and $\Delta t$ is the unit delay time of buffers in the CTDC, i.e., the resolution of the CTDC. In Equation (2), only the first part, i.e., $N_t \epsilon$, denotes the amplified residue, and the needless second part can be easily subtracted in the encoder.

Since there are overlaps between time intervals in different stages, it is necessary to shift these intervals before feeding them to the OR gate. The pulse shifter uses different delay lines to shift the intervals to keep enough wide gap
between any two intervals. The concept of the pulse shifter is shown in Fig. 2(b), where \( N_t = 4 \) and \( i \geq N_t \). With the aim to shorten the delay lines, the widest interval of \((3/C_1 \Delta t + \varepsilon)\) generated in the \((i - 3)\)th stage remains unchanged, while the other three intervals propagate through different delay lines and thereby are shifted for different distances. The shift distance of an interval should be larger than a sum of its width in that stage and its shift distance in the previous stage. Therefore, when \( i \geq N_t \), the length of delay lines can be represented as

\[
L_k = \begin{cases} 
0, & k = i - (N_t - 1) \\
L_{k-1} + (i - k + 2) \Delta t, & 0 < k < i - (N_t - 1) \leq i
\end{cases}
\]

(3)

Otherwise, when \( i < N_t \), the length of delay lines can be represented as

\[
L_k = \begin{cases} 
0, & k = i + N_t \\
L_{k+1} + (k - i + 2) \Delta t, & 0 < k < i + N_t
\end{cases}
\]

(4)

In this work, the PGTA gain is from 2 to 8, and the corresponding lowest and highest time resolutions are about 10 ps and 2.5 ps, respectively. Substituting \( N_{\text{div}} = 120 \) and \( f_{\text{DCO}} = 2.4 \text{ GHz} \) in Equation (1), the in-band noise performances are about \(-100 \text{ dBc/Hz} \) and \(-112 \text{ dBc/Hz}\) at \( N_t = 2 \) and \( N_t = 8 \), respectively, and an improvement of about 12 dBc/Hz is achieved.

### 2.2 Compensator

As already mentioned, the proposed PGTA achieves linear time amplification by duplicating the residue. However, the duplication is not ideal because the pulse width shrinks gradually as the time intervals \( T_I \) propagate through the delay lines in...
the pulse shifter, which is due to the mismatch of the rise and fall times of the inverters in the delay buffers. Therefore, the actual pulse width of the PGTA output is shorter than \( N_t \). The non-ideality will cause a gain error, worsen the measurement accuracy, and further deteriorate the in-band phase noise performance of the ADPLL. In addition, the problem gets worse as the PGTA gain increases.

To solve the aforementioned problem, a compensator is proposed to compensate the lost parts of the pulses, as shown in Fig. 3(a). To align to the compensation object \( P[k] \), \( \text{start}[i-(N_t-1)] \) (or \( \text{start}[i+N_t] \)) and \( \text{stop} \) propagate through two delay lines that have the same length of \( L_k \). Thus, the time interval between \( \text{start}[i-(N_t-1)] \) and \( \text{stop} \), i.e., \( TT[i-(N_t-1)] \), is shifted by \( L_k \) without shrinking. The time difference between \( P[k] \) and \( TT[i-(N_t-1)] \) is obtained by an XOR gate as signal \( A \). Because \( P[k] \) is the shrunk signal of \( TT[k] \), the pulse width of \( A \) equals to \( [k-i+(N_t-1)]\Delta t + (e-e') \), where \( e-e' \) is the lost part, and the pulse width of \( TT[i-(N_t-1)] \) and \( P[k] \) are \( (N_t-1)\Delta t + e \) and \( (i-k)\Delta t + e' \), respectively. At last, signal \( A \) is compared with signal \( B \) whose width is \( [k-i+(N_t-1)]\Delta t \) and then, the compensation result \( C[k] \) is obtained. Fig. 3(b) shows the time diagram of the compensation of a compensation object \( P[i] \) at \( k = i\), \( N_t = 4 \), and \( i \geq N_t \). At first, the pulse \( (3\Delta t + e) \) is shifted by \( 7\Delta t \) without shrinking because the error is neutralized by the two equal delay lines. The signal \( A \) whose width is \( 3\Delta t' \) is wider than the signal \( B \) whose width is \( 3\Delta t \), because the width of \( P[i] \) shrinks in the pulse shifter. The compensation is achieved by subtracting signal \( B \) from signal \( A \) and adding the result \( \Delta e \) to the PGTA output in the OR gate, where \( \Delta e = e - e' \).

2.3 FTDC

Since the PGTA outputs the discrete pulses rather than a continuous one, a TDC based on a 40-stage GVDL structure is proposed for the second-step quantization, and it is shown in Fig. 4.

Take two cases presented in the dashed box in Fig. 5 as an example. In these cases, \( \Delta t_x = 30 \text{ ps} \), \( \Delta t_y = 40 \text{ ps} \), and \( N_t = 8 \). If the signal \( LP \) propagates through one delay buffer in the upper line and zero delay buffer in the lower line, the input time ranges of the upper line and the lower line are from \( 30 \text{ ps} \) to \( 60 \text{ ps} \) and from \( 0 \text{ ps} \) to \( 40 \text{ ps} \), respectively. Hence, the more precise input time range is from \( 30 \text{ ps} \) to \( 60 \text{ ps} \), and the corresponding output code is \( 00100 \). On the other hand, \( LP \) propagates through one delay buffer in the two delay lines, so, the precise input time range is from \( 40 \text{ ps} \) to \( 60 \text{ ps} \) and \( F_{out} \) is \( 00101 \). Although the most three significant bits of the output codes in both cases are the same and equal to 001, the
input time ranges are different. The difference in the input time range between the two situations can be noticed in the two least significant bits. The effective resolution of the FTDC can be defined by

\[
\tau_{\text{LSB,F}} = \frac{\Delta t_a}{1 + \frac{\Delta t_a}{\Delta t_b} - \frac{\Delta t_a}{\Delta t_{\text{lcm}}}} < \Delta t_a
\]  

(5)

where \(\Delta t_{\text{lcm}}\) denotes the least common multiple of \(\Delta t_a\) and \(\Delta t_b\). In this work, the FTDC has a resolution of 20 ps, and the pipeline TDC can achieve the highest resolution of 2.5 ps at \(N_t = 8\).

### 3 ADPLL

The structure of the ADPLL is shown in Fig. 6. On power up, only the auto frequency calibration (AFC) and DCO are active. AFC is used to detect frequency difference between \(f_{\text{ref}}\) and \(f_{\text{div}}\) and changes the integer part of oscillator tuning words (\(OTW_I\)) that control the coarse capacitor bank of DCO. The AFC operation is based on frequency estimation algorithm [11]. Once AFC finishes detection, it freezes \(OTW_I\) and activates digital loop filter (DLF), DCO, TDC and divider by setting Enable low voltage. The TDC senses and quantizes the phase difference between \(f_{\text{ref}}\) and \(f_{\text{div}}\), and the phase difference is then fed to the DLF. In order to keep loop stability, gains of proportional path and integral path in the DLF are set to be programmable according to the gain of the PGTA. The output of the DLF drives the DCO as the fractional part of \(OTW\) (\(OTW_F\)) that control the fine capacitor bank of DCO.
The output frequency of a DCO is discrete, which is different from the continuous frequency tuning in a voltage controlled oscillator. The out-band phase noise of an ADPLL is related to the frequency resolution of DCO as

$$\mathcal{L} = \frac{1}{12 f_{\text{ref}}} \left( \frac{f_{\text{LSB}}}{\Delta f} \right)^2 \left( \sin c \frac{\Delta f}{f_{\text{ref}}} \right)^2$$

(6)

where $f_{\text{LSB}}$ is the frequency resolution of DCO, $f_{\text{ref}}$ is the reference frequency of ADPLL, and $\Delta f$ means the frequency offset from carrier frequency [2]. It can be seen that high frequency resolution of DCO benefits the out-band phase noise performance of ADPLL. In this work, a bridging-capacitance technique [5] and a current-reuse structure are used to improve the frequency resolution and reduce power, as shown in Fig. 7. The LC-based DCO contain two same capacitor bank, coarse bank and fine bank, both of which are controlled by 6-bit $OTW$. A MOS capacitor, comprising two pMOS pairs that are inversely connected in parallel, is used as the unit of the two capacitor banks. When $OTW$ is high, pair1 works in inversion region while pair2 works in depletion region. When $OTW$ is low, pair1 works in depletion region while pair2 works in inversion region. The size of the transistors in pair1 and pair2 are 800/65 and 400/65 respectively, resulting in a unit capacitance $\Delta C_u$ of about 200 aF and a corresponding frequency resolution of 200 kHz/LSB. To enhance the frequency resolution, bridging capacitors $C_b$ are set between the coarse bank and the fine bank. The unit capacitance is then recalculated as

$$\Delta C_{\text{unit}} = \Delta C_u \left( \frac{C_b}{2C_f} \right)^2$$

(7)

where $C_f$ means the total capacitance of the fine bank. Substituting $\Delta C_u = 200$ aF, $C_b = 12.6C_u$ and $C_f = 63C_u$ in Equation (7), we obtain the unit capacitance is about 2 aF and the improved frequency resolution is about 3 kHz/LSB, which theoretically translates to a phase noise of $-135$ dBc/Hz@1 MHz offset.

In order to reduce the power dissipation, a current-reuse structure under a 0.6-V supply is used. By stacking a nMOS and a pMOS as cross-coupled pair, a same current from the near-threshold supply is flowing into the transistors, which means the current is reused. Therefore, the power is greatly reduced due to both the lower current and lower supply.
4 Experimental results

The proposed ADPLL was fabricated in the 65-nm CMOS technology. The core area was 0.64 mm², as shown in Fig. 8. The ADPLL consumed a total power of 4.8 mW at a 1.2-V supply, except the DCO that worked at a 0.6-V supply.

To measure the performance of the proposed TDC, two inputs with a difference of 0.1 Hz at the frequency of 20 MHz were applied to generate a ramp input. As shown in Fig. 9, the effective steps of the code were 192, corresponding to the highest resolution of about 2.47 ps at $N_t = 8$, which agreed with the analysis given in Section 2.3. Fig. 10 shows the comparison of the single-shot measurement results at $N_t = 2$ and $N_t = 8$ for a constant input of 200 ps repeated $10^5$ times. Because of the compensator, the TDC exhibited the centralized code distribution at $N_t = 8$ (standard deviation was 0.64 LSB), which highly approximated the distribution at $N_t = 2$ (standard deviation was 0.62 LSB). Therefore, the measurement accuracy of the TDC scarcely deteriorated as $N_t$ increased.
The phase-noise plots of the ADPLL at $N_t = 2$ and $N_t = 8$ are shown in Fig. 11. The in-band phase noise was about $-90 \text{ dBc/Hz at 10 kHz}$ offset at $N_t = 8$, achieving the improvement of 7.3 dBc/Hz compared with that at $N_t = 2$. The out-band phase noise of $-131 \text{ dBc/Hz at 1 MHz}$ offset was achieved at $N_t = 8$, approximating the result at $N_t = 2$.

The jitter performance is shown in Fig. 12, where it can be seen that at 2.4 GHz, the RMS jitter was 1.24 ps and the peak-to-peak jitter was 8.65 ps. The comparison of the performances of this and a few related works is given in Table I. According
to the values in Table I, in this work, the best jitter performance and FoM were achieved.

5 Conclusion

A 2.4-GHz ADPLL with a pipeline TDC is proposed in this paper. A PGTA is used to achieve the time amplification with the programmable gain and wide linear input range. A compensator is employed to compensate the gain error of the PGTA and improve the measurement accuracy and in-band phase noise performance. An FTDC based on the GVDL structure achieves higher resolution than the CTDC and further improves the effective resolution of the TDC to 2.47 ps. However, the disadvantage of the TDC is that the PGTA gain is limited to an integer value that cannot be larger than the number of stages in the CTDC. The proposed chip was fabricated in the 65-nm CMOS technology, and the measured results showed that the TDC exhibited the centralized code distribution even at high PGTA gain due to the usage of the compensator. The fabricated ADPLL achieved the in-band phase noise and the FoM of $-90$ dBc/Hz@10kHz offset and $-231$ dB, respectively.

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