A Study on Neutral-Point Potential in Three-Level NPC Converters

Maosong Zhang, Ying Cui, Qunjing Wang, Jun Tao, Xiuqin Wang, Hongsheng Zhao and Guoli Li

1 School of Electrical Engineering and Automation, Anhui University, Hefei 230601, China
2 Collaborative Innovation Center of Industrial Energy-Saving and Power Quality Control, Anhui University, Hefei 230601, China
3 Engineering Research Center of Power Quality, Ministry of Education, Anhui University, Hefei 230601, China
4 State Grid Hubei Electric Power Company Limited Economic Research Institute, Wuhan 430077, China

Received: 4 June 2019; Accepted: 27 August 2019; Published: 1 September 2019

Abstract: This paper proposes an accurate mathematical model of three-level neutral-point-clamped (NPC) converters that can accurately represent the midpoint potential drift of the DC link with parameter perturbation. The mathematical relationships between the fluctuation in neutral-point voltage, the parametric perturbation, and the capacitance error are obtained as mathematical expressions in this model. The expressions can be used to quantitatively analyze the reason for the neutral-point voltage imbalance and balancing effect based on a zero-sequence voltage injection. The injected zero-sequence voltage, which can be used to balance the DC-side voltages with the combined action of active current, can be easily obtained from the proposed model. A balancing control under four-quadrant operation modes is proposed by considering the active current to verify the effectiveness of this model. Both the simulation and experiment results validate the excellent performance of the proposed model compared to the conventional model.

Keywords: neutral-point-clamped (NPC) converters; quantitative analysis; uneven shunt loss; zero-sequence voltage; active current

1. Introduction

Three-level neutral-point-clamped (NPC) converters are popularly used in renewable energy generation and energy storage, which have been widely recognized as promising solutions to the problems associated with increasing environmental challenges [1–3]. Compared to the two-level topology, three-level NPC converters are much more attractive because of their lower voltage stress on power electronic devices, lower total harmonic distortion, higher efficiency, and even better economic performance [4–6].

However, the neutral-point potential drift, which results in an imbalance of voltages of the two DC-side capacitors, is an inherent problem for the three-level NPC topology. Without considering the sampling error, capacitance error, inconsistent characteristics of devices, and operation under unbalanced conditions are usually considered the reasons for potential drift. How to keep the upper and lower voltages equal is very important for the devices to run safely and reliably [7–9].

Numerous research works have been carried out to realize control of the DC-side voltage balance [10–27]. In [14–17], it is proposed that the neutral-point potential of the inverters can be balanced by hardware, including independent DC voltage sources and auxiliary converters that inject current into the neutral point. But this method needs an additional circuit, which increases the cost, volume of the converter, and reduces the efficiency. In [18–22], several improved space vector
pulse width modulation (SVPWM) strategies were proposed to adjust the dwell time between small
vector switching states by judging the direction of the neutral point current and the deviation of the
neutral point potential. However, the calculation methods are complex and difficult to implement.
In [24], a pulse width modulation (PWM) strategy was proposed where the both DC-side voltages
can be adjusted independently through zero-sequence voltage injections and compensation for the
unbalance in neutral point voltages, but the process of calculating the injected zero-sequence voltages
is complicated.

However, these control strategies, above all, ignore the quantitative analysis of the potential drift
and balancing effect based on zero-sequence voltage injection. Meanwhile, if the converter is used
in renewable energy generation and energy storage with four-quadrant operation modes, the DC
voltage balancing control is very difficult to realize in existing literature because the active current of
the converter is not taken into consideration.

This paper proposes an accurate mathematical model of the neutral-point potential in three-level
NPC converters based on the SPWM strategy with parametric perturbation and zero-sequence voltage
injection. The model is simple and direct, but very interesting and valuable. To the best of our
knowledge, it is novel and has not been previously reported in the literature. From this model, the
relationship between the drift potential value and all the AC-side and DC-side variables can be deduced
by quantitative analyses. The calculated drift potential value shows that the basic reason for the
neutral-point potential drift is the uneven shunt loss caused by the parametric perturbation, and the
capacitance error has no influence on it. The balancing control can be directly obtained based on the
combined action of the injected zero-sequence voltage and active current. The required zero-sequence
voltage for balancing control can be easily calculated by this model.

The rest of this paper is organized as follows. Section 2 describes the main circuit topology,
modulation strategy and AC-side current control. Section 3 develops the accurate mathematical model
of the neutral-point potential drift, which shows the reason for the neutral-point potential drift. DC
voltage control is realized in Section 4. In Section 5, the effectiveness and performance of this model
and control strategy are verified by simulation and experiment.

2. Operation and Principles

2.1. Main Circuit Topology

The circuit topology of three-level NPC grid-connected converters used in renewable, energy-based
applications is presented in Figure 1. The converter transfers active power from wind energy,
photovoltaic energy, chemical energy, or the energy storage system to the distribution network. In some
cases, it also can transfer active power from the distribution network to the energy storage system as
well as compensate reactive power to the network.

Figure 1. The circuit topology of three-level neutral-point-clamped (NPC) grid-connected converter.
As shown in Figure 1, $U_{dc}$ denotes the DC-side voltage source, and $Y_d$ is the internal resistor. $u_x$ ($x = a, b, c$) is the system voltage, $v_x$ is the output voltage of the converter. $C_1$ and $C_2$ are the two DC-side capacitors. $Y_1$ and $Y_2$ represent the shunt loss, including losses in the two parallel resistors and the power electronic switches. $U_1$ and $U_2$ are the two DC-side capacitor voltages. $L_s$ is the linked reactor. The series losses are represented by the equivalent resistance $R_{iab}$. The AC-side current control model can be derived as

\[
L_s \frac{di_{abc}}{dt} = -R_{iabc} - u_{abc} + v_{abc}
\]

where $i_{abc} = [i_a \ i_b \ i_c]^T$, $u_{abc} = [u_a \ u_b \ u_c]^T$, and $v_{abc} = [v_a \ v_b \ v_c]^T$.

2.2. Modulation Strategy

Power electronic switches in Figure 1 can be turned on and off based on the alternative phase opposition disposition (A POD) sine pulse width modulation (SPWM) strategy, as shown in Figure 2. Take phase $a$ of Figure 1 as an example, $s_a$ is the modulation signal with zero-sequence DC component $s_0$. $CA_1$ and $CA_2$ are the two triangular carrier waveforms with the same frequency, same amplitude, and contrary phases. Switches $Q_1$ and $Q_3$ are turned on and off based on the comparison of $s_a$ and $CA_1$. Switches $Q_2$ and $Q_4$ are turned on and off based on the comparison of $s_a$ and $CA_2$. Diodes $D_1$ and $D_2$ provide the bidirectional current path for the AC-side terminal to the common point of the DC capacitors $O$, when both $Q_2$ and $Q_3$ are on or off. Therefore, $v_a$ swings between the neutral-point potential (here referred to as zero) when both $Q_2$ and $Q_3$ are on or off, $U_1$ when both $Q_1$ and $Q_2$ are on, and $-U_2$ when both $Q_3$ and $Q_4$ are on [28].

![Figure 2. Alternative phase opposition disposition sine pulse width modulation (A POD-SPWM) strategy.](image)

2.3. AC-Side Current Control

The system voltages can be written as

\[
\begin{align*}
    u_a &= U \cos(\omega t) \\
    u_b &= U \cos(\omega t - 2\pi/3) \\
    u_c &= U \cos(\omega t + 2\pi/3)
\end{align*}
\]

Based on Kirchhoff’s voltage law, the AC-side current control model can be derived as

\[
L_s \frac{di_{abc}}{dt} = -R_{iabc} - u_{abc} + v_{abc}
\]
Transforming Equation (2) into the dq rotating frame results in
\[
\begin{align*}
L_s \frac{dI_d}{dt} &= -R_s I_d + \omega L_i I_q - U_d + V_d \\
L_s \frac{dI_q}{dt} &= -R_s I_q - \omega L_d I_d - U_q + V_q
\end{align*}
\]
where
\[
T = \sqrt{\frac{2}{3}}
\begin{bmatrix}
\cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\
-\sin(\omega t) & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3})
\end{bmatrix}
\]
\[
\begin{bmatrix}
I_d \\
I_q
\end{bmatrix}^T = Ti_{abc}
\]
\[
\begin{bmatrix}
U_d \\
U_q
\end{bmatrix}^T = Tu_{abc}
\]
\[
\begin{bmatrix}
V_d \\
V_q
\end{bmatrix}^T = Tv_{abc}
\]

A decoupled, state variable feedback linearization current control with two independent proportional integral (PI) controllers can be defined by [29]
\[
V_d = \left(K_p1 + \frac{K_{i1}}{s}\right)(I_{d}^{\ast} - I_d) - \omega L_i I_q + U_d
\]
\[
V_q = \left(K_p1 + \frac{K_{i1}}{s}\right)(I_{q}^{\ast} - I_q) + \omega L_d I_d + U_q
\]

3. Dynamic Model

3.1. Basic Mathematical Equations

The following assumptions are made in order to derive the mathematical model:

1. The carrier frequency is much larger than that of the modulation signal.
2. There is no harmonic component in the reference output current.

Formulas can be derived as
\[
s_x = s_x^1 + s_0
\]
\[
\begin{align*}
U_1 &= U^\ast + u_1 + u_2 \\
U_2 &= U^\ast + u_1 - u_2
\end{align*}
\]
where \(s_x\) is the modulation signal of phase \(x\), \(s_x^1\) is the fundamental component, and \(s_0\) is the zero-sequence DC component. \(U^\ast\) is the reference value. \(u_1\) reflects the error between the total DC-side voltage and reference value. \(u_2\) reflects the imbalance of the voltages of the two DC-side capacitors [28].

Considering that there is no pathway for zero-sequence component to flow in the three-phase three-wire circuit, \(s_0\) has no fluence on the AC-side current control.

Thus, from Equations (10) and (11), Figures 1 and 2, when \(s_x > 0\):
\[
i_{px} = (s_x^1 + s_0)i_x
\]
\[
i_{nx} = 0
\]
and when \(s_x < 0\):
\[
i_{px} = 0
\]
\[
i_{nx} = (s_x^1 + s_0)i_x
\]

Additionally, during a complete primitive period:
\[
v_x = (s_x^1 + s_0)(U^\ast + u_1) + |s_x^1 + s_0|u_2
\]
\[ i_p = i_{pa} + i_{ph} + i_{pc} \]  
\[ i_n = i_{na} + i_{nb} + i_{nc} \]  
\[ i_d = Y_d U_{dc} - 2 Y_d (U^* + u_t) \]  
\[ C_1 \frac{dU_1}{dt} + Y_1 U_1 + i_p = i_d \]  
\[ C_2 \frac{dU_2}{dt} + Y_2 U_2 + i_n = i_d \]  

The capacitance of the capacitors will decrease slowly as time goes on, and the shunt power loss is not the same during different running states. Let

\[
\begin{align*}
C_1 &= C/2 + \Delta c/2 \\
C_2 &= C/2 - \Delta c/2 \\
Y_1 &= Y/2 + \Delta y/2 \\
Y_2 &= Y/2 - \Delta y/2
\end{align*}
\]  

where \( C \) is the nominal value of the total dc capacitance value, \( Y \) is the estimated value of total shunt loss, \( \Delta c \) reflects the deviation capacity of the two capacitors, and \( \Delta y \) reflects the uneven shunt loss between the two DC-side capacitors [30].

Substituting Equation (22) into Equations (20) and (21) yields

\[
\begin{align*}
(C^2 - \Delta c^2) \frac{dU_1}{dt} &= (-C Y + \Delta c \Delta y - 4 CY_d) u_1 + (-C \Delta y + \Delta c Y) u_2 - C(i_p + i_n) \\
&\quad + \Delta c(i_p - i_n) + (-C Y + \Delta c \Delta y - 4 CY_d) U^* + 2 CY_d U_{dc}
\end{align*}
\]

\[
\begin{align*}
(C^2 - \Delta c^2) \frac{dU_2}{dt} &= (-C \Delta y + \Delta c Y + 4 \Delta c Y_d) u_1 + (-C \Delta y + \Delta c \Delta y) u_2 + \Delta c(i_p + i_n) \\
&\quad - C(i_p - i_n) + (-C \Delta y + \Delta c Y + 4 \Delta c Y_d) U^* - 2 \Delta c Y_d U_{dc}
\end{align*}
\]

Equations (23) and (24) show the basic mathematical model of DC-side voltages with parametric perturbation. From this model, it can be seen that \( u_1 \) and \( u_2 \) can be regulated by \( i_p + i_n \) and \( i_p - i_n \).

### 3.2. Instantaneous Value of \( i_p + i_n \) and \( i_p - i_n \)

In general, the switch function \( s_a \) with zero-sequence dc component \( s_0 \) can be written as

\[
\begin{align*}
s_a &= m \cos(ωt + δ) + s_0 \\
s_b &= m \cos(ωt + δ - \frac{2π}{3}) + s_0 \\
s_c &= m \cos(ωt + δ + \frac{2π}{3}) + s_0
\end{align*}
\]  

where \( m \) is the modulation index and \( 0 < m < 1 \). \( δ \) is the phase angle between the output voltage of the converter and the system voltage, \(-π/2 < δ < π/2\).

It is assumed that the output currents are sinusoidal, as in the following equations:

\[
\begin{align*}
i_a &= I_{ao} \cos(ωt + δ) - I_{eq} \sin(ωt + δ) \\
i_b &= I_{ao} \cos(ωt + δ - \frac{2π}{3}) - I_{eq} \sin(ωt + δ - \frac{2π}{3}) \\
i_c &= I_{ao} \cos(ωt + δ + \frac{2π}{3}) - I_{eq} \sin(ωt + δ + \frac{2π}{3})
\end{align*}
\]  

where \( |I_{ao}| \) and \( |I_{eq}| \) are the amplitudes of active current and reactive current, respectively, that are related to the converter.

Base on the polarity of \( s_a, s_b, \) and \( s_c \), a complete primitive period can be divided into six parts, as shown in Figure 3, where \( ωt_1 \ldots ωt_7 \) are the zero-crossing points of \( s_a \) respectively, and \( ωt_1 = -π - δ - cos^{-1} \frac{50}{m}, ωt_2 = \frac{π}{3} - δ - cos^{-1} \frac{50}{m}, ωt_3 = -\frac{π}{3} - δ + cos^{-1} \frac{50}{m}, ωt_4 = π - δ - cos^{-1} \frac{50}{m}, ωt_5 = \frac{π}{3} - δ + cos^{-1} \frac{50}{m}, ωt_6 = \frac{5π}{3} - δ - cos^{-1} \frac{50}{m}, \) and \( ωt_7 = π - δ + cos^{-1} \frac{50}{m} \).
3.3. The Neutral-Point Potential Model

From Equations (25) and (26), the following can be directly obtained:

$$s_{a}i_{a} + s_{b}i_{b} + s_{c}i_{c} = \frac{3}{2} mI_{cd}$$  \hspace{1cm} (27)$$

Then $i_{p} + i_{n}$ can be deduced from Equation (27) and Table 2, where

Table 1. Instantaneous values of $i_{px}$ and $i_{nx}$.

| Section | $i_{pa}$ | $i_{pb}$ | $i_{pc}$ | $i_{na}$ | $i_{nb}$ | $i_{nc}$ |
|---------|----------|----------|----------|----------|----------|----------|
| 1       | $s_{a}l_{a}$ | 0        | $s_{b}l_{b}$ | 0        | $s_{b}l_{b}$ | 0        |
| 2       | $s_{a}l_{a}$ | 0        | 0        | $s_{b}l_{b}$ | $s_{c}l_{c}$ | $s_{c}l_{c}$ |
| 3       | $s_{a}l_{a}$ | $s_{b}l_{b}$ | 0        | 0        | 0        | $s_{c}l_{c}$ |
| 4       | 0        | $s_{b}l_{b}$ | 0        | $s_{b}l_{b}$ | 0        | $s_{c}l_{c}$ |
| 5       | 0        | $s_{b}l_{b}$ | $s_{c}l_{c}$ | $s_{b}l_{b}$ | 0        | 0        |
| 6       | 0        | 0        | $s_{c}l_{c}$ | $s_{c}l_{c}$ | $s_{b}l_{b}$ | 0        |

Table 2. Instantaneous values of $i_{p} + i_{n}$ and $i_{p} - i_{n}$.

| Section | $i_{p} + i_{n}$ | $i_{p} - i_{n}$ |
|---------|----------------|----------------|
| 1       | $s_{a}l_{a} + s_{b}l_{b} + s_{c}l_{c}$ | $s_{a}l_{a} - s_{b}l_{b} + s_{c}l_{c}$ |
| 2       | $s_{a}l_{a} + s_{b}l_{b} + s_{c}l_{c}$ | $s_{a}l_{a} - s_{b}l_{b} - s_{c}l_{c}$ |
| 3       | $s_{a}l_{a} + s_{b}l_{b} + s_{c}l_{c}$ | $s_{a}l_{a} + s_{b}l_{b} - s_{c}l_{c}$ |
| 4       | $s_{a}l_{a} + s_{b}l_{b} + s_{c}l_{c}$ | $-s_{a}l_{a} + s_{b}l_{b} - s_{c}l_{c}$ |
| 5       | $s_{a}l_{a} + s_{b}l_{b} + s_{c}l_{c}$ | $-s_{a}l_{a} + s_{b}l_{b} + s_{c}l_{c}$ |
| 6       | $s_{a}l_{a} + s_{b}l_{b} + s_{c}l_{c}$ | $-s_{a}l_{a} - s_{b}l_{b} + s_{c}l_{c}$ |

From Equations (12)–(15) and Figure 3, the instantaneous values of $i_{px}$ and $i_{nx}$ can be obtained and are shown in Table 1.

From Equations (17) and (18), and Table 1, the instantaneous values of $i_{p} + i_{n}$ and $i_{p} - i_{n}$ can be derived and are shown in Table 2.
\[ i_p + i_n = \frac{3}{2} mI_{cd} \] (28)

The instantaneous value of \( i_p - i_n \) shown in Table 2 is not always the same. In order to analyze and control the DC-side voltages, the generalized state-space averaging method can be used, which is a mature tool for large signal, dynamic modeling of power converters [31]. Here,

\[
x(t) = \sum_{k=-\infty}^{k=+\infty} \langle x \rangle_k(t) e^{jk\omega t}
\]

(29)

\[
\langle x \rangle_k(t) = \frac{1}{T} \int_{t-T}^{t} x(\tau)e^{-jk\omega \tau} d\tau
\]

(30)

\[
\frac{d}{dt} \langle x \rangle_k(t) = \left\{ \frac{d}{dt} \right\}_k (t) - jk\omega \langle x \rangle_k(t)
\]

(31)

where \( \omega = 2\pi/T \), and \( \langle x \rangle_k(t) \) is the \( k \)th coefficients of Fourier series expansion of \( x(t) \).

Only the DC component within one fundamental period can be taken into consideration for the DC-side voltage control. Thus

\[
\langle i_p + i_n \rangle = \frac{3}{2} mI_{cd}
\]

(32)

Because of \( s_0 \), the interval lengths of Part I, III and V in Figure 3 are not equal to the interval lengths of parts II, IV and VI, which results in a DC component of \( i_p - i_n \). From Equations (25) and (26), and Table 2, it can be deduced that

\[
\langle i_p - i_n \rangle = \frac{1}{T} \int_{t-T}^{t} (i_p - i_n) d\tau = 3I_{cd} \frac{m \sin^{-1} \frac{s_0}{m} + s_0 \sin \left( \frac{\cos^{-1} \frac{s_0}{m}}{\pi} \right)}{\pi}
\]

(33)

Because \( s_0 = 0 \), it can be assumed that

\[
\sin^{-1} \frac{s_0}{m} = \frac{s_0}{m}, \cos^{-1} \frac{s_0}{m} = \frac{\pi}{2} \sin \left( \frac{\cos^{-1} \frac{s_0}{m}}{\pi} \right) = 1
\]

(34)

From Equation (34), Equation (33) can be rewritten as

\[
\langle i_p - i_n \rangle = \frac{6}{\pi} s_0 I_{cd}
\]

(35)

Taking the zeroth averages of both sides of Equations (23) and (24), considering Equations (29)–(31) and (35), the following is obtained

\[
\left(C^2 - \Delta \xi^2\right) \frac{d(u_1)_0}{dt} = (-CY + \Delta \xi Y - 4CY_d)(u_1)_0 + (-C\Delta Y + \Delta \xi Y)(u_2)_0 - \frac{3}{2} C mI_{cd} + \frac{6}{\pi} C s_0 I_{cd} + (-CY + \Delta \xi Y - 4CY_d)U' + 2CY_d U_{dc}
\]

(36)

\[
\left(C^2 - \Delta \xi^2\right) \frac{d(u_2)_0}{dt} = (-C\Delta Y + \Delta \xi Y + 4\Delta \xi Y_d)(u_1)_0 + (-CY + \Delta \xi Y)(u_2)_0 + \frac{3}{2} C mI_{cd} - \frac{6}{\pi} C s_0 I_{cd} + (-C\Delta Y + \Delta \xi Y + 4\Delta \xi Y_d)U' - 2CY_d U_{dc}
\]

(37)

where \( (u_1)_0 \) and \( (u_2)_0 \) are the DC components of \( u_1 \) and \( u_2 \).

Suppose that under DC voltage stable control (which may not be necessary under some operation conditions, such as in renewable energy based applications), \( (u_1)_0 = 0, \) and \( \frac{d(u_1)_0}{dt} = 0 \), then from Equation (36) the following can be obtained

\[
\frac{3}{2} mI_{cd} = (-\Delta Y + \Delta \xi Y)(u_2)_0 + (-Y + \frac{\Delta \xi}{C} \Delta Y - 4Y_d)U' + \frac{6}{\pi} \frac{\Delta \xi}{C} s_0 I_{cd} + 2Y_d U_{dc}
\]

(38)
Substituting Equation (38) into Equation (37) yields

\[
\frac{d\langle u_2 \rangle_0}{dt} = -Y\langle u_2 \rangle_0 - \Delta y U^* - \frac{6}{\pi} s_0 I_{vd}
\]  

(39)

Equation (39) is the accurate mathematical model of the neutral-point potential drift in three-level NPC converters based on the SPWM strategy with parametric perturbations and zero-sequence voltage injections. This model is simple and direct but very interesting and valuable.

From Equation (39), the stable drift potential value with parametric perturbation and zero-sequence voltage injection can be easily obtained as

\[
\langle u_2 \rangle_0 = -\frac{\Delta y}{Y} U^* - \frac{6}{\pi} s_0 I_{vd}
\]  

(40)

Equation (40) shows the relationship between the drift potential value and all AC- and DC-side variables by quantitative analysis. The relationships are very clear.

When \( s_0 = 0 \), a stable value can be derived as \( \langle u_2 \rangle_0 = -\frac{\Delta y}{Y} U^* \). In order to adjust \( \langle u_2 \rangle_0 = 0 \), the required zero-sequence component can be easily obtained as \( s_0 = -\frac{\pi}{6\Delta y} (Y\langle u_2 \rangle_0 + \Delta y U^*) \).

Actually, the parametric perturbation \( \Delta y \) is associated with the inconsistent characteristics of power electronic switches and unequal shunt resistances. If \( \Delta y = 0 \), the potential drift may still exist because of the unexpected zero-sequence component from digital implementation in the modulation signal.

4. DC Voltage Control

4.1. Balancing Control

The DC link of three-level NPC converters is connected by two series capacitors, and the purpose of DC-side voltage control is to maintain the two voltages at an equal and prespecified level. Thus, control can be divided into two parts: (1) Maintain \( U_1 + U_2 \) at a prespecified level, which can be called stable control of the DC-side voltage, and (2) Maintain \( U_1 \) and \( U_2 \) as equal, which can be called DC-side voltage balancing control.

Stable control of the DC-side voltage can be easily obtained from the analytical techniques developed for the two-level converters. If the converter has a DC voltage source, such as that used in renewable energy-based applications, stable control is not necessary.

It is well known that by injecting a zero-sequence voltage, the DC-side voltage balancing control can be realized. However, existing strategies do not take the influence of the active current \( I_{vd} \) of the converter into consideration.

Equation (39) shows that \( I_{vd} \) is very important for the DC-side voltage balancing control. The injected zero-sequence voltage can be used to adjust the potential drift with the combined action of \( I_{vd} \) directly. Thus, it is very difficult to realize the DC link voltage balancing control if the converter is used in four-quadrant operation mode.

Taking the polarity and amplitude of \( I_{vd} \) into consideration, the DC-side voltage balancing control can be realized, as shown in Figure 4, where \( I_{vd} \) can be calculated from Equation (46).

![Figure 4. DC-side voltage balancing control when considering \( I_{vd} \).](image-url)
4.2. Calculating the Value of $I_{vd}$

The value of $I_{vd}$ is very important for the voltage balancing control, but it cannot be directly obtained from sampling or coordinate transformation.

Suppose that $u_2 = 0$, from Equation (16), then the output voltage $v_{abc}$ can be written as

$$
\begin{align*}
    v_a &= (m \cos(\omega t + \delta) + s_0)(U^* + u_1) \\
    v_b &= (m \cos(\omega t + \delta - \frac{2\pi}{3}) + s_0)(U^* + u_1) \\
    v_c &= (m \cos(\omega t + \delta + \frac{2\pi}{3}) + s_0)(U^* + u_1)
\end{align*}
$$

By transforming $v_{abc}$ into the dq rotating frame, based on Equations (4) and (7), it can be deduced that

$$
\cos \delta = \frac{V_d}{\sqrt{V_d^2 + V_q^2}}
$$

$$
\sin \delta = \frac{V_q}{\sqrt{V_d^2 + V_q^2}}
$$

Transforming $I_{abc}$ shown in Equation (26) into the dq rotating frame, based on Equations (4) and (5), $I_{vd}$ and $I_{vq}$ can be obtained as

$$
I_{vd} = \frac{\sqrt{6}}{3} (I_d \cos \delta + I_q \sin \delta)
$$

$$
I_{vq} = \frac{\sqrt{6}}{3} (-I_d \sin \delta + I_q \cos \delta)
$$

Substituting Equations (42) and (43) into Equations (44) and (45), replacing $I_d$ and $I_q$ with $I_{d*}$ and $I_{q*}$, the values of $I_{vd}$ and $I_{vq}$ can be deduced as

$$
I_{vd} = \frac{\sqrt{6}}{3 \sqrt{V_d^2 + V_q^2}} (V_d I_{d*} + V_q I_{q*})
$$

$$
I_{vq} = \frac{\sqrt{6}}{3 \sqrt{V_d^2 + V_q^2}} (-V_q I_{d*} + V_d I_{q*})
$$

5. Simulation and Experiment

5.1. Simulation Analysis

A simulation model based on the topology shown in Figure 1 is set up by using MATLAB/Simulink. The control block is shown in Figure 5, and simulation parameters are shown in Table 3. In this case, the DC link has a DC voltage source, and voltage stable control is not needed here. The reference currents $I_{d*}$ and $I_{q*}$ will be set by the control system under different working conditions, including but not limited to, renewable energy applications.
5.1.1. Accuracy of Equation (39)

The upper and lower DC-side capacitors have two equalizing discharge resistors. Suppose the admittance values are \( Y_p1 \) and \( Y_p2 \). Power electronic switches have identical characteristics in the simulation environment. Suppose the upper and lower equivalent admittances have the same value as \( Y_p \), which is variable under different \( I_{ld} \) and \( I_{eq} \).

From Equation (22), it can be deduced that

\[
\begin{align*}
\Delta y &= Y_{p1} - Y_{p2} \\
\Delta c &= C_1 - C_2 \\
Y &= Y_{p1} + Y_{p2} + 2Y_p \\
C &= C_1 + C_2
\end{align*}
\]

The existence of \((u_2)_0\) may be caused by \( \Delta y \) and \( \Delta c \), which reflect the difference between the upper and lower sides. The amplitude may be influenced by \( Y \) and \( C \). In order to get the relationship, set \( s_0 = 0 \) at first, and the current references can be fixed such as \( I_{ld}^* = I_{eq}^* = 50 \ A \) so as to get a certain value of \( Y_p \).

Figure 6 shows the waveforms of \( u_2 \) under different \( Y_{p1}, Y_{p2}, C_1 \), and \( C_2 \) when \( s_0 = 0 \). The values of \( \Delta y, \Delta c, Y, \) and \( C \) can be obtained from Equation (48), shown in Table 4.
Figure 6. (a–h) Waveforms of $u_2$ when $s_0 = 0$.

**Table 4.** Values of $\langle u_2 \rangle_0$ when $s_0 = 0$.

| Figure 6 | $\Delta y/\Omega^{-1}$ | $\Delta c/\mu F$ | $Y/\Omega^{-1}$ | $C/\mu F$ | $\langle u_2 \rangle_0/V$ (Simulation) | $\langle u_2 \rangle_0/V$ (Calculated) |
|----------|------------------------|------------------|----------------|---------|--------------------------------------|--------------------------------------|
| (a)      | 0                      | 0                | $2Y_P + 0.002$ | 20,000  | 0                                    | 0                                    |
| (b)      | 0                      | 5000             | $2Y_P + 0.002$ | 20,000  | 0                                    | 0                                    |
| (c)      | 0.001                  | 0                | $2Y_P + 0.002$ | 20,000  | $-34.5$                             | $-34.5$                             |
| (d)      | $-0.001$               | 0                | $2Y_P + 0.002$ | 20,000  | 34.5                                 | 34.5                                 |
| (e)      | 0.0005                 | 0                | $2Y_P + 0.002$ | 20,000  | $-18.5$                             | $-17.3$                             |
| (f)      | 0.0015                 | 0                | $2Y_P + 0.002$ | 20,000  | $-49.6$                             | $-51.7$                             |
| (g)      | 0.001                  | 0                | $2Y_P + 0.004$ | 20,000  | $-29.5$                             | $-29.2$                             |
| (h)      | 0.001                  | 0                | $2Y_P + 0.002$ | 10,000  | $-35.0$                             | $-34.5$                             |
Under the conditions shown in Figure 6, the output currents always track the reference currents very well without steady error. The system voltage \( u_d \), reference current \( i_{q*} \), and output current \( i_q \) of phase A in abc frame under the conditions of Figure 6f are shown in Figure 7.

![Figure 7. Waveforms of \( u_d \), \( i_{q*} \), and \( i_q \).](image)

From Figure 6a,c–f, it can be obtained that \( \Delta y \) is proportional to \( \langle u_2 \rangle_0 \) with opposite polarity. From Figure 6a,b, it can be seen that \( \Delta c \) has no influence on \( \langle u_2 \rangle_0 \). From Figure 6c,g, it can be obtained that \( Y \) is inversely proportional to \( \langle u_2 \rangle_0 \). From Figure 6c,h, it can be seen that \( C \) has no influence on the stable value \( \langle u_2 \rangle_0 \). Thus, the relationships between \( \langle u_2 \rangle_0 \) and \( \Delta y, \Delta c, Y, \) and \( C \) all correspond to Equation (39) from Figure 6.

Furthermore, substituting \( U^* = 380 \text{ V}, \Delta y = 0.001 \text{ \Omega}^{-1}, s_0 = 0 \) and \( \langle u_2 \rangle_0 = -34.5 \text{ V} \) from Figure 6c into Equation (39), the estimated value of \( Y_p \) can be derived as

\[
Y_p = -\frac{\langle \Delta y \rangle}{\langle u_2 \rangle_0} + Y_{p1} + Y_{p2} = 0.0045 \text{ \Omega}^{-1}
\]  

(49)

Because the reference currents in Figure 6 are the same, the estimated value of \( Y_p \) from Figure 6c can be used in Figure 6d–h. From this value, the calculated values of \( \langle u_2 \rangle_0 \) in Figure 6d–h can be derived, as shown in Table 4. It can be seen that the simulation values and calculated values are very close, which verified Equation (39) by a quantitative relationship when \( s_0 = 0 \).

From Figure 6, it also can be observed that \( u_2 \) mainly has the DC component and third component, and \( C \) influences the amplitude of the third component, which can be easily derived.

By introducing \( s_0 \), the waveforms of \( u_t \) with different \( I_d^* \) and \( I_q^* \) are shown in Figure 8. The values of \( I_{d0} \) and \( I_{q0} \) can be obtained from Equations (46) and (47), shown in Table 5.

![Figure 8. Cont.](image)
Figure 8. (a–h) Waveforms of $u_2$ when $s_0 \neq 0$.

Table 5. Values of $\langle u_2 \rangle_0$ when $s_0 \neq 0$.

| Figure 8 | $s_0$ | $I_{vd}$/A | $I_{vq}$/A | $\Delta y/\Omega^{-1}$ | $\langle u_2 \rangle_0$/V (Simulation) | $Y_p/\Omega^{-1}$ (Estimated) | $\langle u_2 \rangle_0$/V (Calculated) |
|----------|-------|------------|------------|----------------------|----------------------|----------------------|----------------------|
| (a)      | 0.002 | 40.8       | 0          | 0                    | −12.6                | 0.0052               |                      |
| (b)      | −0.002| 40.8       | 0          | 0                    | 12.6                 | 12.6                 |                      |
| (c)      | 0.001 | 40.8       | 0          | 0                    | −6.5                 | −6.3                 |                      |
| (d)      | 0.004 | 40.8       | 0          | 0                    | −25.0                | −25.2                |                      |
| (e)      | 0.004 | −40.8      | 0          | 0                    | 6.2                  | 0.0241               |                      |
| (f)      | 0.004 | −40.8      | 0          | 0.00082              | −0.3                 | 0                    |                      |
| (g)      | 0.01  | 0          | 40.8       | 0                    | 0.3                  |                      |                      |
| (h)      | 0.02  | 0          | 40.8       | 0                    | 0.6                  |                      |                      |
From Figures 6a and 8a–d, it can be obtained that \( s_0 \) is proportional to \( \langle u_2 \rangle_0 \) with an opposite polarity. From Figure 8d,e, it can be obtained that \( I_{vd} \) influences \( \langle u_2 \rangle_0 \) with an opposite polarity. From Figure 8g,h, it can be obtained that \( I_{vd} \) has no influence on \( \langle u_2 \rangle_0 \). Thus, the relationships between \( \langle u_2 \rangle_0 \) and \( I_{vd} \), \( I_{eq,r} \), and \( s_0 \) all correspond to Equation (39) from Figure 8.

Substituting \( U^* = 380 \text{ V}, \Delta y = 0, s_0 = 0.002, I_{vd} = 40.8 \text{ A}, \) and \( \langle u_2 \rangle_0 = -12.6 \text{ V} \) from Figure 8a into Equation (39), the estimated value of \( Y_p \) can be derived as

\[
Y_p = -\frac{6s_0I_{vd}}{\pi \langle u_2 \rangle_0} + Y_{p1} + Y_{p2} \bigg/ 2 = 0.0052 \Omega^{-1}
\]  

From this value, the calculated values of \( \langle u_2 \rangle_0 \) in Figure 8b–d can be derived, as shown in Table 5. It can be observed that the simulation values and calculated values are very close, which verifies Equation (39) by a quantitative relationship when \( s_0 \neq 0 \).

Substituting \( U^* = 380 \text{ V}, \Delta y = 0, s_0 = 0.004, I_{vd} = -40.8 \text{ A}, \) and \( \langle u_2 \rangle_0 = 6.2 \text{ V} \) from Figure 8e into Equation (39), the estimated value of \( Y_p \) can be derived as

\[
Y_p = -\frac{6s_0I_{vd}}{\pi \langle u_2 \rangle_0} + Y_{p1} + Y_{p2} \bigg/ 2 = 0.0241 \Omega^{-1}
\]  

From this value, the calculated values of \( \langle u_2 \rangle_0 \) in Figure 8f can be derived, as shown in Table 5. From Figure 8e,f, it can be observed that the balancing control can be realized based on the combined action of the injected zero-sequence voltage and active current.

Thus, the accuracy of Equation (39) is sufficiently verified.

5.1.2. DC Voltage Balancing Control

This case study demonstrates the effectiveness of DC voltage balancing control by considering \( I_{vd} \) and \( s_{0\text{max}} = 0.05 \).

Initially the converter is under a steady-state condition with reference currents \( I_{d1} \) and \( I_{q1} \) without DC voltage balancing control. At \( t = 10.0 \text{ s} \) the balancing control has been used. At \( t = 20.0 \text{ s} \) the reference currents have been changed into \( I_{d2} \) and \( I_{q2} \).

Figure 9 shows the waveforms under the traditional balancing control, which do not take the polarity of \( I_{vd} \) into consideration. It can be seen that the potential drift is worsened when the active current is reversed. Figure 10 shows the waveforms under this proposed balancing control. It can be observed that the potential drift is regulated within a narrow range even in response to the current reversal.

![Figure 9. Cont.](image)
Figure 9. Waveforms without considering the polarity of $I_{vd}$. (a) DC voltages. (b) The instruction value $s_0$.

Figure 10. Waveforms when considering the polarity of $I_{vd}$. (a) DC voltages. (b) The instruction value $s_0$.

Figure 11 shows the waveforms without considering the amplitude of $I_{vd}$. It can be seen that the potential drift has been controlled within a certain range. However, the first parameters are much larger when the reference currents have been changed. The instruction value $s_0$ swings between $-0.05$ to $0.05$. Figure 12 shows the waveform under this proposed balancing control with dynamic adjusting parameters by taking the amplitude of $I_{vd}$ into consideration. The instruction value $s_0$ can converge rapidly in Figure 12.
Figure 11. Waveforms without considering the amplitude of $I_{cd}$. (a) DC voltages. (b) The instruction value $s_0$.

Figure 12. Waveforms when considering the amplitude of $I_{cd}$. (a) DC voltages. (b) The instruction value $s_0$. 
Thus, compared with the traditional balancing control, the effectiveness of DC voltage balancing control with considering \( I_{d1} \) has been verified.

5.2. Experimental Verification

As depicted in Figure 13, the experimental platform was set up. Converter I and II have a common DC link, where converter I is used to supply the DC voltage source, and converter II is used to validate the effectiveness of the model and voltage balancing control. Two signals are used to transfer the converters’ running state directly. If one converter is working, the other should work immediately, and vice versa.

The control blocks of converter I and II are the same and are shown in Figure 5. The reference current \( I_d \) of converter I comes from the DC voltage stable control, which is used to maintain DC link stability. The reference currents of converter II are set from the human machine interface (HMI). The two converters use the same module with the same parameters of \( U^* = 380 \) V, \( L_s = 0.3 \) mH, \( R_1 = R_2 = 24 \) k\( \Omega \), \( C_1 = C_2 = 10,000 \) uF, and carrier frequency \( f_c = 9.6 \) kHz.

The control board shown in Figure 14 is composed of an advanced risc machine (ARM) processor and field programmable gate array (FPGA). The arm processor is used to realize the calculation of root mean square (rms) values, system-level protection, running processes, and communicating with HMI. The sample module, digital phase-locked loop (DPLL), current control, and DC voltage control are realized in the FPGA. The realization diagram of the control system is shown in Figure 15.

The control board shown in Figure 14 is composed of an advanced risc machine (ARM) processor and field programmable gate array (FPGA). The arm processor is used to realize the calculation of root mean square (rms) values, system-level protection, running processes, and communicating with HMI. The sample module, digital phase-locked loop (DPLL), current control, and DC voltage control are realized in the FPGA. The realization diagram of the control system is shown in Figure 15.

The control boards shown in Figure 14 are composed of an advanced risc machine (ARM) processor and field programmable gate array (FPGA). The arm processor is used to realize the calculation of root mean square (rms) values, system-level protection, running processes, and communicating with HMI. The sample module, digital phase-locked loop (DPLL), current control, and DC voltage control are realized in the FPGA. The realization diagram of the control system is shown in Figure 15.

The control board shown in Figure 14 is composed of an advanced risc machine (ARM) processor and field programmable gate array (FPGA). The arm processor is used to realize the calculation of root mean square (rms) values, system-level protection, running processes, and communicating with HMI. The sample module, digital phase-locked loop (DPLL), current control, and DC voltage control are realized in the FPGA. The realization diagram of the control system is shown in Figure 15.
Figure 15. Realization diagram of the control system.

Figure 16 shows the waveforms of the system voltage $u_a$, output current $i_q$ of converter II, DC-side up and lower voltages $U_{II1}$ and $U_{II2}$ without the DC voltage balancing control. The reference currents are $I_d^* = I_q^* = 50$ A. From Figure 16b, it can be seen that there is deviation, and $(u_2)_0 = 5$ V, which means that the upper loss is smaller than lower loss, $\Delta y < 0$.

![Waveform Image](image_url)

Figure 16. Waveforms without balancing control. (a) Waveforms of $u_a$ and $i_a$. (b) Waveforms of $U_{II1}$ and $U_{II2}$.

In order to verify the relationship between $(u_2)_0$ and $\Delta y$, an external resistor $R_e = 8$ k$\Omega$ is used. Figure 17 shows the waveforms of $U_{II1}$ and $U_{II2}$ when $R_e$ is connected. From Figure 17a, it can be seen that the deviation becomes smaller when the resistor connected from point $P_2$ to $O_2$ increases the upper-side loss. From Figure 17b, it can be seen that the deviation becomes bigger when the resistor connected from point $N_2$ to $O_2$ increases the lower-side loss. This relationship corresponds to Equation (39).
In order to verify the relationship between $\langle u_2 \rangle_0$ and $\Delta \zeta$, an external capacitor $C_{add} = 10,000 \text{ uF}$ was used. Figure 18 shows the waveforms of $U_{II1}$ and $U_{II2}$ when $C_{add}$ is connected. From this figure, it can be seen that the deviation is nearly stable when the capacitor is connected, which corresponds to Equation (39). It also can be found that $C_{add}$ affects the amplitude of the third component.

Figure 18. Waveforms of $U_1$ and $U_2$ with an additional capacitor. (a) Connected from $P_2$ to $O_2$. (b) Connected from $N_2$ to $O_2$.

In order to validate the effectiveness of voltage balancing control, the current reference values were changed, and the waveforms of $U_1$ and $U_2$ are shown in Figure 19. From this figure, it can be seen that the balancing control considering $I_{cd}$ works very well.

Figure 19. Cont.
Under traditional balancing control, the control effect is nearly the same if the reference currents are the same over the entire time. If the polarity of $I_{cd}$ is changed, equipment will stop working because DC overvoltage is protected.

6. Conclusions

A simple and direct, but very interesting and valuable, model of neutral-point potential in three-level NPC converters is proposed. From this model, simulation and experiment, some conclusions can be drawn from this model, as follows:

1. The basic reason for the neutral-point potential drift is the uneven shunt loss caused by parametric perturbation, and the capacitance error has no influence on it.
2. Zero-sequence voltage can be used to control the potential drift with the combination of the active current of the converter.
3. The total shunt loss, which is related to the output voltages and currents of the converter, is inversely proportional to the stable drift potential value.
4. The total DC capacitance has no influence on the stable drift potential value, but it affects the dynamic performance and amplitude of the third component.

Future work will focus on NPC converters with a higher number of levels based on the proposed analysis method.

Author Contributions: M.Z. and Q.W. put forward the main idea of this paper; Y.C. and X.W. assisted with the writing; J.T. performed the simulation; H.Z. and G.L. contributed analysis tools.

Funding: This research work was funded by National Natural Science Foundation of China (No.51407001) and the National key R&D project of China (2016YFB0900405).

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Gui, S.; Lin, Z.; Huang, S. A Varied VSVM Strategy for Balancing the Neutral-Point Voltage of DC-Link Capacitors in Three-Level NPC Converters. Energies 2015, 8, 2032–2047. [CrossRef]
2. Hammami, M.; Rizzoli, G.; Mandrioli, R.; Grandi, G. Capacitors Voltage Switching Ripple in Three-Phase Three-Level Neutral Point Clamped Inverters with Self-Balancing Carrier-Based Modulation. Energies 2018, 11, 3244. [CrossRef]
3. Wu, M.; Song, Z.; Lv, Z.; Zhou, K.; Cui, Q. A Method for the Simultaneous Suppression of DC Capacitor Fluctuations and Common-Mode Voltage in a Five-Level NPC/H Bridge Inverter. Energies 2019, 12, 779. [CrossRef]
4. Son, Y.; Kim, J. A Novel Phase Current Reconstruction Method for a Three-Level Neutral Point Clamped Inverter (NPCI) with a Neutral Shunt Resistor. Energies 2018, 11, 2616. [CrossRef]
5. Kang, K.P.; Cho, Y.; Ryu, M.H.; Baek, J.W. A Harmonic Voltage Injection Based DC-Link Imbalance Compensation Technique for Single-Phase Three-Level Neutral-Point-Clamped (NPC) Inverters. *Energies* **2018**, *11*, 1886. [CrossRef]

6. In, H.C.; Kim, S.M.; Lee, K.B. Design and Control of Small DC-Link Capacitor-Based Three-Level Inverter with Neutral-Point Voltage Balancing. *Energies* **2018**, *11*, 1435. [CrossRef]

7. Celanovic, N.; Boroyevich, D. A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters. *IEEE Trans. Power Electron.* **2000**, *15*, 242–249. [CrossRef]

8. Pou, J.; Pindado, R.; Boroyevich, D.; Rodriguez, P. Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter. *IEEE Trans. Ind. Electron.* **2005**, *56*, 1582–1588. [CrossRef]

9. Rodriguez, J.; Bernet, S.; Steimer, P.K.; Lizama, I.E. A survey on neutral-point-clamped inverters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2219–2230. [CrossRef]

10. Shen, J.; Schroder, S.; Rosner, R.; El-Barbari, S. A comprehensive study of neutral-point self-balancing effect in neutral-point-clamped three-level inverters. *IEEE Trans. Power Electron.* **2011**, *26*, 3084–3095. [CrossRef]

11. Hu, C.G.; Holmes, G.; Shen, W.X.; Yu, X.B.; Wang, Q.J.; Luo, F.L. Neutral-point potential balancing control strategy of three-level active NPC inverter based on SHEPWM. *IET Power Electron.* **2017**, *10*, 1755–4535. [CrossRef]

12. Stala, R. Application of balancing circuit for DC-link voltages balance in a single-phase diode-clamped inverter with two three-level legs. *IEEE Trans. Ind. Electron.* **2011**, *58*, 4185–4195. [CrossRef]

13. Du Toit Mouton, H. Natural balancing of three-level neutral-point clamped PWM inverters. *IEEE Trans. Ind. Electron.* **2002**, *49*, 1017–1025. [CrossRef]

14. Von Jouanne, A.; Dai, S.; Zhang, H. A multilevel inverter approach providing DC-link balancing, ride-through enhancement, and common mode voltage elimination. *IEEE Trans. Ind. Electron.* **2002**, *49*, 739–745. [CrossRef]

15. Pou, J.; Pindado, R.; Boroyevich, D.; Rodriguez, P. Limits of the neutral-point balance in back-to-back-connected three-level converters. *IEEE Trans. Power Electron.* **2004**, *19*, 722–731. [CrossRef]

16. Kanchan, R.S.; Tekwani, P.N.; Gopakumar, K. Three-level inverter scheme with common mode voltage elimination and DC link capacitor voltage balancing for an open-end winding induction motor drive. *IEEE Trans. Power Electron.* **2006**, *21*, 1676–1683. [CrossRef]

17. Wu, D.; Wu, X.; Su, L.; Yuan, X.; Xu, J. A dual three-level inverter-based open-end winding induction motor drive with averaged zero-sequence voltage elimination and neutral-point voltage balance. *IEEE Trans. Ind. Electron.* **2016**, *63*, 4783–4795. [CrossRef]

18. Liu, G.; Wang, D.F.; Wang, M.R.; Zhu, C.; Wang, M.Y. Neutral-Point Voltage Balancing in Three-Level Inverters Using an Optimized Virtual Space Vector PWM With Reduced Commutations. *IEEE Trans. Ind. Electron.* **2018**, *65*, 6996–6996. [CrossRef]

19. Jiang, W.D.; Wang, L.; Wang, J.P.; Zhang, X.W.; Wang, P.X. A Carrier-Based Virtual Space Vector Modulation with Active Neutral-Point Voltage Control for a Neutral-Point-Clamped Three-Level Inverter. *IEEE Trans. Ind. Electron.* **2018**, *65*, 8687–8696.

20. Jiao, Y.; Lee, F.C.; Lu, S. Space vector modulation for three-level NPC converter with neutral point voltage balance and switching loss reduction. *IEEE Trans. Power Electron.* **2014**, *29*, 5579–5591. [CrossRef]

21. Bhat, A.H.; Langer, N. Capacitor voltage balancing of three-phase neutral-point-clamped rectifier using modified reference vector. *IEEE Trans. Power Electron.* **2014**, *29*, 561–568. [CrossRef]

22. Choi, U.M.; Lee, K.B. Space vector modulation strategy for neutral-point voltage balancing in three-level inverter systems. *IET Power Electron.* **2013**, *6*, 1390–1398. [CrossRef]

23. Lyu, J.; Hu, W.; Wu, F.; Yao, K.; Wu, J. Variable modulation offset SPWM control to balance the neutral-point voltage for three-level inverters. *IEEE Trans. Power Electron.* **2015**, *30*, 7181–7192. [CrossRef]

24. Li, J.; Liu, J.; Boroyevich, D.; Mattavelli, P.; Xue, Y. Three-level active neutral-point-clamped zero-current-transition converter for sustainable energy systems. *IEEE Trans. Power Electron.* **2011**, *26*, 3680–3693. [CrossRef]

25. Wu, Y.; Shafi, M.; Knight, A.; McMahon, R. Comparison of the effects of continuous and discontinuous PWM schemes on power losses of voltage-sourced inverters for induction motor drives. *IEEE Trans. Power Electron.* **2011**, *26*, 182–191. [CrossRef]
26. Zhang, D.; Wang, F.; Burgos, R.; Boroyevich, D. Common mode circulating current control of paralleled interleaved three-phase two-level voltage-source converters with discontinuous space-vector modulation. *IEEE Trans. Power Electron.* 2011, 26, 3925–3935. [CrossRef]

27. Hou, C.C.; Shih, C.C.; Cheng, P.T.; Hava, A.M. Common-mode voltage reduction pulse width modulation techniques for three-phase grid connected converters. *IEEE Trans. Power Electron.* 2013, 28, 1971–1979. [CrossRef]

28. Zhang, M.; Chi, B.; Wang, X.; Wang, Q.; Li, G. Study on neutral-point potential control for the NPC three-level converter. In Proceedings of the 2016 IEEE 11th Conference on Industrial Electronics and Applications (ICIEA), Hefei, China, 5–7 June 2016.

29. Schauder, C.; Mehta, H. Vector analysis and control of advanced static Var compensators. *IEE Proc. C-Gener. Transm. Distrib.* 1993, 140, 299–306. [CrossRef]

30. Zhang, M.; Wang, T.; Wang, X.; Wang, Q.; Li, G. Study on Neutral-point Potential Control for the APF Based on NPC Three-level Inverter. In Proceedings of the 2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC), Shenzhen, China, 4–7 November 2018.

31. Yazdani, A.; Iravani, R. A generalized state-space averaged model of the three-level NPC converter for systematic DC-voltage-balancer and current-controller design. *IEEE Trans. Power Deliv.* 2005, 20, 1105–1114. [CrossRef]

© 2019 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).