A low-power 2.4-GHz receiver front-end with a complementary series feedback LNA and a current-reused passive down-converter based on gm-boosted TIA for WSN applications

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Abstract This letter proposes a 2.4-GHz low power WSN RF front-end with high conversion gain and low noise figure. The proposed complementary series feedback low-noise amplifier (LNA) achieves high voltage gain and low NF with low power consumption. In the passive down-converter, a gm-boosted TIA employing local gm-boosted feedback structure is proposed to improve the power efficiency. Fabricated in TSMC 55-nm CMOS technology, the proposed front-end achieves a measured conversion gain of 38 dB, a noise figure of 2.75 dB at 2.4 GHz with the power consumption of 2.9 mW under 1 V power supply voltage and the chip area of 0.63 mm²×0.43 mm².

Keywords: complementary, CMOS, current-reusing, gm-boosted, low power consumption, radio frequency (RF) front-end

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

With the growing demand for the Internet of Things (IoT), receivers that comply with the 2.4 GHz Bluetooth low energy (BLE) standard are one of the most attractive candidates for wireless sensor applications with low power consumption, short-range, high data rate for wearable devices such as smart bracelets and smartphones that require low-power wireless bracelets and smartphones which is noiseless. The input impedance which is noiseless. The input impedance before the active stage and realizes a virtual real part of the output impedance with less power consumption, increasing the output impedance with less power consumption, achieving low NF and low power consumption at the same time. In this structure, a smaller source inductance helps to achieve a lower NF and higher voltage gain. However, restricted by process and parasitic, the inductance is often limited to 0.5 nH.

In this letter, a current-reused complementary series feedback common-source (CS) LNA is proposed. Compared with the conventional series feedback LNA mentioned above, with the same source inductance, the proposed LNA achieves higher voltage gain and lower NF with only half the power consumption. In the passive down-converter, a trans-impedance amplifier (TIA) with sufficiently low impedance is required to improve the linearity and anti-blocking performance. The mainstream TIA structures include OTA feedback structure and common-gate open-looped structure. OTA-based TIA can only provide low input impedance at low frequency for the limited GBW of the loop-gain [26], limiting the out-of-band linearity. Common-gate TIA can provide moderate input impedance over a wide bandwidth. However, the in-band impedance is not sufficiently low to guarantee linearity and conversion gain. This letter presents a gm-boosted common-gate TIA, which increases the CG stage’s effective gm by adding a CS stage across the input and output nodes of the CG stage. Low input impedance at low frequency and moderate impedance at high frequency are achieved simultaneously. Compared with OTA based TIA, the boosted gm reduces the input impedance and increases the output impedance with less power consumption, suppressing out-of-band interference and block signals.

2. Circuit design

2.1 Current reused complementary series feedback low-noise amplifier

The conventional common-source series feedback LNA structure is illustrated in Fig. 1. It realizes a passive voltage gain before the active stage and realizes a virtual real part of input impedance which is noiseless. The input impedance Z_in, noise figure and effective trans-conductance expressions of the traditional single-end architecture are derived...
as Eq. (1), Eq. (2) and Eq. (3) respectively:

\[ Z_{in} = S \cdot L_g + S \cdot L_{\text{min}} + \frac{1}{S \cdot C_0'} + \frac{g_{m0} \cdot L_{\text{min}}}{C_0'} \]  

(1)

\[ F = 1 + \gamma \omega^2 C_0' \cdot L_{\text{min}} + \frac{\omega^2 C_0' \cdot L_{\text{min}}}{g_{m0} R_1} \]  

(2)

\[ G_m = \frac{g_{m0}}{\omega C_0' \cdot R_s} \]  

(3)

As indicated by Eq. (1)-(3), a low noise figure and boosted gain are achieved. In the expression, the \( g_m \) of the transistor \( M_{n1} \) is \( g_{m0} \) and the source inductance \( L_s = L_{\text{min}} \), \( C_0' \) is the sum of \( C_0 \) and transistor \( M_{n1} \) gate-source parasitic capacitance \( C_{gs} \). It can be seen from the above expression that the smaller the \( L_s \), the smaller the noise figure. However, the minimum value of inductance is limited due to process limitations and parasitic.

Fig. 2 shows the circuit schematic of the proposed current reused complementary series feedback common-source LNA with master-slave biasing circuit. In the current-reused LNA, the NMOS \( g_m \) transistor \( M_{n1} \) reuses part of the current of the PMOS \( g_m \) transistor \( M_{p3} \). PMOS and NMOS \( g_m \) transistor share a common gate transistor \( M_{n2} \), which realizes cascode structure for both \( M_{n1} \) and \( M_{n3} \), providing gain enhancement and bandwidth extension. The bias circuit is shown in Fig. 2(b). For the \( g_m \) transistors under deep-submicron processes, the channel length modulation effect is non-negligible. A bias circuit which is the precise copy of the LNA is designed to automatically overcome the PVT variation. The transistor \( M_4 \) and \( M_{p4} \), \( M_3 \) and \( M_{p2} \), and \( M_{n2} \) and \( M_{n3} \) correspond in proportion to the transistor size, so \( M_4 \) corresponds to the current in \( M_{p4} \) in proportion. The NMOS \( g_m \) transistor \( M_{n1} \) is biased by \( V_{bias} \) so that the voltages at two points \( c \) and \( d \) are equal. The DC voltage drop on the LNA’s load resistor \( R_1 \) is around 0.3V. \( R_2 \) is used to provide a dc voltage drop between gate and drain terminals of \( M_{n2} \), making sure the voltage at node a equals node b.

Since the capacitance value of the capacitor \( C_1 \) is relatively large in Fig. 2(a), the input impedance viewed from point \( P_m \) is the parallel connection of the impedance of the PMOS transistor \( M_{p1} \) and the NMOS transistor \( M_{n1} \). The impedance from \( P_m \) to the NMOS transistor \( M_{n1} \) is given in Eq. (4):

\[ Z_m = L_{S1} S + \frac{1}{C_{GS1} S} + \frac{g_{mn} L_{S1}}{C_{GS1}} \]  

(4)

Therefore, the overall input impedance \( Z_{in} \) is the series of the inductive reactance of the inductor \( L_g \) and the parallel of the two impedances \( Z_m \) and \( Z_{p2} \), and \( L_{S1} = L_{S2} = L_s \), \( g_{mn} = g_{mp} = g_m \), \( C_{01}' = C_{01} + C_{gsMn1} \), \( C_{02}' = C_{02} + C_{gsMp1} \), and \( C_{01}' = C_{02}' = C_{0''} \), which is Eq. (5):

\[ Z_{in} = S \cdot L_g + \frac{1}{2S \cdot C_{0''}} + \frac{g_m \cdot L_s}{C_{0''}} \]  

(5)

The impedance matching is achieved through the resonance of the inductor and the capacitor, which implements narrow-band input matching and suppresses out-of-band signals.

A low \( L_s \) is helpful for achieving a low NF and high gain. However, due to the limitation of Q factor and parasitism, a practical \( L_s \) can’t be arbitrarily small. To emphasize the advantages of the proposed structure in comparison with the traditional single-ended structure. Assuming the source inductances of the single-ended structure and the proposed structure are equal: \( L_{S1} = L_{S2} = L_s = L_{S\text{min}} \). According to Eq. (5), a lower equivalent source inductance of \( L_s/2 \) is obtained. Because of the complementary structure, \( g_{mn} \) and \( g_{mp} \) are 1/2 of the conventional structure. Correspondingly, \( C_0 \) of each branch can be reduced to 1/4 of that in the conventional structure. The noise figure of the proposed complementary structure can be derived as Eq. (6):

\[ F = 1 + \frac{1}{4} \gamma \omega^2 C_0' \cdot L_{\text{min}} + \frac{\omega^2 C_0' \cdot L_{\text{min}}}{4g_{m0} R_1} \]  

(6)

Therefore, the proposed current reused complementary se-
ties feedback LNA architecture achieves a lower noise figure at half the power consumption than the single-ended architecture. As shown in Fig. 2(a), the effective $g_{m}$ of the complementary structure is the sum of the $g_{m}$ values of PMOS trans-conductor $M_{p1}$ and NMOS trans-conductor $M_{n1}$, which is shown as Eq. (7):

$$g_{m} = g_{mn1} + g_{mp1}$$ (7)

In addition, each input branch of the $g_{m}$ stage obtains the passive gain of $1/(\omega C_{gs} R_{s})$, so the overall effective $g_{m}$ of the circuit can be derived as Eq. (8):

$$G_{m} = \frac{g_{mn1} + g_{mp1}}{\omega (C_{gs1} + C_{gs2}) R_{s}} = \frac{2g_{m0}}{\omega C_{o'} R_{s}}$$ (8)

According to the above analysis, $C_{o''}$ is reduced to 1/4 compared with the traditional single-ended structure, which increases the passive gain, making the overall gain doubled. Therefore, the power consumption of the LNA is reduced to half with improved NF and increased voltage gain.

2.2 Mixer with $g_{m}$-boosted common-gate trans-impedance amplifier

Fig. 3 shows the I&Q $g_{m}$ stage and single balanced passive switching pair of the passive mixer. The $g_{m}$ stage adopts a self-biased complementary current reused amplifier structure, in which PMOS and NMOS transistors are used as $g_{m}$ transistors simultaneously to achieve an effective $g_{m}$ value of $g_{mn1}+g_{mp1}$. With the same power consumption, a double $g_{m}$ value is obtained and linearity is improved by carefully choosing the overdrive voltages of NMOS and PMOS $g_{m}$ transistors.

The $g_{m}$-boosted common-gate TIA is shown in Fig. 4, along with the DC offset cancellation circuit and the common-mode feedback circuit. The TIA is based on a $g_{m}$-boosted common-gate amplifier, which increases the effective $g_{m}$ of the CG stage by adding a CS stage across the input and output nodes of the CG stage. Low input impedance at low frequency and moderate impedance at high frequency are achieved simultaneously. The down-converted current flows into the source of the common gate transistor and is converted into output voltage on the load resistor. To guarantee linearity and anti-blocking performance, low input impedance is required. The equivalent impedance of the source of the CG transistor is $1/g_{m}$, and the $g_{m}$ of the CG transistor is boosted by the CS amplifier. The CG transistor and CS amplifier form the negative feedback loop to reduce the input impedance and increase the CG stage’s output impedance. The output current is converted into a voltage signal on the load resistance and transmitted to the subsequent circuit.

The circuit schematic of the TIA is shown in Fig. 4. Because of the symmetrical structure of the circuit, the left half of the circuit of the TIA is analyzed in this section. The input current $I_{in}$ flows into the source of the common gate transistor $M_{16}$. The input and output terminals of the CS stage formed by the transistors $M_8$ and $M_{18}$ are respectively connected to the source and gate of the CG transistor $M_{16}$, forming the $g_{m}$-boost structure. The NMOS transistor $M_{18}$ provides the bias current for the CS stage branch and serves as the load of the CS stage, and the PMOS transistor $M_{8}$ is the $g_{m}$ transistor of the CS stage. The equivalent $g_{m}$ can be derived as Eq. (9):

$$G_{mp16} = [1 + g_{mp8} \cdot (r_{on18}/r_{op8})] \cdot g_{mp16}$$ (9)

The input impedance can be derived as Eq. (10):
\[
R_{in} = \frac{1}{1 + g_{mp8} \cdot \left( \frac{f_{on18}}{f_{op8}} \cdot \frac{1}{\operatorname{Re}C_{p}} \right)} \cdot \frac{1}{j \omega C_{GS}} \tag{10}
\]

It can be seen from Eq. (9) and Eq. (10) that the effective \( g_m \) is greatly increased and the input impedance is significantly reduced, which absorbs more down-converted currents flowing into the TIA, improving the noise figure and conversion gain. Eq. (10) also indicates that, compared with a conventional OTA-based TIA which can only provide low input impedance at low frequency, the proposed TIA can provide lower input impedance over a wider bandwidth range. It is predictable that higher out-of-band linearity can be achieved. The current is converted into the output voltage \( V_{out} \) on the load resistors \( R_1 \) and \( R_2 \). Since the input signal in Fig. 4 is a differential signal, a virtual ground is constructed at the joint point \( \text{VF} \) of the load resistors \( R_1 \) and \( R_2 \). To suppress common-mode signal and supply voltage fluctuations, the common-mode feedback circuit is introduced into the TIA. The output voltages \( V_{out+} \) and \( V_{out-} \) of the TIA are used as the input voltages of the common-mode feedback circuit, which are compared with the reference common-mode voltage \( V_{CM} \). The output of the error amplifier is fed back to \( V_{CMFB} \) so that the common-mode voltage of \( V_{out+} \) and \( V_{out-} \) is stabilized at the voltage \( V_{CM} \).

In the DC offset cancellation circuit, the output voltage of the TIA \( V_{out+} \), \( V_{out-} \) are fed to the RC low-pass filter, obtaining the output DC offset voltage. This voltage is then amplified and filtered again to generate a feedback DC voltage \( V_{FB} \). \( V_{FB} \) is negatively fed back to the DCOC \( g_m \) stage to generate the compensated DC current injecting into the input of the TIA. The DC currents flowing through \( M_{16} \) and \( M_{17} \) of the TIA are neutralized by the feedback loop, so DC offset voltage is eliminated. In the DCOC feedback loop, the error amplifier provide part of the loop gain. To prevent the loop gain from getting too high, the error amplifier that adopts CS amplifier structure with self-biased resistance load achieves moderate DC-gain to ensure stability.

3. Measurement results

The proposed front-end is fabricated in TSMC 55-nm CMOS technology. Fig. 5 shows the die micro-photograph of the die area of 0.63mm\(^2\) x 0.43mm. The on-chip inductor is used for input impedance matching and the source negative feedback inductors of the LNA are made by bonding wires which are not included in the layout. The overall power consumption of the front end at 1V supply voltage is 2.9mW.

Fig. 6 shows the measured conversion gain (CG) and the simulated CG, the measured DSB noise figure (NF) and the simulated DSB NF versus the input frequency. The measured results show that the lowest NF of 2.75dB and the peak gain of 39dB are achieved at 2.4 GHz and the NF is below 3.3 dB and the gain is higher than 37dB in the frequency range of 2.40-2.48 GHz. Due to non-ideal factors such as parasitics and bonding wires, the difference between the measured CG and the simulated CG is less than 4dB, and the NF difference is about 1dB. At the LO frequency of 2.45 GHz, the measured conversion gain versus the input frequency is illustrated in Fig. 7. The peak gain is 38dB at 2.45 GHz with a −3dB bandwidth of 20M. As shown in Fig. 8, the measured input P1 dB is −37 dBm. The linearity of the proposed front end is sufficient for BLE applications.

Table I [27, 28, 29, 30] compares the measured performances of the proposed front-end with the state-of-the-art front-end. [28] and [30] have slightly lower power consumption and higher gain than this work, however, this work achieves the lowest NF. The performances of NF, conversion gain and power consumption are superior to [23, 27] and [29]. Therefore, the proposed front-end achieves the lowest NF with competitive conversion gain and power consumption power.
4. Conclusion

This letter proposes a 2.4-GHz low power WSN RF receiver front-end with high conversion gain and low noise figure with a novel complementary series feedback low-noise amplifier (LNA) and a down-converter based on the \( g_{\text{m}} \)-boosted trans-impedance amplifier (TIA). Compared with a conventional series feedback LNA with the same degenerated inductor, the proposed LNA achieves higher voltage gain and lower NF with only half the power consumption. In the passive down-converter, a \( g_{\text{m}} \)-boosted TIA is proposed to improve the power efficiency of the conventional global-feedback-OTA solution by employing a local \( g_{\text{m}} \)-boosted feedback structure. The TIA also reduces the input impedance at high frequency, suppressing out-of-band interference and block signals. A prototype is designed and fabricated in TSMC 55-nm CMOS technology, which achieves a measured conversion gain of 38 dB, a noise figure of 2.75dB at 2.4 GHz with the power consumption of 2.9mW under 1V power supply voltage and the chip area of 0.63mm\( \times \)0.43mm.

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Fig. 8 The measured input \( P_{1\text{dB}} \).

Table I Comparison with other designs

|                  | [23]-2017 | [27]-2018 | [28]-2018 | [29]-2017 | [30]-2014 | This work |
|------------------|-----------|-----------|-----------|-----------|-----------|-----------|
| Frequency band (GHz) | 2.4       | 2.4       | 0.1-1     | 2.4       | 2.4       | 2.4       |
| Conversion gain (dB) | 42.5      | 30.06     | 28.1      | 55.5      | 25        | 59        |
| DSB NF (dB)       | 10        | 7.68      | 4.2-6.2   | 3.2       | 3.5       | 2.75      |
| \( \left| P_{1\text{dB}} \right| \) (dBm) | NA        | NA        | -22       | NA        | NA        | -37       |
| Power (mW)        | 2.7       | 9.24      | 5.2       | 2.2       | 3.6       | 2.9       |
| Supply Voltage (V) | 1.8       | 1.8       | 1.8       | 1         | 1.2       | 1         |
| CMOS Technology (nm) | 180      | 180       | 180       | 65        | 130       | 55        |
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