Optimal Integration of Capacitor and Distributed Generation in Distribution System Considering Load Variation Using Bat Optimization Algorithm

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Abstract: In this article, an efficient long-term novel scheduling technique is proposed for allocating capacitors in a combined system involving distributed generation (DG) along with radial distribution systems (RDS). We introduce a unique multi-objective function that focuses on the reduction of power loss with the maximization of voltage stability index (VSI) subjected to constraints of equality and inequality systems. Loss sensitivity factor and VSI together are involved in pre-identifying the locations of capacitors and DG. Determination of the optimal size of capacitor and DG is performed by utilizing the Bat algorithm (BA) for all the loads in RDS. The conventional approach considers the medium load of (1.0) condition generally, but the proposed method changes the feeder loads linearly, ranging from light load (0.5) to peak load (1.6) with the value of step size as 1%. BA determines the optimal size of the capacitor and DG for each step load. The curve fitting technique is used for deducing the generalized equation of capacitor size and DG for all conditions of the load with the various loading condition sized by distributed network operators (DNOs). Further, various load models such as industrial, residential, and commercial loads have been considered to show the efficiency of the present approach. Validation of results is performed in different scenarios on a 69-bus test system and on a standard IEEE 33-bus system. The results exhibit improved accuracy with less power loss value, superior bus voltage, and stability of system voltage with a higher rate of convergence.

Keywords: Bat algorithm; distributed generation; capacitor; curve fitting technique; load variation; load models

1. Introduction

Distribution level power losses have risen to a maximum of 13 percent, which could be reduced by optimally selecting and locating the compensating devices [1]. Voltage stability of the radial distribution system (RDS) is yet another challenge, which could also be solved by the above optimal approach [2], thereby improving voltage profile. Distributed generation (DG) is small, scattered generating units integrated with shunt capacitors, which are considered the compensating devices. DG predominantly has a direct...
focus on real power loss, whereas capacitors tackle the problem of loss reduction indirectly by reactive power injection. DGs do not face the transmission loss problem, as it is located near or at the consumer's site. It could be traditional or any other recent renewable energy sources [3,4].

Optimal allocation of such DGs offers many perks, namely reduced power loss, reliability, and improved voltage profile, forming the set of objective functions. The combination of the above objectives is solved using various optimization algorithms as the references therein [5]. Similarly, many such algorithms are employed for optimal allocation of the other compensating device, namely the capacitors as the references therein [6].

Researchers have focused on either solving optimal allocation of capacitors or DG individually. However, very few attempts have considered allocating both capacitors and DG in the RDS simultaneously. The concurrent sitting of capacitors and DG in the RDS includes the benefits of both individual allocations. These include a reduction of real and reactive power loss, operating cost, and pollutant emission and an advance in power quality, system stability, voltage profile, and efficiency. Load balancing and power factor correction are also addressed.

Simultaneous allocation of single/multi-objective optimization problems with various constraints and minima is obtained by various heuristic algorithms. In [7], the authors used an analytical method to allocate both capacitors and DG in the RDS. With power loss reduction being an objective function, PSO [8], BFOA [9], GA [10], and IMDE [11] are utilized by the authors to obtain the minima. Minimization of various indices, which include balancing of load, voltage stability, and mitigation of active power loss, is addressed by an integrated imperialist competitive algorithm with genetic algorithm (ICA/GA) and for addressing the multi-objective problem, a multi-objective differential evolution (MODE) technique is used [12]. Apart from the indices used in [12], parameters such as voltage profile indices, reliability, and investment cost are also minimized by the binary particle swarm optimization algorithm (BPSO) [13]. The authors [14] have performed cost analysis for DG and capacitors with different load models. In [15], the authors considered voltage profile enhancement as the objective function. Further, in [16], the author proposed an integrated technique for solving the multi-objective function utilizing the firefly algorithm (FFA) and backtracking search algorithm (BSA) as a simultaneous optimization technique in locating the DGs and shunt capacitors together. In [17], the authors proposed a fuzzy-GA-method-based simultaneous location of capacitors and a DG optimization technique for distribution systems. In [18], a two-stage multi-objective fuzzy-based grasshopper optimization algorithm (GOA) is proposed for allocating capacitors, DGs, and charging stations for electric vehicle (EV) distribution systems.

Further, the authors utilized passive harmonic filtering to grow PV hosting capacity in distorted distribution systems with various constraints [19]. A combination of a hybrid phasor particle swarm optimization and gravitational search algorithm was implemented to solve the optimal allocation of inverter-based DG and shunt capacitors in the distribution network [20]. Soft open points and DG are considered along with network reconfiguration for loss mitigation of a 83-node balanced distribution system and IEEE 33 RDS [21]. A multi-objective function has been taken to solve the simultaneous allocation of DG and capacitors with the recent thief and police algorithm [22]. Two operation modes, grid-connected and islanded, for a micro grid with switched capacitors are implemented in the RDS while considering various load models [23]. New objective interconnection cost mitigation for the allocation of renewable DG and capacitors in the alleviate network was performed using an analytical optimization technique [24].

From observations made in the literature, many researchers have concentrated on the level of loading, ranging from light load and medium load to peak load, the load variations happening in between being unattended. Optimal sizing of the DG and capacitor need to be performed for each and every load condition, because only three level sizing approaches do not give insight into the intermediate loading conditions creating uncertainty during
the minimization of the objective function. Sizing for the in-between levels needs attention, which is addressed in this paper.

The novelty of this paper is as follows:

- A novel technique is proposed for long-term scheduling to optimally allocate DGs and capacitors.
- For the first time, consideration of load variation is given for the allocation problem of capacitors and DGs.
- A framed set of generalized equations using curve fitting techniques to help distribution network operators to choose the exact size of the DG and capacitor for any load (light load to peak load).
- The present approach is verified on three different load models to check the efficiency in all types of loads.
- Improvement of overall system efficiency is achieved by considering a multi-objective function for the enhancement of stability and reduced power loss, which are not considered previously in the literature for the allocation of capacitors simultaneously.
- For the first time, the Bat algorithm is applied for the allocation of capacitors and DGs.

This paper proposes a novel approach for solving the problems in allocating the DG and capacitor simultaneously in RDS with various load models. The objective of the system is to reduce the power loss and to enhance the VSI of the system. The Bat algorithm is used for sizing and locating both capacitor and DG. Linear changing of feeder loads is performed ranging from 0.5 (light load) to 1.6 (peak load) with a step size of value 0.01, where at each step, sizing is performed using CFT whose formulation is performed in the form of a simple quadrature equation. The present approach is supportive in the selection of a particular size of capacitor and DG based on distribution network operators (DNOs) and their load steps. The standard IEEE 33-bus test system and 69-bus benchmark test system are used to test the effectiveness and feasibility. Comparison of the simulated results is performed with that of other heuristic-based algorithms.

2. Load Models and Formulation of the Proposed Objective Function

2.1. Formulation of Load Models

From a practical perspective, the current methodology is receptive to joining continuous voltage needy load models. To quantify the impact of a few load models on compensator (DG and capacitor) sizing, static load models are utilized to imply various kinds of purchasers. Mostly, the load of the distribution system can be partitioned into three classifications i.e., industrial, residential, and commercial load. In view of the load types, the active and imaginary power values will fluctuate, which influences the voltage and frequency of the system. In this current work, the voltage-dependent load models, for instance, industrial, residential, and commercial load models, have been thought of. The numerical articulation for the voltage-dependent load model is addressed as:

\[ P = P_o V^\alpha \]
\[ Q = Q_o V^\beta \]

where \( P \) and \( Q \) are the values of real and reactive powers, respectively; \( P_o \) and \( Q_o \) are the values of active and reactive powers at nominal voltages, respectively; and \( \alpha \) and \( \beta \) are the real and reactive power exponents. In Table 1, the values of the real and reactive exponents that are used in this paper for constant power, industrial, residential, and commercial loads have been provided [25–27].
2.2. Power Loss in RDS

Generally, the resistance to reactance ratio of RDS (R/X) is high such that the study of conventional power flow is inappropriate over the transmission system for identification of line voltage and flow. Hence, the backward/forward sweep (BFS) algorithm is utilized for load flow calculations [28]. The BFS algorithm became common owing to its simplicity, fastness, and robustness with the requirement of low memory for processing. In addition, it is well suited for unbalanced distribution networks. In BFS, the three basis steps involved are backward sweep, Nodal current calculation, and forward sweep, which are repeated until convergence.

Two buses are considered, as shown in Figure 1, where these two buses are connected by a branch, the sending end bus is represented as \( t \), and the receiving end bus is represented as \( t + 1 \). Real power represented by \( P_{t,t+1} \) and the reactive power represented by \( Q_{t,t+1} \) that are flowing between bus \( t \) and bus \( t + 1 \) are derived by applying the formulae given as follows:

\[
P_{t,t+1} = P_{(t+1)\text{eff}} + P_{\text{Loss}(t,t+1)}
\]

\[
Q_{t,t+1} = Q_{(t+1)\text{eff}} + Q_{\text{Loss}(t,t+1)}
\]

![Figure 1. Sample distribution system.](image)

Computation of \( I \) between buses \( t \) and \( t + 1 \) in the line section is performed as follows:

\[
I_{t,t+1} = \left( \frac{P_{t,t+1} - jQ_{t,t+1}}{V_{t+1} \angle - \alpha_{t+1}} \right)
\]

Additionally,

\[
I_{t,t+1} = \left( \frac{V_{t} \angle \alpha_{t} - V_{t+1} \angle \alpha_{t+1}}{R_{t,t+1} + jX_{t,t+1}} \right)
\]

Equating and cross-multiplying Equations (5) and (6), we obtain:

\[
V_{t}^2 - V_{t}V_{t+1} \angle (\alpha_{t+1} - \alpha_{t}) = (P_{t,t+1} - jQ_{t,t+1})(R_{t,t+1} + jX_{t,t+1})
\]

Further simplification of Equation (7) leads to:

\[
V_{t}V_{t+1} \angle (\alpha_{t+1} - \alpha_{t}) = V_{t}^2 - (P_{t,t+1}R_{t,t+1} + Q_{t,t+1}X_{t,t+1})
\]

\[
V_{t}V_{t+1} \angle (\alpha_{t+1} - \alpha_{t}) = Q_{t,t+1}R_{t,t+1} - P_{t,t+1}X_{t,t+1}
\]
Squaring and adding (8) and (9)

\[ V_{t+1}^2 = V_t^2 - 2(P_{t+1}R_{t+1} + Q_{t+1}X_{t+1}) + \left( R_{t+1}^2 + X_{t+1}^2 \right) \left( \frac{P_{t+1}^2 + Q_{t+1}^2}{|V_t|^2} \right) \]  \hspace{1cm} (10)

Computation of real power loss is performed in the line section using Equation (5) as follows:

\[ P_{\text{Loss}(t+1)} = I_{t+1}^3 * R_{t+1} \]  \hspace{1cm} (11)

\[ P_{\text{Loss}(t+1)} = \left( \frac{P_{t+1}^2 + Q_{t+1}^2}{|V_{t+1}|^2} \right) * R_{t+1} \]  \hspace{1cm} (12)

The total real power loss \( P_{\text{TL}} \) is obtained by computing the summation of all the losses occurring in the line sections specified by:

\[ P_{\text{TL}} = \sum_{t=1}^{nb} P_{\text{Loss}(t+1)} \]  \hspace{1cm} (13)

where \( nb \) represents the total number of branches.

2.3. Reduction of Power Loss by Placement of DG/capacitor

Real power loss is predominant in RDS. This being the case, the focus of the allocation is to reduce the real power loss. Total power loss in the line section due to DG/capacitor allocation is represented as the ratio between total power loss with DG/capacitor allocation and without DG/capacitor allocation,

\[ P_{\text{DG/Cap} \text{TL}} = \frac{P_{\text{DG/Cap} \text{TL}}}{P_{\text{TL}}} \]  \hspace{1cm} (14)

Reduction of \( \Delta P_{\text{DG/Cap} \text{TL}} \) forms one of the objectives during optimization.

2.4. Voltage Stability Index (VSI) in RDS

Maintaining the voltages of all network buses in spite of disturbance forms the crux of voltage stability. This is solely because of the scarce reactive power supply provided by the system to the loads. VSI for the distribution system shown in Figure 1 is obtained by the power flow method using Equation (8), as introduced in [29].

\[ \text{VSI}(t+1) = |V_t|^4 - 4(P_{t+1,eff}X_{t+1} - Q_{t+1}R_{t+1})^2 - 4 \left( P_{t+1,eff}R_{t+1} + Q_{t+1,eff}X_{t+1} \right) |V_t|^2 \]  \hspace{1cm} (15)

For stable operation of RDS, we should have:

\[ \text{VSI}(t+1) \geq 0, \text{for} \ t = 1, 2, 3 \ldots nb \]  \hspace{1cm} (16)

The above Equation (15) can be used to determine the location of the compensating devices as well as the stability. Upon ordering the VSIs of all the buses, the node corresponding to the minimum VSI is the most sensitive node.

2.5. VSI Maximization Using DG/capacitor Placement

Ignoring voltage stability during formalization of objective function makes RDS susceptible to a bad voltage profile. Maintaining a good voltage profile refers to the pertinence of voltage within limits, meeting the contractual obligations, saving the cost of resources of generation, and finally providing good voltage regulation on the grid. This makes the inclusion of VSI in optimization inevitable [18]. In fact, allocating the DG and capacitor simultaneously improves stability. The change in VSI is given by the ratio of VSI...
with DG/capacitor placement over VSI without DG/capacitor placement, as given in (15). This could be maximized during optimization.

\[
\Delta V_{\text{SI}}^{\text{DG/Cap}} = \frac{V_{\text{SI after}}^{\text{DG/Cap}}}{V_{\text{SI before}}^{\text{DG/Cap}}}
\]  

(17)

2.6. Curve-Fitting Technique

Curve fitting is the process of constructing a curve or mathematical function that has the best fit to a series of data points, possibly subject to constraints [30]. The steps involved in the curve-fitting technique for the proposed method are given below:

1. Place the suggested initial (extreme) DG/capacitor sizes one at a time at bus \( t \). Then, run the load flow per DG capacitor size for all load factors (0.5 to 1.6 with step size of 0.01).
2. Register the \( \Sigma P_{\text{Loss}} \) values of these DG/capacitors individually on a scatter plot. The x and y axes are the total system power loss or DG/capacitor size and load factor, respectively.
3. Plot a quadratic fitted curve of these registered results and obtain the curve function \((ax^2 + bx + c)\).
4. Find the x-intersect \((x = -b/2a)\) of the minimum point at that curve. Then, represent that intersection as the best power loss or DG/capacitor size.
5. Place the designated DG/capacitor size and run the power flow. If the constraints are within the limits, that is, this is the best DG/capacitor option of this pf, then print the results. Otherwise, one of three scenarios could arise:
   a. \(|V_t| > |V_{t_{\text{min}}}^{\text{min}}|\) and \(|V_t| > |V_{t_{\text{max}}}^{\text{max}}|\) reduce the DG/capacitor size by 5% and follow step 5.
   b. \(|V_t| < |V_{t_{\text{min}}}^{\text{min}}|\) and \(|V_t| < |V_{t_{\text{max}}}^{\text{max}}|\) increase the DG/capacitor size by 5% and follow step 5.
   c. \(|V_t| < |V_{t_{\text{min}}}^{\text{min}}|\) and \(|V_t| > |V_{t_{\text{max}}}^{\text{max}}|\) increase and decrease the DG/capacitor size by 5% and follow step 5 for both DGs and capacitors one at a time. If both DGs and capacitors satisfy the constraints, retain the one that provides maximum objective function values.

2.7. Proposed Objective Function

The multi-objective function formulated here works on both VSI and real power loss such that it maximizes VSI and minimizes the real power loss. The proposed multi-objective function for optimal DG is given below. Capacitor placement constraints are given in Table 2.

\[
\text{Minimize}(F) = \text{Min} \left( \frac{\Delta P_{TL}^{\text{DG/Cap}}}{\Delta V_{\text{SI}}^{\text{DG/Cap}}} \right)
\]  

(18)

| Table 2. Constraints for optimization. |
|---------------------------------------|
| Constraints                        | Type     | Equations \((t = 1, 2, \ldots, nb)\) |
| Power balance constraints           | Equality | \( P_{TL} + \sum_{t} P_{D(t)} = \sum_{t} P_{\text{DG/Cap}(t)} \) |
| Voltage constraint                  | In-equality | \( V_{t_{\text{min}}}^{\text{min}}|V_t^{\text{max}}| \) |
| Real power compensation             | In-equality | \( P_{\text{DG}(t)}^{\text{min}}|P_{\text{DG}(t)}^{\text{max}}| \) |
| Reactive power compensation         | In-equality | \( Q_{\text{Cap}(t)}^{\text{min}}|Q_{\text{Cap}(t)}^{\text{max}}| \) |
3. Sensitivity Analysis

Sensitivity analysis is utilized to identify the optimum site for placement of the DG/capacitor. Space-time complexity during optimization is met by the locations obtained using the above analysis.

3.1. Voltage Stability Index

The aim of VSI is to find the optimal location of DG along with the level of security of the system [19]. The ode corresponding to the lowest VSI obtained using (15) has the highest priority of DG placement. Additionally, VSI should be maximized to avoid voltage collapse.

3.2. Loss Sensitivity Factor

Optimal locations for capacitors are obtained from LSF [31,32], which reduces the search space during optimization. The bus with the highest LSF obtains a higher chance of capacitor allocation. The expression for LSF is obtained by differentiating Equation (12) with respect to reactive power.

\[
\text{LSF}(t, t+1) = \frac{\partial P_{\text{Loss}}(t+1)}{\partial Q_{t+1,\text{eff}}} = \left(\frac{2Q_{t+1,\text{eff}} * R_{t+1}}{|V_{t+1}|^2}\right)
\]  

(19)

4. Bat Algorithm

In the present scenario, nature-inspired algorithms have gained attention and eventually became a powerful tool to solve complex power system optimization problems easily. A recent meta-heuristic algorithm, “Bat Algorithm”, is proposed by Xin-She Yang in 2010 [33], which is based on the behavior of natural bats using echo signals for locating their food sources. Bats have an interesting way of determining obstacles even in complete darkness by radiating sound waves from their wings. Such auditory behavior is present in very few species.

BA is developed by depicting the characteristics of bats, which are categorized by three rules as given below:

1. Every bat senses the distance and sizing of the food/prey and background obstacles by echolocation, and it can also differentiate between them.
2. In the process of preying, each bat flies arbitrarily with velocity of \( v_i \) considered at a position \( x_i \), with a least frequency of \( f_{\text{min}} \) whose wavelength varies as \( \lambda \) and value of loudness is \( A_0 \). Frequency or the wavelength is determined by target proximity and pulse emission rate \( r \), whose value ranges between \([0, 1]\), happening inherently.
3. The value of loudness varies between a range from a large positive value \( A_0 \) to a least constant value \( A_{\text{min}} \).

Parameters of BAT Algorithm

- Population size: 20
- Number of generation: 50
- Dimension of search space: 6
- Loudness: 0.5
- Pulse rate: 0.5

The steps involved in the process of allocation of DG and capacitor using BA are given as follows.

Step 1: Set the objective function.
Step 2: Initialize the bat population (10 to 40) with variables: \( v_i, x_i, f_{\text{min}}, r \) and \( A_0 \).
Step 3: Computation of fitness value is performed for each bat and then ranking is performed.
Step 4: Update the variables \( v_i, x_i, f_{\text{min}}, r \) and \( A_0 \) by following Equations (20)–(24).

\[
f_i = f_{\text{min}} + (f_{\text{max}} - f_{\text{min}})\beta
\]  

(20)
\[ v_i^t = v_i^{t-1} + \left( x_i^{t-1} - x^\ast \right) f_i \]  
(21)

\[ x_i^t = x_i^{t-1} + v_i^t \]  
(22)

\[ A_i^{t+1} = \tau A_i^t \]  
(23)

\[ R_i^{t+1} = r_i^0 \left[ 1 - \exp(-\gamma t) \right] \]  
(24)

Step 5: If \((\text{rand} > r_i)\).

Then, a solution is taken from the available best solutions, based on which a local solution is produced, which is around the best solution, selected using Equation (25):

\[ x_{\text{new}} = x_{\text{old}} + \epsilon A^t \]  
(25)

and if

A new solution is generated by flying in a random fashion.

Step 6: if \((\text{rand} < A_i \& f(x_i) < f(x^\ast))\).

Then, the new solutions are accepted.

Step 7: Computation of the fitness value of each bat is performed.

Step 8: Steps 4 to 6 are repeated until the loop ends into a criterion stopping it.

5. Simulation Results and Discussion

The value of voltage sensitivity characterizes the load models of the distribution system as constant voltage/power/impedance. The constant power load model in [34] is considered for simulation. The BFS algorithm is utilized to obtain the power loss of the uncompensated system, VSI, LSF, and bus voltages. The minimum and maximum limits of DG and capacitor sizes are 10% and total 100% of the loading in KW and kVAR of the network, respectively. The maximum number of DG/capacitor banks can be three, and the placement is limited to three, after which no improvement in objective function value is observed. No-load to full-load variation is obtained using the following equation:

\[ P_{t,\text{new}} + j Q_{t,\text{new}} = \partial (P_t + j Q_t) \text{ Load factor} \partial = 0.5, 0.51, 0.52, \ldots 1.6 \]  
(26)

The efficiency of the present approach is validated, and then it is implemented on the standard IEEE 33-bus as well as using 69-bus test systems in the MATLAB simulation platform. For both 33-bus and 69-bus test systems, the feeder loads are varied linearly from 50% (light load) to 160% (peak load) with a step size of 1% increasing every time. The optimal sizes of DG and capacitor for all load steps are calculated by BA.

The efficiency of the proposed methodology is analyzed based on four different cases on the IEEE 33- and 69-bus test systems, respectively. They are represented as follows:

- System without involving compensation
- System considering capacitor
- System considering DG
- System considering both DG and capacitor

5.1. Test System Using IEEE 33-Bus

This test system is considered as a medium scale RDS that comprises 33 buses and 32 branches. Base voltage and apparent base power are obtained as 12.66 kV and 10 MVA, respectively. The adoption of line and bus is performed from [20]. IEEE 33-bus RDS with its single line diagram is represented in Figure 2.
Analysis is performed with and without compensation, the former case being together and individual placement of DG and capacitor.

5.1.1. System without Compensation

The computation of the active power loss of the system is performed by running the load flow algorithm. The value of base case power loss is obtained as 210.98 kW, and minimum voltage is obtained as 0.9037 p.u.

CFT is utilized for obtaining the approximated base real power loss of the 33-bus test system, given as (27):

\[ P_{\text{loss}}(kW) = 302.6\delta^2 - 136.8\delta + 45.21 \]  

(27)

5.1.2. System with Capacitor

In this scenario, one optimally sized capacitor is placed at every optimal location found using sensitivity analysis. Optimal locations obtained are the 14th, 24th, and 30th buses. Mitigation of power loss is performed to 138.35 from 210.98 kW, whereas VSI\textsuperscript{min} is maximized from a value of 0.6610 to 0.7423 p.u. Optimal DG and capacitor sizes for different load factors at optimal locations obtained using BA are shown in Figure 3a,b, respectively. Total active power loss with capacitor is formulated by CFT:

\[ P_{\text{loss}}^\text{Cap}(kW) = 169.8\delta^2 - 49.46\delta + 21.55 \]  

(28)

Optimum size of the capacitors is given by:

\[ Q_{\text{optimal}}^{14\text{th}(\text{Loc})} (kVAR) = 23.73\delta^2 + 344.7\delta - 27.08 \]  

(29)

\[ Q_{\text{optimal}}^{24\text{th}(\text{Loc})} (kVAR) = 41.27\delta^2 + 500.4\delta - 25.2 \]  

(30)

\[ Q_{\text{optimal}}^{30\text{th}(\text{Loc})} (kVAR) = 39.96\delta^2 + 1000\delta - 27.11 \]  

(31)
5.1.3. System with DG

DGs are optimally sited in three (13th, 25th, and 30th buses) different places. Optimum sizing of the DGs is calculated using BA. Reduction of real power loss occurs whose values are obtained as 72.78 from 210.98 kW, while there is improvement in the least bus voltage 0.9037 to 0.9669 p.u.

Formulated total active and reactive power losses with DG using CFT are given by:

$$P_{DG}^{loss}(kW) = 82.0\delta^2 - 16.1\delta + 4.9$$  \hspace{1cm} (32)

Optimum kW of DG is given by:

$$P_{optimal}^{14th \, Loc}(kW) = 11.65\delta^2 + 760.4\delta - 31.32$$  \hspace{1cm} (33)

$$P_{optimal}^{24th \, Loc}(kW) = 31.77\delta^2 + 1063\delta - 28.16$$  \hspace{1cm} (34)

$$P_{optimal}^{30th \, Loc}(kW) = 35.36\delta^2 + 1030\delta - 29.82$$  \hspace{1cm} (35)

5.1.4. System with DG and Capacitor

Simultaneous allocation of DG and capacitor units in an RDS enhances system effectiveness, reduces the power losses, and increases the bus voltage. The sizing of DGs and capacitors is performed optimally at appropriate buses obtained by BA (Table 3).
Table 3. Results of IEEE 33 RDS (various load models).

| Parameters                  | Constant Load | Industrial Load | Residential Load | Commercial Load |
|-----------------------------|---------------|-----------------|------------------|-----------------|
| Without Compensation       |               |                 |                  |                 |
| (Scenario 1)               | P_{loss}(kW)  | 210.98          | 163.66           | 159.09          | 152.59          |
|                            | VSI_{min}(p.u)| 0.6610          | 0.6987           | 0.7030          | 0.7097          |
|                            | V_{min}(p.u)  | 0.9037          | 0.9162           | 0.9175          | 0.9195          |
| Only Capacitor (Scenario 2)|               |                 |                  |                 |
| P_{loss}(kW)               | 680 (13)      | 240 (13)        | 270 (13)         | 290 (13)        |
| VSI_{min}(p.u)             | 0.7423        | 0.7499          | 0.7621           | 0.7733          |
| V_{min}(p.u)               | 0.9301        | 0.9324          | 0.9360           | 0.9393          |
| Only DG (Scenario 3)       |               |                 |                  |                 |
| P_{loss}(kW)               | 380 (13)      | 580 (13)        | 700 (13)         | 720 (13)        |
| VSI_{min}(p.u)             | 0.8652        | 0.9069          | 0.9174           | 0.9393          |
| V_{min}(p.u)               | 0.9679        | 0.9782          | 0.9787           | 0.9749          |
| Simultaneous DG and Capacitor (Scenario 4) | | | | |
| P_{loss}(kW)               | 380 (13)      | 200 (13)        | 250 (13)         | 250 (13)        |
| VSI_{min}(p.u)             | 0.9601        | 0.9622          | 0.9626           | 0.9680          |
| V_{min}(p.u)               | 0.9970        | 0.9912          | 0.9914           | 0.9923          |

Extraction of power loss from CFT for simultaneous allocation of DG and capacitor is given by:

\[ P_{Loss}^{DG+Cap} (\text{kW}) = 11.99d^2 - 0.11d + 0.067 \]  

(36)

The voltage profile for the above-discussed scenarios under different load variations shown in Figure 4a–d reveals significant improvement in bus voltage when DG and capacitor are located concurrently (10.32%) over individual scenarios (2.92% and 6.99% for capacitor and DG, respectively).

Further, comparison of VSI (per unit values) under different scenarios in a full load condition (Figure 4) goes with the previous inference of providing maximum VSI enhancement while DG and capacitor are placed together (45.24%). VSI enhancement when the capacitor is placed is 12.29% and is 30.89% during DG placement.

Yet another objective function of power loss minimization also yields similar results. Power loss reduction is 34.4%, 65.5%, and 94.42% for capacitor, DG, and simultaneous DG and capacitor placement conditions, respectively (Figure 5). Interestingly, power loss minimization objective attainment is more than the other objective of VSI improvement. Figure 6 represents the VSI-comparison of the 33-bus system at normal load. Scenario 4 gives the best VSI improvement compared to all other scenarios. The power loss reductions of all scenarios are compared and shown in Figure 7. It is evident that there is vast improvement in the reduction of power loss in Scenario 4 of the system, which is better than the other scenarios represented.
all scenarios are compared and shown in Figure 7. It is evident that there is vast improvement in the reduction of power loss in Scenario 4 of the system, which is better than the other scenarios represented.

Figure 4. (a) IEEE 33-test system voltage profile (Scenario-I). (b) IEEE 33-test system voltage profile (Scenario-II). (c). IEEE 33-test system voltage profile (Scenario-III). (d) IEEE 33-test system voltage profile (Scenario-IV).

Figure 5. Comparison of active power loss for various scenarios (IEEE 33-Bus).
Table 3 addresses a notable enhancement in the power loss decrease in all load models when contrasted with the base case. Figure 8a–d show the enhancement in bus voltage under various load models for all considered scenarios. As demonstrated in Figure 8a–d, the voltage at all feeders essentially improved for all load models because of the inclusion of compensators in the RDS. This exhibits that the present strategy is exceptionally precise in discovering the power loss and bus voltage for the system with various load models.
Simultaneous DG and Capacitor (Scenario 4) Optimal kVAr and Sitting

Optimal kW and Sitting

|       | Scenario-1 | Scenario-2 | Scenario-3 | Scenario-4 |
|-------|------------|------------|------------|------------|
| Ploss (kW) | 11.77      | 11.37      | 10.77      | 10.30      |
| % Ploss Reduction | 94.42      | 93.05      | 93.23      | 93.24      |
| VSI min (p.u) | 0.9601    | 0.9622     | 0.9626     | 0.9680     |
| V min (p.u)  | 0.9970     | 0.9912     | 0.9914     | 0.9923     |

To examine the presentation of the present methodology inside and out, it has been applied to various load models. The compensator sizes and sites, power loss, bus voltage, and VSI for all load models are presented in Table 3.

Table 3 addresses a notable enhancement in the power loss decrease in all load models when contrasted with the base case. Figure 8a–d show the enhancement in bus voltage under various load models for all considered scenarios. As demonstrated in Figure 8a–d, the voltage at all feeders essentially improved for all load models because of the inclusion of compensators in the RDS. This exhibits that the present strategy is exceptionally precise in discovering the power loss and bus voltage for the system with various load models.

Figure 8. (a) Bus voltage comparison of IEEE 33-bus test system under constant load. (b) Bus voltage comparison of IEEE 33-bus test system under industrial load. (c) Bus voltage comparison of IEEE 33-bus test system under residential load. (d) Bus voltage comparison of IEEE 33-bus test system under commercial load.

5.1.5. Comparative Analysis

The effectiveness of the proposed methodology is examined by comparison with other algorithms such as intersect mutation differential evolution (IMDE) [11], particle swarm optimization (PSO) [8], the bacterial foraging optimization algorithm (BFOA) [9], the analytical method [7], multi-objective particle swarm optimization (MOPSO) [12], and the binary particle swarm optimization algorithm (BPSO) [13], as tabulated in Table 2. Power loss reduction with minimization of bus voltage has greater improvement in the proposed method compared to other methods in all scenarios. The system with the DG and capacitor shows more significant improvement in VSI than the base case. Using VSI, the voltage stability level of the RDS can be determined such that if the stability level is poor, then appropriate action is taken as a remedy in the proposed method. The authors could not have compared VSI with other methods, due to unavailability. Mitigation of power loss, enhancement of bus voltage, and maximization of VSI are the attributes achieved using BA-based optimization at a higher end over other methods of comparison Table 4.
Table 4. Results of IEEE 33 RDS (Constant Load Model).

| Parameters                        | BA     | IDME [11] | PSO [8] | BFOA [9] | Analytical [7] | FGA [12] | BPSO [13] |
|-----------------------------------|--------|-----------|---------|----------|----------------|----------|-----------|
| Without Compensation             |        |           |         |          |                |          |           |
| \( P_{\text{loss}} \) (kW)       | 210.98 | 210.98    | 210.98  | 210.98   | 210.98         | 210.98   | 210.98    |
| \( V_{\text{min}} \) (p.u)      | 0.6610 | 0.6610    | 0.6610  | 0.6610   | 0.6610         | 0.6610   | 0.6610    |
| \( V_{\text{min}} \) (p.u)      | 0.9037 | 0.9037    | 0.9037  | 0.9037   | 0.9037         | 0.9037   | 0.9037    |
| Only Capacitor Compensation      |        |           |         |          |                |          |           |
| (Scenario-1) \( P_{\text{loss}} \) (kW) | 350 (18) | 350 (18) | 350 (18) | 350 (18) | 350 (18) | 350 (18) | 350 (18) |
| (Scenario-2) \( P_{\text{loss}} \) (kW) | 920 (33) | 920 (33) | 920 (33) | 920 (33) | 920 (33) | 920 (33) | 920 (33) |
| \( V_{\text{min}} \) (p.u)      | 0.9037 | 0.9037    | 0.9037  | 0.9037   | 0.9037         | 0.9037   | 0.9037    |
| Only DG (Scenario-3)             |        |           |         |          |                |          |           |
| (Scenario-3) \( P_{\text{loss}} \) (kW) | 600 (7)  | 600 (7)   | 600 (7) | 600 (7)  | 600 (7)      | 600 (7)  | 600 (7)  |
| (Scenario-4) \( P_{\text{loss}} \) (kW) | 1500 (30) | 1500 (30) | 1500 (30) | 1500 (30) | 1500 (30) | 1500 (30) | 1500 (30) |
| \( V_{\text{min}} \) (p.u)      | 0.9037 | 0.9037    | 0.9037  | 0.9037   | 0.9037         | 0.9037   | 0.9037    |

5.2. Test System Using IEEE 69-Bus

The performance of the BA algorithm is demonstrated by considering the next test system with radial distribution—a large-scale 69-bus that has a total load of 3.80 MW and 2.69 MVAR. Figure 9 illustrates the single line diagram of the IEEE 69-bus test system where this test system also includes line and bus as adopted from [35].

![Figure 9. Single line diagram of IEEE 69-bus system.](image-url)
5.2.1. System without Compensation

BFS is the load flow for computing the uncompensated system power as well as voltage values. In this system, the real losses are obtained to be 225 kW and the reactive power losses are obtained to be 102.13 kVar. The least value of bus voltage without any compensation technique is obtained as 0.9090 p.u, and the VSI least value is obtained as 0.6822 p.u. CFT is utilized to formulate the generalized equation in order to obtain the total real power loss, without any compensation in the case of the IEEE 69-bus system, which is given as follows:

\[ P_{\text{loss}}(kW) = 335.4\delta^2 - 166.5\delta + 55.38 \]  

(37)

5.2.2. System with Capacitor

In this scenario, three optimally sized capacitors at every optimal location identified using sensitivity analysis are located. Optimal locations attained are the 12th, 19th, and 61st buses. Mitigation of power loss is performed to a value of 144.96 kW from a value of 225 kW (i.e., percentage of mitigation is 35.57%); meanwhile, VSI\text{min} is maximized from 0.6822 to 0.7516 p.u. Optimum DG and capacitor sizes for different load factors at optimal sittings attained using the proposed BA optimization algorithm are represented in Figure 10a,b.

![Figure 10. (a) Optimum kVar for capacitor under various load factors (IEEE 69-Bus). (b) Optimum kW for DG under various load factors (IEEE 69-Bus).](image)

Formulation of total real power loss with the effect of a capacitor is performed by CFT for IEEE 69-bus system is given by:

\[ P_{\text{loss}}^C(kW) = 192.7\delta^2 - 71.08\delta + 23.18 \]  

(38)

Locations of the capacitors at the 12th, 19th, and 61st buses with varying load, indicating the optimal size, are given by:

\[ Q^{12th(Loc)}_{\text{optimal}} (kVAR) = 62.23\delta^2 + 327.6\delta - 2.832 \]  

(39)

\[ Q^{19th(Loc)}_{\text{optimal}} (kVAR) = 0.794\delta^2 + 249.6\delta - 14.96 \]  

(40)

\[ Q^{61st(Loc)}_{\text{optimal}} (kVAR) = 53.2\delta^2 + 1179\delta - 6.655 \]  

(41)

DNOs can plan for capacitor sittings using the above equations in distribution networks.
5.2.3. System with DG

Three DG units are placed at the 12th, 19th, and 61st buses using a VSI- and LSF-based sensitive analysis method. Determination of optimal sizes of the DG units is performed using the proposed BA-based optimization techniques. Mitigation of real power loss is achieved as 68.97 kW power from a power value of 225 kW (i.e., percentage of mitigation is 35.57%), while there is improvement in the minimum bus voltage from a value of 0.9090 p.u to a value of 0.9772 p.u.

The total real power and reactive power losses formulated with DG utilizing CFT are given by:

\[ P_{\text{DG}} \, \text{(kW)} = 74.93\delta^2 - 8.414\delta + 2.644 \] (42)

DGs’ optimal sizes for the 12th, 19th, and 61st locations are given by:

\[ P_{\text{optimal} \, 12th (\text{Loc})} (\text{kW}) = \frac{40.02\delta^2 + 498.16\delta - 12.01}{2} \] (43)

\[ P_{\text{optimal} \, 19th (\text{Loc})} (\text{kW}) = \frac{0.851\delta^2 + 366\delta - 15.61}{2} \] (44)

\[ P_{\text{optimal} \, 61st (\text{Loc})} (\text{kW}) = \frac{52\delta^2 + 1664\delta - 12.16}{2} \] (45)

5.2.4. System with DG and Capacitor

In the present scenario, DGs and capacitors are allocated in an optimal way with a sizing option using the proposed BA technique. Figure 11 illustrates the comparison of real power loss for various scenarios considered for variation in load of the test system with 69-bus. Power loss and VSI\text{min} are obtained as 5.01 kW, 0 p.u, and 0.9607 p.u, respectively, using simultaneous allocation of the DG and capacitor.

![Figure 11. Comparison of active power loss for various scenarios (IEEE 69-Bus).](image)

In all the scenarios, the power loss is mitigated in comparison to the base case (without compensation), and in Scenario 4, the largest loss mitigation is exposed, which is 97.77%. Additionally, the VSI and minimum bus voltage have enhanced in all the scenarios compared to the base case, and the largest enhancement is for Scenario 4, which is 0.9972 and 0.9607 p.u, respectively. For different loading conditions, the voltage profile of the 69-bus is represented, as shown in Figure 12a–d. It can be noted from the figures that simultaneous placement of the DG and capacitor in RDS enhances bus voltages meritoriously. From Table 3 and Figure 13, it is evident that the objective function is enhanced to a maximum value whenever the placements of the DG and capacitor are near to each other (Scenario 4). Attaining optimal solutions in Scenario 4 is the most optimal value for objective functions of all scenarios.
Figure 12. (a) IEEE 69-test system voltage profile (Scenario I). (b) IEEE 69-test system voltage profile (Scenario II). (c) IEEE 69-test system voltage profile (Scenario III). (d) IEEE 69-test system voltage profile (Scenario IV).

Figure 13. Comparison of VSI of 69-bus system at normal load.

Extraction of power loss from CFT for simultaneous allocation of DG and capacitor is given by:

$$p_{\text{loss}}^{\text{DG}+\text{C}}(\text{kW}) = 4.99\delta^2 - 0.1052\delta + 0.2131$$  \hspace{1cm} (46)
Figures 7 and 14 also demonstrate the loss mitigation attained by various methods for 33- and 69-bus systems, respectively. These figures evidently indicate that the BA-based optimization technique provides a superior performance to other optimization techniques available in the literature.

Table 5 depicts the loss mitigation, minimum bus voltage, and VSI of the IEEE 69-RDS under various load models. Figure 15a–d show the enhancement in bus voltage profile under various load models of IEEE 69-RDS. As can be seen from Table 5 and Figure 15a–d, the loss mitigation decrease and bus voltage profile of the system at each load model is enhanced after the situation of a compensator in the RDS utilizing BA optimization procedure.

Table 5. Results of IEEE 69-RDS (various load models).

| Parameters                  | Constant Load | Industrial Load | Residential Load | Commercial Load |
|-----------------------------|---------------|-----------------|------------------|-----------------|
| Without Compensation (_scenario 1) |               |                 |                  |                 |
| \( P_{\text{loss}} \) (kW) | 225           | 171.39          | 164.87           | 156.92          |
| \( V_{\text{Smin}} \) (p.u) | 0.6822        | 0.7136          | 0.7211           | 0.7289          |
| \( V_{\text{min}} \) (p.u) | 0.9090        | 0.9196          | 0.9217           | 0.9242          |
| Only Capacitor (Scenario 2) |               |                 |                  |                 |
| \( P_{\text{loss}} \) (kW) | 400 (12)      | 290 (12)        | 300 (12)         | 300 (12)        |
| \( V_{\text{Smin}} \) (p.u) | 230 (19)      | 160 (19)        | 180 (19)         | 190 (19)        |
| \( V_{\text{min}} \) (p.u) | 1237 (61)     | 740 (61)        | 870 (61)         | 900 (61)        |
| \% P_{\text{loss}} Reduction | 144.96        | 140.39          | 123.95           | 112.36          |
| \% V_{\text{Smin}} Reduction | 35.57         | 18.08           | 24.81            | 28.39           |
| \% V_{\text{min}} Reduction | 0.7516        | 0.7490          | 0.7640           | 0.7747          |
| \% V_{\text{min}} Reduction | 0.9327        | 0.9324          | 0.9281           | 0.9242          |
| Only DG (Scenario 3)       |               |                 |                  |                 |
| \( P_{\text{loss}} \) (kW) | 535 (12)      | 460 (12)        | 450 (12)         | 440 (12)        |
| \( V_{\text{Smin}} \) (p.u) | 340 (19)      | 320 (19)        | 310 (19)         | 300 (19)        |
| \( V_{\text{min}} \) (p.u) | 1693 (61)     | 1670 (61)       | 1570 (61)        | 1480 (61)       |
| \% P_{\text{loss}} Reduction | 68.97         | 28.81           | 37.73            | 41.33           |
| \% V_{\text{Smin}} Reduction | 69.34         | 83.19           | 77.11            | 73.66           |
| \% V_{\text{min}} Reduction | 0.9113        | 0.9431          | 0.9357           | 0.9314          |
| \% V_{\text{min}} Reduction | 0.9772        | 0.9857          | 0.9837           | 0.9826          |
| Simultaneous DG and Capacitor (Scenario 4) |               |                 |                  |                 |
| \( P_{\text{loss}} \) (kW) | 300 (12)      | 250 (12)        | 240 (12)         | 240 (12)        |
| \( V_{\text{Smin}} \) (p.u) | 269 (19)      | 170 (19)        | 200 (19)         | 190 (19)        |
| \( V_{\text{min}} \) (p.u) | 1202 (61)     | 730 (61)        | 760 (61)         | 760 (61)        |
| \% P_{\text{loss}} Reduction | 479 (12)      | 460 (12)        | 410 (12)         | 430 (12)        |
| \% V_{\text{Smin}} Reduction | 365 (19)      | 330 (19)        | 300 (19)         | 300 (19)        |
| \% V_{\text{min}} Reduction | 1680 (61)     | 1660 (61)       | 1550 (61)        | 1480 (61)       |
| \% P_{\text{loss}} Reduction | 5.01          | 4.08            | 4.54             | 4.02            |
| \% V_{\text{Smin}} Reduction | 50.107        | 0.9594          | 0.9593           | 0.9593          |
| \% V_{\text{min}} Reduction | 0.9972        | 0.9944          | 0.9944           | 0.9943          |
Compared with all scenarios, the simultaneous allocation of the DG and capacitor (Scenario 4) produces better loss reduction, bus voltage enhancement, and VSI improvement in all load models.

5.2.5. Comparative Analysis of 69-Bus System

The efficiency of the present approach has been tested by the obtained results from the viewpoint of minimum voltage, power loss, and VSI in comparison to all the scenarios with IMDE [11] and PSO [8] as tabulated in Table 6. The compensating device is required to enhance the performance of the distribution network [25–27]. Power loss mitigation with minimal bus voltage enhancement as in the BA-based optimization technique is better than other existing methods in all scenarios [36–43]. The DG and capacitor installed system shows more noteworthy enhancement in VSI than in the base case. The determination of voltage stability level of RDS can be performed using VSI, based on which appropriate action can be taken for the poor value of the index of stability using the proposed method. The authors could not have compared VSI with other methods due to unavailability. Mitigation of power loss, enhancement of bus voltage, and maximization of VSI attributes are achieved using BA-based optimization at the higher end over other methods of comparison (Table 6).
Table 6. Results of IEEE 69-RDS (constant load model).

| Parameters | BA | IDME [11] | PSO [8] |
|------------|----|-----------|---------|
| Without Compensation (Scenario 1) | | | |
| $P_{\text{loss}}$(kW) | 225 | 225 | 225 |
| $V_{\text{S}}$min (p.u) | 0.6822 | 0.6822 | 0.6822 |
| $V_{\text{min}}$(p.u) | 0.9090 | 0.9090 | 0.9090 |
| Only Capacitor (Scenario 2) | | | |
| Optimal kVAR and Sitting | 400 (12) | 375 (21) | N/A |
| $P_{\text{loss}}$(kW) | 230 (19) | 12637 (61) | N/A |
| $V_{\text{S}}$min (p.u) | 0.7516 | N/A | N/A |
| $V_{\text{min}}$(p.u) | 0.9327 | 0.9330 | N/A |
| Only DG (Scenario 3) | | | |
| Optimal kW and Sitting | 535 (12) | 473 (20) | N/A |
| $P_{\text{loss}}$(kW) | 340 (19) | 1730 (61) | N/A |
| $V_{\text{S}}$min (p.u) | 0.9113 | N/A | N/A |
| $V_{\text{min}}$(p.u) | 0.9772 | 0.9808 | N/A |
| Simultaneous DG and Capacitor (Scenario 4) | | | |
| Optimal kVAR and Sitting | 300 (12) | 1192 (61) | 14013 (61) |
| $P_{\text{loss}}$(kW) | 269 (19) | 109 (63) | |
| $V_{\text{S}}$min (p.u) | 479 (12) | 1202 (61) | |
| $V_{\text{min}}$(p.u) | 1730 (61) | 109 (63) | |
| $P_{\text{loss}}$(kW) | 5.01 | 13.83 | 25.9 |
| $V_{\text{S}}$min (p.u) | 97.77 | 93.84 | 88.4 |
| $V_{\text{min}}$(p.u) | 0.9607 | 0.9915 | 0.9700 |

The accuracy of the results reveals that the present approach of BA is an effective and bio-inspired well-organized method able to solve complex problems in optimization. This BA algorithm is suggested based on the accuracy of the results as an accomplished tool of optimization for solving tough problems of optimization in the engineering field for future research works. Figure 13 depicts the comparison of VSI of a 69-bus system at normal load. Scenario 4 gives the best VSI improvement compared to all other scenarios.

The initial data and inflation rate, interest rate, and feeder distribution rate formulas are taken from the references [44–46]. The economic factors such as inflation and interest rate are considered to check the performance of the proposed method. Table 7 presents the initial data of the problem with all necessary parameters. The size of the capacitor and DG is calculated as 1860 kVAR and 2210 kW, respectively. Table 8 shows the savings of the system after compensation. The failure rate of the distribution feeders is analyzed and tabulated in Table 9.

Table 7. Initial data of the problem.

| Investement Cost of Capacitor/DG | Size of Capacitor, kVAR | Size of DG (kW) | Maintenance Cost of Capacitor/DG | Inflation Rate, %/Year | Interest Rate, %/Year | Load Growth, %/Year | Planning Period, Year |
|--------------------------------|-------------------------|----------------|---------------------------------|------------------------|----------------------|----------------------|----------------------|
| 4000                           | 1860                    | 2210           | 400                             | 10                     | 15                   | 1                    | 20                   |
Table 8. Simulation result for base case and Scenario 4.

|                     | Power Loss, kW/pp | Risk Level Mwh/pp | Investment Cost | Maintenance Cost | Cost of Power Loss | Cost of Risk/pp | Total Cost     |
|---------------------|-------------------|-------------------|-----------------|-----------------|-------------------|----------------|---------------|
| Initial status      | 210.98            | 5914              | 0               | 0               | 1,678,415         | 418,874        | 2,457,841     |
| After planning      | 11.77             | 3214              | 26,000          | 2400            | 1,367,845         | 251,745        | 1,744,154     |

Table 9. Distribution feeder failure rate.

|                     | Power Loss, MW/pp | Risk Level Mwh/pp | Investment Cost | Maintenance Cost | Cost of Power Loss | Cost of Risk/pp | Total Cost |
|---------------------|-------------------|-------------------|-----------------|-----------------|-------------------|----------------|------------|
| Amount of error/detriment | 210.98           | 11.77             | −4000           | −2400           | 9784              | 16,487         | 1147       |

6. Conclusions

The proposed approach investigates the integration of DG and capacitor placing and their sizing in the RDS to minimize the power loss and enhance the voltage stability. BA is applied to obtain optimal sizing of the DG and capacitor in the system of RDS. The generalized equation is derived using CFT to facilitate DNOs in the determination of DGs’ and capacitors’ optimal sizes for any particular change of load. The efficiency of the present algorithm is tested on the 33-bus and IEEE 69-bus RDS with four changing scenarios with various load models such as constant, industrial, residential, and commercial load models. Comparison is performed between simulated results with conventional techniques namely IDME, PSO, BFOA, analytical, FGA, and BPSO available in the literature. The attained results demonstrate that the integration of DG and capacitor (Scenario 4) is efficient in mitigation of power loss with enrichment of voltage stability. Additionally, the proposed approach is effective in determining the optimal solution in various scenarios. Thus, based on the results obtained, it is recommended to allocate both the DG and capacitor simultaneously in the distribution system to ensure maximum benefits from the system.

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