Impact of switches resistance on successive approximation of ADC dynamic performance

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Abstract. This paper discusses the degradation of the dynamic performance in switched capacitors based on successive approximation analog-to-digital converters (SAR ADCs), caused by the resistance of the switch, which connects a voltage reference to a common bus of switched capacitor array. Based on the analysis of the phenomenon, the techniques for reducing its influence are shown. They were used in the design of micro-power SAR ADC, which is presented in the paper.

1. Introduction

A successive approximation analog-to-digital converters (SAR ADCs) are widely used due to the low power consumption and relatively simple structure. Modern SAR ADC consists of the following blocks: a digital-to-analog converter (DAC) based on capacitor array, a comparator and a control logic that provide the implementation of successive approximation algorithm and general synchronization.

Figure 1 shows the simplified structure of an 8-bit SAR ADC with input signals in the range from 0 to a full-scale voltage V_{FS}. For clarity, this figure shows an ADC having single-ended input and a single array of switched capacitors in the DAC. It forms the sequence of voltages required for binary search and serves as a sample-and-hold circuit.

In the sampling phase, all capacitors are connected in parallel. Their bottom plates are connected to the source of the input signal, and their top plates are connected to a reference source with a voltage equal to half of a full scale. In the phase of determining the bit values, the bus of the top plates of the capacitors is disconnected from the reference voltage. The bottom plate of each capacitor, starting with the most significant bit (MSB), is connected to the reference source of the full-scale voltage V_{FS}, while the bottom plates of the other capacitors are connected to the ground bus. The comparator determines the values of the bits, comparing the voltage on the top plate bus with a voltage that is equal to half of the scale.

A great number of papers are devoted to the analysis of SAR ADC errors and the methods for reducing them [1–15]. There are many papers, which propose the methods for improving the dynamic performance of these ADCs [16–20]. Despite the large number of publications on this issue, one point concerning the impact of switches resistance on SAR ADC dynamic performance, has not been considered in previous papers. The purpose of this article is an explanation of this phenomenon, its analysis and discussion of techniques for reducing its impact on the performance of ADCs.
2. Analysis of the phenomenon and identifying ways to reduce its impact on ADC dynamic performance

2.1. Summary of phenomenon

Figure 2 demonstrates the effect in question. The essence of this effect is that, because of the resistance between the reference source and the bus of the top capacitor plates, the potential of this bus during the sampling phase does not remain constant. As shown in Fig. 2, the voltage on the bus of the top plates does not accurately match to the voltage of the reference source. It also contains a component proportional to the derivative of the input signal. The attenuated and phase-shifted input signal is applied to the bus through the capacitors of the DAC matrix that are connected in parallel during the sampling phase.

![Image](image_url)

**Figure 1.** Exemplary architecture of 8-bit SAR ADC.

**Figure 2.** Simulated waveforms during the sampling and conversion: (a) input signal; (b) derivative of input signal; (c) output of voltage reference source; (d) voltage at the top-plate bus of capacitor array.

This effect appears as a reference source of output voltage error. This causes a degradation of the parameters of the SAR ADC, including the effective number of bits (ENOB), as the frequency of the input signal increases, as shown in Figure 3. This effect most affects the dynamic performance of ADC, which features a resolution of 12 bits and more.
Figure 3. Simulated plot of ADC effective resolution degradation with increasing the frequency of the input signal.

2.2. Detailed analysis

The equivalent circuit of the capacitive DAC is shown in Figure 4. A capacitor array of the DAC consists of higher-bits and lower-bits sub-arrays, which are connected via an attenuating capacitor $C_a$.

![Figure 4. Simplified AC equivalent circuit of capacitive array and switches during the sampling phase.](image_url)

During a sampling phase, all capacitors are connected in parallel. They are connected between the input source $V_i$ and the reference source $V_r$ through closed switches with resistance $R_g + R_t$. The reference source is connected through a switch with resistance $R_s$ to a top-plate bus of capacitors. The total capacitance of a higher-bits sub-array is $C_t = C_0 (2^n - 1)$, where $C_0$ is the unit capacitance and $n$ is resolution of a higher-bits sub-array. The total capacitance of a lower-bits sub-array with a series capacitor $C_a$ is equal to $C_0$, and the total capacity of DAC capacitor array is $C_s = C_t + C_a = 2^n C_0$.

A voltage transfer ratio from the input signal source to the top-plate bus of the DAC:

$$K_v(f) = K_i \left( \frac{f}{f_0} \right) \left( 1 + \left( \frac{f}{f_0} \right)^2 \right)^{-\frac{1}{2}}, \quad K_i = R_s \left( R_{g} + R_{s} + R_{t} \right)^{-1}, \quad (1)$$

where $f$ – input frequency and $f_0 = [2 \pi C_s (R_g + R_t + R_s)]$. For the input signals frequencies much lower than $f_0$, the transfer ratio is $K(f) \approx K_i f/f_0 = 2 \pi f C_s R_s$. The total capacity of the DAC array and the resistance of the switch that connects the reference source to the top-plate bus determine it. In this approximation, it is independent of the signal source resistance and resistance of DAC switches.
Deviation of the top-plate voltage $V_t$ from the reference voltage $\Delta V = (V_r - V_t)$ causes the relative error in decibels relative to the carrier that is equal to $\delta(f) = 20 \log(\Delta V/V_g) = 20 \log[K(f)]$.

2.3. Methods for improving the dynamic performance of SAR ADC

According to the analysis performed, the effect of the reference switch resistance on the dynamic performance of the ADC can be mitigated both by using a bootstrapped switch, which has a low and stable resistance, and by minimization of the unit capacitor value.

The refined version of the 10-bit SAR ADC utilizes bootstrapped switches to improve dynamic performance. Fig.5 shows the schematic diagram of the bootstrapped switch. The circuit consists of two switches, which are based on a modified known scheme [21–23]. The second dummy switch performs the function of charge injection compensation.

![Figure 5. Schematic diagram of bootstrapped switch with charge injection compensation by a dummy switch.](image)

In addition, the capacitive array of the DAC in a new version of ADC uses a unit capacitor with capacitance reduced to 60 fF. This allowed not only improving the dynamic parameters, but also reducing the ADC power consumption with the maintenance of acceptable linearity and noise performance. Fig. 6 shows implementation details of the finger-type unit capacitor used in the ADC.

![Figure 6. Implementation of the unit capacitor: (a) layout, (b) stack of metal layers.](image)
Fig. 7 illustrates enhancement of ADC dynamic performance achieved by using the proposed techniques. At a sampling rate of 1 MspS and an input signal frequency of 333 kHz, the effective resolution of ADC has been improved from 9.32 bits to 9.85 bits.

![Graph](image1.png)

**Figure 7.** Output spectrum and dynamic performance of (a) prototype ADC and (b) advanced version of ADC with bootstrapped reference voltage switch and smaller capacitances.

A 10-bit SAR ADC using the methods proposed has been implemented in a commercially available 180 nm CMOS process. ADC has low power consumption, which is less than 0.4 mW at a sampling rate of 1 MspS. Fig. 8 shows the layout of the chip core that is inclusive of the capacitor DAC and switch circuitry.

![Layout](image2.png)

**Figure 8.** Layout of capacitor arrays and switches of designed ADC.

### 3. Conclusion
We considered the phenomenon of degradation of the dynamic parameters of the SAR ADC with capacitor DAC due to the influence of the impedance of the reference source, as well as methods for reducing the impact of this effect. A low-power 10-bit ADC with improved dynamic performance was developed using the proposed methods.

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