Efficient and Generic 1D Dilated Convolution Layer for Deep Learning

Narendra Chaudhary  
Intel Labs  
Bangalore, India  
narendra.chaudhary@intel.com

Sanchit Misra  
Intel Labs  
Bangalore, India  
sanchit.misra@intel.com

Dhiraj Kalamkar  
Intel Labs  
Bangalore, India  
dhiraj.d.kalamkar@intel.com

Alexander Heinecke  
Intel Labs  
Santa Clara, California, USA  
alexander.heinecke@intel.com

Evangelos Georganas  
Intel Labs  
Santa Clara, California, USA  
evangelos.georganas@intel.com

Barukh Ziv  
Intel Corporation  
Haifa, Israel  
barukh.ziv@intel.com

Menachem Adelman  
Intel Corporation  
Haifa, Israel  
menachem.adelman@intel.com

Bharat Kaul  
Intel Labs  
Bangalore, India  
bharat.kaul@intel.com

ABSTRACT

Convolutional neural networks (CNNs) have found many applications in tasks involving two-dimensional (2D) data, such as image classification and image processing. These networks use 2D convolution layers, and therefore, 2D convolution layers have been heavily optimized on CPUs and GPUs. However, in many applications—for example genomics and speech recognition, the data can be one-dimensional (1D) or has one dimension significantly longer than the other dimensions. Such applications can benefit from optimized 1D convolution layers. In this work, we introduce our efficient implementation of a generic 1D convolution layer covering a wide range of input tensor widths, filter widths, number of channels, number of filters, and dilation parameters. It is optimized for x86 CPU architectures, in particular, for architectures containing Intel® AVX-512 and AVX-512 BFloat16 instructions. We use the LibXSMM library’s batch-reduce General Matrix Multiplication (BRGEMM) kernel for single-precision (FP32) and brain floating-point (BFloat16) precision. We demonstrate that our implementation can achieve up to 80% efficiency on Intel® Xeon® Cascade Lake and Cooper Lake CPUs. Additionally, we show the generalization capability of our BRGEMM based approach by achieving high efficiency across a range of parameters. We consistently achieve higher efficiency than the 1D convolution layer with Intel® oneDNN library backend for varying input tensor widths, filter widths, number of channels, filters, and dilation parameters. Finally, we demonstrate the performance of our optimized 1D convolution layer by utilizing it in the end-to-end neural network training with real genomics datasets and achieve up to 6.86× speedup over the oneDNN library-based implementation on Cascade Lake CPUs. We also demonstrate the scaling with 16 sockets of Cascade/Coooper Lake CPUs and achieve significant speedup over eight V100 GPUs using a similar power envelop. In the end-to-end training, we get a speedup of 1.41× on Cascade Lake with FP32, 1.57× on Cooper Lake with FP32, and 2.27× on Cooper Lake with BFloat16 over eight V100 GPUs with FP32. Our results demonstrate that software optimizations with Intel® AVX-512, AVX-512 BFloat16 instructions can provide significant performance benefits and scale to deep learning applications.

Code Availability - https://github.com/hfp/libxsmm/tree/master/samples/deeplearning/conv1dopti_layer

KEYWORDS

Deep learning, convolution layer, genomics, efficient hardware optimization

1 INTRODUCTION

Deep learning techniques can extract information from datasets of text, audio, images, and videos. These techniques have significantly improved performance in image classification [8, 15, 18], image denoising [11, 37], and natural language translation [35] problems. Deep learning has become viable due to growth in dataset sizes and computing power. It is increasingly being employed in emerging fields with tremendous growth in dataset sizes, such as computational genomics [16, 27, 28]. It is expected that the computing needs [10, 31] of deep learning algorithms will grow faster than Moore’s law. At the same time, Leiserson et. al. [19] has argued that improvements in software, algorithm, and hardware architecture can provide higher than Moore’s law [21] speedup to applications. Therefore, deep learning algorithms need optimized implementations to keep pace with their computing demands. One of the key computational kernels in deep learning applications is the convolution layer. Deep convolutional neural networks (CNNs) consist of multiple compute-intensive convolution layers. CNNs with two-dimensional (2D) convolution layers have found applications in several image classification [8, 15, 30], denoising [11, 37], superresolution [5, 34], and segmentation [23] tasks. Therefore, GPU/CPU implementations of CNNs have been heavily optimized for two-dimensional (2D) image data.

However, many datasets in nature are one-dimensional (1D) or have one dimension longer than the other dimensions. Audio, speech, text, and genomic sequencing datasets are some examples...
of 1D datasets. Deep learning applications involving 1D datasets frequently utilize 1D CNNs [12]. 1D CNNs have been used for large scale audio classification [6, 13] and speech processing [14, 20] tasks. Many 1D datasets can also have relationships spanning across long distances along the width. In such cases, CNNs need 1D convolution layers with a wide receptive field. 1D convolution layers with dilation [36] satisfy this need. Dilated convolution layers have been used in Google’s Wavenet [25, 26] architectures for text to audio generation. Recently, deep 1D CNNs have also been utilized to perform denoising [16, 28] and peak detection in Assay for Transposable-Accessible Chromatin sequence (ATAC-seq) data [2]. Rai et al. [28] used a U-Net [29] type CNN architecture with 1D convolutional layers to upscale ATAC-seq data. Lal et al. [16] used a 1D ResNet [8] CNN with dilated convolution layers for simultaneous denoising and peak calling from low-coverage or low-quality ATAC-seq data.

Researchers have made several efforts to optimize 2D convolution layer kernels. Such as convolution using the image-to-column transform [1, 33], the fast Fourier transform (FFT) [22, 32, 38] method and the Winograd [17] method. These implementations make assumptions such as a 2D tensor data input, short filter sizes, local connectivity, and narrow receptive fields. Specialized library implementations, such as oneDNN [24] and cuDNN [3] have efficient implementations for 2D convolution layer. These implementations perform well for 1D convolution layers with short input tensor widths and short filter widths (1 to 3). In such cases, 1D computation is analogous to a 2D computation with tensors of short height and long width. However, oneDNN based implementations quickly become inefficient when we increase the 1D tensor width or filter width. Thus, several applications that need a long receptive field (audio, genomics, speech) do not perform efficiently.

Our goal is to improve the computational efficiency of the 1D dilated convolution layer on CPUs. We want to develop computational kernels that are generic enough to achieve high efficiency across a wide range of parameters for 1D convolution layer. Recently, Georganas et al. [7] have shown that a single computational kernel of batch-reduce GEneral Matrix Multiply (BRGEMM) can implement many popular deep learning algorithms, including direct convolutions. Additionally, BRGEMM and small GEMMs based implementation can achieve high efficiency on CPUs. The LIBXSMM library [9] provides efficient implementation of BRGEMM and small GEMMs in C language and provides support for both FP32 and Bfloat16 precision levels. It generates optimal assembly code with AVX-512 and AVX-512 BFloat16 SIMD instructions where applicable using Just-in-time (JIT) code generation that provides more instruction reduction than manually written intrinsics based code.

In this work, we rewrite the algorithm for 1D convolution in terms of BRGEMM and small GEMM kernels. We use the LIBXSMM library and cache blocking to develop a highly efficient implementation and then integrate the C++ code into the PyTorch framework. We use the LIBXSMM library to implement the 1D dilated convolution layer in single-precision (FP32) and Bfloat16 precision. The combination of BRGEMM, small GEMMs, JIT-based code generation, and cache blocking along the tensor width dimension results in an implementation that performs well across a range of convolution layer parameters. To demonstrate this, we implement a one layer network for each precision type and perform experiments while varying parameters of filters, channels, input width, filter size, and dilation. In our experiments, the forward pass and the backward pass kernels display high efficiency across parameters. Specifically, our implementations achieve significant speedup over the oneDNN library for 1D tensors with long widths and filter sizes greater than or equal to 5.

We also demonstrate the effectiveness of the optimized 1D dilated convolution layer in end-to-end CNN training using real genomics (ATAC-seq) datasets. We integrate our 1D convolution layer in the training workflow presented in [16] for using CNN with dilated convolution layers for denoising and peak calling from low-coverage or low-quality 1D ATAC-seq data. Our experiments show up to 6.86x speedup over the oneDNN library for end-to-end training on Intel® Cascade Lake CPUs. We also scale the experiments to multiple sockets and longer chunks of 1D data. Our scaling experiments demonstrate close to linear speedup while scaling from 1 to 16 CPU sockets of Intel Cascade/Cooper Lake CPUs. We compare the performance of 16 CPU sockets with that reported in [16] for an Nvidia DGX-1 box (8 V100 GPUs with a host CPU) [4] since they are in the similar power envelop. In the end-to-end training with 16 CPU sockets, we get a speedup of 1.41x on Cascade Lake with FP32, 1.57x on Cooper Lake with FP32, and 2.27x on Cooper Lake with BFloat16 over the DGX-1 box using FP32.

The paper is organized as follows. In Section 2, we describe the 1D dilated convolution layer followed by our proposed approach for accelerating it including algorithms for forward and backward pass kernels in Section 3. In Section 4, we present the experiments on efficiency of the convolution layer, end-to-end CNN training, and scaling. In Section 5, we conclude the paper and mention ongoing work.

2 1D DILATED CONVOLUTION LAYER

One-dimensional (1D) convolution operation applies a 1D filter to a 1D input signal and produces a 1D output signal. However, in deep learning frameworks such as PyTorch and Tensorflow, a 1D convolution layer usually operates on a three-dimensional tensor input containing dimensions of batch size (N), input channels (C), and input width (W). Thus, input tensor (In) has a size of (N, C, W). Similarly, if the convolution layer has K number of filters, then the output tensor (Out) dimension becomes (N, K, Q) with output width as Q. We employ multithreading across the batch dimension (N) in the forward pass and the backward pass kernels. Thus, for further discussion, we will ignore the batch dimension and assume two-dimensional tensors for inputs and outputs. Hence, input tensor dimension changes to (C, W) and output tensor dimension changes to (K, Q). If the filter width is S than the weight tensor (Weight) has size as (K, C, S). We can represent the standard 1D convolution layer with parameters equation (1).

\[
Out(k, q) = \sum_c \sum_{w+q} ln(c, w) \ast Weight(k, c, s)
\]  

(1)

In the 1D dilated convolution layer with a dilation amount of d, the filter weights are multiplied with every dth element of the input tensor along the width dimension. We can represent the 1D dilated convolution layer by equation (2).

\[
Out(k, q) = \sum_c \sum_{w+d\times s+q} ln(c, w) \ast Weight(k, c, s)
\]  

(2)
Efficient and Generic 1D Dilated Convolution Layer for Deep Learning

We implement the forward pass and the backward data pass of 1D dilated convolution with input channels ($C$) without increasing its computational cost. We can also observe (Equation (3) shows the batch reduce GEMM operation.)

The blocks to be multiplied and to the output block $C$ of pointers for the sors. BRGEMM kernel needs the following arguments: ($\alpha$ can be taken from any position in the larger $A$ and $B$ input tensors. Results to a block $C$ from equations (1) and (2) that the standard 1D convolution can be thought of as 1D dilated convolution with dilation parameter ($K$) = 3.

Figure 1 illustrates an example of the 1D dilated convolution layer with parameters of dilation, input width, input channels, and the number of filters. We assume zero-padding at the tensor edges.

3 OUR EFFICIENT 1D DILATED CONVOLUTION LAYER

We implement the forward pass and the backward data pass of the 1D dilated convolution layer using BRGEMM kernel of the LIBXSMM library. The backward weight pass kernel is implemented using small GEMM kernels. We do not implement the bias calculation of the forward and the backward pass but instead use the framework’s implementation. BRGEMM kernel multiplies two matrix blocks $A_i \in \mathbb{R}^{m \times k}$ and $B_i \in \mathbb{R}^{k \times n}$ and reduces the partial results to a block $C_j \in \mathbb{R}^{m \times n}$ of a tensor $C$. The blocks $A_i$ and $B_i$ can be taken from any position in the larger $A$ and $B$ input tensors. BRGEMM kernel needs the following arguments: (i) Arrays of pointers for the $A_i$ and $B_i$ blocks to be multiplied, (ii) a pointer to the output block $C_j$, (iii) Size of blocks, (iv) the number ($l_{bp}$) of the blocks to be multiplied and ($\alpha$) the scaling parameters $\alpha$ and $\beta$.

Equation (3) shows the batch reduce GEMM operation.

$$C_j = \beta \star C_j + \alpha \sum_{i=0}^{l_{bp}-1} A_i \star B_i$$

3.1 Forward Pass

To implement the forward pass, we first make some changes in the weight tensor layout to convert the forward pass computation into a matrix multiplication. We change the layout of the weight tensor from ($K, C, S$) to ($S, K, C$). Consequently, the 1D dilated convolution can be described by a series of $S$ GEMM operations explained in algorithm 1.

Algorithm 1 Forward pass using GEMM operations

Inputs: $In \in \mathbb{R}^{C \times W}, Weight \in \mathbb{R}^{S \times K \times C}, d \in \mathbb{R}$

Output: $Out \in \mathbb{R}^{K \times Q}$

1. procedure FORWARD_PASS($Out, In, Weight, d$)
2. for $s = 0, 1, ..., S - 1$
3. $Out[:: :] = GEMM(Weight[::, :], In[::, (d * s) : (d * s + Q)])$
4. end for
5. return $Out$  

6. end procedure

Once we can express the algorithm in terms of GEMM operations, we can convert it into BRGEMM operations. We can replace the for loop of algorithm 1 into a BRGEMM computation. However, a matrix problem-size suitable for the LIBXSMM library with $m, n, k$ matrix dimensions is $(mnk)^{1/3} \ll 64$. The LIBXSMM library automatically employs an efficient utilization of the cache hierarchy when the $(mnk)^{1/3} \ll 64$ condition is satisfied. Thus, we employ blocking along the input width dimension and perform BRGEMM operation on the blocks. In all our kernels, we keep the block length equal to 64 elements along the width dimension. Block length of 64 ensures that one dimension of the GEMM problem size remains within the LIBXSMM library’s constraints. In our implementations, the other two dimensions are defined by the number of channels $C$.

Figure 2 illustrates batch-reduce GEMM operation with two-dimensional tensors. As shown in the figure, we can choose matrix blocks from any place in the tensor by specifying pointers and block sizes. It is also possible for the matrix blocks to overlap. In the following subsections, we present the forward pass, the backward data pass, and the backward weight pass algorithms with some figures for further explanation.
• For blocks in Q

![Diagram of Forward pass kernel using batch-reduce GEMM](image)

Figure 3: Forward pass kernel using batch-reduce GEMM. We multiply \( A_i \) blocks from the weight tensor and \( B_i \) blocks from the input tensor. The result is reduced into \( C_j \) block in the output tensor. Cache blocking occurs along the width dimension.

and the number of filters \( K \) parameters. Thus, we achieve highly efficient cache optimized implementation whenever \((C \times K)^{1/2} \ll 64\). Additionally, the LIBXSMM library’s GEMM kernels maintain good efficiency as long as the value of \((C \times K)^{1/2}\) doesn’t increase drastically. Algorithm 2 and figure 3 show the forward pass computation using BRGEMM kernel.

**Algorithm 2** Forward pass using BRGEMM operation

**Inputs:** \( \text{In} \in \mathbb{R}^{C \times W} \), \( \text{Weight} \in \mathbb{R}^{S \times K \times C} \), \( d \in \mathbb{R} \)

**Output:** \( \text{Out} \in \mathbb{R}^{K \times Q} \)

1. **procedure** FORWARD PASS(\( \text{Out, In, Weight, d} \))
2.  
3.     for pos = 0 to Q in steps of 64 do \hspace{1em} \( \triangleright \) Cache blocking
4.         for s = 0, 1, ..., S - 1 do \hspace{1em} \( \triangleright \) Generate pointers
5.             \( A_{ptrs}[s] = \text{Pointer to Weight}[s, 0, 0] \)
6.             \( B_{ptrs}[s] = \text{Pointer to In}[0, (pos + s + d)] \)
7.     end for
8.     BRGEMM(\( A_{ptrs}, B_{ptrs}, \text{Pointer to Out}[0, pos], S \))
9.     return \( \text{Out} \) \hspace{1em} \( \triangleright \) The output tensor
10. **end procedure**

**3.2 Backward Data Pass**

In the backward data pass implementation, we first change the weight tensor layout from \((K, C, S)\) to \((S, C, K)\). Similar to the forward pass, data gradient (\( \text{Grad}_d \in \mathbb{R}^{C \times W} \)) computation can be converted into a matrix multiplication of weights and output gradient (\( \text{Grad}_\text{out} \in \mathbb{R}^{K \times Q} \)). The backward data pass algorithm is very similar to the forward pass. We again employ the cache blocking along the width dimension with a block size of 64. We zero pad the gradient output (\( \text{Grad}_\text{out} \)) wherever needed. Algorithm 3 implements the backward data kernel using BRGEMM operation.

**Algorithm 3** Backward data pass using BRGEMM operation

**Inputs:** \( \text{Grad}_\text{out} \in \mathbb{R}^{K \times Q} \), \( \text{Weight} \in \mathbb{R}^{S \times K \times C} \), \( d \in \mathbb{R} \)

**Output:** \( \text{Grad}_d \in \mathbb{R}^{C \times W} \)

1. **procedure** BACKWARD DATA PASS(\( \text{Grad}_d, \text{Grad}_\text{out}, \text{Weight}, d \))
2.  
3.     for pos = 0 to W in steps of 64 do \hspace{1em} \( \triangleright \) Cache blocking
4.         for s = 0, 1, ..., S - 1 do \hspace{1em} \( \triangleright \) Generate pointers
5.             \( A_{ptrs}[s] = \text{Pointer to Weight}[s, 0, 0] \)
6.             \( B_{ptrs}[s] = \text{Pointer to Grad}_\text{out}[0, pos-(S-1-s)*d] \)
7.     end for
8.     BRGEMM(\( A_{ptrs}, B_{ptrs}, \text{Pointer to Grad}_d[0, pos], S \))
9.     return \( \text{Grad}_d \) \hspace{1em} \( \triangleright \) Data gradient
10. **end procedure**

**3.3 Backward Weight Pass**

We utilize small GEMM operations in the backward weight pass implementation. We again do cache blocking along the width dimension with a block size of 64. The backward weight pass kernel

**4 EXPERIMENTS AND RESULTS**

In this section, we present details of our experiments and results. We use Intel® Xeon® Cascade Lake and Cooper Lake CPUs for all
our experiments. Our first set of experiments focus on the efficiency and generality of the 1D convolution layer. We present the computational efficiency compared to peak machine performance of the forward pass and the backward pass implementations. We compare the efficiency of our single-precision and Bfloat16 precision implementations with the oneDNN library. In our second experiment set, we conduct end-to-end training of a 1D Resnet CNN with 1D ATAC-seq data. Finally, we scale our experiments by increasing the number of compute sockets, dataset size, and ATAC-seq signal track size. We show multinode scaling results and compare them with multi-GPU results published in [16].

4.2 Experimental Details
We use synthetic datasets for experiments to measure the efficiency of our optimized 1D convolution layer. For end-to-end training experiments, we train a 1D Resnet CNN named AtacWorks [16] and collect end-to-end training results with a genomics (ATAC-Seq) dataset. A trained AtacWorks neural network model takes noisy 1D ATAC-seq signal track segment as input and produces a corresponding 1D denoised signal track segment along with a 1D binary array of called peaks. Multiple loss functions are used to train the AtacWorks network. The loss function uses mean squared error (MSE) for the denoised signal and binary cross-entropy for the peak detection. The AtacWorks neural network architecture consists of multiple residual blocks, and each residual block contains 1D dilated convolution layers followed by a ReLU non-linearity. In total, AtacWorks utilizes 25 1D convolution layers for a wide range of parameters. We vary the output tensor width, number of channels, number of filters, filter widths, and the dilation parameter values. We choose output tensor width from the set \( \{1000, 2000, 5000, 10000, 20000, 60000\} \), number of channels from the set \( \{3, 4, 8, 10, 15, 16, 32, 64\} \), number of filters from the set \( \{1, 4, 8, 10, 15, 16, 32, 64\} \), filter size from the set \( \{1, 5, 9, 15, 21, 25, 31, 49, 51\} \) and the dilation parameter from the set \( \{1, 2, 4, 8, 16, 16\} \). We use the output tensor width instead of the input tensor width because it remains constant for different filter sizes and dilation parameter values.

Our experiments show that in most cases, optimized forward pass and backward pass computations achieve significantly higher efficiency compared to the oneDNN implementations. Specifically, our kernels are more efficient whenever the following condition is satisfied for the parameters of filter size (S), output tensor width (Q), number of channels (C), and number of filters (K).

\[
\text{Condition} \rightarrow (S \geq 5) \land (Q \geq 1000) \land (C > 1) \land (K > 1) \quad (4)
\]

The optimization condition in equation 4 covers a wide range of parameters, and it shows that the optimized convolution layer is generic. It also demonstrates the effectiveness of BRGEMM, JIT code generation, and cache blocking along the width dimension. For the sake of brevity, we present here a few results and plots. Figure 5 plots show computational efficiency of the 1D dilated convolution layer with respect to the output tensor width. Plots
Figure 4: Plots for 1D convolution layer using FP32 with input channels \((C) = 15\), number of filters \((K) = 15\), and dilation \((d) = 8\) on single socket Cascade Lake. The efficiency of the forward pass and the backward pass computation is plotted with respect to output tensor width.

in figure 4 are for the 1D dilated convolution layer with 15 input channels, 15 filters, and with the dilation parameter equal to 8. Each subplot in figure 4 corresponds to a different filter width. These results are obtained on a single-socket of Cascade Lake CPU for 20 iterations. Figure 5 contains the efficiency results for a standard 1D convolution \((dilation=1)\) with 64 channels and 64 filters. We observe that for larger filter widths, the forward pass and the backward pass can achieve up to 80% efficiency. The optimized layer has the highest efficiency with larger filter widths and output tensor widths. Contrarily, the oneDNN based layer has less computation efficiency in those cases.

We conduct similar experiments for the BFloat16 precision on a single-socket Cooper Lake machine. Figure 6 shows the plot of performance (FLOPS) with respect to output tensor width. In this experiment, convolution layers had 32 channels, 32 filters, and a dilation parameter of 4. In these plots, the oneDNN layer runs in single-precision, while our optimized convolution layer runs in BFloat16 precision. We can observe that BFloat16 implementation increases the performance in most cases. We get a 1.6x speedup compared to the FP32 code. We again see the maximum performance with long output tensor widths and filter sizes. Our current implementation of the convolution layer in BFloat16 precision requires the input tensor width, the number of channels, and the number of filters to be even numbers.
Efficient and Generic 1D Dilated Convolution Layer for Deep Learning

Figure 5: Plots for 1D convolution layer using FP32 with input channels (C) = 64, number of filters (K) = 64, and dilation (d) of 1 on single socket Cascade Lake. The efficiency of the forward pass and the backward pass computation is plotted with respect to output tensor width.

4.4 End-to-End Training Experiment on a Single Socket CPU

In this experiment, we use the setup described in Section 4.2 and train the AtacWorks neural network on a single socket of Cascade Lake or Cooper Lake CPUs. We reserve one CPU core on each socket for the PyTorch DataLoader() worker and the remaining 27 CPU cores for computation. An attempt to utilize all 28 CPU cores on a socket for computation decreases efficiency. In such a case, the thread of DataLoader() worker can slow down compute CPU cores by idling them. We use a batch size of 54 for the backend consisting of optimized code and a batch size of 64 with the oneDNN based backend. We use these batch sizes to obtain maximum training efficiency for each code.

Table 1 and figure 7 show the end-to-end training time per epoch results on single-socket Cascade Lake (CLX) and Cooper Lake (CPX). To verify accuracy, we also train the network using original AtacWorks running on a V100 GPU with a batch size of 64. We can observe that the implementation based on our optimized layer on a single-socket Cascade Lake achieves up to $6.86 \times$ speedup over the oneDNN. Cooper Lake CPUs are slightly faster than Cascade Lake CPUs due to higher frequency and memory bandwidth. Additionally, we can observe from Table 1 that the training in BFloat16 precision can provide significant speedup without compromising the accuracy. In BFloat16 training experiments, most convolution layers of AtacWorks had 16 channels, 16 filters, a filter size of 51,
and a dilation of 8. We also implemented a BFloat16 precision rectified linear unit (ReLU) layer using the LIBXSMM library to reduce time-consuming data conversion operations.

4.5 Scaling Experiments for End-to-End Training

In this set of experiments, we scale the ATAC-seq training experiments to multiple sockets, longer signal track segment sizes, and larger dataset size.

4.5.1 Multisocket Scaling Experiment. In this experiment, we train the AtacWorks network with the setup described in Section 4.2 on multiple sockets, ranging from one to sixteen sockets. We train the network on {1,2,4,8,16} sockets of Cooper Lake CPUs in single-precision and BFloat16 precision. In each run, we train for 25 epochs and collect the training time. In multi-socket experiments, we reserve one CPU core on each socket for the PyTorch DataLoader() worker and one more CPU core on each socket for the message passing interface (MPI) communication, and the other 26 CPU cores for computation. Additionally, we increase the batch size in accordance with the increase in the number of sockets. We keep the batch size as {54, 52, 104, 208, 416} for {1, 2, 4, 8, 16} socket experiments respectively. Figure 8 shows the speedup for FP32 precision over single-socket training time as we increase the number of sockets. As earlier, in the FP32 experiment, most convolution layers have 15 channels, 15 filters, a filter size of 51, and a dilation of 8. Figure 9 shows the results of the same experiment in BFloat16 precision.
Efficient and Generic 1D Dilated Convolution Layer for Deep Learning

Figure 7: ATAC-seq training experiment results. Training time per epoch is an average of 25 epoch values during training. Speedup is over the baseline of oneDNN run on a single-socket Cascade Lake (CLX). Timing and speedup results are on a single-socket (28 cores) of Cascade Lake (CLX) and Cooper Lake (CPX).

In BFloat16 precision, most convolution layers have 16 channels, 16 filters, a filter size of 51, and a dilation of 8. In both figures, we observe that training time scales nearly linearly with an increase in the number of sockets. These scaling results demonstrate that our convolution layer kernels are scalable to multiple sockets.

4.5.2 Comparison with original AtacWorks running on Nvidia DGX-1 box. The AtacWorks paper [16] reports that training the AtacWorks network using the same setup as defined in Section 4.2 for 25 epochs on a DGX-1 box [4] consisting of 8 Nvidia V100 GPUs and a dual socket host CPU takes 2.7 minutes (162 seconds) per epoch. In order to compare with it, we train the AtacWorks network for 25 epochs on 16 sockets of Cascade Lake and Cooper Lake CPUs so as to use nearly the same power envelop. Since it is not clear whether the time reported in [16] includes evaluation time or not, we include the evaluation time for the CPU experiments for comparison. In our training process, we again reserve one CPU core on each socket for the PyTorch DataLoader() worker, one more CPU core on each socket for MPI communication, and the other 26 CPU cores on each socket for computation. We use a batch size of 416 to take advantage of 16 CPU sockets. Table 2 and Figure 10 show training accuracy and time per epoch. Note that our training accuracy for the multi socket runs is nearly the same as that of a single socket run. We can observe that our LIBXSMM library based implementation on sixteen sockets of Cascade Lake achieves up to 1.41x speedup over eight Nvidia V100 GPUs. Sixteen sockets of Cooper Lake (CPX) are 1.57x faster than eight V100 GPUs in training with single-precision (FP32) layers, and they are 2.27x faster with BFloat16 (BF16) layers. Eight sockets of Cooper Lake are also 1.32x faster than eight V100 GPUs with BFloat16 layers. The evaluation is single threaded and doesn’t scale, so Figure 10 shows

Table 1: ATAC-seq training experiment results for 25 epochs. Training time per epoch is an average of 25 epoch values during training. Timing and accuracy results are on a single-socket (28 cores) of Cascade Lake (CLX) and Cooper Lake (CPX). Accuracy of original AtacWorks running on a single Nvidia V100 GPU is reported for comparison.

| Device | Code (Precision) | Training time (sec.) | Accuracy (AUROC) |
|--------|------------------|----------------------|------------------|
| 1 V100 | CUDA (FP32)      | –                    | 0.9386           |
| 1s CLX | oneDNN (FP32)    | 9690.4               | 0.9388           |
| 1s CLX | LIBXSMM (FP32)   | 1411.9               | 0.9388           |
| 1s CPX | LIBXSMM (FP32)   | 1254.8               | 0.9387           |
| 1s CPX | LIBXSMM (BF16)   | 769.6                | 0.9378           |
We finished the training without incurring any out-of-memory issue with our optimized implementation. We were not able to run this experiment on V100 due to GPU’s memory constraints.

The training and evaluation time separately. Evaluation time is a significant portion of the total time. Therefore, if the time reported for DGX-1 box does not include the evaluation time, our speedups are significantly higher.

Table 2: ATAC-seq multi socket training time per epoch (in seconds) on CPUs in comparison with Nvidia V100. Training time includes the evaluation time. The time for 8 V100 GPUs is from [16]. The paper did not report accuracy.

| Device | Precision | Time per epoch (sec.) | Accuracy (AUROC) | Speedup |
|--------|-----------|-----------------------|------------------|---------|
| 8 V100 | FP32      | 162.0                 | -                | 1.00x   |
| 16s CLX | FP32      | 115.0                 | 0.9345           | 1.41x   |
| 16s CPX | FP32      | 103.1                 | 0.9341           | 1.57x   |
| 8s CPX  | BF16      | 122.8                 | 0.9346           | 1.32x   |
| 16s CPX | BF16      | 71.3                  | 0.9323           | 2.27x   |

4.5.4 Large Dataset Experiment. In this experiment, we increase the number of signal track segments to 293242 in the training set and 2520 in the validation set while keeping the signal track segment width as 60000. Thus, the training set in this experiment is approximately 9.16× larger than the one used in previous experiments. We train the AtacWorks neural network for 25 epochs on 16 sockets of Cascade Lake CPUs using our optimized implementation. Our training time per epoch excluding the evaluation time was 872.1 seconds. It is approximately 9.16× larger than the training time per epoch with the previous training sets. We were also able to achieve the training accuracy of 0.9390 in terms of the AUROC metric. This demonstrates that our performance scales linearly with the increase in dataset size.

5 CONCLUSION

Researchers have used 1D convolution layers in multiple fields like audio processing, speech recognition, and genomics. Efficient and generic implementations of the 1D convolution kernels are needed to save time and cost. We believe that future progress in applications like genomics will depend on computing costs. We have shown that code optimizations using the LIBXSMM library’s BRGEMM kernel with JIT code generation and cache blocking can increase the efficiency for 1D dilated convolution layers. This approach also helps us generalize the implementations to a wide range of use-cases. Additionally, proper use of Intel® AVX-512 and AVX-512 BFloat16 instructions can unlock substantial speedups over previous implementations.

REFERENCES

[1] Andrew Anderson, Aravind Vasudevan, Cormac Keane, and David Gregg. 2017. Low-memory gemm-based convolution algorithms for deep neural networks. arXiv preprint arXiv:1709.03395 (2017).

[2] Jason D Buenrostro, Beijing Wu, Howard Y Chang, and William J Greenleaf. 2015. ATAC-seq: a method for assessing chromatin accessibility genome-wide. Current protocols in molecular biology 109, 1 (2015), 21–29.

[3] Sharan Chetlur, Cliff Woolley, Philippe Vandermersch, Jonathan Cohen, John Tran, Bryan Catanzaro, and Evan Shelhamer. 2014. cudnn: Efficient primitives for deep learning. arXiv preprint arXiv:1410.0759 (2014).

[4] Nvidia Corporation. (n.d.). NVIDIA DGX-1 User Guide. https://images.nvidia.com/content/technologies/deep-learning/pdf/DGX-1-UserGuide.pdf. Accessed: April 2021.

[5] Chao Dong, Chen Change Loy, Kaiming He, and Xiaou Tang. 2015. Image super-resolution using deep convolutional networks. IEEE transactions on pattern analysis and machine intelligence 38, 2 (2015), 295–307.

[6] Jort F Gemmeke, Daniel PW Ellis, Dylan Freedman, Aron Jansen, Wade Lawrence, R Channing Moore, Manoj Plakal, and Marvin Ritter. 2017. Audio set: An ontology and huma-labeled dataset for audio events. In 2017 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP). IEEE, 776–780.

[7] Evangelos Georganas, Kunal Banerjee, Dhiraj Kalamkar, Sashank Avancha, Anand Venkat, Michael Anderson, Greg Henry, Hans Pabst, and Alexander Heinecke. 2019. High-Performance Deep Learning via a Single Building Block. arXiv preprint arXiv:1906.06440 (2019).

[8] Kaiming He, Xiangyu Zhang, Shaoqing Ren, and Jian Sun. 2016. Deep residual learning for image recognition. In Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition. 770–778.

[9] Alexander Heinecke, Greg Henry, Maxwell Hutchinson, and Hans Pabst. 2016. LIBXSMM: accelerating small matrix multiplications by runtime code generation. In SC’16: Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis. IEEE, 981–991.

[10] Danny Hernandez and Tom B Brown. 2020. Measuring the algorithmic efficiency of neural networks. arXiv preprint arXiv:2005.04305 (2020).

[11] Kyong Hwan Jin, Michael T McCann, Emmanuel Froustey, and Michael Unser. 2017. Deep convolutional neural network for inverse problems in imaging. IEEE Transactions on Image Processing 26, 9 (2017), 4509–4522.

[12] Serkan Kiranyaz, Onur Avci, Osama Abdeljaber, Turker Ince, Moncef Gabbouj, and Daniel J Inman. 2021. 1D convolutional neural networks and applications: A survey. Mechanical Systems and Signal Processing 151 (2021), 107038.
Qiuqiang Kong, Yin Cao, Turah Iqbal, Yuxuan Wang, Wenwu Wang, and Mark D Plumbley. 2020. Panns: Large-scale pretrained audio neural networks for audio pattern recognition. IEEE/ACM Transactions on Audio, Speech, and Language Processing 28 (2020), 2889–2894.

Samuel Krizman, Stanislav Blaeva, Boris Ginsburg, Jocelyn Huang, Oleksii Kuchaiev, Vitaly Lavrukhin, Ryan Leary, Jason Li, and Yang Zhang. 2020. Quartznet: Deep automatic speech recognition with 1d time-channel separable convolutions. In ICASSP 2020-2020 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP). IEEE, 6124–6128.

Alex Krizhevsky, Ilya Sutskever, and Geoffrey E Hinton. 2012. ImageNet classification with deep convolutional neural networks. In Advances in Neural Information Processing Systems 25. F. Pereira, C. J. C. Burges, L. Bottou, and K. Q. Weinberger (Eds.). Curran Associates, Inc., New York, USA, 1097–1105.

Avantika Lal, Zachary D. Chiang, Nikolai Yakovenko, Fabiana M. Duarte, Johnny Israel, and Jason D. Buenrostro. 2019. AtacWorks: A deep convolutional neural network toolkit for epigenomics. bioRxiv (2019). https://doi.org/10.1101/829481 arXiv:https://www.biorxiv.org/content/early/2019/11/04/829481.full.pdf

Andrew Lavin and Scott Gray. 2016. Fast algorithms for convolutional neural networks. In Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition. 4013–4021.

Yann LeCun, Yoshua Bengio, and Geoffrey Hinton. 2015. Deep learning. Nature 521, 7553 (2015), 436.

Charles E. Leiserson, Neil C. Thompson, Joel S. Emer, Bradley C. Kuszmaul, Butler W. Lampson, Daniel Sanchez, and Tao B. Schardl. 2020. There’s plenty of room at the Top: What will drive computer performance after Moore’s law? Science 368, 6495 (2020). https://doi.org/10.1126/science.aam9744 arXiv:https://science.sciencemag.org/content/368/6495/aam9744.full.pdf

Jason Li, Vitaly Lavrukhin, Boris Ginsburg, Ryan Leary, Oleksii Kuchaiev, Jonathan M Cohen, Huyen Nguyen, and Ravi Teja Gadde. 2019. Jasper: An end-to-end convolutional neural acoustic model. arXiv preprint arXiv:1904.03288 (2019).

Chris A Mack. 2011. Fifty years of Moore’s law. IEEE Transactions on semiconductor manufacturing 24, 2 (2011), 202–207.

Michael Mathieu, Mikael Henaff, and Yann LeCun. 2013. Fast training of convolutional networks through fbits. arXiv preprint arXiv:1312.5551 (2013).

Shervin Minaee, Yuri Y Boykov, Fatih Porikli, Antonino J Plaza, Nasser Kehtarnavaz, and Demetri Terzopoulos. 2021. Image segmentation using deep learning: A survey. IEEE Transactions on Pattern Analysis and Machine Intelligence (2021).

Intel onedNN. 2021. https://github.com/onera-ai/onedNN https://github.com/onedapi-ai/onedNN

Aaron Oord, Yazhe Li, Igor Babuschkin, Karen Simonyan, Oriol Vinyals, Koray Kavukcuoglu, George Dieleman, Edward Lockhart, Luis Cubo, Florian Stimberg, and Demetri Terzopoulos. 2021. Image segmentation using deep learning: A survey. IEEE Transactions on Pattern Analysis and Machine Intelligence (2021).

Intel onedNN. 2021. https://github.com/onedapi-ai/onedNN

Aaron van den Oord, Sander Dieleman, Heiga Zen, Karen Simonyan, Oriol Vinyals, Alex Graves, Nal Kalchbrenner, Andrew Senior, and Koray Kavukcuoglu. 2016. Wavenet: A generative model for raw audio. arXiv preprint arXiv:1609.03499 (2016).

Ryan Poplin, Pi-Chuan Chang, David Alexander, Scott Schwartz, Thomas Colthurst, Alexander Ku, Dan Newburger, Jojo Dijamco, Nam Nguyen, Pehagh T Afhar, et al. 2018. A universal SNP and small-indel variant caller using deep neural networks. Nature biotechnology 36, 10 (2018), 983–987.

Vivek Rai, Daniel X Quang, Michael R Erdos, Darren A Cusanovich, Riza M Daza, Naxton Narisu, Lili S Zou, John F Didion, Yuanfang Guan, Jay Shendure, et al. 2020. Single-cell ATAC-Seq in human pancreatic islets and deep learning upscaling of rare cells reveals cell-specific type 2 diabetes regulatory signatures. Molecular metabolism 32 (2020), 109–121.

Olaf Ronneberger, Philipp Fischer, and Thomas Brox. 2015. U-Net: Convolutional networks for biomedical image segmentation. In Proceedings of International Conference on Medical Image Computing and Computer-Assisted Intervention. Springer, 234–241.

Karen Simonyan and Andrew Zisserman. 2014. Very deep convolutional networks for large-scale image recognition. arXiv preprint arXiv:1409.1556 (2014).

Neil C Thompson, Kristjan Greenewald, Kreehon Lee, and Gabriel F Manso. 2020. The computational limits of deep learning. arXiv preprint arXiv:2007.05358 (2020).

Nicolas Vasilache, Jeff Johnson, Michael Mathieu, Soumik Chuntala, Serkan Piantino, and Yann LeCun. 2014. Fast convolutional nets with fbfft: A GPU performance evaluation. arXiv preprint arXiv:1412.7580 (2014).

Aravind Vasudevan, Andrew Anderson, and David Gregg. 2017. Parallel multi channel convolution using general matrix multiplication. In 2017 IEEE 28th international conference on application-specific systems, architectures and processors (ASAP). IEEE, 19–24.

Zhizhou Wu, Mike Schuster, Ziheng Chen, Quoc V Le, Mohammad Norouzi, Wolfgang Macherey, Maxim Krikun, Yuan Cao, Qun Gao, Klaus Macherey, et al. 2016. Google’s neural machine translation system: Bridging the gap between human and machine translation. arXiv preprint arXiv:1609.08144 (2016).

Fisher Yu and Vladlen Koltun. 2015. Multi-scale context aggregation by dilated convolutions. arXiv preprint arXiv:1511.07122 (2015).

Kai Zhang, Wangmeng Zuo, Yunjin Chen, Deyu Meng, and Lei Zhang. 2017. Beyond a Gaussian denoiser: Residual learning of deep CNN for image denoising. IEEE Transactions on Image Processing 26, 7 (2017), 3142–3155.

Aleksar Zlatoski, Zhen Jia, Kai Li, and Fred Durand. 2018. Fh convolutions are faster than winograd on modern cus, here is why. arXiv preprint arXiv:1809.07851 (2018).

Optimization Notice: Software and workloads used in performance tests may have been optimized for performance only on Intel® microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to http://www.intel.com/performance. Intel®, Xeon®, and Intel® Xeon Phi are trademarks of Intel Corporation in the U.S. and/or other countries.