Efficient FPGA-based ECDSA Verification Engine for Permissioned Blockchains

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ABSTRACT
As enterprises embrace blockchain technology, many real-world applications have been developed and deployed using permissioned blockchain platforms (access to network is controlled by allowing only nodes with known identities). Such blockchain platforms heavily depend on cryptography to provide a layer of trust within the network, thus verification of cryptographic signatures often becomes the bottleneck. The Elliptic Curve Digital Signature Algorithm (ECDSA) is the most commonly used cryptographic scheme in permissioned blockchains. In this paper, we propose an efficient implementation of ECDSA signature verification on an FPGA, in order to improve the performance of permissioned blockchains that aim to use FPGA-based hardware accelerators.

In particular, we propose several optimizations for modular arithmetic (e.g., custom multipliers and fast modular reduction) and point arithmetic (e.g., significantly reduced number of point double and addition operations, and optimal width NAF representation). Based on these optimized modular and point arithmetic modules, we propose an ECDSA verification engine that can be used by any application for fast verification of ECDSA signatures. We further optimize our ECDSA verification engine for Hyperledger Fabric (one of the most widely used permissioned blockchain platforms) by moving carefully selected operations to a precomputation block, thus simplifying the critical path of ECDSA signature verification. From our implementation on Xilinx Alveo U250 accelerator board with target frequency of 250MHz, our ECDSA verification engine can perform a single verification in 760μs resulting in a throughput of 1,315 verifications per second, which is ~2.5x faster than state-of-the-art FPGA-based implementations [8, 18]. Our Hyperledger Fabric-specific ECDSA engine can perform a single verification in 368μs with a throughput of 2,717 verifications per second.

KEYWORDS
ECDSA signature verification, FPGA, Hyperledger Fabric

1 INTRODUCTION
Beyond the hype, blockchain technology is emerging as one of the most disruptive technologies, with real-world use cases in many domains from digital identity management to financial services, supply chains, and product provenance. The blockchain technology essentially provides a mechanism to execute and record transactions (representative of business logic) in an immutable ledger, by grouping transactions into blocks and creating a hash-linked chain of those blocks. The nodes in a blockchain network agree upon a total order of the blocks and transactions in each block (consensus), and each node maintains its own copy of the ledger, resulting in a distributed ledger. The beauty of blockchain technology is that it seamlessly combines consensus mechanisms with cryptography to provide a layer of trust for executing and recording transactions within a network of mutually untrusting nodes.

Blockchains are generally categorized into two types. In public blockchains, such as Bitcoin and Ethereum, any node can participate in the network without a specific identity and proof-of-work based consensus is used. Proof-of-work consensus is computationally very intensive because of the massive amounts of hashes that need to be computed, and thus becomes the bottleneck. Consequently, public blockchains use hardware acceleration for hashing. For example, Bitcoin network is dominated by ASIC based nodes while GPU based nodes dominate the Ethereum network [29]. In permissioned blockchains, on the other hand, only nodes with known identities are part of and allowed to interact with the network, while the consensus is delegated to only a few nodes (based on BFT or CFP protocols [1]). Consequently, nodes are authenticated and transactions are validated cryptographically, thus cryptographic operations become the bottleneck rather than the consensus mechanism [35]. Typically, permissioned blockchains are deployed on multi-core servers to benefit from some parallelism available across processing of multiple transactions.

Since permissioned blockchains provide trust through cryptographic authentication, and data integrity and replication through distributed ledger, they are becoming increasingly popular for implementation of enterprise applications. Many permissioned blockchain platforms such as Hyperledger Fabric [13], Quorum [5] and Corda [27] are now available. Fabric is an open-source and enterprise-grade implementation of a permissioned blockchain, and is one of the most widely used platforms with many real-world applications already developed and deployed from finance and supply chain domains [6, 7].

In a Hyperledger (HL) Fabric network, one of the nodes is a validator peer, which is responsible for validating a block and all of its transactions, before committing that block to the ledger. Many recent works [3, 9, 15, 35] have shown that validator peer is the major bottleneck and critically affects the peak throughput. Some of these works [3, 15, 36] further demonstrated that verification of cryptographic signatures is the major bottleneck inside a validator peer. By default, Fabric uses 256-bit ECDSA scheme for signature generation and verification. Validation of a block involves verification of its creator’s ECDSA signature, and validation of each transaction in a block involves verification of multiple ECDSA signatures (from creator and different peers in the network). Similar validation nodes exist in other permissioned blockchains such as Quorum [5] and Hyperledger Besu [14] (permissioned variants of Ethereum).

∗Work done during internship at Xilinx.
Hardware acceleration was recently proposed for validation of blocks in permissioned blockchains, specifically HL Fabric. The work in [16] proposed a CPU-FPGA based system where a multicore server with a network-attached FPGA card (connected to the CPU via PCIe) is used to accelerate validator peer of a Fabric network. All the compute-intensive operations of validation were offloaded to the FPGA accelerator, including verification of ECDSA signatures. Although the work in [16] demonstrated an order of magnitude speedup in block validation compared to CPU-only implementation, interestingly enough, the ECDSA signature verification still turned out to be the critical path in the FPGA accelerator. Therefore, in this paper, we focus on an efficient FPGA-based implementation of ECDSA signature verification, in order to improve performance of permissioned blockchains that aim to use FPGA-based accelerators.

More specifically, we focus on accelerating ECDSA signature verification over NIST P-256 elliptic curve. Working with NIST P-256 curve requires performing 256-bit modular and point arithmetic operations. This is challenging to implement on FPGAs because 256-bit wide multipliers, adders/subtractors, and dividers are not readily available. Therefore, a naive implementation will lead to a resource intensive design, leaving less resources for other operations of an accelerator. This, in turn, makes it challenging to fit the entire accelerator on an FPGA and meet the required timing constraints. In particular, we make the following contributions:

- **FPGA-specific optimizations for modular arithmetic:** We present algorithmic optimizations for modular arithmetic modules to enable optimized FPGA-based implementations. We specifically propose a custom 256-bit multiplier for integer multiplication (used in modular multiplication) and a 258-bit multiplier for Barrett reduction module. These multipliers efficiently leverage internal multipliers and registers of the DSP blocks in FPGA for better performance. We also propose an efficient algorithm to perform fast modular reduction over P-256 without using expensive 256-bit comparators.

- **Algorithmic optimizations for point arithmetic:** We present optimizations for simultaneous-point and fixed-point multiplication algorithms (used in ECDSA verification) by reducing the overall number of point double and addition operations respectively. We use projective Chudnovsky coordinate system along with optimal width for non-adjacent form (NAF) representation to further reduce the total number of point arithmetic operations.

- **HL Fabric-specific ECDSA verification:** We present a fast ECDSA signature verification engine by leveraging the fact that the generator point $G$ is fixed and the public key $K$ can be extracted in advance. This allows us to move a major chunk of point arithmetic from ECDSA verification to a precompute block. Consequently, the point arithmetic during actual ECDSA computation reduces to just point addition operations, resulting in a much faster signature verification.

We implemented our optimized ECDSA verification engines on Xilinx Alveo U250 board [40] with a target frequency of 250MHz. For modular arithmetic modules, we observe on average 1.5× speedup compared to [10], while for point arithmetic modules, we observe on average 3.2× speedup compared to the state-of-the-art implementations [10, 19, 21, 22, 31, 37]. Our ECDSA verification engine, using these modules, performs a signature verification in 760μs resulting in a throughput of 1, 315 verifications per second, which is ~2.5× faster than the existing FPGA-based implementations [8, 18]. With HL Fabric-specific optimizations, our ECDSA verification engine can perform a signature verification in 368μs resulting in a throughput of 2, 717 verifications per second.

## 2 BACKGROUND AND PRELIMINARIES

### 2.1 Blockchain Machine

Figure 1(a) depicts a simplified overview of hardware accelerator for HL Fabric that was proposed in [16]. The blocks are received in the FPGA accelerator card through the integrated network interface. The first module, ProtocolProcessor, processes the incoming packets and extracts relevant data, such as block id, number of transactions in the block, ECDSA signatures, public keys from identity certificates, etc. The second module, BlockProcessor, uses this data to validate the block and its transactions, before committing the transactions. Once a block is validated, the Fabric software running on CPU accesses validation results from hardware and continues on with committing the block to the ledger.

Internally, the BlockProcessor uses a configurable number of ECDSA verification engines distributed across multiple stages to process the ECDSA verifications as fast as possible. Each ECDSA engine accepts a verification request in the form of [signature, key, Generator point on the curve, $G = (x_G, y_G)$]

$$x_G = 6b171d1f2e202e04247 f88ce6e563a440f2$$

$$y_G = 77037d812deb33a0 f4a13945d898c296$$

$$p = 2^{256} - 2^{224} + 2^{192} + 2^96 - 1$$

$$a = -3$$

Order of the curve, $n$

$$n = fffffffd0000000 0000000000000000$$

$$b = 2326c92c0fe32551$$

Figure 1: Blockchain Machine: (a) FPGA-based hardware accelerator, (b) Domain parameters for Hyperledger Fabric.
which corresponds to the affine point where each point \( P \in \mathbb{A} \) on the elliptic curve, \( \mathcal{E} \). Table 1: Point addition and double equations in projective Chudnovsky coordinates [4] and are shown in Figure 2, it is evident that we need to implement modular inverse computations [18]. In this work, we focus on performing point addition and point double operations in projective Chudnovsky coordinates [4], which corresponds to the affine point \( (x = X/Z^2, y = Y/Z^3) \). These coordinates give a speed benefit over affine coordinates when the cost for modulo inversion is significantly higher than the modular multiplication. Therefore, we use projective Chudnovsky coordinates because FPGAs have DSP blocks with multipliers that can perform fast multiplications. The point addition and double equations in projective Chudnovsky coordinates are given in Table 1. For NIST Prime curves, which include P-256 that is used in HLS Fabric, domain parameters are given in FIPS 186-4 [23] and are listed along with Figure 1(b) for reference.

Table 1: Point addition and double equations in projective Chudnovsky coordinates.

| Point Addition | Point Double |
|---------------|--------------|
| \((X_1, Y_1, Z_1, Z_2, Z_3, X_2, Y_2, Z_2, Z_3)\) | \((X, Y, Z, Z_1^2, Z_2^2)\) |
| \(U_1 = X_1 * Z_2^2, U_2 = X_2 * Z_1^2\) | \(S = 4 * X * Y^2\) |
| \(S_1 = Y_1 * Z_2^2, S_2 = Y_2 * Z_1^2\) | \(M = 3 * X^2 + a * (Z^2)^2\) |
| \(H = U_2 - U_1, R = S_2 - S_1\) | \(X_1 = M^2 - 2 * S\) |
| \(X_3 = R^2 - H^2 - 2 * U_1 * U_2\) | \(Y_1 = M * (S - X_1) - 8 * Y^4\) |
| \(Y_3 = R * (U_1 * H^2 - X_3) - S_1 * H^3\) | \(Z_1 = 2 * Y + Z\) |
| \(Z_2 = H * Z_1 + Z_2\) | \(Z_1^2 = Z_1^2 + Z_1\) |
| \(Z_3^2 = Z_2^2, Z_4^2 = Z_2^2 * Z_3\) | \(Z_3^2 = Z_1^2 * Z_4\) |
| Return\((X_3, Y_3, Z_3, Z_1^2, Z_2^2)\) | Return\((X, Y, Z, Z_1^2, Z_2^2)\) |

3 RELATED WORK

In this section, we discuss the most relevant existing works in the literature. There are many publications focusing on acceleration of modular multiplication, point arithmetic for ECC, or ECDSA signature verification in hardware. Overall, these hardware accelerators can be broadly classified into three categories based on their implementation platforms. First category includes reconfigurable architectures that are FPGA-based [8, 10, 19, 30, 32, 34, 37], the second category includes 8-bit AVR-based implementations [11, 20, 25] for embedded devices that are resource constrained, and the third category includes ASIC-based hardwired architectures [17, 18, 41] to achieve high-performance for a specific elliptic curve. Some of the works [30, 41] focus on elliptic curves over binary fields \( GF(2^m) \) only. This is because the hardware implementation of binary field operations results in a carry-free logic, and thus these fields are the most optimal for use in hardware in terms of both speed and area. Other works focus on elliptic curves over prime fields \( GF(p) \), but perform hardware acceleration for a different field size like 163-bits [32], 192-bits [20], or 224-bits [11], which is not of interest to blockchain platforms that typically use 256-bits prime field. There is also a wide range of work [10, 19, 25, 37] that focuses on accelerating only point arithmetic for ECC over NIST P-256 elliptic curve, and do not implement the entire ECDSA verification.

Tachibana et al. [34] accelerate ECDSA verification algorithm over Secp256k1 elliptic curve for Bitcoin on an Intel Cyclone IV FPGA. Their single ECDSA verification takes about 145.52 ms. Glas et al. [8] present an FPGA-based ECDSA core for 256-bits field using Xilinx Virtex 5 FPGA board. The authors integrate their hardware core in a vehicle-to-vehicle communication system and compare the performance against microcontroller-based implementation. Ji et al. [17] and Knežević et al. [18] implement the ECDSA verification algorithm over NIST P-256 elliptic curve as ASICs. However, Ji et al. [17] did not report any latency numbers. We will present the results from both [8] and [18] for comparison in Section 7.

In this work, we optimize modular arithmetic operations (specifically multiplications) to utilize DSP blocks on FPGA and accelerate point arithmetic operations over NIST P-256 elliptic curve, and then combine these modules to implement an efficient ECDSA verification engine (both generic and HLS Fabric-specific). To the best of our knowledge, our proposed architecture performs the fastest ECDSA verification over NIST P-256 prime field on an FPGA (see Section 7).
Algorithm 1: ECDSA Verification

Input: Message digest z, the signature (r, s), and the public key \( \mathcal{K} = (xG, yG) \)

Output: Valid or invalid
1: if \((r, s)\) not in range \([1, n − 1]\) then
2: Return(Invalid)
3: end if
4: Compute \(w = s^{-1} \mod n\)
5: Compute \(k_1 = z \ast w \mod n\)
6: Compute \(k_2 = r \ast w \mod n\)
7: Compute \((x_2, y_2) = k_1G + k_2K\)
8: if \(r == x_2 \mod n\) then
9: Return(Valid)
10: else
11: Return(Invalid)
12: end if

arithmetic operations such as modulo inverse, multiplication and reduction followed by various point arithmetic operations such as point addition, double and scalar-point multiplication.

5 FPGA-BASED ECDSA VERIFICATION ENGINE

In this section, we present the architecture of our efficient ECDSA verification engine. We would like to highlight here that the ECDSA signature verification algorithm deals with the information that is publicly known, therefore there is no secret information to leak through side-channels while performing a signature verification. This widens our choice of algorithms for implementing various modules within the ECDSA verification engine. Therefore, in our hardware implementation, we select algorithms that utilize minimal hardware resources while resulting in low latency.

5.1 Modular Arithmetic

To efficiently implement 256-bit wide modular arithmetic on an FPGA, we implement all modular arithmetic modules using multi-word integer arithmetic [12]. In multi-word arithmetic, a 256-bit field element \(a\) can be represented as

\[
a = 2^{(t−1)W}A[t−1] + \cdots + 2^WA[2] + 2^WA[1] + A[0] \tag{2}
\]

where, \(W\) and \(t = 256/W\) define the word length and the number of words to operate on respectively. We set the value of \(W\) diligently for every operation to efficiently utilize the underlying resources of an FPGA. For example, on Xilinx Alveo U250 FPGA board, the multipliers are 16-bit wide and hence, \(W\) can be set as 16. The advantages of using multi-word integer approach and setting the value of \(W\) carefully are two-fold. First, it helps in performing the modular operations using hardwired DSP blocks on the FPGA. Second, it helps in achieving a higher maximum operating frequency for the entire design.

Modular Subtraction: Subtraction in \(\mathbb{F}_p\) can be performed using Algorithm 2 [12] with multi-word integer approach. The adder/subtractor in DSP blocks have 48-bit wide inputs. However, for multi-word integer approach, the maximum bit width we can use is 32 bits (32 being the largest integer dividing 256 symmetrically). Therefore, to use DSP for subtraction, we set the parameter \(W\) as 32 and thus, we have \(t = 8\) words to operate on. Along with each subtraction operation, we subtract the previous carry bit and store the next carry bit (line 3). As we operate on a single word at a time, we utilize only one DSP block to implement the modular subtraction operation. We want to highlight here that point arithmetic (including point double and add) in projective Chudnovsky coordinates requires only one modular addition operation (see Table 1). Therefore, we decided to perform the modular addition using our modular subtraction module with 2’s complement input for the second operand. Implementing a separate adder leads to inefficient resource utilization as the adder will remain idle for most of the time.

Algorithm 2: Subtraction in \(\mathbb{F}_p\)

Input: Modulus \(p\), integers \(a, b \in [0, p − 1]\), \(t = 8\)

Output: \(c = (a − b) \mod p\)
1: Set \((A[t−1], . . . , A[0])\) ← \(a\), \((B[t−1], . . . , B[0])\) ← \(b\)
2: \((carry, C[0])\) ← \((A[0] − B[0])\)
3: for \(i\) from 1 to \(t − 1\) do
4: \((carry, C[i])\) ← \((A[i] − B[i] − carry)\)
5: end for
6: if \(carry = 1\) then
7: \(add\) \(p\) to \(c = (C[t−1], . . . , C[2], C[1], C[0])\)
8: end if
9: Return(c)

Integer Multiplication Module: We adopt a hybrid approach to integer multiplication through a combined schoolbook [28] and Karatsuba-Ofman [12] approach. The motivation behind adopting a hybrid approach is as follows. Our target FPGA board has DSP blocks with 27x18 bit wide multipliers. However, both multi-word arithmetic and schoolbook algorithm require operands to be split symmetrically (i.e., both operands must have the same base). Therefore, the maximum we can use is 16x16 bit wide multiplier to multiply two 256-bit operands (16 being the largest number that can split 256 symmetrically). If we set \(W\) as 16, we will have \(t = 16\) words to operate on, thus implementing just the schoolbook multiplication algorithm [12] will lead to a high latency (at least 256 clock cycles), which is not acceptable as many multiplications are performed in point arithmetic. Therefore, the use of hybrid approach lowers the latency of a multiplication performed using multi-word approach with schoolbook multiplication. The steps of our proposed approach are shown in Algorithm 3.
implementing different cryptographic schemes) exploit Karatsuba-Olfman reduction is very expensive to implement in hardware due to

\[ n \text{ reduction with } 2^{256} \text{ to } \]

ger multiplication yields a result, we can perform
\[ W \]

Algorithm 3: Hybrid Integer Multiplication

**Input:** Integers \( a, b \in \{0, p-1\} \), \( t = 8 \), \( l = 16 \)

**Output:** \( c = (a,b) \)

1. Set \( (A[1-\ldots,A[0]) \leftarrow a, (B[1-\ldots,B[0]) \leftarrow b \)
2. Set \( C[i] \leftarrow 0 \) for \( 0 \leq i \leq 2t-1 \)
3. for \( i \) from 0 to \( t-1 \) do
4. \( U \leftarrow 0 \)
5. for \( j \) from 0 to \( t-1 \) do
6. \( (a_1, a_0) \leftarrow A[i], (b_1, b_0) \leftarrow B[i] \)
7. \( ab = a_1b_12^{2l} + [(a_0 + a_1)(b_0 + b_1) - a_1b_1 - a_0b_0]2^l + a_0b_0 \)
8. \( (U,V) \leftarrow C[i+j] + ab + U \)
9. \( C[i+j] \leftarrow V \)
10. **end** **for**
11. \( C[i+t] \leftarrow U \)
12. **end** **for**
13. Return\( (c) \)

We first take the schoolbook multiplication algorithm and set the parameter \( W \) as 32 (twice the input width of a multiplier in DSP block) to split 256-bit operands into \( t = 8 \) 32-bit words. Next, we target the 32-bit operands and split them into 16-bit operands (see Figure 3) and multiply these 16-bit operands using Karatsuba-Ofman equation as follows:

\[ ab = (a_1b_12^{2l} + [(a_0 + a_1)(b_0 + b_1) - a_1b_1 - a_0b_0]2^l + a_0b_0) \quad (3) \]

where \( l \) is 16. Moreover, as multiplication operations (line 7 in Algorithm 3) are independent, we unroll the loops in the algorithm to perform multiplications and accumulations in parallel. As a result, we can perform 256-bit integer multiplications in just 39 clock cycles using the schoolbook multiplication algorithm with the Karatsuba-Ofman split to utilize the available wide multipliers in DSP blocks efficiently. Note that various existing works [39, 42, 43] (implementing different cryptographic schemes) exploit Karatsuba-ofman/Karadula algorithm to perform modular multiplication on an FPGA. Therefore, novelty of this work lies in the way we combine schoolbook multiplication and Karatsuba-ofman algorithm together to implement a low-latency, parallel multiplier.

![Figure 3: Schoolbook+Karatsuba-Ofman multiplication approach.](image)

**Algorithm 4: Fast Reduction Modulo \( P \)-256 Algorithm**

**Input:** A 512-bit integer \( c = (c_{15}, \ldots, c_2, c_1, c_0) \) in base \( 2^{32} \)

**Output:** \( r = c \mod P \)

1. \( s_1 = (c_7, c_6, c_5, c_4, c_3, c_2, c_1, c_0) \)
2. \( s_2 = (c_{15}, c_{14}, c_{13}, c_{12}, c_{11}, 0, 0, 0) \)
3. \( r = s_1 + s_2 \) if \( (r \geq p) \) ? \( r - p : r \)
4. \( r = r + s_2 \) if \( (r \geq p) \) ? \( r - p : r \)
5. \( r = r + s_4 \) if \( (r \geq p) \) ? \( r - p : r \)
6. \( s_4 = (c_{15}, c_{14}, 0, 0, 0, c_{10}, c_9, c_8) \)
7. \( r = r + s_4 \) if \( (r \geq p) \) ? \( r - p : r \)
8. \( s_5 = (c_8, c_{13}, c_{15}, c_{14}, c_{13}, c_{11}, c_{10}, c_9) \)
9. \( r = r + s_5 \) if \( (r \geq p) \) ? \( r - p : r \)
10. \( s_6 = (c_{10}, c_8, 0, 0, 0, c_{13}, c_{12}, c_{11}) \)
11. \( r = r - s_6 \) if \( (r < 0) \) ? \( r + p : r \)
12. \( s_7 = (c_{11}, c_9, 0, 0, c_{15}, c_{14}, c_{13}, c_{12}) \)
13. \( s_8 = (c_9, 0, c_{10}, c_9, c_8, c_{15}, c_{14}, c_{13}) \)
14. \( s_9 = (c_{14}, 0, c_{11}, c_{10}, c_9, 0, c_{15}, c_{14}) \)
15. \( r = r - s_8 \) if \( (r < 0) \) ? \( r + p : r \)
16. \( s_9 = (c_{13}, 0, c_{11}, c_{10}, c_9, 0, c_{15}, c_{14}) \)
17. \( r = r - s_9 \) if \( (r < 0) \) ? \( r + p : r \)
18. Return\( (r) \)

Fast \( P \)-256 Modular Reduction Module: The result of an integer multiplication yields a 512 bits result that needs to be reduced to 256 bits by performing modular reduction. In point arithmetic, modular reduction is performed using the prime \( p = P \)-256 while other modular reductions in ECDSA verification engine are performed using the other prime, i.e., the order of the curve \( n \). Modular reduction with \( n \) follows this discussion. Either ways, 256-bit modular reduction is very expensive to implement in hardware due to large division operation. We observe that a single modular reduction using the \( \% \) operator in Verilog requires about 37,000 LUTs on the target FPGA, which is quite expensive. Therefore, efficient implementation of modular reduction is crucial to the design of an ECDSA verification engine.

NIST recommends a fast modulo reduction \( P \)-256 algorithm [12] as \( p = P \)-256 is a general Mersenne prime [33]. The algorithm replaces large division operations with simple additions and subtractions by exploiting the structure of this Mersenne prime. Therefore, by using this algorithm, we can perform the 256-bit modular reduction using two left shifts (multiplication by 2), four additions, and four subtractions. However, the result generated from this algorithm can be in the range \(-4p\) to \(5p\) instead of \(0\) to \(p\). So we need to perform a correction by either adding to the result or subtracting from the result, a suitable value of \(p\) within this range. This correction step, however, requires performing many 256-bit comparisons to figure out the exact range in which the result lies. On FPGAs, a 256-bit comparator leads to long carry chains impacting the timing constraints of the design adversely. Therefore, to avoid performing many large parallel comparisons at once, we check the results immediately after each step of the computation. The steps of our proposed fast modulo reduction \( P \)-256 algorithm are shown in Algorithm 4. We can see that on line 2 of the algorithm as we perform addition, we perform an immediate correction by comparing the result of addition with \(p\). Similarly, after subtraction operation (lines 10, 12, 14, and 16), we compare the result with \(0\) to see if it is negative and correct it accordingly.

From Algorithm 4, it is evident that we avoid using many 256-bit wide comparators in parallel, but we still need a 256-bit comparator to check if the intermediate result is \(\geq p\) or not. To avoid doing so, we further exploit the structure of the Mersenne prime and
propose an efficient algorithm to perform this comparison without actual 256-bit comparators. Our Algorithm 5 is based on the following observation. We can split P-256 into four parts as follows:

\[ P_0 = P[95 : 0] = ffffffff \]
\[ P_1 = P[191 : 96] = 0, P_2 = P[223 : 192] = 1 \]
\[ P_3 = P[255 : 224] = ffffffff \]

Using these four parts, we can generate the following four conditions:

- \( C_0 \) \& \( P_0 = 1, C_1 = P_1 = 0, C_2 = P_2 = 0, C_3 = \& P_3 = 1 \)
- Here, an AND (\&) reduction on \( P_0 \) gives a 1, \( P_1 \) is 0, \( P_2 \) is 1, and again an OR reduction on \( P_3 \) gives a 1. The algorithm starts by splitting the input integer \( r \) in a similar fashion as \( P-256 \) and an additional \( r_4 \) for the 257th bit (as the input integer is of 257-bits). First, we check if \( r_4 = 1 \), then \( r \) is definitely greater. However, if \( r_4 = 0 \), we need to check for other conditions. If \( r_2 > 1 \) or \( r_1 > 0 \) (line 3), then we know that \( r > p \) else if all the four conditions on line 5 are satisfied, then \( r = p \). This algorithm converts 256-bit wide comparisons to four 1-bit comparisons and can be efficiently implemented in hardware using bit-slicing and unary \& operator.

**Modular Reduction over \( n \) using Barrett Reduction:** We propose to use the standard Barrett reduction algorithm [12] for modulo reduction over the prime \( n \). Barrett reduction does not exploit the structure of \( n \) but computes \( r = z \mod n \), by computing a value \( \hat{q} \), which when multiplied with \( n \) and subtracted from \( z \) will give the desired modular reduction value \( r \). The algorithm requires selecting a base \( b \), which when chosen as a power of two gives an efficient implementation in hardware. We select \( b \) as 4 and we precompute the parameters of Barrett reduction \((k, \mu)\) as these parameters are fixed and do not change at any point in computation.

Our modified hardware-friendly version of the Barrett reduction is shown in Algorithm 6. In our hardware implementation, the division operations are performed using right shift operation (line 1) and modular reductions are performed using AND operation (line 2). This optimization is possible because \( b \) is a power-of-2 and for powers-of-2, modular reduction can be efficiently done by masking the lower-order bits using AND operation. Thus, we avoid all large division operations. However, we need to perform two large 258-bit multiplications as the parameter \( \mu \) is a 258-bit integer.

**Algorithm 5: Efficient Comparison with P-256**

**Input:** A 257-bit integer \( r \) with \( 0 \leq r < 2p \), conditions \( C_0, C_1, C_2, \) and \( C_3 \)

**Output:** \( r \geq p \)

1. \( r_0 = \& r[95 : 0], r_1 = r[191 : 96], r_2 = r[223 : 192], \)
\( r_3 = \& r[255 : 224], r_4 = r[256] \)
2. if \((r_4 = 1 \text{ or } (r_3 = C_3 \text{ and } r_2 > C_2 \text{ or } (r_2 = C_2 \text{ and } r_1 > C_1)))) \) then
   3. return(\text{greater})
4. else if \((r_4 = 0 \text{ and } r_3 = C_3 \text{ and } r_2 = C_2 \text{ and } r_1 = C_1 \text{ and } r_0 = C_0) \) then
   5. return(\text{equal})
6. end if

**Algorithm 6: Hardware-friendly Barrett Reduction**

**Input:** \( n, b = 4, k = [\log_b(n)] + 1, 0 \leq z < b^{2k}, \) and \( \mu = [\frac{k^k}{n}] \)

**Output:** \( z \mod n \)

1. \( \hat{q} \leftarrow (z > 2(k - 1)) \cdot (\mu > 2(k + 1)) \)
2. \( r \leftarrow z \& (b^{k+1} - 1) - \hat{q} \cdot n \& (b^{k+1} - 1) \)
3. if \((r < 0) \) then
   4. \( r \leftarrow r + b^{k+1} \)
5. end if
6. while \((r \geq n) \) do
7. \( r \leftarrow r - n \)
8. end while
9. return(\text{result})

For 258-bit multiplication, we again use the hybrid approach proposed in Algorithm 3. However, we set the parameter \( W = 6 \) and split the input operands into 43-bit multi-word integers. In addition, instead of a single Karatsuba-Ofman split as in Algorithm 3, we perform a two-level Karatsuba-Ofman split to efficiently leverage the DSP blocks for 43-bit multiplications. At level-1, we split 43-bit operands into 32- and 11-bit integers. Then at level-2, we again split 32-bit integers into 16-bit integers (see Figure 4). Thus, effectively we perform only 16-bit \( \times 16 \)-bit, 16-bit \( \times 11 \)-bit, and 11-bit \( \times 11 \)-bit multiplications instead of 43-bit multiplication. For example, a 43-bit multiplication can be performed as follows:

**Step-1:** Split \( A[42 : 0] \) into \( a_0 \leftarrow A[10 : 0] \) and \( a_1 \leftarrow A[42 : 11] \)
**Step-2:** Split \( B[42 : 0] \) into \( b_0 \leftarrow B[10 : 0] \) and \( b_1 \leftarrow B[42 : 11] \)
**Step-3:** \( \bar{U}_0, c_1 \leftarrow a_0 + b_0 \| b_1 \) // 11-bit\( \times 11 \)-bit multiplication
**Step-4:** \( \bar{U}_1, c_1 \leftarrow (a_0 + b_1) + \bar{U}_0 \) // 11-bit\( \times 32 \)-bit multiplication
**Step-5:** \( \bar{U}_2, c_2 \leftarrow c_1 + (a_1 + b_0) \) // 11-bit\( \times 32 \)-bit multiplication
**Step-6:** \( \bar{U}_3, c_3 \leftarrow (a_1 + b_1) + \bar{U}_2 \) // 32-bit\( \times 32 \)-bit multiplication
**Step-7:** \( c \leftarrow (U_0, c_3, c_2, c_0) \) // 86-bit multiplication result

In steps 4 and 5 above, we need to perform an 11-bit \( \times 32 \)-bit multiplication, which we further simplify as follows:

**Step-1:** Assign \( a_1_{lower} \leftarrow a_1[15 : 0] \) and \( a_1_{higher} \leftarrow a_1[31 : 16] \)
**Step-2:** Pad a 0 (in MSB) to \( b_0 \) to make it 12-bits
**Step-3:** \( r_{lower} \leftarrow a_1_{lower} \times b_0 \| a_1_{lower} \) // 32-bits
**Step-4:** \( r_{higher} \leftarrow a_1_{higher} \times b_0 \| a_1_{higher} \) // 28-bits
**Step-5:** \( r_{mid} \leftarrow r_{lower} \times b_{[27 : 16]} + r_{higher} \) // 11-bits
**Step-6:** \( r_{higher} \leftarrow r_{higher} \times b_{[26 : 12]} + r_{mid} \) // 12-bits
**Step-7:** result \( \leftarrow (r_{higher} \times b_{[26 : 12]}, r_{mid} \times b_{[11 : 0]}, r_{lower} \times [15 : 0]) \)

![Figure 4: Proposed 258-bit multiplication approach.](image-url)
Note that in step-5 above, $r_{\text{mid}}$ is 13 bits instead of 12 bits to account for an additional carry bit after addition. Note that although the steps listed above are specific to a 43-bit multiplier, they can be generalized to any bit-width that is not a multiple of the DSP multiplier’s input bit-width (assumed 16 in our case) and then can be efficiently implemented leveraging the DSP blocks.

**Modulo Inverse Module:** NIST recommends using Extended Euclidean algorithm [23] to compute modulo inverse in ECDSA verification algorithm. However, extended Euclidean algorithm is expensive to implement in hardware requiring 256-bit division and multiplication to compute quotient and remainder respectively. Second popular option, the Fermat’s theorem [38] is comparatively efficient to implement in hardware as it requires only multiplications. However, it involves 267 modular multiplications leading to a higher latency. Fermat’s theorem approach is more suitable when a side-channel resistant implementation (computation time is independent of the input) is a must.

We choose to implement an optimized, faster modulo inverse algorithm proposed by Chen and Qin [2]. This algorithm is suitable for hardware implementation as it has very low resource footprint and also incurs a low latency. The algorithm computes a modulo inverse using only right shift and addition operations and at any given time only two 256-bit adders are operating in parallel. We observe that the latency of this algorithm ranges from 35-600 clock cycles depending on the input, however for real test cases, the latency averages close to 550 clock cycles across multiple evaluations. It is worth noting that we modified the actual algorithm to take modulus as an input because we leverage the same algorithm to perform modulo inverse with respect to $n$ (line 4 of Algorithm 1) as well as to convert projective Chudnovsky coordinates back to affine coordinates wherein we need to compute modulo inverse with respect to $p$.

### 5.2 Point Arithmetic

During ECDSA signature verification, we need to perform two scalar-point multiplications and one point addition operation (line 7 in Algorithm 1). We first present our generic approach to point arithmetic that can be leveraged in any application requiring fast ECDSA signature verification. We will discuss our optimized Hyperledger Fabric-specific point arithmetic approach later in Section 6.

We leverage the simultaneous-point multiplication (SPM) Algorithm 7, also known as “Shamir’s trick”, to operate on both the generator point ($P$) and public key coordinates ($Q$) at the same time. In addition, this algorithm eliminates the need to perform the point addition separately. We conducted an analysis on how the number of operations varies when different point representations such as binary, NAF, joint-sparse form (JSF), and width-$w$ NAF are used in Algorithm 7. Table 2 shows that point double operations largely remain the same while point addition operations can be reduced to as low as 112 when width-$w$ NAF is used. Note that width-$w$ NAF conversion can be done in hardware using the algorithm-3.35 from [12], and is trivial in comparison to point arithmetic. We use $w = 4$ to keep the storage requirements minimal.

In Algorithm 7, point double operation (line 6) and point additions (lines 8, 10, 13, 15) cannot be done in parallel as they depend on each other. However, we reduce the number of these operations by computing various values of $G$ ($3G, 5G, 7G, 9G, 11G, 13G, 15G$) offline and storing them in BRAM because $G$ is known in advance. This requires 1120 bytes of storage space but reduces the computation of line 1 to only $K$ ($3K, 5K, 7K, 9K, 11K, 13K, 15K$) in hardware. For these values, $3K$ is computed by performing a point double on $K$ followed by a point addition. We store the $2K$ value temporarily and reuse it; for example, $5K$ is computed by performing a point addition between $3K$ and $2K$. Therefore, we only need one point double and seven point addition operations in hardware to compute all the required values. Overall, we significantly reduce the number of point double and addition operations with the use of width-$w$ NAF, and offline and optimized computation for $G$ and $K$.

### 5.3 ECDSA Verification Engine

Figure 5(a) depicts the architecture of our generic ECDSA verification engine, using the modular and point arithmetic modules described earlier. We instantiate only one module corresponding to a unique modular arithmetic operation to keep the resource utilization low. Figure 5(b) depicts the data flow in the ECDSA verification engine using SPM algorithm. Even with single instantiation of the modular arithmetic modules, we leverage as much parallelism as possible by scheduling different operations in parallel to efficiently utilize the hardware resources. For example, we

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**Algorithm 7:** Width-$w$ NAF method for SPM

**Input:** Width $w$, integers $k_1$ and $k_2$, points $P$ and $Q$  
**Output:** $k_1P + k_2Q$

1. Compute: $iP$ and $iQ$ for $i \in \{1, 3, \ldots, 2^w - 1\}$
2. Compute $\text{NAF}_{w}(k_1)$ and $\text{NAF}_{w}(k_2)$
3. $l = \max\{\ell_1, \ell_2\}$ where $\ell_1$ and $\ell_2$ are lengths of $\text{NAF}_{w}(k_1)$ and $\text{NAF}_{w}(k_2)$
4. $\mathcal{A} = \infty$
5. for $i$ from $l - 1$ down to 0 do
6. $\mathcal{A} = 2\mathcal{A}$
7. if $k_1[i] > 0$ then
8. $\mathcal{A} = \mathcal{A} + k_1[i]P$
9. else
10. $\mathcal{A} = \mathcal{A} - k_1[i]P$
11. end if
12. if $k_2[i] > 0$ then
13. $\mathcal{A} = \mathcal{A} + k_2[i]Q$
14. else
15. $\mathcal{A} = \mathcal{A} - k_2[i]Q$
16. end if
17. end for
18. Return($\mathcal{A}$)

| Representation | Point double | Point add |
|----------------|--------------|-----------|
| Binary         | 256          | 193       |
| NAF            | 256          | 148       |
| JSF            | 256          | 130       |
| width-$w$ NAF  ($w = 4$) | 257 | -112 |
perform the NAF$_w(k_2)$ conversion in parallel with the second modular multiplication. Similarly, NAF$_w(k_1)$ conversion happens in parallel to the computation on line 1 in Algorithm 7. Thus, no additional clock cycles are spent in NAF conversions. From amongst all the modules, integer multiplication and modular reduction are the heavily utilized modules.

It is worthwhile to reiterate that an additional point addition operation is not required in this implementation because it is absorbed in the SPM operation. However, after the multiple-point multiplication operation, we need an additional operation to convert $x$ from projective Chudnovsky coordinate back to affine coordinate for final comparison.

6 ECDSA VERIFICATION FOR HL FABRIC

In this section, we propose optimizations in the context of permissioned blockchains specifically HL Fabric. We exploit the fact that some parameters are fixed a priori while other parameters are available in advance, and hence both of these can be preprocessed to speedup ECDSA verification operation. More specifically, we take advantage of the fact that the generator point $G$ is fixed and the public key coordinates $K = (x_K, y_K)$ are known well in advance before the ECDSA verification starts. The ProtocolProcessor in Blockchain Machine (see Figure 1) processes the incoming data and extracts the public key and ECDSA signature information. Therefore, as soon as the public key coordinates are available, we can start processing them. With this goal in mind, we leverage the fixed-point multiplication (FPM) algorithm (refer Algorithm 8) to perform point arithmetic instead of simultaneous-point multiplication algorithm.

The algorithm starts by precomputing various powers-of-2 point multiplications for a point $P$ which is known a priori (for example, when $w = 4$, then precomputations will be $P$, $16P$, $256P$, and so on). As the generator point is fixed, we precompute these values offline and store the values in the BRAM on FPGA. For the public key coordinates, we design a separate precompute block, outside of the ECDSA verification engine, which runs binary scalar-point multiplication algorithm (algorithm-3.27 in [12]) with point double operations only to precompute the values mentioned earlier (i.e., $P$, $16P$, etc). Point addition operations are not required as we are computing power-of-2 point multiplications only, which can be computed using successive point double operations. We further optimize the precompute block by reducing the number of point double operations that it needs to perform. For example, if we want to compute $256P$, we need not start point double operations all the way from $P$. Instead, we can use the value of $16P$ that was computed in the previous step, thus reducing the number of point double operations from $w$ to $w$ in each step $i$ where $0 \leq i \leq d$. This optimization helps reduce the number of point double operations from over 8000 to only 252 when $w = 4$ and $d = 64$.

The precompute block computes the required point values for public key and stores them in the BRAM. The computation within the actual ECDSA verification reduces to lines 4-8 in Algorithm 8. Consequently, ECDSA verification comprises of just point addition operations with the point double operations moved to precomputation. We use the fixed-base (with base $w = 4$) NAF windowing method to reduce the number of point addition operations. Note that the fixed-point multiplication algorithm is executed twice; once for the generator point $G$ accessing offline computed point values in line 1, and second time for the public key $K$ accessing precomputed point values in line 1.

Figures 6 and 7(a) show the architecture of our HL Fabric-specific ECDSA verification engine. The precompute block is placed inside the ProtocolProcessor to store all the required point values in BRAM. With projective Chudnovsky coordinates, we need about 20 KB of memory to store all the precomputed point values (including point

![Figure 5: Generic ECDSA verification engine: (a) Architecture (b) Data flow.](image)

![Algorithm 8: Fixed-base NAF windowing method for FPM](image)

![Figure 6: Integration of Precompute with ProtocolProcessor.](image)
In a permissioned blockchain like HL Fabric, the number of nodes are limited and hence the number of unique identities (public keys) is limited and those identities are known apriori. In a typical HL Fabric network, there may only be tens of unique identities, thus storage of precomputed points will not incur a high memory overhead. The precompute block has its own modular arithmetic modules and the finite state machine (FSM) controlling the movement of data between these modules. The ECDSA verification engine has its own set of modular arithmetic modules. We again instanciated only one module per modular arithmetic operation to keep the resource utilization low. This is beneficial especially in Blockchain Machine where it is desirable to have many ECDSA verification engines within the BlockProcessor module.

Figure 7(b) depicts the data flow in our ECDSA verification engine with the precompute block. The precomputed points are read from the BRAM by the ECDSA verification engine. The read from BRAM is not a bottleneck as read will happen once in a while and then hundreds of clock cycles are spent on processing the data. Since the number of unique public keys is limited, the precompute block is executed only when a new public key is encountered and the precomputed values are stored in the BRAM. Hence, the precompute block does not become the bottleneck. Both in precompute and ECDSA verification engine, with single instanciation of the modular arithmetic modules, most operations are performed serially. However, we leverage as much parallelism as possible by scheduling different modular operations in parallel. For example, the NAF conversion of \( k_2 \) happens in parallel with the second modular multiplication involving \( k_1 \). Similarly, the NAF conversion of \( k_1 \) also happens in parallel with the first fixed-point multiplication. After the fixed-point multiplication, a point addition operation is required (line 7 of Algorithm 1) and conversion back to affine coordinates for comparison.

7 EVALUATION

We designed our ECDSA verification engine and all of its modules in Verilog 2001 and synthesized the design using Xilinx Vivado design suite 2019.2. For functional verification, we generated the test cases using open-source code from OpenSSL library [26] and also from the actual data, i.e., public key, signature, and hash used in Hyperledger Fabric. We also successfully verified the test vectors [24] from NIST for \( P \cdot 256 \) (along with SHA-256) ECDSA signature verification. We implement the design on Xilinx Alveo U250 FPGA. We synthesize our design on this FPGA board because blockchains are typically deployed on a cloud server with FPGA accelerator card. Since our goal is to integrate the ECDSA engine into a blockchain hardware accelerator [16], which is quite complex and operates at 250 MHz frequency, we limit the operating frequency of our ECDSA verification engine to 250 MHz even when it is possible to obtain higher frequencies with DSP blocks like in [10]. This restriction on frequency will also enable better scalability within the blockchain accelerator by instantiating multiple ECDSA engines for distributed computation.

Throughout this section, we report frequency (freq.) in MHz, latency in clock cycles, and throughput (TP) in operations per second. When comparing our work with existing state-of-the-art implementations, we cautiously compare the clock cycles of different designs instead of absolute runtimes to overcome the inherent improvements from upgraded technologies and operating frequencies, and hence provide a fair comparison. In an ideal situation, the existing works should have been implemented on the Alveo U250 FPGA board as well. However, those designs are not open-source and implementation of each requires significant effort. Furthermore, we do not present direct comparison results with CPU/GPU implementations because our goal is not to compete with CPU/GPU implementations but to provide the best FPGA implementation that can be used in accelerators for permissioned blockchains (since they are naturally suitable for FPGA based acceleration [16]).

7.1 Modular Arithmetic

We start by discussing the area footprint and latency of the individual modular arithmetic modules as listed in Table 3. With all the proposed optimizations, our modular arithmetic modules incur low resource utilization. The integer multiplication module consumes the most LUTs, which can be reduced using BRAM-based optimizations. We, however, leave this optimization for future work. Most modules perform fast computations except for Barrett reduction which has the highest latency because of two serial 258-bit multiplications. We made this design choice to keep the hardware resource utilization low. Moreover, modular reduction using Barrett reduction is performed only in lines 5, 6, and 8 of Algorithm 1, which is not the critical path (line 7 is the critical path in ECDSA verification).
perform SPM operation using width-4 NAF approach. However, for fair comparison with [10], which uses a binary representation, we estimated the latencies using the number of operations performed in Algorithm 7 with binary representation. More importantly, our SPM with width-4 NAF incurs about half the latency owing to our faster modular arithmetic modules.

### 7.3 ECDSA Verification Engine

Table 5 presents the hardware resource utilization and latency of the ECDSA verification engine. Our ECDSA verification engine takes ~190,000 clock cycles for a single signature verification leading to a throughput of 1,315 signature verifications per second. Although many prior works have accelerated point arithmetic on FPGA, most works did not implement the entire ECDSA verification algorithm. We found only two relevant comparable works in literature that accelerated ECDSA signature verification for NIST P-256 on FPGA, which are reported in Table 6. Glas et al. [8] reported the implementation results of the complete signature generation and verification unit on a Xilinx XC5VLX110T Virtex-5 FPGA. Their signature verification unit includes a hash generator IP which incurs a latency of 68 clock cycles that we have adjusted accordingly for a fair comparison. Their design achieves a throughput of 110 signature verifications per second that is about 12× lower than the throughput of our ECDSA verification engine.

Knežević et al. [18] did an ASIC implementation for ECDSA verification, but reported performance numbers by synthesizing their design on a Xilinx Virtex-4 FPGA. Their design results in a throughput of 475 signature verifications per second, which is ~2.8× lower than the throughput of our ECDSA verification engine. Note that this design is primarily an ASIC implementation, which means that it has a different optimization flow, resulting in a much lower operating frequency and requiring less clock cycles. Therefore, we do not compare frequency and latency for this design, but compare the throughput for a fair comparison. We do not compare the hardware resource utilization as prior designs use different FPGA boards for implementation. Moreover, we cannot estimate the hardware cost of these existing designs [8, 18] for Alveo U250 FPGA as these designs are not open-sourced.

### 7.4 ECDSA Verification Engine for HL Fabric

Table 7 presents the hardware resource utilization and latency of our ECDSA verification engine with precompute block. We observe that the precompute block incurs a latency of ~120,000 clock cycles. Then, the actual ECDSA verification engine requires only ~92,000 clock cycles to perform a single signature verification. With

#### Table 3: Hardware results of various modular arithmetic modules.

| Operation          | LUT  | FFs | DSP | Latency |
|--------------------|------|-----|-----|---------|
| Modular subtraction| 616  | 781 | 1   | 10      |
| Integer multiplication| 5471 | 7980| 128 | 39      |
| P-256 Modular Reduction| 2225 | 789 | 0   | 19      |
| Barrett Reduction  | 2130 | 3597| 9   | 1,552   |
| Modulo Inverse     | 3503 | 1313| 0   | 550     |

#### Table 4: Performance comparison of point arithmetic.

| Operation          | Platform | Freq. | Latency | TP  |
|--------------------|----------|-------|---------|-----|
| PA [Our work]      | Alveo U250 | 250   | 622     | 402K|
| PA [10]            | Virtex-4  | 375   | 980     | 382K|
| PD [Our work]      | Alveo U250 | 250   | 435     | 574K|
| PD [10]            | Virtex-4  | 375   | 700     | 535K|
| PM [Our work]      | Alveo U250 | 250   | 190,976 | 1,309|
| PM [10]            | Virtex-4  | 375   | 303,450 | 1,236|
| PM [37]            | Virtex-2 Pro | 108.2 | 451,733 | 240  |
| PM [19]            | Virtex-7  | 124.2 | 462,520 | 268  |
| PM [22]            | Virtex-2 Pro | 67    | 567,500 | 118  |
| PM [21]            | Virtex-2  | 39.5  | 960,000 | 41   |
| PM [31]            | Virtex-E  | 39.7  | 987,500 | 40   |
| SPM [Our work]     | Alveo U250 | 250   | 231,406 | 1,080|
| SPM [10]           | Virtex-4  | 375   | 366,905 | 1,022|
| SPM-NAF [Our work] | Alveo U250 | 250   | 181,024 | 1,381|

Note that our modular subtraction module is 1.8× faster and our modular multiplication (integer multiplication+P-256 Modular Reduction) is 1.2× faster than the implementations in state-of-the-art work [10].

#### 7.2 Point Arithmetic

We first evaluate the performance of our point addition (PA) and point double (PD) operations. For a fair comparison, we also report the latencies from state-of-the-art FPGA-based work [10], which also uses projective Chudnovsky coordinates like our implementation. We observe that both of our point add and double operations are ~1.6× than their point add and double operations in terms of clock cycles (refer Table 4). Note that their design involves a dual clock which is much more complicated to implement than our design, which uses only a single clock throughout the entire design. Moreover, the authors in [10] focus on optimizing only the point arithmetic, and do not implement the entire ECDSA verification algorithm. This makes it much easier for their stand-alone point arithmetic modules to run at higher frequencies.

Now we compare the latencies of our scalar point multiplication (PM) with state-of-the-art works that implement scalar point multiplication (refer Table 4). We observe that our PM is ~1.6× to ~5× faster than these existing works in terms of clock cycles. As most of these prior implementation were done using binary double and add algorithm, our PM is also implemented using the same approach. Note that implementation done by Kudithi et al. [19] works with affine coordinates while rest of the works use projective coordinates. Next, we compare the latencies of our simultaneous-point multiplication (SPM) operation. As mentioned in Section 5.2, we

#### Table 5: Performance comparison of ECDSA engine.

| Design    | LUT   | FFs  | DSP | BRAM | Latency |
|-----------|-------|------|-----|------|---------|
| ECDSA verf. | 24394 | 10961| 137 | 5    | 190,000 |

#### Table 6: Performance comparison of ECDSA engine.

| Work        | Platform | Freq. | Latency | TP  |
|-------------|----------|-------|---------|-----|
| Our work    | Alveo U250 | 250   | 190,000 | 1,315|
| [8]         | Virtex-5  | 50    | 454,140 | 110 |
| [18]        | Virtex-4  | 33.3  | 69,972  | 475 |
this approach, we achieve a throughput of 2,717 signature verifications per second.

We also evaluate the HL Fabric-specific ECDSA verification engine in the context of Blockchain Machine. Table 8 presents the throughput (transactions per second) of Blockchain Machine with both the generic and Hyperledger Fabric-specific ECDSA verification engines. We observe a 2× improvement in throughput with our precompute optimization. We also change the number of ECDSA verification engines from 4 – 10, and observe that both types of engines scale the throughput in a similar trend (~1.57× improvement).

8 CONCLUSION

In this work, we focused on an FPGA-based efficient implementation of ECDSA signature verification, in order to improve the performance of permissioned blockchains that aim to use FPGA-based accelerators. We presented several FPGA-specific algorithmic optimizations for modular arithmetic modules. With efficient utilization of DSP blocks on FPGA, we showed on average 1.5× speedup compared to [10]. We also presented optimizations for SPM and FPM algorithms, and used projective Chudnovsky coordinate with optimal width NAF representations. With these optimizations, we observed on average 3.2× speedup in our point arithmetic operations compared to [10, 19, 21, 22, 31, 37]. Our ECDSA verification engine, using these modular and point arithmetic modules, performs a signature verification in 760μs resulting in a throughput of 1,315 verifications per second, which is ~2.5× faster than [8, 18].

With HL Fabric-specific optimizations, our ECDSA verification engine can perform a signature verification in 368μs resulting in a throughput of 2,717 verifications per second.

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