Nonvolatile Programmable WSe$_2$ Photodetector

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Optoelectronic devices with nonvolatile memory are an important component in a wide variety of applications ranging from optoelectronic random-access memories, with the advantage of using optical stimuli as an added parameter, to complex artificial neuromorphic networks that pretend to mimic the working schemes of the human brain. In the past few years, 2D materials have been proposed as attractive candidates to build such optoelectronic devices with memory due to their excellent optoelectronic properties and high sensitivity to external electric fields. Here, a WSe$_2$ monolayer p–n junction working as a nonvolatile programmable photodetector is reported, that, enabled by a split-gate configuration with embedded charge-trapping layers, is capable of retaining custom responsibility values over time, prior configuration by the user. Once configured, this photodetector can operate without external applied bias voltage as a self-driven photodetector, as well as without external back-gate voltage thanks to the charge stored in the floating gates. Furthermore, the device shows a remarkable performance, with open-circuit voltage around 1 V at approximately 270 W m$^{-2}$ white light, fill factor higher than 30%, and fast response times. This programmable photodetector sets a new concept as a building block in more complex image-sensing systems.

1. Introduction

P–n junctions are important building blocks in current optoelectronic technology. From active-pixel sensors, to photovoltaic solar cells or light-emitting diodes, p–n junctions play a major role in light–electricity conversion and energy harvesting. In the past decade, 2D materials have been widely studied as active material in optoelectronic devices such as photodetectors,\textsuperscript{[1–4]} photodiodes, solar cells, or light emitters,\textsuperscript{[5–11]} due to their remarkable properties such as high photoconductive gain or fast photoresponse. The wide spectrum of proposed architectures for the construction of 2D p–n optoelectronic devices covers from homojunctions with capacitive or chemical doping of an ambipolar semiconducting channel, to vertical or lateral heterostructures between two differently doped materials.\textsuperscript{[12]} Within this family, the lateral homojunctions based on electrostatic doping via split-gate have shown remarkable performance in the past and, moreover, they have already been implemented in applications involving photodetectors arrays\textsuperscript{[13]} due to the high photoresponse tunability provided by the split-gates, which allows to set a custom responsivity on each individual sensor. However, these split-gate photodetectors present the drawback of requiring four terminals, that is, four electrical connections on each unit, resulting in a substantial amount of cables when implemented in larger-scale arrays.

Here we demonstrate a nonvolatile programmable photodetector that uses the ambipolar nature of WSe$_2$ to locally dope the active material with custom polarizations via a split-gate configuration, allowing setting any desired responsivity value and, additionally, incorporates charge-trapping layers, similar to those employed in nonvolatile electronic\textsuperscript{[14–19]} and optoelectronic memories,\textsuperscript{[20–27]} that enable the retention of the configured performance over time. The device exhibits remarkable optoelectronic performance as both memory and self-driven photodetector, with various-current voltages around 1 V at approximately 270 W m$^{-2}$ white light, fill factor higher than 30%, and fast respond times. Our programmable p–n junction architecture may establish a new concept as building block in more complex programmable photodetector-based arrays.

2. Results and Discussion

The programmable photodetector, sketched in Figure 1a (an optical microscopy image is shown in Figure S1, Supporting Information), is based on a split-gate configuration photodetector with monolayer WSe$_2$ as active material, similar to that reported in previous works.\textsuperscript{[6,7,10,28]} The key difference in our design with respect to previous works is the addition of a charge-trapping layer (2 nm-thick Au nanoclusters) embedded in the insulator and covering only the region over the back-gate electrodes. Such floating gate allows accumulating charge and, consequently, setting and storing the responsivity of the device over time. We have chosen Au nanoclusters as the floating gate material due to its good retention capability.\textsuperscript{[15,24]} Our device structure differs from that reported by Li et al.,\textsuperscript{[23]} where the authors employ a graphene layer embedded in the insulator as semi-floating gate, covering only part of the WSe$_2$, allowing thus to program the device as a p–n or n–n junction for nonvolatile photodetection or logic rectification. In our case, the device structure consists of two Ti/Au (5 nm/30 nm) electrodes, fabricated by standard e-beam lithography on a SiO$_2$...
substrate, acting as back-gate electrodes (\(V_{g1}\) and \(V_{g2}\), control gates hereafter) and separated a distance of \(\approx 400\) nm. On such structure, an insulating 20 nm-thick \(\text{Al}_2\text{O}_3\) layer is grown by atomic layer deposition (ALD), followed by the e-beam-induced evaporation of the 2 nm-thick Au nanoclusters (floating gates). Finally, another 7 nm-thick layer of \(\text{Al}_2\text{O}_3\) is grown over the whole structure, followed by the transfer of a \(\text{WSe}_2\) monolayer via polydimethylsiloxane (PDMS) exfoliation/transfer technique.\[29\] In the last step, \(\text{Ti}/\text{Au}\) (5 nm/100 nm) drain-source electrodes are fabricated to electrically contact the \(\text{WSe}_2\) monolayer.

The above-described configuration with split-gates allows us to locally dope the \(\text{WSe}_2\) channel either n or p by applying negative/positive voltages. In dark conditions, the current–voltage characteristics (IVs hereafter) displayed in Figure 1b (green and blue curves) show the typical diode-like rectifying behavior when voltages with different polarization are applied to the each control gate;\[6,7,28\] namely, \(V_{g1} = -V_{g2} = -4\) V for a p–n configuration (green curve in Figure 1b), and \(V_{g1} = -V_{g2} = 4\) V for an n–p configuration (blue curve in Figure 1b). We refer the reader to Figure S2, Supporting Information, for a further analysis of the diode. Moreover, the photoresponse is observed when the device is illuminated (red and violet curves in Figure 1b, p–n and n–p configurations, respectively), yielding open-circuit voltage \(V_{oc}\) and short-circuit current \(I_{sc}\) values of \(V_{oc} = 1.03\) V \((V_{oc} = -0.94\) V) and \(I_{sc} = -31\) pA \((I_{sc} = 33\) pA) upon illumination with white light \((P_d = 273\) W m\(^{-2}\)). The S-shape in the curves around \(V_{cc}\) is commonly attributed to the influence of Schottky barriers as a result of non-ohmic contact between the drain and source electrodes and the semiconductor;\[30,31\] Therefore, it should be mentioned here that the overall photoresponse of the device is probably mediated by both the photovoltaic effect derived from the formation of a p–n junction across the semiconductor channel and the Schottky barriers formed at the interface between the Ti/Au electrodes and the \(\text{WSe}_2\) monolayer.

Further device characterization in dark yields the transfer curves displayed in Figure 1c for drain-source voltage \((V_{DS})\) values of \(V_{DS} = 2\) V and \(V_{DS} = -2\) V. In this plot, we show the back-and-forth measurement of the drain-source current \((I_{DS})\) while sweeping the control gates, although the x-axis represents only \(V_{g1}\) with \(V_{g1} = -V_{g2}\) (see Figure S3, Supporting Information, for transfer curves with symmetric control gates), demonstrating rectification of current in opposite directions for p–n and n–p configurations and an on/off ratio of \(\approx 10^3\). We observe some hysteresis between the forth and back measurements, which we attribute to charging/discharging of the floating gates. By sweeping the control gate toward higher positive voltages \((V_{g1})\), it works in the opposite way for \(V_{g2}\), electrons tunnel through the \(\text{Al}_2\text{O}_3\) layer to the floating gate via Fowler–Nordheim tunneling;\[14,32\] resulting in an accumulation of electrons that shift the threshold voltage. When the control gate voltage is swept back to negative values, electrons are removed from the floating gate, which is then discharged. In our device, however, there are two split-control-gates, which are swept with opposite polarity, charging thus the floating gates oppositely. Hence, when one of the gates is swept toward higher positive...
voltages and electrons accumulate in the floating gate, the other control gate is swept toward lower voltages, resulting thus in an accumulation of holes in the floating gate, as well as doping the semiconductor with the opposite polarization. This process leads to the formation of a lateral p–n junction in the ungated region, that is, in the trench that separates the two control gates (=400 nm). The mechanism works in the opposite way when sweeping back the control-gates. The shift in the threshold voltage is commonly referred to as memory window, which in our case yields a maximum value of \( \Delta V = 2 \text{ V} \). This memory window can also be depicted in the transfer curve of the \( I_{sc} \), that is, the current at \( V_{ds} = 0 \), upon illumination with white light (Figure 1d). We address the reader to Figure S4, Supporting Information, for further characterization. From the memory window we can estimate the charge density stored in each floating gate to be \( n = \Delta V \cdot \varepsilon_0 \cdot \varepsilon_r / d \cdot e = 4.4 \times 10^{12} \text{ cm}^{-2} \), with \( \varepsilon_0 \) the vacuum permittivity and \( \varepsilon_r \approx 8 \) that one from our grown \( \text{Al}_2\text{O}_3 \), \( E \) the elementary charge, and \( d = 20 \text{ nm} \) the thickness of the \( \text{Al}_2\text{O}_3 \) layer between the control gate and the floating gates.

We now move to the analysis of the optoelectronic information storage capability of our device. The goal of our photodetector is to retain a desired responsivity value over time after an initial setting. Hence, we first study the temporal evolution of the \( I_{sc} \) once the floating gates have been charged to demonstrate the capacity of the device to maintain a lasting current value. We probe the progression of \( I_{sc} \) over time prior polarization and charging of the floating gates by setting \( V_{g1} \) and \( V_{g2} \) (typically with \( V_{g1} = -V_{g2} \)) during a certain period and disconnecting them afterward. Figure 2a displays three consecutive one-hour-long measurements (separated by vertical dashed lines) of \( I_{sc} \) versus time upon illumination with white light \( (P_d = 273 \text{ W m}^{-2}) \), in which it is demonstrated that the floating gates remain charged and the photodetector retains the set responsivity value, that is, the current remains stable, even if the illumination is switched off and on. Furthermore, we have performed a similar measurement over days (Figure 2b), where we observe that the current drops \( \approx 35\% \) after almost two days, although its value still remains much larger than that of the dark current (highlighted by the dashed horizontal line). This drop could be attributed to poor quality of the thin insulating layer that isolates the floating gates from the semiconductor channel, which might present trap charges that discharge after some time. This issue could be solved by improving the insulator quality.[33,34] Additionally, in Figure 2c we show a set of \( I_{sc} \) values that can be configured by applying different control gate configurations, demonstrating the customizability of the photodetector performance. It should be noted here that all the values displayed in Figure 2c have been extracted from temporal measurements (see Figure S5, Supporting Information, for the full measurements).

In Figure 3 we show the temporal evolution of \( I_{sc} \) when pulses with opposite polarization are applied to each control gate. To operate a memory, the device is often programmed or erased by voltage pulses and read by applying zero voltage to the control gate. Figure 3a displays the program-erase cycles of our programmable photodetector, demonstrating that it can be programmed in any custom state, that is, the current can be set to any desired value. To that purpose, we apply a pulse with \( V_{gl} = -V_{g2} \) with a width of 2 s (illustrated by red and green dots in Figure 3), after which the control gates are left floating while the \( I_{sc} \) is still recorded. Once the pulse stops (after the mentioned 2 s) the floating gates remain charged and the device still shows a relatively constant value until another pulse with \( V_{gl} = V_{g2} = 0 \text{ V} \) is applied to the control gates, and, consequently, the device switches from programmed to erased responsivity. The process is again repeated with a pulse having a different

![Figure 2](https://example.com/figure2.png)  
*Figure 2.* a) Time-dependent evolution of the short-circuit current after program. The vertical dashed lines separate different measurements, each one lasting 1 h, without rewriting. In the middle measurement, the light \( (P_d = 273 \text{ W m}^{-2}) \) was switched-off during \( 15 \text{ min} \) and switched back on afterward. b) Time-dependent evolution of the short-circuit current over days. After almost two days, the short-circuit current value drops by \( \approx 35\% \). c) Short-circuit current value for different control gate values, showing the tunability of the responsivity. The voltage axis shows the value of \( V_{g1} \), with \( V_{gl} = -V_{g2} \).
control gate value. Figure 3b shows schematic band diagrams representing the different states on the measurements displayed in Figure 3a and c for one of the control gates (the other control gate would work the opposite way). Let us note here that, for simplicity, these diagrams do not illustrate the electron or hole current driven by the separation of electron–hole pairs due to the photoresponse when the device is upon illumination. When a positive voltage is applied to the control gate (program), electrons tunnel through the thin insulator toward the floating gate (Au nanoclusters) and holes accumulate on the WSe2 monolayer, followed by the programmed state, where the control gate is left floating and the WSe2 remains p-doped. Now, following the arrow that indicates Figure 3a, we continue with the next state in such a measurement, in which a 0 V pulse is applied to the control gate (reset), resulting in a charge balance that leaves the semiconductor channel in the off-state \((V_{g1} = V_{g2} = 0 \text{ V})\), see Figure 1d). Finally, another pulse is applied to the control gate, entering again another program state. On the other hand, if we follow the arrow indicating Figure 3c, we jump from the programmed state to a rewrite state. In this case, a pulse is applied to the control gate with opposite polarization with respect to the previous state, leading to tunneling of electrons from the floating gate to the WSe2 channel and thus resulting in an n-doping of the channel. Therefore, a current with opposite sign with respect to the previous state will flow, as it can be depicted in Figure 3c. This measurement demonstrates that our device could be employed in applications requiring adjusting the responsivity values such as cameras with unbalanced pixels or image sensors in artificial neural networks.

Finally, we also analyze the optoelectronic performance of our device. Figure 4a shows the IV characteristics of the device in the p–n configuration \((V_{g1} = V_{g2} = -4 \text{ V})\), upon illumination with white light with different power densities (ranging from 6.5 to 273 W m\(^{-2}\)). The corresponding generated electric power is shown in Figure 4b (we address the reader to Figure S6, Supporting Information, for the corresponding analysis with n–p configuration and Figure S7, Supporting Information, for the characterization without back-gate). The device yields a maximum power conversion efficiency (PCE) of \(\approx 1.6\%\), calculated as \(\text{PCE} = P_{el}/(P_{in} \cdot A_{el}/A_{spot})\), where \(P_{el}\) and \(P_{in}\) stand for the electrical power generated at the device and...
the incident optical power, respectively, and \( A_d \) and \( A_{\text{spot}} \) stand for the active device area (\( A_d = 20 \mu \text{m} \times 0.4 \mu \text{m} \)) and the spot area (\( A_{\text{spot}} = \pi \cdot r^2 \approx 2 \times 10^{-9} \text{ m}^2 \)), respectively. Furthermore, the maximum fill factor (FF) of our photodetector is \( \text{FF} = 33\% \), and it shows a high photovoltage responsivity (\( V_{OC}/P_{\text{eff}} \), with \( P_{\text{eff}} = P_{\text{in}} \cdot A_d/A_{\text{spot}} \)) of \( 1.7 \times 10^{10} \text{ V W}^{-1} \) for an illumination of \( P_{\text{eff}} = 49 \text{ pW} \), higher than that previously reported in comparable devices.\(^{[23]}\) The time response of the photodetector is studied by measuring \( I_{\text{SC}} \) upon pulsed excitation by triggering the incident light in a square-function shape (Figure 4c) both in p–n (from \( t = 0 \) to \( t \approx 6 \) s) and n–p (from \( t = 6 \) s to \( t \approx 13 \) s) configurations, yielding rise/fall times lower than 26 ms (limited by our measurement resolution) which, in principle, could be shorter.\(^{[10]}\)

3. Conclusions

We have demonstrated a new concept of programmable photodetector based on monolayer WSe\(_2\) in a split-gate self-driven photodetector configuration including charge-storing floating gates. Our photodetectors are capable of retaining configured and fully customizable responsivity values over time with remarkable performance and can be easily programed, erased, and rewritten by just varying the value of the control gates. These programmable photodetectors could be employed as building blocks in devices such as pixels arrays or image sensors, solving the problem of unbalanced responsivities in individual pixels, as well as in more complex devices such as neural networks.

4. Experimental Section

Sample Fabrication: The samples were fabricated on a 280 nm SiO\(_2\) substrate thermally grown on Si(p++). In the first step, Ti/Au (5 nm/30 nm) back-gate electrodes were fabricated by electron-beam lithography and subsequent electron-beam-induced evaporation with a separation of \( \approx 400 \text{ nm} \). In the second step, a 20 nm-thick Al\(_2\)O\(_3\) layer was grown over the structure by ALD at 200 °C. The floating gates were fabricated afterward by patterning a mask via e-beam lithography, covering the region over the back-gate electrodes, followed by e-beam-induced evaporation of a 2 nm-thick Au film which, in such low thickness, formed nanoclusters rather than a continuous film. Another Al\(_2\)O\(_3\) layer was again grown by ALD prior evaporation of 1.5 nm of Al as seeding layer (which was left 24 h in air to trigger oxidation), with a total thickness of 7 nm. The active material (monolayer WSe\(_2\)) was exfoliated from bulk material (h\(_\text{g}\) graphene) by means of a PDMS stamp (Gelfilm from Gelpak) that allowed optical identification in transmission-mode optical microscopy of the atomically-thin flake, which was then transferred (as described elsewhere\(^{[29]}\)) bridging the back-gate electrodes in the previously fabricated structure. As the final step, drain-source Ti/Au (5 nm/100 nm) electrodes were fabricated by e-beam lithography/evaporation to electrically contact the monolayer film.

Electronic and Optoelectronic Characterization: The optoelectronic measurements were performed in a Lakeshore Cryogenics tabletop probe station at room temperature and high vacuum (10\(^{-6} \text{ mbar}\)). The electronic measurements were carried with an Agilent 4155C semiconductor parameter analyzer. The light excitation was provided...
by a fiber-coupled white LED (Thorlabs MWWHF2) and guided with an optical fiber through the optics of the probe station (similar to as described in ref. [35]), yielding a spot on the sample of 50 μm. For the on/off measurements, the LED was externally triggered by a function generator. The voltage to the control gates for the program-erase measurements were provided by two Keithley 2614B source-meter units, connected to the probe station via a Keithley 3706A-S system switch.

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

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**Conflict of Interest**

The authors declare no conflict of interest.

**Keywords**

2D materials, floating gates, nonvolatilic memories, photodetectors, programmable photodetector, tungsten-diselenide

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