Design of Two-Stage Differential Amplifier with Stacked Transistors for Biomedical Applications

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Abstract— In this paper, CMOS based optimized two stage differential amplifier circuit for convenient biomedical signal conditioning system is presented. A low-power, low noise & high CMRR differential amplifier is designed for portable ECG signal conditioning using MOS based low pass filter with stacked transistors. The stack transistors with MOS which is connected at output terminal optimize the design for ECG signal conditioning and other biomedical device signal conditioning. The presented amplifier is designed with standard 45nm CMOS process technology at a 0.85 V supply voltage. The simulation results are derived using Cadence Analog Virtuoso Spectre Simulator. The simulation results show that the presented differential amplifier has a common-mode rejection ratio (CMRR) of 178dB at 100Hz, power supply rejection ratio (PSRR) of 68 dB and power dissipation of 1.5μW. The input referred (IR) noise is 3.83μV/√f and slew rate is 11volt/μsec. These obtained performance parameters is better and efficient compared to conventional differential amplifier. The noise performance is improved using proposed design compared to previous designed differential amplifier.

Keywords- ECG (Electrocardiogram), Signal conditioning, High CMRR, PSRR, Low-Power, Input noise
1. INTRODUCTION

Bio-medical signal monitoring and recording is an important part of medical diagnosis. Modern clinical practice requires that these signals have to be recorded routinely [1]. Generally, the data of results from various clinical tests are monitored on bulky recording devices for proper diagnosis [2]. The upcoming data from intermediate processing devices should be more precise and accurate. Therefore, it is required to have low-noise and ultra-low power, miniature ambulatory bio-medical acquisition devices. The main challenges for biomedical signal monitoring are of low amplitude and low frequency signal. It is also the emerging task to design the intermediate processing devices with low power dissipation. In order to overcome these challenges, a novel design is proposed of differential amplifier using MOS configuration [3]. The purpose of this design is to provide precise and accurate data of signal with low power consumption and good signal quality (that is low noise) [4]. This signal will be available at the output of the model of signal monitoring using differential amplifier. This represents the analog instrumentation amplifier in the form of extremely basic part in the entire bio-medical signal acquisition system [5]. This amplifier is the main signal processing block of instrumentation amplifier which characterizes the noise level, power dissipation and the common mode rejection ratio (CMRR) of the general system [6]. Generally, it is useful to remove the differential DC offset voltage which is formed by human electrode skin interface. The design procedure must consider a best trade-off amongst noise, power and speed [7]. Signals can be recorded with minimum noise and distortion with low power, so that the instrumentation amplifier using differential amplifier is used to have these characteristics [8, 9]. As we know that, the signals are having amplitude between 0.1mv to 50mv with low frequency range between 0.1-250Hz [10]. The flicker noise (1/f noise) of MOS transistors bounds the limit of minimum values of
detectable signal [11]. Metal-oxide semiconductor (MOS) transistors signify poor input DC offset performance [12]. In the presence of this drawback, the bio-medical application oriented differential amplifier is required to be designed, which should have Low power consumption, High common mode rejection ratio (CMRR), Low noise level, High speed (slew rate) and High input impedance [13, 14]. In order to transfer the biomedical signal without any information loss, the analog interface must have high input impedance [15]. A two-stage differential amplifier using stacked transistors has high CMRR to reject common mode interference. This is typically achieved by proposed amplifier [16, 17]. It should be designed to have low power dissipation for longer battery life and this has to be enhanced for continuous monitoring [18, 19]. This is usually achieved at the expense of noise. In this design approach, transistors are designed to operate in weak and moderate inversion for low power design [20, 21].

2. Literature Review

The general architecture of conventional differential amplifier contains conventional triple-operational amplifier, conventional current balance instrumentation amplifier, operational trans-impedance amplifier and double differential amplifier (DDA) [22, 23]. Difference of the resistances in conventional triple-operational amplifier degrades CMRR. Hence, the perfect matching should be implemented between resistances to improve CMRR [24]. Though, it is difficult to optimize the issues in standard CMOS process technology, hence triple-operational instrumental amplifier is not appropriate in CMOS technology. Opposite of this, similar value of resistances is not essential in CBIA which is one of advantages of CBIA. Maximum CMRR will be there when the transistors of current mirror are ideally same [25]. Even there are differences in process parameters, high CMRR can be obtained [26]. Instrumentation amplifier using operational amplifier has the advantage of very small chip area, so it is suitable for implantable
applications [27]. The CMRR of instrumentation amplifier optimized through operational amplifier is comparative not good. Result of performance parameters has explored 86 dB CMRR value in ideal condition. Differences in process parameters enhanced lower value of CMRR. Double differential amplifier can achieve high CMRR value without resistance matching [28]. It has still good CMRR during variations in process parameters [29]. If triple-operational Instrumentation Amplifier is taken, a high pass filter circuit (HPF) is necessary to add at the input of triple-operational instrumentation amplifier. It can minimize the dc offset. It is declared to perform capacitors and resistances matching in HPF to uphold CMRR [30]. In circuit representation of current balance instrumentation amplifier, a trans-conductance filter is implemented for purpose of coupling. Operational trans-conductance type instrumentation amplifier joins capacitors at the input terminal to separate DC signals. CMRR can also be changed by the dissimilar values of capacitors [31]. The analog front-end circuits are enlightened for wearable sensors. High CMRR, input impedance and low power dissipation parameters are focused to prove the optimized design [32, 33]. Double differential amplifier utilizes only single capacitor to form AC coupled combination, so it matching problem does not possible [34, 35]. Reducing of main power supply is the most effective approach to mitigate the power dissipation as it directly relates to $V_{DD}$. When $V_{DD}$ is scaled down, the circuit delay will not improve. It will not improve the performance of the circuit. At the same time, it is possible to maintain the performance by decreasing the threshold voltage ($V_{TH}$) but the leakage power increases exponentially. Therefore, $V_{DD}$ and $V_{TH}$ have to be optimized to achieve the required performance with low power. The feature size reduces shorter channel length. This is explored in sub threshold leakage region through a transistor when it is off. So, sub-threshold leakage power dissipation is considered as important part of the total power dissipation. At 45nm technologies,
leakage accounts for 4-8% of total power. The proposed circuit is arranged in such a manner that it optimized the delay performance as well as minimized the power dissipation. Finally, the proposed design is much better with improved CMRR, input referred noise & power dissipation. The parameters are optimized through involving stack transistors and MOS connected output terminal in proposed circuit.

3. **Proposed Two Stage Differential Amplifier**

The architecture of proposed amplifier has good performance in terms of high input impedance and high common mode rejection ratio (CMRR) to decrease noise. The function of capacitor-couple MOS decreases the effect of offset voltage with common mode rejection ratio. But, CMRR is reduced due to lower supply voltage. The application of the work is that it is useful in portable biomedical data acquisition system. The flicker noise will present at minimum frequency range and the maximum noise value will dominate the very low detectable signal in instrumentation amplifier. Flicker (1/f) noise is expressed in eq.1 where the K is constant of processing technology. From eq.1, the power spectral density (PSD) of flicker noise is inversely proportional to the transistor area, which is product of width (W) and length (L). On the other word, flicker noise affects much lesser on larger device. In addition, bias current is larger when circuits with maximum switching components are used at the same driving voltage. It is equal to the difference of gate to source voltage and threshold voltage [34]. Power spectral density (PSD) of flicker (1/f) noise is given by equation 1.

\[ \frac{v^2}{n(f)} = \frac{K}{c_{\text{oxide}}WL \times f} \]  

In the differential amplifier, Analog voltage signals of input differential terminal are converted into the output current signals with multiplication by Trans-conductance (Gm). The architecture representation of proposed differential amplifier circuit is demonstrated in Figure 1. The output
current signals are added by summing amplifier and converted into voltage signal at first stage [36, 37]. The next stage behaves as an amplifier with finite gain.

Figure 1 Architectural Distribution presentation of Proposed Differential Amplifier
The basic difference between conventional differential amplifier and the proposed circuit is that conventional differential amplifier compares two input voltages, whereas proposed compares four input voltage available at the input of double differential amplifier. The output is equivalent to the gain multiplied by the difference between the two differential inputs. As shown in Figure 2, the two Trans-conductance stages which have differential inputs: $V_1 = (V_{11} - V_{12})$ and $V_2 = (V_{21} - V_{22})$ and produce equal and opposite current outputs proportional to $(V_1 - V_2)$. The second stage which includes the amplifier is considered as the Trans impedance stage. It helps to translate the differential current into a single ended output voltage. On the other hand, this can be also realized by converting the differential current into differential voltages through resistors using a simple voltage amplifier such as an operation amplifier at the second stage [38].

From figure 2, we can write

$$V_O = A \times (V_{in1} - V_{in2})$$  \hspace{1cm} (2)

$$V_O = A \times [(V_{11} - V_{12}) - (V_{21} - V_{22})]$$  \hspace{1cm} (3)

Here, $A$ is the open loop gain. The value of $A$ (gain) is predicted through the behavior of output with respect to applied input voltages. The proposed amplifier has two differential voltages $V_1$ and $V_2$ which is equal to have the high gain. This is similar to the operational amplifier. Proposed circuit can also be used in closed loop system.

**4. Transistor Level Implementation of Proposed Amplifier**

The schematic representation of proposed circuit is introduced in Figure 2. Power spectral density of the flicker noise is inversely proportional to the length of the device. Transistors (PM$_1$ to PM$_4$) are chosen as a larger length PMOS device at the input stage of proposed amplifier circuit, which is helpful to decrease the flicker noise. Transistors (PM$_{ST}$ & NM$_{ST}$) are stack transistors. The stack transistors with combination of PM$_1$ to PM$_4$ improve the input noise and
reduce the power dissipation. Such innovative combination of MOS enhanced the performance of proposed differential amplifier [39].

Offset voltage can be decreased by choosing larger length PMOS input transistors in the design. The increment of the offset voltage has been avoided with the help of AC-coupling (coupling MOS) in proposed differential amplifier circuit. Output differential current of first stage passes from transistors NM7 and NM8, they convert into voltage. The combination of transistors NM9 and NM10 is used as common source amplifier. It has large value of gain to reduce the noise level. Transistors (NM7 to NM10) and the active load (PM11, PM12) are strongly biased such a
way that the noise will decrease. Transistors (NM13 to PM17) reform the Multi-stage differential circuit. This is important to achieve sufficient value of gain. Maximum gain can decrease the effect of non-linearity [40].

Frequency compensation filtering is applied using PMcc (Coupling MOS). This acts as a miller capacitance Cc. It may improve the phase margin to have a feedback circuit with high stability. The important variation between the proposed circuit and previously designed circuit is that the presented circuit uses two stages in order to improve the noise performance. The simple transistor level circuit is implemented to have a best tradeoff between power and noise of the proposed device. With the usage of two stage differential amplifier, power consumption is reduced and CMRR optimized. The performance of common mode rejection ratio is directly related to Trans-conductance (gm) of first or input stage transistor couples (PM1 to PM4) and impedance of current sink using transistor (PM5 to PM6). Good CMRR is obtained by minimum bias current in the real conduction. Due to mismatching in the proposed circuit, longer input transistor pair size is chosen to reduce the relative interference. Power supply rejection ratio is directly related to the impedance at output terminal of proposed design. The Power supply rejection ratio is improved with help of cascode combination of the transistors. The drawback is that this will reduce the output voltage swing in the circuit [41]. Transistors (PMST & NMST) overcome the situation of overflow of current. Finally, circuit configuration reduces the leakage current due to placing of NMOS in pull-down network [42]. In general, stacked transistor is placed to diminish the short circuit power dissipation and helps to increase the gain in the circuit [43].
5. Simulation Results

In the previous sections, we presented the operation of the proposed differential amplifier. In this part, the results are simulated and calculated for different characteristics of signals [44, 45]. This section represents the behavioral response of the proposed amplifier with characteristics like gain, CMRR, PSRR, input noise, slew rate and power dissipation. These characteristics will represent the performance of the proposed circuit. Proposed circuit is simulated at standard 45nm CMOS process technology with 0.850 V supply voltage. Figure 3 shows the output response of the proposed amplifier circuit with respect to input supply. The input difference voltage \( V_{id} \) is the difference value between the consecutive applied input voltages. The mathematical relation is shown in equation 3.

![Figure 3 Characteristics Graph between output voltage and input voltage](image)

From figure 4, it has been well explained that PSRR values of the proposed circuit which is similar to the conventional differential amplifier.
The PSRR value is represented at multiple values of frequencies. This representation graph also characterizes the PSRR value at which amplifier circuit performs better for particular frequency range. Power supply rejection ratio of proposed differential amplifier is 78 dB at 1.5 kHz frequency [46].

CMRR is one of the significant parameters of amplifying circuit. The technique of AC coupling can decrease the influence of offset voltage on common mode rejection ratio (CMRR) [47]. The common mode gain is calculated and is shown in figure 5. The CMRR of the proposed circuit is 165 dB at 100 Hz which is shown in figure 6. The PSRR is around 62dB at 100Hz which represent the efficient output response of the device [48].

Figure 4 PSRR representation of the proposed circuit

Figure 5 Common mode gain characteristic with respect to frequency of the proposed circuit
Figure 5 represents the analysis of common mode gain values of the proposed amplifier with respect to the various frequencies range. The common mode gain analysis is possible when same characteristics signals are applied at the input [46-48].

Figure 6 represents the common mode rejection ratio (CMRR) at various values of frequencies [49]. This is the ratio of differential mode gain to the common mode gain of the proposed amplifier [50]. Higher the value of CMRR represents the maximum value of differential voltage gain. On the other way, it also represents the minimum value of common mode gain [51].

![Common mode rejection ratio characteristic with respect to frequency of proposed circuit](image)

Figure 6 Common mode rejection ratio characteristic with respect to frequency of proposed circuit

Figure 7 shows the characteristic graph between inputs referred noise and frequency. At low frequencies, the flicker noise dominates [52, 53]. However, it has been analyzed that the noise voltage falls off rapidly with value of $3.832 \, \mu V / \text{Hz}^{1/2}$ [54].

![Characteristic of input noise with respect to frequency for proposed circuit](image)

Figure 7 Characteristic of input noise with respect to frequency for proposed circuit
Slew rate explores the sensitivity in terms of the switching of circuit which is the change of output voltage with respect to the time. **Slew rate of proposed amplifier is 11V/μs.** A slew rate characteristic of the proposed circuit is shown in figure 8.

![Slew rate characteristic](image)

Figure 8 Slew rate characteristics of proposed differential amplifier

| Parameters                  | Previously designed differential amplifier [11] | Previously designed Analog Front-end for wearable device [32] | Previously designed Analog Front-end for wearable device [33] | conventional differential amplifier | Proposed Differential Amplifier Circuit |
|-----------------------------|-----------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------|------------------------------------|----------------------------------------|
| Power Supply (volts)        | 1.0 V                                         | 0.8 V                                                       | 1.8 V                                                       | 0.85 V                             | 0.85 V                                 |
| Differential gain at 10 Hz  | 6.23 dB (20MHz)                               | 34 dB                                                       | ----                                                       | 56dB                               | 62 dB                                  |
| CMRR                        | ----                                          | 66 dB                                                       | 76 dB                                                       | 170 dB                             | 178 dB                                 |
| PSRR at 10 Hz               | ----                                          | 69 dB                                                       | ----                                                       | 70 dB                              | 78 dB                                  |
| Power dissipation           | 1.65 μW                                       | 0.3 μW                                                      | 0.9 μW                                                      | 120.68 μW                           | 1.5 μW                                 |
| Input referred noise        | ----                                          | ----                                                       | ----                                                       | 4.10 μV/√f                         | 3.83 μV/√f                            |
The comparison of various performance parameters between the proposed and conventional amplifier circuit is represented as Table 1. Table 2 shows the comparison of proposed amplifier with previous designed differential amplifier in terms of the standard parameters [55-58].

**TABLE 2 Comparison among Various Instrumentation Amplifiers**

| PARAMETER     | Differential Amplifier [11] | CBIA     | OTA       | TRIPLE OP-AMP | Proposed Double Stage Differential Amplifier |
|---------------|-----------------------------|----------|-----------|---------------|---------------------------------------------|
| Input impedance| Better                      | Better   | Not Good  | Better        | Best                                        |
| CMRR          | Satisfactory                | Satisfactory | Not Good  | Not Good      | Better                                      |
| PSRR          | Satisfactory                | Not Good  | Not Good  | Best          | Better                                      |
| Power         | Satisfactory                | Not Good  | Best      | Not Good      | Best                                        |

6. CONCLUSION

A two stage differential amplifier using low pass filter has been proposed for biomedical signal conditioning. For particular application of biomedical signals, two stages architecture is adopted with stacked transistors to diminish power dissipation and to sustain satisfactory gain. Proposed design of amplifier has larger transistor size to diminish flicker noise (1/f). The proposed circuit has better common mode rejection ratio, high differential gain and low power dissipation. The proposed two stage differential amplifier has admirable performance in terms of input impedance, CMRR and PSRR with comparison of previous designed optimized differential amplifier circuits.

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Authors' contributions
Prateek Jain has written the manuscript and prepared the design. Shambhu Dayal Sharma has done implementation of the design. Amit M Joshi has established the hypothesis.

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