Charge collection properties in an irradiated pixel sensor built in a thick-film HV-SOI process

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\textbf{Abstract:} Investigation of HV-CMOS sensors for use as a tracking detector in the ATLAS experiment at the upgraded LHC (HL-LHC) has recently been an active field of research. A potential candidate for a pixel detector built in Silicon-On-Insulator (SOI) technology has already been characterized in terms of radiation hardness to TID (Total Ionizing Dose) and charge collection after a moderate neutron irradiation. In this article we present results of an extensive irradiation hardness study with neutrons up to a fluence of $1 \times 10^{16}$ $\text{n}_{\text{eq}}$/cm$^2$. Charge collection in a passive pixelated structure was measured by Edge Transient Current Technique (E-TCT). The evolution of the effective space charge concentration was found to be compliant with the acceptor removal model, with the minimum of the space charge concentration being reached after $5 \times 10^{14}$ $\text{n}_{\text{eq}}$/cm$^2$. An investigation of the in-pixel uniformity of the detector response revealed parasitic charge collection by the epitaxial silicon layer characteristic for the SOI design. The results were backed by a numerical simulation of charge collection in an equivalent detector layout.

\textbf{Keywords:} Charge induction; Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc); Particle tracking detectors (Solid-state detectors); Radiation-hard detectors

\textbf{ArXiv ePrint:} 1701.06324

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1 Introduction

Intensive investigations of the possibility to produce particle tracking detectors for experiments at the upgraded LHC (HL-LHC) [1] using technology for commercial integrated CMOS circuits [2] are currently ongoing at several research institutions throughout the world. The potential of the CMOS technology offers production of fully monolithic particle detectors [3], which would enable a smaller pixel size, simpler assembly without costly interconnections between sensors and readout electronics, and consequently less material in the tracking volume [4–7]. Manufacturing detectors in commercial fabrication plants should also result in faster production, larger number of vendors and consequently lower cost.

Monolithic particle detectors have been used already for several years [8–10] but they were not suitable for use in the ATLAS experiment at the LHC because of their relatively slow speed and insufficient radiation hardness, since the dominant charge collection mechanism in these detectors is diffusion [11]. Recently new technologies were developed permitting usage of high voltages and full CMOS circuitry on the same chip. This opened the possibility of designing active pixel detectors with sufficient depleted thickness for fast collection of charge drifting in the electric field [12]. Several other developments followed [13–15] commonly referred to as depleted CMOS pixels [16]. Prototype test structures from various producers were tested recently and their performance after irradiation was investigated [17–21]. One very interesting technological option is Silicon On Insulator (SOI), where Buried OXide (BOX) isolates the bulk from the top layer where electronic circuitry exploiting full CMOS possibilities can be implemented. Since BOX is protecting the electronics, high voltage can be applied to form a significant depleted layer in the bulk for fast charge collection. A test structure investigated in this work is shown in figure 1.

Detector prototypes designed by the University of Bonn were produced in 180 nm SOI CMOS in the XFAB process [22]. XFAB uses the thick film SOI process where double well structures
Figure 1. (a) Microscope image of the array 2A on the XTB02 chip with indicated pads for connecting the single and peripheral pixels and the beam direction in E-TCT. (b) Cross section of a pixel in the structure 2A. Shown are the deep n-well collecting electrode with the corresponding dimensions, the buried oxide (BOX), the LOGIC section on the p-type epitaxial layer (white) with p-wells for the active circuitry, and the P-FIELD implant for inter-pixel insulation. XTB02 is read out by connecting the amplifier directly to the deep n-well (figure taken from [25]). The coordinate system is the one used in E-TCT measurements. Beam direction is along the \( z \)-axis.

shield FET transistors from the charge trapped in the BOX after irradiation. For this reason it is immune to the so called back gate effect [23] and can, unlike other SOI detectors, withstand high ionizing doses of over 700 Mrad [24]. Samples produced by XFB were also tested with radioactive sources [25] and in a test-beam experiment [26] with good results before irradiation. In this paper results of Edge Transient Current Technique (E-TCT) measurements with XFB test structures irradiated up to \( 1 \times 10^{16} \text{n}_{\text{eq}}/\text{cm}^2 \) are presented.

2 Sample and experimental technique

The chip investigated in this work is called XTB02. The substrate is p-type silicon with a resistivity of \( \approx 100 \Omega \cdot \text{cm} \). The chip thickness is 700 \( \mu \text{m} \). The XTB02 chip houses several test structures with different design parameters [14, 25]. The focus of this study is the test structure 2A, a \( 4 \times 4 \) pixel matrix with pixel dimension of \( 110 \times 100 \mu \text{m}^2 \) shown in figure 1a. Cross section of a pixel can be seen in figure 1b. The charge is collected by deep n-well electrodes with dimensions \( 40 \times 50 \mu \text{m}^2 \) placed under the BOX layer. Above the BOX there is a few \( \mu \text{m} \) thick epitaxial layer. In the p-well area above each deep n-well, called LOGIC, active CMOS circuitry can be placed. The epitaxial layer also contains an implant structure called P-FIELD around individual pixels. Its aim is to modify the electrical field below the BOX to break the conductive channel formed in the bulk due to BOX space charge formed after irradiation [24, 25]. XTB02 devices are dedicated for studying the properties of the silicon bulk, so there is no readout circuitry actually implemented in the LOGIC. The charge collection electrode is connected directly to the external amplifier as shown in figure 1b. The substrate is biased via the outermost guard ring, a p-type implant ring surrounding the test structures. LOGIC and P-FIELD can be connected via separate bond pads. The deep n-well of one of the four central pixels is routed to an independent bonding pad while the other pixels are
The schematics of the system for E-TCT measurements and the detector connection are presented in figure 2. The sample is placed with its edge in a focused beam of a pulsing infrared laser (λ = 1064 nm — absorption length in Si ≈ 1 mm, pulse width ≤ 300 ps, repetition rate 500 Hz, FWHM of beam profile in the focal point ≤ 10 μm). The light pulses generate electron-hole pairs along the beam path in the sample. The amount of generated charge is not calibrated, but the laser pulse power is kept constant to ≈ 5 % during individual measurements. Between different measurements the laser power was varied to some extent and different laser diodes were used, therefore the amount of injected charge cannot be directly compared between separate runs. The position of the sample in the laser beam is controlled by a set of positioning stages with sub-μm precision, which allow beam positioning in the xy-plane with a precision better than the beam width. Due to the large absorption length of the infrared light the deposited charge is roughly constant along the z-direction, meaning that the measurement has no resolution in this direction. The charge carriers generated by the laser pulse start to drift in electric field, inducing an electric current on the readout electrodes. This current is amplified by a 1 GHz bandwidth current amplifier and digitized by a 1 GHz bandwidth oscilloscope. Waveforms of 50 pulses are averaged by the scope and stored to the computer. All measurements are carried out at room temperature, since there were no occurrences of the thermal runaway of the sensor at any irradiation stage. A detailed description of the E-TCT method is available in [27]. Measurements reported here were made with an E-TCT system produced by Particulars [28].

The sample was irradiated with neutrons at Jožef Stefan Institute’s research reactor [29]. A single sample was available for the study and it was therefore irradiated in steps. The cumulative fluence after each step was 2 × 10^14, 5 × 10^14, 1 × 10^15, 2 × 10^15, 5 × 10^15 and 1 × 10^16 n_{eq}/cm^2 with a 10 % error margin. During irradiation with neutrons samples also receive an ionizing dose of about 1 kGy (in SiO₂) per each 1e14 n_{eq}/cm^2. The dose was estimated using RadFETs, dedicated...
pMOS transistors, where TID is estimated from the change of threshold voltage [30]. After each irradiation step the sample was annealed (80 min at 60° C) before E-TCT measurements were made. The sample was kept in the freezer at −17° C and it was warmed to room temperature only for few hours during measurements.

3 Evolution of sensitive depth with irradiation

The collected charge in E-TCT is defined as the integral of the induced current pulse over 25 ns after the beginning of the pulse. The collected charge was measured with a single pixel connected to readout. Laser was directed to different depths $y$ (see figure 2 for definition of the coordinate system), while the horizontal beam position $x$ was fixed to the centre of a pixel. The measured charge as a function of the beam position is called charge collection profile. Charge collection profiles measured before irradiation and after each fluence step are shown in figure 3. Measurements were taken at the highest bias voltage of 300 V. The curves were normalized to the same maximal value. The transition at the rising edge of the charge collection profile (charge close to the chip surface, at $y \approx 20 \mu m$) corresponds to the laser beam gradually entering the sample. The transition takes place over $\approx 10 \mu m$ which corresponds to the laser beam diameter. Once the transition at the chip surface is finished, the beam is for a while fully contained within the depletion zone. This results in a plateau in the charge collection profile. The slope of the top of the profile seen in measurements after irradiation may be related to charge trapping as the electric field and thus the carrier velocity is falling with distance from the surface. The transition on the falling edge of the charge collection profile is slower than on the surface side — the collected charge typically reduces from 90 % to 10 % of the maximum value over a depth of approximately 50 $\mu m$, — which is due to the form of the depletion zone deviating from the abrupt junction approximation. Figure 3 shows that the width of the charge collection profile increases with irradiation, reaching a maximum at a fluence of $5 \times 10^{14}$ n$_{eq}$/cm$^2$. The width reduces at higher fluences, however it is still significant even at the highest fluence of $1 \times 10^{16}$ n$_{eq}$/cm$^2$. This behaviour is consistent with radiation induced removal of initial acceptors [21]. Upon first irradiation steps the effective space charge concentration is reduced as more initial acceptors are removed than new are created by irradiation. After the removal process is finished the negative space charge concentration increases with increasing fluence.

The width of the sensitive region was quantified by evaluating the full width at half maximum of the charge collection profiles. Charge collection width (i.e. profile width) as a function of bias voltage is shown in figure 4 for all fluences. The width of the depletion region in a sensor with planar electrode geometry is calculated in the model of constant space charge as $W_{depl} = \sqrt{\frac{2\epsilon}{q_0 N_{eff}} V}$, with $\epsilon$ the electric permittivity of the bulk, $q_0$ the elementary charge, $N_{eff}$ the effective acceptor concentration in the space charge region and $V$ the applied bias voltage. With the rest of the quantities known, one can use this dependence to extract the values of $N_{eff}$ for different fluences. For the measurement before irradiation a fit could be made, yielding the value of $N_{eff} \approx 1.3 \times 10^{14}$ cm$^{-3}$, consistent with the initial resistivity of the substrate. After irradiation the width of the sensitive region grows faster than the square root function of voltage and the fit is therefore not possible. In figure 4 an unusual behaviour at $1 \times 10^{15}$ n$_{eq}$/cm$^2$ and higher fluences can be observed at low bias voltages, where one can notice very low charge collection width for the initial bias voltages followed by a relatively fast increase, which looks like a certain threshold voltage has to be reached before charge collection starts. The mechanism behind this behaviour is not understood.
Figure 3. Normalized charge collection profiles along the pixel centre at 300 V bias for different neutron fluences. Arrows indicate the sequence of irradiation steps.

Figure 4. Width of charge collection profiles vs. bias voltage for different neutron fluences. Arrows indicate the sequence of irradiation steps.
4 Effective acceptor removal parameters

Irradiation of silicon with neutrons introduces defects into its crystal structure. Interaction of initial dopants with these defects may turn them electrically neutral so that they do not contribute to the effective space charge any more [31, 32]. The radiation induced defects also form negatively charged localized energy levels which contribute to the effective acceptor concentration in the depleted layer. If the number of neutralized initial acceptors is larger than the number of newly created acceptors the effective space charge decreases, therefore increasing depleted depth. The increase of depleted depth with irradiation was clearly observed as shown in figure 3 and the behaviour can be explained by the removal of initial acceptors. This has a beneficial impact on the signal after irradiation. As mentioned in the previous section the dependence of depleted depth on bias voltage does not follow the simple square root behavior after irradiation. However, to get some comparison of acceptor removal behavior with other measurements [21, 33, 34] the following procedure was made. \( N_{\text{eff}} \) was calculated from the width of the charge collection profiles by evaluating the formula

\[
W_{\text{depl}} = \sqrt{\frac{2e}{q_0 N_{\text{eff}}}} V
\]

at the bias voltage of 300 V. A systematic uncertainty on the value of \( N_{\text{eff}} \) was estimated from the spread of the values when taking the width of charge collection profiles at (50 ± 10)% of the maximum. The measured values of \( N_{\text{eff}} \) at different fluences calculated at a bias voltage of 300 V are shown in figure 5. The evolution of \( N_{\text{eff}} \) as a function of fluence is given by [17, 21, 32]:

\[
N_{\text{eff}} = N_{\text{eff},0} - N_A (1 - \exp(-c \cdot \Phi_{\text{eq}})) + g_C \Phi_{\text{eq}},
\]  

(4.1)

where \( N_{\text{eff},0} \) denotes the initial effective acceptor concentration of the substrate, \( N_A \) the concentration of the effectively removed acceptors, \( c \) the acceptor removal constant, \( \Phi_{\text{eq}} \) the 1 MeV neutron equivalent fluence and \( g_C \) the generation rate of stable deep acceptors [35]. The measured data were fit with function (4.1) with \( N_{\text{eff},0}, N_A, c \) and \( g_C \) as free parameters. Results of the fit are shown in figure 5. The ratio \( N_A/N_{\text{eff},0} = 1 \) indicates a complete initial acceptor removal. The value of the parameter \( c = 1.1 \times 10^{-14} \text{ cm}^2 \) is consistent with that in [34] measured on a substrate of the same initial resistivity. At the same time it is by a factor of 2–3 larger than for substrates of initial resistivities of 10 and 20 \( \Omega \cdot \text{cm} \) measured in [21]. This is consistent with the observation that the acceptor removal constant is smaller in silicon with a lower initial resistivity [36]. The value of \( c \) is also reflected in the fluence at which the maximal charge collection width is reached. In the XTB02 sample the maximum is reached at \( \sim 5 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2 \) whereas for samples in [21] it occurs at \( \sim 2 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2 \). The value of the parameter \( g_C = 0.036 \text{ cm}^{-1} \) is larger than the value 0.02 cm\(^{-1}\) usually observed for neutron irradiated samples [21]. But this is not surprising since we know that the depleted depth does not follow the \( \sqrt{V} \) behaviour, pointing to an inconsistency with the uniform space charge concentration and abrupt junction approximation. By evaluating \( N_{\text{eff}} \) from measurements at a bias voltage of 210 V we for example obtain the value of \( g_C = 0.08 \text{ cm}^{-1} \), whereas at 150 V the value is \( g_C = 0.2 \text{ cm}^{-1} \). However, the other three fit parameters are stable within 10% of the value at 300 V, because they are related to the maximum of depleted width, which is at \( \sim 5 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2 \) at all bias voltages. This rises the confidence that the value of the acceptor removal constant extracted from the fit in figure 5 is a good estimate for this substrate material.
Figure 5. Evolution of \(N_{\text{eff}}\) of the substrate with fluence. The fit of the data with the function (4.1) and the extracted fit parameters are also shown.

5 Uniformity of charge collection efficiency

An important requirement for a pixel detector is the response uniformity within a pixel. The uniformity can be studied with a two dimensional E-TCT scan, where the position of the laser beam is varied along the sample depth (coordinate \(y\)) as well as along the edge of the sample (coordinate \(x\), see figure 2). Figure 6 shows collected charge as a function of coordinates \(x\) and \(y\) after a fluence of \(5 \times 10^{14} \text{ neq/cm}^2\). In the measurement all sixteen pixels of the test structure are connected together and read out simultaneously. Each region with a high collected charge corresponds to a column of four pixels along the \(z\)-axis, which cannot be distinguished from each other in an E-TCT measurement. Distinct regions with no collected charge can be seen between the columns. Size and spacing of these efficiency gaps roughly coincides with the spacing between deep n-wells of neighbouring pixels. As can be seen in figure 1b, the n-well does not extend over the entire area of the pixel.

Figures 6a and 6b show the induced current pulses from an efficient and an inefficient region at \(y = 50 \mu\text{m}\). While the former is a unipolar pulse with a non-zero integral (with superimposed oscillation due to non-matching impedances of the cable and the amplifier), the latter is bipolar with a vanishing integral. A similar magnitude of both pulses confirms a uniform strength of electric field at a given sample depth. According to the Shockley-Ramo theorem of signal formation, a bipolar pulse with zero integral is observed when the drift path of charge carriers does not end on a readout electrode [37, 38]. The pulse 6b therefore indicates a presence of a parasitic charge collecting electrode which is not connected to readout. The identity of this electrode can be deduced from figure 1b. It can be seen that there are two biased structures present on the top of the pixel — the deep n-well, which is read out, and LOGIC, which is biased separately to the potential of the deep n-well but does not have a low impedance connection to the readout. Although LOGIC is positioned above the insulating BOX layer, it still influences the electric field in the bulk. If this effect is strong the field lines will be roughly perpendicular to the chip surface. When charge is not injected directly underneath the collecting n-wells, its drift path will end on the BOX rather
Two dimensional charge collection profile in a detector irradiated to $5 \times 10^{14} \text{n}_{\text{eq}}/\text{cm}^2$ at $V_{\text{bias}} = 200 \text{ V}$ with induced pulses in regions with high and low charge collection efficiency respectively.

than on the deep n-well, resulting in a low collected charge (figure 9). LOGIC therefore acts as an AC coupled parasitic electrode. This hypothesis was confirmed by switching the deep n-well and LOGIC connections, so that LOGIC was read out. This yielded a complementary picture — low efficiency for charge injection underneath the deep n-wells and high efficiency for injection underneath LOGIC.

The electrons drifting towards LOGIC eventually stop on the non-conductive BOX layer after $\approx 10 \text{ ns}$. Since charge cannot accumulate on BOX indefinitely, it has to be removed laterally towards the deep n-wells, which are the only conductive connection through the BOX. The lateral charge flow should result in an additional measurable induced current. To investigate this assumption, the time scale of the E-TCT measurements was prolonged from 25 ns to 1 $\mu$s. Standard detector biasing scheme was used and the deep n-well was read out. The long time scale pulses from an efficient and an inefficient region of the test structure are compared in figure 7a. After the initial charge collection by drift in the first 25 ns is finished, a current pulse with a small amplitude ($< 1 \%$ amplitude from drift) persists for 1 $\mu$s. Note that on the scale used in figure 7 the initial part of the pulse is truncated as it extends much below $-1000 \mu\text{A}$. The amplitude of this trailing pulse is higher in an inefficient region than in an efficient region. This current appears due to the charge collected on the BOX slowly discharging to the n-wells. Even in an efficient region some sections are not covered by n-wells due to the segmentation along $z$-direction, hence the current is always present.
The exact mechanism of the current flow on the BOX surface was not addressed in this work. The cumulative time integral of both pulses is shown in figure 7b. Two characteristic regimes can be observed. For a short integration time of 25 ns about \( \frac{3}{4} \) of the maximum charge is collected from an efficient region, whereas the charge collected from an inefficient region is zero, as already observed in figure 6. However, for an integration time of several hundred ns the small difference in the amplitude of the pulse tail becomes important. At 600–800 ns integration time the collected charge from both regions is about the same, while for even longer integration times the collected charge in an inefficient region is even slightly higher than in an efficient region. The two dimensional charge collection profiles corresponding to 25 ns and 800 ns charge integration times are shown in figures 7c and 7d. While efficiency gaps are present for the 25 ns integration time, the collected charge is relatively uniform for the 800 ns integration. These measurements are in agreement with the hypothesis of a parasitic charge collection via the AC coupled LOGIC electrode. The part of the charge which ends its drift on the BOX interface is effectively lost for 25 ns charge collection time. The charge from the BOX interface is transported to the collecting electrode by a much slower process, which takes about 1 \( \mu \)s to complete as seen in figure 7.

Figure 7. (a) Induced electrical pulses from different efficiency regions on a time scale of 1 \( \mu \)s in a detector irradiated to \( 5 \times 10^{15} \) n\(_{eq}\)/cm\(^2\). The drift contribution in the first 25 ns is truncated in the image, since it exceeds 1000 \( \mu \)A. The persisting pulse comes from the lateral current flow on the BOX interface. (b) Dependence of the pulse integral (collected charge) from integration time. (c) Charge collection profile with 25 ns integration time. (d) Charge collection profile with 800 ns integration time. The z-axis scales are the same as in figure 6. The difference in measured charge comes from different laser power. All measurements were made at 200 V bias voltage.
Before irradiation the efficiency gaps were not observed. This means that the properties of the BOX and the BOX-Si interface layer before irradiation enabled fast transport of charge carriers to the deep n-wells. Results of measurements shown in figure 7 indicate that after irradiation charge carriers are temporarily trapped on the BOX-Si interface leading to slow charge collection. This may be the consequence of modified electric field due to charge trapped in the BOX layer and/or of the radiation induced defects on the BOX-Si interface slowing the charge transport towards the deep n-wells. Deeper understanding of this process is beyond of the scope of this work.

A further test of charge collection uniformity was carried out by biasing LOGIC to different bias voltages. In each measurement the deep n-well was always biased to +200 V and the outer guard ring was grounded. LOGIC was then biased to either +200 V (standard configuration), +150 V or left floating. Two-dimensional charge collection profiles for different bias configurations were then recorded and are shown in figure 8. All tests were done with a sample irradiated to a fluence of $2 \times 10^{14} \text{neq/cm}^2$.

The charge collection efficiency between the n-wells improves with respect to the standard configuration when LOGIC is biased to +150 V or left floating. In these cases the electric field lines bend more towards the deep n-wells and more electrons end their drift on the readout electrode, hence increasing the response uniformity. The efficiency gaps become less distinctive at higher neutron fluences. The observed changes of the depleted depth for different biasing configurations

![Charge collection profiles for different biasing configurations](image)

**Figure 8.** Charge collection profiles in a $2 \times 10^{14} \text{neq/cm}^2$ irradiated sample for different LOGIC biasing configurations. The laser power was different between the measurements, hence the amount of collected charge differs.
Figure 9. SOI device used in detector simulation. The detector details are described in the text. Shown are also drift paths of electrons (blue) and holes (red) after a point-like charge injection. Electron drift ends when they reach the BOX layer. Diffusion of holes in the undepleted part of the sensor can be observed in the lower part of the figure.

In figure 8 are not well understood, but may be related to screening of the electric field caused by positive charge accumulated in the BOX after irradiation. A similar study was also carried out for the P-FIELD implant, however no large effects were observed in this case.

6 Simulation of charge collection with KDetSim

Measured phenomena in the charge collection were qualitatively verified with the KDetSim simulation tool - a ROOT based library for simulation of charge transport in static detectors [39]. For a given electrode configuration, space charge distribution and boundary conditions, KDetSim calculates the electric (weighting) field in the detector by solving the Poisson (Laplace) equation for the corresponding potential. Changes of the electric field due to injected charge carriers are neglected. Injected charge is divided into buckets, which propagate through the detector as point charges. Moving buckets induce an electric current on the electrodes in accordance with the Shockley-Ramo theorem [37, 38]. Signals for electrons and holes are calculated separately and summed in the end. The induced charge is defined as an integral of the induced current from 0 to 25 ns.

In the simulation of the XTB02 chip several simplifications compared to the real device are assumed in order to reduce the complexity of the problem while still maintaining the main characteristics of the detector. The simulated device can be seen in figure 9. Detector calculation is done in two dimensions with three deep n-well implants (50 µm width, 100 µm pitch) acting as readout electrodes. Above the deep n-wells a 1 µm thick insulation layer and a 3 µm thick silicon layer of BOX and LOGIC respectively are added. Charge carrier mobility in the BOX is assumed to be zero. A conductive back plane at a depth of 100 µm serves as a back bias contact. Although the real device is 700 µm thick and does not have a processed back plane this should not cause a significant difference, since the undepleted bulk is sufficiently conductive to be at the same electrical potential everywhere.

The simulation was performed with bias voltage between the grounded n-wells and the back plane set to −130 V, such that the sensor was not fully depleted. Constant space charge concentration
was assumed in the depleted region. Three electrodes with fixed electrical potentials were defined: the joined n-wells, the LOGIC and the back plane. On the detector edges mirror boundary conditions with electric field lines parallel to the edges were set. Charge trapping on radiation induced defects was not taken into account, since it only becomes relevant on a time scale greater than the charge collection time in this simulation. A two-dimensional charge collection scan was simulated for different bias voltages applied to the LOGIC electrode: 0 V (potential of the n-wells), \(-50\) V and LOGIC left floating. The step size in each direction was 5 \(\mu\)m. For each step a point-like injection of 100 buckets of charge was made. The resulting induced pulses were integrated over 25 ns. The simulated charge collection profiles are shown in figure 10. The results are qualitatively comparable to the E-TCT measurements. When LOGIC is biased to the same potential as the n-wells, efficiency gaps between the electrodes occur (figure 10a). In configurations where electron drift towards the n-wells is more favored, the efficiency gaps between the electrodes are reduced (LOGIC at \(-50\) V, figure 10b) or disappear completely (LOGIC floating, figure 10c). Note that in this simulation the drift of charge is stopped when it reaches the Si-BOX interface. The properties of the interface enabling the transport of charge to the n-wells are not considered so the efficiency gaps are seen also in what would represent a model of an unirradiated detector.

Figure 10. Simulated charge collection profiles for different biasing configurations of LOGIC. The results of the simulation are in a qualitative agreement with the measurements shown in figure 8.
7 Conclusions

The paper reports about an investigation of charge collection properties before and after neutron irradiation in a CMOS pixel detector prototype produced on a $100 \, \Omega \cdot \text{cm}$ p-type substrate in SOI technology by XFAB. The depleted depth was estimated by E-TCT. At 300 V bias voltage the thickness of charge collection layer initially increased with irradiation from 50 $\mu$m before irradiation to 160 $\mu$m after a neutron fluence of $5 \times 10^{14}$ $n_{eq}$/cm$^2$. At higher fluences the depleted depth falls but even at highest fluence of $1 \times 10^{16}$ $n_{eq}$/cm$^2$ it remains larger than 30 $\mu$m. These changes are a consequence of radiation induced removal of initial dopants and introduction of stable deep acceptors. The parameters describing the evolution of $N_{\text{eff}}$ with fluence were extracted from the fit of measured data. The value of acceptor removal constant was larger than the constant estimated with similar method on HV-CMOS devices made on lower resistivity substrate [21]. This is in agreement with the hypothesis that the removal constant is larger in material with a higher initial resistivity. A study of charge collection uniformity within the pixels revealed efficiency gaps on pixel edges. E-TCT tests with different detector biasing configurations, as well as computer simulations, showed that they appear due to a parasitic AC coupled charge collection by the area above the BOX layer not covered with the deep n-well. It was shown that with an appropriate biasing scheme and/or larger n-well fill factor this effect might be greatly reduced.

Acknowledgments

The authors would like to thank the crew at the TRIGA reactor in Ljubljana for help with irradiations of detectors. The authors acknowledge the financial support from the Slovenian Research Agency (research core funding No. P1-0135 and project ID PR-06802).

References

[1] ATLAS, collaboration, Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment, CERN-LHCC-2012-022.

[2] B. Dierickx et al., Near 100% fill factor CMOS active pixel, Proc. SPIE 3410 (1998) 68.

[3] J. Kemmer et al., Experimental Confirmation of a New Semiconductor Detector Principle, Nucl. Instrum. Meth. A 288 (1990) 92.

[4] G. Aad et al., ATLAS pixel detector electronics and sensors, 2008 JINST 3 P07007.

[5] H.C. Kastli et al., CMS barrel pixel detector overview, Nucl. Instrum. Meth. A 582 (2007) 724 [physics/0702182].

[6] ALICE collaboration, The ALICE experiment at the CERN LHC, 2008 JINST 3 S08002.

[7] L. Rossi, P. Fischer, T. Rohe and N. Wermes, Pixel Detectors: From Fundamentals to Applications, Springer, Heidelberg, Germany (2006).

[8] R. Turchetta et al., A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology, Nucl. Instrum. Meth. A 458 (2001) 677.

[9] I. Valin et al., A reticle size CMOS pixel sensor dedicated to the STAR HFT, 2012 JINST 7 C01102.

[10] P. Yang et al., MAPS development for the ALICE ITS upgrade, 2015 JINST 10 C03030.
[11] M. Deveaux, G. Claus, G. Deptuch, W. Dulinski, Yu. Gornushkin and M. Winter, Neutron radiation hardness of monolithic active pixel sensors for charged particle tracking, *Nucl. Instrum. Meth. A* **512** (2003) 71.

[12] I. Perić, A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology, *Nucl. Instrum. Meth. A* **528** (2007) 876.

[13] M. Havránek et al., DMAPS: a fully depleted monolithic active pixel sensor — analog performance characterization, 2015 *JINST* **10** P02013 [arXiv:1407.0641].

[14] T. Hemperek, T. Kishishita, H. Krüger and N. Wermes, A Monolithic Active Pixel Sensor for ionizing radiation using a 180 nm HV-SOI process, *Nucl. Instrum. Meth. A* **796** (2015) 8 [arXiv:1412.3973].

[15] T. Kishishita, T. Hemperek, H. Krüger and N. Wermes, Depleted Monolithic Active Pixel Sensors (DMAPS) implemented in LF-150 nm CMOS technology, 2015 *JINST* **10** C03047.

[16] N. Wermes, From Hybrid to CMOS Pixels . . . a possibility for LHC’s pixel future?, 2015 *JINST* **10** C12023 [arXiv:1509.09052].

[17] A. Affolder et al., Charge collection studies in irradiated HV-CMOS particle detectors, 2016 *JINST* **11** P04007.

[18] J. Liu et al., Performance of radiation-hard HV/HR CMOS sensors for the ATLAS inner detector upgrades, 2016 *JINST* **11** C03044.

[19] ATLAS CMOS Pixel collaboration, Active Pixel Sensors in AMS H18/H35 HV-CMOS Technology for the ATLAS HL-LHC Upgrade, *Nucl. Instrum. Meth. A* **831** (2016) 88 [arXiv:1602.02909].

[20] V. Fadeyev et al., Investigation of HV/HR-CMOS technology for the ATLAS Phase-II Strip Tracker Upgrade, *Nucl. Instrum. Meth. A* **831** (2016) 189.

[21] A. Affolder et al., Charge collection studies in irradiated HV-CMOS particle detectors, 2016 *JINST* **11** P04007.

[22] A. Holke et al., A 200 V partial SOI 0.18 µm CMOS technology, in proceedings of The 22th International Symposium on Power Semiconductor Devices & ICS (ISPSD), Japan (2010), pg. 257–260.

[23] R. Ichimiya et al., Reduction Techniques of the Back Gate Effect in the SOI Pixel Detector, CERN-2009-006.68.

[24] S. Fernandez-Perez et al., Radiation hardness of a 180 nm SOI monolithic active pixel sensor, *Nucl. Instrum. Meth. A* **796** (2015) 13.

[25] S. Fernandez-Perez et al., Charge collection properties of a depleted monolithic active pixel sensor using a HV-SOI process, 2016 *JINST* **11** C01063.

[26] S. Fernandez-Perez, M. Backhaus, C. Padilla, H. Pernegger and D. Schaefer, Test beam results of a depleted monolithic active pixel sensor using an HV-SOI process for the LH-LHC upgrade, 2016 *JINST* **11** C02083.

[27] G. Kramberger et al., Investigation of irradiated silicon detectors by Edge-TCT, *IEEE Trans. Nucl. Sci.*, **57** (2010) 2294.

[28] Particulars webpage, http://www.particulars.si/.

[29] L. Snoj, G. Žerovnik and A. Trkov, Computational analysis of irradiation facilities at the JSI TRIGA reactor, *Appl. Radiat. Isot.* **70** (2012) 483.
[30] I. Mandić et al., Bulk damage in DMILL npn bipolar transistors caused by thermal neutrons versus protons and fast neutrons, *IEEE Trans. Nucl. Sci.* **51** (2004) 1752.

[31] R. Wunstorf et al., Investigations of donor and acceptor removal and long term annealing in silicon with different boron/phosphorus ratios, *Nucl. Instrum. Meth.* **A 377** (1996) 228.

[32] ROSE collaboration, G. Lindström et al., Radiation hard silicon detectors developments by the RD48 (ROSE) Collaboration, *Nucl. Instrum. Meth.* **A 466** (2001) 308.

[33] I. Mandić et al., Neutron irradiation test of depleted CMOS pixel detector prototypes, *2017 JINST* **12** P02021 [arXiv:1701.05033].

[34] E. Cavallaro et al., Studies of irradiated AMS H35 CMOS detectors for the ATLAS tracker upgrade, *2017 JINST* **12** C01074 [arXiv:1611.04970].

[35] V. Cindro et al., Radiation damage in p-type silicon irradiated with neutrons and protons, *Nucl. Instrum. Meth.* **A 599** (2009) 60.

[36] G. Kramberger et al., Radiation effects in Low Gain Avalanche Detectors after hadron irradiations, *2015 JINST* **10** P07006.

[37] W. Shockley, Currents to Conductors Induced by a Moving Point Charge, *J. Appl. Phys.* **9** (1938) 635.

[38] S. Ramo, Currents Induced by Electron Motion, *Proc. IRE* **27** (1939) 584.

[39] KDetSim webpage, http://kdetsim.org/.