PoisSolver: a Tool for Modelling Silicon Dangling Bond Clocking Networks

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Abstract—Advancements in the fabrication of silicon dangling bonds (SiDBs) reveal a potential platform for clocked field coupled nanocomputing structures. This work introduces PoisSolver, a finite element simulator for investigating clocked SiDB systems in the SiQAD design tool. Three clocking schemes borrowed from prior work on quantum-dot cellular automata are examined as potential building blocks for a general clocking framework for SiDB circuits. These clocking schemes are implemented in SiQAD, and power estimates are performed with geometrically agnostic methods to characterise each clocking scheme. Clocking schemes using a 14 nm technology node are found to dissipate 10-100 μW cm\(^{-2}\) at 1 GHz and 1-10 W cm\(^{-2}\) at 1 THz.

I. INTRODUCTION

Recent advancements in silicon dangling bond (SiDB) fabrication [1]–[3] presents a platform for beyond-CMOS binary logic. A binary OR gate with dimensions less than 10 × 10 nm\(^2\) [4] has been experimentally demonstrated on the SiDB platform, with similar simulation results shown for other common logic gates [5]. More complex SiDB circuitry requires data to be synchronized and directed through a large network of SiDBs. To achieve this, the concept of clocking with suspended electrodes is borrowed from quantum-dot cellular automata (QCA) [6], [7]. This work presents PoisSolver, a finite element simulator plugin to the SiQAD SiDB design tool [5] for investigating clocked SiDB systems.

The paper is structured as follows. Section II provides an overview of the SiDB platform and prospective clocking techniques. Section III introduces three selected clocking schemes serving as case studies. Section IV demonstrates PoisSolver’s functionality in obtaining surface potential solutions for a clocked SiDB system. Section V models the clocking network as an RC circuit, and describes geometry agnostic methods for estimating resistance and capacitance. Section VI analyses the power dissipation of the clocking electrode network. Lastly, Section VII compares clocking power with other dissipative sources in the system.

II. BACKGROUND

SiDBs are a novel approach to implement devices beyond the limits of CMOS fabrication, presenting potential advantages in device density, power, and speed. SiDBs are created by selectively removing hydrogen atoms from hydrogen-passivated silicon surface dimers [2], and exhibit discrete charge states similar to quantum dots [4], [8]. The platform relies on specific arrangements of SiDBs, encoding information positionally through charge state configurations [1]. OR gate experiments [4] demonstrate ground state tracking binary logic on the SiDB platform, with information manipulated through the placement and charge state of nearby SiDBs. SiDB devices such as the OR gate can be switched without charge transfer, requiring only a reconfiguration of electrons and potentially lowering computational energy cost. Simulation results of a full suite of binary logic gates are shown in [5], where the SiQAD design tool is used for the design and simulation of each gate.

The behaviour of SiDB gates relies on establishing specific electron populations and making desirable electron configurations energetically favorable under different input conditions. SiDB placement and occupation is tweaked until ground state configurations mimic the truth table of a logical operation. While past experiments demonstrate the use of scanning probes [9] and surface contacts [10] to control charge states, [5] proposes that the transition levels (and thus the occupations) of the SiDBs can also be controlled by the application of an external field. This work proposes the adaptation of suspended electrode clocking schemes found in QCA [11]–[13] for use in SiDB systems to implement control fields.

Clocked SiDB devices dissipate power through resistive losses in nonideal clocking networks in addition to any losses incurred within the SiDB system. Quantitative analysis of clocking networks in the literature is limited to two phase networks using a simple series resistive capacitive model [14], neglecting parasitic self-capacitances and not addressing the four phase clocking network that many designs rely on. To investigate clocking schemes in the context of SiDB systems, PoisSolver is designed for modelling electrode-silicon surface interactions specifically with the SiQAD design tool in mind. PoisSolver is preferred over commercial tools such as COMSOL Multiphysics and ANSYS due to its integration with other physical simulators in the SiQAD environment. We show the combined use of PoisSolver and SiQAD to extend power estimates of clocking networks using a four phase circuit model.

III. CLOCK SCHEMES UNDER CONSIDERATION

Clocking methods in QCA designs range from arbitrary and physically unrealistic [15] to regular and fabricable [12]–[14]. This work will focus on the latter, targeting tileable clocking schemes for universal logic implementation. Tileable schemes are selected for two major purposes: they are infinitely scalable for any SiDB netlist, and they predefine design constraints based on physically realisable clocking networks.
Three schemes are selected from literature: columnar [11], wave [12], and USE [13]. SiQAD implementations of these schemes are shown in Fig. 1 along with numeric labels and arrows depicting relative phase and information flow respectively. A 14 nm technology node [16] was selected, yielding design parameters shown in Table I. Following these geometric constraints, a single tile is created for each clocking scheme as compactly as possible.

### IV. PoisSolveR

With the electrode network defined and routed in the SiQAD design environment, we consider the combined system of electrodes and SiDBs. A model of the clocked SiDB system is shown in Fig. 2 consisting of a silicon substrate, SiDBs on a hydrogen-passivated surface, and the network of electrodes suspended in dielectric above the SiDBs. SiDB clocking is achieved by modulating electrode voltages to induce desired surface potential patterns on the silicon surface to bias the flow of information.

#### A. Finite element model

To quantify these surface potential patterns in this 3D system we utilize a finite element model. PoisSolver is developed in Python, and takes advantage of the FEniCS [17] [18] finite element package. Its primary function is to take user-defined electrode layouts in SiQAD and solve Poisson’s Equation. The electrode network is meshed using Gmsh [19] via the Open CASCADE geometry kernel. Formally, PoisSolver solves the generalized Poisson’s Equation:

\[-\nabla \cdot (\varepsilon \nabla u) = \rho(x) \quad x \in \Omega\]

with the dielectric constant \(\varepsilon\), the three dimensional potential \(u\), the spatial charge density \(\rho\), the position \(x\), and the simulation domain \(\Omega\). By altering \(\rho\), Eq. [1] can be adapted to account for different physical models. PoisSolver supports four different definitions of \(\rho\):

- **LE**: \(\rho = 0\)  
  \[\text{(2a)}\]
- **PE**: \(\rho = q(N_D - N_A + p - n)\)  
  \[\text{(2b)}\]
- **PBE**: \(\rho = q(N_D - N_A + n_i e^{\frac{\varepsilon u}{kT}} - n_i e^{\frac{-\varepsilon u}{kT}})\)  
  \[\text{(2c)}\]
- **LPBE**: \(\rho = q(N_D + 2n_i^2 e^{\frac{\varepsilon u}{kT}})\)  
  \[\text{(2d)}\]

Laplace’s Equation (LE) is used in the case of an intrinsic silicon substrate. Poisson’s Equation (PE) uses static definitions for \(p\) and \(n\), the hole and electron concentrations, accounting for a doped silicon substrate. The Poisson-Boltzmann Equation (PBE) extends PE by including charge migration effects.

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**Table I**

Table of parameters for the system under consideration.

| Parameter               | Symbol | Value  |
|-------------------------|--------|--------|
| Minimum metal pitch     | \(\lambda\) | 53.7 nm |
| Minimum metal width     | \(w\)  | 14 nm  |
| Minimum metal thickness | \(t\)  | 10 nm  |

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Fig. 1. Bird’s eye view of single-tile electrode layouts for the columnar [a], wave [b], and USE [c] clocking schemes. Numbers denote electrode phases, and arrows indicate the direction of information flow. Colour map shows the potential swing on the silicon surface obtained by PoisSolver. Simulations assume periodic boundary conditions.
The Linearized Poisson-Boltzmann Equation (LPBE) is valid for systems with small $u$. The PBE is the most physically representative of the system, but its nonlinearity results in long convergence times.

Appropriate boundary conditions are necessary to arrive at the expected solution. Four types of boundary conditions are supported in PoisSolver:

\[ u = f_D \quad x \in \Gamma_D \]  
\[ \epsilon n \cdot u = g_N \quad x \in \Gamma_N \]  
\[ \epsilon n \cdot u + h_R u = 0 \quad x \in \Gamma_R \]  
\[ u(x + x_p) = u(x) \quad x_p \in \mathbb{R}^3 \]

where $\Gamma_D$, $\Gamma_N$, $\Gamma_R$ are the boundaries for the Dirichlet, Neumann, and Robin boundary conditions respectively, with boundary parameters $f_D$, $g_N$, and $h_R$. Electrodes are defined as domains with high $\epsilon$ and Dirichlet boundary conditions on their surfaces. All other boundary conditions are used on simulation boundaries for uniqueness. Equation (3d) is the periodic boundary condition with periodicity vector $x_p$, and is used to mimic the infinite tiling of schemes discussed in Section III.

B. Comparison between models

Fig. 3 shows potentials at the silicon surface for the columnar system using each of the four physical models with periodic boundary conditions in $x$ and $y$. Each model converges to a columnar clocking pattern, with slightly different offsets and potential swings. These offsets are attributed to the way each model handles spatial charge density.

Fig. 4 compares the PBE and LE/PE models. The LPBE model is neglected here due to its non-generality, only being representative for solutions centered around $u = 0$. To compensate for the LE’s neglect of charge density, an approximate offset was found by the Boltzmann relation and added to the LE solution, resulting in the augmented Laplace’s Equation (ALE).

At the SiDB surface, both linear models converge to solutions of the same magnitude as the PBE model, with the ALE having smaller error. For this reason, this work avoids invoking the time prohibitive nonlinear PBE, instead using the ALE to approximate the electric potential at the silicon surface.

C. Verification with COMSOL

To verify that the results here are valid, we compare results for a four electrode layout from both PoisSolver and COMSOL, a commercial finite element general physics simulator. Figs. 5a and 5b show surface potentials for the system as found by each simulator. Fig. 5c shows the difference when comparing the two tools. PoisSolver and COMSOL results are on the same order of magnitude, with a maximum 25% error.
D. Clocking network results

Using PoisSolver, surface potential patterns arising from the clocking schemes in Fig. 1 are simulated and visualised. The electrode heights and clocking voltages are tuned such that a ±100 mV potential swing appears on the surface, enough to trigger a SiDB state transition [5]. Example results for each clocking scheme are shown in Fig. 1. Though Fig. 1 shows only a single snapshot in time, full clock cycles can be simulated by repeatedly solving the system with different electrode boundary conditions.

V. CIRCUIT MODEL OF THE CLOCKING NETWORK

To model the power dissipation of the clocking network, the clocking system is mapped to a network of resistances and capacitances. A schematic of the circuit model is shown in Fig. 6. Each clocked electrode is modelled by a sinusoidal power supply with voltage amplitude $V_i$ and series resistance $R_i$. Inter-electrode and self-capacitances are denoted by $C_{ij}$ and $C_{ii}$, respectively. These capacitance and resistance values depend heavily on geometry and material properties.

A. Capacitance estimation

Many capacitance estimation techniques are geometrically constrained. Rather than using an approximation for an assumed geometry, a field solver method [20] is employed. Briefly, this method solves for the 3D potential with Pois-Solver to obtain sympathetic charges on electrodes. These charges are then used to generate the Maxwell capacitance matrix, yielding approximations for all capacitances in Fig. 6. Results from the field solver are within 1% of parallel plate approximations.

B. Resistance estimation

To approximate the effective resistance of an interconnected electrode network, the inverse Laplacian method [21] is applied. To start, the resistance of each straight resistor segment is estimated from the electrode geometry provided by SiQAD. A graph is then created, and the Laplacian method is used to obtain the effective resistance between the highest point of the network, where signals are fed in, to the lowest point where clocking fields are generated. The resistance from the inverse Laplacian method is within 2.1% of a reference calculation. This combined method reproduces results obtained by other approximations without any limitation on geometry.

VI. POWER DISSIPATION OF FOUR PHASE CLOCKING SCHEMES

With the resistance and capacitance estimation methods from Section V, power estimates are obtained for the three clocking schemes. Each scheme assumes the use of periodically tiled copper electrodes and SiO$_2$ dielectric with physical dimension constraints defined in Table I. Fig. 7 shows frequency sweeps of parasitic power dissipation for each clocking scheme up to the 100 THz range. The simulation accounts for temperature dependencies, using cryogenic resistivity data interpolated from [22]. Temperature dependence of the dielectric is neglected here, being on the order of 0.0001 K$^{-1}$ [23]. At the operating frequency of 1 GHz and 77 K (liquid nitrogen), the clock schemes dissipate power on the order of 10-100 $\mu$W cm$^{-2}$. These power densities increase to 1-10 W cm$^{-2}$ at 1 THz. Limiting factors on the maximum frequency of these clocking schemes include dissipated heat, transmission line effects, and microstrip signal injection capabilities. State-of-the-art cooling techniques can handle up to 1 kW cm$^{-2}$ [24], making these layouts viable up to the 10 THz range. For
With a cooling limit of 1 kW cm\(^{-2}\), the trend of Figure 11.

The columnar network exhibits the lowest power dissipation, while the USE network has the highest power dissipation at any particular operating point, with the wave scheme falling somewhere in between. These differences are attributed to each scheme’s routing complexity, with complex schemes having higher interelectrode capacitances.

**VII. COMPARISON WITH DEVICE POWER CONSUMPTION**

Although power densities investigated have been related to electrode clocking, the presence of SiDBs on the surface introduce other mechanisms of loss. Figure 11 in [27] relates the power consumption of a QCA cell to its kink energy. Since QCA is a potential computing architecture that can be implemented in the SiDB platform [1], we use this as an estimate for power dissipated in the DB network itself. SiDBs incur relaxations of approximately 200 meV [28], [29], and an SiDB OR gate takes up an area of 28 \(\mu m^2\). With a cooling limit of 1 kW cm\(^{-2}\), the trend of Figure 11 in [27] suggests a maximum operating frequency of 10 GHz for a SiDB system, two orders of magnitude slower than the limit of the clocking network. These estimates suggest that the bandwidth of the clocking network will not bottleneck SiDB operating frequency.

With this model, the power dissipation of the electrode network is dominated by the power dissipation of SiDB devices. However, the exact nature of SiDB power dissipation as electron populations and charge configurations change is not well understood. [30] suggests that electrons along SiDB wires hop as polarons (a combination of a defect state and a trapped electron), possibly mitigating energy loss through lattice relaxation.

**VIII. SUMMARY AND CONCLUSION**

In this paper, PoisSolver was introduced as a 3D potential solver for the SiQAD environment. Three clocking schemes from QCA were implemented in SiQAD and the resulting electrode networks were characterised with geometrically agnostic methods. Using these characterisations, the power draw of four phase clocking schemes were estimated. At 77 K, the power draw of the columnar, wave, and USE layouts were found to be 10-100 \(\mu W cm^{-2}\) at 1 GHz and 1-10 \(W cm^{-2}\) at 1 THz. Although current estimations of SiDB device power overshadow clocking dissipations, these estimates may change as dissipation mechanisms for SiDBs become better understood.

**REFERENCES**

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