Electron Mobility and Magneto Transport Study of Ultra-Thin Channel Double-Gate Si MOSFETs

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We report on detailed room temperature and low temperature transport properties of double-gate Si MOSFETs with the Si well thickness in the range $\sim 7 - 17$ nm. The devices were fabricated on silicon-on-insulator wafers utilizing wafer bonding, which enabled us to use heavily doped metallic back gate. We observe mobility enhancement effects at symmetric gate bias at room temperature, which is the fingerprint of the volume inversion/accumulation effect. An asymmetry in the mobility is detected at 300 K and at 1.6 K between the top and back interfaces of the Si well, which is interpreted to arise from different surface roughnesses of the interfaces. Low temperature peak mobilities of the reported devices scale monotonically with Si well thickness and the maximum low temperature mobility was 1.9 m$^2$/Vs, which was measured from a 16.5 nm thick device. In the magneto transport data we observe single and two sub-band Landau level filling factor behavior depending on the well thickness and gate biasing.

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1. INTRODUCTION

Advances in silicon-on-insulator (SOI) technology have made possible high quality thin channel single-gate and double-gate (DG) Si metal-oxide-field-effect-transistor (MOSFET) device structures, which are intensively explored at the moment. These both devices have many advantages over the standard bulk Si MOSFETs. However, DG MOSFETs are usually regarded as the most promising solution to the problems faced when the device/gate length is down-scaled into sub-50 nm regime (short channel effects) due to superior electrostatic gate control of the transistor channel charge. In addition of boosting the gate control the DG devices also provide other benefits in the form of enhanced electron mobility.

Apart from the relevance to the microelectronics industry the SOI material has also enabled investigation of fundamental phenomena in SiO$_2$-Si-SiO$_2$ quantum well structures. Unfortunately, the electron mobility at the Si-SiO$_2$ interface is intrinsically limited by the effects well known from standard bulk Si-MOSFETs. Despite this fact, the strong electronic and optical confinement provided by the SiO$_2$ barrier, many valley Si conduction band and indirect gap makes this quantum well system a unique tool to study several interesting effects in, for example, electron-hole liquids and bi-layer electron systems.

In this work, we report on the fabrication and detailed room temperature and low temperature electronic properties of DG Si MOSFETs with Si well thickness in the range $\sim 7 - 17$ nm. Mobility, electron density and high magnetic field diagonal resistivity are mapped in large double-gate bias windows, enabling detailed investigation of the transport properties at different gate bias (electron distribution) symmetries.

2. EXPERIMENTAL

The DG MOSFETs were fabricated on commercially available 100 mm unibond (100) SOI wafers with n$^-$ (batch B) and p$^-$ (batch F) Si layer. The nominal Si film thickness was 400 nm and the buried oxide (BOX) was 400 nm thick. First, we exchanged the insulating handle wafer to a n$^+$ wafer to enable efficient metallic back gating at all temperatures. This procedure began by a growth of a 80 nm-thick dry oxide at 1000 °C. Then the SOI wafer was vacuum bonded to a n$^+$ (111) Si wafer with $\sim 2 \times 10^{19}$ cm$^{-3}$ arsenic concentration. The bonded interface was annealed at 1100 °C and the original insulating ~500 µm-thick handle wafer was removed by etching in 25% tetramethyl ammonium hydroxide solution at 80 °C. Finally the "old" BOX layer was stripped in a 10% HF and as a result we had a SOI wafer with heavily doped handle and 360 nm thick SOI film and 80 nm thick BOX (back gate oxide).

The actual device fabrication for batch F begun by locally thinning the Si layer in some parts of the wafer in order to fabricate devices with different Si well thickness, $t_w$. This was done by utilizing standard nitride...
masking and thermal oxidation, i.e., local oxidation of silicon (LOCOS). Another two LOCOS steps were then used to define the thin channels and active areas of the devices. In the channel thinning step the Si thickness was reduced in the channel regions to create a recessed source-drain MOSFET structures. To define the active areas the parts of the Si layer that were not protected by the nitride mask were fully converted to SiO$_2$. After oxide stripping and wafer cleaning a 40 nm-thick gate oxide was grown at 1000 °C in oxygen - DCE (dichloroethylene) ambient. The applied DCE flow into the oxidation furnace corresponded to ∼2% of HCl. A 250 nm-thick polysilicon gate was deposited by CVD, implanted with As and then patterned with UV-lithography and plasma etching. The contact areas were implanted with As while the gate electrode protected the Si channel. A ∼500 nm thick CVD oxide was deposited and the implanted doses were activated at 950 °C. Finally, after contact window opening and Al metallization, the samples were annealed in H$_2$/N$_2$ ambient at 425 °C for 30 min. Devices in batch B were fabricated in a similar fashion. The major difference was that in this batch the active areas of the devices were defined by etching through the Si layer instead of LOCOS process.

Figure 1 shows a schematic cross-section of our DG MOSFET device structure together with HRTEM image of a device from batch B. Properties of the devices reported here are listed in Table I. The gate oxide thickness is $t_{OX} = 40$ nm (43 nm) and the buried oxide thickness is $t_{BOX} = 83$ nm (80 nm) for batch F (B). The cited well type is the Si layer type given by the SOI wafer manufacturer. No intentional doping is introduced into the channel in order to maximize the low temperature mobility. Further details about samples B-E721 and B-E742 can be found from 8 and 9, respectively.

All electrical characteristics reported here were obtained from Hall bar structures with 100 × 1900 μm$^2$ channel dimensions and a 400 μm voltage probe distance. We used two different methods to determine the electron density $N$: "split" capacitance-voltage (SCV) method 8 at room temperature and Shubnikov-de Haas (SdH) oscillations at low temperature. The mobility (or effective mobility) was determined from $\mu = \sigma/eN$ where $\sigma$ is the conductivity measured by a four point method and $e$ is the electronic charge. In the room temperature SCV measurements we used Agilent 4294A precision impedance analyzer at frequency of 691 Hz. This frequency was low enough to provide results that were independent of the channel resistance when all the voltage probes and the source and the drain were connected to the virtual ground of the analyzer. The channel conductivity was determined by Agilent 4156 C precision semiconductor parameter analyzer. DC offsets were systematically removed from this data by applying at least four different source-drain bias values at each gate voltage point. In the low temperature characterization the samples were mounted to a sample holder of a He-3 cryostat and the electrical measurements were performed utilizing standard low frequency lock-in techniques. A combination of voltage and current excitation was utilized in order to keep the source-drain bias from heating the electrons above the lattice temperature at sub-1 K temperatures.

3. RESULTS AND DISCUSSION

3.1. Room Temperature Mobility

Figure 2 shows experimental constant mobility and electron density contours of two DG MOSFETs with $t_W = 6.8$ nm (F-E741) and $t_W = 17.3$ nm (B-E742) as a function of top gate voltage $V_{TG}$ and back gate voltage $V_{BG}$ at 300 K. The family of curves explicitly shows how the electron mobility behaves as a function of carrier density and gate biases. We can see that for both devices on any of the constant $N$ contours the mobility maximum occurs in the vicinity of the symmetric gate bias line $V_{TG}/t_{OX} = V_{BG}/t_{BOX}$ [dashed black lines in Fig. 2]. When gate bias asymmetry is increased the mobil-
FIG. 1: Effective electron mobility $\mu$ (black thin curves) and SCV electron density $N$ (gray thick dashed curves with gray bold labels) as a function of top gate voltage $V_{TG}$ and back gate voltage $V_{BG}$ measured from (a) 6.8 nm thick and (b) 17.3 nm thick DG device at 300 K. The contour spacing for $N$ is $1.0 \times 10^{16}$ m$^{-2}$. For $\mu$ the spacing is 0.1 and $0.2 \times 10^{-2}$ m$^2$/Vs in (a) and (b), respectively. The dashed line is the symmetric gate bias line $V_{BG} = V_{TR} / t_{BOX} / t_{OX}$.

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FIG. 3: Self-consistently calculated quantum mechanical electron distribution in the Si well at different electron density values ($N = 1.2 \times 10^{16}$ m$^{-2}$ from bottom to top) at symmetric gate bias at 300 K. The calculations were performed for 12 sub-bands within the Hartree approximation.
indicates single sub-band occupation and the \( \nu \) disorder broadening of the LLs. The weakening of the minima can be addressed to cyclotron, valley trajectories, which suggest that only the ground 2D sub-band is populated. The constant LL trajectories \( \nu \) trajectory in Fig. 5(b). Therefore, Zeeman and valley splitting can push the lower valley down state of the second sub-band in to the valley gap \( \nu = 3 \) of the first sub-band around the symmetric bias, where \( \Delta_{\text{BAB}} \) has a minimum value. This could explain the destruction of the \( \nu = 3 \) QH state (appearance of finite \( \rho_{xx} \)) at symmetric gate bias. Note that the effect is complicated by the possible symmetry dependency of valley splitting and also by modulation of interface trap Coulomb scattering. These effects will be further explored elsewhere.

3.2. Magneto Transport

Figure 3 shows the diagonal resistivity \( \rho_{xx} \) measured as a function of top and back gate voltages from two DG MOSFETs F-E73 (\( t_W = 7.0 \) nm) and F-E42 (\( t_W = 14.2 \) nm) at \( B = 9.0 \) T at 0.27 K. The numbers inside the axis indicate the Landau level (LL) filling factors \( \nu = Nh/eB \). The bright and dark color correspond to low and high \( \rho_{xx} \), respectively. In the white regions \( \rho_{xx} \approx 0 \) and Hall resistance \( \rho_{xy} \) is equal to integer quantum Hall (QH) value \( h/e^2\nu \). The obscured maximum slightly below the symmetric bias line and close to the threshold in both \( \rho_{xx} \) data is an experimental artefact (present below \( \sim 1 \) K). [11] We first draw our attention to the LL filling factor behavior of the thin sample F-E73 [Fig. 3(a)]. We can observe that the \( \rho_{xx} \) minima are continuous trajectories, which suggest that only the ground 2D sub-band is populated. The constant LL trajectories \( \nu = 4(k+1), \nu = 2k + 3 \) and \( \nu = 4k + 2 \) \( (k = 0,1,2...) \) can be related to cyclotron, valley and spin gaps, respectively. When the gate biases confine the electron gas closer to the back interface \( V_{BG} > V_{TG}t_{\text{BOX}}/t_{\text{OX}} \) the \( \rho_{xx} \) minima corresponding to \( \nu = 6 \) and \( \nu = 10 \) become shallow. This weakening of the minima can be addressed to the stronger elastic scattering in the vicinity of the Si-BOX interface, which was already detected in the room temperature mobility (see also next sub-section), leading to disorder broadening of the LLs.

The thick sample F-E42 [Fig. 3(b)] behaves similarly in comparison to F-E73 when electron density is low (small \( \nu \)) and also when \( V_{BG} \lesssim 0.5 \) V or \( V_{TG} \lesssim 0.25 \) V. This indicates single sub-band occupation and the \( \rho_{xx} \) minimum trajectories can be addressed to cyclotron, valley and spin gaps as was done above. In the bias region where \( V_{BG} \gtrsim 0.5 \) V, \( V_{TG} \gtrsim 0.25 \) V and \( \nu > 4 \) the trajectories are broken into a 2D pattern, which is a signature of two sub-band (bi-layer) transport [7, 8, 12]. By analyzing the SdH oscillations of \( \rho_{xx} \) as a function of inverse magnetic field (at 0.3 K) in the spirit of Ref. [12] along the symmetric bias line we find that when top gate is adjusted between \( V_{TG} = +0.9 \) to \(+2.78 \) V the energy spacing of the bonding - antibonding sub-bands, \( \Delta_{\text{BAB}} \), varies monotonically from 23 to 2 meV.

The threshold for the second sub-band is already at \( V_{TG} \approx 0.75 \) V on the symmetric bias line, which is roughly on the \( \nu = 3 \) trajectory in Fig. 5(b). Therefore, Zeeman and valley splitting can push the lower valley down state of the second sub-band in to the valley gap \( \nu = 3 \) of the first sub-band around the symmetric bias, where \( \Delta_{\text{BAB}} \) has a minimum value. This could explain the destruction of the \( \nu = 3 \) QH state (appearance of finite \( \rho_{xx} \)) at symmetric gate bias. Note that the effect is complicated by the possible symmetry dependency of valley splitting and also by modulation of interface trap Coulomb scattering. These effects will be further explored elsewhere.

3.3. Low Temperature Mobility

Figure 6 shows experimental constant mobility contours at 1.6 K and SdH electron density contours of device F-E73 as a function of \( V_{TG} \) and \( V_{BG} \). The electron density is determined from SdH oscillations at 0.27 K: \( N \) is obtained from similar constant \( \nu \) trajectories in \( \rho_{xx} \) at constant magnetic field that were discussed above. Magnetic field value of \( B = 2.5 \) T was chosen in order to keep all \( \rho_{xx} \) minima clearly above zero, which enabled accurate determination of constant LL trajectories. In the conductivity measurement at 1.6 K a small magnetic field (0.2 T) was applied to suppress the quantum corrections of conductivity.

The electron density and gate bias symmetry dependency of low temperature mobility of F-E73 in Fig. 6 closely resembles that of room temperature effective mobility of F-E741 [Fig. 3(a)]. Due to absence of phonon scattering the asymmetry in the elastic scattering properties of the two interfaces is now brought out more clearly. It is evident that the maximum mobility is shifted from the symmetric gate bias position towards larger \( V_{TG} \) and smaller \( V_{BG} \) on any of the constant \( N \) contours.

If we adjust the gate voltages along an arbitrarily chosen straight line (direction) in Fig. 6 in such a fashion that \( N \) increases the mobility shows the typical MOSFET behavior, where the mobility first increases at low carrier density, reaches a maximum value and then decreases at high carrier density. This behavior can be addressed to well known elastic scattering mechanisms: Coulomb scattering that is most effective at low \( N \) and interface roughness scattering that is most effective at high \( N \). [14]
When \( t_W \gtrsim 10 \text{ nm} \) the second sub-band becomes populated even when both gates have a modest positive bias, as was demonstrated in the previous sub-section. This alters the mobility behavior and in general the simple Coulomb/surface roughness-scattering picture is lost. Further effects arise from the fact that in some bias ranges the electrons in the second sub-band can be localized \[8\]. The coexistence of localized and non-localized electrons complicates the scattering mechanisms \[15, 16\] and discussion of such effects is beyond the scope of this paper. Therefore, full \( V_{TG} - V_{BG} \) mobility dependency of the devices with \( t_W \gtrsim 10 \text{ nm} \) will be reported elsewhere. Here we only cite the maximum mobilities, which can be found from Table II. The maximum mobility \( \mu_{\text{max}} \) decreases with decreasing \( t_W \) as expected. \( \mu_{\text{max}} \) scaling with \( t_W \) is consistent with recent experimental observations on single gate SOI devices \[17\].

Finally, we note that as the maximum mobilities for all devices are relatively high it is unlikely that the mobility degradation at the back interface could originate from increased Coulomb scattering: the degradation is mainly due to interface roughness scattering. High mobility also indicates extremely low interface trap density, which justifies our assumption that in the room temperature measurements the SCV electron density corresponds to that of mobile electrons.

4. SUMMARY

In summary, we have reported on detailed room temperature and low temperature transport properties of ultrathin channel double-gate Si MOSFETs. The devices were fabricated on SOI wafers utilizing wafer bonding, which enabled us to use heavily doped metallic back gate. The devices showed mobility enhancement effects at symmetric gate bias at room temperature, which is the fingerprint of the volume inversion/accumulation effect. Small asymmetry in the mobility could be detected at 300 K between the top and back interfaces of the Si well. The effect could be enhanced at low temperatures and the mobility asymmetry was interpreted to arise from different interface roughness of the top and back interface. Low temperature peak mobilities of the reported devices scale monotonically with Si well thickness and the maximum low temperature mobility was \( 1.9 \text{ m}^2/\text{Vs} \), which was measured from a 16.5 nm thick device. From the magneto transport data we observed single and two sub-band transport effects depending on the well thickness and gate biasing.

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FIG. 6: Contour plot of electron mobility $\mu$ (black thin curves with black labels) and SdH electron density $N$ (gray thick dashed curves with gray bold labels) measured from the 7.0 nm thick DG device. Mobility is determined from conductivity measured at 1.6 K and SdH electron density, which is measured at $B = 2.5$ T at 0.27 K. The contour spacing for $\mu$ above (below) 0.4 m$^2$/Vs is 0.02 m$^2$/Vs (0.05 m$^2$/Vs). The dashed diagonal line is the symmetric gate bias line.

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