A Quasi-Multilevel Gate Driver for Fast Switching and Crosstalk Suppression of SiC Devices

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ABSTRACT The crosstalk phenomenon in a phase-leg configuration forbids the operation of SiC devices at high switching speed. A multilevel gate driver (MGD) is well-known for crosstalk mitigation, however, it requires two driver ICs and two voltage supplies to generate four different levels in the gate-source waveform. This paper presents a low-cost quasi-multilevel gate driver (QMGD) for crosstalk suppression which can be implemented on a single driver IC using only positive supply voltage. With a simple auxiliary circuit of the parallel-connected transistor, zener diode, and a capacitor, the proposed driver can generate multilevel output. The auxiliary transistor governs the charging and discharging of the capacitor, controlling voltage at the source terminal of SiC MOSFET and thus generating different voltage levels essential for crosstalk suppression. Performance of the proposed gate driver is validated through Spice based simulation as well as experimental tests conducted with Cree C2M0025120D. It is concluded that the proposed QMGD can replace a complicated MGD without any loss of performance.

INDEX TERMS Crosstalk suppression, quasi-multilevel gate driver (QMGD), SiC MOSFET.

I. INTRODUCTION Wide bandgap devices have revolutionized the power electronics technology and gained rapid acceptance due to improved characteristics like fast-switching, high-voltage, high-temperature, and high-efficiency. However, these devices have relatively restricted gate voltage range, which introduces gate driver design challenges [1]. Particularly, due to low gate threshold voltage of SiC MOSFET, a phase-leg configuration encounters the crow-bar current which increases switching losses and thus degrades the converter efficiency. Therefore, to fully utilize SiC MOSFET to its potential, the spurious voltage spikes should be restricted.

Phase-leg configuration with low-side MOSFET $S_L$ and a high-side MOSFET $S_H$ is shown in Figure 1(a) with related list of symbols given in Table 1. The crosstalk occurs due to fast-rising or falling of drain-source voltage, which induces a current in the parasitic capacitance and introduces spurious spike in the gate-source voltage [2]. When $v_{GSH}$ climbs above $V_{TH}$, it initiates the turn-on transient of $S_H$ and the steep slope of the drain-source voltage of $S_L$ induces a positive spike in $v_{GSL}$ as illustrated in Figure 1(b). Spurious turn-on of $S_L$ occurs if the peak of the gate voltage spike is more than the threshold voltage, causing shoot-through and increasing switching losses. Figure 1(b) also shows a negative spike in $v_{GSL}$ which occurs during $S_H$ turn-off transient, when $v_{GSH}$ drops below the miller voltage. The negative voltage spike in $v_{GSL}$ can damage the oxide layer, leading to failure of the device. Therefore, it is equally important to protect a SiC MOSFET against the negative excursion of gate-source voltage. To justify the cost of SiC MOSFET by fully capitalizing its advantages, several techniques have been proposed [3], [4]. The conventional technique uses an external gate-source capacitance to suppress spurious spikes, however, it prolongs the rise time of the gate voltage and thus degrades the converter efficiency.

An MGD proposed in [5], has been proven to be the most suitable choice for driving a SiC MOSFET to ensure crosstalk suppression. Moreover, it accelerates the switching transition from blocking to conduction state by applying a maximum allowed gate-source voltage which reduces the switching losses. On the other hand, it relaxes the gate oxide stress by setting gate-source voltage to zero before the transition to the turn-on level. In [6], the authors proposed an active...
MGD by connecting driver ICs in series. Similarly, a 3-level turn-off waveform is generated in [7] by driving the negative pole of one driver IC with the output of another. It means that a combination of driver ICs powered by two voltage supplies is required for the generation of multilevel output, raising cost, and layout design complexity. Other techniques listed in Table 2 are developed employing auxiliary circuits to generate multilevel gate-source voltage waveform.

This paper presents a low-cost four-level QMGD for SiC MOSFET by adding an active switch to the auxiliary circuit of [10] and the capacitor which acts as a local source is charged from driver output instead of driver supply, reducing driver losses. Applying maximum allowable drive voltage accelerates switching transition and clamping the gate voltage to zero reduces the risk of gate breakdown due to negative gate voltage spike. The proposed driver offers several advantages over reported work in literature. First, and the most important feature is its ability to generate a multilevel gate voltage using only a positive supply voltage. This feature eases the layout design of a power converter, leading to low parasitic inductances and reduction in electromagnetic interference (EMI). Second, the proposed circuit enables a four-level output using only one active switch which reduces complexity in implementation because the active switches also need gate signals for their driving to perform the desired operation.

The rest of the paper is organized as follows. Section II presents the operating principle of the QMGD. Also, mathematical relations are derived. The parameters design is given in Section III. Simulation and experimental results verify the performance of the proposed driver in section IV, followed by the conclusion in section V.

**II. OPERATING PRINCIPLE OF QMGD**

In order to overcome the aforementioned shortcomings, a simple gate driver for SiC MOSFET is proposed in Figure 2(a), with auxiliary circuit comprising a transistor $M$, a zener diode $D_Z$, current limiting resistors $R_M$ and $R_C$, and a capacitor $C_Z$. Due to charging and discharging operation of $C_Z$, the transition between gate voltage levels for a given switching state is smooth, therefore, the effect of parasitic inductance in the driver loop is minimized. Since the proposed QMGD enables four-level output using one additional active switch $M$ driven by signal $u_M$ which is a delayed version of $u_{DL}$, thus the auxiliary circuit doesn’t add much complexity. In addition, the source terminal of $M$ is connected to driver ground, which eases its driving as compared to the floating source case.

Since $C_Z$ is connected between the source terminal of SiC MOSFET and driver ground, levels in $v_{GSL}$ can be introduced

| Specification | Value |
|---------------|-------|
| $V_{IN}, V_G$ | Converter source voltage and driver supply voltage |
| $L$ | Output stage inductive filter |
| $f_S, T_S$ | Switching frequency and period |
| $V_{TH}, V_{MIL}, V_{ML}, V_{HL}$ | Threshold and miller voltage |
| $u_{DSL}, u_{DL}$ | Logic signal for $M$, $S_L$, and $S_H$ |
| $C_{GS}, C_{GD}$ | Gate-source, drain-gate, and drain-source capacitance |
| $C_{DS}, R_{ON}, R_{OFF}$ | Gate resistances $\alpha_C = R_C/(R_C + R_{M})$, $\alpha_M = R_M/(R_C + R_M)$ |
| $R_{BH}$ | $R_{BH} = R_{G(ON)} + R_{ON} + \alpha_C R_{M}$ |
| $V_{GSL}, V_{GSH}$ | Capacitor and zener diode of auxiliary circuit |
| $V_{NL}, V_Z$ | Voltage across $C_Z$ and zener voltage |
| $i_{RC}$ | $C_Z$ charging current |

**TABLE 2. Auxiliary circuit based MGD circuits.**

| Auxiliary circuit | Output | Drawback |
|------------------|--------|----------|
| 1. Voltage divider circuit [8] [9] | two-level | Additional gate-source capacitor is required for suppression of negative voltage spike |
| 2. Parallel connection of zener diode and capacitor [10] | two-level | Due to voltage oscillations requires RC snubber |
| 3. Circuit comprising pair of Schottky diode, zener diode, MOSFET and capacitor [11] | three-level | Requires dedicated negative voltage supply |
| 4. Circuit comprising zener diode, MOSFET and capacitor [12] | four-level | Continuous charging current from driver supply |
by controlling the voltage \( v_N \). Due to parallel connection of \( C_Z \) with active switch \( M \) and zener diode \( D_Z \), \( v_N \) has steady-state values of \( V_Z \) and \( \alpha_M V_G \). Thus, voltage \( v_N \) raises when \( u_{DL} = 1 \) and \( u_M = 0 \) and saturates at \( V_Z \) due to parallel connection with \( D_Z \). When \( u_{DL} \) changes to 0, the driver circuit applies \(-V_Z\) to the gate of SiC MOSFET, generating negative turn-off voltage. Therefore, the QMGD enables four-levels, that are \( \alpha_M V_G \), \((V_G - V_Z)\), \(-V_Z\), and 0 in the \( v_{GSL} \) waveform as shown in Figure 2(b), where \( V_G \) is the driver supply voltage and \( \alpha_M \) is the scaling factor determined by \( R_M \) and \( R_C \). The switching signal \( u_M \) is a time-shifted version of \( u_{DL} \) having same time-period, therefore, perform the desired operation without any significant power losses.

The equations for \( v_{GSL} \) and \( v_N \) are derived by applying KVL to the equivalent circuits during each interval, which is essential to determine the optimized parameters of QMGD. The equivalent circuits for each interval are given in Figure 3. To ease the analysis, the conduction resistance of \( M \) and parasitic inductances of SiC MOSFET are neglected.

**A. INTERVAL I: \( t_0 \leq t \leq t_1 \)**

Turn-on transient of SiC MOSFET occurs in this interval. Since \( u_{DL} = u_M = 1 \), the driver supply voltage enforces a charging current \( i_{GS} \) through \( C_{GS} \), which in addition to gate resistances \( R_{ON} \) and \( R_{G(in)} \), also flows through \( R_M \). Applying KVL to the driver loop in the equivalent circuit, the dynamic equation is given in (1).

\[
\begin{align*}
\alpha_C V_G &= R_{th} C_{GS} \frac{dv_{GS}}{dt} + v_{GS} \\
\frac{d}{dt} v_N &= \alpha_M R_C C_{GS} \frac{dv_{GS}}{dt} + \alpha_M V_G
\end{align*}
\]

Solving with initial condition \( v_{GS}(t_0) = 0 \) (stored energy released in \( R_M \) before time \( t_0 \)) results in (2). Equation indicates that \( v_{GS} \) approaches \( \alpha_M V_G \), with time-constant given by the product \( R_{th} C_{GS} \), where \( R_{th} = (R_{G(in)} + R_{ON} + \alpha_C R_M) \) and \( \alpha_C = R_C/(R_M + R_C) \). Since, the time-constant of equivalent circuit depends on \( R_M \), it should be relatively smaller to ensure minimal effect on slope of \( v_{GS} \), meaning that \( \alpha_C \) should be close to 1. Also, the voltage \( v_N \) increases to attain a steady-state value determined by \( \alpha_M = R_M/(R_M + R_C) \), therefore, \( R_M \) should keep \( v_N \) negligibly small in this interval.

\[
\begin{align*}
v_{GS}(t) &= \alpha_C V_G \left[ 1 - \exp \left( -\frac{t}{R_{th} C_{GS}} \right) \right] \\
v_N(t) &= \alpha_M V_G \left[ 1 + \alpha_C \frac{R_M}{R_{th}} \exp \left( -\frac{t}{R_{th} C_{GS}} \right) \right]
\end{align*}
\]

**B. INTERVAL II: \( t_1 \leq t \leq t_2 \)**

By the end of interval I, \( i_{GS} \) decays to 0 and \( v_{GS} \) and \( v_N \) achieve the steady-state values of \( \alpha_C V_G \) and \( \alpha_M V_G \), respectively. Meaning that only current \( i_{RC} = V_G(1 - \alpha_M)/R_C \) flows in \( R_C \), regulating \( v_{GS} \) and \( v_N \). Since \( i_{RC} \) contributes to power dissipation, optimal value of \( R_C \) needs to be chosen.

**C. INTERVAL III: \( t_2 \leq t \leq t_3 \)**

At time \( t_2 \), \( u_{DL} \) is still high while \( u_M \) toggles to the low logic level, turning-off \( M \). \( C_Z \) begins to charge by currents \( i_{GS} \) and \( i_{RC} \), raising \( v_N \). This reduces \( v_{GS} \) as indicated in equation (3), where \( RC_{GS} \) determine the transition time. To ensure that \( v_{GS} \) attain next voltage level before the transition of \( u_{DL} \) to 0 logic level, time-constant \( RC_{GS} \ll D_m t_3 \), where \( D_m \) is the minimum duty ratio of SiC MOSFET. Interval III ends when \( v_N \) and \( v_{GS} \) get to voltage level \( V_Z \) and \( (V_G - V_Z) \), respectively.

\[
\begin{align*}
v_{GS}(t) &= \alpha_C V_G - v_N(t) \\
v_N(t) &= V_G \left[ 1 - \exp \left( -\frac{t}{R_C C_{GS}} \right) \right]
\end{align*}
\]

**D. INTERVAL IV: \( t_3 \leq t \leq t_4 \)**

At time \( t_3 \), \( C_Z \) is pre-charged to voltage \( V_Z \). Due to parallel connection, zener current \( i_Z \) flows in \( D_Z \), regulating \( v_{GS} \) and \( v_N \) at \((V_G - V_Z)\) and \( V_Z \), respectively. Therefore, \( i_{GS} = 0 \) and \( i_Z = i_{RC} = (V_G - V_Z)/R_C \).

**E. INTERVAL V: \( t_4 \leq t \leq t_5 \)**

Turn-off transient of SiC MOSFET occurs in this interval. The logic level of \( u_{DL} \) toggles to 0, internally connecting

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**FIGURE 2. Proposed QMGD for SiC MOSFET (a) circuit diagram (b) operating waveforms.**

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the out of driver IC to the ground. Therefore, current $i_{RC}$ is 0 and $C_{GS}$ and $C_Z$ discharges in $R_{OFF}$. Since, $C_Z$ acts as a local source to generate negative turn-off voltage, negligible change in $v_N$ should be ensured which requires $C_Z \gg C_{GS}$. If we assume $v_N = V_Z$ in interval $V$, transition time of $v_{GS}$ from $(V_G - V_Z)$ to $-V_Z$ is determined by $R_{OFF}$ as indicated by equation (4). $v_{GS}$ and $v_N$ saturates at $-V_Z$ and $V_Z$, respectively, when $i_{GS}$ reduces to 0. The QMGD generates a negative turn-off voltage, that is $-V_Z$ without using an additional voltage supply. To eliminate switching crosstalk, the other SiC MOSFET in the phase-leg must be turned-on in this interval.

$$\begin{align*}
    v_{GS} (t) &= V_G \exp \left( -\frac{t}{R_{OFF} \cdot C_{GS}} \right) - V_Z \\
    v_N (t) &= V_Z
\end{align*}$$

(4)

**F. INTERVAL VI: $t_5 \leq t \leq t_6$**

The signal $u_M$ toggles to its high logic level at $t_5$, turning-on auxiliary switch $M$ and thus discharging $C_Z$. Equation (5) indicates that $v_{GS}$ raises from $-V_Z$ to 0. Since the fast

\[ v_{GS} (t) = V_G \exp \left( -\frac{t}{R_{OFF} + R_{G(in)}} \cdot C_{GS} \right) - V_Z \]
transition in this interval doesn’t offer any advantage, $R_{ON}$ is chosen based on the operation in the interval I. Afterwards, both $v_{GS}$ and $v_{N}$ regulates at 0. Therefore, SiC MOSFET can safely operate when the negative gate voltage spike occurs due to the turn-off transient of complementary device.

$$
\begin{align*}
v_{GS}(t) &= -V_Z \exp \left( -\frac{t}{(R_{ON} + R_{G(in)}) C_{GS}} \right) \\
v_{N}(t) &= V_Z \exp \left( -\frac{t}{R_M C_{GS}} \right)
\end{align*}
$$

(5)

### III. SELECTION OF QMGD PARAMETERS

In this section, design rules for $C_Z$, $R_C$, and $R_M$ are presented. Auxiliary circuit waveforms in Figure 4 indicates four important constraints on QMGD parameters. First, the turn-on voltage is $v_{GS} = \alpha V_G$, which is less than $V_G$ as the drop across resistor $R_M$ is $\alpha M V_G$. Second, during turn-off transient, $C_Z$ releases some of its energy, which can be reduced if $C_Z \gg C_{GS}$. Third, the time required for charging of $C_Z$ to voltage $V_Z$ is determined by $\frac{C_Z}{R_C}$, thereby $R_C$ cannot be selected freely to reduce the power losses, otherwise, the capacitor will charge to a level lower than $V_Z$ which can compromise crosstalk suppression. Fourth, $V_Z$ comes out to be the negative turn-off gate voltage, thus it is important to select diode with zener voltage less than the allowable negative voltage.

Resistor $R_M$ should be of smaller value in order to ensure fast turn-on, however, the $C_Z$ discharging current during interval V will be significantly high. Thus, the power ratings of resistor $R_M$ and transistor $M$ are considered based on the operation in interval I and V. To find $R_M$ for a given value of $t_1$, required for the transition of $i_{GS}$ from $V_G/R_{th}$ to $0.1 V_G/R_{th}$, using (1) gives

$$
R_M = \frac{t_1}{\ln (0.1) \alpha C_{GS}} - \frac{(R_{ON} + R_{G(in)})}{\alpha C}
$$

(6)

### IV. RESULTS AND DISCUSSION

The performance of the proposed QMGD is validated using Spice based simulation as well as with experimental setup. SiC MOSFET employed for the performance verification of driver is C2M0025120D from Cree. Considering the gate-source voltage limits (25 V/−10 V), a 25 V gate driver supply is used to generate drive waveform with levels $+24.67$ V, $+19.57$ V, $-5.1$ V and 0 V. A double pulse test (DPT) with parameters listed in Table 3 are used to evaluate the performance of gate driver. Parameters of the QMGD circuit, optimized using mathematical relations are given in Table 4.
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FIGURE 6. Simulation results (a) Waveforms at full load (b) $v_N$ and $v_{GSL}$ for different values of $R_{OFF}$ (c) $v_N$ and $v_{GSL}$ for different values of $R_C$ (d) Zoomed view of (c).

FIGURE 7. Experimental setup of the proposed QMGD.

1) SIMULATION RESULTS

The Spice model of SiC MOSFET provided by Cree Inc. is tailored to match the simulation response with that in the actual circuit. Parameters of the Spice model are listed in Table 5, simulated with step size and dead-time of 1 ns and 600 ns, respectively. $u_M$ is delayed by 24 $\mu$s relative to $u_{DL}$, meaning that $v_{GSL}$ stays at 24.67 V for nearly 4 $\mu$s as shown in the simulation result of Figure 6(a). It can be observed from

TABLE 3. Parameters of DPT.

| Specification       | Value  |
|---------------------|--------|
| Input voltage ($V_{IN}$) | 400 V  |
| Width of second pulse ($t_w$) | 20 $\mu$s |
| Inductor ($L$)      | 100 $\mu$H |
| Current ($I_L$)     | 20 A   |

TABLE 4. Parameters of the QMGD.

| Specification | Value  |
|---------------|--------|
| $R_C$         | 150 $\Omega$ |
| $R_M$         | 2 $\Omega$  |
| $R_{ON}$      | 10 $\Omega$ |
| $R_{OFF}$     | 10 $\Omega$ |
| $C_T$         | 100 mF   |
| $V_T$         | 5.1 V    |
the simulation results that positive spurious spike is below the gate threshold voltage and thus doesn’t cause crosstalk. Figure 6(b) shows that for higher values of $R_{OFF}$ it takes $v_{GSL}$ longer time to reach $-V_Z$. Figure 6(c) and 6(d) show that higher values of $R_C$ result in lower charging current and longer falling time. Therefore, longer dead-time is required, which increases power losses as body diode of SiC MOSFET is not best in characteristics compared to Si counterpart.

2) EXPERIMENTAL RESULTS

To conduct the experimental tests, a DPT platform is constructed using Cree C2M0025120D SiC MOSFET. Prototype of the proposed gate driver is given in Figure 7. The QMGD is implemented using ADuM4135, which is an isolated gate driver IC having 4 A drive capability. For short circuit protection of power MOSFET, the driver IC embodies the desaturation detection circuit. Also, it features an Under Voltage Lock Out (UVLO) which protects the power circuit when the driver supply voltage drops below the specified threshold. The logic signals $u_{DL}$ and $u_{M}$ are generated from a digital signal processor. Two tests are conducted on the prototype: first, the effect of parameters $C_Z$, $R_C$, and $R_{OFF}$ on the waveform of $v_N$ and $v_{GSL}$ is captured and second, the waveforms of $v_N$, $v_{DSL}$, $v_{GSL}$, and $i_L$ are recorded to verify the crosstalk suppression.

Figure 8 shows the operation of proposed driver at no-load comparing $v_N$ and $v_{GSL}$ for different circuit parameters. Waveforms for 50 nF, 100 nF and 200 nF values of $C_Z$ are compared in Figure 8(a) and two regions are highlighted where the effect is evident. First the $v_{GSL}$ transition time from...
24.67 V to 19.57 V increases with $C_Z$, minimum of 3 $\mu$s for 50 nF (shown in red) and 8.3 $\mu$s for 200 nF (shown in green). Second is the turn-off voltage which gets more negative with $C_Z$, that are $-3.3$ V and $-5.01$ V for 50 nF and 200 nF case, respectively. Since $R_C$ sets the $C_Z$ charging current, its effect on the waveform is quite similar as shown in the comparison of Figure 8(b), for $R_C$ of 150 $\Omega$, 499 $\Omega$ and 1 k$\Omega$. The zoomed view of Figure 8(b) is presented in Figure 8(c), which indicates that bigger $R_C$ cannot charge $C_Z$ to the voltage level $V_Z$ before turn-off transient. For $R_C = 1$ k$\Omega$, $v_N$ has reduced to 2.5 V, which may not be enough to suppress crosstalk because the positive spike can violate the MOSFET threshold voltage. Another parameter that affects the operating waveforms is $R_{OFF}$, which controls the turn-off transient as shown in Figure 8(d). The time required for $v_{GSL}$ transition from 19.57 V to 0 V is 65 ns and 113 ns for $R_{OFF}$ of 150 $\Omega$ and 1 k$\Omega$, respectively. Please note that reducing $R_{OFF}$ suppresses the peak of positive gate voltage spike, accelerates the turn-off transient and lowers the switching losses.

The second set of results are given in Figure 9(a), measured at operating condition 400 V/20 A, with $R_{OFF} = 10 \Omega$. The negative spike in $v_{GSL}$ during turn-off transient of the high-side SiC MOSFET is observed to be $-8.1$ V that is well above the allowable negative gate voltage ($-10$ V for C2M0025120D) as shown in Figure 9(b). Similarly, it is observed from turn-on transient of high-side device shown in Figure 9(c) that $v_{GSL}$ can go as high as 2.2 V which is less than the threshold voltage (2.6 V for C2M0025120D), suppressing crosstalk.

V. CONCLUSION

A QMGD has been proposed in this paper for crosstalk suppression. The simulation and experimental results using Cree C2M0025120D indicate that QMGD can successfully
generate a multilevel gate-source waveform using only positive driver supply. Spurious turn-on of SiC MOSFET is avoided as the gate voltage spike is level shifted and is kept below 2.2 V at full load condition, that is lower than the threshold voltage of 2.6 V. Similarly, using zero-voltage clamping, SiC MOSFET is protected against the negative gate voltage spike, measured as ~8 V at full load condition. Being a simple, low-cost and implementable with one driver IC, the QMGD is an excellent alternative to the conventional MGD. It is worth mentioning that the proposed QMGD is also applicable to GaN cascode transistors.

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