DECTING ERRORS IN REVERSIBLE CIRCUITS WITH INVARIANT RELATIONSHIPS

NUNO ALVES
NUNO@BROWN.EDU
ENGINEERING DIVISION, BROWN UNIVERSITY

ABSTRACT. Reversible logic is experience renewed interest as we are approach the limits of CMOS technologies. While physical implementations of reversible gates have yet to materialize, it is safe to assume that they will rely on faulty individual components. In this work we present a present a method to provide fault tolerance to a reversible circuit based on invariant relationships.

1. Introduction

The advent of CMOS scalability and power dissipation limits is bringing a renewed interest in reversible architectures. In essence, these architectures contain logic gates that are able to reuse energy that was spent to generate previous results. In fact, the main purpose of reversible architectures is to improve the computational efficiency further than the fundamental Von Neumann limit \[ \frac{kT \ln 2}{\text{energy dissipated per irreversible bit operation}} \] where \( k \) is Boltzmann’s constant and \( T \) is absolute temperature. This limit is characterized as fundamental because its value is independent of the properties of the device, materials, or circuit that may be used to implement the logic operation [16]. In theory, a fully reversible architecture would dissipate no energy.

1.1. Historical Perspective. In 1961, Rolf Landauer showed that traditional binary (irreversible) gates lead to power dissipation regardless of their implementation [13]. He did so by noticing that any logically irreversible manipulation of information, such as the erasure of a bit or the merging of two computation paths, always increase the entropy of the system. For each computational operation in which a single bit of logical information is lost, the entropy generated is at least \( kT \ln 2 \), which means the system will have an energy increase of \( kT \ln 2 \) joules. In 1973, Charles Bennett demonstrated that unlike the erase operation, the read operation did not bring any entropy increase to the system [3]. Therefore, one possible way to circumvent the release of energy into the system per operation, is to have a circuit built from gates that are capable of using previous logic outputs as inputs to that same gate. In other words, these gates need to be reversible.

1.2. Synthesis of Reversible Gates. In accordance to Bennett’s demonstration, a reversible gate is one that:

   (1) Has an equal number of inputs and outputs
   (2) Each input/output vector must be unique

When different input vectors have the same output vector, the function is irreversible. It is irreversible because it is impossible to determine the input vectors from the output vectors. The NOT gate is reversible, as every single output maps
Several reversible gates have been proposed. Some well known gates are listed on figure 1. Of the listed gates all are universal, since combinations of them can be used to accomplish any arbitrary Boolean function. For example, in the Toffoli gate on figure 1 when C=1, R=¬(AB), which is the universal Boolean operation NAND.

Figure 2 shows the state table for a 3x3 Fredkin gate, where it can be clearly seen the one-to-one mapping between the inputs and outputs. In addition, Fredkin gate also preserves parity.

As expected, synthesis of reversible circuits does not follow the traditional methods. First of all, as natural consequence of the one-to-one mapping characteristic of reversible gates, neither feedback loops or fan-outs are allowed. Each gate output is used as an input to the next gate, resulting in a network of cascading gates. In the most brutal fashion, converting an irreversible function into a reversible function is simple: one must simply add extra outputs and inputs to guarantee a one to one mapping. This approach is dis-encouraged as it would unnecessarily increase the size of the design and it would also create many instances where information is not re-used. The extra outputs that are produced to maintain the reversibility of
the gate, that are not used downstream are called *garbage outputs*. These *garbage outputs* are undesirable as they dissipate energy into the circuit. If the maximum number of identical output vectors is \( p \), then \( \log_2 p \) garbage outputs (and some inputs) must be added to make the input-output vector mapping unique \([1]\).

To date there has been no definite answer in the synthesis of reversible circuits. Earlier synthesis heuristic methods were plagued by scalability faults and they made extensive use of template matching \([17, 10, 14]\). Some of these algorithms would not converge or the extensive use of *garbage outputs* made the designs impractical. In 2006 Gupta et al \([9]\) presented a synthesis algorithm using networks of \( n \)-bit Toffoli gates and it was expanded in \([5]\) to include \( n \)-bit Fredkin and Peres gates. The source code of this project has been released to the scientific community since then \([12]\).

Other efforts consisted of synthesising using just CNOT gates \([28]\) and creating SAT based synthesis with Toffoli gates network synthesis \([8]\). While recent developments have been promising they are still far from the optimal results computed by slow exhaustive search algorithms \([23]\).

Despite the fact that at the present time no truly reversible architectures have been successfully manufactured, it is not a far fetched assumption that in the future they will have to rely on individual components prone to failures through faulty components. In reversible architectures, fault tolerance is even more critical than in conventional circuits as errors generate heat, the very problem that the architecture is trying to solve \([4]\). This work will investigate the possibility of using natural, or artificial, logic invariant relationships in reversible circuits as a method of achieving fault tolerance.

## 2. Related Work

The synthesis rules referenced above impose a very strong restriction on reversible fault tolerance implementations. In non-reversible logic circuits it is not uncommon to use redundant circuit elements which may include simple duplication of the entire design, triple modular redundancy (TMR). This can be trivially implemented in reversible logic with the addition of extra hardware to accommodate input/output fan-out to feed multiple three copies of the circuit, and a reversible comparator \([4]\). The problem with this approach is the extensive hardware overhead. Another widely studied approach error consists on the implementation of parity codes. This method has been widely studied in reversible architectures. Since reversible gates have the same number of inputs and outputs, a sufficient requirement for parity preservation of a reversible circuit is that each individual gate be parity preserving, i.e. have the same parity for inputs and outputs \([19]\). As an example, Fredkin gate preserves parity (figure 2) but the Toffoli gate does not. During circuit operation, if we know the parity of the inputs and outputs, we can compare them to see if there is an error caused mismatch. Parhami demonstrated the feasibility of the parity preserving design adding parity protection to Toffoli gates and designing a full adder \([19]\). Others have taken this idea even further by also implementing simple circuits that support error correction with hamming codes \([11]\). Another error detection method reported in the literature consisted on self checking reversible gate pairs \([25]\). While an interesting method the excessive number of garbage outputs made its usefulness very limited. In non-reversible architectures a recent approach to online error detection using naturally occurring invariant relationships has been proposed \([18]\). In this paper we will study the feasibility of using invariant relationships in reversible circuits. In addition we will
Figure 3: Invariant relationships in a reversible full adder circuit (rd32) made from Toffoli gates

study situations where additional gates are inserted in order to create new invariant relationships.

3. Methodology

An invariant relationship in a circuit happens whenever two sites are expected to hold the same logic value when the circuit is free of errors. Identifying any violation of these invariants could then be used as a means of error detection for the circuit. As an example, consider the CNOT circuit description of a full adder circuit (rd32) Figure 3a). It can be verified that whenever wire \( a \) contains 0 or 1 at the input, the output logic value will always be 0 or 1. If this relationship does not hold, an error must have occurred in the intervening logic between the two sites or at the second site. These type of implications that naturally occur in the un-modified reversible circuit we call them natural implications. Due to the synthesis rules outlined above, in reversible logic these invariant relationships can only be implemented at the input/output level. These synthesis rules constraint the number, and quality, of natural invariant relationships in the circuit. One will also notice that with the addition of extra reversible gates one can force the additional creation of invariant relationships. For example, as shown in Figure 3b), when we append a 2x2 Toffoli gate to the unmodified rd32 circuit, with the function \((p, q) \rightarrow (p, p \oplus q)\), we artificially generate another invariant relationship, \((b = 0/1) \implies (q = 0/1)\). To this type of artificially created logic invariant relationships we call them artificial implications. It is important to mention that these artificial implications, can only be placed in locations whose logic output is functionally irrelevant (garbage outputs), as they alter the values of the function we are trying to compute. The biggest advantage to these artificial implications is that, previously useless states now have the purpose of providing circuit fault tolerance.

The procedure to find both natural and artificial implications is as follows. After choosing a reversible circuit, we run circuit simulation and record the logic
testgate ← any reversible gate

for each garbage wire permutation do
  - place testgate on wire permutation
  - run circuit simulation
  - check for artificial implications
end for

Figure 4: Exhaustive search algorithm to find artificial implications

state of all output nodes for each input vector applied. In order to avoid potential sampling situations associated with random (or ATPG) vectors simulation, we use all possible combinations of inputs vectors. For this project, the used circuit simulation tool, BRevSim [2], was custom made as none of the existing publicly available simulators [27, 15], was open-source, supported complex reversible gates or performed fault coverage. Once the simulation is complete, we identify in-variate relationships by comparing node pair values in the simulation runs. For instance, for the \((a = 1) \implies (b = 1)\) relationship to exist, there should never be an instance where \(a = 1\) and \(b = 0\). Since we are exhaustively running all input vectors, we do not need a more formal method to verify that these invariant relationships are valid. With the location of these invariant relationships we have found the natural implications.

To create the artificial implications, first we need to assert which of the circuit wires will contain garbage outputs. Then we need to determine the possibility of appending any reversible gate, in order to establish a new invariant relationship, without altering any non-garbage output logic states. This is accomplished by repeating the same steps used to find natural implications with random reversible gates being inserted on all permutations of garbage wires. This algorithm is shown on figure 4. In our work we only used the four common logic gates listed in figure 4, but theoretically any reversible gate could be used.

Also, in our model we do not allow the attached gate to be in any non-garbage producing wire, even if the output for that particular line is not modified. In the Toffoli Gate outlined on Figure 4, we can see that in the first wire, the output and input value of the gate remain unchanged, therefore we could technically allow that particular wire to be on a non-garbage output. However we chose not to do so. The reason being that any inserted gate has the potential to fail, and a failure in a garbage wire will be of no consequence, while a failure elsewhere could be catastrophic.

Once we’ve determined the natural and artificial implications, we performed fault simulation in order to assert the impact of each invariant relationships. We would like to know, for example, how many reversible faulty components could theoretically be detected by our implications. Similar to the work in [18], we would like an invariant relationship to be able to detect as many faults in the circuit as possible. The reversible fault model used in this work is the reversible implementation stuck-at-0/stuck-at-1 outlined in existing work [22]. The model suggests the insertion of a fault on every wire before each gate, even if a particular wire does not impact the outcome of the reversible gate. According to this model, the total number of faults for a given circuit is \(\text{number of gates} \times \text{number of wires} \times 2\). With this model,
### Table 1: Characteristics of the reversible of benchmarks used on our simulations

| Benchmark      | # gates | # wires | # garbage | Source |
|----------------|---------|---------|-----------|--------|
| rd32           | 4       | 4       | 2         | 15     |
| rd53-130       | 30      | 7       | 4         | 27     |
| rd84-143       | 21      | 15      | 11        | 27     |
| sym6-145       | 36      | 7       | 6         | 27     |
| 4gt4-v0-73     | 17      | 5       | 4         | 27     |
| alu-v4-6       | 7       | 5       | 4         | 27     |
| 9symd2         | 28      | 12      | 11        | 15     |
| ckt1-149       | 11553   | 9       | 0         | 27     |
| ham7-25-49     | 25      | 7       | 6         | 15     |
| hwb6-56        | 126     | 6       | 0         | 27     |

The circuit rd32 listed on figure 3 has 32 faults, half of them being stuck-at-zero. The degree of accurateness of this fault model is beyond the scope of this work. Considering that no reversible circuit has been produced, there can be no consensus whether this fault model is less accurate than other proposed reversible fault models [29, 20]. We opted for this fault model, because we had to choose one, and this particular one would generate an excess of faults guaranteeing good stress test to our reversible circuit simulation platform.

It is also beyond the scope of this project the implementation, or conception, of the hardware required to assert the validity of each implication during circuit run-time.

### 4. Results

On table 1 we list the selected reversible benchmarks to be used on our analysis. Unfortunately most of the available benchmark circuits are either very small or they have a strong predilection to being synthesized with Toffoli gates. In the same table, the number of wires correspond to the number of input/output, and the number of garbage correspond to the number of the number of those wires whose logic value is irrelevant on the circuit.

Table 2 contains the number of discovered natural and artificial implications. A quick glimpse at the table shows us that there are very few natural implications for larger and more complex circuits with no garbage outputs, such as hwb6-56 or ckt1-149. In fact, except for ham7-25-49 there is a visible relationship between the number of garbage outputs and the detected implications. We then looked individually at each natural implication detected, and we noticed that every single one of them existed due to a wire whose logic value was never altered, the same behaviour outlined on figure 3a). This result was disheartening as during the conception of this work we were expecting to find more complex implications. The detection of artificial implications was also extremely disappointing. Even with exhaustive search, the only circuit, besides the already studied rd32, that gave us some new artificial implications was 9symd2. Unfortunately every single one of artificial implications was generated due to a trivial addition of a 2x2 Toffoli gate, the same type of artificial implication described on figure 3b). The other circuits did
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\( testImplication \leftarrow \text{any valid implication} \)
\( errorDetected \leftarrow 0 \)
\( errorMissed \leftarrow 0 \)

\[ \text{for each input vector do} \]
\[ \text{for each fault do} \]
\[ \quad \text{if } TestImplication \text{ was violated } \land \text{ error was propagated to output then} \]
\[ \quad \quad errorDetected \leftarrow errorDetected + + \]
\[ \quad \text{end if} \]
\[ \quad \text{if } TestImplication \text{ was NOT violated } \land \text{ error was propagated to output then} \]
\[ \quad \quad errorMissed \leftarrow errorMissed + + \]
\[ \quad \text{end if} \]
\[ \text{end for} \]
\[ \text{end for} \]

\[ implicationImpact \leftarrow \frac{errorDetected}{errorMissed + errorDetected} \times 100 \]

Figure 5: Algorithm that calculates the implication impact

not yield any new implications either because there were no more new implications to detect, or not enough garbage wires.

Despite these poor results, we were still curious about the fault coverage impact of each individual implication on the overall circuit. To the proposed metric we call *implication impact* and it is the ratio between the number of faults detected at the output that caused an implication to be violated and the number of faults that were detected at the output. The algorithm for metric is described in Figure 5, and obviously the higher the implication impact the better. A 55% implication impact would tell us that a particular implication can be expected to detect faults that propagated to the output, an estimated 55% of the times.

| benchmark  | natural implications | artificial implications |
|------------|----------------------|------------------------|
|            | number | avg. impact | number | avg. impact |
| rd32       | 1      | 12.5        | 1      | 18.75      |
| rd53-130   | 3      | 7.14        | 0      | 0          |
| rd84-143   | 1      | 0           | 0      | 0          |
| sym6-145   | 5      | 5.12        | 0      | 0          |
| 4gt4-v0-73 | 0      | 0           | 0      | 0          |
| alu-v4-6   | 1      | 10          | 0      | 0          |
| 9synd2     | 2      | 8.2         | 7      | 22.5       |
| ckt1-149   | 0      | 0           | 0      | 0          |
| ham7-25-49 | 0      | 0           | 0      | 0          |
| hwb6-56    | 0      | 0           | 0      | 0          |

Table 2: Number of different type of implications and their impact

As it can be seen on table 2 not only we have very little implications, but these also have very little overall impact. The results were so poor that we did not see
the need to run a circuit simulation with every single detected implication. One point worth noting is that the average impact of the detected *artificial implications* is greater than the average impact of the *natural implications*, that is mainly due to the fact that we added an extra gate at the output which allowed us to detect more faults. It is worth noting that rd84 only has one detected implication with a 0% impact. This indicated that all the faults that could be detected by the implication circuitry are the faults that are not propagated to the output.

Finally, in terms of computational performance, our experiments have shown the small size of the benchmark reversible circuits, performing an exhaustive input vector simulation took a negligible time. For a sample circuit with 10 input lines and 50 gates, circuit simulation in *BRevSim* takes less than 1 second on a Dual Core 2GHz 2007 MacBook computer.

5. Conclusions

The purpose of this paper was to assert if invariant relationship were also viable for online error detection in reversible circuits. Our results show that unlike non reversible circuits, the implication concept is ineffective. We observed that when implications are naturally present in the reversible circuit they tend to be very simple in nature, occurring due to wires with unchanged logic states. These uninteresting implications obviously cover few faults. When we recursively searched for *artificial implications*, we found that they rarely existed, even with exhaustive search mechanisms. When these exist, these were trivial in nature. In conclusion, our simulations on a small subset of reversible benchmarks, strongly indicate that implications are not suited for reversible circuits.

6. Future Work

One of the positive outcomes of this paper is that a reversible circuit simulation capable of fault analysis was released as an open source project. With it several extensions to this paper can be researched, one example being the investigation of reversible logic synthesis algorithms so that unavoidable garbage outputs, should contain logic implications. Another potential research area direction consist on actually designing the hardware that detects the violations of the invariant relationships.

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