ABSTRACT

This paper proposes RCP, a new reversible coherence protocol that ensures invisible speculative load execution (ISE) with low overhead. RCP can be combined with processor mechanisms that eliminate the effects of speculative instructions on other instructions to achieve low overhead invisible speculative execution (ISE). ISE provides protection that is at least as strong as speculative privacy tracking (SPT) and stronger than speculative taint tracking (STT). RCP is designed by systematically extending the existing coherence protocol to incorporate speculative loads and states. The protocol is implemented in Gem5 and verified with Murphi. The results show that RCP based ISE incurs lower overhead than STT/SDO/SPT while providing similar/stronger protection.

1. INTRODUCTION

As Spectre [15], Meltdown [19] and other attacks demonstrated, modern processor architectures based on speculation are facing major security issues. These attacks exploit speculative execution to modify or leave traces in the cache hierarchy, and extract secrets using side-channels. With several years of intensive research, various kinds of vulnerabilities are identified. It is critical that the defense mechanisms are able to provide comprehensive protection.

Figure 1 shows four typical attacks. For the basic attack (a), an attacker can exploit branch misprediction to leak secret (or arbitrary memory) via the data cache. It first primes the branch to predict that the condition is true by making the code repeatedly run with valid value of i. Then the attacker provides an out-of-bound value for i and the processor (mis)predicts that the condition is still true and speculatively loads out-of-bound data depending on the secret. Once the processor resolves the misprediction, it rolls back execution but the data accessed persists in cache. The secret can be extracted by common techniques, e.g., Flush+Reload, that exploit the cache side-channel vulnerabilities.

Figure 1 (b) and (c) show two advanced speculative interference attacks [3]. In (b), the non-speculative load(A) is not ready to execute and the processor executes the speculative instructions after the branch. If the secret is 1, the sequence of loads will occupy all MSHR entries. When load(A) is ready, it will be delayed until the branch is resolved because there is no available MSHR entry. If the secret is 0, all speculative loads only occupy one MSHR entry since they access the same address, and load(A) can be issued without delay. In (c), if secret is 1, the load (line 4) will miss, and the execution of the following dependent speculative instructions will be delayed until the branch is resolved. If secret is 0, the load hits in cache, the following instructions will be dispatched, and the target instruction is executed after the branch is resolved.

Speculative execution is an important performance enhancing technique used in all commercial processors. The architects understood the needs and mechanisms for rolling back the execution and recovering the architectural (processor) states when the speculative execution is squashed. However, no systematic mechanisms are in place to reverse the state changes due to speculative execution in cache hierarchy. We believe that it is one of the crucial causes (but not all) of the speculative attacks. The goal of the paper is to close this gap. We first briefly review the existing defense schemes.

ISE: incomplete solution focusing on cache. Early mitigation mechanisms [2, 13, 23, 24, 30] focused on invisible speculative load execution (ISE), i.e., ensuring that the executed but then squashed speculative loads do not leave trace in cache hierarchy. Although ISLE can defend specific attacks such as Spectre similar to the basic attack in Figure 1 (a), it cannot provide comprehensive protection since it does not consider other speculative instructions. Thus, it cannot defend speculative interference attacks in Figure 1 (b) and

Figure 1: Speculative Execution Attacks

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A straightforward modification is to treat all accessed data as secrets, taint them, and block the dependent speculative execution. But it will likely block most speculative execution, making the performance unattractive. Speculative Privacy Tracking (SPT) [8] reuses the taint tracking mechanisms in STT and achieves lower overheads by not blocking a speculative secret transmitter if the secret is already transmitted non-speculatively. With SPT, the speculative transmission instruction in Figure 1 (e) is not blocked. Nevertheless, SPT still blocks more speculative execution than STT, and introduces even higher overheads (45% vs. 14.5%).

Our approach: **processor-stall+ISE with reversible coherence protocol.** Based on the discussion so far, neither ISLE nor processor-stall based solutions is optimal: ISLE is not comprehensive while STT/SDO/SPT incur higher overheads. In this paper, we take a hybrid approach: minimally stalling the processor to eliminate the interference of speculative execution on other instructions; and designing a correct and low-overhead reversible cache coherence protocol for ISLE. This approach is inspired by [3], which demonstrated the insufficient protection of ISLE, and proposed additional processor mechanisms for eliminating the effects of speculative instructions on other instructions.

We call this approach as Invisible Speculative Execution (ISE). According to [3], ISE provides two strong security properties:

- **ISE-SP1**: the set of instructions committed and their timing should not be influenced by speculative execution;
- **ISE-SP2**: the time for squashing a set of instructions should not depend on speculatively accessed data.

The two properties can be realized by enforcing three requirements with implementation mechanisms:

- **ISE**: it ensures the security properties ISE-SP1 and ISE-SP2 for speculative loads. We achieve this goal by proposing the systematically designed Reversible Coherence Protocol (RCP) with low overhead;
- **ISE-P1**: “no instruction ever influences the execution time of an older instruction” [3]; and
- **ISE-P2**: “any resources allocated to an instruction at the interface of the frontend and the execution engine are not deallocated until the instruction becomes non-speculative” [3].

ISE-P1 and ISE-P2 ensure ISE-SP1 and ISE-SP2 for speculative non-load instructions. In a nutshell, the relationship between ISE and ISLE is:

\[
ISE = ISE-P1 + ISE-P2 + ISLE
\]

We do not claim the processor policies ISE-P1 and ISE-P2, or the general ISE approach as our contribution since...
they were outlined in [3]. The key contribution of the paper is the novel coherence protocol to implement ISLE.

ISE can defend the speculative interference attacks. For Figure 1 (b), ISE-P1 ensures that an occupied MSHR entry for a speculative load is released and allocated for Load(A) when it is ready to execute. This can be implemented by pre-emption mechanism. For Figure 1 (c), ISE-P2 ensures that, even the speculative instructions (the many additions) can finish execution faster if (secret=0), their RS entries cannot be deallocated until the branch is resolved. ISE—oblivious to the source of the dependent secret—provides stronger protection than STT/SDO and prevents attacks in Figure 1 (d).

Relation to alternative ISE schemes: Figure 2 show the relations between ISE and all existing solutions. Unlike the early ISLE schemes, ISE provides comprehensive protection—even stronger than STT/SDO and similar to SPT. There are two alternative ISE schemes. GhostMinion [1] rephrases ISE-SP1 as “Strictness Ordering” and ISE-P1 as “Temporal Ordering”, which is the basis of its implementation. However, it does not correctly implement ISE for two reasons: (1) it does not enforce ISE-P2 therefore cannot defend the attack in Figure 1 (c); and (2) it uses MuonTrap [2] as the mechanism for ISLE, which is not fully correct based on the security properties in Section 3. Dolma [20] adopts processor mechanisms similar to ISE-P1 and ISE-P2 to ensure transient non-observability by STT-like speculative information flow tracking. Dolma uses Delay On Miss (DOM) to support ISLE, which allows speculative execution if the instruction hits in L1 and delays that on miss. Our results show that DOM incurs higher overheads than RCP, which can be also applied to Dolma. Thanks to RCP, our ISE scheme incurs low overhead than STT/SDO/SPT while providing similar or stronger protection.

Key insights of RCP: To design RCP, we take a principled approach, and show that it can be done by extending the existing coherence protocol in a systematic manner. The key property of RCP is: when an unsafe speculative load is squashed, it should be as if it is not executed; when it is later committed, it should behave like a normal load in the ordinary coherence protocol. The second part of the property is interesting: it is not a correctness property but merely a design choice. Invisispec [30] and DOM [24] satisfy this with high overhead, while MuonTrap [2] does not satisfy this, i.e., a safe speculative load can behave different than a normal load, but still correct. We demonstrate the design of RCP by extending MESI protocol for two level caches (private L1 and shared L2) as shown in Figure 3 (a). The complexity of RCP is relatively high, but our implementation in a simulator is fully functional and can run comprehensive benchmarks to completion. We are confident that our implementation can be used as an initial reference design when the protocol is adopted in a real implementation. We will also make our code publicly available. Specifically, RCP is developed based on the following key insights, which can be also applied to designs based on other protocols and cache organizations.

- Introducing new requests and messages for speculative load. RCP introduces three new operations in the interface between processor and cache coherence, and allow them to participate in coherence operations: (1) speculative load SpedRd; (2) PrMerge, which is performed when a speculative load becomes safe; and (3) PrPurge, which is performed when a speculative load is squashed. They lead to additional messages: (a) GetSpec, the forwarded speculative load request to the owner; (b) L1Merge, the message from L1 to L2 and other L1s when a speculative load is merged; and (c) L1Purge, the message from L1 to L2 (but not to other L1s) when a speculative load is purged. The new (in red) and existing (in blue) requests and messages in a two-processor setting are illustrated in Figure 3 (b). In RCP, the transitions for requests other than the speculative load are exactly the same as Figure 3 (a).

- Split-phase state transition. With merge and purge, the state transitions for a speculative load are split into multiple phases. As shown in Figure 3 (c), when a SpecRd is issued, the cache line state X transitions to the corresponding speculative state XSpec. Later, if the SpecRd becomes safe, i.e., PrMerge is received, XSpec transitions to the corresponding non-speculative state; otherwise, i.e., PrPurge is received, XSpec transitions back to X. The key problem is to specify the transitions among speculative states.

- Non-interference of speculative load. In ISLE, a SpecRd should not cause state changes to remote caches since it will incur timing changes. In RCP, when a SpecRd misses in L1, GetSpec is forwarded to the current owner, which just
We also compare the two ISE designs with STT/SDO/SPT.

whether squash has happened due to CleanupSpec's poten-
tially secret dependent squash operations. The recent work [18]
maintained a spec core counter for each cache line indicating the number of speculative copies in L1. This information can be obtained efficiently with counting bloom filter (see Section 4.2). We design the state transitions of RCP in L2 based on the current status of spec core. The insights are shown in Figure 3 (e) and (f), and the detailed transitions are discussed in Section 5.4.

Advantages of RCP. The coherence actions triggered by the merge and purge operations are not in the critical path of the execution and can be performed in the cache hierarchy concurrently with processor execution. It explains why the additional traffic due to merge and purge does not lead to high performance overhead. In our results, even with certain traffic overheads than InvisiSpec, the performance overheads of RCP is lower. Importantly, the requests and messages related to ordinary loads/stores and speculative load are handled by RCP in a unified manner. It means that RCP is not likely to leak side-channel information on when speculative loads become safe or when squashes happen. The recent work [18] indeed showed the possibility of leaking the information on whether squash has happened due to CleanupSpec’s potentially secret dependent squash operations.

Evaluation highlights. We implemented RCP in Gem5 [5]. The correctness is verified using Murphi model checking tool [10]. We compare the overheads in two scenarios: (1) using RCP for ISLE, comparing to InvisiSpec, CleanupSpec and DOM; (2) using RCP as the ISLE mechanism for ISE (ISE-RCP), comparing to using InvisiSpec for ISLE (ISE-IS). We also compare the two ISE designs with STT/SDO/SPT. Both ISE-RCP and ISE-IS offer stronger security property than STT/SDO, and comparable property to SPT. For (1), our results show that RCP incurs slowdown of (7.7%, 7.4%) on (SPEC2017.PARSEC) under TSO, lower than (12.6%, 18.3%) for InvisiSpec, (9.3%, 24.2%) for CleanupSpec. DOM incurs considerably higher overheads compared to others. For (2), we show that ISE-RCP incurs slowdown of (8.4%, 11%) on (SPEC2017.PARSEC) under TSO, lower than (12.7%, 18.7%) for ISE-IS. The results under RC show similar trends. SSD and SDO incurs (22.5%, 32.2%), (10.9%, 15.1%) overheads on (SPEC2017.PARSEC), respectively; while SPT incurs much higher slowdown ~ 48.5% on SPEC2017. We observe that the overheads due to processor mechanisms to prohibit interference from speculative instructions is very low.

2. BACKGROUND

2.1 Out-of-Order Execution

Modern processors perform speculative out-of-order execution to exploit instruction level parallelism. Recent studies [16, 19] revealed that the secret-dependent speculative execution can cause irreversible state changes or data movements (e.g., left the speculatively accessed cache block in L1 cache) that can lead to a covert channels. It is because the speculative load is secret-dependent.

2.2 Threat Model

We focus on defending transient attacks enabled by speculative instructions, rather than speculative loads. We assume the SameThread and Cross-Core models and do not consider simultaneous multithreading (SMT), which can be prevented by recent techniques such as adding defense on context switches [2] or making the cache way-partitioned to avoid SMT-side channels [23]. Similar to all existing works [23, 30, 31, 32], we do not consider speculative stores. In a typical design, a store buffer sits between processor and L1 cache, and a store starts performing—sending invalidations—after it is retired from reorder buffer (ROB) and inserted to the store buffer. Thus, SpectrePrime and MeltdownPrime [27] which leverage speculative stores are out-of-scope. Our evaluation implements a processor model which does not send invalidations until instruction retirement. The recent papers [9, 14, 22] proposed a new Spectre variant which exploits the micro-op cache at the frontends to create the new timing side-channel. This vulnerability can be mitigated by delaying the update of micro-op cache until the micro-op eventually commits. This variants of spectre attacks are also out-of-scope. We assume that attackers can measure the latency of loads and stores, but cannot measure the latency change due to increased coherence traffic. It is implicitly assumed by existing ISLE schemes since they all incur additional traffic. Specifically, additional traffic is generated for correctly speculated loads in InvisiSpec, due to the redo operation; and MuonTrap, due to additional operation to ensure the consistency of coherence states, e.g., asynchronous upgrades in Figure 4. It is generated for incorrectly speculated loads in CleanupSpec for the undo operation. In comparison, RCP generates traffic for both correctly speculated and squashed speculative loads. We acknowledge that the additional traffic may be explored as a side-channel but no such attack has been demonstrated. Also, it is a potential vulnerability for all schemes. In fact, RCP may leak less information compared to others since the traffic is incurred for all speculatively executed loads.

Our threat model includes the attacks that change the timing of committed instructions before or after mis-speculation, such as SpectreRewind [12] and Speculative Interference [3]. During mis-speculation duration, depending on the secret, different sequences of speculative instructions are executed—putting different pressure on non-speculative instructions before or after mis-speculation duration.

2.3 Existing Defense Schemes
ISLE schemes. InvisiSpec [30] issues a speculative load without affecting cache states and a second load when it becomes safe, which will change cache state and leave trace in cache hierarchy. Sakalis et al. [24,26] delays speculative load on L1 miss (DOM) and avoids processor stall by value prediction. A speculative load does not change the coherence states when missing in the L1 cache. DOM is simple solution, but our results show that it incurs considerably higher overheads than InvisiSpec. CleanupSpec [23] is an undo approach with low overheads. On mis-speculation, besides squashing execution effects within the processor, the cache system performs cleanup operations to invalidate or roll back to the state before the mis-speculation. MuonTrap [2] introduces an L0 filter cache and restrict coherence operations to limit speculative changes to a small region. Later, we show that CleanupSpec does not correctly implement ISLE.

Processor-stall based schemes. STT/SDO [31,32] tracks speculative accessed data and blocks secret-dependent execution. SPT [8] blocks speculative transmission of non-speculatively accessed secret only if it is not transmitted non-speculatively.

Pattern-based Schemes: Conditional speculation [24] defines security dependency and stalls speculative execution based on the patterns. SpecCFI [17] performs static analysis on control flow graph to prevent the malicious indirect branch.

3. ISLE SECURITY PROPERTIES

3.1 Definitions

A speculative load (SpecRd) has three key points during its execution: 1) Issue point (I): when it is ready to be issued speculatively; 2) Non-speculative point (NS): when it is no longer speculative, either becoming safe or squashed; and 3) Globally perform point (G): when all effects of SpecRd are finalized—either becoming a part of system state (if it becomes safe at NS), or completely cleared (if it is squashed at NS)—and the write which produces the read value has been globally performed. We assume atomic writes, so that G for write is well-defined. Non-atomic writes issues are discussed in Section 6. [I,G] is called pending period. If a SpecRd becomes safe and committed (denoted as a property S for each SpecRd), we have SpecRd[S] = true, otherwise SpecRd[C] = false.

We consider two “effects” of a SpecRd: 1) locations of the cache line A after G, defined as a function L[A]; and 2) states of the cache line after G, defined as a function S[A]. Each L[A] is a bit vector e₁, ..., eₘ, where m is the number of private caches in level i; or a bit eᵢ when the level i is shared. Each eᵢ, j ∈ {1, ..., m} or eᵢ indicates whether the cache line resides in the corresponding cache. L[A] is a concatenated bit vector indicating present information of a cache line among cache components in all levels. For S[A], eᵢ,j or eᵢ; are replaced with sᵢ,j or sᵢ, which indicates the cache line state. If the pending period of a ∈ {Rd, Wr} is not overlapped with any other accesses’ pending periods, L([Z,a][A] and S([Z,a][A] define the locations and states of the cache line containing address A after Gᵢ, starting from the initial locations Z and F before the execution of a.

To capture the effects of a number of concurrent accesses (a₁, ..., aₙ), aᵢ ∈ {Rd, Wr}, L([Z,a₁, ..., aₙ][Gₙ, max][A] and S([Z,a₁, ..., aₙ][Gₙ, max][A]) specify the locations and states of the cache line after all accesses are globally performed serialized with certain total order. Iₘᵢₙ and Gₘᵢₙ are the minimum and maximum I and G among a₁, ..., aₙ. Each access may cause the changes of the locations and states. Assuming the total order is a₁ → a₂ → ... → aₙ, the sequences of the location and state change are [Z,a₁] → [Z,a₂] → ... → [Z,aₙ] and [F,a₁] → [F,a₂] → ... → [F,aₙ]. The transition functions when aᵢ is serialized right after aᵢ₋₁ are: L([F,aᵢ₋₁,aᵢ][A] = [Z,aᵢ] and S([F,aᵢ₋₁,aᵢ][A] = [F,aᵢ].

3.2 Security Property

Property 1: (Non-overlapping) No effects from mis-speculated load. Consider a SpecRd, [Lₘₐₜᵢ[Rd,Gₘₐₜᵢ][A] not overlapped with any other access. If SpecRd[C] = false, the locations and states of the cache line should be equivalent to the execution before SpecRd: L([Z,SpecRd][A] = Lₘᵢₙ[Rd][A] = Lₘᵢₙ[SpecRd][A]) and S([Z,SpecRd][A] = Lₘᵢₙ[Gᵢₙ][A]). The states can be handled similarly by replacing L and L with F and S.

Remark: For the correct speculated load, the same effects as a non-speculative load is not a required security property. A coherence protocol can exhibit different behaviors for non-speculative load and a speculative load that later becomes safe. MuonTrap [2] is one such example.

Property 2: (Overlapping) Serialization of the correct speculated loads. Consider two accesses with overlapping pending period, the first is a speculative load SpecRd, the second is an access acc ∈ {Rd,SpecRd,Wr}. If SpecRd[C] = true, then the two accesses should be correctly serialized. From Property 1, the locations and states of the cache line should be equivalent to the execution that replaces the speculative loads with the corresponding non-speculative load: L((SpecRd,acc)[A] = Lₘᵢₙ[Lₘᵢₙ[SpecRd][A] = Lₘᵢₙ[(SpecRd,acc)[A] = Lₘᵢₙ[Lₘᵢₙ[acc][A]. The states can be handled similarly by replacing L[Rd] and S[SpecRd,acc][A].

Property 3: (Overlapping) No effects to overlapping accesses from mis-speculated loads. If SpecRd[C] = false, the squashed SpecRd should not have any effects on other overlapped accesses: L([Z,(SpecRd,acc)[A] = Lₘᵢₙ[acc][A]. Equation for states is similar.

Corollary: A non-speculative request acc ∈ {Rd,Wr} is not aware of any overlapping speculative SpecRd to the same address before NS point of SpecRd. It can be directly obtained from Property 3. If the execution is affected by SpecRd before its NS point and SpecRd is later squashed, acc may not reach L([Z,acc][A] and S([Z,acc][A].

3.3 Existing ISLE Solutions and RCP

InvisiSpec [30] and DOM [24]: correct with high overhead. They satisfy all security properties by not allowing the speculative load to participate the coherence protocol before NS point.

CleanupSpec [23]: incorrect. Consider a sequence of memory accesses from three processors shown in Figure 4 (a) and (b). P₁ is the victim, P₂ and P₃ are attackers. P₁ is induced to speculatively access a cache line A (but later squashed)
whose address will reveal secret. P2 tries to guess and access a cache line that may be A before P1’s SpecRd is squashed, then and P3 can infer the line by measuring the response latency difference caused by irreversible cache state changes. Specifically, if the guess is wrong, P3 gets the line from C1,2, which gets the forwarded request from C2, since P3 is the first to access the line (Figure 4 (a)); if the guess is correct (both P1 and P2 have accessed the line), P3 will directly get the line from C2 (indicated as the red arrow) with shorter latency since P1 is the first to access the line and P3 has changed it to shared (Figure 4 (b)). Due to different latency, P3 can infer whether the guess is correct, and if so, the line accessed by P1. Our security properties prevent such attack by guaranteeing, even if the line is speculatively accessed by P1, if the load is squashed, P3 should get the line with the same latency as if P1 did not execute the SpecRd. A protocol satisfying these properties will behave in the same way as Figure 4 (a).

CleanupSpec’s behavior for the “correct guess” case is illustrated in Figure 4 (c). CleanupSpec allows the state changes to E in C1,1, when P2 accesses it before P1’s SpecRd is squashed, C1,1 is the one who forwards the line. It is different from the scenario if P1’s SpecRd does not exist, in which P2 should experience a cache miss in both L1 and L2 and get the data from memory. Thus, the SpecRd effects the timing of P2’s request (violation of Property 3). In an attempt to ensure the property, CleanupSpec adds a “dummy latency” by forcing an artificial cache miss in C2, which effectively prevents P2 to sense the latency difference. It ensures Property 3 for SpecRd w.r.t. P2’s request. Later, when P1’s SpecRd is squashed, C1,1 locally invalidates the line. Unfortunately, this operation does not reverse the state change in C2. As a result, when later P3 accesses the cache line, it will get the response from C2 with a shorter latency since it is in shared state (both P1 and P2 have accessed it). But the attacker knows that the latency should be longer—forwarded by C1,2—if P1 had not accessed the line. This example explains that CleanupSpec does not protect such an attack and Property 3 is violated by SpecRd in P1 w.r.t. P3’s request: the mis-speculation in P3 effects the state of the line in C2 (making it shared), which is later inferred by P3 with response latency difference.

MuonTrap [2]: correct with low overhead. It uses an L0 cache to keep the speculatively accessed data in restrictive cases when coherence state changes are not exposed. The basic design degrades an MESI protocol to MSI. To recover the benefit from E state, MuonTrap introduces SE state in L0. A line is brought to L0 as SE by SpecRd when a Rd would have brought it to L1 as E. It “behaves like S to the coherence protocol”, but when the SpecRd is committed, an “asynchronous upgrade” is performed to invalidate the other copies so that the line can be install in L1 as E. Figure 4 (d) shows how the previous example works in MuonTrap. P2 and P3 try to detect whether P1 try has speculatively accessed a cache line. (a) No protection: P1 and P2 guess wrong. (b) No protection: P3 and P1 guess right. (c) CleanupSpec with SpecRd failed to defend. (d) MuonTrap with SpecRd (squash) handles the attack.
an instruction is fetched, it is marked as “unsafe”. When the load is issued, if it becomes safe, then a Rd is generated; otherwise, a SpecRd is issued. The update of VP in a cycle will trigger the merge or purge of sequence of instructions. To purge a sequence of speculative loads, only the PrPurge for the oldest one is sent and all younger ones are squashed together. For merge, only the PrMerge for the the youngest is sent and all older ones will be merged. The recent Pinned Load work [33] proposed optimization to speed-up the advance of the VP to either reduce the stall time in processor-stall based solutions, or allow safe loads to be issued earlier. The idea is applicable to RCP and allows PrMerge to be issued earlier—further reducing the overheads.

To enforce ISE-P1, each instruction is assigned a priority tag based on the program order when inserted into ROB. An older instruction has higher priority than a younger instruction. When an instruction is about to be stalled due to shared resource contention (e.g., MSHR or EU), the incoming instruction’s priority tag is compared to the tags of instructions that have occupied the resource. If some instructions have lower priority, the one with the lowest priority (thus the youngest instruction) is preempted, and will be re-scheduled in the next cycle. To enforce ISE-P2, when an instruction become safe or squashed, the ROB informs instruction queue to deallocate the shared resource allocated to the instruction. Thus, for a squashed instruction, the shared resource is only deallocated when at the square point, but not earlier.

4.2 Speculative Buffer Structure

RCP uses speculative buffer (specBuf) to keep the effects of speculation. Similar to InvisiSpec [30]: there is a one-to-one mapping relation between a processor’s load queue (LQ) entry and a specBuf entry in both L1 and L2. Figure 5 shows the specBuf organization. For a given LQ entry in core(i)—LQ[i, j]—there is a corresponding specBuf entry in L1 cache, SB1L1[i, j], and L2 cache, SB1L2[i, j]. We denote the specBuf of a core(i) in L1 and L2 as SB1L1[i, *] and SB1L2[i, *], respectively. The valid bit indicates whether the entry is in use—only the LQ entries for speculative loads have valid specBuf entries. The ready bit indicates whether the coherence transactions related to the entry is in transit. The metadata field keeps speculative access information, e.g., the number of accesses performed to the cache line while it is speculative, which is used to update the cache status if the line is merged later. While we indicate SpecData field, it is only used to store the actual data of the cache line if it is not allocated in cache. Thus, there are not frequent data movements between specBuf and cache during merge. Similarly, Coh_State records the coherence state of the line, and is only used when it does not exist in cache. Otherwise, the normal state field in each cache line is used to keep the state. The combined size of all $SB_{1L1}[i, *]$ and $SB_{1L2}[i, *]$ is $2 \times (\# of\ cores) \times (\# of LQ\ entries)$. The number of specBuf entries is the same as InvisiSpec [30].

The additional hardware structure associated with each $SB_{1L2}[i, *]$ is a counting bloom filter (CBF) [11], which approximately records the address set of cache lines that present in each $SB_{1L2}[i, *]$. In CBF, addresses can be both inserted and removed, thus maintaining a dynamic address set. Using bloom filters, the membership check can be done very fast, it can generate false positives but never false negatives. The CBFs in L2’s specBufs are used to maintain spec core information. Since all speculative loads are recorded in specBuf of L2, this can be obtained by checking all $SB_{1L2}[j, *]$, where $j \neq i$. The CBFs associated with each $SB_{1L2}[j, *]$ can reduce the overheads by first performing membership check of the line address with all $CBF_{2}(j \neq i)$, and only performing search if the outcome is positive. To prevent timing side-channels, we make the time to check the CBFs constant.

5. REVERSIBLE COHERENCE PROTOCOL

5.1 Speculative States

Based on the insights discussed in Section 1, each state X transitions to the corresponding speculative state XSpec on SpecRd (in L1) or GetSpec (in L2). The speculative states can transition among each other triggered by non-speculative requests. Table 1 indicates the speculative states and the corresponding status in RCP.

| States | Global Status |
|--------|---------------|
| ISpec | No non-spec copy, one local spec copy |
| ESpec | One non-spec copy (E), one/more spec copies |
| SSpec | Multiple non-spec copies, one/more spec copies |
| MSpec | One non-spec copy (M), one or more spec copies |

Table 1: Speculative States of RCP

5.2 Split-phase State Transition

    Insights Figure 3 (c) shows the insights with the simplistic...
scenario without conflicting accesses. When a SpecRd is issued and the state of the requested cache line is X, it transitions to XSpec (speculative state), where X can be M/E/S/I. After the transition, further SpecRd will not trigger new transitions. Later, if PrMerge is received, XSpec transitions to X (if X is M/E/S) or S/E (if X is I) depending on the whether line is shared. If PrPurge is received, XSpec transitions back to X. In MESI protocol, a load will directly trigger X → X or I → S/E transitions without going through XSpec. With conflicting accesses, XSpec will transition to other speculative states when a non-speculative or a forwarded speculative request accesses the line.

**RCP specification** Figure 6 (a) shows the first phase transition triggered by a speculative load. If the request misses in L1, a GetSpec request is sent to L2, and the transition I → ISpec is triggered by the response of GetSpec. For the other states, SpecRd triggers the transition. In I, it is possible to receive PrMerge or PrPurge because the cache line is invalidated after SpecRd. In these cases, PrMerge or PrPurge are ignored.

Figure 6 (b) shows the second phase transition in L1 from speculative state back to non-speculative state triggered by PrMerge or PrPurge. For PrPurge, XSpec, X ∈ {M,E,S}, will transition to X because L1 still holds a non-speculative copy. For PrMerge on ISpec, an L1Merge is sent to L2 cache. If the line is shared (S), ISpec will transition to S; otherwise (non-S), it will transition to E. While the L1 cache is waiting for the response from L2, it resolves the race condition by NACK-ing all requests to the cache line.

Figure 7 shows the split-phase transitions in L2. In Figure 7 (a), SpecRd missing in L1 triggers a GetSpec. For M/E, SpecRd is forwarded to the current owner. In Figure 7 (b), The counter spec core is increased or decreased when a GetSpec or an L1Merge/L1Purge is received. If spec core = 0 after an L1Purge, meaning that there is no other speculative loads, each XSpec, X ∈ {M,E,S,I}, will transition back to X; otherwise they stay in the same state.

If spec core = 0 after an L1Merge, the speculative state transitions to a non-speculative state as if a GetS is received. For MSpec, it transitions to S since there are more than one shared copies, in addition, L2 forwards an L1Merge to the current owner. For ESpec, it can transition to E or S. The caveat is that the speculative and non-speculative copy can be brought by the same processor. It can be determined by comparing the current non-speculative owner cur_owner with the sender of L1Merge, if they are the same, then ESpec transitions to E. Otherwise, it transitions to S, and L2 also forwards an L1Merge to cur_owner. Note that the cur_owner information already exists in MESI to identify the owner when a line is in M/E in L2. In RCP, cur_owner is updated in two additional cases: 1) a GetS is received in ISpec—a Rd will get the only non-speculative copy of the line in an

**Figure 7: Split-phase State Transition in L2**

**Figure 9: Speculative State Transitions**

L1; or 2) L1Merge is received in ISpec—a speculative copy becomes the only non-speculative copy.

If spec core > 0 after an L1Merge, there are still speculative copies, but there will be state transitions among speculative states based on the number of non-speculative copies. Specifically, MSpec will transition to SSpec, because now we have more than one non-speculative copies plus some speculative copies. For SSpec and ESpec, they will both transition to SSpec, because there are more than one non-speculative copies plus at least one speculative copy. For ISpec, it transitions to ESpec, because we have one non-speculative copy (just merged) and at least one speculative copy.

### 5.3 Non-interference of Speculative Load

**Insights** When a SpecRd misses in L1, GetSpec is forwarded to the current owner, in which the line can be in X or XSpec, where X is M/E. In RCP, a SpecRd does not cause state changes to remote caches since it will incur timing changes. Figure 3 (d) shows this insight: on receiving a GetSpec on X or XSpec (X = M/E) the state is not changed but data is forwarded; when later an L1Merge is forwarded by L2, X transitions to S or SSpec with data flushed to L2. In RCP, PrPurge is never forwarded (thus no L1Purge message) exactly because GetSpec does not cause state transition. In MESI protocol, X will directly transition to S on GetS.

**RCP specification** Figure 8 shows the state transitions that implement non-interference of speculative load, of which the insight is illustrated in Figure 3 (d). In Figure 8 (a), when L1 receives the forwarded GetSpec, the cache line can be in M/E. The owner forwards the data but stays in the same state, otherwise the speculative load will have effects. When a remote SpecRd is merged, the owner L1 cache will receive an L1Merge, which finalizes the transition (the second phase) to S. For M, the dirty line is flushed to L2 cache, which should be performed only when the speculative load becomes safe. In Figure 8 (b), the three speculative states’ transitions are the same as the corresponding non-speculative states that we described above. The only difference is that, there is a pending speculative load from the processor.

### 5.4 Speculative State Transitions
**Insights** RCP needs to answer two questions: (1) what happens when non-speculative requests access cache lines in speculative states; and (2) what happens when L1Merge are L1Purge are received in L2 (shared cache)? Fortunately, the state transitions can be designed by mechanically extending the original MESI protocol. For (1), as indicated in Figure 3 (e), a request will transition XSpec to YSpec, if the same request transitions X to Y. Here X, Y ≠ I and they can be the same state. Moreover, we have XSpec → I corresponding to each of X → I in MESI; and ISpec → XSpec for I → X. The protocol property is that the non-speculative requests trigger state transitions in the same manner as in MESI but among corresponding speculative states.

For question (2), when an L1Purge or L1Merge is received at L2, spec core is decreased; when a getSpec is received, it is increased. As shown in Figure 3 (f), on receiving a GetSpec, XSpec stays in the same state because a speculative load does not further change speculative state, similar to the case in Figure 3 (c). On receiving an L1Purge, if spec core > 0 after the update, XSpec also stays in the same state because there are other speculative copies; if spec core = 0, XSpec transitions to X — reversing back to the non-speculative state. For L1Merge, the transition can be constructed on the transition triggered by GetS in MESI. For each X GetS Y: (1) if spec core > 0, we have XSpec L1Merge YSpec; (2) if spec core = 0, we have XSpec L1Merge YSpec. The insight is: L1Merge, indicating the second phase of a speculative load, will trigger state transitions in the same way as GetS in MESI.

**RCP specification** Figure 9 shows the transitions among speculative states due to non-speculative requests, of which the insight is illustrated in Figure 3 (d). In Figure 9 (a), the key property is that the speculative states can transition among each other by non-speculative requests, and when a PrMerge or PrPurge is received, the state will return to the correct non-speculative states. All speculative states transition to I on receiving an invalidation (GetX or Upgrade), but processor still sends PrMerge or PrPurge for the previous SpecRd that caused the transition to a speculative state. As shown in Figure 6 (a), they should be ignored. The speculative load may be re-issued depending on memory consistency model. More details are discussed in Section 6. In Figure 9 (b) shows the similar speculative state transitions in L2.

### 5.5 Non-Atomic Transactions

In RCP, non-atomic transactions in the original MESI protocol are handled with the existing mechanisms—Nack-ing incoming requests while in transient states. Among speculative states and requests, only transitions related to ISpec may lead to transient period. It happens when transitioning to ISpec or from ISpec to an E/S. In L1, when a SpecRd misses in L1, a GetSpec request is sent to L2 and when the response is received, the state transitions to ISpec. When L1 receives a PrMerge at ISpec, a request is sent to check whether the line is shared or not, then ISpec transitions to E (non-S) or S (S) accordingly. These two cases can be handled by keeping all requests during such transient period and only processing them when the state is stable. We use a bit to indicate that the cache line is in ISpec but it is waiting for the data (I → ISpec) or non-S/S information (ISpec → E/S). When the bit is set, the incoming requests are Nack-ed and processed later. The reason why RCP is mostly not affected by non-atomic transactions is that, the additional states and transitions are introduced to handle only speculative loads, while most complications are due to writes.

A relevant issue is the ordering guarantee of messages in the on-chip network. For RCP, the protocol state transitions related to speculative states and messages, i.e., speculative load, merge, and purge, do not assume the ordering guarantee. For the normal state transitions in the original MESI protocol, we keep the assumption unchanged. In another word, RCP does not add additional message ordering requirement. RCP is designed in a manner that one state can receive different potential messages in any orders, which will lead to different but all correct state transition paths. For example, consider ESPEC in an L1, it can “concurrently”—in any order—receive a forwarded GetSpec and a local PrPurge. In RCP, processing them in either order is correct. If PrPurge is processed first, the state transitions to E, and the cache will forward data as the response to the later GetSpec but stays in E. If GetSpec is processed first, the state is still ESPEC, which will also transition to E when PrPurge is processed.

Finally, we discuss the handling of cache replacement. The protocol state transitions described so far assume that a cache block’s state should eventually transition to a non-speculative state. If a cache block in speculative state needs to be replaced, we simply allow that to happen. It is important to know that, after the replacement, the speculatively loaded data is still in the specBuf. Later, when the speculative load is merged or purged, the request misses in L1 but hits in specBuf, a GetSpec request is sent to the L2. The returned block from L2 has a bit indicating whether the block in L2 is shared (non-speculatively or speculatively). The block is re-inserted in L1 in SSpec if it is shared in L2; otherwise, the state is the same as the state recorded in the specBuf entry. After that, the operations triggered by the merge or purge are applied and the block eventually transitions to a non-speculative state. In this case, the specBuf has the effect of enlarging L1 size, leading to potential speedups. For simplicity, we do not indicate such transition in the protocol specification.

### 5.6 Protocol Verification

We use Murphi [10] to verify our protocol and quantify the complexity of RCP. We model the two-level MESI protocol from GEM5 implementation suite and make it as a baseline. To keep the number of explored states tractable, we use a single address, two data values with private L1 cache and a shared L2 with directory, similar to [7]. With one address, we modeled replacements as unconditional events that can be triggered at any time. The verification explored 3,244,350 reachable states, which is 70% more than MESI, in 1,186 seconds. We verify that the protocol states transitions happen as designed. The verification reaches all speculative states, which can always transition back to NS eventually.

### 6. SECURITY ANALYSIS


We show that RCP satisfies the three properties in Section 3.2 and the additional requirement that for the correct speculated load, the protocol exhibits the same behavior as a non-speculative load (overcapture requirement). For a normal load/store $A$, the serialization point ($S_A$) is the point during its pending period that the access is serialized in the global total order of accesses to this address. With atomic writes, $S_A$ is well-defined. A speculative load $A$ does not have a single serialization point, instead, it has a reach point ($R_A$), indicating the point that it reaches L1/L2; and a merge point ($M_A$) or purge point ($P_A$), indicating the point that it is merged or purged in L1/L2.

**Proof of Property 1 and the overcapture requirement:**
Without overlapping, this property is ensured by design with the split-phase transition. The location property is ensured because a SpecRd installs the cache line to all cache components (specBuf if miss in a component) as if it is a Rd. Depending on purge or merge, the specBuf entry is simply removed or inserted into cache.

**Proof of Property 2 (SpecRd overlaps with load/store):**
We consider all possible behaviors of a non-speculative access $B$ and a speculative load $A$, where $R_A < S_B < P_A$. We have four combinations: (a) $B$ is a load $R_d$ or a store $W_r$, and (b) they are issued from the same or different L1 cache: $C_{1A} = C_{1B}$ or $C_{1A} \neq C_{1B}$. Figure 10 (left) shows that for each case and all possible initial states, the state and location of the cache line (θ) is the same as $B$ is serialized before a non-speculative load $A$ (χ) to the same location; and the timing for the non-speculative access does not change.

Proof of Property 3 (SpecRd overlaps with load/store): In this case, $A$ is squashed so $R_A < S_B < P_A$, and the effects should be equivalent to executing just $B$. Figure 10 (middle) shows such equivalence for all cases.

Proof of Property 2 and 3 (SpecRd overlaps with another SpecRd): Between two SpecRd $A$ and $B$, Figure 10 (right) shows the equivalence: (1) $(A$ and $B$ merge)=($B$ non-speculative loads serialized according to the merge order); 2) $(A$ purges and $B$ merges)=($A$ non-speculative $B$); and 3) $(A$ purges and $B$ purges)=($A$ no load).

Example: Explanation of Case 4 of Property 2. This case assumes Total-Store-Order (TSO) model, which prevents the reordering of loads. When a write ($B$) is serialized before a non-speculative read ($A$) from a different core, the eventual state in $C_{1A}$ and $C_{1B}$ should be $S$ (θ). For $A$, if the line is in $S$ or $I$ ($X = S/I$) in $C_{1A}$ and $C_{1B}$ (the case above dashed line), it must be in $S$ or $I$ in $C_2$. So $R_A$ will transition from $X$ to $X_{Spec}$, $C_{1B}$ is not affected. When $B$ is serialized ($S_B$), the line in $C_{1B}$ and $C_2$ both transition to $M$. In $C_{1A}$, it is invalidation. At this point, MCM matters: in TSO, if a load cache line is invalided before the load retires from the processor, it has to be “replayed”. It is the “Peekaboo” problem discussed in [25]. The replay is needed because otherwise, the load might be reordered with an earlier load—prohibited by TSO. Thus, the SpecRd is re-issued to $C_{1A}$, first reaching $ISpec$ ($C_2$ transitions from $M$ to MSpec), and finally reaching $S$ on merge in both $C_{1A}$ and $C_2$.

If the cache line is already in an exclusive state in the write $B$’s cache $C_{1B}$ ($X = M/E$ shown below dashed line), it must be $I$ in the SpecRd’s cache $C_{1A}$. At $R_A$, SpecRd misses in $C_{1A}$ and $C_2$ forwards it to $C_{1B}$. RCP provides the data but $M/E$ state does not changes (emphasized in red). At $C_{1A}$, $R_A$ changes the state to $ISpec$. After that, when the write is performed ($S_B$), it can still hit in $C_{1B}$—not affected by SpecRd. When SpecRd is merged, the state in both $C_{1A}$ and $C_2$ transitions to $M$. In both cases ($X = S/I$ or $X = M/E$), final state and location of the cache line are the same as $\Theta$.

RCP and memory consistency models (MCMs). We also use the earlier case to show RCP works with release consistency (RC). In RC, since loads to different locations can be reordered, even if a load cache line is invalided before it retires from the processor, the load do not need to be replayed. In this case, for the final state in $C_{1B}$, $C_{1A}$, and $C_2$ are $I$, $I$, $M$, respectively. However, it is not inconsistent with the θ, because, without the load replay, the read $B$ is essentially serialized before the write $A$ ($R_d \rightarrow W_r$), and the eventual states are the same. In RC, without load replay, it is not possible to have $W_r \rightarrow R_d$.

Non-atomic Writes. RCP works with processors (e.g., IBM PowerPC) that do not enforce write atomicity, i.e., stores are visible to different cores at different time. RCP supports invisible speculative load, which only interacts with stores when it is invalidated. Even with non-atomic writes, the write performance w.r.t. individual load is always well-defined.

Since coherence and MCM are interlinked [21], RCP needs to be sufficient to support correct synchronization. Consider the WRC litmus test [28]: [C0: St x 1; C1: Ld x 1; St y 1; C2: Ld y 1; Ld x 0]. With non-atomic writes, such unintuitive behavior is possible since the write from C0 is performed w.r.t. C1 before C2. To achieve the desired behavior, e.g., ensuring the load in C2 returns 1, fences need to be cumulative, which enforce ordering between instructions across cores. In this case, the cumulative fence should be inserted between the two instructions in C1, and forces the write to perform only after the read from x is globally performed. Implementing such semantics requires C0 to collect all invalidation acknowledgments (from both C1 and C2) and then notify C1 so that it can perform the write to y. In RCP, as in MESI, an acknowledgement is sent after the cache line is invalidated. Moreover, invalidation does not affect speculative state change: the line always transitions to $I$, no matter it was in NSS or SS. Thus, we believe RCP is not affected by non-atomic writes and can correctly implement the necessary synchronizations.

Whole-program Proof Sketch: All proofs consider two instructions, but the security property of the whole program can be inductively obtained. Specifically, we can consider the two-instruction case as the initial case in mathematical induction, then we can assume that these properties hold with a sequence less than $n$ instructions, we need to prove they are true with $(n + 1)$ instructions. The crux of the argument is that, the first $(n - 1)$ instructions satisfy the properties (inductive assumption), and they will produce a state and location setting denoted by $\mathcal{S}_{n-1}$ and $\mathcal{L}_{n-1}$ satisfying the properties. Then the last two instructions execute from $\mathcal{S}_{n-1}$ to $\mathcal{L}_{n-1}$, preserving the properties based on our proof.

Security of SpecBuf. We show that specBuf cannot be used to create new channels. Referring to Section 4.2, there is a one-to-one mapping between a core’s LQ entry, $LQ[i, j]$, to specBuf entries in L1 $SB_{1L}[i, j]$ and L2 $SB_{2L}[i, j]$. There is no fully associative or set-associative hardware structures, thus it is not vulnerable to cache-based side-channel attacks such as Prime+Probe. In fact, the specBuf organization is exactly the same as InvisiSpec—with the same number of entries—expect the bloom filters in L2’s specBuf and some counters for each entry. In RCP, we make the time to check the bloom filter in L2 constant, so the present/absence information in the specBuf cannot be revealed through the time for the check.

Case Study. In Figure 4 (f), consider the case that the probed address from $P_2$ and $P_3$ is the same as SpecRd (correct guess). The key observation is that while $P_1$’s SpecRd causes state transitions at L1 and L2, when $P_2$’s Rd is performed, it behaves as if SpecRd does not exist, both in terms of state ($I \rightarrow E$) and latency (miss in both L1 and L2). When SpecRd is squashed, RCP reverses the state in L1 and L2. Later $P_3$’s Rd get the line forwarded by $P_2$’s cache, exactly the same as in Figure 4 (a) when the guess is wrong. RCP prevents the attack and the final states and locations of the cache line are the same as if only Rd from $P_2$ and $P_3$ are performed.

Figure 4 (g) shows the execution when $P_1$’s SpecRd is committed after $P_3$’s access. When SpecRd in $P_1$ commits,
Table 2: Architecture Configurations

| Architecture | Core | Private L1-I | Private L1-D | Shared L2 | Network | Coherence | DRAM |
|--------------|------|--------------|--------------|-----------|---------|-----------|------|
|              | 1 core (SPEC) or 4 cores (PARSEC) at 2.0GHz | 8-issue, OOO, no SMT, 32 LSQ entries, 192 ROB, Tournament Branch Pred., 4096 BTB, 16 RAS | 4KB, 64B line, 4-way, 1 cycle RT lat., 1 port | 64KB, 64B line, 8-way, 1 cycle RT lat., 3 ports | 4x2 mesh, 128b link width, 1 cycle per hop | RCP and MESI | RT latency: 50 ns after L2 |

7. EVALUATION

7.1 Environment Setup

We implemented RCP and various ISE in GEM5 [5]. To evaluate ISLE, we compare RCP with of Invisispec (corrected), CleanupSpec using their public open source codes, MuonTrap. For Invisispec, we evaluate Futuristic model. For CleanupSpec, we evaluate the scheme for Cleanup_SPEC_L1L2. To evaluate ISE, we use RCP and Invisispec together with processor mechanisms described in Section 4.1, they are named ISE-RCP and ISE-IS. We compare the performance of ISE with STT, SDO and SPT under the same framework. The simulator configuration is shown in Table 2. For all experiments, we use the x86 ISA, while some previous papers used ARM ISA, this may lead to different performance overhead than reported in these papers.

We use SPEC CPU2017 [6] for single-core evaluation, and PARSEC 2.1 [4] for multi-core evaluation. For SPEC CPU2017, we run 19 workloads in intrate and fprate suits with reference input size. We forward execution by 10 billion instructions and simulate 1 billion instructions. For PARSEC, we run 9 of the multi-threaded (4 cores) workload with the simmduced input size. We test two different memory consistency model, RC and TSO for SPEC2017; and only show the results of TSO for PARSEC due to the space limitation.

7.2 Performance Analysis

Figure 11 shows single core performance overheads of (1) ISLE: RCP, Invisispec, CleanupSpec, Muontrap and DOM; (2) ISE: ISE-RCP and ISE-IS; and (3) STT, SDO, SPT on SPEC2017 under TSO and RC, normalized to a non-secure baseline. We observe that both TSO and RC share a similar trend of performance overheads. Overall, TSO incurs slightly lower overheads. Some of the benchmarks failed to run for CleanupSpec (e.g., mcf_r and cactusBSSN_r) and STT (x264_r), we leave a blank bar for these cases. Figure 12 shows the multicore performance overheads under TSO. The results under RC show similar trends.

**ISLE Overheads.** Under TSO, RCP incurs an average slowdown of 7.7%, while CleanupSpec, Muontrap and Invisispec incur average slowdowns of 9.3%, 7.6% and 12.6%, respectively. Under RC, the trends are similar, the slowdown of RCP, CleanupSpec, Muontrap and Invisispec are 8.3%, 9.4%, 7.7% and 12%, respectively. For PARSEC, RCP, CleanupSpec and Invisispec incurs 7.4%, 24.2% and 18.3% slowdown on average, while Muontrap achieve 4% speedup. This speedup is due to the filter L0 cache on top of the two level cache hierarchy. The DOM incurs much higher slowdown about 37.1% and 38.4% under TSO and RC. It can be reduced with further optimizations [26]. Due to the larger gap, we exclude DOM in the comparison.

RCP incurs lower overheads because it neither issues the second load nor stalls the processor during squash. The overheads of RCP are mainly caused by the increased traffic due to merge/purge operations. Depending on mis-speculation rates, RCP is not always better than Invisispec and CleanupSpec. Overall, CleanupSpec incurs lower overheads with lower mis-prediction rate. RCP is less sensitive to mis-prediction rate since the merge/purge operations can be performed concurrently with execution. For example, lbm_r has an extremely low mis-prediction rate (0.36%). RCP has negligible slowdown and CleanupSpec even has a decent speedup. By design, CleanupSpec should never lead to speedups. A probable reason is that some codes of Invisispec were not completely removed (CleanupSpec is modified from Invisispec). Overall, for both RC and TSO, RCP incurs the lowest overheads.

**ISE Overheads.** Under TSO, ISE-RCP and ISE-IS incur on average (8.4%,11%) and (12.7%,18.7%) on (SPEC2017, PARSEC), respectively. Under RC, ISE-RCP and ISE-IS incurs on average 9.5% and 13.5%, which is slightly higher than TSO. The additional overheads to ensure ISE-P1 and ISE-P2 are only (0.7%,3.6%) based on RCP, and (0.1%,0.4%) based on Invisispec under (TSO and RC).

**ISE and STT/SDO/SPT.** Under TSO, STT and SDO incurs (22.5%,32.2%) and (10.9%,15.1%) overheads on (SPEC2017,PARSEC) respectively. ISE-RCP always incurs lower overheads than both STT and SDO even it provides slightly stronger security protection. Under RC, STT and SDO incurs 23.2% and 11.3% overheads, respectively. SPT incurs about 48.5% and 49.6%—considerably higher than ISE-RCP—to ensure the same security property.

**“Speedup” Analysis.** From Figure 12, some benchmarks, e.g., blackschole under Invisispec and freq under RCP, runs faster with ISLE. It is due to the positive “side effects” of specBuf. If a SpecRd issued to L1 cache triggers replacement of a cacheline in a non-secure processor, the specBuf will temporally keep the cache line and the replacement is avoided. As a result, it is possible that an access misses in L1 for non-secure processor while a speculative load (later becomes safe) hits in specBuf. RCP can fully enjoy this benefit given that merge/purge are not in the critical path. For Invisispec, the negative effects of redo access may overshadow the benefit, e.g., incurring overheads in freq and vips.

7.3 Coherence Traffic Analysis
Figure 11: SPEC2017: Performance Overheads under TSO (upper) and RC (bottom)

Figure 12: PARSEC: Performance Overheads under TSO

Figure 13: Traffic Overheads

Figure 13 compares the traffic overheads of RCP, InvisiSpec and CleanupSpec under TSO, normalized to the baseline MESI protocol. We measure the traffic overheads by counting the total number of bytes transferred among the cache system and between cache and the main memory. For RCP, we also count the bytes for each type of the message and show their distribution in Figure 13. RCP incurs on average 26% traffic overheads, while InvisiSpec and CleanupSpec incur 40% and 20%, respectively. Coherence traffic overheads of RCP is mainly attributed to PrMerge, PrPurge, and L1Merge messages. Compared to InvisiSpec, the traffic is decreased because we do not have any traffic caused by the validation and exposure operations. For a correct path, the merge of data does not introduce redundant data movement. Moreover, the merge and purge are performed concurrently with processor execution.

8. CONCLUSION

This paper proposes RCP, a new reversible coherence protocol that ensures invisible speculative load execution (ISE) with low overheads. RCP can be combined with processor mechanisms that eliminate the effects of speculative instructions on other instructions to achieve low-overhead invisible speculative execution (ISE). RCP is designed by systematically extending the existing coherence protocol to incorporate speculative loads and states. The results show that RCP based ISE incurs much lower overheads than STT/SPT while providing similar or stronger protection.

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